1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
A	0001554595	PRODUCTION RELEASED	2012-07-26

iPad 4th Gen

LAST_MODIFIED=Thu Jul 26 10:29:36 2012

PDF	CSA	CONTENTS	SYNC MASTER	DATE	(SYSTEM DRI)
1	1	Table of Contents	N/A	N/A	(AMANDA)
2	2	BLOCK DIAGRAM: SYSTEM	N/A	N/A	(AMANDA)
3	4	BOM TABLES	N/A	N/A	(AMANDA)
4	6	AP: MAIN	N/A	N/A	(TERRY)
5	7	AP: I/Os	N/A	N/A	(AMANDA)
6	8	AP: NAND	N/A	N/A	(TERRY)
7	9	AP: TV,DP,MIPI	N/A	N/A	(TERRY)
8	10	AP: DDR	N/A	N/A	(TERRY)
9	11	AP: POWER	N/A	N/A	(TERRY)
10	12	AP: MISC & ALIASES	N/A	N/A	(TERRY)
11	13	DDR 0 AND 1	N/A	N/A	(TERRY)
12	14	DDR 2 AND 3	N/A	N/A	(AMANDA)
13	16	NAND	N/A	N/A	(AMANDA)
14	21	ALIASES	N/A	N/A	(JOE)
15	22	VIDEO: EDP CONNECTOR	N/A	N/A	(AMANDA)
16	30	GRAPE: GROUNDHOG,CONN,BOOST	N/A	N/A	(AMANDA)
17	31	GRAPE: Z1, Z2	N/A	N/A	(TERRY)
18	36	AUDIO: L81 CODEC	N/A	N/A	(TERRY)
19	37	AUDIO: SPEAKER AMP	N/A	N/A	(MARK)
20	54	SENSOR FLEX CONN	N/A	N/A	(MARK)
21	55	SENSOR CONN FILTERS 1	N/A	N/A	(MARK)
22	56	SENSOR CONN FILTERS 2	N/A	N/A	(JOE)
23	57	E75 DOCK SUPPORT	N/A	N/A	(JOE)
24	58	IO FLEX CONN	N/A	N/A	(JOE)
25	59	TRISTAR	N/A	N/A	(AMANDA)
26	60	CONNECTOR: CELLULAR	N/A	N/A	(MATT)
27	61	WIFI/BT	N/A	N/A	(MADHAVI)
28	75	POWER: BATTERY CONNECTOR	MADHAVI	12/06/2011	(MADHAVI)
29	81	PMU: ADRIANA PAGE 1	MADHAVI	12/06/2011	(MADHAVI)
30	82	PMU: ADRIANA PAGE 2	MADHAVI	12/06/2011	(MADHAVI)
31	83	PMU: ADRIANA PAGE 3	MADHAVI	12/06/2011	(MADHAVI)
32	90	DEBUG/MISC.	MLB	11/09/2011	(AMANDA)
33	93	TEST/HOLES/FIDUCUALS	N/A	N/A	(AMANDA)
34	121	POWER ALIASES	N/A	N/A	(MADHAVI)
35	150	CONSTRAINTS: MLB RULES	MIKE	11/30/2011	(AMANDA)
36	151	CONSTRAINTS: LOW SPEED BUS	MIKE	11/30/2011	(AMANDA)
37	152	CONSTRAINTS: DISPLAY/AUDIO	MIKE	11/30/2011	(AMANDA)
38	153	CONSTRAINTS: DDR/FMI	MIKE	11/30/2011	(AMANDA)
39	154	CONSTRAINTS: POWER / GND	MIKE	11/30/2011	(AMANDA)

DRAWING
MLB
DRAWING

DRAWING TITLE: X140 MLB

Apple Inc.

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REVISION: A.0.0
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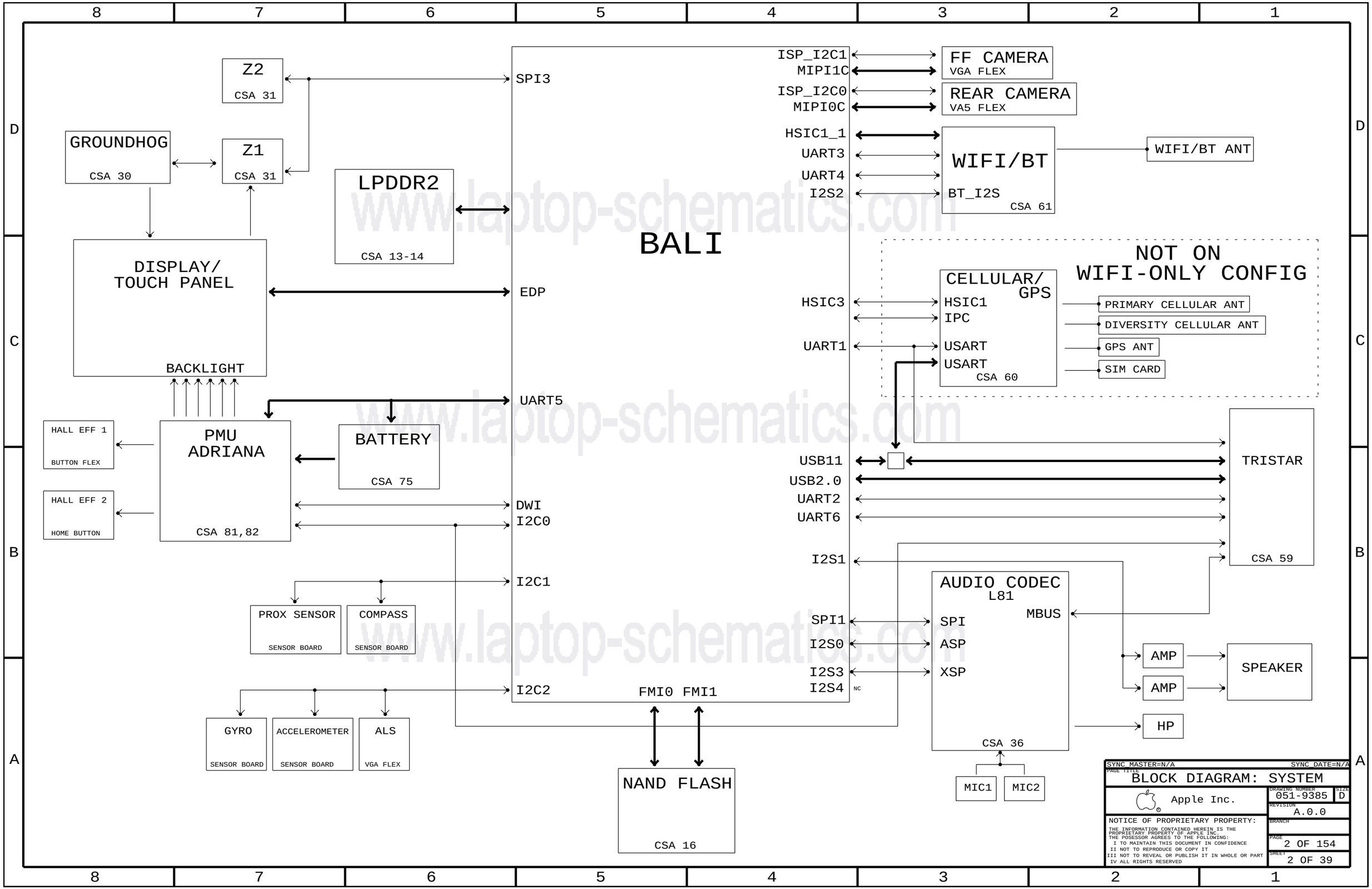

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

BOM OPTIONS

COMMON
ALTERNATE

16GB_PROD: 16GB CONFIG
32GB_PROD: 32GB CONFIG
64GB_PROD: 64 GB CONFIG
DEV: DEV BOARD ONLY

MLB: MLB BOARD ONLY
MLB_A: WIFI ONLY CONFIG
MLB_B: CELLULAR CONFIG
MLB_C: CELLULAR CONFIG
MLB_D: LEGACY CELLULAR CONFIG
MLB_E: LEGACY CELLULAR CONFIG

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE

MECHANICAL PARTS

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
NAND	806-4195	1	FENCE,NAND,TOP,MLB,X140	PD_FENCE_NAND	CRITICAL	
SOC/PMU	806-3493	1	FENCE,LARGE,TOP,MLB,X140	PD_FENCE_LARGE	CRITICAL	
AUDIO	806-3956	1	FENCE,AMP,MLB,X140	PD_FENCE_AMP	CRITICAL	
GRAPE	806-4196	1	FENCE,1,BTM,MLB,X140	PD_FENCE_BTM1	CRITICAL	
MEMORY	806-3492	1	FENCE,2,BTM,MLB,X140	PD_FENCE_BTM2	CRITICAL	

BARCODE LABEL/EEEE CODES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7838	1	EEEE FOR 639-3736 (MLB A 16G)	EEEE_F1WD	CRITICAL	EEEE_MLB_A_16G
825-7838	1	EEEE FOR 639-3737 (MLB A 32G)	EEEE_F1WH	CRITICAL	EEEE_MLB_A_32G
825-7838	1	EEEE FOR 639-3738 (MLB A 64G)	EEEE_F1W8	CRITICAL	EEEE_MLB_A_64G
825-7838	1	EEEE FOR 639-4176 (MLB A 128G)	EEEE_F80Q	CRITICAL	EEEE_MLB_A_128G
825-7838	1	EEEE FOR 639-3263 (MLB B 16G)	EEEE_DWKG	CRITICAL	EEEE_MLB_B_16G
825-7838	1	EEEE FOR 639-3739 (MLB B 32G)	EEEE_F1W7	CRITICAL	EEEE_MLB_B_32G
825-7838	1	EEEE FOR 639-3740 (MLB B 64G)	EEEE_F1WC	CRITICAL	EEEE_MLB_B_64G
825-7838	1	EEEE FOR 639-4177 (MLB B 128G)	EEEE_F80P	CRITICAL	EEEE_MLB_B_128G
825-7838	1	EEEE FOR 639-3741 (MLB C 16G)	EEEE_F1WG	CRITICAL	EEEE_MLB_C_16G
825-7838	1	EEEE FOR 639-3742 (MLB C 32G)	EEEE_F1WF	CRITICAL	EEEE_MLB_C_32G
825-7838	1	EEEE FOR 639-3743 (MLB C 64G)	EEEE_F1W9	CRITICAL	EEEE_MLB_C_64G
825-7838	1	EEEE FOR 639-4178 (MLB C 128G)	EEEE_F80R	CRITICAL	EEEE_MLB_C_128G

SCH AND BOARD P/N

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-9385	1	SCH,MLB,X140	SCH1	CRITICAL	
820-3249	1	PCBF,MLB,X140	PCB1	CRITICAL	

SOC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0598	1	IC,SOC,H5G,FCBGA1089,0.5MM	U0600	CRITICAL	

PMU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0622	1	IC,PMU,ADRIANA,D2018A1,FCBGA	U8100	CRITICAL	

SDRAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0636	2	LPDDR2,533MHZ,512MB,SAMSUNG,38NM	U1300,U1400	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
333S0637	333S0636		U1300,U1400	LPDDR2,533MHZ,HYNIX,38NM
333S0638	333S0636		U1400,U1400	LPDDR2,533MHZ,ELPIDA,38NM

NAND

16GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0878	1	TOSHIBA PPN1.5 16GB	U1600	CRITICAL	16GB_PROD

32GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0879	1	TOSHIBA PPN1.5 32GB	U1600	CRITICAL	32GB_PROD

64GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0880	1	TOSHIBA PPN1.5 64GB	U1600	CRITICAL	64GB_PROD

128GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0912	1	TOSHIBA PPN1.5 128GB	U1600	CRITICAL	128GB_PROD

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
BOM TABLES

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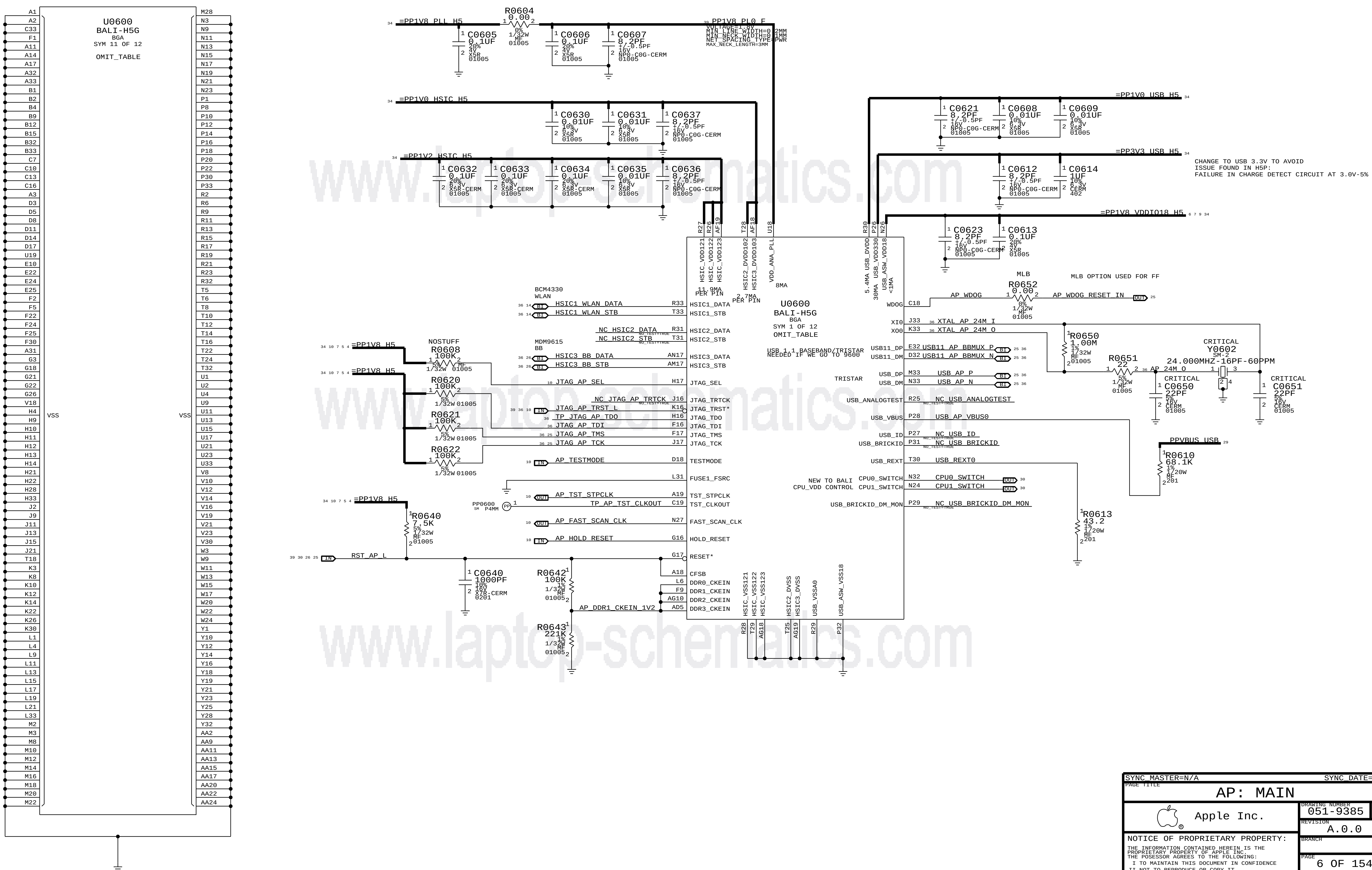

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Apple Inc.	DRAWING NUMBER: 051-9385	SIZE: D
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R0700 33.2 1/32W MF 01005

36 18 OUT I2S0_CODEC_ASP_MCK_R

L81 CODEC ASP
1.8V

R0730 33.2 1/32W MF 01005

19 OUT I2S1_SPKAMP_MCK_R

L19 AMPLIFIERS
1.8V

BT
1.8V

L81 CODEC XSP
1.8V

NOT USED

USED FOR DEBUG
AND SW UPDATE
OS CURRENTLY SUPPORTS
USB1.1 FOR DEBUG.

TO_BB
1.8V IO

R0720 100K 5% 1/20W MF 201

U0600
BALI-H5G
BGA
SYM 3 OF 12
OMIT_TABLE

I2S0_CODEC_ASP_MCK	M27	I2S0_MCK	
I2S0_CODEC_ASP_BCLK	M29	I2S0_BCLK	
I2S0_CODEC_ASP_LRCK	N31	I2S0_LRCK	
I2S0_CODEC_ASP_DIN	M32	I2S0_DIN	
I2S0_CODEC_ASP_DOUT	M26	I2S0_DOUT	
I2S1_SPKAMP_MCK	H30	I2S1_MCK	
I2S1_SPKAMP_BCLK	L24	I2S1_BCLK	
I2S1_SPKAMP_LRCK	L23	I2S1_LRCK	
I2S1_SPKAMP_DIN	M24	I2S1_DIN	
I2S1_SPKAMP_DOUT	N30	I2S1_DOUT	
NC_I2S2_MCK NO_TEST=TRUE	J29	I2S2_MCK	
I2S2_BT_BCLK	L29	I2S2_BCLK	
I2S2_BT_LRCK	L28	I2S2_LRCK	
I2S2_BT_DIN	L26	I2S2_DIN	
I2S2_BT_DOUT	L25	I2S2_DOUT	
NC_I2S3_MCK NO_TEST=TRUE	L32	I2S3_MCK	
I2S3_CODEC_XSP_BCLK	E29	I2S3_BCLK	
I2S3_CODEC_XSP_LRCK	K32	I2S3_LRCK	
I2S3_CODEC_XSP_DIN	J25	I2S3_DIN	
I2S3_CODEC_XSP_DOUT	M30	I2S3_DOUT	
NC_I2S4_MCK NO_TEST=TRUE	F31	I2S4_MCK	
NC_I2S4_BCLK NO_TEST=TRUE	H25	I2S4_BCLK	
NC_I2S4_LRCK NO_TEST=TRUE	K28	I2S4_LRCK	
NC_I2S4_DIN NO_TEST=TRUE	K31	I2S4_DIN	
NC_I2S4_DOUT NO_TEST=TRUE	J32	I2S4_DOUT	
NC_AP_GPIO216 NO_TEST=TRUE	K29	SPDIF	
GPIO_BOARD_ID_2	Y31	SPI0_MISO	
GPIO_BOARD_ID_1	V28	SPI0_MOSI	
GPIO_BOARD_ID_0	V32	SPI0_SCLK	
TP_SPI0_SSIN	V29	SPI0_SSIN	
SPI1_CODEC_MISO	AB29	SPI1_MISO	
SPI1_CODEC_MOSI	Y29	SPI1_MOSI	
SPI1_CODEC_SCLK	AA28	SPI1_SCLK	
SPI1_CODEC_CS_L	AA32	SPI1_SSIN	
BB_JTAG_TRST_RF_L	AB28	SPI2_MISO	
BB_JTAG_TDI_RF	AB33	SPI2_MOSI	
BB_JTAG_TDO_RF	AC29	SPI2_SCLK	
GPIO_BB_HSIC_HOST_RDY	W33	SPI2_SSIN	
SPI3_GRAPE_MISO	D19	SPI3_MISO	
SPI3_GRAPE_MOSI	G20	SPI3_MOSI	
SPI3_GRAPE_SCLK	E19	SPI3_SCLK	
SPI3_GRAPE_CS_L	F19	SPI3_SSIN	

GRAPE
3.0V

I2C0_SCL	Y33	I2C0_SCL_1V8	BI 5 19 25 30 36
I2C0_SDA	U29	I2C0_SDA_1V8	OUT 5 19 25 30 36
I2C1_SCL	W27	I2C1_SCL_1V8	BI 5 22 36
I2C1_SDA	W29	I2C1_SDA_1V8	OUT 5 22 36
I2C2_SCL	H20	I2C2_SCL_3V0	BI 5 22 36
I2C2_SDA	B19	I2C2_SDA_3V0	OUT 5 22 36
SWI_DATA	AB27	NC_SWI_AP NO_TEST=TRUE	
DWI_CLK	T26	DWI_AP_CLK	OUT 30 36
DWI_DI	W32	DWI_AP_DI	IN 30 36
DWI_DO	W28	DWI_AP_DO	OUT 30 36

TO:
TRISTAR 0011010X
ADRIANA_PMU 0111100X
L19 LEFT 1000000X
L19 RIGHT 1000001X

TO SENSOR BOARD:
AD7149 PROX 0101100X
AKM8975B COMPASS 0001110X

TO SENSOR BOARD:
C1805 ALS 0111001X
LIS331DLH ACCEL 0011001X
AP3GDLB GYRO 1101000X

=PP1V8_H5
NOSTUFF
R0760 100K 5% 1/20W MF 201
GPIO_GRAPE_IRQ_L

BUTTON PULLUPS

=PP1V8_S2R_MISC
R0708 220K 5% 1/20W MF 201
GPIO_BTN_HOME_L

=PP1V8_ALWAYS
R0709 220K 5% 1/20W MF 201
GPIO_BTN_ONOFF_L

=PP1V8_S2R_MISC
R0710 220K 5% 1/20W MF 201
GPIO_BTN_SRL_L

GPIO_PMU_KEEPACT
GPIO_FORCE_DFU
GPIO_DFU_STATUS
GPIO_BB_RADIO_ON_L
GPIO_WLAN_HSIC_HOST_RDY
GPIO_SPKAMP_RST_L
GPIO_SPKAMP_KEEPALIVE

R0711 100K 5% 1/20W MF 201
R0713 100K 5% 1/20W MF 201
NOSTUFF R0714 100K 5% 1/20W MF 201
NOSTUFF R0715 100K 5% 1/20W MF 201
R0718 100K 5% 1/20W MF 201
R0719 100K 5% 1/20W MF 201
R0721 100K 5% 1/20W MF 201

OMIT_TABLE
U0600
BALI-H5G
BGA
SYM 2 OF 12

GPIO_BTN_HOME_L	AK20	GPIO0	
GPIO_BTN_ONOFF_L	AJ19	GPIO1	
GPIO_BB_HSIC_DEV_RDY	AK22	GPIO2	
GPIO_BTN_VOL_UP_L	AK19	GPIO3	
GPIO_ALS_IRQ_L	AK21	GPIO4	
GPIO_BT_WAKE	AK24	GPIO5	
GPIO_AP_MODEM_WAKE	AJ21	GPIO6	
BB_JTAG_TMS_RF	AK18	GPIO7	
GPIO_BB_RST_L	AL26	GPIO8	
GPIO_BB_RADIO_ON_L	AH25	GPIO9	
GPIO_BB_RESET_DET_L	AJ18	GPIO10	
GPIO_ACCEL_IRQ2_L	AJ23	GPIO11	
GPIO_BB_HSIC_RESUME	AK23	GPIO12	
GPIO_WLAN_HSIC_HOST_RDY	AJ20	GPIO13	
GPIO_BTN_VOL_DOWN_L	AJ22	GPIO14	
GPIO_BB_GSM_TXBURST	AJ24	GPIO15	
GPIO_BOARD_ID_3	AL25	GPIO16	
PMU_GPIO_TS_INT	AM26	GPIO17	
GPIO_BOOT_CONFIG_0	AK25	GPIO18	
GPIO_BB_GPS_SYNC	AN26	GPIO19	
GPIO_PROX_IRQ_L	F26	GPIO20	
GPIO_GYRO_IRQ1	E26	GPIO21	
GPIO_PMU_KEEPACT	J31	GPIO22	
GPIO_PMU_IRQ_L	F29	GPIO23	
GPIO_WLAN_HSIC_DEV_RDY	E30	GPIO24	
GPIO_BOOT_CONFIG_1	H31	GPIO25	
GPIO_FORCE_DFU	J30	GPIO26	
GPIO_DFU_STATUS	H32	GPIO27	
GPIO_BOOT_CONFIG_2	G27	GPIO28	
GPIO_BOOT_CONFIG_3	E27	GPIO29	
GPIO_BTN_SRL_L	F32	GPIO30	
GPIO_GRAPE_IRQ_L	J28	GPIO31	
GPIO_WL_HSIC_RESUME	G31	GPIO32	
GPIO_SPKAMP_RST_L	G32	GPIO33	
GPIO_SPKAMP_KEEPALIVE	G28	GPIO34	
GPIO_SPKAMP_RIGHT_IRQ_L	G33	GPIO35	
PM_LCDVDD_PWREN	J26	GPIO36	
GPIO_SPKAMP_LEFT_IRQ_L	G30	GPIO37	
SPK_ID	G29	GPIO38	
GPIO_CODEC_IRQ_L	F27	GPIO39	
GPIO_GRAPE_FW_DNLD_EN_L	H19	GPIO_3V0	
GPIO_GRAPE_RST_L	J19	GPIO_3V1	

EHCI_PORT_PWR0	AK28	GPIO_BRD_REV0	IN 10
EHCI_PORT_PWR1	AJ25	GPIO_BRD_REV1	IN 10
EHCI_PORT_PWR2	AK26	GPIO_BRD_REV2	IN 10
EHCI_PORT_PWR3	AK27	NC_EHCI_PORT_PWR3_AP NO_TEST=TRUE	
TMR32_PWM0	V33	GPIO_GYRO_IRQ2	IN 22
TMR32_PWM1	W31	GPIO_ACCEL_IRQ1_L	IN 22
TMR32_PWM2	V27	NC_TMR32_PWM2_AP NO_TEST=TRUE	
UART0_RXD	K18	NC_UART0_RXD NO_TEST=TRUE	
UART0_TXD	K19	NC_UART0_TXD NO_TEST=TRUE	
UART1_CTSN	AM27	UART1_BB_CTS_L	IN 26 36
UART1_RTSN	AM28	UART1_BB_RTS_L	OUT 26 36
UART1_RXD	AN27	UART1_BB_RXD	IN 25 26 36
UART1_TXD	AN28	UART1_BB_TXD	OUT 25 26 36
UART2_CTSN	Y30	BB_JTAG_TCK_RF	OUT 26
UART2_RTSN	AC27	NC_UART2_RTSN NO_TEST=TRUE	
UART2_RXD	AC33	UART2_TS_ACC_RXD	IN 25 36
UART2_TXD	AD33	UART2_TS_ACC_TXD	OUT 25 36
UART3_CTSN	AB32	UART3_BT_CTS_L	IN 14 36
UART3_RTSN	AC30	UART3_BT_RTS_L	OUT 14 36
UART3_RXD	AC32	UART3_BT_RXD	IN 14 36
UART3_TXD	AD32	UART3_BT_TXD	OUT 14 36
UART4_CTSN	Y27	NC_UART4_CTS_L NO_TEST=TRUE	
UART4_RTSN	AA29	NC_UART4_RTC_L NO_TEST=TRUE	
UART4_RXD	AB31	UART4_WLAN_RXD	IN 14 36
UART4_TXD	AC31	UART4_WLAN_TXD	OUT 14 36
UART5_RXD	J18	UART5_BATTERY_TRXD	OUT 28 30
UART5_TXD	K17	NC_UART5_TXD NO_TEST=TRUE	35
UART6_CTSN	AC28	NC_UART6_CTSN NO_TEST=TRUE	
UART6_RTSN	W30	NC_UART6_RTSN NO_TEST=TRUE	
UART6_RXD	AA30	UART6_AP_RXD	IN 25 36
UART6_TXD	AA31	UART6_AP_TXD	OUT 25 36

TO BB UART
MDM9600

TO TRISTAR
1.8V

TO BT UART
BCM4330

WIFI DEBUG

TO TRISTAR
1.8V

GPIO_SVSEL18_FMI	H27	
GPIO_SVSEL25_FMI	G25	
GPIO_VSEL25_I2C2	E31	GPIO_VSEL25_I2C2
GPIO_VSEL25_SPI3	H29	GPIO_VSEL25_SPI3

=PP1V8_H5
R0716 100K 5% 1/20W MF 201
R0717 100K 5% 1/20W MF 201

VSEL18_FMI AND VSEL25_FMI LOW => FMI CHANNEL AT 1.8V
VSEL25_I2C2 HIGH => I2C2 3.0V
VSEL25_SPI3 HIGH => SPI3 3.0V

I2C PULL-UPS

NEED TO CHARACTERIZE RISE TIME
AND SIZE THESE RESISTORS

PP3V0_SENSOR_FLT
=PP1V8_H5
R0701 2.2K 5% 1/32W MF 01005
R0702 2.2K 5% 1/32W MF 01005
R0703 1.00K 5% 1/32W MF 01005
R0704 1.00K 5% 1/32W MF 01005
R0705 1.00K 5% 1/32W MF 01005
R0706 1.00K 5% 1/32W MF 01005

I2C0_SDA_1V8
I2C0_SCL_1V8
I2C1_SDA_1V8
I2C1_SCL_1V8
I2C2_SDA_3V0
I2C2_SCL_3V0

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PAGE TITLE	AP: I/Os
Apple Inc.	DRAWING NUMBER 051-9385 SIZE D
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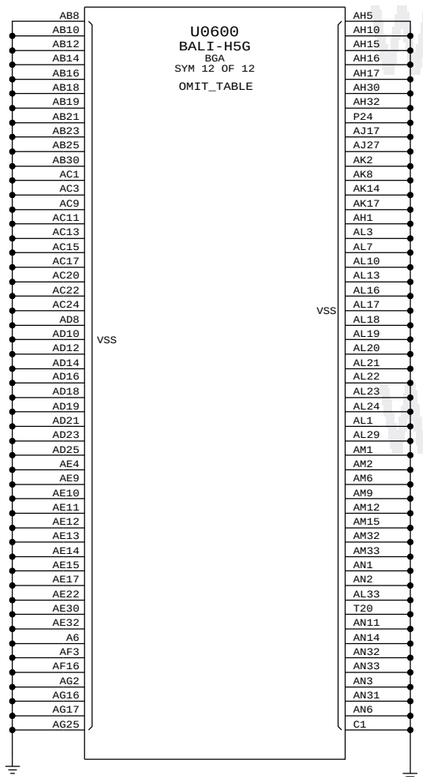

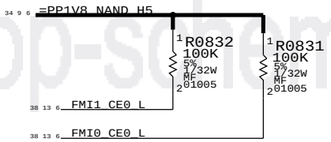

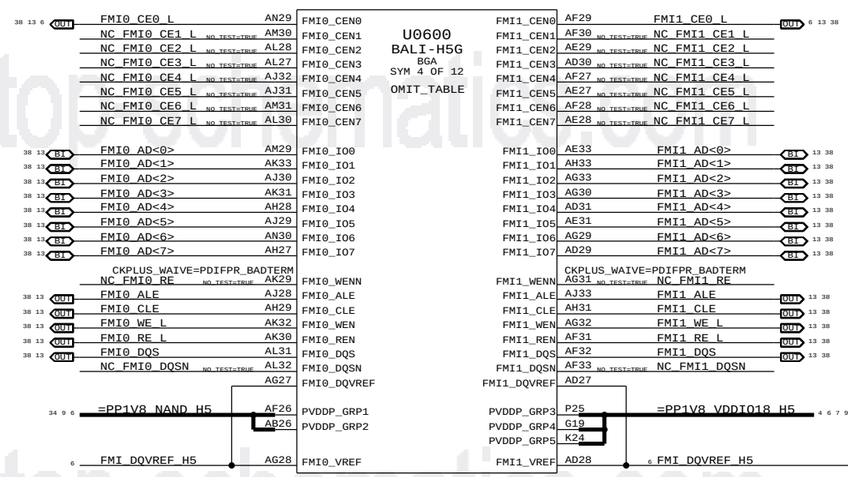

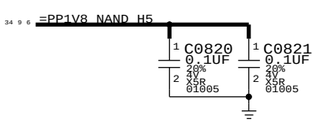

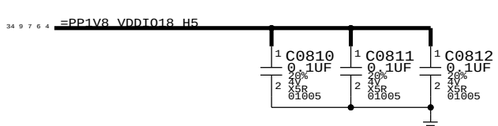

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PAGE TITLE
AP: NAND

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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0725	155S0359	?	FL0910	RDAR://PROBLEM/11104943

=PP1V0_DP_PAD_DVDD_H5 — C0910 8.2PF ±0.1PF% 25V CER 0201

=PP1V8_EDP_H5 — R0911 0 5% 1/20W MF 201 — =PP1V8_EDP_AVDD_AUX

C0931 56PF 5% 6.3V NP0-C0G 01005
C0928 8.2PF ±0.5PF 16V NP0-C0G-CERM 01005
C0929 8.2PF ±0.5PF 16V NP0-C0G-CERM 01005
C0930 56PF 5% 6.3V NP0-C0G 01005
C0932 0.22UF 20% 6.3V X5R 402
C0933 0.22UF 20% 6.3V X5R 402
C0934 0.22UF 20% 6.3V X5R 402

=PP1V8_DP_H5 — C0927 0.1UF 20% 4V X5R 01005 — C0924 56PF 5% 25V NP0-C0G 01005

=PP1V0_EDP_PAD_DVDD_H5 — C0909 0.1UF 10% 6.3V X5R 201

=PP1V8_VDDIO18_H5 — C0953 0.01UF 10% 6.3V X5R 01005

=PP1V8_VDDIO18_H5 — C0951 0.1UF 20% 4V X5R 01005 — C0952 0.01UF 10% 6.3V X5R 01005

NOSTUFF FL0911 240-OHM-0.2A-0.8-OHM 0201 — =PP1V8_VDDIO18_H5 — DAC_AP_COMP_FTR

NOSTUFF C0956 0.1UF 10% 6.3V X5R 201

NOSTUFF C0955 0.1UF 10% 6.3V X5R 201

NOSTUFF R0950 6.34K 1% 1/20W MF 201

DAC_AP_VREF — J23 DAC_VREF
DAC_AP_IREF — J24 DAC_IREF
DAC_AP_COMP — K23 DAC_COMP

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EDP_HPD	E18	EDP_HPD	
EDP_AUX_P	C30	EDP_PAD_AUXP	
EDP_AUX_N	C29	EDP_PAD_AUXN	
EDP_DATA_P<0>	A30	EDP_PAD_TX0P	
EDP_DATA_N<0>	A29	EDP_PAD_TX0N	
EDP_DATA_P<1>	D28	EDP_PAD_TX1P	
EDP_DATA_N<1>	D27	EDP_PAD_TX1N	
EDP_DATA_P<2>	B28	EDP_PAD_TX2P	
EDP_DATA_N<2>	B27	EDP_PAD_TX2N	
EDP_DATA_P<3>	C26	EDP_PAD_TX3P	
EDP_DATA_N<3>	C25	EDP_PAD_TX3N	
AP_EDP_R_BIAS	E28	EDP_PAD_R_BIAS	
	F28	EDP_PAD_DC_TP	

NOTE: 0.6V ANALOG REF

NOSTUFF C0957 0.01UF 10% 6.3V X5R 01005 — R0921 4.99K 1% 1/32W MF 01005

TP_EDP_AP_ANALOG_TEST

DAC_OUT3	D33	NO_TEST=TRUE	NC_DAC_AP_OUT3
DAC_OUT2	E33	NO_TEST=TRUE	NC_DAC_AP_OUT2
DAC_OUT1	F33	NO_TEST=TRUE	NC_DAC_AP_OUT1
DP_HPD	B18	NO_TEST=TRUE	NC_DP_HPD
DP_PAD_AUXP	A26	NO_TEST=TRUE	NC_DP_AUX_P
DP_PAD_AUXN	A25	NO_TEST=TRUE	NC_DP_AUX_N
DP_PAD_TX0P	D24	NO_TEST=TRUE	NC_DP_DATA_P<0>
DP_PAD_TX0N	D23	NO_TEST=TRUE	NC_DP_DATA_N<0>
DP_PAD_TX1P	B24	NO_TEST=TRUE	NC_DP_DATA_P<1>
DP_PAD_TX1N	B23	NO_TEST=TRUE	NC_DP_DATA_N<1>
DP_PAD_TX2P	C22	NO_TEST=TRUE	NC_DP_DATA_P<2>
DP_PAD_TX2N	C21	NO_TEST=TRUE	NC_DP_DATA_N<2>
DP_PAD_TX3P	A22	NO_TEST=TRUE	NC_DP_DATA_P<3>
DP_PAD_TX3N	A21	NO_TEST=TRUE	NC_DP_DATA_N<3>
DP_PAD_R_BIAS	E23		DP_R_BIAS
DP_PAD_DC_TP	F23		TP_DP_AP_ANALOG_TEST

NOTE: 0.6V ANALOG REF

NOSTUFF C0950 0.01UF 10% 6.3V X5R 01005 — R0920 4.99K 1% 1/32W MF 01005

FL0910 80-OHM-0.2A-0.4-OHM 0201-1 — =PP1V0_MIPI_PLL_H5 — PP1V0_MIPI_PLL_F

VOLTAGE=1.0V MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.1MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3MM

C0980 1UF 10% 6.3V CERM 402
C0981 0.01UF 10% 6.3V X5R 01005
C0982 56PF 5% 6.3V NP0-C0G 01005

=PP1V0_MIPI_H5

C0935 1UF 10% 6.3V CERM 402
C0908 0.1UF 10% 6.3V X5R 201
C0903 0.1UF 10% 6.3V X5R 201
C0904 1.7PF ±0.5PF 16V NP0-C0G-CERM 01005

=PP1V8_MIPI_H5 — C0907 0.1UF 10% 6.3V X5R 201

PP0V4_MIPI1D — C0960 2.2NF 10% 16V X5R-CERM 0201

VOLTAGE=0.4V MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.1MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3MM

C0961 2.2NF 10% 16V X5R-CERM 0201

40MA MIPI_VDD10 — 2.2MA MIPI10D_VDD10_PLL — 2.2MA MIPI11D_VDD10_PLL — 2MA MIPI10D_VDD18 — 2MA MIPI11D_VDD18 — 2MA PER PIN — MIPI10D_VREG_0P4V — MIPI11D_VREG_0P4V — MIPI_VSS

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=PP1V8_H5

R0930 1.00K 1% 1/32W MF 01005
R0931 1.00K 1% 1/32W MF 01005
R0932 1.00K 1% 1/32W MF 01005
R0933 1.00K 1% 1/32W MF 01005

NC_MIPI_VSYNC_H5	U27	NO_TEST=TRUE	MIPI_VSYNC
MIPI0C_CAM_RF_DATA_P<0>	AM22		MIPI0C_DPDATA0
MIPI0C_CAM_RF_DATA_N<0>	AN22		MIPI0C_DNDATA0
MIPI0C_CAM_RF_DATA_P<1>	AM21		MIPI0C_DPDATA1
MIPI0C_CAM_RF_DATA_N<1>	AN21		MIPI0C_DNDATA1
NC_MIPI0C_CAM_RF_DATA_P<2>	AM19	NO_TEST=TRUE	MIPI0C_DPDATA2
NC_MIPI0C_CAM_RF_DATA_N<2>	AN19	NO_TEST=TRUE	MIPI0C_DNDATA2
NC_MIPI0C_CAM_RF_DATA_P<3>	AM18	NO_TEST=TRUE	MIPI0C_DPDATA3
NC_MIPI0C_CAM_RF_DATA_N<3>	AN18	NO_TEST=TRUE	MIPI0C_DNDATA3
MIPI0C_CAM_RF_CLK_P	AM20		MIPI0C_DPCLK
MIPI0C_CAM_RF_CLK_N	AN20		MIPI0C_DNCLK

ISP0_FLASH	M25		ISP0_CAM_RF_RST_L
ISP0_PRE_FLASH	M31	NO_TEST=TRUE	NC_ISP0_CAM_RF_FLASH
ISP0_SCL	AA27		ISP0_CAM_RF_I2C_SCL
ISP0_SDA	U28		ISP0_CAM_RF_I2C_SDA
			REAR FACING CAM
ISP1_FLASH	N25	SOCHOT1_L	
ISP1_PRE_FLASH	L30	SOCHOT0_L	
ISP1_SCL	AA33		ISP1_CAM_FF_I2C_SCL
ISP1_SDA	U30		ISP1_CAM_FF_I2C_SDA
			FRONT FACING CAM
SENSOR0_CLK	V31	ISP0_CAM_RF_CLK_R	0.00 2MF 1/32W 01005 ISP0_CAM_RF_CLK
SENSOR0_RST	U32		ISP0_CAM_RF_SHUTDOWN
SENSOR1_CLK	U31	ISP1_CAM_FF_CLK_R	0.00 2MF 1/32W 01005 ISP1_CAM_FF_CLK
SENSOR1_RST	T27		ISP1_CAM_FF_SHUTDOWN_L

SHUTDOWN IS ACTIVE HIGH

SHUTDOWN IS ACTIVE LOW

MIPI1C_DPDATA0	AM23	MIPI1C_CAM_FF_DATA_P<0>	
MIPI1C_DNDATA0	AN23	MIPI1C_CAM_FF_DATA_N<0>	
MIPI1C_DPDATA1	AM25	NO_TEST=TRUE	NC_MIPI1C_CAM_FF_DATA_P<1>
MIPI1C_DNDATA1	AN25	NO_TEST=TRUE	NC_MIPI1C_CAM_FF_DATA_N<1>
MIPI1C_DPCLK	AM24	MIPI1C_CAM_FF_CLK_P	
MIPI1C_DNCLK	AN24	MIPI1C_CAM_FF_CLK_N	

=PP1V8_H5 — NOSTUFF R0942 100K 5% 1/32W MF 01005 — R0941 100K 5% 1/32W MF 01005

SOCHOT1_L PULL-UP ON CSA 90

SOCHOT1_L — SOCHOT0_L

SYNC_MASTER=N/A	SYNC_DATE=N/A
PAGE TITLE	AP: TV,DP,MIPI
Apple Inc.	DRAWING NUMBER 051-9385 SIZE D
	REVISION A.0.0
	BRANCH
	PAGE 9 OF 154
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OMIT_TABLE

DDR0_DQ<0>	B14	DDR0_DQ0	H2	DDR1_DQ0	DDR1_DQ<0>
DDR0_DQ<1>	B13	DDR0_DQ1	H3	DDR1_DQ1	DDR1_DQ<1>
DDR0_DQ<2>	D13	DDR0_DQ2	J3	DDR1_DQ2	DDR1_DQ<2>
DDR0_DQ<3>	C12	DDR0_DQ3	J4	DDR1_DQ3	DDR1_DQ<3>
DDR0_DQ<4>	D12	DDR0_DQ4	K2	DDR1_DQ4	DDR1_DQ<4>
DDR0_DQ<5>	B11	DDR0_DQ5	L2	DDR1_DQ5	DDR1_DQ<5>
DDR0_DQ<6>	C11	DDR0_DQ6	K4	DDR1_DQ6	DDR1_DQ<6>
DDR0_DQ<7>	B10	DDR0_DQ7	K5	DDR1_DQ7	DDR1_DQ<7>
DDR0_DQ<8>	C9	DDR0_DQ8	N2	DDR1_DQ8	DDR1_DQ<8>
DDR0_DQ<9>	D9	DDR0_DQ9	P2	DDR1_DQ9	DDR1_DQ<9>
DDR0_DQ<10>	B8	DDR0_DQ10	P3	DDR1_DQ10	DDR1_DQ<10>
DDR0_DQ<11>	C8	DDR0_DQ11	R3	DDR1_DQ11	DDR1_DQ<11>
DDR0_DQ<12>	B7	DDR0_DQ12	T2	DDR1_DQ12	DDR1_DQ<12>
DDR0_DQ<13>	B6	DDR0_DQ13	R4	DDR1_DQ13	DDR1_DQ<13>
DDR0_DQ<14>	C6	DDR0_DQ14	T3	DDR1_DQ14	DDR1_DQ<14>
DDR0_DQ<15>	D7	DDR0_DQ15	T4	DDR1_DQ15	DDR1_DQ<15>
DDR0_DQ<16>	B17	DDR0_DQ16	C2	DDR1_DQ16	DDR1_DQ<16>
DDR0_DQ<17>	C17	DDR0_DQ17	D2	DDR1_DQ17	DDR1_DQ<17>
DDR0_DQ<18>	B16	DDR0_DQ18	E2	DDR1_DQ18	DDR1_DQ<18>
DDR0_DQ<19>	E17	DDR0_DQ19	E4	DDR1_DQ19	DDR1_DQ<19>
DDR0_DQ<20>	D16	DDR0_DQ20	E3	DDR1_DQ20	DDR1_DQ<20>
DDR0_DQ<21>	E16	DDR0_DQ21	F3	DDR1_DQ21	DDR1_DQ<21>
DDR0_DQ<22>	C15	DDR0_DQ22	F4	DDR1_DQ22	DDR1_DQ<22>
DDR0_DQ<23>	D15	DDR0_DQ23	G2	DDR1_DQ23	DDR1_DQ<23>
DDR0_DQ<24>	E6	DDR0_DQ24	U3	DDR1_DQ24	DDR1_DQ<24>
DDR0_DQ<25>	B5	DDR0_DQ25	V2	DDR1_DQ25	DDR1_DQ<25>
DDR0_DQ<26>	C5	DDR0_DQ26	V3	DDR1_DQ26	DDR1_DQ<26>
DDR0_DQ<27>	E5	DDR0_DQ27	U5	DDR1_DQ27	DDR1_DQ<27>
DDR0_DQ<28>	C4	DDR0_DQ28	V4	DDR1_DQ28	DDR1_DQ<28>
DDR0_DQ<29>	D4	DDR0_DQ29	V5	DDR1_DQ29	DDR1_DQ<29>
DDR0_DQ<30>	B3	DDR0_DQ30	U6	DDR1_DQ30	DDR1_DQ<30>
DDR0_DQ<31>	C3	DDR0_DQ31	V6	DDR1_DQ31	DDR1_DQ<31>
DDR0_CA<0>	G5	DDR0_CA0	E15	DDR1_CA0	DDR1_CA<0>
DDR0_CA<1>	G6	DDR0_CA1	F15	DDR1_CA1	DDR1_CA<1>
DDR0_CA<2>	H5	DDR0_CA2	F14	DDR1_CA2	DDR1_CA<2>
DDR0_CA<3>	H6	DDR0_CA3	E14	DDR1_CA3	DDR1_CA<3>
DDR0_CA<4>	J5	DDR0_CA4	F13	DDR1_CA4	DDR1_CA<4>
DDR0_CA<5>	M5	DDR0_CA5	E8	DDR1_CA5	DDR1_CA<5>
DDR0_CA<6>	M6	DDR0_CA6	F8	DDR1_CA6	DDR1_CA<6>
DDR0_CA<7>	N6	DDR0_CA7	F7	DDR1_CA7	DDR1_CA<7>
DDR0_CA<8>	P5	DDR0_CA8	E7	DDR1_CA8	DDR1_CA<8>
DDR0_CA<9>	P6	DDR0_CA9	F6	DDR1_CA9	DDR1_CA<9>
DDR0_DM<0>	E12	DDR0_DM0	L5	DDR1_DM0	DDR1_DM<0>
DDR0_DM<1>	E9	DDR0_DM1	N5	DDR1_DM1	DDR1_DM<1>
DDR0_DM<2>	C14	DDR0_DM2	G4	DDR1_DM2	DDR1_DM<2>
DDR0_DM<3>	D6	DDR0_DM3	R5	DDR1_DM3	DDR1_DM<3>
DDR0_DQS_P<0>	A13	DDR0_PDQS0	G1	DDR1_PDQS0	DDR1_DQS_P<0>
DDR0_DQS_N<0>	A12	DDR0_NDQS0	H1	DDR1_NDQS0	DDR1_DQS_N<0>
DDR0_DQS_P<1>	A7	DDR0_PDQS1	N1	DDR1_PDQS1	DDR1_DQS_P<1>
DDR0_DQS_N<1>	A8	DDR0_NDQS1	M1	DDR1_NDQS1	DDR1_DQS_N<1>
DDR0_DQS_P<2>	A16	DDR0_PDQS2	D1	DDR1_PDQS2	DDR1_DQS_P<2>
DDR0_DQS_N<2>	A15	DDR0_NDQS2	E1	DDR1_NDQS2	DDR1_DQS_N<2>
DDR0_DQS_P<3>	A4	DDR0_PDQS3	T1	DDR1_PDQS3	DDR1_DQS_P<3>
DDR0_DQS_N<3>	A5	DDR0_NDQS3	R1	DDR1_NDQS3	DDR1_DQS_N<3>
DDR0_CK_P	P4	DDR0_CK	F11	DDR1_CK	DDR1_CK_P
DDR0_CK_N	N4	DDR0_CKB	F12	DDR1_CKB	DDR1_CK_N
DDR0_CKE<0>	J1	DDR0_CKE0	A10	DDR1_CKE0	DDR1_CKE<0>
NC_DDR0_CKE<1> NO_TEST=TRUE	K1	DDR0_CKE1	A9 NO_TEST=TRUE	DDR1_CKE1	NC_DDR1_CKE<1>
H5G_DDR0_ZQ	M4	DDR0_RREF	E11	DDR1_RREF	H5G_DDR1_ZQ
DDR0_CSN0<0>	K6	DDR0_CSN0	F10	DDR1_CSN0	DDR1_CSN<0>
NC_DDR0_CSN<1> NO_TEST=TRUE	J6	DDR0_CSN1	E13 NO_TEST=TRUE	DDR1_CSN1	NC_DDR1_CSN<1>
PPVREF_DDR0_DQ_H5	D10	DDR0_VREF_DQ	L3	DDR1_VREF_DQ	PPVREF_DDR1_DQ_H5
=PP1V2_S2R_H5	H15	DDR0_VDD_CKE	H8	DDR1_VDD_CKE	=PP1V2_S2R_H5

R1020 240 1% 1/20W MF 01005 2
C1020 0.22UF 20% 6.3V X5R 0201 2
C1021 0.22UF 20% 6.3V X5R 0201 2
R1021 240 1% 1/20W MF 01005 2

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OMIT_TABLE

DDR2_DQ<0>	AB2	DDR2_DQ0	AL8	DDR3_DQ0	DDR3_DQ<0>
DDR2_DQ<1>	AB3	DDR2_DQ1	AL9	DDR3_DQ1	DDR3_DQ<1>
DDR2_DQ<2>	AC2	DDR2_DQ2	AK9	DDR3_DQ2	DDR3_DQ<2>
DDR2_DQ<3>	AC4	DDR2_DQ3	AJ9	DDR3_DQ3	DDR3_DQ<3>
DDR2_DQ<4>	AD2	DDR2_DQ4	AM10	DDR3_DQ4	DDR3_DQ<4>
DDR2_DQ<5>	AD3	DDR2_DQ5	AJ10	DDR3_DQ5	DDR3_DQ<5>
DDR2_DQ<6>	AE2	DDR2_DQ6	AK10	DDR3_DQ6	DDR3_DQ<6>
DDR2_DQ<7>	AE3	DDR2_DQ7	AL11	DDR3_DQ7	DDR3_DQ<7>
DDR2_DQ<8>	AF2	DDR2_DQ8	AM11	DDR3_DQ8	DDR3_DQ<8>
DDR2_DQ<9>	AF4	DDR2_DQ9	AL12	DDR3_DQ9	DDR3_DQ<9>
DDR2_DQ<10>	AG5	DDR2_DQ10	AK12	DDR3_DQ10	DDR3_DQ<10>
DDR2_DQ<11>	AH2	DDR2_DQ11	AJ12	DDR3_DQ11	DDR3_DQ<11>
DDR2_DQ<12>	AJ2	DDR2_DQ12	AM13	DDR3_DQ12	DDR3_DQ<12>
DDR2_DQ<13>	AG3	DDR2_DQ13	AK13	DDR3_DQ13	DDR3_DQ<13>
DDR2_DQ<14>	AH3	DDR2_DQ14	AJ13	DDR3_DQ14	DDR3_DQ<14>
DDR2_DQ<15>	AJ3	DDR2_DQ15	AJ14	DDR3_DQ15	DDR3_DQ<15>
DDR2_DQ<16>	W2	DDR2_DQ16	AM5	DDR3_DQ16	DDR3_DQ<16>
DDR2_DQ<17>	W4	DDR2_DQ17	AL6	DDR3_DQ17	DDR3_DQ<17>
DDR2_DQ<18>	Y2	DDR2_DQ18	AK6	DDR3_DQ18	DDR3_DQ<18>
DDR2_DQ<19>	Y3	DDR2_DQ19	AJ6	DDR3_DQ19	DDR3_DQ<19>
DDR2_DQ<20>	Y4	DDR2_DQ20	AM7	DDR3_DQ20	DDR3_DQ<20>
DDR2_DQ<21>	AA3	DDR2_DQ21	AK7	DDR3_DQ21	DDR3_DQ<21>
DDR2_DQ<22>	AA4	DDR2_DQ22	AJ7	DDR3_DQ22	DDR3_DQ<22>
DDR2_DQ<23>	AA5	DDR2_DQ23	AM8	DDR3_DQ23	DDR3_DQ<23>
DDR2_DQ<24>	AK3	DDR2_DQ24	AM14	DDR3_DQ24	DDR3_DQ<24>
DDR2_DQ<25>	AL2	DDR2_DQ25	AL14	DDR3_DQ25	DDR3_DQ<25>
DDR2_DQ<26>	AM3	DDR2_DQ26	AJ15	DDR3_DQ26	DDR3_DQ<26>
DDR2_DQ<27>	AM4	DDR2_DQ27	AK15	DDR3_DQ27	DDR3_DQ<27>
DDR2_DQ<28>	AL4	DDR2_DQ28	AL15	DDR3_DQ28	DDR3_DQ<28>
DDR2_DQ<29>	AL5	DDR2_DQ29	AJ16	DDR3_DQ29	DDR3_DQ<29>
DDR2_DQ<30>	AK5	DDR2_DQ30	AK16	DDR3_DQ30	DDR3_DQ<30>
DDR2_DQ<31>	AJ5	DDR2_DQ31	AM16	DDR3_DQ31	DDR3_DQ<31>
DDR2_CA<0>	AH6	DDR2_CA0	W5	DDR3_CA0	DDR3_CA<0>
DDR2_CA<1>	AG6	DDR2_CA1	W6	DDR3_CA1	DDR3_CA<1>
DDR2_CA<2>	AH7	DDR2_CA2	Y5	DDR3_CA2	DDR3_CA<2>
DDR2_CA<3>	AG7	DDR2_CA3	Y6	DDR3_CA3	DDR3_CA<3>
DDR2_CA<4>	AH8	DDR2_CA4	AA6	DDR3_CA4	DDR3_CA<4>
DDR2_CA<5>	AH11	DDR2_CA5	AD6	DDR3_CA5	DDR3_CA<5>
DDR2_CA<6>	AG11	DDR2_CA6	AE5	DDR3_CA6	DDR3_CA<6>
DDR2_CA<7>	AG12	DDR2_CA7	AE6	DDR3_CA7	DDR3_CA<7>
DDR2_CA<8>	AH12	DDR2_CA8	AF6	DDR3_CA8	DDR3_CA<8>
DDR2_CA<9>	AG13	DDR2_CA9	AF5	DDR3_CA9	DDR3_CA<9>
DDR2_DM<0>	AD4	DDR2_DM0	AK11	DDR3_DM0	DDR3_DM<0>
DDR2_DM<1>	AG4	DDR2_DM1	AG14	DDR3_DM1	DDR3_DM<1>
DDR2_DM<2>	AB6	DDR2_DM2	AJ8	DDR3_DM2	DDR3_DM<2>
DDR2_DM<3>	AK4	DDR2_DM3	AG15	DDR3_DM3	DDR3_DM<3>
DDR2_DQS_P<0>	AA1	DDR2_PDQS0	AN7	DDR3_PDQS0	DDR3_DQS_P<0>
DDR2_DQS_N<0>	AB1	DDR2_NDQS0	AN8	DDR3_NDQS0	DDR3_DQS_N<0>
DDR2_DQS_P<1>	AG1	DDR2_PDQS1	AN13	DDR3_PDQS1	DDR3_DQS_P<1>
DDR2_DQS_N<1>	AF1	DDR2_NDQS1	AN12	DDR3_NDQS1	DDR3_DQS_N<1>
DDR2_DQS_P<2>	V1	DDR2_PDQS2	AN4	DDR3_PDQS2	DDR3_DQS_P<2>
DDR2_DQS_N<2>	W1	DDR2_NDQS2	AN5	DDR3_NDQS2	DDR3_DQS_N<2>
DDR2_DQS_P<3>	AK1	DDR2_PDQS3	AN16	DDR3_PDQS3	DDR3_DQS_P<3>
DDR2_DQS_N<3>	AJ1	DDR2_NDQS3	AN15	DDR3_NDQS3	DDR3_DQS_N<3>
DDR2_CK_P	AH14	DDR2_CK	AH4	DDR3_CK	DDR3_CK_P
DDR2_CK_N	AH13	DDR2_CKB	AJ4	DDR3_CKB	DDR3_CK_N
DDR2_CKE<0>	AN10	DDR2_CKE0	AD1	DDR3_CKE0	DDR3_CKE<0>
NC_DDR2_CKE<1> NO_TEST=TRUE	AN9	DDR2_CKE1	AE1 NO_TEST=TRUE	DDR3_CKE1	NC_DDR3_CKE<1>
H5G_DDR2_ZQ	AH9	DDR2_RREF	AB5	DDR3_RREF	H5G_DDR3_ZQ
DDR2_CSN0<0>	AG9	DDR2_CSN0	AC6	DDR3_CSN0	DDR3_CSN<0>
NC_DDR2_CSN<1> NO_TEST=TRUE	AG8	DDR2_CSN1	AC5 NO_TEST=TRUE	DDR3_CSN1	NC_DDR3_CSN<1>
PPVREF_DDR2_DQ_H5	AB4	DDR2_VREF_DQ	AJ11	DDR3_VREF_DQ	PPVREF_DDR3_DQ_H5
=PP1V2_S2R_H5	Y8	DDR2_VDD_CKE	AE8	DDR3_VDD_CKE	=PP1V2_S2R_H5

R1022 240 1% 1/20W MF 01005 2
C1022 0.22UF 20% 6.3V X5R 0201 2
C1023 0.22UF 20% 6.3V X5R 0201 2
R10234 240 1% 1/20W MF 01005 2

=PP1V2_VDDIOD_H5

R1053 4.7K 1% 1/32W MF 01005 2
C1057 0.01UF 10% 6.3V X5R 01005 2
PPVREF_DDR0_DQ_H5
R1054 4.7K 1% 1/32W MF 01005 2
C1054 0.01UF 10% 6.3V X5R 01005 2

VOLTAGE=0.6V
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.3MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

=PP1V2_VDDIOD_H5

R1055 4.7K 1% 1/32W MF 01005 2
C1058 0.01UF 10% 6.3V X5R 01005 2
PPVREF_DDR1_DQ_H5
R1056 4.7K 1% 1/32W MF 01005 2
C1056 0.01UF 10% 6.3V X5R 01005 2

VOLTAGE=0.6V
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.3MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

=PP1V2_VDDIOD_H5

R1083 4.7K 1% 1/32W MF 01005 2
C1085 0.01UF 10% 6.3V X5R 01005 2
PPVREF_DDR2_DQ_H5
R1084 4.7K 1% 1/32W MF 01005 2
C1084 0.01UF 10% 6.3V X5R 01005 2

VOLTAGE=0.6V
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.3MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

=PP1V2_VDDIOD_H5

R1095 4.7K 1% 1/32W MF 01005 2
C1095 0.01UF 10% 6.3V X5R 01005 2
PPVREF_DDR3_DQ_H5
R1096 4.7K 1% 1/32W MF 01005 2
C1096 0.01UF 10% 6.3V X5R 01005 2

VOLTAGE=0.6V
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.3MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
AP: DDR

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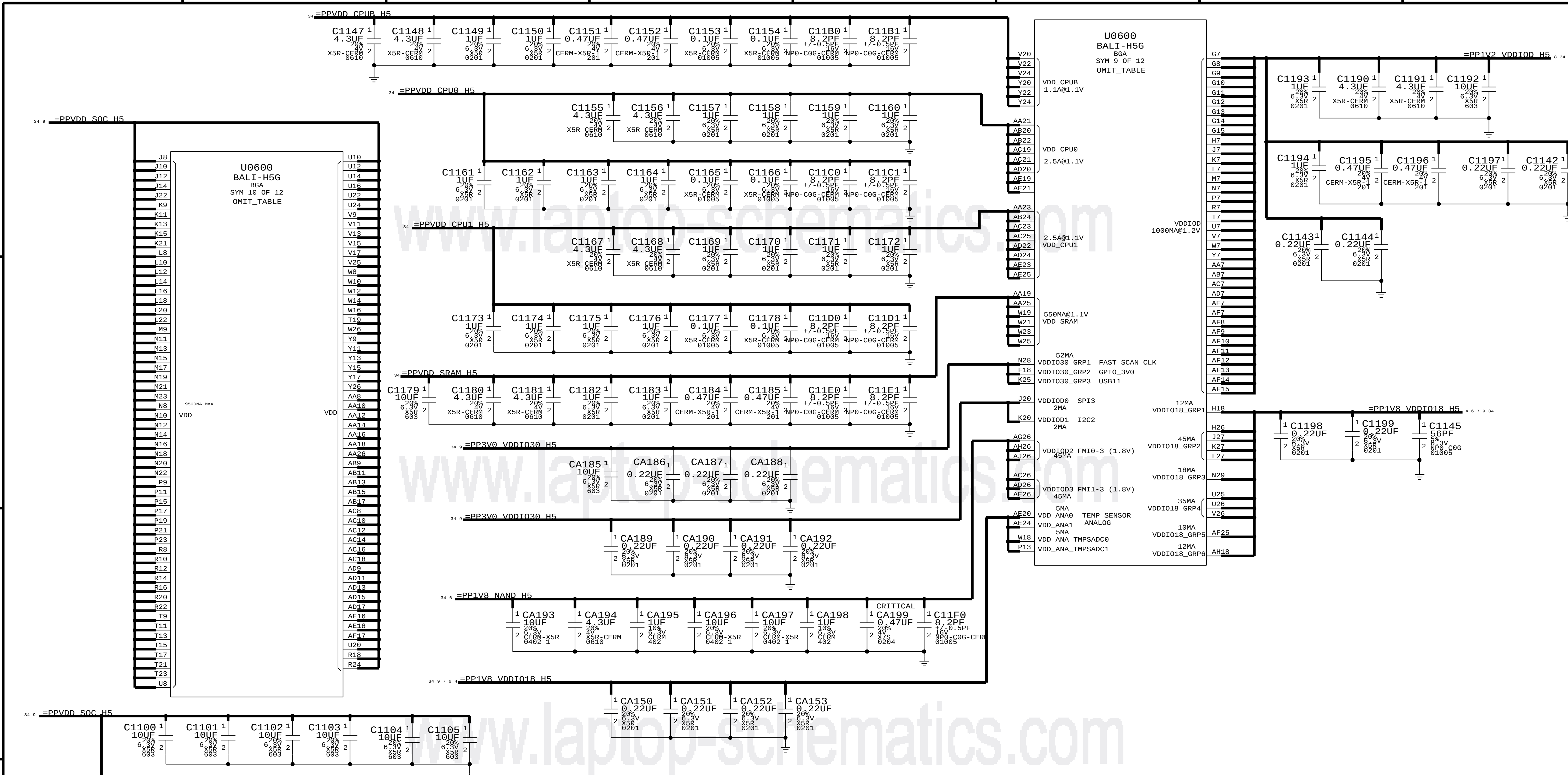

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0702	138S0657			QTY 21 RDAR://PROBLEM/8837828

C1106,C1107,C1108,C1109,C1110,C1111,C1147,C1148,C1155,C1156,C1167,C1168,C1180,C1181,C1190,C1191,C1315,C1321,C1415,C1421,CA194

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE

AP: POWER

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NOTICE OF PROPRIETARY PROPERTY:

BOOT CONFIG ID

=PP1V8_H5

STUFF FOR FORM FACTOR BOARD

R1200	10K 5% 1/32W MF 01005	STUFF FOR FORM FACTOR BOARD
R1201	10K 5% 1/32W MF 01005	STUFF FOR FORM FACTOR BOARD
R1202	10K 5% 1/32W MF 01005	NOSTUFF
R1203	10K 5% 1/32W MF 01005	NOSTUFF

BOOT_CONFIG[3]	GPIO_BOOT_CONFIG_3
BOOT_CONFIG[2]	GPIO_BOOT_CONFIG_2
BOOT_CONFIG[1]	GPIO_BOOT_CONFIG_1
BOOT_CONFIG[0]	GPIO_BOOT_CONFIG_0

BOOT_CONFIG[3-0]

CURRENT SETTING ---> 1100	FMI0/1 2/2 CS
1101	FMI0/1 4/4 CS
1110	FMI0/1 4/4 CS WITH TEST

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

FOR REFERENCE

BOOT_CONFIG[3:0]

0000	SPI0
0001	SPI1
0010	SPI0 W/TEST
0011	SPI1 W/TEST
0100	FMI0 2CS
0101	FMI0 4CS
0110	FMI0 4CS W/TEST
0111	RESERVED
1000	FMI1 2 CS
1001	FMI1 4 CS
1010	FMI1 4CS W/TEST
1100	FMI0/1 2/2 CS
1101	FMI0/1 4/4 CS
1110	FMI0/1 4/4 CS W/TEST
1111	RESERVED

BOARD ID

=PP1V8_H5

R1220	10K 5% 1/32W MF 01005	MLB_D&MLB_E
R1204	10K 5% 1/32W MF 01005	MLB_C&MLB_E
R1205	10K 5% 1/32W MF 01005	MLB_B&MLB_D
R1206	10K 5% 1/32W MF 01005	DEV

BOARD_ID[3]	GPIO_BOARD_ID_3
BOARD_ID[2]	GPIO_BOARD_ID_2
BOARD_ID[1]	GPIO_BOARD_ID_1
BOARD_ID[0]	GPIO_BOARD_ID_0

BOARD_ID[3-0]

0000	X140 AP WLAN (MLB A)
0001	X140 DEV WLAN
0010	X140 AP BB_41 (MLB B)
0011	X140 DEV BB_41
0100	X140 AP BB_42 (MLB C)
0101	X140 DEV BB_42
1010	X140 AP BB_26A (MLB D)
1011	X140 DEV BB_26A
1110	X140 AP BB_26 (MLB E)
1111	X140 DEV BB_26

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

BOARD REVISION

GPIO_BRD_REV2		
GPIO_BRD_REV1		
GPIO_BRD_REV0		
	R1207	NOSTUFF 10K 5% 1/32W 0F 01005
	R1208	NOSTUFF 10K 5% 1/32W 0F 01005
	R1209	10K 5% 1/32W 0F 01005

BRD_REV[2-0]

000	PROTO
001	PROTO 2
010	EVT
CURRENT SETTING ---> 011	DVT

S/W READ FLOW

1. SET GPIO AS INPUT
2. ENABLE PU AND DISABLE PD
3. READ

JTAG

R1210	100 5% 1/32W MF 01005	JTAG_AP_SEL
R1211	100 5% 1/32W MF 01005	JTAG_AP_TRST_L

R1260	100K 5% 1/32W MF 01005
	AP_TESTMODE
XW1200	NOSTUFF SHORT-01005
	AP_TST_STPCLK
XW1201	NOSTUFF SHORT-01005
	AP_FAST_SCAN_CLK
XW1202	NOSTUFF SHORT-01005
	AP_HOLD_RESET

USB_BRICKID — MAKE_BASE=TRUE — PMU_USB_BRICKID

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: AP: MISC & ALIASES

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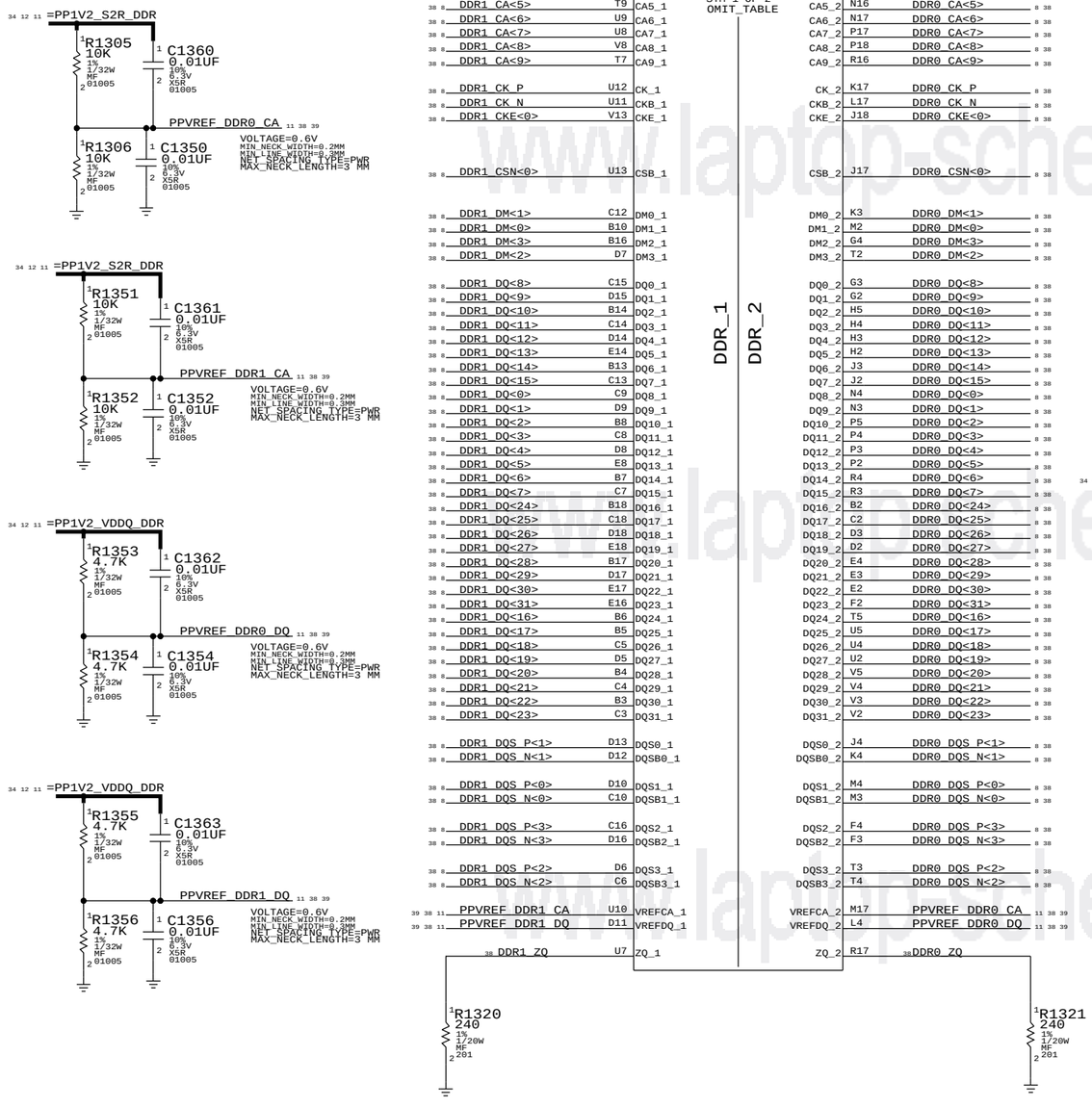

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
DDR 0 AND 1

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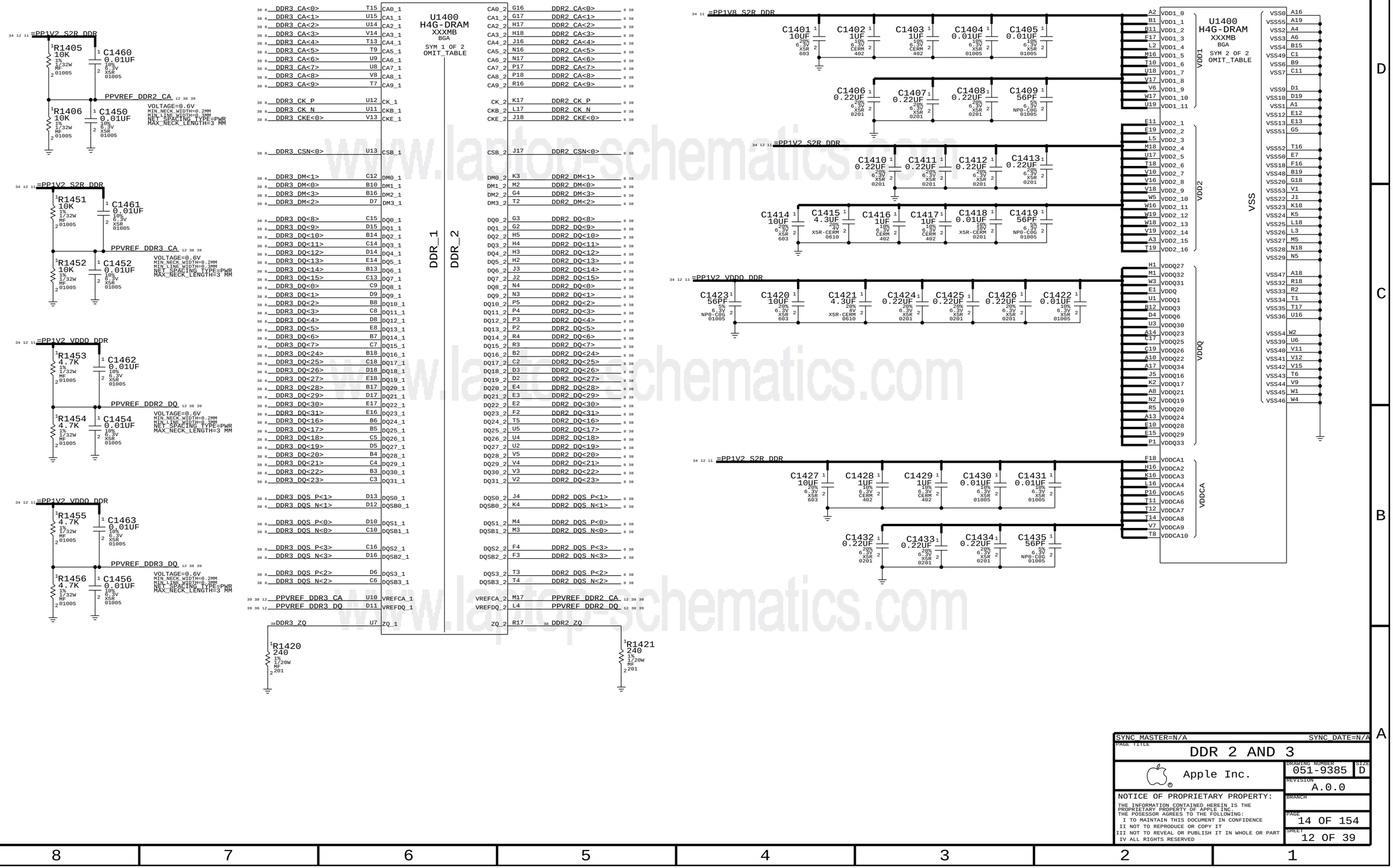

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: DDR 2 AND 3

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REVISION: A.0.0

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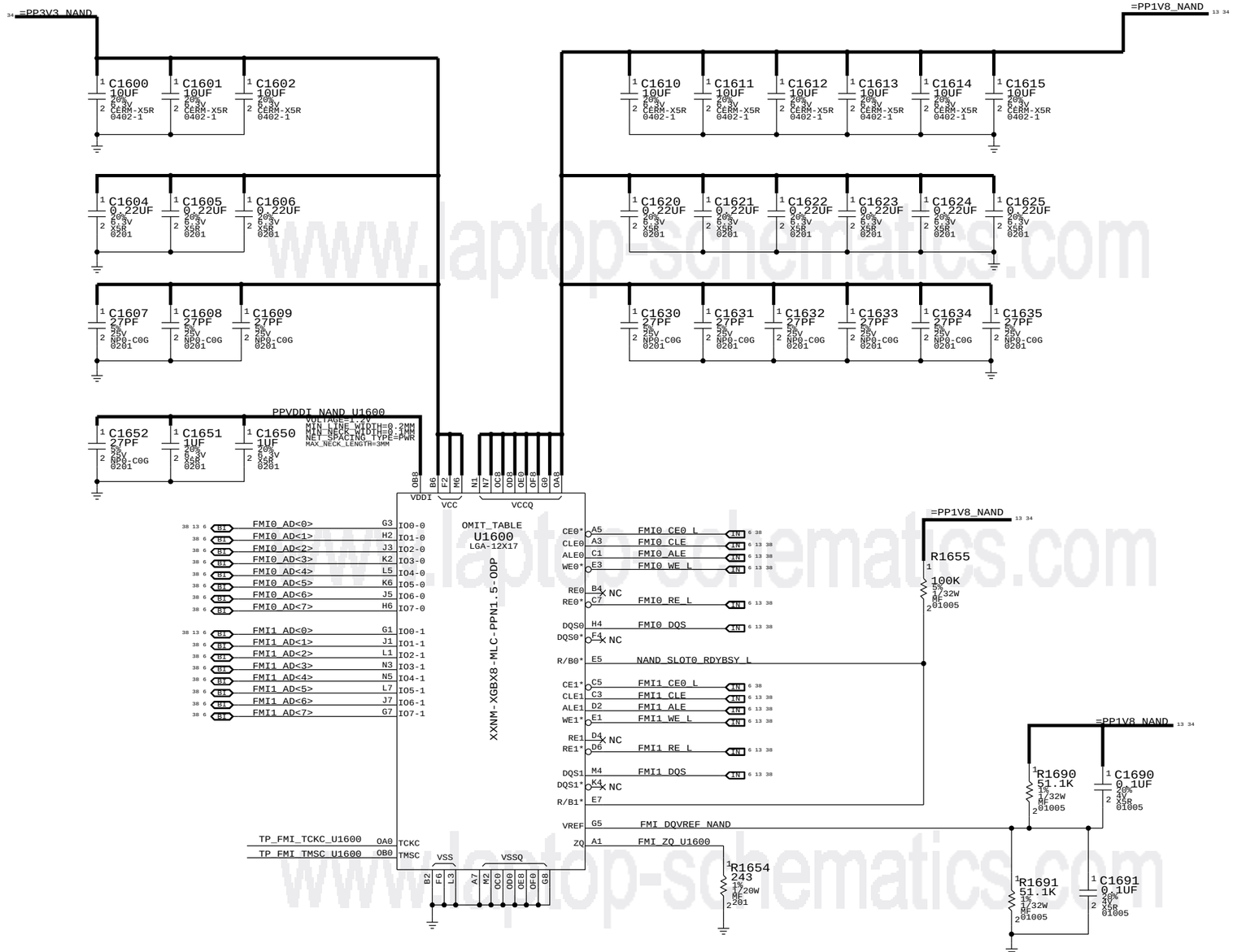

TEST POINTS

DO NOT PLACE IN NAND SINGLE PCS SHIELD CAN AREA

FMI0_AD<0>	TP1600
FMI0_ALE	TP1601
FMI0_CLE	TP1602
FMI0_RE_L	TP1603
FMI0_WE_L	TP1605
FMI0_DQS	TP1613
FMI1_AD<0>	TP1606
FMI1_ALE	TP1607
FMI1_CLE	TP1608
FMI1_RE_L	TP1609
FMI1_WE_L	TP1611
FMI1_DQS	TP1615

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: NAND

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WIFI ALIASES

36 4	HSIC1_WLAN_DATA	MAKE_BASE=TRUE	50_HSIC_WLAN_DATA	27
36 4	HSIC1_WLAN_STB	MAKE_BASE=TRUE	50_HSIC_WLAN_STROBE	27
36 5	GPIO_WLAN_HSIC_HOST_RDY	MAKE_BASE=TRUE	AP_HSIC3_RDY	27
36 5	GPIO_WLAN_HSIC_DEV_RDY	MAKE_BASE=TRUE	DEV_HSIC3_RDY	27
30	PMU_GPIO_WLAN_REG_ON	MAKE_BASE=TRUE	WLAN_REG_ON	27
30	PMU_GPIO_WLAN_HOST_WAKE	MAKE_BASE=TRUE	HOST_WAKE_WLAN	27
30	PMU_GPIO_BT_REG_ON	MAKE_BASE=TRUE	BT_REG_ON	27
30	PMU_GPIO_BT_HOST_WAKE	MAKE_BASE=TRUE	HOST_WAKE_BT	27
5	GPIO_BT_WAKE	MAKE_BASE=TRUE	BT_WAKE	27
36 5	UART3_BT_RXD	MAKE_BASE=TRUE	BT_UART_TXD	27
36 5	UART3_BT_TXD	MAKE_BASE=TRUE	BT_UART_RXD	27
36 5	UART3_BT_CTS_L	MAKE_BASE=TRUE	BT_UART_RTS_L	27
36 5	UART3_BT_RTS_L	MAKE_BASE=TRUE	BT_UART_CTS_L	27
36 30	PMU_GPIO_CLK_32K_WLAN	MAKE_BASE=TRUE	CLK32K_AP	27
36 5	I2S2_BT_BCLK	MAKE_BASE=TRUE	BT_PCM_CLK	27
36 5	I2S2_BT_DOUT	MAKE_BASE=TRUE	BT_PCM_IN	27
36 5	I2S2_BT_DIN	MAKE_BASE=TRUE	BT_PCM_OUT	27
36 5	I2S2_BT_LRCK	MAKE_BASE=TRUE	BT_PCM_SYNC	27
36 5	UART4_WLAN_RXD	MAKE_BASE=TRUE	WLAN_UART_TXD	27
36 5	UART4_WLAN_TXD	MAKE_BASE=TRUE	WLAN_UART_RXD	27
5	GPIO_WL_HSIC_RESUME	MAKE_BASE=TRUE	WLAN_HSIC3_RESUME	27
34	VDDIO_WLAN_BT_1V8	MAKE_BASE=TRUE	PP_WL_BT_VDDIO_AP	27

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SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: ALIASES

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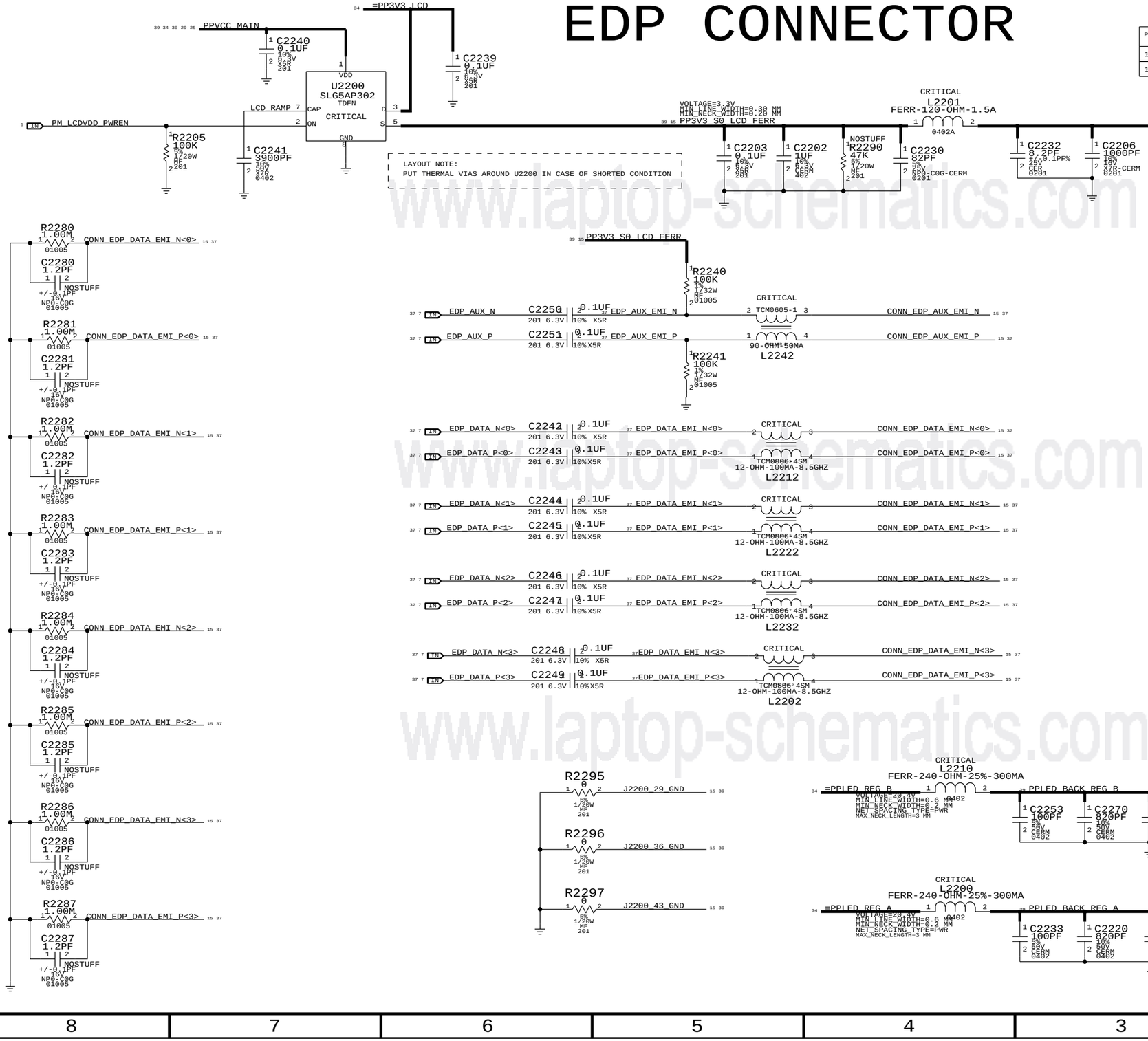
EDP CONNECTOR

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0667	155S0583		L2242,L5500,L5510,L5520,L5530,L5540,L5930,L5931	RDAR://PROBLEM/8616060, RADAR://PROBLEM/9015335
155S0625	155S0559		L2202,L2212,L2222,L2232	RDAR://PROBLEM/9017591



SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
VIDEO: EDP CONNECTOR

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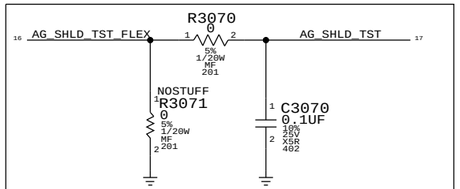
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0525	1	IC,ASIC,GROUNDHOG B0,120B BGA	U3003	CRITICAL	

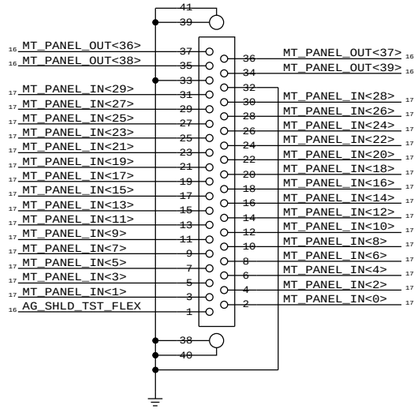
CONNECTORS TO GRAPE FLEX



P/N 518S0828

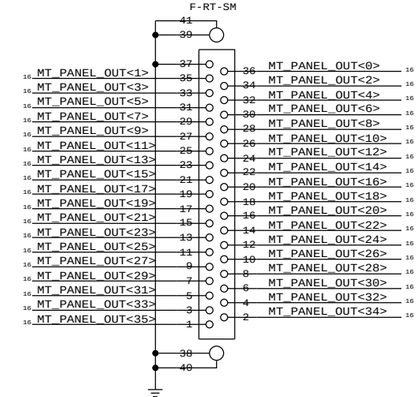
MATES WITH LEFTMOST GRAPE FLEX TAIL

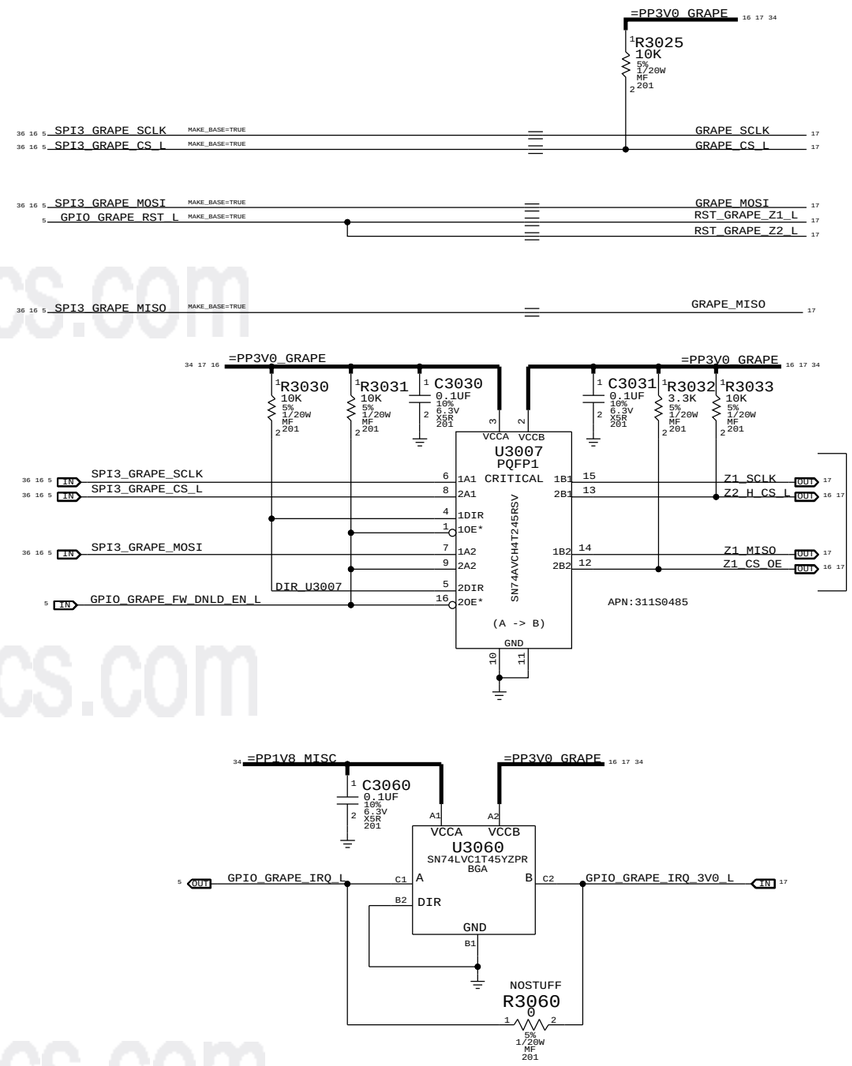
CRITICAL
J3010
502250-8037-B
F-RT-SM



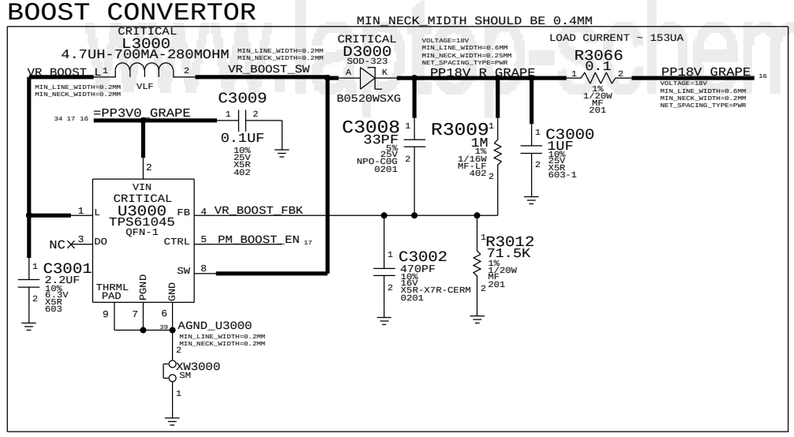
MATES WITH RIGHTMOST GRAPE FLEX TAIL

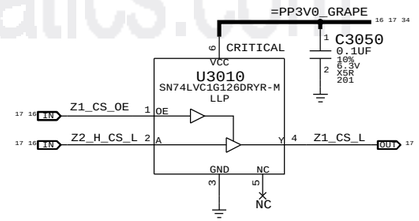
CRITICAL
J3011
502250-8037-B
F-RT-SM

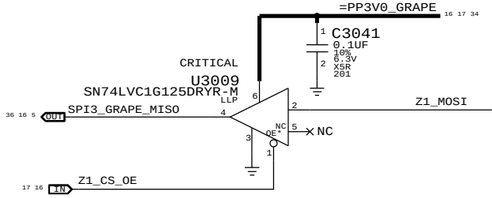




BOOST CONVERTOR







PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0523	311S0485		U3007	
311S0524	311S0533		U3009	
311S0525	311S0532		U3010	

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
GRAPE: GROUNDHOG,CONN,BOOST

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ZEPHYR 1+ ASIC

=PP3V0_GRAPE_Z1 (34)

R3101 4.7 5% 1/20W MF 201 — VOLTAGE=3.0V, MIN_LINE_WIDTH=0.2MM, MIN_NECK_WIDTH=0.2MM, NET_SPACING_TYPE=PWR

MT_3V3_INT

C3102 0.1UF 10% 6.3V X5R 201

C3104 4.7UF 20% 6.3V X5R-CERM1 402

C3103 0.1UF 10% 6.3V X5R 201

Z1_1V8_OUT (17)

C3101 2.2UF 20% 4V X5R 402

=PP3V0_GRAPE (16 17 34)

R3155 100K 5% 1/20W MF 201

VDDANA — VDDDIG — VDDIO — V18

CRITICAL
U3100
BCM5973
BGA

MT_PANEL_IN<0> (16)	H2	IN0	
MT_PANEL_IN<1> (16)	G2	IN1	
MT_PANEL_IN<2> (16)	D7	IN2	
MT_PANEL_IN<3> (16)	C1	IN3	
MT_PANEL_IN<4> (16)	F1	IN4	
MT_PANEL_IN<5> (16)	J1	IN5	
MT_PANEL_IN<6> (16)	D2	IN6	
MT_PANEL_IN<7> (16)	D1	IN7	
MT_PANEL_IN<8> (16)	K7	IN8	
MT_PANEL_IN<9> (16)	H1	IN9	
MT_PANEL_IN<10> (16)	E1	IN10	
MT_PANEL_IN<11> (16)	E2	IN11	
MT_PANEL_IN<12> (16)	J2	IN12	
MT_PANEL_IN<13> (16)	G1	IN13	
MT_PANEL_IN<14> (16)	F2	IN14	
MT_PANEL_IN<15> (16)	J7	IN15	
MT_PANEL_IN<16> (16)	K2	IN16	
MT_PANEL_IN<17> (16)	N4	IN17	
MT_PANEL_IN<18> (16)	M5	IN18	
MT_PANEL_IN<19> (16)	N5	IN19	
MT_PANEL_IN<20> (16)	M6	IN20	
MT_PANEL_IN<21> (16)	N3	IN21	
MT_PANEL_IN<22> (16)	M3	IN22	
MT_PANEL_IN<23> (16)	L1	IN23	
MT_PANEL_IN<24> (16)	K1	IN24	
MT_PANEL_IN<25> (16)	L2	IN25	
MT_PANEL_IN<26> (16)	N6	IN26	
MT_PANEL_IN<27> (16)	M2	IN27	
MT_PANEL_IN<28> (16)	M4	IN28	
MT_PANEL_IN<29> (16)	M1	IN29	
MUX_IN<0> (16)	N2	IN30	
MUX_IN<1> (16)	N1	IN31	
MUX_IN<2> (16)	N13	IN32	
MUX_IN<3> (16)	N12	IN33	
MUX_IN<4> (16)	M10	IN34	
MUX_IN<5> (16)	M13	IN35	
MUX_IN<6> (16)	N8	IN36	
MUX_IN<7> (16)	M12	IN37	
MUX_IN<8> (16)	K13	IN38	
MUX_IN<9> (16)	L13	IN39	
MUX_IN<10> (16)	L12	IN40	
MUX_IN<11> (16)	M11	IN41	
MUX_IN<12> (16)	N11	IN42	
MUX_IN<13> (16)	M8	IN43	
MUX_IN<14> (16)	N9	IN44	
MUX_IN<15> (16)	M9	IN45	
MUX_IN<16> (16)	N10	IN46	
MUX_IN<17> (16)	K12	IN47	
MUX_IN<18> (16)	J13	IN48	
MUX_IN<19> (16)	F12	IN49	
NC	G13	IN50	
NC	J12	IN51	
NC	E12	IN52	
NC	E13	IN53	
NC	H13	IN54	
NC	N7	IN55	
NC	G13	IN56	
NC	B12	IN57	
NC	H12	IN58	
NC	F13	IN59	
NC	C13	IN60	
NC	E7	IN61	
NC	M7	IN62	
NC	G12	IN63	

SCLK	A11	Z1_SCLK	IN (16 17)
CS*	B10	Z1_CS_L	IN (16)
MISO	B9	Z1_MISO	IN (16 17)
MOSI	B8	Z1_MOSI	OUT (16 17)
GO	A8	Z1_GO	(17)
DONE	B7	Z1_DONE	(17)
PCLK	A12	Z1_PCLK	(17)
STMOUT	A10	Z1_STMIN	
STMIN	A13		
B_ADR0	A5	Z1_B_ADR<0>	(16)
B_ADR1	B5	Z1_B_ADR<1>	(16)
B_ADR2	A6	Z1_B_ADR<2>	(16)
BON_L0	A2	Z1_BON_L<0>	(16)
BON_L1	A1	Z1_BON_L<1>	(16)
BON_L2	A3	Z1_BON_L<2>	(16)
BON_L3	A4	Z1_BON_L<3>	(16)
BON_L4	B4	Z1_BON_L<4>	(16)
BON_L5	B3	Z1_BON_L<5>	(16)
TM	A9	U3100_TM	
RESET*	A7	RST_GRAPE_Z1_L	(16)

R3181 100 5% 1/32W MF 01005

GNDANA — GNDDIG GNDIO

B1 B2 B12 B13 C2 C3 C6 C7 C8 C11 C12 D3 D11 F7 H7 L3 L4 L5 L6 L7 L8 L9 L10 L11 C4 B11

ARM9 MCU (Z2 BASED)

Z2_VDDCORE

C3111 10UF 20% 6.3V CERM-X5R 0402-1

C3109 0.1UF 10% 6.3V X5R 201

VOLTAGE=1.8V, MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.1MM, NET_SPACING_TYPE=PWR

VDDANA AND VDDCORE ARE EACH GENERATED WITHIN Z2 AND BYPASSED OUTSIDE

Z2_VDDANA

C3112 2.2UF 20% 4V X5R 402

C3110 0.1UF 10% 6.3V X5R 201

=PP3V0_GRAPE_Z2 (34)

C3105 0.1UF 10% 6.3V X5R 201

C3107 4.7UF 20% 6.3V X5R-CERM1 402

Z2_3V3_1V8_IN

C3108 0.1UF 10% 6.3V X5R 201

C3106 0.1UF 10% 6.3V X5R 201

C3191 10UF 20% 6.3V CERM-X5R 0402-1

C3192 10UF 20% 6.3V CERM-X5R 0402-1

R3190 1.00 1% 1/20W MF 201

Z1_1V8_OUT (17)

MIN_NECK_MIDTH SHOULD BE 0.4MM

VDDANA VDDCORE VDDIO VDDLDO

CRITICAL
U3101
BCM5974CKFBGH
FBGA

NC	A9	IN0_0	
NC	B9	IN0_1	
NC	A7	IN1_0	
NC	A8	IN1_1	
NC	B8	IN2_0	
NC	C8	IN2_1	
NC	B7	IN3_0	
NC	C7	IN3_1	
NC	A6	IN4_0	
NC	B6	IN4_1	
NC	C6	IN5_0	
NC	C5	IN5_1	
NC	B5	IN6_0	
NC	A5	IN6_1	
NC	A4	IN7_0	
NC	B4	IN7_1	
NC	A3	IN8_0	
NC	B3	IN8_1	
NC	C2	IN9_0	
NC	A2	IN9_1	
NC	B2	IN10_0	
NC	C1	IN10_1	
NC	B1	IN11_0	
NC	A1	IN11_1	
NC	E6	ARMTAPMD*	
BOOT_CFG0_R	F6	BOOT_CFG0	
BOOT_CFG1_R	D3	BOOT_CFG1	
NC	G5	FLOO	
NC	F5	LFOO	
NC	G7	EXTFLLIN	

B_ADR0	F9		
B_ADR1	F8	Z1_PCLK	(17)
B_ADR2	G9		
BON_L0	J8	Z1_CS_OE_R	
BON_L1	H9	NC_BON_L1	NO_TEST=TRUE
BON_L2	J9	AG_SHLD_TST	(16)
BON_L3	H7	NC_BON_L3	NO_TEST=TRUE
BON_L4	J7		
BON_L5	H5	NC_BON_L5	NO_TEST=TRUE
GPIO0	J2	GPIO_GRAPE_IRQ_3V0_L	OUT (16)
GPIO1	J3	PM_BOOST_EN	OUT (16)
GPIO2	H4	Z1_GO	(17)
GPIO3	J6	Z1_DONE	(17)
GPIO4	G3	GRAPE_CS_L	IN (16)
GPIO5	F3	GRAPE_MOSI	IN (16)
GPIO6	F4	GRAPE_MISO	OUT (16)
GPIO7	H6	GRAPE_SCLK	IN (16)
JTAG_TCK	G6	TP_U3101_TCK	
JTAG_TDI	E8	TP_U3101_TDI	
JTAG_TDO	E9	TP_U3101_TDO	
JTAG_TMS	F7	TP_U3101_TMS	
H_CS*	H1	Z2_H_CS_L	IN (16)
H_SCLK	J1	Z1_SCLK	IN (16 17)
H_SDI	H3	Z1_MISO	IN (16 17)
H_SDO	J4	Z1_MOSI	OUT (16 17)
A_CS*	F1	Z2_A_CS_L	
A_SCLK	G1	TP_Z2_A_SCLK	
A_SDI	F2	TP_Z2_A_SDI	
A_SDO	G4	TP_Z2_A_SDO	
TM0	E7	TP_U3101_TM0	
TM1	D4	U3101_TM1	
CLKIN	E5	HOST_REFCLK	PMU_GPIO_CLK_32K_GRAPE (30 36) MAKE_BASE=TRUE
CLKOUT	E4	NC	
INTERNAL PU	RESET*	D5	RST_GRAPE_Z2_L (16)

R3120 0 5% 1/20W MF 201

R3160 100K 5% 1/20W MF 201

R3107 100K 5% 1/20W MF 201

=PP3V0_GRAPE (16 17 34)

R3180 100 5% 1/32W MF 01005

=PP3V0_GRAPE (34 17 16)

R3173 0 5% 1/20W MF 201

R3171 0 5% 1/20W MF 201

GND

C3 C4 D6 D7 D8 C9 D9 G2 D1 H8

CFG1	CFG0	MODE
0	0	DEPENDENT 1
0	1	DEPENDENT 2
1	0	AUTONOMOUS
1	1	SLAVE

K48 USES DEPENDENT 2 MODE

Z2 - PRODUCT STRAP OPTIONS

BON_L5	BON_L4	BON_L3	MODE
LOW	X	X	K48
FLOAT	FLOAT	FLOAT	K94
FLOAT	LOW	FLOAT	J2
ALL OTHER STRAPS			CRITICAL ERROR
DEFAULT			J2

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: GRAPE: Z1, Z2

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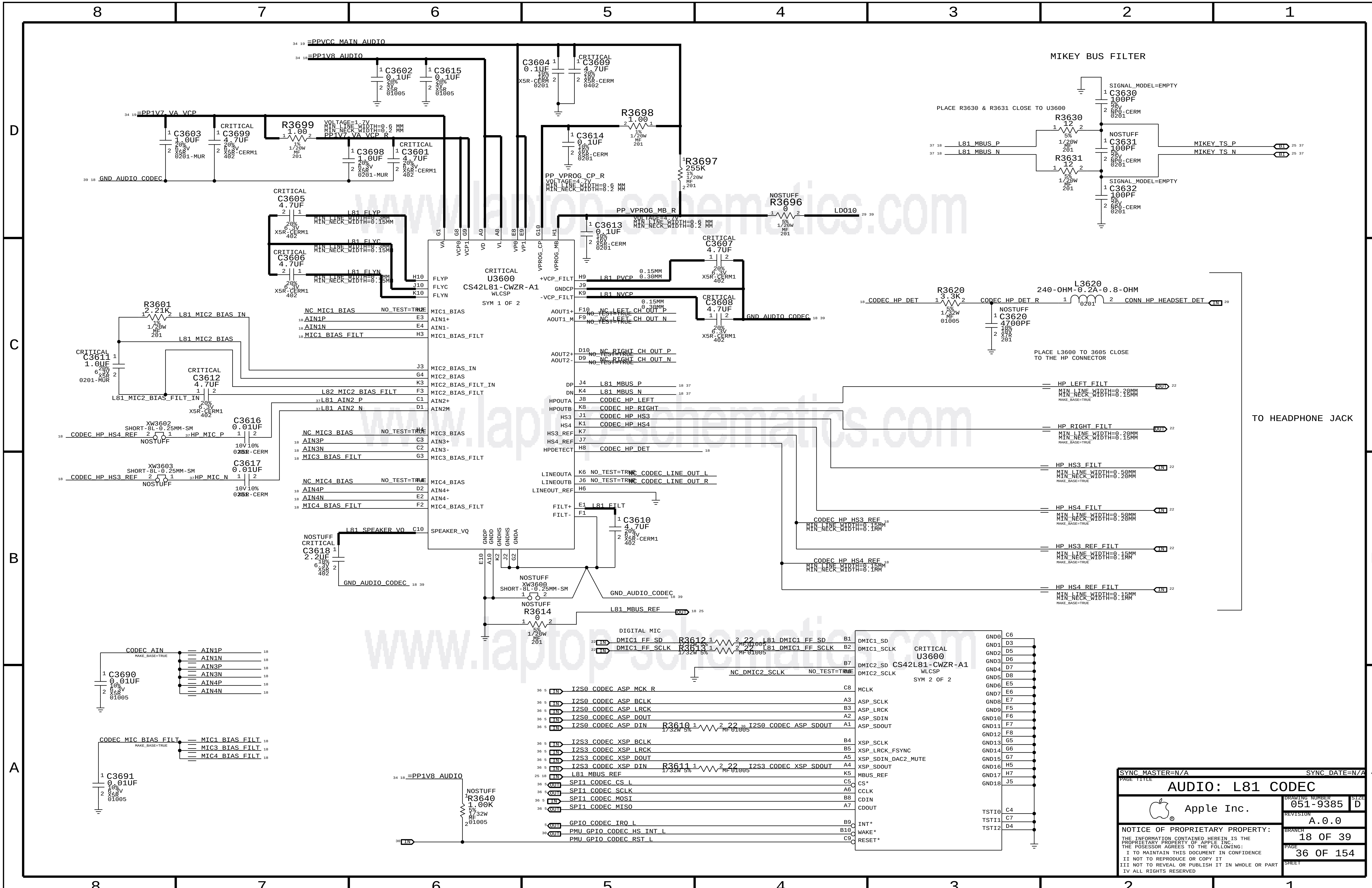

MIKEY BUS FILTER
PLACE R3630 & R3631 CLOSE TO U3600
SIGNAL_MODEL=EMPTY
C3630 100PF
R3630 12
R3631 12
C3631 100PF
C3632 100PF
L81_MBUS_P
L81_MBUS_N
MIKEY_TS_P
MIKEY_TS_N
=PPVCC_MAIN_AUDIO
=PP1V8_AUDIO
=PP1V7_VA_VCP
GND_AUDIO_CODEC
C3602 0.1UF
C3615 0.1UF
C3604 0.1UF
C3609 4.7UF
C3603 1.0UF
C3699 4.7UF
R3699 1.00
C3698 1.0UF
C3601 4.7UF
R3698 1.00
C3614 0.1UF
R3697 255K
PP_VPROG_CP_R
PP_VPROG_MB_R
R3696 0
LDO10
C3613 0.1UF
C3605 4.7UF
C3606 4.7UF
C3607 4.7UF
C3608 4.7UF
CRITICAL
U3600
CS42L81-CWZR-A1
WLCSP
SYM 1 OF 2
FLYP
FLYC
FLYN
MIC1_BIAS
AIN1+
AIN1-
MIC1_BIAS_FILT
MIC2_BIAS_IN
MIC2_BIAS
MIC2_BIAS_FILT_IN
MIC2_BIAS_FILT
AIN2+
AIN2M
MIC3_BIAS
AIN3+
AIN3-
MIC3_BIAS_FILT
MIC4_BIAS
AIN4+
AIN4-
MIC4_BIAS_FILT
SPEAKER_VQ
+VCP_FILT
GNDCP
-VCP_FILT
AOUT1+
AOUT1_M
AOUT2+
AOUT2-
DP
DN
HPOUTA
HPOUTB
HS3
HS4
HS3_REF
HS4_REF
HPDETECT
LINEOUTA
LINEOUTB
LINEOUT_REF
FILT+
FILT-
R3601 2.21K
C3611 1.0UF
C3612 4.7UF
C3616 0.01UF
C3617 0.01UF
XW3602
XW3603
SHORT-8L-0.25MM-SM
NOSTUFF
CODEC_HP_HS4_REF
CODEC_HP_HS3_REF
HP_MIC_P
HP_MIC_N
C3618 2.2UF
C3610 4.7UF
XW3600
R3614 0
L81_MBUS_REF
R3620 3.3K
L3620
240-OHM-0.2A-0.8-OHM
CODEC_HP_DET
CONN_HP_HEADSET_DET
C3620 4700PF
PLACE L3600 TO 3605 CLOSE TO THE HP CONNECTOR
HP_LEFT_FILT
HP_RIGHT_FILT
HP_HS3_FILT
HP_HS4_FILT
HP_HS3_REF_FILT
HP_HS4_REF_FILT
TO HEADPHONE JACK
DIGITAL MIC
DMIC1_FF_SD
DMIC1_FF_SCLK
R3612 22
R3613 22
CRITICAL
U3600
CS42L81-CWZR-A1
WLCSP
SYM 2 OF 2
DMIC1_SD
DMIC1_SCLK
DMIC2_SD
DMIC2_SCLK
MCLK
ASP_SCLK
ASP_LRCK
ASP_SDIN
ASP_SDOUT
XSP_SCLK
XSP_LRCK_FSYNC
XSP_SDIN_DAC2_MUTE
XSP_SDOUT
MBUS_REF
CS*
CCLK
CDIN
CDOUT
INT*
WAKE*
RESET*
I2S0_CODEC_ASP_MCK_R
I2S0_CODEC_ASP_BCLK
I2S0_CODEC_ASP_LRCK
I2S0_CODEC_ASP_DOUT
I2S0_CODEC_ASP_DIN
R3610 22
I2S3_CODEC_XSP_BCLK
I2S3_CODEC_XSP_LRCK
I2S3_CODEC_XSP_DOUT
I2S3_CODEC_XSP_DIN
R3611 22
SPI1_CODEC_CS_L
SPI1_CODEC_SCLK
SPI1_CODEC_MOSI
SPI1_CODEC_MISO
GPIO_CODEC_IRQ_L
PMU_GPIO_CODEC_HS_INT_L
PMU_GPIO_CODEC_RST_L
R3640 1.00K
CODEC_AIN
C3690 0.01UF
CODEC_MIC_BIAS_FILT
C3691 0.01UF
SYNC_MASTER=N/A
SYNC_DATE=N/A
AUDIO: L81 CODEC
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051-9385
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LEFT SPEAKER AMP

I2C ADDRESS: 1000000X

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S0002	4	RES,MF,1/20W,0.0OHM,5,0201,SMD	R3742,R3743,R3752,R3753	?	?
113S0022	4	RES,MF,1/10W,0OHM,5,0603,SMD,LF	FL3740,FL3741,FL3750,FL3751	?	?

=PPVCC_MAIN_AUDIO

CRITICAL C3741 4.7UF 20% 10V X5R-CERM 0402
CRITICAL C3742 4.7UF 20% 10V X5R-CERM 0402
CRITICAL C3743 4.7UF 20% 10V X5R-CERM 0402
C3744 0.1UF 10% 10V X5R-CERM 0201
L19_L_VBOOST
CRITICAL C3745 22UF 20% 10V X5R-CERM 0603-1
CRITICAL C3710 22UF 20% 10V X5R-CERM 0603-1
C3711 0.1UF 10% 10V X5R-CERM 0201
C3712 27PF 5% 16V NP0-C0G 01005

=PP1V7_VA_VCP 18 19 34

C3713 27PF 5% 16V NP0-C0G 01005
C3746 0.1UF 10% 6.3V X5R 201

C3747 4.7UF 20% 6.3V X5R-CERM1 402
C3748 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3740 2.2UH-20%-3.3A-0.115OHM TFA302610A-SM
L19_L_SWITCH

CRITICAL U3740 CS35L19B-CWZR WLCSP VER1

A2	SW	
B2		
D5	SDA	I2C0_SDA_1V8 (36 30 25 19 5)
D6	SCL	I2C0_SCL_1V8 (36 30 25 19 5)
A7	INT*	GPIO_SPKAMP_LEFT_IRQ_L (5)
A6	RESET*	GPIO_SPKAMP_RST_L (19 5)
D7	ALIVE	GPIO_SPKAMP_KEEPALIVE (19 5)
C7	ADO	
E7	MCLK	I2S1_SPKAMP_MCK_R (19 5)
E6	SCLK	I2S1_SPKAMP_BCLK (19 5)
F6	LRCK/FSYNC	I2S1_SPKAMP_LRCK (19 5)
F7	SDIN	I2S1_SPKAMP_DOUT (19 5)
E5	SDOUT	I2S1_SPKAMP_DIN (19 5)
F2	FILT+	L19_L_FILT
C5	LDO_FILT	L19_L_LDO_FILT
E3	VSENSE-	SPKR_L_VSENSE_N_FILT (37)
E2	VSENSE+	SPKR_L_VSENSE_P_FILT (37)
F1	ISENSE-	SPKR_L_SES_N (37)
E1	ISENSE+	SPKR_L_SES_P (37)
D2	OUT+	SPKR_L_P (37)
C2	OUT-	SPKR_L_N (37)
B7	IREF+	L19_L_IREF
A1	VBST	
B1		
C1		
D1		
A4	VP	
A5		
F5	VA	
A3	GNDP	
B3		
B4		
C3		
C4		
D3		
D4	GNDA	
B5		
B6		
C6		
E4		
F3		
F4		

NOSTUFF C3760 0.01UF 10% 10V X5R-CERM 0201

OMIT_TABLE R3743 10 5% 1/20W MF 201
OMIT_TABLE R3742 10 5% 1/20W MF 201

CRITICAL R3740 0.100 1% 1/4W MF 0805
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM

OMIT_TABLE CRITICAL FL3741 220-OHM-2.0A 0603
SPKR_L_FLT

SPKR_L_CONN_P (19 37)

NOSTUFF C3761 18PF 5% 25V NP0-C0G-CERM 0201
NOSTUFF C3763 3.9PF +/-0.1PF 25V NP0-C0G-CERM 0201
C3740 8.2PF +/-0.1PF% 25V CER 0201

R3741 44.2K 1% 1/20W MF 201

OMIT_TABLE CRITICAL FL3740 220-OHM-2.0A 0603

SPKR_L_CONN_N (19 37)

NOSTUFF C3764 18PF 5% 25V NP0-C0G-CERM 0201
NOSTUFF C3766 3.9PF +/-0.1PF 25V NP0-C0G-CERM 0201
C3749 8.2PF +/-0.1PF% 25V CER 0201

R3745 10K 5% 1/20W MF 201 SPKR_L_VSENSE_N (19 37)
R3744 10K 5% 1/20W MF 201 SPKR_L_VSENSE_P (19 37)

NOSTUFF C3767 100PF 5% 25V NP0-CERM 0201
NOSTUFF C3768 100PF 5% 25V NP0-CERM 0201

SPEAKER CONNECTOR

APN 518S0672
CRITICAL J3700 78171-6006 M-RT-SM

37 19	SPKR_L_CONN_P	XW3774 SM
37 19	SPKR_L_VSENSE_P	SIGNAL_MODEL=EMPTY
37 19	SPKR_L_CONN_N	XW3775 SM
37 19	SPKR_L_VSENSE_N	SIGNAL_MODEL=EMPTY
5	SPK_ID	
37 19	SPKR_R_CONN_P	XW3776 SM
37 19	SPKR_R_VSENSE_P	SIGNAL_MODEL=EMPTY
37 19	SPKR_R_CONN_N	XW3777 SM
37 19	SPKR_R_VSENSE_N	SIGNAL_MODEL=EMPTY

PLACE XWS CLOSE TO CONNECTOR

NOSTUFF CRITICAL C3770 100PF 5% 16V NP0-C0G 01005
NOSTUFF CRITICAL C3771 100PF 5% 16V NP0-C0G 01005
NOSTUFF CRITICAL C3772 100PF 5% 16V NP0-C0G 01005
NOSTUFF CRITICAL C3773 100PF 5% 16V NP0-C0G 01005

RIGHT SPEAKER AMP

I2C ADDRESS: 1000001X

=PPVCC_MAIN_AUDIO

CRITICAL C3751 4.7UF 20% 10V X5R-CERM 0402
CRITICAL C3752 4.7UF 20% 10V X5R-CERM 0402
CRITICAL C3753 4.7UF 20% 10V X5R-CERM 0402
C3754 0.1UF 10% 10V X5R-CERM 0201
L19_R_VBOOST
CRITICAL C3755 22UF 20% 10V X5R-CERM 0603-1
CRITICAL C3720 22UF 20% 10V X5R-CERM 0603-1
C3721 0.1UF 10% 10V X5R-CERM 0201
C3722 27PF 5% 16V NP0-C0G 01005

=PP1V7_VA_VCP 18 19 34

C3723 27PF 5% 16V NP0-C0G 01005
C3756 0.1UF 10% 6.3V X5R 201

C3757 4.7UF 20% 6.3V X5R-CERM1 402
C3758 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3750 2.2UH-20%-3.3A-0.115OHM TFA302610A-SM
L19_R_SWITCH

CRITICAL U3750 CS35L19B-CWZR WLCSP VER1

A2	SW	
B2		
D5	SDA	I2C0_SDA_1V8 (36 30 25 19 5)
D6	SCL	I2C0_SCL_1V8 (36 30 25 19 5)
A7	INT*	GPIO_SPKAMP_RIGHT_IRQ_L (5)
A6	RESET*	GPIO_SPKAMP_RST_L (19 5)
D7	ALIVE	GPIO_SPKAMP_KEEPALIVE (19 5)
C7	ADO	PP1V7_VA_VCP (39 34 29)
E7	MCLK	I2S1_SPKAMP_MCK_R (19 5)
E6	SCLK	I2S1_SPKAMP_BCLK (19 5)
F6	LRCK/FSYNC	I2S1_SPKAMP_LRCK (19 5)
F7	SDIN	I2S1_SPKAMP_DOUT (19 5)
E5	SDOUT	I2S1_SPKAMP_DIN (19 5)
F2	FILT+	L19_R_FILT
C5	LDO_FILT	L19_R_LDO_FILT
E3	VSENSE-	SPKR_R_VSENSE_N_FILT (37)
E2	VSENSE+	SPKR_R_VSENSE_P_FILT (37)
F1	ISENSE-	SPKR_R_SES_N (37)
E1	ISENSE+	SPKR_R_SES_P (37)
D2	OUT+	SPKR_R_P (37)
C2	OUT-	SPKR_R_N (37)
B7	IREF+	L19_R_IREF
A1	VBST	
B1		
C1		
D1		
A4	VP	
A5		
F5	VA	
A3	GNDP	
B3		
B4		
C3		
C4		
D3		
D4	GNDA	
B5		
B6		
C6		
E4		
F3		
F4		

NOSTUFF C3780 0.01UF 10% 10V X5R-CERM 0201

OMIT_TABLE R3753 10 5% 1/20W MF 201
OMIT_TABLE R3752 10 5% 1/20W MF 201

CRITICAL R3750 0.100 1% 1/4W MF 0805
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM

OMIT_TABLE CRITICAL FL3751 220-OHM-2.0A 0603
SPKR_R_FLT

SPKR_R_CONN_P (19 37)

NOSTUFF C3781 18PF 5% 25V NP0-C0G-CERM 0201
NOSTUFF C3783 3.9PF +/-0.1PF 25V NP0-C0G-CERM 0201
C3750 8.2PF +/-0.1PF% 25V CER 0201

R3751 44.2K 1% 1/20W MF 201

OMIT_TABLE CRITICAL FL3750 220-OHM-2.0A 0603

SPKR_R_CONN_N (19 37)

NOSTUFF C3784 18PF 5% 25V NP0-C0G-CERM 0201
NOSTUFF C3786 3.9PF +/-0.1PF 25V NP0-C0G-CERM 0201
C3759 8.2PF +/-0.1PF% 25V CER 0201

R3755 10K 5% 1/20W MF 201 SPKR_R_VSENSE_N (19 37)
R3754 10K 5% 1/20W MF 201 SPKR_R_VSENSE_P (19 37)

NOSTUFF C3787 100PF 5% 25V NP0-CERM 0201
NOSTUFF C3788 100PF 5% 25V NP0-CERM 0201

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
AUDIO: SPEAKER AMP

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DRAWING NUMBER 051-9385 SIZE D
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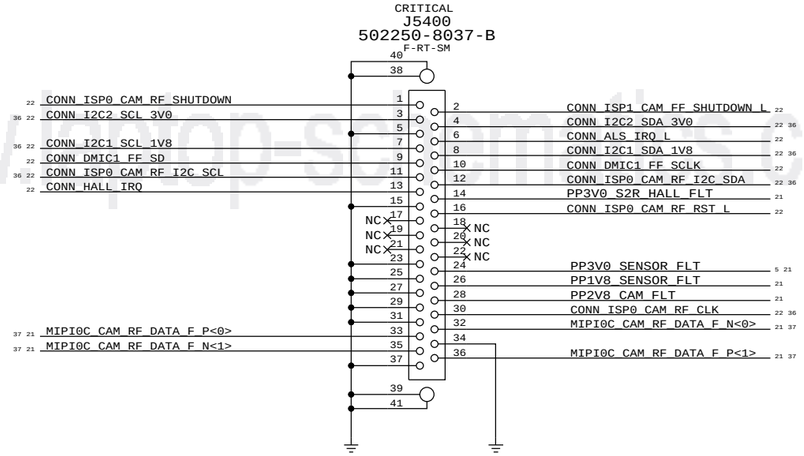
APN: 518S0828



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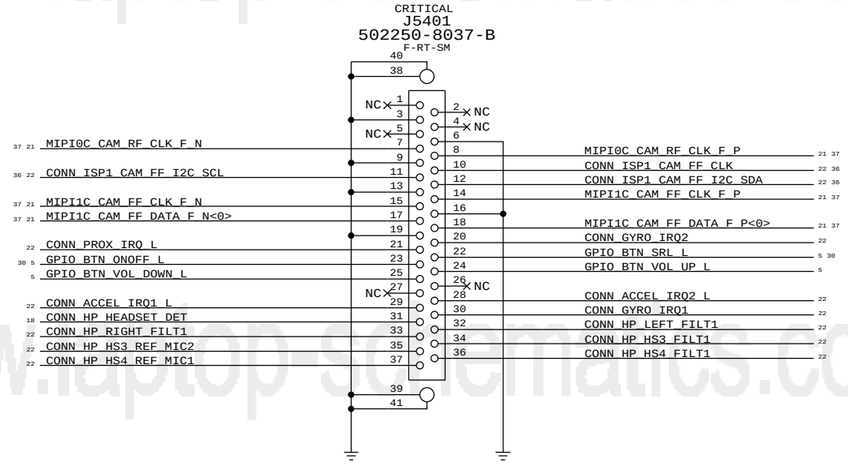

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PAGE TITLE
SENSOR FLEX CONN

Apple Inc.

DRAWING NUMBER 051-9385 SIZE D
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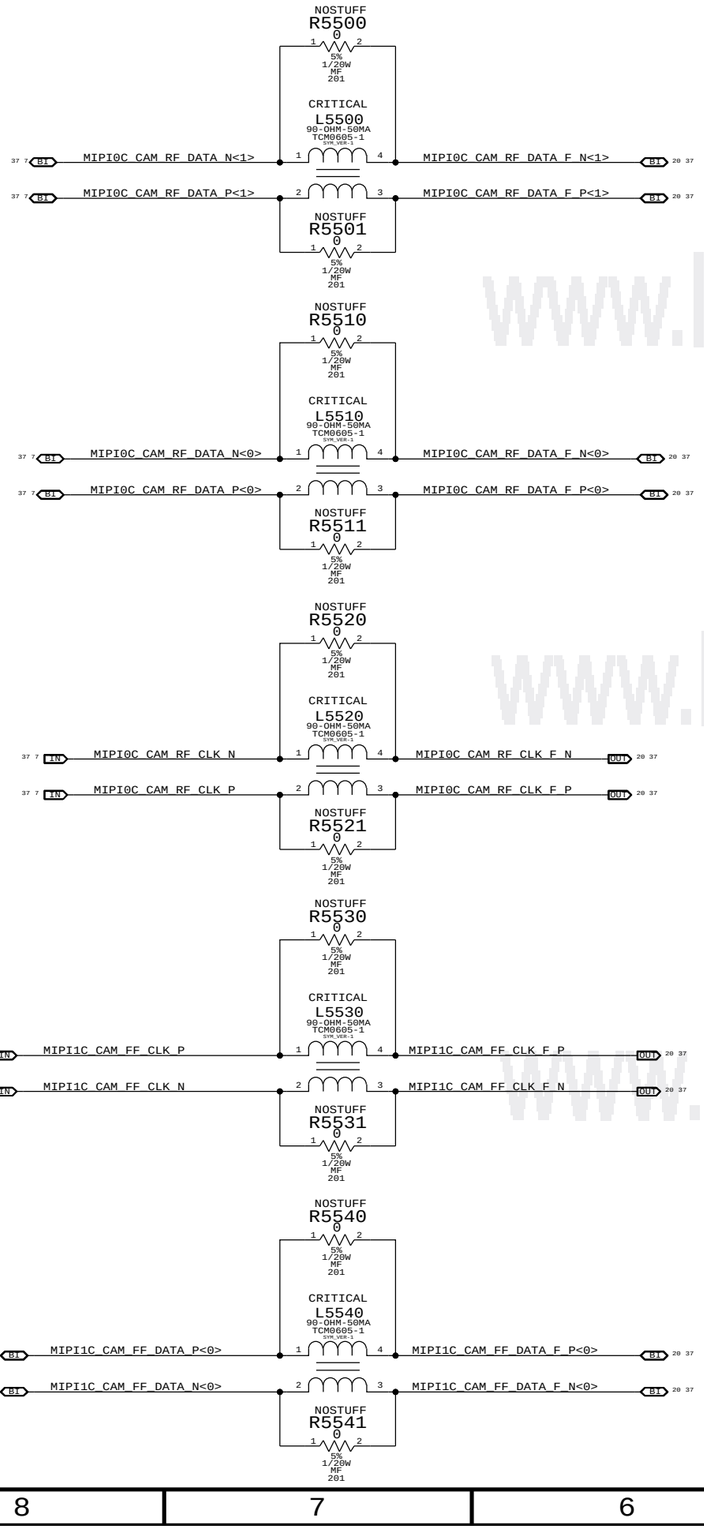

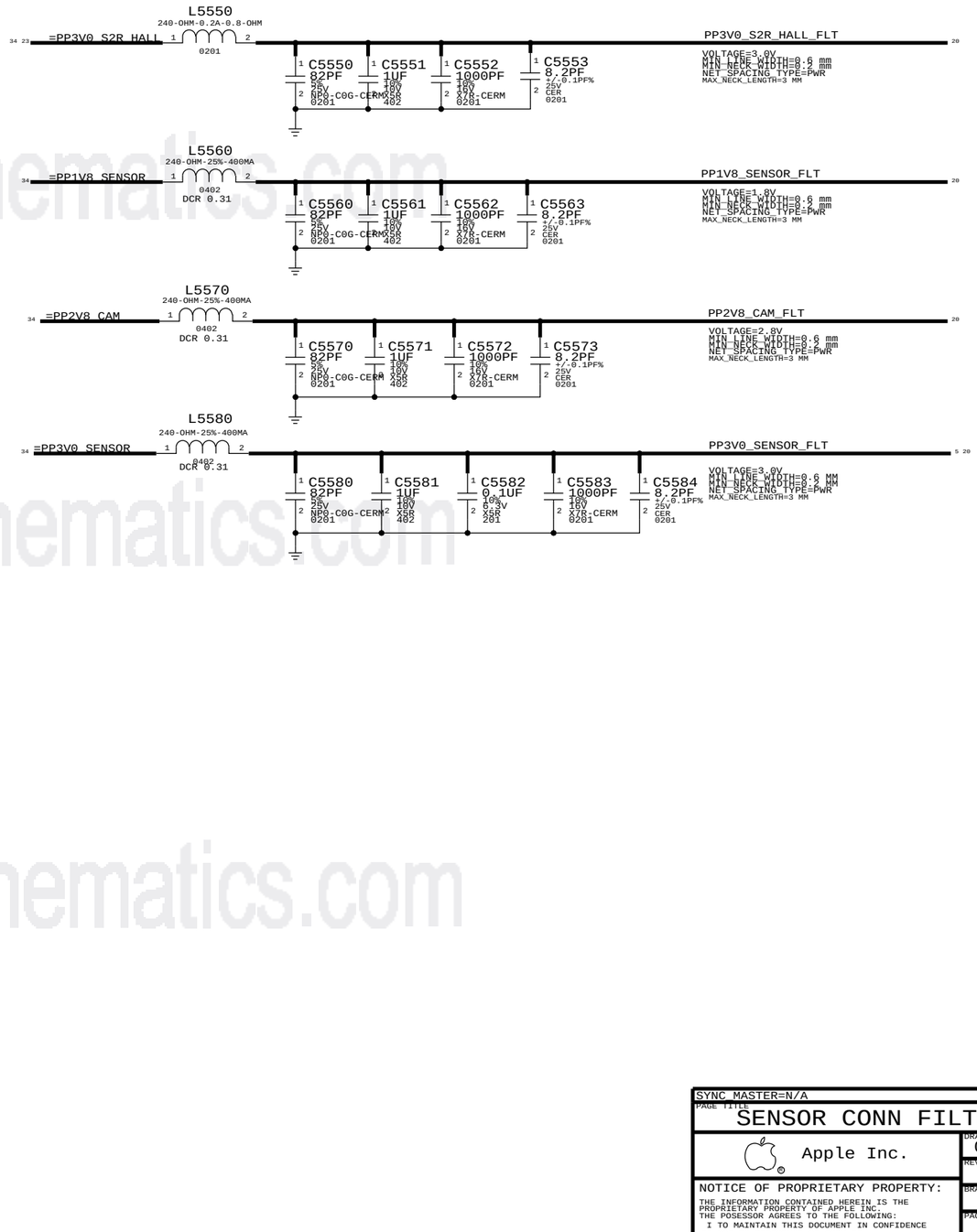

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PAGE TITLE
SENSOR CONN FILTERS 1

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REVISION A.0.0
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
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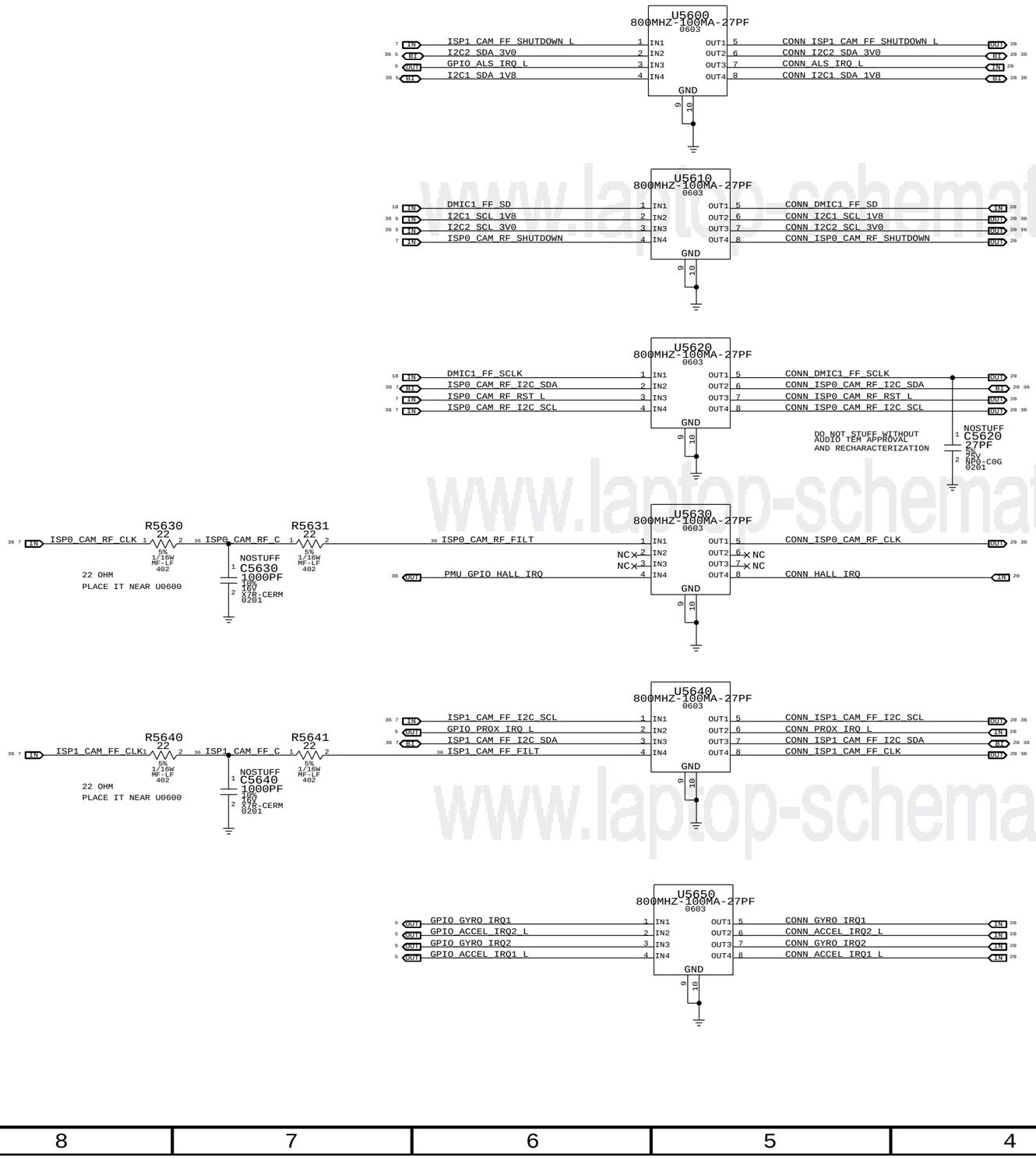

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
SENSOR CONN FILTERS 2

Apple Inc.

DRAWING NUMBER 051-9385 SIZE D

REVISION A.0.0

BRANCH

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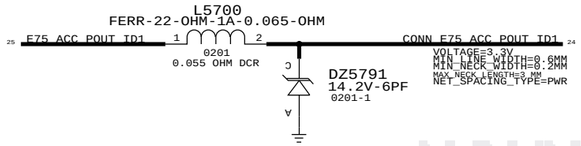
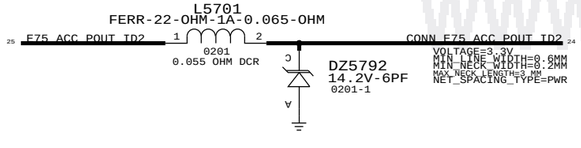
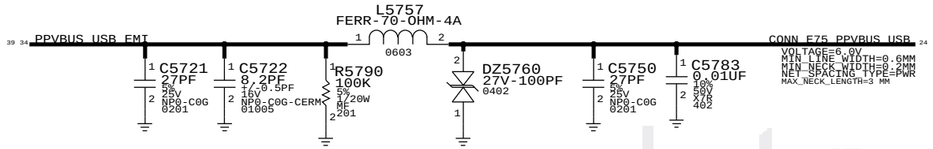
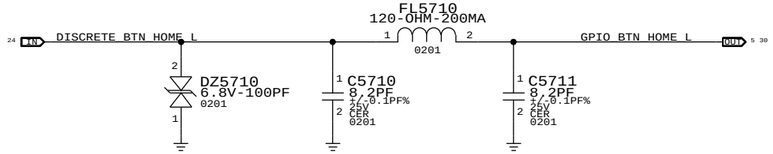
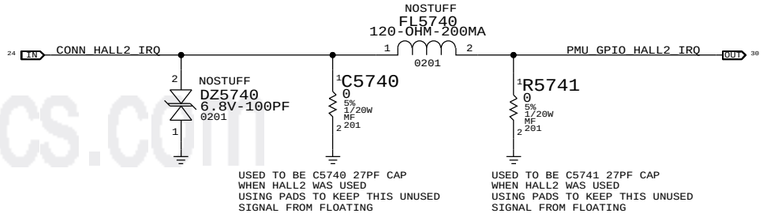


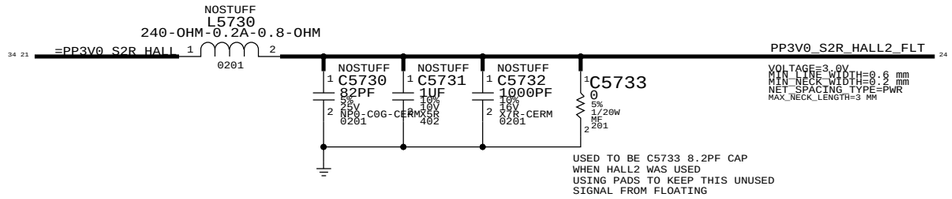




PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0116	377S0108		DZ5760	RDAR://PROBLEM/8370432
155S0320	155S0513		L5700,L5701	RDAR://PROBLEM/9625601
155S0657	155S0537		FL5710,FL5750	
155S0741	155S0397		L5757	RDAR://PROBLEM/11238851







SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: E75 DOCK SUPPORT

Apple Inc.

DRAWING NUMBER: 051-9385 SIZE: D

REVISION: A.0.0

BRANCH:

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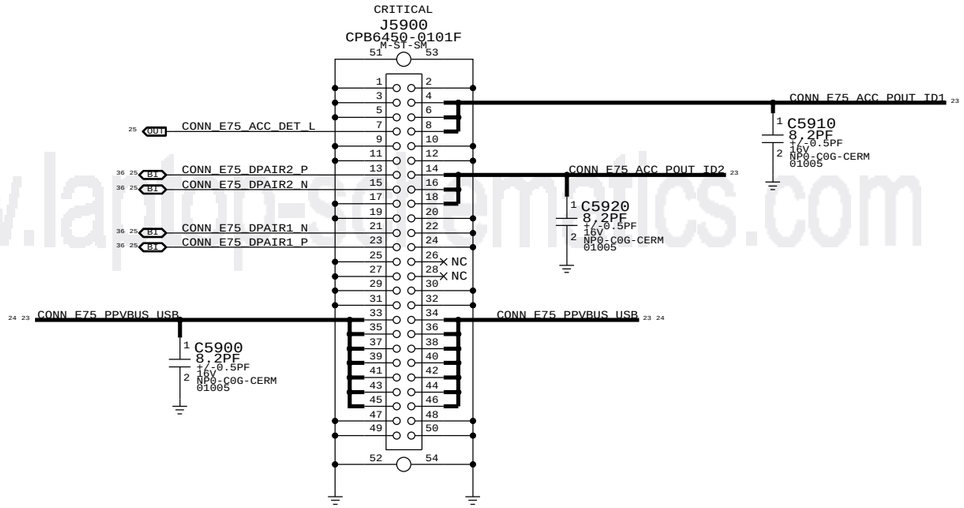
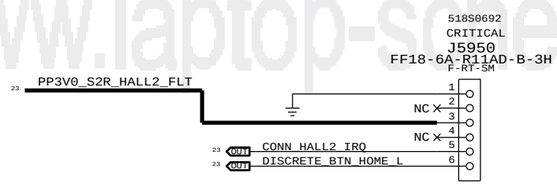
IO FLEX CONNECTOR

PN 516S0542 (PLUG - MALE)





SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: IO FLEX CONN

Apple Inc.

DRAWING NUMBER: 051-9385 SIZE: D

REVISION: A.0.0

BRANCH:

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0614	1	IC,ASIC,TRISTAR,CBTL1608,A1,WLCSP36	U5900	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0773	155S0453	?	FL5990	RDAR://PROBLEM/10882925

TRISTAR BASEBAND USB MUX (NEEDED FOR MDM9600 BB)

BASEBAND USB MUX BYPASS

NOTE: ISOLATE SELECT SIGNAL FROM PMU ON MLB_B AND MLB_C SO THE MUX IS PERMANENTLY POINTED TO THE DOCK

SEL	Y+	Y-
0	M+	M-
1	D+	D-

DEFAULT =>

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: TRISTAR

Apple Inc.

DRAWING NUMBER: 051-9385 SIZE: D

REVISION: A.0.0

BRANCH:

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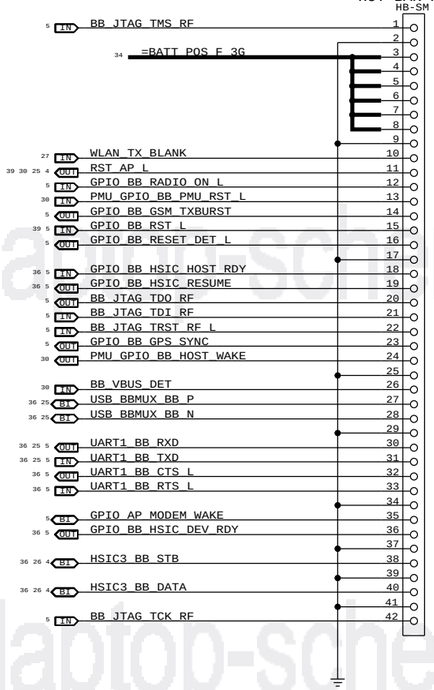
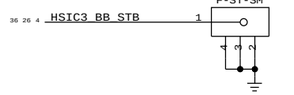
CELLULAR/GPS HOTBAR PADS

OMIT
998-3732
J6000
HOT-BAR-PADS
H8-SM

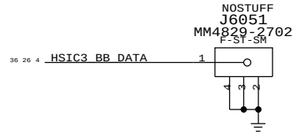


DEBUG

NOSTUFF
J6050
MM4829-2702
F-ST-SM



NOSTUFF
J6051
MM4829-2702
F-ST-SM



SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
CONNECTOR: CELLULAR

Apple Inc.

DRAWING NUMBER 051-9385 SIZE D
REVISION A.0.0
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WLAN/BT

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S0171	1	WIFI MODULE - MURATA	U6101_RF	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S0175	339S0171		U6101_RF	WIFI MODULE - USI
311S0548	311S0398		U6102_RF	

ANTENNA CONNECTOR

CONDUCTED TEST PORT

CRITICAL J6190_RF MM4829-2702 F-ST-SM

CRITICAL C6193_RF 3.9PF +/-0.1PF 50V NP0-CERM 0402

RF_ANT WIFI_50S 50_OHM

NOSTUFF L6190_RF 5.6NH+/-0.3NH 0402

CRITICAL C6191_RF 0.2PF +/-0.05PF 50V NP0-CERM 0402

RF_ANT_MATCH1 WIFI_50S 50_OHM

CRITICAL J6191_RF MM8030-2600RK0 F-ST-SM

RF_CAL WIFI_50S 50_OHM

CRITICAL C6192_RF 8.2PF +/-0.25PF% 25V NP0-C0G 0201

NOSTUFF L6191_RF 5.6NH-3%-0.35A 0201

RF_CAL_MATCH WIFI_50S 50_OHM

NOSTUFF L6192_RF 5.6NH-3%-0.35A 0201

CRITICAL U6104_RF DPX205850DT-9038A1SJ SM

XW6102_RF SHORT-0402

=BATT_VCC

BATT_VCC_WLAN

C6101_RF 10UF 20% 6.3V CERM-X5R 0402-1

C6102_RF 27PF 5% 16V NP0-C0G 01005

PP_WLAN_VDDIO_1V8 VOLTAGE=1.8V

R6108_RF 0.00 1/32W MF 01005

PP_WL_BT_VDDIO_AP VOLTAGE=1.8V

C6103_RF 0.01UF 10% 10V X5R 01005

C6104_RF 27PF 5% 16V NP0-C0G 01005

NOSTUFF R6105_RF 10K 5% 1/32W MF 01005

R6107_RF 10K 5% 1/32W MF 01005

VDDIO_1P8V

BATT_VCC

VBATT_RF_VCC

VBATT_RF_VCC

32K INTERFACE TO AP

XW6101_RF SHORT-01005

CLK32K_AP

WLAN_CLK32K

CLK32K_AP

GPIO_6

VIN_1P2LDO

WLAN_BUCK_OUT

WL_REG_ON

BT_REG_ON

JTAG_SEL

SR_VLX

WLAN_HSIC_DATA

WLAN_HSIC_STROBE

RF_SW_CTRL_3

U6101_RF LBEE5ZHTWC501 LGA OMIT_TABLE

2G_ANT

5G_ANT

50_WLAN_G

50_WLAN_A

HOST_WAKE_BT

BT_WAKE

BT_UART_RXD

BT_UART_TXD

BT_UART_RTS*

BT_UART_CTS*

BT_PCM_CLK

BT_PCM_SYNC

BT_PCM_OUT

BT_PCM_IN

GPIO_0 HOST_WAKE_WLAN

GPIO_1 AP_HSIC3_RDY

GPIO_2 WLAN_HSIC3_RESUME

GPIO_3 AGG_CHANNEL

GPIO_4 WLAN_UART_RXD

GPIO_5 WLAN_UART_TXD

GPIO_12 HSIC_DEVICE_RDY

CRITICAL C6107_RF 8.2PF +/-0.25PF% 25V NP0-C0G 0201

50_WLAN_G_1

CRITICAL C6108_RF 4.7PF +/-0.1PF 25V COG-CERM 0201

50_WLAN_A_DIPLX

NOSTUFF C6111_RF 0.2PF +/-0.1PF 25V COG-CERM 201

CRITICAL L6111_RF 2.5UH-30%-0.7A-0.24OHM 0603

C6109 4.7UF 20% 6.3V X5R-CERM1 402

R6109_RF 10K 5% 1/32W MF 01005

NC

NO LONGER NEEDED BASED ON AND GATE REMOVAL

R6111_RF 10K 5% 1/32W MF 01005

PULL DOWN RESISTORS

GND

THRML_PAD

GPIO6	SDIO_DATA<1>	SDIO_DATA<2>	MODE	DEFAULT ARM STATE
0	X	X	SDIO	IN RESET
1	X	0	GSPI	IN RESET
1	0	1	HSIC	OUT OF RESET
1	1	1	BOOTLESS HSIC	IN RESET

PP_WL_BT_VDDIO_AP

R6113_RF 10K 5% 1/32W MF 01005

HSIC_DEVICE_RDY

U6102_RF 74AUP1G08GF SOT891

R6112_RF 1.00M 1% 1/32W MF 01005

WLAN_REG_ON

WLAN_REG_ON_RC

C6110_RF 0.22UF 6.3V X5R 0201

NC

DEV_HSIC3_RDY

R6114_RF 0.00 1/32W MF 01005

AGG_CHANNEL

WLAN_TX_BLANK

WLAN_REG_ON

HOST_WAKE_WLAN

AP_HSIC3_RDY

DEV_HSIC3_RDY

WLAN_UART_RXD

WLAN_UART_TXD

PP6101_RF P4MM_SM

PP6102_RF P4MM_SM

PP6103_RF P4MM_SM

PP6104_RF P4MM_SM

PP6105_RF P4MM_SM

PP6106_RF P4MM_SM

PP6107_RF P4MM_SM

AGG_CHANNEL

50_HSIC_WLAN_DATA

50_HSIC_WLAN_STROBE

HSIC_DEVICE_RDY

PP6109_RF P4MM_SM

PP6110_RF P4MM_SM

PP6111_RF P4MM_SM

PP6112_RF P4MM_SM

CHANGE LIST

07FEB2012 MUSHTAQ COPIED FROM N41, ADDED J2 ANT MATCH/CONN
C6107 FROM 20PF TO 8.2PF, C6108 FROM 10PF TO 4.7PF
U6104 FROM SOSHIN TO MURATA LFD212G45DS5D355

13FEB2012 AMANDA CHANGED OMIT TO OMIT_TABLE AND UPDATED
BOM OPTION TABLES TO ALTERNATE TABLES
REMOVED BOM TABLE FOR C6111_RF (NOW ALWAYS NOSTUFF)

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: WIFI/BT

Apple Inc.

DRAWING NUMBER: 051-9385 SIZE: D

REVISION: A.0.0

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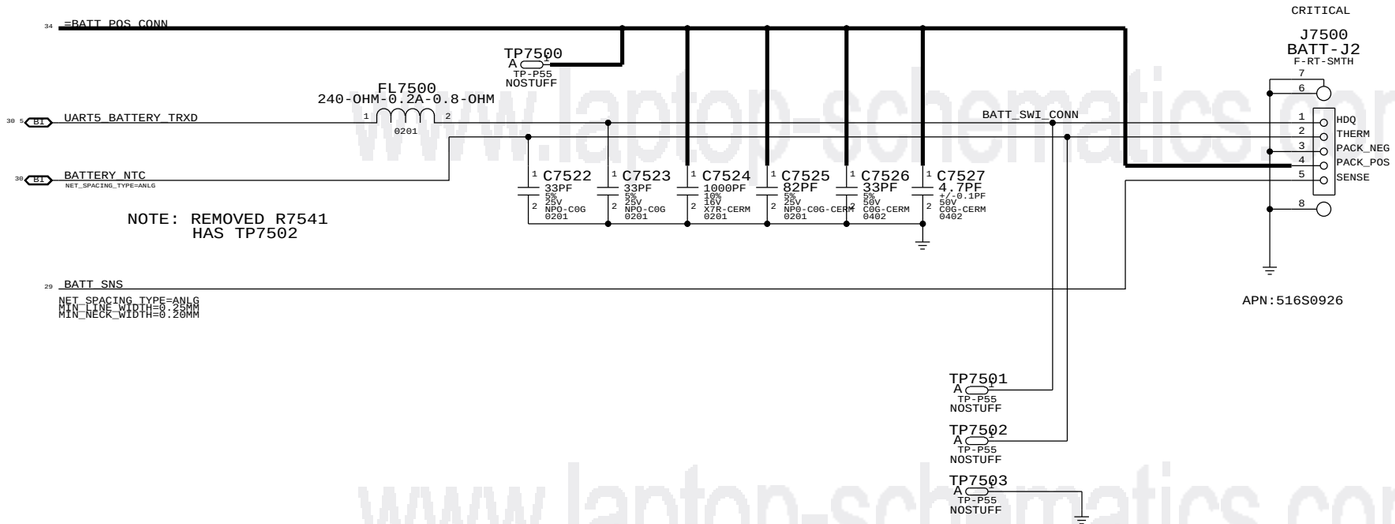
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0644	155S0274	?		RDAR://PROBLEM/11282371

FL7500,L3620,L5550,L5730



SYNC_MASTER=MADHAVI SYNC_DATE=12/06/2011

PAGE TITLE
POWER: BATTERY CONNECTOR

Apple Inc.

DRAWING NUMBER 051-9385 SIZE D
REVISION A.0.0
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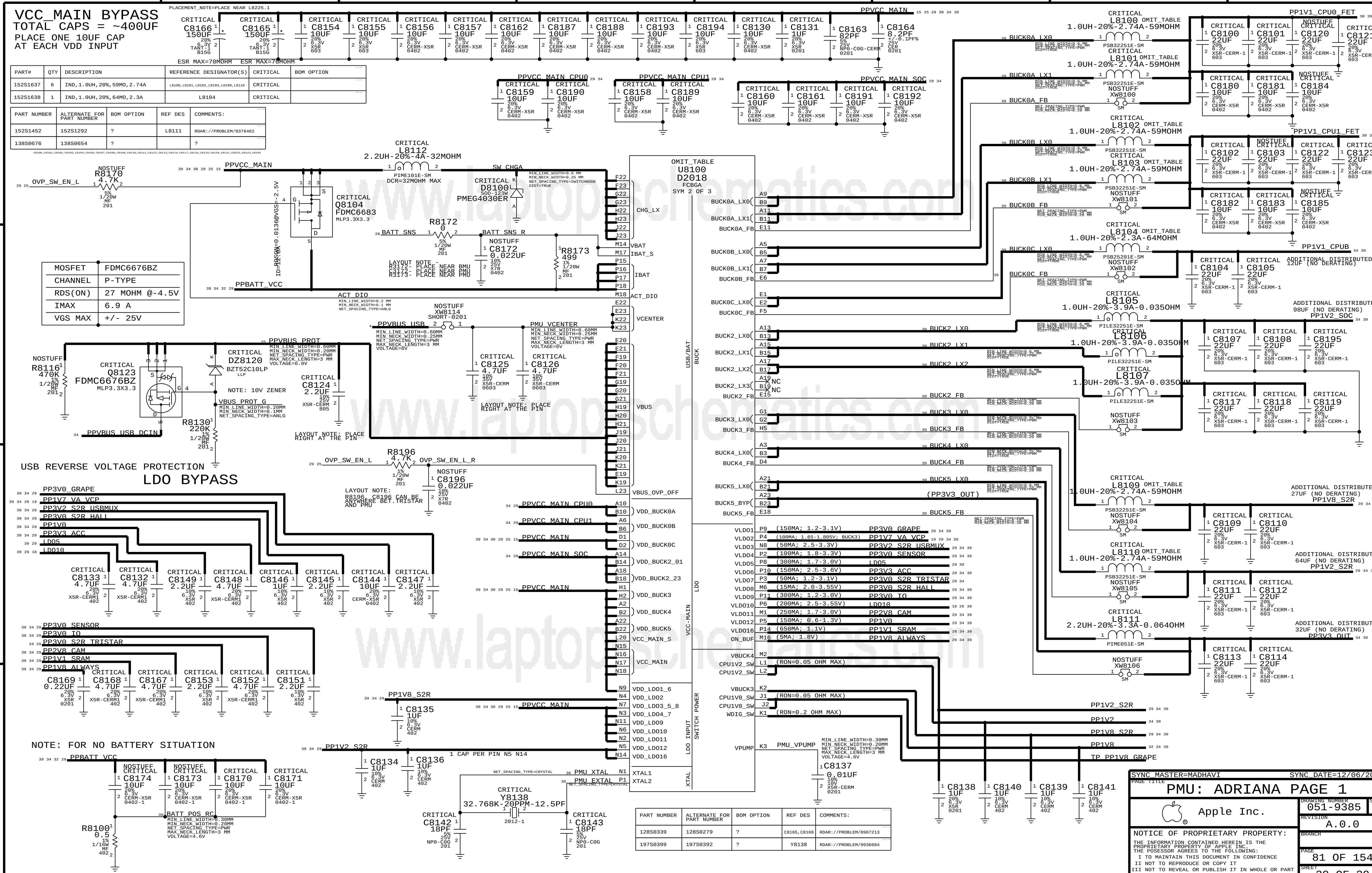
PMU: ADRIANA PAGE 1



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1637	6	IND,1.0UH,20%,59MO,2.74A	L8100,L8101,L8102,L8103,L8109,L8110	CRITICAL	
152S1638	1	IND,1.0UH,20%,64MO,2.3A	L8104	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S1452	152S1292	?	L8111	RDAR://PROBLEM/8376462
138S0676	138S0654	?		?

MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	27 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0339	128S0279	?	C8165,C8166	RDAR://PROBLEM/8967213
197S0399	197S0392	?	Y8138	RDAR://PROBLEM/9936684

SYNC_MASTER=MADHAVI SYNC_DATE=12/06/2011

PAGE TITLE: PMU: ADRIANA PAGE 1

Apple Inc.

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REVISION: A.0.0

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(TEMP5 - TOP SIDE NEAR NAND) BOARD_TEMP5_P
(TEMP6 BOTTOM SIDE NEAR BRIDGE FLEX) BOARD_TEMP6_P

SENSOR LOCATIONS TBD
LOCATION DESCRIPTIONS ARE FROM J2

C8281 100PF 5% 6.3V CERM 01005
C8282 100PF 5% 6.3V CERM 01005
CRITICAL R8281 10KOHM-1%-0.31MW 0201
CRITICAL R8282 10KOHM-1%-0.31MW 0201
XW8282 NOSTUFF
XW8281 NOSTUFF
PLACE XW AND CAP CLOSE TO PMU
PLACE XW AND CAP CLOSE TO PMU

C8292 0.01UF 10% 6.3V X5R 01005
C8206 0.01UF 10% 6.3V X5R 01005
C8207 0.01UF 10% 6.3V X5R 01005

R8299 6.34K 1% 1/20W MF 201
PMU_USB_BRICKID

(INTERNAL PULL-DOWN)
NC_FW_ZENER_PWR

GPIO_BTN_HOME_L
GPIO_BTN_ONOFF_L
GPIO_BTN_SRL_L
PMU_E75_ACC_DET_L

PMU_ACC_ID
PMU_USB_BRICKID_R
ADC_IN7

(TEMP1 - BOTTOM SIDE NEAR H5G)
(TEMP2 - BOTTOM SIDE NEAR PMU)
(TEMP3 - BOTTOM SIDE NEAR I/O FLEX CONN)
(TEMP4 - BOTTOM SIDE NEAR WIFI)

C8215 100PF 5% 6.3V CERM 01005
C8221 100PF 5% 6.3V CERM 01005
C8217 100PF 5% 6.3V CERM 01005
C8223 100PF 5% 6.3V CERM 01005
C8220 100PF 5% 6.3V CERM 01005
CRITICAL R8218 10KOHM-1%-0.31MW 0201
CRITICAL R8222 10KOHM-1%-0.31MW 0201
CRITICAL R8216 10KOHM-1%-0.31MW 0201
0201 CRITICAL R8280 10KOHM-1%-0.31MW
CRITICAL R8219 3.92K 0.1% 402 1/10W MF
XW8200 NOSTUFF
XW8201 NOSTUFF
XW8202 NOSTUFF
XW8203 NOSTUFF
PLACE XW AND CAP CLOSE TO PMU
PLACE XW AND CAP CLOSE TO PMU
PLACE XW AND CAP CLOSE TO PMU
PLACE XW AND CAP CLOSE TO PMU

RESISTOR FOR TEMP CALIBRATION

BOARD_TEMP1
BOARD_TEMP2
BOARD_TEMP3_P
BOARD_TEMP4_P
BOARD_TEMP5_P
BOARD_TEMP6_P
BOARD_TEMP7_P
BOARD_TEMP8_P
BATTERY_NTC
PMU_TCAL

GPIO_PMU_KEEPACT
PMU_SHDWN (INTERNAL PULL-DOWN)
PMU_RESET_IN (INTERNAL PULL-DOWN)
RST_AP_L
GPIO_PMU_IRQ (PULLUP INSIDE H5G)

I2C0_SCL_1V8
I2C0_SDA_1V8

DWI_AP_CLK (INTERNAL PULL-DOWN)
DWI_AP_DO (INTERNAL PULL-DOWN)
DWI_AP_DI

DWI NAMING RELATIVE TO AP

OMIT_TABLE
U8100
D2018
FCBGA
SYM 1 OF 3

FW_DPHP_DET	M19		
BUTTON1	C3	DIGITAL INPUT	REFERENCES
BUTTON2	D3		
BUTTON3	E3		
ACC_DET	C1		
ACC_ID	M8	ANALOG INPUT	
BRICK_ID	M21		
ADC_IN7	L4		
ADC_IN31	L5		
TDEV1	L19	TEMPERATURE	GPIO
TDEV2	K15		
TDEV3	K14		
TDEV4	M13		
TDEV5	M5		
TDEV6	M4		
TDEV7	L3		
TDEV8	M3		
TBAT	L21		
TCAL	M22		
KEEPACT	E10	WDOG	
SHDN	H3		
RESET_IN	G4	RESET	
RESET*	F4		
IRQ*	H4		
SCL	E7	I2C & DWI	ANALOG MUX
SDA	E9		
DWI_CK	A1		
DWI_DI	B1		
DWI_DO	C2		
WLED_LXA	N21	LED BACKLIGHT	LCM/GRAPHE
VOUT_WLED_A	P21		
WLED1_A	K16		
WLED2_A	K5		
WLED3_A	K6		
WLED4_A	K7		
WLED5_A	K8		
WLED6_A	M9		
WLED_LXB	N23		
VOUT_WLED_B	P23		
WLED1_B	K17		
WLED2_B	K10		
WLED3_B	M11		
WLED4_B	K11		
WLED5_B	K12		
WLED6_B	M12		

I2C ADDRESS: 0111100X (0X78)

IREF	M7	PMU_IREF	
VREF	P7	PMU_VREF	
VDD_REF	K18	PMU_VDD_REF	
VDD_REF_A	M15		
VDD_RTC	N10	PMU_VDD_RTC	
ADC_REF	M10	PMU_ADC_REF	
GPIO1	D5	PMU_GPIO_CLK_32K_GRAPE	USED BY Z2
GPIO2	C5	PMU_GPIO_CLK_32K_WLAN	(1.8_S2R PUSH-PULL)
GPIO3	C6	PMU_GPIO_BT_REG_ON	(1.8_S2R;NO PD REQ'D PER BB TEAM)
GPIO4	C7	PMU_GPIO_WLAN_REG_ON	(1.8_S2R;NO PD REQ'D PER BB TEAM)
GPIO5	C8	PMU_GPIO_BB_PMU_RST_L	
GPIO6	C9	UART5_BATTERY_TRXD	(2.5V ALWAYS ON PU IN BMU)
GPIO7	C10	PMU_GPIO_BT_HOST_WAKE	(INTERNAL PD)
GPIO8	C11	PMU_GPIO_WLAN_HOST_WAKE	(INTERNAL PD)
GPIO9	C12	PMU_GPIO_BB_HOST_WAKE	(INTERNAL PD; CAN'T BE USED FOR 32K CLK OUTPUT)
GPIO10	C13	PMU_GPIO_CODEC_HS_INT_L	(INTERNAL PU TO PP1V8_S2R)
GPIO11	C14	PMU_GPIO_BBUSBTODOCK_EN	
GPIO12	C15	PMU_GPIO_TS_INT	NEED RADAR TO STOP GENERATING 32K CLOCK
GPIO13	C16	PMU_GPIO_HALL2_IRQ	
GPIO14	C17	PMU_GPIO_CODEC_RST_L	
GPIO15	C18	PMU_GPIO_HALL_IRQ	
GPIO16	C19	NC_PMU_GPIO16	
GPIO17	C20	PMU_GPIO_BB_VBUS_DET	
AMUX_A0	C21	NC	
AMUX_A1	C22	NC	
AMUX_A2	E14	NC	
AMUX_A3	E13	NC	
AMUX_AY	C23	NC	
AMUX_B0	D22	NC	
AMUX_B1	D21	NC	
AMUX_B2	D19	NC	
AMUX_B3	E12	NC	
AMUX_BY	D23	NC	
VDD_LCM_SW	N19	PPVCC_MAIN	
VDD_BOOST_LCM	P19	PP6V0_LCM_HT	
BOOST_LCM_LX	P20	LCM_LX	
VDD_LCM	N13	PP6V0_LCM_VBOOST	
LCM2_EN	F3	TP_LCM2_EN	
LCM_FB	M20		
VLCM1	P13	NC_VLCM1	
VLCM2	P12	NC_VLCM2	
VLCM3	N12		
CPUA_EN	M23	CPU0_SWITCH	
CPUA_SW_G	J5	CPU0_SW_G	
CPUA_SW_S	J4	CPU0_SW_S	
CPUB_EN	L22	CPU1_SWITCH	
CPUB_SW_G	J3	CPU1_SW_G	
CPUB_SW_S	K4	CPU1_SW_S	
DPHP	E4	NC_PMU_DP_HPD	

C8204 0.1UF 10% 6.3V X5R 201
R8203 200K 1% 1/20W MF 201
C8212 0.1UF 10% 6.3V X5R 201
C8209 1UF 10% 6.3V X5R 402
C8210 0.22UF 20% 6.3V X5R 0201
PLACEMENT NOTE: PLACE NEAR PIN K4
PLACEMENT NOTE: PLACE NEAR PIN K24
C8214 1000PF 10% 6.3V X5R-CERM 01005

BB_VBUS_DET STUFFING OPTION
SELECTING GPIO OPTION BY DEFAULT
REMOVE STUFFING RES AND WIRE DIRECTLY FOR PRODUCTION
R8297 0.00 5% 1/32W MF 01005
R8296 0.00 5% 1/32W MF 01005
NOSTUFF

NOSTUFF CRITICAL L8229 2.2UH-1.05A-0.195OHM (NOTE: 2MHZ)
VLS201612E-SM
NOSTUFF CRITICAL D8230 PMEG2005AEL SOD882

(INTERNAL PULLDOWN; TE ENABLE)

NOSTUFF C8236 2.2UF 20% 10V X5R-CERM 402
NOSTUFF C8237 10UF 20% 25V X5R-CERM 0603
NOSTUFF C8239 1UF 10% 10V X5R 402
NOSTUFF C8238 1UF 10% 10V X5R 402
VLCM3

NOSTUFF R8290 1M 5% 1/20W MF 201
NOSTUFF C8290 0.1UF 10% 16V X5R-CERM 0201
R8292 0 5% 1/20W MF 201
CPU0_SW_G_R
CPU0_SW_S
XW8290 NOSTUFF
PP1V1_CPU0

NOSTUFF R8291 1M 5% 1/20W MF 201
NOSTUFF C8291 0.1UF 10% 16V X5R-CERM 0201
R8293 0 5% 1/20W MF 201
CPU1_SW_G_R
CPU1_SW_S
XW8291 NOSTUFF
PP1V1_CPU1

Q8202 CSD58874W1015 BGA
Q8200 CSD58874W1015 BGA
Q8201 CSD58874W1015 BGA
Q8203 CSD58874W1015 BGA
PP1V1_CPU0_FET
PP1V1_CPU1_FET

CRITICAL L8225 4.7UH-3.2A PIME051E-SM DCR=106MOHM MAX
CRITICAL D8228 PMEG4010BEA SOD-323
=PPVCC_MAIN_LED
CRITICAL C8226 10UF 20% 10V X5R 0603-1
PPLED_OUT_A
CRITICAL C8232 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8233 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8234 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8235 4.7UF 10% 35V X5R-CERM 0603

WLED_LX_A
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
NET_SPACING_TYPE=SWITCHNODE
DIDT=TRUE
(PPLED_OUT_A)

LED_IO_1_A R8227 1.00 1% 1/20W MF 201
LED_IO_2_A R8231 1.00 1% 1/20W MF 201
LED_IO_3_A R8232 1.00 1% 1/20W MF 201
LED_IO_4_A R8235 1.00 1% 1/20W MF 201
LED_IO_5_A R8239 1.00 1% 1/20W MF 201
LED_IO_6_A R8240 1.00 1% 1/20W MF 201

CRITICAL L8255 4.7UH-3.2A PIME051E-SM DCR=106MOHM MAX
CRITICAL D8258 PMEG4010BEA SOD-323
=PPVCC_MAIN_LED
CRITICAL C8256 10UF 20% 10V X5R 0603-1
PPLED_OUT_B
CRITICAL C8262 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8263 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8264 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8265 4.7UF 10% 35V X5R-CERM 0603

WLED_LX_B
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
(PPLED_OUT_B)

LED_IO_1_B R8257 1.00 1% 1/20W MF 201
LED_IO_2_B R8261 1.00 1% 1/20W MF 201
LED_IO_3_B R8262 1.00 1% 1/20W MF 201
LED_IO_4_B R8265 1.00 1% 1/20W MF 201
LED_IO_5_B R8269 1.00 1% 1/20W MF 201
LED_IO_6_B R8270 1.00 1% 1/20W MF 201

PPLED_OUT_A
C8201 0.01UF 10% 50V X7R 402
C8266 0.01UF 10% 50V X7R 402
PLACEMENT_NOTE=PLACE NEAR U8100.K16
PPLED_OUT_B
C8251 0.01UF 10% 50V X7R 402
C8267 0.01UF 10% 50V X7R 402
PLACEMENT_NOTE=PLACE NEAR U8100.K17

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
107S0150	107S0208	?		RDAR://PROBLEM/8380367

R8216,R8218,R8222,R8280,R8281,R8282

SYNC_MASTER=MADHAVI SYNC_DATE=12/06/2011
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OMIT_TABLE

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C4		A8	
D20		VSS/VSS_BUCK0A0B	B8
F6		A12	
F7		VSS/VSS_BUCK0A2	B12
F8		A4	
F9		VSS/VSS_BUCK0B4	B4
F10		F1	
F11		VSS/VSS_BUCK0C3	F2
F12			
F13		A16	
F14		VSS/VSS_BUCK2_01	B16
F15		A20	
F16		VSS/VSS_BUCK25	B20
F17			
G3		VSS/VSSA_BUCK0A	E12
G5		VSS/VSSA_BUCK0B	E8
G7		VSS/VSSA_BUCK0C	G6
G8		VSS/VSSA_BUCK2	E16
G9		VSS/VSSA_BUCK3	H6
G10		VSS/VSSA_BUCK4	E5
G11	VSS	VSS/VSSA_BUCK5	F18
G12			
G13		VSS_WLED	N22
G14		VSS_WLED	P22
G15		VSS_LCM	N20
G16			
G17		J6	
G18		J7	
H7		J8	
H8		J9	
H9		J10	
H10		J11	
H11		J12	
H12		VSS	J13
H13		J14	
H14		J15	
H15		J16	
H16		J17	
H17		J18	
H18			

ADD A VIA PER PIN FOR ALL VSS_* AND VSSA_* PINS

SYNC_MASTER=MADHAVI SYNC_DATE=12/06/2011

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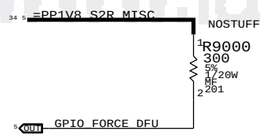
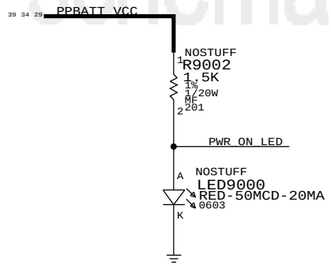
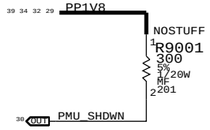
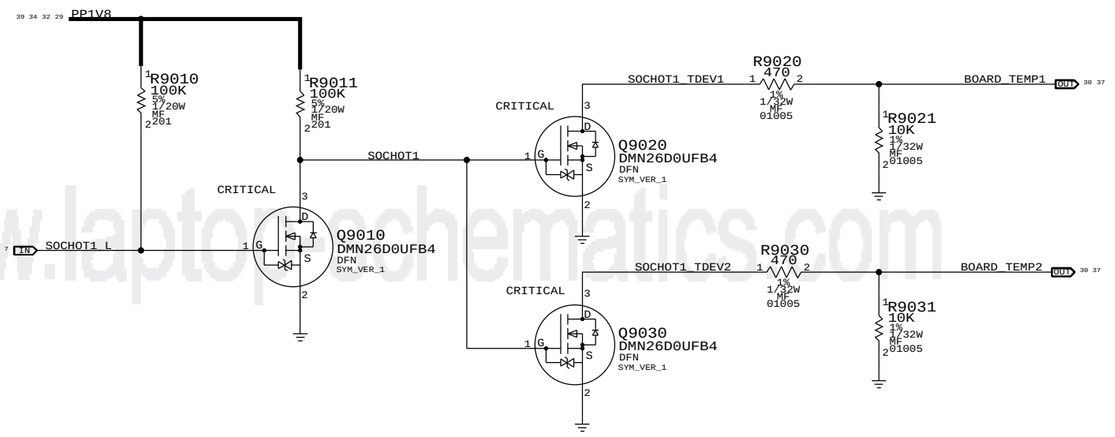
DEBUG RESET ACCESS







SOCHOT TO PMU TDEV1/TDEV2



SYNC_MASTER=MLB SYNC_DATE=11/09/2011

PAGE TITLE
DEBUG/MISC.

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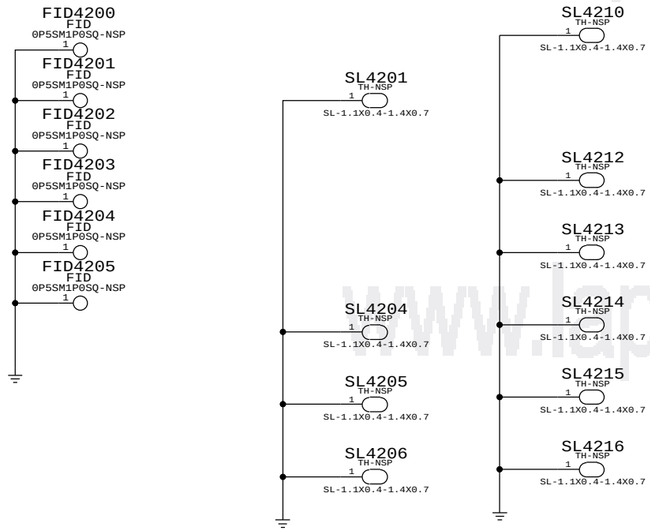
PLATED THROUGH HOLES

DRILL SIZE: 1.1MM X 0.4MM
PLATING SIZE: 1.4MM X 0.7MM



SYNC_MASTER=N/A SYNC_DATE=N/A

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POWER CONNECTIONS

BUCK0A

39 30 PP1V1_CPU0 → =PPVDD_CPU0_H5 9
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

BUCK0B

39 30 PP1V1_CPU1 → =PPVDD_CPU1_H5 9
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

BUCK0C

39 29 PP1V1_CPUB → =PPVDD_CPUB_H5 9
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

BUCK2

39 29 PP1V2_SOC → =PPVDD_SOC_H5 9
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

BUCK3

39 29 PP1V8_S2R
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.15 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP1V8_S2R_MISC 6 32
→ VDDIO_WLAN_BT_1V8 14
→ =PP1V8_S2R_USBMUX 25
→ =PP1V8_S2R_DDR 11 12

BUCK4

39 29 PP1V2_S2R
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP1V2_S2R_H5 8
→ =PP1V2_S2R_DDR 11 12

BUCK3_SW

CPU1V8_SW

32 29 39 PP1V8
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3MM
→ =PP1V8_SENSOR 21
→ =PP1V8_AUDIO 18
→ =PP1V8_VDDIO18_H5 4 6 7 9
→ =PP1V8_H5 4 5 7 10
→ =PP1V8_MIPI_H5 7
→ =PP1V8_DP_H5 7
→ =PP1V8_EDP_H5 7
→ =PP1V8_NAND_H5 6 9
→ =PP1V8_NAND 13
→ =PP1V8_PLL_H5 4
→ =PP1V8_MISC 16

BUCK4_SW

CPU1V2_SW

39 29 PP1V2
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP1V2_VDDQ_DDR 11 12
→ =PP1V2_VDDIOD_H5 8 9
→ =PP1V2_HSIC_H5 4

BUCK5

39 29 PP3V3_OUT
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V3_NAND 13
→ =PP3V3_USB_H5 4
→ =PP3V3_LCD 15

BACKLIGHT BOOST

39 30 PPLED_OUT_A → =PPLED_REG_A 15
MAKE_BASE=TRUE
VOLTAGE=20.4V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

39 30 PPLED_OUT_B → =PPLED_REG_B 15
MAKE_BASE=TRUE
VOLTAGE=20.4V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO1

39 29 PP3V0_GRAPE → =PP3V0_GRAPE 16 17
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V0_GRAPE_MARIO1 16
→ =PP3V0_GRAPE_Z1 17
→ =PP3V0_GRAPE_Z2 17

LDO2

39 29 19 PP1V7_VA_VCP → =PP1V7_VA_VCP 18 19
MAKE_BASE=TRUE
VOLTAGE=1.7V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO3 (NO LONGER NEEDED)

39 29 PP3V2_S2R_USBMUX → =PP3V2_S2R_USBMUX 25
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO4

39 29 PP3V0_SENSOR → =PP3V0_SENSOR 21
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO6

39 29 PP3V3_ACC → =PP3V3_ACC 25
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO7

29 PP3V0_S2R_TRISTAR → =PP3V0_S2R_TRISTAR 25
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO8

39 29 PP3V0_S2R_HALL → 1027 =PP3V0_S2R_HALL 21 23
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO9

39 29 PP3V0_IO → =PP3V0_VDDIO30_H5 9
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO11

39 29 PP2V8_CAM → =PP2V8_CAM 21
MAKE_BASE=TRUE
VOLTAGE=2.8V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO12

39 29 PP1V0 → =PP1V0_MIPI_H5 7
MAKE_BASE=TRUE
VOLTAGE=1.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP1V0_DP_PAD_DVDD_H5 7
→ =PP1V0_EDP_PAD_DVDD_H5 7
→ =PP1V0_USB_H5 4
→ =PP1V0_HSIC_H5 4
→ =PP1V0_MIPI_PLL_H5 7

LDO16

39 29 PP1V1_SRAM → =PPVDD_SRAM_H5 9
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

39 29 PP1V8_ALWAYS → =PP1V8_ALWAYS 5
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

CHARGER MAIN

39 30 29 25 15 PPVCC_MAIN
MAKE_BASE=TRUE
VOLTAGE=4.7V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PPVCC_MAIN_AUDIO 18 19
→ =PPVCC_MAIN_LED 30
→ PPVCC_MAIN_CPU0 29
→ PPVCC_MAIN_CPU1 29
→ PPVCC_MAIN_SOC 29

BATTERY

39 32 29 PPBATT_VCC
MAKE_BASE=TRUE
VOLTAGE=4.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =BATT_POS_CONN 28
→ =BATT_POS_F_3G 26 CELLULAR RADIO
→ =BATT_VCC 27 WLAN

USB POWER INPUT

39 23 PPVBUS_USB_EMI → PPVBUS_USB_DCIN 29
MAKE_BASE=TRUE
VOLTAGE=0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.15 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

SYNC_MASTER=N/A SYNC_DATE=N/A

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POWER ALIASES

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MLB CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,BOTTOM	NO_TYPE,BGA,BGA06-06,BGA_P4	MM	16.2

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	3.0 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

SINGLE-ENDED PHYSICAL RULES 45 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.105 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL2,ISL9	Y	0.055 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL3,ISL8	Y	0.065 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL4,ISL7	Y	0.053 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL5	Y	0.072 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL6	Y	0.059 MM	0.055 MM	3.0 MM		

90 OHMS DIFFERENTIAL PAIR PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP,BOTTOM	Y	0.090 MM	0.090 MM	=STANDARD	0.170 MM	0.170 MM
90_OHM_DIFF	ISL2,ISL9	Y	0.062 MM	0.062 MM	=STANDARD	0.190 MM	0.190 MM
90_OHM_DIFF	ISL3,ISL8	Y	0.062 MM	0.052 MM	=STANDARD	0.190 MM	0.190 MM
90_OHM_DIFF	ISL4,ISL7	Y	0.051 MM	0.051 MM	=STANDARD	0.190 MM	0.190 MM
90_OHM_DIFF	ISL5,ISL6	Y	0.052 MM	0.052 MM	=STANDARD	0.105 MM	0.105 MM

DDR 45 OHMS SINGLE-ENDED PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DDR_45_OHM_SE	TOP,BOTTOM	Y	0.105 MM	0.105 MM	3.0 MM		
DDR_45_OHM_SE	ISL2	Y	0.055 MM	0.055 MM	3.0 MM		
DDR_45_OHM_SE	ISL3	Y	0.065 MM	0.065 MM	3.0 MM		
DDR_45_OHM_SE	ISL4	Y	0.053 MM	0.053 MM	3.0 MM		
DDR_45_OHM_SE	ISL5,ISL6	Y	0.072 MM	0.072 MM	3.0 MM		
DDR_45_OHM_SE	*	N	0.055 MM	0.055 MM	3.0 MM		

DDR 90 OHMS DIFFERENTIAL PAIR PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DDR_90_OHM_DIFF	TOP,BOTTOM	Y	0.090 MM	0.090 MM	=STANDARD	0.170 MM	0.170 MM
DDR_90_OHM_DIFF	ISL2	Y	0.062 MM	0.062 MM	=STANDARD	0.190 MM	0.190 MM
DDR_90_OHM_DIFF	ISL3	Y	0.062 MM	0.062 MM	=STANDARD	0.190 MM	0.190 MM
DDR_90_OHM_DIFF	ISL4	Y	0.051 MM	0.051 MM	=STANDARD	0.190 MM	0.190 MM
DDR_90_OHM_DIFF	ISL5,ISL6	Y	0.066 MM	0.066 MM	=STANDARD	0.180 MM	0.180 MM
DDR_90_OHM_DIFF	*	N	0.056 MM	0.056 MM	=STANDARD	0.180 MM	0.180 MM

WIFI PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
WIFI_50S	TOP,BOTTOM	Y	0.245 MM	0.2 MM	=STANDARD		
WIFI_50S	*	N	=STANDARD	=STANDARD	=STANDARD		
WIFI_PWR100	*	Y	0.10 MM	0.050 MM	=STANDARD		
WIFI_PWR1000	*	Y	1.00 MM	0.100 MM	=STANDARD		

MISC PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.08 MM	0.08 MM
SPEAKER	*	Y	0.5 MM	0.20 MM	10 MM	0.10 MM	0.10 MM
AUDIO_DIFF	*	Y	0.1 MM	0.09 MM	10 MM	0.10 MM	0.10 MM
LED	*	Y	0.1 MM	0.09 MM	10 MM	0.08 MM	0.08 MM
TEMP_SENSE	*	Y	0.1 MM	0.09 MM	10 MM	0.08 MM	0.08 MM

BGA AREA PHYSICAL RULES

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	BGA_PHY

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BGA_PHY	*	Y	0.060 MM	0.060 MM	=STANDARD	0.076 MM	0.075 MM

TCF VERSION (USING SPACING RULE)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TCF_VERSION	*	0.104 MM	?

0.104 - 11/30/2011

J1 TCF_VERSION NC_UART5_TXD 5 ASSIGNING RULE TO NC NET

SPACING CONSTRAINTS

DEFAULT/BGA SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.100 MM	?
STANDARD	*	=DEFAULT	?
BGA_SPA	*	=DEFAULT	?
BGA_P4_SPA	*	0.200 MM	?

REGULAR SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.050 MM	?
0P08_SPACING	*	0.080 MM	?
1.5:1_SPACING	*	0.075 MM	?
2:1_SPACING	*	0.100 MM	?
2.5:1_SPACING	*	0.125 MM	?
3:1_SPACING	*	0.150 MM	?
4:1_SPACING	*	0.200 MM	?
5:1_SPACING	*	0.250 MM	?
0P5MM_SPACING	*	0.5 MM	?
0P64MM_SPACING	*	0.64 MM	?
0P2_SPACING	*	0.20 MM	?

POWER/GND SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR_P1SPACING	*	0.1 MM	
GND_P1SPACING	*	0.1 MM	
SWITCHNODE	*	0.2 MM	

POWER

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PWR	*	Y	0.6MM	0.20 MM	3.0 MM		
GND_PH	*	Y	0.6MM	0.075 MM	3.0 MM		
PWR_PMU	*	Y	0.6MM	0.20 MM	3.0 MM		

MISC

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_SPA
CLK	*	BGA	BGA_SPA
GND	*	*	GND_P1SPACING
SWITCHNODE	*	*	SWITCHNODE
ANLG	*	*	3:1_SPACING
*	*	BGA_P4	BGA_P4_SPA

NOTES:

0.075 MM ~ 3 MIL
0.089 MM ~ 3.5 MIL
0.102 MM ~ 4 MIL
0.114 MM ~ 4.5 MIL
0.125 MM ~ 5 MIL
0.140 MM ~ 5.5 MIL
0.15 MM ~ 6 MIL
0.18 MM ~ 7 MIL
0.2 MM ~ 8 MIL
0.25 MM ~ 10 MIL
0.3 MM ~ 12 MIL
0.33 MM ~ 13 MIL
0.4 MM ~ 16 MIL
1.0 MM = 39.37 MIL

SYNC_MASTER=MIKE SYNC_DATE=11/30/2011

PAGE TITLE: CONSTRAINTS: MLB RULES

Apple Inc.

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Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK	*	*	3:1_SPACING

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	CLK_50S	CLK	PMU_GPIO_CLK_32K_GRAPE 17 30
	CLK_50S	CLK	PMU_GPIO_CLK_32K_WLAN 14 30
	CLK_50S	CLK	ISP1_CAM_FF_CLK 7 22
	CLK_50S	CLK	CONN_ISP1_CAM_FF_CLK 20 22
	CLK_50S	CLK	ISP0_CAM_RF_CLK 7 22
	CLK_50S	CLK	CONN_ISP0_CAM_RF_CLK 20 22
	I2S_50S	I2S	I2S0_CODEC_ASP_MCK 5 36
	I2S_50S	I2S	I2S0_CODEC_ASP_MCK_R 5 18 36
	CLK_50S	CLK	ISP0_CAM_RF_CLK_R 7
	CLK_50S	CLK	ISP1_CAM_FF_CLK_R 7
	CLK_50S	CLK	ISP1_CAM_FF_C 22
	CLK_50S	CLK	ISP0_CAM_RF_C 22
	CLK_50S	CLK	ISP1_CAM_FF_FILT 22
	CLK_50S	CLK	ISP0_CAM_RF_FILT 22

UART

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
UART_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
UART	*	*	3:1_SPACING
UART	UART	*	2:1_SPACING

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	UART_50S	UART	UART2_TS_ACC_RXD 5 25
	UART_50S	UART	UART2_TS_ACC_TXD 5 25
	UART_50S	UART	UART4_WLAN_RXD 5 14
	UART_50S	UART	UART4_WLAN_TXD 5 14
	UART_50S	UART	UART1_BB_CTS_L 5 26
	UART_50S	UART	UART1_BB_RTS_L 5 26
	UART_50S	UART	UART1_BB_TXD 5 25 26
	UART_50S	UART	UART1_BB_RXD 5 25 26
	UART_50S	UART	UART3_BT_CTS_L 5 14
	UART_50S	UART	UART3_BT_RTS_L 5 14
	UART_50S	UART	UART3_BT_RXD 5 14
	UART_50S	UART	UART3_BT_TXD 5 14
	UART_50S	UART	UART6_AP_RXD 5 25
	UART_50S	UART	UART6_AP_TXD 5 25

SPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SPI_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	2:1_SPACING

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	SPI_50S	SPI	SPI3_GRAPE_MISO 5 16
	SPI_50S	SPI	SPI3_GRAPE_MOSI 5 16
	SPI_50S	SPI	SPI3_GRAPE_SCLK 5 16
	SPI_50S	SPI	SPI3_GRAPE_CS_L 5 16
	SPI_50S	SPI	SPI2_IPC_MISO
	SPI_50S	SPI	SPI2_IPC_MOSI
	SPI_50S	SPI	SPI2_IPC_SCLK
	SPI_50S	SPI	GPIO_BB_HSIC_RESUME 5 26
	SPI_50S	SPI	SPI1_CODEC_MISO 5 18
	SPI_50S	SPI	SPI1_CODEC_MOSI 5 18
	SPI_50S	SPI	SPI1_CODEC_SCLK 5 18
	SPI_50S	SPI	SPI1_CODEC_CS_L 5 18

DWI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DWI	*	*	2:1_SPACING

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
		DWI	DWI_AP_CLK 5 30
		DWI	DWI_AP_DI 5 30
		DWI	DWI_AP_DO 5 30

JTAG

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
JTAG	*	*	2:1_SPACING

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
		JTAG	JTAG_AP_TCK 4 25
		JTAG	JTAG_AP_TMS 4 25
		JTAG	JTAG_AP_TDI 4
		JTAG	TP_JTAG_AP_TDO 4
		RST	JTAG_AP_TRST_L 4 10 39

I2C

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2C_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2C	*	*	1.5:1_SPACING

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	I2C_50S	I2C	I2C1_SDA_1V8 5 22
	I2C_50S	I2C	I2C1_SCL_1V8 5 22
	I2C_50S	I2C	I2C0_SDA_1V8 5 19 25 30
	I2C_50S	I2C	I2C0_SCL_1V8 5 19 25 30
	I2C_50S	I2C	I2C2_SDA_3V0 5 22
	I2C_50S	I2C	I2C2_SCL_3V0 5 22
	I2C_50S	I2C	ISP0_CAM_RF_I2C_SCL 7 22
	I2C_50S	I2C	ISP0_CAM_RF_I2C_SDA 7 22
	I2C_50S	I2C	ISP1_CAM_FF_I2C_SCL 7 22
	I2C_50S	I2C	ISP1_CAM_FF_I2C_SDA 7 22
	I2C_50S	I2C	CONN_I2C1_SDA_1V8 20 22
	I2C_50S	I2C	CONN_I2C1_SCL_1V8 20 22
	I2C_50S	I2C	CONN_I2C2_SCL_3V0 20 22
	I2C_50S	I2C	CONN_I2C2_SDA_3V0 20 22
	I2C_50S	I2C	CONN_ISP0_CAM_RF_I2C_SCL 20 22
	I2C_50S	I2C	CONN_ISP0_CAM_RF_I2C_SDA 20 22
	I2C_50S	I2C	CONN_ISP1_CAM_FF_I2C_SCL 20 22
	I2C_50S	I2C	CONN_ISP1_CAM_FF_I2C_SDA 20 22

XTAL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRYSTAL	*	*	5:1_SPACING

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
		CRYSTAL	XTAL_AP_24M_I 4
		CRYSTAL	XTAL_AP_24M_O 4
		CRYSTAL	AP_24M_O 4
		CRYSTAL	PMU_XTAL 29
		CRYSTAL	PMU_EXTAL 29

I2S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2S_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2S	*	*	3:1_SPACING
I2S	I2S	*	2:1_SPACING

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	I2S_50S	I2S	I2S0_CODEC_ASP_BCLK 5 18
	I2S_50S	I2S	I2S0_CODEC_ASP_LRCK 5 18
	I2S_50S	I2S	I2S0_CODEC_ASP_DIN 5 18
	I2S_50S	I2S	I2S0_CODEC_ASP_DOUT 5 18
	I2S_50S	I2S	I2S0_CODEC_ASP_SDOUT 18
	I2S_50S	I2S	I2S0_CODEC_ASP_MCK 5 36
	I2S_50S	I2S	I2S0_CODEC_ASP_MCK_R 5 18 36
	I2S_50S	I2S	I2S3_CODEC_XSP_BCLK 5 18
	I2S_50S	I2S	I2S3_CODEC_XSP_LRCK 5 18
	I2S_50S	I2S	I2S3_CODEC_XSP_DIN 5 18
	I2S_50S	I2S	I2S3_CODEC_XSP_DOUT 5 18
	I2S_50S	I2S	I2S0_CODEC_XSP_SDOUT
	I2S_50S	I2S	I2S2_BT_BCLK 5 14
	I2S_50S	I2S	I2S2_BT_LRCK 5 14
	I2S_50S	I2S	I2S2_BT_DIN 5 14
	I2S_50S	I2S	I2S2_BT_DOUT 5 14

USB

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	*	*	4:1_SPACING

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	USB_90D	USB	USB_AP_P 4 25
	USB_90D	USB	USB_AP_N 4 25
	USB_90D	USB	USB_BBMUX_BB_P 25 26
	USB_90D	USB	USB_BBMUX_BB_N 25 26
	USB_90D	USB	USB_TS_BBMUX_P 25
	USB_90D	USB	USB_TS_BBMUX_N 25
	USB_90D	USB	USB11_AP_BBMUX_P 4 25
	USB_90D	USB	USB11_AP_BBMUX_N 4 25
	USB_90D	USB	CONN_E75_DPAIR1_P 24 25
	USB_90D	USB	CONN_E75_DPAIR1_N 24 25
	USB_90D	USB	CONN_E75_DPAIR2_P 24 25
	USB_90D	USB	CONN_E75_DPAIR2_N 24 25
	USB_90D	USB	TS_E75_DPAIR1_P 25
	USB_90D	USB	TS_E75_DPAIR1_N 25
	USB_90D	USB	TS_E75_DPAIR2_P 25
	USB_90D	USB	TS_E75_DPAIR2_N 25

HSIC

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
HSIC	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HSIC	*	*	4:1_SPACING
HSIC_RDY	*	*	2:1_SPACING

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	HSIC	HSIC	HSIC3_BB_DATA 4 26
	HSIC	HSIC	HSIC3_BB_STB 4 26
	HSIC	HSIC	HSIC1_WLAN_DATA 4 14
	HSIC	HSIC	HSIC1_WLAN_STB 4 14
	HSIC	HSIC_RDY	GPIO_BB_HSIC_DEV_RDY 5 26
	HSIC	HSIC_RDY	GPIO_BB_HSIC_HOST_RDY 5 26
	HSIC	HSIC_RDY	GPIO_WLAN_HSIC_HOST_RDY 5 14 36
	HSIC	HSIC_RDY	GPIO_WLAN_HSIC_HOST_RDY 5 14 36
	HSIC	HSIC_RDY	GPIO_WLAN_HSIC_DEV_RDY 5 14

SYNC_MASTER=MIKE SYNC_DATE=11/30/2011

PAGE TITLE
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MIPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MIPI_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI0C	*	*	4:1_SPACING
MIPI1C	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
J315	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_CLK_P	7 21
J316	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_CLK_N	7 21
J342	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_P<0>	7 21
J342	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_N<0>	7 21
J311	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_P<1>	7 21
J312	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_N<1>	7 21
J305	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_CLK_F_P	20 21
J304	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_CLK_F_N	20 21
J519	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_F_P<0>	20 21
J518	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_F_N<0>	20 21
J521	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_F_P<1>	20 21
J520	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_F_N<1>	20 21
J345	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_CLK_P	7 21
J346	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_CLK_N	7 21
J347	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_DATA_P<0>	7 21
J348	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_DATA_N<0>	7 21
J364	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_CLK_F_P	20 21
J356	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_CLK_F_N	20 21
J415	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_DATA_F_P<0>	20 21
J414	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_DATA_F_N<0>	20 21

AUDIO/SPEAKER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
J684	AUDIO_DIFF	AUDIO	HP_MIC_P	18
J685	AUDIO_DIFF	AUDIO	HP_MIC_N	18
J587	AUDIO_DIFF	AUDIO	L81_AIN2_P	18
J586	AUDIO_DIFF	AUDIO	L81_AIN2_N	18
J589	AUDIO_DIFF	AUDIO	SPKR_L_VSENSE_N_FILT	19
J588	AUDIO_DIFF	AUDIO	SPKR_L_VSENSE_P_FILT	19
J591	AUDIO_DIFF	AUDIO	SPKR_L_VSENSE_N	19
J590	AUDIO_DIFF	AUDIO	SPKR_L_VSENSE_P	19
J692	AUDIO_DIFF	AUDIO	SPKR_R_VSENSE_N_FILT	19
J693	AUDIO_DIFF	AUDIO	SPKR_R_VSENSE_P_FILT	19
J694	AUDIO_DIFF	AUDIO	SPKR_R_VSENSE_N	19
J695	AUDIO_DIFF	AUDIO	SPKR_R_VSENSE_P	19
J597	SPEAKER	AUDIO	SPKR_L_P	19
J596	SPEAKER	AUDIO	SPKR_L_N	19
J608	SPEAKER	AUDIO	SPKR_L_CONN_P	19
J609	SPEAKER	AUDIO	SPKR_L_CONN_N	19
J606	SPEAKER	AUDIO	SPKR_R_P	19
J607	SPEAKER	AUDIO	SPKR_R_N	19
J608	SPEAKER	AUDIO	SPKR_R_CONN_P	19
J609	SPEAKER	AUDIO	SPKR_R_CONN_N	19
J610	SPEAKER	AUDIO	SPKR_L_FLR	19
J611	SPEAKER	AUDIO	SPKR_R_FLR	19
J564	AUDIO_DIFF	AUDIO	SPKR_L_SES_N	19
J565	AUDIO_DIFF	AUDIO	SPKR_L_SES_P	19
J566	AUDIO_DIFF	AUDIO	SPKR_R_SES_N	19
J586	AUDIO_DIFF	AUDIO	SPKR_R_SES_P	19
J579	USB_90D	USB	MIKEY_TS_P	18 25
J569	USB_90D	USB	MIKEY_TS_N	18 25
J600	USB_90D	USB	L81_MBUS_P	18
J601	USB_90D	USB	L81_MBUS_N	18

EMBEDDED DISPLAYPORT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
EDP_90D	*	90_OHM_DIFF

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
EDP_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
EDP	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
J435	EDP_90D	EDP	EDP_AUX_P	7 15
J436	EDP_90D	EDP	EDP_AUX_N	7 15
J437	EDP_50S	EDP	EDP_HPD	7 15
J439	EDP_90D	EDP	EDP_DATA_P<0>	7 15
J438	EDP_90D	EDP	EDP_DATA_N<0>	7 15
J440	EDP_90D	EDP	EDP_DATA_P<1>	7 15
J442	EDP_90D	EDP	EDP_DATA_N<1>	7 15
J441	EDP_90D	EDP	EDP_DATA_P<2>	7 15
J444	EDP_90D	EDP	EDP_DATA_N<2>	7 15
J443	EDP_90D	EDP	EDP_DATA_P<3>	7 15
J445	EDP_90D	EDP	EDP_DATA_N<3>	7 15
J447	EDP_90D	EDP	EDP_AUX_EMI_P	15
J446	EDP_90D	EDP	EDP_AUX_EMI_N	15
J449	EDP_90D	EDP	EDP_DATA_EMI_P<0>	15
J448	EDP_90D	EDP	EDP_DATA_EMI_N<0>	15
J450	EDP_90D	EDP	EDP_DATA_EMI_P<1>	15
J451	EDP_90D	EDP	EDP_DATA_EMI_N<1>	15
J453	EDP_90D	EDP	EDP_DATA_EMI_P<2>	15
J454	EDP_90D	EDP	EDP_DATA_EMI_N<2>	15
J452	EDP_90D	EDP	EDP_DATA_EMI_P<3>	15
J455	EDP_90D	EDP	EDP_DATA_EMI_N<3>	15
J457	EDP_90D	EDP	CONN_EDP_AUX_EMI_P	15
J456	EDP_90D	EDP	CONN_EDP_AUX_EMI_N	15
J458	EDP_90D	EDP	CONN_EDP_DATA_EMI_P<0>	15
J460	EDP_90D	EDP	CONN_EDP_DATA_EMI_N<0>	15
J459	EDP_90D	EDP	CONN_EDP_DATA_EMI_P<1>	15
J462	EDP_90D	EDP	CONN_EDP_DATA_EMI_N<1>	15
J461	EDP_90D	EDP	CONN_EDP_DATA_EMI_P<2>	15
J463	EDP_90D	EDP	CONN_EDP_DATA_EMI_N<2>	15
J464	EDP_90D	EDP	CONN_EDP_DATA_EMI_P<3>	15
J465	EDP_90D	EDP	CONN_EDP_DATA_EMI_N<3>	15

BACKLIGHT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LED	*	LED

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LEDA	*	*	3:1_SPACING
LEDB	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
J482	LED	LEDA	LED_IO1_A_R	30
J484	LED	LEDB	LED_IO1_B_R	30
J483	LED	LEDA	LED_IO2_A_R	30
J485	LED	LEDB	LED_IO2_B_R	30
J487	LED	LEDA	LED_IO3_A_R	30
J486	LED	LEDB	LED_IO3_B_R	30
J489	LED	LEDA	LED_IO4_A_R	30
J488	LED	LEDB	LED_IO4_B_R	30
J490	LED	LEDA	LED_IO5_A_R	30
J491	LED	LEDB	LED_IO5_B_R	30
J492	LED	LEDA	LED_IO6_A_R	30
J493	LED	LEDB	LED_IO6_B_R	30
J494	LED	LEDA	LED_IO_1_A	15 30
J495	LED	LEDB	LED_IO_1_B	15 30
J496	LED	LEDA	LED_IO_2_A	15 30
J497	LED	LEDB	LED_IO_2_B	15 30
J498	LED	LEDA	LED_IO_3_A	15 30
J499	LED	LEDB	LED_IO_3_B	15 30
J500	LED	LEDA	LED_IO_4_A	15 30
J501	LED	LEDB	LED_IO_4_B	15 30
J502	LED	LEDA	LED_IO_5_A	15 30
J503	LED	LEDB	LED_IO_5_B	15 30
J504	LED	LEDA	LED_IO_6_A	15 30
J505	LED	LEDB	LED_IO_6_B	15 30

TEMP SENSORS

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
BOARD_TEMP	*	TEMP_SENSE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BOARD_TEMP	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
J572		BOARD_TEMP	BOARD_TEMP1	30 32
J574		BOARD_TEMP	BOARD_TEMP2	30 32
J575	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP3_P	30
J577	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP3_N	30
J578	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP4_P	30
J576	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP4_N	30
J580	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP5_P	30
J581	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP5_N	30
J582	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP6_P	30
J583	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP6_N	30
J602	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP7_P	30
J603	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP7_N	30
J604	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP8_P	30
J605	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP8_N	30

SYNC_MASTER=MIKE SYNC_DATE=11/30/2011

PAGE TITLE
CONSTRAINTS: DISPLAY/AUDIO

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DDR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_50S	*	DDR_45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR	*	*	3:1_SPACING

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_90D	*	DDR_90_OHM_DIFF

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
I22A	DDR_50S	DDR	DDR0_CA<9..0> 8 11
I22B	DDR_50S	DDR	DDR0_DM<3..0> 8 11
I22C	DDR_90D	DDR	DDR0_CK_P 8 11
I22D	DDR_90D	DDR	DDR0_CK_N 8 11
I22E	DDR_50S	DDR	DDR0_CKE<1..0> 8 11
I22F	DDR_50S	DDR	DDR0_CSN<2..0> 8 11
I22G	DDR_50S	DDR	DDR0_ZQ 11
I23A	DDR_50S	DDR	DDR0_DQ<7..0> 8 11
I23B	DDR_90D	DDR	DDR0_DQS_P<0> 8 11
I23C	DDR_90D	DDR	DDR0_DQS_N<0> 8 11
I23D	DDR_50S	DDR	DDR0_DQ<15..8> 8 11
I23E	DDR_90D	DDR	DDR0_DQS_P<1> 8 11
I23F	DDR_90D	DDR	DDR0_DQS_N<1> 8 11
I23G	DDR_50S	DDR	DDR0_DQ<23..16> 8 11
I23H	DDR_90D	DDR	DDR0_DQS_P<2> 8 11
I23J	DDR_90D	DDR	DDR0_DQS_N<2> 8 11
I23K	DDR_50S	DDR	DDR0_DQ<31..24> 8 11
I23L	DDR_90D	DDR	DDR0_DQS_P<3> 8 11
I24A	DDR_90D	DDR	DDR0_DQS_N<3> 8 11
I20A	DDR_50S	DDR	DDR1_CA<9..0> 8 11
I20B	DDR_50S	DDR	DDR1_DM<3..0> 8 11
I20C	DDR_90D	DDR	DDR1_CK_P 8 11
I20D	DDR_90D	DDR	DDR1_CK_N 8 11
I20E	DDR_50S	DDR	DDR1_CKE<1..0> 8 11
I20F	DDR_50S	DDR	DDR1_CSN<2..0> 8 11
I20G	DDR_50S	DDR	DDR1_ZQ 11
I21A	DDR_50S	DDR	DDR1_DQ<7..0> 8 11
I21B	DDR_90D	DDR	DDR1_DQS_P<0> 8 11
I21C	DDR_90D	DDR	DDR1_DQS_N<0> 8 11
I21D	DDR_50S	DDR	DDR1_DQ<15..8> 8 11
I21E	DDR_90D	DDR	DDR1_DQS_P<1> 8 11
I21F	DDR_90D	DDR	DDR1_DQS_N<1> 8 11
I21G	DDR_50S	DDR	DDR1_DQ<23..16> 8 11
I21H	DDR_90D	DDR	DDR1_DQS_P<2> 8 11
I21J	DDR_90D	DDR	DDR1_DQS_N<2> 8 11
I21K	DDR_50S	DDR	DDR1_DQ<31..24> 8 11
I21L	DDR_90D	DDR	DDR1_DQS_P<3> 8 11
I22M	DDR_90D	DDR	DDR1_DQS_N<3> 8 11
I18A	DDR_50S	DDR	DDR2_CA<9..0> 8 12
I18B	DDR_50S	DDR	DDR2_DM<3..0> 8 12
I18C	DDR_90D	DDR	DDR2_CK_P 8 12
I18D	DDR_90D	DDR	DDR2_CK_N 8 12
I18E	DDR_50S	DDR	DDR2_CKE<1..0> 8 12
I18F	DDR_50S	DDR	DDR2_CSN<2..0> 8 12
I18G	DDR_50S	DDR	DDR2_ZQ 12
I19A	DDR_50S	DDR	DDR2_DQ<7..0> 8 12
I19B	DDR_90D	DDR	DDR2_DQS_P<0> 8 12
I19C	DDR_90D	DDR	DDR2_DQS_N<0> 8 12
I19D	DDR_50S	DDR	DDR2_DQ<15..8> 8 12
I19E	DDR_90D	DDR	DDR2_DQS_P<1> 8 12
I19F	DDR_90D	DDR	DDR2_DQS_N<1> 8 12
I19G	DDR_50S	DDR	DDR2_DQ<23..16> 8 12
I19H	DDR_90D	DDR	DDR2_DQS_P<2> 8 12
I19J	DDR_90D	DDR	DDR2_DQS_N<2> 8 12
I19K	DDR_50S	DDR	DDR2_DQ<31..24> 8 12
I19L	DDR_90D	DDR	DDR2_DQS_P<3> 8 12
I20M	DDR_90D	DDR	DDR2_DQS_N<3> 8 12
I16A	DDR_50S	DDR	DDR3_CA<9..0> 8 12
I16B	DDR_50S	DDR	DDR3_DM<3..0> 8 12
I16C	DDR_90D	DDR	DDR3_CK_P 8 12
I16D	DDR_90D	DDR	DDR3_CK_N 8 12
I16E	DDR_50S	DDR	DDR3_CKE<1..0> 8 12
I16F	DDR_50S	DDR	DDR3_CSN<2..0> 8 12
I16G	DDR_50S	DDR	DDR3_ZQ 12
I17A	DDR_50S	DDR	DDR3_DQ<7..0> 8 12
I17B	DDR_90D	DDR	DDR3_DQS_P<0> 8 12
I17C	DDR_90D	DDR	DDR3_DQS_N<0> 8 12
I17D	DDR_50S	DDR	DDR3_DQ<15..8> 8 12
I17E	DDR_90D	DDR	DDR3_DQS_P<1> 8 12
I17F	DDR_90D	DDR	DDR3_DQS_N<1> 8 12
I17G	DDR_50S	DDR	DDR3_DQ<23..16> 8 12
I17H	DDR_90D	DDR	DDR3_DQS_P<2> 8 12
I17J	DDR_90D	DDR	DDR3_DQS_N<2> 8 12
I17K	DDR_50S	DDR	DDR3_DQ<31..24> 8 12
I17L	DDR_90D	DDR	DDR3_DQS_P<3> 8 12
I18M	DDR_90D	DDR	DDR3_DQS_N<3> 8 12

NAND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
NAND_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
NAND0	*	*	2:1_SPACING
NAND1	*	*	2:1_SPACING

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
I68	NAND_50S	NAND0	FMI0_AD<0> 6 13
I69	NAND_50S	NAND0	FMI0_AD<1> 6 13
I70	NAND_50S	NAND0	FMI0_AD<2> 6 13
I71	NAND_50S	NAND0	FMI0_AD<3> 6 13
I72	NAND_50S	NAND0	FMI0_AD<4> 6 13
I73	NAND_50S	NAND0	FMI0_AD<5> 6 13
I74	NAND_50S	NAND0	FMI0_AD<6> 6 13
I75	NAND_50S	NAND0	FMI0_AD<7> 6 13
I76	NAND_50S	NAND0	FMI0_ALE 6 13
I77	NAND_50S	NAND0	FMI0_CE0_L 6 13
I78	NAND_50S	NAND0	TP_FMI0_CE1_L
I120	NAND_50S	NAND0	TP_FMI0_CE2_L
I121	NAND_50S	NAND0	TP_FMI0_CE3_L
I122	NAND_50S	NAND0	TP_FMI0_CE4_L
I123	NAND_50S	NAND0	TP_FMI0_CE5_L
I124	NAND_50S	NAND0	TP_FMI0_CE6_L
I125	NAND_50S	NAND0	TP_FMI0_CE7_L
I126	NAND_50S	NAND0	FMI0_CLE 6 13
I128	NAND_50S	NAND0	FMI0_DQS 6 13
I130	NAND_50S	NAND0	FMI0_RE_L 6 13
I131	NAND_50S	NAND0	FMI0_WE_L 6 13
I135	NAND_50S	NAND1	FMI1_AD<0> 6 13
I136	NAND_50S	NAND1	FMI1_AD<1> 6 13
I137	NAND_50S	NAND1	FMI1_AD<2> 6 13
I138	NAND_50S	NAND1	FMI1_AD<3> 6 13
I139	NAND_50S	NAND1	FMI1_AD<4> 6 13
I140	NAND_50S	NAND1	FMI1_AD<5> 6 13
I141	NAND_50S	NAND1	FMI1_AD<6> 6 13
I142	NAND_50S	NAND1	FMI1_AD<7> 6 13
I143	NAND_50S	NAND1	FMI1_ALE 6 13
I144	NAND_50S	NAND1	FMI1_CE0_L 6 13
I146	NAND_50S	NAND1	TP_FMI1_CE2_L
I148	NAND_50S	NAND1	TP_FMI1_CE4_L
I149	NAND_50S	NAND1	TP_FMI1_CE5_L
I150	NAND_50S	NAND1	TP_FMI1_CE6_L
I151	NAND_50S	NAND1	TP_FMI1_CE7_L
I152	NAND_50S	NAND1	FMI1_CLE 6 13
I154	NAND_50S	NAND1	FMI1_DQS 6 13
I156	NAND_50S	NAND1	FMI1_RE_L 6 13
I158	NAND_50S	NAND1	FMI1_WE_L 6 13

WIFI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
WIFI_50S	*	WIFI_50S
WIFI_PWR100	*	WIFI_PWR100
WIFI_PWR1000	*	WIFI_PWR1000

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
I240	WIFI_50S		50_WLAN_G 27
I246	WIFI_50S		50_WLAN_A 27
I247	WIFI_50S		50_WLAN_G_1 27
I248	WIFI_50S		50_WLAN_A_DIPLX 27
I249	WIFI_50S		50_WIFI_ANT_FD_2
I250	WIFI_50S		50_WIFI_ANT_FD_1
I251	WIFI_50S		50_WIFI_ANT_FD

DDR VREF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VREF	*	*	5:1_SPACING

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
I49D		PWR	PPVREF_DDR0_CA 11 39
I49V		PWR	PPVREF_DDR0_DQ 11 39
I49W		PWR	PPVREF_DDR1_CA 11 39
I49X		PWR	PPVREF_DDR1_DQ 11 39
I244		PWR	PPVREF_DDR2_CA 12 39
I245		PWR	PPVREF_DDR2_DQ 12 39
I243		PWR	PPVREF_DDR3_CA 12 39
I242		PWR	PPVREF_DDR3_DQ 12 39

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PWR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PP_PWR	*	PWR_PMU

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PWR	*	*	3:1_SPACING

	VOLTAGE	NET_TYPE PHYSICAL	NET_TYPE SPACING		
P22	1.1V	PP_PWR	PWR	BUCK0A_LX0	29
P1	1.1V	PP_PWR	PWR	BUCK0A_LX1	29
P2	1.1V	PP_PWR	PWR	BUCK0A_FB	29
P3	1.1V	PP_PWR	PWR	PP1V1_CPU0_FET	29 30
P4	1.1V	PP_PWR	PWR	BUCK0B_LX0	29
P5	1.1V	PP_PWR	PWR	BUCK0B_LX1	29
P6	1.1V	PP_PWR	PWR	BUCK0B_FB	29
P7	1.1V	PP_PWR	PWR	PP1V1_CPU1_FET	29 30
P8	1.1V	PP_PWR	PWR	BUCK0C_LX0	29
P9	1.1V	PP_PWR	PWR	BUCK0C_FB	29
P10	1.1V	PP_PWR	PWR	PP1V1_CPUB	29 34
P11	1.2V	PP_PWR	PWR	BUCK2_LX0	29
P12	1.2V	PP_PWR	PWR	BUCK2_LX1	29
P13	1.2V	PP_PWR	PWR	BUCK2_LX2	29
P15	1.2V	PP_PWR	PWR	BUCK2_FB	29
P14	1.2V	PP_PWR	PWR	PP1V2_SOC	29 34
P16	1.8V	PP_PWR	PWR	BUCK3_LX0	29
P17	1.8V	PP_PWR	PWR	BUCK3_FB	29
P18	1.8V	PP_PWR	PWR	PP1V8_S2R	29 34
P19	1.2V	PP_PWR	PWR	BUCK4_LX0	29
P20	1.2V	PP_PWR	PWR	BUCK4_FB	29
P21	1.2V	PP_PWR	PWR	PP1V2_S2R	29 34
P23	1.1V	PP_PWR	PWR	BUCK5_LX0	29
P24	1.1V	PP_PWR	PWR	BUCK5_FB	29
P25	3.3V	PP_PWR	PWR	PP3V3_OUT	29 34
P26	3.0V	PP_PWR	PWR	PP3V0_GRAPE	29 34
P27	1.7V	PP_PWR	PWR	PP1V7_VA_VCP	19 29 34
P28	3.0V	PP_PWR	PWR	PP3V2_S2R_USBMUX	29 34 39
P29	3.2V	PP_PWR	PWR	LDO5	29
P30	3.3V	PP_PWR	PWR	PP3V3_ACC	29 34
P31	3.0V	PP_PWR	PWR	PP3V0_S2R_HALL	29 34
P32	3.0V	PP_PWR	PWR	PP3V2_S2R_USBMUX	29 34 39
P33	3.0V	PP_PWR	PWR	PP3V0_IO	29 34
P34	3.0V	PP_PWR	PWR	PP3V0_SENSOR	29 34
P35	2.8V	PP_PWR	PWR	PP2V8_CAM	29 34
P36	1.0V	PP_PWR	PWR	PP1V0	29 34
P37	1.1V	PP_PWR	PWR	PP1V1_SRAM	29 34
P38	1.8V	PP_PWR	PWR	PP1V8_ALWAYS	29 34
P39	1.2V	PP_PWR	PWR	PP1V2	29 34
P40		PP_PWR	PWR	DSP_SW	
P41	1.8V	PP_PWR	PWR	PP1V8	29 32 34
P42	1.8V	PP_PWR	PWR	PP1V8_GRAPE	
P43	4.7V	PP_PWR	PWR	PPVCC_MAIN	15 25 29 30 34
P44	4.2V	PWR500	PWR	PPBATT_VCC	29 32 34
P45	6.0V	PP_PWR	PWR	PP6V0_LCM_HI	30
P46	6.0V	PP_PWR	PWR	LCM_LX	30
P47	6.0V	PP_PWR	PWR	PP6V0_LCM_VBOOST	30
P48	5.25V	PP_PWR	PWR	PP5V25_VLCM1	
P51	1.1V	PP_PWR	PWR	PP1V1_CPU0	30 34
P50	1.1V	PP_PWR	PWR	PP1V1_CPU1	30 34
P53	20.4V	PP_PWR	PWR	PPLED_OUT_A	30 34
P52	20.4V	PP_PWR	PWR	PPLED_OUT_B	30 34
P54	1.8V	PP_PWR	PWR	PP1V8_PL0_F	4
P55	1.0V	PP_PWR	PWR	PP1V0_MIPI_PLL_F	7
P56	1.8V	PP_PWR	PWR	PP1V8_EDP_AVDD_AUX	7
P57	1.8V	PP_PWR	PWR	PP1V8_DP_AVDD_AUX	
P58	3.3V	PP_PWR	PWR	PP3V3_S0_LCD_FERR	15
P59	3.3V	PP_PWR	PWR	PP3V3_LCDVDD_SW_F	15
P60	20.4V	PWR500	PWR	PPLED_BACK_REG_B	15
P61	20.4V	PP_PWR	PWR	PPLED_BACK_REG_A	15
P64	6V	PP_PWR	PWR	PPVBUS_USB_EMI	23 34
P67	0.6V	PP_PWR	PWR	PPVREF_DDR0_CA	11 38
P68	0.6V	PP_PWR	PWR	PPVREF_DDR0_DQ	11 38
P69	0.6V	PP_PWR	PWR	PPVREF_DDR1_CA	11 38
P70	0.6V	PP_PWR	PWR	PPVREF_DDR1_DQ	11 38
P73	0.6V	PP_PWR	PWR	PPVREF_DDR2_CA	12 38
P72	0.6V	PP_PWR	PWR	PPVREF_DDR2_DQ	12 38
P75	0.6V	PP_PWR	PWR	PPVREF_DDR3_CA	12 38
P74	0.6V	PP_PWR	PWR	PPVREF_DDR3_DQ	12 38
P76		PP_PWR	PWR	DAC_AP_VREF	7
P78	4.6V	PP_PWR	PWR	BATT_POS_RC	29
P1220	4.6V	PP_PWR	PWR	BATT_VCC_WLAN	27
P1222	1.8V	PP_PWR	PWR	PP_WLAN_VDDIO_1V8	27
P1229	3.55V	PP_PWR	PWR	LDO10	18 29

GND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GND	*	GND_PH

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
P199	VOLTAGE=0V	GND	GND	GND	
P198	VOLTAGE=0V	GND	GND	GND_AUDIO_CODEC	18
P193	VOLTAGE=0V	GND	GND	GND_SPKR_AMP1	
P197	VOLTAGE=0V	GND	GND	GND_SPKR_AMP2	
P217	VOLTAGE=0V	GND	GND	AGND_U3000	16
TP2200	VOLTAGE=0V	GND	GND	J2200_29_GND	15
TP2201	VOLTAGE=0V	GND	GND	J2200_36_GND	15
TP2202	VOLTAGE=0V	GND	GND	J2200_43_GND	15

RST

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
RST	*	*	4:1_SPACING

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
P165			RST	BB_TRST_L	
P166			RST	DBG_RST	
P167			RST	DEBUG_RST_L	
P171			RST	GSM_TXBURST_IND	
P140			RST	JTAG_AP_TRST_L	4 10 36
P170			RST	RST_AP_1V8_L	
P168			RST	RST_AP_L	4 25 26 30
P172			RST	GPIO_BB_RST_L	5 26
P174			RST	RST_BB_PMU_L	
P173			RST	RST_BT_L	
P176			RST	RST_DET_L	
P156			GRAPE	RST_GRAPE_L	
P177			RST	RST_L63_L	
P178			RST	RST_PMU_IN	
P179			RST	RST_WLAN_L	
P181			RST	SIMCRD_RST	
P187			RST	UD881_RST	
P191			RST	UD882_RST	

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