1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2012-02-23

J11 MLB PIB SCHEMATIC
2.7.0
03/25/12

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9276	1	SCHEM,MLB,J11	SCH	CRITICAL	
820-3208	1	PCBF,MLB,J11	PCB	CRITICAL	

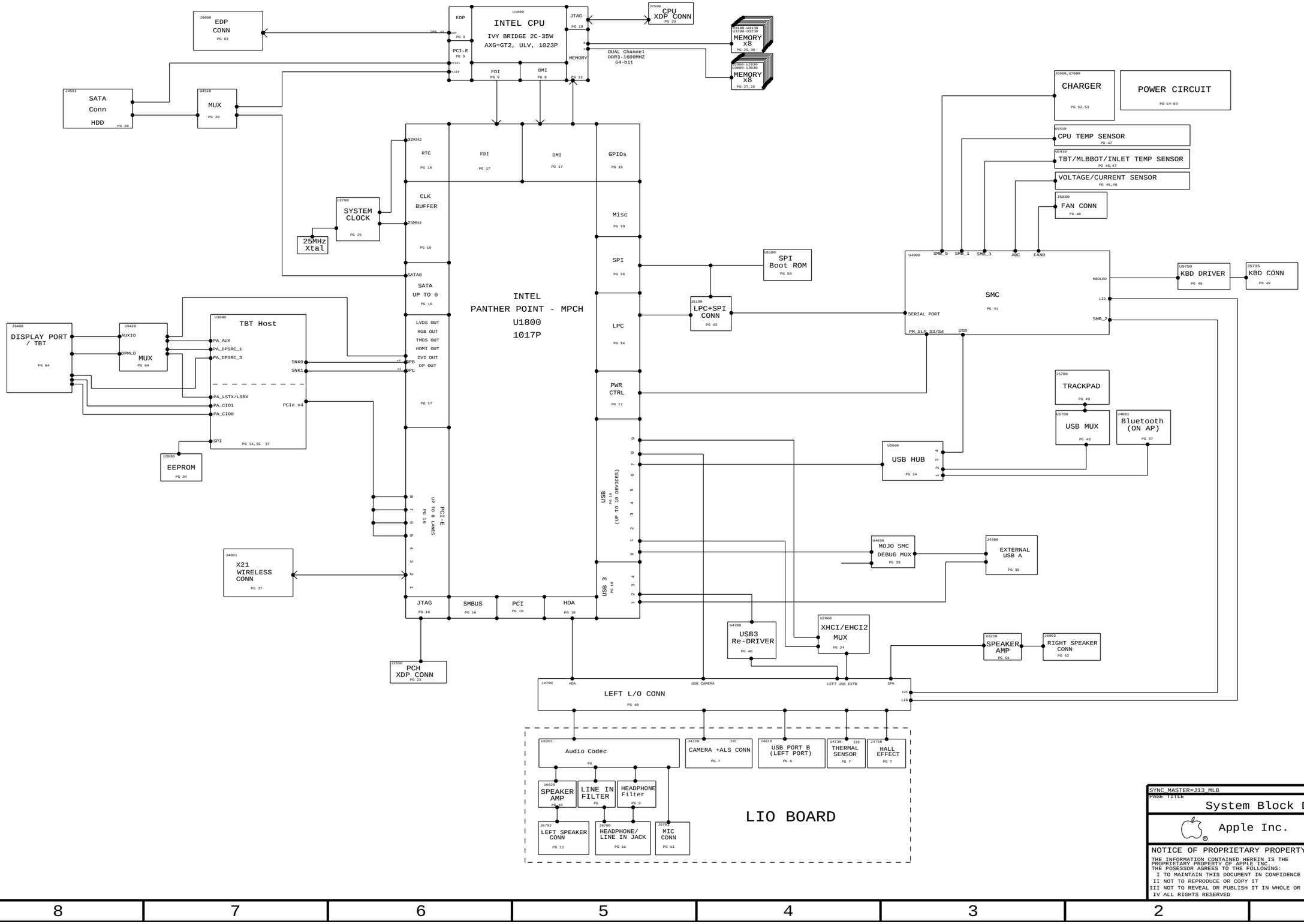
DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Thu Feb 23 12:05:40 2012

PRODUCT SAFETY REQUIREMENTS:
PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.
PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

DRAWING TITLE: SCHEM,MLB,J11

Apple Inc.

DRAWING NUMBER: 051-9276 | SIZE: D
REVISION: 2.7.0
BRANCH:
PAGE: 1 OF 109
SHEET: 1 OF 72



SYNC MASTER=J13 MLB
SYNC DATE=11/18/2013

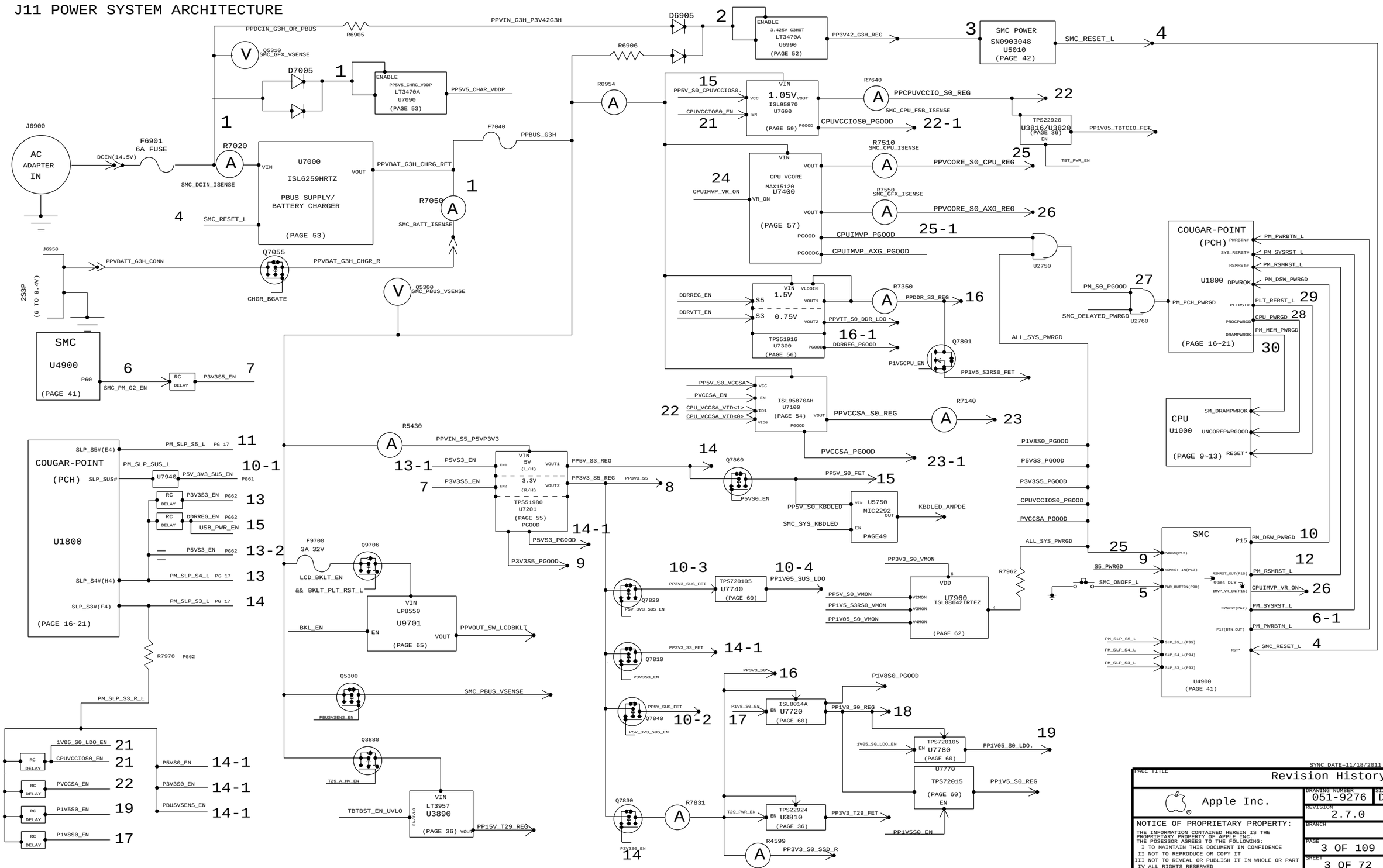
PAGE TITLE

System Block Diagram

Apple Inc.

DRAWING NUMBER 051-9276
SIZE D
REVISION 2.7.0
BRANCH
PAGE 2 OF 109
SHEET 2 OF 72

J11 POWER SYSTEM ARCHITECTURE



PAGE TITLE	Revision History					SYNC_DATE=11/18/2011	
Apple Inc.		DRAWING NUMBER	051-9276	SIZE	D		
		REVISION	2.7.0				
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		BRANCH					
		PAGE	3 OF 109				
		SHEET	3 OF 72				

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-3469	PCBA,MLB,1.5GHZ,HY 4GB,J11	J11_CMNPTS,CPU:1.5GHZ,EEEE:DYKL,DDR3:HYNIX_4GB
639-3470	PCBA,MLB,1.5GHZ,SA 4GB,J11	J11_CMNPTS,CPU:1.5GHZ,EEEE:DYKH,DDR3:SAMSUNG_4GB
639-3473	PCBA,MLB,1.5GHZ,HY 8GB,J11	J11_CMNPTS,CPU:1.5GHZ,EEEE:DYKJ,DDR3:HYNIX_8GB
639-3659	PCBA,MLB,1.5GHZ,EL 8GB,J11	J11_CMNPTS,CPU:1.5GHZ,EEEE:F0V3,DDR3:ELPIDA_8GB
639-3471	PCBA,MLB,1.7GHZ,HY 4GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:DYKK,DDR3:HYNIX_4GB
639-3472	PCBA,MLB,1.7GHZ,SA 4GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:DYKF,DDR3:SAMSUNG_4GB
639-3775	PCBA,MLB,1.7GHZ,EL 4GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:F27J,DDR3:ELPIDA_4GB
639-3474	PCBA,MLB,1.7GHZ,HY 8GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:DYKG,DDR3:HYNIX_8GB
639-3774	PCBA,MLB,1.7GHZ,SA 8GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:F27D,DDR3:SAMSUNG_8GB
639-3660	PCBA,MLB,1.7GHZ,EL 8GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:F0V4,DDR3:ELPIDA_8GB
639-3776	PCBA,MLB,2.0GHZ,HY 4GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F27K,DDR3:HYNIX_4GB
639-3778	PCBA,MLB,2.0GHZ,SA 4GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F27G,DDR3:SAMSUNG_4GB
639-3780	PCBA,MLB,2.0GHZ,EL 4GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F27H,DDR3:ELPIDA_4GB
639-3777	PCBA,MLB,2.0GHZ,HY 8GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F27C,DDR3:HYNIX_8GB
639-3779	PCBA,MLB,2.0GHZ,SA 8GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F27F,DDR3:SAMSUNG_8GB
639-3781	PCBA,MLB,2.0GHZ,EL 8GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F279,DDR3:ELPIDA_8GB
085-3937	J11 MLB DEVELOPMENT BOM	J11_DEVEL:ENG
607-9089	CMN PTS,PCBA,MLB,J11	J11_COMMON
939-0479	PCBA,MLB,1.9GHZ,HY 4GB,J11	J11_CMNPTS,CPU:1.9GHZ,EEEE:DYKL,DDR3:HYNIX_4GB

Bar Code Labels / EEEE #’s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKL]	CRITICAL	EEEE:DYKL
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKH]	CRITICAL	EEEE:DYKH
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKK]	CRITICAL	EEEE:DYKK
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKF]	CRITICAL	EEEE:DYKF
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKJ]	CRITICAL	EEEE:DYKJ
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKG]	CRITICAL	EEEE:DYKG
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F0V3]	CRITICAL	EEEE:F0V3
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F0V4]	CRITICAL	EEEE:F0V4
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F279]	CRITICAL	EEEE:F279
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27C]	CRITICAL	EEEE:F27C
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27D]	CRITICAL	EEEE:F27D
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27F]	CRITICAL	EEEE:F27F
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27G]	CRITICAL	EEEE:F27G
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27H]	CRITICAL	EEEE:F27H
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27J]	CRITICAL	EEEE:F27J
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27K]	CRITICAL	EEEE:F27K

Sub-BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-3937	1	J11 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
607-9089	1	CMN PTS,PCBA,MLB,J11	CMNPTS	CRITICAL	J11_CMNPTS

SYNC_MASTER=K21_MLB SYNC_DATE=11/16/2010

PAGE TITLE

K78 BOM Variants

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D

REVISION 2.7.0

BRANCH

PAGE 4 OF 109

SHEET 4 OF 72

J11 BOM GROUPS

BOM GROUP	BOM OPTIONS
J11_COMMON	ALTERNATE,COMMON,J11_MISC,J11_DEBUG:ENG,J11_PROGPARTS,USBHUB2513B,EDP:YES,PCH_C1
J11_MISC	HUB_3NONREM,TBT,MPM5:YES,CPUMEM_SLG:NO,P5V5_DCIN:NO,TPAD_PCH:NO,SKIP_5V3V3:INAUDIBLE,BTPWR:S4,TBTHV:P15V,LVDDR3_HW:YES,AXG_ACOUSTICS:NO
J11_PROGPARTS	BOOTROM_PROG,SMC_PROG,TBTROM:PROG
J11_DEVEL:ENG	ALTERNATE,BKLT:ENG,XDP_CONN,XDP_PCH,DDRVREF_DAC,VREFDQ:M1_M3,VREFCA:LDO_DAC,S0PGOOD_ISL,S3_S0_LED,VCCIOISNS_ENG,AIRPORTISNS_ENG,HDDISNS_ENG,LCDBKLTISNS_ENG
J11_DEVEL:PVT	XDP_CONN
J11_DEBUG:ENG	DEVEL_BOM,MOJO:YES,XDP,XDP_CPU:BPM,LPCPLUS
J11_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,MOJO:YES,XDP,LPCPLUS,VREFDQ:LDO,VREFCA:LDO,XDP_CPU:BPM,VCCIOISNS_PROD,AIRPORTISNS_PROD,HDDISNS_PROD,LCDBKLTISNS_PROD
J11_DEBUG:PROD	BKLT:PROD,MOJO:YES,XDP,LPCPLUS,VREFDQ:LDO,VREFCA:LDO,XDP_CPU:BPM,VCCIOISNS_PROD,AIRPORTISNS_PROD,HDDISNS_PROD,LCDBKLTISNS_PROD
DDR3:HYNIX_4GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:HYNIX_8GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:HYNIX_8GB
DDR3:SAMSUNG_4GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:SAMSUNG_8GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:SAMSUNG_8GB
DDR3:ELPIDA_4GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:ELPIDA_4GB
DDR3:ELPIDA_8GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:ELPIDA_8GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0865	1	EEPROM,256KBIT,SPI,5MHZ,1.8V,2X3QFN	U3690	CRITICAL	TBTROM:BLANK
341S3526	1	IC,EEPROM,Cactus Ridge (V1.2) PIB, J11/J13	U3690	CRITICAL	TBTROM:PROG
338S1098	1	IC,SMC12-A3,40MHZ/50DMIPS MCU,9X9,157BGA	U4900	CRITICAL	SMC_BLANK
341S3434	1	IC,SMC,PIB,J11	U4900	CRITICAL	SMC_PROG
335S0809	1	64 MBIT SPI SERIAL DUAL I/O FLASH,8X6X0.8	U6100	CRITICAL	BOOTROM_BLANK
335S0803	1	64 MBIT SPI SERIAL DUAL I/O FLASH,8X6X0.8	U6100	CRITICAL	BOOTROM_BLANK
341S3527	1	IC,EFI ROM,PIB,J11/J13	U6100	CRITICAL	BOOTROM_PROG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0855	376S0613		ALL	Diodes alt to Toshiba
376S0977	376S0859		ALL	Diodes alt to Toshiba
376S0972	376S0612		ALL	Rohm alt to Toshiba
138S0676	138S0691		ALL	Murata alt to Samsung
371S0709	371S0652		ALL	NXP alt to NXP
138S0671	138S0673		ALL	Taiyo alt to Murata
152S1085	152S1307		ALL	Toko alt to Cyntec
152S1462	152S1295		ALL	Toko alt to NEC inductor
138S0684	138S0660		ALL	Murata alt to Taiyo Yuden
138S0703	138S0648		ALL	Murata alt to Taiyo Yuden
152S1493	152S1300		ALL	Coilcraft MA5274 alt to Murata
152S0586	152S1301		ALL	Dale/Vishay alt to Cyntec
353S3238	353S1428		ALL	Intersil alt to OPA2333
372S0186	372S0185		ALL	NXP alt to Diodes
197S0431	197S0432		ALL	200uW Epson alt to NDK
376S1053	376S0604		ALL	Diodes alt to Fairchild
376S0855	376S0613		ALL	Diodes alt to Toshiba
376S0903	376S0796		ALL	Fairchild alt to Siliconix
371S0713	371S0558		ALL	Diodes alt to ST Micro
128S0333	998-4435		ALL	Sanyo alt to Kemet
128S0357	998-4435		ALL	Sanyo High Voltage Polymer alt
998-4715	998-4435		ALL	Kemet Rectangular Design alt
998-4716	998-4435		ALL	Kemet Flute Design alt

DRAM CFG CHART

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 2
4GB	0
8GB	1

DIE REV	CFG 3
A	0
B	1

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4197	1	IVB,QBP8,ES2,K0,1.5,17W,2+2,0.95,4M,ULVB	U1000	CRITICAL	CPU:1.5GHZ
337S4299	1	IVB,QC9E,QS,L1,1.7,17W,2+2,1.05,3M,ULVBG	U1000	CRITICAL	CPU:1.7GHZ
337S4296	1	IVB,QC9B,QS,L1,2.0,17W,2+2,1.15,4M,ULVBG	U1000	CRITICAL	CPU:2.0GHZ
337S4198	1	IVB,QBTP,ES2,K0,1.5,17W,2+2,0.95,4M,ULVBGA	U1000	CRITICAL	CPU:1.5GHZTDP
337S4299	1	IVB,QC9E,QS,L1,1.7,17W,2+2,1.05,3M,ULVBG	U1000	CRITICAL	CPU:1.7GHZTDP
337S4296	1	IVB,QC9B,QS,L1,2.0,17W,2+2,1.15,4M,ULVBG	U1000	CRITICAL	CPU:2.0GHZTDP
337S4297	1	IVB,QC9C,QS,L1,1.9,17W,2+2,1.15,4M,ULVBG	U1000	CRITICAL	CPU:1.9GHZ
337S4165	1	IC,PCH,PPT-MB,SFF,ES1	U1800	CRITICAL	PCH_ES1
337S4180	1	IC,PCH,PPT-MB,SFF,ES2,B0	U1800	CRITICAL	PCH_ES2
337S4235	1	IC,PCH,PPT-MB,SFF,P-QS,C0	U1800	CRITICAL	PCH_C0
337S4275	1	IC,PCH,PPT-MB,QS77,C1,QS	U1800	CRITICAL	PCH_C1
337S4275	1	IC,PCH,PPT-MB,QS77,C1,QS	U1800	CRITICAL	PCH_C1TDP
338S1108	1	IC,TBT,CR-4C,LP,ES3,288 FCBGA,12X12MM	U3600	CRITICAL	TBT
333S0622	4	IC,SDRAM,2GBIT,DDR3L-1600,GEMMA,78P FPGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0622	4	IC,SDRAM,2GBIT,DDR3L-1600,GEMMA,78P FPGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0622	4	IC,SDRAM,2GBIT,DDR3L-1600,GEMMA,78P FPGA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0622	4	IC,SDRAM,2GBIT,DDR3L-1600,GEMMA,78P FPGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0625	4	IC,SDRAM,4GBIT,512MX8,DDR3-1600,82 FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0625	4	IC,SDRAM,4GBIT,512MX8,DDR3-1600,82 FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0625	4	IC,SDRAM,4GBIT,512MX8,DDR3-1600,82 FGBA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0625	4	IC,SDRAM,4GBIT,512MX8,DDR3-1600,82 FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0623	4	IC,SDRAM,2GBIT,DDR3-1600,D35,78P FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0623	4	IC,SDRAM,2GBIT,DDR3-1600,D35,78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0623	4	IC,SDRAM,2GBIT,DDR3-1600,D35,78P FGBA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0623	4	IC,SDRAM,2GBIT,DDR3-1600,D35,78P FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0642	4	IC,SDRAM,4GBIT,DDR3-1600,C-DIE,78P FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0642	4	IC,SDRAM,4GBIT,DDR3-1600,C-DIE,78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0642	4	IC,SDRAM,4GBIT,DDR3-1600,C-DIE,78P FGBA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0642	4	IC,SDRAM,4GBIT,DDR3-1600,C-DIE,78P FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D,78P FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D,78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D,78P FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D,78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D,78P FBGA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D,78P FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0629	4	IC,SDRAM,4GBIT,DDR3L-1600,REV B,78P FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0629	4	IC,SDRAM,4GBIT,DDR3L-1600,REV B,78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0629	4	IC,SDRAM,4GBIT,DDR3L-1600,REV B,78P FBGA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0629	4	IC,SDRAM,4GBIT,DDR3L-1600,REV B,78P FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_8GB

607-6811	1	ASSEMBLY,SUBASSY,PCBA,HALL EFFECT,K99	J6955	CRITICAL	
353S2929	1	IC,ISL6259,BATCHARGER,3%,4C4MM,QFN28	U7000	CRITICAL	
946-3116	1	MLB,DYMAX UV EB 0.22 GRAM,K78	GLUE	CRITICAL	

PD Module Parts

806-3706	1	CAN,TOPSIDE,COVER,ALT,J11/J13	TBTTOPSIDE_2P_COVER	CRITICAL	
806-3705	1	CAN,TOPSIDE,FENCE,ALT,J11/J13	TBTTOPSIDE_2P_FENCE	CRITICAL	
806-3214	1	CAN,TOPSIDE,J11/J13	TBTTOPSIDE_1P	CRITICAL	
806-3216	1	CAN,MDP,J11/J13	MDPCAN	CRITICAL	
806-3083	1	SHLD,USB,MLB,J11/J13	USBCAN	CRITICAL	
806-3142	1	CAN,TBT,J11/J13	TBTFENCE	CRITICAL	
806-3215	1	CAN,COVER,TBT,J11/J13	TBTCOVER	CRITICAL	

SYNC_MASTER=J11_MLB_NON_POR SYNC_DATE=11/09/2011

PAGE TITLE

BOM Configuration

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D

REVISION 2.7.0

BRANCH

PAGE 5 OF 109

SHEET 5 OF 72

Functional Test Points

J4001: AirPort / BT Connector

FUNC_TEST

TRUE	PP3V3_WLAN_F (Need 6 TPs)	36 41
TRUE	WIFI_EVENT_L	36 40 41
TRUE	PCIE_AP_R2D_N	36 68
TRUE	PCIE_AP_R2D_P	36 68
TRUE	PCIE_CLK100M_AP_N	16 36 68
TRUE	PCIE_CLK100M_AP_P	16 36 68
TRUE	USB_BT_CONN_P	36 67
TRUE	USB_BT_CONN_N	36 67
TRUE	PCIE_AP_D2R_P	16 36 68
TRUE	PCIE_AP_D2R_N	16 36 68
TRUE	PCIE_WAKE_L	17 36
TRUE	AP_RESET_CONN_L	36
TRUE	AP_CLKREQ_O_L	36
TRUE	PP3V3_S3RS4_BT_F	36

(Need to add 8 GND TPs)

J4501: SATA SSD Connector

FUNC_TEST

TRUE	PP3V3_S0_SSD_FLT (Need 5 TPs)	37
TRUE	SATA_SSD_D2R_P	37 67
TRUE	SATA_SSD_D2R_N	37 67
TRUE	SATA_SSD_R2D_N	37 67
TRUE	SATA_SSD_R2D_P	37 67
TRUE	SMC_OOB1_RX_L	37 40
TRUE	SMC_OOB1_TX_L	37 40 41
TRUE	PCIE_SSD_D2R_N<1>	8 37 65
TRUE	PCIE_SSD_D2R_P<1>	8 37 65
TRUE	PCIE_SSD_R2D_N<1>	37 65
TRUE	PCIE_SSD_R2D_P<1>	37 65
TRUE	PCIE_CLK100M_SSD_N	16 37 65
TRUE	PCIE_CLK100M_SSD_P	16 37 65
TRUE	SSD_CLKREQ_L	16 37
TRUE	SSD_RESET_L	25 37
TRUE	SATA_PCIE_SEL	37
TRUE	SSD_P3V3S0_EN	37

(Need to add 6 GND TPs)

J4700: LIO Connector

FUNC_TEST

TRUE	=PP3V42_G3H_ONEWIRE	7 39
TRUE	=PP3V3_S0_AUDIO	7 39
TRUE	=PP3V3R1V5_S0_AUDIO	7 39
TRUE	SYS_ONEWIRE	39 40
TRUE	SMC_BC_ACOK	39 40 41
TRUE	=USB_PWR_EN	38 39 61
TRUE	=I2C_LIO_SDA	39 43
TRUE	=I2C_LIO_SCL	39 43
TRUE	=I2C_MIKEY_SCL	39 43
TRUE	=I2C_MIKEY_SDA	39 43
TRUE	AUD_IPHS_SWITCH_EN	25 39
TRUE	AUD_IP_PERIPHERAL_DET	18 39
TRUE	AUD_I2C_INT_L	18 39
TRUE	AUD_GPIO_3	39 50
TRUE	SPKRAMP_INR_N	39 50 71
TRUE	SPKRAMP_INR_P	39 50 71
TRUE	USB_EXTB_N	24 39 67
TRUE	USB_EXTB_P	24 39 67
TRUE	USB_CAMERA_N	18 39 67
TRUE	USB_CAMERA_P	18 39 67
TRUE	HDA_SDOUT	16 39 68
TRUE	HDA_BIT_CLK	16 39 68
TRUE	HDA_SDIN0	16 39 68
TRUE	USB_EXTB_OC_L	23 39
TRUE	HDA_RST_L	16 39 68
TRUE	HDA_SYNC	16 39 68
TRUE	USB3_EXTB_RX_RC_N	39 67
TRUE	USB3_EXTB_RX_RC_P	39 67
TRUE	USB3_EXTB_TX_C_P	39 67
TRUE	USB3_EXTB_TX_C_N	39 67

(Need to add 5 GND TPs)

J5100: LPC+SPI Connector

FUNC_TEST

TRUE	=PP3V3_S5_LPCPLUS	7 42
TRUE	=PP5V_S0_LPCPLUS	7 42
TRUE	LPC_AD<3..0>	16 40 42 68
TRUE	SPI_ALT_MOSI	42
TRUE	SPI_ALT_MISO	42
TRUE	LPC_FRAME_L	16 40 42 68
TRUE	PM_CLKRUN_L	17 40 42
TRUE	SMC_TMS	40 41 42
TRUE	LPCPLUS_RESET_L	25 42 68
TRUE	SMC_TDO	40 41 42
TRUE	TP_SMC_TRST_L	42
TRUE	TP_SMC_MD1	42
TRUE	SMC_TX_L	40 41 42
TRUE	LPC_CLK33M_LPCPLUS	25 42 68
TRUE	SPIROM_USE_MLB	19 42 49
TRUE	SPI_ALT_CLK	42
TRUE	SPI_ALT_CS_L	42
TRUE	LPC_SERIRQ	16 40 42
TRUE	LPC_PWRDWN_L	17 25 40 42
TRUE	SMC_TDI	40 41 42
TRUE	SMC_TCK	40 41 42
TRUE	SMC_RESET_L	40 41 42 52
TRUE	SMC_ROMBOOT	41 42
TRUE	SMC_RX_L	40 41 42
TRUE	LPCPLUS_GPIO	19 42

(Need to add 6 GND TPs)

J5600: Fan Connector

FUNC_TEST

TRUE	=PP5V_S0_FAN	7 47
TRUE	FAN_RT_TACH	47
TRUE	FAN_RT_PWM	47

(Need to add 1 GND TP)

J5700: IPD Flex Connector

FUNC_TEST

TRUE	SMC_PME_S4_WAKE_L	40 41 48
TRUE	PP5V_TPAD_FILT	48
TRUE	=PP3V42_G3H_TPAD	7 48
TRUE	PP3V3_TPAD_CONN	48
TRUE	USB_TPAD_P	48 67
TRUE	USB_TPAD_N	48 67
TRUE	=I2C_TPAD_SDA	43 48
TRUE	=I2C_TPAD_SCL	43 48
TRUE	SMC_ONOFF_L	40 41 48
TRUE	SMC_LID	40 41 48 51
TRUE	SMC_TPAD_RST_L	41 48

(Need to add 5 GND TPs)

J6900: DC-In Connector

FUNC_TEST

TRUE	=PP18V5_DCIN_CONN	7 51 (Need 4 TPs)
TRUE	=PP5V_S3_LIO_CONN	7 51 (Need 3 TPs)

(Need to add 5 GND TPs)

J6903: Speaker Connector

FUNC_TEST

TRUE	SPKRAMP_ROUT_P	50 51 71
TRUE	SPKRAMP_ROUT_N	50 51 71

(Need to add 3 GND TPs)

J6950: Battery Connector

FUNC_TEST

TRUE	PPVBAT_G3H_CONN	51 52 (Need 4 TPs)
TRUE	=SMBUS_BATT_SCL	43 51
TRUE	=SMBUS_BATT_SDA	43 51
TRUE	SYS_DETECT_L	51

(Need to add 4 GND TPs near J6950 and 1 for shield)

J9000: Internal DP Connector

FUNC_TEST

TRUE	PPVOUT_SW_LCDBKLT	62 64 (Need 2 TPs)
TRUE	PP3V3_SW_LCD	62 (Need 2 TPs)
TRUE	I2C_TCON_SDA_R	62
TRUE	LED_RETURN_6	62 64
TRUE	LED_RETURN_5	62 64
TRUE	LED_RETURN_4	62 64
TRUE	LED_RETURN_3	62 64
TRUE	LED_RETURN_2	62 64
TRUE	LED_RETURN_1	62 64
TRUE	DP_INT_HPD_CONN	62
TRUE	DP_INT_AUX_CH_C_N	62 65
TRUE	DP_INT_AUX_CH_C_P	62 65
TRUE	DP_INT_ML_F_P<0>	62 65
TRUE	DP_INT_ML_F_N<0>	62 65
TRUE	I2C_TCON_SCL_R	62

(Need to add 5 GND TPs)

J5715: KB BKLT Connector

FUNC_TEST

TRUE	KBDLED_FB	48
TRUE	KBDLED_ANODE	48

(Need to add 2 GND TPs)

J6955: HALL EFFECT Connector

FUNC_TEST

TRUE	SMC_LID_R	51
TRUE	=PP3V42_G3H_HALL	7 51

Misc Voltages & Control Signals

FUNC_TEST

TRUE	PPBUS_G3H	7 51
TRUE	PPVIN_SW_TBTBST	7 35
TRUE	PPBUS_S5_HS_COMPUTING_ISNS	7
TRUE	PPDCIN_G3H	7
TRUE	PP3V42_G3H	7
TRUE	PPVRTC_G3H	7
TRUE	PP5V_S5	7
TRUE	PP5V_SUS	7
TRUE	PP3V3_S5	7 71
TRUE	PP3V3_SUS	7
TRUE	PP3V3_S3	7
TRUE	PP1V8_S0	7
TRUE	PP3V3_S0	7 71
TRUE	PP1V5_S3	7 66
TRUE	PP1V5_S3RS0	7 66
TRUE	PP1V5_S0	7
TRUE	PP1V05_S0	7
TRUE	PPVTTDDR_S3	7
TRUE	PP0V75_S0_DDRVTT	7
TRUE	PPVCCSA_S0_CPU	7
TRUE	PP1V05_SUS	7
TRUE	PP15V_TBT	7
TRUE	PP3V3_TBTLC	7 (Need to add 27 GND TPs)
TRUE	PP1V05_TBTLC	7 35
TRUE	PP1V05_S0_PCH_VCCADPLL	7
TRUE	PPVCORE_S0_CPU	7
TRUE	PPVCORE_S0_AXG	7
TRUE	PP1V5_S3_CPU_VCCDQ	7
TRUE	PP1V05_S0_CPU_VCCPQE	7
TRUE	PP1V8_S0_CPU_VCCPLL_R	7
TRUE	PP1V05_TBTCIO	7
TRUE	PPBUS_S5_HS_OTHER_ISNS	7
TRUE	PPDCIN_G3H_ISOL	7
TRUE	PP5V_S3	7
TRUE	PP5V_S0	7
TRUE	PP3V3_S4	7

NC_EDP_TXP<0..3> MAKE_BASE=TRUE	TRUE	TP_EDP_TX_P<0..3>	9
NC_EDP_TXN<0..3> MAKE_BASE=TRUE	TRUE	TP_EDP_TX_N<0..3>	9
NC_EDP_AUXP MAKE_BASE=TRUE	TRUE	TP_EDP_AUX_P	
NC_EDP_AUXN MAKE_BASE=TRUE	TRUE	TP_EDP_AUX_N	
NC_CPU_THERMDA MAKE_BASE=TRUE	TRUE	TP_CPU_THERMDA	
NC_CPU_THERMDC MAKE_BASE=TRUE	TRUE	TP_CPU_THERMDC	
NC_CPU_RSVD<30..45> MAKE_BASE=TRUE	TRUE	TP_CPU_RSVD<30..45>	
NC_CPU_RSVD<8..27> MAKE_BASE=TRUE	TRUE	TP_CPU_RSVD<8..27>	
NC_PEG_R2D_CP<15..2> MAKE_BASE=TRUE	TRUE	=PEG_R2D_C_P<15..2>	9
NC_PEG_R2D_CN<15..2> MAKE_BASE=TRUE	TRUE	=PEG_R2D_C_N<15..2>	9
NC_PEG_D2RP<15..2> MAKE_BASE=TRUE	TRUE	=PEG_D2R_P<15..2>	9
NC_PEG_D2RN<15..2> MAKE_BASE=TRUE	TRUE	=PEG_D2R_N<15..2>	9

NO_TEST Nets

POWER SIGNALS

1643	TRUE VCCSAS0_SREF	53
1642	TRUE VCCSAS0_SET1_R	53
1641	TRUE VCCSAS0_SET0	53
1644	TRUE VCCSAS0_SET1	53

NO_TEST

17 TP_CRT_IG_BLUE	TRUE MAKE_BASE=TRUE	NC_CRT_IG_BLUE	
17 TP_CRT_IG_GREEN	TRUE MAKE_BASE=TRUE	NC_CRT_IG_GREEN	
17 TP_CRT_IG_RED	TRUE MAKE_BASE=TRUE	NC_CRT_IG_RED	
17 TP_CRT_IG_DDC_CLK	TRUE MAKE_BASE=TRUE	NC_CRT_IG_DDC_CLK	
17 TP_CRT_IG_DDC_DATA	TRUE MAKE_BASE=TRUE	NC_CRT_IG_DDC_DATA	
17 TP_CRT_IG_HSYNC	TRUE MAKE_BASE=TRUE	NC_CRT_IG_HSYNC	
17 TP_CRT_IG_VSYNC	TRUE MAKE_BASE=TRUE	NC_CRT_IG_VSYNC	
TP_LVDS_IG_CTRL_CLK	TRUE MAKE_BASE=TRUE	NC_LVDS_IG_CTRL_CLK	
TP_LVDS_IG_CTRL_DATA	TRUE MAKE_BASE=TRUE	NC_LVDS_IG_CTRL_DATA	
TP_PCH_LVDS_VBG	TRUE MAKE_BASE=TRUE	NC_PCH_LVDS_VBG	
16 TP_HDA_SDIN1	TRUE MAKE_BASE=TRUE	NC_HDA_SDIN1	
16 TP_HDA_SDIN2	TRUE MAKE_BASE=TRUE	NC_HDA_SDIN2	
16 TP_HDA_SDIN3	TRUE MAKE_BASE=TRUE	NC_HDA_SDIN3	
18 TP_PCI_PME_L	TRUE MAKE_BASE=TRUE	NC_PCI_PME_L	
18 TP_PCI_CLK33M_OUT3	TRUE MAKE_BASE=TRUE	NC_PCI_CLK33M_OUT3	
16 TP_CLINK_CLK	TRUE MAKE_BASE=TRUE	NC_CLINK_CLK	
16 TP_CLINK_DATA	TRUE MAKE_BASE=TRUE	NC_CLINK_DATA	
16 TP_CLINK_RESET_L	TRUE MAKE_BASE=TRUE	NC_CLINK_RESET_L	
16 TP_PCIE_CLK100M_PEBN	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEBN	
16 TP_PCIE_CLK100M_PEBP	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEBP	
17 TP_SDVO_TVCLKINN	TRUE MAKE_BASE=TRUE	NC_SDVO_TVCLKINN	
17 TP_SDVO_TVCLKINP	TRUE MAKE_BASE=TRUE	NC_SDVO_TVCLKINP	
17 TP_SDVO_STALLN	TRUE MAKE_BASE=TRUE	NC_SDVO_STALLN	
17 TP_SDVO_STALLP	TRUE MAKE_BASE=TRUE	NC_SDVO_STALLP	
17 TP_SDVO_INTN	TRUE MAKE_BASE=TRUE	NC_SDVO_INTN	
17 TP_SDVO_INTP	TRUE MAKE_BASE=TRUE	NC_SDVO_INTP	
23 TP_XDP_PCH_OBSFN_A<0..1>	TRUE MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_A<0..1>	
23 TP_XDP_PCH_OBSFN_B<0..1>	TRUE MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_B<0..1>	
23 TP_XDPPCH_HOOK2	TRUE MAKE_BASE=TRUE	NC_TP_XDPPCH_HOOK2	
23 TP_XDPPCH_HOOK3	TRUE MAKE_BASE=TRUE	NC_TP_XDPPCH_HOOK3	
23 TP_XDP_PCH_OBSFN_D<0..1>	TRUE MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_D<0..1>	
23 TP_XDP_PCH_HOOK4	TRUE MAKE_BASE=TRUE	NC_TP_XDP_PCH_HOOK4	
23 TP_XDP_PCH_HOOK5	TRUE MAKE_BASE=TRUE	NC_TP_XDP_PCH_HOOK5	
16 TP_PCH_GPIO64_CLKOUTFLEX0	TRUE MAKE_BASE=TRUE	NC_PCH_GPIO64_CLKOUTFLEX0	
16 TP_PCH_GPIO65_CLKOUTFLEX1	TRUE MAKE_BASE=TRUE	NC_PCH_GPIO65_CLKOUTFLEX1	
16 TP_PCH_GPIO66_CLKOUTFLEX2	TRUE MAKE_BASE=TRUE	NC_PCH_GPIO66_CLKOUTFLEX2	
16 TP_PCH_GPIO67_CLKOUTFLEX3	TRUE MAKE_BASE=TRUE	NC_PCH_GPIO67_CLKOUTFLEX3	

16 TP_PCIE_CLK100M_PE4N	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE4N	
16 TP_PCIE_CLK100M_PE4P	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE4P	
TP_PCIE_CLK100M_PE5N	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE5N	
TP_PCIE_CLK100M_PE5P	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE5P	
TP_PCIE_CLK100M_PE6N	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE6N	
TP_PCIE_CLK100M_PE6P	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE6P	
TP_PCIE_CLK100M_PE7N	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE7N	
TP_PCIE_CLK100M_PE7P	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE7P	
TP_PSOC_P1_3	TRUE MAKE_BASE=TRUE	NC_PSOC_P1_3	
TP_SATA_B_D2RN	TRUE MAKE_BASE=TRUE	NC_SATA_B_D2RN	
TP_SATA_B_D2RP	TRUE MAKE_BASE=TRUE	NC_SATA_B_D2RP	
TP_SATA_B_R2D_CN	TRUE MAKE_BASE=TRUE	NC_SATA_B_R2D_CN	
TP_SATA_B_R2D_CP	TRUE MAKE_BASE=TRUE	NC_SATA_B_R2D_CP	
16 TP_SATA_D_D2RN	TRUE MAKE_BASE=TRUE	NC_SATA_D_D2RN	
16 TP_SATA_D_D2RP	TRUE MAKE_BASE=TRUE	NC_SATA_D_D2RP	
16 TP_SATA_D_R2D_CN	TRUE MAKE_BASE=TRUE	NC_SATA_D_R2D_CN	
16 TP_SATA_D_R2D_CP	TRUE MAKE_BASE=TRUE	NC_SATA_D_R2D_CP	
16 TP_SATA_E_D2RN	TRUE MAKE_BASE=TRUE	NC_SATA_E_D2RN	
16 TP_SATA_E_D2RP	TRUE MAKE_BASE=TRUE	NC_SATA_E_D2RP	
16 TP_SATA_E_R2D_CN	TRUE MAKE_BASE=TRUE	NC_SATA_E_R2D_CN	
16 TP_SATA_E_R2D_CP	TRUE MAKE_BASE=TRUE	NC_SATA_E_R2D_CP	
16 TP_SATA_F_D2RN	TRUE MAKE_BASE=TRUE	NC_SATA_F_D2RN	
16 TP_SATA_F_D2RP	TRUE MAKE_BASE=TRUE	NC_SATA_F_D2RP	
16 TP_SATA_F_R2D_CN	TRUE MAKE_BASE=TRUE	NC_SATA_F_R2D_CN	
16 TP_SATA_F_R2D_CP	TRUE MAKE_BASE=TRUE	NC_SATA_F_R2D_CP	
TP_PCH_TP18	TRUE MAKE_BASE=TRUE	NC_PCH_TP18	
TP_PCH_TP17	TRUE MAKE_BASE=TRUE	NC_PCH_TP17	
TP_PCH_TP16	TRUE MAKE_BASE=TRUE	NC_PCH_TP16	
TP_PCH_TP15	TRUE MAKE_BASE=TRUE	NC_PCH_TP15	
TP_PCH_TP14	TRUE MAKE_BASE=TRUE	NC_PCH_TP14	
TP_PCH_TP13	TRUE MAKE_BASE=TRUE	NC_PCH_TP13	
TP_PCH_TP12	TRUE MAKE_BASE=TRUE	NC_PCH_TP12	
TP_PCH_TP10	TRUE MAKE_BASE=TRUE	NC_PCH_TP10	
TP_PCH_TP9	TRUE MAKE_BASE=TRUE	NC_PCH_TP9	
TP_PCH_TP8	TRUE MAKE_BASE=TRUE	NC_PCH_TP8	
TP_PCH_TP7	TRUE MAKE_BASE=TRUE	NC_PCH_TP7	
TP_PCH_TP6	TRUE MAKE_BASE=TRUE	NC_PCH_TP6	
TP_PCH_TP5	TRUE MAKE_BASE=TRUE	NC_PCH_TP5	
TP_PCH_TP4	TRUE MAKE_BASE=TRUE	NC_PCH_TP4	
TP_PCH_TP3	TRUE MAKE_BASE=TRUE	NC_PCH_TP3	
TP_PCH_TP2	TRUE MAKE_BASE=TRUE	NC_PCH_TP2	
TP_PCH_TP1	TRUE MAKE_BASE=TRUE	NC_PCH_TP1	
8 TP_LVDS_IG_B_CLKN	TRUE MAKE_BASE=TRUE	NC_LVDS_IG_B_CLKN	
8 TP_LVDS_IG_B_CLKP	TRUE MAKE_BASE=TRUE	NC_LVDS_IG_B_CLKP	
TP_LVDS_IG_BKL_PWM	TRUE MAKE_BASE=TRUE	NC_LVDS_IG_BKL_PWM	
SMC_BS_ALRT_L	TRUE MAKE_BASE=TRUE	NC_SMC_BS_ALRT_L	

SYNC_MASTER=(K99_MLB) SYNC_DATE=(02/16/2010)

PAGE TITLE: Functional Test / No Test

Apple Inc.

DRAWING NUMBER: 051-9276 SIZE: D

REVISION: 2.7.0

BRANCH:

PAGE: 7 OF 109

SHEET: 6 OF 72

"G3Hot" (Always-Present) Rails

52 =PPBUS_G3H → PPBUS_G3H (6 51)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.4V
MAKE_BASE=TRUE
- =PPBUS_S0_LCDBKLT 64
- =PPBUS_S0_VSENSE 44
- =PPVIN_SW_TBTBST 35
- =PPVIN_S5_HS_COMPUTING_ISNS_R 8
- =PPVIN_S5_HS_OTHER_ISNS_R 45

35 6 PPVIN_SW_TBTBST (VOLTAGE=12.8V)

8 =PPVIN_S5_HS_COMPUTING_ISNS → PPBUS_S5_HS_COMPUTING_ISNS (6)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.4V
MAKE_BASE=TRUE
- =PPVIN_S0_CPUIMVP 56 57
- =PPVIN_S3_DDRREG 55
- =PPVIN_S0_CPUVCCIOS0 58
- =PPVIN_S0_VCCSAS0 53
- =PPVIN_S0_CPUAXG 57

45 =PPVIN_S5_HS_OTHER_ISNS → PPBUS_S5_HS_OTHER_ISNS (6)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.4V
MAKE_BASE=TRUE
- =PPVIN_S5_P5VP3V3 54

51 =PP18V5_DCIN_ISOL → PPDCIN_G3H_ISOL (6)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE
- =PPDCIN_S5_CHGR_ISOL 52
- =PPDCIN_S5_VSENSE 44

51 6 =PP18V5_DCIN_CONN → PPDCIN_G3H (6)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE
- =PPDCIN_S5_CHGR 52

51 =PP3V42_G3H_REG → PP3V42_G3H (6)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE
- =PP3V3_S5_LPCPLUS 6 42
- =PP3V3_S5_SMC 40 41
- =PP3V42_G3H_HALL 6 51
- =PP3V42_G3H_CHGR 52
- =PP3V42_G3H_PWRCTL 61
- =PP3V42_G3H_SMBUS_SMC_BSA 43
- =PP3V42_G3H_SMCUSBMUX 38
- =PP3V42_G3H_TPAD 6 48
- =PPVIN_S5_SMCVREF 41
- =PPVBAT_G3H_SYSCLK 25
- =PP3V42_G3H_ONEWIRE 6 39

25 =PPVRTC_G3_OUT → PPVRTC_G3H (6)
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3V
MAKE_BASE=TRUE
- =PPVRTC_G3_PCH 16 17 20

5V Rails

54 =PP5V_S5_LDO → PP5V_S5 (6)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S5_P1V5DDRFET 60
- =PP5V_S5_P5VSUSFET 60
- =PP5V_S5_TPAD 48

60 =PP5V_SUS_FET → PP5V_SUS (6)
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_SUS_PCH 22

54 =PP5V_S3_REG → PP5V_S3 (6)
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S3_AUDIO_AMP 50
- =PP5V_S3_DDRREG 55
- =PP5V_S3_MEMRESET 26
- =PP5V_S3_P5VS0FET 60
- =PP5V_S3_RTUSB 38
- =PP5V_S3_LIO_CONN 6 51

60 =PP5V_S0_FET → PP5V_S0 (6)
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S0_BKL 64
- =PP5V_S0_CPUIMVP 56
- =PP5V_S0_CPUVCCIOS0 58
- =PP5V_S0_FAN 6 47
- =PP5V_S0_LPCPLUS 6 42
- =PP5V_S0_VCCSA 53
- =PP5V_S0_PCH 22 25
- =PP5V_S0_VMON 61
- =PP5V_S0_KBDLED 48

3.3V Rails

54 =PP3V3_S5_REG → PP3V3_S5 (6 71)
MIN_LINE_WIDTH=0.6 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
- =PP3V3_S5_XDP 23
- =PP3V3_S0_P3V3S0FET 60
- =PP3V3_S3_P3V3S3FET 60
- =PP3V3_S5_CPU_VCCDDR 26
- =PP3V3_S5_LCD 62
- =PP3V3_S5_PCH 17
- =PP3V3_S5_PCHPWRGD 25
- =PP3V3_S5_SMCBATLOW 41
- =PP3V3_S5_PCH_VCCDSW 20 22
- =PP3V3_S5_SYSCLK 25
- =PP3V3_S5_VMON 61
- =PP3V3_S5_PWRCTL 61
- =PP3V3_S5_PCH_GPIO 19
- =PP3V3_S5_P3V3SUSFET 60
- =PP3V3_S4_P3V3S4FET 60
- =PP3V3_S4_TBTAPWRSW 63

60 =PP3V3_S4_FET → PP3V3_S4 (6)
MIN_LINE_WIDTH=0.60MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_S4_SMC 41
- =PP3V3_S4_TPAD 48
- =PP3V3_S4_BT 36

60 =PP3V3_SUS_FET → PP3V3_SUS (6)
MIN_LINE_WIDTH=0.50MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_SUS_ROM 49
- =PP3V3_SUS_PCH_VCCSUS 20 22
- =PP3V3_SUS_PCH_GPIO 16 17 18 19
- =PP3V3_SUS_PCH 22
- =PP3V3_SUS_PWRCTL 61
- =PP3V3_SUS_P1V05SUSLDO 59
- =PP3V3_SUS_SMC 41
- =PP3V3_SUS_PCH_VCC_SPI 20 22
- =PP3V3_SUS_PCH_VCCSUS_USB 20 22

=PP3V3_S4_TBTAPWR → PP3V3_SW_TBTAPWR (63)
MIN_LINE_WIDTH=0.38 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20 MM MAKE_BASE=TRUE
- =PP3V3_S4_TBT 33 34 35

60 =PP3V3_S3_FET → PP3V3_S3 (6)
MIN_LINE_WIDTH=0.50MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_S3_BT 36
- =PP3V3_S3_MEMRESET 26
- =PP3V3_S3_SMBUS_SMC_A_S3 43
- =PP3V3_S3_SMBUS_SMC_MGMT 43
- =PP3V3_S3_USB_HUB 8 24
- =PP3V3_S3_USB_RESET 24
- =PP3V3_S3_VREFMRGN 31
- =PP3V3_S3_WLAN 36
- =PP3V3_S3_WLANISNS 45
- =PP3V3_S3_PCH_GPIO 18 25
- =PP3V3_S3_USBMUX 24
- =PP3V3_S3_1V5S3ISNS 45
- =PP3V3_S3_DBGLEDS 51

60 =PP3V3_S0_FET → PP3V3_S0 (6 71)
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_S0_PCH_VCC3_3_CLK 22
- =PP3V3_S0_CPUVCCIOISNS 44
- =PP3V3_S0_AUDIO 6 39
- =PP3V3_S0_BKL_VDDIO 64
- =PP3V3_S0_HS_COMPUTING_ISNS 45
- =PP3V3_S0_CPUTHMSNS 46
- =PP3V3_S0_CPU_VCCIO_SEL 12
- =PP3V3_S0_DP_DDC 8
- =PP3V3_S0_FAN 47
- =PP3V3_S0_P3V3TBTFET 35
- =PP3V3_S0_P1V8S0 59
- =PP3V3_S0_PCH 16 22
- =PP3V3_S0_PCH_GPIO 16 17 18 19 25 35
- =PP3V3_S0_SATAMUX 37
- =PP3V3_S0_PCH_VCC3_3 20 22
- =PP3V3_S0_HS_OTHER_ISNS 45
- =PP3V3_S0_PCH_VCCADAC 22
- =PP3V3_S0_PWRCTL 61
- =PP3V3_S0_RSTBUF 25
- =PP3V3_S0_SB_PM 25
- =PP3V3_S0_SMBUS_PCH 43
- =PP3V3_S0_SMBUS_SMC_0_S0 43
- =PP3V3_S0_SMBUS_SMC_B_S0 43
- =PP3V3_S0_SMC 41
- =PP3V3_S0_SSD 37
- =PP3V3_S0_HDDISNS 45
- =PP3V3_S0_VMON 61
- =PP3V3_S0_P1V5S0 59
- =PP3V3_S0_TBTPWRCTL 35
- =PP3V3_S0_3V3S0ISNS 44
- =PP3V3_S0_P1V05S0LDO 59
- =PP3V3_S0_IMVPISNS 44
- =PP3V3_S0_XDP 23
- =PP3V3_S0_BKLTISNS 45
- =PP3V3_S0_SYSCLKGEN 25
- =PP3V3_S0_SAISNS 44
- =PP3V3_S0_PCH_STRAPS 19

1.8V/1.5V/1.2V/1.05V Rails

59 =PP1V8_S0_REG → PP1V8_S0 (6)
2A max supply
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
- =PP1V8_S0_CPU_VCCPLL 14
- =PP1V8_S0_PCH_VCC_DFTERM 19 20 22
- =PP1V8_S0_P1V05S0LDO 59
- =PP1V8R1V5_S0_PCH_VCCVRM 20
- =PPVDDIO_S0_SBCLK 25
- =PP1V8_S0_P1V5S0 59

55 =PPDDR_S3_REG → PP1V5_S3 (6 66)
MIN_LINE_WIDTH=0.8 MM
MIN_NECK_WIDTH=0.1 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
- =PP1V5_S3_MEMRESET 26
- =PP1V5_S3_MEM_A 27 28 32
- =PP1V5_S3_MEM_B 29 30 32
- =PP1V5_S3_P1V5S3RS0_FET 60
- =PPVIN_S0_DDRREG_LDO 55
- =PPDDR_S3_MEMVREF 31

60 =PP1V5_S3RS0_FET → PP1V5_S3RS0 (6 66)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
- =PP1V5_S3_CPU_VCCDDR 10 12 15 26
- =PP1V5_S3RS0_VMON 61

59 =PP1V5_S0_REG → PP1V5_S0 (6)
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
- =PP3V3R1V5_S0_AUDIO 6 39
- =PP3V3R1V5_S0_PCH_VCCSUSHDA 20 22 25

55 31 =PPVTT_S3_DDR_BUF → PPVTTDDR_S3 (6)
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE

55 =PPVTT_S0_DDR_LDO → PP0V75_S0_DDRVTT (6)
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE
- =PP0V75_S0_MEM_VTT_A 32
- =PP0V75_S0_MEM_VTT_B 32
- =PPVTT_S0_VTTCLAMP 26

53 =PPVCCSA_S0_REG → PPVCCSA_S0_CPU (6)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.9V
MAKE_BASE=TRUE
- =PPVCCSA_S0_CPU 12 15
- =PPVCCSA_S0_VSENSE 44

59 =PP1V05_SUS_LDO → PP1V05_SUS (6)
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_SUS_PCH_JTAG 23

58 =PPCPUVCCIO_S0_REG → PP1V05_S0 (6)
? mA
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_S0_CPU_VCCIO 9 10 12 14
- =PP1V05_S0_PCH 16 22
- =PP1V05_S0_PCH_VCCIO 20 22
- =PP1V05_S0_PCH_VCCIO_PCIE 17
- =PP1V05_S0_PCH_VCCIO_SATA 16 22
- =PP1V05_S0_PCH_VCCASW 20 22
- =PP1V05_S0_PCH_VCC_CORE 20 22
- =PP1V05_S0_VMON 61
- =PPVCCIO_S0_CPUIMVP 56
- =PP1V05_S0_PCH_VCCDIFFCLK 16 20 22
- =PP1V05_S0_PCH_VCCSSC 20 22
- =PP1V05_S0_PCH_V_PROC_IO 20 22
- =PP1V05_S0_PCH_VCC_DMI 20 22
- =PPVCCIO_S0_XDP 23
- =PPVCCIO_S0_SMC 41
- =PP1V05_S0_P1V05TBTFET 35

TBT Rails (off when no cable)

35 =PP15V_TBT_REG → PP15V_TBT (6)
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=17.8V
MAKE_BASE=TRUE
- =PPHV_SW_TBTAPWRSW 63

35 =PP3V3_TBTLC_FET → PP3V3_TBTLC (6)
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PPVDDIO_TBT_CLK 25
- =PP3V3_TBTLC_RTR 33 34 35
- =PP3V3_TBT_PCH_GPIO 19

35 =PP1V05_TBTLC_FET → PP1V05_TBTLC (6 35)
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_TBTLC_RTR 34

35 =PP1V05_TBTCIO_FET → PP1V05_TBTCIO (6)
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_TBTCIO_RTR 34

1V05 S0 LDO

59 =PP1V05_S0_LDO → PP1V05_S0_PCH_VCCADPLL (6)
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_S0_PCH_VCCADPLL 22

Chipset "VCore" Rails

57 =PPVCORE_S0_CPU_REG → PPVCORE_S0_CPU (6)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE
- =PPVCORE_S0_CPU 9 12 14
- =PPCPUVCORE_S0_VSENSE 44

57 =PPVCORE_S0_AXG_REG → PPVCORE_S0_AXG (6)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PPVCORE_S0_CPU_VCCAXG 9 12 15
- =PPGFXVCORE_S0_VSENSE 44

15 12 =PP1V5_S3_CPU_VCCDQ → PP1V5_S3_CPU_VCCDQ (6)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE

14 12 =PP1V05_S0_CPU_VCCPQE → PP1V05_S0_CPU_VCCPQE (6)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

14 12 =PP1V8_S0_CPU_VCCPLL_R → PP1V8_S0_CPU_VCCPLL_R (6)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE

SYNC_MASTER=K91_MLB SYNC_DATE=05/15/2010
PAGE TITLE
Power Aliases

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D
REVISION 2.7.0
BRANCH
PAGE 8 OF 109
SHEET 7 OF 72

CPU Heat Sink Mounting Bosses

Z0913 STDOFF-4.5OD1.8H-SM
Z0910 STDOFF-4.5OD1.8H-SM
Z0911 STDOFF-4.5OD1.8H-SM
Z0912 STDOFF-4.5OD1.8H-SM
4x 860-1327

Fan Boss
Z0905 STDOFF-4.5OD1.8H-SM
860-1327

X21 Boss
Z0914 STDOFF-4.5OD1.9H-SM
860-1327

SSD Boss
Z0915 STDOFF-4.5OD1.9H-SM
860-1327

EMI I/O Pogo Pins

DisplayPort Pogo
CRITICAL
ZS0905
POGO-2.0OD-3.6H-K86-K87
870-1938

USB/SD Card Pogo
CRITICAL
ZS0907
POGO-2.0OD-2.95H-K86-K87
870-1940

Can Slots

SL0901 TH-NSP, SL-1.1X0.4-1.4x0.7, 998-2691	SL0902 TH-NSP, SL-1.1X0.4-1.4x0.7, 998-2691	2x MDP connector
SL0903 TH-NSP, SL-1.1X0.45-1.4x0.75, 998-3975	SL0904 TH-NSP, SL-1.1X0.45-1.4x0.75, 998-3975	2x USB connector
SL0905 TH-NSP, SL-1.1X0.4-1.4x0.7, 998-2691	SL0906 TH-NSP, SL-1.1X0.4-1.4x0.7, 998-2691	2x TBT pin diodes
SL0907 TH-NSP, SL-1.1X0.45-1.4x0.75, 998-3975	SL0908 TH-NSP, SL-1.1X0.45-1.4x0.75, 998-3975	2x TBT chip
SL0909 TH-NSP, SL-1.1X0.4-1.4x0.7, 998-2691	SL0910 TH-NSP, SL-1.1X0.4-1.4x0.7, 998-2691	2x CPU Vcore

Digital Ground

GND
VOLTAGE=0V
MIN_NECK_WIDTH=0.075MM
MIN_LINE_WIDTH=0.6MM

CPU signals

26 MEMVTT_EN (MAKE_BASE=TRUE) — =DDRVTT_EN 26 55

68 33 DP_TBTSNK0_AUXCH_C_P (MAKE_BASE=TRUE) — DPA_IG_AUX_CH_P 17
68 33 DP_TBTSNK0_AUXCH_C_N (MAKE_BASE=TRUE) — DPA_IG_AUX_CH_N 17

16 PCIE_CLK100M_ENET_N	TRUE	NC_PCIE_CLK100M_ENETN
16 PCIE_CLK100M_ENET_P	MAKE_BASE=TRUE TRUE	NC_PCIE_CLK100M_ENETP
16 PCIE_EXCARD_D2R_N	MAKE_BASE=TRUE TRUE	NC_PCIE_EXCARD_D2RN
16 PCIE_EXCARD_D2R_P	MAKE_BASE=TRUE TRUE	NC_PCIE_EXCARD_D2RP
16 PCIE_EXCARD_R2D_C_N	MAKE_BASE=TRUE TRUE	NC_PCIE_EXCARD_R2D_CN
16 PCIE_EXCARD_R2D_C_P	MAKE_BASE=TRUE TRUE	NC_PCIE_EXCARD_R2D_CP
16 PCIE_CLK100M_EXCARD_N	MAKE_BASE=TRUE TRUE	NC_PCIE_CLK100M_EXCARDN
16 PCIE_CLK100M_EXCARD_P	MAKE_BASE=TRUE TRUE	NC_PCIE_CLK100M_EXCARDP
	MAKE_BASE=TRUE	

68 16 PEG_CLK100M_P (MAKE_BASE=TRUE) — NC_PEG_CLK100MP
68 16 PEG_CLK100M_N (MAKE_BASE=TRUE) — NC_PEG_CLK100MN

16 TP_PCH_CLKOUT_DPN (MAKE_BASE=TRUE) — DPLL_REF_CLK_N — DPLL_REF_CLKN 10 65
16 TP_PCH_CLKOUT_DPP (MAKE_BASE=TRUE) — DPLL_REF_CLK_P — DPLL_REF_CLKP 10 65

66 11 MEM_A_CLK_P<1> (MAKE_BASE=TRUE) — TP_MEM_A_CLKP<1>
66 11 MEM_A_CLK_N<1> (MAKE_BASE=TRUE) — TP_MEM_A_CLKN<1>

66 11 MEM_B_CLK_P<1> (MAKE_BASE=TRUE) — TP_MEM_B_CLKP<1>
66 11 MEM_B_CLK_N<1> (MAKE_BASE=TRUE) — TP_MEM_B_CLKN<1>

18 USB_EXTC_P	TRUE	NC_USB_EXTCP
18 USB_EXTC_N	MAKE_BASE=TRUE TRUE	NC_USB_EXTCN
18 USB3_EXTC_RX_P	MAKE_BASE=TRUE TRUE	NC_USB3_EXTC_RXP
18 USB3_EXTC_RX_N	MAKE_BASE=TRUE TRUE	NC_USB3_EXTC_RXN
18 USB3_EXTC_TX_P	MAKE_BASE=TRUE TRUE	NC_USB3_EXTC_TXP
18 USB3_EXTC_TX_N	MAKE_BASE=TRUE TRUE	NC_USB3_EXTC_TXN
18 USB3_EXTD_RX_P	MAKE_BASE=TRUE TRUE	NC_USB3_EXTD_RXP
18 USB3_EXTD_RX_N	MAKE_BASE=TRUE TRUE	NC_USB3_EXTD_RXN
18 USB3_EXTD_TX_P	MAKE_BASE=TRUE TRUE	NC_USB3_EXTD_TXP
18 USB3_EXTD_TX_N	MAKE_BASE=TRUE TRUE	NC_USB3_EXTD_TXN
18 USB_EXTD_EHCI_P	MAKE_BASE=TRUE TRUE	NC_USB_EXTD_EHCIP
19 USB_EXTD_EHCI_N	MAKE_BASE=TRUE TRUE	NC_USB_EXTD_EHCIN
	MAKE_BASE=TRUE	

TBT_B_R2D_C_P<0>	TRUE	NC_TBT_B_R2D_CP<0>
69 33 TBT_B_R2D_C_N<0>	MAKE_BASE=TRUE TRUE	NC_TBT_B_R2D_CN<0>
69 33 TBT_B_R2D_C_P<1>	MAKE_BASE=TRUE TRUE	NC_TBT_B_R2D_CP<1>
69 33 TBT_B_R2D_C_N<1>	MAKE_BASE=TRUE TRUE	NC_TBT_B_R2D_CN<1>
69 33 TBT_B_D2R_P<0>	MAKE_BASE=TRUE TRUE	NC_TBT_B_D2RP<0>
69 33 TBT_B_D2R_N<0>	MAKE_BASE=TRUE TRUE	NC_TBT_B_D2RN<0>
69 33 TBT_B_D2R_P<1>	MAKE_BASE=TRUE TRUE	NC_TBT_B_D2RP<1>
69 33 TBT_B_D2R_N<1>	MAKE_BASE=TRUE TRUE	NC_TBT_B_D2RN<1>
33 TBT_B_LSTX	MAKE_BASE=TRUE TRUE	NC_TBT_B_LSTX
	MAKE_BASE=TRUE	

69 33 DP_TBTPB_ML_C_P<1>	MAKE_BASE=TRUE	NC_DP_TBTPB_ML_CP<1>
69 33 DP_TBTPB_ML_C_N<1>	MAKE_BASE=TRUE	NC_DP_TBTPB_ML_CN<1>
69 33 DP_TBTPB_ML_C_P<3>	MAKE_BASE=TRUE	NC_DP_TBTPB_ML_CP<3>
69 33 DP_TBTPB_ML_C_N<3>	MAKE_BASE=TRUE	NC_DP_TBTPB_ML_CN<3>

16 PCIE_CLK100M_FW_N	MAKE_BASE=TRUE	NC_PCIE_CLK100M_FWN
16 PCIE_CLK100M_FW_P	MAKE_BASE=TRUE	NC_PCIE_CLK100M_FWP
9 =PEG_D2R_P<1..0>	MAKE_BASE=TRUE	PCIE_SSD_D2R_P<1..0> 6 37 65
9 =PEG_D2R_N<1..0>	MAKE_BASE=TRUE	PCIE_SSD_D2R_N<1..0> 6 37 65
9 =PEG_R2D_C_P<1..0>	MAKE_BASE=TRUE	PCIE_SSD_R2D_C_P<1..0> 37 65
9 =PEG_R2D_C_N<1..0>	MAKE_BASE=TRUE	PCIE_SSD_R2D_C_N<1..0> 37 65

16 PCIE_ENET_D2R_N	TRUE	NC_PCIE_ENET_D2RN
16 PCIE_ENET_D2R_P	MAKE_BASE=TRUE TRUE	NC_PCIE_ENET_D2RP
16 PCIE_ENET_R2D_C_N	MAKE_BASE=TRUE TRUE	NC_PCIE_ENET_R2D_CN
16 PCIE_ENET_R2D_C_P	MAKE_BASE=TRUE TRUE	NC_PCIE_ENET_R2D_CP
16 PCIE_FW_D2R_N	MAKE_BASE=TRUE TRUE	NC_PCIE_FW_D2RN
16 PCIE_FW_D2R_P	MAKE_BASE=TRUE TRUE	NC_PCIE_FW_D2RP
16 PCIE_FW_R2D_C_N	MAKE_BASE=TRUE TRUE	NC_PCIE_FW_R2D_CN
16 PCIE_FW_R2D_C_P	MAKE_BASE=TRUE TRUE	NC_PCIE_FW_R2D_CP
	MAKE_BASE=TRUE	

8 7 =PP3V3_S0_DP_DDC
R0920 2.2K 5% 1/20W MF 201
R0921 2.2K 5% 1/20W MF 201
R0922 2.2K 5% 1/20W MF 201 NOSTUFF
R0923 2.2K 5% 1/20W MF 201 NOSTUFF
DPB_IG_DDC_CLK
DPB_IG_DDC_DATA

17 TP_DP_IG_D_CTRL_CLK (MAKE_BASE=TRUE) — DP_IG_D_CTRL_CLK 17
17 TP_DP_IG_D_CTRL_DATA (MAKE_BASE=TRUE) — DP_IG_D_CTRL_DATA 17

8 7 =PP3V3_S0_DP_DDC
R0924 470K 5% 1/20W MF 201
R0925 470K 5% 1/20W MF 201

63 DP_TBTSNK0_DDC_CLK (MAKE_BASE=TRUE) — DPA_IG_DDC_CLK 17
63 DP_TBTSNK0_DDC_DATA (MAKE_BASE=TRUE) — DPA_IG_DDC_DATA 17
33 DP_TBTSNK0_HPD (MAKE_BASE=TRUE) — DPA_IG_HPD 17

CRITICAL
R0910 0.01 0.5% 1W MF 0612-1
64 PPBUS_SW_LCDBKLT_PWR (MAKE_BASE=TRUE) — PPBUS_SW_BKL
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.375 MM
VOLTAGE=12.6V
MAKE_BASE=TRUE
71 45 OUT ISNS_LCDBKLT_P
71 45 OUT ISNS_LCDBKLT_N
=PPBUS_SW_BKL 64

CRITICAL
R0954 0.002 1% 1W MF 0612
7 OUT =PPVIN_S5_HS_COMPUTING_ISNS
1 =PPVIN_S5_HS_COMPUTING_ISNS_R 7 IN
71 45 OUT ISNS_HS_COMPUTING_N
71 45 OUT ISNS_HS_COMPUTING_P

UNUSED SDCARD USB Aliases

=PP3V3_S3_USB_HUB
R0901 10K 5% 1/20W MF 201
R0902 10K 5% 1/20W MF 201
67 24 OUT USB_SDCARD_N
67 24 OUT USB_SDCARD_P

33 TBT_B_CIO_SEL
33 DP_TBTPB_HPD
33 TBT_B_CONFIG2_RC
33 TBT_B_CONFIG1_BUF
33 TBT_B_LSRX
R0916 10K 5% 1/20W MF 201
R0917 10K 5% 1/20W MF 201
R0918 10K 5% 1/20W MF 201
R0919 10K 5% 1/20W MF 201
R0914 10K 5% 1/20W MF 201

23 19 XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH (MAKE_BASE=TRUE) — ENET_LOW_PWR_PCH 19
23 16 XDP_DC3_PCH_GPIO19_SATARDRVR_EN (MAKE_BASE=TRUE) — SATARDRVR_EN 16

19 MLB_RAMCFG3
19 MLB_RAMCFG2
19 MLB_RAMCFG1
19 MLB_RAMCFG0
RAMCFG3:L R0950 10K 5% 1/20W MF 201
RAMCFG2:L R0951 10K 5% 1/20W MF 201
RAMCFG1:L R0952 10K 5% 1/20W MF 201
RAMCFG0:L R0953 10K 5% 1/20W MF 201

TBT DP Ports

17 DPB_IG_HPD		DP_TBTSNK1_HPD 33
17 TP_DP_IG_C_MLP<3..0>	MAKE_BASE=TRUE	DP_TBTSNK1_ML_C_P<3..0> 33 68
17 TP_DP_IG_C_MLN<3..0>	MAKE_BASE=TRUE	DP_TBTSNK1_ML_C_N<3..0> 33 68
17 DPB_IG_AUX_CH_P	MAKE_BASE=TRUE	DP_TBTSNK1_AUXCH_C_P 33 68
17 DPB_IG_AUX_CH_N	MAKE_BASE=TRUE	DP_TBTSNK1_AUXCH_C_N 33 68
	MAKE_BASE=TRUE	
17 TP_DP_IG_D_HPD		DP_IG_D_HPD
	MAKE_BASE=TRUE	
69 33 DP_TBTPB_AUXCH_C_P	MAKE_BASE=TRUE	NC_DP_TBTPB_AUXCH_CP
69 33 DP_TBTPB_AUXCH_C_N	MAKE_BASE=TRUE	NC_DP_TBTPB_AUXCH_CN
	MAKE_BASE=TRUE	
17 TP_DP_IG_B_MLP<3..0>	MAKE_BASE=TRUE	DP_TBTSNK0_ML_C_P<3..0> 33 68
17 TP_DP_IG_B_MLN<3..0>	MAKE_BASE=TRUE	DP_TBTSNK0_ML_C_N<3..0> 33 68
	MAKE_BASE=TRUE	

R0909 100K 5% 1/20W MF 201

16 NC_PCIE_5_R2D_CP	MAKE_BASE=TRUE	PCIE_TBT_R2D_C_P<0> 33 68
16 NC_PCIE_6_R2D_CP	MAKE_BASE=TRUE	PCIE_TBT_R2D_C_P<1> 33 68
16 NC_PCIE_7_R2D_CP	MAKE_BASE=TRUE	PCIE_TBT_R2D_C_P<2> 33 68
16 NC_PCIE_8_R2D_CP	MAKE_BASE=TRUE	PCIE_TBT_R2D_C_P<3> 33 68
16 NC_PCIE_5_R2D_CN	MAKE_BASE=TRUE	PCIE_TBT_R2D_C_N<0> 33 68
16 NC_PCIE_6_R2D_CN	MAKE_BASE=TRUE	PCIE_TBT_R2D_C_N<1> 33 68
16 NC_PCIE_7_R2D_CN	MAKE_BASE=TRUE	PCIE_TBT_R2D_C_N<2> 33 68
16 NC_PCIE_8_R2D_CN	MAKE_BASE=TRUE	PCIE_TBT_R2D_C_N<3> 33 68
	MAKE_BASE=TRUE	
16 NC_PCIE_5_D2RP	MAKE_BASE=TRUE	PCIE_TBT_D2R_P<0> 33 68
16 NC_PCIE_6_D2RP	MAKE_BASE=TRUE	PCIE_TBT_D2R_P<1> 33 68
16 NC_PCIE_7_D2RP	MAKE_BASE=TRUE	PCIE_TBT_D2R_P<2> 33 68
16 NC_PCIE_8_D2RP	MAKE_BASE=TRUE	PCIE_TBT_D2R_P<3> 33 68
16 NC_PCIE_5_D2RN	MAKE_BASE=TRUE	PCIE_TBT_D2R_N<0> 33 68
16 NC_PCIE_6_D2RN	MAKE_BASE=TRUE	PCIE_TBT_D2R_N<1> 33 68
16 NC_PCIE_7_D2RN	MAKE_BASE=TRUE	PCIE_TBT_D2R_N<2> 33 68
16 NC_PCIE_8_D2RN	MAKE_BASE=TRUE	PCIE_TBT_D2R_N<3> 33 68
	MAKE_BASE=TRUE	

LVDS Aliases

6 TP_LVDS_IG_B_CLKP	MAKE_BASE=TRUE	LVDS_IG_B_CLK_P
6 TP_LVDS_IG_B_CLKN	MAKE_BASE=TRUE	LVDS_IG_B_CLK_N
NC_LVDS_IG_B_DATAP<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE	LVDS_IG_B_DATA_P<0..3>
NC_LVDS_IG_B_DATAN<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE	LVDS_IG_B_DATA_N<0..3>
NC_LVDS_IG_A_DATAP<3>	MAKE_BASE=TRUE NO_TEST=TRUE	LVDS_IG_A_DATA_P<3>
NC_LVDS_IG_A_DATAN<3>	MAKE_BASE=TRUE NO_TEST=TRUE	LVDS_IG_A_DATA_N<3>
64 LCD_BKLT_PWM	MAKE_BASE=TRUE	LVDS_IG_BKL_PWM 17
62 LCD_IG_PWR_EN	MAKE_BASE=TRUE	LVDS_IG_PANEL_PWR 17
64 LCD_BKLT_EN	MAKE_BASE=TRUE	LVDS_IG_BKL_ON 17

SATA Aliases

Unused SATA ODD Signals

16 IN SATA_ODD_R2D_C_P	MAKE_BASE=TRUE NO_TEST=TRUE	NC_SATA_ODD_R2DCP
16 IN SATA_ODD_R2D_C_N	MAKE_BASE=TRUE NO_TEST=TRUE	NC_SATA_ODD_R2DCN
16 OUT SATA_ODD_D2R_P	MAKE_BASE=TRUE NO_TEST=TRUE	NC_SATA_ODD_D2RP
16 OUT SATA_ODD_D2R_N	MAKE_BASE=TRUE NO_TEST=TRUE	NC_SATA_ODD_D2RN

SMC Aliases

Unused SMC Signals

40 IN SMC_SYS_LED	MAKE_BASE=TRUE NO_TEST=TRUE	NC_SMC_SYS_LED
40 OUT IR_RX_OUT_RC	MAKE_BASE=TRUE NO_TEST=TRUE	NC_IR_RX_OUT_RC

Unused PGOOD signal

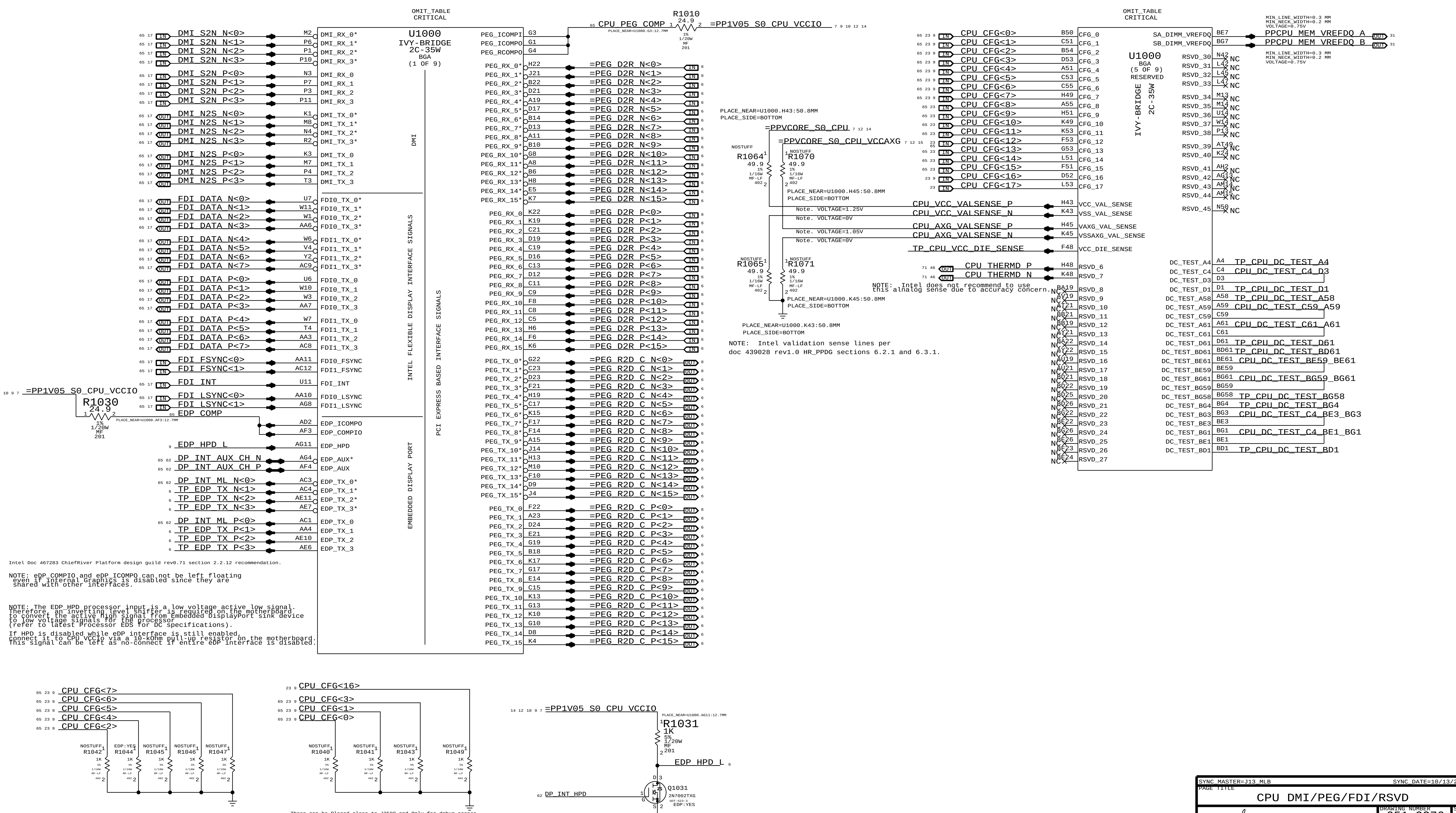
TP_P1V5S3RS0_RAMP_DONE (MAKE_BASE=TRUE) — P1V5S3RS0_RAMP_DONE IN 60
TP_DDRREG_PGOOD (MAKE_BASE=TRUE) — DDRREG_PGOOD IN 55

SYNC_MASTER=K91_MLB SYNC_DATE=05/15/2010
PAGE TITLE: Signal Aliases

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D
REVISION 2.7.0
BRANCH
PAGE 9 OF 109
SHEET 8 OF 72

NOTE: Intel provides an internal pull-up OF 5-15k to VCCIO on all CFG signals.



Intel Doc 467283 ChiefRiver Platform design guild rev0.71 section 2.2.12 recommendation.

NOTE: eDP_COMPIO and eDP_ICOMPO can not be left floating even if internal Graphics is disabled since they are shared with other interfaces.

NOTE: The EDP_HPD processor input is a low voltage active low signal. Therefore, an inverting level shifter is required on the motherboard to convert the active high signal from Embedded DisplayPort sink device to low voltage signals for the processor (refer to latest Processor EDS for DC specifications).

If HPD is disabled while eDP interface is still enabled, connect it to CPU VCCIO via a 10-kOhm pull-up resistor on the motherboard. This signal can be left as no-connect if entire eDP interface is disabled.

FOR IVYBRIDGE PROCESSOR

CFG [7]	:PEG DEFER TRAINING	1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB 0 = WAIT FOR BIOS
CFG [6:5]	:PCIE BIFURCATION	11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4]	:eDP ENABLE/DISABLE	1 = DISABLED 0 = ENABLED
CFG [3]	:PCIE x4 LANE REVERSAL	1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [2]	:PCIE x16 LANE REVERSAL	1 = NORMAL OPERATION 0 = LANES REVERSED

SYNC_MASTER=J13_MLB SYNC_DATE=10/13/2011

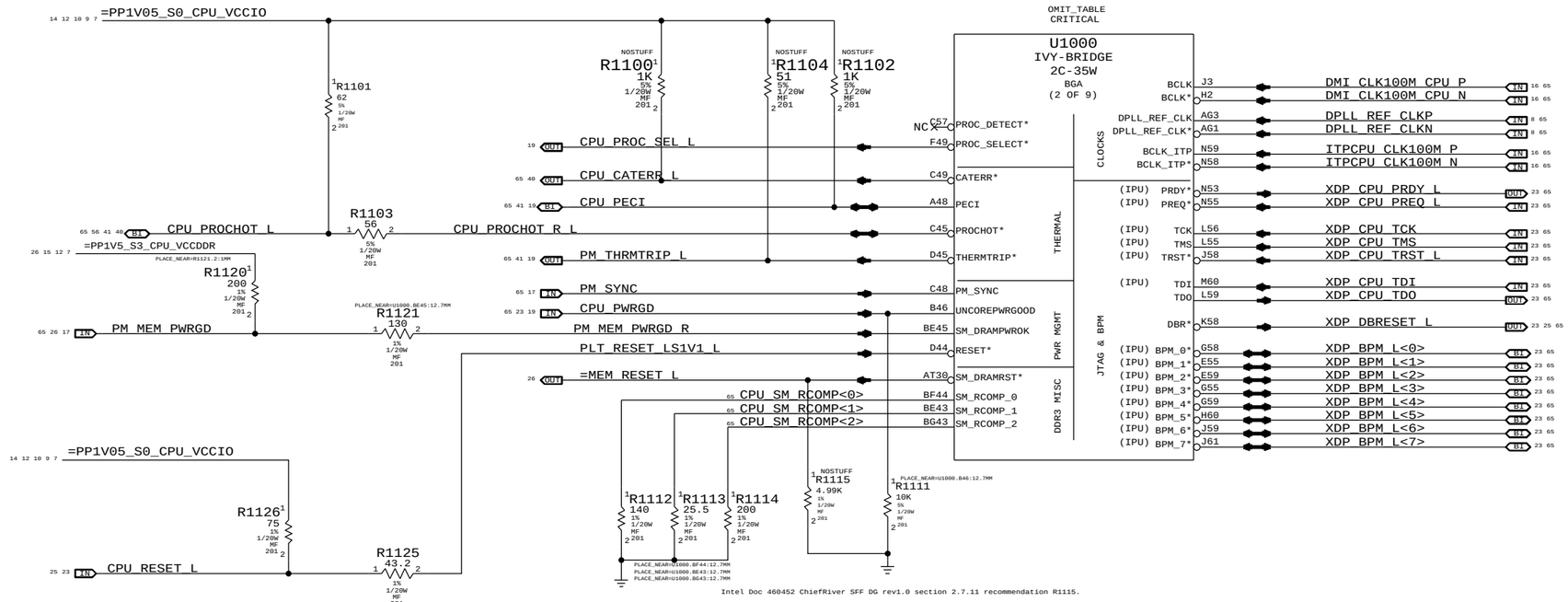
PAGE TITLE: CPU DMI/PEG/FDI/RSVD

Apple Inc.

DRAWING NUMBER: 051-9276 SIZE: D

REVISION: 2.7.0

BRANCH



SYNC_MASTER=J13_MLB SYNC_DATE=09/22/2013

PAGE TITLE

CPU CLOCK/MISC/JTAG

Apple Inc.

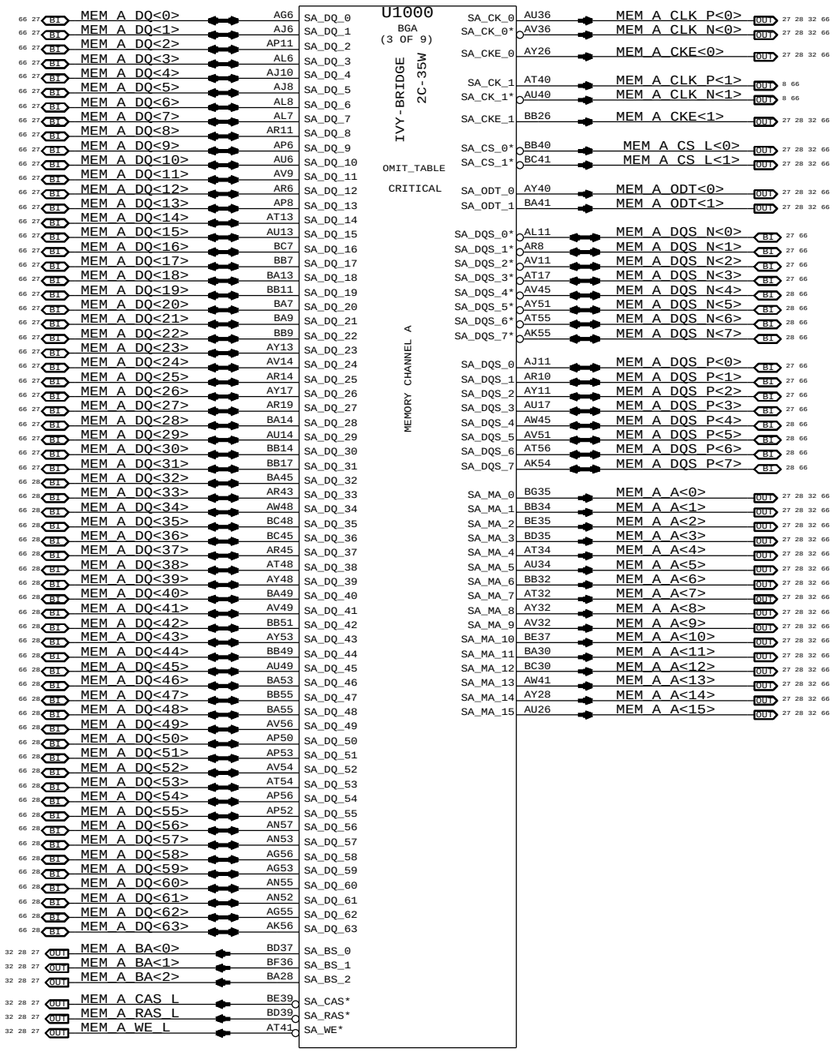
DRAWING NUMBER 051-9276 SIZE D

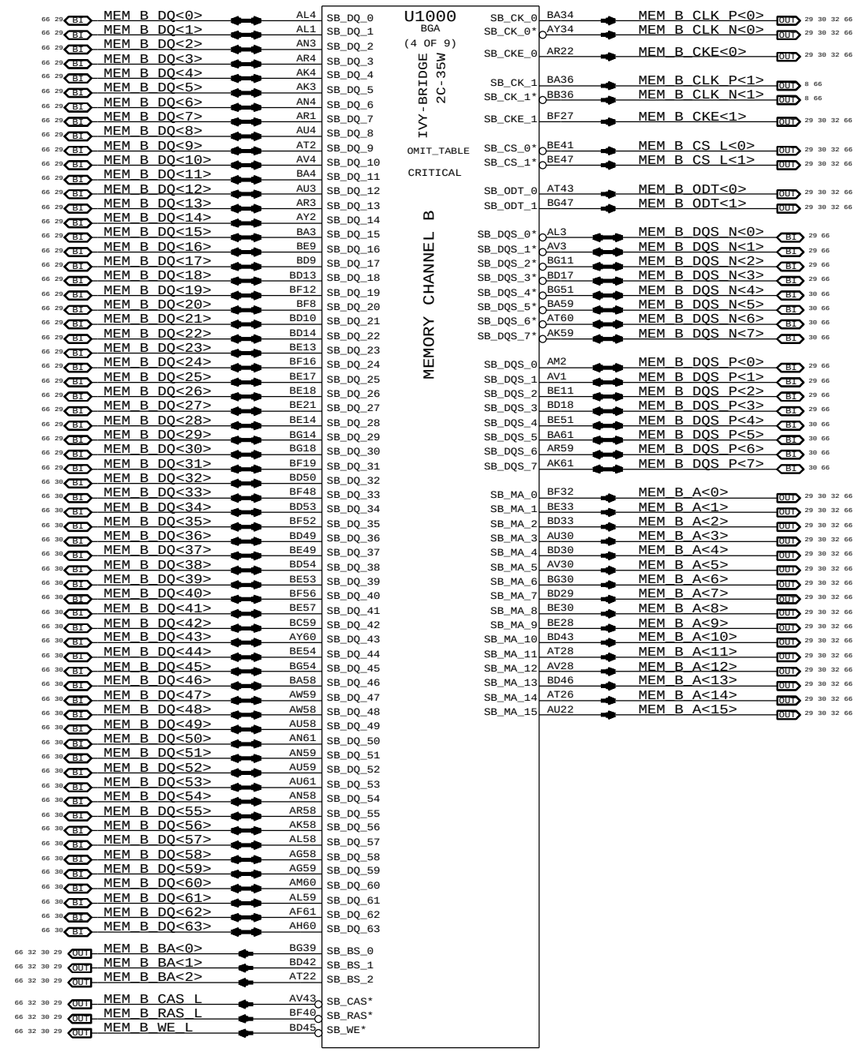
REVISION 2.7.0

BRANCH

PAGE 11 OF 109

SHEET 10 OF 72



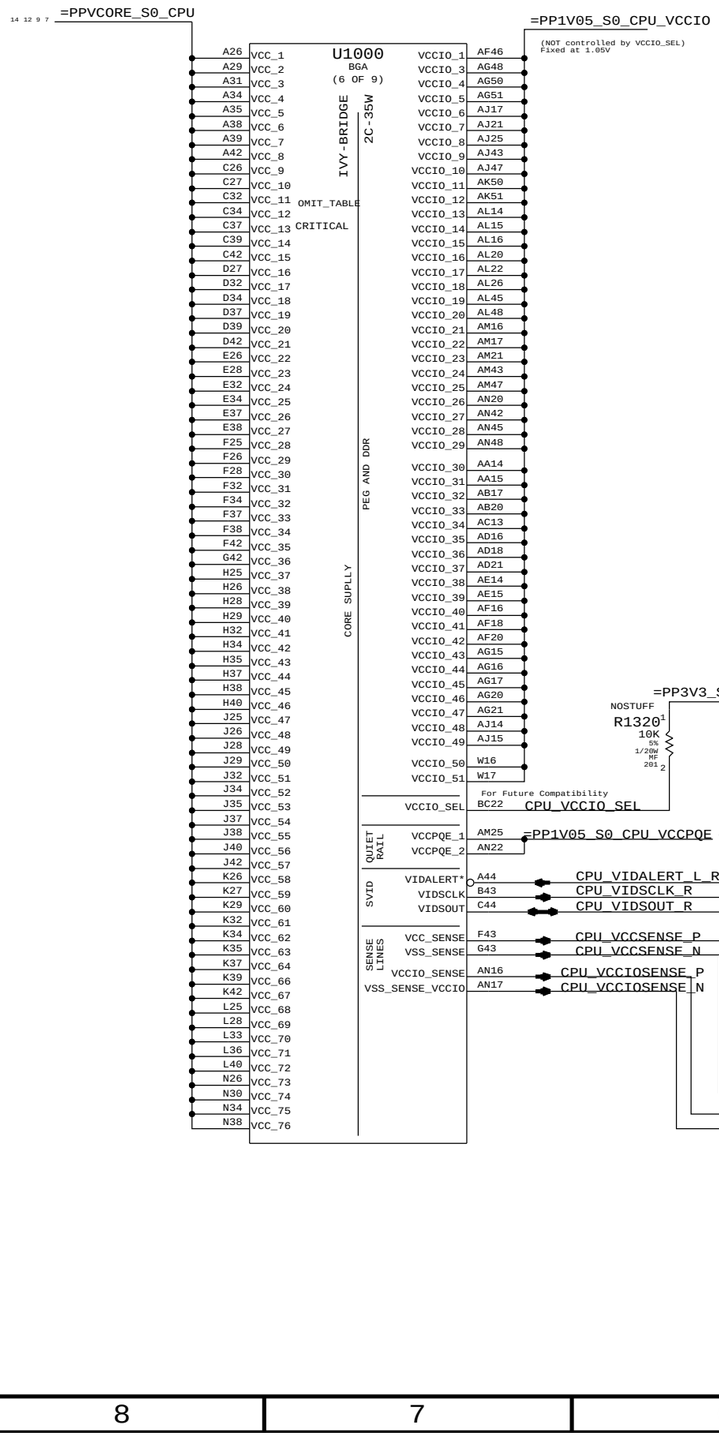


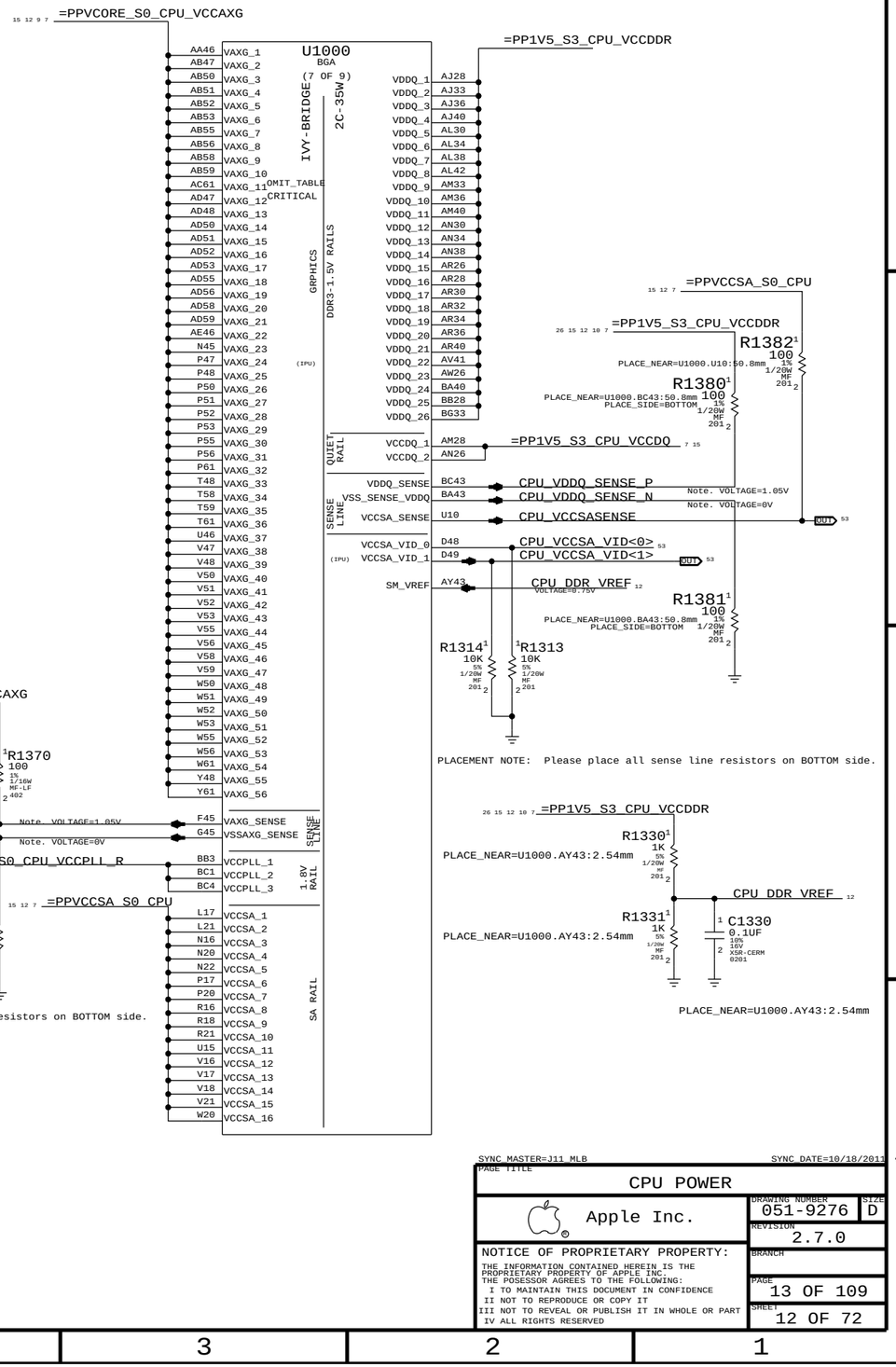
SYNC_DATE=12/13/2010

PAGE TITLE
CPU DDR3 INTERFACES

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D
REVISION 2.7.0
BRANCH
PAGE 12 OF 109
SHEET 11 OF 72





SYNC_MASTER=J11_MLB SYNC_DATE=10/18/2013

PAGE TITLE

CPU POWER

Apple Inc.

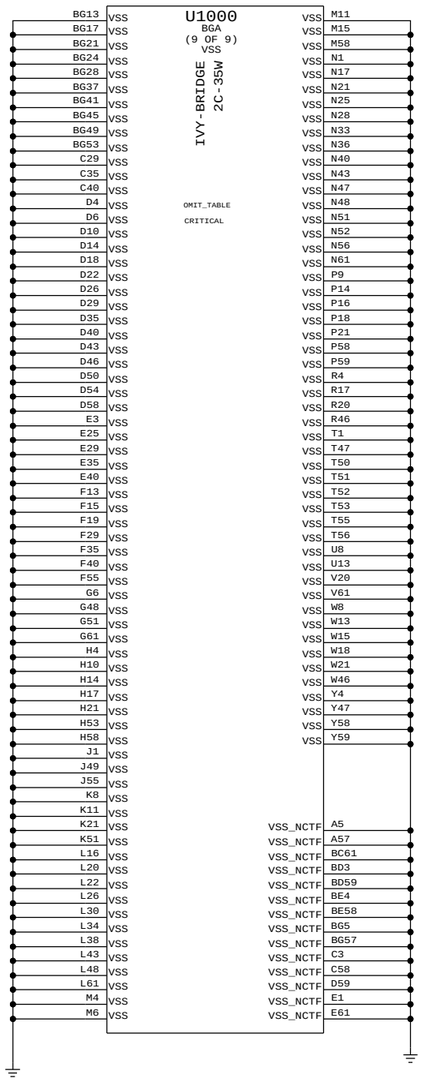
DRAWING NUMBER 051-9276 SIZE D

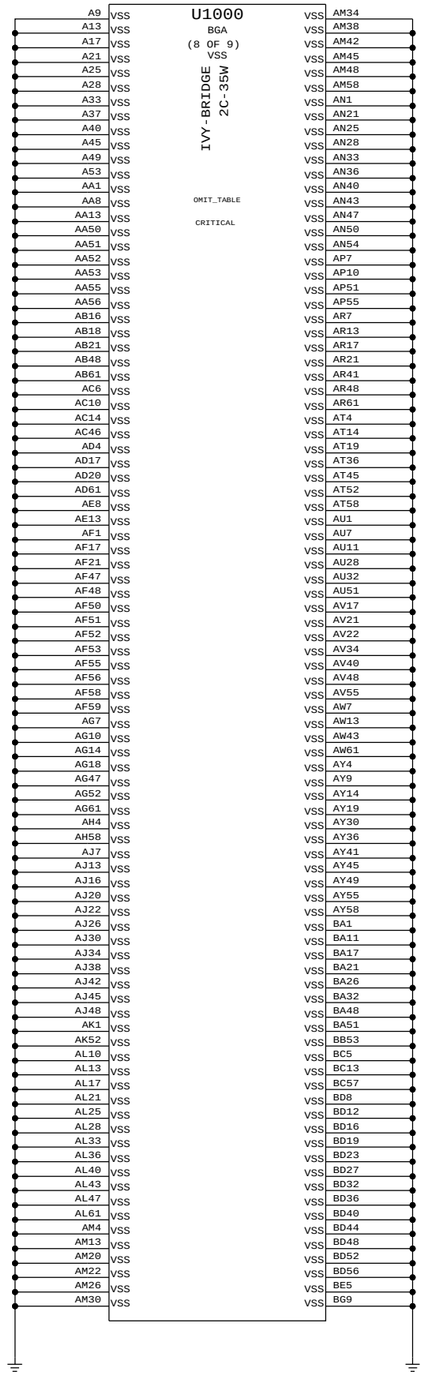
REVISION 2.7.0

BRANCH

PAGE 13 OF 109

SHEET 12 OF 72





PAGE TITLE

CPU GROUNDS

Apple Inc.

DRAWING NUMBER 051-9276

SIZE D

REVISION 2.7.0

BRANCH

PAGE 14 OF 109

SHEET 13 OF 72

All INTEL recommendations from Intel doc #4439028 Huron River Platform Power Design Guide

CPU VCORE DECOUPLING

Intel recommendation (Table 7-1): 16x 2.2uF, 12x 22uF, 3x 330uF

Processor Load Line : -2.9 mOhms

12 9 7 =PPVCORE_S0_CPU

CRITICAL
C1600 1UF 20% 6.3V X6S 0201
C1601 1UF 20% 6.3V X6S 0201
C1602 1UF 20% 6.3V X6S 0201
C1603 1UF 20% 6.3V X6S 0201
C1604 1UF 20% 6.3V X6S 0201
C1605 1UF 20% 6.3V X6S 0201
C1606 1UF 20% 6.3V X6S 0201
C1607 1UF 20% 6.3V X6S 0201
C1608 1UF 20% 6.3V X6S 0201
C1609 1UF 20% 6.3V X6S 0201
C1610 1UF 20% 6.3V X6S 0201
C1611 1UF 20% 6.3V X6S 0201
C1612 1UF 20% 6.3V X6S 0201
C1613 1UF 20% 6.3V X6S 0201
C1614 1UF 20% 6.3V X6S 0201
C1615 1UF 20% 6.3V X6S 0201
C1640 1UF 20% 6.3V X6S 0201
C1641 1UF 20% 6.3V X6S 0201
C1642 1UF 20% 6.3V X6S 0201

CRITICAL
C1616 1UF 20% 6.3V X6S 0201
C1617 1UF 20% 6.3V X6S 0201
C1618 1UF 20% 6.3V X6S 0201
C1619 1UF 20% 6.3V X6S 0201
C1620 1UF 20% 6.3V X6S 0201
C1621 1UF 20% 6.3V X6S 0201
C1622 1UF 20% 6.3V X6S 0201
C1623 1UF 20% 6.3V X6S 0201
C1624 1UF 20% 6.3V X6S 0201
C1625 1UF 20% 6.3V X6S 0201
C1626 1UF 20% 6.3V X6S 0201
C1627 1UF 20% 6.3V X6S 0201
C1628 1UF 20% 6.3V X6S 0201
C1629 1UF 20% 6.3V X6S 0201
C1630 1UF 20% 6.3V X6S 0201
C1631 1UF 20% 6.3V X6S 0201
C1632 1UF 20% 6.3V X6S 0201
C1633 1UF 20% 6.3V X6S 0201
C1634 1UF 20% 6.3V X6S 0201
C1635 1UF 20% 6.3V X6S 0201
C1636 1UF 20% 6.3V X6S 0201
C1637 1UF 20% 6.3V X6S 0201
C1638 1UF 20% 6.3V X6S 0201
C1639 1UF 20% 6.3V X6S 0201

PLACEMENT_NOTE (C1655-C1666):
Place close to U1000 on top side.

CRITICAL
C1655 10UF 20% 6.3V CERM-X5R 0402-1
C1656 10UF 20% 6.3V CERM-X5R 0402-1
C1657 10UF 20% 6.3V CERM-X5R 0402-1
C1658 10UF 20% 6.3V CERM-X5R 0402-1
C1659 10UF 20% 6.3V CERM-X5R 0402-1
C1660 10UF 20% 6.3V CERM-X5R 0402-1
C1661 10UF 20% 6.3V CERM-X5R 0402-1
C1662 10UF 20% 6.3V CERM-X5R 0402-1
C1663 10UF 20% 6.3V CERM-X5R 0402-1
C1664 10UF 20% 6.3V CERM-X5R 0402-1
C1665 10UF 20% 6.3V CERM-X5R 0402-1
C1666 10UF 20% 6.3V CERM-X5R 0402-1
C1667 10UF 20% 6.3V CERM-X5R 0402-1
C1668 10UF 20% 6.3V CERM-X5R 0402-1
C1669 10UF 20% 6.3V CERM-X5R 0402-1
C1670 10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1667-C1679):

PLACEMENT_NOTE (C1640-C1645):

C1680 270UF 20% 2V TANT CASE-B2-SM
C1681 270UF 20% 2V TANT CASE-B2-SM
C1682 270UF 20% 2V TANT CASE-B2-SM
C1683 270UF 20% 2V TANT CASE-B2-SM
C1679 270UF 20% 2V TANT CASE-B2-SM

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Section 6.5): 26x 1uF, 10x 10uF, 2x 330uF

PLACEMENT_NOTE (C1684-C167F):

12 10 9 7 =PP1V05_S0_CPU_VCCIO

Place on bottom side of U1000

C1684 1UF 10% 10V X5R 402
C1685 1UF 10% 10V X5R 402
C1686 1UF 10% 10V X5R 402
C1687 1UF 10% 10V X5R 402
C1688 1UF 10% 10V X5R 402
C1689 1UF 10% 10V X5R 402
C1690 1UF 10% 10V X5R 402
C1691 1UF 10% 10V X5R 402
C1692 1UF 10% 10V X5R 402
C1693 1UF 10% 10V X5R 402
C1694 1UF 10% 10V X5R 402
C1695 1UF 10% 10V X5R 402
C1696 1UF 10% 10V X5R 402

C1697 1UF 10% 10V X5R 402
C1698 1UF 10% 10V X5R 402
C1699 1UF 10% 10V X5R 402
C169A 1UF 10% 10V X5R 402
C169B 1UF 10% 10V X5R 402
C169C 1UF 10% 10V X5R 402
C169D 1UF 10% 10V X5R 402
C169E 1UF 10% 10V X5R 402
C169F 1UF 10% 10V X5R 402
C161A 1UF 10% 10V X5R 402
C161B 1UF 10% 10V X5R 402
C161C 1UF 10% 10V X5R 402
C161D 1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1672-C1681):

Place near U1000 on bottom side

C161E 10UF 20% 6.3V CERM-X5R 0402-1
C161F 10UF 20% 6.3V CERM-X5R 0402-1
C162A 10UF 20% 6.3V CERM-X5R 0402-1
C162B 10UF 20% 6.3V CERM-X5R 0402-1
C162C 10UF 20% 6.3V CERM-X5R 0402-1
C162D 10UF 20% 6.3V CERM-X5R 0402-1
C162E 10UF 20% 6.3V CERM-X5R 0402-1
C167A 10UF 20% 6.3V CERM-X5R 0402-1
C167B 10UF 20% 6.3V CERM-X5R 0402-1
C167C 10UF 20% 6.3V CERM-X5R 0402-1

C167D 270UF 20% 2V TANT CASE-B2-SM
C167E 270UF 20% 2V TANT CASE-B2-SM
C167G 270UF 20% 2V TANT CASE-B2-SM
C167H 270UF 20% 2V TANT CASE-B2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1601 0.010 1% 1/4W MF 0603
=PP1V05_S0_CPU_VCCPQE 7 12
C167F 1UF 10% 10V X5R 402
Note:The smallest 10mOhm available in the library are 0805s

CPU VCCPLL DECOUPLING

Intel recommendation (section 6.4): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):

Place near U1000 on top side

7 =PP1V8_S0_CPU_VCCPLL
R1600 0 5% 1/10W MF-LF 402
=PP1V8_S0_CPU_VCCPLL_R 7 12
C160X 1UF 10% 10V X5R 402
C160Y 1UF 10% 10V X5R 402
C160Z 270UF 20% 2V TANT CASE-B2-SM

PLACE_NEAR=U1000.B8:2.54 mm:NO_VIA
PLACE_NEAR=U1000.B8:2.54 mm:NO_VIA

CPU VCCPLL Low pass filter

SYNC_MASTER=J13_MLB SYNC_DATE=08/16/2012

PAGE TITLE
CPU DECOUPLING-I

Apple Inc.

DRAWING NUMBER 051-9276
SIZE D
REVISION 2.7.0
BRANCH
PAGE 16 OF 109
SHEET 14 OF 72

VAXG DECOUPLING

Graphics Load Line : -3.9 mOhms

Intel recommendation (section 6.3): 18x 1uF(9 no-stuff), 10x 104F(2 no-stuff), 8x 22uF(2 no stuff), 4x 470uF(2 no-stuff)

12 9 7 =PPVCORE_S0_CPU_VCCAXG

PLACEMENT_NOTE (C1700-C1710):

Place on bottom side of U1000

CRITICAL

C1700 1UF 10% 10V X5R 402
C1701 1UF 10% 10V X5R 402
C1702 1UF 10% 10V X5R 402
C1703 1UF 10% 10V X5R 402
C1704 1UF 10% 10V X5R 402
C1705 1UF 10% 10V X5R 402
C1706 1UF 10% 10V X5R 402
C1707 1UF 10% 10V X5R 402
C1708 1UF 10% 10V X5R 402
C1709 1UF 10% 10V X5R 402
C1710 1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1711-C1716):

CRITICAL

C1711 10UF 20% 6.3V CERM-X5R 0402-1
C1712 10UF 20% 6.3V CERM-X5R 0402-1
C1713 10UF 20% 6.3V CERM-X5R 0402-1
C1714 10UF 20% 6.3V CERM-X5R 0402-1
C1715 10UF 20% 6.3V CERM-X5R 0402-1
C1716 10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1717-C1722):

CRITICAL, AXG_ACOUSTICS:NO

C1717 22UF 20% 6.3V X5R-CERM1 0603
C1718 22UF 20% 6.3V X5R-CERM1 0603
C1719 22UF 20% 6.3V X5R-CERM1 0603
C1720 22UF 20% 6.3V X5R-CERM1 0603
C1721 22UF 20% 6.3V X5R-CERM1 0603
C1722 22UF 20% 6.3V X5R-CERM1 0603

CRITICAL, AXG_ACOUSTICS:YES

C1727 22UF 20% 4V X5R 402
C1728 22UF 20% 4V X5R 402
C1729 22UF 20% 4V X5R 402
C1730 22UF 20% 4V X5R 402
C1731 22UF 20% 4V X5R 402
C1732 22UF 20% 4V X5R 402

PLACEMENT_NOTE (C1723-C1724):

C1723 270UF 20% 2V TANT CASE-B2-SM
C1724 270UF 20% 2V TANT CASE-B2-SM
C1725 270UF 20% 2V TANT CASE-B2-SM

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation (Section 6.13): 10x 1uF, 8x 10uF, 1x 330uF

26 12 10 7 =PP1V5_S3_CPU_VCCDDR

PLACEMENT_NOTE (C1738-C1747):

Place on bottom side of U1000

C1738 1UF 10% 10V X5R 402
C1739 1UF 10% 10V X5R 402
C1740 1UF 10% 10V X5R 402
C1741 1UF 10% 10V X5R 402
C1742 1UF 10% 10V X5R 402
C1743 1UF 10% 10V X5R 402
C1744 1UF 10% 10V X5R 402
C1745 1UF 10% 10V X5R 402
C1746 1UF 10% 10V X5R 402
C1747 1UF 10% 10V X5R 402

Place close to U1000 on bottom side

C1748 10UF 20% 6.3V CERM-X5R 0402-1
C1749 10UF 20% 6.3V CERM-X5R 0402-1
C1750 10UF 20% 6.3V CERM-X5R 0402-1
C1751 10UF 20% 6.3V CERM-X5R 0402-1
C1752 10UF 20% 6.3V CERM-X5R 0402-1
C1753 10UF 20% 6.3V CERM-X5R 0402-1
C1754 10UF 20% 6.3V CERM-X5R 0402-1
C1755 10UF 20% 6.3V CERM-X5R 0402-1

C1756 270UF 20% 2V TANT CASE-B2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1702 0.010 1% 1/4W MF 0603

=PP1V5_S3_CPU_VCCDQ 7 12

C1757 1UF 10% 10V X5R 402

CPU VCCSA DECOUPLING

Intel recommendation (Section 6.6): 3x 1uf, 3x 10uf, 1x 330uf

PLACEMENT_NOTE (C1758-C1762):

12 7 =PPVCCSA_S0_CPU

Place on bottom side of U1000

C1758 1UF 10% 10V X5R 402
C1759 1UF 10% 10V X5R 402
C1760 1UF 10% 10V X5R 402
C1761 1UF 10% 10V X5R 402
C1762 1UF 10% 10V X5R 402

C1763 10UF 20% 6.3V CERM-X5R 0402-1
C1764 10UF 20% 6.3V CERM-X5R 0402-1
C1765 10UF 20% 6.3V CERM-X5R 0402-1
C1766 10UF 20% 6.3V CERM-X5R 0402-1
C1767 10UF 20% 6.3V CERM-X5R 0402-1

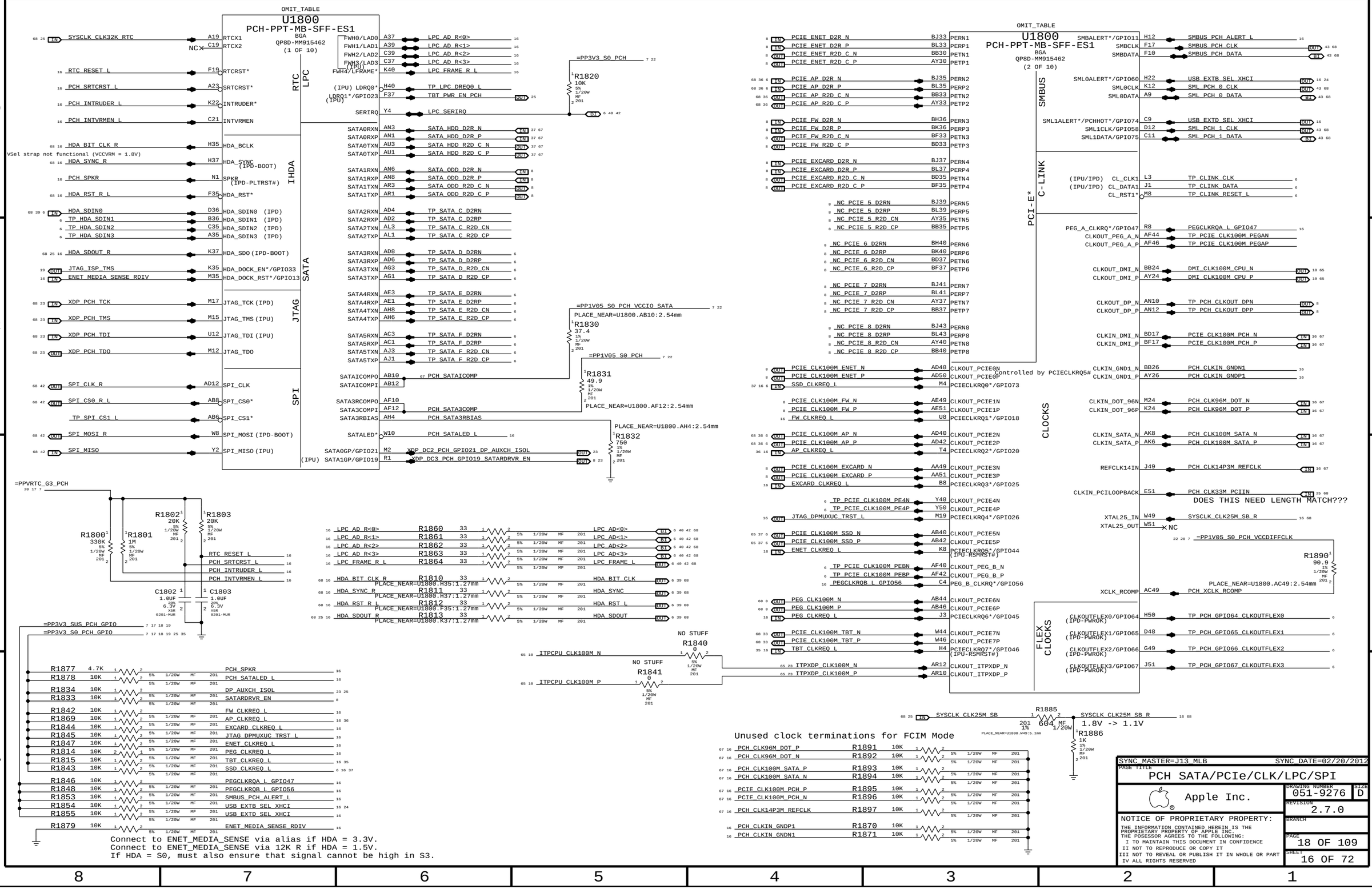
C1768 270UF 20% 2V TANT CASE-B2-SM

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE: CPU DECOUPLING-II

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D
REVISION 2.7.0
BRANCH
PAGE 17 OF 109
SHEET 15 OF 72


OMIT_TABLE
U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(1 OF 10)
RTC
LPC
IHDA
SATA
JTAG
SPI
SYSCLK_CLK32K_RTC
RTCX1
RTCX2
NC
RTC_RESET_L
RTCRST*
PCH_SRTCRST_L
SRTCRST*
PCH_INTRUDER_L
INTRUDER*
PCH_INTVRMEN_L
INTVRMEN
HDA_BIT_CLK_R
HDA_BCLK
VSel strap not functional (VCCVRM = 1.8V)
HDA_SYNC_R
HDA_SYNC (IPD-BOOT)
PCH_SPKR
SPKR (IPD-PLTRST#)
HDA_RST_R_L
HDA_RST*
HDA_SDIN0
HDA_SDIN0 (IPD)
TP_HDA_SDIN1
HDA_SDIN1 (IPD)
TP_HDA_SDIN2
HDA_SDIN2 (IPD)
TP_HDA_SDIN3
HDA_SDIN3 (IPD)
HDA_SDOUT_R
HDA_SDO (IPD-BOOT)
JTAG_ISP_TMS
HDA_DOCK_EN*/GPIO33
ENET_MEDIA_SENSE_RDIV
HDA_DOCK_RST*/GPIO13
XDP_PCH_TCK
JTAG_TCK (IPD)
XDP_PCH_TMS
JTAG_TMS (IPU)
XDP_PCH_TDI
JTAG_TDI (IPU)
XDP_PCH_TDO
JTAG_TDO
SPI_CLK_R
SPI_CLK
SPI_CS0_R_L
SPI_CS0*
TP_SPI_CS1_L
SPI_CS1*
SPI_MOSI_R
SPI_MOSI (IPD-BOOT)
SPI_MISO
SPI_MISO (IPU)
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME*
LPC_AD_R<0>
LPC_AD_R<1>
LPC_AD_R<2>
LPC_AD_R<3>
LPC_FRAME_R_L
(IPU) LDRQ0*
LDRQ1*/GPIO23 (IPU)
TP_LPC_DREQ0_L
TBT_PWR_EN_PCH
SERIRQ
LPC_SERIRQ
=PP3V3_S0_PCH
R1820 10K 5% 1/20W MF 201
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA_HDD_D2R_N
SATA_HDD_D2R_P
SATA_HDD_R2D_C_N
SATA_HDD_R2D_C_P
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA_ODD_D2R_N
SATA_ODD_D2R_P
SATA_ODD_R2D_C_N
SATA_ODD_R2D_C_P
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
TP_SATA_C_D2RN
TP_SATA_C_D2RP
TP_SATA_C_R2D_CN
TP_SATA_C_R2D_CP
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
TP_SATA_D_D2RN
TP_SATA_D_D2RP
TP_SATA_D_R2D_CN
TP_SATA_D_R2D_CP
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
TP_SATA_E_D2RN
TP_SATA_E_D2RP
TP_SATA_E_R2D_CN
TP_SATA_E_R2D_CP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
TP_SATA_F_D2RN
TP_SATA_F_D2RP
TP_SATA_F_R2D_CN
TP_SATA_F_R2D_CP
=PP1V05_S0_PCH_VCCIO_SATA
PLACE_NEAR=U1800.AB10:2.54mm
R1830 37.4 1% 1/20W MF 201
=PP1V05_S0_PCH
R1831 49.9 1% 1/20W MF 201
PLACE_NEAR=U1800.AF12:2.54mm
SATA0COMPO
SATA0COMPI
PCH_SATA0COMP
SATA3RCOMPO
SATA3COMPI
SATA3RBIAS
PCH_SATA3COMP
PCH_SATA3RBIAS
PLACE_NEAR=U1800.AH4:2.54mm
R1832 750 1% 1/20W MF 201
SATALED*
PCH_SATALED_L
SATA0GP/GPIO21
SATA1GP/GPIO19 (IPU)
XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL
XDP_DC3_PCH_GPIO19_SATARDRVR_EN
=PPVRTC_G3_PCH
R1800 330K 5% 1/20W MF 201
R1801 1M 5% 1/20W MF 201
R1802 20K 5% 1/20W MF 201
R1803 20K 5% 1/20W MF 201
C1802 1.0UF 20% 6.3V X5R 0201-MUR
C1803 1.0UF 20% 6.3V X5R 0201-MUR
R1860 33
R1861 33
R1862 33
R1863 33
R1864 33
R1810 33
R1811 33
R1812 33
R1813 33
HDA_BIT_CLK_R
HDA_SYNC_R
HDA_RST_R_L
HDA_SDOUT_R
PLACE_NEAR=U1800.H35:1.27mm
PLACE_NEAR=U1800.R37:1.27mm
PLACE_NEAR=U1800.F35:1.27mm
PLACE_NEAR=U1800.K37:1.27mm
=PP3V3_SUS_PCH_GPIO
=PP3V3_S0_PCH_GPIO
R1877 4.7K PCH_SPKR
R1878 10K PCH_SATALED_L
R1834 10K DP_AUXCH_ISOL
R1833 10K SATARDRVR_EN
R1842 10K FW_CLKREQ_L
R1869 10K AP_CLKREQ_L
R1844 10K EXCARD_CLKREQ_L
R1845 10K JTAG_DPMUXUC_TRST_L
R1847 10K ENET_CLKREQ_L
R1814 10K PEG_CLKREQ_L
R1815 10K TBT_CLKREQ_L
R1843 10K SSD_CLKREQ_L
R1846 10K PEGCLKRQA_L_GPIO47
R1848 10K PEGCLKRQB_L_GPIO56
R1853 10K SMBUS_PCH_ALERT_L
R1854 10K USB_EXTB_SEL_XHCI
R1855 10K USB_EXTD_SEL_XHCI
R1879 10K ENET_MEDIA_SENSE_RDIV
Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.
NO STUFF
R1840 0
R1841 0
ITPCPU_CLK100M_N
ITPCPU_CLK100M_P
OMIT_TABLE
U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(2 OF 10)
PCI-E*
SMBUS
C-LINK
CLOCKS
FLEX CLOCKS
PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_N
PCIE_ENET_R2D_C_P
PCIE_AP_D2R_N
PCIE_AP_D2R_P
PCIE_AP_R2D_C_N
PCIE_AP_R2D_C_P
PCIE_FW_D2R_N
PCIE_FW_D2R_P
PCIE_FW_R2D_C_N
PCIE_FW_R2D_C_P
PCIE_EXCARD_D2R_N
PCIE_EXCARD_D2R_P
PCIE_EXCARD_R2D_C_N
PCIE_EXCARD_R2D_C_P
NC_PCIE_5_D2RN
NC_PCIE_5_D2RP
NC_PCIE_5_R2D_CN
NC_PCIE_5_R2D_CP
NC_PCIE_6_D2RN
NC_PCIE_6_D2RP
NC_PCIE_6_R2D_CN
NC_PCIE_6_R2D_CP
NC_PCIE_7_D2RN
NC_PCIE_7_D2RP
NC_PCIE_7_R2D_CN
NC_PCIE_7_R2D_CP
NC_PCIE_8_D2RN
NC_PCIE_8_D2RP
NC_PCIE_8_R2D_CN
NC_PCIE_8_R2D_CP
PCIE_CLK100M_ENET_N
PCIE_CLK100M_ENET_P
SSD_CLKREQ_L
PCIE_CLK100M_FW_N
PCIE_CLK100M_FW_P
FW_CLKREQ_L
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
AP_CLKREQ_L
PCIE_CLK100M_EXCARD_N
PCIE_CLK100M_EXCARD_P
EXCARD_CLKREQ_L
TP_PCIE_CLK100M_PE4N
TP_PCIE_CLK100M_PE4P
JTAG_DPMUXUC_TRST_L
PCIE_CLK100M_SSD_N
PCIE_CLK100M_SSD_P
ENET_CLKREQ_L
TP_PCIE_CLK100M_PEBN
TP_PCIE_CLK100M_PEBP
PEGCLKRQB_L_GPIO56
PEG_CLK100M_N
PEG_CLK100M_P
PEG_CLKREQ_L
PCIE_CLK100M_TBT_N
PCIE_CLK100M_TBT_P
TBT_CLKREQ_L
ITPXDP_CLK100M_N
ITPXDP_CLK100M_P
PERN1
PERP1
PETN1
PETP1
PERN2
PERP2
PETN2
PETP2
PERN3
PERP3
PETN3
PETP3
PERN4
PERP4
PETN4
PETP4
PERN5
PERP5
PETN5
PETP5
PERN6
PERP6
PETN6
PETP6
PERN7
PERP7
PETN7
PETP7
PERN8
PERP8
PETN8
PETP8
CLKOUT_PCIE0N
CLKOUT_PCIE0P
PCIECLKRQ0*/GPIO73
(controlled by PCIECLKRQ5#)
CLKOUT_PCIE1N
CLKOUT_PCIE1P
PCIECLKRQ1*/GPIO18
CLKOUT_PCIE2N
CLKOUT_PCIE2P
PCIECLKRQ2*/GPIO20
CLKOUT_PCIE3N
CLKOUT_PCIE3P
PCIECLKRQ3*/GPIO25
CLKOUT_PCIE4N
CLKOUT_PCIE4P
PCIECLKRQ4*/GPIO26
CLKOUT_PCIE5N
CLKOUT_PCIE5P
PCIECLKRQ5*/GPIO44 (IPU-RSMRST#)
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
PEG_B_CLKRQ*/GPIO56
CLKOUT_PCIE6N
CLKOUT_PCIE6P
PCIECLKRQ6*/GPIO45
CLKOUT_PCIE7N
CLKOUT_PCIE7P
PCIECLKRQ7*/GPIO46 (IPU-RSMRST#)
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
SMBALERT*/GPIO11
SMBCLK
SMBDATA
SML0ALERT*/GPIO60
SML0CLK
SML0DATA
SML1ALERT*/PCHHOT*/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
SMBUS_PCH_ALERT_L
SMBUS_PCH_CLK
SMBUS_PCH_DATA
USB_EXTB_SEL_XHCI
SML_PCH_0_CLK
SML_PCH_0_DATA
USB_EXTD_SEL_XHCI
SML_PCH_1_CLK
SML_PCH_1_DATA
(IPU/IPD) CL_CLK1
(IPU/IPD) CL_DATA1
CL_RST1*
TP_CLINK_CLK
TP_CLINK_DATA
TP_CLINK_RESET_L
PEG_A_CLKRQ*/GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
PEGCLKRQA_L_GPIO47
TP_PCIE_CLK100M_PEGAN
TP_PCIE_CLK100M_PEGAP
CLKOUT_DMI_N
CLKOUT_DMI_P
DMI_CLK100M_CPU_N
DMI_CLK100M_CPU_P
CLKOUT_DP_N
CLKOUT_DP_P
TP_PCH_CLKOUT_DPN
TP_PCH_CLKOUT_DPP
CLKIN_DMI_N
CLKIN_DMI_P
PCIE_CLK100M_PCH_N
PCIE_CLK100M_PCH_P
CLKIN_GND1_N
CLKIN_GND1_P
PCH_CLKIN_GNDN1
PCH_CLKIN_GNDP1
CLKIN_DOT_96N
CLKIN_DOT_96P
PCH_CLK96M_DOT_N
PCH_CLK96M_DOT_P
CLKIN_SATA_N
CLKIN_SATA_P
PCH_CLK100M_SATA_N
PCH_CLK100M_SATA_P
REFCLK14IN
PCH_CLK14P3M_REFCLK
CLKIN_PCILOOPBACK
PCH_CLK33M_PCIIN
DOES THIS NEED LENGTH MATCH???
XTAL25_IN
XTAL25_OUT
SYSCLK_CLK25M_SB_R
=PP1V05_S0_PCH_VCCDIFFCLK
R1890 90.9 1% 1/20W MF 201
PLACE_NEAR=U1800.AC49:2.54mm
XCLK_RCOMP
PCH_XCLK_RCOMP
CLKOUTFLEX0/GPIO64 (IPD-PWROK)
CLKOUTFLEX1/GPIO65 (IPD-PWROK)
CLKOUTFLEX2/GPIO66 (IPD-PWROK)
CLKOUTFLEX3/GPIO67 (IPD-PWROK)
TP_PCH_GPIO64_CLKOUTFLEX0
TP_PCH_GPIO65_CLKOUTFLEX1
TP_PCH_GPIO66_CLKOUTFLEX2
TP_PCH_GPIO67_CLKOUTFLEX3
SYSCLK_CLK25M_SB
R1885 604 1% MF 1/20W
PLACE_NEAR=U1800.W49:5.1mm
SYSCLK_CLK25M_SB_R
1.8V -> 1.1V
R1886 1K 1% 1/20W MF 201
Unused clock terminations for FCIM Mode
PCH_CLK96M_DOT_P R1891 10K
PCH_CLK96M_DOT_N R1892 10K
PCH_CLK100M_SATA_P R1893 10K
PCH_CLK100M_SATA_N R1894 10K
PCIE_CLK100M_PCH_P R1895 10K
PCIE_CLK100M_PCH_N R1896 10K
PCH_CLK14P3M_REFCLK R1897 10K
PCH_CLKIN_GNDP1 R1870 10K
PCH_CLKIN_GNDN1 R1871 10K
SYNC_MASTER=J13_MLB
SYNC_DATE=02/20/2012
PAGE TITLE
PCH SATA/PCIe/CLK/LPC/SPI
Apple Inc.
DRAWING NUMBER 051-9276
SIZE D
REVISION 2.7.0
BRANCH
PAGE 18 OF 109
SHEET 16 OF 72
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

=PP3V3_SUS_PCH_GPIO 7 16 17 18 19
=PP1V05_S0_PCH_VCCIO_PCIE 7

R1905 10K 5% 1/20W MF 201
R1900 49.9 1% 1/20W MF 201
PLACE_NEAR=U1800.BF19:12.7mm

OMIT_TABLE

U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(3 OF 10)

DMI FDI

65 9 IN	DMI_N2S_N<0>	BL21	DMI0RXN	FDI_RXN0	BL13	FDI_DATA_N<0>	IN 9 65
65 9 IN	DMI_N2S_N<1>	BL23	DMI1RXN	FDI_RXN1	BJ15	FDI_DATA_N<1>	IN 9 65
65 9 IN	DMI_N2S_N<2>	BJ19	DMI2RXN	FDI_RXN2	BD12	FDI_DATA_N<2>	IN 9 65
65 9 IN	DMI_N2S_N<3>	BL17	DMI3RXN	FDI_RXN3	BJ11	FDI_DATA_N<3>	IN 9 65
				FDI_RXN4	AY15	FDI_DATA_N<4>	IN 9 65
65 9 IN	DMI_N2S_P<0>	BJ21	DMI0RXP	FDI_RXN5	AY12	FDI_DATA_N<5>	IN 9 65
65 9 IN	DMI_N2S_P<1>	BJ23	DMI1RXP	FDI_RXN6	BJ9	FDI_DATA_N<6>	IN 9 65
65 9 IN	DMI_N2S_P<2>	BL19	DMI2RXP	FDI_RXN7	BF10	FDI_DATA_N<7>	IN 9 65
65 9 IN	DMI_N2S_P<3>	BJ17	DMI3RXP				
				FDI_RXP0	BJ13	FDI_DATA_P<0>	IN 9 65
65 9 OUT	DMI_S2N_N<0>	BD22	DMI0TXN	FDI_RXP1	BL15	FDI_DATA_P<1>	IN 9 65
65 9 OUT	DMI_S2N_N<1>	BB22	DMI1TXN	FDI_RXP2	BF12	FDI_DATA_P<2>	IN 9 65
65 9 OUT	DMI_S2N_N<2>	BB19	DMI2TXN	FDI_RXP3	BL11	FDI_DATA_P<3>	IN 9 65
65 9 OUT	DMI_S2N_N<3>	BB17	DMI3TXN	FDI_RXP4	BB15	FDI_DATA_P<4>	IN 9 65
				FDI_RXP5	BB12	FDI_DATA_P<5>	IN 9 65
65 9 OUT	DMI_S2N_P<0>	BF22	DMI0TXP	FDI_RXP6	BL9	FDI_DATA_P<6>	IN 9 65
65 9 OUT	DMI_S2N_P<1>	AY22	DMI1TXP	FDI_RXP7	BD10	FDI_DATA_P<7>	IN 9 65
65 9 OUT	DMI_S2N_P<2>	AY19	DMI2TXP				
65 9 OUT	DMI_S2N_P<3>	AY17	DMI3TXP	FDI_INT	BB10	FDI_INT	OUT 9 65
				FDI_FSYNC0	BH12	FDI_FSYNC<0>	OUT 9 65
PCH_DMI_COMP		BF19	DMI_ZCOMP	FDI_FSYNC1	BK8	FDI_FSYNC<1>	OUT 9 65
		BD19	DMI_IRCOMP				
				FDI_LSYNC0	BK12	FDI_LSYNC<0>	OUT 9 65
PCH_DMI2RBIAS		BK20	DMI2RBIAS	FDI_LSYNC1	BH8	FDI_LSYNC<1>	OUT 9 65

=PPVRTC_G3_PCH 7 16 20
R1915 390K 5% 1/20W MF 201

SYSTEM POWER MANAGEMENT

	DSWVRMEN	F22	PCH_DSWVRMEN	
	DPWROK	A21	PM_DSW_PWRGD	IN 40
	WAKE*	D8	PCIE_WAKE_L	IN 6 17 36
	CLKRUN*/GPIO32	T2	PM_CLKRUN_L	B/D 6 17 40 42
	SUS_STAT*/GPIO61	G6	LPC_PWRDWN_L	OUT 6 25 40 42
	SUSCLK/GPIO62	D3	PM_CLK32K_SUSCLK_R	OUT 41 68
	SLP_S5*/GPIO63	F6	PM_SLP_S5_L	OUT 17 40 61
	SLP_S4*	K10	PM_SLP_S4_L	OUT 17 26 36 40 48 61
	SLP_S3*	D4	PM_SLP_S3_L	OUT 17 26 40 61
	SLP_A*	C7	TP_PM_SLP_A_L	
	SLP_SUS*	A15	PM_SLP_SUS_L	OUT 17 61
	PMSYNCH	BB8	PM_SYNC	OUT 10 65
	SLP_LAN*/GPIO29	A7	MEM_VDD_SEL_1V5_L	OUT 17 55

R1909 100K 5% 1/20W MF 201

R1920 750 1% 1/20W MF 201
PLACE_NEAR=U1800.BK20:2.54mm

17 PCH_SUSACK_L	F15	SUSACK*(IPU)		
40 25 IN PM_SYSRST_L	L1	SYS_RESET*		
40 25 23 IN PM_PCH_SYS_PWROK	M10	SYS_PWROK		
25 IN PM_PCH_PWROK	M22	PWROK		
25 IN PM_PCH_APWROK	G3	APWROK		
65 26 10 OUT PM_MEM_PWRGD	B12	DRAMPWROK		
61 IN PM_RSMRST_L	B20	RSMRST*		
17 PCH_SUSWARN_L	C13	SUSWARN*/SUSPWRDNACK/GPIO30		
40 23 17 IN PM_PWRBTN_L	K19	PWRBTN*(IPU)		
61 41 40 IN SMC_ADAPTER_EN	H19	ACPRESENT/GPIO31 (IPD-DeepS4/S5)		
41 IN PM_BATLOW_L	H10	BATLOW*/GPIO72 (IPU)		
PCH_RI_L	F12	RI*		

R1955 100K 5% 1/20W MF 201
8 OUT LVDS_IG_BKL_ON
8 OUT LVDS_IG_PANEL_PWR
8 OUT LVDS_IG_BKL_PWM

OMIT_TABLE

U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(4 OF 10)

LVDS DIGITAL DISPLAY INTERFACE

M44	L_BKLTEN			
M42	L_VDD_EN			
L49	L_BKLTCTL			
NC L51	L_DDC_CLK			
NC K46	L_DDC_DATA (IPD-PLTRST#)			
NC R42	L_CTRL_CLK			
NC M40	L_CTRL_DATA			
NC AH42	LVD_IBG			
NC AH40	LVD_VBG			
NC AG51	LVD_VREFH			
NC AG49	LVD_VREFL			
NC AK44	LVDSA_CLK*			
NC AK46	LVDSA_CLK			
NC AR46	LVDSA_DATA0*			
NC AN49	LVDSA_DATA1*			
NC AN44	LVDSA_DATA2*			
NC AK40	LVDSA_DATA3*			
NC AR44	LVDSA_DATA0			
NC AN51	LVDSA_DATA1			
NC AN46	LVDSA_DATA2			
NC AK42	LVDSA_DATA3			
AH46	LVDSB_CLK*			
AH44	LVDSB_CLK			
NC AM50	LVDSB_DATA0*			
NC AL49	LVDSB_DATA1*			
NC AJ51	LVDSB_DATA2*			
NC AH50	LVDSB_DATA3*			
NC AM48	LVDSB_DATA0			
NC AL51	LVDSB_DATA1			
NC AJ49	LVDSB_DATA2			
NC AH48	LVDSB_DATA3			

CRT

6 TP_CRT_IG_BLUE	M46	CRT_BLUE		
6 TP_CRT_IG_GREEN	R46	CRT_GREEN		
6 TP_CRT_IG_RED	U46	CRT_RED		
6 TP_CRT_IG_DDC_CLK	R49	CRT_DDC_CLK		
6 TP_CRT_IG_DDC_DATA	N49	CRT_DDC_DATA		
6 TP_CRT_IG_HSYNC	M50	CRT_HSYNC		
6 TP_CRT_IG_VSYNC	N51	CRT_VSYNC		
PCH_DAC_IREF	R51	DAC_IREF		
	T48	CRT_IRTN		

PLACE_NEAR=U1800.R51:2.54mm
R1951 1K 5% 1/20W MF 201

	SDVO_TVCLKINN (IPD)	AU40	TP_SDVO_TVCLKINN	6
	SDVO_TVCLKINP (IPD)	AU42	TP_SDVO_TVCLKINP	6
	SDVO_STALLN (IPD)	AR51	TP_SDVO_STALLN	6
	SDVO_STALLP (IPD)	AR49	TP_SDVO_STALLP	6
	SDVO_INTN (IPD)	AT50	TP_SDVO_INTN	6
	SDVO_INTP (IPD)	AT48	TP_SDVO_INTP	6
	SDVO_CTRLCLK	W42	DPA_IG_DDC_CLK	8
	SDVO_CTRLDATA (IPD-PLTRST#)	R44	DPA_IG_DDC_DATA	8
	DDPB_AUXN	AW51	DPA_IG_AUX_CH_N	8
	DDPB_AUXP	AW49	DPA_IG_AUX_CH_P	8
	DDPB_HPD	AY42	DPA_IG_HPD	8
	DDPB_0N	AY48	TP_DP_IG_B_MLN<0>	8
	DDPB_0P	AY50	TP_DP_IG_B_MLP<0>	8
	DDPB_1N	AY44	TP_DP_IG_B_MLN<1>	8
	DDPB_1P	AY46	TP_DP_IG_B_MLP<1>	8
	DDPB_2N	BB44	TP_DP_IG_B_MLN<2>	8
	DDPB_2P	BB46	TP_DP_IG_B_MLP<2>	8
	DDPB_3N	BA49	TP_DP_IG_B_MLN<3>	8
	DDPB_3P	BA51	TP_DP_IG_B_MLP<3>	8
	DDPC_CTRLCLK	T50	DPB_IG_DDC_CLK	8
	DDPC_CTRLDATA (IPD-PLTRST#)	U44	DPB_IG_DDC_DATA	8
	DDPC_AUXN	AU51	DPB_IG_AUX_CH_N	8
	DDPC_AUXP	AU49	DPB_IG_AUX_CH_P	8
	DDPC_HPD	BE46	DPB_IG_HPD	8
	DDPC_0N	BC49	TP_DP_IG_C_MLN<0>	8
	DDPC_0P	BC51	TP_DP_IG_C_MLP<0>	8
	DDPC_1N	BD48	TP_DP_IG_C_MLN<1>	8
	DDPC_1P	BD50	TP_DP_IG_C_MLP<1>	8
	DDPC_2N	BF46	TP_DP_IG_C_MLN<2>	8
	DDPC_2P	BF45	TP_DP_IG_C_MLP<2>	8
	DDPC_3N	BE49	TP_DP_IG_C_MLN<3>	8
	DDPC_3P	BE51	TP_DP_IG_C_MLP<3>	8
	DDPD_CTRLCLK	M48	TP_DP_IG_D_CTRL_CLK	8
	DDPD_CTRLDATA (IPD-PLTRST#)	U42	TP_DP_IG_D_CTRL_DATA	8
	DDPD_AUXN	AU46	TP_DP_IG_D_AUXN	
	DDPD_AUXP	AU44	TP_DP_IG_D_AUXP	
	DDPD_HPD	BK44	TP_DP_IG_D_HPD	8
	DDPD_0N	BG51	TP_DP_IG_D_MLN<0>	
	DDPD_0P	BG49	TP_DP_IG_D_MLP<0>	
	DDPD_1N	BF42	TP_DP_IG_D_MLN<1>	
	DDPD_1P	BD42	TP_DP_IG_D_MLP<1>	
	DDPD_2N	BJ47	TP_DP_IG_D_MLN<2>	
	DDPD_2P	BL47	TP_DP_IG_D_MLP<2>	
	DDPD_3N	BL45	TP_DP_IG_D_MLN<3>	
	DDPD_3P	BJ45	TP_DP_IG_D_MLP<3>	

19 18 17 16 7 =PP3V3_SUS_PCH_GPIO
R1983 10K 5% 1/20W MF 201
R1986 0 5% 1/20W MF 201
17 PCH_SUSWARN_L — PCH_SUSACK_L 17

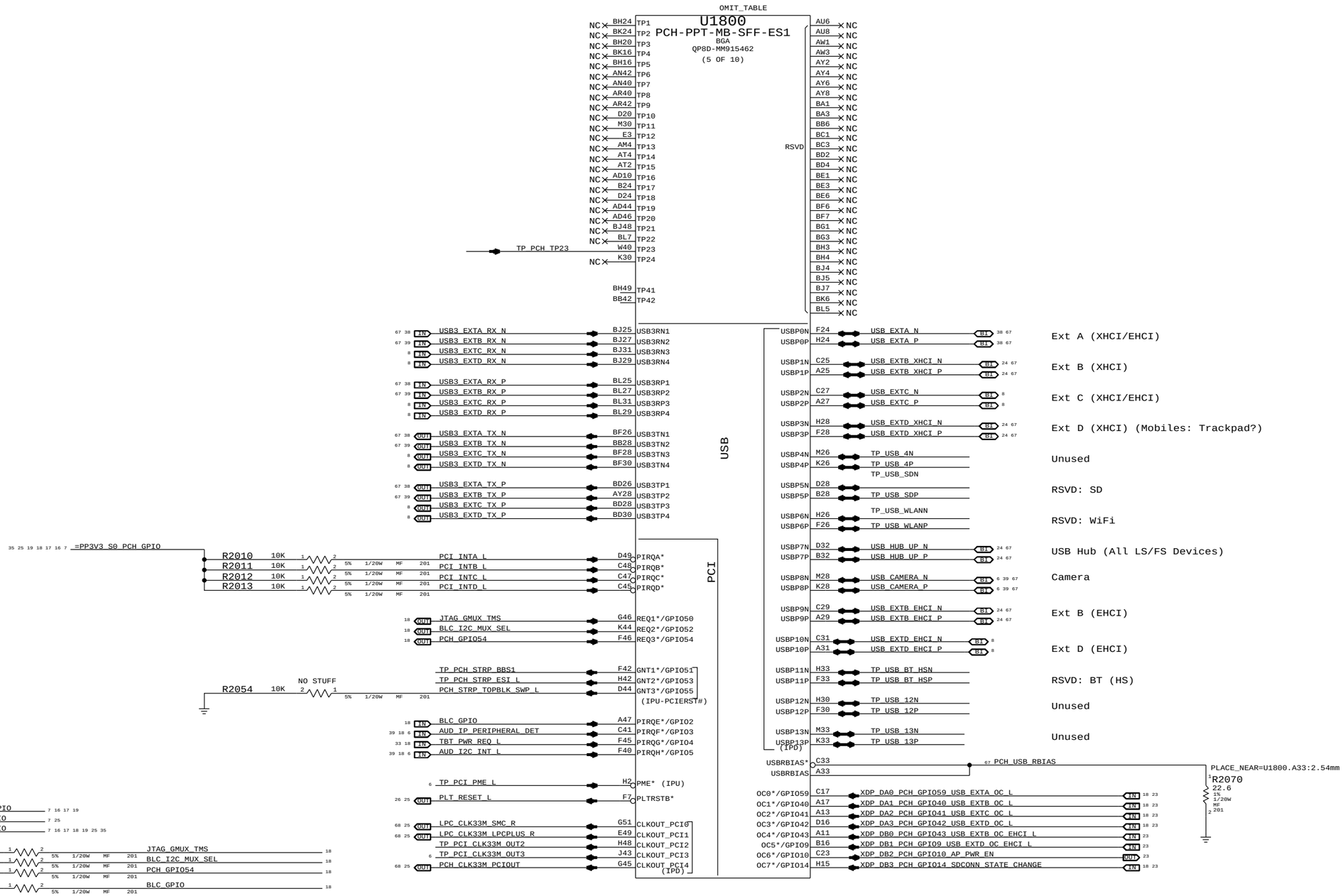
=PP3V3_SUS_PCH_GPIO 7 16 17 18 19
=PP3V3_S0_PCH_GPIO 7 16 18 19 25 35
=PP3V3_S5_PCH 7

R1985	1K	PM_PWRBTN_L	17 23 40
R1991	8.2K	PM_CLKRUN_L	6 17 40 42
R1982	10K	MEM_VDD_SEL_1V5_L	17 55
R1925	1K	PCIE_WAKE_L	6 17 36
R1924	100K	PM_SLP_S3_L	17 26 40 61
R1921	100K	PM_SLP_S4_L	17 26 36 40 48 61
R1922	100K	PM_SLP_S5_L	17 40 61
R1923	100K	PM_SLP_SUS_L	17 61

All: 5% 1/20W MF 201

SYNC_MASTER=J13_MLB SYNC_DATE=10/06/2011
PAGE TITLE
PCH DMI/FDI/PM/Graphics
Apple Inc.
DRAWING NUMBER 051-9276
SIZE D
REVISION 2.7.0
BRANCH
PAGE 19 OF 109
SHEET 17 OF 72

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=J13_MLB	SYNC_DATE=09/22/2011
PAGE TITLE: PCH PCI/USB/TP/RSVD	
Apple Inc.	DRAWING NUMBER: 051-9276 · SIZE: D
	REVISION: 2.7.0
	BRANCH:
	PAGE: 20 OF 109
	SHEET: 18 OF 72

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.

=PP3V3_S0_PCH_GPIO

RAMCFG3:H R2172 10K 5% 1/20W MF 201
RAMCFG2:H R2173 10K 5% 1/20W MF 201
RAMCFG1:H R2174 10K 5% 1/20W MF 201
RAMCFG0:H R2175 10K 5% 1/20W MF 201

OMIT_TABLE

U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(6 OF 10)

(TBT_CIO_PLUG_EVENT_ISOL)

XDP_FC1_PCH_GPIO0	W1	BMBUSY*/GPIO0	
FW_PME_L	B40	GPIO1	
DPMUX_UC_IRQ	C43	GPIO6	
SMC_RUNTIME_SCI_L	A45	GPIO7	
TP_PCH_GPIO8	H17	GPIO8 (IPU-RSMRST#)	
WOL_EN	C5	LAN_PHY_PWR_CTRL/GPIO12	
XDP_FC0_PCH_GPIO15	K6	GPIO15 (IPU)	
XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH	AA3	SATA4GP/GPIO16	
LPCPLUS_GPIO	B44	GPIO17	
ODD_PWR_EN_L	W3	SCLOCK/GPIO22	
TBT_GO2SX_BIDIR	K15	GPIO24	
SMC_WAKE_SCI_L	C15	GPIO27 (IPU-DeepS4/S5)	
XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L	G1	GPIO28 (IPU-RSMRST#)	
TBT_SW_RESET_R_L	R3	STP_PCI*/GPIO34	
XDP_DC1_PCH_GPIO35_MXM_GOOD	W12	GPIO35	
XDP_DD0_PCH_GPIO36_DP_GPU_TBT_SEL	W6	SATA2GP/GPIO36	
XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK	M6	SATA3GP/GPIO37 (IPD-PLTRST#)	
JTAG_ISP_TDO	N3	SLOAD/GPIO38	
JTAG_ISP_TDI	U10	SDATAOUT0/GPIO39	
FW_PWR_EN_PCH	U1	SDATAOUT1/GPIO48	
XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH	AA1	SATA5GP/GPIO49	
SPIROM_USE_MLB	K17	GPIO57	

GPIO CPU/MISC

	K42	GPIO68	MLB_RAMCFG3
	A43	GPIO69	MLB_RAMCFG2
	D40	GPIO70	MLB_RAMCFG1
	A41	GPIO71	MLB_RAMCFG0
PCH_A20GATE	U3	A20GATE	
PCH_PECI	AU12	(IPD)PECI	
PCH_RCIN_L	U6	RCIN*	
PCH_PROCPWRGD	AU10	PROCPWRGD	
PM_THRMTRIP_L_R	BC9	THRMTRIP*	
PCH_INIT3V3_L	R6	INIT3_3V* (IPU)	
PCH_DF_TVS	BC7	DF_TVS (IPD-PLTRST#7)	
	AK10	TS_VSS1	
	AH12	TS_VSS2	
	AK12	TS_VSS3	
	AH10	TS_VSS4	
	U40	NC_1	NC

NCTF

	A4	VSS_NCTF	
	A5		
	A48		
	A49		
	A51		
	BH1		
	BH51		
	BJ1		
	BJ3		
	BJ49		
	BJ51		
	BL1		
	BL3		
	BL4		
	BL48	VSS_NCTF	
	BL49		
	BL51		
	C3		
	C49		
	C51		
	D1		
	D51		
	E1		

TBT_SW_RESET_L → R2180 0 5% 1/20W MF 201 → TBT_SW_RESET_R_L

NO STUFF
R2130 1K 5% 1/20W MF 201
This has internal pull up and should not pulled low.
THIS SIGNAL IS INTENDED FOR FIRMWARE HUB AND WE ARE NOT USING IT.

R2170 43 5% 1/20W MF 201 — NO STUFF — PCH_PECI → CPU_PECI
R2140 0 5% 1/20W MF 201 — PCH_PROCPWRGD → CPU_PWRGD
R2156 390 5% 1/20W MF 201 — PM_THRMTRIP_L_R → PM_THRMTRIP_L

=PP1V8_S0_PCH_VCC_DFTERM
R2179 2.2K 5% 1/20W MF 201
R2178 1K 5% 1/20W MF 201 — CPU_PROC_SEL_L
DF_TVS:DMI & FDI Term Voltage
Set to Vss when Low
Set to Vcc when High

=PP3V3_S5_PCH_GPIO
=PP3V3_SUS_PCH_GPIO
=PP3V3_S0_PCH_GPIO

Stuff R2160 or R2574, not both
NO STUFF
Must stuff R2197 when R2180 NO STUFFed.

R2160	10K	XDP_FC1_PCH_GPIO0
R2185	10K	FW_PME_L
R2196	10K	SMC_RUNTIME_SCI_L
R2190	100K	LPCPLUS_GPIO
R2197	10K	TBT_SW_RESET_R_L
R2184	10K	FW_PWR_EN_PCH
R2150	10K	PCH_A20GATE
R2155	10K	PCH_RCIN_L
R2194	10K	WOL_EN
R2192	10K	TBT_GO2SX_BIDIR
R2193	100K	SPIROM_USE_MLB
R2191	10K	SMC_WAKE_SCI_L
R2111	20K	DPMUX_UC_IRQ
R2195	100K	AUD_IPHS_SWITCH_EN_PCH
R2112	10K	ODD_PWR_EN_L
R2198	10K	XDP_DD0_PCH_GPIO36_DP_GPU_TBT_SEL
R2116	10K	ENET_LOW_PWR_PCH

JTAG Isolation due to glitch in and out of sleep
NOTE: TCK from PCH is Push-Pull CMOS
NOTE: TMS/TDI from PCH is Open Drain
NOTE: TDO from CR is Push-Pull CMOS

CRITICAL
Q2160 SSM6N15AFE SOT563
=PP3V3_S0_PCH_STRAPS → R2188 10K → JTAG_ISP_TMS
=PP3V3_TBT_PCH_GPIO → R2163 10K → JTAG_TBT_TMS

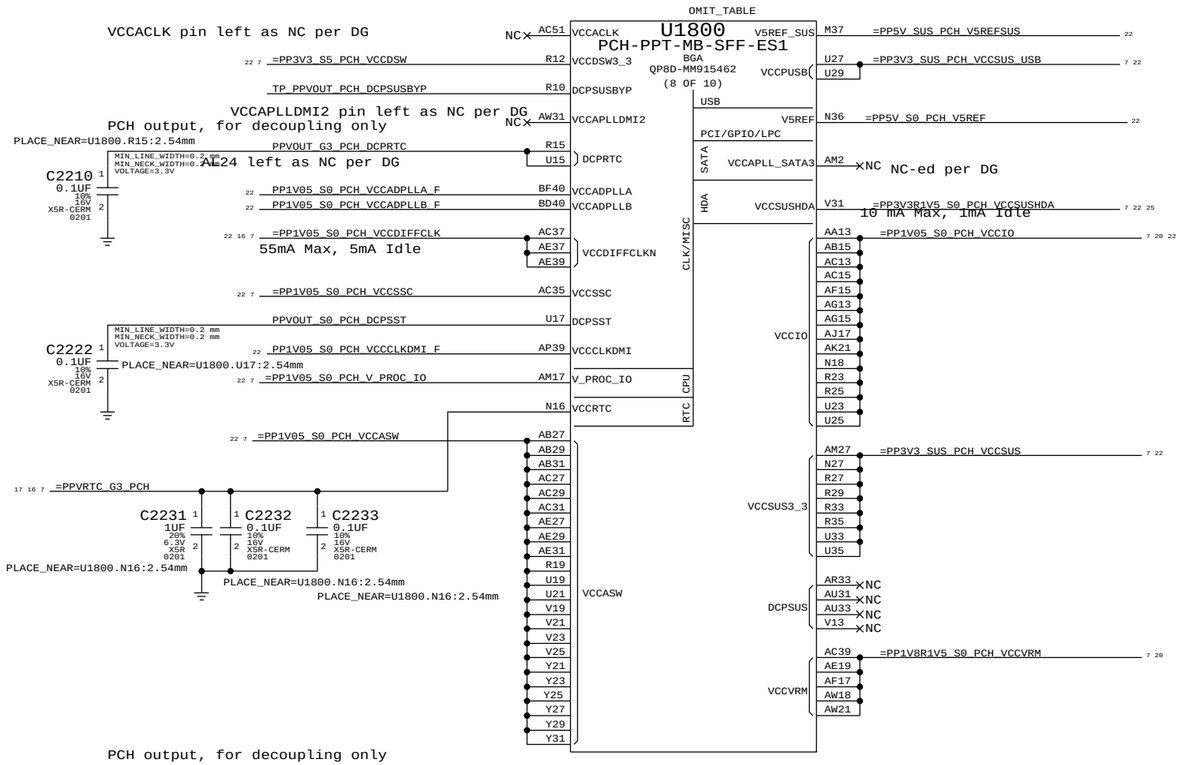
CRITICAL
Q2160 SSM6N15AFE SOT563
=PP3V3_S0_PCH_STRAPS → R2199 10K → JTAG_ISP_TDI
=PP3V3_TBT_PCH_GPIO → R2161 10K → JTAG_TBT_TDI

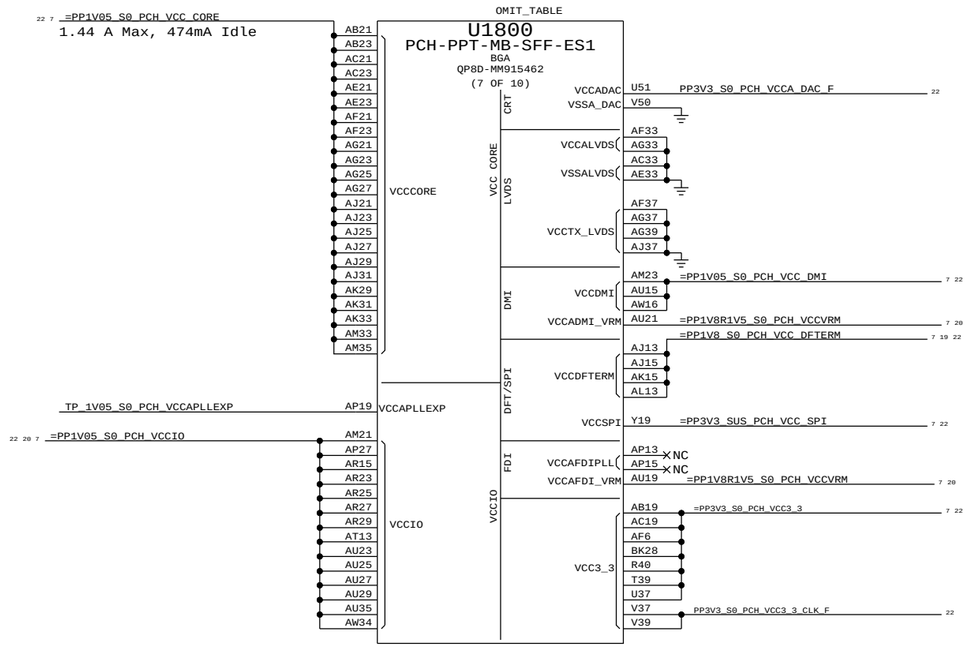
CRITICAL
Q2162 SSM3K15FV SOD-VESM-HF
=PP3V3_S0_PCH_STRAPS → R2186 10K → JTAG_ISP_TDO
=PP3V3_TBT_PCH_GPIO → R2162 10K → JTAG_TBT_TDO

=PP3V3_S0_PCH_GPIO
C2113 0.1UF 10% 16V X5R-CERM 0201
TBT_PWR_EN goes high for JTAG Programming
TBT_PWR_EN → U2100 CRITICAL 74LVC1G08 SOT891 → JTAG_TBT_TCK
JTAG_ISP_TCK
R2113 10K 5% 1/20W MF 201

=PP3V3_S0_PCH_GPIO
C2114 0.1UF 10% 16V X5R-CERM 0201
TBT_CIO_PLUG_EVENT → U2101 CRITICAL 74LVC1G08 SOT891 → TBT_CIO_PLUG_EVENT_ISOL
R2166 10K 5% 1/20W MF 201
NO STUFF R2167 10K 5% 1/20W MF 201

SYNC_MASTER=J13_MLB	SYNC_DATE=02/23/2012
PAGE TITLE	PCH GPIO/MISC/NCTF
Apple Inc.	DRAWING NUMBER 051-9276 · SIZE D
	REVISION 2.7.0
	BRANCH
	PAGE 21 OF 109
	SHEET 19 OF 72





SYNC_MASTER=J13_MLB	SYNC_DATE=09/22/2011
PAGE TITLE	PCH POWER
Apple Inc.	DRAWING NUMBER 051-9276 · SIZE D
	REVISION 2.7.0
	BRANCH
	PAGE 22 OF 109
	SHEET 20 OF 72

OMIT_TABLE

U1800

PCH-PPT-MB-SFF-ES1

BGA

QP8D-MM915462

(9 OF 10)

AA7			AP2
AA9			AP4
AA11			AP7
AA39			AP9
AA41			AP11
AA43			AP17
AA45			AP21
AB2			AP23
AB4			AP25
AB17			AP29
AB25			AP31
AB33			AP33
AB35			AP35
AB37			AP37
AB48			AP41
AB50			AP43
AC7			AP45
AC9			AP48
AC11			AP50
AC17			AR6
AC25			AR8
AC41			AR17
AC43			AR19
AC45			AR21
AE7			AR31
AE9			AR35
AE11			AR37
AE13			AT7
AE15			AT9
AE17			AT11
AE25			AT39
AE35			AT41
AE41			AT43
AE43			AT45
AE45			AU17
AF2			AU37
AF4			AV2
AF8			AV4
AF19			AV48
AF25			AV50
AF27			AW7
AF29	VSS	VSS	AW9
AF31			AW11
AF35			AW13
AF48			AW23
AF50			AW25
AG7			AW27
AG9			AW29
AG11			AW36
AG17			AW39
AG19			AW41
AG29			AW43
AG31			AW45
AG35			AY10
AG41			B6
AG43			B10
AG45			B14
AH2			B18
AJ7			B22
AJ9			B26
AJ11			B30
AJ19			B34
AJ33			B38
AJ35			B42
AJ39			B46
AJ41			BA7
AJ43			BA9
AJ45			BA11
AK2			BA13
AK4			BA16
AK17			BA18
AK19			BA21
AK23			BA23
AK25			BA25
AK27			BA27
AK35			BA29
AK37			BA31
AK48			BA34
AK50			BA36
AL7			BA39
AL9			BA41
AL11			BA43
AL39			BA45
AL41			BB2
AL43			BB4
AL45			BB48
AM15			BB50
AM19			BC11
AM25			BC13
AM29			BC16
AM31			BC18
AM37			BC21

OMIT_TABLE

U1800

PCH-PPT-MB-SFF-ES1

BGA

QP8D-MM915462

(10 OF 10)

BC23			G39
BC25			G41
BC27			G43
BC29			J7
BC31			J9
BC34			J11
BC36			J13
BC39			J16
BC41			J18
BC43			J21
BC45			J23
BD15			J25
BD24			J27
BE7			J29
BE9			J31
BE11			J34
BE13			J36
BE16			J39
BE18			J41
BE21			J45
BE23			K2
BE25			K4
BE27			K48
BE29			K50
BE31			L7
BE34			L9
BE36			L11
BE39			L13
BE41			L16
BE43			L18
BE45			L21
BF2			L23
BF4			L25
BF15			L27
BF24			L29
BF48			L31
BF50			L34
BH6			L36
BH10			L39
BH14	VSS	VSS	L41
BH18			L43
BH22			L45
BH26			N7
BH28			N9
BH30			N11
BH32			N13
BH34			N21
BH38			N23
BH42			N25
BH44			N29
BH46			N31
BH48			N34
BK10			N39
BK14			N41
BK18			N43
BK22			N45
BK26			P2
BK30			P4
BK32			P48
BK34			P50
BK38			R17
BK42			R21
BK46			R31
D6			R37
D10			T7
D14			T9
D18			T11
D22			T13
D26			T41
D30			T43
D34			T45
D38			U31
D42			U49
D46			V2
F2			V4
F4			V7
F48			V9
F50			V11
G7			V15
G9			V17
G11			V27
G13			V29
G16			V33
G18			V35
G21			V41
G23			V43
G25			V45
G27			V48
G29			Y15
G31			Y17
G34			Y33
G36			Y35
			Y37

SYNC_MASTER=J13_MLB SYNC_DATE=08/12/2011

PAGE TITLE

PCH GROUNDS

Apple Inc.

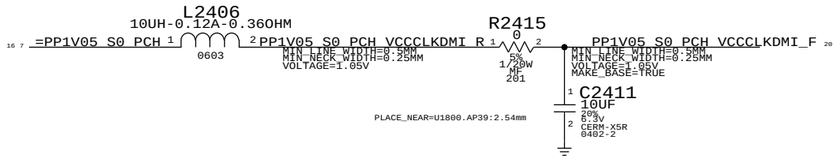
DRAWING NUMBER 051-9276 SIZE D

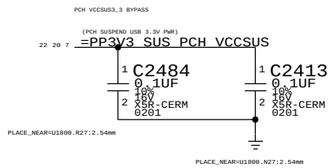
REVISION 2.7.0

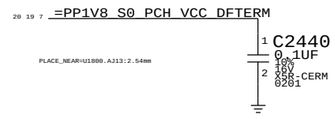
BRANCH

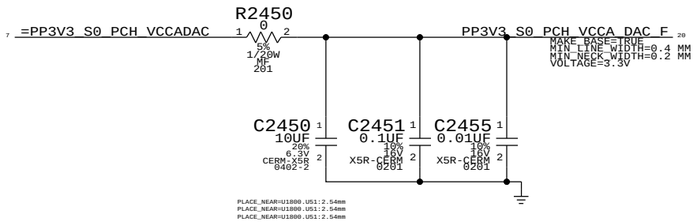
PAGE 23 OF 109

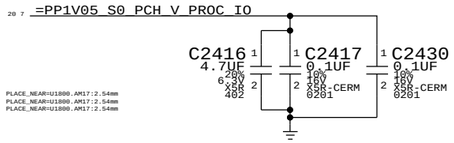
SHEET 21 OF 72

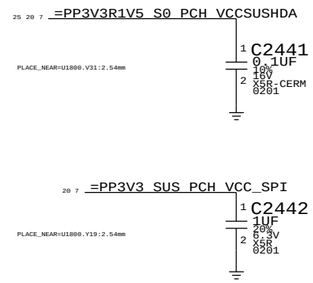


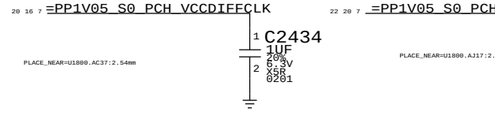


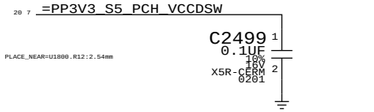


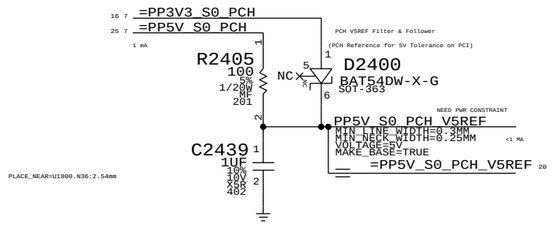


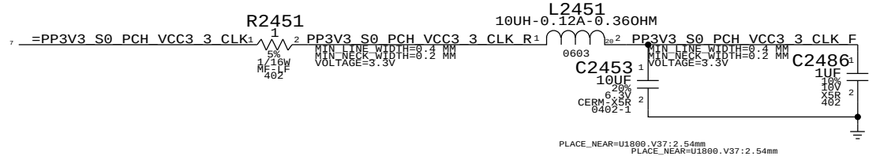


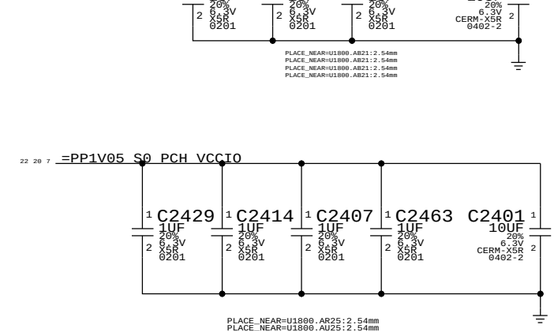


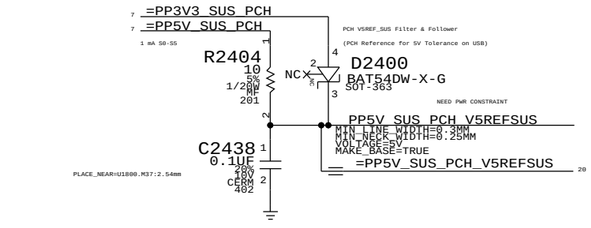


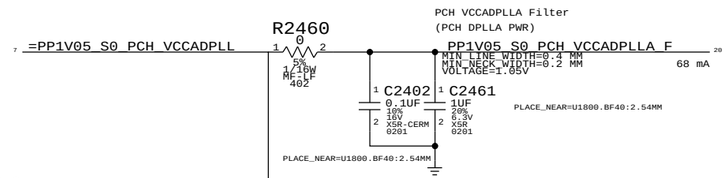


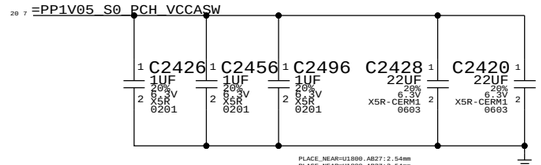


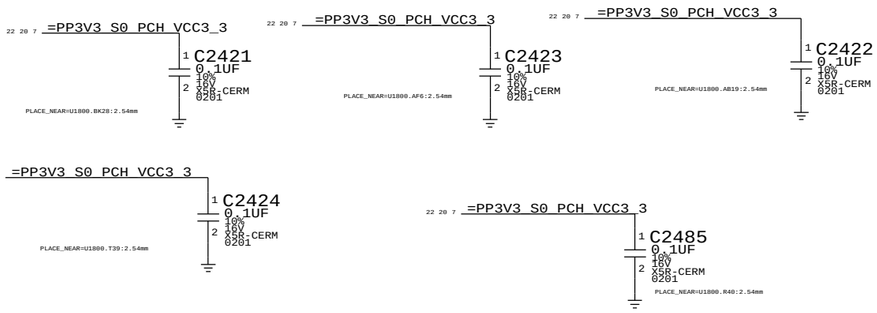












SYNC MASTER=J13_MLB SYNC_DATE=11/18/2013

PAGE TITLE
PCH DECOUPLING

Apple Inc.

DRAWING NUMBER 051-9276
SIZE D
REVISION 2.7.0
BRANCH
PAGE 24 OF 109
SHEET 22 OF 72

CPU Micro2-XDP

=PPVCCIO_S0_XDP

=PP3V3_S0_XDP
NO STUFF
R2540 1K 5% 1/16W MF-LF 402

CRITICAL
XDP_CONN
J2500
DF40RC-60DP-0.4V
M-ST-SM1

518S0847

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

XDP_CPU_PREQ_L	OBSEN_A0	OBSEN_C0	CPU_CFG<16>
XDP_CPU_PRDY_L	OBSEN_A1	OBSEN_C1	CPU_CFG<17>
XDP_BPM_L<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<0>
XDP_BPM_L<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<1>
XDP_BPM_L<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<2>
XDP_BPM_L<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<3>
CPU_CFG<10>	OBSEN_B0	OBSEN_D0	CPU_CFG<8>
CPU_CFG<11>	OBSEN_B1	OBSEN_D1	CPU_CFG<9>
XDP_OBSDATA_B<0>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<4>
XDP_OBSDATA_B<1>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<5>
XDP_OBSDATA_B<2>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<6>
XDP_OBSDATA_B<3>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<7>
XDP_CPU_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	XDP_CPU_CLK100M_P
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	XDP_CPU_CLK100M_N
XDP_CPU_CFG<0>	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_VR_READY	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
=SMBUS_XDP_SDA	SDA	TDO	XDP_CPU_TDO
=SMBUS_XDP_SCL	SCL	TRSTn	XDP_CPU_TRST_L
	TCK1	TDI	XDP_CPU_TDI
XDP_CPU_TCK	TCK0	TMS	XDP_CPU_TMS
	VCC_OBS_AB	XDP_PRESENT#	

NC

R2581 1K 1/20W 5% MF 201
R2580 1K 1/20W 5% MF 201

C2500 0.1uF 10% 16V X5R 402
C2501 0.1uF 10% 16V X5R 402

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

R2515 0 XDP_CPU_CLK100M_P — XDP PLACE_NEAR=R1841.1:2.54mm — ITPXDP_CLK100M_P
R2516 0 XDP_CPU_CLK100M_N — XDP PLACE_NEAR=R1840.1:2.54mm — ITPXDP_CLK100M_N
R2505 1K XDP_DBRESET_L — XDP PLACE_NEAR=U1000.D44:2.54mm — CPU_RESET_L

(R2560-R2563)
XDP_CPU:BPM

XDP_BPM_L<4>	R2560	0
XDP_BPM_L<5>	R2561	0
XDP_BPM_L<6>	R2562	0
XDP_BPM_L<7>	R2563	0

PLACE_SIDE=BOTTOM
PLACE_SIDE=BOTTOM

(R2564-R2567)
XDP_CPU:CFG

CPU_CFG<12>	R2564	0
CPU_CFG<13>	R2565	0
CPU_CFG<14>	R2566	0
CPU_CFG<15>	R2567	0

CPU_PWRGD	R2500	1K	PLACE_NEAR=U1000.B46:2.54mm
PM_PWRBTN_L	R2502	0	PLACE_NEAR=U4900.J3:2.54mm
CPU_CFG<0>	R2501	1K	PLACE_NEAR=U1000.B50:2.54mm
PM_PCH_SYS_PWROK	R2504	330	

=PPVCCIO_S0_XDP

XDP_CPU_TDO	R2510	51
XDP_CPU_TDI	R2511	51
XDP_CPU_TMS	R2512	51
XDP_CPU_TCK	R2513	51
XDP_CPU_TRST_L	R2514	51

XDP PLACE_NEAR=J2500.52:2.54mm
XDP PLACE_NEAR=U1000.K61:2.54mm
XDP PLACE_NEAR=U1000.H59:2.54mm
XDP PLACE_NEAR=U1000.J58:2.54mm
XDP PLACE_NEAR=U1000.H63:2.54mm

XDP SIGNALS

(R2520-R2537)
XDP PCH SIGNALS

XDP_DA0_USB_EXTA_OC_L	R2520	33	XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L
XDP_DA1_USB_EXTB_OC_L	R2521	33	XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L
XDP_DA2_USB_EXTC_OC_L	R2522	33	XDP_DA2_PCH_GPIO41_USB_EXTC_OC_L
XDP_DA3_USB_EXTD_OC_L	R2523	33	XDP_DA3_PCH_GPIO42_USB_EXTD_OC_L
XDP_DB0_USB_EXTB_OC_EHCI_L	R2524	33	XDP_DB0_PCH_GPIO43_USB_EXTB_OC_EHCI
XDP_DB1_USB_EXTD_OC_EHCI_L	R2525	33	XDP_DB1_PCH_GPIO9_USB_EXTD_OC_EHCI_L
XDP_DB2_AP_PWR_EN	R2526	33	XDP_DB2_PCH_GPIO10_AP_PWR_EN
XDP_DB3_SDCONN_STATE_CHANGE	R2527	33	XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE
XDP_FC0	R2528	33	XDP_FC0_PCH_GPIO15
XDP_FC1	R2529	33	XDP_FC1_PCH_GPIO0
XDP_DC0_ISOLATE_CPU_MEM_L	R2530	33	XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L
XDP_DC1_MXM_GOOD	R2531	33	XDP_DC1_PCH_GPIO35_MXM_GOOD
XDP_DC2_DP_AUXCH_ISOL	R2532	33	XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL
XDP_DC3_SATARDRVR_EN	R2533	33	XDP_DC3_PCH_GPIO19_SATARDRVR_EN
XDP_DD0_DP_GPU_TBT_SEL	R2534	33	XDP_DD0_PCH_GPIO36_DP_GPU_TBT_SEL
XDP_DD1_JTAG_ISP_TCK	R2535	33	XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK
XDP_DD2_AUD_IPHS_SWITCH_EN	R2536	33	XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH
XDP_DD3_ENET_LOW_PWR	R2537	33	XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH

PCH SIGNALS

XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L	R2590	0
XDP_DB2_PCH_GPIO10_AP_PWR_EN	R2596	0
XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L	R2592	0
XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L	R2570	0
XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL	R2572	0
XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK	R2575	0
XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH	R2576	0
XDP_FC1_PCH_GPIO0	R2574	1K

Non-XDP Signals

USB_EXTA_OC_L	
AP_PWR_EN	
USB_EXTB_OC_L	
ISOLATE_CPU_MEM_L	
DP_AUXCH_ISOL	
JTAG_ISP_TCK	
AUD_IPHS_SWITCH_EN_PCH	
TBT_CIO_PLUG_EVENT_ISOL	

PCH Micro2-XDP

=PP3V3_S5_XDP

CRITICAL
XDP_CONN
J2550
DF40RC-60DP-0.4V
M-ST-SM1

518S0847

TP_XDP_PCH_OBSFN_A<0>	OBSFN_A0	OBSFN_C0	XDP_FC0
TP_XDP_PCH_OBSFN_A<1>	OBSFN_A1	OBSFN_C1	XDP_FC1
XDP_DA0_USB_EXTA_OC_L	OBSDATA_A0	OBSDATA_C0	XDP_DC0_ISOLATE_CPU_MEM_L
XDP_DA1_USB_EXTB_OC_L	OBSDATA_A1	OBSDATA_C1	XDP_DC1_MXM_GOOD
XDP_DA2_USB_EXTC_OC_L	OBSDATA_A2	OBSDATA_C2	XDP_DC2_DP_AUXCH_ISOL
XDP_DA3_USB_EXTD_OC_L	OBSDATA_A3	OBSDATA_C3	XDP_DC3_SATARDRVR_EN
TP_XDP_PCH_OBSFN_B<0>	OBSFN_B0	OBSFN_D0	TP_XDP_PCH_OBSFN_D<0>
TP_XDP_PCH_OBSFN_B<1>	OBSFN_B1	OBSFN_D1	TP_XDP_PCH_OBSFN_D<1>
XDP_DB0_USB_EXTB_OC_EHCI_L	OBSDATA_B0	OBSDATA_D0	XDP_DD0_DP_GPU_TBT_SEL
XDP_DB1_USB_EXTD_OC_EHCI_L	OBSDATA_B1	OBSDATA_D1	XDP_DD1_JTAG_ISP_TCK
XDP_DB2_AP_PWR_EN	OBSDATA_B2	OBSDATA_D2	XDP_DD2_AUD_IPHS_SWITCH_EN
XDP_DB3_SDCONN_STATE_CHANGE	OBSDATA_B3	OBSDATA_D3	XDP_DD3_ENET_LOW_PWR
XDP_PCH_S5_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	TP_XDP_PCH_HOOK4
XDP_PCH_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	TP_XDP_PCH_HOOK5
	VCC_OBS_AB	VCC_OBS_CD	
TP_XDPPCH_HOOK2	HOOK2	RESET#/HOOK6	XDPPCH_PLTRST_L
TP_XDPPCH_HOOK3	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
=SMBUS_XDP_SDA	SDA	TDO	XDP_PCH_TDO
=SMBUS_XDP_SCL	SCL	TRSTn	TP_XDP_PCH_TRST_L
	TCK1	TDI	XDP_PCH_TDI
XDP_PCH_TCK	TCK0	TMS	XDP_PCH_TMS
		XDP_PRESENT#	

NC

C2580 0.1uF 10% 16V X5R 402
C2581 0.1uF 10% 16V X5R 402

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

1K series R on PCH Support Page

R2584 1K XDP_PCH_S5_PWRGD — XDP PLACE_NEAR=J2550.40:2.54mm
R2585 0 XDP_PCH_PWRBTN_L — XDP PLACE_NEAR=U4900.J3:2.54mm

=PP1V05_SUS_PCH_JTAG

XDP_PCH_TDO	R2550	51
XDP_PCH_TDI	R2551	51
XDP_PCH_TMS	R2552	51
XDP_PCH_TCK	R2556	51

XDP PLACE_NEAR=J2550.51:2.54mm
XDP PLACE_NEAR=U1800.U12:2.54mm
XDP PLACE_NEAR=U1800.M15:2.54mm
XDP PLACE_NEAR=U1800.M17:2.54mm

PCH/XDP Signal Isolation Notes:

- Following Intel's Debug Prot Design Guid for HR and CR v1.3 doc id 404081.
Initially, stuffing both 33 and 0 ohms and validate whether it is functional in that state, else add BOM options.
- For isolated GPIOs:
  - 'Output' non-XDP signals require pulls.
  - 'Output' PCH/XDP signals require pulls.

R252x, R253x, R257x and R259x should be placed where signal path needs to split between route from PCH to J2550 and path to non-XDP signal destination.

SYNC_MASTER=J13_MLB	SYNC_DATE=08/04/2011
PAGE TITLE	CPU & PCH XDP
Apple Inc.	DRAWING NUMBER 051-9276 · SIZE D
	REVISION 2.7.0
	BRANCH
	PAGE 25 OF 109
	SHEET 23 OF 72

BOM GROUP	BOM OPTIONS
HUB_ALLREM	HUB_NONREM1_0,HUB_NONREM0_0
HUB_1NONREM	HUB_NONREM1_0,HUB_NONREM0_1
HUB_2NONREM	HUB_NONREM1_1,HUB_NONREM0_0
HUB_3NONREM	HUB_NONREM1_1,HUB_NONREM0_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0903	1	IC,USB2512B,USB 2.0 HUB CNTRL,36-QFN	U2600	CRITICAL	USBHUB2512B
338S0923	1	IC,USB2513B,USB 2.0,HUB CNTRL,3PRT,36QFN	U2600	CRITICAL	USBHUB2513B

USB XHCI/EHCI2 PORT MUX FOR EXT B

PCH PORT 9 (EHCI2)

PCH PORT 1 (XHCI)

TO LIO CONNECTOR

PULL-UP TO 3.3V SUS ON PCH PAGE, SEL PIN IS LEAKAGE-SAFE

SEL=0 CHOOSE USB EHCI2 PORT

SEL=1 CHOOSE USB XHCI PORT

PCH GPIO60

TO USB HUB

TO TP/KB

TO PCH XHCI

TO CONNECT TP/KB TO PCH XHCI
NOSTUFF R2611 & R2615, STUFF R2621,R2622,R2616 & R2617

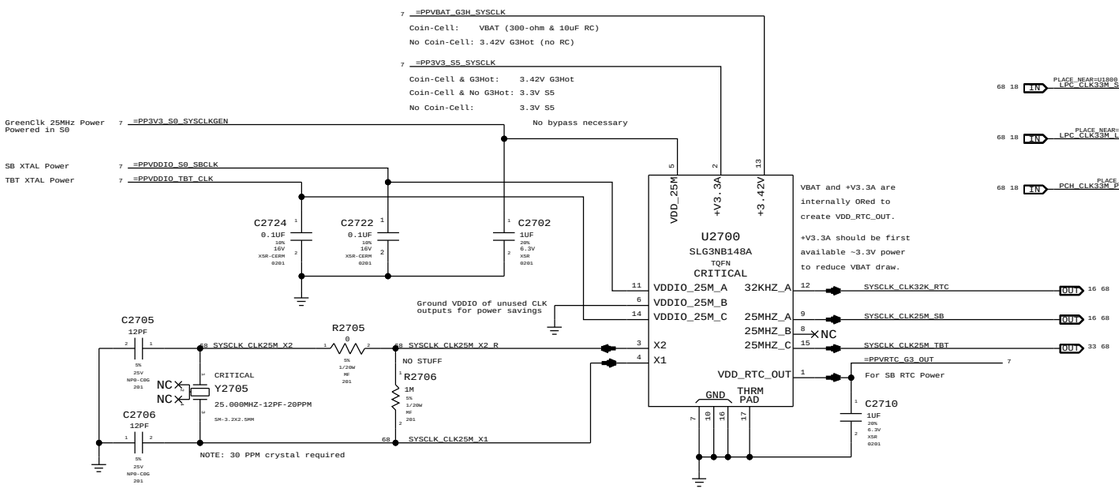
PLACE_NEAR=U2600.26:2.5MM

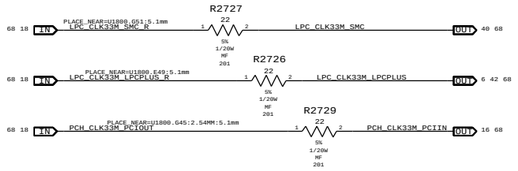
SYNC_MASTER=J13_MLB	SYNC_DATE=08/12/2011
PAGE TITLE	USB HUB & MUX
Apple Inc.	DRAWING NUMBER 051-9276 · SIZE D
	REVISION 2.7.0
	BRANCH
	PAGE 26 OF 109
	SHEET 24 OF 72

NOTICE OF PROPRIETARY PROPERTY:

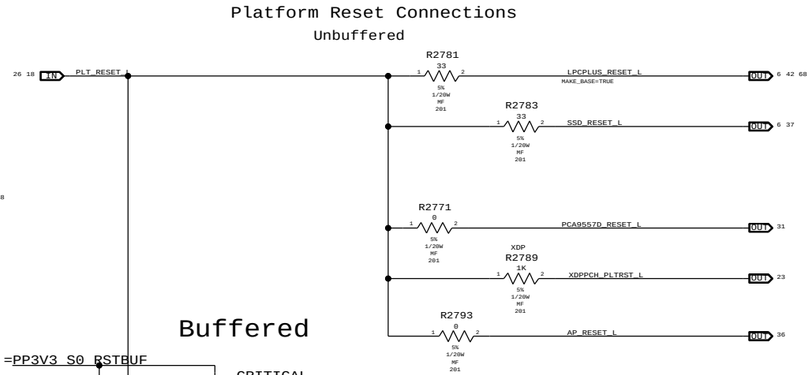
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

System RTC Power Source & 32kHz / 25MHz Clock Generator

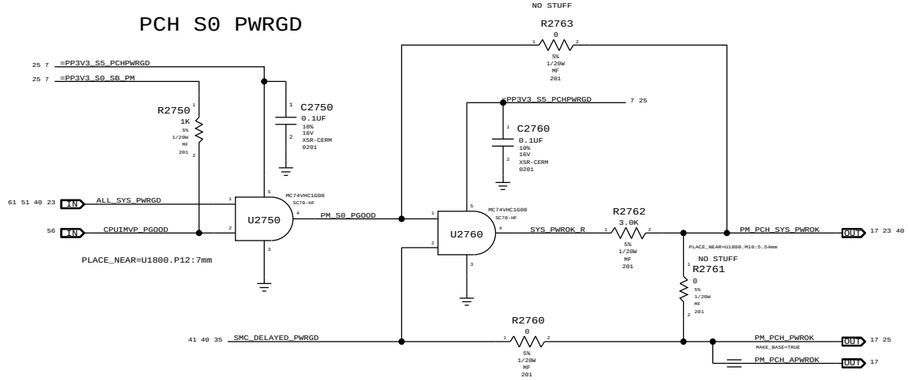




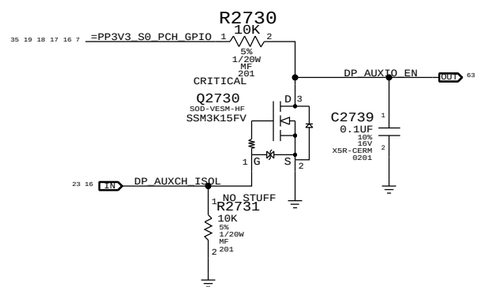
Platform Reset Connections



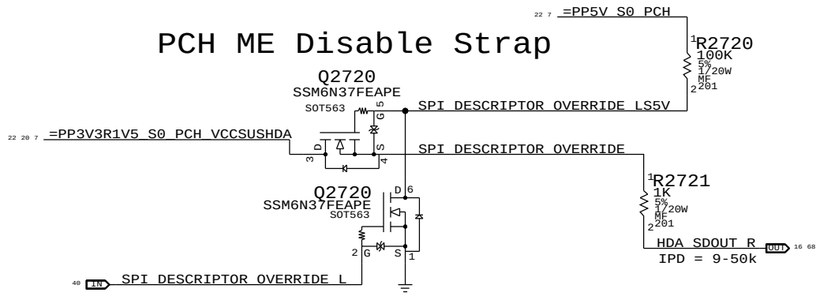
PCH S0 PWRGD



DP_AUXIO_EN Inversion

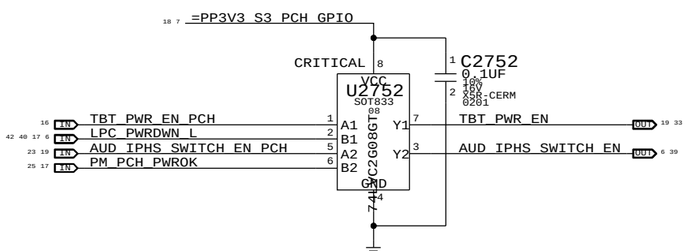


PCH ME Disable Strap

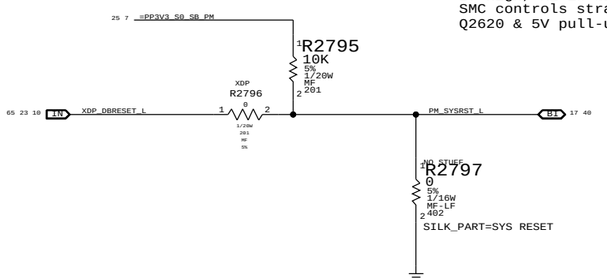


PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q2620 & 5V pull-up allows circuit to work regardless of HDA voltage.

GPIO Glitch Prevention



PCH Reset Button



SYNC_MASTER=J13_MLB	SYNC_DATE=08/12/2011
PAGE TITLE	Clock (CK505) and Chipset Support
Apple Inc.	DRAWING NUMBER 051-9276 · SIZE D
	REVISION 2.7.0
	BRANCH
	PAGE 27 OF 109
	SHEET 25 OF 72

NOTICE OF PROPRIETARY PROPERTY:

The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.

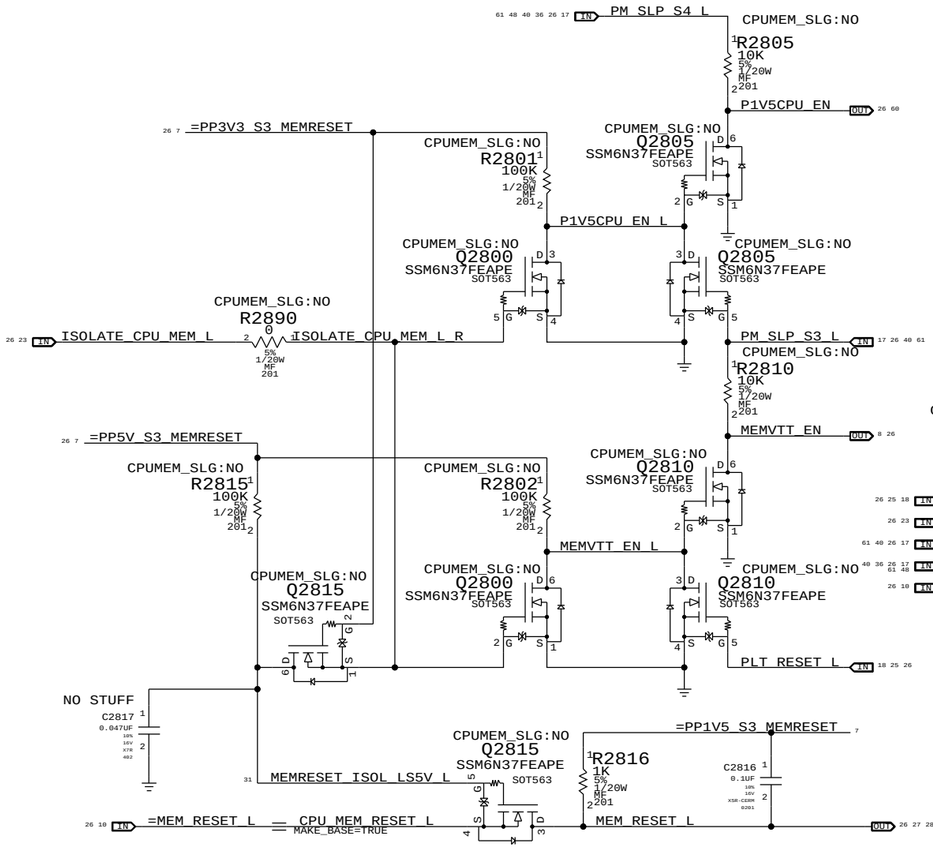
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.

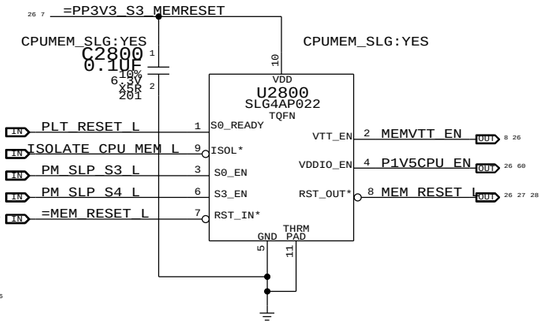
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L

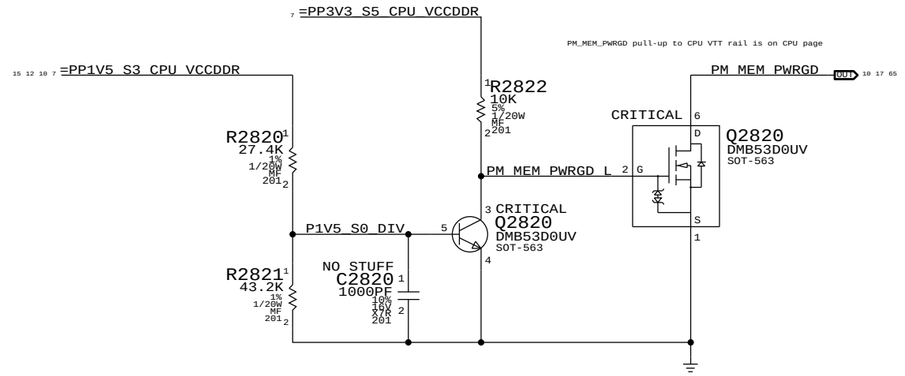
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L

MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L



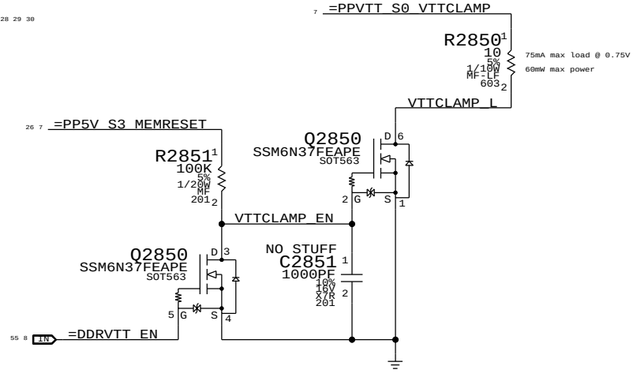


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
	1	0	1	1	1	1	1	1	1
to	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
S3	4	0	0	1	1	X	1	0	1
	5	0	1	1	1	0 (*)	1	1	1
to	6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC_MASTER=J13_MLB SYNC_DATE=11/18/2012

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

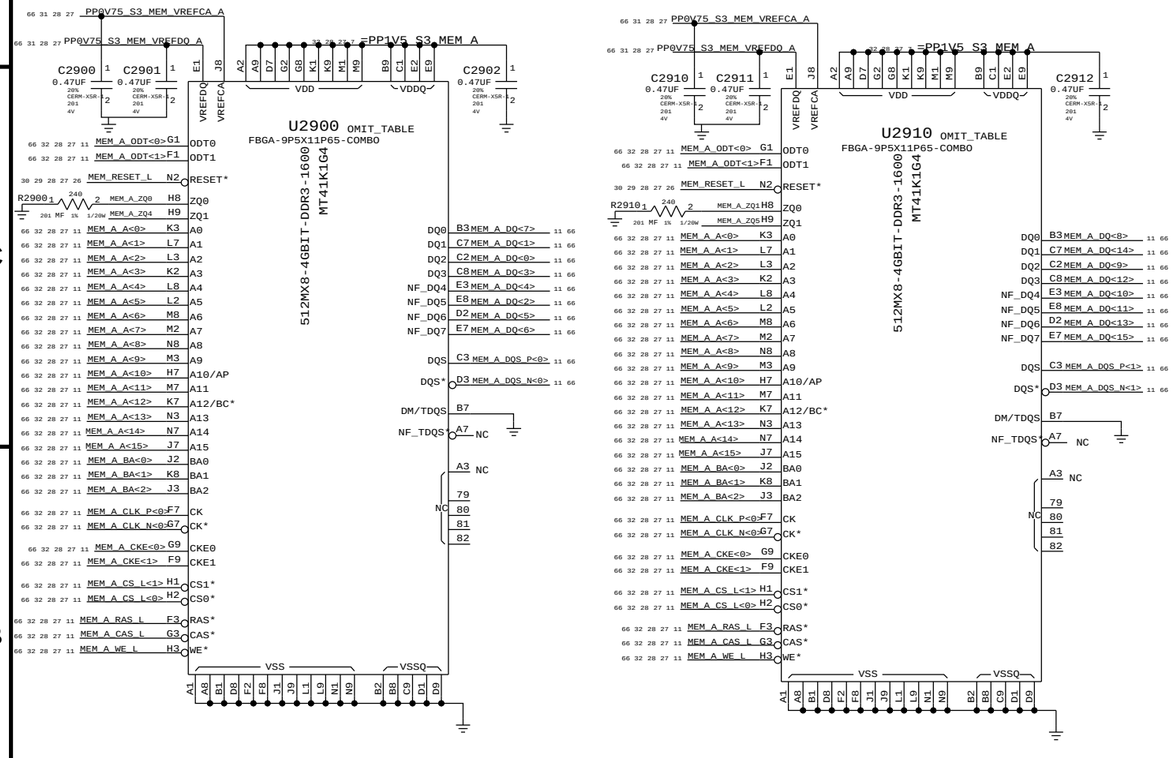
DRAWING NUMBER: 051-9276 SIZE: D

REVISION: 2.7.0

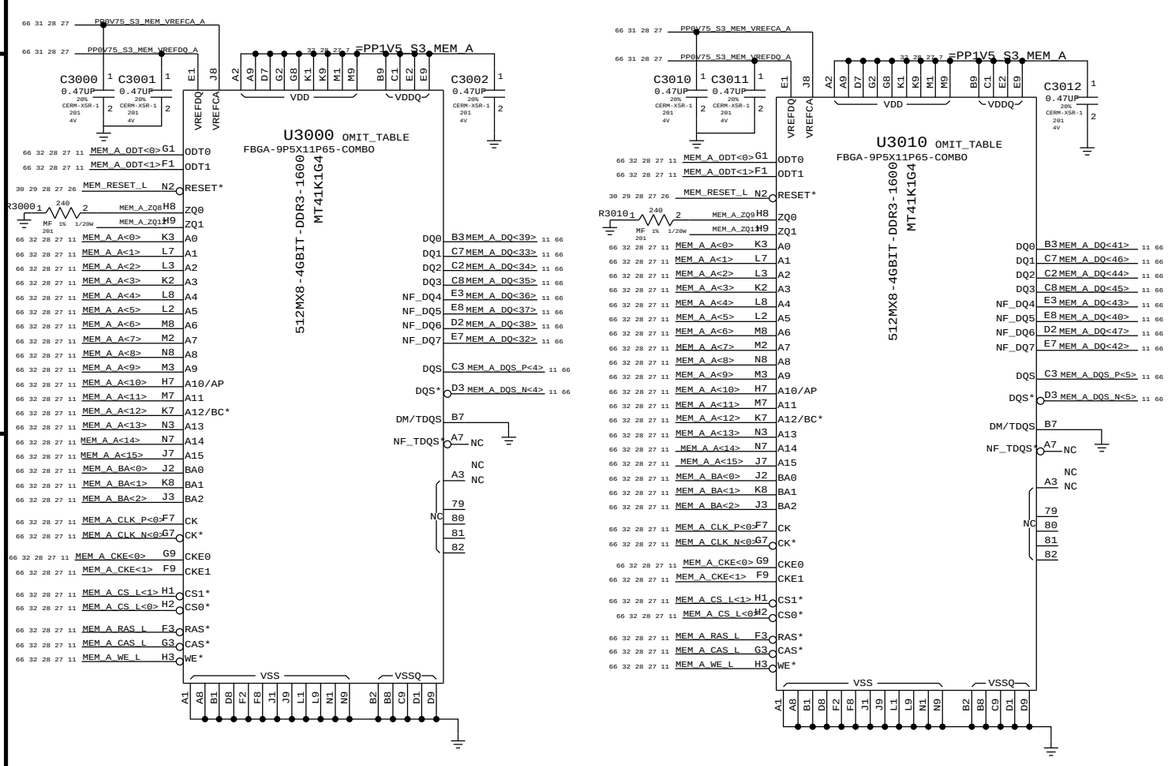
BRANCH:

PAGE: 28 OF 109

SHEET: 26 OF 72



SYNC_MASTER=J13_MLB						SYNC_DATE=08/29/2011	
PAGE TITLE: DDR3 DRAM CHANNEL A (0-31)							
Apple Inc.						DRAWING NUMBER: 051-9276	SIZE: D
						REVISION: 2.7.0	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED						BRANCH:	
						PAGE: 29 OF 109	
						SHEET: 27 OF 72	



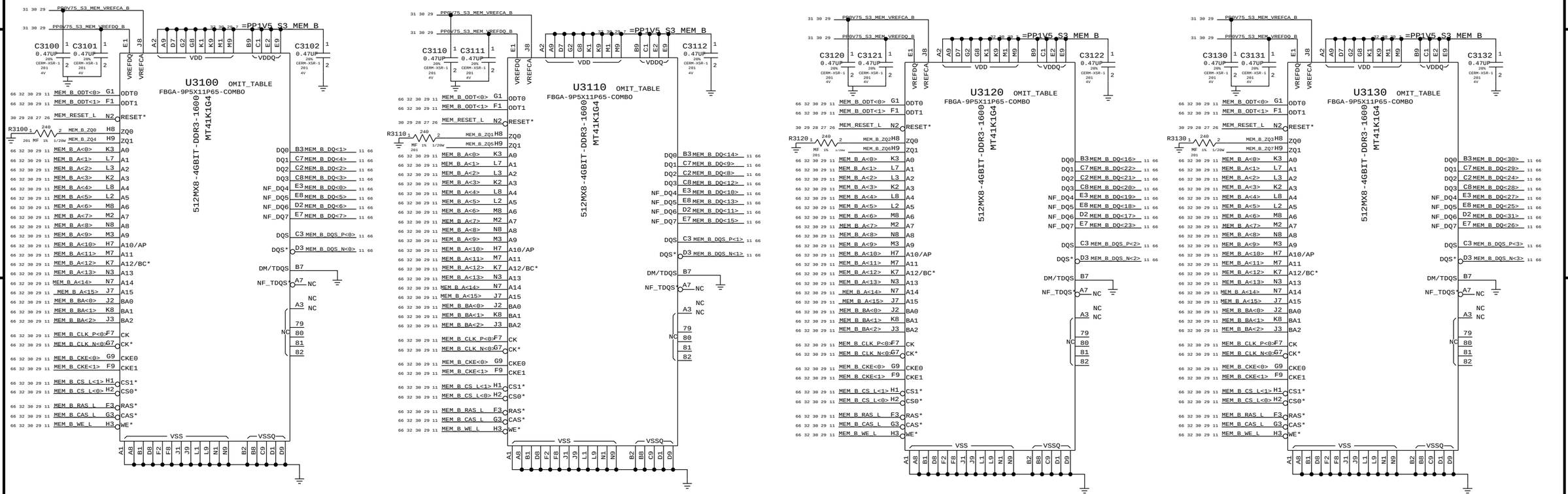
A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC_MASTER=J13_MLB SYNC_DATE=08/29/2011

PAGE TITLE
DDR3 DRAM CHANNEL A (32-63)

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D
REVISION 2.7.0
BRANCH
PAGE 30 OF 109
SHEET 28 OF 72



SYNC_MASTER=J13_MLB SYNC_DATE=08/29/2013

PAGE TITLE

DDR3 DRAM CHANNEL B (0-31)

Apple Inc.

DRAWING NUMBER 051-9276

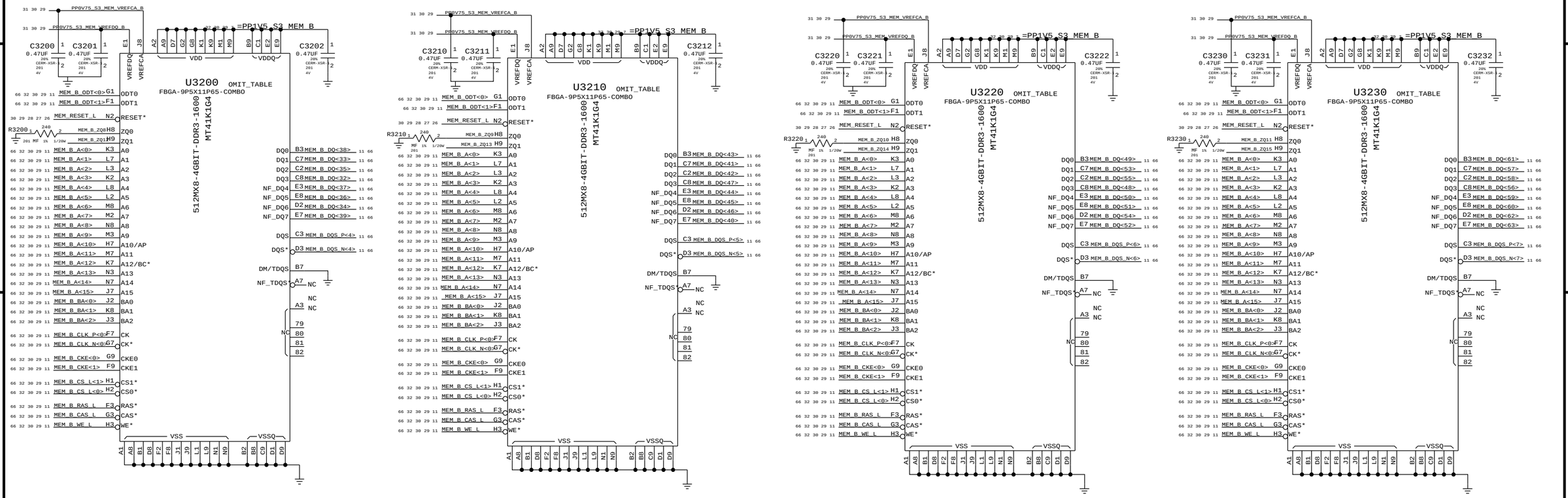
SIZE D

REVISION 2.7.0

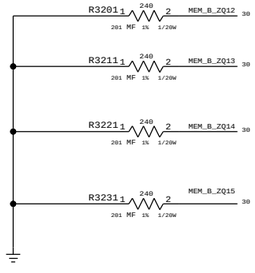
BRANCH

PAGE 31 OF 109

SHEET 29 OF 72



A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL



SYNC_MASTER=J13_MLB
SYNC_DATE=08/29/2017

PAGE TITLE
DDR3 DRAM CHANNEL B (32-63)

Apple Inc.

DRAWING NUMBER 051-9276
SIZE D
REVISION 2.7.0
BRANCH
PAGE 32 OF 109
SHEET 30 OF 72

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
DDRVREF_DAC - Stuffs Apple margining circuit.
VREFDQ:LDO - LDO outputs sent to DQ inputs.
VREFDQ:LDO_DAC - Margined LDO outputs sent to DQ inputs.
VREFDQ:M1_M3 - CPU margined DDR voltage divider sent to DQ inputs.
VREFDQ:M1_DAC - DAC margined DDR voltage divider sent to DQ inputs.
VREFCA:LDO - LDO outputs sent to CA inputs.
VREFCA:LDO_DAC - DAC margined LDO outputs sent to CA inputs.

NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.

=PP3V3_S3_VREFMRGN
OMIT R3318 SHORT PP3V3_S3_VREFMRGN_DAC
DDRVREF_DAC C3300 2.2UF 20% 6.3V CERM 402-LF
DDRVREF_DAC C3301 0.1UF 10% 16V X5R-CERM 0201
CRITICAL DDRVREF_DAC U3300 DAC5574 MSOP
=I2C_VREFDACS_SCL
=I2C_VREFDACS_SDA
Addr=0x98(WR)/0x99(RD)
VREFMRGN_SODIMMA_DQ
VREFMRGN_SODIMMS_CA
VREFMRGN_MEMVREG_FBVREF
NOTE: MEMVREG and FRAMEBUF share a DAC output, cannot enable both at the same time!
OMIT R3319 SHORT PP3V3_S3_VREFMRGN_CTRL
DDRVREF_DAC C3302 0.1UF 10% 6.3V X5R 201
CRITICAL DDRVREF_DAC U3301 PCA9557 QFN
Addr=0x30(WR)/0x31(RD)
=I2C_PCA9557D_SCL
=I2C_PCA9557D_SDA
VREFMRGN_DQ_SODIMMA_EN
VREFMRGN_CA_SODIMMB_EN
VREFMRGN_CA_SODIMMA_EN
VREFMRGN_MEMVREG_EN
PCA9557D_RESET_L
RST* on 'platform reset' so that system watchdog will disable margining.
NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.
=PPDDR_S3_MEMVREF
CRITICAL Q3320 SSM6N15AFE SOT563
MEMRESET_ISOL_LS5V_L
PPCPU_MEM_VREFDQ_A
PLACE_NEAR=Q3320.6:2mm
PLACE_NEAR=Q3320.6:1mm
C3320 0.1UF 10% 16V X5R-CERM 0201
R3321 1K 1% 1/20W MF 201
R3322 1K 1% 1/20W MF 201
PP0V75_S3_MEM_VREFDQ_A
PLACE_NEAR=R3321.2:1mm
NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step
CRITICAL Q3320 SSM6N15AFE SOT563
PLACE_NEAR=Q3320.3:2mm
C3310 0.1UF 10% 16V X5R-CERM 0201
R3311 1K 1% 1/20W MF 201
R3312 1K 1% 1/20W MF 201
PPCPU_MEM_VREFDQ_B
PP0V75_S3_MEM_VREFDQ_B
PLACE_NEAR=R3311.2:1mm
DDRVREF_DAC C3303 0.1UF 10% 16V X5R-CERM 0201
DDRVREF_DAC U3302 MAX4253 UCSP
VREFMRGN_DQ_SODIMMA_BUF
DDRVREF_DAC R3301 100K 5% 1/20W MF 201
DDRVREF_DAC U3302 MAX4253 UCSP
VREFMRGN_CA_SODIMMB_BUF
DDRVREF_DAC R3307 100K 5% 1/20W MF 201
DDRVREF_DAC U3304 MAX4253 UCSP
VREFMRGN_CA_SODIMMA_BUF
DDRVREF_DAC R3315 100K 5% 1/20W MF 201
DDRVREF_DAC C3305 0.1UF 10% 16V X5R-CERM 0201
DDRVREF_DAC U3304 MAX4253 UCSP
VREFMRGN_MEMVREG_BUF
DDRVREF_DAC R3313 100K 5% 1/20W MF 201
=PPVTT_S3_DDR_BUF
10mA max load
VREFDQ:LDO_DAC R3303 200 1% 1/20W MF 201
VREFDQ:LDO_DAC R3304 133 1% 1/20W MF 201
PP0V75_S3_MEM_VREFDQ_B
PLACE_NEAR=U2900.E1:2.54mm
PLACE_NEAR=R3303.2:1mm
PLACE_NEAR=Q3310.3:1mm
VREFDQ:LDO_DAC R3360 0 5% 1/20W MF 201
PP0V75_S3_MEM_VREFDQ_A
VREFCA:LDO_DAC R3309 200 1% 1/20W MF 201
VREFCA:LDO_DAC R3310 133 1% 1/20W MF 201
PP0V75_S3_MEM_VREFCA_B
PLACE_NEAR=U2900.J8:2.54mm
PLACE_NEAR=R3309.2:1mm
PLACE_NEAR=R3309:1mm NOSTUFF
R3361 0 5% 1/20W MF 201
VREFCA:LDO_DAC R3305 200 1% 1/20W MF 201
VREFCA:LDO_DAC R3306 133 1% 1/20W MF 201
PP0V75_S3_MEM_VREFCA_A
PLACE_NEAR=U3100.J8:2.54mm
PLACE_NEAR=R3305.2:1mm
DDRVREF_DAC R3314 33.2K 1% 1/20W MF 201
DDRREG_FB
PLACE_NEAR=R7315.2:1mm

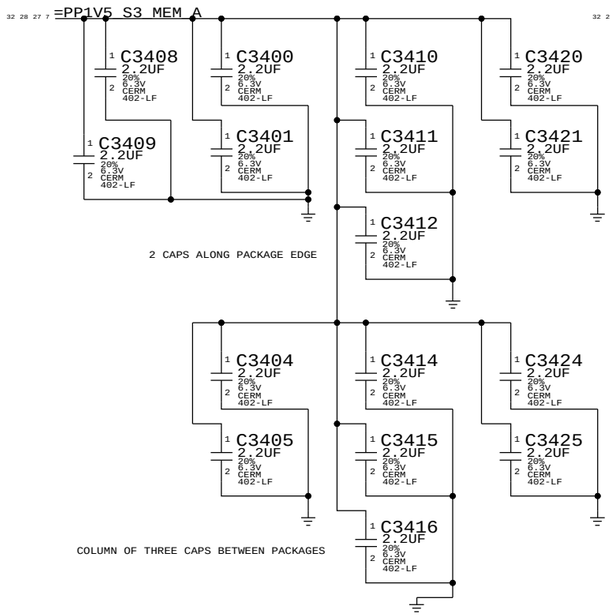
Required zero ohm resistors when no VREF margining circuit stuffed

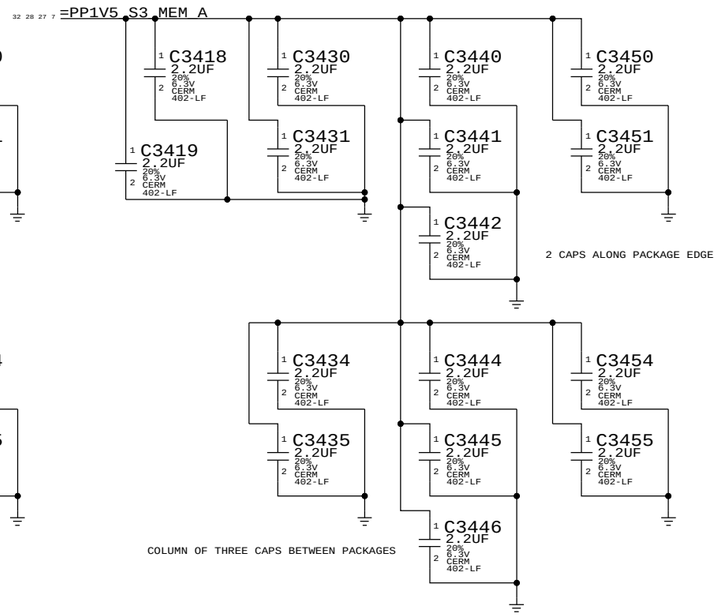
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	2	RES,MF,1/20W,0.0 OHM,5,0201,SMD	R3303,R3360		VREFDQ:LDO
117S0002	2	RES,MF,1/20W,0.0 OHM,5,0201,SMD	R3309,R3305		VREFCA:LDO

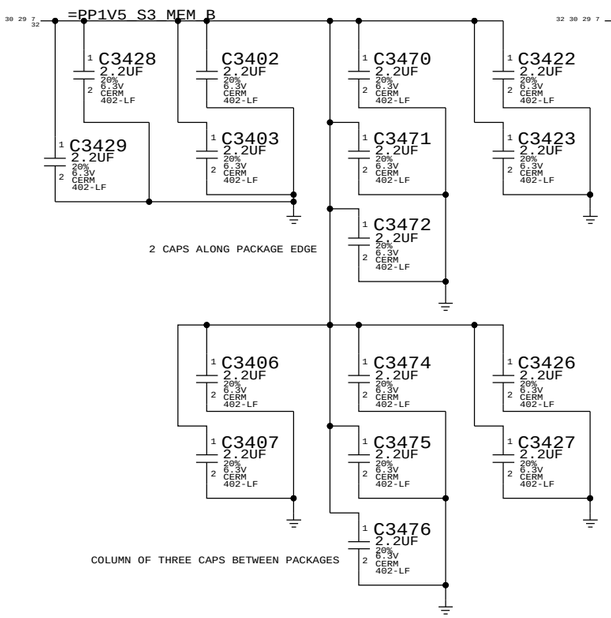
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0012	4	RES,MF,1KOHM,1,1/20W,0201	R3321,R3322,R3311,R3312		VREFDQ:M1_DAC
118S0303	1	RES,MF,332OHM,1,1/20W,0201	R3304		VREFDQ:M1_DAC

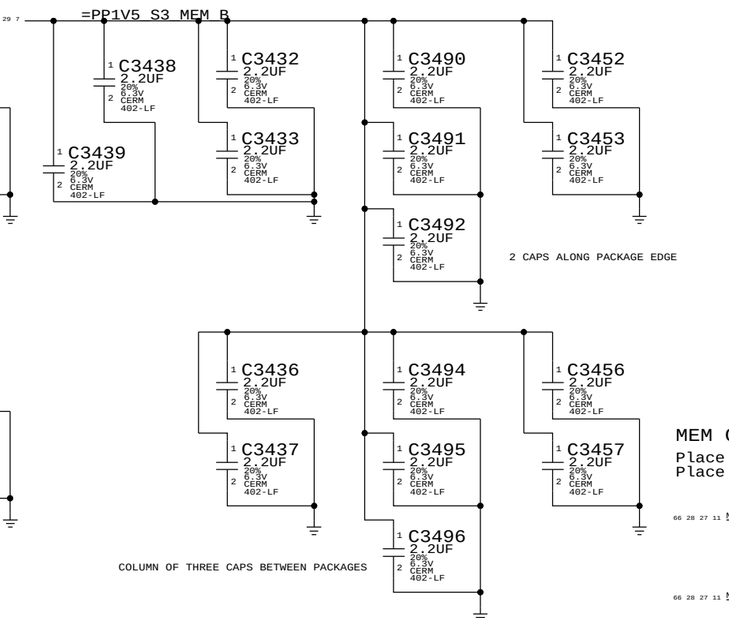
	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=J13_MLB SYNC_DATE=11/18/2013
PAGE TITLE: FSB/DDR3/FRAMEBUF Vref Margining
Apple Inc.
DRAWING NUMBER: 051-9276 SIZE: D
REVISION: 2.7.0
BRANCH:
PAGE: 33 OF 109
SHEET: 31 OF 72

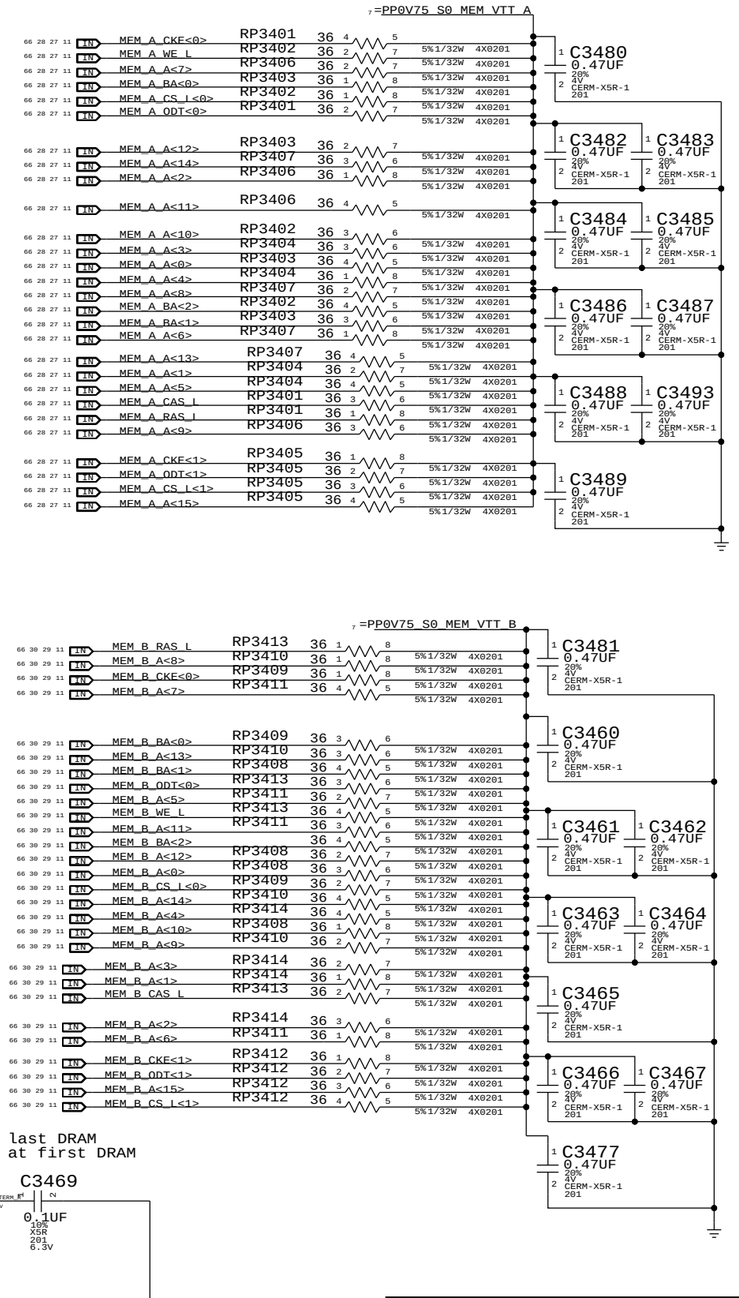






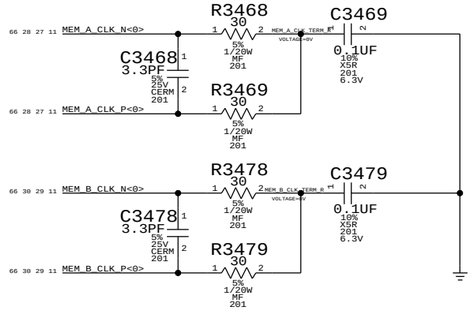


JEDEC recommends 30 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE



MEM CLOCK TERMINATION

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM

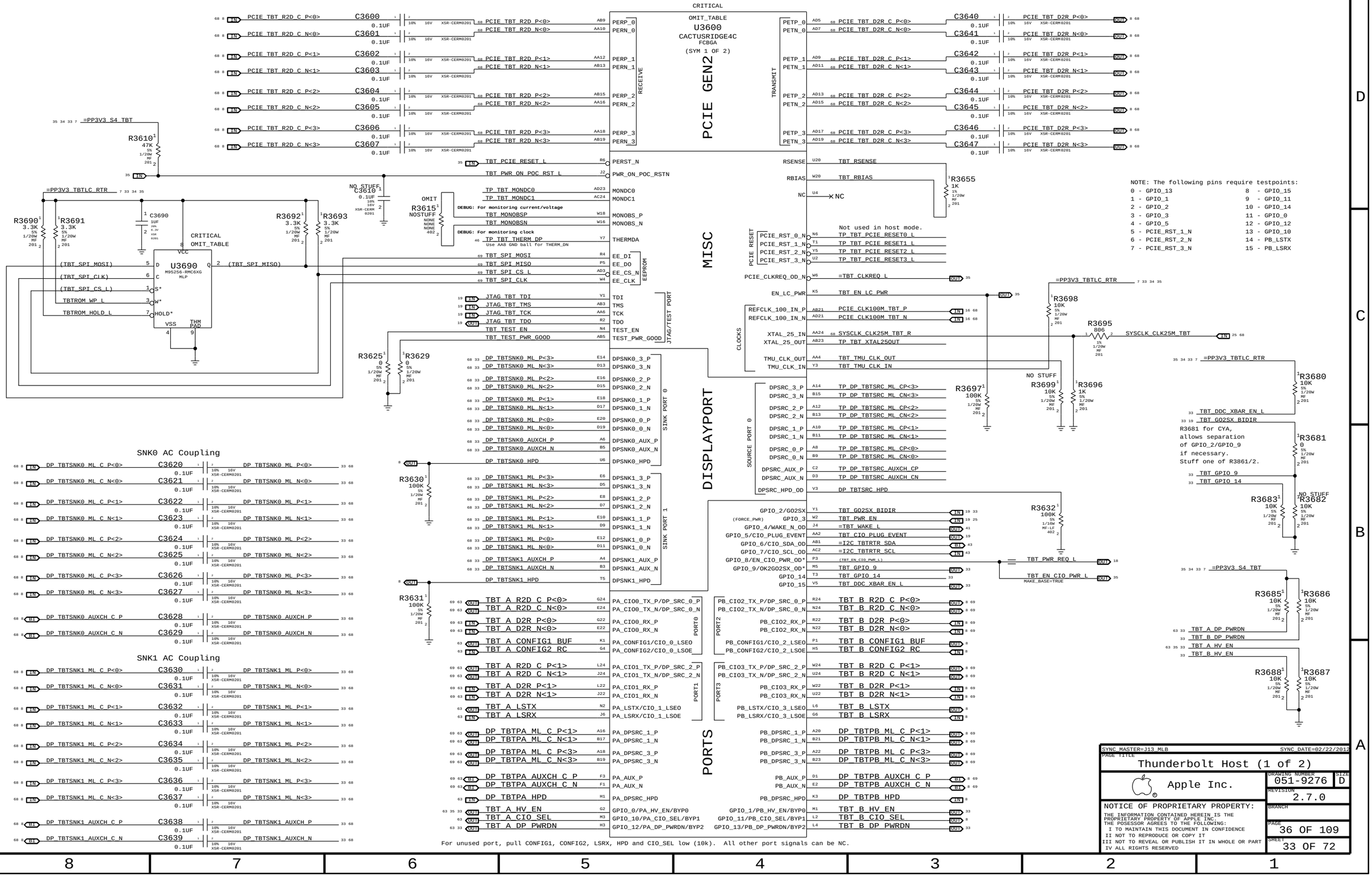


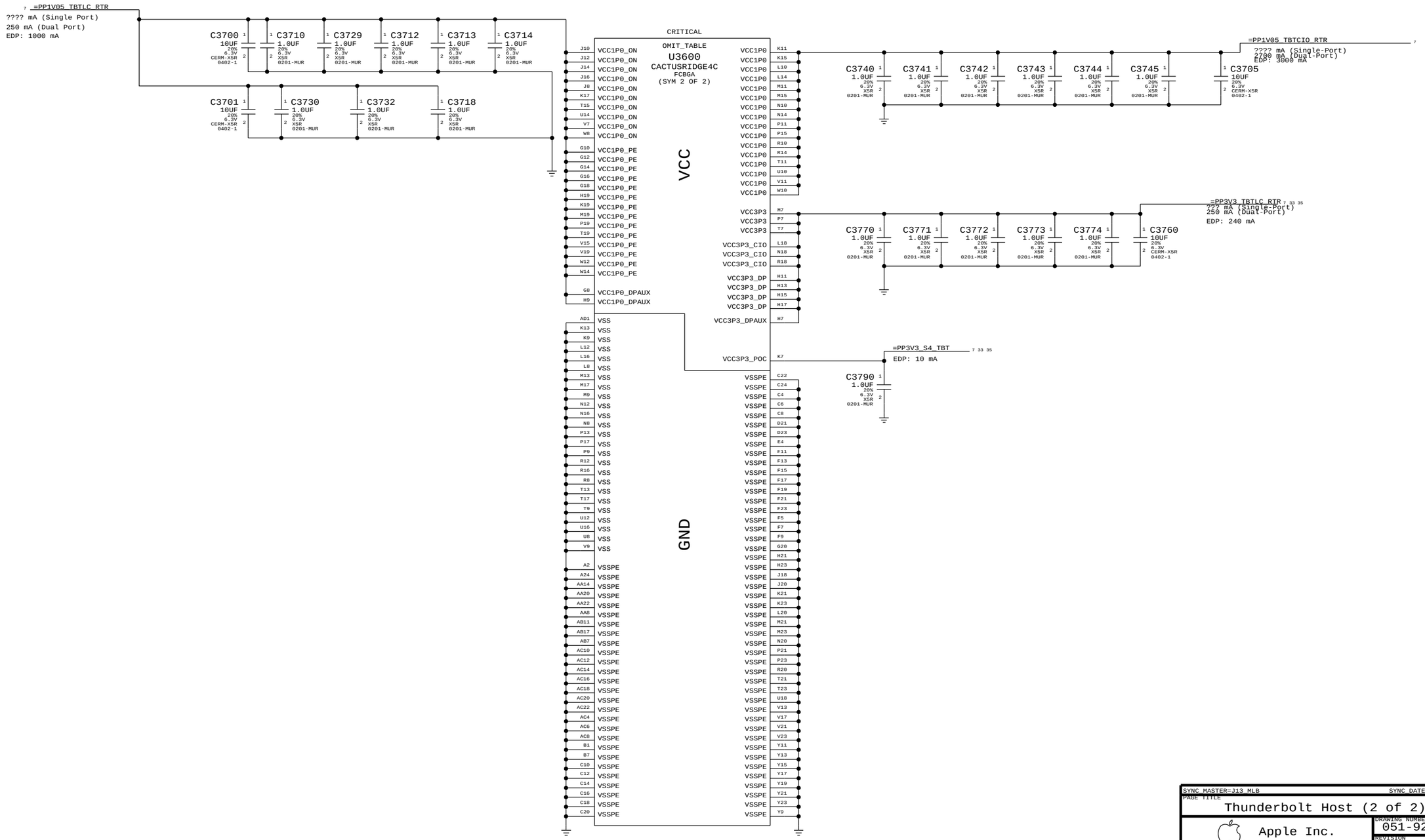
SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE
DDR3 DRAM Channel B (32-63)

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D
REVISION 2.7.0
BRANCH
PAGE 34 OF 109
SHEET 32 OF 72


CRITICAL
OMIT_TABLE
U3600
CACTUSRIDGE4C
FCBGA
(SYM 1 OF 2)
PCIE GEN2
RECEIVE
TRANSMIT
PCIE_TBT_R2D_C_P<0>
PCIE_TBT_R2D_C_N<0>
PCIE_TBT_R2D_C_P<1>
PCIE_TBT_R2D_C_N<1>
PCIE_TBT_R2D_C_P<2>
PCIE_TBT_R2D_C_N<2>
PCIE_TBT_R2D_C_P<3>
PCIE_TBT_R2D_C_N<3>
PCIE_TBT_R2D_P<0>
PCIE_TBT_R2D_N<0>
PCIE_TBT_R2D_P<1>
PCIE_TBT_R2D_N<1>
PCIE_TBT_R2D_P<2>
PCIE_TBT_R2D_N<2>
PCIE_TBT_R2D_P<3>
PCIE_TBT_R2D_N<3>
PCIE_TBT_D2R_C_P<0>
PCIE_TBT_D2R_C_N<0>
PCIE_TBT_D2R_C_P<1>
PCIE_TBT_D2R_C_N<1>
PCIE_TBT_D2R_C_P<2>
PCIE_TBT_D2R_C_N<2>
PCIE_TBT_D2R_C_P<3>
PCIE_TBT_D2R_C_N<3>
PCIE_TBT_D2R_P<0>
PCIE_TBT_D2R_N<0>
PCIE_TBT_D2R_P<1>
PCIE_TBT_D2R_N<1>
PCIE_TBT_D2R_P<2>
PCIE_TBT_D2R_N<2>
PCIE_TBT_D2R_P<3>
PCIE_TBT_D2R_N<3>
C3600 0.1UF
C3601 0.1UF
C3602 0.1UF
C3603 0.1UF
C3604 0.1UF
C3605 0.1UF
C3606 0.1UF
C3607 0.1UF
C3640 0.1UF
C3641 0.1UF
C3642 0.1UF
C3643 0.1UF
C3644 0.1UF
C3645 0.1UF
C3646 0.1UF
C3647 0.1UF
MISC
PERST_N
PWR_ON_POC_RST_L
TBT_PCIE_RESET_L
MONDC0
MONDC1
MONOBS_P
MONOBS_N
THERMDA
EE_DI
EE_DO
EE_CS_N
EE_CLK
EEPROM
TBT_SPI_MOSI
TBT_SPI_MISO
TBT_SPI_CS_L
TBT_SPI_CLK
JTAG/TEST PORT
TDI
TMS
TCK
TDO
TEST_EN
TEST_PWR_GOOD
JTAG_TBT_TDI
JTAG_TBT_TMS
JTAG_TBT_TCK
JTAG_TBT_TDO
TBT_TEST_EN
TBT_TEST_PWR_GOOD
DISPLAYPORT
SINK PORT 0
SINK PORT 1
DPSNK0_3_P
DPSNK0_3_N
DPSNK0_2_P
DPSNK0_2_N
DPSNK0_1_P
DPSNK0_1_N
DPSNK0_0_P
DPSNK0_0_N
DPSNK0_AUX_P
DPSNK0_AUX_N
DPSNK0_HPD
DPSNK1_3_P
DPSNK1_3_N
DPSNK1_2_P
DPSNK1_2_N
DPSNK1_1_P
DPSNK1_1_N
DPSNK1_0_P
DPSNK1_0_N
DPSNK1_AUX_P
DPSNK1_AUX_N
DPSNK1_HPD
DP_TBTSNK0_ML_P<3>
DP_TBTSNK0_ML_N<3>
DP_TBTSNK0_ML_P<2>
DP_TBTSNK0_ML_N<2>
DP_TBTSNK0_ML_P<1>
DP_TBTSNK0_ML_N<1>
DP_TBTSNK0_ML_P<0>
DP_TBTSNK0_ML_N<0>
DP_TBTSNK0_AUXCH_P
DP_TBTSNK0_AUXCH_N
DP_TBTSNK0_HPD
DP_TBTSNK1_ML_P<3>
DP_TBTSNK1_ML_N<3>
DP_TBTSNK1_ML_P<2>
DP_TBTSNK1_ML_N<2>
DP_TBTSNK1_ML_P<1>
DP_TBTSNK1_ML_N<1>
DP_TBTSNK1_ML_P<0>
DP_TBTSNK1_ML_N<0>
DP_TBTSNK1_AUXCH_P
DP_TBTSNK1_AUXCH_N
DP_TBTSNK1_HPD
PORT0
PORT1
PORT2
PORT3
PA_CIO0_TX_P/DP_SRC_0_P
PA_CIO0_TX_N/DP_SRC_0_N
PA_CIO0_RX_P
PA_CIO0_RX_N
PA_CONFIG1/CIO_0_LSEO
PA_CONFIG2/CIO_0_LSOE
PA_CIO1_TX_P/DP_SRC_2_P
PA_CIO1_TX_N/DP_SRC_2_N
PA_CIO1_RX_P
PA_CIO1_RX_N
PA_LSTX/CIO_1_LSEO
PA_LSRX/CIO_1_LSOE
PB_CIO2_TX_P/DP_SRC_0_P
PB_CIO2_TX_N/DP_SRC_0_N
PB_CIO2_RX_P
PB_CIO2_RX_N
PB_CONFIG1/CIO_2_LSEO
PB_CONFIG2/CIO_2_LSOE
PB_CIO3_TX_P/DP_SRC_2_P
PB_CIO3_TX_N/DP_SRC_2_N
PB_CIO3_RX_P
PB_CIO3_RX_N
PB_LSTX/CIO_3_LSEO
PB_LSRX/CIO_3_LSOE
PORTS
PA_DPSRC_1_P
PA_DPSRC_1_N
PA_DPSRC_3_P
PA_DPSRC_3_N
PA_AUX_P
PA_AUX_N
PA_DPSRC_HPD
PB_DPSRC_1_P
PB_DPSRC_1_N
PB_DPSRC_3_P
PB_DPSRC_3_N
PB_AUX_P
PB_AUX_N
PB_DPSRC_HPD
DP_TBTPA_ML_C_P<1>
DP_TBTPA_ML_C_N<1>
DP_TBTPA_ML_C_P<3>
DP_TBTPA_ML_C_N<3>
DP_TBTPA_AUXCH_C_P
DP_TBTPA_AUXCH_C_N
DP_TBTPA_HPD
DP_TBTPB_ML_C_P<1>
DP_TBTPB_ML_C_N<1>
DP_TBTPB_ML_C_P<3>
DP_TBTPB_ML_C_N<3>
DP_TBTPB_AUXCH_C_P
DP_TBTPB_AUXCH_C_N
DP_TBTPB_HPD
GPIO_0/PA_HV_EN/BYP0
GPIO_10/PA_CIO_SEL/BYP1
GPIO_12/PA_DP_PWRDN/BYP2
GPIO_1/PB_HV_EN/BYP0
GPIO_11/PB_CIO_SEL/BYP1
GPIO_13/PB_DP_PWRDN/BYP2
TBT_A_HV_EN
TBT_A_CIO_SEL
TBT_A_DP_PWRDN
TBT_B_HV_EN
TBT_B_CIO_SEL
TBT_B_DP_PWRDN
For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.
RSENSE
RBIAS
NC
TBT_RSENSE
TBT_RBIAS
R3655 1K
Not used in host mode.
PCIE RESET
PCIE_RST_0_N
PCIE_RST_1_N
PCIE_RST_2_N
PCIE_RST_3_N
TP_TBT_PCIE_RESET0_L
TP_TBT_PCIE_RESET1_L
TP_TBT_PCIE_RESET2_L
TP_TBT_PCIE_RESET3_L
PCIE_CLKREQ_OD_N
=TBT_CLKREQ_L
EN_LC_PWR
TBT_EN_LC_PWR
CLOCKS
REFCLK_100_IN_P
REFCLK_100_IN_N
PCIE_CLK100M_TBT_P
PCIE_CLK100M_TBT_N
XTAL_25_IN
XTAL_25_OUT
SYSCLK_CLK25M_TBT_R
TP_TBT_XTAL25OUT
TMU_CLK_OUT
TMU_CLK_IN
TBT_TMU_CLK_OUT
TBT_TMU_CLK_IN
R3695 806
SYSCLK_CLK25M_TBT
R3698 10K
R3697 100K
R3699 10K NO STUFF
R3696 1K
R3680 10K
R3681 0
R3683 10K
R3682 10K NO STUFF
R3632 100K
R3685 10K
R3686 10K
R3688 10K
R3687 10K
TBT_DDC_XBAR_EN_L
TBT_GO2SX_BIDIR
R3681 for CYA, allows separation of GPIO_2/GPIO_9 if necessary. Stuff one of R3861/2.
TBT_GPIO_9
TBT_GPIO_14
GPIO_2/GO2SX
GPIO_3 (FORCE_PWR)
GPIO_4/WAKE_N_OD
GPIO_5/CIO_PLUG_EVENT
GPIO_6/CIO_SDA_OD
GPIO_7/CIO_SCL_OD
GPIO_8/EN_CIO_PWR_OD*
GPIO_9/OK2GO2SX_OD*
GPIO_14
GPIO_15
TBT_GO2SX_BIDIR
TBT_PWR_EN
=TBT_WAKE_L
TBT_CIO_PLUG_EVENT
=I2C_TBTRTR_SDA
=I2C_TBTRTR_SCL
TBT_GPIO_9
TBT_GPIO_14
TBT_DDC_XBAR_EN_L
TBT_PWR_REQ_L
TBT_EN_CIO_PWR_L
MAKE_BASE=TRUE
=PP3V3_TBTLC_RTR
=PP3V3_S4_TBT
R3610 47K
R3690 3.3K
R3691 3.3K
R3692 3.3K
R3693 3.3K
C3690 1UF
R3615 NOSTUFF
C3610 0.1UF NO STUFF
R3625 0
R3629 0
R3630 100K
R3631 100K
CRITICAL
OMIT_TABLE
U3690
M9525G-RMC6XG
MLP
VCC
VSS
THM PAD
(TBT_SPI_MOSI)
(TBT_SPI_CLK)
(TBT_SPI_CS_L)
TBTROM_WP_L
TBTROM_HOLD_L
(TBT_SPI_MISO)
DEBUG: For monitoring current/voltage
TBT_MONOBSP
TBT_MONOBSN
DEBUG: For monitoring clock
TP_TBT_THERM_DP
Use AA8 GND ball for THERM_DN
SNK0 AC Coupling
SNK1 AC Coupling
C3620 0.1UF
C3621 0.1UF
C3622 0.1UF
C3623 0.1UF
C3624 0.1UF
C3625 0.1UF
C3626 0.1UF
C3627 0.1UF
C3628 0.1UF
C3629 0.1UF
C3630 0.1UF
C3631 0.1UF
C3632 0.1UF
C3633 0.1UF
C3634 0.1UF
C3635 0.1UF
C3636 0.1UF
C3637 0.1UF
C3638 0.1UF
C3639 0.1UF
NOTE: The following pins require testpoints:
0 - GPIO_13
1 - GPIO_1
2 - GPIO_2
3 - GPIO_3
4 - GPIO_5
5 - PCIE_RST_1_N
6 - PCIE_RST_2_N
7 - PCIE_RST_3_N
8 - GPIO_15
9 - GPIO_11
10 - GPIO_14
11 - GPIO_0
12 - GPIO_12
13 - GPIO_10
14 - PB_LSTX
15 - PB_LSRX
SYNC MASTER=J13 MLB
SYNC_DATE=02/22/2012
PAGE TITLE
Thunderbolt Host (1 of 2)
Apple Inc.
DRAWING NUMBER 051-9276
SIZE D
REVISION 2.7.0
BRANCH
PAGE 36 OF 109
SHEET 33 OF 72
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=J13_MLB SYNC_DATE=09/01/2011

PAGE TITLE: Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER: 051-9276 SIZE: D

REVISION: 2.7.0

BRANCH:

PAGE: 37 OF 109

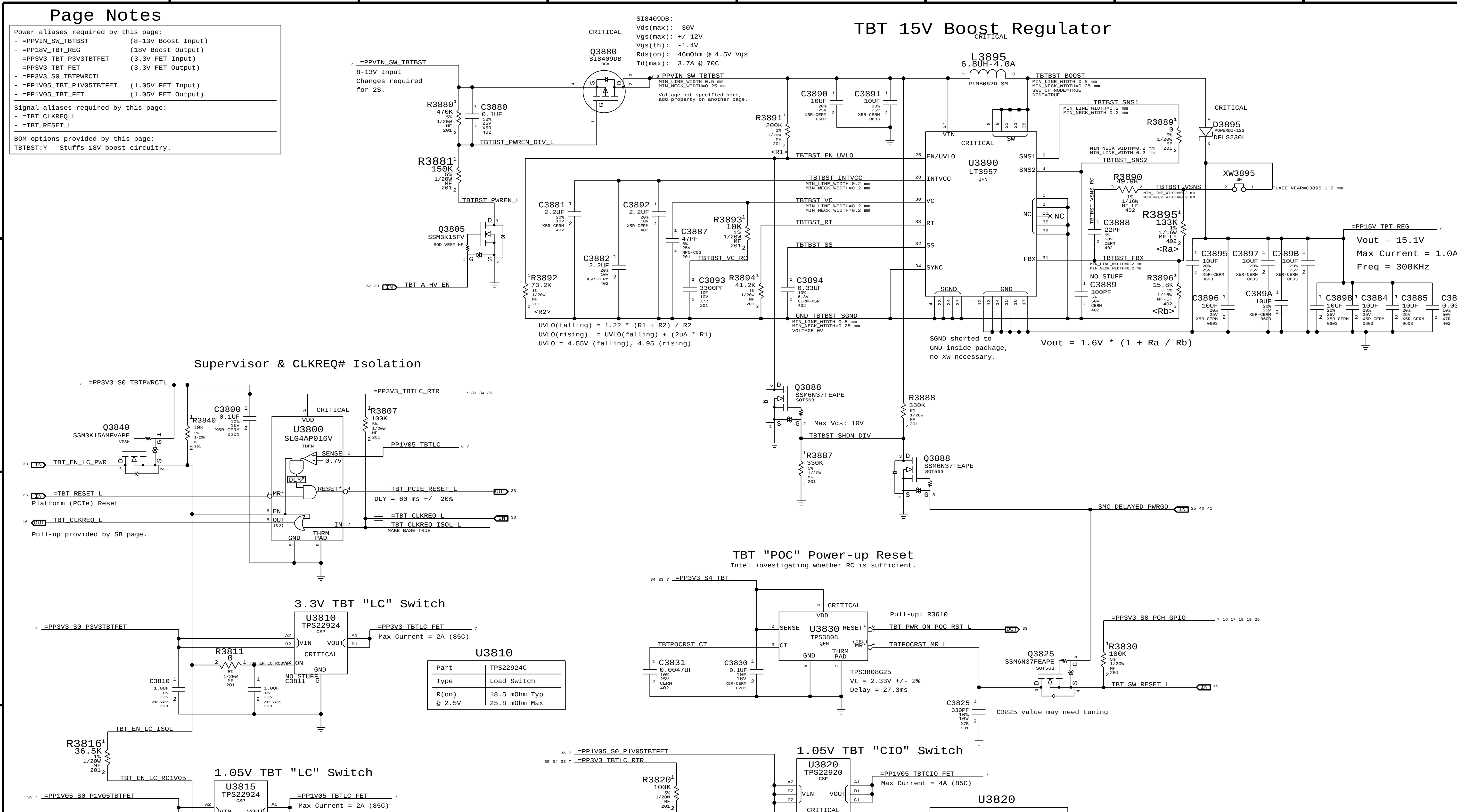
SHEET: 34 OF 72

Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP18V_TBT_REG (18V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBT_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBT_FET (1.05V FET Output)

Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
TBTBST:Y - Stuffs 18V boost circuitry.



U3810

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

U3815

Part	TPS22924C
Type	Load Switch
R(on) @ 1.0V	20.3 mOhm Typ 28.6 mOhm Max

U3820

Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	8 mOhm Typ 11.5 mOhm Max

SYNC_MASTER=J13_MLB SYNC_DATE=11/18/2011

PAGE TITLE: TBT Power Support

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D

REVISION 2.7.0

BRANCH

AIRPORT

CRITICAL
J4001
SSD-K99
F-RT-SM1

514S0335

WIFI_EVENT_L OUT 6 40 41
PCIE_AP_R2D_N 68 6 — C4030 0.1UF 10% 6.3V X5R 201 — PCIE_AP_R2D_C_N IN 16 68
PCIE_AP_R2D_P 68 6 — C4031 0.1UF 10% 6.3V X5R 201 — PCIE_AP_R2D_C_P IN 16 68
PCIE_CLK100M_AP_N IN 6 16 68
PCIE_CLK100M_AP_P IN 6 16 68
PCIE_AP_D2R_P OUT 6 16 68
PCIE_AP_D2R_N OUT 6 16 68
PCIE_WAKE_L OUT 6 17

C4030 PLACEMENT_NOTE=Place close to J4001.
C4031 PLACEMENT_NOTE=Place close to J4001.

3V S3 WLAN FET

MOSFET	DMP2018LFK
CHANNEL	P-TYPE
RDS(ON)	14-20 mOHM @2.5V
LOADING	0.750 A (EDP)

CRITICAL
R4052 0.020 1% 0.25W MF 805
MIN_LINE_WIDTH=1 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=3.3V

CRITICAL
Q4050
DMP2018LFK
DFN2563-6

MIN_LINE_WIDTH=1 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=3.3V
41 35 6 PP3V3_WLAN_F — 2 PP3V3_WLAN_R — 4 — =PP3V3_S3_WLAN 7 36

C4021 0.1UF 10% 6.3V X5R 201
C4020 10UF 20% 16V X5R 603
PLACEMENT_NOTE=Place close to Q4050.
PLACEMENT_NOTE=Place close to Q4050.

C4050 0.1UF 10% 16V X5R-CERM 0201
P3V3WLAN_SS
C4051 0.033UF 10% 16V X5R 402
R4050 100K 5% 1/20W MF 201
R4051 10K 5% 1/20W MF 201
PM_WLAN_EN_L IN 61

ISNS_AIRPORT_P OUT 45 71
ISNS_AIRPORT_N OUT 45 71

BLUETOOTH

67 6 USB_BT_CONN_N
67 6 USB_BT_CONN_P

BTPWR:S4 R4001 0 5% 1/16W MF-LF 402
36 6 PP3V3_S3RS4_BT_F — =PP3V3_S4_BT 7
MIN_NECK_WIDTH=0.2 mm MIN_LINE_WIDTH=0.5 mm VOLTAGE=3.3V

C4032 0.1UF 10% 6.3V X5R 201
PLACE_NEAR=J4001.18:1.5mm

BTPWR:S3 R4002 0 5% 1/16W MF-LF 402
=PP3V3_S3_BT 7

NOSTUFF BTPWR:S3 R4017 15K 1% 1/20W MF 201
BTPWR:S3 R4018 0 5% 1/20W MF 201
PP3V3_S3RS4_BT_F 6 36
C4010 0.1UF 10% 6.3V X5R 201
NOSTUFF R4014 15K 1% 1/20W MF 201

BTPWR:S4 Q4010 SSM3K15FV SOD-VESM-HF
=BT_WAKE_L OUT 41

U4010 PI3USB102ZLE TQFN CRITICAL
VCC
Y+ Y- SEL GND OE* M+ M- D+ D-
USB_BT_WAKE_P 67
USB_BT_WAKE_N 67
USB_BT_P BT 24 67
USB_BT_N BT 24 67

NOSTUFF R4015 15K 1% 1/20W MF 201
NOSTUFF R4016 15K 1% 1/20W MF 201
BTPWR:S4 R4012 15K 1% 1/20W MF 201
BTPWR:S4 NOSTUFF R4013 15K 1% 1/20W MF 201

BTPWR:S4 R4011 0 5% 1/20W MF 201
40 26 17 51 48 PM_SLP_S4_L — BTMUX_SEL
NOSTUFF C4011 0.01UF 10% 16V CERM 402

SEL	OUTPUT
L	USB_BT_WAKE
H	USB_BT

DLY = 60 MS +/- 20%

41 36 6 PP3V3_WLAN_F
=PP3V3_S3_WLAN 7 36
C4053 0.1UF 10% 6.3V X5R 201

CRITICAL
U4002 SLG4AP016V TDFN
VDD SENSE 0.7V RDLY RESET* MR* EN OUT (OD) IN THRM PAD GND

R4053 100K 5% 1/20W MF 201
R4054 232K 1% 1/20W MF 201
R4055 100K 1% 1/20W MF 201

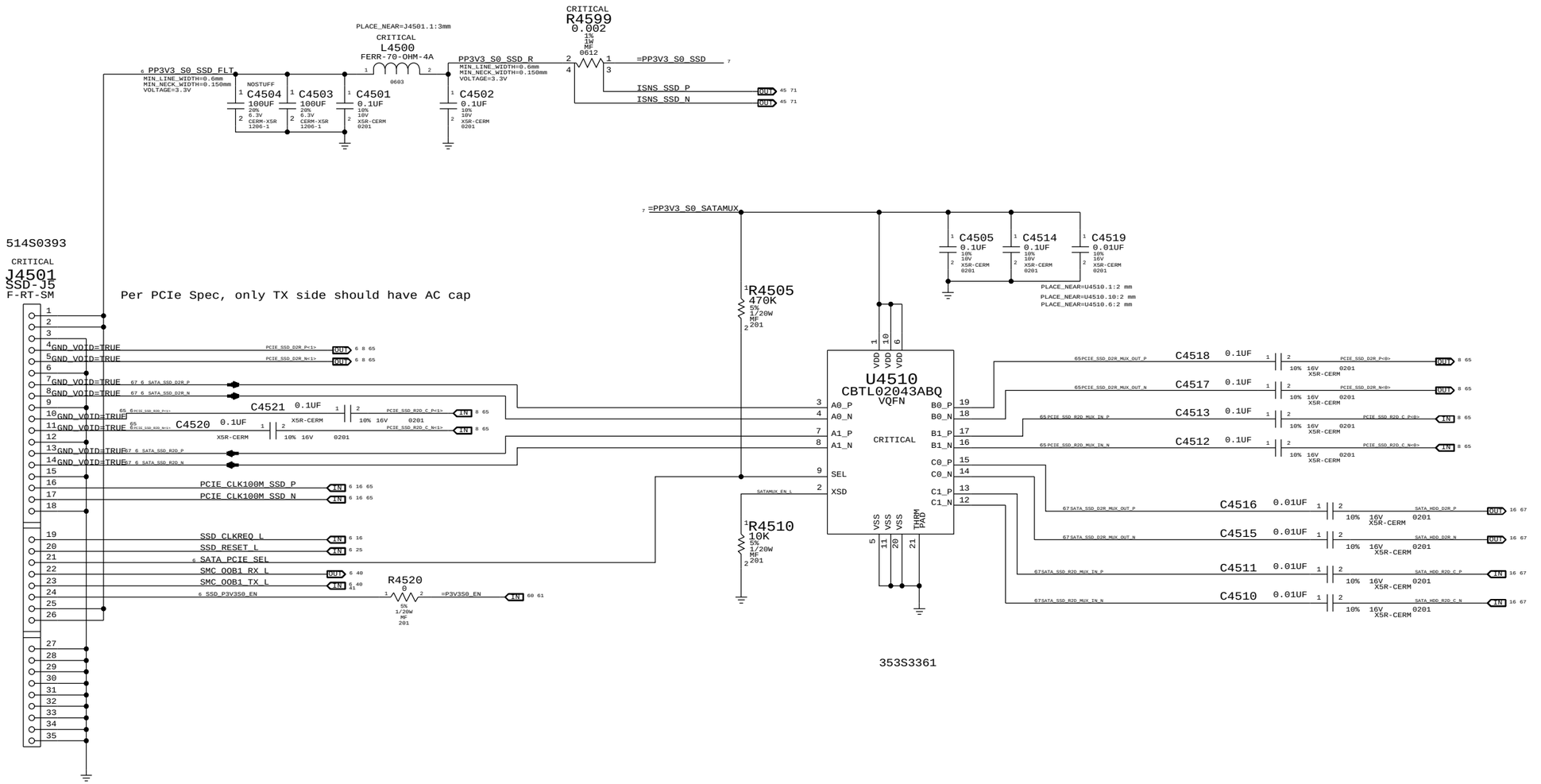
P3V3WLAN_VMON
6 AP_RESET_CONN_L
6 AP_CLKREQ_Q_L

AP_RESET_L IN 25
AP_PWR_EN IN 18 23 61
AP_CLKREQ_L_R — R4090 0 5% 1/20W MF 201 — AP_CLKREQ_L OUT 16

SYNC MASTER=J13_MLB SYNC_DATE=10/06/2013
PAGE TITLE
X21 WIRELESS CONNECTOR

Apple Inc.

DRAWING NUMBER 051-9276
SIZE D
REVISION 2.7.0
BRANCH
PAGE 40 OF 109
SHEET 36 OF 72

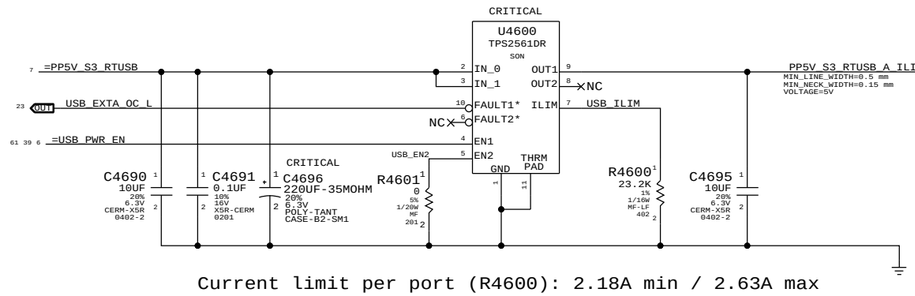


PCIE/SATA GUMSTICK2 CONNECTOR

SYNC_MASTER=J13_MLB	SYNC_DATE=11/18/2011
PAGE TITLE	SSD CONNECTOR
Apple Inc.	DRAWING NUMBER 051-9276 SIZE D
	REVISION 2.7.0
	BRANCH
	PAGE 45 OF 109
	SHEET 37 OF 72

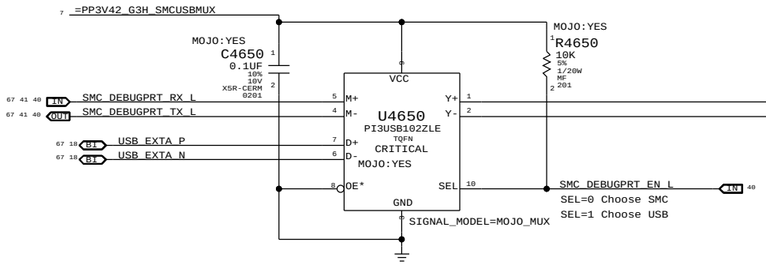
Right USB Port A

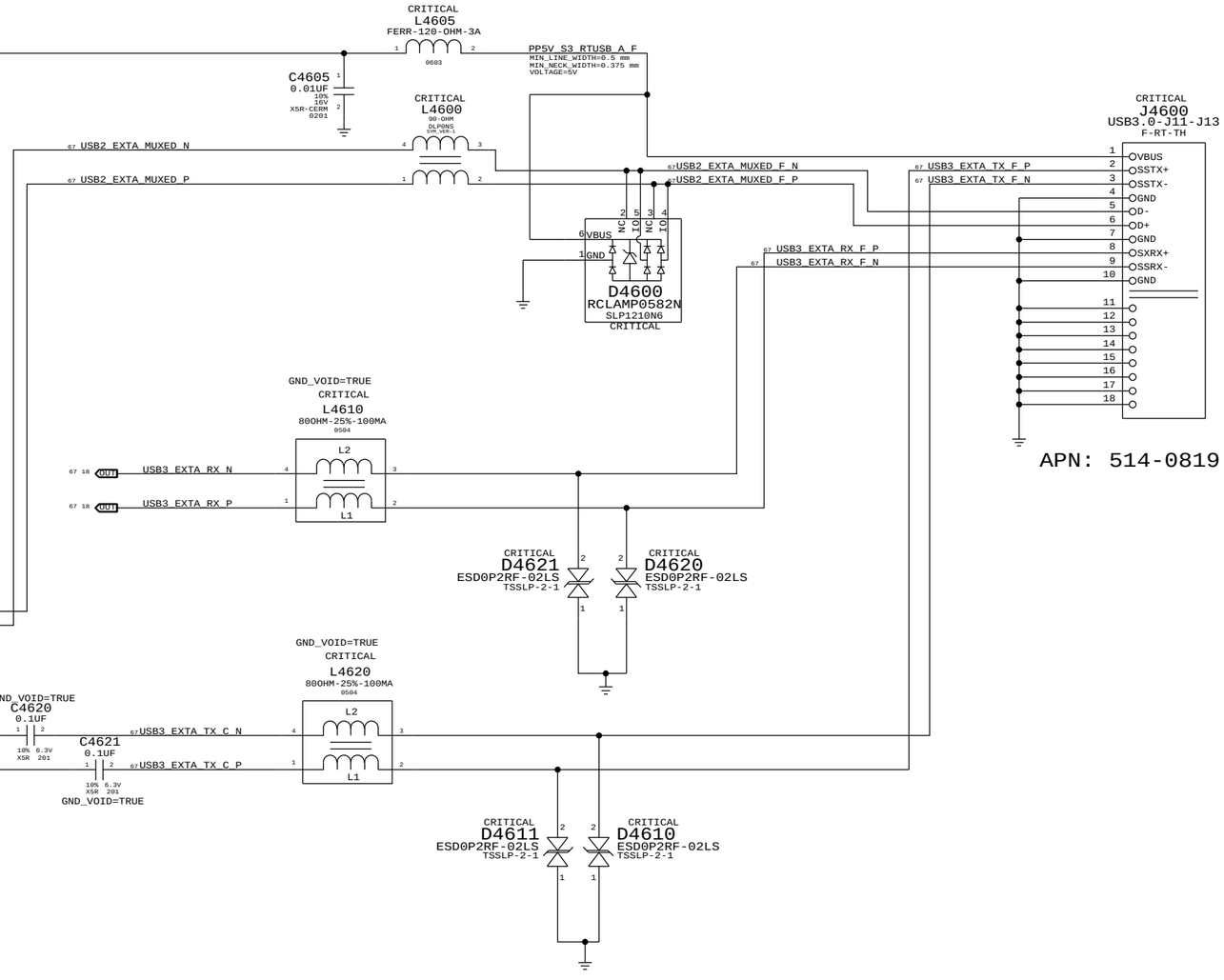
USB Port Power Switch



Current limit per port (R4600): 2.18A min / 2.63A max

Mojo SMC Debug Mux

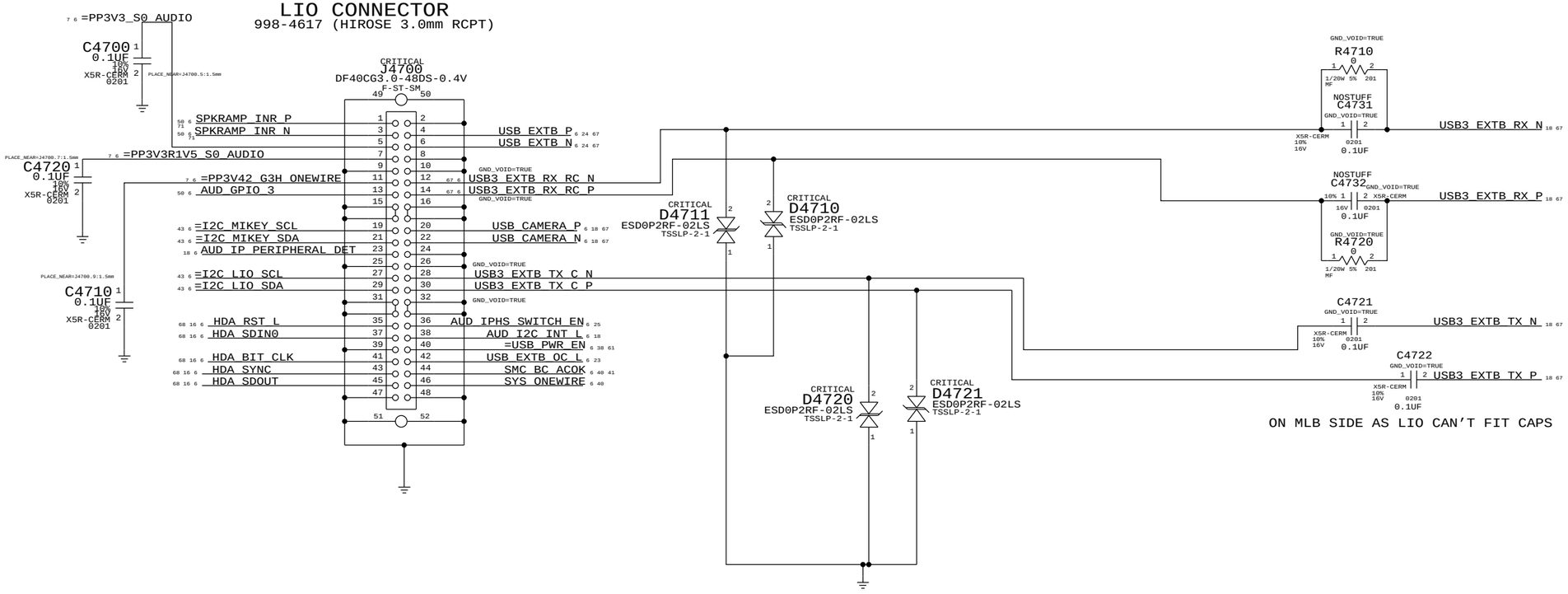




APN: 514-0819

SYNC_MASTER=J13_MLB	SYNC_DATE=10/06/2011
PAGE TITLE	External A USB3 Connector
Apple Inc.	DRAWING NUMBER 051-9276 SIZE D
	REVISION 2.7.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH
	PAGE 46 OF 109
	SHEET 38 OF 72

LIO CONNECTOR
998-4617 (HIROSE 3.0mm RCPT)



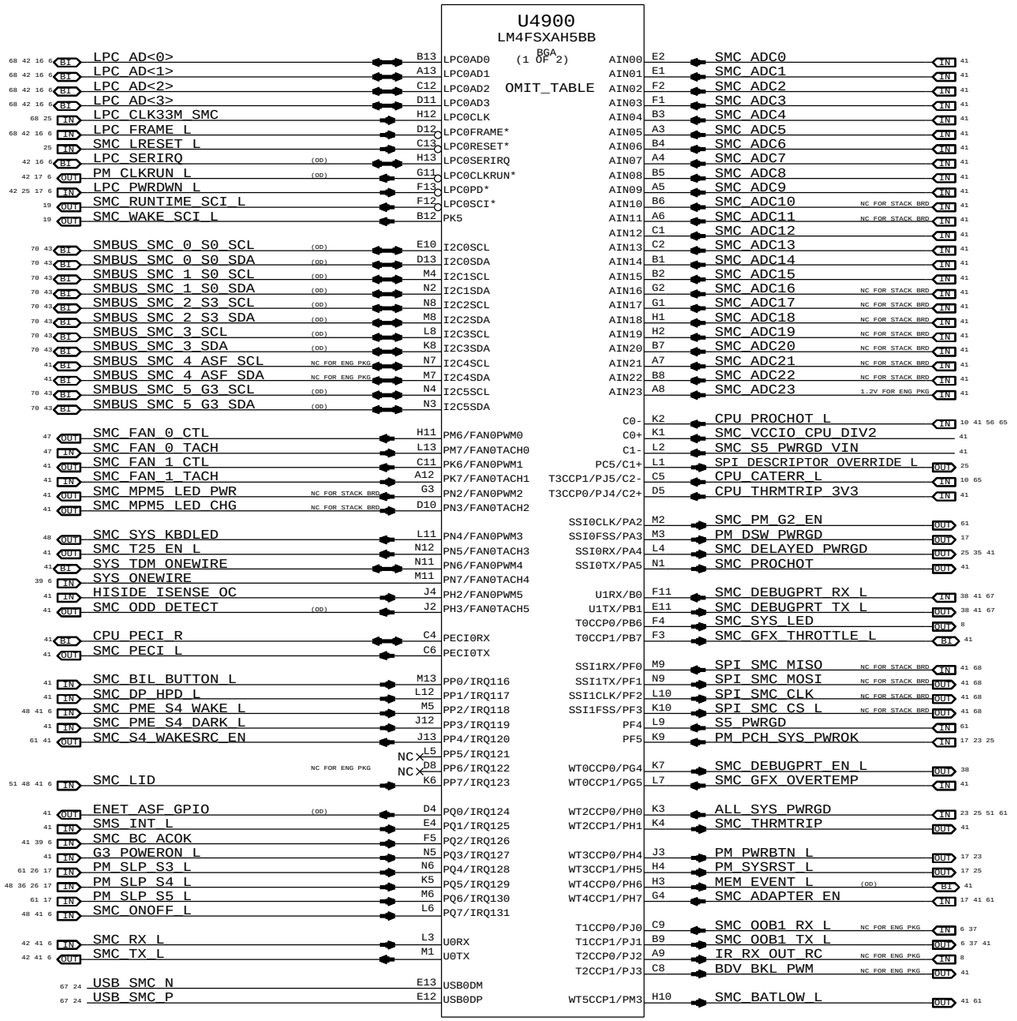
ON MLB SIDE AS LIO CAN'T FIT CAPS

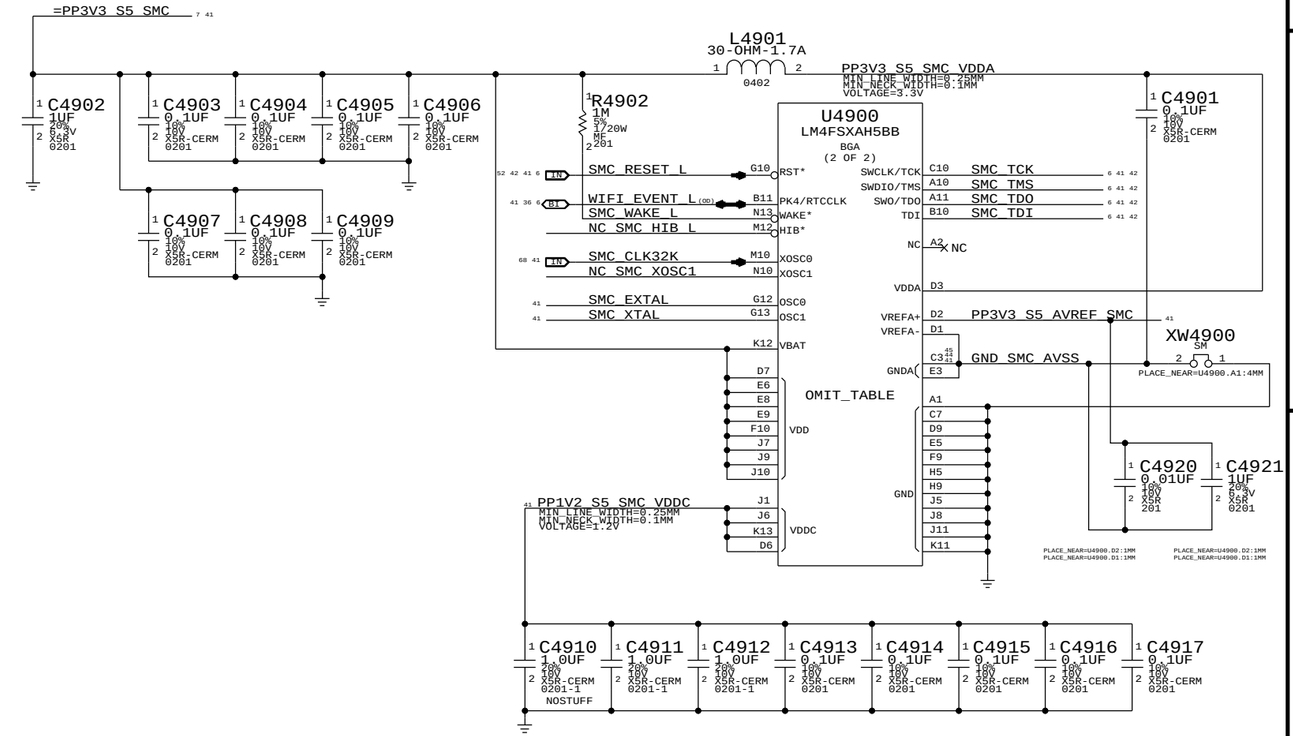
SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
LIO CONNECTORS

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D
REVISION 2.7.0
BRANCH
PAGE 47 OF 109
SHEET 39 OF 72





NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

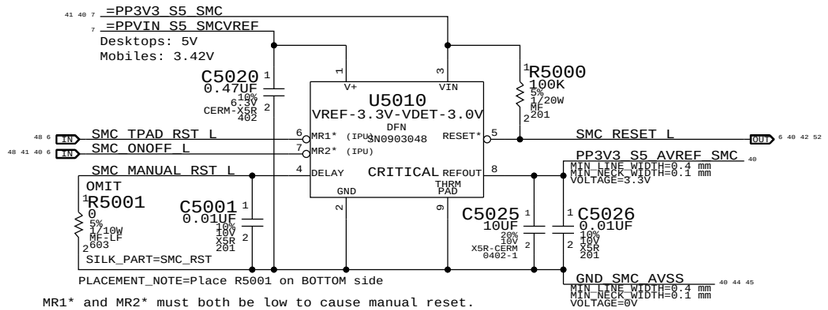
SYNC_MASTER=J30_MLB SYNC_DATE=07/26/2011

PAGE TITLE: SMC

Apple Inc.

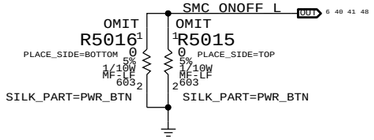
DRAWING NUMBER: 051-9276 SIZE: D
REVISION: 2.7.0
BRANCH:
PAGE: 49 OF 109
SHEET: 40 OF 72

SMC Reset "Button", Supervisor & AVREF Supply



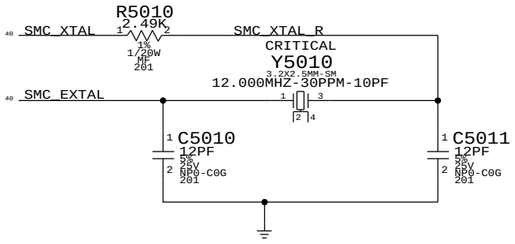
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.
NOTE: Internal pull-ups are to VIN, not V+.

Debug Power "Buttons"



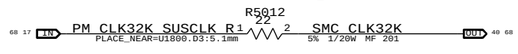
SMC Crystal Circuit

SMC USB Clock require these crystal values:5,6,8,10,12,16,18,20,24,25 MHz



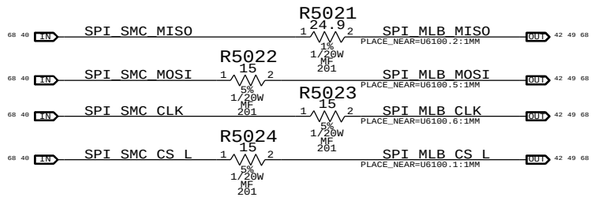
Note:
ADC10 and ADC11 are shared with comparators on Stack Board.

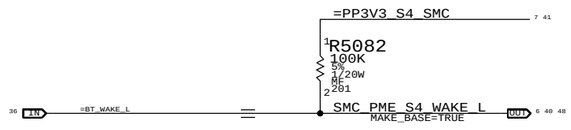
SMC_ADC0	SMC_CPU_VSENSE	MAKE_BASE=TRUE
SMC_ADC1	SMC_CPU_ISENSE	MAKE_BASE=TRUE
SMC_ADC2	SMC_VCCSA_VSENSE	MAKE_BASE=TRUE
SMC_ADC3	SMC_DCIN_VSENSE	MAKE_BASE=TRUE
SMC_ADC4	SMC_DCIN_ISENSE	MAKE_BASE=TRUE
SMC_ADC5	SMC_PBUS_VSENSE	MAKE_BASE=TRUE
SMC_ADC6	SMC_HDD_ISENSE	MAKE_BASE=TRUE
SMC_ADC7	SMC_BMON_ISENSE	MAKE_BASE=TRUE
SMC_ADC8	SMC_HS_COMPUTING_ISENSE	MAKE_BASE=TRUE
SMC_ADC9	SMC_OTHER_HI_ISENSE	MAKE_BASE=TRUE
SMC_ADC10	SMC_1V5S3_ISENSE	MAKE_BASE=TRUE
SMC_ADC11	SMC_CPUVCCIO_ISENSE	MAKE_BASE=TRUE
SMC_ADC12	SMC_GFX_VSENSE	MAKE_BASE=TRUE
SMC_ADC13	SMC_CPU_SA_ISENSE	MAKE_BASE=TRUE
SMC_ADC14	SMC_3V3S0_ISENSE	MAKE_BASE=TRUE
SMC_ADC15	SMC_WLAN_ISENSE	MAKE_BASE=TRUE
SMC_ADC16	SMC_LCDBKLT_ISENSE	MAKE_BASE=TRUE
SMC_ADC17	NC_SCM_ADC17	MAKE_BASE=TRUE
SMC_ADC18	SMC_GFX_ISENSE	MAKE_BASE=TRUE
SMC_ADC19	NC_SMC_ADC19	MAKE_BASE=TRUE
SMC_ADC20	NC_SMC_ADC20	MAKE_BASE=TRUE
SMC_ADC21	NC_SMC_ADC21	MAKE_BASE=TRUE
SMC_ADC22	NC_SMC_ADC22	MAKE_BASE=TRUE
SMC_ADC23	SMC_ADC23	MAKE_BASE=TRUE
SMC_GFX_OVERTEMP	NC_SMC_GFX_OVERTEMP	MAKE_BASE=TRUE
SMC_GFX_THROTTLE_L	NC_SMC_GFX_THROTTLE_L	MAKE_BASE=TRUE
SMC_FAN_1_CTL	NC_SMC_FAN_1_CTL	MAKE_BASE=TRUE
SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH	MAKE_BASE=TRUE
ENET_ASF_GPIO	NC_ENET_ASF_GPIO	MAKE_BASE=TRUE
SMC_MPM5_LED_PWR	NC_SMC_MPM5_LED_PWR	MAKE_BASE=TRUE
SMC_MPM5_LED_CHG	NC_SMC_MPM5_LED_CHG	MAKE_BASE=TRUE
SYS_TDM_ONEWIRE	NC_SYS_TDM_ONEWIRE	MAKE_BASE=TRUE
SMC_DP_HPD_L	NC_SMC_DP_HPD_L	MAKE_BASE=TRUE
=CHGR_ACOK	SMC_BC_ACOK	MAKE_BASE=TRUE
HISIDE_ISENSE_OC	NC_HISIDE_ISENSE_OC	MAKE_BASE=TRUE
SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL	MAKE_BASE=TRUE
SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA	MAKE_BASE=TRUE
BDV_BKL_PWM	NC_BDV_BKL_PWM	MAKE_BASE=TRUE
SMC_PME_S4_DARK_L	=TBT_WAKE_L	MAKE_BASE=TRUE
SMC_T25_EN_L	NC_SMC_T25_EN_L	MAKE_BASE=TRUE



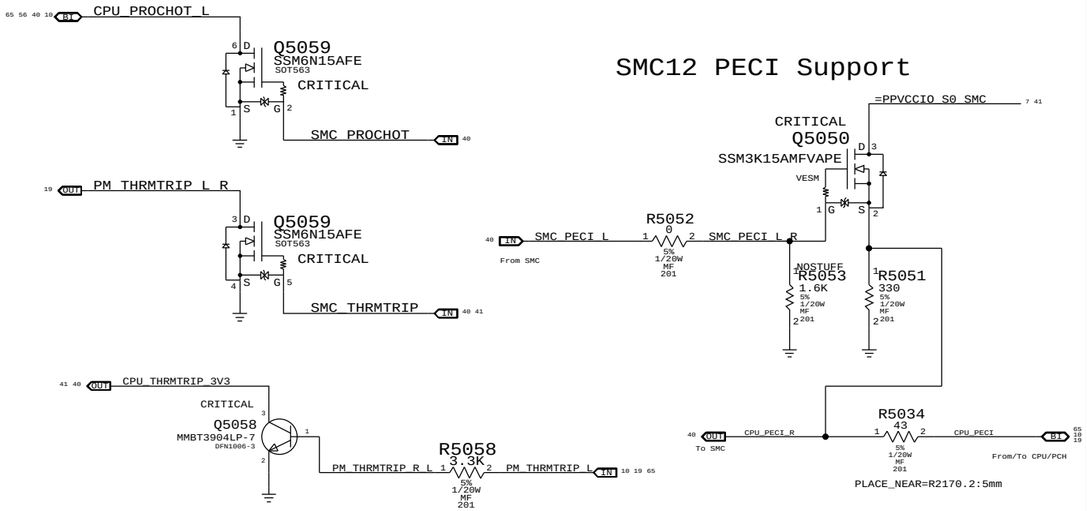
SMC12 SPI Support

Series resistors are no stuffed until the topology of 2 SPI Masters are verified.



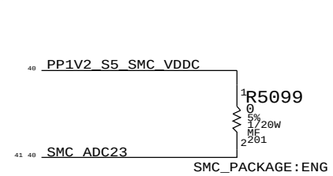


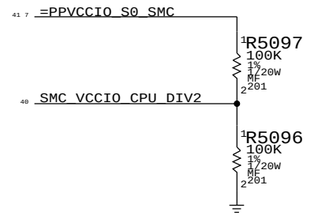
SMC12 PECI Support



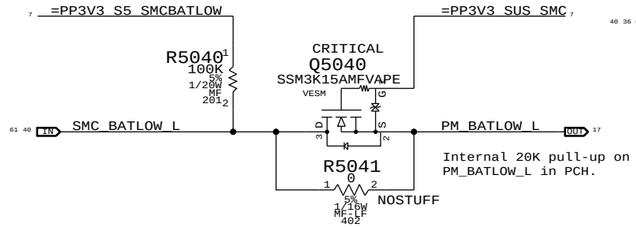
SMC12 Eng Pkg Support

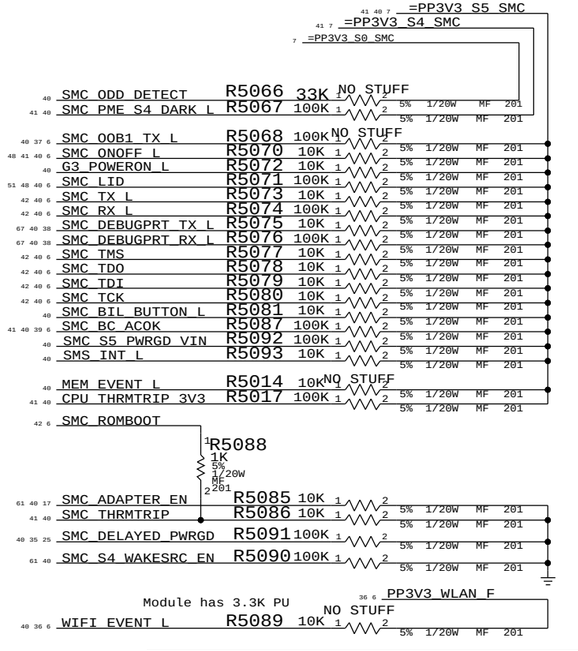
Eng Package requires 1.2V ON SMC_ADC23 pin.





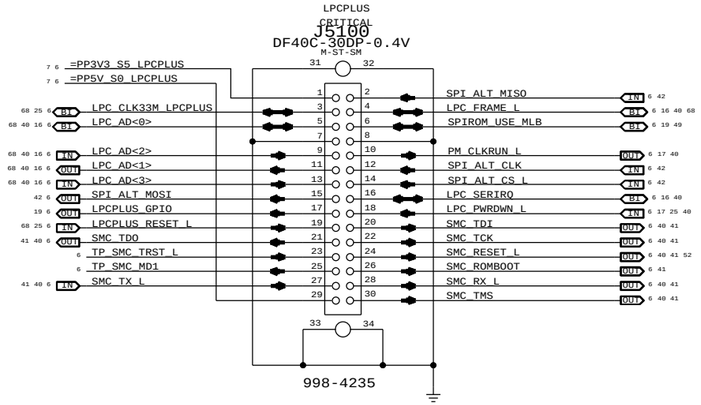
BATLOW# Isolation



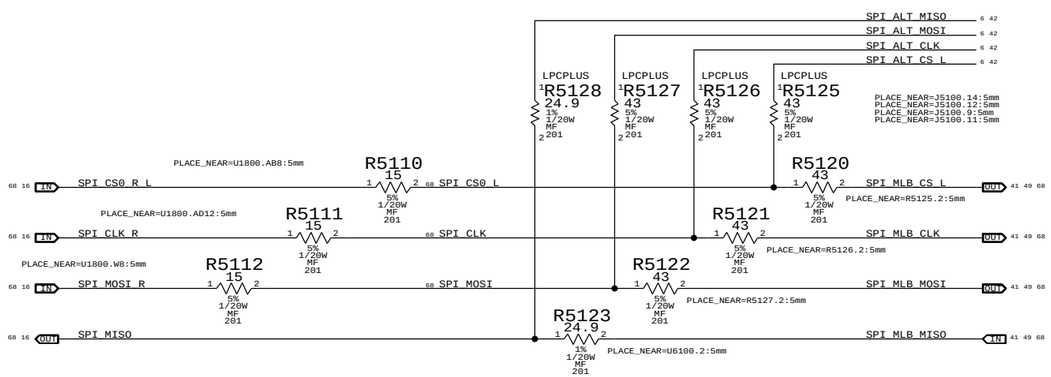


SYNC_MASTER=J13_MLB
SYNC_DATE=10/06/2011
PAGE TITLE: SMC Support
Apple Inc.
DRAWING NUMBER: 051-9276
SIZE: D
REVISION: 2.7.0
BRANCH:
PAGE: 50 OF 109
SHEET: 41 OF 72

LPC+SPI Connector



SPI Bus Series Termination



SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE

LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D

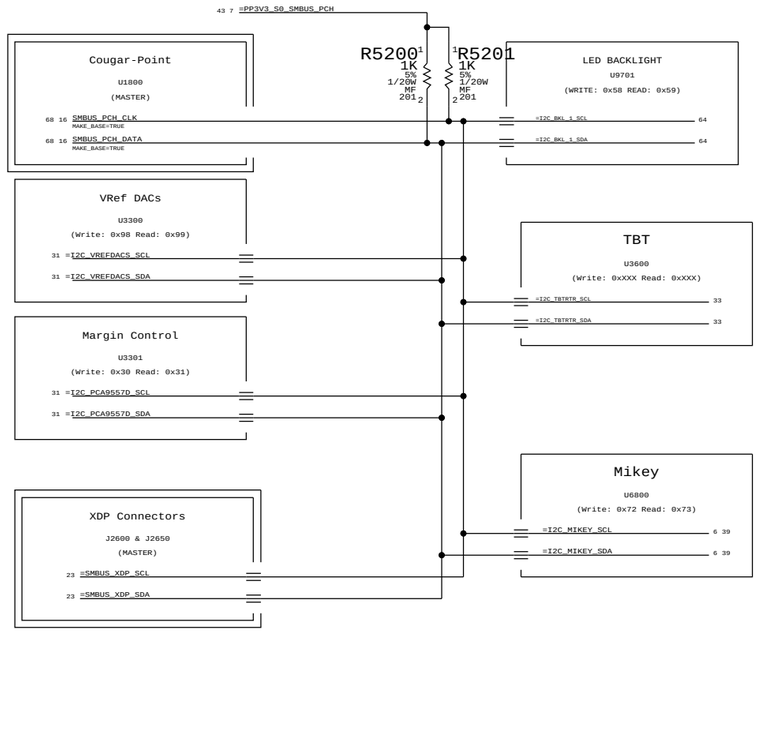
REVISION 2.7.0

BRANCH

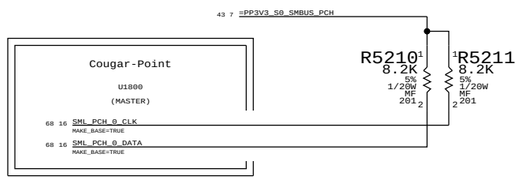
PAGE 51 OF 109

SHEET 42 OF 72

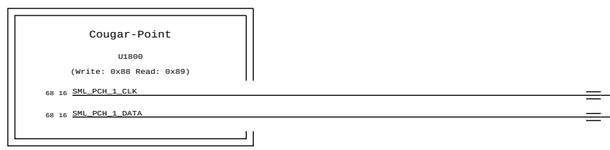
PCH S0 SMBus "0" Connections



PCH S0 "SMLink 0" Connections

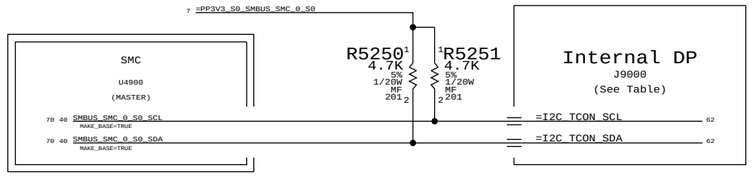


PCH S0 "SMLink 1" Connections



SMLink 1 is slave port to
access PCH

SMC "0" SMBus S0 Connections



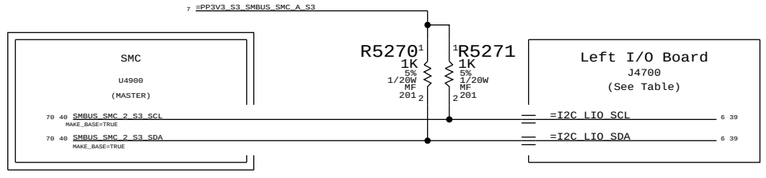
(* = Multiple options)

Internal DP

	K21		K78		
	Samsung	LGD	Samsung	LGD	AUO
Analogix T-con - (Write: 0x7B/0x87 Read: 0x7C/0x88)	N	Y	*	Y	*
Parade T-con - (0x10-0x1F or 0x30-0x3F)	Y	N	*	N	*
DVR - (Write: 0x4E Read: 0x4F)	Y	Y	Y	Y	N

SMC "2" SMBus S3 Connections

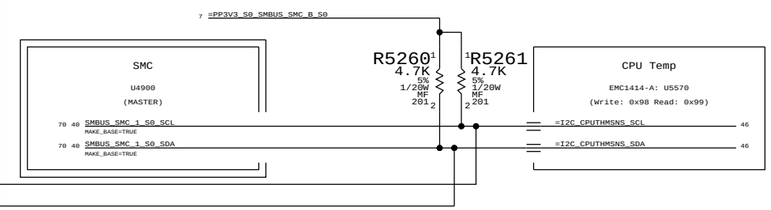
NOTE: SMC RMT bus remains powered and may be active in S3 state



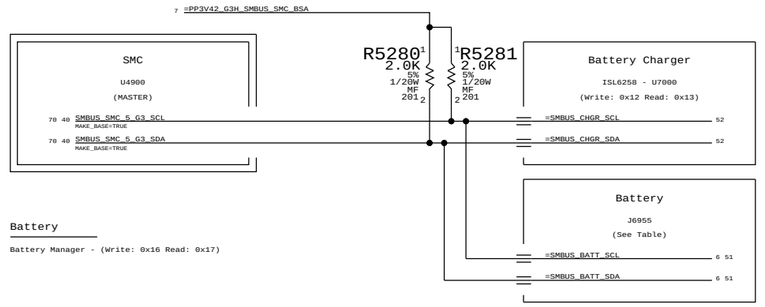
Left I/O Board

ALS - (write: 0x72 Read: 0x73)
Finstack Temp - (Write: 0x92 Read: 0x93)

SMC S0 "1" SMBus Connections



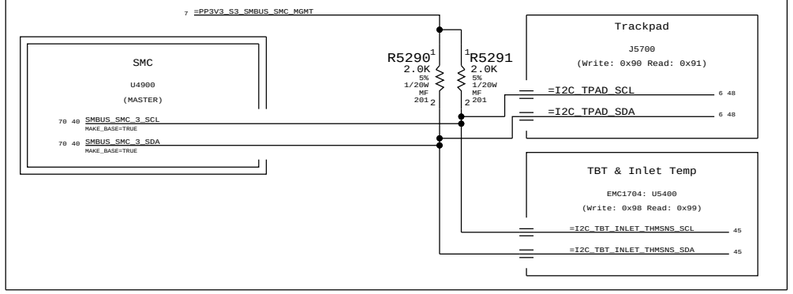
SMC "5" SMBus G3H Connections



Battery

Battery Manager - (Write: 0x16 Read: 0x17)

SMC "3" SMBus S3 Connections



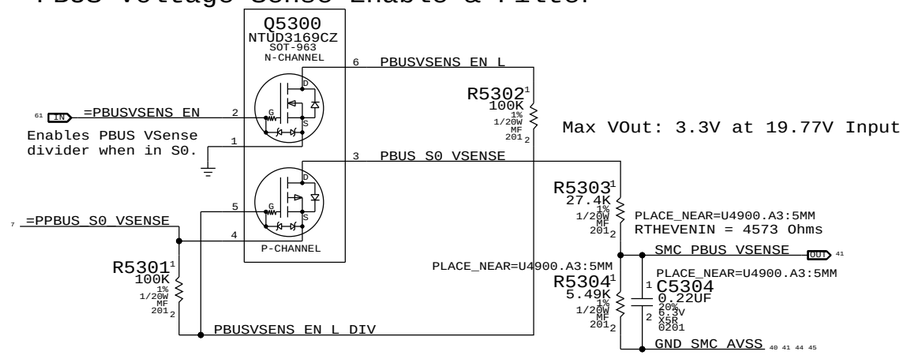
SYNC_MASTER=J13_MLB SYNC_DATE=10/05/2011

PAGE TITLE
SMBus Connections

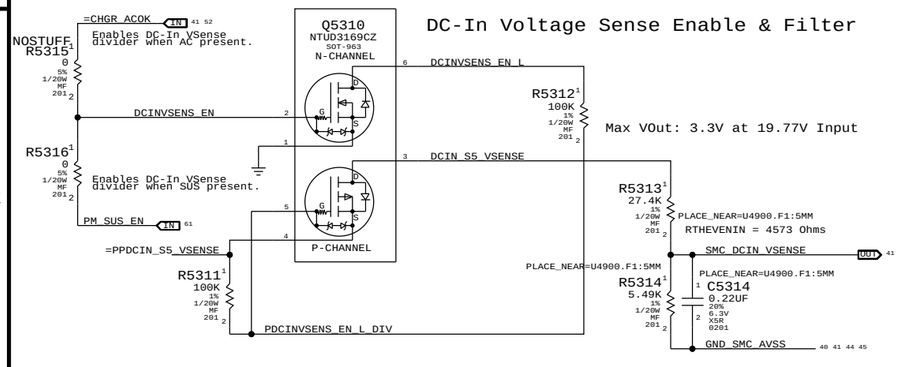
Apple Inc.

DRAWING NUMBER 051-9276 SIZE D
REVISION 2.7.0
BRANCH
PAGE 52 OF 109
SHEET 43 OF 72

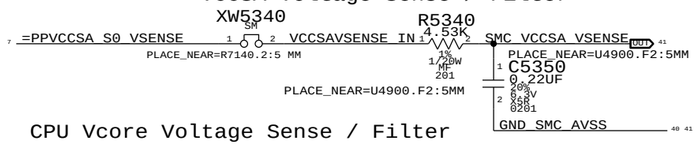
PBUS Voltage Sense Enable & Filter



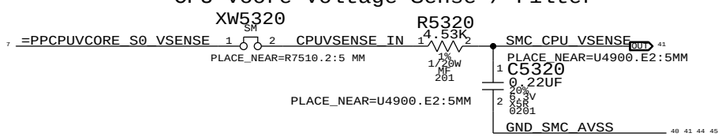
DC-In Voltage Sense Enable & Filter



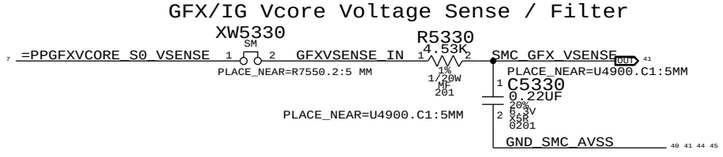
VCCSA Voltage Sense / Filter



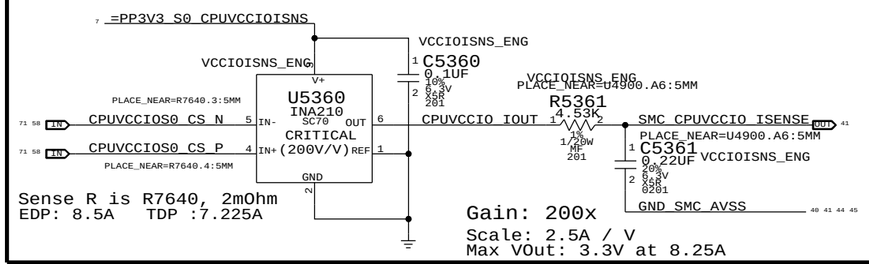
CPU Vcore Voltage Sense / Filter



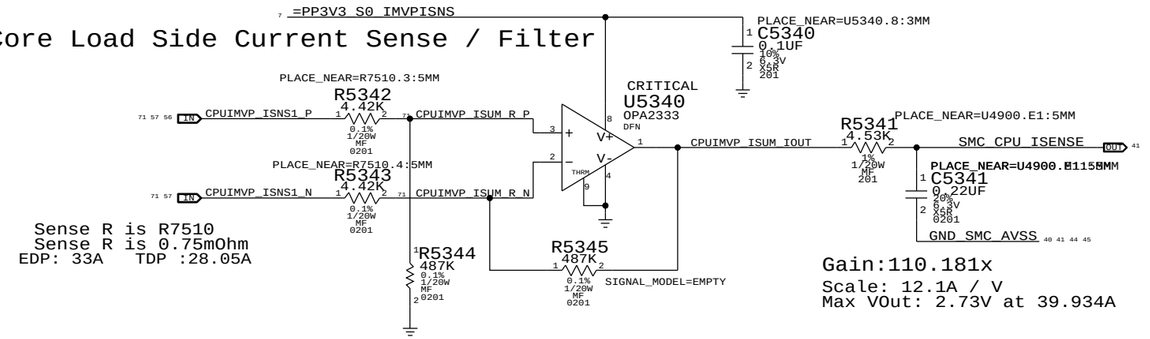
GFX/IG Vcore Voltage Sense / Filter



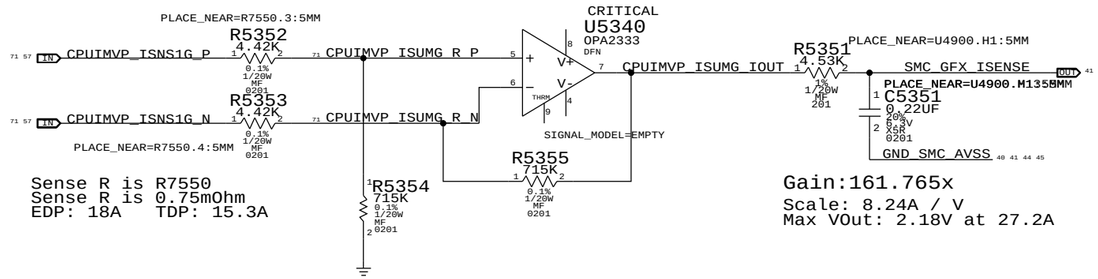
CPU 1.05V VCCIO Current Sense / Filter



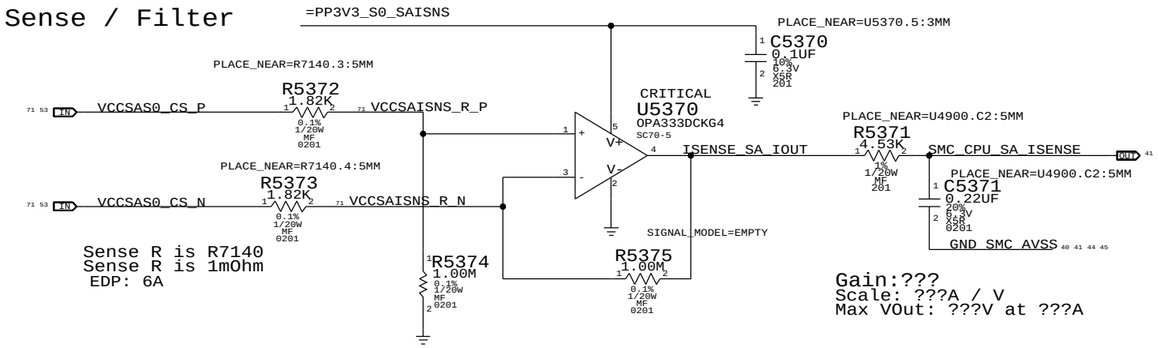
CPU VCore Load Side Current Sense / Filter



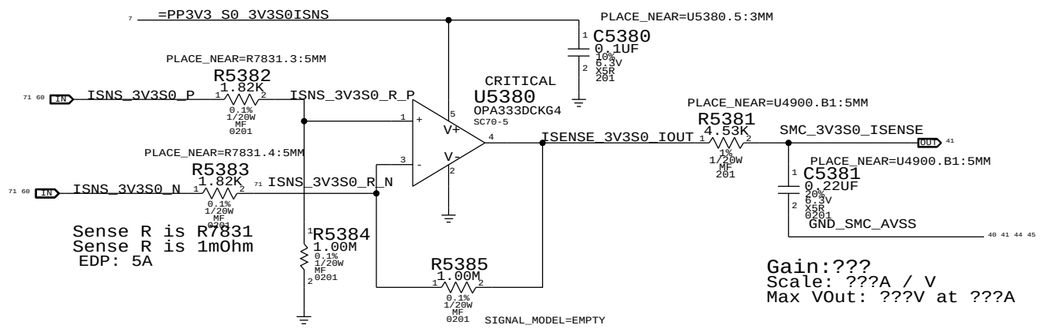
GFX/IG VCore Load Side Current Sense / Filter



CPU SA Current Sense / Filter



3.3V S0 FET Current Sense / Filter



SYNC_MASTER=J13_MLB SYNC_DATE=09/15/2011

PAGE TITLE: Voltage & Load Side Current Sensing

Apple Inc.

DRAWING NUMBER: 051-9276 SIZE: D

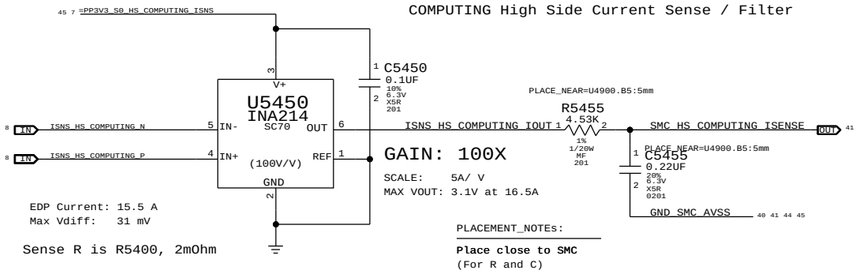
REVISION: 2.7.0

BRANCH:

PAGE: 53 OF 109

SHEET: 44 OF 72

COMPUTING High Side Current Sense / Filter



GAIN: 100X

SCALE: 5A/ V

MAX VOUT: 3.1V at 16.5A

EDP Current: 15.5 A

Max Vdiff: 31 mV

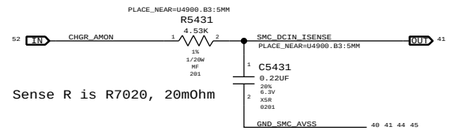
Sense R is R5400, 2mOhm

PLACEMENT_NOTES:

Place close to SMC

(For R and C)

DC-IN (AMON) Current Sense Filter



Sense R is R7020, 20mOhm

DC-In AMON

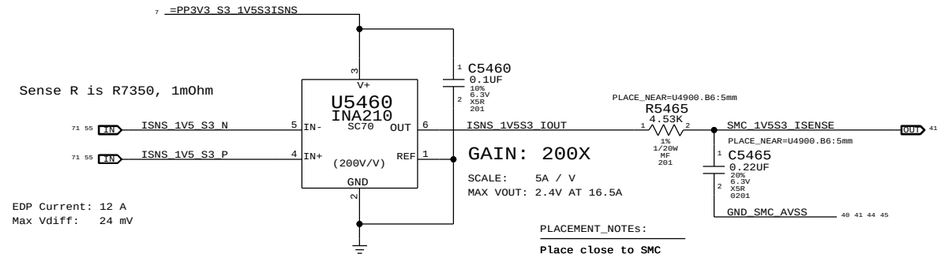
ISL6259 Gain: 20x

Scale: 2.5A / V

Max VOut: 1.4V at 8.25A

EDP Current: 3.5A

DDR3 1V5R1V35 Current Sense / Filter



Sense R is R7350, 1mOhm

EDP Current: 12 A

Max Vdiff: 24 mV

GAIN: 200X

SCALE: 5A / V

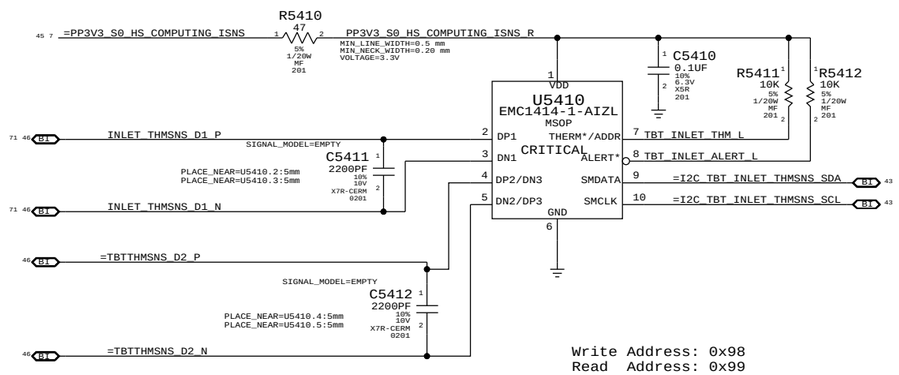
MAX VOUT: 2.4V AT 16.5A

PLACEMENT_NOTES:

Place close to SMC

(For R and C)

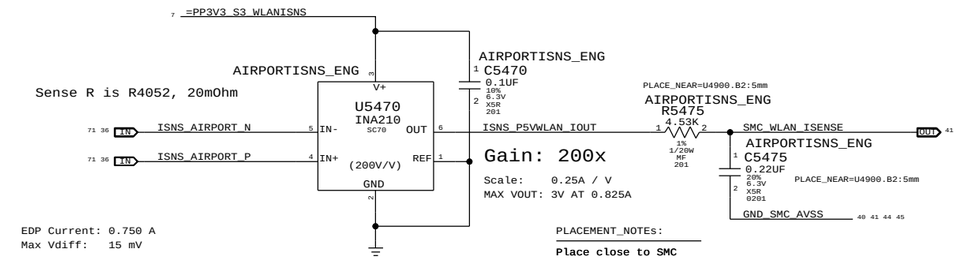
TBT/Inlet Temp Sensor



Write Address: 0x98

Read Address: 0x99

AirPort Current Sense / Filter



Sense R is R4052, 20mOhm

EDP Current: 0.750 A

Max Vdiff: 15 mV

Gain: 200x

Scale: 0.25A / V

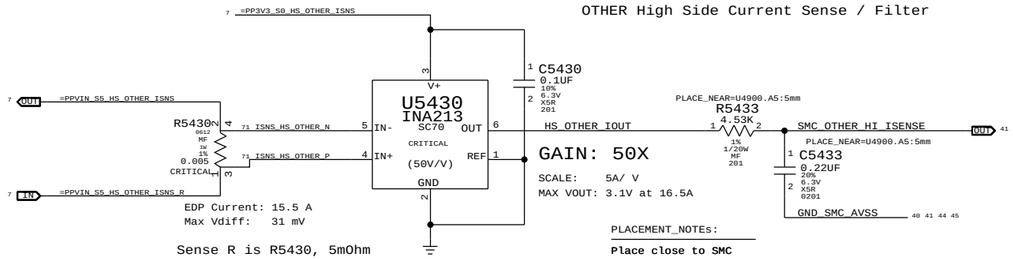
MAX VOUT: 3V AT 0.825A

PLACEMENT_NOTES:

Place close to SMC

(For R and C)

OTHER High Side Current Sense / Filter



EDP Current: 15.5 A

Max Vdiff: 31 mV

Sense R is R5430, 5mOhm

GAIN: 50X

SCALE: 5A/ V

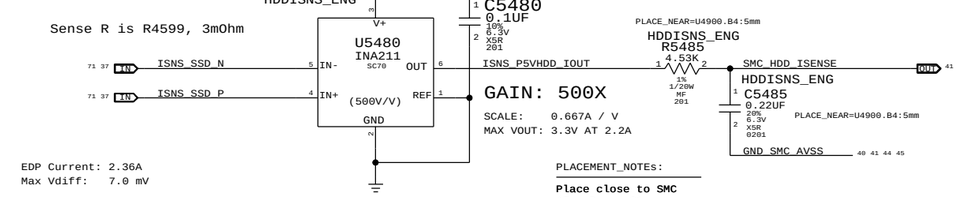
MAX VOUT: 3.1V at 16.5A

PLACEMENT_NOTES:

Place close to SMC

(For R and C)

HDD Current Sense / Filter



Sense R is R4599, 3mOhm

EDP Current: 2.36A

Max Vdiff: 7.0 mV

GAIN: 500X

SCALE: 0.667A / V

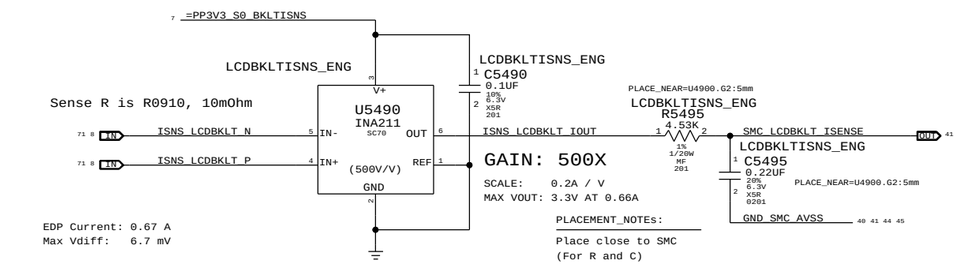
MAX VOUT: 3.3V AT 2.2A

PLACEMENT_NOTES:

Place close to SMC

(For R and C)

LCD Backlight Driver Input Current Sense / Filter



Sense R is R0910, 10mOhm

EDP Current: 0.67 A

Max Vdiff: 6.7 mV

GAIN: 500X

SCALE: 0.2A / V

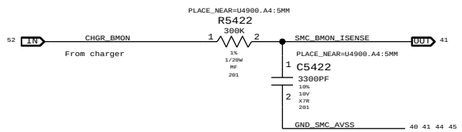
MAX VOUT: 3.3V AT 0.66A

PLACEMENT_NOTES:

Place close to SMC

(For R and C)

CHARGER BMON High Side (BATTERY DISCHAEGE) Current Sense, MUX & Filter



Charger BMON (Production) Solution

ISL6259 Gain: 36x

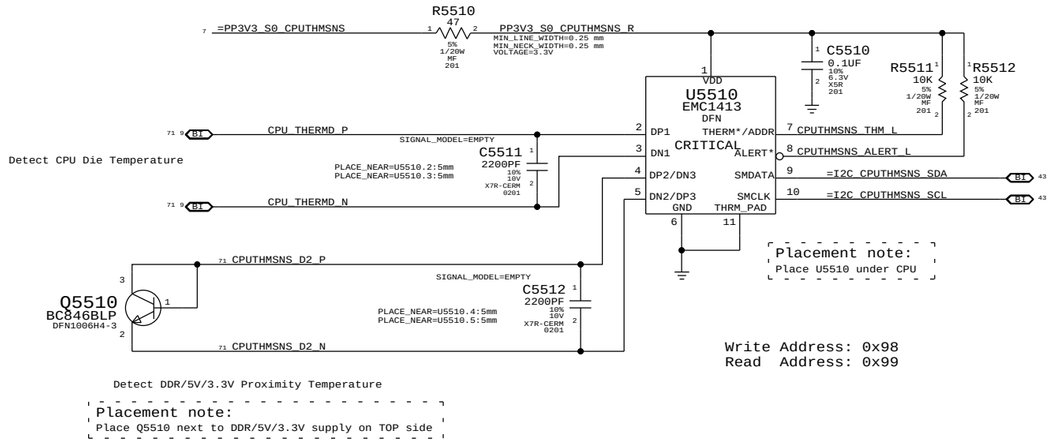
Scale: 2.78A / V

Max VOut: 3.3V at 9.167A

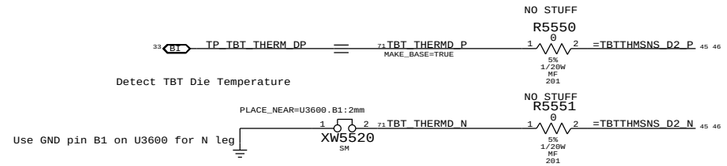
EDP Current: 310A

SYNC_MASTER=J13_MLB	SYNC_DATE=09/15/2011
PAGE TITLE: High Side Current Sensing	
Apple Inc.	DRAWING NUMBER: 051-9276 SIZE: D
	REVISION: 2.7.0
	BRANCH:
	PAGE: 54 OF 109
	SHEET: 45 OF 72

CPU Proximity Sensor



TBT Die

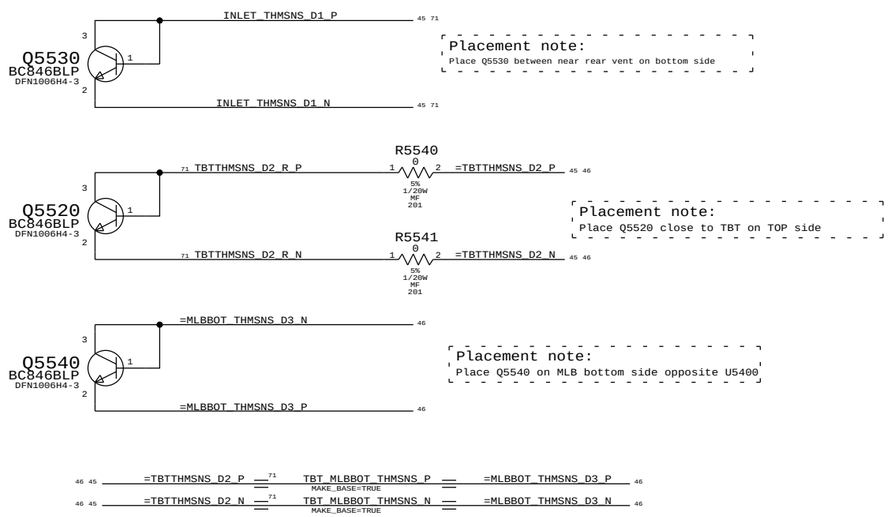


To connect Die Sensor, Stuff R5550 & R5551, No stuff R5540 & R5541
To connect Proximity Sensor, Stuff R5540 & R5541, No Stuff R5550,R5551

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5361		VCCIOISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5475		AIRPORTISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5485		HDDISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5495		LCDBKLTISNS_PROD

Replacing caps with 100K PD on ISENSE SMC inputs

TBT,MLB Bottom & Inlet Proximity Sensors



SYNC_MASTER=J13_MLB SYNC_DATE=08/30/2011

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: 051-9276 SIZE: D

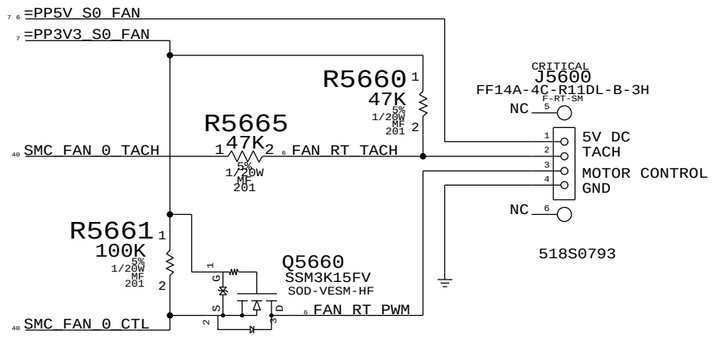
REVISION: 2.7.0

BRANCH:

PAGE: 55 OF 109

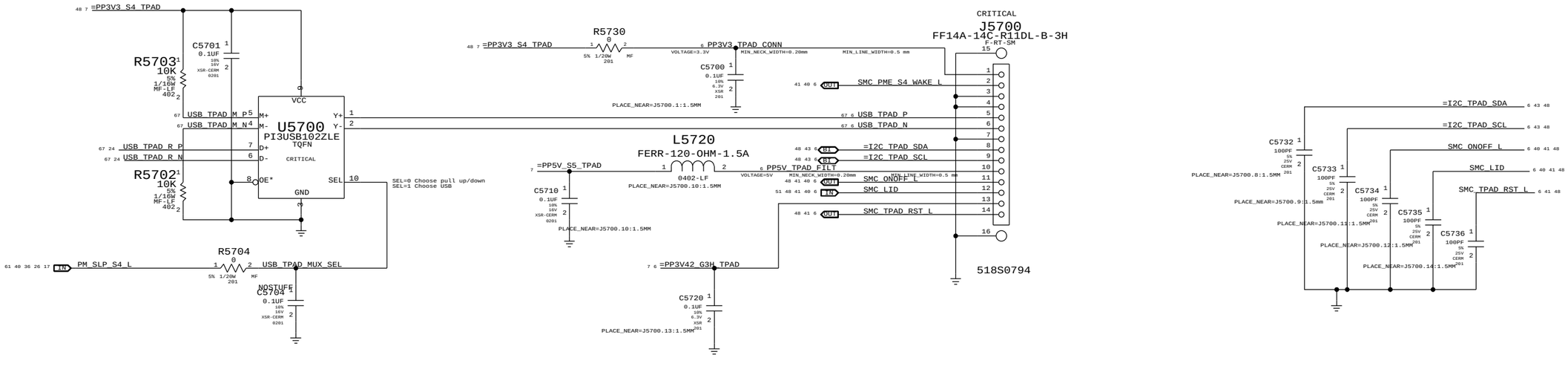
SHEET: 46 OF 72

FAN CONNECTOR

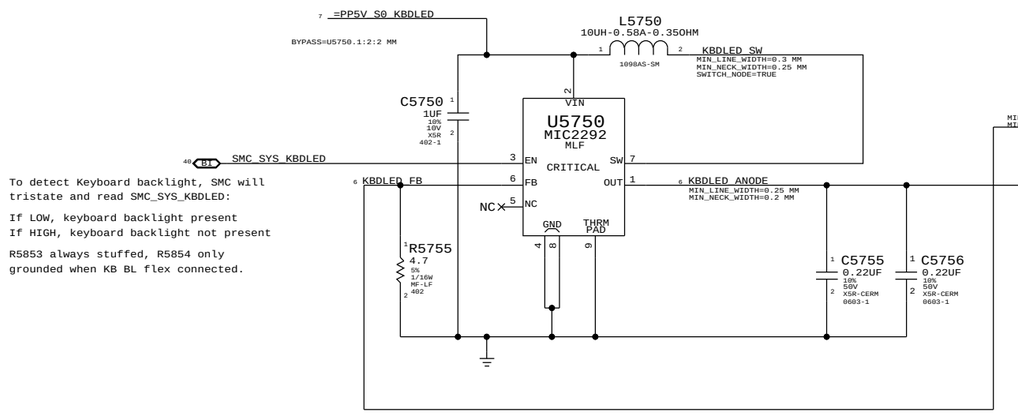


SYNC MASTER=K21_MLB	SYNC DATE=12/13/2010
PAGE TITLE	Fan
Apple Inc.	DRAWING NUMBER 051-9276 · SIZE D
	REVISION 2.7.0
	BRANCH
	PAGE 56 OF 109
	SHEET 47 OF 72

IPD Flex Connector



Keyboard Backlight Driver & Detection

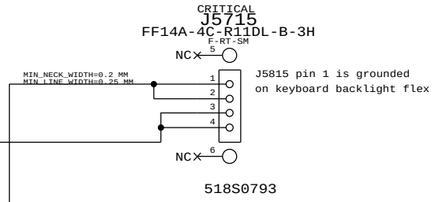


To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:

If LOW, keyboard backlight present
If HIGH, keyboard backlight not present

R5853 always stuffed, R5854 only grounded when KB BL flex connected.

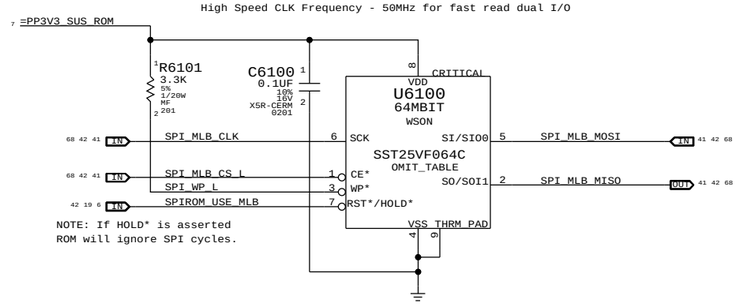
Keyboard Backlight Connector



J5815 pin 1 is grounded on keyboard backlight flex

SYNC_MASTER=K21_MLB	SYNC_DATE=12/13/2010
PAGE TITLE	IPD / KBD Backlight
Apple Inc.	DRAWING NUMBER 051-9276 · SIZE D
	REVISION 2.7.0
	BRANCH
	PAGE 57 OF 109
	SHEET 48 OF 72

DUAL I/O MODE (MODE 0 & 3) SUPPORTED
High Speed CLK Frequency - 50MHz for fast read dual I/O



NOTE: If HOLD* is asserted
ROM will ignore SPI cycles.

SYNC_MASTER=J13_MLB SYNC_DATE=10/13/2011

PAGE TITLE

SPI ROM

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D

REVISION 2.7.0

BRANCH

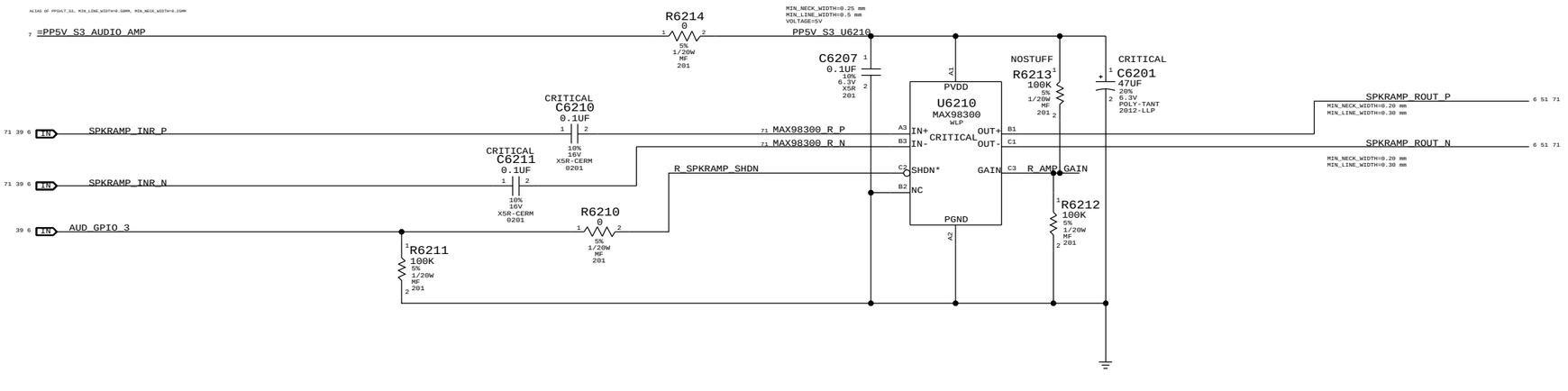
PAGE 61 OF 109

SHEET 49 OF 72

SPEAKER AMPLIFIERS

APN:353S2888

SPEAKER LOWPASS	80 HZ < FC < 132 HZ
GAIN	6DB



SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE

AUDI0: SPEAKER AMP

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D

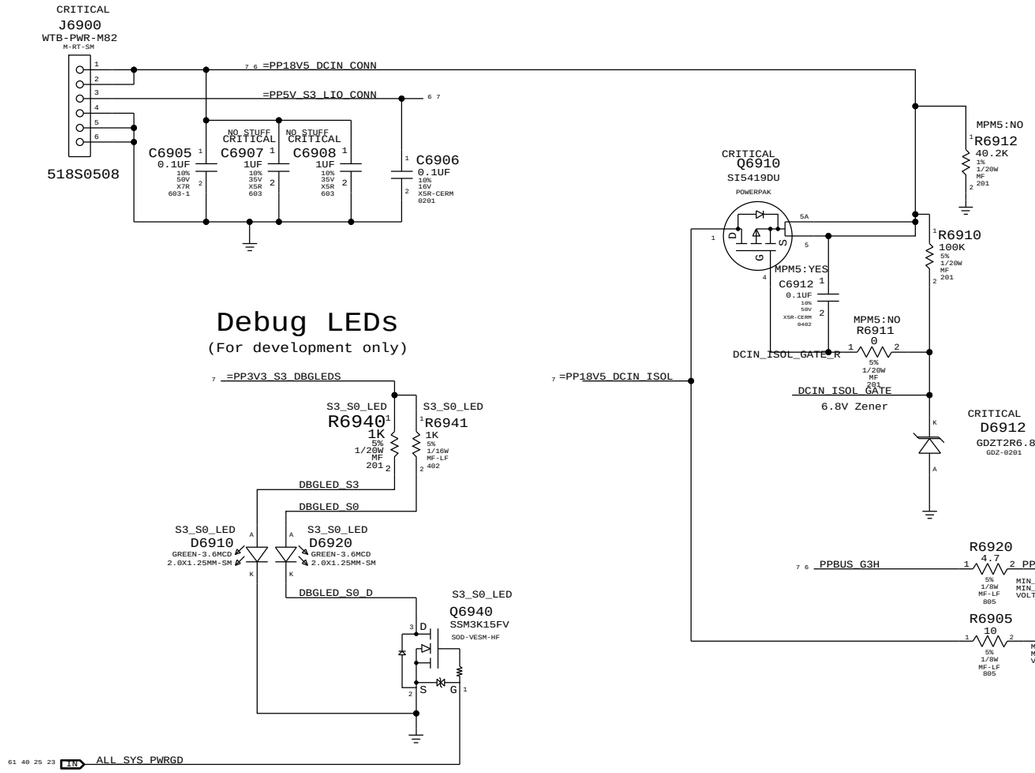
REVISION 2.7.0

BRANCH

PAGE 62 OF 109

SHEET 50 OF 72

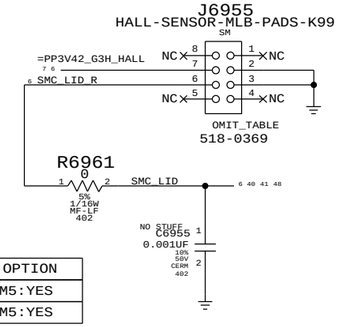
MLB to LIO Power Cable Connector



Debug LEDs

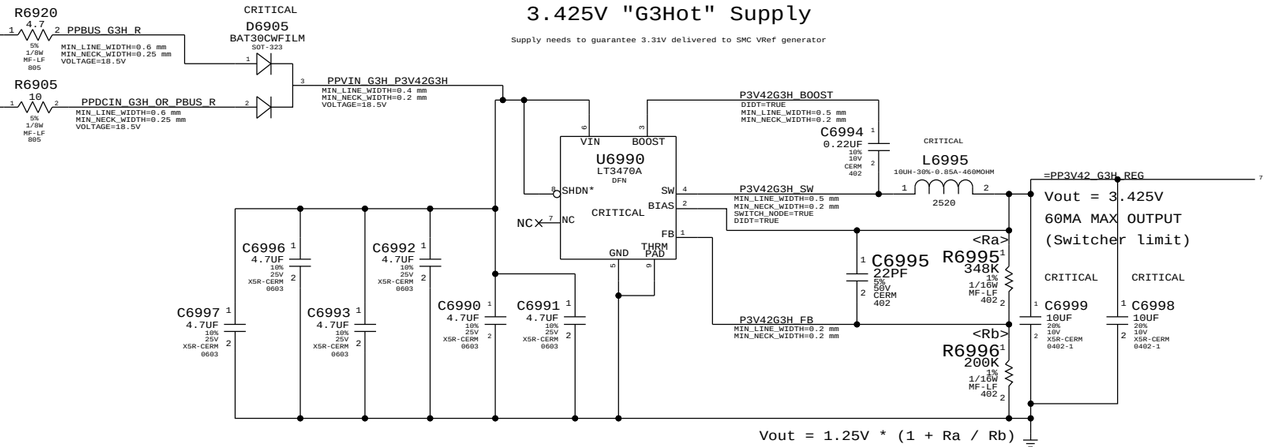
(For development only)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0560	1	RES,MF,90.9KOHM,1,1/20W,0201	R6912	CRITICAL	MPM5:YES
117S0008	1	RES,MF,100KOHM,1,1/20W,0201	R6911	CRITICAL	MPM5:YES

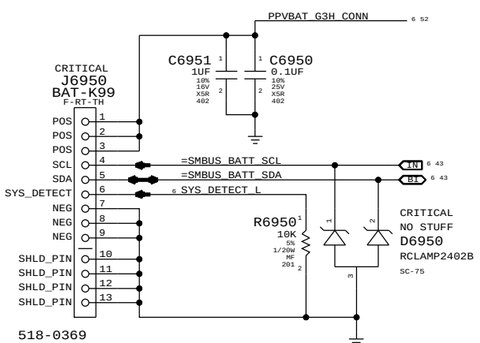


3.425V "G3Hot" Supply

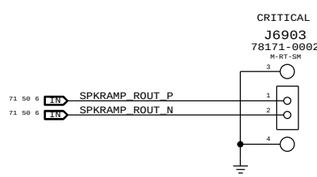
Supply needs to guarantee 3.31V delivered to SMC VRef generator



K99-Specific Battery Connector



Right Speaker Connector



SYNC_MASTER=K21_MLB SYNC_DATE=11/11/2011

PAGE TITLE: DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER: 051-9276 SIZE: D

REVISION: 2.7.0

BRANCH:

PAGE: 69 OF 109

SHEET: 51 OF 72

Need to stuff R7092 if either PP5V5_DCIN:YES or PP5V5_VDDP are used!

Reverse-Current Protection

This node is powered through body diodes:
* DCIN through Q7080.
* PBUS through Q7085, Charger TOP FETs and Q7055.

Inrush Limiter

FROM ADAPTER

=PPDCIN_S5_CHGR

CRITICAL Q7080 SI5419DU POWERPAK

CRITICAL Q7085 SI5419DU POWERPAK

R7080 100K 5% 1/20W MF 201

C7084 4.7UF 10% 25V X5R-CERM 0603

C7085 0.1UF 10% 25V X5R 402

R7085 470K 1% 1/20W MF 201

PPDCIN_G3H_OR_PBUS

PPDCIN_G3H_INRUSH

CHGR_SGATE_DIV

CHGR_AGATE_DIV

R7081 62K 5% 1/20W MF 201

R7086 332K 1% 1/20W MF 201

=PPDCIN_S5_CHGR_ISOL

CRITICAL D7005 BAT30CWFILM SOT-323

(CHGR_SGATE)

(CHGR_AGATE)

PP5V5_DCIN:NO

R7005 20 5% 1/10W MF-LF 603

PPCHGR_DCIN_D_R

(CHGR_DCIN)

ACIN pin threshold is 3.2V, +/- 50mV

DIVIDER SETS ACIN THRESHOLD AT 12.18V

Input impedance of ~40K meets sparkitecture requirements

30mA max load

PP5V1_CHGR_VDD

R7001 4.7 5% 1/16W MF-LF 402

PP5V1_CHGR_VDDP

C7001 1UF 10% 10V X5R 402

=PP3V42_G3H_CHGR

R7010 66.5K 1% 1/20W MF 201

NO STUFF R7002 100K 5% 1/20W MF 201

CRITICAL OMIT_TABLE

R7000 0 5% 1/20W MF 201

SMC_RESET_L

Float CELL for 1S

R7013 100 1% 1/20W MF 201

R7015 255K 1% 1/20W MF 201

R7011 23.7K 1% 1/20W MF 201

R7016 220 1% 1/20W MF 201

CHGR_VCOMP_R

CHGR_VNEG_R

C7015 470PF 10% 16V X5R-X7R 201

C7016 470PF 10% 16V X5R-X7R 201

C7050 0.47UF 10% 10V X5R 402

C7042 0.1UF 10% 6.3V X5R 201

C7011 0.01UF 10% 10V X5R 201

C7000 1UF 10% 10V X5R 402-1

C7002 1UF 10% 10V X5R 402

XW7000 SM

PLACE_NEAR=U7000.29:1mm
PLACE_NEAR=U7000.22:1mm

C7005 0.22UF 10% 50V X5R-CERM 0603-1

C7026 1000PF 10% 16V X7R 201

GND_CHGR_AGND

(GND)

(CHGR_CSO_P)

(CHGR_CSO_N)

(PPVBAT_G3H_CHGR_R)

U7000 ISL6259HRTZ TQFN

VHST	12		
SMB_RST_N	13		
SCL	11	=SMBUS_CHGR_SCL	
SDA	10	=SMBUS_CHGR_SDA	
VFRQ	4	CHGR_VFRQ	
CELL	6	CHGR_CELL	
ACIN	3	CHGR_ACIN	
ICOMP	5	CHGR_ICOMP	
VCOMP	7	CHGR_VCOMP	
VNEG	8	CHGR_VNEG	
CSOP	18	CHGR_CSO_P	
CSON	17	CHGR_CSO_N	
(AGND) THRM_PAD	29		
PGND	22		
VDD	19		
VDDP	20		
DCIN	2	CHGR_DCIN	
SGATE	26	CHGR_SGATE	
AGATE	1	CHGR_AGATE	
CSIP	28	CHGR_CSI_P	
CSIN	27	CHGR_CSI_N	
BOOT	25	CHGR_BOOT	
UGATE	24	CHGR_UGATE	
PHASE	23	CHGR_PHASE	
LGATE	21	CHGR_LGATE	
BGATE	16	CHGR_BGATE	
20V/V AMON	9	CHGR_AMON	OUT
36V/V BMON	15	CHGR_BMON	OUT
(0.6) ACOK	14	=CHGR_ACOK	OUT

R7021 10 5% 1/20W MF 201

R7022 10 5% 1/20W MF 201

C7020 0.047UF 10% 16V X7R 402

C7022 0.1UF 10% 25V X5R 402

C7021 0.1UF 10% 25V X5R 402

CHGR_CSI_R_P

CHGR_CSI_R_N

CRITICAL R7020 0.020 0.5% MF-LF 0612 1W

PPDCIN_G3H_CHGR

C7025 0.22UF 10% 10V CERM 402

CRITICAL Q7030 RJK03P0DPA WPAK

CRITICAL L7030 4.7UH-17A PIMC104T4R7MN-SM

SWITCH_NODE=TRUE DIDT=TRUE

Max Current = 8A

f = 400 kHz

TO SYSTEM

CRITICAL F7040 8AMP-24V 1206

=PPBUS_G3H

R7051 2.2 5% 1/20W MF 201

R7052 0 5% 1/20W MF 201

CHGR_CSO_R_P

CHGR_CSO_R_N

* R7051 HAS 2.2OHM TO COMPENSATE UNBALANCED VOLTAGE DUE TO DIFFERENT CURRENT ON _P AND _N. (FROM INTERSIL)

PPVBAT_G3H_CHGR_REG

CRITICAL C7040 62UF 20% 11V POLY CASE-B

CRITICAL C7041 62UF 20% 11V POLY CASE-B

CRITICAL C7043 62UF 20% 11V POLY CASE-B

C7045 1000PF 10% 16V X7R 201

PLACE_NEAR=L7030.2:1.5mm

R7050 0.01 0.5% 1W MF 0612-3

CRITICAL Q7055 SI7615DN PWRPK-1212-8

PPVBAT_G3H_CHGR_R

TO/FROM BATTERY

PPVBAT_G3H_CONN

C7017 10UF 10% 25V X5R 805

C7014 1UF 10% 25V X5R 603-1

C7013 0.1UF 10% 25V X5R 402

C7012 0.01UF 10% 50V X7R 402

5.5v "G3Hot" Supply For Erp Lot6 spec

NO STUFF R7092 0 5% 1/16W 402

PPCHGR_DCIN_D_R

CHGR_DCIN_D

C7090 4.7UF 10% 25V XSR-CERM 0603

U7090 LT3470A DFN

VIN BOOST SHDN* SW BIAS NC FB THRM GND PAD

P5V1_BOOST DIDT=TRUE

C7094 0.22UF 10% 16V CERM 402

CRITICAL L7095 10UH-30%-0.85A-460MOHM 2520

P5V1_SW

C7095 22PF 5% 50V CERM 201

P5V1_FB

<Ra> R7095 681K 1% 1/20W MF 201

<Rb> R7096 200K 1% 1/20W MF 201

CRITICAL C7098 10UF 20% 10V X5R 603

CRITICAL C7099 10UF 20% 10V X5R 603

Vout = 1.25V * (1 + Ra / Rb)

PP5V5_DCIN:YES

R7090 0 5% 1/16W 402

CHGR_DCIN

PP5V5_VDDP

R7091 0 5% 1/16W 402

PP5V1_CHGR_VDDP

PP5V5_CHGR_VDDP

Vout = 5.50V
200MA MAX OUTPUT
(Switcher limit)

C7030 33UF-0.060HM 20% 25V POLY-TANT CASE-D3L

C7031 33UF-0.060HM 20% 25V POLY-TANT CASE-D3L

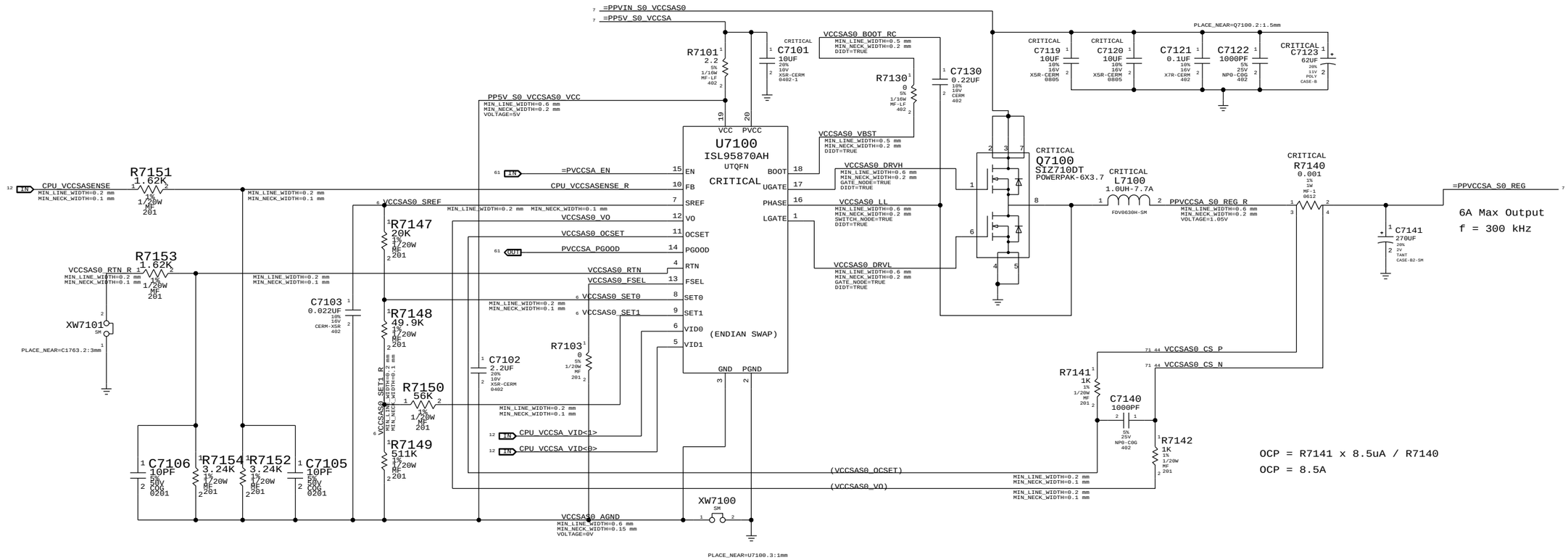
C7035 1UF 10% 25V X5R 603-1

C7036 1UF 10% 25V X5R 603-1

C7037 0.001UF 10% 50V X7R 402

PLACE_NEAR=Q7030.5:1.5mm

SYNC_MASTER	J13_MLB
SYNC_DATE	10/10/2013
PAGE TITLE	PBus Supply & Battery Charger
Apple Inc.	
DRAWING NUMBER	051-9276
SIZE	D
REVISION	2.7.0
BRANCH	
PAGE	70 OF 109
SHEET	52 OF 72



INTEL TABLE:

VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V
0	1	0.725V
1	1	0.675V

SYNC MASTER=J13_MLB SYNC DATE=09/01/2013

PAGE TITLE

System Agent Supply

Apple Inc.

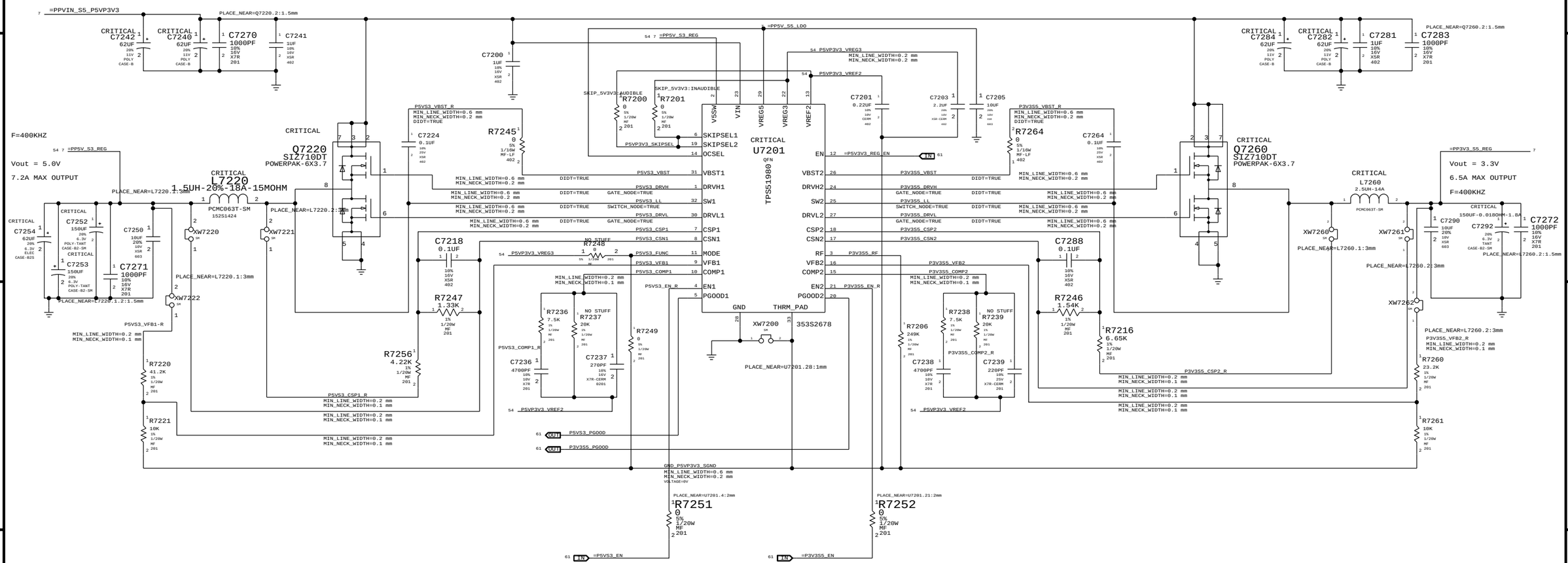
DRAWING NUMBER 051-9276 SIZE D

REVISION 2.7.0

BRANCH

PAGE 71 OF 109

SHEET 53 OF 72



SYNC_MASTER=J13_MLB SYNC_DATE=11/10/2011

PAGE TITLE

5V / 3.3V Power Supply

Apple Inc.

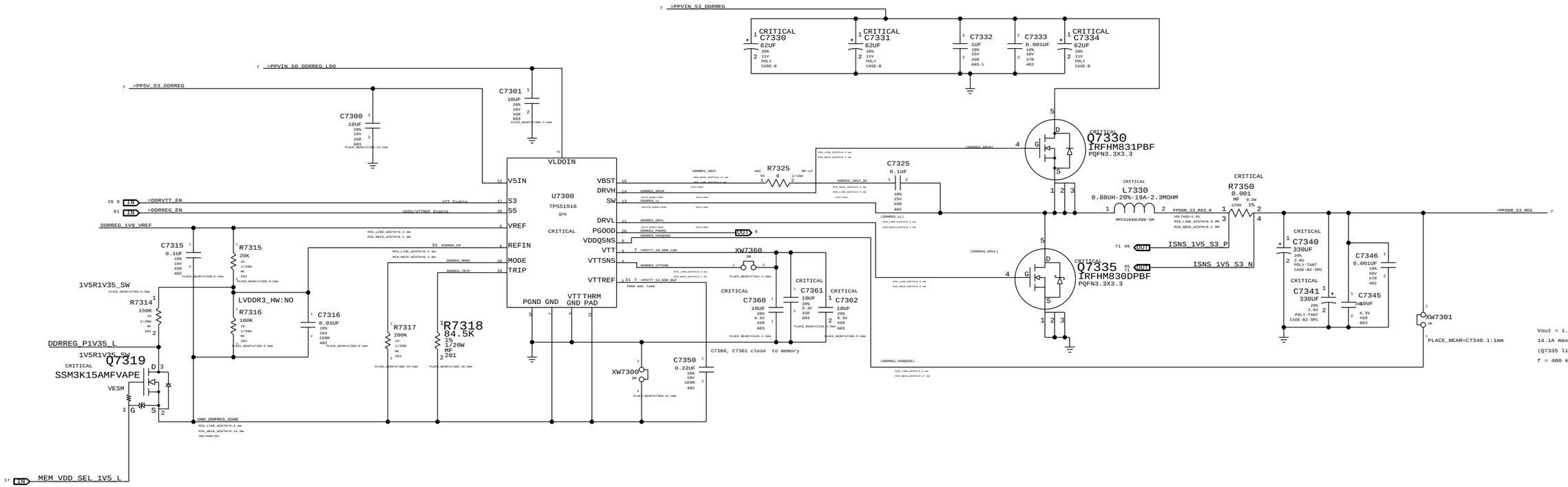
DRAWING NUMBER 051-9276 SIZE D

REVISION 2.7.0

BRANCH

PAGE 72 OF 109

SHEET 54 OF 72



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0460	1	RES,MF,60.4KOHM,1,1/20W,0201	R7316		LVDDR3_HW:YES

If LVDDR3_HW:NO is turned ON, switch R2821 & R7971 back to the original value for 1.5V DDR unless 1V5R1V35_SW is turned ON

SYNC_MASTER=J13_MLB SYNC_DATE=10/07/2013

PAGE TITLE

1.5V DDR3 Supply

Apple Inc.

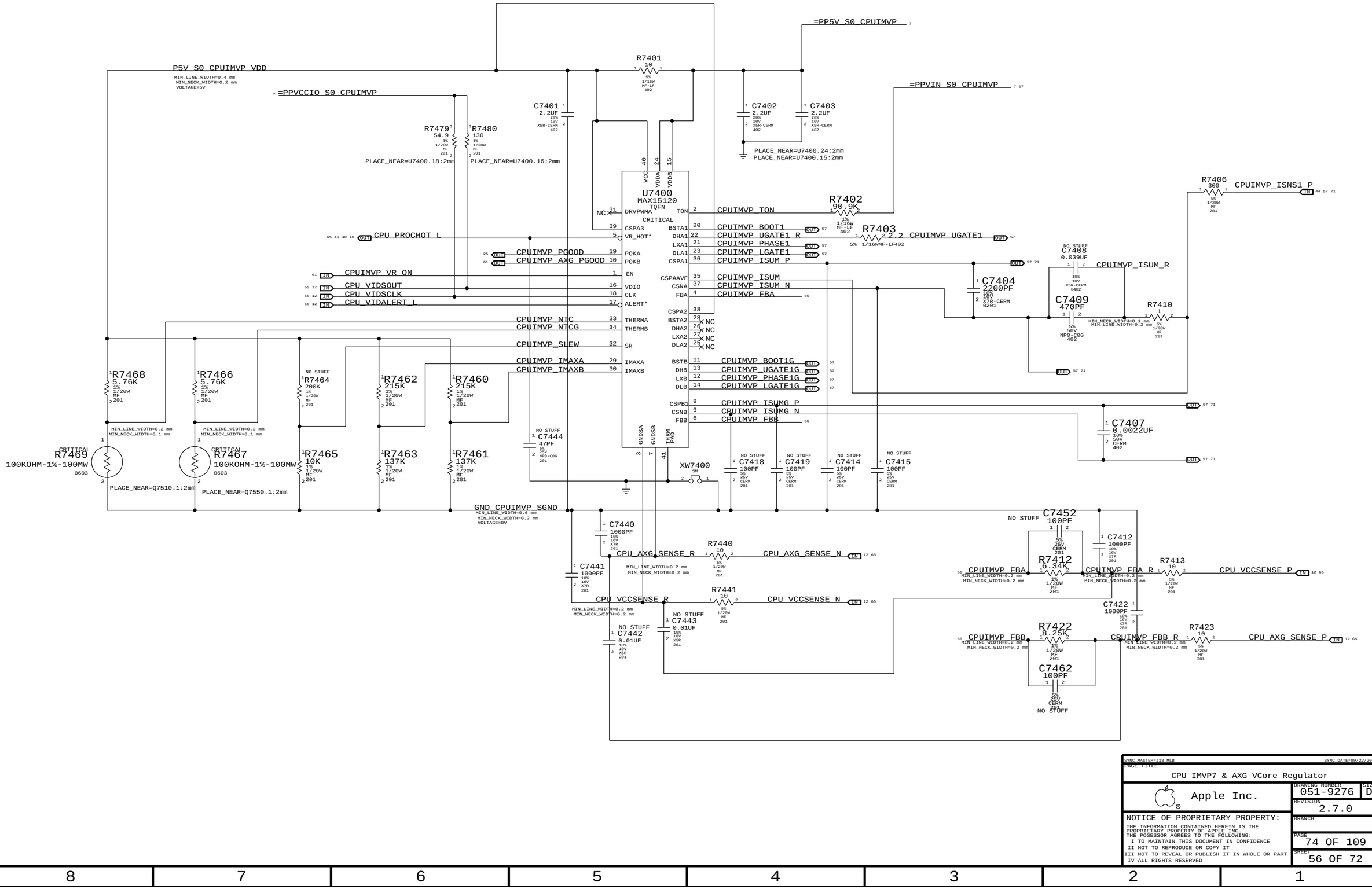
DRAWING NUMBER 051-9276 SIZE D

REVISION 2.7.0

BRANCH

PAGE 73 OF 109

SHEET 55 OF 72


P5V_S0_CPUIMVP_VDD
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
=PP5V_S0_CPUIMVP
=PPVCCIO_S0_CPUIMVP
=PPVIN_S0_CPUIMVP
R7401 10
C7401 2.2UF
C7402 2.2UF
C7403 2.2UF
R7479 54.9
R7480 130
PLACE_NEAR=U7400.18:2mm
PLACE_NEAR=U7400.16:2mm
PLACE_NEAR=U7400.24:2mm
PLACE_NEAR=U7400.15:2mm
U7400
MAX15120
TQFN
CRITICAL
CPU_PROCHOT_L
CPUIMVP_PGOOD
CPUIMVP_AXG_PGOOD
CPUIMVP_VR_ON
CPU_VIDSOUT
CPU_VIDSCLK
CPU_VIDALERT_L
CPUIMVP_NTC
CPUIMVP_NTCG
CPUIMVP_SLEW
CPUIMVP_IMAXA
CPUIMVP_IMAXB
CPUIMVP_TON
CPUIMVP_BOOT1
CPUIMVP_UGATE1_R
CPUIMVP_PHASE1
CPUIMVP_LGATE1
CPUIMVP_ISUM_P
CPUIMVP_ISUM
CPUIMVP_ISUM_N
CPUIMVP_FBA
CPUIMVP_BOOT1G
CPUIMVP_UGATE1G
CPUIMVP_PHASE1G
CPUIMVP_LGATE1G
CPUIMVP_ISUMG_P
CPUIMVP_ISUMG_N
CPUIMVP_FBB
R7402 90.9K
R7403 2.2
CPUIMVP_UGATE1
R7406 300
CPUIMVP_ISNS1_P
C7408 0.039UF
CPUIMVP_ISUM_R
C7404 2200PF
C7409 470PF
R7410 1
C7407 0.0022UF
R7468 5.76K
R7466 5.76K
R7464 200K
R7462 215K
R7460 215K
R7469 100KOHM-1%-100MW
R7467 100KOHM-1%-100MW
R7465 10K
R7463 137K
R7461 137K
C7444 47PF
C7418 100PF
C7419 100PF
C7414 100PF
C7415 100PF
XW7400
GND_CPUIMVP_SGND
C7440 1000PF
C7441 1000PF
C7442 0.01UF
C7443 0.01UF
R7440 10
R7441 10
CPU_AXG_SENSE_R
CPU_AXG_SENSE_N
CPU_VCCSENSE_R
CPU_VCCSENSE_N
C7452 100PF
C7412 1000PF
R7412 6.34K
R7413 10
C7422 1000PF
R7422 8.25K
R7423 10
C7462 100PF
CPUIMVP_FBA
CPUIMVP_FBA_R
CPUIMVP_FBB
CPUIMVP_FBB_R
CPU_VCCSENSE_P
CPU_AXG_SENSE_P
SYNC_MASTER=J13_MLB
SYNC_DATE=09/22/2011
PAGE TITLE
CPU IMVP7 & AXG VCore Regulator
Apple Inc.
DRAWING NUMBER 051-9276
SIZE D
REVISION 2.7.0
BRANCH
PAGE 74 OF 109
SHEET 56 OF 72
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

CPU=IV Bridge ULV, AXG=GT2

PHASE 1

=PPVIN_S0_CPUIMVP

C7513 62UF 20% 11V POLY CASE-B
C7514 62UF 20% 11V POLY CASE-B
C7515 10UF 20% 25V X5R-CERM 0603
C7516 10UF 20% 25V X5R-CERM 0603
C7517 1UF 10% 16V X5R 402
C7518 0.001UF 10% 50V X7R 402
C7519 0.001UF 10% 50V X7R 402
THESE TWO CAPS ARE FOR EMC
C7540 62UF 20% 11V POLY CASE-B
C7541 62UF 20% 11V POLY CASE-B
C7510 62UF 20% 11V POLY CASE-B
C7520 62UF 20% 11V POLY CASE-B

CPUIMVP_BOOT1_RC
R7511 0 5% 1/16W MF-LF 402
C7511 0.22UF 10% 10V CERM 402

376S0984
Q7510
IRF6811STRPBF
SO

CPUIMVP_BOOT1
CPUIMVP_UGATE1
CPUIMVP_PHASE1
CPUIMVP_LGATE1

376S0985
Q7520
IRF6894MTRPBF
DIRECTFET-MX

L7510
0.36UH-20%-30A-1.2MOHM
PIMB104T-SM
152S1323

PPVCORE_S0_CPU_PH1

R7510 0.00075 1% 1W MF 0612
=PPVCORE_S0_CPU_REG
CPUIMVP_ISNS1_N
CPUIMVP_ISNS1_P
R7513 46.4 1% 1/20W MF 201
R7514 10 1% 1/20W MF 201
CPUIMVP_ISUM_N
C7571 2200PF 10% 16V X7R-CERM 0201 NO STUFF
CPUIMVP_ISUM_P

AXG PHASE

=PPVIN_S0_CPUAXG

C7553 62UF 20% 11V POLY CASE-B
C7554 62UF 20% 11V POLY CASE-B
C7555 10UF 20% 25V X5R-CERM 0603
C7556 10UF 20% 25V X5R-CERM 0603
C7557 1UF 10% 16V X5R 402
C7558 0.001UF 10% 50V X7R 402
C7559 0.001UF 10% 50V X7R 402
THESE TWO CAPS ARE FOR EMC
C7560 62UF 20% 11V POLY CASE-B

CPUIMVP_UGATE1G_R
CPUIMVP_BOOT1G_RC
R7551 10 5% 1/16W MF-LF 402
C7551 0.22UF 10% 10V CERM 402

376S1005
Q7550
CSD58872Q5D
SON5X6

CPUIMVP_BOOT1G
CPUIMVP_UGATE1G
R7555 4.7 5% 1/16W MF-LF 402
CPUIMVP_PHASE1G
CPUIMVP_LGATE1G

CPUIMVP_VSWG
CPUIMVP_AXG_SNUBB
R7552 2.2 5% 1/10W MF-LF 603 NOSTUFF
C7552 0.001UF 10% 50V CERM 402 NOSTUFF

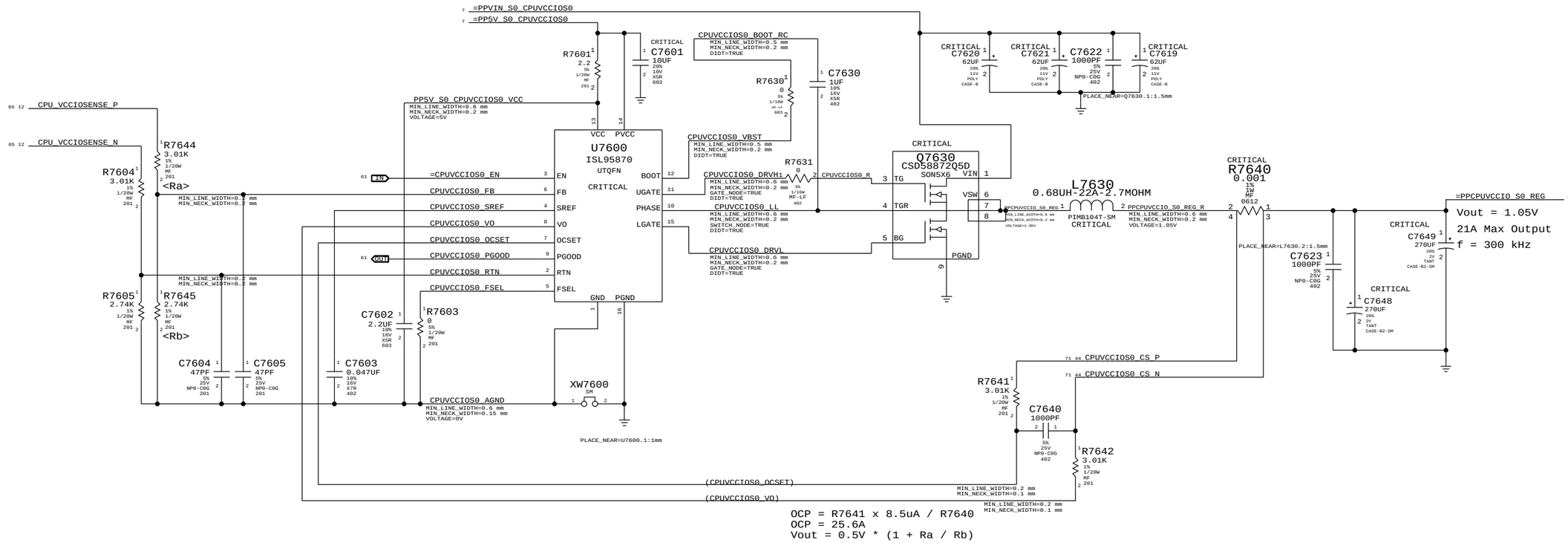
L7550
0.36UH-20%-30A-1.2MOHM
PIMB104T-SM
152S1323

PPVCORE_S0_AXG_R

R7550 0.00075 1% 1W MF 0612
=PPVCORE_S0_AXG_REG
CPUIMVP_ISNS1G_P
CPUIMVP_ISNS1G_N
R7553 46.4 1% 1/20W MF 201
R7554 10 1% 1/20W MF 201
CPUIMVP_ISUMG_N
C7574 1000PF 10% 16V X7R 201 NO STUFF
CPUIMVP_ISUMG_P

SYNC_MASTER=K21_MLB	SYNC_DATE=12/13/2010
PAGE TITLE	CPU IMVP7 & AXG VCore Output
Apple Inc.	DRAWING NUMBER 051-9276 SIZE D
	REVISION 2.7.0
	BRANCH
	PAGE 75 OF 109
	SHEET 57 OF 72

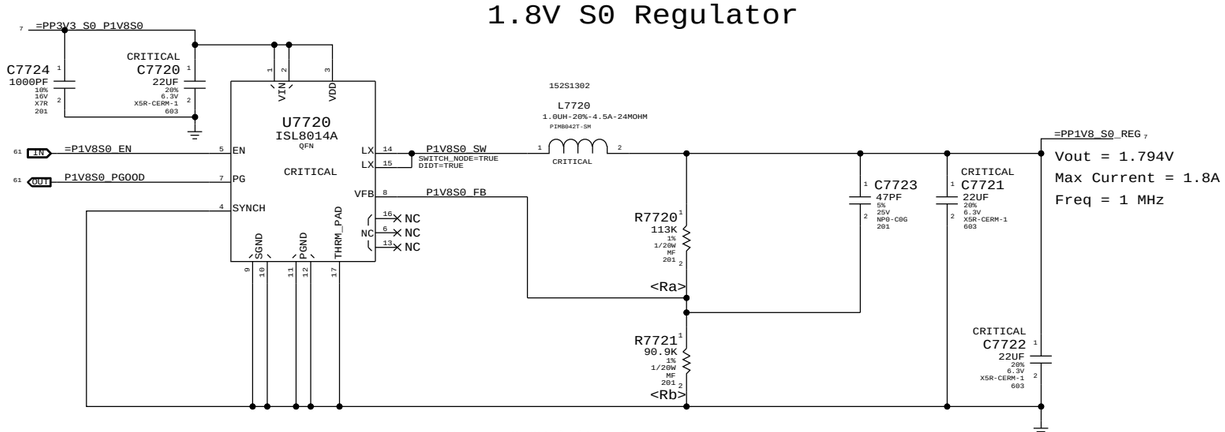
CPU VCCIO (1.05V S0) Regulator



OCP = R7641 x 8.5uA / R7640
OCP = 25.6A
Vout = 0.5V * (1 + Ra / Rb)

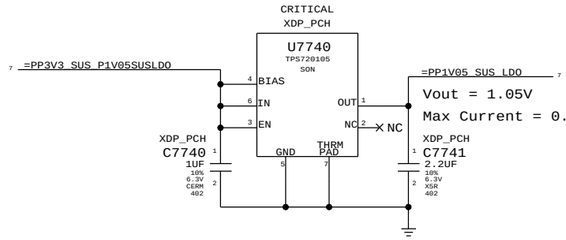
SYNC_MASTER=J13_MLB	SYNC_DATE=09/01/2011
PAGE TITLE	CPU VCCIO (1.05V) Power Supply
Apple Inc.	DRAWING NUMBER 051-9276 · SIZE D
	REVISION 2.7.0
	BRANCH
	PAGE 76 OF 109
	SHEET 58 OF 72

1.8V S0 Regulator

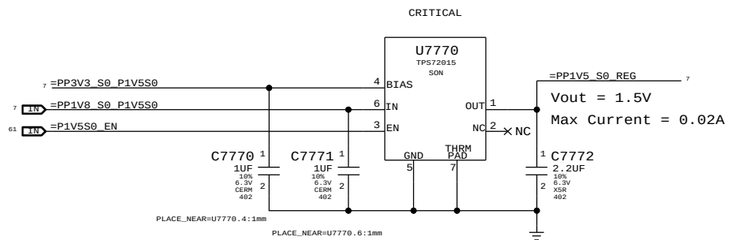


1.05V SUS LDO

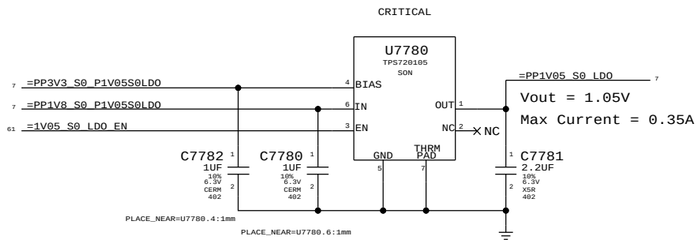
Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



1.5V S0 LDO



1.05V S0 LDO



SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: 051-9276 SIZE: D

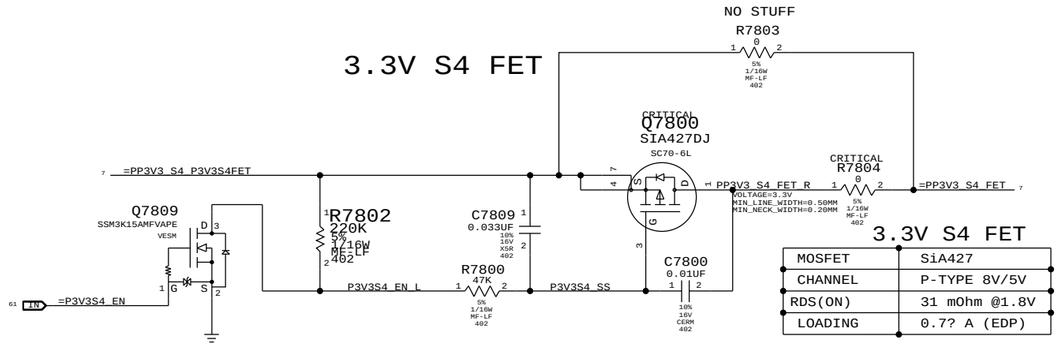
REVISION: 2.7.0

BRANCH:

PAGE: 77 OF 109

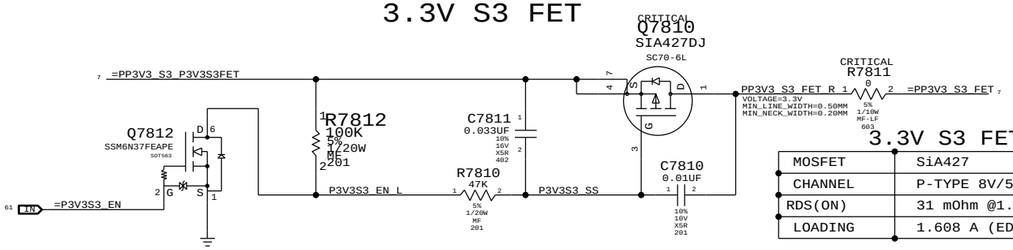
SHEET: 59 OF 72

3.3V S4 FET



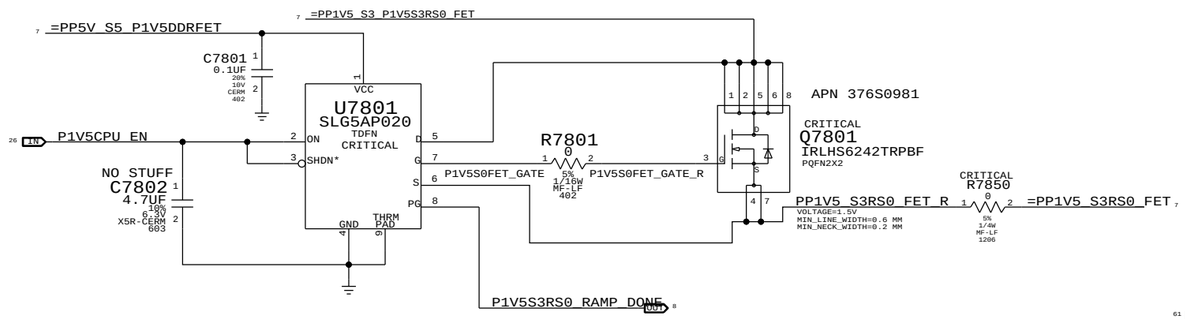
3.3V S4 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	31 mOhm @1.8V
LOADING	0.7? A (EDP)

3.3V S3 FET



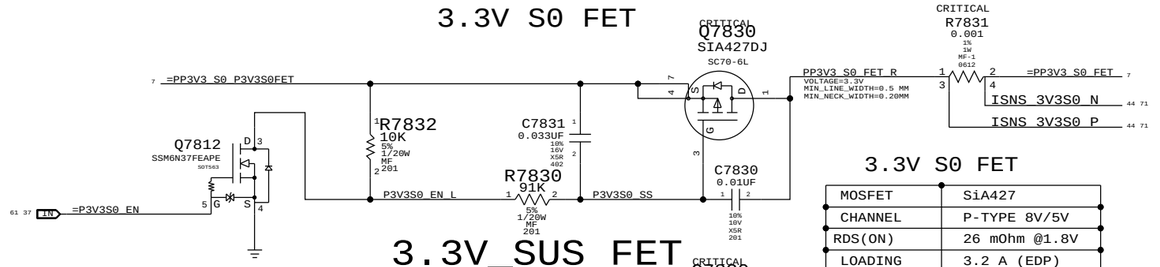
3.3V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	31 mOhm @1.8V
LOADING	1.608 A (EDP)

1.5V S3/S0 FET



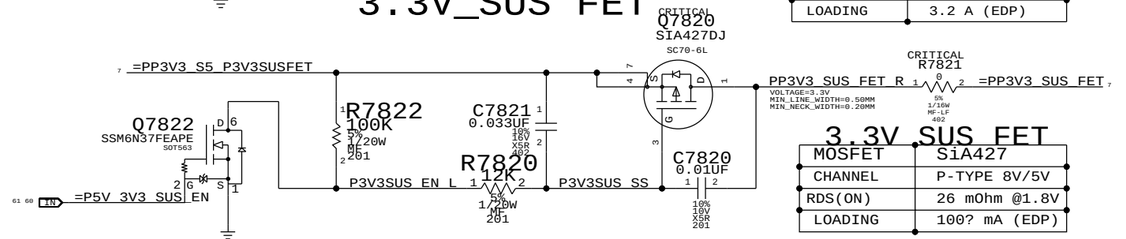
1.5V S3/S0 FET	
MOSFET	PQFN2X2
CHANNEL	N-TYPE
RDS(ON)	9.4 mOhm @4.5V
LOADING	5 A (EDP)

3.3V S0 FET



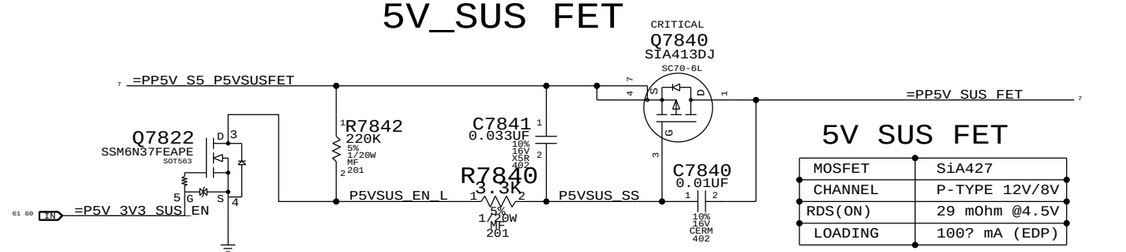
3.3V S0 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3.2 A (EDP)

3.3V_SUS FET



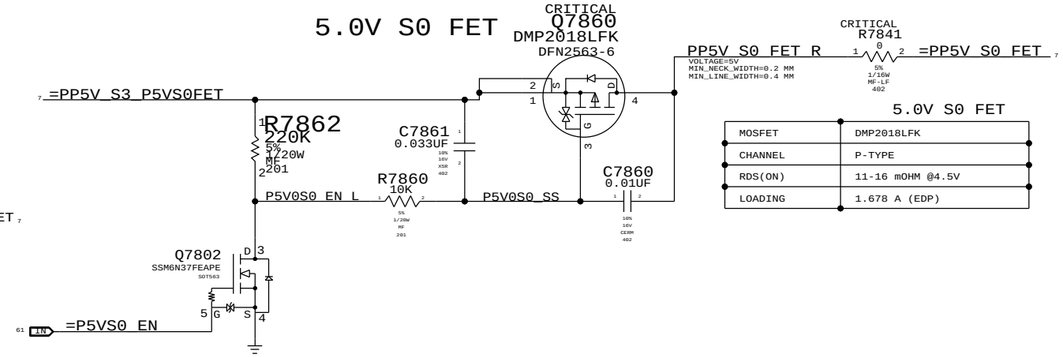
3.3V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

5V_SUS FET



5V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 12V/8V
RDS(ON)	29 mOhm @4.5V
LOADING	100? mA (EDP)

5.0V S0 FET



5.0V S0 FET	
MOSFET	DMP2018LFK
CHANNEL	P-TYPE
RDS(ON)	11-16 mOHM @4.5V
LOADING	1.678 A (EDP)

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE: Power FETs

Apple Inc.

DRAWING NUMBER: 051-9276 SIZE: D

REVISION: 2.7.0

BRANCH:

PAGE: 78 OF 109

SHEET: 60 OF 72

S5 Rail Enables & PGOOD

Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SUS_EN	PM_SLP_SS_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (S4AC)	1	1	1	0	0	0	0
Deep Sleep (S4)	0	1	1	0	0	0	0
Deep Sleep (S5AC)	1	1	0	0	0	0	0
Deep Sleep (S5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

=PP3V42_G3H_PWRCTL — Internal pull-ups 100K +/- 20%

C7940 0.1UF 10% 6.3V X5R 201 — U7941 SLG4AP012 TDFN — CRITICAL 343S0497

SMC_PM_G2_EN (MAKE_BASE=TRUE) → IN A (IPU)

=PP3V3_S5_PWRCTL → IN B

Threshold: ??
DLY > 10 ms
S5PGOOD_DLY

OUT A (OD,IPU) → NC

OUT B (OD,IPU) → P5V3V3_REG_EN (MAKE_BASE=TRUE) → =P5V3V3_REG_EN OUT 54

C7941 220PF 10% 25V X7R-CERM 201

GND — THRM PAD

R7941 100 5% 1/20W MF 201 — C7942 0.033UF 10% 16V X5R 402 NO STUFF

P3V3S5_EN (MAKE_BASE=TRUE) → =P3V3S5_EN OUT

S5_PWRGD (MAKE_BASE=TRUE) OUT 40

S5_PWRGD (old name RSMRST_PWRGD)-->SMC
SMC-->PM_DSW_PWRGD

CPUVCORE ENABLE

ALL_SYS_PWRGD → R7974 0 5% 1/20W MF 201 (PLACE_NEAR=U7400.1:5mm) → CPUIMVP_VR_ON OUT 56

3.3V,5V S3 ENABLE

PM_SLP_S4_L (MAKE_BASE=TRUE) IN

R7913 0 5% 1/20W MF 201 — P5VS3_EN (MAKE_BASE=TRUE) → =P5VS3_EN OUT 54

R7911 5.1K 5% 1/20W MF 201 (PLACE_NEAR=U7300.16:6mm)

R7912 9.1K 5% 1/20W MF 201 (PLACE_NEAR=Q7812.2:6mm)

NO STUFF C7913 0.068UF 10% 16V CERM 402

P3V3S3_EN (MAKE_BASE=TRUE) → =P3V3S3_EN OUT 60

DDRREG_EN (MAKE_BASE=TRUE) → =DDRREG_EN OUT 55

=USB_PWR_EN OUT 6 38 39

C7910 0.47UF 10% 6.3V CERM-X5R 402 (PLACE_NEAR=U7300.16:6mm)

C7912 0.47UF 10% 6.3V CERM-X5R 402 (PLACE_NEAR=Q7812.2:6mm)

U7970 DP S4 Power Enable

=PP3V3_S5_PWRCTL (PLACE_NEAR=U7940.1:2.3mm) → C7970 0.1uF 20% 10V CERM 402

PM_SLP_SS_L:100K pull down on PCH page → 40 17 IN → PM_SLP_SS_L

U7970 74LVC1G32 SOT891 — NC

P5V3V3_S4_EN (MAKE_BASE=TRUE) → =TBTAPWRSW_EN OUT 63 ; =P3V3S4_EN OUT 60

SMC_S4_WAKESRC_EN (MAKE_BASE=TRUE) → 41 40 IN

NOSTUFF R7915 0 5% 1/16W MF-LF 402

S0 ENABLE

PM_SLP_S3_L → R7978 100 5% 1/20W MF 201 → PM_SLP_S3_R_L (MAKE_BASE=TRUE)

=PP3V42_G3H_PWRCTL

R7931 10K 5% 1/20W MF 201 → CHGR_VFRQ OUT 52

Q7931 SSM3K15FV SOD-VESM-HF

(PM_SLP_S3_R_L)

R7987 33K 5% 1/20W MF 201 (PLACE_NEAR=U7100.15:6mm)

R7981 20K 5% 1/20W MF 201 (PLACE_NEAR=U7600.3:6mm)

R7988 39K 5% 1/20W MF 201 (PLACE_NEAR=U7770.3:6mm)

R7986 5.1K 5% 1/20W MF 201 (PLACE_NEAR=U7720.5:6mm)

=P5VS0_EN OUT 60
=P3V3S0_EN OUT 37 60
=PBUSVSENS_EN OUT 44
=TBT_S0_EN OUT 63

P1V8S0_EN (MAKE_BASE=TRUE) → =P1V8S0_EN OUT 59

P1V5S0_EN (MAKE_BASE=TRUE) → =P1V5S0_EN OUT 59

=1V05_S0_LDO_EN OUT 59

CPUVCCIOS0_EN (MAKE_BASE=TRUE) → =CPUVCCIOS0_EN OUT 58

PVCCSA_EN (MAKE_BASE=TRUE) → =PVCCSA_EN OUT 53

C7987 0.47UF 10% 6.3V CERM-X5R 402 (PLACE_NEAR=U7100.15:6mm)
C7981 0.47UF 10% 6.3V CERM-X5R 402 (PLACE_NEAR=U7600.3:6mm)
C7988 0.47UF 10% 6.3V CERM-X5R 402 (PLACE_NEAR=U7770.3:6mm)
C7986 0.47UF 10% 6.3V CERM-X5R 402 (PLACE_NEAR=U7720.5:6mm)

VFRQ Low: Fix Frequency
VFRQ High: Variable Frequency

CHGR VFRQ Generation

3.3V/5.0V Sus ENABLE

=PP3V3_S5_PWRCTL (PLACE_NEAR=U7940.5:2.3mm) → C7943 0.1UF 10% 6.3V X5R 201

SMC_BATLOW_L:100K pull up on SMC page → SMC_BATLOW_L IN

U7940 74AUP1G3208 SOT891 — VCC

PM_SLP_SUS_L IN → PM_SUS_EN (MAKE_BASE=TRUE) → =P5V_3V3_SUS_EN OUT 60

NO STUFF R7917 0 5% 1/20W MF 201

S0 Rail PGOOD (BJT Version)

=PP3V3_S5_VMON → R7956 150K 1% 1/20W MF 201 — S0PGD_C

R7951 15K 1% 1/20W MF 201 — R7952 7.15K 1% 1/20W MF 201

R7953 1K 5% 1/20W MF 201 (VMON_3V3_DIV → VMON_Q2_BASE)

R7954 1K 5% 1/20W MF 201 (=PP1V5_S3RS0_VMON → VMON_Q3_BASE)

R7955 1K 5% 1/20W MF 201 (=PP1V05_S0_VMON → VMON_Q4_BASE)

PP1V5_S3RS0

Q7950 ASMCC0179 DFN2015H4-8 (Q1 Q2 Q3 Q4) — NC — CRITICAL — NC

353S2809 S0PGD_BJT_GND_R

Worst-Case Thresholds:
Q2: 0.XXXV
Q3: 0.640V
3.3V w/Divider: 2.345V
Q4: 0.660V

3.3V SUS Detect

NO STUFF R7930 0 5% 1/20W MF 201

Could stuff R7930 to satisfy PCH power down timing tz35

No stuff C7931, 12ms Min delay time

U7930 Sense input threhold is 3.07V

=PP3V3_S5_PWRCTL (PLACE_NEAR=U7930.6:2.3mm) → C7930 0.1UF 10% 6.3V X5R 201

=PP3V3_SUS_PWRCTL → R7933 100K 5% 1/20W MF 201

U7930 TPS3808G33DBVRG4 SOT23-6 (90K IP9) — CRITICAL — SENSE — CT — S4_PGOOD_CT — RESET* — MR* — GND

PM_RSMRST_L → OUT 17

PM_RSMRST_L goes to U1800.C21

C7931 1000PF 10% 16V X7R 201 NO STUFF

SUS_PGOOD_MR_L

S0 Rail PGOOD Circuitry (ISL Version in development)

Thresholds:
VDD: 2.734V-3.010V
V2MON: 2.815V-3.099V
V3MON: 0.572V-0.630V
V4MON: 0.572V-0.630V

P1V5S0_PGOOD from U7710

=PP5V_S0_VMON — =PP1V5_S3RS0_VMON — =PP1V05_S0_VMON — =PP3V3_S0_VMON

R7960 6.04K 1% 1/20W MF 201 — R7970 10K 1% 1/20W MF 201 — R7972 6.04K 1% 1/20W MF 201 (S0PGOOD_ISL → P5V_DIV_VMON)

R7961 15K 1% 1/20W MF 201 — R7971 12.4K 1% 1/20W MF 201 — R7973 15K 1% 1/20W MF 201 (P1V5_DIV_VMON)

C7960 0.1UF 10% 6.3V X5R 201

U7960 ISL88042IRTEZ TDFN (IPU) — VDD — V2MON — V3MON — V4MON — CRITICAL — MR* — RST* — GND — THRM_PAD

P1V05_DIV_VMON

S0PGOOD_ISL → ALL_SYS_PWRGD_R

353S2310

R7967 10K 5% 1/20W MF 201 — NO STUFF R7968 100 5% 1/20W MF 201

CPUIMVP_AXG_PGOOD → R7966 100 5% 1/20W MF 201

P1V8S0_PGOOD → R7965 100 5% 1/20W MF 201

P3V3S5_PGOOD → R7901 100 5% 1/20W MF 201

CPUVCCIOS0_PGOOD → R7964 100 5% 1/20W MF 201

PVCCSA_PGOOD → R7963 100 5% 1/20W MF 201

R7962 330 5% 1/20W MF 201 (ALL_SYS_PWRGD) → OUT 23 25 40 51 61

WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

PM_WLAN_EN_L OUT 36

Q7925 2N7002DW-X-G SOT-363 — AP_PWR_EN IN 36 23 18 — (AC_EN_L)

Q7920 2N7002DW-X-G SOT-363 — AC_EN_L

SMC_ADAPTER_EN IN 41 40 17

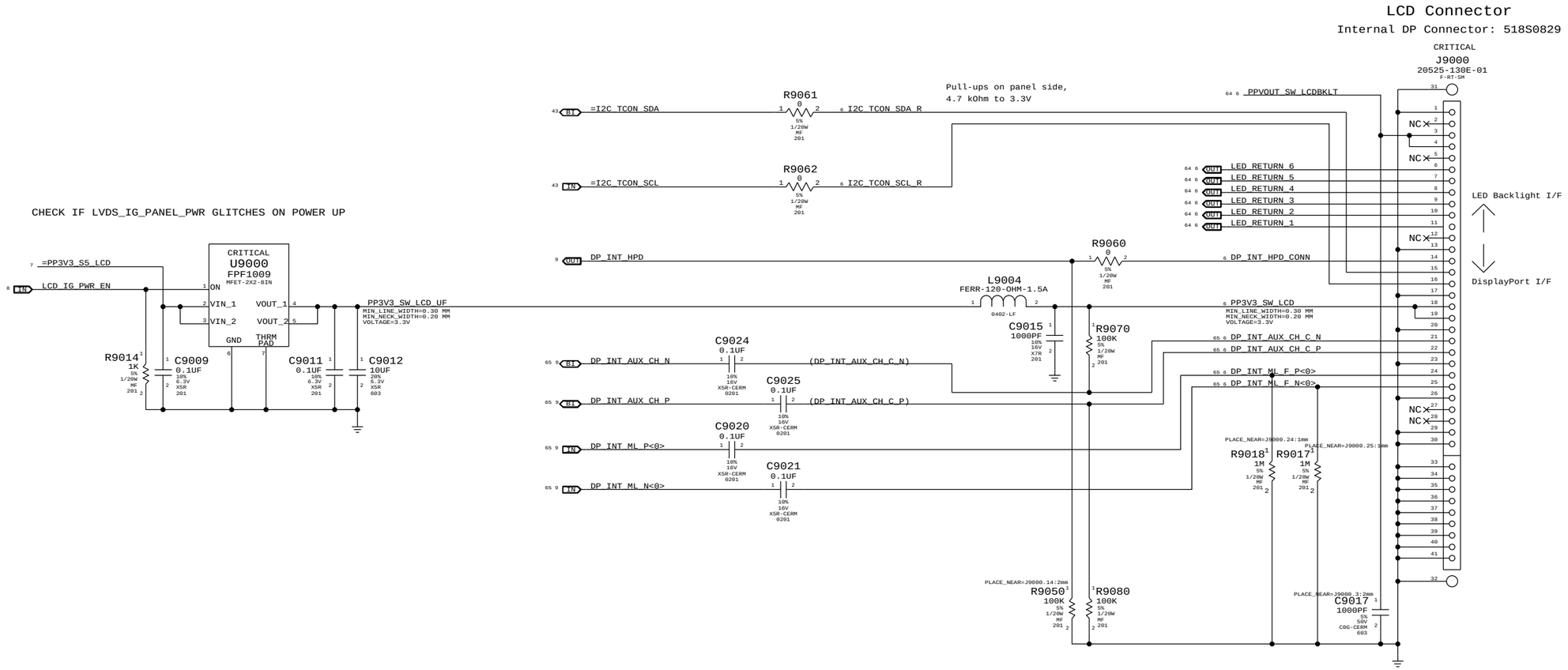
NO STUFF R7929 0 5% 1/20W MF 201

Q7920 2N7002DW-X-G SOT-363 — (PM_SLP_S3_L)

PM_SLP_S3_L IN 61 40 26 17

Q7925 2N7002DW-X-G SOT-363 — NC — Unused fet

SYNC_MASTER=J13_MLB	SYNC_DATE=11/18/2011
PAGE TITLE	Power Control 1/ENABLE
Apple Inc.	DRAWING NUMBER 051-9276 · SIZE D · REVISION 2.7.0 · BRANCH · PAGE 79 OF 109 · SHEET 61 OF 72



SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE
Internal DisplayPort Connector

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D
REVISION 2.7.0
BRANCH
PAGE 90 OF 109
SHEET 62 OF 72

3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

=PP3V3_S4_TBTAPWRSW

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)

C9487 100UF 20% 6.3V POLY-TANT CASE-B2-SM (CRITICAL)
C9480 22UF 20% 6.3V X5R-CERM-1 603 (CRITICAL)
C9481 0.1UF 10% 16V X5R-CERM 0201

=PPHV_SW_TBTAPWRSW
18.9V Max

C9415 4.7UF 10% 25V X5R-CERM 0603
C9410 0.1UF 10% 25V X5R 402

U9410 CRITICAL
CD3210A0RGP
QFN

V3P3 (19, 20)
VHV (6, 7)
V3P3OUT (18)
OUT (12, 14)
RSVD (16)
RSVD (15)
EN (5)
HV_EN (11)
S0 (17)
ISET_V3P3 (8)
ISET_S0 (10)
ISET_S3 (9)
GND (1, 2, 3, 4, 13)
THRM PAD (21)

C9485 0.1UF 10% 16V X5R-CERM 0201
C9486 10UF 20% 6.3V CERM-X5R 0402
C9411 0.1UF 10% 25V X5R 402

PP3V3_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

PPHV_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V

=TBTAPWRSW_EN
TBT_A_HV_EN
=TBT_S0_EN

TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3

12V: See below

R9410 22.6K 1% 1/20W MF 201 (TBTHV:P15V)
R9411 22.6K 1% 1/20W MF 201 (TBTHV:P15V)
R9412 36.5K 1% 1/20W MF 201

TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R

R9413 22.6K 1% 1/20W MF 201 (TBTHV:P15V)
R9414 22.6K 1% 1/20W MF 201 (TBTHV:P15V)

Single-fault protection requires two R's per HV ISET_Sx with CD3210.
Single R on ISET_V3P3 OK.

ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MF,1/20W,17.8K,1,0201	R9410,R9413		TBTHV:P12V
118S0145	2	RES,MF,1/20W,17.8K,1,0201	R9411,R9414		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

Thunderbolt Connector A

PP3V3_SW_TBTAPWR

C9420 0.1UF 10% 16V X5R-CERM 0201
C9421 0.1UF 10% 16V X5R-CERM 0201
R9427 10K 5% 1/20W MF 201
R9429 100K 5% 1/20W MF 201

U9420 CRITICAL
CBTL05023
HVQFN
VDD

SIGNAL_MODEL=TBT_MUX

TBT_A_CIO_SEL	1	BIASIN	
DP_AUXIO_EN	2	AUXIO_EN	
DP_TBTPA_AUXCH_C_N	7	AUX-	
DP_TBTPA_AUXCH_C_P	8	AUX+	
DP_TBTSNK0_DDC_DATA	4	DDC_DAT	
DP_TBTSNK0_DDC_CLK	5	DDC_CLK	
TBT_A_CONFIG1_BUF	16	CA_DETOUT	
DP_TBTPA_ML_P<1>	11	DP+	
DP_TBTPA_ML_N<1>	10	DP-	
TBT_A_LSTX	14	LSTX	
TBT_A_LSRX_UNBUF	13	LSRX	
TBT_A_DP_PWRDN	6	DP_PD	
DP_TBTPA_HPD	12	HPDOUT	
	24	BIASOUT	
	23	AUXIO-	
	22	AUXIO+	
	18	CA_DETOUT	
	19	DPMLO+	
	20	DPMLO-	
	17	HPD	

TBT_A_BIAS (VOLTAGE=3.3V)
C9425 0.1UF 10% 16V X5R-CERM 0201

DP_A_AUXCH_DDC_N
DP_A_AUXCH_DDC_P
TBT: RX_1 Bias Sink

TBT_A_CONFIG1_RC
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)

R9426 1M 5% 1/20W MF 201
R9428 100K 5% 1/20W MF 201

GND_THMPAD

C9430 0.1UF 10% 16V X5R-CERM 0201
C9431 0.1UF 10% 16V X5R-CERM 0201
C9432 0.22UF 20% 6.3V X5R 0201
C9433 0.22UF 20% 6.3V X5R 0201

DP_TBTPA_AUXCH_C_N
DP_TBTPA_AUXCH_C_P
DP_TBTPA_ML_C_P<1>
DP_TBTPA_ML_C_N<1>

PP3V3_SW_TBTAPWR

U9460 CRITICAL
74AUP1T97
SOT891
VCC
GND
TBT_A_LSRX
Y = B
C9460 0.1UF 20% 10V CERM 402

L9400 FERR-120-OHM-3A 0603
C9400 0.01UF 10% 50V X7R 402
R9401 12 5% 1/20W MF 201
PP3V3RHV_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V

TBTACONN_20_RC
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V

C9401 0.01UF 10% 50V X7R 402

For J9400 TBT SMT pads (3, 5, 17 & 19):
GND_VOID=TRUE

J9400 CRITICAL
MDP-J11
F-RT-TH

HOT_PLUG_DETECT	2	GND	1
CONFIG1	4	ML_LANE0P	3
CONFIG2	6	ML_LANE0N	5
GND	13	GND	7
ML_LANE3P	10	ML_LANE1P	9
ML_LANE3N	12	ML_LANE1N	11
GND	14	GND	8
AUX_CHP	16	ML_LANE2P	15
AUX_CHN	18	ML_LANE2N	17
DP_PWR	20	RETURN	19
SHIELD PINS	28	27	26	25	24	23	22	21

514-0818

C9405 0.01UF 10% 25V X5R-CERM 0201
TBTACONN_1_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V

(0-18.9V)
DP Dir
TBT Dir

TBT: TX_0

C9406 0.01UF 10% 25V X5R-CERM 0201
TBTACONN_7_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V

(0-18.9V)
TBT: LSX_R2P/P2R (P/N)

TBT: TX_1

GND_VOID=TRUE (Both C's)
C9470 0.22UF
C9471 0.22UF
C9472 0.22UF
C9473 0.22UF
20% 6.3V X5R 0201

TBT_A_R2D_C_P<0>
TBT_A_R2D_C_N<0>
TBT_A_R2D_C_P<1>
TBT_A_R2D_C_N<1>

R9470 470K 5% 1/20W MF 201
R9471 470K 5% 1/20W MF 201
R9472 470K 5% 1/20W MF 201
R9473 470K 5% 1/20W MF 201

470k R's for ESD protection on AC-coupled signals.

GND_VOID=TRUE (Both C's)
C9474 0.47UF
C9475 0.47UF
C9476 0.47UF
C9477 0.47UF
20% 6.3V CERM-X5R-1 201

TBT_A_D2R_P<0>
TBT_A_D2R_N<0>
TBT_A_D2R_C_P<0>
TBT_A_D2R_C_N<0>
TBT_A_D2R_P<1>
TBT_A_D2R_N<1>
TBT_A_D2R_C_P<1>
TBT_A_D2R_C_N<1>

R9494 1K 5% 1/20W MF 201 (SIGNAL_MODEL=EMPTY)
R9495 1K 5% 1/20W MF 201 (SIGNAL_MODEL=EMPTY)

TBT Dir
DP Dir

C9478 0.22UF
C9479 0.22UF
20% 6.3V X5R 0201

DP_TBTPA_ML_C_P<3>
DP_TBTPA_ML_C_N<3>
DP_TBTPA_ML_P<3>
DP_TBTPA_ML_N<3>
TBT: Unused

R9478 470K 5% 1/20W MF 201
R9479 470K 5% 1/20W MF 201

TBT_A_BIAS

R9498 2.2K 5% 1/20W MF 201
R9499 2.2K 5% 1/20W MF 201

CRITICAL
SIGNAL_MODEL=TBTPIN
GND_VOID=TRUE
D9498 BAR90-02LRH TSLP-2-7 (Both D's)
D9499 BAR90-02LRH TSLP-2-7

TBT_A_D2R1_AUXDDC_P
TBT_A_D2R1_AUXDDC_N

CRITICAL
L9498 650NH-5%-0.430MA-0.52OHM 0603
L9499 650NH-5%-0.430MA-0.52OHM 0603
GND_VOID=TRUE
SIGNAL_MODEL=EMPTY

DP_A_AUXCH_DDC_P
DP_A_AUXCH_DDC_N

C9498 30PF 5% 50V CERM 402
C9499 30PF 5% 50V CERM 402

TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC

R9452 1M 5% 1/20W MF 201
R9451 1M 5% 1/20W MF 201
C9494 330PF 10% 16V X7R 201
C9495 330PF 10% 16V X7R 201
R9441 100K 5% 1/20W MF 201

C9402 0.01UF 10% 25V X5R-CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

SYNC_MASTER=J13_MLB SYNC_DATE=11/18/2011

PAGE TITLE: Thunderbolt Connector A

Apple Inc.

DRAWING NUMBER: 051-9276 SIZE: D
REVISION: 2.7.0
BRANCH:
PAGE: 94 OF 109
SHEET: 63 OF 72

PPBUS S0 LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.65 A (EDP)

THERE IS A SENSE RESISTOR BETWEEN PPBUS_SW_LCDBKLT_PWR AND PPBUS_SW_BKL ON THE SENSOR PAGE

*C9797 AND C9799 SHOULD BE PLACED IN T-BONE FOR ACOUSTICS
*PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
*LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

F9700 3AMP-32V-467 603-HF BOTTOM
=PPBUS_S0_LCDBKLT → PPBUS_S0_LCDBKLT_FUSED (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=12.6V)
R9788 301K 1% 1/20W MF 201
C9782 0.1UF 10% 16V X5R 402
CRITICAL Q9706 FDC638APZ_SBMS001 SSOT6-HF
PPBUS_SW_LCDBKLT_PWR (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=12.6V) → 8 64
LCDBKLT_EN_DIV
R9789 147K 1% 1/20W MF 201
LCDBKLT_EN_L
Q9707 SSM6N15FEAPE SOT563
8 IN LCD_BKLT_EN
LCDBKLT_DISABLE
Q9707 SSM6N15FEAPE SOT563
25 IN BKLT_PLT_RST_L

=PP5V_S0_BKL
=PPBUS_SW_BKL
CRITICAL L9701 15UH-2.8A PIMB053T-SM
PPBUS_SW_LCDBKLT_PWR_SW (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.150 MM, VOLTAGE=50V, SWITCH_NODE=TRUE, DIDT=TRUE)
PLACE_NEAR=L9701.2:3mm
CRITICAL D9701 SOD-123 RB160M-60G
PLACE_NEAR=U9701.A5:3mm
C9796 220PF 10% 50V X7R-CERM 402
CRITICAL C9797 10UF 10% 50V X5R 1210-1
CRITICAL C9799 10UF 10% 50V X5R 1210-1
PLACE_NEAR=D9701.2:5mm
PLACE_NEAR=D9701.2:3mm
PPVOUT_SW_LCDBKLT (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.375 MM, VOLTAGE=50V) → 6 62
CRITICAL C9712 10UF 10% 25V X5R 805
C9713 0.1UF 10% 25V X5R 402
PLACE_NEAR=L9701.1:3mm
PLACE_NEAR=L9701.1:3mm
PLACE_NEAR=U9701.D1:5mm
C9710 1UF 10% 25V X5R 603-1
PLACE_NEAR=U9701.D1:3mm
C9714 0.01UF 10% 10V X5R 201
XW9720 SM
PPVOUT_SW_LCDBKLT_FB (VOLTAGE=50V, MIN_LINE_WIDTH=0.1 MM, MIN_NECK_WIDTH=0.1 MM)
PLACE_NEAR=C9797.1:5mm
=PP3V3_S0_BKL_VDDIO
PLACE_NEAR=U9701.C4:4mm
C9711 0.1UF 10% 6.3V X5R 201

U9701 25-BUMP-MICRO LP8550 CRITICAL
VDDIO VLDO VIN (C4, D1, C1)
VSYNC (D2) ← BKL_VSYNC_R
FILTER (C2) ← BKL_FLTR
ISET (B3) ← BKL_ISET
FSET (B4) ← BKL_FSET
SCLK (D3) ← BKL_SCL
SDA (D4) ← BKL_SDA
PWM (A4) ← BKL_PWM
EN (A3) ← BKL_EN
FAULT (C3) → TP_BKL_FAULT
SW_0 (B1), SW_1 (B2)
FB (A5)
OUT1 (E5) BKL_ISEN1
OUT2 (D5) BKL_ISEN2
OUT3 (C5) BKL_ISEN3
OUT4 (E3) BKL_ISEN4
OUT5 (E2) BKL_ISEN5
OUT6 (E1) BKL_ISEN6
GND_S (B5), GND_L (E4), GND_SW (A1), GND_SW (A2)

R9741 10K 5% 1/20W MF 201
R9753 0 5% 1/20W MF 201
43 IN =I2C_BKL_1_SCL
R9757 0 5% 1/20W MF 201
43 BI =I2C_BKL_1_SDA
Addr: 0x58(Wr)/0x59(Rd)
64 8 PPBUS_SW_LCDBKLT_PWR
R9731 200K 1% 1/20W MF 201
R9715 100K 1% 1/20W MF 201
PLACE_SIDE=BOTTOM
8 IN LCD_BKLT_PWM
R9704 33 5% 1/20W MF 201
C9704 33PF 5% 25V NP0-C0G 201
Fpwm=9.62kHz
see spec for others
R9755 10K 1% 1/20W MF 201
R9716 90.9K 1% 1/20W MF 201
I_LED=20.3mA
R9714 18.2K 1% 1/20W MF 201
GND_BKL_SGND (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=0V)
XW9710 SM
PLACEMENT_NOTE=Keep away from noise nodes(E4, A1, A2, B1, B2 pins)
I_LED=369/Riset
(EEPROM should set EN_I_RES=1)

BKLT:PROD
R9717 0 5% 1/16W MF-LF 402 BOTTOM
PLACE_NEAR=U9701.E5:10mm
LED_RETURN_1 (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.20 mm) OUT → 6 62
BKLT:PROD
R9718 0 5% 1/16W MF-LF 402 BOTTOM
PLACE_NEAR=U9701.D5:10mm
LED_RETURN_2 (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.20 mm) OUT → 6 62
BKLT:PROD
R9719 0 5% 1/16W MF-LF 402 BOTTOM
PLACE_NEAR=U9701.C5:10mm
LED_RETURN_3 (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.20 mm) OUT → 6 62
BKLT:PROD
R9720 0 5% 1/16W MF-LF 402 BOTTOM
PLACE_NEAR=U9701.E3:10mm
LED_RETURN_4 (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.20 mm) OUT → 6 62
BKLT:PROD
R9721 0 5% 1/16W MF-LF 402 BOTTOM
PLACE_NEAR=U9701.E2:10mm
LED_RETURN_5 (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.20 mm) OUT → 6 62
BKLT:PROD
R9722 0 5% 1/16W MF-LF 402 BOTTOM
PLACE_NEAR=U9701.E1:10mm
LED_RETURN_6 (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.20 mm) OUT → 6 62

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC_MASTER=J13_MLB SYNC_DATE=10/13/2011
PAGE TITLE: LCD Backlight Driver
Apple Inc.
DRAWING NUMBER 051-9276 SIZE D
REVISION 2.7.0
BRANCH
PAGE 97 OF 109
SHEET 64 OF 72

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.100 MM	0.100 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_AGTL	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_8MIL	*	*	CPU_8MIL_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_8MIL_2ANY	*	8 MIL	?

Note: CPU_8MIL and CPU_ITP can be converted back to TABLE_SPACING_RULE once rdar://10308147 is resolved

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_ITP	*	*	CPU_ITP_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ITP_2ANY	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	CPU_COMP	*	CPU_COMP_2SELF
CPU_COMP	*	*	CPU_COMP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_COMP_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	*	=4x_DIELECTRIC	?
CPU_COMP_2OTHER	*	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	CPU_VCCSENSE	*	CPU_VCCSENSE_2SELF
CPU_VCCSENSE	*	*	CPU_VCCSENSE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	*	=4x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	*	=6x_DIELECTRIC	?

PCI-Express Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
CLK_PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

PCIE Clock Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	CLK_PCIE	*	CLK_PCIE_2SELF
CLK_PCIE	*	*	CLK_PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CLK_PCIE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	*	=4x_DIELECTRIC	?
CLK_PCIE_2OTHER	*	=6x_DIELECTRIC	?

CPU PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_CPU_TX	PCIE_CPU_TX	*	PCIE_TX2TX
PCIE_CPU_RX	PCIE_CPU_RX	*	PCIE_RX2RX
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2OTHERTX
PCIE_CPU_RX	*_CPU_RX	*	PCIE_RX2OTHERRX
PCIE_CPU_TX	*_CPU_RX	*	PCIE_TX2RX
PCIE_CPU_RX	*_CPU_TX	*	PCIE_RX2TX
PCIE_CPU_TX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*	*	PCIE_2OTHER
PCIE_CPU_RX	*	*	PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	*	=2.5x_DIELECTRIC	?
PCIE_RX2RX	*	=2.5x_DIELECTRIC	?
PCIE_TX2OTHERTX	*	=4x_DIELECTRIC	?
PCIE_RX2OTHERRX	*	=4x_DIELECTRIC	?
PCIE_TX2RX	*	=6x_DIELECTRIC	?
PCIE_RX2TX	*	=6x_DIELECTRIC	?
PCIE_2OTHERHS	*	=4x_DIELECTRIC	?
PCIE_2OTHER	*	=3x_DIELECTRIC	?

PCH PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_PCH_TX	PCIE_PCH_TX	*	PCIE_TX2TX
PCIE_PCH_RX	PCIE_PCH_RX	*	PCIE_RX2RX
PCIE_PCH_TX	*_PCH_TX	*	PCIE_TX2OTHERTX
PCIE_PCH_RX	*_PCH_RX	*	PCIE_RX2OTHERRX
PCIE_PCH_TX	*_PCH_RX	*	PCIE_TX2RX
PCIE_PCH_RX	*_PCH_TX	*	PCIE_RX2TX
PCIE_PCH_TX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*	*	PCIE_2OTHER
PCIE_PCH_RX	*	*	PCIE_2OTHER

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

Note: DisplayPort tables are on Page 103

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_80D	PCIE_PCH_TX	DMI_S2N_P<3:0>	9 17
DMI_S2N	PCIE_80D	PCIE_PCH_TX	DMI_S2N_N<3:0>	9 17
DMI_N2S	PCIE_80D	PCIE_PCH_RX	DMI_N2S_P<3:0>	9 17
DMI_N2S	PCIE_80D	PCIE_PCH_RX	DMI_N2S_N<3:0>	9 17
FDI_DATA	PCIE_80D	PCIE_PCH_RX	FDI_DATA_P<7:0>	9 17
FDI_DATA	PCIE_80D	PCIE_PCH_RX	FDI_DATA_N<7:0>	9 17
	CPU_45S	CPU_AGTL	FDI_FSYNC<1..0>	9 17
	CPU_45S	CPU_AGTL	FDI_LSYNC<1..0>	9 17
	CPU_45S	CPU_AGTL	FDI_INT	9 17
CPU_PECI	CPU_45S	CPU_COMP	CPU_PECI	10 19 41
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	10 17
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	10 17 26
	CPU_45S	CPU_TTP	XDP_DBRESET_L	10 23 25
	CPU_45S	CPU_TTP	XDP_CPU_PRDY_L	10 23
	CPU_45S	CPU_TTP	XDP_CPU_PREQ_L	10 23
	CPU_27P4S	CPU_COMP	EDP_COMP	9
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>	10
	CPU_45S	CPU_TTP	CPU_CFG<11..0>	9 23
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L	10 40
	CPU_45S	CPU_AGTL	CPU_VCCIO_SEL	12
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	10 40 41 56
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD	10 19 23
PM_THRMTRIP_L	CPU_45S	CPU_8MIL	PM_THRMTRIP_L	10 19 41
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_P	10 16
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_N	10 16
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKP	8 10
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKN	8 10
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_P	10 16
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_N	10 16
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_P	16 23
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_N	16 23
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_P	23
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_N	23
XDP_TDI	CPU_45S	CPU_TTP	XDP_CPU_TDI	10 23
XDP_TDO	CPU_45S	CPU_TTP	XDP_CPU_TDO	10 23
XDP_TMS	CPU_45S	CPU_TTP	XDP_CPU_TMS	10 23
XDP_TCK	CPU_45S	CPU_TTP	XDP_CPU_TCK	10 23
XDP_TRST_L	CPU_45S	CPU_TTP	XDP_CPU_TRST_L	10 23
XDP_BPM_L	CPU_45S	CPU_TTP	XDP_BPM_L<3..0>	10 23
XDP_BPM_L_R_CFG	CPU_45S	CPU_TTP	XDP_BPM_L<7..4>	10 23
(XDP_BPM_L_R_CFG)	CPU_45S	CPU_TTP	XDP_OBSDATA_B<3..0>	23
(XDP_BPM_L_R_CFG)	CPU_45S	CPU_TTP	CPU_CFG<15..12>	9 23
(FSB_CPURST_L)	CPU_45S	CPU_TTP	XDP_CPURST_L	23
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_P	12 56
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_N	12 56
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_P	12 58
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_N	12 58
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_P	12 56
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_N	12 56
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_P	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_N	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	9
CPU_SVIDALERT_L	CPU_45S	CPU_COMP	CPU_VIDALERT_L	12 56
CPU_SVIDSCLK	CPU_45S	CPU_COMP	CPU_VIDSCLK	12 56
CPU_SVIDSOUT	CPU_45S	CPU_COMP	CPU_VIDSOUT	12 56
PCIE_CPU_MUX_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_P<0>	8 37
PCIE_CPU_MUX_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_N<0>	8 37
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_MUX_IN_P	37
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_MUX_IN_N	37
PCIE_CPU_MUX_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<0>	8 37
PCIE_CPU_MUX_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<0>	8 37
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_MUX_OUT_P	37
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_MUX_OUT_N	37
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_R2D_C_P<1>	8 37
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_R2D_C_N<1>	8 37
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_P<1>	6 37
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_N<1>	6 37
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<1>	6 8 37
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<1>	6 8 37
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_P<1>	
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_N<1>	
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_P	6 16 37
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_N	6 16 37
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_P<3..0>	9 62
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_N<3..0>	9 62
	DP_80D	DP_TX	DP_INT_ML_F_P<3..0>	6 62
	DP_80D	DP_TX	DP_INT_ML_F_N<3..0>	6 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_P	6 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_N	6 62
	DP_80D	DP_AUX	DP_INT_AUX_CH_P	9 62
	DP_80D	DP_AUX	DP_INT_AUX_CH_N	9 62

DMI/FDI

PCIe SSD

DP

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM_CMD2CTRL	*	=3x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=PWR_P2MM	?
MEM_2GND	*	=GND_P2MM	?
MEM_2OTHER	*	=6x_DIELECTRIC	?

PalPilot Spacing	"Real" Spacing
=2x_DIELECTRIC	=2x_DIELECTRIC
=5.7x_DIELECTRIC	=3x_DIELECTRIC
=4x_DIELECTRIC	=3x_DIELECTRIC
=4x_DIELECTRIC	=3x_DIELECTRIC
=4x_DIELECTRIC	=3x_DIELECTRIC
=8.6x_DIELECTRIC	=6x_DIELECTRIC
=5.7x_DIELECTRIC	=4x_DIELECTRIC
=PWR_P2MM	=PWR_P2MM
=GND_P2MM	=GND_P2MM
=8.6x_DIELECTRIC	=6x_DIELECTRIC

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	*	*	MEM_2OTHER
MEM_A_DQS_1	*	*	MEM_2OTHER
MEM_A_DQS_2	*	*	MEM_2OTHER
MEM_A_DQS_3	*	*	MEM_2OTHER
MEM_A_DQS_4	*	*	MEM_2OTHER
MEM_A_DQS_5	*	*	MEM_2OTHER
MEM_A_DQS_6	*	*	MEM_2OTHER
MEM_A_DQS_7	*	*	MEM_2OTHER
MEM_B_DQS_0	*	*	MEM_2OTHER
MEM_B_DQS_1	*	*	MEM_2OTHER
MEM_B_DQS_2	*	*	MEM_2OTHER
MEM_B_DQS_3	*	*	MEM_2OTHER
MEM_B_DQS_4	*	*	MEM_2OTHER
MEM_B_DQS_5	*	*	MEM_2OTHER
MEM_B_DQS_6	*	*	MEM_2OTHER
MEM_B_DQS_7	*	*	MEM_2OTHER
MEM_A_DATA_0	*	*	MEM_2OTHER
MEM_A_DATA_1	*	*	MEM_2OTHER
MEM_A_DATA_2	*	*	MEM_2OTHER
MEM_A_DATA_3	*	*	MEM_2OTHER
MEM_A_DATA_4	*	*	MEM_2OTHER
MEM_A_DATA_5	*	*	MEM_2OTHER
MEM_A_DATA_6	*	*	MEM_2OTHER
MEM_A_DATA_7	*	*	MEM_2OTHER
MEM_B_DATA_0	*	*	MEM_2OTHER
MEM_B_DATA_1	*	*	MEM_2OTHER
MEM_B_DATA_2	*	*	MEM_2OTHER
MEM_B_DATA_3	*	*	MEM_2OTHER
MEM_B_DATA_4	*	*	MEM_2OTHER
MEM_B_DATA_5	*	*	MEM_2OTHER
MEM_B_DATA_6	*	*	MEM_2OTHER
MEM_B_DATA_7	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0>	8 11 27 28 32
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0>	8 11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM_A_CKE<3..0>	11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM_A_CS_L<3..0>	11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM_A_ODT<3..0>	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM_A_A<15..0>	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM_A_BA<2..0>	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM_A_RAS_L	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM_A_CAS_L	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM_A_WE_L	11 27 28 32
MEM_A_DQ_BYTE0	MEM_45S	MEM_A_DATA_0	MEM_A_DQ<7..0>	11 27
MEM_A_DQ_BYTE1	MEM_45S	MEM_A_DATA_1	MEM_A_DQ<15..8>	11 27
MEM_A_DQ_BYTE2	MEM_45S	MEM_A_DATA_2	MEM_A_DQ<23..16>	11 27
MEM_A_DQ_BYTE3	MEM_45S	MEM_A_DATA_3	MEM_A_DQ<31..24>	11 27
MEM_A_DQ_BYTE4	MEM_45S	MEM_A_DATA_4	MEM_A_DQ<39..32>	11 28
MEM_A_DQ_BYTE5	MEM_45S	MEM_A_DATA_5	MEM_A_DQ<47..40>	11 28
MEM_A_DQ_BYTE6	MEM_45S	MEM_A_DATA_6	MEM_A_DQ<55..48>	11 28
MEM_A_DQ_BYTE7	MEM_45S	MEM_A_DATA_7	MEM_A_DQ<63..56>	11 28
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM_A_DQS_P<0>	11 27
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM_A_DQS_N<0>	11 27
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM_A_DQS_P<1>	11 27
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM_A_DQS_N<1>	11 27
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM_A_DQS_P<2>	11 27
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM_A_DQS_N<2>	11 27
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM_A_DQS_P<3>	11 27
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM_A_DQS_N<3>	11 27
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM_A_DQS_P<4>	11 28
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM_A_DQS_N<4>	11 28
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM_A_DQS_P<5>	11 28
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM_A_DQS_N<5>	11 28
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM_A_DQS_P<6>	11 28
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM_A_DQS_N<6>	11 28
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM_A_DQS_P<7>	11 28
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM_A_DQS_N<7>	11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0>	8 11 29 30 32
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0>	8 11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM_B_CKE<3..0>	11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM_B_CS_L<3..0>	11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM_B_ODT<3..0>	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM_B_A<15..0>	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM_B_BA<2..0>	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM_B_RAS_L	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM_B_CAS_L	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM_B_WE_L	11 29 30 32
MEM_B_DQ_BYTE0	MEM_45S	MEM_B_DATA_0	MEM_B_DQ<7..0>	11 29
MEM_B_DQ_BYTE1	MEM_45S	MEM_B_DATA_1	MEM_B_DQ<15..8>	11 29
MEM_B_DQ_BYTE2	MEM_45S	MEM_B_DATA_2	MEM_B_DQ<23..16>	11 29
MEM_B_DQ_BYTE3	MEM_45S	MEM_B_DATA_3	MEM_B_DQ<31..24>	11 29
MEM_B_DQ_BYTE4	MEM_45S	MEM_B_DATA_4	MEM_B_DQ<39..32>	11 30
MEM_B_DQ_BYTE5	MEM_45S	MEM_B_DATA_5	MEM_B_DQ<47..40>	11 30
MEM_B_DQ_BYTE6	MEM_45S	MEM_B_DATA_6	MEM_B_DQ<55..48>	11 30
MEM_B_DQ_BYTE7	MEM_45S	MEM_B_DATA_7	MEM_B_DQ<63..56>	11 30
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM_B_DQS_P<0>	11 29
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM_B_DQS_N<0>	11 29
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM_B_DQS_P<1>	11 29
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM_B_DQS_N<1>	11 29
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM_B_DQS_P<2>	11 29
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM_B_DQS_N<2>	11 29
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM_B_DQS_P<3>	11 29
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM_B_DQS_N<3>	11 29
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM_B_DQS_P<4>	11 30
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM_B_DQS_N<4>	11 30
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM_B_DQS_P<5>	11 30
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM_B_DQS_N<5>	11 30
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM_B_DQS_P<6>	11 30
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM_B_DQS_N<6>	11 30
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM_B_DQS_P<7>	11 30
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM_B_DQS_N<7>	11 30
		MEM_PWR	PP1V5_S3RS0	6 7
		MEM_PWR	PP1V5_S3	6 7
		MEM_PWR	PP0V75_S3_MEM_VREFCA_A	27 28 31
		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A	27 28 31

SYNC_MASTER=CONSTRAINTS SYNC_DATE=01/11/2012

PAGE TITLE: Memory Constraints

Apple Inc.

DRAWING NUMBER: 051-9276 SIZE: D

REVISION: 2.7.0

BRANCH:

PAGE: 101 OF 109

SHEET: 66 OF 72

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ICOMP	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA3_PCH_TX	SATA3_PCH_TX	*	SATA3_TX2TX
SATA3_PCH_RX	SATA3_PCH_RX	*	SATA3_RX2RX
SATA3_PCH_TX	*_PCH_TX	*	SATA3_TX2OTHERTX
SATA3_PCH_RX	*_PCH_RX	*	SATA3_RX2OTHERRX
SATA3_PCH_TX	*_PCH_RX	*	SATA3_TX2RX
SATA3_PCH_RX	*_PCH_TX	*	SATA3_RX2TX
SATA3_PCH_TX	*_TX	*	SATA3_2OTHERHS
SATA3_PCH_RX	*_TX	*	SATA3_2OTHERHS
SATA3_PCH_TX	*_RX	*	SATA3_2OTHERHS
SATA3_PCH_RX	*_RX	*	SATA3_2OTHERHS
SATA3_PCH_TX	*	*	SATA3_2OTHER
SATA3_PCH_RX	*	*	SATA3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
SATA3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
SATA3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
SATA3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA3_TX2TX	*	=2.5x_DIELECTRIC	?
SATA3_RX2RX	*	=2.5x_DIELECTRIC	?
SATA3_TX2OTHERTX	*	=4x_DIELECTRIC	?
SATA3_RX2OTHERRX	*	=4x_DIELECTRIC	?
SATA3_TX2RX	*	=6x_DIELECTRIC	?
SATA3_RX2TX	*	=6x_DIELECTRIC	?
SATA3_2OTHERHS	*	=4x_DIELECTRIC	?
SATA3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x_DIELECTRIC	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_PCH_TX	USB3_PCH_TX	*	USB3_TX2TX
USB3_PCH_RX	USB3_PCH_RX	*	USB3_RX2RX
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2OTHERTX
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2OTHERRX
USB3_PCH_TX	*_PCH_RX	*	USB3_TX2RX
USB3_PCH_RX	*_PCH_TX	*	USB3_RX2TX
USB3_PCH_TX	*_TX	*	USB3_2OTHERHS
USB3_PCH_RX	*_TX	*	USB3_2OTHERHS
USB3_PCH_TX	*_RX	*	USB3_2OTHERHS
USB3_PCH_RX	*_RX	*	USB3_2OTHERHS
USB3_PCH_TX	*	*	USB3_2OTHER
USB3_PCH_RX	*	*	USB3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	*	=2.5x_DIELECTRIC	?
USB3_RX2RX	*	=2.5x_DIELECTRIC	?
USB3_TX2OTHERTX	*	=4x_DIELECTRIC	?
USB3_RX2OTHERRX	*	=4x_DIELECTRIC	?
USB3_TX2RX	*	=6x_DIELECTRIC	?
USB3_RX2TX	*	=6x_DIELECTRIC	?
USB3_2OTHERHS	*	=4x_DIELECTRIC	?
USB3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SATA_PCH_MUX_R2D	SATA_80D	SATA3_PCH_TX	SATA_HDD_R2D_C_P	16 37
SATA_PCH_MUX_R2D	SATA_80D	SATA3_PCH_TX	SATA_HDD_R2D_C_N	16 37
	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_MUX_IN_P	37
	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_MUX_IN_N	37
SATA_MUX_SSD_R2D	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_P	6 37
SATA_MUX_SSD_R2D	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_N	6 37
SATA_PCH_MUX_D2R	SATA_80D	SATA3_PCH_RX	SATA_HDD_D2R_P	16 37
SATA_PCH_MUX_D2R	SATA_80D	SATA3_PCH_RX	SATA_HDD_D2R_N	16 37
	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_MUX_OUT_P	37
	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_MUX_OUT_N	37
SATA_MUX_SSD_D2R	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_P	6 37
SATA_MUX_SSD_D2R	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_N	6 37
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP	16
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_P	18 24
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_N	18 24
USB_BT	USB_80D	USB	USB_BT_P	24 36
USB_BT	USB_80D	USB	USB_BT_N	24 36
	USB_80D	USB	USB_BT_CONN_P	6 36
	USB_80D	USB	USB_BT_CONN_N	6 36
	USB_80D	USB	USB_BT_WAKE_P	36
	USB_80D	USB	USB_BT_WAKE_N	36
USB_TPAD	USB_80D	USB	USB_TPAD_P	6 48
USB_TPAD	USB_80D	USB	USB_TPAD_N	6 48
	USB_80D	USB	USB_TPAD_CONN_P	
	USB_80D	USB	USB_TPAD_CONN_N	
USB_TPAD_HUB	USB_80D	USB	USB_TPAD_HUB_P	24
USB_TPAD_HUB	USB_80D	USB	USB_TPAD_HUB_N	24
	USB_80D	USB	USB_TPAD_R_P	24 48
	USB_80D	USB	USB_TPAD_R_N	24 48
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_P	48
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_N	48
USB_SDCARD	USB_80D	USB	USB_SDCARD_P	8 24
USB_SDCARD	USB_80D	USB	USB_SDCARD_N	8 24
USB_SMC	USB_80D	USB	USB_SMC_P	24 40
USB_SMC	USB_80D	USB	USB_SMC_N	24 40
USB_CAMERA	USB_80D	USB	USB_CAMERA_P	6 18 39
USB_CAMERA	USB_80D	USB	USB_CAMERA_N	6 18 39
USB_EXTA	USB_80D	USB	USB_EXTA_P	18 38
USB_EXTA	USB_80D	USB	USB_EXTA_N	18 38
	UART_45S	UART	SMC_DEBUGPRT_TX_L	38 40 41
	UART_45S	UART	SMC_DEBUGPRT_RX_L	38 40 41
	USB_80D	USB	USB2_EXTA_MUXED_P	38
	USB_80D	USB	USB2_EXTA_MUXED_N	38
	USB_80D	USB	USB2_EXTA_MUXED_F_P	38
	USB_80D	USB	USB2_EXTA_MUXED_F_N	38
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_RX_P	18 38
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_RX_N	18 38
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_P	18 38
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_N	18 38
	USB_80D	USB3_PCH_RX	USB3_EXTA_RX_F_P	38
	USB_80D	USB3_PCH_RX	USB3_EXTA_RX_F_N	38
	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_F_P	38
	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_F_N	38
	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_C_P	38
	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_C_N	38
USB_EXTB	USB_80D	USB	USB_EXTB_P	6 24 39
USB_EXTB	USB_80D	USB	USB_EXTB_N	6 24 39
	USB_80D	USB	USB_EXTB_EHCI_P	18 24
	USB_80D	USB	USB_EXTB_EHCI_N	18 24
	USB_80D	USB	USB_EXTB_XHCI_P	18 24
	USB_80D	USB	USB_EXTB_XHCI_N	18 24
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_P	18 39
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_N	18 39
	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_RC_P	6 39
	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_RC_N	6 39
	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_CONN_P	
	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_CONN_N	
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_P	18 39
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_N	18 39
	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_C_P	6 39
	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_C_N	6 39
(USB_TPAD_HUB)	USB_80D	USB	USB_EXTD_XHCI_P	18 24
(USB_TPAD_HUB)	USB_80D	USB	USB_EXTD_XHCI_N	18 24
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	18
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_P	16
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_N	16
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_P	16
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_N	16
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_P	16
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_N	16
	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK	16

SATA SSD

USB Hub nets

USB Camera nets

USB EXTA nets (Right USB port)

USB EXTB nets (Left USB port)

Unused USB nets

SYNC_MASTER=CONSTRAINTS SYNC_DATE=01/11/2012

PAGE TITLE: PCH Constraints 1

Apple Inc.

DRAWING NUMBER: 051-9276 SIZE: D

REVISION: 2.7.0

BRANCH:

PAGE: 102 OF 109

SHEET: 67 OF 72

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x_DIELECTRIC	?
CLK_LPC	*	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S_R_50S	TOP,BOTTOM	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE		
SMB_45S_R_50S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x_DIELECTRIC	?

XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_ITP	*	=2:1_SPACING	?

DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	*	=3x_DIELECTRIC	?
DP_2OTHERHS	*	=4x_DIELECTRIC	?
DP_2OTHER	*	=3x_DIELECTRIC	?
DP_AUX	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_AUX	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_TX	DP_TX	*	DP_2DP
DP_TX	*_TX	*	DP_2OTHERHS
DP_TX	*_RX	*	DP_2OTHERHS
DP_TX	*	*	DP_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	6 16 40 42
LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L	6 16 40 42
	LPC_45S	LPC	LPCPLUS_RESET_L	6 25 42
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC	25 40
	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC_R	18 25
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 25 42
	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	18 25
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	PCH_CLK33M_PCIIN	16 25
	CLK_LPC_45S	CLK_LPC	PCH_CLK33M_PCIOUT	18 25
SMBUS_PCH_CLK	SMB_45S_R_50S	SMB	SMBUS_PCH_CLK	16 43
SMBUS_PCH_DATA	SMB_45S_R_50S	SMB	SMBUS_PCH_DATA	16 43
SMBUS_PCH_0_CLK	SMB_45S_R_50S	SMB	SML_PCH_0_CLK	16 43
SMBUS_PCH_0_DATA	SMB_45S_R_50S	SMB	SML_PCH_0_DATA	16 43
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SML_PCH_1_CLK	16 43
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SML_PCH_1_DATA	16 43
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	6 16 39
	HDA_45S	HDA	HDA_BIT_CLK_R	16
HDA_SYNC	HDA_45S	HDA	HDA_SYNC	6 16 39
	HDA_45S	HDA	HDA_SYNC_R	16
HDA_RST_L	HDA_45S	HDA	HDA_RST_R_L	16
	HDA_45S	HDA	HDA_RST_L	6 16 39
HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0	6 16 39
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	6 16 39
	HDA_45S	HDA	HDA_SDOUT_R	16 25
PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM_CLK32K_SUSCLK_R	17 41
	CLK_SLOW_45S	CLK_SLOW	SMC_CLK32K	40 41
SPI_CLK	SPI_45S	SPI	SPI_CLK_R	16 42
	SPI_45S	SPI	SPI_CLK	42
SPI_MOSI	SPI_45S	SPI	SPI_MOSI_R	16 42
	SPI_45S	SPI	SPI_MOSI	42
SPI_MISO	SPI_45S	SPI	SPI_MISO	16 42
SPI_CS0	SPI_45S	SPI	SPI_CS0_R_L	16 42
	SPI_45S	SPI	SPI_CS0_L	42
	SPI_45S	SPI	SPI_SMC_CLK	40 41
	SPI_45S	SPI	SPI_SMC_MOSI	40 41
	SPI_45S	SPI	SPI_SMC_MISO	40 41
	SPI_45S	SPI	SPI_SMC_CS_L	40 41
	SPI_45S	SPI	SPI_MLB_CLK	41 42 49
	SPI_45S	SPI	SPI_MLB_MOSI	41 42 49
	SPI_45S	SPI	SPI_MLB_MISO	41 42 49
	SPI_45S	SPI	SPI_MLB_CS_L	41 42 49
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_P	6 36
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_N	6 36
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_P	16 36
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_N	16 36
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_P	6 16 36
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_N	6 16 36
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_P	6 16 36
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_N	6 16 36
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_P<3..0>	33
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_N<3..0>	33
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_P<3..0>	8 33
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_N<3..0>	8 33
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_P<3..0>	8 33
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_N<3..0>	8 33
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_P<3..0>	33
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_N<3..0>	33
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_P	16 33
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_N	16 33
	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_P	8 16
	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_N	8 16
XDP_TDI	PCH_45S	PCH_ITP	XDP_PCH_TDI	16 23
XDP_TDO	PCH_45S	PCH_ITP	XDP_PCH_TDO	16 23
XDP_TMS	PCH_45S	PCH_ITP	XDP_PCH_TMS	16 23
XDP_TCK	PCH_45S	PCH_ITP	XDP_PCH_TCK	16 23

Chipset Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DP_TBT_MI	DP_80D	DP_TX	DP_TBTSNK0_ML_P<3..0>	33
DP_TBT_MI	DP_80D	DP_TX	DP_TBTSNK0_ML_N<3..0>	33
	DP_80D	DP_TX	DP_TBTSNK0_ML_C_P<3..0>	8 33
	DP_80D	DP_TX	DP_TBTSNK0_ML_C_N<3..0>	8 33
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_P	33
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_N	33
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_P	8 33
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_N	8 33
DP_TBT_MI	DP_80D	DP_TX	DP_TBTSNK1_ML_P<3..0>	33
DP_TBT_MI	DP_80D	DP_TX	DP_TBTSNK1_ML_N<3..0>	33
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_P<3..0>	8 33
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_N<3..0>	8 33
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_P	33
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_N	33
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_P	8 33
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_N	8 33

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTC	16 25
SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB	16 25
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB_R	16
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	25 33
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	33
SYSCLK_CLK25M_XTAL	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1	25
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2	25
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R	25

SYNC_MASTER=CONSTRAINTS SYNC_DATE=01/11/2012

PAGE TITLE: PCH Constraints 2

Apple Inc.

DRAWING NUMBER: 051-9276 SIZE: D

REVISION: 2.7.0

BRANCH:

PAGE: 103 OF 109

SHEET: 68 OF 72

DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_TX	TBTDP_TX	*	TBTDP_TX2TX
TBTDP_RX	TBTDP_RX	*	TBTDP_RX2RX
TBTDP_TX	TBTDP_RX	*	TBTDP_TX2RX
TBTDP_RX	TBTDP_TX	*	TBTDP_TX2RX
TBTDP_TX	*_TX	*	TBTDP_2OTHERHS
TBTDP_RX	*_TX	*	TBTDP_2OTHERHS
TBTDP_TX	*_RX	*	TBTDP_2OTHERHS
TBTDP_RX	*_RX	*	TBTDP_2OTHERHS
TBTDP_TX	*	*	TBTDP_2OTHER
TBTDP_RX	*	*	TBTDP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_TX2TX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_RX2RX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_TX2RX	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHERHS	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_TX2TX	*	=4x_DIELECTRIC	?
TBTDP_RX2RX	*	=4x_DIELECTRIC	?
TBTDP_TX2RX	*	=6x_DIELECTRIC	?
TBTDP_2OTHERHS	*	=6x_DIELECTRIC	?
TBTDP_2OTHER	*	=4x_DIELECTRIC	?

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_P<1..0>	33 63
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_N<1..0>	33 63
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_P<1..0>	63
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_N<1..0>	63
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_P<1>	33 63
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_N<1>	33 63
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_P<3>	33 63
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_N<3>	33 63
	DP_80D	DP_TX	DP_TBTPA_ML_P<3..1:2>	63
	DP_80D	DP_TX	DP_TBTPA_ML_N<3..1:2>	63
	DP_80D	DP_TX	DP_A_LSX_ML_P<1>	63
	DP_80D	DP_TX	DP_A_LSX_ML_N<1>	63
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_P<1..0>	63
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_N<1..0>	63
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<1>	33 63
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<1>	33 63
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<0>	33 63
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<0>	33 63
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_P	33 63
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_N	33 63
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_P	63
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_N	63
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_P	63
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_N	63
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_P	63
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_N	63
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_P<1..0>	8 33
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_N<1..0>	8 33
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_P<1..0>	
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_N<1..0>	
DP_TBTPB_ML	DP_80D	DP_TX	DP_TBTPB_ML_C_P<3..1:2>	8 33
DP_TBTPB_ML	DP_80D	DP_TX	DP_TBTPB_ML_C_N<3..1:2>	8 33
	DP_80D	DP_TX	DP_TBTPB_ML_P<3..1:2>	
	DP_80D	DP_TX	DP_TBTPB_ML_N<3..1:2>	
	DP_80D	DP_TX	DP_B_LSX_ML_P<1>	
	DP_80D	DP_TX	DP_B_LSX_ML_N<1>	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_P<1..0>	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_N<1..0>	
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_P<1..0>	8 33
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_N<1..0>	8 33
TBT_B_AUXCH	DP_80D	DP_AUX	DP_TBTPB_AUXCH_C_P	8 33
TBT_B_AUXCH	DP_80D	DP_AUX	DP_TBTPB_AUXCH_C_N	8 33
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_P	
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_N	
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_P	
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_N	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_P	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_N	

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DP_80D	DP_TX	DP_TBTSRC_ML_C_P<3..0>	
	DP_80D	DP_TX	DP_TBTSRC_ML_C_N<3..0>	
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_P	
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_N	
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK	33
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI	33
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO	33
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L	33

Only used on hosts supporting Thunderbolt video-in

SYNC_MASTER=CONSTRAINTS SYNC_DATE=01/11/2012

PAGE TITLE: Thunderbolt Constraints

Apple Inc.

DRAWING NUMBER: 051-9276 SIZE: D

REVISION: 2.7.0

BRANCH:

PAGE: 105 OF 109

SHEET: 69 OF 72

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_0_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SCL	40 43
SMBUS_SMC_0_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SDA	40 43
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL	40 43
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA	40 43
SMBUS_SMC_2_S3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SCL	40 43
SMBUS_SMC_2_S3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SDA	40 43
SMBUS_SMC_3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SCL	40 43
SMBUS_SMC_3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SDA	40 43
SMBUS_SMC_5_G3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SCL	40 43
SMBUS_SMC_5_G3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SDA	40 43

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSI_P	52
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSI_N	52
	1:1_DIFFPAIR		CHGR_CSI_R_P	52
	1:1_DIFFPAIR		CHGR_CSI_R_N	52
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSO_P	52
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSO_N	52
	1:1_DIFFPAIR		CHGR_CSO_R_P	52
	1:1_DIFFPAIR		CHGR_CSO_R_N	52

SYNC_MASTER=CONSTRAINTS SYNC_DATE=01/11/2012

PAGE TITLE

SMC Constraints

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D

REVISION 2.7.0

BRANCH

PAGE 106 OF 109

SHEET 70 OF 72

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SENSE_1TO1_P2MM	*	=1:1_DIFFPAIR	0.200 MM	0.100 MM	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SPKR_DIFFPAIR	*	=1:1_DIFFPAIR	0.300 MM	0.100 MM	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCIE	*	GND_P2MM
GND	PCIE*	*	GND_P2MM
GND	SATA*	*	GND_P2MM
GND	USB*	*	GND_P2MM
GND	LVDS*	*	GND_P2MM
SB_POWER	CLK_PCIE	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM

J11/J13 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_P	45 46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_N	45 46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_THERMD_P	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_THERMD_N	46
	THERM_1TO1_45S	THERM	TBT_MLBBOT_THMSNS_P	46
	THERM_1TO1_45S	THERM	TBT_MLBBOT_THMSNS_N	46
	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_R_P	46
	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_R_N	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPU_THERMD_P	9 46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPU_THERMD_N	9 46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_P	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_N	46
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVCCIOS0_CS_N	44 58
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVCCIOS0_CS_P	44 58
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISNS1_P	44 56 57
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISNS1_N	44 57
	SENSE_1TO1_45S	SENSE	CPUIMVP_ISUM_R_P	44
	SENSE_1TO1_45S	SENSE	CPUIMVP_ISUM_R_N	44
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISNS1G_P	44 57
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISNS1G_N	44 57
	SENSE_1TO1_45S	SENSE	CPUIMVP_ISUMG_R_P	44
	SENSE_1TO1_45S	SENSE	CPUIMVP_ISUMG_R_N	44
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	VCCSAS0_CS_P	44 53
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	VCCSAS0_CS_N	44 53
	SENSE_1TO1_45S	SENSE	VCCSAISNS_R_P	44
	SENSE_1TO1_45S	SENSE	VCCSAISNS_R_N	44
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3S0_P	44 60
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3S0_N	44 60
	SENSE_1TO1_45S	SENSE	ISNS_3V3S0_R_P	44
	SENSE_1TO1_45S	SENSE	ISNS_3V3S0_R_N	44
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISUMG_P	56 57
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISUMG_N	56 57
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISUM_P	56 57
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISUM_N	56 57
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N	8 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P	8 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER_N	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER_P	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V5_S3_N	45 55
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V5_S3_P	45 55
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_N	36 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_P	36 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_N	37 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_P	37 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N	8 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P	8 45
AUD_DIFF	1:1_DIFFPAIR	AUDIO	SPKRAMP_INR_P	6 39 50
AUD_DIFF	1:1_DIFFPAIR	AUDIO	SPKRAMP_INR_N	6 39 50
	1:1_DIFFPAIR	AUDIO	MAX98300_R_P	50
	1:1_DIFFPAIR	AUDIO	MAX98300_R_N	50
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_P	6 50 51
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_N	6 50 51
		SB_POWER	PP3V3_S5	6 7
		SB_POWER	PP3V3_S0	6 7
		GND	GND	

SYNC_MASTER=CONSTRAINTS SYNC_DATE=01/11/2012

PAGE TITLE

Project Specific Constraints

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D

REVISION 2.7.0

BRANCH

PAGE 108 OF 109

SHEET 71 OF 72

J11/J13 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	TOP,BOTTOM	Y	=50_OHM_SE	=50_OHM_SE			
DEFAULT	ISL2,ISL11	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL3,ISL10	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL4,ISL9	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	*	N	100 MM	100 MM	10 MM	0 MM	0 MM
STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

Single-ended Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	ISL2,ISL11	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL3,ISL10	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL4,ISL9	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.195 MM	0.195 MM			
35_OHM_SE	ISL2,ISL11	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL3,ISL10	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL4,ISL9	Y	0.125 MM	0.125 MM			
35_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL2,ISL11	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL3,ISL10	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL4,ISL9	Y	0.099 MM	0.099 MM			
40_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.135 MM			
45_OHM_SE	ISL2,ISL11	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL3,ISL10	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL4,ISL9	Y	0.080 MM	0.080 MM			
45_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Differential Pair Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.165 MM		0.130 MM	0.130 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.109 MM	0.109 MM		0.150 MM	0.150 MM
72_OHM_DIFF	ISL3,ISL10	Y	0.109 MM	0.109 MM		0.150 MM	0.150 MM
72_OHM_DIFF	ISL4,ISL9	Y	0.114 MM	0.114 MM		0.150 MM	0.150 MM
72_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	TOP,BOTTOM	Y	0.132 MM	0.132 MM		0.130 MM	0.130 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL3,ISL10	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL4,ISL9	Y	0.088 MM	0.088 MM		0.110 MM	0.110 MM
80_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Spacing Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.100 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.071 MM	?
1x_DIELECTRIC	ISL3,ISL10	0.053 MM	?
1x_DIELECTRIC	ISL4,ISL9	0.050 MM	?
1x_DIELECTRIC	*	0.090 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

SYNC MASTER=CONSTRAINTS SYNC_DATE=01/11/2012

PAGE TITLE

PCB Rule Definitions

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D

REVISION 2.7.0

BRANCH

PAGE 109 OF 109

SHEET 72 OF 72