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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.  
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.  
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

Tue Jul 5 21:36:16 2011

REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
12	0001170763	ENGINEERING RELEASED		2011-07-05

# N94 POR MLB\_V3 DVT FOR BOARD\_REV11/REV12

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SCH 051-8890  
 BRD 820-3031  
 MCO 056-4257

BOM 639-1723(16G,GUC,US)  
 BOM 639-1724(32G,GUC,US)  
 BOM 639-1777(64G,GUC,US)  
 BOM 639-2727(16G,GU,US)  
 BOM 639-2728(32G,GU,US)  
 BOM 639-2729(64G,GU,US)  
 BOM 639-2788(16G,GU,EU)  
 BOM 639-2789(32G,GU,EU)  
 BOM 639-2790(64G,GU,EU)

## N94 EEEE BOM LABELS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-2029	1	EEEE FOR 639-1723 (16G)	EEEE_DJF1	Y	EEEE_16G_GUC_US
825-2029	1	EEEE FOR 639-1724 (32G)	EEEE_DJF2	Y	EEEE_32G_GUC_US
825-2029	1	EEEE FOR 639-1777 (64G)	EEEE_DK00	Y	EEEE_64G_GUC_US
825-2029	1	EEEE FOR 639-2727 (16G)	EEEE_DQ5M	Y	EEEE_16G_GU_US
825-2029	1	EEEE FOR 639-2728 (32G)	EEEE_DQ5D	Y	EEEE_32G_GU_US
825-2029	1	EEEE FOR 639-2729 (64G)	EEEE_DQ5G	Y	EEEE_64G_GU_US
825-2029	1	EEEE FOR 639-2788 (16G)	EEEE_DR42	Y	EEEE_16G_GU_EU
825-2029	1	EEEE FOR 639-2789 (32G)	EEEE_DR44	Y	EEEE_32G_GU_EU
825-2029	1	EEEE FOR 639-2790 (64G)	EEEE_DR41	Y	EEEE_64G_GU_EU

## WIFI/BT MODULE BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S0143	1	MURATA WIFI_BT MODULE	U1_RF	Y	WIFI_BT_MODULE

## WIFI/BT MODULE ALTERNATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S0154	339S0143	WIFI_BT_MODULE	U1_RF	USI WIFI_BT_MODULE
339S0155	339S0143	WIFI_BT_MODULE	U1_RF	SEMCO WIFI_BT_MODULE

## UPPER ANTENNA MATCHING BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	
131S0318	1	CAP,CER,COG,1.6PF,+/-0.1PF,25V	0201,HQ	C6_RF	Y	UAT_US
152S0562	1	IND,WV,HF,5.1NH,+/-0.2NH,470MA	03015	L12_RF	Y	UAT_US
C66_RF = NOSTUFF						
131S0364	1	CAP,CER,4.7PF,+/-0.1PF,25V,COG	0201,HQ	C86_RF	Y	UAT_US
152S1240	1	IND,WV,HF,4.3NH,+/-0.2NH,530MA	03015	L14_RF	Y	UAT_US
131S0279	1	CAP,CER,COG,1.3PF,+/-0.1PF,25V	0201,HQ	C6_RF	Y	UAT_EU
152S0562	1	IND,WV,HF,5.1NH,+/-0.2NH,470MA	03015	L12_RF	Y	UAT_EU
131S0278	1	CAP,CER,CCOG,HF,1PF,+/-0.1PF,25V	0201,HQ	C66_RF	Y	UAT_EU
131S0449	1	CAP,CER,3.6PF,+/-0.1PF,25V,COG	0201,HQ	C86_RF	Y	UAT_EU
152S1240	1	IND,WV,HF,4.3NH,+/-0.2NH,530MA	03015	L14_RF	Y	UAT_EU

## 4.3UF CAP ALTERNATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0702	138S0657			MURATA 4.3UF CAP

## INVERTER GATE ALTERNATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0549	311S0539		U19_RF	TI INVERTER GATE

## AND GATE ALTERNATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0548	311S0398		U18_RF,U20_RF	TI 2-INPUT AND GATE

## 19.2MHZ ALTERNATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0402	197S0340		Y1_RF	NDK 19.2MHZ XTAL

## N94 SCH & PCB BOM CALLOUT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-8890	1	N94_MLB_V3 SCHEMATIC	SCH	Y	?
820-3031	1	N94_MLB_V3 PCB	PCB	Y	?

## NAND BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0781	1	16G,HYNIX 26NM PPN10 TLGA52	U1	Y	NAND_16GB_PPN10
335S0782	1	32G,HYNIX 26NM PPN10 TLGA52	U1	Y	NAND_32GB_PPN10
335S0814	1	64G,HYNIX 26NM PPN10 TLGA52	U1	Y	NAND_64GB_PPN10

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0815	335S0781	NAND_16GB_PPN10	U1	16G,SAMSUNG,27NM PPN10
335S0804	335S0781	NAND_16GB_PPN10	U1	16G,TOSHIBA,24NM PPN10
335S0816	335S0782	NAND_32GB_PPN10	U1	32G,SAMSUNG,27NM PPN10
335S0805	335S0782	NAND_32GB_PPN10	U1	32G,TOSHIBA,24NM PPN10
335S0806	335S0814	NAND_64GB_PPN10	U1	64G,TOSHIBA,24NM PPN10

## VIDEO BUFFER ALTERNATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
343S0539	343S0520		U9	INTERSIL VIDEO BUFFER

## 32KHZ XTAL ALTERNATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0382	197S0392		Y1	TXC XTAL

## STROBE INDUCTOR ALTERNATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S1173	152S0979		L9	CYNTEC INDUCTOR

## CHARGER INDUCTOR ALTERNATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S1051	152S0927		L28	CYNTEC INDUCTOR

## LEVEL TRANSLATOR ALTERNATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0562	311S0372		U11	TI LEVEL TRANSLATOR

## THERMISTOR ALTERNATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
107S0208	107S0150		R21,R22,R34,R35	MURATA THERMISTOR

DRAWING TITLE		DRAWING NUMBER		SIZE
N94 MLB_V3		051-8890		D
Apple Inc.		REVISION		12.0.0
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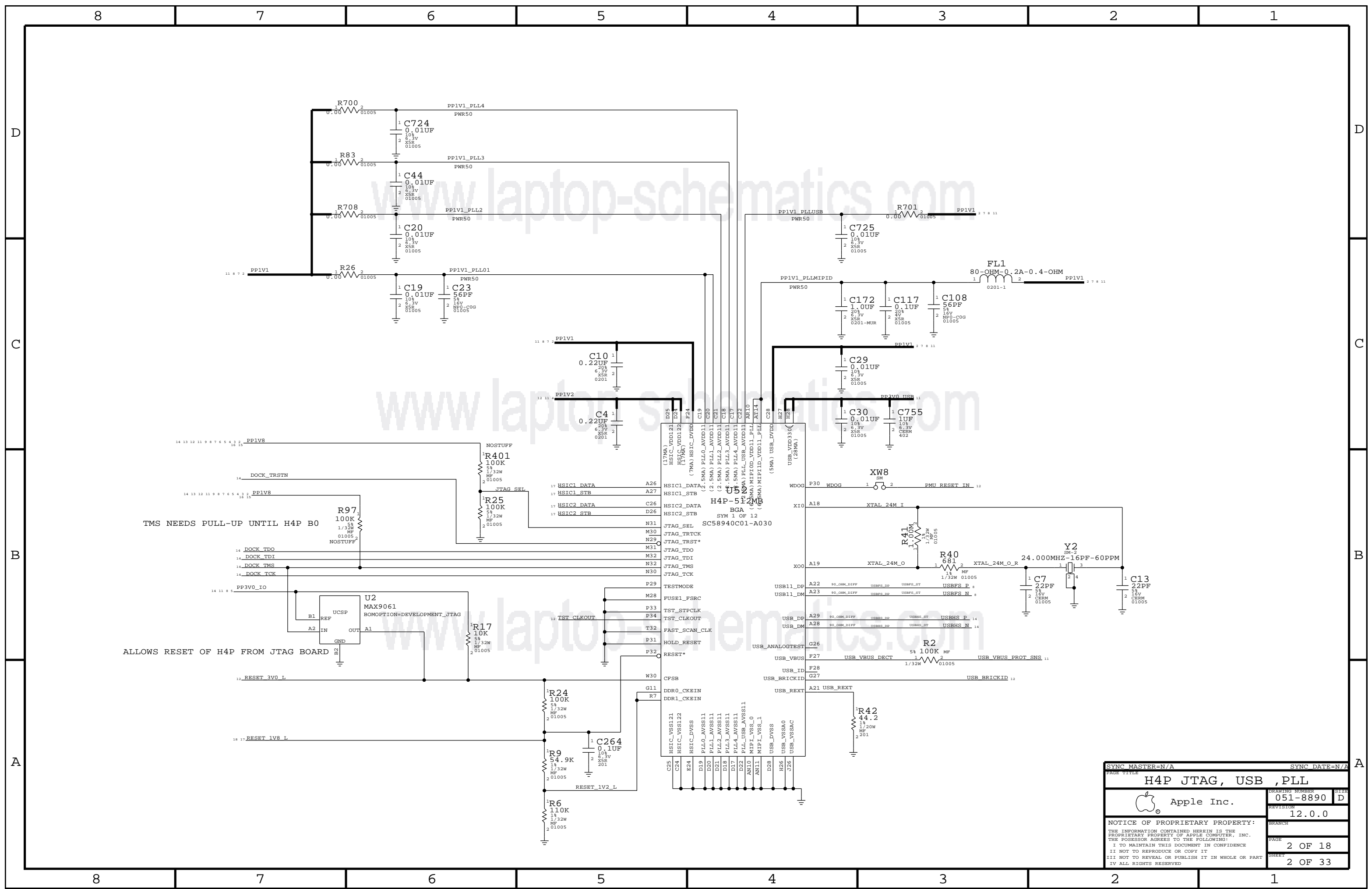
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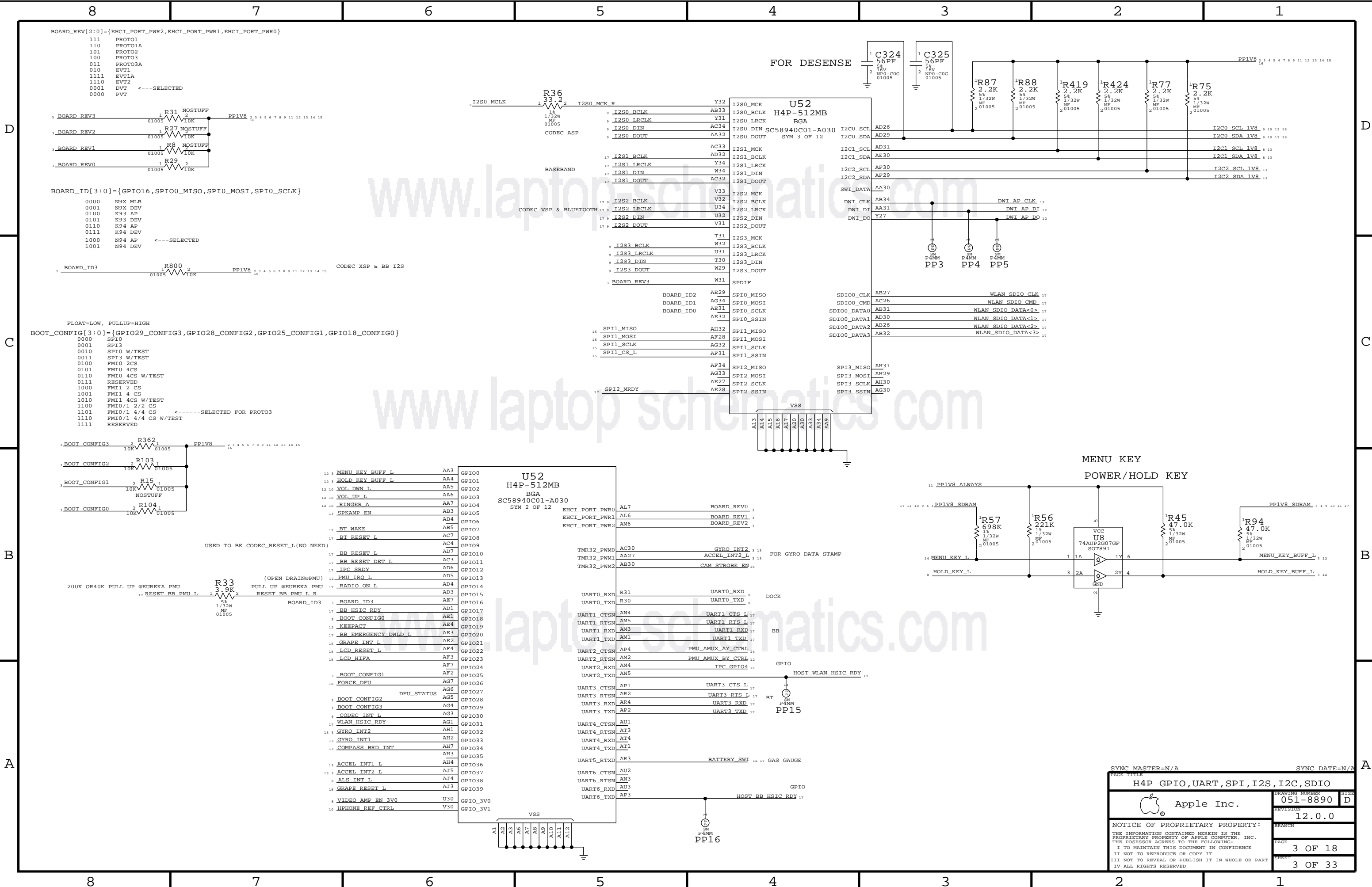
1



TMS NEEDS PULL-UP UNTIL H4P B0

ALLOWS RESET OF H4P FROM JTAG BOARD

PAGE TITLE		SYNC DATE=N/A	
<b>H4P JTAG, USB ,PLL</b>			
Apple Inc.		DRAWING NUMBER	051-8890
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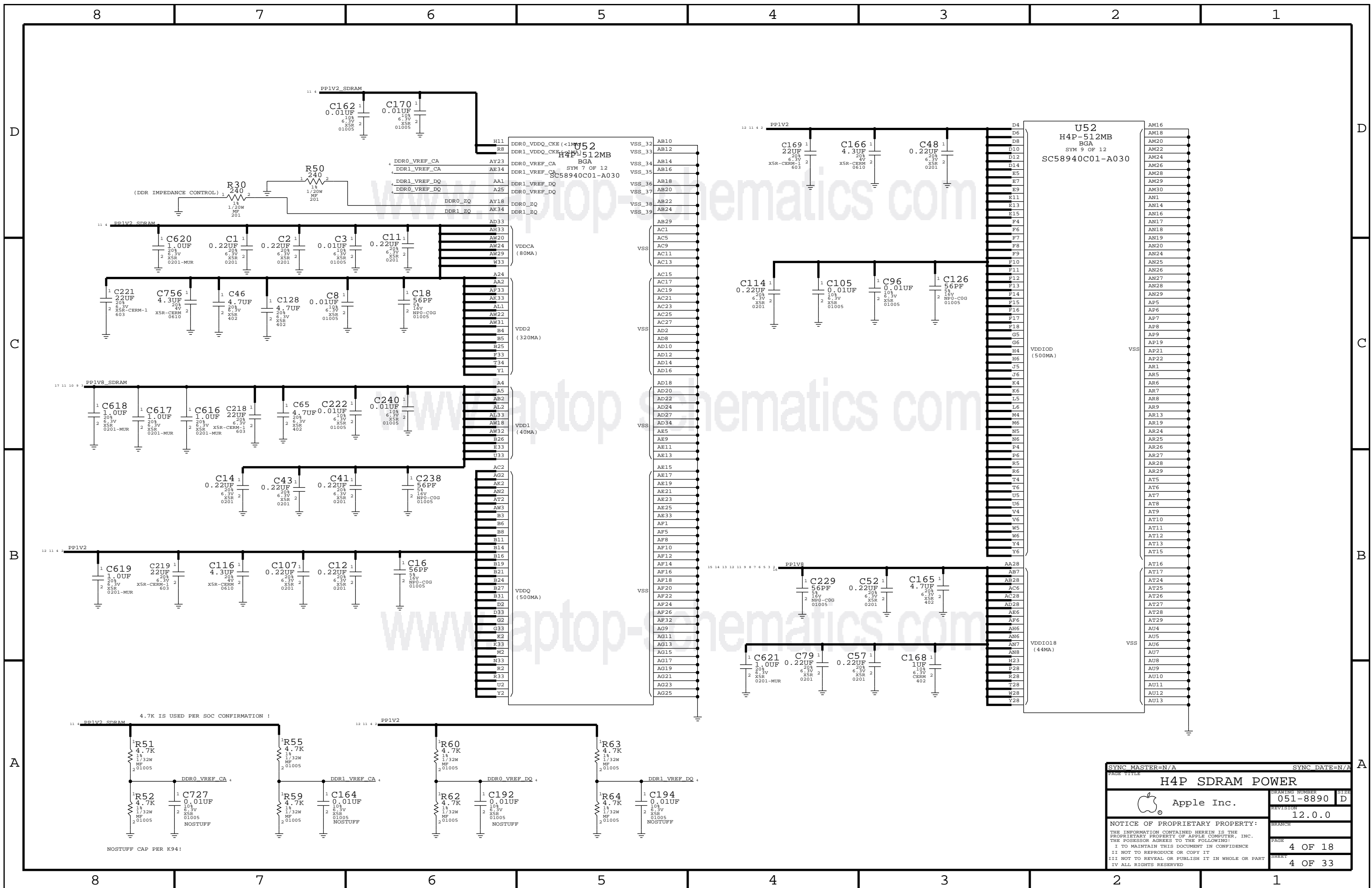
```
BOARD_REV[2:0]={EHCI_PORT_PWR2,EHCI_PORT_PWR1,EHCI_PORT_PWR0}
111 PROTO1
110 PROTO1A
101 PROTO2
100 PROTO3
011 PROTO3A
010 EVT1
1111 EVT1A
1110 EVT2
0001 DVT
0000 PVT <---SELECTED
```

```
BOARD_ID[3:0]={GPIO16,SPI0_MISO,SPI0_MOSI,SPI0_SCLK}
0000 N9X MLB
0001 N9X DEV
0100 K93 AP
0101 K93 DEV
0110 K94 AP
0111 K94 DEV
1000 N94 AP <---SELECTED
1001 N94 DEV
```

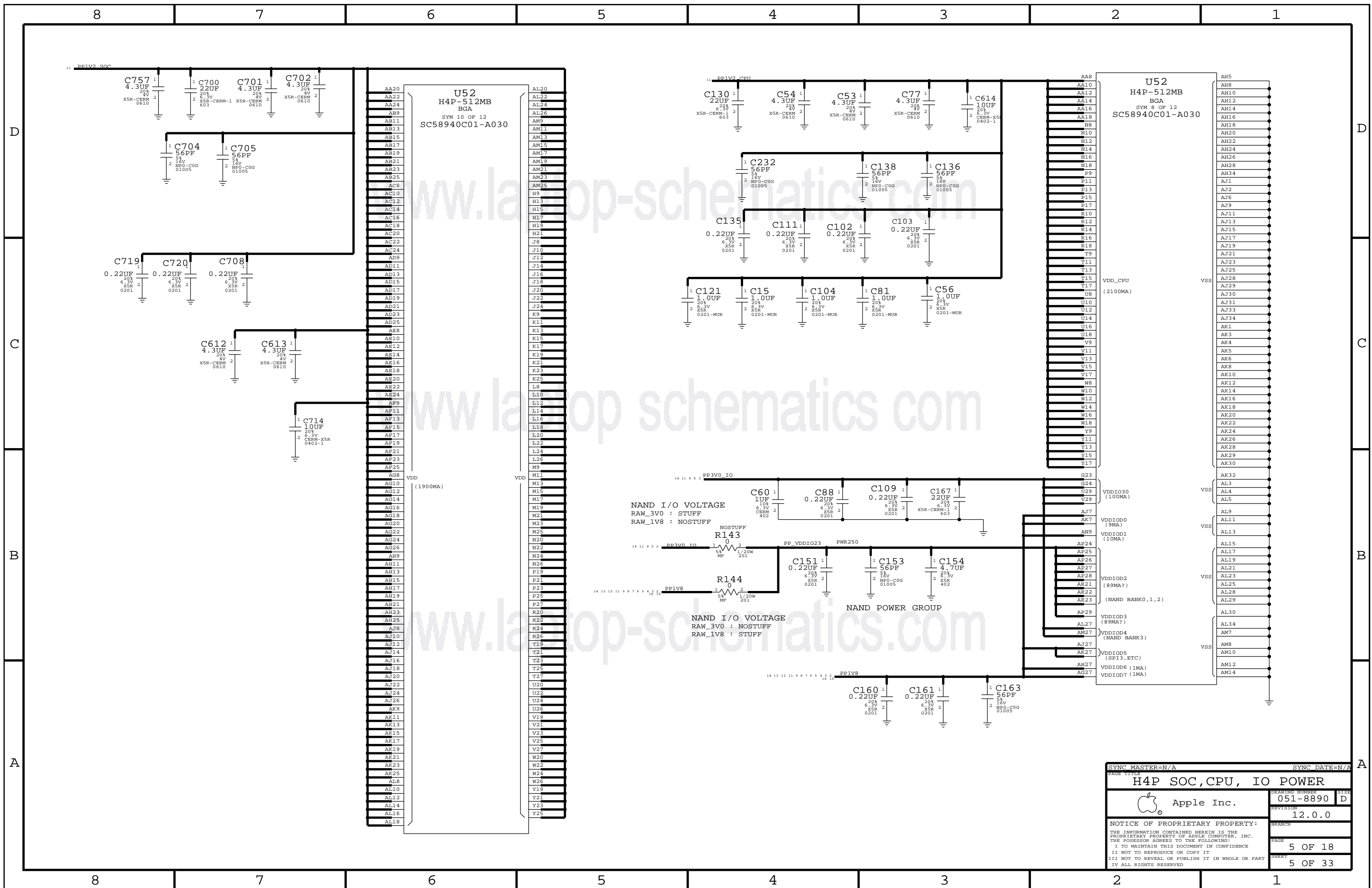
```
BOOT_CONFIG[3:0]={GPIO29_CONFIG3,GPIO28_CONFIG2,GPIO25_CONFIG1,GPIO18_CONFIG0}
0000 SPI0
0001 SPI3
0010 SPI0 W/TEST
0011 SPI3 W/TEST
0100 FMIO 2CS
0101 FMIO 4CS
0110 FMIO 4CS W/TEST
0111 RESERVED
1000 FMIL 2 CS
1001 FMIL 4 CS
1010 FMIL 4CS W/TEST
1100 FMIO/1 2/2 CS
1101 FMIO/1 4/4 CS <-----SELECTED FOR PROTO3
1110 FMIO/1 4/4 CS W/TEST
1111 RESERVED
```

Pin	Signal	Pin	Signal
AA3	GPIO0	AA7	BOARD_REV0
AA4	GPIO1	AA8	BOARD_REV1
AA5	GPIO2	AA9	BOARD_REV2
AA6	GPIO3		
AA7	GPIO4		
AA8	GPIO5		
AA9	GPIO6		
AB4	GPIO7		
AB5	GPIO8		
AC4	GPIO9		
AD7	GPIO10		
AC3	GPIO11		
AD6	GPIO12		
AD5	GPIO13		
AD4	GPIO14		
AD3	GPIO15		
AE7	GPIO16		
AD1	GPIO17		
AE1	GPIO18		
AE4	GPIO19		
AE3	GPIO20		
AE2	GPIO21		
AF4	GPIO22		
AF3	GPIO23		
AF7	GPIO24		
AF2	GPIO25		
AG7	GPIO26		
AG6	GPIO27		
AG5	GPIO28		
AG4	GPIO29		
AG3	GPIO30		
AG1	GPIO31		
AH1	GPIO32		
AH2	GPIO33		
AH7	GPIO34		
AH3	GPIO35		
AH4	GPIO36		
AJ5	GPIO37		
AJ4	GPIO38		
AJ3	GPIO39		
U30	GPIO_3V0		
V30	GPIO_3V1		

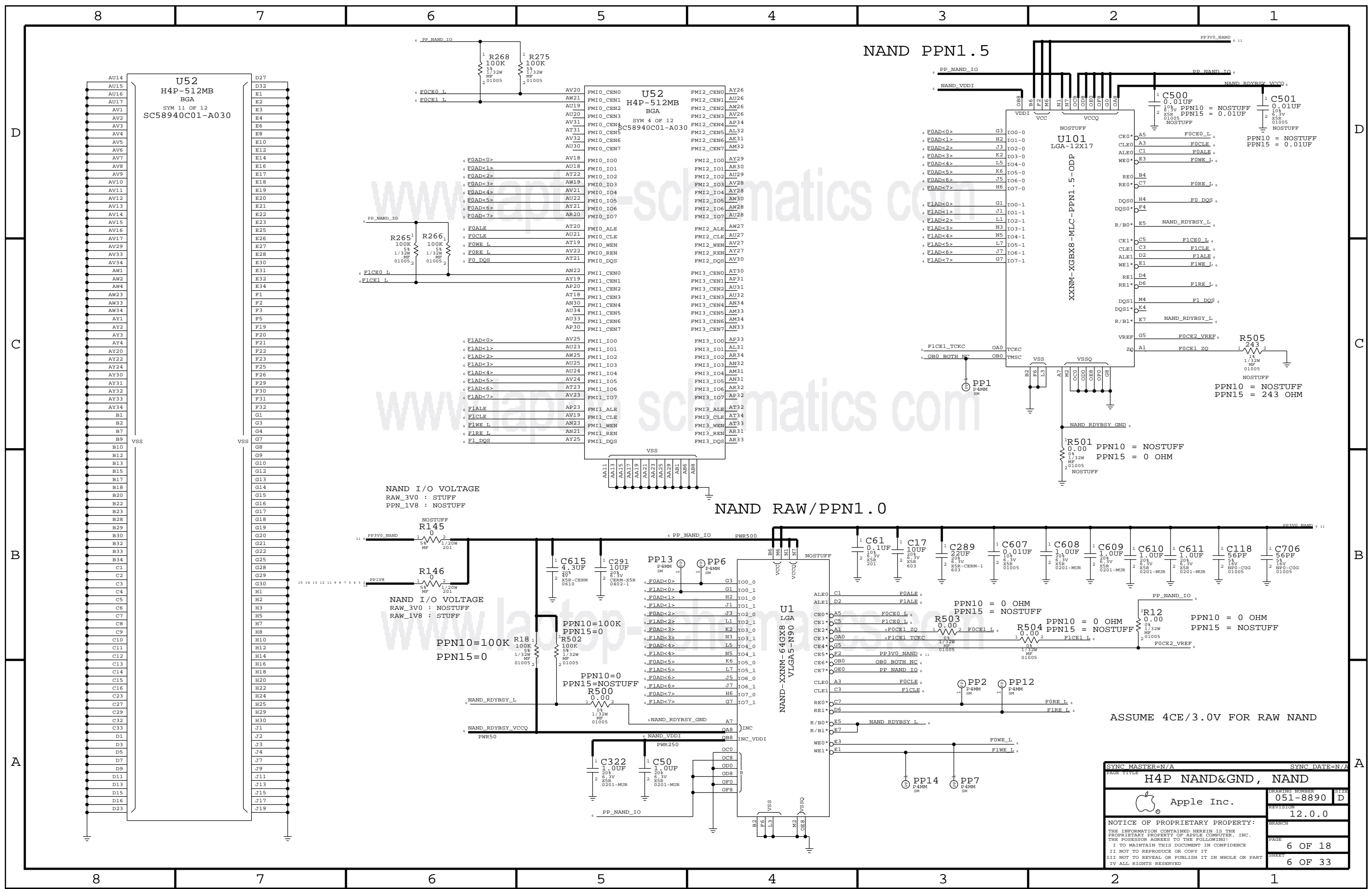
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H4P GPIO, UART, SPI, I2S, I2C, SDIO		DRAWING NUMBER	051-8890
Apple Inc.		REVISION	12.0.0
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<b>H4P SDRAM POWER</b>			
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SYNC MASTER=N/A		SYNC DATE=N/A	
PAGE TITLE <b>H4P SOC, CPU, IO POWER</b>			
DRAWING NUMBER 051-8890		SIZE D	
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NAND I/O VOLTAGE  
 RAW\_3V0 : STUFF  
 PPN\_1V8 : NOSTUFF

NAND I/O VOLTAGE  
 RAW\_3V0 : NOSTUFF  
 RAW\_1V8 : STUFF

PPN10=100K  
 PPN15=0

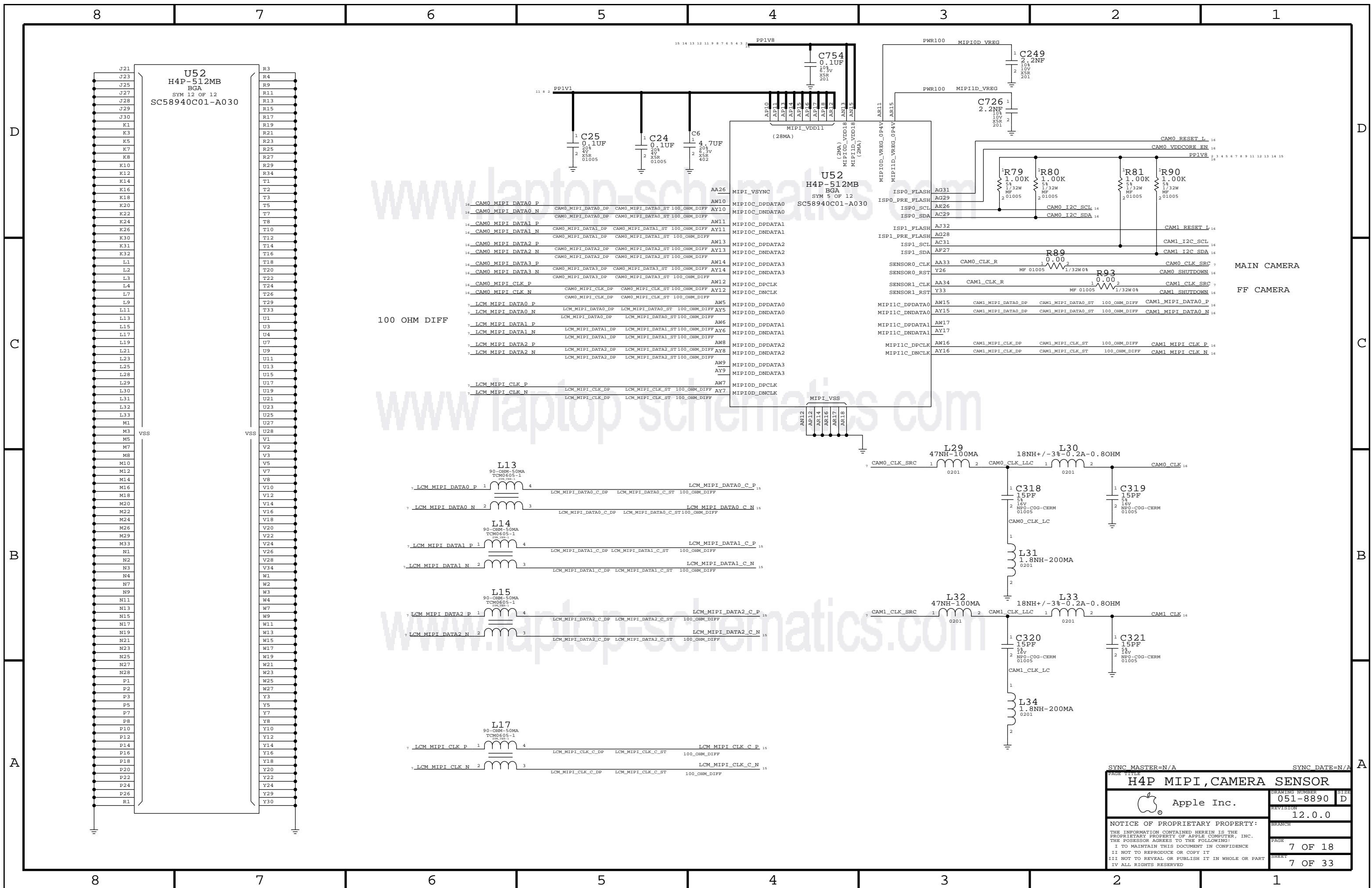
PPN10=100K  
 PPN15=0

PPN10=0  
 PPN15=NOSTUFF

NAND RAW/PPN1.0

ASSUME 4CE/3.0V FOR RAW NAND

SYNC MASTER=N/A		SYNC DATE=N/A	
PAGE TITLE			
H4P NAND&GND, NAND		DRAWING NUMBER	051-8890
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U52  
H4P-512MB  
BGA  
SYM 12 OF 12  
SC58940C01-A030

U52  
H4P-512MB  
BGA  
SYM 5 OF 12  
SC58940C01-A030

www.laptop-schematics.com

100 OHM DIFF

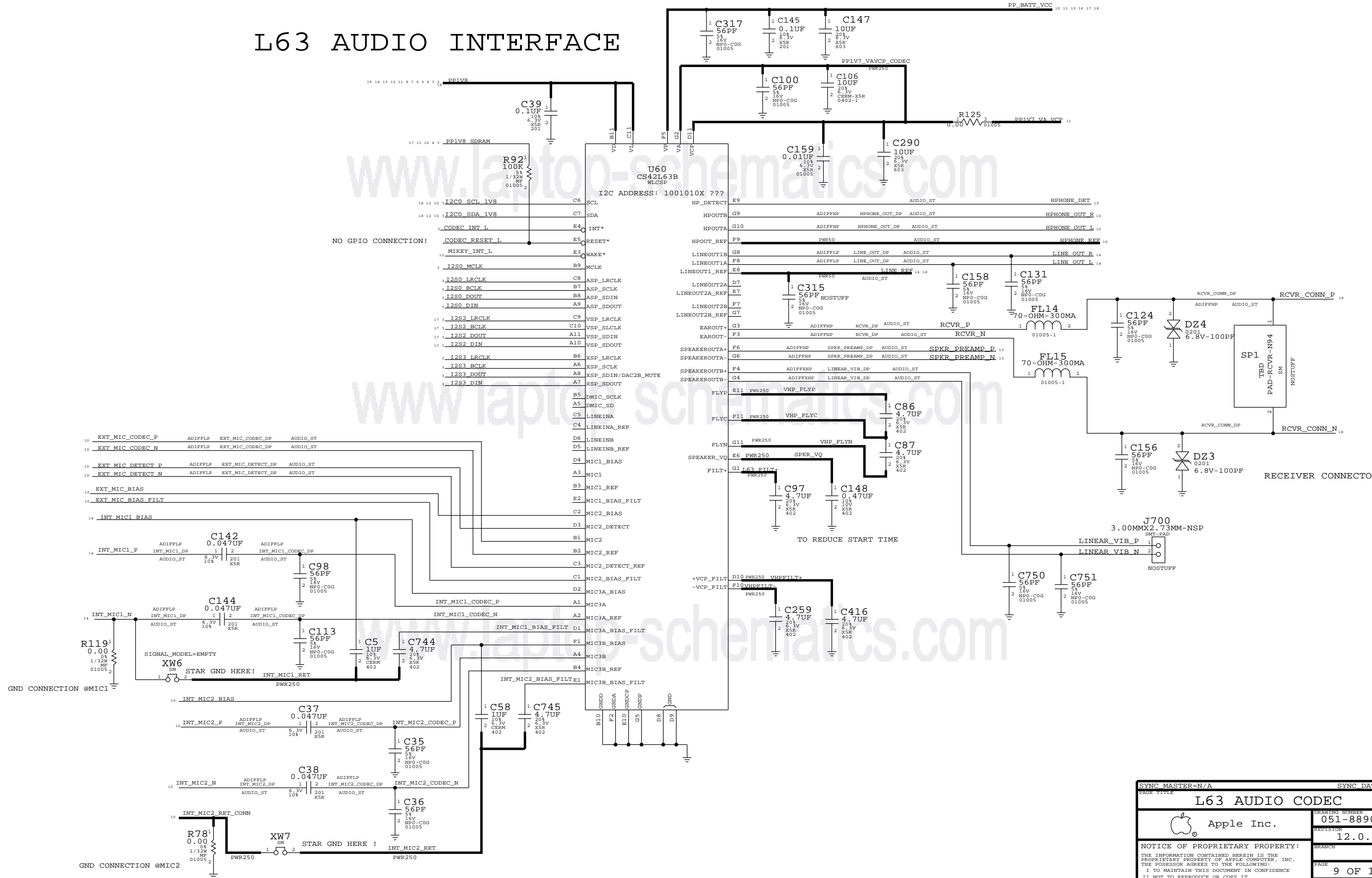
www.laptop-schematics.com

MAIN CAMERA  
FF CAMERA

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<b>H4P MIPI , CAMERA SENSOR</b>			
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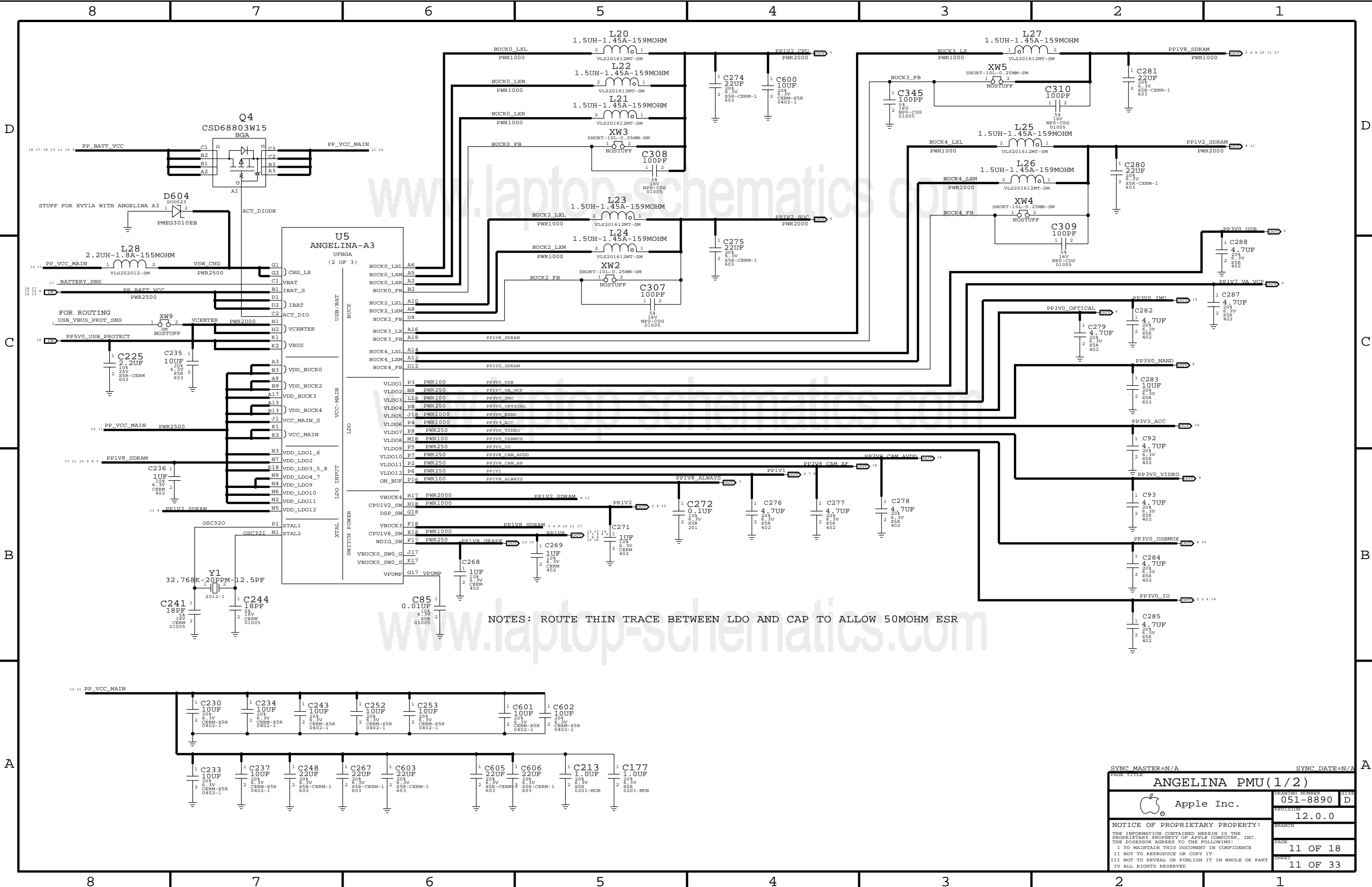


# L63 AUDIO INTERFACE



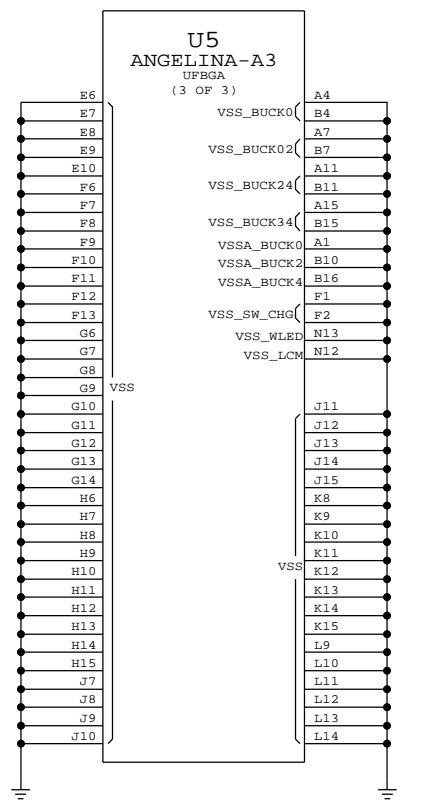
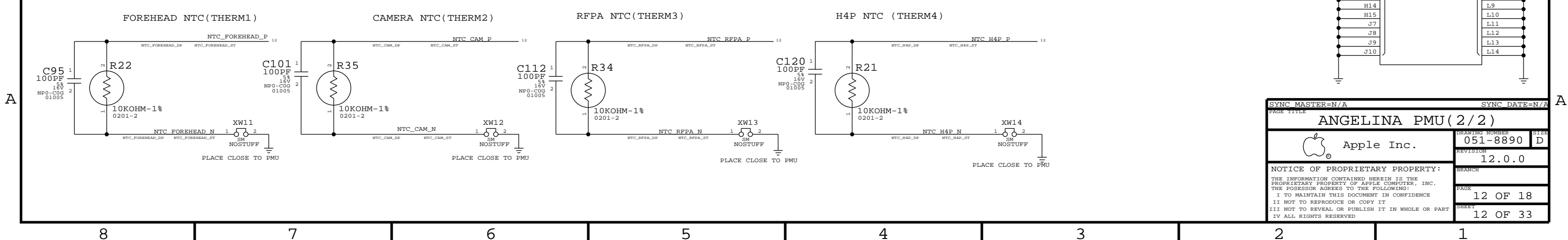
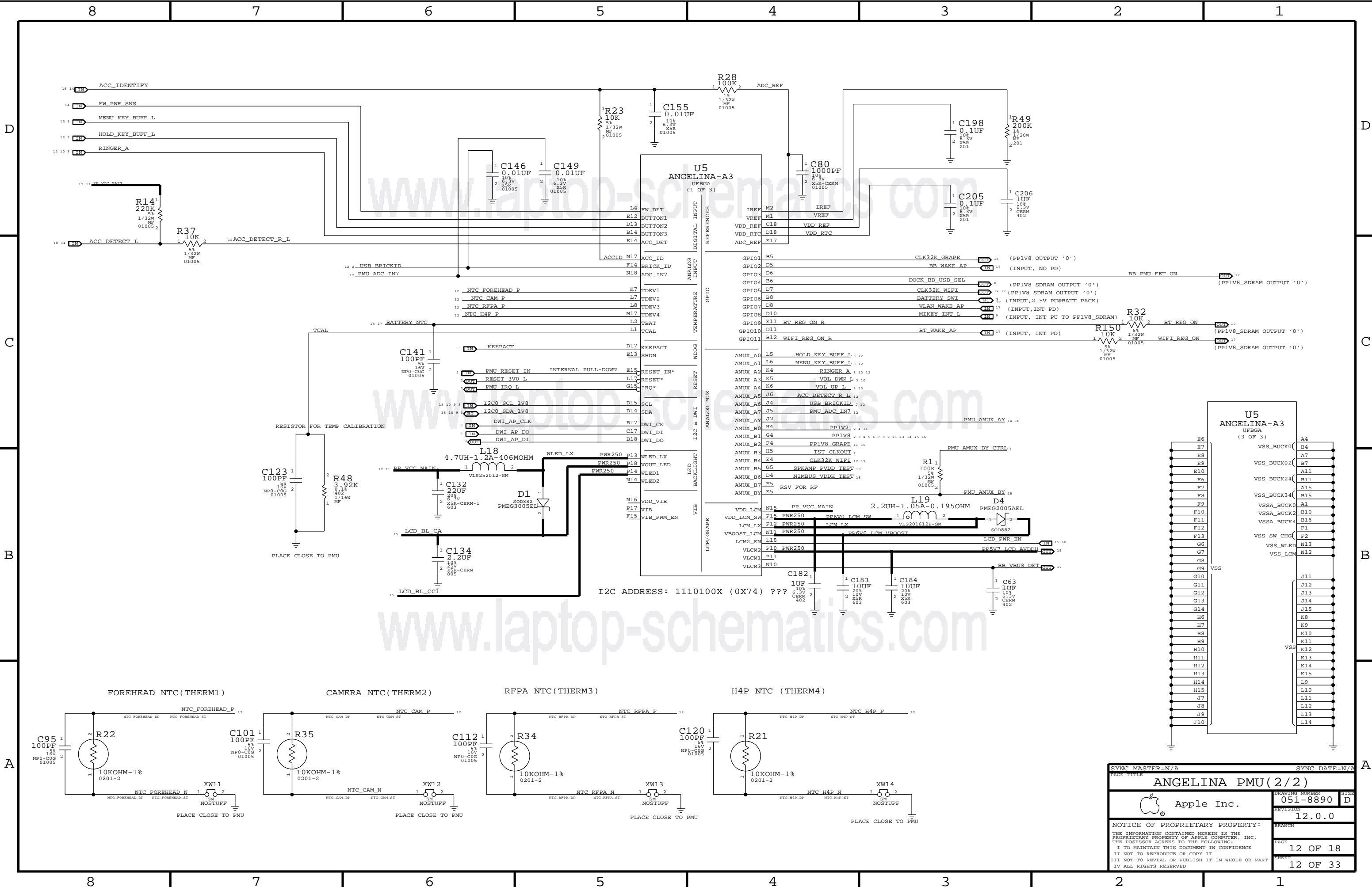
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<b>L63 AUDIO CODEC</b>			
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	REVISION	12.0.0	
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			9 OF 33



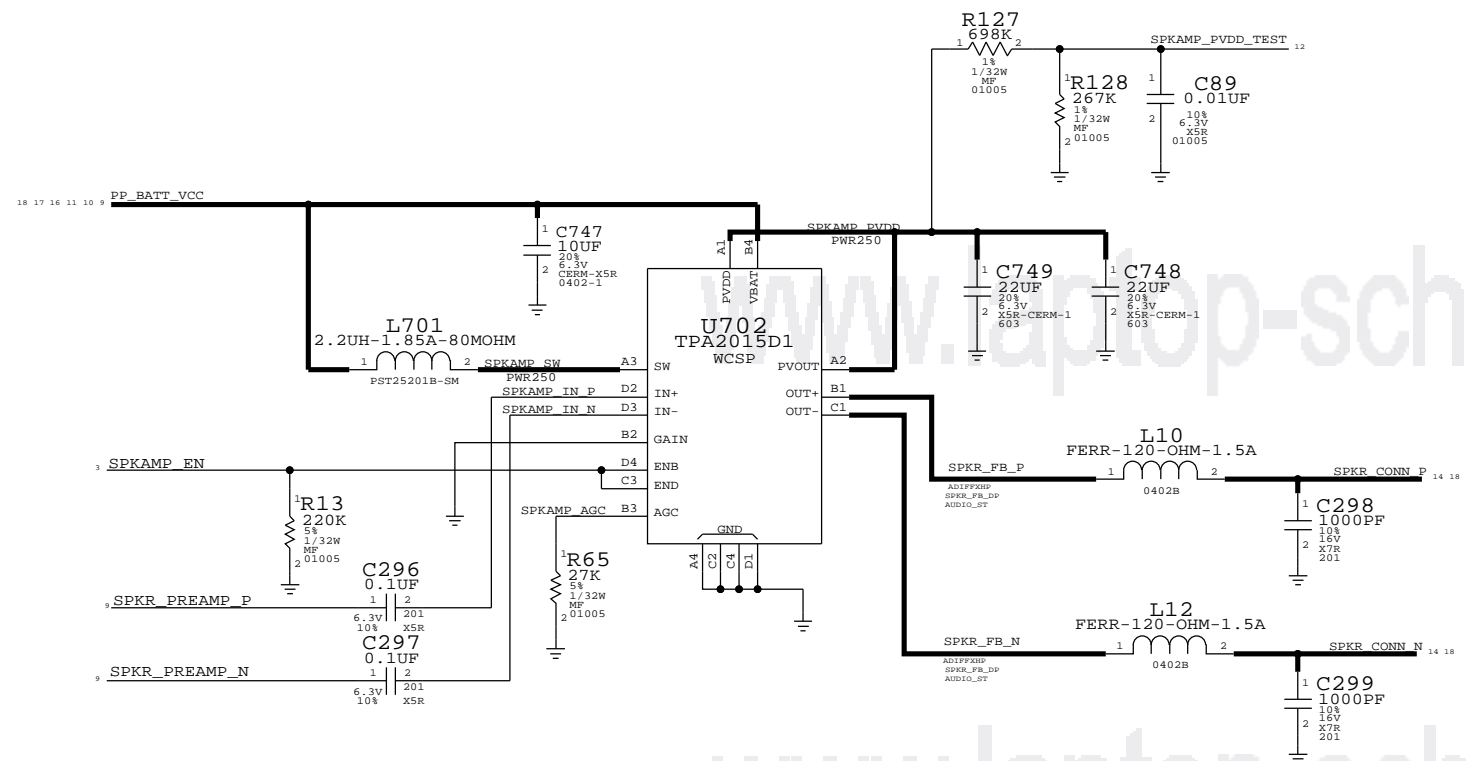


NOTES: ROUTE THIN TRACE BETWEEN LDO AND CAP TO ALLOW 50MOHM ESR

SYNC MASTER=N/A		SYNC DATE=N/A	
<b>ANGELINA PMU(1/2)</b>			
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		REVISION	12.0.0
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		SHEET	11 OF 33

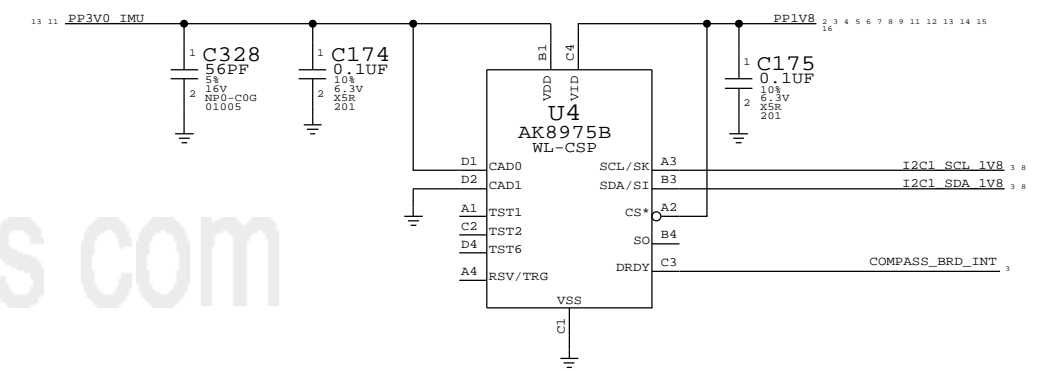


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		SHEET	12 OF 33



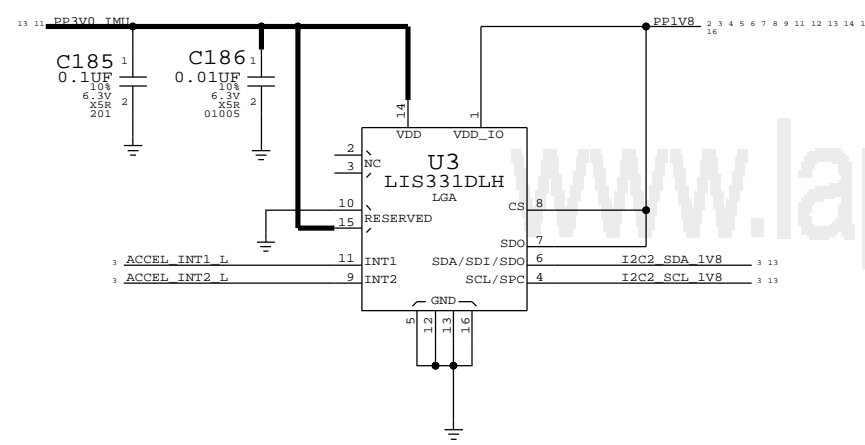
### COMPASS OPTION1

I2C ADDR: 0001100X (0X0D)



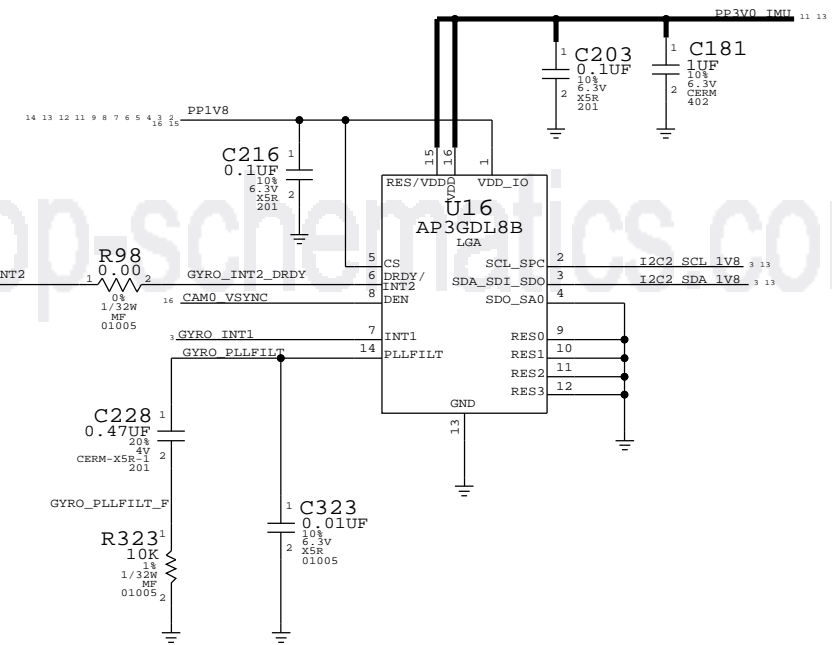
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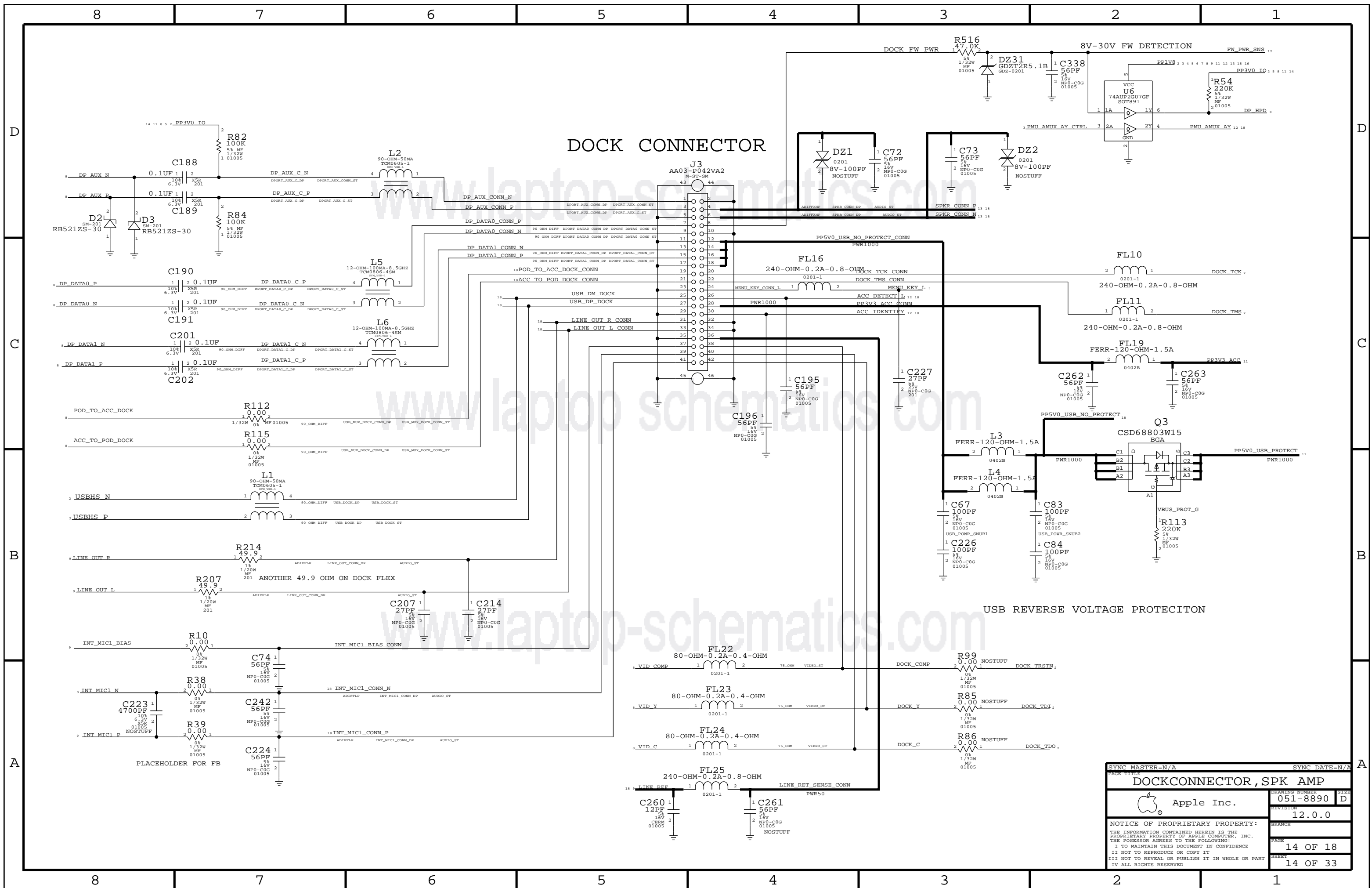


### GYRO 8KHZ

I2C ADDRESS: 0XD0

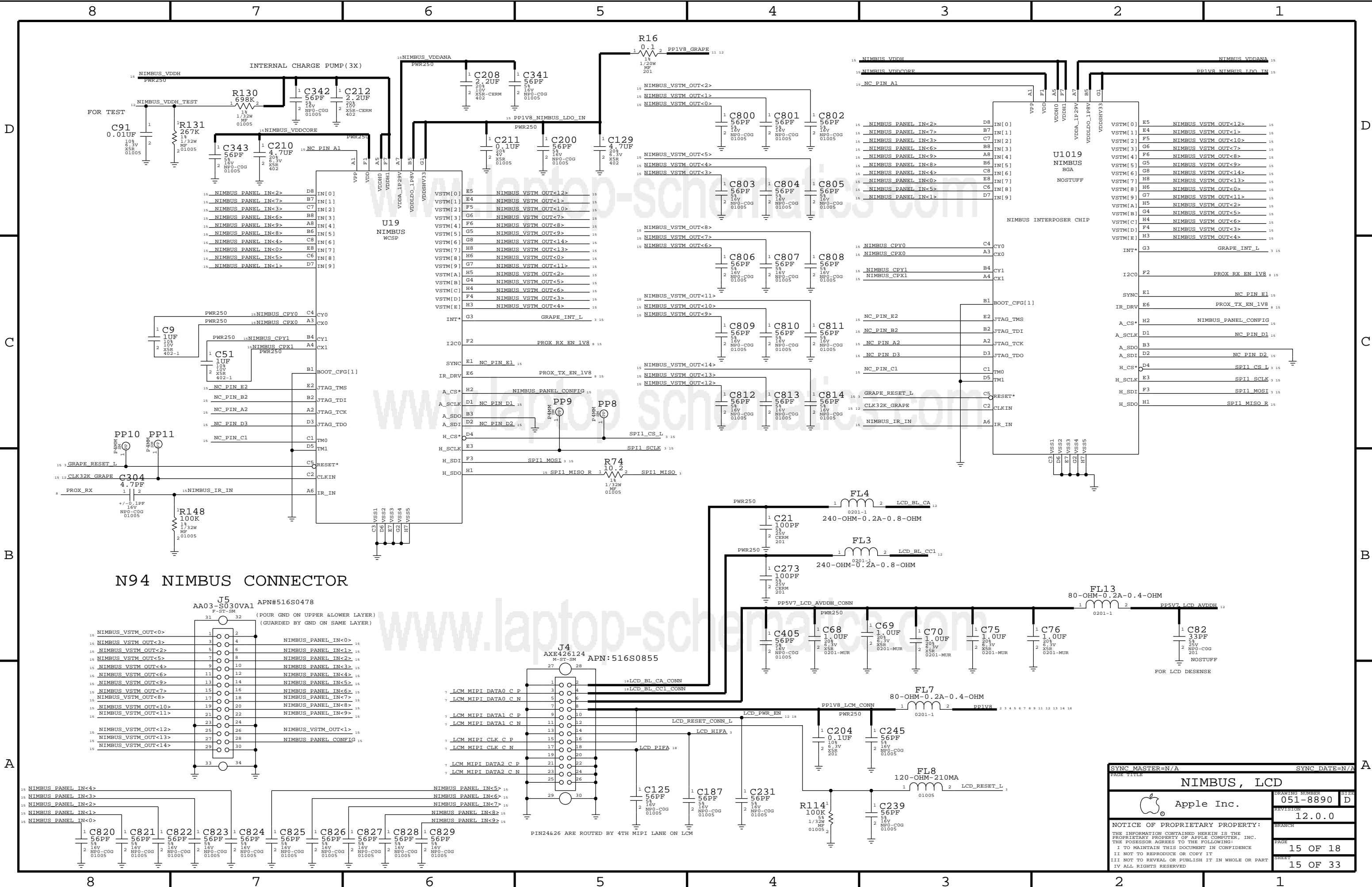


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<b>ACCEL, GYRO, COMPASS, SPK AMP</b>					
		DRAWING NUMBER	051-8890	SIZE	D
		REVISION	12.0.0		
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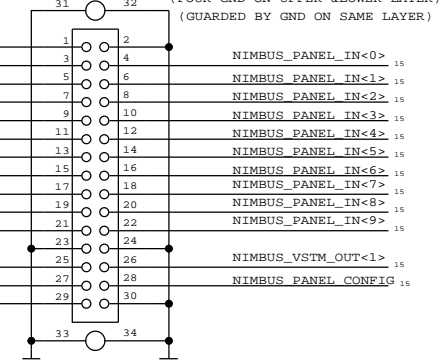
DOCK CONNECTOR

SYNC MASTER=N/A		SYNC DATE=N/A	
<b>DOCKCONNECTOR, SPK AMP</b>			
Apple Inc.		DRAWING NUMBER	051-8890
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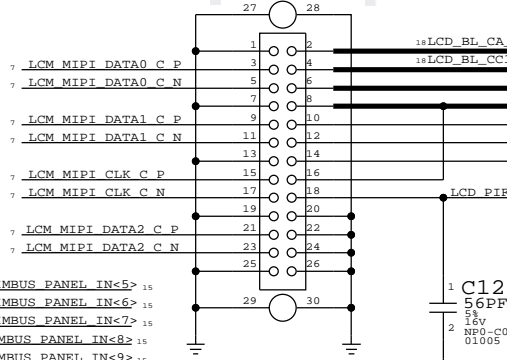


**N94 NIMBUS CONNECTOR**

J5 AA03-S030VA1 APN#516S0478 (POUR GND ON UPPER & LOWER LAYER) (GUARDED BY GND ON SAME LAYER)

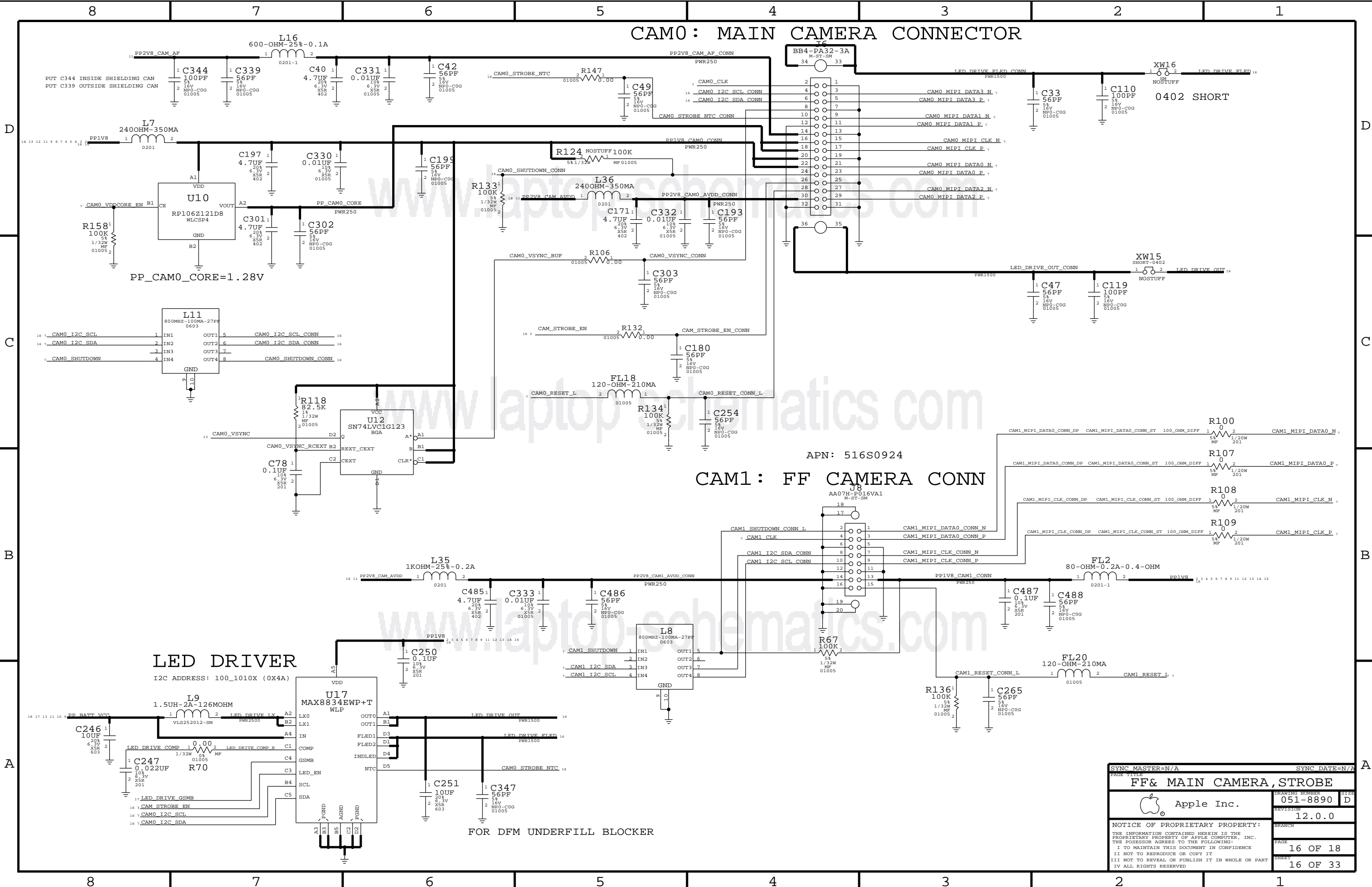


J4 AXE426124 APN:516S0855



PAGE TITLE		SYNC DATE=N/A	
<b>NIMBUS, LCD</b>			
Apple Inc.		DRAWING NUMBER	SIZE
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# CAMO: MAIN CAMERA CONNECTOR



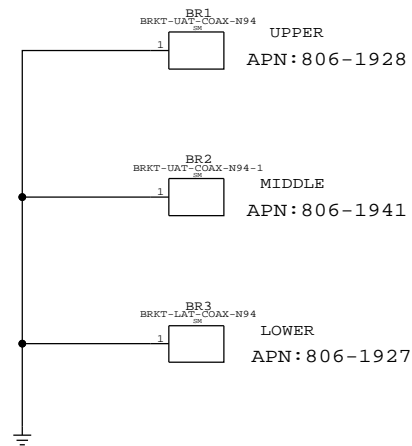
APN: 516S0924  
CAM1: FF CAMERA CONN

LED DRIVER  
I2C ADDRESS: 100\_1010X (0X4A)

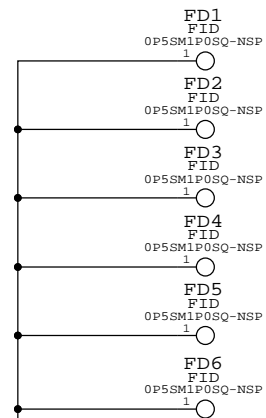
FOR DFM UNDERFILL BLOCKER

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FF& MAIN CAMERA, STROBE			
DRAWING NUMBER		SIZE	
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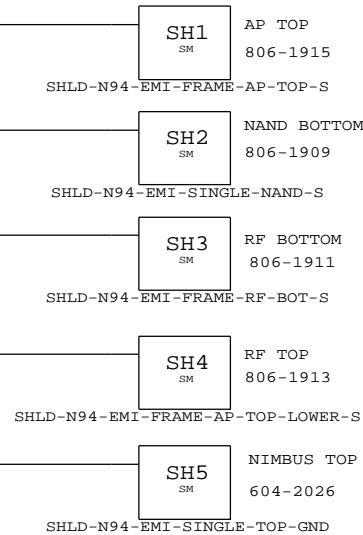
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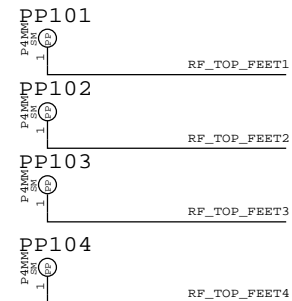
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### SHIELDS

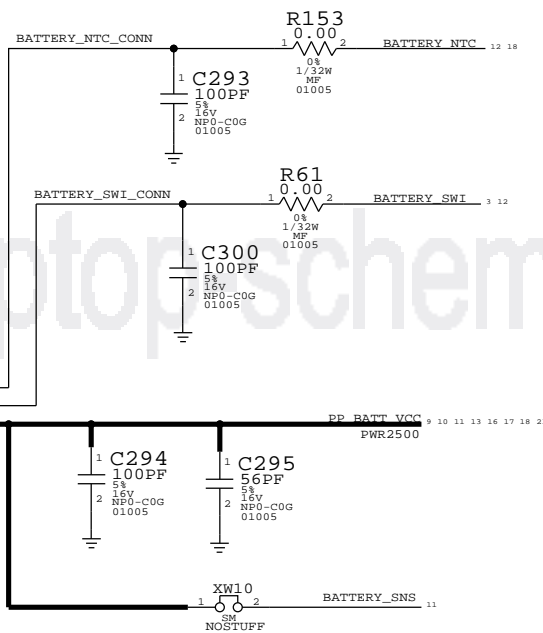


FOR RF TOP SHIELDING FEET  
WILL CONNECT TO GND VIA SHIELD

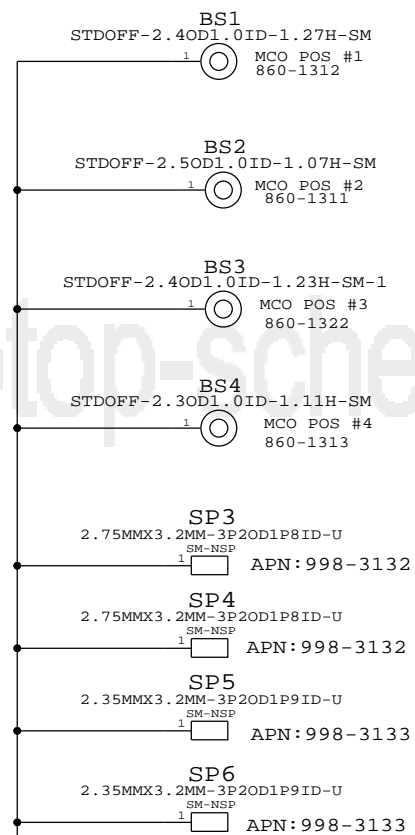


APN: 516S0908

J9  
1.8PITCH  
F-ST-SM



### STANDOFFS

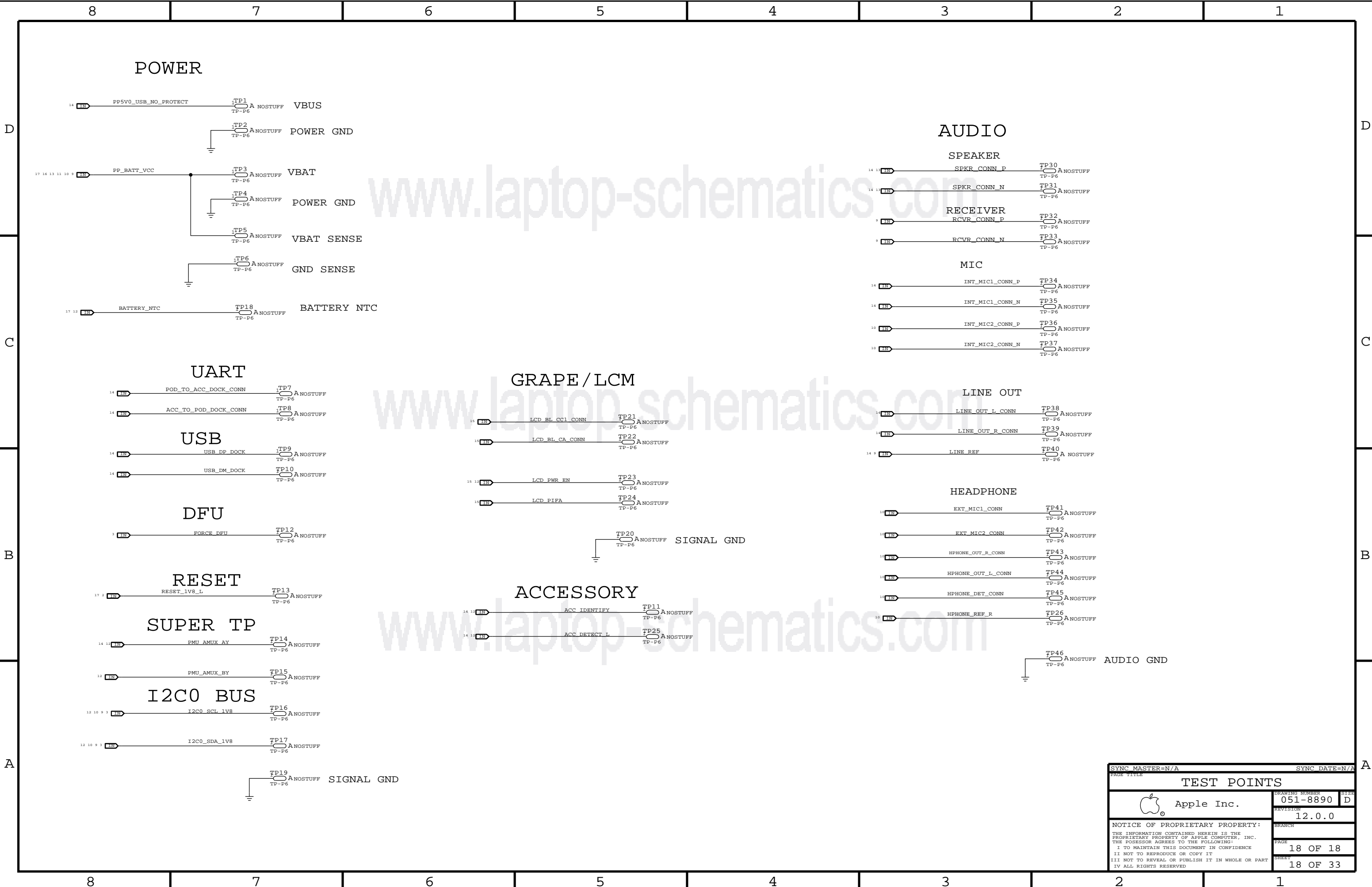


### AP/RADIO INTERFACE

SUBDESIGN\_SUFFIX=RF  
I550

23	18	17	16	13	11	9	PP_BATT_VCC	MAKE_BASE=TRUE	BATT_VCC
23	3	RADIO_ON_L	MAKE_BASE=TRUE	RADIO_ON_N					
20	3	BB_RESET_DET_L	MAKE_BASE=TRUE	RESET_DET_N					
23	12	BB_PMU_FFT_ON	MAKE_BASE=TRUE	FFT_ON	(ANGELINA)				
23	3	RESET_BB_PMU_L	MAKE_BASE=TRUE	RESET_PMU_N	(AP - H4P)				
20	3	BB_RESET_L	MAKE_BASE=TRUE	BB_RST_N					
20	12	BB_WAKE_AP	MAKE_BASE=TRUE	BB_WAKE_AP					
25	18	RESET_IV8_L	MAKE_BASE=TRUE	RF_RESET_N					
20	16	LED_DRIVE_GSMB	MAKE_BASE=TRUE	GSM_TXBURST_IND					
20	3	SPI2_MRDY	MAKE_BASE=TRUE	IPC_MRDY					
20	3	IPC_SRDY	MAKE_BASE=TRUE	IPC_SRDY					
20	3	IPC_GPIO4	MAKE_BASE=TRUE	IPC_GPIO4					
20	12	BB_VBUS_DET	MAKE_BASE=TRUE	BB_USB_VBUS					
20	8	BB_USB_N	MAKE_BASE=TRUE	BB_USB_DN					
20	8	BB_USB_P	MAKE_BASE=TRUE	BB_USB_DP					
20	3	UART1_RTS_L	MAKE_BASE=TRUE	BB_UART_CTS_N	RADIO_MLB_V3				
20	3	UART1_CTS_L	MAKE_BASE=TRUE	BB_UART_RTS_N					
20	3	UART1_TXD	MAKE_BASE=TRUE	BB_UART_RXD					
20	3	UART1_RXD	MAKE_BASE=TRUE	BB_UART_TXD					
20	3	I2S1_BCLK	MAKE_BASE=TRUE	BB_I2S_CLK					
20	3	I2S1_DOUT	MAKE_BASE=TRUE	BB_I2S_RXD					
20	3	I2S1_DIN	MAKE_BASE=TRUE	BB_I2S_TXD					
20	3	I2S1_LRCLK	MAKE_BASE=TRUE	BB_I2S_WS					
32	11	10	9	4	3	PP1V8_SDRAM	MAKE_BASE=TRUE	WL_BT_VDDIO	
32	12	BT_REG_ON	MAKE_BASE=TRUE	BT_REG_ON					
32	12	WIFI_REG_ON	MAKE_BASE=TRUE	WLAN_REG_ON					
32	12	WLAN_SDIO_CLK	MAKE_BASE=TRUE	WLAN_SDIO_CLK					
32	12	WLAN_SDIO_CMD	MAKE_BASE=TRUE	WLAN_SDIO_CMD					
32	12	WLAN_SDIO_DATA<3..0>	MAKE_BASE=TRUE	WLAN_SDIO_DATA<3..0>					
32	12	WLAN_WAKE_AP	MAKE_BASE=TRUE	HOST_WAKE_WLAN					
32	3	BT_WAKE	MAKE_BASE=TRUE	BT_WAKE					
32	12	CLK32K_WIFI	MAKE_BASE=TRUE	CLK32K_AP					
32	3	BT_RESET_L	MAKE_BASE=TRUE	BT_RESET_N					
32	12	BT_WAKE_AP	MAKE_BASE=TRUE	HOST_WAKE_BT					
32	3	UART3_RTS_L	MAKE_BASE=TRUE	BT_UART_CTS_N					
32	3	UART3_CTS_L	MAKE_BASE=TRUE	BT_UART_RTS_N					
32	3	UART3_TXD	MAKE_BASE=TRUE	BT_UART_RXD					
32	3	UART3_RXD	MAKE_BASE=TRUE	BT_UART_TXD					
32	9	I2S2_BCLK	MAKE_BASE=TRUE	BT_PCM_CLK					
32	9	I2S2_DOUT	MAKE_BASE=TRUE	BT_PCM_IN					
32	9	I2S2_DIN	MAKE_BASE=TRUE	BT_PCM_OUT					
32	9	I2S2_LRCLK	MAKE_BASE=TRUE	BT_PCM_SYNC					
20	7	HSIC1_DATA	50_OHM HSIC_ST	MAKE_BASE=TRUE	HSIC_BB_DATA				
20	7	HSIC1_STB	50_OHM HSIC_ST	MAKE_BASE=TRUE	HSIC_BB_STROBE				
20	3	HOST_BB_HSIC_RDY	MAKE_BASE=TRUE	HOST_BB_HSIC_RDY					
20	3	HOST_WLAN_HSIC_RDY	MAKE_BASE=TRUE	HOST_WLAN_HSIC_RDY					
20	3	BB_HSIC_RDY	MAKE_BASE=TRUE	BB_HSIC_RDY					
32	2	HSIC2_DATA	50_OHM HSIC_ST	MAKE_BASE=TRUE	HSIC_WLAN_DATA				
32	2	HSIC2_STB	50_OHM HSIC_ST	MAKE_BASE=TRUE	HSIC_WLAN_STROBE				
20	3	BB_EMERGENCY_DWLD_L	MAKE_BASE=TRUE	BB_EMERGENCY_DWLD					
32	2	WLAN_HSIC_RDY	MAKE_BASE=TRUE	WLAN_HSIC_RDY					

SYNC MASTER=N/A		SYNC DATE=N/A	
RF INT, SHIELD, STNDOFFS			
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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.  
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.  
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

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REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
12	0001170763	ENGINEERING RELEASED		2011-07-05

# N94 RADIO\_MLB\_V3 SUBDESIGN

## RADIO - 07/05/2011: SUBDESIGN

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02	BASEBAND
03	BASEBAND MEMORY
04	BASEBAND POWER
05	POWER1: CONTROL
06	POWER2: DIGITAL, ANALOG, RF
07	AP INTERFACE AND DEBUG CONNECTOR
08	RF TRANSCEIVER - RX AND TX
09	RF TRANSCEIVER - POWER DECOUPLING
10	RF TRANSCEIVER AND ASM
11	MMPA AND PA DC/DC CONVERTER
12	B2 AND B5 PADS
13	DIVERSITY AND EXTERNAL GPS LNA
14	WLAN/BT/FM
15	DIVERSITY ANTENNA SWITCH AND SIM

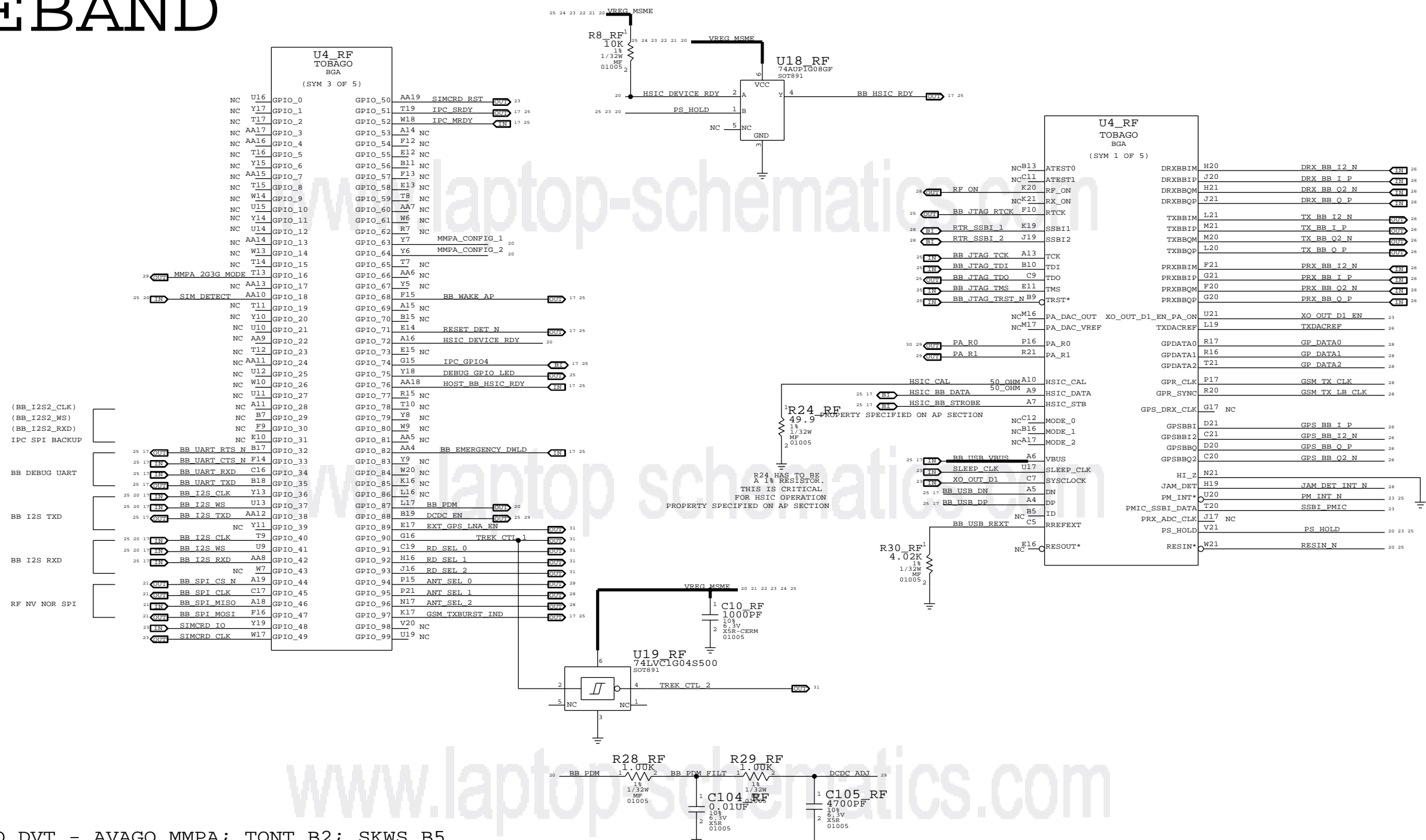
SCH #: 951-1604

BASED ON RADIO\_MLB\_EVT2\_RFPE

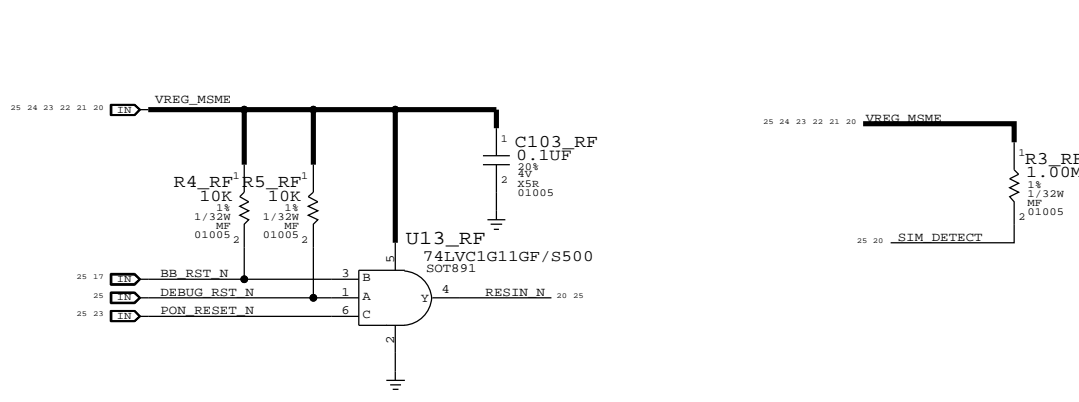
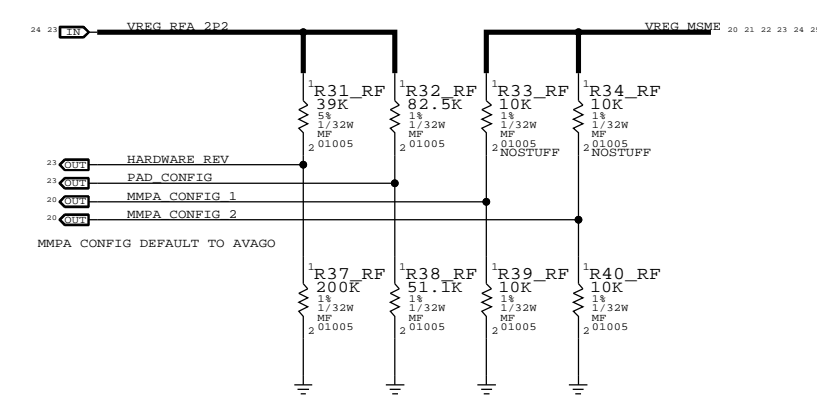
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# BASEBAND

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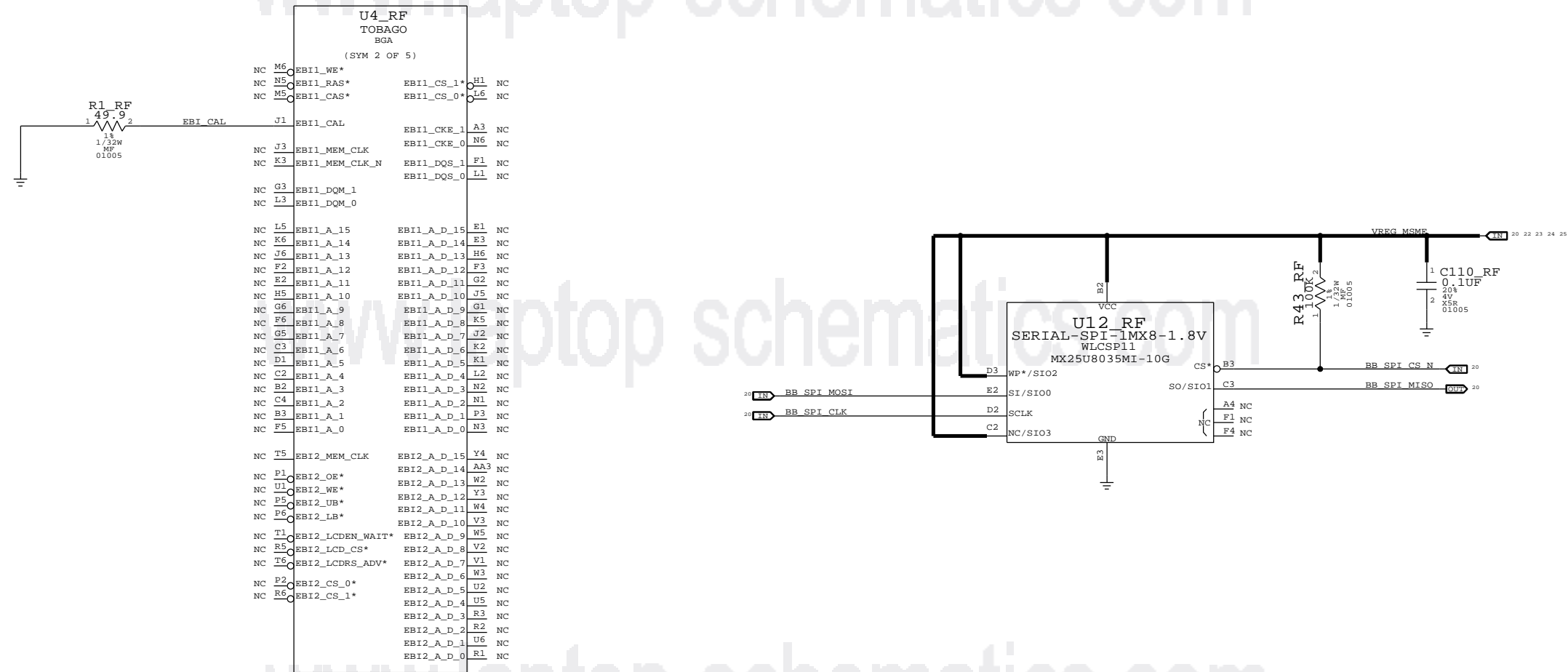
DEFAULT TO DVT - AVAGO MMPA; TQNT B2; SKWS B5



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BRANCH					
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**BASEBAND**  
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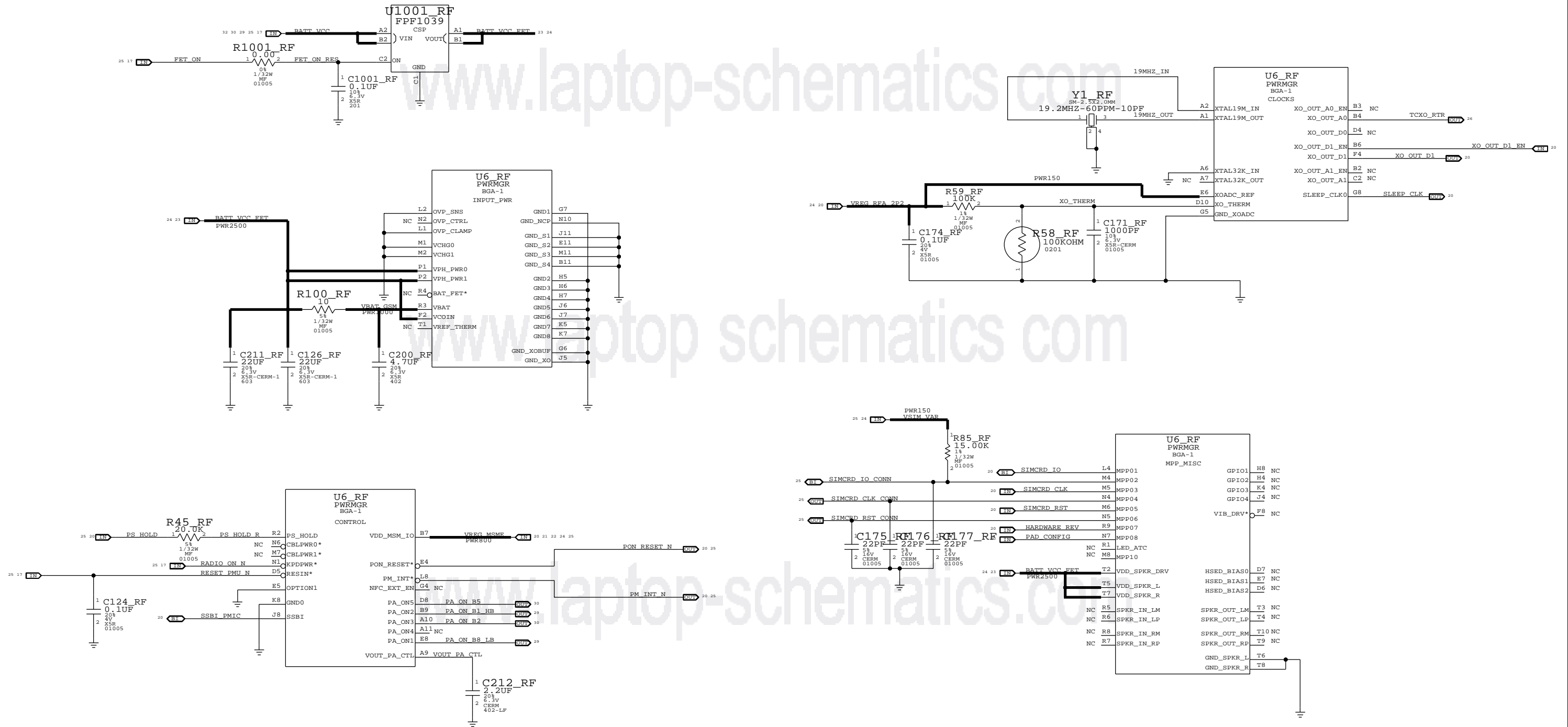
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# BASEBAND PMU

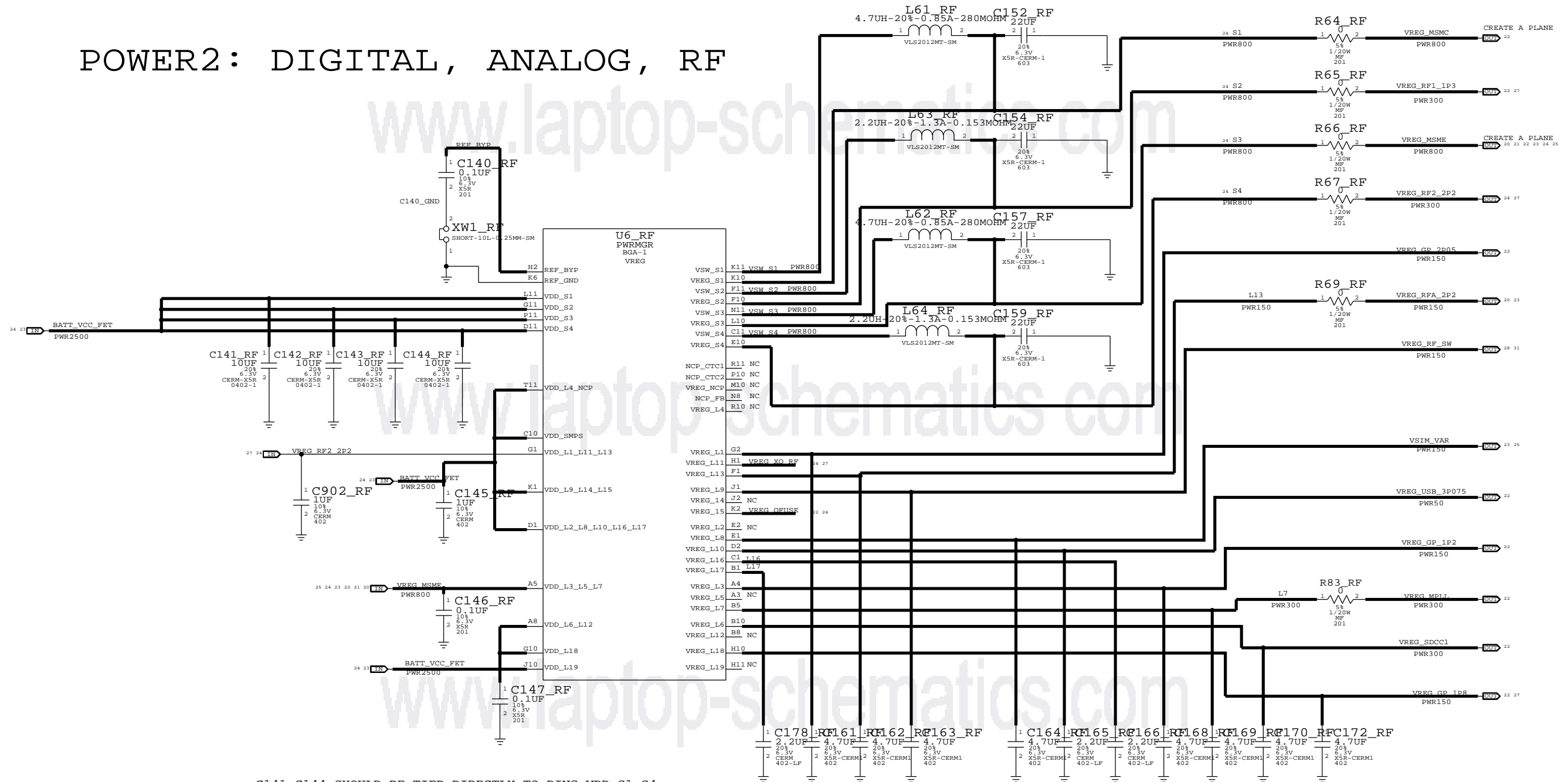
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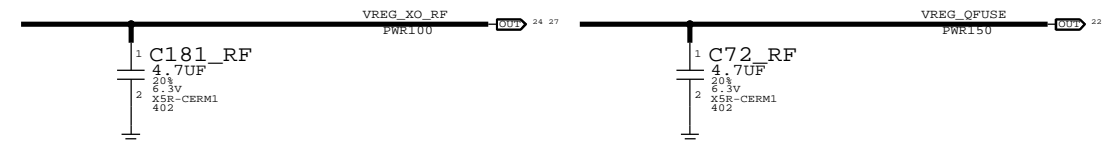
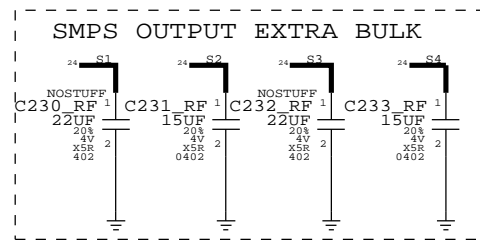
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## POWER2: DIGITAL, ANALOG, RF



C141-C144 SHOULD BE TIED DIRECTLY TO PINS VDD\_S1-S4

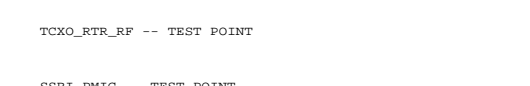
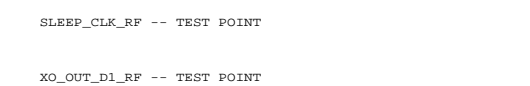
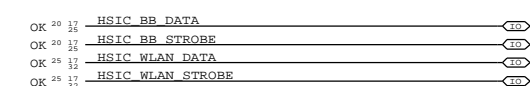
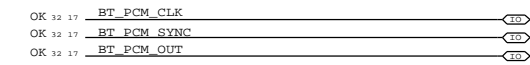
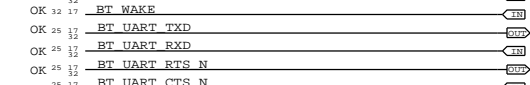
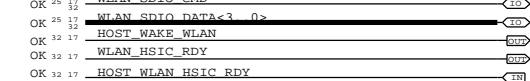
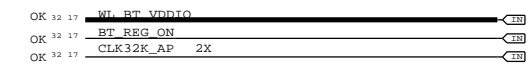
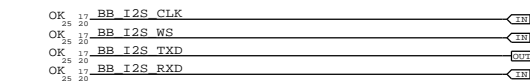
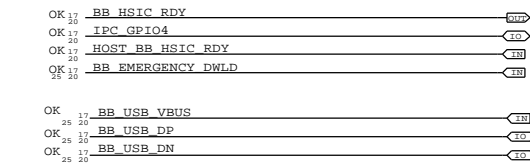
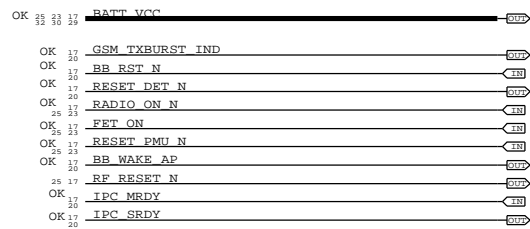
L16 AND L17 DECOUPLED PER EUREKA'S RECOMMENDATION



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# DEBUG CONNECTOR

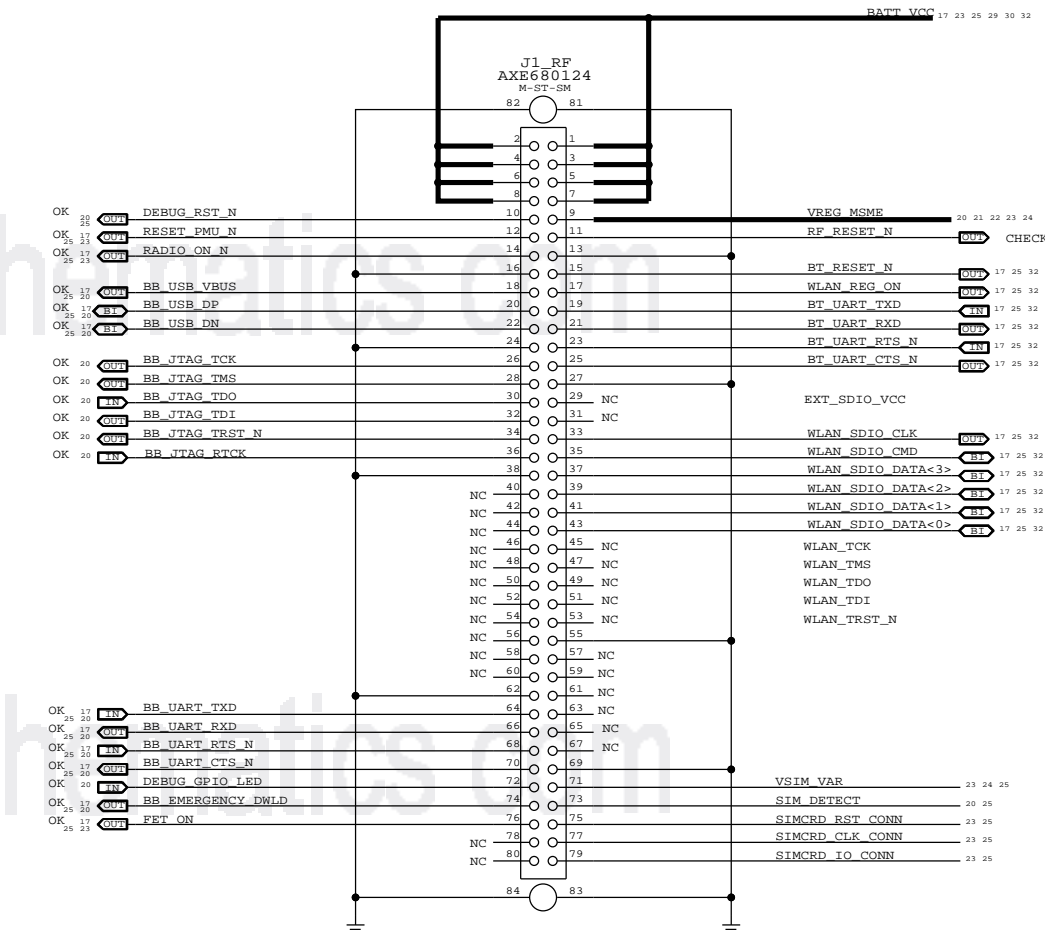
## AP CONNECTIONS



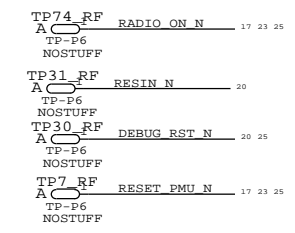
## WLAN

## DIGITAL AUDIO

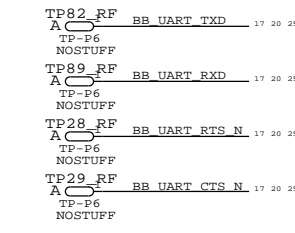
## POWER DOMAINS



## CONTROL

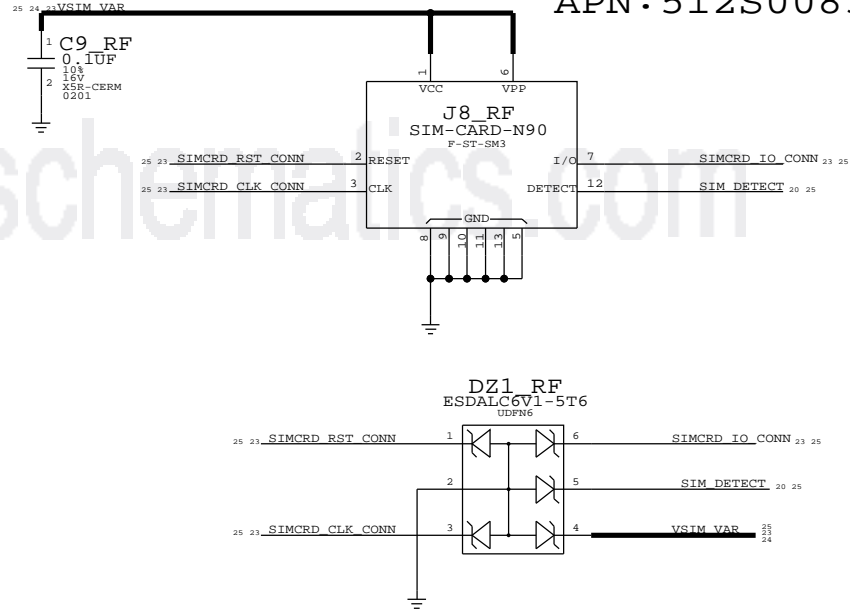


## UART



## SIM CARD CONNECTOR

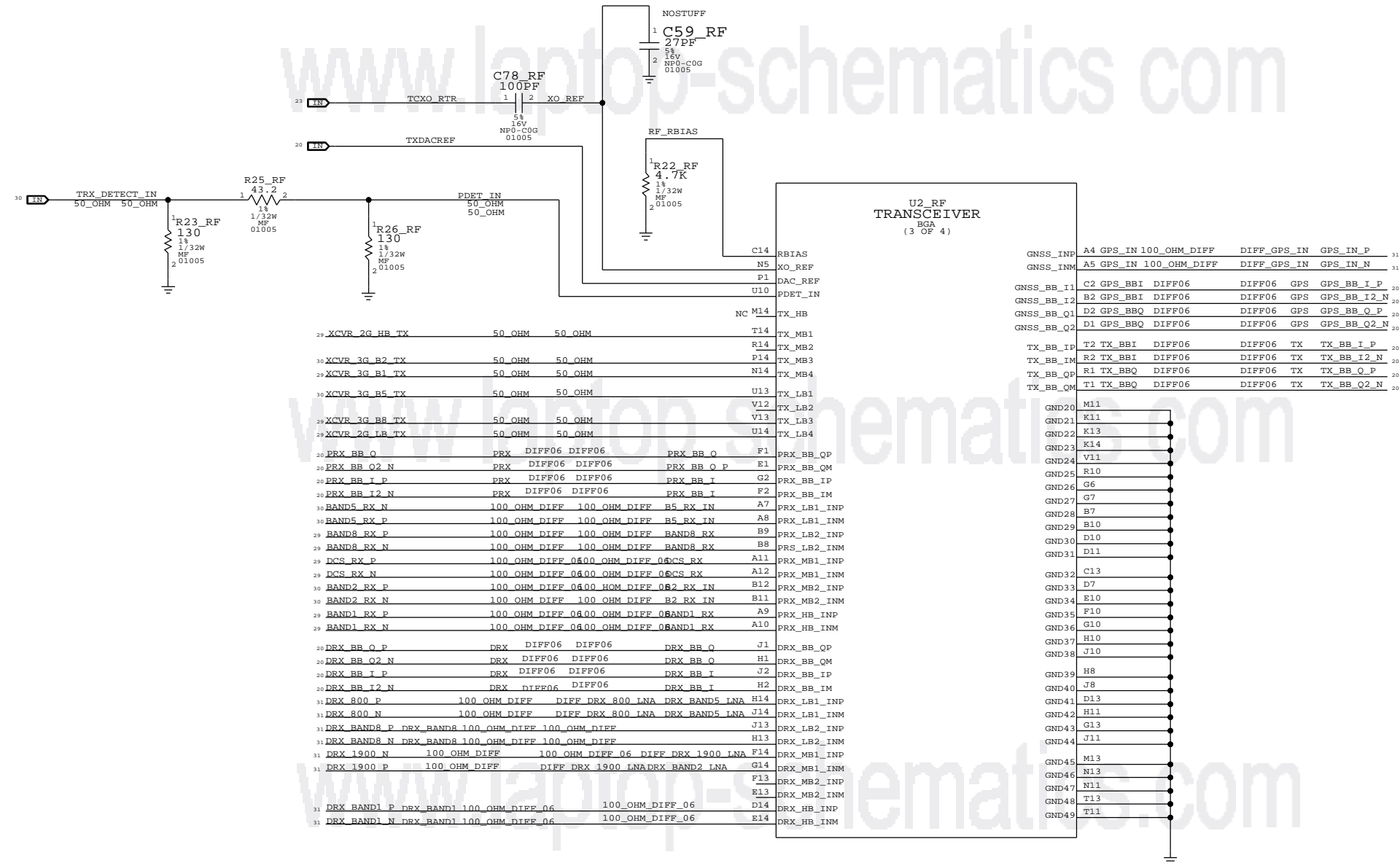
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# RF TRANSCEIVER

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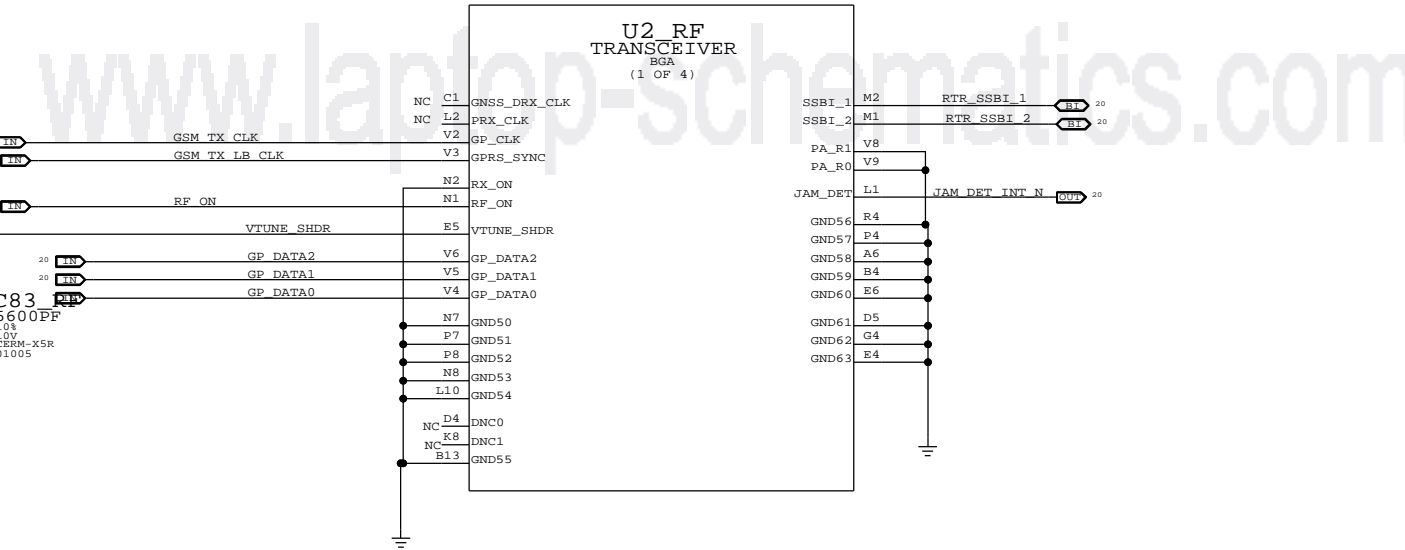
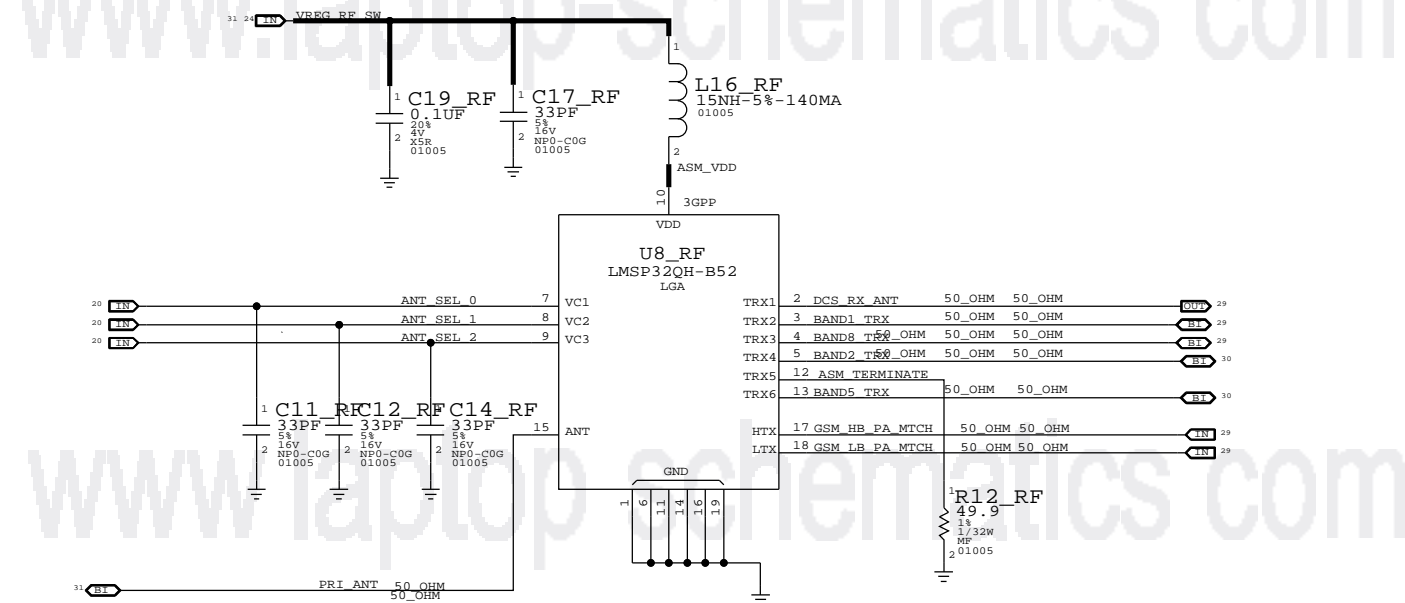


RF RX/TX INTERFACE	
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# RF TRANSCEIVER AND ASM

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# MMPA, DC/DC CONVERTER & FILTER BANK

D

C

B

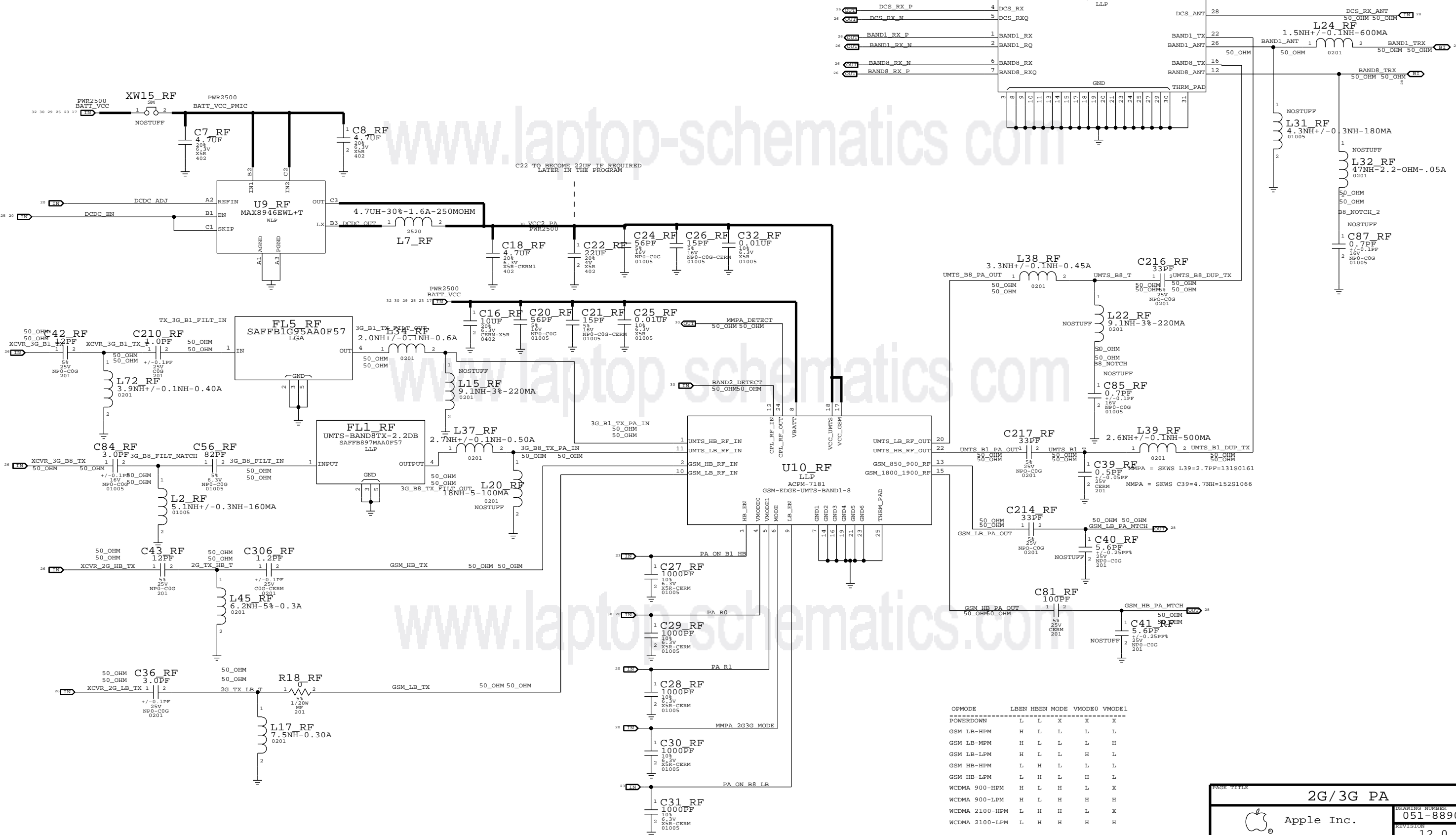
A

D

C

B

A



OPMODE	LBEN	HBEN	MODE	VMODE0	VMODE1
POWERDOWN	L	L	X	X	X
GSM LB-HPM	H	L	L	L	L
GSM LB-MPM	H	L	L	L	H
GSM LB-LPM	H	L	L	H	L
GSM HB-HPM	L	H	L	L	L
GSM HB-LPM	L	H	L	H	L
WCDMA 900-HPM	H	L	H	L	X
WCDMA 900-LPM	H	L	H	H	H
WCDMA 2100-HPM	L	H	H	L	X
WCDMA 2100-LPM	L	H	H	H	H

2G/3G PA

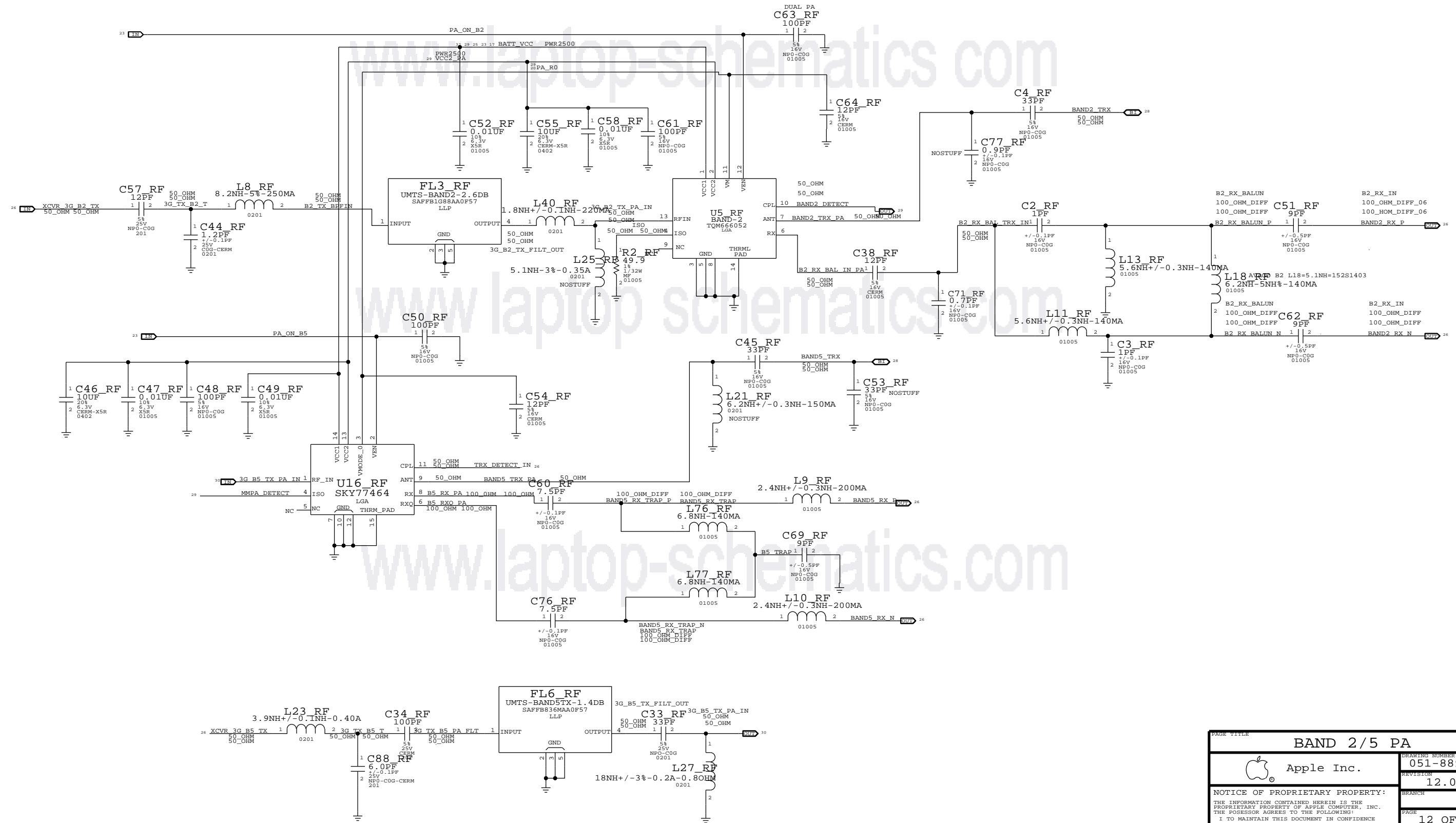
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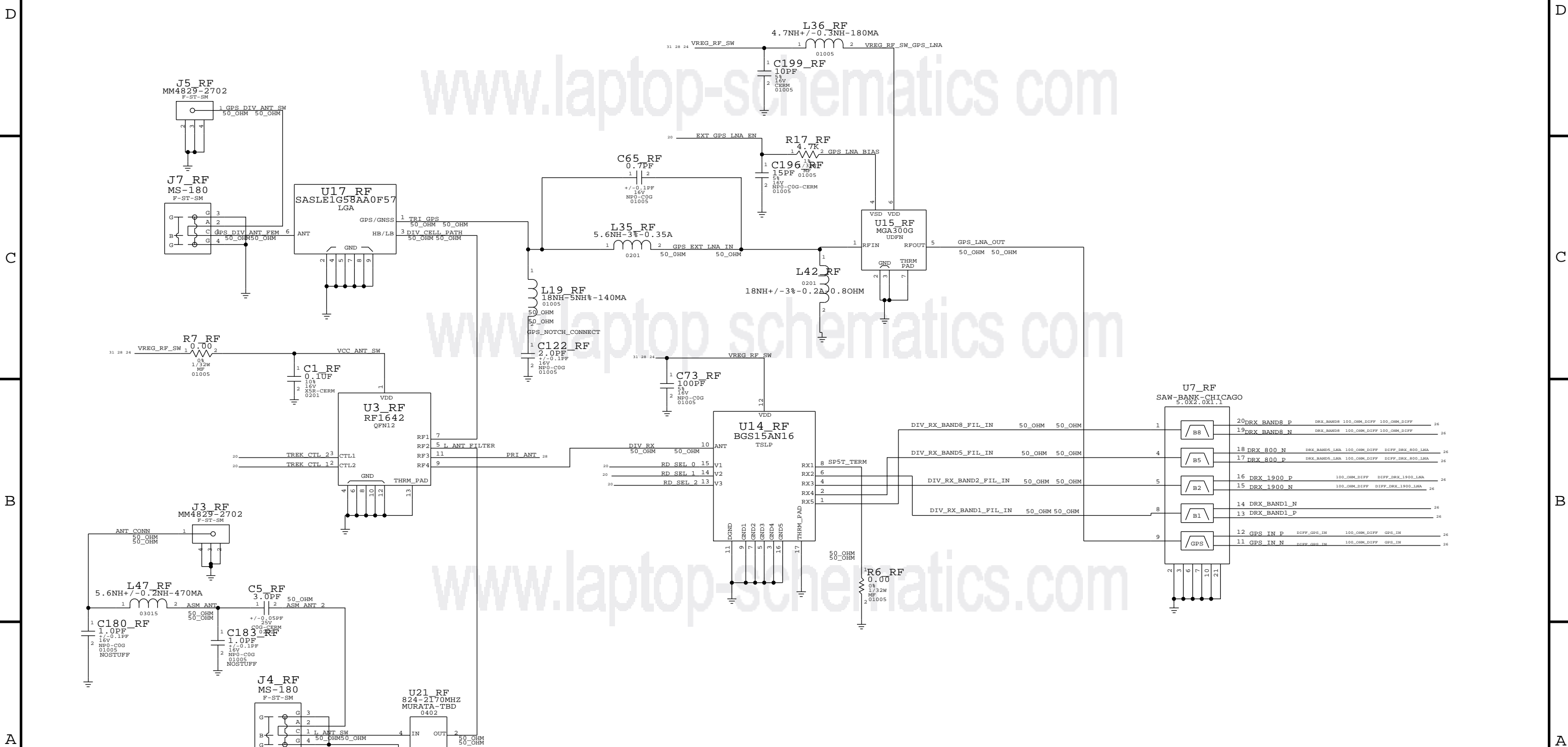
# BAND 2 AND BAND 5 PAD



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		SHEET	30 OF 33

# DIVERSITY AND EXTERNAL GPS LNA

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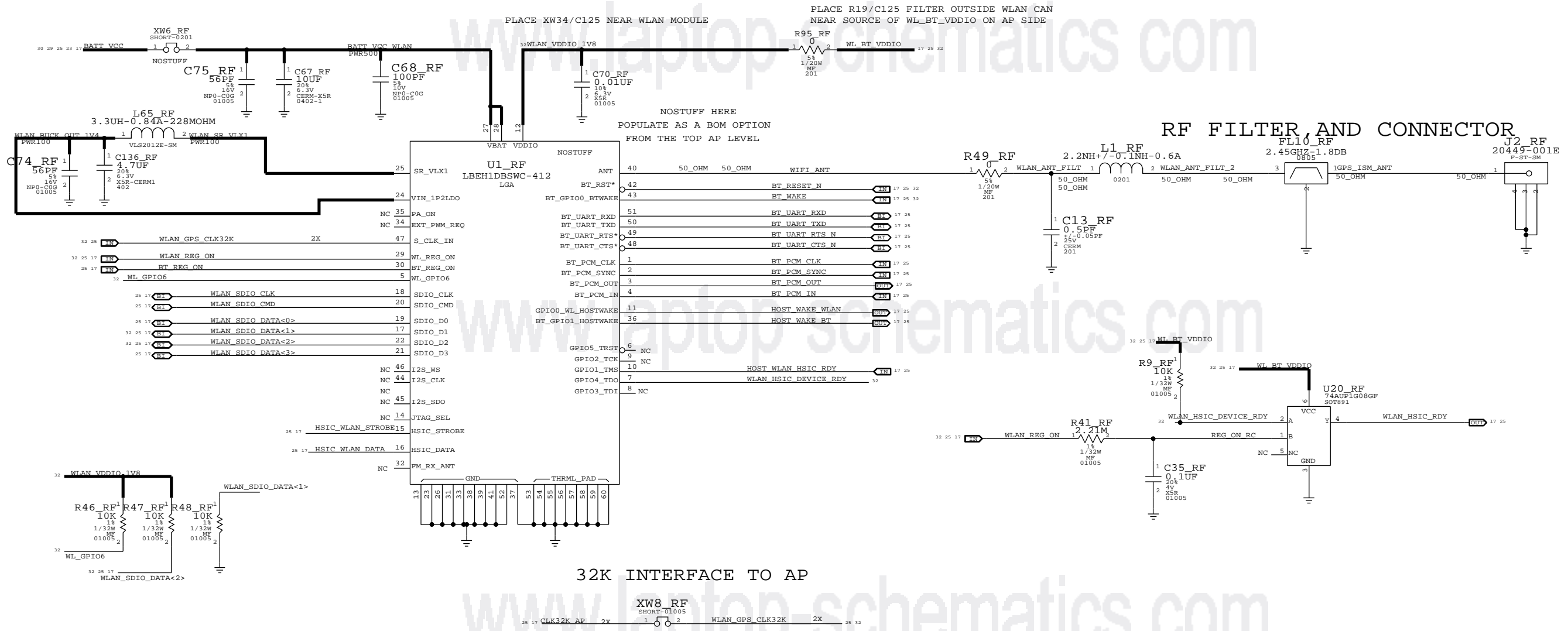


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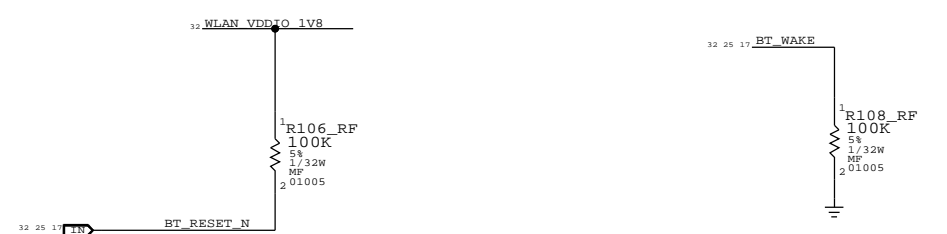
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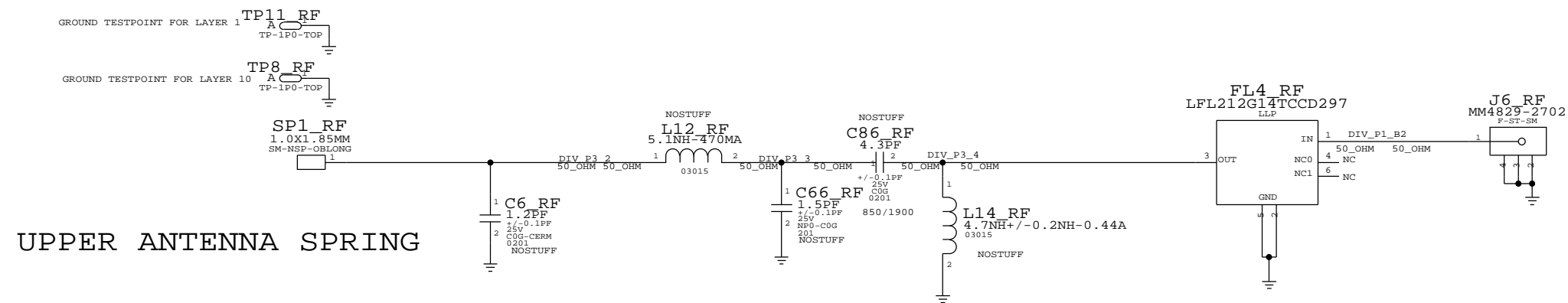
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