


1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.  
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.  
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
C	0001188998	PRODUCTION RELEASED		2011-07-22

# J59

(7/22/2011)

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41	90	Tethered Cable Connector	T29 D	03/17/2011
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DRAWING TITLE		SCH, J59, MLB	
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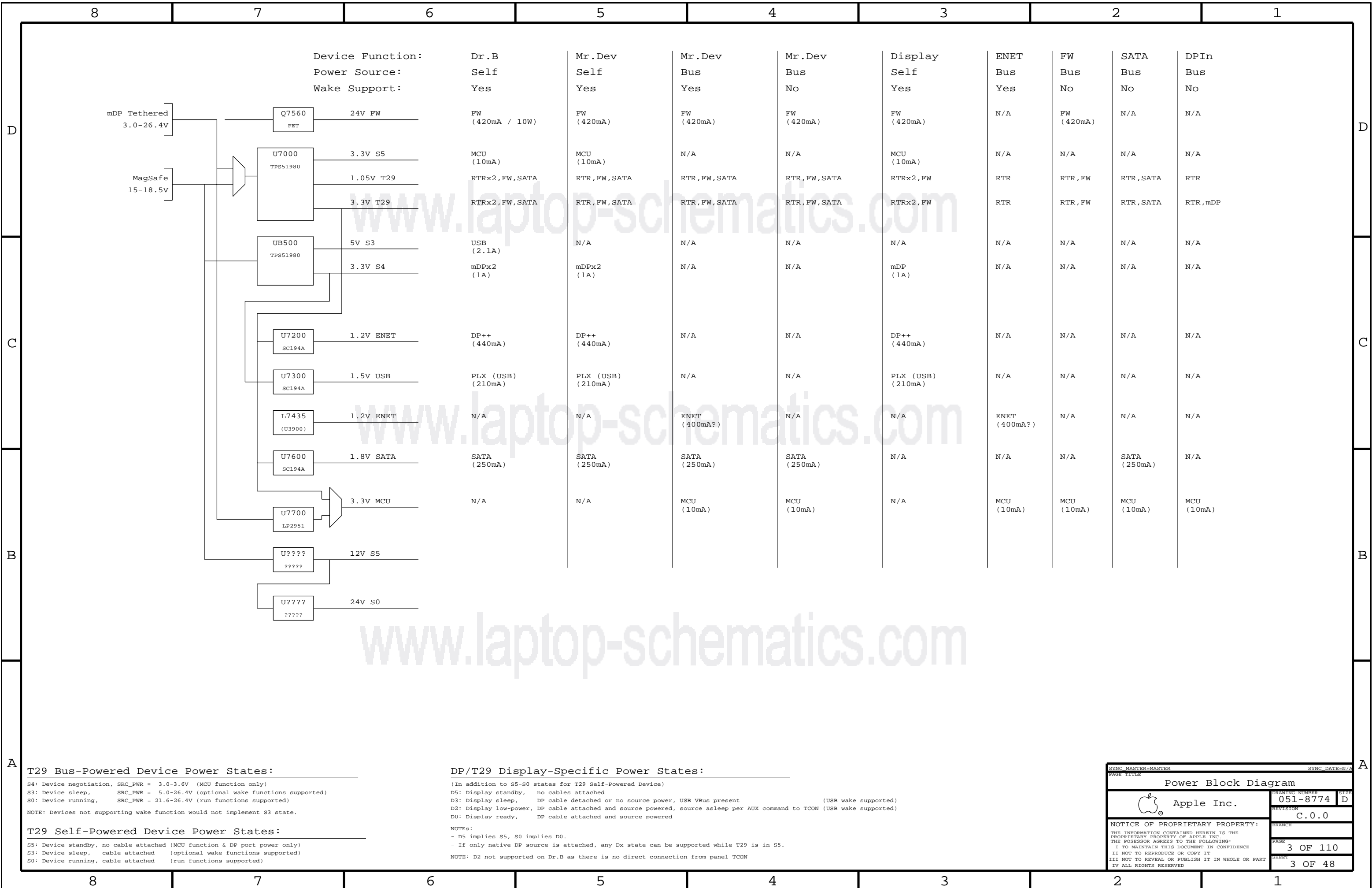
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J59 BLOCK DIAGRAM			
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**T29 Bus-Powered Device Power States:**  
 S4: Device negotiation, SRC\_PWR = 3.0-3.6V (MCU function only)  
 S3: Device sleep, SRC\_PWR = 5.0-26.4V (optional wake functions supported)  
 S0: Device running, SRC\_PWR = 21.6-26.4V (run functions supported)  
 NOTE: Devices not supporting wake function would not implement S3 state.

**T29 Self-Powered Device Power States:**  
 S5: Device standby, no cable attached (MCU function & DP port power only)  
 S3: Device sleep, cable attached (optional wake functions supported)  
 S0: Device running, cable attached (run functions supported)

**DP/T29 Display-Specific Power States:**  
 (In addition to S5-S0 states for T29 Self-Powered Device)  
 D5: Display standby, no cables attached  
 D3: Display sleep, DP cable detached or no source power, USB VBUS present (USB wake supported)  
 D2: Display low-power, DP cable attached and source powered, source asleep per AUX command to TCON (USB wake supported)  
 D0: Display ready, DP cable attached and source powered

NOTES:  
 - D5 implies S5, S0 implies D0.  
 - If only native DP source is attached, any Dx state can be supported while T29 is in S5.

NOTE: D2 not supported on Dr.B as there is no direct connection from panel TCON

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<b>Power Block Diagram</b>			
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BOM NUMBER	BOM NAME	BOM OPTIONS
639-1575	PCBA,MLB,J59	BASIC
085-2422	PCBA,MLB,DEV,J59	DEVELOPMENT

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE,T29HV:P12V,BIT_BANG_I2C,ENET_WAKE:PCIE,PIUSB_REV:B,PRODUCTION

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0945	1	IC,T29-PRQ,220 FCBGA,15X15MM	U3600	CRITICAL	
338S0753	1	IC FW43 E 1394B PHY/ONCI LINK/PCI R 12	U4100	CRITICAL	
343S0549	1	IC ASIC CRIT ENET QFN 48 6X6 SCHT7761 80	U3900	CRITICAL	
338S0977	1	PCI EXPRESS TO USB 2.0 HOST CONTROLLER(REV B)	U4600	CRITICAL	

FLASH	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
RAW: 335S0550	341T0376	1	IC EEPROM J59 PRIMARY SPI 32KBIT MLPS	U3690	CRITICAL	
RAW: 335S0800	341T0331	1	ENET FLASH C IV NO SD J59	U3990	CRITICAL	
RAW: 335S0559	341T0375	1	IC EEPROM FW43 E2 GUID I2C 2KBIT MLPS	U4290	CRITICAL	
RAW: 337S4115	341T0385	1	IC MCU 32B LPC1114 32KB/8KB HVQFN33 J59	U5000	CRITICAL	
RAW: 337S4115	341T0385	1	IC PROGRAM LPC1114 T29 SUPER MCU HVQFN33	U9330	CRITICAL	
RAW: 337S3558	341T0378	1	IC PROGRAM LPC2144 J59 SYSTEM MCU	U2617	CRITICAL	
RAW: 353S2320	341T0369	1	IC PROGRAM PRK0261 AUDIO/HD TPGDAB	U1400	CRITICAL	

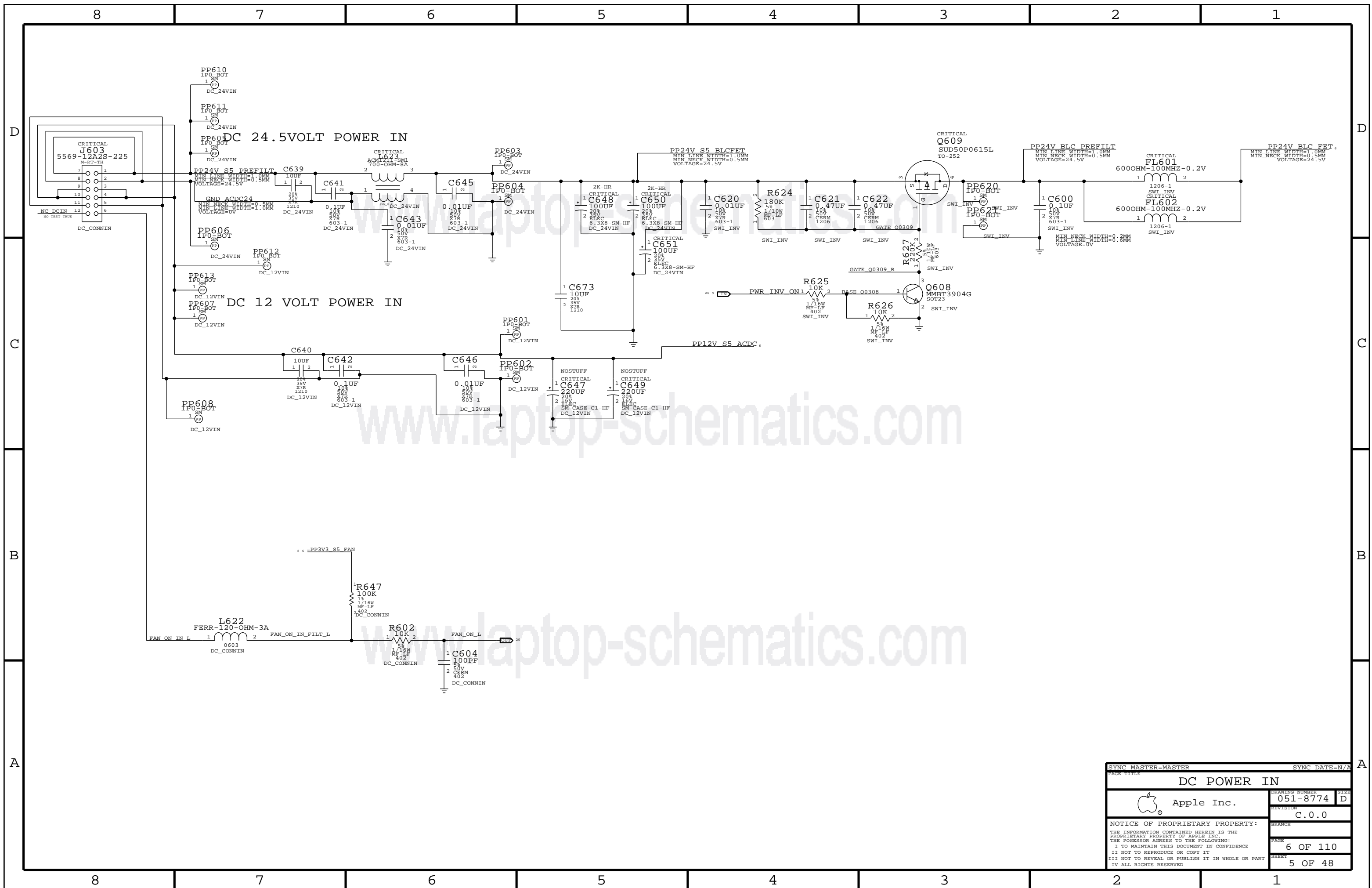
ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0977	376S0859		ALL	DIODESINC ALT FET
376S0972	376S0612		ALL	ROHM ALT FET
377S0107	377S0066		ALL	ON SEMI ALT RCLAMP
155S0431	155S0289		L1204	ALTERNATE CM CHOKE
376S1029	376S0953		ALL	ALTERNATE DC/DC FET
376S1030	376S0801		ALL	ALTERNATE DC/DC FET
376S1017	376S0612		ALL	ALTERNATE TOSH SS FET
377S0124	377S0057		ALL	ALTERNATE VARISTOR
152S1483	152S1376		ALL	ALTERNATE INDUCTOR
155S0691	155S0183		ALL	ALT BEAD FOR BL FILT
128S0262	128S0220		ALL	ADDS KEMET TO SANYO
138S0684	138S0660		ALL	ADDS MURATA TO TAIYO
155S0571	155S0309		ALL	ALTERNATE FERRITE
353S3477	353S3207		ALL	ALTERNATE FAB U9410

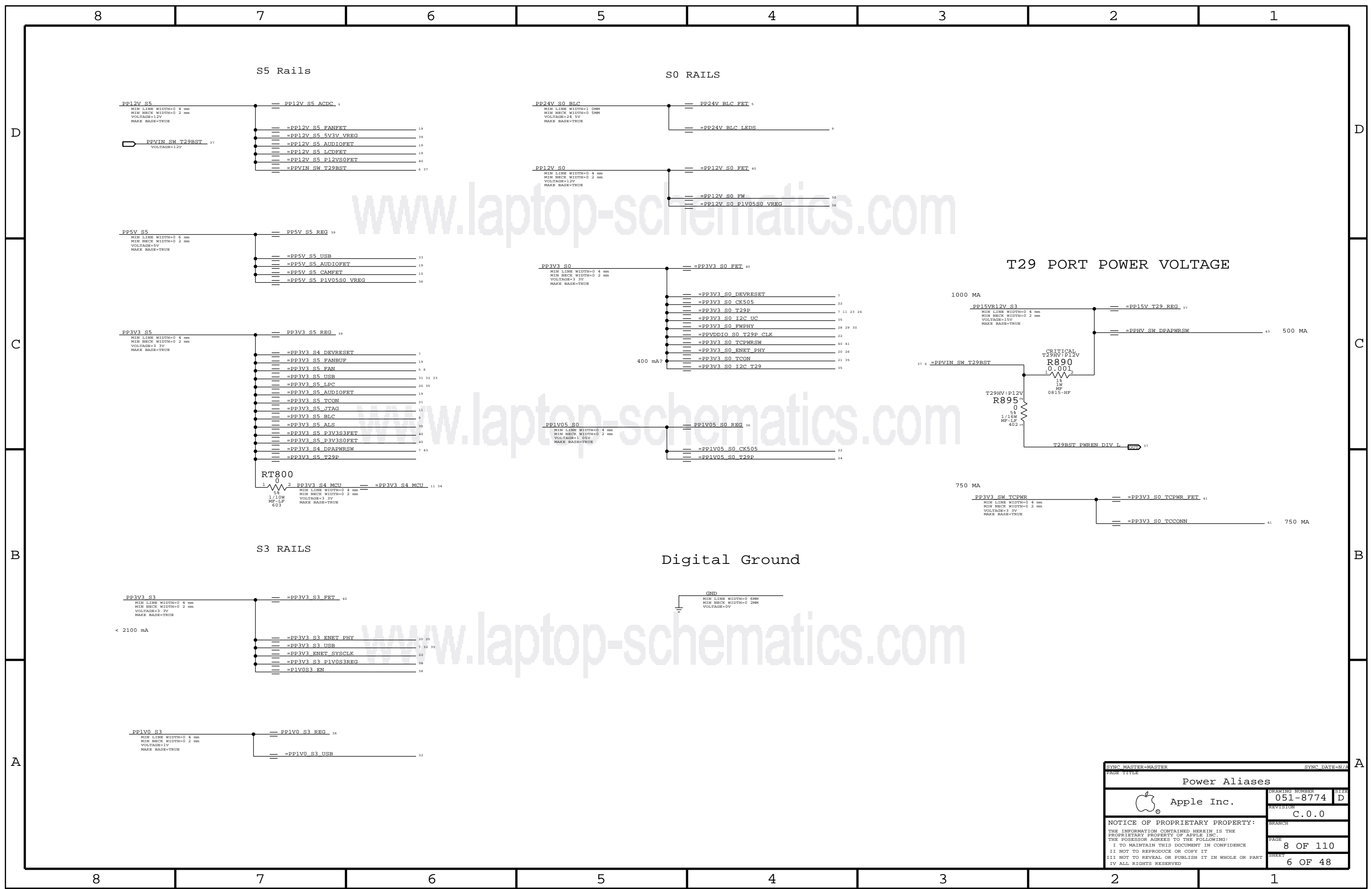
Schematic / PCB / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
820-2997	1	PCBF MLB J59	PCB1	CRITICAL	
051-8774	1	SCH MLB J59	SCH1	CRITICAL	
825-7122	1	MLB LABEL 48 OMM X 4 8MM	[EEEE_DHMY]	CRITICAL	

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BOM Configuration & Misc			
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<b>DC POWER IN</b>			
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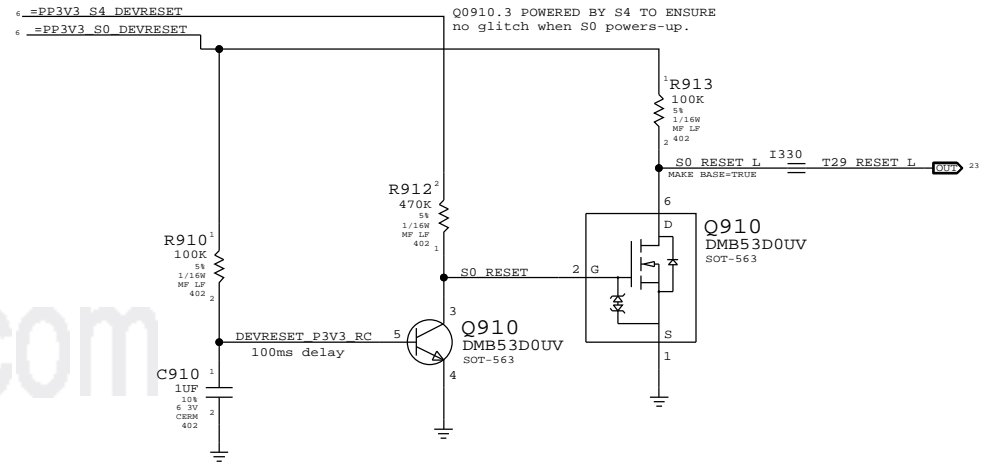
PCIe Assignments

PCIE T29 R2D C P<0>	==	PCIE USB R2D C P	32 46
PCIE T29 R2D C N<0>	==	PCIE USB R2D C N	32 46
PCIE T29 D2R P<0>	==	PCIE USB D2R P	32 46
PCIE T29 D2R N<0>	==	PCIE USB D2R N	32 46
T29 PCIE RESET L<0>	==	USB RESET L	32
PCIE T29 R2D C P<1>	==	PCIE ENET R2D C P	26 46
PCIE T29 R2D C N<1>	==	PCIE ENET R2D C N	26 46
PCIE T29 D2R P<1>	==	PCIE ENET D2R P	26 46
PCIE T29 D2R N<1>	==	PCIE ENET D2R N	26 46
T29 PCIE RESET L<1>	==	ENET RESET L	26
PCIE T29 R2D C P<2>	==	PCIE FW R2D C P	28 46
PCIE T29 R2D C N<2>	==	PCIE FW R2D C N	28 46
PCIE T29 D2R P<2>	==	PCIE FW D2R P	28 46
PCIE T29 D2R N<2>	==	PCIE FW D2R N	28 46
T29 PCIE RESET L<2>	==	FW RESET L	28
PCIE T29 R2D C P<3>	==	NC PCIE T29 R2D C P3	
PCIE T29 R2D C N<3>	==	NC PCIE T29 R2D C N3	
PCIE T29 D2R P<3>	==	NC PCIE T29 D2R P3	
PCIE T29 D2R N<3>	==	NC PCIE T29 D2R N3	
T29 PCIE RESET L<3>	==	NC T29 PCIE RESET L3	

INTERNAL DP PANEL SOURCE MUX BYPASS

DP T29SRCA ML C P<0>	==	DP INT ML C P<0>	7 44
DP T29SRCA ML C N<0>	==	DP INT ML C N<0>	7 44
DP T29SRCA ML C P<1>	==	DP INT ML C P<1>	7 44
DP T29SRCA ML C N<1>	==	DP INT ML C N<1>	7 44
DP T29SRCA ML C P<2>	==	DP INT ML C P<2>	7 44
DP T29SRCA ML C N<2>	==	DP INT ML C N<2>	7 44
DP T29SRCA ML C P<3>	==	DP INT ML C P<3>	7 44
DP T29SRCA ML C N<3>	==	DP INT ML C N<3>	7 44
DP T29SRCA AUXCH C P	==	DP INT AUXCH C P	7 44
DP T29SRCA AUXCH C N	==	DP INT AUXCH C N	7 44
DP T29SRCA HPD	==	DP INT HPD	21

Power-Up Reset Generation



MISC T29 ALIAS CONNECTIONS

T29 LSX R2P	==	T29 LSX R2P	34
T29 LSX P2R	==	T29 LSX P2R	34
TP T29 A BIAS	==	T29 A BIAS	42
PP3V3 S4 DPAPRSW	==	DPAPRSW EN	43
U5000 IS SLAVE MCU - U9330 IS MASTER (SEE REFERENCE DESIGN)	==	TCMCU ADDR	34

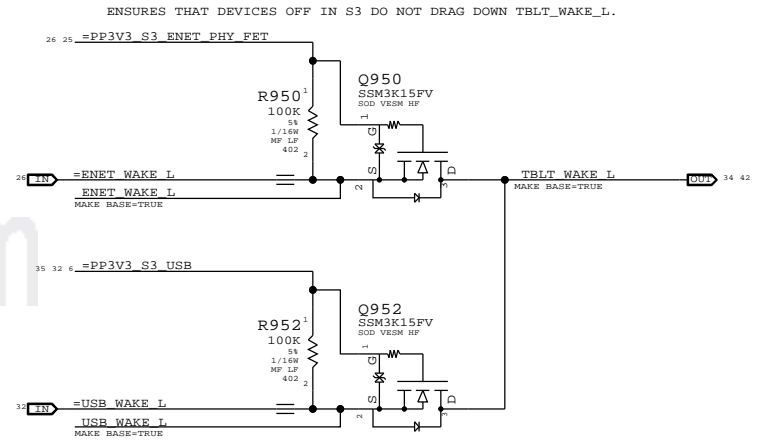
INTERNAL DP PANEL AC COUPLING CAPS

DP INT ML C P<0>	C900	DP INT ML P<0>	21 44 48
DP INT ML C N<0>	C901	DP INT ML N<0>	21 44 48
DP INT ML C P<1>	C902	DP INT ML P<1>	21 44 48
DP INT ML C N<1>	C903	DP INT ML N<1>	21 44 48
DP INT ML C P<2>	C904	DP INT ML P<2>	21 44 48
DP INT ML C N<2>	C905	DP INT ML N<2>	21 44 48
DP INT ML C P<3>	C906	DP INT ML P<3>	21 44 48
DP INT ML C N<3>	C907	DP INT ML N<3>	21 44 48
DP INT AUXCH C P	C908	DP INT AUXCH P	21 44 48
DP INT AUXCH C N	C909	DP INT AUXCH N	21 44 48

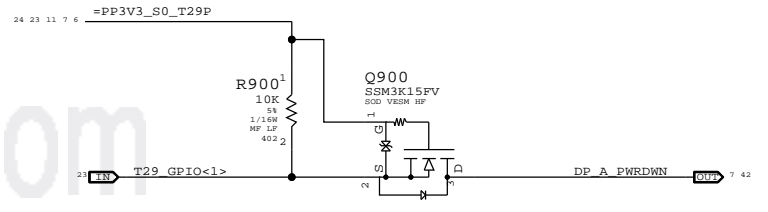
CLOCKS

PCIE CLK100M PCIBR P	==	PCIE CLK100M USB P	32 46
PCIE CLK100M PCIBR N	==	PCIE CLK100M USB N	32 46
PCIBR CLKREQ L	==	PCIE CLKREQ4	
PCIE CLK100M T29S P	==	NC PCIE CLK100M SRC6P	
PCIE CLK100M T29S N	==	NC PCIE CLK100M SRC6N	
T29S CLKREQ L	==	PCIE CLKREQ6	
PCIE CLK100M SLOT P	==	NC PCIE CLK100M SRC1P	
PCIE CLK100M SLOT N	==	NC PCIE CLK100M SRC1N	
PCIESLOT CLKREQ L	==	PCIE CLKREQ1	
PCIE CLK100M SATA P	==	NC PCIE CLK100M SRC9P	
PCIE CLK100M SATA N	==	NC PCIE CLK100M SRC9N	
SATA CLKREQ L	==	PCIE CLKREQ9	
FW CLK24P576M	==	NC FW CLK24P576M	
PS161 CLK27M R	==	NC CLK27M	
PCI CLK33M PCIBR	==	NC PCI CLK33M	
PCI CLK33M NECUSB	==	NC PCI CLK33M	

Wake Sources Power State Isolation



T29 GPIO TO DETECT ERRANT PASSIVE DP CABLE CONNECTION



UNUSED T29 ROUTER GPIOs



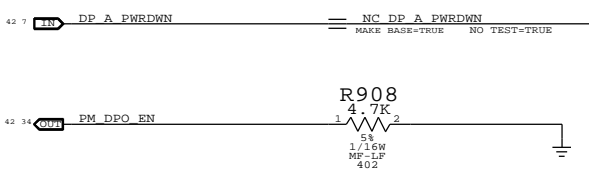
Misc Ethernet Aliases

ENET LOW PWR	==	TP ENET LOW PWR	
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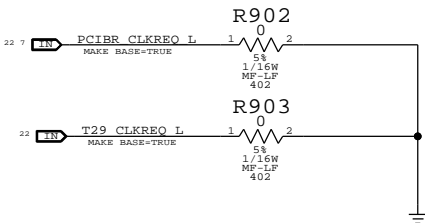
Misc FireWire Aliases

FW PME L	==	TP FW WAKE L	
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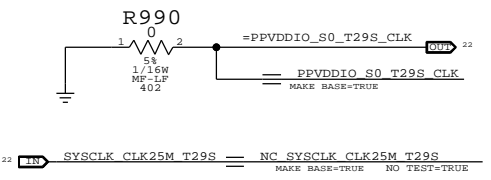
T29 NOCONNECTS DUE TO SINGLE PORT AND NO DPOUT



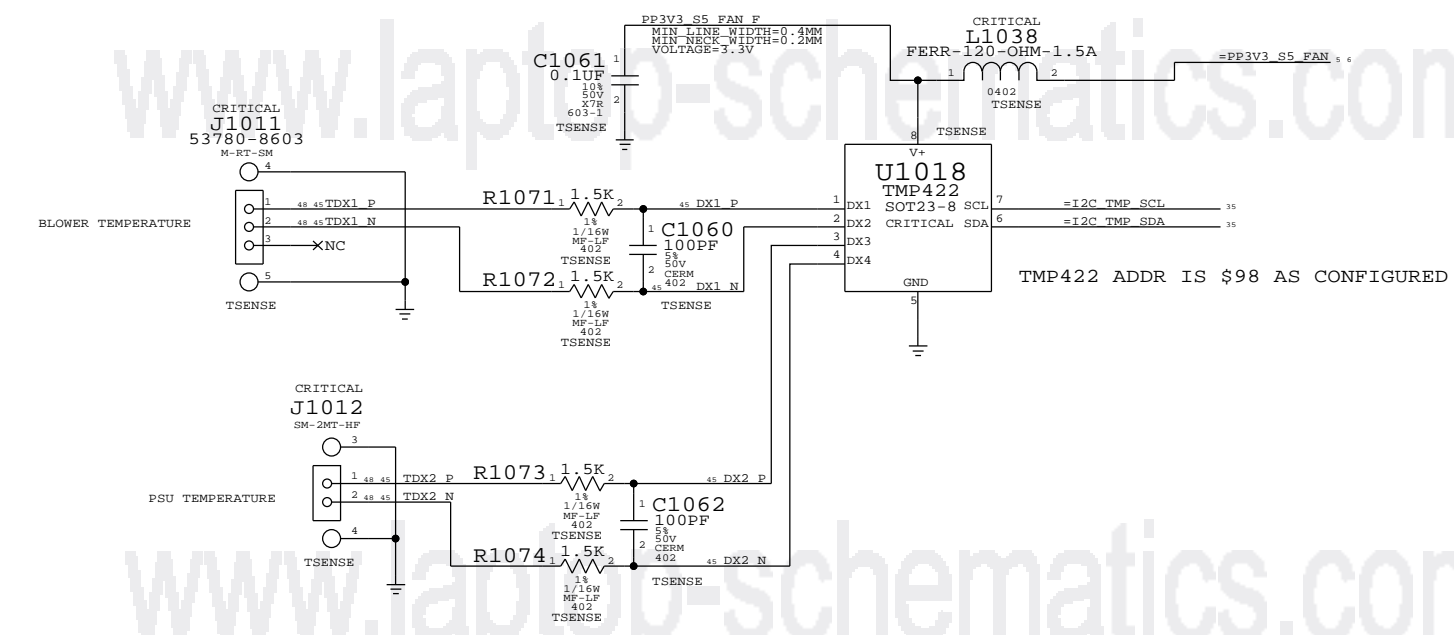
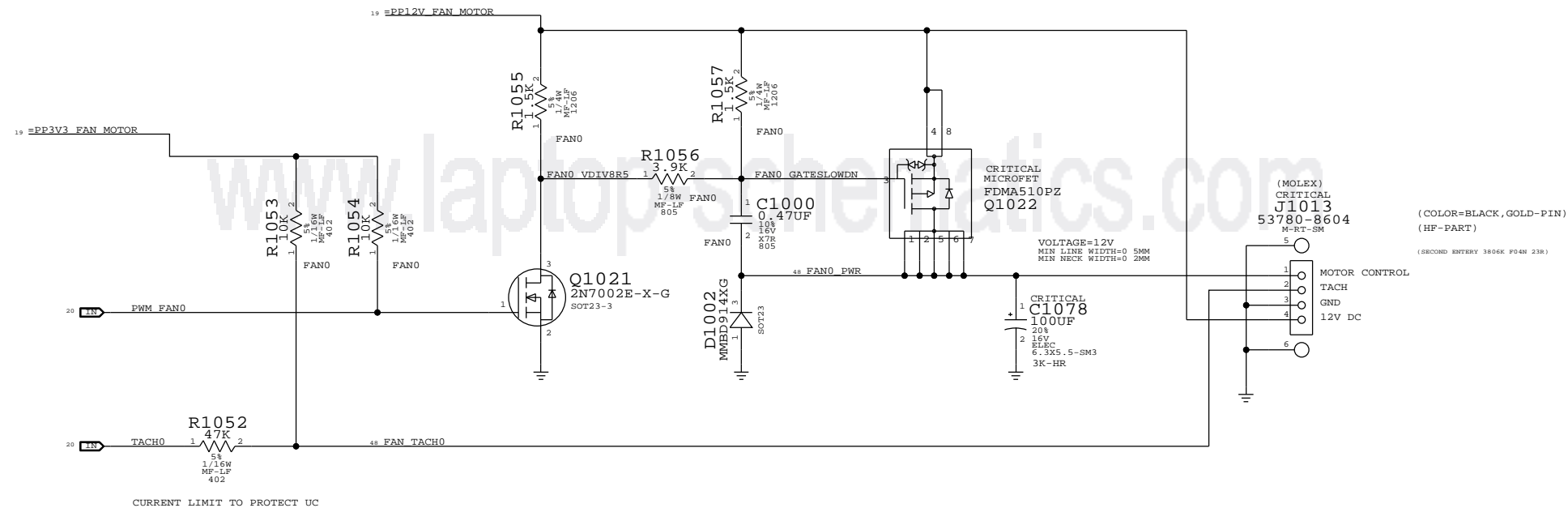
PCIe CLKREQ ENABLING



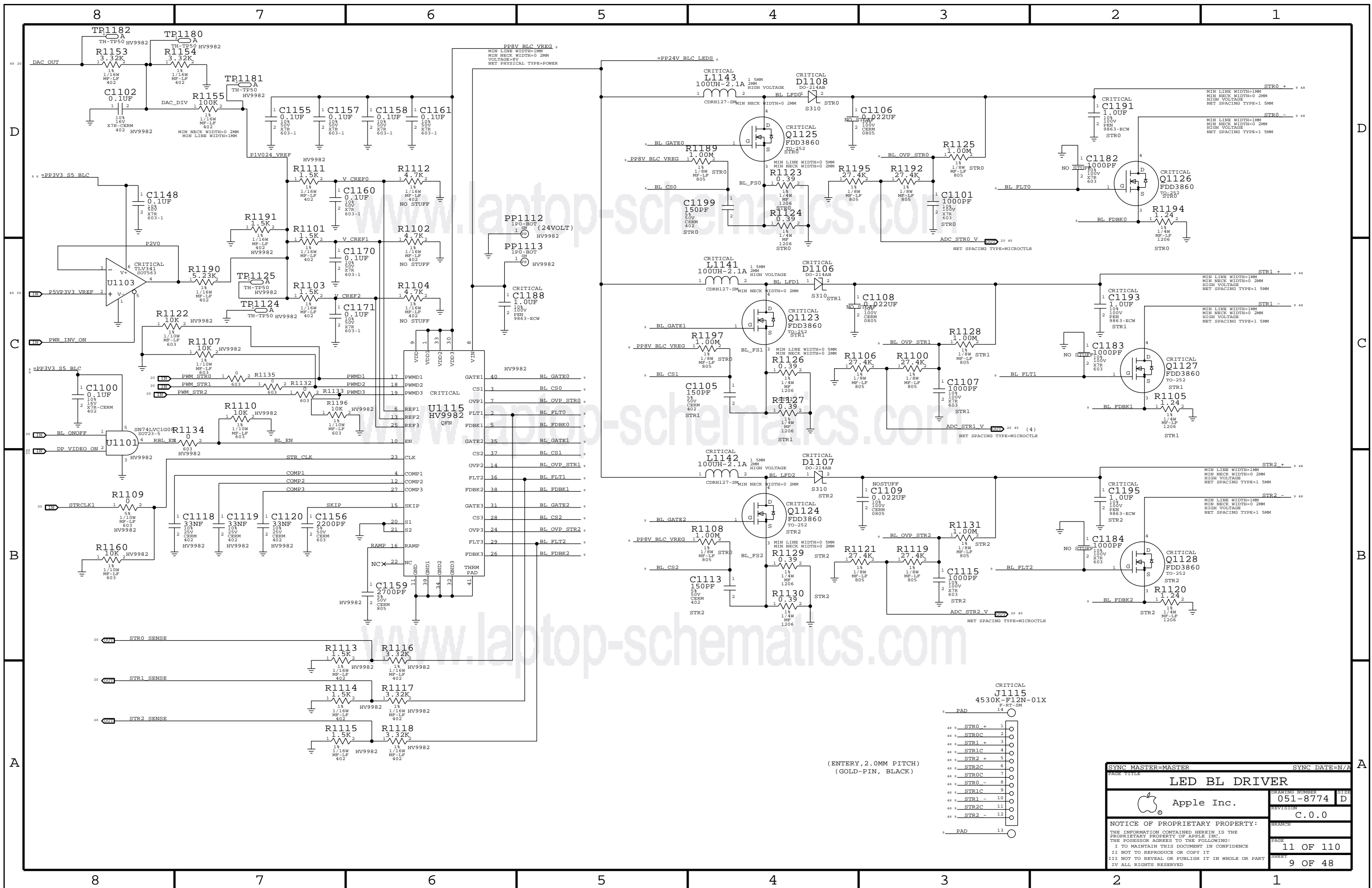
UNUSED T29S GREENCLK



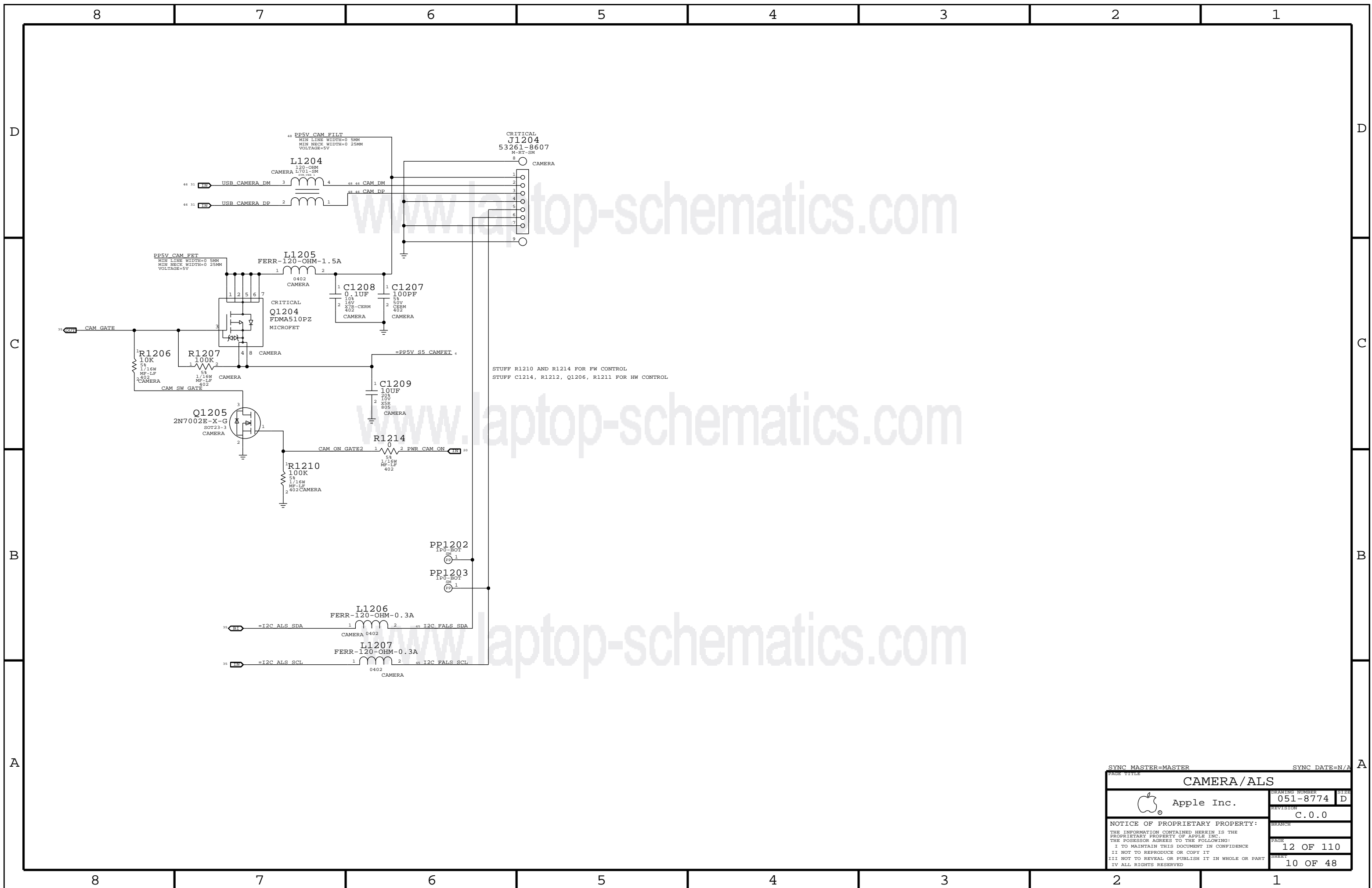
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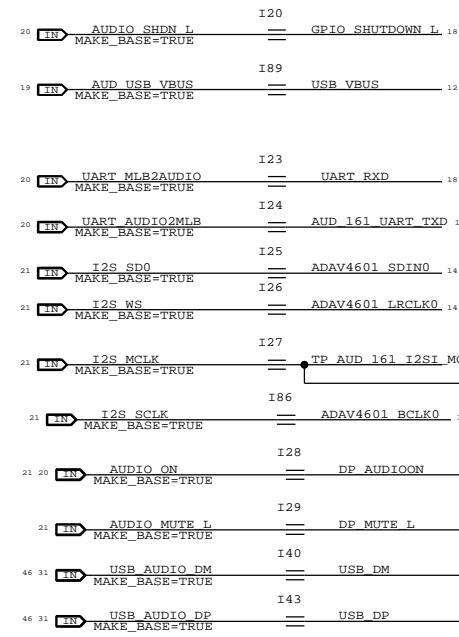
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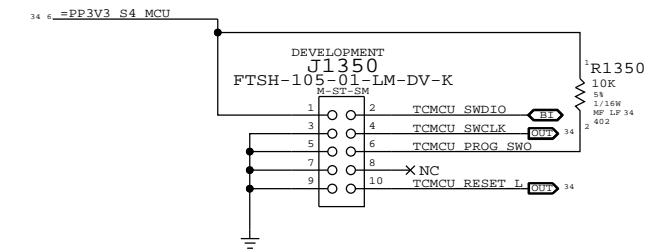
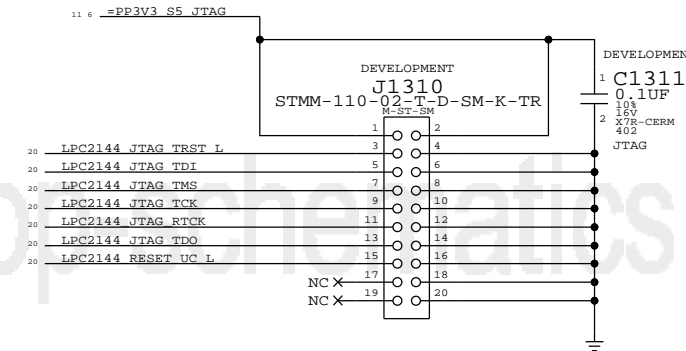
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T29 JTAG AND DEBUG

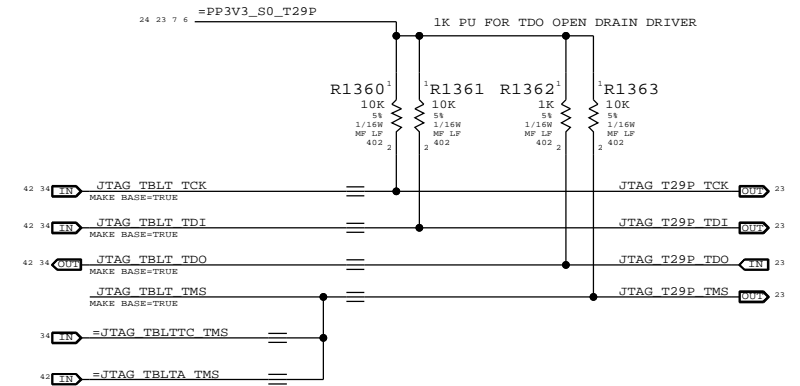
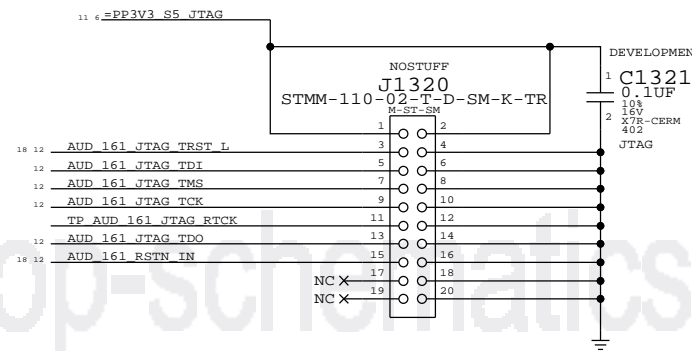
AUDIO ALIASES



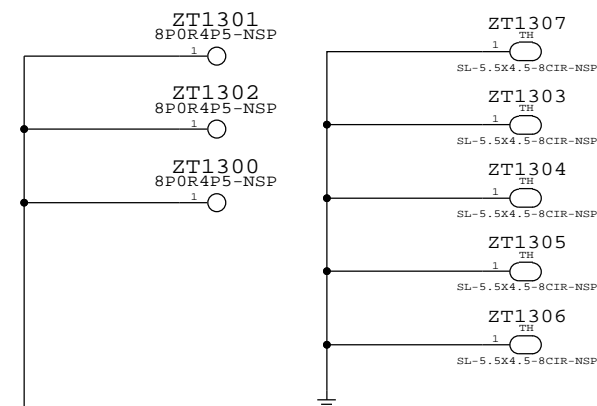
SYSTEM MICRO JTAG



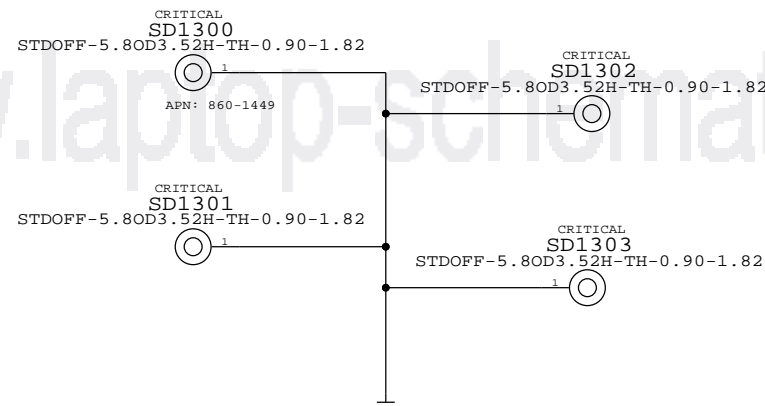
AUDIO JTAG



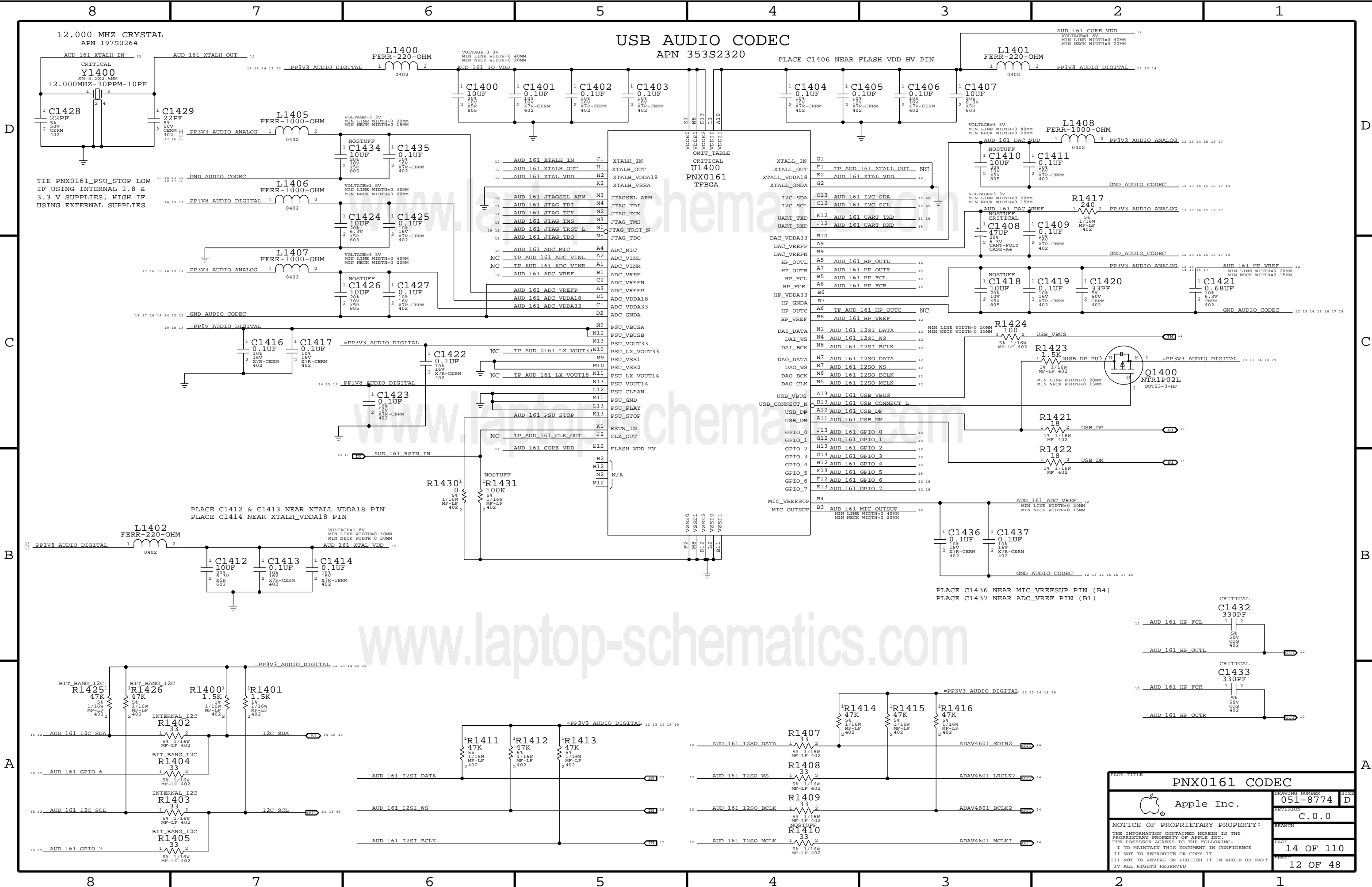
MOUNTING HOLES



J9000 TETHERED CABLE CLAMP STANDOFFS



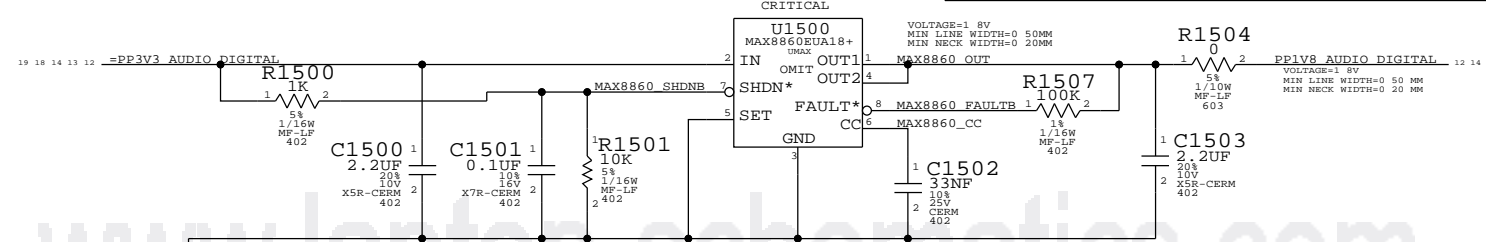
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		C.0.0	
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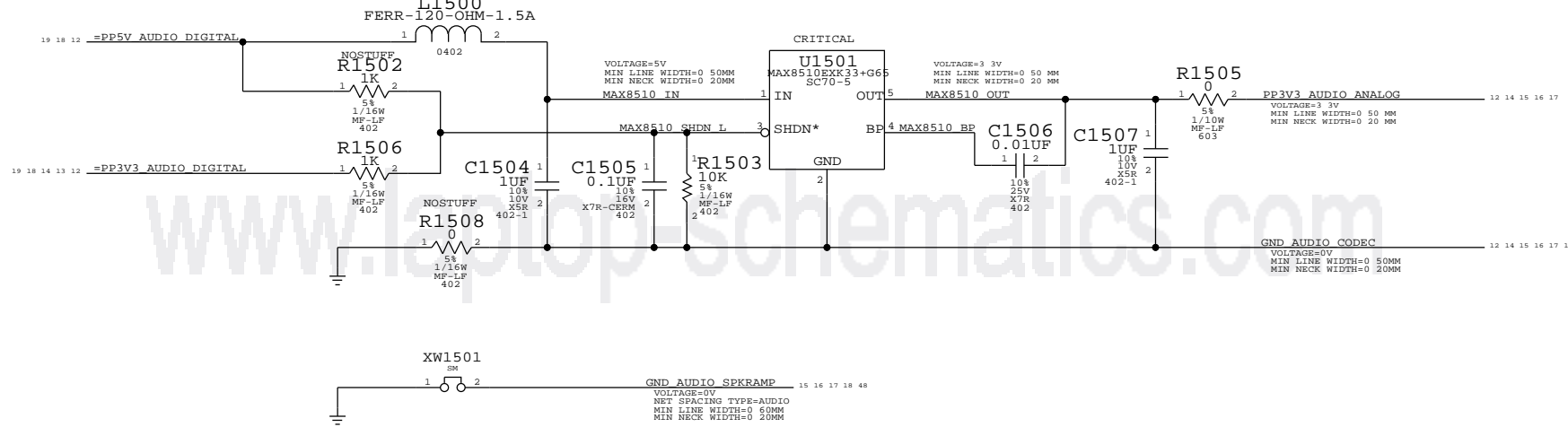
1.8 V REGULATOR  
APN 353S2847

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S2847	1	HF MAX8860EUA18+G65	U1500	



6/16 IT'S UNCLEAR IF ANALOG 3.3 V NEEDS TO COME UP WITH DIGITAL 3.3 V,  
OR IF IT CAN COME UP INDEPENDENTLY (WITH 5 V)  
ANALOG 3.3 COMES UP WITH DIGITAL 3.3 --> POPULATE R1506  
ANALOG 3.3 COMES UP INDEPENDENTLY --> POPULATE R1502

3.3 V REGULATOR  
APN 353S2147



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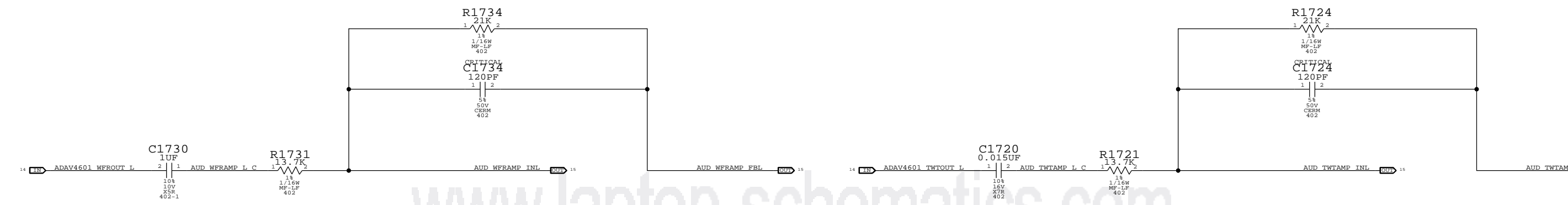
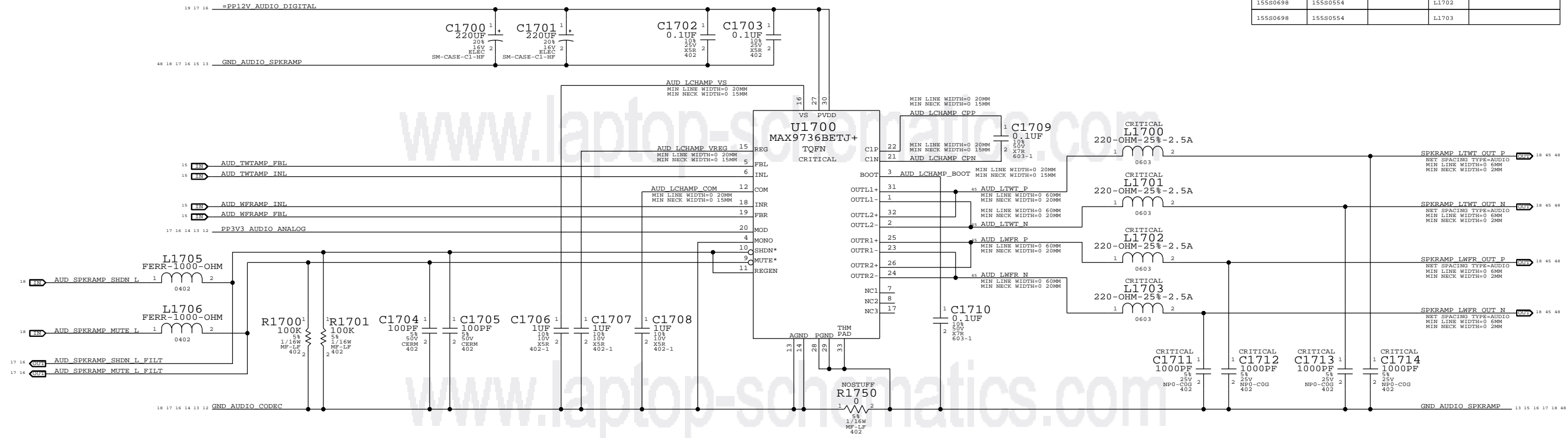
PAGE TITLE <b>AUDIO DC-DC REGULATORS</b>		
	DRAWING NUMBER 051-8774	SIZE D
	REVISION C.0.0	BRANCH
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	PAGE 15 OF 110	SHEET 13 OF 48



# LEFT SPEAKER AMP

APN 353S2042  
 GAIN = 7.36 V/V (+17.33 DB)  
 FC = ~774 HZ (TWEETER), ~12 HZ (WOOFER)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0698	155S0554		L1700	
155S0698	155S0554		L1701	
155S0698	155S0554		L1702	
155S0698	155S0554		L1703	

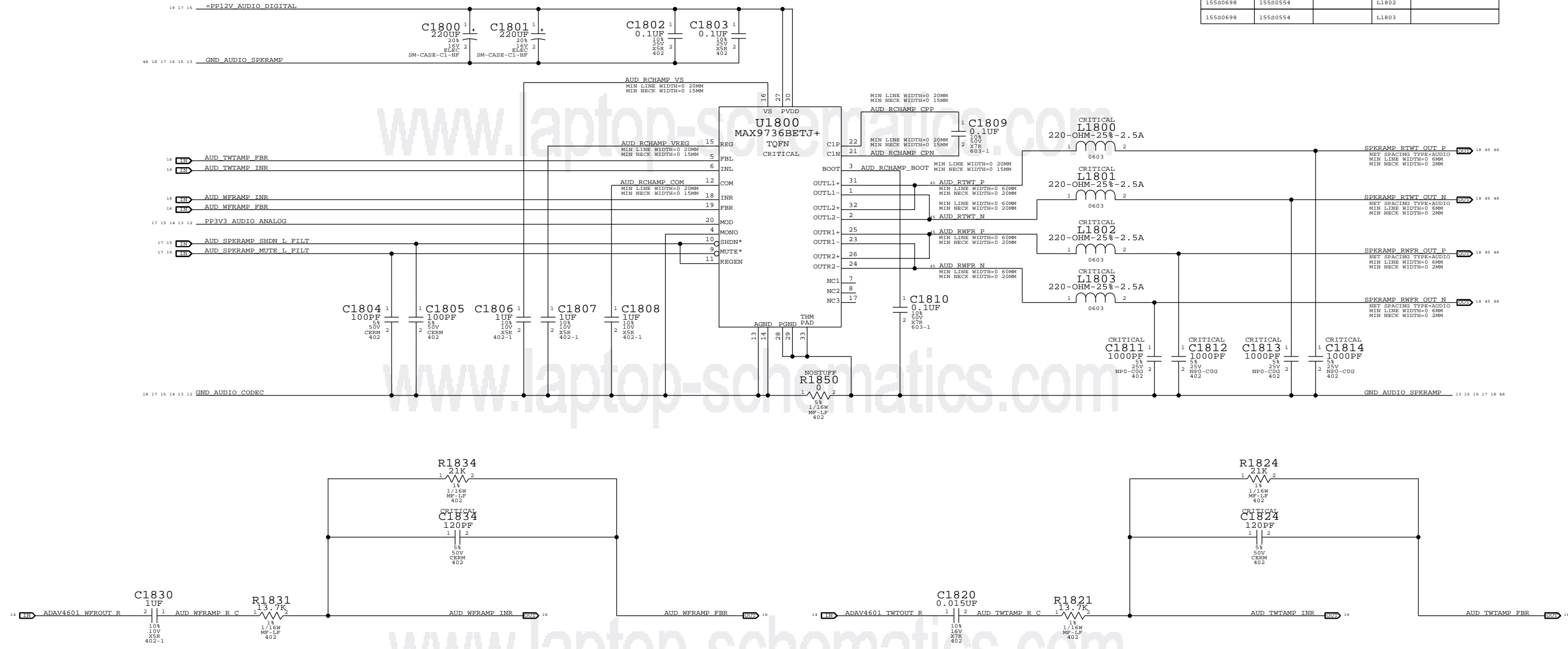


PAGE TITLE		LEFT SPEAKER AMP	
DRAWING NUMBER		051-8774	SIZE D
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# RIGHT SPEAKER AMP

APN 353S2042  
 GAIN = 7.36 V/V (+17.33 DB)  
 FC = ~774 HZ (TWEETER), ~12 HZ (WOOFER)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0698	155S0554		L1800	
155S0698	155S0554		L1801	
155S0698	155S0554		L1802	
155S0698	155S0554		L1803	

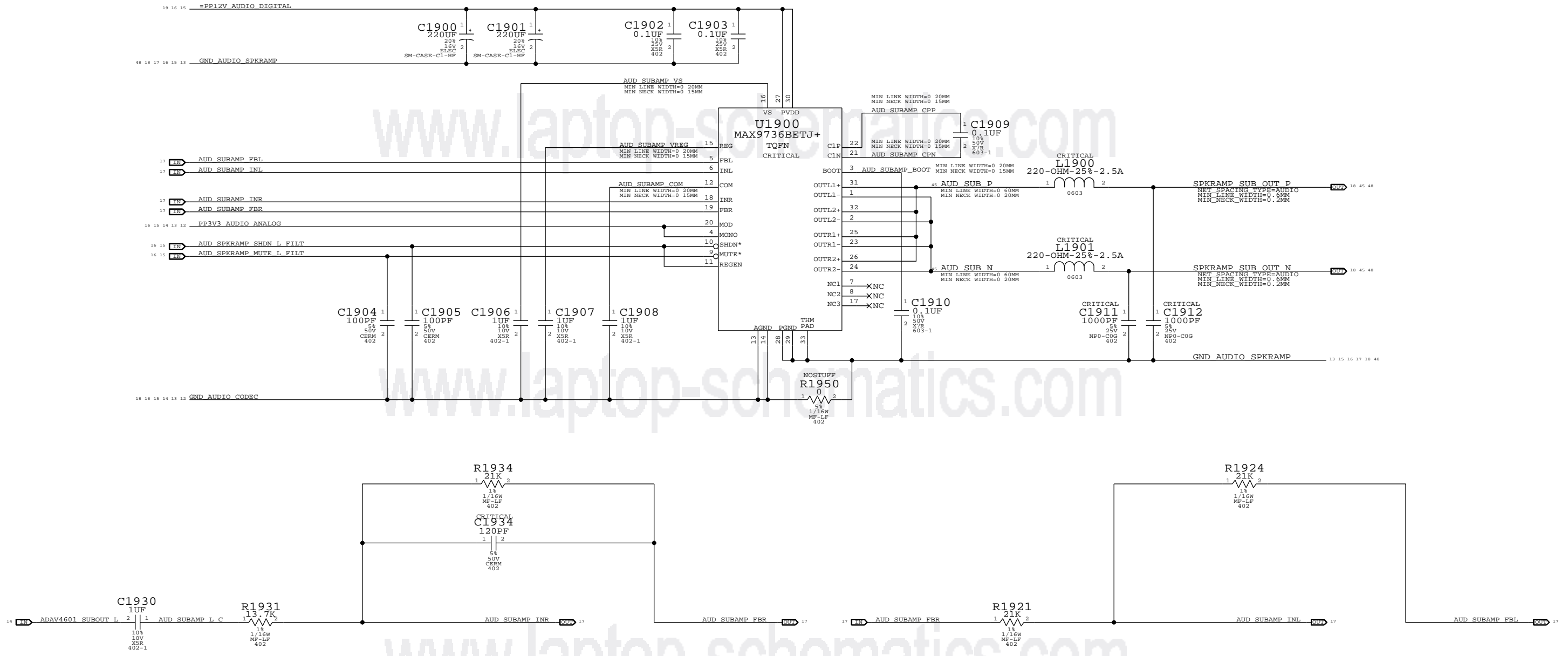


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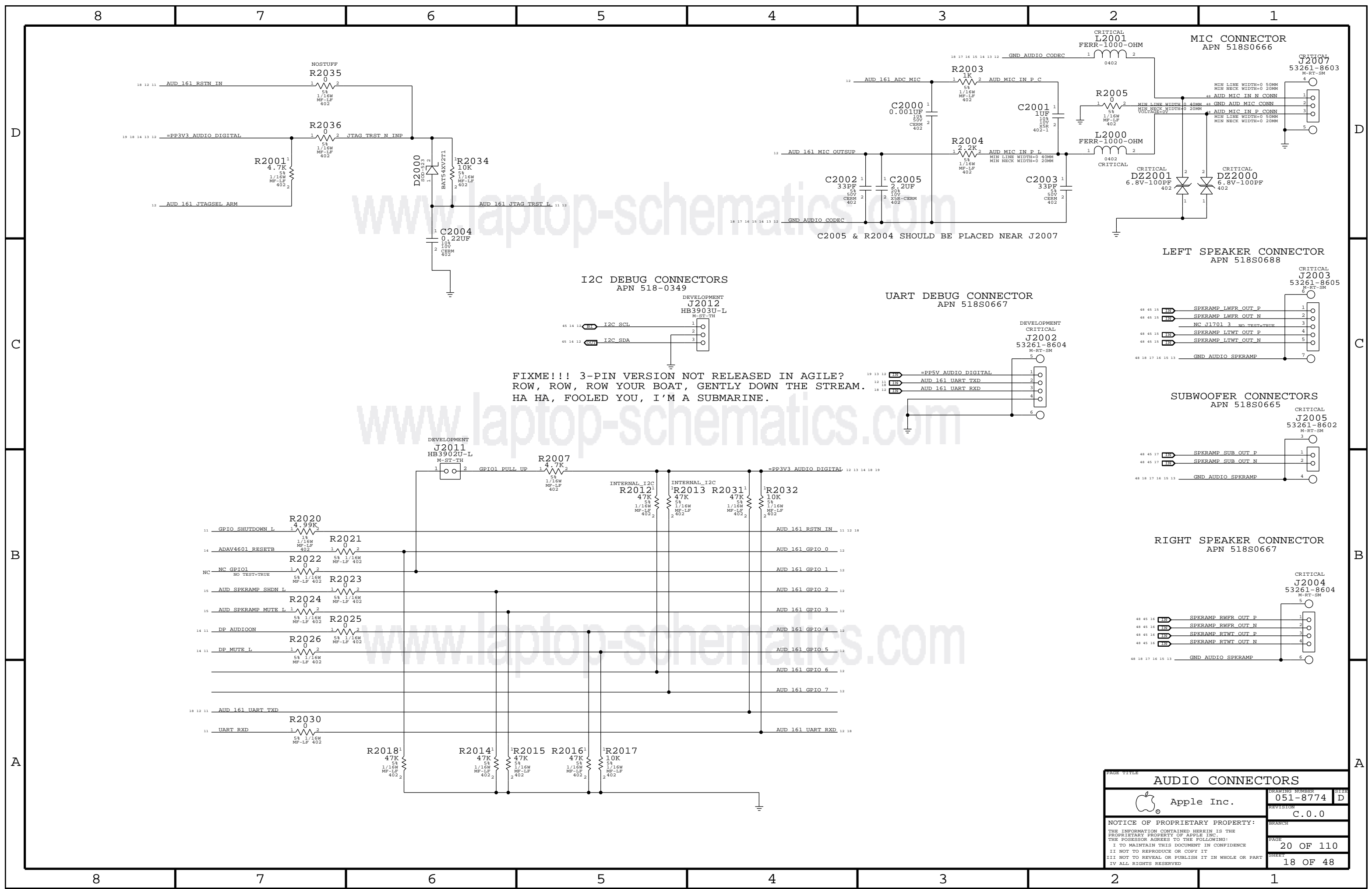
# SUBWOOFER SPEAKER AMP

APN 353S2042  
 GAIN = 7.36 V/V (+17.33 DB)  
 FC = ~12 HZ

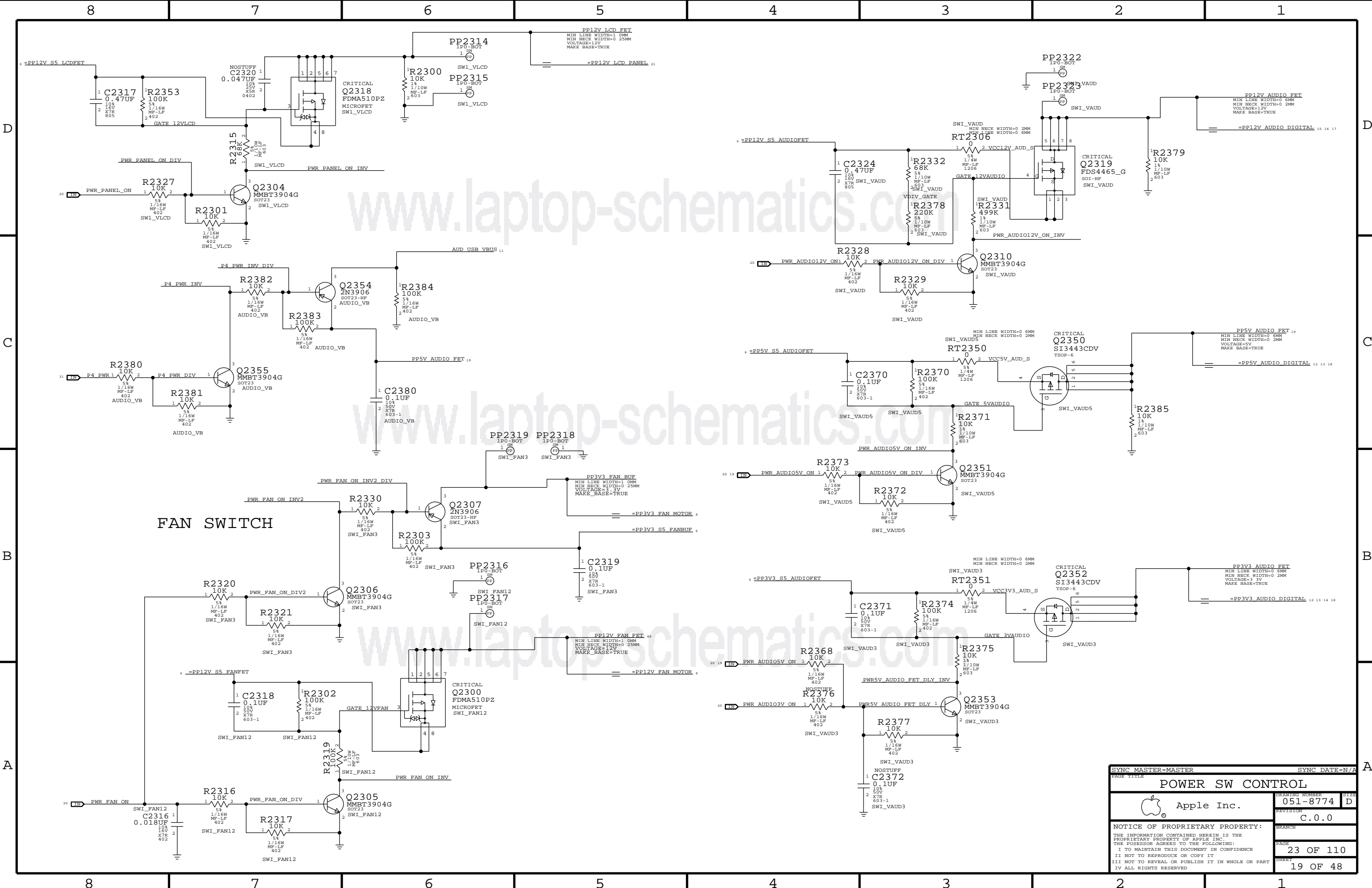
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
155S0698	155S0554		L1900	
155S0698	155S0554		L1901	



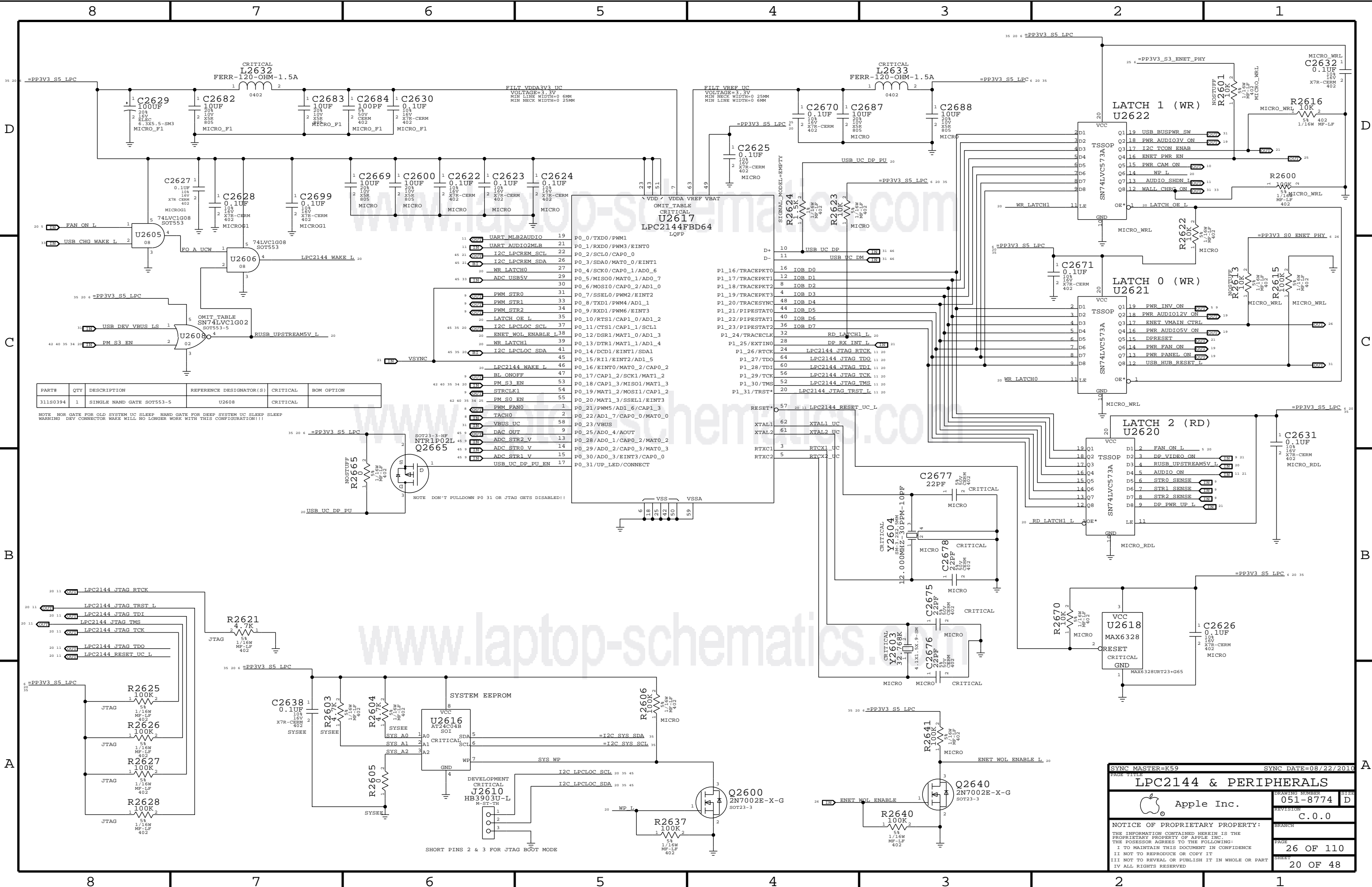
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<b>SUBWOOFER SPEAKER AMP</b>	
Apple Inc.	DRAWING NUMBER <b>051-8774</b>
REVISION <b>C.0.0</b>	
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PAGE TITLE		
<b>AUDIO CONNECTORS</b>		
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SYNC MASTER=MASTER		SYNC DATE=N/A	
PAGE TITLE			
POWER SW CONTROL		DRAWING NUMBER	SIZE
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		19 OF 48	



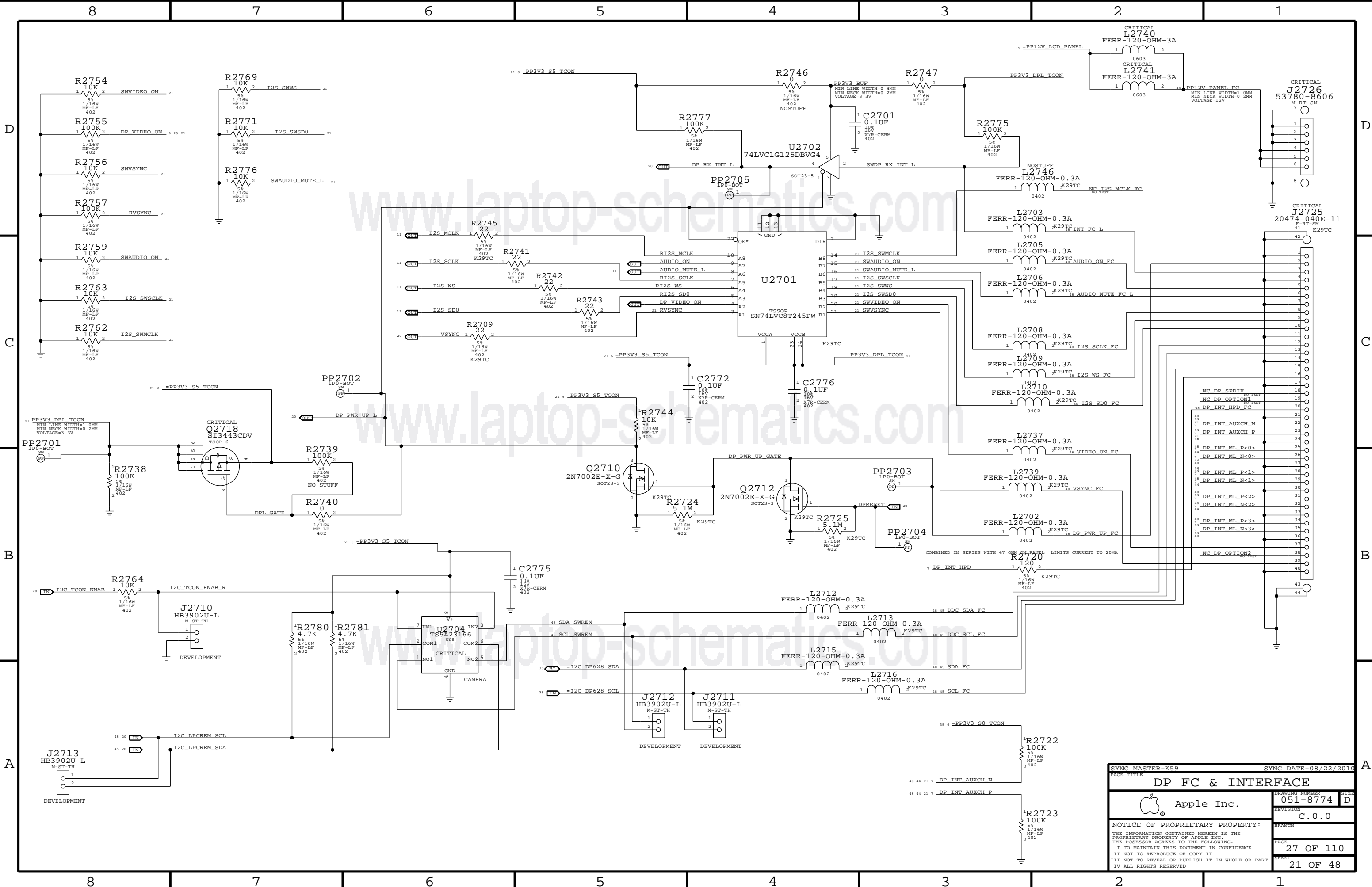
SYNC MASTER=K59 SYNC DATE=08/22/2010

**LPC2144 & PERIPHERALS**

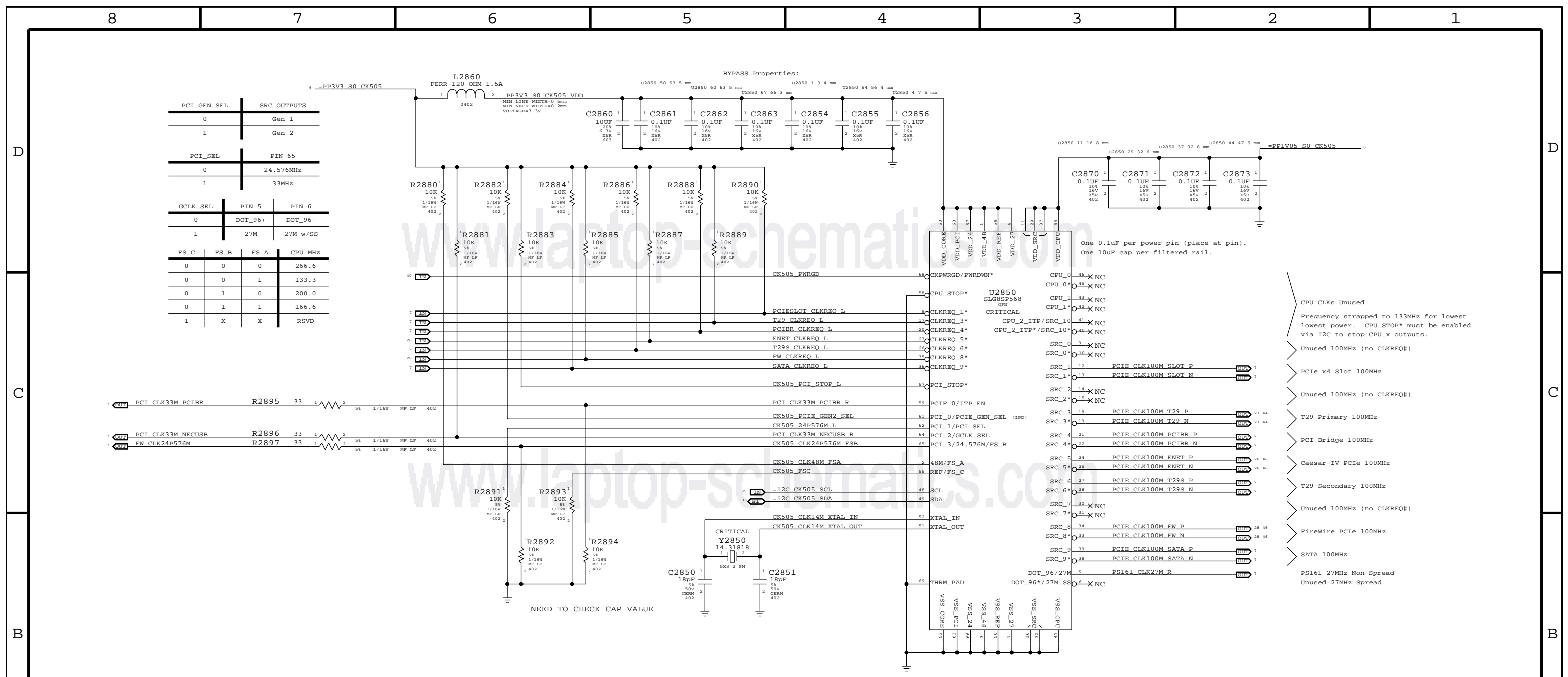
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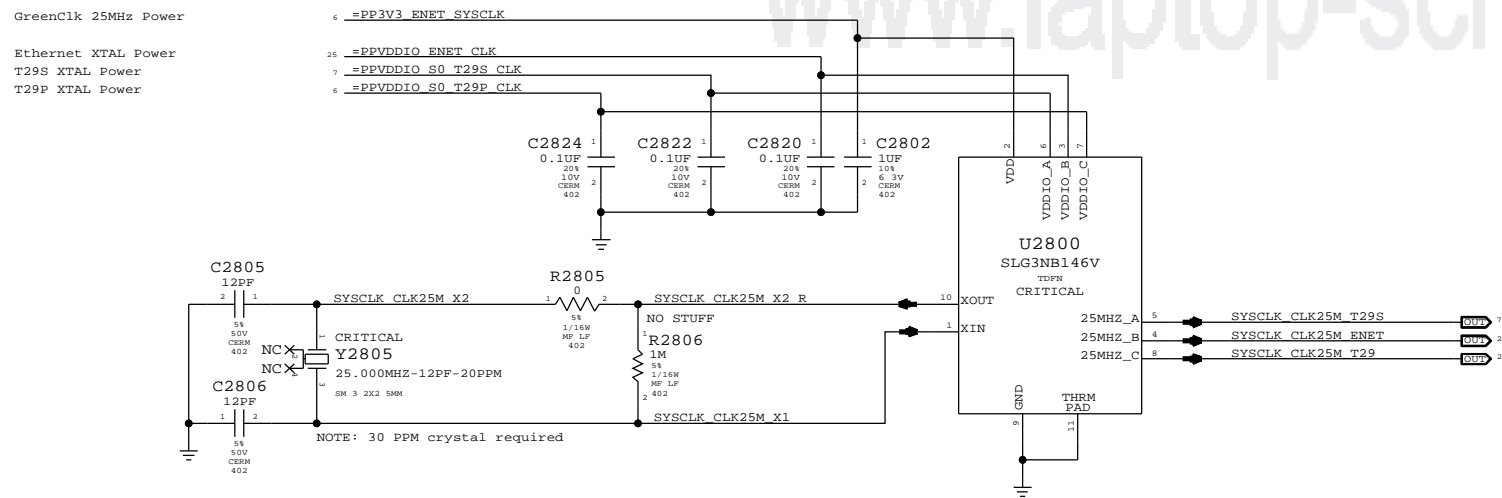


SYNC MASTER=K59		SYNC DATE=08/22/2010	
PAGE TITLE			
DP FC & INTERFACE		DRAWING NUMBER	051-8774
Apple Inc.		REVISION	C.0.0
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PAGE		27 OF 110	
SHEET		21 OF 48	

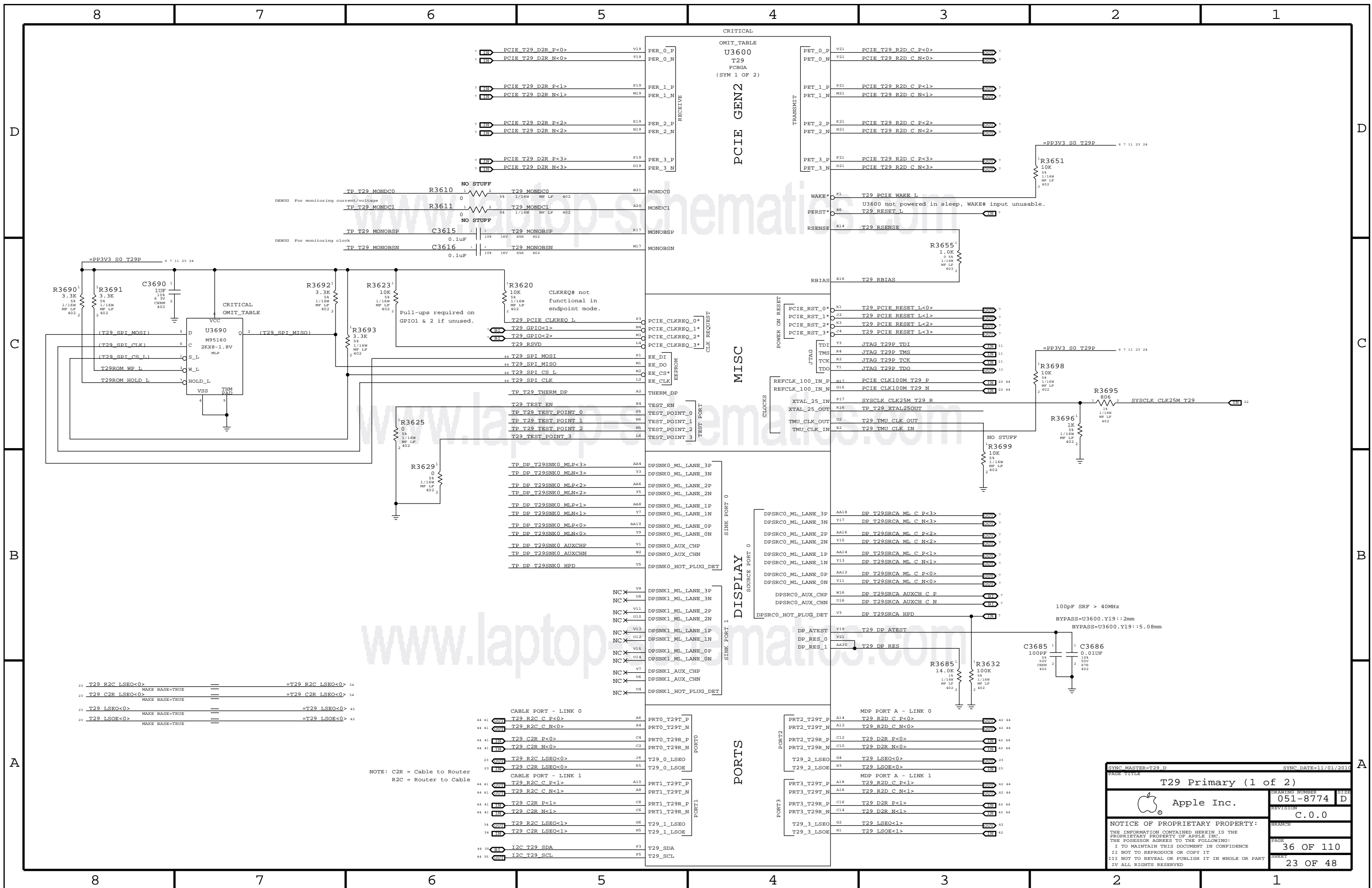


- CPU CLKs Unused
- Frequency strapped to 133MHz for lowest lowest power. CPU\_STOP\* must be enabled via I2C to stop CPU\_x outputs.
- Unused 100MHz (no CLKREQ#)
- PCIe x4 Slot 100MHz
- Unused 100MHz (no CLKREQ#)
- T29 Primary 100MHz
- PCI Bridge 100MHz
- Caesar-IV PCIe 100MHz
- T29 Secondary 100MHz
- Unused 100MHz (no CLKREQ#)
- FireWire PCIe 100MHz
- SATA 100MHz
- PS161 27MHz Non-Spread
- Unused 27MHz Spread

### System 25MHz Clock Generator



SYNCH MASTER=T29 D		SYNCH DATE=03/17/2011	
PAGE TITLE			
<b>T29 Clocking</b>			
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DEBUG For monitoring current/voltage

TP T29 MONDC0 R3610 NO STUFF

TP T29 MONDC1 R3611 NO STUFF

DEBUG For monitoring clock

TP T29 MONOBSP C3615 NO STUFF

TP T29 MONOBSN C3616 NO STUFF

CRITICAL OMIT\_TABLE

Pull-ups required on GPIO1 & 2 if unused.

CLKREQ# not functional in endpoint mode.

TP T29 THERM DP

T29 TEST EN

TP T29 TEST POINT 0

TP T29 TEST POINT 1

TP T29 TEST POINT 2

TP T29 TEST POINT 3

TP DP T29SNK0\_MLP<3>

TP DP T29SNK0\_MLN<3>

TP DP T29SNK0\_MLP<2>

TP DP T29SNK0\_MLN<2>

TP DP T29SNK0\_MLP<1>

TP DP T29SNK0\_MLN<1>

TP DP T29SNK0\_MLP<0>

TP DP T29SNK0\_MLN<0>

TP DP T29SNK0\_AUXCHP

TP DP T29SNK0\_AUXCHN

TP DP T29SNK0\_HPD

NOTE: C2R = Cable to Router

R2C = Router to Cable

CABLE PORT - LINK 0

T29 R2C C P<0>

T29 R2C C N<0>

T29 C2R P<0>

T29 C2R N<0>

T29 R2C LSEO<0>

T29 C2R LSEO<0>

T29\_0\_LSEO

T29\_0\_LSOE

CABLE PORT - LINK 1

T29 R2C C P<1>

T29 R2C C N<1>

T29 C2R P<1>

T29 C2R N<1>

T29 R2C LSEO<1>

T29 C2R LSEO<1>

T29\_1\_LSEO

T29\_1\_LSOE

I2C T29 SDA

I2C T29 SCL

SYNC MASTER=T29 D SYNC DATE=11/01/2011

PAGE TITLE

T29 Primary (1 of 2)

Apple Inc.

DRAWING NUMBER 051-8774

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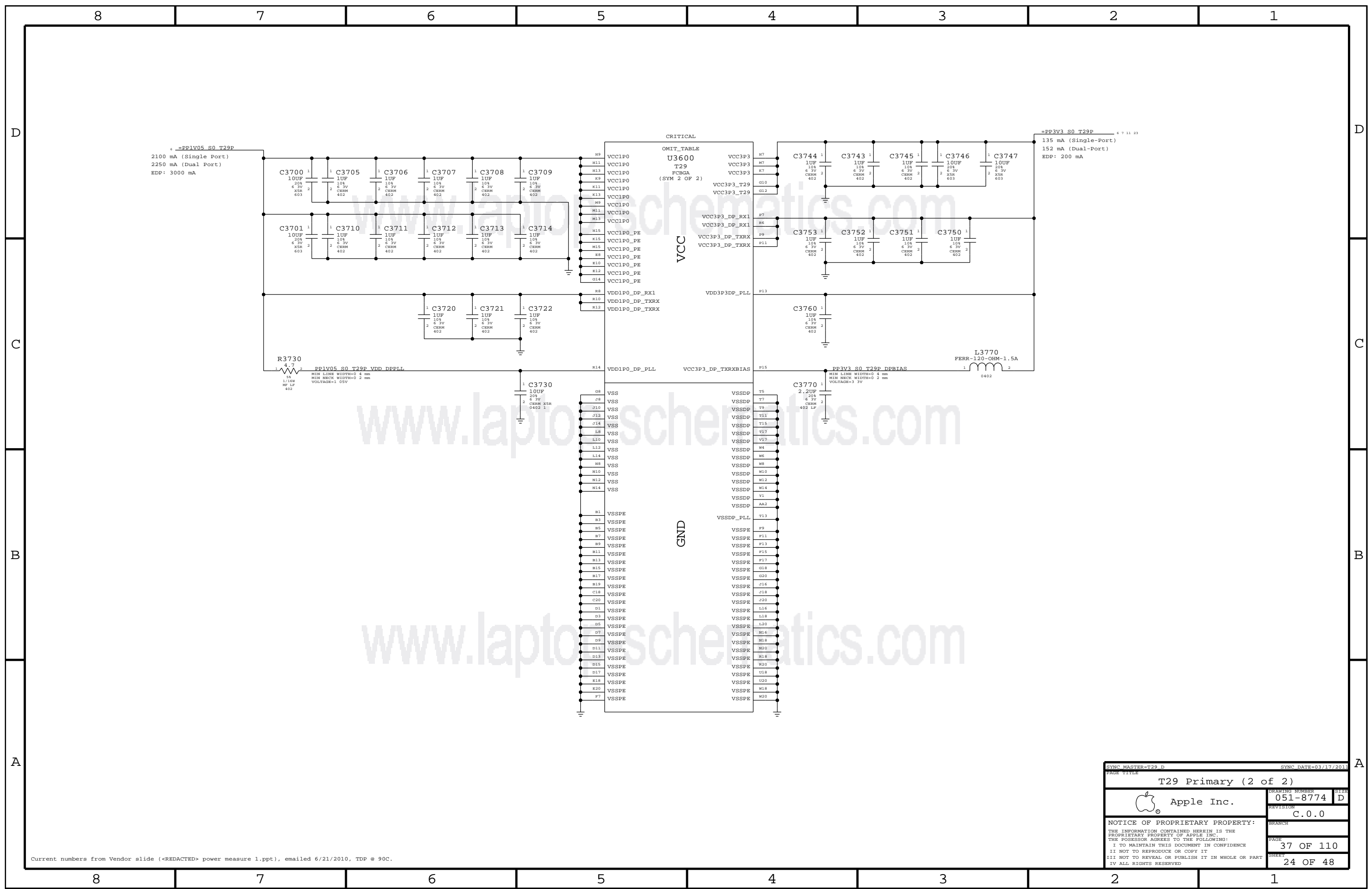
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=PP1V05 S0 T29P  
 2100 mA (Single Port)  
 2250 mA (Dual Port)  
 EDP: 3000 mA

=PP3V3 S0 T29P  
 135 mA (Single-Port)  
 152 mA (Dual-Port)  
 EDP: 200 mA

R3730  
 5k  
 1/16W  
 0402

PP1V05 S0 T29P VDD DEPLL  
 MIN LINE WIDTH=0.4 mm  
 MIN NECK WIDTH=0.2 mm  
 VOLTAGE=1.05V

C3730  
 10UF  
 20%  
 6.3V  
 X5R  
 0402 1

C3770  
 2.2UF  
 20%  
 6.3V  
 X5R  
 0402 LP

L3770  
 FERR-120-OHM-1.5A  
 0402

CRITICAL  
 OMIT\_TABLE  
 U3600  
 T29  
 FBGA  
 (SYM 2 OF 2)

H9	VCC1P0	VCC3P3	H7	C3744	1	1UF	10%	6.3V	X5R	402
H11	VCC1P0	VCC3P3	H7	C3743	1	1UF	10%	6.3V	X5R	402
H13	VCC1P0	VCC3P3	K7	C3745	1	1UF	10%	6.3V	X5R	402
K9	VCC1P0	VCC3P3	K7	C3746	1	10UF	20%	6.3V	X5R	603
K11	VCC1P0	VCC3P3_T29	G10	C3747	1	10UF	20%	6.3V	X5R	603
K13	VCC1P0	VCC3P3_T29	G12							
M9	VCC1P0	VCC3P3_DP_RX1	P7							
M11	VCC1P0	VCC3P3_DP_RX1	R6							
M13	VCC1P0	VCC3P3_DP_TXRX	P9	C3753	1	1UF	10%	6.3V	X5R	402
H15	VCC1P0_PE	VCC3P3_DP_TXRX	P11	C3752	1	1UF	10%	6.3V	X5R	402
K15	VCC1P0_PE	VCC3P3_DP_TXRX	P9	C3751	1	1UF	10%	6.3V	X5R	402
M15	VCC1P0_PE	VCC3P3_DP_TXRX	P11	C3750	1	1UF	10%	6.3V	X5R	402
K15	VCC1P0_PE	VCC3P3_DP_TXRX								
M15	VCC1P0_PE	VCC3P3_DP_TXRX								
K12	VCC1P0_PE	VCC3P3_DP_TXRX								
G14	VCC1P0_PE	VCC3P3_DP_TXRX								
R8	VDD1P0_DP_RX1	VDD3P3DP_PLL	P13	C3760	1	1UF	10%	6.3V	X5R	402
R10	VDD1P0_DP_TXRX	VDD3P3DP_PLL								
R12	VDD1P0_DP_TXRX	VDD3P3DP_PLL								
R14	VDD1P0_DP_PLL	VCC3P3_DP_TXRXBIAS	P15							
G8	VSS	VSSDP	T5							
J8	VSS	VSSDP	T7							
J10	VSS	VSSDP	T9							
J12	VSS	VSSDP	T11							
J14	VSS	VSSDP	T13							
L8	VSS	VSSDP	T17							
L10	VSS	VSSDP	V17							
L12	VSS	VSSDP	W4							
L14	VSS	VSSDP	W6							
N8	VSS	VSSDP	W8							
N10	VSS	VSSDP	W10							
N12	VSS	VSSDP	W12							
N14	VSS	VSSDP	W14							
B1	VSSPE	VSSDP_PLL	T13							
B3	VSSPE	VSSDP	F9							
B5	VSSPE	VSSDP	F11							
B7	VSSPE	VSSDP	F13							
B9	VSSPE	VSSDP	F15							
B11	VSSPE	VSSDP	F17							
B13	VSSPE	VSSDP	G18							
B15	VSSPE	VSSDP	G20							
B17	VSSPE	VSSDP	J16							
B19	VSSPE	VSSDP	J18							
C18	VSSPE	VSSDP	J20							
C20	VSSPE	VSSDP	L16							
D1	VSSPE	VSSDP	L18							
D3	VSSPE	VSSDP	L20							
D5	VSSPE	VSSDP	N16							
D7	VSSPE	VSSDP	N18							
D9	VSSPE	VSSDP	N20							
D11	VSSPE	VSSDP	N18							
D13	VSSPE	VSSDP	N20							
D15	VSSPE	VSSDP	U18							
D17	VSSPE	VSSDP	U20							
R18	VSSPE	VSSDP	W18							
R20	VSSPE	VSSDP	W20							
F7	VSSPE	VSSDP								

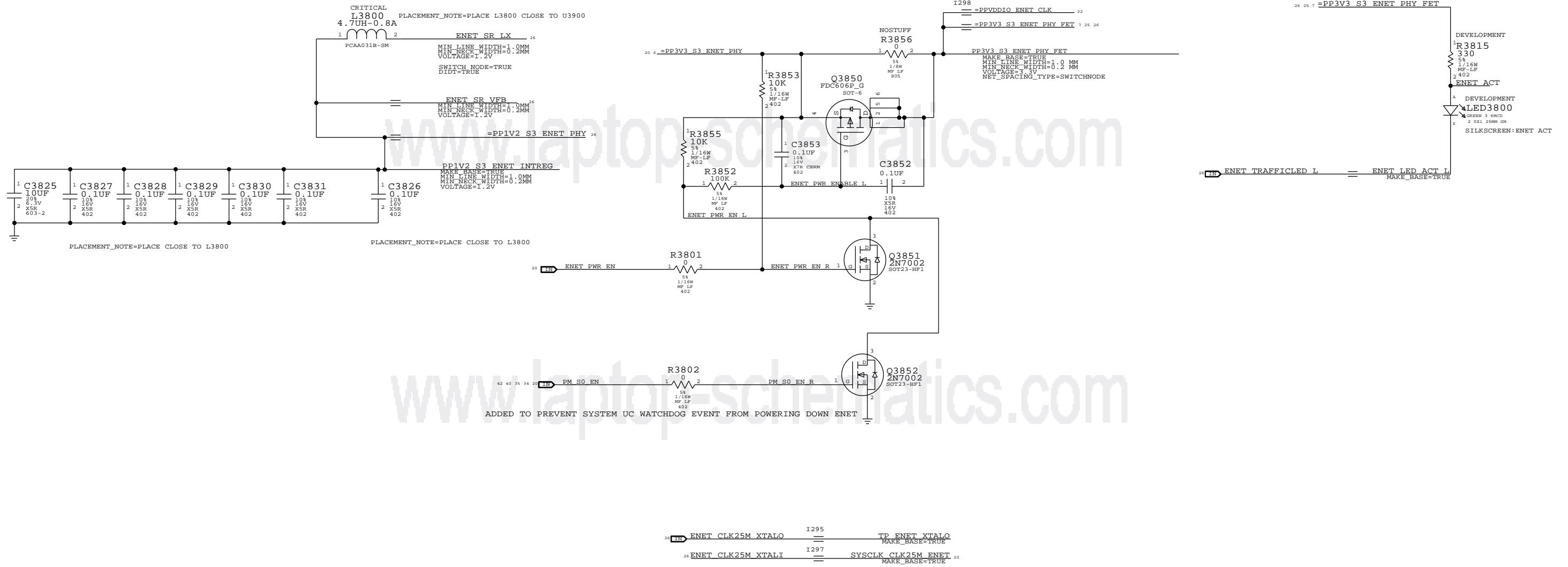
Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC MASTER=T29 D		SYNC DATE=03/17/2011	
PAGE TITLE T29 Primary (2 of 2)			
DRAWING NUMBER 051-8774		SIZE D	
REVISION C.0.0		BRANCH	
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CAESAR IV 1.2V INT.VR CMPTS

CAESAR IV POWER ENABLE CIRCUIT

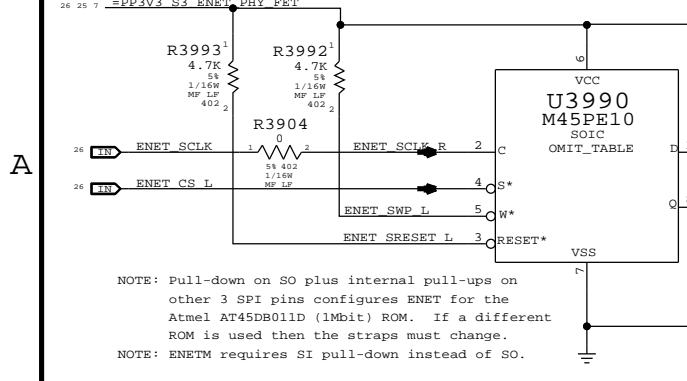
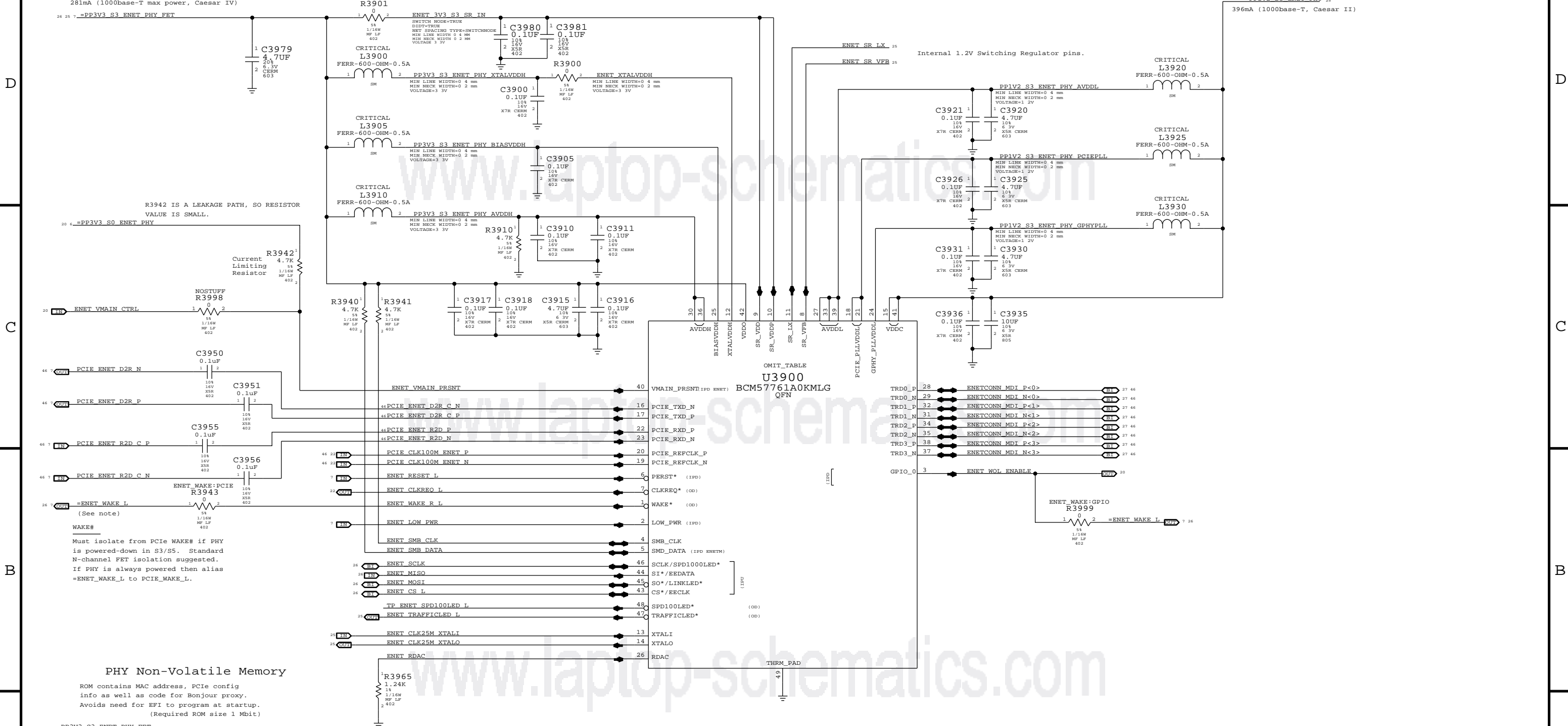
CAESAR IV ACTIVITY LED



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SYNC MASTER=K62		SYNC DATE=09/16/2010	
<b>CAESAR IV SUPPORT</b>			
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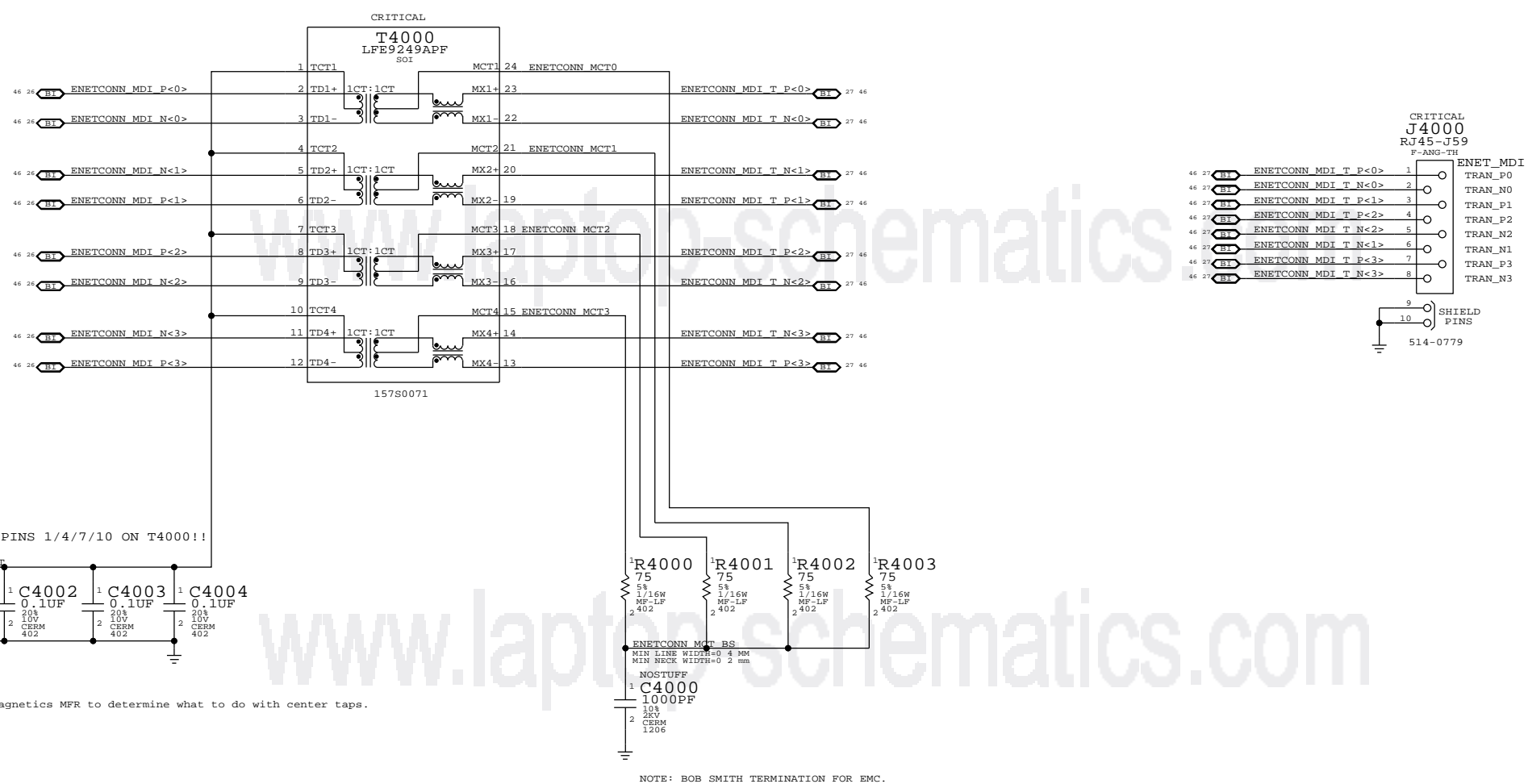
BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR\_DISABLE below. If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PPIV2\_S3\_ENET\_PHY. If enabled: VDD/VDDP connect to =PP3V3\_S3\_ENET\_PHY (add bypassing), LX connects to inductor. Special Star routing needed on these pins. Decoupling on Pg 37.



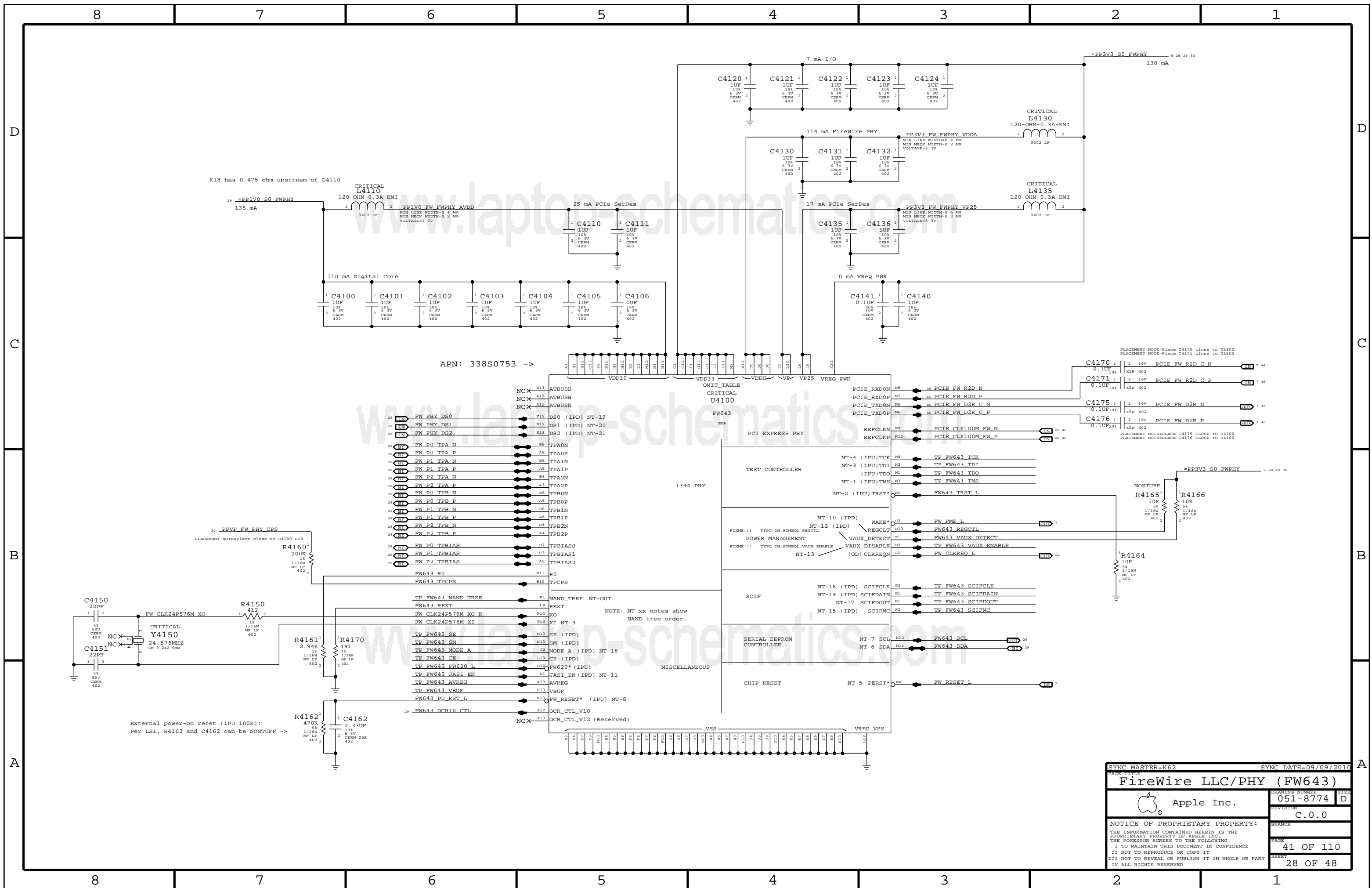
PHY Non-Volatile Memory  
ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Avoids need for EFI to program at startup. (Required ROM size 1 Mbit)  
NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.  
NOTE: ENETM requires SI pull-down instead of SO.

SYNC MASTER=TONY		SYNC DATE=10/01/2011	
PAGE TITLE		PAGE TITLE	
ETHERNET PHY (CAESAR IV)		DRAWING NUMBER	051-8774
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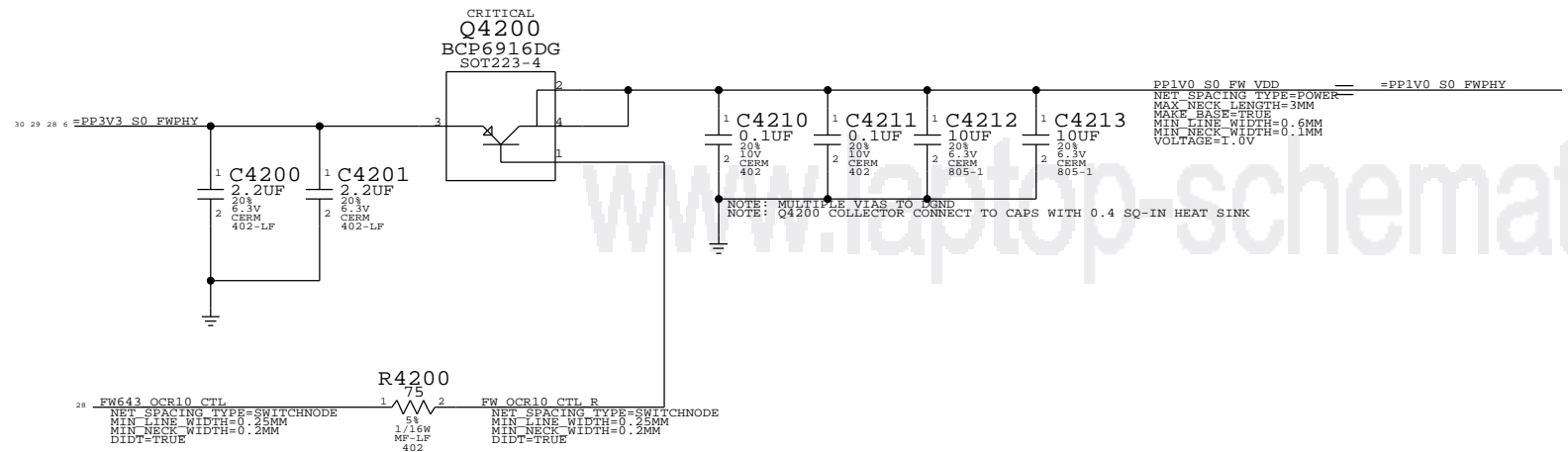


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Ethernet Connector			
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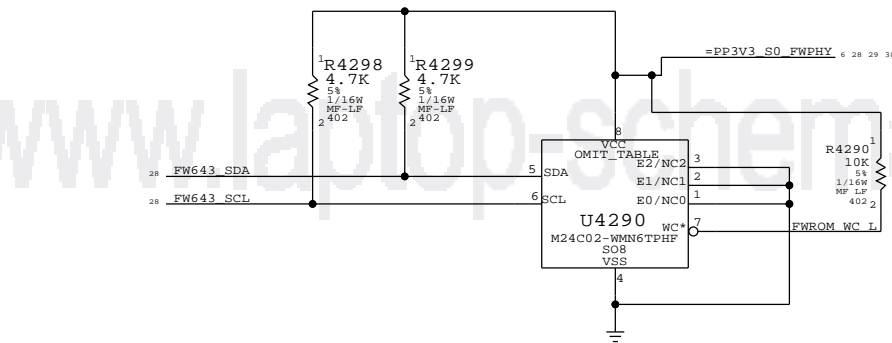


SYNC MASTER=K62		SYNC DATE=09/09/2010	
PAGE TITLE <b>FireWire LLC/PHY (FW643)</b>			
Apple Inc.		DRAWING NUMBER 051-8774	SIZE D
		REVISION C.0.0	
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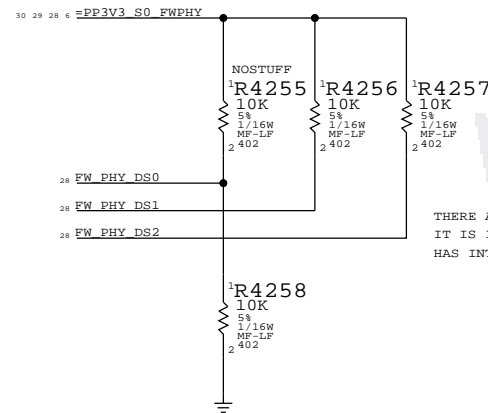
FW643 1.0V GENERATION



FW643 GUID ROM

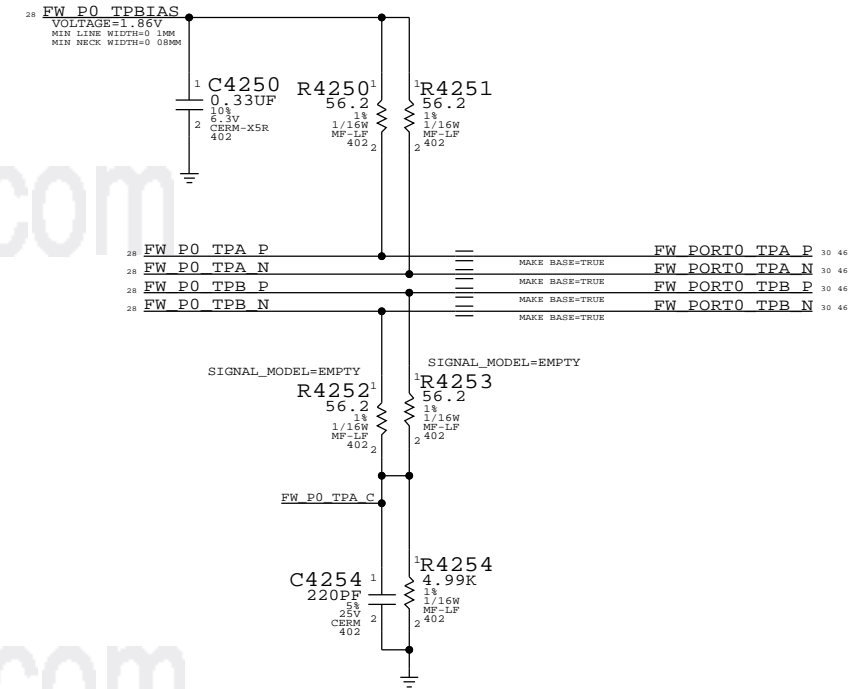


1394 PHY DATA/STROBE OPTIONS



THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED. NO STUFF MEANS THAT IT IS IN BILINGUAL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE, FW643 HAS INTERNAL 100K PULL-DOWNS, ONLY PULL-UPS NECESSARY.

Termination  
Place close to FireWire PHY

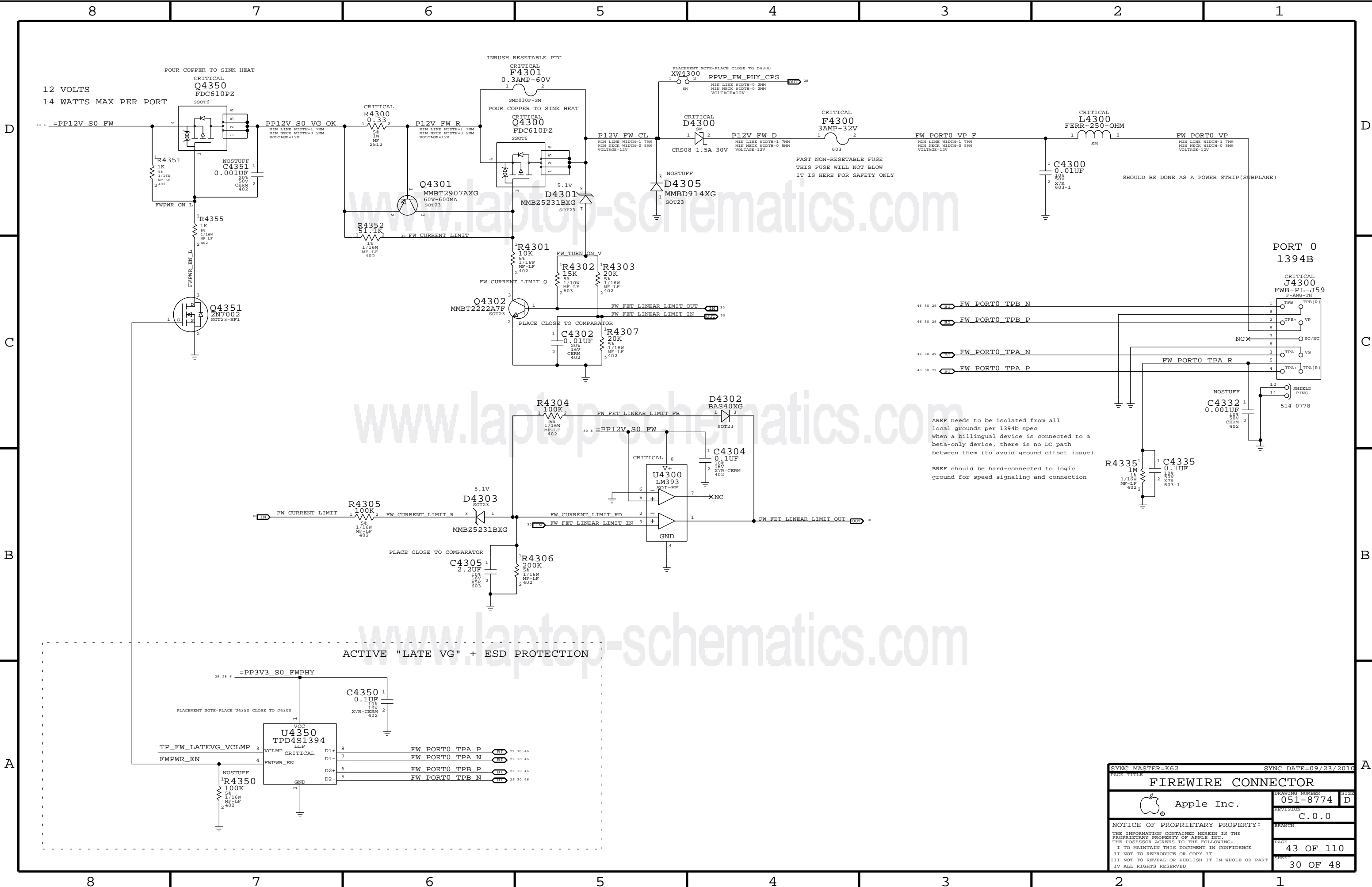


2ND & 3RD TPA/TPB PAIR UNUSED

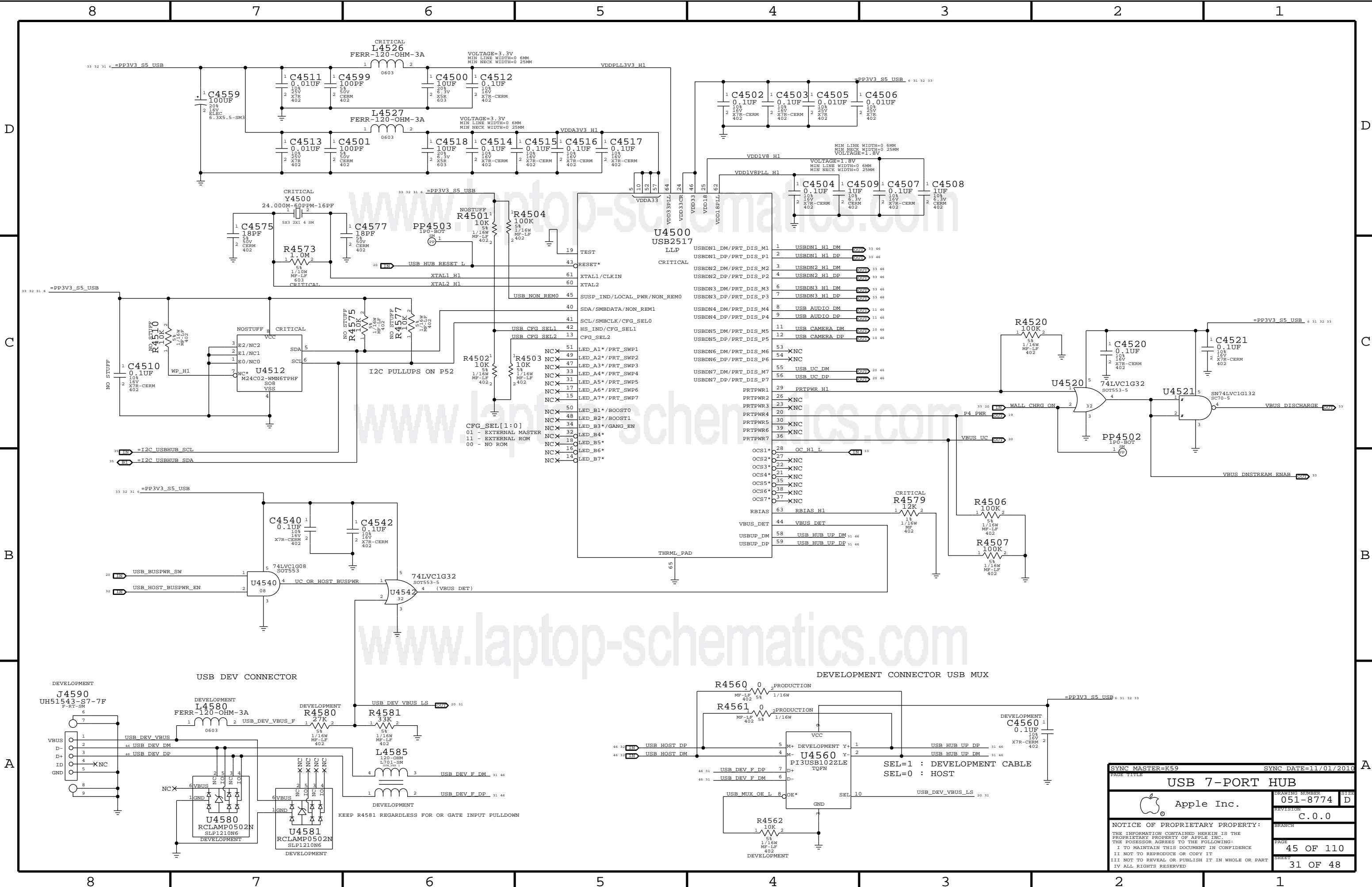
- FW\_P1\_TPBIAIS == NC FW\_PORT1\_TPBIAIS
- FW\_P1\_TPA\_P == NC FW\_PORT1\_TPA\_P
- FW\_P1\_TPA\_N == NC FW\_PORT1\_TPA\_N
- FW\_P1\_TPB\_P == NC FW\_PORT1\_TPB\_P
- FW\_P1\_TPB\_N == NC FW\_PORT1\_TPB\_N
- FW\_P2\_TPBIAIS == NC FW\_PORT2\_TPBIAIS
- FW\_P2\_TPA\_P == NC FW\_PORT2\_TPA\_P
- FW\_P2\_TPA\_N == NC FW\_PORT2\_TPA\_N
- FW\_P2\_TPB\_P == NC FW\_PORT2\_TPB\_P
- FW\_P2\_TPB\_N == NC FW\_PORT2\_TPB\_N

NOTE: AGERE'S RECOMMENDATION FOR UNUSED PORTS

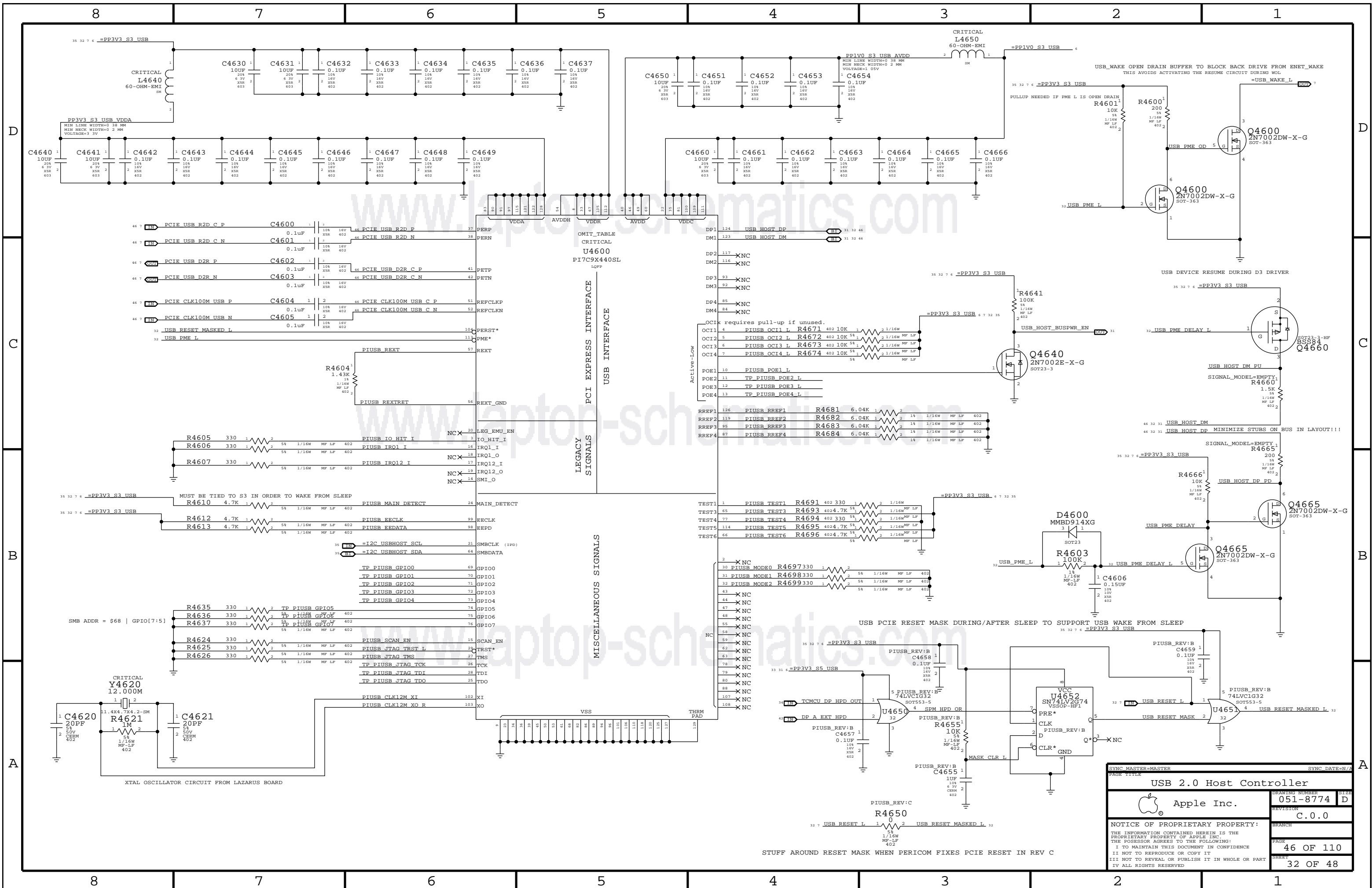
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PAGE TITLE <b>FireWire: 1394B MISC</b>			
DRAWING NUMBER 051-8774		SIZE D	
REVISION C.0.0		BRANCH	
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PAGE TITLE		SYNC DATE=09/23/2010	
<b>FIREWIRE CONNECTOR</b>			
	DRAWING NUMBER		SIZE
	051-8774		D
REVISION			BRANCH
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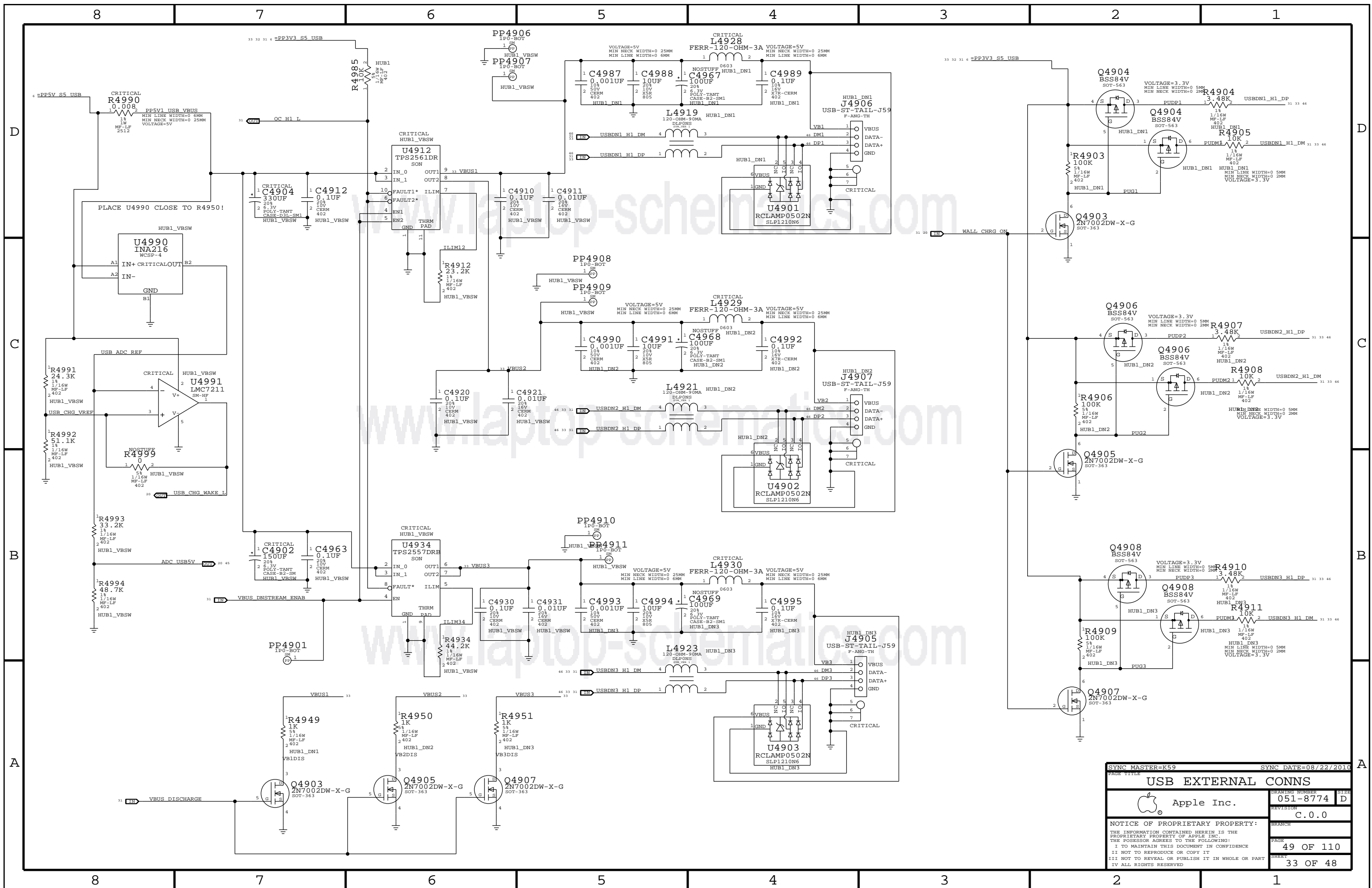


PAGE TITLE		SYNC DATE=11/01/2010	
<b>USB 7-PORT HUB</b>			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8774	D
		REVISION	
		C.0.0	
		BRANCH	
		PAGE	45 OF 110
		SHEET	31 OF 48
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<b>USB 2.0 Host Controller</b>			
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		PAGE	46 OF 110
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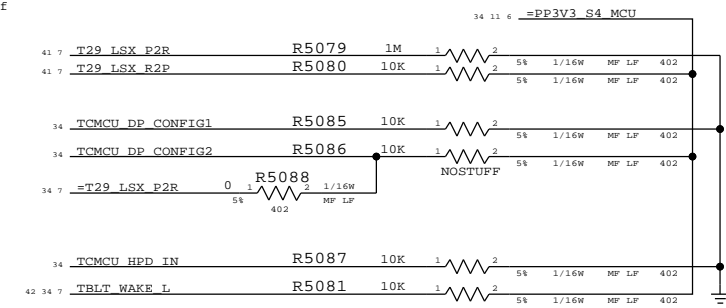
STUFF AROUND RESET MASK WHEN PERICOM FIXES PCIE RESET IN REV C



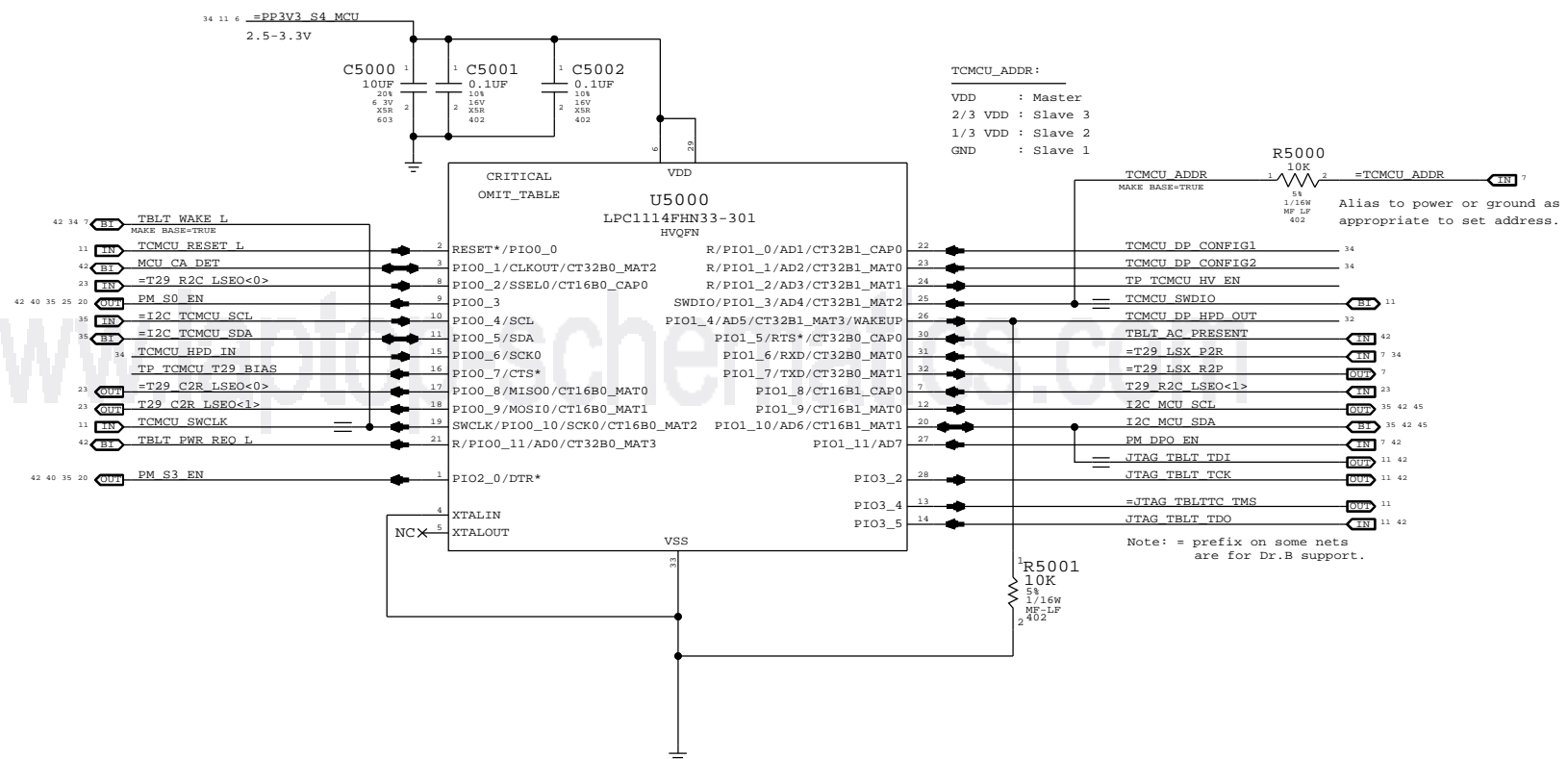
SYNC MASTER=K59		SYNC DATE=08/22/2010	
<b>USB EXTERNAL CONNS</b>			
Apple Inc.		DRAWING NUMBER	051-8774
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MCU Pull-ups/downs

T29 host/device has 10K pull-up on LSX\_R2P.  
 Dual-plug cable has cross-over for P2R/R2P.  
 Device micro (U5000) senses pull-up to  
 detect host. Cable may be powered-off  
 until host pull-up is detected.  
 P2R = Plug to Receptacle  
 R2P = Receptacle to Plug



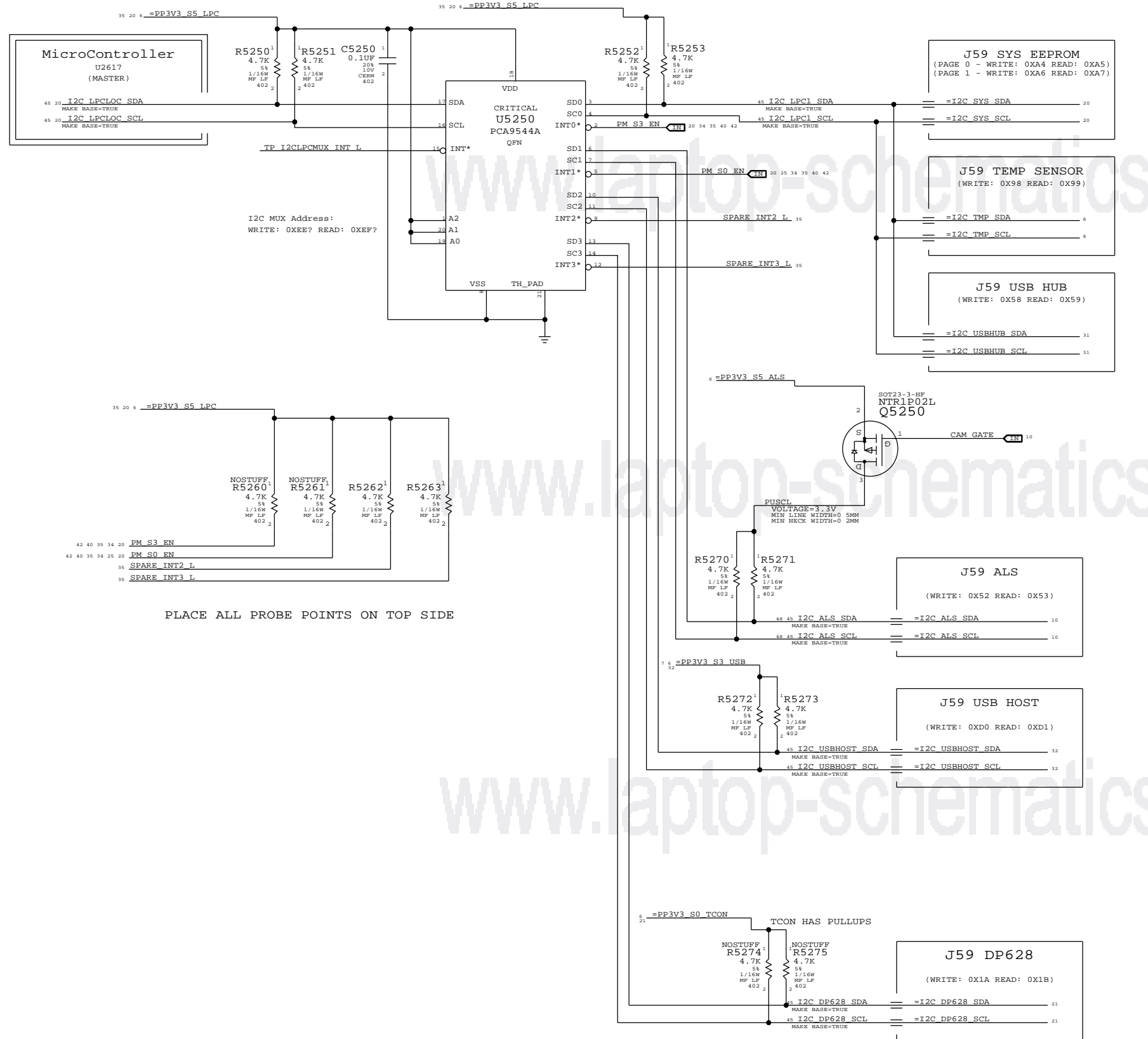
www.laptop-schematics.com



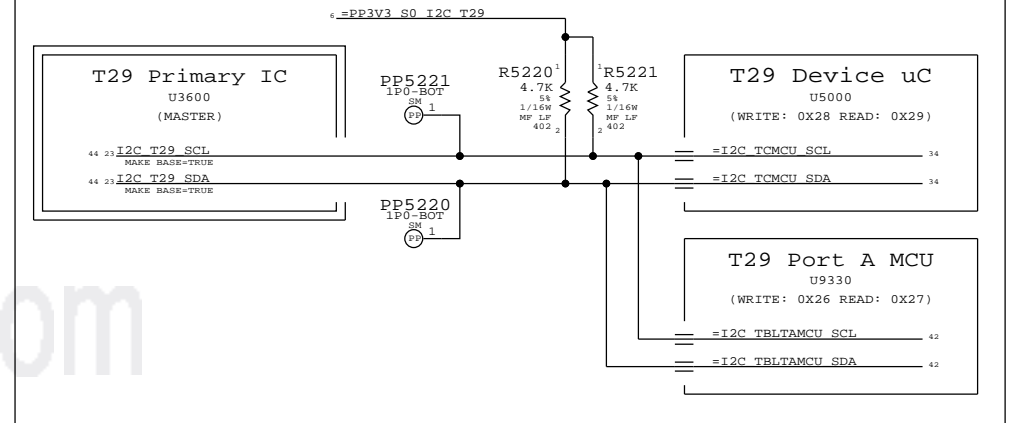
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SYNC MASTER=T29_D		SYNC DATE=03/17/2011	
Tethered Cable MCU			
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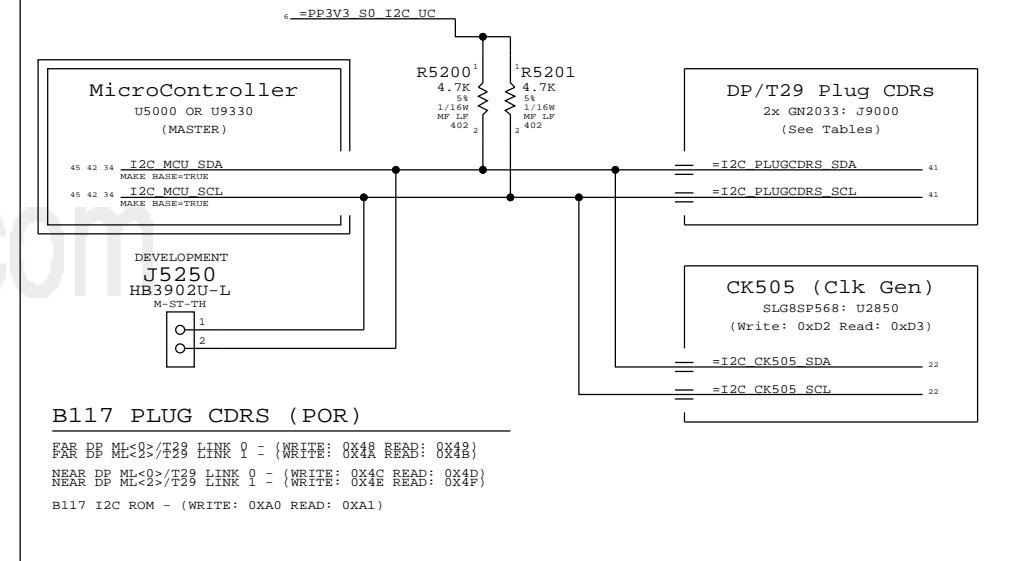
### LPC I2C CONNECTIONS



### T29 IC I2C Connections



### T29 MCU I2C CONNECTIONS

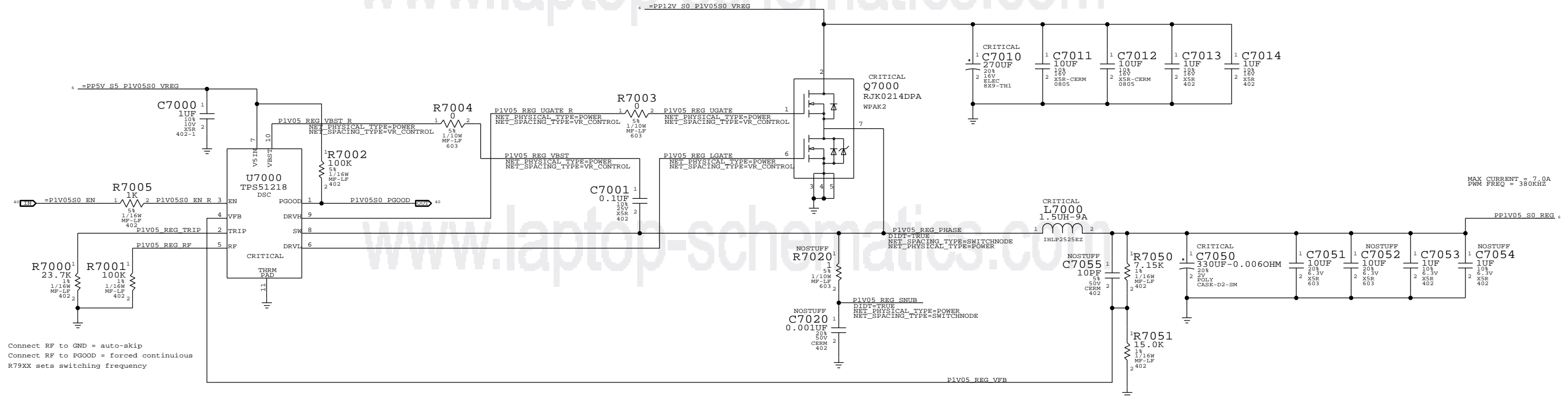


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Apple Inc.		DRAWING NUMBER: 051-8774	SIZE: D
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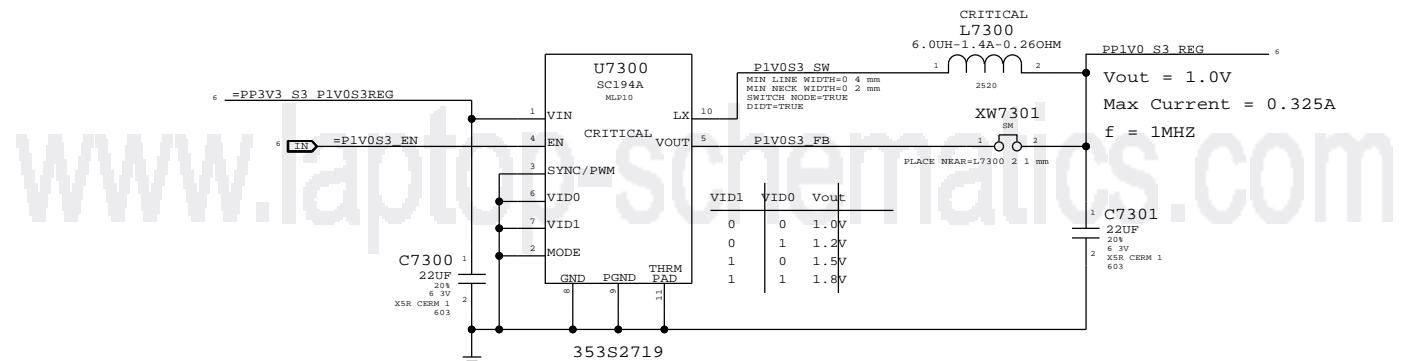


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### 1.0V Switcher



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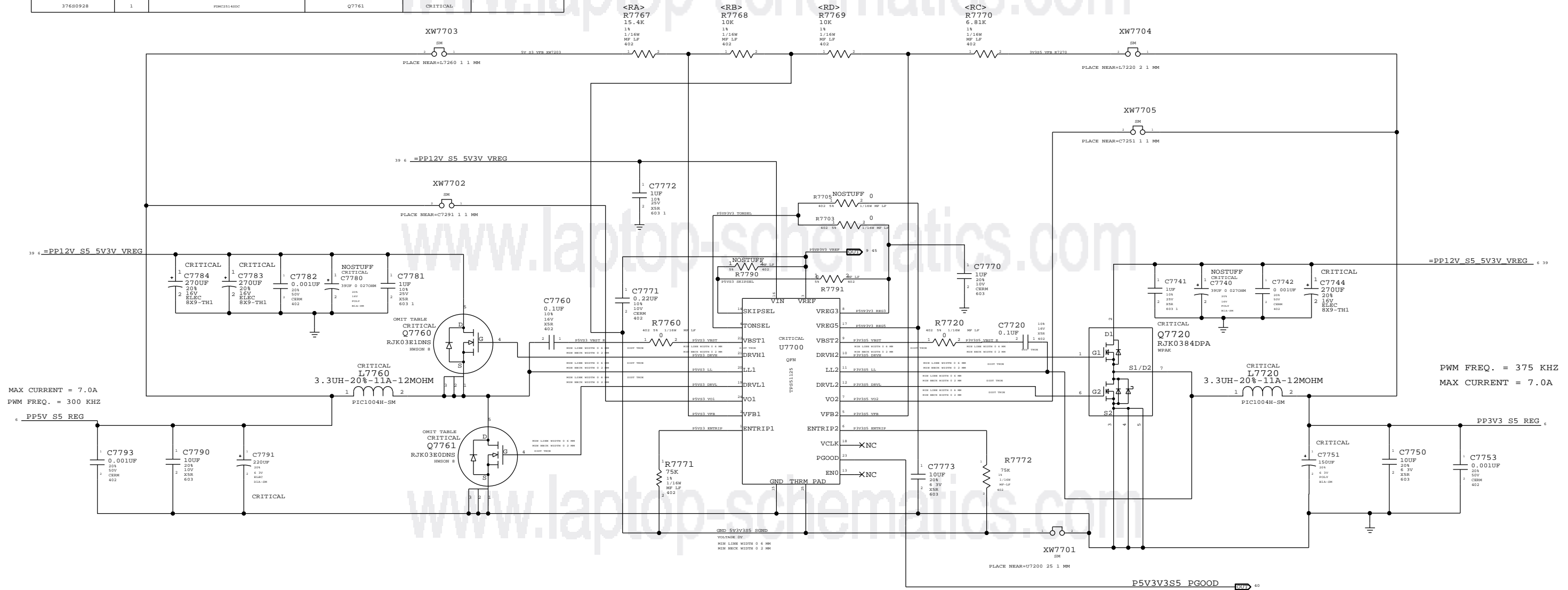
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Power: USB (1.0V S3)			
DRAWING NUMBER		SIZE	
051-8774		D	
REVISION		BRANCH	
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# 5V\_S3/3.3V\_S5 POWER SUPPLY

$$V_{OUT} = (2 * R_A / R_B) + 2$$

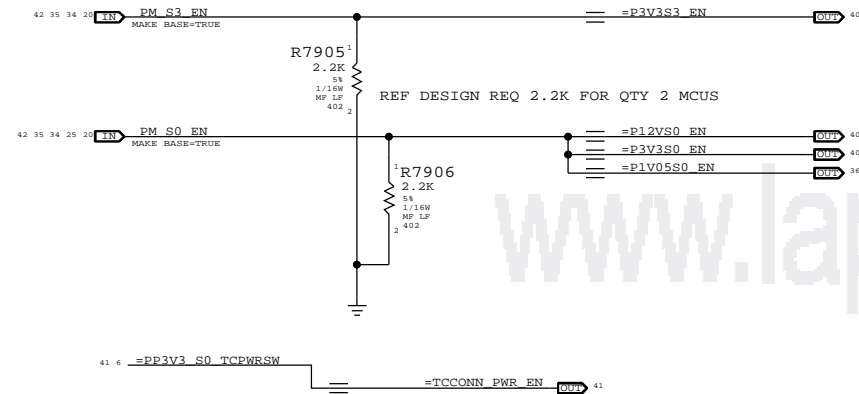
$$V_{OUT} = (2 * R_C / R_D) + 2$$

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
37680927	1	PMIC3120DC	Q7760	CRITICAL	
37680928	1	PMIC3143DC	Q7761	CRITICAL	

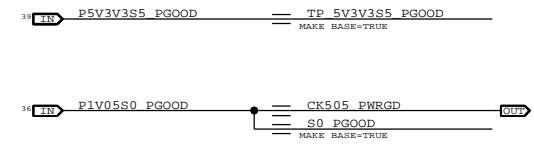


5V/3.3V SUPPLY		DRAWING NUMBER	051-8774	SIZE	D
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T29 / Device Rails



Power Goods

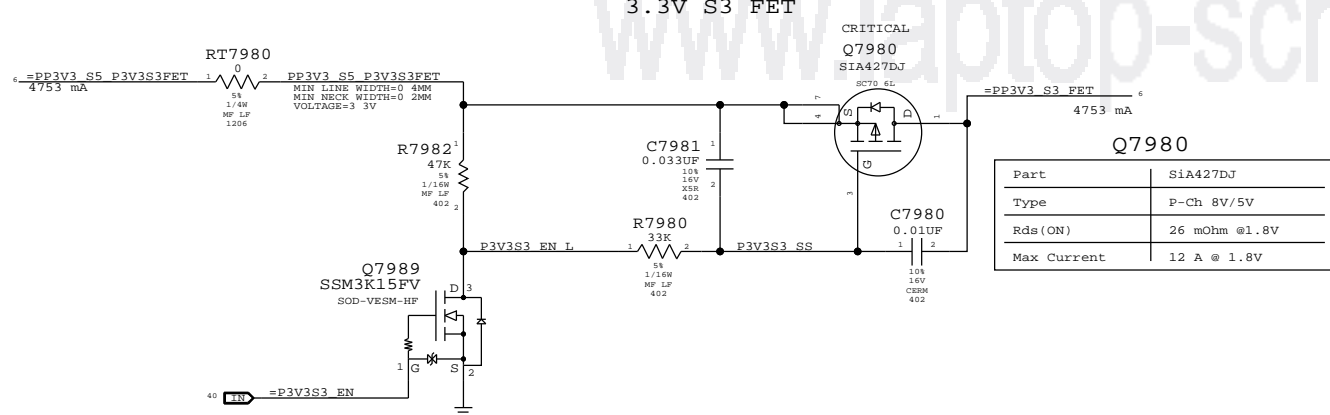


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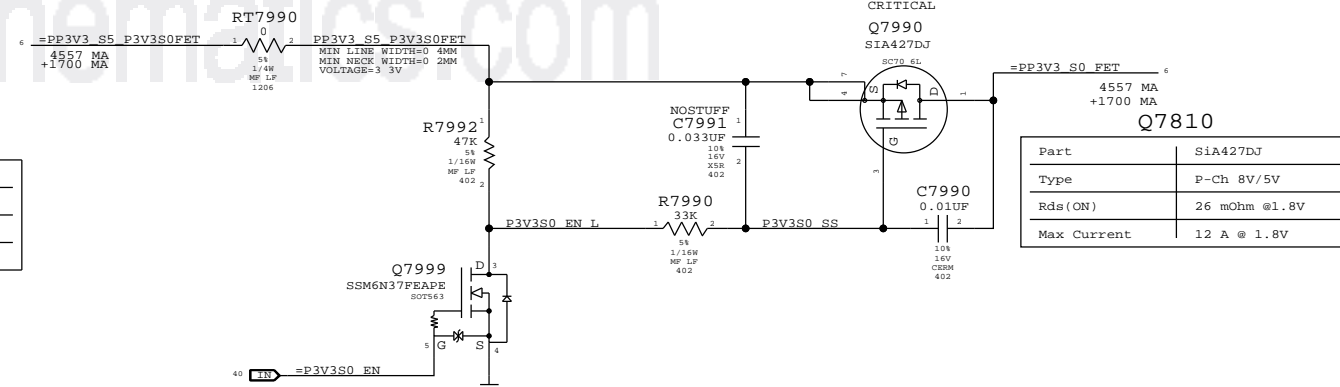
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3.3V S3 FET



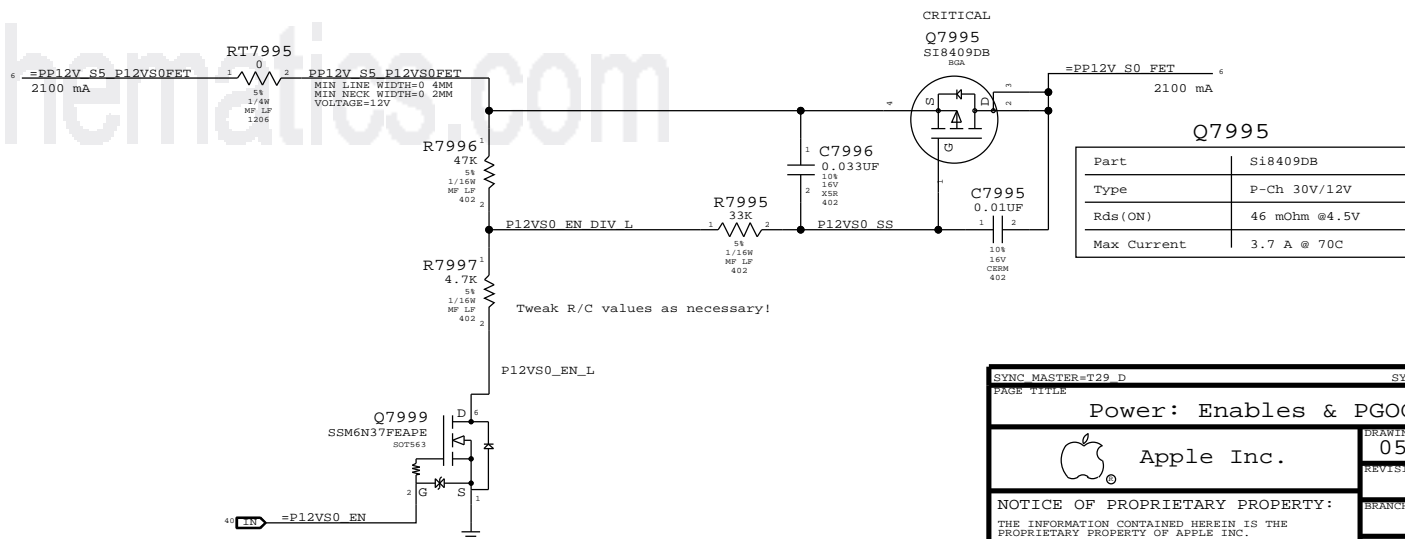
Part	SiA427DJ
Type	P-Ch 8V/5V
Rds(ON)	26 mOhm @1.8V
Max Current	12 A @ 1.8V

3.3V S0 FET



Part	SiA427DJ
Type	P-Ch 8V/5V
Rds(ON)	26 mOhm @1.8V
Max Current	12 A @ 1.8V

12V S0 FET



Part	Si8409DB
Type	P-Ch 30V/12V
Rds(ON)	46 mOhm @4.5V
Max Current	3.7 A @ 70C

SYNC MASTER=T29\_D SYNC DATE=09/30/2011

Power: Enables & PGOODS

Apple Inc.

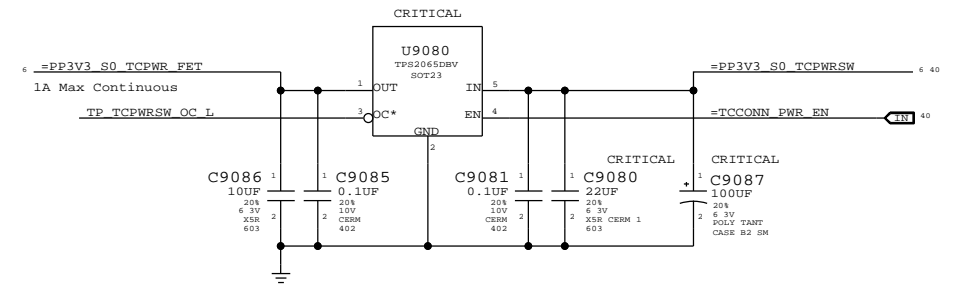
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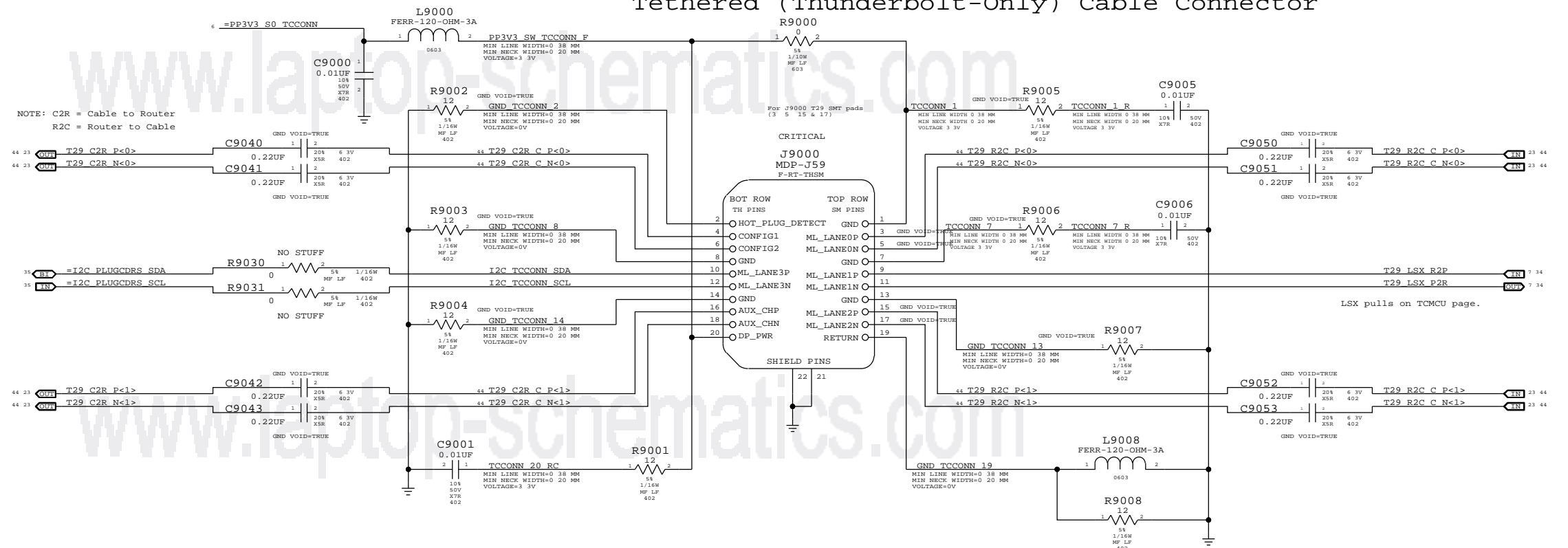
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### Cable 3.3V Power Switch

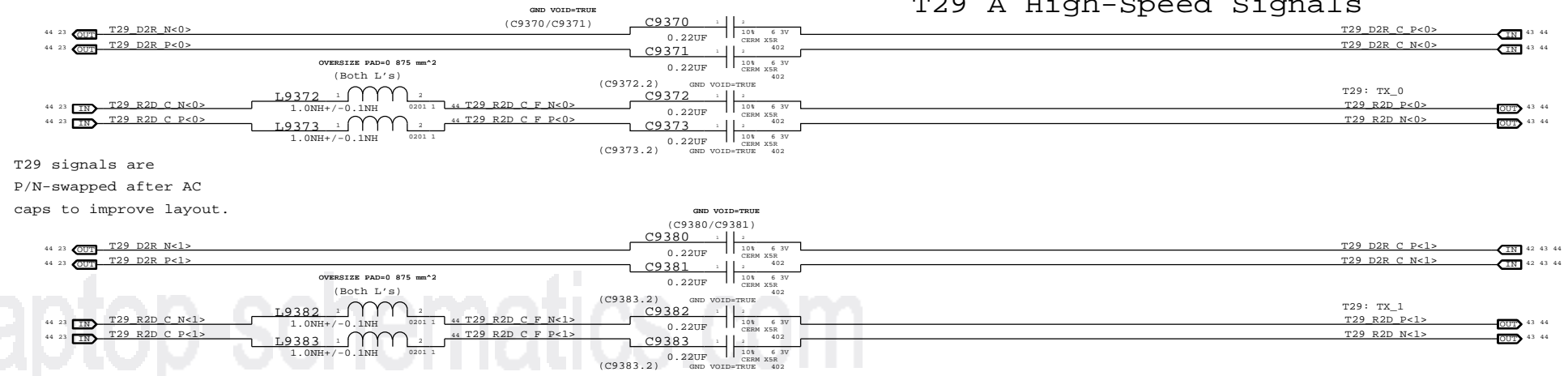


### Tethered (Thunderbolt-Only) Cable Connector

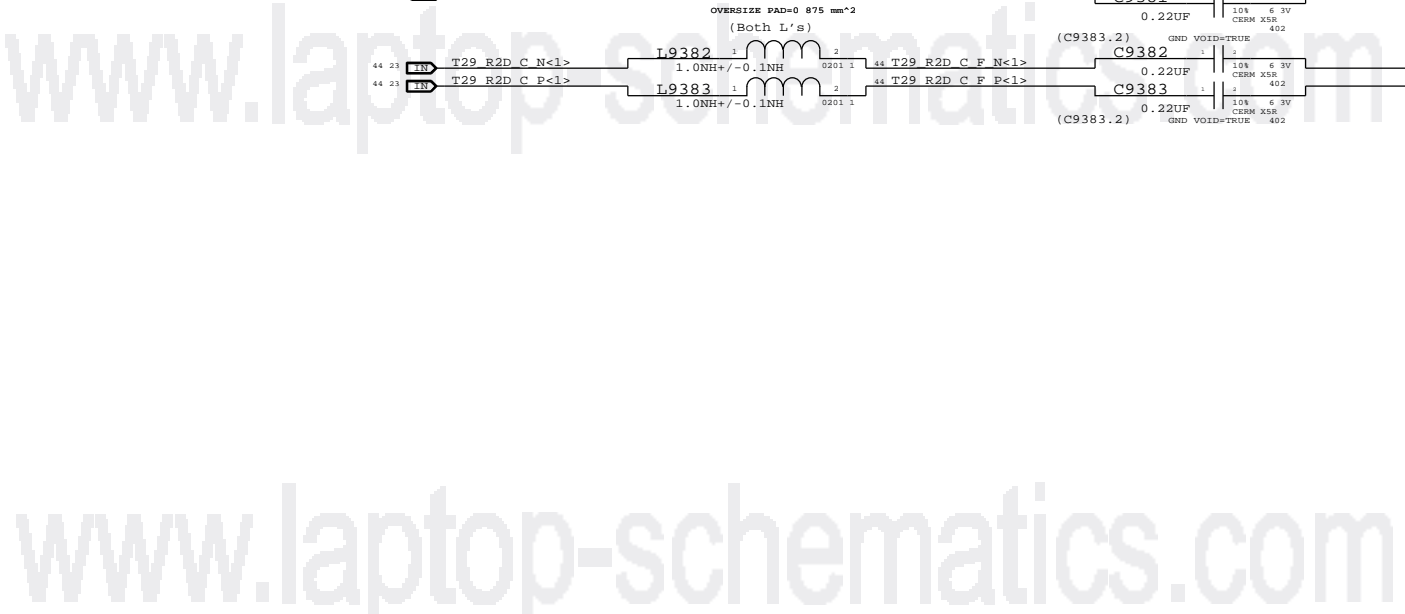


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Tethered Cable Connector			
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		PAGE	90 OF 110
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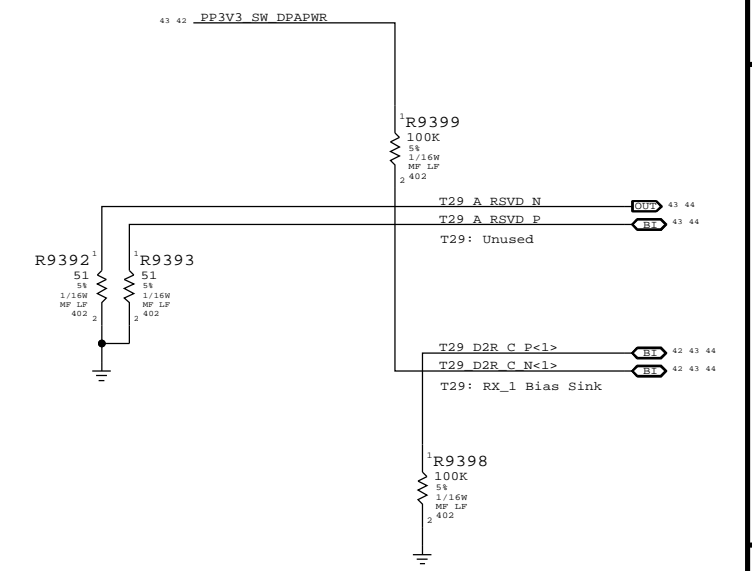
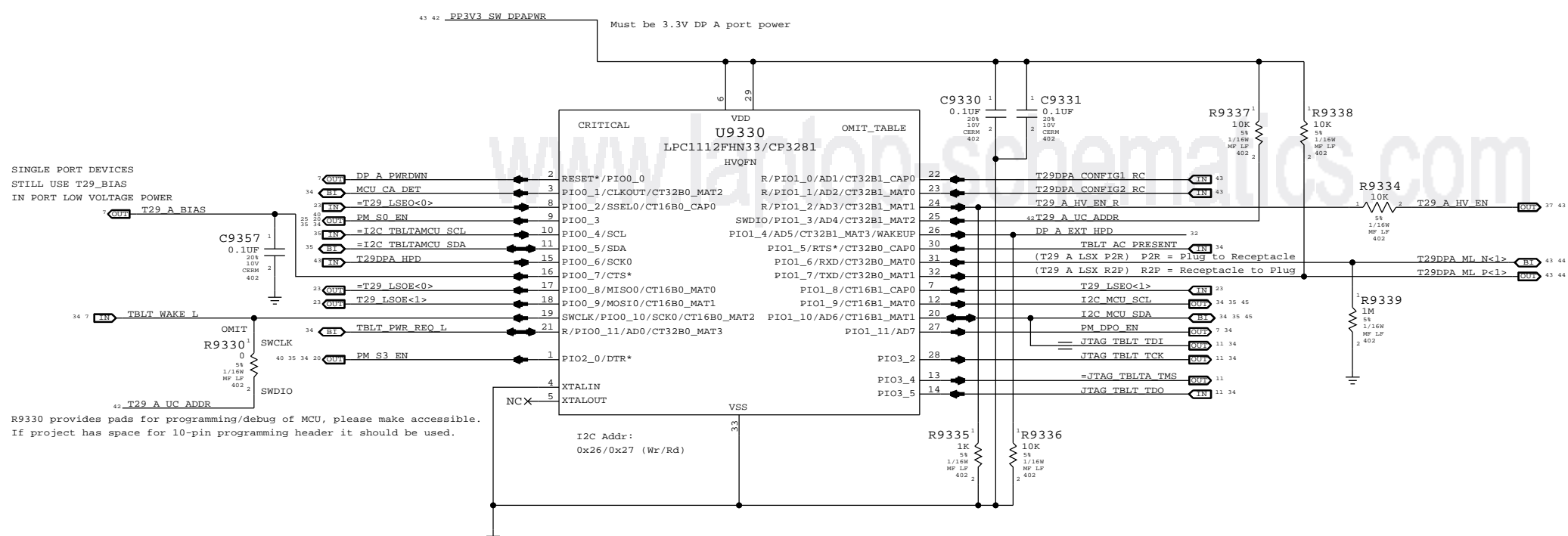
# T29 A High-Speed Signals



T29 signals are P/N-swapped after AC caps to improve layout.



## Port A MCU



SYNC MASTER=T29 D		SYNC DATE=11/01/2011	
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T29 A PORT MICROCONTROLLER		DRAWING NUMBER	051-8774
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### 3.3V/HV Power MUX

### Port A 3.3V Power Switch

### Port A HV Power Switch

	Nominal	Min	Max
IFLT	2A	1.8A	2.2A
ILIM	829mA	687mA	971mA (*)
TFLT	18.3ms	13.4ms	26.7ms
TSD	470ms	235ms	724ms

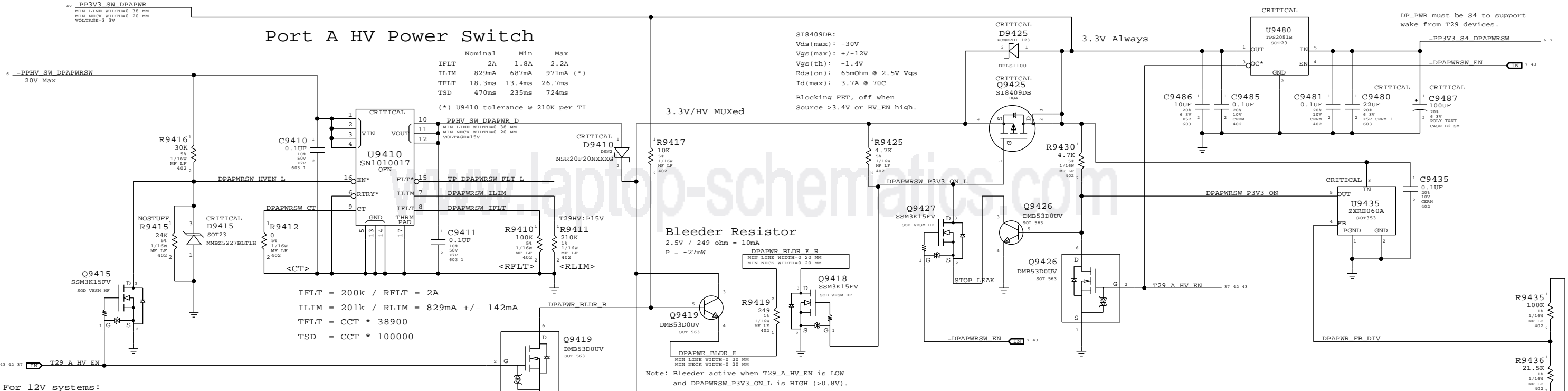
(\*) U9410 tolerance @ 210k per TI

SI8409DB:  
 Vds(max): -30V  
 Vgs(max): +/-12V  
 Vgs(th): -1.4V  
 Rds(on): 65mOhm @ 2.5V Vgs  
 Id(max): 3.7A @ 70C  
 Blocking FET, off when Source >3.4V or HV\_EN high.

3.3V/HV MUXed

**Bleeder Resistor**  
 2.5V / 249 ohm = 10mA  
 P = ~27mW

Note: Bleeder active when T29\_A\_HV\_EN is LOW and DPAPRSW\_P3V3\_ON\_L is HIGH (>0.8V).

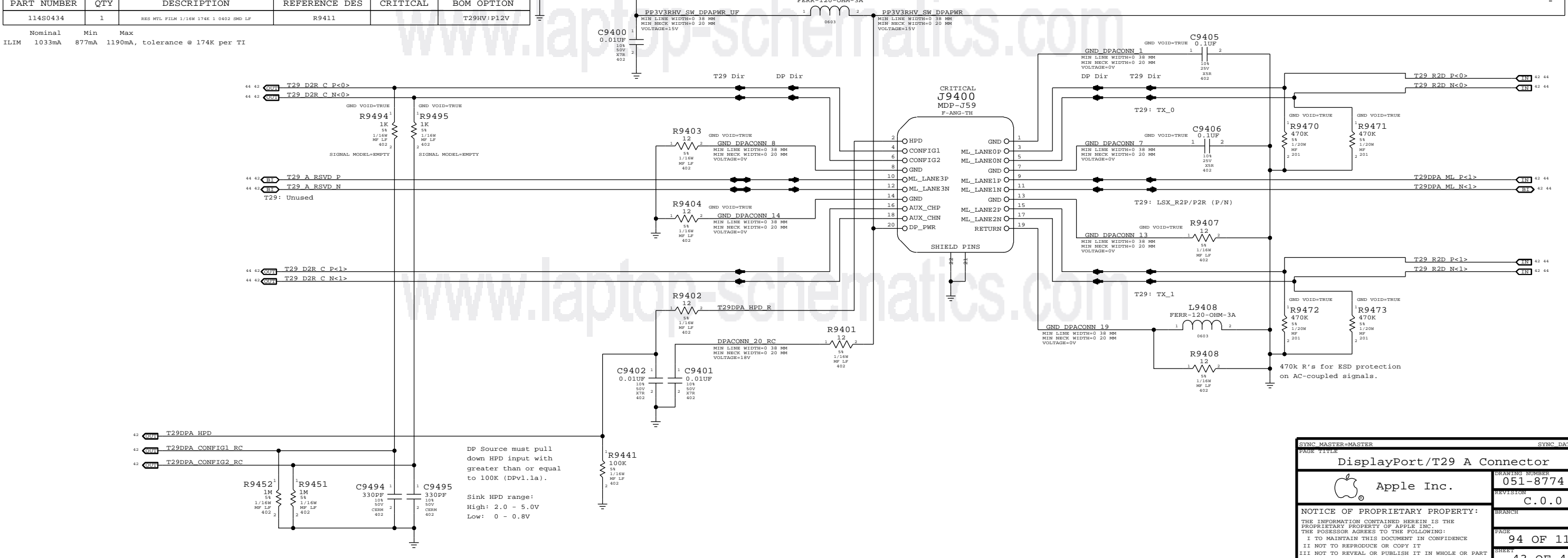


For 12V systems:  
 ILIM = 201k / RLIM = 1033mA +/- 156mA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11450434	1	RES MTL FILM 1/16W 174K 1 0402 GND LP	R9411		T29HV:P12V

Nominal Min Max  
 ILIM 1033mA 877mA 1190mA, tolerance @ 174K per TI

### DisplayPort/T29 A Connector



DP Source must pull down HPD input with greater than or equal to 100k (DPv1.1a).  
 Sink HPD range:  
 High: 2.0 - 5.0V  
 Low: 0 - 0.8V

SYNC MASTER=MASTER		SYNC DATE=N/A	
PAGE TITLE			
<b>DisplayPort/T29 A Connector</b>			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8774	D
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PCI-Express Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE 85D	*	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF
PCIEG2 85D	*	N	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF
PCIEG2 85D	TOP BOTTOM	Y	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF
CLK PCIE 90D	*	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X DIELECTRIC	?	PCIE	TOP BOTTOM	=4X DIELECTRIC	?
PCIEG2	*	=3X DIELECTRIC	?	PCIEG2	TOP BOTTOM	=4X DIELECTRIC	?
CLK PCIE	*	20 MIL	?				

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
I2C 55SE	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	0 1MM	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
I2C	*	=2x DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29 SPI 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29 SPI	*	=2x DIELECTRIC	?

T29/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP 90D	*	N	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF
T29DP 90D	TOP BOTTOM	Y	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

DP CONNECTOR SIGNAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP 90D	*	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=4 1 SPACING	?	DISPLAYPORT	TOP BOTTOM	=4 1 SPACING	?

T29 Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE		SPACING	
	PHYSICAL	SPACING		
PCIE CLK100M T29	CLK PCIE 90D	CLK PCIE		PCIE CLK100M T29 P 23 23
PCIE CLK100M T29	CLK PCIE 90D	CLK PCIE		PCIE CLK100M T29 N 23 23
	I2C 55SE	I2C		I2C T29 SCL 23 35
	I2C 55SE	I2C		I2C T29 SDA 23 35
T29 SPI CLK	T29 SPI 55S	T29 SPI		T29 SPI CLK 23
T29 SPI MOSI	T29 SPI 55S	T29 SPI		T29 SPI MOSI 23
T29 SPI MISO	T29 SPI 55S	T29 SPI		T29 SPI MISO 23
T29 SPI CS L	T29 SPI 55S	T29 SPI		T29 SPI CS L 23
	T29DP 90D	T29DP		T29 R2D C P<3..0> 23 42
	T29DP 90D	T29DP		T29 R2D C N<3..0> 23 42
	T29DP 90D	T29DP		T29 D2R P<3..0> 23 42
	T29DP 90D	T29DP		T29 D2R N<3..0> 23 42
	T29DP 90D	T29DP		T29 R2D P<0> 42 43
	T29DP 90D	T29DP		T29 R2D N<0> 42 43
	T29DP 90D	T29DP		T29 R2D P<1> 42 43
	T29DP 90D	T29DP		T29 R2D N<1> 42 43
	T29DP 90D	T29DP		T29 R2D C F P<1..0> 42
	T29DP 90D	T29DP		T29 R2D C F N<1..0> 42
	T29DP 90D	T29DP		T29 D2R C P<0> 42 43
	T29DP 90D	T29DP		T29 D2R C N<0> 42 43
	T29DP 90D	T29DP		T29 D2R C P<1> 42 43
	T29DP 90D	T29DP		T29 D2R C N<1> 42 43
	DP 90D	DISPLAYPORT		T29DPA ML P<1> 42 43
	DP 90D	DISPLAYPORT		T29DPA ML N<1> 42 43
	USB2 90D	USB2		T29 A RSVD P 42 43
	USB2 90D	USB2		T29 A RSVD N 42 43
	T29DP 90D	T29DP		T29 R2C P<1..0> 41
	T29DP 90D	T29DP		T29 R2C N<1..0> 41
	T29DP 90D	T29DP		T29 R2C C P<0> 23 41
	T29DP 90D	T29DP		T29 R2C C N<0> 23 41
	T29DP 90D	T29DP		T29 R2C C P<1> 23 41
	T29DP 90D	T29DP		T29 R2C C N<1> 23 41
	T29DP 90D	T29DP		T29 C2R P<0> 23 41
	T29DP 90D	T29DP		T29 C2R N<0> 23 41
	T29DP 90D	T29DP		T29 C2R P<1> 23 41
	T29DP 90D	T29DP		T29 C2R N<1> 23 41
	T29DP 90D	T29DP		T29 C2R C P<1..0> 41
	T29DP 90D	T29DP		T29 C2R C N<1..0> 41

T29 DP AND DOWNSTREAM PORTS  
T29/DP TETHERED CABLE

INTERNAL PANEL PROPERTIES

ELECTRICAL CONSTRAINT SET	NET TYPE		SPACING	
	PHYSICAL	SPACING		
DP 90D	DISPLAYPORT			DP INT ML C P<3..0> 7
DP 90D	DISPLAYPORT			DP INT ML C N<3..0> 7
DP INT ML	DP 90D	DISPLAYPORT		DP INT ML P<3..0> 7 21 48
DP INT ML	DP 90D	DISPLAYPORT		DP INT ML N<3..0> 7 21 48
DP INT ML	DP 90D	DISPLAYPORT		DP INT AUXCH C P 7
DP INT ML	DP 90D	DISPLAYPORT		DP INT AUXCH C N 7
DP INT AUXCH	DP 90D	DISPLAYPORT		DP INT AUXCH P 7 21 48
DP INT AUXCH	DP 90D	DISPLAYPORT		DP INT AUXCH N 7 21 48

SYNC MASTER=TONY SYNC DATE=11/17/2011

PAGE TITLE

**CONSTRAINTS: T29**

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Temp Sensor Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
TMPSENS PAIR	*	55 OHM SE	=55 OHM SE	=55 OHM SE	20MM	0.25MM	0.10MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
TMPSENS	*	=2x DIELECTRIC	?

Temp Sensor Net Properties

ELECTRICAL CONSTRAINT SET	PHYSICAL	NET TYPE	SPACING
ESD	TEMPSENS PAIR	TEMPSENS	DX1 P
ESD	TEMPSENS PAIR	TEMPSENS	DX1 N
ESD	TEMPSENS PAIR	TEMPSENS	TDX1 P
ESD	TEMPSENS PAIR	TEMPSENS	TDX1 N
ESD	TEMPSENS PAIR	TEMPSENS	DX2 P
ESD	TEMPSENS PAIR	TEMPSENS	DX2 N
ESD	TEMPSENS PAIR	TEMPSENS	TDX2 P
ESD	TEMPSENS PAIR	TEMPSENS	TDX2 N

Temp sensor routes

AUDIO CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
AUDIODIFF	*	Y	0.6 MM	0.2 MM	10 MM	0.2 MM	0.2 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
AUDIO	*	0.2 MM	?

AUDIO NET PROPERTIES

ELECTRICAL CONSTRAINT SET	PHYSICAL	NET TYPE	SPACING
ESD	AUDIODIFF	AUDIO	AUD_LTWT N
ESD	AUDIODIFF	AUDIO	AUD_LTWT P
ESD	AUDIODIFF	AUDIO	AUD_LMFR N
ESD	AUDIODIFF	AUDIO	AUD_LMFR P
ESD	AUDIODIFF	AUDIO	AUD_RTWT N
ESD	AUDIODIFF	AUDIO	AUD_RTWT P
ESD	AUDIODIFF	AUDIO	AUD_RMFR N
ESD	AUDIODIFF	AUDIO	AUD_RMFR P
ESD	AUDIODIFF	AUDIO	AUD_SUB N
ESD	AUDIODIFF	AUDIO	AUD_SUB P

SPEAKER NET PROPERTIES

ELECTRICAL CONSTRAINT SET	PHYSICAL	NET TYPE	SPACING
ESD	AUDIODIFF	AUDIO	SPKRAMP_LTWT_OUT N
ESD	AUDIODIFF	AUDIO	SPKRAMP_LTWT_OUT P
ESD	AUDIODIFF	AUDIO	SPKRAMP_LMFR_OUT N
ESD	AUDIODIFF	AUDIO	SPKRAMP_LMFR_OUT P
ESD	AUDIODIFF	AUDIO	SPKRAMP_RTWT_OUT N
ESD	AUDIODIFF	AUDIO	SPKRAMP_RTWT_OUT P
ESD	AUDIODIFF	AUDIO	SPKRAMP_RMFR_OUT N
ESD	AUDIODIFF	AUDIO	SPKRAMP_RMFR_OUT P
ESD	AUDIODIFF	AUDIO	SPKRAMP_SUB_OUT N
ESD	AUDIODIFF	AUDIO	SPKRAMP_SUB_OUT P

I2C Net Properties

ELECTRICAL CONSTRAINT SET	PHYSICAL	NET TYPE	SPACING
ESD	I2C 550K	I2C	I2C LPCREEM_SDA
ESD	I2C 550K	I2C	I2C LPCREEM_SCL
ESD	I2C 550K	I2C	DDC_SDA_FC
ESD	I2C 550K	I2C	DDC_SCL_FC
ESD	I2C 550K	I2C	SDA_FC
ESD	I2C 550K	I2C	SCL_FC
ESD	I2C 550K	I2C	SDA_SWREM
ESD	I2C 550K	I2C	SCL_SWREM
ESD	I2C 550K	I2C	I2C DP628_SDA
ESD	I2C 550K	I2C	I2C DP628_SCL
ESD	I2C 550K	I2C	I2C LPCLOC_SDA
ESD	I2C 550K	I2C	I2C LPCLOC_SCL
ESD	I2C 550K	I2C	I2C FALS_SDA
ESD	I2C 550K	I2C	I2C FALS_SCL
ESD	I2C 550K	I2C	I2C LPC1_SDA
ESD	I2C 550K	I2C	I2C LPC1_SCL
ESD	I2C 550K	I2C	I2C ALS_SCL
ESD	I2C 550K	I2C	I2C ALS_SDA
ESD	I2C 550K	I2C	I2C USBHOST_SCL
ESD	I2C 550K	I2C	I2C USBHOST_SDA

I2C pairs from LPC

ELECTRICAL CONSTRAINT SET	PHYSICAL	NET TYPE	SPACING
ESD	I2C 550K	I2C	ADAV4601_I2C_SDA
ESD	I2C 550K	I2C	ADAV4601_I2C_SCL
ESD	I2C 550K	I2C	I2C_SDA
ESD	I2C 550K	I2C	I2C_SCL
ESD	I2C 550K	I2C	AUD_161_I2C_SDA
ESD	I2C 550K	I2C	AUD_161_I2C_SCL
ESD	I2C 550K	I2C	I2C MCU_SCL
ESD	I2C 550K	I2C	I2C MCU_SDA

Audio I2C pairs

MicroCtrl Net Properties

ELECTRICAL CONSTRAINT SET	PHYSICAL	NET TYPE	SPACING
ESD	MICROCTRL 550K	MICROCTRL	ADC_STR0_V
ESD	MICROCTRL 550K	MICROCTRL	ADC_STR1_V
ESD	MICROCTRL 550K	MICROCTRL	ADC_STR2_V
ESD	MICROCTRL 550K	MICROCTRL	DAC_OUT
ESD	MICROCTRL 550K	MICROCTRL	ADC_USB5V
ESD	MICROCTRL 550K	MICROCTRL	P5VP3V3_VREF

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Ethernet MDI Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET MDI 100D	*	100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001\_v01), Section 2.7.4

PCie Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE			
	PHYSICAL	SPACING		
ENET	PCIE 85d	PCIE	PCIE ENET R2D P	26
ENET	PCIE 85d	PCIE	PCIE ENET R2D N	26
ENET	PCIE ENET R2D	PCIE	PCIE ENET R2D C P	7 26
ENET	PCIE ENET R2D	PCIE	PCIE ENET R2D C N	7 26
ENET	PCIE ENET D2R	PCIE	PCIE ENET D2R P	7 26
ENET	PCIE ENET D2R	PCIE	PCIE ENET D2R N	7 26
ENET	PCIE ENET D2R	PCIE	PCIE ENET D2R C P	26
ENET	PCIE ENET D2R	PCIE	PCIE ENET D2R C N	26
ENET	PCIE CLK100M ENET	CLK PCIE 80d	PCIE CLK100M ENET P	22 26
ENET	PCIE CLK100M ENET	CLK PCIE 80d	PCIE CLK100M ENET N	22 26

Ethernet MDI Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE			
	PHYSICAL	SPACING		
ENET MDI	ENET MDI 100d	ENET MDI	ENETCONN MDI P<3..0>	26 27
ENET MDI	ENET MDI 100d	ENET MDI	ENETCONN MDI N<3..0>	26 27
ENET MDI	ENET MDI 100d	ENET MDI	ENETCONN MDI T P<3..0>	27
ENET MDI	ENET MDI 100d	ENET MDI	ENETCONN MDI T N<3..0>	27

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW 110D	*	110 OHM DIFF	=110 OHM DIFF	=110 OHM DIFF	=110 OHM DIFF	=110 OHM DIFF	=110 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW TP	*	=3 1 SPACING	?

FIREWIRE PCIE NET PROPERTIES

ELECTRICAL CONSTRAINT SET	NET TYPE			
	PHYSICAL	SPACING		
FW R2D TPA	PCIE 85d	PCIE	PCIE FW R2D P	28
FW R2D TPA	PCIE 85d	PCIE	PCIE FW R2D N	28
FW R2D TPA	PCIE 85d	PCIE	PCIE FW R2D C P	7 28
FW R2D TPA	PCIE 85d	PCIE	PCIE FW R2D C N	7 28
FW R2D TPB	PCIE 85d	PCIE	PCIE FW D2R P	7 28
FW R2D TPB	PCIE 85d	PCIE	PCIE FW D2R N	7 28
FW R2D TPB	PCIE 85d	PCIE	PCIE FW D2R C P	28
FW R2D TPB	PCIE 85d	PCIE	PCIE FW D2R C N	28
FW CLK100M	CLK PCIE 80d	CLK PCIE	PCIE CLK100M FW P	22 28
FW CLK100M	CLK PCIE 80d	CLK PCIE	PCIE CLK100M FW N	22 28

FireWire Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE			
	PHYSICAL	SPACING		
FW R2D TPA	FW 110d	FW TP	FW PORT0 TPA P	29 30
FW R2D TPA	FW 110d	FW TP	FW PORT0 TPA N	29 30
FW R2D TPB	FW 110d	FW TP	FW PORT0 TPB P	29 30
FW R2D TPB	FW 110d	FW TP	FW PORT0 TPB N	29 30

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB2 90D	*	90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2	*	=4 1 SPACING	?

USB PCIE NET PROPERTIES

ELECTRICAL CONSTRAINT SET	NET TYPE			
	PHYSICAL	SPACING		
USB D2R C P	PCIE92 85d	PCIE92	PCIE USB D2R C P	32
USB D2R C N	PCIE92 85d	PCIE92	PCIE USB D2R C N	32
USB R2D P	PCIE92 85d	PCIE92	PCIE USB R2D P	32
USB R2D N	PCIE92 85d	PCIE92	PCIE USB R2D N	32
USB R2D C P	PCIE92 85d	PCIE92	PCIE USB R2D C P	7 32
USB R2D C N	PCIE92 85d	PCIE92	PCIE USB R2D C N	7 32
USB D2R P	PCIE92 85d	PCIE92	PCIE USB D2R P	7 32
USB D2R N	PCIE92 85d	PCIE92	PCIE USB D2R N	7 32
CLK100M USB P	CLK PCIE 80d	CLK PCIE	PCIE CLK100M USB P	7 32
CLK100M USB N	CLK PCIE 80d	CLK PCIE	PCIE CLK100M USB N	7 32
CLK100M USB C P	CLK PCIE 80d	CLK PCIE	PCIE CLK100M USB C P	32
CLK100M USB C N	CLK PCIE 80d	CLK PCIE	PCIE CLK100M USB C N	32

USB Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE			
	PHYSICAL	SPACING		
USB2 90d	USB2	USB2	USB HUB UP DP	31
USB2 90d	USB2	USB2	USB HUB UP DM	31
USB2 90d	USB2	USB2	USB DEV DP	31
USB2 90d	USB2	USB2	USB DEV DM	31
USB2 90d	USB2	USB2	USB DEV F DP	31
USB2 90d	USB2	USB2	USB DEV F DM	31
USB2 90d	USB2	USB2	USB HOST DP	31 32
USB2 90d	USB2	USB2	USB HOST DM	31 32
USB2 90d	USB2	USB2	USB D1 H1 DP	31 33
USB2 90d	USB2	USB2	USB D1 H1 DM	31 33
USB2 90d	USB2	USB2	USB D2 H1 DP	31 33
USB2 90d	USB2	USB2	USB D2 H1 DM	31 33
USB2 90d	USB2	USB2	USB D3 H1 DP	31 33
USB2 90d	USB2	USB2	USB D3 H1 DM	31 33
USB2 90d	USB2	USB2	USB UC DP	20 31
USB2 90d	USB2	USB2	USB UC DM	20 31
USB2 90d	USB2	USB2	USB AUDIO DP	11 31
USB2 90d	USB2	USB2	USB AUDIO DM	11 31
USB2 90d	USB2	USB2	USB CAMERA DP	10 31
USB2 90d	USB2	USB2	USB CAMERA DM	10 31
USB2 90d	USB2	USB2	CAM DP	10 48
USB2 90d	USB2	USB2	CAM DM	10 48
USB2 90d	USB2	USB2	AUD 161 USB DP	12
USB2 90d	USB2	USB2	AUD 161 USB DM	12
USB2 90d	USB2	USB2	DM1	33
USB2 90d	USB2	USB2	DP1	33
USB2 90d	USB2	USB2	DM2	33
USB2 90d	USB2	USB2	DP2	33
USB2 90d	USB2	USB2	DM3	33
USB2 90d	USB2	USB2	DP3	33

USB UPSTREAM

USB Hub ports

USB AUDIO

USB connector routes

D

C

B

A

D

C

B

A

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PAGE TITLE: CONSTRAINTS:ENET, FIREWIRE & USB

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T29 Dr.B-Specific Physical & Spacing Constraints

BOARD LAYERS			BOARD AREAS				BOARD UNITS (MIL. OR MM)	ALLEGRO VERSION
TOP ISL2 ISL3 ISL4 ISL5 ISL6 ISL7 BOTTOM			NO TYPE				MM	15.7
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
DEFAULT	*	Y	=55 OHM SE	=55 OHM SE	6.35 MM	0 MM	0 MM	
STANDARD	*	Y	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
55 OHM SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD	
55 OHM SE	TOP BOTTOM	Y	0.085 MM	0.085 MM				

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80 OHM DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80 OHM DIFF	ISL3 ISL6	Y	0.120 MM	0.120 MM		0.150 MM	0.150 MM
80 OHM DIFF	TOP BOTTOM	Y	0.135 MM	0.135 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85 OHM DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85 OHM DIFF	ISL3 ISL6	Y	0.115 MM	0.115 MM		0.200 MM	0.200 MM
85 OHM DIFF	TOP BOTTOM	Y	0.125 MM	0.125 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90 OHM DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90 OHM DIFF	ISL3 ISL6	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM
90 OHM DIFF	TOP BOTTOM	Y	0.099 MM	0.099 MM		0.150 MM	0.150 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100 OHM DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100 OHM DIFF	ISL3 ISL6	Y	0.081 MM	0.081 MM		0.250 MM	0.250 MM
100 OHM DIFF	TOP BOTTOM	Y	0.091 MM	0.091 MM		0.250 MM	0.250 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110 OHM DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110 OHM DIFF	ISL3 ISL6	Y	0.067 MM	0.067 MM		0.300 MM	0.300 MM
110 OHM DIFF	TOP BOTTOM	Y	0.075 MM	0.075 MM		0.300 MM	0.300 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1.1 DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

Standard Spacing Rules

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.1 SPACING	*	0.1 MM	?
2.1 SPACING	*	0.2 MM	?
3.1 SPACING	*	0.3 MM	?
4.1 SPACING	*	0.4 MM	?
5.1 SPACING	*	0.5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X DIELECTRIC	TOP BOTTOM	0.140 MM	?
3X DIELECTRIC	TOP BOTTOM	0.210 MM	?
4X DIELECTRIC	TOP BOTTOM	0.280 MM	?
5X DIELECTRIC	TOP BOTTOM	0.355 MM	?
2X DIELECTRIC	*	0.152 MM	?
3X DIELECTRIC	*	0.228 MM	?
4X DIELECTRIC	*	0.304 MM	?
5X DIELECTRIC	*	0.380 MM	?

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# FUNCTIONAL TEST POINTS

# NC AND NO\_TEST NETS

FLIP SIDE PCI BRIDGE AND USB CONTROLLER MOUNTING AND ROUTING MAKES TEST VIRTUALLY IMPOSSIBLE

## J1013 ODD FAN

8 FAN0\_PMR FUNC TEST TRUP  
 8 FAN\_TACHO FUNC TEST TRUP  
 19 PPI2V\_FAN\_FET FUNC TEST TRUP  
 MIN ALLOWED TPS=3  
 3 GROUND TESTPOINTS NEAR J1013

## J1115 BLC CONNECTOR

9 STR0\_+ FUNC TEST TRUP  
 9 STR0\_- FUNC TEST TRUP  
 9 STR0C FUNC TEST TRUP  
 9 STR1\_+ FUNC TEST TRUP  
 9 STR1\_- FUNC TEST TRUP  
 9 STR1C FUNC TEST TRUP  
 9 STR2\_+ FUNC TEST TRUP  
 9 STR2\_- FUNC TEST TRUP  
 9 STR2C FUNC TEST TRUP  
 2 GROUND TESTPOINTS NEAR J1013

## J1204 USB CAMERA

10 PREV\_CAM\_FLIT FUNC TEST TRUP  
 MIN ALLOWED TPS=1  
 46 CAM\_DM FUNC TEST TRUP  
 46 CAM\_DP FUNC TEST TRUP  
 45 I2C\_ALS\_SCL FUNC TEST TRUP  
 45 I2C\_ALS\_SDA FUNC TEST TRUP  
 4 GROUND TESTPOINTS NEAR J1204

## J2007 MICROPHONE

18 AUD\_MIC\_IN\_N\_CONN FUNC TEST TRUP  
 18 GND\_AUD\_MIC\_CONN FUNC TEST TRUP  
 18 AUD\_MIC\_IN\_P\_CONN FUNC TEST TRUP  
 2 GROUND TESTPOINTS NEAR J2007

## J2003 AUDIO LEFT SPEAKER

45 SPKRAMP\_LWFR\_OUT\_P FUNC TEST TRUP  
 45 SPKRAMP\_LWFR\_OUT\_N FUNC TEST TRUP  
 45 SPKRAMP\_LTWI\_OUT\_P FUNC TEST TRUP  
 45 SPKRAMP\_LTWI\_OUT\_N FUNC TEST TRUP

## J2004 AUDIO RIGHT SPEAKER

45 SPKRAMP\_RWFR\_OUT\_P FUNC TEST TRUP  
 45 SPKRAMP\_RWFR\_OUT\_N FUNC TEST TRUP  
 45 SPKRAMP\_RTWI\_OUT\_P FUNC TEST TRUP  
 45 SPKRAMP\_RTWI\_OUT\_N FUNC TEST TRUP

## J2005 AUDIO SUBWOOFER

45 SPKRAMP\_SUB\_OUT\_P FUNC TEST TRUP  
 45 SPKRAMP\_SUB\_OUT\_N FUNC TEST TRUP  
 18 17 16 15 GND\_AUDIO\_SPKRAMP FUNC TEST TRUP  
 MIN ALLOWED TPS=6

## J1011 BLOWER TEMP SENSOR

45 TDX1\_N FUNC TEST TRUP  
 45 TDX1\_P FUNC TEST TRUP  
 2 GROUND TESTPOINTS NEAR J1011

## J1012 PSU TEMP SENSOR

45 TDX2\_N FUNC TEST TRUP  
 45 TDX2\_P FUNC TEST TRUP  
 2 GROUND TESTPOINTS NEAR J1012

## J2726 PANEL POWER

21 PPI2V\_PANEL\_FC FUNC TEST TRUP  
 MIN ALLOWED TPS=4  
 4 GROUND TESTPOINTS NEAR J2726

## J2725 INTERNAL DP PANEL


44 DP\_INT\_ML\_P<3..0> FUNC TEST TRUP  
 44 DP\_INT\_ML\_N<3..0> FUNC TEST TRUP  
 44 DP\_INT\_AUXCH\_P FUNC TEST TRUP  
 44 DP\_INT\_AUXCH\_N FUNC TEST TRUP  
 45 DDC\_SCL\_FC FUNC TEST TRUP  
 45 DDC\_SDA\_FC FUNC TEST TRUP  
 45 SCL\_FC FUNC TEST TRUP  
 45 SDA\_FC FUNC TEST TRUP  
 21 AUDIO\_ON\_FC FUNC TEST TRUP  
 21 AUDIO\_MUTE\_FC\_L FUNC TEST TRUP  
 21 I2S\_SCLK\_FC FUNC TEST TRUP  
 21 I2S\_WS\_FC FUNC TEST TRUP  
 21 I2S\_SDO\_FC FUNC TEST TRUP  
 21 DP\_PWR\_UP\_FC FUNC TEST TRUP  
 21 INT\_FC\_L FUNC TEST TRUP  
 21 DP\_INT\_HPD\_FC FUNC TEST TRUP  
 21 VIDEO\_ON\_FC FUNC TEST TRUP  
 21 VSYNC\_FC FUNC TEST TRUP  
 17 GROUND TESTPOINTS NEAR J2725

GND 26 TESTS FUNC TEST TRUP  
 MIN ALLOWED TPS=6

TP\_PCIBR\_WAKE\_L == NC\_PCIBR\_WAKE\_L  
 MAKE BASE=TRUE NO TEST=TRUE  
 TP\_PEX8112\_EECS\_L == NC\_PEX8112\_EECS\_L  
 MAKE BASE=TRUE NO TEST=TRUE  
 TP\_PEX8112\_EECLK == NC\_PEX8112\_EECLK  
 MAKE BASE=TRUE NO TEST=TRUE  
 TP\_PEX8112\_EERDDATA == NC\_PEX8112\_EERDDATA  
 MAKE BASE=TRUE NO TEST=TRUE  
 TP\_PEX8112\_EEWRDATA == NC\_PEX8112\_EEWRDATA  
 MAKE BASE=TRUE NO TEST=TRUE  
 TP\_PEX8112\_GPI00 == NC\_PEX8112\_GPI00  
 MAKE BASE=TRUE NO TEST=TRUE  
 TP\_PEX8112\_GPI01 == NC\_PEX8112\_GPI01  
 MAKE BASE=TRUE NO TEST=TRUE  
 TP\_PEX8112\_GPI02 == NC\_PEX8112\_GPI02  
 MAKE BASE=TRUE NO TEST=TRUE  
 TP\_PEX8112\_GPI03 == NC\_PEX8112\_GPI03  
 MAKE BASE=TRUE NO TEST=TRUE  
 TP\_PEX8112\_PWR\_OK == NC\_PEX8112\_PWR\_OK  
 MAKE BASE=TRUE NO TEST=TRUE  
 TP\_PEX8112\_BAR0ENB\_L == NC\_PEX8112\_BAR0ENB\_L  
 MAKE BASE=TRUE NO TEST=TRUE  
 TP\_PEX8112\_PCLKO62SEL\_L == NC\_PEX8112\_PCLKO62SEL\_L  
 MAKE BASE=TRUE NO TEST=TRUE  
 TP\_PEX8112\_PMEOUT\_L == NC\_PEX8112\_PMEOUT\_L  
 MAKE BASE=TRUE NO TEST=TRUE  
 TP\_PEX8112\_GNT1\_L == NC\_PEX8112\_GNT1\_L  
 MAKE BASE=TRUE NO TEST=TRUE  
 TP\_PEX8112\_GNT2\_L == NC\_PEX8112\_GNT2\_L  
 MAKE BASE=TRUE NO TEST=TRUE  
 TP\_PEX8112\_GNT3\_L == NC\_PEX8112\_GNT3\_L  
 MAKE BASE=TRUE NO TEST=TRUE  
 TP\_PEX8112\_PCLKO == NC\_PEX8112\_PCLKO  
 MAKE BASE=TRUE NO TEST=TRUE

TP\_NECUSB\_SMI\_L == NC\_NECUSB\_SMI\_L  
 MAKE BASE=TRUE NO TEST=TRUE  
 TP\_NECUSB\_PPON1 == NC\_NECUSB\_PPON1  
 MAKE BASE=TRUE NO TEST=TRUE  
 TP\_NECUSB\_PPON2 == NC\_NECUSB\_PPON2  
 MAKE BASE=TRUE NO TEST=TRUE  
 TP\_NECUSB\_PPON3 == NC\_NECUSB\_PPON3  
 MAKE BASE=TRUE NO TEST=TRUE  
 TP\_NECUSB\_SRCLK == NC\_NECUSB\_SRCLK  
 MAKE BASE=TRUE NO TEST=TRUE  
 TP\_NECUSB\_SRPDA == NC\_NECUSB\_SRPDA  
 MAKE BASE=TRUE NO TEST=TRUE  
 TP\_NECUSB\_SRMOD == NC\_NECUSB\_SRMOD  
 MAKE BASE=TRUE NO TEST=TRUE  
 TP\_NECUSB\_TESTEN == NC\_NECUSB\_TESTEN  
 MAKE BASE=TRUE NO TEST=TRUE  
 TP\_NECUSB\_TEST3 == NC\_NECUSB\_TEST3  
 MAKE BASE=TRUE NO TEST=TRUE  
 TP\_NECUSB\_TEST4 == NC\_NECUSB\_TEST4  
 MAKE BASE=TRUE NO TEST=TRUE

NO TEST=TRUE PCI\_AD<31..0>  
 NO TEST=TRUE PCI\_CBE<1..3..0>  
 NO TEST=TRUE PCI\_PAB  
 NO TEST=TRUE PCI\_FRAME\_L  
 NO TEST=TRUE PCI\_IRDY\_L  
 NO TEST=TRUE PCI\_TRDY\_L  
 NO TEST=TRUE PCI\_DEVSEL\_L  
 NO TEST=TRUE PCI\_STOP\_L  
 NO TEST=TRUE PCI\_PERR\_L  
 NO TEST=TRUE PCI\_SERR\_L  
 NO TEST=TRUE PCI\_NECUSB\_REQ\_L  
 NO TEST=TRUE PCI\_NECUSB\_GNT\_L  
 NO TEST=TRUE PCI\_NECUSB\_INT\_L  
 NO TEST=TRUE PCI\_CLKRUN\_L  
 NO TEST=TRUE PCI\_RESET\_L

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