

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.  
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.  
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
10	0001231154	ENGINEERING RELEASED		2011-09-06

## J2 MLB - DVT OK2FAB

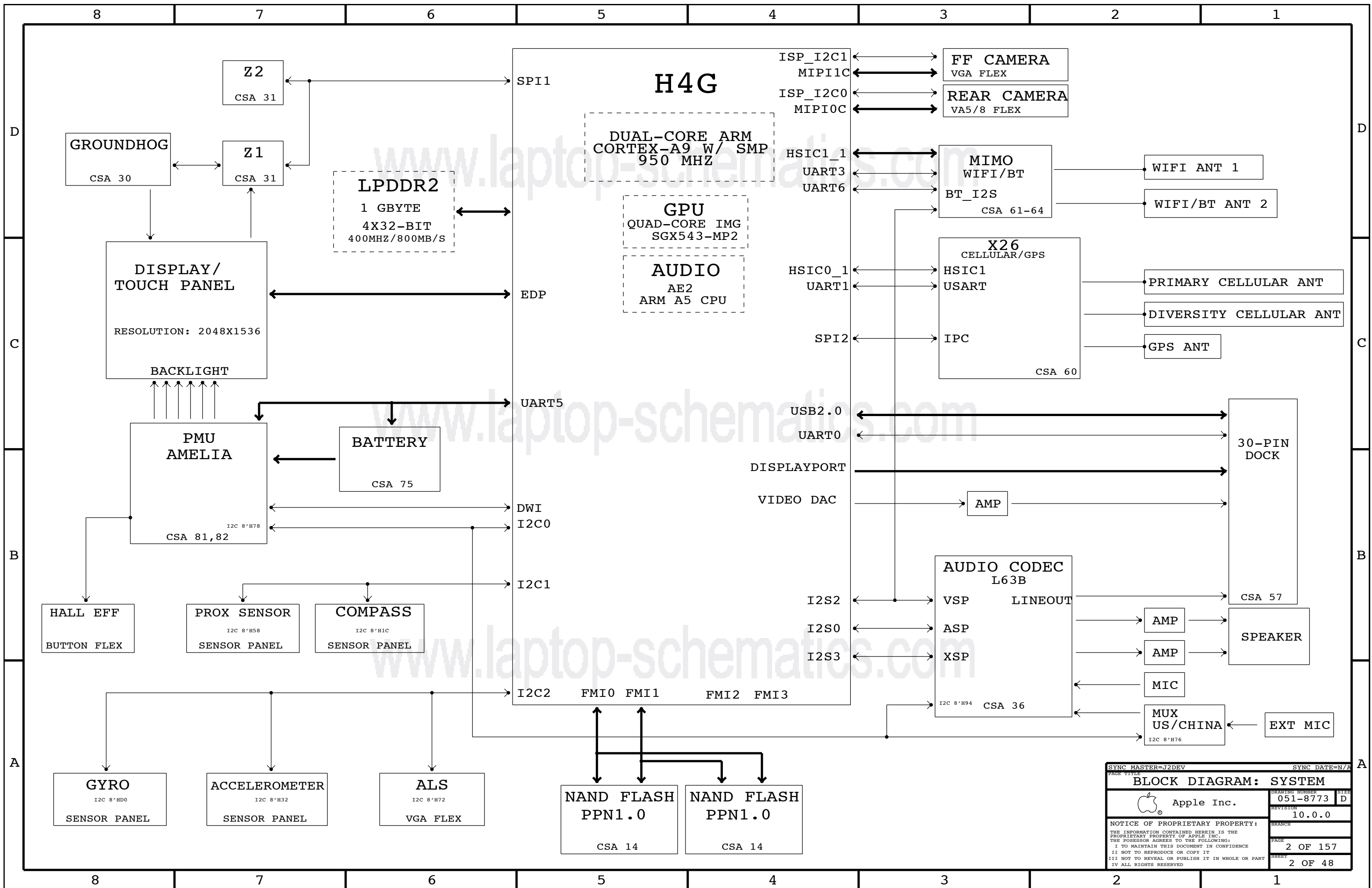
LAST\_MODIFIED= Tue Sep 6 17:35:11 2011

PDF	CSA	CONTENTS	SYNC MASTER	DATE
1	1	Table of Contents	MIKE	NA
2	2	BLOCK DIAGRAM: SYSTEM	J2DEV	N/A
3	4	BOM TABLES	MIKE	N/A
4	6	AP: MAIN	MIKE	N/A
5	7	AP: I/Os	JOE	N/A
6	8	AP: NAND	MIKE	N/A
7	9	AP: TV, DP, MIPI	JOE	01/13/2011
8	10	AP: DDR	MIKE	N/A
9	11	AP: POWER	MIKE	N/A
10	12	AP: MISC & ALIASES	ALEX	N/A
11	13	AP: VIDEO BUFFER, BB USB MUXES	CHOPIN	12/10/2010
12	14	NAND	MIKE	N/A
13	16	DDR 0 AND 1	MIKE	06/21/2010
14	17	DDR 2 AND 3	MIKE	06/21/2010
15	21	MLB ALIASES/CONNECTIONS	ALEX	09/30/2010
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17	30	GRAPE: GROUNDHOG, CONN, BOOST	RAMSIN	12/17/2010
18	31	GRAPE: Z1, Z2	RAMSIN	12/17/2010
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20	37	AUDIO: SPEAKER AMP	KAVITHA	02/03/2011
21	38	AUDIO: HEADPHONE OUT	KAVITHA	02/03/2011
22	42	AUDIO: DETECT/MIC BIAS	KAVITHA	02/03/2011
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24	54	CONNECTOR: SENSOR	MARK	01/11/2011
25	55	SENSOR PANEL FILTERS 1	MARK	01/11/2011
26	56	SENSOR PANEL FILTERS 2	MARK	01/11/2011
27	57	IO FLEX: DOCK COMPONENTS	JOE	01/19/2011
28	58	DISPLAY PORT MISC	JOE	01/19/2011
29	59	IO FLEX: B2B CONNECTOR	JOE	01/19/2011
30	60	CONNECTOR: X26	JOE	01/19/2011
31	61	WLAN BB & POWER	X26_WIFI_MIKE_BT	09/01/2011

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32	62	WLAN 2.4GHZ AND ANT	X26_WIFI_MIKE_BT	09/01/2011
33	63	WLAN 5GHZ AND TEST POINTS	X26_WIFI_MIKE_BT	09/01/2011
34	75	POWER: BATTERY CONNECTOR	MADHAVI	01/13/2011
35	80	POWER ALIASES	MADHAVI	01/13/2011
36	81	POWER: AMELIA PMU	MADHAVI	01/13/2011
37	82	POWER: AMELIA PMU	MLB	01/14/2011
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39	90	DEBUG AND MISC	ALEX	10/04/2010
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43	152	CONSTRAINTS: DISPLAY/AUDIO	MIKE	01/21/2011
44	153	CONSTRAINTS: DDR/FMI	MIKE	01/21/2011
45	154	CONSTRAINTS: POWER / GND	MIKE	01/21/2011
46	155	CONSTRAINTS: DEBUG	MIKE	01/21/2011
47	156	FUNC TEST POINTS	MIKE	01/21/2011
48	157	FUNC TEST POINTS	MIKE	01/21/2011

DRAWING  
 DRAWING  
 MLB  
 Schematic / PCB #'s

DRAWING TITLE		SCH, J2, MLB	
DRAWING NUMBER		051-8773	SIZE D
REVISION		10.0.0	
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SYNC MASTER=J2DEV		SYNC DATE=N/A	
BLOCK DIAGRAM: SYSTEM			
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### Page Notes

Power aliases required by this page:  
(NONE)

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:

#### ALL AVAIL BOM OPTIONS

COMMON  
ALTERNATE

16GB\_PROD  
32GB\_PROD  
64GB\_PROD  
128GB\_PROD

DEVELOPMENT\_JTAG  
DEVELOPMENT\_JTAG\_TAP  
JTAG\_DAP

SPEAKER  
INTERNAL\_MIC

NAND\_IO\_1V8  
NAND\_IO=3V3

SNOTE  
DEV  
MLB  
J2

BOM GROUP	BOM OPTIONS
BASIC	COMMON, ALTERNATE
AUDIO	SPEAKER, INTERNAL_MIC

#### BARCODE LABEL/EEEE CODES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7691	1	EEEE FOR 639-2352 (J1 16G)	EEEE_DNKT	CRITICAL	EEEE_J1_16G
825-7691	1	EEEE FOR 639-2058 (J1 32G)	EEEE_DM2N	CRITICAL	EEEE_J1_32G
825-7691	1	EEEE FOR 639-2059 (J1 64G)	EEEE_DM2P	CRITICAL	EEEE_J1_64G
825-7691	1	EEEE FOR 639-2353 (J2 16G)	EEEE_DNKV	CRITICAL	EEEE_J2_16G
825-7691	1	EEEE FOR 639-1572 (J2 32G)	EEEE_DHWV	CRITICAL	EEEE_J2_32G
825-7691	1	EEEE FOR 639-1871 (J2 64G)	EEEE_DKQL	CRITICAL	EEEE_J2_64G
825-7691	1	EEEE FOR 639-1870 (J2 128G)	EEEE_DKQK	CRITICAL	EEEE_J2_128G
825-7691	1	EEEE FOR 639-2844 (J2A 16G)	EEEE_DRJQ	CRITICAL	EEEE_J2A_16G
825-7691	1	EEEE FOR 639-2826 (J2A 32G)	EEEE_DRP6	CRITICAL	EEEE_J2A_32G
825-7691	1	EEEE FOR 639-2827 (J2A 64G)	EEEE_DRP5	CRITICAL	EEEE_J2A_64G

#### MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-2105	1	FENCE, NAND, TOP, MLB, J2	PD_FENCE_NAND	CRITICAL	
806-1857	1	FENCE, LARGE, TOP, MLB, J2	PD_FENCE_LARGE	CRITICAL	
806-2349	1	FENCE, SMALLER, TOP, MLB, J2	PD_FENCE_SMALL	CRITICAL	
806-1860	1	FENCE, 1, BTM, MLB, J2	PD_FENCE_BT1	CRITICAL	
806-1865	1	FENCE, 2, BTM, MLB, J2	PD_FENCE_BT2	CRITICAL	
806-2352	1	FENCE, SMALLER, BTM, MLB, J2	PD_FENCE_BT3	CRITICAL	

#### SCH AND BOARD P/N

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-8773	1	SCH, MLB, J2	SCH1	CRITICAL	?
820-2996	1	PCBF, MLB, J2	PCB1	CRITICAL	?
085-3058	1	DEV BOM, MLB, J2	DEV1		?

#### SOC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
34380533	1	IC, SOC, H4G, FCBGA1225	U0600	CRITICAL	?

#### PMU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
34380561	1	IC, PMU, AMELIA, D1974AB	U8100	CRITICAL	?

#### SDRAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33380579	2	SDRAM, LPDDR2, 512MB, SAMSUNG 46NM	U1600, U1700	CRITICAL	?

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
33380580	33380579		U1600, U1700	LPDDR2, HYNIX 44NM
33380581	33380579		U1600, U1700	LPDDR2, ELPIDA 45NM

#### NAND

##### 16GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33580781	1	HYNIX 26NM PPN1.0 16GB	U1400	CRITICAL	16GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
33580804	33580781	16GB_PROD	U1400	TOSHIBA 24NM PPN1.0

##### 32GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33580781	2	HYNIX 26NM PPN1.0 32GB	U1400, U1410	CRITICAL	32GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
33580804	33580781	32GB_PROD	U1400, U1410	TOSHIBA 24NM PPN1.0

##### 64GB FLASH CONFIGURATIONS


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33580782	2	HYNIX 26NM PPN1.0 64GB	U1400, U1410	CRITICAL	64GB_PROD

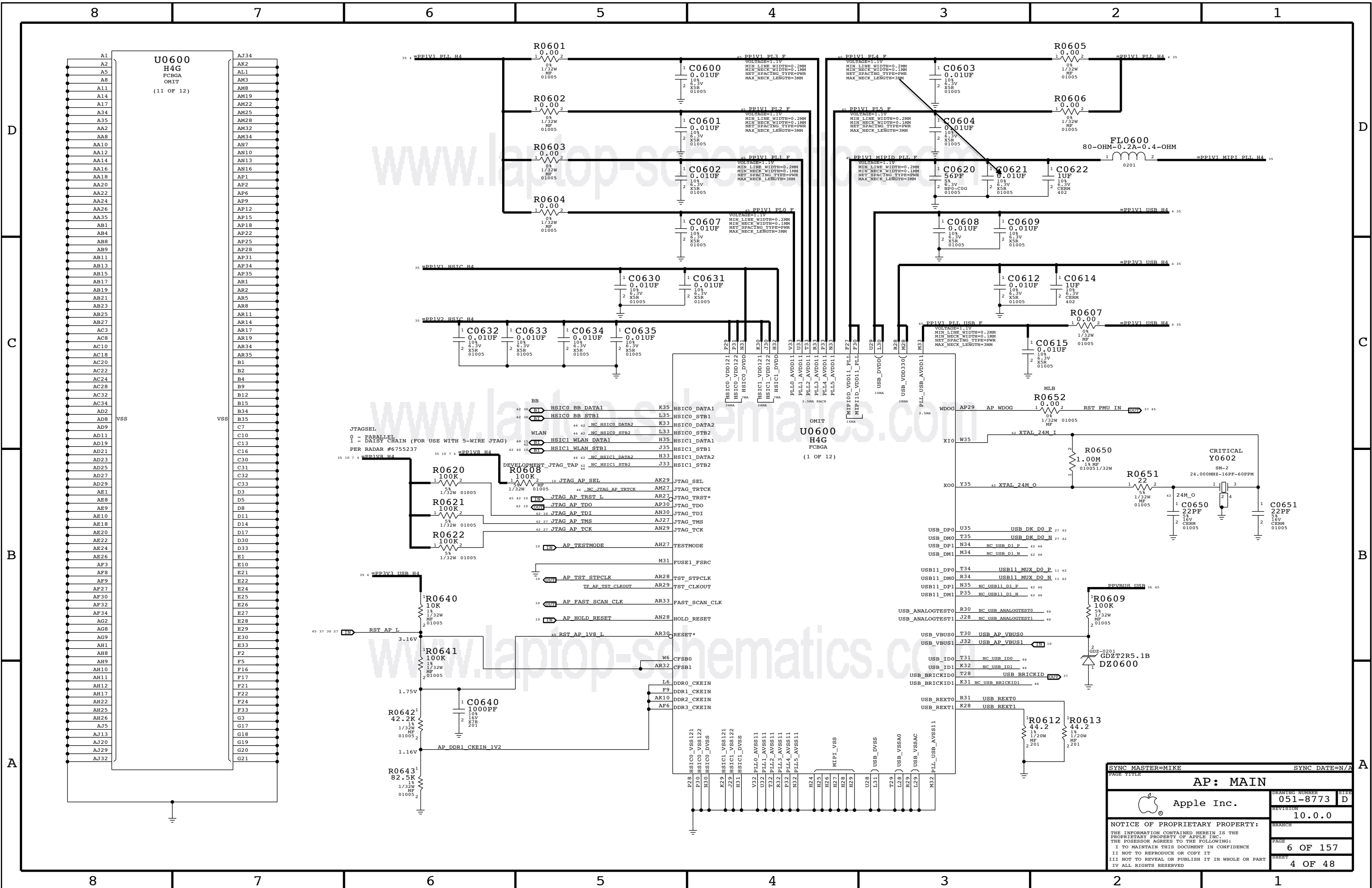
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
33580805	33580782	64GB_PROD	U1400, U1410	TOSHIBA 24NM PPN1.0

##### 128GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33580814	2	HYNIX 26NM PPN1.0 128GB	U1400, U1410	CRITICAL	128GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
33580806	33580814	128GB_PROD	U1400, U1410	TOSHIBA 24NM PPN1.0

SYNC MASTER=MIKE		SYNC DATE=N/A	
<b>BOM TABLES</b>			
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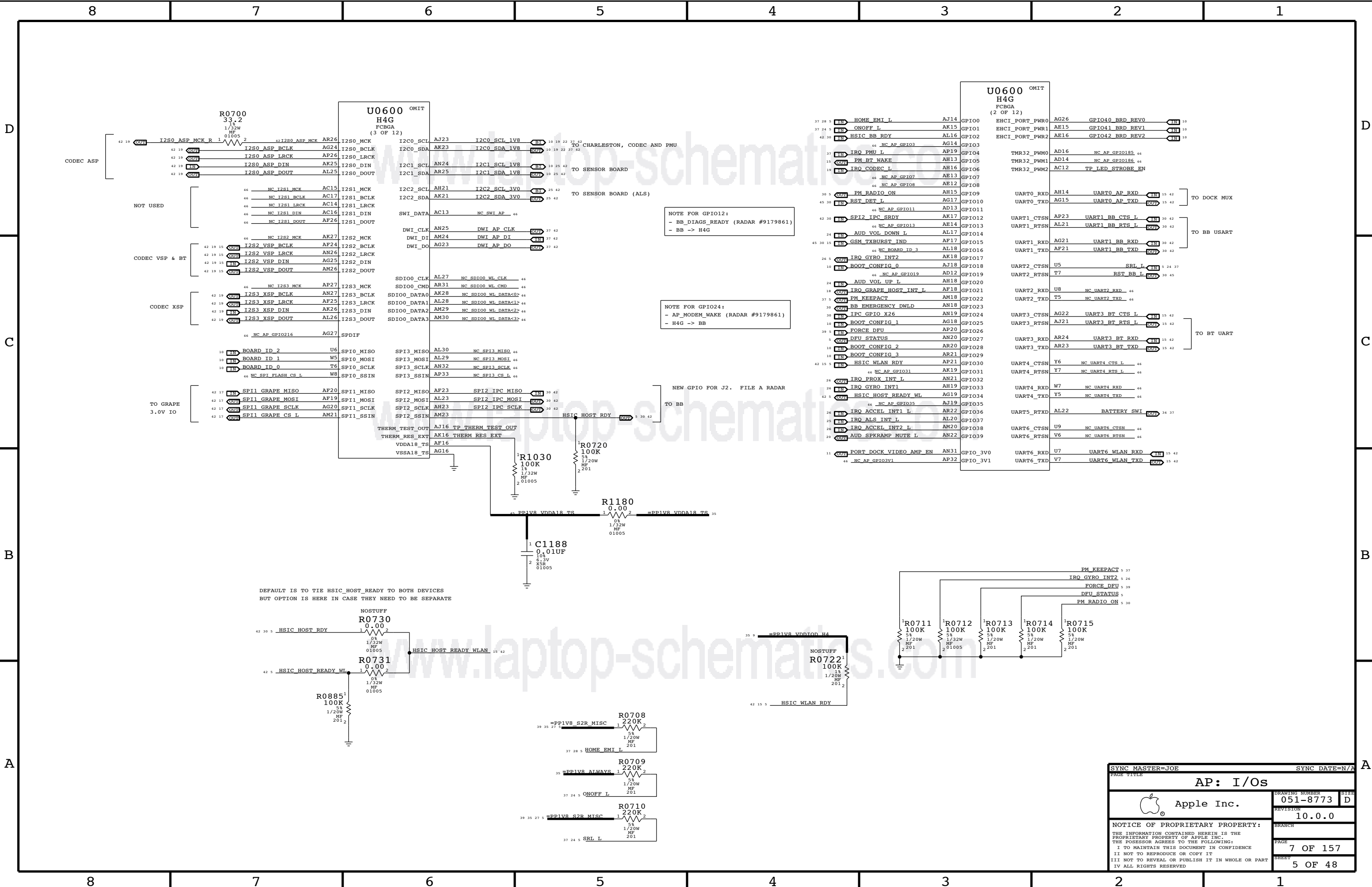


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PAGE TITLE		SYNC DATE=N/A	
<b>AP: MAIN</b>			
Apple Inc.	DRAWING NUMBER	051-8773	SIZE
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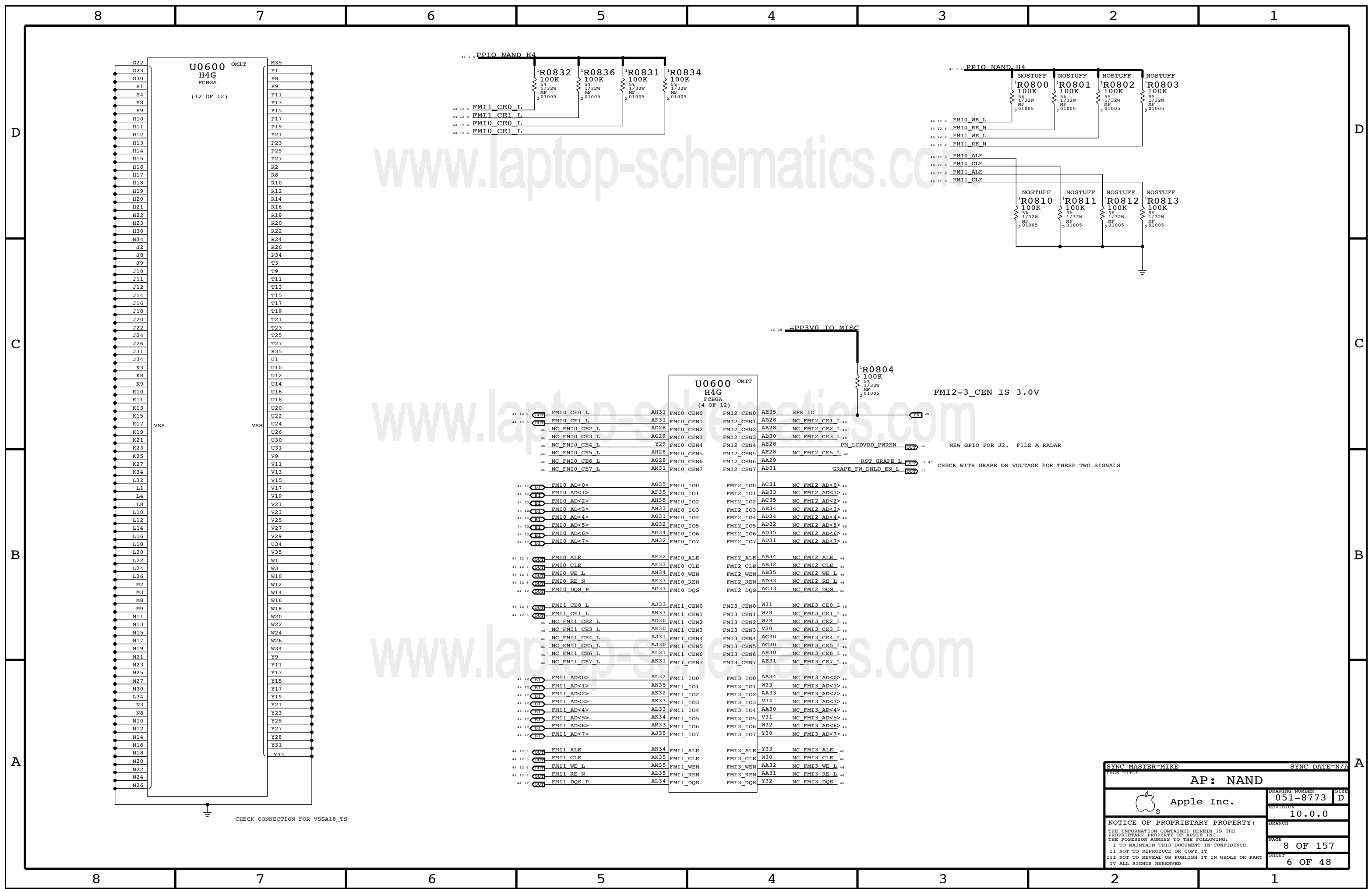
DEFAULT IS TO TIE HSI\_HOST\_READY TO BOTH DEVICES  
 BUT OPTION IS HERE IN CASE THEY NEED TO BE SEPARATE

NOTE FOR GPIO12:  
 - BB\_DIAGS\_READY (RADAR #9179861)  
 - BB -> H4G

NOTE FOR GPIO24:  
 - AP\_MODEM\_WAKE (RADAR #9179861)  
 - H4G -> BB

NEW GPIO FOR J2. FILE A RADAR

SYNC MASTER=JOE		SYNC DATE=N/A	
PAGE TITLE			
AP: I/Os		DRAWING NUMBER	SIZE
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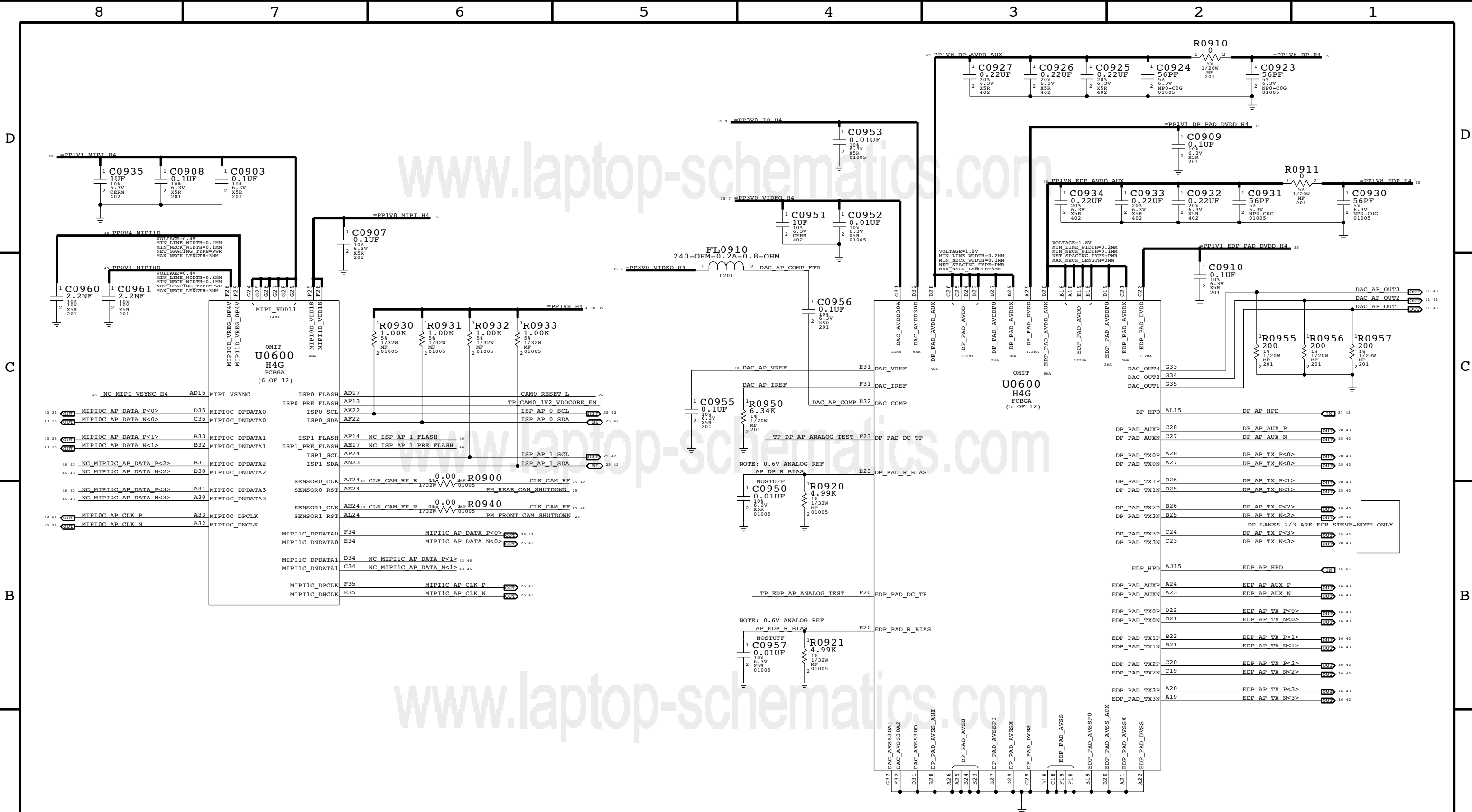


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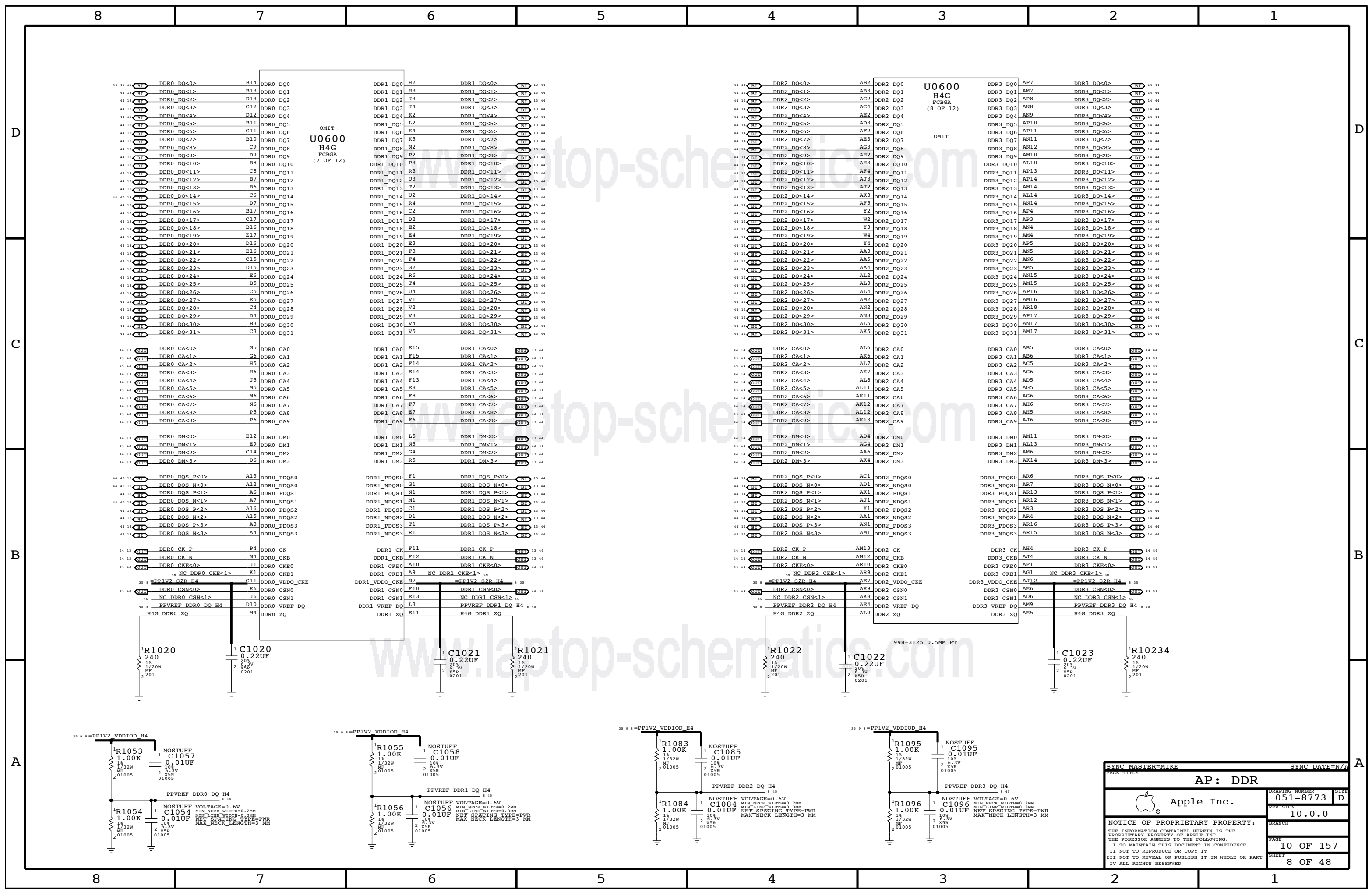
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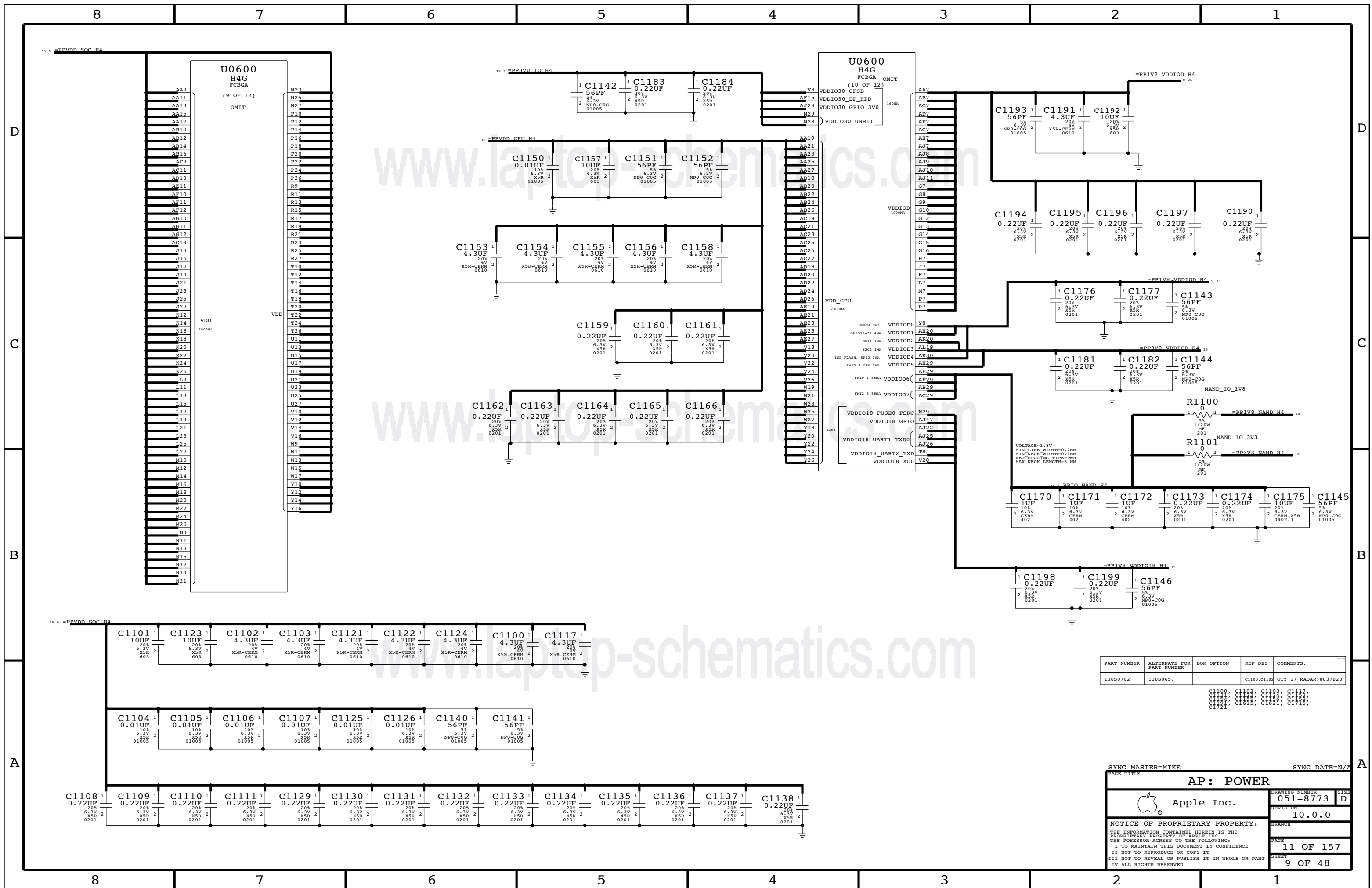


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132S0279	132S0154		C0960, C0961	RADAR:9624625

SYNC MASTER=JOE		SYNC DATE=01/13/2011	
PAGE TITLE			
<b>AP: TV, DP, MIPI</b>			
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<b>AP: DDR</b>			
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
13880702	13880657		C1100, C1102	QTY 17 RADAR:8837828

C1100, C1102, C1103, C1117, C1144, C1145, C1156, C1158, C1159, C1161, C1162, C1163, C1164, C1165, C1166, C1171, C1172, C1173, C1174, C1175, C1176, C1177, C1181, C1182, C1184, C1185, C1186, C1187, C1188, C1189, C1190, C1191, C1192, C1193, C1194, C1195, C1196, C1197, C1198, C1199

SYNC MASTER=MIKE SYNC DATE=N/A

**AP: POWER**

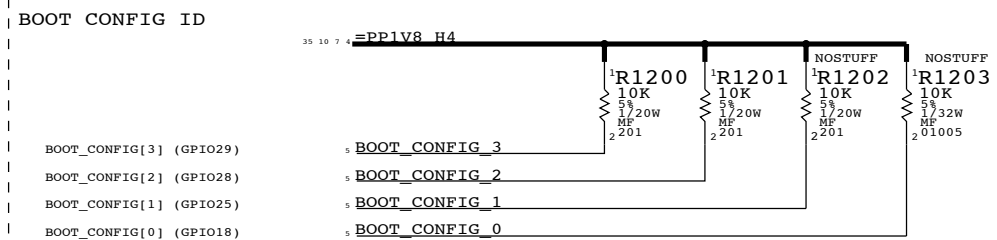
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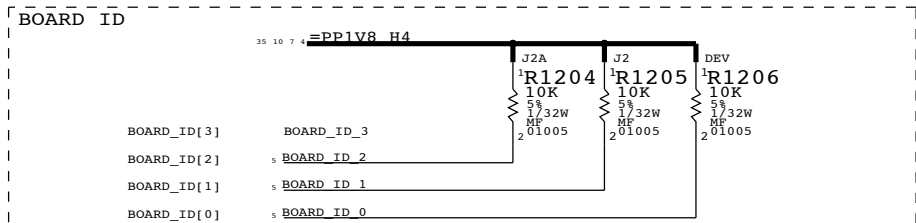


BOOT\_CONFIG[3-0]

1100	FMIO/1 2/2 CS
1101	FMIO/1 4/4 CS
1110	FMIO/1 4/4 CS WITH TEST

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

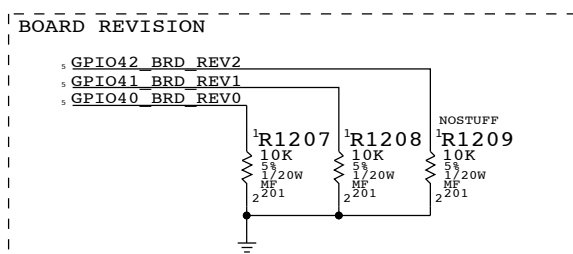


BOARD\_ID[3-0]

0000	J1 AP
0001	J1 DEV
0010	J2 AP
0011	J2 DEV
0100	J2A AP
0101	J2A DEV

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ



BRD\_REV[2-0]

000	PROTO 0
001	PROTO 1 LOCAL
010	PROTO 1 CHINA
011	PROTO 2
100	EVT

S/W READ FLOW

1. SET GPIO AS INPUT
2. ENABLE PU AND DISABLE PD
3. READ

FOR REFERENCE

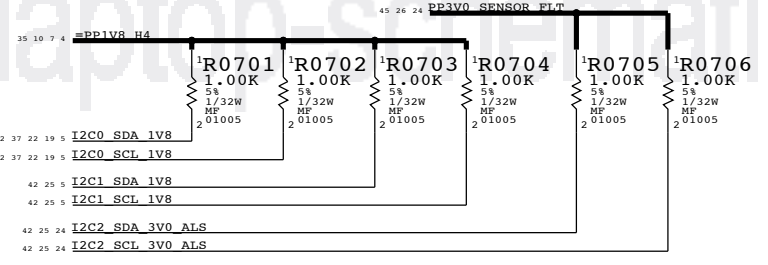
BOOT\_CONFIG[3:0]

0000	SPIO
0001	SPI1
0010	SPIO W/TEST
0011	SPI1 W/TEST
0100	FMIO 2CS
0101	FMIO 4CS
0110	FMIO 4CS W/TEST
0111	RESERVED
1000	FMIO 2 CS
1001	FMIO 4 CS
1010	FMIO 4CS W/TEST

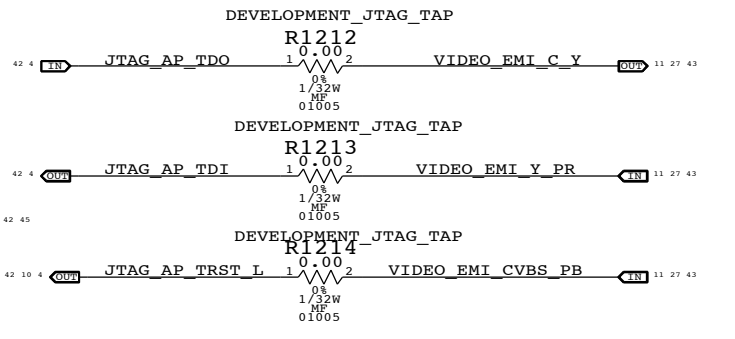
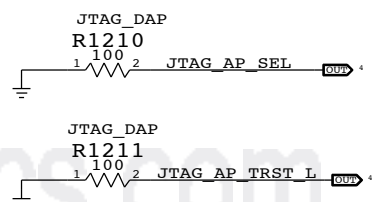
CURRENT SETTING ->

1100	FMIO/1 2/2 CS
1101	FMIO/1 4/4 CS
1110	FMIO/1 4/4 CS W/TEST
1111	RESERVED

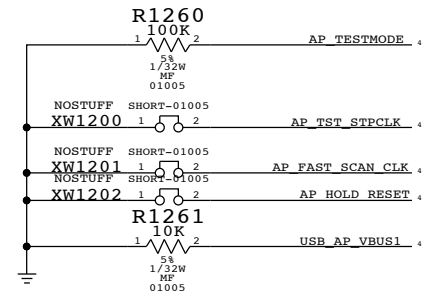
### I2C PULL-UPS



### JTAG



2-WIRE DAP	SCAN DUMP	PRODUCTION
DEVELOPMENT_JTAG	DEVELOPMENT_JTAG	JTAG_DAP
JTAG_DAP	DEVELOPMENT_JTAG_TAP	



SYNC MASTER=ALEX SYNC DATE=N/A

AP: MISC & ALIASES

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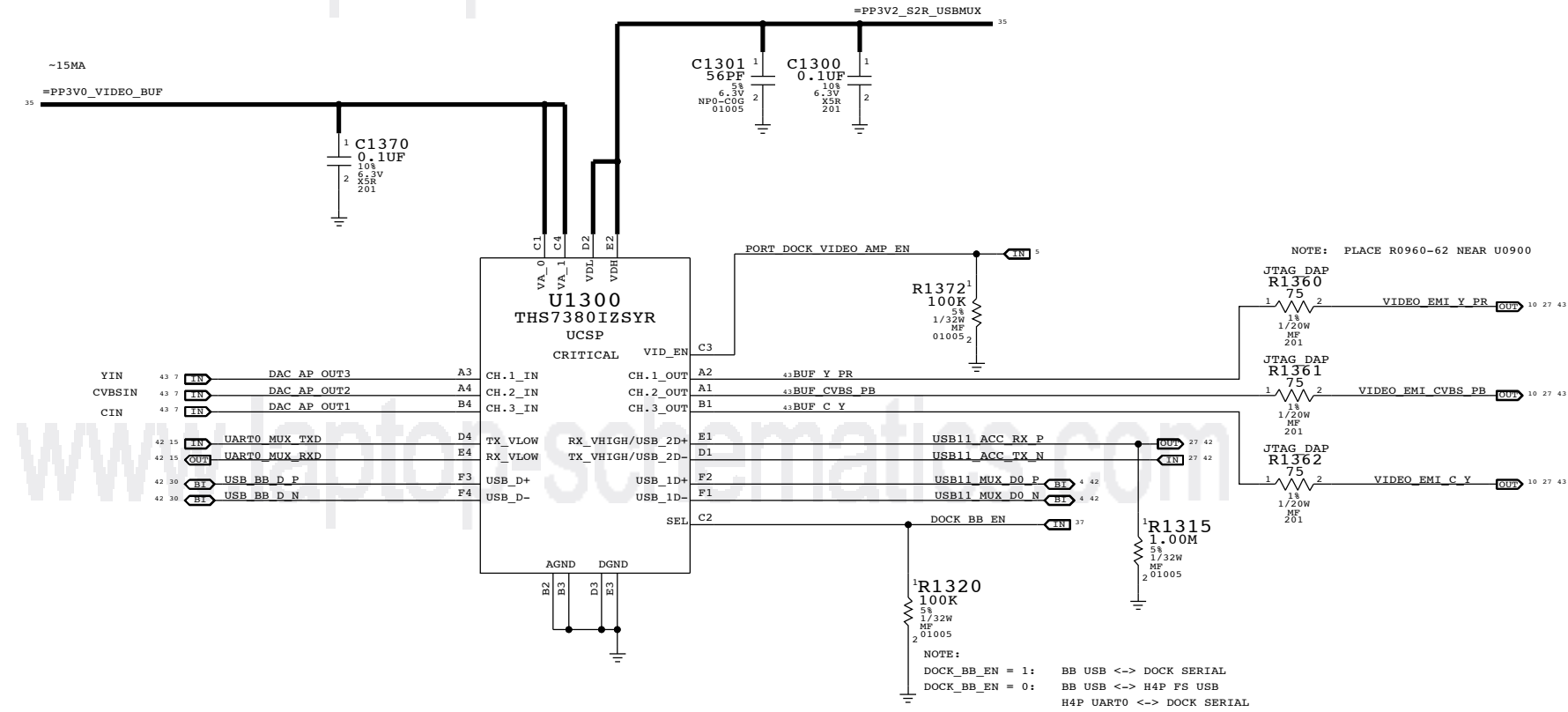
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
34380539	34380520		U1300	RADAR:9009078

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SYNC MASTER=CHOPIN SYNC DATE=12/10/2010

PAGE TITLE: AP: VIDEO BUFFER, BB USB MUXES

DRAWING NUMBER: 051-8773 SIZE: D

REVISION: 10.0.0

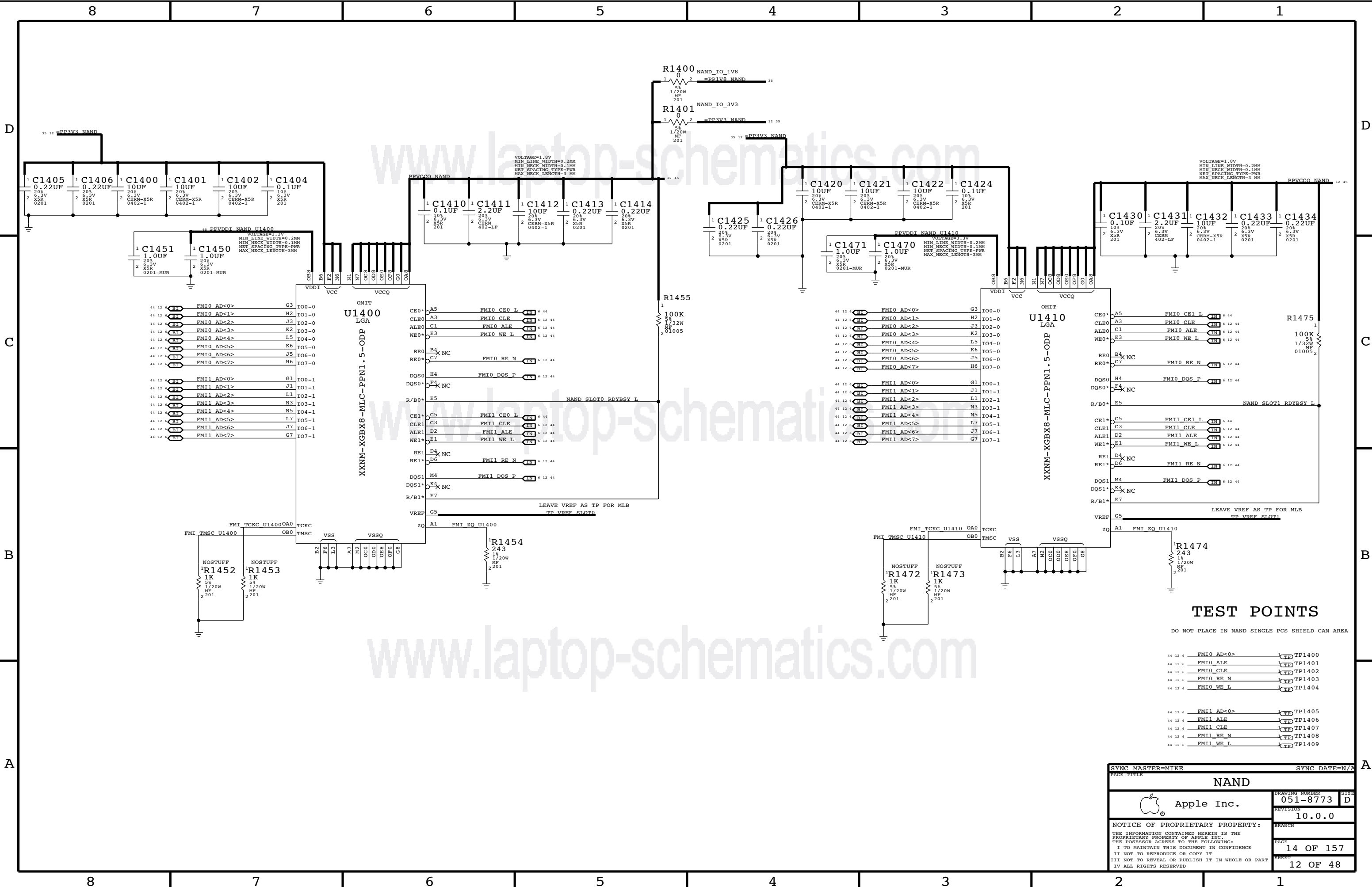
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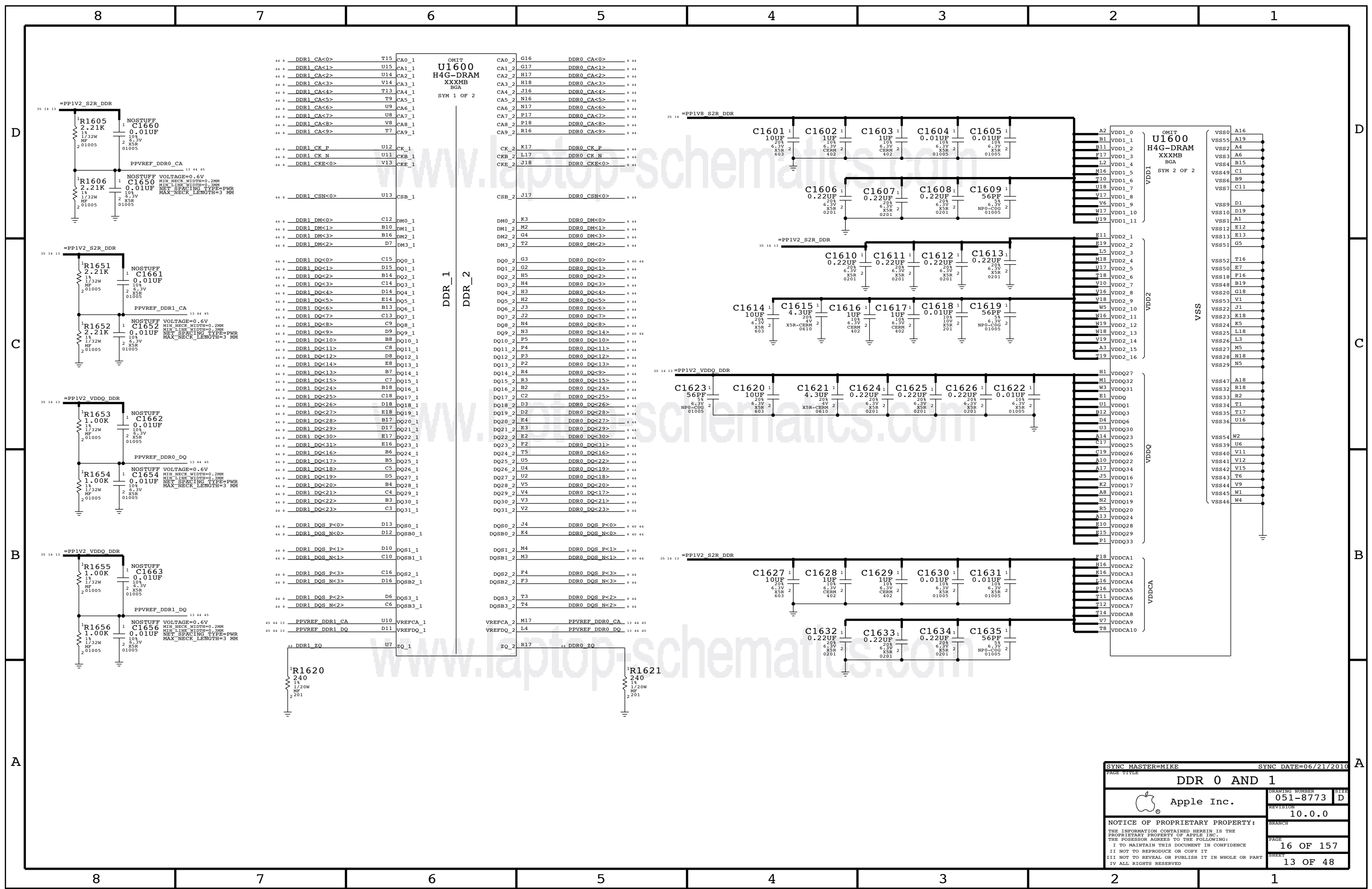


**TEST POINTS**

DO NOT PLACE IN NAND SINGLE PCS SHIELD CAN AREA

- 44 12 6 FMIO AD<0> TP1400
- 44 12 6 FMIO ALE TP1401
- 44 12 6 FMIO CLE TP1402
- 44 12 6 FMIO RE\_N TP1403
- 44 12 6 FMIO WE\_L TP1404
  
- 44 12 6 FMII AD<0> TP1405
- 44 12 6 FMII ALE TP1406
- 44 12 6 FMII CLE TP1407
- 44 12 6 FMII RE\_N TP1408
- 44 12 6 FMII WE\_L TP1409

SYNC MASTER=MIKE		SYNC DATE=N/A	
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Pin	Signal	Component	Value
U15	CA0_1	Capacitor	100uF
U14	CA1_1	Capacitor	100uF
U13	CA2_1	Capacitor	100uF
U12	CA3_1	Capacitor	100uF
U11	CA4_1	Capacitor	100uF
U10	CA5_1	Capacitor	100uF
U9	CA6_1	Capacitor	100uF
U8	CA7_1	Capacitor	100uF
U7	CA8_1	Capacitor	100uF
U6	CA9_1	Capacitor	100uF
U12	CK_1	Capacitor	100uF
U11	CKB_1	Capacitor	100uF
U13	CKE_1	Capacitor	100uF
U13	CSB_1	Capacitor	100uF
C12	DM0_1	Capacitor	100uF
B10	DM1_1	Capacitor	100uF
B16	DM2_1	Capacitor	100uF
D7	DM3_1	Capacitor	100uF
C15	DQ0_1	Capacitor	100uF
B15	DQ1_1	Capacitor	100uF
B14	DQ2_1	Capacitor	100uF
C14	DQ3_1	Capacitor	100uF
D14	DQ4_1	Capacitor	100uF
E14	DQ5_1	Capacitor	100uF
B13	DQ6_1	Capacitor	100uF
C13	DQ7_1	Capacitor	100uF
C9	DQ8_1	Capacitor	100uF
D9	DQ9_1	Capacitor	100uF
B8	DQ10_1	Capacitor	100uF
C8	DQ11_1	Capacitor	100uF
D8	DQ12_1	Capacitor	100uF
E8	DQ13_1	Capacitor	100uF
B7	DQ14_1	Capacitor	100uF
C7	DQ15_1	Capacitor	100uF
B18	DQ16_1	Capacitor	100uF
D18	DQ17_1	Capacitor	100uF
E18	DQ18_1	Capacitor	100uF
B17	DQ19_1	Capacitor	100uF
D17	DQ20_1	Capacitor	100uF
E17	DQ21_1	Capacitor	100uF
E16	DQ22_1	Capacitor	100uF
B6	DQ23_1	Capacitor	100uF
B5	DQ24_1	Capacitor	100uF
C5	DQ25_1	Capacitor	100uF
D5	DQ26_1	Capacitor	100uF
B4	DQ27_1	Capacitor	100uF
C4	DQ28_1	Capacitor	100uF
B3	DQ29_1	Capacitor	100uF
C3	DQ30_1	Capacitor	100uF
C3	DQ31_1	Capacitor	100uF
D13	DQS0_1	Capacitor	100uF
D12	DQS0B_1	Capacitor	100uF
D10	DQS1_1	Capacitor	100uF
C10	DQS1B_1	Capacitor	100uF
C16	DQS2_1	Capacitor	100uF
D16	DQS2B_1	Capacitor	100uF
D6	DQS3_1	Capacitor	100uF
C6	DQS3B_1	Capacitor	100uF
U10	VREFCA_1	Resistor	240 Ohm
D11	VREFDQ_1	Resistor	240 Ohm
U7	ZQ_1	Resistor	240 Ohm

SYNC MASTER=MIKE SYNC DATE=06/21/2010

DDR 0 AND 1

Apple Inc.

DRAWING NUMBER: 051-8773

REVISION: 10.0.0

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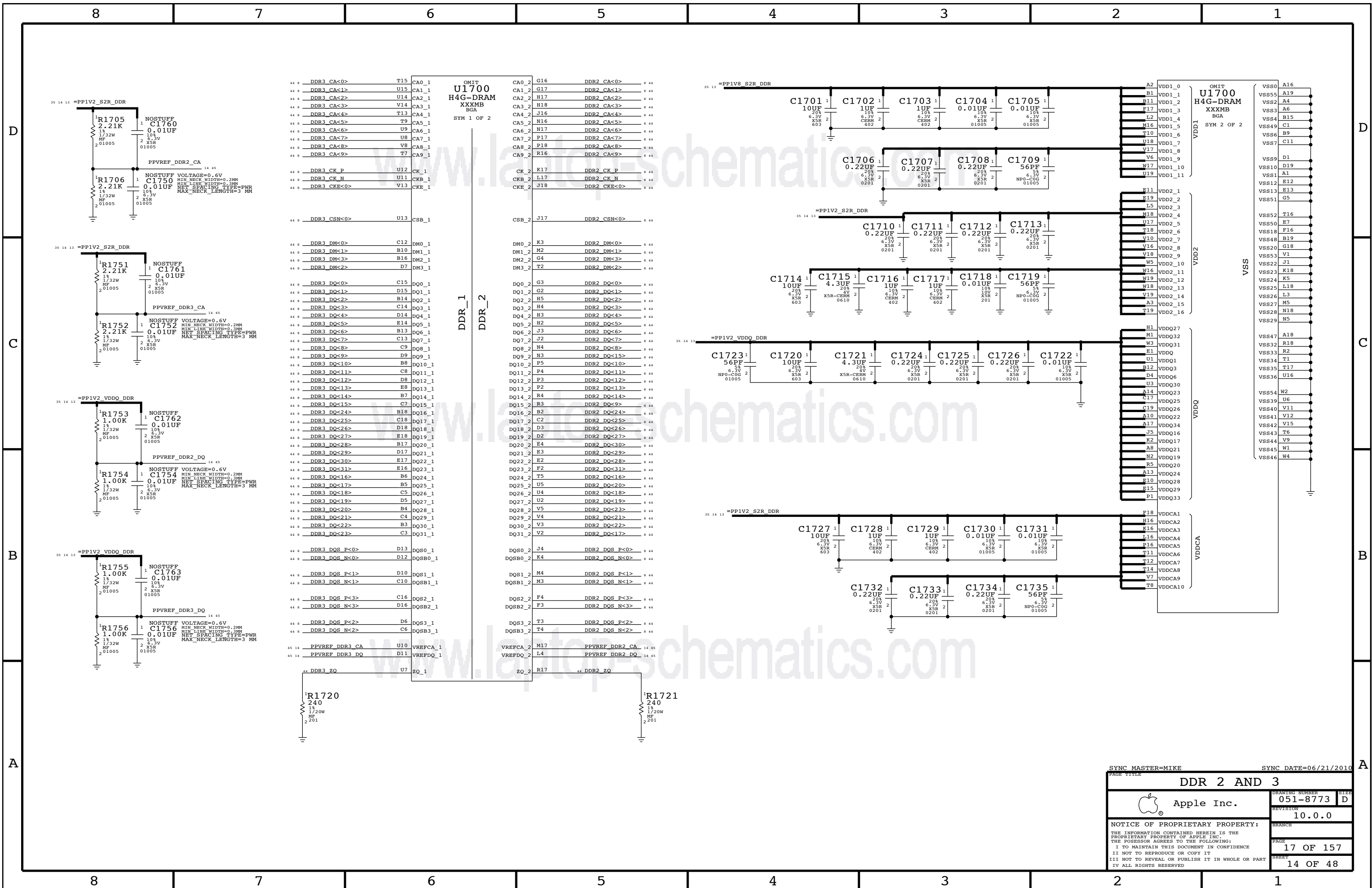
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### WIFI ALIASES

42 40 4	HSIC1 WLAN DATA1	====	HSIC DATA 4330	31 33
42 40 4	HSIC1 WLAN STB1	====	HSIC STROBE 4330	31 33
42 5	HSIC HOST READY WLAN	====	WLAN GPIO1	31 33
42 5	HSIC WLAN_RDY	====	HSIC_DEVICE_READY	31
45 37	RST WLAN_L	====	WLAN_ENABLE	31 33
37	PM WLAN HOST WAKE	====	WLAN GPIO0	31 33
45 37	RST BT_L	====	BT RESET_N	31 33
37	PM BT HOST WAKE	====	BT_HOST_WAKE	31 33
37	PM BT WAKE	====	BT_WAKE	31 33
42 5	UART3 BT_RXD	====	BT_UART_TXD	31 33
42 5	UART3 BT_TXD	====	BT_UART_RXD	31 33
42 5	UART3 BT_CTS_L	====	BT_UART_RTS_N	31 33
42 5	UART3 BT_RTS_L	====	BT_UART_CTS_N	31 33
42 37	CLK_32K WLAN	====	CLK32K	32 33
42 19 5	I2S2_VSP_BCLK	====	BT_FCM_CLK	31
42 19 5	I2S2_VSP_DOUT	====	BT_FCM_DIN	31
42 19 5	I2S2_VSP_DIN	====	BT_FCM_DOUT	31
42 19 5	I2S2_VSP_LRCK	====	BT_FCM_SYNC	31
42 5	UART6 WLAN_RXD	====	WLAN_GPIO4	31 33
42 5	UART6 WLAN_TXD	====	WLAN_GPIO3	31 33

### UART ALIASES

42 5	UART0_AP_RXD	====	UART0_MUX_RXD	11 42
42 5	UART0_AP_TXD	====	UART0_MUX_TXD	11 42

### OBSOLETE ALIASES

NC_EXT_SMPS_REQ	====	EXT_SMPS_REQ	31
NC_EXT_PWM_REQ	====	EXT_PWM_REQ	31
NC_BT_GPIO5	====	BT_GPIO5	31
TP_WLAN_GPIO5	====	WLAN_GPIO5	31

45 30 5 GSM\_TXBURST\_IND ===== LED\_DRIVE\_GSMB  
NEED TO DOUBLE CHECK IF WE NEED THIS IN IPAD, OR IF THIS MIGHT BE A PHONE SPECIFIC ISSUE

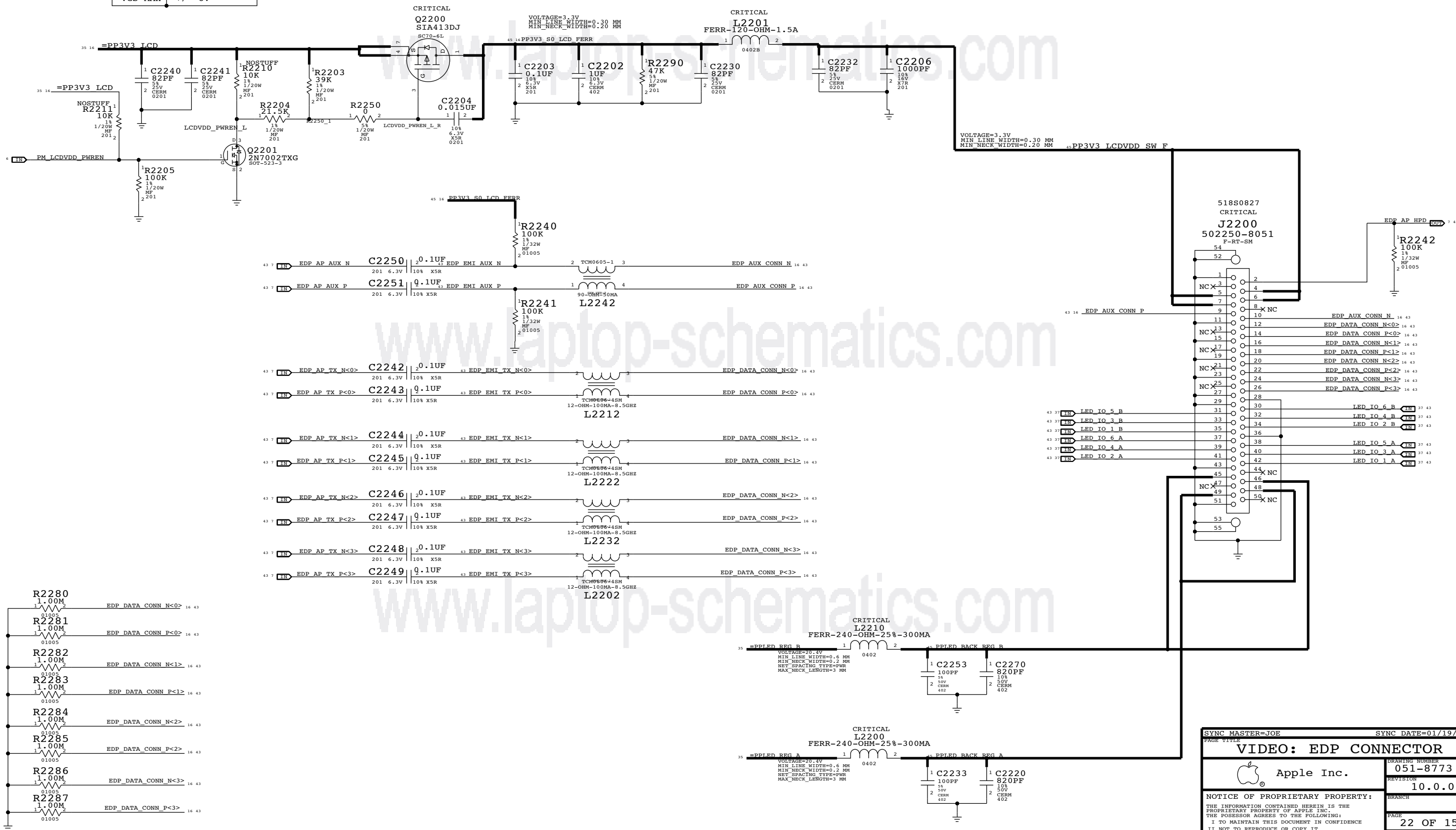
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PAGE TITLE <b>MLB ALIASES/CONNECTIONS</b>			
DRAWING NUMBER 051-8773		SIZE D	
REVISION 10.0.0		BRANCH	
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# EDP CONNECTOR

SIA413DJ

MOSFET	SIA413DJ
CHANNEL	P-TYPE
RDS(ON)	100MOHM @-1.5V
IMAX	3 A
VGS MAX	+/- 8V

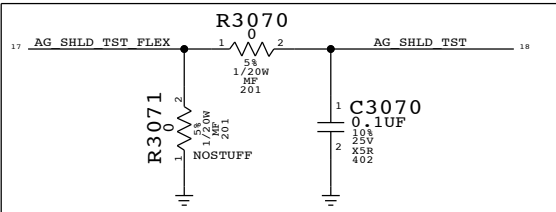
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
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15580667	15580583			RADAR:8616060, RADAR: 9015335



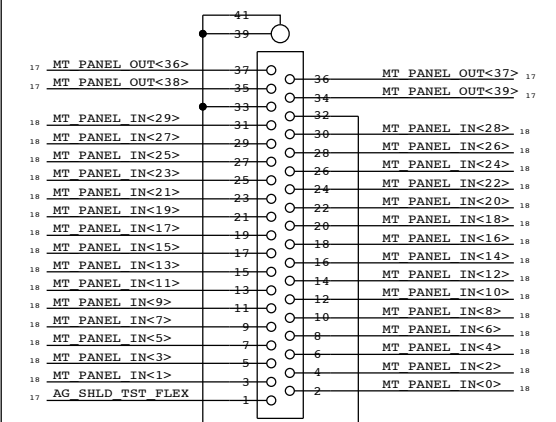
SYNC MASTER=JOE		SYNC DATE=01/19/2011	
<b>VIDEO: EDP CONNECTOR</b>			
Apple Inc.		DRAWING NUMBER	051-8773
		REVISION	10.0.0
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
34380525	1	IC,ASIC,GROUNDHOG B0,120B BGA	U3003	CRITICAL	

### CONNECTORS TO GRAPE FLEX

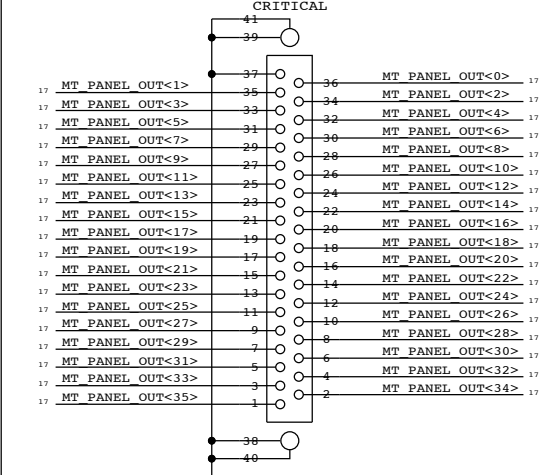


### CRITICAL P/N 518S0828



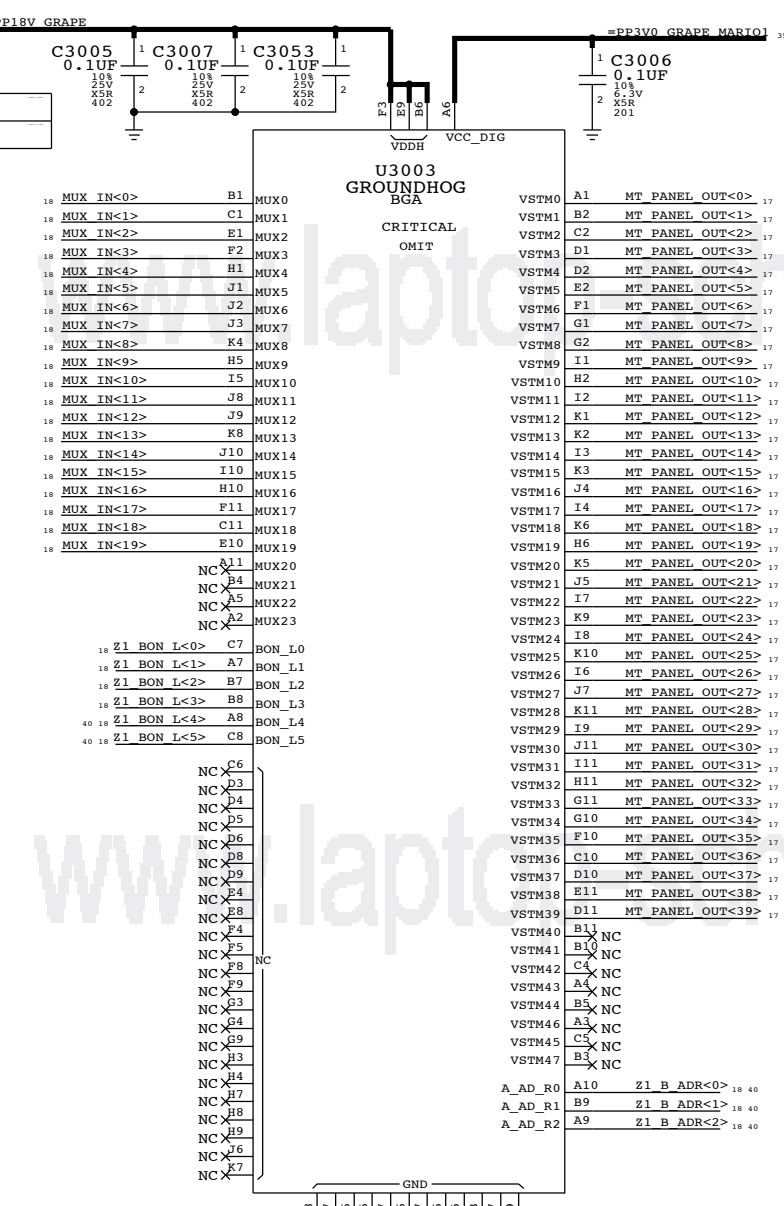
### F-RT-SM 502250-8037 J3010

MATES WITH LEFTMOST GRAPE FLEX TAIL

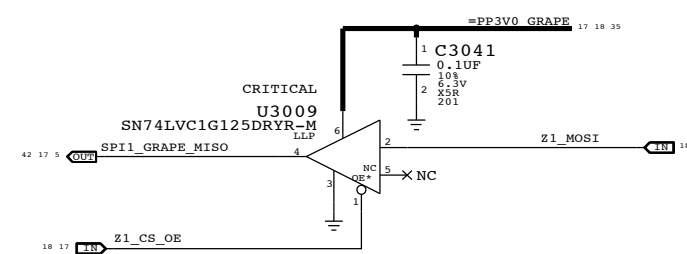
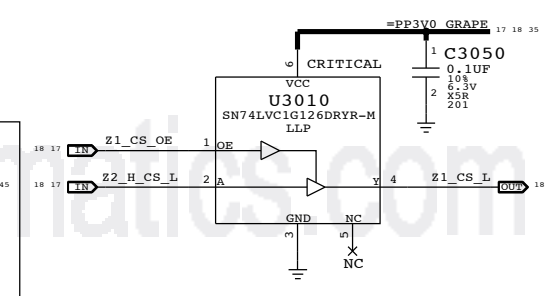
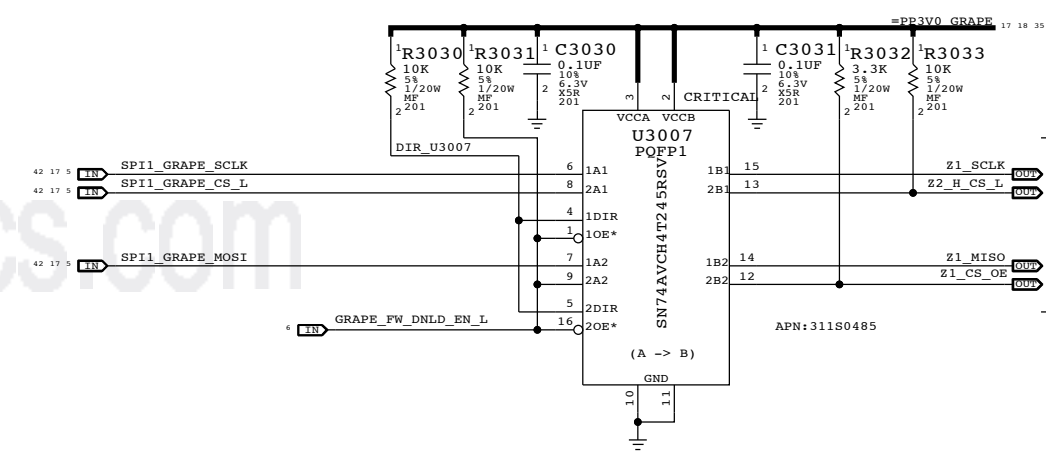
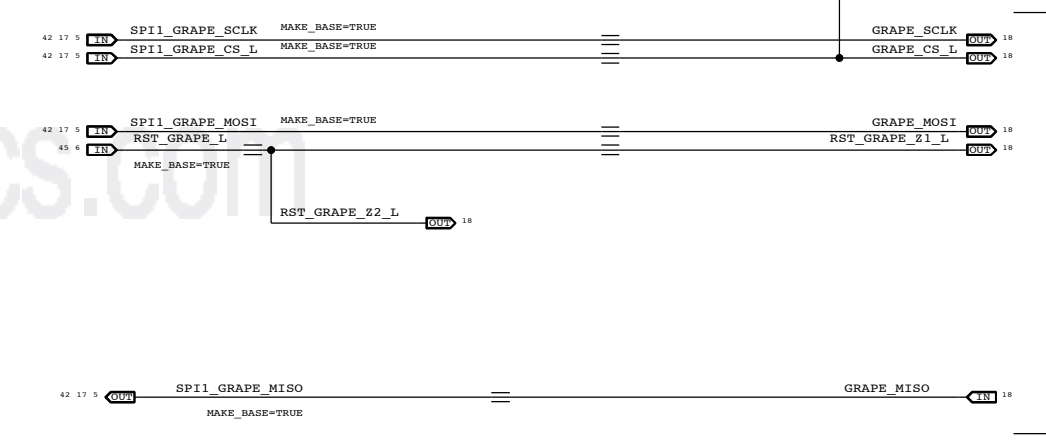
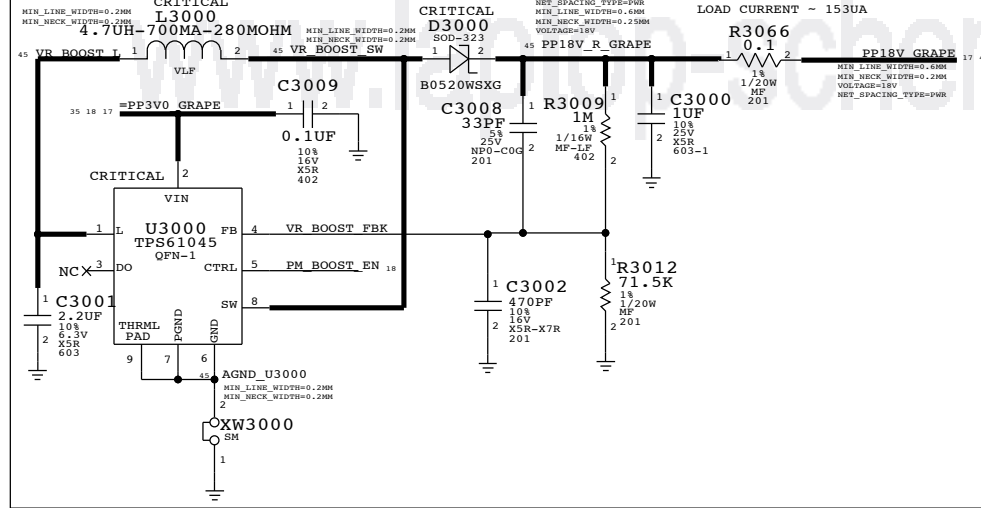


### F-RT-SM 502250-8037 J3011

MATES WITH RIGHTMOST GRAPE FLEX TAIL



### BOOST CONVERTOR



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
31180523	31180485		U3007	
31180524	31180533		U3009	
31180525	31180532		U3010	

SYNC MASTER=RAMSIN SYNC DATE=12/17/2010

**GRAPE: GROUNDHOG, CONN, BOOST**

Apple Inc.

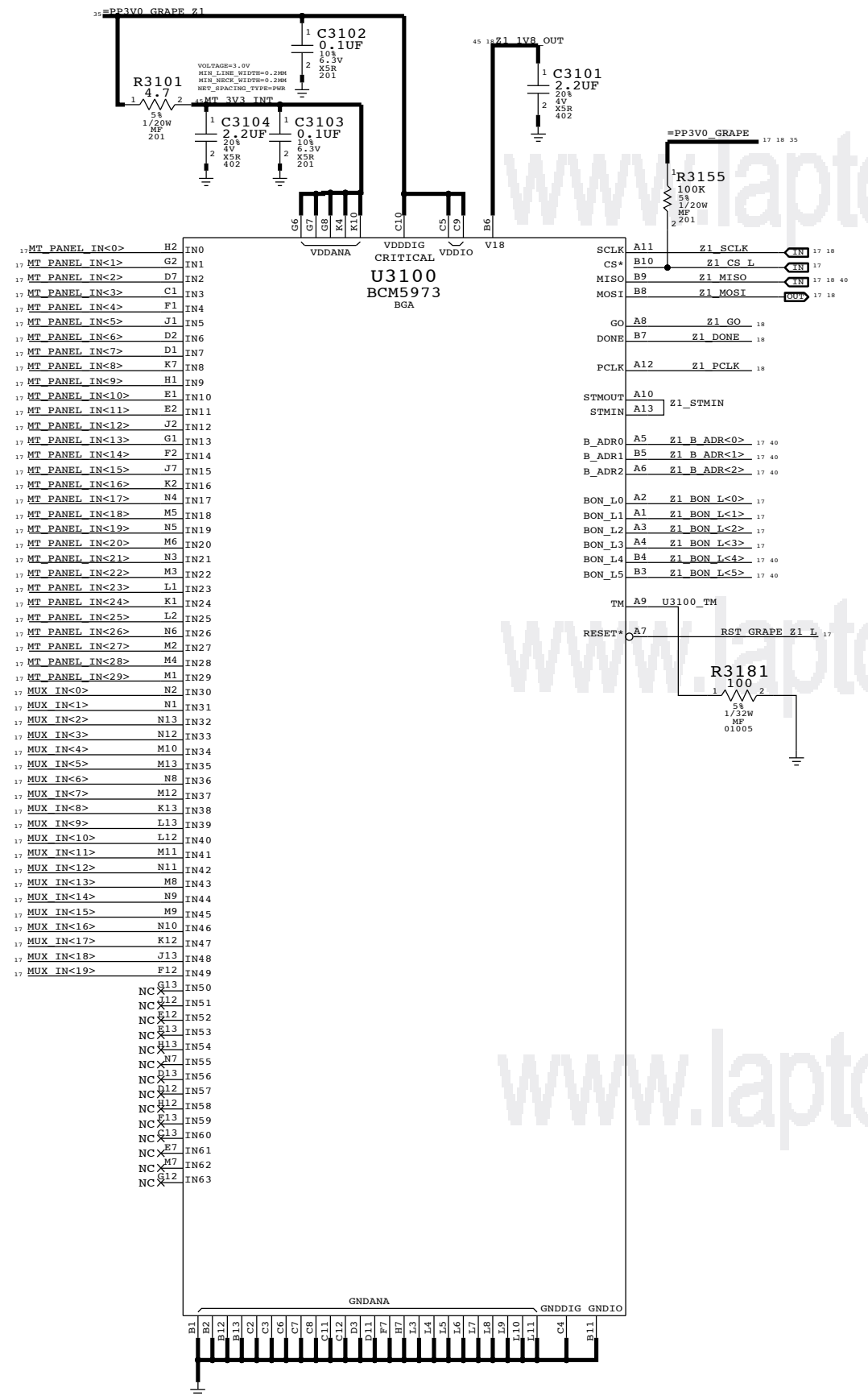
DRAWING NUMBER: 051-8773

REVISION: 10.0.0

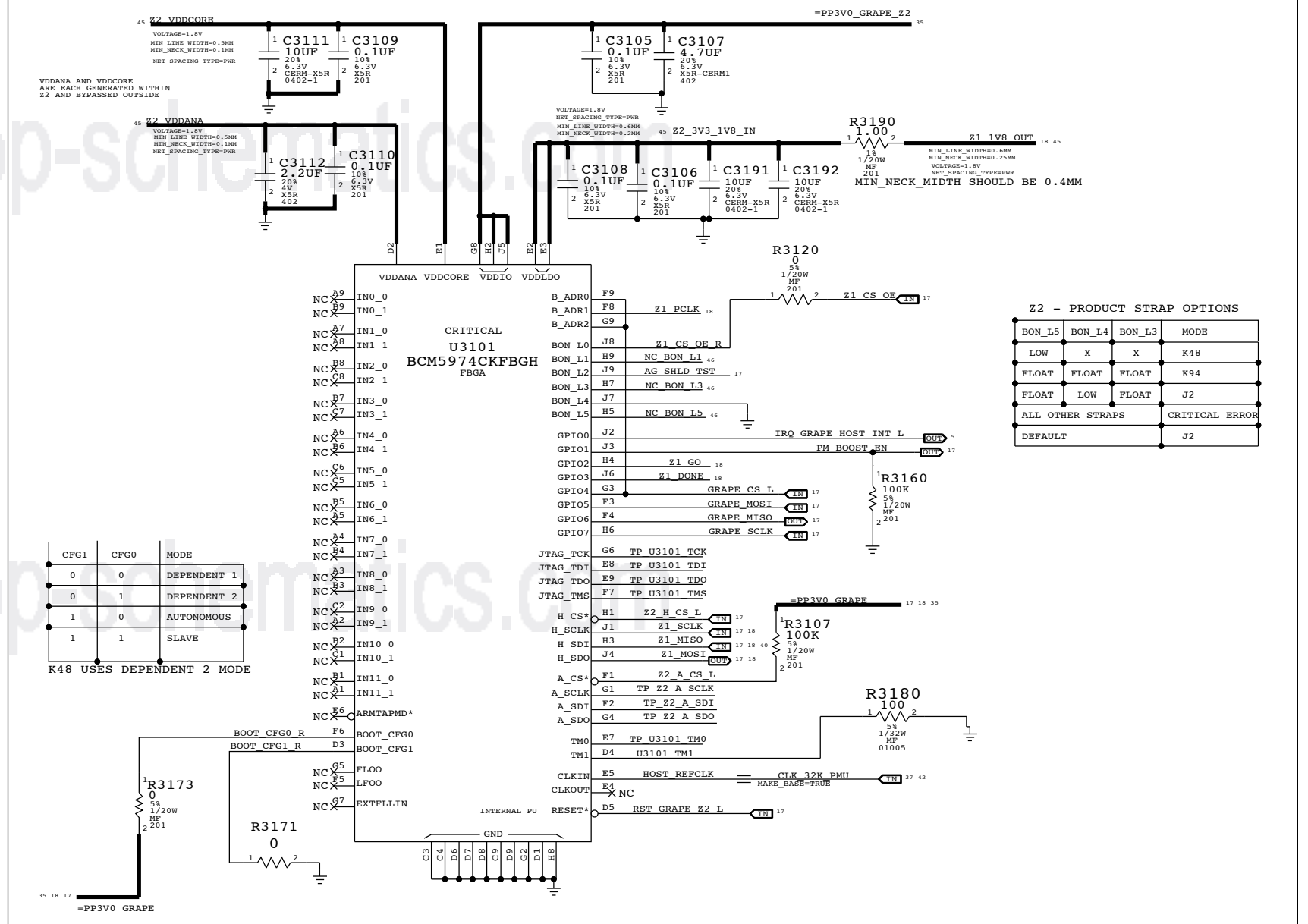
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ZEPHYR 1+ ASIC



ARM9 MCU (Z2 BASED)



SYNC MASTER=RAMSIN SYNC DATE=12/17/2010

PAGE TITLE: GRAPE: Z1, Z2

Apple Inc.

DRAWING NUMBER: 051-8773 SIZE: D

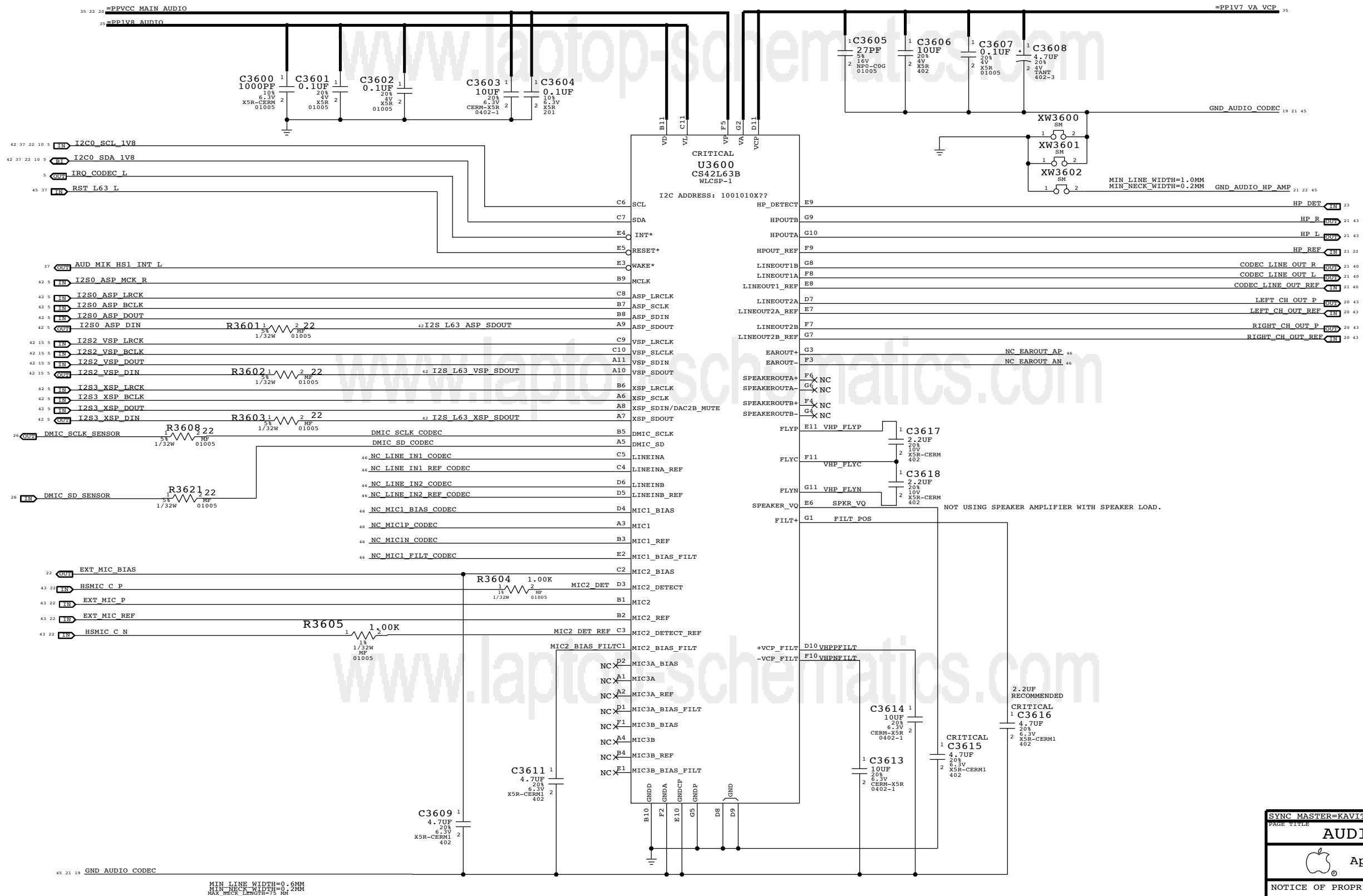
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BRANCH: 31 OF 157 SHEETS: 18 OF 48

# L63B AUDIO CODEC

APN:338S0940



MIN LINE WIDTH=0.6MM  
MIN NECK WIDTH=0.2MM  
MAX NECK LENGTH=75 MM

SYNC MASTER=KAVITHA		SYNC DATE=02/03/2011	
PAGE TITLE			
AUDIO: L63B CODEC			
Apple Inc.		DRAWING NUMBER	051-8773
		REVISION	10.0.0
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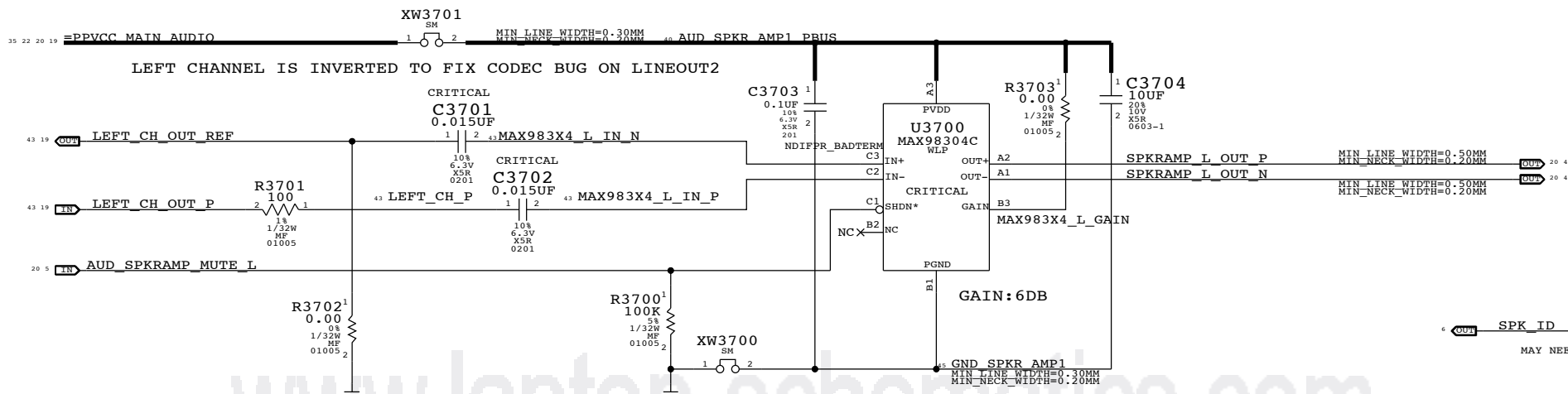
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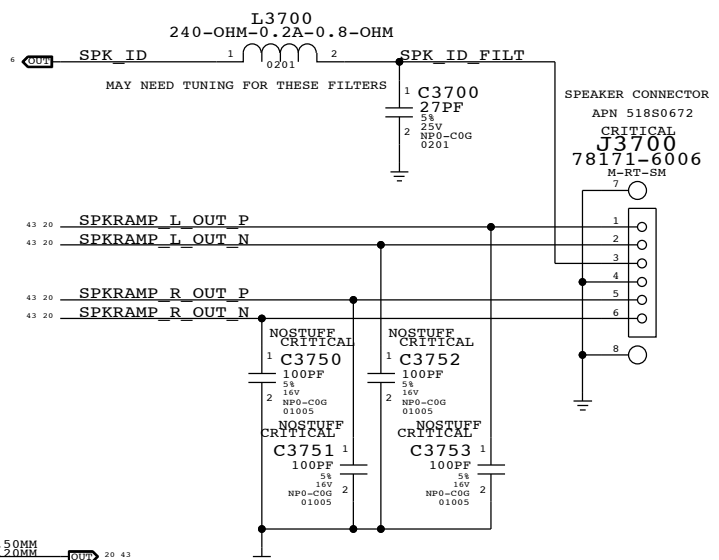
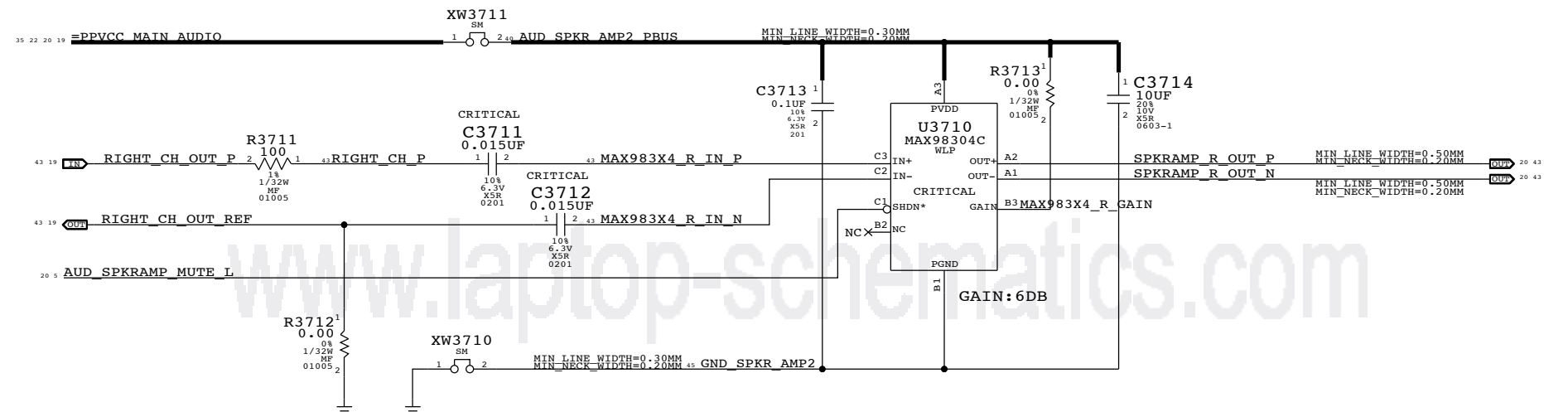
# SPEAKER AMPLIFIER

APN:353S3317)  
TURN ON TIME: 3.5MS  
75HZ +/- XXX%

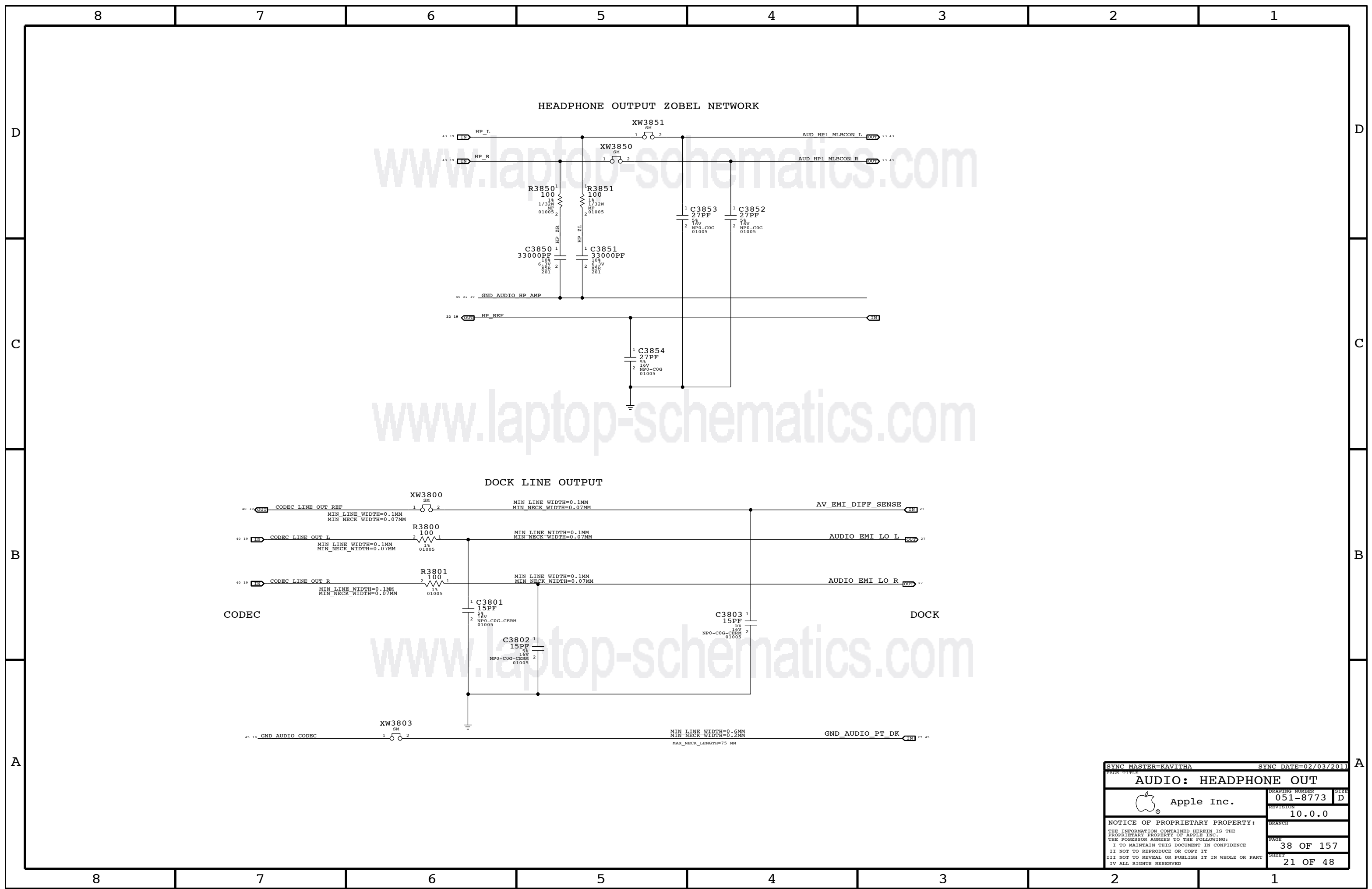
GAIN	VDD	GND
12DB	NC	SHORT
9DB	NC	100K
6DB	SHORT	NC
3DB	100K	NC
0DB	NC	NC



L63 LINEOUT2A IS CONNECTED TO U3700  
L63 LINEOUT2B IS CONNECTED TO U3710



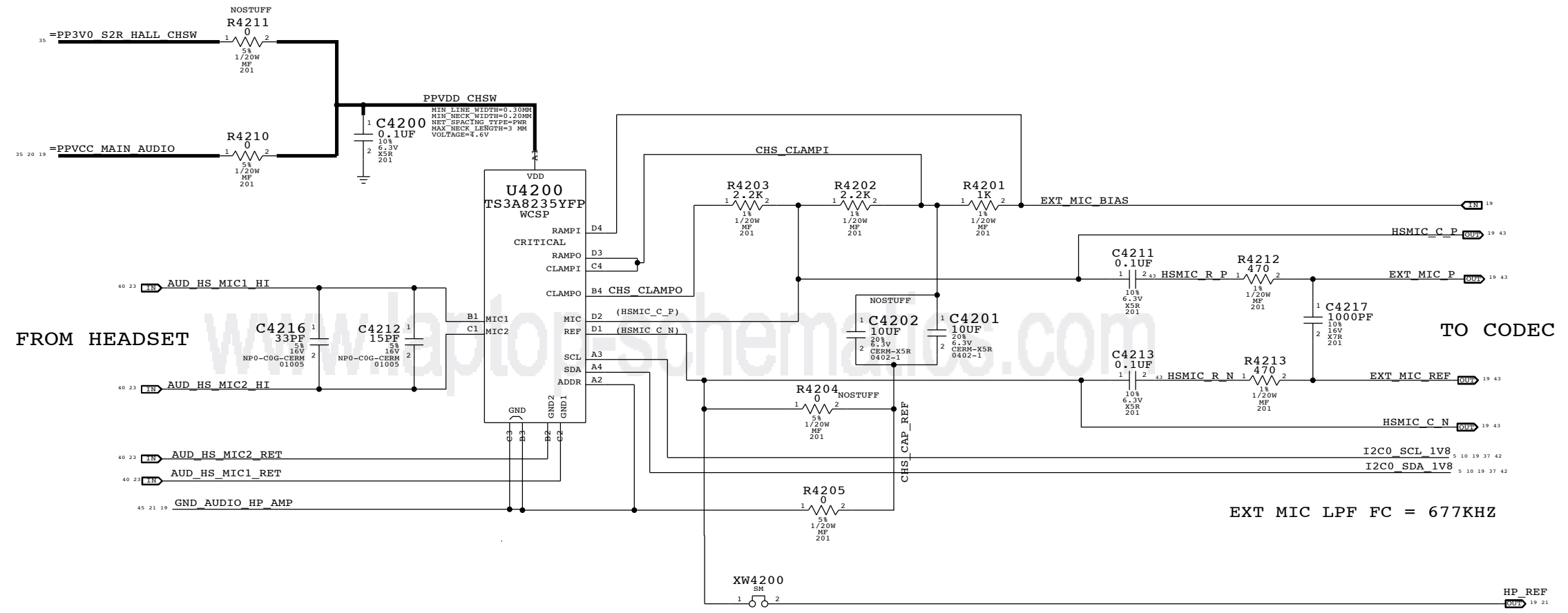
SYNC MASTER=KAVITHA		SYNC DATE=02/03/2011	
<b>AUDIO: SPEAKER AMP</b>			
Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
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		20 OF 48	



SYNC MASTER=KAVITHA		SYNC DATE=02/03/2011	
PAGE TITLE <b>AUDIO: HEADPHONE OUT</b>			
DRAWING NUMBER 051-8773		SIZE D	
REVISION 10.0.0		BRANCH	
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### EXTERNAL (HEADSET) MIC INPUT CIRCUITRY

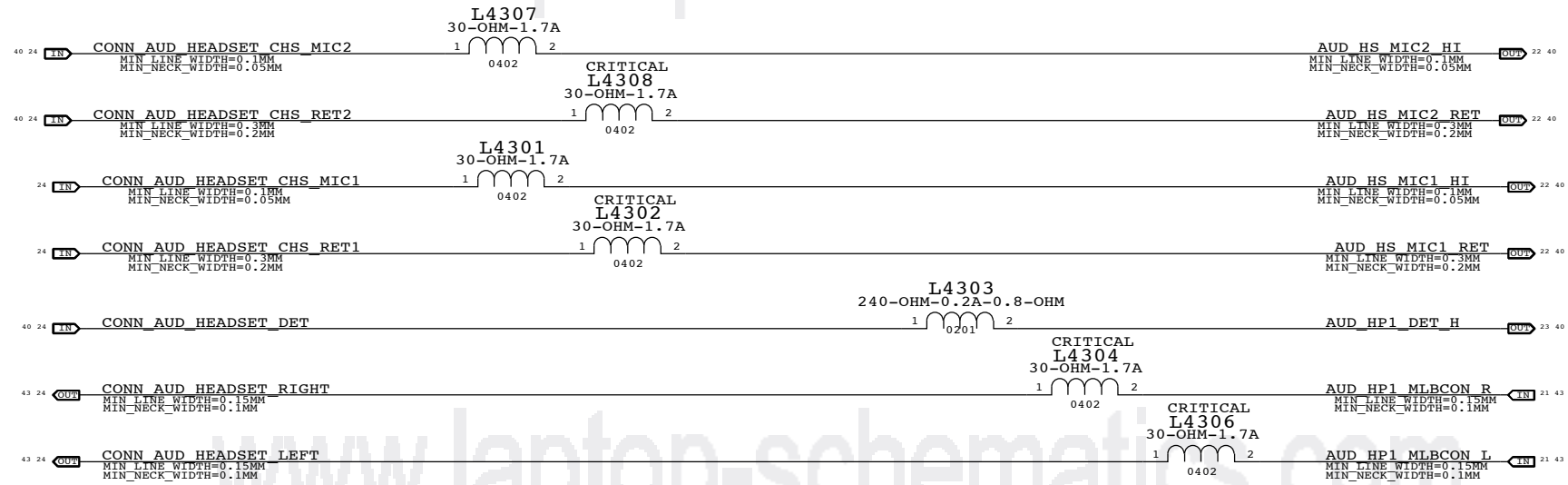


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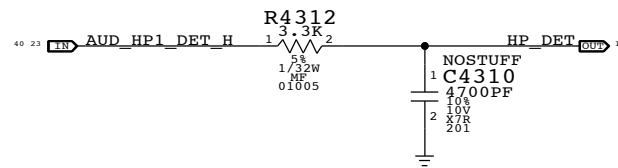
SYNC MASTER=KAVITHA		SYNC DATE=02/03/2011	
PAGE TITLE			
AUDIO: DETECT/MIC BIAS			
DRAWING NUMBER		051-8773	SIZE
REVISION		10.0.0	D
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HEADPHONE JACK CONNECTION IS ON FRONT PANEL FLEX, CSA 55/PDF 29

PLACE ALL COMPONENTS NEAR J5401



HEADSET JACK INSERTION DETECT



SYNC MASTER=KAVITHA		SYNC DATE=02/03/2011	
PAGE TITLE <b>AUDIO: HP/MIC FILTERS</b>			
DRAWING NUMBER 051-8773		SIZE D	
REVISION 10.0.0		BRANCH	
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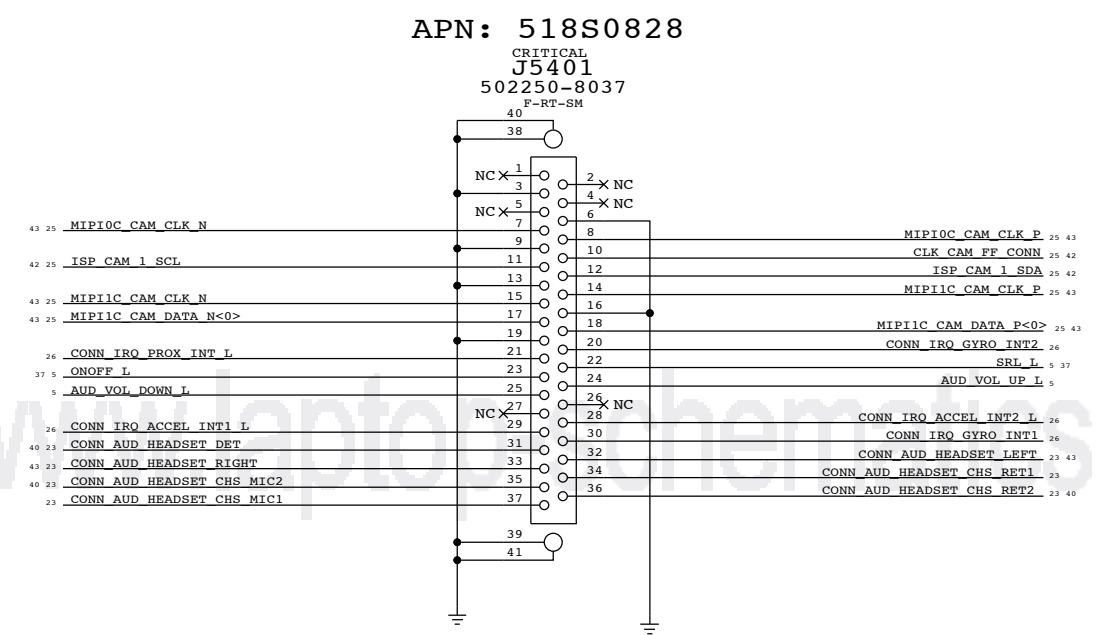
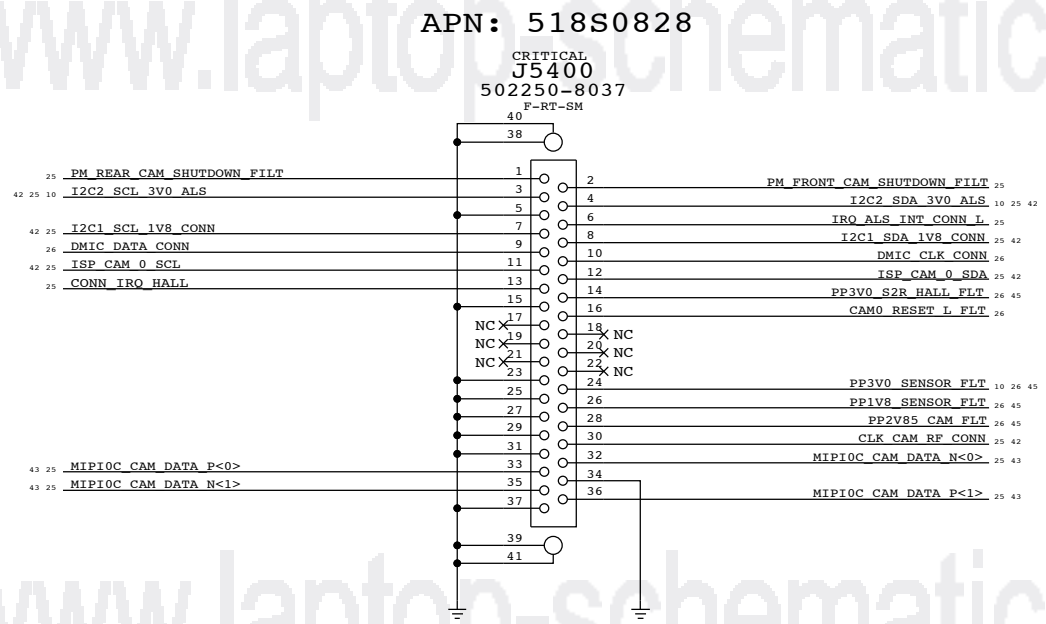
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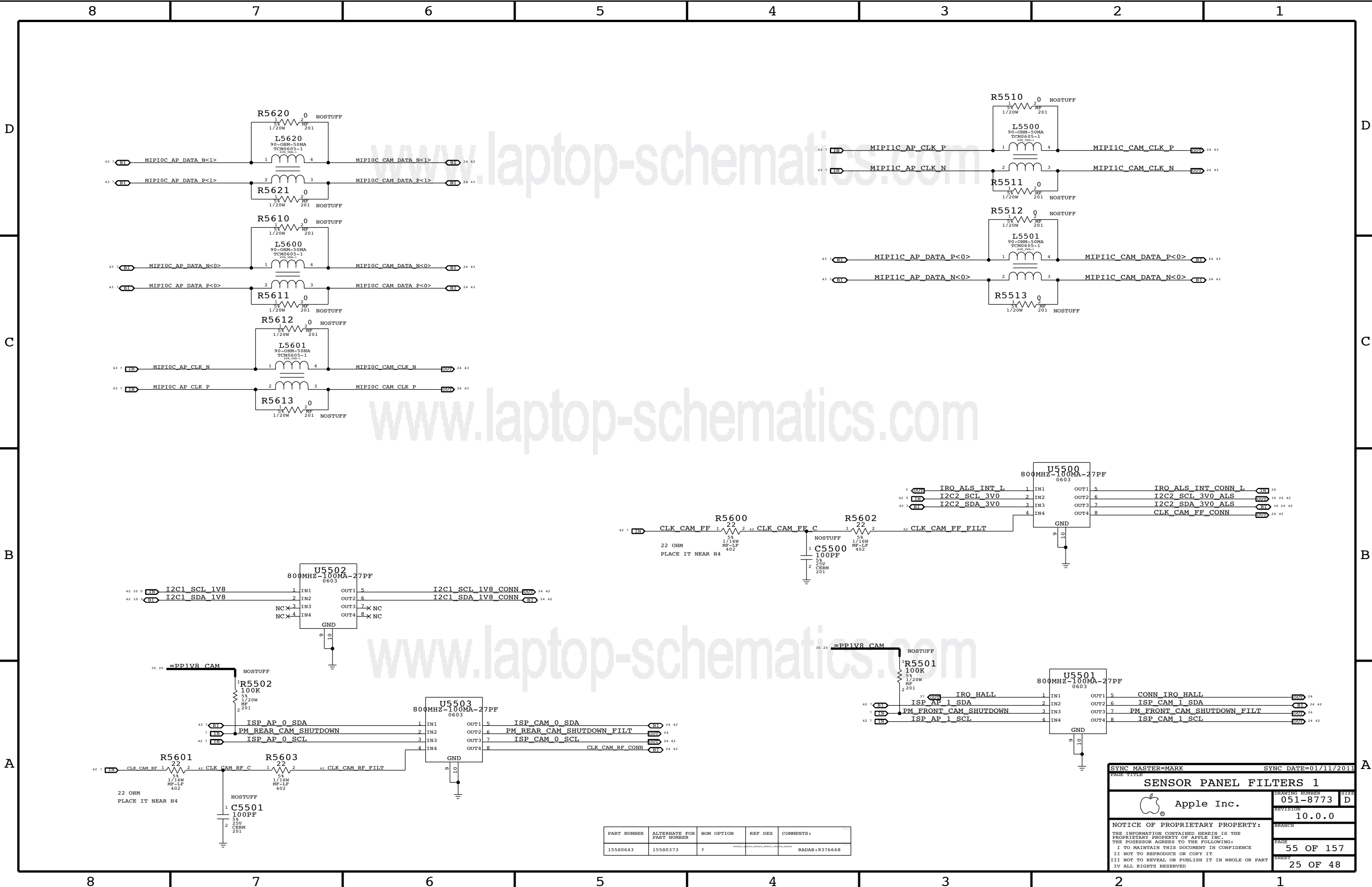
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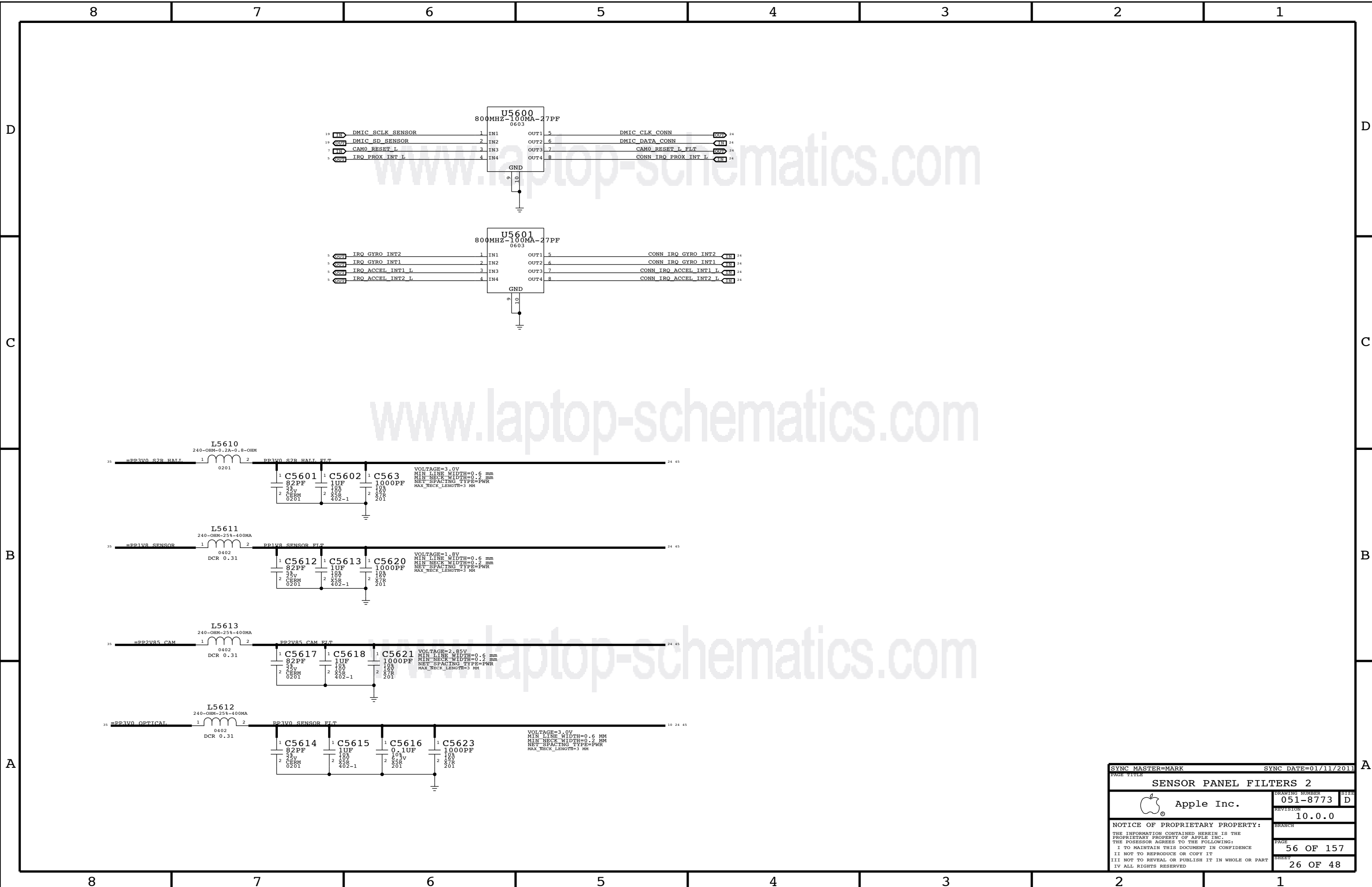


SYNC MASTER=MARK		SYNC DATE=01/11/2011	
PAGE TITLE			
<b>CONNECTOR: SENSOR</b>			
Apple Inc.		DRAWING NUMBER	051-8773
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		SHEET	24 OF 48
		SIZE	D

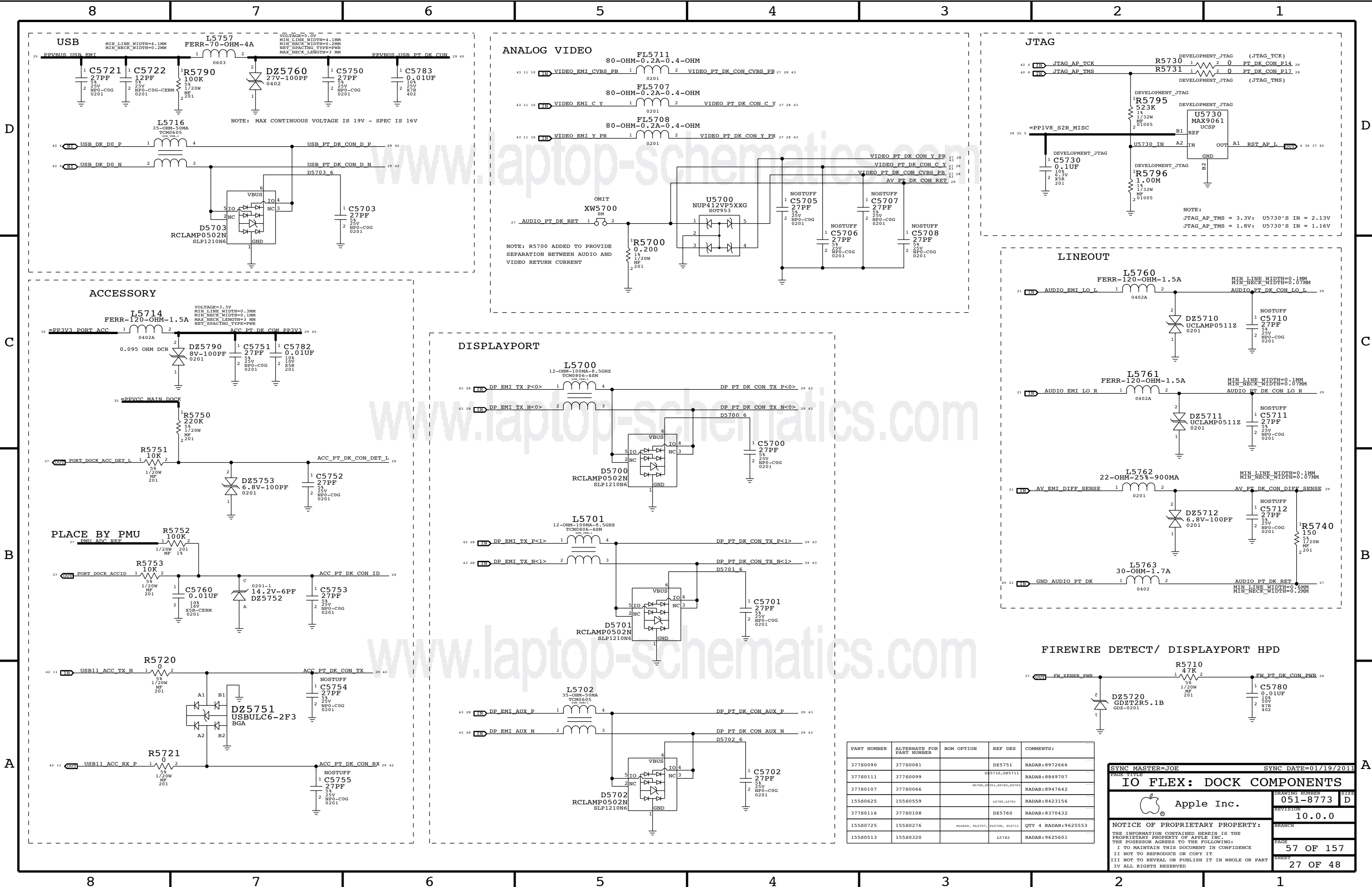


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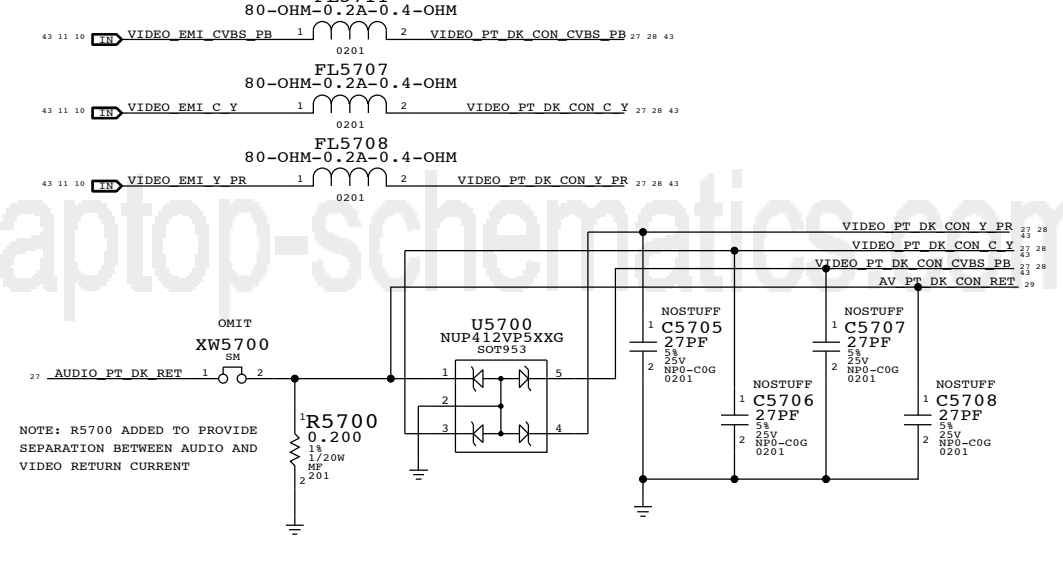
SYNC MASTER=MARK SYNC DATE=01/11/2011  
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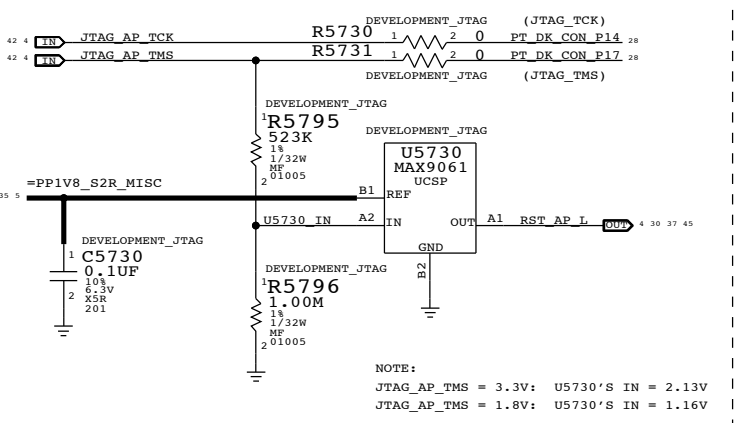
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	REVISION	10.0.0	
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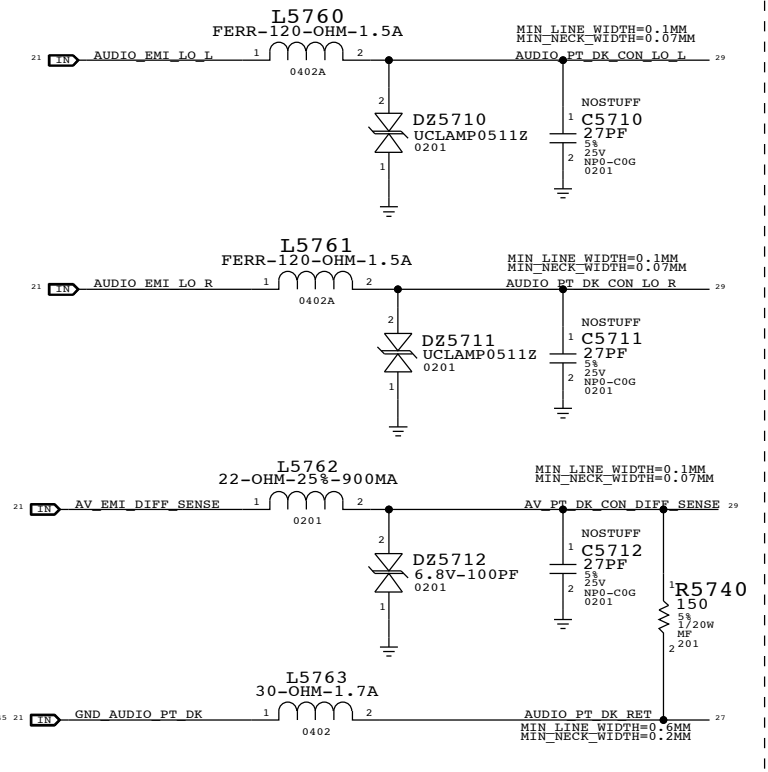
**ANALOG VIDEO**



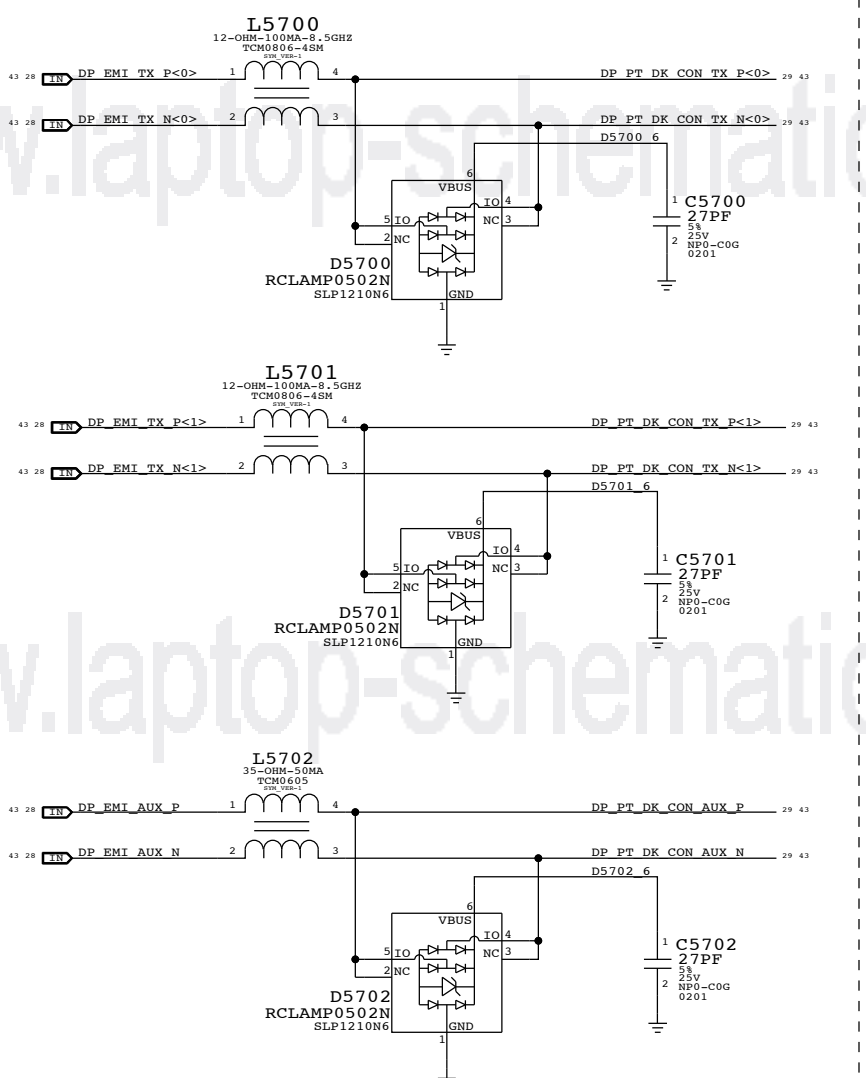
**JTAG**



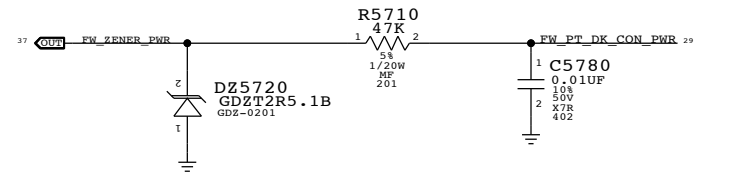
**LINEOUT**



**DISPLAYPORT**



**FIREWIRE DETECT/ DISPLAYPORT HPD**



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
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37780107	37780066		D5700,D5701,D5702,D5703	RADAR:8947642
15580625	15580559		L5700,L5701	RADAR:8423156
37780116	37780108		D25760	RADAR:8370432
15580725	15580276	FL6000, FL5707, FL5708, FL5711	QTY 4	RADAR:9625553
15580513	15580320		L5762	RADAR:9625601

SYNC MASTER=JOE SYNC DATE=01/19/2011

**IO FLEX: DOCK COMPONENTS**

Apple Inc.

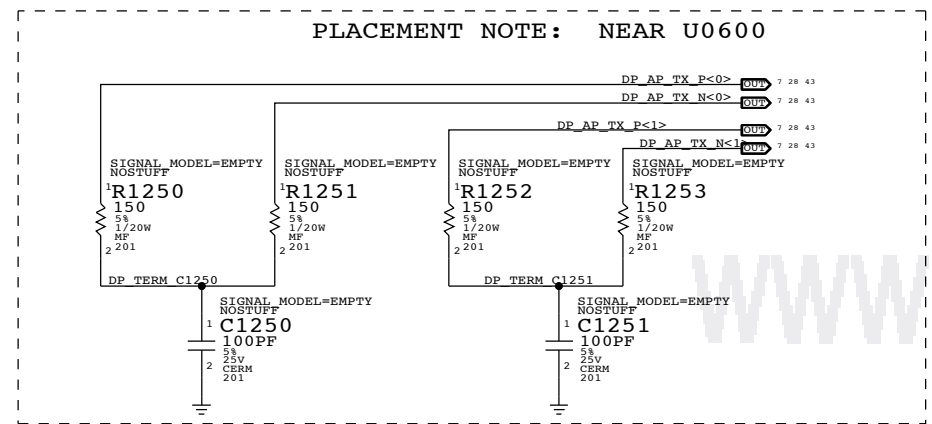
DRAWING NUMBER: 051-8773 SIZE: D

REVISION: 10.0.0

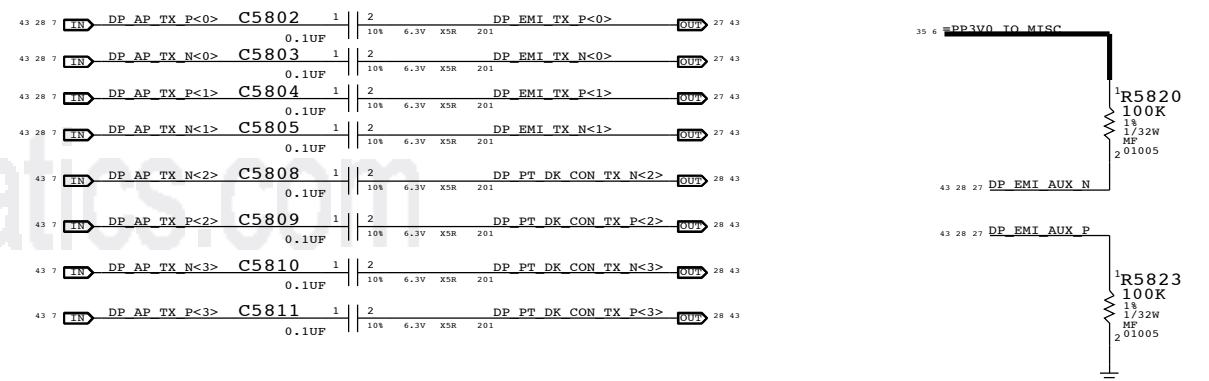
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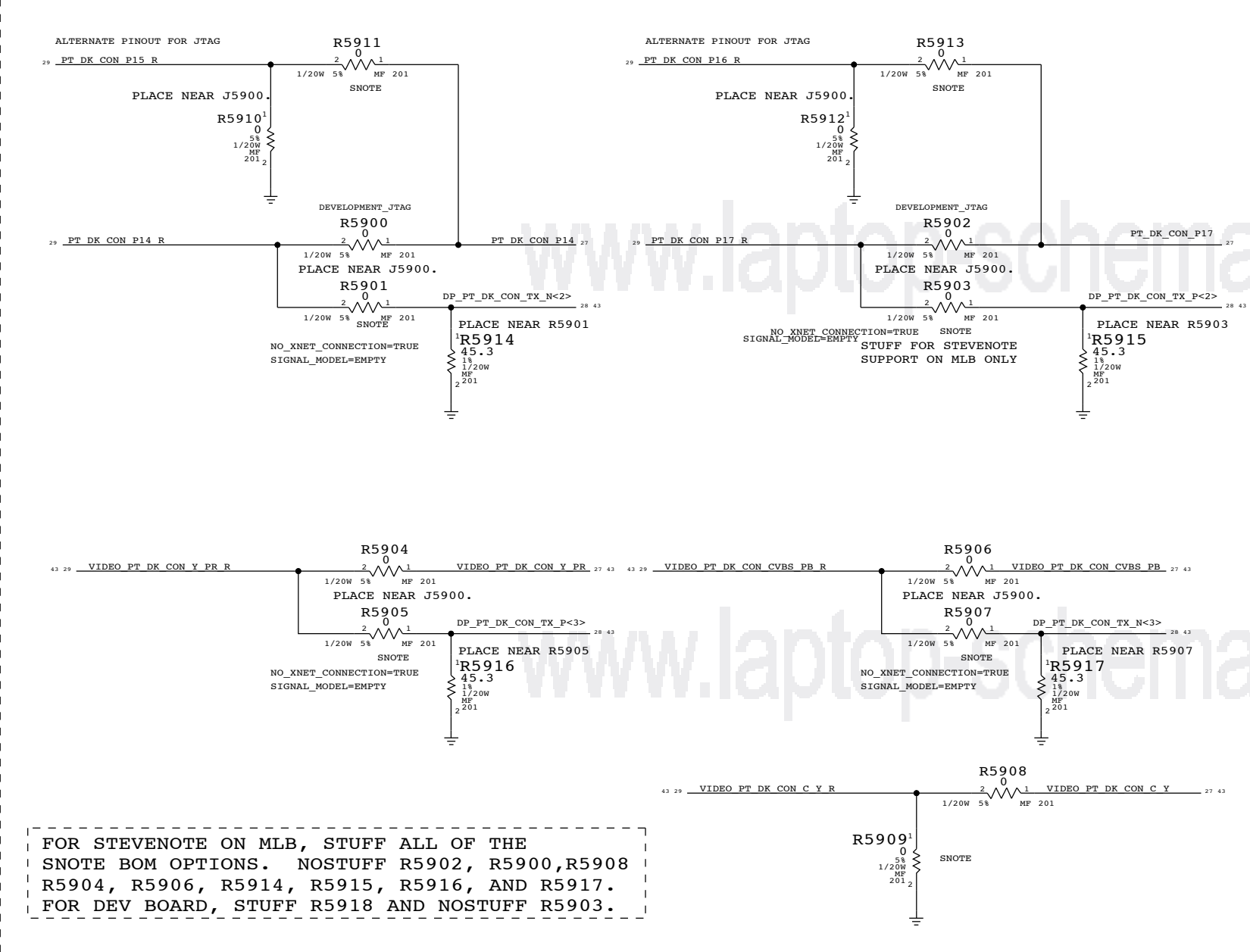
PLACEMENT NOTE: NEAR U0600



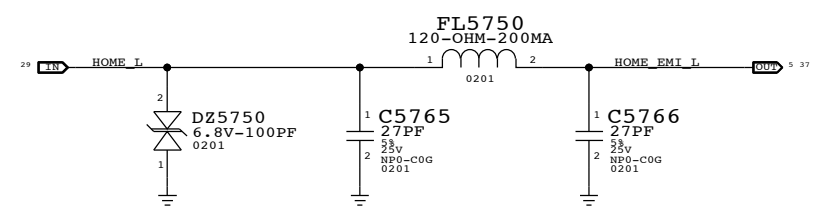
DISPLAYPORT AC COUPLING



STUFFING OPTIONS FOR DP LANES 2, 3 FOR STEVENOTE.

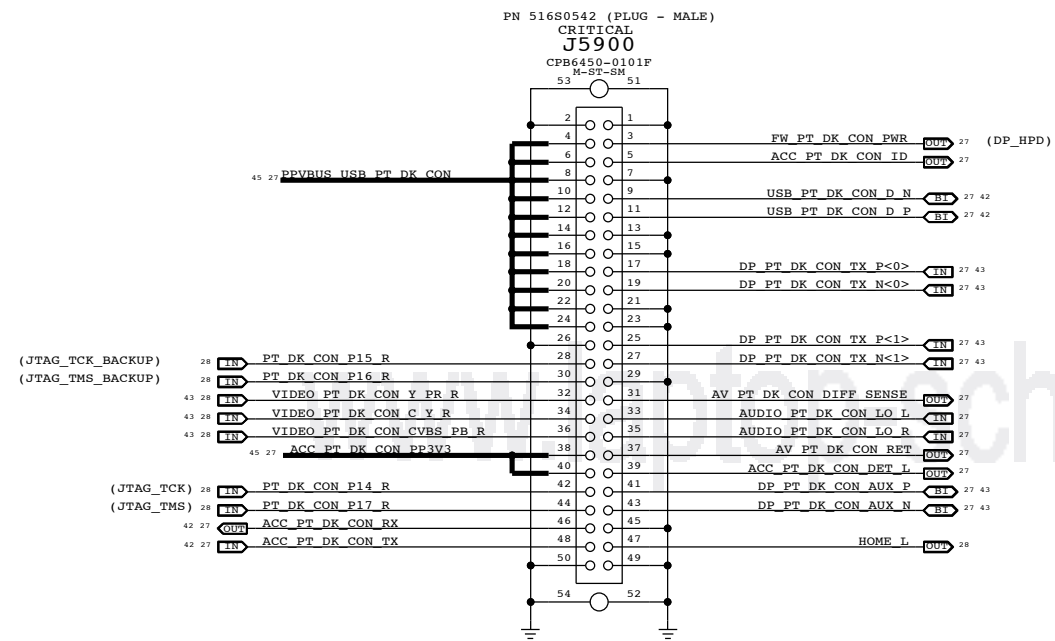


FOR STEVENOTE ON MLB, STUFF ALL OF THE SNOTE BOM OPTIONS. NOSTUFF R5902, R5900, R5908 R5904, R5906, R5914, R5915, R5916, AND R5917. FOR DEV BOARD, STUFF R5918 AND NOSTUFF R5903.



SYNC MASTER=JOE		SYNC DATE=01/19/2011	
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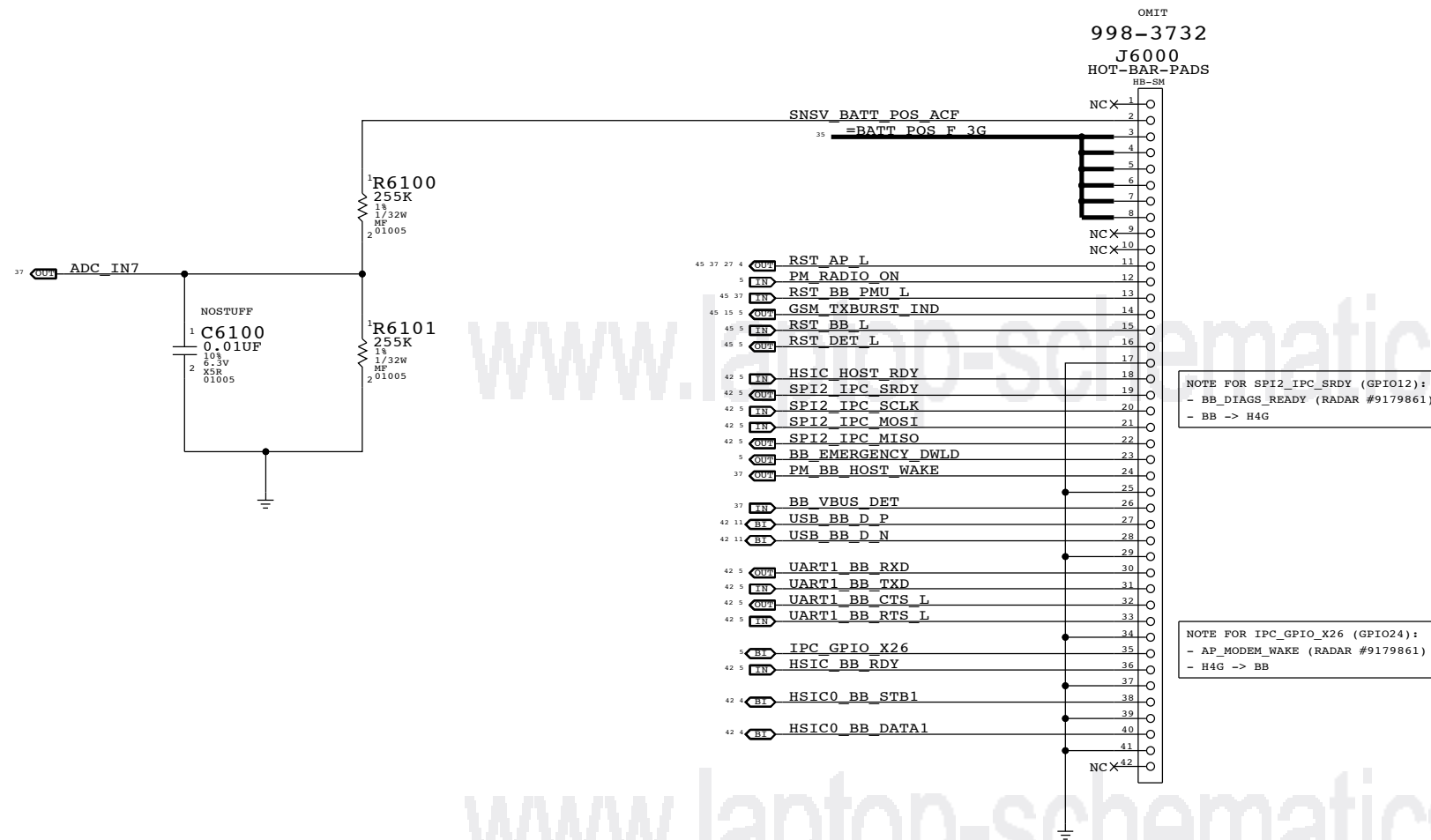
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<b>IO FLEX: B2B CONNECTOR</b>			
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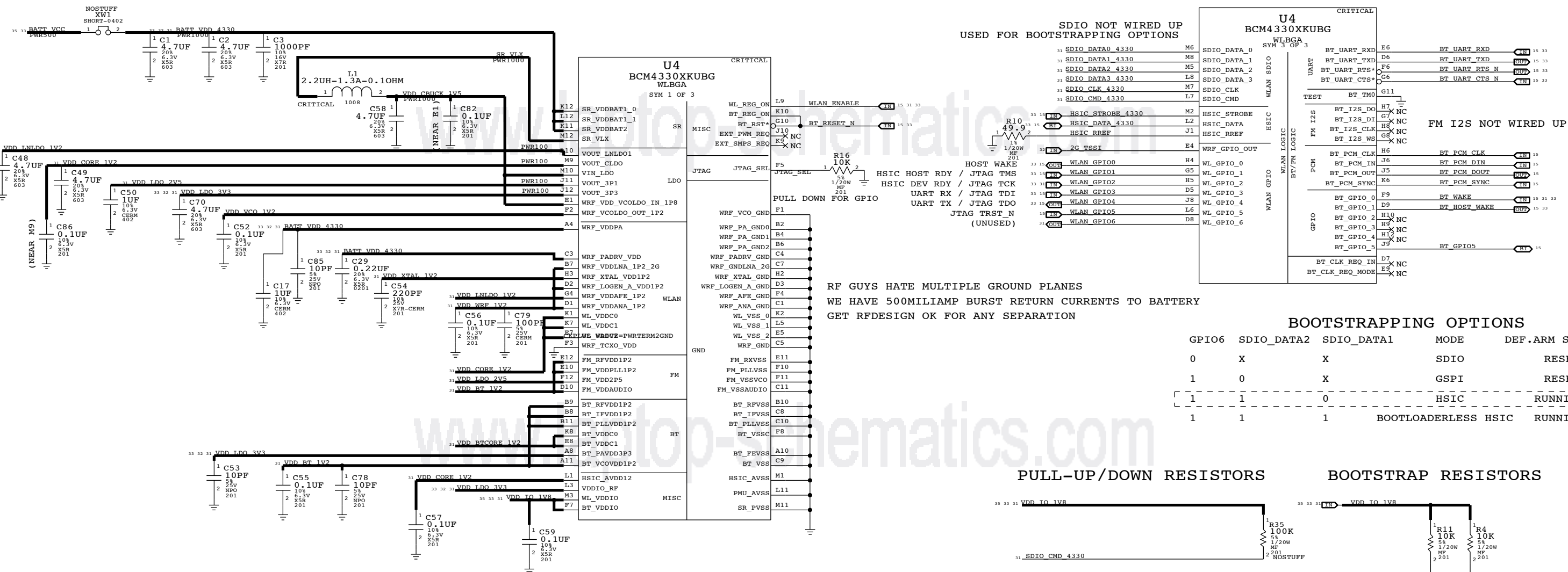
# X26 CELLULAR/GPS CONNECTOR



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<b>CONNECTOR: X26</b>			
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	REVISION	10.0.0	
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# WLAN/BT POWER

# WLAN/BT BASEBAND

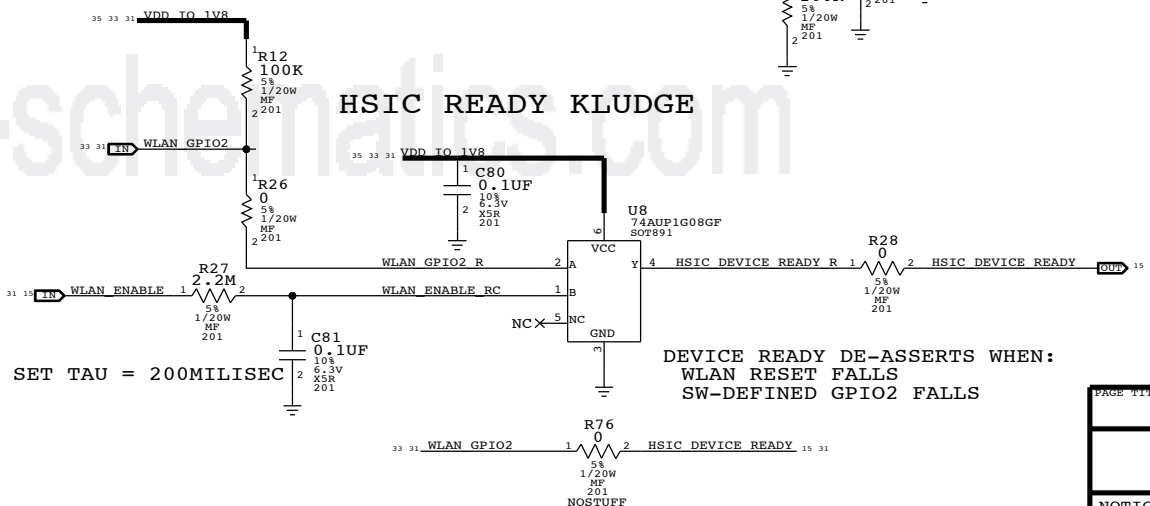
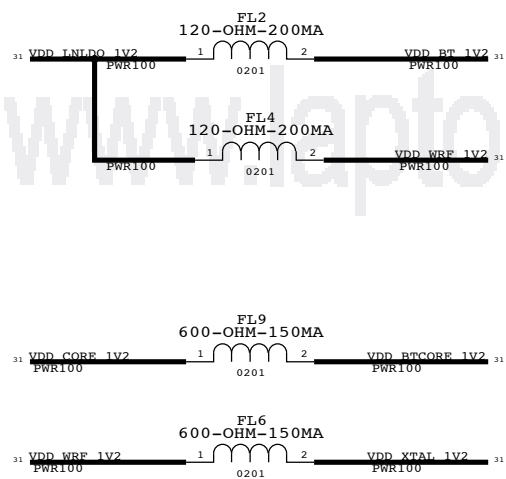


RF GUYS HATE MULTIPLE GROUND PLANES  
WE HAVE 500MILIAMP BURST RETURN CURRENTS TO BATTERY  
GET RFDESIGN OK FOR ANY SEPARATION

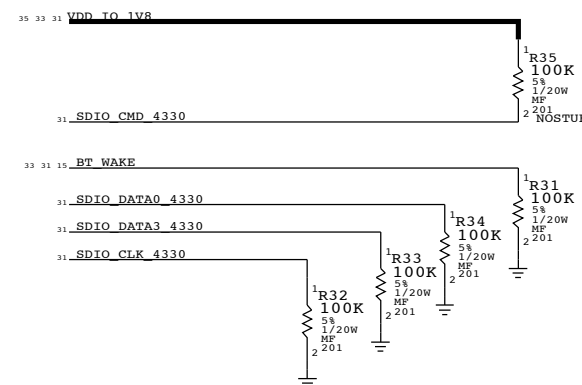
### ALTERNATE PARTS AVAILABLE:

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
31180548	31180398	ANDGATE_TI	U8	TI
15580657	15580537	FERRITE_TY	FL2,FL4	TAIYO YUDEN
15580337	15580444	FERRITE_TDK	FL6,FL9	TDK

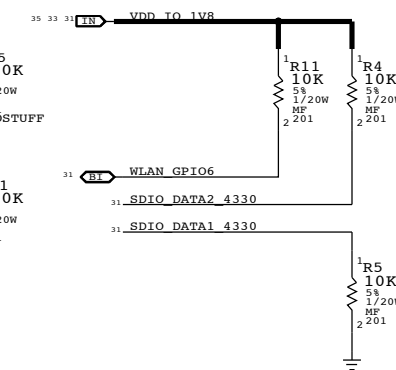
### SUPPLY FILTERING



### PULL-UP/DOWN RESISTORS



### BOOTSTRAP RESISTORS

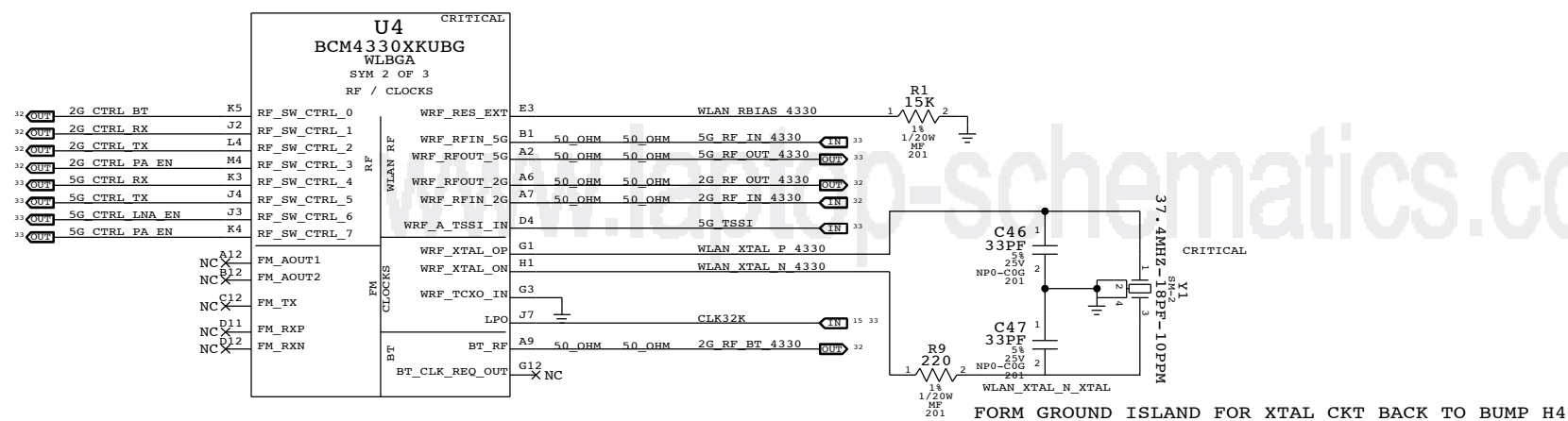


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		REVISION	10.0.0
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RF I/O PLAN

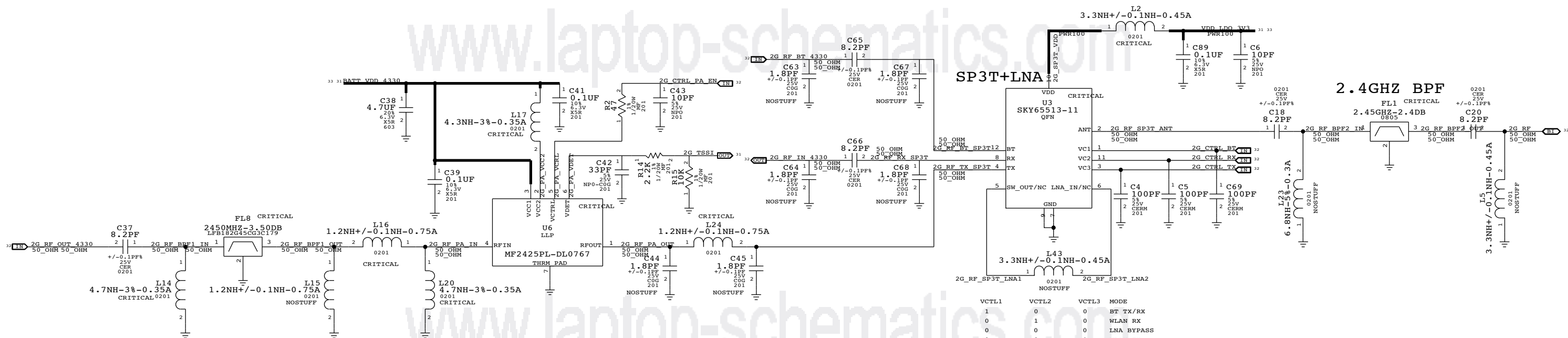
RF\_SW\_CTRL\_0: 2G\_CTRL\_BT  
 RF\_SW\_CTRL\_1: 2G\_CTRL\_RX  
 RF\_SW\_CTRL\_2: 2G\_CTRL\_TX  
 RF\_SW\_CTRL\_3: 2G\_CTRL\_PA\_EN  
 RF\_SW\_CTRL\_4: 5G\_CTRL\_RX  
 RF\_SW\_CTRL\_5: 5G\_CTRL\_TX  
 RF\_SW\_CTRL\_6: 5G\_CTRL\_LNA\_EN  
 RF\_SW\_CTRL\_7: 5G\_CTRL\_PA\_EN

WLAN TRANSCEIVER



2.4GHZ TX

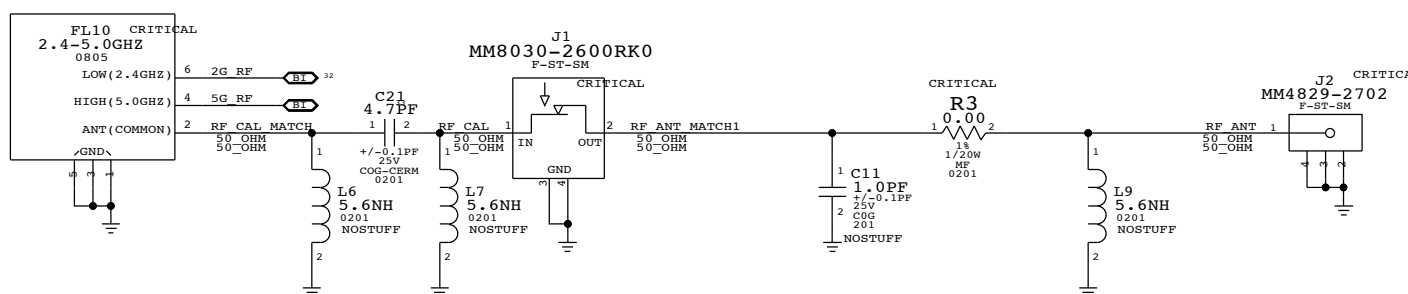
2.4GHZ RX + T/R SWITCH



2.4GHZ/5GHZ DIPLEXER

CONDUCTED TEST PORT

ANTENNA CONNECTOR



PAGE TITLE <b>WLAN 2.4GHZ AND ANT</b>		
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# 5GHZ FRONT-END CONTROL

VCRL1	VCTL2	PA_EN	LNA_EN	MODE
1	0	0	1	RX SUPERBYPASS MODE -- 26DB GAIN STEP
0	1	0	1	RX
1	0	1	0	TX

## 5GHZ LNA

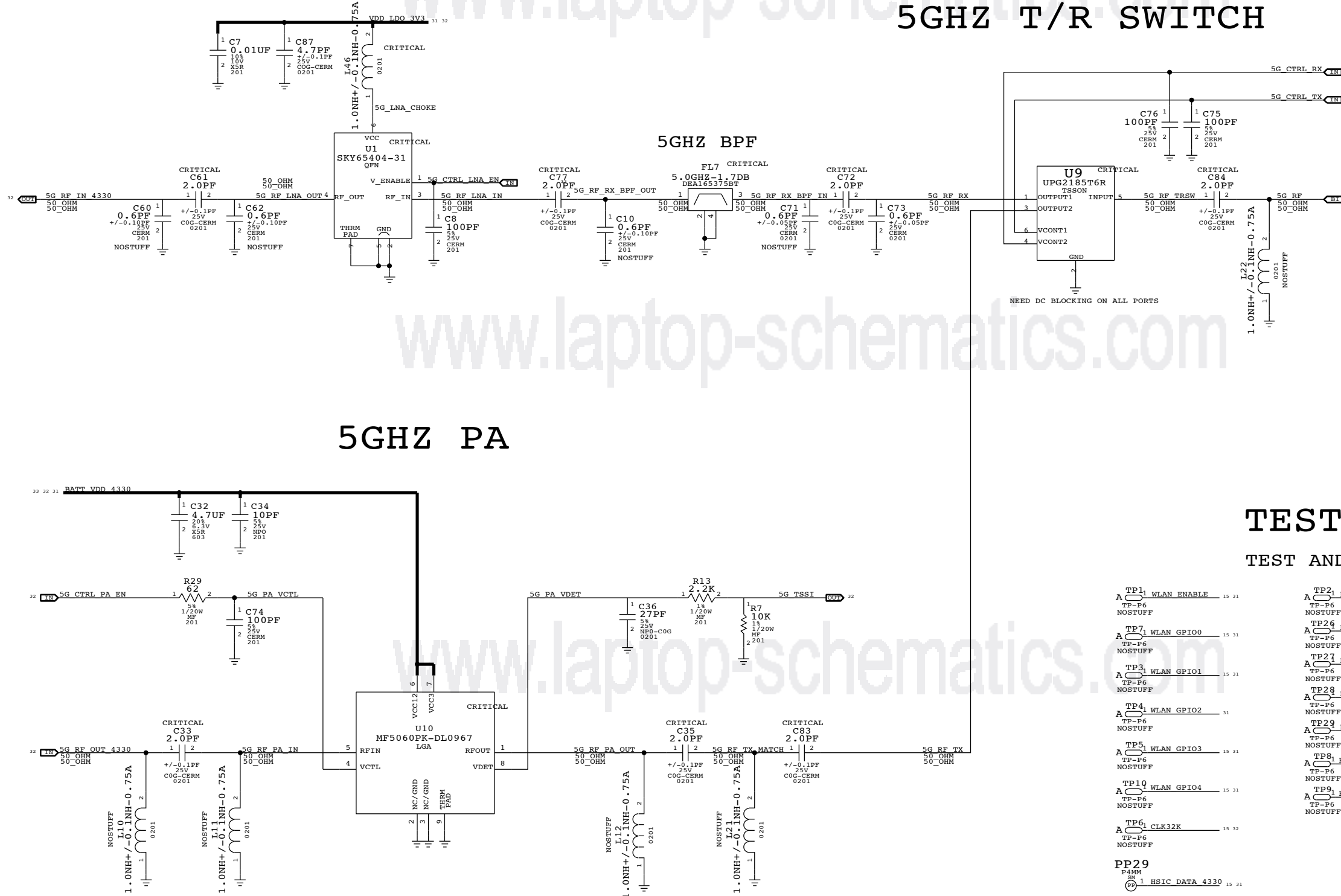
## 5GHZ T/R SWITCH

## 5GHZ BPF

## 5GHZ PA

## TEST POINTS

### TEST AND PROBE POINTS

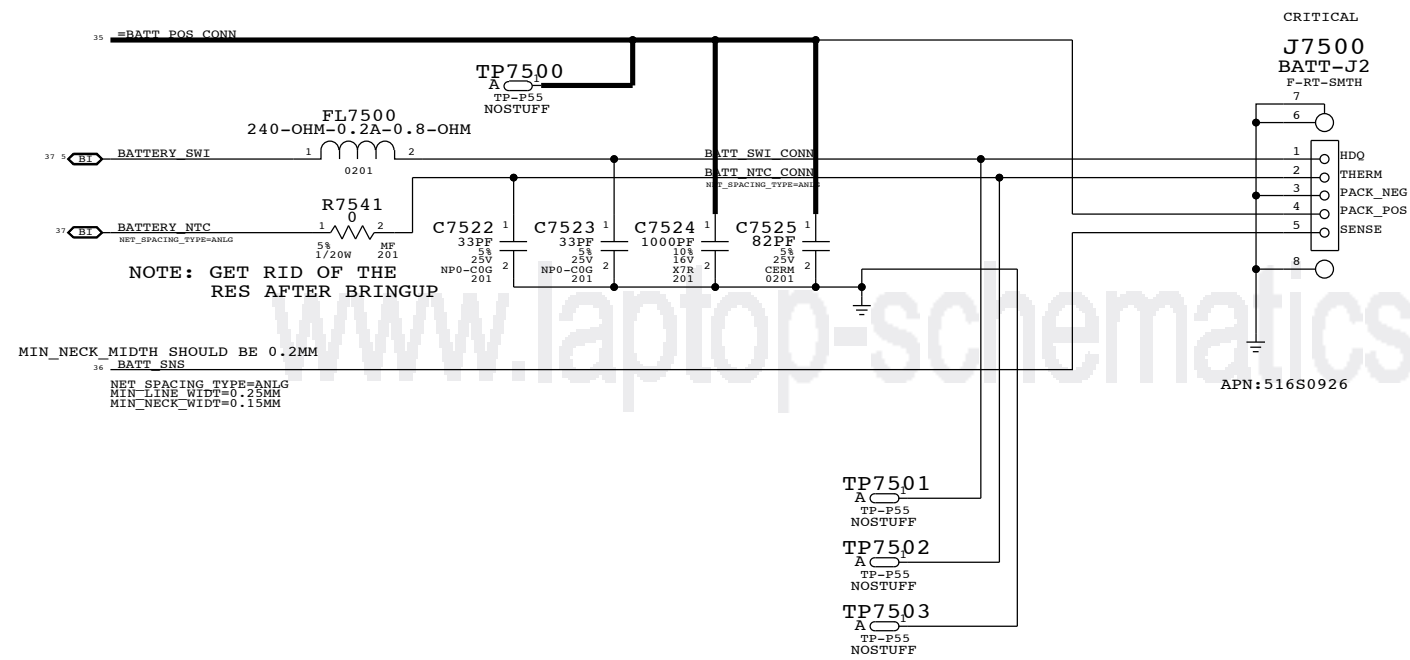


- TP1 WLAN ENABLE 15 31
- TP2 BT RESET N 15 31
- TP3 WLAN GPIO0 15 31
- TP4 WLAN GPIO1 31
- TP5 WLAN GPIO2 15 31
- TP6 WLAN GPIO3 15 31
- TP7 WLAN GPIO4 15 31
- TP8 BT HOST WAKE 15 31
- TP9 BT WAKE 15 31
- TP10 BT UART TXD 15 31
- TP11 BT UART RXD 15 31
- TP12 BT UART RTS N 15 31
- TP13 BT UART CTS N 15 31
- TP14 BT WAKE 15 31
- TP15 BATT VCC 31 35
- TP16 BATT VDD 4330 31 32 33
- TP17 VDD IO 1VB 31 35

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WLAN 5GHZ AND TEST POINTS		051-8773	D
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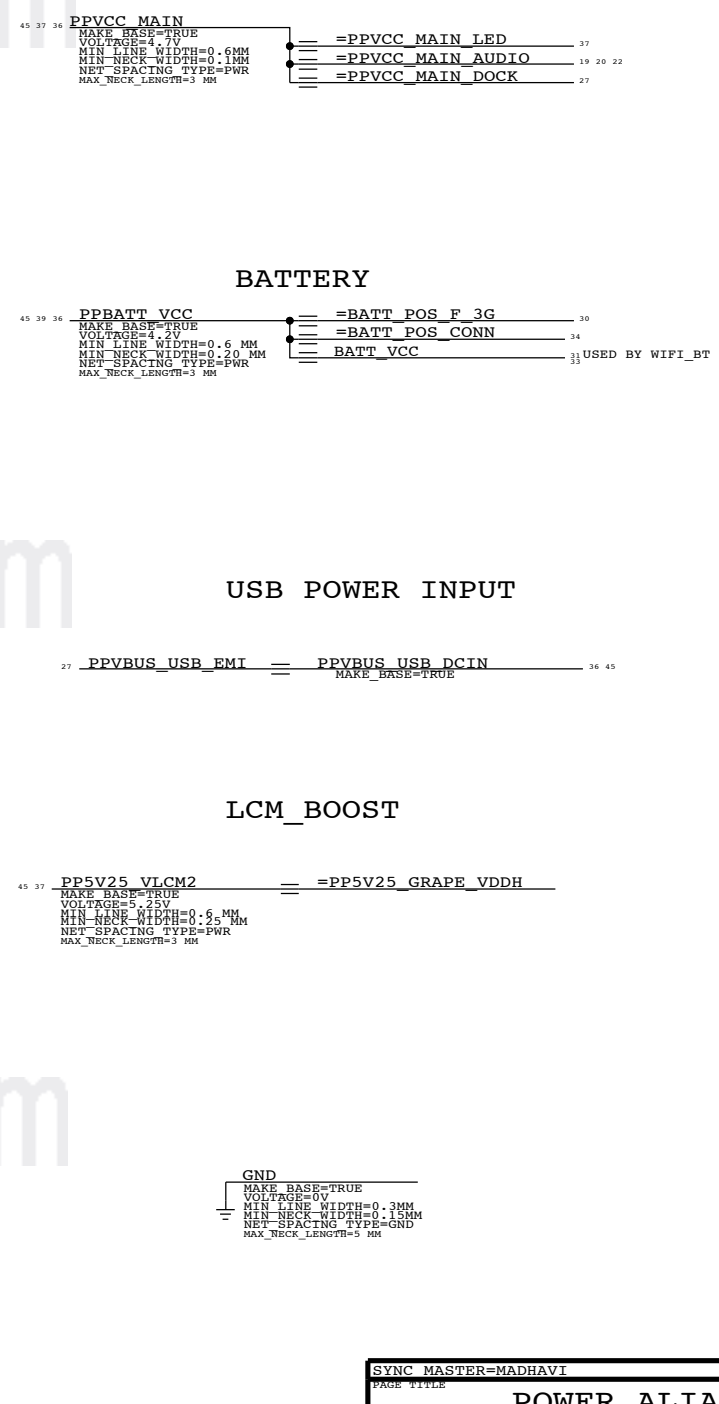
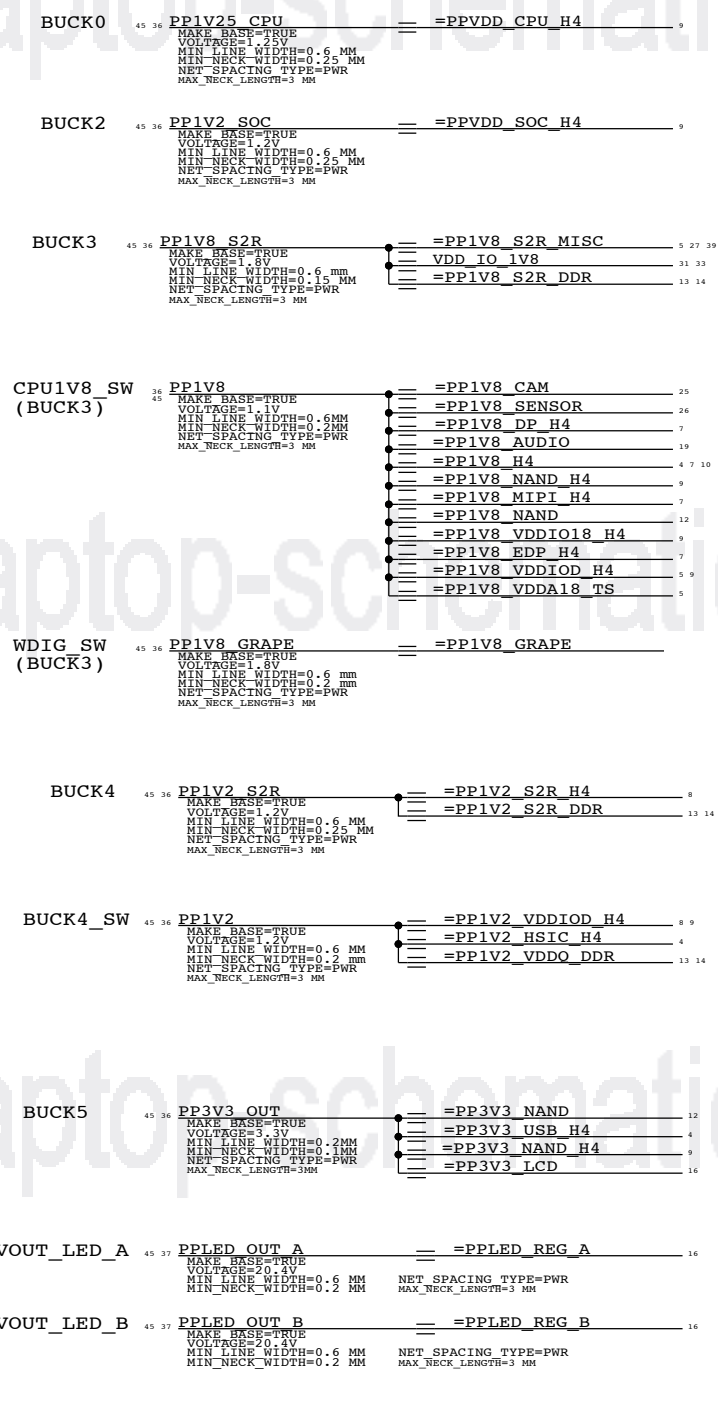
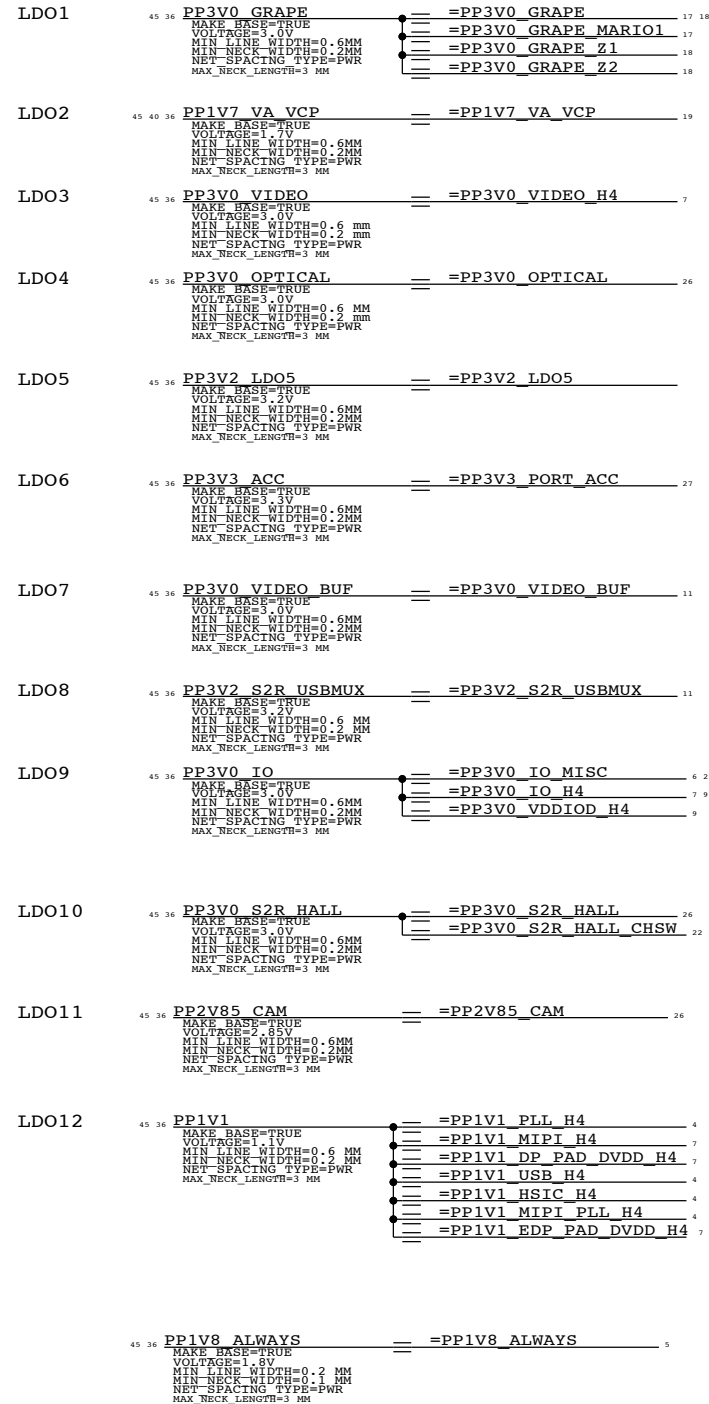
SYNC MASTER=MADHAVI		SYNC DATE=01/13/2011	
PAGE TITLE <b>POWER: BATTERY CONNECTOR</b>			
DRAWING NUMBER 051-8773		SIZE D	
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# POWER CONN / ALIAS

## LDO RAILS PROGRAMMABLE ON/OFF

## BUCK RAILS

## CHARGER MAIN

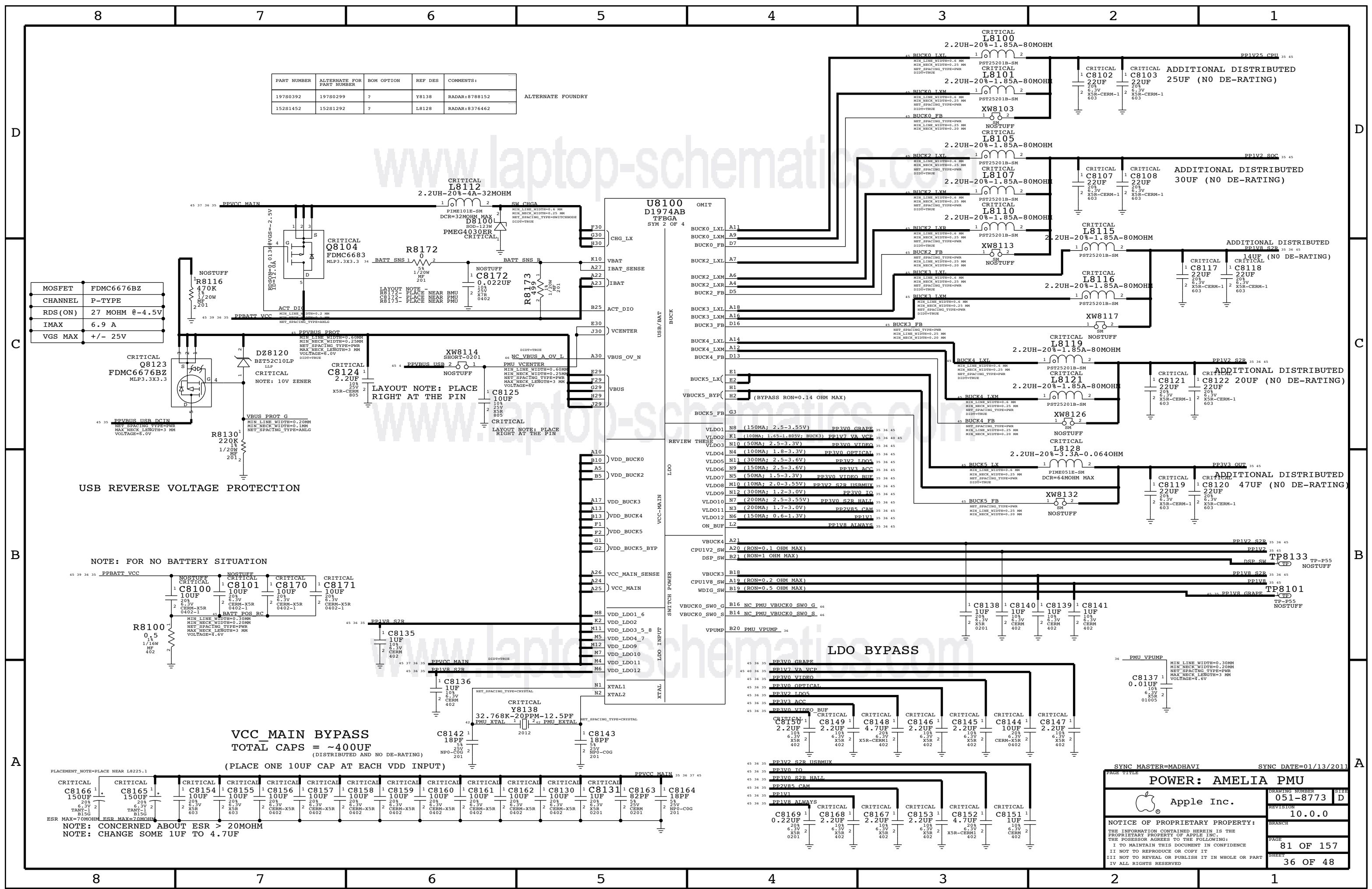


SYNC MASTER=MADHAVI		SYNC DATE=01/13/2011	
<b>POWER ALIASES</b>			
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		PAGE	80 OF 157
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
19780392	19780299	?	Y8138	RADAR:8788152
15281452	15281292	?	L8128	RADAR:8376462

ALTERNATE FOUNDRY

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
19780392	19780299	?	Y8138	RADAR:8788152
15281452	15281292	?	L8128	RADAR:8376462



PARAMETER	VALUE
MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	27 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
19780392	19780299	?	Y8138	RADAR:8788152
15281452	15281292	?	L8128	RADAR:8376462

USB REVERSE VOLTAGE PROTECTION

NOTE: FOR NO BATTERY SITUATION

VCC MAIN BYPASS  
TOTAL CAPS = ~400UF  
(DISTRIBUTED AND NO DE-RATING)

(PLACE ONE 10UF CAP AT EACH VDD INPUT)

CAPACITOR	VALUE	TYPE	REF DES
C8166	150UF	CRITICAL	
C8165	150UF	CRITICAL	
C8154	10UF	CRITICAL	
C8155	10UF	CRITICAL	
C8156	10UF	CRITICAL	
C8157	10UF	CRITICAL	
C8158	10UF	CRITICAL	
C8159	10UF	CRITICAL	
C8160	10UF	CRITICAL	
C8161	10UF	CRITICAL	
C8162	10UF	CRITICAL	
C8130	10UF	CRITICAL	
C8131	10UF	CRITICAL	
C8163	82PF	CRITICAL	
C8164	18PF	CRITICAL	

NOTE: CONCERNED ABOUT ESR > 20MOHM  
NOTE: CHANGE SOME 1UF TO 4.7UF

POWER: AMELIA PMU

Apple Inc.

DRAWING NUMBER: 051-8773

REVISION: 10.0.0

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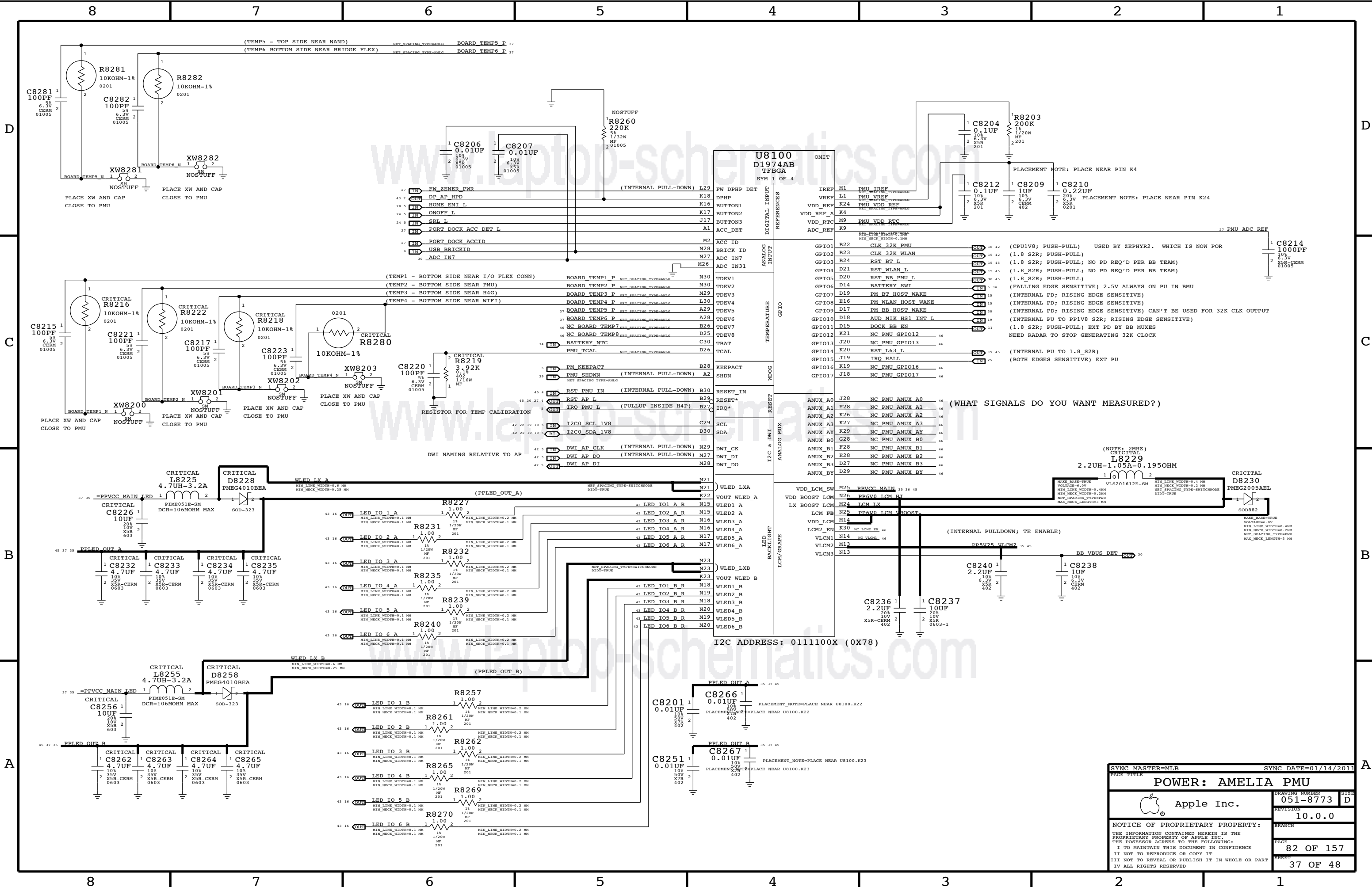
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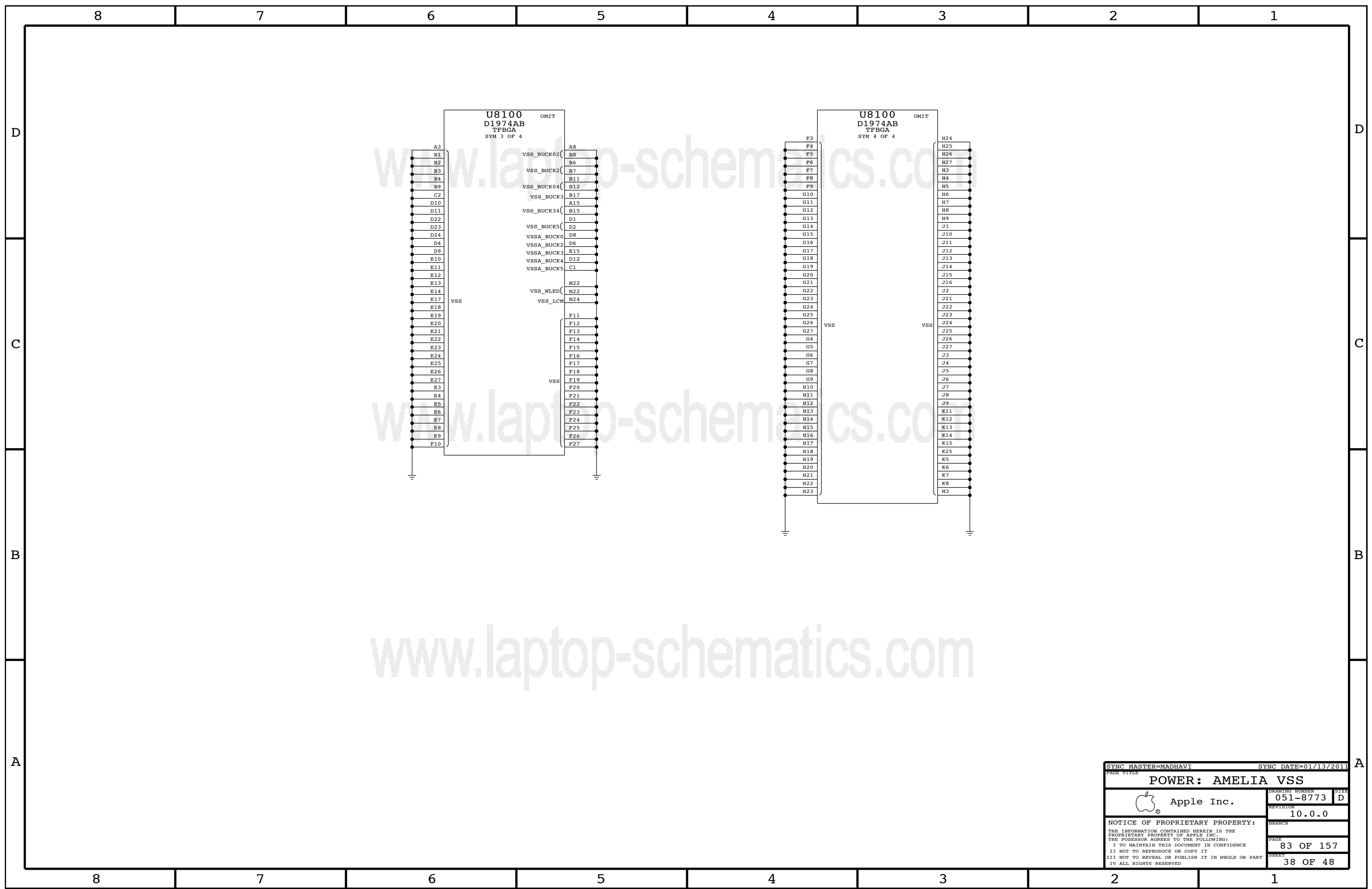
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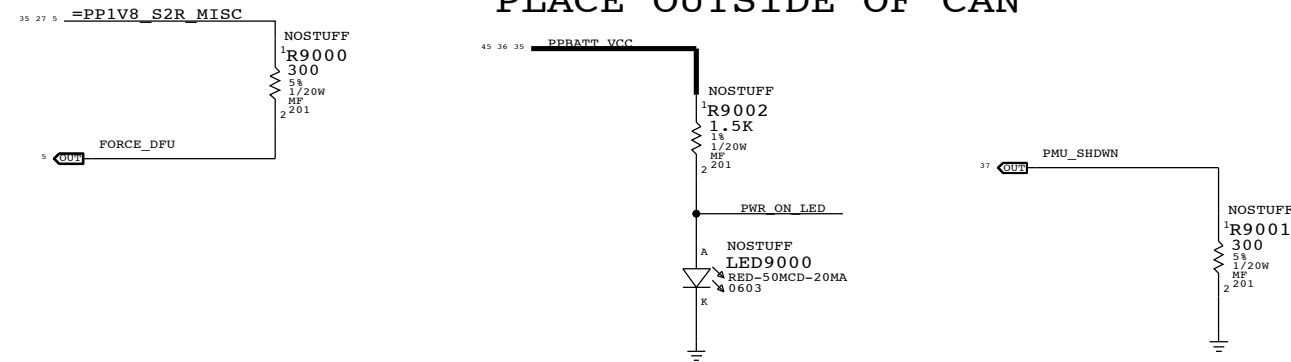
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SYNC MASTER=MADHAVI		SYNC DATE=01/13/2011	
<b>POWER: AMELIA VSS</b>			
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# DEBUG RESET ACCESS

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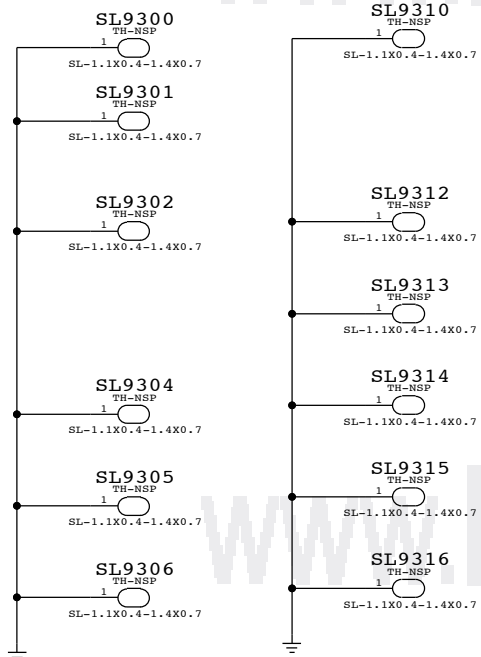
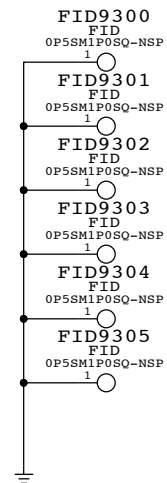
3

2

1

PLATED THROUGH HOLES

DRILL SIZE: 1.1MM X 0.4MM  
PLATING SIZE: 1.4MM X 0.7MM



PROBE POINTS

- PP0  
P4MM  
SK  
1 CODEC\_LINE\_OUT\_REF 19 21
- PP1  
P4MM  
SK  
1 CODEC\_LINE\_OUT\_R 19 21
- PP2  
P4MM  
SK  
1 AUD\_SPKR\_AMP2\_PBUS 20
- PP3  
P4MM  
SK  
1 AUD\_SPKR\_AMP1\_PBUS 20
- PP4  
P4MM  
SK  
1 CODEC\_LINE\_OUT\_L 19 21
- PP5  
P4MM  
SK  
1 DDR0\_DQS\_P<0> 8 13 44
- PP6  
P4MM  
SK  
1 DDR0\_DQ<0> 8 13 44
- PP7  
P4MM  
SK  
1 DDR0\_DQS\_N<0> 8 13 44
- PP8  
P4MM  
SK  
1 DDR0\_DQS\_N<1> 8 13 44
- PP9  
P4MM  
SK  
1 DDR0\_DQ<14> 8 13 44
- PP10  
P4MM  
SK  
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- PP11  
P4MM  
SK  
1 HSD1\_WLAN\_STB1 4 15 42
- PP12  
P4MM  
SK  
1 Z1\_BON\_L<5> 17 18
- PP13  
P4MM  
SK  
1 Z1\_B\_ADR<2> 17 18
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P4MM  
SK  
1 Z1\_B\_ADR<1> 17 18
- PP15  
P4MM  
SK  
1 Z1\_B\_ADR<0> 17 18
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SK  
1 Z1\_MISO 17 18
- PP17  
P4MM  
SK  
1 Z1\_BON\_L<4> 17 18
- PP18  
P4MM  
SK  
1 PPIV7\_VA\_VCP 35 36 45
- PP19  
P4MM  
SK  
1 CONN\_AUD\_HEADSET\_CHS\_RET2 23 24
- PP20  
P4MM  
SK  
1 CONN\_AUD\_HEADSET\_CHS\_MIC2 23 24
- PP21  
P4MM  
SK  
1 CONN\_AUD\_HEADSET\_DET 23 24
- PP22  
P4MM  
SK  
1 AUD\_HP1\_DET\_H 23
- PP23  
P4MM  
SK  
1 AUD\_HS\_MIC2\_RET 22 23
- PP24  
P4MM  
SK  
1 AUD\_HS\_MIC1\_HI 22 23
- PP25  
P4MM  
SK  
1 AUD\_HS\_MIC1\_RET 22 23
- PP26  
P4MM  
SK  
1 AUD\_HS\_MIC2\_HI 22 23

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1

# MLB CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM	NO_TYPE, BGA, BGA06-06	MM	16.2

## PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

### SINGLE-ENDED PHYSICAL RULES

#### 45 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	ISL1, ISL12	Y	0.110 MM	0.060 MM	3.0 MM		
45_OHM_SE	ISL5, ISL8	Y	0.077 MM	0.060 MM	3.0 MM		
45_OHM_SE	ISL3	Y	0.055 MM	0.050 MM	3.0 MM		
45_OHM_SE	*	N	0.055 MM	0.050 MM	3.0 MM		

#### 50 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	ISL1, ISL12	Y	0.088 MM	0.050 MM	3.0 MM		
50_OHM_SE	ISL3	Y	0.050 MM	0.050 MM	3.0 MM		
50_OHM_SE	ISL5, ISL8	Y	0.062 MM	0.050 MM	3.0 MM		
50_OHM_SE	*	N	0.050 MM	0.050 MM	3.0 MM		

## DIFFERENTIAL PAIR PHYSICAL RULES

### 90 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP, BOTTOM	Y	0.085 MM	0.085 MM		0.110 MM	0.110 MM
90_OHM_DIFF	ISL3	Y	0.051 MM	0.051 MM	=STANDARD	0.120 MM	0.120 MM
90_OHM_DIFF	ISL5, ISL8	Y	0.072 MM	0.075 MM	=STANDARD	0.120 MM	0.120 MM

### MISC PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.08 MM	0.08 MM
SPEAKER	*	Y	0.3 MM	0.19MM	10 MM	0.08 MM	0.08 MM
LED	*	Y	0.2 MM	0.10MM	10 MM	0.08 MM	0.08 MM

### BGA AREA PHYSICAL RULES

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	BGA_PHY

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BGA_PHY	*	Y	0.060 MM	0.060 MM	=STANDARD	0.076 MM	0.075 MM

## SPACING CONSTRAINTS

### DEFAULT/BGA SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.100 MM	?
STANDARD	*	=DEFAULT	?
BGA_SPA	*	=DEFAULT	?

### REGULAR SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.057 MM	?
0P08_SPACING	*	0.080 MM	?
1.5:1_SPACING	*	0.086 MM	?
2:1_SPACING	*	0.114 MM	?
2.5:1_SPACING	*	0.143 MM	?
3:1_SPACING	*	0.171 MM	?
4:1_SPACING	*	0.228 MM	?
5:1_SPACING	*	0.285 MM	?
0P5MM_SPACING	*	0.5 MM	?
0P64MM_SPACING	*	0.64 MM	?

\*NOTE: ASSUMING 0.060MM DIELECTRIC THICKNESS

### POWER/GND SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR_P1SPACING	*	0.1 MM	900
GND_P1SPACING	*	0.1 MM	950
SWITCHNODE	*	0.5 MM	1000
SWITCHNODE	TOP, BOTTOM	0.2 MM	1000

## POWER

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PWR	*	Y	0.6MM	0.25 MM	10.0 MM		
GND_PH	*	Y	0.6MM	0.075 MM	10.0 MM		

## MISC

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_SPA
CLK	*	BGA	BGA_SPA
PWR	*	*	PWR_P1SPACING
GND	*	*	GND_P1SPACING
SWITCHNODE	*	*	SWITCHNODE
ANLG	*	*	3:1_SPACING
LED	*	*	3:1_SPACING

### NOTES:

- 0.075 MM ~ 3 MIL
- 0.089 MM ~ 3.5 MIL
- 0.102 MM ~ 4 MIL
- 0.114 MM ~ 4.5 MIL
- 0.125 MM ~ 5 MIL
- 0.140 MM ~ 5.5 MIL
- 0.15 MM ~ 6 MIL
- 0.18 MM ~ 7 MIL
- 0.2 MM ~ 8 MIL
- 0.25 MM ~ 10 MIL
- 0.3 MM ~ 12 MIL
- 0.33 MM ~ 13 MIL
- 0.4 MM ~ 16 MIL
- 1.0 MM = 39.37 MIL

SYNC MASTER=MIKE		SYNC DATE=01/21/2011	
PAGE TITLE			
<b>CONSTRAINTS: MLB RULES</b>			
DRAWING NUMBER		051-8773	
REVISION		10.0.0	
BRANCH			
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Clock Signal Constraints

Table with 3 columns: NET\_PHYSICAL\_TYPE, AREA\_TYPE, PHYSICAL\_RULE\_SET. Row: CLK\_50S, \*, 50\_OHM\_SE

Table with 4 columns: NET\_SPACING\_TYPE1, NET\_SPACING\_TYPE2, AREA\_TYPE, SPACING\_RULE\_SET. Row: CLK, \*, \*, 5:1\_SPACING

Table with 4 columns: ELECTRICAL\_CONSTRAINT\_SET, PHYSICAL, NET\_TYPE, SPACING. Lists constraints for CLK\_50S, CLK\_32K, etc.

UART

Table with 3 columns: NET\_PHYSICAL\_TYPE, AREA\_TYPE, PHYSICAL\_RULE\_SET. Row: UART\_50S, \*, 50\_OHM\_SE

Table with 4 columns: NET\_SPACING\_TYPE1, NET\_SPACING\_TYPE2, AREA\_TYPE, SPACING\_RULE\_SET. Row: UART, \*, \*, 3:1\_SPACING

Table with 4 columns: ELECTRICAL\_CONSTRAINT\_SET, PHYSICAL, NET\_TYPE, SPACING. Lists constraints for UART AP RXD, TXD, MUX, etc.

SPI

Table with 3 columns: NET\_PHYSICAL\_TYPE, AREA\_TYPE, PHYSICAL\_RULE\_SET. Row: SPI\_50S, \*, 45\_OHM\_SE

Table with 4 columns: NET\_SPACING\_TYPE1, NET\_SPACING\_TYPE2, AREA\_TYPE, SPACING\_RULE\_SET. Row: SPI, \*, \*, 2:1\_SPACING

Table with 4 columns: ELECTRICAL\_CONSTRAINT\_SET, PHYSICAL, NET\_TYPE, SPACING. Lists constraints for SPI1 GRAPE MISO, MOSI, SCLK, CS L, etc.

DWI

Table with 4 columns: NET\_SPACING\_TYPE1, NET\_SPACING\_TYPE2, AREA\_TYPE, SPACING\_RULE\_SET. Row: DWI, \*, \*, 2:1\_SPACING

Table with 4 columns: ELECTRICAL\_CONSTRAINT\_SET, PHYSICAL, NET\_TYPE, SPACING. Lists constraints for DWI AP CLK, AP DI, AP DO

JTAG

Table with 4 columns: NET\_SPACING\_TYPE1, NET\_SPACING\_TYPE2, AREA\_TYPE, SPACING\_RULE\_SET. Row: JTAG, \*, \*, 2:1\_SPACING

Table with 4 columns: ELECTRICAL\_CONSTRAINT\_SET, PHYSICAL, NET\_TYPE, SPACING. Lists constraints for JTAG AP TCK, TMS, TDI, TDO, TRST L

I2C

Table with 3 columns: NET\_PHYSICAL\_TYPE, AREA\_TYPE, PHYSICAL\_RULE\_SET. Row: I2C\_50S, \*, 50\_OHM\_SE

Table with 4 columns: NET\_SPACING\_TYPE1, NET\_SPACING\_TYPE2, AREA\_TYPE, SPACING\_RULE\_SET. Row: I2C, \*, \*, 1.5:1\_SPACING

Table with 4 columns: ELECTRICAL\_CONSTRAINT\_SET, PHYSICAL, NET\_TYPE, SPACING. Lists constraints for I2C1 SDA, SCL, I2C2 SDA, SCL, etc.

XTAL

Table with 4 columns: NET\_SPACING\_TYPE1, NET\_SPACING\_TYPE2, AREA\_TYPE, SPACING\_RULE\_SET. Row: CRYSTAL, \*, \*, 5:1\_SPACING

Table with 4 columns: ELECTRICAL\_CONSTRAINT\_SET, PHYSICAL, NET\_TYPE, SPACING. Lists constraints for XTAL 24M I, O, PMU XTAL, EXTAL

I2S

Table with 3 columns: NET\_PHYSICAL\_TYPE, AREA\_TYPE, PHYSICAL\_RULE\_SET. Row: I2S\_90S, \*, 45\_OHM\_SE

Table with 4 columns: NET\_SPACING\_TYPE1, NET\_SPACING\_TYPE2, AREA\_TYPE, SPACING\_RULE\_SET. Row: I2S, \*, \*, 3:1\_SPACING

Table with 4 columns: ELECTRICAL\_CONSTRAINT\_SET, PHYSICAL, NET\_TYPE, SPACING. Lists constraints for I2S0 ASP BCLK, LRCK, DIN, DOUT, etc.

USB

Table with 3 columns: NET\_PHYSICAL\_TYPE, AREA\_TYPE, PHYSICAL\_RULE\_SET. Row: USB\_90D, \*, 90\_OHM\_DIFF

Table with 4 columns: NET\_SPACING\_TYPE1, NET\_SPACING\_TYPE2, AREA\_TYPE, SPACING\_RULE\_SET. Row: USB, \*, \*, 5:1\_SPACING

Table with 4 columns: ELECTRICAL\_CONSTRAINT\_SET, PHYSICAL, NET\_TYPE, SPACING. Lists constraints for USB DK DO P, BB D P, BB D N, etc.

HSIC

Table with 3 columns: NET\_PHYSICAL\_TYPE, AREA\_TYPE, PHYSICAL\_RULE\_SET. Row: HSIC, \*, 50\_OHM\_SE

Table with 4 columns: NET\_SPACING\_TYPE1, NET\_SPACING\_TYPE2, AREA\_TYPE, SPACING\_RULE\_SET. Row: HSIC, \*, \*, 5:1\_SPACING

Table with 4 columns: ELECTRICAL\_CONSTRAINT\_SET, PHYSICAL, NET\_TYPE, SPACING. Lists constraints for HSIC0 BB DATA1, STB1, etc.

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DDR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR	*	*	3:1_SPACING

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_90D	*	90_OHM_DIFF

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
E222	DDR_50S	DDR	DDR0_CA<9..0>
E223	DDR_50S	DDR	DDR0_DM<3..0>
E224	DDR_90D	DDR	DDR0_CK_P
E225	DDR_90D	DDR	DDR0_CK_N
E226	DDR_50S	DDR	DDR0_CKE<1..0>
E227	DDR_50S	DDR	DDR0_CSN<2..0>
E228	DDR_50S	DDR	DDR0_ZQ
E229	DDR_50S	DDR0	DDR0_DQ<7..0>
E230	DDR_50S	DDR0	DDR0_DQS_P<0>
E231	DDR_50S	DDR0	DDR0_DQS_N<0>
E232	DDR_50S	DDR1	DDR0_DQ<15..8>
E233	DDR_50S	DDR1	DDR0_DQS_P<1>
E234	DDR_50S	DDR1	DDR0_DQS_N<1>
E235	DDR_50S	DDR2	DDR0_DQ<23..16>
E236	DDR_50S	DDR2	DDR0_DQS_P<2>
E237	DDR_50S	DDR2	DDR0_DQS_N<2>
E238	DDR_50S	DDR3	DDR0_DQ<31..24>
E239	DDR_50S	DDR3	DDR0_DQS_P<3>
E240	DDR_50S	DDR3	DDR0_DQS_N<3>
E241	DDR_50S	DDR	DDR1_CA<9..0>
E242	DDR_50S	DDR	DDR1_DM<3..0>
E243	DDR_90D	DDR	DDR1_CK_P
E244	DDR_90D	DDR	DDR1_CK_N
E245	DDR_50S	DDR	DDR1_CKE<1..0>
E246	DDR_50S	DDR	DDR1_CSN<2..0>
E247	DDR_50S	DDR	DDR1_ZQ
E248	DDR_50S	DDR0	DDR1_DQ<7..0>
E249	DDR_50S	DDR0	DDR1_DQS_P<0>
E250	DDR_50S	DDR0	DDR1_DQS_N<0>
E251	DDR_50S	DDR1	DDR1_DQ<15..8>
E252	DDR_50S	DDR1	DDR1_DQS_P<1>
E253	DDR_50S	DDR1	DDR1_DQS_N<1>
E254	DDR_50S	DDR2	DDR1_DQ<23..16>
E255	DDR_50S	DDR2	DDR1_DQS_P<2>
E256	DDR_50S	DDR2	DDR1_DQS_N<2>
E257	DDR_50S	DDR3	DDR1_DQ<31..24>
E258	DDR_50S	DDR3	DDR1_DQS_P<3>
E259	DDR_50S	DDR3	DDR1_DQS_N<3>
E260	DDR_50S	DDR	DDR2_CA<9..0>
E261	DDR_50S	DDR	DDR2_DM<3..0>
E262	DDR_90D	DDR	DDR2_CK_P
E263	DDR_90D	DDR	DDR2_CK_N
E264	DDR_50S	DDR	DDR2_CKE<1..0>
E265	DDR_50S	DDR	DDR2_CSN<2..0>
E266	DDR_50S	DDR	DDR2_ZQ
E267	DDR_50S	DDR0	DDR2_DQ<7..0>
E268	DDR_50S	DDR0	DDR2_DQS_P<0>
E269	DDR_50S	DDR0	DDR2_DQS_N<0>
E270	DDR_50S	DDR1	DDR2_DQ<15..8>
E271	DDR_50S	DDR1	DDR2_DQS_P<1>
E272	DDR_50S	DDR1	DDR2_DQS_N<1>
E273	DDR_50S	DDR2	DDR2_DQ<23..16>
E274	DDR_50S	DDR2	DDR2_DQS_P<2>
E275	DDR_50S	DDR2	DDR2_DQS_N<2>
E276	DDR_50S	DDR3	DDR2_DQ<31..24>
E277	DDR_50S	DDR3	DDR2_DQS_P<3>
E278	DDR_50S	DDR3	DDR2_DQS_N<3>
E279	DDR_50S	DDR	DDR3_CA<9..0>
E280	DDR_50S	DDR	DDR3_DM<3..0>
E281	DDR_90D	DDR	DDR3_CK_P
E282	DDR_90D	DDR	DDR3_CK_N
E283	DDR_50S	DDR	DDR3_CKE<1..0>
E284	DDR_50S	DDR	DDR3_CSN<2..0>
E285	DDR_50S	DDR	DDR3_ZQ
E286	DDR_50S	DDR0	DDR3_DQ<7..0>
E287	DDR_50S	DDR0	DDR3_DQS_P<0>
E288	DDR_50S	DDR0	DDR3_DQS_N<0>
E289	DDR_50S	DDR1	DDR3_DQ<15..8>
E290	DDR_50S	DDR1	DDR3_DQS_P<1>
E291	DDR_50S	DDR1	DDR3_DQS_N<1>
E292	DDR_50S	DDR2	DDR3_DQ<23..16>
E293	DDR_50S	DDR2	DDR3_DQS_P<2>
E294	DDR_50S	DDR2	DDR3_DQS_N<2>
E295	DDR_50S	DDR3	DDR3_DQ<31..24>
E296	DDR_50S	DDR3	DDR3_DQS_P<3>
E297	DDR_50S	DDR3	DDR3_DQS_N<3>

NAND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
NAND_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
NAND	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
E300	NAND_50S	NAND0	FMIO_AD<0>
E301	NAND_50S	NAND0	FMIO_AD<1>
E302	NAND_50S	NAND0	FMIO_AD<2>
E303	NAND_50S	NAND0	FMIO_AD<3>
E304	NAND_50S	NAND0	FMIO_AD<4>
E305	NAND_50S	NAND0	FMIO_AD<5>
E306	NAND_50S	NAND0	FMIO_AD<6>
E307	NAND_50S	NAND0	FMIO_AD<7>
E308	NAND_50S	NAND0	FMIO_ALE
E309	NAND_50S	NAND0	FMIO_CE0_L
E310	NAND_50S	NAND0	FMIO_CE1_L
E311	NAND_50S	NAND0	FMIO_CE2_L
E312	NAND_50S	NAND0	FMIO_CE3_L
E313	NAND_50S	NAND0	FMIO_CE4_L
E314	NAND_50S	NAND0	FMIO_CE5_L
E315	NAND_50S	NAND0	FMIO_CE6_L
E316	NAND_50S	NAND0	FMIO_CE7_L
E317	NAND_50S	NAND0	FMIO_CLE
E318	NAND_50S	NAND0	FMIO_DOS_N
E319	NAND_50S	NAND0	FMIO_DQS_P
E320	NAND_50S	NAND0	FMIO_RB0_L
E321	NAND_50S	NAND0	FMIO_RB1_L
E322	NAND_50S	NAND0	FMIO_RE_N
E323	NAND_50S	NAND0	FMIO_RE_P
E324	NAND_50S	NAND0	FMIO_WE_L
E325	NAND_50S	NAND0	FMIO_WP_L
E326	NAND_50S	NAND1	FM11_AD<0>
E327	NAND_50S	NAND1	FM11_AD<1>
E328	NAND_50S	NAND1	FM11_AD<2>
E329	NAND_50S	NAND1	FM11_AD<3>
E330	NAND_50S	NAND1	FM11_AD<4>
E331	NAND_50S	NAND1	FM11_AD<5>
E332	NAND_50S	NAND1	FM11_AD<6>
E333	NAND_50S	NAND1	FM11_AD<7>
E334	NAND_50S	NAND1	FM11_ALE
E335	NAND_50S	NAND1	FM11_CE0_L
E336	NAND_50S	NAND1	FM11_CE1_L
E337	NAND_50S	NAND1	FM11_CE2_L
E338	NAND_50S	NAND1	FM11_CE3_L
E339	NAND_50S	NAND1	FM11_CE4_L
E340	NAND_50S	NAND1	FM11_CE5_L
E341	NAND_50S	NAND1	FM11_CE6_L
E342	NAND_50S	NAND1	FM11_CE7_L
E343	NAND_50S	NAND1	FM11_CLE
E344	NAND_50S	NAND1	FM11_DQS_N
E345	NAND_50S	NAND1	FM11_DQS_P
E346	NAND_50S	NAND1	FM11_RB0_L
E347	NAND_50S	NAND1	FM11_RB1_L
E348	NAND_50S	NAND1	FM11_RE_N
E349	NAND_50S	NAND1	FM11_RE_P
E350	NAND_50S	NAND1	FM11_WE_L
E351	NAND_50S	NAND1	FM11_WP_L

DDR VREF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VREF	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
E352	PWR	PWR	PPVREF_DDR0_CA
E353	PWR	PWR	PPVREF_DDR0_DQ
E354	PWR	PWR	PPVREF_DDR1_CA
E355	PWR	PWR	PPVREF_DDR1_DQ

NAND DEV

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
E356	NAND_50S	NAND0	SLOT0_FMIO_AD<0>
E357	NAND_50S	NAND0	SLOT0_FMIO_AD<1>
E358	NAND_50S	NAND0	SLOT0_FMIO_AD<2>
E359	NAND_50S	NAND0	SLOT0_FMIO_AD<3>
E360	NAND_50S	NAND0	SLOT0_FMIO_AD<4>
E361	NAND_50S	NAND0	SLOT0_FMIO_AD<5>
E362	NAND_50S	NAND0	SLOT0_FMIO_AD<6>
E363	NAND_50S	NAND0	SLOT0_FMIO_AD<7>
E364	NAND_50S	NAND0	SLOT0_FMIO_ALE
E365	NAND_50S	NAND0	SLOT0_FMIO_CE0_L
E366	NAND_50S	NAND0	SLOT0_FMIO_CE1_L
E367	NAND_50S	NAND0	SLOT0_FMIO_CLE
E368	NAND_50S	NAND0	SLOT0_FMIO_DQS_P
E369	NAND_50S	NAND0	SLOT0_FMIO_RE_N
E370	NAND_50S	NAND0	SLOT0_FMIO_WE_L
E371	NAND_50S	NAND1	SLOT0_FM11_AD<0>
E372	NAND_50S	NAND1	SLOT0_FM11_AD<1>
E373	NAND_50S	NAND1	SLOT0_FM11_AD<2>
E374	NAND_50S	NAND1	SLOT0_FM11_AD<3>
E375	NAND_50S	NAND1	SLOT0_FM11_AD<4>
E376	NAND_50S	NAND1	SLOT0_FM11_AD<5>
E377	NAND_50S	NAND1	SLOT0_FM11_AD<6>
E378	NAND_50S	NAND1	SLOT0_FM11_AD<7>
E379	NAND_50S	NAND1	SLOT0_FM11_ALE
E380	NAND_50S	NAND1	SLOT0_FM11_CE0_L
E381	NAND_50S	NAND1	SLOT0_FM11_CE1_L
E382	NAND_50S	NAND1	SLOT0_FM11_CLE
E383	NAND_50S	NAND1	SLOT0_FM11_DQS_P
E384	NAND_50S	NAND1	SLOT0_FM11_RE_N
E385	NAND_50S	NAND1	SLOT0_FM11_WE_L
E386	NAND_50S	NAND0	SLOT1_FMIO_AD<0>
E387	NAND_50S	NAND0	SLOT1_FMIO_AD<1>
E388	NAND_50S	NAND0	SLOT1_FMIO_AD<2>
E389	NAND_50S	NAND0	SLOT1_FMIO_AD<3>
E390	NAND_50S	NAND0	SLOT1_FMIO_AD<4>
E391	NAND_50S	NAND0	SLOT1_FMIO_AD<5>
E392	NAND_50S	NAND0	SLOT1_FMIO_AD<6>
E393	NAND_50S	NAND0	SLOT1_FMIO_AD<7>
E394	NAND_50S	NAND0	SLOT1_FMIO_ALE
E395	NAND_50S	NAND0	SLOT1_FMIO_CE0_L
E396	NAND_50S	NAND0	SLOT1_FMIO_CE1_L
E397	NAND_50S	NAND0	SLOT1_FMIO_CLE
E398	NAND_50S	NAND0	SLOT1_FMIO_DQS_P
E399	NAND_50S	NAND0	SLOT1_FMIO_RE_N
E400	NAND_50S	NAND0	SLOT1_FMIO_WE_L
E401	NAND_50S	NAND1	SLOT1_FM11_AD<0>
E402	NAND_50S	NAND1	SLOT1_FM11_AD<1>
E403	NAND_50S	NAND1	SLOT1_FM11_AD<2>
E404	NAND_50S	NAND1	SLOT1_FM11_AD<3>
E405	NAND_50S	NAND1	SLOT1_FM11_AD<4>
E406	NAND_50S	NAND1	SLOT1_FM11_AD<5>
E407	NAND_50S	NAND1	SLOT1_FM11_AD<6>
E408	NAND_50S	NAND1	SLOT1_FM11_AD<7>
E409	NAND_50S	NAND1	SLOT1_FM11_ALE
E410	NAND_50S	NAND1	SLOT1_FM11_CE0_L
E411	NAND_50S	NAND1	SLOT1_FM11_CE1_L
E412	NAND_50S	NAND1	SLOT1_FM11_CLE
E413	NAND_50S	NAND1	SLOT1_FM11_DQS_P
E414	NAND_50S	NAND1	SLOT1_FM11_RE_N
E415	NAND_50S	NAND1	SLOT1_FM11_WE_L

SYNC MASTER=MIKE SYNC DATE=01/21/2011

**CONSTRAINTS: DDR/FMI**

Apple Inc.

DRAWING NUMBER: 051-8773 SIZE: D

REVISION: 10.0.0

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PWR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PWR	*	PWR_PMU

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PWR	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
PP33	3.0V	PP_PWR	PWR	MT 3V3 INT 18 45
PP34	1.8V	PP_PWR	PWR	Z1 1V8 OUT 18
PP35	1.8V	PP_PWR	PWR	Z2 VDDCORE 18
PP36	1.8V	PP_PWR	PWR	Z2 VDDANA 18
PP37	1.8V	PP_PWR	PWR	Z2 3V3 1V8 IN 18

VOLTAGE	NET_TYPE			
	PHYSICAL	SPACING		
PP27	3.3V	PP_PWR	PWR	ACC_PT_DK_CON_PP3V3 27 29
PP28		PP_PWR	PWR	BUCK0_FB 36
PP29		PP_PWR	PWR	BUCK0_LXL 36
PP30		PP_PWR	PWR	BUCK0_LXM 36
PP31		PP_PWR	PWR	BUCK2_FB 36
PP32		PP_PWR	PWR	BUCK2_LXL 36
PP33		PP_PWR	PWR	BUCK2_LXM 36
PP34		PP_PWR	PWR	BUCK2_LXR 36
PP35		PP_PWR	PWR	BUCK3_FB 36
PP36		PP_PWR	PWR	BUCK3_LXL 36
PP37		PP_PWR	PWR	BUCK3_LXM 36
PP38		PP_PWR	PWR	BUCK4_FB 36
PP39		PP_PWR	PWR	BUCK4_LXL 36
PP40		PP_PWR	PWR	BUCK4_LXM 36
PP41		PP_PWR	PWR	BUCK5_FB 36
PP42		PP_PWR	PWR	BUCK5_LX 36
PP43	0.4V	PP_PWR	PWR	PP0V4_MIPI0D 7
PP44	0.4V	PP_PWR	PWR	PP0V4_MIPI1D 7
PP45	1.1V	PP_PWR	PWR	PP1V1 35 36
PP46	1.2V	PP_PWR	PWR	PP1V2 35 36
PP47	1.1V	PP_PWR	PWR	PP1V8 35 36
PP48	1.1V	PP_PWR	PWR	PP1V1_MIPID_PLL_F 4
PP49	1.1V	PP_PWR	PWR	PP1V1_PL0_F 4
PP50	1.1V	PP_PWR	PWR	PP1V1_PL1_F 4
PP51	1.1V	PP_PWR	PWR	PP1V1_PL2_F 4
PP52	1.1V	PP_PWR	PWR	PP1V1_PL3_F 4
PP53	1.1V	PP_PWR	PWR	PP1V1_PL4_F 4
PP54	1.1V	PP_PWR	PWR	PP1V1_PL5_F 4
PP55	1.1V	PP_PWR	PWR	PP1V1_PLL_USB_F 4
PP56	1.25V	PP_PWR	PWR	PP1V25_CPU 35 36
PP57	1.2V	PP_PWR	PWR	PP1V2_S2R 35 36
PP58	1.2V	PP_PWR	PWR	PP1V2_SOC 35 36
PP59	1.2V	PP_PWR	PWR	PP1V7_VA_VCP 35 36 40
PP60	1.8V	PP_PWR	PWR	PP1V8_ALWAYS 35 36
PP61	1.8V	PP_PWR	PWR	PP1V8_DP_AVDD_AUX 7
PP62	1.8V	PP_PWR	PWR	PP1V8_EDP_AVDD_AUX 7
PP63	1.8V	PP_PWR	PWR	PP1V8_GRAPE 35 36
PP64	1.8V	PP_PWR	PWR	PP1V8_S2R 35 36
PP65	1.8V	PP_PWR	PWR	PP1V8_SENSOR_FLT 24 26
PP66	1.8V	PP_PWR	PWR	PP1V8_VDDA18_TS 5
PP67	2.85V	PP_PWR	PWR	PP2V85_CAM 35 36
PP68	2.85V	PP_PWR	PWR	PP2V85_CAM_FLT 24 26
PP69	3.0V	PP_PWR	PWR	PP3V0_GRAPE 35 36
PP70	3.0V	PP_PWR	PWR	PP3V0_IO 35 36
PP71	3.0V	PP_PWR	PWR	PP3V0_OPTICAL 35 36
PP72	3.0V	PP_PWR	PWR	PP3V0_S2R_HALL 35 36
PP73	3.0V	PP_PWR	PWR	PP3V0_S2R_HALL_FLT 24 26
PP74	3.0V	PP_PWR	PWR	PP3V0_SENSOR_FLT 10 24 26
PP75	3.0V	PP_PWR	PWR	PP3V0_VIDEO 35 36
PP76	3.0V	PP_PWR	PWR	PP3V0_VIDEO_BUF 35 36
PP77	3.2V	PP_PWR	PWR	PP3V2_LDO5 35 36
PP78	3.2V	PP_PWR	PWR	PP3V2_S2R_USBMUX 35 36
PP79	3.3V	PP_PWR	PWR	PP3V3_ACC 35 36
PP80	3.3V	PP_PWR	PWR	PP3V3_LCDVDD_SW_F 16
PP81	3.3V	PP_PWR	PWR	PP3V3_OUT 35 36
PP82	3.3V	PP_PWR	PWR	PP3V3_S0_LCD_FERR 16
PP83	5.25V	PP_PWR	PWR	PP5V25_VLCM2 35 37
PP84	6.0V	PP_PWR	PWR	PP6V0_LCM_HI 37
PP85	6.0V	PP_PWR	PWR	PP6V0_LCM_VBOOST 37
PP86	4.2V	PWR500	PWR	PPBATT_VCC 35 36 39
PP87	1.8V	PP_PWR	PWR	PPIO_NAND_H4 6 9
PP88	20.4V	PP_PWR	PWR	PPLED_BACK_REG_A 16
PP89	20.4V	PP_PWR	PWR	PPLED_BACK_REG_B 16
PP90	20.4V	PP_PWR	PWR	PPLED_OUT_A 35 37
PP91	20.4V	PP_PWR	PWR	PPLED_OUT_B 35 37
PP92	6.0V	PP_PWR	PWR	PPVBUS_PROT 36
PP93	6.0V	PP_PWR	PWR	PPVBUS_USB 4 36
PP94	6.0V	PP_PWR	PWR	PPVBUS_USB_DCIN 35 36
PP95	5.0V	PP_PWR	PWR	PPVBUS_USB_PT_DK_CON 27 29
PP96	1.8V	PP_PWR	PWR	PPVCCO_NAND 12
PP97	4.7V	PP_PWR	PWR	PPVCC_MAIN 35 36 37
PP98	0.6V	PP_PWR	PWR	PPVREF_DDR0_CA 13 44
PP99	0.6V	PP_PWR	PWR	PPVREF_DDR0_DO 13 44
PP100	0.6V	PP_PWR	PWR	PPVREF_DDR0_DO_H4 6
PP101	0.6V	PP_PWR	PWR	PPVREF_DDR1_CA 13 44
PP102	0.6V	PP_PWR	PWR	PPVREF_DDR1_DO 13 44
PP103	0.6V	PP_PWR	PWR	PPVREF_DDR1_DO_H4 6
PP104	0.6V	PP_PWR	PWR	PPVREF_DDR2_CA 14
PP105	0.6V	PP_PWR	PWR	PPVREF_DDR2_DO 14
PP106	0.6V	PP_PWR	PWR	PPVREF_DDR2_DO_H4 6
PP107	0.6V	PP_PWR	PWR	PPVREF_DDR3_CA 14
PP108	0.6V	PP_PWR	PWR	PPVREF_DDR3_DO 14
PP109	0.6V	PP_PWR	PWR	PPVREF_DDR3_DO_H4 6
PP110	4.6V	PP_PWR	PWR	BATT_POS_RC 36
PP111	1.8V	PP_PWR	PWR	PP18V_GRAPE 17
PP112	1.8V	PP_PWR	PWR	PP18V_R_GRAPE 17
PP113		PP_PWR	PWR	DAC_AP_VREF 7
PP114	3.3V	PP_PWR	PWR	PPVDDI_NAND_U1400 12
PP115		PP_PWR	PWR	VR_BOOST_SW 17
PP116		PP_PWR	PWR	VR_BOOST_L 17
PP117	3.0V	PP_PWR	PWR	MT_3V3_INT 18 45

GND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GND_PH	*	GND

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
PP30	GND	GND	GND	
PP31	GND	GND	VOLTAGE=0V	GND_AUDIO_CODEC 19 21
PP32	GND	GND	VOLTAGE=0V	GND_AUDIO_HP_AMP 19 21 22
PP33	GND	GND	VOLTAGE=0V	GND_AUDIO_PT_DK 21 27
PP34	GND	GND	VOLTAGE=0V	GND_SPKR_AMP1 20
PP35	GND	GND	VOLTAGE=0V	GND_SPKR_AMP2 20
PP36	GND	GND	VOLTAGE=0V	GND_PMU 20
PP37	GND	GND		AGND 17
PP38	GND	GND		AGND_U3000 17

RST

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
RST	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
PP39		RST	RST	BB_TRST_L 19 21
PP40		RST	RST	DBG_RST 19 21
PP41		RST	RST	DEBUG_RST_L 19 21
PP42		RST	RST	GSM_TXBURST_IND 5 15 30
PP43		RST	RST	JTAG_AP_TRST_L 4 10 42
PP44		RST	RST	RST_AP_IV8_L 4
PP45		RST	RST	RST_AP_L 4 27 30 37
PP46		RST	RST	RST_BB_L 5 30
PP47		RST	RST	RST_BB_PMU_L 10 37
PP48		RST	RST	RST_BT_L 15 37
PP49		RST	RST	RST_DET_L 5 30
PP50		GRAPE	GRAPE	RST_GRAPE_L 4 17
PP51		RST	RST	RST_L63_L 19 37
PP52		RST	RST	RST_PMU_IN 4 37
PP53		RST	RST	RST_WLAN_L 15 37
PP54		RST	RST	SIMCRD_RST 15 37
PP55		RST	RST	TP_WLAN_TRST_L 15 37
PP56		RST	RST	UD881_RST 15 37
PP57		RST	RST	UD882_RST 15 37

SYNC MASTER=MIKE SYNC DATE=01/21/2011

**CONSTRAINTS: POWER / GND**

Apple Inc.

DRAWING NUMBER: 051-8773 SIZE: D

REVISION: 10.0.0

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SNS

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SNS_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SNS	*	*	311_SPACING

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SNS_90D	*	90_OHM_DIFF

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1E10 NC HSIC0\_DATA2 NO\_TEST=TRUE 4 42  
 1E11 NC HSIC0\_STB2 NO\_TEST=TRUE 4 42  
 1E12 NC HSIC1\_DATA2 NO\_TEST=TRUE 4 42  
 1E13 NC HSIC1\_STB2 NO\_TEST=TRUE 4 42

1E14 NC JTAG\_AP\_TRICK NO\_TEST=TRUE 4

1E15 NC\_USB\_D1\_P NO\_TEST=TRUE 4 42  
 1E16 NC\_USB\_D1\_N NO\_TEST=TRUE 4 42  
 1E17 NC\_USB11\_D1\_P NO\_TEST=TRUE 4 42  
 1E18 NC\_USB11\_D1\_N NO\_TEST=TRUE 4 42

1E19 NC\_USB\_ANALOGTEST0 NO\_TEST=TRUE 4  
 1E20 NC\_USB\_ANALOGTEST1 NO\_TEST=TRUE 4  
 1E21 NC\_USB\_ID0 NO\_TEST=TRUE 4  
 1E22 NC\_USB\_ID1 NO\_TEST=TRUE 4  
 1E23 NC\_USB\_BRICKID1 NO\_TEST=TRUE 4

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 1E27 NC\_I2S1\_DIN NO\_TEST=TRUE 5  
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 1E30 NC\_I2S3\_MCK NO\_TEST=TRUE 5  
 1E31 NC\_AP\_GPIO216 NO\_TEST=TRUE 5  
 1E32 NC\_SPI\_FLASH\_CS\_L NO\_TEST=TRUE 5

1E33 NC\_SWI\_AP NO\_TEST=TRUE 5  
 1E34 NC\_SDIO0\_WL\_CLK NO\_TEST=TRUE 5  
 1E35 NC\_SDIO0\_WL\_CMD NO\_TEST=TRUE 5  
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 1E38 NC\_SDIO0\_WL\_DATA<2> NO\_TEST=TRUE 5  
 1E39 NC\_SDIO0\_WL\_DATA<3> NO\_TEST=TRUE 5  
 1E40 NC\_SPI3\_MISO NO\_TEST=TRUE 5  
 1E41 NC\_SPI3\_MOSI NO\_TEST=TRUE 5  
 1E42 NC\_SPI3\_SCLK NO\_TEST=TRUE 5  
 1E43 NC\_SPI3\_CS\_L NO\_TEST=TRUE 5

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 1E45 NC\_AP\_GPIO7 NO\_TEST=TRUE 5  
 1E46 NC\_AP\_GPIO8 NO\_TEST=TRUE 5  
 1E47 NC\_AP\_GPIO11 NO\_TEST=TRUE 5  
 1E48 NC\_AP\_GPIO13 NO\_TEST=TRUE 5  
 1E49 NC\_BOARD\_ID\_3 NO\_TEST=TRUE 5  
 1E50 NC\_AP\_GPIO19 NO\_TEST=TRUE 5  
 1E51 NC\_AP\_GPIO31 NO\_TEST=TRUE 5  
 1E52 NC\_AP\_GPIO35 NO\_TEST=TRUE 5  
 1E53 NC\_AP\_GPIO2V1 NO\_TEST=TRUE 5  
 1E54 NC\_AP\_GPIO185 NO\_TEST=TRUE 5  
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 1E61 NC\_UART4\_TXD NO\_TEST=TRUE 5  
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 1E63 NC\_UART6\_RTSN NO\_TEST=TRUE 5

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 1E91 NC\_FMI2\_RE\_L NO\_TEST=TRUE 6  
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 1E93 NC\_FMI3\_CE0\_L NO\_TEST=TRUE 6  
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 1E98 NC\_FMI3\_CE5\_L NO\_TEST=TRUE 6  
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 1E100 NC\_FMI3\_CE7\_L NO\_TEST=TRUE 6

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 1E109 NC\_FMI3\_ALE NO\_TEST=TRUE 6  
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 1E115 NC\_MIPI0C\_AP\_DATA\_P<2> NO\_TEST=TRUE 7 43  
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 1E119 NC\_MIPI1C\_AP\_DATA\_P<1> NO\_TEST=TRUE 7 43  
 1E120 NC\_MIPI1C\_AP\_DATA\_N<1> NO\_TEST=TRUE 7 43

1E121 NC\_ISP\_AP\_1\_FLASH NO\_TEST=TRUE 7  
 1E122 NC\_ISP\_AP\_1\_PRE\_FLASH NO\_TEST=TRUE 7

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 1E129 NC\_DDR2\_CSN<1> NO\_TEST=TRUE 8  
 1E130 NC\_DDR3\_CSN<1> NO\_TEST=TRUE 8

1E131 NC\_PMU\_VBUCK0\_SW0\_G NO\_TEST=TRUE 36  
 1E132 NC\_PMU\_VBUCK0\_SW0\_S NO\_TEST=TRUE 36  
 1E133 NC\_VBUS\_A\_OV\_L NO\_TEST=TRUE 36  
 1E134 NC\_BOARD\_TEMP7 NO\_TEST=TRUE 37  
 1E135 NC\_BOARD\_TEMP8 NO\_TEST=TRUE 37

1E136 NC\_PMU\_GPIO12 NO\_TEST=TRUE 37  
 1E137 NC\_PMU\_GPIO13 NO\_TEST=TRUE 37

1E138 NC\_PMU\_GPIO16 NO\_TEST=TRUE 37  
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1E140 NC\_PMU\_AMUX\_A0 NO\_TEST=TRUE 37  
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 1E142 NC\_PMU\_AMUX\_A2 NO\_TEST=TRUE 37  
 1E143 NC\_PMU\_AMUX\_A3 NO\_TEST=TRUE 37  
 1E144 NC\_PMU\_AMUX\_AY NO\_TEST=TRUE 37  
 1E145 NC\_PMU\_AMUX\_B0 NO\_TEST=TRUE 37  
 1E146 NC\_PMU\_AMUX\_B1 NO\_TEST=TRUE 37  
 1E147 NC\_PMU\_AMUX\_B2 NO\_TEST=TRUE 37  
 1E148 NC\_PMU\_AMUX\_B3 NO\_TEST=TRUE 37  
 1E149 NC\_PMU\_AMUX\_BY NO\_TEST=TRUE 37

1E150 NC\_BON\_L1 NO\_TEST=TRUE 18  
 1E151 NC\_BON\_L3 NO\_TEST=TRUE 18  
 1E152 NC\_BON\_L5 NO\_TEST=TRUE 18  
 1E153 NC\_EAROUT\_AP NO\_TEST=TRUE 19  
 1E154 NC\_EAROUT\_AN NO\_TEST=TRUE 19

1E155 NC\_LINE\_IN1\_CODEC NO\_TEST=TRUE 19  
 1E156 NC\_LINE\_IN1\_REF\_CODEC NO\_TEST=TRUE 19  
 1E157 NC\_LINE\_IN2\_CODEC NO\_TEST=TRUE 19  
 1E158 NC\_LINE\_IN2\_REF\_CODEC NO\_TEST=TRUE 19  
 1E159 NC\_MIC1\_BIAS\_CODEC NO\_TEST=TRUE 19  
 1E160 NC\_MIC1P\_CODEC NO\_TEST=TRUE 19  
 1E161 NC\_MIC1N\_CODEC NO\_TEST=TRUE 19  
 1E162 NC\_MIC1\_FILT\_CODEC NO\_TEST=TRUE 19

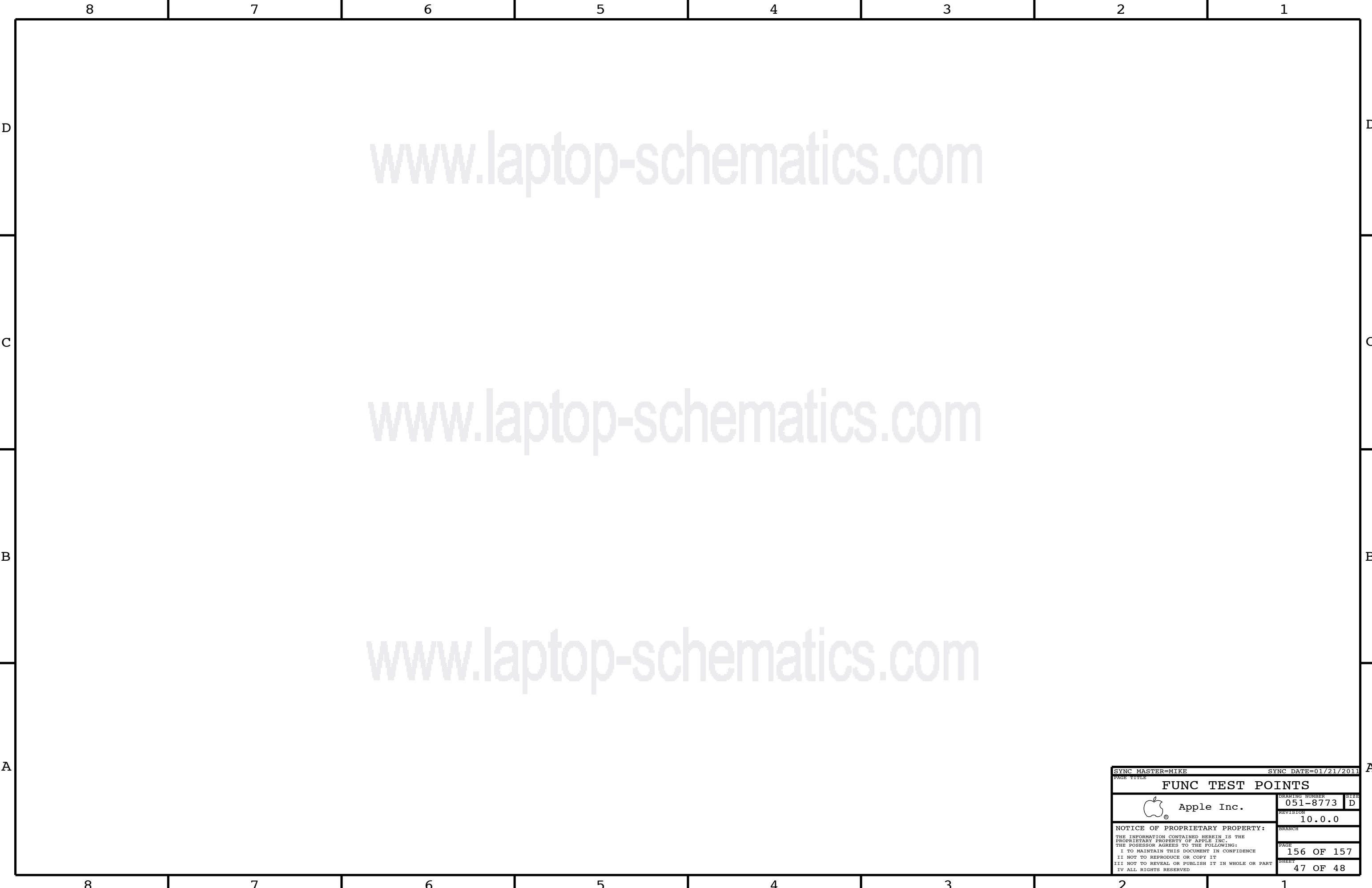
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 1E168 NC\_VLCM1 NO\_TEST=TRUE 37

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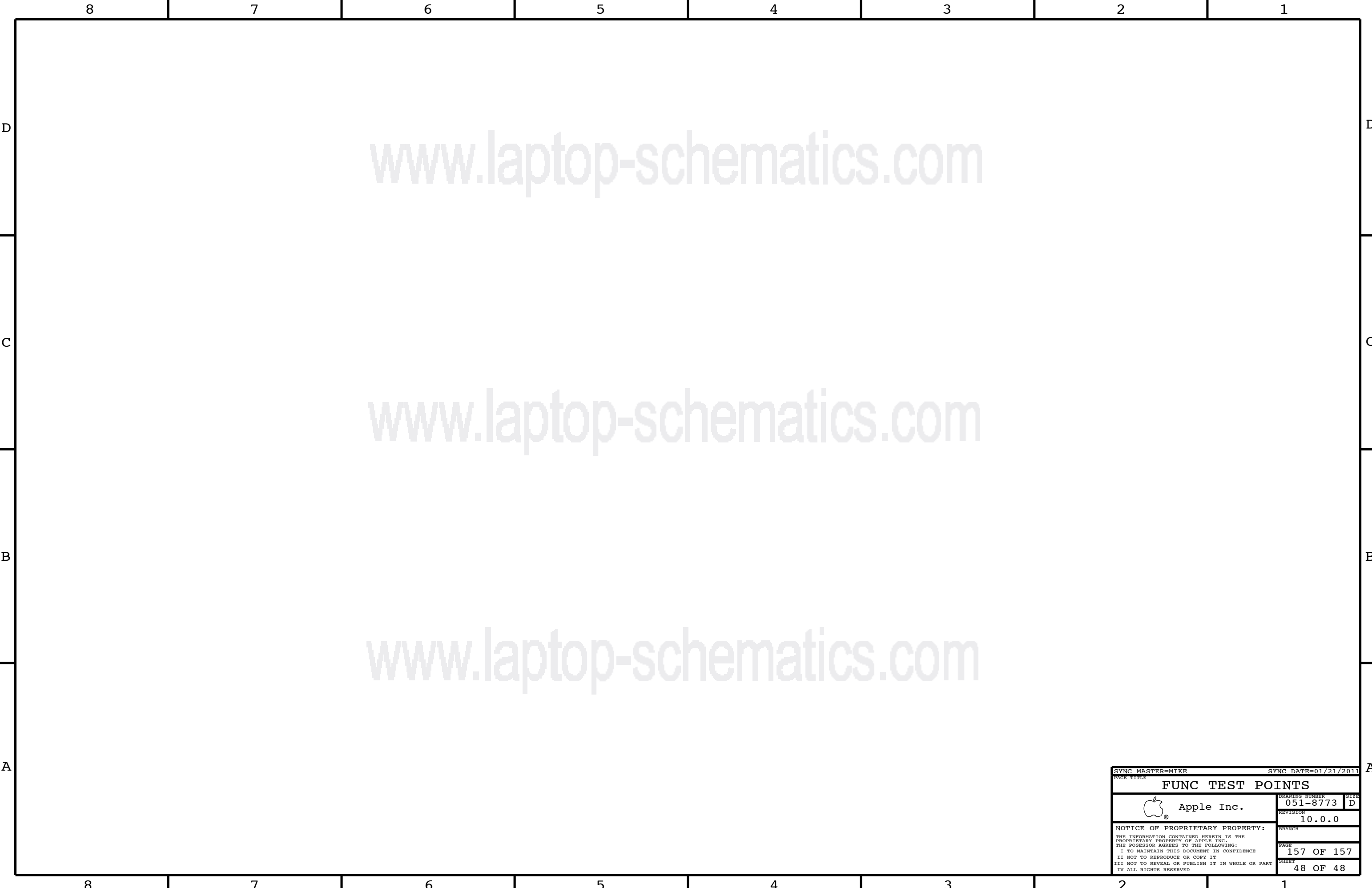


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