1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,"BLACK PEARL",MLB

12/18/10

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2009-05-19

DRAWING TITLE

Apple Inc.

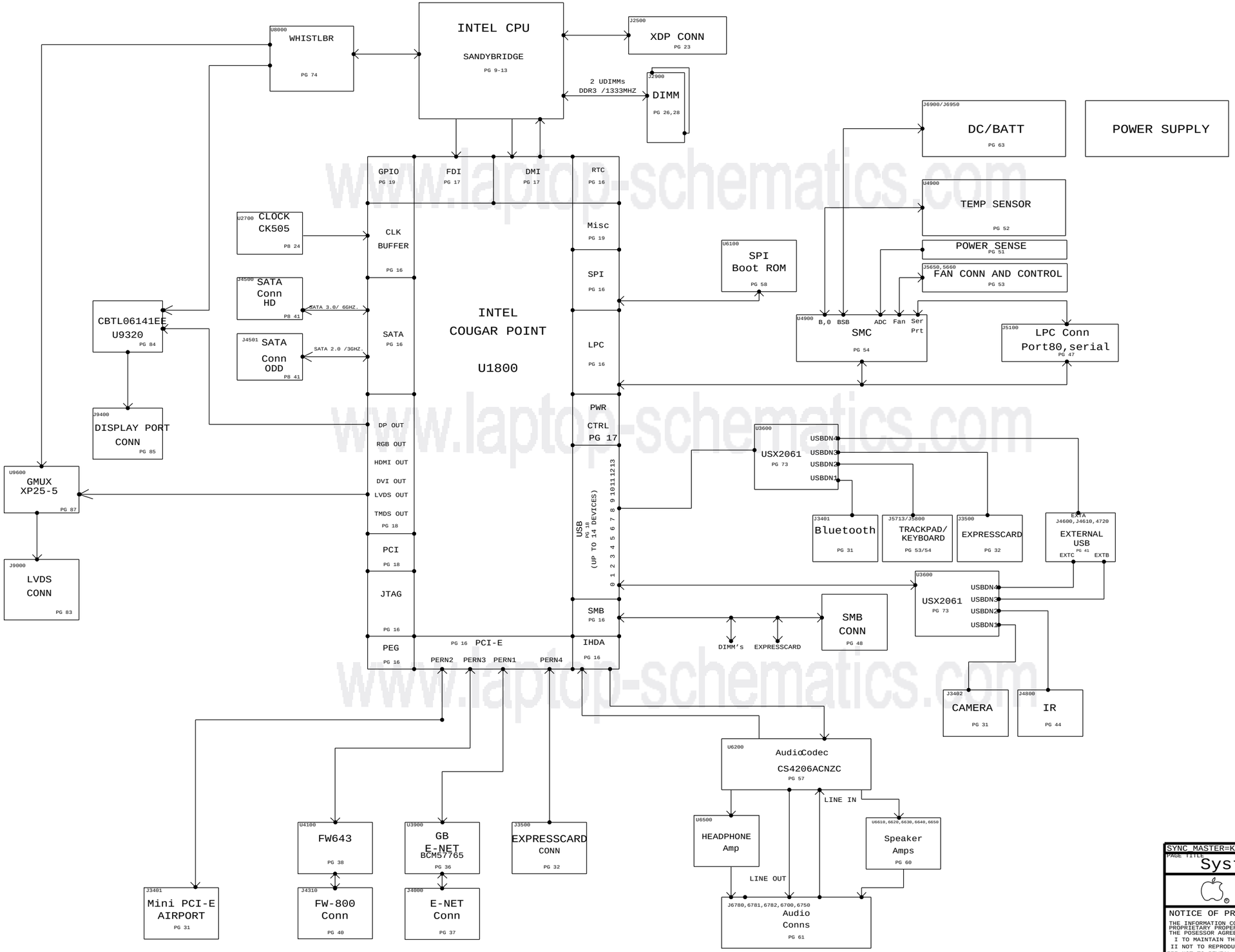
DRAWING NUMBER | SIZE D

REVISION

BRANCH

PAGE 1 OF 132

SHEET 1 OF 105



SYNC_MASTER=K60_MLB SYNC_DATE=04/26/2010

PAGE TITLE

System Block Diagram

Apple Inc.

DRAWING NUMBER | SIZE D

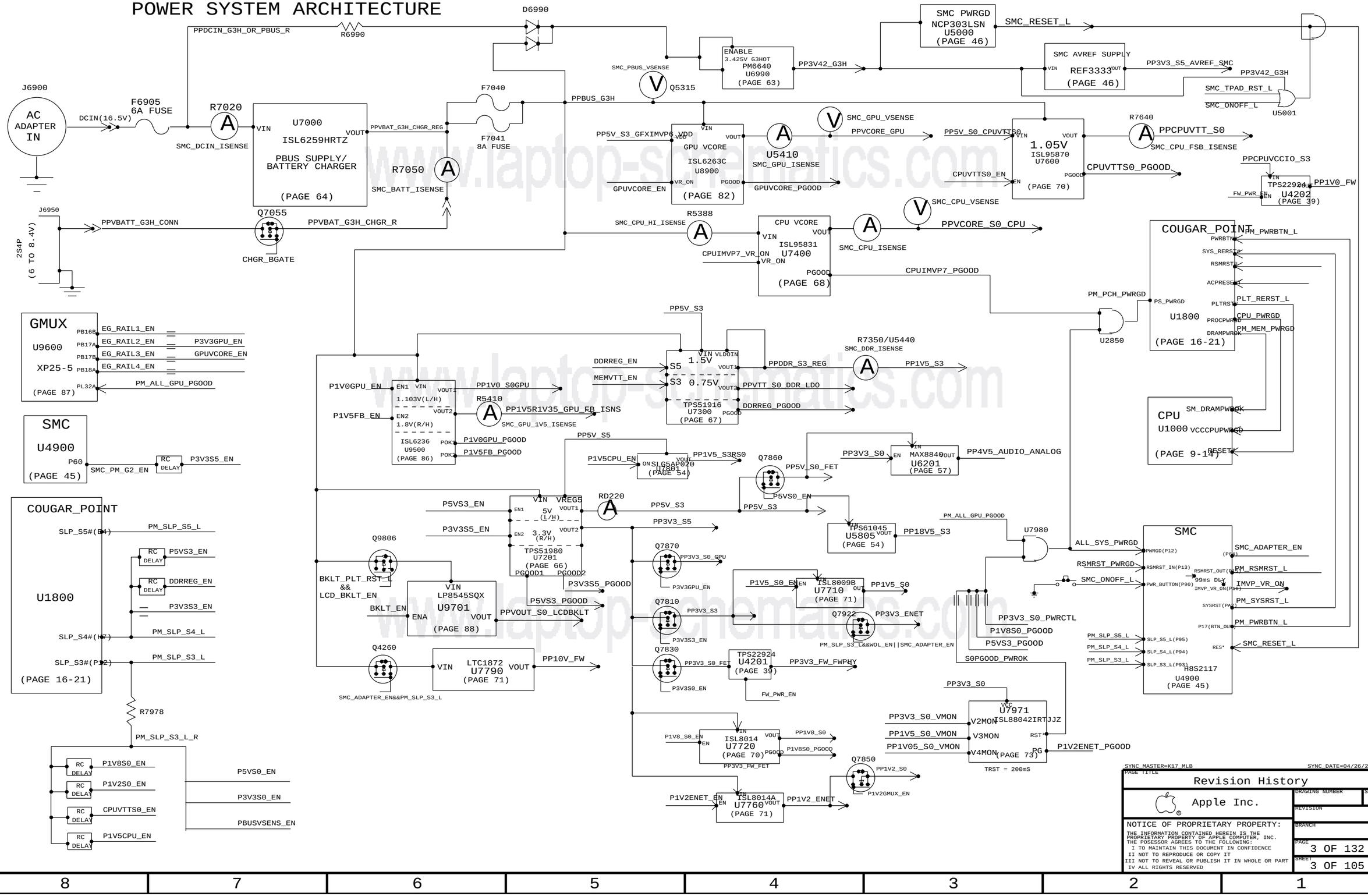
REVISION

BRANCH

PAGE 2 OF 132

SHEET 2 OF 105

POWER SYSTEM ARCHITECTURE



SYNC_MASTER=K17_MLB
SYNC_DATE=04/26/2010
PAGE TITLE

Revision History

Apple Inc.

DRAWING NUMBER
SIZE D
REVISION
BRANCH
PAGE 3 OF 132
SHEET 3 OF 105

SYNC_MASTER=K17_MLB SYNC_DATE=04/26/2010

PAGE TITLE

Revision History

Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH

PAGE 4 OF 132

SHEET 4 OF 105

Bar Code Labels / EEEE #’s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5Y]	CRITICAL	EEEE_DG5Y
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG60]	CRITICAL	EEEE_DG60
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG61]	CRITICAL	EEEE_DG61
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG62]	CRITICAL	EEEE_DG62

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4032	1	IC,CPU,SNB,SR00W,PRQ,D2,2.2,45W,4+2,1.30,6M,BGA	U1000	CRITICAL	CPU:2_2GHZ
337S4033	1	IC,CPU,SNB,SR00U,PRQ.D2,2.3,45W,4+2,1.30,8M,BGA	U1000	CRITICAL	CPU:2_3GHZ
337S4029	1	IC,PCH,COUGARPOINT SLH9D,PRQ,BD82HM63	U1800	CRITICAL	
343S0534	1	IC,ASIC,GBIT ETHNET&SD CTRLR,686 QFN 8X8	U3900	CRITICAL	ENET:B0
343S0494	1	IC,ASIC,GBIT ETHNET&SD CTRLR,686 QFN 8X8	U3900	CRITICAL	ENET:A0
338S0753	1	IC,FW643-E,1394B PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	
333S0543	4	IC,SGRAM,GDDR5,32MX32.1.25GHz,E-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_512_SAMSUNG
333S0564	4	IC,SDRAM,GDDR5,32MX32,1.25GHz,A-DIE1.35V	U8400,U8450,U8500,U8550	CRITICAL	FB_512_HYNIX
333S0571	4	IC,SGRAM,GDDR5,64MX32,3.6GBPS,C-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_1G_SAMSUNG
333S0572	4	IC,SGRAM,GDDR5,64MX32,3.6GBPS,M-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_1G_HYNIX
337S3936	1	IC,GPU,AMD,WHISTLER,962FCBGA,40NM,ES	U8000	CRITICAL	
338S0945	1	Light Ridge,S LHAJ,FCBGA,15x15mmm	U3600	CRITICAL	T29:YES
353S3055	1	IC, P13VEDP212,x2 DISPLAYPORT 2:1 MUX, QFN	U9390	CRITICAL	

Programmed Parts-All Builds

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0777	1	IC,EEPROM,SERIAL,8KB,SOIC	U3690	CRITICAL	T29ROM:BLANK
341S2899	1	IC,T29 EEPROM,K92	U3690	CRITICAL	T29ROM:PROG
341S2384	1	IR,ENCORE II, CY7C63833-LFXC	U4800	CRITICAL	
335S0724	1	IC,GPU ROM,K91/F,K92	U8701	CRITICAL	GPUROM:BLANK
341S2957	1	IC,GPU ROM,K91/F,K92	U8701	CRITICAL	GPUROM:PROG
336S0042	1	IC,PLD,LATTICE,LFXP2-5E-5,132 BALL CSBGA	U9600	CRITICAL	GMUX_BLANK
341S2996	1	IC,GMUX,K92	U9600	CRITICAL	GMUX_PROG
337S3997	1	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29MCU:BLANK
341S2939	1	IC,PROGRAMMED MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29MCU:PROG

GPUROM will NOSUFFED @EVT

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
157S0058	157S0055		ALL	Delta alt to TDK Magnetics	
152S0896	152S0518		ALL	MAG LAYERS ALT TO CYNTEC	
152S0915	152S0796		ALL	MAG LAYERS ALT TO CYNTEC	
155S0457	155S0329		ALL	MAG LAYERS ALT TO MURATA	
516S0805	516S0806		ALL	FOXCONN ALT TO MOLEX	
353S2805	353S2603		ALL	Fairchild 8’ alt to 6’wafer	
127S0111	127S0060		ALL	Rohm alt to Kemet	
353S3085	353S1658		ALL	ST Micro alt to LT	(U5850)
152S0905	152S1307		ALL	Cyntec (used on K90i) as alt	(L7630)
353S3055	353S3151		ALL	Pericom alt to NXP DP Mux	(U9390)
376S0855	376S0613		ALL	radar8515240 Toshiba FET	(Q3200, etc)
870-1939	870-1698		ALL	Silver alt to Gold tall pogo pins	
870-2015	870-1699		ALL	Silver alt to Gold short pogo pins	
376S0972	376S0612		ALL	add ROHM part as 2nd source	
138S0676	138S0691		ALL	add Murata part as 2nd source	
128S0327	128S0264		ALL	add NEC part as 2nd source	
376S0977	376S0859		ALL	add new part as 2nd source	
138S0681	138S0638		ALL	add new part as 2nd source	(Q3888,Q9430)

SMC

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0895	1	IC,SMC,HS8/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341S2855	1	IC,SMC,DEVELOPMENT-PROTO,K92	U4900	CRITICAL	SMC_PROG:PROTO0
341S2855	1	IC,SMC,DEVELOPMENT-PROTO1,K92	U4900	CRITICAL	SMC_PROG:PROTO1
341S2995	1	IC,SMC,DEVELOPMENT-PROTO2,K92	U4900	CRITICAL	SMC_PROG:PROTO2
341S2862	1	IC,SMC,DEVELOPMENT-EVT,K92	U4900	CRITICAL	SMC_PROG:EVT
341S2865	1	IC,SMC,DEVELOPMENT-DVT,K92	U4900	CRITICAL	SMC_PROG:DVT
341S2868	1	IC,SMC,DEVELOPMENT-PVT,K92	U4900	CRITICAL	SMC_PROG:PVT

EFI

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0740	1	64 MBIT SPI SERIAL DUAL I/O FLASH	U6100	CRITICAL	BOOTROM_BLANK
341S2893	1	IC,EFI,ROM,PROTO, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO0
341S2934	1	IC,EFI,ROM,PROTO1, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO1
341S2991	1	IC,EFI,ROM,PROTO1, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO2
341S2894	1	IC,EFI,ROM,EVT, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:EVT
341S2895	1	IC,EFI,ROM,DVT, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:DVT
341S2896	1	IC,EFI,ROM,PVT, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PVT

Ethernet

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0539	1	IC,FLASH,SERIAL,SPI,1MBIT,2V7,8P,SOIC	U3990	CRITICAL	ENETROM_BLANK
341S2685	1	IC,ENET ROM,PROTO1,K92	U3990	CRITICAL	ENETROM_PROG:A0_SD
341S3027	1	IC,ENET ROM, PROTO2, EVT,DVT,PVT,K92	U3990	CRITICAL	ENETROM_PROG:B0_NOSD

PSOC

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S2902	1	IC,TP PSOC,PROTO,K90,K90i,K91,K91F,K92	U5701	CRITICAL	TPAD_PROG:PROTO1
341S3024	1	IC,TP PSOC,proto2,K90,K90i,K91,K91F,K92T	U5701	CRITICAL	TPAD_PROG:PROTO2
341S3024	1	IC,TP PSOC,proto1,EVT,K90,K90i,K91,K91F,K92T	U5701	CRITICAL	TPAD_PROG:EVT
341S3024	1	IC,TP PSOC,proto1,DVT,pVT,K90,K90i,K91,K91F,K92T	U5701	CRITICAL	TPAD_PROG:DVTPVT

SYNC_MASTER=K17_MLB SYNC_DATE=04/26/2010

PAGE TITLE

BOM Configuration

Apple Inc.

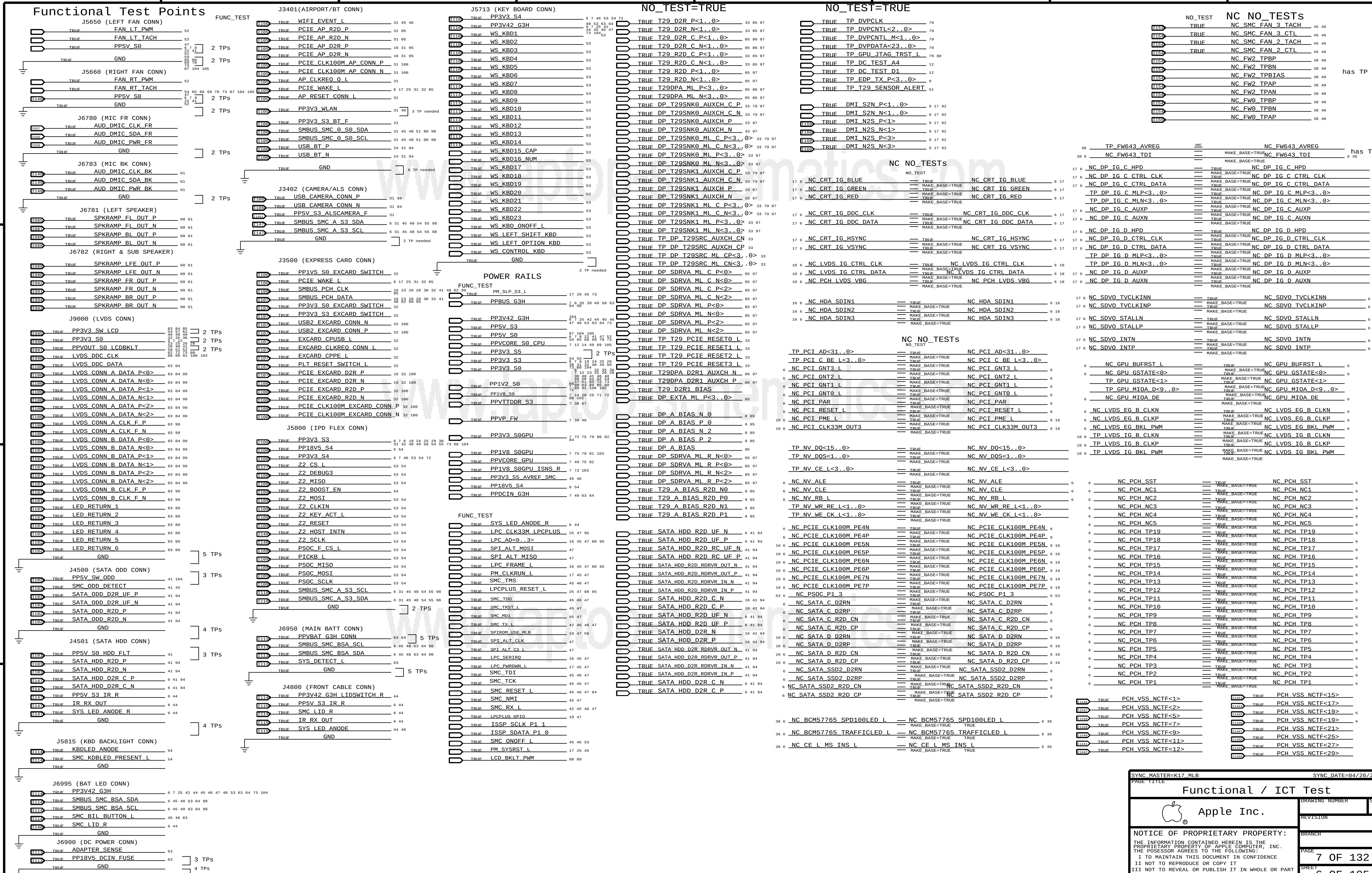
DRAWING NUMBER SIZE D

REVISION

BRANCH

PAGE 5 OF 132

SHEET 5 OF 105



SYNC_MASTER=K17_MLB SYNC_DATE=04/26/2010

PAGE TITLE

Functional / ICT Test

Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH

NOTICE OF PROPRIETARY PROPERTY:

PAGE 7 OF 132

SHEET 6 OF 105

"G3Hot" (Always-Present) Rails

PPBUS_G3H
PPVIN_S5_HS_COMPUTING_ISNS
PPVIN_S5_HS_OTHER_ISNS
PPVIN_S5_HS_GPU_ISNS
PPDCIN_G3H
PP3V42_G3H
PPVRTC_G3H

5V Rails

PP5V_S5
PP5V_S3
PP5V_S3_ISNS_R
PP5V_S0
PP5V_S0_ISNS_R
PP5V_SUS

3.3V/1.8V Rails

PP3V3_S5
PP3V3_S4
PP3V3_S5_ISNS_R
PP3V3_SUS
PP3V3_S3
PP3V3_S3_ISNS_R
PP3V3_S0
PP3V3_S0_ISNS_R
PP3V3_S0_ISNS_R
PP1V8_S0
PP1V8_S0_CPU_VCCPLL_R
PPVP_FW
PP3V3_FW_FWPHY
PP1V0_FW_FWPHY
PP1V5_S0
PP1V2_S0
PP1V05_SUS
PP1V05_S0
PPVCORE_S0_CPU
PPVCORE_S0_AXG
PPVCCSA_S0_CPU
PP1V5_S3_CPU_VCCDQ
PP1V05_S0_CPU_VCCPQE
PP3V3_ENET
PP1V2_ENET
PP3V3_T29
PP1V05_T29
PP15V_T29

"FW" (FireWire) Rails

1.5V/1.05V Rails

Chipset Rails

ENET Rails

T29 Rails

DDR Rails

PP1V5_S3
PP1V5_S3RS0
PP1V5_S3RS0_CPUDDR
PPVTTDDR_S3
PP0V75_S0_DDRVTT

"GPU" Rails

PPVCORE_GPU
PP3V3_S0GPU
PP1V5_S0GPU_ISNS_R
PP1V5R1V35_GPU_FB_ISNS
PP1V0_S0GPU_ISNS_R
PP1V0_S0GPU
PP1V8_S0GPU_ISNS_R
PP1V8_S0GPU

~2 mA

SYNC_MASTER=K17_MLB
SYNC_DATE=04/26/2010
PAGE TITLE
Power Aliases

Apple Inc.

DRAWING NUMBER
SIZE D
REVISION
BRANCH
PAGE 8 OF 132
SHEET 7 OF 105

Thermal Module Holes

Bottom GPU Right TM Hole — ZT0982 STDOFF-4.5OD.98H-1.1-3.48-TH
Right CPU TM Hole — ZT0984 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0981 STDOFF-4.5OD.98H-1.1-3.48-TH — Top GPU Center TM Hole
ZT0983 STDOFF-4.5OD.98H-1.1-3.48-TH — Left CPU TM Hole
ZT0980 STDOFF-4.5OD.98H-1.1-3.48-TH — Bottom CPU Left TM Hole
ZT0930 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0987 STDOFF-4.5OD.98H-1.1-3.48-TH — Bottom GPU Left TM Hole

Frame Holes

ZT0915 3R2P5 — GND
ZT0932 3R2P5
ZT0960 3R2P5
ZT0971 3R2P5
ZT0940 3R2P5
ZT0970 3R2P5
ZT0934 STDOFF-4.0OD3.35H-TH
ZT0931 STDOFF-4.0OD3.35H-TH
ZT0988 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0989 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0991 STDOFF-4.5OD.98H-1.1-3.48-TH

Bosses for Flex Protector Bracket

ZT0957 4.0OD1.65H-M1.6X0.35
ZT0958 4.0OD1.65H-M1.6X0.35

SH0920 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0936 1.4DIA-SHORT-EMI-MLB-M97-M98 — GND_CHASSIS_AUDIO_JACK
SH0911 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0910 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0913 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0912 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0914 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0923 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0924 2.0DIA-TALL-EMI-MLB-M97-M98
SH0916 2.0DIA-TALL-EMI-MLB-M97-M98
SH0917 2.0DIA-TALL-EMI-MLB-M97-M98
SH0918 2.0DIA-TALL-EMI-MLB-M97-M98
SH0919 2.0DIA-TALL-EMI-MLB-M97-M98
SH0930 2.0DIA-TALL-EMI-MLB-M97-M98
SH0921 2.0DIA-TALL-EMI-MLB-M97-M98
SH0931 2.0DIA-TALL-EMI-MLB-M97-M98
SH0922 2.0DIA-TALL-EMI-MLB-M97-M98
SH0932 2.0DIA-TALL-EMI-MLB-M97-M98
SH0902 2.0DIA-TALL-EMI-MLB-M97-M98
SH0900 2.0DIA-TALL-EMI-MLB-M97-M98
SH0934 2.0DIA-TALL-EMI-MLB-M97-M98
SH0933 2.0DIA-TALL-EMI-MLB-M97-M98
SH0903 2.0DIA-TALL-EMI-MLB-M97-M98
SH0901 2.0DIA-TALL-EMI-MLB-M97-M98
SH0935 2.0DIA-TALL-EMI-MLB-M97-M98

GMUX ALIASES

PM_ALL_GPU_PGOOD — MAKE_BASE=TRUE — 91 88 87 82 74 8 — PM_ALL_GPU_PGOOD — 8 74 82 87 88 91
TP_LVDS_MUX_SEL_EG — MAKE_BASE=TRUE — 88 8 — TP_LVDS_MUX_SEL_EG — 8 88
EG_RESET_L — MAKE_BASE=TRUE — 88 74 8 — EG_RESET_L — 8 74 88
LVDS_IG_BKL_ON — MAKE_BASE=TRUE — 88 18 8 — LVDS_IG_BKL_ON — 8 18 88
LVDS_IG_PANEL_PWR — MAKE_BASE=TRUE — 88 18 8 — LVDS_IG_PANEL_PWR — 8 18 88
LCD_BKLT_EN — MAKE_BASE=TRUE — 90 88 8 — LCD_BKLT_EN — 8 88 90
PEX_CLKREQ_L — MAKE_BASE=TRUE — 88 80 8 — PEX_CLKREQ_L — 8 80 88
PEG_CLKREQ_L — MAKE_BASE=TRUE — 88 16 8 — PEG_CLKREQ_L — 8 16 88
GND — GND — MAKE_BASE=TRUE
FW_PLUG_DET_L — MAKE_BASE=TRUE — 39 19 8 — FW_PLUG_DET_L — 8 19 39
FW643_WAKE_L — MAKE_BASE=TRUE — 39 38 8 — FW643_WAKE_L — 8 38 39

Unused SD card signals

TP_SDCONN_DATA<0..7> — MAKE_BASE=TRUE — 36 — SDCONN_DATA<0..7>
TP_SDCONN_CLK — MAKE_BASE=TRUE — 36 8 — TP_SDCONN_CLK — 8 36
TP_SDCONN_CMD — MAKE_BASE=TRUE — 36 8 — TP_SDCONN_CMD — 8 36
TP_SDCONN_DETECT_L — MAKE_BASE=TRUE — 36 8 — TP_SDCONN_DETECT_L — 8 36
TP_SDCONN_WP — MAKE_BASE=TRUE — 36 8 — TP_SDCONN_WP — 8 36
TP_ENET_CR_PWREN — MAKE_BASE=TRUE — 36 8 — TP_ENET_CR_PWREN — 8 36

AUDIO ALIASES

PP5V_S0 — 105 104 97 95 70 69 68 65 54 52 47 41 22 7 6
XW0900 SM — PP5V_S0_AUDIO — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=5V — 57
XW0901 SM — PP5V_S0_AUDIO_AMP_R — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=5V — 60
XW0902 SM — PP5V_S0_AUDIO_AMP_L — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=5V — 60

Digital Ground

GND — MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.11MM, VOLTAGE=0V

LVDS_IG_PANEL_PWR — 88 18 8 — R0902 100K 5% 1/16W MF-LF 402 — 2

Unused USB ports

PP3V3_S3 — 6 7 18 24 25 29 30 31 32 48 49 50 54 55 73 88 104
R0915 10K 5% 1/16W MF-LF 402
R0916 10K 5% 1/16W MF-LF 402
USB_T29A_N — 24 94
USB_T29A_P — 24 94

Heat spreader mounting boss for T29 router

SH0940 STDOFF-4.0OD1.85H-SM
SH0941 STDOFF-4.0OD1.85H-SM

Heat spreader mounting boss for PCH

SH0942 STDOFF-4.0OD2.23H-SM
SH0943 STDOFF-4.0OD2.23H-SM

CPU signals

CPU_VID<0..6> — MAKE_BASE=TRUE — 92 — CPUIMVP_VID<0..6>
GFX_VID<0..6> — MAKE_BASE=TRUE — 92 — GFXIMVP_VID<0..6>
MEMVTT_EN — MAKE_BASE=TRUE — 67 29 8 — MEMVTT_EN — 8 29 67

Unused PEG lanes

NC_PEG_D2R_P<15..12> — MAKE_BASE=TRUE — 9 — =PEG_D2R_P<15..12>
NC_PEG_D2R_N<15..12> — MAKE_BASE=TRUE — 9 — =PEG_D2R_N<15..12>
NC_PEG_R2D_C_P<15..12> — MAKE_BASE=TRUE — 9 — =PEG_R2D_C_P<15..12>
NC_PEG_R2D_C_N<15..12> — MAKE_BASE=TRUE — 9 — =PEG_R2D_C_N<15..12>

GPU signals

PEG_D2R_P<7..0> — MAKE_BASE=TRUE — 92 74 — =PEG_D2R_P<7..0> — 9
PEG_D2R_N<7..0> — MAKE_BASE=TRUE — 92 74 — =PEG_D2R_N<7..0> — 9
PEG_R2D_C_P<7..0> — MAKE_BASE=TRUE — 92 74 — =PEG_R2D_C_P<7..0> — 9
PEG_R2D_C_N<7..0> — MAKE_BASE=TRUE — 92 74 — =PEG_R2D_C_N<7..0> — 9
DP_IG_AUX_CH_P — MAKE_BASE=TRUE — 94 84 17 8 — DP_IG_AUX_CH_P — 8 17 84 94
DP_IG_AUX_CH_N — MAKE_BASE=TRUE — 94 84 17 8 — DP_IG_AUX_CH_N — 8 17 84 94
DP_IG_DDC_CLK — MAKE_BASE=TRUE — 84 80 17 8 — DP_IG_DDC_CLK — 8 17 80 84
DP_IG_DDC_DATA — MAKE_BASE=TRUE — 84 80 17 8 — DP_IG_DDC_DATA — 8 17 80 84
DP_IG_HPD — MAKE_BASE=TRUE — 84 17 8 — DP_IG_HPD — 8 17 84

T29 Signals

PCIE_T29_D2R_P<3..0> — MAKE_BASE=TRUE — 95 33 — =PEG_D2R_P<11..8> — 9
PCIE_T29_D2R_N<3..0> — MAKE_BASE=TRUE — 95 33 — =PEG_D2R_N<11..8> — 9
PCIE_T29_R2D_C_P<3..0> — MAKE_BASE=TRUE — 95 33 — =PEG_R2D_C_P<11..8> — 9
PCIE_T29_R2D_C_N<3..0> — MAKE_BASE=TRUE — 95 33 — =PEG_R2D_C_N<11..8> — 9

Unused T29 Ports

T29_D2R_P<2..3> — MAKE_BASE=TRUE NO_TEST=TRUE — 97 — NC_T29_D2RP<2..3> — 33
T29_D2R_N<2..3> — MAKE_BASE=TRUE NO_TEST=TRUE — 97 — NC_T29_D2RN<2..3> — 33
T29_R2D_C_P<2..3> — MAKE_BASE=TRUE NO_TEST=TRUE — 97 — NC_T29_R2D_CP<2..3> — 33
T29_R2D_C_N<2..3> — MAKE_BASE=TRUE NO_TEST=TRUE — 97 — NC_T29_R2D_CN<2..3> — 33
T29_LSE0_LSOE3 — MAKE_BASE=TRUE NO_TEST=TRUE — 33 8 — T29_LSE0_LSOE3 — 8 33
T29_LSE0_LSOE2 — MAKE_BASE=TRUE NO_TEST=TRUE — 33 8 — T29_LSE0_LSOE2 — 8 33

T29 / GMUX JTAG Signals

JTAG_ISP_TCK — MAKE_BASE=TRUE — 88 33 23 19 8 — JTAG_ISP_TCK — 8 19 23 33 88
JTAG_ISP_TDI — MAKE_BASE=TRUE — 88 33 19 8 — JTAG_ISP_TDI — 8 19 33 88
JTAG_ISP_TDO — MAKE_BASE=TRUE — 88 33 19 8 — JTAG_ISP_TDO — 8 19 33 88

T29_A_BIAS caps

SIGNAL_MODEL=EMPTY
T29_A_BIAS_R — 86 8 — R0926 51 5% 1/20W MF 201 — T29_A_BIAS_D2R_P1 — 86
C0906 0.01UF 10% 10V X5R 201 SIGNAL_MODEL=EMPTY

SIGNAL_MODEL=EMPTY
T29_A_BIAS_R — 86 8 — R0927 51 5% 1/20W MF 201 — T29_A_BIAS_D2R_N1 — 86
C0907 0.01UF 10% 10V X5R 201 SIGNAL_=EMPTY

DP_A_BIAS caps

DP_A_BIAS_P_2 — 85 6 — SIGNAL_MODEL=EMPTY — C0910 0.01UF 10% 10V X5R 201
DP_A_BIAS_P_0 — 85 6 — SIGNAL_MODEL=EMPTY — C0911 0.01UF 10% 10V X5R 201

T29BST:N
PPBUS_G3H — 90 64 63 50 49 39 35 7 6 — R0950 0 5% 1/8W MF-LF 805 — PP15V_T29 — 7 35 86

USB Hub Aliases

EXCARD_OC_L — MAKE_BASE=TRUE — 32 24 8 — EXCARD_OC_L — 8 24 32
USB_EXTC_OC_L — MAKE_BASE=TRUE — 43 24 8 — USB_EXTC_OC_L — 8 24 43
USB_EXCARD_N — MAKE_BASE=TRUE — 100 32 24 8 — USB_EXCARD_N — 8 24 32 100
USB_EXCARD_P — MAKE_BASE=TRUE — 100 32 24 8 — USB_EXCARD_P — 8 24 32 100

Rev. A NCs

NC_ISNS_P1V05S0PCH_N — MAKE_BASE=TRUE — 8 — NC_ISNS_P1V05S0PCH_N — 8
NC_ISNS_P1V05S0PCH_P — MAKE_BASE=TRUE — 8 — NC_ISNS_P1V05S0PCH_P — 8
NC_ISNS_P3V3S0MPCH_N — MAKE_BASE=TRUE — 8 — NC_ISNS_P3V3S0MPCH_N — 8
NC_ISNS_P3V3S0MPCH_P — MAKE_BASE=TRUE — 8 — NC_ISNS_P3V3S0MPCH_P — 8
NC_ISNS_PVTTS0PCH_N — MAKE_BASE=TRUE — 8 — NC_ISNS_PVTTS0PCH_N — 8
NC_ISNS_PVTTS0PCH_P — MAKE_BASE=TRUE — 8 — NC_ISNS_PVTTS0PCH_P — 8

T29_A_BIAS caps

SIGNAL_MODEL=EMPTY
T29_A_BIAS_R — 86 8 — R0921 51 5% 1/20W MF 201 — T29_A_BIAS_R2D_P0 — 6 85
C0901 0.01UF 10% 10V X5R 201 SIGNAL_MODEL=EMPTY

SIGNAL_MODEL=EMPTY
T29_A_BIAS_R — 86 8 — R0922 51 5% 1/20W MF 201 — T29_A_BIAS_R2D_N0 — 6 85
C0902 0.01UF 10% 10V X5R 201 SIGNAL_MODEL=EMPTY

SIGNAL_MODEL=EMPTY
T29_A_BIAS_R — 86 8 — R0923 51 5% 1/20W MF 201 — T29_A_BIAS_R2D_P1 — 6 85
C0903 0.01UF 10% 10V X5R 201 SIGNAL_MODEL=EMPTY

SIGNAL_MODEL=EMPTY
T29_A_BIAS_R — 86 8 — R0924 51 5% 1/20W MF 201 — T29_A_BIAS_R2D_N1 — 6 85
C0904 0.01UF 10% 10V X5R 201 SIGNAL_MODEL=EMPTY

DP_A_BIAS caps

DP_A_BIAS_N_2 — 85 6 — SIGNAL_MODEL=EMPTY — C0905 0.01UF 10% 10V X5R 201
DP_A_BIAS_N_0 — 85 6 — SIGNAL_MODEL=EMPTY — C0908 0.01UF 10% 10V X5R 201

SYNC_MASTER=K17_MLB — SYNC_DATE=04/26/2010
PAGE TITLE: Signal Aliases
Apple Inc.
DRAWING NUMBER — SIZE: D
REVISION
BRANCH
PAGE: 9 OF 132
SHEET: 8 OF 105

PP1V05_S0 → R1010 24.9 1% 1/16W MF-LF 402 → CPU_PEG_COMP

U1000 SANDY-BRIDGE MOBILE-REV1 BGA (SYM 1 OF 11) OMIT

DMI
- DMI_S2N_N<0> N10 → DMI_RX_0*
- DMI_S2N_N<1> R10 → DMI_RX_1*
- DMI_S2N_N<2> R8 → DMI_RX_2*
- DMI_S2N_N<3> U10 → DMI_RX_3*
- DMI_S2N_P<0> N8 → DMI_RX_0
- DMI_S2N_P<1> T9 → DMI_RX_1
- DMI_S2N_P<2> R6 → DMI_RX_2
- DMI_S2N_P<3> U8 → DMI_RX_3
- DMI_N2S_N<0> N4 → DMI_TX_0*
- DMI_N2S_N<1> R4 → DMI_TX_1*
- DMI_N2S_N<2> P1 → DMI_TX_2*
- DMI_N2S_N<3> U6 → DMI_TX_3*
- DMI_N2S_P<0> N2 → DMI_TX_0
- DMI_N2S_P<1> R2 → DMI_TX_1
- DMI_N2S_P<2> P3 → DMI_TX_2
- DMI_N2S_P<3> T5 → DMI_TX_3

INTEL FLEXIBLE DISPLAY INTERFACE SIGNALS
- FDI_DATA_N<0> V7 → FDI_TX_0*
- FDI_DATA_N<1> W8 → FDI_TX_1*
- FDI_DATA_N<2> AA8 → FDI_TX_2*
- FDI_DATA_N<3> AC10 → FDI_TX_3*
- FDI_DATA_N<4> U4 → FDI_TX_4*
- FDI_DATA_N<5> W2 → FDI_TX_5*
- FDI_DATA_N<6> V1 → FDI_TX_6*
- FDI_DATA_N<7> Y5 → FDI_TX_7*
- FDI_DATA_P<0> W6 → FDI_TX_0
- FDI_DATA_P<1> W10 → FDI_TX_1
- FDI_DATA_P<2> Y9 → FDI_TX_2
- FDI_DATA_P<3> AA10 → FDI_TX_3
- FDI_DATA_P<4> U2 → FDI_TX_4
- FDI_DATA_P<5> W4 → FDI_TX_5
- FDI_DATA_P<6> V3 → FDI_TX_6
- FDI_DATA_P<7> AA6 → FDI_TX_7
- FDI_FSYNC<0> AC8 → FDI0_FSYNC
- FDI_FSYNC<1> AA2 → FDI1_FSYNC
- FDI_INT AD9 → FDI_INT
- FDI_LSYNC<0> AB7 → FDI0_LSYNC
- FDI_LSYNC<1> AB3 → FDI1_LSYNC

EMBEDDED DISPLAY PORT
- TP_EDP_TX_N<0> AG2 → EDP_TX_0*
- TP_EDP_TX_N<1> AF1 → EDP_TX_1*
- TP_EDP_TX_N<2> AE6 → EDP_TX_2*
- TP_EDP_TX_N<3> AG6 → EDP_TX_3*
- TP_EDP_TX_P<0> AG4 → EDP_TX_0
- TP_EDP_TX_P<1> AF3 → EDP_TX_1
- TP_EDP_TX_P<2> AF7 → EDP_TX_2
- TP_EDP_TX_P<3> AG8 → EDP_TX_3
- TP_EDP_AUX_P AE4 → EDP_AUX
- TP_EDP_AUX_N AE2 → EDP_AUX*
- CPU_EDP_COMP AB1 → EDP_ICOMPO
- AC2 → EDP_COMPIO
- CPU_EDP_HPD AE8 → EDP_HPD

PP1V05_S0 → R1031 10K 1% 1/16W MF-LF 402 → R1030 24.9 1% 1/16W MF-LF 402 → CPU_EDP_COMP

PLACE_NEAR=U1000.AB1:12.7mm

10K PU disables eDP HPD

CPU_CFG<4> should be pulled down to enable EDP

PCI EXPRESS BASED INTERFACE SIGNALS
- PEG_ICOMPI G2 ← CPU_PEG_COMP
- PEG_ICOMPO H1
- PEG_RCOMPO F3
- PEG_RX_0* F23 → =PEG_D2R_N<0>
- PEG_RX_1* H23 → =PEG_D2R_N<1>
- PEG_RX_2* H21 → =PEG_D2R_N<2>
- PEG_RX_3* H19 → =PEG_D2R_N<3>
- PEG_RX_4* J20 → =PEG_D2R_N<4>
- PEG_RX_5* G18 → =PEG_D2R_N<5>
- PEG_RX_6* K17 → =PEG_D2R_N<6>
- PEG_RX_7* F15 → =PEG_D2R_N<7>
- PEG_RX_8* H15 → =PEG_D2R_N<8>
- PEG_RX_9* H13 → =PEG_D2R_N<9>
- PEG_RX_10* H11 → =PEG_D2R_N<10>
- PEG_RX_11* J12 → =PEG_D2R_N<11>
- PEG_RX_12* E8 → NC_PEG_D2R_N<12>
- PEG_RX_13* G10 → NC_PEG_D2R_N<13>
- PEG_RX_14* J8 → NC_PEG_D2R_N<14>
- PEG_RX_15* F7 → NC_PEG_D2R_N<15>
- PEG_RX_0 G22 → =PEG_D2R_P<0>
- PEG_RX_1 K23 → =PEG_D2R_P<1>
- PEG_RX_2 K21 → =PEG_D2R_P<2>
- PEG_RX_3 F19 → =PEG_D2R_P<3>
- PEG_RX_4 K19 → =PEG_D2R_P<4>
- PEG_RX_5 H17 → =PEG_D2R_P<5>
- PEG_RX_6 K15 → =PEG_D2R_P<6>
- PEG_RX_7 G14 → =PEG_D2R_P<7>
- PEG_RX_8 J16 → =PEG_D2R_P<8>
- PEG_RX_9 K13 → =PEG_D2R_P<9>
- PEG_RX_10 F11 → =PEG_D2R_P<10>
- PEG_RX_11 K11 → =PEG_D2R_P<11>
- PEG_RX_12 F9 → NC_PEG_D2R_P<12>
- PEG_RX_13 H9 → NC_PEG_D2R_P<13>
- PEG_RX_14 H7 → NC_PEG_D2R_P<14>
- PEG_RX_15 G6 → NC_PEG_D2R_P<15>
- PEG_TX_0* A22 → =PEG_R2D_C_N<0>
- PEG_TX_1* B23 → =PEG_R2D_C_N<1>
- PEG_TX_2* C18 → =PEG_R2D_C_N<2>
- PEG_TX_3* D21 → =PEG_R2D_C_N<3>
- PEG_TX_4* B19 → =PEG_R2D_C_N<4>
- PEG_TX_5* E20 → =PEG_R2D_C_N<5>
- PEG_TX_6* A14 → =PEG_R2D_C_N<6>
- PEG_TX_7* D17 → =PEG_R2D_C_N<7>
- PEG_TX_8* B15 → =PEG_R2D_C_N<8>
- PEG_TX_9* E16 → =PEG_R2D_C_N<9>
- PEG_TX_10* D13 → =PEG_R2D_C_N<10>
- PEG_TX_11* A10 → =PEG_R2D_C_N<11>
- PEG_TX_12* B11 → NC_PEG_R2D_C_N<12>
- PEG_TX_13* D9 → NC_PEG_R2D_C_N<13>
- PEG_TX_14* B7 → NC_PEG_R2D_C_N<14>
- PEG_TX_15* E12 → NC_PEG_R2D_C_N<15>
- PEG_TX_0 C22 → =PEG_R2D_C_P<0>
- PEG_TX_1 D23 → =PEG_R2D_C_P<1>
- PEG_TX_2 A18 → =PEG_R2D_C_P<2>
- PEG_TX_3 B21 → =PEG_R2D_C_P<3>
- PEG_TX_4 D19 → =PEG_R2D_C_P<4>
- PEG_TX_5 F21 → =PEG_R2D_C_P<5>
- PEG_TX_6 C14 → =PEG_R2D_C_P<6>
- PEG_TX_7 B17 → =PEG_R2D_C_P<7>
- PEG_TX_8 D15 → =PEG_R2D_C_P<8>
- PEG_TX_9 F17 → =PEG_R2D_C_P<9>
- PEG_TX_10 B13 → =PEG_R2D_C_P<10>
- PEG_TX_11 C10 → =PEG_R2D_C_P<11>
- PEG_TX_12 D11 → NC_PEG_R2D_C_P<12>
- PEG_TX_13 B9 → NC_PEG_R2D_C_P<13>
- PEG_TX_14 D7 → NC_PEG_R2D_C_P<14>
- PEG_TX_15 F13 → NC_PEG_R2D_C_P<15>

NOTE:
Intel is investigating processor driven VREF_DQ generation.
This connection is to support the same.

NOSTUFF R1021 0 5% 1/16W MF-LF 402
- PP0V75_S3_MEM_VREFDQ_A → CPU_MEM_VREFDQ_A
- R1020 1K 1% 1/16W MF-LF 402 → CPU_MEM_VREFDQ_B

NOSTUFF R1023 0 5% 1/16W MF-LF 402
- PP0V75_S3_MEM_VREFDQ_B
- R1022 1K 1% 1/16W MF-LF 402

U1000 SANDY-BRIDGE MOBILE-REV1 BGA (5 OF 11) RESERVED OMIT
- CPU_CFG<0> B57 CFG_0 (IPU)
- CPU_CFG<1> D57 CFG_1 (IPU)
- CPU_CFG<2> B55 CFG_2 (IPU)
- CPU_CFG<3> A54 CFG_3 (IPU)
- CPU_CFG<4> A58 CFG_4 (IPU)
- CPU_CFG<5> D55 CFG_5 (IPU)
- CPU_CFG<6> C56 CFG_6 (IPU)
- CPU_CFG<7> E54 CFG_7 (IPU)
- CPU_CFG<8> J54 CFG_8 (IPU)
- CPU_CFG<9> G56 CFG_9 (IPU)
- CPU_CFG<10> F55 CFG_10 (IPU)
- CPU_CFG<11> K55 CFG_11 (IPU)
- CPU_CFG<12> F57 CFG_12 (IPU)
- CPU_CFG<13> E58 CFG_13 (IPU)
- CPU_CFG<14> H57 CFG_14 (IPU)
- CPU_CFG<15> H55 CFG_15 (IPU)
- CPU_CFG<16> D53 CFG_16 (IPU)
- CPU_CFG<17> K57 CFG_17 (IPU)

RESERVED
- NC BB17 RSVD_1
- NC AY17 RSVD_2
- NC BD29 RSVD_3
- NC BD33 RSVD_4
- NC BC30 RSVD_5
- NC BE32 RSVD_6
- NC AW42 RSVD_7
- NC BA48 RSVD_8
- NC BC42 RSVD_9
- NC AW46 RSVD_10
- NC BG26 RSVD_11
- NC BB25 RSVD_12
- NC BG34 RSVD_13
- NC BH35 RSVD_14
- NC BJ34 RSVD_15
- NC BF35 RSVD_16
- NC BF41 RSVD_17
- NC BH43 RSVD_18
- NC BJ42 RSVD_19
- NC BF43 RSVD_20
- NC AW50 RSVD_22
- NC BB57 RSVD_23
- NC BF63 RSVD_24
- NC AD5 RSVD_25
- NC AH5 RSVD_26
- NC AJ6 RSVD_27
- BF3 RSVD_28 (DDR_VREF0)
- BG4 RSVD_29 (DDR_VREF1)
- NC BD19 RSVD_30
- NC AY45 RSVD_31
- NC AY41 RSVD_32
- NC BG62 RSVD_33
- NC BB43 RSVD_34
- NC D49 RSVD_35
- NC B53 RSVD_36
- NC G52 RSVD_38
- NC G64 RSVD_39
- NC AJ10 RSVD_40
- NC BE6 RSVD_41
- NC AA4 RSVD_42
- NC AC4 RSVD_43
- NC AC6 RSVD_44
- NC C52 RSVD_45
- NC D3 RSVD_46
- NC C4 RSVD_47
- NC C24 RSVD_48
- NC D25 RSVD_49
- NC B25 RSVD_50
- CPU_THERMD_P K47 RSVD_51 (THERMDA)
- CPU_THERMD_N H47 RSVD_52 (THERMDC)
- RSVD_53 F5 → NC
- RSVD_54 K9 → NC
- RSVD_55 H5 → NC
- RSVD_56 L10 → NC
- RSVD_57 G4 → NC
- RSVD_58 K7 → NC
- RSVD_59 K5 → NC
- RSVD_60 M9 → NC
- RSVD_61 L6 → NC
- RSVD_62 J2 → NC
- RSVD_63 L2 → NC
- RSVD_64 P7 → NC
- RSVD_65 M5 → NC
- RSVD_66 J4 → NC
- RSVD_67 L4 → NC
- RSVD_68 N6 → NC
- RSVD_69 G48 → NC
- RSVD_70 K49 → NC
- RSVD_71 H49 → NC
- RSVD_72 J50 → NC
- RSVD_78 AY13 → NC
- RSVD_79 BB13 → NC
- RSVD_80 BB15 → NC
- RSVD_81 AY15 → NC
- RSVD_82 AW14 → NC
- RSVD_83 BD13 → NC
- RSVD_84 BA16 → NC
- RSVD_85 BE16 → NC
- RSVD_86 BD15 → NC
- RSVD_87 BC14 → NC
- RSVD_88 BF19 → NC
- RSVD_89 BH19 → NC
- RSVD_90 BF21 → NC
- RSVD_91 BH21 → NC
- RSVD_92 BF23 → NC
- RSVD_93 BH23 → NC
- RSVD_94 BF25 → NC
- RSVD_95 BH25 → NC
- RSVD_96 BJ22 → NC
- RSVD_97 BG22 → NC

CPU_CFG<7> CPU_CFG<6> CPU_CFG<5> CPU_CFG<4> CPU_CFG<2>
- NOSTUFF R1042 1K 5% 1/16W MF-LF 402
- EDP R1044 1K 5% 1/16W MF-LF 402
- R1045 1K 5% 1/16W MF-LF 402
- NOSTUFF R1046 1K 5% 1/16W MF-LF 402
- NOSTUFF R1047 1K 5% 1/16W MF-LF 402

CPU_CFG<16> CPU_CFG<3> CPU_CFG<1> CPU_CFG<0>
- NOSTUFF R1040 1K 5% 1/16W MF-LF 402
- NOSTUFF R1041 1K 5% 1/16W MF-LF 402
- NOSTUFF R1043 1K 5% 1/16W MF-LF 402
- NOSTUFF R1049 1K 5% 1/16W MF-LF 402

These can be Placed close to J2500 and Only for debug access

FOR SANDYBRIDGE PROCESSOR

CFG [7] :PEG DEFER TRAINING	1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB 0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION	11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE	1 = DISABLED 0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL	1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL	1 = NORMAL OPERATION 0 = LANES REVERSED

PAGE TITLE: CPU DMI/PEG/FDI/RSVD

Apple Inc.

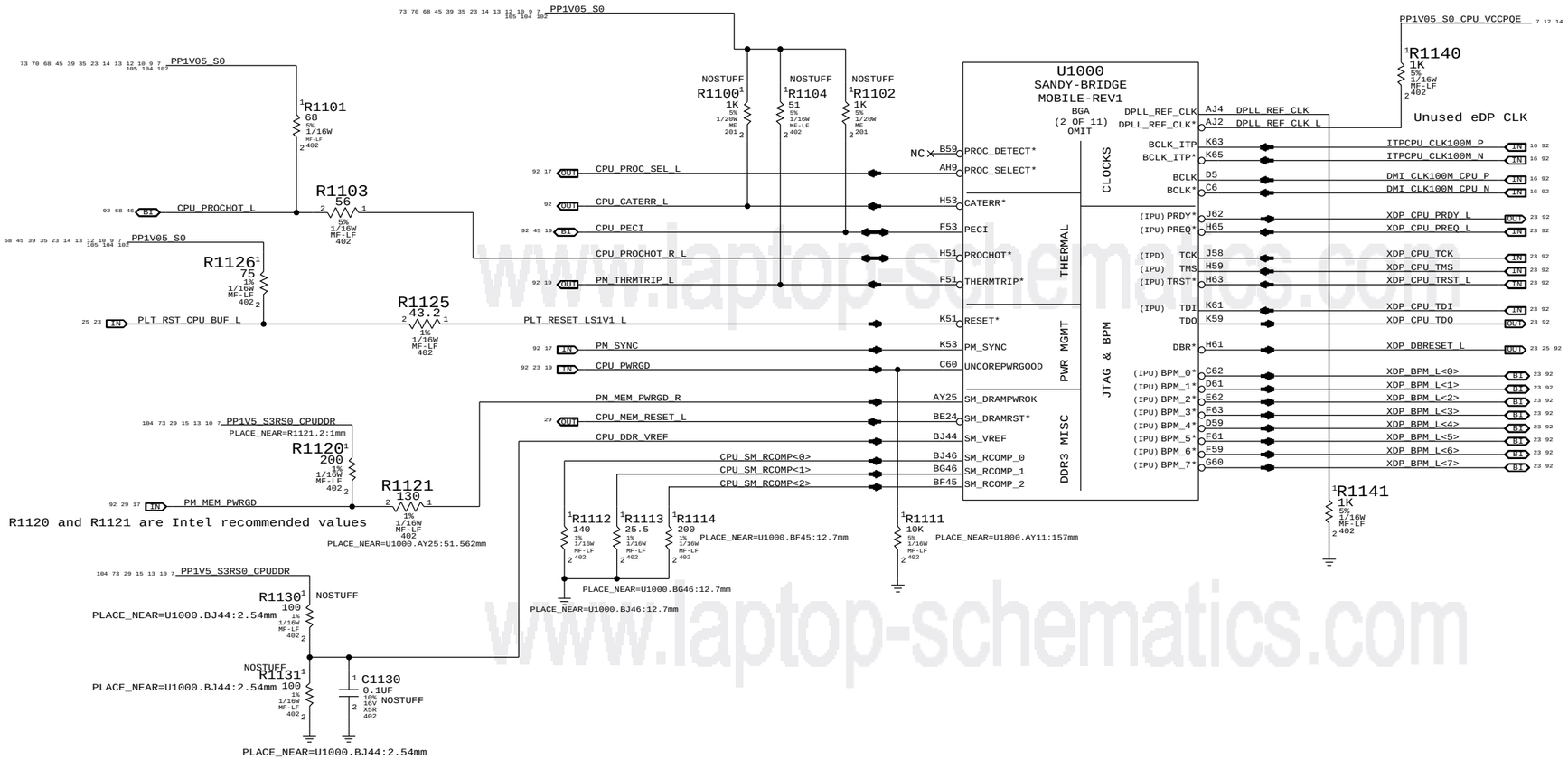
DRAWING NUMBER | SIZE D

REVISION

BRANCH

PAGE 10 OF 132

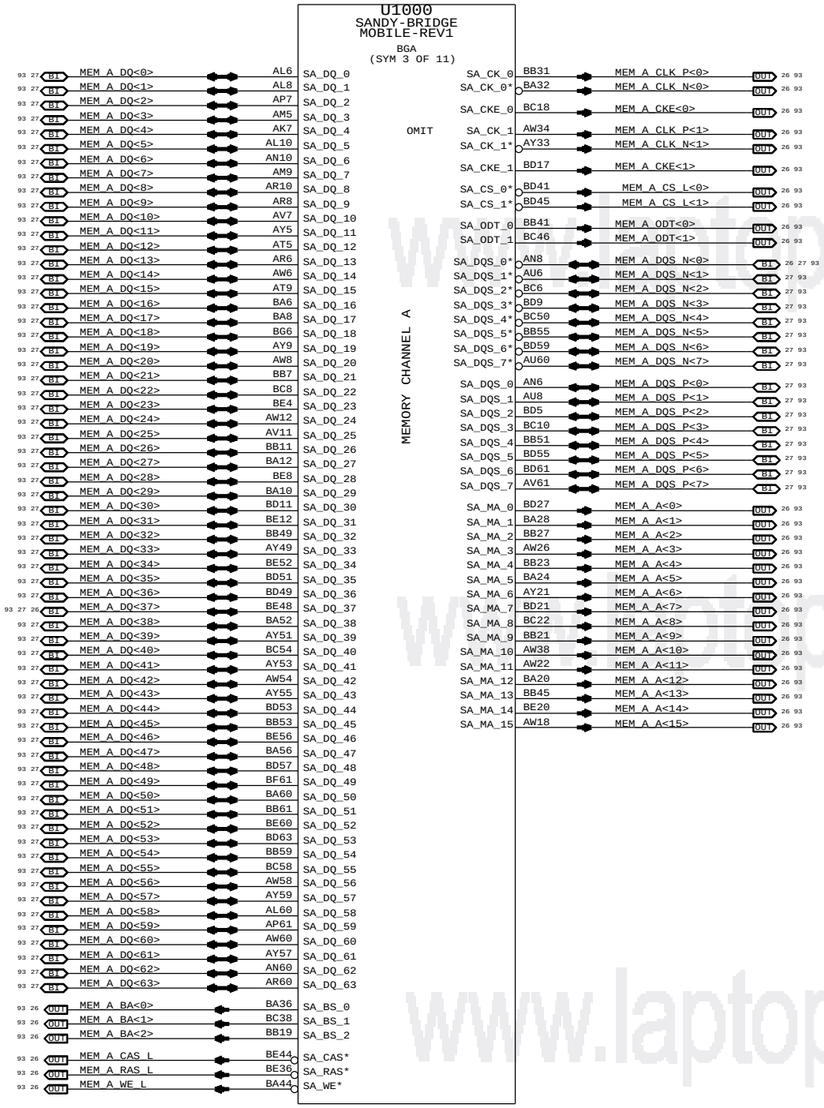
SHEET 9 OF 105

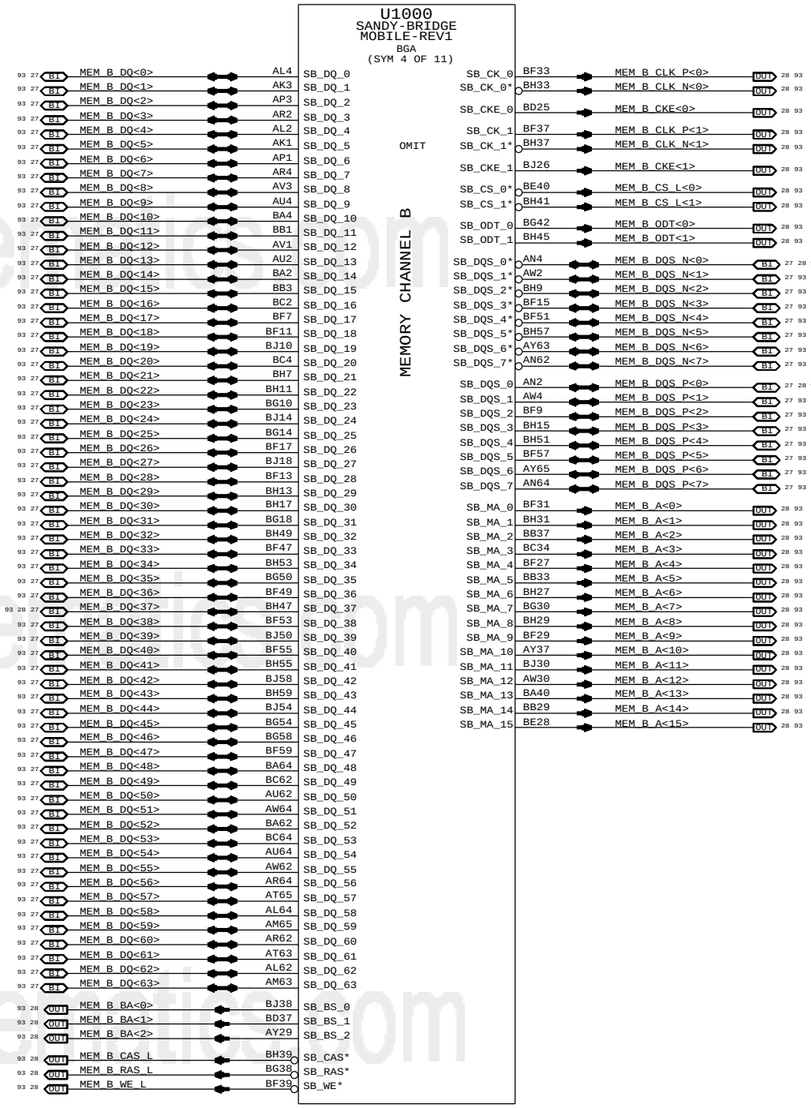


PAGE TITLE
CPU CLOCK/MISC/JTAG

Apple Inc.

DRAWING NUMBER
SIZE D
REVISION
BRANCH
PAGE 11 OF 132
SHEET 10 OF 105



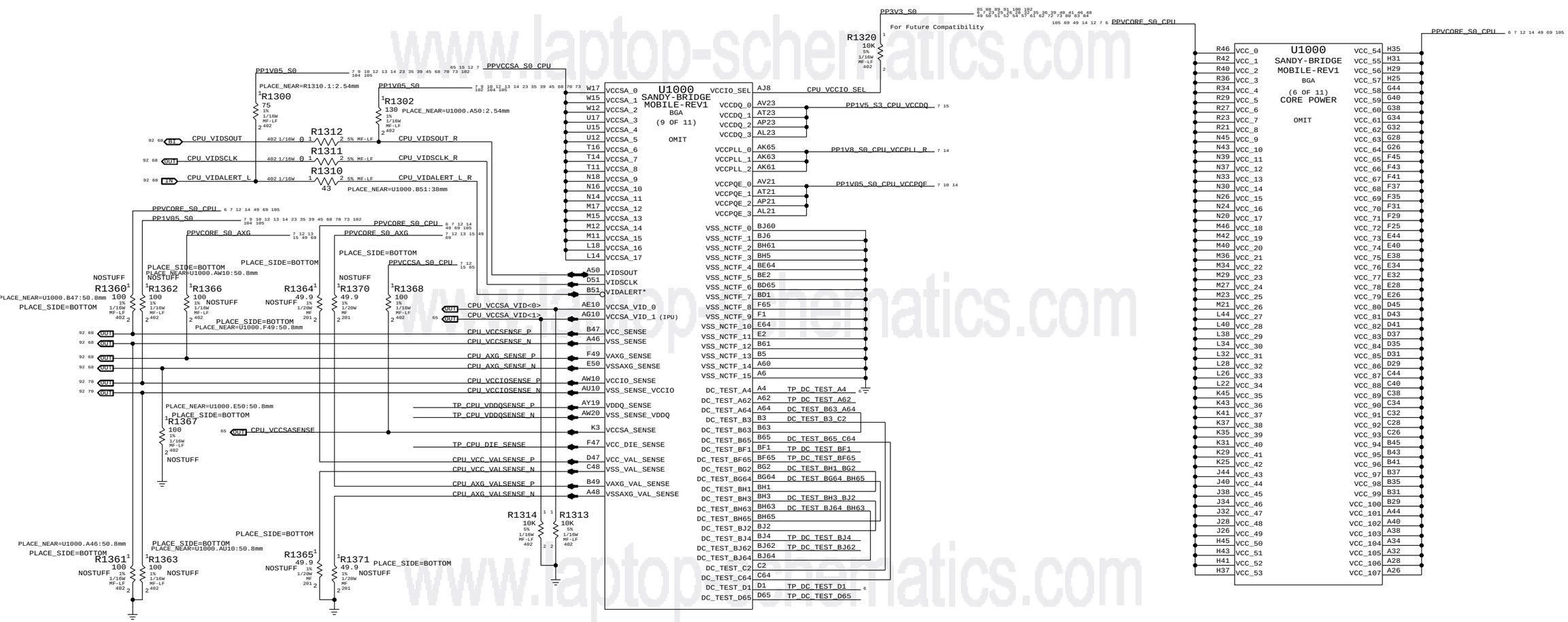


SYNC_DATE=04/26/2010

PAGE TITLE
CPU DDR3 INTERFACES

Apple Inc.

DRAWING NUMBER
SIZE D
REVISION
BRANCH
PAGE 12 OF 132
SHEET 11 OF 105



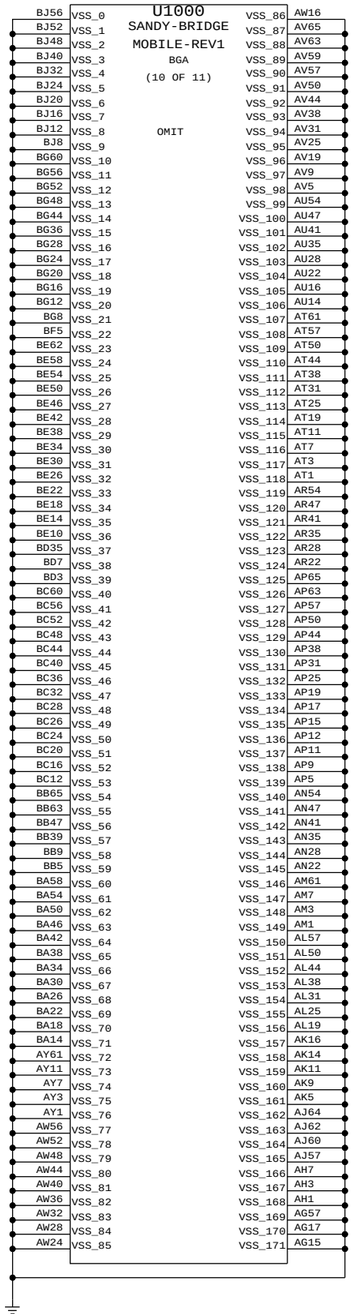
PLACEMENT NOTE: Please place all sense line resistors on BOTTOM side.
NOTE: Intel validation sense lines per doc 439028 rev1.0
HR_PPDG sections 6.2.1 and 6.3.1.

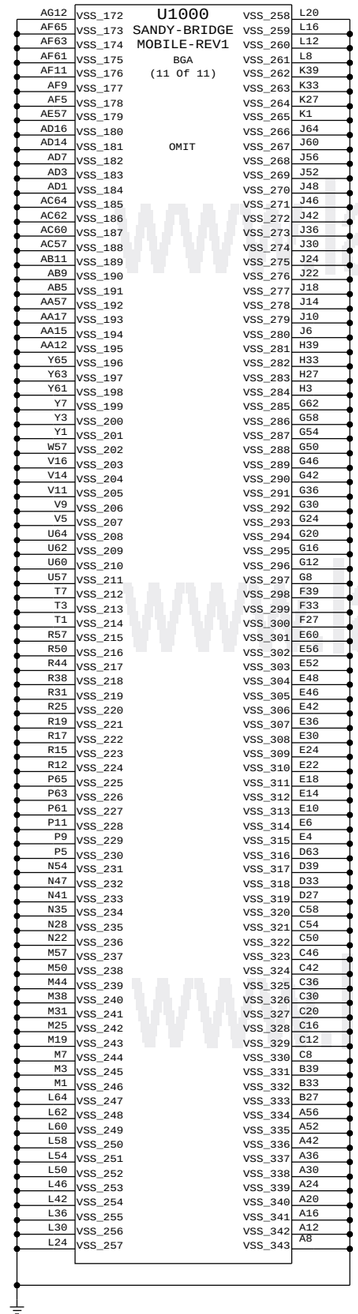
SYNC_MASTER=K91_MLB SYNC_DATE=07/16/2010

PAGE TITLE: CPU POWER

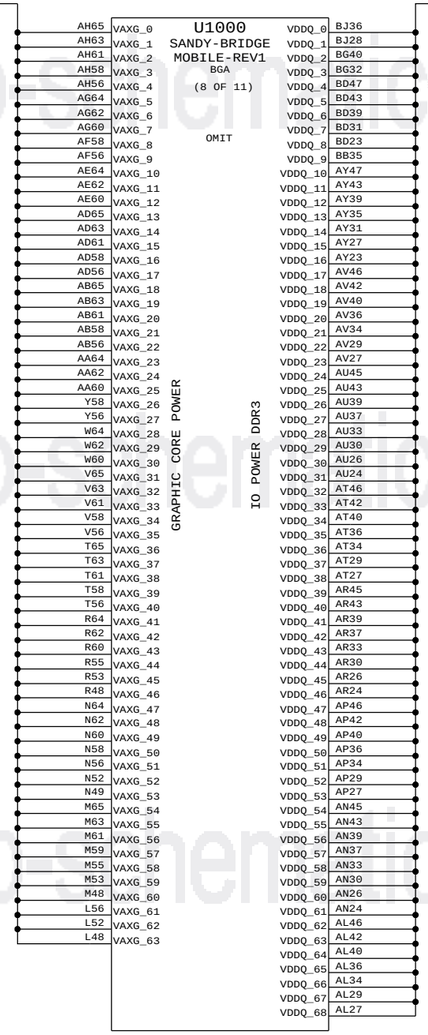
Apple Inc.

DRAWING NUMBER: SIZE: D
REVISION:
BRANCH:
PAGE: 13 OF 132
SHEET: 12 OF 105



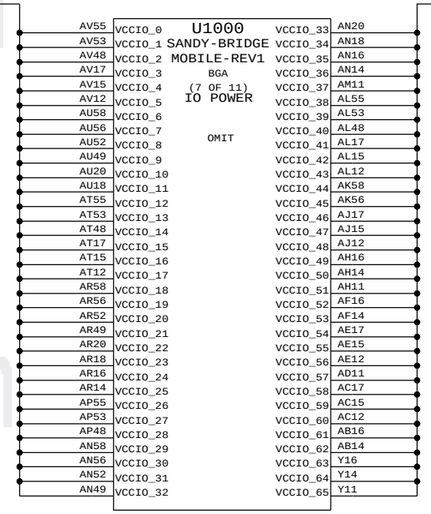


PPVCORE_S0_AXG (69 49 15 12 7)



PP1V5_S3RS0_CPUDDR (7 10 15 29 73 104)

PP1V05_S0 (39 23 14 13 12 10 9 8 105 104 102 73 70 68 45 39)



PP1V05_S0 (7 9 10 12 13 14 23 35 39 45 66 70 73 102 104 105)

PAGE TITLE
CPU POWER AND GND

Apple Inc.

DRAWING NUMBER
SIZE D
REVISION
BRANCH
PAGE 14 OF 132
SHEET 13 OF 105

CPU VCORE DECOUPLING

Intel recommendation: 4x 470uF 4mOhm, 2x 470uF 4mOhm (NOSTUFF), 16x 22uF 0805, 4x 10uF 0603, 20x 1uF 0402, 28x 1uF 0402 (NOSTUFF)
Apple Implementation: 4x 470uF 4mOhm, 1x 470uF 4mOhm (NOSTUFF), 16x 22uF 0603, 4x 10uF 0402, 20x 1uF 0402, 28x 1uF 0201 (NOSTUFF), 4x 22uF 0603 (NOSTUFF)

105 69 49 12 7 6 PPVCORE_S0_CPU

PLACEMENT_NOTE (C1600-C16C7):
Place on bottom side of U1000

C1600 C1601 C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609 C1610 C1611 C1612 C1613 C1614 C1615 C1616 C1617 C1618 C1619
1UF 20% 10V X5R 402

NOSTUFF C16A0 C16A1 C16A2 C16A3 C16A4 C16A5 C16A6 C16A7 C16A8 C16A9 C16B0 C16B1 C16B2 C16B3 C16B4 C16B5 C16B6 C16B7 C16B8 C16B9
1UF 20% 6.3V X5R 0201

NOSTUFF C16C0 C16C1 C16C2 C16C3 C16C4 C16C5 C16C6 C16C7
1UF 20% 6.3V X5R 0201

PLACEMENT_NOTE (C1620-C1623):
Place near U1000 on bottom side

C1620 C1621 C1622 C1623
10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL

PLACEMENT_NOTE (C1624-C16D5):
Place near inductors on bottom side.

CRITICAL C1624 C1625 C1626 C1627 C1628 C1629 C1630 C1631 C1632 C1633 C1634 C1635 C1636 C1637 C1638 C1639
22UF 20% 6.3V X5R CERM 0603

NOSTUFF C16D0 C16D1 C16D2 C16D3
22UF 20% 6.3V X5R CERM 0603

PLACEMENT_NOTE (C1640-C1645):
Place near inductors on bottom side.

CRITICAL C1640 C1641 C1642 NOSTUFF C1643 CRITICAL C1644
470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402
Apple Implementation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402

PLACEMENT_NOTE (C1646-C1671):
Place on bottom side of U1000

13 73 70 68 45 39 35 22 105 104 102 PP1V05_S0

C1646 C1647 C1648 C1649 C1650 C1651 C1652 C1653 C1654 C1655 C1656 C1657 C1658
C1659 C1660 C1661 C1662 C1663 C1664 C1665 C1666 C1667 C1668 C1669 C1670 C1671
1UF 20% 10V X5R 402

PLACEMENT_NOTE (C1672-C1681):
Place near U1000 on bottom side

C1672 C1673 C1674 C1675 C1676 C1677 C1678 C1679 C1680 C1681
10UF 20% 6.3V X5R 603
CRITICAL

Place near inductors on bottom side

C1682 C1683
330UF-0.006OHM 20% 2V POLY CASE-D2-SM
CRITICAL

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1601
0.010
1% 1/4W MF 0603
PP1V05_S0_CPU_VCCPQE 7 10 12

C1684
1UF 10% 10V X5R 402

CPU VCCPLL DECOUPLING

102 88 72 71 25 20 7 6 PP1V8_S0

R1600
0
5% 1/16W MF-LF 402
PP1V8_S0_CPU_VCCPLL_R 7 12

C1685
1UF 10% 10V X5R 402
PLACE_NEAR=U1000.AK63:2.54 mm:NO_VIA

C1686
1UF 10% 10V X5R 402
PLACE_NEAR=U1000.AK65:2.54 mm:NO_VIA

CRITICAL C1687
330UF-0.006OHM 20% 2V POLY CASE-D2-SM
PLACE_NEAR=U1000.AK61:5 mm

CPU VCCPLL Low pass filter

SYNC_MASTER=K91_MLB SYNC_DATE=07/21/2010

PAGE TITLE
CPU DECOUPLING-I

Apple Inc.

DRAWING NUMBER
SIZE D
REVISION
BRANCH
PAGE 16 OF 132
SHEET 14 OF 105

VAXG DECOUPLING

Intel recommendation: 2x 470uF 4mOhm, 2x 470uF 4mOhm (NOSTUFF), 6x 22uF 0805, 2x 22uF 0805 (NOSTUFF), 6x 10uF 0603, 2x 10uF 0603 (NOSTUFF), 9x 1uF 0402, 9x 1uF 0402 (NOSTUFF)
Apple Implementation: 2x 470uF 4mOhm, 1x 470uF 4mOhm (NOSTUFF), 6x 22uF 0603, 2x 22uF 0603 (NOSTUFF), 6x 10uF 0402, 2x 10uF 0402 (NOSTUFF), 9x 1uF 0402, 9x 1uF 0402 (NOSTUFF)

69 49 13 12 7 PPVCORE_S0_AXG

PLACEMENT_NOTE (C1700-C1708):
Place on bottom side of U1000

C1700 1UF 10% 10V X5R 402
C1701 1UF 10% 10V X5R 402
C1702 1UF 10% 10V X5R 402
C1703 1UF 10% 10V X5R 402
C1704 1UF 10% 10V X5R 402
C1705 1UF 10% 10V X5R 402
C1706 1UF 10% 10V X5R 402
C1707 1UF 10% 10V X5R 402
C1708 1UF 10% 10V X5R 402
NOSTUFF C1709 1UF 10% 10V X5R 402
NOSTUFF C1710 1UF 10% 10V X5R 402
NOSTUFF C1711 1UF 10% 10V X5R 402
NOSTUFF C1712 1UF 10% 10V X5R 402
NOSTUFF C1713 1UF 10% 10V X5R 402
NOSTUFF C1714 1UF 10% 10V X5R 402
NOSTUFF C1715 1UF 10% 10V X5R 402
NOSTUFF C1716 1UF 10% 10V X5R 402
NOSTUFF C1717 1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1718-C1723):
Place close to U1000 on bottom side

C1718 10UF 20% 6.3V CERM-X5R 0402-1
C1719 10UF 20% 6.3V CERM-X5R 0402-1
C1720 10UF 20% 6.3V CERM-X5R 0402-1
C1721 10UF 20% 6.3V CERM-X5R 0402-1
C1722 10UF 20% 6.3V CERM-X5R 0402-1
C1723 10UF 20% 6.3V CERM-X5R 0402-1
NOSTUFF C1724 10UF 20% 6.3V CERM-X5R 0402-1
NOSTUFF C1725 10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1726-C1731):
Place near inductors on bottom side.

C1726 22UF 20% 6.3V X5R-CERM1 0603
C1727 22UF 20% 6.3V X5R-CERM1 0603
C1728 22UF 20% 6.3V X5R-CERM1 0603
C1729 22UF 20% 6.3V X5R-CERM1 0603
C1730 22UF 20% 6.3V X5R-CERM1 0603
C1731 22UF 20% 6.3V X5R-CERM1 0603
NOSTUFF C1732 22UF 20% 6.3V X5R-CERM1 0603
NOSTUFF C1733 22UF 20% 6.3V X5R-CERM1 0603

PLACEMENT_NOTE (C1734-C1735):
Place near inductors on bottom side.

C1734 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM
C1735 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM
NOSTUFF C1737 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402

104 73 29 13 10 7 PP1V5_S3RS0_CPUDDR

PLACEMENT_NOTE (C1738-C1747):
Place on bottom side of U1000

C1738 1UF 10% 10V X5R 402
C1739 1UF 10% 10V X5R 402
C1740 1UF 10% 10V X5R 402
C1741 1UF 10% 10V X5R 402
C1742 1UF 10% 10V X5R 402
C1743 1UF 10% 10V X5R 402
C1744 1UF 10% 10V X5R 402
C1745 1UF 10% 10V X5R 402
C1746 1UF 10% 10V X5R 402
C1747 1UF 10% 10V X5R 402

Place close to U1000 on bottom side

C1748 10UF 20% 6.3V X5R 603
C1749 10UF 20% 6.3V X5R 603
C1750 10UF 20% 6.3V X5R 603
C1751 10UF 20% 6.3V X5R 603
C1752 10UF 20% 6.3V X5R 603
C1753 10UF 20% 6.3V X5R 603
C1754 10UF 20% 6.3V X5R 603
C1755 10UF 20% 6.3V X5R 603

Place near inductors on bottom side

CRITICAL
C1756 330UF-0.0060HM 20% 2V POLY CASE-D2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1700 0.010 1% 1/4W MF 0603
PP1V5_S3_CPU_VCCDQ 7 12
C1757 1UF 10% 10V X5R 402

CPU VCCSA DECOUPLING

Intel recommendation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402
Apple Implementation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402

65 12 7 PPVCCSA_S0_CPU

PLACEMENT_NOTE (C1758-C1762):
Place on bottom side of U1000

C1758 1UF 10% 10V X5R 402
C1759 1UF 10% 10V X5R 402
C1760 1UF 10% 10V X5R 402
C1761 1UF 10% 10V X5R 402
C1762 1UF 10% 10V X5R 402

C1763 10UF 20% 6.3V X5R 603
C1764 10UF 20% 6.3V X5R 603
C1765 10UF 20% 6.3V X5R 603
C1766 10UF 20% 6.3V X5R 603
C1767 10UF 20% 6.3V X5R 603

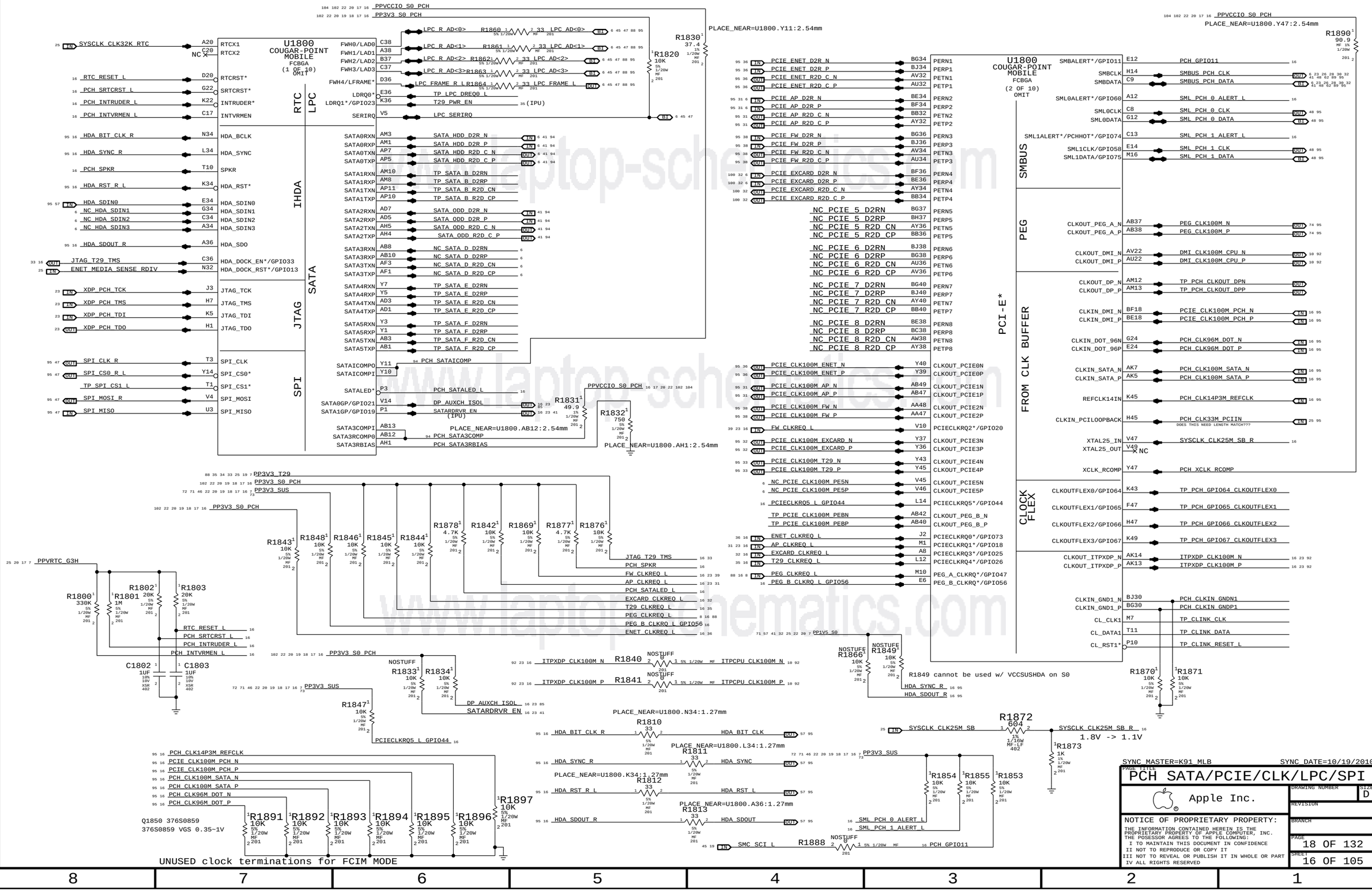
C1768 270UF 20% 2V TANT CASE-B4-SM

SYNC_MASTER=K91_MLB SYNC_DATE=07/21/2010

PAGE TITLE: CPU DECOUPLING-II

Apple Inc.

DRAWING NUMBER | SIZE: D
REVISION
BRANCH
PAGE: 17 OF 132
SHEET: 15 OF 105



PP3V3_SUS
PPVCCIO_S0_PCH
R1905 10K 5% 1/20W MF 201
R1900 49.9 1% 1/20W MF 201 PLACE_NEAR=U1800.BJ24:12.7mm

U1800 COUGAR-POINT MOBILE FCBGA (3 OF 10) OMIT

DMI
DMI_N2S_N<0> BC24 DMI0RXN
DMI_N2S_N<1> BE20 DMI1RXN
DMI_N2S_N<2> BG18 DMI2RXN
DMI_N2S_N<3> BG20 DMI3RXN
DMI_N2S_P<0> BE24 DMI0RXP
DMI_N2S_P<1> BC20 DMI1RXP
DMI_N2S_P<2> BJ18 DMI2RXP
DMI_N2S_P<3> BJ20 DMI3RXP
DMI_S2N_N<0> AW24 DMI0TXN
DMI_S2N_N<1> AW20 DMI1TXN
DMI_S2N_N<2> BB18 DMI2TXN
DMI_S2N_N<3> AV18 DMI3TXN
DMI_S2N_P<0> AY24 DMI0TXP
DMI_S2N_P<1> AY20 DMI1TXP
DMI_S2N_P<2> AY18 DMI2TXP
DMI_S2N_P<3> AU18 DMI3TXP
PCH_DMI2RBIAS BH21 DMI2RBIAS PLACE_NEAR=U1800.BH21:2.54mm
PCH_DMI_COMP BJ24 DMI_ZCOMP
BG25 DMI_IRCOMP
R1920 750 1% 1/20W MF 201

FDI
FDI_DATA_N<0> BJ14 FDI_RXN0
FDI_DATA_N<1> AY14 FDI_RXN1
FDI_DATA_N<2> BE14 FDI_RXN2
FDI_DATA_N<3> BH13 FDI_RXN3
FDI_DATA_N<4> BC12 FDI_RXN4
FDI_DATA_N<5> BJ12 FDI_RXN5
FDI_DATA_N<6> BG10 FDI_RXN6
FDI_DATA_N<7> BG9 FDI_RXN7
FDI_DATA_P<0> BG14 FDI_RXP0
FDI_DATA_P<1> BB14 FDI_RXP1
FDI_DATA_P<2> BF14 FDI_RXP2
FDI_DATA_P<3> BG13 FDI_RXP3
FDI_DATA_P<4> BE12 FDI_RXP4
FDI_DATA_P<5> BG12 FDI_RXP5
FDI_DATA_P<6> BJ10 FDI_RXP6
FDI_DATA_P<7> BH9 FDI_RXP7
FDI_INT AW16 FDI_INT
FDI_FSYNC<0> AV12 FDI_FSYNC0
FDI_FSYNC<1> BC10 FDI_FSYNC1
FDI_LSYNC<0> AV14 FDI_LSYNC0
FDI_LSYNC<1> BB10 FDI_LSYNC1

SYSTEM POWER MANAGEMENT
PM_SYSRST_L K3 SYS_RESET*
PM_PCH_SYS_PWROK P12 SYS_PWROK
PM_PCH_PWROK L22 PWROK
PM_MEM_PWRGD B13 DRAMPWROK
PM_DSW_PWRGD E22 DPWROK
PM_PCH_PWROK L10 APWROK
PM_RSMRST_L C21 RSMRST*
SUSWARN_L K16 SUSWARN*/SUSPWRDNACK/GPIO30
PM_PWRBTN_L E20 PWRBTN*
PD on SMC page SMC_ADAPTER_EN H20 ACPRESENT/GPIO31
PM_BATLOW_L E10 BATLOW*/GPIO72
PCH_RI_L A10 RI*
R1909 100K 5% 1/20W MF 201
WAKE* B9 PCIE_WAKE_L
CLKRUN*/GPIO32 N3 PM_CLKRUN_L
SUS_STAT*/GPIO61 G8 LPC_PWRDWN_L
SUSCLK/GPIO62 N14 PM_CLK32K_SUSCLK_R
SLP_S5*/GPIO63 D10 PM_SLP_S5_L
SLP_S4* H4 PM_SLP_S4_L
SLP_S3* F4 PM_SLP_S3_L
SLP_A* G10 TP_PM_SLP_A_L
TP23 AY16 TP_PCH_TP23
PMSYNCH AP14 PM_SYNC
SLP_LAN*/GPIO29 K14 GPIO29_SLP_LAN_L
DF_TVS AY1 PCH_DF_TVS
DSWVRMEN A18 PCH_DSWVRMEN
SLP_SUS* G16 PM_SLP_SUS_L
SUSACK* C12 PCH_SUSACK_L

PPVRTC_G3H
R1981 2.2K 5% 1/20W MF 201
PP1V8_S0_PCH
R1915 390K 5% 1/20W MF 201
R1980 1K 5% 1/20W MF 201
CPU_PROC_SEL_L

DF_TVS:DMI & FDI Term Voltage
Set to Vss when low
Set to Vcc when high

R1986 0 5% 1/20W MF
SUSWARN_L
PCH_SUSACK_L

PLACE_NEAR=U1800.T43:2.54mm

U1800 COUGAR-POINT MOBILE FCBGA (4 OF 10) OMIT

DIGITAL DISPLAY INTERFACE

CRT
NC_CRT_IG_BLUE N48 CRT_BLUE
NC_CRT_IG_GREEN P49 CRT_GREEN
NC_CRT_IG_RED T49 CRT_RED
NC_CRT_IG_DDC_CLK T39 CRT_DDC_CLK
NC_CRT_IG_DDC_DATA M40 CRT_DDC_DATA
NC_CRT_IG_HSYNC M47 CRT_HSYNC
NC_CRT_IG_VSYNC M49 CRT_VSYNC
PCH_DAC_IREF T43 DAC_IREF
T42 CRT_IRTN
R1951 1K 5% 1/20W MF 201

SDVO_TVCLKINN AP43 NC_SDVO_TVCLKINN
SDVO_TVCLKINP AP45 NC_SDVO_TVCLKINP
SDVO_STALLN AM42 NC_SDVO_STALLN
SDVO_STALLP AM40 NC_SDVO_STALLP
SDVO_INTN AP39 NC_SDVO_INTN
SDVO_INTP AP40 NC_SDVO_INTP
SDVO_CTRLCLK P38 DP_IG_DDC_CLK
SDVO_CTRLDATA M39 DP_IG_DDC_DATA
DDPB_AUXN AT49 DP_IG_AUX_CH_N
DDPB_AUXP AT47 DP_IG_AUX_CH_P
DDPB_HPD AT40 DP_IG_HPD
DDPB_0N AV42 TP_DP_IG_B_MLN<0>
DDPB_0P AV40 TP_DP_IG_B_MLP<0>
DDPB_1N AV45 TP_DP_IG_B_MLN<1>
DDPB_1P AV46 TP_DP_IG_B_MLP<1>
DDPB_2N AU48 TP_DP_IG_B_MLN<2>
DDPB_2P AU47 TP_DP_IG_B_MLP<2>
DDPB_3N AV47 TP_DP_IG_B_MLN<3>
DDPB_3P AV49 TP_DP_IG_B_MLP<3>
DDPC_CTRLCLK P46 NC_DP_IG_C_CTRL_CLK
DDPC_CTRLDATA P42 NC_DP_IG_C_CTRL_DATA
DDPC_AUXN AP47 NC_DP_IG_C_AUXN
DDPC_AUXP AP49 NC_DP_IG_C_AUXP
DDPC_HPD AT38 NC_DP_IG_C_HPD
DDPC_0N AY47 NC_DP_IG_C_MLN<0>
DDPC_0P AY49 NC_DP_IG_C_MLP<0>
DDPC_1N AY43 NC_DP_IG_C_MLN<1>
DDPC_1P AY45 NC_DP_IG_C_MLP<1>
DDPC_2N BA47 NC_DP_IG_C_MLN<2>
DDPC_2P BA48 NC_DP_IG_C_MLP<2>
DDPC_3N BB47 NC_DP_IG_C_MLN<3>
DDPC_3P BB49 NC_DP_IG_C_MLP<3>
DDPD_CTRLCLK M43 NC_DP_IG_D_CTRL_CLK
DDPD_CTRLDATA M36 NC_DP_IG_D_CTRL_DATA
DDPD_AUXN AT45 NC_DP_IG_D_AUXN
DDPD_AUXP AT43 NC_DP_IG_D_AUXP
DDPD_HPD BH41 NC_DP_IG_D_HPD
DDPD_0N BB43 NC_DP_IG_D_MLN<0>
DDPD_0P BB45 NC_DP_IG_D_MLP<0>
DDPD_1N BF44 NC_DP_IG_D_MLN<1>
DDPD_1P BE44 NC_DP_IG_D_MLP<1>
DDPD_2N BF42 NC_DP_IG_D_MLN<2>
DDPD_2P BE42 NC_DP_IG_D_MLP<2>
DDPD_3N BJ42 NC_DP_IG_D_MLN<3>
DDPD_3P BG42 NC_DP_IG_D_MLP<3>

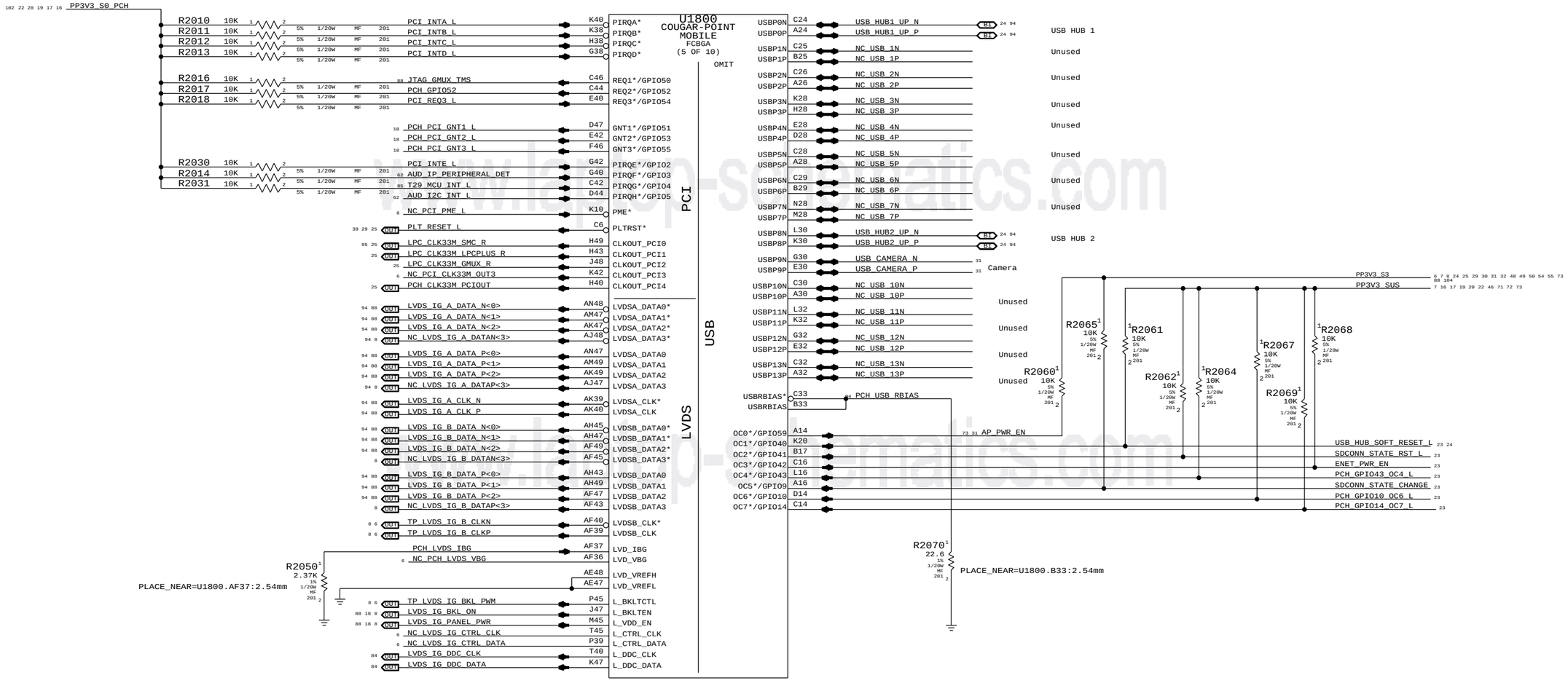
T29 WAKE
PCIE_WAKE_L IN — PCIE_WAKE_L OUT
MAKE_BASE=TRUE

PP3V3_SUS
PP3V3_S5
PP3V3_SUS
R1925 1K 1% 1/20W MF 201
R1985 1K 1% 1/20W MF 201
R1982 10K 5% 1/20W MF 201
R1983 10K 5% 1/20W MF 201
SUSWARN_L
GPIO29_SLP_LAN_L
PM_PWRBTN_L
PCIE_WAKE_L

PP3V3_S0_PCH
R1991 8.2K 5% 1/20W MF 201
PM_CLKRUN_L

PM_SLP_S3_L
PM_SLP_SUS_L
PM_SLP_S5_L
PM_SLP_S4_L
R1921 100K 5% 1/20W MF 201
R1922 100K 5% 1/20W MF 201
R1923 100K 5% 1/20W MF 201
R1924 100K 5% 1/20W MF 201

PAGE TITLE
PCH DMI/FDI/GRAPHICS
Apple Inc.
DRAWING NUMBER
SIZE D
REVISION
BRANCH
PAGE 19 OF 132
SHEET 17 OF 105

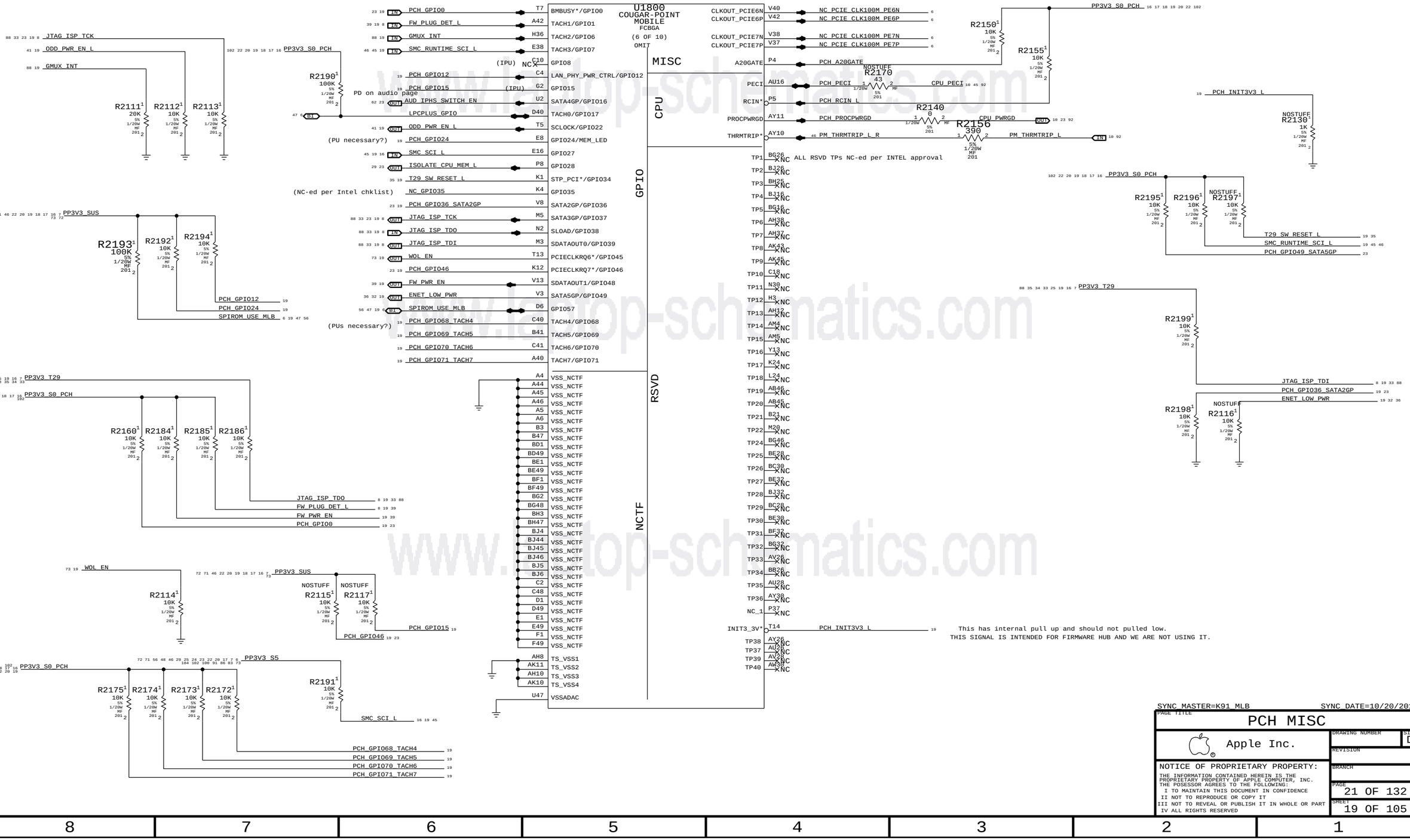


SYNC_MASTER=K91_MLB SYNC_DATE=10/20/2010

PAGE TITLE
PCH PCI/FLASHCACHE/USB

Apple Inc.

DRAWING NUMBER
SIZE D
REVISION
BRANCH
PAGE 20 OF 132
SHEET 18 OF 105



SYNC_MASTER=K91_MLB SYNC_DATE=10/20/2010

PAGE TITLE: PCH MISC

Apple Inc.

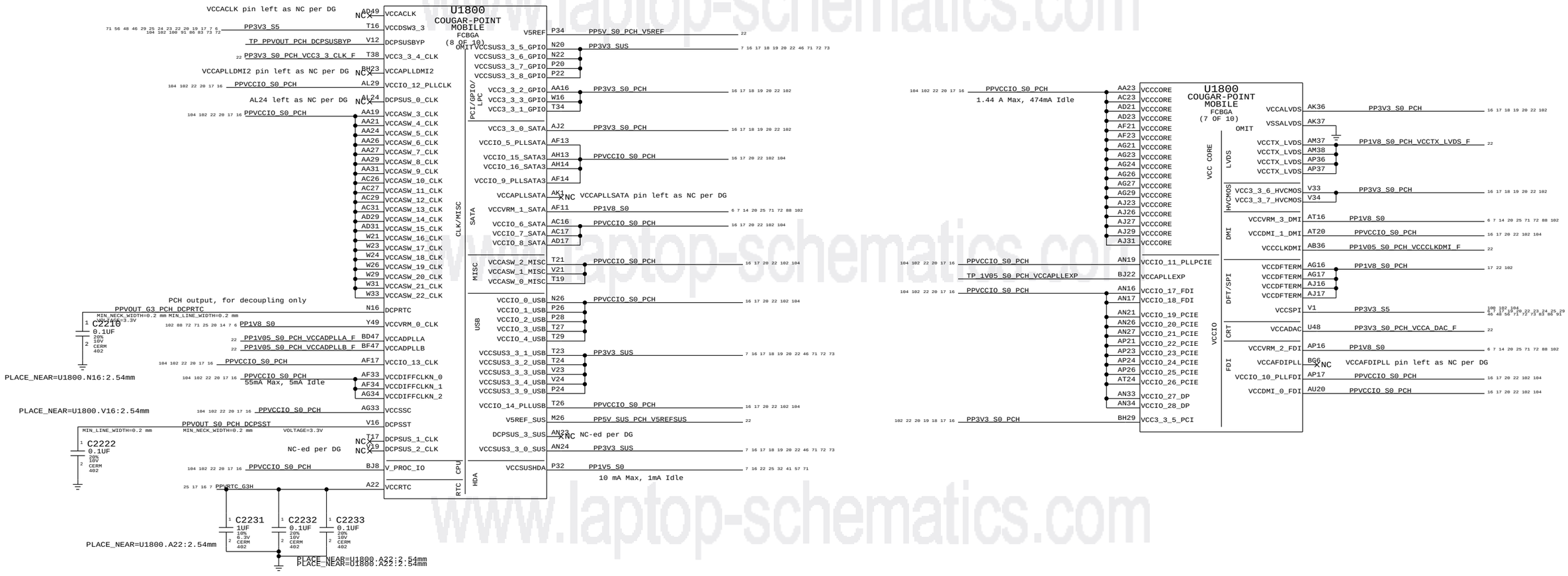
DRAWING NUMBER | SIZE: D

REVISION

BRANCH

PAGE: 21 OF 132

SHEET: 19 OF 105



PAGE TITLE: PCH POWER

Apple Inc.

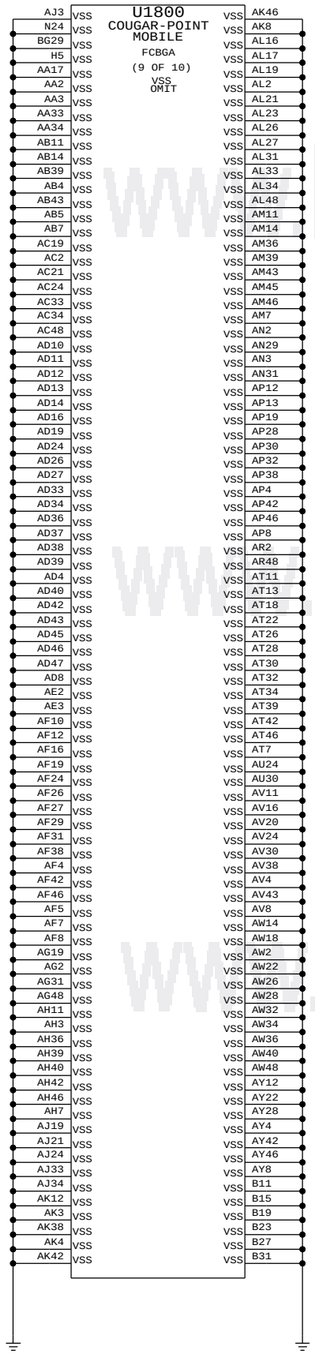
DRAWING NUMBER | SIZE: D

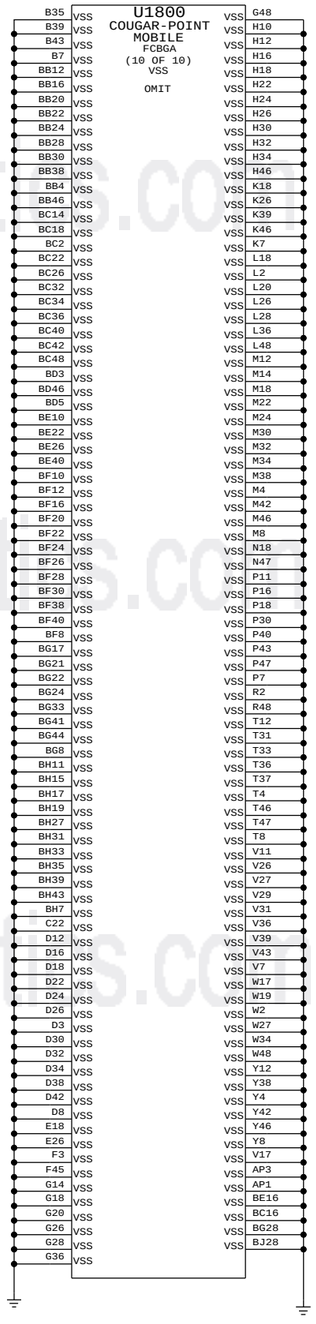
REVISION

BRANCH

PAGE: 22 OF 132

SHEET: 20 OF 105





SYNC_MASTER=K92_YUN SYNC_DATE=05/20/2010

PAGE TITLE
PCH GROUNDS

Apple Inc.

DRAWING NUMBER | SIZE D
REVISION
BRANCH
PAGE 23 OF 132
SHEET 21 OF 105

CRITICAL
L2406
10UH-0.45A
1210-HF
PPVCCIO_S0_PCH
PP1V05_S0_PCH_VCCCLKDMI_R
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.05V
R2415
PP1V05_S0_PCH_VCCCLKDMI_F
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
C2411
PLACE_NEAR=U1800.AB36:2.54mm

PCH VCCSUS3_3 BYPASS
(PCH SUSPEND USB 3.3V PWR)
PP3V3_SUS
C2484
C2413
PLACE_NEAR=U1800.P24:2.54mm
PLACE_NEAR=U1800.V24:2.54mm

PP1V8_S0_PCH
C2440
PLACE_NEAR=U1800.AJ16:2.54mm

PCH VCCIO BYPASS
(PCH USB 1.05V PWR)
PPVCCIO_S0_PCH
C2444
C2452
PLACE_NEAR=U1800.AH13:2.54mm
PLACE_NEAR=U1800.AC17:2.54mm
PPVCCIO_S0_PCH
C2446
PLACE_NEAR=U1800.P28:2.54mm

CRITICAL
L2407
0.1UH
0805
PP1V8_S0_PCH
PP1V8_S0_PCH_VCCTX_LVDS_F
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.8V
CRITICAL
C2400
22UF
C2406
0.01UF
C2408
0.01UF
PLACE_NEAR=U1800.AM37:2.54mm
PLACE_NEAR=U1800.AM37:2.54mm
PLACE_NEAR=U1800.AM37:2.54mm

PCH VCCSUSHDA BYPASS
PP1V5_S0
C2441
PLACE_NEAR=U1800.P32:2.54mm
PPVCCIO_S0_PCH
C2416
4.7UF
C2417
0.1UF
C2430
0.1UF
PLACE_NEAR=U1800.BJ8:2.54mm
PLACE_NEAR=U1800.BJ8:2.54mm
PLACE_NEAR=U1800.BJ8:2.54mm
PP3V3_S5
C2442
PLACE_NEAR=U1800.V1:2.54mm

PPVCCIO_S0_PCH
C2475
PLACE_NEAR=U1800.AG33:2.54mm
PP3V3_SUS
C2476
PLACE_NEAR=U1800.P22:2.54mm

R2450
0
PP3V3_S0_PCH
PP3V3_S0_PCH_VCCA_DAC_F
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
CRITICAL
C2450
10UF
C2451
0.1UF
C2455
0.01UF
PLACE_NEAR=U1800.U48:2.54mm
PLACE_NEAR=U1800.U48:2.54mm
PLACE_NEAR=U1800.U48:2.54mm

PCH VCCIO BYPASS
PPVCCIO_S0_PCH
C2419
PCH VCC3_3 BYPASS
(PCH PCI 3.3V PWR)
PLACE_NEAR=U1800.AT20:2.54mm
PP3V3_S5
C2499
PLACE_NEAR=U1800.T16:2.54mm

PPVCCIO_S0_PCH
C2434
PLACE_NEAR=U1800.AF34:2.54mm
PPVCCIO_S0_PCH
C2469
PLACE_NEAR=U1800.AF17:2.54mm

PCH VCCCORE BYPASS
(PCH 1.05V CORE PWR)
PPVCCIO_S0_PCH
C2481
C2482
C2483
CRITICAL
C2460
10UF
PLACE_NEAR=U1800.AD21:2.54mm
PLACE_NEAR=U1800.AG24:2.54mm
PLACE_NEAR=U1800.AG25:2.54mm
PLACE_NEAR=U1800.AG26:2.54mm

PP3V3_S0_PCH
PP5V_S0
1 mA
R2405
100
NCX
D2400
BAT54DW-X-G
SOT-363
PCH V5REF Filter & Follower
(PCH Reference for 5V Tolerance on PCI)
NEED PWR CONSTRAINT
PP5V_S0_PCH_V5REF
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=5V
MAKE_BASE=TRUE
<1 MA
PP5V_S0_PCH_V5REF
C2439
1UF
PLACE_NEAR=U1800.P34:2.54mm

CRITICAL
L2451
10UH-0.12A-0.36OHM
0603
PP3V3_S0_PCH
R2451
PP3V3_S0_PCH_VCC3_3_CLK_R
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=3.3V
PP3V3_S0_PCH_VCC3_3_CLK_F
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=3.3V
C2453
10UF
C2454
1UF
CRITICAL
PLACE_NEAR=U1800.T38:2.54mm
PLACE_NEAR=U1800.T38:2.54mm

PPVCCIO_S0_PCH
C2426
C2456
C2496
C2428
22UF
C2420
22UF
PLACE_NEAR=U1800.AC27:2.54mm
PLACE_NEAR=U1800.AC27:2.54mm
PLACE_NEAR=U1800.AC27:2.54mm
PLACE_NEAR=U1800.AC27:2.54mm
PLACE_NEAR=U1800.AC27:2.54mm

PP3V3_SUS
PP5V_SUS
1 mA S0-S5
R2404
10
D2400
BAT54DW-X-G
SOT-363
PCH V5REF_SUS Filter & Follower
(PCH Reference for 5V Tolerance on USB)
NEED PWR CONSTRAINT
PP5V_SUS_PCH_V5REFSUS
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=5V
MAKE_BASE=TRUE
<1 MA S0-S5
PP5V_SUS_PCH_V5REFSUS
C2438
0.1UF
PLACE_NEAR=U1800.M26:2.54mm

CRITICAL
L2490
10UH-0.12A-0.36OHM
0603
PPVCCIO_S0_PCH
R2490
0
PP1V05_S0_PCH_VCCADPLLA_R
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.05V
PP1V05_S0_PCH_VCCADPLLA_F
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
68 mA
NO STUFF
C2491
220UF
C2492
1UF
PLACE_NEAR=U1800.BD47:2.54MM
PLACE_NEAR=U1800.BD47:2.54MM
CRITICAL
PCH VCCADPLLA Filter
(PCH DPLLA PWR)

CRITICAL
L2491
10UH-0.12A-0.36OHM
0603
R2491
0
PP1V05_S0_PCH_VCCADPLLB_R
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.05V
PP1V05_S0_PCH_VCCADPLLB_F
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
69 mA
NO STUFF
C2493
220UF
C2494
1UF
PLACE_NEAR=U1800.BF47:2.54MM
PLACE_NEAR=U1800.BF47:2.54MM
CRITICAL
PCH VCCADPLLB Filter
(PCH DPLLB PWR)

PPVCCIO_S0_PCH
C2429
C2414
C2407
C2463
C2401
10UF
PLACE_NEAR=U1800.AN27:2.54mm
PLACE_NEAR=U1800.AN27:2.54mm
PLACE_NEAR=U1800.AN27:2.54mm
PLACE_NEAR=U1800.AN27:2.54mm
PLACE_NEAR=U1800.AN27:2.54mm

PP3V3_S0_PCH
C2421
0.1UF
PLACE_NEAR=U1800.BH29:2.54mm
PP3V3_S0_PCH
C2423
0.1UF
PLACE_NEAR=U1800.AJ2:2.54mm

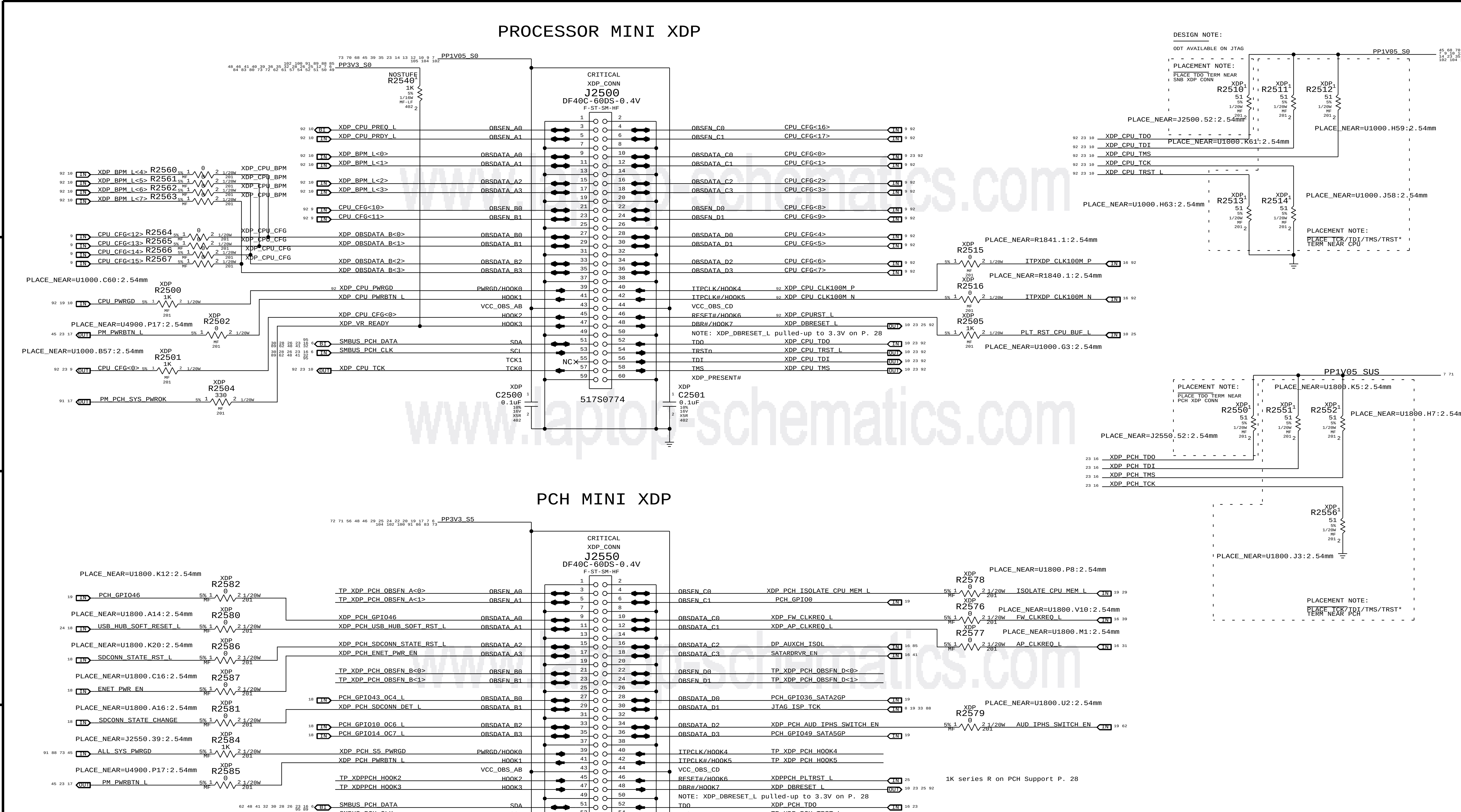
PP3V3_S0_PCH
C2424
0.1UF
PLACE_NEAR=U1800.V33:2.54mm
PP3V3_S0_PCH
C2486
0.1UF
C2485
0.1UF
PLACE_NEAR=U1800.T34:2.54mm
PLACE_NEAR=U1800.AA16:2.54mm

SYNC_MASTER=K91_YUN
SYNC_DATE=08/06/2010

PAGE TITLE
PCH DECOUPLING

Apple Inc.

DRAWING NUMBER
SIZE D
REVISION
BRANCH
PAGE 24 OF 132
SHEET 22 OF 105



SYNC_MASTER=K91_MLB

SYNC_DATE=10/17/2010

PAGE TITLE

CPU & PCH XDP

Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH

NOTICE OF PROPRIETARY PROPERTY:

BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0,HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0,HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1,HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1,HUB1_NONREM0_1
HUB2_ALLREM	HUB2_NONREM1_0,HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0,HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1,HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1,HUB2_NONREM0_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	SMSC USB2514	U2600,U2650	CRITICAL	USBHUB_2514
338S0824	2	SMSC USB2514B	U2600,U2650	CRITICAL	USBHUB_2514B
338S0721	2	SMSC USX2061	U2600,U2650	CRITICAL	USBHUB_2061

T29 unused USB port, only has pull up

IR Receiver

External B

External C

Bluetooth

Trackpad/Keyboard

External A

SD Card/Express Card

SYNC MASTER=K92_BEN SYNC DATE=06/29/2010

PAGE TITLE: USB HUBS

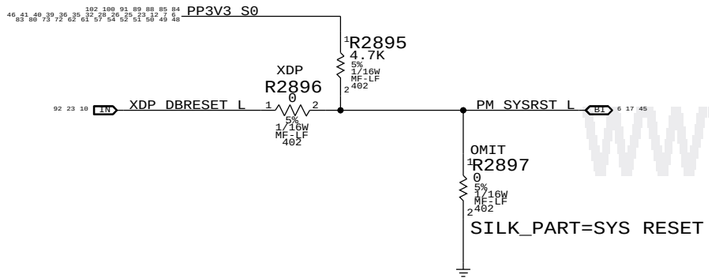
Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:

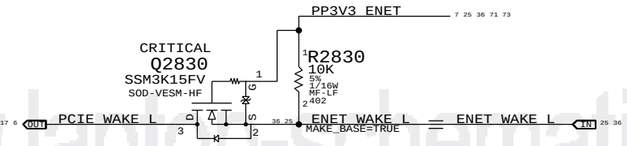
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

DRAWING NUMBER: | SIZE: D
REVISION:
BRANCH:
PAGE: 26 OF 132
SHEET: 24 OF 105

PCH Reset Button

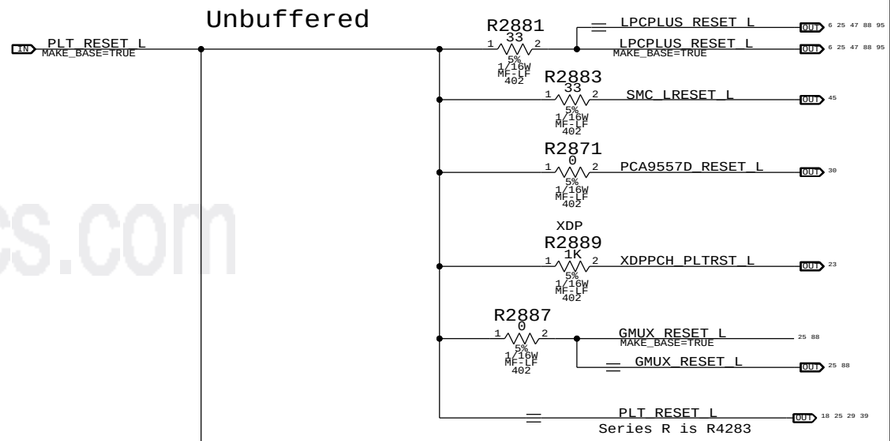


Ethernet WAKE# Isolation

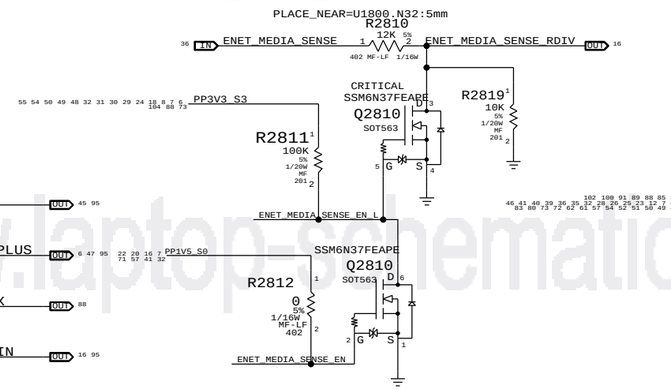


Platform Reset Connections

Unbuffered

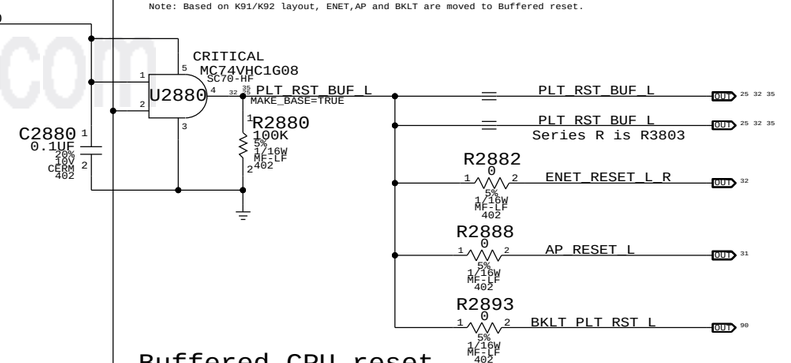


ENET_MEDIA_SENSE ISOLATION CIRCUIT

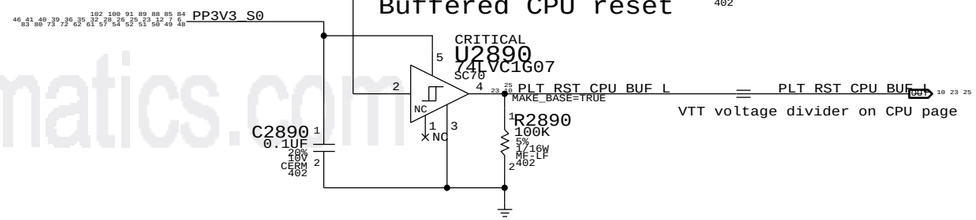


Buffered

Note: Based on K91/K92 layout, ENET,AP and BKLT are moved to Buffered reset.



Buffered CPU reset



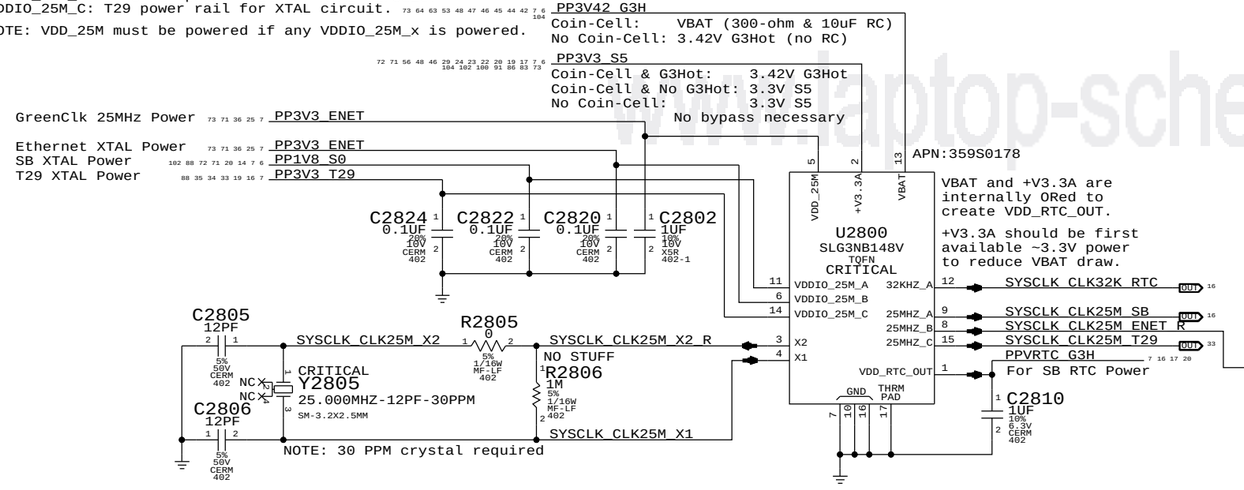
System RTC Power Source & 32kHz / 25MHz Clock Generator

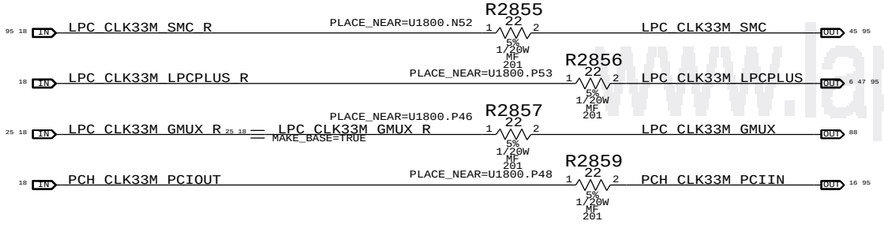
VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: T29 power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.

PP3V42_G3H
Coin-Cell: VBAT (300-ohm & 10uF RC)
No Coin-Cell: 3.42V G3Hot (no RC)

PP3V3_S5
Coin-Cell & G3Hot: 3.42V G3Hot
Coin-Cell & No G3Hot: 3.3V S5
No Coin-Cell: 3.3V S5
No bypass necessary





SYNC_MASTER=K91_MLB	SYNC_DATE=06/29/2010
PAGE TITLE	Chipset Support
Apple Inc.	DRAWING NUMBER / SIZE D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	REVISION / BRANCH / PAGE 28 OF 132 / SHEET 25 OF 105

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

PP1V5_S3

C2900 10UF 20% 6.3V X6S 603 — PLACE_NEAR=J2900.75:2.54mm
C2901 10UF 20% 6.3V X6S 603 — PLACE_NEAR=J2900.75:2.54mm

C2910 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2911 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2912 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2913 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2914 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2915 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2916 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2917 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2918 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2919 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2920 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2921 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2922 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2923 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm

PP0V75_S3_MEM_VREFDQ_A

C2930 2.2UF 20% 6.3V CERM 402-LF
C2931 0.1UF 20% 10V CERM 402

J2900 — DDR3-SODIMM-DUAL-K6 (SYMBOL 2 OF 2) — F-RT-THB

KEY

	CKE0	CKE1	
	VDD	VDD	
NC	NC	A15	MEM_A_A<15>
MEM_A_BA<2>	BA2	A14	MEM_A_A<14>
	VDD	VDD	
MEM_A_A<12>	A12/BC*	A11	MEM_A_A<11>
MEM_A_A<9>	A9	A7	MEM_A_A<7>
	VDD	VDD	
MEM_A_A<8>	A8	A6	MEM_A_A<6>
MEM_A_A<5>	A5	A4	MEM_A_A<4>
	VDD	VDD	
MEM_A_A<3>	A3	A2	MEM_A_A<2>
MEM_A_A<1>	A1	A0	MEM_A_A<0>
	VDD	VDD	
MEM_A_CLK_P<0>	CK0	CK1	MEM_A_CLK_P<1>
MEM_A_CLK_N<0>	CK0*	CK1*	MEM_A_CLK_N<1>
	VDD	VDD	
MEM_A_A<10>	A10/AP	BA1	MEM_A_BA<1>
MEM_A_BA<0>	BA0	RAS*	MEM_A_RAS_L
	VDD	VDD	
MEM_A_WE_L	WE*	S0*	MEM_A_CS_L<0>
MEM_A_CAS_L	CAS*	ODT0	MEM_A_ODT<0>
	VDD	VDD	
MEM_A_A<13>	A13	ODT1	MEM_A_ODT<1>
MEM_A_CS_L<1>	S1*	NC	NC
	VDD	VDD	
	TEST	VREFCA	
	VSS	VSS	
=MEM_A_DQ<32>	DQ32	DQ36	=MEM_A_DQ<36>
=MEM_A_DQ<33>	DQ33	DQ37	MEM_A_DQ<37>
	VSS	VSS	
=MEM_A_DQS_N<4>	DQS4*	DM4	
=MEM_A_DQS_P<4>	DQS4	VSS	
	VSS	DQ38	=MEM_A_DQ<38>
=MEM_A_DQ<34>	DQ34	DQ39	=MEM_A_DQ<39>
=MEM_A_DQ<35>	DQ35	VSS	
	VSS	DQ44	=MEM_A_DQ<44>
=MEM_A_DQ<40>	DQ40	DQ45	=MEM_A_DQ<45>
=MEM_A_DQ<41>	DQ41	VSS	
	VSS	DQS5*	=MEM_A_DQS_N<5>
	DM5	DQS5	=MEM_A_DQS_P<5>
	VSS	VSS	
=MEM_A_DQ<42>	DQ42	DQ46	=MEM_A_DQ<46>
=MEM_A_DQ<43>	DQ43	DQ47	=MEM_A_DQ<47>
	VSS	VSS	
=MEM_A_DQ<48>	DQ48	DQ52	=MEM_A_DQ<52>
=MEM_A_DQ<49>	DQ49	DQ53	=MEM_A_DQ<53>
	VSS	VSS	
=MEM_A_DQS_N<6>	DQS6*	DM6	
=MEM_A_DQS_P<6>	DQS6	VSS	
	VSS	DQ54	=MEM_A_DQ<54>
=MEM_A_DQ<50>	DQ50	DQ55	=MEM_A_DQ<55>
=MEM_A_DQ<51>	DQ51	VSS	
	VSS	DQ60	=MEM_A_DQ<60>
=MEM_A_DQ<56>	DQ56	DQ61	=MEM_A_DQ<61>
=MEM_A_DQ<57>	DQ57	VSS	
	VSS	DQS7*	=MEM_A_DQS_N<7>
	DM7	DQS7	=MEM_A_DQS_P<7>
	VSS	VSS	
=MEM_A_DQ<58>	DQ58	DQ62	=MEM_A_DQ<62>
=MEM_A_DQ<59>	DQ59	DQ63	=MEM_A_DQ<63>
	VSS	VSS	
MEM_A_SA<0>	SA0	EVENT*	MEM_EVENT_L
	VDDSPD	SDA	SMBUS_PCH_DATA
MEM_A_SA<1>	SA1	SCL	SMBUS_PCH_CLK
	VTT	VTT	PP0V75_S0_DDRVTT

516-0229
SPD ADDR=0xA0(WR)/0xA1(RD)

PP3V3_S0

C2940 2.2UF 20% 6.3V CERM 402-LF
R2940 10K 5% 1/16W MF-LF 402
R2941 10K 5% 1/16W MF-LF 402

J2900 — DDR3-SODIMM-DUAL-K6 (SYMBOL 1 OF 2) — F-RT-THB — CRITICAL

KEY

	VREFDQ	VSS	
	VSS	DQ4	=MEM_A_DQ<4>
=MEM_A_DQ<0>	DQ0	DQ5	=MEM_A_DQ<5>
=MEM_A_DQ<1>	DQ1	VSS	
	VSS	DQS0*	MEM_A_DQS_N<0>
	DM0	DQS0	=MEM_A_DQS_P<0>
	VSS	VSS	
=MEM_A_DQ<2>	DQ2	DQ6	=MEM_A_DQ<6>
=MEM_A_DQ<3>	DQ3	DQ7	=MEM_A_DQ<7>
	VSS	VSS	
=MEM_A_DQ<8>	DQ8	DQ12	=MEM_A_DQ<12>
=MEM_A_DQ<9>	DQ9	DQ13	=MEM_A_DQ<13>
	VSS	VSS	
=MEM_A_DQS_N<1>	DQS1*	DM1	
=MEM_A_DQS_P<1>	DQS1	RESET*	MEM_RESET_L
	VSS	VSS	
=MEM_A_DQ<10>	DQ10	DQ14	=MEM_A_DQ<14>
=MEM_A_DQ<11>	DQ11	DQ15	=MEM_A_DQ<15>
	VSS	VSS	
=MEM_A_DQ<16>	DQ16	DQ20	=MEM_A_DQ<20>
=MEM_A_DQ<17>	DQ17	DQ21	=MEM_A_DQ<21>
	VSS	VSS	
=MEM_A_DQS_N<2>	DQS2*	DM2	
=MEM_A_DQS_P<2>	DQS2	VSS	
	VSS	DQ22	=MEM_A_DQ<22>
=MEM_A_DQ<18>	DQ18	DQ23	=MEM_A_DQ<23>
=MEM_A_DQ<19>	DQ19	VSS	
	VSS	DQ28	=MEM_A_DQ<28>
=MEM_A_DQ<24>	DQ24	DQ29	=MEM_A_DQ<29>
=MEM_A_DQ<25>	DQ25	VSS	
	VSS	DQS3*	=MEM_A_DQS_N<3>
	DM3	DQS3	=MEM_A_DQS_P<3>
	VSS	VSS	
=MEM_A_DQ<26>	DQ26	DQ30	=MEM_A_DQ<30>
=MEM_A_DQ<27>	DQ27	DQ31	=MEM_A_DQ<31>
	VSS	VSS	

516-0229

PP0V75_S3_MEM_VREFCA_A

C2935 2.2UF 20% 6.3V CERM 402-LF
C2936 0.1UF 20% 10V CERM 402

C2950 1UF 10% 10V X5R 402
C2951 1UF 10% 10V X5R 402
C2952 1UF 10% 10V X5R 402
C2953 1UF 10% 10V X5R 402

"Factory" (top) slot

SYNC_MASTER=K92_YUN SYNC_DATE=06/14/2010

PAGE TITLE: DDR3 SO-DIMM Connector A

Apple Inc.

DRAWING NUMBER — SIZE: D
REVISION
BRANCH
PAGE: 29 OF 132
SHEET: 26 OF 105

CPU CHANNEL A DQS 0 -> DIMM A DQS 0

93 27 26 11	MEM_A_DQS_N<0>	MAKE_BASE=TRUE	MEM_A_DQS_N<0>	11 26 27 93 93 28 27 11	MEM_B_DQS_N<0>
93 11	MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=MEM_A_DQS_P<0>	93 28 27 11	MEM_B_DQS_P<0>
93 11	MEM_A_DQ<7>	MAKE_BASE=TRUE	=MEM_A_DQ<7>	93 11	MEM_B_DQ<7>
93 11	MEM_A_DQ<6>	MAKE_BASE=TRUE	=MEM_A_DQ<6>	93 11	MEM_B_DQ<6>
93 11	MEM_A_DQ<5>	MAKE_BASE=TRUE	=MEM_A_DQ<5>	93 11	MEM_B_DQ<5>
93 11	MEM_A_DQ<4>	MAKE_BASE=TRUE	=MEM_A_DQ<4>	93 11	MEM_B_DQ<4>
93 11	MEM_A_DQ<3>	MAKE_BASE=TRUE	=MEM_A_DQ<3>	93 11	MEM_B_DQ<3>
93 11	MEM_A_DQ<2>	MAKE_BASE=TRUE	=MEM_A_DQ<2>	93 11	MEM_B_DQ<2>
93 11	MEM_A_DQ<1>	MAKE_BASE=TRUE	=MEM_A_DQ<1>	93 11	MEM_B_DQ<1>
93 11	MEM_A_DQ<0>	MAKE_BASE=TRUE	=MEM_A_DQ<0>	93 11	MEM_B_DQ<0>

CPU CHANNEL A DQS 1 -> DIMM A DQS 1

93 11	MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=MEM_A_DQS_N<1>	93 11	MEM_B_DQS_N<1>
93 11	MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=MEM_A_DQS_P<1>	93 11	MEM_B_DQS_P<1>
93 11	MEM_A_DQ<15>	MAKE_BASE=TRUE	=MEM_A_DQ<15>	93 11	MEM_B_DQ<15>
93 11	MEM_A_DQ<14>	MAKE_BASE=TRUE	=MEM_A_DQ<14>	93 11	MEM_B_DQ<14>
93 11	MEM_A_DQ<13>	MAKE_BASE=TRUE	=MEM_A_DQ<13>	93 11	MEM_B_DQ<13>
93 11	MEM_A_DQ<12>	MAKE_BASE=TRUE	=MEM_A_DQ<12>	93 11	MEM_B_DQ<12>
93 11	MEM_A_DQ<11>	MAKE_BASE=TRUE	=MEM_A_DQ<11>	93 11	MEM_B_DQ<11>
93 11	MEM_A_DQ<10>	MAKE_BASE=TRUE	=MEM_A_DQ<10>	93 11	MEM_B_DQ<10>
93 11	MEM_A_DQ<9>	MAKE_BASE=TRUE	=MEM_A_DQ<9>	93 11	MEM_B_DQ<9>
93 11	MEM_A_DQ<8>	MAKE_BASE=TRUE	=MEM_A_DQ<8>	93 11	MEM_B_DQ<8>

CPU CHANNEL A DQS 2 -> DIMM A DQS 2

93 11	MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=MEM_A_DQS_N<2>	93 11	MEM_B_DQS_N<2>
93 11	MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=MEM_A_DQS_P<2>	93 11	MEM_B_DQS_P<2>
93 11	MEM_A_DQ<23>	MAKE_BASE=TRUE	=MEM_A_DQ<23>	93 11	MEM_B_DQ<23>
93 11	MEM_A_DQ<22>	MAKE_BASE=TRUE	=MEM_A_DQ<22>	93 11	MEM_B_DQ<22>
93 11	MEM_A_DQ<21>	MAKE_BASE=TRUE	=MEM_A_DQ<21>	93 11	MEM_B_DQ<21>
93 11	MEM_A_DQ<20>	MAKE_BASE=TRUE	=MEM_A_DQ<20>	93 11	MEM_B_DQ<20>
93 11	MEM_A_DQ<19>	MAKE_BASE=TRUE	=MEM_A_DQ<19>	93 11	MEM_B_DQ<19>
93 11	MEM_A_DQ<18>	MAKE_BASE=TRUE	=MEM_A_DQ<18>	93 11	MEM_B_DQ<18>
93 11	MEM_A_DQ<17>	MAKE_BASE=TRUE	=MEM_A_DQ<17>	93 11	MEM_B_DQ<17>
93 11	MEM_A_DQ<16>	MAKE_BASE=TRUE	=MEM_A_DQ<16>	93 11	MEM_B_DQ<16>

CPU CHANNEL A DQS 3 -> DIMM A DQS 3

93 11	MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=MEM_A_DQS_N<3>	93 11	MEM_B_DQS_N<3>
93 11	MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=MEM_A_DQS_P<3>	93 11	MEM_B_DQS_P<3>
93 11	MEM_A_DQ<31>	MAKE_BASE=TRUE	=MEM_A_DQ<31>	93 11	MEM_B_DQ<31>
93 11	MEM_A_DQ<30>	MAKE_BASE=TRUE	=MEM_A_DQ<30>	93 11	MEM_B_DQ<30>
93 11	MEM_A_DQ<29>	MAKE_BASE=TRUE	=MEM_A_DQ<29>	93 11	MEM_B_DQ<29>
93 11	MEM_A_DQ<28>	MAKE_BASE=TRUE	=MEM_A_DQ<28>	93 11	MEM_B_DQ<28>
93 11	MEM_A_DQ<27>	MAKE_BASE=TRUE	=MEM_A_DQ<27>	93 11	MEM_B_DQ<27>
93 11	MEM_A_DQ<26>	MAKE_BASE=TRUE	=MEM_A_DQ<26>	93 11	MEM_B_DQ<26>
93 11	MEM_A_DQ<25>	MAKE_BASE=TRUE	=MEM_A_DQ<25>	93 11	MEM_B_DQ<25>
93 11	MEM_A_DQ<24>	MAKE_BASE=TRUE	=MEM_A_DQ<24>	93 11	MEM_B_DQ<24>

CPU CHANNEL A DQS 4 -> DIMM A DQS 4

93 11	MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=MEM_A_DQS_N<4>	93 11	MEM_B_DQS_N<4>
93 11	MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=MEM_A_DQS_P<4>	93 11	MEM_B_DQS_P<4>
93 11	MEM_A_DQ<39>	MAKE_BASE=TRUE	=MEM_A_DQ<39>	93 11	MEM_B_DQ<39>
93 11	MEM_A_DQ<38>	MAKE_BASE=TRUE	=MEM_A_DQ<38>	93 11	MEM_B_DQ<38>
93 27 26 11	MEM_A_DQ<37>	MAKE_BASE=TRUE	MEM_A_DQ<37>	11 26 27 93 93 28 27 11	MEM_B_DQ<37>
93 11	MEM_A_DQ<36>	MAKE_BASE=TRUE	=MEM_A_DQ<36>	93 11	MEM_B_DQ<36>
93 11	MEM_A_DQ<35>	MAKE_BASE=TRUE	=MEM_A_DQ<35>	93 11	MEM_B_DQ<35>
93 11	MEM_A_DQ<34>	MAKE_BASE=TRUE	=MEM_A_DQ<34>	93 11	MEM_B_DQ<34>
93 11	MEM_A_DQ<33>	MAKE_BASE=TRUE	=MEM_A_DQ<33>	93 11	MEM_B_DQ<33>
93 11	MEM_A_DQ<32>	MAKE_BASE=TRUE	=MEM_A_DQ<32>	93 11	MEM_B_DQ<32>

CPU CHANNEL A DQS 5 -> DIMM A DQS 5

93 11	MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=MEM_A_DQS_N<5>	93 11	MEM_B_DQS_N<5>
93 11	MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=MEM_A_DQS_P<5>	93 11	MEM_B_DQS_P<5>
93 11	MEM_A_DQ<47>	MAKE_BASE=TRUE	=MEM_A_DQ<47>	93 11	MEM_B_DQ<47>
93 11	MEM_A_DQ<46>	MAKE_BASE=TRUE	=MEM_A_DQ<46>	93 11	MEM_B_DQ<46>
93 11	MEM_A_DQ<45>	MAKE_BASE=TRUE	=MEM_A_DQ<45>	93 11	MEM_B_DQ<45>
93 11	MEM_A_DQ<44>	MAKE_BASE=TRUE	=MEM_A_DQ<44>	93 11	MEM_B_DQ<44>
93 11	MEM_A_DQ<43>	MAKE_BASE=TRUE	=MEM_A_DQ<43>	93 11	MEM_B_DQ<43>
93 11	MEM_A_DQ<42>	MAKE_BASE=TRUE	=MEM_A_DQ<42>	93 11	MEM_B_DQ<42>
93 11	MEM_A_DQ<41>	MAKE_BASE=TRUE	=MEM_A_DQ<41>	93 11	MEM_B_DQ<41>
93 11	MEM_A_DQ<40>	MAKE_BASE=TRUE	=MEM_A_DQ<40>	93 11	MEM_B_DQ<40>

CPU CHANNEL A DQS 6 -> DIMM A DQS 6

93 11	MEM_A_DQS_N<6>	MAKE_BASE=TRUE	=MEM_A_DQS_N<6>	93 11	MEM_B_DQS_N<6>
93 11	MEM_A_DQS_P<6>	MAKE_BASE=TRUE	=MEM_A_DQS_P<6>	93 11	MEM_B_DQS_P<6>
93 11	MEM_A_DQ<55>	MAKE_BASE=TRUE	=MEM_A_DQ<55>	93 11	MEM_B_DQ<55>
93 11	MEM_A_DQ<54>	MAKE_BASE=TRUE	=MEM_A_DQ<54>	93 11	MEM_B_DQ<54>
93 11	MEM_A_DQ<53>	MAKE_BASE=TRUE	=MEM_A_DQ<53>	93 11	MEM_B_DQ<53>
93 11	MEM_A_DQ<52>	MAKE_BASE=TRUE	=MEM_A_DQ<52>	93 11	MEM_B_DQ<52>
93 11	MEM_A_DQ<51>	MAKE_BASE=TRUE	=MEM_A_DQ<51>	93 11	MEM_B_DQ<51>
93 11	MEM_A_DQ<50>	MAKE_BASE=TRUE	=MEM_A_DQ<50>	93 11	MEM_B_DQ<50>
93 11	MEM_A_DQ<49>	MAKE_BASE=TRUE	=MEM_A_DQ<49>	93 11	MEM_B_DQ<49>
93 11	MEM_A_DQ<48>	MAKE_BASE=TRUE	=MEM_A_DQ<48>	93 11	MEM_B_DQ<48>

CPU CHANNEL A DQS 7 -> DIMM A DQS 7

93 11	MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=MEM_A_DQS_N<7>	93 11	MEM_B_DQS_N<7>
93 11	MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=MEM_A_DQS_P<7>	93 11	MEM_B_DQS_P<7>
93 11	MEM_A_DQ<63>	MAKE_BASE=TRUE	=MEM_A_DQ<63>	93 11	MEM_B_DQ<63>
93 11	MEM_A_DQ<62>	MAKE_BASE=TRUE	=MEM_A_DQ<62>	93 11	MEM_B_DQ<62>
93 11	MEM_A_DQ<61>	MAKE_BASE=TRUE	=MEM_A_DQ<61>	93 11	MEM_B_DQ<61>
93 11	MEM_A_DQ<60>	MAKE_BASE=TRUE	=MEM_A_DQ<60>	93 11	MEM_B_DQ<60>
93 11	MEM_A_DQ<59>	MAKE_BASE=TRUE	=MEM_A_DQ<59>	93 11	MEM_B_DQ<59>
93 11	MEM_A_DQ<58>	MAKE_BASE=TRUE	=MEM_A_DQ<58>	93 11	MEM_B_DQ<58>
93 11	MEM_A_DQ<57>	MAKE_BASE=TRUE	=MEM_A_DQ<57>	93 11	MEM_B_DQ<57>
93 11	MEM_A_DQ<56>	MAKE_BASE=TRUE	=MEM_A_DQ<56>	93 11	MEM_B_DQ<56>

CPU CHANNEL B DQS 0 -> DIMM B DQS 0

CPU CHANNEL B DQS 1 -> DIMM B DQS 1

CPU CHANNEL B DQS 2 -> DIMM B DQS 2

CPU CHANNEL B DQS 3 -> DIMM B DQS 3

CPU CHANNEL B DQS 4 -> DIMM B DQS 4

CPU CHANNEL B DQS 5 -> DIMM B DQS 5

CPU CHANNEL B DQS 6 -> DIMM B DQS 6

CPU CHANNEL B DQS 7 -> DIMM B DQS 7

SYNC_MASTER=K92_YUN SYNC_DATE=05/14/2010

PAGE TITLE: DDR3 Byte/Bit Swaps

Apple Inc.

DRAWING NUMBER | SIZE: D

REVISION

BRANCH

PAGE: 30 OF 132

SHEET: 27 OF 105

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

PP1V5_S3

C3100 10UF 20% 6.3V X6S 603
C3101 10UF 20% 6.3V X6S 603
PLACE_NEAR=J3100.75:2.54mm

C3110 C3111 C3112 C3113 C3114 C3115 C3116 C3117 C3118 C3119 C3120 C3121 C3122 C3123
0.1UF 20% 10V CERM 402
PLACE_NEAR=J3100.75:2.54mm

PP0V75_S3_MEM_VREFDQ_B

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

PP0V75_S3_MEM_VREFCA_B

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

PP3V3_S0

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402

PP0V75_S0_DDRVTT

C3150 C3151 C3152 C3153
1UF 10% 10V X5R 402

J3100 F-RT-BGA6
DDR3-SODIMM (2 OF 2)

73	CKE0		74	CKE1	
75	VDD		76	VDD	
77	NC	NC	78	A15	MEM_B_A<15>
79	BA2		80	A14	MEM_B_A<14>
81	VDD		82	VDD	
83	A12/BC*	MEM_B_A<12>	84	A11	MEM_B_A<11>
85	A9	MEM_B_A<9>	86	A7	MEM_B_A<7>
87	VDD		88	VDD	
89	A8	MEM_B_A<8>	90	A6	MEM_B_A<6>
91	A5	MEM_B_A<5>	92	A4	MEM_B_A<4>
93	VDD		94	VDD	
95	A3	MEM_B_A<3>	96	A2	MEM_B_A<2>
97	A1	MEM_B_A<1>	98	A0	MEM_B_A<0>
99	VDD		100	VDD	
101	CK0	MEM_B_CLK_P<0>	102	CK1	MEM_B_CLK_P<1>
103	CK0*	MEM_B_CLK_N<0>	104	CK1*	MEM_B_CLK_N<1>
105	VDD		106	VDD	
107	A10/AP	MEM_B_A<10>	108	BA1	MEM_B_BA<1>
109	BA0	MEM_B_BA<0>	110	RAS*	MEM_B_RAS_L
111	VDD		112	VDD	
113	WE*	MEM_B_WE_L	114	S0*	MEM_B_CS_L<0>
115	CAS*	MEM_B_CAS_L	116	ODT0	MEM_B_ODT<0>
117	VDD		118	VDD	
119	A13	MEM_B_A<13>	120	ODT1	MEM_B_ODT<1>
121	S1*	MEM_B_CS_L<1>	122	NC	NC
123	VDD		124	VDD	
125	TEST	NC	126	VREFCA	
127	VSS		128	VSS	
129	DQ32	=MEM_B_DQ<32>	130	DQ36	=MEM_B_DQ<36>
131	DQ33	=MEM_B_DQ<33>	132	DQ37	MEM_B_DQ<37>
133	VSS		134	VSS	
135	DQS4*	=MEM_B_DQS_N<4>	136	DM4	
137	DQS4	=MEM_B_DQS_P<4>	138	VSS	
139	VSS		140	DQ38	=MEM_B_DQ<38>
141	DQ34	=MEM_B_DQ<34>	142	DQ39	=MEM_B_DQ<39>
143	DQ35	=MEM_B_DQ<35>	144	VSS	
145	VSS		146	DQ44	=MEM_B_DQ<44>
147	DQ40	=MEM_B_DQ<40>	148	DQ45	=MEM_B_DQ<45>
149	DQ41	=MEM_B_DQ<41>	150	VSS	
151	VSS		152	DQS5*	=MEM_B_DQS_N<5>
153	DM5		154	DQS5	=MEM_B_DQS_P<5>
155	VSS		156	VSS	
157	DQ42	=MEM_B_DQ<42>	158	DQ46	=MEM_B_DQ<46>
159	DQ43	=MEM_B_DQ<43>	160	DQ47	=MEM_B_DQ<47>
161	VSS		162	VSS	
163	DQ48	=MEM_B_DQ<48>	164	DQ52	=MEM_B_DQ<52>
165	DQ49	=MEM_B_DQ<49>	166	DQ53	=MEM_B_DQ<53>
167	VSS		168	VSS	
169	DQS6*	=MEM_B_DQS_N<6>	170	DM6	
171	DQS6	=MEM_B_DQS_P<6>	172	VSS	
173	VSS		174	DQ54	=MEM_B_DQ<54>
175	DQ50	=MEM_B_DQ<50>	176	DQ55	=MEM_B_DQ<55>
177	DQ51	=MEM_B_DQ<51>	178	VSS	
179	VSS		180	DQ60	=MEM_B_DQ<60>
181	DQ56	=MEM_B_DQ<56>	182	DQ61	=MEM_B_DQ<61>
183	DQ57	=MEM_B_DQ<57>	184	VSS	
185	VSS		186	DQS7*	=MEM_B_DQS_N<7>
187	DM7		188	DQS7	=MEM_B_DQS_P<7>
189	VSS		190	VSS	
191	DQ58	=MEM_B_DQ<58>	192	DQ62	=MEM_B_DQ<62>
193	DQ59	=MEM_B_DQ<59>	194	DQ63	=MEM_B_DQ<63>
195	VSS		196	VSS	
197	SA0	MEM_B_SA<0>	198	EVENT*	MEM_EVENT_L
199	VDDSPD		200	SDA	SMBUS_PCH_DATA
201	SA1	MEM_B_SA<1>	202	SCL	SMBUS_PCH_CLK
203	VTT		204	VTT	
205	MTG PIN		206	MTG PIN	
207	MTG PIN		208	MTG PIN	
209	MTG PIN		210	MTG PIN	
211	MTG PIN		212	MTG PIN	

516S0806
SPD ADDR=0xA4(WR)/0xA5(RD)

J3100 F-RT-BGA6
DDR3-SODIMM (1 OF 2)
CRITICAL

1	VREFDQ		2	VSS	
3	VSS		4	DQ4	=MEM_B_DQ<4>
5	DQ0	=MEM_B_DQ<0>	6	DQ5	=MEM_B_DQ<5>
7	DQ1	=MEM_B_DQ<1>	8	VSS	
9	VSS		10	DQS0*	MEM_B_DQS_N<0>
11	DM0		12	DQS0	MEM_B_DQS_P<0>
13	VSS		14	VSS	
15	DQ2	=MEM_B_DQ<2>	16	DQ6	=MEM_B_DQ<6>
17	DQ3	=MEM_B_DQ<3>	18	DQ7	=MEM_B_DQ<7>
19	VSS		20	VSS	
21	DQ8	=MEM_B_DQ<8>	22	DQ12	=MEM_B_DQ<12>
23	DQ9	=MEM_B_DQ<9>	24	DQ13	=MEM_B_DQ<13>
25	VSS		26	VSS	
27	DQS1*	=MEM_B_DQS_N<1>	28	DM1	
29	DQS1	=MEM_B_DQS_P<1>	30	RESET*	MEM_RESET_L
31	VSS		32	VSS	
33	DQ10	=MEM_B_DQ<10>	34	DQ14	=MEM_B_DQ<14>
35	DQ11	=MEM_B_DQ<11>	36	DQ15	=MEM_B_DQ<15>
37	VSS		38	VSS	
39	DQ16	=MEM_B_DQ<16>	40	DQ20	=MEM_B_DQ<20>
41	DQ17	=MEM_B_DQ<17>	42	DQ21	=MEM_B_DQ<21>
43	VSS		44	VSS	
45	DQS2*	=MEM_B_DQS_N<2>	46	DM2	
47	DQS2	=MEM_B_DQS_P<2>	48	VSS	
49	VSS		50	DQ22	=MEM_B_DQ<22>
51	DQ18	=MEM_B_DQ<18>	52	DQ23	=MEM_B_DQ<23>
53	DQ19	=MEM_B_DQ<19>	54	VSS	
55	VSS		56	DQ28	=MEM_B_DQ<28>
57	DQ24	=MEM_B_DQ<24>	58	DQ29	=MEM_B_DQ<29>
59	DQ25	=MEM_B_DQ<25>	60	VSS	
61	VSS		62	DQS3*	=MEM_B_DQS_N<3>
63	DM3		64	DQS3	=MEM_B_DQS_P<3>
65	VSS		66	VSS	
67	DQ26	=MEM_B_DQ<26>	68	DQ30	=MEM_B_DQ<30>
69	DQ27	=MEM_B_DQ<27>	70	DQ31	=MEM_B_DQ<31>
71	VSS		72	VSS	

516S0806

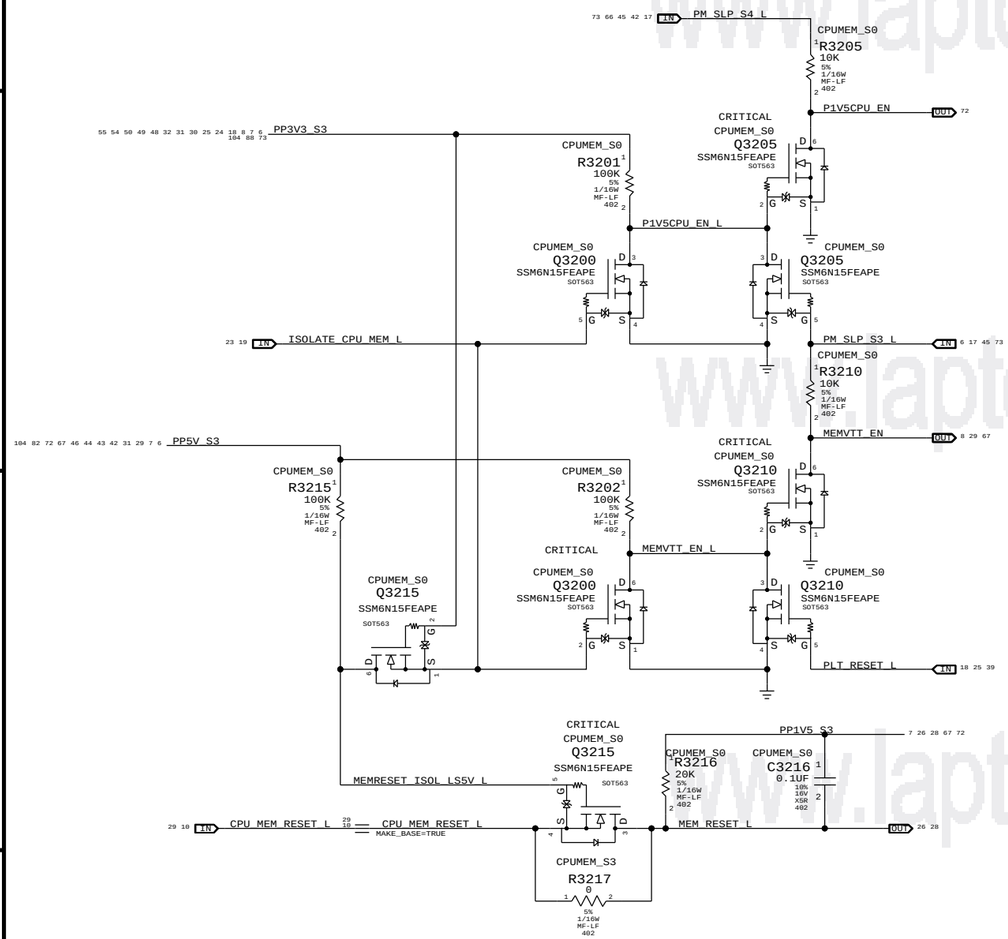
"Expansion" (bottom) slot

SYNC_MASTER=K92_YUN SYNC_DATE=06/14/2010
PAGE TITLE: DDR3 SO-DIMM Connector B
Apple Inc.
DRAWING NUMBER
SIZE: D
REVISION
BRANCH
PAGE: 31 OF 132
SHEET: 28 OF 105

The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

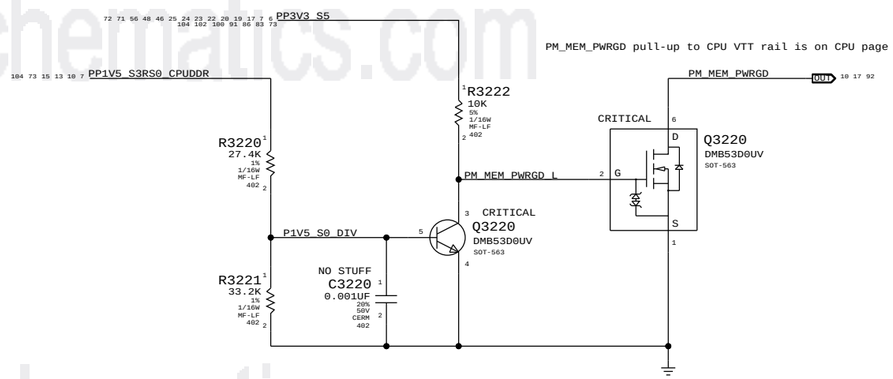
ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L



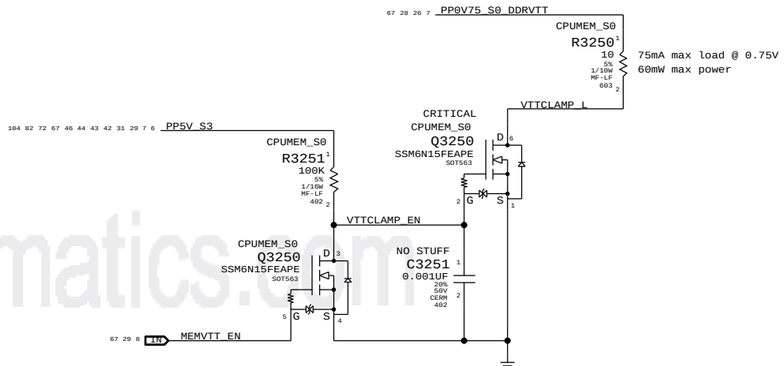
1V5 S0 "PGOOD" for CPU

PM_MEM_PWRGD pull-up to CPU VTT rail is on CPU page



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
to	4	0	0	1	1	X	1	0	1
S0	5	0	1	1	1	0 (*)	1	1	1
	6	0	1	1	1	1	1	1	1
	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC_MASTER=K17_MLB SYNC_DATE=04/26/2010

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

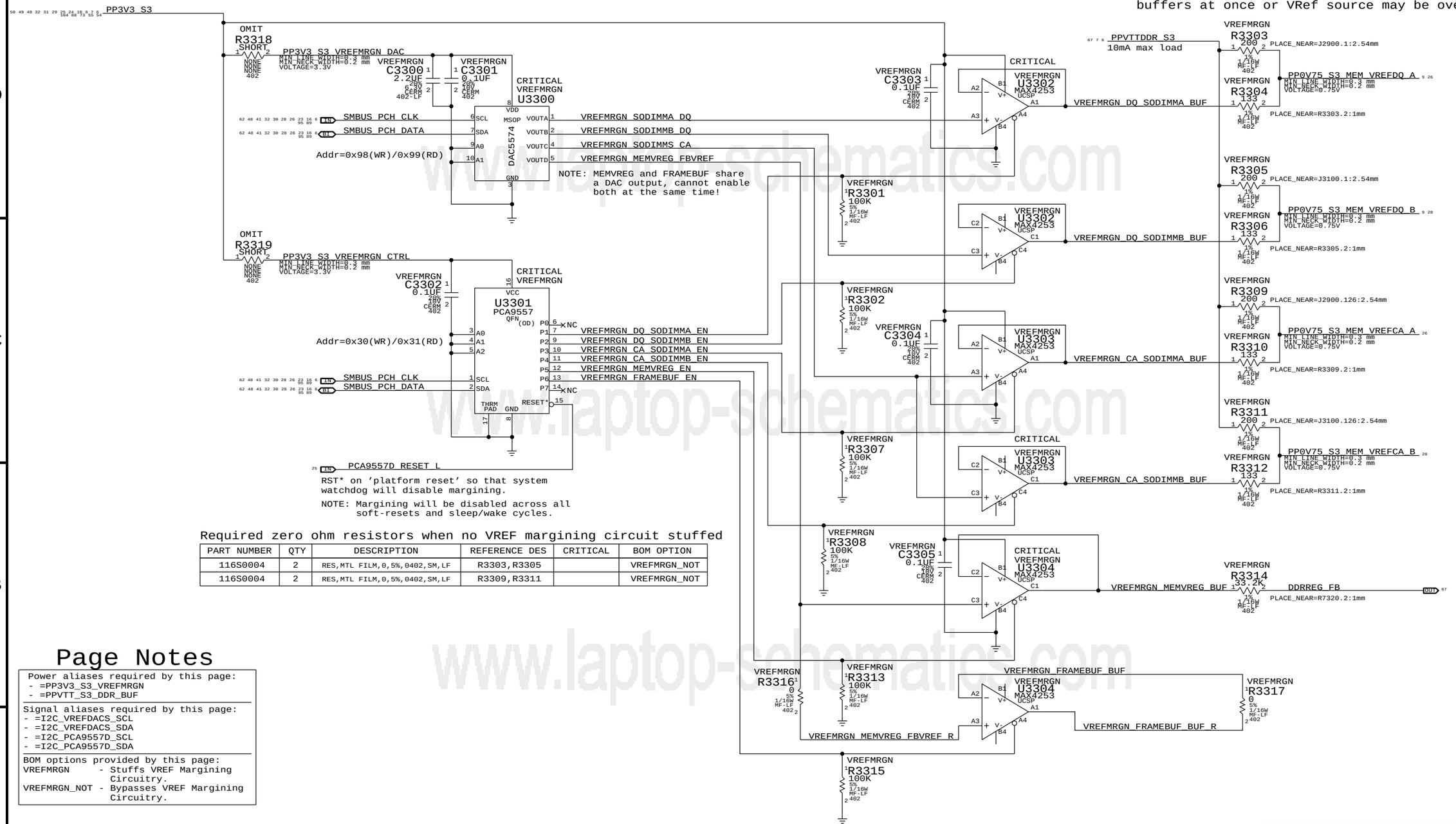
DRAWING NUMBER: D SIZE

REVISION

BRANCH

PAGE: 32 OF 132

SHEET: 29 OF 105



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3303,R3305		VREFMRGN_NOT
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3309,R3311		VREFMRGN_NOT

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.
VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=K91_YUN SYNC_DATE=08/26/2010

PAGE TITLE: FSB/DDR3/FRAMEBUF Vref Margining

Apple Inc.

DRAWING NUMBER | SIZE: D

REVISION

BRANCH

PAGE: 33 OF 132

SHEET: 30 OF 105

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	4	RES, 0OHM, 0201	L3470,L3471,L3473,L3474		

3V S3 WLAN FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	1 A (EDP)

AIRPORT

BLUETOOTH

ALS CAMERA

Supervisor & CLKFREG # Isolation

Delay = 60 ms +/- 20%

275 mA peak
206 mA nominal max

SYNC_MASTER=K91_MLB	SYNC_DATE=10/21/2016
PAGE TITLE	X19/ALS/CAMERA CONNECTOR
Apple Inc.	DRAWING NUMBER: D
	REVISION:
	BRANCH:
	PAGE: 34 OF 132
	SHEET: 31 OF 105

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

OMIT
R3504
SHORT NONE NONE
PP3V3_S3 — PP3V3_S3_EXCARD_R
NONE 402
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=3.3V

OMIT
R3503
SHORT NONE NONE
PP3V3_S0 — PP3V3_S0_EXCARD_R
NONE 402
MIN_LINE_WIDTH=0.3mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=3.3V

OMIT
R3502
SHORT NONE NONE
PP1V5_S0 — PP1V5_S0_EXCARD_R
NONE 402
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=1.5V

R3505
0
1/16W 5% MF-LF 402
TP_EXCARD_STBY_L
PLT_RST_BUF_L (IN) — EXCARD_RESET_R_L
EXCARD_OC_L (OUT)

PP3V3_S3
C3550 0.1uF 20% 10V CERM 402
32 6 EXCARD_CPUSB_L
32 6 EXCARD_CPPE_L
U3551 74HC1G00GWDG SC70-5
EXCARD_CP

CRITICAL
U3500
TPS2231
QFN
AUXIN 17 — AUXOUT 15
VIN3P3 2 — VOUT3P3 3
VIN1P5 12 — VOUT1P5 11
SHDN* 20
STBY* 1
SYSRST* 6
OC* 19
(IPU)
PERST* 8
CPPE* 10
CPUSB* 9
(IPU)
NC0 4
NC1 5
NC2 13
NC3 14
NC4 16
RCLKEN 18 (IPU) — EXCARD_RCLKEN 32
THRML_PAD 21
GND 7
All pull-ups to AUXIN rail

OUTPUT DECOUPLING

PP3V3_S3_EXCARD_SWITCH 6 32
VOLTAGE=3.3V
C3500 0.1uF 20% 16V CERM 402
C3503 10uF 20% 6.3V X5R 603

PP3V3_S0_EXCARD_SWITCH 6 32
VOLTAGE=3.3V
C3501 0.1UF 10% 16V X5R 402-1
C3504 10uF 20% 6.3V X5R 603

PP1V5_S0_EXCARD_SWITCH 6 32
VOLTAGE=1.5V
C3502 0.1UF 10% 16V X5R 402-1
C3505 10uF 20% 6.3V X5R 603

PLT_RESET_SWITCH_L 6 32
EXCARD_CPPE_L 6 32
EXCARD_CPUSB_L 6 32

EXPRESSCARD/34 FLEX CONNECTOR

CRITICAL
J3500
502250-8627
SHORT

100 32 6	PCIE_EXCARD_R2D_N	PCIE_EXCARD_R2D_P	6 32 100
100 16 6 OUT	PCIE_EXCARD_D2R_P	PCIE_EXCARD_D2R_N	OUT 6 16 100
100 32 6	PCIE_CLK100M_EXCARD_CONN_N	PCIE_CLK100M_EXCARD_CONN_P	6 32 100
32 6	EXCARD_CLKREQ_CONN_L	EXCARD_CPPE_L	6 32
32 6	PP3V3_S0_EXCARD_SWITCH	PP3V3_S0_EXCARD_SWITCH	6 32
32 6	PP3V3_S3_EXCARD_SWITCH	PLT_RESET_SWITCH_L	6 32
32 6	PP1V5_S0_EXCARD_SWITCH	PCIE_WAKE_L	OUT 6 17 25 31 85
89 62 48 41 30 28 26 23 16 6 95 B1	SMBUS_PCH_DATA	PP1V5_S0_EXCARD_SWITCH	6 32
	NC	SMBUS_PCH_CLK	B1 6 16 23 26 28 30 41 48 62 89 95
32 6	EXCARD_CPUSB_L	NC	
100 32 6	USB2_EXCARD_CONN_N	USB2_EXCARD_CONN_P	6 32 100

518S0647

DETECT-CHANGED PCH GPIO LATCH CIRCUIT

54 50 49 48 32 31 30 29 25 24 18 8 7 6 104 88 73 55 PP3V3_S3
C3510 1UF 10% 10V X5R 2 402-1

DLY block is 20ms nominal
When ENET_LOW_PWR deasserts, RST_OUT# deasserts for >80ms, then asserts for 10ms regardless of RST_IN# state. Otherwise RST_OUT# follows RST_IN#

Must STUFF R3512 and NOSTUFF R3514 when R3511 is NOT STUFFED.

R3514 and R3512 mutually exclusive to bypass reset logic

CRITICAL
U3511
SLG4AP014V
TDFN
VDD 1
LOW_PWR 2 — ENET_LOW_PWR (IN) 36 19
RST_IN* 3 — ENET_RESET_L_R (IN) 25
RST_OUT* 4 — SLG_ENET_RESET_OUT_L
DET_IN (IPU) 6
DET_CHNGD* (OD) 8 — NC
DET_OUT (OD) 7 — NC
GND 5
THRM PAD 9

R3514 0 5% 1/16W MF-LF 402
ENET_RESET_L (OUT) 36 19

NOSTUFF
R3512 0 5% 1/16W MF-LF 402

INPUT DECOUPLING

32 PP3V3_S3_EXCARD_R
C3530 0.1uF 20% 10V CERM 402
C3531 10uF 20% 6.3V X5R 603

25 22 20 16 7 71 57 41 32 PP1V5_S0
C3534 0.1uF 20% 10V CERM 402
C3535 10uF 20% 6.3V X5R 603

46 41 40 39 36 35 102 100 91 89 88 85 84 83 80 73 72 62 61 57 54 52 53 50 49 48 PP3V3_S0
32 EXCARD_RCLKEN
R3561 100K 1% 1/16W MF-LF 402
32 6 EXCARD_CLKREQ_CONN_L
U3561 SN74LVC1G04YZPR BGA
EXCARD_CLKREQ_CONN
U3560 74HC1G00GWDG SC70-5
EXCARD_CLKREQ_L (OUT) 16
C3560 0.1uF 20% 10V CERM 402

L3502
90-OHM DLP8NS

100 32 24 8 B1	USB_EXCARD_N — USB_EXCARD_N MAKE_BASE=TRUE	4 3	USB2_EXCARD_CONN_N 6 32 100
100 32 24 8 B1	USB_EXCARD_P — USB_EXCARD_P MAKE_BASE=TRUE	1 2	USB2_EXCARD_CONN_P 6 32 100

PLACE_NEAR=J3500.3:4mm

L3503
90-OHM-100MA DLP11S

95 16 IN	PCIE_CLK100M_EXCARD_N	4 3	PCIE_CLK100M_EXCARD_CONN_N 6 32 100
95 16 IN	PCIE_CLK100M_EXCARD_P	1 2	PCIE_CLK100M_EXCARD_CONN_P 6 32 100

PLACE_NEAR=J3500.19:4mm
PLACE_NEAR=J3500.24:4mm

100 16 IN	PCIE_EXCARD_R2D_C_N	C3571 0.1UF 10% 16V X5R 402-1	PCIE_EXCARD_R2D_N 6 32 100
100 16 IN	PCIE_EXCARD_R2D_C_P	C3570 0.1UF 10% 16V X5R 402-1	PCIE_EXCARD_R2D_P 6 32 100

PLACE_NEAR=J3500.25:4mm

SYNC_MASTER=K92_ERIC SYNC_DATE=07/27/2010
PAGE TITLE: ExpressCard Connector
Apple Inc.
DRAWING NUMBER: SIZE D
REVISION:
BRANCH:
PAGE: 35 OF 132
SHEET: 32 OF 105

SNK0 AC Coupling

DP_T29SNK0_ML_C_P<0>	C3620 0.1uF	DP_T29SNK0_ML_P<0>	
DP_T29SNK0_ML_C_N<0>	C3621 0.1uF	DP_T29SNK0_ML_N<0>	
DP_T29SNK0_ML_C_P<1>	C3622 0.1uF	DP_T29SNK0_ML_P<1>	
DP_T29SNK0_ML_C_N<1>	C3623 0.1uF	DP_T29SNK0_ML_N<1>	
DP_T29SNK0_ML_C_P<2>	C3624 0.1uF	DP_T29SNK0_ML_P<2>	
DP_T29SNK0_ML_C_N<2>	C3625 0.1uF	DP_T29SNK0_ML_N<2>	
DP_T29SNK0_ML_C_P<3>	C3626 0.1uF	DP_T29SNK0_ML_P<3>	
DP_T29SNK0_ML_C_N<3>	C3627 0.1uF	DP_T29SNK0_ML_N<3>	
DP_T29SNK0_AUXCH_C_P	C3628 0.1uF	DP_T29SNK0_AUXCH_P	
DP_T29SNK0_AUXCH_C_N	C3629 0.1uF	DP_T29SNK0_AUXCH_N	

SNK1 AC Coupling

DP_T29SNK1_ML_C_P<0>	C3630 0.1uF	DP_T29SNK1_ML_P<0>	
DP_T29SNK1_ML_C_N<0>	C3631 0.1uF	DP_T29SNK1_ML_N<0>	
DP_T29SNK1_ML_C_P<1>	C3632 0.1uF	DP_T29SNK1_ML_P<1>	
DP_T29SNK1_ML_C_N<1>	C3633 0.1uF	DP_T29SNK1_ML_N<1>	
DP_T29SNK1_ML_C_P<2>	C3634 0.1uF	DP_T29SNK1_ML_P<2>	
DP_T29SNK1_ML_C_N<2>	C3635 0.1uF	DP_T29SNK1_ML_N<2>	
DP_T29SNK1_ML_C_P<3>	C3636 0.1uF	DP_T29SNK1_ML_P<3>	
DP_T29SNK1_ML_C_N<3>	C3637 0.1uF	DP_T29SNK1_ML_N<3>	
DP_T29SNK1_AUXCH_C_P	C3638 0.1uF	DP_T29SNK1_AUXCH_P	
DP_T29SNK1_AUXCH_C_N	C3639 0.1uF	DP_T29SNK1_AUXCH_N	

CRITICAL
OMIT_TABLE
U3600
T29
FCBGA
(SYM 1 OF 2)

PCIE GEN2

RECEIVE

PCIE_T29_R2D_C_P<0>	C3600 0.1uF	PCIE_T29_R2D_P<0> V19
PCIE_T29_R2D_C_N<0>	C3601 0.1uF	PCIE_T29_R2D_N<0> T19
PCIE_T29_R2D_C_P<1>	C3602 0.1uF	PCIE_T29_R2D_P<1> P19
PCIE_T29_R2D_C_N<1>	C3603 0.1uF	PCIE_T29_R2D_N<1> M19
PCIE_T29_R2D_C_P<2>	C3604 0.1uF	PCIE_T29_R2D_P<2> K19
PCIE_T29_R2D_C_N<2>	C3605 0.1uF	PCIE_T29_R2D_N<2> H19
PCIE_T29_R2D_C_P<3>	C3606 0.1uF	PCIE_T29_R2D_P<3> F19
PCIE_T29_R2D_C_N<3>	C3607 0.1uF	PCIE_T29_R2D_N<3> D19

PER_0_P, PER_0_N, PER_1_P, PER_1_N, PER_2_P, PER_2_N, PER_3_P, PER_3_N

TRANSMIT

PCIE_T29_D2R_C_P<0>	C3640 0.1uF	PCIE_T29_D2R_P<0>
PCIE_T29_D2R_C_N<0>	C3641 0.1uF	PCIE_T29_D2R_N<0>
PCIE_T29_D2R_C_P<1>	C3642 0.1uF	PCIE_T29_D2R_P<1>
PCIE_T29_D2R_C_N<1>	C3643 0.1uF	PCIE_T29_D2R_N<1>
PCIE_T29_D2R_C_P<2>	C3644 0.1uF	PCIE_T29_D2R_P<2>
PCIE_T29_D2R_C_N<2>	C3645 0.1uF	PCIE_T29_D2R_N<2>
PCIE_T29_D2R_C_P<3>	C3646 0.1uF	PCIE_T29_D2R_P<3>
PCIE_T29_D2R_C_N<3>	C3647 0.1uF	PCIE_T29_D2R_N<3>

PET_0_P (V21), PET_0_N (T21), PET_1_P (P21), PET_1_N (M21), PET_2_P (K21), PET_2_N (H21), PET_3_P (F21), PET_3_N (D21)

TP_T29_MONDC0 — R3610 0 5% 1/16W MF-LF 402 — T29_MONDC0 B21 MONDC0
DEBUG: For monitoring current/voltage
TP_T29_MONDC1 — R3611 0 5% 1/16W MF-LF 402 — T29_MONDC1 A20 MONDC1
NO STUFF

TP_T29_MONOBSP — C3615 0.1uF — T29_MONOBSP K17 MONOBSP
DEBUG: For monitoring clock
TP_T29_MONOBSN — C3616 0.1uF — T29_MONOBSN M17 MONOBSN

PP3V3_T29

R3690 3.3K 5% 1/16W MF-LF 402
R3691 3.3K 5% 1/16W MF-LF 402
C3690 1UF 10% 6.3V CERM 402
R3692 3.3K 5% 1/16W MF-LF 402
R3693 3.3K 5% 1/16W MF-LF 402
R3623 10K 5% 1/16W MF-LF 402
R3622 10K 5% 1/16W MF-LF 402
R3621 10K 5% 1/16W MF-LF 402

CRITICAL
OMIT_TABLE
U3690
M95160
2KX8-1.8V
MLP

(T29_SPI_MOSI), (T29_SPI_CLK), (T29_SPI_CS_L), T29ROM_WP_L, T29ROM_HOLD_L, (T29_SPI_MISO)

MISC

CLK REQUEST

T29_CLKREQ_ISOL_L	PCIE_CLKREQ_0* P3
T29_GPIO<1>	PCIE_CLKREQ_1* N4
T29_GPIO<2>	PCIE_CLKREQ_2* M3
T29_RSVD	PCIE_CLKREQ_3* L4

EEPROM

T29_SPI_MOSI	EE_DI P1
T29_SPI_MISO	EE_DO M1
T29_SPI_CS_L	EE_CS* N2
T29_SPI_CLK	EE_CLK L2

T29_THERMD_P — THERM_DP A2
Use B1 GND ball for THERM_DN

TEST PORT

T29_TEST_EN	TEST_EN E4
TP_T29_TEST_POINT_0	TEST_POINT_0 P5
TP_T29_TEST_POINT_1	TEST_POINT_1 N6
TP_T29_TEST_POINT_2	TEST_POINT_2 M5
T29_TEST_POINT_3	TEST_POINT_3 L6

R3625 0 5% 1/16W MF-LF 402
R3629 0 5% 1/16W MF-LF 402

POWER ON RESET

Not used in host mode.

PCIE_RST_0*	TP_T29_PCIE_RESET0_L K1
PCIE_RST_1*	TP_T29_PCIE_RESET1_L J2
PCIE_RST_2*	TP_T29_PCIE_RESET2_L K3
PCIE_RST_3*	TP_T29_PCIE_RESET3_L J4

JTAG

JTAG_ISP_TDI	TDI T3
JTAG_T29_TMS	TMS R4
JTAG_ISP_TCK	TCK R2
JTAG_ISP_TDO	TDO T1

CLOCKS

PCIE_CLK100M_T29_P	REFCLK_100_IN_P H17
PCIE_CLK100M_T29_N	REFCLK_100_IN_N G16
SYSCLK_CLK25M_T29_R	XTAL_25_IN P17
TP_T29_XTAL25OUT	XTAL_25_OUT R16
T29_TMU_CLK_OUT	TMU_CLK_OUT U2
T29_TMU_CLK_IN	TMU_CLK_IN E2

PP3V3_T29
R3698 10K 5% 1/16W MF-LF 402
R3695 806 1% 1/16W MF-LF 402 — SYSCLK_CLK25M_T29
R3696 1K 5% 1/16W MF-LF 402
NO STUFF
R3699 10K 5% 1/16W MF-LF 402

R3651 10K 5% 1/16W MF-LF 402 — PP3V3_T29
WAKE* F1 T29_PCIE_WAKE_L
PERST* E6 T29_RESET_L
RSENSE E14 T29_RSENSE
R3655 1.0K 0.5% 1/16W MF-LF 603
RBIAS E16 T29_RBIAS

DISPLAY

SINK PORT 0

DP_T29SNK0_ML_P<3>	DPSNK0_ML_LANE_3P AA4
DP_T29SNK0_ML_N<3>	DPSNK0_ML_LANE_3N Y3
DP_T29SNK0_ML_P<2>	DPSNK0_ML_LANE_2P AA6
DP_T29SNK0_ML_N<2>	DPSNK0_ML_LANE_2N Y5
DP_T29SNK0_ML_P<1>	DPSNK0_ML_LANE_1P AA8
DP_T29SNK0_ML_N<1>	DPSNK0_ML_LANE_1N Y7
DP_T29SNK0_ML_P<0>	DPSNK0_ML_LANE_0P AA10
DP_T29SNK0_ML_N<0>	DPSNK0_ML_LANE_0N Y9
DP_T29SNK0_AUXCH_P	DPSNK0_AUX_CHP V1
DP_T29SNK0_AUXCH_N	DPSNK0_AUX_CHN W2
DP_T29SNK0_HPD	DPSNK0_HOT_PLUG_DET V5

SINK PORT 1

DP_T29SNK1_ML_P<3>	DPSNK1_ML_LANE_3P V9
DP_T29SNK1_ML_N<3>	DPSNK1_ML_LANE_3N U8
DP_T29SNK1_ML_P<2>	DPSNK1_ML_LANE_2P V11
DP_T29SNK1_ML_N<2>	DPSNK1_ML_LANE_2N U10
DP_T29SNK1_ML_P<1>	DPSNK1_ML_LANE_1P V13
DP_T29SNK1_ML_N<1>	DPSNK1_ML_LANE_1N U12
DP_T29SNK1_ML_P<0>	DPSNK1_ML_LANE_0P V15
DP_T29SNK1_ML_N<0>	DPSNK1_ML_LANE_0N U14
DP_T29SNK1_AUXCH_P	DPSNK1_AUX_CHP V7
DP_T29SNK1_AUXCH_N	DPSNK1_AUX_CHN U6
DP_T29SNK1_HPD	DPSNK1_HOT_PLUG_DET U4

R3630 100K 5% 1/16W MF-LF 402
R3631 100K 5% 1/16W MF-LF 402

SOURCE PORT 0

DPSRC0_ML_LANE_3P	TP_DP_T29SRC_ML_CP<3> AA18
DPSRC0_ML_LANE_3N	TP_DP_T29SRC_ML_CN<3> Y17
DPSRC0_ML_LANE_2P	TP_DP_T29SRC_ML_CP<2> AA16
DPSRC0_ML_LANE_2N	TP_DP_T29SRC_ML_CN<2> Y15
DPSRC0_ML_LANE_1P	TP_DP_T29SRC_ML_CP<1> AA14
DPSRC0_ML_LANE_1N	TP_DP_T29SRC_ML_CN<1> Y13
DPSRC0_ML_LANE_0P	TP_DP_T29SRC_ML_CP<0> AA12
DPSRC0_ML_LANE_0N	TP_DP_T29SRC_ML_CN<0> Y11
DPSRC0_AUX_CHP	TP_DP_T29SRC_AUXCH_CP W16
DPSRC0_AUX_CHN	TP_DP_T29SRC_AUXCH_CN U16
DPSRC0_HOT_PLUG_DET	T29_DP_SRC_HPD V3
DP_ATEST	T29_DP_ATEST Y19
DP_RES_0	Y21
DP_RES_1	T29_DP_RES AA20

100pF SRF > 40MHz
BYPASS=U3600.Y19::2mm
BYPASS=U3600.Y19::5.08mm

R3685 14.0K 1% 1/16W MF-LF 402
R3632 100K 5% 1/16W MF-LF 402
C3685 100PF 5% 50V CERM 402
C3686 0.01UF 10% 16V CERM 402

PORTS

PORT0

T29_R2D_C_P<0>	T29_R2D_C_P<0> A6
T29_R2D_C_N<0>	T29_R2D_C_N<0> A4
T29_D2R_P<0>	T29_D2R_P<0> C4
T29_D2R_N<0>	T29_D2R_N<0> C2
T29_LSEO<0>	T29_0_LSEO J6
T29_LSOE<0>	T29_0_LSOE K5

PORT1

T29_R2D_C_P<1>	PRT1_T29T_P A10
T29_R2D_C_N<1>	PRT1_T29T_N A8
T29_D2R_P<1>	PRT1_T29R_P C8
T29_D2R_N<1>	PRT1_T29R_N C6
T29_LSEO<1>	T29_1_LSEO G6
T29_LSOE<1>	T29_1_LSOE H5

I2C_T29_SDA — T29_SDA F3
I2C_T29_SCL — T29_SCL F5

PORT2

NC_T29_R2D_CP<2>	PRT2_T29T_P A14
NC_T29_R2D_CN<2>	PRT2_T29T_N A12
NC_T29_D2RP<2>	PRT2_T29R_P C12
NC_T29_D2RN<2>	PRT2_T29R_N C10
T29_LSEO_LSOE2	T29_2_LSEO G4
T29_LSEO_LSOE2	T29_2_LSOE H3

PORT3

NC_T29_R2D_CP<3>	PRT3_T29T_P A18
NC_T29_R2D_CN<3>	PRT3_T29T_N A16
NC_T29_D2RP<3>	PRT3_T29R_P C16
NC_T29_D2RN<3>	PRT3_T29R_N C14
T29_LSEO_LSOE3	T29_3_LSEO G2
T29_LSEO_LSOE3	T29_3_LSOE H1

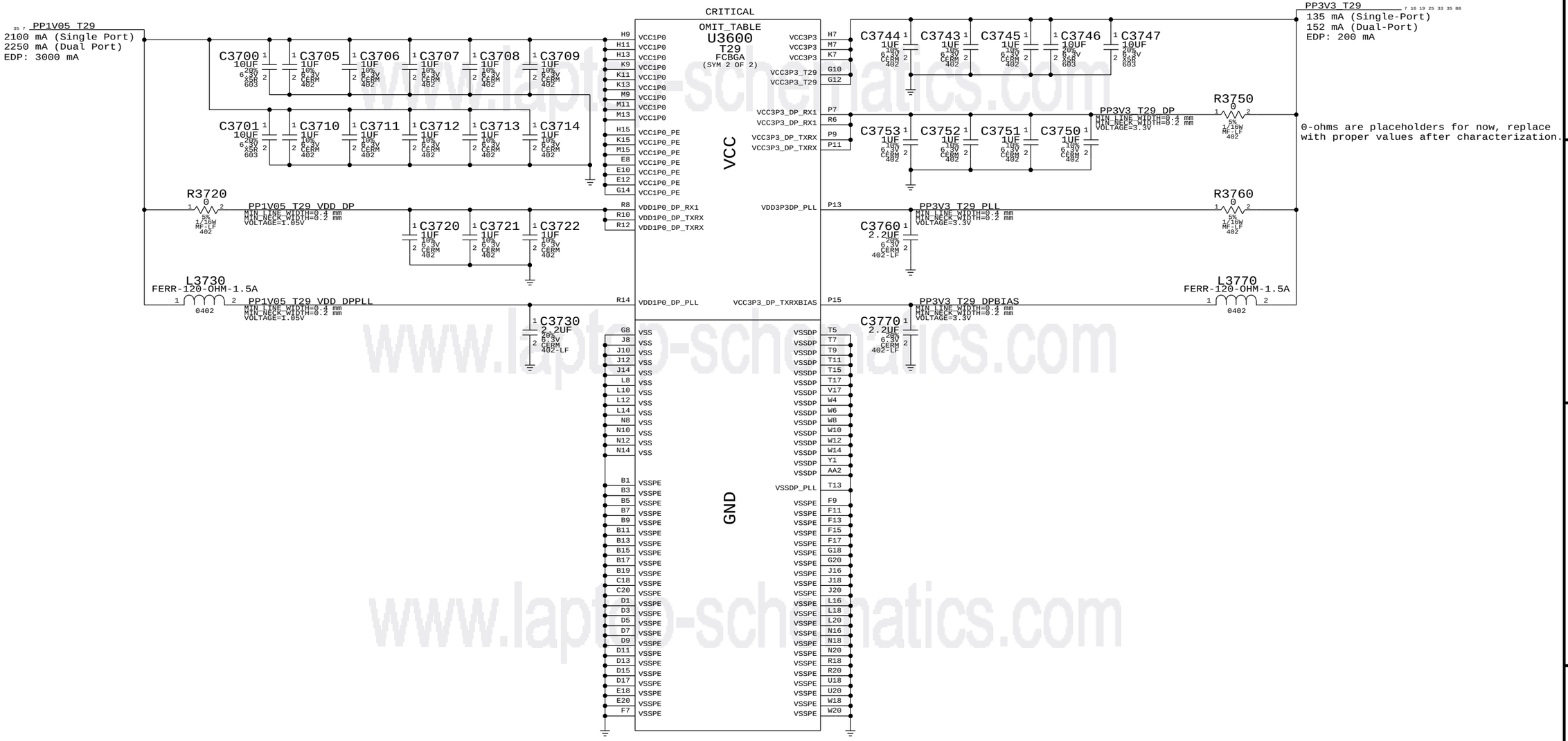
NOTE: All unused LSOE/EO pairs should be aliased together. Other signals okay to float (TP/NC).

SYNC_MASTER=T29_REF SYNC_DATE=11/09/2010

PAGE TITLE: T29 Host (1 of 2)

Apple Inc.

DRAWING NUMBER — SIZE: D
REVISION
BRANCH
PAGE: 36 OF 132
SHEET: 33 OF 105



Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC_MASTER=T29_REF SYNC_DATE=11/09/2010

PAGE TITLE: T29 Host (2 of 2)

Apple Inc.

DRAWING NUMBER | SIZE: D

REVISION

BRANCH

PAGE: 37 OF 132

SHEET: 34 OF 105

Page Notes

Power aliases required by this page:
- =PPVIN_SW_T29BST (8-13V Boost Input)
- =PP18V_T29_REG (18V Boost Output)
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

Signal aliases required by this page:
- =T29_CLKREQ_L
- =T29_RESET_L

BOM options provided by this page:
T29BST:Y - Stuffs 18V boost circuitry.

T29 15V Boost Regulator

PPBUS_G3H
8-13V Input
Changes required for 2S.

T29BST:Y R3880 470K 5% 1/16W MF-LF 402
T29BST:Y C3880 0.1UF 10% 25V X5R 402
T29BST_PWREN_DIV_L
T29BST:Y R3881 330K 5% 1/10W MF-LF 402
T29BST_PWREN_L
T29BST:Y Q3805 SSM3K15FV SOD-VESM-HF
T29_A_HV_EN

CRITICAL
T29BST:Y Q3880 SI8409DB 86A

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

PPVIN_SW_T29BST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here, add property on another page.

T29BST:Y C3890 10UF 10% 25V X5R 805
T29BST:Y C3891 10UF 10% 25V X5R 805
T29BST:Y R3891 200K 1% 1/10W MF-LF 402 <R1>
T29BST_EN_UVLO

CRITICAL
T29BST:Y L3895 10UH-4A-68-MOHM PCMB063T-100MS

T29BST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL
T29BST:Y U3890 LT3957 QFN
VIN, SW, SNS1, SNS2, EN/UVLO, INTVCC, VC, RT, SS, SYNC, NC, FBX, SGND, GND

T29BST_SNS1
T29BST:Y R3889 0 5% 1/10W MF-LF 402
CRITICAL
T29BST:Y D3895 POWERDI-123 DFLS230L
T29BST_SNS2
XW3895 SM PLACE_NEAR=C3895.1:2 mm

T29BST_INTVCC
T29BST:Y C3892 4.7UF 10% 10V X5R 805

T29BST_VC
NO STUFF T29BST:Y C3887 100PF 5% 50V CERM 402
T29BST:Y R3893 10K 1% 1/10W MF-LF 402

T29BST_RT
T29BST:Y R3892 73.2K 1% 1/10W MF-LF 402 <R2>

T29BST_SS
T29BST_VC_RC
T29BST:Y C3893 0.01UF 10% 50V X7R 402
T29BST:Y R3894 41.2K 1% 1/10W MF-LF 402

T29BST:Y C3894 0.33UF 10% 6.3V CERM-X5R 402

GND_T29BST_SGND
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

T29BST_VSNS
NO STUFF T29BST:Y C3888 100PF 5% 50V CERM 402
T29BST:Y R3895 137K 1% 1/10W MF-LF 402 <Ra>
T29BST_FBX
NO STUFF T29BST:Y C3889 100PF 5% 50V CERM 402
T29BST:Y R3896 15.8K 1% 1/10W MF-LF 402 <Rb>

T29BST:Y C3895 4.7UF 10% 10V X7R-CERM 1206
T29BST:Y C3896 4.7UF 10% 50V X7R-CERM 1206
T29BST:Y C3897 4.7UF 10% 50V X7R-CERM 1206
T29BST:Y C3898 4.7UF 10% 50V X7R-CERM 1206
T29BST:Y C3899 0.001UF 10% 50V X7R 402

PP15V_T29
Vout = 15.47V
Max Current = 1A
Freq = 300KHz

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

SGND shorted to GND inside package, no XW necessary.

Vout = 1.6V * (1 + Ra / Rb)

Supervisor & CLKREQ# Isolation

PP3V3_S0
C3800 0.1UF 10% 10V X5R 402
Platform (PCIe) Reset
PLT_RST_BUF_L
R3803 10K 5% 1/10W MF-LF 402
Open-Drain GPIO
T29_SW_RESET_L

CRITICAL
U3800 SLG4AP016V TDFN
VDD, SENSE 0.7V, DLY, RESET*, MR*, EN, OUT (OD), IN, GND, THRM PAD

PP3V3_T29
R3807 100K 5% 1/10W MF-LF 402
PP1V05_T29
T29_RESET_L
DLY = 60 ms +/- 20%
T29_CLKREQ_ISOL_L
T29_CLKREQ_ISOL_L
MAKE_BASE=TRUE
T29_CLKREQ_L
Pull-up provided by SB page.

T29BST:Y Q3888 SSM6N37FEAPE SOT563
Max Vgs: 10V
T29BST_SHDN_DIV
T29BST:Y R3888 330K 5% 1/10W MF-LF 402
T29BST:Y R3887 330K 5% 1/10W MF-LF 402
T29BST:Y Q3888 SSM6N37FEAPE SOT563
SMC_DELAYED_PWRGD

3.3V T29 Switch

PP3V3_S0
U3810 TPS22924 CSP
A2, B2, VIN, ON, C2, GND, C1, VOUT, A1, B1
CRITICAL
C3810 1UF 10% 6.3V CERM 402
PP3V3_T29
Max Current = 1.7A (85C)

U3810 & U3815/U3816

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A per IC

1.05V T29 Switch

PP1V05_S0
U3815 TPS22924 CSP
C3815 1UF 10% 6.3V CERM 402
PP1V05_T29
Max Current = 3.4A (85C)

U3816 TPS22924 CSP
T29_PWR_EN
Pull-up provided by SB page.
U3816.A2: PLACE_NEAR=U3815.B2:3 mm

SYNC_MASTER=T29_REF SYNC_DATE=11/09/2010

PAGE TITLE: T29 Power Support

Apple Inc.

DRAWING NUMBER: D
REVISION:
BRANCH:
PAGE: 38 OF 132
SHEET: 35 OF 105

BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

PP3V3_ENET
281mA (1000base-T max power, Caesar IV)

VDD for Card Reader I/O
PP3V3R1V8_ENET_LR_OUT_REG

CRITICAL L3900 FERR-600-OHM-0.5A — PP3V3_S3_ENET_PHY_XTALVDDH — C3900 0.1UF
CRITICAL L3905 FERR-600-OHM-0.5A — PP3V3_S3_ENET_PHY_BIASVDDH — C3905 0.1UF
CRITICAL L3910 FERR-600-OHM-0.5A — PP3V3_S3_ENET_PHY_AVDDH — R3910 4.7K, C3910 0.1UF, C3911 0.1UF

R3940 4.7K, R3941 4.7K, C3915 4.7UF, C3916 0.1UF

ENET_SR_LX
PP1V2_ENET
Internal 1.2V Switching Regulator pins.

PP1V2_ENET
???mA (1000base-T, Caesar V)

CRITICAL L3920 FERR-600-OHM-0.5A — PP1V2_ENET_PHY_AVDDL — C3921 0.1UF, C3920 4.7UF
CRITICAL L3925 FERR-600-OHM-0.5A — PP1V2_ENET_PHY_PCIEPLL — C3926 0.1UF, C3925 4.7UF
CRITICAL L3930 FERR-600-OHM-0.5A — PP1V2_ENET_PHY_GPHYPLL — C3931 0.1UF, C3930 4.7UF
C3936 0.1UF, CRITICAL C3935 10UF

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

PP3V3_S0
R3942 1K Current Limiting Resistor
C3950 0.1uF, C3951 0.1uF, C3955 0.1uF, C3956 0.1uF

PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_P
PCIE_ENET_R2D_C_N
R3943 0
ENET_WAKE_L
(See note)

WAKE#

Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested.
If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

OMIT
U3900
BCM57765B0
QFN-8X8
CRITICAL

ENET_VMAIN_PRSNT — VMAIN_PRSNT(IPD)
PCIE_ENET_D2R_C_N — PCIE_TXD_N
PCIE_ENET_D2R_C_P — PCIE_TXD_P
PCIE_ENET_R2D_P — PCIE_RXD_P
PCIE_ENET_R2D_N — PCIE_RXD_N
PCIE_CLK100M_ENET_P — PCIE_REFCLK_P
PCIE_CLK100M_ENET_N — PCIE_REFCLK_N
ENET_RESET_L — PERST* (IPD)
ENET_CLKREQ_L — CLKREQ* (OD)
ENET_WAKE_R_L — WAKE* (OD)
ENET_LOW_PWR — LOW_PWR (IPD)
BCM57765_SMB_CLK — SMB_CLK
BCM57765_SMB_DATA — SMD_DATA (IPD)
BCM57765_SCLK — SCLK
BCM57765_MISO — SI/LINKLED*
BCM57765_MOSI — SO
BCM57765_CS_L — CS*
NC_BCM57765_SPD100LED_L — SPD100LED*/SERIAL_DO (OD)
NC_BCM57765_TRAFFICLED_L — TRAFFICLED*/SERIAL_DI (OD)
SYSCLK_CLK25M_ENET — XTALI
NC — XTALO
BCM57765_RDAC — RDAC
THRM_PAD
R3965 1.24K

TRD0_P — ENET_MDI_P<0>
TRD0_N — ENET_MDI_N<0>
TRD1_P — ENET_MDI_P<1>
TRD1_N — ENET_MDI_N<1>
TRD2_P — ENET_MDI_P<2>
TRD2_N — ENET_MDI_N<2>
TRD3_P — ENET_MDI_P<3>
TRD3_N — ENET_MDI_N<3>

PP3V3R1V8_ENET_LR_OUT_REG
PP3V3R1V8_ENET_LR_OUT_REG
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
C3970 4.7UF, C3971 0.1UF, C3972 0.1UF

GPIO_0 — NC
GPIO_1/CR_BUS_PWR
RE*/GPIO_2 — ENET_MEDIA_SENSE
(IPD) SD_DETECT/WE* — TP_SDCONN_DETECT_L
(IPU) CR_CMD/CLE — TP_SDCONN_CMD
CR_CLK/RY_BY* — TP_SDCONN_CLK
CR_DATA0 — TP_SDCONN_DATA<0>
CR_DATA1 — TP_SDCONN_DATA<1>
CR_DATA2 — TP_SDCONN_DATA<2>
CR_DATA3 — TP_SDCONN_DATA<3>
CR_DATA4 — TP_SDCONN_DATA<4>
CR_DATA5 — TP_SDCONN_DATA<5>
CR_DATA6 — TP_SDCONN_DATA<6>
CR_DATA7 — TP_SDCONN_DATA<7>
CE*/MS_INS* — NC_CE_L_MS_INS_L
CR_LED/ALE — TP_ENET_CR_PWREN
CR_WP*/XD_WP* — TP_SDCONN_WP
XD_DETECT — BDM57765_SR_DISABLE — R3980 1K

NOTE: "IPx" == Programmable pull-up/down
SD_DETECT can only be used active low due to errata.

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

BCM57765 supports both active-levels for WP.

SR_DISABLE must be pulled down to use internal SR. IPD has a race condition.

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy.
Required for proper PHY operation.
(Required ROM size TBD)

PP3V3_ENET
U3990 AT45DB011D SOIC-8S1 OMIT
C3990 0.1UF
BCM57765_SCLK, BCM57765_CS_L, BCM57765_MOSI, BCM57765_MISO
NOSTUFF R3990 4.7K, R3997 4.7K

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC_MASTER=K92_ERIC SYNC_DATE=10/19/2010
PAGE TITLE
ETHERNET PHY (CAESAR IV)
Apple Inc.
DRAWING NUMBER D
REVISION
BRANCH
PAGE 39 OF 132
SHEET 36 OF 105

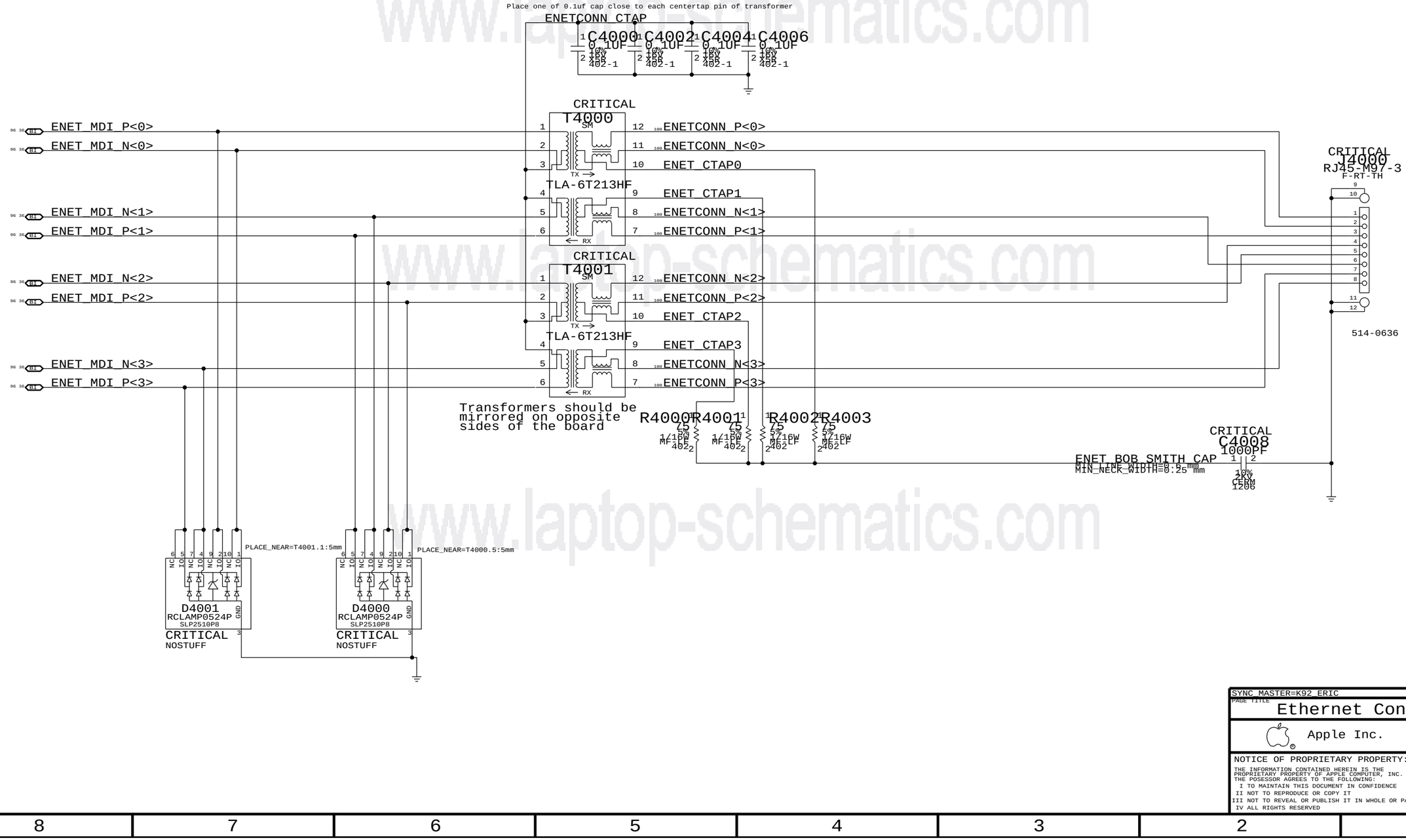
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC_MASTER=K92_ERIC SYNC_DATE=08/24/2010

PAGE TITLE: Ethernet Connector

Apple Inc.

DRAWING NUMBER | SIZE: D

REVISION

BRANCH

PAGE: 40 OF 132

SHEET: 37 OF 105

PP1V0_FW_FWPHY 135 mA
R4100 0 5% 1/10W MF-LF 402
PP1V0_FW_R MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.0V
L4110 120-OHM-0.3A-EMI 0402-LF
PP1V0_FW_FWPHY_AVDD MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.0V

PP3V3_FW_FWPHY 7 38 39 40 138 mA
7 mA I/O
C4120 C4121 C4122 C4123 C4124 1UF 10% 6.3V CERM 402
L4130 120-OHM-0.3A-EMI 0402-LF
114 mA FireWire PHY
PP3V3_FW_FWPHY_VDDA MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=3.3V
C4130 C4131 C4132 1UF 10% 6.3V CERM 402
L4135 120-OHM-0.3A-EMI 0402-LF
25 mA PCIe SerDes
C4110 C4111 1UF 10% 6.3V CERM 402
17 mA PCIe SerDes
PP3V3_FW_FWPHY_VP25 MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=3.3V
C4135 C4136 1UF 10% 6.3V CERM 402
110 mA Digital Core
C4100 C4101 C4102 C4103 C4104 C4105 C4106 1UF 10% 6.3V CERM 402
0 mA VReg PWR
C4141 0.1UF 20% 10V CERM 402
C4140 1UF 10% 6.3V CERM 402

VDD10 VDD33 VDDH VP VP25 VREG_PWR

OMIT CRITICAL
U4100 FW643 BGA

NC B13 ATBUSB
NC A13 ATBUSH
NC A11 ATBUSN

FWPHY_DS0 F12 DS0 (IPD) NT-19
FWPHY_DS1 E12 DS1 (IPD) NT-20
FWPHY_DS2 E13 DS2 (IPD) NT-21

NC_FW0_TPAN B8 TPA0N
NC_FW0_TPAP A8 TPA0P
FW_PORT1_TPA_N B5 TPA1N
FW_PORT1_TPA_P A5 TPA1P
NC_FW2_TPAN B3 TPA2N
NC_FW2_TPAP A3 TPA2P
NC_FW0_TPBN B9 TPB0N
NC_FW0_TPBP A9 TPB0P
FW_PORT1_TPB_N B6 TPB1N
FW_PORT1_TPB_P A6 TPB1P
NC_FW2_TPBN B4 TPB2N
NC_FW2_TPBP A4 TPB2P

NC_FW0_TPBIAS B7 TPBIAS0
FW_P1_TPBIAS C3 TPBIAS1
NC_FW2_TPBIAS A2 TPBIAS2

PPVP_FW_CPS
R4160 200K 1% 1/16W MF-LF 402
PLACE_NEAR=U4100.B10:2mm
FW643_R0 B11 R0
FW643_TPCPS B10 TPCPS

C4150 22PF 5% 50V CERM 402
C4151 22PF 5% 50V CERM 402
FW_CLK24P576M_XO CRITICAL Y4150 24.576MHZ SM-3.2X2.5MMZ
R4150 412 1% 1/16W MF-LF 402
R4161 2.94K 1% 1/16W MF-LF 402
R4170 191 1% 1/16W MF-LF 402
R4162 470K 5% 1/16W MF-LF 402
C4162 0.33UF 10% 6.3V CERM-X5R 402

TP_FW643_NAND_TREE K1 NAND_TREE NT-OUT
FW643_REXT L8 REXT
FW_CLK24P576M_XO_R F13 XO
FW_CLK24P576M_XI G13 XI NT-9
NOTE: NT-xx notes show NAND tree order.
TP_FW643_SE M13 SE (IPD)
TP_FW643_SM N13 SM (IPD)
TP_FW643_MODE_A J2 MODE_A (IPD) NT-18
TP_FW643_CE L13 CE (IPD)
TP_FW643_FW620_L D12 FW620* (IPU)
TP_FW643_JASI_EN D1 JASI_EN (IPD) NT-11
TP_FW643_AVREG A10 AVREG
TP_FW643_VBUF H13 VBUF
FW643_PU_RST_L K13 FW_RESET* (IPU) NT-8
TP_FW643_OCR10_CTL J12 OCR_CTL_V10
NC J13 OCR_CTL_V12 (Reserved)

VSS VREG_VSS

PCIE_RXD0N N8 PCIE_FW_R2D_N
PCIE_RXD0P N7 PCIE_FW_R2D_P
PCIE_TXD0N N5 PCIE_FW_D2R_C_N
PCIE_TXD0P N6 PCIE_FW_D2R_C_P
C4170 0.1UF 10% 16V X5R 402-1 PCIE_FW_R2D_C_N PLACE_NEAR=U1800.AV34:2.54mm
C4171 0.1UF 10% 16V X5R 402-1 PCIE_FW_R2D_C_P PLACE_NEAR=U1800.AU34:2.54mm
C4175 0.1UF 10% 16V X5R 402-1 PCIE_FW_D2R_N PLACE_NEAR=U1800.BG36:2.54mm
C4176 0.1UF 10% 16V X5R 402-1 PCIE_FW_D2R_P PLACE_NEAR=U1800.BJ36:2.54mm
REFCLKN N9 PCIE_CLK100M_FW_N
REFCLKP N10 PCIE_CLK100M_FW_P

PCI EXPRESS PHY
TEST CONTROLLER
1394 PHY
POWER MANAGEMENT
FIXME!!! - TYPO IN SYMBOL REGCTL
SCIF
SERIAL EEPROM CONTROLLER
MISCELLANEOUS
CHIP RESET

NT-4 (IPU) TCK M4 TP_FW643_TCK
NT-3 (IPU) TDI N2 NC_FW643_TDI
(IPU) TDO M1 TP_FW643_TDO
NT-1 (IPU) TMS M3 TP_FW643_TMS
NT-2 (IPU) TRST* N1 FW643_TRST_L
NT-10 (IPD) WAKE* C2 FW643_WAKE_L
REGCLT D13 FW643_REGCTL
VAUX_DETECT E1 FW643_VAUX_DETECT
NT-12 (IPD) VAUX_DISABLE D2 TP_FW643_VAUX_ENABLE
NT-13 (OD) CLKREQN L2 FW_CLKREQ_PHY_L
NT-16 (IPD) SCIFCLK G2 TP_FW643_SCIFCLK
NT-14 (IPD) SCIFDAIN G1 TP_FW643_SCIFDAIN
NT-17 SCIFDOUT H1 TP_FW643_SCIFDOUT
NT-15 (IPD) SCIFMC F2 TP_FW643_SCIFMC
NT-7 SCL N12 FW643_SCL
NT-6 SDA M11 TP_FW643_SDA
NT-5 PERST* N4 FW_RESET_L

PP3V3_FW_FWPHY
FW643_LDO
R4165 10K 5% 1/16W MF-LF 402
R4166 10K 5% 1/16W MF-LF 402
R4164 10K 5% 1/16W MF-LF 402
R4163 10K 5% 1/16W MF-LF 402

SYNC_MASTER=K91_MLB SYNC_DATE=10/20/2010
PAGE TITLE
FireWire LLC/PHY (FW643)
Apple Inc.
DRAWING NUMBER D
REVISION
BRANCH
PAGE 41 OF 132
SHEET 38 OF 105

Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (FW VP FET Input)
- =PPBUS_FW_FET (FW VP FET Output)
- =PP3V3_FW_P3V3FWFET (3.3V FET Input)
- =PP3V3_FW_FET (3.3V FET Output)
- =PP3V3_FW_FWPHY (PHY 3.3V Power)
- =PP3V3_S0_FWLATEVG
- =PP3V3_S0_FWPWRCTL
- =PP1V05_S0_FWPWRCTL (5KPD Bias Rail)
- =PP1V05_FW_P1V0FWFET (1.0V FET Input)
- =PP1V0_FW_FET_R (1.0V FET Output)
- =PP1V0_FW_FWPHY (PHY 1.0V)

Signal aliases required by this page:
- =FW_CLKREQ_L
- =FW_PME_L

BOM options provided by this page:
(NONE)

FireWire Port Power Switch

PPBUS_G3H

Q4262 provides for fast-off of Q4260 in S0 (Late-VG detection)

CRITICAL Q4260 FDC638P_G SM

PPBUS_FW_FWPWRSW_F — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=12.6V

CRITICAL F4260 1.1A-24V MINISMDC110H24

PPBUS_FW_FWPWRSW_D — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=12.6V

CRITICAL D4260 SM CRS08-1.5A-30V

PPVP_FW

R4262 10K 5% 1/10W MF-LF 402

FWPORT_FASTOFF_L_DIV

CRITICAL Q4262 BSS8402DW SOT-363 (SYM-VER1)

R4263 10 5% 1/10W MF-LF 402

FWPORT_FASTOFF_L

R4260 300K 5% 1/16W MF-LF 402

C4260 0.1UF 10% 16V X5R 402

FWPORT_PWREN_L_DIV

R4261 470K 5% 1/16W MF-LF 402

PP3V3_S0

CRITICAL Q4262 BSS8402DW SOT-363 (SYM-VER1)

FWPORT_PWREN_L

CRITICAL Q4261 SSM3K15FV SOD-VESM-HF

NO STUFF C4261 0.1UF 10% 25V X5R 402

IN FWPORT_PWR_EN

Supervisor & CLKREQ# Isolation

PP3V3_S0

C4290 0.1UF 10% 16V X5R 402

CRITICAL U4290 SLG4AP016V TDFN

R4290 100K 5% 1/16W MF-LF 402

PP3V3_FW_FWPHY

IN PLT_RESET_L

R4283 10K 5% 1/16W MF-LF 402

SENSE 0.7V

PP1V0_FW_FWPHY

DLY

RESET*

FW_RESET_L

DLY = 60 ms +/- 20%

FW_RESET_R_L

MR*

IN FW_PWR_EN

IN FW_CLKREQ_L

EN

OUT (OD)

IN

FW_CLKREQ_PHY_L

FW_CLKREQ_PHY_L MAKE_BASE=TRUE

GND

THRM PAD

Pull-up provided by another page.

FireWire Port 5K Pull-Down Detect

All FireWire devices require 5K pull-down on TPB pair.
Host can detect as load on TPBIAS signal.
Current source only active when FW_PWR_EN is low.

PP1V05_S0

R4275 1K 5% 1/16W MF-LF 402

FW_PWR_EN_L

IN FW_PWR_EN

CRITICAL Q4275 DMB53D0UV SOT-563

R4270 330K 5% 1/16W MF-LF 402

R4271 56K 5% 1/16W MF-LF 402

FW_5KPD_DET_L MAKE_BASE=TRUE

FW_5KPD_DET_RC

CRITICAL Q4275 DMB53D0UV SOT-563

CRITICAL Q4270 BC847CDXV6TXG SOT563

FWDET_MIRROR

CRITICAL Q4270 BC847CDXV6TXG SOT563

C4270 0.1UF 10% 16V X5R 402

FW_P1_TPBIAS_R

FWDET_EMIT

R4272 1K 5% 1/16W MF-LF 402

R4273 12K 5% 1/16W MF-LF 402

PLACE_NEAR=C4360.1:2 mm

OUT FW_P1_TPBIAS

FireWire PHY WAKE# Support

When PHY is powered, FW_5KPD_DET_L acts as legacy PME# signal.

PP3V3_FW_FWPHY

R4277 10K 5% 1/16W MF-LF 402

R4276 100K 5% 1/16W MF-LF 402

FW_WAKE

NO STUFF C4276 0.1UF 10% 16V X5R 402

Dual-purpose output:
1) 5K Pull-down Detect when FW_PWR_EN is low.
2) FW643 WAKE# (PME#) when PHY is powered.

OUT FW_PLUG_DET_L

Pull-up provided on another page.

CRITICAL Q4276 DMB53D0UV SOT-563

IN FW643_WAKE_L — FW643_WAKE_L MAKE_BASE=TRUE

CRITICAL Q4276 DMB53D0UV SOT-563

3.3V FW Switch

PP3V3_S0

U4201 TPS22924 CSP

C4201 1UF 10% 6.3V CERM 402

CRITICAL

PP3V3_FW_FWPHY

Max Current = 1.7A (85C)

U4201 & U4202

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

1.0V FW Switch

PP1V05_S0

U4202 TPS22924 CSP

C4202 1UF 10% 6.3V CERM 402

CRITICAL

PP1V05_FW_FET — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.05V

R4202 0.549 1% 1/16W MF 402

PP1V0_FW_FWPHY

LSI FireWire PHY requires 1.0V.
To avoid an extra power supply,
1.05V is used with a series R
to reduce voltage.

SYNC_MASTER=K91_MLB SYNC_DATE=10/20/2010

PAGE TITLE: FireWire Port & PHY Power

Apple Inc.

DRAWING NUMBER: — SIZE: D
REVISION:
BRANCH:
PAGE: 42 OF 132
SHEET: 39 OF 105

Page Notes

Power aliases required by this page:
- =PPVP_FW_PORT1
- =PPVP_FW_PHY_CPS_FET (From Port)
- =PPVP_FW_PHY_CPS (To PHY)
- =PP3V3_FW_FWPHY
- =PP3V3_S0_FWLATEVG

Signal aliases required by this page:
- =FW_PHY_DS0
- =FW_PHY_DS1
- =FW_PHY_DS2

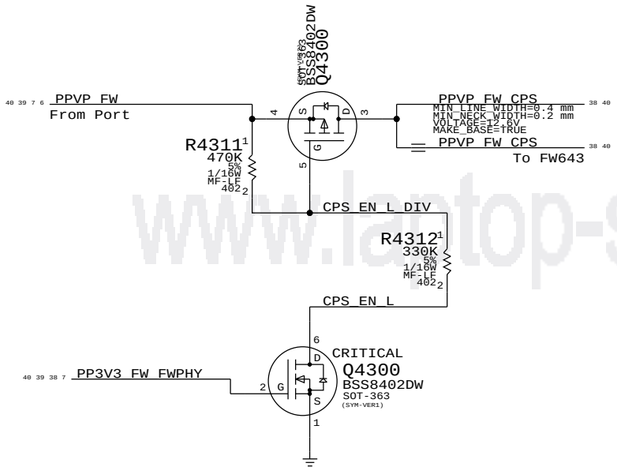
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

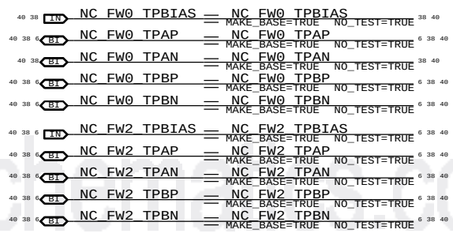
FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VDD33.
FET blocks current to TPCPS until VDD33 is powered.



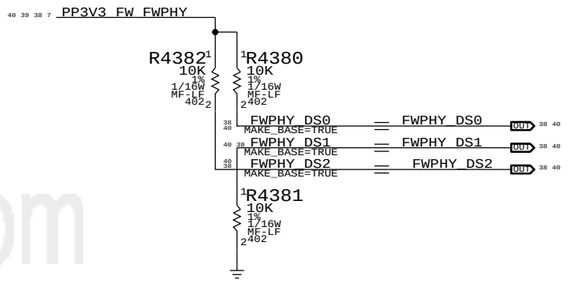
Unused FireWire Ports

Disabled per LSI instructions
(All unused port signals TP/NC)



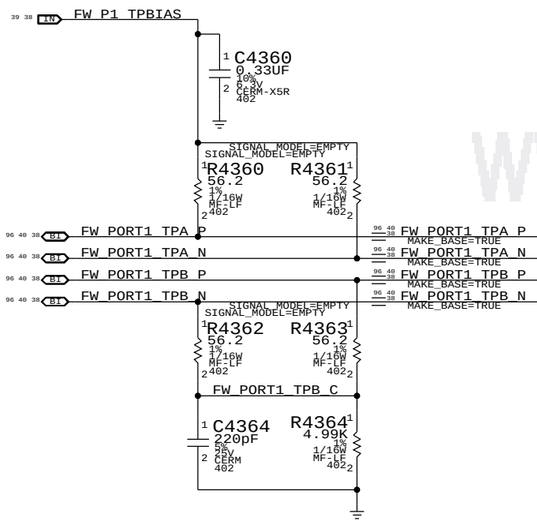
FireWire PHY Config Straps

Configures PHY for:
- Port "1" Bilingual (1394B)

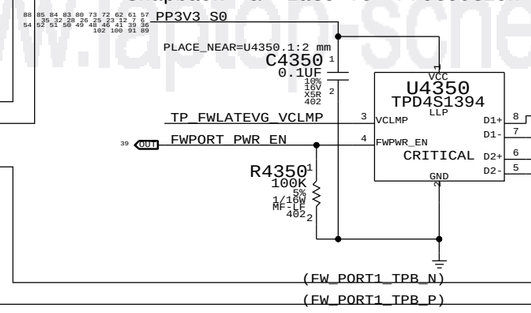


Termination

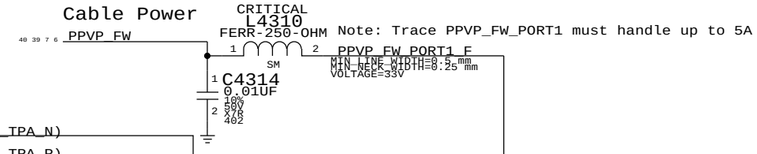
Place close to FireWire PHY



"Snapback" & "Late VG" Protection



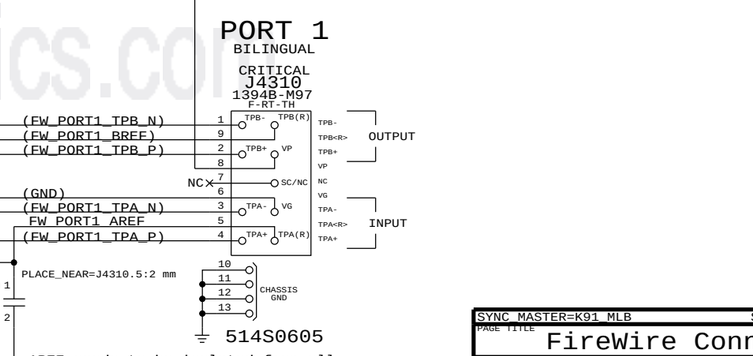
Cable Power



Note: Trace PPVP_FW_PORT1 must handle up to 5A

PORT 1

BILINGUAL



514S0605

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

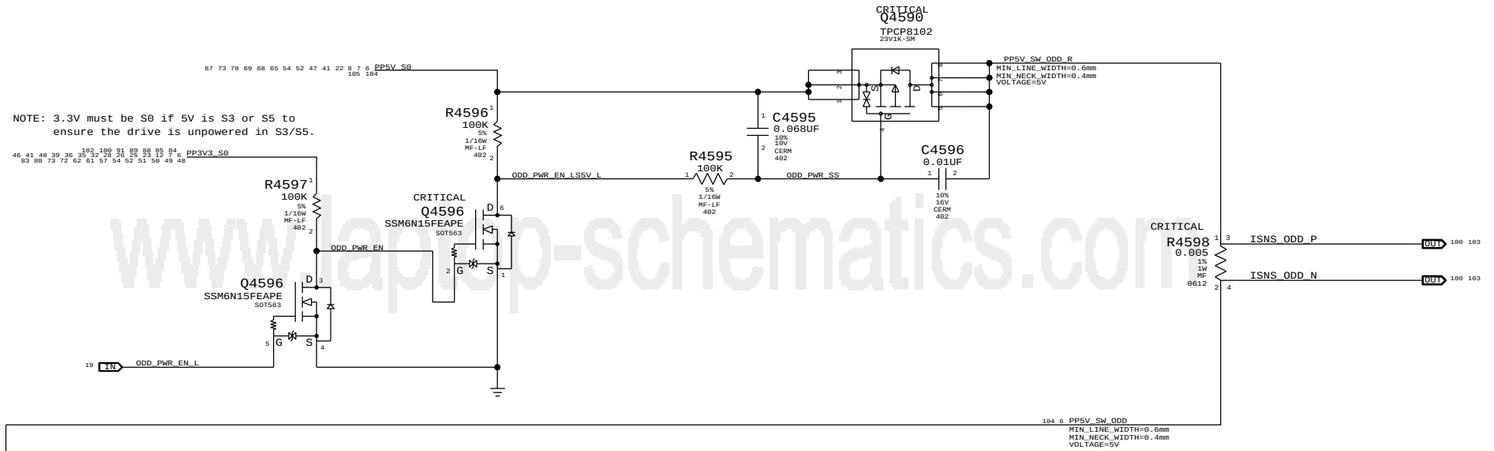
SYNC_MASTER=K91_MLB SYNC_DATE=07/22/2010

PAGE TITLE: FireWire Connector

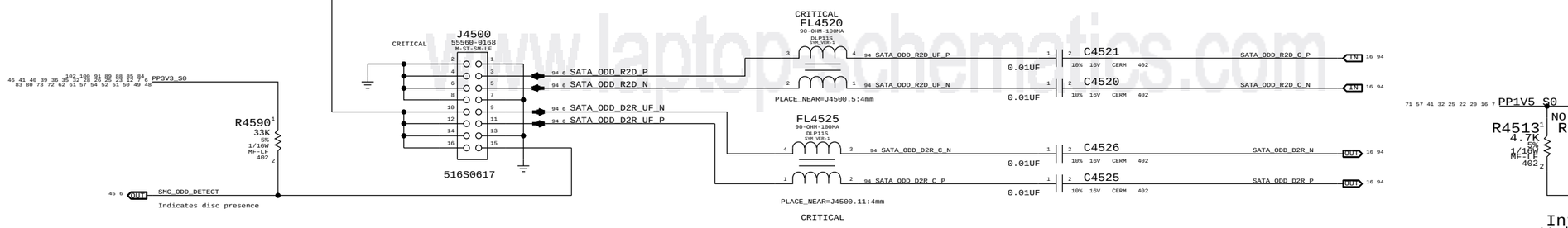
Apple Inc.

DRAWING NUMBER: D
REVISION:
BRANCH:
PAGE: 43 OF 132
SHEET: 40 OF 105

ODD Power Control



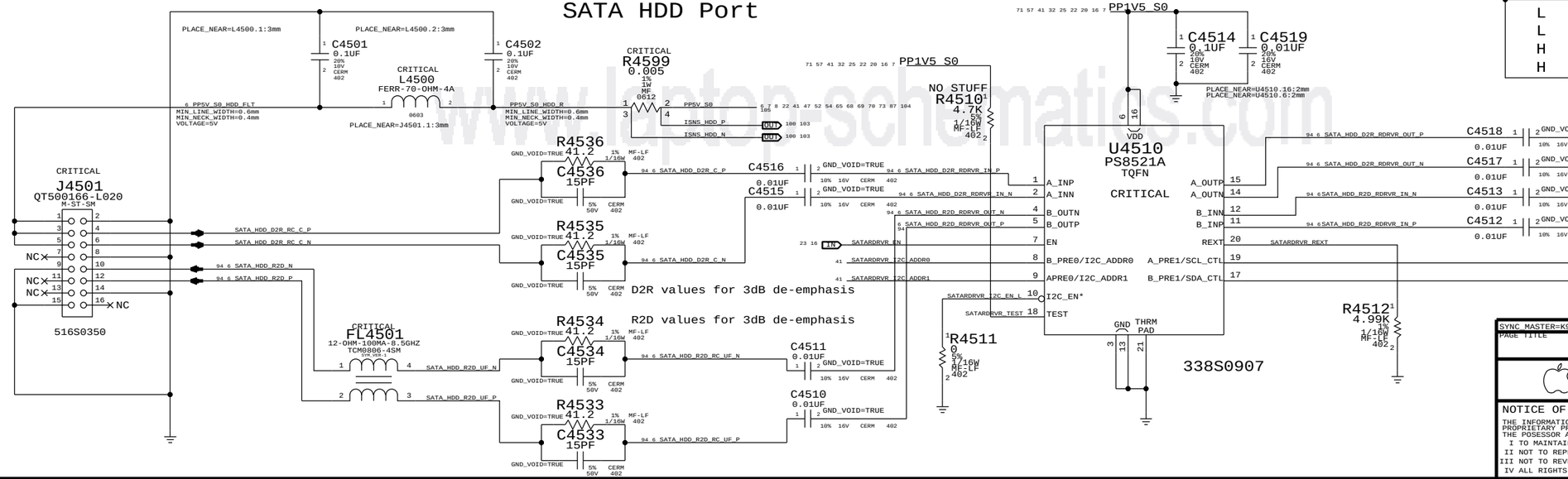
SATA ODD Port



Internally PD ~150K
Write:0xB6 Read:0xB7

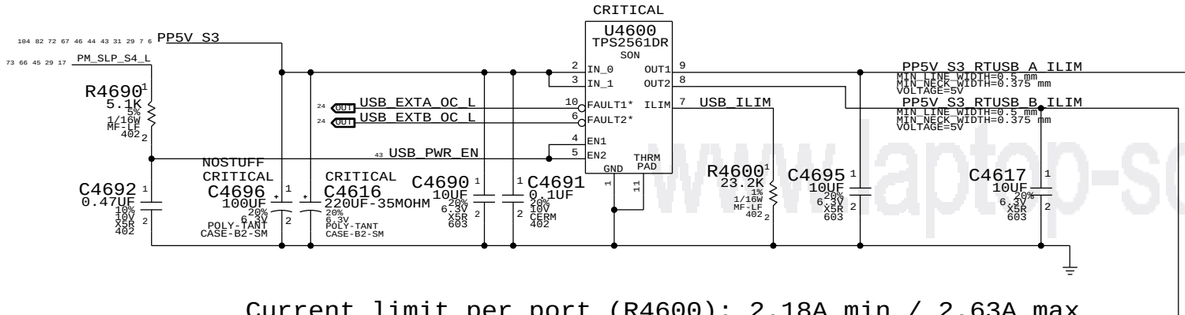
ADDR1	ADDR0	Address (R/W)
L	L	0x96/0x97
L	H	0x98/0x99
H	L	0xB6/0xB7
H	H	0xB8/0xB9

SATA HDD Port



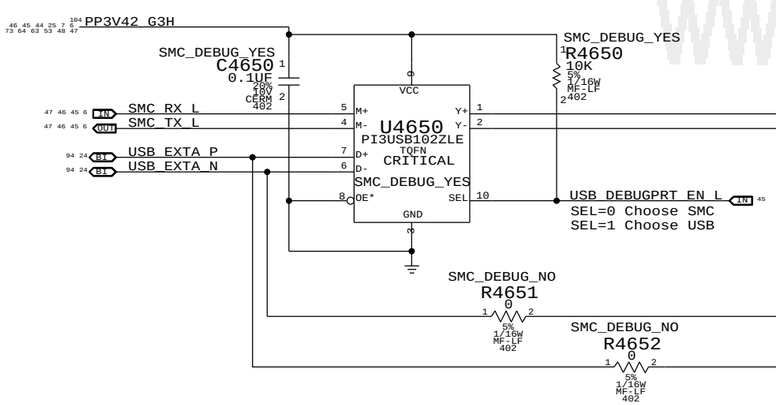
SYNC_MASTER=K92_ERIC	SYNC_DATE=11/08/2010
PAGE TITLE	SATA Connectors
Apple Inc.	DRAWING NUMBER: SIZE D
	REVISION:
	BRANCH:
	PAGE: 45 OF 132
	SHEET: 41 OF 105

USB Port Power Switch

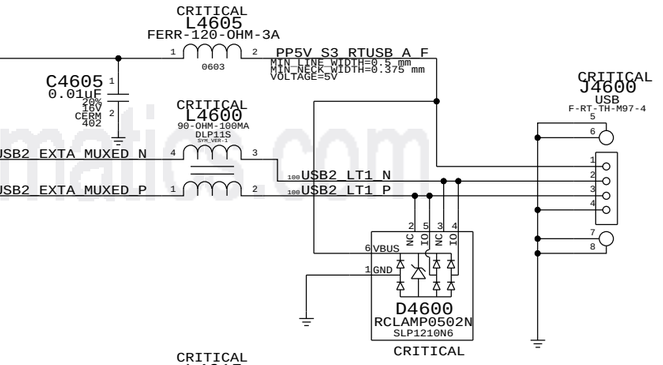


Current limit per port (R4600): 2.18A min / 2.63A max

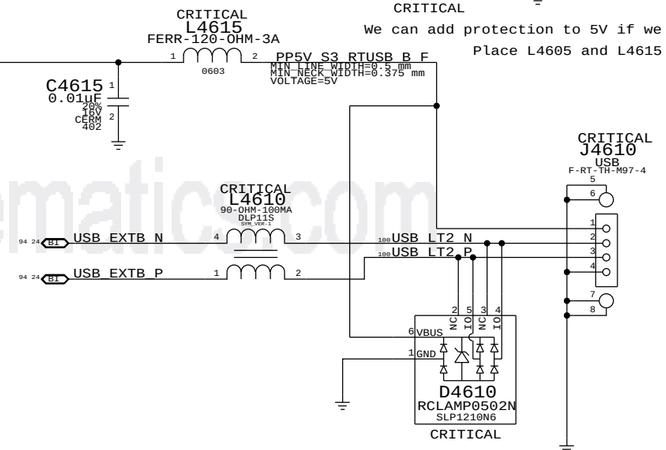
USB/SMC Debug Mux



Left USB Port A



We can add protection to 5V if we want, but leaving NC for now
Place L4605 and L4615 at connector pin



Left USB Port B

SYNC_MASTER=K92_ERIC SYNC_DATE=08/24/2010

PAGE TITLE: External USB Connectors

Apple Inc.

DRAWING NUMBER | SIZE: D

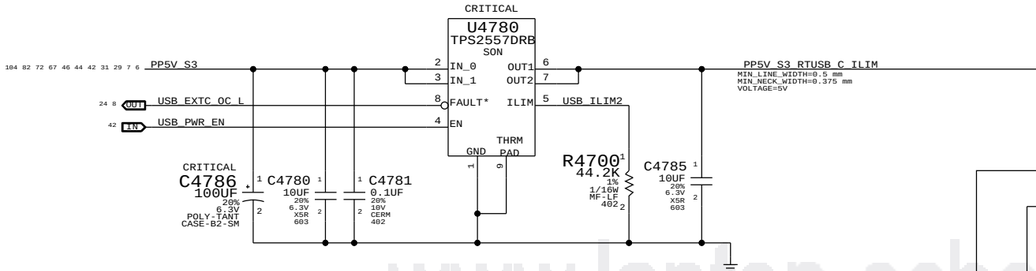
REVISION

BRANCH

PAGE: 46 OF 132

SHEET: 42 OF 105

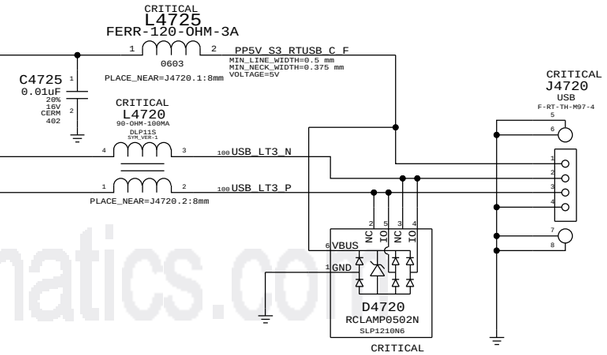
USB Port Power Switch



Current limit (R4700): 2.19A min / 2.76A max

94 24 B7 USB_EXTC_N
94 24 B7 USB_EXTC_P

LEFT USB PORT C



SYNC_MASTER=K92_ERIC SYNC_DATE=07/22/2010

PAGE TITLE

PROJECT SPECIFIC CONNS

Apple Inc.

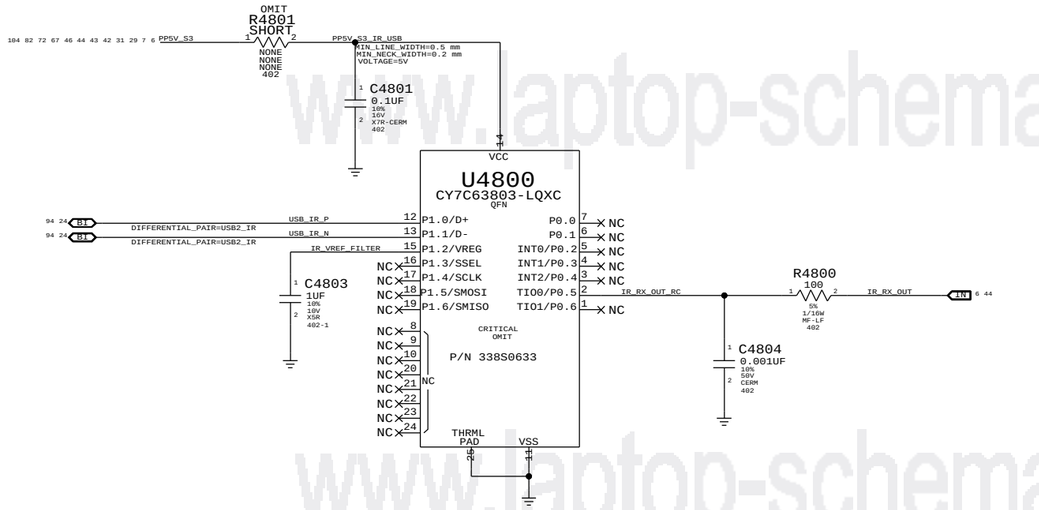
DRAWING NUMBER | SIZE D

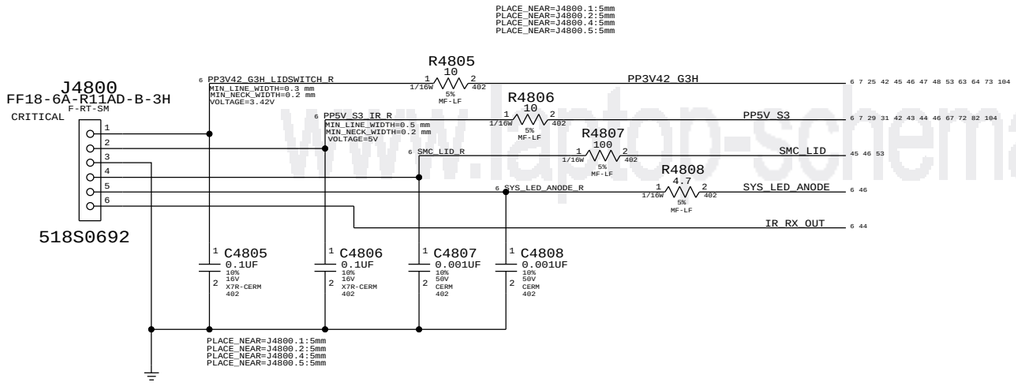
REVISION

BRANCH

PAGE 47 OF 132

SHEET 43 OF 105





SYNC_MASTER=K17_MLB SYNC_DATE=04/26/2010

PAGE TITLE

Front Flex Support

Apple Inc.

DRAWING NUMBER

SIZE D

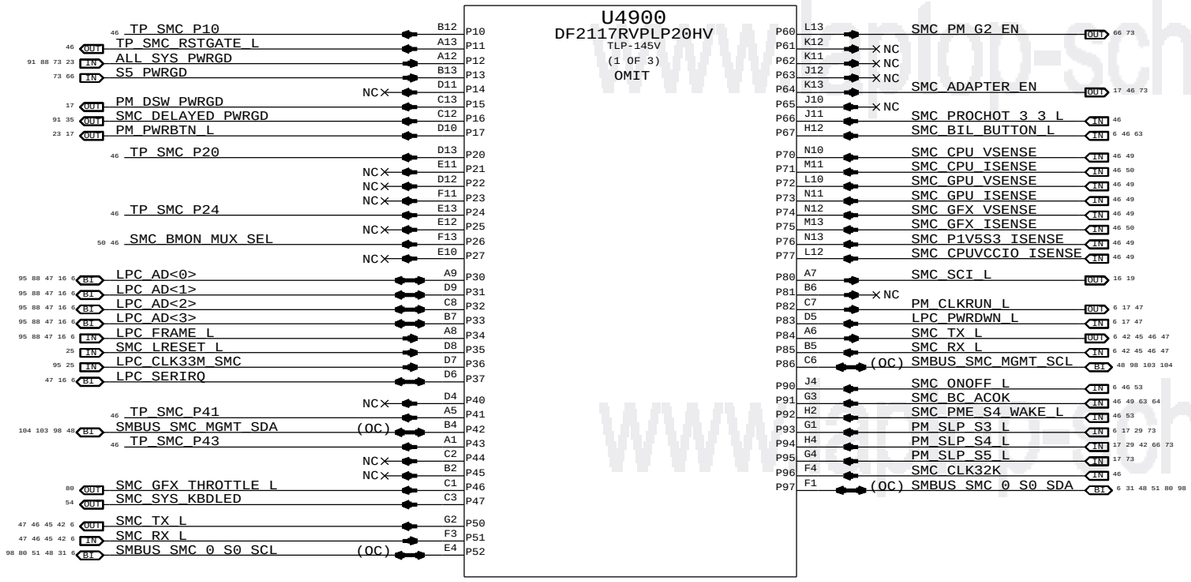
REVISION

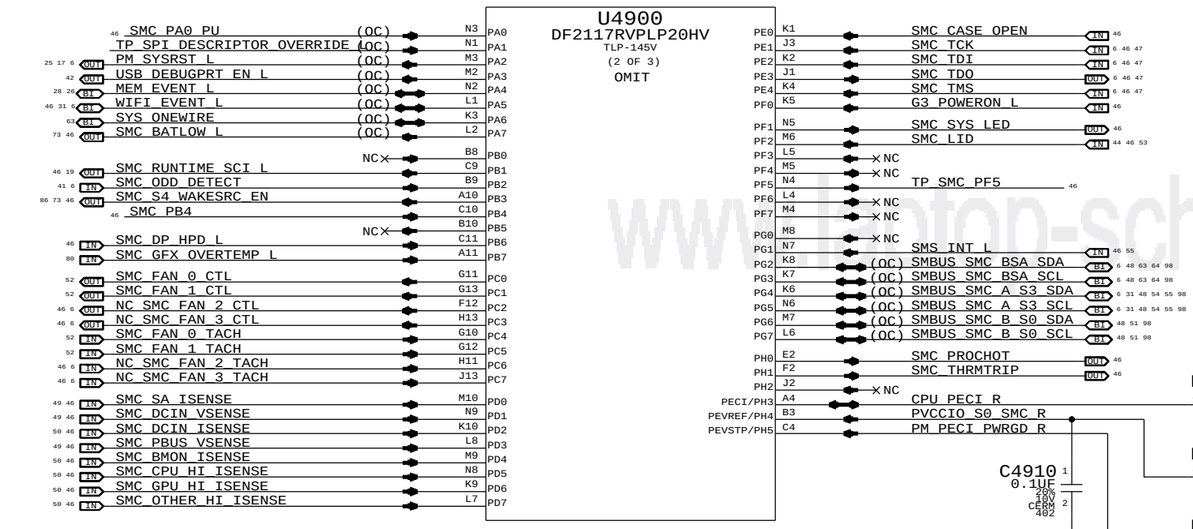
BRANCH

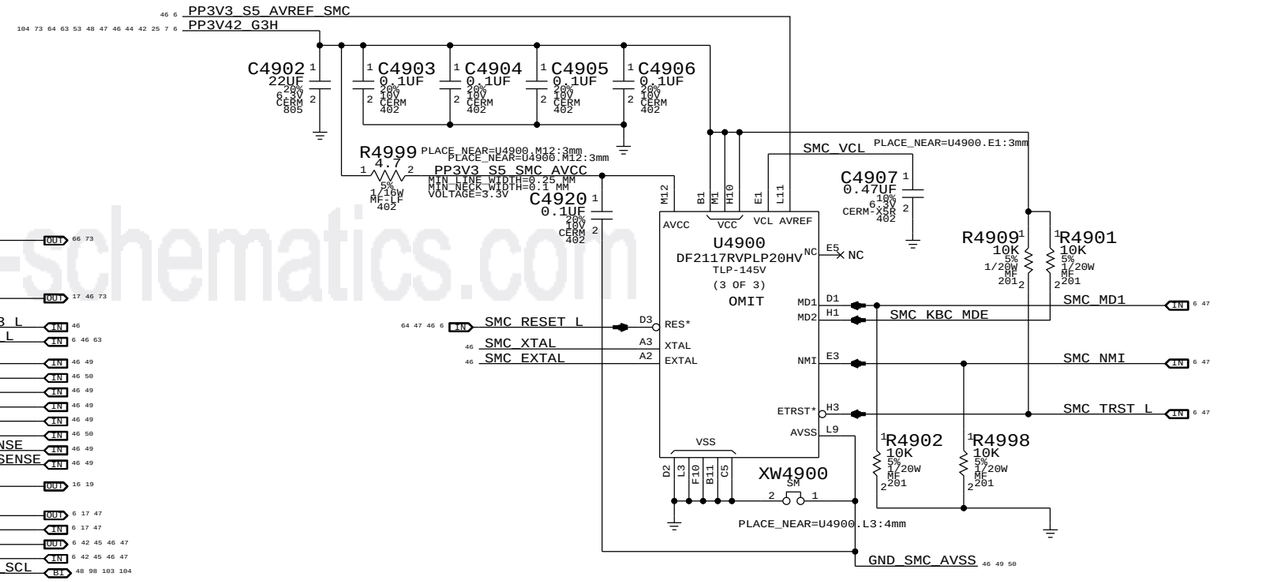
PAGE 48 OF 132

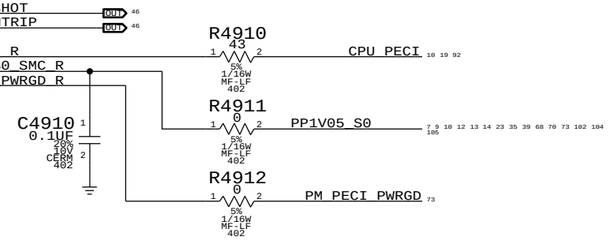
SHEET 44 OF 105

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.









NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC_MASTER=K91_BEN SYNC_DATE=07/12/2010

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER | SIZE: D

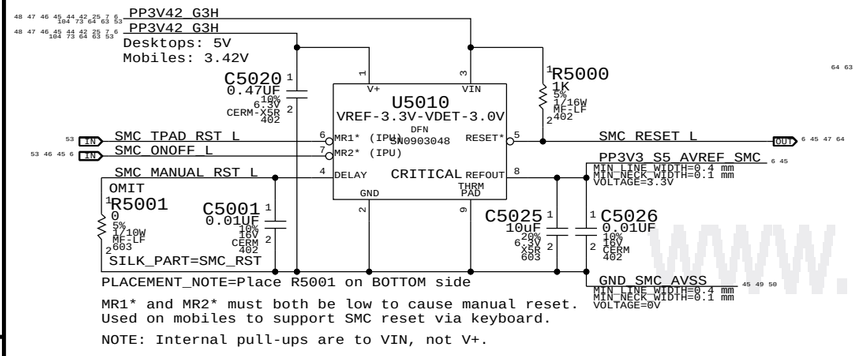
REVISION

BRANCH

PAGE: 49 OF 132

SHEET: 45 OF 105

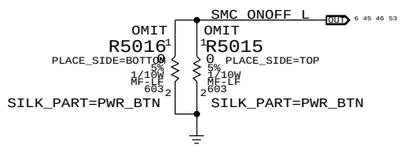
SMC Reset "Button", Supervisor & AVREF Supply



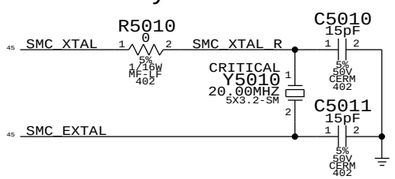
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

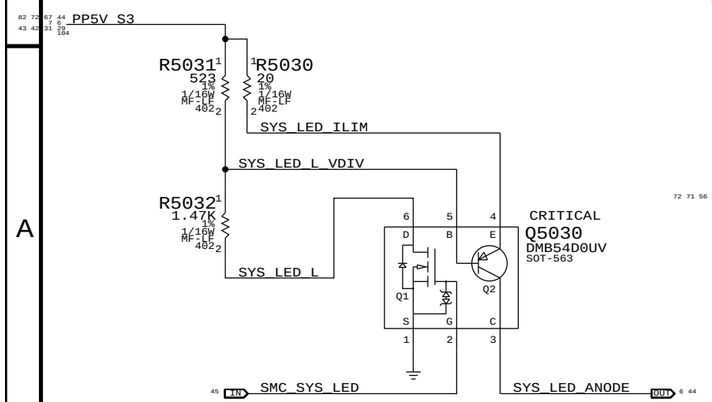
Debug Power "Buttons"



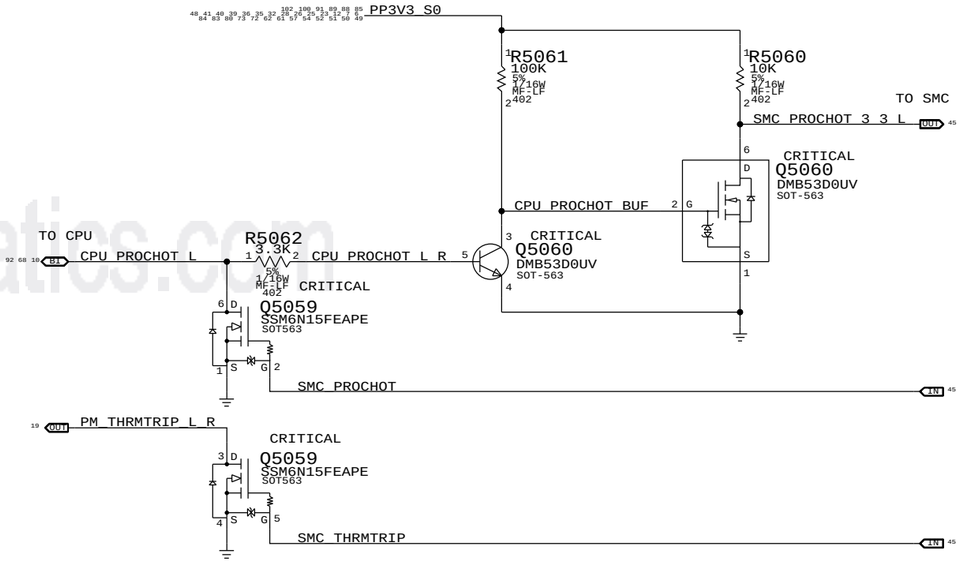
SMC Crystal Circuit



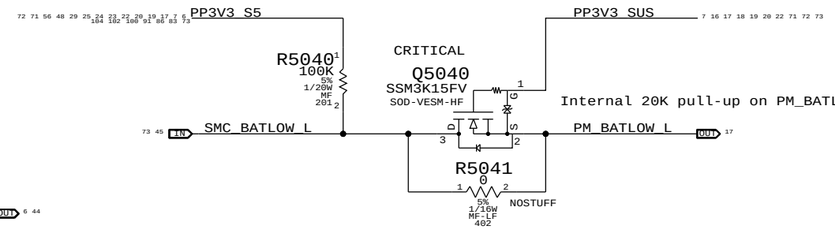
System (Sleep) LED Circuit

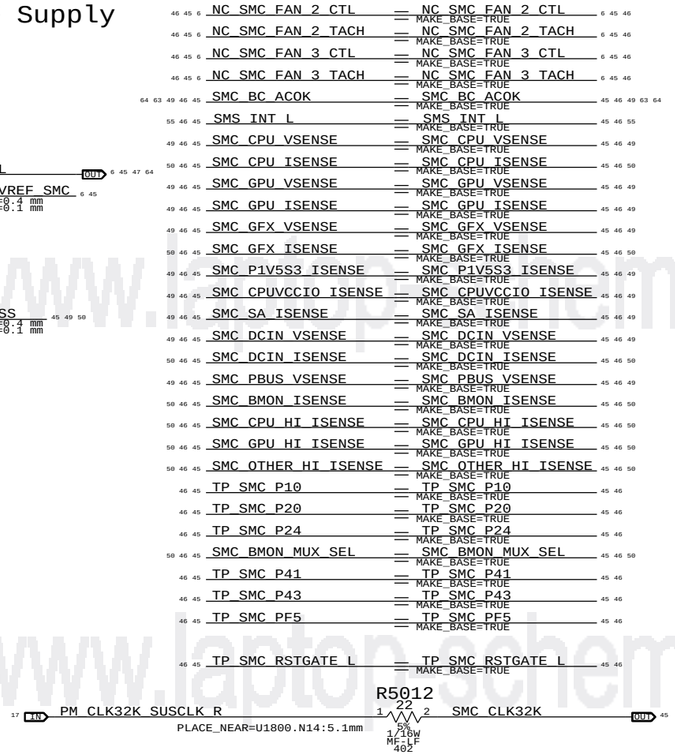


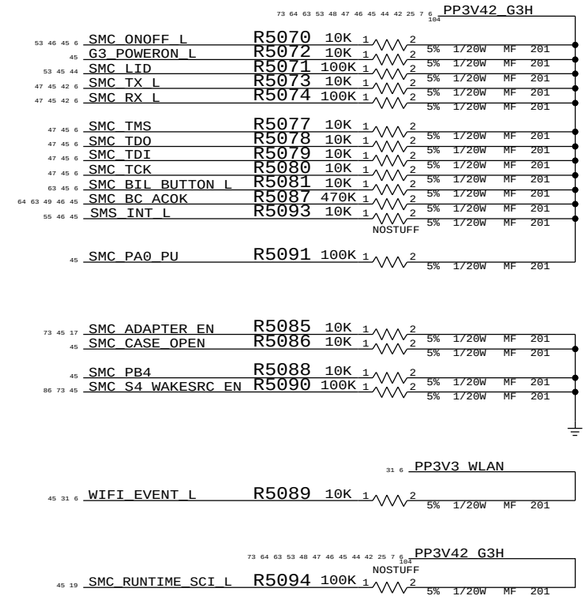
SMC FSB to 3.3V Level Shifting



BATLOW# Isolation







SYNC_MASTER=K91_BEN SYNC_DATE=07/12/2010

PAGE TITLE: SMC Support

Apple Inc.

DRAWING NUMBER: SIZE D

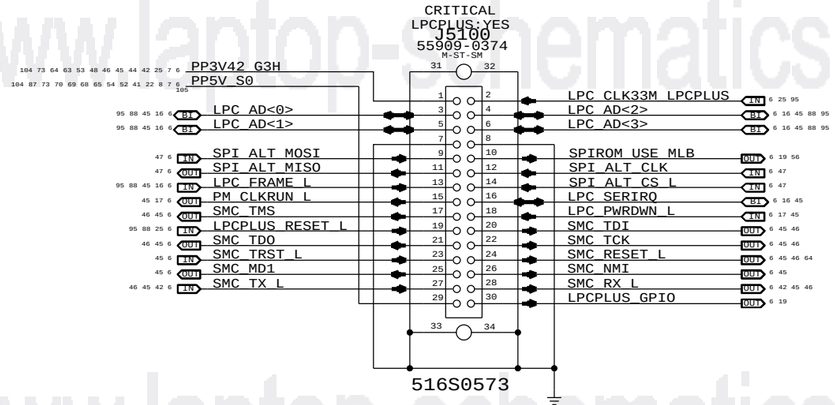
REVISION:

BRANCH:

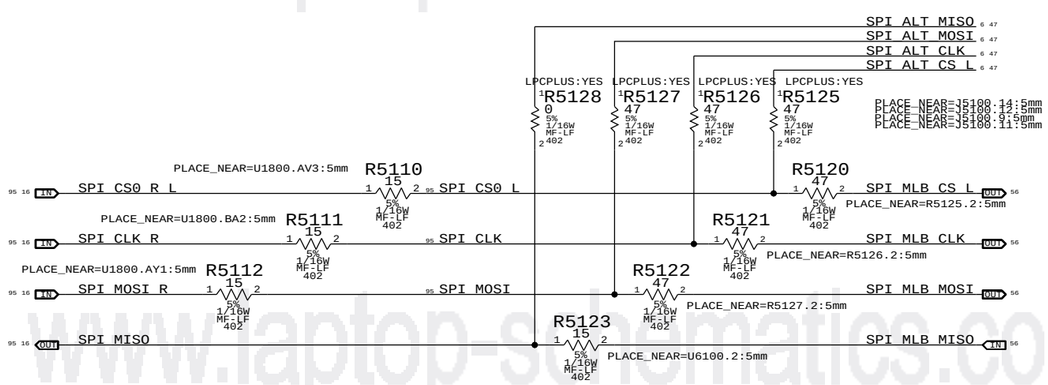
PAGE: 50 OF 132

SHEET: 46 OF 105

LPC+SPI Connector



SPI Bus Series Termination



SYNC_MASTER=K91_YUN SYNC_DATE=09/23/2010

PAGE TITLE: LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER | SIZE D

REVISION

BRANCH

PAGE 51 OF 132

SHEET 47 OF 105

PCH SMBus "0" Connections

PP3V3_S0

PCH — U1800 (MASTER)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

R5200 1K 5% 1/16W MF-LF 402 — R5201 1K 5% 1/16W MF-LF 402

SO-DIMM "A" — J2900 (Write: 0xA0 Read: 0xA1)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

VRef DACs — U2900 (Write: 0x98 Read: 0x99)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

SO-DIMM "B" — J3100 (Write: 0xA4 Read: 0xA5)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

Margin Control — U2901 (Write: 0x30 Read: 0x31)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

SATA Redriver — U4510 (Write: 0xB6 Read: 0xB7)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

XDP Connectors — J2600 & J2650 (MASTER)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

ExpressCard Slot — J3500 (Address via ARP)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

LED BACKLIGHT — U9701 (WRITE: 0x58 READ: 0x59)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

Mikey — U6800 (Write: 0x72 Read: 0x73)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

SDRVI2C:SB
R5237 0 5% 1/16W MF-LF 402

SDRVI2C:SB
R5236 0 5% 1/16W MF-LF 402

DP SDRV "A" — U9310 (Write: 0x94 Read: 0x95)
- I2C_DPSDRVA_SCL
- I2C_DPSDRVA_SDA

PCH "SMLink 0" Connections

PP3V3_S0

R5210 8.2K 5% 1/16W MF-LF 402 — R5211 8.2K 5% 1/16W MF-LF 402

PCH — U1800 (MASTER)
- SML_PCH_0_CLK
- SML_PCH_0_DATA

PCH "SMLink 1" Connections

PP3V3_S0

NO STUFF R5220 8.2K 5% 1/16W MF-LF 402 — NO STUFF R5221 8.2K 5% 1/16W MF-LF 402

R5223 0 5% 1/16W MF-LF 402

R5222 0 5% 1/16W MF-LF 402

PCH — U1800 (Write: 0x88 Read: 0x89)
- SML_PCH_1_CLK
- SML_PCH_1_DATA

SMLink 1 is slave port to access PCH & CPU via PECI.

SMC "0" SMBus Connections

PP3V3_S0

SMC — U4900 (MASTER)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA

R5250 4.7K 5% 1/16W MF-LF 402 — R5251 4.7K 5% 1/16W MF-LF 402

GPU Temp (Ext) — EMC1414: U5550 (Write: 0x98 Read: 0x99)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA

GPU Temp (Int) — Whistler: U8000 (Write: 0x82 Read: 0x83)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA

X19 Temp — J3401 (Write: 0x90 Read: 0x91)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA

SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state

PP3V3_S3

SMC — U4900 (MASTER)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

R5270 1K 5% 1/16W MF-LF 402 — R5271 1K 5% 1/16W MF-LF 402

Trackpad — J5800 (Write: 0x90 Read: 0x91)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

J3401 ALS (Write: 0x72 Read: 0x73)
Lid Angle detect, SMS (Write: 0x32 Read: 0x33)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

SMS — U5920 (Write: 0x30 Read: 0x31)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

SMC "B" SMBus Connections

PP3V3_S0

SMC — U4900 (MASTER)
- SMBUS_SMC_B_S0_SCL
- SMBUS_SMC_B_S0_SDA

R5260 4.7K 5% 1/16W MF-LF 402 — R5261 4.7K 5% 1/16W MF-LF 402

CPU Temp — EMC1414: U5570 (Write: 0x98 Read: 0x99)
- SMBUS_SMC_B_S0_SCL
- SMBUS_SMC_B_S0_SDA

T29 Temp — EMC1412: U5520 (Write: 0x90 Read: 0x91)
- SMBUS_SMC_B_S0_SCL
- SMBUS_SMC_B_S0_SDA

SMC "Battery A" SMBus Connections

PP3V42_G3H

SMC — U4900 (MASTER)
- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA

R5280 2.0K 5% 1/16W MF-LF 402 — R5281 2.0K 5% 1/16W MF-LF 402

Battery Charger — ISL6258 - U7000 (Write: 0x12 Read: 0x13)
- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA

Battery — J6955 (See Table)
- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA

Battery

Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x92 Read: 0x93)

SMC "Management" SMBus Connections

The bus formerly known as "Battery B"

PP3V3_S5

SMC — U4900 (MASTER)
- SMBUS_SMC_MGMT_SCL
- SMBUS_SMC_MGMT_SDA

R5290 4.7K 5% 1/16W MF-LF 402 — R5291 4.7K 5% 1/16W MF-LF 402

Sensor ADC A — UD100 (Write: 0x10 Read: 0x11)
- SMBUS_SMC_MGMT_SCL
- SMBUS_SMC_MGMT_SDA

Sensor ADC B — UD210 (Write: 0x32 Read: 0x33)
- SMBUS_SMC_MGMT_SCL
- SMBUS_SMC_MGMT_SDA

T29 SMBus Connections

PP3V3_S0

T29 — U3600 (MASTER)
- I2C_T29_SCL
- I2C_T29_SDA

R5230 4.7K 5% 1/16W MF-LF 402 — R5231 4.7K 5% 1/16W MF-LF 402

T29 PortA MCU — U9330 (Write: 0x26 Read: 0x27)
- I2C_T29_SCL
- I2C_T29_SDA

SDRVI2C:MCU
R5234 0 5% 1/16W MF-LF 402

SDRVI2C:MCU
R5235 0 5% 1/16W MF-LF 402

DP SDRV "A" — U9310 (Write: 0x94 Read: 0x95)
- I2C_DPSDRVA_SCL
- I2C_DPSDRVA_SDA

SYNC_MASTER=K17_MLB SYNC_DATE=04/26/2010

PAGE TITLE: K92 SMBus Connections

Apple Inc.

DRAWING NUMBER — SIZE: D

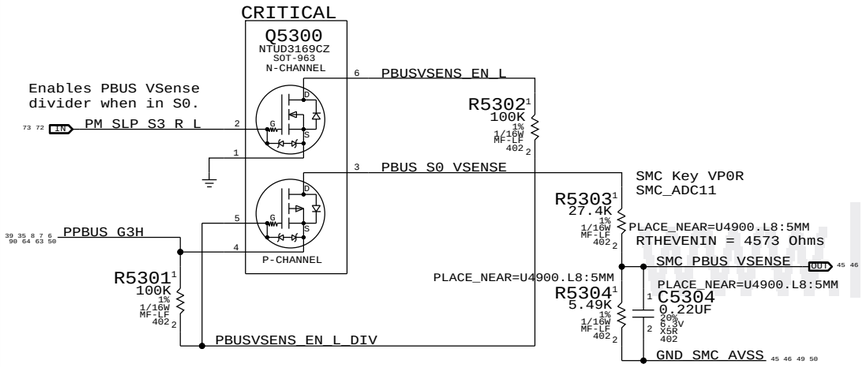
REVISION

BRANCH

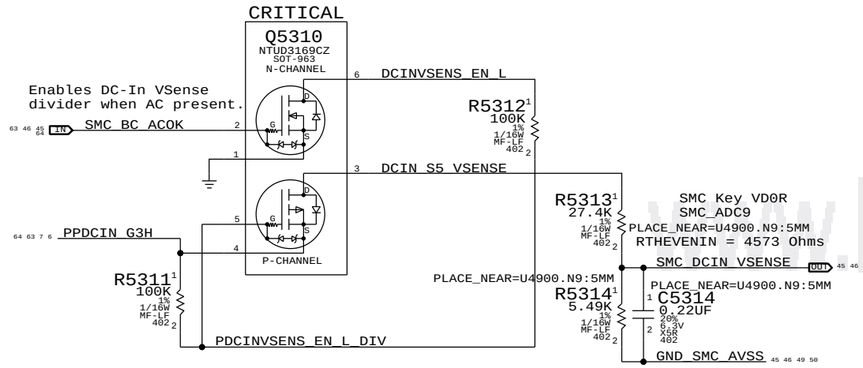
PAGE: 52 OF 132

SHEET: 48 OF 105

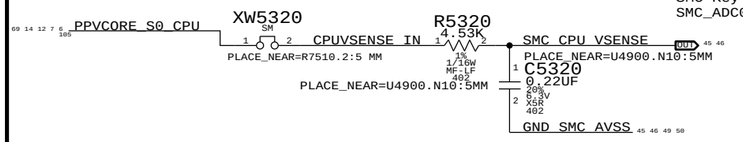
PBUS Voltage Sense Enable & Filter



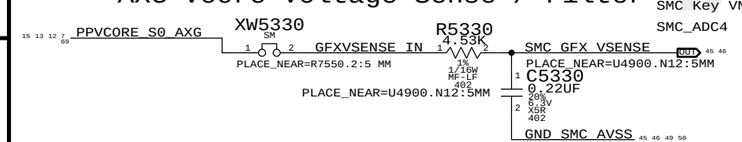
DC-In Voltage Sense Enable & Filter



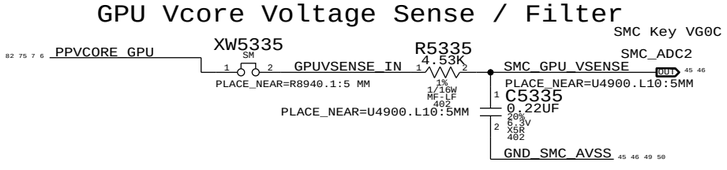
CPU Vcore Voltage Sense / Filter



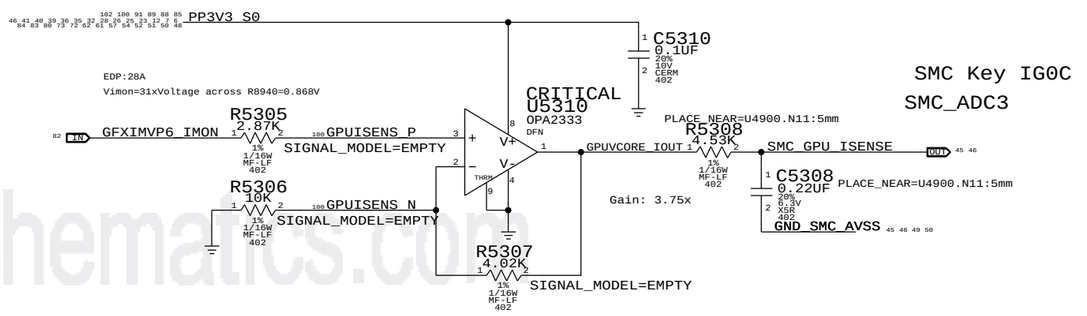
AXG Vcore Voltage Sense / Filter



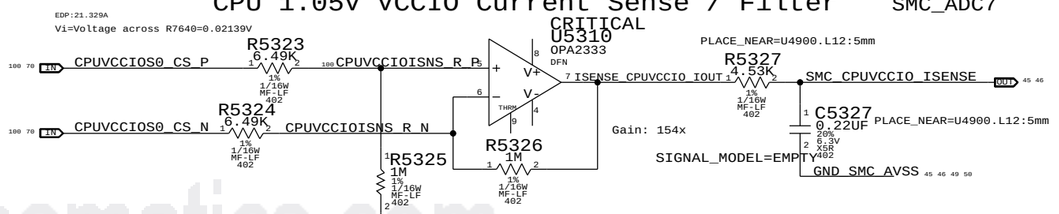
GPU Vcore Voltage Sense / Filter



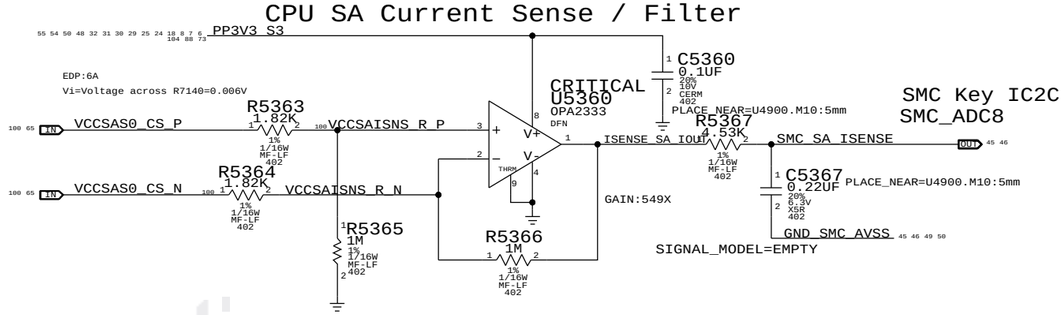
GPU VCore Load Side Current Sense / Filter



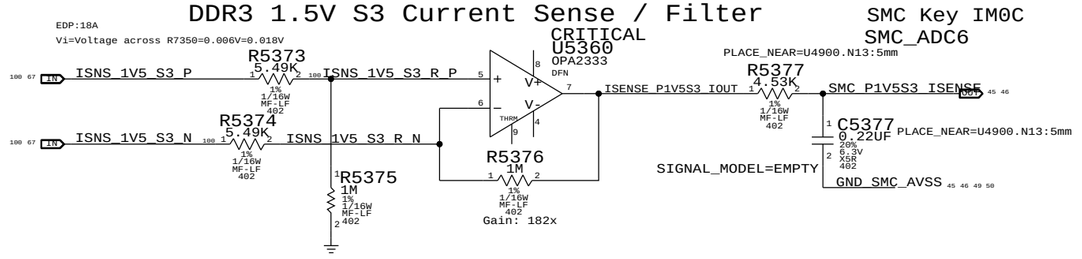
CPU 1.05V VCCIO Current Sense / Filter



CPU SA Current Sense / Filter



DDR3 1.5V S3 Current Sense / Filter



SYNC_MASTER=K92_DINESH SYNC_DATE=09/24/2010

PAGE TITLE: Voltage & Load Side Current Sensing

Apple Inc.

DRAWING NUMBER: SIZE D

REVISION:

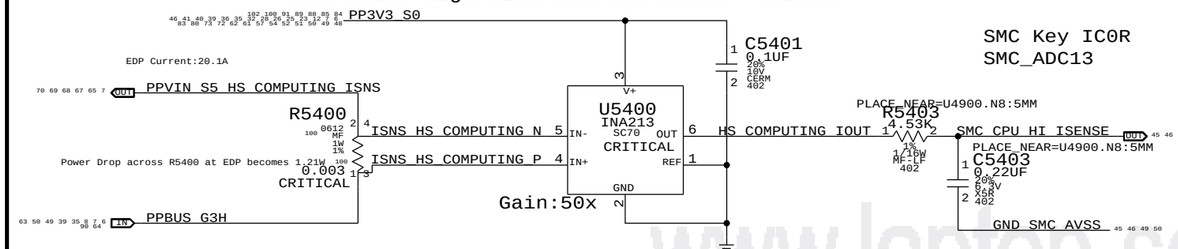
BRANCH:

PAGE: 53 OF 132

SHEET: 49 OF 105

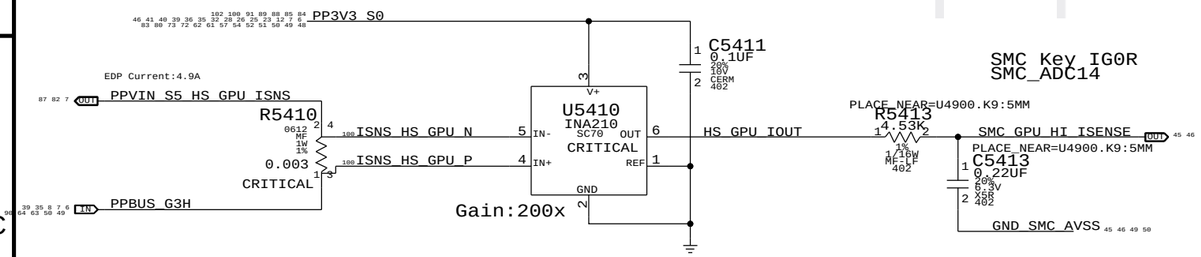
Rsense value and INA gain need to be scrubbed!!

COMPUTING High Side Current Sense / Filter



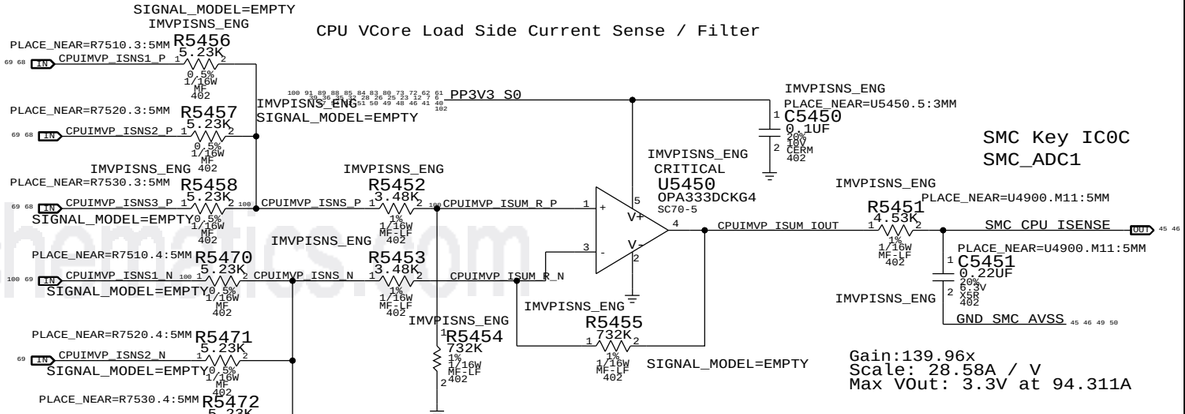
SMC Key IC0R
SMC_ADC13

GRAPHICS High Side Current Sense / Filter



SMC Key IG0R
SMC_ADC14

CPU VCore Load Side Current Sense / Filter

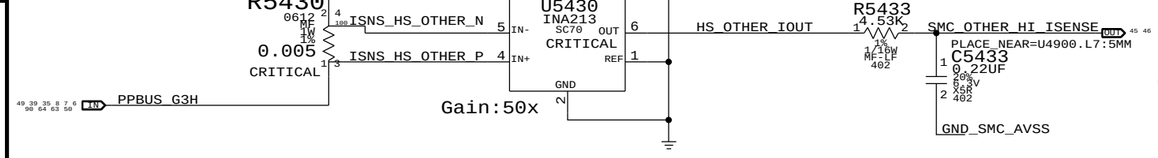


SMC Key IC0C
SMC_ADC1

Gain:139.96x
Scale: 28.58A / V
Max VOut: 3.3V at 94.311A

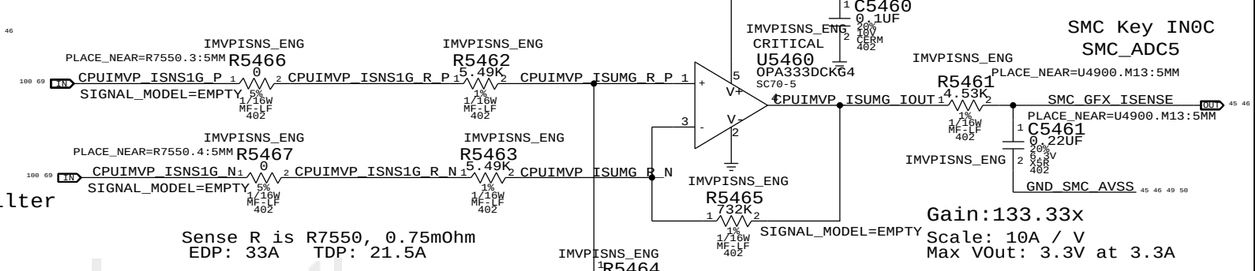
Sense R is R7510, R7520 & R7530
Sense R is 0.75mOhm
EDP: 94A TDP :45A
(Effective Sense R is 0.25mOhm due to summing of the 3 cores)

OTHER High Side Current Sense / Filter



SMC Key IO0R
SMC_ADC15

GFX/IG VCore Load Side Current Sense / Filter

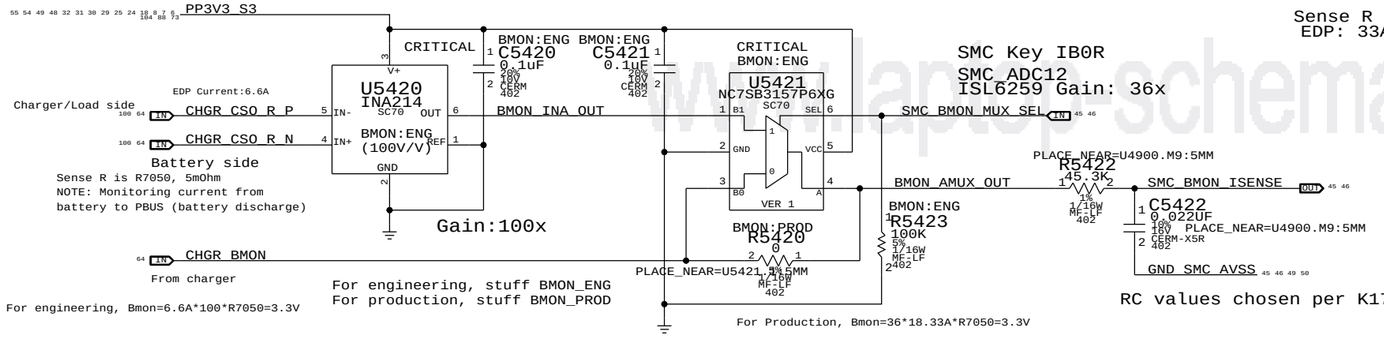


SMC Key IN0C
SMC_ADC5

Gain:133.33x
Scale: 10A / V
Max VOut: 3.3V at 3.3A

Sense R is R7550, 0.75mOhm
EDP: 33A TDP: 21.5A

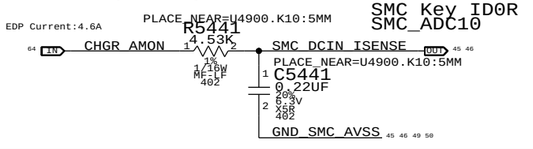
CHARGER BMON High Side (BATTERY DISCHARGE) Current Sense, MUX & Filter



SMC Key IB0R
SMC_ADC12
ISL6259 Gain: 36x

RC values chosen per K17 Radar 7337775

DC-IN (AMON) Current Sense Filter



SMC Key ID0R
SMC_ADC10

SYNC_MASTER=K92_DINESH SYNC_DATE=10/29/2016

PAGE TITLE: High Side and CPU/AXG Current Sensing

Apple Inc.

DRAWING NUMBER | SIZE: D

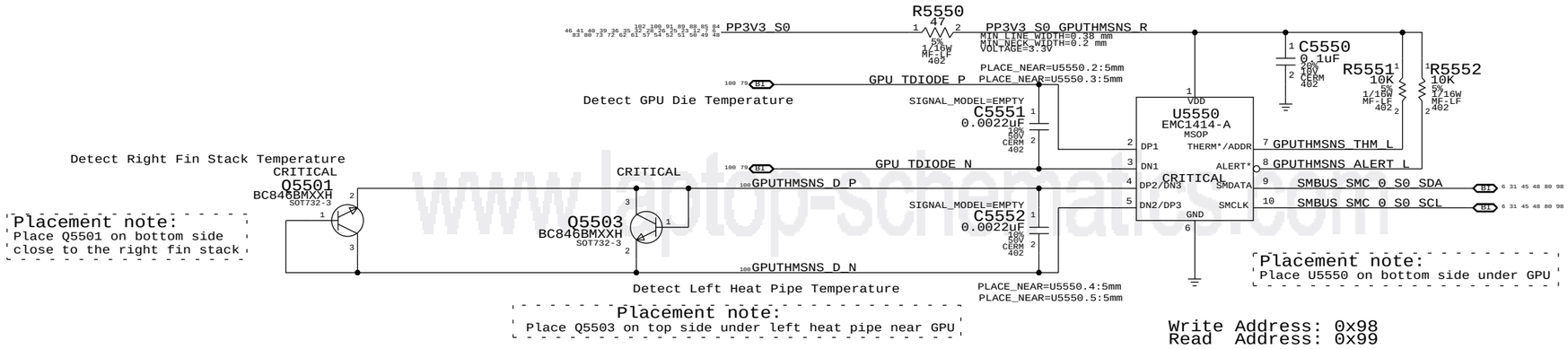
REVISION

BRANCH

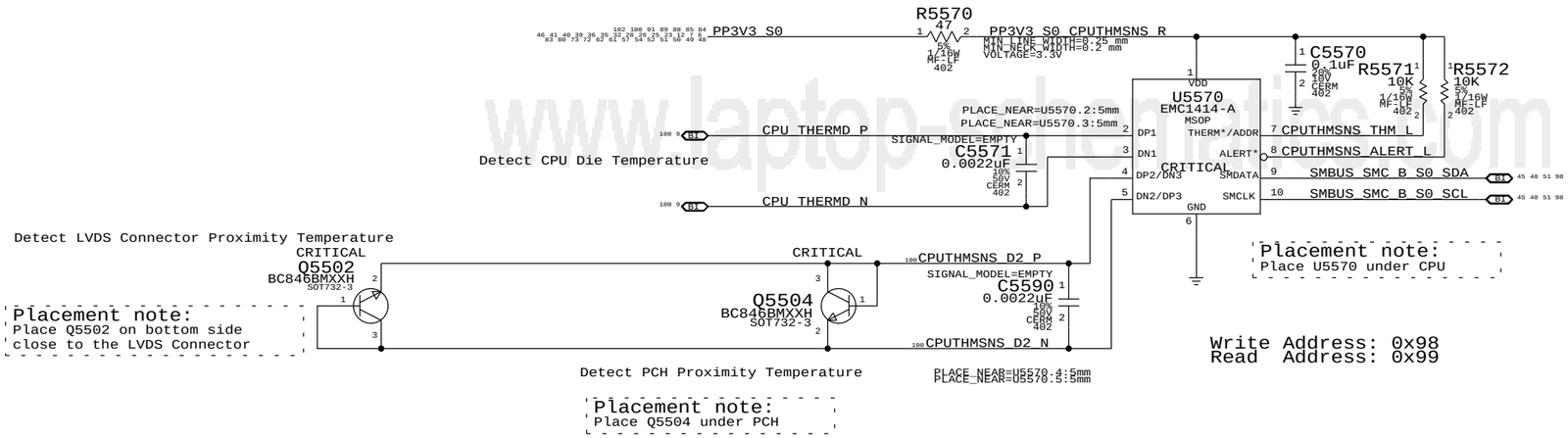
PAGE: 54 OF 132

SHEET: 50 OF 105

GPU Proximity/GPU Die/Left Heat Pipe/Right Fin Stack

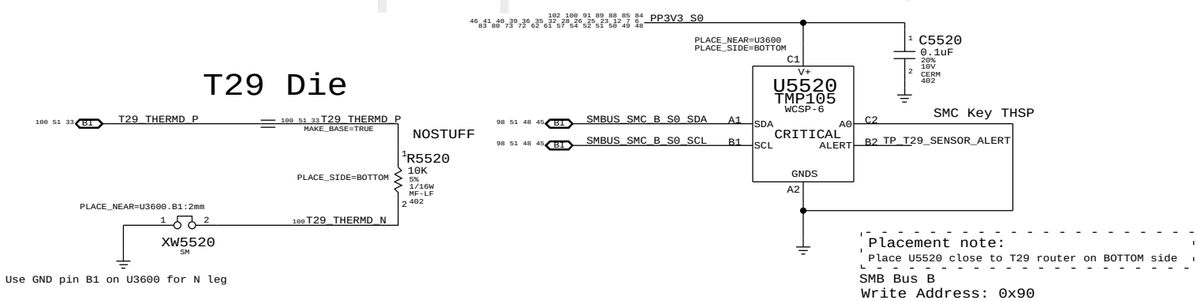


CPU Proximity/CPU Die/PCH Proximity/LVDS Connector Proximity



Note: EMC1414 can perform Beta Compensation for External Diode 1 only

T29 Proximity



SYNC_MASTER=K92_DINESH SYNC_DATE=09/24/2010

PAGE TITLE

Thermal Sensors

Apple Inc.

DRAWING NUMBER

SIZE D

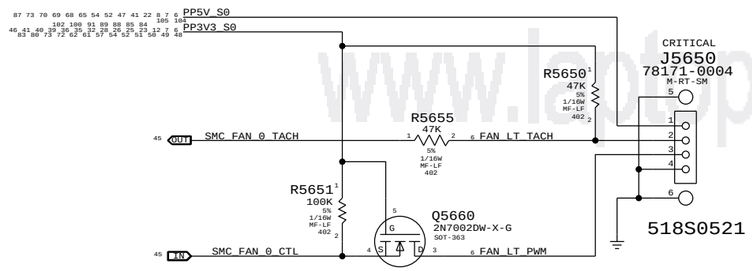
REVISION

BRANCH

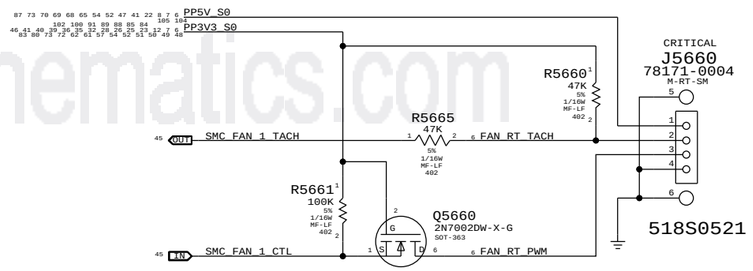
PAGE 55 OF 132

SHEET 51 OF 105

Left Fan



Right Fan



SYNC_MASTER=K17_MLB SYNC_DATE=04/26/2010

PAGE TITLE: Fan Connectors

Apple Inc.

DRAWING NUMBER: SIZE D

REVISION:

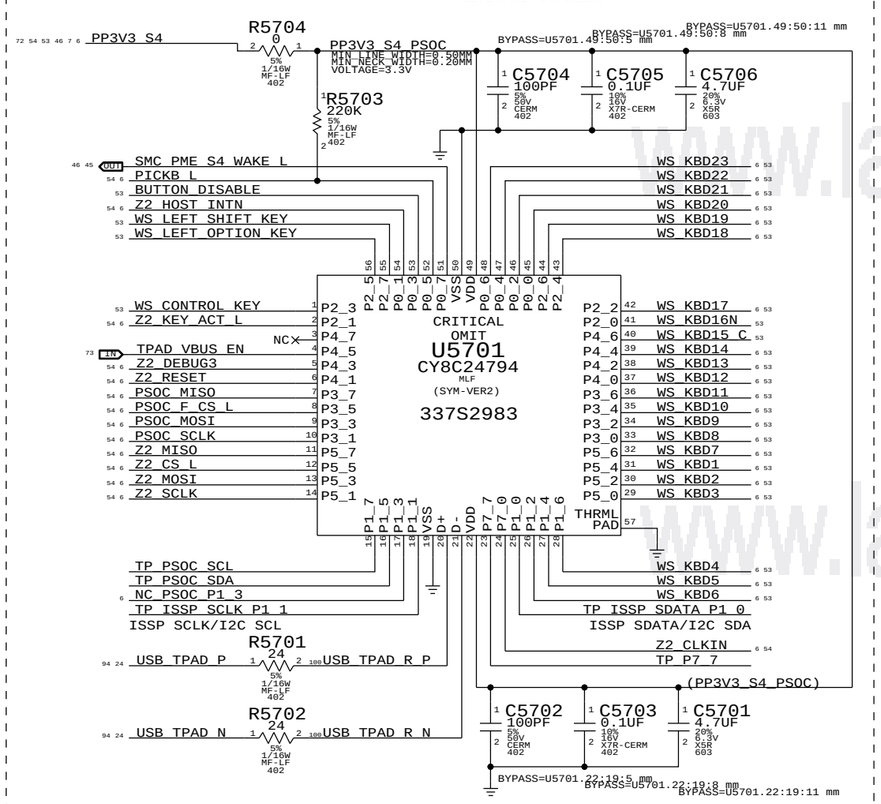
BRANCH:

PAGE: 56 OF 132

SHEET: 52 OF 105

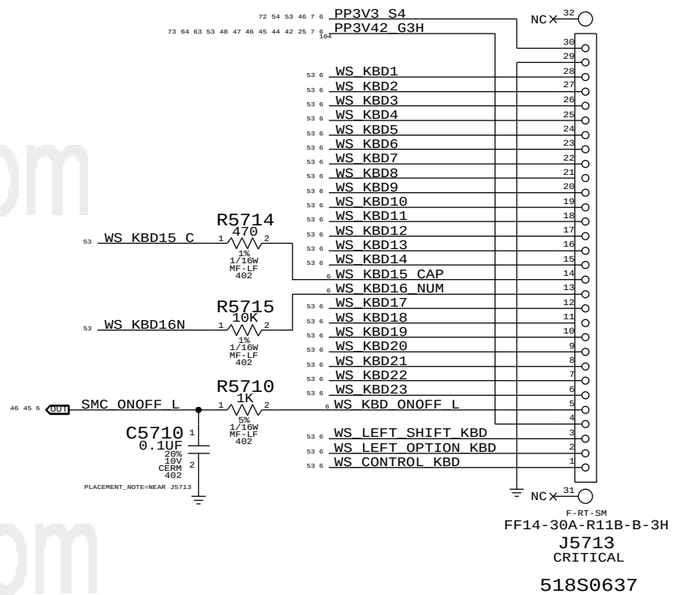
PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



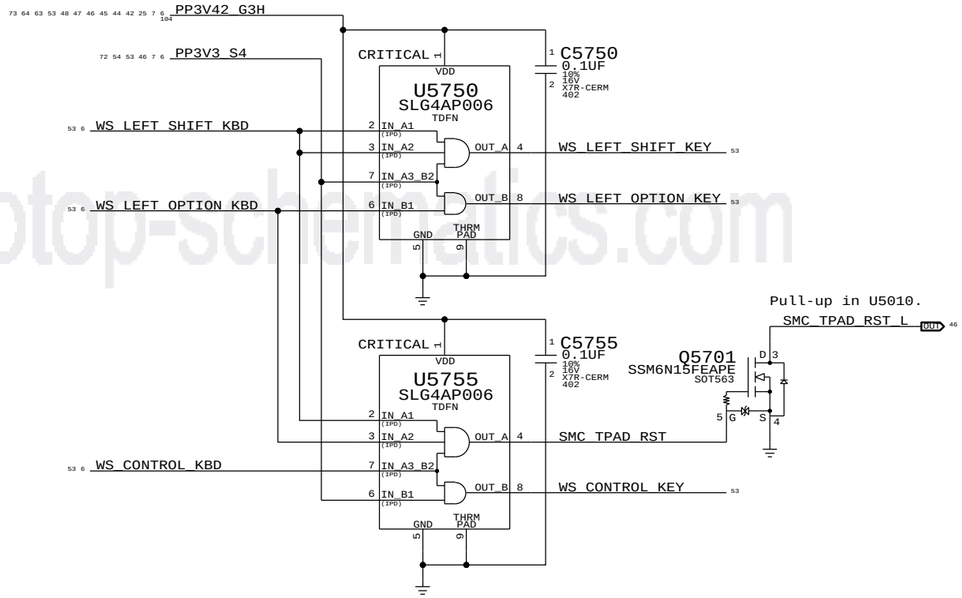
IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

Keyboard Connector

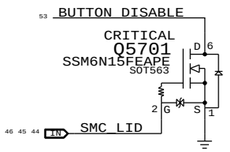


SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSOC power to isolate when PSOC is not powered.



TPAD Buttons Disable



PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

SYNC_MASTER=K92_ERIC SYNC_DATE=10/11/2010

PAGE TITLE: WELLSPRING 1

Apple Inc.

DRAWING NUMBER | SIZE: D

REVISION

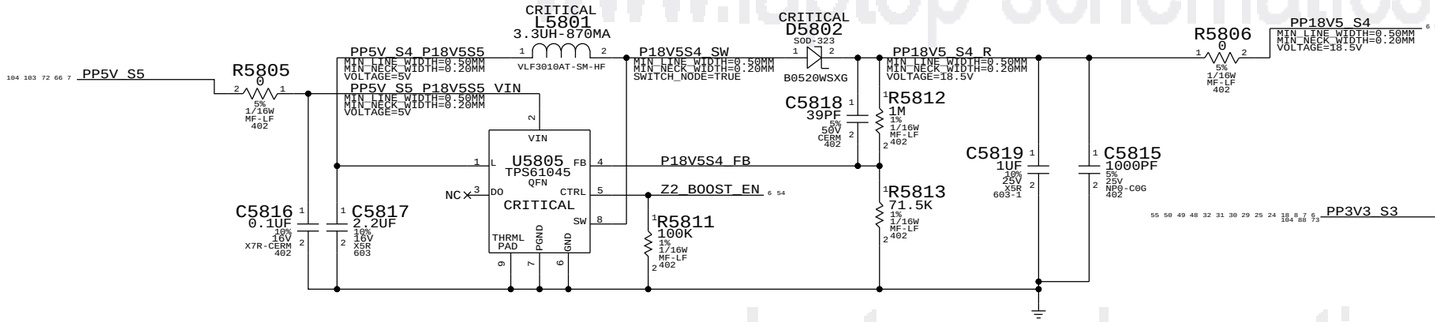
BRANCH

PAGE: 57 OF 132

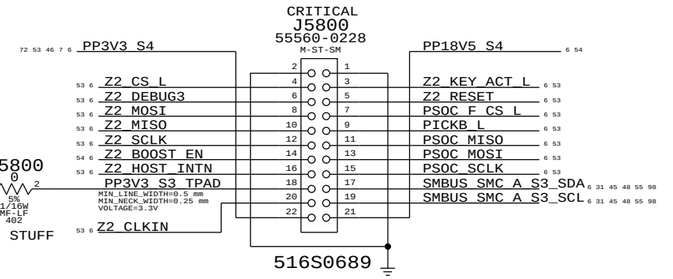
SHEET: 53 OF 105

BOOSTER +18.5VDC FOR SENSORS

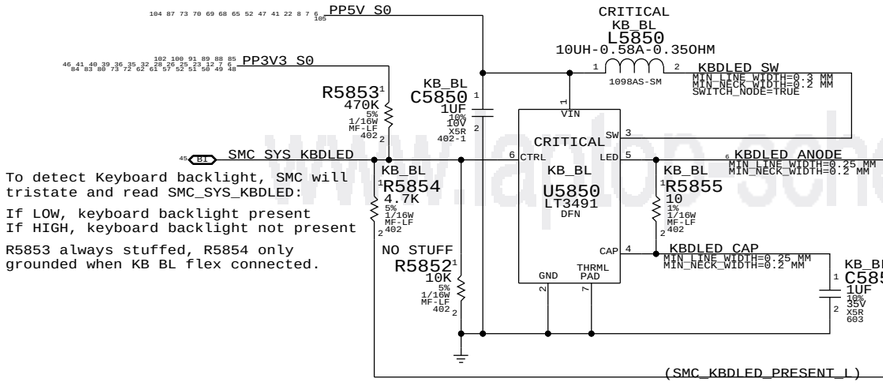
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD Flex Connector



Keyboard Backlight Driver & Detection

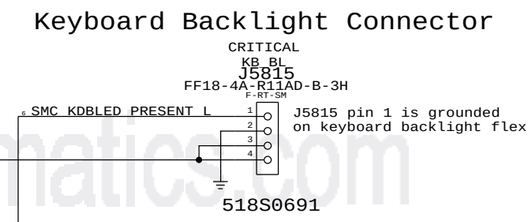


To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:

If LOW, keyboard backlight present
If HIGH, keyboard backlight not present

R5853 always stuffed, R5854 only grounded when KB BL flex connected.

Keyboard Backlight Connector



J5815 pin 1 is grounded on keyboard backlight flex

SYNC_MASTER=K92_ERIC SYNC_DATE=07/27/2010

PAGE TITLE: WELLSPRING 2

Apple Inc.

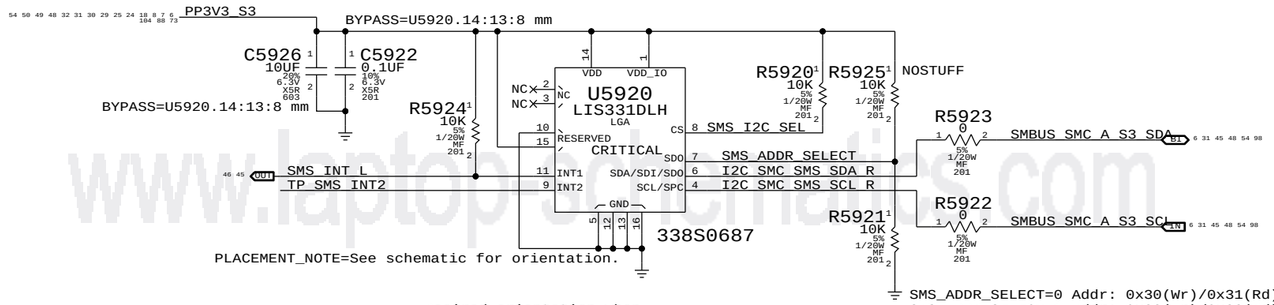
DRAWING NUMBER | SIZE: D

REVISION

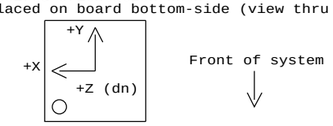
BRANCH

PAGE: 58 OF 132

SHEET: 54 OF 105



Desired orientation when
placed on board bottom-side (view thru top):



Circle indicates pin 1 location when placed
in correct orientation

SMS_ADDR_SELECT=0 Addr: 0x30(Wr)/0x31(Rd)
SMS_ADDR_SELECT=1 Addr: 0x32(Wr)/0x33(Rd)

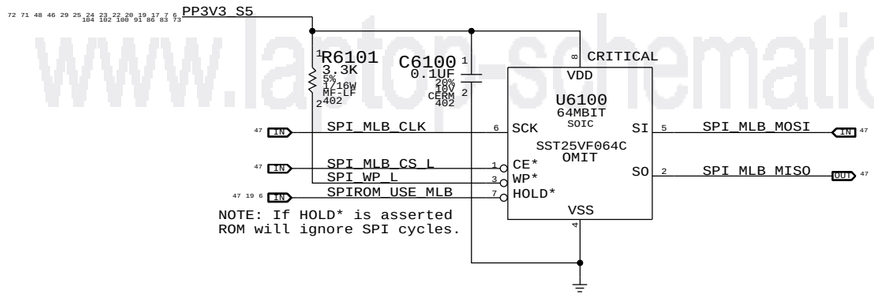
NOTE: SDA and SCL have internal pull-ups to VDD_IO.

SYNC_MASTER=K92_DINESH SYNC_DATE=06/02/2010

PAGE TITLE
Digital Accelerometer

Apple Inc.

DRAWING NUMBER
SIZE D
REVISION
BRANCH
PAGE 59 OF 132
SHEET 55 OF 105



SYNC_MASTER=K92_BEN SYNC_DATE=05/27/2010

PAGE TITLE

SPI ROM

Apple Inc.

DRAWING NUMBER | SIZE D

REVISION

BRANCH

PAGE 61 OF 132

SHEET 56 OF 105

AUDIO CODEC
APPLE P/N 353S3199

PP1V5_S0
C6200 4.7UF 20% 4V X5R 402
C6201 0.47UF 10% 10V X5R 402
C6202 10UF 20% 10V POLY-TANT CASE-B2-SM
C6203 0.47UF 10% 10V X5R 402
C6204 10UF 20% 10V POLY-TANT CASE-B2-SM
C6205 0.47UF 10% 10V X5R 402
C6206 1UF 10% 10V X5R 402-1
C6207 0.47UF 10% 10V X5R 402
CRITICAL C6208 10UF 20% 10V X5R 805
PP5V_S0_AUDIO
PP3V3_S0
PP4V5_AUDIO_ANALOG
GND_AUDIO_HPAMP
PP4V5_AUDIO_ANALOG
PLACE_XW6206_BETWEEN_IN_39_&_THERMAL_PAD
XW6206 SM
GND_AUDIO_CODEC
R6200 2.67K 1% 1/16W MF-LF 402
C6209 2.2UF 20% 6.3V CERM 402-LF
C6210 2.2UF 20% 6.3V CERM 402-LF
VBIAS_DAC
CS4206_FP
CS4206_FN
CRITICAL U6200 CS4206B QFN
VD VA_REF VA_HP VA
VBIAS_DAC 29
VHP_FILT+ 44
VHP_FILT- 41
HPOUT_L 38
HPOUT_R 40
HPREF 39
MIN_LINE_WIDTH=0.30MM MIN_NECK_WIDTH=0.20MM
MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM
AUD_HP_PORT_L
AUD_HP_PORT_R
AUD_INT_HP_REF
DIGITAL MIC DATA LINE
HP AMP CNTRL
MAC SPKR AMP CNTRL
AUD_DMIC_SDA1
AUD_GPIO_1
AUD_GPIO_2
GPIO0/DMIC_SDA1 2
GPIO1/DMIC_SDA2/SPDIF_OUT2 12
GPIO2 14
GPIO3 15
D6200 SOD-523 BAT54XV2T1
WIN SPKR AMP CNTRL
AUD_GPIO_3
SENSE_A 13
AUD_SENSE_A
CS4206_FLYP
CS4206_FLYC
CS4206_FLYN
C6211 2.2UF 20% 6.3V CERM 402-LF
C6212 2.2UF 20% 6.3V CERM 402-LF
FLYP 45
FLYC 43
FLYN 42
VL_HD 3
VL_IF 1
LINEOUT_L1+ 35
LINEOUT_L1- 34
LINEOUT_R1+ 36
LINEOUT_R1- 37
LINEOUT_L2+ 31
LINEOUT_L2- 30
LINEOUT_R2+ 32
LINEOUT_R2- 33
TP_AUD_LO2_L_P
TP_AUD_LO2_L_N
AUD_LO2_R_P
AUD_LO2_R_N
LFE SPKR AMP (FC/LFE)
AUD_LO3_L_P
AUD_LO3_L_N
AUD_LO3_R_P
AUD_LO3_R_N
WFR SPKR AMPS (L2/R2)
MICBIAS 16
AUD_CODEC_MICBIAS
XW6201 SIGNAL_MODEL=EMPTY SM
AUD_HP_PORT_L
AUD_HP_PORT_L_P
XW6202 SM
GND_AUDIO_HPAMP
AUD_HP_PORT_L_N
HDA_BIT_CLK
HDA_SYNC
HDA_SDIN0
HDA_SDOUT
HDA_RST_L
AUD_SPDIF_IN
BITCLK 6
SYNC 10
SDI 8
SDO 5
RESET* 11
SPDIF_IN 47
SPDIF_OUT 48
R6201 22 5% 1/10W MF-LF 402
AUD_SDI_R
R6202 33 5% 1/10W MF-LF 402
CS4206_SPDIF_OUT
AUD_SPDIF_OUT
R6203 100K 1% 1/16W MF-LF 402
NOSTUFF R6204 0 5% 1/16W MF-LF 402
DGND_THRM_PAD_AGND
LINEIN_L+ 21
LINEIN_C- 22
LINEIN_R+ 23
AUD_LI_L
AUD_LI_C
AUD_LI_R
MICIN_L+ 18
MICIN_L- 17
MICIN_R+ 19
MICIN_R- 20
AUD_MIC_INL_P
AUD_MIC_INL_N
AUD_MIC_INR_P
AUD_MIC_INR_N
EXTERNAL MIC INPUT
INTERNAL MIC INPUT
VCOM 28
CS4206_VCOM
NC
VREF+_ADC 27
CS4206_VREF_ADC
NC
DMIC_SCL 4
CODEC_DMIC_CLK
R6205 33 5% 1/10W MF-LF 402
AUD_DMIC_CLK
DIGITAL MIC CLOCK LINE
CRITICAL C6213 1UF 10% 20V TANT CASE-R-HF
CRITICAL C6214 10UF 20% 10V POLY-TANT CASE-B2-SM
GND_AUDIO_CODEC
GND_AUDIO_HPAMP
VOLTAGE=0V MIN_LINE_WIDTH=0.60MM MIN_NECK_WIDTH=0.20MM

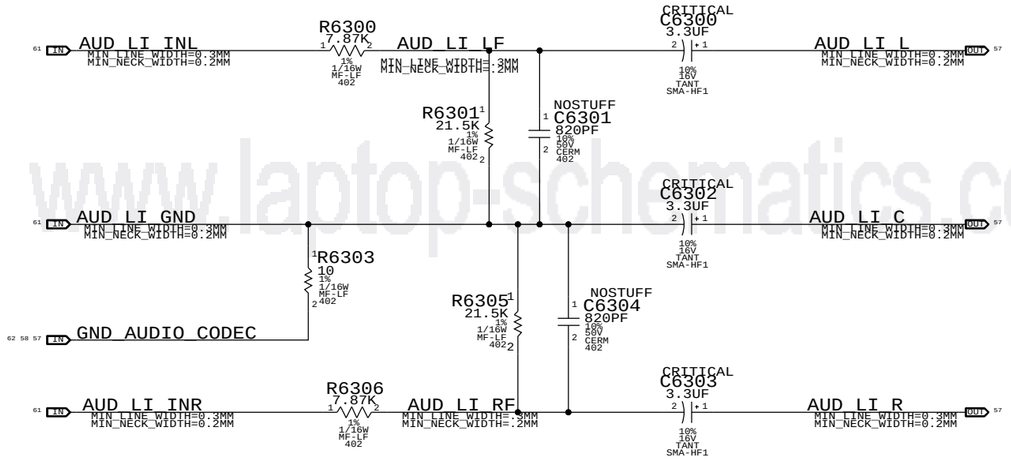
DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

AUDIO 4.5V REGULATOR
APPLE P/N 353S2234

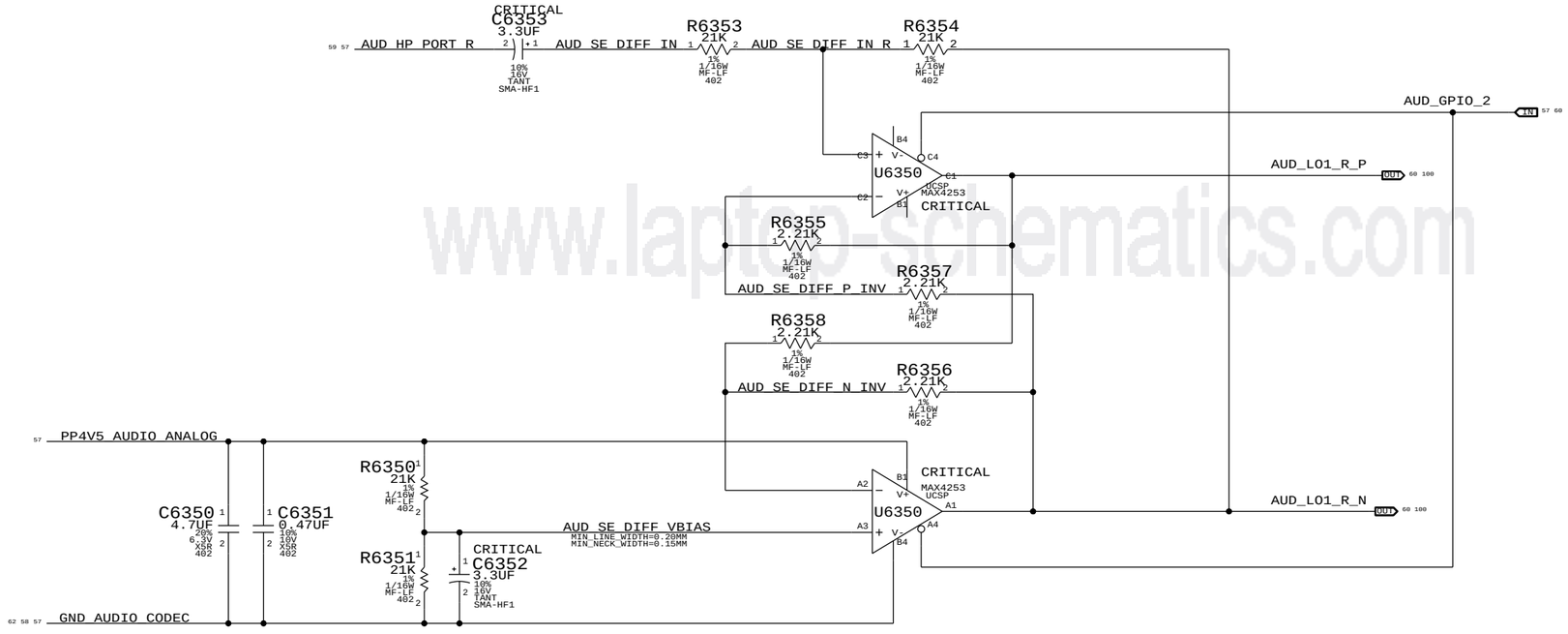
PP5V_S0_AUDIO
L6251 FERR-220-OHM 0402
PP5V_AUDIO_HPAMP
VOLTAGE=5V MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM
L6250 FERR-220-OHM 0402
AUD_4V5_REG_IN
VOLTAGE=5V MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM
U6201 MAX8840-4.5V UDFN
CRITICAL
IN OUT BP SHDN* GND NC
PP3V3_S0
R6250 1K 5% 1/10W MF-LF 402
AUD_REG_SHDN_L
MAX8840_BP
MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM
C6253 0.01UF 10% 16V CERM 402
C6254 1UF 10% 10V X5R 402
PP4V5_AUDIO_ANALOG
VOLTAGE=4.5V MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM
C6250 0.1UF 10% 16V X5R 402-1
C6251 1UF 10% 10V X5R 402
C6252 0.001UF 10% 50V CERM 402
XW6200 SM
XW6251 SM
GND_AUDIO_CODEC
GND_AUDIO_HPAMP
VOLTAGE=0V MIN_LINE_WIDTH=0.50MM MIN_NECK_WIDTH=0.20MM
VOLTAGE=0V MIN_LINE_WIDTH=0.60MM MIN_NECK_WIDTH=0.20MM

SYNC_MASTER=K92_KAVITHA SYNC_DATE=07/30/2010
PAGE TITLE: AUDIO:CODEC
Apple Inc.
DRAWING NUMBER: SIZE D
REVISION:
BRANCH:
PAGE: 62 OF 132
SHEET: 57 OF 105

CODEC Nom SE RIN = 20K OHMS
FC = 5 HZ Max
VIN = 2VRMS CODEC VIN = 1.14 VRMS
NET RIN = 18K OHMS



SE-TO-DIFF CONVERTER



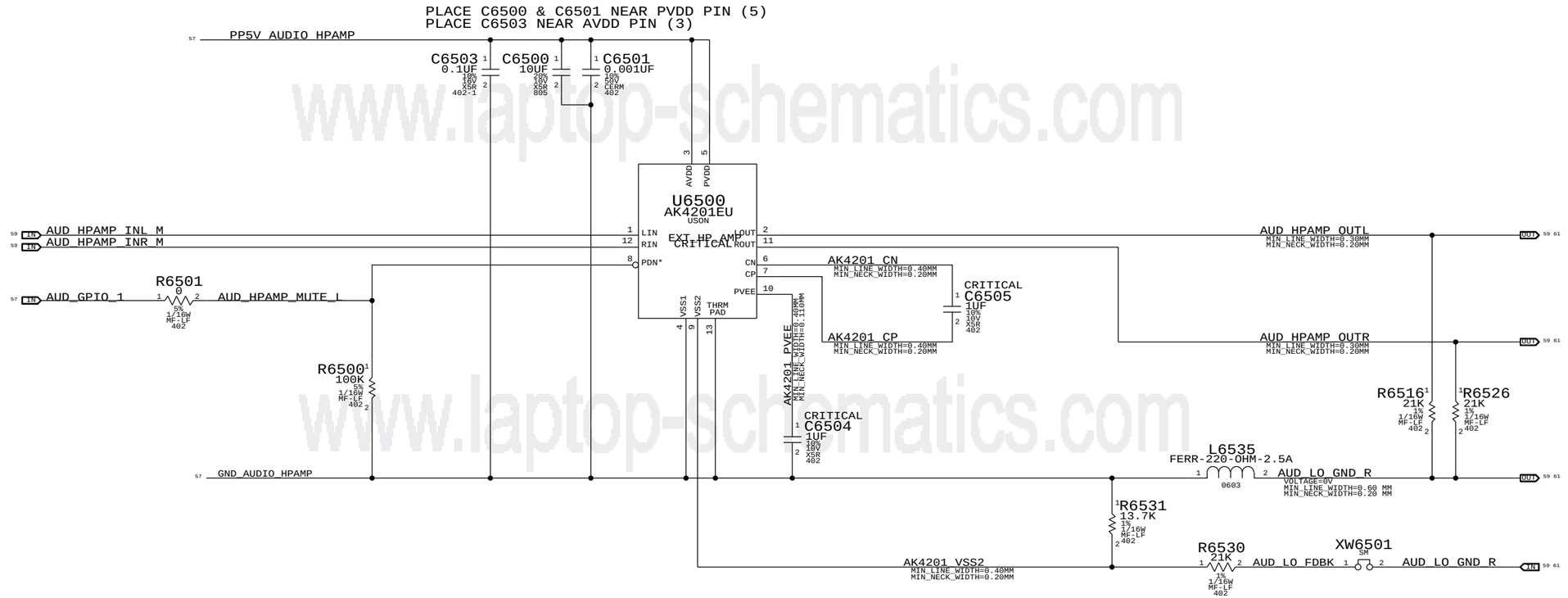
SYNC_MASTER=K92_AUDIO SYNC_DATE=06/16/2010

PAGE TITLE: AUDIO: LINE IN

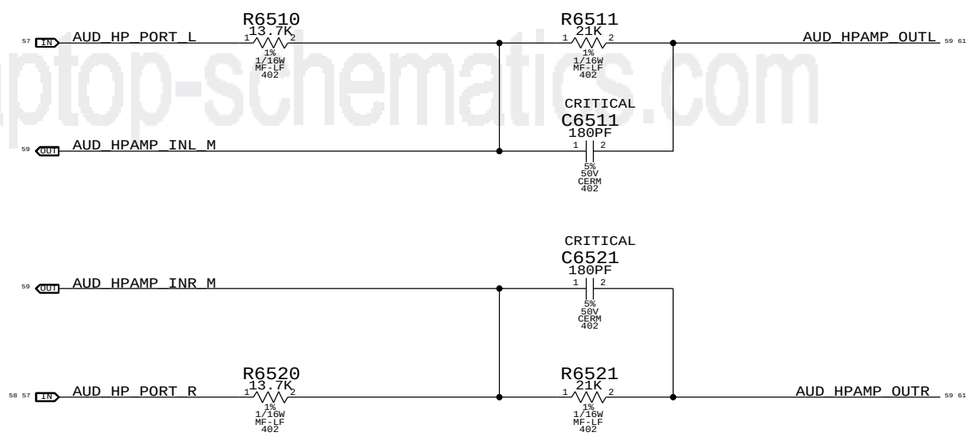
Apple Inc.

DRAWING NUMBER | SIZE: D
REVISION
BRANCH
PAGE: 63 OF 132
SHEET: 58 OF 105

HEADPHONE AMPLIFIER (AK4201)
APN:353S2347
VOLTAGE GAIN:1.53



1ST ORDER DAC FILTER
LP:42.10 KHZ



SYNC_MASTER=K92_KAVITHA SYNC_DATE=10/22/2010

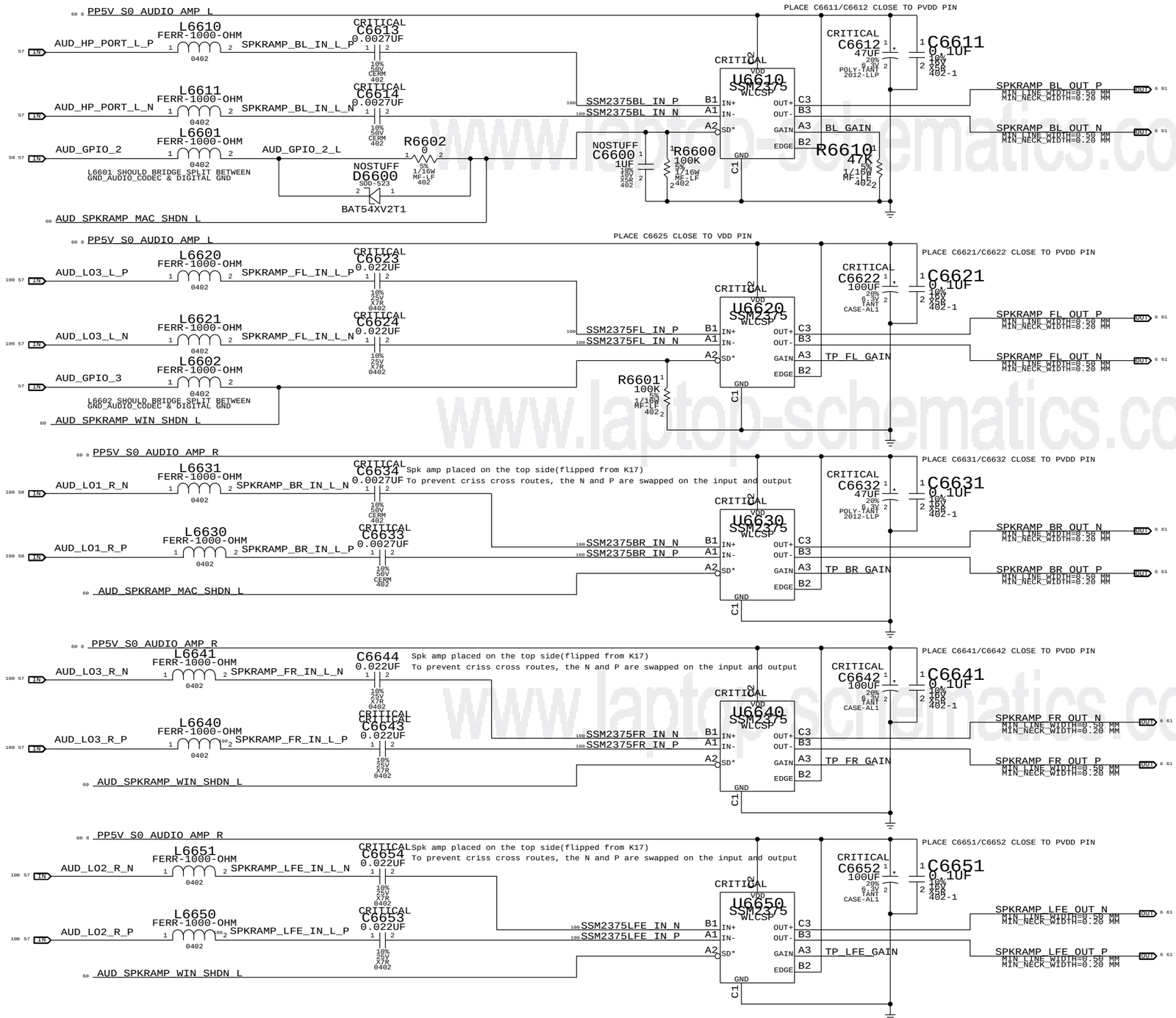
PAGE TITLE
AUDIO: HEADPHONE OUT

Apple Inc.

DRAWING NUMBER | SIZE D
REVISION
BRANCH
PAGE 65 OF 132
SHEET 59 OF 105

5X MONO SPEAKER AMPLIFIERS (SSM2375)

APN: 353S2958
GAIN = +3 DB (BR, FL, FR, LFE), +9 DB (BL)
FC (SPEAKERS BL/BR) = ~737 HZ
FC (SPEAKERS FL/FR/LFE) = ~90 HZ



SYNC_MASTER=K92_KAVITHA SYNC_DATE=10/22/2010

PAGE TITLE: AUDIO:SPEAKER AMP

Apple Inc.

DRAWING NUMBER: SIZE D
REVISION:
BRANCH:
PAGE: 66 OF 132
SHEET: 60 OF 105

AUDIO JACK 1 LO/HP JACK, SPDIF TX

PP3V3_S0

APN: 514-0632

CRITICAL
J6700
SPDIF-TX-K20
F-RT-TH

MICROPHONE 6
DETECT_FOR_PT 5
SWITCH 2
LEFT 1
RIGHT 3
GROUND 4

AUDIO
A - VIN 7
B - VCC 8
C - GND 9
OPERATING VOLTAGE 3.3
POF

SHELL PINS 10 11 12 13

AUD_CONNJ1_SLEEVE2 — MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM
AUD_CONNJ1_SLEEVEDET — MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM
AUD_CONNJ1_TIPDET — MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM
AUD_CONNJ1_TIP — MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM
AUD_CONNJ1_RING — MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM
AUD_CONNJ1_SLEEVE — MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM

L6700 FERR-1000-OHM 0402 — HS_MIC_HI OUT 62
R6701 10K 5% 1/16W MF-LF 402 — AUD_J1_SLEEVEDET_R OUT 62
L6702 FERR-1000-OHM 0402 — AUD_J1_PERIPHDET_R OUT 62
L6703 FERR-1000-OHM 0402 — AUD_J1_TIPDET_R OUT 62
L6704 CRITICAL FERR-220-OHM 0402 — AUD_HPAMP_OUTL BI 59
L6705 CRITICAL FERR-220-OHM 0402 — AUD_HPAMP_OUTR BI 59
L6706 CRITICAL FERR-1200-OHM-200MA 0402 — HS_MIC_LO OUT 62
L6707 CRITICAL FERR-220-OHM-2.5A 0603 — AUD_LO_GND_R OUT 59
PP3V3_S0 → L6783 600-OHM-300MA 0402
AUD_SPDIF_OUT — AUD_SPDIF_OUT IN 57

C6700 1UF 10% 10V X5R 402

OMIT_TABLE
CRITICAL DX6706 ESDALC5-1BM2 SOD882

CRITICAL DZ6700 6.8V-100PF 402
CRITICAL DZ6701 6.8V-100PF 402
CRITICAL DZ6702 6.8V-100PF 402
CRITICAL DZ6703 6.8V-100PF 402
CRITICAL DZ6704 6.8V-100PF 402
CRITICAL DZ6705 6.8V-100PF 402

XW6701 SM
XW6702 SM

GND_CHASSIS_AUDIO_JACK — MIN_LINE_WIDTH=0.50MM MIN_NECK_WIDTH=0.20MM VOLTAGE=0V

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
377S0112	1	EMC supressor	DX6706		

MIC CONNECTORS: single anlg mic + 1 dig mic

APN: 518S0520

CRITICAL
J6780
78171-0003
M-RT-SM

BI_MIC_N
BI_MIC_SHIELD
BI_MIC_P

APN: 518S0521

CRITICAL
J6783
78171-0004
M-RT-SM

AUD_DMIC_CLK
AUD_DMIC_SDA1
PP3V3_S0
AUD_DMIC_CLK_BK
AUD_DMIC_SDA_BK
AUD_DMIC_PWR_BK

SPEAKER CONNECTORS
APN: 518S0521

CRITICAL
J6781
78171-0004
M-RT-SM

SPKRAMP_FL_OUT_P
SPKRAMP_FL_OUT_N
SPKRAMP_BL_OUT_P
SPKRAMP_BL_OUT_N

NOSTUFF C6781 100PF 5% 50V CERM 402
NOSTUFF C6782 100PF 5% 50V CERM 402
NOSTUFF C6783 100PF 5% 50V CERM 402
NOSTUFF C6784 100PF 5% 50V CERM 402

APN: 518S0672

CRITICAL
J6782
78171-6006
M-RT-SM

SPKRAMP_FR_OUT_P
SPKRAMP_FR_OUT_N
SPKRAMP_BR_OUT_P
SPKRAMP_BR_OUT_N
SPKRAMP_LFE_OUT_P
SPKRAMP_LFE_OUT_N

AUDIO JACK 2 LINE IN JACK, SPDIF RX

PP3V3_S0

APN: 514-0633

CRITICAL
J6750
SPDIF-RX-K20
F-RT-TH

DETECT_FOR_PT 5
SWITCH 2
LEFT 1
RIGHT 3
GROUND 4

AUDIO
A - VDD 6
B - GND 7
C - VOUT 8
OPERATING VOLTAGE 3.3
POF

SHELL PINS 9 10 11 12

AUD_CONNJ2_TIPDET
AUD_CONNJ2_TIP — MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM
AUD_CONNJ2_RING — MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM
AUD_CONNJ2_SLEEVE — MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM
AUD_J2_OPT_OUT

L6751 FERR-1000-OHM 0402 — AUD_J2_TIPDET_R OUT 62
L6752 FERR-1000-OHM 0402 — AUD_LI_INL BI 58
L6753 FERR-1000-OHM 0402 — AUD_LI_INR BI 58
L6754 600-OHM-300MA 0402 — AUD_LI_GND OUT 58
R6755 10 5% 1/16W MF-LF 402 — AUD_SPDIF_IN OUT 57

C6750 1UF 10% 10V X5R 402

CRITICAL DZ6753 ESDALC5-1BM2 SOD882
CRITICAL DZ6750 ESDALC5-1BM2 SOD882
CRITICAL DZ6751 6.8V-100PF 402
CRITICAL DZ6752 6.8V-100PF 402

GND_CHASSIS_AUDIO_JACK

RETURN FOR HF NOISE
R6750 0 5% 1/16W MF-LF 402

SYNC_MASTER=K92_KAVITHA SYNC_DATE=11/02/2010

PAGE TITLE: AUDIO: JACKS

Apple Inc.

DRAWING NUMBER:
SIZE: D
REVISION:
BRANCH:
PAGE: 67 OF 132
SHEET: 61 OF 105

CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	MAC OS SHDN	WIN SHDN	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	N/A	0X09 (A)
SPEAKERS BL/BR	0X02 (2)	0X02 (2)	0X09 (9,V23)	GPIO_2	N/A	N/A
SPEAKERS FL/FR	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_2	GPIO_3	N/A
SPEAKER LFE	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	N/A	0X0D (B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X05 (5)	0X12 (12,C)	N/A	0X12 (C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
INTERNAL MIC	0X06 (6)	0X0D (13,B,RIGHT)	MICBIAS (80%)	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

"MIKEY"/EXTERNAL MICROPHONE
APN 353S2640

PP3V3_S0
L6880 FERR-1000-OHM 0402
MIN_LINE_WIDTH=0.15MM
MIN_NECK_WIDTH=0.10MM
VOLTAGE=3.3V
PP3V3_S0_HS_RX
R6886 10K 5% 1/16W MF-LF 402
CRITICAL C6880 10UF 20% 6.3V X5R 603
C6881 0.001UF 10% 50V CERM 402
SMBUS_PCH_CLK (IN) R6890 0 5% 1/16W MF-LF 402
SMBUS_PCH_DATA (BI) R6891 0 5% 1/16W MF-LF 402
AUD_I2C_INT_L (OUT) R6892 0 5% 1/16W MF-LF 402
AUD_IPHS_SWITCH_EN (IN) R6893 0 5% 1/16W MF-LF 402
AUD_J1_PERIPHDET_R R6894 0 5% 1/16W MF-LF 402
PERIPHDET_UNFILT
R6880 100K 5% 1/16W MF-LF 402
GND_AUDIO_CODEC
NOSTUFF R6884 0 5% 1/16W MF-LF 402
CRITICAL U6880 CD3282A1 WCSP
AVDD A2
HS_SCL C3 SCL
HS_SDA B3 SDA
HS_INT_L D3 INT*
HS_RST_L A3 ENABLE
A1 HDET
B2 CS
MICBIAS C1 HS_MIC_BIAS
DETECT B1 HS_SW_DET
BYPASS D1 HS_RX_BP
DGND C2
AGND D2
KEEP DET TRACE AS SHORT AS POSS
C6882 0.01UF 10% 25V X7R 402
CRITICAL C6883 4.7UF 20% 6.3V TANT 603-HF
R6881 1K 5% 1/16W MF-LF 402
R6882 2.2K 5% 1/16W MF-LF 402
CRITICAL C6884 0.47UF 10% 10V X5R 402
AUD_MIC_INL_P (OUT)
R6885 2.2K 5% 1/16W MF-LF 402
HS_MIC_HI (IN)
R6883 100K 5% 1/16W MF-LF 402
C6886 0.0082UF 10% 25V X7R 402
NOSTUFF C6887 15PF 5% 50V CERM 402
CRITICAL C6885 0.47UF 10% 10V X5R 402
AUD_MIC_INL_N (OUT)
HS_MIC_LO (IN)
XW6800 SM
GND_AUDIO_CODEC

PORT A DETECT (LINE OUT)
PORT B DETECT (SPDIF DELEGATE)
AUD_SENSE_A (OUT)
PP3V3_S0_AUDIO_F
R6806 39.2K 1% 1/10W MF-LF 402
R6805 20.0K 1% 1/10W MF-LF 402
AUD_OUTJACK_INSERT_L
AUD_PORTA_DET_L_NC
AUD_PORTB_DET_L_NC
R6801 270K 5% 1/16W MF-LF 402
Q6800 SSM6N15FEAPE SOT563
Q6801 SSM6N15FEAPE SOT563
Q6801 SSM6N15FEAPE SOT563
R6802 47K 5% 1/16W MF-LF 402
AUD_J1_TIPDET_R (IN)
AUD_J1_DET_RC
C6801 0.1UF 10% 16V CERM 402
GND_AUDIO_CODEC
R6803 100K 5% 1/16W MF-LF 402
PP3V3_S0_AUDIO_F
AUD_J1_SLEEVEDET_INV
R6804 220K 5% 1/16W MF-LF 402
Q6800 SSM6N15FEAPE SOT563
AUD_J1_SLEEVEDET_R
AUD_J1_SLEEVEDET_R (IN)
C6802 0.01UF 10% 16V CERM 402
GND_AUDIO_CODEC

PORT C DETECT (LINE IN)
AUD_SENSE_A (OUT)
PP3V3_S0_AUDIO_F
R6813 10K 1% 1/10W MF-LF 402
AUD_INJACK_INSERT_L_NC
R6811 270K 5% 1/16W MF-LF 402
Q6802 SSM3K15FV SOD-VESM-HF
R6812 47K 5% 1/16W MF-LF 402
AUD_J2_TIPDET_R (IN)
AUD_J2_DET_RC
C6811 0.1UE 10% 16V CERM 402
GND_AUDIO_CODEC

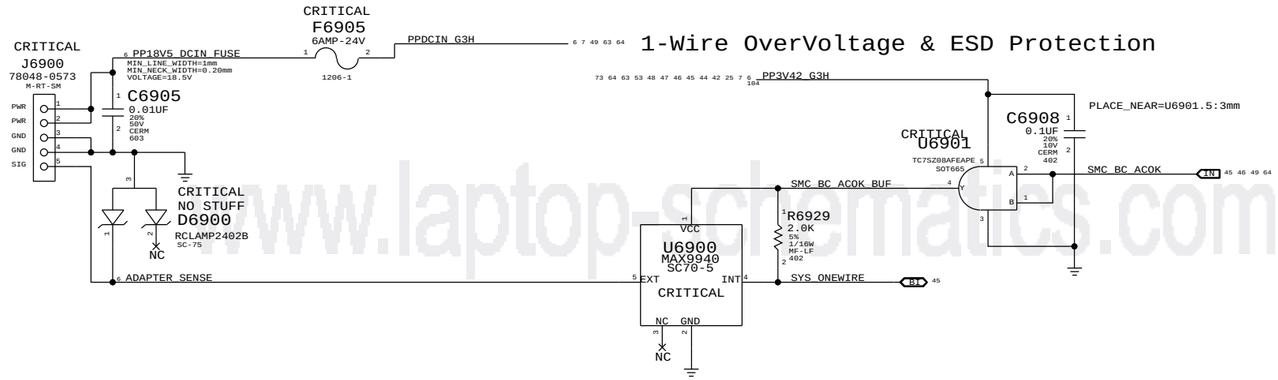
PLACE L6800/C6800 CLOSE TO Q6800/01/02
L6800 FERR-1000-OHM 0402
PP3V3_S0
PP3V3_S0_AUDIO_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.20MM
MIN_NECK_WIDTH=0.10MM
C6800 0.1UF 10% 16V X5R 402-1
GND_AUDIO_CODEC

EXTRACTION NOTIFICATION CKT
PP3V3_S0_AUDIO_F (IN)
R6861 220K 5% 1/16W MF-LF 402
R6862 100K 5% 1/16W MF-LF 402
Q6803 SSM6N15FEAPE SOT563
R6863 0 5% 1/16W MF-LF 402
AUD_PERIPH_DET_R
AUD_IP_PERIPHERAL_DET (OUT)
R6860 15K 5% 1/16W MF-LF 402
AUD_J1_PERIPHDET_R (IN)
PERIPHDET_FILT
Q6803 SSM6N15FEAPE SOT563
C6860 0.1UF 20% 16V CERM 402
AUD_J1_PERIPHDET_INV
GND_AUDIO_CODEC

INTERNAL MICROPHONE
AUD_CODEC_MICBIAS (IN)
R6855 2.2K 5% 1/16W MF-LF 402
INT_MIC_BIAS
CRITICAL C6854 10UF 20% 6.3V TANT-POLY 2012-LLP
R6850 3.40K 1% 1/16W MF-LF 402
GND_AUDIO_CODEC
CRITICAL C6850 0.47UF 10% 10V X5R 402
AUD_MIC_INR_P (OUT)
BI_MIC_P
C6852 0.0082UF 10% 25V X7R 402
R6852 100K 5% 1/16W MF-LF 402
CRITICAL C6851 0.47UF 10% 10V X5R 402
AUD_MIC_INR_N (OUT)
BI_MIC_N
R6851 3.40K 1% 1/16W MF-LF 402
XW6850 SM
GND_AUDIO_CODEC
INT_MIC_RET
XW6851 SM
BI_MIC_SHIELD

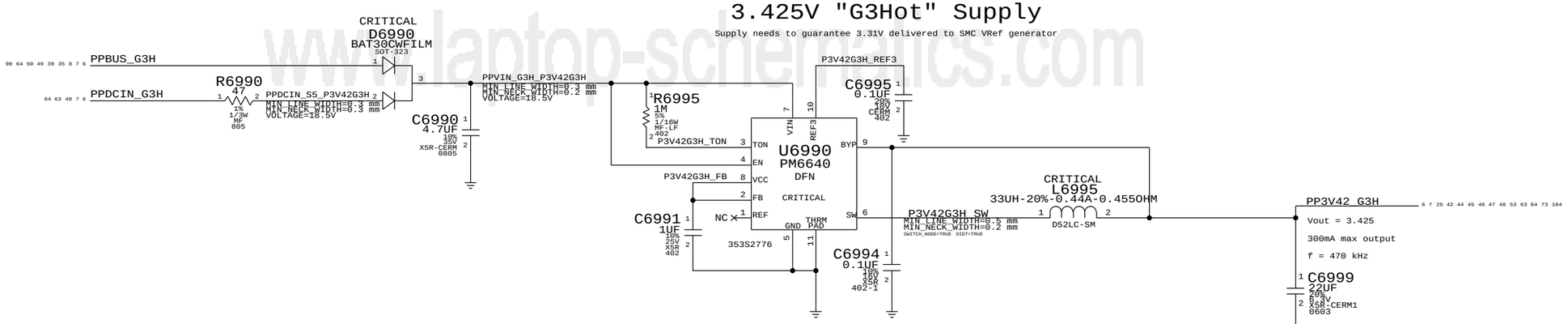
SYNC_MASTER=K92_KAVITHA SYNC_DATE=11/22/2010
PAGE TITLE: AUDIO: JACK TRANSLATORS
Apple Inc.
DRAWING NUMBER SIZE D
REVISION
BRANCH
PAGE 68 OF 132
SHEET 62 OF 105

MagSafe DC Power Jack



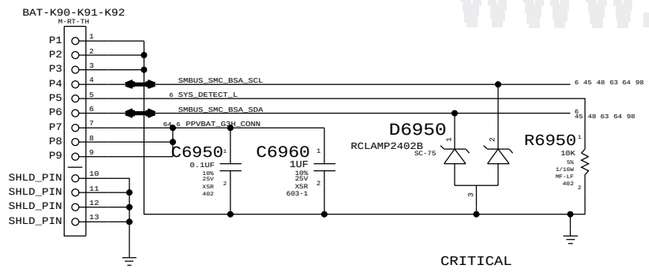
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



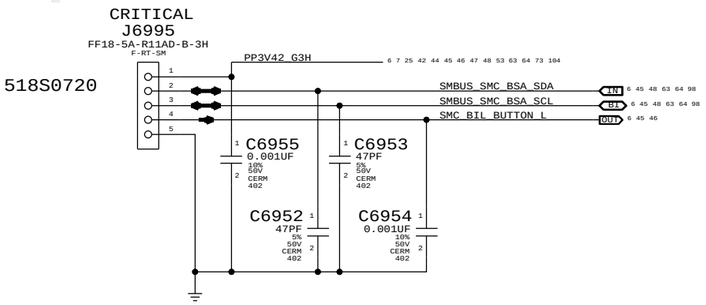
BATTERY CONNECTOR

518-0375



BIL Connector

518S0720



SYNC_MASTER=K92_CHANG SYNC_DATE=06/28/2010

PAGE TITLE: DC-In & Battery Connectors

Apple Inc.

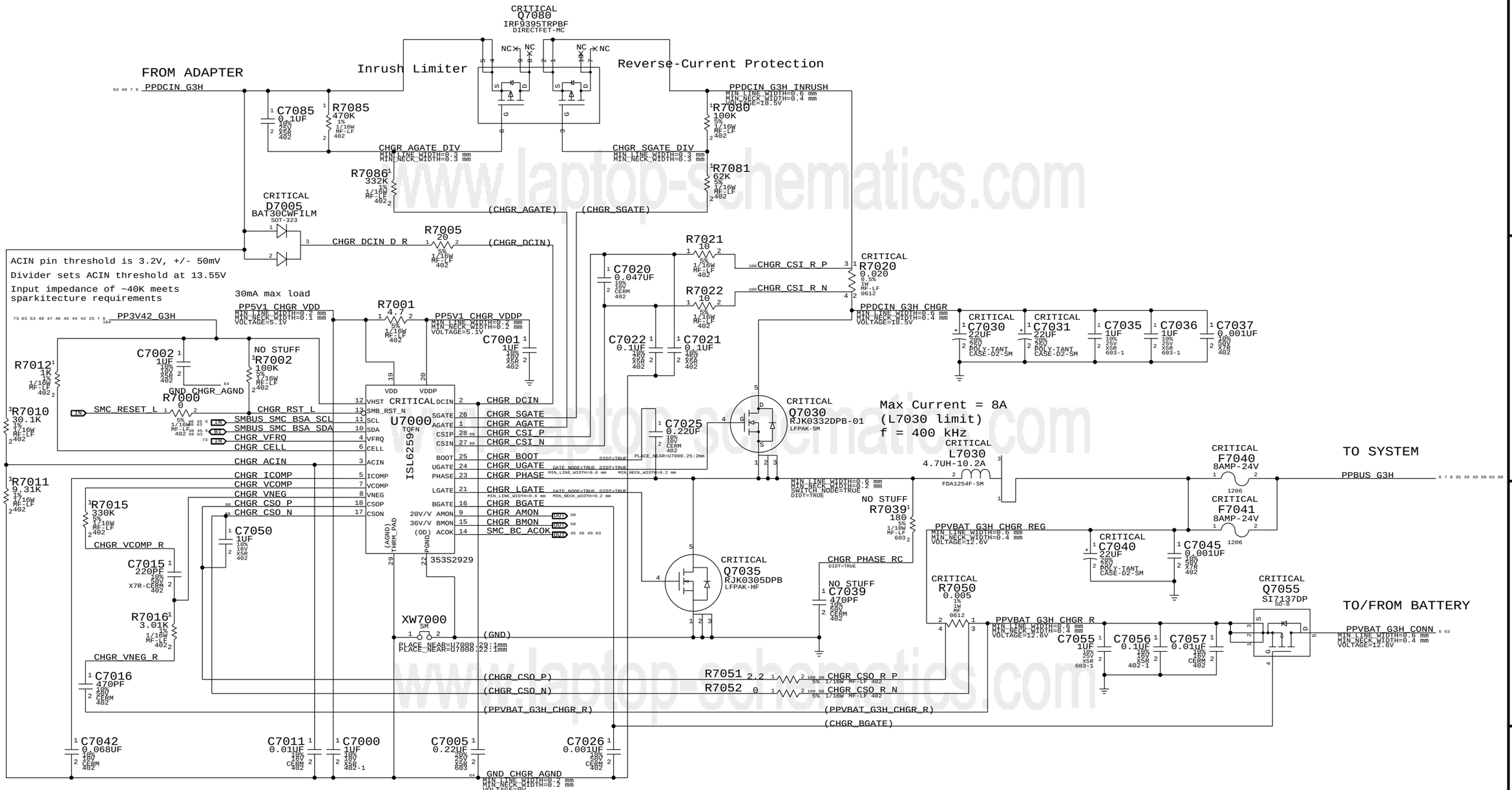
DRAWING NUMBER | SIZE: D

REVISION

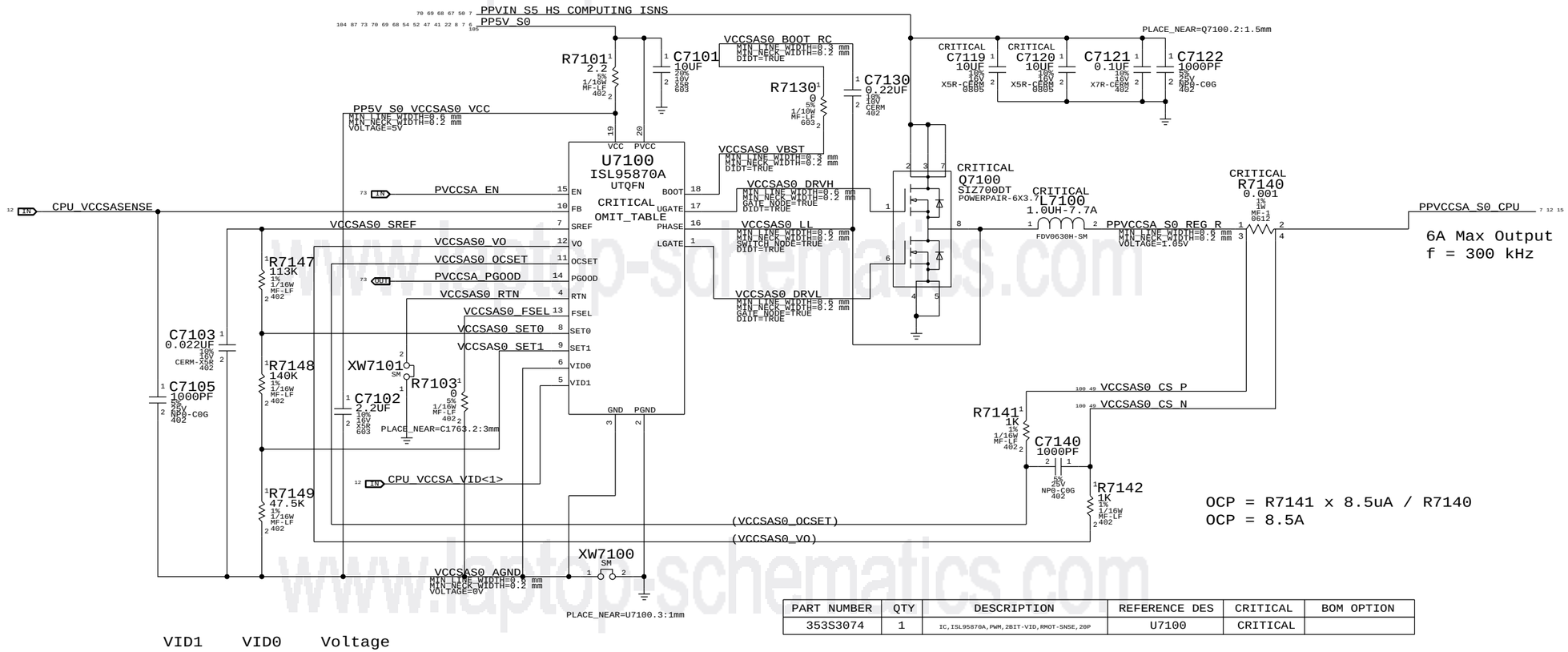
BRANCH

PAGE: 69 OF 132

SHEET: 63 OF 105



SYNC_MASTER=K91_CHANG	SYNC_DATE=07/21/2016
PAGE TITLE	PBus Supply & Battery Charger
Apple Inc.	DRAWING NUMBER: SIZE: D
	REVISION:
	BRANCH:
	PAGE: 70 OF 132
	SHEET: 64 OF 105



VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3074	1	IC,ISL95870A,PWM,2BIT-VID,RMOT-SNSE,20P	U7100	CRITICAL	

SYNC_MASTER=K91_CHANG SYNC_DATE=07/21/2010

PAGE TITLE: System Agent Supply

Apple Inc.

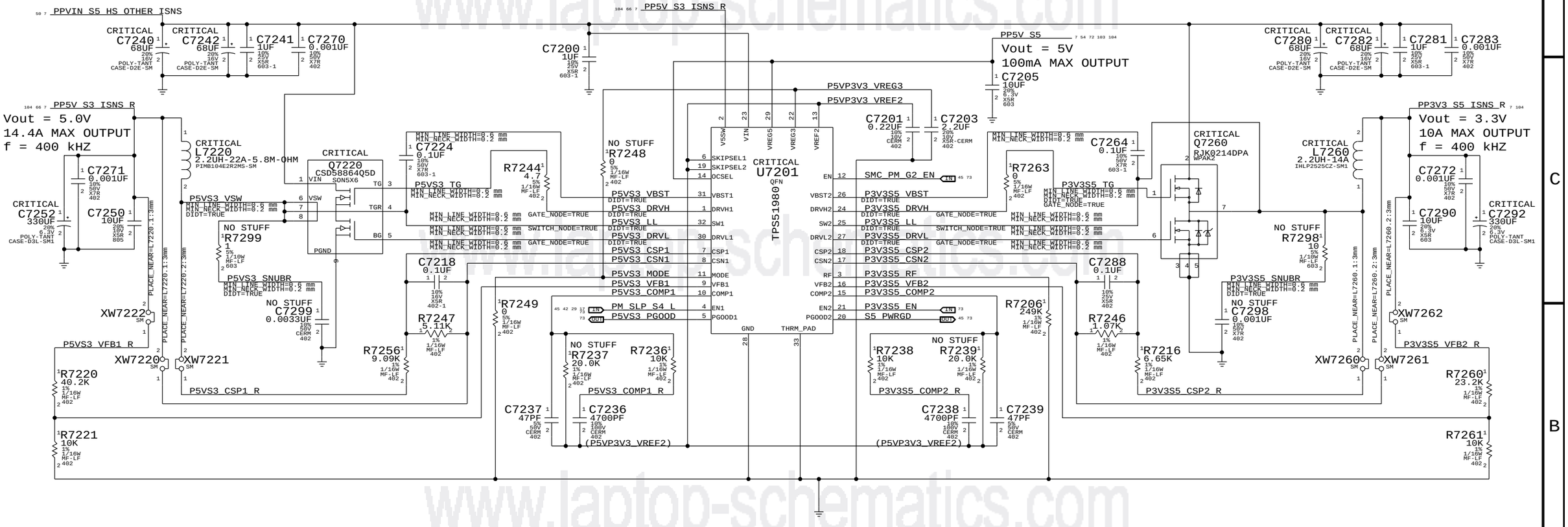
DRAWING NUMBER | SIZE: D

REVISION

BRANCH

PAGE: 71 OF 132

SHEET: 65 OF 105



SYNC_MASTER=K92_ERIC SYNC_DATE=08/30/2010

PAGE TITLE: 5V / 3.3V Power Supply

Apple Inc.

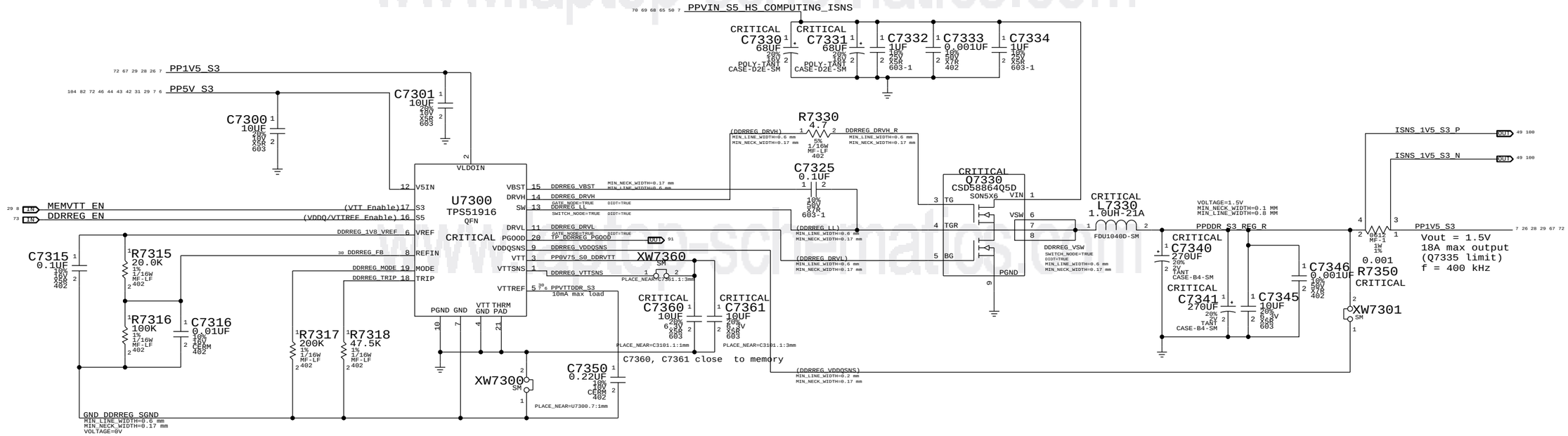
DRAWING NUMBER | SIZE: D

REVISION

BRANCH

PAGE: 72 OF 132

SHEET: 66 OF 105



SYNC_MASTER=K91_CHANG SYNC_DATE=07/21/2010

PAGE TITLE: 1.5V DDR3 Supply

Apple Inc.

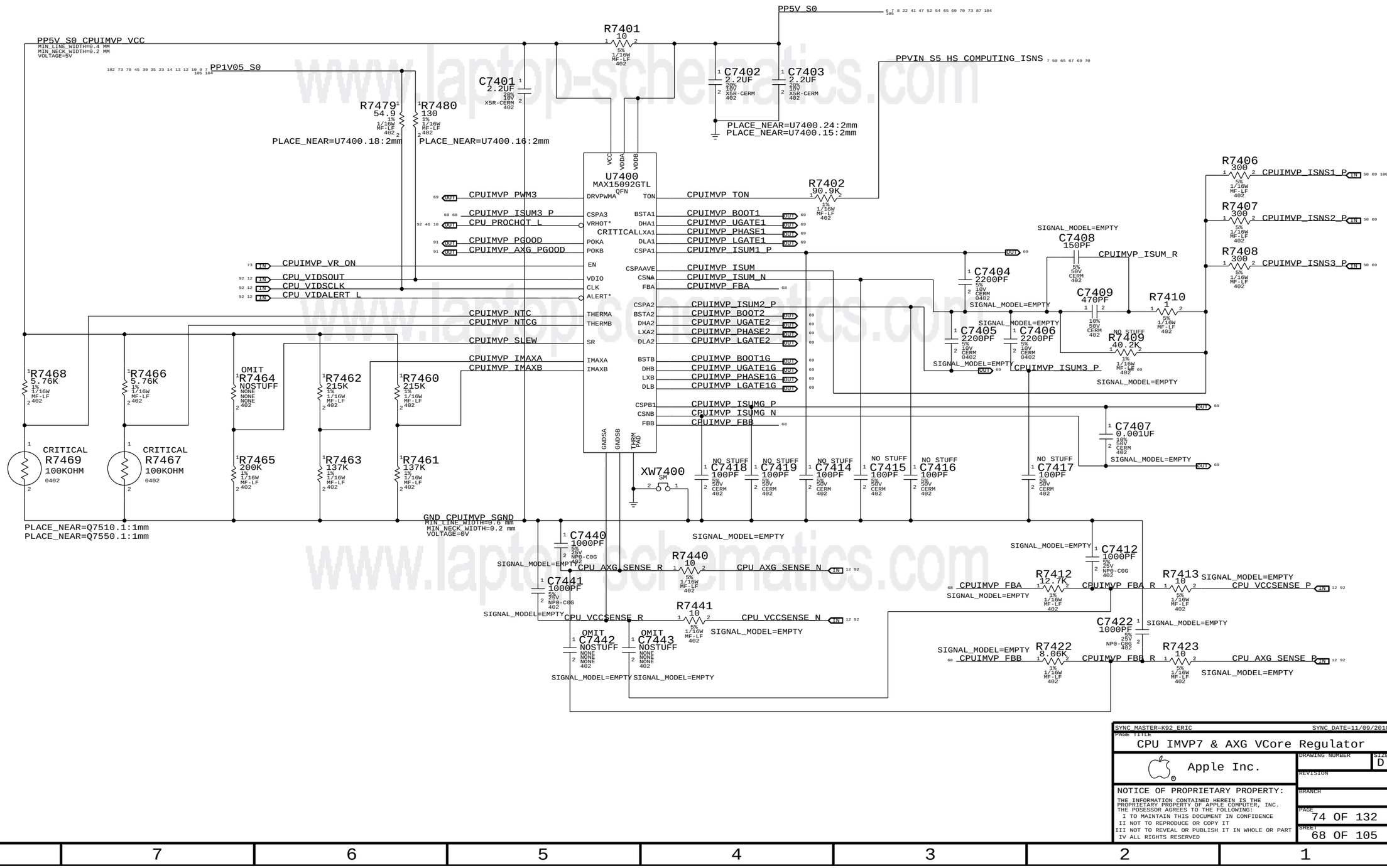
DRAWING NUMBER | SIZE: D

REVISION

BRANCH

PAGE: 73 OF 132

SHEET: 67 OF 105



SYNC_MASTER=K92_ERIC SYNC_DATE=11/09/2010

PAGE TITLE
CPU IMVP7 & AXG VCore Regulator

Apple Inc.

DRAWING NUMBER
SIZE D

REVISION

BRANCH

PAGE 74 OF 132

SHEET 68 OF 105

PHASE 1

PPVIN_S5_HS_COMPUTING_ISNS

376S0872

CRITICAL Q7510 IRF6723M2DPBF DIRECTFET-MA

CRITICAL L7510 0.36UH-20%-40A-0.000750HM PIMA104E-SM 152S1019

CRITICAL R7510 0.00075 1% 1W MF 0612

PPVCORE_S0_CPU_PH1_L → PPVCORE_S0_CPU_PH1 → PPVCORE_S0_CPU

THESE TWO CAPS ARE FOR EMC

CRITICAL C7513 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7514 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7515 10UF 10% 16V X5R-CERM 0805
CRITICAL C7516 10UF 10% 16V X5R-CERM 0805
CRITICAL C7517 1UF 10% 16V X5R 402
CRITICAL C7518 0.001UF 10% 50V X7R 402
C7519 0.001UF 10% 50V X7R 402

C7511 0.22UF 10% 16V CERM 402

R7511 0 5% 1/16W MF-LF 402

CPUIMVP_BOOT1_RC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.25 MM
DIDT=TRUE

CPUIMVP_BOOT1 — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE
CPUIMVP_UGATE1 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE_NODE=TRUE
CPUIMVP_PHASE1 — MIN_LINE_WIDTH=1.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, SWITCH_NODE=TRUE
CPUIMVP_LGATE1 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE_NODE=TRUE

376S0930

CRITICAL Q7515 IRF6798MTRPBF DIRECTFET-MX

NOSTUFF R7512 2.2 5% 1/10W MF-LF 603

CPUIMVP_PH1_SNUB — DIDT=TRUE
NOSTUFF C7512 0.001UF 10% 50V CERM 402

CPUIMVP_ISNS1_P
CPUIMVP_ISNS1_N

R7513 46.4 1% 1/10W MF-LF 402
R7514 10.2 1% 1/16W MF-LF 402

CPUIMVP_ISUM_N

NOSTUFF C7571 330PF 10% 50V CERM 402

CPUIMVP_ISUM1_P

PHASE 2

376S0872

CRITICAL Q7510 IRF6723M2DPBF DIRECTFET-MA

CRITICAL L7520 0.36UH-20%-40A-0.000750HM PIMA104E-SM 152S1019

CRITICAL R7520 0.00075 1% 1W MF 0612

PPVCORE_S0_CPU_PH2_L → PPVCORE_S0_CPU_PH2 → PPVCORE_S0_CPU

THESE TWO CAPS ARE FOR EMC

CRITICAL C7523 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7524 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7525 10UF 10% 16V X5R-CERM 0805
CRITICAL C7526 10UF 10% 16V X5R-CERM 0805
CRITICAL C7527 1UF 10% 16V X5R 402
CRITICAL C7528 0.001UF 10% 50V X7R 402
C7529 0.001UF 10% 50V X7R 402

C7521 0.22UF 10% 16V CERM 402

R7521 0 5% 1/10W MF-LF 402

CPUIMVP_BOOT2_RC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.25 MM
DIDT=TRUE

CPUIMVP_BOOT2 — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE
CPUIMVP_UGATE2 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE_NODE=TRUE
CPUIMVP_PHASE2 — MIN_LINE_WIDTH=1.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, SWITCH_NODE=TRUE
CPUIMVP_LGATE2 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE_NODE=TRUE

376S0930

CRITICAL Q7525 IRF6798MTRPBF DIRECTFET-MX

NOSTUFF R7522 2.2 5% 1/10W MF-LF 603

CPUIMVP_PH2_SNUB — DIDT=TRUE
NOSTUFF C7522 0.001UF 10% 50V CERM 402

CPUIMVP_ISNS2_P
CPUIMVP_ISNS2_N

R7523 46.4 1% 1/10W MF-LF 402
R7524 10.2 1% 1/16W MF-LF 402

CPUIMVP_ISUM_N

NOSTUFF C7572 330PF 10% 50V CERM 402

CPUIMVP_ISUM2_P

PHASE 3

376S0772

CRITICAL Q7530 IRF6710 S1

THESE TWO CAPS ARE FOR EMC

CRITICAL C7533 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7534 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7535 10UF 10% 16V X5R-CERM 0805
CRITICAL C7536 10UF 10% 16V X5R-CERM 0805
CRITICAL C7537 1UF 10% 16V X5R 402
CRITICAL C7538 0.001UF 10% 50V X7R 402
C7539 0.001UF 10% 50V X7R 402

CRITICAL R7530 0.00075 1% 1W MF 0612

CRITICAL L7530 0.36UH-20%-40A-0.000750HM PIMA104E-SM 152S1019

SWITCH_NODE=TRUE
PPVCORE_S0_CPU_PH3_L → PPVCORE_S0_CPU_PH3 → PPVCORE_S0_CPU

CPUIMVP_ISNS3_P
CPUIMVP_ISNS3_N

R7533 46.4 1% 1/10W MF-LF 402
R7534 10.2 1% 1/16W MF-LF 402

CPUIMVP_ISUM_N

NOSTUFF C7573 330PF 10% 50V CERM 402

CPUIMVP_ISUM3_P

CPUIMVP_BOOT3_RC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.25 MM
DIDT=TRUE

R7531 0 5% 1/10W MF-LF 402

C7531 0.22UF 10% 16V CERM 402

NOSTUFF R7532 2.2 5% 1/10W MF-LF 603

CPUIMVP_PH3_SNUB — DIDT=TRUE
NOSTUFF C7532 0.001UF 10% 50V CERM 402

CRITICAL Q7535 IRF6798MTRPBF DIRECTFET-MX

376S0930

PP5V_S0

R7547 10K 5% 1/16W MF-LF 402

C7541 1UF 10% 16V X5R 402

U7541 MAX17491 TQFN CRITICAL
VDD, PWN, SKIP*, BST, DH, LX, DL, GND, THRM PAD

CPUIMVP_PWM3
CPUIMVP_SKIP

CPUIMVP_BOOT3 — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE
CPUIMVP_UGATE3 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE_NODE=TRUE
CPUIMVP_PHASE3 — MIN_LINE_WIDTH=1.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, SWITCH_NODE=TRUE
CPUIMVP_LGATE3 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE_NODE=TRUE

Additonal Input Bulk Caps

CRITICAL C7561 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7562 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7563 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7564 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7565 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7566 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7567 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7568 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7569 68UF 20% 16V POLY-TANT CASE-D2E-SM

AXG PHASE

PPVIN_S5_HS_COMPUTING_ISNS

THESE TWO CAPS ARE FOR EMC

CRITICAL C7553 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7554 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7555 10UF 10% 16V X5R-CERM 0805
CRITICAL C7556 10UF 10% 16V X5R-CERM 0805
CRITICAL C7557 1UF 10% 16V X5R 402
CRITICAL C7558 0.001UF 10% 50V X7R 402
C7559 0.001UF 10% 50V X7R 402

CRITICAL Q7550 CSD58864Q5D SON5X6
TG, TGR, BG, VIN, VSW, PGND

376S0906

CRITICAL L7550 0.36UH-20%-40A-0.000750HM PIMA104E-SM 152S1019

CRITICAL R7550 0.00075 1% 1W MF 0612

CPUIMVP_VSWG — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM, SWITCH_NODE=TRUE

PPVCORE_S0_AXG_L → PPVCORE_S0_AXG

CPUIMVP_ISNS1G_P
CPUIMVP_ISNS1G_N

R7552 2.2 5% 1/10W MF-LF 603
R7553 46.4 1% 1/10W MF-LF 402
R7554 10.2 1% 1/16W MF-LF 402

CPUIMVP_AXG_SNUB — DIDT=TRUE
NOSTUFF C7552 0.001UF 10% 50V CERM 402

CPUIMVP_ISUMG_N

NOSTUFF C7574 330PF 10% 50V CERM 402

CPUIMVP_ISUMG_P

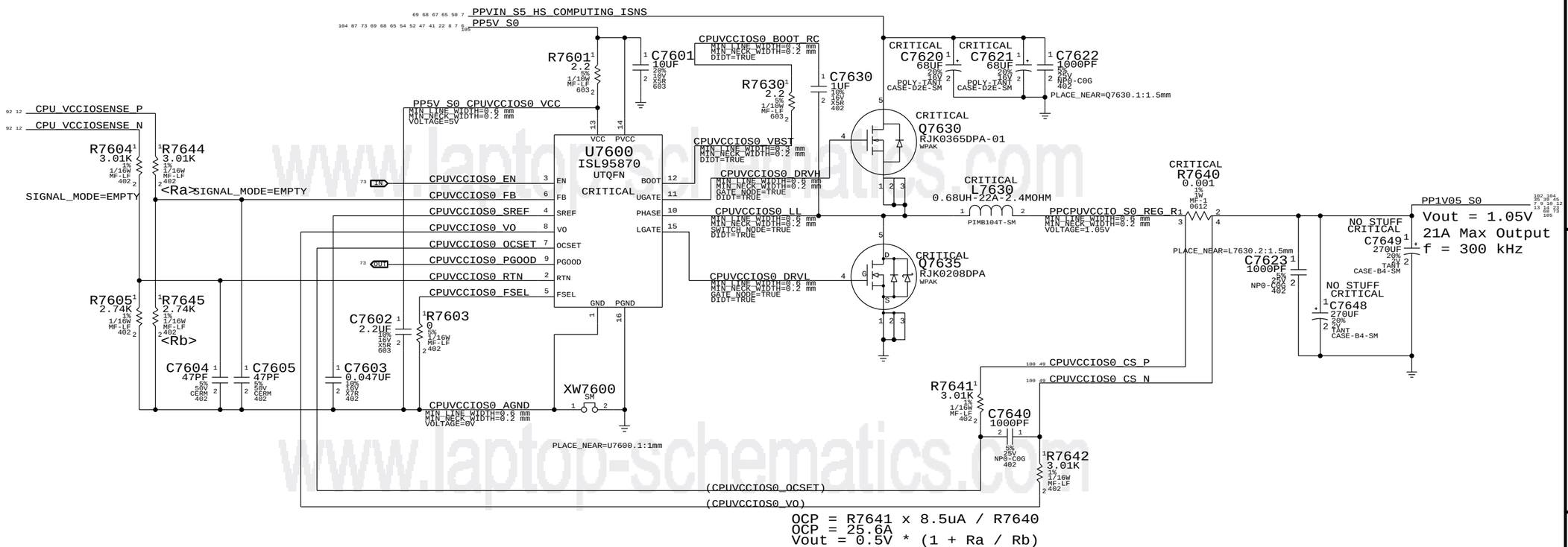
R7556 0 5% 1/16W MF-LF 402 — CPUIMVP_BOOT1G_R
C7551 0.22UF 10% 16V CERM 402
R7555 4.7 5% 1/10W MF-LF 402 — CPUIMVP_UGATE1G_R

CPUIMVP_BOOT1G — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE
CPUIMVP_UGATE1G — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE_NODE=TRUE
CPUIMVP_PHASE1G — MIN_LINE_WIDTH=1.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, SWITCH_NODE=TRUE
CPUIMVP_LGATE1G — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE_NODE=TRUE

SYNC_MASTER=K92_ERIC	SYNC_DATE=09/27/2010
PAGE TITLE	CPU IMVP7 & AXG VCore Output
Apple Inc.	DRAWING NUMBER: SIZE D
	REVISION:
	BRANCH:
	PAGE: 75 OF 132
	SHEET: 69 OF 105

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

CPU VCCIO (1.05V S0) Regulator



SYNC_MASTER=K92_ERIC SYNC_DATE=09/23/2010

PAGE TITLE: CPU VCCIO (1.05V) Power Supply

Apple Inc.

DRAWING NUMBER | SIZE: D

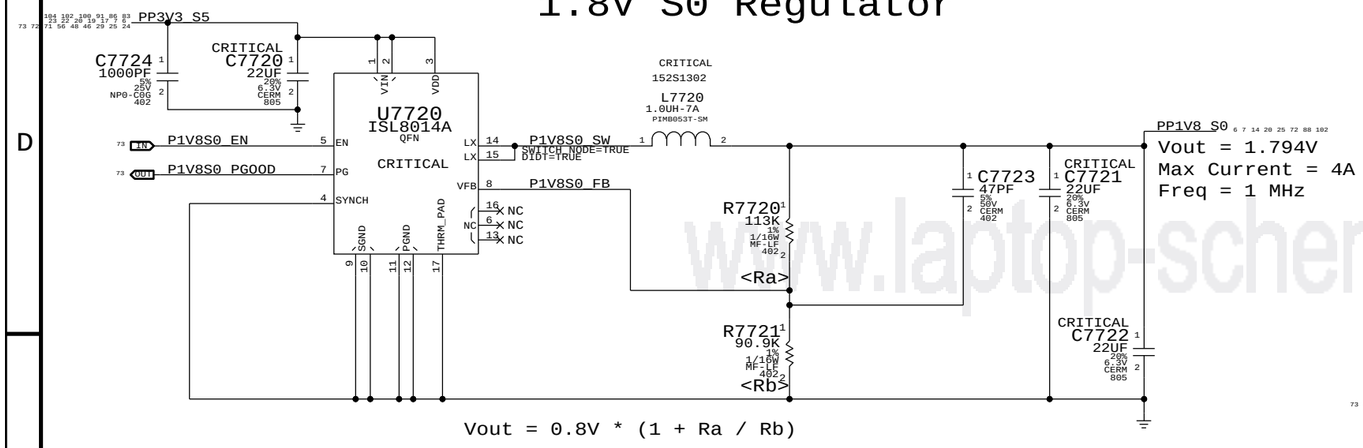
REVISION

BRANCH

PAGE: 76 OF 132

SHEET: 70 OF 105

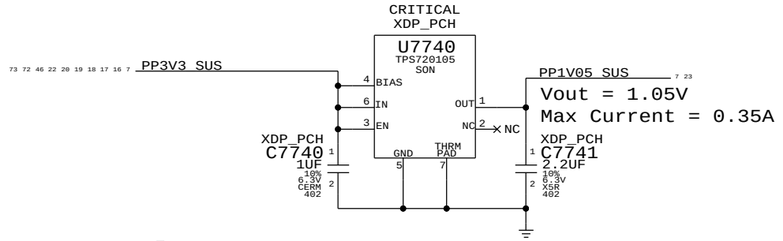
1.8V S0 Regulator



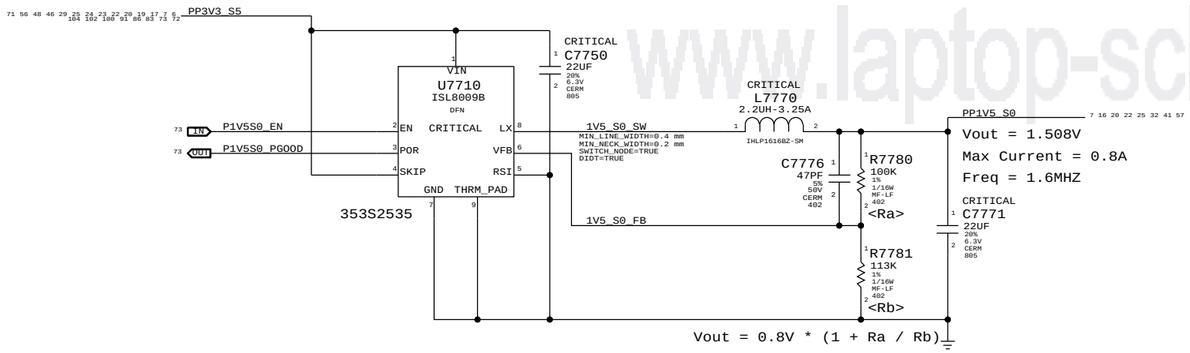
Vout = 0.8V * (1 + Ra / Rb)

1.05V S5 LDO

Cougar Point-M requires JTAG pull-ups to be powered at 1.05V in S5.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.

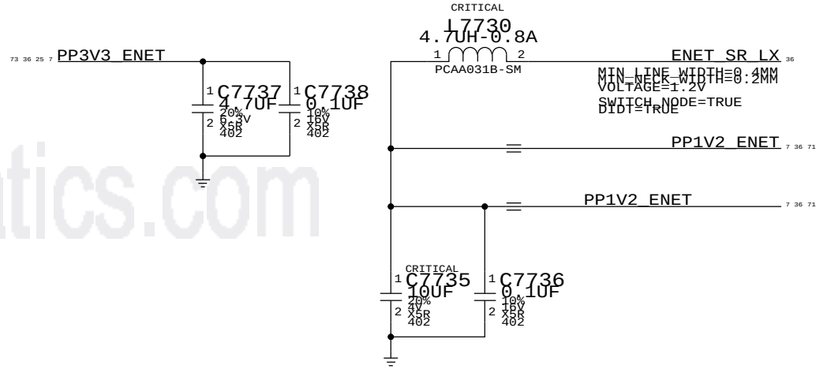


1.5V S0 Regulator

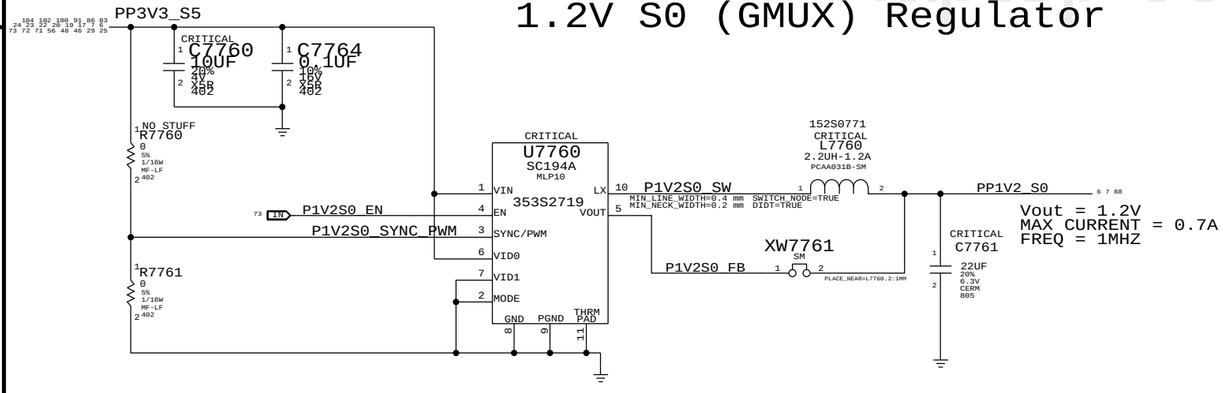


Vout = 0.8V * (1 + Ra / Rb)

CAESAR IV 1.2V INT.VR CMPTS



1.2V S0 (GMUX) Regulator



SYNC_MASTER=K91_CHANG SYNC_DATE=07/21/2010

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: SIZE D

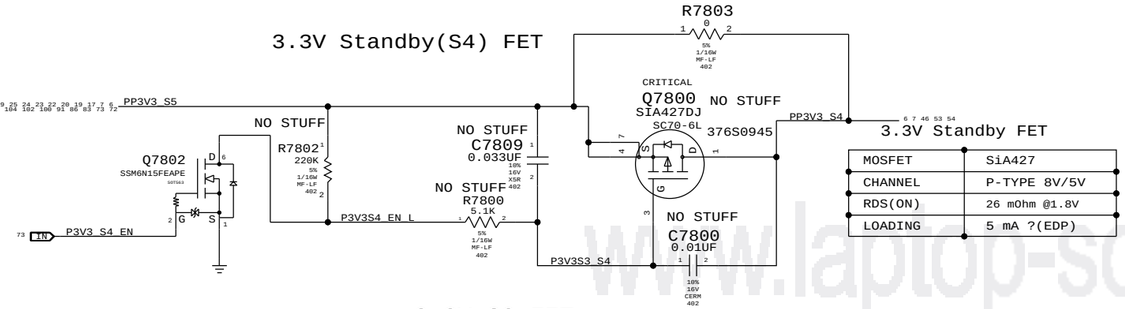
REVISION:

BRANCH:

PAGE: 77 OF 132

SHEET: 71 OF 105

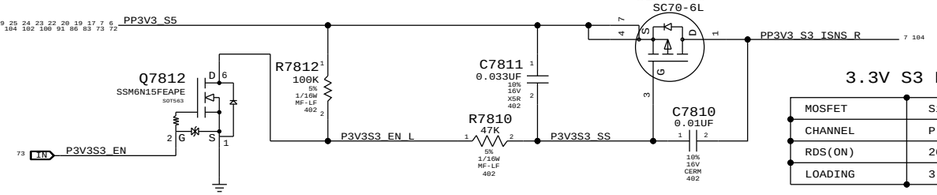
3.3V Standby(S4) FET



3.3V Standby FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	5 mA ?(EDP)

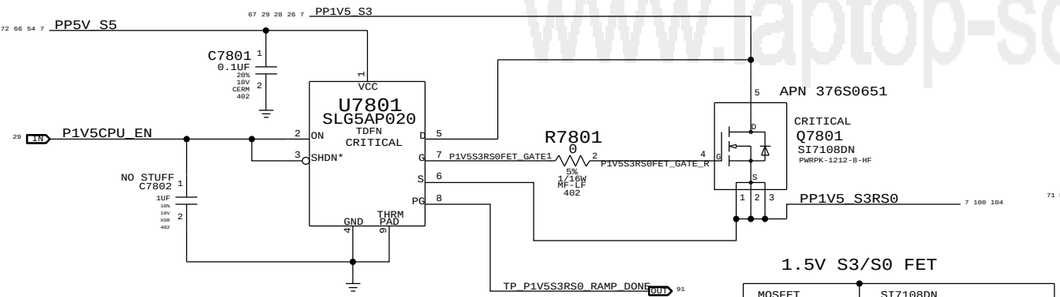
3.3V S3 FET



3.3V S3 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3 A (EDP)

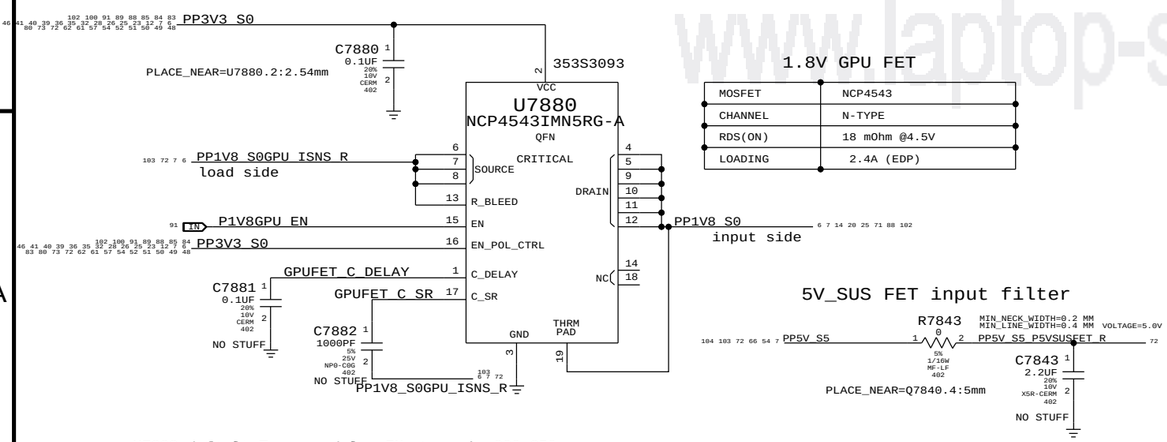
1.5V S3/S0 FET



1.5V S3/S0 FET

MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	5 A (EDP)

1.8V GPU FET



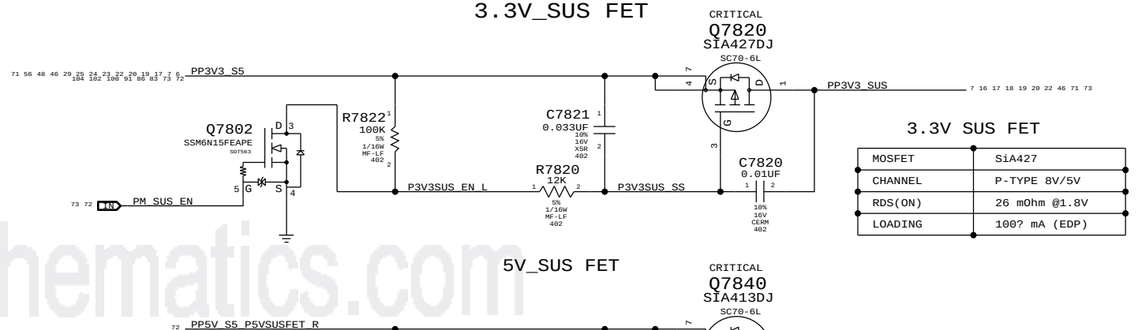
1.8V GPU FET

MOSFET	NCP4543
CHANNEL	N-TYPE
RDS(ON)	18 mOhm @4.5V
LOADING	2.4A (EDP)

5V_SUS FET input filter

U7880 default Turn on delay EN--> on is 200~650us.

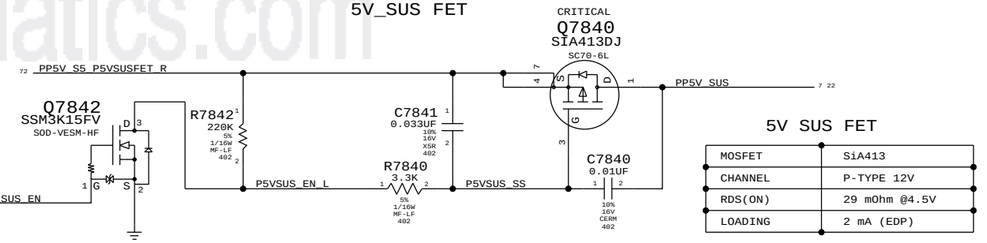
3.3V_SUS FET



3.3V SUS FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

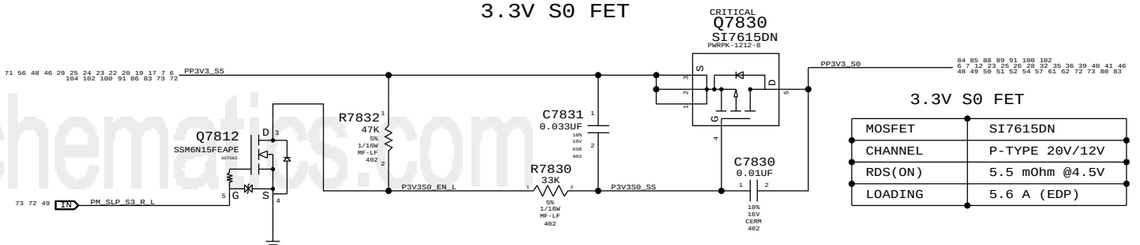
5V_SUS FET



5V SUS FET

MOSFET	SiA413
CHANNEL	P-TYPE 12V
RDS(ON)	29 mOhm @4.5V
LOADING	2 mA (EDP)

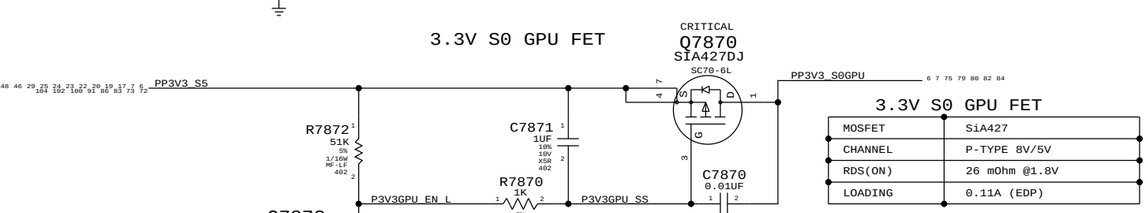
3.3V S0 FET



3.3V S0 FET

MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5.6 A (EDP)

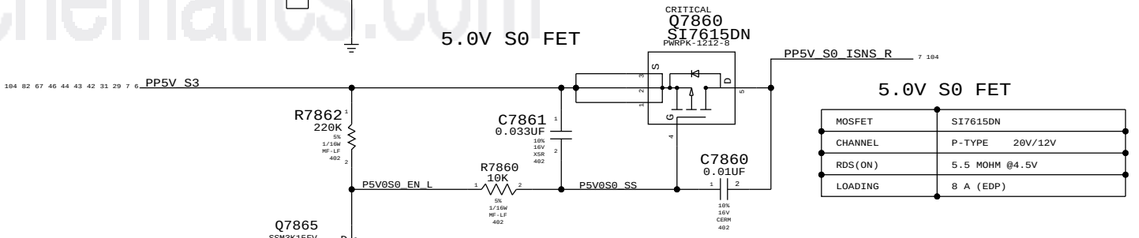
3.3V S0 GPU FET



3.3V S0 GPU FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.11A (EDP)

5.0V S0 FET



5.0V S0 FET

MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	8 A (EDP)

SYNC_MASTER=K91_MLB SYNC_DATE=10/18/2010

PAGE TITLE: Power FETs

Apple Inc.

DRAWING NUMBER | SIZE: D

REVISION

BRANCH

PAGE: 78 OF 132

SHEET: 72 OF 105

S5 Rail Enables & PGOOD

SMC_PM_G2_EN (OUT) → R7940 100 → P3V3S5_EN (MAKE_BASE=TRUE) → P3V3S5_EN (OUT)
PLACE_NEAR=U7201.21:7mm
C7942 0.0033UF 10% 50V CERM 402 NO STUFF

PP3V42_G3H
PLACE_NEAR=U7201.20:7mm
R7941 100K 5% 1/10W MF-LF 402

S5_PWRGD (OUT) → S5_PWRGD (MAKE_BASE=TRUE) (OUT)
S5_PWRGD (old name RSMRST_PWRGD)-->SMC
SMC-->PM_DSW_PWRGD

State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	0	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

3.3V,5V S3 ENABLE

PM_SLP_S4_L (IN) MAKE_BASE=TRUE
PM_SLP_S4_L:100K pull down in PCH page
(PM_SLP_S4_L)
R7911 5.1K 5% 1/16W MF-LF 402 PLACE_NEAR=U7300.16:6mm
R7912 0 5% 1/16W MF-LF 402 PLACE_NEAR=Q7812.2:6mm
R7913 3.3K 5% 1/16W MF-LF 402
PM_SLP_S4_L (OUT) PLACE_NEAR=U5701.4:6mm
TPAD_VBUS_EN (OUT)
P3V3S3_EN (MAKE_BASE=TRUE) P3V3S3_EN (OUT)
DDRREG_EN (MAKE_BASE=TRUE) DDRREG_EN (OUT)
C7910 0.47UF 10% 6.3V CERM-X5R 402
C7912 NO STUFF 0.47UF 10% 6.3V CERM-X5R 402

3.3V/5.0V S4 ENABLE

NO STUFF
R7916 0 5% 1/16W MF-LF 402 PLACE_NEAR=U1800.G18:5mm
PM_SLP_S5_L (IN) → P3V3_S4_EN (MAKE_BASE=TRUE) → P3V3_S4_EN (OUT)
PM_SLP_S5_L:100K pull down on PCH page

S0 ENABLE

R7978 100 5% 1/16W MF-LF 402
PM_SLP_S3_L (IN)
PM_SLP_S3_L:100K pull down in PCH page
(PM_SLP_S3_R_L)
R7987 33K 5% 1/16W MF-LF 402 PLACE_NEAR=U7100.15:6mm
R7981 20K 5% 1/16W MF-LF 402 PLACE_NEAR=U7600.3:6mm
R7985 20K 5% 1/16W MF-LF 402 PLACE_NEAR=U7760.4:6mm
R7988 10K 5% 1/16W MF-LF 402
R7986 5.1K 5% 1/16W MF-LF 402 PLACE_NEAR=U7720.5:6mm
PM_SLP_S3_R_L (MAKE_BASE=TRUE) → PM_SLP_S3_R_L (OUT) ×3
P1V8S0_EN (MAKE_BASE=TRUE) P1V8S0_EN (OUT)
P1V5S0_EN (MAKE_BASE=TRUE) P1V5S0_EN (OUT)
P1V2S0_EN (MAKE_BASE=TRUE) P1V2S0_EN (OUT)
CPUVCCIOS0_EN (MAKE_BASE=TRUE) CPUVCCIOS0_EN (OUT)
PVCCSA_EN (MAKE_BASE=TRUE) PVCCSA_EN (OUT)
C7987 C7981 C7985 1UF C7988 C7986 0.47UF 10% 6.3V CERM-X5R 402

CPUVCORE ENABLE

ALL_SYS_PWRGD (IN)
R7974 0 5% 1/16W MF-LF 402 PLACE_NEAR=U7400.7:5mm
CPUIMVP_VR_ON (OUT)
NO STUFF
R7976 0 5% 1/16W MF-LF 402 PLACE_NEAR=U7400.7:5mm
CPUVCCIOS0_PGOOD (IN)
R7975 0 5% 1/16W MF-LF 402 PLACE_NEAR=U7400.7:5mm
PM_PECI_PWRGD (OUT)

3.3V/5.0V Sus ENABLE

PP3V3_S5
PLACE_NEAR=U7940.1:2.3mm
C7940 0.1uF 20% 10V CERM 402
U7940 74AUP1G3208 SOT891 (VCC, A, B, C, Y, GND)
SMC_BATLOW_L:100K pull up on SMC page
SMC_BATLOW_L (IN)
PM_SLP_SUS_L:100K pull down on PCH page
PM_SLP_SUS_L (IN)
PM_SUS_EN (MAKE_BASE=TRUE) PM_SUS_EN (OUT) ×2
NO STUFF
R7917 0 5% 1/16W MF-LF 402

CHGR VFRQ Generation

PP3V42_G3H
R7931 100K 5% 1/16W MF-LF 402
CHGR_VFRQ (OUT)
Q7931 SSM3K15FV SOD-VESM-HF
VFRQ Low: Fix Frequency
VFRQ High: Variable Frequency

S0 Rail PGOOD (BJT Version)

PP3V3_S5
PP3V5_S0
PP1V5_S3RS0_CPUDDR
PP1V05_S0
R7951 15.0K 1% 1/16W MF-LF 402
R7952 7.15K 1% 1/16W MF-LF 402
R7953 1K 5% 1/16W MF-LF 402
R7954 1K 5% 1/16W MF-LF 402
R7955 1K 5% 1/16W MF-LF 402
R7956 150K 1% 1/16W MF-LF 402
VMON_3V3_DIV, VMON_Q2_BASE, VMON_Q3_BASE, VMON_Q4_BASE
S0PGD_C
Q7950 ASMCC0179 DFN2015H4-8 (Q1, Q2, Q3, Q4) CRITICAL
NC, NC
ALL_SYS_PWRGD (IN)
353S2809 S0PGD_BJT_GND_R
R7957 100 5% 1/16W MF-LF 402
Worst-Case Thresholds:
Q2: 0.XXXV
Q3: 0.640V
3.3V w/Divider: 2.345V
Q4: 0.660V

3.3V SUS Detect

PP3V3_S5
PLACE_NEAR=U7930.6:2.3mm
C7930 0.1uF 20% 16V CERM 402
No stuff C7931, 12ms Min delay time
U7930 Sense input threhold is 3.07V
U7930 TPS3808G33DBVRG4 SOT23-6 (SENSE, RESET*, MR*, VDD, CT, GND) CRITICAL
R7933 100K 5% 1/16W MF-LF 402
PP3V3_SUS
PM_RSMRST_L (OUT)
PM_RSMRST_L goes to U1800.C21
C7931 0.001UF 10% 50V CERM 402 NO STUFF

ENET Enable Generation

3.3V ENET FET

PP3V3_S3
Q7922 NTR4101P SOT-23-HF (CRITICAL)
PP3V3_ENET
C7921 0.033UF 10% 16V CERM 402
C7922 0.01UF 10% 16V CERM 402
R7921 10K 5% 1/16W MF-LF 402
R7922 100K 5% 1/16W MF-LF 402
PM_SLP_S3_ENET
P3V3ENET_SS
Q7921 SSM3K15FV SOD-VESM-HF
"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

PM_SLP_S3_L (IN)
Q7925 2N7002DW-X-G SOT-363
WOL_EN (IN)
PM_WLAN_EN_L (OUT)
Q7925 2N7002DW-X-G SOT-363
AP_PWR_EN (IN)
AC_EN_L
(AC_EN_L)
Q7920 2N7002DW-X-G SOT-363
NO STUFF
R7929 0 5% 1/16W MF-LF 402
SMC_ADAPTER_EN (IN)
Q7920 2N7002DW-X-G SOT-363
(PM_SLP_S3_L)

S0 Rail PGOOD Circuitry (ISL Version in development)

Thresholds:
VDD: 2.734V-3.010V
V2MON: 2.815V-3.099V
V3MON: 0.572V-0.630V
V4MON: 0.572V-0.630V

PP3V3_S0
PP5V_S0
PP1V5_S3RS0_CPUDDR
PP1V05_S0
S0PGOOD_ISL
R7960 6.04K 1%
R7970 10K 1%
R7972 6.04K 1%
R7961 15.0K 1%
R7971 10K 1%
R7973 15.0K 1%
VMON_PP5V_DIV, VMON_PP1V5_DIV, VMON_PP1V05_DIV
C7960 0.1uF 20% 10V CERM 402
U7960 ISL88042IRTEZ TDFN (IPU) CRITICAL (VDD, V2MON, V3MON, V4MON, MR*, RST*, GND, THRM_PAD)
NC
353S2310
S0PGOOD_ISL R7962 330 5% 1/16W MF-LF 402
ALL_SYS_PWRGD_R
ALL_SYS_PWRGD (OUT)
P1V5S0_PGOOD (IN) from U7710
R7968 100
P1V8S0_PGOOD (IN)
R7967 10K
R7966 100
P5VS3_PGOOD (IN)
R7965 100
CPUVCCIOS0_PGOOD (IN)
R7964 100
PVCCSA_PGOOD (IN)
R7963 100

SMC_S4_WAKESRC_EN (MAKE_BASE=TRUE) SMC_S4_WAKESRC_EN (OUT)

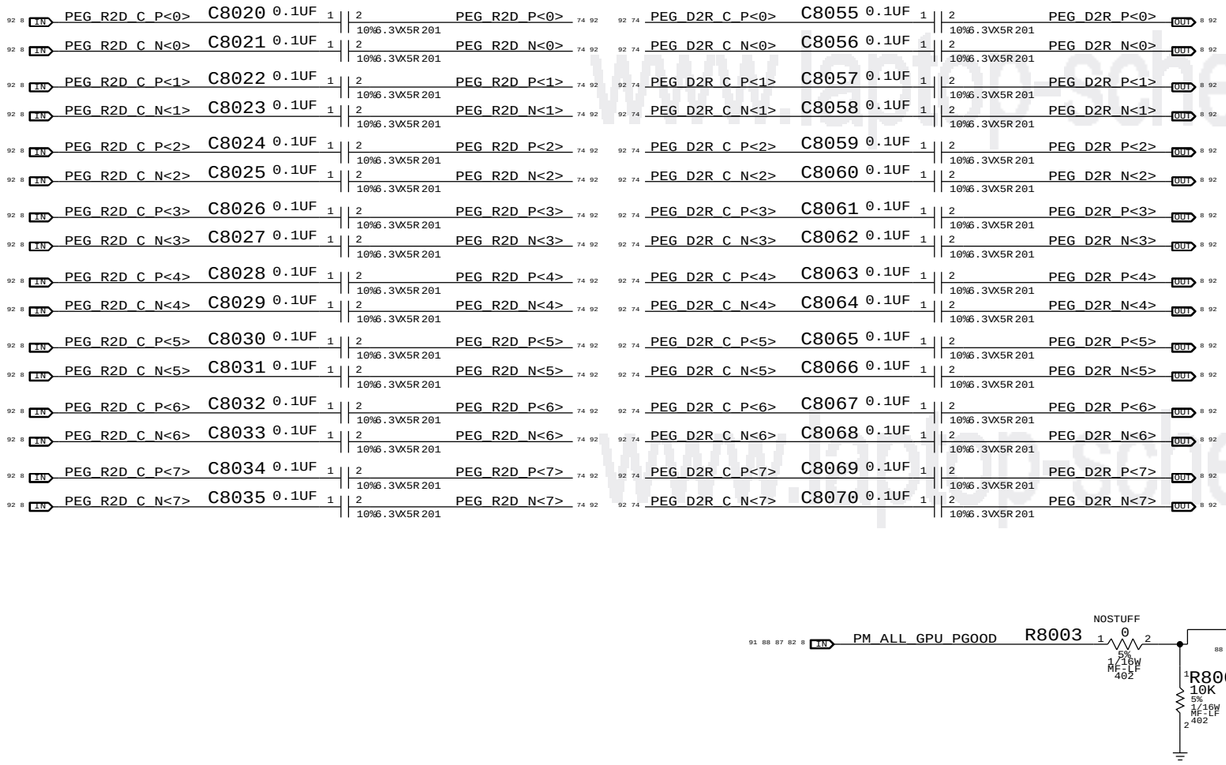
SYNC_MASTER=K92_YUAN SYNC_DATE=07/22/2010
PAGE TITLE: Power Control 1/ENABLE
Apple Inc.
DRAWING NUMBER: SIZE D
REVISION:
BRANCH:
PAGE: 79 OF 132
SHEET: 73 OF 105

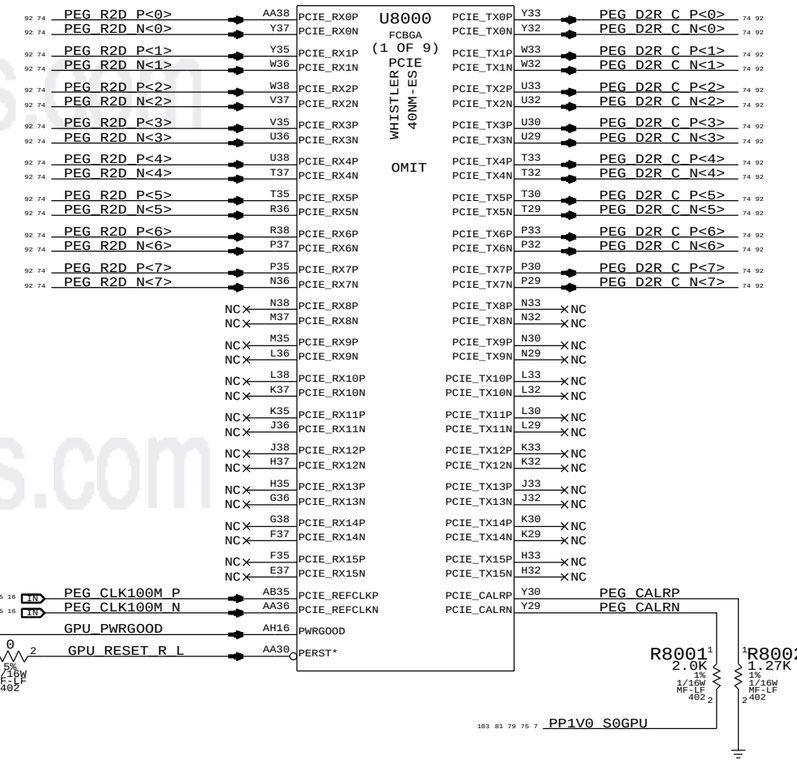
Page Notes

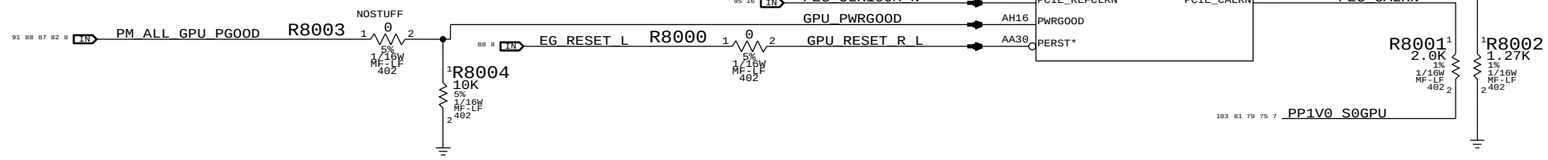
Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)







SYNC_MASTER=K91_MLB SYNC_DATE=10/19/2010

PAGE TITLE: Whistler PCI-E

Apple Inc.

DRAWING NUMBER | SIZE: D

REVISION

BRANCH

PAGE: 80 OF 132

SHEET: 74 OF 105

Page Notes

Power aliases required by this page:

- =PPVCORE_GPU
- =PP1V5R1V35_GPU_FB_VDDR1
- =PP1V8_GPU_VDD_CT
- =PP1V0_GPU_PLL
- =PP3V3_GPU_VDDR3
- =PP3V3_GPU_VDDR4
- =PP1V8_GPU_MEM_PLL
- =PP1V8_GPU_PLL
- =PP1V8_GPU_PCIE_VDDR
- =PP1V0_GPU_PCIE_VDDC

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

PP1V5R1V35_GPU_FB_ISNS — TBD mA
C8100 10UF 20% 10V X5R 603
C8101 10UF 20% 10V X5R 603
C8102 10UF 20% 10V X5R 603
C8103 10UF 20% 10V X5R 603
C8104 10UF 20% 10V X5R 603
C8105 1UF 10% 25V X5R 402
C8106 1UF 10% 25V X5R 402
C8107 1UF 10% 25V X5R 402
C8108 1UF 10% 25V X5R 402
C8109 1UF 10% 25V X5R 402
C8110 1UF 10% 25V X5R 402
C8111 1UF 10% 25V X5R 402
C8112 1UF 10% 25V X5R 402
C8113 1UF 10% 25V X5R 402
C8114 1UF 10% 25V X5R 402
C8115 0.1UF 10% 6.3V X5R 201
C8116 0.1UF 10% 6.3V X5R 201
C8117 0.1UF 10% 6.3V X5R 201
C8118 0.1UF 10% 6.3V X5R 201
C8119 0.1UF 10% 6.3V X5R 201
C8120 0.1UF 10% 6.3V X5R 201
C8121 0.1UF 10% 6.3V X5R 201
C8122 0.1UF 10% 6.3V X5R 201
C8123 0.1UF 10% 6.3V X5R 201
C8124 0.1UF 10% 6.3V X5R 201

L8120 120OHM-0.3A 0402 CRITICAL
PP1V8_S0GPU
PP1V8_GPU_VDD_CT — 219mA
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
C8125 10UF 20% 10V X5R 603
C8126 1UF 10% 25V X5R 402
C8127 1UF 10% 25V X5R 402
C8128 1UF 10% 25V X5R 402
C8129 0.1UF 10% 6.3V X5R 201

L8130 470OHM-1A-150MOHM 0603 CRITICAL
PP1V0_S0GPU
PP1V0_GPU_PLL
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1V
C8130 10UF 20% 10V X5R 603
C8131 1UF 10% 25V X5R 402
C8132 0.1UF 10% 6.3V X5R 201
GND_GPU_PLL

PP3V3_S0GPU — 60 mA
C8133 10UF 20% 10V X5R 603
C8134 1UF 10% 25V X5R 402
C8135 1UF 10% 25V X5R 402
C8136 1UF 10% 25V X5R 402

L8131 4700HM-1A-150MOHM 0603 CRITICAL
PP1V8_S0GPU
PP1V8_GPU_MEM_PLL
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
C8137 10UF 20% 10V X5R 603
C8138 1UF 10% 25V X5R 402
C8139 1UF 10% 25V X5R 402
C8140 0.1UF 10% 6.3V X5R 201
C8141 0.1UF 10% 6.3V X5R 201

PP1V8_GPU_VDDR4 — TBD mA

L8132 120OHM-0.3A 0402 CRITICAL
PP1V8_S0GPU
PP1V8_GPU_PLL — 75mA
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
PP1V0_GPU_PLL — 120mA
GND_GPU_PLL
C8142 1UF 10% 25V X5R 402
C8143 1UF 10% 25V X5R 402
C8144 0.1UF 10% 6.3V X5R 201
XW8100 SM
GPU_VDD_SENSE
GPU_GND_SENSE

L8140 FERR-220-OHM-2A 0603 CRITICAL
PP1V8_S0GPU
PP1V8_GPU_PCIE_VDDR — 504mA
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
C8145 10UF 20% 10V X5R 603
C8146 1UF 10% 25V X5R 402
C8147 1UF 10% 25V X5R 402
C8148 1UF 10% 25V X5R 402
C8149 0.1UF 10% 6.3V X5R 201
C8150 0.1UF 10% 6.3V X5R 201

L8155 FERR-120-OHM-3A 0603 CRITICAL
PP1V0_S0GPU
PP1V0_GPU_PCIE_VDDC — 1920mA
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1V
C8151 10UF 20% 10V X5R 603
C8152 1UF 10% 25V X5R 402
C8153 1UF 10% 25V X5R 402
C8154 1UF 10% 25V X5R 402
C8155 1UF 10% 25V X5R 402
C8156 1UF 10% 25V X5R 402
C8157 1UF 10% 25V X5R 402
C8158 1UF 10% 25V X5R 402

U8000 WHISTLER 40NM-ES FCBGA (7 OF 9)

MEM I/O	VDDR1_AC7 … VDDR1_Y11	OMIT
CORE	VDD_CT_AF26 … VDD_CT_AG27	LEVEL TRNSL
I/O	VDDR3_AF23 … VDDR3_AG24	
I/O	VDDR4_AF13 … VDDR4_AG15	
I/O	VDDR4_AD12 … VDDR4_AG11	
	NC/VDDRHA, NC/VSSRHA, NC/VSSRHB, NC/VDDRHB	
PLL	MPV18_H7, MPV18_H8	150mA
PLL	SPV18	75mA
PLL	SPV10	120mA
PLL	SPVSS	
VOLT SENSE	FB_VDDC	GPU_VDD_SENSE
VOLT SENSE	FB_VDDCI	NC
VOLT SENSE	FB_GND	GPU_GND_SENSE
PCIE ISOLATED CORE I/O	PCIE_VDDR_AA31 … PCIE_VDDR_Y31	
PCIE ISOLATED CORE I/O	PCIE_VDDC_G30 … PCIE_VDDC_U28	

CRITICAL L8150 120OHM-0.3A 0402
PP1V8_S0GPU
PP1V8_GPU_VDDR4
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
C81C0 1UF 10% 25V X5R 402
C81C1 0.1UF 10% 6.3V X5R 201

PPVCORE_GPU

VDDC_AA15 … VDDC_Y28
C8160 C8161 C8162 C8163 C8164 C8165 C8166 C8167 C8168 C8169 1UF 10% 25V X5R 402
C8170 C8171 C8172 C8173 C8174 C8175 C8176 C8177 C8178 C8179 1UF 10% 25V X5R 402
C8180 C8181 C8182 C8183 C8184 C8185 C8186 C8187 C8188 C8189 1UF 10% 25V X5R 402
C8190 C8191 C8192 C8193 C8194 C8195 C8196 C8197 C8198 C8199 10UF 20% 10V X5R 603

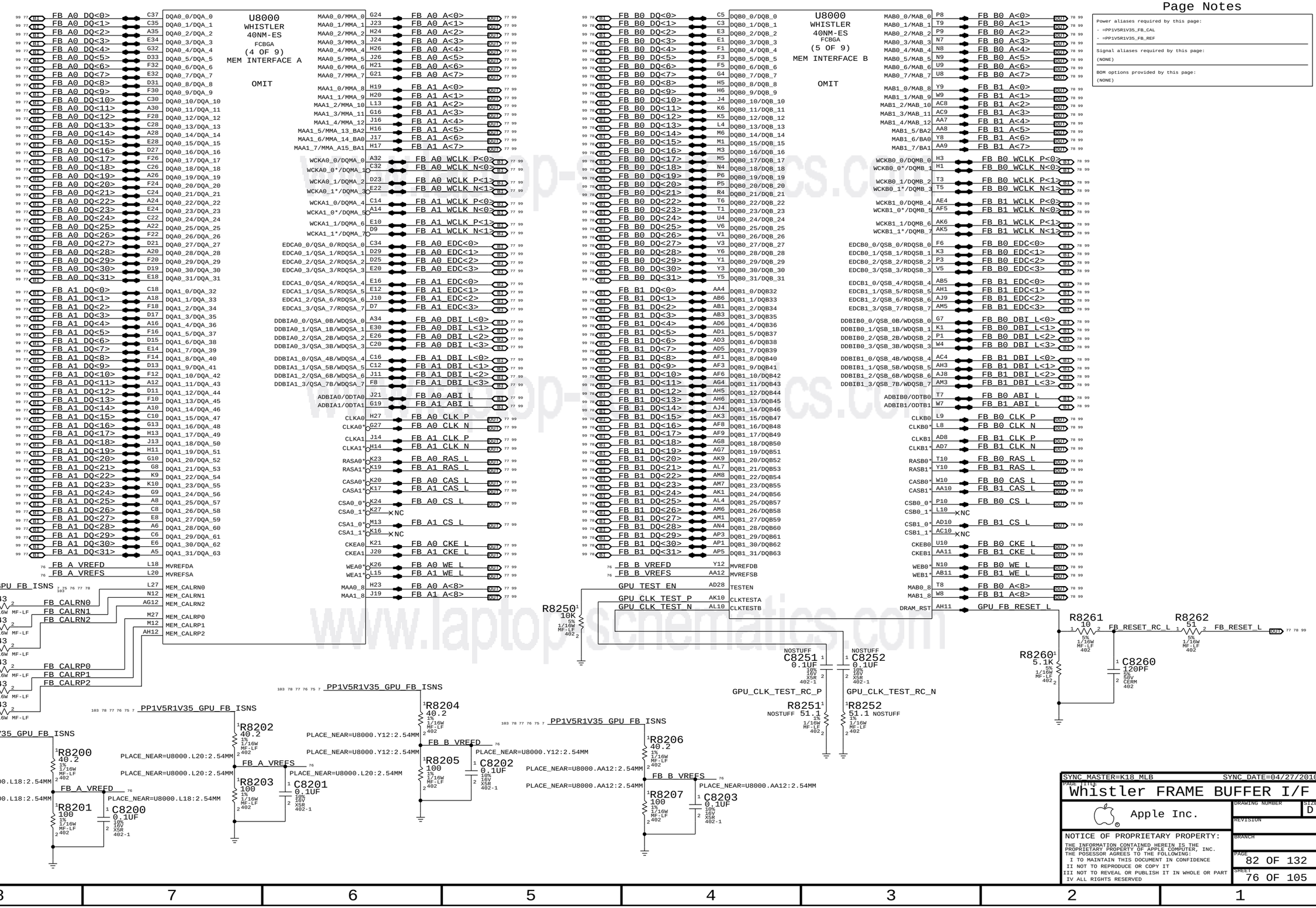
VDDCI_AA13 … VDDCI_Y13
C81A0 C81A1 C81A2 C81A3 C81A4 C81A5 C81A6 C81A7 C81A8 C81A9 1UF 10% 25V X5R 402
C81B0 C81B1 C81B2 10UF 20% 10V X5R 603

BIF_VDDC_N27
BIF_VDDC_T27

SYNC_MASTER=K92_BEN SYNC_DATE=06/03/2010
PAGE TITLE: Whistler CORE/FB POWER

Apple Inc.

DRAWING NUMBER — SIZE D
REVISION
BRANCH
PAGE 81 OF 132
SHEET 75 OF 105

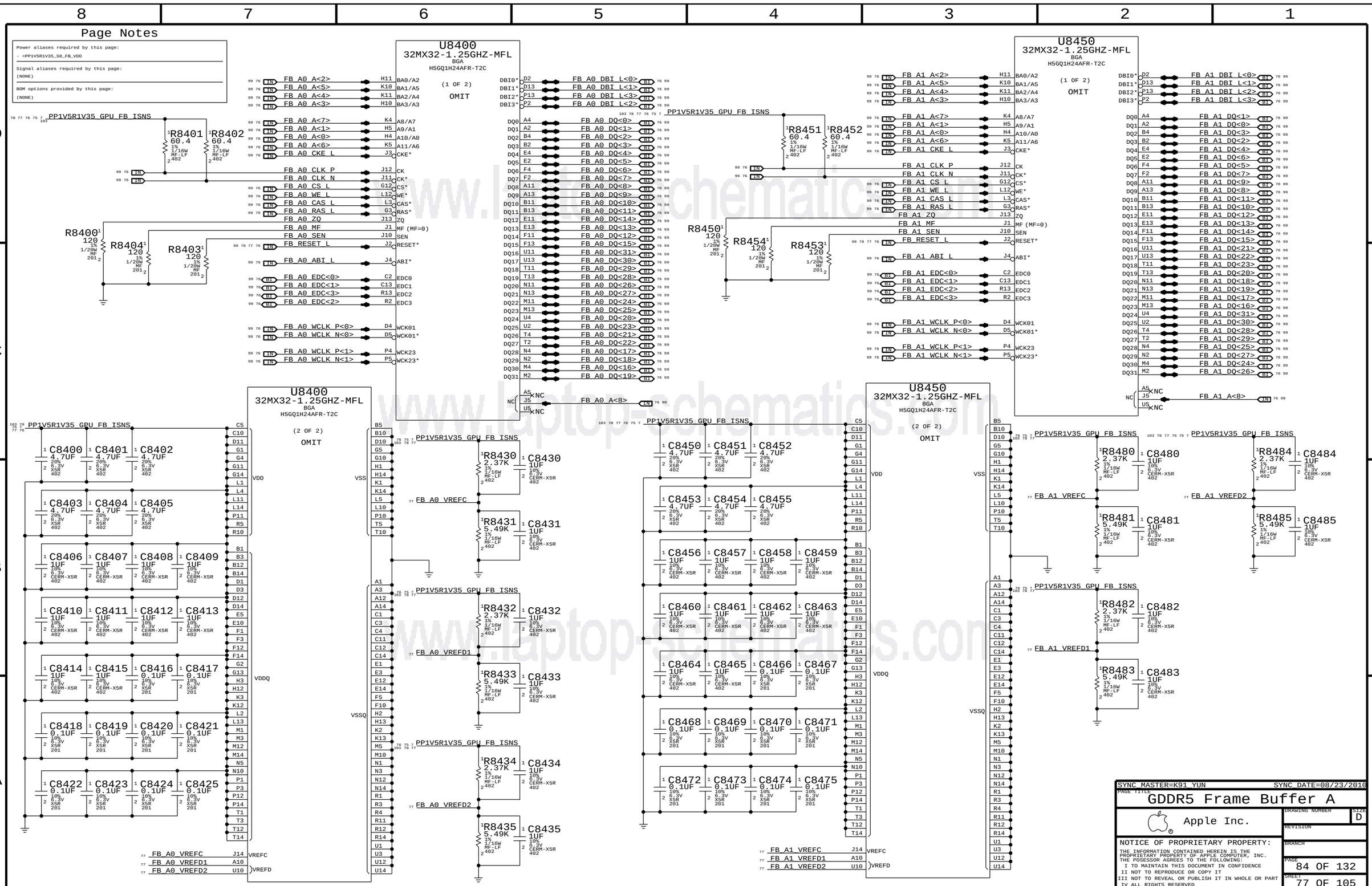

U8000
WHISTLER
40NM-ES
FCBGA
(4 OF 9)
MEM INTERFACE A
OMIT
U8000
WHISTLER
40NM-ES
FCBGA
(5 OF 9)
MEM INTERFACE B
OMIT
Page Notes
Power aliases required by this page:
- =PP1V5R1V35_FB_CAL
- =PP1V5R1V35_FB_REF
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)
PP1V5R1V35_GPU_FB_ISNS
R8210 243 402 1% 1/16W MF-LF
R8211 243 402 1% 1/16W MF-LF
R8212 243 402 1% 1/16W MF-LF
R8213 243 402 1% 1/16W MF-LF
R8214 243 402 1% 1/16W MF-LF
R8215 243 402 1% 1/16W MF-LF
R8200 40.2 1% 1/16W MF-LF 402
R8201 100 1% 1/16W MF-LF 402
C8200 0.1UF 10% 16V X5R 402-1
R8202 40.2 1% 1/16W MF-LF 402
R8203 100 1% 1/16W MF-LF 402
C8201 0.1UF 10% 16V X5R 402-1
R8204 40.2 1% 1/16W MF-LF 402
R8205 100 1% 1/16W MF-LF 402
C8202 0.1UF 10% 16V X5R 402-1
R8206 40.2 1% 1/16W MF-LF 402
R8207 100 1% 1/16W MF-LF 402
C8203 0.1UF 10% 16V X5R 402-1
R8250 10K 5% 1/16W MF-LF 402
R8251 51.1 1% 1/16W MF-LF 402 NOSTUFF
R8252 51.1 1% 1/16W MF-LF 402 NOSTUFF
C8251 0.1UF 10% 16V X5R 402-1 NOSTUFF
C8252 0.1UF 10% 16V X5R 402-1 NOSTUFF
R8260 5.1K 5% 1/16W MF-LF 402
R8261 10 5% 1/16W MF-LF 402
R8262 51 5% 1/16W MF-LF 402
C8260 120PF 5% 50V CERM 402
GPU_CLK_TEST_RC_P
GPU_CLK_TEST_RC_N
FB_RESET_RC_L
FB_RESET_L
PLACE_NEAR=U8000.L18:2.54MM
PLACE_NEAR=U8000.L20:2.54MM
PLACE_NEAR=U8000.Y12:2.54MM
PLACE_NEAR=U8000.AA12:2.54MM
SYNC_MASTER=K18_MLB
SYNC_DATE=04/27/2016
PAGE TITLE
Whistler FRAME BUFFER I/F
Apple Inc.
DRAWING NUMBER
SIZE
D
REVISION
BRANCH
PAGE
82 OF 132
SHEET
76 OF 105
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Page Notes

Power aliases required by this page:
- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC_MASTER=K91_YUN SYNC_DATE=08/23/2016

PAGE TITLE: GDDR5 Frame Buffer A

Apple Inc.

DRAWING NUMBER | SIZE D

REVISION

BRANCH

PAGE 84 OF 132

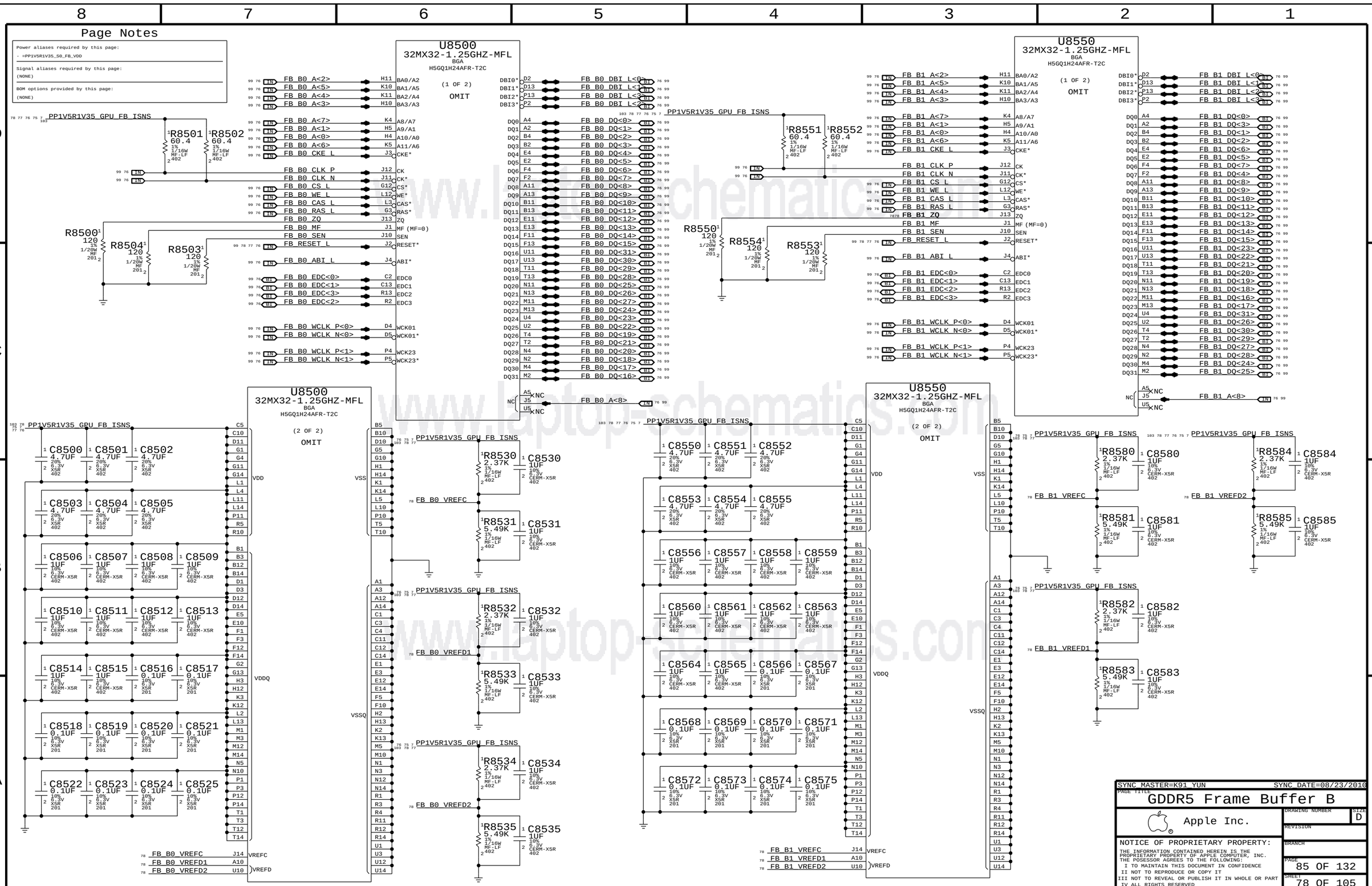
SHEET 77 OF 105

Page Notes

Power aliases required by this page:
- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC_MASTER=K91_YUN SYNC_DATE=08/23/2016

PAGE TITLE: GDDR5 Frame Buffer B

Apple Inc.

DRAWING NUMBER | SIZE D

REVISION

BRANCH

PAGE 85 OF 132

SHEET 78 OF 105

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_I2C
- =PP1V8_GPU_VREFG
- =PP1V8_GPU_DPLL
- =PP1V0_GPU_DPLL
- =PP1V0_GPU_TS

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE:

AMD STRAPS FOR IDENTIFYING VRAM VENDOR & SIZE FOR WHISTLER

K92 Samsung 1G - NOSTUFF R8613, NOSTUFF R8612, STUFF R8611
K92 Hynix 1G - STUFF R8613, NOSTUFF R8612, STUFF R8611

PP1V8_S0GPU
OMIT R8610 10K 5% 1/16W MF-LF 402
R8611 10K 5% 1/16W MF-LF 402
NOSTUFF R8612 10K 5% 1/16W MF-LF 402
VRAM_HYNIX R8613 10K 5% 1/16W MF-LF 402

PP3V3_S0GPU
R8600 4.7K 5% 1/16W MF-LF 402
R8601 4.7K 5% 1/16W MF-LF 402

PP1V8_S0GPU
R8602 499 1% 1/16W MF-LF 402
C8600 0.1UF 20% 10V X5R 402-1
R8603 249 1% 1/16W MF-LF 402

CRITICAL L8600 470OHM-1A-150MOHM 0603
PP1V8_S0GPU VOLTAGE=1.8V
C8601 10UF 20% 10V X5R 603
C8602 1UF 10% 10V X5R 402
C8603 0.1UF 10% 16V X5R 402-1
MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.8V

CRITICAL L8601 470OHM-1A-150MOHM 0603
PP1V0_S0GPU
C8604 10UF 20% 10V X5R 603
C8605 1UF 10% 25V X5R 402
C8606 0.1UF 10% 16V X5R 402-1
MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1V

XW8600 SM
GND_GPU_DPLL
MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=0V

L8602 120OHM-0.3A 0402
PP1V8_S0GPU
C8607 10UF 20% 10V X5R 603
C8608 1UF 10% 25V X5R 402
C8609 0.1UF 10% 16V X5R 402-1
XW8601 SM
GND_GPU_TSVSS
MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=0V

U8000 WHISTLER 40NM-ES FCBGA (2 OF 9)

TP_DVPCNTL_M<0>	AR8	DVPCNTL_MVP_0	
TP_DVPCNTL_M<1>	AU8	DVPCNTL_MVP_1	
TP_DVPCNTL<0>	AP8	DVPCNTL_0	
TP_DVPCNTL<1>	AW8	DVPCNTL_1	
TP_DVPCNTL<2>	AR3	DVPCNTL_2	
TP_DVPCLK	AR1	DVPCLK	
DVPDATA<0>	AU1	DVPDATA_0	
DVPDATA<1>	AU3	DVPDATA_1	
DVPDATA<2>	AW3	DVPDATA_2	
DVPDATA<3>	AP6	DVPDATA_3	
TP_DVPDATA<4>	AW5	DVPDATA_4	
TP_DVPDATA<5>	AU5	DVPDATA_5	
TP_DVPDATA<6>	AR6	DVPDATA_6	
TP_DVPDATA<7>	AW6	DVPDATA_7	
TP_DVPDATA<8>	AU6	DVPDATA_8	
TP_DVPDATA<9>	AT7	DVPDATA_9	
TP_DVPDATA<10>	AV7	DVPDATA_10	
TP_DVPDATA<11>	AN7	DVPDATA_11	
TP_DVPDATA<12>	AV9	DVPDATA_12	
TP_DVPDATA<13>	AT9	DVPDATA_13	
TP_DVPDATA<14>	AR10	DVPDATA_14	
TP_DVPDATA<15>	AW10	DVPDATA_15	
TP_DVPDATA<16>	AU10	DVPDATA_16	
TP_DVPDATA<17>	AP10	DVPDATA_17	
TP_DVPDATA<18>	AV11	DVPDATA_18	
TP_DVPDATA<19>	AT11	DVPDATA_19	
TP_DVPDATA<20>	AR12	DVPDATA_20	
TP_DVPDATA<21>	AW12	DVPDATA_21	
TP_DVPDATA<22>	AU12	DVPDATA_22	
TP_DVPDATA<23>	AP12	DVPDATA_23	
NC	AJ21	SWAPLOCKA	
NC	AK21	SWAPLOCKB	
GPU_I2C_SCL	AK26	SCL	I2C
GPU_I2C_SDA	AJ26	SDA	
GPU_PCIE_TX_PWR	AH20	GPIO_0	
GPU_GPIO_TX_DEEMP	AH18	GPIO_1	
GPU_PCIE_GEN2	AN16	GPIO_2	
GPU_SMB_DAT	AH23	GPIO_3_SMBDATA	
GPU_SMB_CLK	AJ23	GPIO_4_SMBCLK	
GPU_AC_BATT	AH17	GPIO_5_AC_BATT	
GPU_VCORE_VID0	AJ17	GPIO_6	
EG_BKLT_EN	AK17	GPIO_7_BLON	
GPU_ROM_SO	AJ13	GPIO_8_ROMSO	
GPU_ROM_SI	AH15	GPIO_9_ROMSI	
GPU_ROM_SCLK	AJ16	GPIO_10_ROMSCK	
GPU_CONFIG_0	AK16	GPIO_11	
GPU_CONFIG_1	AL16	GPIO_12	
GPU_CONFIG_2	AM16	GPIO_13	
DP_T29SNK0_HPD_GPU	AM14	GPIO_14_HPD2	
GPU_VCORE_VID1	AM13	GPIO_15_PWRCNTL_0	GPIO
GPU_VCORE_VID2	AK14	GPIO_16	
SMC_GFX_THROTTLE_R_L	AG30	GPIO_17_THERMAL_INT	
DP_T29SNK1_HPD_GPU	AN14	GPIO_18_HPD3	
SMC_GFX_OVERTEMP_R_L	AM17	GPIO_19_CTF	
GPU_VCORE_VID3	AL13	GPIO_20_PWRCNTL_1	
FBVDD_ALTVO	AJ14	GPIO_21_BB_EN	
GPU_ROM_CS_L	AK13	GPIO_22_ROMCS*	
PEX_CLKREQ_L_R	AN13	GPIO_23_CLKREQ*	
TP_GPU_JTAG_TRST_L	AM23	JTAG_TRST*	
TP_GPU_JTAG_TDI	AN23	JTAG_TDI	
TP_GPU_JTAG_TCK	AK23	JTAG_TCK	
TP_GPU_JTAG_TMS	AL24	JTAG_TMS	
TP_GPU_JTAG_TDO	AM24	JTAG_TDO	
NC_GPU_GENERICA	AJ19	GENERICA	
NC_GPU_GENERICB	AK19	GENERICB	
NC_GPU_GENERICC	AJ20	GENERICC	
DP_CA_DET_EG_R	AK20	GENERICD	
NC_GPU_GENERICE	AJ24	GENERICE_HPD4	
NC_GPU_GENERICF	AH26	GENERICF_HPD5	
NC_GPU_GENERICG	AH24	GENERICG_HPD6	
DP_EG_HPD	AK24	HPD1	
GPU_VREFG	AH13	VREFG	
PP1V8_GPU_DPLL 75mA (GND_GPU_DPLL)	AM32	DPLL_PVDD	PLL/CLK
	AN32	DPLL_PVSS	
PP1V0_GPU_DPLL 125mA	AN31	DPLL_VDDC	
NC	AV33	XTALIN	
NC	AU34	XTALOUT	
GPU_CLK27M	AW34	XO_IN	
GPU_CLK100M	AW35	XO_IN2	
GPU_TDIODE_P	AF29	DPLUS	THERMAL
GPU_TDIODE_N	AG29	DMINUS	
NC	AK32	TS_FDO	
NC	AL31	TSA/NC	
PP1V8_GPU_TSVDD 20mA (GND_GPU_TSVSS)	AJ32	TSVDD	DDC/AUX
	AJ33	TSVSS	

OMIT

MULTI GFX: DPA, DPB, DPC, DPD, DAC1, DAC2

TXCAP_DPA3P	AU24	DP_EXTA_ML_C_P<3>	OUT
TXCAM_DPA3N	AV23	DP_EXTA_ML_C_N<3>	OUT
TX0P_DPA2P	AT25	DP_EXTA_ML_C_P<2>	OUT
TX0M_DPA2N	AR24	DP_EXTA_ML_C_N<2>	OUT
TX1P_DPA1P	AU26	DP_EXTA_ML_C_P<1>	OUT
TX1M_DPA1N	AV25	DP_EXTA_ML_C_N<1>	OUT
TX2P_DPA0P	AT27	DP_EXTA_ML_C_P<0>	OUT
TX2M_DPA0N	AR26	DP_EXTA_ML_C_N<0>	OUT
TXCBP_DPB3P	AR30	DP_T29SNK0_ML_C_P<3>	OUT
TXCBM_DPB3N	AT29	DP_T29SNK0_ML_C_N<3>	OUT
TX3P_DPB2P	AV31	DP_T29SNK0_ML_C_P<2>	OUT
TX3M_DPB2N	AU30	DP_T29SNK0_ML_C_N<2>	OUT
TX4P_DPB1P	AR32	DP_T29SNK0_ML_C_P<1>	OUT
TX4M_DPB1N	AT31	DP_T29SNK0_ML_C_N<1>	OUT
TX5P_DPB0P	AT33	DP_T29SNK0_ML_C_P<0>	OUT
TX5M_DPB0N	AU32	DP_T29SNK0_ML_C_N<0>	OUT
TXCCP_DPC3P	AU14	DP_T29SNK1_ML_C_P<3>	OUT
TXCCM_DPC3N	AV13	DP_T29SNK1_ML_C_N<3>	OUT
TX0P_DPC2P	AT15	DP_T29SNK1_ML_C_P<2>	OUT
TX0M_DPC2N	AR14	DP_T29SNK1_ML_C_N<2>	OUT
TX1P_DPC1P	AU16	DP_T29SNK1_ML_C_P<1>	OUT
TX1M_DPC1N	AV15	DP_T29SNK1_ML_C_N<1>	OUT
TX2P_DPC0P	AT17	DP_T29SNK1_ML_C_P<0>	OUT
TX2M_DPC0N	AR16	DP_T29SNK1_ML_C_N<0>	OUT
TXCDP_DPD3P	AU20	NC	
TXCDM_DPD3N	AT19	NC	
TX3P_DPD2P	AT21	NC	
TX3M_DPD2N	AR20	NC	
TX4P_DPD1P	AU22	NC	
TX4M_DPD1N	AV21	NC	
TX5P_DPD0P	AT23	NC	
TX5M_DPD0N	AR22	NC	
R	AD39	NC	
R*	AD37	NC	
G	AE36	NC	
G*	AD35	NC	
B	AF37	NC	
B*	AE38	NC	
HSYNC	AC36	GPU_AUD_1	
VSYNC	AC38	GPU_AUD_0	
RSET	AB34	NC	
AVDD	AD34	PP1V8_S0GPU	
AVSSQ	AE34		
VDD1DI	AC33		
VSS1DI	AC34		
R2/NC	AC30	NC	
R2*/NC	AC31	NC	
G2/NC	AD30	NC	
G2*/NC	AD31	NC	
B2/NC	AF30	NC	
B2*/NC	AF31	NC	
C/NC	AC32	NC	
Y/NC	AD32	NC	
COMP/NC	AF32	NC	
H2SYNC/GENLK_CLK	AD29	NC	
V2SYNC/GENLK_VSYNC	AC29	NC	
VDD2DI/NC	AG31	NC	
VSS2DI/NC	AG32	NC	
A2VDD/NC	AG33	NC	
A2VDDQ/NC	AD33	NC	
A2VSSQ/TSVSSQ	AF33	GND_GPU_TVSSQ	
R2SET/NC	AA29	NC	
DDC1CLK	AM26	DP_EG_DDC_CLK	OUT
DDC1DATA	AM26	DP_EG_DDC_DATA	BI
AUX1P	AM27	DP_EG_AUX_CH_P	BI
AUX1N	AL27	DP_EG_AUX_CH_N	BI
DDC2CLK	AM19	NC	
DDC2DATA	AL19	NC	
AUX2P	AN20	DP_T29SNK0_AUXCH_C_P	BI
AUX2N	AM20	DP_T29SNK0_AUXCH_C_N	BI
DDCCLK_AUX3P	AL30	DP_T29SNK1_AUXCH_C_P	BI
DDCDATA_AUX3N	AM30	DP_T29SNK1_AUXCH_C_N	BI
DDCCLK_AUX4P	AL29	NC	
DDCDATA_AUX4N	AM29	NC	
DDCCLK_AUX5P	AN21	LVDS_EG_DDC_CLK	OUT
DDCDATA_AUX5N	AM21	LVDS_EG_DDC_DATA	BI
DDC6CLK	AJ30	NC	
DDC6DATA	AJ31	NC	
DDCCLK_AUX7P	AK30	NC	
DDCDATA_AUX7N	AK29	NC	

XW8602 SM
MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=0V

PP3V3_S0GPU
Straps for audio on DP and HDMI
R8604 10K 5% 1/10W MF-LF 402
R8605 10K 5% 1/16W MF-LF 402

PP1V8_S0GPU
R8606 10K 5% 1/16W MF-LF 402

U8000 WHISTLER 40NM-ES FCBGA (3 OF 9)
LVDS CNTL

LVTMDP:

VARY_BL	AK27	LVDS_EG_BLK_PWM
DIGON	AJ27	EG_LCD_PWR_EN
TXCLK_UP_DPF3P	AK35	NC_LVDS_EG_B_CLK_P
TXCLK_UN_DPF3N	AL36	NC_LVDS_EG_B_CLK_N
TXOUT_U0P_DPF2P	AJ38	LVDS_EG_B_DATA_P<0>
TXOUT_U0N_DPF2N	AK37	LVDS_EG_B_DATA_N<0>
TXOUT_U1P_DPF1P	AH35	LVDS_EG_B_DATA_P<1>
TXOUT_U1N_DPF1N	AJ36	LVDS_EG_B_DATA_N<1>
TXOUT_U2P_DPF0P	AG38	LVDS_EG_B_DATA_P<2>
TXOUT_U2N_DPF0N	AH37	LVDS_EG_B_DATA_N<2>
TXOUT_U3P	AF35	NC_LVDS_EG_B_DATA_P<3>
TXOUT_U3N	AG36	NC_LVDS_EG_B_DATA_N<3>
TXCLK_LP_DPE3P	AP34	LVDS_EG_A_CLK_P
TXCLK_LN_DPE3N	AR34	LVDS_EG_A_CLK_N
TXOUT_L0P_DPE2P	AW37	LVDS_EG_A_DATA_P<0>
TXOUT_L0N_DPE2N	AU35	LVDS_EG_A_DATA_N<0>
TXOUT_L1P_DPE1P	AR37	LVDS_EG_A_DATA_P<1>
TXOUT_L1N_DPE1N	AU39	LVDS_EG_A_DATA_N<1>
TXOUT_L2P_DPE0P	AP35	LVDS_EG_A_DATA_P<2>
TXOUT_L2N_DPE0N	AR35	LVDS_EG_A_DATA_N<2>
TXOUT_L3P	AN36	NC_LVDS_EG_A_DATA_P<3>
TXOUT_L3N	AP37	NC_LVDS_EG_A_DATA_N<3>

OMIT

SYNC_MASTER=K92_SUMA SYNC_DATE=10/21/2010
PAGE TITLE: Whistler LVDS/DP/GPIO
Apple Inc.
DRAWING NUMBER: SIZE D
REVISION:
BRANCH:
PAGE: 86 OF 132
SHEET: 79 OF 105

GPIOs

GPU_PCIE_TX_PWR	GP	GPU_PCIE_TX_PWR	MAKE_BASE=TRUE
GPU_GPIO_TX_DEEMP	GP	GPU_GPIO_TX_DEEMP	MAKE_BASE=TRUE
GPU_PCIE_GEN2	GP	GPU_PCIE_GEN2	MAKE_BASE=TRUE
GPU_SMB_DAT	GP	GPU_SMB_DAT	MAKE_BASE=TRUE
GPU_SMB_CLK	GP	GPU_SMB_CLK	MAKE_BASE=TRUE
GPU_AC_BATT	GP	GPU_AC_BATT	MAKE_BASE=TRUE
GPU_VCORE_VID0	GP	GPU_VCORE_VID0	MAKE_BASE=TRUE
EG_BKLT_EN	GP	EG_BKLT_EN	MAKE_BASE=TRUE
GPU_ROM_SO	GP	GPU_ROM_SO	MAKE_BASE=TRUE
GPU_ROM_SI	GP	GPU_ROM_SI	MAKE_BASE=TRUE
GPU_ROM_SCLK	GP	GPU_ROM_SCLK	MAKE_BASE=TRUE
GPU_CONFIG_0	GP	GPU_CONFIG_0	MAKE_BASE=TRUE
GPU_CONFIG_1	GP	GPU_CONFIG_1	MAKE_BASE=TRUE
GPU_CONFIG_2	GP	GPU_CONFIG_2	MAKE_BASE=TRUE
DP_T29SNK0_HPD_GPU		DP_T29SNK0_HPD_GPU	MAKE_BASE=TRUE
GPU_VCORE_VID1	GP	GPU_VCORE_VID1	MAKE_BASE=TRUE

GPIOs

GPU_VCORE_VID2	GP	GPU_VCORE_VID2	MAKE_BASE=TRUE
SMC_GFX_THROTTLE_R_L	GP	SMC_GFX_THROTTLE_R_L	MAKE_BASE=TRUE
DP_T29SNK1_HPD_GPU	GP	DP_T29SNK1_HPD_GPU	MAKE_BASE=TRUE
SMC_GFX_OVERTEMP_R_L	GP	SMC_GFX_OVERTEMP_R_L	MAKE_BASE=TRUE
GPU_VCORE_VID3	GP	GPU_VCORE_VID3	MAKE_BASE=TRUE
FBVDD_ALTVO	GP	FBVDD_ALTVO	MAKE_BASE=TRUE
GPU_ROM_CS_L	GP	GPU_ROM_CS_L	MAKE_BASE=TRUE
PEX_CLKREQ_L_R	GP	PEX_CLKREQ_L_R	MAKE_BASE=TRUE
NC_GPU_GENERICA	GP	NC_GPU_GENERICA	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_GENERICB	GP	NC_GPU_GENERICB	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_GENERICC	GP	NC_GPU_GENERICC	MAKE_BASE=TRUE NO_TEST=TRUE
DP_CA_DET_EG_R	GP	DP_CA_DET_EG_R	MAKE_BASE=TRUE
NC_GPU_GENERICE	GP	NC_GPU_GENERICE	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_GENERICF	GP	NC_GPU_GENERICF	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_GENERICG	GP	NC_GPU_GENERICG	MAKE_BASE=TRUE NO_TEST=TRUE
DP_EG_HPD	GP	DP_EG_HPD	MAKE_BASE=TRUE

T29 HPD GPU isolation

CRITICAL

DP_T29SNK0_HPD → U8741 (74LVC2G08GT SOT833) → DP_T29SNK0_HPD_GPU

PP3V3_S0 → C8741 0.1UF 20% 10V X5R CERM 402

PP3V3_GPU_VDD33_R → R8741 0 5% 1/16W MF-LF 402 → PP3V3_S0GPU

DP_T29SNK1_HPD → U8741 (74LVC2G08GT SOT833) → DP_T29SNK1_HPD_GPU

PP3V3_S0 → U8741

Unused signals

TP_GPU_JTAG_TCK		TP_GPU_JTAG_TCK	MAKE_BASE=TRUE
TP_GPU_JTAG_TDI		TP_GPU_JTAG_TDI	MAKE_BASE=TRUE
TP_GPU_JTAG_TDO		TP_GPU_JTAG_TDO	MAKE_BASE=TRUE
TP_GPU_JTAG_TMS		TP_GPU_JTAG_TMS	MAKE_BASE=TRUE
TP_GPU_JTAG_TRST_L		TP_GPU_JTAG_TRST_L	MAKE_BASE=TRUE
NC_LVDS_EG_B_CLK_P		NC_LVDS_EG_B_CLK_P	MAKE_BASE=TRUE NO_TEST=TRUE
NC_LVDS_EG_B_CLK_N		NC_LVDS_EG_B_CLK_N	MAKE_BASE=TRUE NO_TEST=TRUE
NC_LVDS_EG_A_DATA_P<3>		NC_LVDS_EG_A_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE
NC_LVDS_EG_A_DATA_N<3>		NC_LVDS_EG_A_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE
NC_LVDS_EG_B_DATA_P<3>		NC_LVDS_EG_B_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE
NC_LVDS_EG_B_DATA_N<3>		NC_LVDS_EG_B_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE

ISOLATION R's for GPU Int Temp Sense

GPU_SMB_DAT → R8780 0 5% 1/16W MF-LF 402 NOSTUFF → SMBUS_SMC_0_S0_SDA

GPU_SMB_CLK → R8781 0 5% 1/16W MF-LF 402 NOSTUFF → SMBUS_SMC_0_S0_SCL

Config Straps

PP3V3_S0GPU

R8700 10K 1% 1/16W MF-LF 402 NOSTUFF → GPU_PCIE_TX_PWR

R8701 10K 1% 1/16W MF-LF 402 NOSTUFF → GPU_GPIO_TX_DEEMP

R8702 10K 1% 1/16W MF-LF 402 → GPU_PCIE_GEN2

R8703 10K 1% 1/16W MF-LF 402 NOSTUFF → GPU_SMB_DAT

R8704 10K 1% 1/16W MF-LF 402 NOSTUFF → GPU_SMB_CLK

R8705 10K 1% 1/16W MF-LF 402 NOSTUFF → GPU_AC_BATT

R8706 10K 1% 1/16W MF-LF 402 NOSTUFF → EG_BKLT_EN

R8707 10K 1% 1/16W MF-LF 402 NOSTUFF → GPU_ROM_SO

R8708 10K 1% 1/16W MF-LF 402 NOSTUFF → GPU_ROM_SI

R8709 10K 1% 1/16W MF-LF 402 NOSTUFF → GPU_ROM_SCLK

R8710 10K 1% 1/16W MF-LF 402 → GPU_CONFIG_0

R8711 10K 1% 1/16W MF-LF 402 NOSTUFF → GPU_CONFIG_1

R8712 10K 1% 1/16W MF-LF 402 GPU_ROM:YES → GPU_CONFIG_2

R8713 10K 1% 1/16W MF-LF 402 NOSTUFF → FBVDD_ALTVO

R8714 10K 1% 1/16W MF-LF 402 NOSTUFF → PEX_CLKREQ_L_R

GPU_ROM:YES

PP3V3_S0GPU

GPU_ROM_SI → R8723 33 5% 1/16W MF-LF 402 → GPU_ROM_SI_R

GPU_ROM_SCLK → R8724 33 5% 1/16W MF-LF 402 → GPU_ROM_SCLK_R

GPU_ROM_CS_L → R8725 33 5% 1/16W MF-LF 402 → GPU_ROM_CS_L_R

R8720 10K 5% 1/16W MF-LF 402

R8721 0 5% 1/16W MF-LF 402

C8721 0.1UF 20% 10V CERM 402

U8701 M25P10A UFDFPN8 CRITICAL OMIT_TABLE

GPU_ROM_SI_R, GPU_ROM_SCLK_R, GPU_ROM_CS_L_R, GPU_ROM_WP_L

R8722 NO STUFF 0 5% 1/16W MF-LF 402

GPU_ROM_SO_R → R8726 33 5% 1/16W MF-LF 402 → GPU_ROM_SO

GPU_ROM:YES

? BOM OPTION NEED CONFIRMATION HERE!

PP3V3_S0

PP3V3_S0GPU

R8750 2.2K 5% 1/16W MF-LF 402 NO STUFF → DP_EG_DDC_CLK

R8751 2.2K 5% 1/16W MF-LF 402 NO STUFF → DP_EG_DDC_DATA

R8752 4.7K 5% 1/16W MF-LF 402 → DP_IG_DDC_CLK

R8753 4.7K 5% 1/16W MF-LF 402 → DP_IG_DDC_DATA

PP3V3_S0GPU

R8796 2.2K 5% 1/16W MF-LF 402 NO STUFF

R8797 2.2K 5% 1/16W MF-LF 402

SMC_GFX_OVERTEMP_R_L → R8798 0 5% 1/16W MF-LF 402 → SMC_GFX_OVERTEMP_L

SMC_GFX_THROTTLE_R_L → R8799 0 5% 1/16W MF-LF 402 → SMC_GFX_THROTTLE_L

EG_LCD_PWR_EN

EG_BKLT_EN

FBVDD_ALTVO

R8792 10K 5% 1/16W MF-LF 402

R8793 10K 5% 1/16W MF-LF 402

R8794 10K 5% 1/16W MF-LF 402

PP3V3_S0GPU

L8703 1200OHM-0.3A 0402 → PP3V3_GPU_OSC_27M (MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)

L8702 1200OHM-0.3A 0402 → PP3V3_GPU_OSC_100M (MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)

C8702 0.1UF 10% 16V X5R 402-1

C8703 0.1UF 10% 16V X5R 402-1

GPU Reference Clocks

U8700 SL16010DC TDFN CRITICAL

VDD1, VDD2

XIN/CLKIN ← GPU_OSC_27M_XTALIN

XOUT → GPU_OSC_27M_XTALOUT

SSCLK → R8730 0 5% 1/16W MF-LF 402 → GPU_CLK100M

REFCLK → R8731 0 5% 1/16W MF-LF 402 → GPU_CLK27M

SSEL0, SSEL1

VSS1, VSS2, THM PAD

Y8700 CRITICAL SM-2.5X2.0MM 27MHZ-15PPM-18PF

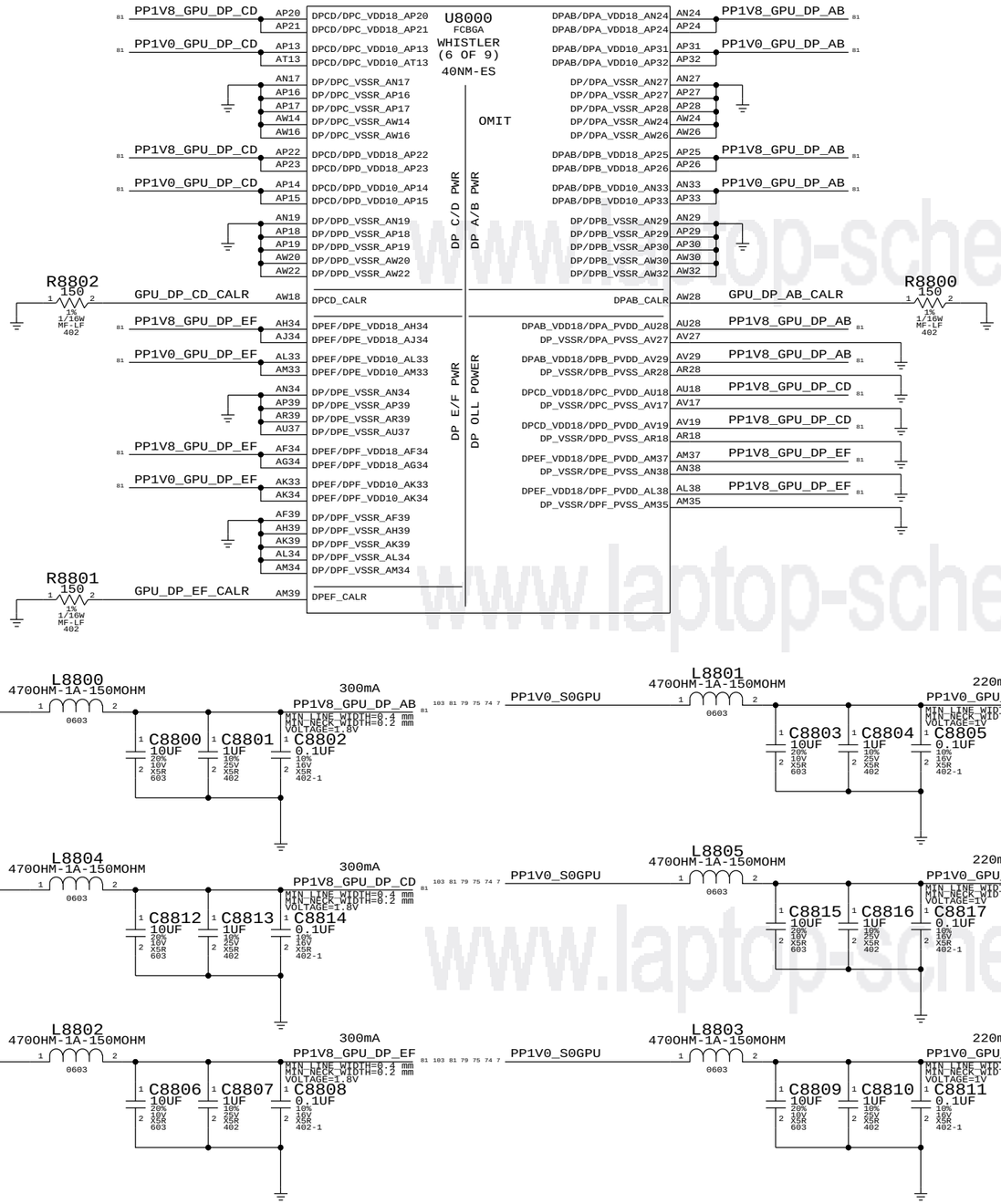
C8700 30PF 5% 50V CERM 402

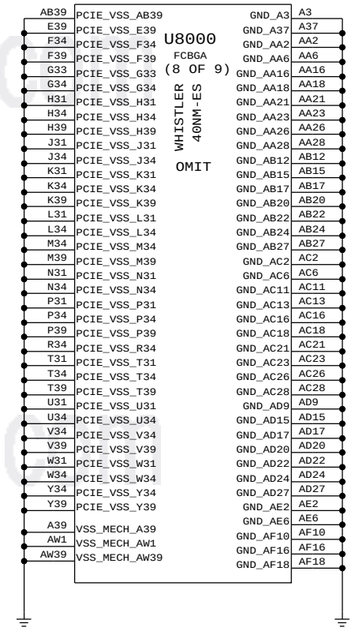
C8701 30PF 5% 50V CERM 402

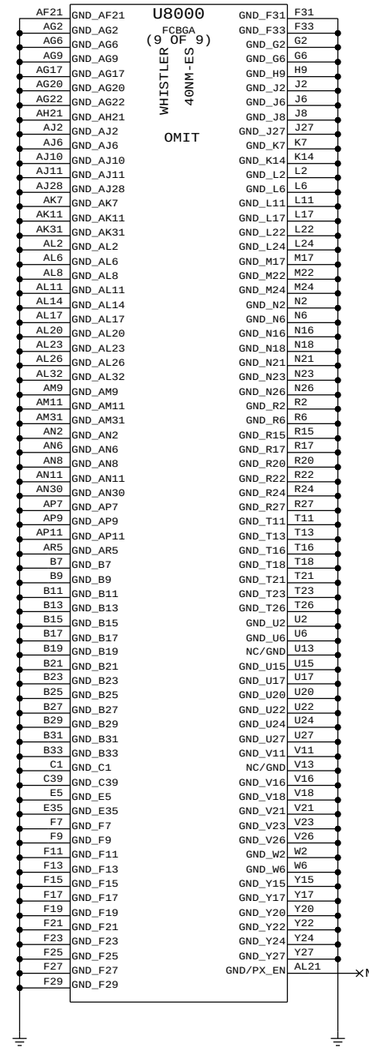
SYNC_MASTER=K91_MLB	SYNC_DATE=07/17/2010
PAGE TITLE	Whistler GPIOs & STRAPs
Apple Inc.	DRAWING NUMBER: SIZE D
	REVISION:
	BRANCH:
	PAGE: 87 OF 132
	SHEET: 80 OF 105

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED







Page Notes

Power aliases required by this page:
- =PP1V8_GPU_DP_AB
- =PP1V8_GPU_DP_CD
- =PP1V8_GPU_DP_EF
- =PP1V0_GPU_DP_AB
- =PP1V0_GPU_DP_CD
- =PP1V0_GPU_DP_EF

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

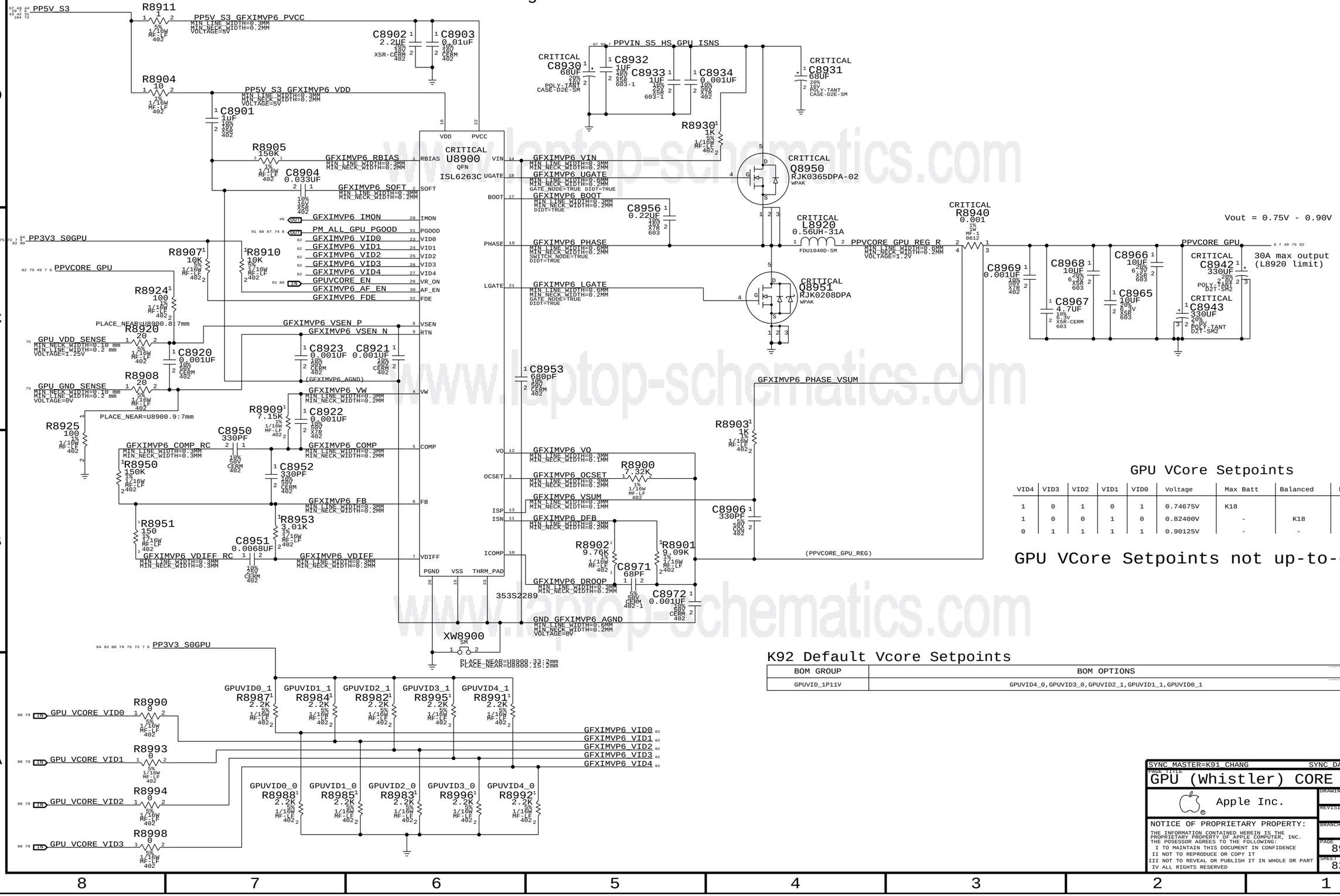
SYNC_MASTER=K92_BEN SYNC_DATE=06/01/2010

PAGE TITLE: Whistler DP PWR/GNDs

Apple Inc.

DRAWING NUMBER: D
SIZE: D
REVISION:
BRANCH:
PAGE: 88 OF 132
SHEET: 81 OF 105

GPU VCore Regulator



GPU VCore Setpoints

VID4	VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	0	1	0	1	0.74675V	K18		-
1	0	0	1	0	0.82400V	-	K18	-
0	1	1	1	1	0.90125V	-	-	K18

GPU VCore Setpoints not up-to-date!

K92 Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_1P11V	GPUVID4_0,GPUVID3_0,GPUVID2_1,GPUVID1_1,GPUVID0_1

SYNC_MASTER=K91_CHANG SYNC_DATE=07/21/2010

PAGE TITLE: GPU (Whistler) CORE SUPPLY

Apple Inc.

DRAWING NUMBER: D | SIZE: D

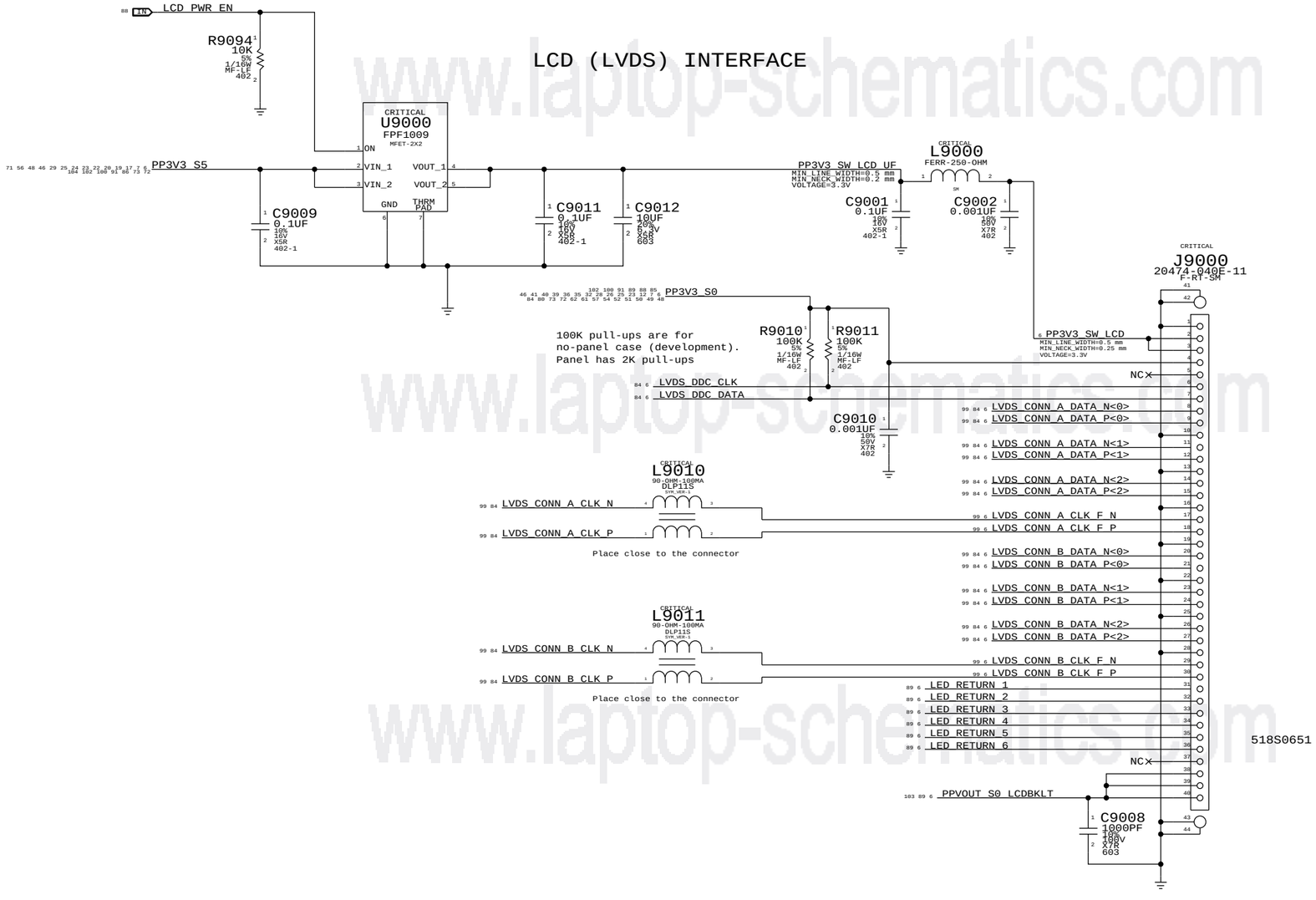
REVISION:

BRANCH:

PAGE: 89 OF 132

SHEET: 82 OF 105

LCD (LVDS) INTERFACE



518S0651

SYNC_MASTER=K17_MLB SYNC_DATE=04/26/2010

PAGE TITLE: LVDS Display Connector

Apple Inc.

DRAWING NUMBER | SIZE: D

REVISION

BRANCH

PAGE: 90 OF 132

SHEET: 83 OF 105

LVDS Transmitter Termination

All emulated LVDS outputs require this termination

PLACE_NEAR=U9600.A6:7mm
R9220 357 1% 1/20W MF 201
LVDS_A_CLK_P → LVDS_CONN_A_CLK_P

PLACE_NEAR=U9600.A7:7mm
R9222 357 1% 1/20W MF 201
LVDS_A_CLK_N → LVDS_CONN_A_CLK_N

R9225 357 1% 1/20W MF 201
LVDS_A_DATA_P<0> → LVDS_CONN_A_DATA_P<0>
PLACE_NEAR=U9600.A8:7mm

PLACE_NEAR=U9600.B9:7mm
R9227 357 1% 1/20W MF 201
LVDS_A_DATA_N<0> → LVDS_CONN_A_DATA_N<0>

R9230 357 1% 1/20W MF 201
LVDS_A_DATA_P<1> → LVDS_CONN_A_DATA_P<1>
PLACE_NEAR=U9600.A9:7mm

PLACE_NEAR=U9600.C10:7mm
R9232 357 1% 1/20W MF 201
LVDS_A_DATA_N<1> → LVDS_CONN_A_DATA_N<1>

R9235 357 1% 1/20W MF 201
LVDS_A_DATA_P<2> → LVDS_CONN_A_DATA_P<2>
PLACE_NEAR=U9600.B10:7mm

PLACE_NEAR=U9600.A10:7mm
R9237 357 1% 1/20W MF 201
LVDS_A_DATA_N<2> → LVDS_CONN_A_DATA_N<2>

R9240 357 1% 1/20W MF 201
LVDS_B_CLK_P → LVDS_CONN_B_CLK_P
PLACE_NEAR=U9600.C8:7mm

PLACE_NEAR=U9600.C9:7mm
R9242 357 1% 1/20W MF 201
LVDS_B_CLK_N → LVDS_CONN_B_CLK_N

R9245 357 1% 1/20W MF 201
LVDS_B_DATA_P<0> → LVDS_CONN_B_DATA_P<0>
PLACE_NEAR=U9600.A2:7mm

PLACE_NEAR=U9600.A3:7mm
R9247 357 1% 1/20W MF 201
LVDS_B_DATA_N<0> → LVDS_CONN_B_DATA_N<0>

R9250 357 1% 1/20W MF 201
LVDS_B_DATA_P<1> → LVDS_CONN_B_DATA_P<1>
PLACE_NEAR=U9600.A1:7mm

PLACE_NEAR=U9600.B3:7mm
R9252 357 1% 1/20W MF 201
LVDS_B_DATA_N<1> → LVDS_CONN_B_DATA_N<1>

R9255 357 1% 1/20W MF 201
LVDS_B_DATA_P<2> → LVDS_CONN_B_DATA_P<2>
PLACE_NEAR=U9600.C5:7mm

R9257 357 1% 1/20W MF 201
LVDS_B_DATA_N<2> → LVDS_CONN_B_DATA_N<2>
PLACE_NEAR=U9600.A5:7mm

DP AUX, DDC, & HPD muxing to IG/EG

PP3V3_S0
R9202 10K 5% 1/10W MF-LF 402
C9220 0.1UF 20% 16V X5R 2 CERM 402
C9230 0.1UF 20% 16V X5R 2 CERM 402

U9220 CBTL03062 BGA (CRITICAL)
VDD

DP_IG_AUX_CH_P	17	DAUX1+
DP_IG_AUX_CH_N	16	DAUX1-
DP_EG_AUX_CH_P	14	DAUX2+
DP_EG_AUX_CH_N	13	DAUX2-
DP_IG_DDC_CLK	12	DDC_CLK1
DP_IG_DDC_DATA	11	DDC_DAT1
DP_EG_DDC_CLK	9	DDC_CLK2
DP_EG_DDC_DATA	8	DDC_DAT2
DP_IG_HPD	10	HPD_1
DP_EG_HPD	7	HPD_2
DP_MUX_SEL_EG	5	GPU_SEL
DP_MUX_EN	15	XSD*

AUX+ 20 DP_EXTA_AUXCH_C_P
AUX- 1 DP_EXTA_AUXCH_C_N
DDC_CLK 2 DP_EXTA_DDC_CLK
DDC_DAT 3 DP_EXTA_DDC_DATA
HPDIN 4 (DP_EXTA_HPD)
GND 19

R9204 100K 5% 1/10W MF-LF 402
R9205 100K 5% 1/10W MF-LF 402

T29/DP HOT PLUG IN

T29_DP_HPD:MUX_GMUX
R9206 0 5% 1/10W MF-LF 402
DP_EXTA_HPD

PP3V3_S0
T29_DP_HPD:ALL_OR
C9210 0.1UF 20% 16V X5R 2 CERM 402
CRITICAL
T29_DP_HPD:ALL_OR 74LVC2G32GT SOT833 U9210
DP_T29SNK0_HPD
DP_T29SNK1_HPD
T29_HOTPLUG_DET_OR

T29_DP_HPD:ALL_OR 74LVC2G32GT SOT833 U9210
(DP_EXTA_HPD)
DP_HOTPLUG_DET

PP3V3_S0
T29_DP_HPD:MCU_GMUX
Q9280 SSM3K15FV SOT-VESM-MF
T29_DP_HPD:MCU_GMUX
R9281 100K 5% 1/10W MF-LF 402
DP_A_EXT_HPD

LVDS DDC MUX

PP3V3_S0GPU
PP3V3_S0
R9270 20K 5% 1/10W MF-LF 402
R9271 20K 5% 1/10W MF-LF 402
C9270 0.1UF 10% 16V CERM 402
R9272 20K 5% 1/10W MF-LF 402
R9273 20K 5% 1/10W MF-LF 402

U9270 SN74LV4066A QFN1 (CRITICAL)
VCC

LVDS_DDC_SEL_EG	C1	A1	LVDS_EG_DDC_CLK
LVDS_DDC_SEL_IG	C2	A2	LVDS_IG_DDC_CLK
		B2	LVDS_DDC_CLK
	C3	A3	LVDS_EG_DDC_DATA
		B3	
	C4	A4	LVDS_IG_DDC_DATA
		B4	LVDS_DDC_DATA
	GND	THRM	

SYNC_MASTER=K92_YUN SYNC_DATE=06/25/2010

PAGE TITLE: Muxed Graphics Support

Apple Inc.

DRAWING NUMBER: D
SIZE: D
REVISION:
BRANCH:
PAGE: 92 OF 132
SHEET: 84 OF 105

T29 A High-Speed Signals

T29 signals are P/N-swapped after AC caps to improve layout.

T29 Path Biasing

DP A Super-Driver

PS8301 I2C Addresses:

A1	A0	Addr (W/R)
0	0	0x96/0x97
0	1	0xB6/0xB7
1	0	0x94/0x95
1	1	0xB4/0xB5

Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.

PS8301 has internal ~150K pull-down on PD pin. Okay to drive this pin even when VCC=0V per Parade (pin is 5V-tolerant).

If GPU uses common pins for AUX_CH and DDC, alias nets together at GPU.

R9308/R9309 maintain bias on C9308/C9309 to prevent spikes when U9310 AUXDDC_OFF transitions from high to low.

DP/T29 A Low-Speed MUX

IC supports input high while Vcc = 0V.

DP Path Biasing

CBTL04DP081 (353S3151) and PI3vEDP212 (353S3055) are footprint-compatible parts with similar pinouts. NXP uses pin 10 for ML and HPD, Pericom uses pin 10 for ML and pin 11 for HPD.

U9390 BOM table in csa 5!!!

Note: U9390 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9390 AUX defaults to DP mode because 100-ohm pull-downs would defeat DP Sink's detection of DP Source.

Port A MCU

=T29_WAKE_L:
use PCIe WAKE#

R9330 provides pads for programming/debug of MCU, please make accessible. If project has space for 10-pin programming header it should be used.

P2R = Plug to Receptacle
R2P = Receptacle to Plug

I2C Addr: 0x26/0x27 (Wr/Rd)

AUXCH Snoop Port, used by PS8301 during training.

SIGNAL_MODEL=T29DP_MUX

SYNC_MASTER=K91_MLB	SYNC_DATE=10/22/2010
PAGE TITLE: DisplayPort/T29 A MUXing	
Apple Inc.	DRAWING NUMBER: SIZE D
	REVISION:
	BRANCH:
	PAGE: 93 OF 132
	SHEET: 85 OF 105

Port A HV Power Switch

	Nominal	Min	Max
IFLT	885mA	876mA	894mA (*)
ILIM	935mA	925mA	944mA (*)
TFLT	18.3ms	13.4ms	26.7ms
TSD	470ms	235ms	724ms

(*) U9410 tolerance unknown

IFLT = 200k / RFLT = 885mA
ILIM = 201k / RLIM = 935mA
TFLT = CCT * 38900
TSD = CCT * 100000

Bleeder Resistor
2.5V / 249 ohm = 10mA
P = ~27mW

Note: Bleeder active when DPAPWRSW_HV_DET is HIGH and T29_A_HV_EN is LOW.

3.3V/HV Power MUX

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 65mOhm @ 2.5V Vgs
Id(max): 3.7A @ 70C

3.3V/HV MUXed

Blocking FET, off when Source >3.4V or HV_EN high.

ZXRE060A REF range: 0.595-0.605V (0.600V nominal)
Circuit threshold range: 3.363-3.439V (3.395V nominal)

Port A 3.3V Power Switch

DP_PWR must be S4/S5 to support wake from T29 devices.

3.3V Always

Circuit threshold range: 2.877-2.941V (2.903V nominal)

DisplayPort/T29 A Connector

For J9400 T29 SMT pads (3, 5, 7, 8, 19):
GND_VOID=TRUE

T29: TX_0
T29: LSX_R2P/P2R (P/N)
T29: TX_1

470k R's for ESD protection on AC-coupled signals.

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

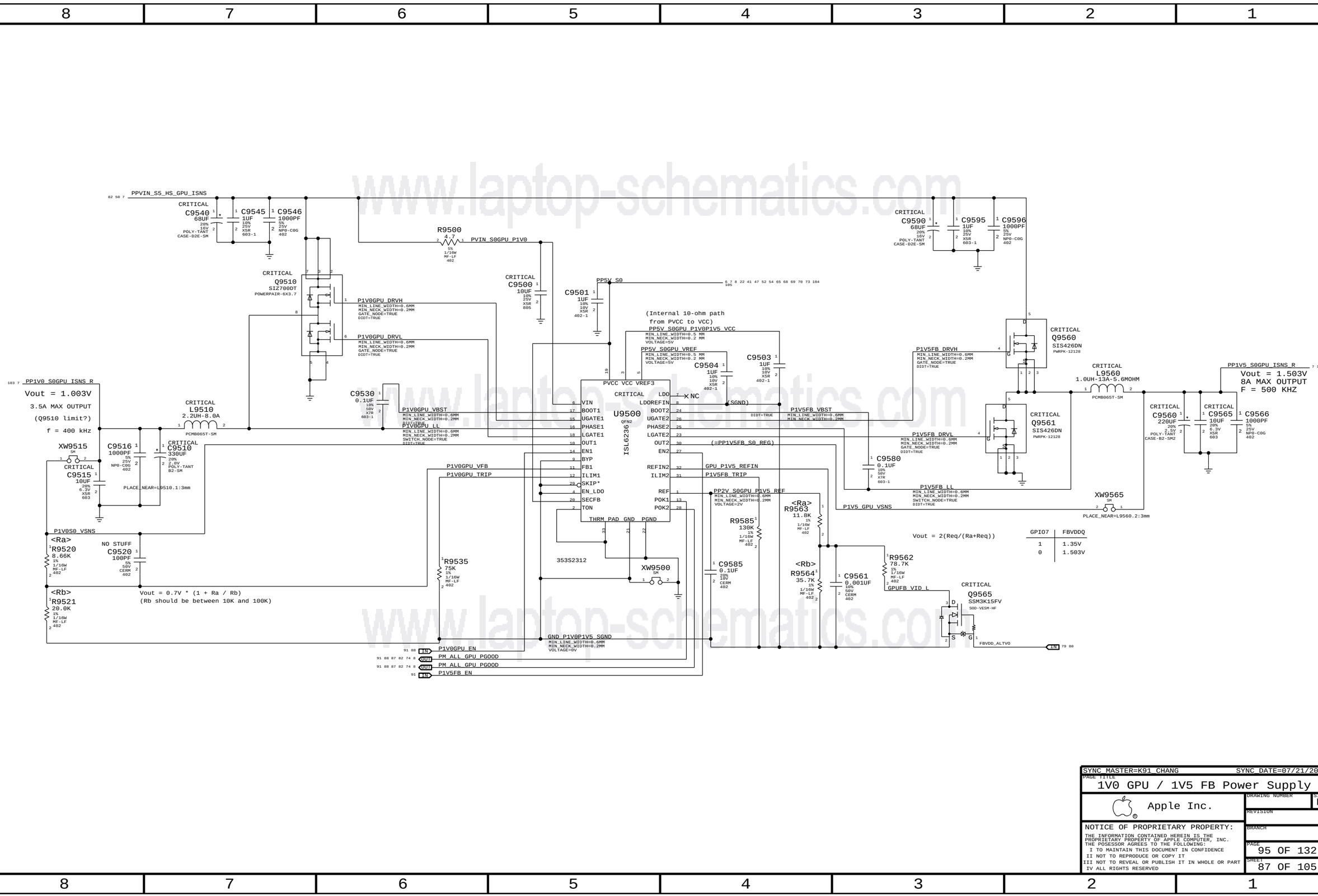
T29: Unused

SYNC_MASTER=K91_MLB SYNC_DATE=10/22/2010

PAGE TITLE: DisplayPort/T29 A Connector

Apple Inc.

DRAWING NUMBER | SIZE: D
REVISION
BRANCH
PAGE: 94 OF 132
SHEET: 86 OF 105



SYNC_MASTER=K91_CHANG SYNC_DATE=07/21/2010

PAGE TITLE
1V0 GPU / 1V5 FB Power Supply

Apple Inc.

DRAWING NUMBER | SIZE D

REVISION

BRANCH

PAGE 95 OF 132

SHEET 87 OF 105

GMUX CPLD

LVDS Receiver Termination

LVDS_IG_A_CLK_P	R9650	100	1% 1/20W MF 201	PLACE_NEAR=U9600.H3:5mm	LVDS_IG_A_CLK_N	94 88 18	18 88 94
LVDS_IG_A_DATA_P<0>	R9651	100	1% 1/20W MF 201	PLACE_NEAR=U9600.E1:5mm	LVDS_IG_A_DATA_N<0>	94 88 18	18 88 94
LVDS_IG_A_DATA_P<1>	R9652	100	1% 1/20W MF 201	PLACE_NEAR=U9600.E3:5mm	LVDS_IG_A_DATA_N<1>	94 88 18	18 88 94
LVDS_IG_A_DATA_P<2>	R9653	100	1% 1/20W MF 201	PLACE_NEAR=U9600.G1:5mm	LVDS_IG_A_DATA_N<2>	94 88 18	18 88 94
LVDS_IG_B_DATA_P<0>	R9654	100	1% 1/20W MF 201	PLACE_NEAR=U9600.G2:5mm	LVDS_IG_B_DATA_N<0>	94 88 18	18 88 94
LVDS_IG_B_DATA_P<1>	R9655	100	1% 1/20W MF 201	PLACE_NEAR=U9600.G3:5mm	LVDS_IG_B_DATA_N<1>	94 88 18	18 88 94
LVDS_IG_B_DATA_P<2>	R9656	100	1% 1/20W MF 201	PLACE_NEAR=U9600.B2:5mm	LVDS_IG_B_DATA_N<2>	94 88 18	18 88 94
LVDS_EG_A_CLK_P	R9660	100	1% 1/20W MF 201	PLACE_NEAR=U9600.J12:5mm	LVDS_EG_A_CLK_N	99 88 79	79 88 99
LVDS_EG_A_DATA_P<0>	R9661	100	1% 1/20W MF 201	PLACE_NEAR=U9600.D13:5mm	LVDS_EG_A_DATA_N<0>	99 88 79	79 88 99
LVDS_EG_A_DATA_P<1>	R9662	100	1% 1/20W MF 201	PLACE_NEAR=U9600.E14:5mm	LVDS_EG_A_DATA_N<1>	99 88 79	79 88 99
LVDS_EG_A_DATA_P<2>	R9663	100	1% 1/20W MF 201	PLACE_NEAR=U9600.F12:5mm	LVDS_EG_A_DATA_N<2>	99 88 79	79 88 99
LVDS_EG_B_DATA_P<0>	R9664	100	1% 1/20W MF 201	PLACE_NEAR=U9600.G14:5mm	LVDS_EG_B_DATA_N<0>	99 88 79	79 88 99
LVDS_EG_B_DATA_P<1>	R9665	100	1% 1/20W MF 201	PLACE_NEAR=U9600.G13:5mm	LVDS_EG_B_DATA_N<1>	99 88 79	79 88 99
LVDS_EG_B_DATA_P<2>	R9666	100	1% 1/20W MF 201	PLACE_NEAR=U9600.H12:5mm	LVDS_EG_B_DATA_N<2>	99 88 79	79 88 99

Required Pullups

SIGNAL_MODEL=EMPTY

EG_PWRSEQ_EN	R9684	1K	5% 1/20W MF 201	PP3V3_S0
JTAG_GMUX_TDI	R9685	10K	5% 1/20W MF 201	
JTAG_GMUX_TDO	R9686	10K	5% 1/20W MF 201	
GMUX_DEBUG_RESET_L	R9680	1K	5% 1/20W MF 201	

NO STUFF R9679 10K 1% 1/10W MF-LF 402 — SILK_PART=GMUX_RST

Required Pulldowns

DP_MUX_SEL_EG	R9681	10K	5% 1/20W MF 201
LVDS_DDC_SEL_IG	R9682	10K	5% 1/20W MF 201
LVDS_DDC_SEL_EG	R9683	10K	5% 1/20W MF 201
EG_RESET_L	R9691	100K	5% 1/20W MF 201
LCD_BKLT_PWM	R9693	100K	5% 1/20W MF 201

NO STUFF

(Use open-drain PGOOD output to hold off the start of the GPU PWRSEQ until the first GPU rail's source is valid)

Power Rails

- PP3V3_S0 via R9600 0 5% 1/16W MF-LF 402
- PP1V8_S0 via R9610 0 5% 1/10W MF-LF 402
- PP1V2_S0
- PP3V3_S0_GMUX_R (MIN_LINE_WIDTH=0.4mm, MIN_NECK_WIDTH=0.09 mm, VOLTAGE=3.3V)
- PP1V8_S0_GMUX_R (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.09 mm, VOLTAGE=1.8V)
- PP3V3_S0_GMUX_ULC_VCCPLL via L9621 FERR-220-OHM 0402 (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.09 mm, VOLTAGE=3.3V)
- PP3V3_S0_GMUX_LRC_VCCPLL via L9620 FERR-220-OHM 0402 (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.09 mm, VOLTAGE=3.3V)

Decoupling: C9600 4.7UF 20% 4V X5R 402; C9610–C9629 0.1UF 20% 10V CERM 402; C9630 0.1UF 20% 10V CERM 402; C9631 0.1UF 20% 10V CERM 402

U9600 XP25-5 CSBGA

OMIT CRITICAL

VCC: B11 C4 J3 J13 N11 P8 C11
VCCAUX: J2 J14 M8
VCCIO0: B5
VCCIO1: B7 A12
VCCIO2: C14 F13
VCCIO3: M12 M9
VCCIO4: M3 N5
VCCIO5: M1 C3
VCCIO6: F2
VCCIO7: K12
VCCJ: A4
ULC_VCCPLL: P11
LRC_VCCPLL

JTAG_ISP_TCK	K14	TCK
JTAG_GMUX_TDI	L13	TDI
JTAG_GMUX_TDO	K13	TDO
JTAG_GMUX_TMS	L12	TMS
GMUX_TOE	K2	TOE
GMUX_CFG0	K1	CFG0

BANK5

LCD_BKLT_EN	P2	PB7A
LCD_BKLT_PWM	N2	PB7B
LVDS_DDC_SEL_EG	P4	PB14A
LVDS_DDC_SEL_IG	N4	PB14B
DP_MUX_EN	N3	PB15A (OD)
DP_MUX_SEL_EG	M4	PB15B
EG_RESET_L	P5	PB16A
P3V3GPU_EN	M5	PB16B
GPUVCORE_EN	P6	PB17A
P1V0GPU_EN	M6	PB17B
P1V5FB1V8GPU_R_EN	P7	PB18A
PEG_CLKREQ_L	M7	PB18B (OD)
DP_CA_DET_EG	N7	PB19A
LCD_PWR_EN	N8	PB19B

BANK4

LPC_AD<0>	P9	PB20A
LPC_AD<1>	N9	PB20B
LPC_AD<2>	P10	PB26A
LPC_AD<3>	M10	PB26B
LPC_FRAME_L	P12	PB27A
LPCPLUS_RESET_L	P13	PB27B
LPC_CLK33M_GMUX	N12	PB28A
GMUX_INT	P14	PB28B

BANK7

LVDS_IG_B_DATA_P<2>	B1	PL2A
LVDS_IG_B_DATA_N<2>	B2	PL2B
GMUX_PL6A	C2	PL6A
TP_GMUX_PL6B	D3	PL6B
LVDS_IG_A_DATA_P<0>	D1	PL7A
LVDS_IG_A_DATA_N<0>	E1	PL7B
LVDS_IG_A_DATA_P<1>	D2	PL8A
LVDS_IG_A_DATA_N<1>	E3	PL8B
LVDS_IG_A_DATA_P<2>	F1	PL9A
LVDS_IG_A_DATA_N<2>	G1	PL9B
LVDS_IG_B_DATA_P<0>	F3	PL10A
LVDS_IG_B_DATA_N<0>	G2	PL10B
LVDS_IG_B_DATA_P<1>	H2	PL11A
LVDS_IG_B_DATA_N<1>	G3	PL11B
LVDS_IG_A_CLK_P	H1	PL12A
LVDS_IG_A_CLK_N	H3	PL12B
TP_LVDS_MUX_SEL_EG	L1	PL14A
TP_GMUX_PL14B	L3	PL14B
GMUX_RESET_L	K3	PL15A
GMUX_VSYNC	L2	PL15B
PM_ALL_GPU_PGOOD	N1	PL25A
PEX_CLKREQ_L	P1	PL25B

(Tie/strap low if EGPU doesn't provide CLKREQ_L output, provide pullup to GPU rail if using CLKREQ_L output from EGPU)

BANK6

LVDS_B_DATA_P<0>	A2	PT7A
LVDS_B_DATA_N<0>	A3	PT7B
LVDS_B_DATA_P<1>	A1	PT8A
LVDS_B_DATA_N<1>	B3	PT8B
LVDS_B_DATA_P<2>	C5	PT9A
LVDS_B_DATA_N<2>	A5	PT9B
EG_PWRSEQ_EN	B6	PT14A
GMUX_DEBUG_RESET_L	C7	PT14B
LVDS_A_CLK_P	A6	PT15A
LVDS_A_CLK_N	A7	PT15B
LVDS_B_CLK_P	C8	PT16A
LVDS_B_CLK_N	C9	PT16B
LVDS_A_DATA_P<0>	A8	PT17A
LVDS_A_DATA_N<0>	B9	PT17B
LVDS_A_DATA_P<1>	A9	PT18A
LVDS_A_DATA_N<1>	C10	PT18B
LVDS_A_DATA_P<2>	B10	PT19A
LVDS_A_DATA_N<2>	A10	PT19B
GND	A11	PT20A
GND	B12	PT20B
GND	B13	PT28A
GND	A13	PT28B

BANK1

BANK2

DP_A_CA_DET	A14	PR2A
DP_HOTPLUG_DET	B14	PR2B
LVDS_EG_A_DATA_P<0>	D12	PR6A
LVDS_EG_A_DATA_N<0>	D13	PR6B
LVDS_EG_A_DATA_P<1>	D14	PR7A
LVDS_EG_A_DATA_N<1>	E14	PR7B
LVDS_EG_A_DATA_P<2>	E12	PR8A
LVDS_EG_A_DATA_N<2>	F12	PR8B
LVDS_EG_B_DATA_P<0>	F14	PR9A
LVDS_EG_B_DATA_N<0>	G14	PR9B
LVDS_EG_B_DATA_P<1>	G12	PR10A
LVDS_EG_B_DATA_N<1>	G13	PR10B
LVDS_EG_B_DATA_P<2>	H13	PR11A
LVDS_EG_B_DATA_N<2>	H12	PR11B
LVDS_EG_A_CLK_P	H14	PR12A
LVDS_EG_A_CLK_N	J12	PR12B
LVDS_IG_PANEL_PWR	L14	PR14A
EG_LCD_PWR_EN	M13	PR14B
LVDS_IG_BKL_ON	N14	PR24A
EG_BKLT_EN	N13	PR24B

BANK3

GND: J1 B8 C6 C12 C13 G13 M14 N10 N6 P3 M2 C1 E2 B4 M11

GNDIO0 GNDIO1 GNDIO2 GNDIO3 GNDIO4 GNDIO5 GNDIO6 GNDIO7 ULC_GNDPLL LRC_GNDPLL

CRITICAL J9600 1909782 M-RT-SM

GMUX_JTAG_CONN

1	PP3V3_S0	
2	JTAG_GMUX_TDO	
3	JTAG_GMUX_TDI	
4	JTAG_GMUX_TMS	
5		
6	JTAG_ISP_TCK	
7		
8		

JTAG Circuit

- R9645 10K 1% 1/20W MF 201 — PP3V3_S0
- R9640 10K 1% 1/20W MF 201 — PP3V3_S0
- NO STUFF R9646 10K 1% 1/20W MF 201
- NO STUFF R9641 10K 1% 1/20W MF 201
- NO STUFF R9647 10K 1% 1/20W MF 201
- R9670 10K 1% 1/20W MF 201 — PP3V3_S0 — GMUX_VSYNC
- R9605 1K 5% 1/10W MF-LF 402 — PP3V3_T29 — T29_JTAG_FET
- Q9605 SSM6N15FEAPE SOT563 — JTAG_GMUX_TDI — JTAG_ISP_TDI
- Q9605 SSM6N15FEAPE SOT563 — JTAG_GMUX_TDO — JTAG_ISP_TDO

Power Sequencing

- PP3V3_S3 — R9676 100K 5% 1/20W MF 201 — GMUX_S3_PD_EN — Q9607 SSM6N15FEAPE SOT563
- Q9607 SSM6N15FEAPE SOT563 — ALL_SYS_PWRGD
- R9675 NO STUFF 0 5% 1/10W MF-LF 402
- R9671 4.7K 5% 1/20W MF 201
- R9672 4.7K 5% 1/20W MF 201
- R9673 4.7K 5% 1/20W MF 201
- R9674 4.7K 5% 1/20W MF 201
- R9678 4.7K 5% 1/20W MF 201
- GMUX_S3_PD_GND

SYNC_MASTER=K92_YUAN SYNC_DATE=07/28/2016

PAGE TITLE: Graphics MUX (GMUX)

Apple Inc.

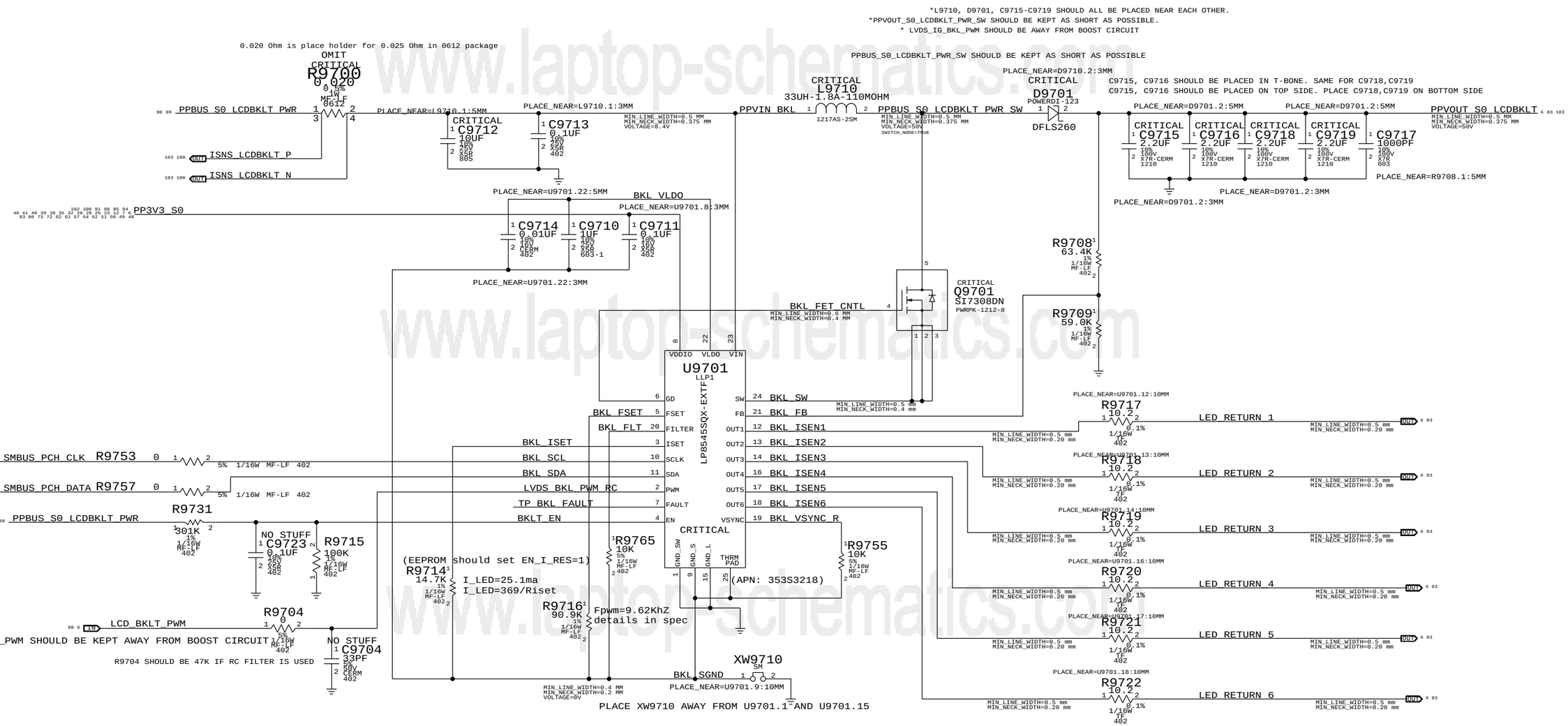
DRAWING NUMBER — SIZE D

REVISION

BRANCH

PAGE 96 OF 132

SHEET 88 OF 105



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
107S0196	1	0.025OHM,1W,0612,MTL FILM RES	R9700	CRITICAL	

SYNC_MASTER=K92_DINESH SYNC_DATE=09/07/2010

PAGE TITLE: LCD Backlight Driver (LP8545)

Apple Inc.

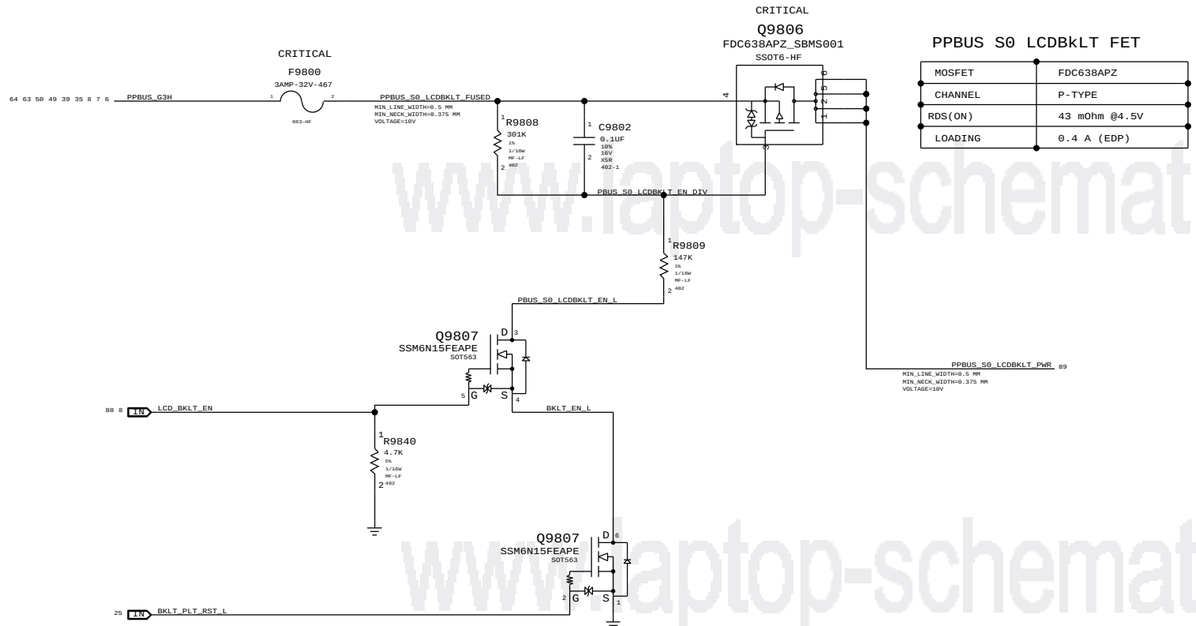
DRAWING NUMBER | SIZE: D

REVISION

BRANCH

PAGE: 97 OF 132

SHEET: 89 OF 105



PPBUS S0 LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.4 A (EDP)

SYNC_MASTER=K17_MLB SYNC_DATE=04/26/2010

PAGE TITLE

LCD Backlight Support

Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH

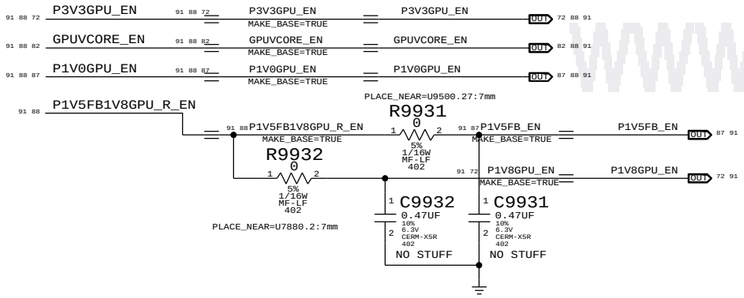
PAGE 98 OF 132

SHEET 90 OF 105

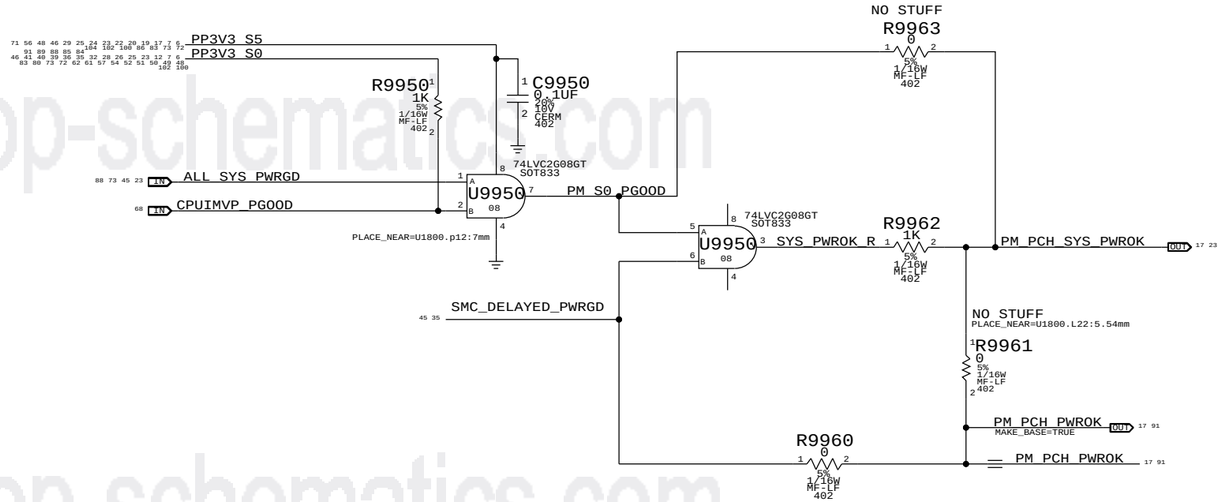
GPU Rail Sequencing

Whistler GPU requires rails to come up in the following order:

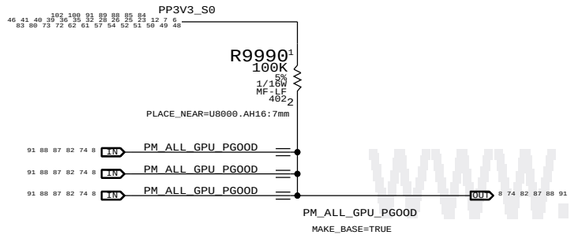
1) GPU_3.3V
2) GPUVcore
3) GPU_1.0V
4) GPU_1.8V;GDDR5 1.5/1.35V



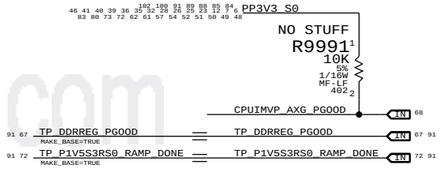
PCH S0 PWRGD



EXT GPU PWRGD Pullup



Unused PGOOD signal



SYNC_MASTER=K92_YUAN SYNC_DATE=07/30/2010

PAGE TITLE
Power Sequencing EG/PCH S0

Apple Inc.

DRAWING NUMBER
SIZE D
REVISION
BRANCH
PAGE 99 OF 132
SHEET 91 OF 105

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Calpella SFF DG (DG-407364_v1.5), Section 2.8

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	6 9 17
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	6 9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	6 9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	6 9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	9 17
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	9 17
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	9 17
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	10 16
	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	10 16
	CPU_50S	CPU_AGTL	FDI_INT	9 17
CPU_PECI	CPU_50S	PCIE	CPU_PECI	10 19 45
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	10 17
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	10 17 29
XDP_CPU_PWRGOOD	CPU_50S	CPU_ITP	XDP_CPU_PWRGD	23
XDP_DBRESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L	10 23 25
XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	10 23
XDP_PREQ_L	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	10 23
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP0	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP1	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP2	
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<11..0>	9 23
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..16>	9 23
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	10
	CPU_50S	CPU_AGTL	CPU_PROC_SEL_L	10 17
	CPU_50S	CPU_AGTL	TP_CPU_VTT_SELECT	8
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 46 68
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 19 23
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 19
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	10 16
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	10 16
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	16 23
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	16 23
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	23
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	23
	CPU_55S	CPU_8MIL	CPU_PSI_L	
PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
	CPU_27P4S	CPU_COMP	CPU_PEG_RBIAS	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP3	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP2	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP1	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP0	
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	10 23
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	10 23
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	10 23
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	10 23
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	10 23
XDP_BPM	CPU_50S	CPU_ITP	XDP_BPM_L<3..0>	10 23
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7..4>	10 23
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	23
	CPU_55S	CPU_8MIL	CPU_VID<6..0>	8
	CPU_50S	CPU_AGTL	CPUIMVP_IMON	
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	12 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	12 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	12 70
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	12 70
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	12 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	12 68
	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	12
	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	12
	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	12
	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	12
	CPU_55S	CPU_8MIL	GFX_VID<6..0>	8
PM_DPRSLPVR	CPU_50S	CPU_AGTL	GFX_DPRSLPVR	
	CPU_50S	CPU_AGTL	GFX_VR_EN	
	CPU_50S	CPU_AGTL	GFXIMVP_IMON	
	PCIE_85D	PCIE	PEG_R2D_P<7..0>	74
	PCIE_85D	PCIE	PEG_R2D_N<7..0>	74
PEG_R2D	PCIE_85D	PCIE	PEG_R2D_C_P<7..0>	8 74
	PCIE_85D	PCIE	PEG_R2D_C_N<7..0>	8 74
PEG_D2R	PCIE_85D	PCIE	PEG_D2R_P<7..0>	8 74
	PCIE_85D	PCIE	PEG_D2R_N<7..0>	8 74
	PCIE_85D	PCIE	PEG_D2R_C_P<7..0>	74
	PCIE_85D	PCIE	PEG_D2R_C_N<7..0>	74
	CPU_50S	CPU_VID	CPU_VIDSOUT	12 68
	CPU_50S	CPU_VID	CPU_VIDSCLK	12 68
	CPU_50S	CPU_VID	CPU_VIDALERT_L	12 68

SYNC_MASTER=K91_MLB SYNC_DATE=07/22/2010

PAGE TITLE: CPU Constraints

Apple Inc.

DRAWING NUMBER | SIZE: D

REVISION

BRANCH

PAGE: 100 OF 132

SHEET: 92 OF 105

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3:
DQ/DM signals should be matched within 0.508mm of associated DQS pair.
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-12.7mm] and [CLK+25.4mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-12.7mm] to [CLK+0.0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to SODIMM pad is 139.7mm, from procesor ball to SODIMM pad is 114.3mm.

SOURCE: Calpella SFF Platform DG, Rev 1.5 (#407364), Section 2.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0> 11 26
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0> 11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<3..0> 11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<3..0> 11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<3..0> 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0> 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0> 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L 11 26
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0> 11 27
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8> 11 27
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16> 11 27
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24> 11 27
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32> 11 26 27
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40> 11 27
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48> 11 27
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56> 11 27
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0> 11 27
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0> 11 26 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1> 11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1> 11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2> 11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2> 11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3> 11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3> 11 27
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4> 11 27
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4> 11 27
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5> 11 27
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5> 11 27
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6> 11 27
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6> 11 27
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7> 11 27
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7> 11 27
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0> 11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0> 11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<3..0> 11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0> 11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<3..0> 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0> 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0> 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L 11 28
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0> 11 27
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8> 11 27
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16> 11 27
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24> 11 27
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32> 11 27 28
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40> 11 27
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48> 11 27
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56> 11 27
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0> 11 27 28
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0> 11 27 28
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1> 11 27
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1> 11 27
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2> 11 27
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2> 11 27
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3> 11 27
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3> 11 27
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4> 11 27
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4> 11 27
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5> 11 27
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5> 11 27
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6> 11 27
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6> 11 27
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7> 11 27
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7> 11 27

SYNC_MASTER=K17_MLB SYNC_DATE=05/14/2010

PAGE TITLE: Memory Constraints

Apple Inc.

DRAWING NUMBER: | SIZE: D

REVISION:

BRANCH:

PAGE: 101 OF 132

SHEET: 93 OF 105

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_85D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	ISL3,ISL4,ISL9,ISL10	=4:1_SPACING	?
LVDS	ISL3,ISL4,ISL9,ISL10	=4:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4:1_SPACING	?
LVDS	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	ISL3,ISL4,ISL9,ISL10	=5:1_SPACING	?
SATA_ICOMP	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=5:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	ISL3,ISL4,ISL9,ISL10	=4:1_SPACING	?
USB_RBIAS	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_P 8 17 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_N 8 17 84
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_P 18 88
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_N 18 88
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_P<2..0> 18 88
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_N<2..0> 18 88
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAP<3> 8 18
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAN<3> 8 18
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_P<2..0> 18 88
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_N<2..0> 18 88
DP_SATA_G3_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P 6 16 41
	SATA_90D	SATA	SATA_HDD_R2D_C_N 6 16 41
SATA_HDD_RDVR_R2D	SATA_90D	SATA	SATA_HDD_R2D_P 6 41
	SATA_90D	SATA	SATA_HDD_R2D_N 6 41
DP_SATA_G3_R2D	SATA_90D	SATA	SATA_HDD_R2D_UF_P 6 41
	SATA_90D	SATA	SATA_HDD_R2D_UF_N 6 41
DP_SATA_G3_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_OUT_P 6 41
	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_OUT_N 6 41
DP_SATA_G3_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_IN_P 6 41
	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_IN_N 6 41
DP_SATA_G3_R2D	SATA_90D	SATA	SATA_HDD_R2D_RC_UF_P 6 41
	SATA_90D	SATA	SATA_HDD_R2D_RC_UF_N 6 41
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P 6 16 41
	SATA_90D	SATA	SATA_HDD_D2R_N 6 16 41
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_OUT_P 6 41
	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_OUT_N 6 41
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_IN_P 6 41
	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_IN_N 6 41
SATA_HDD_RDVR_D2R	SATA_90D	SATA	SATA_HDD_D2R_C_P 6 41
	SATA_90D	SATA	SATA_HDD_D2R_C_N 6 41
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P 16 41
	SATA_90D	SATA	SATA_ODD_R2D_C_N 16 41
	SATA_90D	SATA	SATA_ODD_R2D_P 6 41
	SATA_90D	SATA	SATA_ODD_R2D_N 6 41
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_UF_P 41
	SATA_90D	SATA	SATA_ODD_R2D_UF_N 41
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P 16 41
	SATA_90D	SATA	SATA_ODD_D2R_N 16 41
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_C_P 41
	SATA_90D	SATA	SATA_ODD_D2R_C_N 41
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_UF_P 6 41
	SATA_90D	SATA	SATA_ODD_D2R_UF_N 6 41
PCH_SATA3_ICOMP	SATA_50SE	SATA_ICOMP	PCH_SATA3COMP 16
PCH_SATA_ICOMP	SATA_37SE	SATA_ICOMP	PCH_SATAICOMP 16
USB_HUB1_UP	USB_85D	USB	USB_HUB1_UP_P 18 24
	USB_85D	USB	USB_HUB1_UP_N 18 24
USB_HUB2_UP	USB_85D	USB	USB_HUB2_UP_P 18 24
	USB_85D	USB	USB_HUB2_UP_N 18 24
USB_EXTA	USB_85D	USB	USB_EXTA_P 24 42
	USB_85D	USB	USB_EXTA_N 24 42
USB_EXTB	USB_85D	USB	USB_EXTB_P 24 42
	USB_85D	USB	USB_EXTB_N 24 42
USB_EXTC	USB_85D	USB	USB_EXTC_P 24 43
	USB_85D	USB	USB_EXTC_N 24 43
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P 6 31
	USB_85D	USB	USB_CAMERA_CONN_N 6 31
USB_BT	USB_85D	USB	USB_BT_P 6 24 31
	USB_85D	USB	USB_BT_N 6 24 31
USB_TPAD	USB_85D	USB	USB_TPAD_P 24 53
	USB_85D	USB	USB_TPAD_N 24 53
USB_IR	USB_85D	USB	USB_IR_P 24 44
	USB_85D	USB	USB_IR_N 24 44
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS 18
USB_T29A	USB_85D	USB	USB_T29A_P 8 24
	USB_85D	USB	USB_T29A_N 8 24

SYNC_MASTER=K92_YUN SYNC_DATE=06/25/2010

PAGE TITLE: PCH Constraints 1

Apple Inc.

DRAWING NUMBER | SIZE: D

REVISION

BRANCH

PAGE: 102 OF 132

SHEET: 94 OF 105

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_50S	LPC	LPC_AD<3..0>	6 16 45 47 88
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	6 16 45 47 88
LPC_RESET_L	LPC_50S	LPC	LPCPLUS_RESET_L	6 25 47 88
PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	18 25
PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	25 45
PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 25 47
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	6 16 23 26 28 30 32 41 48 62 89
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	6 16 23 26 28 30 32 41 48 62 89
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	16 48
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	16 48
SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK	16 48
SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA	16 48
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	16 57
	HDA_50S	HDA	HDA_BIT_CLK_R	16
HDA_SYNC	HDA_50S	HDA	HDA_SYNC	16 57
	HDA_50S	HDA	HDA_SYNC_R	16
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	16
	HDA_50S	HDA	HDA_RST_L	16 57
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	16 57
	HDA_50S	HDA	AUD_SDI_R	57
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	16 57
	HDA_50S	HDA	HDA_SDOUT_R	16
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	16 47
SPI_CLK	SPI_55S	SPI	SPI_CLK	47
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	16 47
SPI_MOSI	SPI_55S	SPI	SPI_MOSI	47
SPI_MISO	SPI_55S	SPI	SPI_MISO	16 47
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	16 47
	SPI_55S	SPI	SPI_CS0_L	47
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_P	36
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_N	36
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	16 36
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	16 36
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	16 36
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_N	16 36
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P	36
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N	36
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_P	6 31
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_N	6 31
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	16 31
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	16 31
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	6 16 31
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_N	6 16 31
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_PI_P	31
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_PI_N	31
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_PI_P	31
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_PI_N	31
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_P	38
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_N	38
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	16 38
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	16 38
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_P	16 38
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_N	16 38
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	38
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	38
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	16
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	16
PCIE_CLK100M_T29_	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_P	16 33
PCIE_CLK100M_T29_	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_N	16 33
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	16
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	16
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	16
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	16
	CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	16
	CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN	16 25
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	16 74
	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	16 74
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	16 36
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	16 36
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	16 31
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	16 31
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	16 38
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	16 38
PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	16 32
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	16 32
PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_C_P<3..0>	8 33
PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_C_N<3..0>	8 33
PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_P<3..0>	33
PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_N<3..0>	33
PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_P<3..0>	8 33
PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_N<3..0>	8 33
PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_C_P<3..0>	33
PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_C_N<3..0>	33

SYNC_MASTER=K91_MLB SYNC_DATE=07/22/2010

PAGE TITLE

PCH Constraints 2

Apple Inc.

DRAWING NUMBER | SIZE D

REVISION

BRANCH

PAGE 103 OF 132

SHEET 95 OF 105

CAESAR II (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

CAESAR II (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO
	ENET_50S	ENET_3X	ENET_RESET_L 32 36
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0> 36 37
	ENET_100D	ENET_MDI	ENET_MDI_N<3..0> 36 37

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_P 38 40
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_N 38 40
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_P 38 40
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_N 38 40

Port 0 and 2 Not Used

SYNC_MASTER=K91_MLB SYNC_DATE=07/22/2010

PAGE TITLE: Ethernet/FW Constraints

Apple Inc.

DRAWING NUMBER | SIZE: D

REVISION

BRANCH

PAGE: 104 OF 132

SHEET: 96 OF 105

DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

T29/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
T29DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

T29/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
T29_R2D0	T29DP_80D	T29DP	T29_R2D_P<0>	6 85
T29_R2D0	T29DP_80D	T29DP	T29_R2D_N<0>	6 85
T29_R2D1	T29DP_80D	T29DP	T29_R2D_P<1>	6 85
T29_R2D1	T29DP_80D	T29DP	T29_R2D_N<1>	6 85
	T29DP_80D	T29DP	T29_R2D_C_F_P<1..0>	85
	T29DP_80D	T29DP	T29_R2D_C_F_N<1..0>	85
T29_D2R0	T29DP_100D	T29DP	T29_D2R_C_P<0>	6 85 86
T29_D2R0	T29DP_100D	T29DP	T29_D2R_C_N<0>	6 85 86
T29_D2R1	T29DP_100D	T29DP	T29_D2R_C_P<1>	6 85 86
T29_D2R1	T29DP_100D	T29DP	T29_D2R_C_N<1>	6 85 86
	T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_P	6 86
	T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_N	6 86
	T29DP_80D	T29DP	DP_SDRVA_ML_C_P<3..0>	6 85
	T29DP_80D	T29DP	DP_SDRVA_ML_C_N<3..0>	6 85
	T29DP_80D	T29DP	DP_SDRVA_ML_R_P<3..0>	6 85
	T29DP_80D	T29DP	DP_SDRVA_ML_R_N<3..0>	6 85
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_P<2..0:2>	6 85 97
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_N<2..0:2>	6 85 97
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_P<3..1:2>	85
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_N<3..1:2>	85
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_P	85
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_N	85
	T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_P	85
	T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_N	85
	T29DP_80D	T29DP	T29DPA_ML_P<3..0>	6 85 86
	T29DP_80D	T29DP	T29DPA_ML_N<3..0>	6 85 86
	T29DP_80D	T29DP	T29DPA_ML_C_P<3..0>	85 86
	T29DP_80D	T29DP	T29DPA_ML_C_N<3..0>	85 86
	T29DP_80D	T29DP	DP_A_EXT_AUXCH_P	85 86
	T29DP_80D	T29DP	DP_A_EXT_AUXCH_N	85 86
T29_R2D2	T29DP_80D	T29DP	T29_R2D_P<2>	
T29_R2D2	T29DP_80D	T29DP	T29_R2D_N<2>	
T29_R2D3	T29DP_80D	T29DP	T29_R2D_P<3>	
T29_R2D3	T29DP_80D	T29DP	T29_R2D_N<3>	
	T29DP_80D	T29DP	T29_R2D_C_F_P<3..2>	
	T29DP_80D	T29DP	T29_R2D_C_F_N<3..2>	
T29_D2R2	T29DP_100D	T29DP	T29_D2R_C_P<2>	
T29_D2R2	T29DP_100D	T29DP	T29_D2R_C_N<2>	
T29_D2R3	T29DP_100D	T29DP	T29_D2R_C_P<3>	
T29_D2R3	T29DP_100D	T29DP	T29_D2R_C_N<3>	
	T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_P	
	T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_N	
	T29DP_80D	T29DP	DP_SDRVB_ML_C_P<3..0>	
	T29DP_80D	T29DP	DP_SDRVB_ML_C_N<3..0>	
	T29DP_80D	T29DP	DP_SDRVB_ML_R_P<3..0>	
	T29DP_80D	T29DP	DP_SDRVB_ML_R_N<3..0>	
DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP_SDRVB_ML_P<2..0:2>	97
DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP_SDRVB_ML_N<2..0:2>	97
DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP_SDRVB_ML_P<3..1:2>	
DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP_SDRVB_ML_N<3..1:2>	
DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP_SDRVB_AUXCH_P	
DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP_SDRVB_AUXCH_N	
	T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_P	
	T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_N	
	T29DP_80D	T29DP	T29DPB_ML_P<3..0>	
	T29DP_80D	T29DP	T29DPB_ML_N<3..0>	
	T29DP_80D	T29DP	T29DPB_ML_C_P<3..0>	
	T29DP_80D	T29DP	T29DPB_ML_C_N<3..0>	
	T29DP_80D	T29DP	DP_B_EXT_AUXCH_P	
	T29DP_80D	T29DP	DP_B_EXT_AUXCH_N	

Only used on dual-port hosts.

T29 IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_P<3..0>	6 33 79
	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_N<3..0>	6 33 79
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_P<3..0>	6 33
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_N<3..0>	6 33
	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_P	6 33 79
	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_N	6 33 79
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_P	6 33
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_N	6 33
	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_P<3..0>	6 33 79
	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_N<3..0>	6 33 79
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_P<3..0>	6 33
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_N<3..0>	6 33
	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_P	6 33 79
	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_N	6 33 79
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_P	6 33
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_N	6 33
	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_P<3..0>	
	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_N<3..0>	
	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_P	
	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_N	
	T29_I2C_55S	T29_I2C	I2C_T29_SCL	33 48 85
	T29_I2C_55S	T29_I2C	I2C_T29_SDA	33 48 85
T29_SPI_CLK	T29_SPI_55S	T29_SPI	T29_SPI_CLK	33
T29_SPI_MOSI	T29_SPI_55S	T29_SPI	T29_SPI_MOSI	33
T29_SPI_MISO	T29_SPI_55S	T29_SPI	T29_SPI_MISO	33
T29_SPI_CS_L	T29_SPI_55S	T29_SPI	T29_SPI_CS_L	33
	T29DP_80D	T29DP	T29_R2D_C_P<3..0>	6 8 33 85
	T29DP_80D	T29DP	T29_R2D_C_N<3..0>	6 8 33 85
	T29DP_100D	T29DP	T29_D2R_P<3..0>	6 8 33 85
	T29DP_100D	T29DP	T29_D2R_N<3..0>	6 8 33 85

Only used on hosts supporting T29 video-in

SYNC_MASTER=T29_REF SYNC_DATE=10/20/2010

PAGE TITLE

T29 Constraints

Apple Inc.

DRAWING NUMBER | SIZE D

REVISION

BRANCH

PAGE 105 OF 132

SHEET 97 OF 105

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL 6 31 45 48 54 55
SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA 6 31 45 48 54 55
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL 45 48 51
SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA 45 48 51
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL 6 31 45 48 51 80
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA 6 31 45 48 51 80
SMBUS_SMC_BSA_SCL	SMB_50S	SMB	SMBUS_SMC_BSA_SCL 6 45 48 63 64
SMBUS_SMC_BSA_SDA	SMB_50S	SMB	SMBUS_SMC_BSA_SDA 6 45 48 63 64
SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL 45 48 103 104
SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA 45 48 103 104

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P 64
	1TO1_DIFFPAIR		CHGR_CSI_N 64
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P 64
	1TO1_DIFFPAIR		CHGR_CSO_N 64

SYNC_MASTER=K17_MLB SYNC_DATE=05/14/2010

PAGE TITLE: SMC Constraints

Apple Inc.

DRAWING NUMBER | SIZE: D

REVISION

BRANCH

PAGE: 106 OF 132

SHEET: 98 OF 105

GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?
GDDR5_CMD	*	=2x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?
GDDR5_EDC	*	=7x_DIELECTRIC	?

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 0.127 mm. Pairs should be within 0.508mm of entire channel.
DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
Max length of LVDS/DisplayPort/TMDS traces: 13 inches.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

GDDR5 FB A Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_P	76 77
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_N	76 77
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_P	76 77
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_N	76 77
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_A<8..0>	76 77
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_A<8..0>	76 77
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_ABI_L	76 77
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_ABI_L	76 77
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_RAS_L	76 77
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_RAS_L	76 77
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_CAS_L	76 77
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_CAS_L	76 77
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_WE_L	76 77
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_WE_L	76 77
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_CKE_L	76 77
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_CKE_L	76 77
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_CS_L	76 77
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_CS_L	76 77
FB_A0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<0>	76 77
FB_A0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<1>	76 77
FB_A0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<2>	76 77
FB_A0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<3>	76 77
FB_A1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<0>	76 77
FB_A1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<1>	76 77
FB_A1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<2>	76 77
FB_A1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<3>	76 77
FB_A0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<0>	76 77
FB_A0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<1>	76 77
FB_A0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<2>	76 77
FB_A0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<3>	76 77
FB_A1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<0>	76 77
FB_A1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<1>	76 77
FB_A1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<2>	76 77
FB_A1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<3>	76 77
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<0>	76 77
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<0>	76 77
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<1>	76 77
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<1>	76 77
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<0>	76 77
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<0>	76 77
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<1>	76 77
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<1>	76 77
FB_A0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<7..0>	76 77
FB_A0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<15..8>	76 77
FB_A0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<23..16>	76 77
FB_A0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<31..24>	76 77
FB_A1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<7..0>	76 77
FB_A1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<15..8>	76 77
FB_A1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<23..16>	76 77
FB_A1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<31..24>	76 77
FB_AB_RESET	GDDR5_45R50SE	GDDR5_CMD	FB_RESET_L	76 77 78

GDDR5 FB B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_P	76 78
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_N	76 78
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_P	76 78
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_N	76 78
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_A<8..0>	76 78
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_A<8..0>	76 78
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_ABI_L	76 78
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_ABI_L	76 78
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_RAS_L	76 78
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_RAS_L	76 78
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CAS_L	76 78
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CAS_L	76 78
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_WE_L	76 78
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_WE_L	76 78
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CKE_L	76 78
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CKE_L	76 78
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CS_L	76 78
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CS_L	76 78
FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<0>	76 78
FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<1>	76 78
FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<2>	76 78
FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<3>	76 78
FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<0>	76 78
FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<1>	76 78
FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<2>	76 78
FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<3>	76 78
FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<0>	76 78
FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<1>	76 78
FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<2>	76 78
FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<3>	76 78
FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<0>	76 78
FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<1>	76 78
FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<2>	76 78
FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<3>	76 78
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<0>	76 78
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<0>	76 78
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<1>	76 78
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<1>	76 78
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<0>	76 78
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<0>	76 78
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<1>	76 78
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<1>	76 78
FB_B0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<7..0>	76 78
FB_B0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<15..8>	76 78
FB_B0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<23..16>	76 78
FB_B0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<31..24>	76 78
FB_B1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<7..0>	76 78
FB_B1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<15..8>	76 78
FB_B1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<23..16>	76 78
FB_B1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<31..24>	76 78

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_P	84 88
LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_N	84 88
LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_P<2..0>	84 88
LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_N<2..0>	84 88
LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_P	84 88
LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_N	84 88
LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_P<2..0>	84 88
LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_N<2..0>	84 88
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_P	6 83
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_N	6 83
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_P	6 83
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_N	6 83
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_P	83 84
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_N	83 84
	LVDS_85D	LVDS	LVDS_CONN_A_DATA_P<2..0>	6 83 84
	LVDS_85D	LVDS	LVDS_CONN_A_DATA_N<2..0>	6 83 84
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_P	83 84
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_N	83 84
	LVDS_85D	LVDS	LVDS_CONN_B_DATA_P<2..0>	6 83 84
	LVDS_85D	LVDS	LVDS_CONN_B_DATA_N<2..0>	6 83 84

Whistler Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
GPU_CLK27M	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M	79 80
GPU_CLK100M	CLK_SLOW_55S	CLK_SLOW	GPU_CLK100M	79 80
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_P	79 88
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_N	79 88
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_P<2..0>	79 88
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_N<2..0>	79 88
LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_P<3>	79 80
LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_N<3>	79 80
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_P<2..0>	79 88
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_N<2..0>	79 88
LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_P<3>	79 80
LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_N<3>	79 80
DP_MI	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_P<3..0>	79 85
	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_N<3..0>	79 85
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_P	84 85
	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_N	84 85
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_P	79 84
	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_N	79 84

SYNC_MASTER=K91_MLB SYNC_DATE=07/21/2010

PAGE TITLE
GPU (Whistler) CONSTRAINTS

Apple Inc.

DRAWING NUMBER | SIZE: D
REVISION
BRANCH
PAGE: 107 OF 132
SHEET: 99 OF 105

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*			0.09 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D	*			0.09 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D	*			0.09 MM	10 mm		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_85D	BGA	LVDS_85D
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

K92 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_100D	ENETCONN	ENETCONN_P<3..0>	37
	ENET_100D	ENETCONN	ENETCONN_N<3..0>	37
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_P	49 65
	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_N	49 65
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAISNS_R_P	49
	SENSE_1TO1_55S	SENSE	VCCSAISNS_R_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_R_P	49
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_R_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_P	49 70
	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_N	49 70
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOISNS_R_P	49
	SENSE_1TO1_55S	SENSE	CPUVCCIOISNS_R_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUISENS_N	49
	SENSE_1TO1_55S	SENSE	GPUISENS_P	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_N	49 67
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_P	49 67
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	31 103
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	31 103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_P	103
	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V8_S0GPU_P	103
	SENSE_1TO1_55S	SENSE	ISNS_PP1V8_S0GPU_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_N	41 103
	SENSE_1TO1_55S	SENSE	ISNS_HDD_P	41 103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S0GPU_P	103
	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S0GPU_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	89 103
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	89 103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_N	41 103
	SENSE_1TO1_55S	SENSE	ISNS_ODD_P	41 103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_P	50
	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_P	50
	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_P	50
	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_P	50 68 69
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_N	50 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_P	50
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_P	50
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_P	50 69
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_N	50 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_P	50
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_R_P	50
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_R_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_P	103
	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V8_S0GPU_R_P	103
	SENSE_1TO1_55S	SENSE	ISNS_PP1V8_S0GPU_R_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S0GPU_R_P	103
	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S0GPU_R_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_P	103
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_P	103
	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_P	103
	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_N	103
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	BI_MIC_P	61 62
	AUDIODIFF	AUDIO	BI_MIC_N	61 62
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	58 60
	AUDIODIFF	AUDIO	AUD_LO1_R_N	58 60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	57 60
	AUDIODIFF	AUDIO	AUD_LO2_R_N	57 60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_P	57 60
	AUDIODIFF	AUDIO	AUD_LO3_R_N	57 60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_P	57 60
	AUDIODIFF	AUDIO	AUD_LO3_L_N	57 60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INR_P	57 62
	AUDIODIFF	AUDIO	AUD_MIC_INR_N	57 62
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_P	57 62
	AUDIODIFF	AUDIO	AUD_MIC_INL_N	57 62
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_BL_IN_L_P	60
	AUDIODIFF	AUDIO	SPKRAMP_BL_IN_L_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_FL_IN_L_P	60
	AUDIODIFF	AUDIO	SPKRAMP_FL_IN_L_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_BR_IN_L_P	60
	AUDIODIFF	AUDIO	SPKRAMP_BR_IN_L_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_FR_IN_L_P	60
	AUDIODIFF	AUDIO	SPKRAMP_FR_IN_L_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_LFE_IN_L_P	60
	AUDIODIFF	AUDIO	SPKRAMP_LFE_IN_L_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375BL_IN_P	60
	AUDIODIFF	AUDIO	SSM2375BL_IN_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375FL_IN_P	60
	AUDIODIFF	AUDIO	SSM2375FL_IN_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375BR_IN_P	60
	AUDIODIFF	AUDIO	SSM2375BR_IN_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375FR_IN_P	60
	AUDIODIFF	AUDIO	SSM2375FR_IN_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375LFE_IN_P	60
	AUDIODIFF	AUDIO	SSM2375LFE_IN_N	60

K92 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE_EXCARD_R2D	PCIE_85D	PCIE	PCIE_EXCARD_R2D_P	6 32
	PCIE_85D	PCIE	PCIE_EXCARD_R2D_N	6 32
PCIE_EXCARD_D2R	PCIE_85D	PCIE	PCIE_EXCARD_D2R_P	6 16 32
	PCIE_85D	PCIE	PCIE_EXCARD_D2R_N	6 16 32
PCIE_EXCARD_R2D	PCIE_85D	PCIE	PCIE_EXCARD_R2D_C_P	16 32
	PCIE_85D	PCIE	PCIE_EXCARD_R2D_C_N	16 32
PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_P	6 32
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_N	6 32
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	6 31
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	6 31
	1TO1_DIFFPAIR		CHGR_CSI_R_P	64
	1TO1_DIFFPAIR		CHGR_CSI_R_N	64
	1TO1_DIFFPAIR		CHGR_CSO_R_P	50 64
	1TO1_DIFFPAIR		CHGR_CSO_R_N	50 64
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_P	42
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_N	42
(USB_EXTA)	USB_85D	USB	USB2_LT1_P	42
(USB_EXTA)	USB_85D	USB	USB2_LT1_N	42
	USB_85D	USB	CONN_USB2_BT_P	
	USB_85D	USB	CONN_USB2_BT_N	
(USB_EXTB)	USB_85D	USB	USB_LT2_P	42
	USB_85D	USB	USB_LT2_N	42
USB_EXCARD	USB_85D	USB	USB_EXCARD_P	8 24 32
	USB_85D	USB	USB_EXCARD_N	8 24 32
USB_EXCARD	USB_85D	USB	USB2_EXCARD_CONN_P	6 32
	USB_85D	USB	USB2_EXCARD_CONN_N	6 32
(USB_EXTC)	USB_85D	USB	USB_LT3_P	43
	USB_85D	USB	USB_LT3_N	43
	USB_85D	USB	USB_TPAD_R_P	53
	USB_85D	USB	USB_TPAD_R_N	53
		SB_POWER	PP3V3_S5	48 56 71 72 73 83 86 91 102 104 6 7 17 19 20 22 23 24 25 35 46
		SB_POWER	PP3V3_S0	61 62 72 73 80 83 84 86 88 89 6 7 12 23 25 26 29 32 35 36 39 49 41 46 48 49 50 51 52 54 57
		SB_POWER	PP1V5_S3RS0	7 72 104 91 102
		GND	GND	

K92 Specific Net Properties
K91 does not have

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	51
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P	9 51
	THERM_1TO1_55S	THERM	CPU_THERMD_N	9 51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	51
	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P	51 79
	THERM_1TO1_55S	THERM	GPU_TDIODE_N	51 79
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	T29_THERMD_P	33 51
	THERM_1TO1_55S	THERM	T29_THERMD_N	51

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S3_P	104
	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S3_N	104
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S5_N	104
	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S5_P	104
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP5V_S3_N	104
	SENSE_1TO1_55S	SENSE	ISNS_PP5V_S3_P	104
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V05_S0PCH_N	104
	SENSE_1TO1_55S	SENSE	ISNS_PP1V05_S0PCH_P	104
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP5V_S0_N	104
	SENSE_1TO1_55S	SENSE	ISNS_PP5V_S0_P	104
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPU_DDR_N	104
	SENSE_1TO1_55S	SENSE	ISNS_CPU_DDR_P	104

SYNC_MASTER=K91_MLB SYNC_DATE=07/22/2010

PAGE TITLE: Project Specific Constraints

Apple Inc.

DRAWING NUMBER | SIZE: D

REVISION

BRANCH

PAGE: 108 OF 132

SHEET: 100 OF 105

Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.095 MM			
37_OHM_SE	*	Y	0.155 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.13 MM	0.13 MM			
45_OHM_SE	*	Y	0.099 MM	0.099 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL9,ISL10	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.135 MM	0.135 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL9,ISL10	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.090 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.090 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?

NOTE: Based on K92 mlb stackup.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

SYNC_MASTER=K17_MLB SYNC_DATE=05/14/2010

PAGE TITLE: PCB Rule Definitions

Apple Inc.

DRAWING NUMBER | SIZE: D

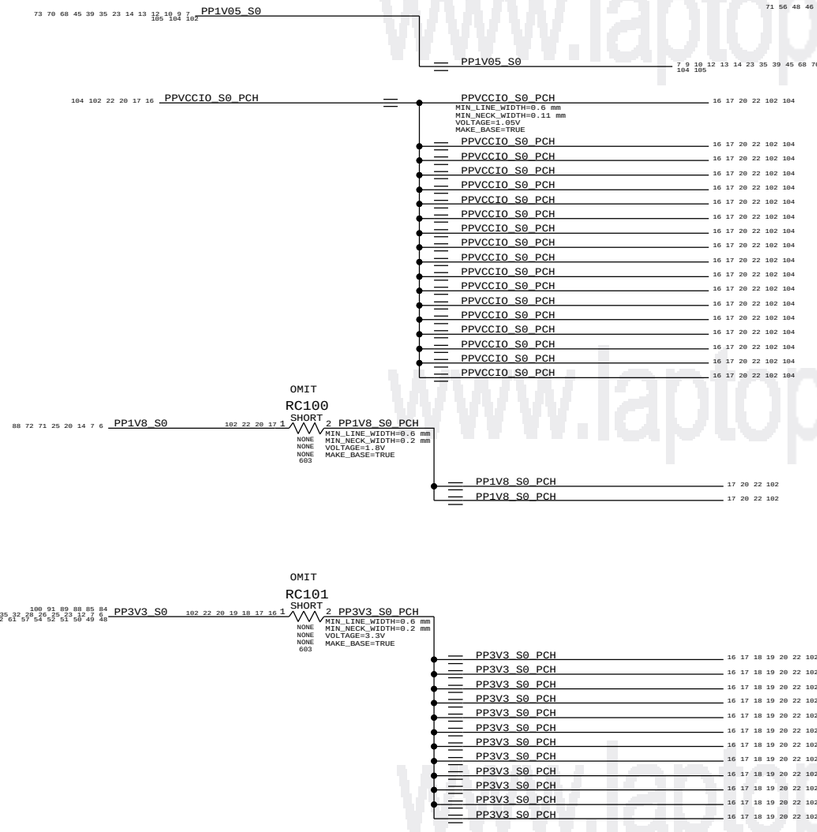
REVISION

BRANCH

PAGE: 109 OF 132

SHEET: 101 OF 105

PCH "S0" Rails



PCH "S5" Rail

SYNC_MASTER=K17_MLB SYNC_DATE=04/27/2010

PAGE TITLE

PCH Power Aliases

Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH

PAGE 121 OF 132

SHEET 102 OF 105

LCD BKLT Current Sense

PP5V_S5 → DEBUG_ADC CD144 0.1UF 20% 10V CERM 402

UD120 INA214 SC70
- IN- ← ISNS_LCDBKLT_N
- IN+ ← ISNS_LCDBKLT_P
- OUT → ISNS_LCDBKLT_IOUT
- REF → GND
- V+ → DEBUG_ADC
- GND
- GAIN: 100X

Sense Resistor 0.025 Ohm
EDP Current: 0.715A

ISNS_LCDBKLT_IOUT → DEBUG_ADC RD150 4.53K 1% 1/16W MF-LF 402 → ADC_CH0
PLACE_NEAR=UD100.22:5mm
DEBUG_ADC CD145 0.22UF 20% 6.3V XSR 402
PLACE_NEAR=UD100.22:5mm

LCD BKLT Voltage Sense

XWD150 SM
PPVOUT_S0_LCDBKLT → VOUT_S0_LCDBKLT_XW

DEBUG_ADC RD156 1M 1% 1/16W MF-LF 402
VOUT_S0_LCDBKLT_DIV
DEBUG_ADC RD157 46.4K 1% 1/16W MF-LF 402

PLACE_NEAR=UD100.5:5mm
DEBUG_ADC RD158 226K 1% 1/16W MF-LF 402 → ADC_CH7
DEBUG_ADC CD152 2.2UF 10% 6.3V XSR 402
PLACE_NEAR=UD100.5:5mm

DIVIDER: ~ 1/22

PP5V_S5 → DEBUG_ADC RD103 10 5% 1/16W MF-LF 402 → PP5V_S5_DEBUG_ADC_AVDD_FILT
- DEBUG_ADC CD100 0.1UF 20% 10V CERM 402
- DEBUG_ADC CD101 10UF 20% 6.3V XSR 603

PP5V_S5_DEBUG_ADC_DVDD_FILT
- DEBUG_ADC CD102 0.1UF 20% 10V CERM 402
- DEBUG_ADC CD103 10UF 20% 6.3V XSR 603

DEBUG_ADC RD104 10 5% 1/16W MF-LF 402 → PP5V_S5

UD100 LTC2309 QFN
- AVDD, DVDD ← PP5V_S5_DEBUG_ADC_AVDD_FILT / PP5V_S5_DEBUG_ADC_DVDD_FILT
- CH0 ← ADC_CH0
- CH1 ← ADC_CH1
- CH2 ← ADC_CH2
- CH3 ← ADC_CH3
- CH4 ← ADC_CH4
- CH5 ← ADC_CH5
- CH6 ← ADC_CH6
- CH7 ← ADC_CH7
- COM → GND
- THRM PAD → GND
- AD0 → DEBUG_ADC RD101 33 5% 1/16W MF-LF 402 → SMBUS_SMC_MGMT_SDA
- AD1 → DEBUG_ADC RD102 33 5% 1/16W MF-LF 402 → SMBUS_SMC_MGMT_SCL
- SDA ← ADC_SDA
- SCL ← ADC_SCL
- VREF → ADC_VREF
- REFCOMP → ADC_REFCOMP
- DEBUG_ADC CD104 0.1UF 20% 10V CERM 402
- DEBUG_ADC CD105 10UF 20% 6.3V XSR 603
- DEBUG_ADC CD106 2.2UF 20% 6.3V CERM 402-LF

I2C ADDRESS: 0X10 / 0X11
ADC RANGE: 0V TO 4.096V
LSB: 0.001V

AIRPORT Current Sense

PP5V_S5 → DEBUG_ADC CD130 0.1UF 20% 10V CERM 402

Sense Resistor 0.005 Ohm
EDP Current: 1.06A

ISNS_AIRPORT_P → DEBUG_ADC RD130 2.61K 1% 1/16W MF-LF 402 → ISNS_AIRPORT_R_P
ISNS_AIRPORT_N → DEBUG_ADC RD131 2.61K 1% 1/16W MF-LF 402 → ISNS_AIRPORT_R_N

UD130 OPA2333 DFN
- V+ ← PP5V_S5
- V- → GND
- THRM → GND
- GAIN: 383X

PLACE_NEAR=UD100.1:5mm
DEBUG_ADC RD134 226K 1% 1/16W MF-LF 402 → ADC_CH2
ISNS_AIRPORT_IOUT
DEBUG_ADC CD131 2.2UF 10% 6.3V XSR 402
PLACE_NEAR=UD100.24:5mm

DEBUG_ADC RD132 1M 1% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY
DEBUG_ADC RD133 1M 1% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY

ODD Current Sense

Sense Resistor 0.005 Ohm
EDP Current: 1.8A

ISNS_ODD_P → DEBUG_ADC RD151 4.42K 1% 1/16W MF-LF 402 → ISNS_ODD_R_P
ISNS_ODD_N → DEBUG_ADC RD152 4.42K 1% 1/16W MF-LF 402 → ISNS_ODD_R_N

PP5V_S5 → DEBUG_ADC CD151 0.1UF 20% 10V CERM 402

UD140 OPA2333 DFN
- V+ ← PP5V_S5
- V- → GND
- THRM → GND
- GAIN: 226X

ISNS_ODD_IOUT
PLACE_NEAR=UD100.1:5mm
NOSTUFF RD155 226K 1% 1/16W MF-LF 402 → ADC_CH3
NOSTUFF CD150 2.2UF 10% 6.3V XSR 402
PLACE_NEAR=UD100.1:5mm

DEBUG_ADC RD153 1M 1% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY
DEBUG_ADC RD154 1M 1% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY

GPU 1.0V Current Sense

EDP Current: 2.846A

PP1V0_S0GPU_ISNS_R → RD145 0.003 0612 MF 1W 1% → PP1V0_S0GPU_ISNS_N → PP1V0_S0GPU

ISNS_PP1V0_S0GPU_P → DEBUG_ADC RD140 4.22K 1% 1/16W MF-LF 402 → ISNS_PP1V0_S0GPU_R_P
ISNS_PP1V0_S0GPU_N → DEBUG_ADC RD141 4.22K 1% 1/16W MF-LF 402 → ISNS_PP1V0_S0GPU_R_N

UD130 OPA2333 DFN
- V+ ← PP5V_S5
- V- → GND
- THRM → GND
- GAIN: 237X

ISNS_1V0_GPU_IOUT
PLACE_NEAR=UD100.2:8mm
DEBUG_ADC RD144 226K 1% 1/16W MF-LF 402 → ADC_CH4
DEBUG_ADC CD142 2.2UF 10% 6.3V X5R 402
PLACE_NEAR=UD100.2:8mm

DEBUG_ADC RD142 1M 1% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY
DEBUG_ADC RD143 1M 1% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY

HDD Current Sense

Sense Resistor 0.005 Ohm
EDP Current: 1.2A

ISNS_HDD_P → DEBUG_ADC RD160 2.94K 1% 1/16W MF-LF 402 → ISNS_HDD_R_P
ISNS_HDD_N → DEBUG_ADC RD161 2.94K 1% 1/16W MF-LF 402 → ISNS_HDD_R_N

UD140 OPA2333 DFN
- V+ ← PP5V_S5
- V- → GND
- THRM → GND
- GAIN: 340X

ISNS_HDD_IOUT
PLACE_NEAR=UD100.3:5mm
DEBUG_ADC RD164 226K 1% 1/16W MF-LF 402 → ADC_CH5
DEBUG_ADC CD140 2.2UF 10% 6.3V X5R 402
PLACE_NEAR=UD100.3:5mm

DEBUG_ADC RD162 1M 1% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY
DEBUG_ADC RD163 1M 1% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY

GPU 1.8V Current Sense

PP5V_S5 → DEBUG_ADC CD180 0.1UF 20% 10V CERM 402

EDP Current: 2.406SA

PP1V8_S0GPU_ISNS_R → RD186 0.005 1% 1W MF 0612 → PP1V8_S0GPU_ISNS_N → PP1V8_S0GPU

ISNS_PP1V8_S0GPU_P → DEBUG_ADC RD187 5.90K 1% 1/16W MF-LF 402 → ISNS_PP1V8_S0GPU_R_P
ISNS_PP1V8_S0GPU_N → DEBUG_ADC RD188 5.90K 1% 1/16W MF-LF 402 → ISNS_PP1V8_S0GPU_R_N

UD180 OPA2333 DFN
- V+ ← PP5V_S5
- V- → GND
- THRM → GND
- GAIN: 169x

ISNS_1V8_S0GPU_IOUT
PLACE_NEAR=UD.23:5mm
RD191 4.53K 1% 1/16W MF-LF 402 → ADC_CH1
DEBUG_ADC CD182 0.22UF 20% 6.3V X5R 402
PLACE_NEAR=UD.23:5mm

DEBUG_ADC RD189 1M 1% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY
DEBUG_ADC RD190 1M 1% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY

1.5V FB Current Sense

EDP Current: 7.8A

PP1V5_S0GPU_ISNS_R → RD180 0.002 1% 1W MF 0612 → PP1V5R1V35_GPU_FB_ISNS

ISNS_PP1V5_S0GPU_P → DEBUG_ADC RD181 7.68K 1% 1/16W MF-LF 402 → ISNS_PP1V5_S0GPU_R_P
ISNS_PP1V5_S0GPU_N → DEBUG_ADC RD182 7.68K 1% 1/16W MF-LF 402 → ISNS_PP1V5_S0GPU_R_N

UD180 OPA2333 DFN
- V+ ← PP5V_S5
- V- → GND
- THRM → GND
- GAIN: 130x

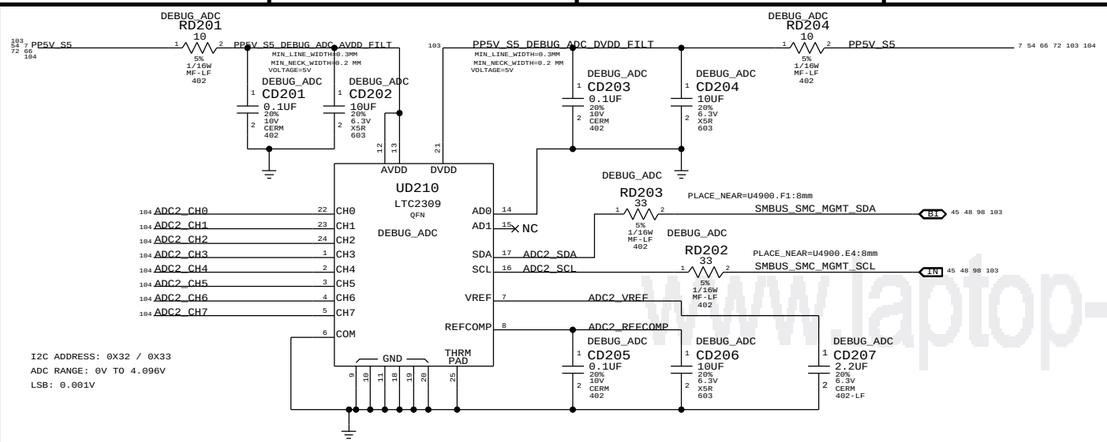
ISNS_1V5_S0GPU_IOUT
PLACE_NEAR=UD100.4:5mm
DEBUG_ADC RD185 4.53K 1% 1/16W MF-LF 402 → ADC_CH6
DEBUG_ADC CD181 0.22UF 20% 6.3V X5R 402
PLACE_NEAR=UD100.4:5mm

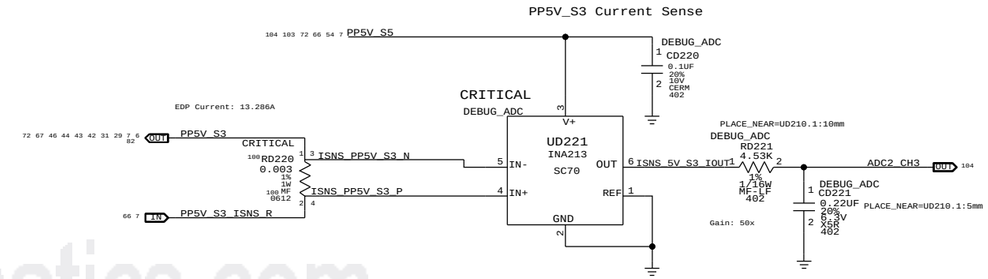
DEBUG_ADC RD183 1M 1% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY
DEBUG_ADC RD184 1M 1% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY

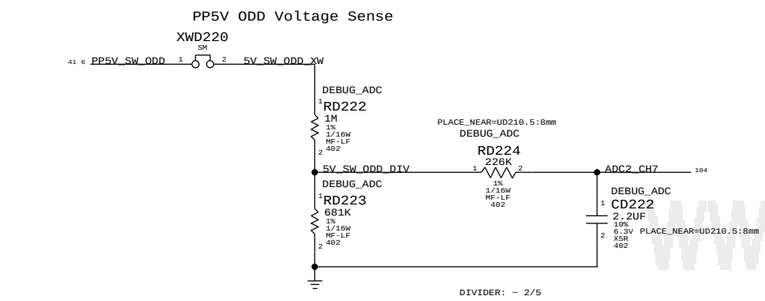
SYNC_MASTER=K92_DINESH
SYNC_DATE=09/07/2010
PAGE TITLE
DEBUG SENSORS AND ADC

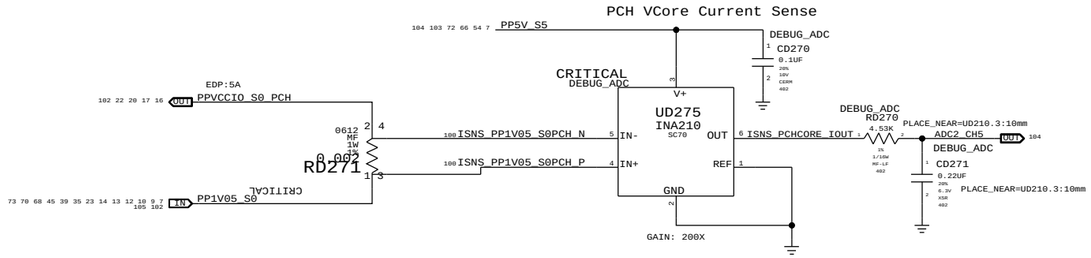
Apple Inc.

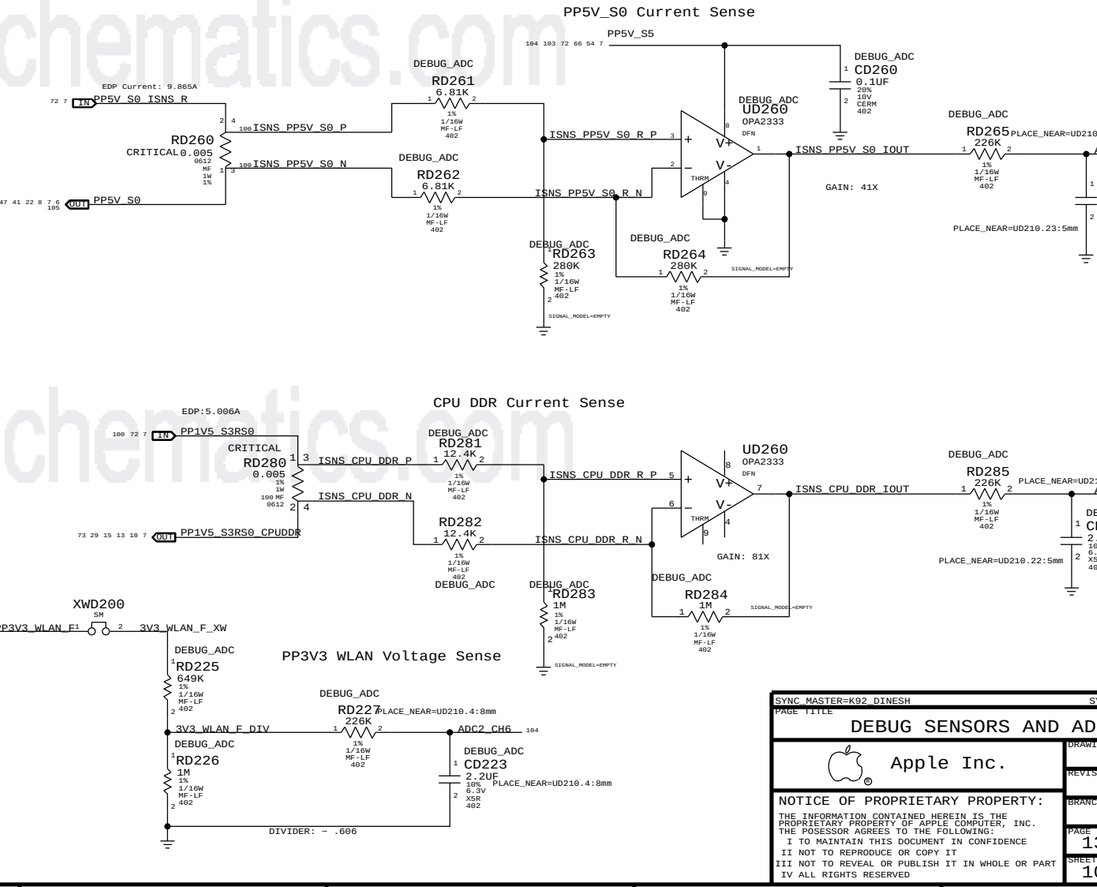
DRAWING NUMBER
SIZE D
REVISION
BRANCH
PAGE 130 OF 132
SHEET 103 OF 105

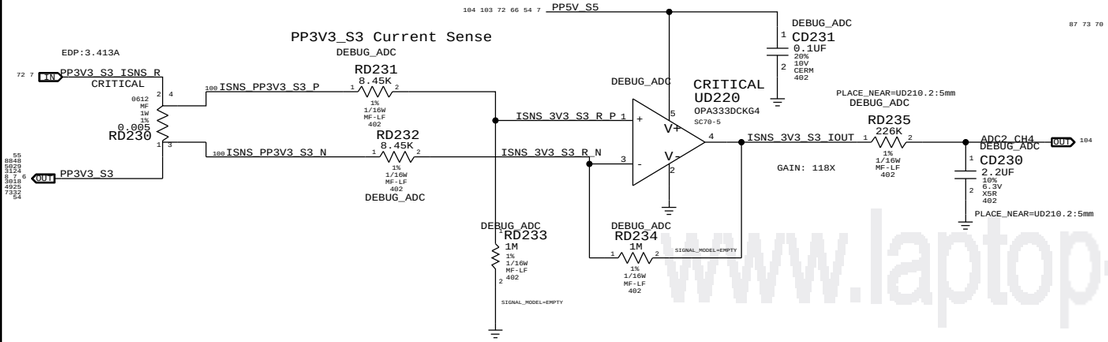


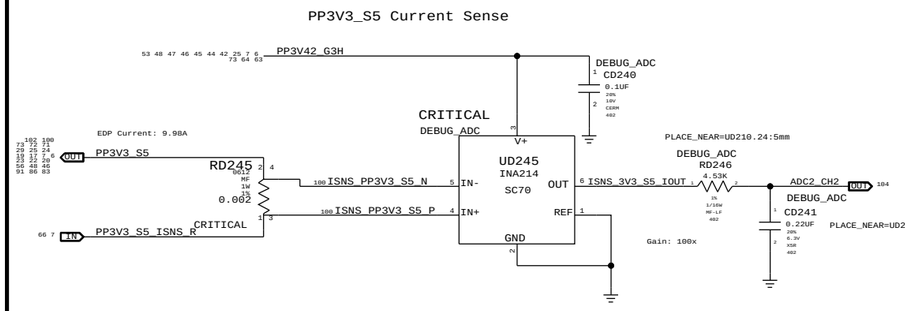












SYNC_MASTER=K92_DINESH SYNC_DATE=07/28/2010

PAGE TITLE

DEBUG SENSORS AND ADC 2

Apple Inc.

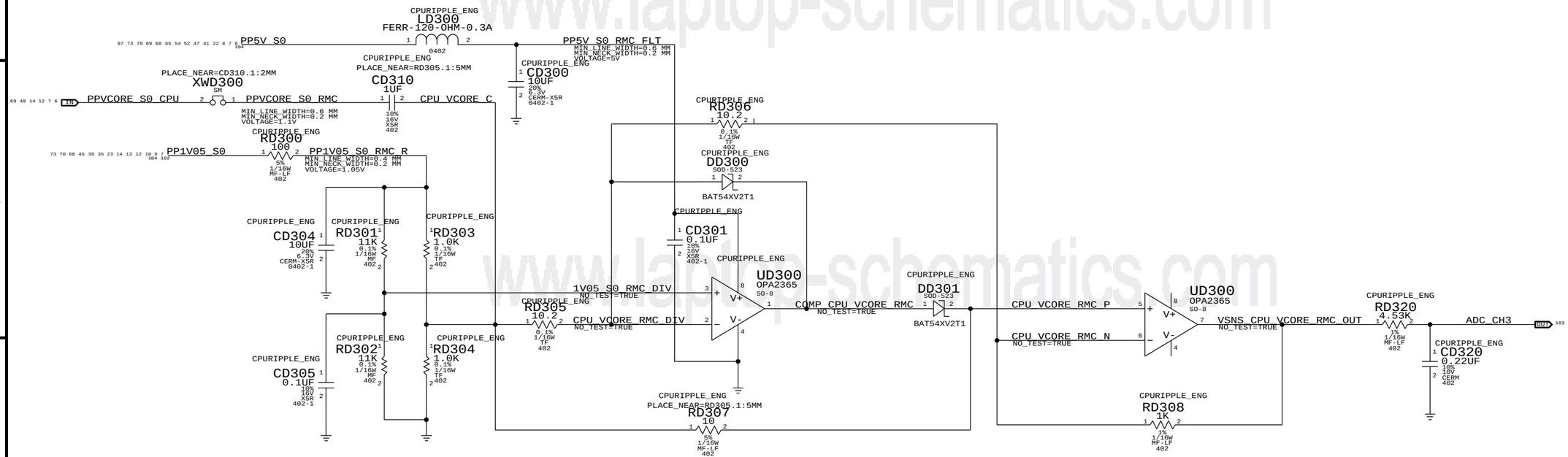
DRAWING NUMBER | SIZE D

REVISION

BRANCH

PAGE 131 OF 132

SHEET 104 OF 105



SYNC_MASTER=K92_DINESH SYNC_DATE=08/23/2010

PAGE TITLE

Power Supplies BIST

Apple Inc.

DRAWING NUMBER | SIZE D

REVISION

BRANCH

PAGE 132 OF 132

SHEET 105 OF 105