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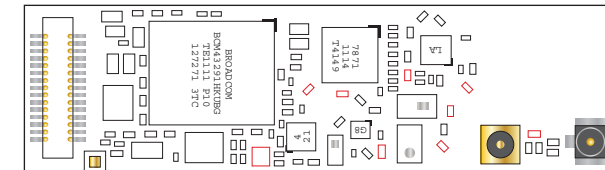
READ BEFORE PROCEED!

- PRINTS MARKED WITH COPPER ARE NC, EMPTY!
- PRINTS MARKED WITH GOLD ARE CONNECTED TO TEST POINTS ONLY
- NOSTUFF COMPONENTS (NOT MOUNTED)

D

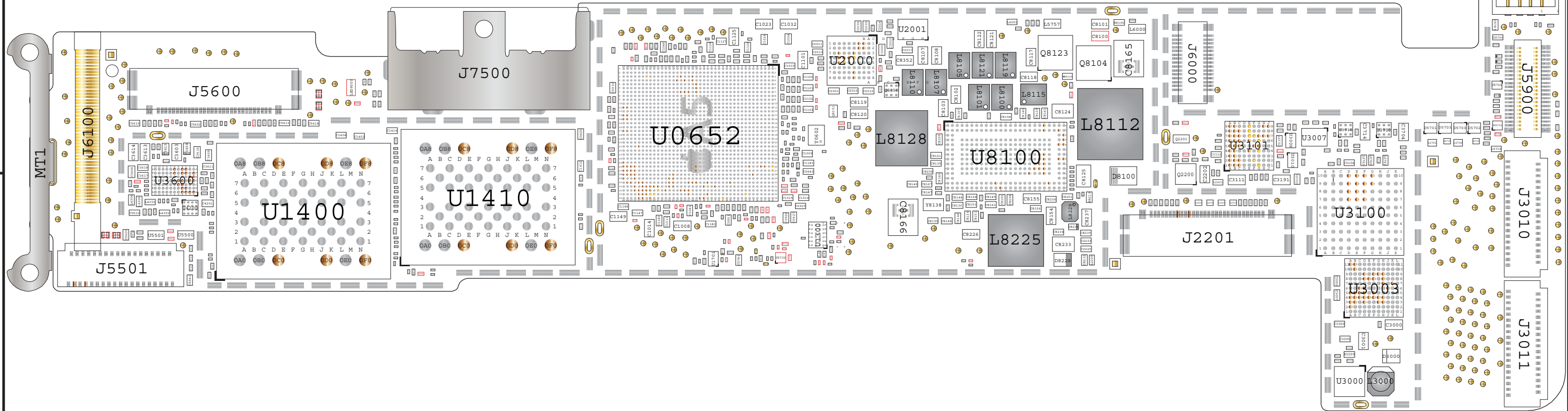
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WLAN/BT PCB



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820-2875-05 MLB TOP PCB

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COMPEQ

HF/e1

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820-2875-05 MLB BOTTOM PCB

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- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

# K94 CHOPIN MLB

PVT

REV. A

REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
A	0001052699	PRODUCTION RELEASED		2011-01-10

LAST\_MODIFIED=Mon Jan 10 13:11:06 2011

PDF	CSA	CONTENTS	SYNC	MASTER	DATE	PDF	CSA	CONTENTS	SYNC	MASTER	DATE
1	1	TABLE OF CONTENTS	MIKE	N/A		32	73	POWER: ALIASES	YOSH	N/A	
2	2	BLOCK DIAGRAM: SYSTEM	MIKE	N/A		33	75	POWER: BATTERY CONNECTOR	YOSH	N/A	
3	5	BOM TABLE	MIKE	N/A		34	81	POWER: PMU	YOSH	N/A	
4	6	AP: MAIN	JAMES	N/A		35	82	POWER: PMU	YOSH	N/A	
5	7	AP: I/Os	JAMES	N/A		36	83	POWER: 3.3V VR	YOSH	N/A	
6	8	AP: NAND	JAMES	N/A		37	90	DEBUG AND MISC	MIKE	N/A	
7	9	AP: TV, DP, MIPI	JAMES	N/A		38	93	FCT/ICT TEST/BRACKETS	MIKE	N/A	
8	10	AP: PWR	JAMES	N/A		39	100	CONSTRAINTS: ASSIGNMENTS	MIKE	N/A	
9	11	AP: PWR	JAMES	N/A		40	101	CONSTRAINTS: ASSIGNMENTS	MIKE	N/A	
10	12	AP: MISC & ALIASES	JAMES	N/A		41	102	CONSTRAINTS: MLB RULES	MIKE	N/A	
11	13	AP: VIDEO BUFFER, BB USB MUXES	JAMES	N/A		42	106	CONSTRAINTS: RF RULES	MIKE	N/A	
12	14	NAND	JONATHAN	N/A							
13	17	VIDEO: DISPLAY PORT	JAMES	N/A							
14	20	VIDEO: MLC	MIKE	N/A							
15	21	VIDEO: MLC ALIASES	MIKE	N/A							
16	22	VIDEO: LVDS CONNECTOR	ALEX	N/A							
17	30	GRAPE: GROUNDHOG, CONN, BOOST	RAMSIN	N/A							
18	31	GRAPE: Z1, Z2	RAMSIN	N/A							
19	36	AUDIO: L63 CODEC	LENG	N/A							
20	37	AUDIO: SPEAKER AMP	LENG	N/A							
21	38	AUDIO: HEADPHONE OUT	LENG	N/A							
22	39	AUDIO: BLANK	LENG	N/A							
23	42	AUDIO: DETECT/MIC BIAS	LENG	N/A							
24	43	AUDIO: HP/MIC FILTERS	LENG	N/A							
25	54	CONNECTOR: CANADA FLEX CONN, SENSOR PANEL ALIASES	MARK B.	N/A							
26	55	CONNECTOR: CANADA FLEX FILTERS	MARK B.	N/A							
27	56	CONNECTOR: SENSOR PANEL CONNECTOR	MARK B.	N/A							
28	57	IO FLEX: DOCK COMPONENTS	JAMES	N/A							
29	59	IO FELX: B2B Connector	JAMES	N/A							
30	60	CONNECTOR: X23 WIFI/BT	MIKE	N/A							
31	61	CONNECTOR: X24 CELLULAR/GPS	MIKE	N/A							

DRAWING  
TITLE-BACH  
ABBREV-DRAWING

DRAWING TITLE		CHOPIN MLB	
DRAWING NUMBER		051-8962	SIZE D
REVISION		A.0.0	
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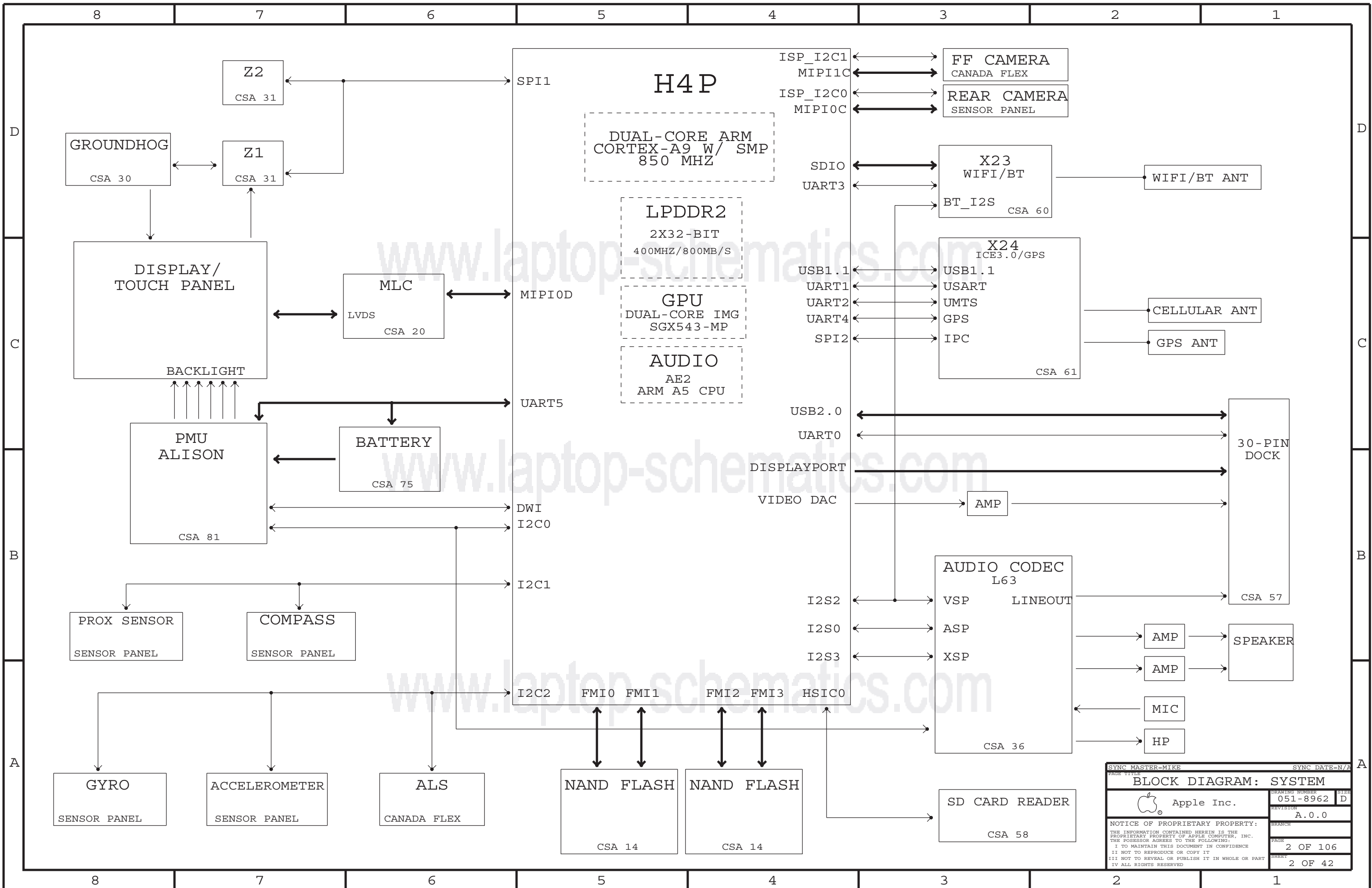
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BLOCK DIAGRAM: SYSTEM			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8962	D
		REVISION	
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		SHEET	2 OF 42

Page Notes

Power aliases required by this page:  
(NONE)

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:

ALL AVAIL BOM OPTIONS

COMMON  
ALTERNATE  
16GB\_PROD  
32GB\_PROD  
64GB\_PROD  
BKLT\_PLL  
DEVELOPMENT\_JTAG  
DEVELOPMENT\_JTAG\_TAP  
JTAG\_DAP  
JTAG\_TAP\_NOT  
SPEAKER  
INTERNAL\_MIC  
PORTRAIT\_DOCK  
MLC\_DEV  
MLC\_PROD  
K93  
K94

BOM GROUP	BOM OPTIONS
BASIC	COMMON, ALTERNATE

ADD DEVELOPMENT AND OTHER BOMS ONCE YOU GET BOM NUMBERS

# BOM OPTIONS

PROGRAMMABLE PARTS

SCH AND BOARD P/N

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-8962	1	SCH CHOPIN AUDIO MLB K94	SCH1	
820-3069	1	PCBF CHOPIN AUDIO MLB K94	PCB1	

PD PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
806-1396	1	FENCE GRAPE MLB K93/K94	FENCE1	
806-1397	1	CAN GRAPE MLB K93/K94	CAN1	NOSTUFF
806-1398	1	FENCE CPU MLB K93/K94	FENCE2	
806-1399	1	CAN CPU MLB K93/K94	CAN2	NOSTUFF
806-1400	1	FENCE NAND MLB K93/K94	FENCE3	
806-1401	1	CAN NAND MLB K93/K94	CAN3	NOSTUFF

TOP BARCODE LABEL/EEE CODES  
(ONLY ONE IS USED PER BOM)


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7651	1	EEEE FOR 639-1180 (K93 16G)	DH36	CRITICAL	EEEE_K93_16G
825-7651	1	EEEE FOR 639-1426 (K93 32G)	DH37	CRITICAL	EEEE_K93_32G
825-7651	1	EEEE FOR 639-1428 (K93 64G)	DG99	CRITICAL	EEEE_K93_64G
825-7651	1	EEEE FOR 639-1112 (K94 16G)	DPC4	CRITICAL	EEEE_K94_16G
825-7651	1	EEEE FOR 639-1181 (K94 32G)	DPC5	CRITICAL	EEEE_K94_32G
825-7651	1	EEEE FOR 639-1182 (K94 64G)	DPC6	CRITICAL	EEEE_K94_64G
825-7651	1	EEEE FOR 639-1430 (K95 16G)	DH3C	CRITICAL	EEEE_K95_16G
825-7651	1	EEEE FOR 639-1427 (K95 32G)	DH3D	CRITICAL	EEEE_K95_32G
825-7651	1	EEEE FOR 639-1429 (K95 64G)	DG9C	CRITICAL	EEEE_K95_64G

BOTTOM LABEL TYPE 1

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7639	1	631- B/C LABEL	LBL1	CRITICAL	
825-7639	1	639- B/C LABEL	LBL2	CRITICAL	

BOTTOM LABEL TYPE 2

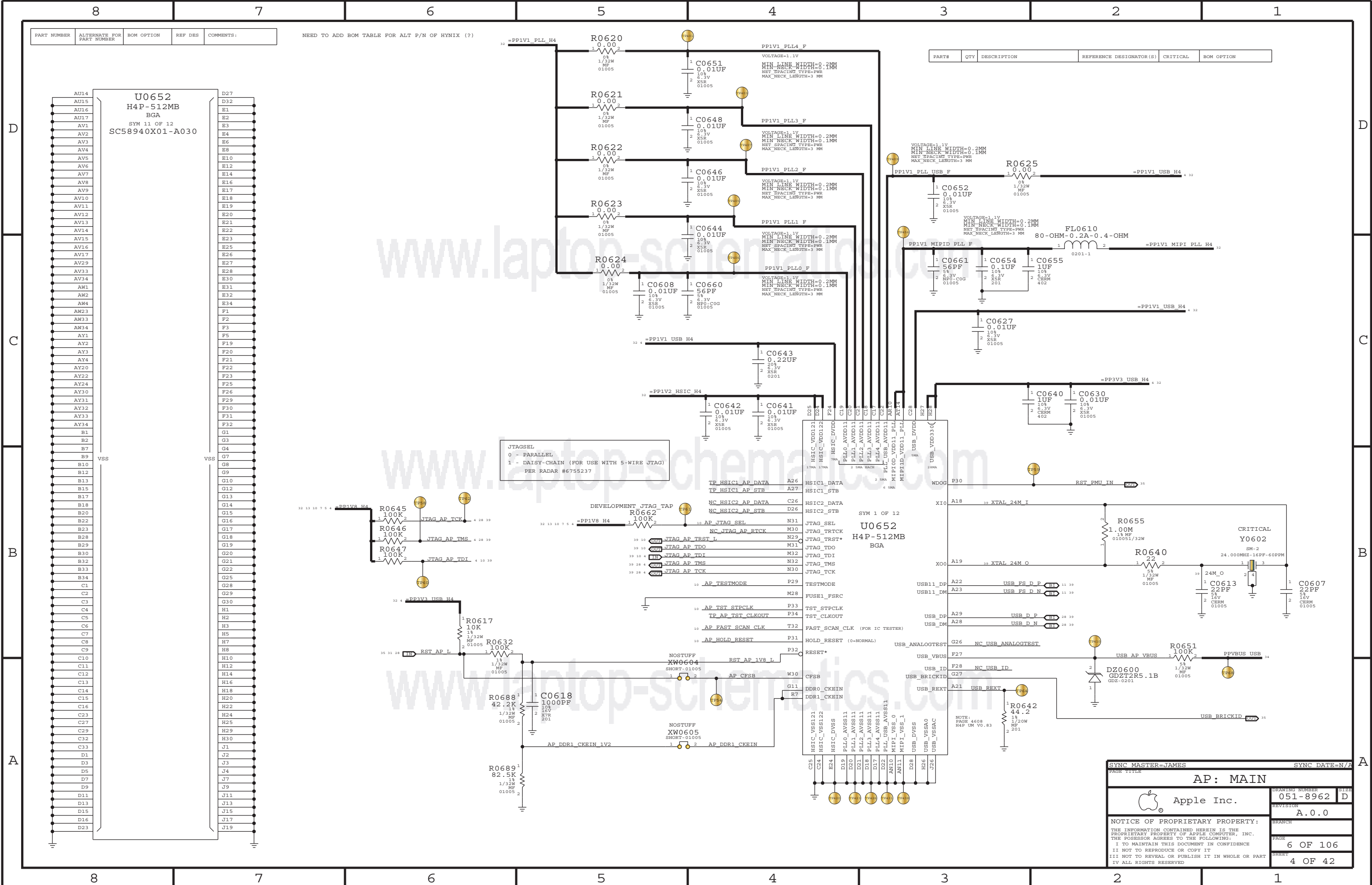
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825-7640	1	MATRIX LABEL	LBL3	CRITICAL	
825-7640	1	631- MATRIX LABEL	LBL4	CRITICAL	

SYNC MASTER=MIKE		SYNC DATE=N/A	
<b>BOM TABLE</b>			
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		REVISION	A.0.0
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		SHEET	3 OF 42

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
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NEED TO ADD BOM TABLE FOR ALT P/N OF HYNIX (?)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
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U0652  
H4P-512MB  
BGA  
SYM 11 OF 12  
SC58940X01-A030

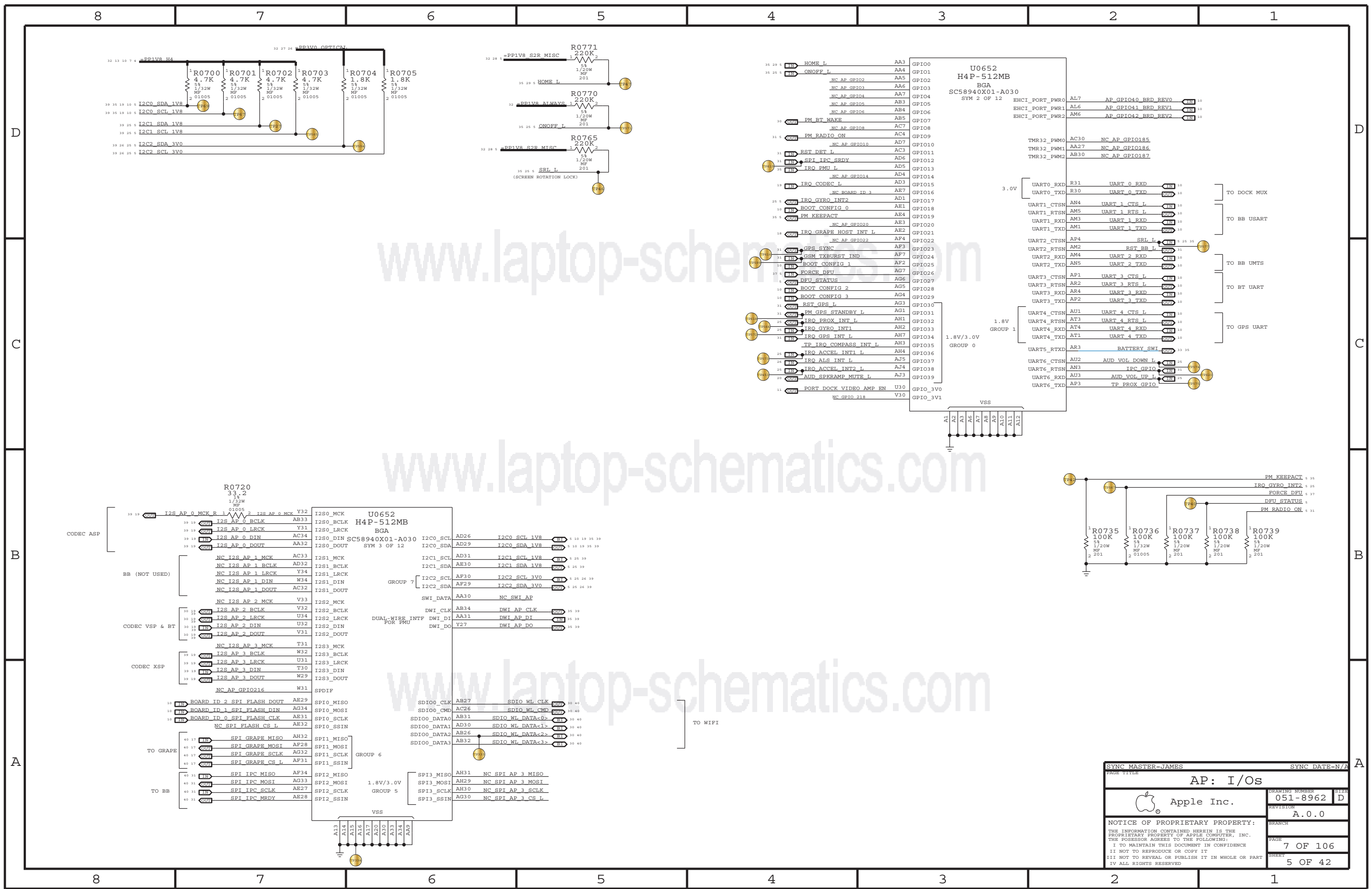
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- J19

JTAGSEL  
0 - PARALLEL  
1 - DAISY-CHAIN (FOR USE WITH 5-WIRE JTAG)  
PER RADAR #6755237

SYM 11 OF 12  
U0652  
H4P-512MB  
BGA

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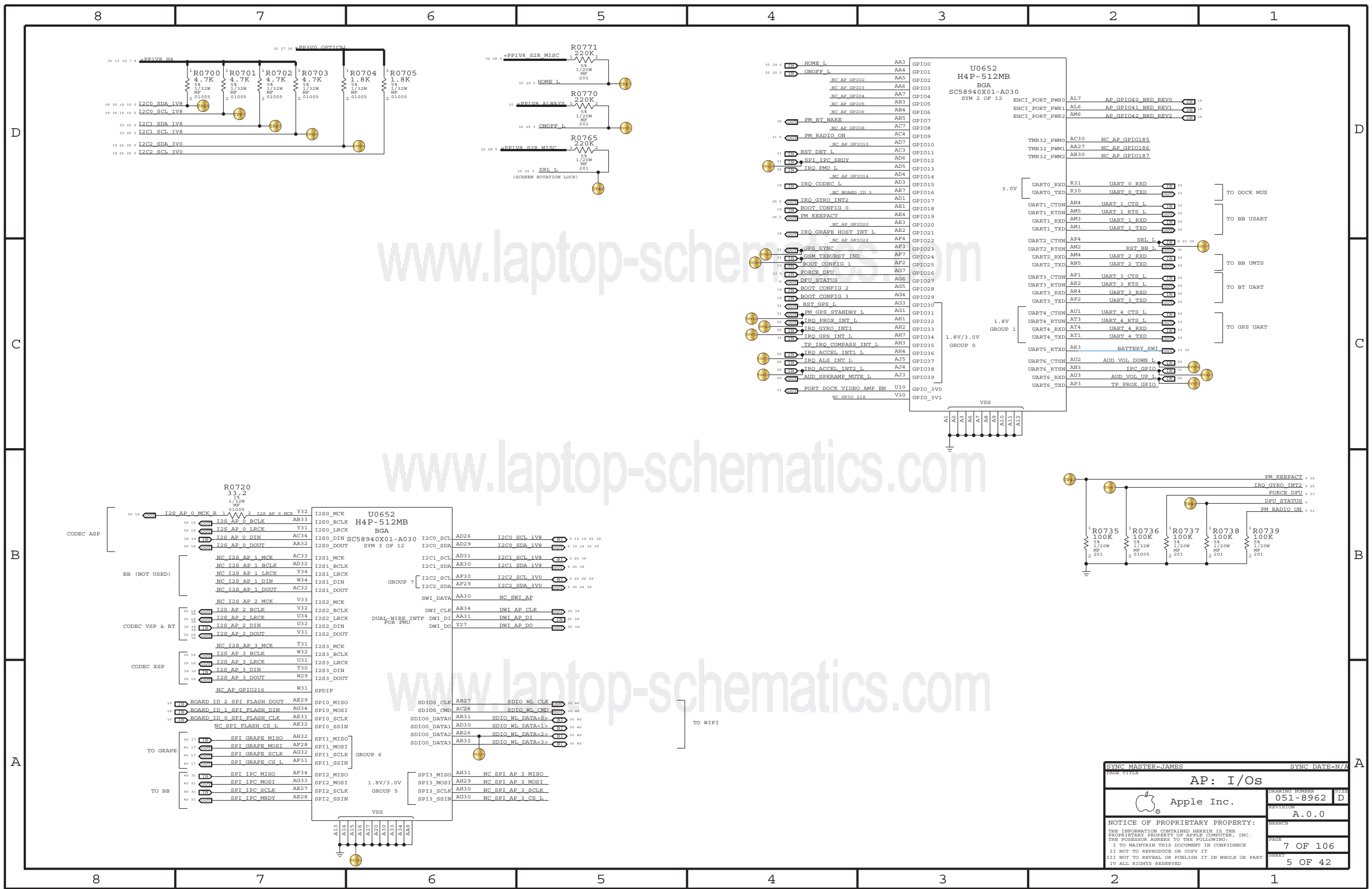


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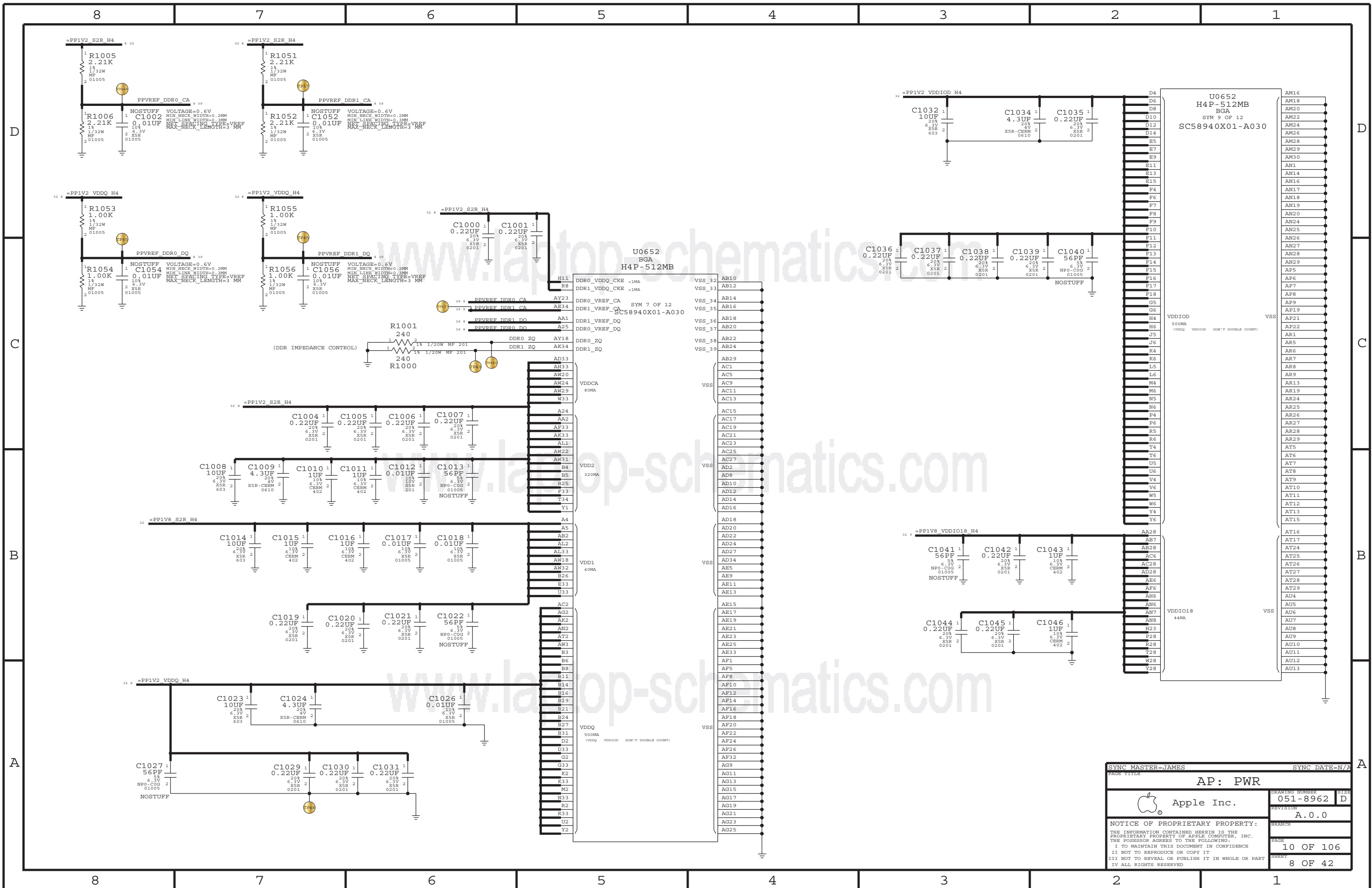
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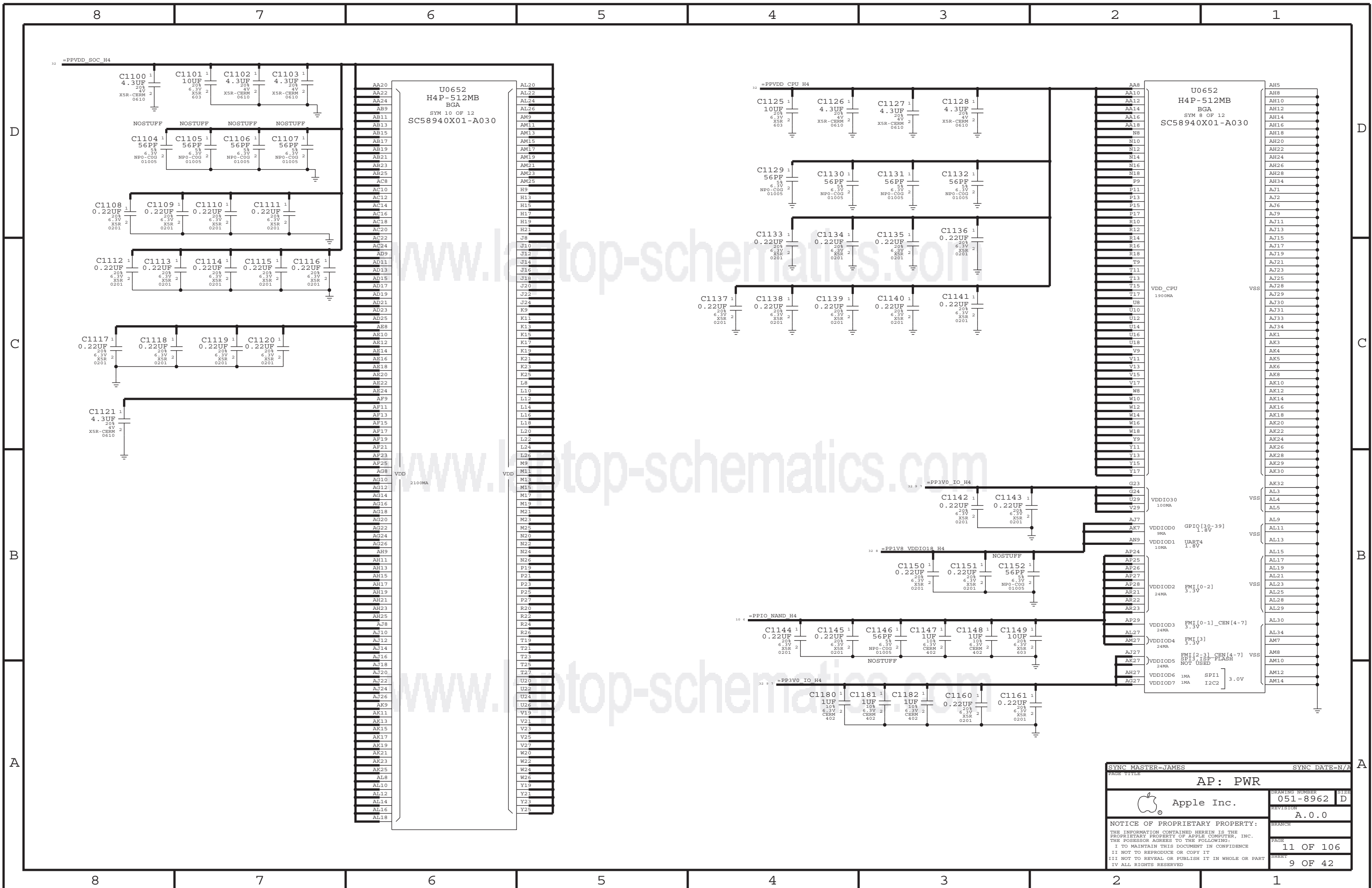




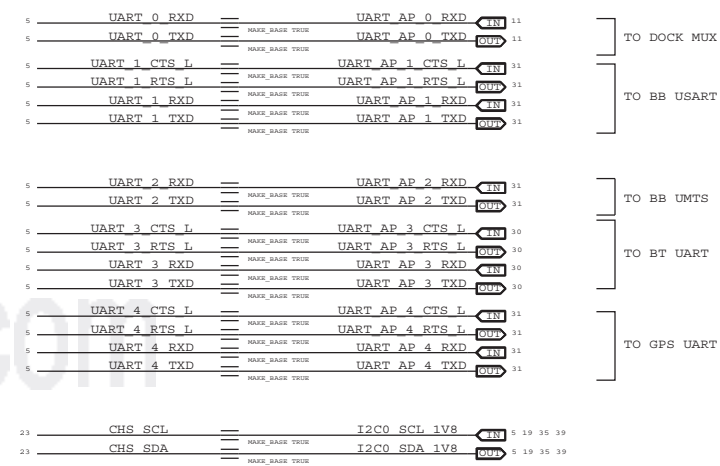
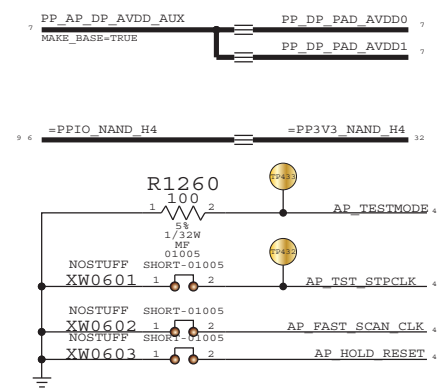
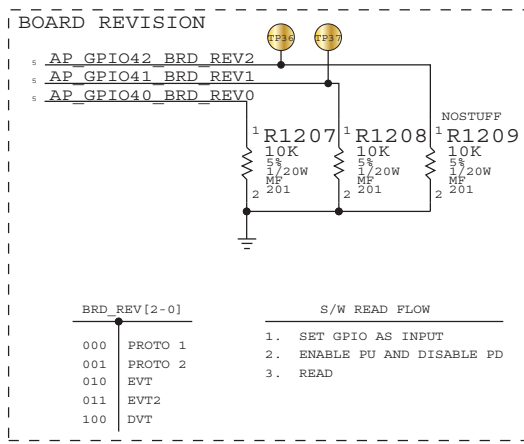
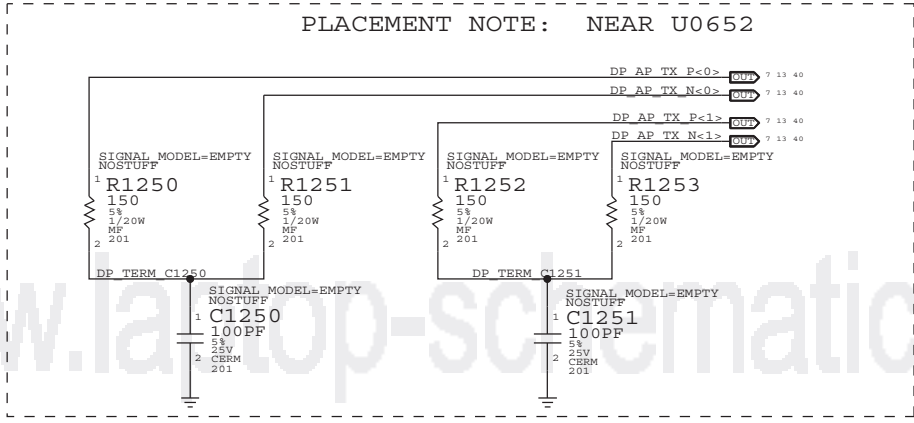
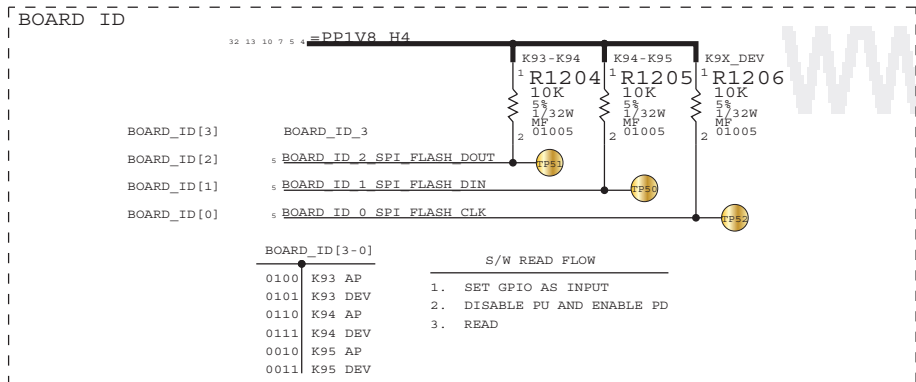
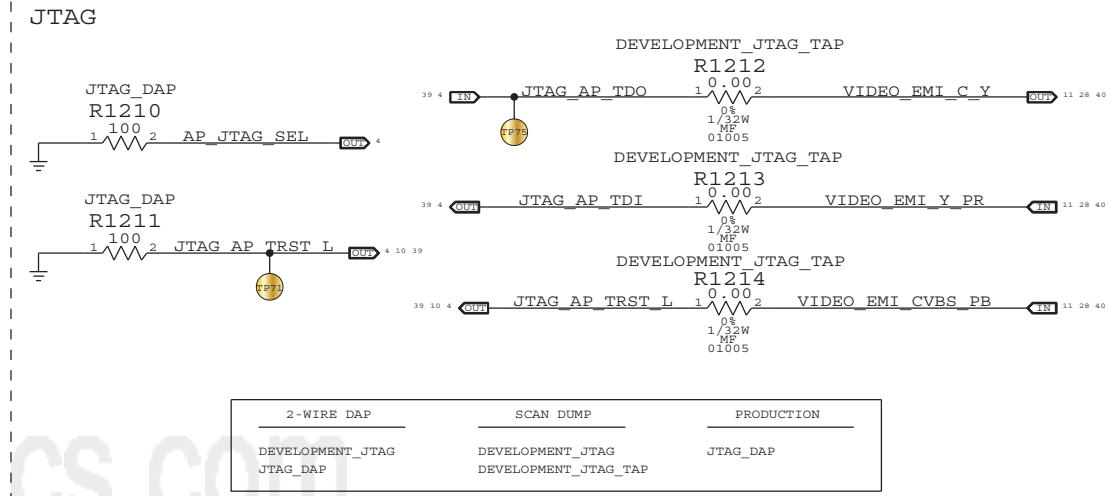
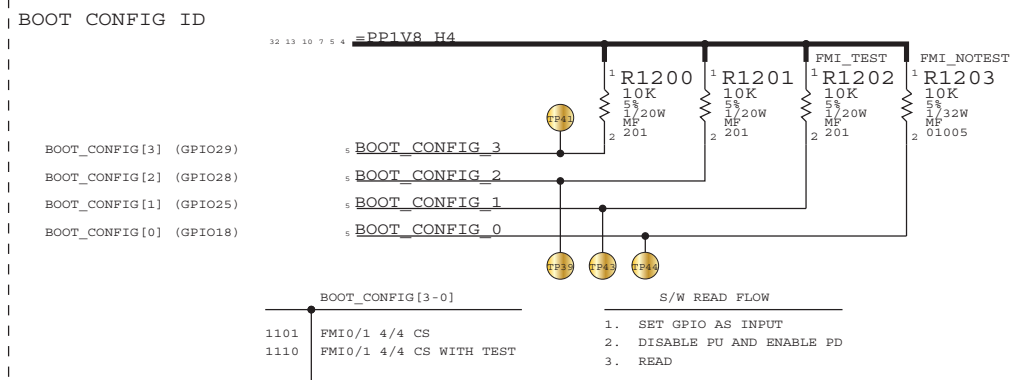


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**FOR REFERENCE**

BOOT\_CONFIG[3:0]

0000	SPI0
0001	SPI3
0010	SPI0 W/TEST
0011	SPI3 W/TEST
0100	FMIO 2CS
0101	FMIO 4CS
0110	FMIO 4CS W/TEST
0111	RESERVED
1000	FM11 2 CS
1001	FM11 4 CS
1010	FM11 4CS W/TEST
1011	RESERVED
1100	FMIO/1 2/2 CS
1101	FMIO/1 4/4 CS
1110	FMIO/1 4/4 CS W/TEST
1111	RESERVED

CURRENT SETTING ->

SYNC MASTER=JAMES SYNC DATE=N/A

**AP: MISC & ALIASES**

Apple Inc.

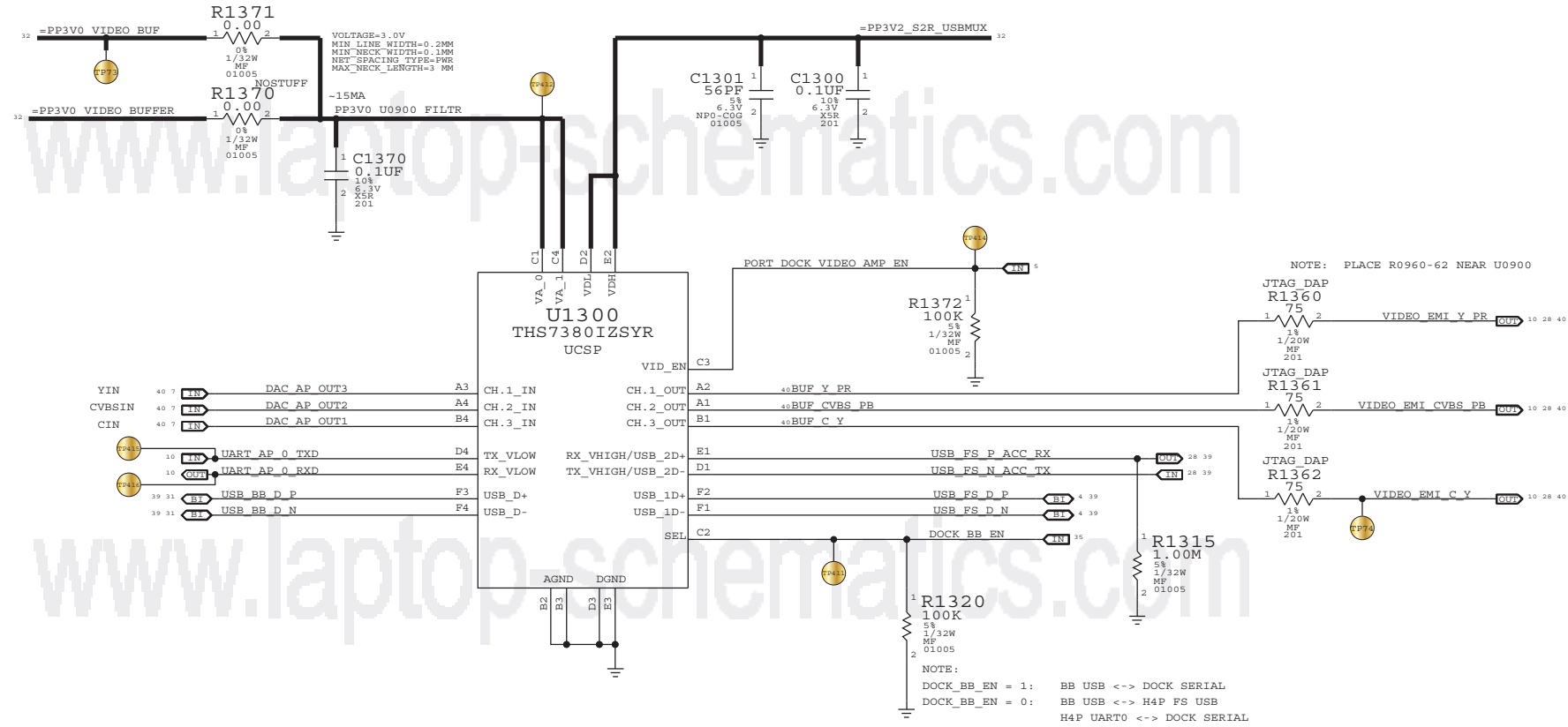
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NOTE:  
 LDO3 PROVIDES 50MA TO BOTH H4P AND U1300  
 IF THAT'S NOT ENOUGH, STUFF R1371 AND NOSTUFF R1370



SYNC MASTER=JAMES		SYNC DATE=N/A	
AP: VIDEO BUFFER, BB USB MUXES			
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### 16GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0701	1	TOSHIBA 32NM 16GB RAW	U1400	16GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0682	335S0701	16GB_PROD	U1400	SAMSUNG 35NM 16GB RAW
335S0790	335S0701	16GB_PROD	U1400	SAMSUNG 27NM 16GB RAW
335S0781	335S0701	16GB_PROD	U1400	HYNIX 26NM 16GB PPN

### 32GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0701	2	TOSHIBA 32NM 16GB RAW	U1400,U1410	32GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0682	335S0701	32GB_PROD	U1400 U1410	SAMSUNG 35NM 16GB RAW
335S0790	335S0701	32GB_PROD	U1400 U1410	SAMSUNG 27NM 16GB RAW
335S0781	335S0701	32GB_PROD	U1400 U1410	HYNIX 26NM 16GB PPN

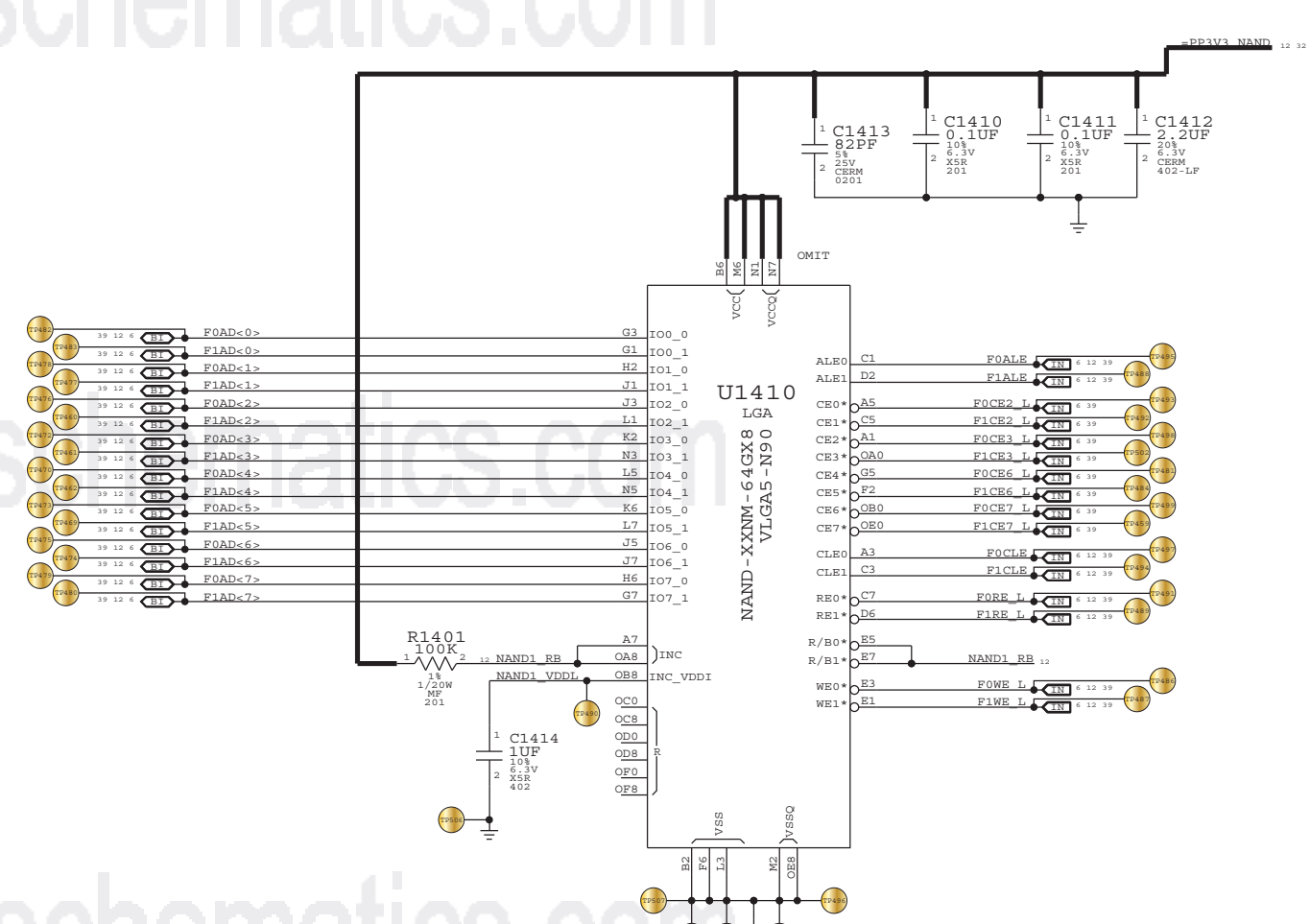
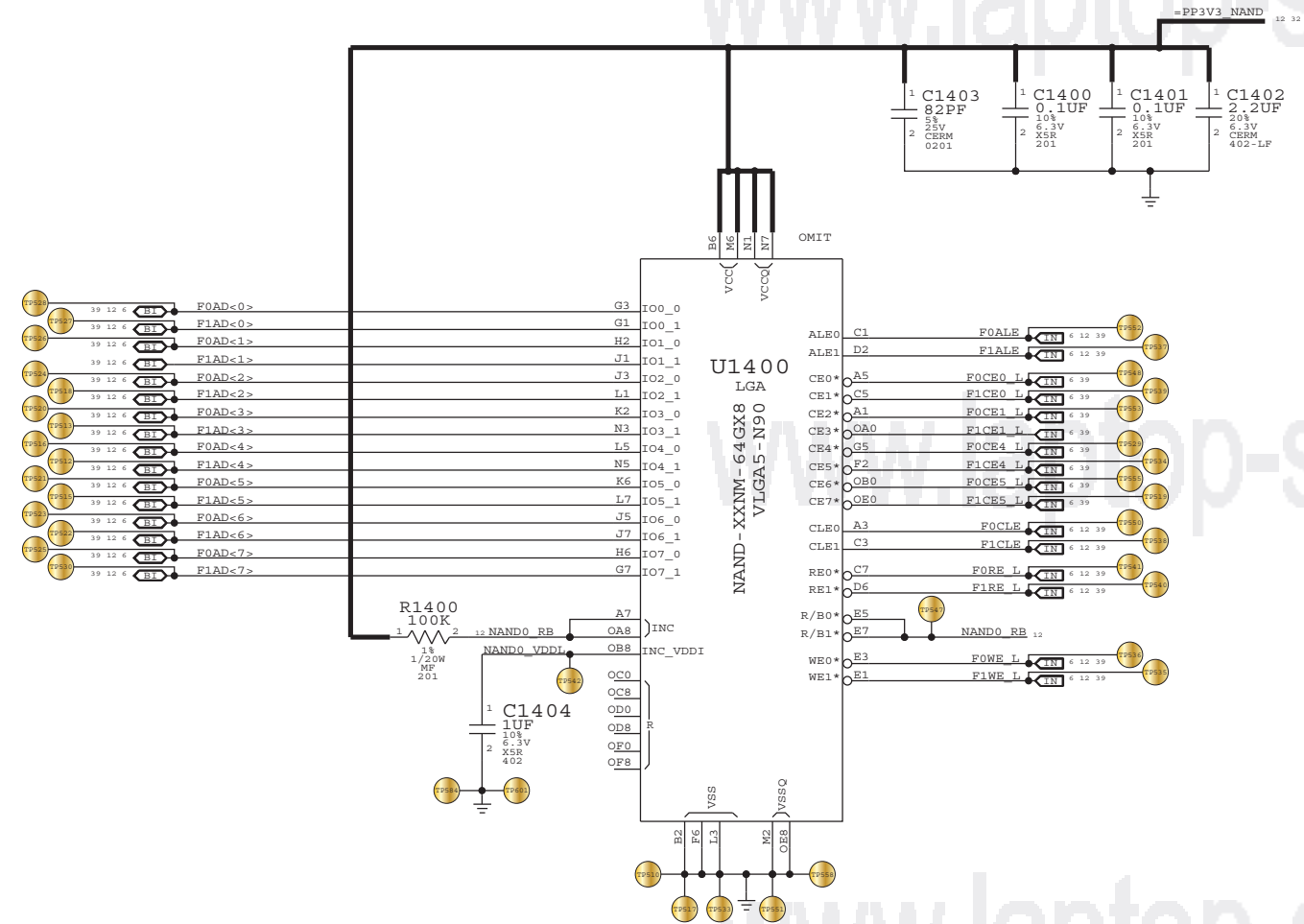
### 64GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0702	2	TOSHIBA 32NM 32GB RAW	U1400,U1410	64GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0665	335S0702	64GB_PROD	U1400 U1410	SAMSUNG 35NM 32GB RAM
335S0791	335S0702	64GB_PROD	U1400 U1410	SAMSUNG 27NM 32GB RAM
335S0722	335S0702	64GB_PROD	U1400 U1410	SANDISK 32NM 32GB RAM
335S0782	335S0702	64GB_PROD	U1400 U1410	HYNIX 26NM 32GB PPN

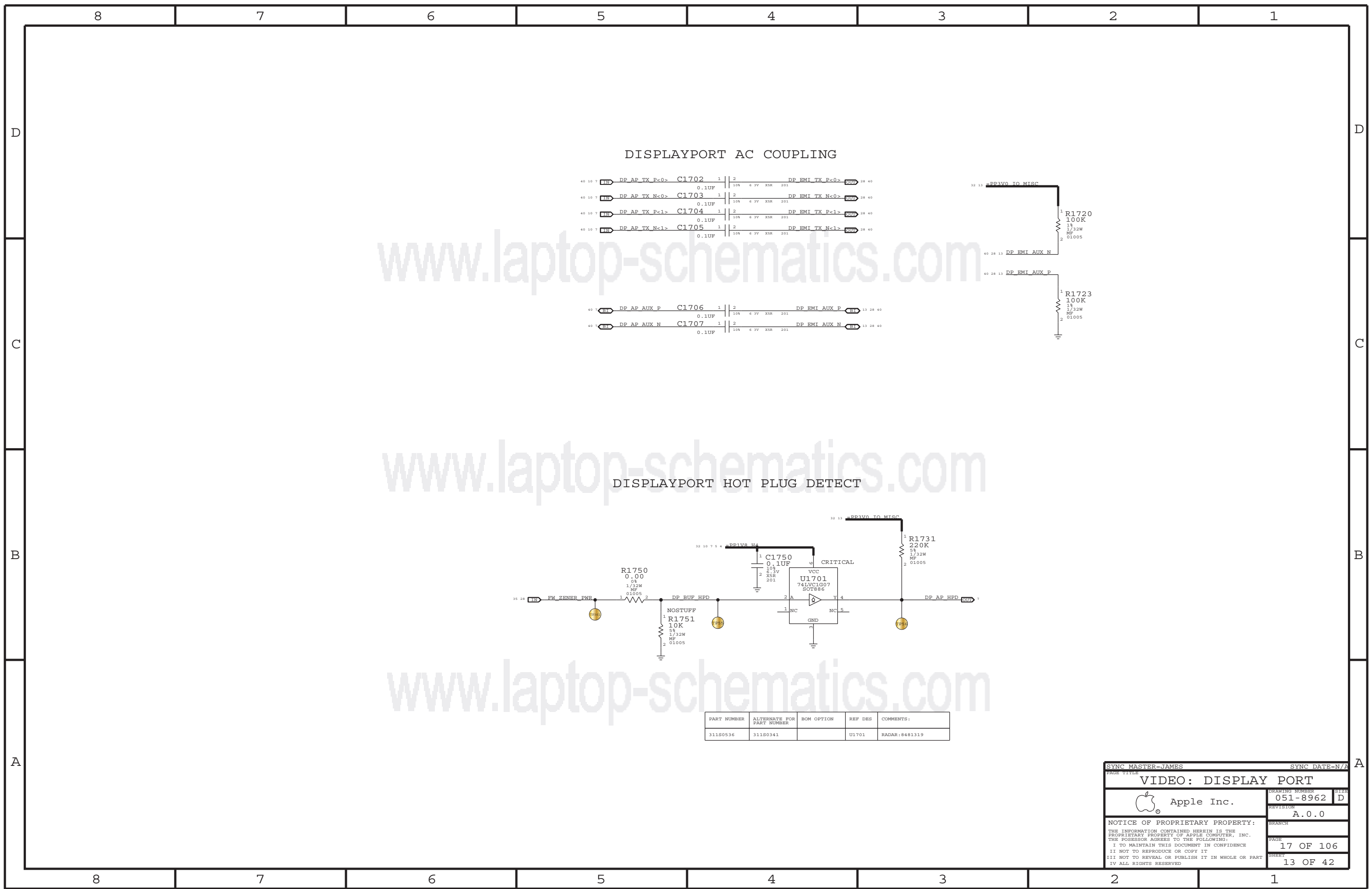
### 128GB FLASH CONFIGURATIONS

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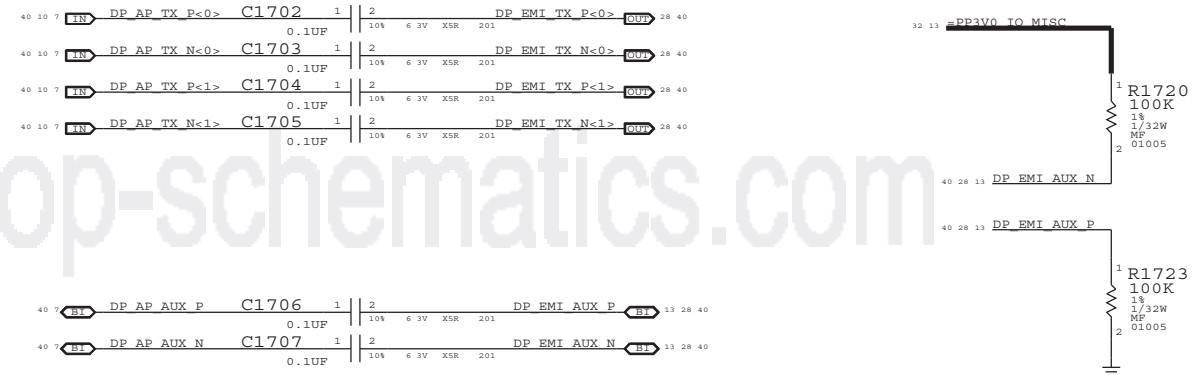


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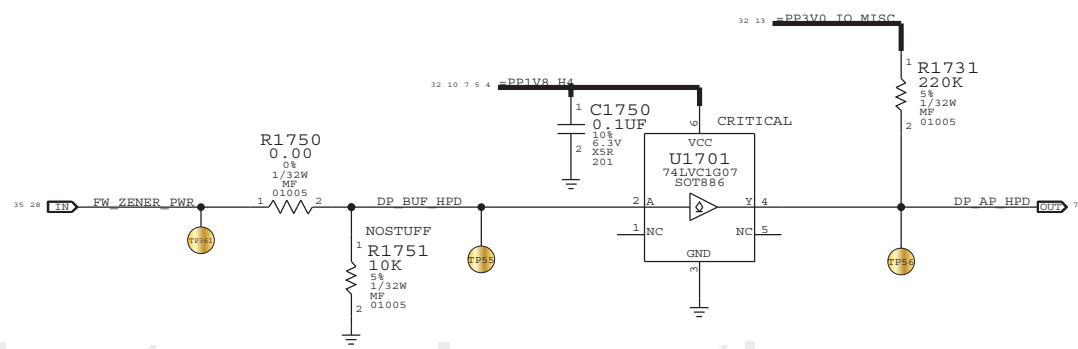
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DISPLAYPORT AC COUPLING



DISPLAYPORT HOT PLUG DETECT



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0536	311S0341		U1701	RADAR:8481319

SYNC MASTER=JAMES SYNC DATE=N/A

VIDEO: DISPLAY PORT

Apple Inc.

051-8962 D

REVISION A.0.0

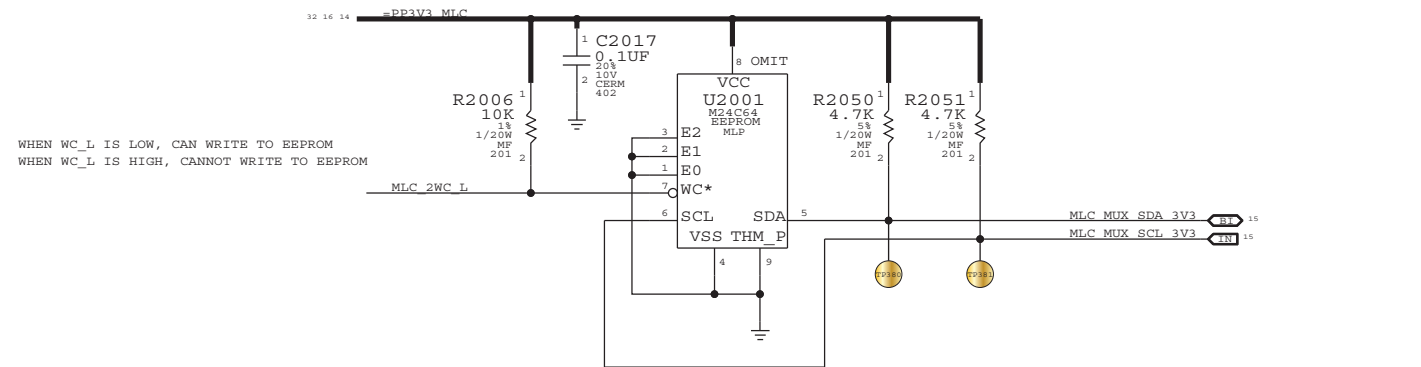
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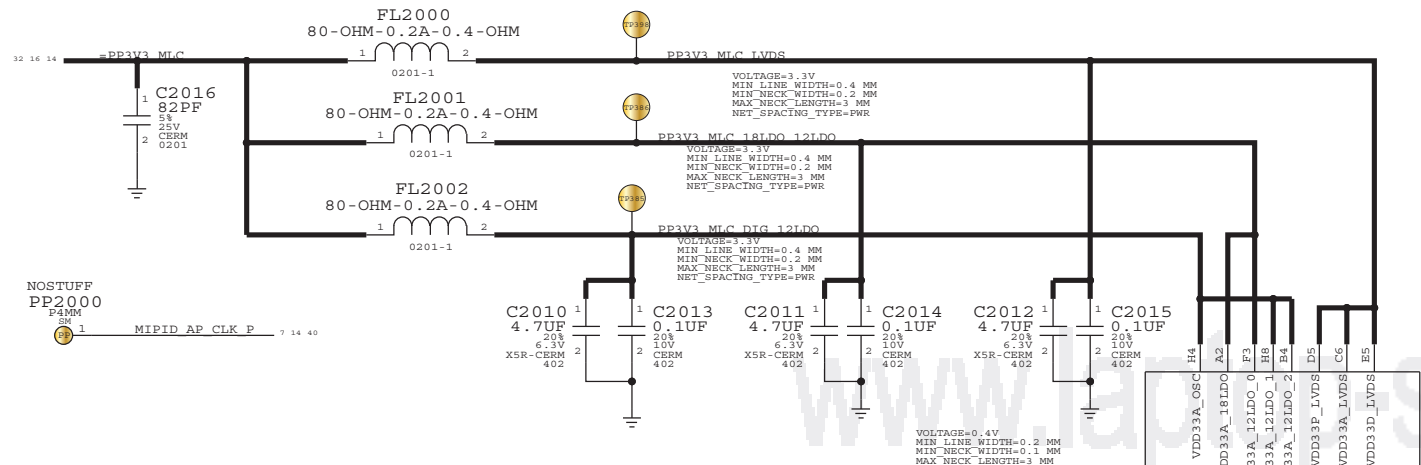
13 OF 42

MLC EEPROM:RAW APN 335S0661

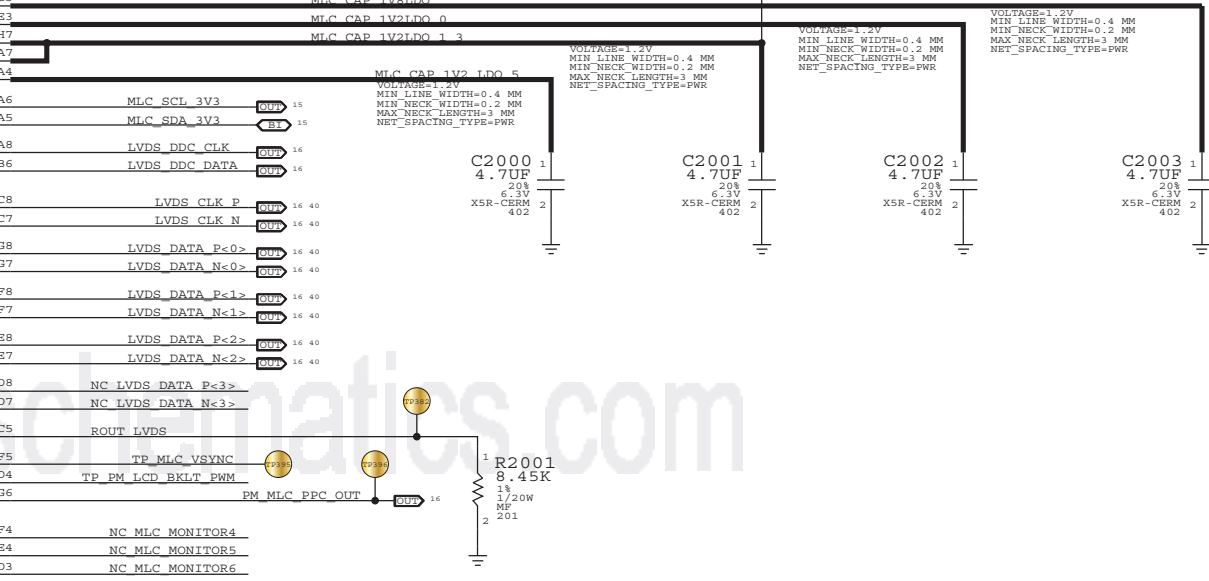
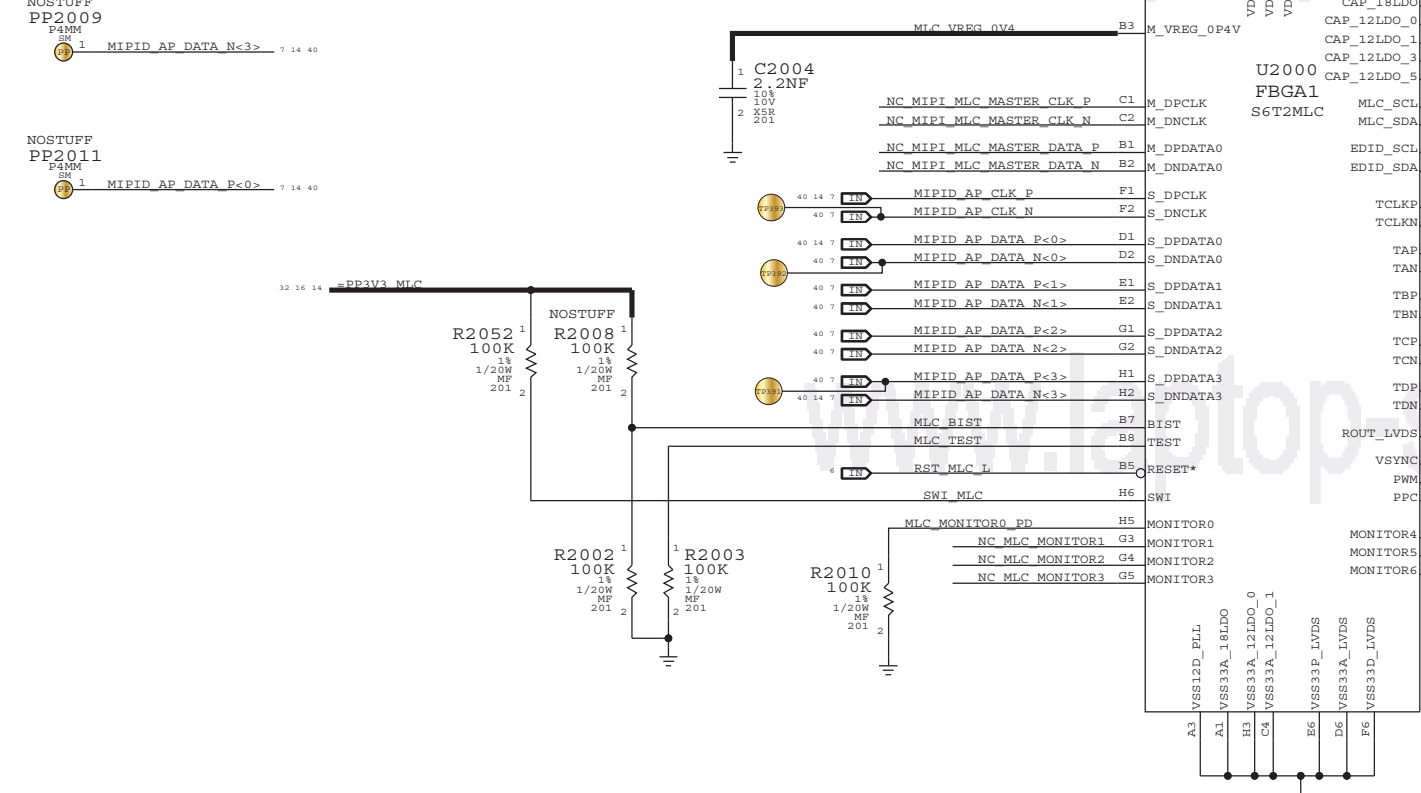
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S2799	1	MLC EEPROM 100MHZ LVDS,2MHZ SWI	U2001	CRITICAL	100MHZ_PANEL



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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
138S0652	138S0618			RADAR:8377307



SYNC MASTER=MIKE SYNC DATE=N/A

**VIDEO: MLC**

Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D

REVISION: A.0.0

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```

  14 MLC_SDA_3V3 ----- MLC_MUX_SDA_3V3 14
  14 MLC_SCL_3V3 ----- MLC_MUX_SCL_3V3 14

```

D

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C

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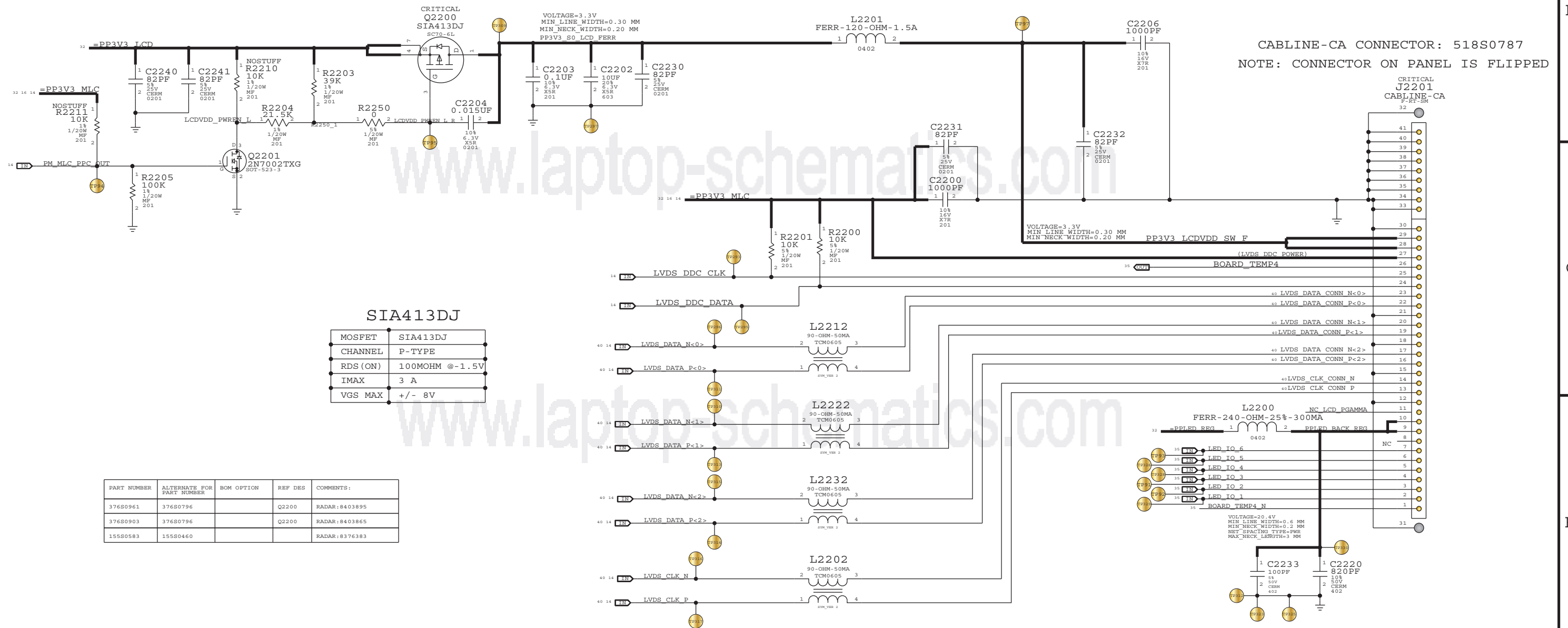
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1

SYNC MASTER=MIKE		SYNC DATE=N/A	
PAGE TITLE VIDEO: MLC ALIASES			
DRAWING NUMBER		SIZE	
051-8962		D	
REVISION			
A.0.0			
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# LVDS (LCD) CONNECTOR

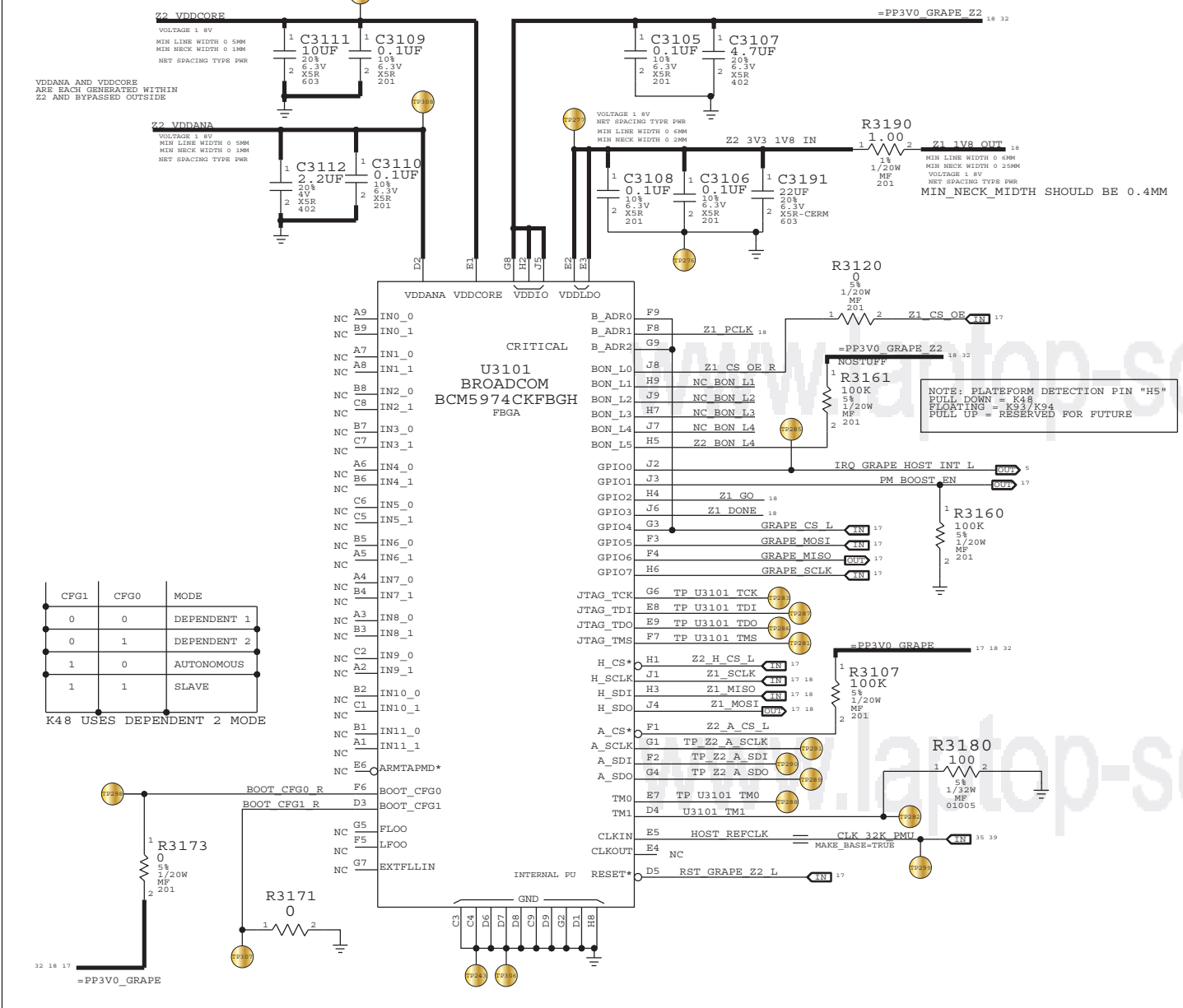


NOSTUFF RESISTORS ARE THERE TO INVESTIGATE POSSIBILITY OF REMOVING THE CHOKE

SYNC MASTER=ALEX		SYNC DATE=N/A	
PAGE TITLE <b>VIDEO: LVDS CONNECTOR</b>			
Apple Inc.		DRAWING NUMBER 051-8962	SIZE D
		REVISION A.0.0	BRANCH
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		PAGE 22 OF 106	SHEET 16 OF 42

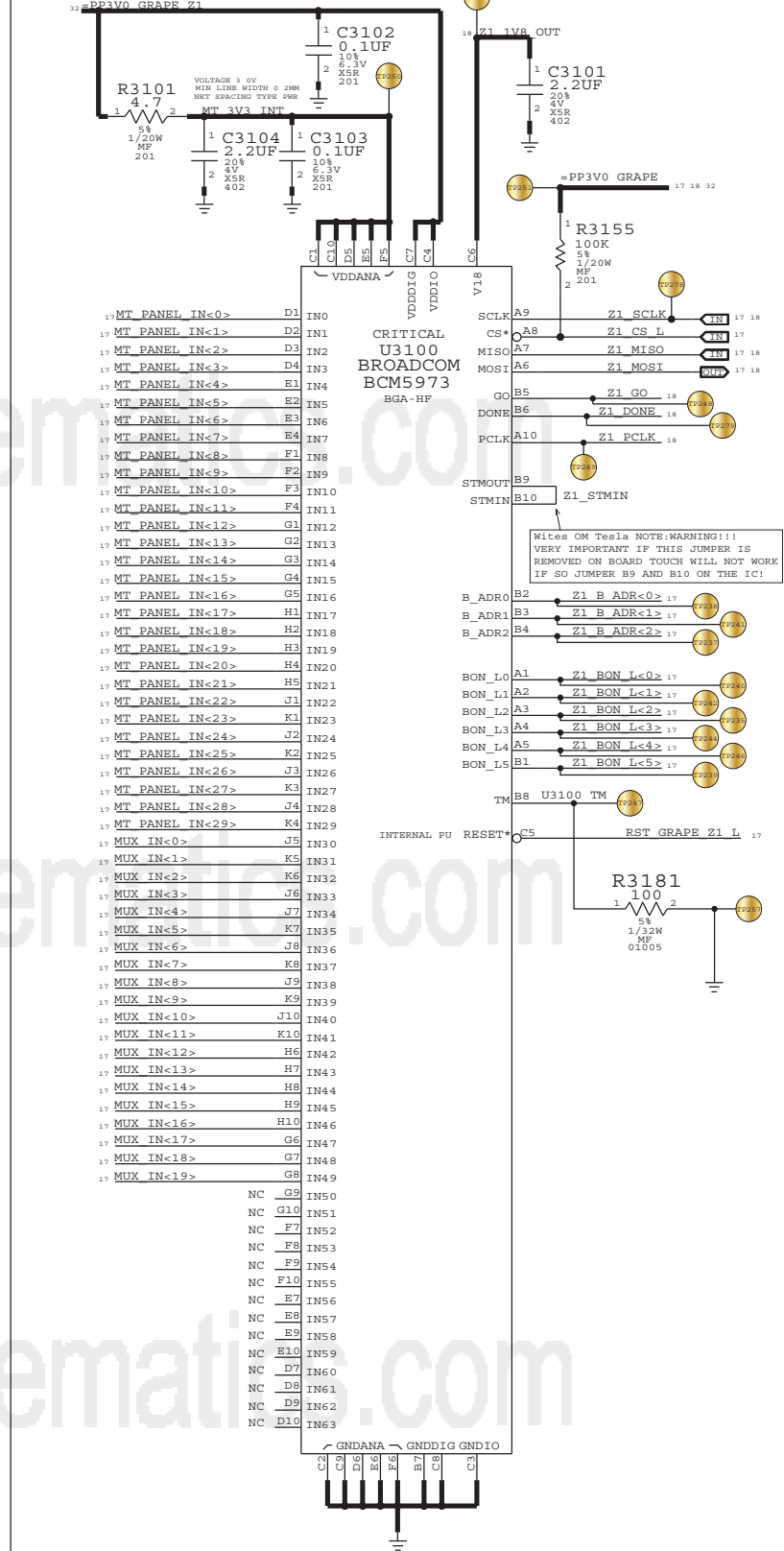


ARM9 MCU (Z2 BASED)



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0652	138S0648		C3107	RADAR: 8392120
138S0618	138S0648		C3107	BOM CONSOLIDATION

ZEPHYR 1+ ASIC



SYNC MASTER=RAMSIN SYNC DATE=N/A

GRAPE: Z1, Z2

Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D

REVISION: A.0.0

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PAGE: 31 OF 106 SHEET: 18 OF 42

# L63 AUDIO CODEC

APN:338S0940

8 7 6 5 4 3 2 1

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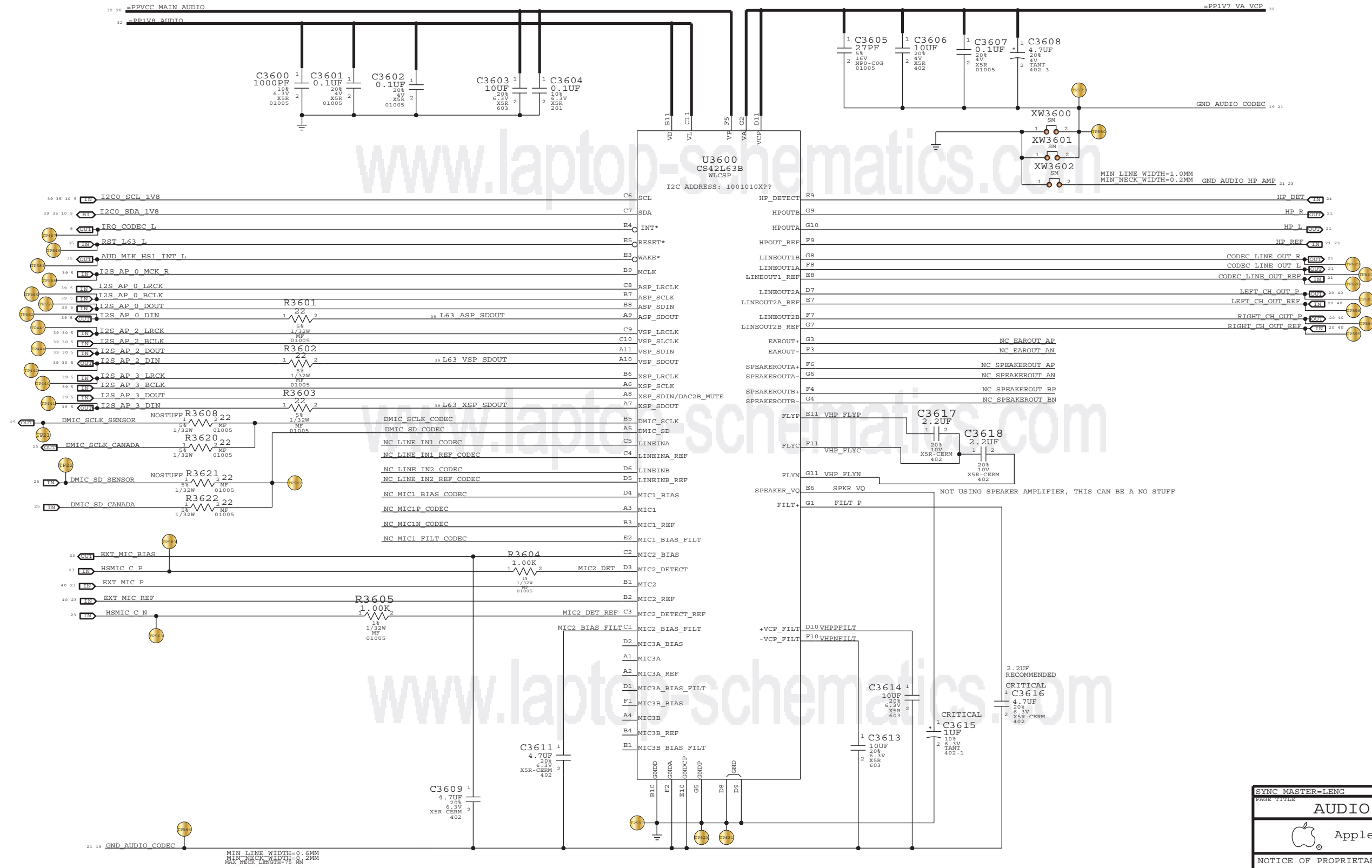
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MIN LINE WIDTH=0.6MM  
MIN NECK WIDTH=0.2MM  
MAX NECK WIDTH=0.2MM

SYNC MASTER=LENG		SYNC DATE=N/A	
PAGE TITLE			
AUDIO: L63 CODEC			
Apple Inc.		DRAWING NUMBER	051-8962
		REVISION	A.0.0
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BRANCH		PAGE	36 OF 106
SHEET		19 OF 42	

8 7 6 5 4 3 2 1

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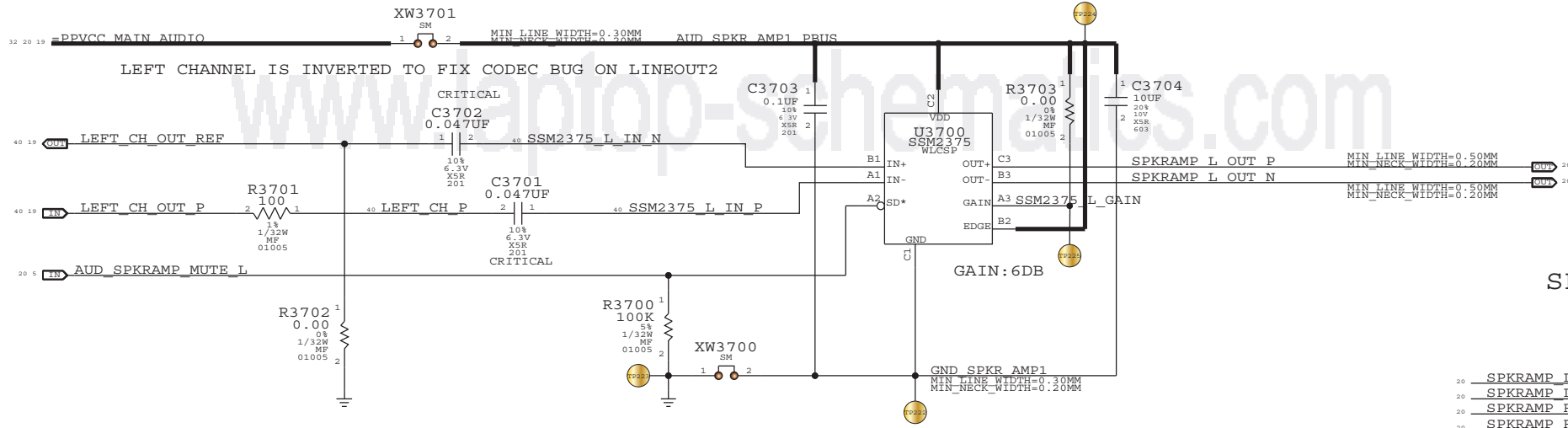
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### SPEAKER AMPLIFIER 1

APN:353S2958

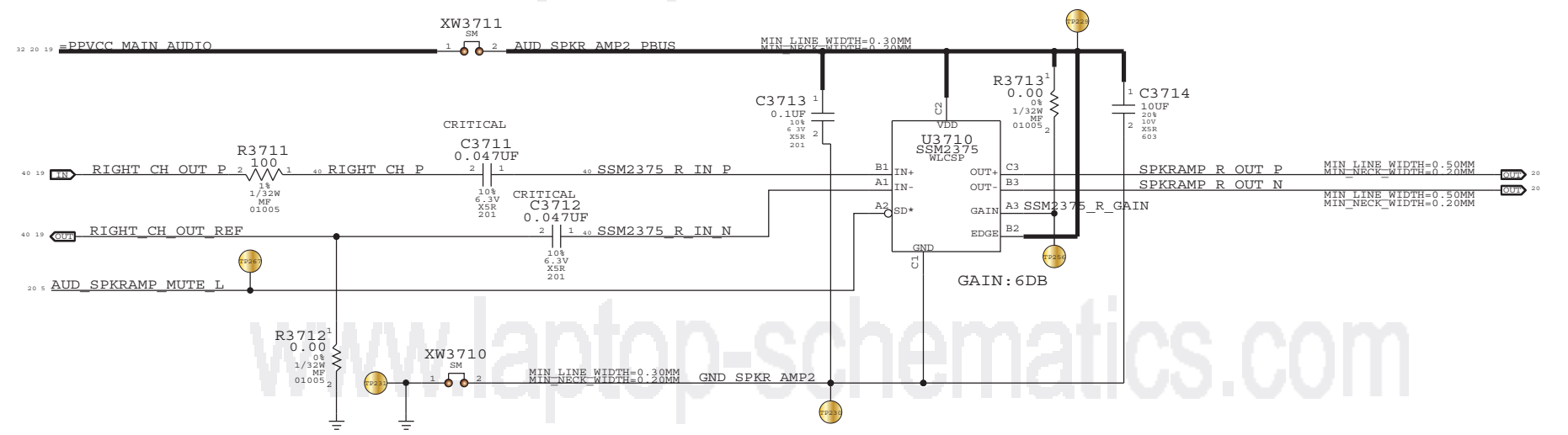
TURN ON TIME: 7.5MS  
TURN ON DELAY: 20MS  
80HZ +/- XXX%

GAIN	VDD	GND
12DB	47K	NC
9DB	NC	47K
6DB	SHORT	NC
3DB	NC	NC
0DB	NC	SHORT



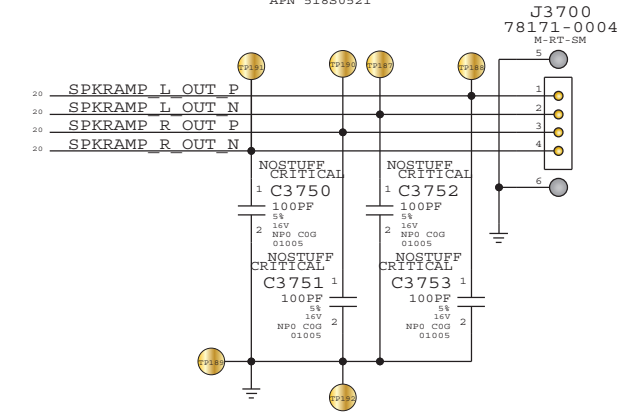
L63 LINEOUT2A IS CONNECTED TO U3700  
L63 LINEOUT2B IS CONNECTED TO U3710

### SPEAKER AMPLIFIER 2



### SPEAKER CONNECTOR

APN 518S0521



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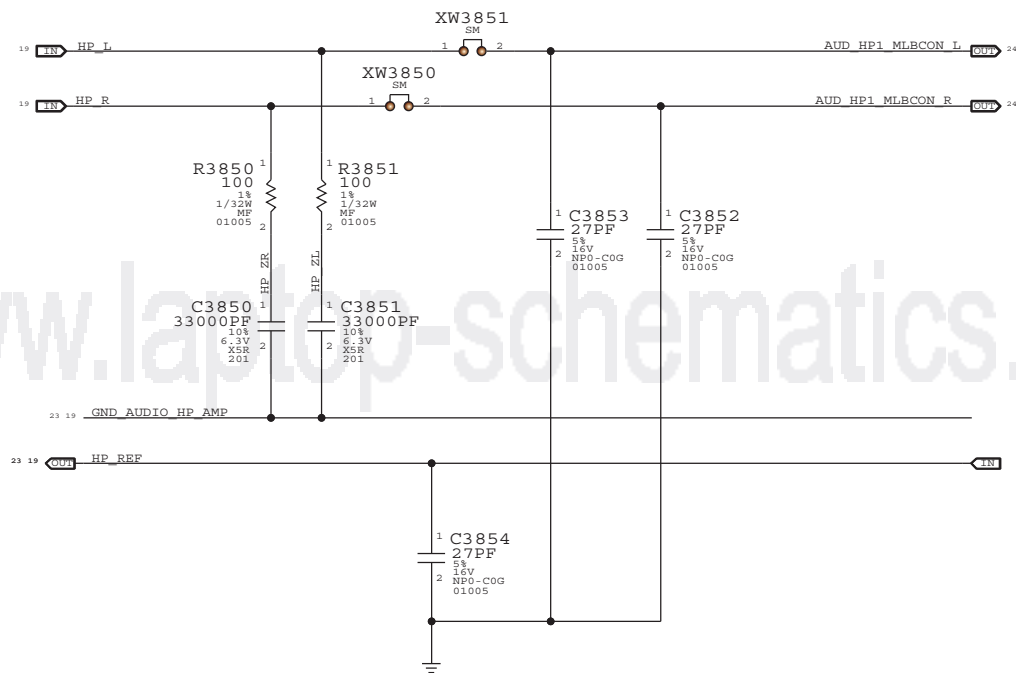
B

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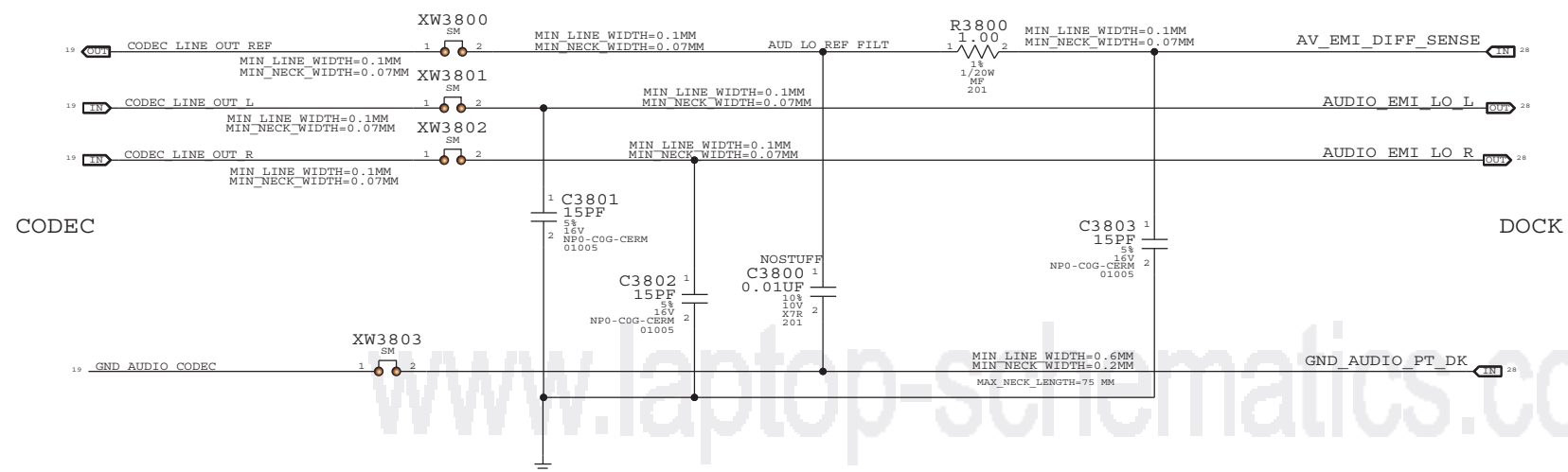
A

SYNC MASTER=LENG		SYNC DATE=N/A	
PAGE TITLE: AUDIO: SPEAKER AMP			
DRAWING NUMBER: 051-8962		SIZE: D	
REVISION: A.0.0		BRANCH:	
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PAGE: 37 OF 106		SHEET: 20 OF 42	

HEADPHONE OUTPUT ZOBEL NETWORK



DOCK LINE OUTPUT



SYNC MASTER=LENG		SYNC DATE=N/A	
PAGE TITLE <b>AUDIO: HEADPHONE OUT</b>			
DRAWING NUMBER 051-8962		SIZE D	
REVISION A.0.0		BRANCH	
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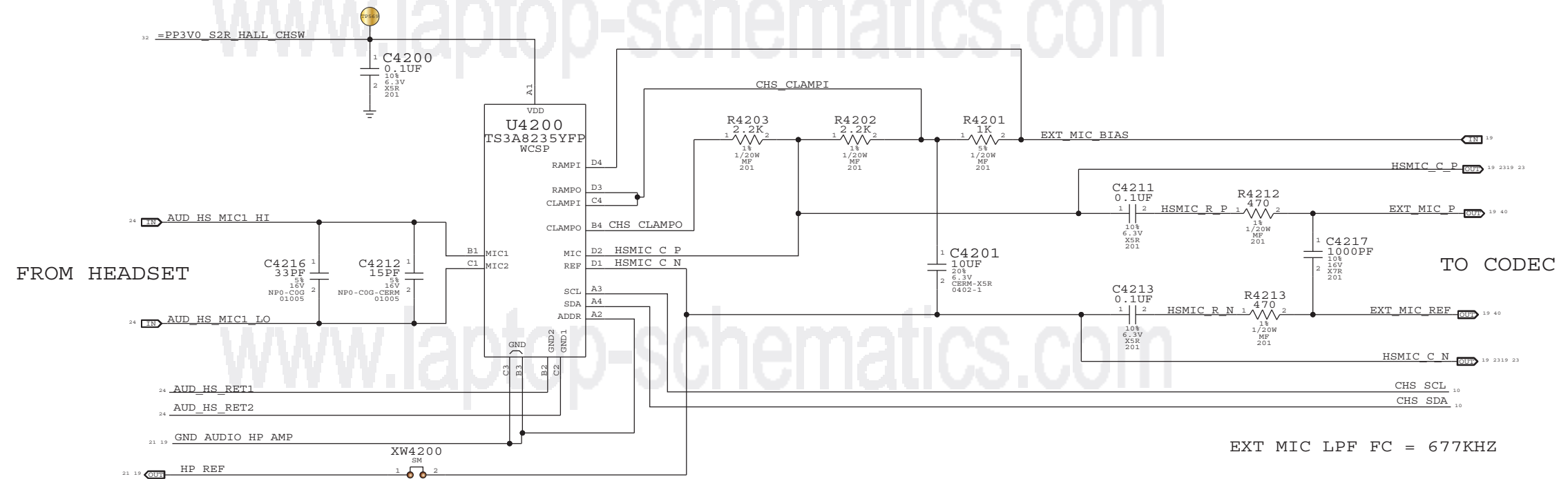
3

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1

SYNC MASTER=LENG		SYNC DATE=N/A	
PAGE TITLE <b>AUDIO: BLANK</b>			
 <b>Apple Inc.</b>	DRAWING NUMBER 051-8962	SIZE D	
	REVISION A.0.0	BRANCH	
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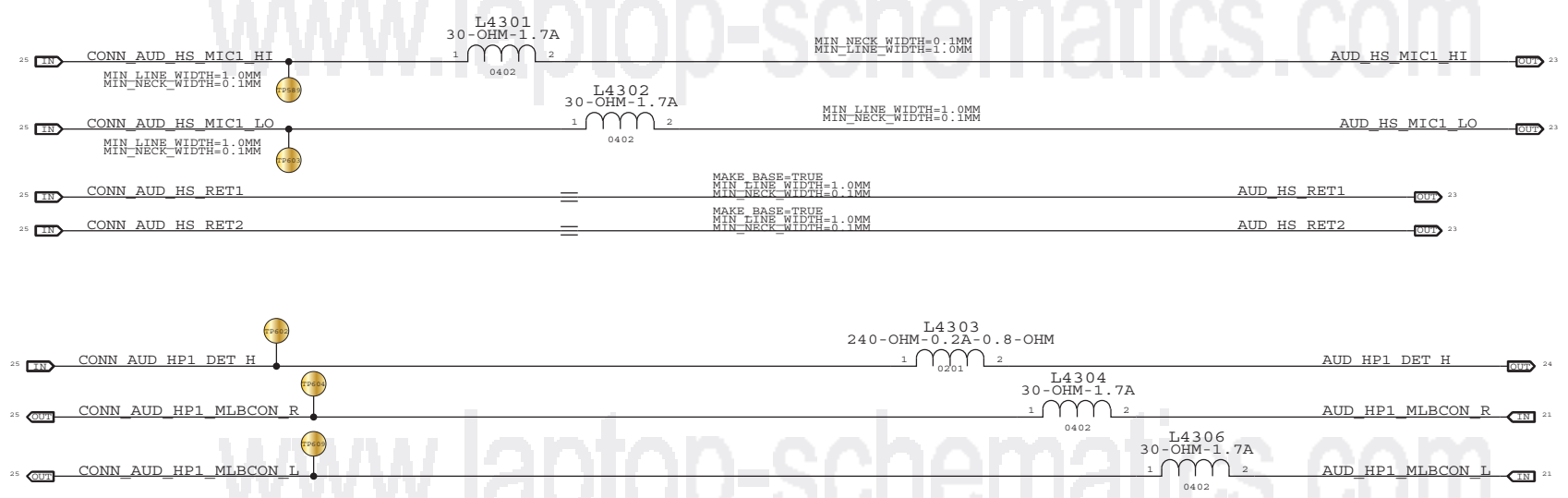
EXTERNAL (HEADSET) MIC INPUT CIRCUITRY



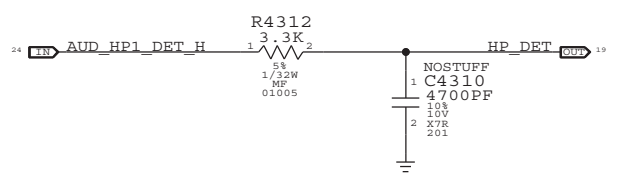
EXT MIC LPF FC = 677KHZ

SYNC MASTER=LENG		SYNC DATE=N/A	
PAGE TITLE <b>AUDIO: DETECT/MIC BIAS</b>			
Apple Inc.	DRAWING NUMBER	051-8962	SIZE D
	REVISION	A.0.0	
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		PAGE	42 OF 106
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HEADPHONE JACK CONNECTION IS ON FRONT PANEL FLEX, CSA 55/PDF 29  
 PLACE ALL COMPONENTS NEAR J5501



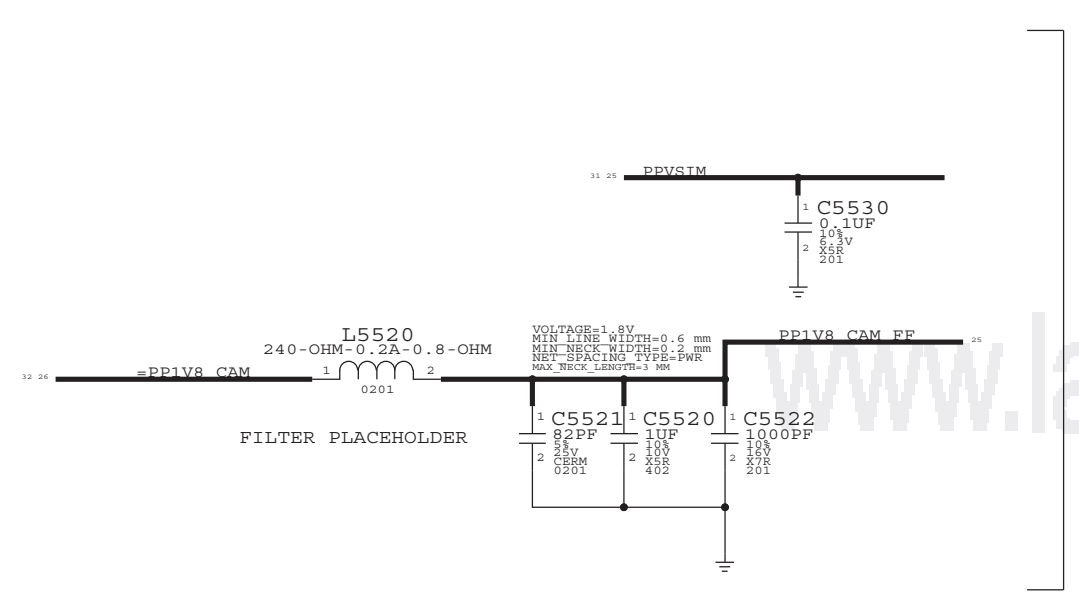
HEADSET JACK INSERTION DETECT



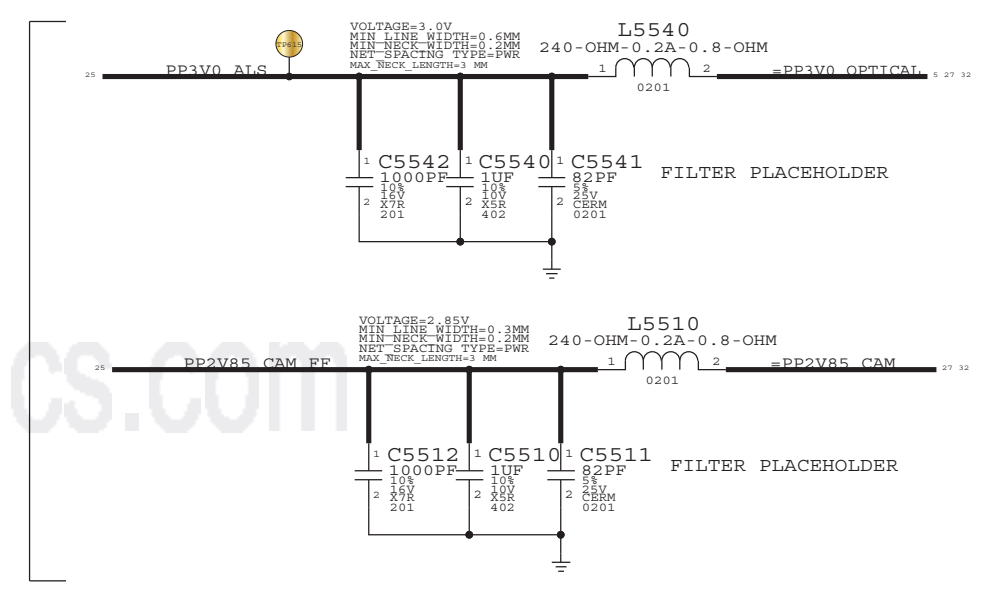
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SYNC MASTER=LENG		SYNC DATE=N/A	
PAGE TITLE <b>AUDIO: HP/MIC FILTERS</b>			
Apple Inc.	DRAWING NUMBER	051-8962	SIZE D
	REVISION	A.0.0	
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		SHEET	24 OF 42

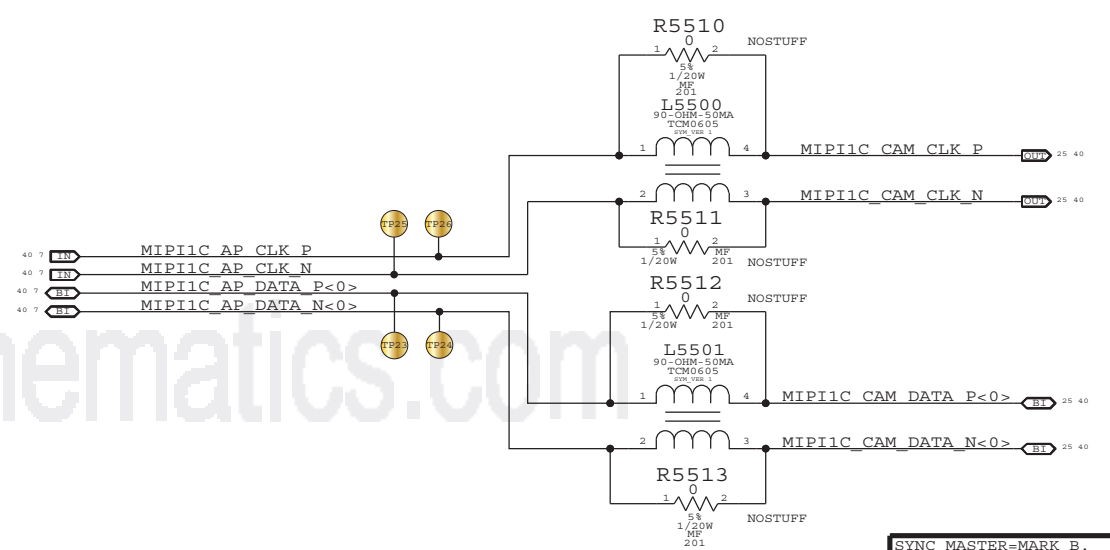
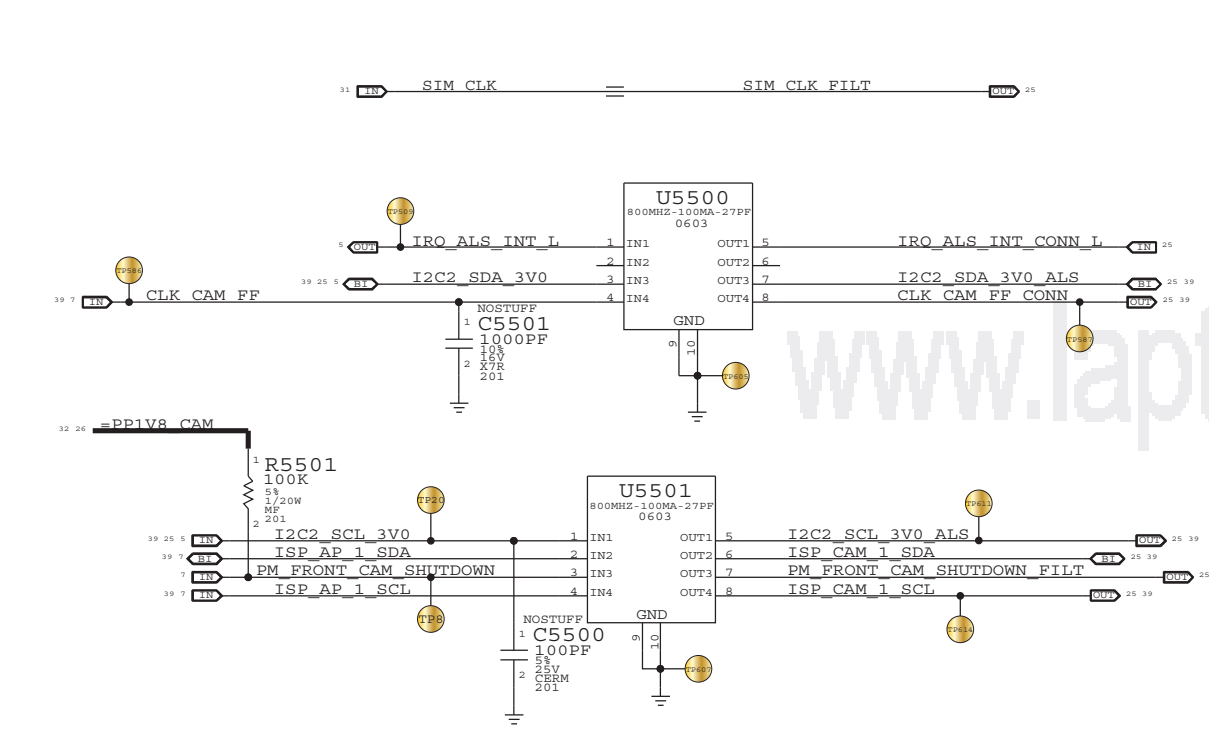




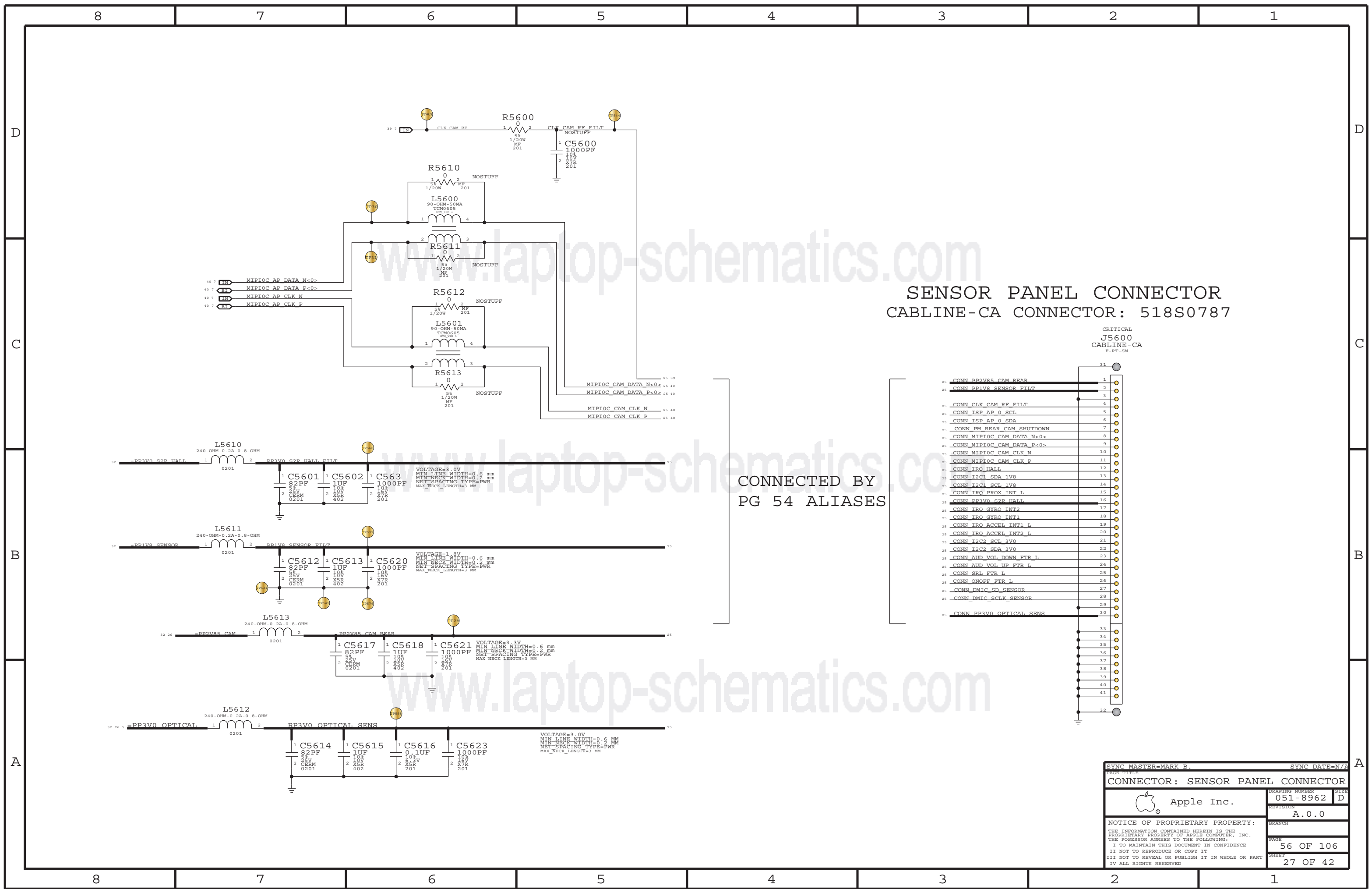
CANADA FLEX CONN ON PG 54



CANADA FLEX SIGNAL FILTERS



PAGE TITLE		SYNC DATE=N/A	
CONNECTOR: CANADA FLEX FILTERS			
Apple Inc.	DRAWING NUMBER	051-8962	SIZE
	REVISION	A.0.0	
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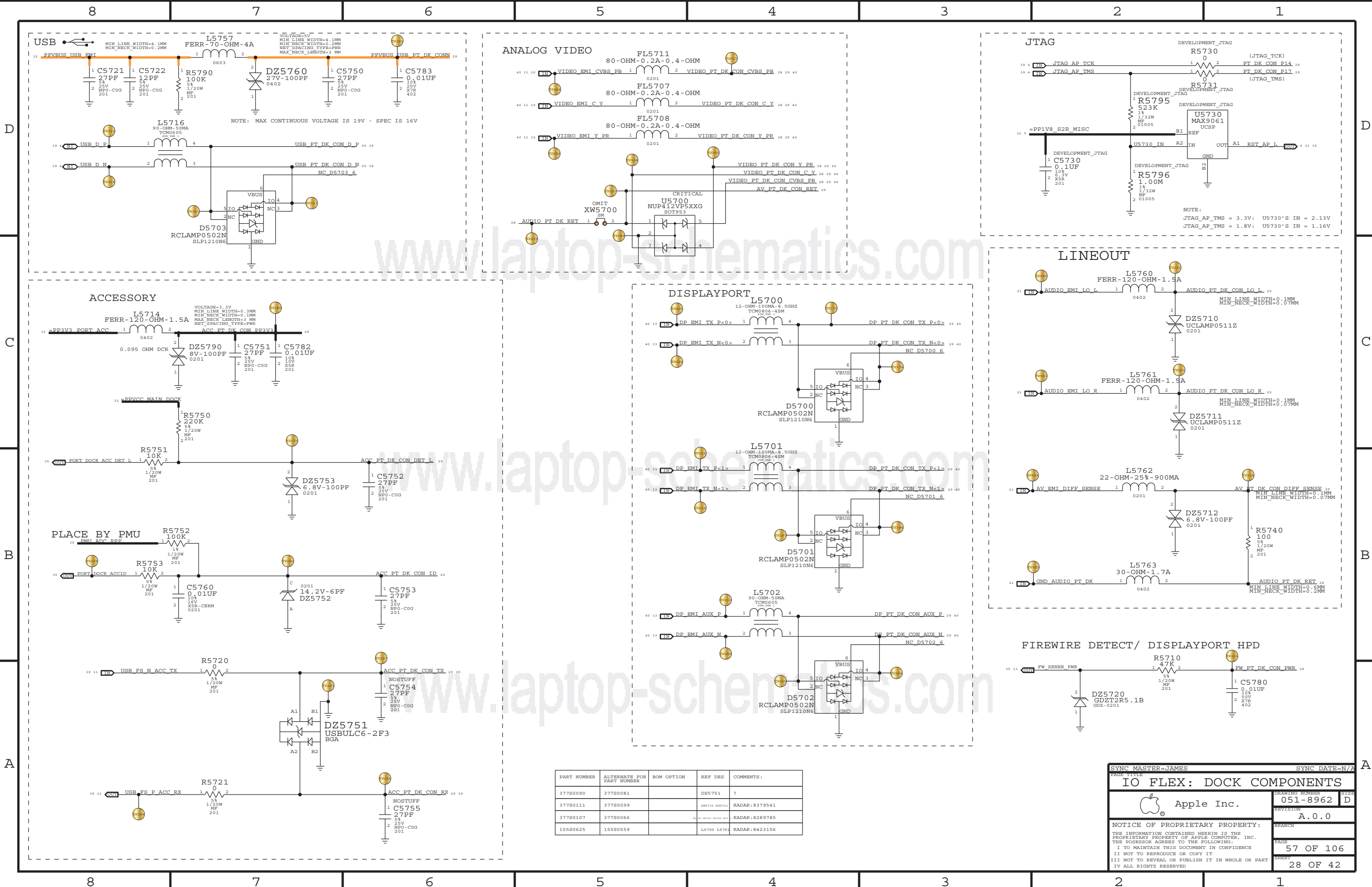
**SENSOR PANEL CONNECTOR**  
**CABLINA-CA CONNECTOR: 518S0787**

CRITICAL  
**J5600**  
 CABLINE-CA  
 F-RT-SM

CONNECTED BY  
 PG 54 ALIASES

1	CONN_PP2V85_CAM_REAR
2	CONN_PP1V8_SENSOR_FILT
3	
4	CONN_CLK_CAM_RF_FILT
5	CONN_ISP_AP_0_SCL
6	CONN_ISP_AP_0_SDA
7	CONN_PM_REAR_CAM_SHUTDOWN
8	CONN_MIPIOC_CAM_DATA_N<0>
9	CONN_MIPIOC_CAM_DATA_P<0>
10	CONN_MIPIOC_CAM_CLK_N
11	CONN_MIPIOC_CAM_CLK_P
12	CONN_IRO_HALL
13	CONN_I2C1_SDA_1V8
14	CONN_I2C1_SCL_1V8
15	CONN_IRO_PROX_INT_L
16	CONN_PP3V0_S2R_HALL
17	CONN_IRO_GYRO_INT2
18	CONN_IRO_GYRO_INT1
19	CONN_IRO_ACCEL_INT1_L
20	CONN_IRO_ACCEL_INT2_L
21	CONN_I2C2_SCL_3V0
22	CONN_I2C2_SDA_3V0
23	CONN_AUD_VOL_DOWN_FTR_L
24	CONN_AUD_VOL_UP_FTR_L
25	CONN_SRL_FTR_L
26	CONN_ONOFF_FTR_L
27	CONN_DMIC_SD_SENSOR
28	CONN_DMIC_SCLK_SENSOR
29	
30	CONN_PP3V0_OPTICAL_SENS
31	
32	
33	
34	
35	
36	
37	
38	
39	
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41	
42	

PAGE TITLE		SYNC DATE=N/A	
<b>CONNECTOR: SENSOR PANEL CONNECTOR</b>			
Apple Inc.	DRAWING NUMBER	051-8962	SIZE
	REVISION	A.0.0	D
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
377S0090	377S0081		DZ5751	?
377S0111	377S0099		08Y10 08Y11	RADAR:8379541
377S0107	377S0066		08 08 08Y10 08Y11	RADAR:8289785
155S0625	155S0559		L5700 L5702	RADAR:8423156

SYNC MASTER=JAMES SYNC DATE=N/A

**IO FLEX: DOCK COMPONENTS**

Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D

REVISION: A.0.0

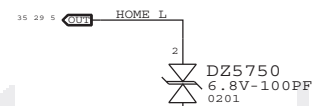
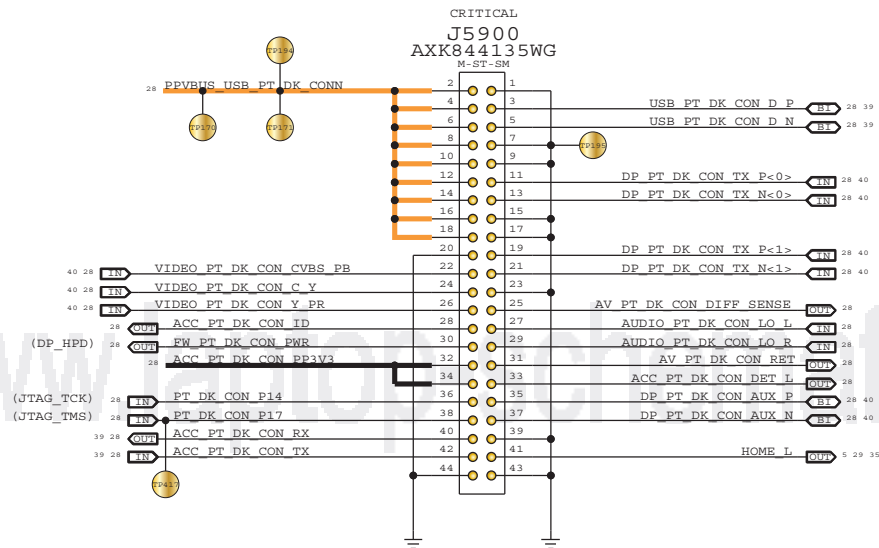
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DOCK CONNECTOR

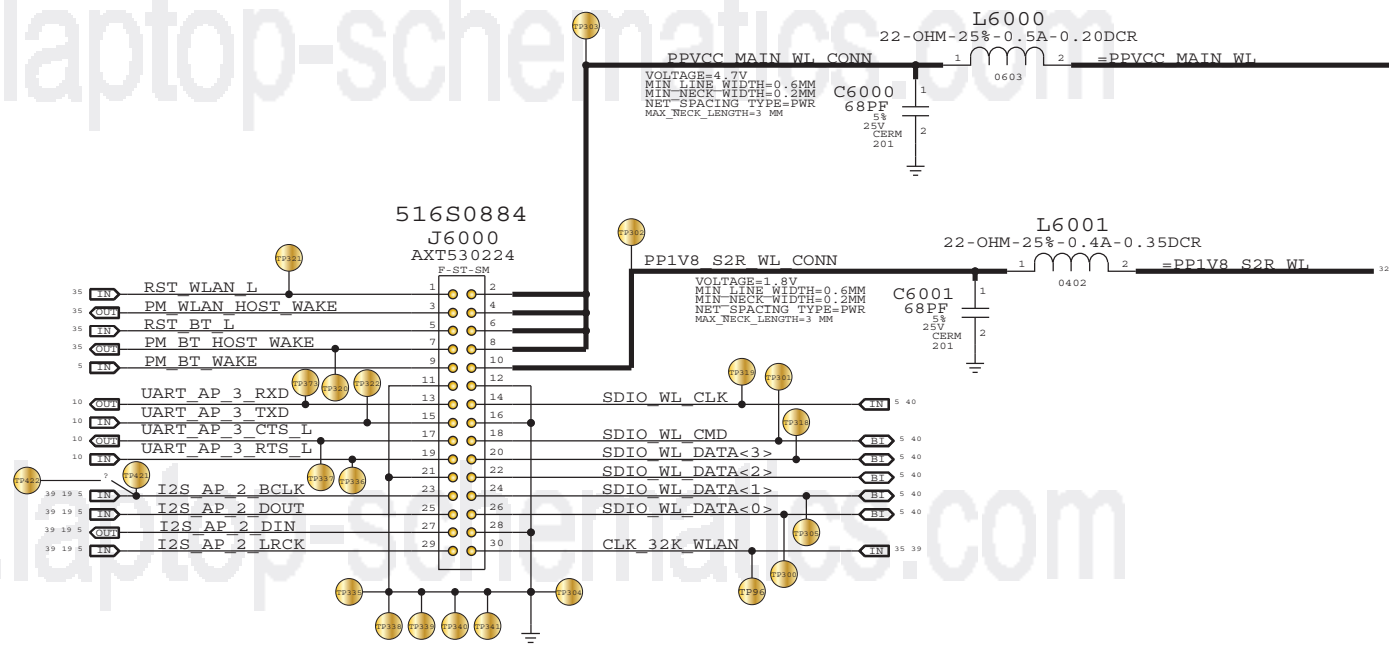
PN 516S0817 (PLUG - MALE)



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SYNC MASTER=JAMES		SYNC DATE=N/A	
PAGE TITLE <b>IO FELX: B2B Connector</b>			
DRAWING NUMBER 051-8962		SIZE D	
REVISION A.0.0		BRANCH	
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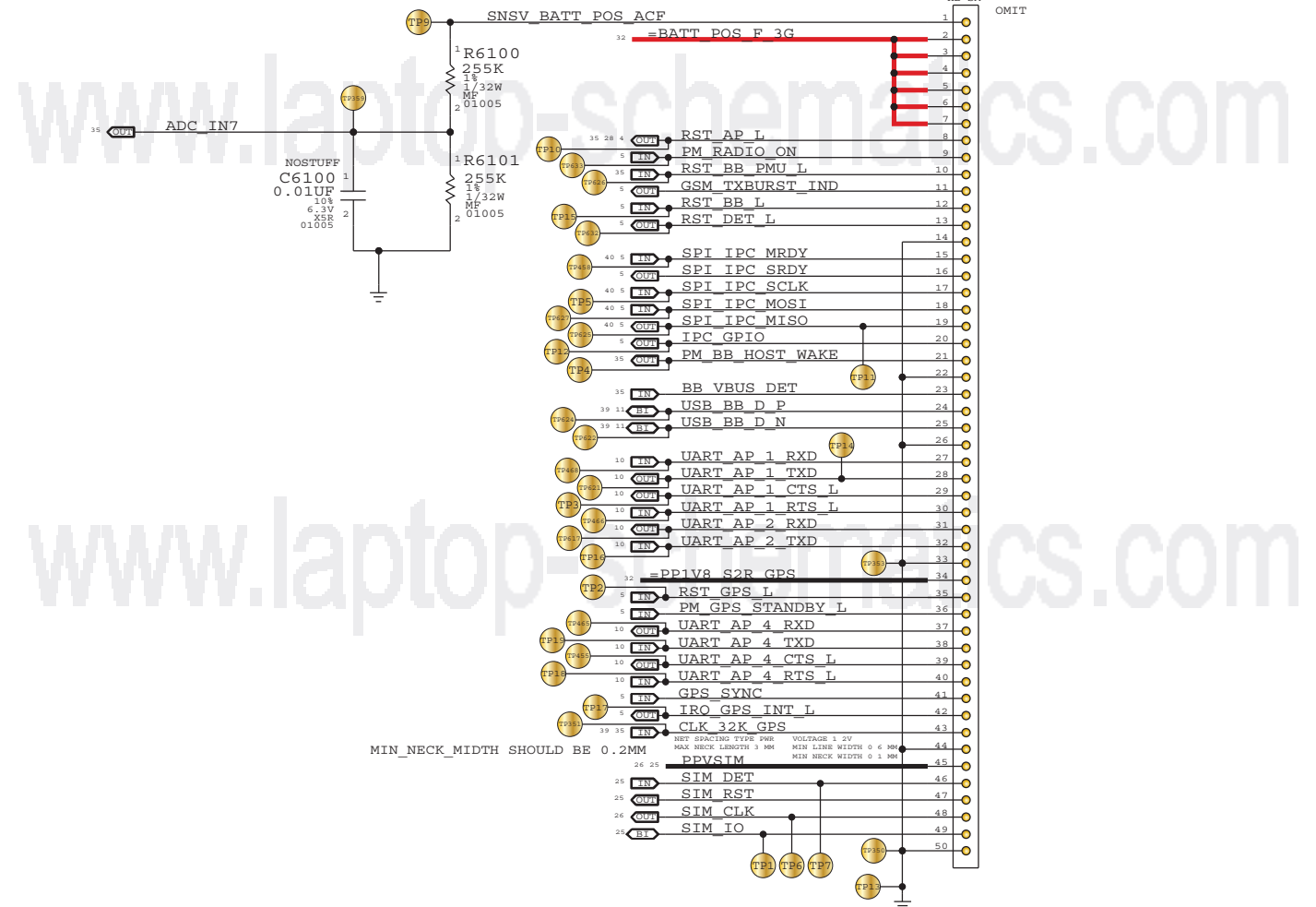
# X23 WIFI/BT CONNECTOR



SYNC MASTER=MIKE		SYNC DATE=N/A	
CONNECTOR: X23 WIFI/BT			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8962	D
		REVISION	
		A.0.0	
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# X24 CELLULAR/GPS CONNECTOR

998-3141  
J6100  
CELL-MODULE-X24



SYNC MASTER=MIKE		SYNC DATE=N/A	
CONNECTOR: X24 CELLULAR/GPS			
Apple Inc.	DRAWING NUMBER	051-8962	SIZE
	REVISION	A.0.0	D
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# POWER CONN / ALIAS

## LDO RAILS

PROGRAMMABLE ON/OFF

## BUCK RAILS

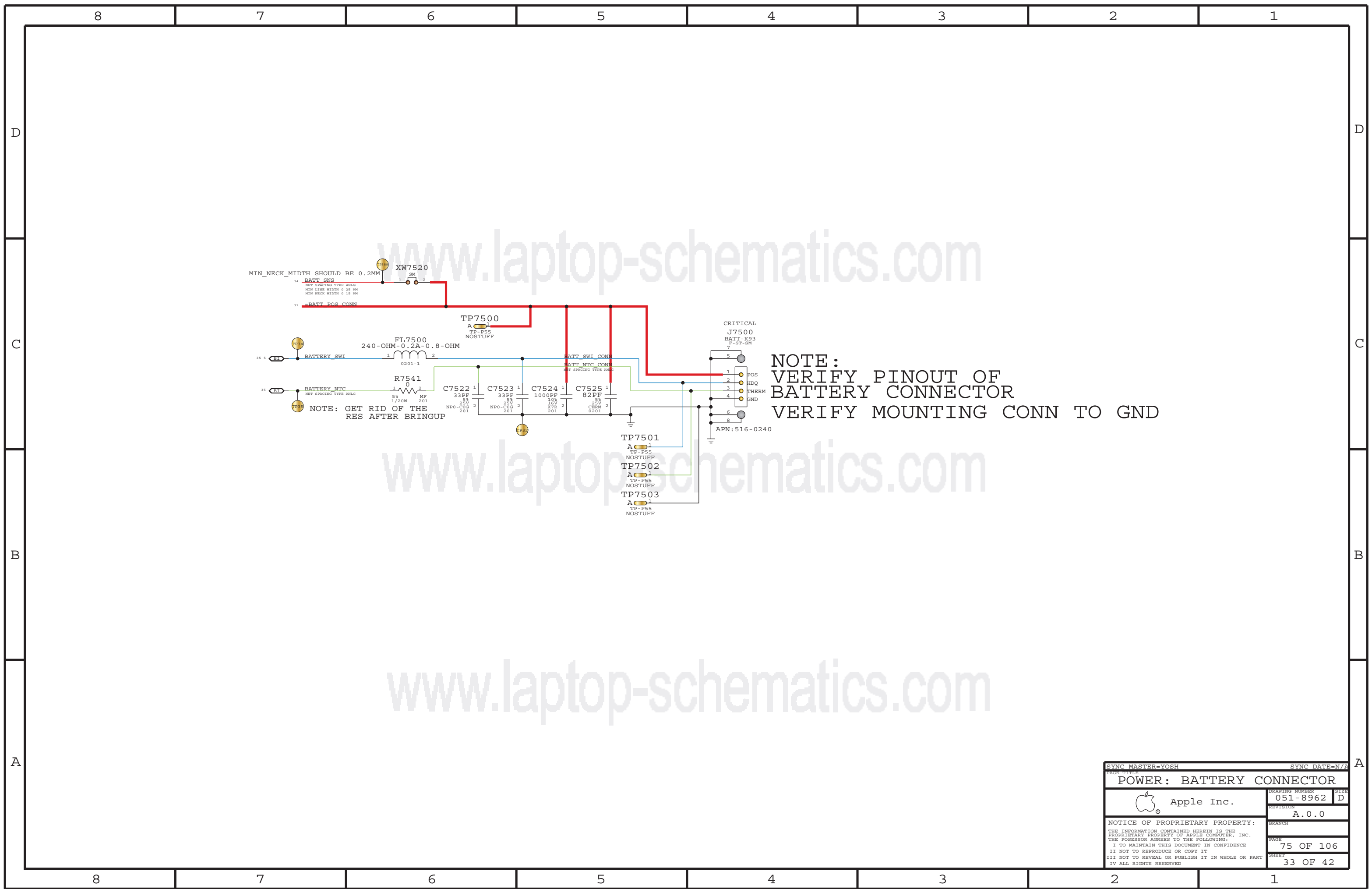
## CHARGER MAIN

## BATTERY

## USB POWER INPUT



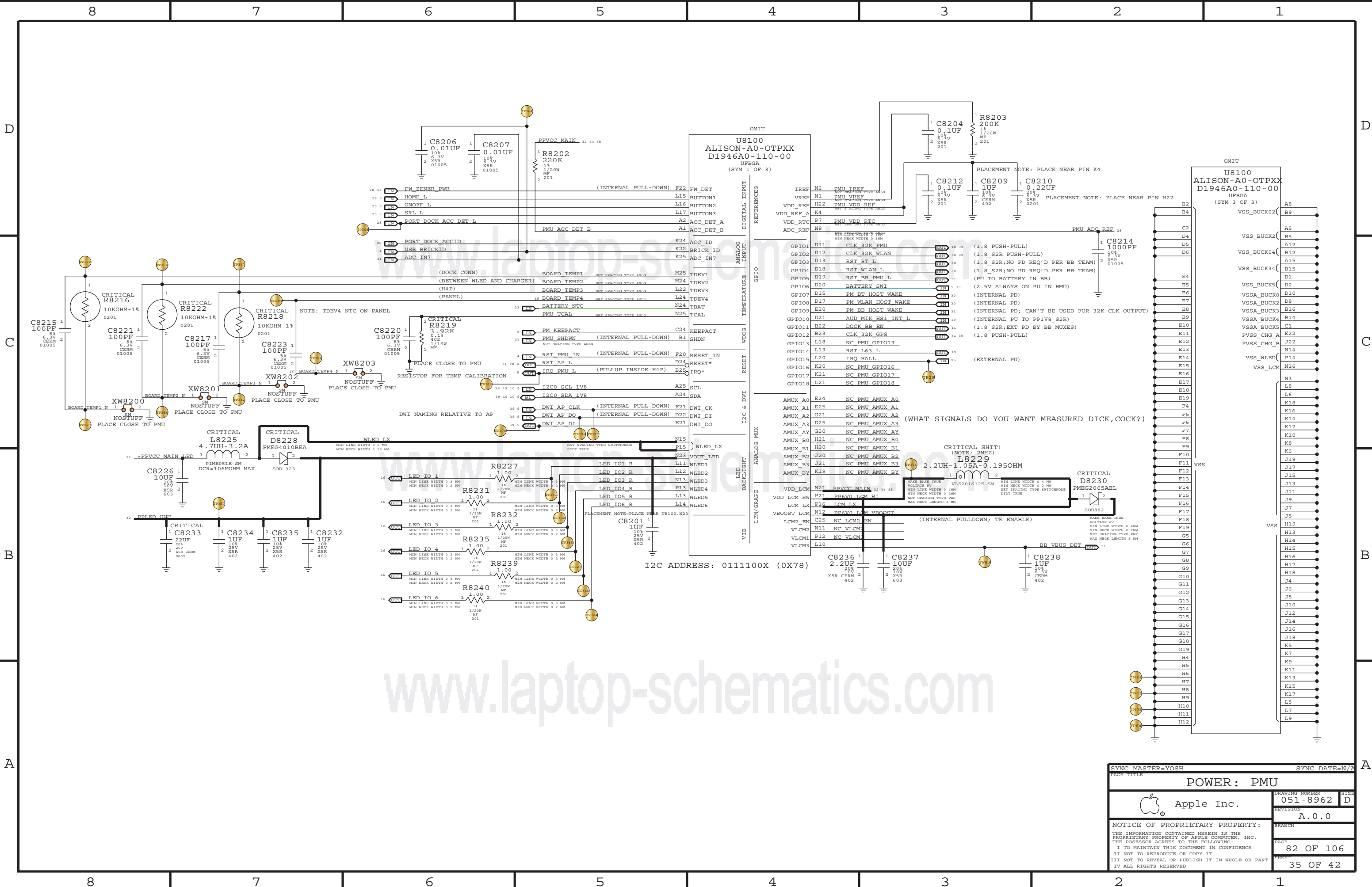
SYNC MASTER=YOSH		SYNC DATE=N/A	
PAGE TITLE: POWER: ALIASES			
Apple Inc.		DRAWING NUMBER: 051-8962	SIZE: D
		REVISION: A.0.0	
NOTICE OF PROPRIETARY PROPERTY:			
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NOTE:  
 VERIFY PINOUT OF  
 BATTERY CONNECTOR  
 VERIFY MOUNTING CONN TO GND

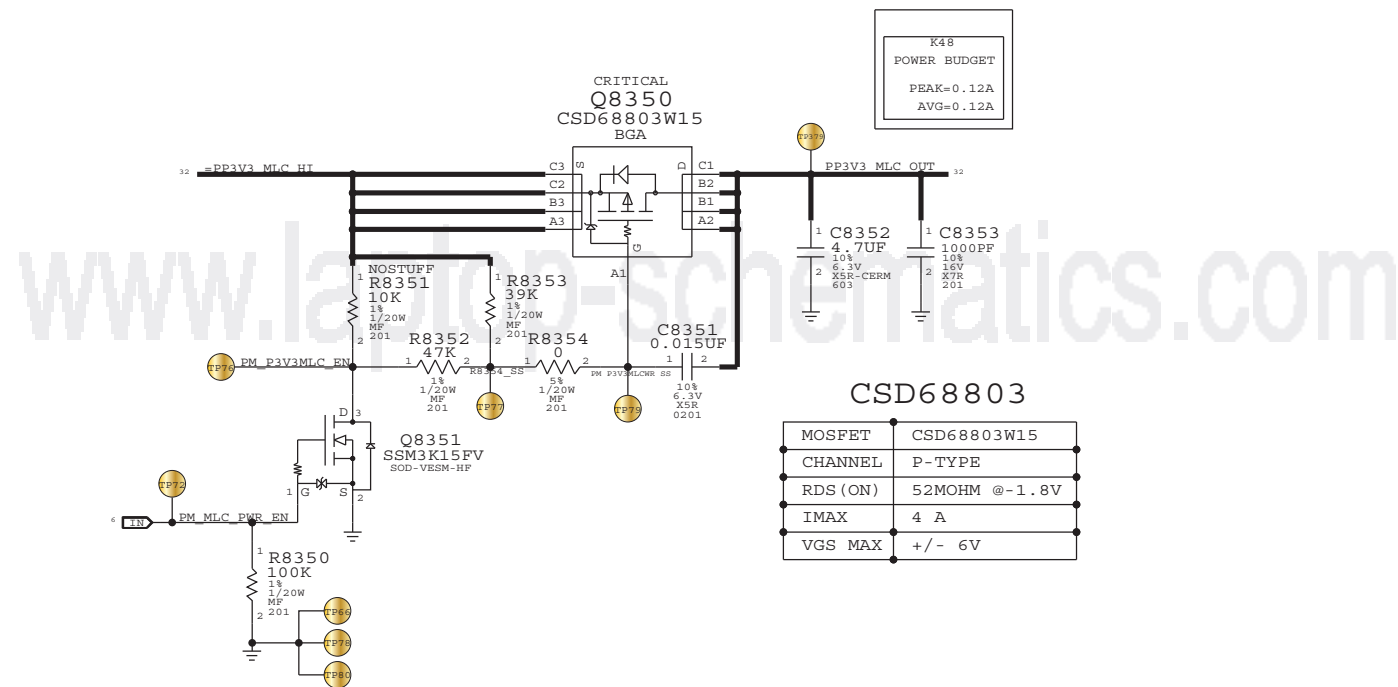
SYNC MASTER=YOSH		SYNC DATE=N/A	
POWER: BATTERY CONNECTOR			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8962	D
		REVISION	
		A.0.0	
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SYNC MASTER=YOSH		SYNC DATE=N/A	
<b>POWER: PMU</b>			
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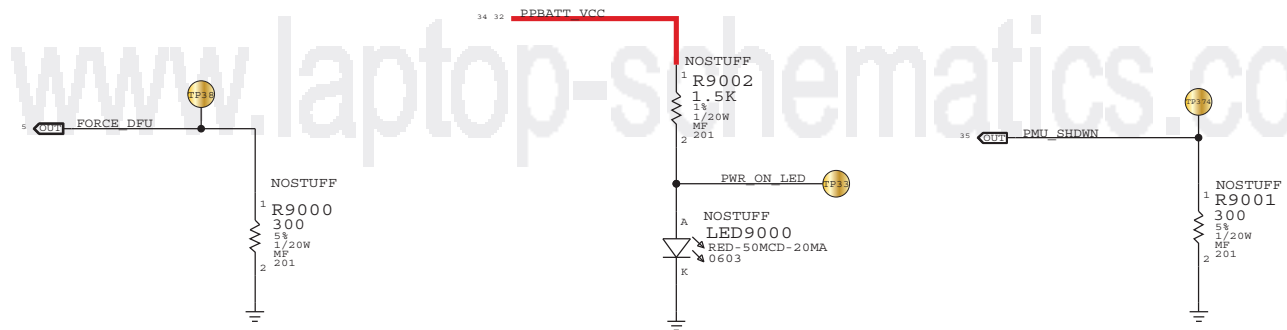


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
376S0972	376S0612		Q8351	RADAR: 8537160

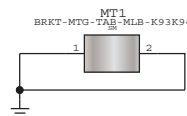
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POWER: 3.3V MLC & 1.2V VR			
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# DEBUG RESET ACCESS

PLACE OUTSIDE OF CAN?



LEFT AND RIGHT MOUNTING TABS

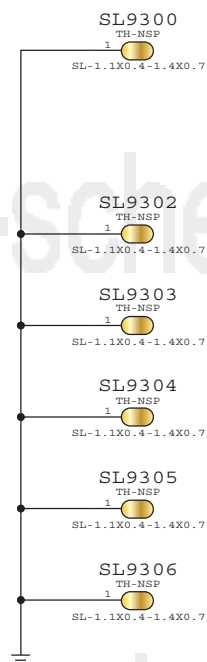


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Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET TYPE		
	PHYSICAL	SPACING	
HE0	CLK_50S	CLK	CLK 32K PMU 18 35
HE0	CLK_50S	CLK	CLK 32K WLAN 30 35
HE0	CLK_50S	CLK	CLK 32K GPS 31 35
HE0	CLK_50S	CLK	CLK CAM FF 7 26
HE0	CLK_50S	CLK	CLK CAM FF FILT 7 26
HE0	CLK_50S	CLK	CLK CAM FF CONN 25 26
HE0	CLK_50S	CLK	CLK CAM RF 7 27
HE0	CLK_50S	CLK	CLK CAM RF FILT 25 27
HE0	CLK_50S	CLK	I2S AP 0 MCK 4
HE0	CLK_50S	CLK	I2S AP 0 MCK R 4 19
HE0	CLK_50S	CLK	CLK CAM FF R 7
HE0	CLK_50S	CLK	CLK CAM RF R 7

NAND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
NAND_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
NAND	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET TYPE		
	PHYSICAL	SPACING	
HE0	NAND_50S	NAND	FOAD<7..0> 6 12
HE0	NAND_50S	NAND	FOCE0 L 4 12
HE0	NAND_50S	NAND	FOCE1 L 4 12
HE0	NAND_50S	NAND	FOCE2 L 4 12
HE0	NAND_50S	NAND	FOCE3 L 4 12
HE0	NAND_50S	NAND	FOCE4 L 4 12
HE0	NAND_50S	NAND	FOCE5 L 4 12
HE0	NAND_50S	NAND	FOCE6 L 4 12
HE0	NAND_50S	NAND	FOCE7 L 4 12
HE0	NAND_50S	NAND	FOCLE 4 12
HE0	NAND_50S	NAND	FOALE 4 12
HE0	NAND_50S	NAND	FORE L 4 12
HE0	NAND_50S	NAND	FOWE L 4 12
HE0	NAND_50S	NAND	FOWP L 4 12
HE0	NAND_50S	NAND	F1AD<7..0> 6 12
HE0	NAND_50S	NAND	F1CE0 L 4 12
HE0	NAND_50S	NAND	F1CE1 L 4 12
HE0	NAND_50S	NAND	F1CE2 L 4 12
HE0	NAND_50S	NAND	F1CE3 L 4 12
HE0	NAND_50S	NAND	F1CE4 L 4 12
HE0	NAND_50S	NAND	F1CE5 L 4 12
HE0	NAND_50S	NAND	F1CE6 L 4 12
HE0	NAND_50S	NAND	F1CE7 L 4 12
HE0	NAND_50S	NAND	F1CLE 4 12
HE0	NAND_50S	NAND	F1ALE 4 12
HE0	NAND_50S	NAND	F1RE L 4 12
HE0	NAND_50S	NAND	F1WE L 4 12
HE0	NAND_50S	NAND	F1WP L 4 12
HE0	NAND_50S	NAND	F2AD<7..0> 6 12
HE0	NAND_50S	NAND	F2CE0 L 4 12
HE0	NAND_50S	NAND	F2CE1 L 4 12
HE0	NAND_50S	NAND	F2CE2 L 4 12
HE0	NAND_50S	NAND	F2CE3 L 4 12
HE0	NAND_50S	NAND	F2CLE 4 12
HE0	NAND_50S	NAND	F2ALE 4 12
HE0	NAND_50S	NAND	F2RE L 4 12
HE0	NAND_50S	NAND	F2WE L 4 12
HE0	NAND_50S	NAND	F2WP L 4 12
HE0	NAND_50S	NAND	F3AD<7..0> 6 12
HE0	NAND_50S	NAND	F3CE0 L 4 12
HE0	NAND_50S	NAND	F3CE1 L 4 12
HE0	NAND_50S	NAND	F3CE2 L 4 12
HE0	NAND_50S	NAND	F3CE3 L 4 12
HE0	NAND_50S	NAND	F3CLE 4 12
HE0	NAND_50S	NAND	F3ALE 4 12
HE0	NAND_50S	NAND	F3RE L 4 12
HE0	NAND_50S	NAND	F3WE L 4 12
HE0	NAND_50S	NAND	F3WP L 4 12

JTAG

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
JTAG	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET TYPE		
	PHYSICAL	SPACING	
HE0	JTAG	JTAG	JTAG AP TCK 4 28
HE0	JTAG	JTAG	JTAG AP TMS 4 28
HE0	JTAG	JTAG	JTAG AP TDI 4 10
HE0	JTAG	JTAG	JTAG AP TDO 4 10
HE0	JTAG	JTAG	JTAG AP TRST_L 4 10

I2C

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2C_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2C	*	*	1.5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET TYPE		
	PHYSICAL	SPACING	
HE0	I2C_50S	I2C	I2C1_SDA_1V8 5 25
HE0	I2C_50S	I2C	I2C1_SCL_1V8 5 25
HE0	I2C_50S	I2C	I2C0_SDA_1V8 5 10 19 35
HE0	I2C_50S	I2C	I2C0_SCL_1V8 5 10 19 35
HE0	I2C_50S	I2C	I2C2_SDA_3V0 5 25 26
HE0	I2C_50S	I2C	I2C2_SCL_3V0 5 25 26
HE0	I2C_50S	I2C	ISP_AP_0_SCL 7 25
HE0	I2C_50S	I2C	ISP_AP_0_SDA 7 25
HE0	I2C_50S	I2C	ISP_AP_1_SCL 7 26
HE0	I2C_50S	I2C	ISP_AP_1_SDA 7 26
HE0	I2C_50S	I2C	I2C2_SCL_3V0_ALS 25 26
HE0	I2C_50S	I2C	I2C2_SDA_3V0_ALS 25 26
HE0	I2C_50S	I2C	ISP_CAM_1_SCL 25 26
HE0	I2C_50S	I2C	ISP_CAM_1_SDA 25 26

XTAL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRYSTAL	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET TYPE		
	PHYSICAL	SPACING	
HE0	CRYSTAL	CRYSTAL	XTAL 24M I 4
HE0	CRYSTAL	CRYSTAL	XTAL 24M O 4
HE0	CRYSTAL	CRYSTAL	24M O 4

VREF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VREF	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET TYPE		
	PHYSICAL	SPACING	
HE0	VREF	VREF	PPVREF_DDR0_CA *
HE0	VREF	VREF	PPVREF_DDR0_DO *
HE0	VREF	VREF	PPVREF_DDR1_CA *
HE0	VREF	VREF	PPVREF_DDR1_DO *

USB

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET TYPE		
	PHYSICAL	SPACING	
HE0	USB_90D	USB	USB D P 4 28
HE0	USB_90D	USB	USB D N 4 28
HE0	USB_90D	USB	USB_PT_DK_CON_D_P 28 29
HE0	USB_90D	USB	USB_PT_DK_CON_D_N 28 29
HE0	USB_90D	USB	USB_BB_D_P 11 31
HE0	USB_90D	USB	USB_BB_D_N 11 31
HE0	USB_90D	USB	USB_FS_D_P 4 11
HE0	USB_90D	USB	USB_FS_D_N 4 11
HE0	USB_90D	USB	USB_FS_N_ACC_TX 11 28
HE0	USB_90D	USB	USB_FS_P_ACC_RX 11 28
HE0	USB_90D	USB	ACC_PT_DK_CON_TX 28 29
HE0	USB_90D	USB	ACC_PT_DK_CON_RX 28 29

I2S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2S_90S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2S	*	*	3:1_SPACING
I2S	I2S	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET TYPE		
	PHYSICAL	SPACING	
HE0	I2S_50S	I2S	I2S_AP_0_BCLK 5 19
HE0	I2S_50S	I2S	I2S_AP_0_LRCK 5 19
HE0	I2S_50S	I2S	I2S_AP_0_DIN 5 19
HE0	I2S_50S	I2S	I2S_AP_0_DOUT 5 19
HE0	I2S_50S	I2S	I2S_AP_2_BCLK 5 19 30
HE0	I2S_50S	I2S	I2S_AP_2_LRCK 5 19 30
HE0	I2S_50S	I2S	I2S_AP_2_DIN 5 19 30
HE0	I2S_50S	I2S	I2S_AP_2_DOUT 5 19 30
HE0	I2S_50S	I2S	I63_VSP_SDOUT 19
HE0	I2S_50S	I2S	I2S_AP_3_BCLK 5 19
HE0	I2S_50S	I2S	I2S_AP_3_LRCK 5 19
HE0	I2S_50S	I2S	I2S_AP_3_DIN 5 19
HE0	I2S_50S	I2S	I2S_AP_3_DOUT 5 19
HE0	I2S_50S	I2S	I63_XSP_SDOUT 19

DWI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DWI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET TYPE		
	PHYSICAL	SPACING	
HE0	DWI	DWI	DWI AP CLK 5 35
HE0	DWI	DWI	DWI AP DI 5 35
HE0	DWI	DWI	DWI AP DO 5 35

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ANALOG VIDEO CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
VID_50S	*	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ANALOG_VIDEO	*	*	5:1_SPACING
ANALOG_VIDEO	ANALOG_VIDEO	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET TYPE		SPACING	PHYSICAL
	PHYSICAL	SPACING		
1E230	VID_50S	ANALOG_VIDEO	DAC AP OUT1	7 11
1E230	VID_50S	ANALOG_VIDEO	DAC AP OUT2	7 11
1E230	VID_50S	ANALOG_VIDEO	DAC AP OUT3	7 11
1E230	VID_50S	ANALOG_VIDEO	BUF C Y	11
1E230	VID_50S	ANALOG_VIDEO	BUF CVBS PB	11
1E230	VID_50S	ANALOG_VIDEO	BUF Y PR	11
1E230	VID_50S	ANALOG_VIDEO	VIDEO EMI CVBS PB	10 11 28
1E230	VID_50S	ANALOG_VIDEO	VIDEO EMI C Y	10 11 28
1E230	VID_50S	ANALOG_VIDEO	VIDEO EMI Y PR	10 11 28
1E230	VID_50S	ANALOG_VIDEO	VIDEO PT DK CON CVBS PB	28 29
1E230	VID_50S	ANALOG_VIDEO	VIDEO PT DK CON C Y	28 29
1E230	VID_50S	ANALOG_VIDEO	VIDEO PT DK CON Y PR	28 29

LVDS

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET TYPE		SPACING	PHYSICAL
	PHYSICAL	SPACING		
1E240	LVDS_100D	LVDS	LVDS DATA P<2 .0>	14 16
1E240	LVDS_100D	LVDS	LVDS DATA N<2 .0>	14 16
1E240	LVDS_100D	LVDS	LVDS DATA CONN P<2..0>	14 16
1E240	LVDS_100D	LVDS	LVDS DATA CONN N<2..0>	14 16
1E240	LVDS_100D	LVDS	LVDS CLK P	14 16
1E240	LVDS_100D	LVDS	LVDS CLK N	14 16
1E240	LVDS_100D	LVDS	LVDS CLK CONN P	14 16
1E240	LVDS_100D	LVDS	LVDS CLK CONN N	14 16

DISPLAYPORT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET TYPE		SPACING	PHYSICAL
	PHYSICAL	SPACING		
1E240	DP_100D	DP	DP AP TX P<0>	7 10 13
1E240	DP_100D	DP	DP AP TX N<0>	7 10 13
1E240	DP_100D	DP	DP AP TX P<1>	7 10 13
1E240	DP_100D	DP	DP AP TX N<1>	7 10 13
1E240	DP_100D	DP	DP AP AUX P	7 13
1E240	DP_100D	DP	DP AP AUX N	7 13
1E240	DP_100D	DP	DP EMI TX P<0>	13 28
1E240	DP_100D	DP	DP EMI TX N<0>	13 28
1E240	DP_100D	DP	DP EMI TX P<1>	13 28
1E240	DP_100D	DP	DP EMI TX N<1>	13 28
1E240	DP_100D	DP	DP EMI AUX P	13 28
1E240	DP_100D	DP	DP EMI AUX N	13 28
1E240	DP_100D	DP	DP PT DK CON TX P<0>	28 29
1E240	DP_100D	DP	DP PT DK CON TX N<0>	28 29
1E240	DP_100D	DP	DP PT DK CON TX P<1>	28 29
1E240	DP_100D	DP	DP PT DK CON TX N<1>	28 29
1E240	DP_100D	DP	DP PT DK CON AUX P	28 29
1E240	DP_100D	DP	DP PT DK CON AUX N	28 29

MIPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MIPI_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET TYPE		SPACING	PHYSICAL
	PHYSICAL	SPACING		
1E240	MIPI_100D	MIPT	MIPI AP DATA P<0>	7 14
1E240	MIPI_100D	MIPT	MIPI AP DATA N<0>	7 14
1E240	MIPI_100D	MIPT	MIPI AP DATA P<1>	7 14
1E240	MIPI_100D	MIPT	MIPI AP DATA N<1>	7 14
1E240	MIPI_100D	MIPT	MIPI AP DATA P<2>	7 14
1E240	MIPI_100D	MIPT	MIPI AP DATA N<2>	7 14
1E240	MIPI_100D	MIPT	MIPI AP DATA P<3>	7 14
1E240	MIPI_100D	MIPT	MIPI AP DATA N<3>	7 14
1E240	MIPI_100D	MIPT	MIPI AP CLK P	7 14
1E240	MIPI_100D	MIPT	MIPI AP CLK N	7 14
1E240	MIPI_100D	MIPT	MIPI OC AP DATA P<0>	7 27
1E240	MIPI_100D	MIPT	MIPI OC AP DATA N<0>	7 27
1E240	MIPI_100D	MIPT	MIPI OC AP CLK P	7 27
1E240	MIPI_100D	MIPT	MIPI OC AP CLK N	7 27
1E240	MIPI_100D	MIPT	MIPI OC CAM DATA P<0>	25 27
1E240	MIPI_100D	MIPT	MIPI OC CAM DATA N<0>	25 27
1E240	MIPI_100D	MIPT	MIPI OC CAM CLK P	25 27
1E240	MIPI_100D	MIPT	MIPI OC CAM CLK N	25 27
1E240	MIPI_100D	MIPT	MIPI IC AP DATA P<0>	7 26
1E240	MIPI_100D	MIPT	MIPI IC AP DATA N<0>	7 26
1E240	MIPI_100D	MIPT	MIPI IC AP CLK P	7 26
1E240	MIPI_100D	MIPT	MIPI IC AP CLK N	7 26
1E240	MIPI_100D	MIPT	MIPI IC CAM DATA P<0>	25 26
1E240	MIPI_100D	MIPT	MIPI IC CAM DATA N<0>	25 26
1E240	MIPI_100D	MIPT	MIPI IC CAM CLK P	25 26
1E240	MIPI_100D	MIPT	MIPI IC CAM CLK N	25 26

AUDIO/SPEAKER

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIO	*	1:1_DIFFPAIR
SPEAKER	*	SPEAKER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET TYPE		SPACING	PHYSICAL
	PHYSICAL	SPACING		
1E240	AUDIO	AUDIO	LEFT CH OUT P	19 20
1E240	AUDIO	AUDIO	LEFT CH OUT REF	19 20
1E240	AUDIO	AUDIO	LEFT CH P	20
1E240	AUDIO	AUDIO	SSM2375 L IN P	20
1E240	AUDIO	AUDIO	SSM2375 L IN N	20
1E240	AUDIO	AUDIO	RIGHT CH OUT P	19 20
1E240	AUDIO	AUDIO	RIGHT CH OUT REF	19 20
1E240	AUDIO	AUDIO	RIGHT CH P	20
1E240	AUDIO	AUDIO	SSM2375 R IN P	20
1E240	AUDIO	AUDIO	SSM2375 R IN N	20
1E240	AUDIO	AUDIO	EXT MIC P	19 23
1E240	AUDIO	AUDIO	EXT MIC REF	19 23

SDIO

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SDIO_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SDIO	*	*	2:1_SPACING
SDIO_CLK	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET TYPE		SPACING	PHYSICAL
	PHYSICAL	SPACING		
1E240	SDIO_50S	SDIO	SDIO WL CLK	5 30
1E240	SDIO_50S	SDIO	SDIO WL CLK R	5 30
1E240	SDIO_50S	SDIO	SDIO WL CMD	5 30
1E240	SDIO_50S	SDIO	SDIO WL DATA<3 0>	5 30

SPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SPI_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET TYPE		SPACING	PHYSICAL
	PHYSICAL	SPACING		
1E240	SPT_50S	SPT	SPI GRAPE MISO	5 17
1E240	SPT_50S	SPT	SPI GRAPE MOSI	5 17
1E240	SPT_50S	SPT	SPI GRAPE SCLK	5 17
1E240	SPT_50S	SPT	SPI GRAPE CS L	5 17
1E240	SPT_50S	SPT	SPI IPC MISO	5 31
1E240	SPT_50S	SPT	SPI IPC MOSI	5 31
1E240	SPT_50S	SPT	SPI IPC SCLK	5 31
1E240	SPT_50S	SPT	SPI IPC MRDY	5 31

SYNC MASTER=MIKE SYNC DATE=N/A

PAGE TITLE: CONSTRAINTS: ASSIGNMENTS

Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D

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# MLB CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, BOTTOM	NO_TYPE, BGA, BGA06-06	MM	15.2

## PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	3.0 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

### SINGLE-ENDED PHYSICAL RULES 45 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	ISL2, ISL3, ISL6, ISL9	Y	0.055 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL4, ISL5, ISL6, ISL7	Y	0.060 MM	0.060 MM	3.0 MM		
45_OHM_SE	*	N	0.060 MM	0.060 MM	3.0 MM		

### 50 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.085 MM	0.085 MM	3.0 MM		
50_OHM_SE	*	N	0.050 MM	0.050 MM	3.0 MM		

### 50 OHMS - CLEAR ON LAYER 2 AND 5

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE_RF	TOP	Y	0.240 MM	0.240 MM	3.0 MM		
50_OHM_SE	ISL4	Y	0.060 MM	0.060 MM	3.0 MM		

### 50 OHMS - CLEAR ON TOP AND BOTTOM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	ISL2, ISL9	Y	0.090 MM	0.090 MM	3.0 MM		

### DIFFERENTIAL PAIR PHYSICAL RULES

#### 100 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	TOP, BOTTOM	Y	0.076 MM	0.076 MM		0.210 MM	0.210 MM
100_OHM_DIFF	N	Y	0.057 MM	0.057 MM	=STANDARD	0.300 MM	0.300 MM

#### 90 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP, BOTTOM	Y	0.095 MM	0.095 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2, ISL3, ISL6, ISL9	Y	0.054 MM	0.054 MM	=STANDARD	0.200 MM	0.100 MM
90_OHM_DIFF	ISL4, ISL5, ISL6, ISL7	Y	0.060 MM	0.060 MM	=STANDARD	0.200 MM	0.100 MM

### AUDIO PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.08 MM	0.08 MM
SPEAKER	*	Y	0.3 MM	0.19MM	1.0 MM	0.08 MM	0.08 MM

### BGA AREA PHYSICAL RULES

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	BGA_PHY

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BGA_PHY	*	Y	0.060 MM	0.060 MM	=STANDARD	0.076 MM	0.075 MM

## SPACING CONSTRAINTS

### DEFAULT/BGA SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.08 MM	?
STANDARD	*	=DEFAULT	?
BGA_SPA	*	=DEFAULT	?

### REGULAR SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.060 MM	?
0P08_SPACING	*	0.080 MM	?
1.5:1_SPACING	*	0.090 MM	?
2:1_SPACING	*	0.120 MM	?
2.5:1_SPACING	*	0.150 MM	?
3:1_SPACING	*	0.180 MM	?
4:1_SPACING	*	0.240 MM	?
5:1_SPACING	*	0.300 MM	?
0P5MM_SPACING	*	0.5 MM	?
0P64MM_SPACING	*	0.64 MM	?

\*NOTE: ASSUMING 0.060MM DIELECTRIC THICKNESS


### POWER/GND SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR_P1SPACING	*	0.1 MM	900
GND_P1SPACING	*	0.1 MM	950
SWITCHNODE	*	0.5 MM	1000
SWITCHNODE	TOP, BOTTOM	0.2 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_SPA
CLK	*	BGA	BGA_SPA
PWR	*	*	PWR_P1SPACING
GND	*	*	GND_P1SPACING
SWITCHNODE	*	*	SWITCHNODE
ANLG	*	*	3:1_SPACING

### NOTES:

- 0.075 MM ~ 3 MIL
- 0.089 MM ~ 3.5 MIL
- 0.102 MM ~ 4 MIL
- 0.114 MM ~ 4.5 MIL
- 0.125 MM ~ 5 MIL
- 0.140 MM ~ 5.5 MIL
- 0.15 MM ~ 6 MIL
- 0.18 MM ~ 7 MIL
- 0.2 MM ~ 8 MIL
- 0.25 MM ~ 10 MIL
- 0.3 MM ~ 12 MIL
- 0.33 MM ~ 13 MIL
- 0.4 MM ~ 16 MIL
- 1.0 MM = 39.37 MIL

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