1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEMATIC , WHITE_ARROW,MLB

02/01/10

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

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11	12	CPU DDR3 Interfaces	K17_REF	06/15/2009
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13	14	CPU Power (2 of 2)	K17_REF	06/15/2009
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17	18	PCH SATA/PCIE/CLK/LPC/SPI	K17_REF	08/24/2009
18	19	PCH DMI/FDI/Graphics	K17_REF	06/15/2009
19	20	PCH PCI/FlashCache/USB	K18_MLB	10/07/2009
20	21	PCH MISC	K17_REF	06/15/2009
21	22	PCH Power	K17_REF	06/15/2009
22	23	PCH Grounds	K17_REF	06/15/2009
23	24	PCH Non-GFX Decoupling	K17_REF	06/15/2009
24	25	CPU/PCH GFX Decoupling	K17_REF	06/15/2009
25	26	eXtended Debug Port (XDP)	K17_REF	06/15/2009
26	27	Clock (CK505)	K17_MLB	06/23/2009
27	28	Chipset Support	K17_REF	06/15/2009
28	29	DDR3 SO-DIMM Connector A	MASTER	MASTER
29	30	DDR3 Byte/Bit Swaps	MASTER	MASTER
30	31	DDR3 SO-DIMM Connector B	MASTER	MASTER
31	32	CPU Memory S3 Support	K17_REF	06/15/2009
32	33	FSB/DDR3/FRAMEBUF Vref Margining	K17_REF	06/15/2009
33	34	X16/ALS/CAMERA CONNECTOR	K18_COMMS	06/15/2009
34	35	SecureDigital Card Reader	T27_REF	08/26/2009
35	36	USB HUB 1	K18_MLB	10/07/2009
36	37	USB HUB 2	K23F	10/06/2009
37	39	Ethernet PHY (Caesar II/IV)	T27_REF	08/20/2009
38	40	Ethernet Connector	K17_REF	06/15/2009
39	41	FireWire LLC/PHY (FW643)	K19_MLB	05/29/2009
40	42	FireWire Port Power	K19_MLB	05/29/2009
41	43	FireWire Ports	K19_MLB	05/29/2009
42	45	SATA Connectors	T27_REF	10/01/2009
43	46	External USB Connectors	K17_REF	06/15/2009
44	48	Front Flex Support	K19_MLB	05/29/2009
45	49	SMC	K17_REF	06/15/2009
46	50	SMC Support	K18_SENSORS	06/29/2009
47	51	LPC+SPI Debug Connector	K17_MLB	06/23/2009
48	52	K18 SMBus Connections	K18_SENSORS	06/18/2009
49	53	Current & Voltage Sensing	K18_SENSORS	06/29/2009
50	54	Current Sensing	K18_SENSORS	07/02/2009
51	55	Thermal Sensors	K18_SENSORS	06/18/2009
52	56	Fan Connectors	K19_MLB	05/29/2009
53	57	WELLSPRING 1	K19_MLB	05/29/2009
54	58	WELLSPRING 2	K19_MLB	05/29/2009
55	59	Sudden Motion Sensor (SMS)	K19_MLB	05/29/2009
56	60	DEBUG SENSORS AND ADC	K18_SENSORS	07/07/2009
57	61	SPI ROM	K17_REF	06/15/2009
58	62	AUDIO: CODEC/REGULATOR	K18_AUDIO	09/21/2009
59	63	AUDIO: LINE INPUT FILTER	K18_AUDIO	07/29/2009
60	65	AUDIO: HEADPHONE FILTER	K18_AUDIO	07/29/2009
61	66	AUDIO: SPEAKER AMP	K18_AUDIO	07/29/2009
62	67	AUDIO: JACKS	K18_AUDIO	07/29/2009
63	68	AUDIO: JACK TRANSLATORS	K18_AUDIO	07/29/2009
64	69	DC-In & Battery Connectors	K18_POWER	06/30/2009
65	70	PBus Supply & Battery Charger	K18_POWER	06/30/2009
66	72	5V / 3.3V Power Supply	K18_POWER	07/13/2009
67	73	1.5V DDR3 Supply	K18_POWER	07/14/2009
68	74	CPU IMVP VCore Regulator	K18_POWER	06/29/2009
69	75	GFX IMVP VCore Regulator	K18_POWER	07/08/2009
70	76	CPUVTT (1.05V) Power Supply	K18_POWER	07/14/2009
71	77	Misc Power Supplies	K18_POWER	06/29/2009
72	78	Power FETs	K18_POWER	06/10/2009
73	79	Power Control	K17_REF	06/15/2009
74	80	NV GT216 PCI-E	K17_REF	06/15/2009
75	81	NV GT216 CORE/FB POWER	K17_REF	06/15/2009
76	82	NV GT216 FRAME BUFFER I/F	K17_REF	06/15/2009
77	84	GDDR3 Frame Buffer A (Top)	K17_REF	06/15/2009
78	85	GDDR3 Frame Buffer B (Top)	K17_REF	06/15/2009
79	86	NV GT216 GPIO/MIO/MISC	K17_REF	06/15/2009
80	87	GT216 GPIOS & STRAPS	K17_REF	06/15/2009
81	88	NV GT216 VIDEO INTERFACES	K17_REF	06/15/2009
82	89	GPU (GT216) CORE SUPPLY	K18_POWER	07/14/2009
83	90	LVDS Display Connector	K19_MLB	05/29/2009
84	93	Muxed Graphics Support	K17_REF	06/15/2009
85	94	DisplayPort Connector	K17_REF	06/15/2009
86	95	1V8 / 1V55 FB Power Supply	K18_POWER	06/26/2009
87	96	Graphics MUX (GMUX)	K17_REF	06/15/2009
88	97	LCD BACKLIGHT DRIVER	K18_BKLT	07/29/2009
89	98	LCD Backlight Support	K19_MLB	05/29/2009
90	99	Misc Power Supplies	K18_POWER	06/10/2009
91	100	CPU Constraints	K17_REF	06/15/2009
92	101	Memory Constraints	K17_REF	06/15/2009
93	102	PCH Constraints 1	K17_REF	06/15/2009
94	103	PCH Constraints 2	K17_REF	06/15/2009
95	104	Ethernet Constraints	K17_REF	06/15/2009
96	105	FireWire Constraints	K17_REF	06/15/2009
97	106	SMC Constraints	K17_REF	06/15/2009
98	107	GPU (GT216) CONSTRAINTS	K17_REF	06/15/2009
99	108	Project Specific Constraints	K17_REF	06/15/2009
100	109	PCB Rule Definitions	K17_REF	06/15/2009
101	132	BluRay Decrypter Card Connector	K17_REF	06/15/2009

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DRAWING TITLE: SCHEM,WHITE_ARROW,MLB,K18

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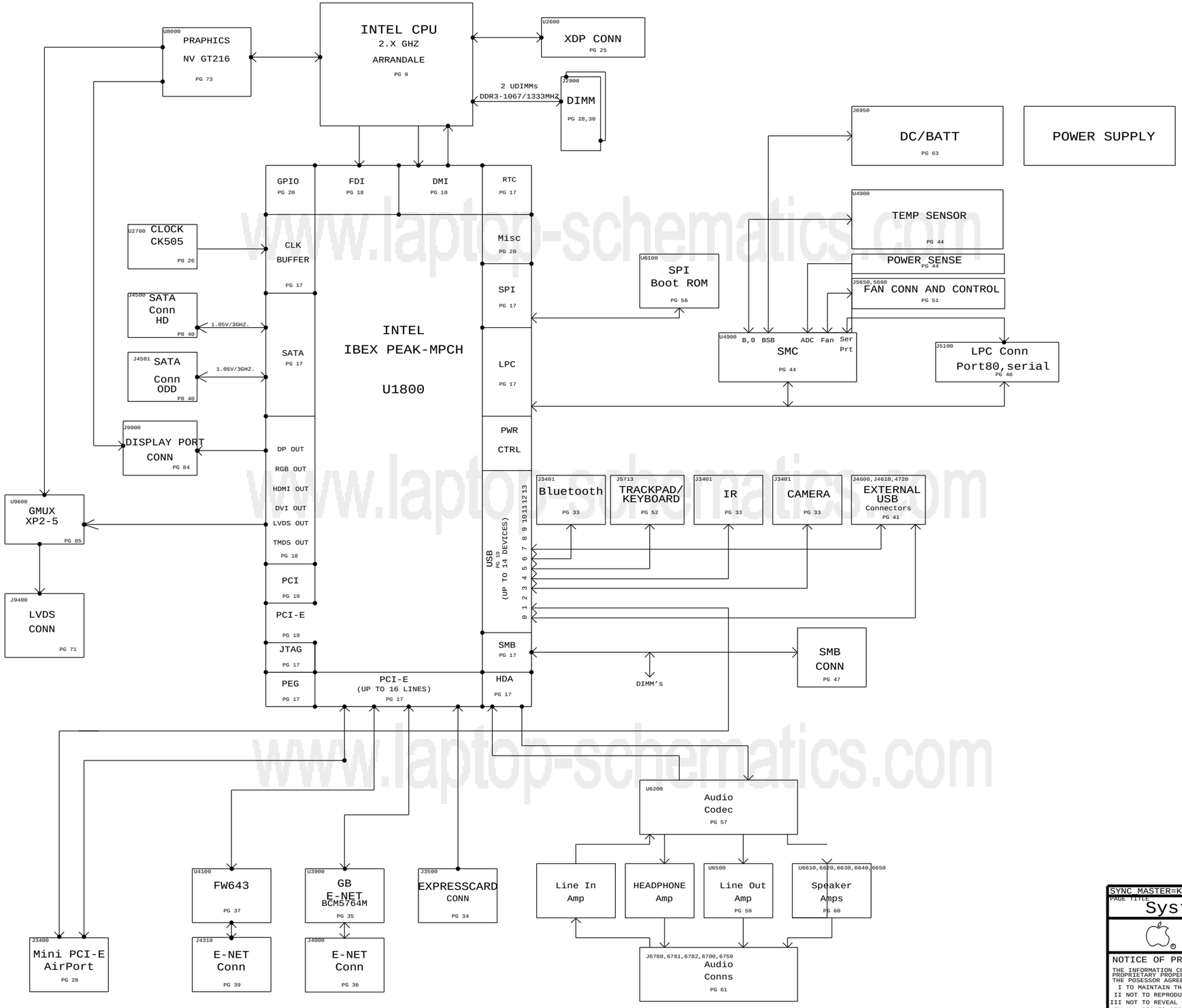

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System Block Diagram

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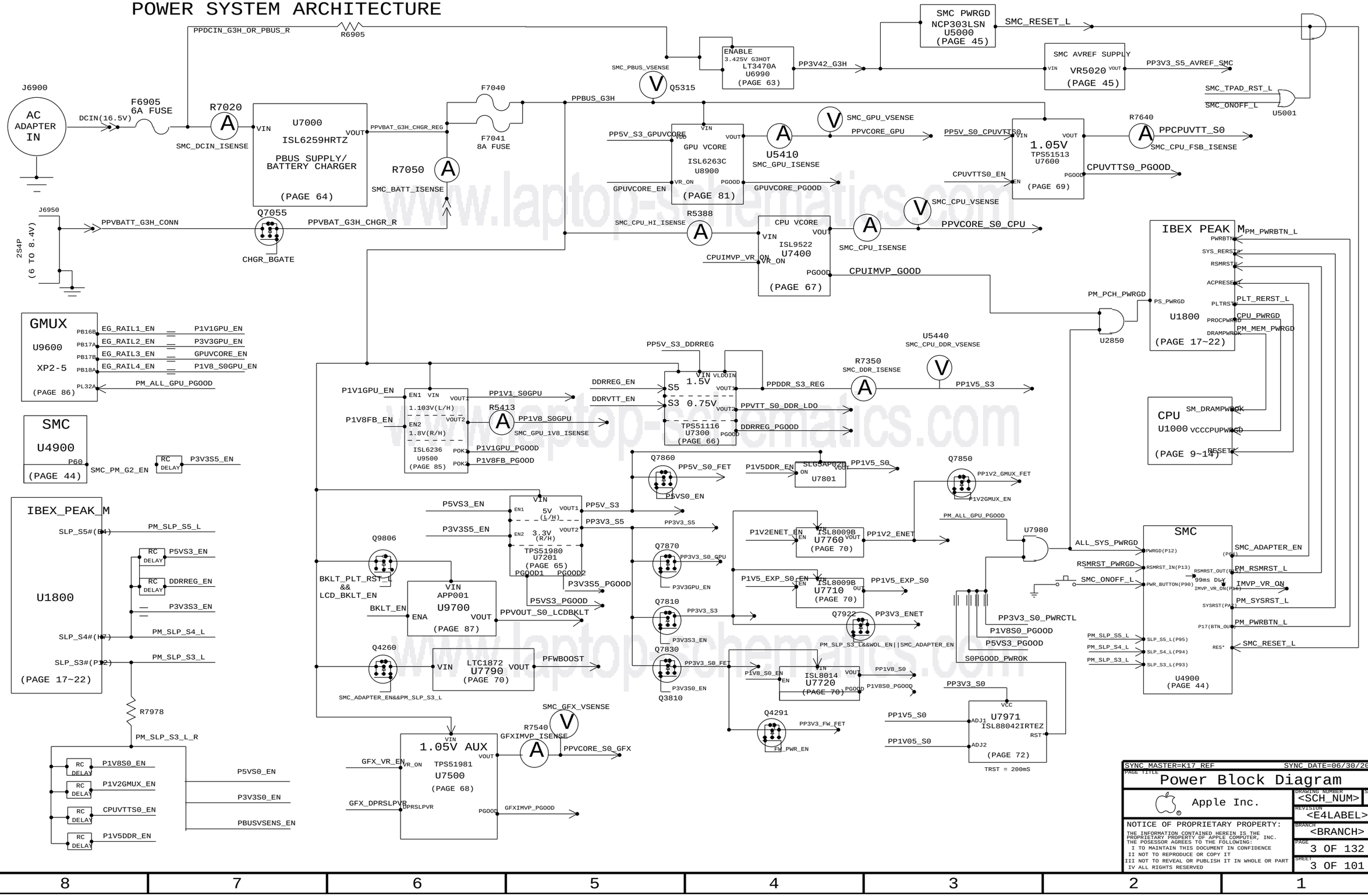
POWER SYSTEM ARCHITECTURE



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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8504	1	SCHEM,WHITE_ARROW,MLB,K18	SCH	CRITICAL	
820-2850	1	PCBF,WHITE_ARROW,MLB,K18	PCB	CRITICAL	

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TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 1 10:13:48 2010

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0952	PCBA,2.0G,512SAM_VRAM,K18	K18_COMMON,CPU_2_4GHZ,FB_256_SAMSUNG,K18_PVT,EEEE_DCJ7
639-0953	PCBA,2.0G,512HYN_VRAM,K18	K18_COMMON,CPU_2_4GHZ,FB_256_HYNIX,K18_PVT,EEEE_DCJ8
639-0954	PCBA,2.13G,512SAM_VRAM,K18	K18_COMMON,CPU_2_53GHZ,FB_512_SAMSUNG,K18_PVT,EEEE_DCJ9
639-0955	PCBA,2.13G,512HYN_VRAM,K18	K18_COMMON,CPU_2_53GHZ,FB_512_HYNIX,K18_PVT,EEEE_DCJC
639-0956	PCBA,2.4G,512SAM_VRAM,K18	K18_COMMON,CPU_2_66GHZ,FB_512_SAMSUNG,K18_PVT,EEEE_DCJD
639-0957	PCBA,2.4G,512HYN_VRAM,K18	K18_COMMON,CPU_2_66GHZ,FB_512_HYNIX,K18_PVT,EEEE_DCJF
085-1404	K18 DEVELOPMENT BOM	

K18 BOM GROUPS

BOM GROUP	BOM OPTIONS
K18_COMMON	ALTERNATE,COMMON,K18_COMMON1,K18_COMMON2,K18_PROGPARTS,USBHUB_2061,RDRV:8515A2,DCI
K18_COMMON1	BATT_3S,BCM5764M,GL137,CPUPOC_IMAX_40_50,CPUMEM_S0,SMC_EXCARD_NOT,SMC_DEBUG_YES,HUB1_2NONREM,HUB2_3NONREM
K18_COMMON2	GMUXPLL_3V3,GPU_SS_INT,MIKEY,GPUVID_0P90V,DPMUX_EN_PLD,DP_CA_DET_EG_PLD,DP_ESD,VFRQ_SLPS3,SMC_OSC_YES,RAIL_MON
K18_PVT	BMON_PROD,VREFMRGN_NOT,XDP,XDP_NORMAL,XDP_CPU_BPM
K18_PROGPARTS	GMUX_PROG,BOOTROM_PROG,SMC_PROG,TPAD_PROG

BOM GROUP	BOM OPTIONS
FB_256_SAMSUNG	VRAM4,VRAM_256_SAMSUNG,FB1V55
FB_256_HYNIX	VRAM4,VRAM_256_HYNIX,FB1V55
FB_512_SAMSUNG	VRAM4,VRAM_512_SAMSUNG,FB1V35
FB_512_HYNIX	VRAM4,VRAM_512_HYNIX,FB1V35

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602		ALL	Murata alt to Samsung
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
152S0896	152S0518		ALL	MAG LAYERS ALT TO CYNTEC
155S0457	155S0329		ALL	MAG LAYERS ALT TO MURATA
333S0506	333S0535		ALL	Hynix 900M alt to 1000M
516S0805	516S0806		ALL	Molex alt to Foxconn
152S1102	152S1088		ALL	Mag layer alt to Vishay
353S2805	353S2603		ALL	Fairchild wafer option
333S0542	333S0507		ALL	Samsung I die alt to H
128S0264	128S0257		ALL	Sanyo alt to Kemet
128S0303	128S0282		ALL	Panasonic alt to Sanyo
337S3808	337S3839		ALL	A02 alt to A03 GPU
128S0305	128S0294		ALL	6.3V alt to 11V Sanyo

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJ7]	CRITICAL	EEEE_DCJ7
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJ8]	CRITICAL	EEEE_DCJ8
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJ9]	CRITICAL	EEEE_DCJ9
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJC]	CRITICAL	EEEE_DCJC
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJD]	CRITICAL	EEEE_DCJD
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJF]	CRITICAL	EEEE_DCJF

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3848	1	ARD,SLBPE,PRQ,2.66G,35W,C2,3M,BGA	U1000	CRITICAL	CPU_2_66GHZ
337S3847	1	ARD,SLBPF,PRQ,2.53G,35W,C2,3M,BGA	U1000	CRITICAL	CPU_2_53GHZ
337S3846	1	ARD,SLBNA,PRQ,2.4G,35W,C2,4M,BGA	U1000	CRITICAL	CPU_2_4GHZ
337S3849	1	IC,PCH,IBEX PEAK-M,SLGZS,PRQ,B3,BGA	U1800	CRITICAL	
337S3839	1	IC,GPU,NV GT216 LP++,969BGA,40NM,A03	U8000	CRITICAL	
343S0493	1	IC,ASIC,BCM5764M,ENET CONTROLLER,8X8,64 QFN	U3900	CRITICAL	BCM5764M
341S2731	1	IC,1MBIT,SPI FLASH,K17/K18	U3990	CRITICAL	
338S0753	1	IC,FW643-E2,1394B PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	
338S0563	1	IC,SMC,HS8/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341T0233	1	IC,SMC,K18	U4900	CRITICAL	SMC_PROG
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341S2562	1	IC,EFI ROM,DEVELOPMENT,K18	U6100	CRITICAL	BOOTROM_PROG
341S2384	1	IR,ENCORE II, CY7C63833-LFXC	U4800	CRITICAL	
341S2616	1	IC,PSOC +W/USB,56PIN,MLF,K18	U5701	CRITICAL	TPAD_PROG
336S0025	1	IC,XP2-5,HF,CPLD,BLANK	U9600	CRITICAL	GMUX_5K_BLANK
341S2566	1	IC,CPLD,LATTICE,132CSBGA,K18	U9600	CRITICAL	GMUX_PROG
333S0507	4	IC,SGRAM,GDDR3,16MX32,1000MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_SAMSUNG
333S0483	4	IC,SDRAM,GDDR3,16MX32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_HYNIX
333S0533	4	IC,SGRAM,GDDR3,32MX32,1000MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_SAMSUNG
333S0535	4	IC,SDRAM,GDDR3,32MX32,1000MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_HYNIX

Development BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-1404	1	K18 MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM

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PAGE TITLE: BOM Configuration

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Functional Test Points

J5650 (LEFT FAN CONN)

FUNC_TEST

TRUE	PP5V_S0	70 72 86 88 8 7 29 42 47 52 54 68 76	3 TPs per Fan
TRUE	FAN_LT_PWM	52	
TRUE	FAN_LT_TACH	52	

J5660 (RIGHT FAN CONN)

TRUE	FAN_RT_PWM	52	
TRUE	FAN_RT_TACH	52	
TRUE	GND		5 TPs per Fan

J6780 (MIC CONN)

TRUE	BI_MIC_N	62 63	
TRUE	BI_MIC_SHIELD	62 63	
TRUE	BI_MIC_P	62 63	

J6781 & J6782 (SPEAKERS CONN)

TRUE	SPKRCONN_L_OUT_P	61 62 99
TRUE	SPKRCONN_L_OUT_N	61 62 99
TRUE	SPKRCONN_R_OUT_P	61 62 99
TRUE	SPKRCONN_R_OUT_N	61 62 99
TRUE	SPKRCONN_S_OUT_P	61 62 99
TRUE	SPKRCONN_S_OUT_N	61 62 99

J9000 (LVDS CONN)

TRUE	PP3V3_SW_LCD	84 85 87 88 98 83
TRUE	PP3V3_S0	6 7 51 52 54 59 62 63 68 69 72 77 78 80 81 23 24 25 26
TRUE	PPVOUT_S0_LCDBKLT	27 28 30 31 37 40 42 46 47 48 73 80 83 — 2 TP needed
TRUE	LVDS_DDC_CLK	83 84
TRUE	LVDS_DDC_DATA	83 84
TRUE	LVDS_CONN_A_DATA_P<0>	83 84 98
TRUE	LVDS_CONN_A_DATA_N<0>	83 84 98
TRUE	LVDS_CONN_A_DATA_P<1>	83 84 98
TRUE	LVDS_CONN_A_DATA_N<1>	83 84 98
TRUE	LVDS_CONN_A_DATA_P<2>	83 84 98
TRUE	LVDS_CONN_A_DATA_N<2>	83 84 98
TRUE	LVDS_CONN_A_CLK_F_P	83 98
TRUE	LVDS_CONN_A_CLK_F_N	83 98
TRUE	LVDS_CONN_B_DATA_P<0>	83 84 98
TRUE	LVDS_CONN_B_DATA_N<0>	83 84 98
TRUE	LVDS_CONN_B_DATA_P<1>	83 84 98
TRUE	LVDS_CONN_B_DATA_N<1>	83 84 98
TRUE	LVDS_CONN_B_DATA_P<2>	83 84 98
TRUE	LVDS_CONN_B_DATA_N<2>	83 84 98
TRUE	LVDS_CONN_B_CLK_F_P	83 98
TRUE	LVDS_CONN_B_CLK_F_N	83 98
TRUE	LED_RETURN_1	83 88
TRUE	LED_RETURN_2	83 88
TRUE	LED_RETURN_3	83 88
TRUE	LED_RETURN_4	83 88
TRUE	LED_RETURN_5	83 88
TRUE	LED_RESET	83 88
TRUE	GND	— 4 TPs

J4500 (SATA ODD CONN)

TRUE	PP5V_SW_ODD	42 56	3 TPs
TRUE	SMC_ODD_DETECT	42 45	
TRUE	SATA_ODD_D2R_C_P	42 93	
TRUE	SATA_ODD_D2R_C_N	42 93	
TRUE	SATA_ODD_R2D_P	42 93	
TRUE	SATA_ODD_R2D_N	42 93	
TRUE	GND		5 TPs

J4501 (SATA HDD CONN)

TRUE	PP5V_S0_HDD_FLT	42
TRUE	SATA_HDD_R2D_P	42 93
TRUE	SATA_HDD_R2D_N	42 93
TRUE	SATA_HDD_D2R_C_N	42 93
TRUE	SATA_HDD_D2R_C_P	42 93
TRUE	GND	

J5815 (KBD BACKLIGHT CONN)

TRUE	KBDLED_ANODE	54
TRUE	SMC_KDBLED_PRESENT_L	54
TRUE	GND	

FUNC_TEST

TRUE	GND
TRUE	GND — 6 TPs

USB PORTS

TRUE	PP5V_S3_RTUSB_A_F	43	
TRUE	USB2_LT1_N	43 99	
TRUE	USB2_LT1_P	43 99	
TRUE	GND		
TRUE	PP5V_S3_RTUSB_B_F	43	
TRUE	USB_LT2_N	43 99	
TRUE	USB_LT2_P	43 99	
TRUE	GND		

J3401 & J3402 (AIRPORT/BT/CAMERA CONN)

TRUE	PCIE_AP_D2R_P	17 33 94
TRUE	PCIE_AP_D2R_N	17 33 94
TRUE	PCIE_AP_R2D_P	33 94
TRUE	PCIE_AP_R2D_N	33 94
TRUE	PCIE_CLK100M_AP_CONN_P	33 94
TRUE	PCIE_CLK100M_AP_CONN_N	33 94
TRUE	AP_CLKREQ_O_L	33
TRUE	PCIE_WAKE_L	18 27 33
TRUE	AP_RESET_CONN_L	33
TRUE	PP3V3_WLAN	33
TRUE	PP5V_S3_ALSCAMERA_F	33
TRUE	SMBUS_SMC_A_S3_SDA	6 33 45 48 54 97
TRUE	SMBUS_SMC_A_S3_SCL	6 33 45 48 54 97
TRUE	USB_CAMERA_CONN_P	33 93
TRUE	USB_CAMERA_CONN_N	33 93
TRUE	CONN_USB2_BT_P	33 99
TRUE	CONN_USB2_BT_N	33 99

J3500 (SD CARD CONN)

TRUE	SD_D<7..0>	34
TRUE	SD_CMD	34
TRUE	SD_CLK	34
TRUE	SD_CD_L	34 37
TRUE	SD_WP	34 37
TRUE	GND	— 2 TPs

J5713 (KEY BOARD CONN)

TRUE	PP3V3_S3	25 72 87 101
TRUE	PP3V42_G3H	6 7 21 23 25 26 27 28 30 31 33 34 35 36 48 50 53 54 64 65 72 73
TRUE	WS_KBD1	7 17 21 23 43 46 47 48 49 53 64 65 66 73
TRUE	WS_KBD2	53
TRUE	WS_KBD3	53
TRUE	WS_KBD4	53
TRUE	WS_KBD5	53
TRUE	WS_KBD6	53
TRUE	WS_KBD7	53
TRUE	WS_KBD8	53
TRUE	WS_KBD9	53
TRUE	WS_KBD10	53
TRUE	WS_KBD11	53
TRUE	WS_KBD12	53
TRUE	WS_KBD13	53
TRUE	WS_KBD14	53
TRUE	WS_KBD15_CAP	53
TRUE	WS_KBD16_NUM	53
TRUE	WS_KBD17	53
TRUE	WS_KBD18	53
TRUE	WS_KBD19	53
TRUE	WS_KBD20	53
TRUE	WS_KBD21	53
TRUE	WS_KBD22	53
TRUE	WS_KBD23	53
TRUE	WS_KBD_ONOFF_L	53
TRUE	WS_LEFT_SHIFT_KBD	53
TRUE	WS_LEFT_OPTION_KBD	53
TRUE	WS_CONTROL_KBD	53

J6950 (BIL CABLE CONN)

TRUE	PP5V_S3_IR_R	42
TRUE	SMC_LID_R	64
TRUE	IR_RX_OUT	42 44
TRUE	SYS_LED_ANODE	42 46
TRUE	GND	

J5800 (IPD FLEX CONN)

TRUE	PP18V5_S3	6 54
TRUE	Z2_CS_L	53 54
TRUE	Z2_DEBUG3	53 54
TRUE	Z2_MISO	53 54
TRUE	Z2_BOOST_EN	54
TRUE	Z2_SCLK	53 54
TRUE	Z2_CLKIN	53 54
TRUE	Z2_KEY_ACT_L	53 54
TRUE	Z2_RESET	53 54
TRUE	PSOC_F_CS_L	53 54
TRUE	PICKB_L	53 54
TRUE	PSOC_MISO	53 54
TRUE	PSOC_MOSI	53 54
TRUE	PSOC_SCLK	53 54
TRUE	SMBUS_SMC_A_S3_SCL	6 33 45 48 54 97
TRUE	SMBUS_SMC_A_S3_SDA	6 33 45 48 54 97

J6900 (DC POWER CONN)

TRUE	ADAPTER_SENSE	64
TRUE	PP18V5_DCIN_FUSE	64
TRUE	GND	

J6950 (MAIN BATT CONN)

TRUE	PPVBAT_G3H_CONN	64 65
TRUE	SMBUS_SMC_BSA_SCL	6 45 48 64 65 97
TRUE	SMBUS_SMC_BSA_SDA	6 45 48 64 65 97
TRUE	NC_SMC_BS_ALRT_L	6
TRUE	GND	

J6995 (BAT LED CONN)

TRUE	PP3V42_G3H	73 64 65 66 48 49 53 7 21 23 43 46 47 17 6 65 97
TRUE	SMBUS_SMC_BSA_SDA	6 45 48 64 65 97
TRUE	SMBUS_SMC_BSA_SCL	6 45 48 64 65 97
TRUE	SMC_BIL_BUTTON_L	45 46 64
TRUE	GND	

FUNC_TEST

TRUE	BKLT_EN	88
TRUE	TP_ISSP_SCLK_P1_1	8 53
TRUE	TP_ISSP_SDATA_P1_0	8 53
TRUE	LCD_BKLT_PWM	87 88
TRUE	LPCPLUS_GPIO	20 47
TRUE	LPCPLUS_RESET_L	27 47 87 94
TRUE	LPC_AD<0..3>	17 45 47 87 94
TRUE	LPC_CLK33M_LPCPLUS	27 47 94
TRUE	LPC_FRAME_L	17 45 47 87 94
TRUE	LPC_PWRDWN_L	18 45 47
TRUE	LPC_SERIRQ	17 45 47
TRUE	PM_CLKRUN_L	18 45 47
TRUE	PM_SYSRST_L	18 27 45
TRUE	SMC_MD1	45 47
TRUE	SMC_NMI	45 47
TRUE	SMC_ONOFF_L	45 46 53
TRUE	SMC_RESET_L	45 46 47 65
TRUE	SMC_RX_L	43 45 46 47
TRUE	SMC_TCK	45 46 47
TRUE	SMC_TDI	45 46 47
TRUE	SMC_TDO	45 46 47
TRUE	SMC_TMS	45 46 47
TRUE	SMC_TRST_L	45 47
TRUE	SMC_TX_L	43 45 46 47
TRUE	SPIROM_USE_MLB	20 47 57
TRUE	SPI_ALT_CLK	47
TRUE	SPI_ALT_CS_L	47
TRUE	SPI_ALT_MISO	47
TRUE	SPI_ALT_MOSI	47
TRUE	SYS_LED_ANODE_R	42

POWER RAILS

FUNC_TEST

TRUE	PM_SLP_S3_L	18 31 45 73 85
TRUE	PP0V75_S0_DDRVTT	7 28 30 31 67
TRUE	PP18V5_S3	6 54
TRUE	PP1V05_S0	7 19 12 13 15 17 18 20 21 23 24 25 26 30 40 73 76 86
TRUE	PP1V05_S0GPU	7 74 76 79 81 86
TRUE	PP1V05_S5	7 17 71
TRUE	PP1V0_FW_FWPHY	7 39 40
TRUE	PP1V2_ENET	7 37 71 72
TRUE	PP1V2_S0	7 72 87
TRUE	PP1V5_S3	7 28 30 31 67 72
TRUE	PP1V5_S3RS0	7 13 16 31 42 72 73 99
TRUE	PP1V8R1V55_S0GPU_ISNS	7 8 50 56 75 76 77 78
TRUE	PP1V8R1V55_S0GPU_ISNS_R	7 50 86
TRUE	PP1V8_GPUIFPX	7 72 81
TRUE	PP1V8_S0	7 12 16 21 23 24 58 71 72 87
TRUE	PP3V3_ENET	7 27 37 73
TRUE	PP3V3_FW_FWPHY	7 39 40 41
TRUE	PP3V3_S0	50 51 52 54 73 83 84 85 87 88 99 6 7 13 14 19 20 21 23 24 25 26 27 28 30 34 37 40 42 46 47 48
TRUE	PP3V3_S0GPU	7 72 74 79 80 81 82 84
TRUE	PP3V3_S3	6 7 21 23 25 31 32 33 34 35 36 48 50 53 54 55 72 73 87 101
TRUE	PP3V3_S5	7 17 18 19 20 22 23 27 31 35 57
TRUE	PP3V3_S5_AVREF_SMC	45 46 66 71 72 73 83 85 99
TRUE	PP3V42_G3H	6 7 17 21 23 43 45 46 47 48 49 53 64 65 66 73
TRUE	PP5V_S0	6 7 23 42 47 52 54 68 69 70 72 86 88
TRUE	PP5V_S3	7 31 33 42 43 44 46 54 56 58 61 66 67 72 82 101
TRUE	PP5V_S5	7 23 66 72
TRUE	PPBUS_G3H	7 40 49 65 66 67 69 70 82 86 89
TRUE	PPDCIN_G3H	7 64 65
TRUE	PPVCORE_GPU	7 49 75 82
TRUE	PPVCORE_S0_CPU	7 12 15 49 68
TRUE	PPVCORE_S0_GFX	7 13 24 49 69
TRUE	PPVP_FW	7 40 41
TRUE	PPVTTDDR_S3	7 32 67

NC NO_TESTs

NO_TEST

17 6	NC_PCIE_PE5_D2RN	TRUE	NC_PCIE_PE5_D2RN 6 17
17 6	NC_PCIE_PE5_D2RP	TRUE	NC_PCIE_PE5_D2RP 6 17
17 6	NC_PCIE_PE5_R2D_CN	TRUE	NC_PCIE_PE5_R2D_CN 6 17
17 6	NC_PCIE_PE5_R2D_CP	TRUE	NC_PCIE_PE5_R2D_CP 6 17
17 6	NC_PCIE_PE6_D2RN	TRUE	NC_PCIE_PE6_D2RN 6 17
17 6	NC_PCIE_PE6_D2RP	TRUE	NC_PCIE_PE6_D2RP 6 17
17 6	NC_PCIE_PE6_R2D_CN	TRUE	NC_PCIE_PE6_R2D_CN 6 17
17 6	NC_PCIE_PE6_R2D_CP	TRUE	NC_PCIE_PE6_R2D_CP 6 17
17 6	NC_PCIE_PE7_D2RN	TRUE	NC_PCIE_PE7_D2RN 6 17
17 6	NC_PCIE_PE7_D2RP	TRUE	NC_PCIE_PE7_D2RP 6 17
17 6	NC_PCIE_PE7_R2D_CN	TRUE	NC_PCIE_PE7_R2D_CN 6 17
17 6	NC_PCIE_PE7_R2D_CP	TRUE	NC_PCIE_PE7_R2D_CP 6 17
17 6	NC_PCIE_PE8_D2RN	TRUE	NC_PCIE_PE8_D2RN 6 17
17 6	NC_PCIE_PE8_D2RP	TRUE	NC_PCIE_PE8_D2RP 6 17
17 6	NC_PCIE_PE8_R2D_CN	TRUE	NC_PCIE_PE8_R2D_CN 6 17
17 6	NC_PCIE_PE8_R2D_CP	TRUE	NC_PCIE_PE8_R2D_CP 6 17

ICT Test Points

CPU NO_TESTs

NO_TEST

9	TP_CPU_RSVD<65..62>	TRUE	NC_TP_CPU_RSVD<65..62>
9	TP_CPU_RSVD<58..45>	TRUE	NC_TP_CPU_RSVD<58..45>
	TP_CPU_RSVD<43..32>	TRUE	NC_TP_CPU_RSVD<43..32> 9
9	TP_CPU_RSVD<27..26>	TRUE	NC_TP_CPU_RSVD<27..26>
9	TP_CPU_RSVD<24..15>	TRUE	NC_TP_CPU_RSVD<24..15>
9	TP_CPU_RSVD<2..1>	TRUE	NC_TP_CPU_RSVD<2..1>
	TP_CPU_RSVD_NCTF<8..5>	TRUE	NC_TP_CPU_RSVD_NCTF<8..5> 9

NC NO_TESTs

NO_TEST

18 6	NC_CRT_IG_BLUE	TRUE	NC_CRT_IG_BLUE 6 18
18 6	NC_CRT_IG_GREEN	TRUE	NC_CRT_IG_GREEN 6 18
18 6	NC_CRT_IG_RED	TRUE	NC_CRT_IG_RED 6 18
18 6	NC_CRT_IG_DDC_CLK	TRUE	NC_CRT_IG_DDC_CLK 6 18
18 6	NC_CRT_IG_DDC_DATA	TRUE	NC_CRT_IG_DDC_DATA 6 18
18 6	NC_CRT_IG_HSYNC	TRUE	NC_CRT_IG_HSYNC 6 18
18 6	NC_CRT_IG_VSYNC	TRUE	NC_CRT_IG_VSYNC 6 18
18 6	NC_LVDS_IG_CTRL_CLK	TRUE	NC_LVDS_IG_CTRL_CLK 6 18
18 6	NC_LVDS_IG_CTRL_DATA	TRUE	NC_LVDS_IG_CTRL_DATA 6 18
18 6	NC_PCH_LVDS_VBG	TRUE	NC_PCH_LVDS_VBG 6 18
17 6	NC_HDA_SDIN1	TRUE	NC_HDA_SDIN1 6 17
17 6	NC_HDA_SDIN2	TRUE	NC_HDA_SDIN2 6 17
17 6	NC_HDA_SDIN3	TRUE	NC_HDA_SDIN3 6 17

NC NO_TESTs

NO_TEST

	TP_PCI_AD<31..0>	TRUE	NC_PCI_AD<31..0> 19
	TP_PCI_C_BE_L<3..0>	TRUE	NC_PCI_C_BE_L<3..0> 19
19 6	NC_PCI_GNT3_L	TRUE	NC_PCI_GNT3_L 6 19
19 6	NC_PCI_GNT2_L	TRUE	NC_PCI_GNT2_L 6 19
19 6	NC_PCI_GNT1_L	TRUE	NC_PCI_GNT1_L 6 19
19 6	NC_PCI_GNT0_L	TRUE	NC_PCI_GNT0_L 6 19
19 6	NC_PCI_PAR	TRUE	NC_PCI_PAR 6 19
19 6	NC_PCI_RESET_L	TRUE	NC_PCI_RESET_L 6 19
19 6	NC_PCI_PME_L	TRUE	NC_PCI_PME_L 6 19
19 6	NC_PCI_CLK33M_OUT3	TRUE	NC_PCI_CLK33M_OUT3 6 19
19 6	NC_PCH_NV_RCOMP	TRUE	NC_PCH_NV_RCOMP 6 19
	TP_NV_DQ<15..0>	TRUE	NC_NV_DQ<15..0> 19
	TP_NV_DQS<1..0>	TRUE	NC_NV_DQS<1..0> 19
	TP_NV_CE_L<3..0>	TRUE	NC_NV_CE_L<3..0> 19
19 6	NC_NV_ALE	TRUE	NC_NV_ALE 6 19
19 6	NC_NV_CLE	TRUE	NC_NV_CLE 6 19
19 6	NC_NV_RB_L	TRUE	NC_NV_RB_L 6 19
	TP_NV_WR_RE_L<1..0>	TRUE	NC_NV_WR_RE_L<1..0> 19
	TP_NV_WE_CK_L<1..0>	TRUE	NC_NV_WE_CK_L<1..0> 19
17 6	NC_PCIE_CLK100M_PE4N	TRUE	NC_PCIE_CLK100M_PE4N 6 17
17 6	NC_PCIE_CLK100M_PE4P	TRUE	NC_PCIE_CLK100M_PE4P 6 17
17 6	NC_PCIE_CLK100M_PE5N	TRUE	NC_PCIE_CLK100M_PE5N 6 17
17 6	NC_PCIE_CLK100M_PE5P	TRUE	NC_PCIE_CLK100M_PE5P 6 17
20 6	NC_PCIE_CLK100M_PE6N	TRUE	NC_PCIE_CLK100M_PE6N 6 20
20 6	NC_PCIE_CLK100M_PE6P	TRUE	NC_PCIE_CLK100M_PE6P 6 20
20 6	NC_PCIE_CLK100M_PE7N	TRUE	NC_PCIE_CLK100M_PE7N 6 20
20 6	NC_PCIE_CLK100M_PE7P	TRUE	NC_PCIE_CLK100M_PE7P 6 20
53 6	NC_PSOC_P1_3	TRUE	NC_PSOC_P1_3 6 53
17 6	NC_SATA_C_D2RN	TRUE	NC_SATA_C_D2RN 6 17
17 6	NC_SATA_C_D2RP	TRUE	NC_SATA_C_D2RP 6 17
17 6	NC_SATA_C_R2D_CN	TRUE	NC_SATA_C_R2D_CN 6 17
17 6	NC_SATA_C_R2D_CP	TRUE	NC_SATA_C_R2D_CP 6 17
17 6	NC_SATA_D_D2RN	TRUE	NC_SATA_D_D2RN 6 17
17 6	NC_SATA_D_D2RP	TRUE	NC_SATA_D_D2RP 6 17
17 6	NC_SATA_D_R2D_CN	TRUE	NC_SATA_D_R2D_CN 6 17
17 6	NC_SATA_D_R2D_CP	TRUE	NC_SATA_D_R2D_CP 6 17
17 6	NC_SATA_SSD2_D2RN	TRUE	NC_SATA_SSD2_D2RN 6 17
17 6	NC_SATA_SSD2_D2RP	TRUE	NC_SATA_SSD2_D2RP 6 17
17 6	NC_SATA_SSD2_R2D_CN	TRUE	NC_SATA_SSD2_R2D_CN 6 17
17 6	NC_SATA_SSD2_R2D_CP	TRUE	NC_SATA_SSD2_R2D_CP 6 17
46 45	TP_SMC_P41	TRUE	NC_SMC_P41

NC NO_TESTs

NO_TEST

39 6	NC_FW643_AVREG	TRUE	NC_FW643_AVREG 6 39
39 6	NC_FW643_TDI	TRUE	NC_FW643_TDI 6 39
18 6	NC_DP_IG_C_HPD	TRUE	NC_DP_IG_C_HPD 6 18
18 6	NC_DP_IG_C_CTRL_CLK	TRUE	NC_DP_IG_C_CTRL_CLK 6 18
18 6	NC_DP_IG_C_CTRL_DATA	TRUE	NC_DP_IG_C_CTRL_DATA 6 18
	TP_DP_IG_C_MLP<3..0>	TRUE	NC_DP_IG_C_MLP<3..0> 18
	TP_DP_IG_C_MLN<3..0>	TRUE	NC_DP_IG_C_MLN<3..0> 18
18 6	NC_DP_IG_C_AUXP	TRUE	NC_DP_IG_C_AUXP 6 18
18 6	NC_DP_IG_C_AUXN	TRUE	NC_DP_IG_C_AUXN 6 18
18 6	NC_DP_IG_D_HPD	TRUE	NC_DP_IG_D_HPD 6 18
18 6	NC_DP_IG_D_CTRL_CLK	TRUE	NC_DP_IG_D_CTRL_CLK 6 18
18 6	NC_DP_IG_D_CTRL_DATA	TRUE	NC_DP_IG_D_CTRL_DATA 6 18
	TP_DP_IG_D_MLP<3..0>	TRUE	NC_DP_IG_D_MLP<3..0> 18
	TP_DP_IG_D_MLN<3..0>	TRUE	NC_DP_IG_D_MLN<3..0> 18
18 6	NC_DP_IG_D_AUXP	TRUE	NC_DP_IG_D_AUXP 6 18
18 6	NC_DP_IG_D_AUXN	TRUE	NC_DP_IG_D_AUXN 6 18
18 6	NC_SDVO_TVCLKINN	TRUE	NC_SDVO_TVCLKINN 6 18
18 6	NC_SDVO_TVCLKINP	TRUE	NC_SDVO_TVCLKINP 6 18
18 6	NC_SDVO_STALLN	TRUE	NC_SDVO_STALLN 6 18
18 6	NC_SDVO_STALLP	TRUE	NC_SDVO_STALLP 6 18
18 6	NC_SDVO_INTN	TRUE	NC_SDVO_INTN 6 18
18 6	NC_SDVO_INTP	TRUE	NC_SDVO_INTP 6 18
74 6	NC_GPU_BUFRST_L	TRUE	NC_GPU_BUFRST_L 6 74
80 79	TP_GPU_GSTATE<0>	TRUE	NC_GPU_GSTATE<0>
80	TP_GPU_GSTATE<1>	TRUE	NC_GPU_GSTATE<1>
80 79	TP_GPU_MIOA_D<9..0>	TRUE	NC_GPU_MIOA_D<9..0>
80 79	TP_GPU_MIOA_DE	TRUE	NC_GPU_MIOA_DE
6	NC_LVDS_EG_BKL_PWM	TRUE	NC_LVDS_EG_BKL_PWM 6
93 18 8	TP_LVDS_IG_B_CLKN	TRUE	NC_LVDS_IG_B_CLKN
93 18 8	TP_LVDS_IG_B_CLKP	TRUE	NC_LVDS_IG_B_CLKP
93 18 8	TP_LVDS_IG_BKL_PWM	TRUE	NC_LVDS_IG_BKL_PWM
6	NC_SMC_BS_ALRT_L	TRUE	NC_SMC_BS_ALRT_L 6
20 6	NC_PCH_SST	TRUE	NC_PCH_SST 6 20
20 6	NC_PCH_NC1	TRUE	NC_PCH_NC1 6 20
20 6	NC_PCH_NC2	TRUE	NC_PCH_NC2 6 20
20 6	NC_PCH_NC3	TRUE	NC_PCH_NC3 6 20
20 6	NC_PCH_NC4	TRUE	NC_PCH_NC4 6 20
20 6	NC_PCH_NC5	TRUE	NC_PCH_NC5 6 20
20 6	NC_PCH_TP19	TRUE	NC_PCH_TP19 6 20
20 6	NC_PCH_TP18	TRUE	NC_PCH_TP18 6 20
20 6	NC_PCH_TP17	TRUE	NC_PCH_TP17 6 20
20 6	NC_PCH_TP16	TRUE	NC_PCH_TP16 6 20
20 6	NC_PCH_TP15	TRUE	NC_PCH_TP15 6 20
20 6	NC_PCH_TP14	TRUE	NC_PCH_TP14 6 20
20 6	NC_PCH_TP13	TRUE	NC_PCH_TP13 6 20
20 6	NC_PCH_TP12	TRUE	NC_PCH_TP12 6 20
20 6	NC_PCH_TP11	TRUE	NC_PCH_TP11 6 20
20 6	NC_PCH_TP10	TRUE	NC_PCH_TP10 6 20
20 6	NC_PCH_TP9	TRUE	NC_PCH_TP9 6 20
20 6	NC_PCH_TP8	TRUE	NC_PCH_TP8 6 20
20 6	NC_PCH_TP7	TRUE	NC_PCH_TP7 6 20
20 6	NC_PCH_TP6	TRUE	NC_PCH_TP6 6 20
20 6	NC_PCH_TP5	TRUE	NC_PCH_TP5 6 20
20 6	NC_PCH_TP4	TRUE	NC_PCH_TP4 6 20
20 6	NC_PCH_TP3	TRUE	NC_PCH_TP3 6 20
20 6	NC_PCH_TP2	TRUE	NC_PCH_TP2 6 20
20 6	NC_PCH_TP1	TRUE	NC_PCH_TP1 6 20
17 6	NC_CLINK_CLK	TRUE	NC_CLINK_CLK 6 17
17 6	NC_CLINK_DATA	TRUE	NC_CLINK_DATA 6 17
17 6	NC_CLINK_RESET_L	TRUE	NC_CLINK_RESET_L 6 17
17 6	NC_PCIE_CLK100M_PEBN	TRUE	NC_PCIE_CLK100M_PEBN 6 17
17 6	NC_PCIE_CLK100M_PEBP	TRUE	NC_PCIE_CLK100M_PEBP 6 17

TP38	TRUE	PCH_VSS_NCTF<1>	20 94
TP43	TRUE	PCH_VSS_NCTF<2>	20 94
TP44	TRUE	PCH_VSS_NCTF<5>	20 94
TP45	TRUE	PCH_VSS_NCTF<7>	
TP46	TRUE	PCH_VSS_NCTF<9>	20 94
TP47	TRUE	PCH_VSS_NCTF<11>	20 94
TP48	TRUE	PCH_VSS_NCTF<12>	20 94
TP49	TRUE	PCH_VSS_NCTF<15>	20 94
TP50	TRUE	PCH_VSS_NCTF<17>	20 94
TP51	TRUE	PCH_VSS_NCTF<19>	6 20 94
TP52	TRUE	PCH_VSS_NCTF<19>	6 20 94
TP53	TRUE	PCH_VSS_NCTF<21>	20 94
TP54	TRUE	PCH_VSS_NCTF<25>	20 94
TP55	TRUE	PCH_VSS_NCTF<27>	20 94
TP56	TRUE	PCH_VSS_NCTF<29>	20 94

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

Functional / ICT Test

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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"G3Hot" (Always-Present) Rails

PPBUS_G3H
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=12.6V
MAKE_BASE=TRUE

PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H

PPBUS_CPU_IMVP_ISNS
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=12.6V
MAKE_BASE=TRUE

PPBUS_CPU_IMVP_ISNS

PPDCIN_G3H
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18V
MAKE_BASE=TRUE

PPDCIN_G3H

PP3V42_G3H
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE

PP3V42_G3H ×16

5V Rails

PP5V_S5
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S5 ×3

PP5V_S3
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S3 ×20

PP5V_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S0 ×20

3.3V Rails

PP3V_S5
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.4V
MAKE_BASE=TRUE

PP3V_S5 ×40

PP3V_S3
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.4V
MAKE_BASE=TRUE

PP3V_S3 ×40

PP3V_S0
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.4V
MAKE_BASE=TRUE

PP3V_S0 ×40

PP1V8_S0 — 2A max supply

PP1V8_S0 ×10

PP1V5_S3
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.17 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE

PP1V5_S3 ×6

PP1V5_S3RS0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE

PP1V5_S3RS0 ×4

PPVTTDDR_S3
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.75V
MAKE_BASE=TRUE

PPVTTDDR_S3

PP0V75_S0_DDRVTT
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE

PP0V75_S0_DDRVTT ×4

PP1V2_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.09 MM
VOLTAGE=1.2V
MAKE_BASE=TRUE

PP1V2_S0 ×2

PP1V05_S5
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

PP1V05_S5

PP1V05_S0 — ? mA
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

PP1V05_S0 ×16

PP3V3_ENET
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_ENET ×2

PP1V2_ENET
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.2V
MAKE_BASE=TRUE

PP1V2_ENET ×2

1.8V/1.5V/1.2V/1.05V Rails

ENET Rails

"FW" (FireWire) Rails

PPVP_FW
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=12.6V
MAKE_BASE=TRUE

PPVP_FW ×2

PP3V3_FW_FWPHY
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_FW_FWPHY ×3

PP1V0_FW_FWPHY
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.0V
MAKE_BASE=TRUE

PP1V0_FW_FWPHY ×2

"GPU" Rails

PP3V3_S0GPU
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.10MM
VOLTAGE=3V
MAKE_BASE=TRUE

PP3V3_S0GPU ×5

PP1V8_GPUIFPX
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.15 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE

PP1V8_GPUIFPX ×2

PP1V8R1V55_S0GPU_ISNS
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE

PP1V8R1V55_S0GPU_ISNS ×4

PP1V8R1V55_S0GPU_ISNS_R
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE

PP1V8R1V55_S0GPU_ISNS_R

PP1V05_S0GPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

PP1V05_S0GPU ×12

PPVCORE_GPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

PPVCORE_GPU

Chipset "VCore" Rails

PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE

PPVCORE_S0_CPU

PPVCORE_S0_GFX
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

PPVCORE_S0_GFX

PPVCORE_S0_CPU_VCAP0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE

PPVCORE_S0_CPU_VCAP0

PPVCORE_S0_CPU_VCAP1
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE

PPVCORE_S0_CPU_VCAP1

PPVCORE_S0_CPU_VCAP2
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE

PPVCORE_S0_CPU_VCAP2

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
Power Aliases

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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Thermal Module Holes

ZT0984 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0987 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0980 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0981 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0985 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0986 STDOFF-4.50D.98H-1.1-3.48-TH

Fan Holes

ZT0930 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0988 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0989 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0991 STDOFF-4.50D.98H-1.1-3.48-TH

Frame Holes

ZT0915 3R2P5 — GND
ZT0940 3R2P5 — GND
ZT0950 TH — GND
SL-3.1X2.7-6CIR-NSP
ZT0960 3R2P5 — GND
ZT0990 3R2P5 — GND

Left Speaker Holes

ZT0934 STDOFF-4.0OD3.0H-TH
ZT0935 STDOFF-4.0OD3.0H-TH

Keyboard / IPD Conn Protect

ZT0952 4.0OD1.85H-M1.6X0.35
ZT0953 4.0OD1.85H-M1.6X0.35

Tall EMI pogo pins

SH0902 2.0DIA-TALL-EMI-MLB-M97-M98 SM
SH0903 2.0DIA-TALL-EMI-MLB-M97-M98 SM
SH0904 2.0DIA-TALL-EMI-MLB-M97-M98 SM
SH0900 2.0DIA-TALL-EMI-MLB-M97-M98 SM
SH0916 2.0DIA-TALL-EMI-MLB-M97-M98 SM

Short (IO Row) EMI pogo pins

SH0910 1.4DIA-SHORT-EMI-MLB-M97-M98 SM
SH0911 1.4DIA-SHORT-EMI-MLB-M97-M98 SM
SH0912 1.4DIA-SHORT-EMI-MLB-M97-M98 SM
SH0913 1.4DIA-SHORT-EMI-MLB-M97-M98 SM
SH0901 1.4DIA-SHORT-EMI-MLB-M97-M98 SM
SH0917 1.4DIA-SHORT-EMI-MLB-M97-M98 SM
SH0914 1.4DIA-SHORT-EMI-MLB-M97-M98 SM
GND_CHASSIS_AUDIO_JACK

GMUX ALIASES

PM_ALL_GPU_PGOOD — PM_ALL_GPU_PGOOD
TP_LVDS_MUX_SEL_EG — TP_LVDS_MUX_SEL_EG
EG_RESET_L — EG_RESET_L
LVDS_IG_BKL_ON — LVDS_IG_BKL_ON
LVDS_IG_PANEL_PWR — LVDS_IG_PANEL_PWR
LCD_BKLT_EN — LCD_BKLT_EN

PEX_CLKREQ_L — PEX_CLKREQ_L
PEG_CLKREQ_L — PEG_CLKREQ_L

PM_ENET_EN — PM_ENET_EN

FW_PLUG_DET_L — FW_PLUG_DET_L
FW643_WAKE_L — FW643_WAKE_L

TP_SMC_EXCARD_PWR_EN — TP_SMC_EXCARD_PWR_EN
NC_SATA_EXTA_D2R_N — NC_SATA_EXTA_D2R_N
NC_SATA_EXTA_D2R_P — NC_SATA_EXTA_D2R_P
NC_SATA_EXTA_R2D_C_N — NC_SATA_EXTA_R2D_C_N
NC_SATA_EXTA_R2D_C_P — NC_SATA_EXTA_R2D_C_P
NC_PCIE_EXCARD_D2R_N — NC_PCIE_EXCARD_D2R_N
NC_PCIE_EXCARD_D2R_P — NC_PCIE_EXCARD_D2R_P
NC_PCIE_EXCARD_R2D_C_N — NC_PCIE_EXCARD_R2D_C_N
NC_PCIE_EXCARD_R2D_C_P — NC_PCIE_EXCARD_R2D_C_P
NC_PCIE_CLK100M_EXCARD_N — NC_PCIE_CLK100M_EXCARD_N
NC_PCIE_CLK100M_EXCARD_P — NC_PCIE_CLK100M_EXCARD_P

TP_ISSP_SCLK_P1_1 — TP_ISSP_SCLK_P1_1
TP_ISSP_SDATA_P1_0 — TP_ISSP_SDATA_P1_0

GND
GND
GND
GND
GND

CPU signals

CPU_VID<0..6> — CPUIMVP_VID<0..6>
GFX_VID<0..6> — GFXIMVP_VID<0..6>
MEMVTT_EN — MEMVTT_EN

TP_CPU_VTT_SELECT — TP_CPU_VTT_SELECT

GPU signals

PEG_D2R_P<15..0> — =PEG_D2R_P<0..15>
PEG_D2R_N<15..0> — =PEG_D2R_N<0..15>
PEG_R2D_C_P<15..0> — =PEG_R2D_C_P<0..15>
PEG_R2D_C_N<15..0> — =PEG_R2D_C_N<0..15>

** PEG LANES REVERSED. ARD STRAP REQ'D. **

CPU_CFG<3> — R0902 3.0K 5% 1/16W MF-LF 402

TP_LVDS_IG_B_CLKP — TP_LVDS_IG_B_CLKP
TP_LVDS_IG_B_CLKN — TP_LVDS_IG_B_CLKN
TP_LVDS_IG_BKL_PWM — TP_LVDS_IG_BKL_PWM
NC_GPU_XTALOUT — NC_GPU_XTALOUT
NC_LVDS_IG_A_DATAP<3> — NC_LVDS_IG_A_DATAP<3>
NC_LVDS_IG_A_DATAN<3> — NC_LVDS_IG_A_DATAN<3>
NC_LVDS_IG_B_DATAP<3> — NC_LVDS_IG_B_DATAP<3>
NC_LVDS_IG_B_DATAN<3> — NC_LVDS_IG_B_DATAN<3>

DP_IG_ML_P<3..0> — DP_IG_B_ML_P<3..0>
DP_IG_ML_N<3..0> — DP_IG_B_ML_N<3..0>
DP_IG_AUX_CH_P — DP_IG_AUX_CH_P
DP_IG_AUX_CH_N — DP_IG_AUX_CH_N
DP_IG_DDC_CLK — DP_IG_DDC_CLK
DP_IG_DDC_DATA — DP_IG_DDC_DATA
DP_IG_HPD — DP_IG_HPD

NC_USB_HUB1_OCS4 — NC_USB_HUB1_OCS4
NC_USB_HUB2_OCS3 — NC_USB_HUB2_OCS3
USB_SDCARD_P — USB_SDCARD_P
USB_SDCARD_N — USB_SDCARD_N

PP3V3_S3 — R0903 10K 5% 1/16W MF-LF 402 — R0904 10K 5% 1/16W MF-LF 402 — USB_EXTC_N / USB_EXTC_P

PP1V8R1V55_S0GPU_ISNS — R0900 10 1% 1/16W MF-LF 402 — GPU_FB_A_VREF_DIV
R0901 10 1% 1/16W MF-LF 402 — GPU_FB_B_VREF_DIV

Digital Ground

GND
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.095 mm
VOLTAGE=0V

SYNC_MASTER=K17_REF SYNC_DATE=06/11/2009

PAGE TITLE: Signal Aliases

Apple Inc.

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OMIT

U1000
ARRANDALE
BGA
(SYM 1 OF 11)

DMI

DMI_S2N N<0>	F7	DMI_RX0*
DMI_S2N N<1>	J8	DMI_RX1*
DMI_S2N N<2>	K8	DMI_RX2*
DMI_S2N N<3>	J4	DMI_RX3*
DMI_S2N P<0>	F9	DMI_RX0
DMI_S2N P<1>	J6	DMI_RX1
DMI_S2N P<2>	K9	DMI_RX2
DMI_S2N P<3>	J2	DMI_RX3
DMI_N2S N<0>	H17	DMI_TX0*
DMI_N2S N<1>	K15	DMI_TX1*
DMI_N2S N<2>	J13	DMI_TX2*
DMI_N2S N<3>	F16	DMI_TX3*
DMI_N2S P<0>	G17	DMI_TX0
DMI_N2S P<1>	M15	DMI_TX1
DMI_N2S P<2>	G13	DMI_TX2
DMI_N2S P<3>	J11	DMI_TX3

FLEXIBLE DISPLAY INTERFACE

FDI_DATA_N<0>	L2	FDI_TX0*
FDI_DATA_N<1>	N7	FDI_TX1*
FDI_DATA_N<2>	M4	FDI_TX2*
FDI_DATA_N<3>	P1	FDI_TX3*
FDI_DATA_N<4>	N10	FDI_TX4*
FDI_DATA_N<5>	R7	FDI_TX5*
FDI_DATA_N<6>	U7	FDI_TX6*
FDI_DATA_N<7>	W8	FDI_TX7*
FDI_DATA_P<0>	K1	FDI_TX0
FDI_DATA_P<1>	N5	FDI_TX1
FDI_DATA_P<2>	N2	FDI_TX2
FDI_DATA_P<3>	R2	FDI_TX3
FDI_DATA_P<4>	N9	FDI_TX4
FDI_DATA_P<5>	R8	FDI_TX5
FDI_DATA_P<6>	U6	FDI_TX6
FDI_DATA_P<7>	W10	FDI_TX7
FDI_FSYNC<0>	AC7	FDI_FSYNC0
FDI_FSYNC<1>	AC9	FDI_FSYNC1
FDI_INT	AB5	FDI_INT
FDI_LSYNC<0>	AA1	FDI_LSYNC0
FDI_LSYNC<1>	AB2	FDI_LSYNC1

PCI EXPRESS -- GRAPHICS

PEG_ICOMPI	B12	
PEG_ICOMPO	A13	
PEG_RCOMPO	D12	
PEG_RBIAS	B11	CPU_PEG_RBIAS

CPU_PEG_COMP

R1012 750 1% 1/16W MF-LF 402
R1010 49.9 1% 1/16W MF-LF 402

PEG_RX0*	G40	=PEG_D2R_N<0>
PEG_RX1*	G38	=PEG_D2R_N<1>
PEG_RX2*	H34	=PEG_D2R_N<2>
PEG_RX3*	P34	=PEG_D2R_N<3>
PEG_RX4*	G28	=PEG_D2R_N<4>
PEG_RX5*	H25	=PEG_D2R_N<5>
PEG_RX6*	H24	=PEG_D2R_N<6>
PEG_RX7*	D29	=PEG_D2R_N<7>
PEG_RX8*	B26	=PEG_D2R_N<8>
PEG_RX9*	D26	=PEG_D2R_N<9>
PEG_RX10*	B23	=PEG_D2R_N<10>
PEG_RX11*	D22	=PEG_D2R_N<11>
PEG_RX12*	A20	=PEG_D2R_N<12>
PEG_RX13*	D19	=PEG_D2R_N<13>
PEG_RX14*	A17	=PEG_D2R_N<14>
PEG_RX15*	B14	=PEG_D2R_N<15>
PEG_RX0	F40	PEG_D2R_P<15>
PEG_RX1	J38	PEG_D2R_P<14>
PEG_RX2	G34	PEG_D2R_P<13>
PEG_RX3	M34	PEG_D2R_P<12>
PEG_RX4	J28	PEG_D2R_P<11>
PEG_RX5	G25	PEG_D2R_P<10>
PEG_RX6	K24	PEG_D2R_P<9>
PEG_RX7	B28	PEG_D2R_P<8>
PEG_RX8	A27	PEG_D2R_P<7>
PEG_RX9	B25	PEG_D2R_P<6>
PEG_RX10	A24	PEG_D2R_P<5>
PEG_RX11	B21	PEG_D2R_P<4>
PEG_RX12	B19	PEG_D2R_P<3>
PEG_RX13	B18	PEG_D2R_P<2>
PEG_RX14	B16	PEG_D2R_P<1>
PEG_RX15	D15	PEG_D2R_P<0>

Embedded DisplayPort (eDP) pins (Auburndale only):

eDP_AUX#

NOTE: HPD must be inverted and level-shifted for Auburndale (1.05V).

eDP_HPD#
eDP_AUX

PEG_TX0*	N40	=PEG_R2D_C_N<0>
PEG_TX1*	L38	=PEG_R2D_C_N<1>
PEG_TX2*	M32	=PEG_R2D_C_N<2>
PEG_TX3*	D40	=PEG_R2D_C_N<3>
PEG_TX4*	A38	=PEG_R2D_C_N<4>
PEG_TX5*	G32	=PEG_R2D_C_N<5>
PEG_TX6*	B33	=PEG_R2D_C_N<6>
PEG_TX7*	B35	=PEG_R2D_C_N<7>
PEG_TX8*	L30	=PEG_R2D_C_N<8>
PEG_TX9*	A31	=PEG_R2D_C_N<9>
PEG_TX10*	B32	=PEG_R2D_C_N<10>
PEG_TX11*	L28	=PEG_R2D_C_N<11>
PEG_TX12*	N26	=PEG_R2D_C_N<12>
PEG_TX13*	M24	=PEG_R2D_C_N<13>
PEG_TX14*	G21	=PEG_R2D_C_N<14>
PEG_TX15*	J20	=PEG_R2D_C_N<15>
PEG_TX0	L40	PEG_R2D_C_P<15>
PEG_TX1	N38	PEG_R2D_C_P<14>
PEG_TX2	N32	PEG_R2D_C_P<13>
PEG_TX3	B39	PEG_R2D_C_P<12>
PEG_TX4	B37	PEG_R2D_C_P<11>
PEG_TX5	H32	PEG_R2D_C_P<10>
PEG_TX6	A34	PEG_R2D_C_P<9>
PEG_TX7	D36	PEG_R2D_C_P<8>
PEG_TX8	J30	PEG_R2D_C_P<7>
PEG_TX9	B30	PEG_R2D_C_P<6>
PEG_TX10	D33	PEG_R2D_C_P<5>
PEG_TX11	N28	PEG_R2D_C_P<4>
PEG_TX12	M25	PEG_R2D_C_P<3>
PEG_TX13	N24	PEG_R2D_C_P<2>
PEG_TX14	F21	PEG_R2D_C_P<1>
PEG_TX15	L20	PEG_R2D_C_P<0>

eDP_TX#<3>
eDP_TX#<2>
eDP_TX#<1>
eDP_TX#<0>

eDP_TX<3>
eDP_TX<2>
eDP_TX<1>
eDP_TX<0>

OMIT

U1000
ARRANDALE
BGA
(SYM 5 OF 11)

RESERVED

CPU_CFG<0>	AL4	CFG0 (IPU)
CPU_CFG<1>	AM2	CFG1 (IPU)
CPU_CFG<2>	AK1	CFG2 (IPU)
CPU_CFG<3>	AK2	CFG3 (IPU)
CPU_CFG<4>	AK4	CFG4 (IPU)
CPU_CFG<5>	AJ2	CFG5 (IPU)
CPU_CFG<6>	AT2	CFG6 (IPU)
CPU_CFG<7>	AG7	CFG7 (IPU)
CPU_CFG<8>	AF4	CFG8 (IPU)
CPU_CFG<9>	AG2	CFG9 (IPU)
CPU_CFG<10>	AH1	CFG10 (IPU)
CPU_CFG<11>	AC2	CFG11 (IPU)
CPU_CFG<12>	AC4	CFG12 (IPU)
CPU_CFG<13>	AE2	CFG13 (IPU)
CPU_CFG<14>	AD1	CFG14 (IPU)
CPU_CFG<15>	AF8	CFG15 (IPU)
CPU_CFG<16>	AF6	CFG16 (IPU)
CPU_CFG<17>	AB7	CFG17 (IPU)
TP_CPU_RSVD_TP0	AU1	RSVD_TP0
TP_CPU_RSVD<15>	T4	RSVD15
TP_CPU_RSVD<16>	T2	RSVD16
TP_CPU_RSVD<17>	U1	RSVD17
TP_CPU_RSVD<18>	V2	RSVD18
TP_CPU_RSVD<19>	AV71	RSVD19
TP_CPU_RSVD<20>	AW70	RSVD20
TP_CPU_RSVD<21>	AY69	RSVD21
TP_CPU_RSVD<22>	BB69	RSVD22
TP_CPU_RSVD<23>	D8	RSVD23
TP_CPU_RSVD<24>	B7	RSVD24
TP_CPU_RSVD<26>	A10	RSVD26
TP_CPU_RSVD<27>	B9	RSVD27
NC_TP_CPU_RSVD_NCTF<7>	C5	RSVD_NCTF7
NC_TP_CPU_RSVD_NCTF<8>	A6	RSVD_NCTF8
NC_TP_CPU_RSVD_NCTF<6>	E3	RSVD_NCTF6
NC_TP_CPU_RSVD_NCTF<5>	F1	RSVD_NCTF5

RSVD32	W66	NC_TP_CPU_RSVD<32>
RSVD33	W64	NC_TP_CPU_RSVD<33>
RSVD34	AC69	NC_TP_CPU_RSVD<34>
RSVD35	AC71	NC_TP_CPU_RSVD<35>
RSVD36	AA71	NC_TP_CPU_RSVD<36>
RSVD37	AA69	NC_TP_CPU_RSVD<37>
RSVD38	R66	NC_TP_CPU_RSVD<38>
RSVD39	R64	NC_TP_CPU_RSVD<39>
RSVD_NCTF3	BT5	NC_TP_CPU_RSVD<40>
RSVD_NCTF4	BR5	NC_TP_CPU_RSVD<41>
RSVD_NCTF2	BV6	NC_TP_CPU_RSVD<42>
RSVD_NCTF1	BV8	NC_TP_CPU_RSVD<43>
RSVD45	AV69	TP_CPU_RSVD<45>
RSVD46	AK71	TP_CPU_RSVD<46>
RSVD47	AN69	TP_CPU_RSVD<47>
RSVD48	AP66	TP_CPU_RSVD<48>
RSVD49	AH66	TP_CPU_RSVD<49>
RSVD50	AK66	TP_CPU_RSVD<50>
RSVD51	AR71	TP_CPU_RSVD<51>
RSVD52	AM66	TP_CPU_RSVD<52>
RSVD53	AK69	TP_CPU_RSVD<53>
RSVD54	AU71	TP_CPU_RSVD<54>
RSVD55	AT70	TP_CPU_RSVD<55>
RSVD56	AR69	TP_CPU_RSVD<56>
RSVD57	AU69	TP_CPU_RSVD<57>
RSVD58	AT67	TP_CPU_RSVD<58>
RSVD_TP2	AP2	TP_CPU_RSVD<2>
RSVD_TP1	AN7	TP_CPU_RSVD<1>
RSVD62	AV4	CPU_THERMD_P
RSVD63	AU2	CPU_THERMD_N
RSVD64	BE69	TP_CPU_RSVD<64>
RSVD65	BE71	TP_CPU_RSVD<65>

DC_TEST_BV71	BV71	CPU_TEST_BV71_BV69
DC_TEST_BV69	BV69	
DC_TEST_BV68	BV68	TP_CPU_TEST_BV68
DC_TEST_BV5	BV5	TP_CPU_TEST_BV5
DC_TEST_BV3	BV3	CPU_TEST_BV3_BT3
DC_TEST_BV1	BV1	CPU_TEST_BV1_BT1
DC_TEST_BT71	BT71	CPU_TEST_BT71_BT69
DC_TEST_BT69	BT69	
DC_TEST_BT3	BT3	
DC_TEST_BT1	BT1	
DC_TEST_BR71	BR71	TP_CPU_TEST_BR71
DC_TEST_BR1	BR1	TP_CPU_TEST_BR1
DC_TEST_E71	E71	TP_CPU_TEST_E71
DC_TEST_E1	E1	TP_CPU_TEST_E1
DC_TEST_C71	C71	CPU_TEST_C71_A71
DC_TEST_C69	C69	CPU_TEST_C69_A69
DC_TEST_C3	C3	TP_CPU_TEST_C3
DC_TEST_A71	A71	
DC_TEST_A69	A69	
DC_TEST_A68	A68	TP_CPU_TEST_A68
DC_TEST_A5	A5	TP_CPU_TEST_A5

CFG0: PCIe Configuration Select 1 = Single PEG 0 = Bifurcation Enabled
CFG3: PCIe Lane Reversal 1 = Normal Operation 0 = Lanes Reversed
CFG4: Display Port Presence 1 = eDP Disabled 0 = Embedded Display Port Enabled

WF: RSVD nets with arrows have offpage marks on CRB schematic.
WF: RSVD nets with red wires have 0-ohm resistors to GND in CRB schematic.

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SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: CPU DMI/PEG/FDI/RSVD

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DRAWING NUMBER: <SCH_NUM> SIZE: D
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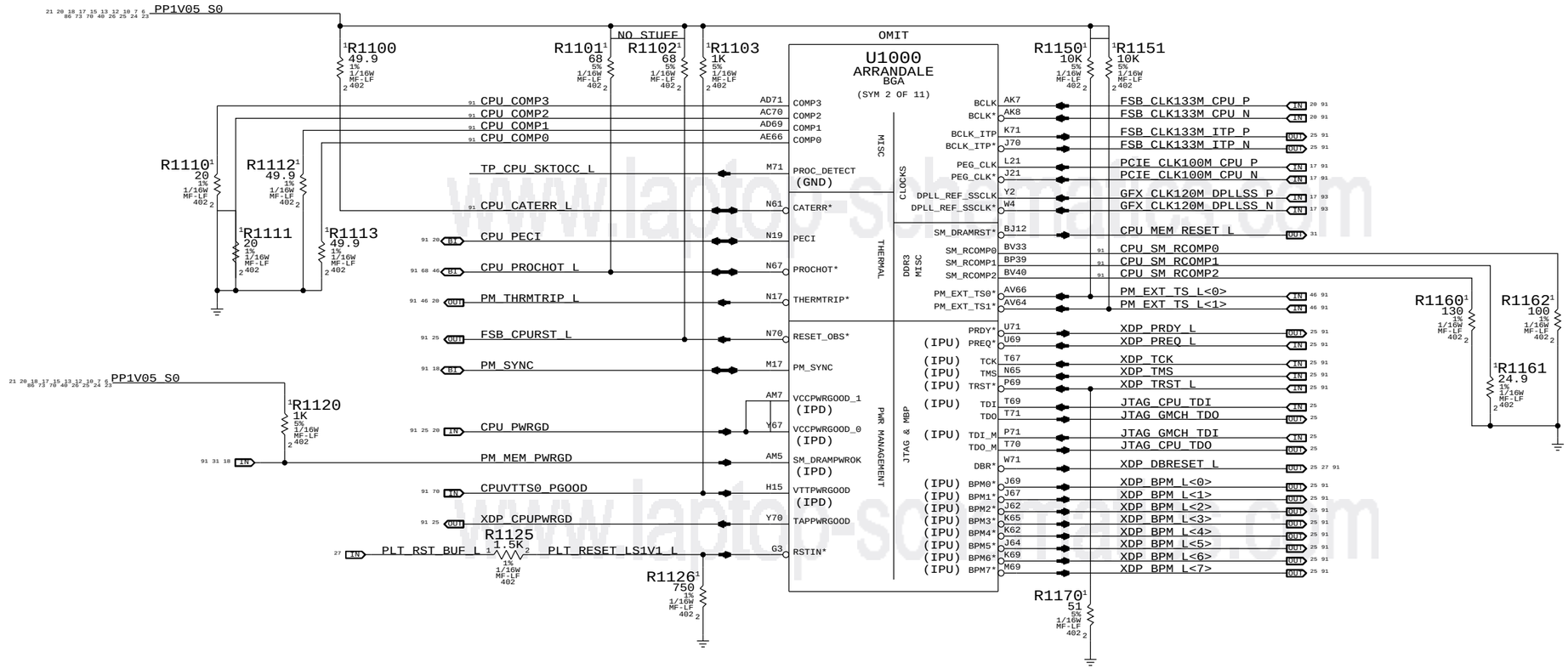

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CPU Clock/Misc/JTAG

Apple Inc.

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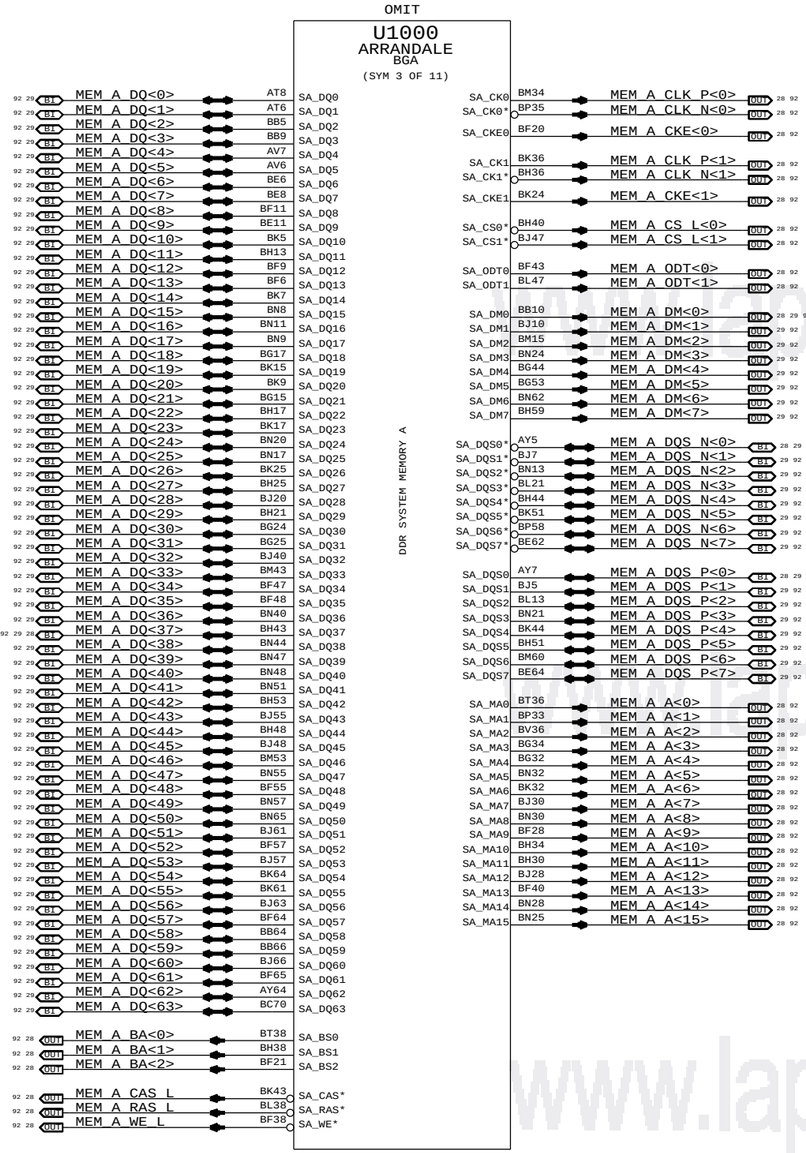

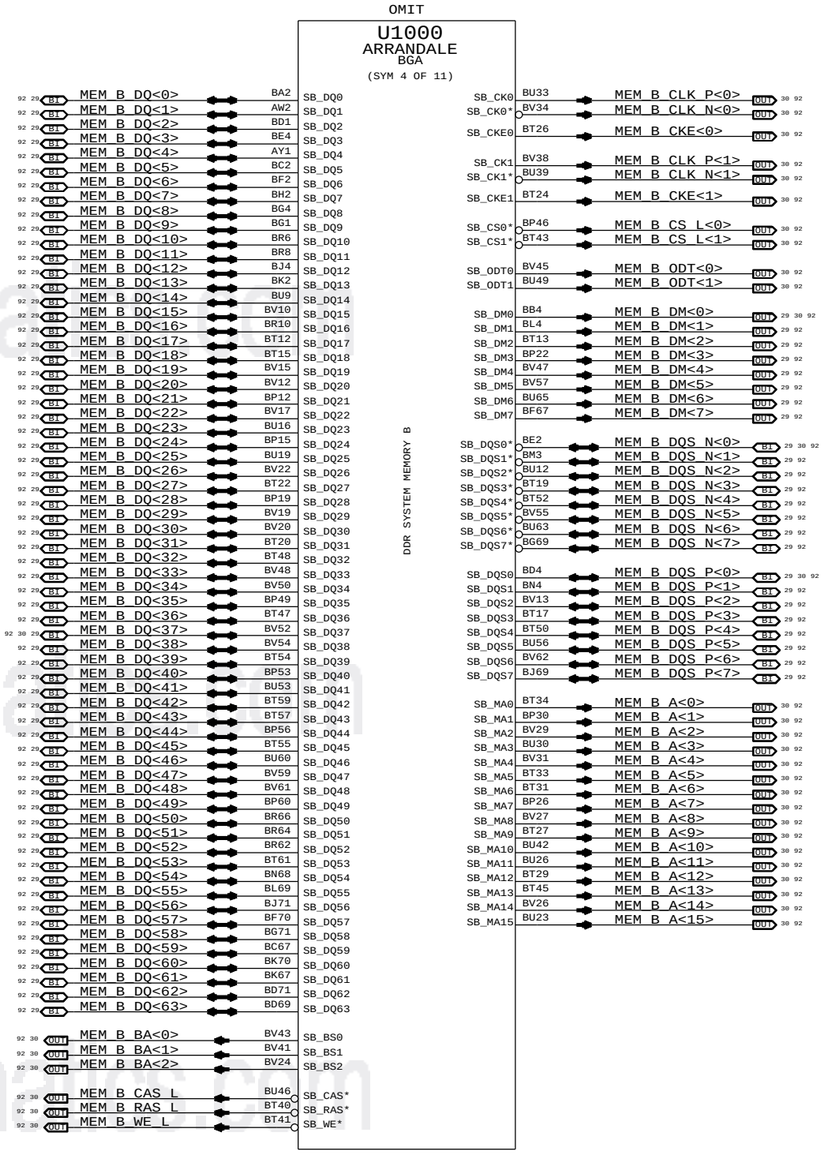

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CPU DDR3 Interfaces

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BGA
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POWER

CPU CORE SUPPLY

PPVCORE_S0_CPU_VCAP0

NOTE: VCAP0 is sourced by CPU
Do not connect to power supply,
but provide bypass caps on PCB.

BD55	VCAP0_1
BD51	VCAP0_2
BD48	VCAP0_3
BB55	VCAP0_4
BB51	VCAP0_5
BB48	VCAP0_6
AY57	VCAP0_7
AY53	VCAP0_8
AY50	VCAP0_9
AW57	VCAP0_10
AW53	VCAP0_11
AW50	VCAP0_12
AU55	VCAP0_13
AU51	VCAP0_14
AU48	VCAP0_15
AR55	VCAP0_16
AR51	VCAP0_17
AR48	VCAP0_18
AN57	VCAP0_19
AN53	VCAP0_20
AN50	VCAP0_21
AL57	VCAP0_22
AL53	VCAP0_23
AL50	VCAP0_24
AK57	VCAP0_25
AK53	VCAP0_26
AK50	VCAP0_27

PPVCORE_S0_CPU_VCAP1

NOTE: VCAP1 is sourced by CPU
Do not connect to power supply,
but provide bypass caps on PCB.

BD44	VCAP1_1
BD41	VCAP1_2
BD37	VCAP1_3
BB44	VCAP1_4
BB41	VCAP1_5
BB37	VCAP1_6
AY46	VCAP1_7
AY42	VCAP1_8
AY39	VCAP1_9
AW46	VCAP1_10
AW42	VCAP1_11
AW39	VCAP1_12
AU44	VCAP1_13
AU41	VCAP1_14
AU37	VCAP1_15
AR44	VCAP1_16
AR41	VCAP1_17
AR37	VCAP1_18
AN46	VCAP1_19
AN42	VCAP1_20
AN39	VCAP1_21
AL46	VCAP1_22
AL42	VCAP1_23
AL39	VCAP1_24
AK46	VCAP1_25
AK42	VCAP1_26
AK39	VCAP1_27

PPVCORE_S0_CPU

VCC_1	AF57
VCC_2	AF55
VCC_3	AF53
VCC_4	AF51
VCC_5	AF50
VCC_6	AF48
VCC_7	AF46
VCC_8	AF44
VCC_9	AF42
VCC_10	AF41
VCC_11	AD55
VCC_12	AD51
VCC_13	AD48
VCC_14	AD44
VCC_15	AD41
VCC_16	AB55
VCC_17	AB51
VCC_18	AB48
VCC_19	AB44
VCC_20	AB41
VCC_21	AA55
VCC_22	AA51
VCC_23	AA48
VCC_24	AA44
VCC_25	AA41
VCC_26	W55
VCC_27	W51
VCC_28	W48
VCC_29	W44
VCC_30	W41
VCC_31	U55
VCC_32	U51
VCC_33	U48
VCC_34	U44
VCC_35	U41
VCC_36	R55
VCC_37	R51
VCC_38	R48
VCC_39	R44
VCC_40	R41
VCC_41	P60
VCC_42	N55
VCC_43	N51
VCC_44	N48
VCC_45	N44
VCC_46	N42
VCC_47	M60
VCC_48	M51
VCC_49	M44
VCC_50	L55
VCC_51	K60
VCC_52	K51
VCC_53	K44
VCC_54	J55
VCC_55	H60
VCC_56	H51
VCC_57	H44
VCC_58	G60
VCC_59	G55
VCC_60	G51
VCC_61	G44
VCC_62	F55
VCC_63	E60
VCC_64	E57
VCC_65	E53
VCC_66	E50
VCC_67	E46
VCC_68	E42
VCC_69	D59
VCC_70	D57
VCC_71	D55
VCC_72	D54
VCC_73	D52
VCC_74	D50
VCC_75	D48
VCC_76	D47
VCC_77	D45
VCC_78	D43
VCC_79	B60
VCC_80	B56
VCC_81	B53
VCC_82	B49
VCC_83	B46
VCC_84	B42
VCC_85	A57
VCC_86	A54
VCC_87	A50
VCC_88	A47
VCC_89	A43

PP1V05_S0
PPVCORE_S0_CPU

R1300 100 1% 1/16W MF-LF 402
R1305 10 1% 1/16W MF-LF 402
PLACE_NEAR=U1000.F64:25.4MM
PLACE_NEAR=U1000.N13:25.4MM

R1301 100 1% 1/16W MF-LF 402
R1306 10 1% 1/16W MF-LF 402
PLACE_NEAR=U1000.F63:25.4MM
PLACE_NEAR=U1000.R12:25.4MM

CPU_PSI_L
CPU_VID<0>
CPU_VID<1>
CPU_VID<2>
CPU_VID<3>
CPU_VID<4>
CPU_VID<5>
CPU_VID<6>
TP_CPU_VTT_SELECT
PM_DPRSLPVR

VTT_SELECT: 1 = 1.05V, 0 = 1.1V

CPUIMVP_IMON
CPU_VCCSENSE_P
CPU_VCCSENSE_N
CPU_VTTSENSE_P
CPU_VTTSENSE_N

PP1V8_S0

PP1V5_S3_CPU_VCCDDR_CLK
MIN_LINE_WIDTH=0.4mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=1.5V

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F68	PSI*
A61	VID0
D61	VID1
D62	VID2
A62	VID3
B63	VID4
D64	VID5
D66	VID6
AN1	VTT_SELECT1
F66	PROC_DPRSLPVR

CPU VIDS

A41	ISENSE
F64	VCC_SENSE
F63	VSS_SENSE
N13	VTT_SENSE
R12	VSS_SENSE_VTT

SENSE LINES

W39	VCCPLL1
W37	VCCPLL2
U37	VCCPLL3
R39	VCCPLL4
R37	VCCPLL5

1.8V

POWER

BB14	VDDQ_CK1
BB12	VDDQ_CK2

1.1V RAIL POWER

PP1V05_S0
Arrandale: 1.05V
Clarksfield: 1.1V
(Controlled by VTT_SELECT pin)

BF60	VTT0_1
BF59	VTT0_2
BD60	VTT0_3
BD59	VTT0_4
BB60	VTT0_5
BB59	VTT0_6
AY60	VTT0_7
AW60	VTT0_8
AW35	VTT0_9
AW33	VTT0_10
AW14	VTT0_11
AW12	VTT0_12
AU60	VTT0_13
AU59	VTT0_14
AU12	VTT0_15
AR60	VTT0_16
AR59	VTT0_17
AR12	VTT0_18
AN60	VTT0_19
AN59	VTT0_20
AN35	VTT0_21
AN33	VTT0_22
AN17	VTT0_23
AN15	VTT0_24
AN14	VTT0_25
AN12	VTT0_26
AM10	VTT0_27
AL60	VTT0_28
AL59	VTT0_29
AL17	VTT0_30
AL15	VTT0_31
AL14	VTT0_32
AL12	VTT0_33
AK35	VTT0_34
AK33	VTT0_35
AF39	VTT0_36
AF37	VTT0_37
AF35	VTT0_38
AF33	VTT0_39
AF32	VTT0_40
AF30	VTT0_41
AD39	VTT0_42
AD37	VTT0_43
AD35	VTT0_44
AD33	VTT0_45
AD32	VTT0_46
AD30	VTT0_47
W35	VTT0_48
W33	VTT0_49
W32	VTT0_50
W30	VTT0_51
W28	VTT0_52
W26	VTT0_53
W24	VTT0_54
W23	VTT0_55
U35	VTT0_56
U33	VTT0_57
U32	VTT0_58
U30	VTT0_59
U28	VTT0_60
U26	VTT0_61
U24	VTT0_62
U23	VTT0_63
R35	VTT0_64
R33	VTT0_65
R32	VTT0_66
R30	VTT0_67
R28	VTT0_68
R26	VTT0_69
R24	VTT0_70
R23	VTT0_71
AY10	VTT0_72
AN9	VTT0_73

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CPU Power (1 of 2)

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U1000
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69 49 24 13 7 6 PPVCORE_S0_GFX

AN32	VAXG1	
AN30	VAXG2	
AN28	VAXG3	
AN26	VAXG4	
AN24	VAXG5	
AN23	VAXG6	
AN21	VAXG7	
AN19	VAXG8	
AL32	VAXG9	
AL30	VAXG10	
AL28	VAXG11	
AL26	VAXG12	
AL24	VAXG13	
AL23	VAXG14	
AL21	VAXG15	
AL19	VAXG16	
AK14	VAXG17	
AK12	VAXG18	
AJ10	VAXG19	
AH14	VAXG20	
AH12	VAXG21	
AF28	VAXG22	
AF26	VAXG23	
AF24	VAXG24	
AF23	VAXG25	
AF21	VAXG26	
AF19	VAXG27	
AF17	VAXG28	
AF15	VAXG29	
AF14	VAXG30	
AD28	VAXG31	
AD26	VAXG32	
AD24	VAXG33	
AD23	VAXG34	
AD21	VAXG35	
AD19	VAXG36	
AD17	VAXG37	

GRAPHICS

SENSE LINES

VAXG_SENSE	AF12	GFX_VSENSE_P
VSSAXG_SENSE	AF10	GFX_VSENSE_N

GRAPHICS VIDS

GFX_VID0	AF71	GFX_VID<0>
GFX_VID1	AG67	GFX_VID<1>
GFX_VID2	AG70	GFX_VID<2>
GFX_VID3	AH71	GFX_VID<3>
GFX_VID4	AN71	GFX_VID<4>
GFX_VID5	AM67	GFX_VID<5>
GFX_VID6	AM70	GFX_VID<6>
GFX_VR_EN	AH69	GFX_VR_EN
GFX_DPRSLPVR	AL71	GFX_DPRSLPVR
GFX_IMON	AL69	GFXIMVP_IMON

GFX_VID0 OUT 8 91
GFX_VID1 OUT 8 91
GFX_VID2 OUT 8 91
GFX_VID3 OUT 8 91
GFX_VID4 OUT 8 91
GFX_VID5 OUT 8 91
GFX_VID6 OUT 8 91
GFX_VR_EN OUT 69 91
GFX_DPRSLPVR OUT 69 91
GFX_IMON IN 69 91

69 49 24 13 7 6 PPVCORE_S0_GFX

R1400[1]
100
1%
1/10W
MF-LF
402[2]

GFX_VSENSE_P PLACE_NEAR=U1000.AF12:25.4MM OUT 69 91
GFX_VSENSE_N PLACE_NEAR=U1000.AF10:25.4MM OUT 69 91

R1401[1]
100
1%
1/10W
MF-LF
402[2]

GFX_VR_EN OUT 69 91

R1405[1]
4.7K
5%
1/10W
MF-LF
402[2]

PP1V5_S3RS0 6 7 16 31 42 72 73 99

DDR3 -1.5 V RAILS

VDDQ1	BU40	
VDDQ2	BU35	
VDDQ3	BU28	
VDDQ4	BN38	
VDDQ5	BM25	
VDDQ6	BL30	
VDDQ7	BJ38	
VDDQ8	BH32	
VDDQ9	BH28	
VDDQ10	BG43	
VDDQ11	BF16	
VDDQ12	BF15	
VDDQ13	BD35	
VDDQ14	BD33	
VDDQ15	BD32	
VDDQ16	BD30	
VDDQ17	BD28	
VDDQ18	BD26	
VDDQ19	BD24	
VDDQ20	BD23	
VDDQ21	BD21	
VDDQ22	BD19	
VDDQ23	BD17	
VDDQ24	BD15	
VDDQ25	BB35	
VDDQ26	BB33	
VDDQ27	BB32	
VDDQ28	BB30	
VDDQ29	BB28	
VDDQ30	BB26	
VDDQ31	BB24	
VDDQ32	BB23	
VDDQ33	BB21	
VDDQ34	BB19	
VDDQ35	BB17	
VDDQ36	BB15	

21 20 18 17 15 13 12 10 7 6 PP1V05_S0
88 73 70 40 26 25 24 23

PEG & DMI

W21	VTT1_1	
W19	VTT1_2	
U21	VTT1_3	
U19	VTT1_4	
U17	VTT1_5	
U15	VTT1_6	
U14	VTT1_7	
U12	VTT1_8	
R21	VTT1_9	
R19	VTT1_10	
R17	VTT1_11	

POWER

24 7 PPVCORE_S0_CPU_VCAP2

NOTE: VCAP2 is sourced by CPU
Do not connect to power supply,
but provide bypass caps on PCB.

AK62	VCAP2_1
AK60	VCAP2_2
AK59	VCAP2_3
AH60	VCAP2_4
AH59	VCAP2_5
AF60	VCAP2_6
AF59	VCAP2_7
AD60	VCAP2_8
AD59	VCAP2_9
AB60	VCAP2_10
AB59	VCAP2_11
AA60	VCAP2_12
AA59	VCAP2_13
W60	VCAP2_14
W59	VCAP2_15
U60	VCAP2_16
U59	VCAP2_17
R60	VCAP2_18
R59	VCAP2_19

PP1V1R1V05_S0_CPU_VTT0_DDR 15

VTT0_DDR	AW32	
VTT0_DDR1	AW30	
VTT0_DDR2	AW28	
VTT0_DDR3	AW26	
VTT0_DDR4	AW24	
VTT0_DDR5	AW23	
VTT0_DDR6	AW21	
VTT0_DDR7	AW19	
VTT0_DDR8	AW17	
VTT0_DDR9	AW15	

PP1V05_S0 6 7 10 12 13 15 17 18 20 21 23 24 25 26 40 70 73 80

VTT1_12	AD15	
VTT1_13	AD14	
VTT1_14	AD12	
VTT1_15	AB12	
VTT1_16	AA12	
VTT1_17	W17	
VTT1_18	W15	
VTT1_19	W14	
VTT1_20	W12	
VTT1_21	R15	

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BU62	VSS1	VSS76 AY62
BU58	VSS2	VSS77 AY59
BU55	VSS3	VSS78 AY55
BU51	VSS4	VSS79 AY51
BU48	VSS5	VSS80 AY48
BU44	VSS6	VSS81 AY44
BU37	VSS7	VSS82 AY41
BU32	VSS8	VSS83 AY37
BU25	VSS9	VSS84 AY35
BU21	VSS10	VSS85 AY33
BU18	VSS11	VSS86 AY32
BU14	VSS12	VSS87 AY30
BU11	VSS13	VSS88 AY28
BU7	VSS14	VSS89 AY26
BR42	VSS15	VSS90 AY24
BN64	VSS16	VSS91 AY23
BN6	VSS17	VSS92 AY21
BM70	VSS18	VSS93 AY19
BM51	VSS19	VSS94 AY17
BM44	VSS20	VSS95 AY15
BM32	VSS21	VSS96 AY14
BM24	VSS22	VSS97 AY12
BM17	VSS23	VSS98 AY8
BL57	VSS24	VSS99 AY4
BL55	VSS25	VSS100 AW67
BL48	VSS26	VSS101 AW62
BL40	VSS27	VSS102 AW59
BL28	VSS28	VSS103 AW55
BL20	VSS29	VSS104 AW51
BK63	VSS30	VSS105 AW48
BK60	VSS31	VSS106 AW44
BK53	VSS32	VSS107 AW41
BK34	VSS33	VSS108 AW37
BK10	VSS34	VSS109 AV9
BJ64	VSS35	VSS110 AV1
BJ21	VSS36	VSS111 AU70
BJ9	VSS37	VSS112 AU62
BJ1	VSS38	VSS113 AU57
BH70	VSS39	VSS114 AU53
BH57	VSS40	VSS115 AU50
BH55	VSS41	VSS116 AU46
BH47	VSS42	VSS117 AU42
BH24	VSS43	VSS118 AU39
BH20	VSS44	VSS119 AU35
BH15	VSS45	VSS120 AU33
BG51	VSS46	VSS121 AU32
BG36	VSS47	VSS122 AU30
BF62	VSS48	VSS123 AU28
BF30	VSS49	VSS124 AU26
BF13	VSS50	VSS125 AU24
BF8	VSS51	VSS126 AU23
BE70	VSS52	VSS127 AU21
BE65	VSS53	VSS128 AU19
BE9	VSS54	VSS129 AU17
BE1	VSS55	VSS130 AU15
BD57	VSS56	VSS131 AU14
BD53	VSS57	VSS132 AU4
BD50	VSS58	VSS133 AT64
BD46	VSS59	VSS134 AT10
BD42	VSS60	VSS135 AR62
BD39	VSS61	VSS136 AR57
BD14	VSS62	VSS137 AR53
BB71	VSS63	VSS138 AR50
BB62	VSS64	VSS139 AR46
BB57	VSS65	VSS140 AR42
BB53	VSS66	VSS141 AR39
BB50	VSS67	VSS142 AR35
BB46	VSS68	VSS143 AR33
BB42	VSS69	VSS144 AR32
BB39	VSS70	VSS145 AR30
BB7	VSS71	VSS146 AR28
BB1	VSS72	VSS147 AR26
BA70	VSS73	VSS148 AR24
AY71	VSS74	VSS149 AR23
AY66	VSS75	VSS150 AR21

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AR19	VSS151	VSS226 BN71
AR17	VSS152	VSS227 E68
AR15	VSS153	VSS228 AH28
AR14	VSS154	VSS229 AH41
AR4	VSS155	VSS230 A66
AR1	VSS156	VSS231 AH26
AP70	VSS157	VSS232 BN1
AP64	VSS158	VSS233 A64
AN62	VSS159	VSS234 AH24
AN55	VSS160	VSS235 AH39
AN51	VSS161	VSS236 E5
AN48	VSS162	VSS237 AH23
AN44	VSS163	VSS238 C68
AN41	VSS164	VSS239 AH21
AN37	VSS165	VSS240 AH19
AN5	VSS166	VSS241 AH17
AN4	VSS167	VSS242 AH15
AM64	VSS168	VSS243 AH4
AM8	VSS169	VSS244 AG64
AL62	VSS170	VSS245 AG9
AL55	VSS171	VSS246 AG6
AL51	VSS172	VSS247 AF69
AL48	VSS173	VSS248 AF62
AL44	VSS174	VSS249 AF1
AL41	VSS175	VSS250 AE70
AL37	VSS176	VSS251 AE64
AL35	VSS177	VSS252 AD62
AL33	VSS178	VSS253 AD57
AL1	VSS179	VSS254 AD53
AK70	VSS180	VSS255 AD50
AK64	VSS181	VSS256 AD46
AK55	VSS182	VSS257 AD42
AK51	VSS183	VSS258 AD4
AK48	VSS184	VSS259 AC67
AK44	VSS185	VSS260 AC64
AK41	VSS186	VSS261 AC10
AK37	VSS187	VSS262 AC5
AK32	VSS188	VSS263 AC1
AK30	VSS189	VSS264 AB70
AK28	VSS190	VSS265 AB62
AK26	VSS191	VSS266 AB57
AK24	VSS192	VSS267 AB53
AK23	VSS193	VSS268 AB50
AK21	VSS194	VSS269 AB46
AK19	VSS195	VSS270 AB42
AK17	VSS196	VSS271 AB39
AK15	VSS197	VSS272 AB37
AJ70	VSS198	VSS273 AB35
AH62	VSS199	VSS274 AB33
AH57	VSS200	VSS275 AB32
AH55	VSS201	VSS276 AB30
AH53	VSS202	VSS277 AB28
BV66	VSS203	VSS278 AB26
AH51	VSS204	VSS279 AB24
BV64	VSS205	VSS280 AB23
AH50	VSS206	VSS281 AB21
BT68	VSS207	VSS282 AB19
AH48	VSS208	VSS283 AB17
BR69	VSS209	VSS284 AB15
BL71	VSS210	VSS285 AB14
AH46	VSS211	VSS286 AB9
BL1	VSS212	VSS287 AA66
AH37	VSS213	VSS288 AA64
BR68	VSS214	VSS289 AA62
R14	VSS215	VSS290 AA57
AH35	VSS216	VSS291 AA53
AH44	VSS217	VSS292 AA50
H71	VSS218	VSS293 AA46
AH33	VSS219	VSS294 AA42
BR3	VSS220	VSS295 AA39
F71	VSS221	VSS296 AA37
AH32	VSS222	VSS297 AA35
AH42	VSS223	VSS298 AA33
E69	VSS224	VSS299 AA32
AH30	VSS225	VSS300 AA30

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U1000
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BGA
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AA28	VSS301	VSS367 K6
AA26	VSS302	VSS368 K4
AA24	VSS303	VSS369 J65
AA23	VSS304	VSS370 J57
AA21	VSS305	VSS371 J48
AA19	VSS306	VSS372 J47
AA17	VSS307	VSS373 J40
AA15	VSS308	VSS374 J9
AA14	VSS309	VSS375 H53
AA4	VSS310	VSS376 H43
W69	VSS311	VSS377 H36
W62	VSS312	VSS378 H1
W57	VSS313	VSS379 G70
W53	VSS314	VSS380 G57
W50	VSS315	VSS381 G53
W46	VSS316	VSS382 G48
W42	VSS317	VSS383 G47
W6	VSS318	VSS384 G43
W1	VSS319	VSS385 G30
V70	VSS320	VSS386 G24
U64	VSS321	VSS387 G20
U62	VSS322	VSS388 G15
U57	VSS323	VSS389 F61
U53	VSS324	VSS390 F48
U50	VSS325	VSS391 F47
U46	VSS326	VSS392 F28
U42	VSS327	VSS393 F20
U39	VSS328	VSS394 F4
U9	VSS329	VSS395 E37
U4	VSS330	VSS396 E33
T1	VSS331	VSS397 E30
R70	VSS332	VSS398 E16
R62	VSS333	VSS399 E12
R57	VSS334	VSS400 D41
R53	VSS335	VSS401 D38
R50	VSS336	VSS402 D34
R46	VSS337	VSS403 D31
R42	VSS338	VSS404 D27
R5	VSS339	VSS405 D24
P4	VSS340	VSS406 D20
N63	VSS341	VSS407 D17
N57	VSS342	VSS408 D13
N53	VSS343	VSS409 D10
N50	VSS344	VSS410 D6
N46	VSS345	VSS411 B65
N30	VSS346	VSS412 B62
N21	VSS347	VSS413 B58
N15	VSS348	VSS414 B55
N53	VSS349	VSS415 B51
M42	VSS350	VSS416 B48
M36	VSS351	VSS417 B44
M1	VSS352	VSS418 A59
L70	VSS353	VSS419 A55
L57	VSS354	VSS420 A52
L48	VSS355	VSS421 A48
L47	VSS356	VSS422 A45
L13	VSS357	VSS423 A40
K64	VSS358	VSS424 A36
K53	VSS359	VSS425 A33
K43	VSS360	VSS426 A29
K36	VSS361	VSS427 A26
K34	VSS362	VSS428 A22
K32	VSS363	VSS429 A19
K25	VSS364	VSS430 A15
K17	VSS365	VSS431 A12
K11	VSS366	VSS432 A8
		VSS433 B40

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PAGE TITLE

CPU Grounds

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CPU VCore HF and Bulk Decoupling

4x 470uF 4.5mOhm, 3x 62uF B2, 10x 22uF 0603, 25x 1uF 0402

PPVCORE_S0_CPU

PLACEMENT_NOTE (C1600-C1624):

Place on bottom side of U1000..

C1600 C1601 C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609 C1610 C1611 C1612
1UF 10% 16V X5R 402

C1613 C1614 C1615 C1616 C1617 C1618 C1619 C1620 C1621 C1622 C1623 C1624
1UF 10% 16V X5R 402

PLACEMENT_NOTE (C1625-C1634):

Place near U1000 on bottom side.

NO STUFF C1625 NO STUFF C1626 C1627 NO STUFF C1628 NO STUFF C1629 C1630 NO STUFF C1631 C1632 NO STUFF C1634 C1691 NO STUFF C1692 NO STUFF C1693 C1694 C1698
22UF 20% 6.3V X5R-CERM 603

PLACEMENT_NOTE (C1635-C1648):

Place near inductors on bottom side.

NO STUFF C1635 NO STUFF C1636 NO STUFF C1637 C1638 NO STUFF C1640 NO STUFF C1641 C1642 NO STUFF C1643 C1644 NO STUFF C1645 NO STUFF C1646 C1648
22UF 20% 6.3V X5R-CERM 603

C1649 C1650 C1651 C1652 NO STUFF C16A0 NO STUFF C16A1 C16A2 C16A3 C16A4
470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM
62UF 20% 11V ELEC CASE-B2

VTT (CPU Uncore) DECOUPLING

3x 330uF 6 mOhm, 4x 22uF 0805, 7x 10uF 0603, 24x 1uF 0402

PP1V05_S0

PLACEMENT_NOTE (C1653-C1656):

Place on bottom side of U1000.

C1653 C1654 C1655 C1656
22UF 20% 6.3V X5R-CERM 603

PLACEMENT_NOTE (C1657-C1663):

Place on bottom side of U1000..

C1657 C1658 C1659 C1660 C1661 C1662 C1663
10UF 20% 6.3V X5R 603

PLACEMENT_NOTE (C1664-C1687):

Place on bottom side of U1000.

C1664 C1665 C1666 C1667 C1668 C1669 C1670 C1671 C1672 C1673 C1674 C1675
1UF 10% 16V X5R 402

C1676 C1677 C1678 C1679 C1680 C1681 C1682 C1683 C1684 C1685 C1686 C1687
1UF 10% 16V X5R 402

C1688 C1689 C1690
330UF 20% 2.0V POLY-TANT D2T-SM2

CPU Power On Configuration (POC) Straps

Intel recommends all option straps should be provided in layout

PP1V05_S0

R1600 1K	R1602 1K	CPUPOC4U R1604 1K	NO STUFF R1606 1K
	R1601 1K	CPUPOC3U R1603 1K	CPUPOC5U R1605 1K
			NO STUFF R1607 1K

1K 5% 1/16W MF-LF 402

CPU_VID<0>
CPU_VID<1>
CPU_VID<2>
CPU_VID<3>
CPU_VID<4>
CPU_VID<5>
CPU_VID<6>
PM_DPRSLPVR
CPU_PSI_L

NO STUFF R1610 1K	NO STUFF R1612 1K	CPUPOC4D R1614 1K	R1616 1K	R1618 1K
	NO STUFF R1611 1K	CPUPOC3D R1613 1K	CPUPOC5D R1615 1K	NO STUFF R1617 1K

VID[2:0] = Reserved (111)
VID[5:3] = GPU Gain Setting (See below)
VID[6] = Reserved (0)
DPRSLPVR = 1 - IMVP-6.5 compliant controller
PSI# = Reserved (0)

BOM GROUP	IMAX @ 900mV	CPU Gain Setting	BOM OPTIONS	Equivalent Gain
CPUPOC_IMAX_DIS		000	CPUPOC3D,CPUPOC4D,CPUPOC5D	
CPUPOC_IMAX_0_20	20A	001	CPUPOC3D,CPUPOC4D,CPUPOC5U	45
CPUPOC_IMAX_20_30	30A	010	CPUPOC3D,CPUPOC4U,CPUPOC5D	30
CPUPOC_IMAX_30_40	40A	011	CPUPOC3D,CPUPOC4U,CPUPOC5U	22.5
CPUPOC_IMAX_40_50	50A	100	CPUPOC3U,CPUPOC4D,CPUPOC5D	18
CPUPOC_IMAX_50_60	60A	101	CPUPOC3U,CPUPOC4D,CPUPOC5U	15
CPUPOC_IMAX_60_70	70A	110	CPUPOC3U,CPUPOC4U,CPUPOC5D	12.857
CPUPOC_IMAX_70_90	90A	111	CPUPOC3U,CPUPOC4U,CPUPOC5U	10

NOTE: BOM Configurations should not call out CPUPOCnU/D BOMOPTIONs directly. Instead call out appropriate BOM GROUP defined in tables above.

VTT0_DDR DECOUPLING

3x 1uF 0402

PLACEMENT_NOTE (C1695-C1697):

Place on bottom side of U1000.

L1695 30-OHM-5A 0603

PP1V1R1V05_S0_CPU_VTT0_DDR
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.1V

C1695 C1696 C1697
1UF 10% 16V X5R 402

Design recommendations from Calpella Small Form Factor Design Guide Rev 1.5 (doc #407364) table 2-34 and Calpella Small Form Factor Schematic Check List Rev 1.1 (doc #395914) table 3.26.

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PAGE TITLE: CPU Non-GFX Decoupling (1 of 2)

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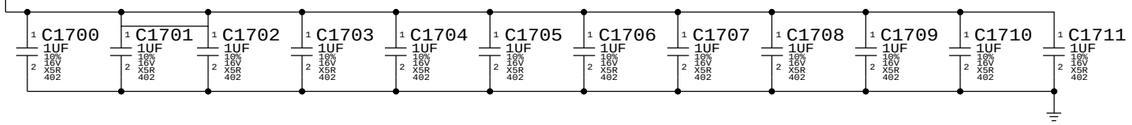
VCAP0 (CPU BSC Package) DECOUPLING

12x 1uF 0402

PLACEMENT_NOTE (C1700-C1711):

Place on bottom side of U1000.

PPVCORE_S0_CPU_VCAP0



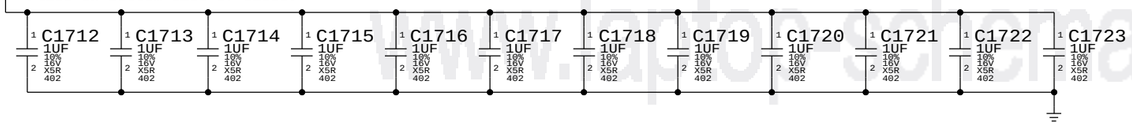
VCAP1 (CPU BSC Package) DECOUPLING

12x 1uF 0402

PLACEMENT_NOTE (C1712-C1723):

Place on bottom side of U1000.

PPVCORE_S0_CPU_VCAP1

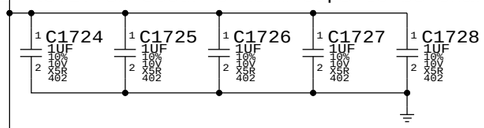


Memory (CPU VCCDDR) DECOUPLING

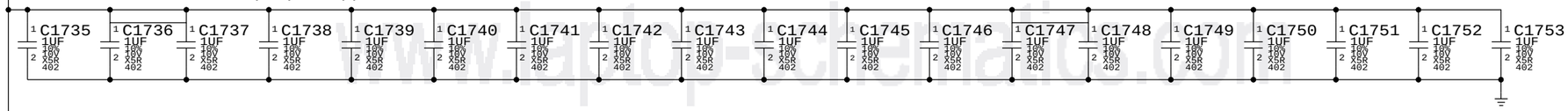
5x 1uF 0402

NOTE: 3x 330uF 6 mOhm caps to be shared between CPU and SO-DIMMs. DG recommends 2x 22uF at SO_DIMM not provided. Decoupling caps at SO-DIMMs on CSA 29 and CSA 31.

PP1V5_S3RS0



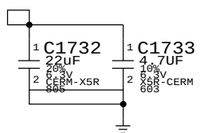
NOTE: 19x 1uF 0402 caps per Apple SI for CMD and CNTRL lines.



PLL (CPU VCCSFR) DECOUPLING

1x 22uF 0805, 1x 4.7uF 0603

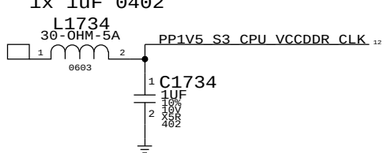
PP1V8_S0



DDR Clock (CPU VDDQ_CK) DECOUPLING

1x 1uF 0402

PP1V5_S3RS0



Design recommendations from Calpella Small Form Factor Design Guide Rev 1.5 (doc #407364) table 2-34 and Calpella Small Form F
actor Schematic Check List Rev 1.1 (doc #395914) table 3.26.

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PAGE TITLE: CPU Non-GFX Decoupling (2 of 2)

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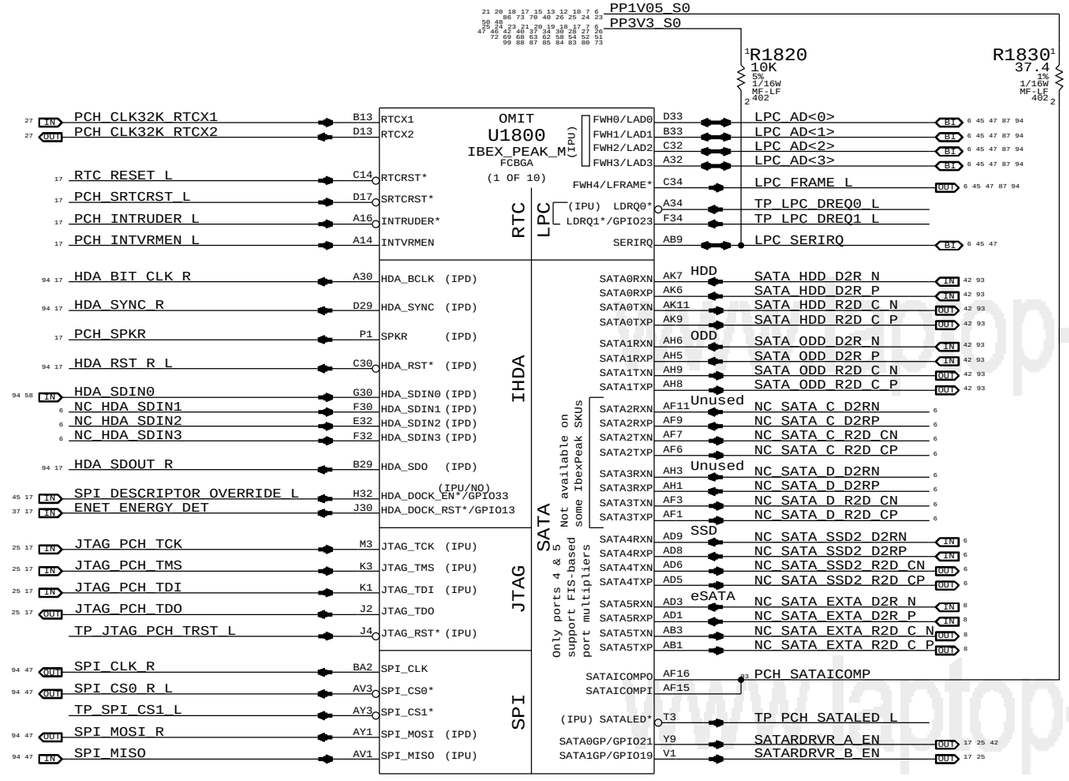

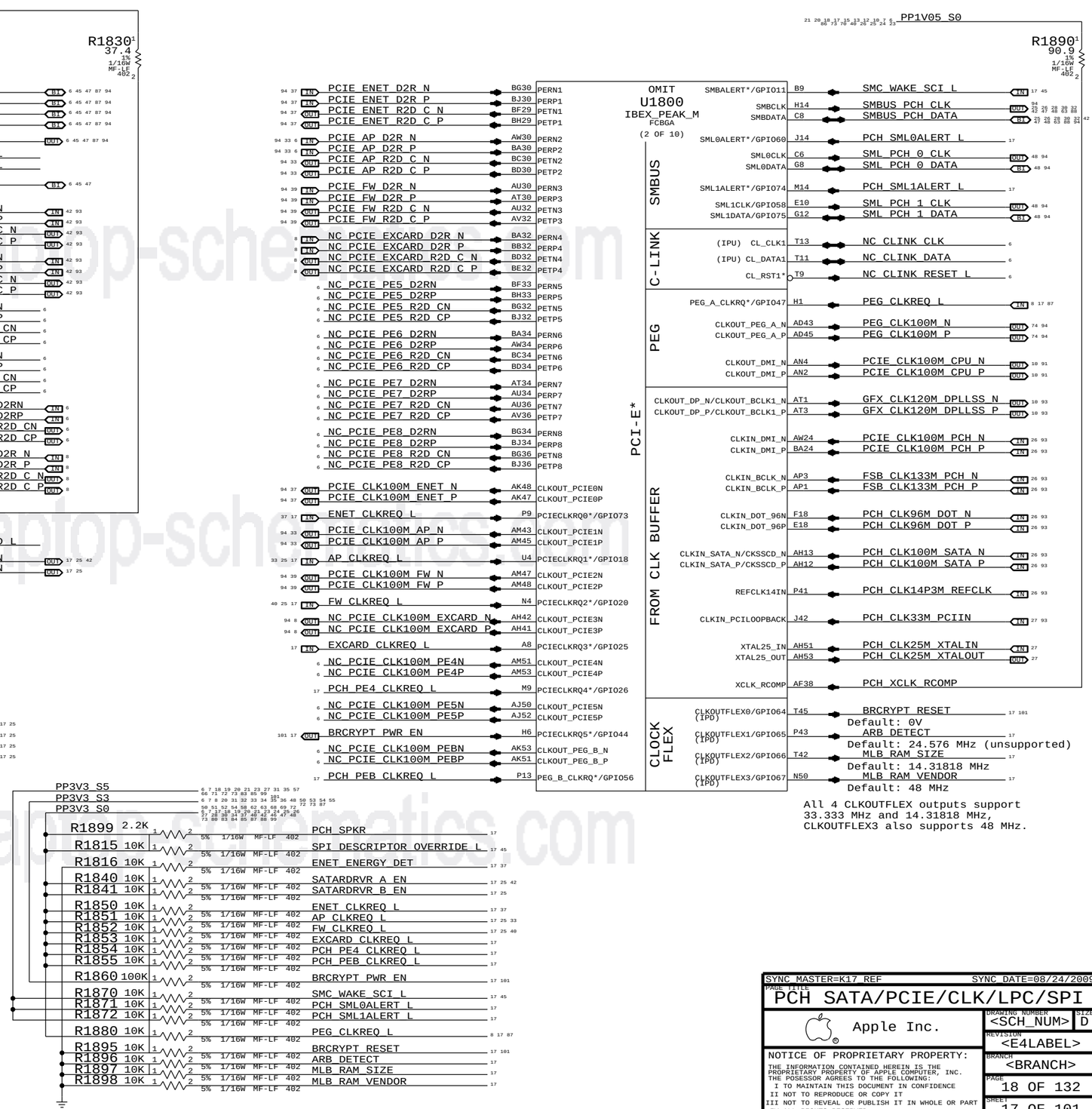

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PCH SATA/PCIE/CLK/LPC/SPI

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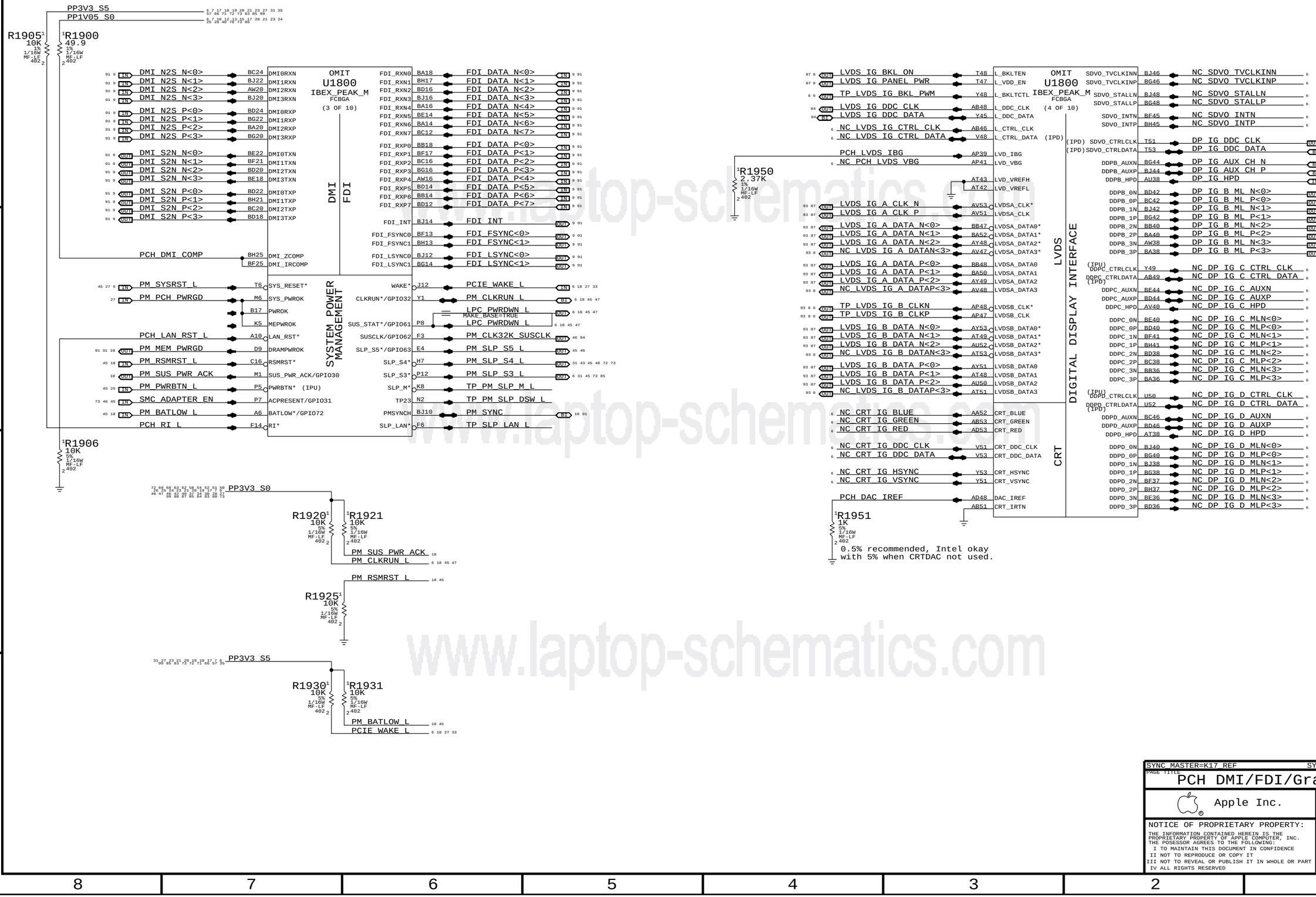

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PCI

NC_PCI_AD<0>	H40	AD0	
NC_PCI_AD<1>	N34	AD1	
NC_PCI_AD<2>	C44	AD2	
NC_PCI_AD<3>	A38	AD3	
NC_PCI_AD<4>	C36	AD4	
NC_PCI_AD<5>	J34	AD5	
NC_PCI_AD<6>	A40	AD6	
NC_PCI_AD<7>	D45	AD7	
NC_PCI_AD<8>	E36	AD8	
NC_PCI_AD<9>	H48	AD9	
NC_PCI_AD<10>	E40	AD10	
NC_PCI_AD<11>	C40	AD11	
NC_PCI_AD<12>	M48	AD12	
NC_PCI_AD<13>	M45	AD13	
NC_PCI_AD<14>	F53	AD14	
NC_PCI_AD<15>	M40	AD15	
NC_PCI_AD<16>	M43	AD16	
NC_PCI_AD<17>	J36	AD17	
NC_PCI_AD<18>	K48	AD18	
NC_PCI_AD<19>	F40	AD19	
NC_PCI_AD<20>	C42	AD20	
NC_PCI_AD<21>	K46	AD21	
NC_PCI_AD<22>	M51	AD22	
NC_PCI_AD<23>	J52	AD23	
NC_PCI_AD<24>	K51	AD24	
NC_PCI_AD<25>	L34	AD25	
NC_PCI_AD<26>	F42	AD26	
NC_PCI_AD<27>	J40	AD27	
NC_PCI_AD<28>	G46	AD28	
NC_PCI_AD<29>	F44	AD29	
NC_PCI_AD<30>	M47	AD30	
NC_PCI_AD<31>	H36	AD31	
NC_PCI_C_BE_L<0>	J50	C/BE0*	
NC_PCI_C_BE_L<1>	G42	C/BE1*	
NC_PCI_C_BE_L<2>	H47	C/BE2*	
NC_PCI_C_BE_L<3>	G34	C/BE3*	
PCI_INTA_L	G38	PIRQA*	
PCI_INTB_L	H51	PIRQB*	
PCI_INTC_L	B37	PIRQC*	
PCI_INTD_L	A44	PIRQD*	
PCI_REQ0_L	F51	REQ0*	
JTAG_GMUX_TMS	A46	REQ1*/GPIO50	
JTAG_GMUX_TDI	B45	REQ2*/GPIO52	
PCI_REQ3_L	M53	REQ3*/GPIO54	
NC_PCI_GNT0_L	F48	GNT0* (IPU)	
NC_PCI_GNT1_L	K45	GNT1*/GPIO51	
NC_PCI_GNT2_L	E36	GNT2*/GPIO53	
NC_PCI_GNT3_L	H53	GNT3*/GPIO55	
PCH_GPIO2	B41	PIRQE*/GPIO2	
AUD_IP_PERIPHERAL_DET	K53	PIRQF*/GPIO3	
MIKEY_MIC_LOAD_DET	A36	PIRQG*/GPIO4	
AUD_I2C_INT_L	A48	PIRQH*/GPIO5	
NC_PCI_RESET_L	K6	PCIRST*	
PCI_SERR_L	E44	SERR*	
PCI_PERR_L	E50	PERR*	
PCI_IRDY_L	A42	IRDY*	
NC_PCI_PAR	H44	PAR	
PCI_DEVSEL_L	F46	DEVSEL*	
PCI_FRAME_L	C46	FRAME*	
PCI_PLOCK_L	D49	PLOCK*	
PCI_STOP_L	D41	STOP*	
PCI_TRDY_L	C48	TRDY*	
NC_PCI_PME_L	M7	PME* (IPU)	
PLT_RESET_L	D5	PLTRST*	
LPC_CLK33M_SMC_R	N52	CLKOUT_PCI0	
LPC_CLK33M_LPCPLUS_R	P53	CLKOUT_PCI1	
LPC_CLK33M_GMUX_R	P46	CLKOUT_PCI2	
NC_PCI_CLK33M_OUT3	P51	CLKOUT_PCI3	
PCH_CLK33M_PCIOUT	P48	CLKOUT_PCI4	

NVRAM

NV_CE0*	AY9	NC_NV_CE_L<0>
NV_CE1*	BD1	NC_NV_CE_L<1>
NV_CE2*	AP15	NC_NV_CE_L<2>
NV_CE3*	BD8	NC_NV_CE_L<3>
NV_DQS0	AV9	NC_NV_DQS<0>
NV_DQS1	BG8	NC_NV_DQS<1>
NV_DQ0/NV_IO0	AP7	NC_NV_DQ<0>
NV_DQ1/NV_IO1	AP6	NC_NV_DQ<1>
NV_DQ2/NV_IO2	AT6	NC_NV_DQ<2>
NV_DQ3/NV_IO3	AT9	NC_NV_DQ<3>
NV_DQ4/NV_IO4	BB1	NC_NV_DQ<4>
NV_DQ5/NV_IO5	AV6	NC_NV_DQ<5>
NV_DQ6/NV_IO6	BB3	NC_NV_DQ<6>
NV_DQ7/NV_IO7	BA4	NC_NV_DQ<7>
NV_DQ8/NV_IO8	BE4	NC_NV_DQ<8>
NV_DQ9/NV_IO9	BB6	NC_NV_DQ<9>
NV_DQ10/NV_IO10	BD6	NC_NV_DQ<10>
NV_DQ11/NV_IO11	BB7	NC_NV_DQ<11>
NV_DQ12/NV_IO12	BC8	NC_NV_DQ<12>
NV_DQ13/NV_IO13	BJ8	NC_NV_DQ<13>
NV_DQ14/NV_IO14	BJ6	NC_NV_DQ<14>
NV_DQ15/NV_IO15	BG6	NC_NV_DQ<15>
(IPD) NV_ALE	BD3	NC_NV_ALE
(IPD) NV_CLE	AY6	NC_NV_CLE
NV_RCOMP	AU2	NC_PCH_NV_RCOMP
(IPU) NV_RB*	AV7	NC_NV_RB_L
NV_WR0_RE*	AY8	NC_NV_WR_RE_L<0>
NV_WR1_RE*	AY5	NC_NV_WR_RE_L<1>
NV_WE_CK0*	AV11	NC_NV_WE_CK_L<0>
NV_WE_CK1*	BF5	NC_NV_WE_CK_L<1>

USB

NOTE: Internal pull-downs on all USB pins

EHCI1 (DPD)

USBP0N	H18	USB_HUB1_UP_N	External Hub 1
USBP0P	J18	USB_HUB1_UP_P	External Hub 1
USBP1N	A18	NC_USB_1N	
USBP1P	C18	NC_USB_1P	
USBP2N	N20	USB_BRCRYPT_N	T57
USBP2P	P20	USB_BRCRYPT_P	T57
USBP3N	J20	NC_USB_3N	
USBP3P	L20	NC_USB_3P	
USBP4N	F20	NC_USB_4N	
USBP4P	G20	NC_USB_4P	
USBP5N	A20	NC_USB_5N	
USBP5P	C20	NC_USB_5P	
USBP6N	M22	NC_USB_6N	
USBP6P	N22	NC_USB_6P	
USBP7N	B21	NC_USB_7N	
USBP7P	D21	NC_USB_7P	

EHCI2 (DPD)

USBP8N	H22	USB_HUB2_UP_N	External Hub 2
USBP8P	J22	USB_HUB2_UP_P	External Hub 2
USBP9N	E22	NC_USB_9N	
USBP9P	F22	NC_USB_9P	
USBP10N	A22	NC_USB_10N	
USBP10P	C22	NC_USB_10P	
USBP11N	G24	NC_USB_11N	
USBP11P	H24	NC_USB_11P	
USBP12N	L24	NC_USB_12N	
USBP12P	M24	NC_USB_12P	
USBP13N	A24	NC_USB_13N	
USBP13P	C24	NC_USB_13P	
USBRBIAS*	B25	PCH_USB_RBIAS	
USBRBIAS	D25		

OMIT U1800 IBEX_PEAK_M FCBGA (5 OF 10)

OC0*/GPIO59	N16	PCH_GPIO59	
OC1*/GPIO40	J16	USB_HUB_SOFT_RESET_L	
OC2*/GPIO41	F16	PCH_GPIO41	
OC3*/GPIO42	L16	PCH_GPIO42	
OC4*/GPIO43	E14	PCH_GPIO43	
OC5*/GPIO9	G16	PCH_GPIO9	
OC6*/GPIO10	F12	PCH_GPIO10	
OC7*/GPIO14	T15	PM_LATRIGGER_L	

PP3V3_S0

R2010 10K 5% 1/16W MF-LF 402 — PCI_INTA_L
R2011 10K 5% 1/16W MF-LF 402 — PCI_INTB_L
R2012 10K 5% 1/16W MF-LF 402 — PCI_INTC_L
R2013 10K 5% 1/16W MF-LF 402 — PCI_INTD_L
R2014 10K 5% 1/16W MF-LF 402 — PCI_REQ0_L

R2020 10K 5% 1/16W MF-LF 402 — PCI_SERR_L
R2021 10K 5% 1/16W MF-LF 402 — PCI_PERR_L
R2022 10K 5% 1/16W MF-LF 402 — PCI_IRDY_L
R2023 10K 5% 1/16W MF-LF 402 — NC_PCI_PAR
R2024 10K 5% 1/16W MF-LF 402 — PCI_DEVSEL_L
R2025 10K 5% 1/16W MF-LF 402 — PCI_FRAME_L
R2026 10K 5% 1/16W MF-LF 402 — PCI_PLOCK_L
R2027 10K 5% 1/16W MF-LF 402 — PCI_STOP_L
PCI_TRDY_L

R2030 10K 5% 1/16W MF-LF 402 — JTAG_GMUX_TMS
R2031 10K 5% 1/16W MF-LF 402 — JTAG_GMUX_TDI
R2032 10K 5% 1/16W MF-LF 402 — PCI_REQ0_L
R2035 10K 5% 1/16W MF-LF 402 — PCH_GPIO2
R2036 10K 5% 1/16W MF-LF 402 — AUD_IP_PERIPHERAL_DET
R2037 10K 5% 1/16W MF-LF 402 — MIKEY_MIC_LOAD_DET
R2038 10K 5% 1/16W MF-LF 402 — AUD_I2C_INT_L

PP3V3_S5

R2080 10K 5% 1/16W MF-LF 402 — PCH_GPIO59
R2081 10K 5% 1/16W MF-LF 402 — PM_LATRIGGER_L

R2060 10K 5% 1/16W MF-LF 402
R2061 10K 5% 1/16W MF-LF 402
R2062 10K 5% 1/16W MF-LF 402
R2064 10K 5% 1/16W MF-LF 402
R2065 10K 5% 1/16W MF-LF 402
R2066 10K 5% 1/16W MF-LF 402

R2070 22.6 1% 1/10W MF-LF 402

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IPU* = Only on TACH function.

46 45 25 20	IN	SMC_IG_THROTTLE_L	Y3	BMBUSY*/GPIO0		
40 20 8	IN	FW_PLUG_DET_L	C38	TACH1/GPIO1 (IPU*)		
87 20	IN	GMUX_INT	D37	TACH2/GPIO6 (IPU*)		
45 20	IN	SMC_RUNTIME_SCI_L	J32	TACH3/GPIO7 (IPU*)		
20		PCH_FCIM_EN_L	F10	GPIO8 (IPU)		
37 20	OUT	ENET_LOW_PWR	K9	LAN_PHY_PWR_CTRL/GPIO12		
20		PCH_GPIO15	T7	GPIO15 (IPD)		
63 25 20	OUT	AUD_IPHS_SWITCH_EN	AA2	SATA4GP/GPIO16		
47 20 6	BI	LPCPLUS_GPIO	F38	TACH0/GPIO17 (IPU*)		
42 20	OUT	ODD_PWR_EN_L	Y7	SCLOCK/GPIO22		
20		PCH_GPIO24	H10	MEM_LED/GPIO24		
20		PCH_VRM_EN	AB12	GPIO27		
31 25	OUT	ISOLATE_CPU_MEM_L	V13	GPIO28 (IPU)		
		TP_PCH_STP_PCI_L	M11	STP_PCI*/GPIO34		
20	OUT	MXM_GOOD	V6	SATACLKREQ*/GPIO35		
34 25 20	OUT	SDCARD_RESET	AB7	SATA2GP/GPIO36		
87 25 20	OUT	JTAG_GMUX_TCK	AB13	SATA3GP/GPIO37		
87 20	IN	JTAG_GMUX_TDO	V3	SLOAD/GPIO38		
20		PCH_GPIO39	P3	SDATAOUT0/GPIO39		
73 20	OUT	WOL_EN	H3	PCIECLKRQ6*/GPIO45		
73 33 20	OUT	AP_PWR_EN	F1	PCIECLKRQ7*/GPIO46		
40 20	OUT	FW_PWR_EN	AB6	SDATAOUT1/GPIO48		
25 20	OUT	ME_TEMP_ALERT_L	AA4	SATA5GP/GPIO49		
57 47 20 6	BI	SPIROM_USE_MLB	F8	GPIO57		

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GPIO

94 6		PCH_VSS_NCTF<1>	A4	VSS_NCTF1		
94 6		PCH_VSS_NCTF<2>	A49	VSS_NCTF2		
			A5	VSS_NCTF3		
			A50	VSS_NCTF4		
94 6		PCH_VSS_NCTF<5>	A52	VSS_NCTF5		
			A53	VSS_NCTF6		
94		TP_PCH_VSS_NCTF<7>	B2	VSS_NCTF7		
			B4	VSS_NCTF8		
94 6		PCH_VSS_NCTF<9>	B52	VSS_NCTF9		
			B53	VSS_NCTF10		
94 6		PCH_VSS_NCTF<11>	BE1	VSS_NCTF11		
94 6		PCH_VSS_NCTF<12>	BE53	VSS_NCTF12		
			BF1	VSS_NCTF13		
			BF53	VSS_NCTF14		
94 6		PCH_VSS_NCTF<15>	BH1	VSS_NCTF15		
			BH2	VSS_NCTF16		
94 6		PCH_VSS_NCTF<17>	BH52	VSS_NCTF17		
			BH53	VSS_NCTF18		
94 6		PCH_VSS_NCTF<19>	BJ1	VSS_NCTF19		
			BJ2	VSS_NCTF20		
94 6		PCH_VSS_NCTF<21>	BJ4	VSS_NCTF21		
94		PCH_VSS_NCTF<22>	BJ49	VSS_NCTF22		
			BJ5	VSS_NCTF23		
			BJ50	VSS_NCTF24		
94 6		PCH_VSS_NCTF<25>	BJ52	VSS_NCTF25		
			BJ53	VSS_NCTF26		
94 6		PCH_VSS_NCTF<27>	D1	VSS_NCTF27		
			D2	VSS_NCTF28		
94 6		PCH_VSS_NCTF<29>	D53	VSS_NCTF29		
			E1	VSS_NCTF30		
			E53	VSS_NCTF31		

NCTF

RSVD

CPU

			CLKOUT_PCIE6N	AH45	NC_PCIE_CLK100M_PE6N	6
			CLKOUT_PCIE6P	AH46	NC_PCIE_CLK100M_PE6P	6
			CLKOUT_PCIE7N	AF48	NC_PCIE_CLK100M_PE7N	6
			CLKOUT_PCIE7P	AF47	NC_PCIE_CLK100M_PE7P	6
			A20GATE	U2	PCH_A20GATE	
			CLKOUT_BCLK0_N/CLKOUT_PCIE8N	AM3	FSB_CLK133M_CPU_N	OUT 10 91
			CLKOUT_BCLK0_P/CLKOUT_PCIE8P	AM1	FSB_CLK133M_CPU_P	OUT 10 91
			PECI	BG10	CPU_PECI	BI 10 91
			RCIN*	T1	PCH_RCIN_L	
			PROCPWRGD	BE10	CPU_PWRGD	OUT 10 25 91
			THRMTRIP*	BD10	PCH_THRMTRIP_L	
			TP1	BA22	NC_PCH_TP1	6
			TP2	AW22	NC_PCH_TP2	6
			TP3	BB22	NC_PCH_TP3	6
			TP4	AY45	NC_PCH_TP4	6 (DPL_B_MON1_N)
			TP5	AY46	NC_PCH_TP5	6 (DPL_B_MON1_P)
			TP6	AV43	NC_PCH_TP6	6 (DPL_B_MON2_N)
			TP7	AV45	NC_PCH_TP7	6 (DPL_B_MON2_P)
			TP8	AF13	NC_PCH_TP8	6 (SATA_OB_ANA)
			TP9	M18	NC_PCH_TP9	6
			TP10	N18	NC_PCH_TP10	6
			TP11	AJ24	NC_PCH_TP11	6
			TP12	AK41	NC_PCH_TP12	6 (XCKPLL_MON1_N)
			TP13	AK42	NC_PCH_TP13	6 (XCKPLL_MON1_P)
			TP14	M32	NC_PCH_TP14	6
			TP15	N32	NC_PCH_TP15	6
			TP16	M30	NC_PCH_TP16	6
			TP17	N30	NC_PCH_TP17	6
			TP18	H12	NC_PCH_TP18	6
			TP19	AA23	NC_PCH_TP19	6
			NC_1	AB45	NC_PCH_NC1	6
			NC_2	AB38	NC_PCH_NC2	6
			NC_3	AB42	NC_PCH_NC3	6
			NC_4	AB41	NC_PCH_NC4	6
			NC_5	T39	NC_PCH_NC5	6
(IPD)		INIT3_3V*	P6		TP_PCH_INIT3V3_L	
			TP24	C10	NC_PCH_SST	6

PP3V3_S0 — 50 51 52 54 58 62 63 68 69 72 8 7 17 18 19 20 21 23 24 25 26 27 28 30 34 37 40 42 45 47 48 73 80 83 84 85 87 88 99

R2150 10K 5% 1/16W MF-LF 402 (1–2)
R2155 10K 5% 1/16W MF-LF 402 (1–2)

PP1V05_S0 — 6 7 10 12 13 15 17 18 21 23 24 25 26 40 70 73 86

R2160 56 5% 1/16W MF-LF 402 (1–2)
R2161 56 5% 1/16W MF-LF 402 (1–2)
PM_THRMTRIP_L — IN 10 46 91

PP3V3_S5
PP3V3_S3
PP3V3_S0

R2110	10K	5% 1/16W MF-LF 402	SMC_IG_THROTTLE_L	20 25 45 46
R2111	10K	5% 1/16W MF-LF 402	FW_PLUG_DET_L	8 20 40
R2112	20K	5% 1/16W MF-LF 402	GMUX_INT	20 87
R2113	10K	5% 1/16W MF-LF 402	SMC_RUNTIME_SCI_L	20 45
R2114	10K	5% 1/16W MF-LF 402	PCH_FCIM_EN_L	20
R2115	2.2K	5% 1/16W MF-LF 402	ENET_LOW_PWR	20 37
R2116	10K	5% 1/16W MF-LF 402	PCH_GPIO15	20
R2120	10K	5% 1/16W MF-LF 402	AUD_IPHS_SWITCH_EN	20 25 63
R2121	10K	5% 1/16W MF-LF 402	LPCPLUS_GPIO	6 20 47
R2122	10K	5% 1/16W MF-LF 402	ODD_PWR_EN_L	20 42
R2123	10K	5% 1/16W MF-LF 402	PCH_GPIO24	20
R2124	10K	5% 1/16W MF-LF 402	PCH_VRM_EN	20
R2130	10K	5% 1/16W MF-LF 402	MXM_GOOD	20
R2131	10K	5% 1/16W MF-LF 402	SDCARD_RESET	20 25 34
R2132	10K	5% 1/16W MF-LF 402	JTAG_GMUX_TCK	20 25 87
R2133	10K	5% 1/16W MF-LF 402	JTAG_GMUX_TDO	20 87
R2134	10K	5% 1/16W MF-LF 402	PCH_GPIO39	20
R2135	10K	5% 1/16W MF-LF 402	WOL_EN	20 73
R2136	10K	5% 1/16W MF-LF 402	AP_PWR_EN	20 33 73
R2137	10K	5% 1/16W MF-LF 402	FW_PWR_EN	20 40
R2138	10K	5% 1/16W MF-LF 402	ME_TEMP_ALERT_L	20 25
R2139	100K	5% 1/16W MF-LF 402	SPIROM_USE_MLB	6 20 47 57

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CLOCK AND MISCELLANEOUS

PP1V05_S0_PCH_VCCA_CLK → AP51 VCCACLK1, AP53 VCCACLK2
52 mA

GND → AF23 VCCLAN1, AF24 VCCLAN2
320 mA S0, 67 mA M-on

PCH output, for decoupling only
PPVOUT_S5_PCH_DCPSUSBYP → Y20 DCPSUSBYP
MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.05V
C2200 0.1UF 20% 10V CERM 402
PLACE_NEAR=U1800.Y20:2.54MM

PP1V05_S0 → AD38 VCCME1, AD39 VCCME2, AD41 VCCME3, AF43 VCCME4, AF41 VCCME5, AF42 VCCME6, V39 VCCME7, V41 VCCME8, V42 VCCME9, Y39 VCCME10, Y41 VCCME11, Y42 VCCME12
1849 mA S0, 700 mA M-on
(VCCME[1-16] total)

PCH output, for decoupling only
PPVOUT_G3_PCH_DCPRTC → V9 DCPRTC
MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=X.XV
C2210 0.1UF 20% 10V CERM 402
PLACE_NEAR=U1800.V9:2.54MM

PP1V8_S0 → AU24 VCCVRM3
164 mA (VCCVRM[1-4] total)

PP1V05_S0_PCH_VCCADPLLA → BB51 VCCADPLLA1, BB53 VCCADPLLA2
68 mA

PP1V05_S0_PCH_VCCADPLLB → BD51 VCCADPLLB1, BD53 VCCADPLLB2
69 mA

PP1V05_S0 → AH23 VCCIO21, AJ35 VCCIO22, AH35 VCCIO23
3062 mA (VCCIO[1-56] total)

R2225 0.2 1% 1/8W MF 402-HF
C2225 4.7UF 20% 4V X5R 402
MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.1 mm VOLTAGE=1.05V
PLACE_NEAR=U1800.V12:2.54MM
PP1V05_S0_PCH_VCCIO_SSC_FLT → AE34 VCCIO2, AH34 VCCIO3, AE32 VCCIO4
115 mA

PCH output, for decoupling only
PPVOUT_S0_PCH_DCPSST → V12 DCPSST
MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=X.XV
C2220 0.1UF 20% 10V CERM 402

PCH output, for decoupling only
PPVOUT_S5_PCH_DCPSUS → Y22 DCPSUS
MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=X.XV
C2230 0.1UF 20% 10V CERM 402
PLACE_NEAR=U1800.Y22:2.54MM

PCI/GPIO/LPC

PP3V3_S5 → P18 VCCSUS3_3_29, U19 VCCSUS3_3_30, U20 VCCSUS3_3_31, U22 VCCSUS3_3_32
163 mA S0, 65 mA S3-S5
(VCCSUS3_3[1-32] total)

PP3V3_S0 → V15 VCC3_3_5, V16 VCC3_3_6, Y16 VCC3_3_7
357 mA
(VCC3_3[1-14] total)

SATA

PP1V05_S0 → AH19 VCCIO10, AD20 VCCIO11, AF22 VCCIO12, AD19 VCCIO13, AF20 VCCIO14, AF19 VCCIO15, AH20 VCCIO16, AB19 VCCIO17, AB20 VCCIO18, AB22 VCCIO19, AD22 VCCIO20
3062 mA (VCCIO[1-56] total)

PP1V8_S0 → AT20 VCCVRM4
164 mA (VCCVRM[1-4] total)

GPIO27	HDA_SYNC	VccVRM	PLLs
1 (IPU)	0 (IPD)	1.8V	Float
1 (IPU)	1	1.5V	Float
0	X	1.05V	1.05V

Note: 1.5V option consumes more current than 1.8V
PLLs = VccAClk, VccSATAPLL, VccAPLLEXP & VccFDIPLL

CPU

PP1V05_S0 → AT18 V_CPU_IO1, AU18 V_CPU_IO2
< 1 mA

RTC

PP3V42_G3H → A12 VCCRTC
2 mA S0-S5, ~6 uA G3

HDA

PP3V3_S0 → L30 VCCSUSHDA
6 mA S0, < 1 mA S3-S5

USB

PP1V05_S0 → V24 VCCIO5, V26 VCCIO6, Y24 VCCIO7, Y26 VCCIO8
3062 mA (VCCIO[1-56] total)

PP3V3_S5 → V28 VCCSUS3_3_1, U28 VCCSUS3_3_2, U26 VCCSUS3_3_3, U24 VCCSUS3_3_4, P28 VCCSUS3_3_5, P26 VCCSUS3_3_6, N28 VCCSUS3_3_7, N26 VCCSUS3_3_8, M28 VCCSUS3_3_9, M26 VCCSUS3_3_10, L28 VCCSUS3_3_11, L26 VCCSUS3_3_12, J28 VCCSUS3_3_13, J26 VCCSUS3_3_14, H28 VCCSUS3_3_15, H26 VCCSUS3_3_16, G28 VCCSUS3_3_17, G26 VCCSUS3_3_18, F28 VCCSUS3_3_19, F26 VCCSUS3_3_20, E28 VCCSUS3_3_21, E26 VCCSUS3_3_22, C28 VCCSUS3_3_23, C26 VCCSUS3_3_24, B27 VCCSUS3_3_25, A28 VCCSUS3_3_26, A26 VCCSUS3_3_27, U23 VCCSUS3_3_28
163 mA S0, 65 mA S3-S5
(VCCSUS3_3[1-32] total)

PP1V05_S0 → V23 VCCIO56
3062 mA (VCCIO[1-56] total)

PP5V_S5_PCH_V5REFSUS → F24 V5REF_SUS
< 1 mA S0-S5

PP5V_S0_PCH_V5REF → K49 V5REF
< 1 mA

PP3V3_S0 → J38 VCC3_3_8, L38 VCC3_3_9, M36 VCC3_3_10, N36 VCC3_3_11, P36 VCC3_3_12, U35 VCC3_3_13
357 mA
(VCC3_3[1-14] total)

PP3V3_S0 → AD13 VCC3_3_14
357 mA (VCC3_3[1-14] total)

PP1V05_S0_PCH_VCCAPLL_SATA → AK3 VCCSATAPLL1, AK1 VCCSATAPLL2
31 mA (if GPIO27 is low)

PP1V05_S0 → AH22 VCCIO9
3062 mA (VCCIO[1-56] total)

PP1V05_S0 → AA34 VCCME13, Y34 VCCME14, Y35 VCCME15, AA35 VCCME16
1849 mA S0, 700 mA M-on
(VCCME[1-16] total)

PP3V3_S0 → L30 VCCSUSHDA
6 mA S0, < 1 mA S3-S5
Verify S0 okay

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VCC CORE

PP1V05_S0 → AB24 VCCCORE1, AB26 VCCCORE2, AB28 VCCCORE3, AD26 VCCCORE4, AD28 VCCCORE5, AF26 VCCCORE6, AF28 VCCCORE7, AF30 VCCCORE8, AF31 VCCCORE9, AH26 VCCCORE10, AH28 VCCCORE11, AH30 VCCCORE12, AH31 VCCCORE13, AJ30 VCCCORE14, AJ31 VCCCORE15
1432 mA

PP1V05_S0 → AK24 VCCIO24
3062 mA (VCCIO[1-56] total)

PP1V05_S0_PCH_VCCAPLL_EXP → BJ24 VCCAPLLEXP
40 mA (if GPIO27 is low)

PP1V05_S0 → AN20 VCCIO25, AN22 VCCIO26, AN23 VCCIO27, AN24 VCCIO28, AN26 VCCIO29, AN28 VCCIO30, BJ26 VCCIO31, BJ28 VCCIO32, AT26 VCCIO33, AT28 VCCIO34, AU26 VCCIO35, AU28 VCCIO36, AV26 VCCIO37, AV28 VCCIO38, AW26 VCCIO39, AW28 VCCIO40, BA26 VCCIO41, BA28 VCCIO42, BB26 VCCIO43, BB28 VCCIO44, BC26 VCCIO45, BC28 VCCIO46, BD26 VCCIO47, BD28 VCCIO48, BE26 VCCIO49, BE28 VCCIO50, BG26 VCCIO51, BG28 VCCIO52, BH27 VCCIO53, AN30 VCCIO54, AN31 VCCIO55
3062 mA
(VCCIO[1-56] total)

PCI-E*

PP3V3_S0 → AN35 VCC3_3_1
357 mA (VCC3_3[1-14] total)

PP1V8_S0 → AT22 VCCVRM1
164 mA (VCCVRM[1-4] total)

PP1V05_S0_PCH_VCCAPLL_FDI → BJ18 VCCFDIPLL
5 mA (if GPIO27 is low)

PP1V05_S0 → AM23 VCCIO1
3062 mA (VCCIO[1-56] total)

FDI

CRT

PP3V3_S0_PCH_VCCA_DAC → AE50 VCCADAC1, AE52 VCCADAC2
69 mA

VSSA_DAC1 AE53, VSSA_DAC2 AF51

LVDS

PP3V3_S0 → AH38 VCCALVDS
< 1 mA

VSSA_LVDS AH39

PP1V8_S0_PCH_VCCTX_LVDS → AP43 VCCTX_LVDS1, AP45 VCCTX_LVDS2, AT46 VCCTX_LVDS3, AT45 VCCTX_LVDS4
59 mA

HVCMOS

PP3V3_S0 → AB34 VCC3_3_2, AB35 VCC3_3_3, AD35 VCC3_3_4
357 mA
(VCC3_3[1-14] total)

DMI

PP1V8_S0 → AT24 VCCVRM2
164 mA (VCCVRM[1-4] total)

PP1V05_S0 → AT16 VCCDMI1, AU16 VCCDMI2
61 mA (1.1V)
58 mA (1.05V)

NAND / SPI

PP1V8_S0 → AM16 VCCPNAND1, AK16 VCCPNAND2, AK20 VCCPNAND3, AK19 VCCPNAND4, AK15 VCCPNAND5, AK13 VCCPNAND6, AM12 VCCPNAND7, AM13 VCCPNAND8, AM15 VCCPNAND9
156 mA (1.8V)
NOTE: Connect to 3.3V if NAND not used.

PP3V3_S0 → AM8 VCCME3_3_1, AM9 VCCME3_3_2, AP11 VCCME3_3_3, AP9 VCCME3_3_4
85 mA S0, 22 mA M-on

Current numbers from Ibex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

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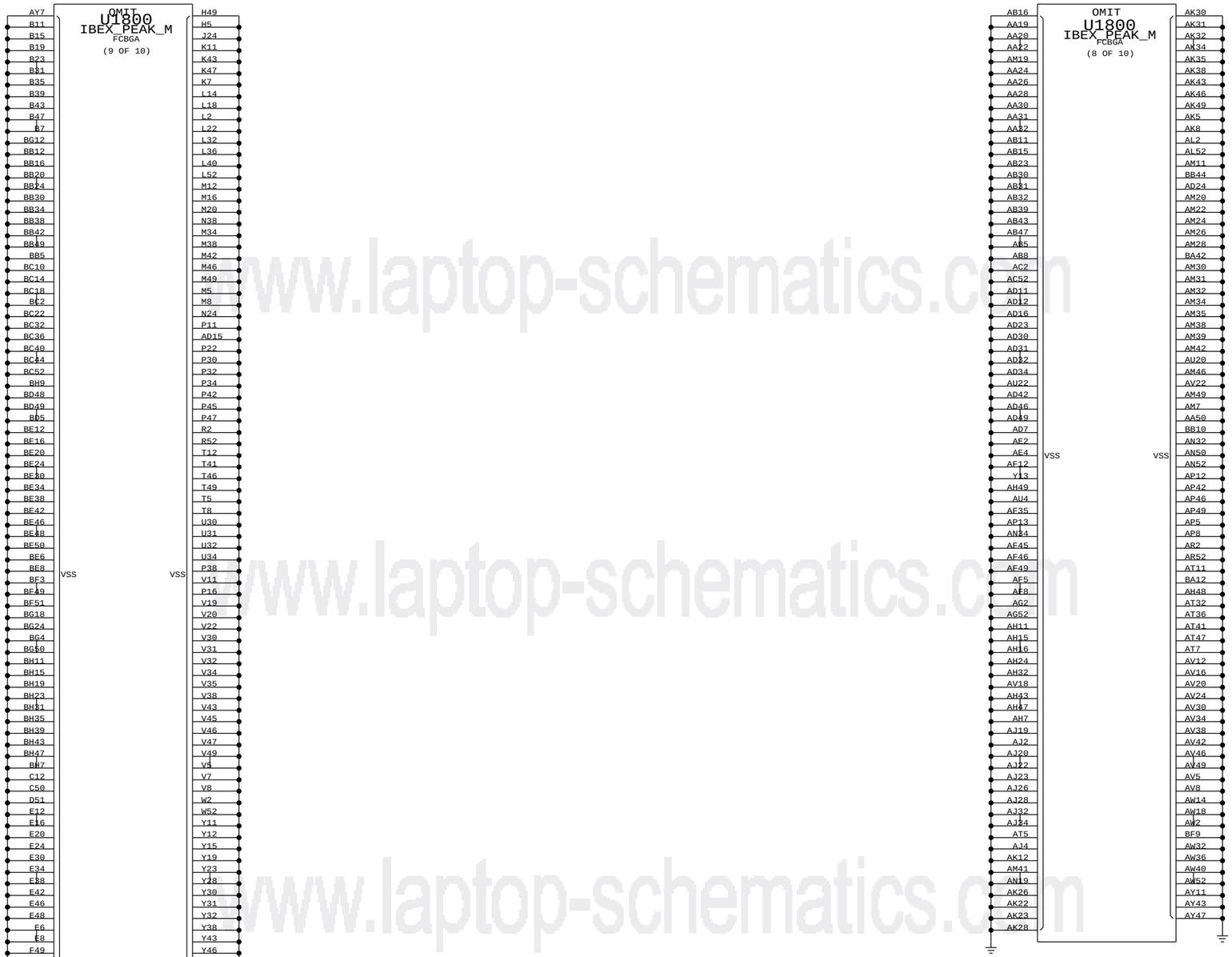

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PP3V3_S5
PP5V_S5
1 mA S0-S5
R2400 10 5% 1/16W MF-LF 402
D2400 BAT54DW-X-G SOT-363
PCH V5REF_SUS Filter & Follower
(PCH Reference for 5V Tolerance on USB)
PP5V_S5_PCH_V5REFSUS
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=5V
1 mA S0-S5
C2400 1UF 10% 10V X5R 402
PLACE_NEAR=U1800.F24:2.54MM

PP3V3_S0
PP5V_S0
1 mA
R2401 100 5% 1/16W MF-LF 402
D2400 BAT54DW-X-G SOT-363
PCH V5REF Filter & Follower
(PCH Reference for 5V Tolerance on PCI)
PP5V_S0_PCH_V5REF
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=5V
1 mA
C2401 1UF 10% 10V X5R 402
PLACE_NEAR=U1800.K49:2.54MM

PCH VCCRTC BYPASS
(PCH RTC 3.3V PWR)
PP3V42_G3H
2 mA S0-S5 /
6 uA G3
C2420 1UF 10% 6.3V CERM 402
C2421 0.1UF 10% 16V X5R 402
C2422 0.1UF 10% 16V X5R 402
PLACE_NEAR=U1800.A12:2.54MM

PCH VCCSUS3_3 BYPASS
(PCH SUSPEND PCI 3.3V PWR)
PP3V3_S5
C2425 0.1UF 10% 16V X5R 402
PLACE_NEAR=U1800.P18:2.54MM

163 mA S0 /
65 mA S3-S5
(VCCSUS3_3 Total)
PCH USB/VCCSUS3_3 BYPASS
(PCH SUSPEND USB 3.3V PWR)
PP3V3_S5
C2426 0.1UF 10% 16V X5R 402
C2427 0.1UF 10% 16V X5R 402
PLACE_NEAR=U1800.A26:2.54MM
PLACE_NEAR=U1800.U23:2.54MM

PCH VCCME3_3 BYPASS
(PCH ME 3.3V PWR)
PP3V3_S0
C2430 0.1UF 10% 16V X5R 402
PLACE_NEAR=U1800.AM8:2.54MM

PCH CORE/VCC3_3 BYPASS
(PCH MISC 3.3V PWR)
PP3V3_S0
C2435 0.1UF 10% 16V X5R 402
PLACE_NEAR=U1800.V15:2.54MM

PCH VCCAPLLEXP Filter
(PCH PCIe PLL PWR)
PP1V05_S0_PCH_VCCAPLL_EXP
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.05V
OMIT_WF: C2311 not in DG or CRB
C2413 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.BJ24:2.54MM

PCH VCC3_3 BYPASS
(PCH PCI 3.3V PWR)
PP3V3_S0
C2436 0.1UF 10% 16V X5R 402
PLACE_NEAR=U1800.J38:2.54MM

PCH VCCFDIPLL Filter
(PCH FDI PLL PWR)
PP1V05_S0_PCH_VCCAPLL_FDI
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.05V
OMIT_WF: C2413 not in DG or CRB
C2415 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.BJ18:2.54MM

PCH VCC3_3 BYPASS
(PCH SATA 3.3V PWR)
PP3V3_S0
C2437 0.1UF 10% 16V X5R 402
PLACE_NEAR=U1800.AD13:2.54MM

PCH VCCSATAPLL Filter
(PCH SATA PLL PWR)
PP1V05_S0_PCH_VCCAPLL_SATA
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.05V
BB: C2417 removed from DG
NO STUFF
C2417 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AK1:2.54MM

PCH VCC3_3 BYPASS
(PCH PCIe/DMI 3.3V PWR)
PP3V3_S0
C2438 0.1UF 10% 16V X5R 402
PLACE_NEAR=U1800.AN35:2.54MM

PCH VCCACLK Filter
(PCH Misc PLL PWR)
PP1V05_S0_PCH_VCCA_CLK
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.05V
BB: C2419 removed from DG
NO STUFF
C2419 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AP51:2.54MM

PCH VCC3_3 BYPASS
(PCH CLK/HVCMOS 3.3V PWR)
PP3V3_S0
C2439 0.1UF 10% 16V X5R 402
PLACE_NEAR=U1800.AB34:2.54MM

PCH VCCPNAND BYPASS
(PCH NAND 1.8V/3.3V PWR)
PP1V8_S0
C2440 0.1UF 10% 16V X5R 402
PLACE_NEAR=U1800.AK13:2.54MM

PCH VCCSUSHDA BYPASS
(PCH HD Audio 3.3V/1.5V PWR)
PP3V3_S0
C2445 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.L30:2.54MM

PCH V_CPU_IO BYPASS
(PCH 1.1V/1.05V CPU I/O PWR)
PP1V05_S0
C2450 4.7UF 20% 6.3V X5R 603
C2451 0.1UF 10% 16V X5R 402
C2452 0.1UF 10% 16V X5R 402
PLACE_NEAR=U1800.AT18:2.54MM
PLACE_NEAR=U1800.AT18:2.54MM
PLACE_NEAR=U1800.AT18:2.54MM

PCH VCCIO BYPASS
(PCH DMI 1.05V PWR)
PP1V05_S0
C2455 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AT16:2.54MM

PCH VCCLAN BYPASS
(PCH 1.05V LAN Core PWR)
GND
NO STUFF
C2460 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AF23:2.54MM

PCH VCCME BYPASS
(PCH 1.05V ME Core PWR)
PP1V05_S0
C2465 22UF 20% 6.3V X5R-CERM 603
C2466 22UF 20% 6.3V X5R-CERM 603
C2467 22UF 20% 6.3V X5R-CERM 603
C2468 1UF 10% 6.3V CERM 402
C2469 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AD38:2.54MM
PLACE_NEAR=U1800.V39:2.54MM
PLACE_NEAR=U1800.AD38:2.54MM
PLACE_NEAR=U1800.AD38:2.54MM
PLACE_NEAR=U1800.V39:2.54MM
PLACE_NEAR=U1800.AD38:2.54MM

PCH VCCCORE BYPASS
(PCH 1.05V CORE PWR)
PP1V05_S0
C2470 10UF 20% 6.3V X5R 603
C2471 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AB24:2.54MM
PLACE_NEAR=U1800.AB24:2.54MM

PCH VCCIO BYPASS
(PCH CLK 1.05V PWR)
PP1V05_S0
C2475 1UF 10% 6.3V CERM 402
C2476 1UF 10% 6.3V CERM 402
C2477 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AF32:2.54MM
PLACE_NEAR=U1800.AH23:2.54MM
PLACE_NEAR=U1800.AH23:2.54MM
PLACE_NEAR=U1800.AH35:2.54MM

PCH VCCIO BYPASS
(PCH USB 1.05V PWR)
PP1V05_S0
C2480 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.V24:2.54MM

PCH VCCIO BYPASS
(PCH SATA 1.05V PWR)
PP1V05_S0
C2485 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AB19:2.54MM

PCH VCCIO BYPASS
(PCH PCIE 1.05V PWR)
PP1V05_S0
C2490 10UF 20% 6.3V X5R 603
C2491 1UF 10% 6.3V CERM 402
C2492 1UF 10% 6.3V CERM 402
C2493 1UF 10% 6.3V CERM 402
C2494 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AN20:2.54MM
PLACE_NEAR=U1800.AN20:2.54MM
PLACE_NEAR=U1800.AN20:2.54MM
PLACE_NEAR=U1800.AN20:2.54MM

Current numbers from Ibex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

SYNC_MASTER=K17_REF
SYNC_DATE=06/15/2009

PAGE TITLE
PCH Non-GFX Decoupling

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 24 OF 132
SHEET 23 OF 101

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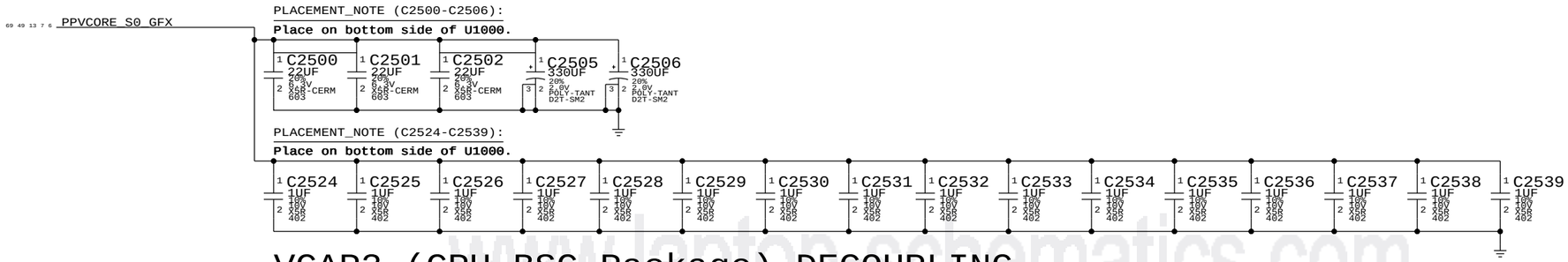
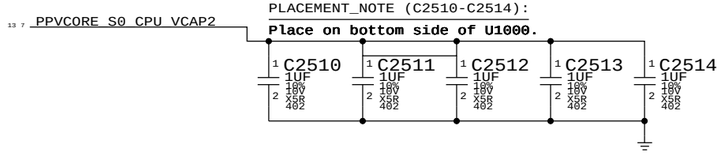
GFX (CPU VCCAXG) DECOUPLING

3x 330uF 6 mOhm (2 stuffed), 3x 22uF 0603, 16x 1uF 0402

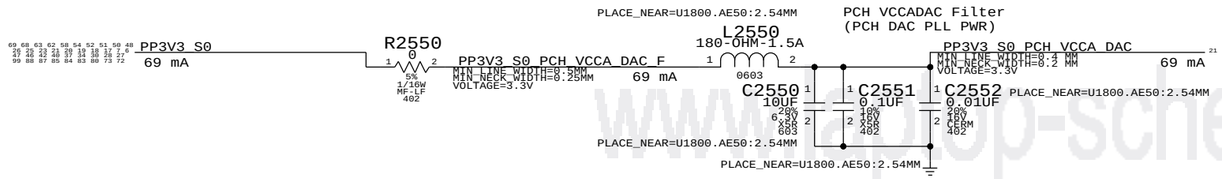


VCAP2 (CPU BSC Package) DECOUPLING

5x 1uF 0402



Design recommendations from Calpella Small Form Factor Design Guide Rev 1.5 (doc #407364) table 2-34 and Calpella Small Form F actor Schematic Check List Rev 1.1 (doc #395914) table 3.26.



Design recommendations from Calpella Design Guide Rev 1.5 (doc #398905) Section 3.25.3 tables 161 and 162.

Current numbers from Ibex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

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SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: CPU/PCH GFX Decoupling

Apple Inc.

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REVISION: <E4LABEL>

BRANCH: <BRANCH>

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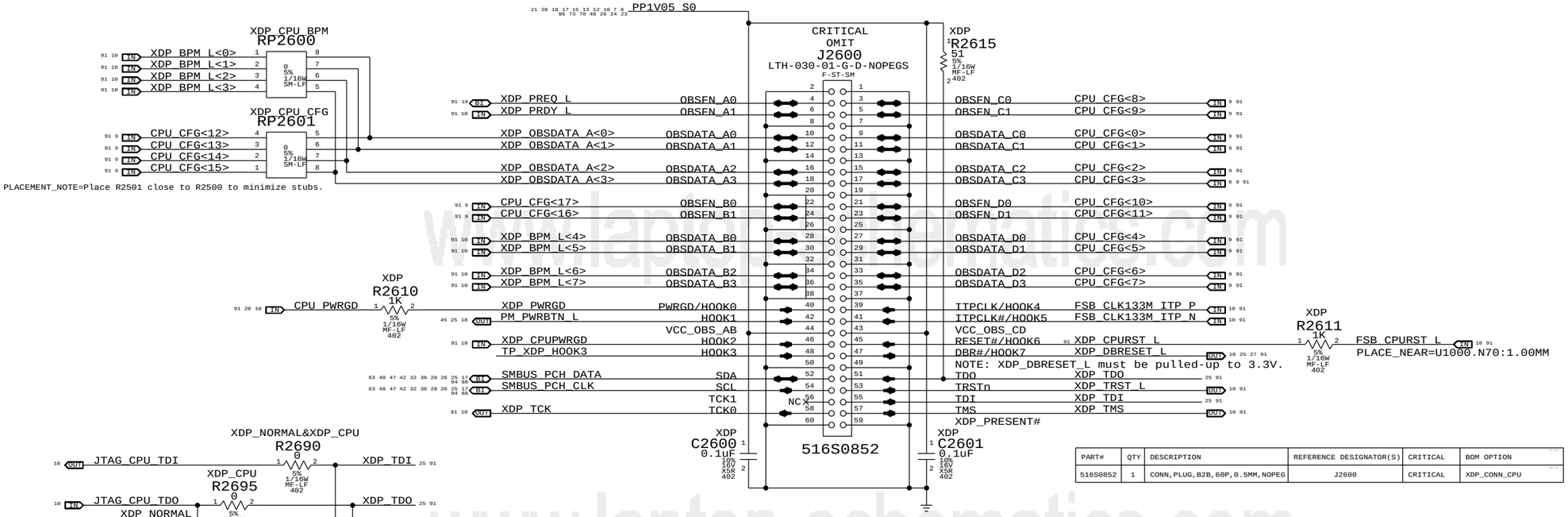
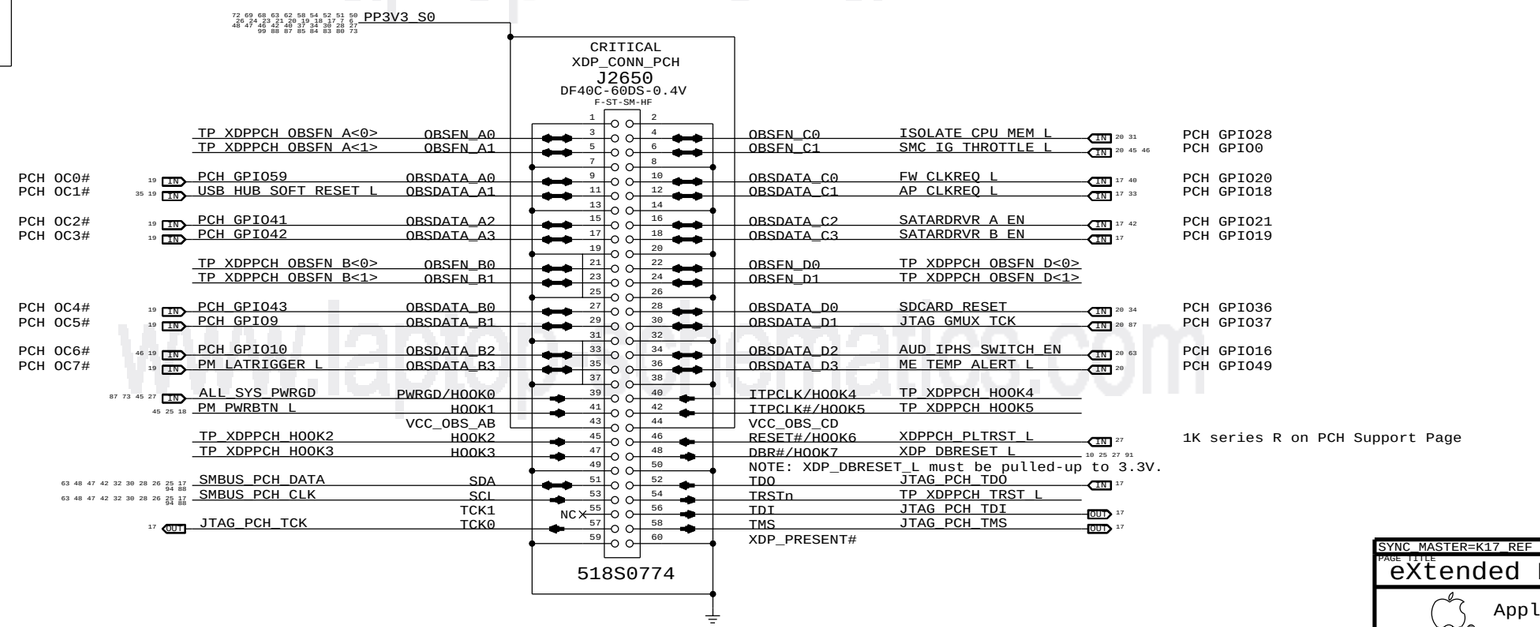
Calpella Processor mini XDP



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0852	1	CONN,PLUG,B2B,60P,0.5MM,NOPEG	J2600	CRITICAL	XDP_CONN_CPU

Calpella PCH mini XDP



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SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE

eXtended Debug Port (XDP)

Apple Inc.

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REVISION <E4LABEL>

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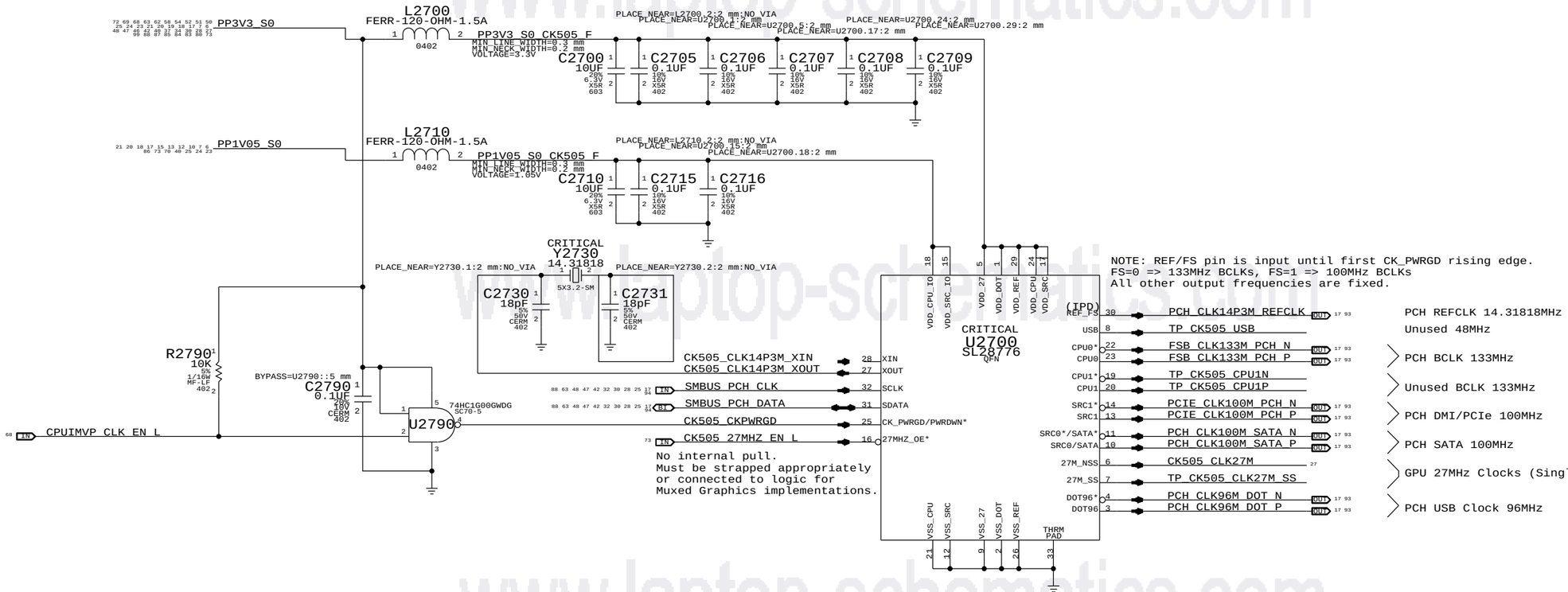

NOTE: REF/FS pin is input until first CK_PWRGD rising edge.
FS=0 => 133MHz BCLKs, FS=1 => 100MHz BCLKs
All other output frequencies are fixed.

- PCH REFCLK 14.31818MHz
- Unused 48MHz
- PCH BCLK 133MHz
- Unused BCLK 133MHz
- PCH DMI/PCIe 100MHz
- PCH SATA 100MHz
- GPU 27MHz Clocks (Single-Ended)
- PCH USB Clock 96MHz

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SYNC_MASTER=K17_MLB SYNC_DATE=06/23/2009

PAGE TITLE: Clock (CK505)

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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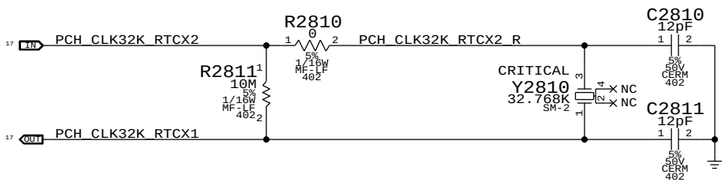
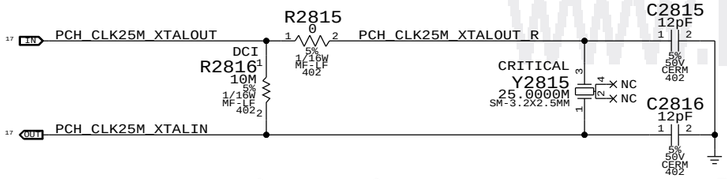
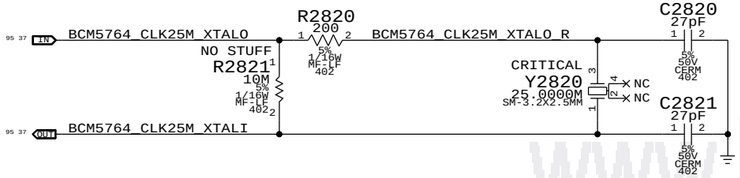
PCH RTC Crystal



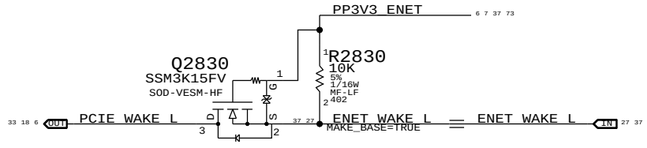
PCH 25MHz Crystal



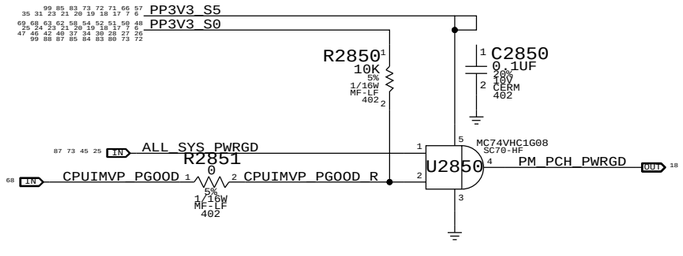
Caesar II (ENET) 25MHz Crystal



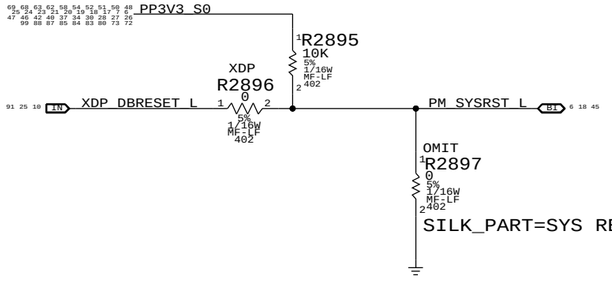
Ethernet WAKE# Isolation



PCH S0 PWRGD

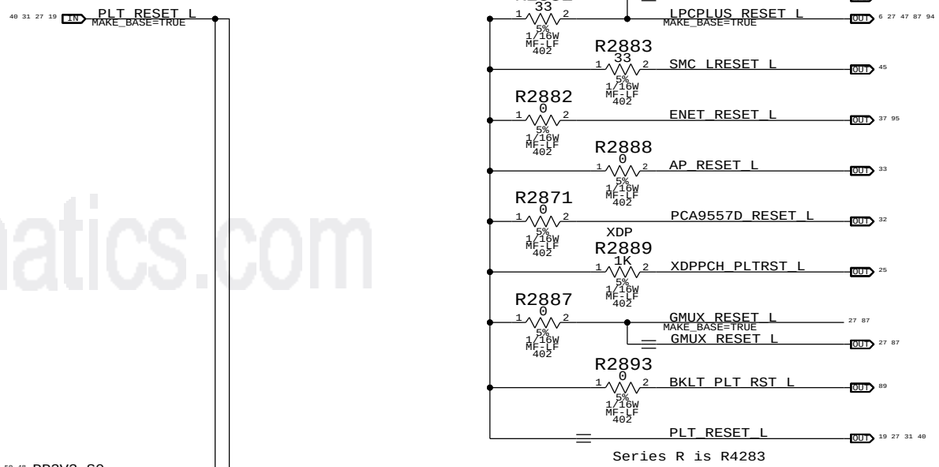


PCH Reset Button



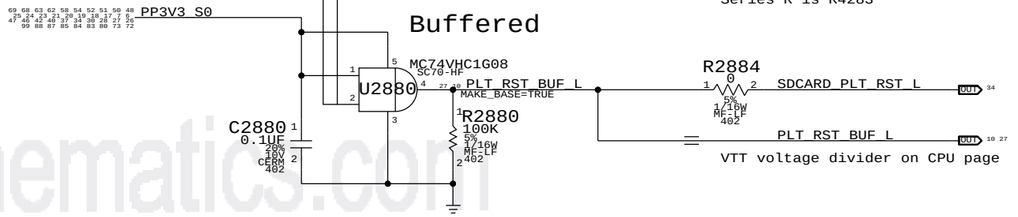
Platform Reset Connections

Unbuffered

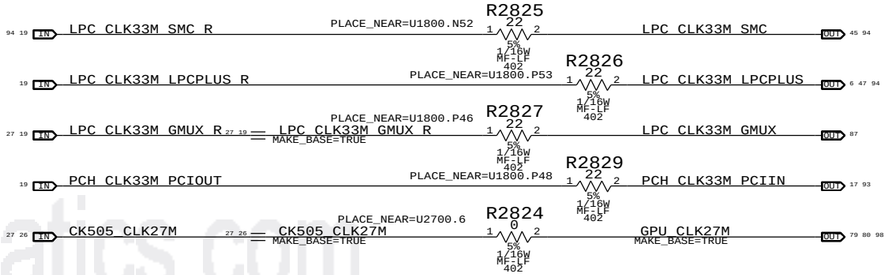


Series R is R4283

Buffered



VTT voltage divider on CPU page



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SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: Chipset Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

PP1V5_S3

C2900 10UF 20% 6.3V X6S CERM 603
C2901 10UF 20% 6.3V X6S CERM 603
C2910 0.1UF 20% 10V CERM 402
C2911 0.1UF 20% 10V CERM 402
C2912 0.1UF 20% 10V CERM 402
C2913 0.1UF 20% 10V CERM 402
C2914 0.1UF 20% 10V CERM 402
C2915 0.1UF 20% 10V CERM 402
C2916 0.1UF 20% 10V CERM 402
C2917 0.1UF 20% 10V CERM 402
C2918 0.1UF 20% 10V CERM 402
C2919 0.1UF 20% 10V CERM 402
C2920 0.1UF 20% 10V CERM 402
C2921 0.1UF 20% 10V CERM 402
C2922 0.1UF 20% 10V CERM 402
C2923 0.1UF 20% 10V CERM 402

PP0V75_S3_MEM_VREFDQ_A

C2930 2.2UF 20% 6.3V CERM 402-LF
C2931 0.1UF 20% 10V CERM 402

J2900 DDR3-SODIMM-DUAL-K6 (SYMBOL 2 OF 2) F-RT-THB

MEM_A_CKE<0>	73 CKE0	CKE1 74	MEM_A_CKE<1>
NC	75 VDD	VDD 76	
MEM_A_BA<2>	77 NC	A15 78	MEM_A_A<15>
	79 BA2	A14 80	MEM_A_A<14>
MEM_A_A<12>	81 VDD	VDD 82	
MEM_A_A<9>	83 A12/BC*	A11 84	MEM_A_A<11>
	85 A9	A7 86	MEM_A_A<7>
MEM_A_A<8>	87 VDD	VDD 88	
MEM_A_A<5>	89 A8	A6 90	MEM_A_A<6>
	91 A5	A4 92	MEM_A_A<4>
MEM_A_A<3>	93 VDD	VDD 94	
MEM_A_A<1>	95 A3	A2 96	MEM_A_A<2>
	97 A1	A0 98	MEM_A_A<0>
MEM_A_CLK_P<0>	99 VDD	VDD 100	
MEM_A_CLK_N<0>	101 CK0	CK1 102	MEM_A_CLK_P<1>
	103 CK0*	CK1* 104	MEM_A_CLK_N<1>
MEM_A_A<10>	105 VDD	VDD 106	
MEM_A_BA<0>	107 A10/AP	BA1 108	MEM_A_BA<1>
	109 BA0	RAS* 110	MEM_A_RAS_L
MEM_A_WE_L	111 VDD	VDD 112	
MEM_A_CAS_L	113 WE*	S0* 114	MEM_A_CS_L<0>
	115 CAS*	ODT0 116	MEM_A_ODT<0>
MEM_A_A<13>	117 VDD	VDD 118	
MEM_A_CS_L<1>	119 A13	ODT1 120	MEM_A_ODT<1>
	121 S1*	NC 122	NC
	123 VDD	VDD 124	
NC	125 TEST	VREFCA 126	
	127 VSS	VSS 128	
=MEM_A_DQ<32>	129 DQ32	DQ36 130	=MEM_A_DQ<36>
=MEM_A_DQ<33>	131 DQ33	DQ37 132	MEM_A_DQ<37>
	133 VSS	VSS 134	
=MEM_A_DQS_N<4>	135 DQS4*	DM4 136	=MEM_A_DM<4>
=MEM_A_DQS_P<4>	137 DQS4	VSS 138	
	139 VSS	DQ38 140	=MEM_A_DQ<38>
=MEM_A_DQ<34>	141 DQ34	DQ39 142	=MEM_A_DQ<39>
=MEM_A_DQ<35>	143 DQ35	VSS 144	
	145 VSS	DQ44 146	=MEM_A_DQ<44>
=MEM_A_DQ<40>	147 DQ40	DQ45 148	=MEM_A_DQ<45>
=MEM_A_DQ<41>	149 DQ41	VSS 150	
	151 VSS	DQS5* 152	=MEM_A_DQS_N<5>
=MEM_A_DM<5>	153 DM5	DQS5 154	=MEM_A_DQS_P<5>
	155 VSS	VSS 156	
=MEM_A_DQ<42>	157 DQ42	DQ46 158	=MEM_A_DQ<46>
=MEM_A_DQ<43>	159 DQ43	DQ47 160	=MEM_A_DQ<47>
	161 VSS	VSS 162	
=MEM_A_DQ<48>	163 DQ48	DQ52 164	=MEM_A_DQ<52>
=MEM_A_DQ<49>	165 DQ49	DQ53 166	=MEM_A_DQ<53>
	167 VSS	VSS 168	
=MEM_A_DQS_N<6>	169 DQS6*	DM6 170	=MEM_A_DM<6>
=MEM_A_DQS_P<6>	171 DQS6	VSS 172	
	173 VSS	DQ54 174	=MEM_A_DQ<54>
=MEM_A_DQ<50>	175 DQ50	DQ55 176	=MEM_A_DQ<55>
=MEM_A_DQ<51>	177 DQ51	VSS 178	
	179 VSS	DQ60 180	=MEM_A_DQ<60>
=MEM_A_DQ<56>	181 DQ56	DQ61 182	=MEM_A_DQ<61>
=MEM_A_DQ<57>	183 DQ57	VSS 184	
	185 VSS	DQS7* 186	=MEM_A_DQS_N<7>
=MEM_A_DM<7>	187 DM7	DQS7 188	=MEM_A_DQS_P<7>
	189 VSS	VSS 190	
=MEM_A_DQ<58>	191 DQ58	DQ62 192	=MEM_A_DQ<62>
=MEM_A_DQ<59>	193 DQ59	DQ63 194	=MEM_A_DQ<63>
	195 VSS	VSS 196	
MEM_A_SA<0>	197 SA0	EVENT* 198	MEM_EVENT_A_L
	199 VDDSPD	SDA 200	SMBUS_PCH_DATA
MEM_A_SA<1>	201 SA1	SCL 202	SMBUS_PCH_CLK
	203 VTT	VTT 204	PP0V75_S0_DDRVTT

516-0229
SPD ADDR=0xA0(WR)/0xA1(RD)

PP3V3_S0

C2940 2.2UF 20% 6.3V CERM 402-LF
R2940 10K 5% 1/16W MF-LF 402
R2941 10K 5% 1/16W MF-LF 402

J2900 DDR3-SODIMM-DUAL-K6 (SYMBOL 1 OF 2) F-RT-THB CRITICAL

	1 VREFDQ	VSS 2	
=MEM_A_DQ<0>	3 VSS	DQ4 4	=MEM_A_DQ<4>
=MEM_A_DQ<1>	5 DQ0	DQ5 6	=MEM_A_DQ<5>
	7 DQ1	VSS 8	
MEM_A_DM<0>	9 VSS	DQS0* 10	MEM_A_DQS_N<0>
	11 DM0	DQS0 12	MEM_A_DQS_P<0>
=MEM_A_DQ<2>	13 VSS	VSS 14	
=MEM_A_DQ<3>	15 DQ2	DQ6 16	=MEM_A_DQ<6>
	17 DQ3	DQ7 18	=MEM_A_DQ<7>
=MEM_A_DQ<8>	19 VSS	VSS 20	
=MEM_A_DQ<9>	21 DQ8	DQ12 22	=MEM_A_DQ<12>
	23 DQ9	DQ13 24	=MEM_A_DQ<13>
=MEM_A_DQS_N<1>	25 VSS	VSS 26	
=MEM_A_DQS_P<1>	27 DQS1*	DM1 28	=MEM_A_DM<1>
	29 DQS1	RESET* 30	MEM_RESET_L
=MEM_A_DQ<10>	31 VSS	VSS 32	
=MEM_A_DQ<11>	33 DQ10	DQ14 34	=MEM_A_DQ<14>
	35 DQ11	DQ15 36	=MEM_A_DQ<15>
=MEM_A_DQ<16>	37 VSS	VSS 38	
=MEM_A_DQ<17>	39 DQ16	DQ20 40	=MEM_A_DQ<20>
	41 DQ17	DQ21 42	=MEM_A_DQ<21>
=MEM_A_DQS_N<2>	43 VSS	VSS 44	
=MEM_A_DQS_P<2>	45 DQS2*	DM2 46	=MEM_A_DM<2>
	47 DQS2	VSS 48	
=MEM_A_DQ<18>	49 VSS	DQ22 50	=MEM_A_DQ<22>
=MEM_A_DQ<19>	51 DQ18	DQ23 52	=MEM_A_DQ<23>
	53 DQ19	VSS 54	
=MEM_A_DQ<24>	55 VSS	DQ28 56	=MEM_A_DQ<28>
=MEM_A_DQ<25>	57 DQ24	DQ29 58	=MEM_A_DQ<29>
	59 DQ25	VSS 60	
=MEM_A_DM<3>	61 VSS	DQS3* 62	=MEM_A_DQS_N<3>
	63 DM3	DQS3 64	=MEM_A_DQS_P<3>
=MEM_A_DQ<26>	65 VSS	VSS 66	
=MEM_A_DQ<27>	67 DQ26	DQ30 68	=MEM_A_DQ<30>
	69 DQ27	DQ31 70	=MEM_A_DQ<31>
	71 VSS	VSS 72	

516-0229

PP0V75_S3_MEM_VREFCA_A

C2935 2.2UF 20% 6.3V CERM 402-LF
C2936 0.1UF 20% 10V CERM 402

"Factory" (top) slot

www.laptop-schematics.com

SYNC_MASTER=MASTER SYNC_DATE=MASTER
PAGE TITLE: DDR3 SO-DIMM Connector A
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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CPU CHANNEL A DQS 0 -> DIMM A DQS 0

MEM_A_DQS_N<0>	MAKE_BASE=TRUE	⟷	MEM_A_DQS_N<0>	11 28 29 92 92 30 29 11	
MEM_A_DQS_P<0>	MAKE_BASE=TRUE	⟷	MEM_A_DQS_P<0>	11 28 29 92 92 30 29 11	
MEM_A_DM<0>	MAKE_BASE=TRUE	⟷	MEM_A_DM<0>	11 28 29 92 92 30 29 11	
MEM_A_DQ<7>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<7>	28	
MEM_A_DQ<6>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<6>	28	
MEM_A_DQ<5>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<1>	28	
MEM_A_DQ<4>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<0>	28	
MEM_A_DQ<3>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<2>	28	
MEM_A_DQ<2>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<3>	28	
MEM_A_DQ<1>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<5>	28	
MEM_A_DQ<0>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<4>	28	

CPU CHANNEL A DQS 1 -> DIMM A DQS 1

MEM_A_DQS_N<1>	MAKE_BASE=TRUE	⟷	=MEM_A_DQS_N<1>	28	
MEM_A_DQS_P<1>	MAKE_BASE=TRUE	⟷	=MEM_A_DQS_P<1>	28	
MEM_A_DM<1>	MAKE_BASE=TRUE	⟷	=MEM_A_DM<1>	28	
MEM_A_DQ<15>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<11>	28	
MEM_A_DQ<14>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<10>	28	
MEM_A_DQ<13>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<8>	28	
MEM_A_DQ<12>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<9>	28	
MEM_A_DQ<11>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<15>	28	
MEM_A_DQ<10>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<14>	28	
MEM_A_DQ<9>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<13>	28	
MEM_A_DQ<8>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<12>	28	

CPU CHANNEL A DQS 2 -> DIMM A DQS 2

MEM_A_DQS_N<2>	MAKE_BASE=TRUE	⟷	=MEM_A_DQS_N<2>	28
MEM_A_DQS_P<2>	MAKE_BASE=TRUE	⟷	=MEM_A_DQS_P<2>	28
MEM_A_DM<2>	MAKE_BASE=TRUE	⟷	=MEM_A_DM<2>	28
MEM_A_DQ<23>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<23>	28
MEM_A_DQ<22>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<19>	28
MEM_A_DQ<21>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<20>	28
MEM_A_DQ<20>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<22>	28
MEM_A_DQ<19>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<21>	28
MEM_A_DQ<18>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<18>	28
MEM_A_DQ<17>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<17>	28
MEM_A_DQ<16>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<16>	28

CPU CHANNEL A DQS 3 -> DIMM A DQS 3

MEM_A_DQS_N<3>	MAKE_BASE=TRUE	⟷	=MEM_A_DQS_N<3>	28
MEM_A_DQS_P<3>	MAKE_BASE=TRUE	⟷	=MEM_A_DQS_P<3>	28
MEM_A_DM<3>	MAKE_BASE=TRUE	⟷	=MEM_A_DM<3>	28
MEM_A_DQ<31>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<27>	28
MEM_A_DQ<30>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<26>	28
MEM_A_DQ<29>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<25>	28
MEM_A_DQ<28>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<24>	28
MEM_A_DQ<27>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<31>	28
MEM_A_DQ<26>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<30>	28
MEM_A_DQ<25>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<28>	28
MEM_A_DQ<24>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<29>	28

CPU CHANNEL A DQS 4 -> DIMM A DQS 4

MEM_A_DQS_N<4>	MAKE_BASE=TRUE	⟷	=MEM_A_DQS_N<4>	28	
MEM_A_DQS_P<4>	MAKE_BASE=TRUE	⟷	=MEM_A_DQS_P<4>	28	
MEM_A_DM<4>	MAKE_BASE=TRUE	⟷	=MEM_A_DM<4>	28	
MEM_A_DQ<39>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<33>	28	
MEM_A_DQ<38>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<39>	28	
MEM_A_DQ<37>	MAKE_BASE=TRUE	⟷	MEM_A_DQ<37>	11 28 29 92 92 30 29 11	
MEM_A_DQ<36>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<38>	28	
MEM_A_DQ<35>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<35>	28	
MEM_A_DQ<34>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<34>	28	
MEM_A_DQ<33>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<32>	28	
MEM_A_DQ<32>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<36>	28	

CPU CHANNEL A DQS 5 -> DIMM A DQS 5

MEM_A_DQS_N<5>	MAKE_BASE=TRUE	⟷	=MEM_A_DQS_N<5>	28	
MEM_A_DQS_P<5>	MAKE_BASE=TRUE	⟷	=MEM_A_DQS_P<5>	28	
MEM_A_DM<5>	MAKE_BASE=TRUE	⟷	=MEM_A_DM<5>	28	
MEM_A_DQ<47>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<43>	28	
MEM_A_DQ<46>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<42>	28	
MEM_A_DQ<45>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<45>	28	
MEM_A_DQ<44>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<44>	28	
MEM_A_DQ<43>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<47>	28	
MEM_A_DQ<42>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<46>	28	
MEM_A_DQ<41>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<40>	28	
MEM_A_DQ<40>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<41>	28	

CPU CHANNEL A DQS 6 -> DIMM A DQS 6

MEM_A_DQS_N<6>	MAKE_BASE=TRUE	⟷	=MEM_A_DQS_N<6>	28
MEM_A_DQS_P<6>	MAKE_BASE=TRUE	⟷	=MEM_A_DQS_P<6>	28
MEM_A_DM<6>	MAKE_BASE=TRUE	⟷	=MEM_A_DM<6>	28
MEM_A_DQ<55>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<49>	28
MEM_A_DQ<54>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<50>	28
MEM_A_DQ<53>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<54>	28
MEM_A_DQ<52>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<53>	28
MEM_A_DQ<51>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<55>	28
MEM_A_DQ<50>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<51>	28
MEM_A_DQ<49>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<48>	28
MEM_A_DQ<48>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<52>	28

CPU CHANNEL A DQS 7 -> DIMM A DQS 7

MEM_A_DQS_N<7>	MAKE_BASE=TRUE	⟷	=MEM_A_DQS_N<7>	28
MEM_A_DQS_P<7>	MAKE_BASE=TRUE	⟷	=MEM_A_DQS_P<7>	28
MEM_A_DM<7>	MAKE_BASE=TRUE	⟷	=MEM_A_DM<7>	28
MEM_A_DQ<63>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<62>	28
MEM_A_DQ<62>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<63>	28
MEM_A_DQ<61>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<56>	28
MEM_A_DQ<60>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<61>	28
MEM_A_DQ<59>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<59>	28
MEM_A_DQ<58>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<58>	28
MEM_A_DQ<57>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<57>	28
MEM_A_DQ<56>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<60>	28

CPU CHANNEL B DQS 0 -> DIMM B DQS 0

MEM_B_DQS_N<0>	MAKE_BASE=TRUE	⟷	MEM_B_DQS_N<0>	11 28 29 92 92 30 29 11	11 29 30 92
MEM_B_DQS_P<0>	MAKE_BASE=TRUE	⟷	MEM_B_DQS_P<0>	11 28 29 92 92 30 29 11	11 29 30 92
MEM_B_DM<0>	MAKE_BASE=TRUE	⟷	MEM_B_DM<0>	11 28 29 92 92 30 29 11	11 29 30 92
MEM_B_DQ<7>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<7>	30	
MEM_B_DQ<6>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<6>	30	
MEM_B_DQ<5>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<2>	30	
MEM_B_DQ<4>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<4>	30	
MEM_B_DQ<3>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<3>	30	
MEM_B_DQ<2>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<1>	30	
MEM_B_DQ<1>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<5>	30	
MEM_B_DQ<0>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<0>	30	

CPU CHANNEL B DQS 1 -> DIMM B DQS 1

MEM_B_DQS_N<1>	MAKE_BASE=TRUE	⟷	=MEM_B_DQS_N<1>	30
MEM_B_DQS_P<1>	MAKE_BASE=TRUE	⟷	=MEM_B_DQS_P<1>	30
MEM_B_DM<1>	MAKE_BASE=TRUE	⟷	=MEM_B_DM<1>	30
MEM_B_DQ<15>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<15>	30
MEM_B_DQ<14>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<14>	30
MEM_B_DQ<13>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<13>	30
MEM_B_DQ<12>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<8>	30
MEM_B_DQ<11>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<11>	30
MEM_B_DQ<10>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<10>	30
MEM_B_DQ<9>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<12>	30
MEM_B_DQ<8>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<9>	30

CPU CHANNEL B DQS 2 -> DIMM B DQS 2

MEM_B_DQS_N<2>	MAKE_BASE=TRUE	⟷	=MEM_B_DQS_N<2>	30
MEM_B_DQS_P<2>	MAKE_BASE=TRUE	⟷	=MEM_B_DQS_P<2>	30
MEM_B_DM<2>	MAKE_BASE=TRUE	⟷	=MEM_B_DM<2>	30
MEM_B_DQ<23>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<23>	30
MEM_B_DQ<22>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<18>	30
MEM_B_DQ<21>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<20>	30
MEM_B_DQ<20>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<17>	30
MEM_B_DQ<19>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<19>	30
MEM_B_DQ<18>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<22>	30
MEM_B_DQ<17>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<21>	30
MEM_B_DQ<16>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<16>	30

CPU CHANNEL B DQS 3 -> DIMM B DQS 3

MEM_B_DQS_N<3>	MAKE_BASE=TRUE	⟷	=MEM_B_DQS_N<3>	30
MEM_B_DQS_P<3>	MAKE_BASE=TRUE	⟷	=MEM_B_DQS_P<3>	30
MEM_B_DM<3>	MAKE_BASE=TRUE	⟷	=MEM_B_DM<3>	30
MEM_B_DQ<31>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<27>	30
MEM_B_DQ<30>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<26>	30
MEM_B_DQ<29>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<24>	30
MEM_B_DQ<28>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<30>	30
MEM_B_DQ<27>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<28>	30
MEM_B_DQ<26>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<29>	30
MEM_B_DQ<25>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<31>	30
MEM_B_DQ<24>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<25>	30

CPU CHANNEL B DQS 4 -> DIMM B DQS 4

MEM_B_DQS_N<4>	MAKE_BASE=TRUE	⟷	=MEM_B_DQS_N<4>	30	
MEM_B_DQS_P<4>	MAKE_BASE=TRUE	⟷	=MEM_B_DQS_P<4>	30	
MEM_B_DM<4>	MAKE_BASE=TRUE	⟷	=MEM_B_DM<4>	30	
MEM_B_DQ<39>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<35>	30	
MEM_B_DQ<38>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<38>	30	
MEM_B_DQ<37>	MAKE_BASE=TRUE	⟷	MEM_B_DQ<37>	11 29 30 92	
MEM_B_DQ<36>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<32>	30	
MEM_B_DQ<35>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<33>	30	
MEM_B_DQ<34>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<39>	30	
MEM_B_DQ<33>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<37>	30	
MEM_B_DQ<32>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<36>	30	

CPU CHANNEL B DQS 5 -> DIMM B DQS 5

MEM_B_DQS_N<5>	MAKE_BASE=TRUE	⟷	=MEM_B_DQS_N<5>	30
MEM_B_DQS_P<5>	MAKE_BASE=TRUE	⟷	=MEM_B_DQS_P<5>	30
MEM_B_DM<5>	MAKE_BASE=TRUE	⟷	=MEM_B_DM<5>	30
MEM_B_DQ<47>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<43>	30
MEM_B_DQ<46>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<43>	30
MEM_B_DQ<45>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<45>	30
MEM_B_DQ<44>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<41>	30
MEM_B_DQ<43>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<46>	30
MEM_B_DQ<42>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<42>	30
MEM_B_DQ<41>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<44>	30
MEM_B_DQ<40>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<40>	30

CPU CHANNEL B DQS 6 -> DIMM B DQS 6

MEM_B_DQS_N<6>	MAKE_BASE=TRUE	⟷	=MEM_B_DQS_N<6>	30
MEM_B_DQS_P<6>	MAKE_BASE=TRUE	⟷	=MEM_B_DQS_P<6>	30
MEM_B_DM<6>	MAKE_BASE=TRUE	⟷	=MEM_B_DM<6>	30
MEM_B_DQ<55>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<50>	30
MEM_B_DQ<54>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<55>	30
MEM_B_DQ<53>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<54>	30
MEM_B_DQ<52>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<53>	30
MEM_B_DQ<51>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<49>	30
MEM_B_DQ<50>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<51>	30
MEM_B_DQ<49>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<48>	30
MEM_B_DQ<48>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<52>	30

CPU CHANNEL B DQS 7 -> DIMM B DQS 7

MEM_B_DQS_N<7>	MAKE_BASE=TRUE	⟷	=MEM_B_DQS_N<7>	30
MEM_B_DQS_P<7>	MAKE_BASE=TRUE	⟷	=MEM_B_DQS_P<7>	30
MEM_B_DM<7>	MAKE_BASE=TRUE	⟷	=MEM_B_DM<7>	30
MEM_B_DQ<63>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<63>	30
MEM_B_DQ<62>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<62>	30
MEM_B_DQ<61>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<57>	30
MEM_B_DQ<60>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<56>	30
MEM_B_DQ<59>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<59>	30
MEM_B_DQ<58>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<58>	30
MEM_B_DQ<57>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<60>	30
MEM_B_DQ<56>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<61>	30

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: DDR3 Byte/Bit Swaps

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

72 67 31 28 7 6 PP1V5_S3

C3110 0.1UF 20% 10V CERM 402
C3111 0.1UF 20% 10V CERM 402
C3112 0.1UF 20% 10V CERM 402
C3113 0.1UF 20% 10V CERM 402
C3114 0.1UF 20% 10V CERM 402
C3115 0.1UF 20% 10V CERM 402
C3116 0.1UF 20% 10V CERM 402
C3117 0.1UF 20% 10V CERM 402
C3118 0.1UF 20% 10V CERM 402
C3119 0.1UF 20% 10V CERM 402
C3120 0.1UF 20% 10V CERM 402
C3121 0.1UF 20% 10V CERM 402
C3122 0.1UF 20% 10V CERM 402
C3123 0.1UF 20% 10V CERM 402

C3100 10UF 20% 6.3V X6S 603
C3101 10UF 20% 6.3V X6S 603

32 PP0V75_S3_MEM_VREFDQ_B

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

J3100 DDR3-SODIMM (2 OF 2) F-RT-BGA6

92 11 IN	MEM_B_CKE<0>	73	CKE0	CKE1	74	MEM_B_CKE<1>	IN 11 92
	NC	75	VDD	VDD	76		
		77	NC	A15	78	MEM_B_A<15>	IN 11 92
92 11 IN	MEM_B_BA<2>	79	BA2	A14	80	MEM_B_A<14>	IN 11 92
		81	VDD	VDD	82		
92 11 IN	MEM_B_A<12>	83	A12/BC*	A11	84	MEM_B_A<11>	IN 11 92
92 11 IN	MEM_B_A<9>	85	A9	A7	86	MEM_B_A<7>	IN 11 92
		87	VDD	VDD	88		
92 11 IN	MEM_B_A<8>	89	A8	A6	90	MEM_B_A<6>	IN 11 92
92 11 IN	MEM_B_A<5>	91	A5	A4	92	MEM_B_A<4>	IN 11 92
		93	VDD	VDD	94		
92 11 IN	MEM_B_A<3>	95	A3	A2	96	MEM_B_A<2>	IN 11 92
92 11 IN	MEM_B_A<1>	97	A1	A0	98	MEM_B_A<0>	IN 11 92
		99	VDD	VDD	100		
92 11 IN	MEM_B_CLK_P<0>	101	CK0	CK1	102	MEM_B_CLK_P<1>	IN 11 92
92 11 IN	MEM_B_CLK_N<0>	103	CK0*	CK1*	104	MEM_B_CLK_N<1>	IN 11 92
		105	VDD	VDD	106		
92 11 IN	MEM_B_A<10>	107	A10/AP	BA1	108	MEM_B_BA<1>	IN 11 92
92 11 IN	MEM_B_BA<0>	109	BA0	RAS*	110	MEM_B_RAS_L	IN 11 92
		111	VDD	VDD	112		
92 11 IN	MEM_B_WE_L	113	WE*	S0*	114	MEM_B_CS_L<0>	IN 11 92
92 11 IN	MEM_B_CAS_L	115	CAS*	ODT0	116	MEM_B_ODT<0>	IN 11 92
		117	VDD	VDD	118		
92 11 IN	MEM_B_A<13>	119	A13	ODT1	120	MEM_B_ODT<1>	IN 11 92
92 11 IN	MEM_B_CS_L<1>	121	S1*	NC	122		
		123	VDD	VDD	124		
	NC	125	TEST	VREFCA	126		
		127	VSS	VSS	128		
29 BI	=MEM_B_DQ<32>	129	DQ32	DQ36	130	=MEM_B_DQ<36>	BI 29
29 BI	=MEM_B_DQ<33>	131	DQ33	DQ37	132	=MEM_B_DQ<37>	BI 29
		133	VSS	VSS	134		
29 BI	=MEM_B_DQS_N<4>	135	DQS4*	DM4	136	=MEM_B_DM<4>	IN 29
29 BI	=MEM_B_DQS_P<4>	137	DQS4	VSS	138		
		139	VSS	DQ38	140	=MEM_B_DQ<38>	BI 29
92 29 11 BI	MEM_B_DQ<37>	141	DQ34	DQ39	142	=MEM_B_DQ<39>	BI 29
29 BI	=MEM_B_DQ<35>	143	DQ35	VSS	144		
		145	VSS	DQ44	146	=MEM_B_DQ<44>	BI 29
29 BI	=MEM_B_DQ<40>	147	DQ40	DQ45	148	=MEM_B_DQ<45>	BI 29
29 BI	=MEM_B_DQ<41>	149	DQ41	VSS	150		
		151	VSS	DQS5*	152	=MEM_B_DQS_N<5>	BI 29
29 IN	=MEM_B_DM<5>	153	DM5	DQS5	154	=MEM_B_DQS_P<5>	BI 29
		155	VSS	VSS	156		
29 BI	=MEM_B_DQ<42>	157	DQ42	DQ46	158	=MEM_B_DQ<46>	BI 29
29 BI	=MEM_B_DQ<43>	159	DQ43	DQ47	160	=MEM_B_DQ<47>	BI 29
		161	VSS	VSS	162		
29 BI	=MEM_B_DQ<48>	163	DQ48	DQ52	164	=MEM_B_DQ<52>	BI 29
29 BI	=MEM_B_DQ<49>	165	DQ49	DQ53	166	=MEM_B_DQ<53>	BI 29
		167	VSS	VSS	168		
29 BI	=MEM_B_DQS_N<6>	169	DQS6*	DM6	170	=MEM_B_DM<6>	IN 29
29 BI	=MEM_B_DQS_P<6>	171	DQS6	VSS	172		
		173	VSS	DQ54	174	=MEM_B_DQ<54>	BI 29
29 BI	=MEM_B_DQ<50>	175	DQ50	DQ55	176	=MEM_B_DQ<55>	BI 29
29 BI	=MEM_B_DQ<51>	177	DQ51	VSS	178		
		179	VSS	DQ60	180	=MEM_B_DQ<60>	BI 29
29 BI	=MEM_B_DQ<56>	181	DQ56	DQ61	182	=MEM_B_DQ<61>	BI 29
29 BI	=MEM_B_DQ<57>	183	DQ57	VSS	184		
		185	VSS	DQS7*	186	=MEM_B_DQS_N<7>	BI 29
29 IN	=MEM_B_DM<7>	187	DM7	DQS7	188	=MEM_B_DQS_P<7>	BI 29
		189	VSS	VSS	190		
29 BI	=MEM_B_DQ<58>	191	DQ58	DQ62	192	=MEM_B_DQ<62>	BI 29
29 BI	=MEM_B_DQ<59>	193	DQ59	DQ63	194	=MEM_B_DQ<63>	BI 29
		195	VSS	VSS	196		
	MEM_B_SA<0>	197	SA0	EVENT*	198	MEM_EVENT_A_L	OUT 28 45 46
40 72 73 24 28 27 26 69 68 63 62 60 64 23 99 88 87 85 84 83 80 79 78 77 76 75 74 31 30 18 17 7 4 PP3V3_S0		199	VDDSPD	SDA	200	SMBUS_PCH_DATA	BI 17 25 26 28 32 42 47 48 63 88 94
	MEM_B_SA<1>	201	SA1	SCL	202	SMBUS_PCH_CLK	IN 17 25 26 28 32 42 47 48 63 88 94
		203	VTT	VTT	204		PP0V75_S0_DDRVTT 6 7 28 31 67
		205	MTG PIN	MTG PIN	206		
		207	MTG PIN	MTG PIN	208		
		209	MTG PIN	MTG PIN	210		
		211	MTG PIN	MTG PIN	212		

KEY

516S0806

SPD ADDR=0xA4(WR)/0xA5(RD)

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402

J3100 DDR3-SODIMM (1 OF 2) F-RT-BGA6 CRITICAL

		1	VREFDQ	VSS	2		
		3	VSS	DQ4	4	=MEM_B_DQ<4>	BI 29
29 BI	=MEM_B_DQ<0>	5	DQ0	DQ5	6	=MEM_B_DQ<5>	BI 29
29 BI	=MEM_B_DQ<1>	7	DQ1	VSS	8		
		9	VSS	DQS0*	10	MEM_B_DQS_N<0>	BI 11 29 92
92 29 11 IN	MEM_B_DM<0>	11	DM0	DQS0	12	MEM_B_DQS_P<0>	BI 11 29 92
		13	VSS	VSS	14		
29 BI	=MEM_B_DQ<2>	15	DQ2	DQ6	16	=MEM_B_DQ<6>	BI 29
29 BI	=MEM_B_DQ<3>	17	DQ3	DQ7	18	=MEM_B_DQ<7>	BI 29
		19	VSS	VSS	20		
29 BI	=MEM_B_DQ<8>	21	DQ8	DQ12	22	=MEM_B_DQ<12>	BI 29
29 BI	=MEM_B_DQ<9>	23	DQ9	DQ13	24	=MEM_B_DQ<13>	BI 29
		25	VSS	VSS	26		
29 BI	=MEM_B_DQS_N<1>	27	DQS1*	DM1	28	=MEM_B_DM<1>	IN 29
29 BI	=MEM_B_DQS_P<1>	29	DQS1	RESET*	30	MEM_RESET_L	IN 28 31
		31	VSS	VSS	32		
29 BI	=MEM_B_DQ<10>	33	DQ10	DQ14	34	=MEM_B_DQ<14>	BI 29
29 BI	=MEM_B_DQ<11>	35	DQ11	DQ15	36	=MEM_B_DQ<15>	BI 29
		37	VSS	VSS	38		
29 BI	=MEM_B_DQ<16>	39	DQ16	DQ20	40	=MEM_B_DQ<20>	BI 29
29 BI	=MEM_B_DQ<17>	41	DQ17	DQ21	42	=MEM_B_DQ<21>	BI 29
		43	VSS	VSS	44		
29 BI	=MEM_B_DQS_N<2>	45	DQS2*	DM2	46	=MEM_B_DM<2>	IN 29
29 BI	=MEM_B_DQS_P<2>	47	DQS2	VSS	48		
		49	VSS	DQ22	50	=MEM_B_DQ<22>	BI 29
29 BI	=MEM_B_DQ<18>	51	DQ18	DQ23	52	=MEM_B_DQ<23>	BI 29
29 BI	=MEM_B_DQ<19>	53	DQ19	VSS	54		
		55	VSS	DQ28	56	=MEM_B_DQ<28>	BI 29
29 BI	=MEM_B_DQ<24>	57	DQ24	DQ29	58	=MEM_B_DQ<29>	BI 29
29 BI	=MEM_B_DQ<25>	59	DQ25	VSS	60		
		61	VSS	DQS3*	62	=MEM_B_DQS_N<3>	BI 29
29 IN	=MEM_B_DM<3>	63	DM3	DQS3	64	=MEM_B_DQS_P<3>	BI 29
		65	VSS	VSS	66		
29 BI	=MEM_B_DQ<26>	67	DQ26	DQ30	68	=MEM_B_DQ<30>	BI 29
29 BI	=MEM_B_DQ<27>	69	DQ27	DQ31	70	=MEM_B_DQ<31>	BI 29
		71	VSS	VSS	72		

KEY

516S0806

PP0V75_S3_MEM_VREFCA_B 32

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

"Expansion" (bottom) slot

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: DDR3 SO-DIMM Connector B

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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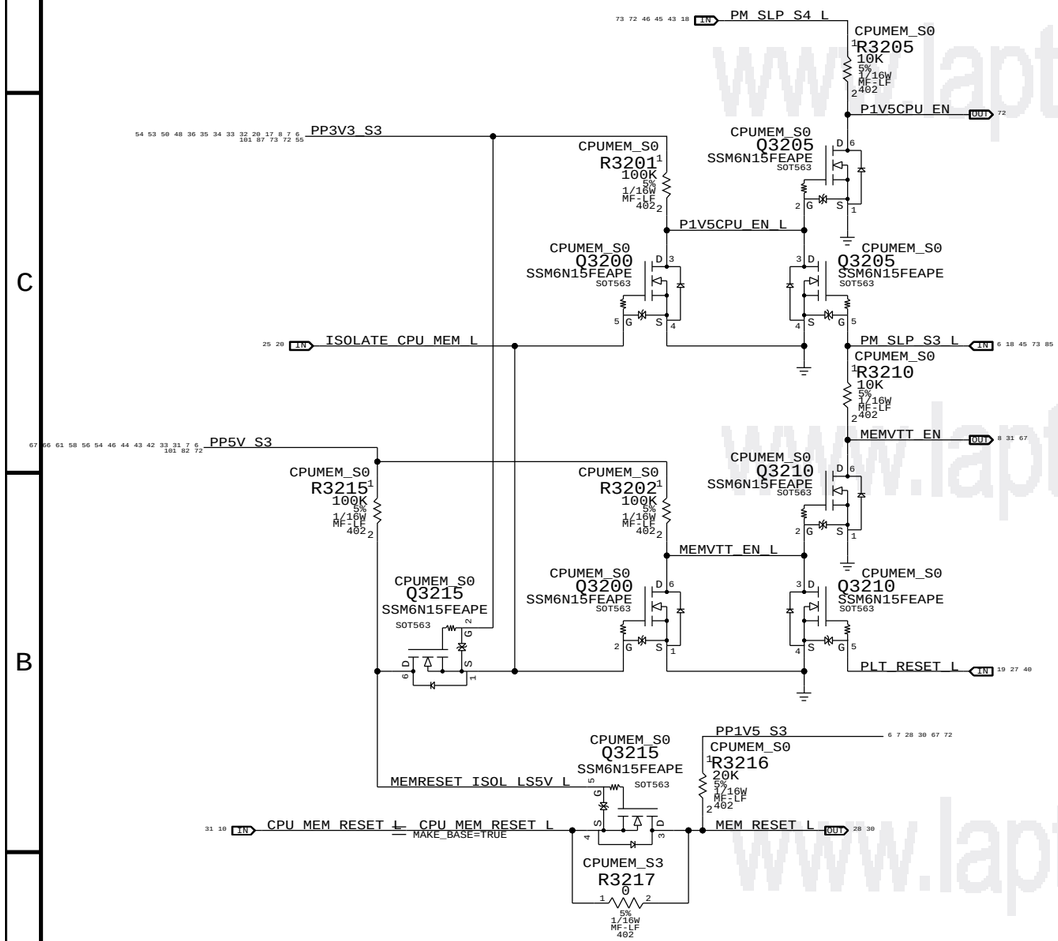
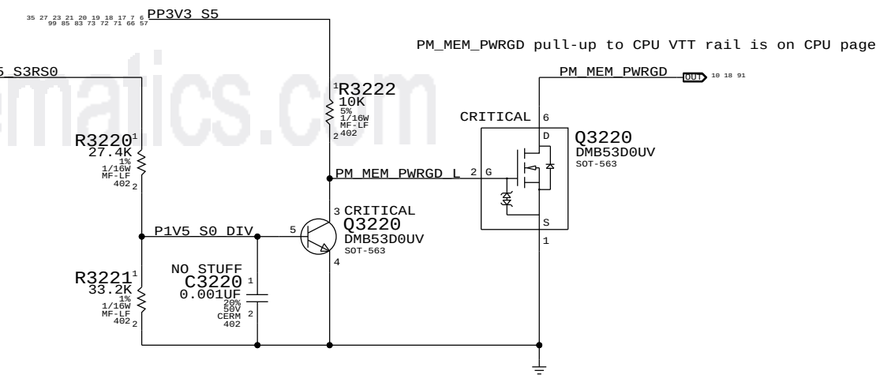
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

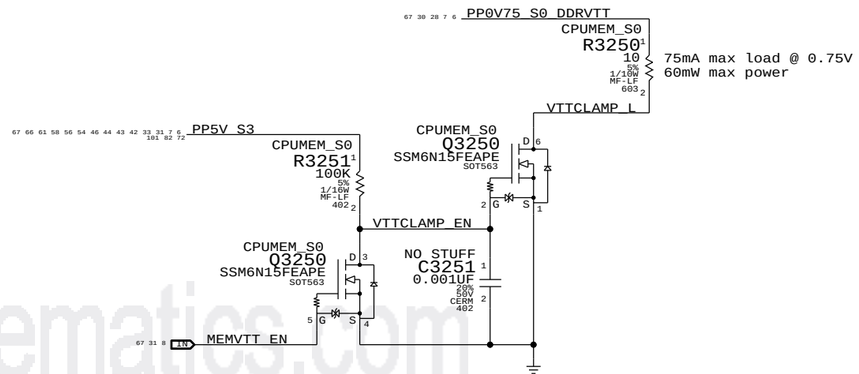


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
	4	0	0	1	1	X	1	0	1
S3	5	0	1	1	1	0 (*)	1	1	1
to	6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

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SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: CPU Memory S3 Support

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DRAWING NUMBER: <SCH_NUM> SIZE: D
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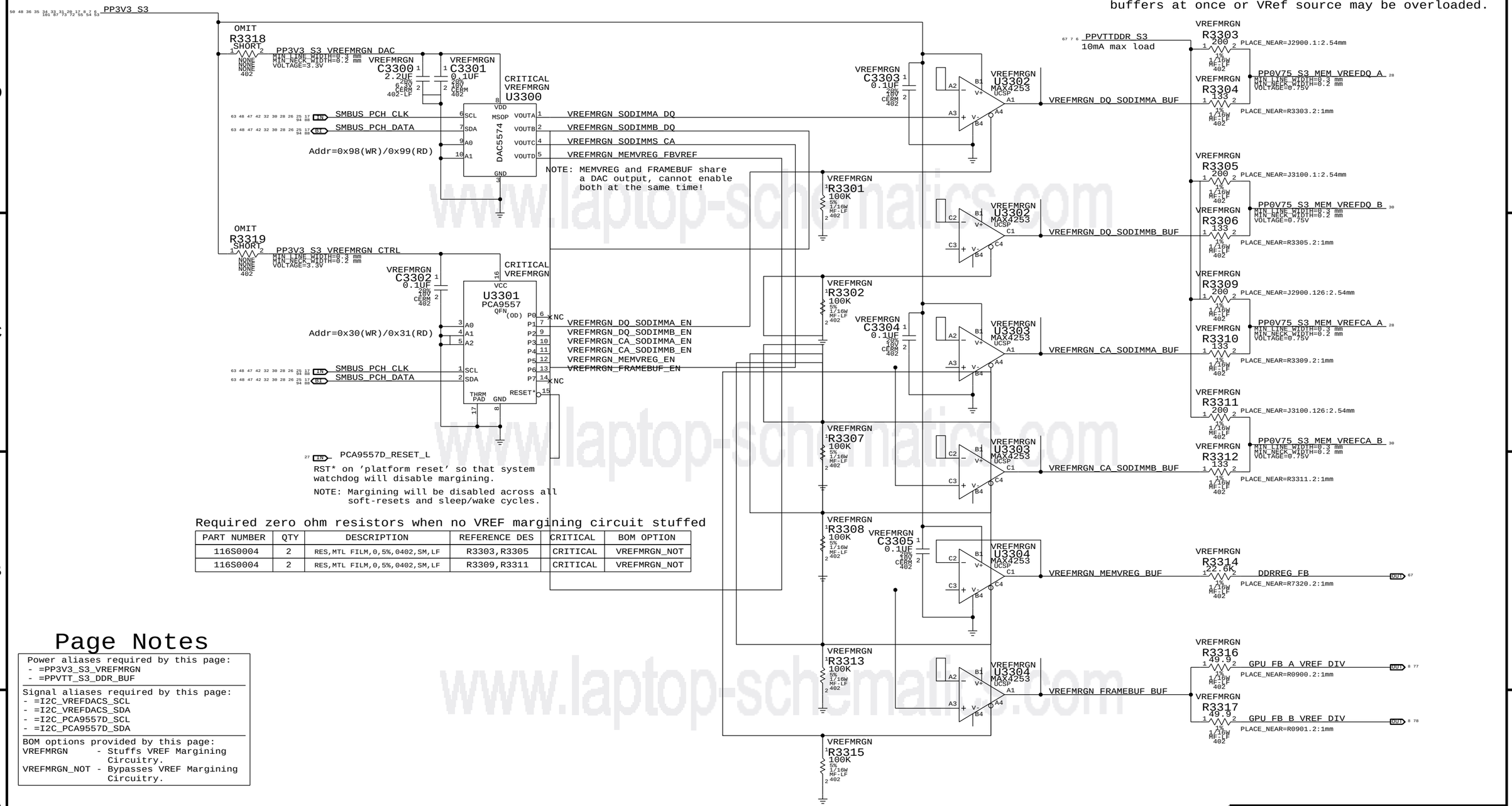

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3303,R3305	CRITICAL	VREFMRGN_NOT
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3309,R3311	CRITICAL	VREFMRGN_NOT

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.
VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: FSB/DDR3/FRAMEBUF Vref Margining

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AP_PWR_EN IN 20 73

AP_CLKREQ_L OUT 25 17

Q3401 SSM6N15FEAPE SOT563

AP_CLKREQ_Q_L 6

3V S3 WLAN FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	0.727 A (EDP)

CRITICAL Q3450 TPCP8102 23V1K-SM

727 MA PEAK
606 MA NOMINAL MAX

155S0367 L3404 FERR-120-OHM-3A 0603

PP3V3_WLAN 6 → PP3V3_WLAN_F → XW3452 SM → PP3V3_WLAN_R

MIN_LINE_WIDTH=1 mm MIN_NECK_WIDTH=0.4 mm
MIN_LINE_WIDTH=1 mm
MIN_LINE_WIDTH=1 mm MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=1 mm MIN_NECK_WIDTH=0.5 mm

C3422 0.1uF 20% 10V CERM 402
C3421 0.1uF 10% 10V CERM 402
C3420 10UF 20% 10V X5R 805
PLACEMENT_NOTE=Place close to J3401.
PLACEMENT_NOTE=Place close to Q3450.
PLACEMENT_NOTE=Place close to Q3450.

C3450 0.1UF 10% 16V X5R 402
C3451 0.033UF 10% 16V X5R 402
R3450 33K 5% 1/16W MF-LF 402
P3V3WLAN_SS
R3451 10K 5% 1/16W MF-LF 402
PP3V3_S3 93 94 99 72 73 87 97 6 7 8 17 20 31 32 33 34 35 36 48 50 53 54 101
PM_WLAN_EN_L IN 33 73

PCIE_AP_R2D_P 94 6 → C3431 0.1uF 10% 16V X5R 402 → PCIE_AP_R2D_C_P IN 17 94
PCIE_AP_R2D_N 94 6 → C3430 0.1uF 10% 16V X5R 402 → PCIE_AP_R2D_C_N IN 17 94
PLACEMENT_NOTE=Place close to J3401.

516S0582
CRITICAL
J3401
500913-0302
F-ST-SM

PCIE_AP_D2R_P OUT 6 17 94
PCIE_AP_D2R_N OUT 94 6 17

CRITICAL L3401 90-OHM-100MA DLP11S

AIRPORT

99 6 PCIE_CLK100M_AP_CONN_P → PCIE_CLK100M_AP_P IN 17 94
99 6 PCIE_CLK100M_AP_CONN_N → PCIE_CLK100M_AP_N IN 17 94
PLACEMENT_NOTE=Place close to J3401.

NC
NC

BLUETOOTH

L3403 90-OHM CRITICAL DLP0NS
PLACE_NEAR=J3401.21:2.54MM

99 6 CONN_USB2_BT_P → USB_BT_P BT 36 93
99 6 CONN_USB2_BT_N → USB_BT_N BT 36 93
PLACEMENT_NOTE=Place close to J3401.

PP3V3_S3_BT_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm

C3432 0.01UF 10% 16V CERM 402

L3406 FERR-120-OHM-1.5A 0402-LF
PLACEMENT_NOTE=PLACE L3406 NEAR J3401.

PP3V3_S3 6 7 8 17 20 31 32 33 34 35 36 48 50 53 54 55 72 73 87 101

PLACEMENT_NOTE=PLACE C3432 NEAR J3401

PCIE_WAKE_L OUT 6 18 27

RC (R3453 AND C3453)VALUE IS CHOSEN TO MEET THE 100 MS DELAY REQUIREMENT BETWEEN
3.3 WLAN POWER GETTING STABLE AND AIRPORT CARD COMING OUT OF RESET

PP3V3_WLAN_F 33 56
PP3V3_S3 6 7 8 17 20 31 32 33 34 35 36 48 50 53 54 55 72 73 87 101

R3453 110K 5% 1/16W MF-LF 402

U3402 74LVC1G17 SOT353-1
TC7SZ08AFEAPE SOT665 U3401

WLAN_SMIT_BUF
WLAN_SMIT_RC
R3455 1 5% 1/16W MF-LF 402
WLAN_SMIT_DISCHRG

C3453 1UF 10% 6.3V CERM 402
R3454 62K 5% 1/16W MF-LF 402 NOSTUFF

Q3401 SSM6N15FEAPE SOT563
PM_WLAN_EN_L 33 73

AP_RESET_L IN 27
6 AP_RESET_CONN_L

518S0767
CRITICAL
J3402
8190-3506-K281
F-RT-SM

6 PP5V_S3_ALSCAMERA_F
SMBUS_SMC_A_S3_SCL IN 6 45 48 54 97
SMBUS_SMC_A_S3_SDA BI 6 45 48 54 97
93 6 USB_CAMERA_CONN_P
93 6 USB_CAMERA_CONN_N

MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm

ALS CAMERA

CRITICAL L3407 90-OHM DLP0NS
PLACE_NEAR=J3402.6:2.54MM
USB_CAMERA_P BI 35
USB_CAMERA_N BI 35
PLACEMENT_NOTE=Place close to J3402

275 mA peak
206 mA nominal max

L3408 FERR-120-OHM-1.5A 0402-LF PLACEMENT_NOTE=Place close to J3402
PP5V_S3 6 7 31 42 43 44 46 54 56 58 61 66 67 72 82 101

C3452 0.1uF 20% 10V CERM 402

SYNC_MASTER=K18_COMMS SYNC_DATE=06/15/2009
PAGE TITLE
X16/ALS/CAMERA CONNECTOR

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Caesar IV Support

PP3V3_S3

GL137 R3511 0 5% 1/16W MF-LF 402

PP3V3_S3_CARDREADER_DVDD
MIN_LINE_WIDTH=0.40MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V

BYPASS=U3500.15:16:5 mm
BYPASS=U3500.26:27:5 mm
BYPASS=U3500.35:34:5 mm

GL137 C3500 10UF 20% 6.3V X5R 603
GL137 C3501 0.1UF 20% 10V CERM 402
GL137 C3502 0.1UF 20% 10V CERM 402
GL137 C3503 0.1UF 20% 10V CERM 402

GL137 L3500 0.22UH 0805-1

PP3V3_S3_CARDREADER_AVDD
MIN_LINE_WIDTH=0.40MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V

BYPASS=U3500.6:5:5 mm
BYPASS=U3500.11:12:5 mm

GL137 C3514 10UF 20% 6.3V X5R 603
GL137 C3504 0.1UF 20% 10V CERM 402
GL137 C3508 0.1UF 20% 10V CERM 402

PP1V8_S3_CARDREADER
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=1.8V

BYPASS=U3500.4:5:5 mm
GL137 C3506 0.1UF 20% 10V CERM 402

GL137 R3507 10K 5% 1/16W MF-LF 402
NO STUFF R3508 10K 5% 1/16W MF-LF 402
NO STUFF R3509 10K 5% 1/16W MF-LF 402
GL137 R3510 10K 5% 1/16W MF-LF 402

NO STUFF R3503 1M 5% 1/16W MF-LF 402
GL137 CRITICAL Y3500 12.000M-100PPM 8X4.5X1.4-SM
GL137 C3511 33PF 5% 50V CERM 402
GL137 C3512 33PF 5% 50V CERM 402

GL137 R3506 715 1% 1/16W MF-LF 402
GL137 R3502 0 5% 1/16W MF-LF 402
NO STUFF C3513 0.1UF 20% 10V CERM 402

U3500 GL137A LQFP CRITICAL GL137

USB_SDCARD_N	7	DM
USB_SDCARD_P	8	DP
GL137_GPIO1	48	GPIO1
GL137_GPIO2	47	GPIO2
NC	46	GPIO3
NC	19	SK
NC	20	CS
NC	21	DO
NC	22	DI (IPD)
GL137_CLK12M_X1	13	X1
GL137_CLK12M_X2	14	X2
GL137_RREF	10	RREF
GL137_TESTMOD	17	TESTMOD (IPD)
GL137_RESET_L	18	EXTRSTZ* (IPU)
VDD180	4	
AVDD	6, 11, 15	
DVDD	26, 35	
VDD5V	25	
PMOSO	36	
GND	5, 9, 12, 16, 27, 34	
D0	40	
D1	43	
D2	37	
D3	29	
D4	28	
D5	30	
D6	32	
D7	38	
CLK	39	SD_CLK_R
(IPD) SD_WP	3	
(IPD) SD_CMD	41	
(IPU) PDMOD	2	GL137_PDMOD
(IPU) SD_CDZ	23	
(IPU) XD_CDZ	1	NC
XD_CE	31	NC
(IPD) XD_WEZ	42	NC
(IPD) XD_RBZ	44	NC
(IPD) XD_WPZ	45	NC
(IPU) MS_INS	24	NC
(IPD) MS_BS	33	NC

GL137 Q3500 SSM6N15FEAPE SOT563
SDCARD_RESET
SDCARD_PLT_RST

GL137 Q3500 SSM6N15FEAPE SOT563
SDCARD_PLT_RST
SDCARD_PLT_RST_L

PP3V3_S0

GL137 R3512 10K 5% 1/16W MF-LF 402

Keep this net short!

GL137 C3507 2.2UF 20% 6.3V CERM1 603
GL137 C3505 0.1UF 20% 10V CERM 402
R3505 39K 5% 1/16W MF-LF 402

PP3V3_SW_SD_PWR
MIN_LINE_WIDTH=0.40 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

Max Current = 250 mA

BCM57765 R3550 0 5% 1/16W MF-LF 402
BCM57765 R3551 0 5% 1/16W MF-LF 402
BCM57765 R3552 0 5% 1/16W MF-LF 402
BCM57765 R3553 0 5% 1/16W MF-LF 402
BCM57765 R3554 0 5% 1/16W MF-LF 402
BCM57765 R3556 0 5% 1/16W MF-LF 402
BCM57765 R3555 0 5% 1/16W MF-LF 603

SDCONN_DATA<0>	R3550	SD_D<0>
SDCONN_DATA<1>	R3551	SD_D<1>
SDCONN_DATA<2>	R3552	SD_D<2>
SDCONN_DATA<3>	R3553	SD_D<3>
SDCONN_DATA<4..7>		SD_D<4..7> MAKE_BASE=TRUE
SDCONN_CLK	R3554	SD_CLK
SDCONN_CMD	R3556	SD_CMD
SD_WP		SD_WP MAKE_BASE=TRUE
SD_CD_L		SD_CD_L MAKE_BASE=TRUE

CRITICAL J3500 SD-CARD-K19-K24 F-RT-TH

3	VSS
6	VSS
5	CLK
2	CMD
7	DAT0
8	DAT1
9	DAT2
1	CD/DAT3
10	DAT4
11	DAT5
12	DAT6
13	DAT7
14	CARD_DETECT_SW
15	CARD_DETECT_GND
16	WRITE_PROTECT_SW
4	VDD
17	SHLD_PIN
18	SHLD_PIN
19	SHLD_PIN
20	SHLD_PIN

516-0225

GL137 R3504 0 5% 1/16W MF-LF 402
NO STUFF C3515 10PF 5% 50V CERM 402-1

NO STUFF R3513 10K 5% 1/16W MF-LF 402

PDMOD: POWER DOWN MODES
NC = DISABLE (DEFAULT)
10K LOW = POWER SAVING MODE ENABLE
10K HIGH = REMOTE WAKE UP ENABLE

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SYNC_MASTER=T27_REF SYNC_DATE=08/26/2009

PAGE TITLE: SecureDigital Card Reader

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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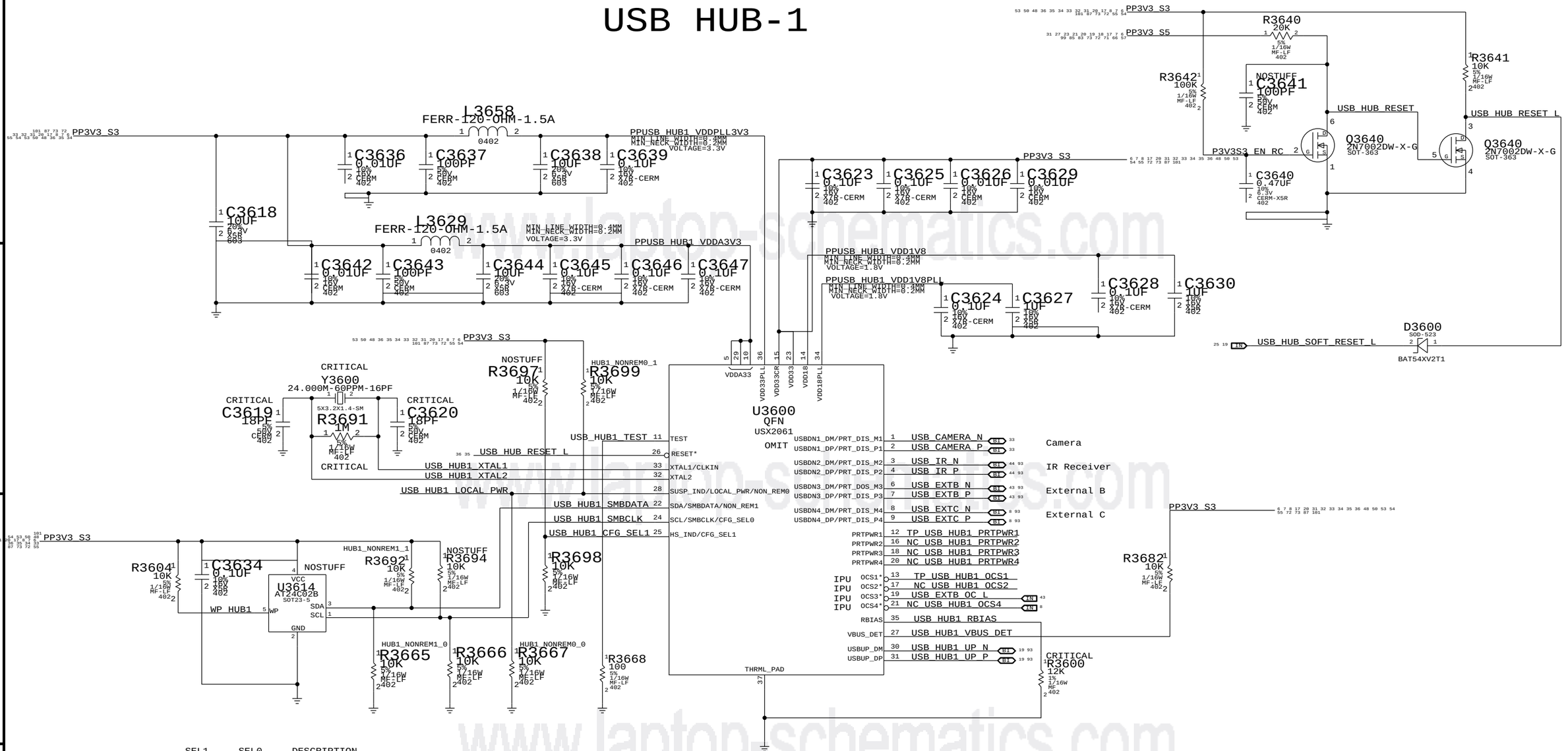
USB HUB-1



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	SEL1	SEL0	DESCRIPTION
K17/K18 configuration:	0	0	Internal Default with Self powered Operation
	0	1	SMBUS Slave Config
	1	0	Internal Default with Bus powered Operation
	1	1	EEPROM Supported

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	SMSC USB2514	U3600,U3700	CRITICAL	USBHUB_2514
338S0824	2	SMSC USB2514B	U3600,U3700	CRITICAL	USBHUB_2514B
338S0721	2	SMSC USX2061	U3600,U3700	CRITICAL	USBHUB_2061

BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0,HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0,HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1,HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1,HUB1_NONREM0_1

SYNC MASTER=K18_MLB SYNC DATE=10/07/2009

PAGE TITLE: USB HUB 1

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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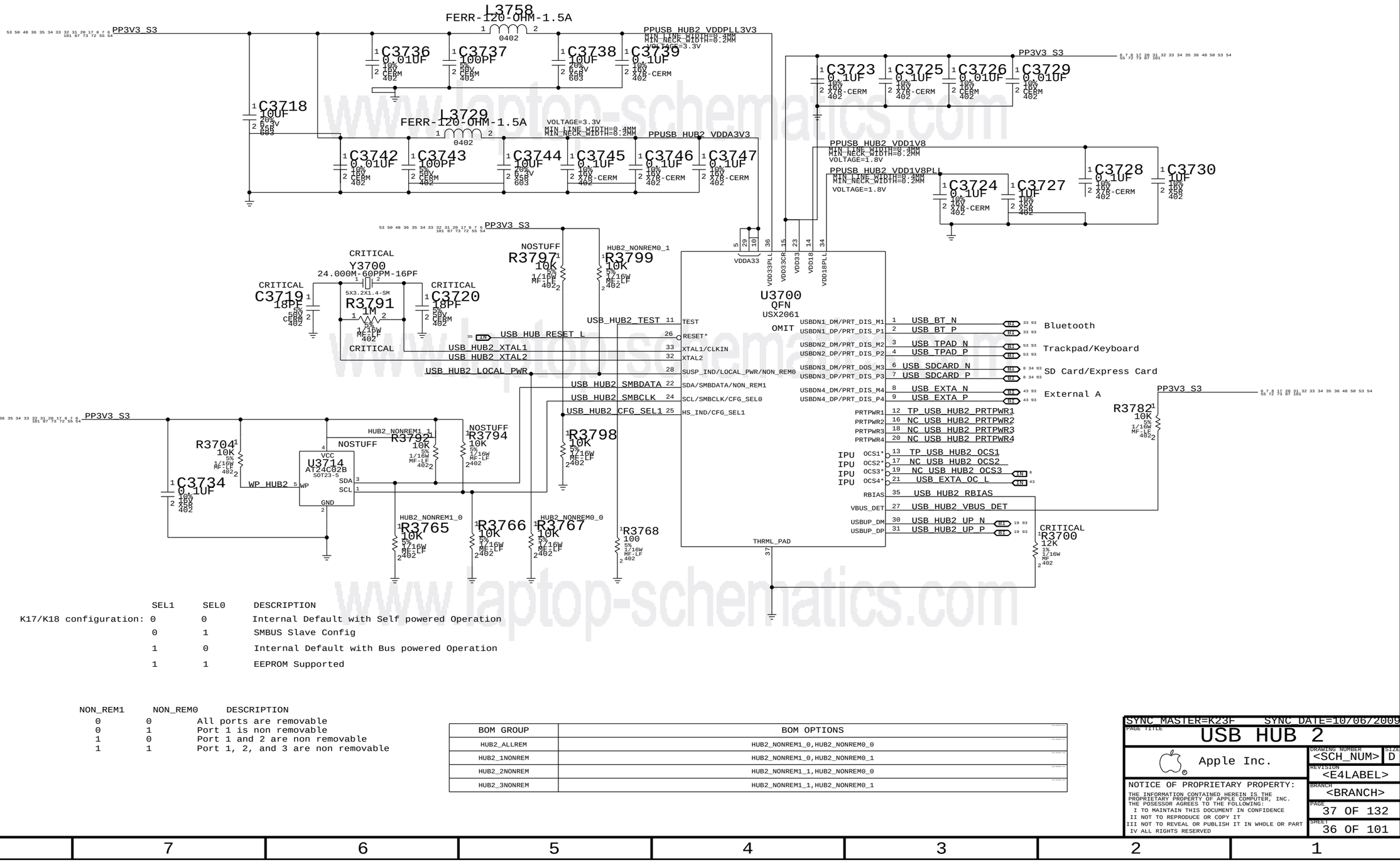
USB HUB-2



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	SEL1	SEL0	DESCRIPTION
K17/K18 configuration:	0	0	Internal Default with Self powered Operation
	0	1	SMBUS Slave Config
	1	0	Internal Default with Bus powered Operation
	1	1	EEPROM Supported

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM GROUP	BOM OPTIONS
HUB2_ALLREM	HUB2_NONREM1_0,HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0,HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1,HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1,HUB2_NONREM0_1

SYNC_MASTER=K23F SYNC_DATE=10/06/2009

PAGE TITLE: USB HUB 2

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BRANCH: <BRANCH>
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BCM57765 SR pins are internal 1.2V switching regulator.
If unused: Okay to float all 4 pins. (Broadcom not so sure now)
If used: VDD/VDDP connect to =PP3V3_ENET_PHY (add bypassing), LX connects to inductor, VFB to =PP1V2_ENET_PHY

PP3V3_ENET
86mA (1000base-T, Caesar II)

CRITICAL L3900 FERR-600-OHM-0.5A
CRITICAL L3905 FERR-600-OHM-0.5A
CRITICAL L3910 FERR-600-OHM-0.5A

PP3V3_ENET_PHY_XTALVDDH
PP3V3_ENET_PHY_BIASVDDH
PP3V3_ENET_PHY_AVDDH

BCM57765 R3915 0
BCM57765 R3900 0
C3900 0.1UF
C3905 0.1UF
C3910 0.1UF
C3911 0.1UF
R3910 4.7K
C3915 4.7UF
C3916 0.1UF
BCM57765 R3940 4.7K
BCM57765 R3941 4.7K

TP_BCM57765_SR_VDDP
BCM57765_SR_VDD
BCM57765_VDDO_PIN20
BCM57765_XTALVDDH
BCM57765_SR_LX
BCM57765_SR_VFB

CRITICAL L3920 FERR-600-OHM-0.5A
PP1V2_ENET
396mA (1000base-T, Caesar II)
PP1V2_ENET_PHY_AVDDL
CRITICAL L3925 FERR-600-OHM-0.5A
PP1V2_ENET_PHY_PCIEPLL
CRITICAL L3930 FERR-600-OHM-0.5A
PP1V2_ENET_PHY_GPHYPLL

C3921 0.1UF
C3920 4.7UF
C3926 0.1UF
C3925 4.7UF
C3931 0.1UF
C3930 4.7UF
C3936 0.1UF
C3935 10UF

AVDDH BIASVDDH VDDC VDDIO XTALVDDH VDDIO VDDC REGCTL12 VDDIO WAKE* AVDDL PCIE_PLLVDDL GPHY_PLLVDDL VDDC VDDC

PP3V3_S0
BCM57765 R3942 1K
C3950 0.1uF
C3951 0.1uF
C3955 0.1uF
C3956 0.1uF
BCM57765 R3943 0

PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_P
PCIE_ENET_R2D_C_N
ENET_WAKE_L (See note)

WAKE#

Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

BCM57765_VMAIN_PRSNT
PCIE_ENET_D2R_C_N
PCIE_ENET_D2R_C_P
PCIE_ENET_R2D_P
PCIE_ENET_R2D_N
PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
ENET_RESET_L
ENET_CLKREQ_L
BCM57765_WAKE_L
ENET_LOW_PWR
BCM57765_SMB_CLK
BCM57765_SMB_DATA
BCM5764_SCLK
BCM5764_MISO
BCM5764_MOSI
BCM5764_CS_L
TP_BCM5764_SPD100LED_L
TP_BCM5764_TRAFFICLED_L
BCM5764_CLK25M_XTALI
BCM5764_CLK25M_XTALO
BCM5764_RDAC

SMB_DATA (IPD)
PCIE_TXD_N
PCIE_TXD_P
PCIE_RXD_P
PCIE_RXD_N
PCIE_REFCLK_P
PCIE_REFCLK_N
PERST* (IPD)
CLKREQ* (OD)
LINKLED* (OD)
LOW_PWR (IPD)
VDDC
UART_MODE (IPD-BCM5764M)
SCLK
SI
SO
CS*
SPD100LED*
TRAFFICLED*
XTALI
XTALO
RDAC

CRITICAL OMIT U3900 BCM5764M QFN-8X8 VERSION 2

THRM_PAD

R3965 1.24K

ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>

CR_BUS_PWR is not for SD Card power, just decoupling for BCM57765 CR I/Os.
C3970 4.7UF
C3971 0.1UF
C3972 0.1UF

PP3V3R1V8_SW_SD_VIO
BCM57765_MEDIA_SENSE
BCM57765_SD_DETECT
BCM57765_CR_CMD
ENET_ENERGY_DET
SD_CD_L
SDCONN_CMD
SDCONN_CLK
SDCONN_DATA<0>
SDCONN_DATA<1>
SDCONN_DATA<2>
SDCONN_DATA<3>
SDCONN_DATA<4>
SDCONN_DATA<5>
SDCONN_DATA<6>
SDCONN_DATA<7>
SD_WP

R3972 0
R3973 0
R3974 0
PLACE_NEAR=L3999.1:1 mm

BCM57765_CR_DATA<4> R3975 0
BCM57765_CR_DATA<5> R3976 0
BCM57765_CR_DATA<6> R3977 0
BCM57765_CR_DATA<7> R3978 0

BCM57765_CE_L_MS_INS_L
BCM57765_CR_LED
TP_BCM57765_XD_DET

All resistors above BOMOPTIONed BCM57765
BCM57765 supports both active-levels for WP.

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Required for proper PHY operation. (Required ROM size TBD)

PP3V3_ENET
U3990 AT45DB011D SOIC-8S1 OMIT
C3990 0.1UF
BCM5764_SCLK
BCM5764_CS_L
BCM5764_MOSI
BCM5764_MISO
BCM57765 R3990 4.7K
BCM5764M R3997 4.7K

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures BCM57765 for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: BCM5764M requires SI pull-down instead of SO.

BCM5764M Support

All parts below BOMOPTIONed BCM5764M

BCM5764M pin-function

60-ENERGY_DET	BCM57765_CR_LED	R3980	0	ENET_ENERGY_DET
13-WAKE*	BCM57765_SR_VFB	R3981	0	ENET_WAKE_L (See note)
53-VMAIN_PRSNT	BCM57765_CR_DATA<5>	R3982	1K	PP3V3_S0
59-SMB_CLK	BCM57765_CE_L_MS_INS_L	R3983	4.7K	PP3V3_ENET
58-SMB_DATA	BCM57765_VMAIN_PRSNT	R3984	4.7K	
54-VAUX_PRSNT	BCM57765_CR_DATA<6>	R3985	1K	
16-VDDIO	BCM57765_SR_LX	R3986	0	
20-XTALVDDH	BCM57765_VDDO_PIN20	R3987	0	PP3V3_ENET_PHY_XTALVDDH
55-VDDC	BCM57765_CR_DATA<7>	R3988	0	PP1V2_ENET
17-VDDC	BCM57765_XTALVDDH	R3989	0	
14-VDDC	BCM57765_SR_VDD	R3998	0	
06-VDDC	BCM57765_SMB_CLK	R3999	0	
26-PCIE_VDDL	BCM57765_CR_CMD	L3999 FERR-600-OHM-0.5A		

Keep net short, with no stubs.

BCM5764M C3999 0.1UF
BCM5764M C3998 4.7UF
PLACE_NEAR=U3900.26:2 mm
PLACE_NEAR=U3900.26:1 mm
PLACE_NEAR=L3999.1:1 mm

SYNC_MASTER=T27_REF SYNC_DATE=08/20/2009
PAGE TITLE: Ethernet PHY (Caesar II/IV)
Apple Inc.
DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Place one of 0.1uf cap close to each centertap pin of transformer

ENETCONN_CTAP

C4000 0.1UF 10% 10V X5R 402
C4002 0.1UF 10% 10V X5R 402
C4004 0.1UF 10% 10V X5R 402
C4006 0.1UF 10% 10V X5R 402

ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_N<1>
ENET_MDI_P<1>
ENET_MDI_N<2>
ENET_MDI_P<2>
ENET_MDI_N<3>
ENET_MDI_P<3>

CRITICAL
T4000
SM
TX
RX
TLA-6T213HF

1 ENET_MDI_P<0>
2 ENET_MDI_N<0>
3 ENET_CTAP0
4 ENET_CTAP1
5 ENET_MDI_N<1>
6 ENET_MDI_P<1>
7 ENETCONN_P<1>
8 ENETCONN_N<1>
9 ENET_CTAP1
10 ENET_CTAP0
11 ENETCONN_N<0>
12 ENETCONN_P<0>

CRITICAL
T4001
SM
TX
RX
TLA-6T213HF

1 ENET_MDI_N<2>
2 ENET_MDI_P<2>
3 ENET_CTAP2
4 ENET_CTAP3
5 ENETCONN_N<3>
6 ENETCONN_P<3>
7 ENETCONN_P<3>
8 ENETCONN_N<3>
9 ENET_CTAP3
10 ENET_CTAP2
11 ENETCONN_P<2>
12 ENETCONN_N<2>

Transformers should be mirrored on opposite sides of the board

R4000 75 5% 1/10W MF 402
R4001 75 5% 1/10W MF 402
R4002 75 5% 1/10W MF 402
R4003 75 5% 1/10W MF 402

CRITICAL
J4000
RJ45-M97-3
F-RT-TH
514-0636

CRITICAL
C4008
1000PF 10% 2KV CERM 1206
ENET_BOB_SMITH_CAP
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

D4001
RCLAMP0524P
SLP2510P8
CRITICAL
PLACE_NEAR=T4001.1:5mm

D4000
RCLAMP0524P
SLP2510P8
CRITICAL
PLACE_NEAR=T4000.5:5mm

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SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: Ethernet Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0557	1	RES,0.475 ohm,1%,1/16W,0402	R4100	CRITICAL	

PP1V0_FW_FWPHY 135 mA
OMIT R4100 0.2 1% 1/10W MF-LF 402
PP1V0_FW_R MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.0V
L4110 120-OHM-0.3A-EMI 0402-LF
PP1V0_FW_FWPHY_AVDD MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.0V

25 mA PCIe SerDes
C4110 1UF 10% 6.3V CERM 402
C4111 1UF 10% 6.3V CERM 402

110 mA Digital Core
C4100 1UF 10% 6.3V CERM 402
C4101 1UF 10% 6.3V CERM 402
C4102 1UF 10% 6.3V CERM 402
C4103 1UF 10% 6.3V CERM 402
C4104 1UF 10% 6.3V CERM 402
C4105 1UF 10% 6.3V CERM 402
C4106 1UF 10% 6.3V CERM 402

7 mA I/O
C4120 1UF 10% 6.3V CERM 402
C4121 1UF 10% 6.3V CERM 402
C4122 1UF 10% 6.3V CERM 402
C4123 1UF 10% 6.3V CERM 402
C4124 1UF 10% 6.3V CERM 402
PP3V3_FW_FWPHY 6 7 39 40 41 138 mA

114 mA FireWire PHY
C4130 1UF 10% 6.3V CERM 402
C4131 1UF 10% 6.3V CERM 402
C4132 1UF 10% 6.3V CERM 402
L4130 120-OHM-0.3A-EMI 0402-LF
PP3V3_FW_FWPHY_VDDA MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=3.3V

17 mA PCIe SerDes
C4135 1UF 10% 6.3V CERM 402
C4136 1UF 10% 6.3V CERM 402
L4135 120-OHM-0.3A-EMI 0402-LF
PP3V3_FW_FWPHY_VP25 MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=3.3V

0 mA VReg PWR
C4141 0.1UF 20% 10V CERM 402
C4140 1UF 10% 6.3V CERM 402

VDD10 VDD33 VDDH VP VP25 VREG_PWR

OMIT CRITICAL U4100 FW643 BGA

PCI EXPRESS PHY
PCIE_RXD0N N8 — PCIE_FW_R2D_N
PCIE_RXD0P N7 — PCIE_FW_R2D_P
PCIE_TXD0N N5 — PCIE_FW_D2R_C_N
PCIE_TXD0P N6 — PCIE_FW_D2R_C_P
REFCLKN N9 — PCIE_CLK100M_FW_N
REFCLKP N10 — PCIE_CLK100M_FW_P

C4170 0.1UF 10% 16V X5R 402 PCIE_FW_R2D_C_N
C4171 0.1UF 10% 16V X5R 402 PCIE_FW_R2D_C_P
C4175 0.1UF 10% 16V X5R 402 PCIE_FW_D2R_N
C4176 0.1UF 10% 16V X5R 402 PCIE_FW_D2R_P
PLACEMENT_NOTE=Place C4170 close to U1800
PLACEMENT_NOTE=Place C4171 close to U1800
PLACEMENT_NOTE=Place C4175 close to U4100
PLACEMENT_NOTE=Place C4176 close to U4100

TEST CONTROLLER
NT-4 (IPU) TCK M4 — TP_FW643_TCK
NT-3 (IPU) TDI N2 — NC_FW643_TDI
(IPU) TDO M1 — TP_FW643_TDO
NT-1 (IPU) TMS M3 — TP_FW643_TMS
NT-2 (IPU) TRST* N1 — FW643_TRST_L

POWER MANAGEMENT (FIXME!!! - TYPO IN SYMBOL REGCTL)
NT-10 (IPD) WAKE* C2 — FW643_WAKE_L
REGCLT D13 — FW643_REGCTL
NT-12 (IPD) VAUX_DETECT E1 — FW643_VAUX_DETECT
NT-13 VAUX_DISABLE D2 — TP_FW643_VAUX_ENABLE
(OD) CLKREQN L2 — FW_CLKREQ_PHY_L

SCIF
NT-16 (IPD) SCIFCLK G2 — TP_FW643_SCIFCLK
NT-14 (IPD) SCIFDAIN G1 — TP_FW643_SCIFDAIN
NT-17 SCIFDOUT H1 — TP_FW643_SCIFDOUT
NT-15 (IPD) SCIFMC F2 — TP_FW643_SCIFMC

SERIAL EEPROM CONTROLLER
NT-7 SCL N12 — FW643_SCL
NT-6 SDA M11 — TP_FW643_SDA

CHIP RESET
NT-5 PERST* N4 — FW_RESET_L

1394 PHY
ATBUSB B13 (NC)
ATBUSH A13 (NC)
ATBUSN A11 (NC)
DS0 (IPD) NT-19 ← FWPHY_DS0
DS1 (IPD) NT-20 ← FWPHY_DS1
DS2 (IPD) NT-21 ← FWPHY_DS2
TPA0N B8 ← NC_FW0_TPAN
TPA0P A8 ← NC_FW0_TPAP
TPA1N B5 ← FW_PORT1_TPA_N
TPA1P A5 ← FW_PORT1_TPA_P
TPA2N B3 ← NC_FW2_TPAN
TPA2P A3 ← NC_FW2_TPAP
TPB0N B9 ← NC_FW0_TPBN
TPB0P A9 ← NC_FW0_TPBP
TPB1N B6 ← FW_PORT1_TPB_N
TPB1P A6 ← FW_PORT1_TPB_P
TPB2N B4 ← NC_FW2_TPBN
TPB2P A4 ← NC_FW2_TPBP
TPBIAS0 B7 ← NC_FW0_TPBIAS
TPBIAS1 C3 ← FW_P1_TPBIAS
TPBIAS2 A2 ← NC_FW2_TPBIAS
R0 B11 ← FW643_R0
TPCPS B10 ← FW643_TPCPS
NAND_TREE NT-OUT K1 ← TP_FW643_NAND_TREE
REXT L8 ← FW643_REXT
XO F13 ← FW_CLK24P576M_XO_R
XI NT-9 G13 ← FW_CLK24P576M_XI
SE (IPD) M13 ← TP_FW643_SE
SM (IPD) N13 ← TP_FW643_SM
MODE_A (IPD) NT-18 J2 ← TP_FW643_MODE_A
CE (IPD) L13 ← TP_FW643_CE
FW620* (IPU) D12 ← TP_FW643_FW620_L
JASI_EN (IPD) NT-11 D1 ← TP_FW643_JASI_EN
AVREG A10 → NC_FW643_AVREG
VBUF H13 ← TP_FW643_VBUF
FW_RESET* (IPU) NT-8 K13 ← FW643_PU_RST_L
OCR_CTL_V10 J12 ← TP_FW643_OCR10_CTL
OCR_CTL_V12 (Reserved) J13 (NC)

NOTE: NT-xx notes show NAND tree order.

MISCELLANEOUS
PPVP_FW_CPS → R4160 200K 1% 1/16W MF-LF 402 (PLACE_NEAR=U4100.B10:2mm)
C4150 22PF 5% 50V CERM 402
C4151 22PF 5% 50V CERM 402
FW_CLK24P576M_XO CRITICAL Y4150 24.576MHZ SM-3.2X2.5MMZ
R4150 412 1% 1/16W MF-LF 402
R4161 2.94K 1% 1/16W MF-LF 402
R4170 191 1% 1/16W MF-LF 402
R4162 470K 5% 1/16W MF-LF 402
C4162 0.33UF 10% 6.3V CERM-X5R 402

VSS VREG_VSS

PP3V3_FW_FWPHY
FW643_LDO
R4165 10K 5% 1/16W MF-LF 402
R4166 10K 5% 1/16W MF-LF 402
R4164 10K 5% 1/16W MF-LF 402
R4163 10K 5% 1/16W MF-LF 402

SYNC_MASTER=K19_MLB SYNC_DATE=05/29/2009

PAGE TITLE: FireWire LLC/PHY (FW643)

Apple Inc.

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Page Notes

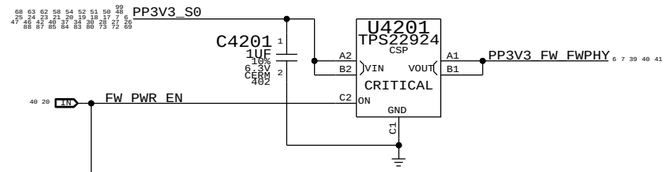
Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

Signal aliases required by this page:
(NONE)

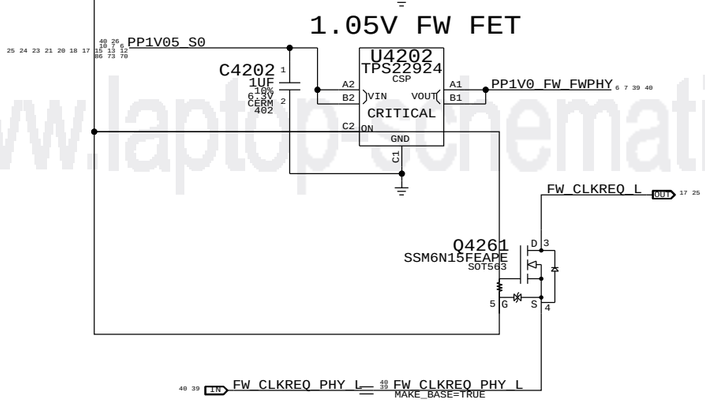
BOM options provided by this page:

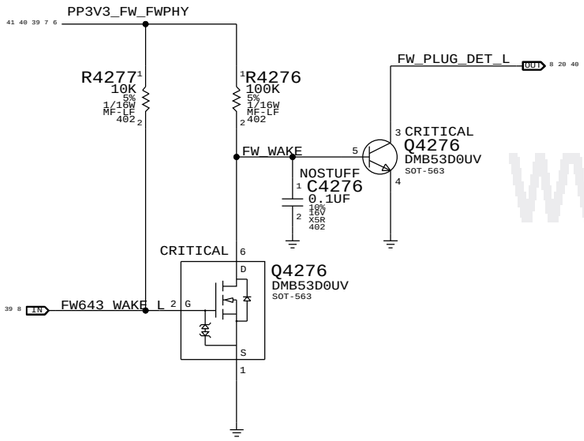
3.3V FW FET

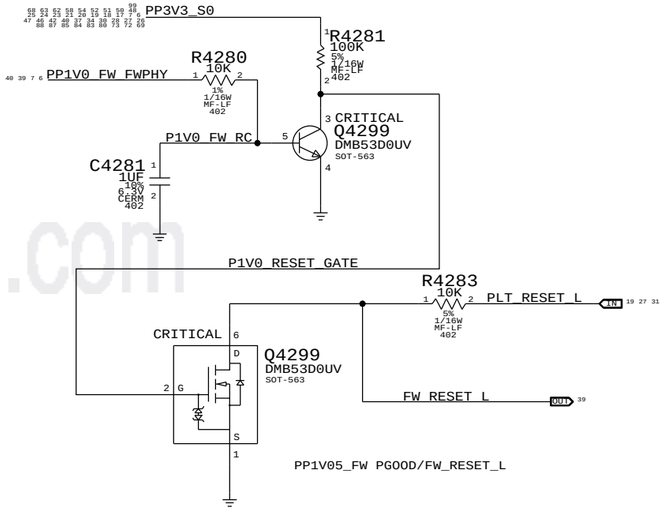
I(max) = 1.7A (85C)



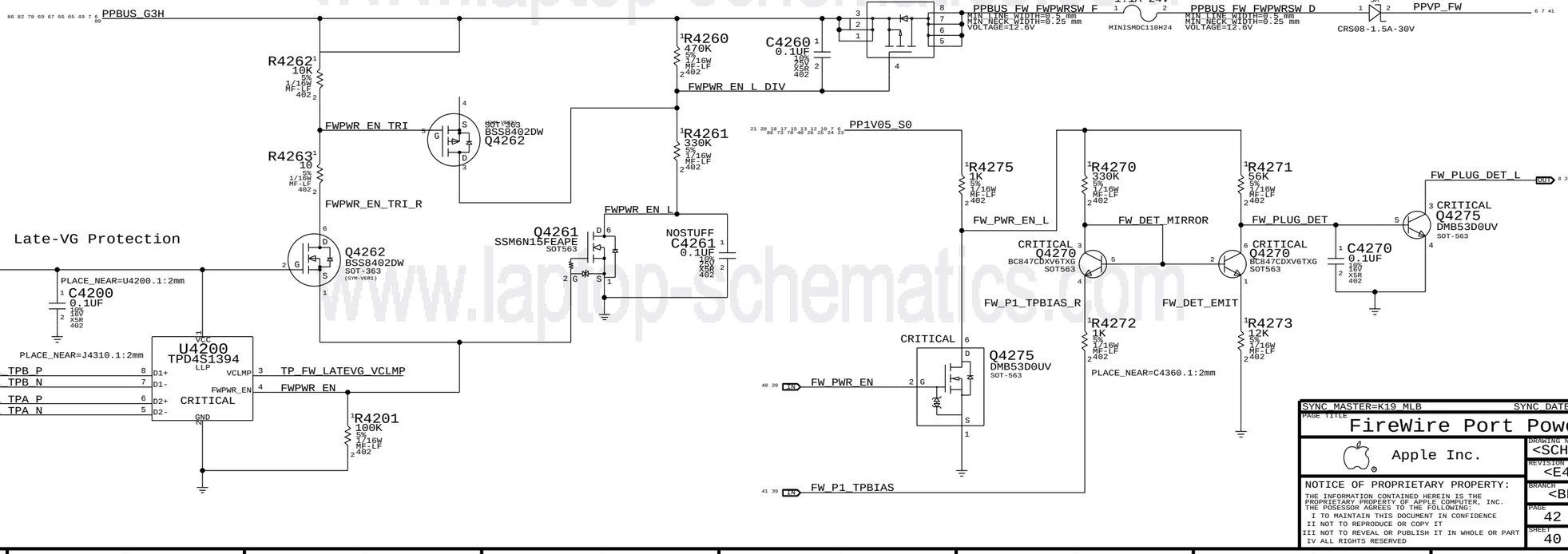
1.05V FW FET







FireWire Port Power Switch



SYNC_MASTER=K19_MLB SYNC_DATE=05/29/2009

PAGE TITLE: FireWire Port Power

Apple Inc.

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Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG

- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:

- 1-port Portable Power Class (0)

- Port "1" Bilingual (1394B)

41 40 39 7 6 PP3V3_FW_FWPHY

R4382 10K 1% 1/10W MF-LF 402

R4380 10K 1% 1/10W MF-LF 402

41 39 FWPHY_DS0 MAKE_BASE=TRUE — FWPHY_DS0 39 41

41 39 FWPHY_DS2 MAKE_BASE=TRUE — FWPHY_DS2 39 41

R4381 10K 1% 1/10W MF-LF 402

41 39 FWPHY_DS1 MAKE_BASE=TRUE — FWPHY_DS1 39 41

41 39 NC_FW0_TPBIAS — NC_FW0_TPBIAS MAKE_BASE=TRUE 39 41

41 39 6 NC_FW2_TPBIAS — NC_FW2_TPBIAS MAKE_BASE=TRUE 6 39 41

96 41 39 NC_FW0_TPAN — NC_FW0_TPAN MAKE_BASE=TRUE 39 41 96

96 41 39 6 NC_FW0_TPAP — NC_FW0_TPAP MAKE_BASE=TRUE 6 39 41 96

41 39 6 NC_FW2_TPAN — NC_FW2_TPAN MAKE_BASE=TRUE 6 39 41

41 39 6 NC_FW2_TPAP — NC_FW2_TPAP MAKE_BASE=TRUE 6 39 41

96 41 39 6 NC_FW0_TPBN — NC_FW0_TPBN MAKE_BASE=TRUE 6 39 41 96

96 41 39 6 NC_FW0_TPBP — NC_FW0_TPBP MAKE_BASE=TRUE 6 39 41 96

41 39 6 NC_FW2_TPBN — NC_FW2_TPBN MAKE_BASE=TRUE 6 39 41

41 39 6 NC_FW2_TPBP — NC_FW2_TPBP MAKE_BASE=TRUE 6 39 41

Termination

Place close to FireWire PHY

40 39 FW_P1_TPBIAS

TI PHYs require 1uF even though FW spec calls out 0.33uF

C4360 0.33UF 10% 6.3V CERM-X5R 402

SIGNAL_MODEL=EMPTY SIGNAL_MODEL=EMPTY

R4360 56.2 1% 1/16W MF-LF 402 — R4361 56.2 1% 1/16W MF-LF 402

PLACE_NEAR=U4100.A5:2mm — PLACE_NEAR=U4100.B5:2mm

96 41 40 39 FW_PORT1_TPA_P — FW_PORT1_TPA_P MAKE_BASE=TRUE 39 40 41 96

96 41 40 39 FW_PORT1_TPA_N — FW_PORT1_TPA_N MAKE_BASE=TRUE 39 40 41 96

96 41 40 39 FW_PORT1_TPB_P — FW_PORT1_TPB_P MAKE_BASE=TRUE 39 40 41 96

96 41 40 39 FW_PORT1_TPB_N — FW_PORT1_TPB_N MAKE_BASE=TRUE 39 40 41 96

SIGNAL_MODEL=EMPTY SIGNAL_MODEL=EMPTY

R4362 56.2 1% 1/16W MF-LF 402 — R4363 56.2 1% 1/16W MF-LF 402

PLACE_NEAR=U4100.B6:4mm — PLACE_NEAR=U4100.A6:4mm

FW_PORT1_TPB_C

C4364 220pF 5% 25V CERM 402

R4364 4.99K 1% 1/16W MF-LF 402

41 40 7 6 PPVP_FW

R4311 470K 5% 1/16W MF-LF 402

Q4300 BSS8402DW SOT-363 (SYM-VER1)

41 39 PPVP_FW_CPS MAKE_BASE=TRUE — PPVP_FW_CPS 39 41

MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=12.6V

CPS_EN_L_DIV

R4312 330K 5% 1/16W MF-LF 402

CPS_EN_L

PP3V3_FW_FWPHY

Q4300 BSS8402DW SOT-363 (SYM-VER1)

Cable Power

41 40 7 6 PPVP_FW

CRITICAL L4310 FERR-250-OHM SM

Note: Trace PPVP_FW_PORT1 must handle up to 5A

PPVP_FW_PORT1_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=33V

C4314 0.01UF 10% 50V X7R 402

96 41 40 39 FW_PORT1_TPB_N

96 41 40 39 FW_PORT1_TPB_P

96 41 40 39 FW_PORT1_TPA_N

96 41 40 39 FW_PORT1_TPA_P

(FW_PORT1_BREF)

(GND_FW_PORT1_VG)

FW_PORT1_AREF

C4319 0.1uF 10% 50V X7R 603-1

R4319 1M 5% 1/16W MF-LF 402

PLACEMENT_NOTE=Place C4319 close to connector pin 5.

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

PORT 1
BILINGUAL

CRITICAL J4310 1394B-M97 F-RT-TH

1	TPB-	TPB(R) TPB-	OUTPUT
9	TPB<R>	TPB<R>	
2	TPB+	TPB+ VP	
8		VP	
NC 7		VBC/NC	
6		VG	
3	TPA-	TPA- VG	INPUT
5	TPA<R>	TPA<R>	
4	TPA+	TPA(R) TPA+	
10			
11			
12		CHASSIS GND	
13			

514S0605

SYNC_MASTER=K19_MLB SYNC_DATE=05/29/2009

PAGE TITLE: FireWire Ports

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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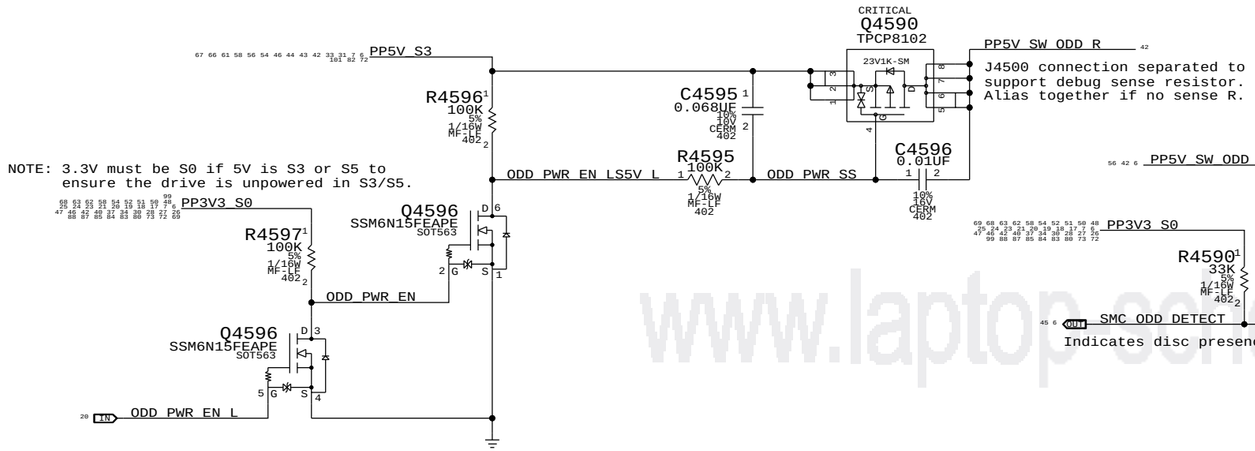
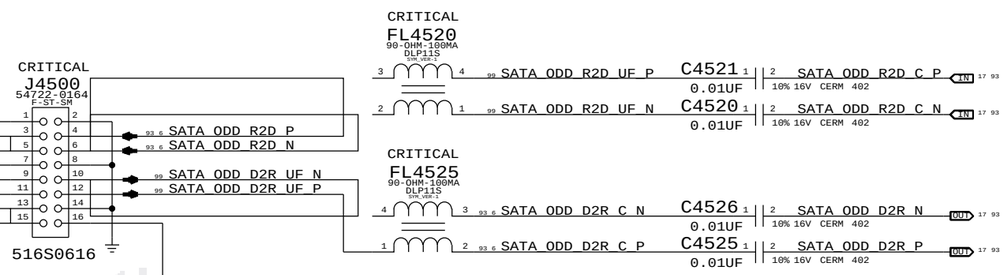
ODD Power Control

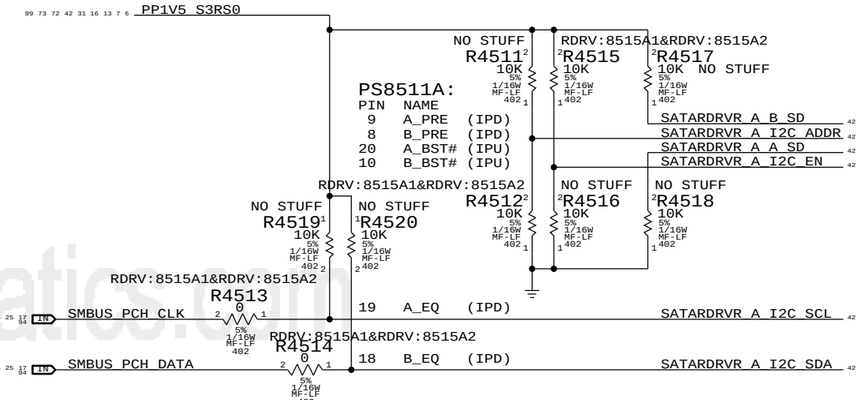


SATA ODD Connector

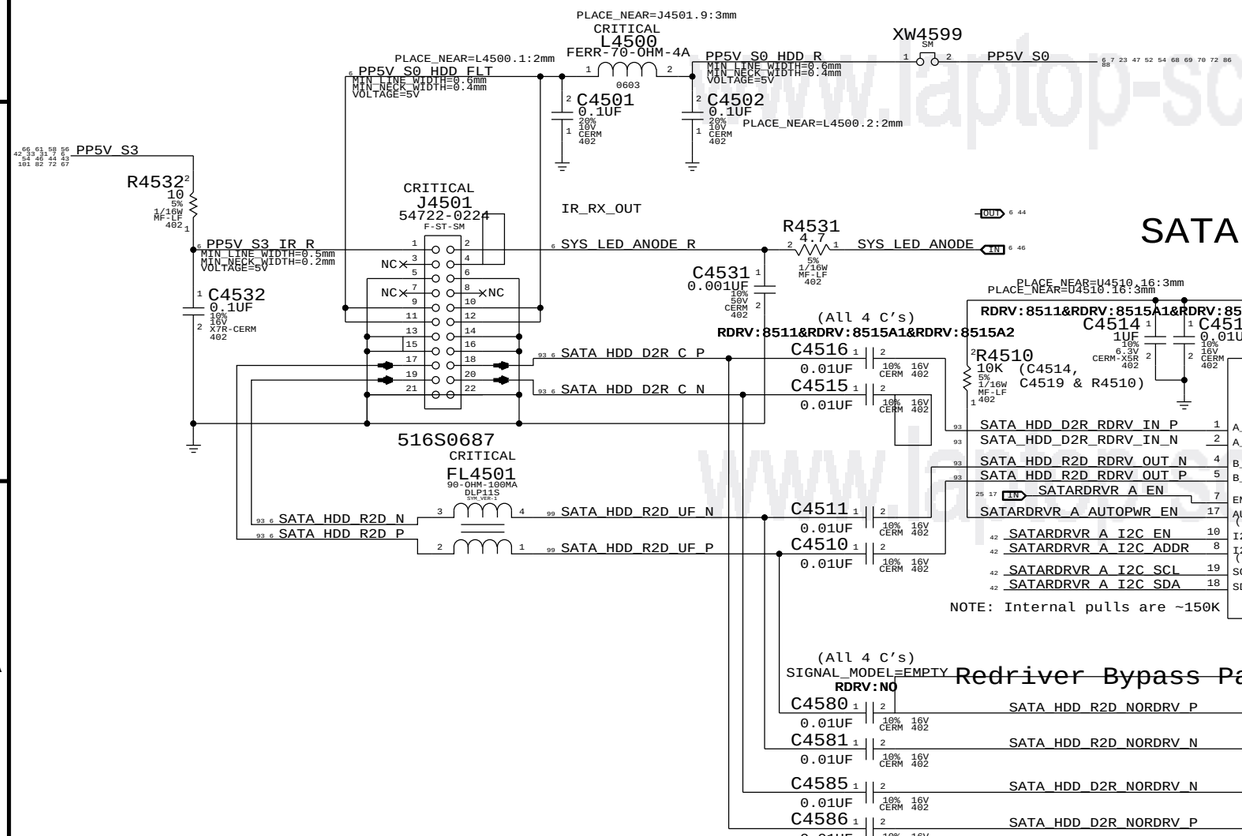


XW4598 SM — PP5V_SW_ODD_R ↔ PP5V_SW_ODD (MIN_LINE_WIDTH=0.6mm, MIN_NECK_WIDTH=0.4mm, VOLTAGE=5V)

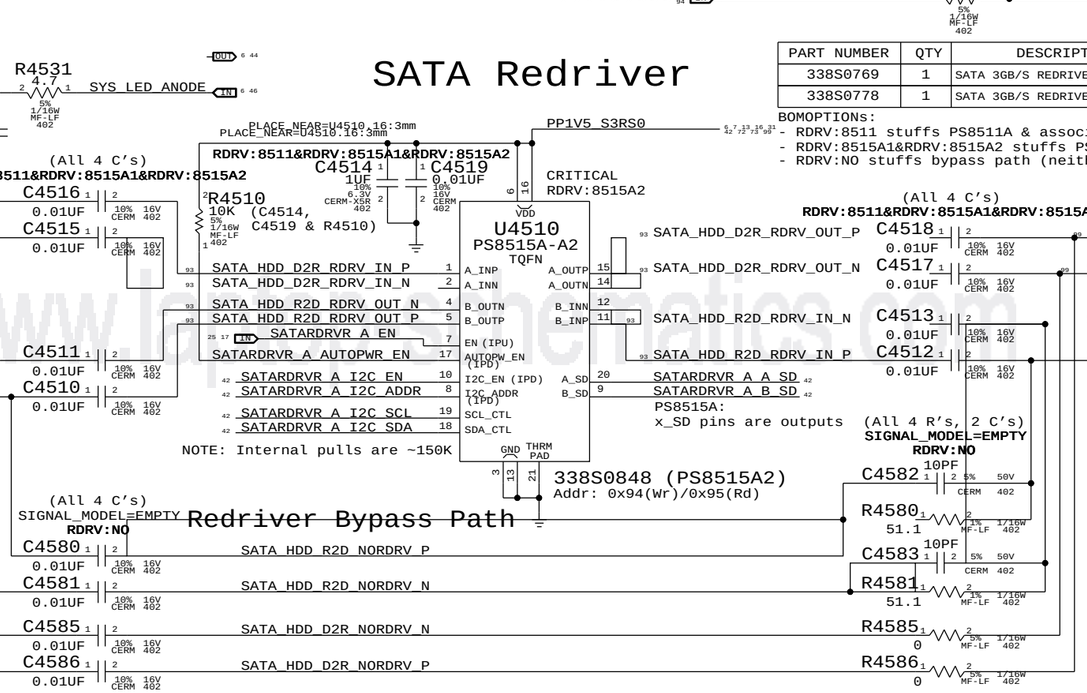
PS8511A / PS8515A Straps



SATA HDD/IR/SIL Connector



SATA Redriver



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0769	1	SATA 3GB/S REDRIVER, LOW POWER	U4510	CRITICAL	RDRV:8511
338S0778	1	SATA 3GB/S REDRIVER, LOW POWER	U4510	CRITICAL	RDRV:8515A1

BOMOPTIONs:
- RDRV:8511 stuffs PS8511A & associated parts (STRAPS TBD!!!)
- RDRV:8515A1&RDRV:8515A2 stuffs PS8515A & associated parts
- RDRV:NO stuffs bypass path (neither IC or associated parts stuffed)

SYNC_MASTER=T27_REF SYNC_DATE=10/01/2009

PAGE TITLE: SATA Connectors

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Port Power Switch

PP5V_S3
PM_SLP_S4_L
R4690 5.1K 5% 1/16W MF-LF 402
C4692 0.47UF 10% 10V X5R 402
USB_PWR_EN
USB_EXTA_OC_L
USB_EXTB_OC_L
CRITICAL
Q4690 TPS2064DGN MSOP
IN OUT1 OUT2 OC1* OC2* EN1 EN2 GND TPAD
PP5V_S3_RTUSB_A_ILIM
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.375 mm
VOLTAGE=5V
PP5V_S3_RTUSB_B_ILIM
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.375 mm
VOLTAGE=5V
C4690 10UF 20% 6.3V X5R 603
C4691 0.1UF 20% 10V CERM 402
C4695 10UF 20% 6.3V X5R 603
C4696 100UF 20% 6.3V POLY-TANT CASE-B2-SM
C4617 10UF 20% 6.3V X5R 603
C4616 100UF 20% 6.3V POLY-TANT CASE-B2-SM

Left USB Port A

CRITICAL
L4605 FERR-220-OHM-2.5A 0603
PP5V_S3_RTUSB_A_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.375 mm
VOLTAGE=5V
C4605 0.01uF 10% 16V CERM 402
CRITICAL
L4600 90-OHM-100MA DLP11S
USB2_EXTA_MUXED_N
USB2_EXTA_MUXED_P
USB2_LT1_N
USB2_LT1_P
CRITICAL
J4600 USB F-RT-TH-M97-4
D4600 RCLAMP0502N SLP1210N6
CRITICAL

CRITICAL
L4615 FERR-220-OHM-2.5A 0603
PP5V_S3_RTUSB_B_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.375 mm
VOLTAGE=5V
C4615 0.01uF 10% 16V CERM 402

We can add protection to 5V if we want, but leaving NC for now

Place L4600 and L4605 at connector pin

CRITICAL
J4610 USB F-RT-TH-M97-4
CRITICAL
L4610 90-OHM-100MA DLP11S
USB_EXTB_N
USB_EXTB_P
USB_LT2_N
USB_LT2_P
D4610 RCLAMP0502N SLP1210N6
CRITICAL

USB/SMC Debug Mux

SMC_DEBUG_YES
PP3V42_G3H
C4650 0.1UF 20% 10V CERM 402
R4650 10K 5% 1/16W MF-LF 402
SMC_RX_L
SMC_TX_L
USB_EXTA_P
USB_EXTA_N
U4650 PI3USB102ZLE TQFN CRITICAL
VCC GND M+ M- D+ D- OE* Y+ Y- SEL
USB_DEBUGPRT_EN_L
SEL=0 Choose SMC
SEL=1 Choose USB
SMC_DEBUG_NO
R4651 0 5% 1/16W MF-LF 402
SMC_DEBUG_NO
R4652 0 5% 1/16W MF-LF 402

Left USB Port B

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: External USB Connectors

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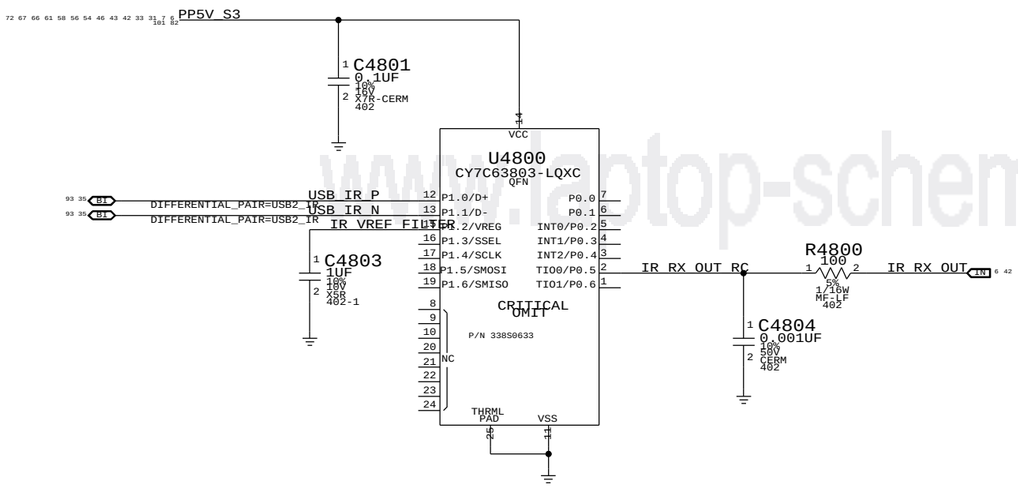
IR SUPPORT



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SYNC_MASTER=K19_MLB SYNC_DATE=05/29/2009

PAGE TITLE: Front Flex Support

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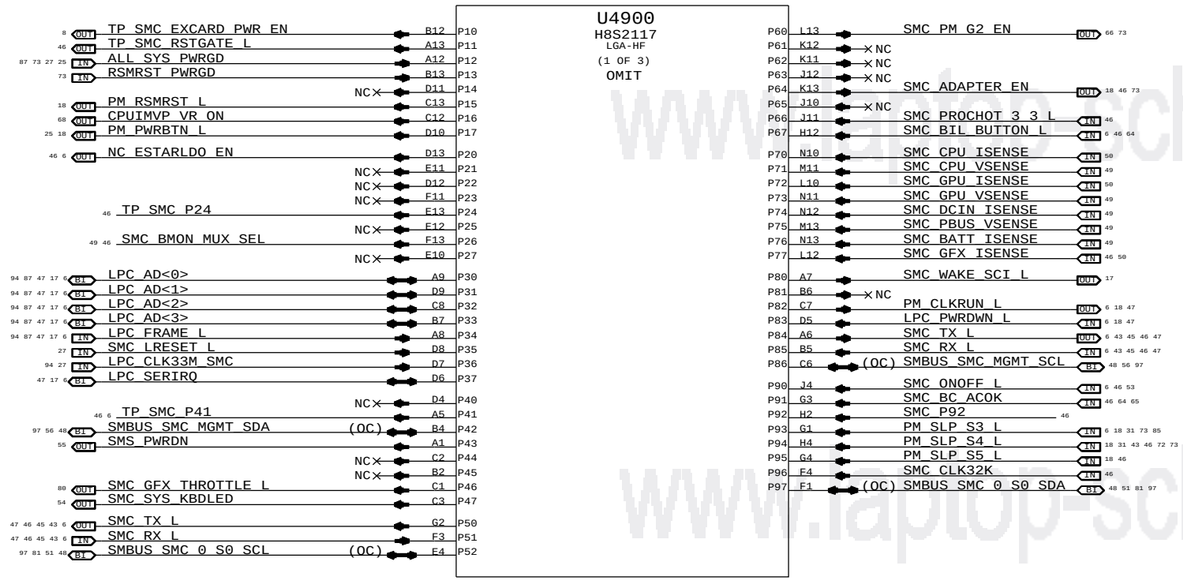
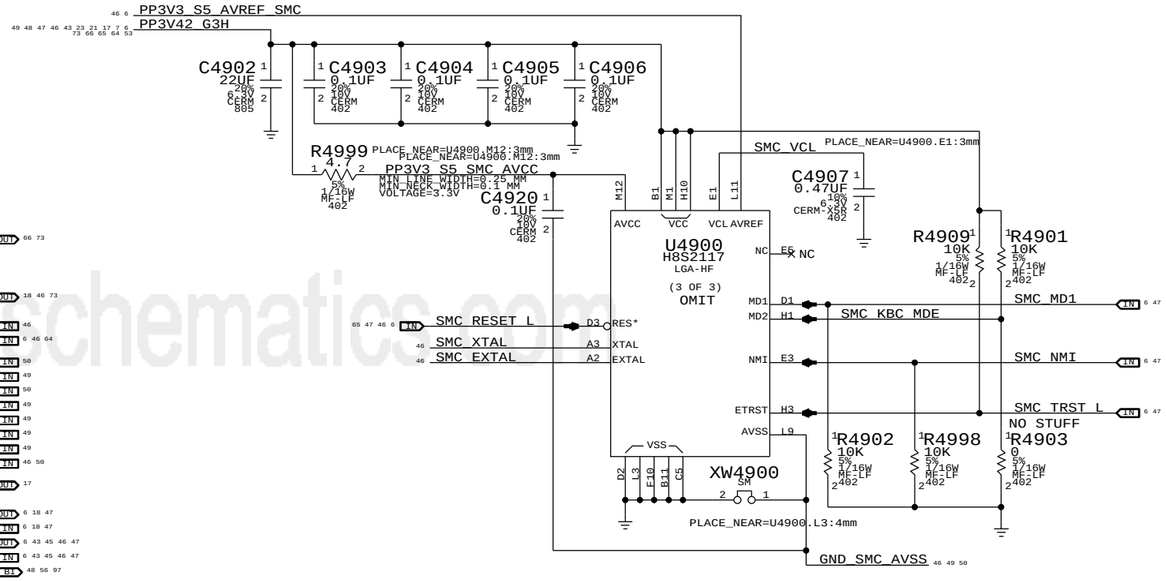
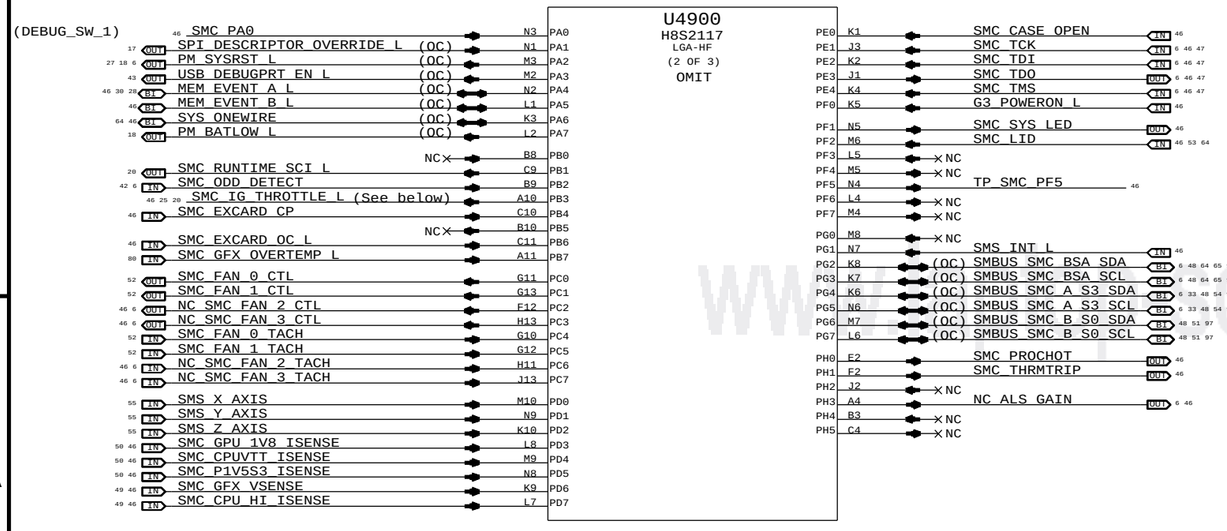
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





NOTE: P94 and P95 are shorted, P95 could be spare.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)

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SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 49 OF 132

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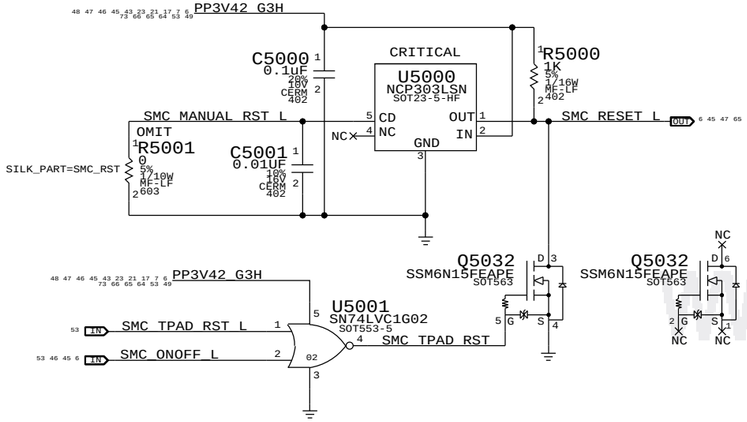
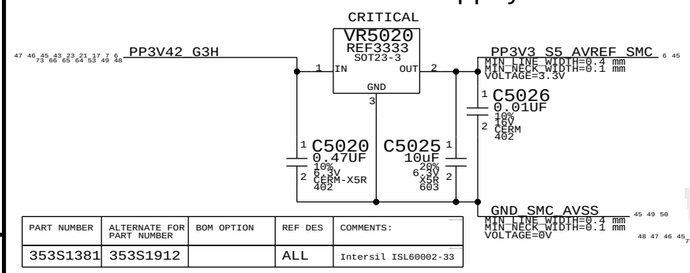
SMC Reset "Button" / Brownout Detect

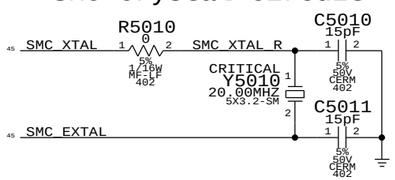


SMC AVREF Supply



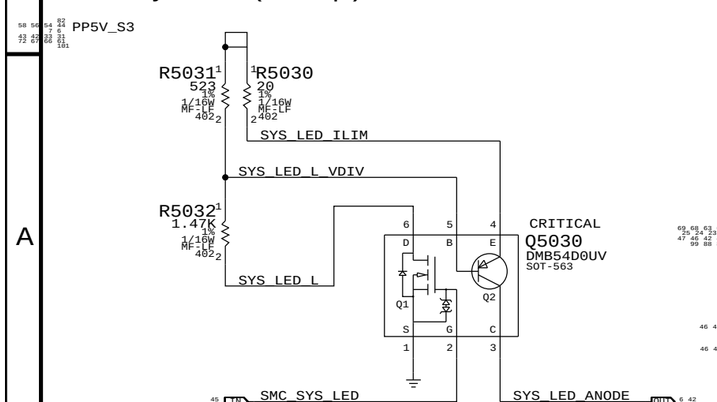
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	Intersil ISL60002-33

SMC Crystal Circuit

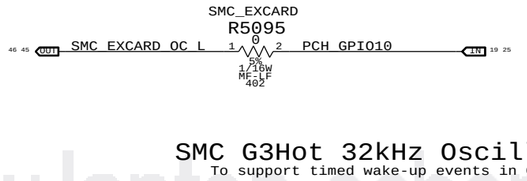


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0350	1	OSC,XTAL,32.768KHZ,LF,HF	U5010	CRITICAL	SMC_OSC_YES

System (Sleep) LED Circuit

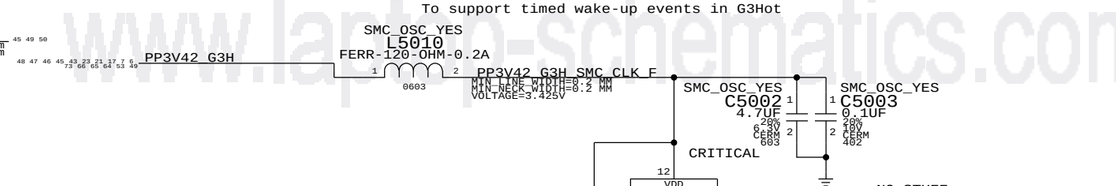


SMC_EXCARD

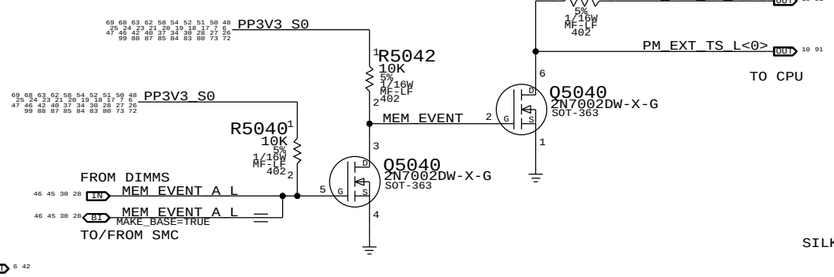


SMC G3Hot 32kHz Oscillator

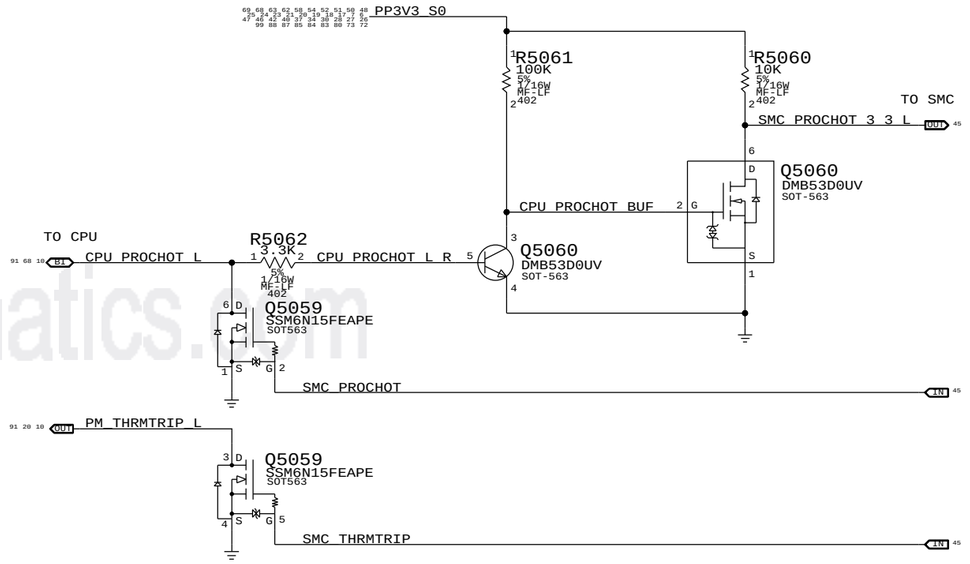
To support timed wake-up events in G3Hot



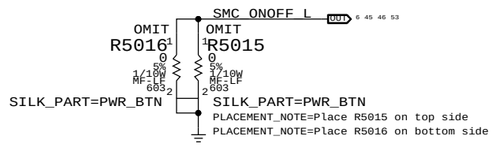
CPU PM_EXTTS_L / MEM_EVENT_L Level Shifting

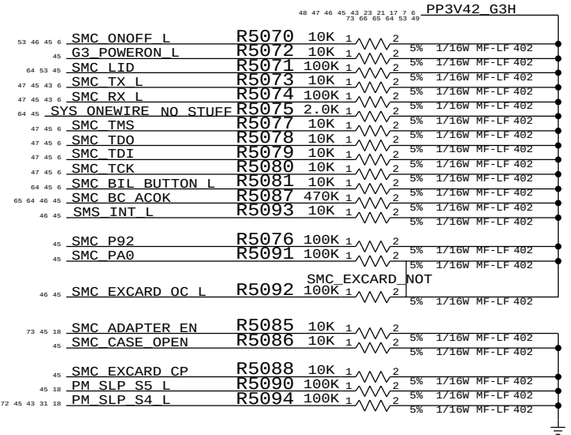


SMC FSB to 3.3V Level Shifting

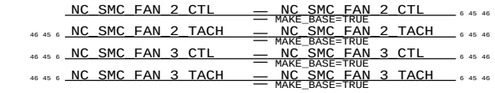


Debug Power "Buttons"





SMC_OSC_YES



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SYNC_MASTER=K18_SENSORS	SYNC_DATE=06/29/2009
PAGE TITLE	SMC Support
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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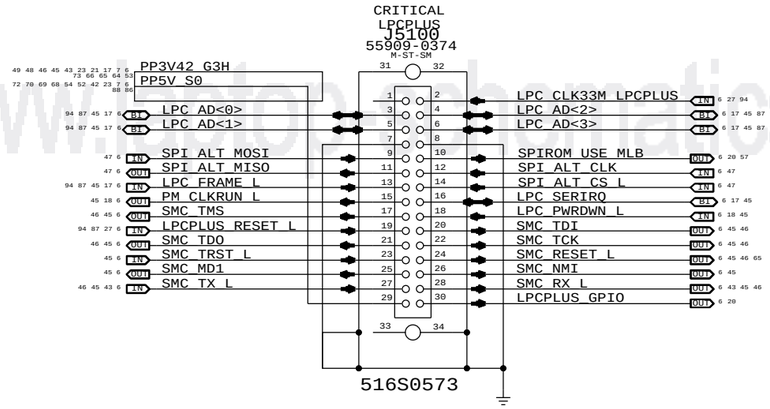
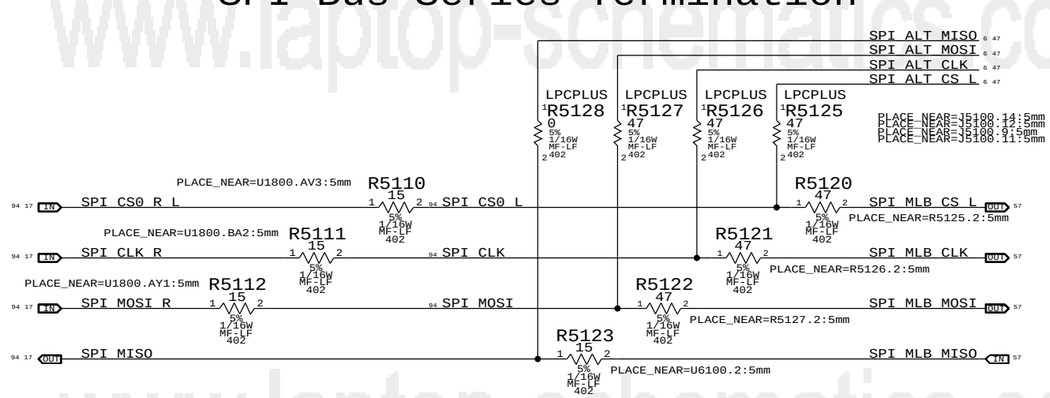
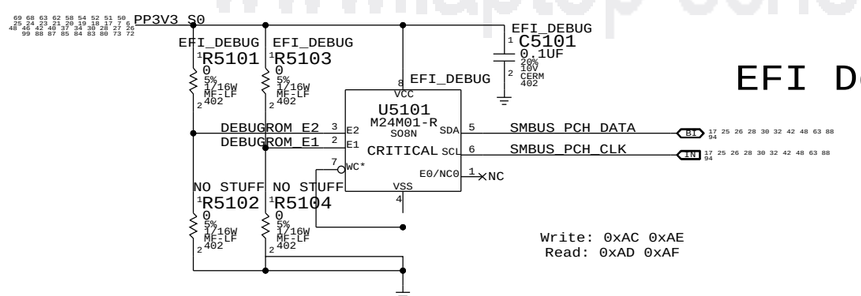
LPC+SPI Connector



SPI Bus Series Termination



EFI Debug ROM



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SYNC_MASTER=K17_MLB SYNC_DATE=06/23/2009

PAGE TITLE
LPC+SPI Debug Connector

Apple Inc.

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PCH SMBus "0" Connections

PP3V3_S0

R5200 1K 5% 1/16W MF-LF 402
R5201 1K 5% 1/16W MF-LF 402

Ibex Peak-M
U1800
(MASTER)

- SMBUS_PCH_CLK
- SMBUS_PCH_DATA
- MAKE_BASE=TRUE

SO-DIMM "A"
J2900
(Write: 0xA0 Read: 0xA1)

- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

VRef DACs
U2900
(Write: 0x98 Read: 0x99)

- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

SO-DIMM "B"
J3100
(Write: 0xA4 Read: 0xA5)

- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

Margin Control
U2901
(Write: 0x30 Read: 0x31)

- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

CK505 (Clock)
U2700
(Write: 0xD2 Read: 0xD3)

- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

EFI Debug Serial
U5101
(Write: 0xAC/AE Read: 0xAD/AF)

- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

LED BACKLIGHT
U9701
(WRITE: 0x58 READ: 0x59)

- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

XDP Connectors
J2600 & J2650
(MASTER)

- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

Mikey
U6800
(Write: 0x72 Read: 0x73)

- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

HDD Redriver Control A
U4510
(Write: 0x94 Read: 0x95)

- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

PCH "SMLink 0" Connections

PP3V3_S0

R5210 8.2K 5% 1/16W MF-LF 402
R5211 8.2K 5% 1/16W MF-LF 402

Ibex Peak-M
U1800
(MASTER)

- SML_PCH_0_CLK
- SML_PCH_0_DATA
- MAKE_BASE=TRUE

PCH "SMLink 1" Connections

PP3V3_S0

NO STUFF
R5220 8.2K 5% 1/16W MF-LF 402
NO STUFF
R5221 8.2K 5% 1/16W MF-LF 402
R5223 0 5% 1/16W MF-LF 402
R5222 0 5% 1/16W MF-LF 402

Ibex Peak-M
U1800
(Write: 0x90 Read: 0x91)

- SML_PCH_1_CLK
- SML_PCH_1_DATA
- MAKE_BASE=TRUE

SMLink 1 is slave port to
access PCH & CPU via PECI.

SMC "0" SMBus Connections

PP3V3_S0

R5250 4.7K 5% 1/16W MF-LF 402
R5251 4.7K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)

- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA
- MAKE_BASE=TRUE

GPU Temp (Ext)
EMC1414-A: U5550
(Write: 0x98 Read: 0x99)

- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA

GPU Temp (Int)
GT216: U8000
(Write: 0x9E Read: 0x9F)

- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA

SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state

PP3V3_S3

R5270 1K 5% 1/16W MF-LF 402
R5271 1K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)

- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA
- MAKE_BASE=TRUE

Trackpad
J5800
(Write: 0x90 Read: 0x91)

- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

ALS
J3401
(Write: 0x72 Read: 0x73)

- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

SMC "B" SMBus Connections

PP3V3_S0

R5260 4.7K 5% 1/16W MF-LF 402
R5261 4.7K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)

- SMBUS_SMC_B_S0_SCL
- SMBUS_SMC_B_S0_SDA
- MAKE_BASE=TRUE

CPU Temp
EMC1414-A: U5570
(Write: 0x98 Read: 0x99)

- SMBUS_SMC_B_S0_SCL
- SMBUS_SMC_B_S0_SDA

SMC "Battery A" SMBus Connections

PP3V42_G3H

R5280 1K 5% 1/16W MF-LF 402
R5281 1K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)

- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA
- MAKE_BASE=TRUE

Battery Charger
ISL6258 - U7000
(Write: 0x12 Read: 0x13)

- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA

Battery
J6955
(See Table)

- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA

Battery

Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x90 Read: 0x91)

SMC "Management" SMBus Connections

The bus formerly known as "Battery B"

PP3V3_S3

R5290 4.7K 5% 1/16W MF-LF 402
R5291 4.7K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)

- SMBUS_SMC_MGMT_SCL
- SMBUS_SMC_MGMT_SDA
- MAKE_BASE=TRUE

Sensor ADC A
U5930
(Write: 0x10 Read: 0x11)

- SMBUS_SMC_MGMT_SCL
- SMBUS_SMC_MGMT_SDA

SYNC_MASTER=K18_SENSORS SYNC_DATE=06/18/2009

PAGE TITLE
K18 SMBus Connections

Apple Inc.

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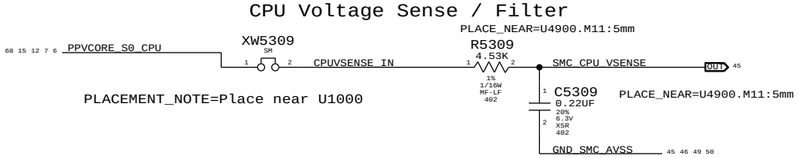
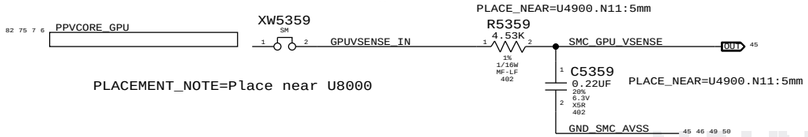
CPU Voltage Sense / Filter



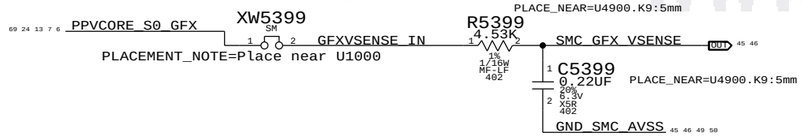
PLACEMENT_NOTE=Place near U1000

GPU Voltage Sense / Filter



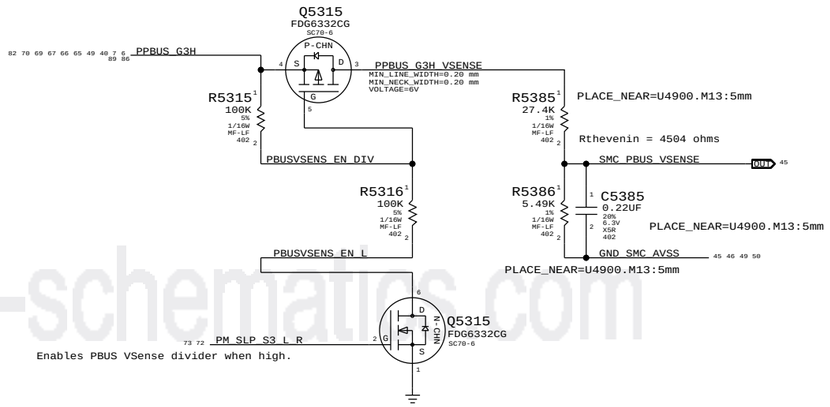
PLACEMENT_NOTE=Place near U8000

GFX Voltage Sense / Filter



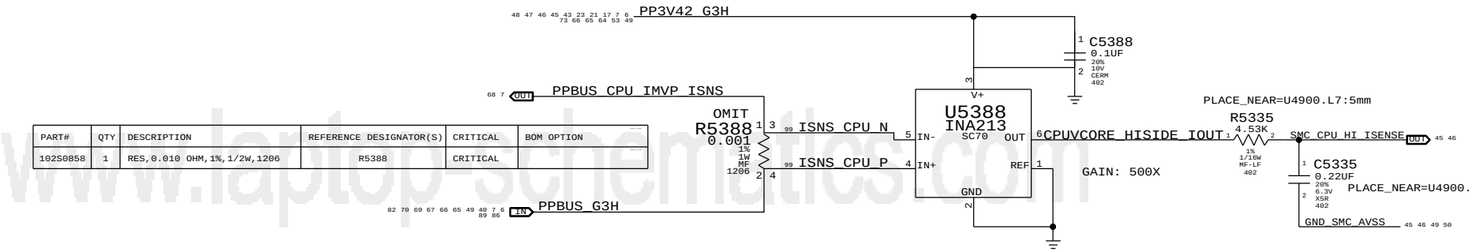
PLACEMENT_NOTE=Place near U1000

PBUS Voltage Sense & Filter



Enables PBUS VSense divider when high.

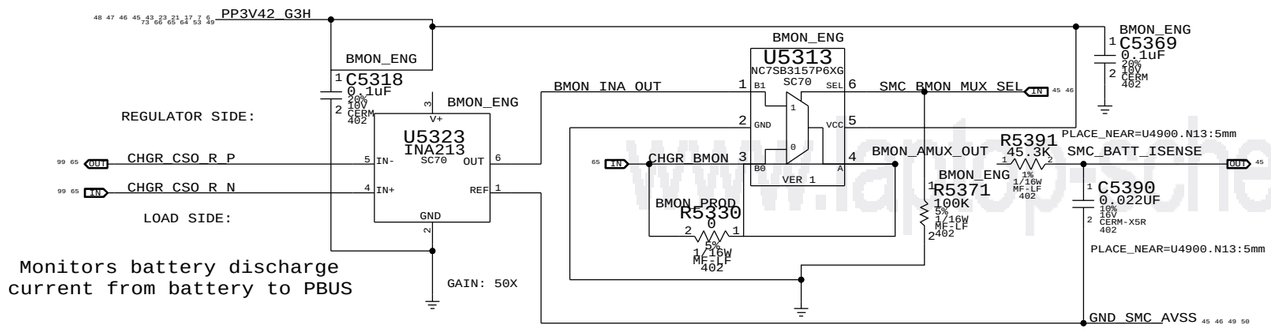
CPU VCore High Side Current Sensor



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
102S0858	1	RES,0.010 OHM,1%,1/2W,1206	R5388	CRITICAL	

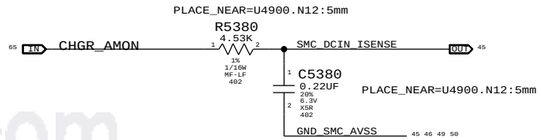
EDP for PPVIN_S5_CPU_IMVP_ISNS_R = 5.867 amps for K18.

BMON Current Sense - Entire circuit must be near SMC (U4900)



U5303 only senses current up to 6.6A

DCIN Current Sense Filter



SYNC_MASTER=K18_SENSORS SYNC_DATE=06/29/2009

PAGE TITLE: Current & Voltage Sensing

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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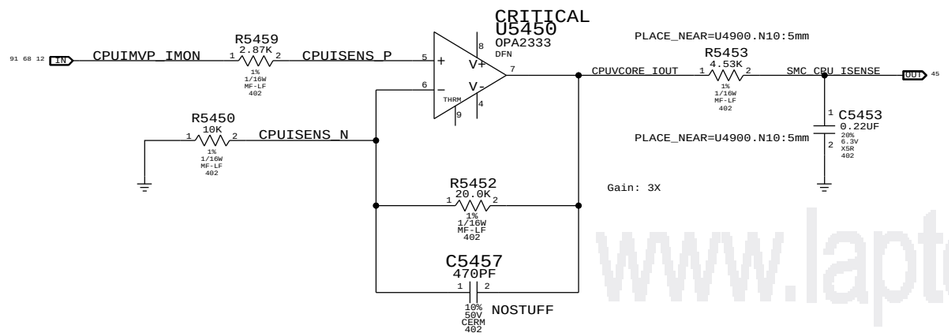
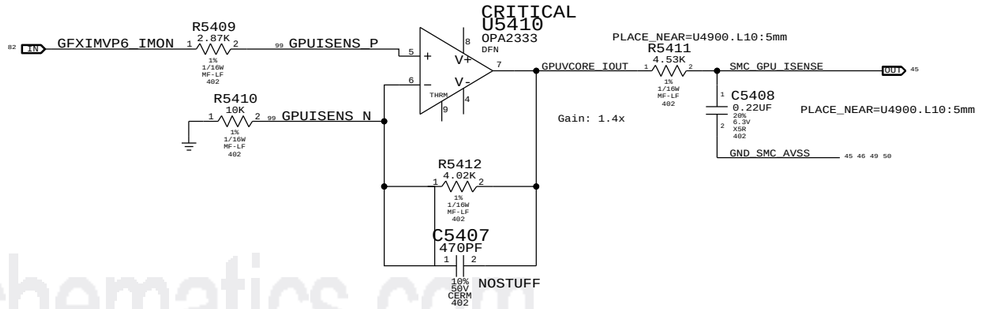
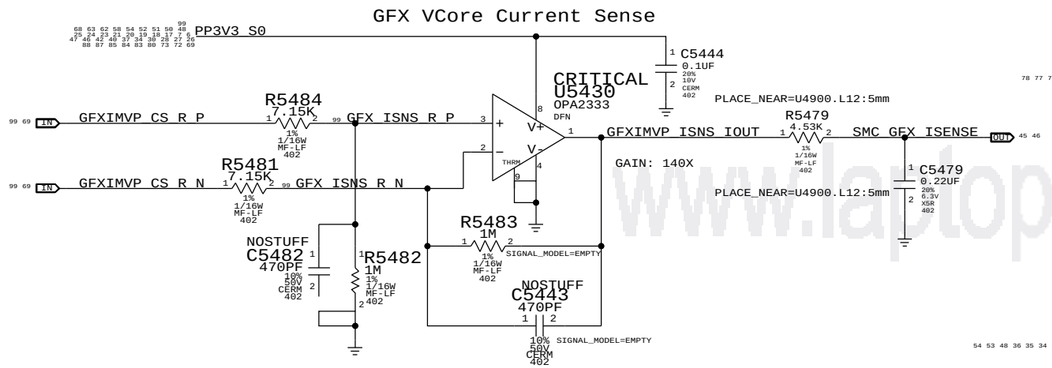
CPU VCore Load Side Current Sense / Filter



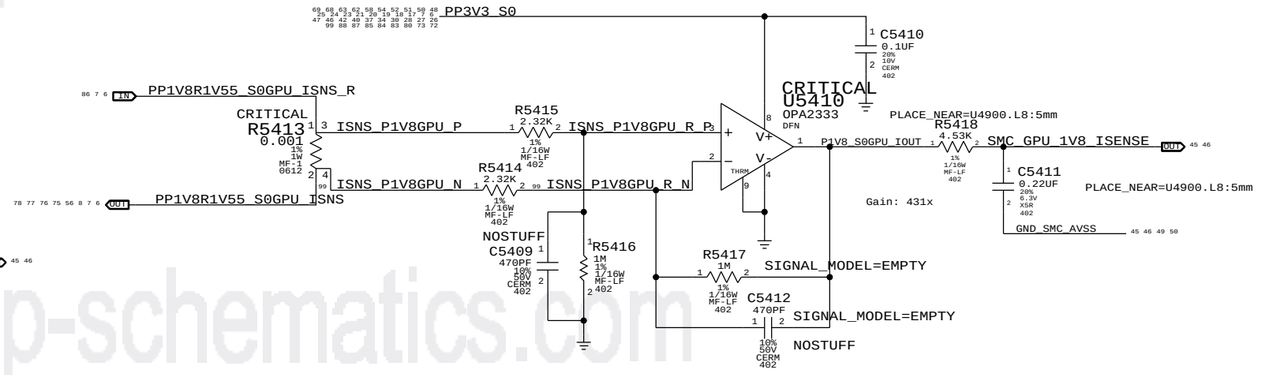
GPU VCore Current Sense



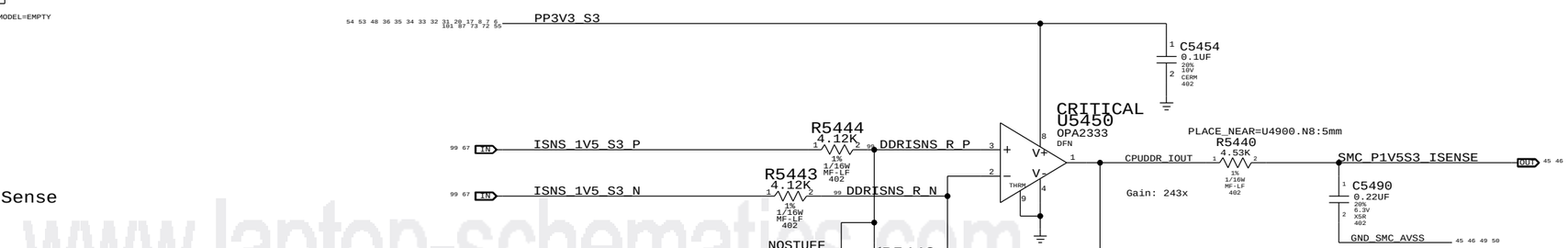
GFX VCore Current Sense



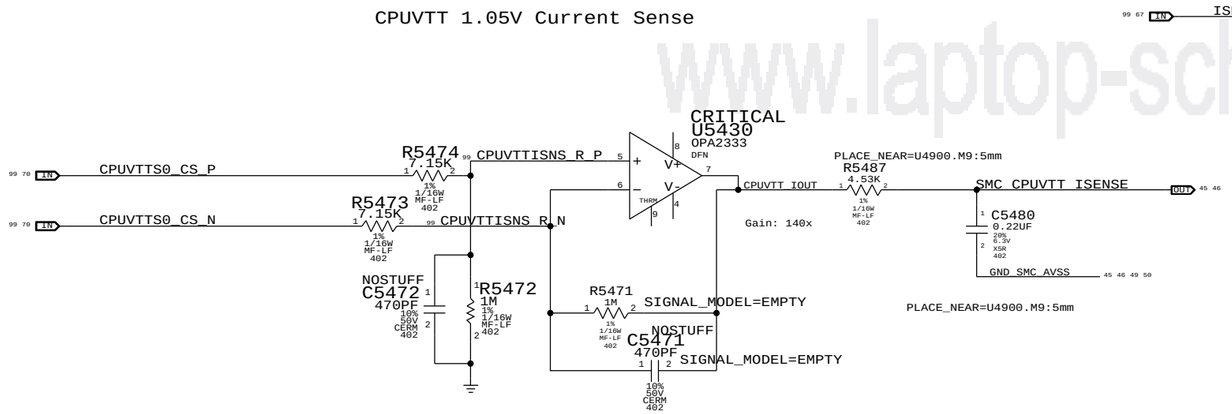
1.8V FB Current Sense



CPU & MEM 1.5V S3 (DDR) Current Sense



CPUVTT 1.05V Current Sense



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SYNC_MASTER=K18_SENSORS SYNC_DATE=07/02/2009

PAGE TITLE: Current Sensing

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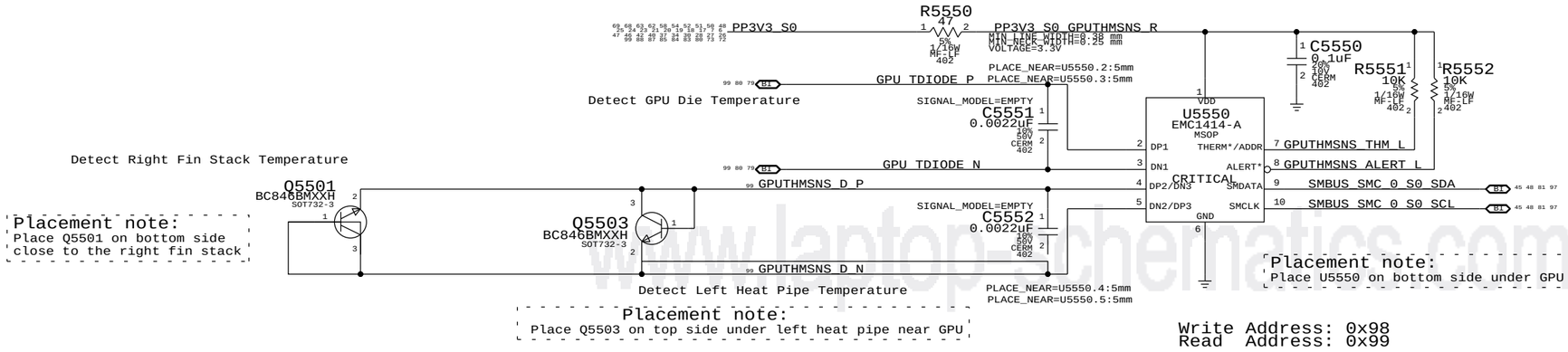
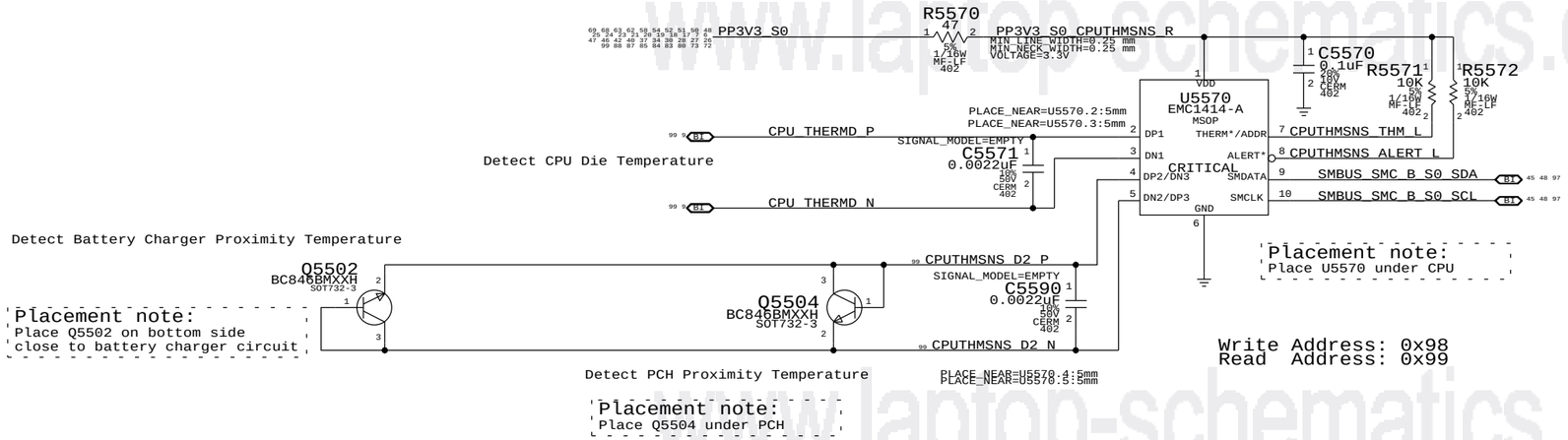
SHEET	50 OF 101

GPU Proximity/GPU Die/Left Heat Pipe/Right Fin Stack



CPU Proximity/CPU Die/PCH Proximity/Battery Charger Proximity



Note: EMC1414 can perform Beta Compensation for External Diode 1 only

www.laptop-schematics.com

SYNC_MASTER=K18_SENSORS SYNC_DATE=06/18/2009

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 55 OF 132

SHEET: 51 OF 101

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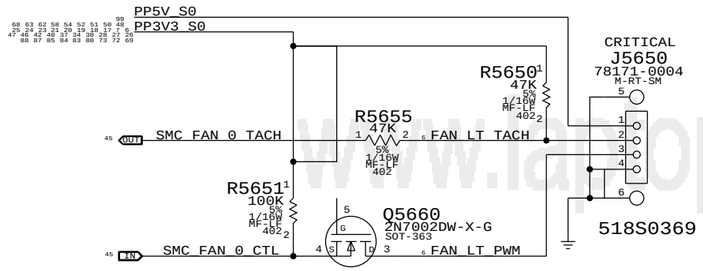
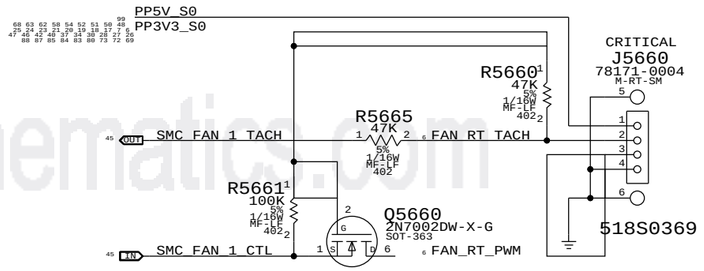
Left Fan



Right Fan



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SYNC_MASTER=K19_MLB SYNC_DATE=05/29/2009

PAGE TITLE: Fan Connectors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 56 OF 132

SHEET: 52 OF 101

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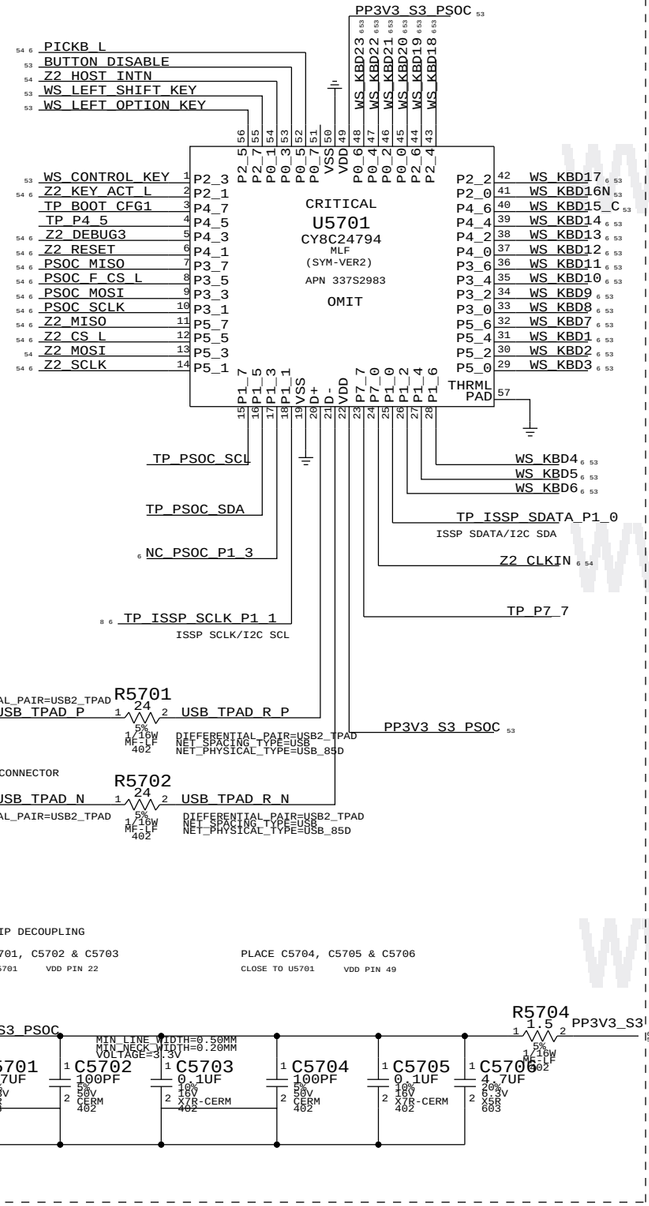
PSOC USB CONTROLLER

USB INTERFACES TO MLB
SPI HOST TO Z2

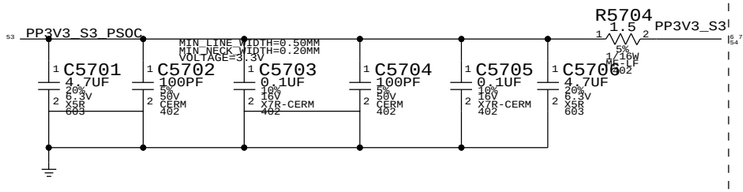
TRACKPAD PICK BUTTONS
KEYBOARD SCANNER



U5701 CHIP DECOUPLING

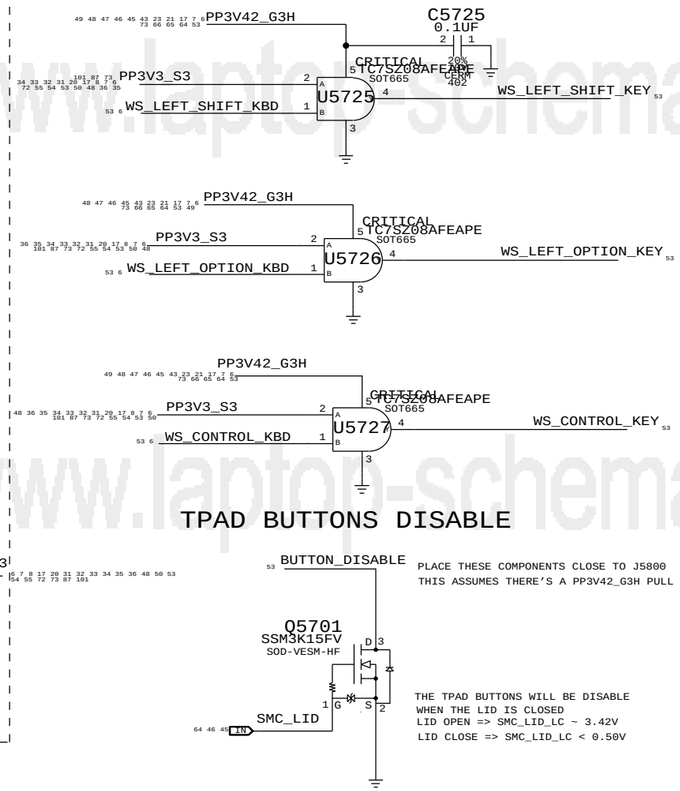
PLACE C5701, C5702 & C5703
CLOSE TO U5701 VDD PIN 22

PLACE C5704, C5705 & C5706
CLOSE TO U5701 VDD PIN 49



IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA MAX	10 OHM	0.6 V	36E-3 W
	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

ISOLATION CIRCUIT

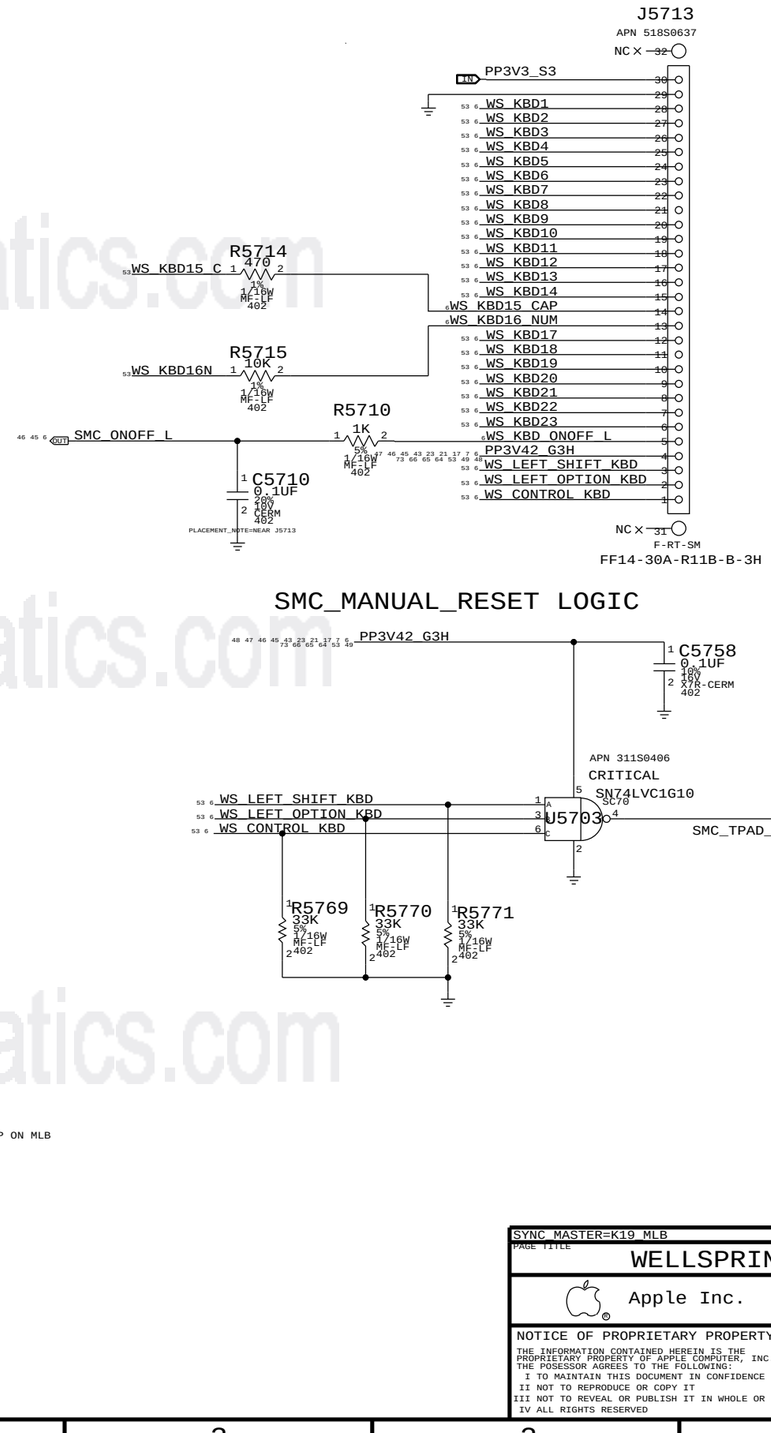


TPAD BUTTONS DISABLE

PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

KEYBOARD CONNECTOR



SMC_MANUAL_RESET LOGIC

www.laptop-schematics.com

SYNC_MASTER=K19_MLB SYNC_DATE=05/29/2009

PAGE TITLE: WELLSPRING 1

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 57 OF 132
SHEET: 53 OF 101

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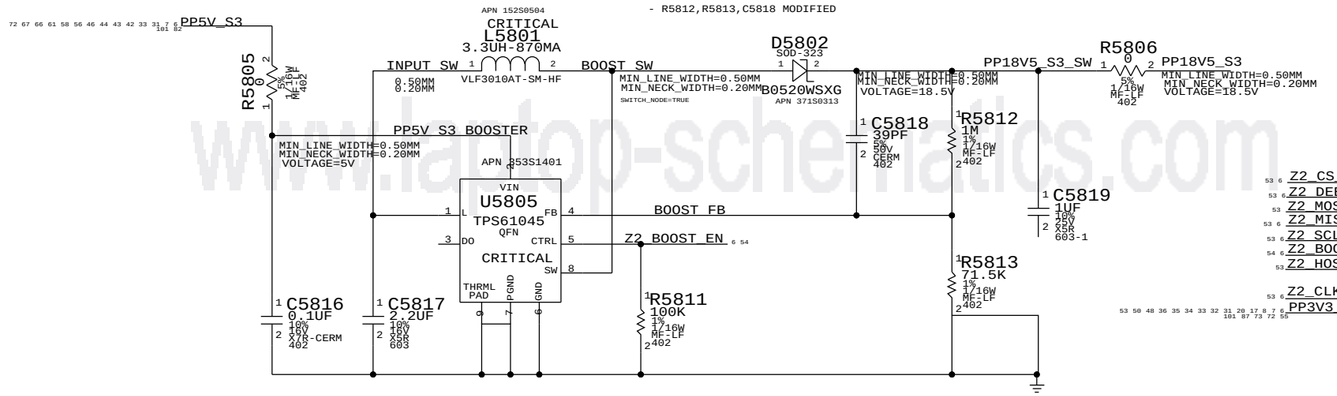
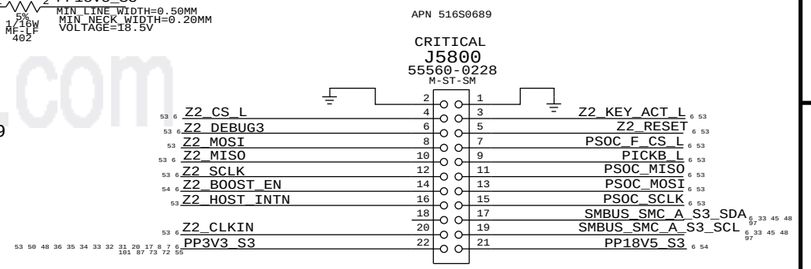
BOOSTER +18.5VDC FOR SENSORS

BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD FLEX CONNECTOR



To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:

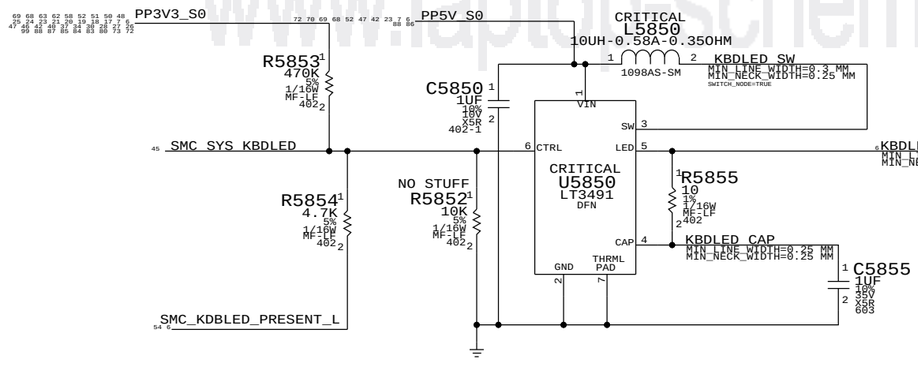
LOW = keyboard backlight present

HIGH= keyboard backlight not present

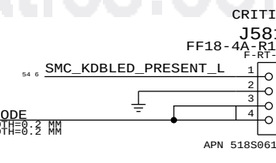
BOM OPTION: KBDLED_YES

R5853 ALWAYS PRESENT

Keyboard LED Driver



KBD BACKLIGHT CONNECTOR



J5815 pin 1 is grounded on keyboard backlight flex

SYNC_MASTER=K19_MLB	SYNC_DATE=05/29/2009
PAGE TITLE	WELLSPRING 2
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 58 OF 132
	SHEET 54 OF 101

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Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC

PP3V3_S3

R5921 10K 5% 1/10W MF-LF 402

NO STUFF

C5922 0.1UF 10% 10V X5R 402

C5926 10UF 20% 4V X5R 603

U5920 AP344ALH LGA

SMS_PWRDN

SMS_PWRDN

MAKE_BASE=TRUE

SMS_SELFTEST

CRITICAL

NO STUFF R5922 10K 5% 1/16W MF-LF 402

SMS_X_AXIS

SMS_Y_AXIS

SMS_Z_AXIS

C5923 0.1UF 10% 10V X5R 402

C5924 0.1UF 10% 10V X5R 402

C5925 0.1UF 10% 10V X5R 402

PLACE CAPS ON SMS OUTPUT SIGNALS CLOSE TO SMC

R5940 0 5% 1/16W MF-LF 402

R5941 0 5% 1/16W MF-LF 402

R5942 0 5% 1/16W MF-LF 402

Desired orientation when placed on board top-side:

+Y, +X, +Z (up), Front of system

Circle indicates pin 1 location when placed in correct orientation

Alternate location Analog SMS

PP3V3_S3

NO STUFF C5932 0.1UF 10% 10V X5R 402

NO STUFF C5936 10UF 20% 4V X5R 603

U5930 AP344ALH LGA

SMS_ALT_SELFTEST

CRITICAL

R5932 10K 5% 1/16W MF-LF 402

SMS_ALT_X_AXIS

SMS_ALT_Y_AXIS

SMS_ALT_Z_AXIS

Desired orientation when placed on board top-side:

+Y, +X, +Z (up), Front of system

Circle indicates pin 1 location when placed in correct orientation

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SYNC_MASTER=K19_MLB SYNC_DATE=05/29/2009

PAGE TITLE: Sudden Motion Sensor (SMS)

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 59 OF 132

SHEET: 55 OF 101

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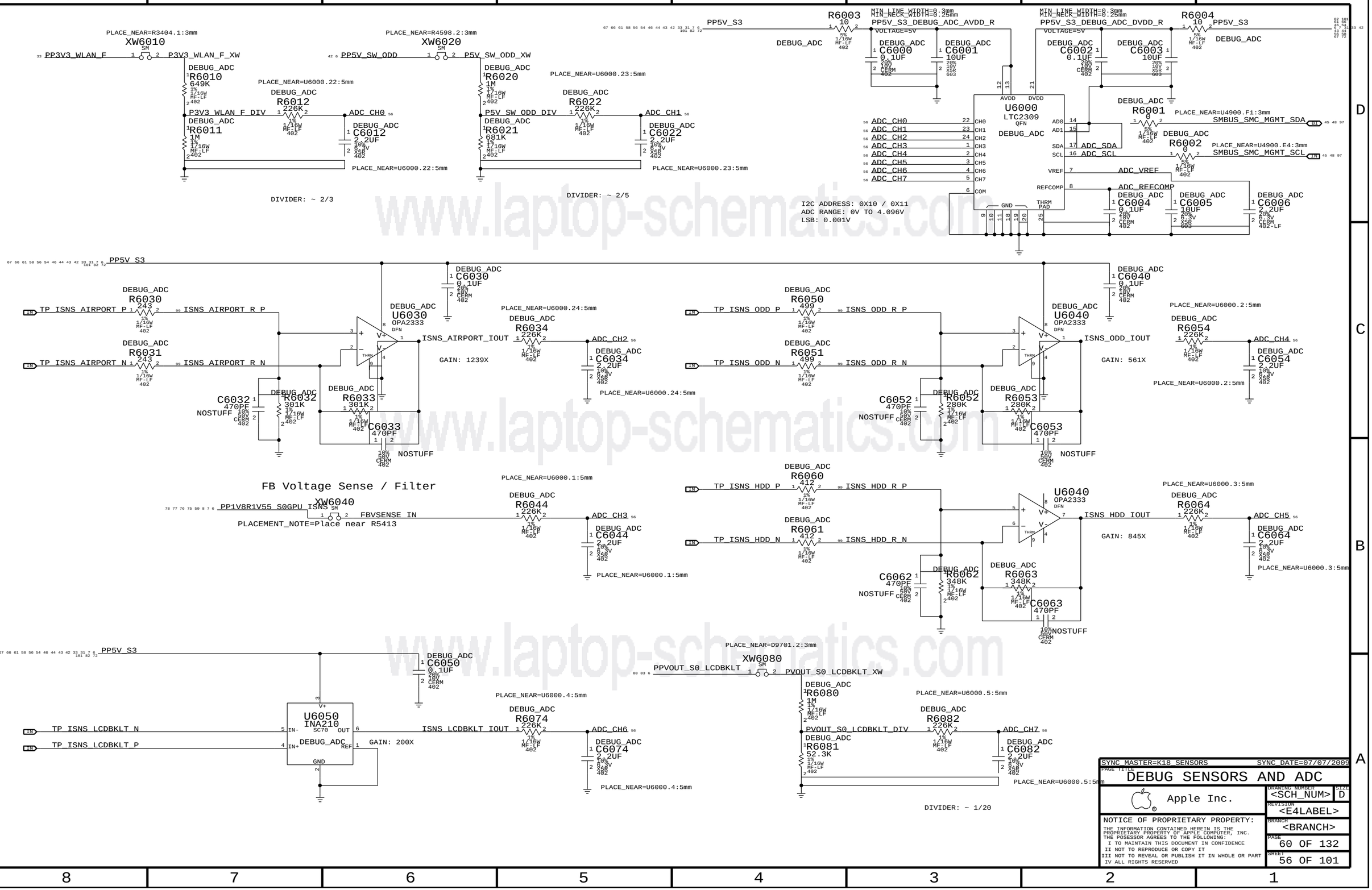

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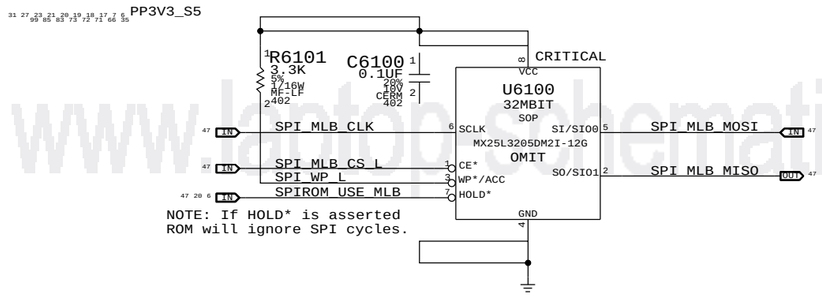

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SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE

SPI ROM

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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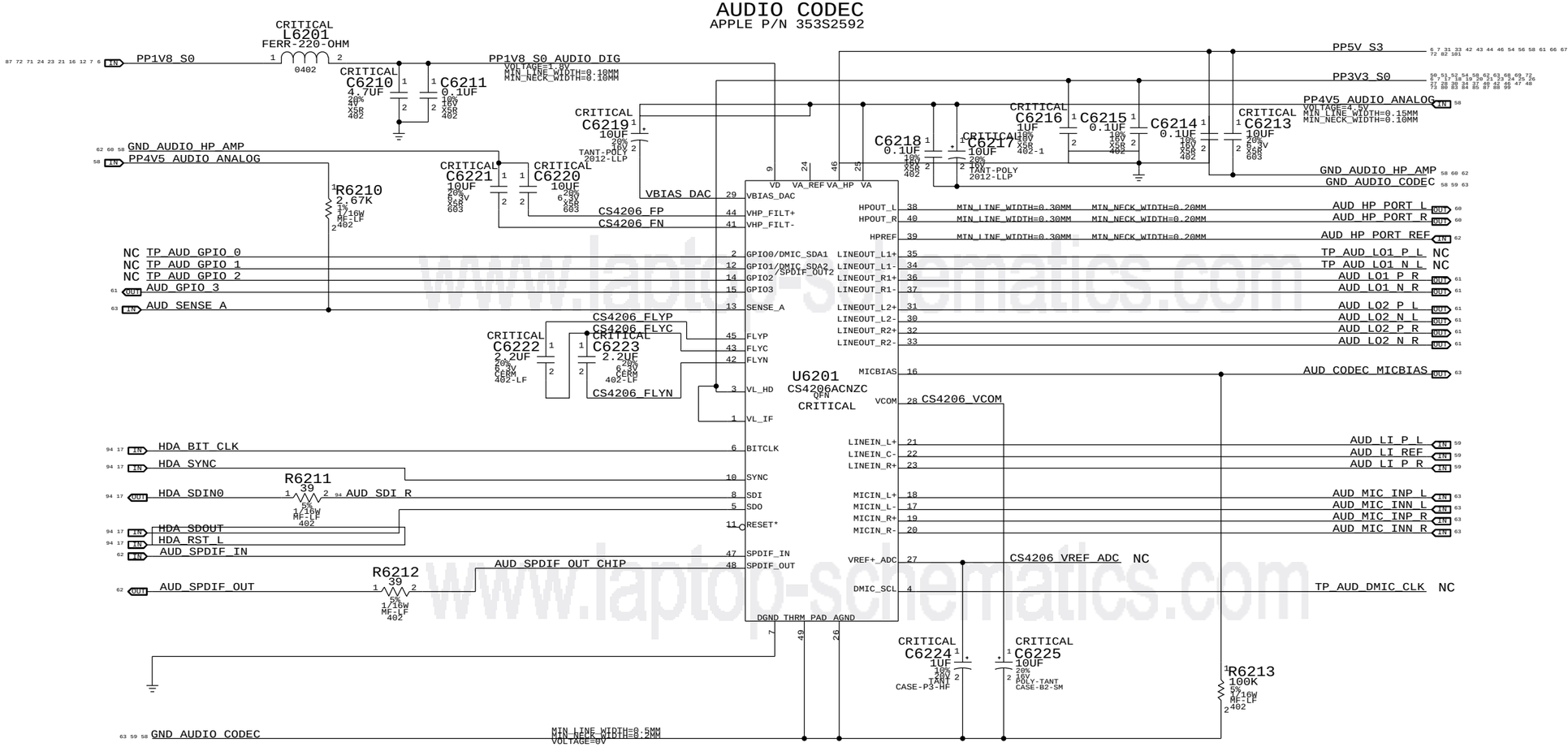
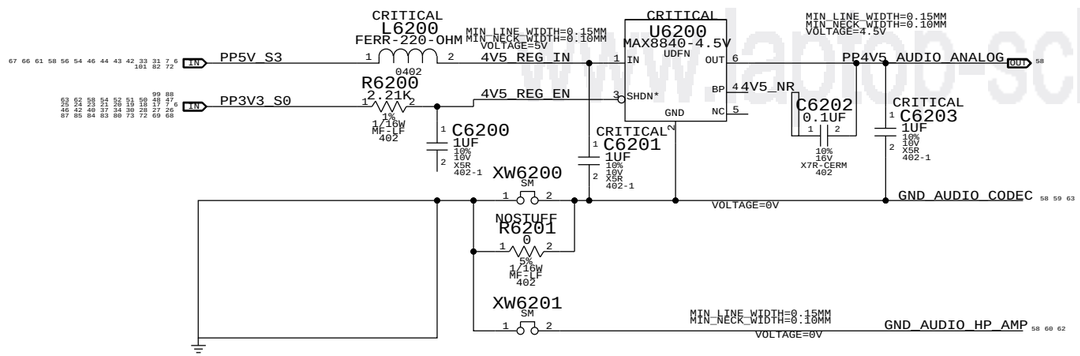
AUDIO CODEC
APPLE P/N 353S2592



4.5V POWER SUPPLY FOR CODEC
APPLE P/N 353S2234



NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC_MASTER=K18_AUDIO SYNC_DATE=09/21/2009

PAGE TITLE
AUDIO: CODEC/REGULATOR

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 62 OF 132
SHEET 58 OF 101

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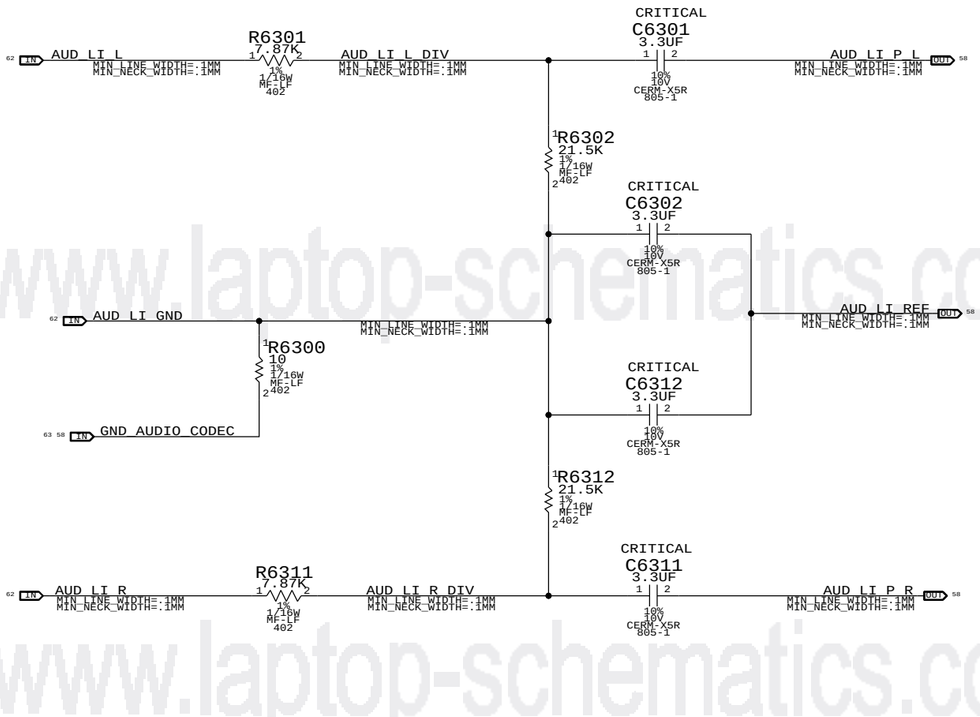
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 18K OHMS
FC = 8 HZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS



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SYNC_MASTER=K18_AUDIO SYNC_DATE=07/29/2009

PAGE TITLE
AUDIO: LINE INPUT FILTER

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 63 OF 132
SHEET 59 OF 101

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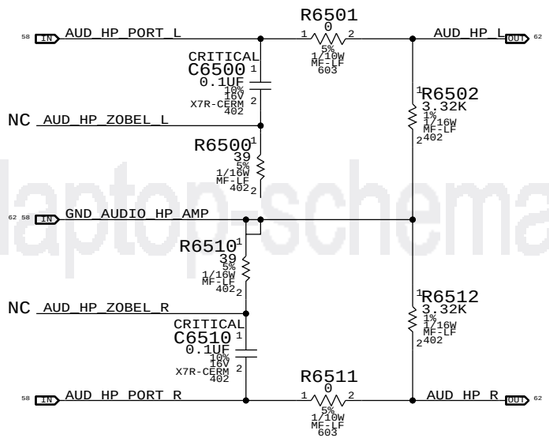
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



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SYNC_MASTER=K18_AUDIO SYNC_DATE=07/29/2009

PAGE TITLE
AUDIO: HEADPHONE FILTER

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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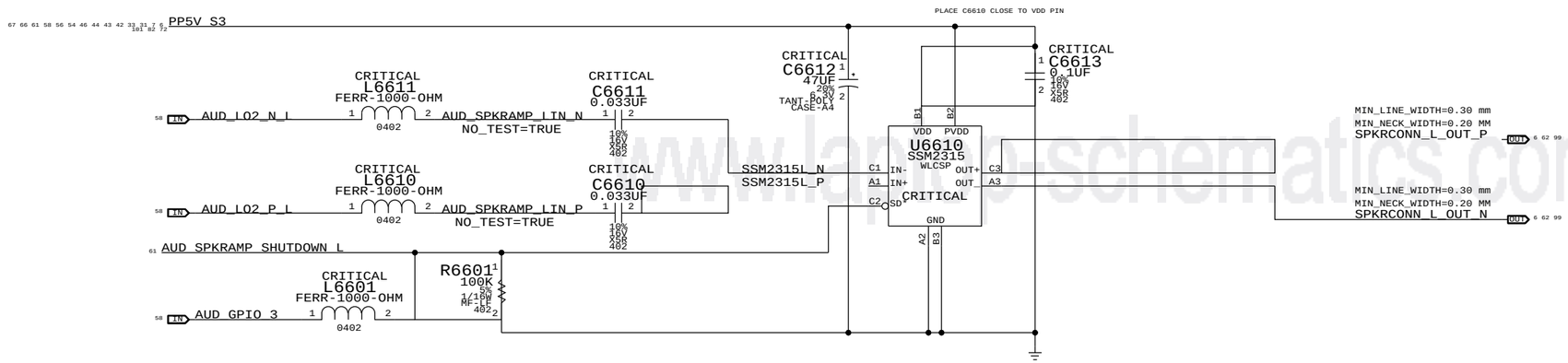
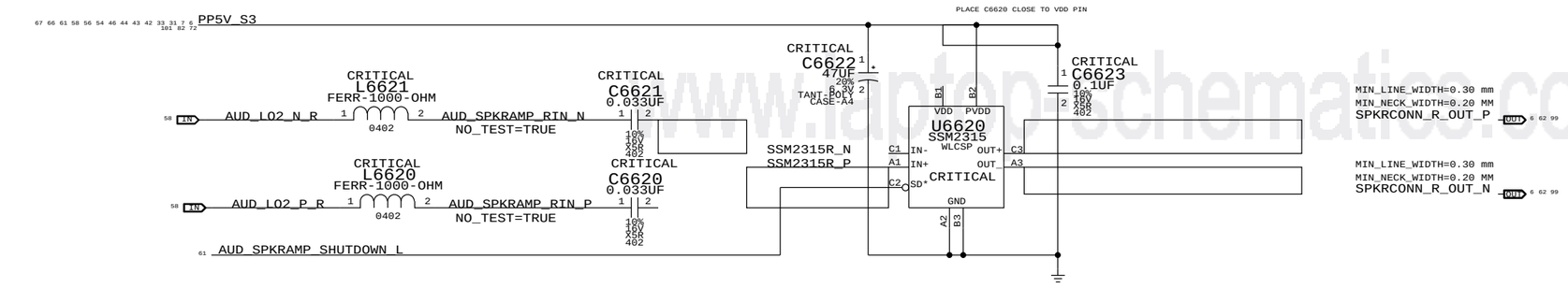
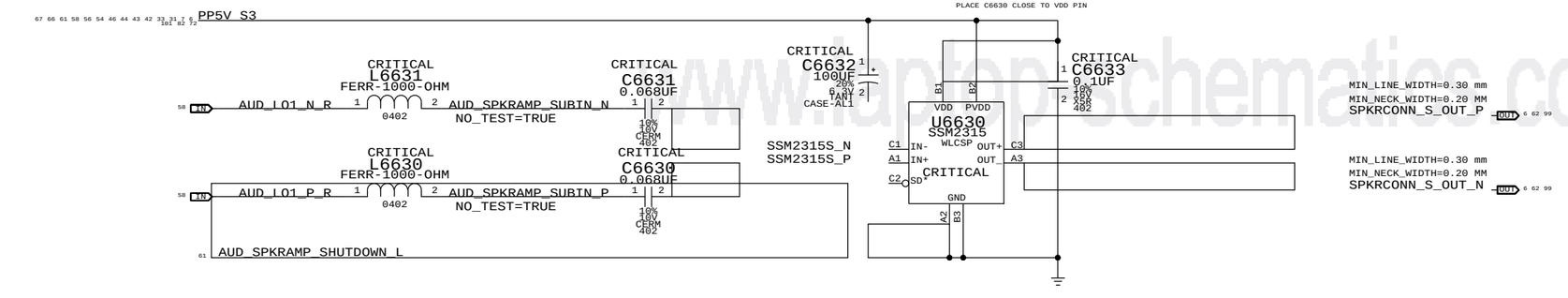
3X MONO SPEAKER AMPLIFIERS (SSM2315)
APN: 353S2500

GAIN = 6DB
1ST ORDER FC (L&R) = 120 HZ +/- 30%
1ST ORDER FC (SUB) = 58HZ +/- 30%







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SYNC_MASTER=K18_AUDIO SYNC_DATE=07/29/2009

PAGE TITLE
AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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SHEET 61 OF 101

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AUDIO JACK 1 LO/HP JACK, SPDIF TX

PP3V3_S0

APN: 514-0671

J6700
SPDIF-TXRX-K24
F-RT-TH

AUDIO
MIC 6
DETECT 5
SWITCH 2
LEFT 1
RIGHT 3
GND 4

AUD_CONNJ1_SLEEVE2
AUD_CONNJ1_SLEEVEDET
AUD_CONNJ1_TIPDET
AUD_CONNJ1_TIP
AUD_CONNJ1_RING
AUD_CONNJ1_SLEEVE

A - VIN 7
B - VCC 8
C - GND 9
OPERATING VOLTAGE 3.3
POF

SHELL 10
SHIELD PINS 11 12 13

C6700 0.1UF 10% 10V X5R 402
C6701 2.2UF 20% 6.3V CERM 402-LF

CRITICAL DZ6703 6.8V-100PF 402
CRITICAL DZ6704 6.8V-100PF 402
CRITICAL DZ6700 6.8V-100PF 402
CRITICAL DZ6706 6.8V-100PF 402
CRITICAL DZ6701 6.8V-100PF 402

C6705 100PF 5% 50V C0G CERM 402

MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.10 MM
VOLTAGE=0V

GND_CHASSIS_AUDIO_JACK 8 62

AUD_SPDIF_OUT IN 58

CRITICAL L6703 FERR-1000-OHM 0402
HS_MIC_P OUT 63

CRITICAL L6702 FERR-1000-OHM 0402
HS_MIC_N OUT 63

CRITICAL L6707 FERR-220-OHM 0402
AUD_HP_PORT_REF BI 58

CRITICAL L6701 FERR-220-OHM-2.5A 0603
GND_AUDIO_HP_AMP OUT 58 60

CRITICAL L6704 FERR-220-OHM 0402
AUD_HP_R BI 60

CRITICAL L6706 FERR-220-OHM 0402
AUD_HP_L BI 60

R6700 10K 5% 1/16W MF-LF 402
AUD_J1_SLEEVEDET_R OUT 63

CRITICAL L6705 FERR-1000-OHM 0402
AUD_J1_TIPDET_R OUT 63

MIC CONNECTOR

APN: 518S0520

CRITICAL J6780 78171-0003 M-RT-SM
BI_MIC_N OUT 63 6
BI_MIC_SHIELD OUT 63 6
BI_MIC_P OUT 63 6

SPEAKER CONNECTOR

APN: 518S0519

CRITICAL J6781 78171-0002 M-RT-SM
SPKRCONN_L_OUT_P IN 99 61 6
SPKRCONN_L_OUT_N IN 99 61 6

APN: 518S0521

CRITICAL J6782 78171-0004 M-RT-SM
SPKRCONN_S_OUT_P IN 99 61 6
SPKRCONN_S_OUT_N IN 99 61 6
SPKRCONN_R_OUT_P IN 99 61 6
SPKRCONN_R_OUT_N IN 99 61 6

NOSTUFF CRITICAL C6783 33PF 5% 50V C0G CERM 402
NOSTUFF CRITICAL C6784 33PF 5% 50V C0G CERM 402
NOSTUFF CRITICAL C6781 33PF 5% 50V C0G CERM 402
NOSTUFF CRITICAL C6782 33PF 5% 50V C0G CERM 402

XW6701 SM
GND PATCH
XW6702 SM
R6701 0 5% 1/16W MF-LF 402
GND_CHASSIS_AUDIO_JACK 62 8

AUDIO JACK 2 LINE IN JACK, SPDIF RX

PP3V3_S0

APN: 514-0635

J6750
AUDIO-RCVR-M97
F-RT-TH5

AUDIO
DETECT_FOR_PLUG_TYPE 5
SWITCH 2
LEFT 1
RIGHT 3
GROUND 4

A - VDD 6
B - GND 7
C - VOUT 8
OPERATING VOLTAGE 3.3
POF

SHELL 9
SHIELD PINS 10 11 12

C6750 1UF 10% 10V X5R 402-1

AUD_J2_OPT_OUT
R6749 4.7 5% 1/16W MF-LF 402
AUD_SPDIF_IN OUT 58

AUD_CONNJ2_TIPDET
AUD_CONNJ2_RING
AUD_CONNJ2_TIP
AUD_CONNJ2_SLEEVE

CRITICAL DZ6757 ESDALC5-1BM2 SOD882
CRITICAL DZ6758 ESDALC5-1BM2 SOD882
CRITICAL DZ6754 6.8V-100PF 402
CRITICAL DZ6756 6.8V-100PF 402

CRITICAL L6754 FERR-1000-OHM 0402
AUD_LI_R BI 59

CRITICAL L6756 FERR-1000-OHM 0402
AUD_LI_L BI 59

CRITICAL L6758 600-OHM-300MA 0402
AUD_LI_GND 59

CRITICAL L6752 FERR-1000-OHM 0402
AUD_J2_TIPDET_R OUT 63

C6756 100PF 5% 50V C0G CERM 402

GND_CHASSIS_AUDIO_JACK 8 62

SYNC_MASTER=K18_AUDIO	SYNC_DATE=07/29/2009
PAGE TITLE: AUDIO: JACKS	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	0X09 (A)
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0C (B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X05 (5)	0X0C (12,C)	N/A	0X0C (12,C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

SYSTEM INT AND GPIO LINES

FUNCTION	INT	GPIO
MIKEY ENABLE		SATA4GP/GPIO 16
MIKEY INTERRUPT	PIRQ H	GPIO 5
PERIPHERAL DETECT	PIRQ F	GPIO 3

PORT B LEFT(HEADSET MIC)
CRITICAL HP=80HZ, LP=8.82KHZ
MIKEY MIN_LINE_WIDTH=0.1MM
L6880 MIN_NECK_WIDTH=0.1MM
FERR-1000-OHM VOLTAGE=3.3V
PP3V3_S0 PP3V3_S0_HS_RX
DRC MIKEY
APN:353S2256
CRITICAL MIKEY
C6880 10UF
U6880 CD3275 DRC
PULLUPS ON MCP PAGE
SMBUS_PCH_CLK SCL
SMBUS_PCH_DATA SDA
AUD_I2C_INT_L INT*
AUD_IPHS_SWITCH_EN ENABLE
MICBIAS DETECT BYPASS GND THM
HS_MIC_BIAS HS_SW_DET HS_RX_BP
MIKEY CRITICAL C6882 2.2UF
GND_AUDIO_CODEC
MIKEY C6881 0.01UF
MIKEY R6881 1K
MIKEY R6882 2.2K
MIKEY CRITICAL C6883 0.1UF
MIKEY R6884 2.2K
AUD_MIC_INP_L HS_MIC_HI_RC HS_MIC_P
MIKEY CRITICAL C6886 0.1UF
MIKEY R6883 100K
MIKEY C6884 0.0082UF
MIKEY C6885 27PF
AUD_MIC_INN_L XW6880 SM
GND_AUDIO_CODEC HS_MIC_N

PORT A DETECT (HEADPHONES) PORT B DETECT(SPDIF DELEGATE)
AUD_SENSE_A
PP3V3_S0_AUDIO_F
R6801 220K
APN:376S0613
AUD_OUTJACK_INSERT_L
R6806 39.2K
R6805 20.0K
Q6800 SSM6N15FEAPE SOT563
Q6801 SSM6N15FEAPE SOT563
Q6801 SSM6N15FEAPE SOT563
AUD_PORTA_DET_L NC
AUD_PORTB_DET_L NC
R6802 47K
AUD_J1_TIPDET_R
AUD_J1_DET_RC
C6801 0.1UF
GND_AUDIO_CODEC
R6803 220K
AUD_J1_SLEEVEDET_INV
R6804 220K
Q6800 SSM6N15FEAPE SOT563
AUD_J1_SLEEVEDET_R
C6802 0.01UF
GND_AUDIO_CODEC
AUD_J1_SLEEVEDET_R

EXTRACTION NOTIFICATION
CRITICAL L6862 FERR-1000-OHM
PP3V3_S0 PP3V3_S0_AUDIO_F
MIN_LINE_WIDTH=0.1MM
MIN_NECK_WIDTH=0.1MM
VOLTAGE=3.3V
C6861 0.1UF
GND_AUDIO_CODEC
R6865 100K
AUD_PERPH_DET_R
R6861 100
AUD_IP_PERIPHERAL_DET
R6864 220K
AUD_J1_TIPDET_INV
Q6803 SSM6N15FEAPE SOT563
Q6803 SSM6N15FEAPE SOT563
R6860 15K
AUD_J1_TIPDET_R
TIPDET_FILT
C6860 0.1UF
GND_AUDIO_CODEC

PORT B RIGHT(BUILT-IN MIC)
R6850 100
R6851 2.4K
AUD_CODEC_MICBIAS
MIC_BIAS_FILT
CRITICAL C6852 2.2UF
GND_AUDIO_CODEC
CRITICAL C6850 0.1UF
AUD_MIC_INP_R
CRITICAL C6851 0.1UF
AUD_MIC_INN_R
R6853 2.4K
GND_AUDIO_CODEC
BI_MIC_HI_F
R6852 100K
BI_MIC_LO_F
CRITICAL C6853 0.001UF
CRITICAL C6854 27PF
L6850 FERR-1000-OHM
BI_MIC_P
L6851 FERR-1000-OHM
BI_MIC_N
XW6851 SM
BI_MIC_SHIELD
HP=80HZ

PORT C DETECT (LINE-IN)
AUD_SENSE_A
PP3V3_S0_AUDIO_F
R6813 10K
R6811 270K
AUD_INJACK_INSERT_L NC
Q6802 SSM3K15FV SOD-VESM-HF
APN:376S0612
R6812 47K
AUD_J2_TIPDET_R
AUD_J2_DET_RC
C6811 0.1UF
GND_AUDIO_CODEC

SYNC_MASTER=K18_AUDIO SYNC_DATE=07/29/2009
PAGE TITLE
AUDIO: JACK TRANSLATORS
Apple Inc.
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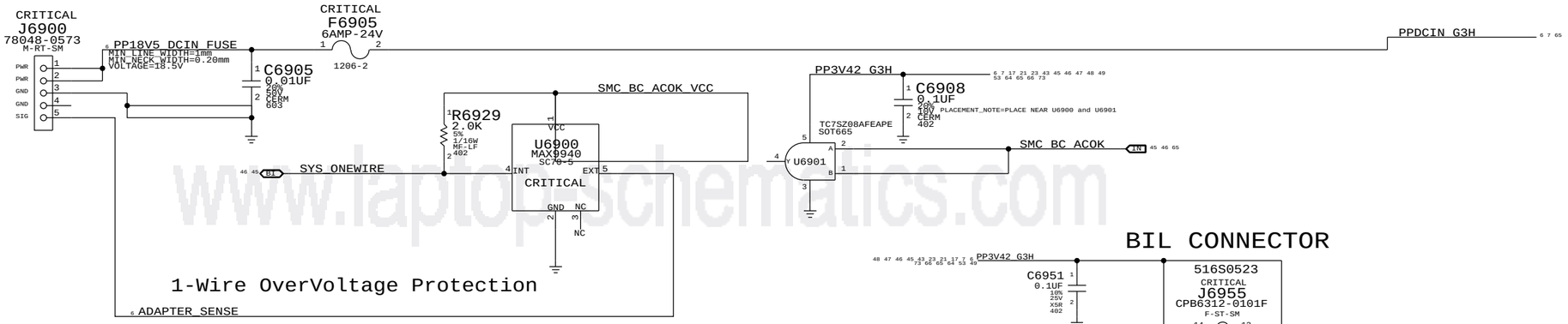
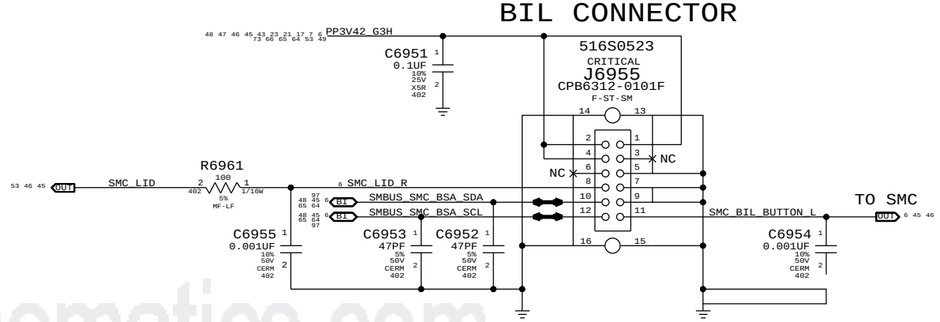
MagSafe DC Power Jack



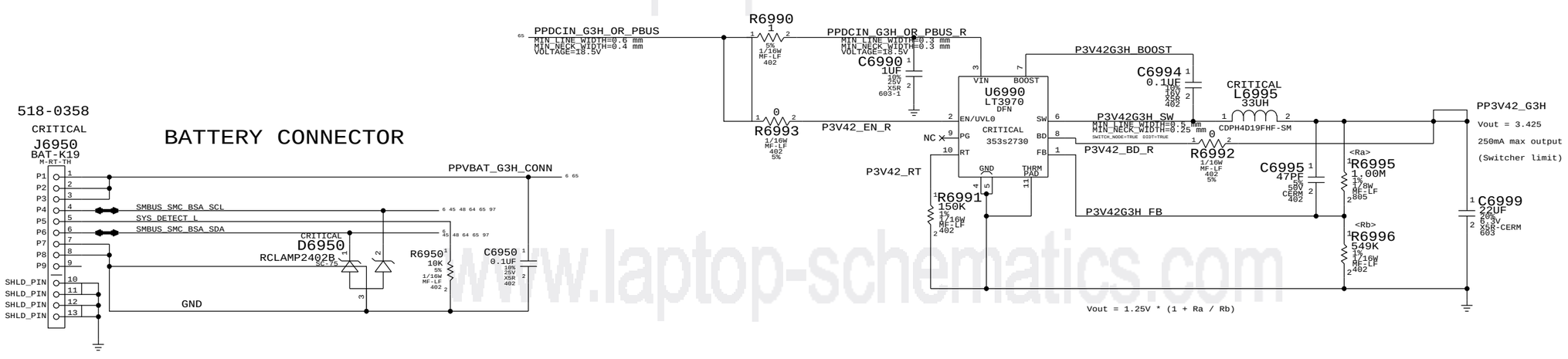
The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.

BIL CONNECTOR



3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



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SYNC_MASTER=K18_POWER SYNC_DATE=06/30/2009

PAGE TITLE: DC-In & Battery Connectors

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Reverse-Current Protection

Inrush Limiter

This node is powered through body diodes:
* DCIN through Q7080.
* PBUS through Q7085, Charger TOP FETs and Q7055.

FROM ADAPTER

PPDCIN_G3H

CRITICAL Q7080 HAT1128R01 SOI

CRITICAL Q7085 HAT1128R01 SOI

PPDCIN_G3H_OR_PBUS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=18.5V

PPDCIN_G3H_INRUSH
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=18.5V

R7080 100K 5% 1/16W MF-LF 402

C7085 0.1UF 10% 25V X5R 402

R7085 470K 1% 1/16W MF-LF 402

CHGR_SGATE_DIV
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.3 mm

CHGR_AGATE_DIV
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.3 mm

R7081 62K 5% 1/16W MF-LF 402

R7086 332K 1% 1/16W MF-LF 402

CRITICAL D7005 BAT30CWFILM SOT-323

CHGR_DCIN_D_R

R7005 20 5% 1/16W MF-LF 402

(CHGR_DCIN)

(CHGR_SGATE)

(CHGR_AGATE)

ACIN pin threshold is 3.2V, +/- 50mV

Divider sets ACIN threshold at 13.55V

Input impedance of ~40K meets sparkitecture requirements

30mA max load

PP3V42_G3H

PP5V1_CHGR_VDD
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=5.1V

R7001 4.7 5% 1/16W MF-LF 402

PP5V1_CHGR_VDDP
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5.1V

C7001 1UF 10% 10V X5R 402

BATT_3S

R7012 1K 1% 1/16W MF-LF 402

C7002 1UF 10% 10V X5R 402

NO STUFF R7002 100K 5% 1/16W MF-LF 402

GND_CHGR_AGND

R7000 0 5% 1/16W MF-LF 402

R7010 30.1K 1% 1/16W MF-LF 402

SMC_RESET_L

SMBUS_SMC_BSA_SCL

SMBUS_SMC_BSA_SDA

CHGR_VFRQ

CHGR_CELL

Float CELL for 1S

CHGR_ACIN

R7011 9.31K 1% 1/16W MF-LF 402

CHGR_ICOMP

CHGR_VCOMP

CHGR_VNEG

CHGR_CSO_P

CHGR_CSO_N

R7015 220K 5% 1/16W MF-LF 402

C7050 1UF 10% 16V X5R 402

BATT_2S

R7013 1K 1% 1/16W MF-LF 402

CHGR_VCOMP_R

C7015 470PF 10% 50V C0G 402

R7016 3.01K 1% 1/16W MF-LF 402

CHGR_VNEG_R

C7016 470PF 10% 50V C0G 402

C7042 0.033UF 10% 16V X5R 402

C7011 0.01UF 10% 16V C0G 402

C7000 1UF 10% 10V X5R 402-1

C7005 0.22UF 20% 25V X5R 603

C7026 0.001UF 10% 50V C0G 402

GND_CHGR_AGND
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0V

U7000 ISL6259HRTZ TQFN

VHST	12	DCIN	2 CHGR_DCIN
SMB_RST_N	13	SGATE	26 CHGR_SGATE
SCL	11	AGATE	1 CHGR_AGATE
SDA	10	CSIP	28 CHGR_CSI_P
VFRQ	4	CSIN	27 CHGR_CSI_N
CELL	6	BOOT	25 CHGR_BOOT
ACIN	3	UGATE	24 CHGR_UGATE
ICOMP	5	PHASE	23 CHGR_PHASE
VCOMP	7	LGATE	21 CHGR_LGATE
VNEG	8	BGATE	16 CHGR_BGATE
CSOP	18	20V/V AMON	9 CHGR_AMON
CSON	17	36V/V BMON	15 CHGR_BMON
		(OD) ACOK	14 SMC_BC_ACOK
(AGND) THRM_PAD	29	PGND	22 353S2392

XW7000 SM

(GND)

PLACE_NEAR=U7000.29:1mm
PLACE_NEAR=U7000.22:1mm

(CHGR_CSO_P)

(CHGR_CSO_N)

(PPVBAT_G3H_CHGR_R)

R7051 2.2 5% 1/16W MF-LF 402

R7052 0 5% 1/16W MF-LF 402

CHGR_CSO_R_P

CHGR_CSO_R_N

(PPVBAT_G3H_CHGR_R)

(CHGR_BGATE)

C7020 0.047UF 10% 10V CERM 402

R7021 10 5% 1/16W MF-LF 402

R7022 10 5% 1/16W MF-LF 402

C7022 0.1UF 10% 25V X5R 402

C7021 0.1UF 10% 25V X5R 402

CHGR_CSI_R_P

CHGR_CSI_R_N

CRITICAL R7020 0.020 1% 1W MF-LF 0612

PPDCIN_G3H_CHGR
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=18.5V

CRITICAL C7030 22UF 20% 25V POLY-TANT CASE-D2-SM

CRITICAL C7031 22UF 20% 25V POLY-TANT CASE-D2-SM

C7035 1UF 10% 25V X5R 603-1

C7036 1UF 10% 25V X5R 603-1

C7037 0.001UF 10% 50V X7R 402

C7025 0.22UF 10% 10V CERM 402
PLACE_NEAR=U7000.25:2mm

CRITICAL Q7030 RJK0332DPB-01 LFPAK-SM

Max Current = 8A
(L7030 limit)
f = 400 kHz

CRITICAL L7030 4.7UH-10.2A FDA1254F-SM

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
SWITCH_NODE=TRUE
DIDT=TRUE

NO STUFF R7039 180 5% 1/10W MF-LF 603

CRITICAL F7040 8AMP-24V 1206

TO SYSTEM

PPBUS_G3H

CRITICAL Q7035 RJK0305DPB LFPAK-HF

CHGR_PHASE_RC
DIDT=TRUE

NO STUFF C7039 470PF 10% 50V C0G 402

PPVBAT_G3H_CHGR_REG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=12.6V

CRITICAL C7040 22UF 20% 25V POLY-TANT CASE-D2-SM

C7045 0.001UF 10% 50V X7R 402

BATT_2S

R7050 0.005 1% 1W MF 0612

CRITICAL Q7055 SI7137DP SO-8

TO/FROM BATTERY

PPVBAT_G3H_CHGR_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=12.6V

C7055 1UF 10% 25V X5R 603-1

C7056 0.1UF 10% 16V X5R 402

C7057 0.01UF 10% 16V C0G 402

PPVBAT_G3H_CONN
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=12.6V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
107S0139	1	RES,0.010,0.5%,1W,0612-1	R7050	CRITICAL	BATT_3S

SYNC_MASTER=K18_POWER SYNC_DATE=06/30/2009

PAGE TITLE
PBus Supply & Battery Charger

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PPBUS_G3H
C7243 0.001UF 10% 50V CERM 402
CRITICAL C7240 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7241 1UF 10% 25V X5R 603-1
R7224 0 5% 1/16W MF-LF 402
P5VS3_VBST_R
C7224 0.1UF 10% 50V X7R 603-1
CRITICAL Q7220 SIS424DN PWRPK-1212-8-SM
C7200 1UF 10% 25V X5R 603-1
SMC_PM_G2_EN
R7273 100K 5% 1/16W MF-LF 402
PP5V_S5
P5VP3V3_VREF
P5VP3V3_VREG3
C7203 1UF 10% 16V X5R 603-1
C7205 10UF 10% 16V X5R 603
C7201 0.22UF 10% 10V CERM 402
R7264 0 5% 1/10W MF-LF 402
P3V3S5_VBST_R
C7264 0.1UF 10% 25V X7R 603-1
CRITICAL C7280 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7282 0.001UF 10% 50V CERM 402
C7281 1UF 10% 25V X5R 603-1
f=365KHz
PP5V_S3
Vout = 5.0V
9.1A MAX OUTPUT
(Q7220 limit)
CRITICAL L7220 4.7UH-13A-15MOHM PCMB104E4R7-SM
NO STUFF R7222 10 5% 1/10W MF-LF 402
Q7225 SIS426DN PWRPK-12128
CRITICAL
P5VS3_RC
NO STUFF C7222 100PF 10% 50V CERM 402
C7252 330UF 20% 6.3V POLY-TANT CASE-D3L-SM1
C7250 10UF 20% 16V X5R 805
C7251 0.001UF 10% 50V CERM 402
XW7220 SM
XW7221 SM
PLACE_NEAR=L7220.1:1mm
PLACE_NEAR=C7252.1:1mm
P5V_S3_REG_XW
P5V_S3_V01_XW
R7220 15.0K 1% 1/16W MF-LF 402
R7221 10K 1% 1/16W MF-LF 402
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
P5VS3_VBST
P5VS3_DRVH
GATE_NODE=TRUE DIDT=TRUE
P5VS3_LL
SWITCH_NODE=TRUE DIDT=TRUE
P5VS3_DRVL
GATE_NODE=TRUE DIDT=TRUE
(P5VS5_V01)
P5VS3_VFB
P5VS3_ENTRIP
U7201 QFN TPS51125
VIN VREF SKIPSEL TONSEL VBST1 DRVH1 LL1 DRVL1 VO1 VFB1 ENTRIP1 VREG3 VREG5 VBST2 DRVH2 LL2 DRVL2 VO2 VFB2 ENTRIP2 VCLK PGOOD EN0 GND THRM_PAD
NC
5V3V3_REG_EN
R7200 88.7K 1% 1/16W MF-LF 402
NO STUFF C7208 220PF 5% 25V CERM 402
R7206 88.7K 1% 1/16W MF-LF 402
XW7200 SM
PLACE_NEAR=U7201.25:1mm
GND_P5VP3V3_SGND
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0V
One master PGOOD for both 5V and 3V3
P5V3V3_PGOOD
P3V3S5_VBST
P3V3S5_DRVH
P3V3S5_LL
P3V3S5_DRVL
(P3V3S5_V02)
P3V3S5_VFB
P3V3S5_ENTRIP
CRITICAL Q7260 RJK0384DPA WPAK
NO STUFF R7262 10 5% 1/10W MF-LF 402
P3V3S5_RC
NO STUFF C7262 100PF 10% 50V CERM 402
152S1115
CRITICAL L7260 2.2UH-10A-14MOHM FDVE0830-SM
f=460KHz
PP3V3_S5
Vout = 3.3V
7.2A MAX OUTPUT
(L7260 limit)
CRITICAL C7292 150UF-D2E-9V-025-OHM POLY-TANT CASE-B2-SM
C7290 10UF 20% 6.3V X5R 603
C7291 0.001UF 10% 50V CERM 402
XW7261 SM
XW7260 SM
PLACE_NEAR=C7292.1:1mm
PLACE_NEAR=L7260.1:1mm
P3V3_S5_V02_XW
P3V3_S5_REG_XW
R7260 6.49K 1% 1/16W MF-LF 402
R7261 10K 1% 1/16W MF-LF 402
Q7210 SSM6N15FEAPE SOT563
PP3V42_G3H
R7210 10K 5% 1/16W MF-LF 402
P5VS3_EN_L
Q7211 SSM6N15FEAPE SOT563
R7211 10K 5% 1/16W MF-LF 402
P3V3S5_EN_L
P5VS3_EN
P3V3S5_EN

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PAGE TITLE: 5V / 3.3V Power Supply	
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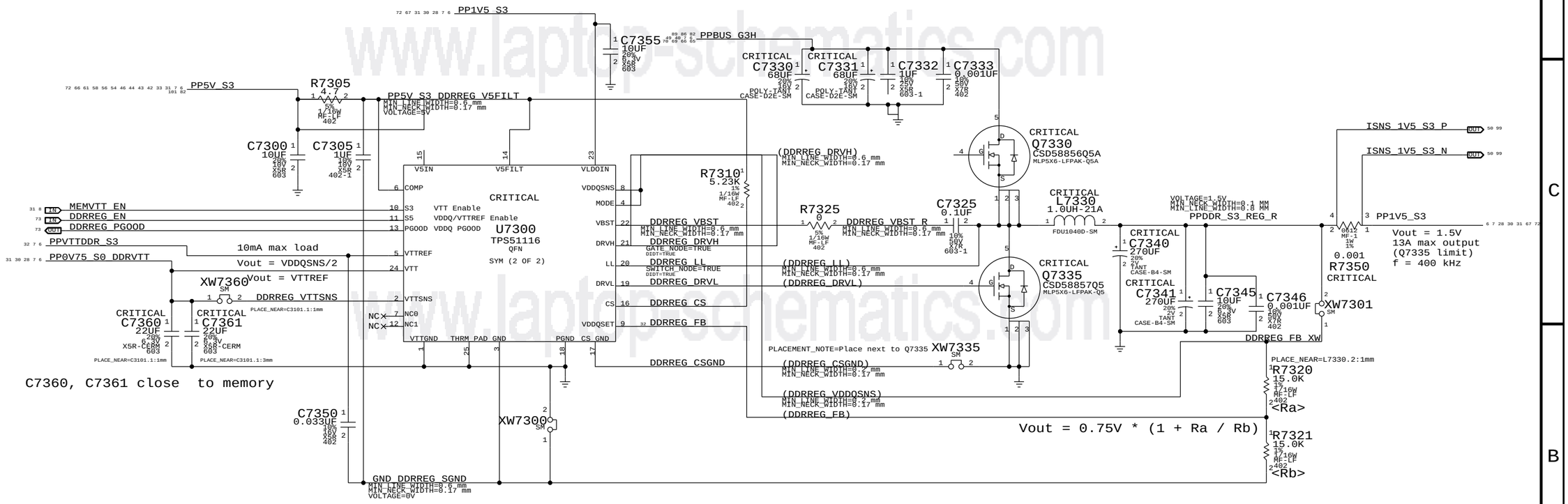

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PAGE TITLE: 1.5V DDR3 Supply

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PPBUS_CPU_IMVP_ISNS

PP3V3_S0

PP5V_S0

PP5V_S0_CPUIMVP_V5FILT
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V

C7401 2.2UF 20% 10V X5R-CERM 402

C7400 4.7UF 20% 35V X5R 805

C7403 33PF 5% 50V CERM 402

R7403 3.92K 1% 1/16W MF-LF 402

C7402 0.22UF 10% 10V CERM 402

CPUIMVP_DROOP
CPU_VCCSENSE_P
CPU_VCCSENSE_N
CPUIMVP_VREF
CPUIMVP_VID<0>
CPUIMVP_VID<1>
CPUIMVP_VID<2>
CPUIMVP_VID<3>
CPUIMVP_VID<4>
CPUIMVP_VID<5>
CPUIMVP_VID<6>
CPUIMVP_SLEW

R7400 249K 1% 1/16W MF-LF 402

CPUIMVP_ISEN1P
CPUIMVP_ISEN1N
CPUIMVP_ISEN2P
CPUIMVP_ISEN2N

OMIT C7440 NOSTUFF NONE 402
OMIT C7441 NOSTUFF NONE 402
OMIT C7442 NOSTUFF NONE 402
OMIT C7443 NOSTUFF NONE 402

U7400 TPS51621 QFN 353S2942

36	TONSEL	VBST1	22
39	DROOP	DRVH1	21
	VSNS	LL1	23
	GNDSNS	DRVL1	24
40	VREF	VBST2	29
20	VID0	DRVH2	30
19	VID1	LL2	28
18	VID2	DRVL2	27
17	VID3	PGOOD	33
16	VID4	CLK_EN*	34
15	VID5	VR_ON	35
14	VID6	DPRSLPVR	12
37	SLEW	PSI*	13
		MODE	1
6	CSP1	THERM	9
5	CSN1	VR_TT*	10
3	CSP2	IMON	11
4	CSN2	TRIPSEL	31
		OSRSEL	32
	GND	PGND	THRM PAD
	2	25	41

V5FILT V5IN

CPUIMVP_BOOT1
CPUIMVP_UGATE1
CPUIMVP_PHASE1
CPUIMVP_LGATE1
CPUIMVP_BOOT2
CPUIMVP_UGATE2
CPUIMVP_PHASE2
CPUIMVP_LGATE2
CPUIMVP_PGOOD
CPUIMVP_CLK_EN_L
CPUIMVP_VR_ON
PM_DPRSLPVR
CPU_PSI_L
CPUIMVP_NTC
CPUIMVP_VR_TT_L
CPUIMVP_IMON

R7414 0 5% 1/16W — CPUIMVP_BOOT1_RC — C7414 1UF 10% 25V X5R 603-2
R7424 0 5% 1/16W — CPUIMVP_BOOT2_RC — C7424 1UF 10% 25V X5R 603-2

MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM GATE_NODE=TRUE DIDT=TRUE
MIN_LINE_WIDTH=1.5 MM MIN_NECK_WIDTH=0.2 MM SWITCH_NODE=TRUE DIDT=TRUE

R7440 0 5% 1/16W — CPU_PROCHOT_L

R7450 16.9K 1% 1/16W MF-LF 402
C7450 0.0033UF 10% 50V CERM 402

IMON output range: 1.1V

CPU_VCCSENSE_N

R7445 100K 5% 1/16W MF-LF 402

XW7400 SM

CPUIMVP_AGND
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.15 mm
VOLTAGE=0V

Loadline = DCR * K * 5.95 / (R7403 * 2uA/mV)
Loadline = 1.83 mohm

VIMON = Io * DCR * 2uA/mV * R7450
50 A = 1.00 V

K = (R7417 || (R7418 + R7419)) / (R7417 || (R7418 + R7419) + R7416) = 0.66

PLACE_NEAR=Q7410.1:8mm
PLACE_NEAR=Q7410.1:8mm
PLACE_NEAR=Q7410.1:8mm

CRITICAL C7405 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7410 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7413 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7415 68UF 20% 16V POLY-TANT CASE-D2E-SM

PLACE_NEAR=Q7410.1:8mm
PLACE_NEAR=Q7410.1:8mm

C7411 10UF 10% 25V X5R 805
C7412 0.001UF 10% 50V X7R 402

PLACE_NEAR=Q7420.1:8mm
PLACE_NEAR=Q7420.1:8mm

C7421 10UF 10% 25V X5R 805
C7422 0.001UF 10% 50V X7R 402

CRITICAL Q7410 RJK0365DPA-02 WPAK
CRITICAL Q7415 RJK0208DPA WPAK
CRITICAL Q7420 RJK0365DPA-02 WPAK
CRITICAL Q7425 RJK0208DPA WPAK

(CPUIMVP_PHASE1)
(CPUIMVP_PHASE2)

CRITICAL L7415 0.36UH-20%-40A-0.00075OHM PIMA104E-SM
CRITICAL L7425 0.36UH-20%-40A-0.00075OHM PIMA104E-SM

XW7416 SM — PLACE_NEAR=L7415.1:4mm
XW7417 SM — PLACE_NEAR=L7415.2:4mm
XW7426 SM — PLACE_NEAR=L7425.1:4mm
XW7427 SM — PLACE_NEAR=L7425.2:4mm

CPUIMVP_PHASE1X
CPUIMVP_ISEN1N_R
CPUIMVP_PHASE2X
CPUIMVP_ISEN2N_R
CPUIMVP_ISEN1P_R
CPUIMVP_ISEN2P_R
CPUIMVP_ISEN1P
CPUIMVP_ISEN1N
CPUIMVP_ISEN2P
CPUIMVP_ISEN2N

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.15 MM

R7416 22.1K 1% 1/16W MF-LF 402
R7426 22.1K 1% 1/16W MF-LF 402

R7417 294K 1% 1/16W MF-LF 402
R7427 294K 1% 1/16W MF-LF 402

R7418 0402 — 150KOHM-5%
R7428 0402 — 150KOHM-5%

R7419 41.2K 1% 1/16W MF-LF 402
R7429 41.2K 1% 1/16W MF-LF 402

CPUIMVP_ISEN1_NTC
CPUIMVP_ISEN2_NTC

C7420 27.0NF 10% 10V X5R 402
C7430 27.0NF 10% 10V X5R 402

R7421 0 5% 1/16W MF-LF 402
R7422 0 5% 1/16W MF-LF 402
R7430 0 5% 1/16W MF-LF 402
R7431 0 5% 1/16W MF-LF 402

48A max current
PPVCORE_S0_CPU

SYNC_MASTER	K18_POWER
SYNC_DATE	06/29/2009
PAGE TITLE	CPU IMVP VCore Regulator
DRAWING NUMBER	<SCH_NUM>
SIZE	D
REVISION	<E4LABEL>
BRANCH	<BRANCH>
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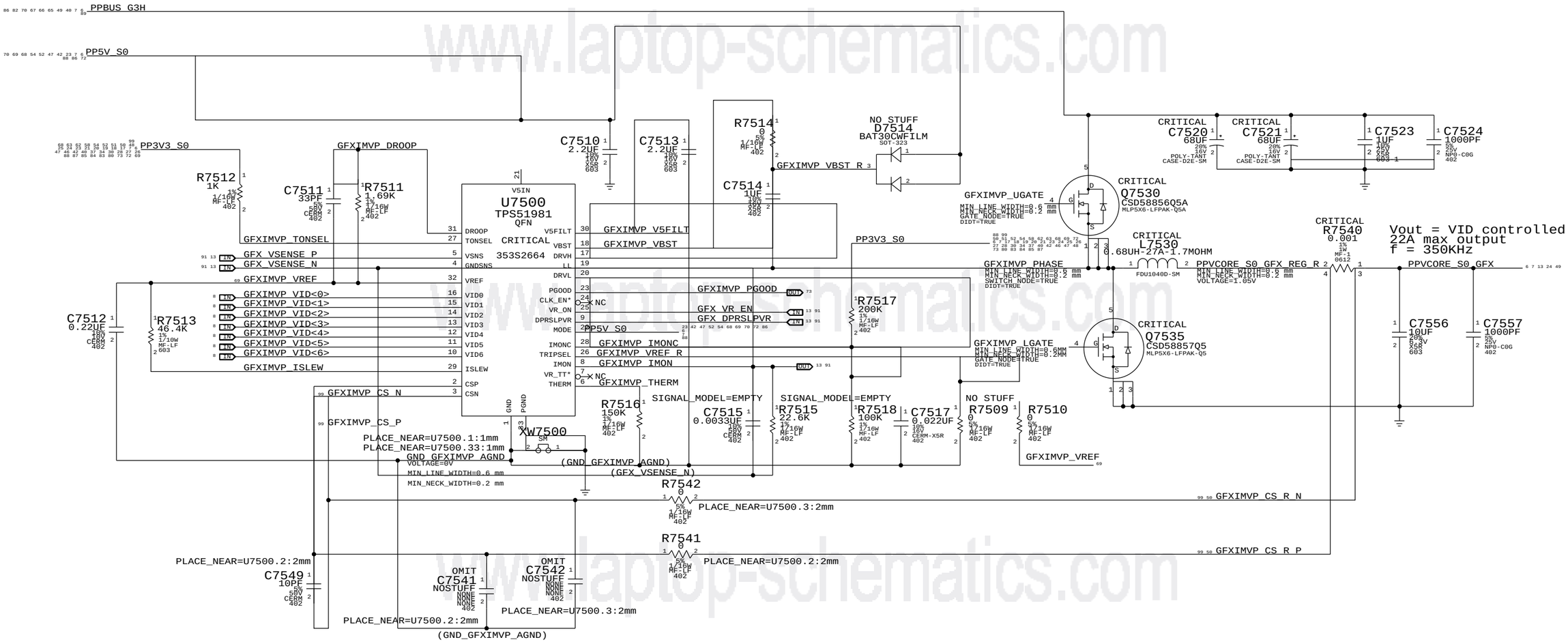
GFX IMVP VCORE



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SYNC_MASTER=K18_POWER SYNC_DATE=07/08/2009

PAGE TITLE: GFX IMVP VCore Regulator

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DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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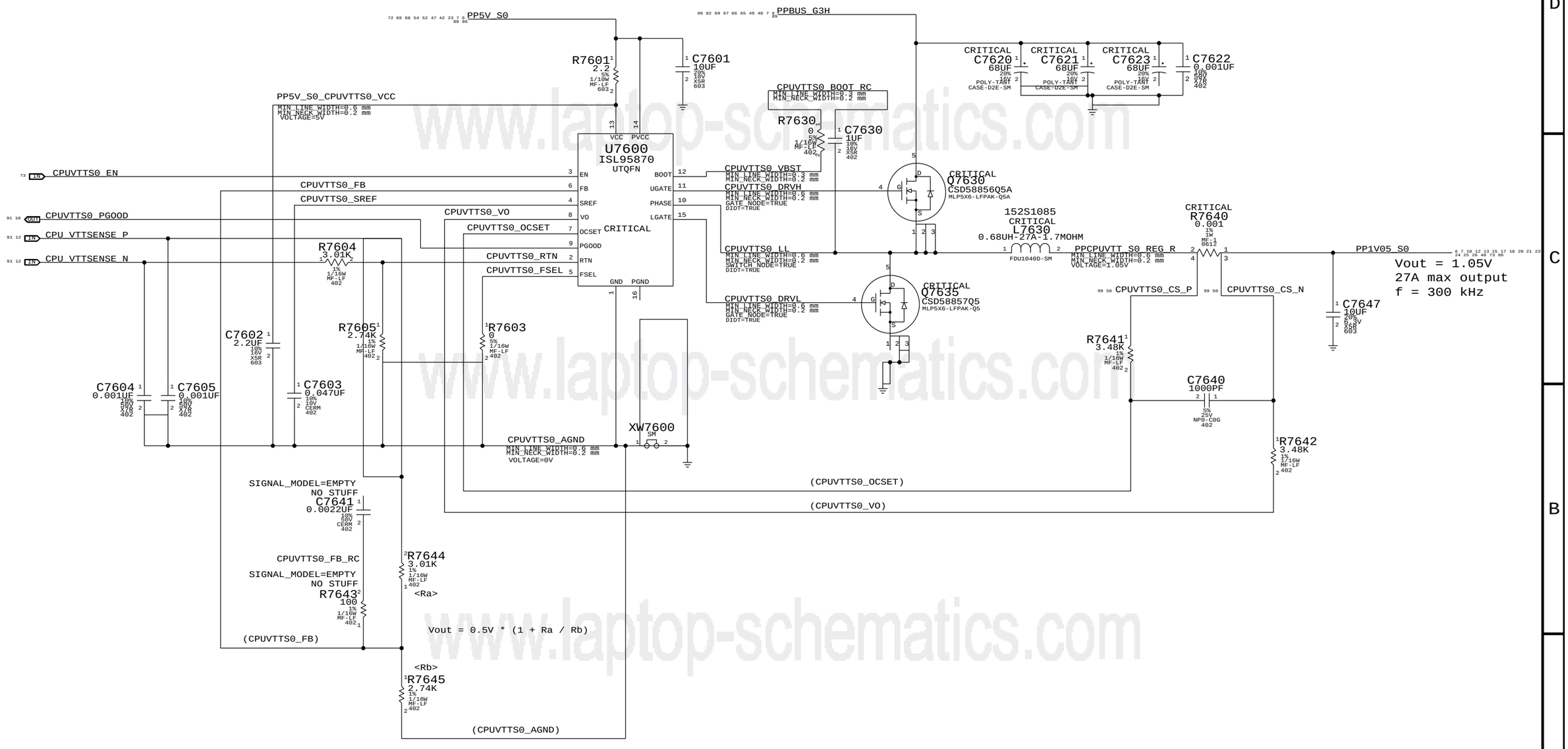
CPU VTT (1.05V S0) Regulator



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SYNC_MASTER=K18_POWER SYNC_DATE=07/14/2009

PAGE TITLE: CPUVTT (1.05V) Power Supply

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DRAWING NUMBER: <SCH_NUM> SIZE: D

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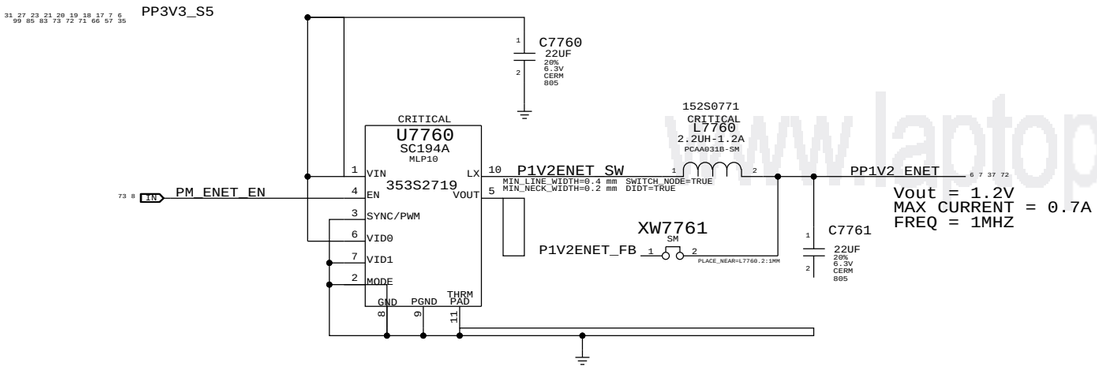
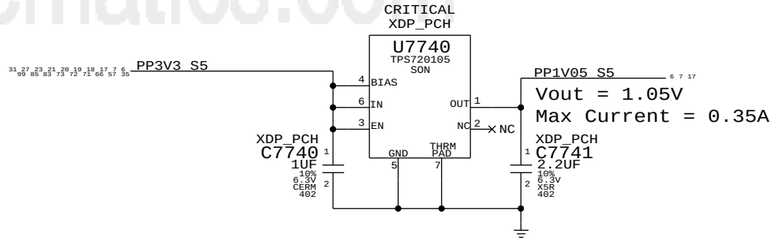
1.2V S3 Regulator



Vout = 1.2V
MAX CURRENT = 0.7A
FREQ = 1MHZ

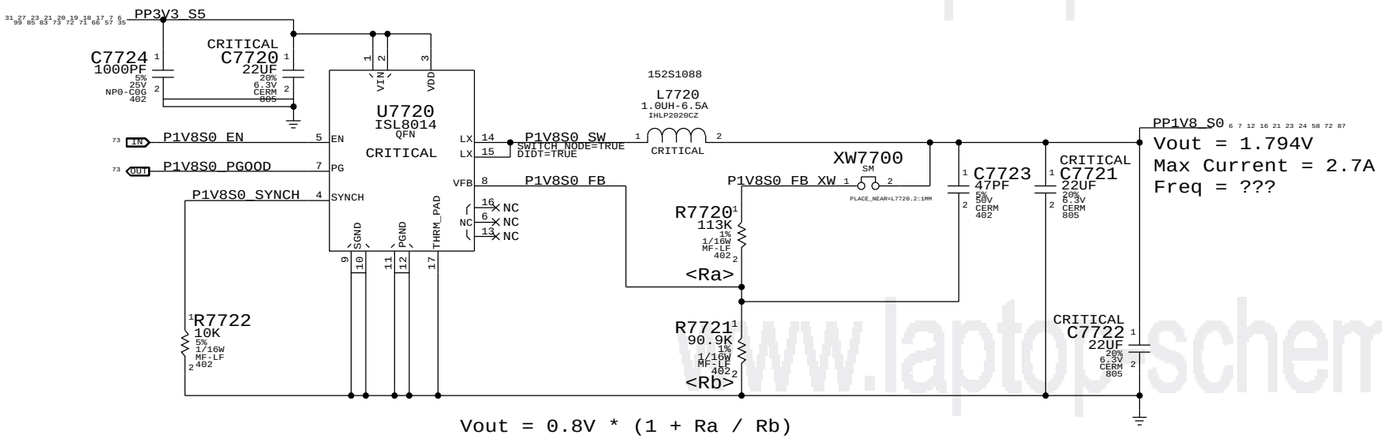
1.05V S5 LDO

Ibex Peak-M requires JTAG pull-ups to be powered at 1.05V in S5.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



Vout = 1.05V
Max Current = 2.35A

1.8V S0 Regulator



Vout = 1.794V
Max Current = 2.7A
Freq = ???

Vout = 0.8V * (1 + Ra / Rb)

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SYNC_MASTER=K18_POWER SYNC_DATE=06/29/2009

PAGE TITLE
Misc Power Supplies

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DRAWING NUMBER <SCH_NUM> SIZE D
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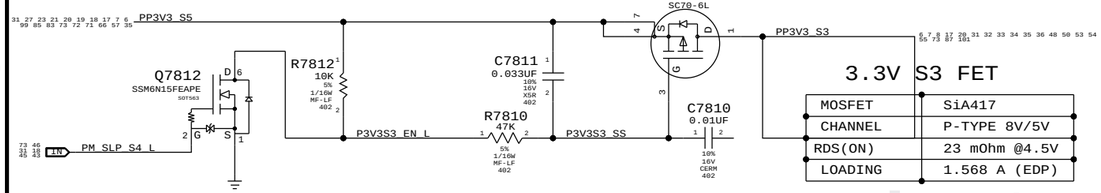
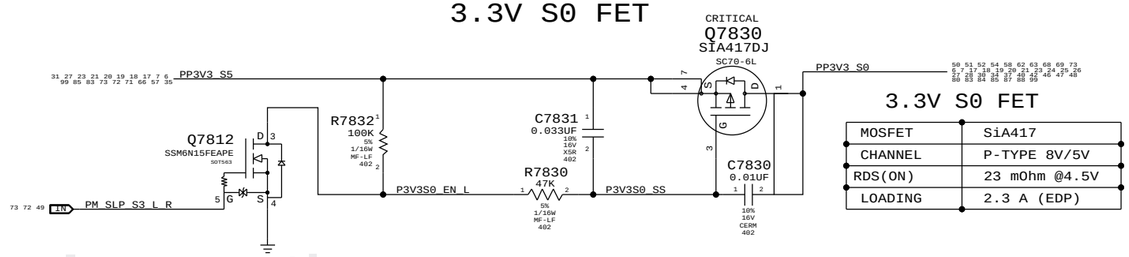
3.3V S3 FET



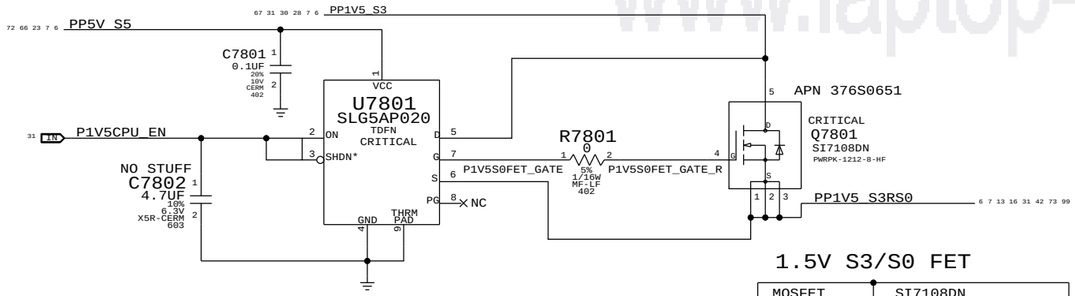
3.3V S3 FET	
MOSFET	SiA417
CHANNEL	P-TYPE 8V/5V
RDS(ON)	23 mOhm @4.5V
LOADING	1.568 A (EDP)

3.3V S0 FET



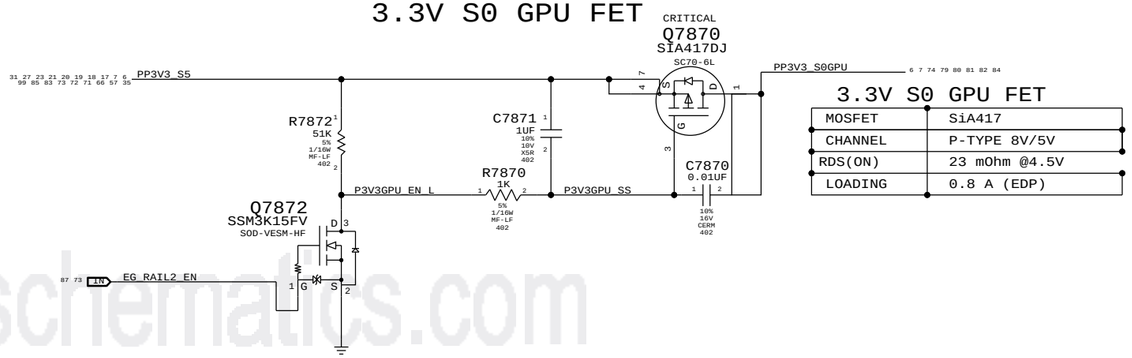
3.3V S0 FET	
MOSFET	SiA417
CHANNEL	P-TYPE 8V/5V
RDS(ON)	23 mOhm @4.5V
LOADING	2.3 A (EDP)

1.5V S3/S0 FET



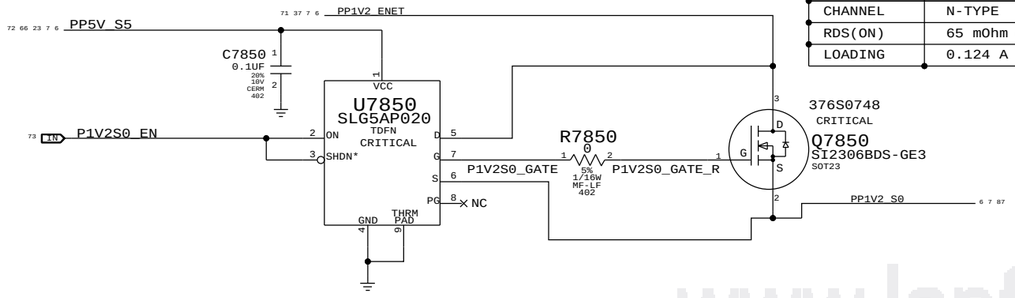
1.5V S3/S0 FET	
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	3.2 A (EDP)

3.3V S0 GPU FET



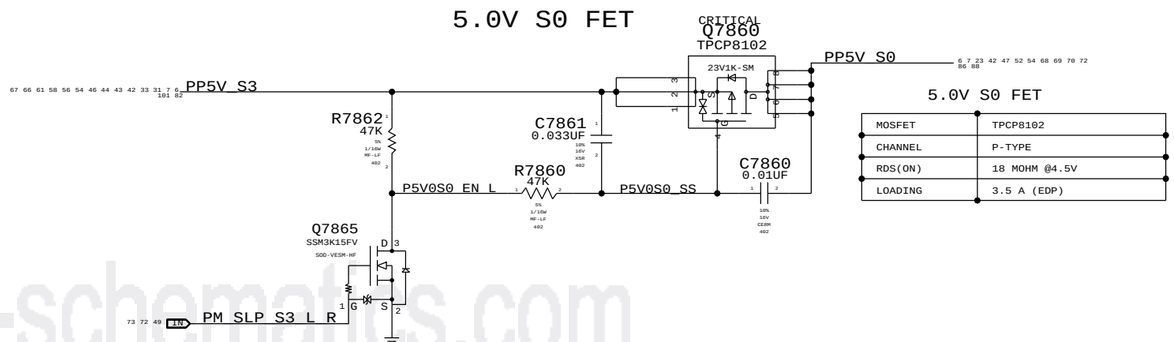
3.3V S0 GPU FET	
MOSFET	SiA417
CHANNEL	P-TYPE 8V/5V
RDS(ON)	23 mOhm @4.5V
LOADING	0.8 A (EDP)

1.2V S0 FET



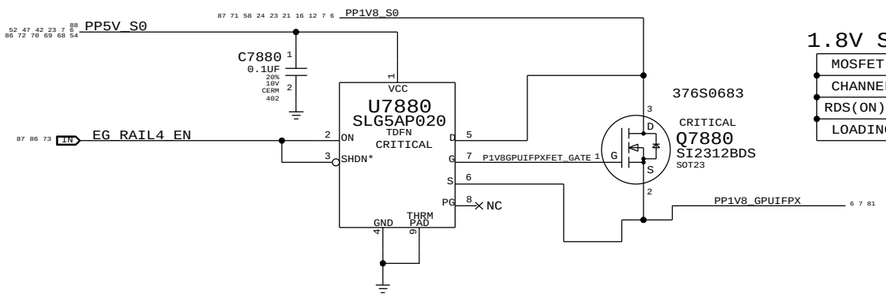
1.2V S0 FET	
MOSFET	SI2306BDS-GE3
CHANNEL	N-TYPE
RDS(ON)	65 mOhm @4.5V
LOADING	0.124 A (EDP)

5.0V S0 FET



5.0V S0 FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	18 MOHM @4.5V
LOADING	3.5 A (EDP)

1.8V S0 GPU_IFPX FET



1.8V S0 GPU_IFPX FET	
MOSFET	SI2312BDS
CHANNEL	N-TYPE
RDS(ON)	31 mOhm @4.5V
LOADING	0.3 A (EDP)

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SYNC_MASTER=K18_POWER SYNC_DATE=06/10/2009

PAGE TITLE: Power FETs

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DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

3.3V S5 ENABLE

SMC_PM_G2_EN → R7902 100 5% 1/16W MF-LF 402 → P3V3S5_EN (MAKE_BASE=TRUE) → P3V3S5_EN

R7958 100K 5% 1/16W MF-LF 402 (PLACE_NEAR=U4900.L13:3mm)

NO STUFF C7902 0.068UF 10% 10V CERM 402 (PLACE_NEAR=Q7211.2:2mm)

S5 rail PWRGD

PP3V42_G3H

PP3V3_S5

C7940 0.1UF 20% 10V CERM 402

R7940 100K 5% 1/16W MF-LF 402

CRITICAL U7940 TPS3808G33DBVRG4 SOT23-6 (VDD, SENSE, CT, GND, RESET*, MR* (IPU)) → RSMRST_PWRGD

S5_PGOOD_CT

C7941 0.001UF 10% 50V CERM 402

3.3V,5V S3 ENABLE

PM_SLP_S4_L (MAKE_BASE=TRUE) → (PM_S4_STATE_L) → PM_SLP_S4_L

R7911 5.1K 5% 1/16W MF-LF 402 (PLACE_NEAR=U7300.11:3mm)

R7912 0 5% 1/16W MF-LF 402 (PLACE_NEAR=Q7210.2:3mm)

P5VS3_EN (MAKE_BASE=TRUE) → P5VS3_EN

DDRREG_EN (MAKE_BASE=TRUE) → DDRREG_EN

NO STUFF C7910 0.47UF 10% 6.3V CERM-X5R 402 (PLACE_NEAR=U7300.11:3mm)

NO STUFF C7912 0.47UF 10% 6.3V CERM-X5R 402 (PLACE_NEAR=Q7210.2:3mm)

S0 ENABLE (PM_SLP_S3_L)

PM_SLP_S3_L → R7978 100 5% 1/16W MF-LF 402 → R7979 100K 5% 1/16W MF-LF 402 (PLACE_NEAR=U1800.P12:5mm)

PM_SLP_S4_L

VFRQ_SLPS4 R7933 0 5% 1/16W MF-LF 402

VFRQ_SLPS3 R7932 0 5% 1/16W MF-LF 402

PP3V42_G3H → R7931 10K 5% 1/16W MF-LF 402

Q7931 SSM3K15FV SOD-VESM-HF

CHGR VFRQ Generation

CHGR_VFRQ → NO STUFF R7935 0 5% 1/16W MF-LF 402

VFRQ_EN_GATE

(Need to confirm if SMC can provide 1 pin for control)

PM_SLP_S3_L_R (MAKE_BASE=TRUE)

R7981 33K 5% 1/16W MF-LF 402 (PLACE_NEAR=U7600.25:6mm)

R7985 20K 5% 1/16W MF-LF 402 (PLACE_NEAR=U7850.2:6mm)

R7986 5.1K 5% 1/16W MF-LF 402 (PLACE_NEAR=U7720.5:6mm)

PM_SLP_S3_L_R → PM_SLP_S3_L_R, PM_SLP_S3_L_R, PM_SLP_S3_L_R

P1V8S0_EN (MAKE_BASE=TRUE) → P1V8S0_EN

P1V2S0_EN (MAKE_BASE=TRUE) → P1V2S0_EN

CPUVTTS0_EN (MAKE_BASE=TRUE) → CPUVTTS0_EN

C7981 0.47UF 10% 6.3V CERM-X5R 402 (PLACE_NEAR=U7600.25:6mm)

C7985 1UF 10% 6.3V CERM 402 (PLACE_NEAR=U7850.2:6mm)

C7986 0.47UF 10% 6.3V CERM-X5R 402 (PLACE_NEAR=U7720.5:6mm)

Other S0 RAILS

PP3V3_S0

R7992 10K 5% 1/16W MF-LF 402

R7995 0 5% 1/16W MF-LF 402 ← S0PGOOD_PWROK

R7996 0 5% 1/16W MF-LF 402 ← P1V8S0_PGOOD

R7997 0 5% 1/16W MF-LF 402 ← P5V3V3_PGOOD

NO STUFF R7998 0 5% 1/16W MF-LF 402 ← DDRREG_PGOOD

R7988 0 5% 1/16W MF-LF 402 ← GFXIMVP_PGOOD

PM_ALL_GFX_PGOOD

TG: HIGH

EG: PM_ALL_GPU_PGOOD

PP3V3_S5

PLACE_NEAR=U7980.1:2mm

R7994 0 5% 1/16W MF-LF 402

C7989 0.1UF 20% 10V CERM 402

S0_PWR_PGOOD

NO STUFF R7991 0 5% 1/16W MF-LF 402 (PLACE_NEAR=U7980.1:2mm)

PM_ALL_GPU_PGOOD → ALL_GFX_PGOOD_R

U7980 TC7SZ08AFEAPE SOT665 → ALL_SYS_PWRGD

PP3V3_S0

R7999 10K 5% 1/16W MF-LF 402

27MHZ OE EN Generation

CK505_27MHZ_EN_L

Q7995 SSM3K15FV SOD-VESM-HF

EXT GPU PWRGD Pullup

PP3V3_S0 → R7990 100K 5% 1/16W MF-LF 402

PM_ALL_GPU_PGOOD (MAKE_BASE=TRUE)

ENET Enable Generation

"ENET" = "S0" || ("S3" && "AC" && "WOL_EN")

NOTE: S3 term is guaranteed by source of R7920 & Q7920, MUST BE S3 RAIL.

3.3V ENET FET

CRITICAL Q7922 NTR4101P SOT-23-HF

PP3V3_S3 → R7920 10K 5% 1/16W MF-LF 402 ← PM_ENET_EN

R7921 10K 5% 1/16W MF-LF 402

C7921 0.033UF 10% 16V X5R 402

R7922 100K 5% 1/16W MF-LF 402 ← P3V3ENET_SS

C7922 0.01UF 10% 16V CERM 402

PP3V3_ENET

C7920 0.22UF 10% 10V CERM 402

Q7921 2N7002DW-X-G SOT-363 → PM_ENET_EN_L

Q7921 2N7002DW-X-G SOT-363 ← PM_SLP_S3_L

Q7920 2N7002DW-X-G SOT-363 ← WOL_EN

PM_WLAN_EN_L

Q7925 2N7002DW-X-G SOT-363 ← AP_PWR_EN

AC_EN_L → (AC_EN_L)

Q7920 2N7002DW-X-G SOT-363 ← SMC_ADAPTER_EN

Q7925 2N7002DW-X-G SOT-363 ← (PM_SLP_S3_L)

WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT

PP3V3_S0

RAIL_MON U7971 ISL88042IRTJJZ TDFN (VDD, VDDA, V2MON, V3MON, V4MON, MR*, RST*, GND, THRM_PAD)

C7971 0.1uF 20% 10V CERM 402 (PLACE_NEAR=U7971.7:2mm)

PP3V3_S0 → V2MON

PP1V5_S3RS0 → V3MON

PP1V05_S0 → V4MON

NC

S0PGOOD_PWROK

V2MON THRESHOLD IS 3.0V
V3MON THRESHOLD IS 2.0V
V4MON THRESHOLD IS 0.6V

GPU Rail Sequencing

GT216 GPU requires rails to come up in the following order:
1) 1.05V 2) GPU 3V3 3) GPU Vcore 4) GDDR3 1V8

EG_RAIL1_EN → EG_RAIL1_EN (MAKE_BASE=TRUE)

EG_RAIL2_EN → EG_RAIL2_EN (MAKE_BASE=TRUE)

EG_RAIL3_EN → EG_RAIL3_EN (MAKE_BASE=TRUE)

EG_RAIL4_EN → EG_RAIL4_EN (MAKE_BASE=TRUE)

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: Power Control

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Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PP1V05_S0GPU
PP1V05_S0GPU
PP1V05_S0GPU

PEX 1.1V Current = 2A

250mA

C8002 1UF 10% 6.3V CERM 402
C8001 4.7UF 20% 6.3V CERM 603
C8000 22UF 20% 6.3V CERM-X5R 805

C8003 1UF 10% 6.3V CERM 402
C8004 0.1UF 20% 10V CERM 402
C8005 0.1UF 20% 10V CERM 402

1500mA

C8008 1UF 10% 6.3V CERM 402
C8007 4.7UF 20% 6.3V CERM 603
C8006 22UF 20% 6.3V CERM-X5R 805
C8018 10UF 20% 6.3V X5R 603

C8009 1UF 10% 6.3V CERM 402
C8010 0.1UF 20% 10V CERM 402
C8011 0.1UF 20% 10V CERM 402

NC_GPU_DFM
ND_TEST=TRUE

OMIT

U8000
NV-GT216
BGA
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H32	PEX_IOVDD1	AK16
M7	PEX_IOVDD2	AK17
P6	PEX_IOVDD3	AK21
A5	PEX_IOVDD4	AK24
U7	PEX_IOVDD5	AK27
V6		
AB7		
AD6	PEX_IOVDDQ1	AG11
AF6	PEX_IOVDDQ2	AG12
AG6	PEX_IOVDDQ3	AG13
AJ5	PEX_IOVDDQ4	AG15
AK15	PEX_IOVDDQ5	AG16
AL7	PEX_IOVDDQ6	AG17
E7	PEX_IOVDDQ7	AG18
A2	PEX_IOVDDQ8	AG22
A7	PEX_IOVDDQ9	AG23
B7	PEX_IOVDDQ10	AG24
C5	PEX_IOVDDQ11	AG25
C7	PEX_IOVDDQ12	AG26
D5	PEX_IOVDDQ13	AJ14
D6	PEX_IOVDDQ14	AJ15
D7	PEX_IOVDDQ15	AJ19
E5	PEX_IOVDDQ16	AJ21
E4	PEX_IOVDDQ17	AJ22
G5	PEX_IOVDDQ18	AJ24
J18	PEX_IOVDDQ19	AJ25
J19	PEX_IOVDDQ20	AJ27
J25	PEX_IOVDDQ21	AK18
J26	PEX_IOVDDQ22	AK20
AA4	PEX_IOVDDQ23	AK23
AB4	PEX_IOVDDQ24	AK26
AC5	PEX_IOVDDQ25	AL16
Y4		
AG20		
D35		
F7	VDD_SENSE	PEX_PLLVDD AG14
E35		
B7	GND_SENSE	VDD_SENSE AD20
A4	BUFRST*	GND_SENSE AD19

NC

GPU_VDD_SENSE 82
GPU_GND_SENSE 82

NC_GPU_BUFRST_L OUT 6

L8015 100NH-700MA-0.14OHM 0603
120 mA: GT216 A01 DG v3 01/09

PP1V1_GPU_PEX_PLLVDD_F
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.1V

C8017 1UF 10% 6.3V CERM 402
C8016 4.7UF 20% 6.3V CERM 603
C8015 4.7UF 20% 6.3V CERM 603

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PEG_R2D_C_P<0>	C8020 0.1uF	PEG_R2D_P<0>	AP17	PEX_RX0	PEX_TX0 AL17 PEG_D2R_C_P<0> C8055 0.1uF PEG_D2R_P<0>
PEG_R2D_C_N<0>	C8021 0.1uF	PEG_R2D_N<0>	AN17	PEX_RX0*	PEX_TX0* AM17 PEG_D2R_C_N<0> C8056 0.1uF PEG_D2R_N<0>
PEG_R2D_C_P<1>	C8022 0.1uF	PEG_R2D_P<1>	AN19	PEX_RX1	PEX_TX1 AM18 PEG_D2R_C_P<1> C8057 0.1uF PEG_D2R_P<1>
PEG_R2D_C_N<1>	C8023 0.1uF	PEG_R2D_N<1>	AP19	PEX_RX1*	PEX_TX1* AM19 PEG_D2R_C_N<1> C8058 0.1uF PEG_D2R_N<1>
PEG_R2D_C_P<2>	C8024 0.1uF	PEG_R2D_P<2>	AR19	PEX_RX2	PEX_TX2 AL19 PEG_D2R_C_P<2> C8059 0.1uF PEG_D2R_P<2>
PEG_R2D_C_N<2>	C8025 0.1uF	PEG_R2D_N<2>	AR20	PEX_RX2*	PEX_TX2* AK19 PEG_D2R_C_N<2> C8060 0.1uF PEG_D2R_N<2>
PEG_R2D_C_P<3>	C8026 0.1uF	PEG_R2D_P<3>	AP20	PEX_RX3	PEX_TX3 AL20 PEG_D2R_C_P<3> C8061 0.1uF PEG_D2R_P<3>
PEG_R2D_C_N<3>	C8027 0.1uF	PEG_R2D_N<3>	AN20	PEX_RX3*	PEX_TX3* AM20 PEG_D2R_C_N<3> C8062 0.1uF PEG_D2R_N<3>
PEG_R2D_C_P<4>	C8028 0.1uF	PEG_R2D_P<4>	AN22	PEX_RX4	PEX_TX4 AM21 PEG_D2R_C_P<4> C8063 0.1uF PEG_D2R_P<4>
PEG_R2D_C_N<4>	C8029 0.1uF	PEG_R2D_N<4>	AP22	PEX_RX4*	PEX_TX4* AM22 PEG_D2R_C_N<4> C8064 0.1uF PEG_D2R_N<4>
PEG_R2D_C_P<5>	C8030 0.1uF	PEG_R2D_P<5>	AR22	PEX_RX5	PEX_TX5 AL22 PEG_D2R_C_P<5> C8065 0.1uF PEG_D2R_P<5>
PEG_R2D_C_N<5>	C8031 0.1uF	PEG_R2D_N<5>	AR23	PEX_RX5*	PEX_TX5* AK22 PEG_D2R_C_N<5> C8066 0.1uF PEG_D2R_N<5>
PEG_R2D_C_P<6>	C8032 0.1uF	PEG_R2D_P<6>	AP23	PEX_RX6	PEX_TX6 AL23 PEG_D2R_C_P<6> C8067 0.1uF PEG_D2R_P<6>
PEG_R2D_C_N<6>	C8033 0.1uF	PEG_R2D_N<6>	AN23	PEX_RX6*	PEX_TX6* AM23 PEG_D2R_C_N<6> C8068 0.1uF PEG_D2R_N<6>
PEG_R2D_C_P<7>	C8034 0.1uF	PEG_R2D_P<7>	AN25	PEX_RX7	PEX_TX7 AM24 PEG_D2R_C_P<7> C8069 0.1uF PEG_D2R_P<7>
PEG_R2D_C_N<7>	C8035 0.1uF	PEG_R2D_N<7>	AP25	PEX_RX7*	PEX_TX7* AM25 PEG_D2R_C_N<7> C8070 0.1uF PEG_D2R_N<7>
PEG_R2D_C_P<8>	C8036 0.1uF	PEG_R2D_P<8>	AR25	PEX_RX8	PEX_TX8 AL25 PEG_D2R_C_P<8> C8071 0.1uF PEG_D2R_P<8>
PEG_R2D_C_N<8>	C8037 0.1uF	PEG_R2D_N<8>	AR26	PEX_RX8*	PEX_TX8* AK25 PEG_D2R_C_N<8> C8072 0.1uF PEG_D2R_N<8>
PEG_R2D_C_P<9>	C8038 0.1uF	PEG_R2D_P<9>	AP26	PEX_RX9	PEX_TX9 AL26 PEG_D2R_C_P<9> C8073 0.1uF PEG_D2R_P<9>
PEG_R2D_C_N<9>	C8039 0.1uF	PEG_R2D_N<9>	AN26	PEX_RX9*	PEX_TX9* AM26 PEG_D2R_C_N<9> C8074 0.1uF PEG_D2R_N<9>
PEG_R2D_C_P<10>	C8040 0.1uF	PEG_R2D_P<10>	AN28	PEX_RX10	PEX_TX10 AM27 PEG_D2R_C_P<10> C8075 0.1uF PEG_D2R_P<10>
PEG_R2D_C_N<10>	C8041 0.1uF	PEG_R2D_N<10>	AP28	PEX_RX10*	PEX_TX10* AM28 PEG_D2R_C_N<10> C8076 0.1uF PEG_D2R_N<10>
PEG_R2D_C_P<11>	C8042 0.1uF	PEG_R2D_P<11>	AR28	PEX_RX11	PEX_TX11 AL28 PEG_D2R_C_P<11> C8077 0.1uF PEG_D2R_P<11>
PEG_R2D_C_N<11>	C8043 0.1uF	PEG_R2D_N<11>	AR29	PEX_RX11*	PEX_TX11* AK28 PEG_D2R_C_N<11> C8078 0.1uF PEG_D2R_N<11>
PEG_R2D_C_P<12>	C8044 0.1uF	PEG_R2D_P<12>	AP29	PEX_RX12	PEX_TX12 AK29 PEG_D2R_C_P<12> C8079 0.1uF PEG_D2R_P<12>
PEG_R2D_C_N<12>	C8045 0.1uF	PEG_R2D_N<12>	AN29	PEX_RX12*	PEX_TX12* AL29 PEG_D2R_C_N<12> C8080 0.1uF PEG_D2R_N<12>
PEG_R2D_C_P<13>	C8046 0.1uF	PEG_R2D_P<13>	AN31	PEX_RX13	PEX_TX13 AM29 PEG_D2R_C_P<13> C8081 0.1uF PEG_D2R_P<13>
PEG_R2D_C_N<13>	C8047 0.1uF	PEG_R2D_N<13>	AP31	PEX_RX13*	PEX_TX13* AM30 PEG_D2R_C_N<13> C8082 0.1uF PEG_D2R_N<13>
PEG_R2D_C_P<14>	C8048 0.1uF	PEG_R2D_P<14>	AR31	PEX_RX14	PEX_TX14 AN31 PEG_D2R_C_P<14> C8083 0.1uF PEG_D2R_P<14>
PEG_R2D_C_N<14>	C8049 0.1uF	PEG_R2D_N<14>	AR32	PEX_RX14*	PEX_TX14* AM32 PEG_D2R_C_N<14> C8084 0.1uF PEG_D2R_N<14>
PEG_R2D_C_P<15>	C8050 0.1uF	PEG_R2D_P<15>	AR34	PEX_RX15	PEX_TX15 AN32 PEG_D2R_C_P<15> C8085 0.1uF PEG_D2R_P<15>
PEG_R2D_C_N<15>	C8051 0.1uF	PEG_R2D_N<15>	AP34	PEX_RX15*	PEX_TX15* AP32 PEG_D2R_C_N<15> C8086 0.1uF PEG_D2R_N<15>

PEG_CLK100M_P	AR16	PEX_REFCLK	PEX_TSTCLK_OUT AJ17 PEX_TSTCLK_P
PEG_CLK100M_N	AR17	PEX_REFCLK*	PEX_TSTCLK_OUT* AJ18 PEX_TSTCLK_N
EG_RESET_L R8020 0	AM16	GPU_RESET_R_L	PEX_TERMP AG21 PEX_TERMP_PD R8050 2.49K
PEX_CLKREQ_L	AR13	PEX_CLKREQ*	PEX_SVDD_3V3 AG19 F7

NO STUFF R8060 200

C8013 4.7UF 10% 6.3V X5R-CERM 603
C8012 0.1UF 10% 10V X5R 402

PP3V3_S0GPU

R8021 10K 5% 1/16W MF-LF 402

NO STUFF
PP1V05_S0GPU R8012 0 PP3V3R1V1_GPU_PEX_SVDD
R8013 0
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE
NV GT216 PCI-E

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PPVCORE_GPU

???A @ ???/???MHz Core/Mem Clk for VDD

C8100 1UF 10% 16V X5R 402
C8101 0.22UF 10% 6.3V CERM-X5R 402
C8102 0.22UF 10% 6.3V CERM-X5R 402
C8103 0.1UF 20% 16V X7R-CERM 402
C8104 0.047UF 10% 16V X7R 402
C8105 0.047UF 10% 16V X7R 402
C8106 0.047UF 10% 16V X7R 402
C8107 0.022UF 10% 16V CERM-X5R 402
C8108 0.022UF 10% 16V CERM-X5R 402
C8109 0.022UF 10% 16V CERM-X5R 402
C8110 0.015UF 10% 16V X7R 402
C8111 0.015UF 10% 16V X7R 402
C8112 0.01UF 10% 25V X7R 402
C8113 0.01UF 10% 25V X7R 402
C8114 0.01UF 10% 25V X7R 402
C8115 0.01UF 10% 25V X7R 402
C8116 0.01UF 10% 25V X7R 402
C8117 0.01UF 10% 25V X7R 402
C8118 0.0068UF 10% 25V CERM 402
C8119 0.0047UF 10% 25V CERM 402

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VDD

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GND

PP1V8R1V55_S0GPU_ISNS

Nvidia PRD for GB-128 uses 4x4.7uF, 8x0.47uF, 16x0.1uF

???A @ ???MHz 1.8V GDDR3

C8150 4.7UF 20% 6.3V CERM 603
C8156 4.7UF 20% 6.3V CERM 603
C8157 0.1UF 20% 10V CERM 402
C8158 0.1UF 20% 10V CERM 402
C8159 0.1UF 20% 10V CERM 402
C8160 0.047UF 10% 16V X7R 402
C8162 0.047UF 10% 16V X7R 402
C8163 0.047UF 10% 16V X7R 402
C8164 0.01UF 10% 25V X7R 402
C8165 0.01UF 10% 25V X7R 402
C8166 0.01UF 10% 25V X7R 402

OMIT

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FBVDDQ

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SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: NV GT216 CORE/FB POWER

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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Page Notes

Power aliases required by this page:
- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

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FB_A_DQ<0> L32 FBA_D00
FB_A_DQ<1> N33 FBA_D01
FB_A_DQ<2> L33 FBA_D02
FB_A_DQ<3> N34 FBA_D03
FB_A_DQ<4> N35 FBA_D04
FB_A_DQ<5> P35 FBA_D05
FB_A_DQ<6> P33 FBA_D06
FB_A_DQ<7> P34 FBA_D07
FB_A_DQ<8> K35 FBA_D08
FB_A_DQ<9> K33 FBA_D09
FB_A_DQ<10> K34 FBA_D10
FB_A_DQ<11> H33 FBA_D11
FB_A_DQ<12> G34 FBA_D12
FB_A_DQ<13> G33 FBA_D13
FB_A_DQ<14> E34 FBA_D14
FB_A_DQ<15> E33 FBA_D15
FB_A_DQ<16> G31 FBA_D16
FB_A_DQ<17> F30 FBA_D17
FB_A_DQ<18> G30 FBA_D18
FB_A_DQ<19> G32 FBA_D19
FB_A_DQ<20> K30 FBA_D20
FB_A_DQ<21> K32 FBA_D21
FB_A_DQ<22> H30 FBA_D22
FB_A_DQ<23> K31 FBA_D23
FB_A_DQ<24> L31 FBA_D24
FB_A_DQ<25> L30 FBA_D25
FB_A_DQ<26> M32 FBA_D26
FB_A_DQ<27> N30 FBA_D27
FB_A_DQ<28> M30 FBA_D28
FB_A_DQ<29> P31 FBA_D29
FB_A_DQ<30> R32 FBA_D30
FB_A_DQ<31> R30 FBA_D31
FB_A_DQ<32> AG30 FBA_D32
FB_A_DQ<33> AG32 FBA_D33
FB_A_DQ<34> AH31 FBA_D34
FB_A_DQ<35> AF31 FBA_D35
FB_A_DQ<36> AF30 FBA_D36
FB_A_DQ<37> AE30 FBA_D37
FB_A_DQ<38> AC32 FBA_D38
FB_A_DQ<39> AD30 FBA_D39
FB_A_DQ<40> AN33 FBA_D40
FB_A_DQ<41> AL31 FBA_D41
FB_A_DQ<42> AM33 FBA_D42
FB_A_DQ<43> AL33 FBA_D43
FB_A_DQ<44> AK30 FBA_D44
FB_A_DQ<45> AK32 FBA_D45
FB_A_DQ<46> AJ30 FBA_D46
FB_A_DQ<47> AH30 FBA_D47
FB_A_DQ<48> AH33 FBA_D48
FB_A_DQ<49> AH35 FBA_D49
FB_A_DQ<50> AH34 FBA_D50
FB_A_DQ<51> AH32 FBA_D51
FB_A_DQ<52> AJ33 FBA_D52
FB_A_DQ<53> AL35 FBA_D53
FB_A_DQ<54> AM34 FBA_D54
FB_A_DQ<55> AM35 FBA_D55
FB_A_DQ<56> AF33 FBA_D56
FB_A_DQ<57> AE32 FBA_D57
FB_A_DQ<58> AF34 FBA_D58
FB_A_DQ<59> AE35 FBA_D59
FB_A_DQ<60> AE34 FBA_D60
FB_A_DQ<61> AE33 FBA_D61
FB_A_DQ<62> AB32 FBA_D62
FB_A_DQ<63> AC35 FBA_D63

NCX H29
NCX R29
NCX L29
NCX M29
NCX AD29
NCX AE29
NCX AG29
NCX AH29
NC

FBA_CMD0 V32 FB_A_LMA<4>
FBA_CMD1 W31 FB_A_RAS_L
FBA_CMD2 U31 FB_A_LMA<5>
FBA_CMD3 Y32 FB_A_BA<1>
FBA_CMD4 AB35 FB_A_UMA<2>
FBA_CMD5 AB34 FB_A_UMA<4>
FBA_CMD6 W35 FB_A_UMA<3>
FBA_CMD7 W33 FB_A_UCKE
FBA_CMD8 W30 FB_A_UCS0_L
FBA_CMD9 T34 FB_A_MA<11>
FBA_CMD10 T35 FB_A_LCAS_L
FBA_CMD11 AB31 FB_A_WE_L
FBA_CMD12 Y30 FB_A_BA<0>
FBA_CMD13 Y34 FB_A_UMA<5>
FBA_CMD14 W32 FB_A_MA<12>
FBA_CMD15 AA30 FB_A_DRAM_RST
FBA_CMD16 AA32 FB_A_MA<7>
FBA_CMD17 Y33 FB_A_MA<10>
FBA_CMD18 U32 FB_A_LCKE
FBA_CMD19 Y31 FB_A_MA<0>
FBA_CMD20 U34 FB_A_MA<9>
FBA_CMD21 Y35 FB_A_MA<6>
FBA_CMD22 W34 FB_A_LMA<2>
FBA_CMD23 V30 FB_A_MA<8>
FBA_CMD24 U35 FB_A_LMA<3>
FBA_CMD25 U30 FB_A_MA<1>
FBA_CMD26 U33 NC_FBA_MA<13>
FBA_CMD27 AB30 FB_A_BA<2>
FBA_CMD28 AB33 NC_FB_A_UCS1_L
FBA_CMD29 T33 FB_A_LCS0_L
FBA_CMD30 W29 NC_FB_A_LCS1_L

FBA_CLK0 T32 FB_A_CLK_P<0>
FBA_CLK0* T31 FB_A_CLK_N<0>
FBA_CLK1 AC31 FB_A_CLK_P<1>
FBA_CLK1* AC30 FB_A_CLK_N<1>

FBA_DQM0 P32 FB_A_DQM_L<0>
FBA_DQM1 H34 FB_A_DQM_L<1>
FBA_DQM2 J30 FB_A_DQM_L<2>
FBA_DQM3 P30 FB_A_DQM_L<3>
FBA_DQM4 AF32 FB_A_DQM_L<4>
FBA_DQM5 AL32 FB_A_DQM_L<5>
FBA_DQM6 AL34 FB_A_DQM_L<6>
FBA_DQM7 AF35 FB_A_DQM_L<7>

FBA_DQS_RN0 L35 FB_A_RDQS<0>
FBA_DQS_RN1 G35 FB_A_RDQS<1>
FBA_DQS_RN2 H31 FB_A_RDQS<2>
FBA_DQS_RN3 N32 FB_A_RDQS<3>
FBA_DQS_RN4 AD32 FB_A_RDQS<4>
FBA_DQS_RN5 AJ31 FB_A_RDQS<5>
FBA_DQS_RN6 AJ35 FB_A_RDQS<6>
FBA_DQS_RN7 AC34 FB_A_RDQS<7>

FBA_DQS_WP0 L34 FB_A_WDQS<0>
FBA_DQS_WP1 H35 FB_A_WDQS<1>
FBA_DQS_WP2 J32 FB_A_WDQS<2>
FBA_DQS_WP3 N31 FB_A_WDQS<3>
FBA_DQS_WP4 AE31 FB_A_WDQS<4>
FBA_DQS_WP5 AJ32 FB_A_WDQS<5>
FBA_DQS_WP6 AJ34 FB_A_WDQS<6>
FBA_DQS_WP7 AC33 FB_A_WDQS<7>

FB_DLLAVDD AG27 PP1V1_GPU_FBPLLAVDD_F
FB_PLLAVDD AE27
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.1V

FBA_DEBUG T30 FB_A_UCAS_L

FB_CAL_PD_VDDQ K27 FBCAL_PD_VDDQ
FB_CAL_PU_GND L27 FBCAL_PU_GND
FB_CAL_TERM_GND M27 FBCAL_TERM_GND

R8203 1 10K 5% 1/16W MF-LF 402 2
R8200 1 10K 5% 1/16W MF-LF 402 2
R8201 1 10K 5% 1/16W MF-LF 402 2

R8292 1 40.2 1% 1/16W MF-LF 402 2
PLACE_NEAR=U8000.M27:3mm
R8291 1 31.6 1% 1/16W MF-LF 402 2
PLACE_NEAR=U8000.L27:3mm

PP1V05_S0GPU
CRITICAL
L8200
300-OHM-0.5A
0603-1
C8202 1 1UF 10% 6.3V CERM 402
C8200 1 4.7UF 10% 6.3V X5R-CERM 603
C8201 1 4.7UF 10% 6.3V X5R-CERM 603

PP1V8R1V55_S0GPU_ISNS
R8290 1 56.2 1% 1/16W MF-LF 402 2
PLACE_NEAR=U8000.K27:3mm

OMIT
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FB_B_DQ<0> B13 FBC_D00
FB_B_DQ<1> D13 FBC_D01
FB_B_DQ<2> A13 FBC_D02
FB_B_DQ<3> A14 FBC_D03
FB_B_DQ<4> C16 FBC_D04
FB_B_DQ<5> B16 FBC_D05
FB_B_DQ<6> A17 FBC_D06
FB_B_DQ<7> D16 FBC_D07
FB_B_DQ<8> C13 FBC_D08
FB_B_DQ<9> B11 FBC_D09
FB_B_DQ<10> C11 FBC_D10
FB_B_DQ<11> A11 FBC_D11
FB_B_DQ<12> C10 FBC_D12
FB_B_DQ<13> C8 FBC_D13
FB_B_DQ<14> B8 FBC_D14
FB_B_DQ<15> A8 FBC_D15
FB_B_DQ<16> F8 FBC_D16
FB_B_DQ<17> F8 FBC_D17
FB_B_DQ<18> F10 FBC_D18
FB_B_DQ<19> F9 FBC_D19
FB_B_DQ<20> F12 FBC_D20
FB_B_DQ<21> D8 FBC_D21
FB_B_DQ<22> D11 FBC_D22
FB_B_DQ<23> E11 FBC_D23
FB_B_DQ<24> D12 FBC_D24
FB_B_DQ<25> E13 FBC_D25
FB_B_DQ<26> F13 FBC_D26
FB_B_DQ<27> F14 FBC_D27
FB_B_DQ<28> F15 FBC_D28
FB_B_DQ<29> E16 FBC_D29
FB_B_DQ<30> F16 FBC_D30
FB_B_DQ<31> F17 FBC_D31
FB_B_DQ<32> D29 FBC_D32
FB_B_DQ<33> F27 FBC_D33
FB_B_DQ<34> F28 FBC_D34
FB_B_DQ<35> E28 FBC_D35
FB_B_DQ<36> D26 FBC_D36
FB_B_DQ<37> F25 FBC_D37
FB_B_DQ<38> D24 FBC_D38
FB_B_DQ<39> E25 FBC_D39
FB_B_DQ<40> E32 FBC_D40
FB_B_DQ<41> F32 FBC_D41
FB_B_DQ<42> D33 FBC_D42
FB_B_DQ<43> E31 FBC_D43
FB_B_DQ<44> C33 FBC_D44
FB_B_DQ<45> E29 FBC_D45
FB_B_DQ<46> D30 FBC_D46
FB_B_DQ<47> E29 FBC_D47
FB_B_DQ<48> B29 FBC_D48
FB_B_DQ<49> C31 FBC_D49
FB_B_DQ<50> C29 FBC_D50
FB_B_DQ<51> B31 FBC_D51
FB_B_DQ<52> C32 FBC_D52
FB_B_DQ<53> B32 FBC_D53
FB_B_DQ<54> B35 FBC_D54
FB_B_DQ<55> B34 FBC_D55
FB_B_DQ<56> A29 FBC_D56
FB_B_DQ<57> B28 FBC_D57
FB_B_DQ<58> A28 FBC_D58
FB_B_DQ<59> C28 FBC_D59
FB_B_DQ<60> C26 FBC_D60
FB_B_DQ<61> D25 FBC_D61
FB_B_DQ<62> B25 FBC_D62
FB_B_DQ<63> A25 FBC_D63

NCX C11
NCX C12
NCX C14
NCX C15
NCX C24
NCX C25
NCX C27
NCX C28
NC

FBC_CMD0 C17 FB_B_LMA<4>
FBC_CMD1 B19 FB_B_RAS_L
FBC_CMD2 D18 FB_B_LMA<5>
FBC_CMD3 F21 FB_B_BA<1>
FBC_CMD4 A23 FB_B_UMA<2>
FBC_CMD5 D21 FB_B_UMA<4>
FBC_CMD6 B23 FB_B_UMA<3>
FBC_CMD7 E20 FB_B_UCKE
FBC_CMD8 G21 FB_B_UCS0_L
FBC_CMD9 F20 FB_B_MA<11>
FBC_CMD10 F19 FB_B_LCAS_L
FBC_CMD11 F23 FB_B_WE_L
FBC_CMD12 A22 FB_B_BA<0>
FBC_CMD13 C22 FB_B_UMA<5>
FBC_CMD14 B17 FB_B_MA<12>
FBC_CMD15 F24 FB_B_DRAM_RST
FBC_CMD16 C25 FB_B_MA<7>
FBC_CMD17 E22 FB_B_MA<10>
FBC_CMD18 C20 FB_B_LCKE
FBC_CMD19 B22 FB_B_MA<0>
FBC_CMD20 A19 FB_B_MA<9>
FBC_CMD21 D22 FB_B_MA<6>
FBC_CMD22 D20 FB_B_LMA<2>
FBC_CMD23 E19 FB_B_MA<8>
FBC_CMD24 D19 FB_B_LMA<3>
FBC_CMD25 F18 FB_B_MA<1>
FBC_CMD26 C19 NC_FBB_MA<13>
FBC_CMD27 F22 FB_B_BA<2>
FBC_CMD28 C23 NC_FB_B_UCS1_L
FBC_CMD29 B20 FB_B_LCS0_L
FBC_CMD30 A20 NC_FB_B_LCS1_L

FBC_CLK0 E17 FB_B_CLK_P<0>
FBC_CLK0* D17 FB_B_CLK_N<0>
FBC_CLK1 D23 FB_B_CLK_P<1>
FBC_CLK1* E23 FB_B_CLK_N<1>

FBC_DQM0 A16 FB_B_DQM_L<0>
FBC_DQM1 D10 FB_B_DQM_L<1>
FBC_DQM2 E11 FB_B_DQM_L<2>
FBC_DQM3 D15 FB_B_DQM_L<3>
FBC_DQM4 D27 FB_B_DQM_L<4>
FBC_DQM5 D34 FB_B_DQM_L<5>
FBC_DQM6 A34 FB_B_DQM_L<6>
FBC_DQM7 D28 FB_B_DQM_L<7>

FBC_DQS_RN0 B14 FB_B_RDQS<0>
FBC_DQS_RN1 B10 FB_B_RDQS<1>
FBC_DQS_RN2 D9 FB_B_RDQS<2>
FBC_DQS_RN3 E14 FB_B_RDQS<3>
FBC_DQS_RN4 F26 FB_B_RDQS<4>
FBC_DQS_RN5 D31 FB_B_RDQS<5>
FBC_DQS_RN6 A31 FB_B_RDQS<6>
FBC_DQS_RN7 A26 FB_B_RDQS<7>

FBC_DQS_WP0 C14 FB_B_WDQS<0>
FBC_DQS_WP1 A10 FB_B_WDQS<1>
FBC_DQS_WP2 E10 FB_B_WDQS<2>
FBC_DQS_WP3 D14 FB_B_WDQS<3>
FBC_DQS_WP4 F26 FB_B_WDQS<4>
FBC_DQS_WP5 D32 FB_B_WDQS<5>
FBC_DQS_WP6 A32 FB_B_WDQS<6>
FBC_DQS_WP7 B26 FB_B_WDQS<7>

FBC_DEBUG G19 FB_B_UCAS_L
FB_VREF J27 GPU_FB_VREF

R8252 1 10K 5% 1/16W MF-LF 402 2
R8251 1 10K 5% 1/16W MF-LF 402 2
R8250 1 10K 5% 1/16W MF-LF 402 2

PP1V8R1V55_S0GPU_ISNS
R8295 1 1.07K 1% 1/16W MF-LF 402 2
R8296 1 2.49K 1% 1/16W MF-LF 402 2

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009
PAGE TITLE
NV GT216 FRAME BUFFER I/F
Apple Inc.
DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 82 OF 132
SHEET 76 OF 101

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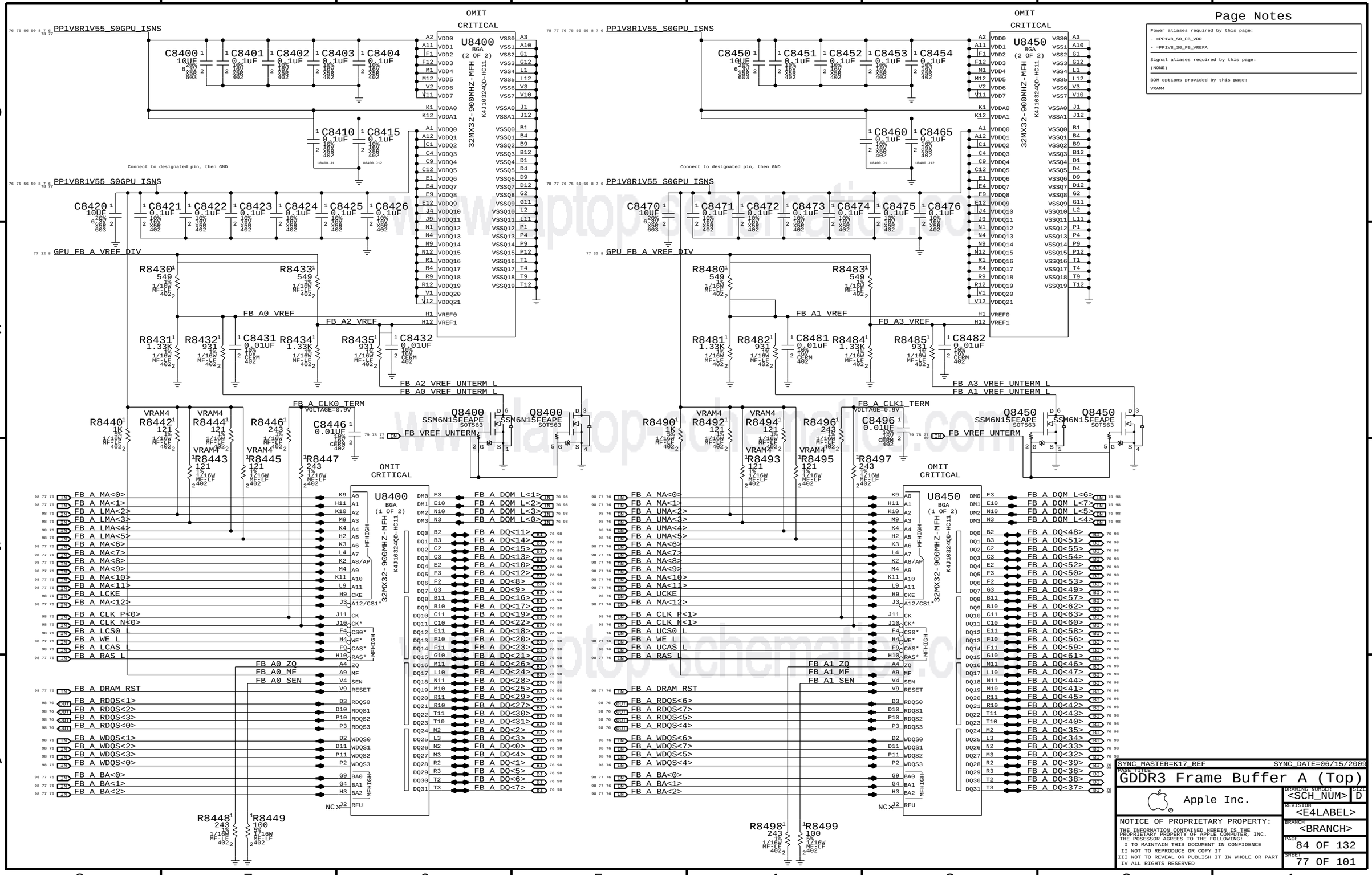
OMIT
CRITICAL
U8400
BGA
(2 OF 2)
32MX32-900MHZ-MFH
K4J10324QD-HC11
PP1V8R1VSS_S0GPU_ISNS
C8400 10UF 20% 6.3V X5R 603
C8401 0.1UF 10% 16V X5R 402
C8402 0.1UF 10% 16V X5R 402
C8403 0.1UF 10% 16V X5R 402
C8404 0.1UF 10% 16V X5R 402
C8410 0.1UF 10% 16V X5R 402
C8415 0.1UF 10% 16V X5R 402
Connect to designated pin, then GND
C8420 10UF 20% 6.3V X5R 603
C8421 0.1UF 10% 16V X5R 402
C8422 0.1UF 10% 16V X5R 402
C8423 0.1UF 10% 16V X5R 402
C8424 0.1UF 10% 16V X5R 402
C8425 0.1UF 10% 16V X5R 402
C8426 0.1UF 10% 16V X5R 402
GPU_FB_A_VREF_DIV
R8430 549 1% 1/16W MF-LF 402
R8433 549 1% 1/16W MF-LF 402
FB_A0_VREF
FB_A2_VREF
R8431 1.33K 1% 1/16W MF-LF 402
R8432 931 1% 1/16W MF-LF 402
C8431 0.01UF 10% 16V CERM 402
R8434 1.33K 1% 1/16W MF-LF 402
R8435 931 1% 1/16W MF-LF 402
C8432 0.01UF 10% 16V CERM 402
FB_A2_VREF_UNTERM_L
FB_A0_VREF_UNTERM_L
FB_A_CLK0_TERM
VOLTAGE=0.9V
C8446 0.01UF 10% 16V CERM 402
FB_VREF_UNTERM
Q8400 SSM6N15FEAPE SOT563
R8440 1K 1% 1/16W MF-LF 402
VRAM4
R8442 121 1% 1/16W MF-LF 402
R8444 121 1% 1/16W MF-LF 402
R8446 243 1% 1/16W MF-LF 402
R8443 121 1% 1/16W MF-LF 402
R8445 121 1% 1/16W MF-LF 402
R8447 243 1% 1/16W MF-LF 402
OMIT
CRITICAL
FB_A_MA<0>
FB_A_MA<1>
FB_A_LMA<2>
FB_A_LMA<3>
FB_A_LMA<4>
FB_A_LMA<5>
FB_A_MA<6>
FB_A_MA<7>
FB_A_MA<8>
FB_A_MA<9>
FB_A_MA<10>
FB_A_MA<11>
FB_A_LCKE
FB_A_MA<12>
FB_A_CLK_P<0>
FB_A_CLK_N<0>
FB_A_LCS0_L
FB_A_WE_L
FB_A_LCAS_L
FB_A_RAS_L
FB_A_DRAM_RST
FB_A_RDQS<1>
FB_A_RDQS<2>
FB_A_RDQS<3>
FB_A_RDQS<0>
FB_A_WDQS<1>
FB_A_WDQS<2>
FB_A_WDQS<3>
FB_A_WDQS<0>
FB_A_BA<0>
FB_A_BA<1>
FB_A_BA<2>
FB_A0_ZQ
FB_A0_MF
FB_A0_SEN
R8448 243 1% 1/16W MF-LF 402
R8449 100 5% 1/16W MF-LF 402
FB_A_DQM_L<1>
FB_A_DQM_L<2>
FB_A_DQM_L<3>
FB_A_DQM_L<0>
FB_A_DQ<11>
FB_A_DQ<14>
FB_A_DQ<15>
FB_A_DQ<13>
FB_A_DQ<10>
FB_A_DQ<12>
FB_A_DQ<8>
FB_A_DQ<9>
FB_A_DQ<16>
FB_A_DQ<17>
FB_A_DQ<19>
FB_A_DQ<22>
FB_A_DQ<18>
FB_A_DQ<20>
FB_A_DQ<23>
FB_A_DQ<21>
FB_A_DQ<26>
FB_A_DQ<24>
FB_A_DQ<28>
FB_A_DQ<25>
FB_A_DQ<29>
FB_A_DQ<27>
FB_A_DQ<30>
FB_A_DQ<31>
FB_A_DQ<2>
FB_A_DQ<3>
FB_A_DQ<0>
FB_A_DQ<4>
FB_A_DQ<1>
FB_A_DQ<5>
FB_A_DQ<6>
FB_A_DQ<7>
PP1V8R1VSS_S0GPU_ISNS
C8450 10UF 20% 6.3V X5R 603
C8451 0.1UF 10% 16V X5R 402
C8452 0.1UF 10% 16V X5R 402
C8453 0.1UF 10% 16V X5R 402
C8454 0.1UF 10% 16V X5R 402
C8460 0.1UF 10% 16V X5R 402
C8465 0.1UF 10% 16V X5R 402
Connect to designated pin, then GND
C8470 10UF 20% 6.3V X5R 603
C8471 0.1UF 10% 16V X5R 402
C8472 0.1UF 10% 16V X5R 402
C8473 0.1UF 10% 16V X5R 402
C8474 0.1UF 10% 16V X5R 402
C8475 0.1UF 10% 16V X5R 402
C8476 0.1UF 10% 16V X5R 402
GPU_FB_A_VREF_DIV
R8480 549 1% 1/16W MF-LF 402
R8483 549 1% 1/16W MF-LF 402
FB_A1_VREF
FB_A3_VREF
R8481 1.33K 1% 1/16W MF-LF 402
R8482 931 1% 1/16W MF-LF 402
C8481 0.01UF 10% 16V CERM 402
R8484 1.33K 1% 1/16W MF-LF 402
R8485 931 1% 1/16W MF-LF 402
C8482 0.01UF 10% 16V CERM 402
FB_A3_VREF_UNTERM_L
FB_A1_VREF_UNTERM_L
FB_A_CLK1_TERM
VOLTAGE=0.9V
C8496 0.01UF 10% 16V CERM 402
FB_VREF_UNTERM
Q8450 SSM6N15FEAPE SOT563
R8490 1K 1% 1/16W MF-LF 402
VRAM4
R8492 121 1% 1/16W MF-LF 402
R8494 121 1% 1/16W MF-LF 402
R8496 243 1% 1/16W MF-LF 402
R8493 121 1% 1/16W MF-LF 402
R8495 121 1% 1/16W MF-LF 402
R8497 243 1% 1/16W MF-LF 402
OMIT
CRITICAL
FB_A_MA<0>
FB_A_MA<1>
FB_A_UMA<2>
FB_A_UMA<3>
FB_A_UMA<4>
FB_A_UMA<5>
FB_A_MA<6>
FB_A_MA<7>
FB_A_MA<8>
FB_A_MA<9>
FB_A_MA<10>
FB_A_MA<11>
FB_A_UCKE
FB_A_MA<12>
FB_A_CLK_P<1>
FB_A_CLK_N<1>
FB_A_UCS0_L
FB_A_WE_L
FB_A_UCAS_L
FB_A_RAS_L
FB_A_DRAM_RST
FB_A_RDQS<6>
FB_A_RDQS<7>
FB_A_RDQS<5>
FB_A_RDQS<4>
FB_A_WDQS<6>
FB_A_WDQS<7>
FB_A_WDQS<5>
FB_A_WDQS<4>
FB_A_BA<0>
FB_A_BA<1>
FB_A_BA<2>
FB_A1_ZQ
FB_A1_MF
FB_A1_SEN
R8498 243 1% 1/16W MF-LF 402
R8499 100 5% 1/16W MF-LF 402
FB_A_DQM_L<6>
FB_A_DQM_L<7>
FB_A_DQM_L<5>
FB_A_DQM_L<4>
FB_A_DQ<48>
FB_A_DQ<51>
FB_A_DQ<55>
FB_A_DQ<54>
FB_A_DQ<52>
FB_A_DQ<50>
FB_A_DQ<53>
FB_A_DQ<49>
FB_A_DQ<57>
FB_A_DQ<62>
FB_A_DQ<63>
FB_A_DQ<60>
FB_A_DQ<58>
FB_A_DQ<56>
FB_A_DQ<59>
FB_A_DQ<61>
FB_A_DQ<46>
FB_A_DQ<47>
FB_A_DQ<44>
FB_A_DQ<41>
FB_A_DQ<45>
FB_A_DQ<42>
FB_A_DQ<43>
FB_A_DQ<40>
FB_A_DQ<35>
FB_A_DQ<34>
FB_A_DQ<33>
FB_A_DQ<32>
FB_A_DQ<39>
FB_A_DQ<36>
FB_A_DQ<38>
FB_A_DQ<37>
Page Notes
Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VREFA
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
VRAM4
SYNC_MASTER=K17_REF
SYNC_DATE=06/15/2009
PAGE TITLE
GDDR3 Frame Buffer A (Top)
Apple Inc.
DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 84 OF 132
SHEET 77 OF 101
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Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VREF_B

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
VRAM4

OMIT CRITICAL

PP1V8R1V55_S0GPU_ISNS

C8500 10UF 20% 6.3V X5R 603; C8501 0.1uF 10% 16V X5R 402; C8502 0.1uF 10% 16V X5R 402; C8503 0.1uF 10% 16V X5R 402; C8504 0.1uF 10% 16V X5R 402

C8510 0.1uF 10% 16V X5R 402 (U8500.J1); C8515 0.1uF 10% 16V X5R 402 (U8500.J12)

Connect to designated pin, then GND

PP1V8R1V55_S0GPU_ISNS

C8520 10UF 20% 6.3V X5R 603; C8521 0.1uF 10% 16V X5R 402; C8522 0.1uF 10% 16V X5R 402; C8523 0.1uF 10% 16V X5R 402; C8524 0.1uF 10% 16V X5R 402; C8525 0.1uF 10% 16V X5R 402; C8526 0.1uF 10% 16V X5R 402

GPU_FB_B_VREF_DIV

R8530 549 1% 1/16W MF-LF 402; R8533 549 1% 1/16W MF-LF 402

FB_B0_VREF; FB_B2_VREF

R8531 1.33K 1% 1/16W MF-LF 402; R8532 931 1% 1/16W MF-LF 402; C8531 0.01uF 10% 16V CERM 402; R8534 1.33K 1% 1/16W MF-LF 402; R8535 931 1% 1/16W MF-LF 402; C8532 0.01uF 10% 16V CERM 402

FB_B2_VREF_UNTERM_L
FB_B0_VREF_UNTERM_L

FB_B_CLK0_TERM
VOLTAGE=0.9V

C8546 0.01UF 10% 16V CERM 402

FB_VREF_UNTERM

Q8500 SSM6N15FEAPE SOT563; Q8500 SSM6N15FEAPE SOT563

R8540 1K 1% 1/16W MF-LF 402; R8542 121 1% 1/16W MF-LF 402; R8544 121 1% 1/16W MF-LF 402; R8546 243 1% 1/16W MF-LF 402

VRAM4 R8543 121 1% 1/16W MF-LF 402; VRAM4 R8545 121 1% 1/16W MF-LF 402; R8547 243 1% 1/16W MF-LF 402

OMIT CRITICAL

U8500 BGA (2 OF 2) 32MX32-900MHZ-MFH K4J10324QD-HC11

A2 VDD0	A11 VDD1	F1 VDD2	H12 VDD3
M1 VDD4	M12 VDD5	V2 VDD6	V11 VDD7
K1 VDDA0	K12 VDDA1		
A1 VDDQ0	A12 VDDQ1	C1 VDDQ2	C4 VDDQ3
C9 VDDQ4	C12 VDDQ5	E1 VDDQ6	E4 VDDQ7
E9 VDDQ8	E12 VDDQ9	J4 VDDQ10	J9 VDDQ11
N1 VDDQ12	N4 VDDQ13	N9 VDDQ14	N12 VDDQ15
R1 VDDQ16	R4 VDDQ17	R9 VDDQ18	R12 VDDQ19
V1 VDDQ20	V12 VDDQ21		
A3 VSS0	A10 VSS1	G1 VSS2	G12 VSS3
L1 VSS4	L12 VSS5	V3 VSS6	V10 VSS7
J1 VSSA0	J12 VSSA1		
B1 VSSQ0	B4 VSSQ1	B9 VSSQ2	B12 VSSQ3
D1 VSSQ4	D4 VSSQ5	D9 VSSQ6	D12 VSSQ7
G2 VSSQ8	G11 VSSQ9	L2 VSSQ10	L11 VSSQ11
P1 VSSQ12	P4 VSSQ13	P9 VSSQ14	P12 VSSQ15
T1 VSSQ16	T4 VSSQ17	T9 VSSQ18	T12 VSSQ19
H1 VREF0	H12 VREF1		

MFHIGH

K9 A0	H11 A1	K10 A2	M9 A3
K4 A4	H2 A5	K3 A6	L4 A7
K2 A8/AP	M4 A9	K11 A10	L9 A11
H9 CKE	J3 A12/CS1*		
J11 CK	J10 CK*		
F4 CS0*	H4 WE*	F9 CAS*	H10 RAS*
A4 ZQ	A9 MF	V4 SEN	V9 RESET
D3 RDQS0	D10 RDQS1	P10 RDQS2	P3 RDQS3
D2 WDQS0	D11 WDQS1	P11 WDQS2	P2 WDQS3
G9 BA0	G4 BA1	H3 BA2	J2 RFU

MFHIGH

E3 DM0	E10 DM1	N10 DM2	N3 DM3
B2 DQ0	B3 DQ1	C2 DQ2	C3 DQ3
E2 DQ4	F3 DQ5	F2 DQ6	G3 DQ7
B11 DQ8	B10 DQ9	C11 DQ10	C10 DQ11
E11 DQ12	F10 DQ13	F11 DQ14	G10 DQ15
M11 DQ16	L10 DQ17	N11 DQ18	M10 DQ19
R11 DQ20	R10 DQ21	T11 DQ22	T10 DQ23
M2 DQ24	L3 DQ25	N2 DQ26	M3 DQ27
R2 DQ28	R3 DQ29	T2 DQ30	T3 DQ31

FB_B_DQM_L<1>, FB_B_DQM_L<2>, FB_B_DQM_L<3>, FB_B_DQM_L<0>

FB_B_DQ<15>, FB_B_DQ<9>, FB_B_DQ<14>, FB_B_DQ<11>, FB_B_DQ<13>, FB_B_DQ<12>, FB_B_DQ<10>, FB_B_DQ<8>, FB_B_DQ<16>, FB_B_DQ<19>, FB_B_DQ<21>, FB_B_DQ<17>, FB_B_DQ<22>, FB_B_DQ<18>, FB_B_DQ<23>, FB_B_DQ<20>, FB_B_DQ<29>, FB_B_DQ<27>, FB_B_DQ<24>, FB_B_DQ<30>, FB_B_DQ<28>, FB_B_DQ<31>, FB_B_DQ<26>, FB_B_DQ<4>, FB_B_DQ<3>, FB_B_DQ<0>, FB_B_DQ<2>, FB_B_DQ<1>, FB_B_DQ<6>, FB_B_DQ<7>, FB_B_DQ<5>

FB_B_MA<0>, FB_B_MA<1>, FB_B_LMA<2>, FB_B_LMA<3>, FB_B_LMA<4>, FB_B_LMA<5>, FB_B_MA<6>, FB_B_MA<7>, FB_B_MA<8>, FB_B_MA<9>, FB_B_MA<10>, FB_B_MA<11>, FB_B_LCKE, FB_B_MA<12>

FB_B_CLK_P<0>, FB_B_CLK_N<0>, FB_B_LCS0_L, FB_B_WE_L, FB_B_LCAS_L, FB_B_RAS_L

FB_B0_ZQ, FB_B0_MF, FB_B0_SEN

FB_B_DRAM_RST

FB_B_RDQS<1>, FB_B_RDQS<2>, FB_B_RDQS<3>, FB_B_RDQS<0>

FB_B_WDQS<1>, FB_B_WDQS<2>, FB_B_WDQS<3>, FB_B_WDQS<0>

FB_B_BA<0>, FB_B_BA<1>, FB_B_BA<2>

R8548 243 1% 1/16W MF-LF 402; R8549 100 5% 1/16W MF-LF 402

PP1V8R1V55_S0GPU_ISNS

C8550 10UF 20% 6.3V X5R 603; C8551 0.1uF 10% 16V X5R 402; C8552 0.1uF 10% 16V X5R 402; C8553 0.1uF 10% 16V X5R 402; C8554 0.1uF 10% 16V X5R 402

C8560 0.1uF 10% 16V X5R 402 (U8500.J1); C8565 0.1uF 10% 16V X5R 402 (U8500.J12)

Connect to designated pin, then GND

PP1V8R1V55_S0GPU_ISNS

C8570 10UF 20% 6.3V X5R 603; C8571 0.1uF 10% 16V X5R 402; C8572 0.1uF 10% 16V X5R 402; C8573 0.1uF 10% 16V X5R 402; C8574 0.1uF 10% 16V X5R 402; C8575 0.1uF 10% 16V X5R 402; C8576 0.1uF 10% 16V X5R 402

GPU_FB_B_VREF_DIV

R8580 549 1% 1/16W MF-LF 402; R8583 549 1% 1/16W MF-LF 402

FB_B1_VREF; FB_B3_VREF

R8581 1.33K 1% 1/16W MF-LF 402; R8582 931 1% 1/16W MF-LF 402; C8581 0.01uF 10% 16V CERM 402; R8584 1.33K 1% 1/16W MF-LF 402; R8585 931 1% 1/16W MF-LF 402; C8582 0.01uF 10% 16V CERM 402

FB_B3_VREF_UNTERM_L
FB_B1_VREF_UNTERM_L

FB_B_CLK1_TERM
VOLTAGE=0.9V

C8596 0.01UF 10% 16V CERM 402

FB_VREF_UNTERM

Q8550 SSM6N15FEAPE SOT563; Q8550 SSM6N15FEAPE SOT563

R8590 1K 1% 1/16W MF-LF 402; R8592 121 1% 1/16W MF-LF 402; R8594 121 1% 1/16W MF-LF 402; R8596 243 1% 1/16W MF-LF 402

VRAM4 R8593 121 1% 1/16W MF-LF 402; VRAM4 R8595 121 1% 1/16W MF-LF 402; R8597 243 1% 1/16W MF-LF 402

OMIT CRITICAL

U8550 BGA (2 OF 2) 32MX32-900MHZ-MFH K4J10324QD-HC11

A2 VDD0	A11 VDD1	F1 VDD2	H12 VDD3
M1 VDD4	M12 VDD5	V2 VDD6	V11 VDD7
K1 VDDA0	K12 VDDA1		
A1 VDDQ0	A12 VDDQ1	C1 VDDQ2	C4 VDDQ3
C9 VDDQ4	C12 VDDQ5	E1 VDDQ6	E4 VDDQ7
E9 VDDQ8	E12 VDDQ9	J4 VDDQ10	J9 VDDQ11
N1 VDDQ12	N4 VDDQ13	N9 VDDQ14	N12 VDDQ15
R1 VDDQ16	R4 VDDQ17	R9 VDDQ18	R12 VDDQ19
V1 VDDQ20	V12 VDDQ21		
A3 VSS0	A10 VSS1	G1 VSS2	G12 VSS3
L1 VSS4	L12 VSS5	V3 VSS6	V10 VSS7
J1 VSSA0	J12 VSSA1		
B1 VSSQ0	B4 VSSQ1	B9 VSSQ2	B12 VSSQ3
D1 VSSQ4	D4 VSSQ5	D9 VSSQ6	D12 VSSQ7
G2 VSSQ8	G11 VSSQ9	L2 VSSQ10	L11 VSSQ11
P1 VSSQ12	P4 VSSQ13	P9 VSSQ14	P12 VSSQ15
T1 VSSQ16	T4 VSSQ17	T9 VSSQ18	T12 VSSQ19
H1 VREF0	H12 VREF1		

MFHIGH

K9 A0	H11 A1	K10 A2	M9 A3
K4 A4	H2 A5	K3 A6	L4 A7
K2 A8/AP	M4 A9	K11 A10	L9 A11
H9 CKE	J3 A12/CS1*		
J11 CK	J10 CK*		
F4 CS0*	H4 WE*	F9 CAS*	H10 RAS*
A4 ZQ	A9 MF	V4 SEN	V9 RESET
D3 RDQS0	D10 RDQS1	P10 RDQS2	P3 RDQS3
D2 WDQS0	D11 WDQS1	P11 WDQS2	P2 WDQS3
G9 BA0	G4 BA1	H3 BA2	J2 RFU

MFHIGH

E3 DM0	E10 DM1	N10 DM2	N3 DM3
B2 DQ0	B3 DQ1	C2 DQ2	C3 DQ3
E2 DQ4	F3 DQ5	F2 DQ6	G3 DQ7
B11 DQ8	B10 DQ9	C11 DQ10	C10 DQ11
E11 DQ12	F10 DQ13	F11 DQ14	G10 DQ15
M11 DQ16	L10 DQ17	N11 DQ18	M10 DQ19
R11 DQ20	R10 DQ21	T11 DQ22	T10 DQ23
M2 DQ24	L3 DQ25	N2 DQ26	M3 DQ27
R2 DQ28	R3 DQ29	T2 DQ30	T3 DQ31

FB_B_DQM_L<5>, FB_B_DQM_L<7>, FB_B_DQM_L<4>, FB_B_DQM_L<6>

FB_B_DQ<45>, FB_B_DQ<46>, FB_B_DQ<47>, FB_B_DQ<43>, FB_B_DQ<42>, FB_B_DQ<40>, FB_B_DQ<41>, FB_B_DQ<44>, FB_B_DQ<59>, FB_B_DQ<56>, FB_B_DQ<60>, FB_B_DQ<61>, FB_B_DQ<62>, FB_B_DQ<57>, FB_B_DQ<63>, FB_B_DQ<58>, FB_B_DQ<36>, FB_B_DQ<38>, FB_B_DQ<37>, FB_B_DQ<39>, FB_B_DQ<35>, FB_B_DQ<34>, FB_B_DQ<32>, FB_B_DQ<33>, FB_B_DQ<48>, FB_B_DQ<50>, FB_B_DQ<54>, FB_B_DQ<49>, FB_B_DQ<51>, FB_B_DQ<55>, FB_B_DQ<52>, FB_B_DQ<53>

FB_B_MA<0>, FB_B_MA<1>, FB_B_UMA<2>, FB_B_UMA<3>, FB_B_UMA<4>, FB_B_UMA<5>, FB_B_MA<6>, FB_B_MA<7>, FB_B_MA<8>, FB_B_MA<9>, FB_B_MA<10>, FB_B_MA<11>, FB_B_UCKE, FB_B_MA<12>

FB_B_CLK_P<1>, FB_B_CLK_N<1>, FB_B_UCS0_L, FB_B_WE_L, FB_B_UCAS_L, FB_B_RAS_L

FB_B1_ZQ, FB_B1_MF, FB_B1_SEN

FB_B_DRAM_RST

FB_B_RDQS<5>, FB_B_RDQS<7>, FB_B_RDQS<4>, FB_B_RDQS<6>

FB_B_WDQS<5>, FB_B_WDQS<7>, FB_B_WDQS<4>, FB_B_WDQS<6>

FB_B_BA<0>, FB_B_BA<1>, FB_B_BA<2>

R8598 243 1% 1/16W MF-LF 402; R8599 100 5% 1/16W MF-LF 402

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE
GDDR3 Frame Buffer B (Top)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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Page Notes

Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP3V3_GPI_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

OMIT

U8000
NV-GT216
BGA
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PP3V3_S0GPU
C8694 0.1UF 20% 10V CERM 402
C8696 1UF 10% 6.3V X5R 402
C8698 4.7UF 20% 6.3V X5R-CERM1 402
J9 J10 J11 J12 J13 VDD33

NC_GPU_ROM_CS_L
GPU_ROM_SCLK
GPU_ROM_SI
GPU_ROM_SO
C3 ROM_CS*
D4 ROM_SCLK
D3 ROM_SI
C4 ROM_SO
R8696 40.2K 1% 1/16W MF-LF 402
R8697 40.2K 1% 1/16W MF-LF 402
GPU_STRAP_REF_3V3_PD
GPU_STRAP_REF_MIOB_PD
N9 MULTI_STRAP_REF0_GND
P9 MULTI_STRAP_REF1_GND

PP3V3_S0GPU
R8620 49.9 1% 1/16W MF-LF 402
R8621 49.9 1% 1/16W MF-LF 402
GPU_MIOA_PD_VDDQ
GPU_MIOB_PD_VDDQ
GPU_MIOA_PU_GND
GPU_MIOB_PU_GND
R8622 49.9 1% 1/16W MF-LF 402
R8623 49.9 1% 1/16W MF-LF 402
R8616 10K 5% 1/16W MF-LF 402
R8618 10K 5% 1/16W MF-LF 402
R8617 10K 5% 1/16W MF-LF 402
C8617 0.1UF 10% 16V X5R 402
R8619 10K 5% 1/16W MF-LF 402
C8619 0.1UF 10% 16V X5R 402
R8660 10K 5% 1/16W MF-LF 402

C8610 1UF 10% 6.3V CERM 402
C8611 1UF 10% 6.3V CERM 402
P9 MIOA_VDDQ_1
R9 MIOA_VDDQ_2
T9 MIOA_VDDQ_3
U9 MIOA_VDDQ_4
AA9 MIOB_VDDQ_1
AB9 MIOB_VDDQ_2
W9 MIOB_VDDQ_3
Y9 MIOB_VDDQ_4

GPU_TESTMODE_PD
GPU_MIOA_VREF
GPU_MIOB_VREF
AP35 TESTMODE
N5 MIOA_VREF
AF1 MIOB_VREF
GPU_MIOA_PD_VDDQ
GPU_MIOA_PU_GND
GPU_MIOB_PD_VDDQ
GPU_MIOB_PU_GND
U5 MIOA_CAL_PD_VDDQ
T5 MIOA_CAL_PU_GND
AA7 MIOB_CAL_PD_VDDQ
AA6 MIOB_CAL_PU_GND

AF9 SP_PLLVDD
AE9 PLLVDD
AD9 VID_PLLVDD

PP1V05_S0GPU
L8635 100NH-700MA-0.14OHM 0603
PP1V1_GPU_H_PLLVDD_F
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
C8637 4.7UF 20% 6.3V CERM 603
C8635 4.7UF 20% 6.3V CERM 603
C8636 1UF 10% 6.3V X5R 402

PP1V05_S0GPU
L8640 100NH-700MA-0.14OHM 0603
PP1V1_GPU_VID_PLLVDD_F
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
C8643 4.7UF 20% 6.3V CERM 603
C8640 4.7UF 20% 6.3V CERM 603
C8641 1UF 10% 6.3V X5R 402
C8631 0.1UF 10% 16V X5R 402

GPU_CLK27M
NC_GPU_XTALOUT
B1 XTAL_IN
B2 XTAL_OUT
GPU_XTALOUTBUFF
GPU_CLK27M_SS
D1 XTAL_OUTBUFF
D2 XTAL_SSIN

GPU_STRAP<0>
GPU_STRAP<1>
GPU_STRAP<2>
W5 STRAP0
W7 STRAP1
V7 STRAP2

GPIO0 K1 GPU_VCORE_VID3
GPIO1 K2 DP_EG_HPD
GPIO2 K3 GPU_VCORE_VID4
GPIO3 H3 EG_LCD_PWR_EN
GPIO4 H2 EG_BKLT_EN
GPIO5 H1 GPU_VCORE_VID0
GPIO6 H4 GPU_VCORE_VID1
GPIO7 H5 GPU_VCORE_VID2
GPIO8 H6 SMC_GFX_OVERTEMP_R_L
GPIO9 J7 TP_GPU_GSTATE<0>
GPIO10 K4 FB_VREF_UNTERM
GPIO11 K5 GPU_GPIO_11
GPIO12 H7 SMC_GFX_THROTTLE_R_L
GPIO13 J4 FBVDD_ALTVO
GPIO14 J6 NC_GPU_GPIO_14
GPIO15 L1 NC_GPU_GPIO_15
GPIO16 L2 GPU_GPIO_16
GPIO17 L4 NC_GPU_GPIO_17
GPIO18 M4 NC_GPU_GPIO_18
GPIO19 L7 NC_GPU_GPIO_19
GPIO20 L5 NC_GPU_GPIO_20
GPIO21 K6 NC_GPU_GPIO_21
GPIO22 L6 NC_GPU_GPIO_22
GPIO23 M6 NC_GPU_GPIO_23

JTAG_TCK AP14 TP_GPU_JTAG_TCK
JTAG_TDI AN14 TP_GPU_JTAG_TDI
JTAG_TDO AN16 TP_GPU_JTAG_TDO
JTAG_TMS AR14 TP_GPU_JTAG_TMS
JTAG_TRST* AP16 TP_GPU_JTAG_TRST_L
MIOA_CLKIN N4 NC_GPU_MIOA_CLKIN
MIOA_CLKOUT R4 NC_GPU_MIOA_CLKOUT
MIOA_CLKOUT* T4 NC_GPU_MIOA_CLKOUT_N
MIOA_CTL3 P5 NC_GPU_MIOA_CTL3
MIOA_DE N2 TP_GPU_MIOA_DE
MIOA_D0 N1 TP_GPU_MIOA_D<0>
MIOA_D1 P4 TP_GPU_MIOA_D<1>
MIOA_D2 P1 TP_GPU_MIOA_D<2>
MIOA_D3 P2 TP_GPU_MIOA_D<3>
MIOA_D4 P3 TP_GPU_MIOA_D<4>
MIOA_D5 T3 TP_GPU_MIOA_D<5>
MIOA_D6 T2 TP_GPU_MIOA_D<6>
MIOA_D7 T1 TP_GPU_MIOA_D<7>
MIOA_D8 U4 TP_GPU_MIOA_D<8>
MIOA_D9 U1 TP_GPU_MIOA_D<9>
MIOA_D10 U2 GPU_MIOA_D<10>
MIOA_D11 U3 GPU_MIOA_D<11>
MIOA_D12 R6 GPU_MIOA_D<12>
MIOA_D13 T6 GPU_MIOA_D<13>
MIOA_D14 N6 GPU_MIOA_D<14>
MIOA_HSYNC N3 NC_GPU_MIOA_HSYNC
MIOA_VSYNC L3 NC_GPU_MIOA_VSYNC

MIOB_CLKIN AE1 NC_GPU_MIOB_CLKIN
MIOB_CLKOUT V4 NC_GPU_MIOB_CLKOUT
MIOB_CLKOUT* W4 NC_GPU_MIOB_CLKOUT_N
MIOB_CTL3 W3 NC_GPU_MIOB_CTL3
MIOB_DE Y5 NC_GPU_MIOB_DE
MIOB_D0 Y1 NC_GPU_MIOB_D<0>
MIOB_D1 Y2 NC_GPU_MIOB_D<1>
MIOB_D2 Y3 NC_GPU_MIOB_D<2>
MIOB_D3 AB3 NC_GPU_MIOB_D<3>
MIOB_D4 AB2 NC_GPU_MIOB_D<4>
MIOB_D5 AB1 NC_GPU_MIOB_D<5>
MIOB_D6 AC4 NC_GPU_MIOB_D<6>
MIOB_D7 AC1 NC_GPU_MIOB_D<7>
MIOB_D8 AC2 NC_GPU_MIOB_D<8>
MIOB_D9 AC3 NC_GPU_MIOB_D<9>
MIOB_D10 AE3 NC_GPU_MIOB_D<10>
MIOB_D11 AE2 NC_GPU_MIOB_D<11>
MIOB_D12 U6 NC_GPU_MIOB_D<12>
MIOB_D13 W6 NC_GPU_MIOB_D<13>
MIOB_D14 Y6 NC_GPU_MIOB_D<14>
MIOB_HSYNC W1 NC_GPU_MIOB_HSYNC
MIOB_VSYNC W2 NC_GPU_MIOB_VSYNC

THERMDP B5 GPU_TDIODE_P
THERMDN B4 GPU_TDIODE_N

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SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE
NV GT216 GPIO/MIO/MISC

Apple Inc.

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GPIOs

GPU_VCORE_VID3	GP	GPU_VCORE_VID3	MAKE_BASE=TRUE	
DP_EG_HPD	HPDC	DP_EG_HPD	MAKE_BASE=TRUE	IN
GPU_VCORE_VID4	LCD0_BL_PWM	GPU_VCORE_VID4	MAKE_BASE=TRUE	
EG_LCD_PWR_EN	LCD0_VDD	EG_LCD_PWR_EN	MAKE_BASE=TRUE	
EG_BKLT_EN	LCD0_BL_EN	EG_BKLT_EN	MAKE_BASE=TRUE	
GPU_VCORE_VID0	VID0	GPU_VCORE_VID0	MAKE_BASE=TRUE	
GPU_VCORE_VID1	VID1	GPU_VCORE_VID1	MAKE_BASE=TRUE	
GPU_VCORE_VID2	VID2/MEM_VID	GPU_VCORE_VID2	MAKE_BASE=TRUE	
SMC_GFX_OVERTEMP_R_L	THERM	SMC_GFX_OVERTEMP_R_L	MAKE_BASE=TRUE	
TP_GPU_GSTATE<0>	FAN_PWM	TP_GPU_GSTATE<0>	MAKE_BASE=TRUE	
FB_VREF_UNTERM	MEM_VREF	FB_VREF_UNTERM	MAKE_BASE=TRUE	
GPU_GPIO_11	SLI_SYNC	TP_GPU_GSTATE<1>	MAKE_BASE=TRUE	OUT
SMC_GFX_THROTTLE_R_L	AC_DET	SMC_GFX_THROTTLE_R_L	MAKE_BASE=TRUE	OUT
FBVDD_ALTVO	PWR_CTL0	FBVDD_ALTVO	MAKE_BASE=TRUE	OUT
NC_GPU_GPIO_14	PWR_CTL1	NC_GPU_GPIO_14	MAKE_BASE=TRUE	

GPIOs

NC_GPU_GPIO_15	HPDE	NC_GPU_GPIO_15	MAKE_BASE=TRUE	
GPU_GPIO_16	DVI_MODE0	EG_DP_CA_DET		
NC_GPU_GPIO_17	HDMI_DETECT0	NC_GPU_GPIO_17	MAKE_BASE=TRUE	
NC_GPU_GPIO_18	DVI_MODE1	NC_GPU_GPIO_18	MAKE_BASE=TRUE	
NC_GPU_GPIO_19	HDMI_DETECT1	NC_GPU_GPIO_19	MAKE_BASE=TRUE	
NC_GPU_GPIO_20	HPDD	NC_GPU_GPIO_20	MAKE_BASE=TRUE	
NC_GPU_GPIO_21	HPDF	NC_GPU_GPIO_21	MAKE_BASE=TRUE	
NC_GPU_GPIO_22	SWAPRDY_A	NC_GPU_GPIO_22	MAKE_BASE=TRUE	
NC_GPU_GPIO_23	GP	NC_GPU_GPIO_23	MAKE_BASE=TRUE, NO_TEST=TRUE	

Renamed signals

GPU_CLK27M	MAKE_BASE=TRUE	GPU_CLK27M
GPU_CLK27M_SS	MAKE_BASE=TRUE	GPU_CLK27M_SS
GPU_TDIODE_P	MAKE_BASE=TRUE	GPU_TDIODE_P
GPU_TDIODE_N	MAKE_BASE=TRUE	GPU_TDIODE_N
LVDS_EG_DDC_CLK	MAKE_BASE=TRUE	LVDS_EG_DDC_CLK
LVDS_EG_DDC_DATA	MAKE_BASE=TRUE	LVDS_EG_DDC_DATA
DP_EG_DDC_CLK	MAKE_BASE=TRUE	DP_EG_DDC_CLK
DP_EG_DDC_DATA	MAKE_BASE=TRUE	DP_EG_DDC_DATA

Unused signals

TP_GPU_JTAG_TCK	MAKE_BASE=TRUE	TP_GPU_JTAG_TCK	
TP_GPU_JTAG_TDI	MAKE_BASE=TRUE	TP_GPU_JTAG_TDI	
TP_GPU_JTAG_TDO	MAKE_BASE=TRUE	TP_GPU_JTAG_TDO	
TP_GPU_JTAG_TMS	MAKE_BASE=TRUE	TP_GPU_JTAG_TMS	
TP_GPU_JTAG_TRST_L	MAKE_BASE=TRUE	TP_GPU_JTAG_TRST_L	
NC_FBA_MA<13>	MAKE_BASE=TRUE, NO_TEST=TRUE	NC_FBA_MA<13>	
NC_FBB_MA<13>	MAKE_BASE=TRUE, NO_TEST=TRUE	NC_FBB_MA<13>	

Unused I2C Buses

NC_GPU_I2CC_SCL	MAKE_BASE=TRUE	NC_GPU_I2CC_SCL	NO_TEST=TRUE
NC_GPU_I2CC_SDA	MAKE_BASE=TRUE	NC_GPU_I2CC_SDA	NO_TEST=TRUE
NC_GPU_I2CH_SCL	MAKE_BASE=TRUE	NC_GPU_I2CH_SCL	NO_TEST=TRUE
NC_GPU_I2CH_SDA	MAKE_BASE=TRUE	NC_GPU_I2CH_SDA	NO_TEST=TRUE

I2CS ties into SMBus connection page
(I2CS requires pullups even if not used)

NC_FB_B_UCS1_L	MAKE_BASE=TRUE	NC_FB_B_UCS1_L	NO_TEST=TRUE
NC_FB_B_LCS1_L	MAKE_BASE=TRUE	NC_FB_B_LCS1_L	NO_TEST=TRUE
NC_GPU_ROM_CS_L	MAKE_BASE=TRUE	NC_GPU_ROM_CS_L	NO_TEST=TRUE
NC_FB_A_UCS1_L	MAKE_BASE=TRUE	NC_FB_A_UCS1_L	NO_TEST=TRUE
NC_FB_A_LCS1_L	MAKE_BASE=TRUE	NC_FB_A_LCS1_L	NO_TEST=TRUE
NC_LVDS_EG_B_CLK_P	MAKE_BASE=TRUE	NC_LVDS_EG_B_CLK_P	
NC_LVDS_EG_B_CLK_N	MAKE_BASE=TRUE	NC_LVDS_EG_B_CLK_N	
NC_LVDS_EG_A_DATA_P<3>	MAKE_BASE=TRUE	NC_LVDS_EG_A_DATA_P<3>	NO_TEST=TRUE
NC_LVDS_EG_A_DATA_N<3>	MAKE_BASE=TRUE	NC_LVDS_EG_A_DATA_N<3>	NO_TEST=TRUE
NC_LVDS_EG_B_DATA_P<3>	MAKE_BASE=TRUE	NC_LVDS_EG_B_DATA_P<3>	NO_TEST=TRUE
NC_LVDS_EG_B_DATA_N<3>	MAKE_BASE=TRUE	NC_LVDS_EG_B_DATA_N<3>	NO_TEST=TRUE

G96 MIOA_DE and MIOA_D<9..0> are used as Debug Port.

NC_GPU_MIOA_CLKOUT_P	MAKE_BASE=TRUE	NC_GPU_MIOA_CLKOUT_P	NO_TEST=TRUE
NC_GPU_MIOA_CLKOUT_N	MAKE_BASE=TRUE	NC_GPU_MIOA_CLKOUT_N	NO_TEST=TRUE
NC_GPU_MIOA_CTL3	MAKE_BASE=TRUE	NC_GPU_MIOA_CTL3	NO_TEST=TRUE
TP_GPU_MIOA_DE	MAKE_BASE=TRUE	TP_GPU_MIOA_DE	
TP_GPU_MIOA_D<9..0>	MAKE_BASE=TRUE	GPU_MIOA_D<9..0>	
NC_GPU_MIOA_CLKIN	MAKE_BASE=TRUE	NC_GPU_MIOA_CLKIN	NO_TEST=TRUE
NC_GPU_MIOA_D<14..10>	MAKE_BASE=TRUE	GPU_MIOA_D<14..10>	NO_TEST=TRUE
NC_GPU_MIOA_HSYNC	MAKE_BASE=TRUE	NC_GPU_MIOA_HSYNC	NO_TEST=TRUE
NC_GPU_MIOA_VSYNC	MAKE_BASE=TRUE	NC_GPU_MIOA_VSYNC	NO_TEST=TRUE
NC_GPU_MIOB_CLKIN	MAKE_BASE=TRUE	NC_GPU_MIOB_CLKIN	NO_TEST=TRUE
NC_GPU_MIOB_CLKOUT_P	MAKE_BASE=TRUE	NC_GPU_MIOB_CLKOUT_P	NO_TEST=TRUE
NC_GPU_MIOB_CLKOUT_N	MAKE_BASE=TRUE	NC_GPU_MIOB_CLKOUT_N	NO_TEST=TRUE
NC_GPU_MIOB_CTL3	MAKE_BASE=TRUE	NC_GPU_MIOB_CTL3	NO_TEST=TRUE
NC_GPU_MIOB_DE	MAKE_BASE=TRUE	NC_GPU_MIOB_DE	NO_TEST=TRUE
NC_GPU_MIOB_D<14..0>	MAKE_BASE=TRUE	GPU_MIOB_D<14..0>	NO_TEST=TRUE
NC_GPU_MIOB_VSYNC	MAKE_BASE=TRUE	NC_GPU_MIOB_VSYNC	NO_TEST=TRUE
NC_GPU_MIOB_HSYNC	MAKE_BASE=TRUE	NC_GPU_MIOB_HSYNC	NO_TEST=TRUE

Config Straps

PP3V3_S0GPU

R8701 45.3K 1% 1/10W MF-LF 402 — OMIT
R8703 34.8K 1% 1/10W MF-LF 402 — NO STUFF
R8705 10K 1% 1/10W MF-LF 402 — NO STUFF
GPU_STRAP<0>
GPU_STRAP<1>
GPU_STRAP<2>
R8702 2.0K 5% 1/10W MF-LF 402 — NO STUFF
R8704 10K 1% 1/10W MF-LF 402 — NO STUFF
R8706 24.9K 1% 1/10W MF-LF 402 — NO STUFF

Physical Strapping Pin	Strapping Bit 3	Strapping Bit 2	Strapping Bit 1	Strapping Bit 0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP 2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP 1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP 0	USER[3]	USER[2]	USER[1]	USER[0]

PP3V3_S0GPU

R8708 OMIT
R8710 10K 1% 1/10W MF-LF 402
R8712 15.0K 1% 1/10W MF-LF 402
GPU_ROM_SI (OUT)
GPU_ROM_SO (IN)
GPU_ROM_SCLK (IN)

Strap S1/S2 Bit[3:0] PU/PD Rval

0 0000 PD 5k
1 0001 PD 10k
2 0010 PD 15k (HYN 256)
3 0011 PD 20k (SAM 256)
4 0100 PD 25k (SAM 512)
5 0101 PD 30k
6 0110 PD 35k (HYN 512)
7 0111 PD 45k

Strap S1/S2 Bit[3:0] PU/PD Rval

8 1000 PU 5k
9 1001 PU 10k
A 1010 PU 15k
B 1011 PU 20k
C 1100 PU 25k
D 1101 PU 30k
E 1110 PU 35k
F 1111 PU 45k

PCI_DEVID[4:0]=0x14

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0353	1	RES,MTL FILM,1/16W,24.9K,1,0402,SMD,LF	R8708		VRAM_512_SAMSUNG
114S0368	1	RES,MTL FILM,1/16W,35.7K,1,0402,SMD,LF	R8708		VRAM_512_HYNIX
114S0343	1	RES,MTL FILM,1/16W,20.0K,1,0402,SMD,LF	R8708		VRAM_256_SAMSUNG
114S0331	1	RES,MTL FILM,1/16W,15.0K,1,0402,SMD,LF	R8708		VRAM_256_HYNIX

PP3V3_S0
PP3V3_S0GPU

R8750 2.2K 5% 1/10W MF-LF 402
R8751 2.2K 5% 1/10W MF-LF 402
R8752 4.7K 5% 1/10W MF-LF 402
R8753 4.7K 5% 1/10W MF-LF 402
DP_EG_DDC_CLK (IN)
DP_EG_DDC_DATA (BI)
DP_IG_DDC_CLK (IN)
DP_IG_DDC_DATA (BI)

PP3V3_S0GPU

DP_CA_DET_EG_FET
R8742 100K 5% 1/10W MF-LF 402
Q8742 SOD-VESM-HF SSM3K15FV
EG_DP_CA_DET
DP_CA_DET
R8743 0 5% 1/10W MF-LF 402
DP_CA_DET_EG
DP_CA_DET_EG_PLD

Isolation FETs for DP MUX inputs

PP3V3_S0GPU

R8796 2.2K 5% 1/10W MF-LF 402
R8797 2.2K 5% 1/10W MF-LF 402
R8798 0 5% 1/16W MF-LF 402 — NO STUFF
R8799 0 5% 1/16W MF-LF 402 — NO STUFF
SMC_GFX_OVERTEMP_R_L → SMC_GFX_OVERTEMP_L (OUT)
SMC_GFX_THROTTLE_R_L → SMC_GFX_THROTTLE_L (OUT)
EG_LCD_PWR_EN (OUT)
EG_BKLT_EN (OUT)
FBVDD_ALTVO (OUT)
FB_VREF_UNTERM (OUT)

R8792 10K 5% 1/10W MF-LF 402
R8793 10K 5% 1/10W MF-LF 402
R8794 10K 5% 1/10W MF-LF 402
R8795 10K 5% 1/10W MF-LF 402 — NO STUFF

Unused Clocks

GPU_CLK27M_SS
GPU_XTALOUTBUFF
R8780 10K 5% 1/10W MF-LF 402
R8781 10K 5% 1/10W MF-LF 402 — GPU_SS_INT

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: GT216 GPIOS & STRAPS

Apple Inc.

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REVISION: <E4LABEL>
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Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents: 240mA

72 7 6 PP1V8_GPUIFPX

81 79 76 74 7 6 PP1V05_S0GPU

GPU_IFPEF_RSET 81
GPU_IFPC_RSET 81
GPU_IFPAB_RSET 81
GPU_IFPD_RSET 81

R8855 1K 1% 1/16W MF-LF 0402
R8850 1K 1% 1/16W MF-LF 0402
R8851 1K 1% 1/16W MF-LF 0402
R8858 1K 1% 1/16W MF-LF 0402

PP1V1_GPU_IFPEF_IOVDD_F 81
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.1V

PP1V8_GPU_IFPEF_PLLVDD_F 81
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.8V
Power inputs must be pulled down if not used

R8856 10K 5% 1/16W MF-LF 0402
R8857 10K 5% 1/16W MF-LF 0402

CRITICAL
L8800 300-OHM-0.5A 0603-1
?mA peak per diff pair
?mA peak for all pairs
C8800 4.7UF 20% 6.3V CERM 603
C8801 0.1UF 20% 10V CERM 402
C8803 0.1UF 20% 10V CERM 402
Place at AG9
Place at AG10

PP1V8_GPU_IFPAB_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

L8805 180-OHM-1.5A 0603
80mA peak
PP1V1_GPU_IFPAB_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.1V
C8805 4.7UF 20% 6.3V CERM 603
C8806 1UF 10% 6.3V CERM 402

L8810 180-OHM-1.5A 0603
86 81 79 76 74 7 6 PP1V05_S0GPU
?mA peak per diff pair
?mA peak for all pairs
C8810 4.7UF 20% 6.3V CERM 603
C8811 0.1UF 20% 10V CERM 402
C8813 0.1UF 20% 10V CERM 402
Place at AJ8
Place at AK8

PP1V1_GPU_IFPCD_IOVDD_F 81
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.1V

I2CS must be pulled up if not used
I2CS addr fixed at 0x9E,0x9F

CRITICAL
L8815 300-OHM-0.5A 0603-1
84 82 81 80 79 74 72 7 6 PP3V3_S0GPU
160mA peak
C8815 4.7UF 20% 6.3V CERM 603
C8816 1UF 10% 6.3V CERM 402

PP3V3_GPU_IFPC_PLLVDD_F 81
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

I2CS must be pulled up if not used.
I2CS addr fixed at 0x9E,0x9F

R8852 10K 5% 1/16W MF-LF 0402
R8853 10K 5% 1/16W MF-LF 0402
R8854 10K 5% 1/16W MF-LF 0402

PP1V8_GPU_IFPD_PLLVDD
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.8V

OMIT

U8000
NV-GT216
BGA
(5 OF 9)

AG9	IFPA_IOVDD	IFPA_TXC	AM11
AG10	IFPB_IOVDD	IFPA_TXC*	AM12
AJ8	IFPC_IOVDD	IFPA_TXD0	AM8
AK8	IFPD_IOVDD	IFPA_TXD0*	AL8
AE7	IFPE_IOVDD	IFPA_TXD1	AM10
AD7	IFPF_IOVDD	IFPA_TXD1*	AM9
AK9	IFPAB_PLLVDD	IFPA_TXD2	AK10
AJ11	IFPAB_RSET	IFPA_TXD2*	AL10
AJ9	IFPC_PLLVDD	IFPA_TXD3	AK11
AK7	IFPC_RSET	IFPA_TXD3*	AL11
AJ6	IFPEF_PLLVDD	IFPB_TXC	AP13
AL1	IFPEF_RSET	IFPB_TXC*	AN13
		IFPB_TXD4	AN8
		IFPB_TXD4*	AP8
		IFPB_TXD5	AP10
		IFPB_TXD5*	AN10
		IFPB_TXD6	AR11
		IFPB_TXD6*	AR10
		IFPB_TXD7	AN11
		IFPB_TXD7*	AP11
G1	I2CA_SCL	IFPC_AUX_I2CW_SCL	AP2
G4	I2CA_SDA	IFPC_AUX_I2CW_SDA*	AN3
E3	I2CC_SCL	IFPC_L0	AM7
E4	I2CC_SDA	IFPC_L0*	AM6
		IFPC_L1	AL5
		IFPC_L1*	AM5
		IFPC_L2	AM3
		IFPC_L2*	AM4
		IFPC_L3	AP1
		IFPC_L3*	AR2
E2	I2CS_SCL	IFPD_AUX_I2CX_SCL	AP4
E1	I2CS_SDA	IFPD_AUX_I2CX_SDA*	AN4
F6	I2CH_SCL	IFPD_L0	AP6
G6	I2CH_SDA	IFPD_L0*	AP7
		IFPD_L1	AP9
		IFPD_L1*	AN9
		IFPD_L2	AN6
		IFPD_L2*	AP5
		IFPD_L3	AR5
		IFPD_L3*	AR4
G3	I2CB_SCL	IFPE_AUX_I2CY_SCL	AE4
G2	I2CB_SDA	IFPE_AUX_I2CY_SDA*	AD4
		IFPE_L0	AH6
		IFPE_L0*	AH5
		IFPE_L1	AH4
		IFPE_L1*	AG4
		IFPE_L2	AF4
		IFPE_L2*	AF5
		IFPE_L3	AE6
		IFPE_L3*	AE5
		IFPF_AUX_I2CZ_SCL	AE3
		IFPF_AUX_I2CZ_SDA*	AE2
		IFPF_L0	AL2
		IFPF_L0*	AL3
		IFPF_L1	AJ3
		IFPF_L1*	AJ2
		IFPF_L2	AH1
		IFPF_L2*	AH2
		IFPF_L3	AG3
		IFPF_L3*	AG2
AJ12	DACA_VDD	DACA_RED	AM16
		DACA_GREEN	AM14
		DACA_BLUE	AL14
AK12	DACA_VREF	DACA_HSYNC	AM13
NCX	DACA_RSET	DACA_VSYNC	AL13
AG7	DACB_VDD	DACB_RED	AK4
		DACB_GREEN	AL4
		DACB_BLUE	AJ4
AK6	DACB_VREF	CEC	AB5
NCX	DACB_RSET		
AC6	IFPD_PLLVDD		
		DACB_HSYNC	AM1
AB6	IFPD_RSET	DACB_VSYNC	AM2

LVDS_EG_DDC_CLK 84 86 B1
LVDS_EG_DDC_DATA 84 86 B1
NC_GPU_I2CC_SCL 89 B1
NC_GPU_I2CC_SDA 89 B1
SMBUS_SMC_0_S0_SCL 97 51 48 45 B1
SMBUS_SMC_0_S0_SDA 97 51 48 45 B1
NC_GPU_I2CH_SDA 89 B1
NC_GPU_I2CH_SCL 89 B1
DP_EG_DDC_CLK 84 86 B1
DP_EG_DDC_DATA 84 86 B1
GPU_IFPD_RSET 81

LVDS_EG_A_CLK_P OUT 87 98
LVDS_EG_A_CLK_N OUT 87 98
LVDS_EG_A_DATA_P<0> OUT 87 98
LVDS_EG_A_DATA_N<0> OUT 87 98
LVDS_EG_A_DATA_P<1> OUT 87 98
LVDS_EG_A_DATA_N<1> OUT 87 98
LVDS_EG_A_DATA_P<2> OUT 87 98
LVDS_EG_A_DATA_N<2> OUT 87 98
NC_LVDS_EG_A_DATA_P<3> OUT 80 98
NC_LVDS_EG_A_DATA_N<3> OUT 80 98
NC_LVDS_EG_B_CLK_P OUT 80
NC_LVDS_EG_B_CLK_N OUT 80
LVDS_EG_B_DATA_P<0> OUT 87 98
LVDS_EG_B_DATA_N<0> OUT 87 98
LVDS_EG_B_DATA_P<1> OUT 87 98
LVDS_EG_B_DATA_N<1> OUT 87 98
LVDS_EG_B_DATA_P<2> OUT 87 98
LVDS_EG_B_DATA_N<2> OUT 87 98
NC_LVDS_EG_B_DATA_P<3> OUT 80 98
NC_LVDS_EG_B_DATA_N<3> OUT 80 98
DP_EG_AUX_CH_P OUT 84 98
DP_EG_AUX_CH_N OUT 84 98
DP_EG_ML_P<0> OUT 84 98
DP_EG_ML_N<0> OUT 84 98
DP_EG_ML_P<1> OUT 84 98
DP_EG_ML_N<1> OUT 84 98
DP_EG_ML_P<2> OUT 84 98
DP_EG_ML_N<2> OUT 84 98
DP_EG_ML_P<3> OUT 84 98
DP_EG_ML_N<3> OUT 84 98

NO STUFF
R8861 1K 5% 1/16W MF-LF 0402
NO STUFF
R8860 1K 5% 1/16W MF-LF 0402

PP3V3_S0GPU
6 7 72 74 79 80 81 82 84
R8859 10K 5% 1/16W MF-LF 0402
GPU_CEC

GPU_DACA_VDD
GPU_DACB_VDD

NC
NC
NC

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SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE
NV GT216 VIDEO INTERFACES

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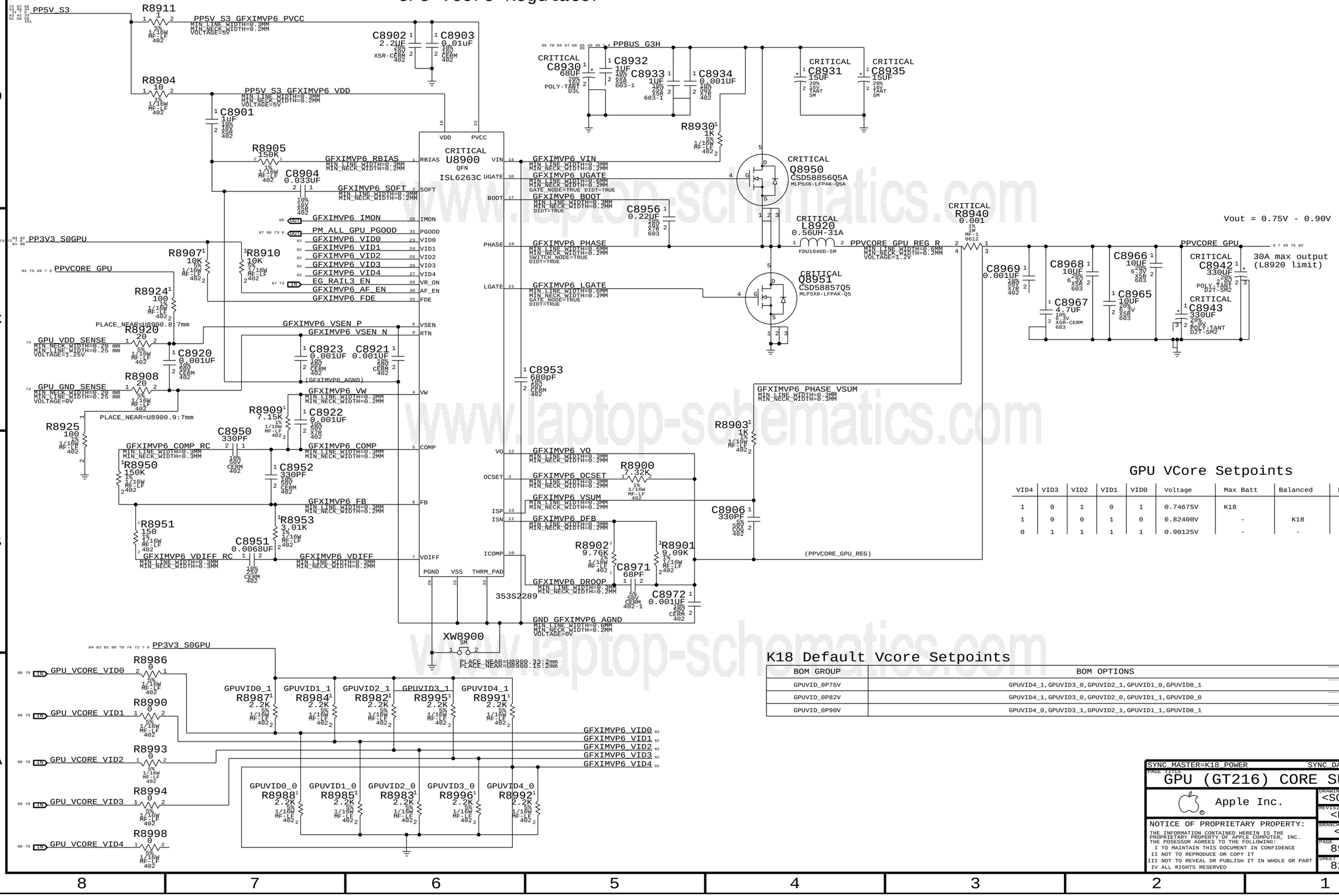
GPU VCore Regulator



GPU VCore Setpoints

VID4	VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	0	1	0	1	0.74675V	K18		-
1	0	0	1	0	0.82400V	-	K18	-
0	1	1	1	1	0.90125V	-	-	K18

K18 Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_0P75V	GPUVID4_1,GPUVID3_0,GPUVID2_1,GPUVID1_0,GPUVID0_1
GPUVID_0P82V	GPUVID4_1,GPUVID3_0,GPUVID2_0,GPUVID1_1,GPUVID0_0
GPUVID_0P90V	GPUVID4_0,GPUVID3_1,GPUVID2_1,GPUVID1_1,GPUVID0_1

SYNC_MASTER=K18_POWER SYNC_DATE=07/14/2009

PAGE TITLE

GPU (GT216) CORE SUPPLY

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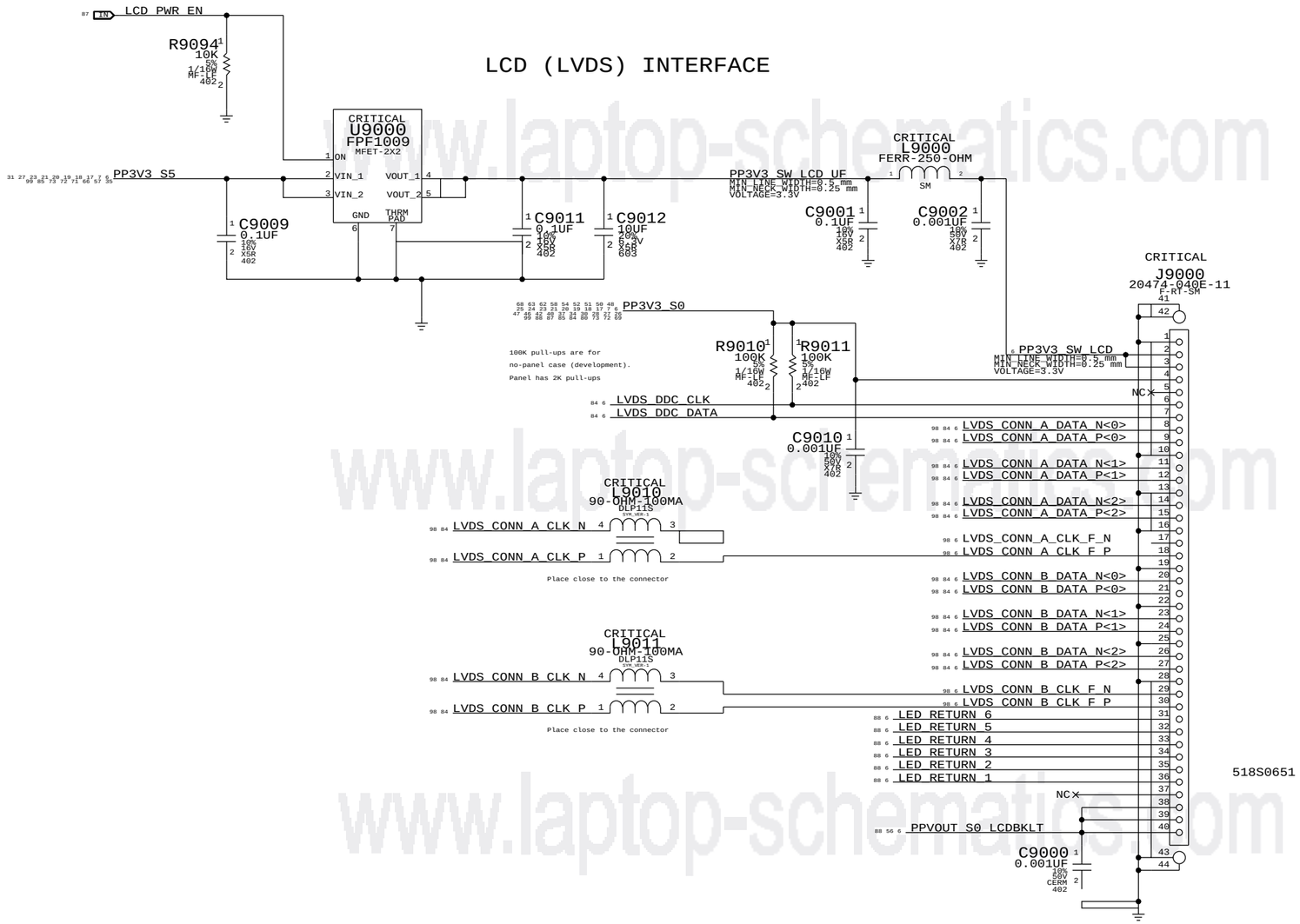
LCD (LVDS) INTERFACE



518S0651

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SYNC_MASTER=K19_MLB SYNC_DATE=05/29/2009

PAGE TITLE: LVDS Display Connector

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LVDS Transmitter Termination

All emulated LVDS outputs require this termination

PLACE_NEAR=U9600.A6:7mm
R9320 357 1% 1/10W MF-LF 402
LVDS_A_CLK_P → LVDS_CONN_A_CLK_P

PLACE_NEAR=U9600.A7:7mm
R9322 357 1% 1/10W MF-LF 402
LVDS_A_CLK_N → LVDS_CONN_A_CLK_N

R9325 357 1% 1/10W MF-LF 402
LVDS_A_DATA_P<0> → LVDS_CONN_A_DATA_P<0>
PLACE_NEAR=U9600.A8:7mm

PLACE_NEAR=U9600.B9:7mm
R9327 357 1% 1/10W MF-LF 402
LVDS_A_DATA_N<0> → LVDS_CONN_A_DATA_N<0>

R9330 357 1% 1/10W MF-LF 402
LVDS_A_DATA_P<1> → LVDS_CONN_A_DATA_P<1>
PLACE_NEAR=U9600.A9:7mm

PLACE_NEAR=U9600.C10:7mm
R9332 357 1% 1/10W MF-LF 402
LVDS_A_DATA_N<1> → LVDS_CONN_A_DATA_N<1>

R9335 357 1% 1/10W MF-LF 402
LVDS_A_DATA_P<2> → LVDS_CONN_A_DATA_P<2>
PLACE_NEAR=U9600.B10:7mm

PLACE_NEAR=U9600.A10:7mm
R9337 357 1% 1/10W MF-LF 402
LVDS_A_DATA_N<2> → LVDS_CONN_A_DATA_N<2>

R9340 357 1% 1/10W MF-LF 402
LVDS_B_CLK_P → LVDS_CONN_B_CLK_P
PLACE_NEAR=U9600.C8:7mm

PLACE_NEAR=U9600.C9:7mm
R9342 357 1% 1/10W MF-LF 402
LVDS_B_CLK_N → LVDS_CONN_B_CLK_N

R9345 357 1% 1/10W MF-LF 402
LVDS_B_DATA_P<0> → LVDS_CONN_B_DATA_P<0>
PLACE_NEAR=U9600.A2:7mm

PLACE_NEAR=U9600.A3:7mm
R9347 357 1% 1/10W MF-LF 402
LVDS_B_DATA_N<0> → LVDS_CONN_B_DATA_N<0>

R9350 357 1% 1/10W MF-LF 402
LVDS_B_DATA_P<1> → LVDS_CONN_B_DATA_P<1>
PLACE_NEAR=U9600.A1:7mm

PLACE_NEAR=U9600.B3:7mm
R9352 357 1% 1/10W MF-LF 402
LVDS_B_DATA_N<1> → LVDS_CONN_B_DATA_N<1>

R9355 357 1% 1/10W MF-LF 402
LVDS_B_DATA_P<2> → LVDS_CONN_B_DATA_P<2>
PLACE_NEAR=U9600.C5:7mm

R9357 357 1% 1/10W MF-LF 402
LVDS_B_DATA_N<2> → LVDS_CONN_B_DATA_N<2>
PLACE_NEAR=U9600.A5:7mm

DisplayPort Mux

PP3V3_S0

U9320 CBTL06141EE BGA CRITICAL

DP_IG_ML_P<0> → DIN1_0+ / DOUT_0+ → DP_ML_P<0>
DP_IG_ML_N<0> → DIN1_0- / DOUT_0- → DP_ML_N<0>
DP_IG_ML_P<1> → DIN1_1+ / DOUT_1+ → DP_ML_P<1>
DP_IG_ML_N<1> → DIN1_1- / DOUT_1- → DP_ML_N<1>
DP_IG_ML_P<2> → DIN1_2+ / DOUT_2+ → DP_ML_P<2>
DP_IG_ML_N<2> → DIN1_2- / DOUT_2- → DP_ML_N<2>
DP_IG_ML_P<3> → DIN1_3+ / DOUT_3+ → DP_ML_P<3>
DP_IG_ML_N<3> → DIN1_3- / DOUT_3- → DP_ML_N<3>
DP_IG_AUX_CH_P → C9330 0.1uF → DAUX1+ / AUX+ → DP_AUX_CH_C_P
DP_IG_AUX_CH_N → C9331 0.1uF → DAUX1- / AUX- → DP_AUX_CH_C_N
DP_IG_DDC_CLK → DDC_CLK1
DP_IG_DDC_DATA → DDC_DAT1
DP_IG_HPD → R9304 100K → HPD_1
PLACE_NEAR=U9320.J1:3mm

DP_EG_ML_P<0> → DIN2_0+
DP_EG_ML_N<0> → DIN2_0-
DP_EG_ML_P<1> → DIN2_1+
DP_EG_ML_N<1> → DIN2_1-
DP_EG_ML_P<2> → DIN2_2+
DP_EG_ML_N<2> → DIN2_2-
DP_EG_ML_P<3> → DIN2_3+
DP_EG_ML_N<3> → DIN2_3-
DP_EG_AUX_CH_P → C9335 0.1uF → DAUX2+
DP_EG_AUX_CH_N → C9336 0.1uF → DAUX2-
DP_EG_DDC_CLK → DDC_CLK2
DP_EG_DDC_DATA → DDC_DAT2
DP_EG_HPD → R9305 100K → HPD_2

LO=PORT1 HI=PORT2
DP_MUX_SEL_EG → GPU_SEL
LO=AUX_CH HI=DDC
DDC_AUX_SEL → DP_CA_DET

DP_MUX_XSD_L → XSD*
TST0 → GND
DPMUX_EN_HPD → R9301 10K → PP3V3_S0
DPMUX_EN_HPD → C9301 1UF → GND
DPMUX_EN_PLD → R9302 10K → PP3V3_S0
DPMUX_EN_S0&DPMUX_EN_PLD
DP_MUX_EN → R9303 0 → DPMUX_EN_PLD

HPDIN ← DP_HPD_R ← R9307 1K ← DP_HOTPLUG_DET
DP_HOTPLUG_DET → DP_HOTPLUG_DET MAKE_BASE=TRUE

LVDS DDC MUX

PP3V3_S0GPU
PP3V3_S0
R9370 20K
R9371 20K
R9372 20K
R9373 20K
C9370 0.1UF

U9370 SN74LV4066A QFN1 CRITICAL
VCC
GND_THRM

LVDS_DDC_SEL_EG → C1
LVDS_DDC_SEL_IG → C2
C3
C4

A1 ↔ B1 : LVDS_EG_DDC_CLK
A2 ↔ B2 : LVDS_IG_DDC_CLK / LVDS_DDC_CLK
A3 ↔ B3 : LVDS_EG_DDC_DATA
A4 ↔ B4 : LVDS_IG_DDC_DATA / LVDS_DDC_DATA

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SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: Muxed Graphics Support

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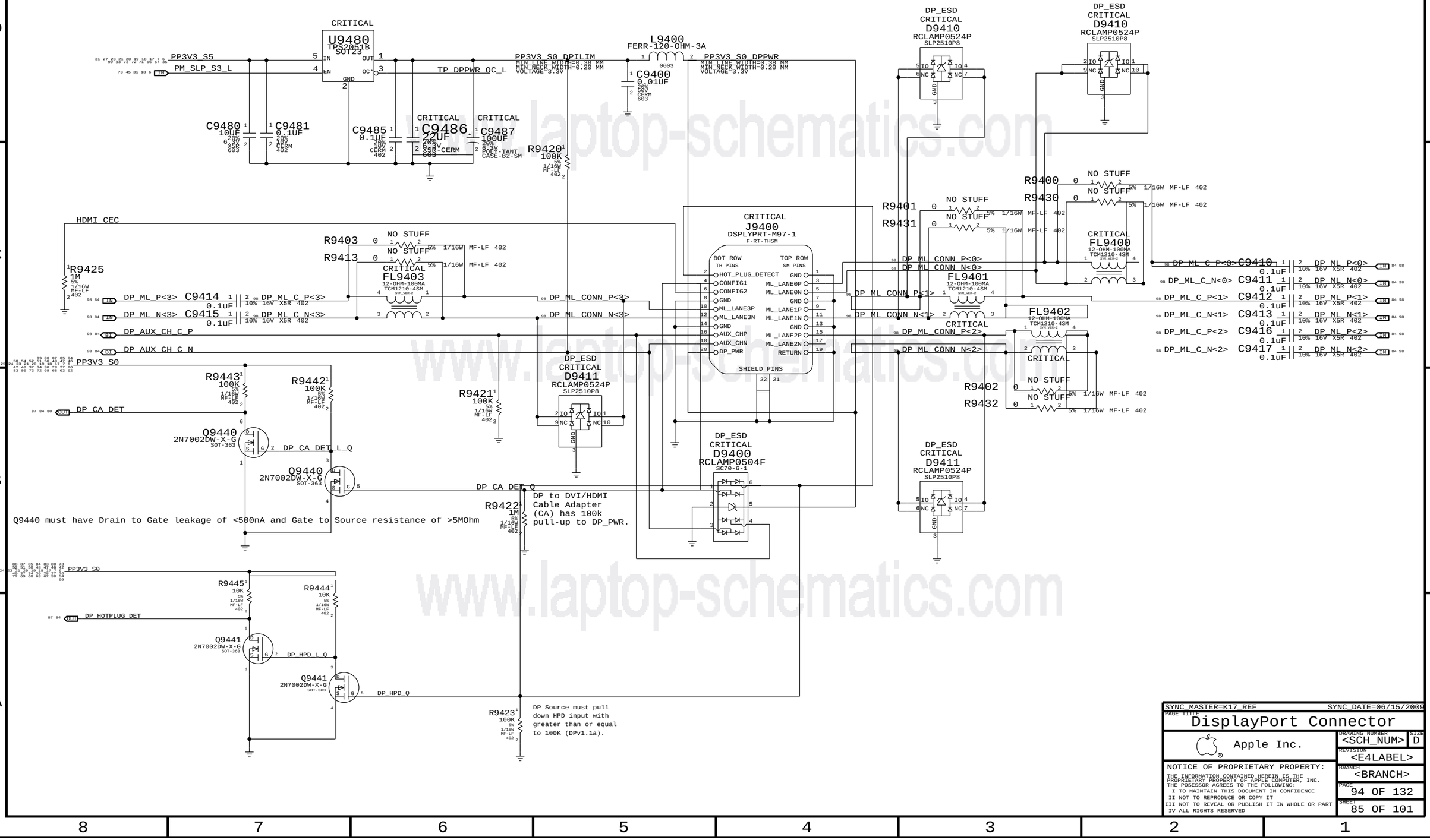
Port Power Switch



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SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: DisplayPort Connector

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DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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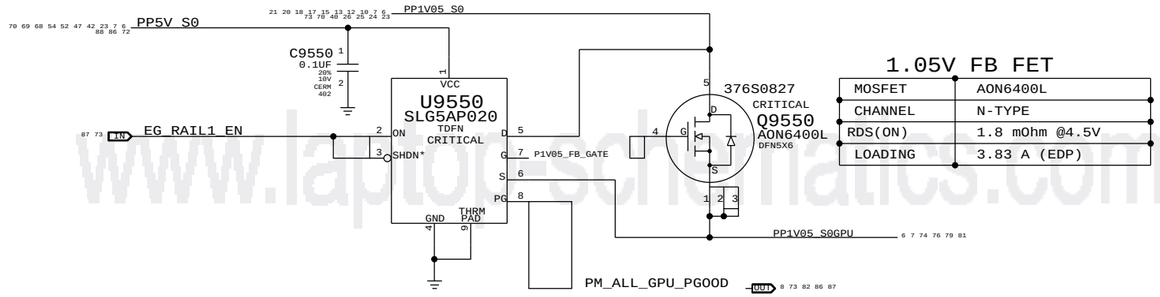
1V05 S0 GPU FET



1.05V FB FET

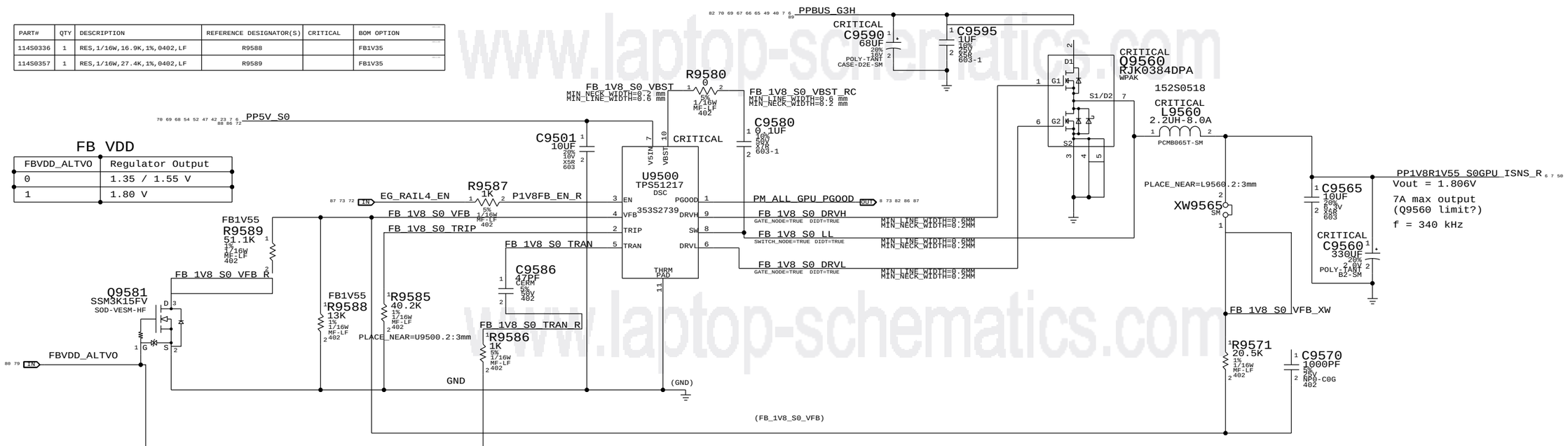
MOSFET	AON6400L
CHANNEL	N-TYPE
RDS(ON)	1.8 mOhm @4.5V
LOADING	3.83 A (EDP)

1V8 / 1V55 / 1V35 S0 FRAMEBUFFER REGULATOR

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0336	1	RES,1/16W,16.9K,1%,0402,LF	R9588		FB1V35
114S0357	1	RES,1/16W,27.4K,1%,0402,LF	R9589		FB1V35

FB_VDD

FBVDD_ALTVO	Regulator Output
0	1.35 / 1.55 V
1	1.80 V



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SYNC_MASTER=K18_POWER SYNC_DATE=06/26/2009

PAGE TITLE
1V8 / 1V55 FB Power Supply

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GMUX CPLD

LVDS Receiver Termination

LVDS_IG_A_CLK_P	R9650	100	PLACE_NEAR=U9600.H3:5mm	LVDS_IG_A_CLK_N
LVDS_IG_A_DATA_P<0>	R9651	100	PLACE_NEAR=U9600.E1:5mm	LVDS_IG_A_DATA_N<0>
LVDS_IG_A_DATA_P<1>	R9652	100	PLACE_NEAR=U9600.E3:5mm	LVDS_IG_A_DATA_N<1>
LVDS_IG_A_DATA_P<2>	R9653	100	PLACE_NEAR=U9600.G1:5mm	LVDS_IG_A_DATA_N<2>
LVDS_IG_B_DATA_P<0>	R9654	100	PLACE_NEAR=U9600.G2:5mm	LVDS_IG_B_DATA_N<0>
LVDS_IG_B_DATA_P<1>	R9655	100	PLACE_NEAR=U9600.G3:5mm	LVDS_IG_B_DATA_N<1>
LVDS_IG_B_DATA_P<2>	R9656	100	PLACE_NEAR=U9600.B2:5mm	LVDS_IG_B_DATA_N<2>
LVDS_EG_A_CLK_P	R9660	100	PLACE_NEAR=U9600.J12:5mm	LVDS_EG_A_CLK_N
LVDS_EG_A_DATA_P<0>	R9661	100	PLACE_NEAR=U9600.D13:5mm	LVDS_EG_A_DATA_N<0>
LVDS_EG_A_DATA_P<1>	R9662	100	PLACE_NEAR=U9600.E14:5mm	LVDS_EG_A_DATA_N<1>
LVDS_EG_A_DATA_P<2>	R9663	100	PLACE_NEAR=U9600.E12:5mm	LVDS_EG_A_DATA_N<2>
LVDS_EG_B_DATA_P<0>	R9664	100	PLACE_NEAR=U9600.G14:5mm	LVDS_EG_B_DATA_N<0>
LVDS_EG_B_DATA_P<1>	R9665	100	PLACE_NEAR=U9600.G13:5mm	LVDS_EG_B_DATA_N<1>
LVDS_EG_B_DATA_P<2>	R9666	100	PLACE_NEAR=U9600.H12:5mm	LVDS_EG_B_DATA_N<2>

All: 1% 1/16W MF-LF 402

Required Pullups

SIGNAL_MODEL=EMPTY

GMUX_DEBUG_RESET_L	R9680	1K	PP3V3_S0
EG_PWRSEQ_EN	R9684	1K	PP3V3_S0

5% 1/16W MF-LF 402

NO STUFF
R9679 10K 1% 1/16W MF-LF 402
SILK_PART=GMUX_RST

Required Pulldowns

DP_MUX_SEL_EG	R9681	10K	
LVDS_DDC_SEL_IG	R9682	10K	
LVDS_DDC_SEL_EG	R9683	10K	NO STUFF
EG_RESET_L	R9691	100K	
LCD_BKLT_PWM	R9693	100K	

5% 1/16W MF-LF 402

(Use open-drain PGOOD output to hold off the start of the GPU PWRSEQ until the first GPU rail's source is valid)

Power rails

- PP3V3_S0 — R9600 0 5% 1/16W MF-LF 402
- PP1V8_S0 — R9610 0 5% 1/16W MF-LF 402
- PP1V2_S0
- PP3V3_S0 — R9640 10K 1% 1/16W MF-LF 402; R9645 10K 1% 1/16W MF-LF 402
- NO STUFF R9641 10K 1% 1/16W MF-LF 402
- NO STUFF R9646 10K 1% 1/16W MF-LF 402
- GMUX_CFG0
- GMUX_TOE
- PP3V3_S0 — R9611 0 5% 1/16W MF-LF 402 (GMUXPLL_1V8)
- PP1V8_S0
- PP3V3_S0 — R9612 0 5% 1/16W MF-LF 402 (GMUXPLL_3V3)
- PP3V3R1V8_S0_GMUX_ULC_VCCPLL — L9621 FERR-220-OHM 0402; C9631 0.1UF
- PP3V3R1V8_S0_GMUX_LRC_VCCPLL — L9620 FERR-220-OHM 0402; C9630 0.1UF
- PP3V3_S3 — R9676 100K 5% 1/16W MF-LF 402
- NO STUFF R9675 0 5% 1/16W MF-LF 402
- NO STUFF R9670 10K 1% 1/16W MF-LF 402
- NO STUFF R9647 10K 1% 1/16W MF-LF 402

Decoupling

- PP3V3_S0 S0_GMUX_R: C9610–C9629 0.1UF 20% 10V CERM 402
- PP1V8_S0 GMUX_R: C9611–C9617 0.1UF 20% 10V CERM 402
- PP1V2_S0: C9600 4.7UF 20% 10V X5R 402; C9604–C9609 0.1UF 20% 10V CERM 402

U9600 XP25-5 CSBGA

OMIT CRITICAL

VCC: C4, J3, J13, N11, P8
VCCAUX: C11, J4, J14, M8
VCCIO06: B5
VCCIO01: B7
VCCIO02: A12, C14
VCCIO03: F13, M12
VCCIO04: M9
VCCIO05: M3
VCCIO06: N5
VCCIO6: M1
VCCIO07: C3, F2
VCCJ: K12
ULC_VCCPLL: A4
LRC_VCCPLL: P11

JTAG_GMUX_TCK	K14	TCK
JTAG_GMUX_TDI	L13	TDI
JTAG_GMUX_TDO	K13	TDO
JTAG_GMUX_TMS	L12	TMS
GMUX_TOE	K2	TOE
GMUX_CFG0	K1	CFG0

BANK5

LCD_BKLT_EN	P2	PB7A
LCD_BKLT_PWM	N2	PB7B
LVDS_DDC_SEL_EG	P4	PB14A
LVDS_DDC_SEL_IG	N4	PB14B
DP_MUX_EN	N3	PB15A (OD)
DP_MUX_SEL_EG	M4	PB15B
EG_RESET_L	P5	PB16A
EG_RAIL1_EN	M5	PB16B
EG_RAIL2_EN	P6	PB17A
EG_RAIL3_EN	M6	PB17B
EG_RAIL4_EN	P7	PB18A
PEG_CLKREQ_L	M7	PB18B (OD)
DP_CA_DET_EG	N7	PB19A
LCD_PWR_EN	N8	PB19B

BANK4

LPC_AD<0>	P9	PB20A
LPC_AD<1>	N9	PB20B
LPC_AD<2>	P10	PB26A
LPC_AD<3>	M10	PB26B
LPC_FRAME_L	P12	PB27A
LPCPLUS_RESET_L	P13	PB27B
LPC_CLK33M_GMUX	N12	PB28A
GMUX_INT	P14	PB28B

BANK7

LVDS_IG_B_DATA_P<2>	B1	PL2A
LVDS_IG_B_DATA_N<2>	B2	PL2B
GMUX_PL10A	C2	PL6A
TP_GMUX_PL10B	D3	PL6B
LVDS_IG_A_DATA_P<0>	D1	PL7A
LVDS_IG_A_DATA_N<0>	E1	PL7B
LVDS_IG_A_DATA_P<1>	D2	PL8A
LVDS_IG_A_DATA_N<1>	E3	PL8B
LVDS_IG_A_DATA_P<2>	F1	PL9A
LVDS_IG_A_DATA_N<2>	G1	PL9B
LVDS_IG_B_DATA_P<0>	F3	PL10A
LVDS_IG_B_DATA_N<0>	G2	PL10B
LVDS_IG_B_DATA_P<1>	H2	PL11A
LVDS_IG_B_DATA_N<1>	G3	PL11B
LVDS_IG_A_CLK_P	H1	PL12A
LVDS_IG_A_CLK_N	H3	PL12B

BANK6

TP_LVDS_MUX_SEL_EG	L1	PL14A
GMUX_VSYNC	L3	PL14B
GMUX_RESET_L	K3	PL15A
GMUX_VSYNC	L2	PL15B
PM_ALL_GPU_PGOOD	N1	PL25A
PEX_CLKREQ_L	P1	PL25B

(Tie/strap low if EGPU doesn't provide CLKREQ_L output, provide pullup to GPU rail if using CLKREQ_L output from EGPU)

BANK0

LVDS_B_DATA_P<0>	A2	PT7A
LVDS_B_DATA_N<0>	A3	PT7B
LVDS_B_DATA_P<1>	A1	PT8A
LVDS_B_DATA_N<1>	B3	PT8B
LVDS_B_DATA_P<2>	C5	PT9A
LVDS_B_DATA_N<2>	A5	PT9B
EG_PWRSEQ_EN	B6	PT14A
GMUX_DEBUG_RESET_L	C7	PT14B
LVDS_A_CLK_P	A6	PT15A
LVDS_A_CLK_N	A7	PT15B
LVDS_B_CLK_P	C8	PT16A
LVDS_B_CLK_N	C9	PT16B
LVDS_A_DATA_P<0>	A8	PT17A
LVDS_A_DATA_N<0>	B9	PT17B
LVDS_A_DATA_P<1>	A9	PT18A
LVDS_A_DATA_N<1>	C10	PT18B
LVDS_A_DATA_P<2>	B10	PT19A
LVDS_A_DATA_N<2>	A10	PT19B
GND	A11	PT20A
GND	B12	PT20B
GND	B13	PT28A
GND	A13	PT28B

BANK1

BANK2

DP_CA_DET	A14	PR2A
DP_HOTPLUG_DET	B14	PR2B
LVDS_EG_A_DATA_P<0>	D12	PR6A
LVDS_EG_A_DATA_N<0>	D13	PR6B
LVDS_EG_A_DATA_P<1>	D14	PR7A
LVDS_EG_A_DATA_N<1>	E14	PR7B
LVDS_EG_A_DATA_P<2>	E12	PR8A
LVDS_EG_A_DATA_N<2>	F12	PR8B
LVDS_EG_B_DATA_P<0>	F14	PR9A
LVDS_EG_B_DATA_N<0>	G14	PR9B
LVDS_EG_B_DATA_P<1>	G12	PR10A
LVDS_EG_B_DATA_N<1>	G13	PR10B
LVDS_EG_B_DATA_P<2>	H13	PR11A
LVDS_EG_B_DATA_N<2>	H12	PR11B
LVDS_EG_A_CLK_P	H14	PR12A
LVDS_EG_A_CLK_N	J12	PR12B
LVDS_EG_PANEL_PWR	L14	PR14A
EG_LCD_PWR_EN	M13	PR14B
LVDS_IG_BKL_ON	N14	PR24A
EG_BKLT_EN	N13	PR24B

BANK3

GMUX_JTAG_CONN

CRITICAL J9600 1909782 M-RT-SM

1	PP3V3_S0
2	JTAG_GMUX_TDO
3	JTAG_GMUX_TDI
4	JTAG_GMUX_TMS
5	
6	JTAG_GMUX_TCK
7	
8	

Q9607 SSM6N15FEAPE SOT563

- EG_RAIL1_EN
- EG_RAIL2_EN
- EG_RAIL3_EN
- EG_RAIL4_EN
- LCD_PWR_EN
- R9678 4.7K 5% 1/16W MF-LF 402
- R9671 4.7K 5% 1/16W MF-LF 402
- R9672 4.7K 5% 1/16W MF-LF 402
- R9673 4.7K 5% 1/16W MF-LF 402
- R9674 4.7K 5% 1/16W MF-LF 402
- GMUX_S3_PD_GND
- GMUX_S3_PD_EN
- ALL_SYS_PWRGD

GND

GNDIO0, GNDIO1, GNDIO2, GNDIO3, GNDIO4, GNDIO5, GNDIO6, GNDIO7, ULC_GNDPLL, LRC_GNDPLL

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SYNC_MASTER=K17_REF	SYNC_DATE=06/15/2009
PAGE TITLE	Graphics MUX (GMUX)
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*L9701, D9701, C9796, C9797, C9799, C9712 AND C9713 SHOULD ALL BE PLACED NEAR EACHOTHER.
*PPVOUT_S0_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
* LVDS_IG_BKL_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

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PP5V_S0
R9701 0 5% 1/16W MF-LF 402 — MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=5V
R9702 0 5% 1/16W MF-LF 402
XW9700 SM
PPBUS_S0_LCDBKLT_PWR
CRITICAL C9712 10UF 10% 16V X5R 805
C9713 0.1UF 10% 25V X5R 402
CRITICAL L9701 22UH-2.5A IHLP2525CZ-SM
PPVIN_BKL — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.375 MM, VOLTAGE=8.4V
PPBUS_S0_LCDBKLT_PWR_SW — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.375 MM, VOLTAGE=50V, SWITCH_NODE=TRUE
CRITICAL D9701 SOD-123 RB160M-60G
PPVOUT_S0_LCDBKLT — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=50V
NO STUFF R9703 0 5% 1/16W MF-LF 402
C9796 220PF 10% 50V X7R-CERM 402
CRITICAL C9797 10UF 10% 50V X5R 1210-1
CRITICAL C9799 10UF 10% 50V X5R 1210-1
PPVIN_BKL_R — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM

PP3V3_S0
BKL_VLDO
C9714 0.01UF 10% 16V X7R-CERM 402
C9710 1UF 10% 25V X5R 603-1
C9711 0.1UF 10% 16V X5R 402
NO STUFF C9741 1UF 10% 6.3V X5R 402
NO STUFF C9740 10UF 20% 6.3V X5R 603
R9740 47.0K 1% 1/16W MF-LF 402
BKL_FLTR_RC
R9741 10K 5% 1/16W MF-LF 402
VOLTAGE=5V

CRITICAL
U9701 LLP LP8545SQX
VDDIO (8) VLDO (22) VIN (23)
NCX (6) GD — SW (24)
BKL_FSET (5) FSET — FB (21)
BKL_FLTR (20) FILTER — OUT1 (12) BKL_ISEN1
ISET (3) — OUT2 (13) BKL_ISEN2
SCLK (10) — OUT3 (14) BKL_ISEN3
SDA (11) — OUT4 (16) BKL_ISEN4
PWM (2) — OUT5 (17) BKL_ISEN5
FAULT (7) — OUT6 (18) BKL_ISEN6
EN (4) — VSYNC (19) BKL_VSYNC_R
GND_SW (1), GND_S (9), GND_L (15), THRM PAD (25)

SMBUS_PCH_CLK R9753 0 5% 1/16W MF-LF 402
SMBUS_PCH_DATA R9757 0 5% 1/16W MF-LF 402
BKL_ISET
BKL_SCL
BKL_SDA
LVDS_BKL_PWM_RC
TP_BKL_FAULT
BKLT_EN
PPBUS_S0_LCDBKLT_PWR
R9731 301K 1% 1/16W MF-LF 402
NO STUFF C9723 0.1UF 10% 25V X5R 402
R9715 100K 1% 1/16W MF-LF 402
(EEPROM should set EN_I_RES=1)
R9714 16.2K 1% 1/16W MF-LF 402 — I_LED=23.2Ma, I_LED=369/Riset
R9716 90.9K 1% 1/16W MF-LF 402 — Fpwm=9.62KHZ, details in spec
R9704 0 5% 1/16W MF-LF 402
LCD_BKLT_PWM
NO STUFF C9704 33PF 5% 50V CERM 402
R9704 SHOULD BE 47K IF RC FILTER IS USED
R9755 10K 5% 1/16W MF-LF 402
NO STUFF R9754 0 5% 1/16W MF-LF 402
XW9710 SM
BKL_SGND
GMUX_VSYNC

R9717 10.2 0.1% 1/16W TF 402 — LED_RETURN_1
R9718 10.2 0.1% 1/16W TF 402 — LED_RETURN_2
R9719 10.2 0.1% 1/16W TF 402 — LED_RETURN_3
R9720 10.2 0.1% 1/16W TF 402 — LED_RETURN_4
R9721 10.2 0.1% 1/16W TF 402 — LED_RETURN_5
R9722 10.2 0.1% 1/16W TF 402 — LED_RETURN_6
MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.20 MM

SYNC_MASTER=K18_BKLT SYNC_DATE=07/29/2009

PAGE TITLE: LCD BACKLIGHT DRIVER

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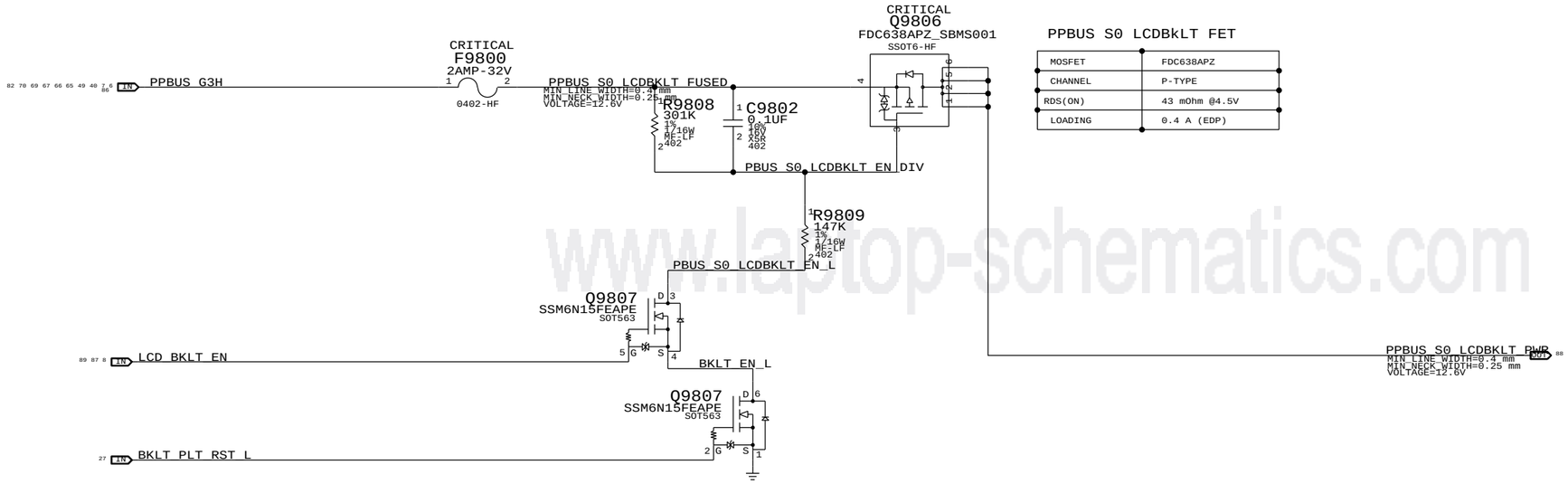
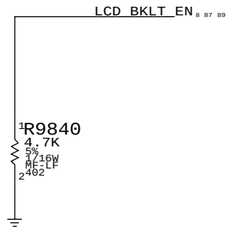


PPBUS S0 LCDBkLT FET	
MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.4 A (EDP)



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SYNC_MASTER=K19_MLB SYNC_DATE=05/29/2009

PAGE TITLE: LCD Backlight Support

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DRAWING NUMBER: <SCH_NUM> SIZE: D

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SYNC_MASTER=K18_POWER SYNC_DATE=06/10/2009

PAGE TITLE: Misc Power Supplies

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Calpella SFF DG (DG-407364_v1.5), Section 2.8

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: Calpella SFF DG (DG-407364_v1.5), Section 2.1 and Table 4-184.

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	9 18
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	9 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	9 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	9 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	9 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	9 18
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	9 18
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	9 18
	CPU_50S	CPU_AGTL	FDI_INT	9 18
CPU_PECI	CPU_50S	PCIE	CPU_PECI	10 20
FSB_CPURST_L	CPU_50S	CPU_AGTL	FSB_CPURST_L	10 25
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	10 18
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	10 18 31
CPU_VTT_S0_PGOOD	CPU_50S	CPU_AGTL	CPUVTTS0_PGOOD	10 70
XDP_XPU_PWRGOOD	CPU_50S	CPU_ITP	XDP_CPUPWRGD	10 25
XDP_DBRESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L	10 25 27
XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_PRDY_L	10 25
XDP_PREQ_L	CPU_50S	CPU_ITP	XDP_PREQ_L	10 25
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<0>	10 46
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<1>	10 46
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP0	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP1	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP2	10
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..0>	8 9 25
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	10
	CPU_50S	CPU_AGTL	TP_CPU_VTT_SELECT	8 12
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 46 68
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 20 25
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 20 46
FSB_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_CPU_P	10 20
FSB_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_CPU_N	10 20
FSB_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_ITP_P	10 25
FSB_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_ITP_N	10 25
PCIE_CLK100M_CPU	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_CPU_P	10 17
PCIE_CLK100M_CPU	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_CPU_N	10 17
	CPU_55S	CPU_8MIL	CPU_PSI_L	12 15 68
PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	12 15 68
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
	CPU_27P4S	CPU_COMP	CPU_PEG_RBIAS	9
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP3	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP2	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP1	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP0	10
XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	25
XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO	25
XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	10 25
XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	10 25
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	10 25
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<6..0>	10 25
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7>	10 25
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	25
	CPU_55S	CPU_8MIL	CPU_VID<6..0>	8 12 15
	CPU_50S	CPU_AGTL	CPUIMVP_IMON	12 50 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	12 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	12 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VTTSENSE_P	12 70
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VTTSENSE_N	12 70
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	GFX_VSENSE_P	13 69
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	GFX_VSENSE_N	13 69
	CPU_55S	CPU_8MIL	GFX_VID<6..0>	8 13
PM_DPRSLPVR	CPU_50S	CPU_AGTL	GFX_DPRSLPVR	13 69
	CPU_50S	CPU_AGTL	GFX_VR_EN	13 69
	CPU_50S	CPU_AGTL	GFXIMVP_IMON	13 69
	PCIE_85D	PCIE	PEG_R2D_P<15..0>	74
	PCIE_85D	PCIE	PEG_R2D_N<15..0>	74
PEG_R2D	PCIE_85D	PCIE	PEG_R2D_C_P<15..0>	8 9 74
	PCIE_85D	PCIE	PEG_R2D_C_N<15..0>	8 74
PEG_D2R	PCIE_85D	PCIE	PEG_D2R_P<15..0>	8 9 74
	PCIE_85D	PCIE	PEG_D2R_N<15..0>	8 74
	PCIE_85D	PCIE	PEG_D2R_C_P<15..0>	74
	PCIE_85D	PCIE	PEG_D2R_C_N<15..0>	74

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3:
DQ/DM signals should be matched within 0.508mm of associated DQS pair.
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-12.7mm] and [CLK+25.4mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-12.7mm] to [CLK+0.0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to SODIMM pad is 139.7mm, from procesor ball to SODIMM pad is 114.3mm.

SOURCE: Calpella SFF Platform DG, Rev 1.5 (#407364), Section 2.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0> 11 28
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0> 11 28
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<3..0> 11 28
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<3..0> 11 28
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<3..0> 11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0> 11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0> 11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L 11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L 11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L 11 28
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0> 11 29
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8> 11 29
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16> 11 29
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24> 11 29
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32> 11 28 29
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40> 11 29
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48> 11 29
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56> 11 29
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DM<0> 11 28 29
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DM<1> 11 29
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DM<2> 11 29
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DM<3> 11 29
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DM<4> 11 29
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DM<5> 11 29
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DM<6> 11 29
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DM<7> 11 29
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0> 11 28 29
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0> 11 28 29
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1> 11 29
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1> 11 29
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2> 11 29
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2> 11 29
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3> 11 29
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3> 11 29
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4> 11 29
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4> 11 29
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5> 11 29
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5> 11 29
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6> 11 29
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6> 11 29
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7> 11 29
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7> 11 29
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0> 11 30
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0> 11 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<3..0> 11 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0> 11 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<3..0> 11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0> 11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0> 11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L 11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L 11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L 11 30
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0> 11 29
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8> 11 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16> 11 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24> 11 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32> 11 29 30
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40> 11 29
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48> 11 29
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56> 11 29
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DM<0> 11 29 30
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DM<1> 11 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DM<2> 11 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DM<3> 11 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DM<4> 11 29
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DM<5> 11 29
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DM<6> 11 29
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DM<7> 11 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0> 11 29 30
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0> 11 29 30
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1> 11 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1> 11 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2> 11 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2> 11 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3> 11 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3> 11 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4> 11 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4> 11 29
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5> 11 29
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5> 11 29
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6> 11 29
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6> 11 29
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7> 11 29
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7> 11 29

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_ICOMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DP_ML	DP_85D	DISPLAYPORT	DP_IG_ML_P<3..0>	8 84
DP_ML	DP_85D	DISPLAYPORT	DP_IG_ML_N<3..0>	8 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_P	8 18 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_N	8 18 84
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_P	18 87
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_N	18 87
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_P<2..0>	18 87
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_N<2..0>	18 87
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAP<3>	8 18
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAN<3>	8 18
LVDS_IG_B_CLK	LVDS_85D	LVDS	TP_LVDS_IG_B_CLKP	6 8 18
LVDS_IG_B_CLK	LVDS_85D	LVDS	TP_LVDS_IG_B_CLKN	6 8 18
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_P<2..0>	18 87
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_N<2..0>	18 87
LVDS_IG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_B_DATAP<3>	8 18
LVDS_IG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_B_DATAN<3>	8 18
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P	17 42
	SATA_90D	SATA	SATA_HDD_R2D_C_N	17 42
	SATA_90D	SATA	SATA_HDD_R2D_P	6 42
	SATA_90D	SATA	SATA_HDD_R2D_N	6 42
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P	17 42
	SATA_90D	SATA	SATA_HDD_D2R_N	17 42
	SATA_90D	SATA	SATA_HDD_D2R_C_P	6 42
	SATA_90D	SATA	SATA_HDD_D2R_C_N	6 42
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P	17 42
	SATA_90D	SATA	SATA_ODD_R2D_C_N	17 42
	SATA_90D	SATA	SATA_ODD_R2D_P	6 42
	SATA_90D	SATA	SATA_ODD_R2D_N	6 42
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P	17 42
	SATA_90D	SATA	SATA_ODD_D2R_N	17 42
	SATA_90D	SATA	SATA_ODD_D2R_C_P	6 42
	SATA_90D	SATA	SATA_ODD_D2R_C_N	6 42
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDRV_IN_P	42
	SATA_90D	SATA	SATA_HDD_R2D_RDRV_IN_N	42
	SATA_90D	SATA	SATA_HDD_R2D_RDRV_OUT_P	42
	SATA_90D	SATA	SATA_HDD_R2D_RDRV_OUT_N	42
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDRV_IN_P	42
	SATA_90D	SATA	SATA_HDD_D2R_RDRV_IN_N	42
	SATA_90D	SATA	SATA_HDD_D2R_RDRV_OUT_P	42
	SATA_90D	SATA	SATA_HDD_D2R_RDRV_OUT_N	42
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP	17
USB_HUB1_UP	USB_85D	USB	USB_HUB1_UP_P	19 35
	USB_85D	USB	USB_HUB1_UP_N	19 35
USB_HUB2_UP	USB_85D	USB	USB_HUB2_UP_P	19 36
	USB_85D	USB	USB_HUB2_UP_N	19 36
USB_EXTA	USB_85D	USB	USB_EXTA_P	36 43
	USB_85D	USB	USB_EXTA_N	36 43
USB_EXTB	USB_85D	USB	USB_EXTB_P	35 43
	USB_85D	USB	USB_EXTB_N	35 43
USB_EXTC	USB_85D	USB	USB_EXTC_P	8 35
	USB_85D	USB	USB_EXTC_N	8 35
USB_EXTD	USB_85D	USB	USB_EXTD_P	
	USB_85D	USB	USB_EXTD_N	
USB_MINI	USB_85D	USB	USB_MINI_P	
	USB_85D	USB	USB_MINI_N	
USB_WM	USB_85D	USB	USB_WM_P	
	USB_85D	USB	USB_WM_N	
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P	6 33
	USB_85D	USB	USB_CAMERA_CONN_N	6 33
USB_BT	USB_85D	USB	USB_BT_P	33 36
	USB_85D	USB	USB_BT_N	33 36
USB_TPAD	USB_85D	USB	USB_TPAD_P	36 53
	USB_85D	USB	USB_TPAD_N	36 53
USB_IR	USB_85D	USB	USB_IR_P	35 44
	USB_85D	USB	USB_IR_N	35 44
USB_SDCARD	USB_85D	USB	USB_SDCARD_P	8 34 36
	USB_85D	USB	USB_SDCARD_N	8 34 36
USB_BRCRYPT	USB_85D	USB	USB_BRCRYPT_P	19 101
	USB_85D	USB	USB_BRCRYPT_N	19 101
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	19
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	17 26
PCH_CLK100M_PCH	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	17 26
	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_PCH_P	17 26
	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_PCH_N	17 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	17 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	17 26
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	17 26
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	17 26
	CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	17 26
	CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN	17 27
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_P	10 17
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_N	10 17

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
LPC_AD	LPC_50S	LPC	LPC_AD<3..0>	6 17 45 47 87
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	6 17 45 47 87
LPC_RESET_L	LPC_50S	LPC	LPCPLUS_RESET_L	6 27 47 87
MCP_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	19 27
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	27 45
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 27 47
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	17 25 26 28 30 32 42 47 48 63 88
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	17 25 26 28 30 32 42 47 48 63 88
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	17 48
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	17 48
SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK	17 48
SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA	17 48
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	17 58
	HDA_50S	HDA	HDA_BIT_CLK_R	17
HDA_SYNC	HDA_50S	HDA	HDA_SYNC	17 58
	HDA_50S	HDA	HDA_SYNC_R	17
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	17
	HDA_50S	HDA	HDA_RST_L	17 58
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	17 58
	HDA_50S	HDA	AUD_SDI_R	58
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	17 58
	HDA_50S	HDA	HDA_SDOUT_R	17
PM_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	18 46
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	17 47
	SPI_55S	SPI	SPI_CLK	47
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	17 47
	SPI_55S	SPI	SPI_MOSI	47
SPI_MISO	SPI_55S	SPI	SPI_MISO	17 47
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	17 47
	SPI_55S	SPI	SPI_CS0_L	47
	PCIE_85D	PCIE	PCIE_ENET_R2D_P	37
	PCIE_85D	PCIE	PCIE_ENET_R2D_N	37
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	17 37
	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	17 37
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	17 37
	PCIE_85D	PCIE	PCIE_ENET_D2R_N	17 37
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P	37
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N	37
	PCIE_85D	PCIE	PCIE_AP_R2D_P	6 33
	PCIE_85D	PCIE	PCIE_AP_R2D_N	6 33
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	17 33
	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	17 33
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	6 17 33
	PCIE_85D	PCIE	PCIE_AP_D2R_N	6 17 33
	PCIE_85D	PCIE	PCIE_FW_R2D_P	39
	PCIE_85D	PCIE	PCIE_FW_R2D_N	39
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	17 39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	17 39
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_P	17 39
	PCIE_85D	PCIE	PCIE_FW_D2R_N	17 39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	39
PCIE_AP_D2R	PCIE_85D	PCIE	CONN_PCIE_AP_D2R_P	
	PCIE_85D	PCIE	CONN_PCIE_AP_D2R_N	
PCIE_AP_R2D	PCIE_85D	PCIE	CONN_PCIE_AP_R2D_P	
	PCIE_85D	PCIE	CONN_PCIE_AP_R2D_N	
MCP_PE0_REFCLK	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	17 74
	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	17 74
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	17 37
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	17 37
MCP_PE1_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	17 33
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	17 33
MCP_PE2_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	17 39
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	17 39
MCP_PE3_REFCLK	CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARD_P	8 17
	CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARD_N	8 17
123	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<1>	6 20
123	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<2>	6 20
123	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<5>	6 20
123	CPU_27P4S	CPU_COMP	TP_PCH_VSS_NCTF<7>	20
123	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<9>	6 20 94
124	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<9>	6 20 94
124	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<11>	6 20
124	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<12>	6 20
124	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<15>	6 20
124	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<17>	6 20
124	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<19>	6 20
124	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<21>	6 20
124	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<22>	20
124	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<25>	6 20
124	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<27>	6 20
125	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<29>	6 20

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CAESAR II (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

CAESAR II (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI 27 37
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO 27 37
	ENET_50S	ENET_3X	ENET_RESET_L 27 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0> 37 38
	ENET_100D	ENET_MDI	ENET_MDI_N<3..0> 37 38

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAP	6 39 41
FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAN	39 41
FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBP	6 39 41
FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBN	6 39 41
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_P	39 40 41
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_N	39 40 41
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_P	39 40 41
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_N	39 40 41

Port 2 Not Used

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL 6 33 45 48 54
SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA 6 33 45 48 54
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL 45 48 51
SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA 45 48 51
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL 45 48 51 81
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA 45 48 51 81
SMBUS_SMC_BSA_SCL	SMB_50S	SMB	SMBUS_SMC_BSA_SCL 6 45 48 64 65
SMBUS_SMC_BSA_SDA	SMB_50S	SMB	SMBUS_SMC_BSA_SDA 6 45 48 64 65
SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL 45 48 56
SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA 45 48 56

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P 65
	1TO1_DIFFPAIR		CHGR_CSI_N 65
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P 65
	1TO1_DIFFPAIR		CHGR_CSO_N 65

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GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R55SE	*	=55_OHM_SE	=40_OHM_SE	0.095 MM	12.7 MM	=STANDARD	=STANDARD
GDDR3_40SE	*	=40_OHM_SE	=40_OHM_SE	0.095 MM	=40_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.095 MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 0.127 mm. Pairs should be within 0.508mm of entire channel.
DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
Max length of LVDS/DisplayPort/TMDS traces: 13 inches.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FB_A_CLK	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<0>
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<0>
FB_B_CLK	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<1>
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<1>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<1..0>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<12..6>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_BA<2..0>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_RAS_L
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_UCAS_L
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_WE_L
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_UCKE
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_LCKE
U20G FB_AB_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_A_LCS0_L
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_DRAM_RST
FB_A_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_LMA<5..2>
FB_B_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_UMA<5..2>
FB_A_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<0>
FB_A_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<1>
FB_A_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<2>
FB_A_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<3>
FB_A_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<0>
FB_A_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<1>
FB_A_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<2>
FB_A_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<3>
FB_A_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<7..0>
FB_A_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<15..8>
FB_A_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<23..16>
FB_A_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<31..24>
FB_A_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<0>
FB_A_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<1>
FB_A_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<2>
FB_A_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<3>
FB_B_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<4>
FB_B_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<5>
FB_B_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<6>
FB_B_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<7>
FB_B_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<4>
FB_B_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<5>
FB_B_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<6>
FB_B_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<7>
FB_B_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<39..32>
FB_B_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<47..40>
FB_B_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<55..48>
FB_B_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<63..56>
FB_B_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<4>
FB_B_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<5>
FB_B_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<6>
FB_B_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<7>

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FB_C_CLK	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<0>
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<0>
FB_D_CLK	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<1>
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<1>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<1..0>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<12..6>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_BA<2..0>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_RAS_L
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_UCAS_L
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_WE_L
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_UCKE
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_LCKE
U20G FB_CD_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_B_LCS0_L
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_DRAM_RST
FB_C_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_LMA<5..2>
FB_D_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_UMA<5..2>
FB_C_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<0>
FB_C_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<1>
FB_C_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<2>
FB_C_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<3>
FB_C_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<0>
FB_C_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<1>
FB_C_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<2>
FB_C_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<3>
FB_C_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<7..0>
FB_C_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<15..8>
FB_C_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<23..16>
FB_C_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<31..24>
FB_C_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<0>
FB_C_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<1>
FB_C_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<2>
FB_C_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<3>
FB_D_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<4>
FB_D_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<5>
FB_D_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<6>
FB_D_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<7>
FB_D_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<4>
FB_D_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<5>
FB_D_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<6>
FB_D_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<7>
FB_D_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<39..32>
FB_D_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<47..40>
FB_D_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<55..48>
FB_D_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<63..56>
FB_D_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<4>
FB_D_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<5>
FB_D_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<6>
FB_D_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<7>
U21G FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_LCAS_L
U21G FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_LCAS_L

G96 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
(CK505_DATAB1)	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M
CK505_CLK27MSS	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_P
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_N
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_P<2..0>
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_N<2..0>
U20F LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_P<3>
U20F LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_N<3>
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_P<2..0>
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_N<2..0>
U20H LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_P<3>
U20H LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_N<3>
DP_ML	DP_85D	DISPLAYPORT	DP_EG_ML_P<3..0>
DP_ML	DP_85D	DISPLAYPORT	DP_EG_ML_N<3..0>
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_P
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_N
	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_C_P
	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_C_N

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
J14G LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_P
J14G LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_N
J15G LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_P<2..0>
J15G LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_N<2..0>
J15F LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_P
J15F LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_N
J20F LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_P<2..0>
J20G LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_N<2..0>
J13F	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_P
J13F	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_N
J13H	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_P
J13G	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_N
J13D	LVDS_85D	LVDS	LVDS_CONN_A_CLK_P
J13J	LVDS_85D	LVDS	LVDS_CONN_A_CLK_N
J13C	LVDS_85D	LVDS	LVDS_CONN_A_DATA_P<2..0>
J13D	LVDS_85D	LVDS	LVDS_CONN_A_DATA_N<2..0>
J13H	LVDS_85D	LVDS	LVDS_CONN_B_CLK_P
J13J	LVDS_85D	LVDS	LVDS_CONN_B_CLK_N
J13K	LVDS_85D	LVDS	LVDS_CONN_B_DATA_P<2..0>
J13L	LVDS_85D	LVDS	LVDS_CONN_B_DATA_N<2..0>
J15J DP_ML	DP_85D	DISPLAYPORT	DP_ML_C_P<3..0>
J15G	DP_85D	DISPLAYPORT	DP_ML_C_N<3..0>
J15J DP_ML	DP_85D	DISPLAYPORT	DP_ML_P<3..0>
J15J	DP_85D	DISPLAYPORT	DP_ML_N<3..0>
J20G DP_ML	DP_85D	DISPLAYPORT	DP_ML_CONN_P<3..0>
J20J	DP_85D	DISPLAYPORT	DP_ML_CONN_N<3..0>
J15H DP_AUX_CH	DP_85D	DISPLAYPORT	DP_AUX_CH_C_P
J15H DP_AUX_CH	DP_85D	DISPLAYPORT	DP_AUX_CH_C_N

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_85D	BGA	LVDS_85D
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

K18 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	ENET_100D	ENETCONN	ENETCONN_P<3..0> 38
	ENET_100D	ENETCONN	ENETCONN_N<3..0> 38
	SATA_90D	SATA	SATA_ODD_R2D_UF_P 42
	SATA_90D	SATA	SATA_ODD_R2D_UF_N 42
	SATA_90D	SATA	SATA_ODD_D2R_UF_P 42
	SATA_90D	SATA	SATA_ODD_D2R_UF_N 42
	SATA_90D	SATA	SATA_HDD_D2R_UF_P 42
	SATA_90D	SATA	SATA_HDD_D2R_UF_N 42
	SATA_90D	SATA	SATA_HDD_R2D_UF_P 42
	SATA_90D	SATA	SATA_HDD_R2D_UF_N 42
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P 51
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N 51
U28 SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P 9 51
U28	THERM_1TO1_55S	THERM	CPU_THERMD_N 9 51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P 51
	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N 51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P 51 79 80
	THERM_1TO1_55S	THERM	GPU_TDIODE_N 51 79 80
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVTTISNS_R_N 50
	SENSE_1TO1_55S	SENSE	CPUVTTISNS_R_P 50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVTTS0_CS_N 50 70
	SENSE_1TO1_55S	SENSE	CPUVTTS0_CS_P 50 70
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	DDRISNS_R_N 50
	SENSE_1TO1_55S	SENSE	DDRISNS_R_P 50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFXIMVP_CS_N 69
	SENSE_1TO1_55S	SENSE	GFXIMVP_CS_P 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFXIMVP_CS_R_N 50 69
	SENSE_1TO1_55S	SENSE	GFXIMVP_CS_R_P 50 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFX_ISNS_R_N 50
	SENSE_1TO1_55S	SENSE	GFX_ISNS_R_P 50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUISENS_N 50
	SENSE_1TO1_55S	SENSE	GPUISENS_P 50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_N 50 67
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_P 50 67
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N 99
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N 99
U241 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P 99
U256	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P 99
U252 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_N 56
U253	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_P 56
U255 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPU_N 49
U255	SENSE_1TO1_55S	SENSE	ISNS_CPU_P 49
U250 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_N
U250	SENSE_1TO1_55S	SENSE	ISNS_HDD_P
U251 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_N 56
U251	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_P 56
U281 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N
U281	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P
U280 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_N
U280	SENSE_1TO1_55S	SENSE	ISNS_ODD_P
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_N 56
	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_P 56
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_N 50
	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_P 50
U292 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_R_N 50
U293	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_R_P 50

K18 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
PCIE CLK100M AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P 6 33
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N 6 33
	1TO1_DIFFPAIR		CHGR_CSI_R_P 65
	1TO1_DIFFPAIR		CHGR_CSI_R_N 65
	1TO1_DIFFPAIR		CHGR_CSO_R_P 49 65
	1TO1_DIFFPAIR		CHGR_CSO_R_N 49 65
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_P 43
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_N 43
(USB_EXTA)	USB_85D	USB	USB2_LT1_P 6 43
(USB_EXTA)	USB_85D	USB	USB2_LT1_N 6 43
	USB_85D	USB	CONN_USB2_BT_P 6 33
	USB_85D	USB	CONN_USB2_BT_N 6 33
	USB_85D	USB	USB_LT2_P 6 43
	USB_85D	USB	USB_LT2_N 6 43
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_P 84
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_N 84
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P 6 61 62
	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N 6 61 62
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P 6 61 62
	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N 6 61 62
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_P 6 61 62
	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_N 6 61 62
	USB_85D	USB	USB_TPAD_R_P 53
	USB_85D	USB	USB_TPAD_R_N 53
		SB_POWER	PP3V3_S5 6 7 17 18 19 20 21 23 27 31 35 57 60 71 72 73 83 85 88 91 92 93
		SB_POWER	PP3V3_S0 6 7 17 18 19 20 21 23 27 28 30 34 37 40 42 54 56 57 58 59 64
		SB_POWER	PP1V5_S3RS0 6 7 13 16 31 42 72 73 83 88 89 93
		GND	GND

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K18 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.095 MM			
37_OHM_SE	*	Y	0.155 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL9,ISL10	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL9,ISL10	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.090 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.090 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.

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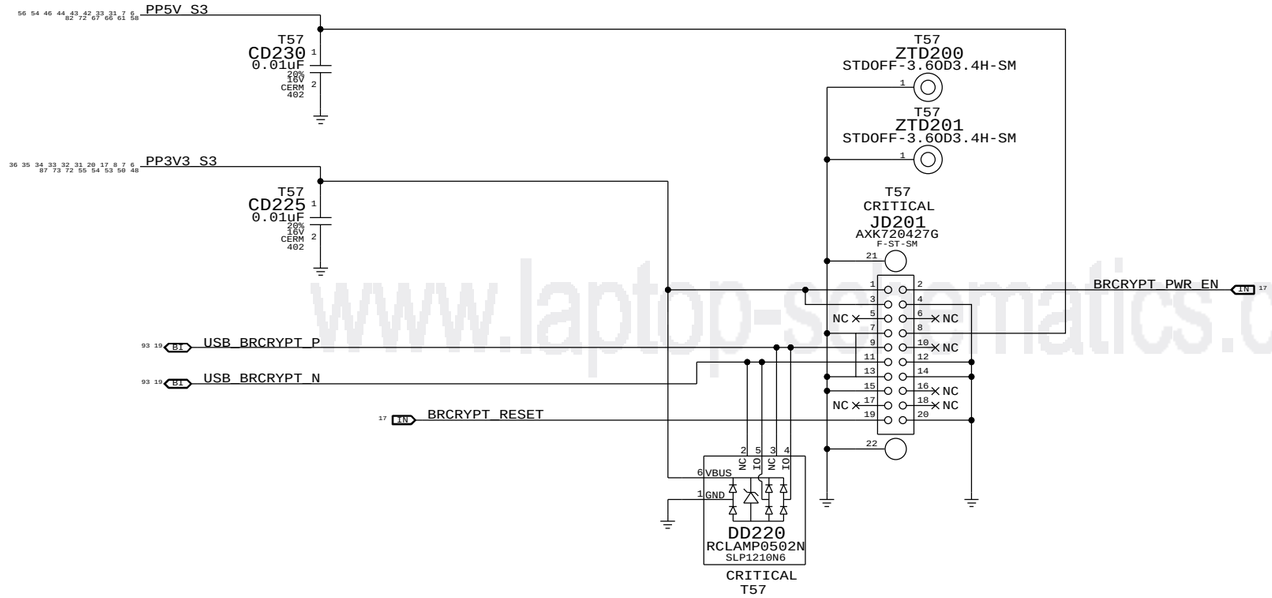

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