

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
			2010-07-23

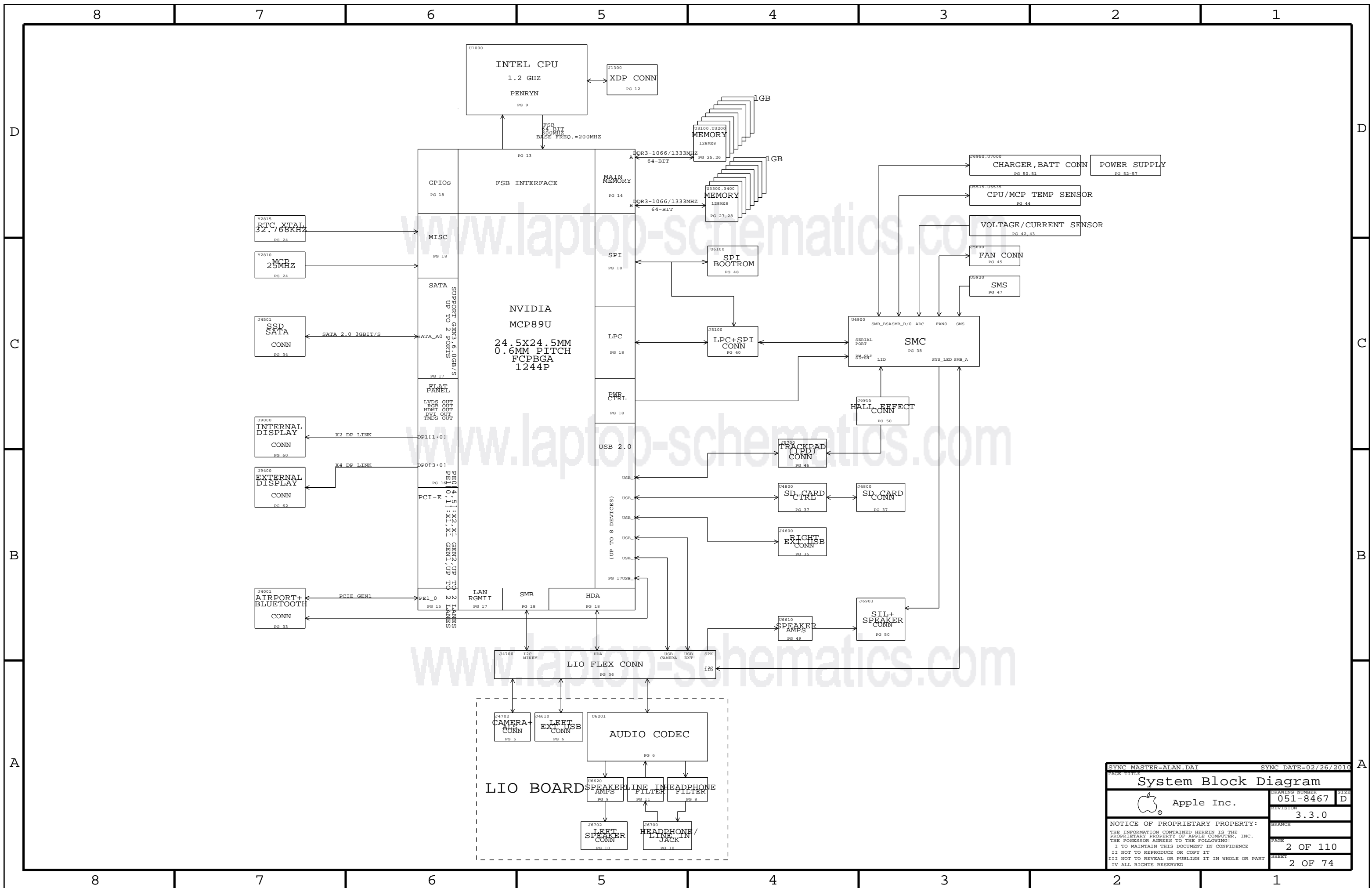
SCHEMATIC, MLB, "Moonlight"

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07/23/2010

DRAWING TITLE		SCHEM, MLB, K16	
Apple Inc.	DRAWING NUMBER	051-8467	SIZE
	REVISION	3.3.0	D
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SYNC MASTER=ALAN.DAI		SYNC DATE=02/26/2010	
System Block Diagram			
Apple Inc.		DRAWING NUMBER	SIZE
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DRAM CFG CHART

VENDOR	CFG 0	CFG 1
HYNIX	0	0
SAMSUNG	0	1
MICRON	1	0
ELPIDA	1	1

SIZE	CFG 2	DIE REV	CFG 3
2GB	0	A	0
4GB	1	B	1

BOM Variants on following page

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3820	1	IC,MCP89U-A01,24,598K24,59M,1244FCBGA	U1400	CRITICAL	MCP89U:A01
337S3868	1	IC,MCP89U-A02,24,598K24,59M,1244FCBGA	U1400	CRITICAL	MCP89U:A02
337S3938	1	IC,MCP89U-A03,24,598K24,59M,1244FCBGA	U1400	CRITICAL	MCP89U:A03

333S0552	4	HYNIX,LVDDR3,1GBIT,7.5K11.0	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0552	4	HYNIX,LVDDR3,1GBIT,7.5K11.0	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0552	4	HYNIX,LVDDR3,1GBIT,7.5K11.0	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0552	4	HYNIX,LVDDR3,1GBIT,7.5K11.0	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0553	4	SAMSUNG,LVDDR3,1GBIT,7.5K11.0	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0553	4	SAMSUNG,LVDDR3,1GBIT,7.5K11.0	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0553	4	SAMSUNG,LVDDR3,1GBIT,7.5K11.0	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0553	4	SAMSUNG,LVDDR3,1GBIT,7.5K11.0	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0554	4	MICRON,LVDDR3,1GBIT,8K11.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0554	4	MICRON,LVDDR3,1GBIT,8K11.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0554	4	MICRON,LVDDR3,1GBIT,8K11.5	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0554	4	MICRON,LVDDR3,1GBIT,8K11.5	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0565	4	ELPIDA,LVDDR3,1GBIT,7.5K10.6	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_2GB
333S0565	4	ELPIDA,LVDDR3,1GBIT,7.5K10.6	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_2GB
333S0565	4	ELPIDA,LVDDR3,1GBIT,7.5K10.6	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:ELPIDA_2GB
333S0565	4	ELPIDA,LVDDR3,1GBIT,7.5K10.6	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:ELPIDA_2GB
333S0566	4	ELPIDA,LVDDR3,1GBIT,7.5K10.6	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0566	4	ELPIDA,LVDDR3,2GBIT,7.5K10.6	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0566	4	ELPIDA,LVDDR3,2GBIT,7.5K10.6	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0566	4	ELPIDA,LVDDR3,2GBIT,7.5K10.6	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0555	4	HYNIX,LVDDR3,2GBIT,9K11.1	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0555	4	HYNIX,LVDDR3,2GBIT,9K11.1	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0555	4	HYNIX,LVDDR3,2GBIT,9K11.1	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0555	4	HYNIX,LVDDR3,2GBIT,9K11.1	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0556	4	SAMSUNG,LVDDR3,2GBIT,7.5K11.0	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0556	4	SAMSUNG,LVDDR3,2GBIT,7.5K11.0	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0556	4	SAMSUNG,LVDDR3,2GBIT,7.5K11.0	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0556	4	SAMSUNG,LVDDR3,2GBIT,7.5K11.0	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0557	4	MICRON,LVDDR3,2GBIT,9K11.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:MICRON_4GB
333S0557	4	MICRON,LVDDR3,2GBIT,9K11.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:MICRON_4GB
333S0557	4	MICRON,LVDDR3,2GBIT,9K11.5	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:MICRON_4GB
333S0557	4	MICRON,LVDDR3,2GBIT,9K11.5	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:MICRON_4GB
353S2392	1	IC,ISL6259,BATCHCHARGER,4X4MM,QFN28	U7000	CRITICAL	ISL6259_SCREENED:NO
353S2929	1	IC,ISL6259,BATCHCHARGER,3x,4C4MM,QFN28	U7000	CRITICAL	ISL6259_SCREENED:YES

BOM Groups

BOM GROUP	BOM OPTIONS
K16_COMMON	COMMON,ALTERNATE,PROJ:K16,K16_MISC,MCP89U:A03,K16_DEBUG:ENG,K16_PROGPARTS,SPI:41MHZ,LVDDR3:YES,WLAN_PCTL:HW,IPD_5V:S5_INT,IPD_3V3:S5
K16_MISC	DP_ESD,DP_PWR:SMC,VFRQ:SLPS3,HVDDLDO:FIXED,MCPHVD:P2V5,MCPPLL_R:REG,SOPGOOD_BJT,ISL6259_SCREENED:YES,DP12C:SMC
K16_PROGPARTS	BOOTROM:UNLOCKED,SMC:PROG
K16_DEVEL:ENG	BKLT:ENG,BMON:ENG,XDP_CONN,LPCPLUS,VREFMRGN:YES,EFI_DEBUG,SOPGOOD_ISL,MCPPLL_LDO,S3_S0_LED
K16_DEVEL:PVT	LPCPLUS
K16_DEBUG:ENG	DEVEL_BOM,SMC_DEBUG:YES,XDP
K16_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,BMON:PROD,SMC_DEBUG:YES,XDP,VREFMRGN:NO
K16_DEBUG:PROD	BKLT:PROD,BMON:PROD,SMC_DEBUG:YES,XDP,VREFMRGN:NO
DDR3:HYNIX_2GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:HYNIX_2GB
DDR3:SAMSUNG_2GB	DRAM_CFG0:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_2GB
DDR3:MICRON_2GB	DRAM_CFG0:H,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:MICRON_2GB
DDR3:ELPIDA_2GB	DRAM_CFG0:H,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:ELPIDA_2GB
DDR3:ELPIDA_4GB	DRAM_CFG0:H,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:ELPIDA_4GB
DDR3:HYNIX_4GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:SAMSUNG_4GB	DRAM_CFG0:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:MICRON_4GB	DRAM_CFG0:H,DRAM_CFG1:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:MICRON_4GB
CAPS:SS	SS_CAP_2_2UF,SS_CAP_10UF,SS_CAP_1UF,SS_CAP_22UF
CAPS:MU	MU_CAP_2_2UF,MU_CAP_10UF,MU_CAP_1UF,MU_CAP_22UF
CAPS:TY	TY_CAP_2_2UF,TY_CAP_10UF,TY_CAP_1UF,TY_CAP_22UF

Programmable Parts

338S0563	1	IC,SMC,HS8/2117,9X9MM,TLP,HF	U4900	CRITICAL	SMC:BLANK
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM:BLANK

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
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138S0681	138S0638		ALL	TAIYO YUDEN AS ALTERNATE
152S0874	152S0516		ALL	WALAYERS AS ALTERNATE
152S0847	152S0586		ALL	WALAYERS AS ALTERNATE
353S2987	353S2988	HVDDLDO:FIXED	ALL	T987126 ALTERNATE FOR U2590
104S0023	104S0018		ALL	CYTRIC/DIAE AS ALTERNATE
107S0139	107S0075		ALL	CYTRIC AS ALTERNATE
138S0671	138S0673		ALL	TAIYO AS ALTERNATE
155S0578	155S0367		ALL	TAIYO AS ALTERNATE
376S0926	376S0610		ALL	FAIRCHILD AS ALTERNATE
155S0457	155S0329		ALL	WALAYERS AS ALTERNATE
377S0107	377S0066		ALL	ON SEMI AS ALTERNATE

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8467	1	SCHEM,MLB,K16	SCH	CRITICAL	
820-2838	1	PCBF,MLB,K16	PCB	CRITICAL	

PAGE TITLE		SYNC DATE=12/11/2009	
BOM Configuration			
Apple Inc.		DRAWING NUMBER	051-8467
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-1070	PCBA,MLB,1.86GHZ HY 2GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCWQ,CAPS:MU,DDR3:HYNIX_2GB
639-0837	PCBA,MLB,1.86GHZ,HY 2GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXW,CAPS:SS,DDR3:HYNIX_2GB
639-1096	PCBA,MLB,1.86GHZ HY 2GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXN,CAPS:TY,DDR3:HYNIX_2GB
639-1101	PCBA,MLB,1.86GHZ HY 4GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXV,CAPS:MU,DDR3:HYNIX_4GB
639-1098	PCBA,MLB,1.86GHZ HY 4GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXQ,CAPS:SS,DDR3:HYNIX_4GB
639-1068	PCBA,MLB,1.86GHZ HY 4GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCWN,CAPS:TY,DDR3:HYNIX_4GB
639-1083	PCBA,MLB,1.86GHZ MI 2GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCX6,CAPS:MU,DDR3:MICRON_2GB
639-1078	PCBA,MLB,1.86GHZ MI 2GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCX1,CAPS:SS,DDR3:MICRON_2GB
639-1090	PCBA,MLB,1.86GHZ MI 2GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXG,CAPS:TY,DDR3:MICRON_2GB
639-1088	PCBA,MLB,1.86GHZ MI 4GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXD,CAPS:MU,DDR3:MICRON_4GB
639-1067	PCBA,MLB,1.86GHZ MI 4GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCWM,CAPS:SS,DDR3:MICRON_4GB
639-1077	PCBA,MLB,1.86GHZ MI 4GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCX0,CAPS:TY,DDR3:MICRON_4GB
639-1080	PCBA,MLB,1.86GHZ SA 2GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCX3,CAPS:MU,DDR3:SAMSUNG_2GB
639-1095	PCBA,MLB,1.86GHZ SA 2GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXM,CAPS:SS,DDR3:SAMSUNG_2GB
639-1071	PCBA,MLB,1.86GHZ SA 2GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCWR,CAPS:TY,DDR3:SAMSUNG_2GB
639-1097	PCBA,MLB,1.86GHZ SA 4GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXP,CAPS:MU,DDR3:SAMSUNG_4GB
639-1084	PCBA,MLB,1.86GHZ SA 4GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCX7,CAPS:SS,DDR3:SAMSUNG_4GB
639-1091	PCBA,MLB,1.86GHZ SA 4GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXH,CAPS:TY,DDR3:SAMSUNG_4GB
639-1092	PCBA,MLB,2.13GHZ HY 2GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXJ,CAPS:MU,DDR3:HYNIX_2GB
639-1082	PCBA,MLB,2.13GHZ,HY 2GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCX5,CAPS:SS,DDR3:HYNIX_2GB
639-1085	PCBA,MLB,2.13GHZ HY 2GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCX8,CAPS:TY,DDR3:HYNIX_2GB
639-1089	PCBA,MLB,2.13GHZ HY 4GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXF,CAPS:MU,DDR3:HYNIX_4GB
639-1075	PCBA,MLB,2.13GHZ HY 4GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWX,CAPS:SS,DDR3:HYNIX_4GB
639-1079	PCBA,MLB,2.13GHZ HY 4GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCX2,CAPS:TY,DDR3:HYNIX_4GB
639-1099	PCBA,MLB,2.13GHZ MI 2GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXR,CAPS:MU,DDR3:MICRON_2GB
639-1087	PCBA,MLB,2.13GHZ MI 2GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXC,CAPS:SS,DDR3:MICRON_2GB
639-1069	PCBA,MLB,2.13GHZ MI 2GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWP,CAPS:TY,DDR3:MICRON_2GB
639-1100	PCBA,MLB,2.13GHZ MI 4GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXT,CAPS:MU,DDR3:MICRON_4GB
639-1093	PCBA,MLB,2.13GHZ MI 4GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXK,CAPS:SS,DDR3:MICRON_4GB
639-1076	PCBA,MLB,2.13GHZ MI 4GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWY,CAPS:TY,DDR3:MICRON_4GB
639-1074	PCBA,MLB,2.13GHZ SA 2GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWW,CAPS:MU,DDR3:SAMSUNG_2GB
639-1072	PCBA,MLB,2.13GHZ SA 2GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWT,CAPS:SS,DDR3:SAMSUNG_2GB
639-1086	PCBA,MLB,2.13GHZ SA 2GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCX9,CAPS:TY,DDR3:SAMSUNG_2GB
639-1073	PCBA,MLB,2.13GHZ SA 4GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWV,CAPS:MU,DDR3:SAMSUNG_4GB
639-1081	PCBA,MLB,2.13GHZ SA 4GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCX4,CAPS:SS,DDR3:SAMSUNG_4GB
639-1094	PCBA,MLB,2.13GHZ SA 4GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXL,CAPS:TY,DDR3:SAMSUNG_4GB
639-1450	PCBA,MLB,1.86GHZ EL 2GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG4W,CAPS:MU,DDR3:ELPIDA_2GB
639-1451	PCBA,MLB,1.86GHZ EL 2GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG4Y,CAPS:SS,DDR3:ELPIDA_2GB
639-1455	PCBA,MLB,1.86GHZ EL 2GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG53,CAPS:TY,DDR3:ELPIDA_2GB
639-1453	PCBA,MLB,2.13GHZ EL 2GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG51,CAPS:MU,DDR3:ELPIDA_2GB
639-1454	PCBA,MLB,2.13GHZ EL 2GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG52,CAPS:SS,DDR3:ELPIDA_2GB
639-1452	PCBA,MLB,2.13GHZ EL 2GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG50,CAPS:TY,DDR3:ELPIDA_2GB
639-1458	PCBA,MLB,1.86GHZ EL 4GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG5P,CAPS:MU,DDR3:ELPIDA_4GB
639-1463	PCBA,MLB,1.86GHZ EL 4GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG5W,CAPS:SS,DDR3:ELPIDA_4GB
639-1460	PCBA,MLB,1.86GHZ EL 4GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG5T,CAPS:TY,DDR3:ELPIDA_4GB
639-1462	PCBA,MLB,2.13GHZ EL 4GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG5Q,CAPS:MU,DDR3:ELPIDA_4GB
639-1459	PCBA,MLB,2.13GHZ EL 4GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG5V,CAPS:SS,DDR3:ELPIDA_4GB
639-1461	PCBA,MLB,2.13GHZ EL 4GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG5R,CAPS:TY,DDR3:ELPIDA_4GB
607-6915	CMN PTS,PCBA,MLB,K16	K16_COMMON
085-1327	K16 MLB DEVELOPMENT BOM	K16_DEVEL:ENG

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWM]	CRITICAL	EEEE:DCWM
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWN]	CRITICAL	EEEE:DCWN
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWP]	CRITICAL	EEEE:DCWP
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWQ]	CRITICAL	EEEE:DCWQ
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCLR]	CRITICAL	EEEE:DCWR
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWT]	CRITICAL	EEEE:DCWT
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWV]	CRITICAL	EEEE:DCWV
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWW]	CRITICAL	EEEE:DCWW
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWX]	CRITICAL	EEEE:DCWX
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWY]	CRITICAL	EEEE:DCWY
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX0]	CRITICAL	EEEE:DCX0
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX1]	CRITICAL	EEEE:DCX1
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX2]	CRITICAL	EEEE:DCX2
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX3]	CRITICAL	EEEE:DCX3
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX4]	CRITICAL	EEEE:DCX4
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX5]	CRITICAL	EEEE:DCX5
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX6]	CRITICAL	EEEE:DCX6
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX7]	CRITICAL	EEEE:DCX7
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX8]	CRITICAL	EEEE:DCX8
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX9]	CRITICAL	EEEE:DCX9
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXC]	CRITICAL	EEEE:DCXC
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXD]	CRITICAL	EEEE:DCXD
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXF]	CRITICAL	EEEE:DCXF
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXG]	CRITICAL	EEEE:DCXG
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXH]	CRITICAL	EEEE:DCXH
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXJ]	CRITICAL	EEEE:DCXJ
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXK]	CRITICAL	EEEE:DCXK
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXL]	CRITICAL	EEEE:DCXL
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXM]	CRITICAL	EEEE:DCXM
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXN]	CRITICAL	EEEE:DCXN
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXP]	CRITICAL	EEEE:DCXP
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXQ]	CRITICAL	EEEE:DCXQ
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCLR]	CRITICAL	EEEE:DCXR
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXT]	CRITICAL	EEEE:DCXT
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXV]	CRITICAL	EEEE:DCXV
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXW]	CRITICAL	EEEE:DCXW
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG4W]	CRITICAL	EEEE:DG4W
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG4Y]	CRITICAL	EEEE:DG4Y
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG53]	CRITICAL	EEEE:DG53
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG51]	CRITICAL	EEEE:DG51
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG52]	CRITICAL	EEEE:DG52
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG50]	CRITICAL	EEEE:DG50
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5P]	CRITICAL	EEEE:DG5P
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5W]	CRITICAL	EEEE:DG5W
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5T]	CRITICAL	EEEE:DG5T
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5Q]	CRITICAL	EEEE:DG5Q
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5V]	CRITICAL	EEEE:DG5V
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5R]	CRITICAL	EEEE:DG5R

SAMSUNG

MURATA

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0632	1	CAP, 2.2UF, 6.3V, 20%, 0402	C4807	CRITICAL	SS_CAP_2_2UF	138S0633	1	CAP, 2.2UF, 6.3V, 20%, 0402	C4807	CRITICAL	MU_CAP_2_2UF	138S0634	1	CAP, 2.2UF, 6.3V, 20%, 0402	C4807	CRITICAL	TY_CAP_2_2UF

K16-Specific BOM Tables

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3751	1	PDC,SLGAB,PRQ,1.86,17M,1066,ED,6M,BGA	U1000	CRITICAL	CPU:1.86GHZ
337S3758	1	PDC,SLGEQ,PRQ,2.13,17M,1066,ED,6M,BGA	U1000	CRITICAL	CPU:2.13GHZ
341T0276	1	IC ASSY,SMC EXTERNAL,K16	U4900	CRITICAL	SMC:PROG
341T0275	1	IC ASSY,EPI UNLOCKED,K16	U6100	CRITICAL	BOOTROM:UNLOCKED
341S2785	1	IC EPI ROM,FVT,LOCKED,K16	U6100	CRITICAL	BOOTROM:LOCKED

Sub-BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-1327	1	K16 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
607-6915	1	CMN PTS,PCBA,MLB,K16	CMNPTS	CRITICAL	K16_CMNPTS

SYNC MASTER=N/A SYNC DATE=N/A

Apple Inc.

051-8467

3.3.0

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Revision History

Proto 0 (ECO #0000876215, v1.0.0, P4 change #210266, 03/16/2010)

v1.1.0 (P4 change #211399, 03/24/2010)

- MCP:
 - 7742015 - Added RC to DDC pass FETs to avoid glitch (pp. 7, 93).
 - 7788138 - Added feedback divider and BOM tables for more HVDD LDOs (pp. 4, 25).
- SMC:
 - 7761747 - Added resistors to connect TCON to SMC or MCP SMBus (pp. 4, 52, 90).
 - 7787883 - Added support for DP HPD wake / S4 state (pp. 4, 7, 8, 19, 49, 50, 78, 94).
- SMS:
 - 7765466 - Added S3 pull-up to SMS_INT_L to prevent leakage path (pp. 50, 59).
- General:
 - 7769139 - Unstuffed SMS circuit (pg. 4).
 - 7787897 - Property/page fixes to reduce CheckPlus warnings/errors (pp. 7, 8, 12, 17, 74, 93, 108).

v1.2.0 (P4 change #211839, 03/26/2010)

- USB:
 - 7796626 - Changed port switch from TPS2052B to TPS2069 (pg. 46).
- SMC:
 - 7787883 - Added PLACE_NEAR property on R5022 to avoid stub (pg. 50).
- SMBus:
 - 7761747 - Added TCON I2C nets to FUNC_TEST list for J9000 (pg. 7).
- Power:
 - 7796648 - Changed DP and LCD power from PP3V3_S3 to PP3V3_S5 (pp. 8, 90).
 - 7796658 - Changed backlight driver to E00 version (pg. 97).
- BOM:
 - 7796661 - Set up primary & alternate for power supply FET (pp. 4, 72).
 - 7796654 - Consolidated SSM6N15FE to SSM6N37FE (pg. 48).
 - 7796658 - Changed RCs on some SMC analog inputs (pg. 54).
 - 7796683 - Stuffed RC on backlight driver PWM input (pg. 97).
- General:
 - 7796631 - Sorted BOM variants for easier verification (pg. 5).
 - 7796631 - Cosmetic clean-up (pg. 76).

v1.3.0 (P4 change #212050, 03/26/2010)

- SMBus:
 - 7761747 - Added isolation FET and unstuffed series R's on TCON I2C for now (pp. 4, 90, 108).
- Power Supply:
 - 7796661 - Removed alternate FET, made some FETs primary to other APN (pp. 4, 72, 73, 76).
 - 7798425 - R/C value changes for 3.42V G3Hot power supply (pg. 69).
 - 7798399 - R/C value changes for 5V/3.3V power supply (pg. 72).
 - 7800179 - R value changes for CPU VCore power supply (pg. 74).
 - 7798445 - R value changes for 0.9V S5 power supply (pg. 77).
 - 7796658 - Changed backlight driver back to non-E00 version (pp. 4, 97).
- BOM:
 - 7796658 - Added alternates for two caps per GSM and removed unused alternates (pg. 4).
 - 7798399 - Consolidated 100pF caps (pp. 74, 75).

v1.4.0 (P4 change #212757, 03/31/2010)

- MCP SPI:
 - 7809733 - Changed strapping to select 62.5MHz SPI bus frequency (pg. 4).
- SMBus:
 - 7796631 - Added XDP connection to SMBus aliases page (pp. 13, 52).
 - 7808530 - Changed SMC 'MGMT' SMBus pull-ups from 4.7K to 2K (pg. 52).
 - 7761747 - Documented SMBus addresses for panel (pg. 52).
- SD Card:
 - 7800415 - Changed SD Card discharge R to more standard value (pg. 48).
- Power Supplies:
 - 7803283 - Changed 5V S3 regulator output from 5.02V to 5.12V nominal (pg. 72).
 - 7809760 - Stuffed C9799 and clarified tables/BOMOPTIONS around these parts (pg. 97).

Proto 1 (ECO #0000884508, v2.0.0, P4 change #212783, 03/31/2010)

v2.1.0 (P4 change #??????, ??/??/2010)


- BOM:
 - 7796658 - Changed OMITs to OMIT_TABLES (pp. 10-11, 14-20, 26, 31-36, 49, 61).

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NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

SYNC MASTER=N/A		SYNC DATE=N/A	
Revision History			
 Apple Inc.	DRAWING NUMBER	051-8467	SIZE
	REVISION	3.3.0	D
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		SHEET	6 OF 74

Functional Test Points

NO_TEST Nets

J4001: AirPort / BT Connector

FUNC_TEST	Signal	Pin
TRUE	PP3V3 WLAN_F	7 34 40
TRUE	WIFI_EVENT_L	34 39 40
TRUE	PCIE AP R2D N	34 68
TRUE	PCIE AP R2D P	34 68
TRUE	PCIE CLK100M AP N	16 34 68
TRUE	PCIE CLK100M AP P	16 34 68
TRUE	USB BT P	18 34 69
TRUE	USB BT N	18 34 69
TRUE	PCIE AP D2R P	16 34 68
TRUE	PCIE AP D2R N	16 34 68
TRUE	PCIE_WAKE_L	16 34
TRUE	AP_RESET_CONN_L	34
TRUE	AP_CLKREQ_O_L	34
TRUE	=PP3V3_S3_BT	8 34

(Need 5 TPs)

J5600: Fan Connector

FUNC_TEST	Signal	Pin
TRUE	PP5V_S0	7 8 58
TRUE	FAN_RT_TACH	46
TRUE	FAN_RT_PWM	46

(Need to add 1 GND TP)

FSB Signals (Covered via CPU/MCP JTAG)

NO_TEST	Signal	Pin
TRUE	FSB_A_L<35..3>	10 14 66
TRUE	FSB_ADS_L	10 14 66
TRUE	FSB_ADSTB_L<1..0>	10 14 66
TRUE	FSB_D_L<63..0>	10 14 66
TRUE	FSB_DINV_L<3..0>	10 14 66
TRUE	FSB_DSTB_L_N<3..0>	10 14 66
TRUE	FSB_DSTB_L_P<3..0>	10 14 66
TRUE	FSB_HIT_L	10 14 66
TRUE	FSB_HITM_L	10 14 66
TRUE	FSB_LOCK_L	10 14 66
TRUE	FSB_REQ_L<4..0>	10 14 66

J4501: SATA SSD Connector

FUNC_TEST	Signal	Pin
TRUE	PP3V3_S0_HDD_R	7 35
TRUE	SATA_HDD_D2R_C_P	35 68
TRUE	SATA_HDD_D2R_C_N	35 68
TRUE	SATA_HDD_R2D_N	35 68
TRUE	SATA_HDD_R2D_P	35 68
TRUE	SMC_HDD_QQB_TEMP	35 39
TRUE	SMC_HDD_TEMP_CTL	35 39

(Need 5 TPs)

J5700: IPD Flex Connector

FUNC_TEST	Signal	Pin
TRUE	=PP5V_S3_TPAD	8 57
TRUE	=PP3V42_G3H_TPAD	8 47
TRUE	=PP3V3_S3_TPAD	8 47
TRUE	USB_TPAD_CONN_P	47 72
TRUE	USB_TPAD_CONN_N	47 72
TRUE	=I2C_TPAD_SDA	42 47
TRUE	=I2C_TPAD_SCL	42 47
TRUE	SMC_ONOFF_L	39 40 47
TRUE	SMC_LID	7 37 39 40 47
TRUE	SMC_TPAD_RST_L	40 47

(Need to add 5 GND TPs)

J6900: DC-In Connector

FUNC_TEST	Signal	Pin
TRUE	=PP18V5_DCIN_CONN	8 50
TRUE	=PP5V_S3_LIO_CONN	8 50

(Need 6 TPs)

J6903: Speaker Connector

FUNC_TEST	Signal	Pin
TRUE	SPKRAMP_R_P_OUT	49 50
TRUE	SPKRAMP_R_N_OUT	49 50

J6950: Battery Connector

FUNC_TEST	Signal	Pin
TRUE	PPVBAT_G3H_CONN	50 51
TRUE	SMBUS_SMC_BSA_SCL	42 71
TRUE	SMBUS_SMC_BSA_SDA	42 71
TRUE	SYS_DETECT_L	50

(Need to add 4 GND TPs near J6950 and 1 for shield)

J9000: Internal DP Connector

FUNC_TEST	Signal	Pin
TRUE	PPVOUT_SW_LCDBKLT	7 43 60 63
TRUE	PP3V3_SW_LCD	60
TRUE	=I2C_TCON_SDA	42 60
TRUE	LED_RETURN_6	60 63
TRUE	LED_RETURN_5	60 63
TRUE	LED_RETURN_4	60 63
TRUE	LED_RETURN_3	60 63
TRUE	LED_RETURN_2	60 63
TRUE	LED_RETURN_1	60 63
TRUE	DP_INT_HPD_CONN	60
TRUE	DP_INT_AUX_CH_C_N	60 72
TRUE	DP_INT_AUX_CH_C_P	60 72
TRUE	DP_INT_ML_F_P<0>	60 72
TRUE	DP_INT_ML_F_N<0>	60 72
TRUE	DP_INT_ML_F_P<1>	60 72
TRUE	DP_INT_ML_F_N<1>	60 72
TRUE	=I2C_TCON_SCL	42 60

(Need 2 TPs)

Misc Voltages & Control Signals

FUNC_TEST	Signal	Pin
TRUE	PPVOUT_SW_LCDBKLT	7 43 60 63
TRUE	PPDCIN_S5_S5	8
TRUE	PPBUS_G3H	8 43 50
TRUE	PPBUS_G3H_ISNS	8
TRUE	PP5V_S3	8
TRUE	PP5V_S3_RTUSB_A_F	36
TRUE	PP5V_S0	7 8 58
TRUE	PP3V42_G3H	8
TRUE	PP3V3_S5	8 58 72
TRUE	PP3V3_SW_DPPWR	62
TRUE	PP3V3_S3	8
TRUE	PP3V3_WLAN_F	7 34 40
TRUE	PP3V3_S0	8 58 72
TRUE	PP3V3_S0_HDD_R	7 35
TRUE	PP3V3_ENET	8
TRUE	PP1V5R1V35_S3	8 72
TRUE	PP1V5_S0	8 58 72
TRUE	PP1V05_S0	8 58
TRUE	PP1V05_S0_MCP_PLL_UF	8
TRUE	PP0V9_S5	8
TRUE	PP0V9_ENET	8
TRUE	PPVCORE_S0_CPU	8 43
TRUE	PPVCORE_S0_MCP	8 43

(Need to add 27 GND TPs)

J4700: LIO Connector

FUNC_TEST	Signal	Pin
TRUE	=PP3V42_G3H_ONEWIRE	8 37
TRUE	=PP3V3_S0_AUDIO	8 37
TRUE	=PP1V8R1V5_S0_AUDIO	8 37
TRUE	SYS_ONEWIRE	37 39
TRUE	SMC_BC_ACOK	9 37 39 40
TRUE	=USB_PWR_EN	36 37 58
TRUE	SMC_LID	7 37 39 40 47
TRUE	=I2C_LIO_SDA	37 42
TRUE	=I2C_LIO_SCL	37 42
TRUE	=I2C_MIKEY_SCL	37 42
TRUE	=I2C_MIKEY_SDA	37 42
TRUE	AUD_IPHS_SWITCH_EN	19 37
TRUE	AUD_IP_PERIPHERAL_DET	17 37
TRUE	AUD_I2C_INT_L	19 37
TRUE	AUD_GPIO_3	37 49
TRUE	SPKRAMP_INR_N	37 49 72
TRUE	SPKRAMP_INR_P	37 49 72
TRUE	USB_EXTD_N	18 37 69
TRUE	USB_EXTD_P	18 37 69
TRUE	USB_CAMERA_N	18 37 69
TRUE	USB_CAMERA_P	18 37 69
TRUE	HDA_SDOUT	19 37 69
TRUE	HDA_BIT_CLK	19 37 69
TRUE	HDA_SDIN0	19 37 69
TRUE	USB_EXTD_OC_L	18 37
TRUE	HDA_RST_L	19 37 69
TRUE	HDA_SYNC	19 37 69

(Need 2 TPs)

J4800: SD Card Connector

FUNC_TEST	Signal	Pin
TRUE	PP3V3_SW_SD_PWR	38
TRUE	SD_CLK	38 70
TRUE	SD_CMD	38 70
TRUE	SD_D<7..0>	38 70
TRUE	SD_CD_L	38
TRUE	SD_WP	38

(Need to add 2 GND TPs)

J5100: LPC+SPI Connector

FUNC_TEST	Signal	Pin
TRUE	=PP3V3_S5_LPCPLUS	8 41
TRUE	=PP5V_S0_LPCPLUS	8 41
TRUE	LPC_AD<3..0>	19 39 41 69
TRUE	SPI_ALT_MOSI	41 69
TRUE	SPI_ALT_MISO	41 69
TRUE	LPC_FRAME_L	19 39 41 69
TRUE	PM_CLKRUN_L	19 39 41
TRUE	SMC_TMS	39 40 41
TRUE	LPCPLUS_RESET_L	25 41
TRUE	SMC_TDO	39 40 41
TRUE	SMC_TRST_L	39 41
TRUE	SMC_MDI	39 41
TRUE	SMC_TX_L	36 39 40 41
TRUE	LPC_CLK33M_LPCPLUS	25 41 69
TRUE	SPIROM_USE_MLB	19 41 68
TRUE	SPI_ALT_CLK	41 69
TRUE	SPI_ALT_CS_L	41 69
TRUE	LPC_SERIRQ	19 39 41
TRUE	LPC_PWRDWN_L	19 39 41
TRUE	SMC_TDI	39 40 41
TRUE	SMC_TCK	39 40 41
TRUE	SMC_RESET_L	39 40 41 51
TRUE	SMC_NMI	39 41
TRUE	SMC_RX_L	36 39 40 41
TRUE	LPCPLUS_GPIO	19 41

(Need to add 6 GND TPs)

SYNC MASTER=(K99_MLB) SYNC DATE=(02/16/2010)

Functional Test / No Test

Apple Inc.

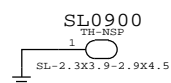
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REVISION: 3.3.0

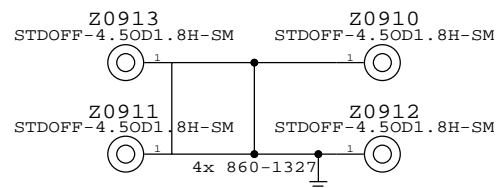
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PAGE: 7 OF 110 SHEET: 7 OF 74

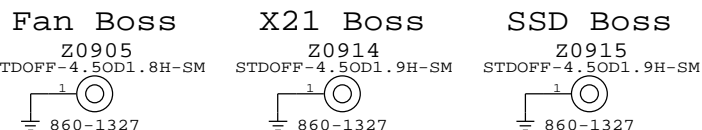
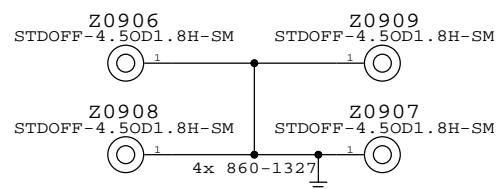
Plated Board Slot



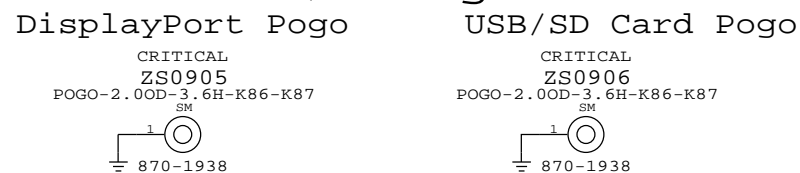
CPU Heat Sink Mounting Bosses



MCP Heat Sink Mounting Bosses

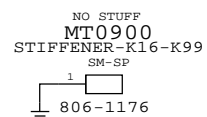


EMI I/O Pogo Pins

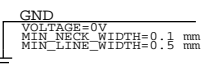


DisplayPort PCB Stiffener

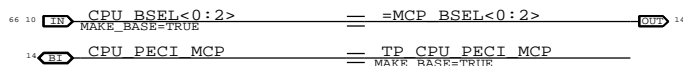
(Provides PCB support for small finger above J9400)



Digital Ground

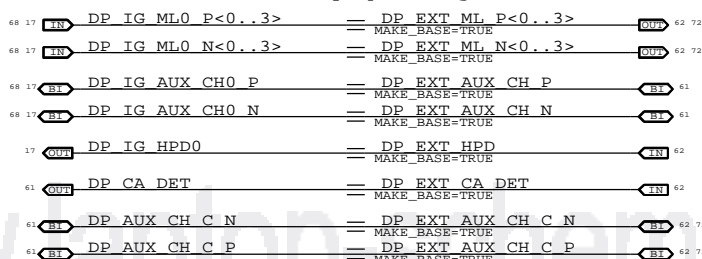


CPU Aliases

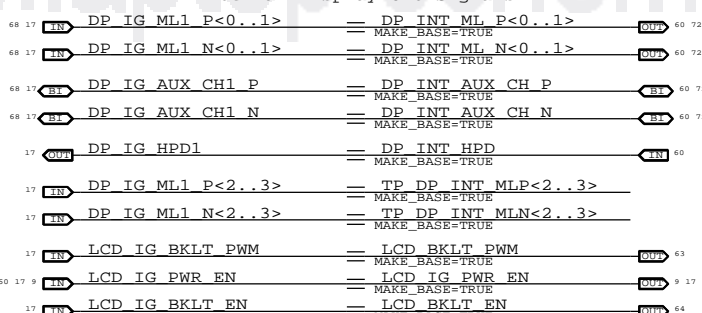


DisplayPort Aliases

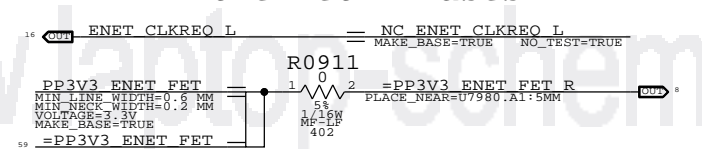
External DisplayPort Signals



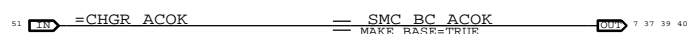
Internal DisplayPort Signals



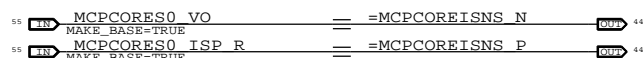
Ethernet Aliases



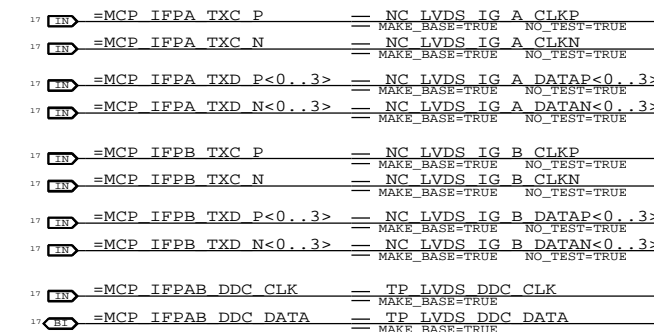
Charger Signal



MCPCOREISNS Signals

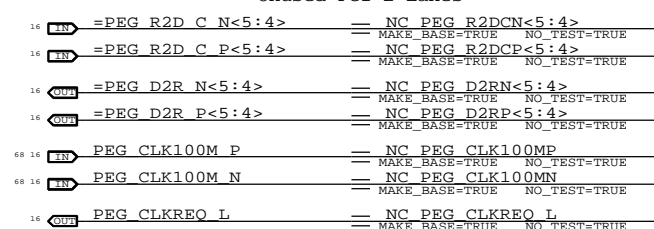


LVDS Aliases



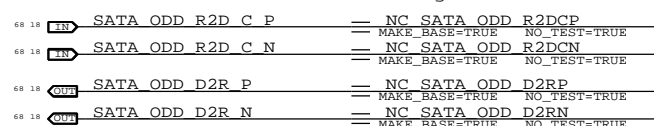
PCI-E Aliases

Unused PCI-E Lanes



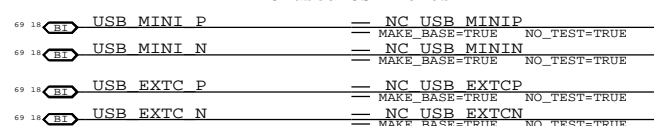
SATA Aliases

Unused SATA ODD Signals

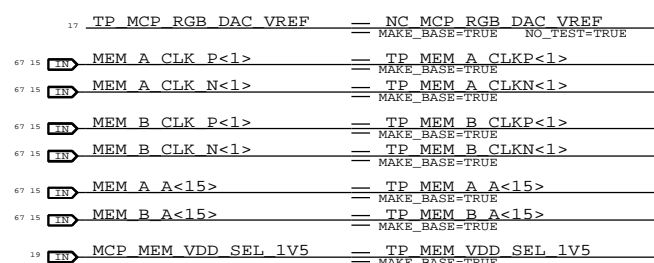


USB Aliases

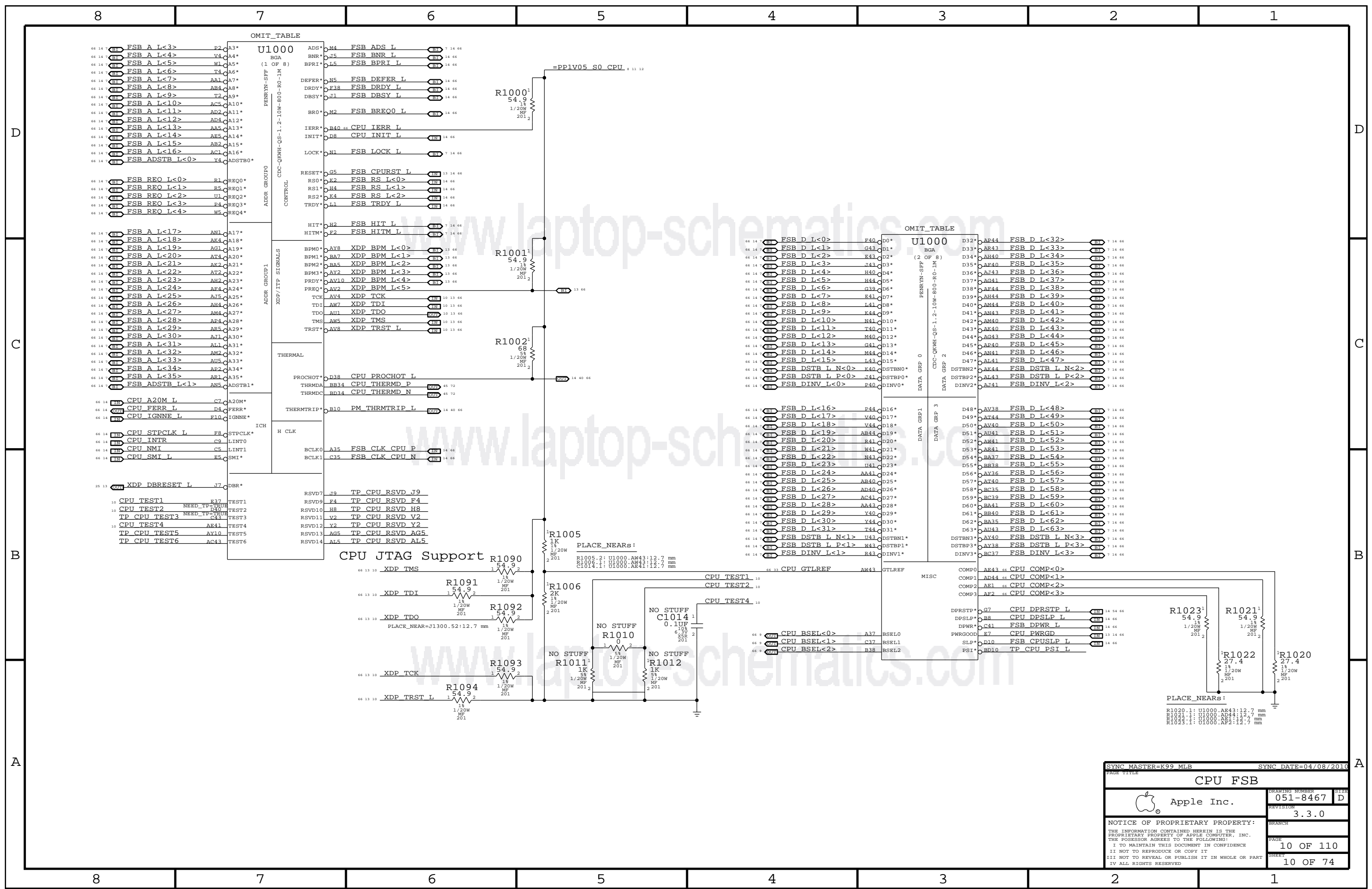
Unused USB Ports



Misc MCP89 Aliases



SYNC MASTER=(MASTER)		SYNC DATE=(MASTER)	
Signal Aliases			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8467	D
		REVISION	
		3.3.0	
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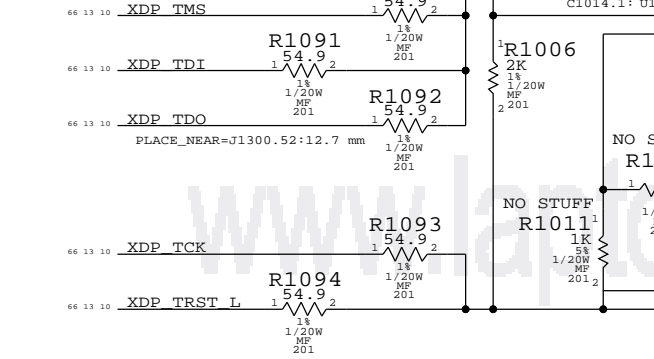


OMIT TABLE

Signal	Pin	Processor Pin
FSB A L<3>	P2	A3*
FSB A L<4>	Y4	A4*
FSB A L<5>	W1	A5*
FSB A L<6>	T4	A6*
FSB A L<7>	AA1	A7*
FSB A L<8>	AB4	A8*
FSB A L<9>	T2	A9*
FSB A L<10>	AC5	A10*
FSB A L<11>	AD2	A11*
FSB A L<12>	AD4	A12*
FSB A L<13>	AA5	A13*
FSB A L<14>	AE5	A14*
FSB A L<15>	AB2	A15*
FSB A L<16>	AC1	A16*
FSB ADSTB L<0>	Y4	ADSTB0*
FSB REQ L<0>	R1	REQ0*
FSB REQ L<1>	R5	REQ1*
FSB REQ L<2>	U1	REQ2*
FSB REQ L<3>	P4	REQ3*
FSB REQ L<4>	W5	REQ4*
FSB A L<17>	AN1	A17*
FSB A L<18>	AK1	A18*
FSB A L<19>	AG1	A19*
FSB A L<20>	AT4	A20*
FSB A L<21>	AK2	A21*
FSB A L<22>	AT2	A22*
FSB A L<23>	AH2	A23*
FSB A L<24>	AF4	A24*
FSB A L<25>	AV5	A25*
FSB A L<26>	AH4	A26*
FSB A L<27>	AM4	A27*
FSB A L<28>	AP4	A28*
FSB A L<29>	AR5	A29*
FSB A L<30>	AT1	A30*
FSB A L<31>	AL1	A31*
FSB A L<32>	AM2	A32*
FSB A L<33>	AU5	A33*
FSB A L<34>	AP2	A34*
FSB A L<35>	AR1	A35*
FSB ADSTB L<1>	AN5	ADSTB1*
CPU A20M L	C7	A20M*
CPU FERR L	D4	FERR*
CPU IGNE L	F10	IGNE*
CPU STPCLK L	F8	STPCLK*
CPU INTR	C9	LINT0*
CPU NMI	C5	LINT1*
CPU SMI L	R5	SMI*
XDP DBRESET L	J7	DBR*
CPU TEST1	E37	TEST1
CPU TEST2	NEED_TP=TRUE D10	TEST2
TP CPU TEST3	NEED_TP=TRUE C13	TEST3
CPU TEST4	AE41	TEST4
TP CPU TEST5	AY10	TEST5
TP CPU TEST6	AC43	TEST6

Signal	Pin	Processor Pin
ADS*	M4	FSB ADS L
BNR*	J5	FSB BNR L
BPRI*	L5	FSB BPRI L
DEFER*	N5	FSB DEFER L
DRDY*	F38	FSB DRDY L
DBSY*	J1	FSB DBSY L
BREQ*	M2	FSB BREQ L
IERR*	B40	CPU IERR L
INIT*	DB8	CPU INIT L
LOCK*	W1	FSB LOCK L
RESET*	G5	FSB CPURST L
RS0*	X2	FSB RS L<0>
RS1*	H4	FSB RS L<1>
RS2*	K4	FSB RS L<2>
TRDY*	L1	FSB TRDY L
HIT*	H2	FSB HIT L
HITM*	F2	FSB HITM L
BPM0*	AY8	XDP BPM L<0>
BPM1*	BA7	XDP BPM L<1>
BPM2*	BA5	XDP BPM L<2>
BPM3*	AY2	XDP BPM L<3>
PRDY*	AV10	XDP BPM L<4>
PREQ*	AV2	XDP BPM L<5>
TCK	AV4	XDP TCK
TDI	AM7	XDP TDI
TDO	AM1	XDP TDO
TMS	AM5	XDP TMS
TRST*	AV8	XDP TRST L
D38	CPU	PROCHOT L
BB34	CPU	THERMD P
BD34	CPU	THERMD N
R10	PM	THRMTRIP L
A35	FSB	CLK CPU P
C35	FSB	CLK CPU N
J9	TP	CPU RSVD J9
F4	TP	CPU RSVD F4
H8	TP	CPU RSVD H8
V2	TP	CPU RSVD V2
Y2	TP	CPU RSVD Y2
AG5	TP	CPU RSVD AG5
AL5	TP	CPU RSVD AL5

CPU JTAG Support



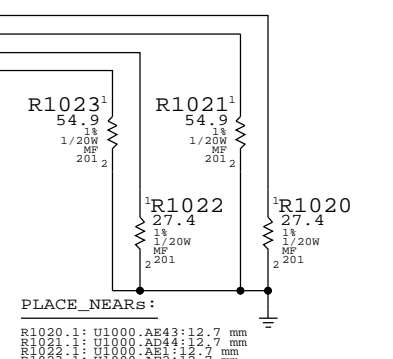
OMIT TABLE

Signal	Pin	Processor Pin
FSB D L<0>	F40	D0*
FSB D L<1>	G43	D1*
FSB D L<2>	E43	D2*
FSB D L<3>	F43	D3*
FSB D L<4>	H40	D4*
FSB D L<5>	H44	D5*
FSB D L<6>	G39	D6*
FSB D L<7>	E41	D7*
FSB D L<8>	L41	D8*
FSB D L<9>	K44	D9*
FSB D L<10>	N41	D10*
FSB D L<11>	T40	D11*
FSB D L<12>	M40	D12*
FSB D L<13>	G41	D13*
FSB D L<14>	M44	D14*
FSB D L<15>	L43	D15*
FSB D L<16>	P44	D16*
FSB D L<17>	V40	D17*
FSB D L<18>	V44	D18*
FSB D L<19>	AB44	D19*
FSB D L<20>	R41	D20*
FSB D L<21>	W41	D21*
FSB D L<22>	N43	D22*
FSB D L<23>	U41	D23*
FSB D L<24>	AA41	D24*
FSB D L<25>	AB40	D25*
FSB D L<26>	AD40	D26*
FSB D L<27>	AC41	D27*
FSB D L<28>	AA43	D28*
FSB D L<29>	Y40	D29*
FSB D L<30>	Y44	D30*
FSB D L<31>	T44	D31*
FSB DSTB L N<0>	K40	DSTBN0*
FSB DSTB L P<0>	J41	DSTBP0*
FSB DSTB L P<1>	W43	DSTBP1*
FSB DINV L<1>	R43	DINV1*

Signal	Pin	Processor Pin
AP44	FSB	D L<32>
AR43	FSB	D L<33>
AH40	FSB	D L<34>
AF40	FSB	D L<35>
AT43	FSB	D L<36>
AG41	FSB	D L<37>
AF44	FSB	D L<38>
AH44	FSB	D L<39>
AM44	FSB	D L<40>
AN43	FSB	D L<41>
AM40	FSB	D L<42>
AK40	FSB	D L<43>
AG43	FSB	D L<44>
AP40	FSB	D L<45>
AN41	FSB	D L<46>
AL41	FSB	D L<47>
AK44	FSB	D L<48>
AT44	FSB	D L<49>
AV40	FSB	D L<50>
AU41	FSB	D L<51>
AW41	FSB	D L<52>
AR41	FSB	D L<53>
BA37	FSB	D L<54>
BB38	FSB	D L<55>
AY36	FSB	D L<56>
AT40	FSB	D L<57>
BC35	FSB	D L<58>
BC39	FSB	D L<59>
BA41	FSB	D L<60>
BB40	FSB	D L<61>
BA35	FSB	D L<62>
AU43	FSB	D L<63>
AY40	FSB	D L<64>
AY38	FSB	D L<65>
BC37	FSB	D L<66>

MISC

Signal	Pin	Processor Pin
AE43	CPU	COMP<0>
AD44	CPU	COMP<1>
AE1	CPU	COMP<2>
AF2	CPU	COMP<3>
G7	CPU	DPRSTP L
B8	CPU	DPSTP L
C41	FSB	DPWR L
E7	CPU	PWRGOOD
D10	FSB	CPUSLP L
BD10	TP	CPU PSI L



SYNC MASTER=K99 MLB SYNC DATE=04/08/2010

CPU FSB

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D

REVISION: 3.3.0

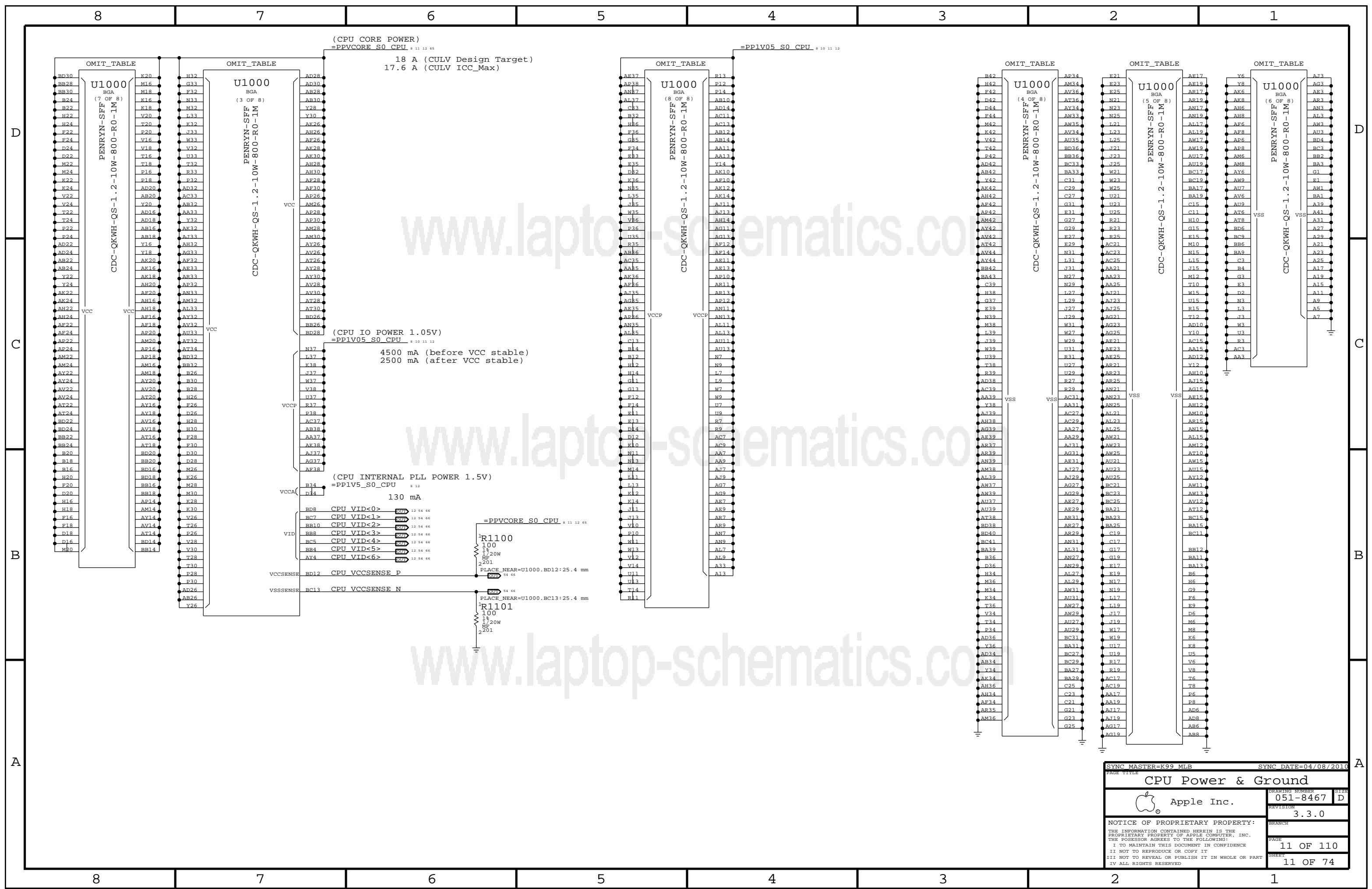
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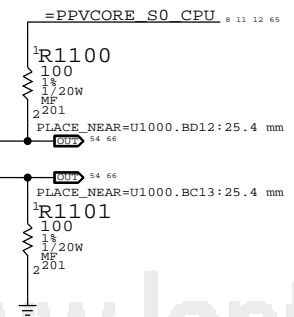


(CPU CORE POWER)
 =PPVCORE_S0_CPU 8 11 12 65
 18 A (CULV Design Target)
 17.6 A (CULV ICC_Max)

=PP1V05_S0_CPU 8 10 11 12

(CPU IO POWER 1.05V)
 =PP1V05_S0_CPU 8 10 11 12
 4500 mA (before VCC stable)
 2500 mA (after VCC stable)

(CPU INTERNAL PLL POWER 1.5V)
 =PP1V5_S0_CPU 8 12
 130 mA

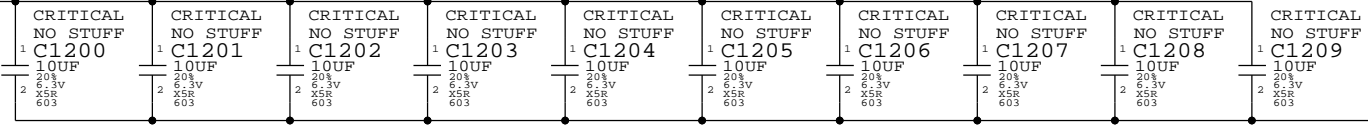


SYNC MASTER=K99_MLB		SYNC DATE=04/08/2010	
CPU Power & Ground			
Apple Inc.		DRAWING NUMBER 051-8467	SIZE D
		REVISION 3.3.0	BRANCH
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		PAGE 11 OF 110	SHEET 11 OF 74

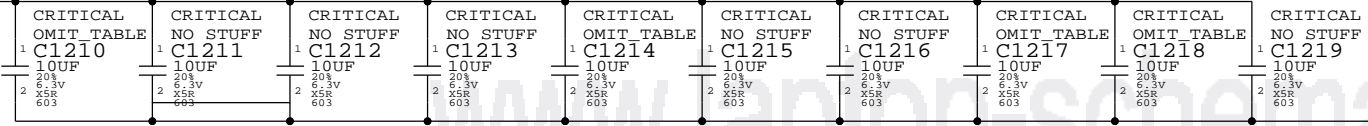
CPU VCORE HF AND BULK DECOUPLING

4x 270uF, 32x 10uF 0603, 28x 2.2uF 0402 + 40x 2.2uF 0402

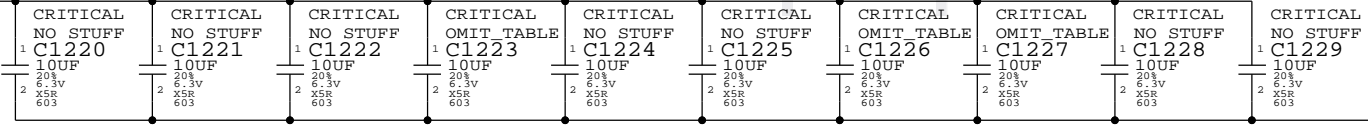
LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU



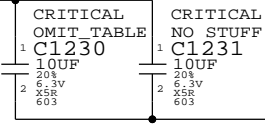
LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU



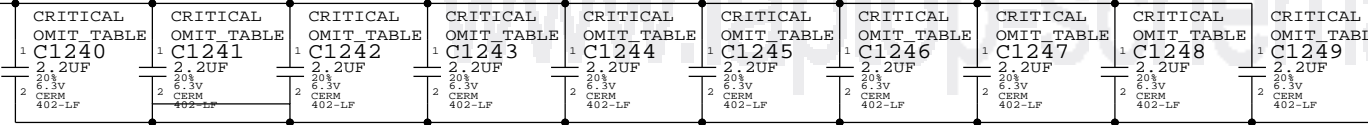
LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU



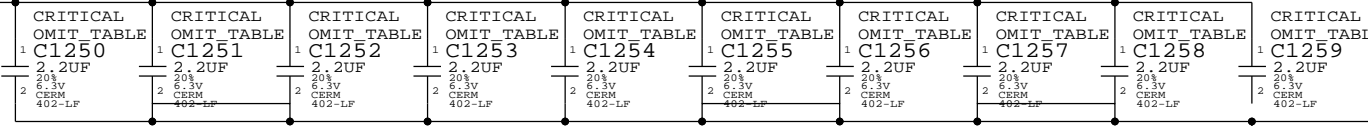
LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU



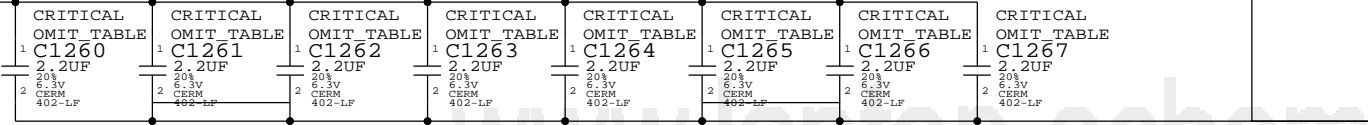
LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU



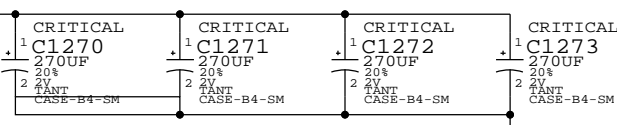
LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU



LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU



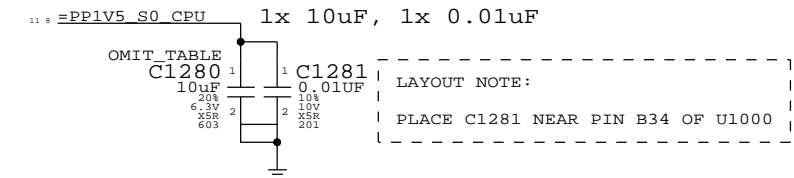
LAYOUT NOTE:
PLACE ON SAME SIDE AS CPU



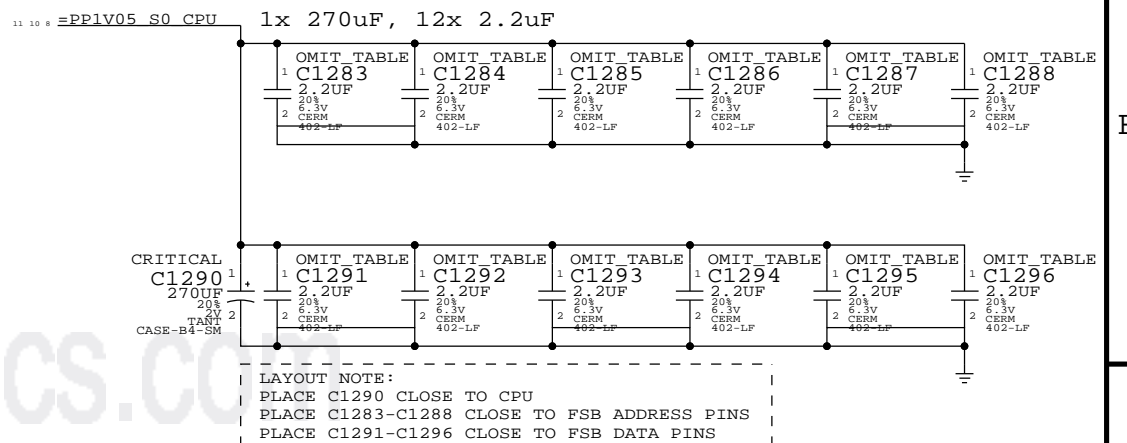
CPU VCORE VID CONNECTIONS

66 54 11 CPU VID<0..6> = IMVP6 VID<0..6>

VCCA (CPU AVdd) DECOUPLING



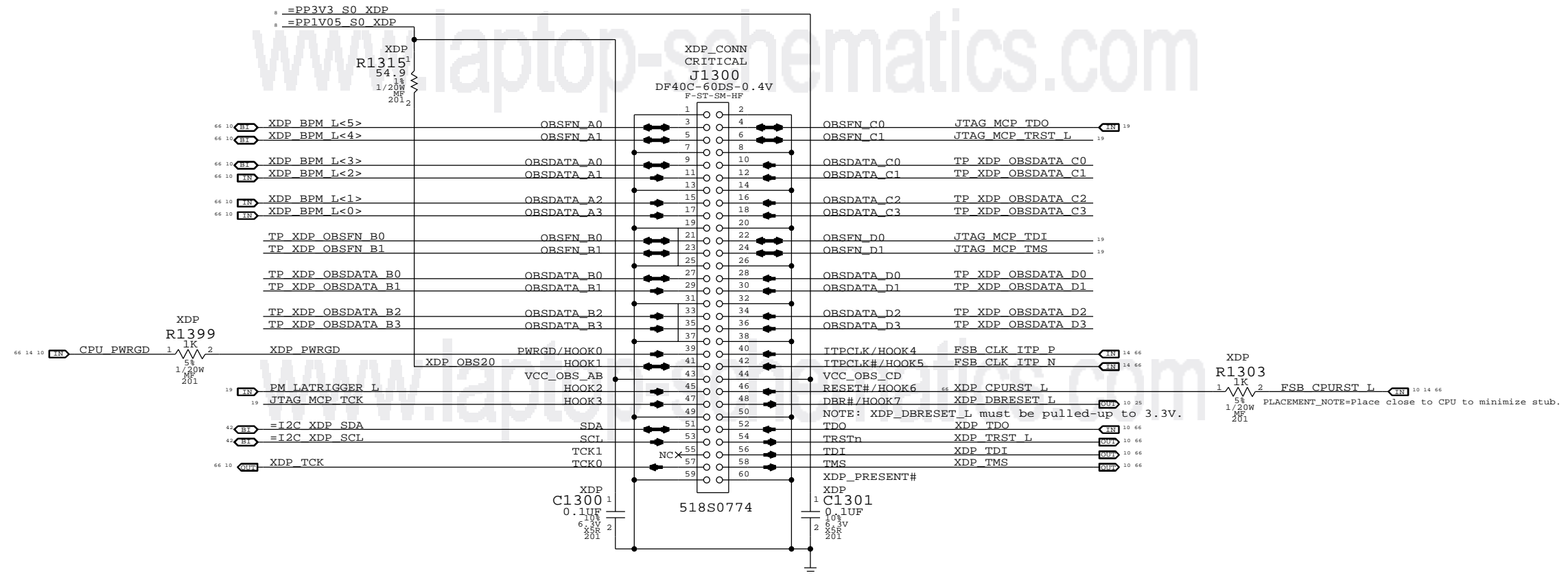
VCCP (CPU I/O) DECOUPLING



PAGE TITLE		SYNC MASTER=(K99 MLB)		SYNC DATE=(02/11/2010)	
CPU Decoupling & VID			DRAWING NUMBER	051-8467	SIZE
Apple Inc.			REVISION	3.3.0	D
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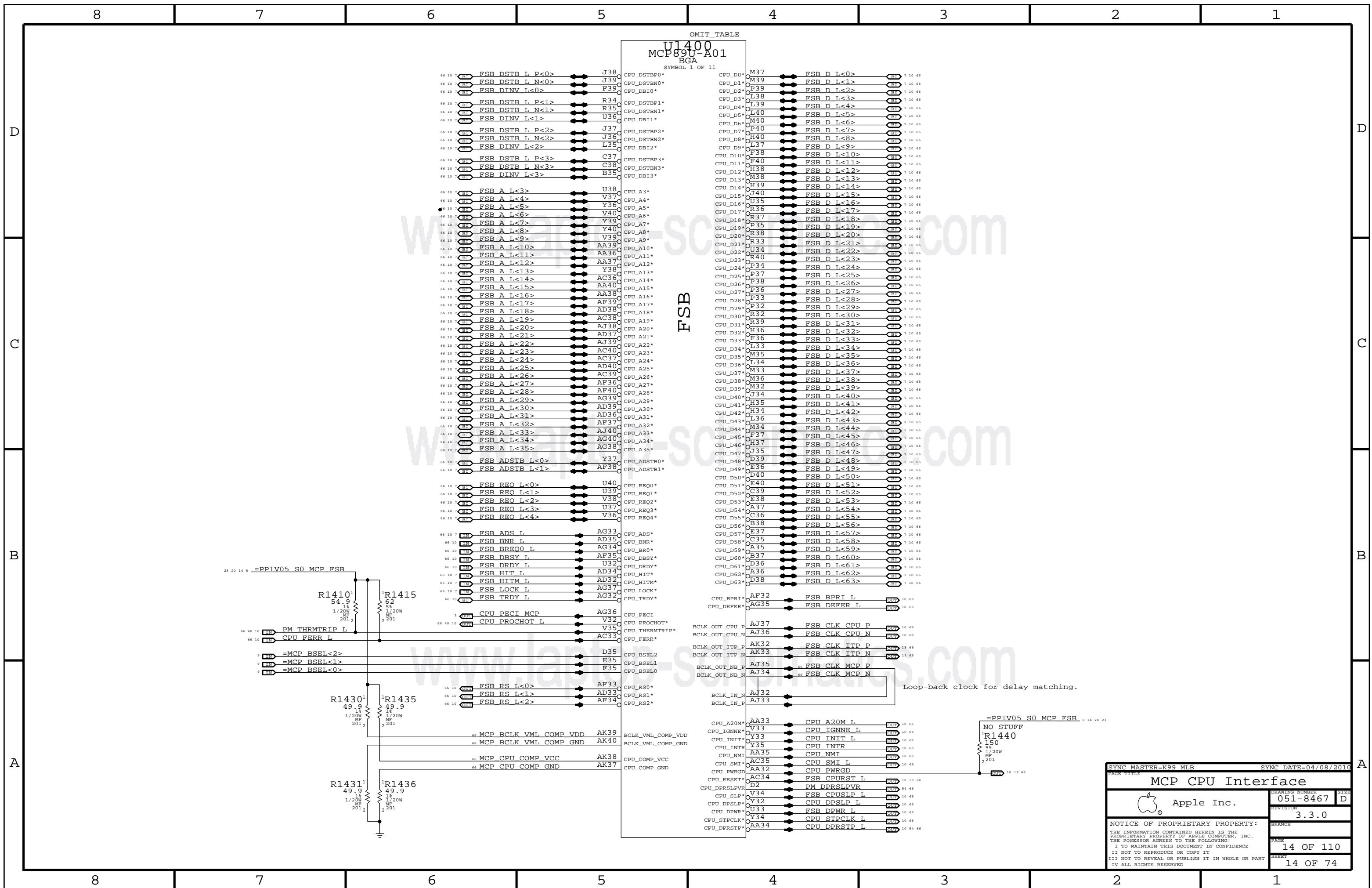
Micro2-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with 920-0782 Adapter Flex to support chipset debug.

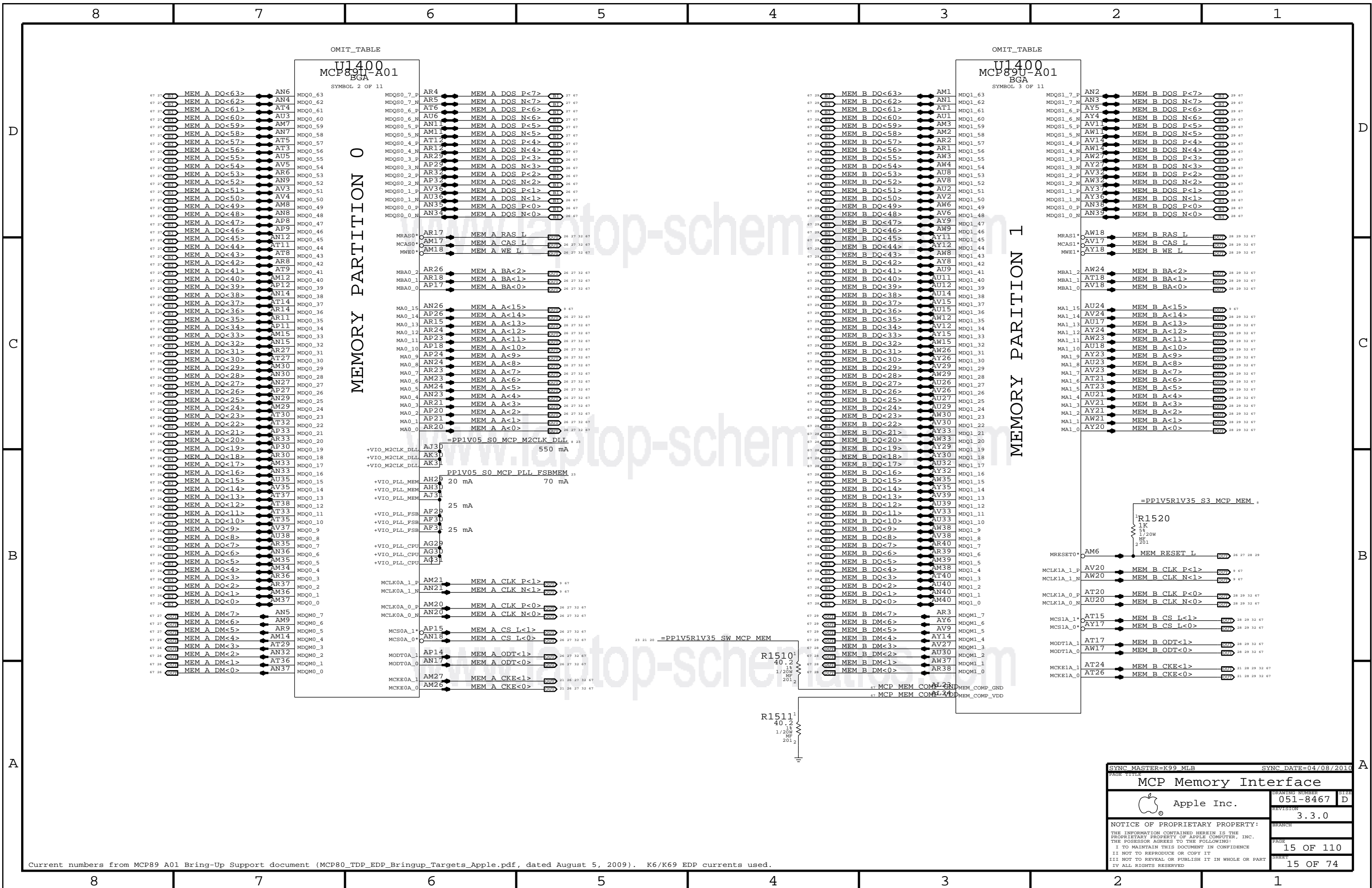


← Direction of XDP adapter flex
Please place J1300 within 1" of board edge with odd-numbered pins facing edge. Avoid any tall components between J1300 and edge.

SYNC MASTER=K99 MLB		SYNC DATE=03/01/2010	
eXtended Debug Port (Micro-XDP)			
Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
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MCP CPU Interface			
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	REVISION	3.3.0	
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OMIT_TABLE

U1400
MCP89U-A01
BGA

SYMBOL 2 OF 11

MEMORY PARTITION 0

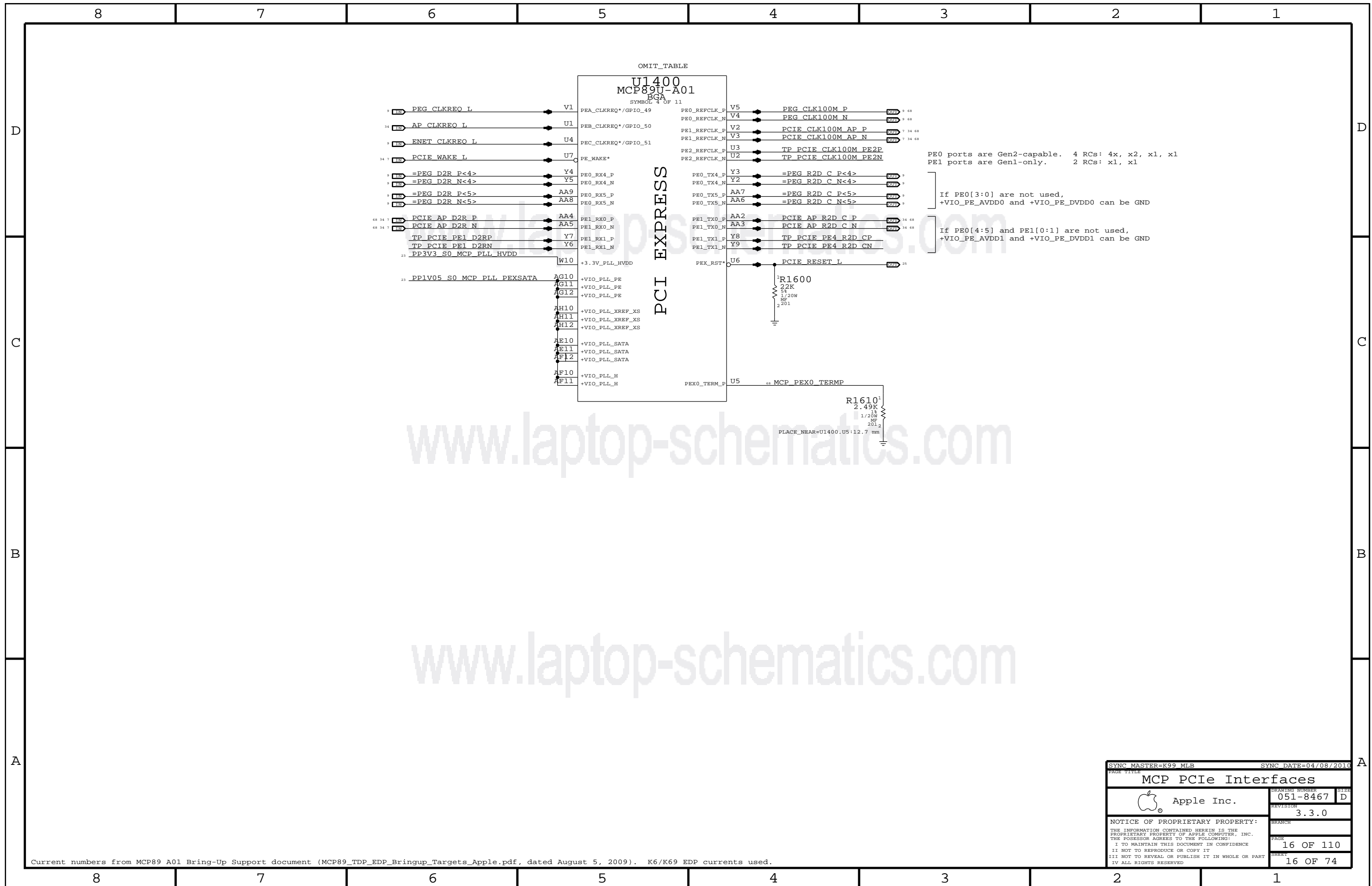
OMIT_TABLE

U1400
MCP89U-A01
BGA

SYMBOL 3 OF 11

MEMORY PARTITION 1

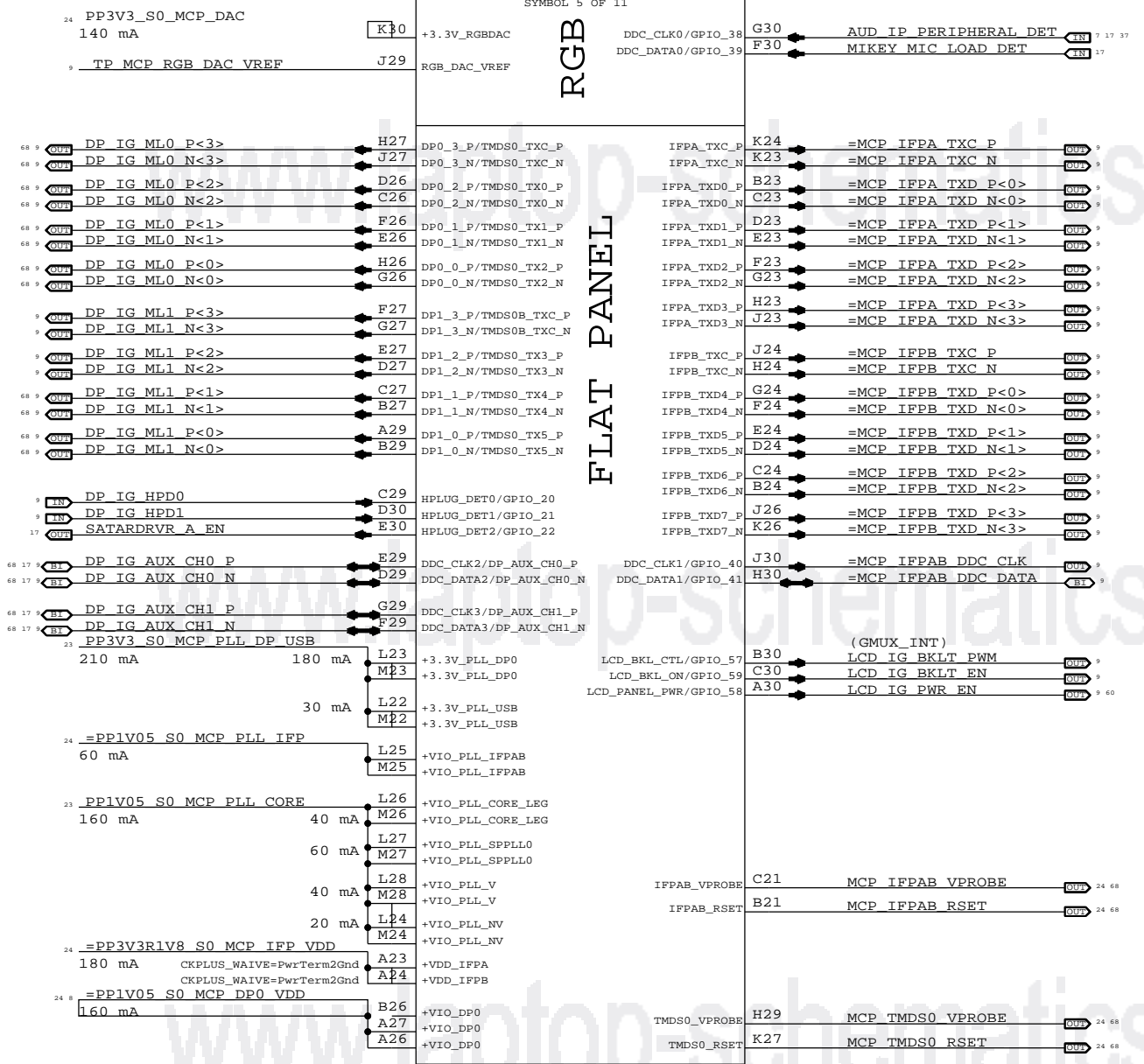
SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
MCP Memory Interface			
Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
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SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
MCP PCIe Interfaces			
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OMIT_TABLE

U1400
MCP890-A01
BGA
SYMBOL 5 OF 11



NOTE: 100K pull-downs required if HPLUG_DET0/HPLUG_DET1 are not used.

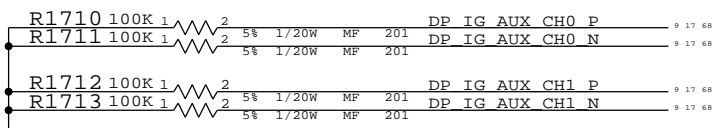
RGB DAC Disable:
 Okay to float all RGB_DAC signals.
 DDC_CLK0/DDC_DATA0 pull-ups still required (or use as GPIOs).
 Connect +3.3V_RGBDAC pin to GND.
 NOTE: No Composite/S-Video/Component Video support on MCP89

Interface Mode		
MCP Signal	TMDS/HDMI	LVDS
=MCP_IFFPA_TXC_P/N	TMDS_IG_TXC_P/N	LVDS_IG_A_CLK_P/N
=MCP_IFFPA_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	LVDS_IG_A_DATA_P/N<0>
=MCP_IFFPA_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	LVDS_IG_A_DATA_P/N<1>
=MCP_IFFPA_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	LVDS_IG_A_DATA_P/N<2>
=MCP_IFFPA_TXD_P/N<3>	(UNUSED)	LVDS_IG_A_DATA_P/N<3>
=MCP_IFFPB_TXC_P/N	(UNUSED)	LVDS_IG_B_CLK_P/N
=MCP_IFFPB_TXD_P/N<0>	TMDS_IG_TXD_P/N<3>	LVDS_IG_B_DATA_P/N<0>
=MCP_IFFPB_TXD_P/N<1>	TMDS_IG_TXD_P/N<4>	LVDS_IG_B_DATA_P/N<1>
=MCP_IFFPB_TXD_P/N<2>	TMDS_IG_TXD_P/N<5>	LVDS_IG_B_DATA_P/N<2>
=MCP_IFFPB_TXD_P/N<3>	(UNUSED)	LVDS_IG_B_DATA_P/N<3>
=MCP_IFFPAB_DDC_CLK	TMDS_IG_DDC_CLK	LVDS_IG_DDC_CLK
=MCP_IFFPAB_DDC_DATA	TMDS_IG_DDC_DATA	LVDS_IG_DDC_DATA

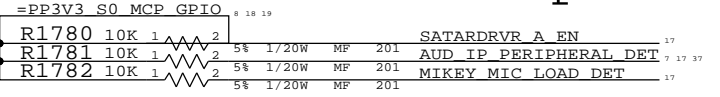
LVDS: Power +VDD_IFFPx at 1.8V
 TMDS: Power +VDD_IFFPx at 3.3V

DDC Mode Pull-downs

NOTE: DP_AUX_CH1 also requires pull-downs if used for dual-mode DisplayPort (DP++). If unused no pulls are necessary, if used for TMDS/HDMI only then only pull-ups are necessary.



GPIO Pull-Ups



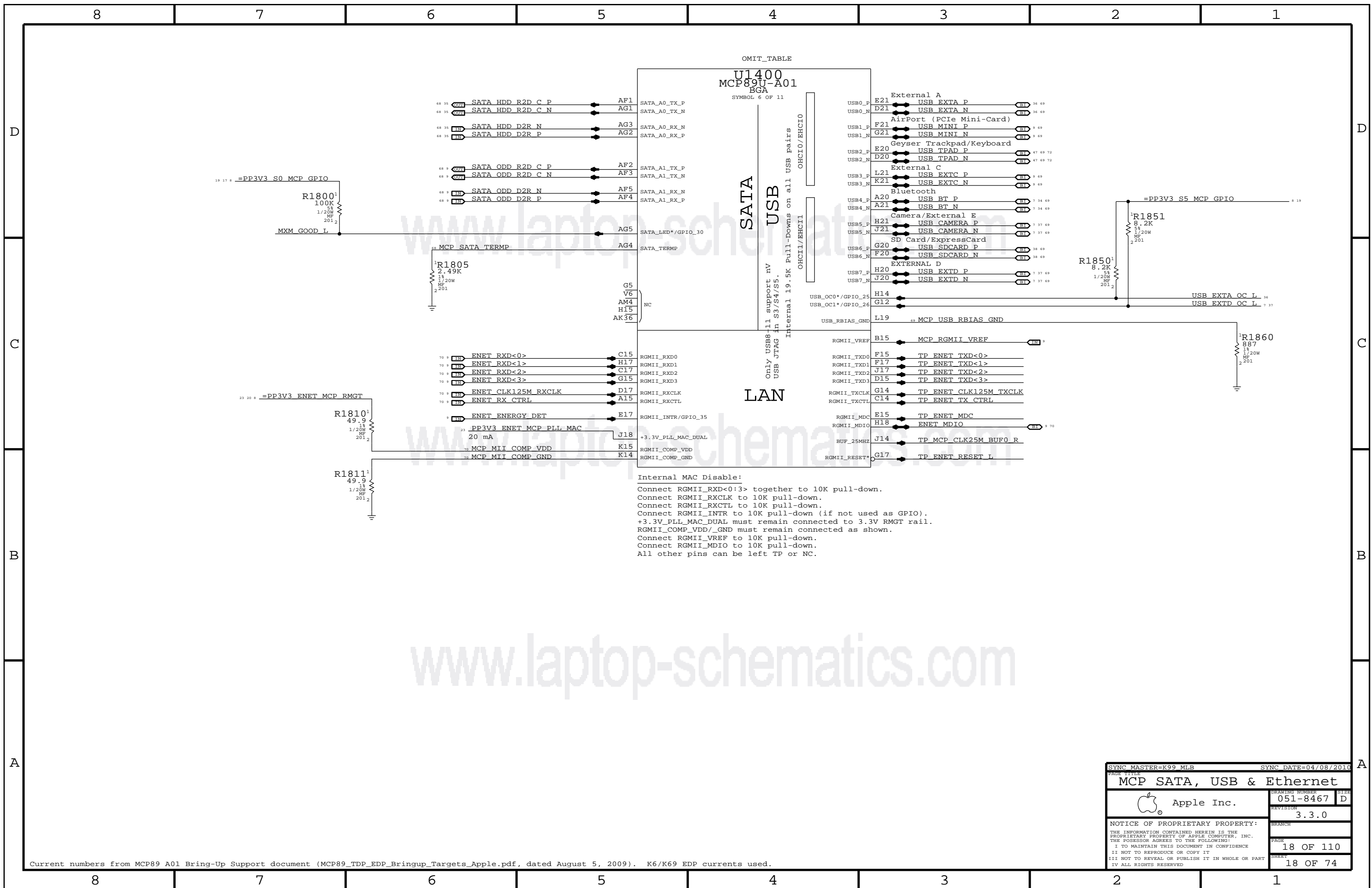
SYNC MASTER=K99 MLB SYNC DATE=04/08/2010

MCP Graphics

Apple Inc. DRAWING NUMBER 051-8467 SIZE D
 REVISION 3.3.0

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OMIT TABLE

U1400
MCP89U-A01
BGA
SYMBOL 6 OF 11

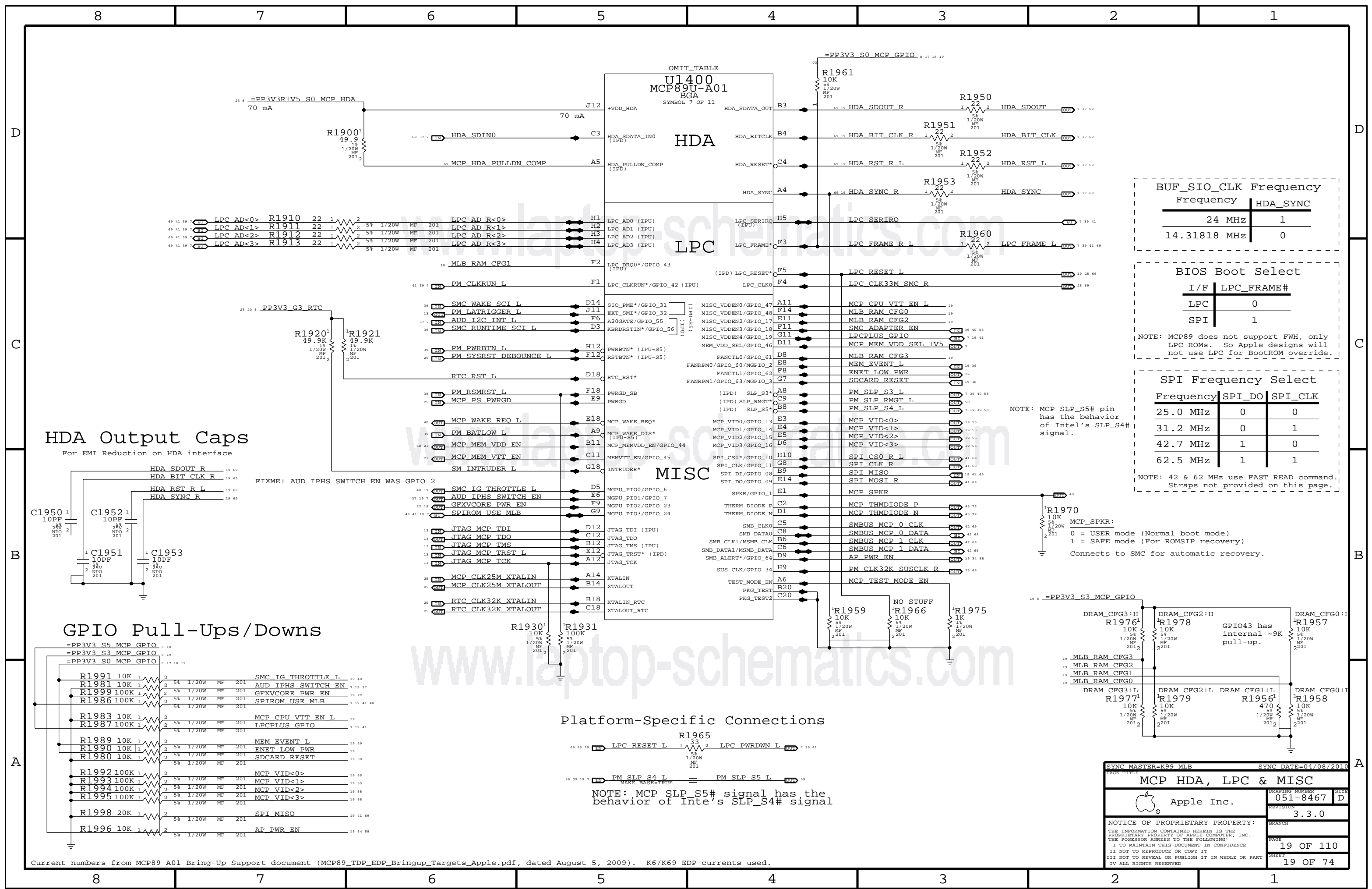
SATA
USB

LAN

Only USB8+11 support nv
USB JTAG in S3/S4/S5.
Internal 19.5K Pull-Downs on all USB pairs
OHCI0/EHCIO
OHCI1/EHC11

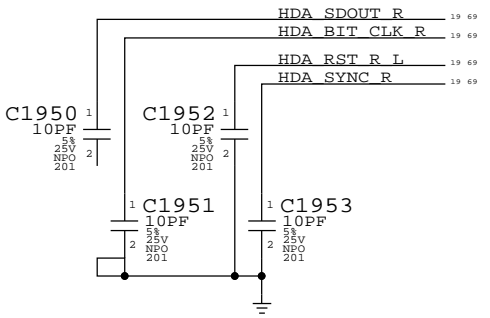
Internal MAC Disable:
Connect RGMII_RXD<0:3> together to 10K pull-down.
Connect RGMII_RXCLK to 10K pull-down.
Connect RGMII_RXCTL to 10K pull-down.
Connect RGMII_INTR to 10K pull-down (if not used as GPIO).
+3.3V_PLL_MAC_DUAL must remain connected to 3.3V RMGT rail.
RGMII_COMP_VDD/_GND must remain connected as shown.
Connect RGMII_VREF to 10K pull-down.
Connect RGMII_MDIO to 10K pull-down.
All other pins can be left TP or NC.

SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE MCP SATA, USB & Ethernet			
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	REVISION	3.3.0	
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		SHEET	18 OF 74

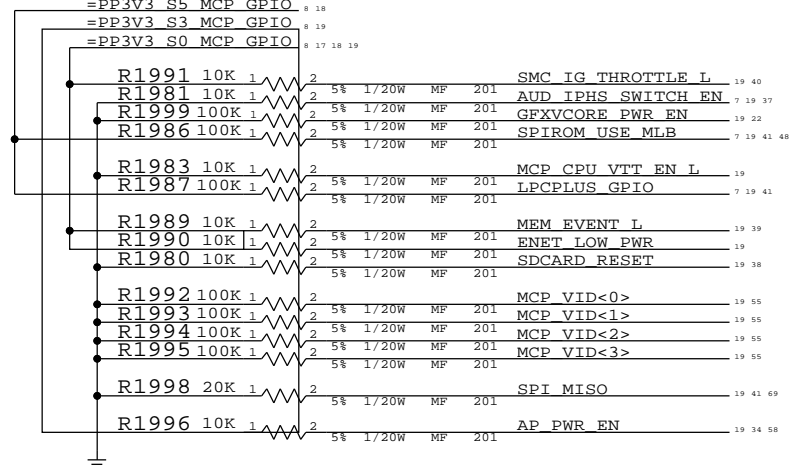


HDA Output Caps

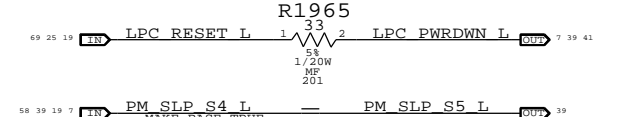
For EMI Reduction on HDA interface



GPIO Pull-Ups/Downs



Platform-Specific Connections



NOTE: MCP SLP_S5# signal has the behavior of Intel's SLP_S4# signal

BUF_SIO_CLK Frequency	
Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

BIOS Boot Select	
I/F	LPC_FRAME#
LPC	0
SPI	1

NOTE: MCP89 does not support FWB, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

SPI Frequency Select		
Frequency	SPI_DO	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
42.7 MHz	1	0
62.5 MHz	1	1

NOTE: 42 & 62 MHz use FAST_READ command. Straps not provided on this page.

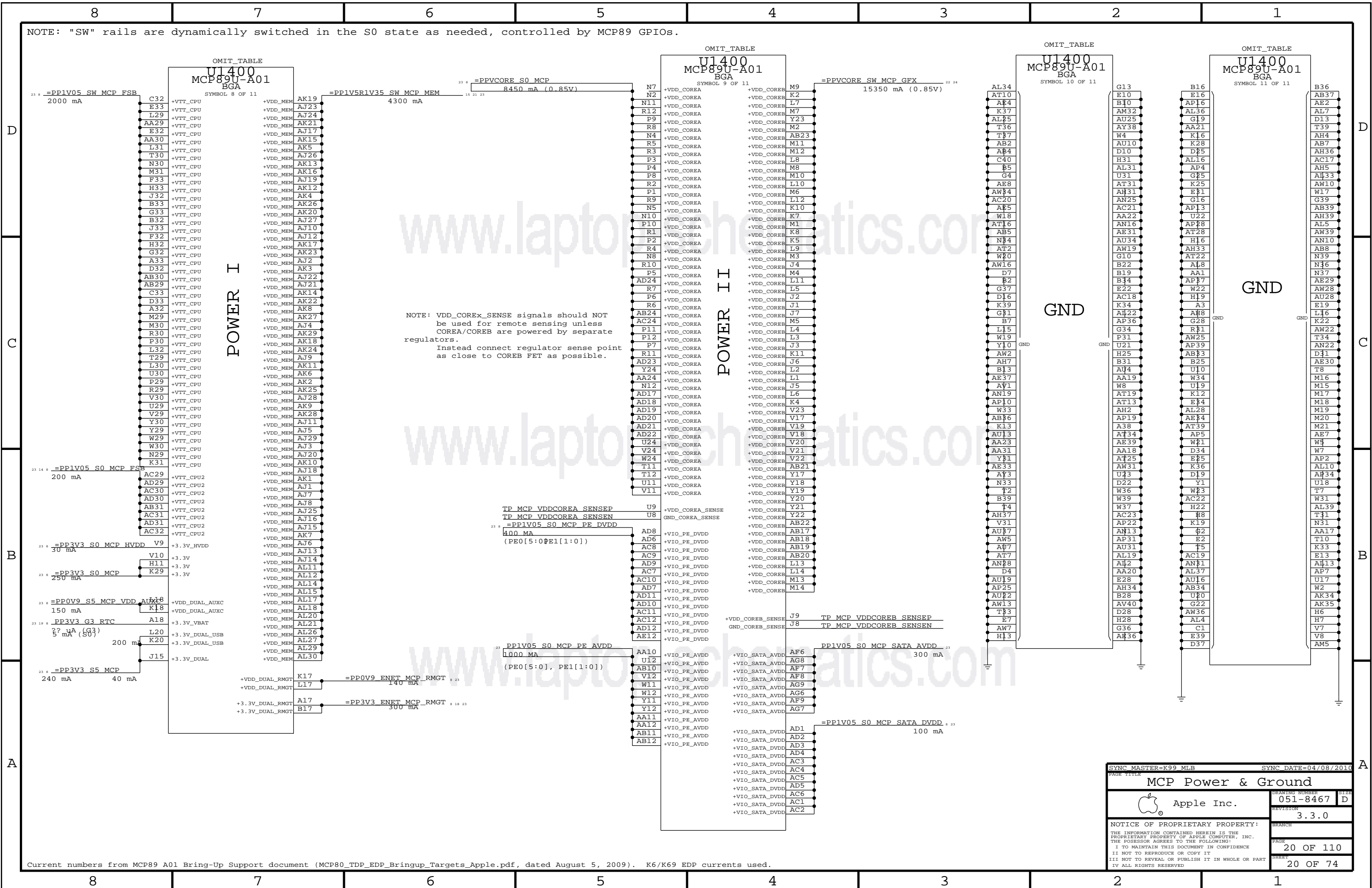
NOTE: MCP SLP_S5# pin has the behavior of Intel's SLP_S4# signal.

R1970 MCP_SPKR:
 0 = USER mode (Normal boot mode)
 1 = SAFE mode (For ROMSIP recovery)
 Connects to SMC for automatic recovery.

SYNC MASTER=K99_MLB SYNC DATE=04/08/2010

MCP HDA, LPC & MISC	
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NOTE: "SW" rails are dynamically switched in the S0 state as needed, controlled by MCP89 GPIOs.



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SYNC MASTER=K99 MLB SYNC DATE=04/08/2010

MCP Power & Ground

Apple Inc.

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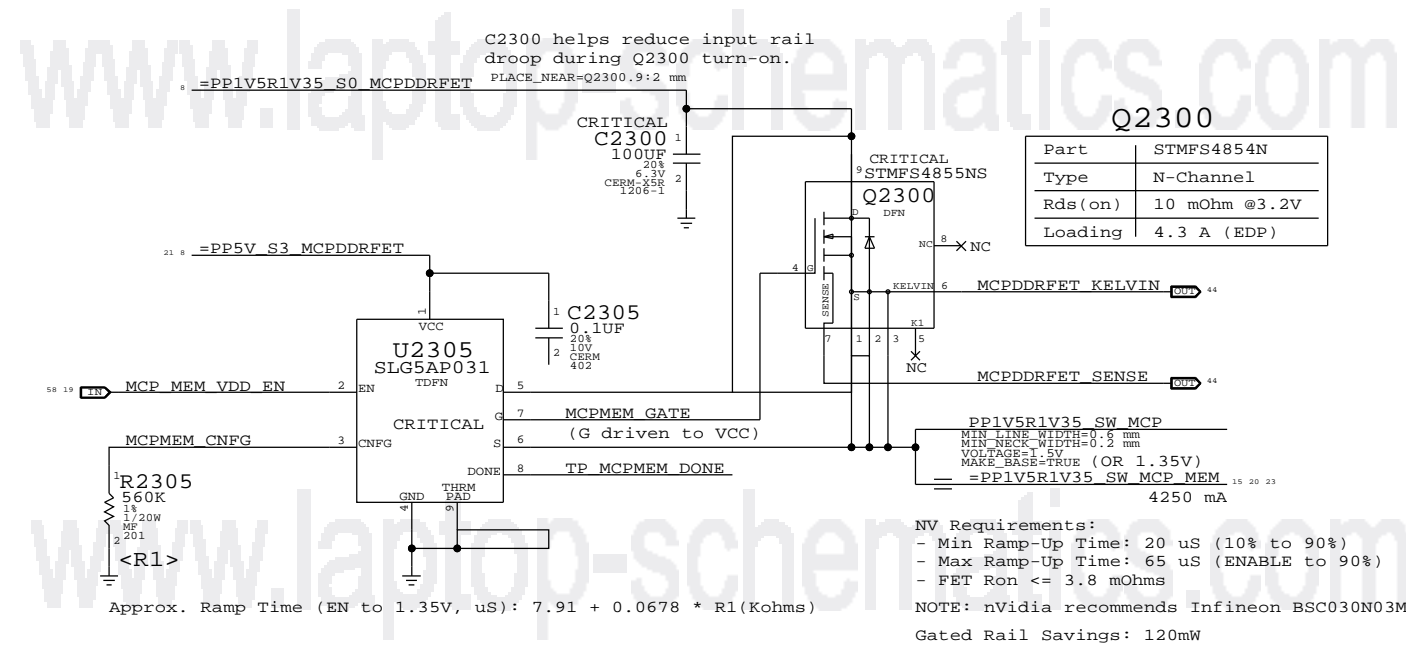
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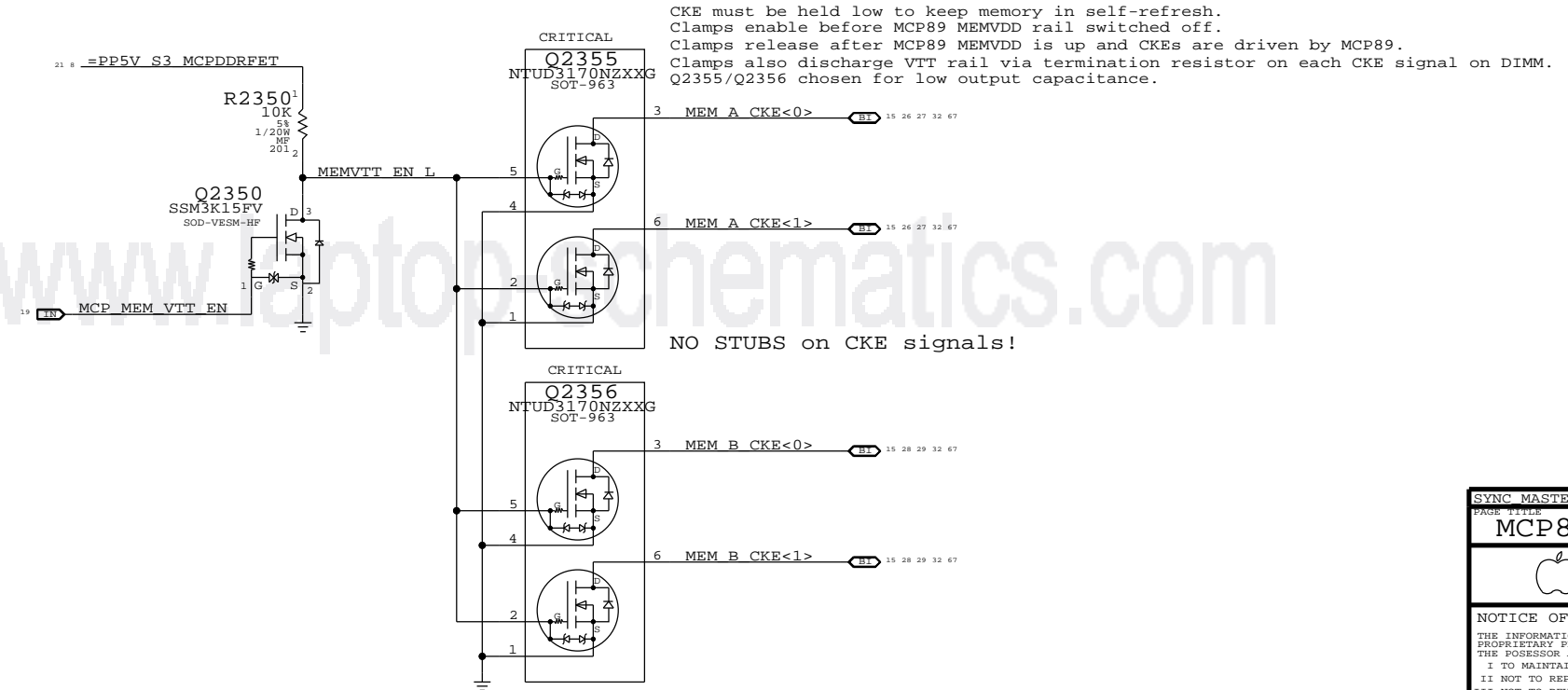
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Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

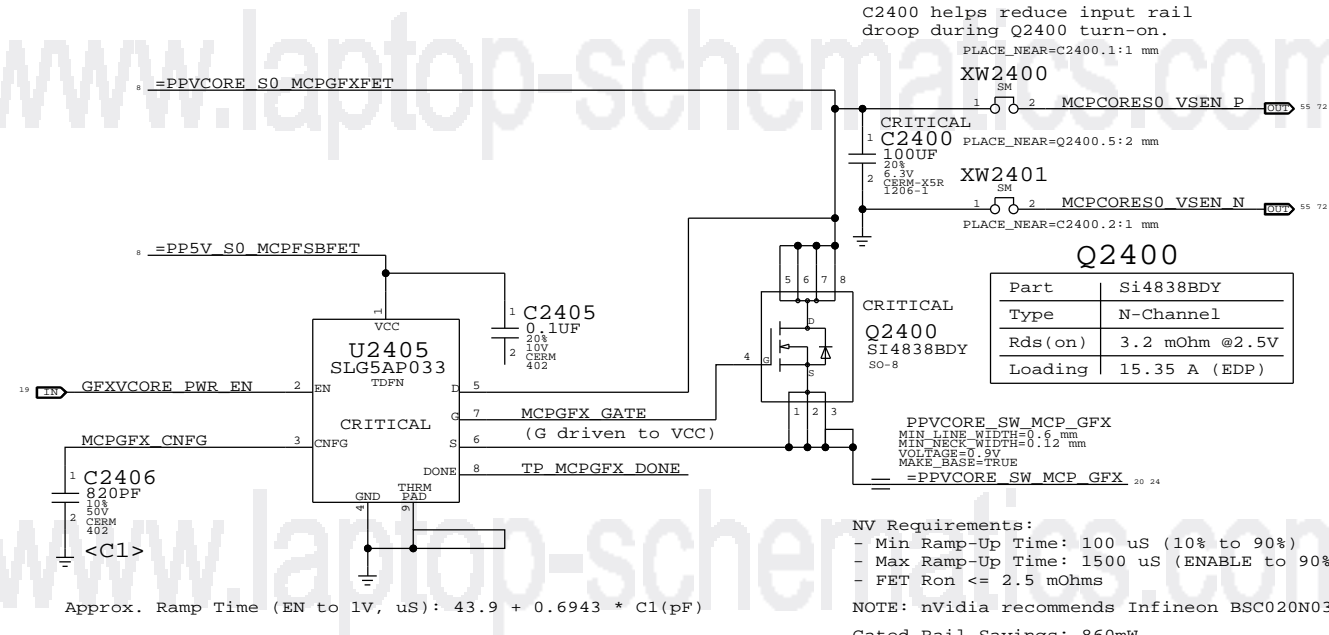


DIMM CKE Clamps



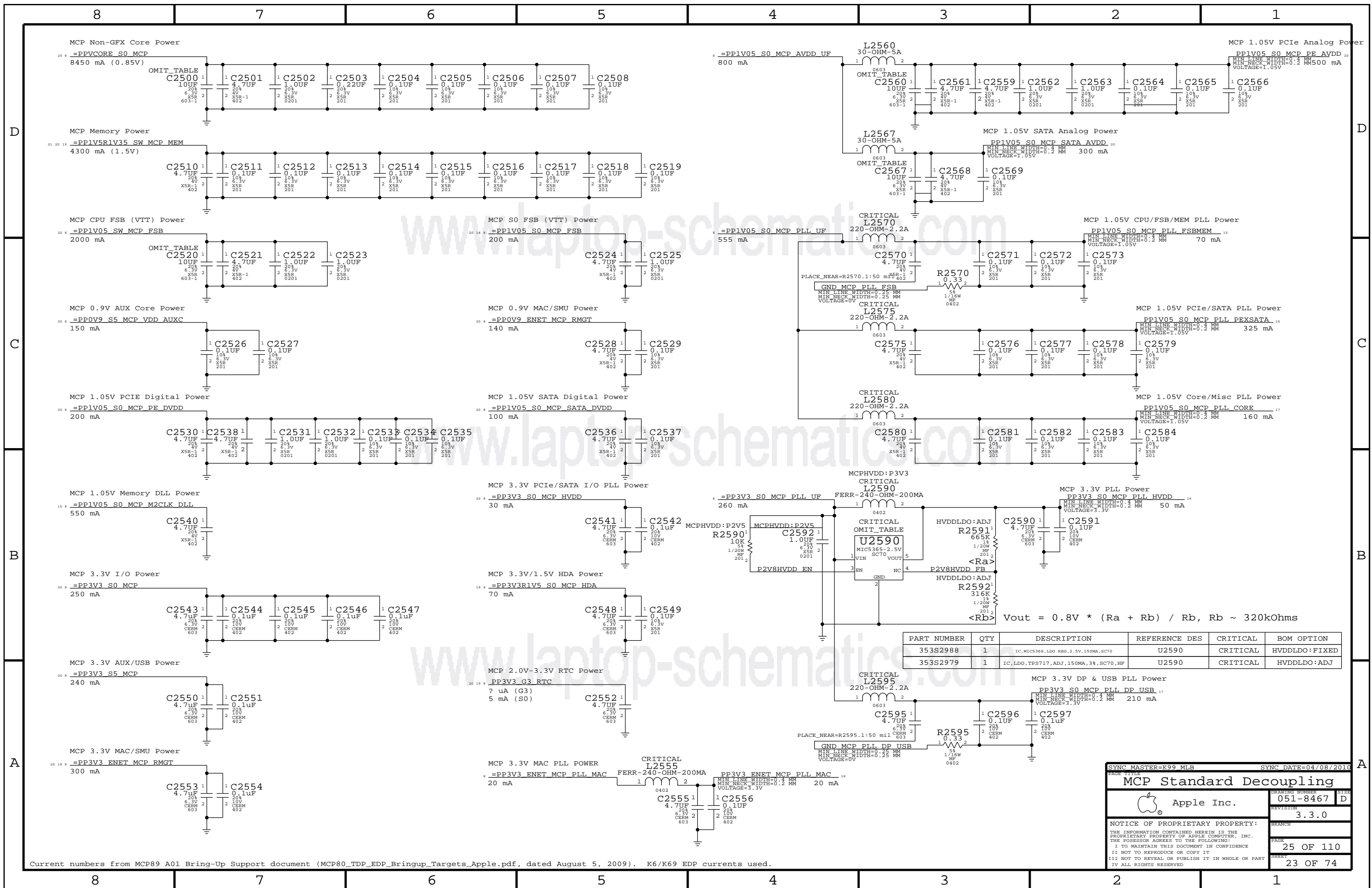
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MCP89 Memory Rail Gating			
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		REVISION	3.3.0
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MCP89 GFX Core Rail Gating			
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2988	1	IC, MIC5366, LDO REG, 2.5V, 150mA, SC70	U2590	CRITICAL	HVDDLDO: FIXED
353S2979	1	IC, LDO, TPS717, ADJ, 150mA, 3%, SC70, HF	U2590	CRITICAL	HVDDLDO: ADJ

$$V_{out} = 0.8V * (R_a + R_b) / R_b, R_b \sim 320k\Omega$$

SYNC MASTER=K99 MLB SYNC DATE=04/08/2010

MCP Standard Decoupling

Apple Inc.

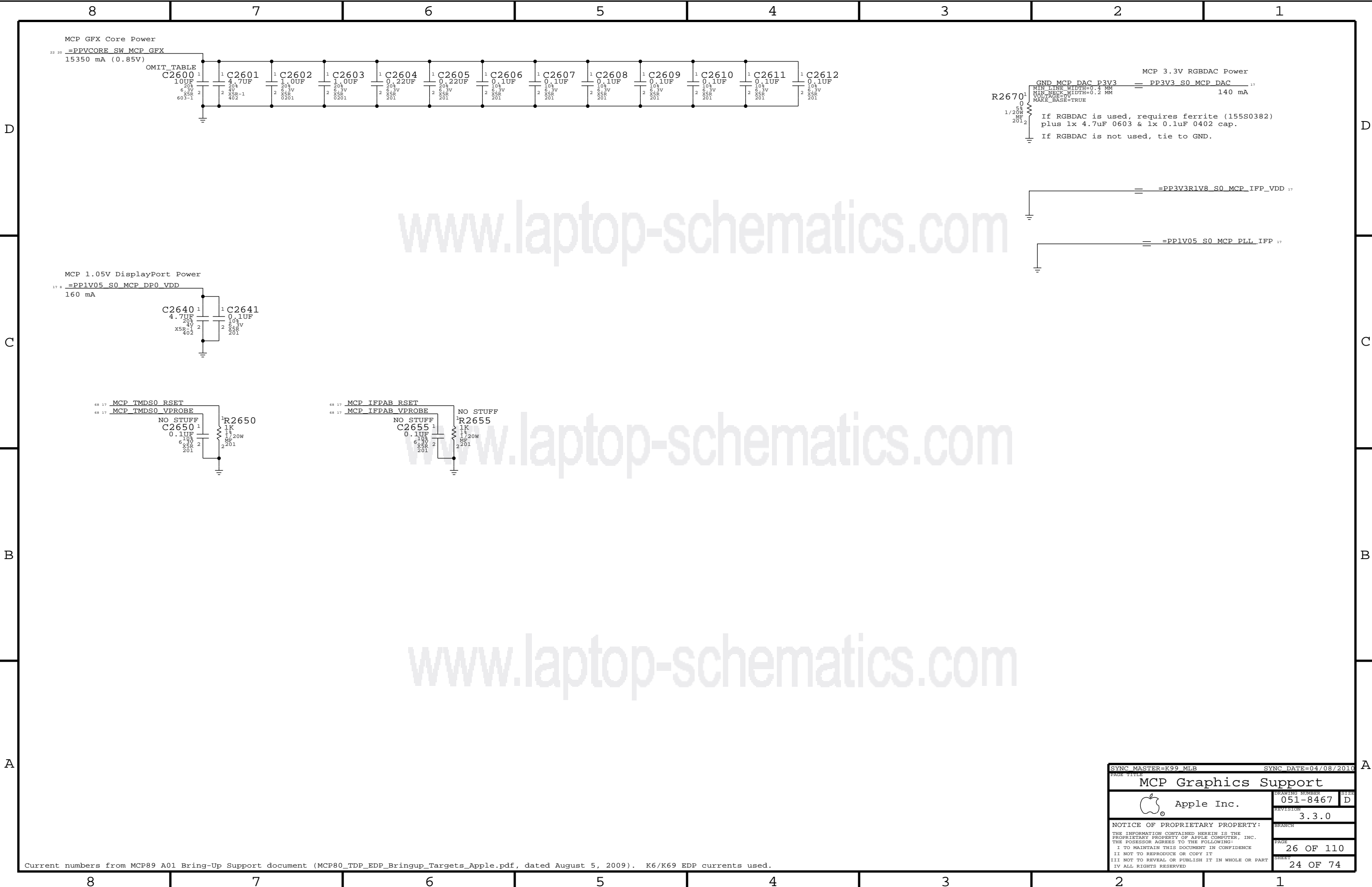
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REVISION: 3.3.0

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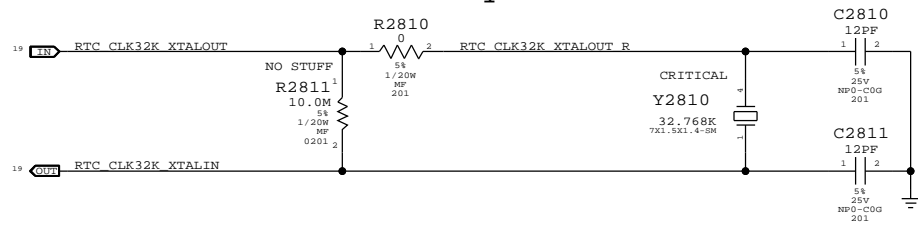
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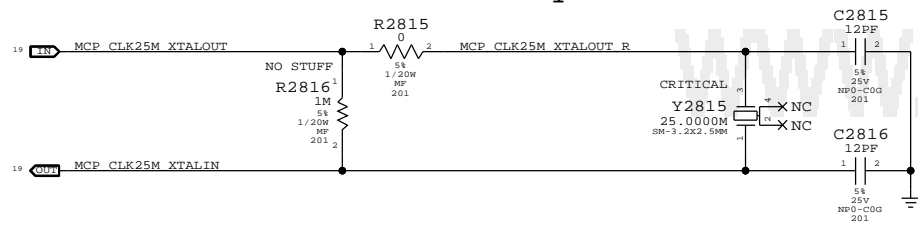
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SYNC MASTER=K99_MLB		SYNC DATE=04/08/2010	
MCP Graphics Support			
	DRAWING NUMBER	051-8467	SIZE
	REVISION	3.3.0	
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RTC Crystal

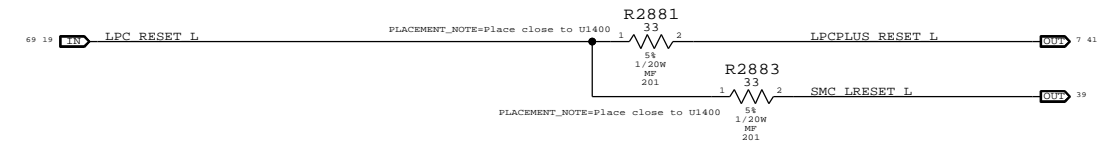


MCP 25MHz Crystal

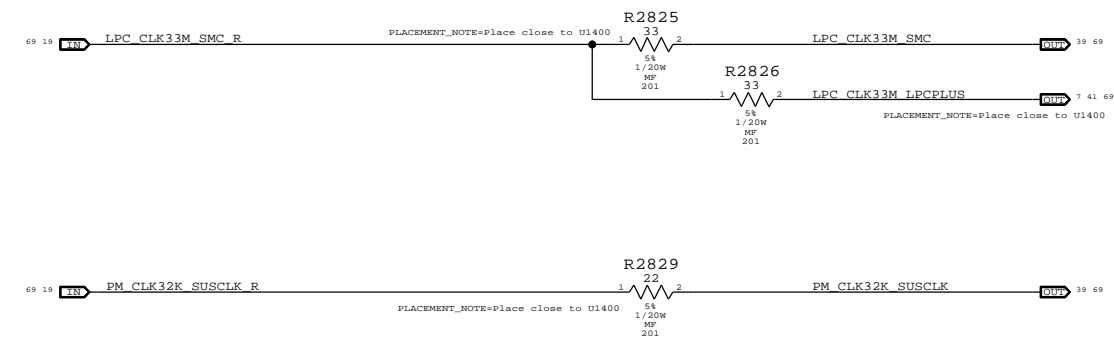
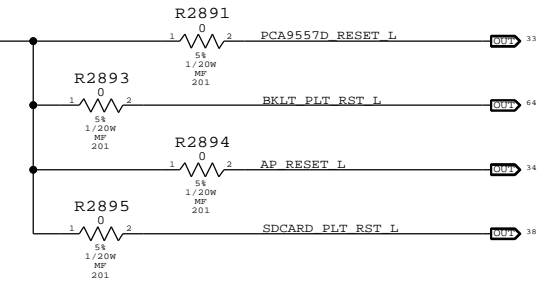


Platform Reset Connections

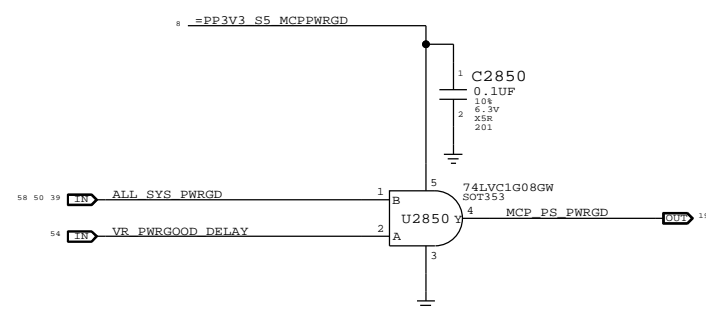
LPC Reset (Unbuffered)



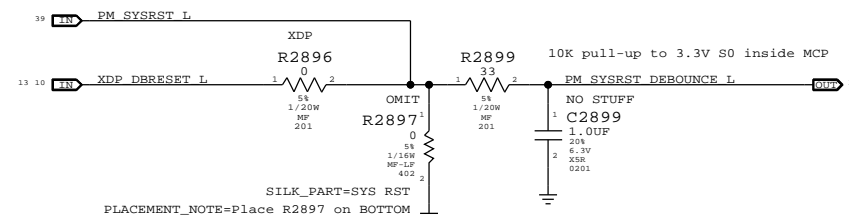
PCIE Reset (Unbuffered)



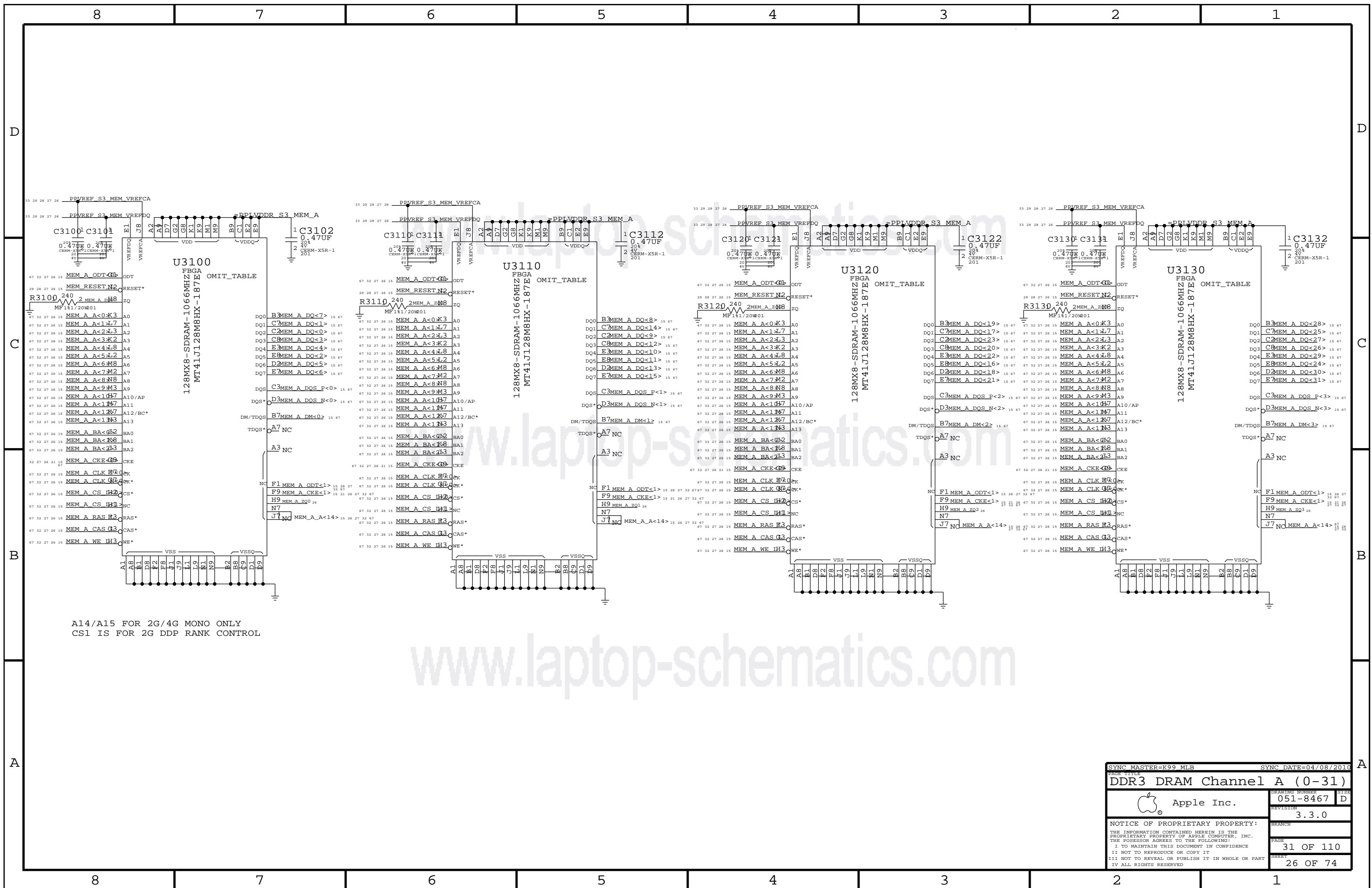
MCP S0 PWRGD & CPU_VLD



System Reset Circuit

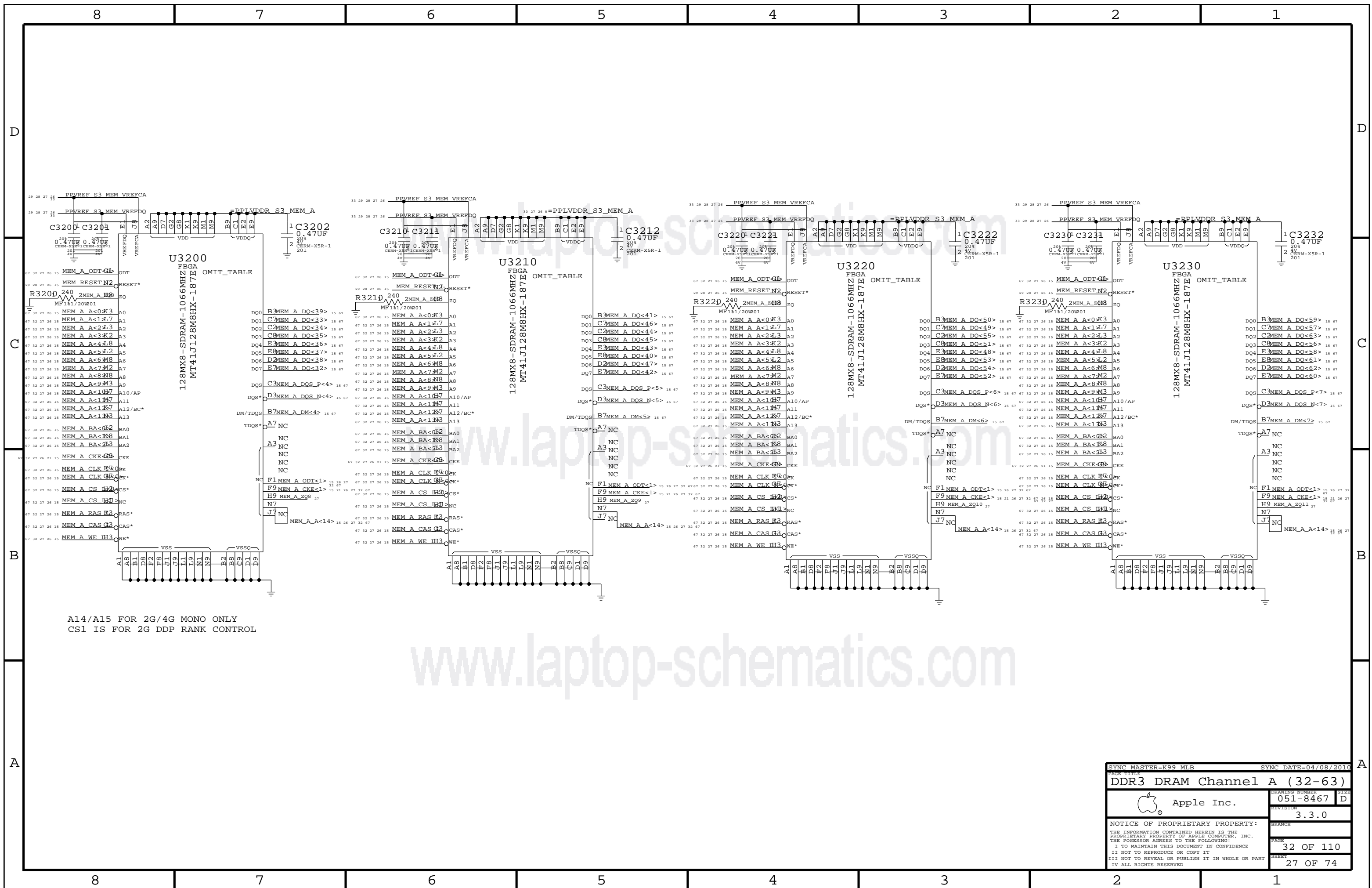


PAGE TITLE		SYNC DATE=(02/11/2010)	
SB Misc			
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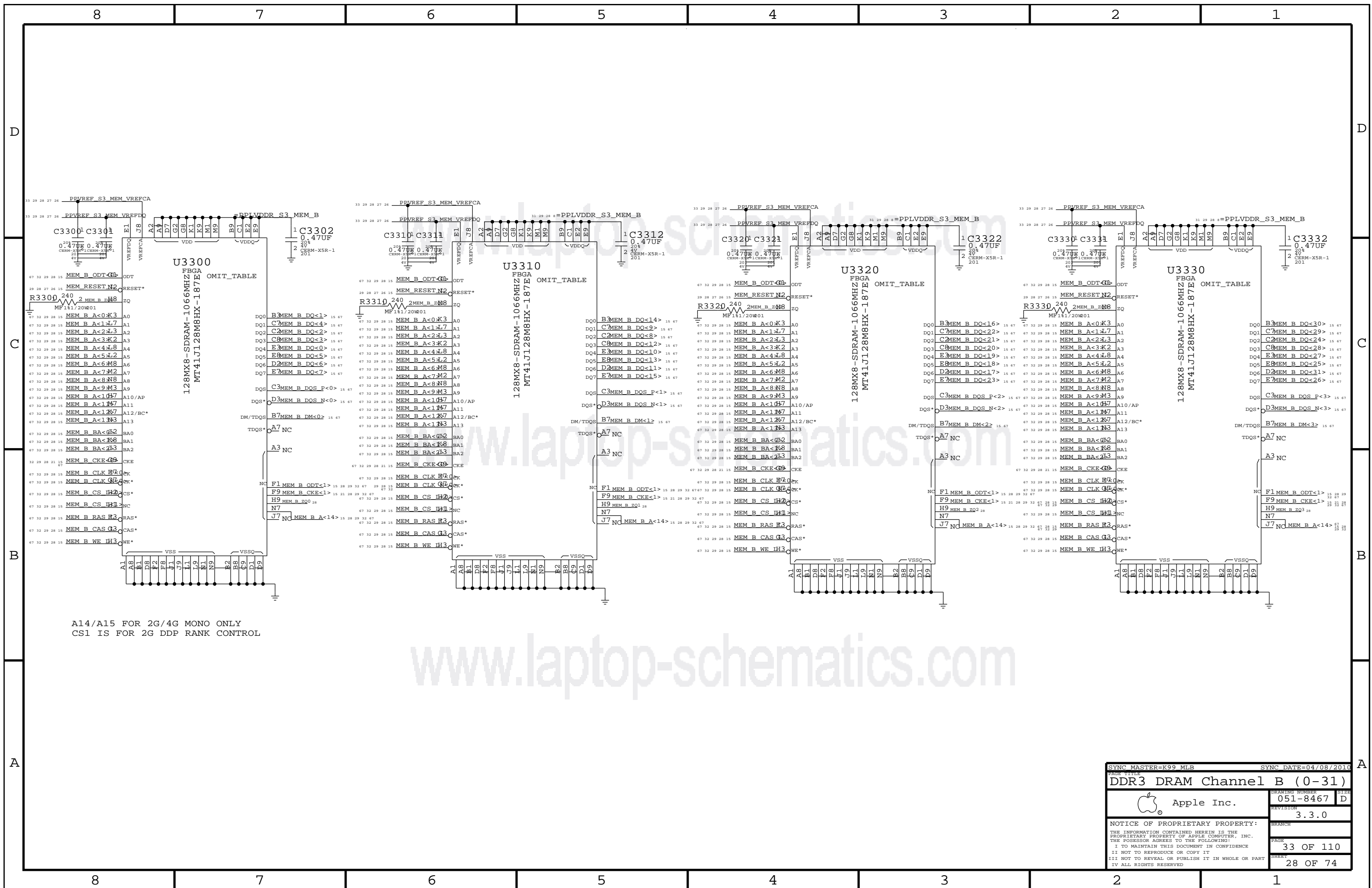
A14/A15 FOR 2G/4G MONO ONLY
 CS1 IS FOR 2G DDP RANK CONTROL

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DRAWING NUMBER 051-8467		SIZE D	
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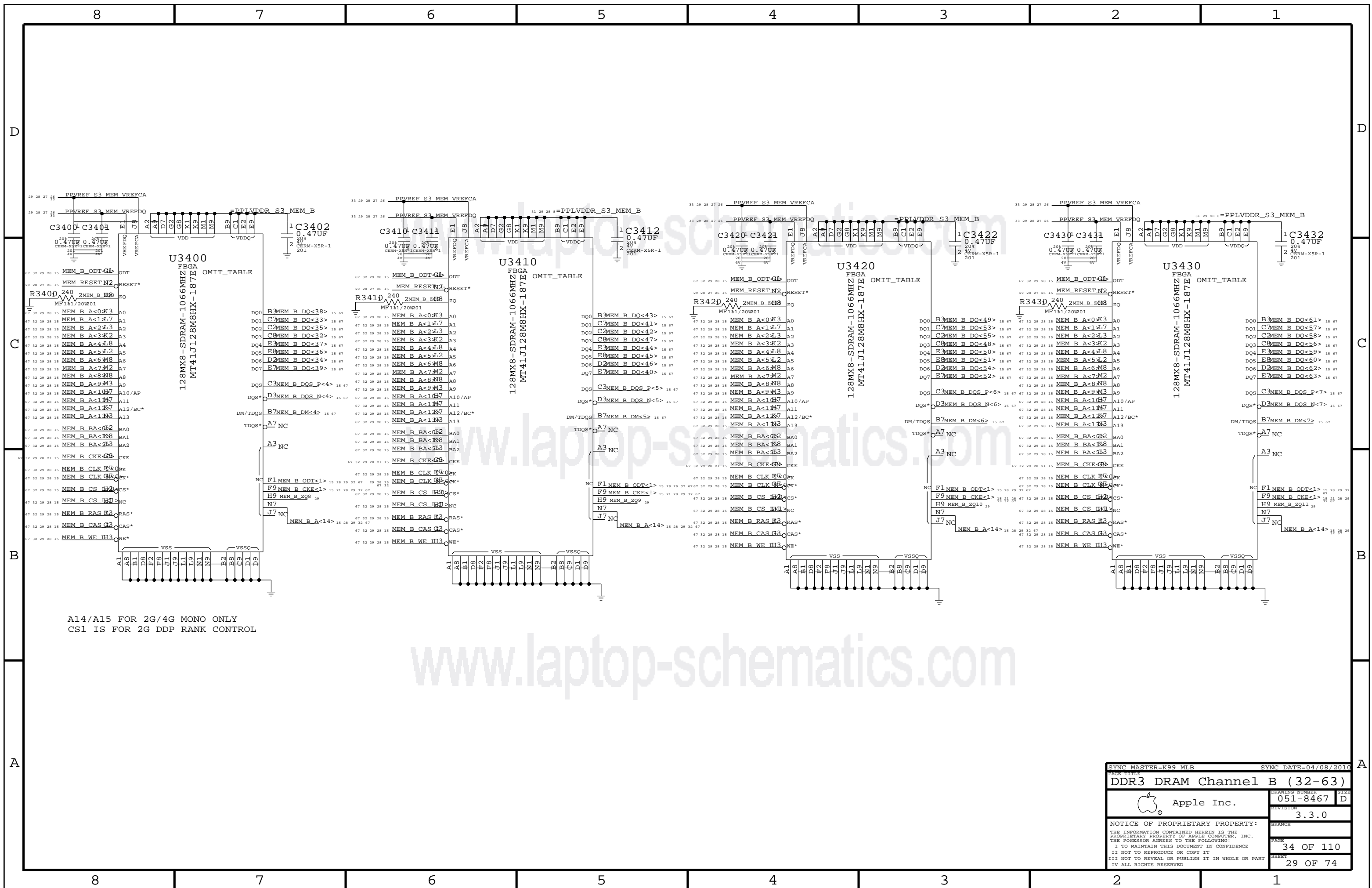
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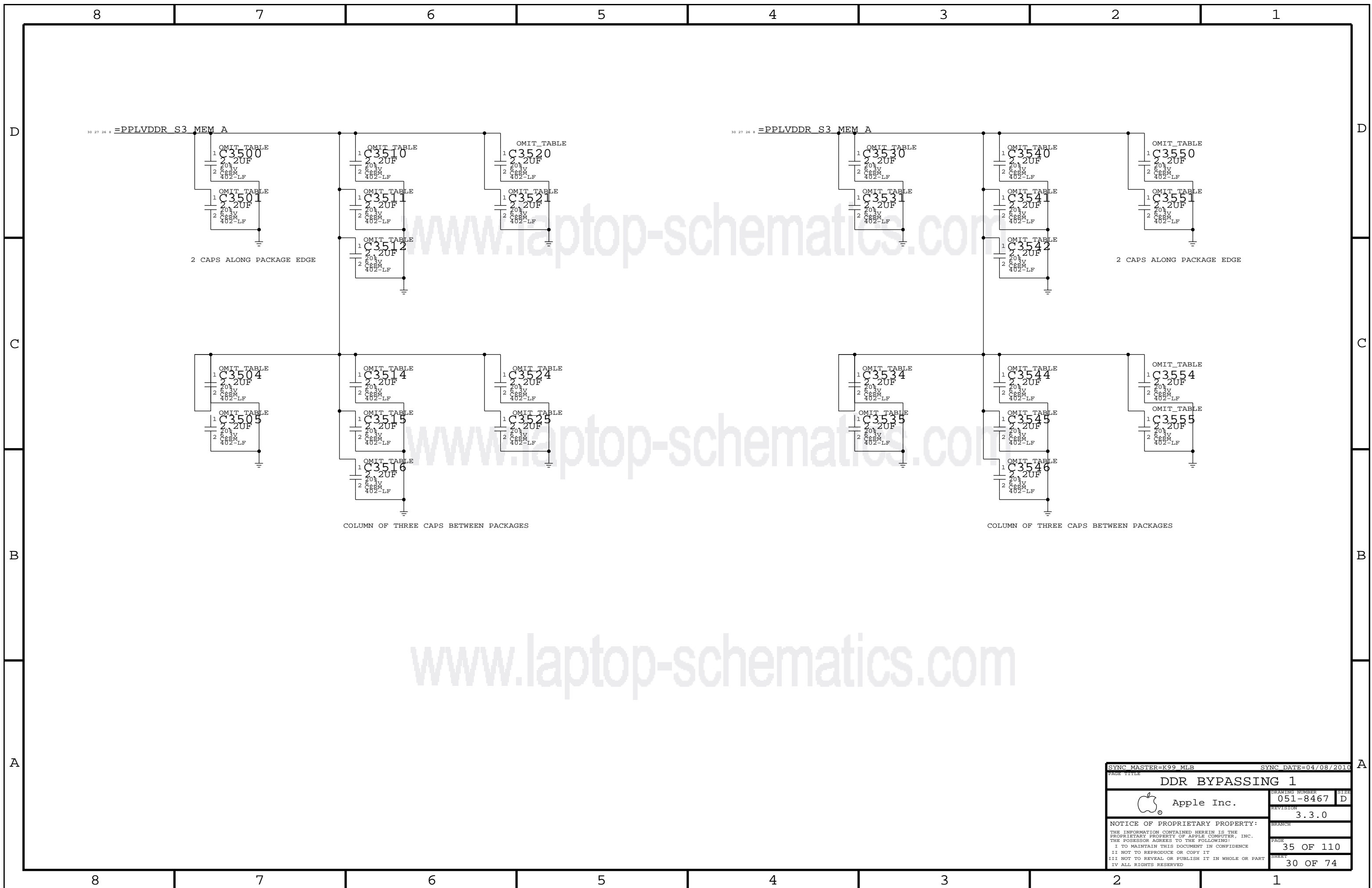
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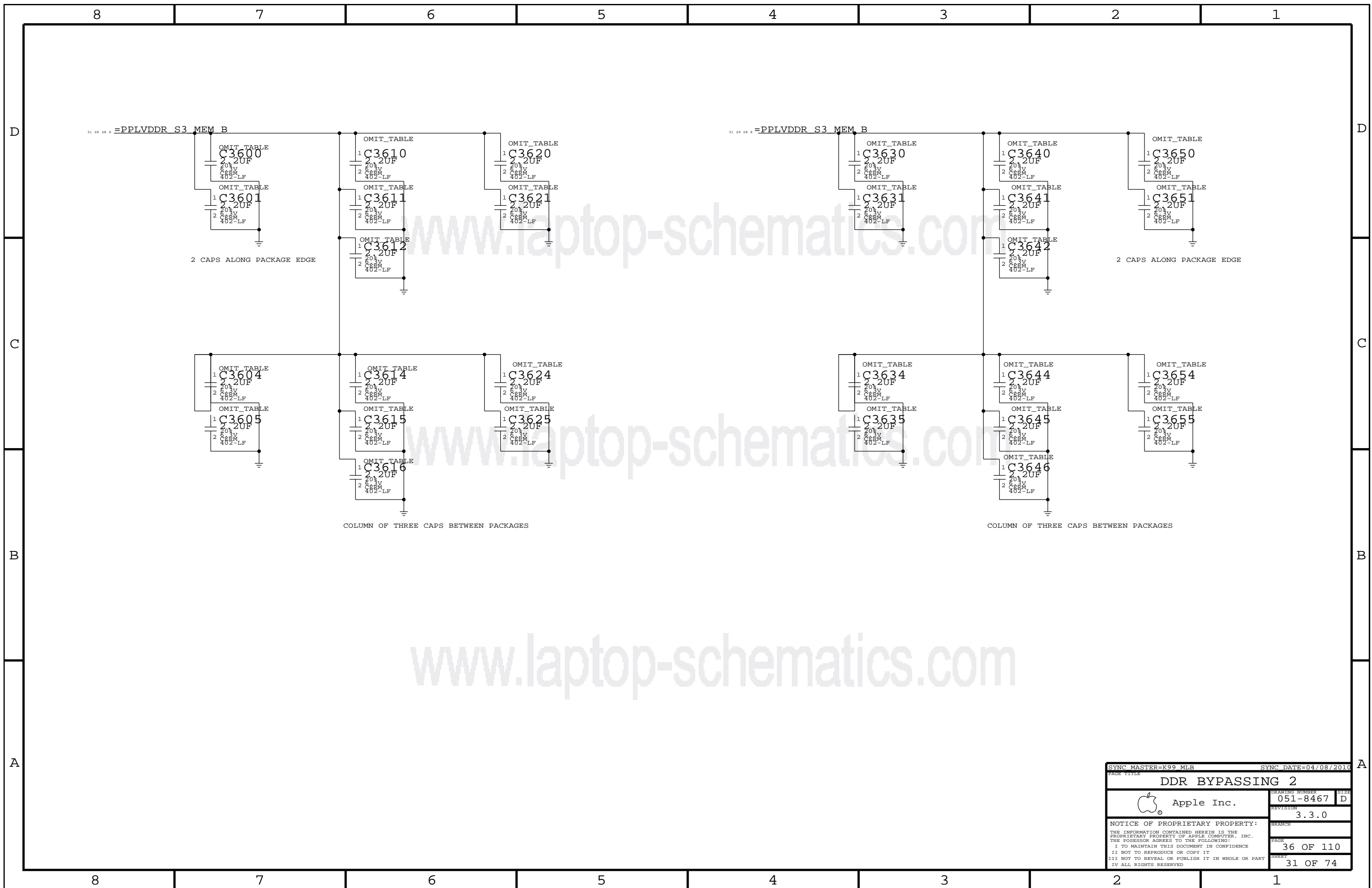
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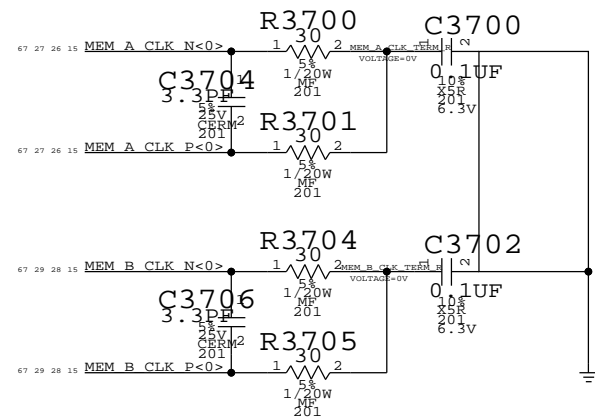
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DDR BYPASSING 1			
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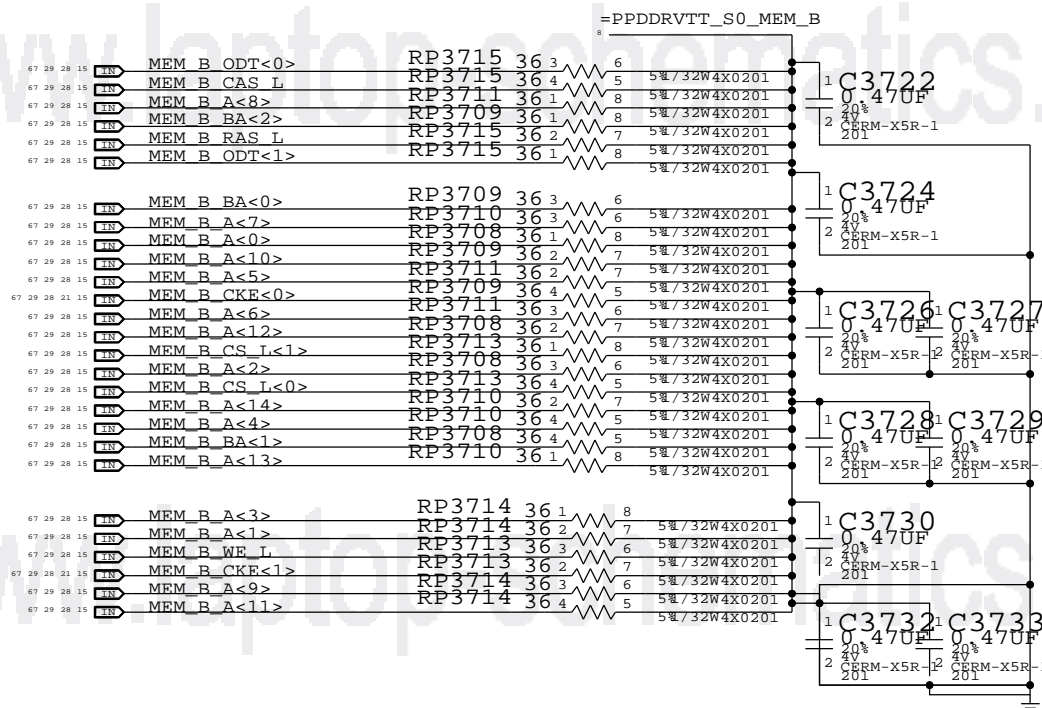
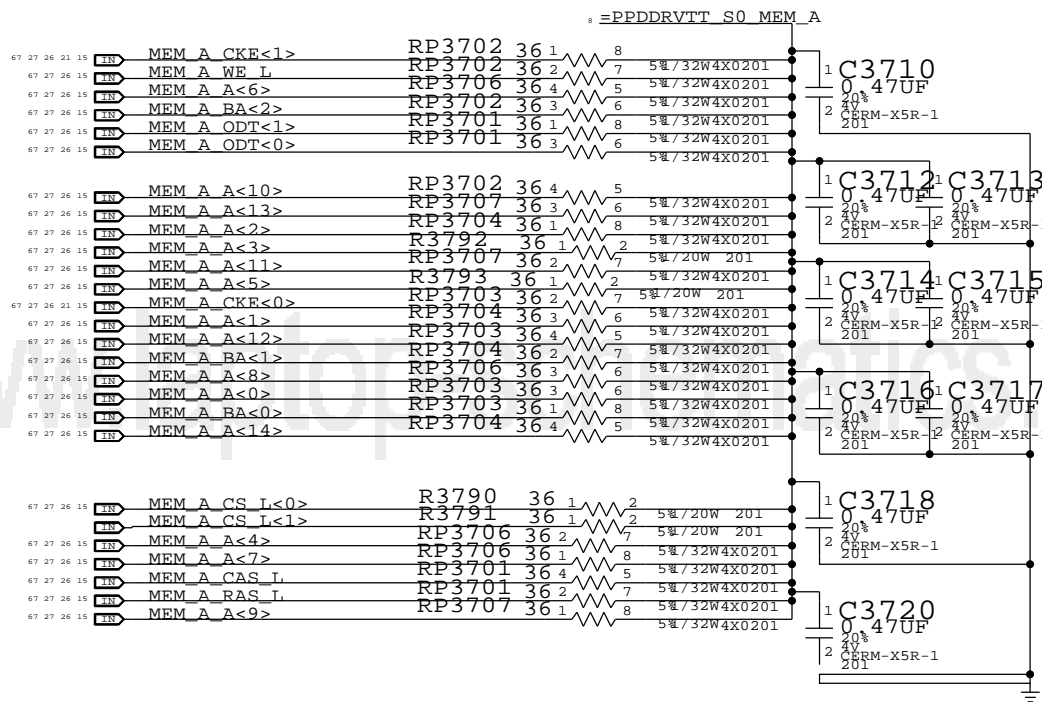
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		SHEET	31 OF 74

MEM CLOCK TERMINATION

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM

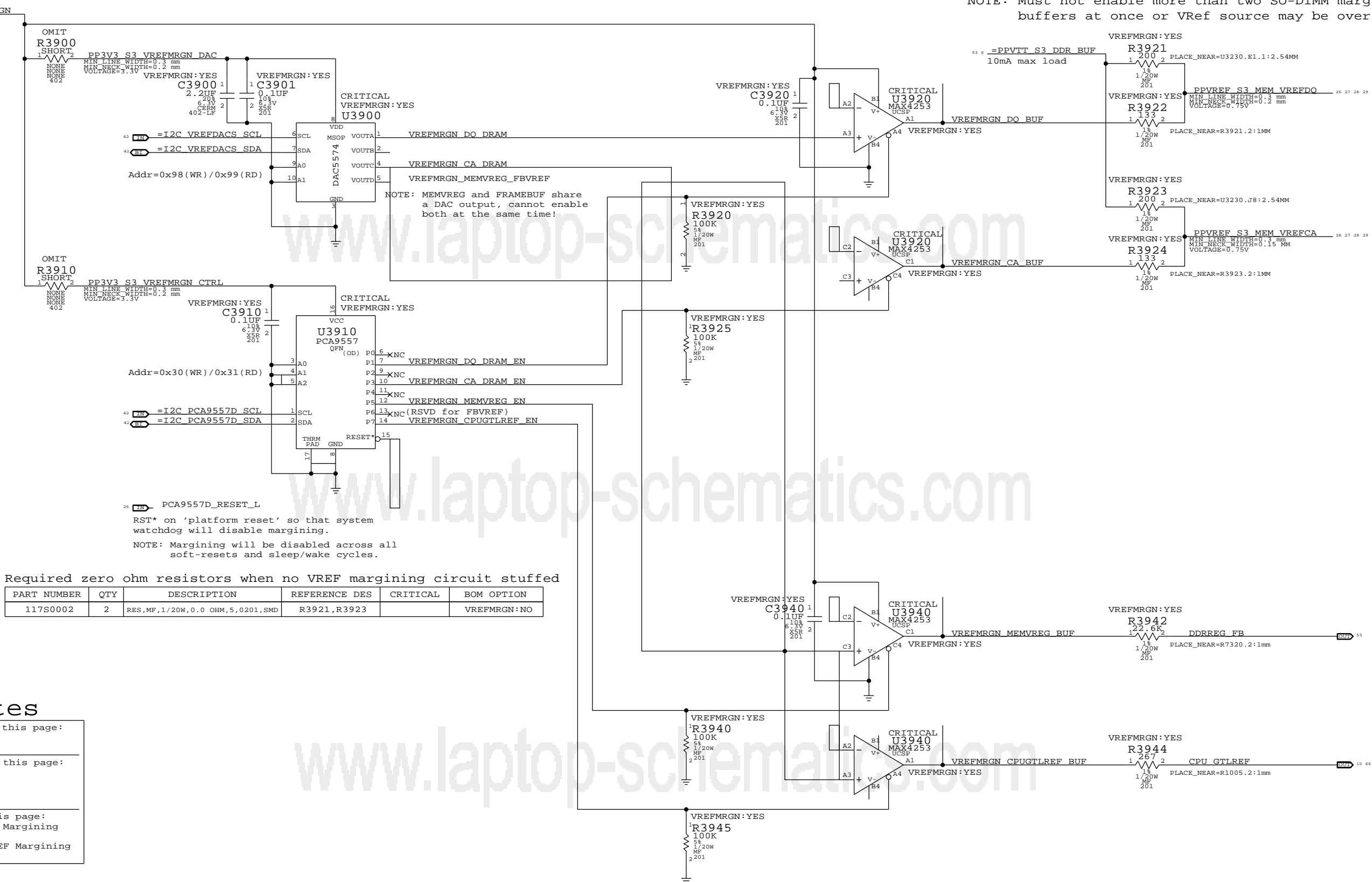


JEDEC recommends 30 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE



SYNC MASTER=K99_MLB		SYNC DATE=04/08/2010	
Memory Active Termination			
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NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.



NOTE: MEMVREG and FRAMEBUF share a DAC output, cannot enable both at the same time!

PCA9557D_RESET_L
RST* on 'platform reset' so that system watchdog will disable margining.
NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	2	RES, MF, 1/20W, 0.0 OHM, 5, 0201, SMD	R3921, R3923		VREFMRGN:NO

Page Notes

- Power aliases required by this page:
 - =PP3V3_S3_VREFMRGN
 - =PPVTT_S3_DDR_BUF
- Signal aliases required by this page:
 - =I2C_VREFDACS_SCL
 - =I2C_VREFDACS_SDA
 - =I2C_PCA9557D_SCL
 - =I2C_PCA9557D_SDA
- BOM options provided by this page:
 - VREFMRGN:YES - Stuffs VREF Margining Circuitry.
 - VREFMRGN:NO - Bypasses VREF Margining Circuitry.

	MEM VREF DQ	MEM VREF CA	MEM VREG	CPU GTLREF (FSB)
DAC Channel:	A	C	D	D
PCA9557D Pin:	1	3	5	7
Nominal value		0.75V (DAC: 0x3A)	1.5V (DAC: 0x3A)	0.7V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)	1.998V - 1.002V (+/- 498mV)	0.200V - 1.050V (+/- 500mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)	0.000V - 1.501V (0x00 - 0x74)	0.000V - 1.191V (0x00 - 0x5C)
Vref current:		+3.4mA - -3.4mA (- = sourced)	+33uA - -33uA (- = sourced)	+750uA - -528uA (- = sourced)
DAC step size:		7.69mV / step @ output	8.59mV / step @ output	9.24mV / step @ output

SYNC MASTER=K99 MLB SYNC DATE=04/08/2010

FSB/DDR3 Vref Margining

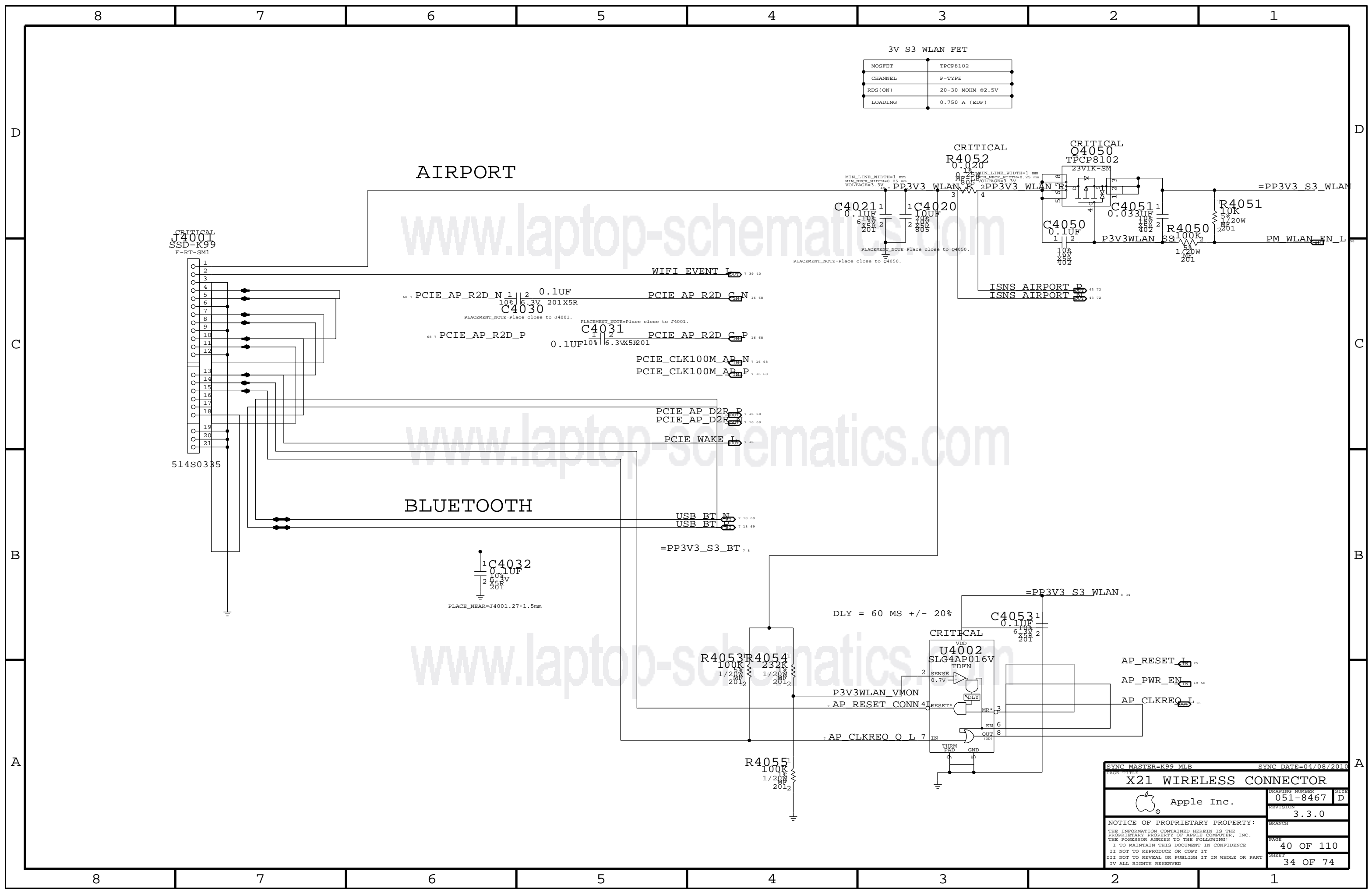
Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D

REVISION: 3.3.0

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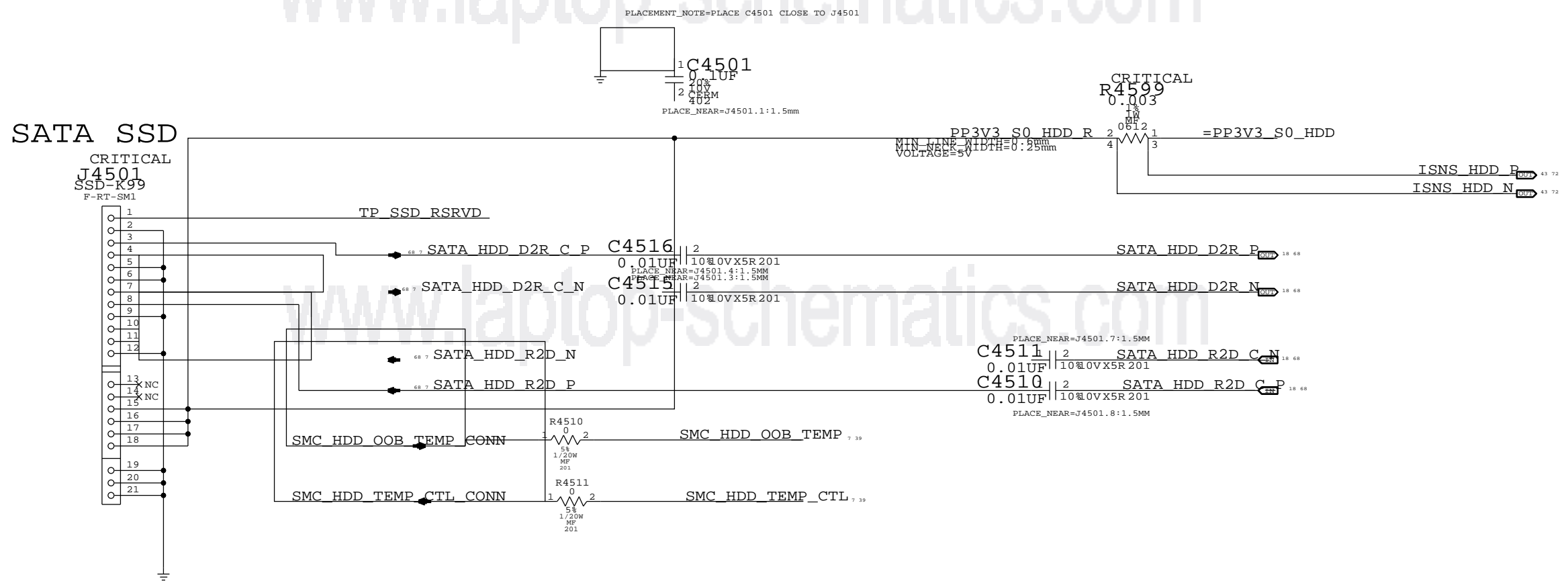
PAGE: 39 OF 110 SHEET: 33 OF 74



3V S3 WLAN FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	0.750 A (EDP)

SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
X21 WIRELESS CONNECTOR			
Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
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		PAGE	40 OF 110
		SHEET	34 OF 74

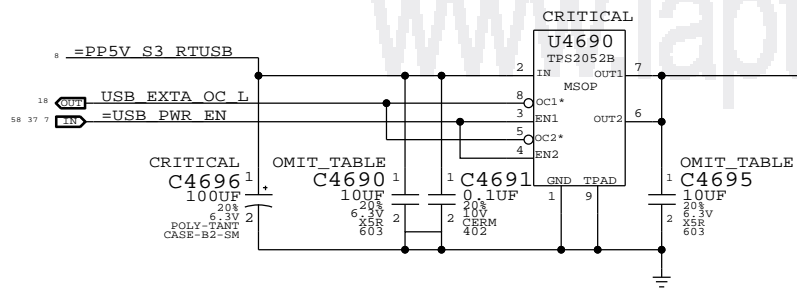
www.laptop-schematics.com



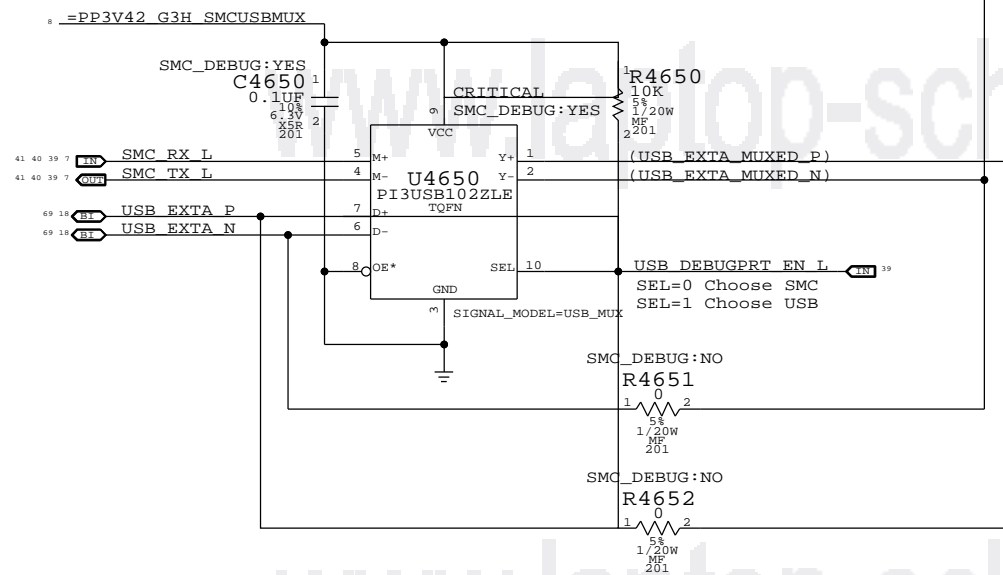
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SYNC MASTER=K99_MLB		SYNC DATE=04/08/2010	
PAGE TITLE SATA CONNECTOR			
DRAWING NUMBER 051-8467		SIZE D	
REVISION 3.3.0		BRANCH	
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		SHEET 35 OF 74	

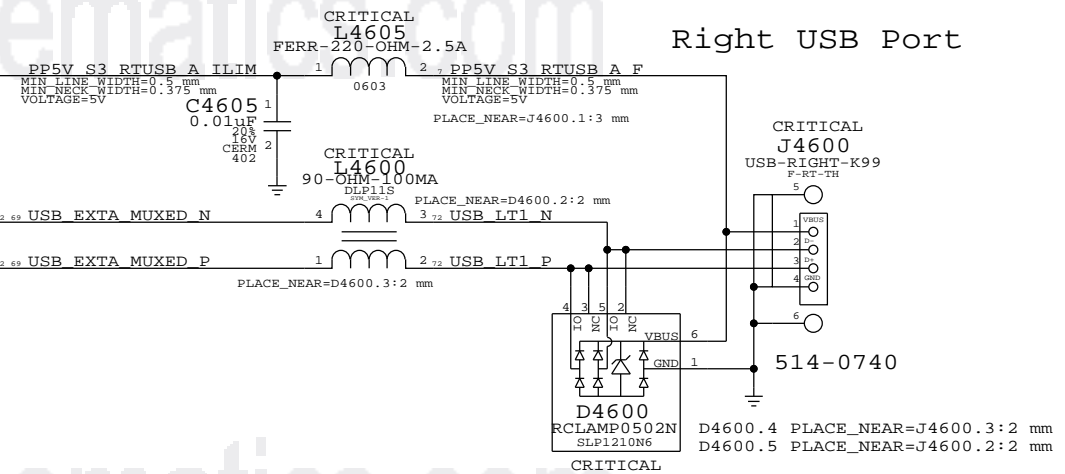
Port Power Switch



USB/SMC Debug Mux

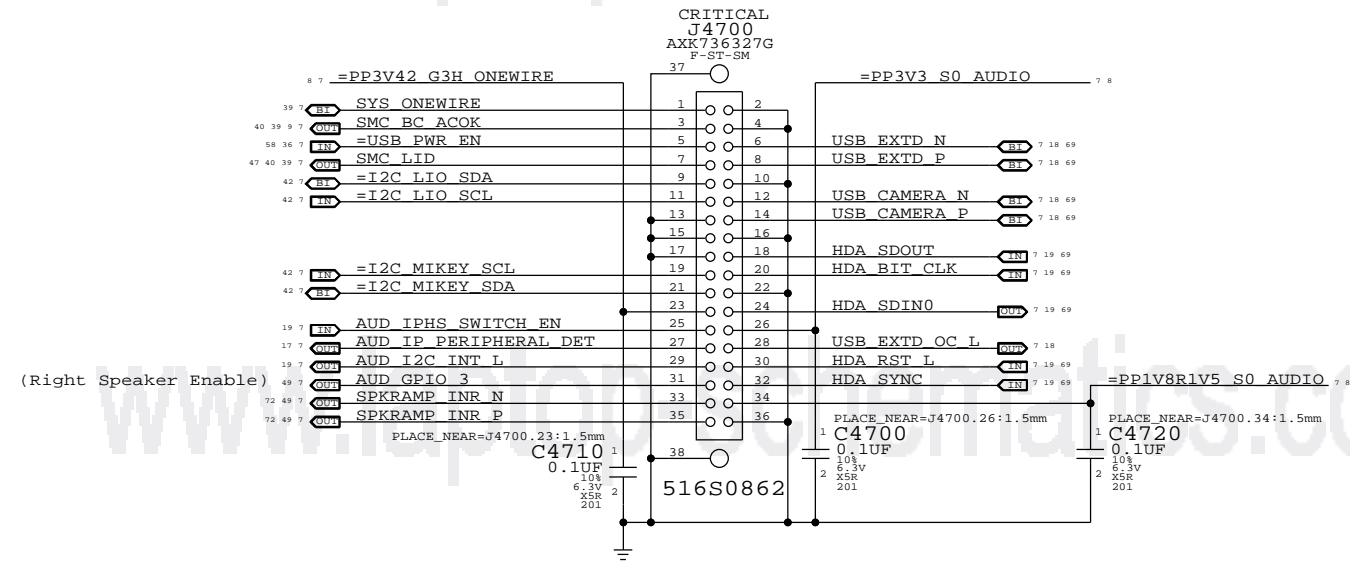


Right USB Port



SYNC MASTER=K99 MLB		SYNC DATE=03/01/2010	
External USB Connectors			
Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
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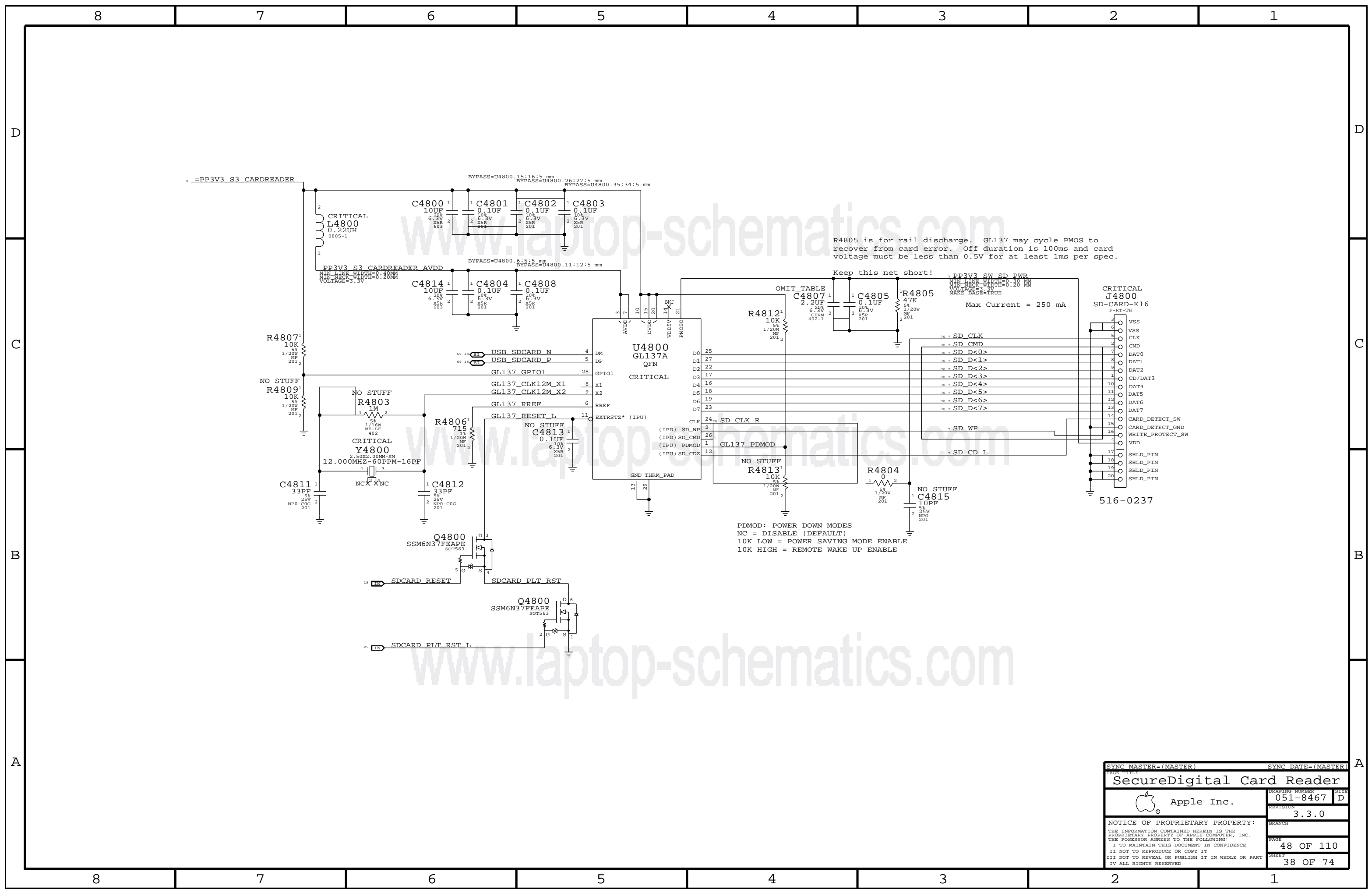
www.laptop-schematics.com



(Right Speaker Enable)

www.laptop-schematics.com

SYNC MASTER=(MASTER)		SYNC DATE=(MASTER)	
PAGE TITLE Left I/O (LIO) Connector			
DRAWING NUMBER 051-8467		SIZE D	
REVISION 3.3.0		BRANCH	
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PAGE 47 OF 110		SHEET 37 OF 74	



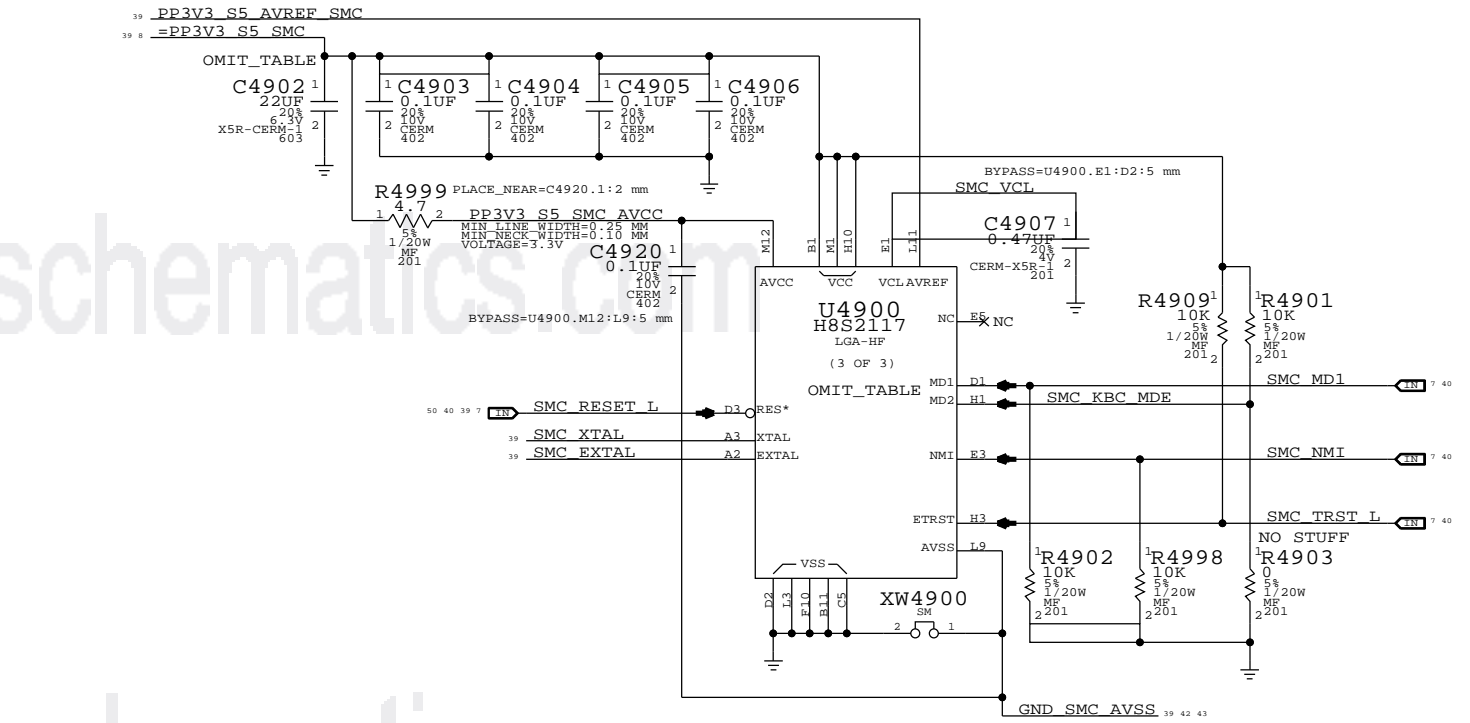
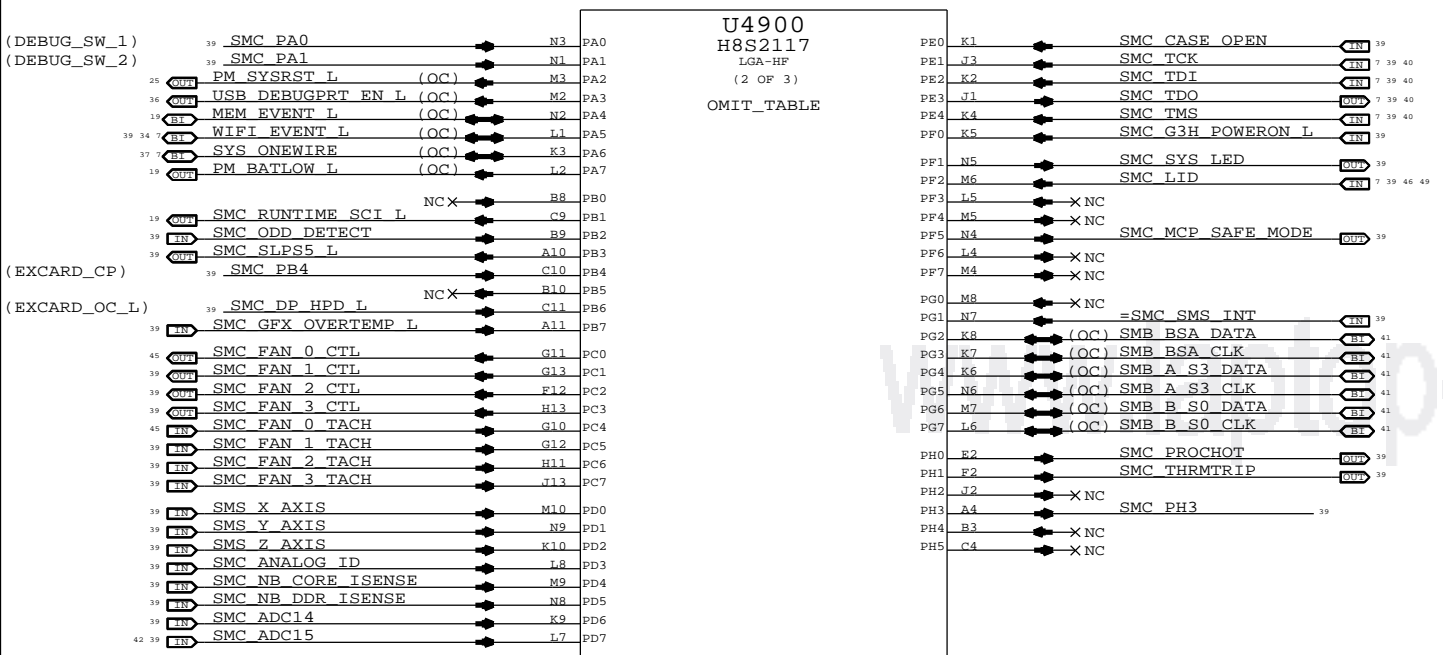
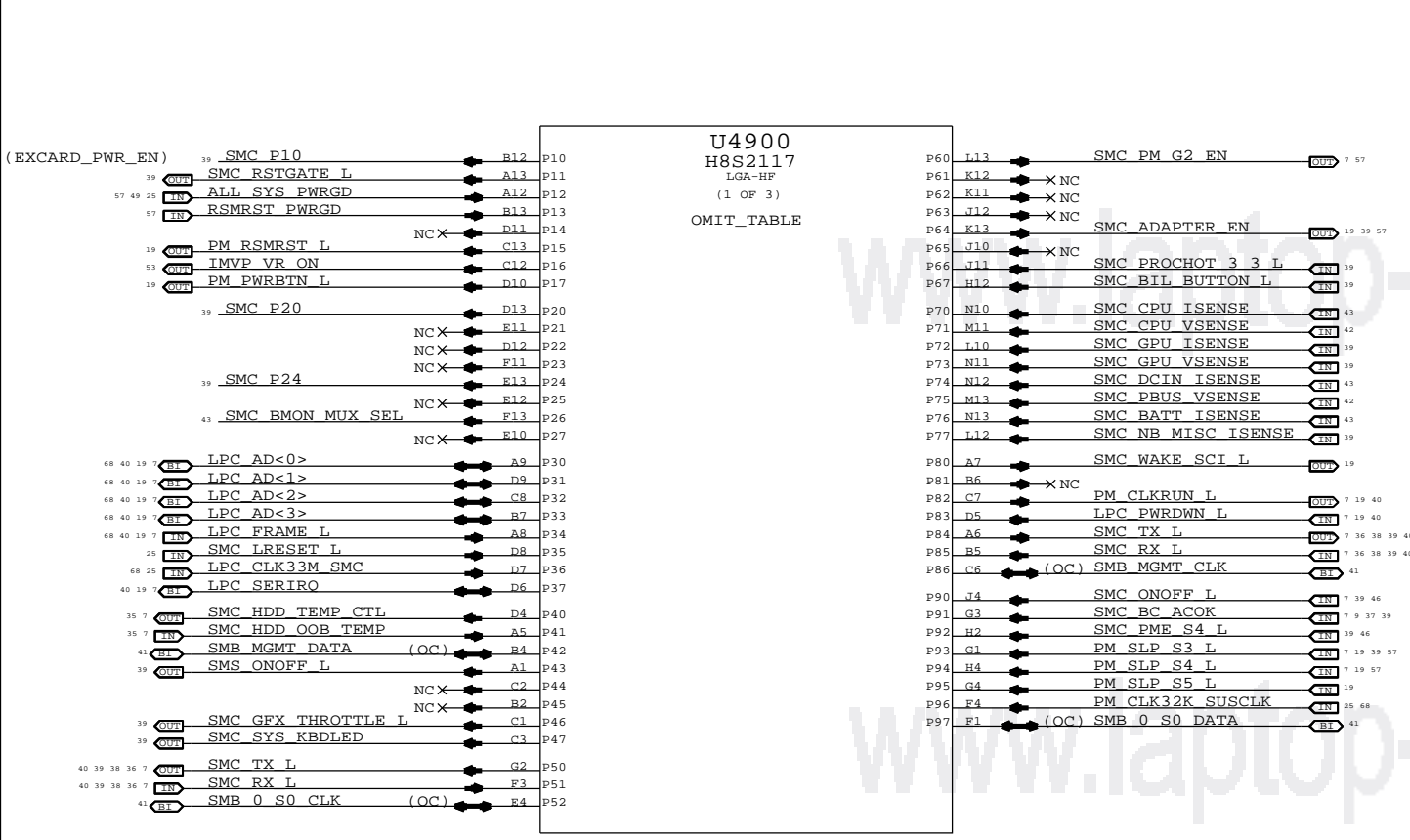
R4805 is for rail discharge. GL137 may cycle PMOS to recover from card error. Off duration is 100ms and card voltage must be less than 0.5V for at least 1ms per spec.

Keep this net short!
 PP3V3 SW SD PWR
 Max Current = 250 mA

PDMOD: POWER DOWN MODES
 NC = DISABLE (DEFAULT)
 10K LOW = POWER SAVING MODE ENABLE
 10K HIGH = REMOTE WAKE UP ENABLE

SYNC MASTER=(MASTER)		SYNC DATE=(MASTER)	
SecureDigital Card Reader			
Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
		3.3.0	
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NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

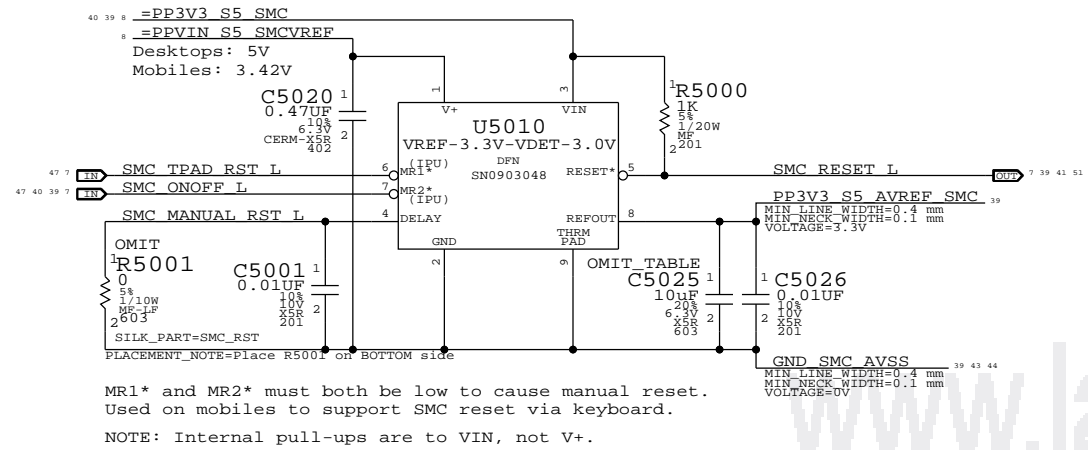


NOTE: SMS Interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

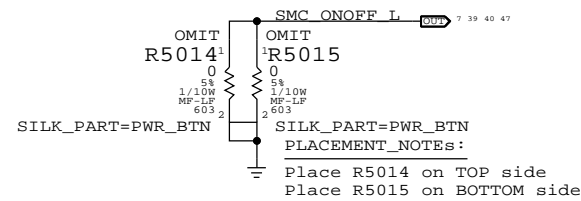
H8S2117-R:
(SMC_PECI)
(SMC_PECI_VREF)
(SMC_PECI_VSTP)

SYNC MASTER=K16 MLB		SYNC DATE=06/01/2010	
SMC			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8467	D
		REVISION	
		3.3.0	
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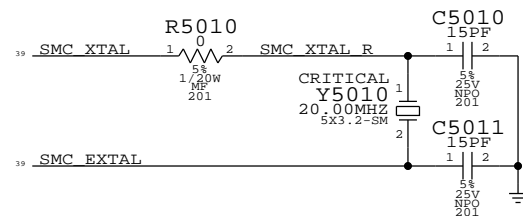
SMC Reset "Button", Supervisor & AVREF Supply



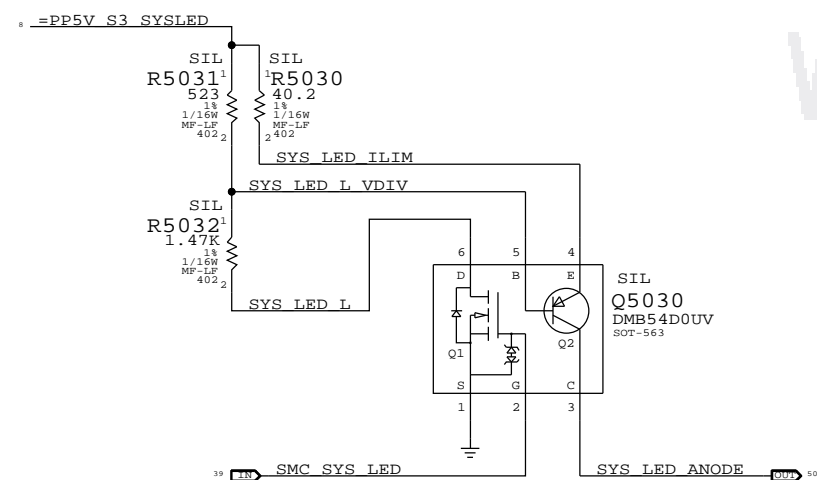
Debug Power "Buttons"



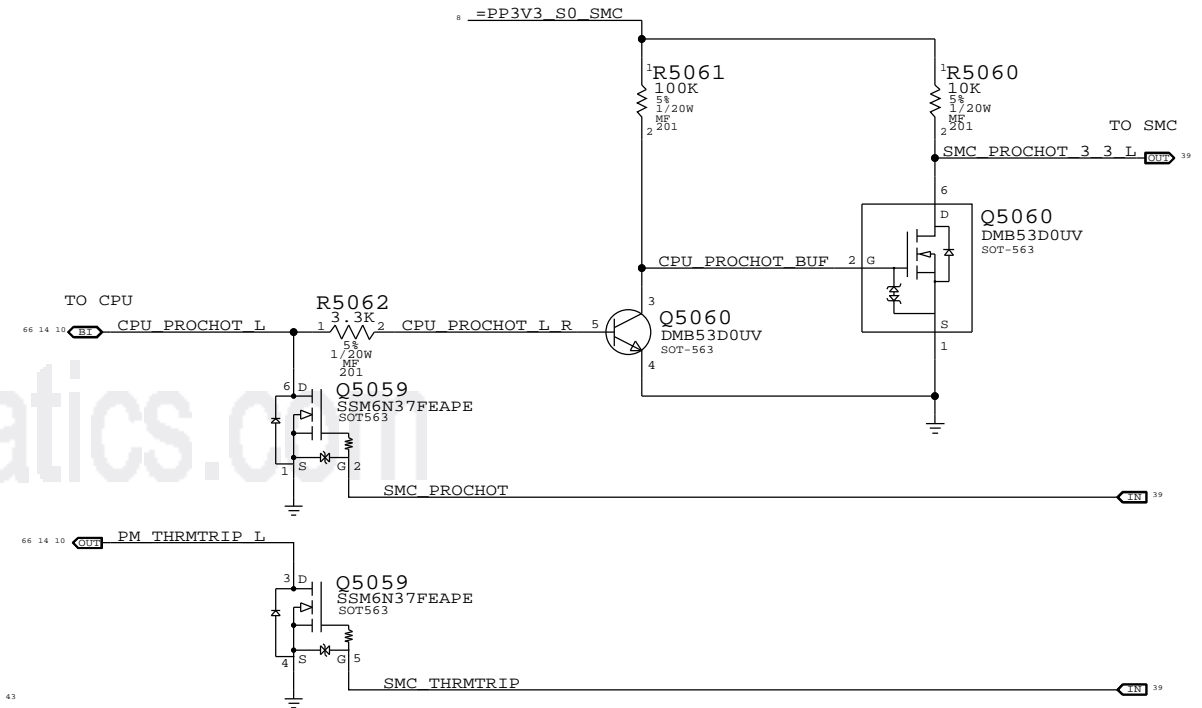
SMC Crystal Circuit



System (Sleep) LED Circuit

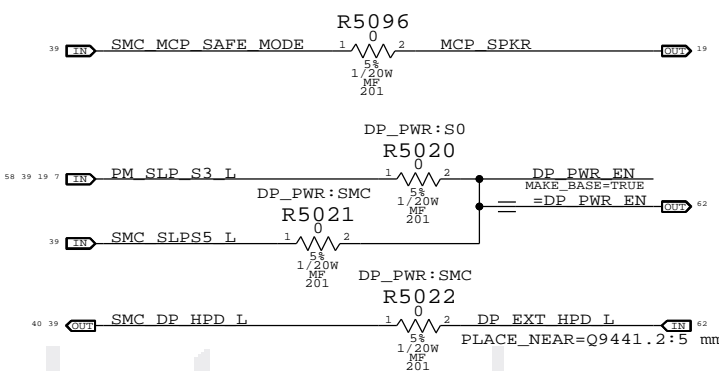


SMC FSB to 3.3V Level Shifting



SMC Aliases

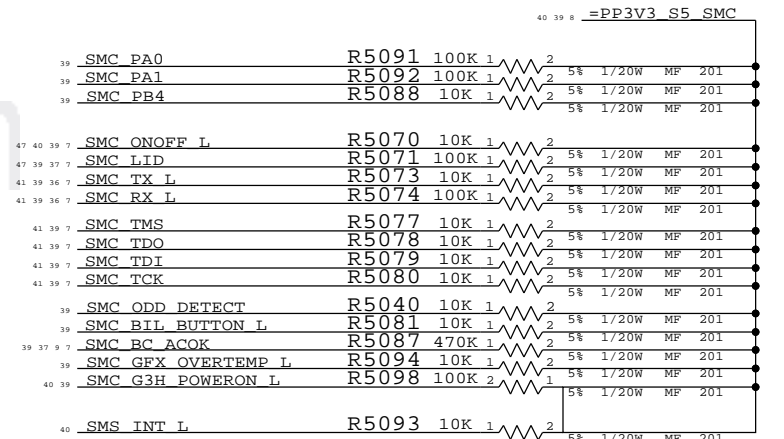
SMC LCDCLKT ISENSE	==	SMS X AXIS
SMC WLAN ISENSE	==	SMS Y AXIS
SMC HDD ISENSE	==	SMS Z AXIS
SMC CSREG ISENSE	==	SMC ADC14
SMC LCDCLKT VSENSE	==	SMC ADC15
SMC MCP CORE ISENSE	==	SMC NB CORE ISENSE
SMC MCP DDR ISENSE	==	SMC NB DDR ISENSE
SMC 1V5S3 ISENSE	==	SMC NB MISC ISENSE
TP SMC ANALOG ID	==	SMC ANALOG ID
TP SMC GPU ISENSE	==	SMC GPU ISENSE
SMC MCP VSENSE	==	SMC GPU VSENSE
SMC GFX THROTTLE L	==	SMC IG THROTTLE L
SMS INT L	==	SMC SMS INT
MCP WAKE REO L	==	SMC G3H POWERON L



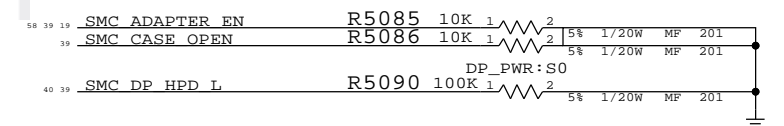
Unused Pins

SMS ONOFF L	==	TP SMS ONOFF L
SMC SYS KBDLED	==	TP SMC SYS KBDLED
SMC FAN 1 CTL	==	TP SMC FAN 1 CTL
TP SMC FAN 1 TACH	==	SMC FAN 1 TACH
SMC FAN 2 CTL	==	NC SMC FAN 2 CTL
NC SMC FAN 2 TACH	==	SMC FAN 2 TACH
SMC FAN 3 CTL	==	NC SMC FAN 3 CTL
NC SMC FAN 3 TACH	==	SMC FAN 3 TACH
SMC RSTGATE L	==	TP SMC RSTGATE L
SMC P10	==	TP SMC P10
SMC P20	==	TP SMC P20
SMC P24	==	TP SMC P24
SMC PH3	==	TP SMC PH3

SMC Pull-ups



SMC Pull-downs



SYNC MASTER=(K99 MLB) SYNC DATE=(03/01/2010)

SMC Support

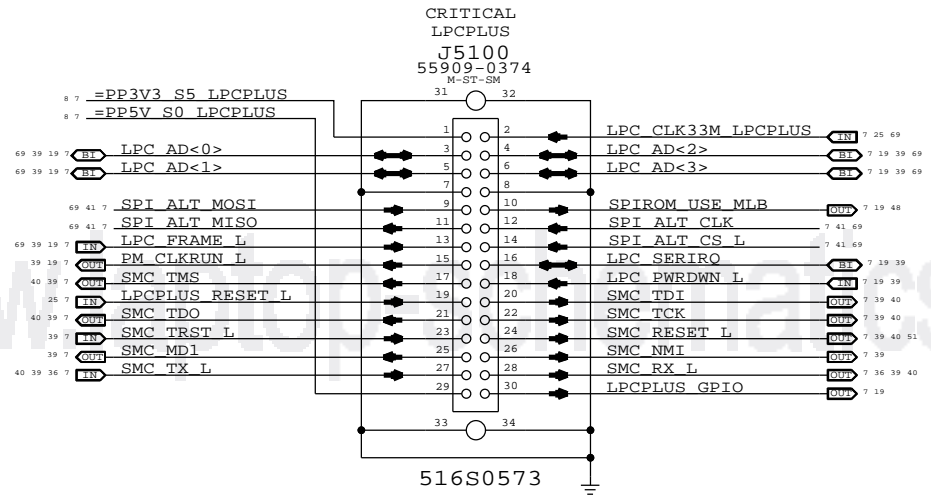
Apple Inc.

Drawing Number: 051-8467
Revision: 3.3.0

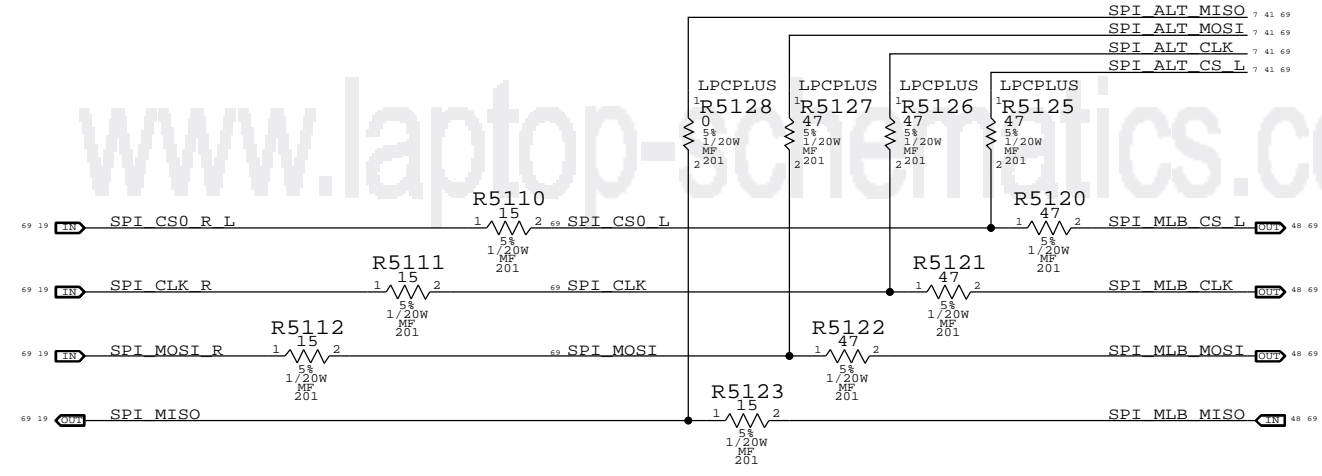
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Sheet: 40 OF 74

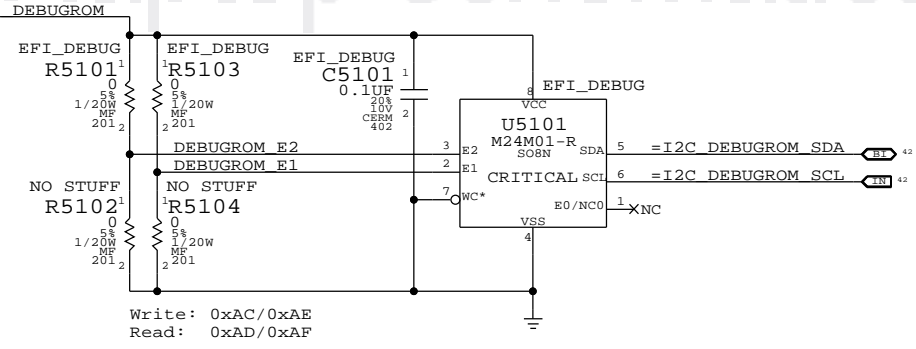
LPC+SPI Connector



SPI Bus Series Termination

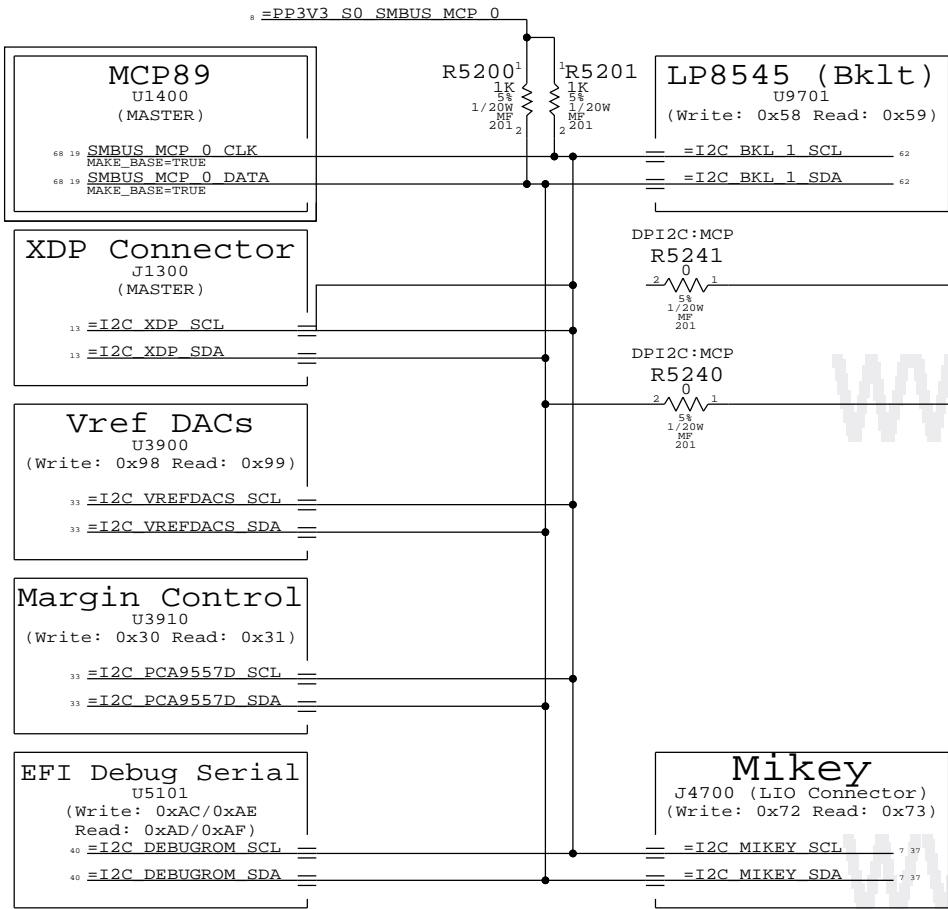


EFI Debug ROM

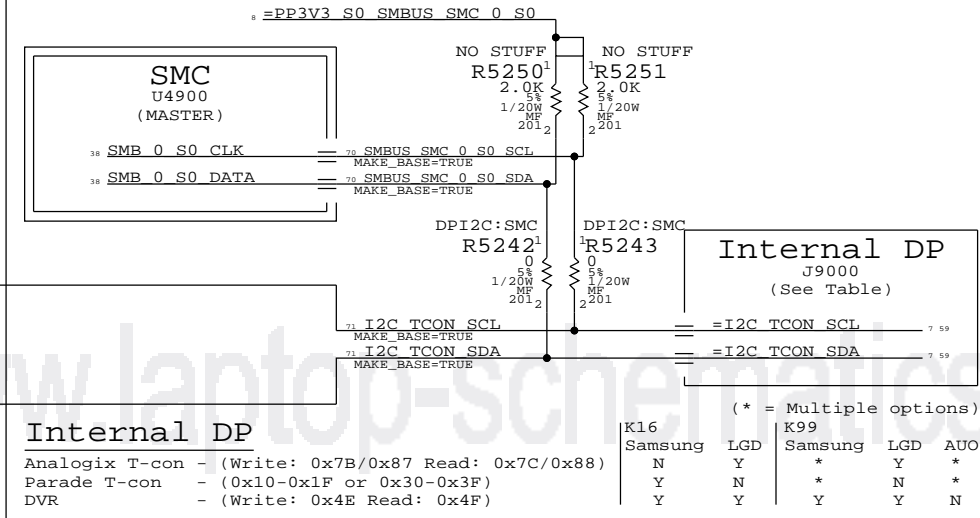


SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
LPC+SPI Debug Connector			
Apple Inc.		DRAWING NUMBER	SIZE
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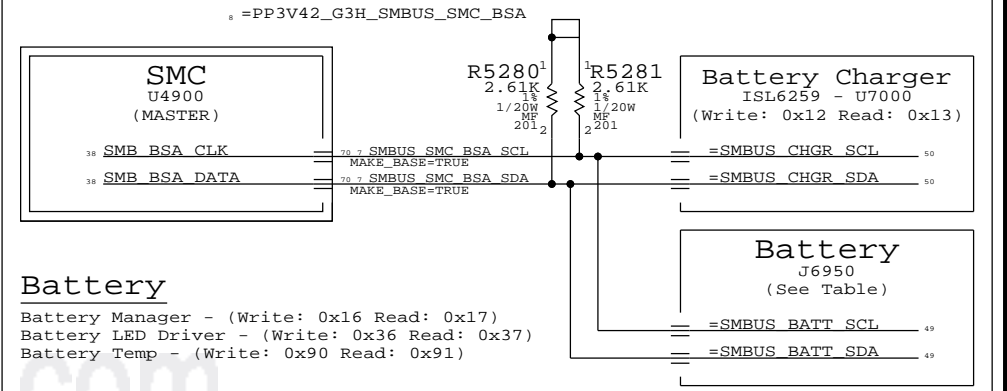
MCP89 SMBus "0" Connections



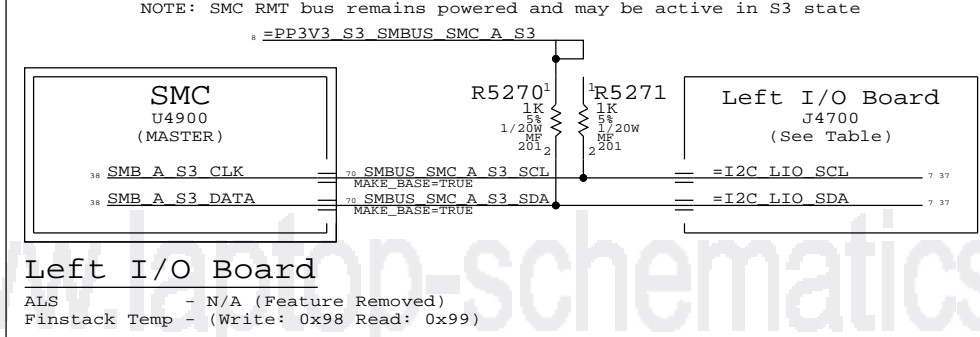
SMC "0" SMBus Connections



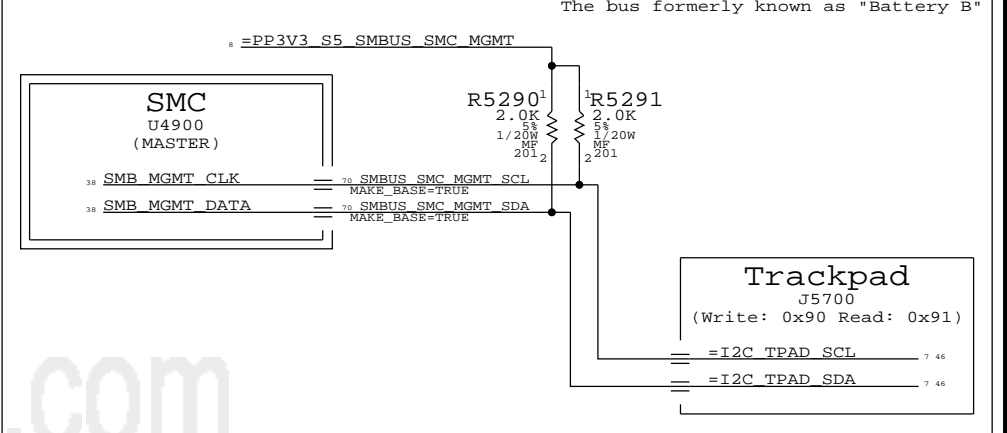
SMC "Battery A" SMBus Connections



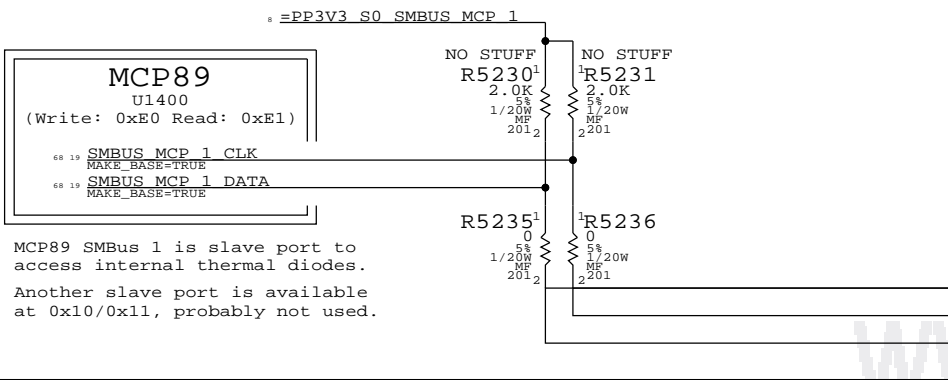
SMC "A" SMBus Connections



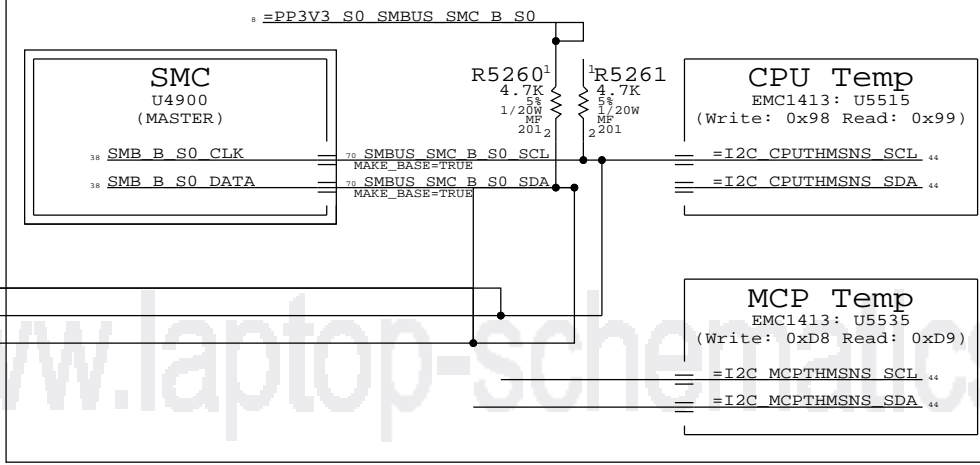
SMC "Management" SMBus Connections



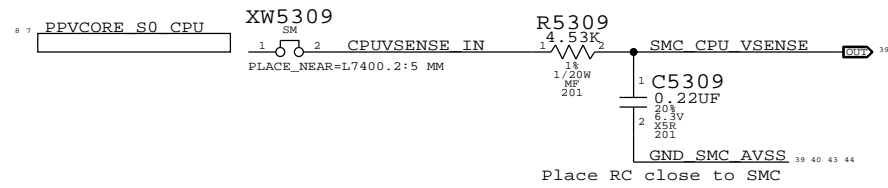
MCP89 SMBus "1" Connections



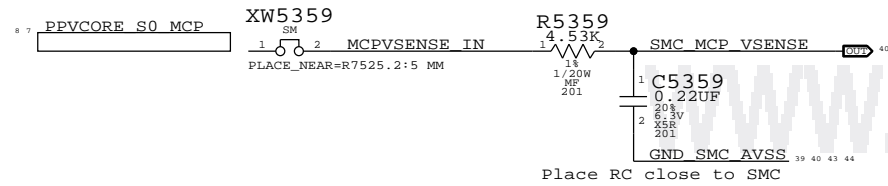
SMC "B" SMBus Connections



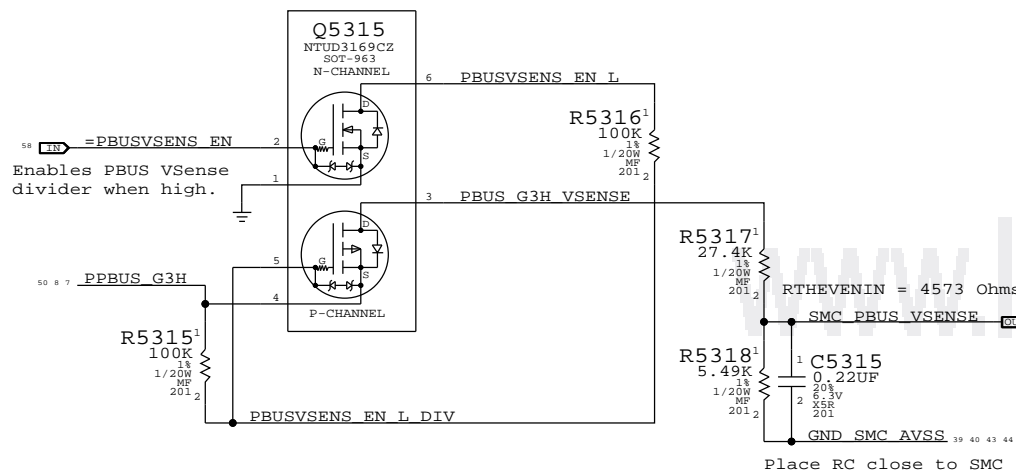
CPU Voltage Sense / Filter



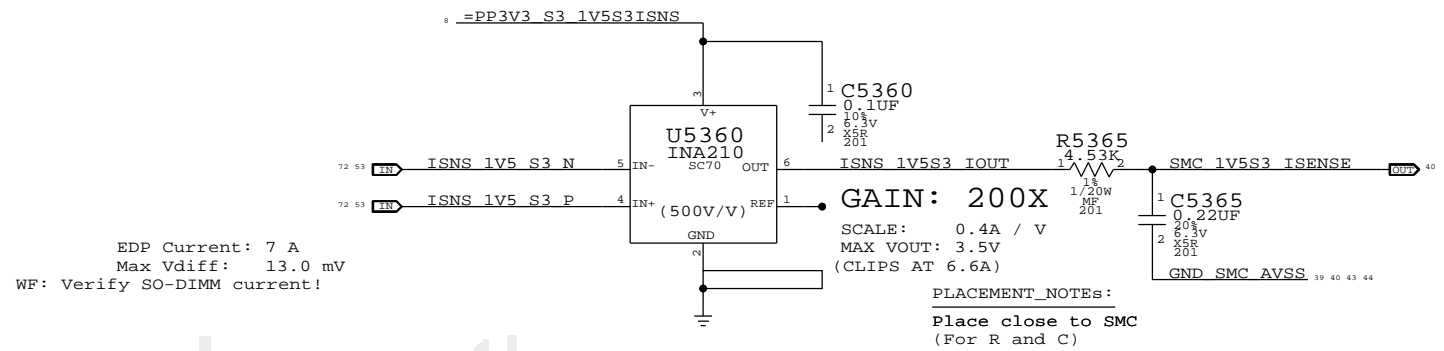
MCP Voltage Sense / Filter



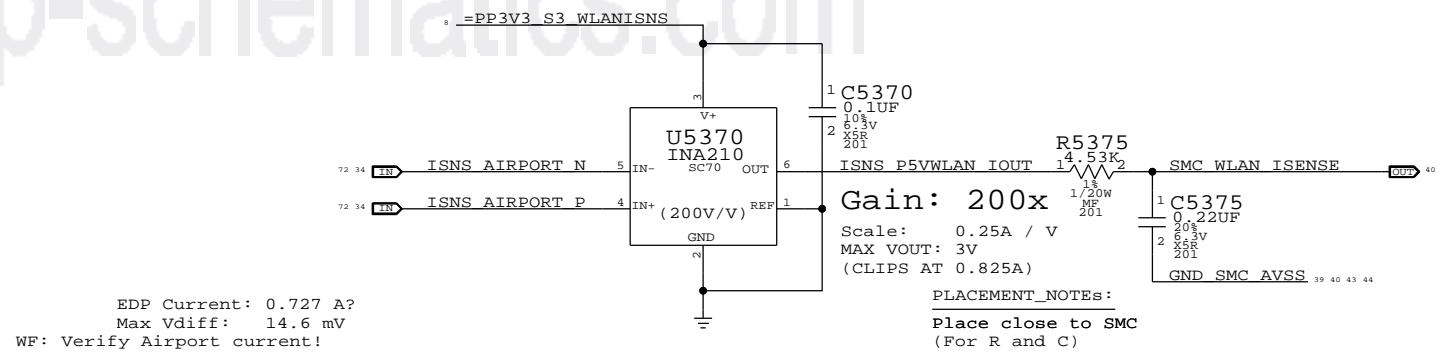
PBUS Voltage Sense Enable & Filter



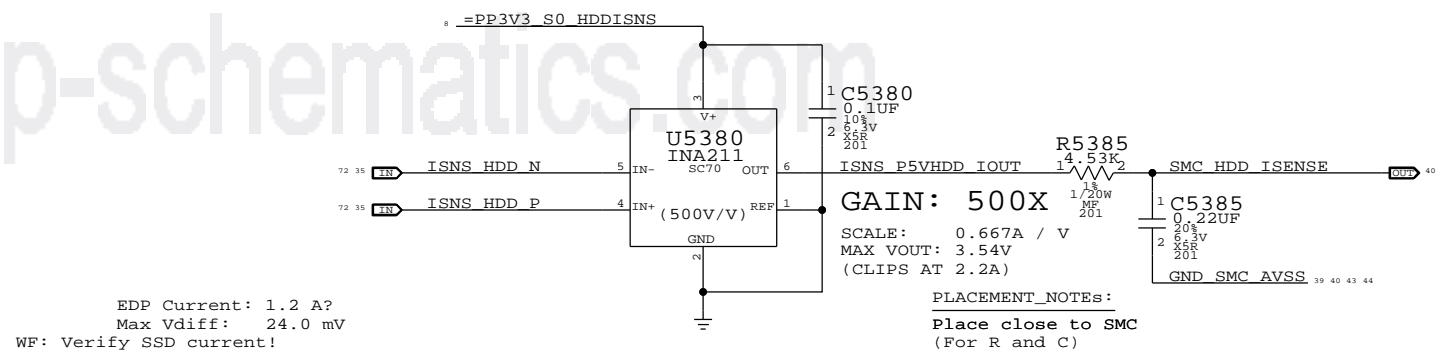
DDR3 1V5R1V35 Current Sense / Filter



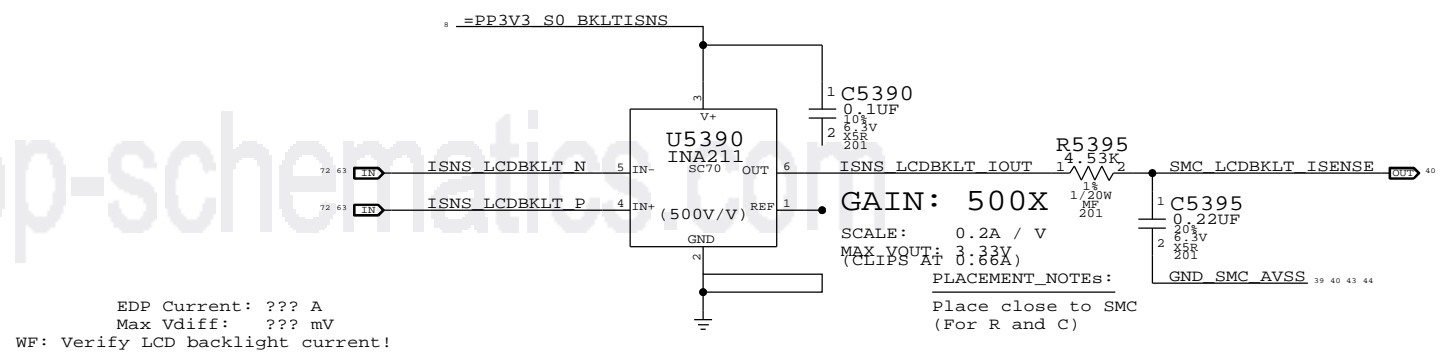
AirPort Current Sense / Filter



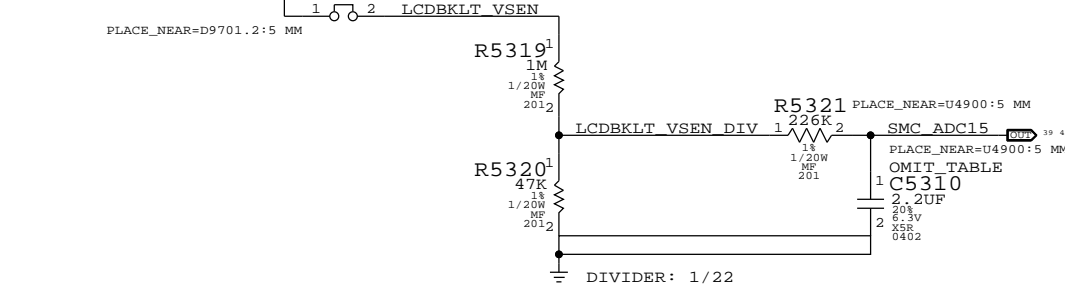
HDD Current Sense / Filter



LCD Backlight Driver Input Current Sense / Filter

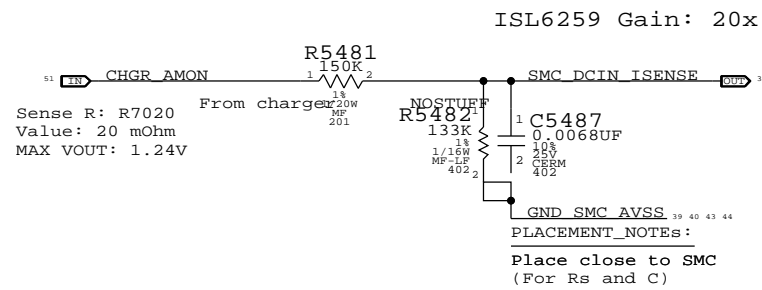


PPVOUT SW LCDBKLT Voltage Sense / Filter

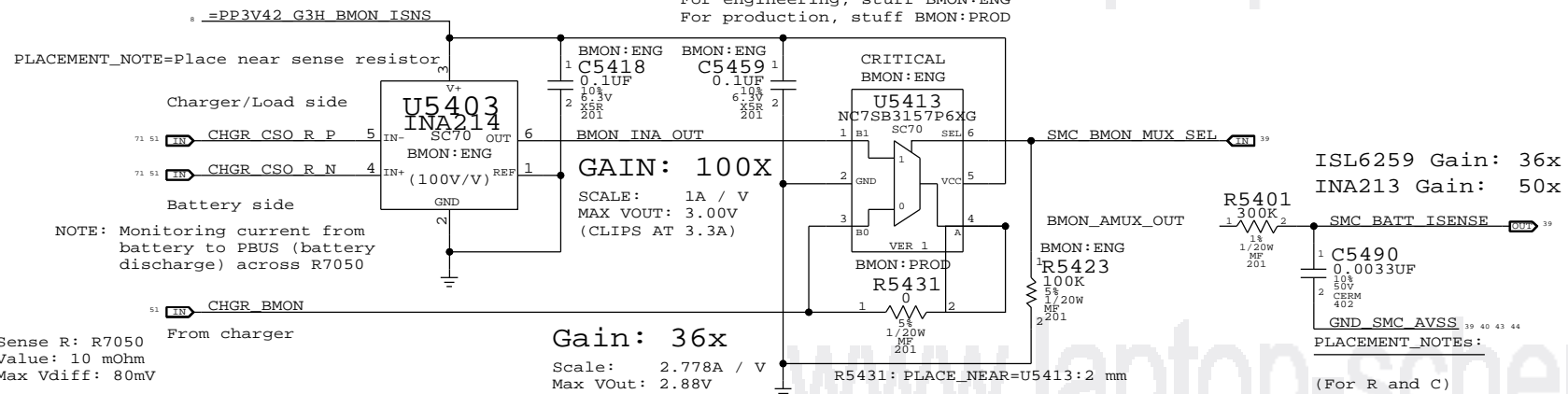


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Voltage & Current Sensing		051-8467	
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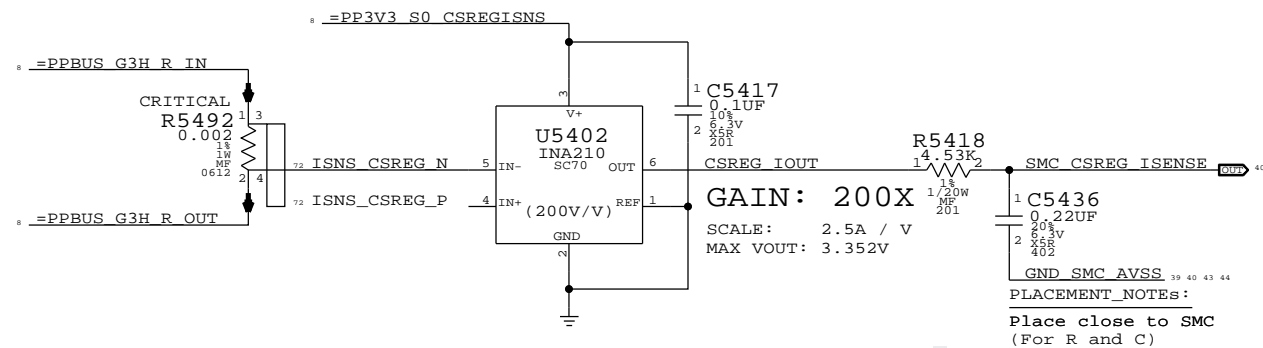
DCIN (AMON) Current Sense, RMUX & Filter



Battery (BMON) Current Sense, MUX & Filter

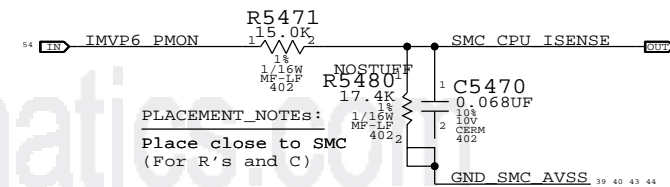


Chipset Regulators High-Side Current Sense / Filter

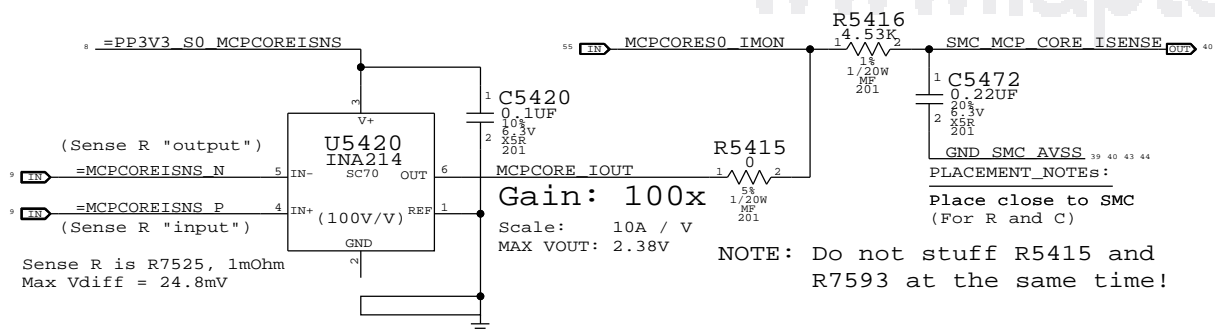


VERIFY ALL RESISTOR AND GAINS

CPU VCore Load Side Current Sense / Filter

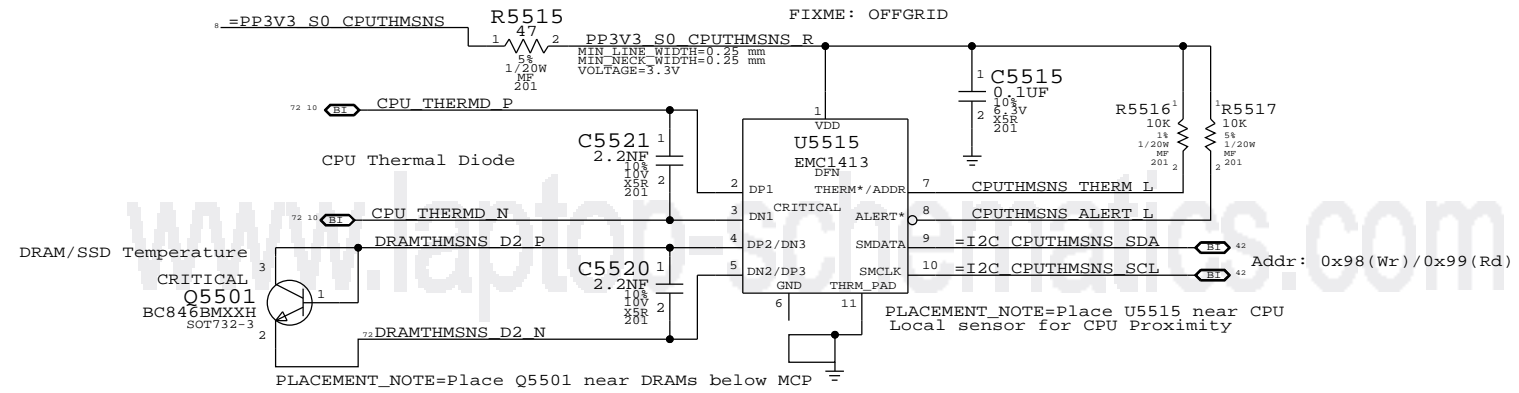


MCP VCore Current Sense Filter

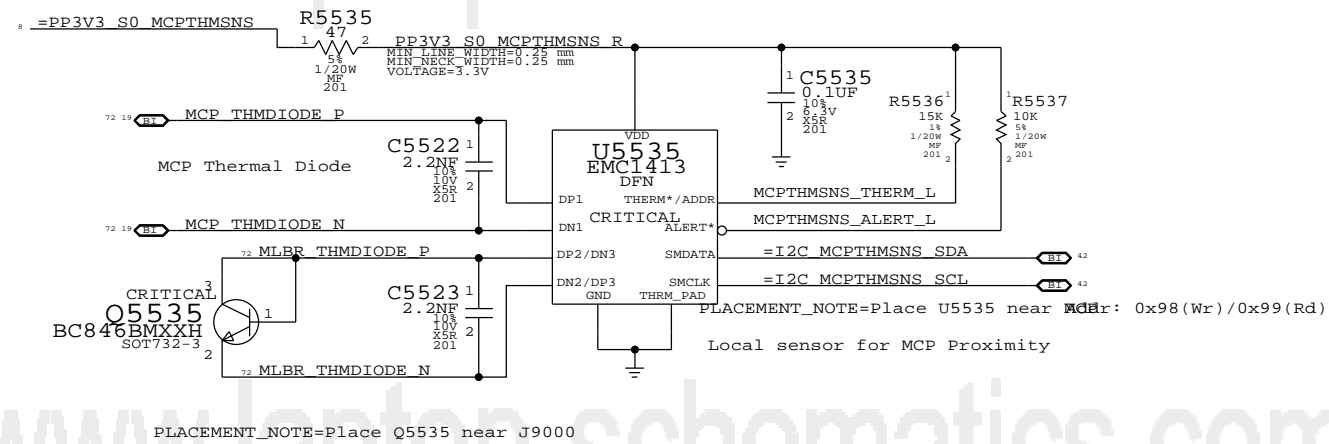


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Current Sensing			
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		051-8467	D
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CPU T-Diode Thermal Sensor



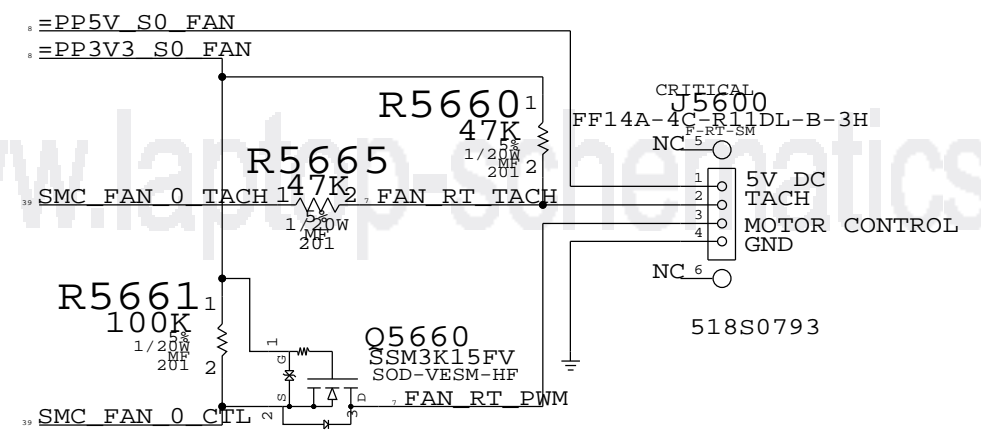
MCP T-Diode Thermal Sensor



SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
Thermal Sensors			
Apple Inc.		DRAWING NUMBER	051-8467
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FAN CONNECTOR

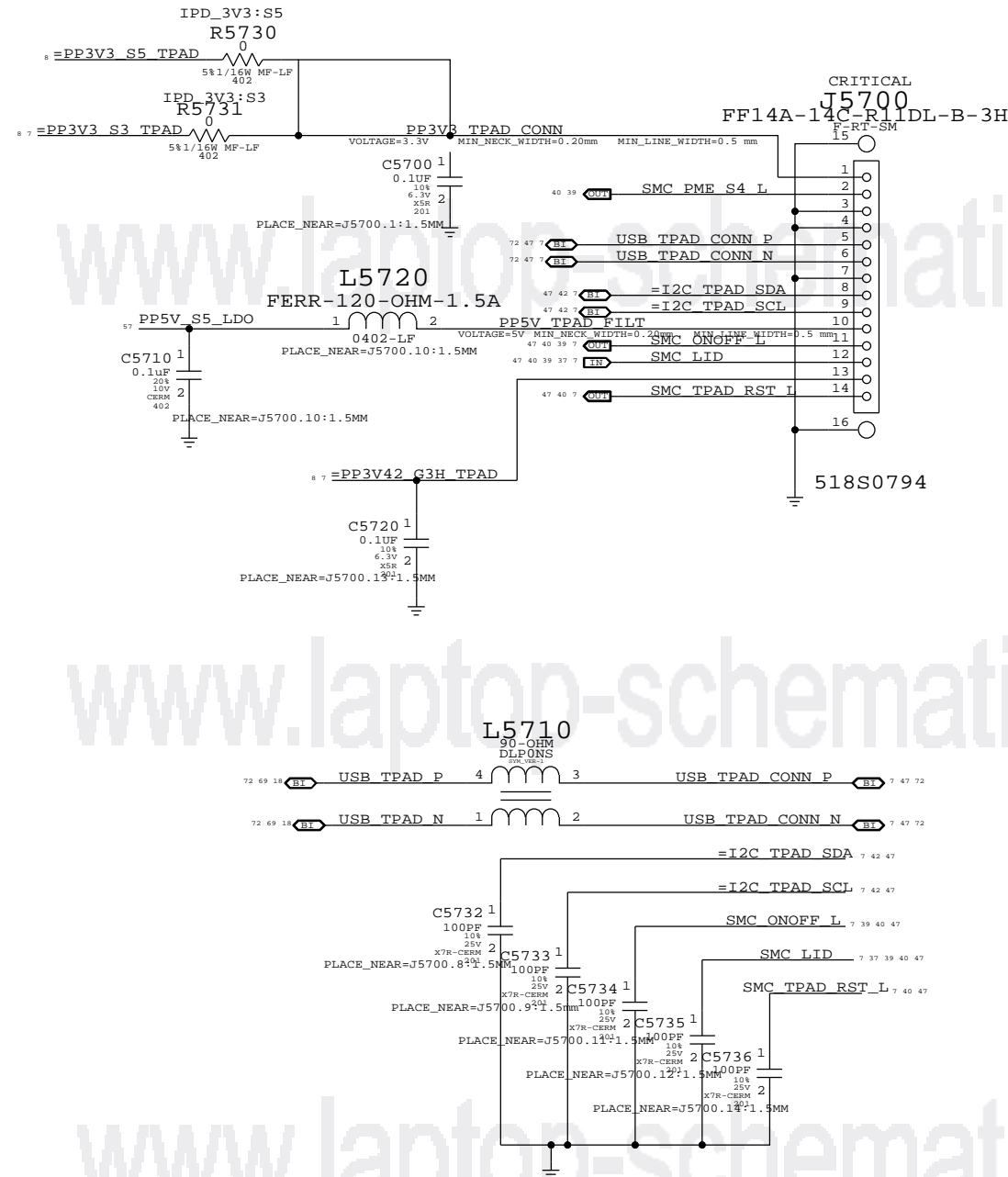


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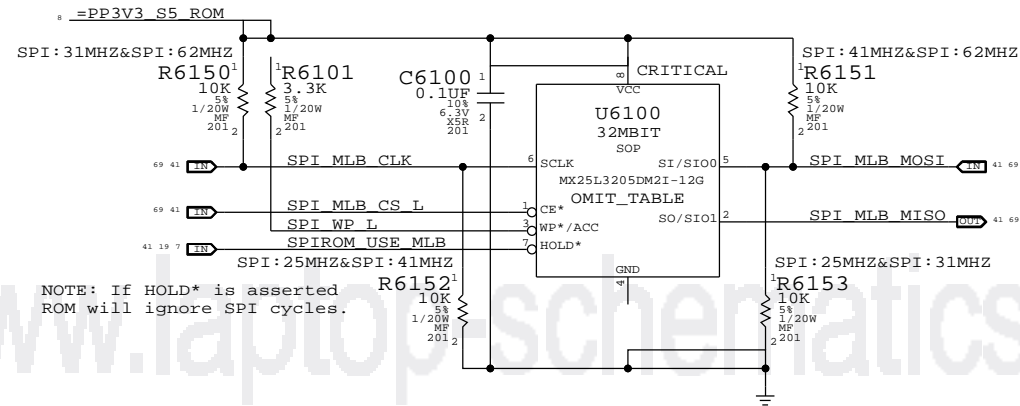
SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE			
Fan			
Apple Inc.		DRAWING NUMBER	051-8467
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IPD Flex Connector



SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
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MCP89 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
41.7 MHz	1	0
62.5 MHz	1	1

NOTE: 42 & 62 MHz use FAST_READ command.

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SYNC MASTER=K99 MLB SYNC DATE=04/08/2010

SPI ROM

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D

REVISION: 3.3.0

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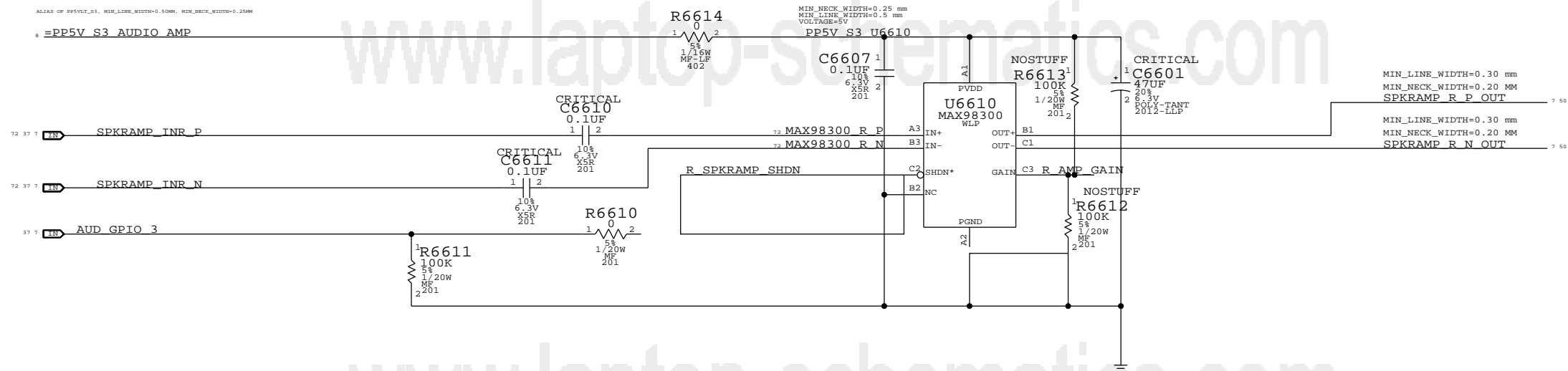
PAGE: 61 OF 110
 SHEET: 48 OF 74

SPEAKER AMPLIFIERS

APN: 353S2888

SPEAKER LOWPASS 80 HZ < FC < 132 HZ

GAIN 6DB



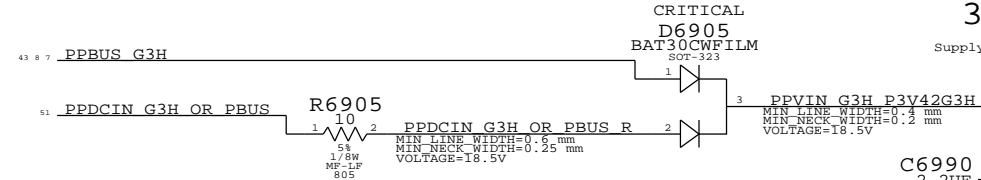
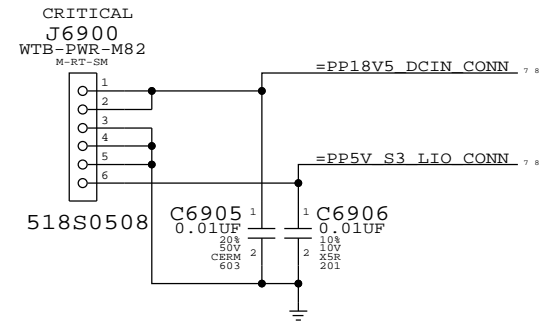
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www.laptop-schematics.com

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SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE AUDIO: SPEAKER AMP			
DRAWING NUMBER 051-8467		SIZE D	
REVISION 3.3.0		BRANCH	
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PAGE 66 OF 110		SHEET 49 OF 74	

MLB to LIO Power Cable Connector



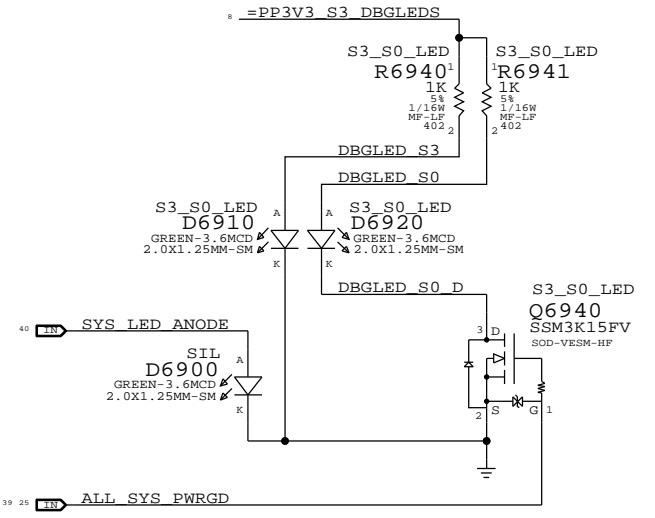
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

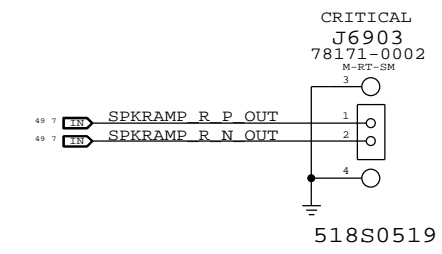
Vout = 3.425V
60MA MAX OUTPUT
(Switcher limit)

$$V_{out} = 1.25V * (1 + R_a / R_b)$$

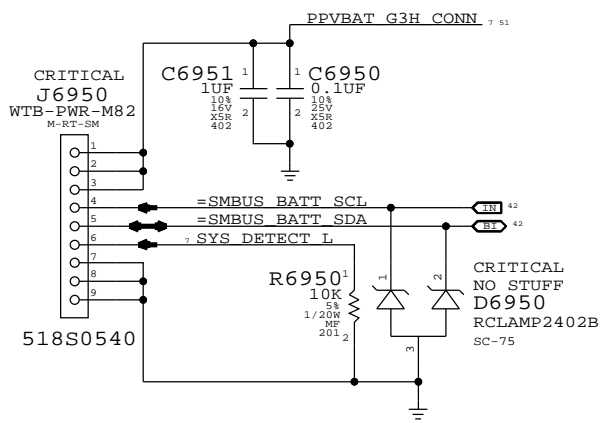
Debug LEDs
(For development only)



Right Speaker Connector



K16-Specific
Battery Connector

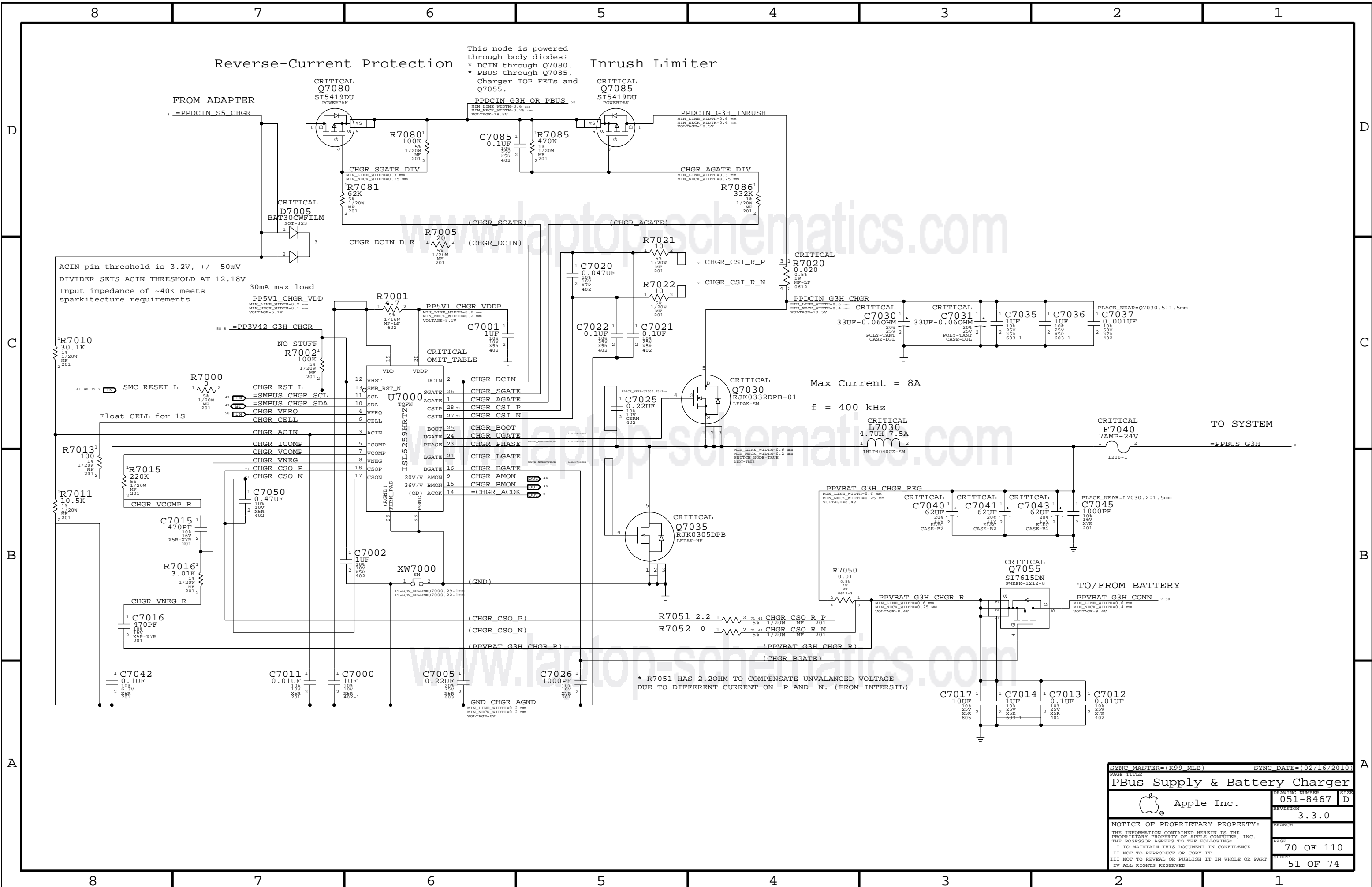


SYNC MASTER=(MASTER)		SYNC DATE=(MASTER)	
DC-In & Battery Connectors			
Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
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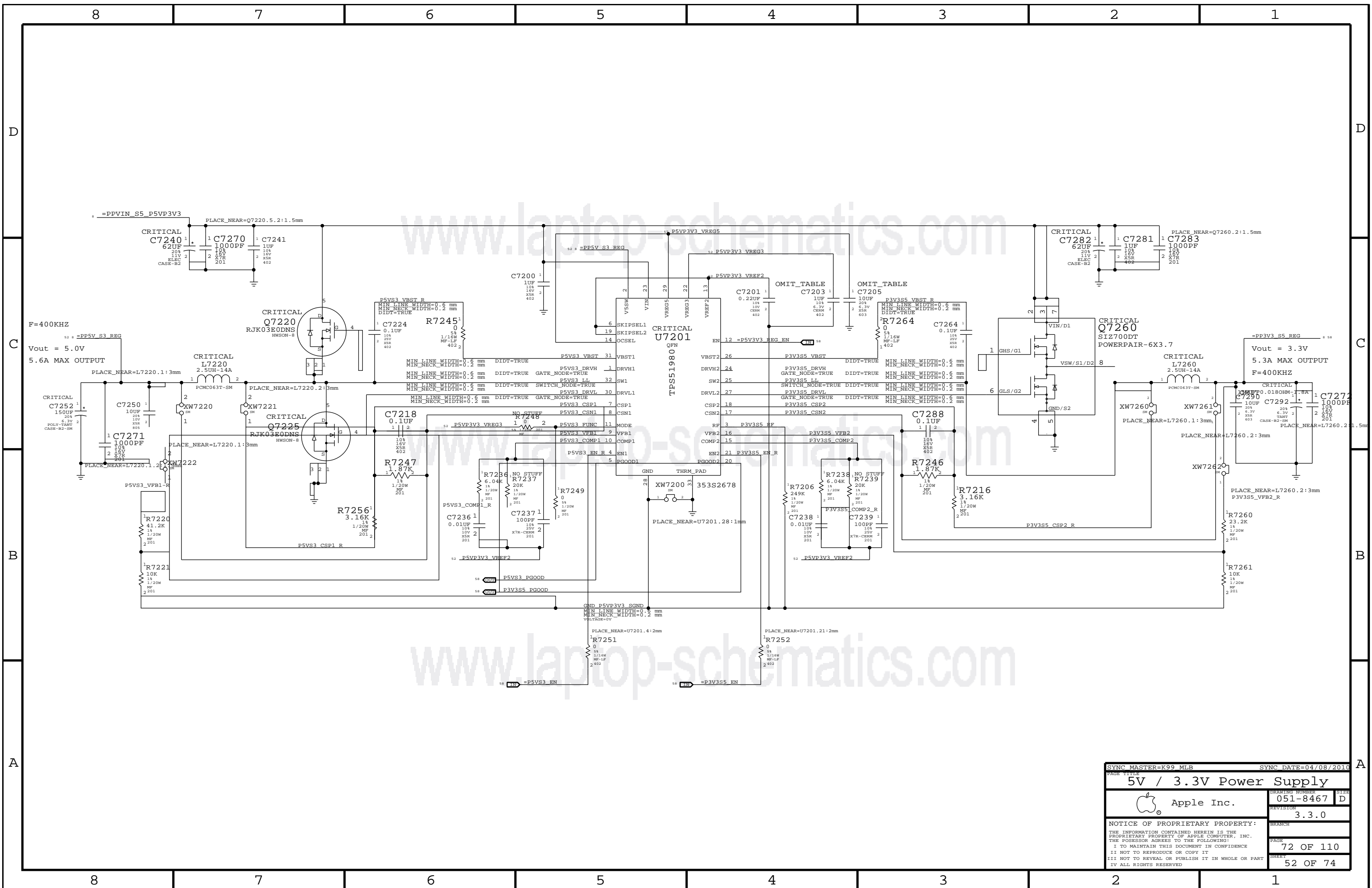
Reverse-Current Protection

Inrush Limiter

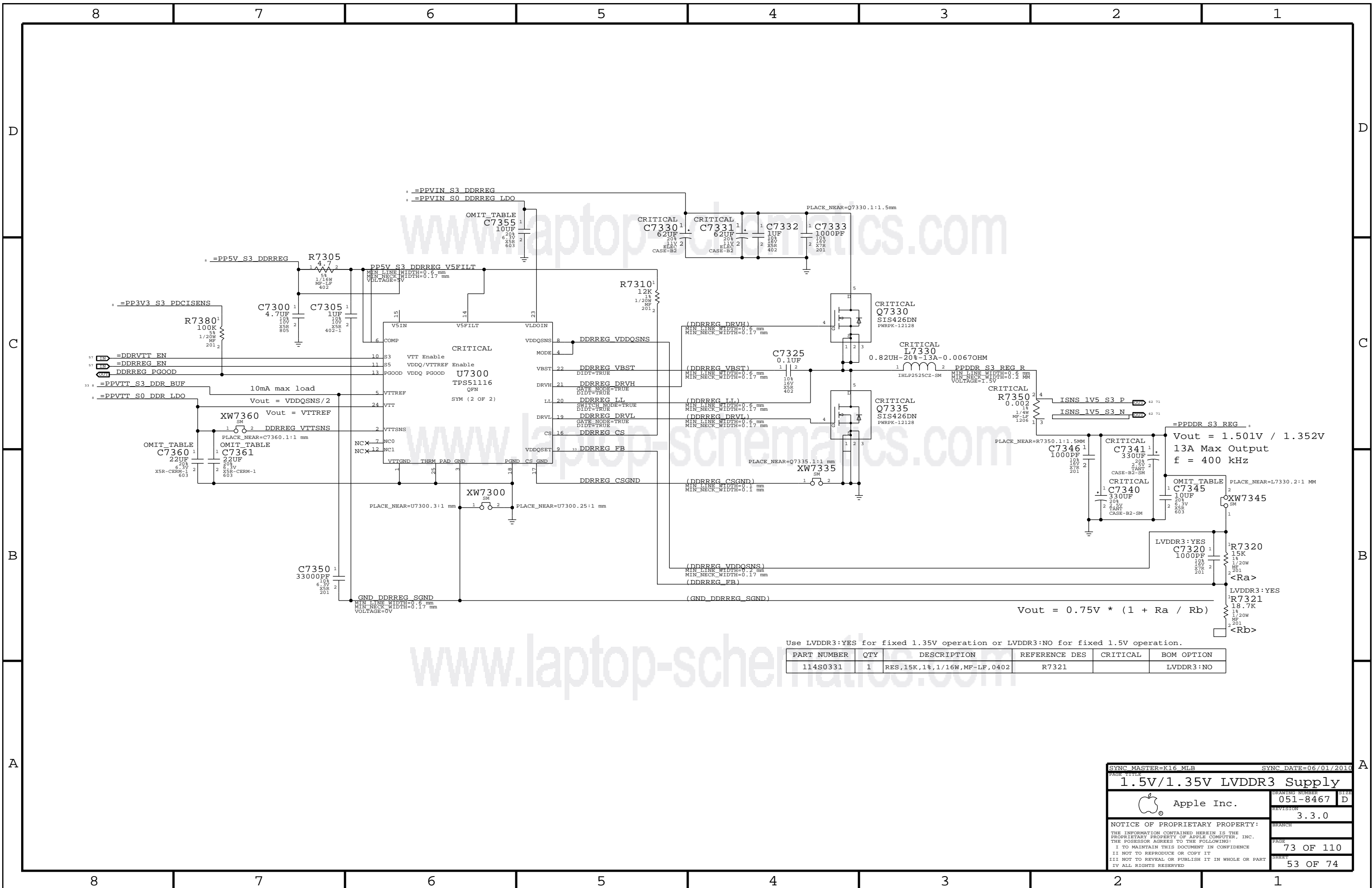
This node is powered through body diodes:
 * DCIN through Q7080.
 * PBUS through Q7085, Charger TOP FETs and Q7055.



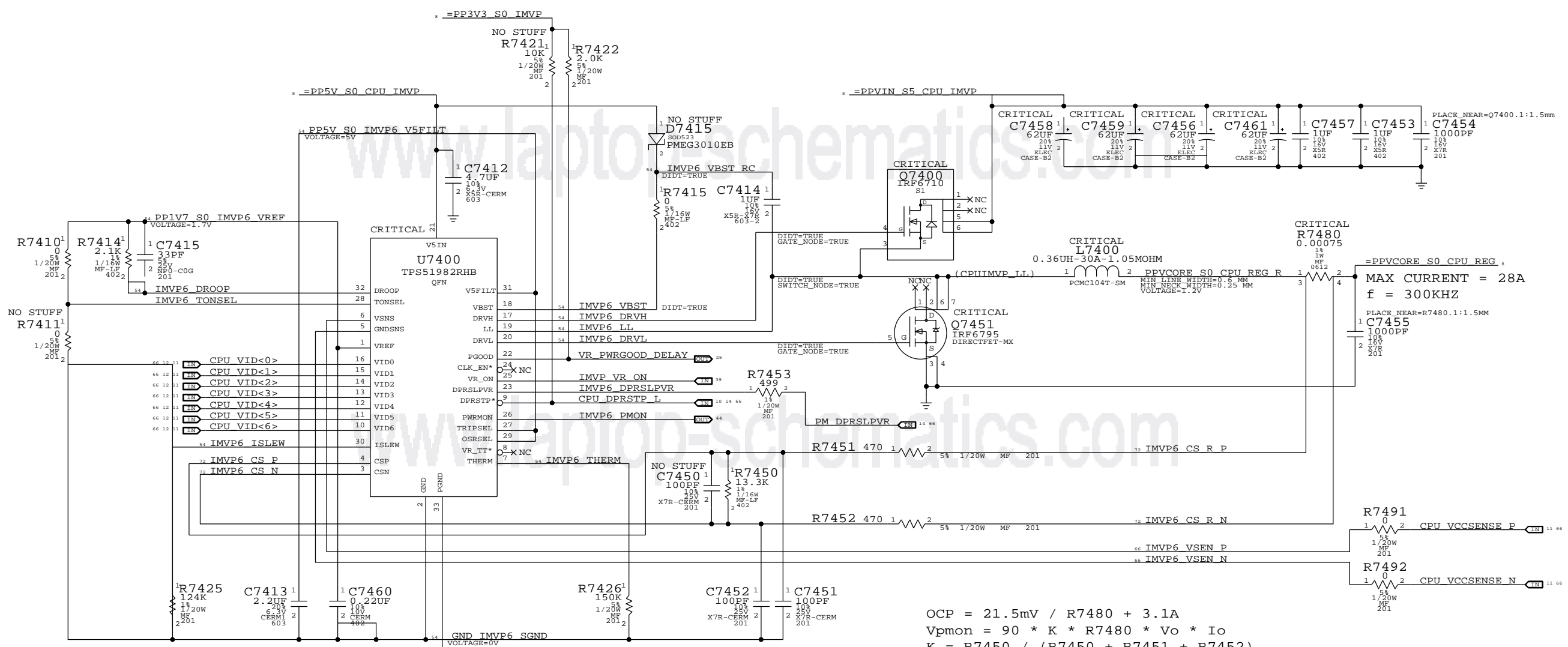
SYNC MASTER=(K99 MLB)		SYNC DATE=(02/16/2010)	
PAGE TITLE PBus Supply & Battery Charger			
Apple Inc.		DRAWING NUMBER 051-8467	SIZE D
		REVISION 3.3.0	
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		PAGE 70 OF 110	SHEET 51 OF 74



SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
5V / 3.3V Power Supply			
Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
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		SHEET	52 OF 74



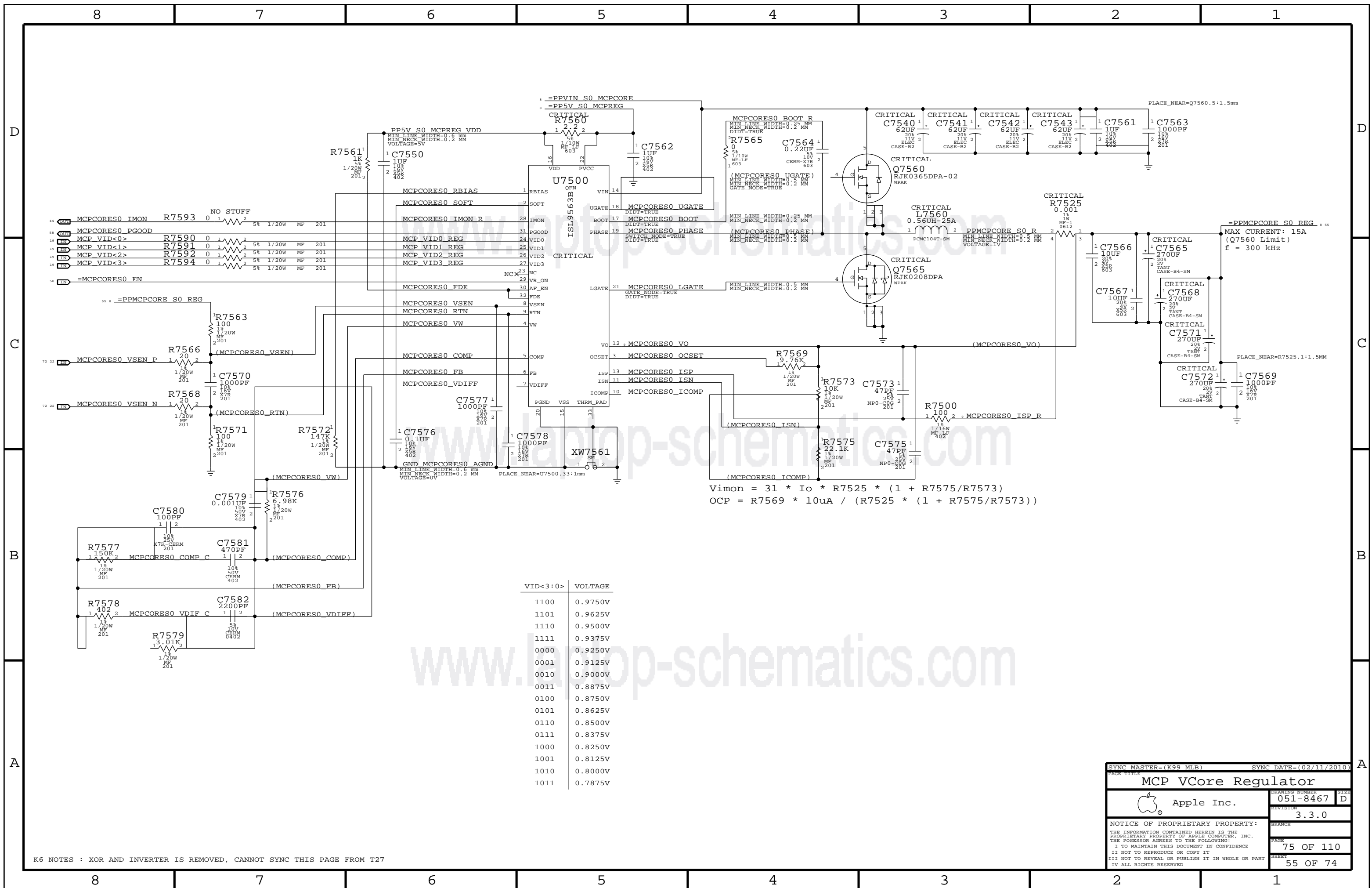
SYNC MASTER=K16 MLB		SYNC DATE=06/01/2010	
PAGE TITLE 1.5V/1.35V LVDDR3 Supply			
Apple Inc.		DRAWING NUMBER 051-8467	SIZE D
		REVISION 3.3.0	
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		SHEET	53 OF 74



$OCP = 21.5mV / R7480 + 3.1A$
 $V_{pmon} = 90 * K * R7480 * V_o * I_o$
 $K = R7450 / (R7450 + R7451 + R7452)$
 $28A @ 1V = 1.764V$
 $Load\ Line = R7480 * 6 / (500U * R7414)$

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
54 GND IMVP6 SGND	0.50 MM	0.20 MM
54 IMVP6 DROOP	0.25 MM	0.20 MM
54 IMVP6 THERM	0.25 MM	0.20 MM
54 IMVP6 ISLEW	0.25 MM	0.20 MM
54 PP1V7 S0 IMVP6 VREF	0.25 MM	0.20 MM
54 PP5V S0 IMVP6 V5FILT	0.25 MM	0.20 MM
54 IMVP6 LL	1.5 MM	0.20 MM
54 IMVP6 VBST	0.25 MM	0.20 MM
54 IMVP6 DRVH	1.5 MM	0.20 MM
54 IMVP6 DRVL	1.5 MM	0.20 MM
54 IMVP6 VBST RC	1.5 MM	0.20 MM

SYNC MASTER=(K99 MLB) SYNC DATE=(02/16/2010)
IMVP6 CPU VCore Regulator
 Apple Inc.
 DRAWING NUMBER: 051-8467
 REVISION: 3.3.0
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$$V_{im} = 31 * I_o * R_{7525} * (1 + R_{7575}/R_{7573})$$

$$OCP = R_{7569} * 10\mu A / (R_{7525} * (1 + R_{7575}/R_{7573}))$$

VID<3:0>	VOLTAGE
1100	0.9750V
1101	0.9625V
1110	0.9500V
1111	0.9375V
0000	0.9250V
0001	0.9125V
0010	0.9000V
0011	0.8875V
0100	0.8750V
0101	0.8625V
0110	0.8500V
0111	0.8375V
1000	0.8250V
1001	0.8125V
1010	0.8000V
1011	0.7875V

SYNC MASTER=(K99 MLB) SYNC DATE=(02/11/2010)

MCP VCore Regulator

Apple Inc.

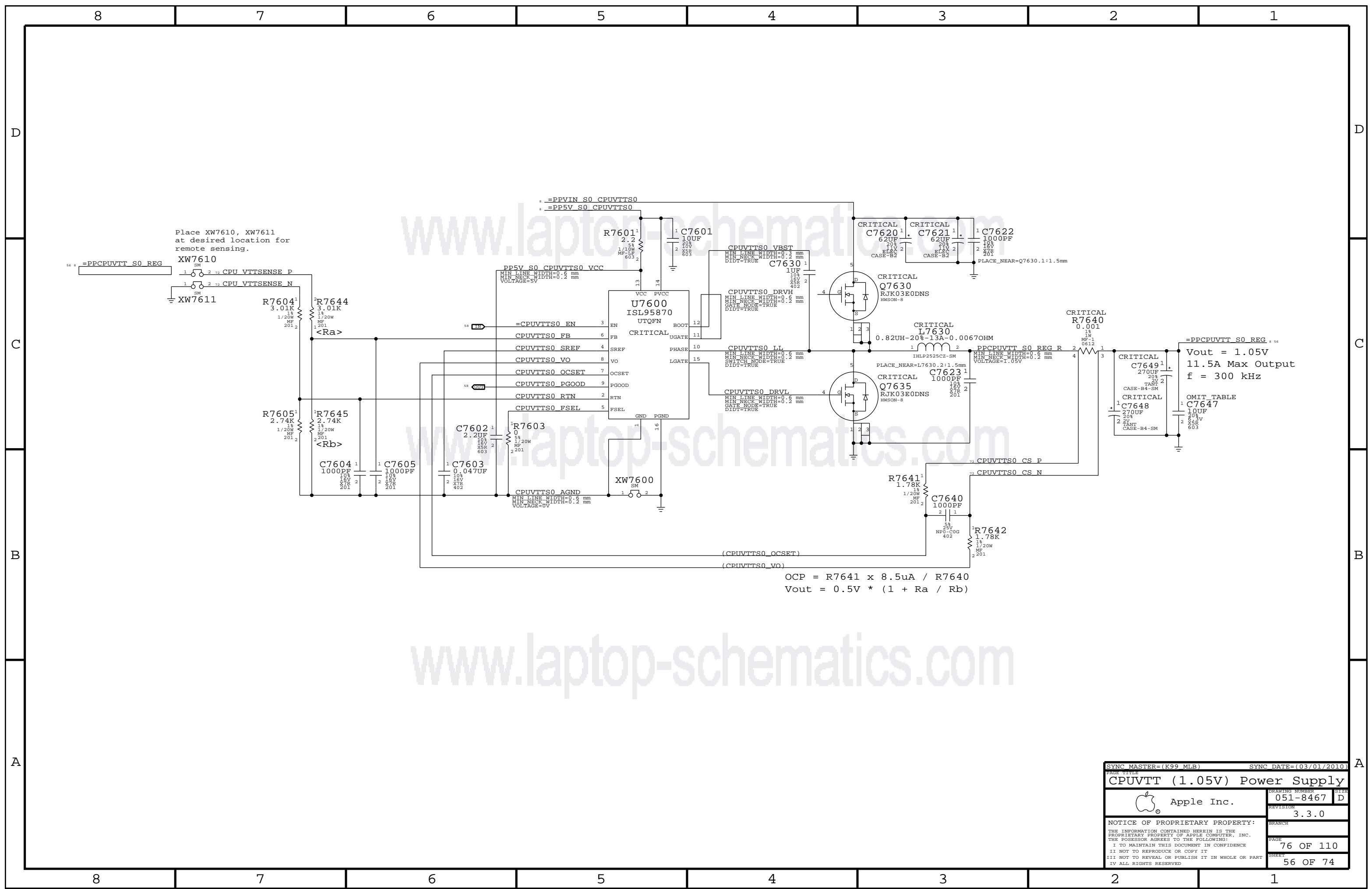
DRAWING NUMBER: 051-8467 SIZE: D

REVISION: 3.3.0

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PAGE: 75 OF 110 SHEET: 55 OF 74

K6 NOTES : XOR AND INVERTER IS REMOVED, CANNOT SYNC THIS PAGE FROM T27



Place XW7610, XW7611
at desired location for
remote sensing.
XW7610
XW7611

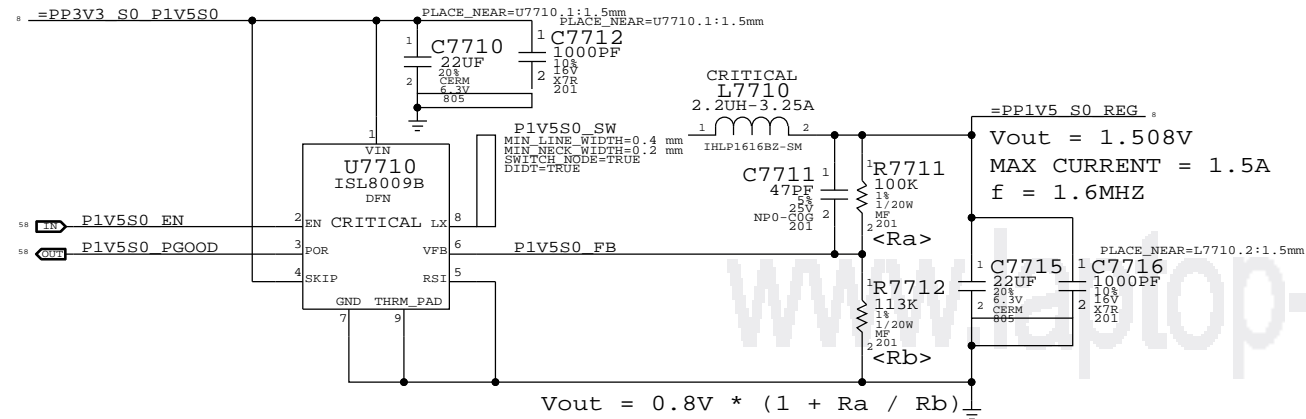
Vout = 1.05V
11.5A Max Output
f = 300 kHz

$$OCP = R7641 \times 8.5\mu A / R7642$$

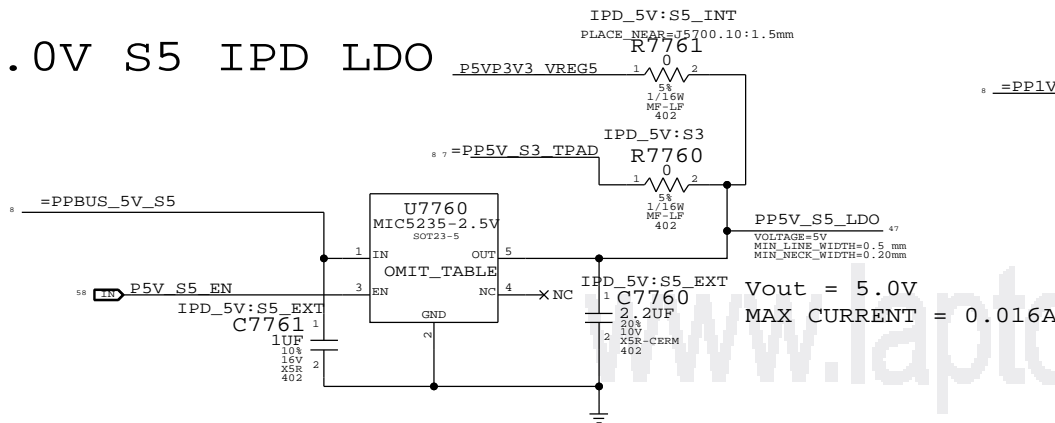
$$Vout = 0.5V * (1 + Ra / Rb)$$

SYNC MASTER=(K99_MLB)		SYNC DATE=(03/01/2010)	
CPUVTT (1.05V) Power Supply			
Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
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1.5V S0 Regulator

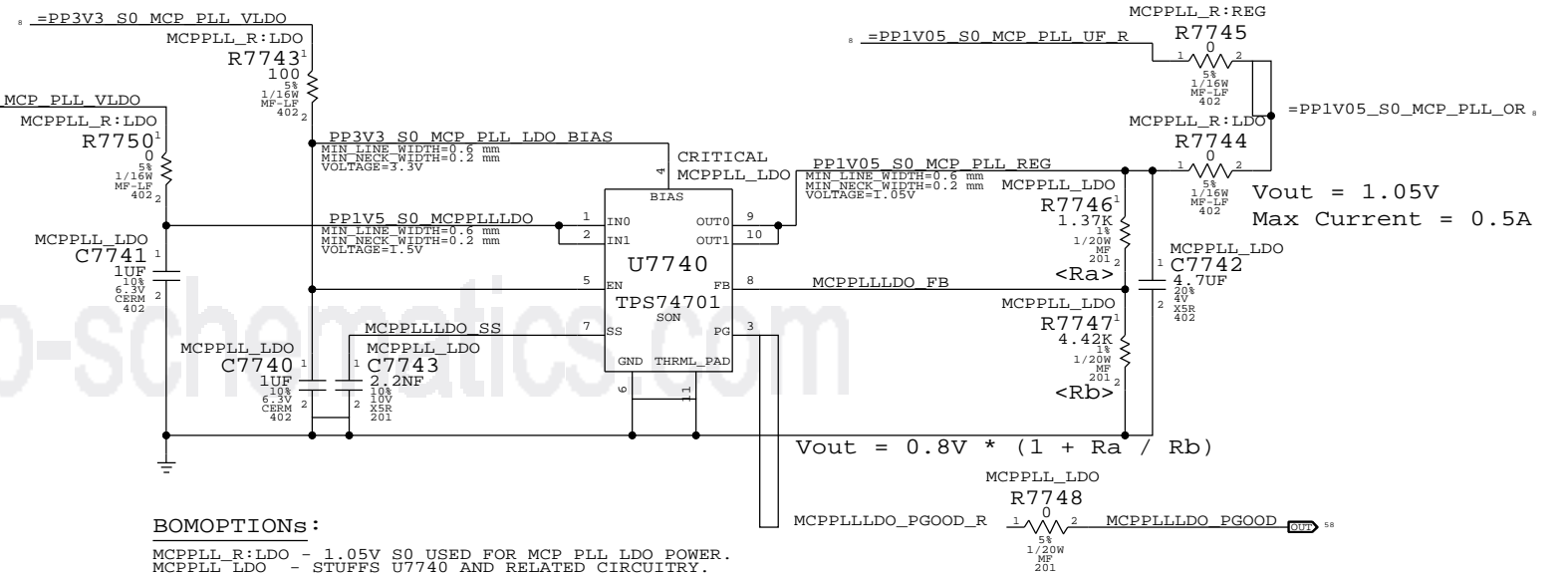


5.0V S5 IPD LDO



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3034	1	IC,LDO,MIC5235,5V,1A,150MA,SOT23-5	U7760		IPD_5V:S5_EXT

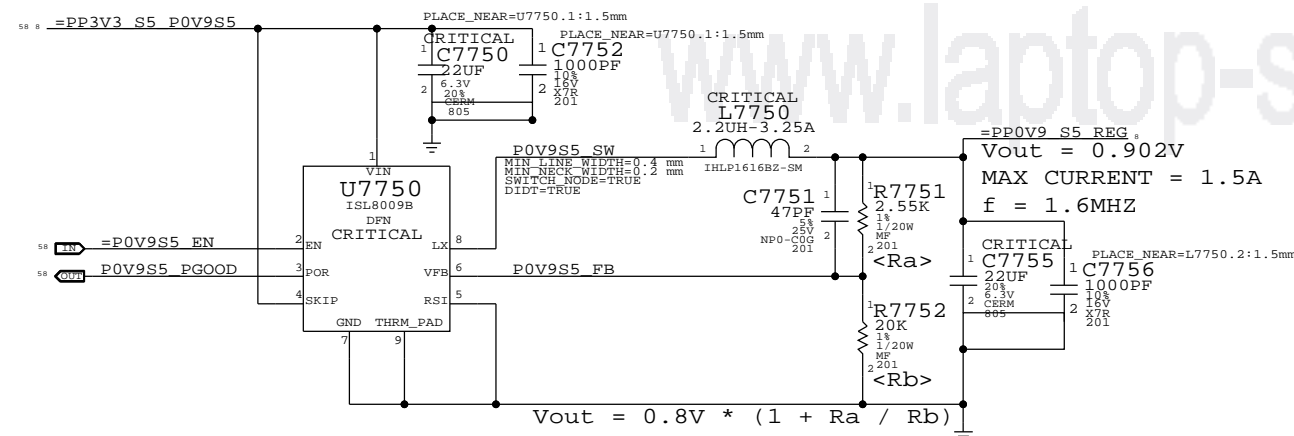
1.05V S0 MCP PLL LDO



BOMOPTIONS:

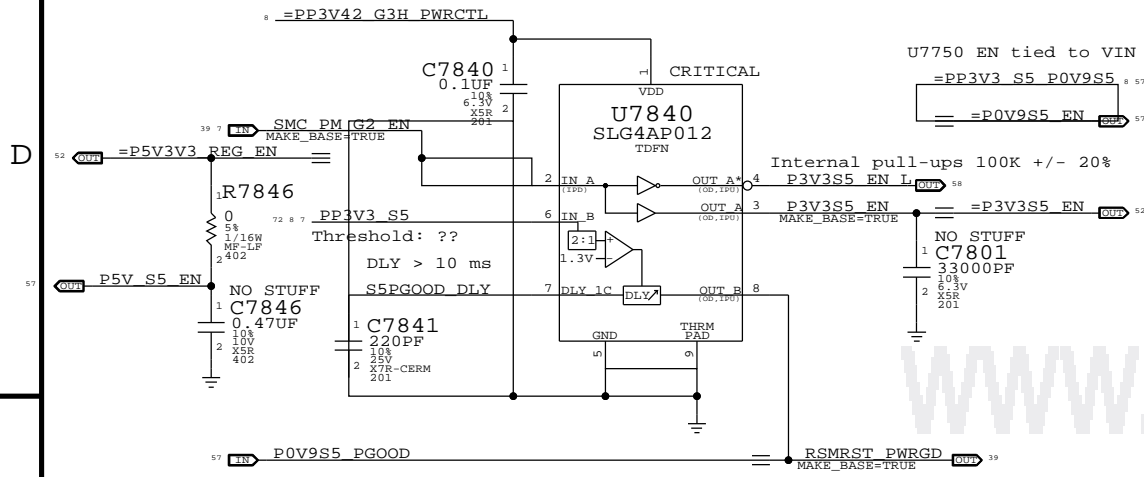
MCPPLL_R:LDO - 1.05V S0 USED FOR MCP PLL LDO POWER.
MCPPLL_LDO - STUFFS U7740 AND RELATED CIRCUITRY.
TO USE U7740, MCPPLL_R:LDO AND MCPPLL_LDO MUST BE ACTIVE.
TO USE 1.05V S0, MCPPLL_R:REG MUST BE ACTIVE, MCPPLL_LDO CAN BE ACTIVE, MCPPLL_R:LDO MUST BE INACTIVE.

MCP 0.9V S5 (AUXC) Switcher

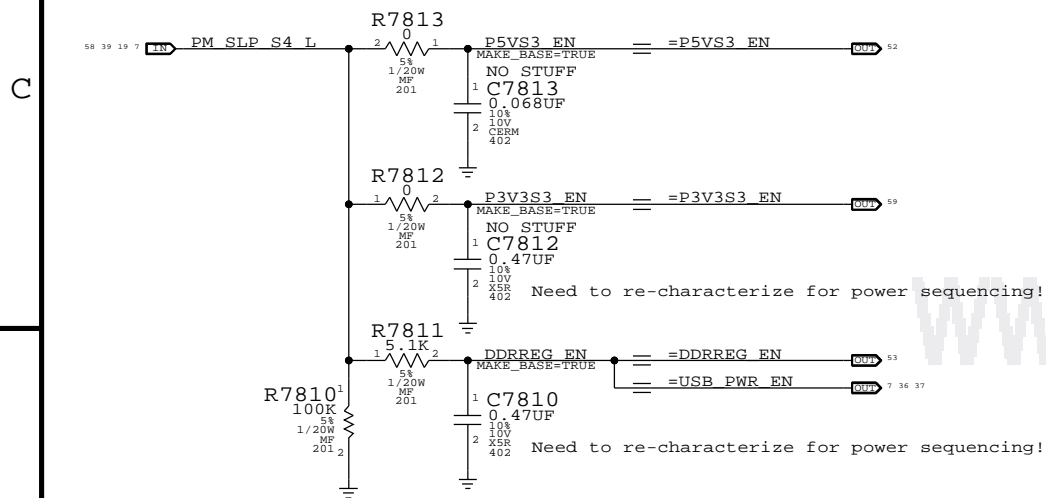


SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
Misc Power Supplies			
Apple Inc.		DRAWING NUMBER	051-8467
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		SHEET	57 OF 74

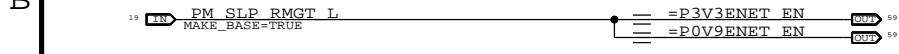
S5 Rail Enables & PGOOD



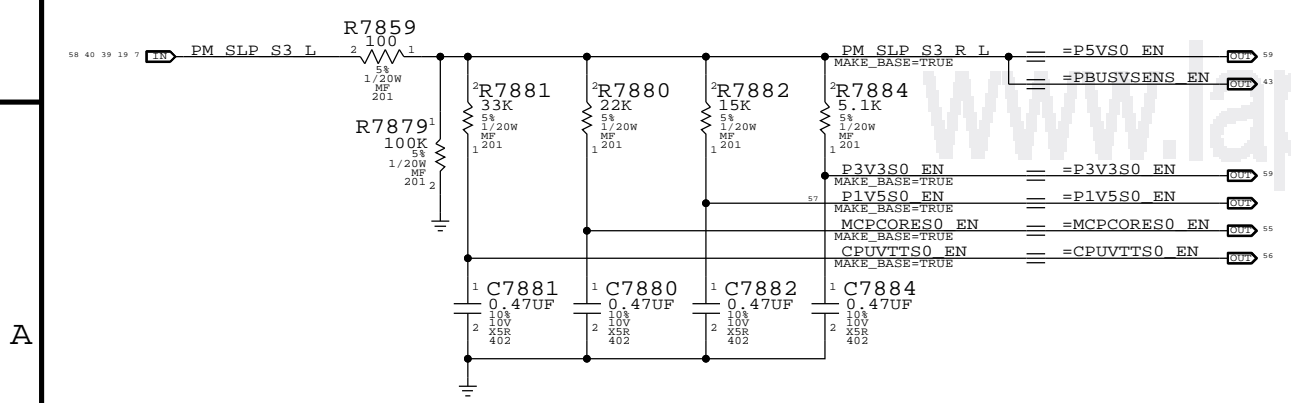
S3 Rail Enables



ENET Rail Enables

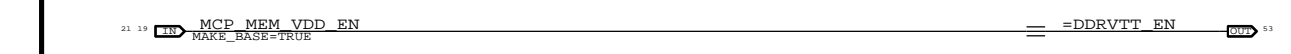


S0 Rail Enables



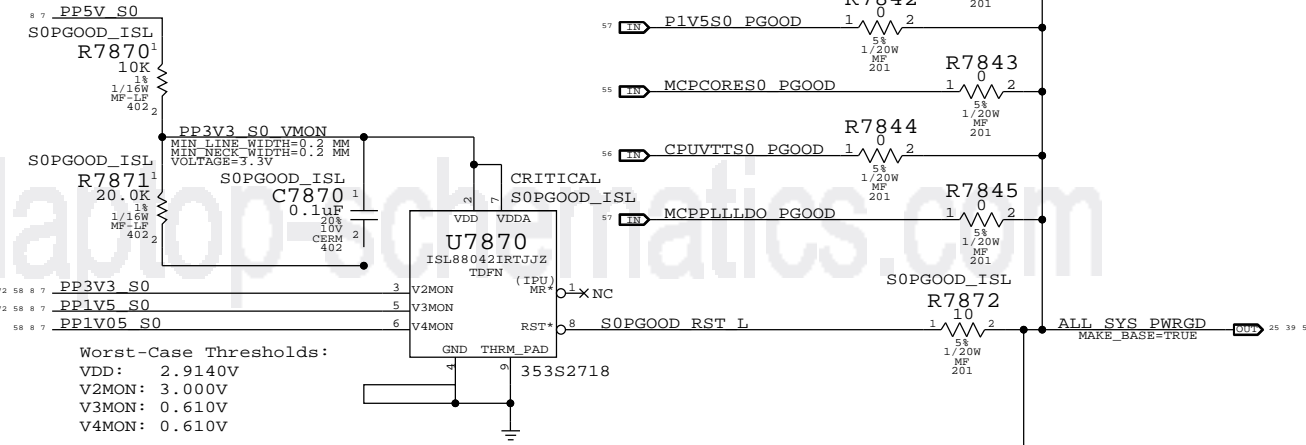
VTT Rail Enable

VTT rail must ramp up in about the same time as MEMVDD rail (Q2300).

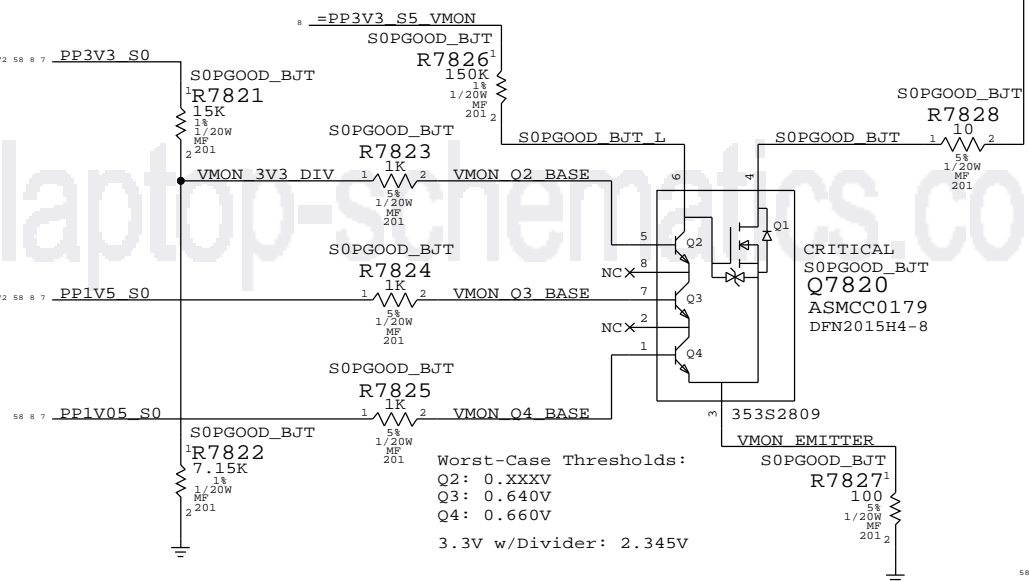


S0 Rail PGOOD Circuitry

S0 Rail PGOOD (ISL Version)



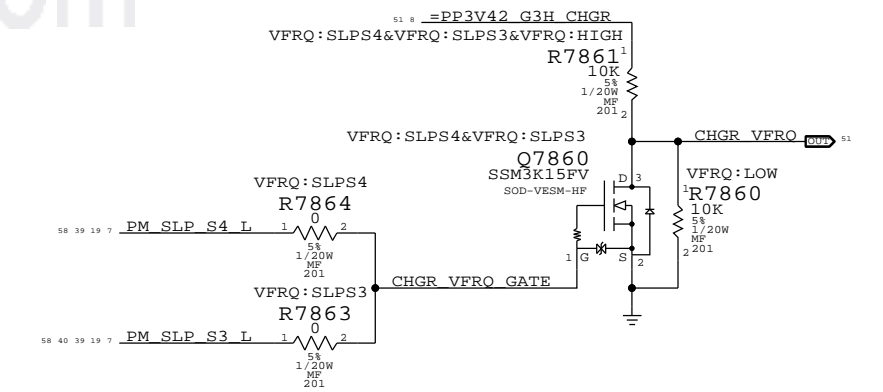
S0 Rail PGOOD (BJT Version)



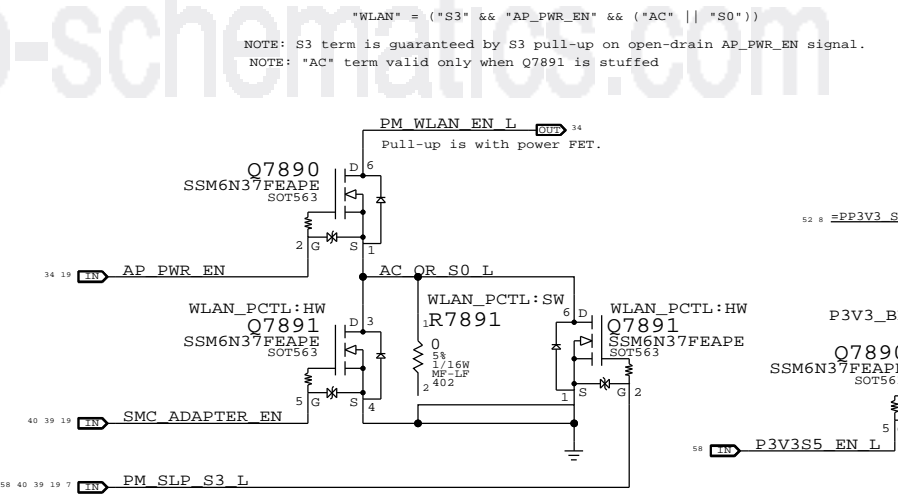
Power Control Signals

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

ISL6259 Frequency Select



WLAN Enable Generation



SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

Power Sequencing

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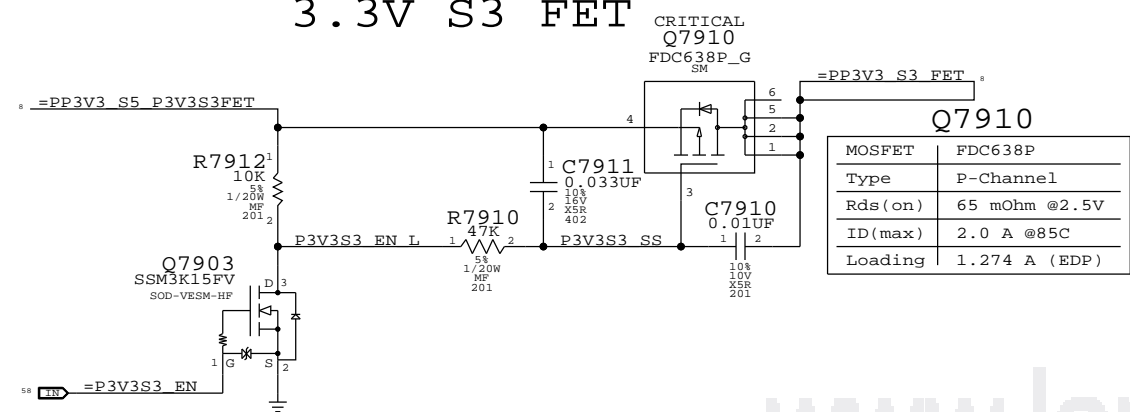
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REVISION: 3.3.0

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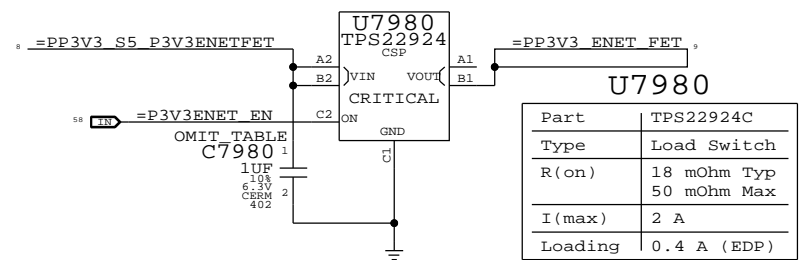
PAGE: 78 OF 110 SHEET: 58 OF 74

3.3V S3 FET



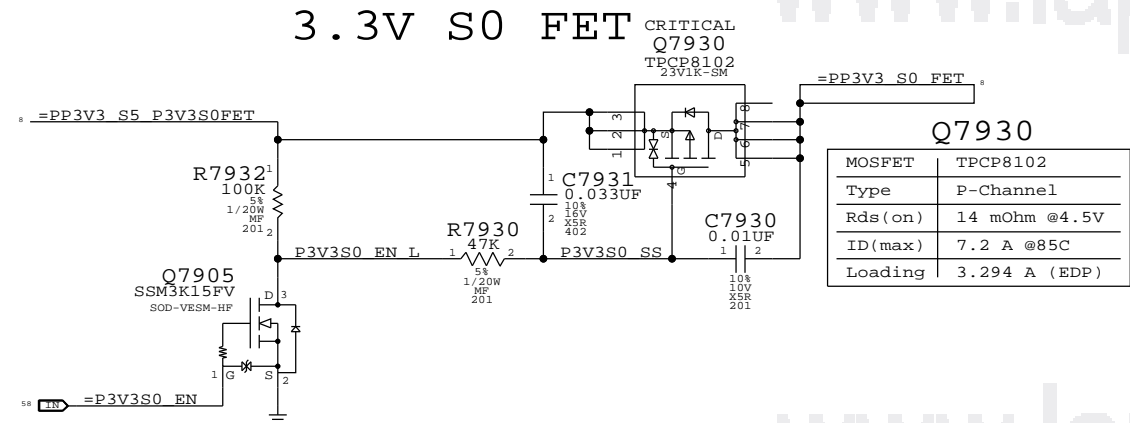
Part	FDC638P
Type	P-Channel
Rds(on)	65 mOhm @2.5V
ID(max)	2.0 A @85C
Loading	1.274 A (EDP)

3.3V ENET Switch



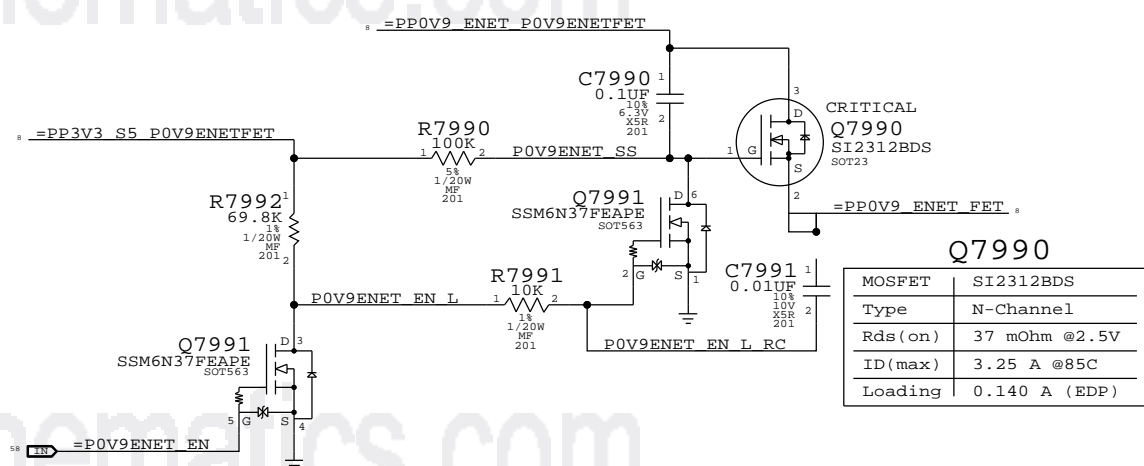
Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ
I(max)	2 A
Loading	0.4 A (EDP)

3.3V S0 FET



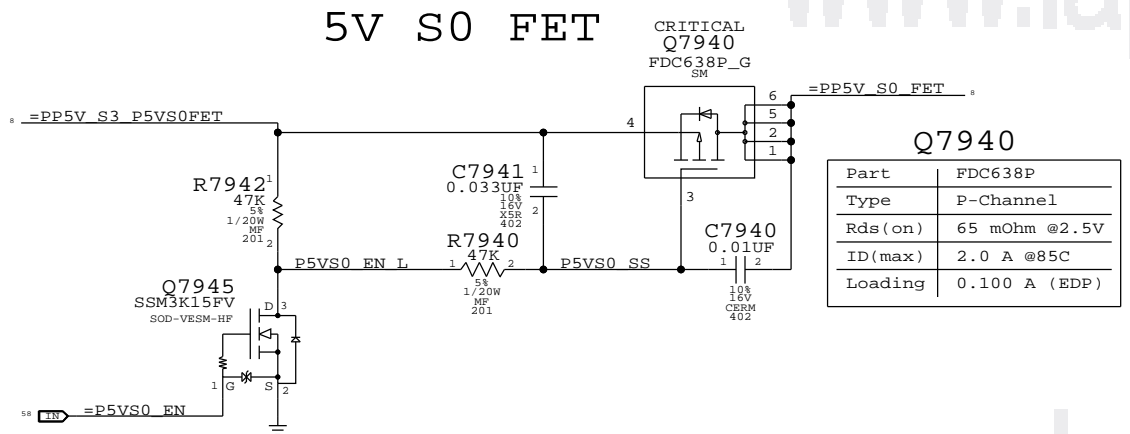
Part	TPCP8102
Type	P-Channel
Rds(on)	14 mOhm @4.5V
ID(max)	7.2 A @85C
Loading	3.294 A (EDP)

0.9V ENET FET



Part	SI2312BDS
Type	N-Channel
Rds(on)	37 mOhm @2.5V
ID(max)	3.25 A @85C
Loading	0.140 A (EDP)

5V S0 FET



Part	FDC638P
Type	P-Channel
Rds(on)	65 mOhm @2.5V
ID(max)	2.0 A @85C
Loading	0.100 A (EDP)

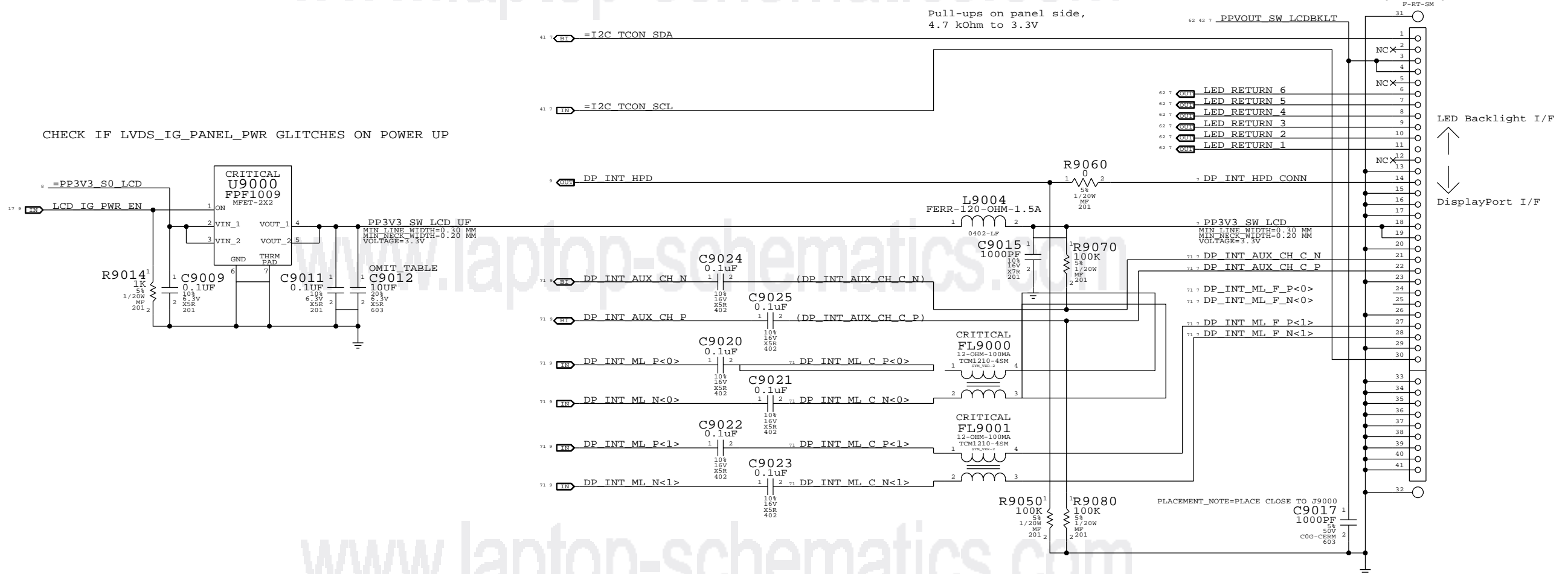
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Power FETs			
 Apple Inc.	DRAWING NUMBER	051-8467	SIZE
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LCD Connector

Internal DP Connector: 518S0787

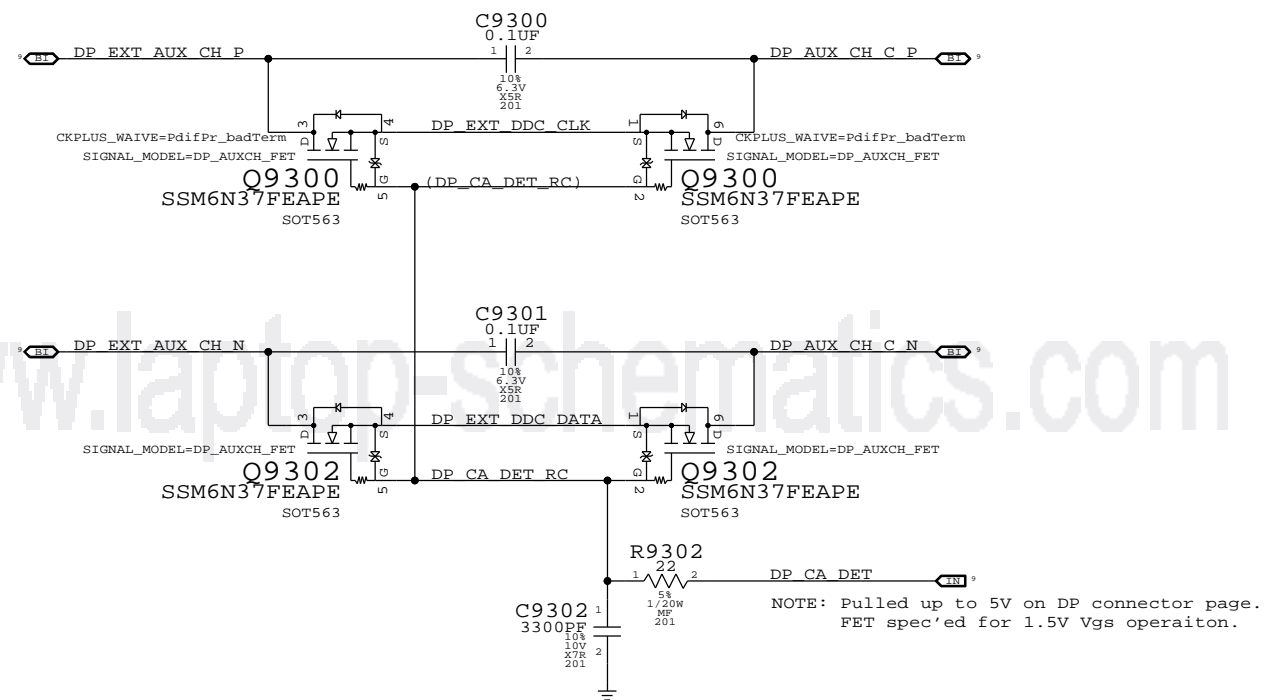
CRITICAL
J9000
CABLINE-CA
P-RT-SM



CHECK IF LVDS_IG_PANEL_PWR GLITCHES ON POWER UP

SYNC MASTER=K99 MLB		SYNC DATE=07/23/2010	
Internal DisplayPort Connector			
Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
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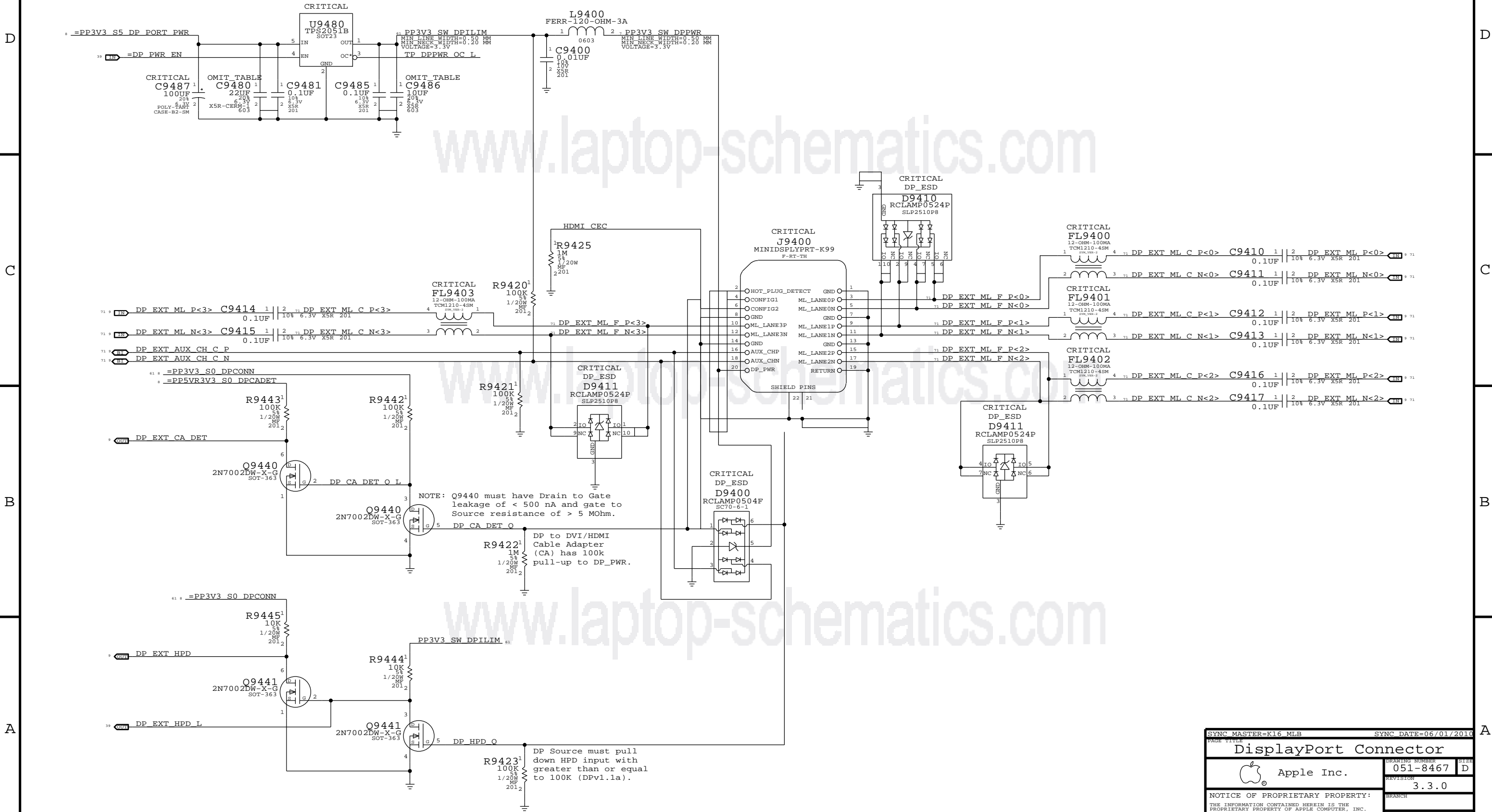


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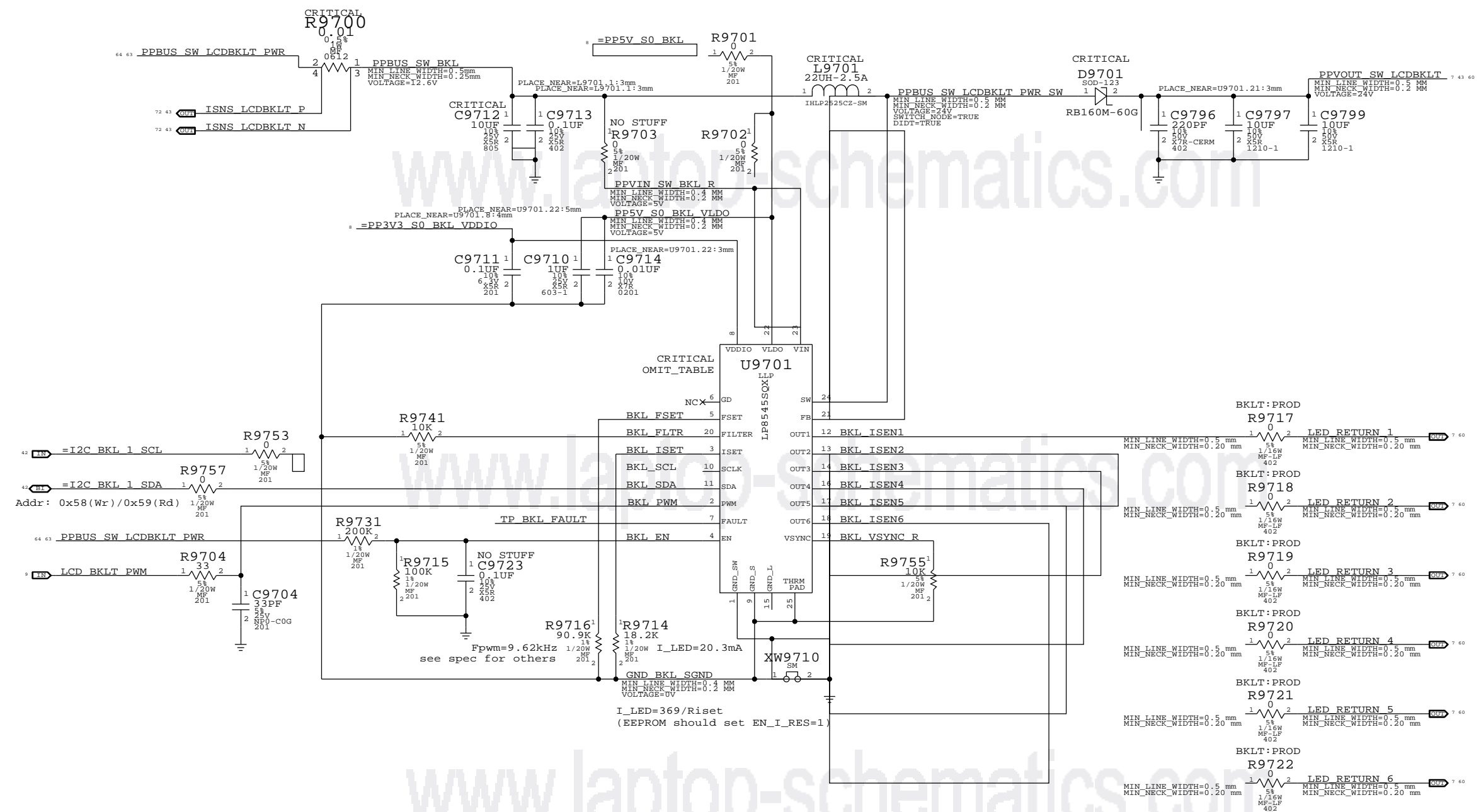
SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
External DisplayPort Support			
Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
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Port Power Switch



SYNC MASTER=K16 MLB		SYNC DATE=06/01/2010	
DisplayPort Connector			
Apple Inc.		DRAWING NUMBER	051-8467
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		SHEET	62 OF 74

*L9701, D9701, C9796, C9797, C9799, C9712 AND C9713 SHOULD ALL BE PLACED NEAR EACHOTHER.
 *PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
 *LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT



FOR LP8543:
 STUFF R9741
 NO STUFF R9740, C9740, C9741, R9754

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG
353S2896	1	IC,LP8545,LED BKLT CTRLR,PRODUCTIO,LLP24	U9701	CRITICAL	PROJ:K16
353S2967	1	IC,LP8545,LED BKLT CTRLR,LLP24,K99 VER	U9701	CRITICAL	PROJ:K99

10.2 ohm resistors for current measurement on LED strings.

SYNC MASTER=(K99_MLB) SYNC DATE=(03/01/2010)

LCD Backlight Driver

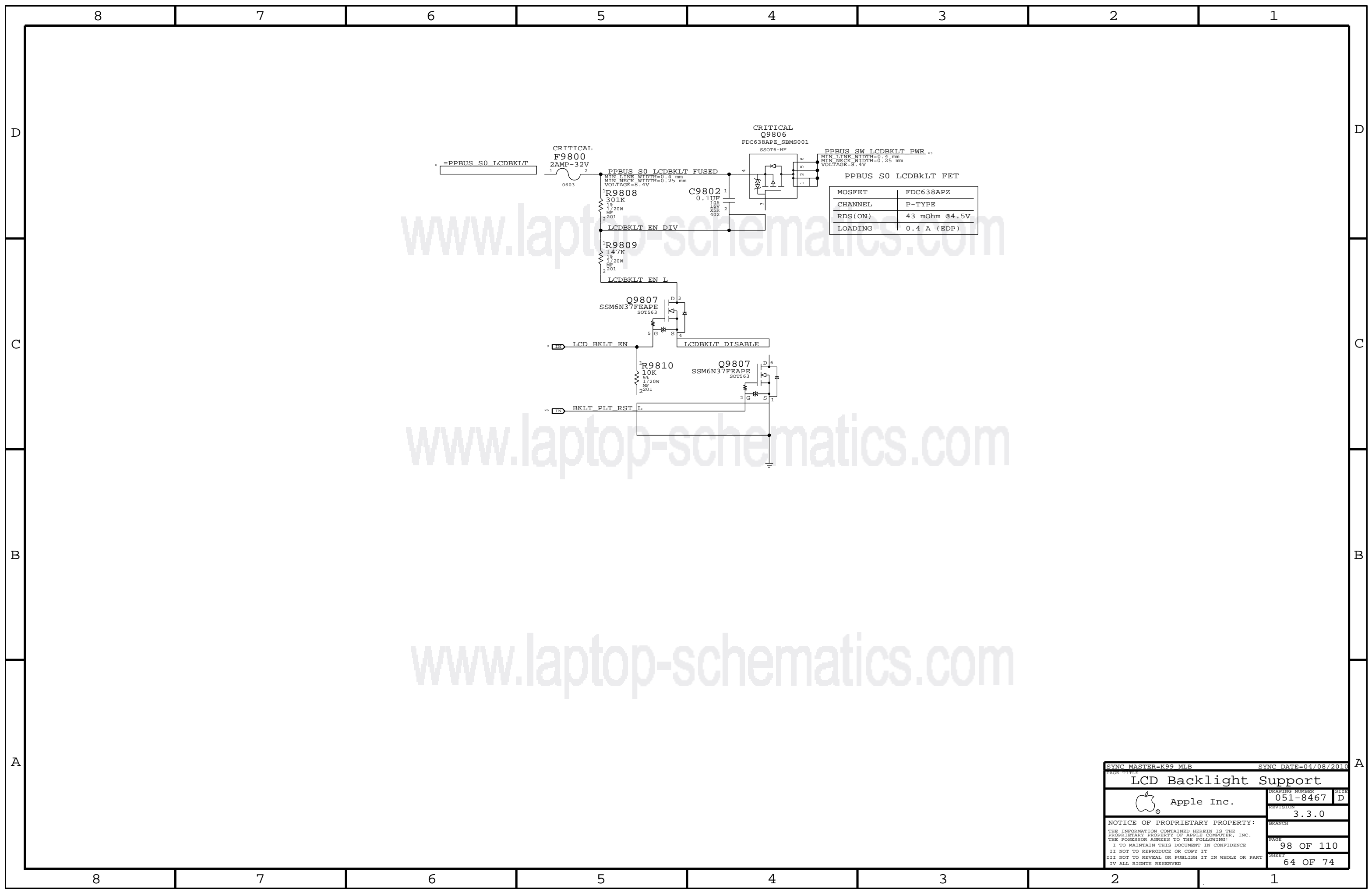
Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D

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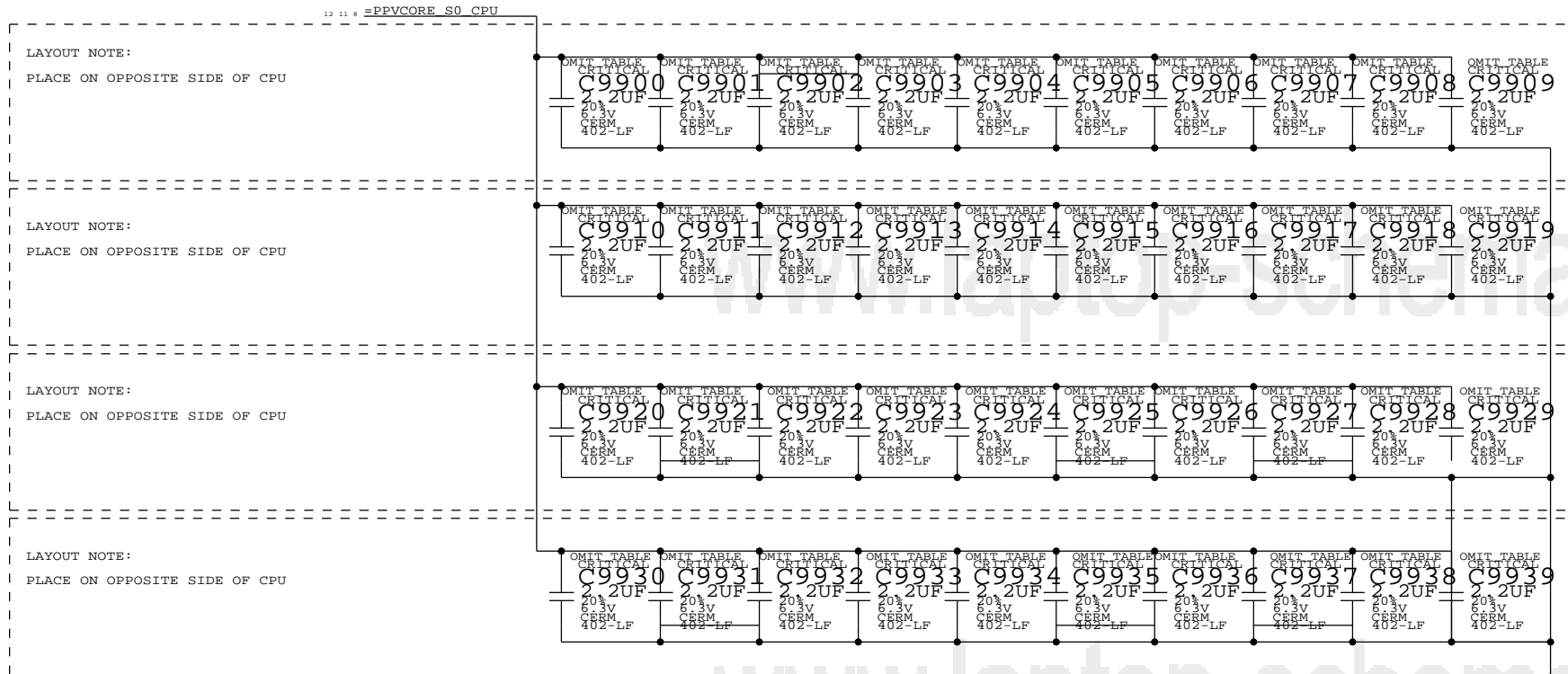
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SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
LCD Backlight Support			
Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
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ADDITIONAL CPU VCORE HF DECOUPLING

40x 1uF 0402



SYNC MASTER=K99 MLB		SYNC DATE=05/18/2010	
Additional CPU/GPU Decoupling			
	DRAWING NUMBER	051-8467	SIZE
	REVISION	3.3.0	D
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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?	FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?	FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?	FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	*	=2x_DIELECTRIC	?	FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?	FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.

Signals within each 4x group should be matched within 5 ps of strobe.

DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 135 ps.

Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

FSB 2X signals / groups shown in signal table on right.

Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 270 ps.

Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADTSB#.

FSB 1X signals shown in signal table on right.

Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1

SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCsense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?	CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_8MIL	*	8 MIL	?				
CPU_COMP	*	25 MIL	?				
CPU_GTLREF	*	25 MIL	?				
CPU_ITP	*	=2:1_SPACING	?				
CPU_VCCSENSE	*	25 MIL	?				

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.

Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?	CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB D L<15..0>	7 10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB DINV L<0>	7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<0>	7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<0>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB D L<31..16>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB DINV L<1>	7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<1>	7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<1>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB D L<47..32>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB DINV L<2>	7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<2>	7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<2>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB D L<63..48>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB DINV L<3>	7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<3>	7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB A L<16..3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB REQ L<4..0>	7 10 14
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB ADSTB L<0>	7 10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB A L<35..17>	7 10 14
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB ADSTB L<1>	7 10 14
FSB_1X	FSB_55S	FSB_1X	FSB ADS L	7 10 14
FSB_BREQ0_L	FSB_55S	FSB_1X	FSB BREQ0 L	10 14
FSB_1X	FSB_55S	FSB_1X	FSB BNR L	10 14
FSB_1X	FSB_55S	FSB_1X	FSB BPRI L	10 14
FSB_1X	FSB_55S	FSB_1X	FSB DBSY L	10 14
FSB_1X	FSB_55S	FSB_1X	FSB DEFER L	10 14
FSB_1X	FSB_55S	FSB_1X	FSB DRDY L	10 14
FSB_1X	FSB_55S	FSB_1X	FSB HIT L	7 10 14
FSB_1X	FSB_55S	FSB_1X	FSB HITM L	7 10 14
FSB_1X	FSB_55S	FSB_1X	FSB LOCK L	7 10 14
FSB_CPURST_L	FSB_55S	FSB_1X	FSB CPURST L	10 13 14
FSB_1X	FSB_55S	FSB_1X	FSB RS L<2..0>	10 14
FSB_1X	FSB_55S	FSB_1X	FSB TRDY L	10 14
CPU_ASYNC	CPU_55S	CPU_AGTL	CPU A20M L	10 14
CPU_BSEL	CPU_55S	CPU_AGTL	CPU BSEL<2..0>	9 10
CPU_FERR_L	CPU_55S	CPU_8MIL	CPU FERR L	10 14
CPU_ASYNC	CPU_55S	CPU_AGTL	CPU IGNE L	10 14
CPU_INIT_L	CPU_55S	CPU_AGTL	CPU INIT L	10 14
CPU_ASYNC_R	CPU_55S	CPU_AGTL	CPU INTR	10 14
CPU_ASYNC_R	CPU_55S	CPU_AGTL	CPU NMI	10 14
CPU_PROCHOT_L	CPU_55S	CPU_AGTL	CPU PROCHOT L	10 14 40
CPU_PWRGD	CPU_55S	CPU_AGTL	CPU PWRGD	10 13 14
CPU_ASYNC	CPU_55S	CPU_AGTL	CPU SMI L	10 14
CPU_ASYNC	CPU_55S	CPU_AGTL	CPU STPCLK L	10 14
PM_THERMTRIP_L	CPU_55S	CPU_8MIL	PM THERMTRIP L	10 14 40
FSB_CPUSLP_L	CPU_55S	CPU_AGTL	FSB CPUSLP L	10 14
CPU_PROM_SB	CPU_55S	CPU_AGTL	CPU DPRSLP L	10 14
CPU_DPRSTP_L	CPU_55S	CPU_AGTL	CPU DPRSTP L	10 14 54
CPU_ASYNC	CPU_55S	CPU_AGTL	FSB DPWR L	10 14
FSB_CLK_CPUH	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P	10 14
FSB_CLK_CPUN	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N	10 14
FSB_CLK_ITP_P	CLK_FSB_100D	CLK_FSB	FSB CLK ITP P	13 14
FSB_CLK_ITP_N	CLK_FSB_100D	CLK_FSB	FSB CLK ITP N	13 14
FSB_CLK_MCP_P	CLK_FSB_100D	CLK_FSB	FSB CLK MCP P	14
FSB_CLK_MCP_N	CLK_FSB_100D	CLK_FSB	FSB CLK MCP N	14
CPU_IERR_L	CPU_55S		CPU IERR L	10
PM_DPRSLPVR	CPU_55S	CPU_AGTL	PM DPRSLPVR	14 54
(See above)	CPU_55S	CPU_AGTL	IMVP DPRSLPVR	
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP VDD	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP GND	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP VCC	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP GND	14
CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU GTLREF	10 33
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<3>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	10
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<1>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	10
XDP_TDI	CPU_55S	CPU_ITP	XDP TDI	10 33
XDP_TDO	CPU_55S	CPU_ITP	XDP TDO	10 33
XDP_TMS	CPU_55S	CPU_ITP	XDP TMS	10 33
XDP_TCK	CPU_55S	CPU_ITP	XDP TCK	10 33
XDP_TRST_L	CPU_55S	CPU_ITP	XDP TRST L	10 33
XDP_BPM_L	CPU_55S	CPU_ITP	XDP BPM L<4..0>	10 33
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP BPM L<5>	10 33
(FSB_CPURST_I)	CPU_55S	CPU_ITP	XDP CPURST L	13
	CPU_55S	CPU_8MIL	CPU VID<6..0>	11 12 54
	CPU_55S	CPU_8MIL	IMVP6 VID<6..0>	12
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P	11 54
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N	11 54
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN P	54
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN N	54

SYNC MASTER=K99 MLB SYNC DATE=04/08/2010

CPU/FSB Constraints		DRAWING NUMBER	SIZE
Apple Inc.		051-8467	D
		REVISION	3.3.0
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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NV DG says 3x inner, 4x outer
 NV DG says 2x inner, 4x outer
 NV DG says 2x inner, 4x outer
 NV DG says 2x inner, 4x outer
 NV DG says 2x inner, 4x outer
 NV DG says 2x inner, 4x outer
 NV DG says 4x inner, 5x outer

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2MEM
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

DDR3:
 DQ signals should be matched within 5 ps of associated DQS pair.
 DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 360 ps
 No DQS to clock matching requirement.
 CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
 CMD/CTRL signals should be matched within 150 ps.
 All memory signals maximum length is 1.030 ps.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.3
 SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
MEM_A_CLK	MEM_70D	MEM_CLK	MEM A CLK P<5..0>
MEM_A_CLK	MEM_70D	MEM_CLK	MEM A CLK N<5..0>
MEM_A_CKE	MEM_50S	MEM_CTRL	MEM A CKE<3..0>
MEM_A_CNTRL	MEM_50S	MEM_CTRL	MEM A CS L<3..0>
MEM_A_CNTRL	MEM_50S	MEM_CTRL	MEM A ODT<3..0>
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A A<15..0>
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A BA<2..0>
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A RAS L
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A CAS L
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A WE L
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM A DQ<7..0>
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM A DQ<15..8>
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM A DQ<23..16>
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM A DQ<31..24>
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM A DQ<39..32>
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM A DQ<47..40>
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM A DQ<55..48>
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM A DQ<63..56>
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM A DM<0>
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM A DM<1>
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM A DM<2>
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM A DM<3>
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM A DM<4>
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM A DM<5>
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM A DM<6>
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM A DM<7>
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS P<0>
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS N<0>
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS P<1>
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS N<1>
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS P<2>
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS N<2>
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS P<3>
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS N<3>
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS P<4>
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS N<4>
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS P<5>
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS N<5>
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS P<6>
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS N<6>
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS P<7>
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS N<7>
MEM_B_CLK	MEM_70D	MEM_CLK	MEM B CLK P<5..0>
MEM_B_CLK	MEM_70D	MEM_CLK	MEM B CLK N<5..0>
MEM_B_CKE	MEM_50S	MEM_CTRL	MEM B CKE<3..0>
MEM_B_CNTRL	MEM_50S	MEM_CTRL	MEM B CS L<3..0>
MEM_B_CNTRL	MEM_50S	MEM_CTRL	MEM B ODT<3..0>
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B A<15..0>
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B BA<2..0>
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B RAS L
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B CAS L
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B WE L
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM B DQ<7..0>
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM B DQ<15..8>
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM B DQ<23..16>
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM B DQ<31..24>
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM B DQ<39..32>
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM B DQ<47..40>
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM B DQ<55..48>
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM B DQ<63..56>
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM B DM<0>
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM B DM<1>
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM B DM<2>
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM B DM<3>
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM B DM<4>
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM B DM<5>
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM B DM<6>
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM B DM<7>
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS P<0>
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS N<0>
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS P<1>
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS N<1>
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS P<2>
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS N<2>
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS P<3>
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS N<3>
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS P<4>
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS N<4>
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS P<5>
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS N<5>
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS P<6>
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS N<6>
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS P<7>
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS N<7>
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP VDD
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP GND

MEM_A/B_CKE EC SET NAME IS CHANGED ON K6, CANNOT SYNC THIS PAGE FROM T27

SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
Memory Constraints			
Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?	PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?				
MCP_PEX_COMP	*	8 MIL	?				

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.3

NEED PCIe Gen1/Gen2 notes!

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	*	20 MIL	?	CRT	CRT	*	CRT_2CRT
CRT_2CRT	*	15 MIL	?				
CRT_2CLK	*	50 MIL	?				
CRT_2SWITCHER	*	250 MIL	?				
CRT_SYNC	*	=4x_DIELECTRIC	?				
MCP_DAC_COMP	*	=2x_DIELECTRIC	?				

CRT signal single-ended impedance varies by location:

- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.1.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?	DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?	LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be matched within 100 mils.
 NOTE: NV DG recommends 90 ohm differential for LVDS, but cable/display assume 100 ohm.
 DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 100 ps.
 DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
 Max trace length: LVDS 10 inches, DP 8.5 inches.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.2

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=3x_DIELECTRIC	?	SATA	TOP,BOTTOM	=4x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?				

SATA intra-pair matching should be 1 ps.

Max trace length: 12 inches for SATA Gen1/Gen2, TBD for SATA Gen3.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.6

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
PEG_R2D	PCIE_90D	PCIE	PEG R2D P<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG R2D N<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG R2D C P<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG R2D C N<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R P<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R N<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R C P<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R C N<15..0>
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE AP R2D P
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE AP R2D N
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE AP R2D C P
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE AP R2D C N
PCIE_AP_D2R	PCIE_90D	PCIE	PCIE AP D2R P
PCIE_AP_D2R	PCIE_90D	PCIE	PCIE AP D2R N
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE ENET R2D P
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE ENET R2D N
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE ENET R2D C P
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE ENET R2D C N
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE ENET D2R P
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE ENET D2R N
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE ENET D2R C P
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE ENET D2R C N
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE FW R2D P
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE FW R2D N
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE FW R2D C P
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE FW R2D C N
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE FW D2R P
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE FW D2R N
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE FW D2R C P
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE FW D2R C N
MCP_PEG0_BEECLK	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M P
MCP_PEG0_BEECLK	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M N
MCP_PEG1_BEECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M AP P
MCP_PEG1_BEECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M AP N
MCP_PEG2_BEECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET P
MCP_PEG2_BEECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET N
MCP_PEG3_BEECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW P
MCP_PEG3_BEECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW N
MCP_PEX_CLK_COMP			MCP_PEX0_TERMP
CRT_RED	CRT_50S	CRT	CRT IG R C PR
CRT_GREEN	CRT_50S	CRT	CRT IG G Y Y
CRT_BLUE	CRT_50S	CRT	CRT IG B COMP PB
CRT_SYNC	CRT_50S	CRT_SYNC	CRT IG HSYNC
CRT_SYNC	CRT_50S	CRT_SYNC	CRT IG VSYNC
MCP_DAC_RSET		MCP_DAC_COMP	MCP_TV_DAC_RSET
MCP_DAC_VREF		MCP_DAC_COMP	MCP_TV_DAC_VREF
DP_INT_ML	DP_90D	DISPLAYPORT	DP IG ML1 P<1..0>
DP_INT_ML	DP_90D	DISPLAYPORT	DP IG ML1 N<1..0>
DP_INT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH1 P
DP_INT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH1 N
DP_EXT_ML	DP_90D	DISPLAYPORT	DP IG ML0 P<3..0>
DP_EXT_ML	DP_90D	DISPLAYPORT	DP IG ML0 N<3..0>
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH0 P
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH0 N
MCP_TMDS0_RSET	MCP_DV_COMP		MCP_TMDS0_RSET
MCP_TMDS0_VPROBE			MCP_TMDS0_VPROBE
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK P
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK N
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS IG A DATA P<2..0>
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS IG A DATA N<2..0>
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS IG A DATA P<3>
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS IG A DATA N<3>
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS IG B CLK P
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS IG B CLK N
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS IG B DATA P<2..0>
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS IG B DATA N<2..0>
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS IG B DATA P<3>
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS IG B DATA N<3>
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D C P
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D C N
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D P
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D N
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R P
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R N
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R C P
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R C N
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D C P
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D C N
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D P
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D N
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R P
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R N
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R C P
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R C N
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP

SYNC MASTER=K99 MLB SYNC DATE=04/08/2010

MCP Constraints 1

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D

REVISION: 3.3.0

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=1.5x_DIELECTRIC	?
CLK_LPC	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.7

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIA5	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?	USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.8

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.10

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.11

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.12

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
LPC_AD	LPC_55S	LPC	LPC AD<3..0>	7 19 39 41
LPC_FRAME_L	LPC_55S	LPC	LPC FRAME L	7 19 39 41
LPC_RESET_L	LPC_55S	LPC	LPC RESET L	19 25
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC R	19 25
	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC	25 39
	CLK_LPC_55S	CLK_LPC	LPC CLK33M LPCPLUS	7 25 41
USB_EXT_A	USB_90D	USB	USB EXT_A P	18 36
	USB_90D	USB	USB EXT_A N	18 36
	USB_90D	USB	USB EXT_A MUXED P	36 72
	USB_90D	USB	USB EXT_A MUXED N	36 72
USB_MINI	USB_90D	USB	USB MINI P	9 18
	USB_90D	USB	USB MINI N	9 18
USB_EXTD	USB_90D	USB	USB EXT_D P	7 18 37
	USB_90D	USB	USB EXT_D N	7 18 37
USB_CAMERA	USB_90D	USB	USB CAMERA P	7 18 37
	USB_90D	USB	USB CAMERA N	7 18 37
USB_BT	USB_90D	USB	USB BT P	7 18 34
	USB_90D	USB	USB BT N	7 18 34
USB_TPAD	USB_90D	USB	USB TPAD P	18 47 72
	USB_90D	USB	USB TPAD N	18 47 72
USB_IR	USB_90D	USB	USB IR P	
	USB_90D	USB	USB IR N	
USB_EXTR	USB_90D	USB	USB EXTB P	
	USB_90D	USB	USB EXTB N	
USB_T57	USB_90D	USB	USB T57 P	
	USB_90D	USB	USB T57 N	
USB_EXTC	USB_90D	USB	USB EXTC P	9 18
	USB_90D	USB	USB EXTC N	9 18
USB_SDCARD	USB_90D	USB	USB SDCARD P	18 38
	USB_90D	USB	USB SDCARD N	18 38
USB_WM	USB_90D	USB	USB WM P	
	USB_90D	USB	USB WM N	
MCP_USB_RBIA5	MCP_USB_RBIA5		MCP USB RBIA5 GND	18
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS MCP 0 CLK	19 42
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS MCP 0 DATA	19 42
(SMBUS_SMC_MGMT_SCL)	SMB_55S	SMB	SMBUS MCP 1 CLK	19 42
(SMBUS_SMC_MGMT_SDA)	SMB_55S	SMB	SMBUS MCP 1 DATA	19 42
HDA_BIT_CLK	HDA_55S	HDA	HDA BIT CLK	7 19 37
	HDA_55S	HDA	HDA BIT CLK R	19
HDA_SYNC	HDA_55S	HDA	HDA SYNC	7 19 37
	HDA_55S	HDA	HDA SYNC R	19
HDA_RST_L	HDA_55S	HDA	HDA RST L	7 19 37
	HDA_55S	HDA	HDA RST L	7 19 37
HDA_SDIN0	HDA_55S	HDA	HDA SDIN0	7 19 37
	HDA_55S	HDA	HDA SDIN CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA SDOUT	7 19 37
	HDA_55S	HDA	HDA SDOUT R	19
MCP_HDA_PULLDN_COMP	MCP_HDA_COMP		MCP HDA PULLDN COMP	19
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM CLK32K SUSCLK R	19 25
	CLK_SLOW_55S	CLK_SLOW	PM CLK32K SUSCLK	25 39
SPI_CLK	SPI_55S	SPI	SPI CLK R	19 41
	SPI_55S	SPI	SPI CLK	41
SPI_MOSI	SPI_55S	SPI	SPI MOSI R	19 41
	SPI_55S	SPI	SPI MOSI	41
SPI_MISO	SPI_55S	SPI	SPI MISO	19 41
SPI_CS0	SPI_55S	SPI	SPI CS0 R L	19 41
	SPI_55S	SPI	SPI CS0 L	41
	SPI_55S	SPI	SPI MLB CLK	41 48
	SPI_55S	SPI	SPI MLB MOSI	41 48
	SPI_55S	SPI	SPI MLB MISO	41 48
	SPI_55S	SPI	SPI MLB CS L	41 48
	SPI_55S	SPI	SPI ALT CLK	7 41
	SPI_55S	SPI	SPI ALT MOSI	7 41
	SPI_55S	SPI	SPI ALT MISO	7 41
	SPI_55S	SPI	SPI ALT CS L	7 41

SYNC MASTER=K99 MLB SYNC DATE=04/08/2010

MCP Constraints 2

Apple Inc.

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REVISION: 3.3.0

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

SD Card Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_INTERFACE	*	=3X_DIELECTRIC	?

RGMII Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP VDD
MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP GND
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP CLK25M BUF0 R
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211 CLK25M CKXTAL1
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET INTR L
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET MDIO
ENET_MDC	ENET_MII_55S	ENET_MII	ENET MDC
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET PWRDWN L
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET CLK125M RXCLK R
	ENET_MII_55S	ENET_MII	ENET CLK125M RXCLK
	ENET_MII_55S	ENET_MII	ENET RXD R<3..0>
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET RXD<0>
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET RXD<3..1>
ENET_RXD	ENET_MII_55S	ENET_MII	ENET RX CTRL
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET CLK125M TXCLK
ENET_TXD	ENET_MII_55S	ENET_MII	ENET TXD<0>
ENET_TXD	ENET_MII_55S	ENET_MII	ENET TXD<3..1>
ENET_TXD	ENET_MII_55S	ENET_MII	ENET TX CTRL
	ENET_MII_55S	ENET_MII	ENET RESET L


Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET MDI P<3..0>
	ENET_MDI_100D	ENET_MDI	ENET MDI N<3..0>

SD Card Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
SD_DATA	SD_55S	SD_INTERFACE	SD D<4..0>
	SD_55S	SD_INTERFACE	SDCONN DATA<4..0>
	SD_55S	SD_INTERFACE	BCM57765_CR_DATA<4>
SD_DATA_B	SD_55S	SD_INTERFACE	SD D<7..5>
	SD_55S	SD_INTERFACE	SDCONN DATA<7..5>
	SD_55S	SD_INTERFACE	BCM57765_CR_DATA<7..5>
SD_CLK	SD_55S	SD_INTERFACE	SD CLK
	SD_55S	SD_INTERFACE	SD CLK R
	SD_55S	SD_INTERFACE	SDCONN CLK
SD_CMD	SD_55S	SD_INTERFACE	SD CMD
	SD_55S	SD_INTERFACE	SDCONN_CMD
	SD_55S	SD_INTERFACE	BCM57765_CR_CMD

NOTE: SD_D<7..5> are different to support BCM5764M/BCM57765 co-layout.

SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
Ethernet Constraints			
 Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB 550	0300	SMBUS_SMC_A_S3_SCL	42
SMBUS_SMC_A_S3_SDA	SMB 550	0300	SMBUS_SMC_A_S3_SDA	42
SMBUS_SMC_B_S0_SCL	SMB 550	0300	SMBUS_SMC_B_S0_SCL	42
SMBUS_SMC_B_S0_SDA	SMB 550	0300	SMBUS_SMC_B_S0_SDA	42
SMBUS_SMC_O_S0_SCL	SMB 550	0300	SMBUS_SMC_O_S0_SCL	42
SMBUS_SMC_O_S0_SDA	SMB 550	0300	SMBUS_SMC_O_S0_SDA	42
SMBUS_SMC_BSA_SCL	SMB 550	0300	SMBUS_SMC_BSA_SCL	7 42
SMBUS_SMC_BSA_SDA	SMB 550	0300	SMBUS_SMC_BSA_SDA	7 42
SMBUS_SMC_MGMT_SCL	SMB 550	0300	SMBUS_SMC_MGMT_SCL	42
SMBUS_SMC_MGMT_SDA	SMB 550	0300	SMBUS_SMC_MGMT_SDA	42


SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	51
	1TO1_DIFFPAIR		CHGR_CSI_N	51
	1TO1_DIFFPAIR		CHGR_CSI_R_P	51
	1TO1_DIFFPAIR		CHGR_CSI_R_N	51
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	51
	1TO1_DIFFPAIR		CHGR_CSO_N	51
	1TO1_DIFFPAIR		CHGR_CSO_R_P	44 51
	1TO1_DIFFPAIR		CHGR_CSO_R_N	44 51

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SYNC_MASTER=K99_MLB		SYNC_DATE=04/08/2010	
SMC Constraints			
 Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=1:1_SPACING	?
THERM	*	=1:1_SPACING	?
AUDIO	*	=1:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
MEM_POWER	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_POWER	*	PWR_P2MM
MEM_CMD	MEM_POWER	*	PWR_P2MM
MEM_CTRL	MEM_POWER	*	PWR_P2MM
MEM_DATA	MEM_POWER	*	PWR_P2MM
MEM_DQS	MEM_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SD CARD READER LAYOUT RELAXATIONS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55S_OVERRIDE	*	VERRIDE	=STANDARD_OVERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE

MCP Fanout Constraint Relaxations

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S_OVERRIDE	*	VERRIDE	VERRIDE	0.09 MM_OVERRIDE	5.8 MM_OVERRIDE	VERRIDE	VERRIDE
MCP_DV_COMP_OVERRIDE	TOP_OVERRIDE	VERRIDE	VERRIDE	0.1 MM_OVERRIDE	500 MIL_OVERRIDE	VERRIDE	VERRIDE
MCP_MEM_COMP_OVERRIDE	TOP_OVERRIDE	VERRIDE	VERRIDE	0.1 MM_OVERRIDE	500 MIL_OVERRIDE	VERRIDE	VERRIDE
MCP_MII_COMP_OVERRIDE	TOP_OVERRIDE	VERRIDE	VERRIDE	0.1 MM_OVERRIDE	500 MIL_OVERRIDE	VERRIDE	VERRIDE
MCP_USB_RBIA_OVERRIDE	TOP_OVERRIDE	VERRIDE	VERRIDE	0.1 MM_OVERRIDE	500 MIL_OVERRIDE	VERRIDE	VERRIDE
MCP_DV_COMP_OVERRIDE	*	VERRIDE	VERRIDE	0.25 MM_OVERRIDE	250 MIL_OVERRIDE	VERRIDE	VERRIDE

Misc Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
(USB_EXT_A)	USB_90D	USB	USB_EXT_A MUXED P
(USB_EXT_A)	USB_90D	USB	USB_EXT_A MUXED N
(USB_EXT_A)	USB_90D	USB	USB LT1 P
(USB_EXT_A)	USB_90D	USB	USB LT1 N
(USB_TPAD)	USB_90D	USB	USB TPAD P
(USB_TPAD)	USB_90D	USB	USB TPAD N
(USB_TPAD)	USB_90D	USB	USB TPAD CONN P
(USB_TPAD)	USB_90D	USB	USB TPAD CONN N
SMBUS_SMC_MNET_SDA	SMB_55S	SMB	I2C SMC SMS SDA R
SMBUS_SMC_MNET_SCL	SMB_55S	SMB	I2C SMC SMS SCL R
	SMB_55S	SMB	I2C TCON SCL
	SMB_55S	SMB	I2C TCON SDA
	SMB_55S	SMB	I2C TCON SCL CONN
	SMB_55S	SMB	I2C TCON SDA CONN

Graphics Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
	DP_90D	DISPLAYPORT	DP INT ML P<1..0>
	DP_90D	DISPLAYPORT	DP INT ML N<1..0>
	DP_90D	DISPLAYPORT	DP INT ML C P<1..0>
	DP_90D	DISPLAYPORT	DP INT ML C N<1..0>
	DP_90D	DISPLAYPORT	DP INT ML F P<1..0>
	DP_90D	DISPLAYPORT	DP INT ML F N<1..0>
	DP_90D	DISPLAYPORT	DP INT AUX CH C P
	DP_90D	DISPLAYPORT	DP INT AUX CH C N
	DP_90D	DISPLAYPORT	DP INT AUX CH P
	DP_90D	DISPLAYPORT	DP INT AUX CH N
(DP_EXT_ML)	DP_90D	DISPLAYPORT	DP EXT ML P<3..0>
	DP_90D	DISPLAYPORT	DP EXT ML N<3..0>
	DP_90D	DISPLAYPORT	DP EXT ML C P<3..0>
	DP_90D	DISPLAYPORT	DP EXT ML C N<3..0>
	DP_90D	DISPLAYPORT	DP EXT ML F P<3..0>
	DP_90D	DISPLAYPORT	DP EXT ML F N<3..0>
(DP_EXT_AUX_CH)	DP_90D	DISPLAYPORT	DP EXT AUX CH C P
	DP_90D	DISPLAYPORT	DP EXT AUX CH C N

Power Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
CPHTHMSNS_D2	THERM_1T01_55S	THERM	DRAMTHMSNS D2 P
	THERM_1T01_55S	THERM	DRAMTHMSNS D2 N
CPU_THERMD	THERM_1T01_55S	THERM	CPU_THERMD P
	THERM_1T01_55S	THERM	CPU_THERMD N
MCPTHMSNS_D2	THERM_1T01_55S	THERM	MLBR THMDIODE P
	THERM_1T01_55S	THERM	MLBR THMDIODE N
MCP_THMDIODE	THERM_1T01_55S	THERM	MCP_THMDIODE P
	THERM_1T01_55S	THERM	MCP_THMDIODE N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS 1V5 S3 P
	SENSE_1T01_55S	SENSE	ISNS 1V5 S3 N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS AIRPORT P
	SENSE_1T01_55S	SENSE	ISNS AIRPORT N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS CSREG P
	SENSE_1T01_55S	SENSE	ISNS CSREG N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS HDD P
	SENSE_1T01_55S	SENSE	ISNS HDD N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS LCDBKLT P
	SENSE_1T01_55S	SENSE	ISNS LCDBKLT N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUVTT50 CS P
	SENSE_1T01_55S	SENSE	CPUVTT50 CS N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	IMVP6 CS P
	SENSE_1T01_55S	SENSE	IMVP6 CS N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	IMVP6 CS R P
	SENSE_1T01_55S	SENSE	IMVP6 CS R N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPU VTTSENSE P
	SENSE_1T01_55S	SENSE	CPU VTTSENSE N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	MCPCORES0 VSEN P
	SENSE_1T01_55S	SENSE	MCPCORES0 VSEN N
	MEM_POWER		PP1V5R1V35 S3
	SB_POWER		PP3V3 S5
	SB_POWER		PP3V3 S0
	SB_POWER		PP1V5 S0
	GND		GND

Audio Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
SPKRAMP_INR	DIFFPAIR	AUDIO	SPKRAMP_INR P
	DIFFPAIR	AUDIO	SPKRAMP_INR N
MAX98300_R	DIFFPAIR	AUDIO	MAX98300_R P
	DIFFPAIR	AUDIO	MAX98300_R N

SYNC MASTER=T27_MLB SYNC DATE=09/08/2009

K16/K99 Specific Constraints

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D

REVISION: 3.3.0

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K99 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS			BOARD AREAS				BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM			NO_TYPE, BGA				MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.100 MM	0.076 MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
27P4_OHM_SE	ISL3, ISL10	Y	0.250 MM	0.250 MM			
27P4_OHM_SE	ISL4, ISL9	Y	0.250 MM	0.250 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	TOP, BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL3, ISL4, ISL9, ISL10	Y	0.140 MM	0.140 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP, BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	ISL3, ISL4, ISL9, ISL10	Y	0.090 MM	0.090 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	ISL3, ISL4, ISL9, ISL10	Y	0.076 MM	0.076 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	TOP, BOTTOM	Y	0.175 MM	0.175 MM		0.130 MM	0.130 MM
70_OHM_DIFF	ISL3, ISL10	Y	0.135 MM	0.135 MM		0.130 MM	0.130 MM
70_OHM_DIFF	ISL4, ISL9	Y	0.155 MM	0.155 MM		0.130 MM	0.130 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.160 MM	0.160 MM
80_OHM_DIFF	ISL3, ISL10	Y	0.109 MM	0.109 MM		0.160 MM	0.160 MM
80_OHM_DIFF	ISL4, ISL9	Y	0.125 MM	0.125 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
75_OHM_DIFF	TOP, BOTTOM	Y	0.160 MM	0.160 MM		0.160 MM	0.160 MM
75_OHM_DIFF	ISL3, ISL10	Y	0.120 MM	0.120 MM		0.140 MM	0.140 MM
75_OHM_DIFF	ISL4, ISL9	Y	0.140 MM	0.140 MM		0.140 MM	0.140 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL3, ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL4, ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
95_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
95_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM
95_OHM_DIFF	ISL3, ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
95_OHM_DIFF	ISL4, ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	TOP, BOTTOM	Y	0.091 MM	0.091 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL3, ISL10	Y	0.075 MM	0.075 MM		0.300 MM	0.300 MM
100_OHM_DIFF	ISL4, ISL9	Y	0.085 MM	0.085 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.28:1_SPACING	*	0.228 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V5_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
NB_STATIC	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
1.5X_DIELECTRIC	*	0.105 MM	?
5X_DIELECTRIC	*	0.350 MM	?

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SYNC MASTER=K99_MLB		SYNC DATE=04/08/2010	
K99 RULE DEFINITIONS			
Apple Inc.		DRAWING NUMBER	051-8467
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1UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

MURATA

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0629	2	CAP, 1UF, 6.3V, 10%, 0402	C7203,C7940	CRITICAL	SS_CAP_1UF	138S0628	2	CAP, 1UF, 6.3V, 10%, 0402	C7203,C7940	CRITICAL	MU_CAP_1UF	138S0630	2	CAP, 1UF, 6.3V, 10%, 0402	C7203,C7940	CRITICAL	TY_CAP_1UF

2.2UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

MURATA

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	TY_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	SS_CAP_2_2UF	138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	MU_CAP_2_2UF	138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	TY_CAP_2_2UF
138S0632	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	SS_CAP_2_2UF	138S0633	12	CAP, 2.2UF, 6.3V, 20%, 0402	C241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	MU_CAP_2_2UF	138S0634	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	TY_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	SS_CAP_2_2UF	138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	MU_CAP_2_2UF	138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	TY_CAP_2_2UF
138S0632	9	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	SS_CAP_2_2UF	138S0633	9	CAP, 2.2UF, 6.3V, 20%, 0402	C241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	MU_CAP_2_2UF	138S0634	9	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	TY_CAP_2_2UF

10UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

MURATA

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0626	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	SS_CAP_10UF	138S0625	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	MU_CAP_10UF	138S0627	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	TY_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C1280,C1281,C1282,C1283,C1284,C1285,C1286,C1287,C1288	CRITICAL	SS_CAP_10UF	138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C1280,C1281,C1282,C1283,C1284,C1285,C1286,C1287,C1288	CRITICAL	MU_CAP_10UF	138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C1280,C1281,C1282,C1283,C1284,C1285,C1286,C1287,C1288	CRITICAL	TY_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C1280,C1281,C1282,C1283,C1284,C1285,C1286,C1287,C1288	CRITICAL	SS_CAP_10UF	138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C1280,C1281,C1282,C1283,C1284,C1285,C1286,C1287,C1288	CRITICAL	MU_CAP_10UF	138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C1280,C1281,C1282,C1283,C1284,C1285,C1286,C1287,C1288	CRITICAL	TY_CAP_10UF

22UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS

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TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0635	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213	CRITICAL	SS_CAP_22UF	138S0676	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213	CRITICAL	MU_CAP_22UF	138S0688	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213	CRITICAL	TY_CAP_22UF
138S0635	3	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213	CRITICAL	SS_CAP_22UF	138S0676	3	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213	CRITICAL	MU_CAP_22UF	138S0688	3	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213	CRITICAL	TY_CAP_22UF
138S0635	5	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213,C1214,C1215	CRITICAL	SS_CAP_22UF	138S0676	5	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213,C1214,C1215	CRITICAL	MU_CAP_22UF	138S0688	5	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213,C1214,C1215	CRITICAL	TY_CAP_22UF

SYNC MASTER=K16 MLB SYNC DATE=06/01/2010

Acoustic Cap BOM Config Tables

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