1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

K62 MLB

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2011-02-08

LAST_MODIFIED=Tue Feb 8 15:20:30 2011

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78	MXM PCIE CAPS	N/A K62
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85	DisplayPort/T29 A MUXing	(MASTER) (MASTER)
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DRAWING
TITLE=K22
ABBREV=DRAWING
LAST MODIFIED=Tue Feb 8 15 20 30 2011

DRAWING TITLE: SCH,K62,MLB

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D
REVISION: 10.1.0
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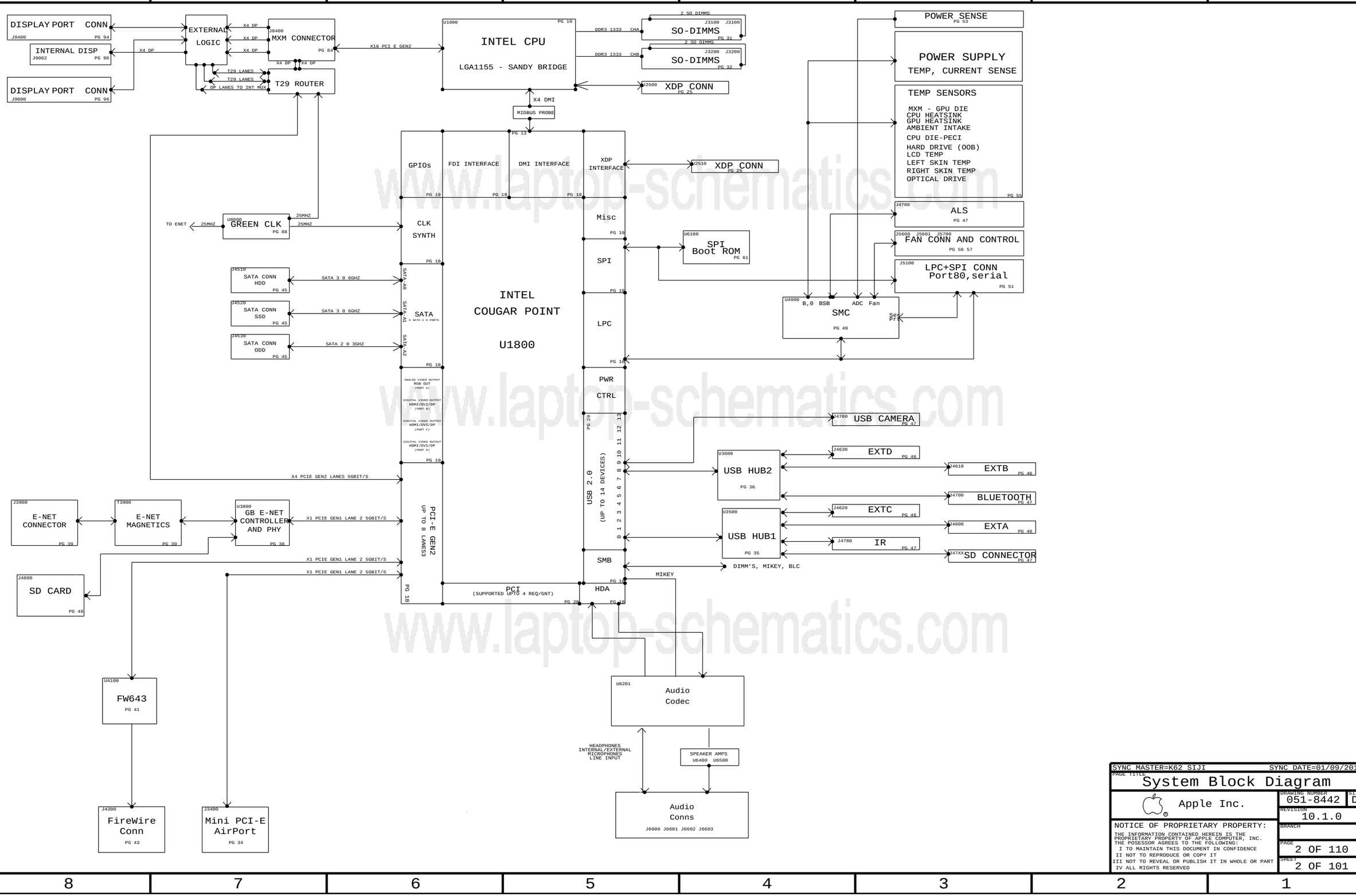

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SYNC MASTER=K62 SIJI SYNC DATE=01/09/2011

PAGE TITLE

System Block Diagram

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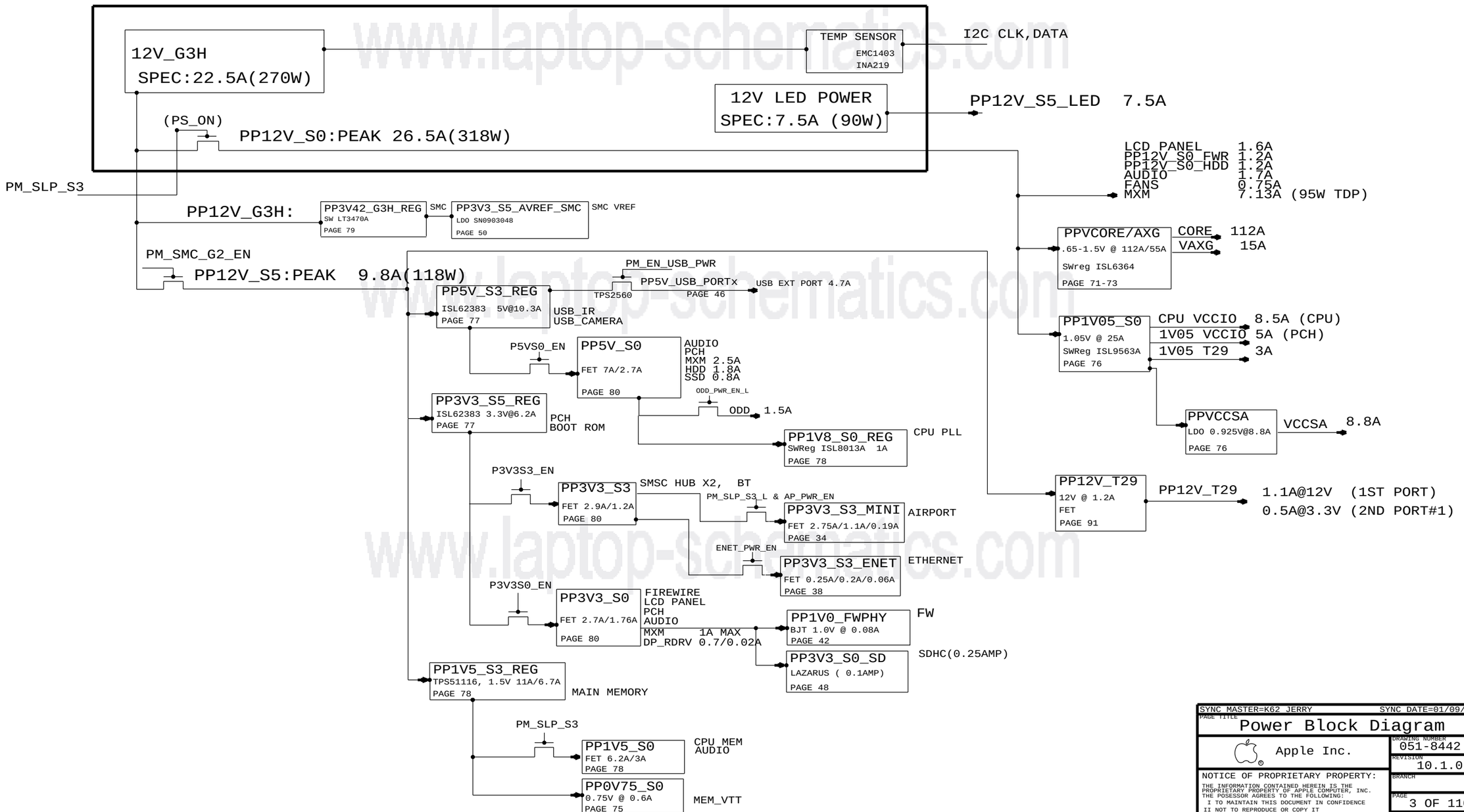
K75F AC/DC POWER SUPPLY (SPEC:310W)



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SYNC MASTER=K62 JERRY SYNC DATE=01/09/2011

PAGE TITLE: Power Block Diagram

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
085-1226	PCBA,MLB,DEV,K62	DEVELOPMENT,DEV_GROUP
639-1769	PCBA,MLB,K62,2.8G,4C,PRQ,P2_ODD	K62,2P8GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P2,YES_DBG
639-1770	PCBA,MLB,K62,3.1G,4C,PRQ,P2_ODD	K62,3P1GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P2,YES_DBG
639-1771	PCBA,MLB,K62,3.4G,4C,PRQ,P2_ODD	K62,3P4GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P2,YES_DBG
639-2186	PCBA,MLB,K62,2.8G,4C,PRQ,P2_ODD,NO_DBG	K62,2P8GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P2,NO_DBG
639-2187	PCBA,MLB,K62,3.1G,4C,PRQ,P2_ODD,NO_DBG	K62,3P1GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P2,NO_DBG
639-2188	PCBA,MLB,K62,3.4G,4C,PRQ,P2_ODD,NO_DBG	K62,3P4GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P2,NO_DBG
639-2124	PCBA,MLB,K62,2.8G,4C,PRQ,P1_ODD	K62,2P8GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P1,YES_DBG
639-2121	PCBA,MLB,K62,3.1G,4C,PRQ,P1_ODD	K62,3P1GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P1,YES_DBG
639-2123	PCBA,MLB,K62,3.4G,4C,PRQ,P1_ODD	K62,3P4GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P1,YES_DBG
639-2129	PCBA,MLB,K62,2.8G,4C,PRQ,P1_ODD,NO_DBG	K62,2P8GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P1,NO_DBG
639-2131	PCBA,MLB,K62,3.1G,4C,PRQ,P1_ODD,NO_DBG	K62,3P1GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P1,NO_DBG
639-2130	PCBA,MLB,K62,3.4G,4C,PRQ,P1_ODD,NO_DBG	K62,3P4GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P1,NO_DBG

BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC1	COMMON,ALTERNATE,MXM,FCIM,CPU_1V5_SENSE,CPU_VCCSA_SENSE,1V05_PCH_SENSE
BASIC2	HUB_USX2061,AP,BT,IR,T29,VAXG,PRODUCTION
DEV_GROUP	VREFMRGN_A,VREFMRGN_B,DIMM_1V5_SENSE
YES_DBG	XDP,XDP_CONN,XDP_CPU_BPM,MOJOMUX:YES,LPCPLUS:YES
NO_DBG	MOJOMUX:NO,LPCPLUS:NO

CPU SOCKET & ILM SUB-BOMS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0071	1	SOCKET,LGA1155,CPU-LF	U1000	CRITICAL	TYCO_SOCKET
604-1474	1	ASSY,PURCHASED,ILM,TYCO	ILM	CRITICAL	TYCO_SOCKET
511S0073	1	SOCKET,LGA1155,CPU-LF	U1000	CRITICAL	MOLEX_SOCKET
604-1161	1	ASSY,PURCHASED,ILM,MOLEX	ILM	CRITICAL	MOLEX_SOCKET

BOM NUMBER	BOM NAME	BOM OPTIONS
085-2451	SUB ASSY,CPU SOCKET,K62,TYCO	TYCO_SOCKET
085-2450	SUB ASSY,CPU SOCKET,K62,MOLEX	MOLEX_SOCKET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
085-2451	1	TYCO CPU SOCKET AND ILM	SKT_ILM	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
085-2450	085-2451		SKT_ILM	MOLEX ALTERNATE

BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL
4	POWER
5	POWER
6	SIGNAL
7	GROUND
BOTTOM	SIGNAL

COMMON

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	337S4088	1	IC COUGAR POINT SLJ4F BD82Z68 PRQ B3	U1800	CRITICAL	
	353S3055	2	IC PI3VEDP212 X2 DP MUX QFN	U9390,U9590	CRITICAL	
	338S0753	1	IC,FW643,1394B_PCIE,PHY/LINK	U4100	CRITICAL	
	825-7122	1	MLB LABEL,48.0X4.8	X14	CRITICAL	
	343S0534	1	IC,BCM57765,ENET&SD,8X8	U3900	CRITICAL	
RAW:	341T0184	1	FLASH,EFI BOOTROM,K60/K62	U6100	CRITICAL	
RAW:	335S0539	1	SFLASH ENET 2MBIT,CIV	U3990	CRITICAL	
	338S0945	1	T29 ROUTER, IC, ASSP	U9700	CRITICAL	T29
RAW:	335S0550	1	IC,T29 SERIAL EEPROM	U9790	CRITICAL	T29
RAW:	337S3997	2	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330,U9530	CRITICAL	T29
RAW:	338S0878	1	IC,SMC,K62	U4900	CRITICAL	

CPUS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4042	1	SNB SR00D PRQ D2 2 8 95W 4+1 6M LGA	CPU	CRITICAL	2P8GHZ_SNB_CPU
337S4040	1	SNB SR00Q PRQ D2 3 1 95W 4+1 6M LGA	CPU	CRITICAL	3P1GHZ_SNB_CPU
337S4041	1	SNB SR00B PRQ D2 3 4 95W 4+1 8M LGA	CPU	CRITICAL	3P4GHZ_SNB_CPU

K62 PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-8442	1	SCH,MLB,K62	SCH1		K62
820-2828	1	PCBF,MLB,K62	MLB1		K62

K62 ALTERNATE PARTS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0298	128S0293		ALL	330UF
371S0679	371S0652		ALL	PIN DIODE
377S0107	377S0066		ALL	USB DIODE
376S0972	376S0612		ALL	ROHM TRA-BJT

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SYNC MASTER=K62 AARON SYNC DATE=N/A

PAGE TITLE
BOM Configuration

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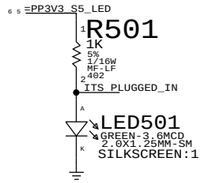
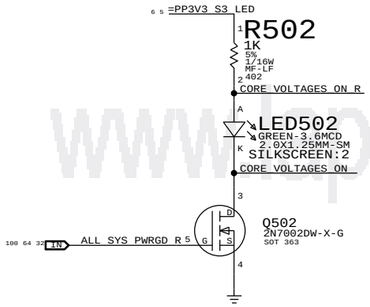
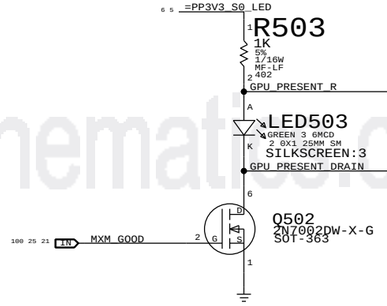
S5 Led



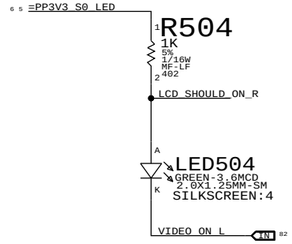
ALL_SYS_PWRGD Led



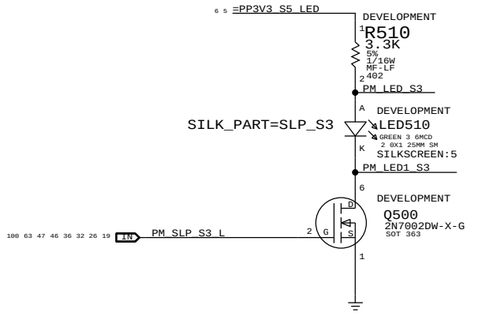
MXM PWR GOOD Led

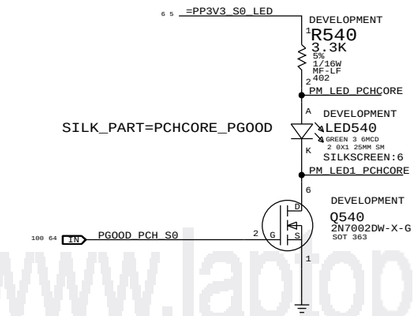


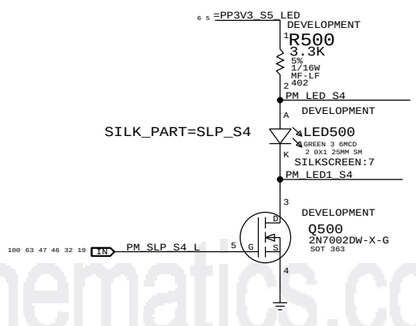
VIDEO ON Led

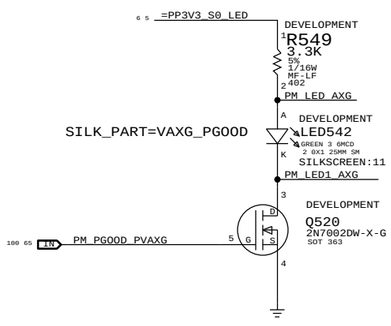


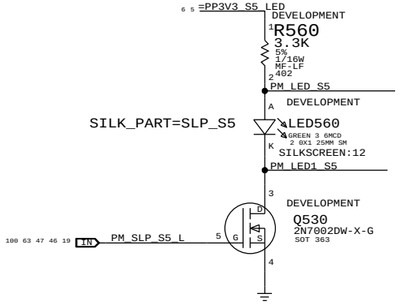
PROTO DEBUG LEDS ARE SHOWN BELOW

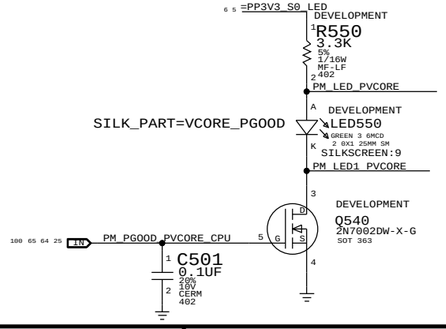


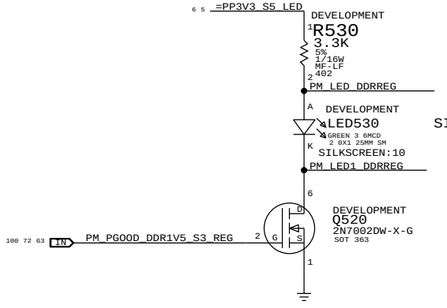


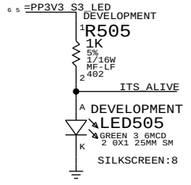












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PAGE TITLE: DEBUG LEDS

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DRAWING NUMBER: 051-8442 SIZE: D
REVISION: 10.1.0
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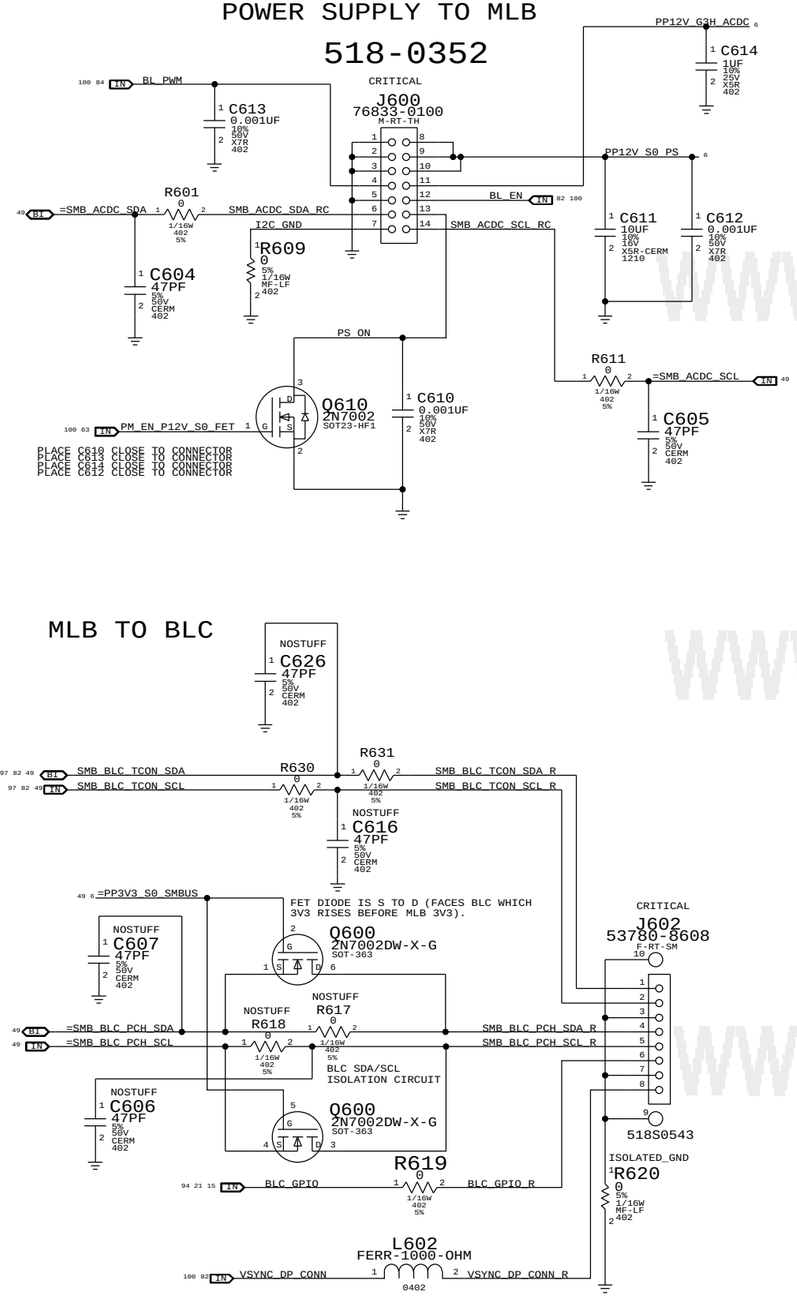
POWER SUPPLY TO MLB

518-0352



MLB TO BLC

"S0" RAILS

ONLY ON IN RUN

PP0V75_S0	PPVTT_S0_DDR_LDO	72
	=PP0V75_S0_MEM_VTT_S0FET	32
PPVTT_S0_DDR	PPVTT_S0_DDR_FET	32
	=PP0V75_S0_MEM_VTT_B	31
	=PP0V75_S0_MEM_VTT_A	30
PPVCORE_S0_CPU	PPVCORE_S0_CPU_REG	66 67
	=PPVCORE_S0_CPU	13 16 50 65
PPVAXG_S0	PPVAXG_S0_REG	67
	=PPVAXG_S0_CPU	13 17 50 65
PP1V05_S0	PP1V05_S0_REG	68
	=PP1V05_S0_PWR	50
	=PPVCCIO_S0_XDP	25
	=PPVCCIO_S0_CPU	10 11 13 16 65
	=PPVCCIO_S0_SMC	46 47
	=PP1V05_S0_PCH_PWR	50
	=PPVCCSA_S0_INPUT_PWR	50 69
	=PP1V05_S0_CK505	26
PP1V05_S0_PCH	PP1V05_S0_PCH_SNS	50
	=PP1V05_S0_PCH_VCC_DMI	22 24
	=PP1V05_S0_PCH_VCCADPLL	17
	=PP1V05_S0_PCH_VCCIO_DMI	22 24
	=PP1V05_S0_PCH_VCCIO_SATA	18 22 24
	=PP1V05_S0_PCH_VCCIO_PCIE	18 19 22 24
	=PP1V05_S0_PCH_VCC_CORE	22 24
	=PP1V05_S0_PCH_VCCIO_USB	22 24
	=PP1V05_S0_PCH	18 24 80
	=PP1V05_S0_PCH_VCCDIFFCLK	22 24
	=PP1V05_S0_PCH_VCCSSC	22 24
	=PP1V05_S0_PCH_V_PROC_IO	22 24
	=PP1V05_S0_PCH_VCCASW	22 24
	=PP1V05_S0_P1V05T29FET	81
PP1V05_S0_INPUT_VCCSA	PPVCCSA_S0_INPUT_SNS	50
	=PPVCCIO_S0_CPU_VCCSA	69
PPVCCSA_S0_CPU	PPVCCSA_S0_FET	69
	=PPVCCSA_S0_CPU	13 50
	=PPVCCSA_S0_PWRCTL	64
PP1V5_S0	PP1V5_S0_FET	74
	=PP1V5_S0_AUD_DIG	56
	=PP1V5_S0_CK505	26
	=PP1V5_S0_MINI	33
	=PP1V5_S0_PWR	50
	=PP1V5_S0_DP	84
PP1V5_S0_CPU_MEM	PP1V5_S0_CPU_MEM_SNS	50
	=PP1V5_S0_CPU_MEM	11 13 16 28 29
PP3V3_S0	PP3V3_S0_FET	74
	=PP3V3_S0_PCH	18 21 24
	=PP3V3_S0_FAN	53 54
	=PP3V3_S0_PCH_VCCADAC	17
	=PPSPD_S0_MEM_A	30 47
	=PPSPD_S0_MEM_B	31
	=PP3V3_S0_AUDIO	56 58 59 60 61 62
	=PP3V3R1V5_S0_PCH_VCCSUSHDA	24
	=PP3V3_S0_SMBUS	6 49
	=PP3V3_S0_SMC_LS	47 51
	=PP3V3_S0_SMBUS_SMC_0	49
	=PP3V3_S0_SMBUS_SMC_B	49
	=PP3V3_S0_SMBUS_SMC_MGMT	49
	=PP3V3_S0_MXM	21 64 76 77
	=PP3V3_S0_ODD	42
	=PP3V3_S0_SATALED	18 42
	=PP3V3_S0_SENSE	50 52
	=PP3V3_S0_PWRCTL	63 64 74 81
	=PP3V3_S0_PCH_VCC3_3_GPIO	22 24
	=PP3V3_S0_FWPHY	39 40 41
	=PP3V3_S0_DP	82
	=PP3V3_S0_PCH_VCC3_3_PCI	22 24
	=PP3V3_S0_CK505	26
	=PP3V3_S0_PCH_GPIO	20 45
	=PP3V3_S0_PCH_STRAPS	15
	=PP3V3_S0_PCH_VCC3_3_SATA	22 24
	=PP3V3_S0_RSTBUF	11 27
	=PP3V3_S0_PCH_PM	27
	=PP3V3_S0_SMBUS_SMC_BSA	49
	=PP3V3_S0_SDCARD	45
	=PP3V3_S0_P1V05_VREG	68
	=PP3V3_S0_PCH_VCC3V3	22 24
	=PP3V3_S0_VRD	65 68
	=PP3V3_S0_LED	5
	=PP3V3_S0_P3V3T29FET	81
	=PP3V3_S0_DPSDRVA	85
	=PP3V3_S0_DPSDRVB	87
	=PP3V3_S0_INTDPMUX	84
	=PP3V3_S0_T29PWRCTL	81
	=PP3V3_S0_T29I2C	49
	=PP3V3_S0_ENET_PHY	36 37

"S0" RAILS

PP1V8_S0	PP1V8_S0_REG	72
	=PP3V3R1V8_S0_PCH_VCCDFTERM	22 24
	=PP1V8R1V5_S0_PCH_VCCVRM	24 80
	=PP1V8_S0_CPU_PLL	13 16
	=PP1V8_S0_PCH	19
	=PP1V8_S0_PWRCTL	64
PP5V_S0	PP5V_S0_FET	74
	=PP5V_S0_AUDIO	56
	=PP5V_S0_SATA	42
	=PP5V_S0_MXM	76
	=PP5V_S0_VRD	65 67
	=PP5V_S0_ISENSE	50
	=PP5V_S0_PCH	24
	=PP5V_S0_P1V05_VREG	68
	=PP5V_S0_LPCPLUS	48
	=PP5V_S0_P1V8_REG	72
PP12V_S0	PP12V_S0_PS	6
	=PP12V_S0_AUDIO_SPKRAMP	58 59
	=PP12V_S0_VRD	65
	=PP12V_S0_MXM_PWR	50
	=PP12V_S0_LCD	82
	=PP12V_S0_P1V05_VREG	68
	=PP12V_S0_PWRCTL	63 64 81
	=PP12V_S0_SENSE	51
	=PP12V_S0_FW	41
	=PP12V_S0_CPU_VCCSA	69
	=PP12V_S0_SATA	42
	=PP12V_S0_FAN	53 54
PP12V_S0_MXM	PP12V_S0_MXM_SNS	50
	=PP12V_S0_MXM	76

"S3" RAILS

ON IN RUN AND SLEEP

PP1V5_S3	PP1V5_S3_REG	72
	=PP1V5_S3_MEM_PWR	50
	=PP1V5_S3_S0FET	74
PP1V5_S3_MEM	PP1V5_S3_MEM_SNS	50
	=PP1V5_S3_MEMRESET	32
	=PP1V5_S3_MEM_A	28 29 30
	=PP1V5_S3_MEM_B	28 29 31
PP3V3_S3	PP3V3_S3_FET	74
	=PP3V3_S3_BT	44
	=PP3V3_S3_SMBUS_SMC_A	49
	=PP3V3_S3_MINI	33
	=PP3V3_S3_PWRCTL	64 74 83
	=PP3V3_S3_MEMRESET	32
	=PP3V3_S3_USB_HUB	34 35
	=PP3V3_S3_ENET_PHY	36
	=PP3V3_S3_SDCARD	44 45
	=PP3V3_S3_VREFMRGN	28
	=PP3V3_S3_VRD	72
	=PP3V3_S3_LED	5
	=PP3V3_SW_DPAPWR	79
	=PP3V3_SW_DPBPWR	79
	=PP3V3_S3_SYSCLK	80
	=PP3V3_S3_P3V3R2V9_REG_A	83
	=PP3V3_S3_P3V3R2V9_REG_B	83
	=PP3V3_S3_PCH	21
PP5V_S3	PP5V_S3_REG	71
	=PP5V_S3_USB	43
	=PP5V_S3_S0FET	74
	=PP5V_S3_CAMERA	44
	=PP5V_S3_IR	44
	=PP5V_S3_MEMRESET	32
	=PP5V_S3_DDR_VREG	72
	=PP5V_S3_VREFMRGN	28
	=PP5V_S3_P3V3R2V9_REG_A	83
	=PP5V_S3_P3V3R2V9_REG_B	83

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER AND IN S5

PP3V3_S5	PP3V3_S5_REG	71
	=PP3V3_S5_PCH	18 19 21 24
	=PP3V3_S5_PCH_GPIO	20
	=PP3V3_S5_ROM	48 55
	=PP3V3_S5_PCH_VCCSUS3_3_USB	22 24
	=PP3V3_S5_PWRCTL	11 63 64
	=PP3V3_S5_S3FET	74
	=PP3V3_S5_S0FET	74
	=PP3V3_S5_PCH_STRAPS	15
	=PP3V3_S5_XDP	25
	=PP3V3_S5_LPCPLUS	48
	=PP3V3_S5_PCH_VCCDSW	22 24
	=PP3V3_S5_USB_HUB	34
	=PP3V3_S5_CPU_VCCSA	69
	=PP3V3_S5_PCH_VCCSPI	22 24
	=PP3V3_S5_VRD	71
	=PP3V3_S5_LED	5
	=PP3V3_S5_MEMRESET	32
	=PP3V3_S5_RSTBUF	27
	=PP3V3_S5_SMCUSBMUX	43
	=PP3V3_S5_P3V3R2V9_A	83
	=PP3V3_S5_P3V3R2V9_B	83
	=PP3V3R1V5_S5_PCH_VCCSUSHDA	24
PP5V_S5	PP5V_S5_LDO	71
	=PP5V_S5_PCH	24
PP12V_S5	PP12V_S5_FET	75 98
	=PP12V_S5_DDR_VREG	72
	=PP12V_S5_P5VS3_VREG	71
	=PP12V_S5_PWRCTL	33 64 74
	=PP12V_S5_T29_A	83
	=PP12V_S5_T29_B	83

"G3H" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER AND IN G3HOT PER SMC

G3H: ALIASES

PP3V42_G3H	PP3V42_G3H_REG	73
	=PP3V3_G3H_RTC_D	27
	=PP3V3_G3H_SMC	46 47
	=PP3V3_G3H_SMCUSBMUX	43
	=PP3V3_G3H_LPCPLUS	48
PP12V_G3H	PP12V_G3H_ACDC	6
	=PP12V_G3H_S5_FET	75
	=PP12V_G3H_3V42	73

T29 RAILS

PP3V3_S0_T29	PP3V3_T29_FET	81
	=PP3V3_T29_RTR	80 81 89 90
PP1V05_S0_T29	PP1V05_T29_FET	81
	=PP1V05_T29_RTR	90
	=PP1V05_T29	81

GND RAILS

GND
MIN LINE WIDTH=0 6MM
MIN NECK WIDTH=0 2MM
VOLTAGE=0V
NET SPACING TYPE=GND
MAKE BASE=TRUE
MAX NECK LENGTH=4 1 MM

SYNC MASTER=K62_AARON SYNC DATE=12/30/2010

PAGE TITLE: Power Conn / Alias

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

REVISION: 10.1.0

BRANCH:

PAGE: 6 OF 110

SHEET: 6 OF 101

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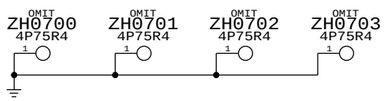
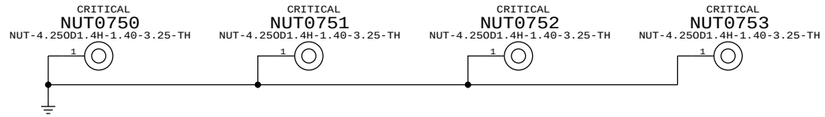
CPU Heatsink

4mm Plated Holes (998-0850)



DIMM CONNECTOR NUTS

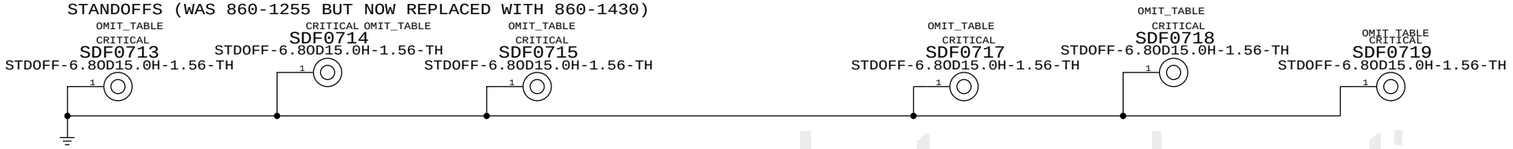
Nuts (805-9582)



PCH HEATSINK MTG HOLES (NON-PLATED HOLE ON PCB ONLY)

Rear Cover

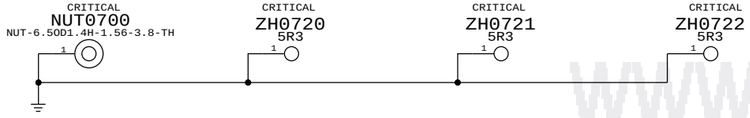
STANDOFFS (WAS 860-1255 BUT NOW REPLACED WITH 860-1430)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
860-1430	6	STANDOFF,MLB,K60/K62	SDF0713 SDF0714 SDF0715 SDF0717 SDF0718 SDF0719	COMMON

Backer Plate

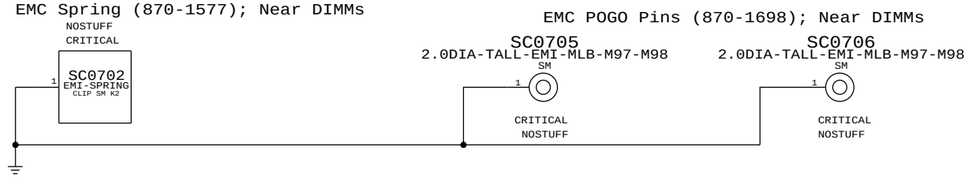
Nuts (835-0269)



For EMC

EMC Spring (870-1577); Near DIMMs

EMC POGO Pins (870-1698); Near DIMMs



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SYNC MASTER=K62_AARON SYNC DATE=11/30/2009

PAGE TITLE: Holes

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

REVISION: 10.1.0

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PAGE: 7 OF 110

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UNUSED CPU SIGNALS

10 TP_CPU_RSVD<16..1> = NC_CPU_RSVD<16..1> MAKE_BASE=TRUE NO_TEST=TRUE
10 TP_CPU_RSVD<46..19> = NC_CPU_RSVD<46..19> MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED PCI ALIASES

20 TP_PCI_AD<31..0> = NC_PCI_AD<31..0> MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_PCI_C_BE_L<3..0> = NC_PCI_C_BE_L<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_PCI_PAR = NC_PCI_PAR MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_PCI_RESET_L = NC_PCI_RESET_L MAKE_BASE=TRUE NO_TEST=TRUE

18 TP_LPC_DREQ0_L = NC_LPC_DREQ0_L MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED MEM ALIASES

12 TP_MEM_A_DQ_CB<7..0> = NC_MEM_A_DQ_CB<7..0> MAKE_BASE=TRUE NO_TEST=TRUE
12 TP_MEM_A_DQS_N<8> = NC_MEM_A_DQSN<8> MAKE_BASE=TRUE NO_TEST=TRUE
12 TP_MEM_A_DQS_P<8> = NC_MEM_A_DQSP<8> MAKE_BASE=TRUE NO_TEST=TRUE

12 TP_MEM_B_DQ_CB<7..0> = NC_MEM_B_DQ_CB<7..0> MAKE_BASE=TRUE NO_TEST=TRUE
12 TP_MEM_B_DQS_N<8> = NC_MEM_B_DQSN<8> MAKE_BASE=TRUE NO_TEST=TRUE
12 TP_MEM_B_DQS_P<8> = NC_MEM_B_DQSP<8> MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED MISC ALIASES

18 TP_HDA_SDIN1 = NC_HDA_SDIN1 MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_HDA_SDIN2 = NC_HDA_SDIN2 MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_HDA_SDIN3 = NC_HDA_SDIN3 MAKE_BASE=TRUE NO_TEST=TRUE

21 TP_PCH_PWM0 = NC_PCH_PWM0 MAKE_BASE=TRUE NO_TEST=TRUE
21 TP_PCH_PWM1 = NC_PCH_PWM1 MAKE_BASE=TRUE NO_TEST=TRUE
21 TP_PCH_PWM2 = NC_PCH_PWM2 MAKE_BASE=TRUE NO_TEST=TRUE
21 TP_PCH_PWM3 = NC_PCH_PWM3 MAKE_BASE=TRUE NO_TEST=TRUE
21 TP_PCH_SST = NC_PCH_SST MAKE_BASE=TRUE NO_TEST=TRUE

18 TP_PCH_CL_CLK1 = NC_PCH_CL_CLK1 MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_PCH_CL_DATA1 = NC_PCH_CL_DATA1 MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_PCH_CL_RST1 = NC_PCH_CL_RST1 MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED PCIE ALIASES

18 TP_PCIE_CLK100M_PE5P = NC_PCIE_CLK100M_PE5P MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_PCIE_CLK100M_PE5N = NC_PCIE_CLK100M_PE5N MAKE_BASE=TRUE NO_TEST=TRUE

21 TP_PCIE_CLK100M_PE6P = NC_PCIE_CLK100M_PE6P MAKE_BASE=TRUE NO_TEST=TRUE
21 TP_PCIE_CLK100M_PE6N = NC_PCIE_CLK100M_PE6N MAKE_BASE=TRUE NO_TEST=TRUE

21 TP_PCIE_CLK100M_PE7P = NC_PCIE_CLK100M_PE7P MAKE_BASE=TRUE NO_TEST=TRUE
21 TP_PCIE_CLK100M_PE7N = NC_PCIE_CLK100M_PE7N MAKE_BASE=TRUE NO_TEST=TRUE

10 TP_PE_RX_N<3..0> = NC_PE_RXN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
10 TP_PE_RX_P<3..0> = NC_PE_RXP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE

10 TP_PE_TX_N<3..0> = NC_PE_TXN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
10 TP_PE_TX_P<3..0> = NC_PE_TXP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE

18 TP_PCIE_D2R_PERN4 = NC_PCIE_D2R_PERN4 MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_PCIE_D2R_PERP4 = NC_PCIE_D2R_PERP4 MAKE_BASE=TRUE NO_TEST=TRUE

18 TP_PCIE_R2D_PETN4 = NC_PCIE_R2D_PETN4 MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_PCIE_R2D_PETP4 = NC_PCIE_R2D_PETP4 MAKE_BASE=TRUE NO_TEST=TRUE

18 TP_PCIE_CLK100M_PE4P = NC_PCIE_CLK100M_PE4P MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_PCIE_CLK100M_PE4N = NC_PCIE_CLK100M_PE4N MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED USB ALIASES

20 TP_USB_1N = NC_USB_1N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_1P = NC_USB_1P MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_2N = NC_USB_2N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_2P = NC_USB_2P MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_3N = NC_USB_3N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_3P = NC_USB_3P MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_4N = NC_USB_4N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_4P = NC_USB_4P MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_5N = NC_USB_5N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_5P = NC_USB_5P MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_6N = NC_USB_6N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_6P = NC_USB_6P MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_7N = NC_USB_7N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_7P = NC_USB_7P MAKE_BASE=TRUE NO_TEST=TRUE

20 TP_USB_10N = NC_USB_10N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_10P = NC_USB_10P MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_11N = NC_USB_11N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_11P = NC_USB_11P MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_12N = NC_USB_12N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_12P = NC_USB_12P MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_13N = NC_USB_13N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_13P = NC_USB_13P MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED DISPLAY ALIASES

19 TP_CRT_IG_DDC_CLK = NC_CRT_IG_DDC_CLK MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_CRT_IG_DDC_DATA = NC_CRT_IG_DDC_DATA MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_CRT_IG_RED = NC_CRT_IG_RED MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_CRT_IG_GREEN = NC_CRT_IG_GREEN MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_CRT_IG_BLUE = NC_CRT_IG_BLUE MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_CRT_IG_HSYNC = NC_CRT_IG_HSYNC MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_CRT_IG_VSYNC = NC_CRT_IG_VSYNC MAKE_BASE=TRUE NO_TEST=TRUE

19 TP_DP_IG_B_MLN<3..0> = NC_DP_IG_B_MLN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_B_MLP<3..0> = NC_DP_IG_B_MLP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_B_AUX_N = NC_DP_IG_B_AUXN MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_B_AUX_P = NC_DP_IG_B_AUXP MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_B_HPD = NC_DP_IG_B_HPD MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_B_DDC_CLK = NC_DP_IG_B_CTRL_CLK MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_B_DDC_DATA = NC_DP_IG_B_CTRL_DATA MAKE_BASE=TRUE NO_TEST=TRUE

19 TP_DP_IG_C_MLN<3..0> = NC_DP_IG_C_MLN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_C_MLP<3..0> = NC_DP_IG_C_MLP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_C_AUX_N = NC_DP_IG_C_AUXN MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_C_AUX_P = NC_DP_IG_C_AUXP MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_C_HPD = NC_DP_IG_C_HPD MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_C_CTRL_CLK = NC_DP_IG_C_CTRL_CLK MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_C_CTRL_DATA = NC_DP_IG_C_CTRL_DATA MAKE_BASE=TRUE NO_TEST=TRUE

19 TP_DP_IG_D_MLN<3..0> = NC_DP_IG_D_MLN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_D_MLP<3..0> = NC_DP_IG_D_MLP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_D_AUXN = NC_DP_IG_D_AUXN MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_D_AUXP = NC_DP_IG_D_AUXP MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_D_HPD = NC_DP_IG_D_HPD MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_D_CTRL_CLK = NC_DP_IG_D_CTRL_CLK MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_D_CTRL_DATA = NC_DP_IG_D_CTRL_DATA MAKE_BASE=TRUE NO_TEST=TRUE

19 TP_SDVO_TVCLKINN = NC_SDVO_TVCLKINN MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_SDVO_TVCLKINP = NC_SDVO_TVCLKINP MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_SDVO_STALLN = NC_SDVO_STALLN MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_SDVO_STALLP = NC_SDVO_STALLP MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_SDVO_INTN = NC_SDVO_INTN MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_SDVO_INTP = NC_SDVO_INTP MAKE_BASE=TRUE NO_TEST=TRUE

18 TP_PCH_L_BKLTCTL = NC_PCH_L_BKLTCTL MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_PCH_L_BKLTEN = NC_PCH_L_BKLTEN MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_PCH_L_VDD_EN = NC_PCH_L_VDD_EN MAKE_BASE=TRUE NO_TEST=TRUE

18 TP_PCH_CLKOUT_DPN = NC_PCH_CLKOUT_DPN MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_PCH_CLKOUT_DPP = NC_PCH_CLKOUT_DPP MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED FDI ALIASES

10 TP_CPU_FDI_TX_N<7..0> = NC_CPU_FDI_TXN<7..0> MAKE_BASE=TRUE NO_TEST=TRUE
10 TP_CPU_FDI_TX_P<7..0> = NC_CPU_FDI_TXP<7..0> MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_PCH_FDI_RX_N<7..0> = NC_PCH_FDI_RXN<7..0> MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_PCH_FDI_RX_P<7..0> = NC_PCH_FDI_RXP<7..0> MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED SATA ALIASES

18 TP_SATA_D_D2RN = NC_SATA_D_D2RN MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_D_D2RP = NC_SATA_D_D2RP MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_D_R2D_CN = NC_SATA_D_R2D_CN MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_D_R2D_CP = NC_SATA_D_R2D_CP MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_E_D2RN = NC_SATA_E_D2RN MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_E_D2RP = NC_SATA_E_D2RP MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_E_R2D_CN = NC_SATA_E_R2D_CN MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_E_R2D_CP = NC_SATA_E_R2D_CP MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_F_D2RN = NC_SATA_F_D2RN MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_F_D2RP = NC_SATA_F_D2RP MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_F_R2D_CN = NC_SATA_F_R2D_CN MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_F_R2D_CP = NC_SATA_F_R2D_CP MAKE_BASE=TRUE NO_TEST=TRUE

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SYNC_MASTER=K62_SIJI SYNC_DATE=01/09/2011

PAGE TITLE
UNUSED SIGNAL ALIAS

Apple Inc.

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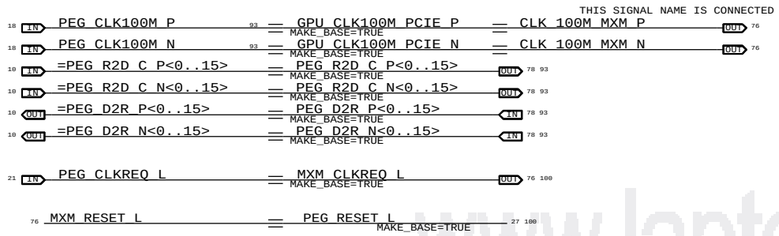
PEG Slot Support

THIS SIGNAL NAME IS CONNECTED TO MXM



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SYNC MASTER=K62 SIJI SYNC DATE=09/11/2010

PAGE TITLE
Signal Aliases

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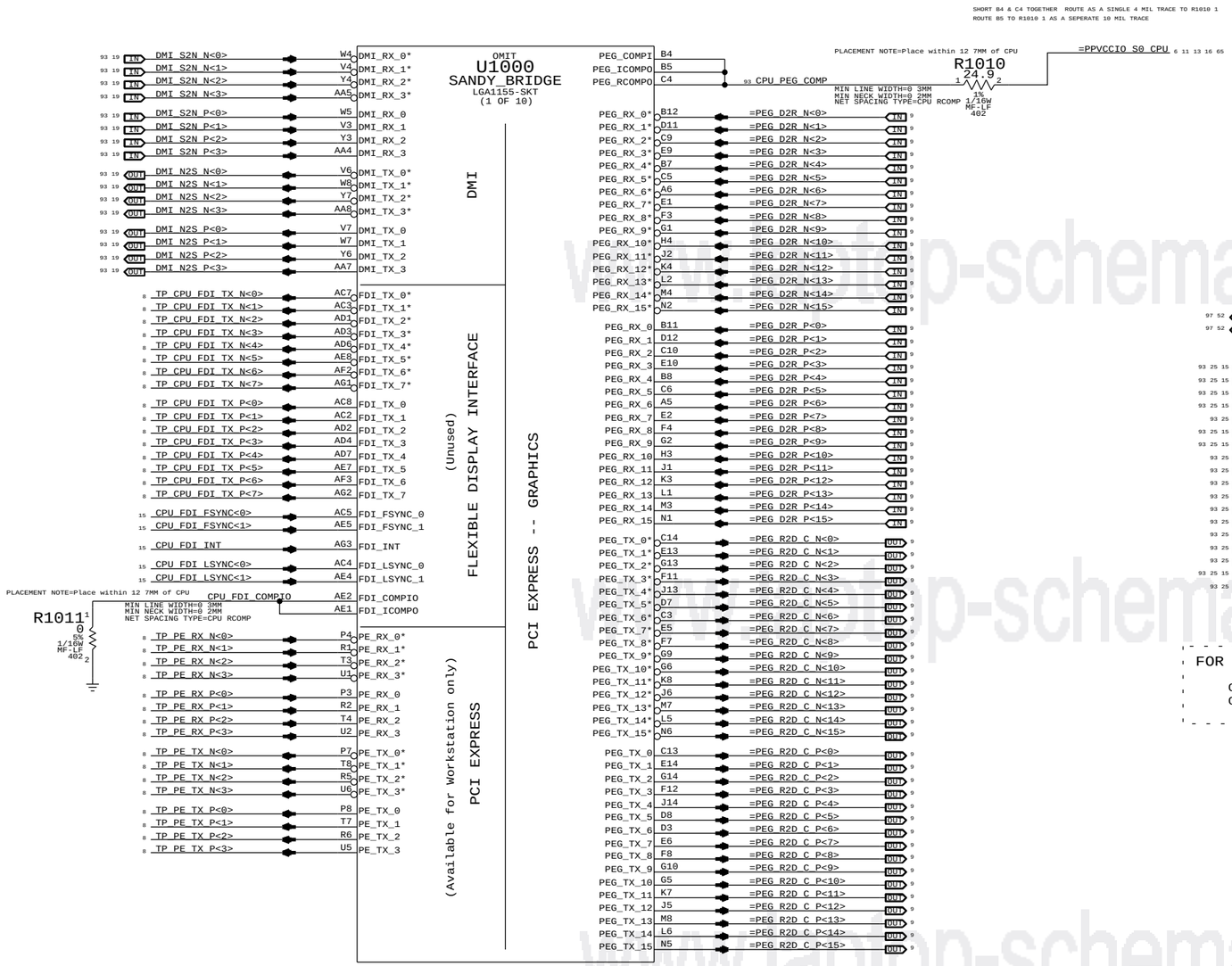

FOR SANDYBRIDGE PROCESSOR

CFG [6:5] :PCIE CONFIGURATION SELECT 11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [2] :PCIE LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED

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PAGE TITLE: CPU DMI/PEG/FDI/RSVD

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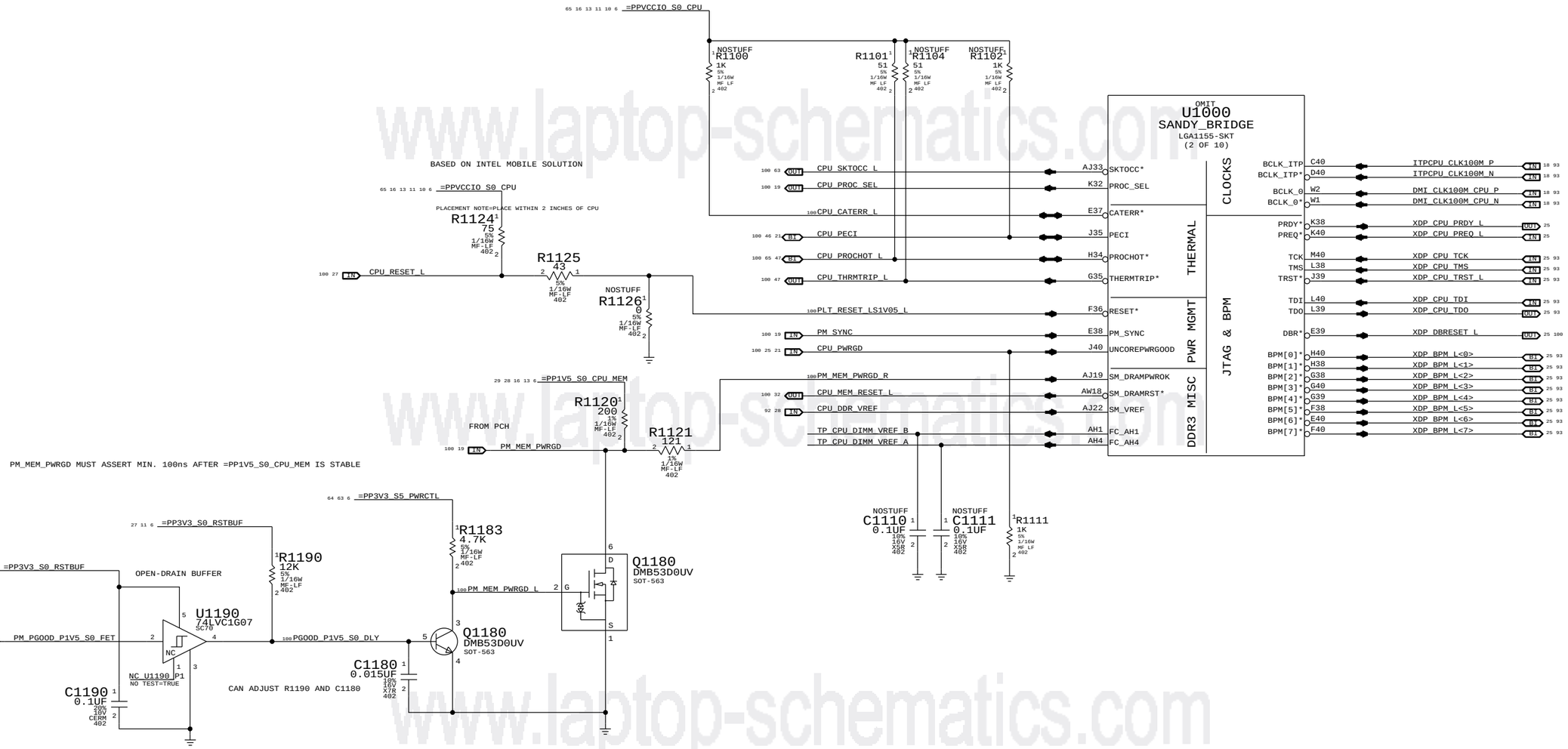

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PAGE TITLE	CPU CLOCK/MISC/JTAG
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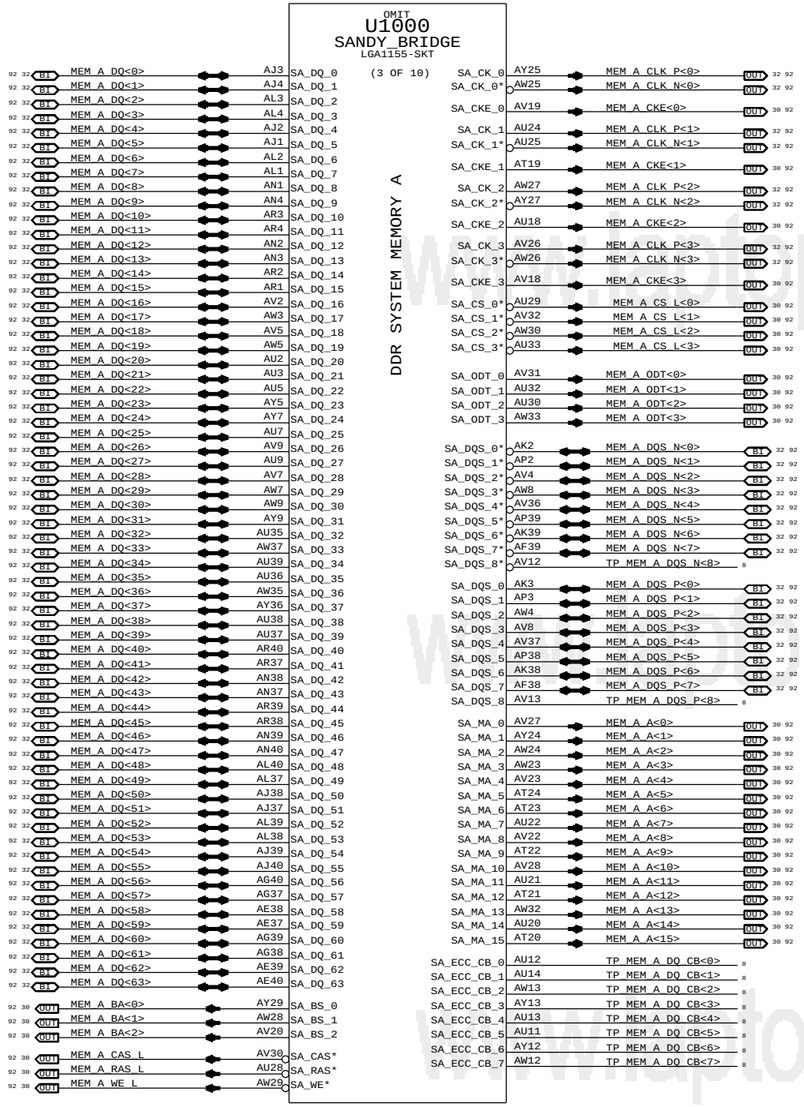

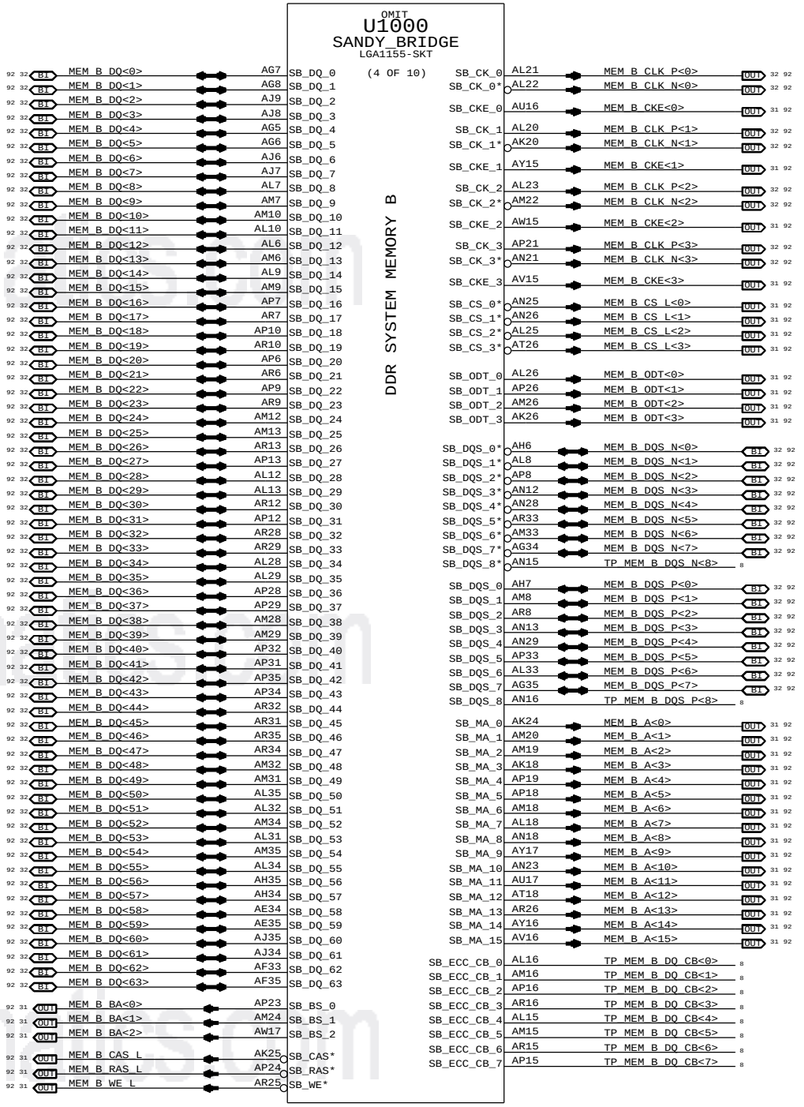

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SYNC DATE=01/09/2011

PAGE TITLE
CPU DDR3 INTERFACES

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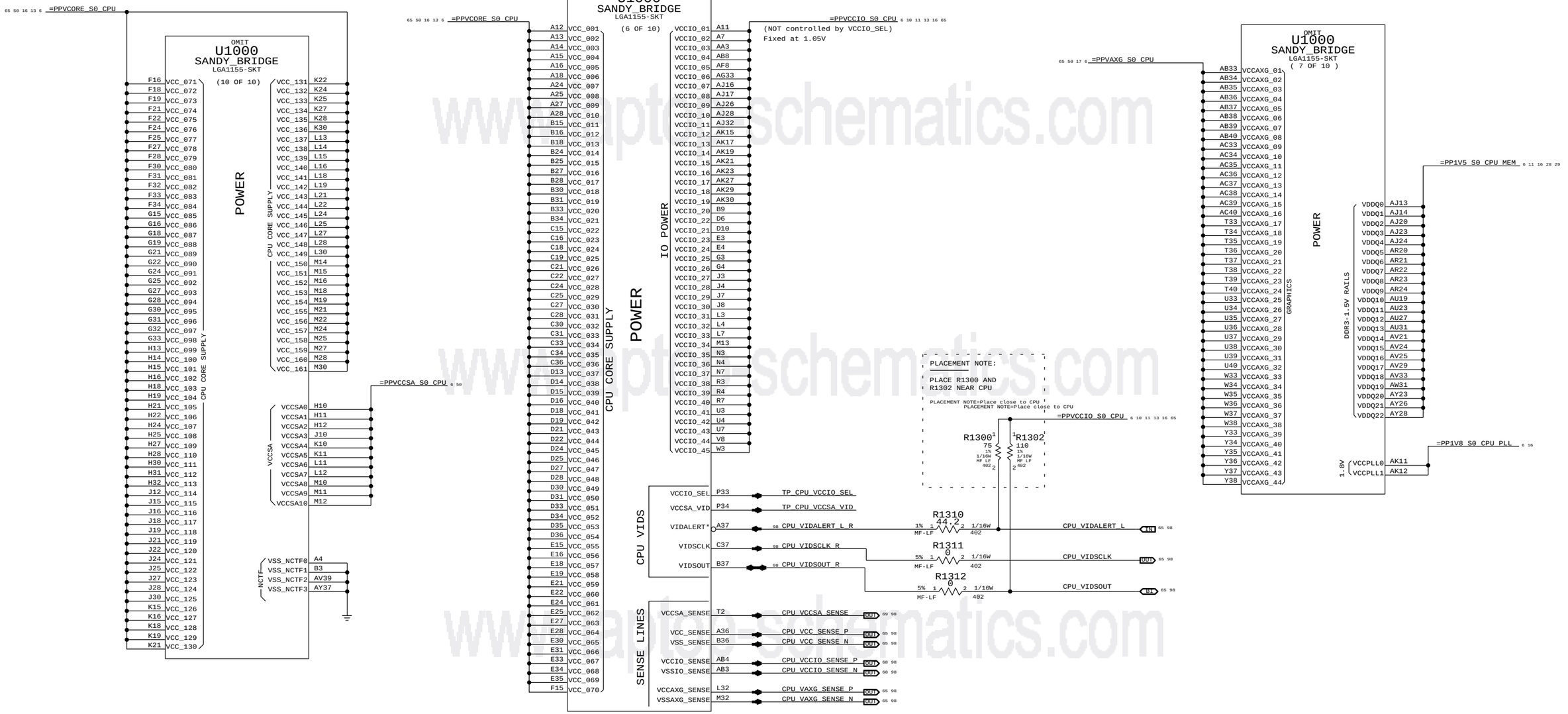

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PAGE TITLE
CPU POWER

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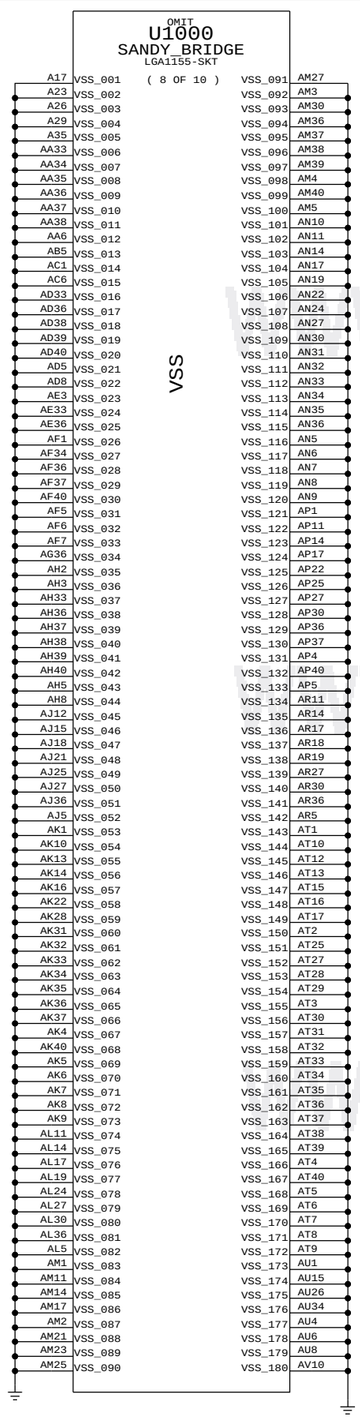

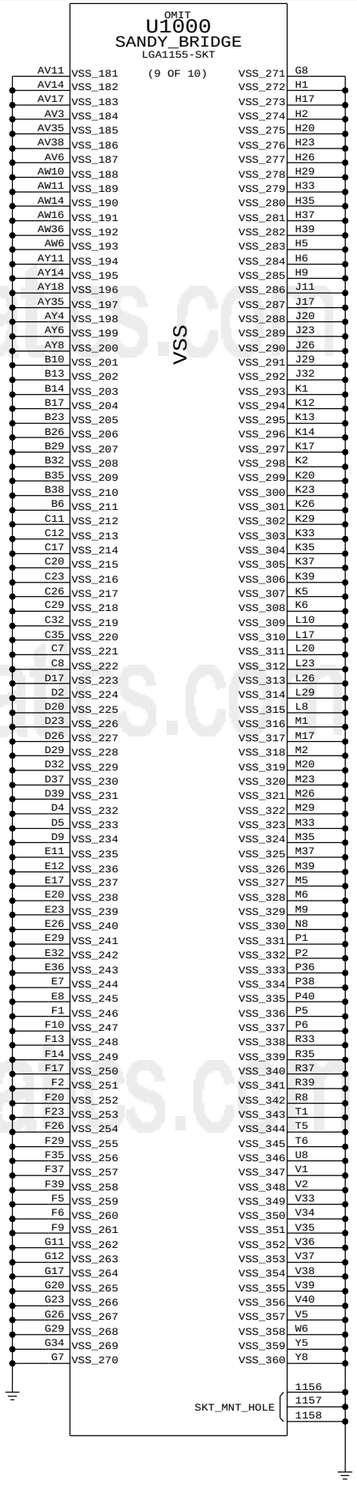

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PAGE TITLE
CPU GROUNDS

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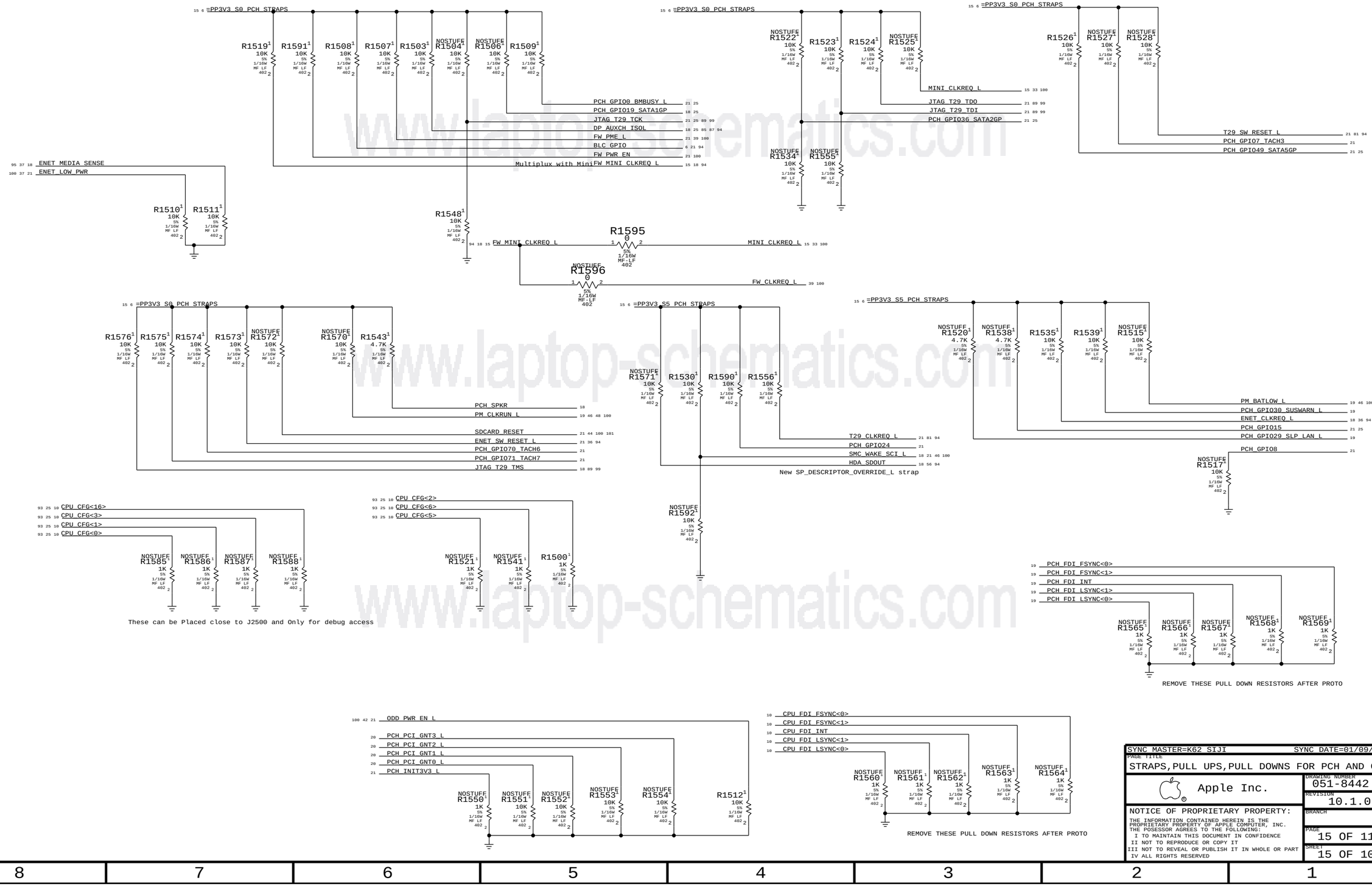

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CPU VCORE DECOUPLING

14x 22UF,0805 INTEL RECOMMENDATION 18X 22UF 0805 (14 Inside cavity and 4 North of processor)

16 13 6 =PPVCORE_S0_CPU
65 50

PLACEMENT_NOTE (C1600-C1613):

Place inside socket cavity

C1600 C1601 C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609
22UF 20% 6.3V CERM X5R 805 3

C1610 C1611 C1612 C1613
22UF 20% 6.3V CERM X5R 805 3

BULK CAPS ON CPU VREG PAGE 72

65 50 16 13 6 =PPVCORE_S0_CPU

10x 10UF and 10x 1UF CAPACITORS

Place inside socket cavity

C1620 C1621 C1622 C1623 C1624 C1625 C1626 C1627 C1628 C1629
10UF 20% 10V X5R 603

C1630 C1631 C1632 C1633 C1634 C1635 C1636 C1637 C1638 C1639
1UF 10% 10V X5R 402

CPU VCCIO DECOUPLING

8X 22UF 0805, 6X 10UF 0805 INTEL RECOMMENDATION 9X22UF 0805,16X 0805 placeholders

13 11 10 6 =PPVCCIO_S0_CPU
65

PLACEMENT_NOTE (C1650-C1657):

Place under socket cavity on secondary side.

C1650 C1651 C1652 C1653 C1654 C1655 C1656 C1657
22UF 20% 6.3V CERM X5R 805

PLACEMENT_NOTE (C1660-C1665):

Place at edge of socket.

BULK CAPS ON CPU VREG PAGE 72

C1660 C1661 C1662 C1663 C1664 C1665
10uF 20% 6.3V X5R 603

C1670
330UF-0.0045OHM 20% 2V POLY CASE-D2-SM

Memory (CPU VCCDDR) DECOUPLING

6x 22uF 0805, 5x 1uF 0402. INTEL RECOMMENDATION 9X 22uF 0805

28 13 11 6 29 =PP1V5_S0_CPU_MEM

C1676 C1677 C1678 C1679 C1680 C1681 C1682 C1683 C1684 C1685 C1686
22uF 20% 6.3V CERM X5R 805
1UF 10% 10V X5R 402

Note: VCCSA decoupling is on regulator page

PLL (CPU VCCSFR) DECOUPLING

2x 47uF, 1x 22uF 0805, 1x 10uF 0603, 1x 4.7uF 0603, 1x 2.2uF 0402, 2x 1uF 0402. INTEL RECOMMENDATION 10x 10uF 0805

13 6 =PP1V8_S0_CPU_PLL

C1693 C1694 C1692 C1691 C1695 C1690 C1696 C1697
1UF 10% 10V X5R 402
2.2UF 10% 6.3V X5R 402
4.7UF 10% 6.3V X5R CERM 603
10UF 20% 6.3V X5R 603
22uF 20% 6.3V CERM X5R 805
47UF 20% 6.3V X5R 0805

BULK CAPS ON VTT REG PAGE 78

SYNC MASTER=K62 AARON SYNC DATE=N/A

PAGE TITLE
CPU NON-GFX DECOUPLING

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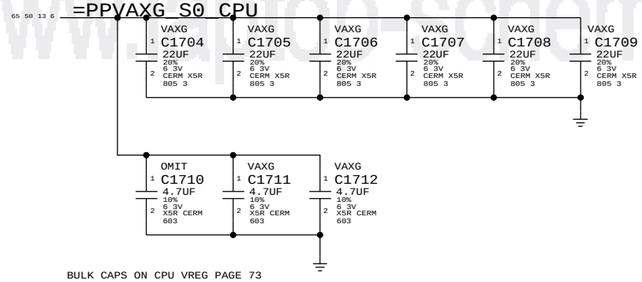
VAXG DECOUPLING

INTEL RECOMMENDATION 6X22UF 0805,3X 4.7UF

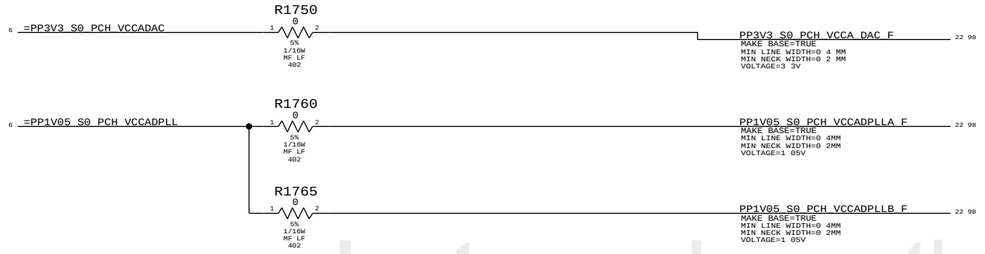
PLACEMENT_NOTE (C1704-C1709):

Place inside socket cavity



BULK CAPS ON CPU VREG PAGE 73

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
138S0586	1	CAP,4.7UF,10%,6.3V,0603	C1710	VAXG
113S0022	1	RES,0 OHM,5%,0603	C1710	NO_VAXG



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SYNC MASTER=K62 AARON SYNC DATE=11/30/2009

PAGE TITLE: GFX DECOUPLING & PCH PWR ALIAS

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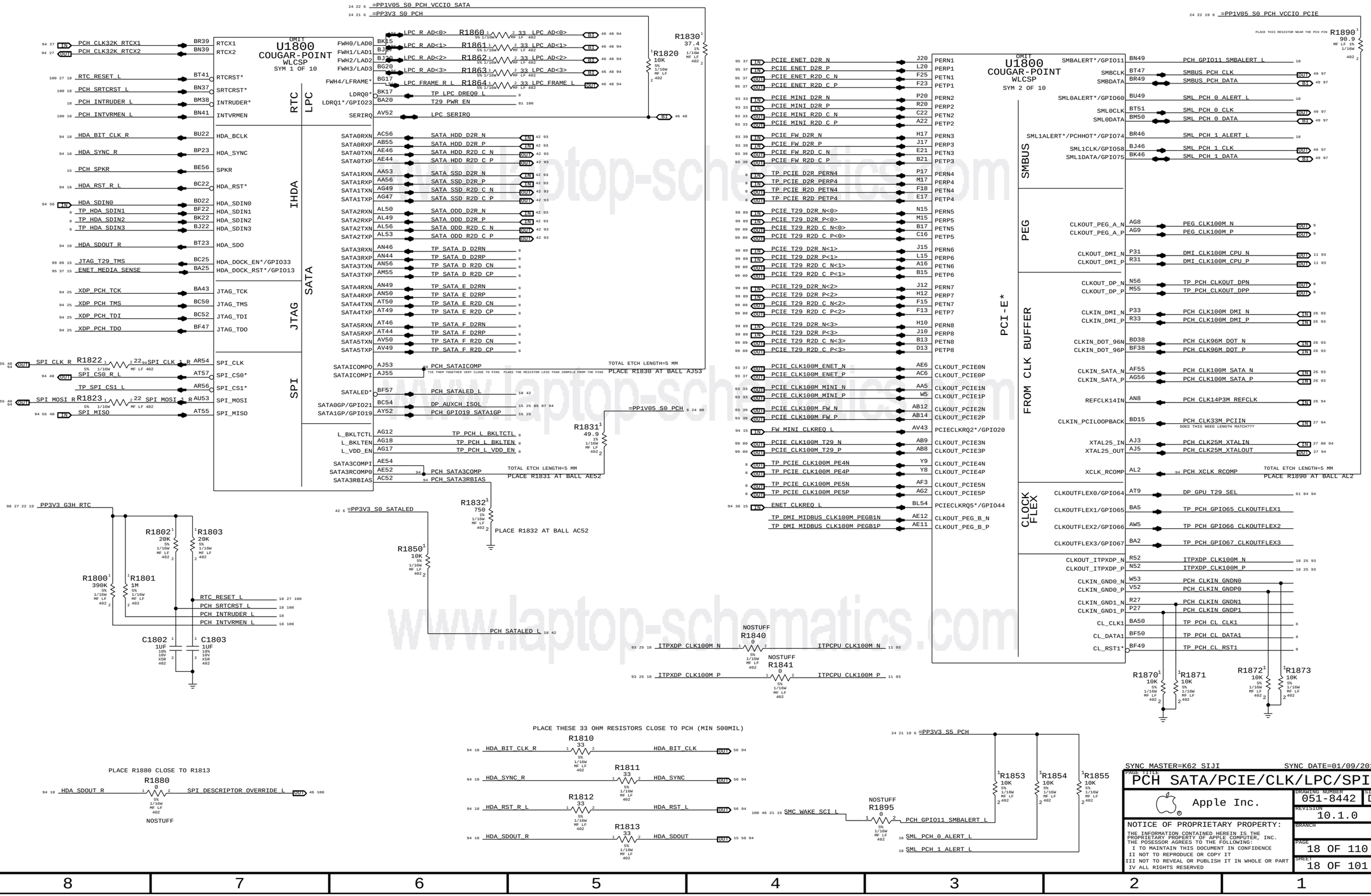
OMIT
U1800
COUGAR-POINT
WLCSP
SYM 1 OF 10
RTC
LPC
IHDA
SATA
JTAG
SPI
PCI-E*
SMBUS
PEG
FROM CLK BUFFER
CLOCK FLEX
OMIT
U1800
COUGAR-POINT
WLCSP
SYM 2 OF 10
=PP1V05_S0_PCH_VCCIO_SATA
=PP3V3_S0_PCH
=PP1V05_S0_PCH_VCCIO_PCIE
=PP3V3_S0_SATALED
PP3V3_G3H_RTC
=PP3V3_S5_PCH
PLACE R1831 AT BALL AE52
PLACE R1832 AT BALL AC52
PLACE R1830 AT BALL AJ53
PLACE R1890 AT BALL AL2
PLACE THESE 33 OHM RESISTORS CLOSE TO PCH (MIN 500MIL)
PLACE R1880 CLOSE TO R1813
NOSTUFF
SYNC_MASTER=K62_SIJI
SYNC_DATE=01/09/2011
PAGE TITLE
PCH SATA/PCIE/CLK/LPC/SPI
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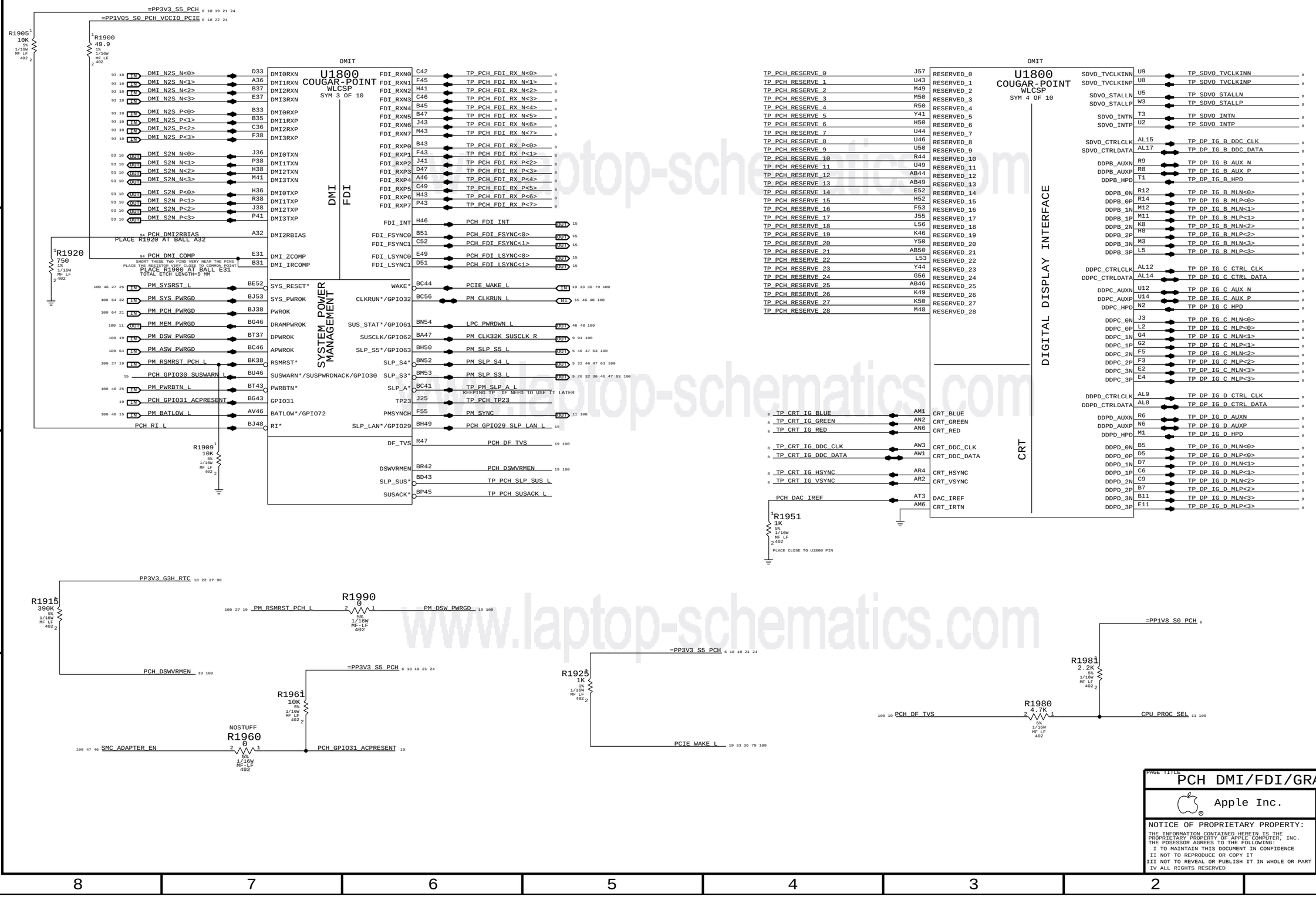

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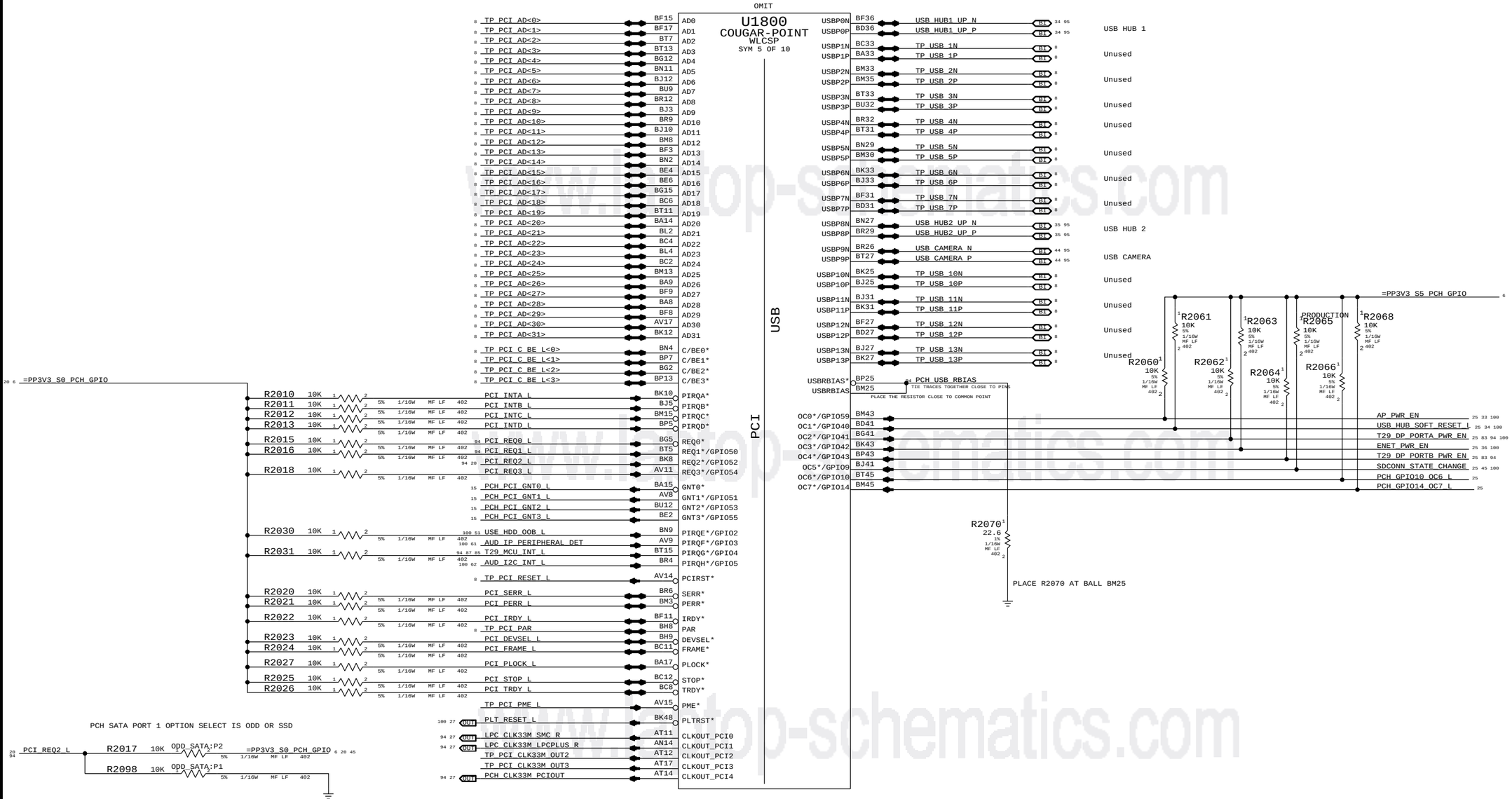

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PAGE TITLE
PCH PCI/FLASHCACHE/USB

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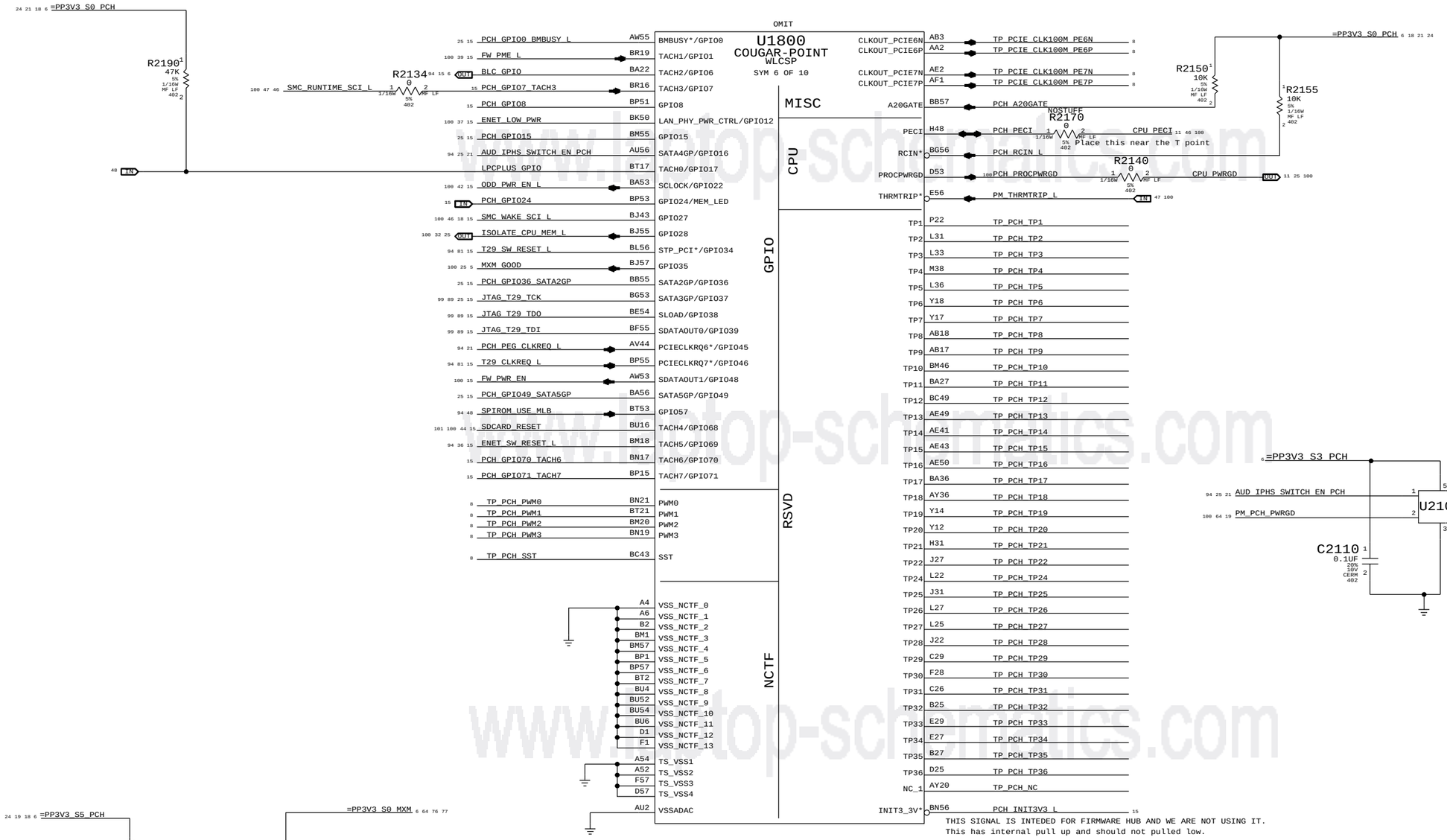

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SYNC MASTER=K62 SIJI SYNC DATE=01/09/2011

PAGE TITLE: PCH MISC

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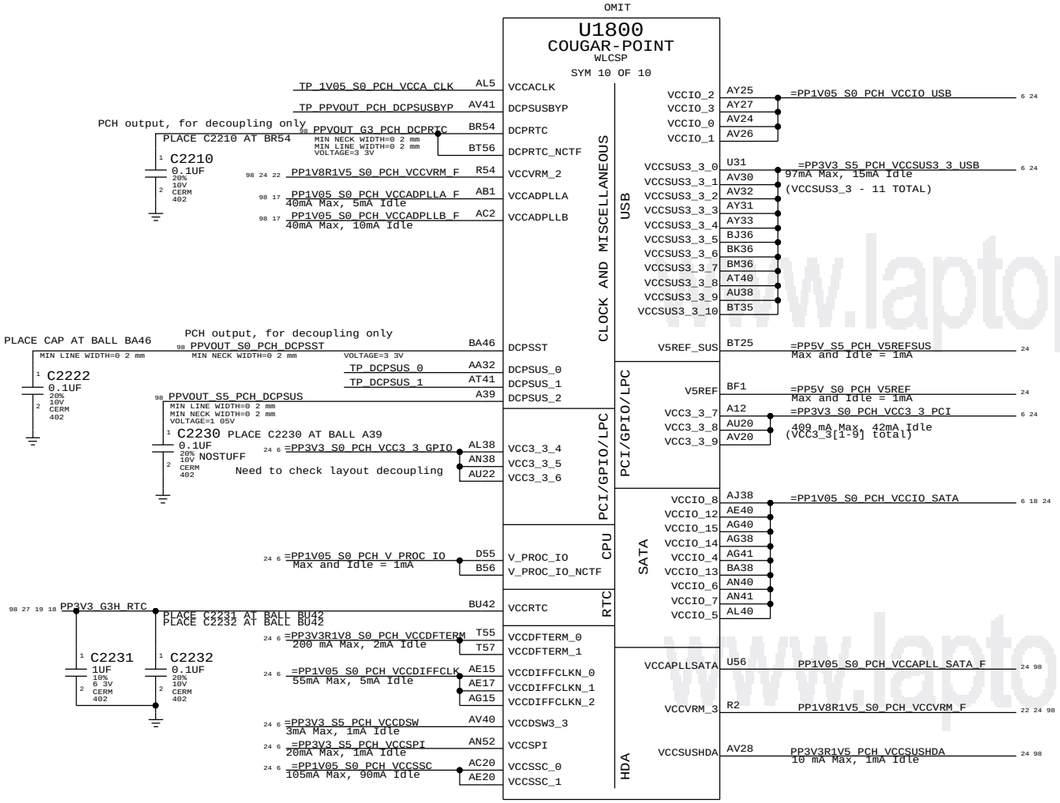

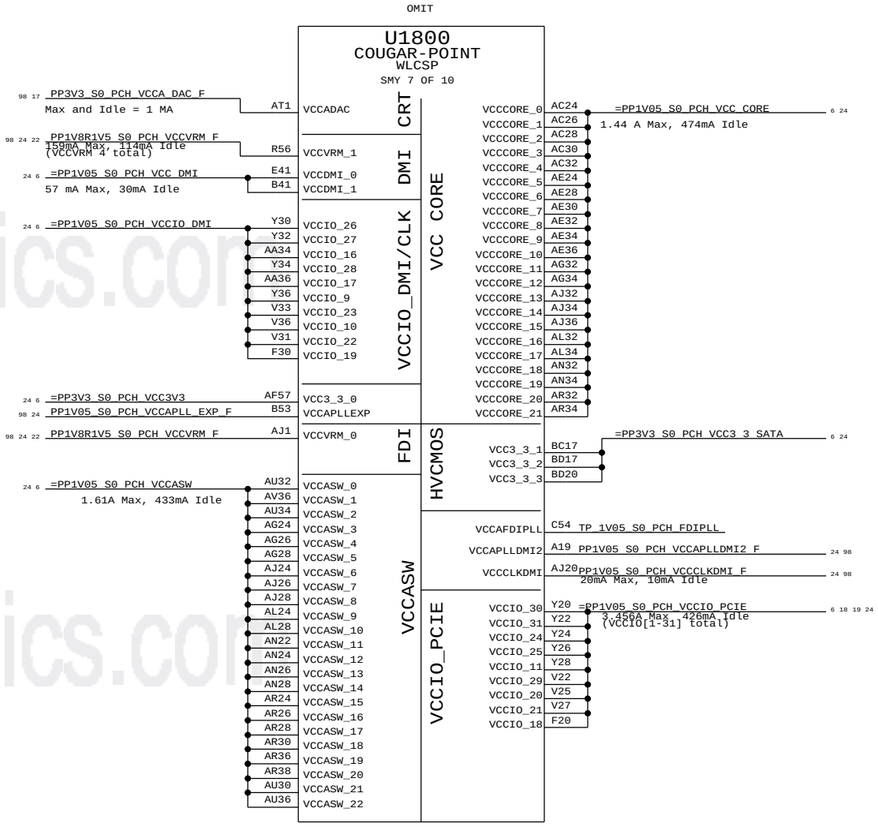

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PAGE TITLE
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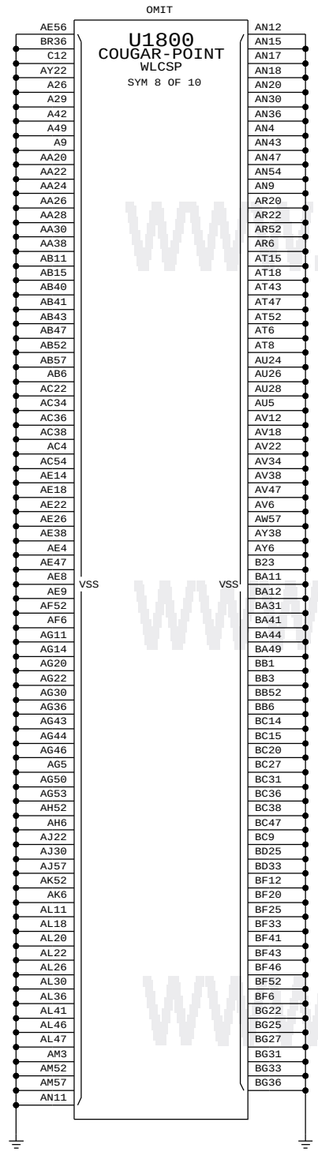

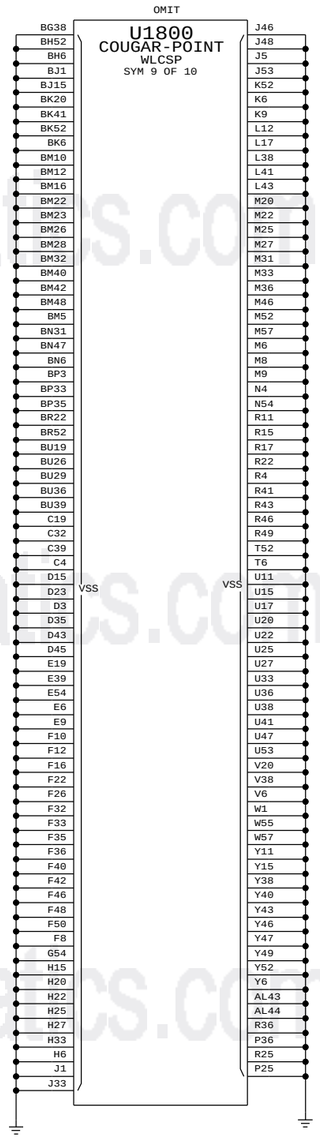

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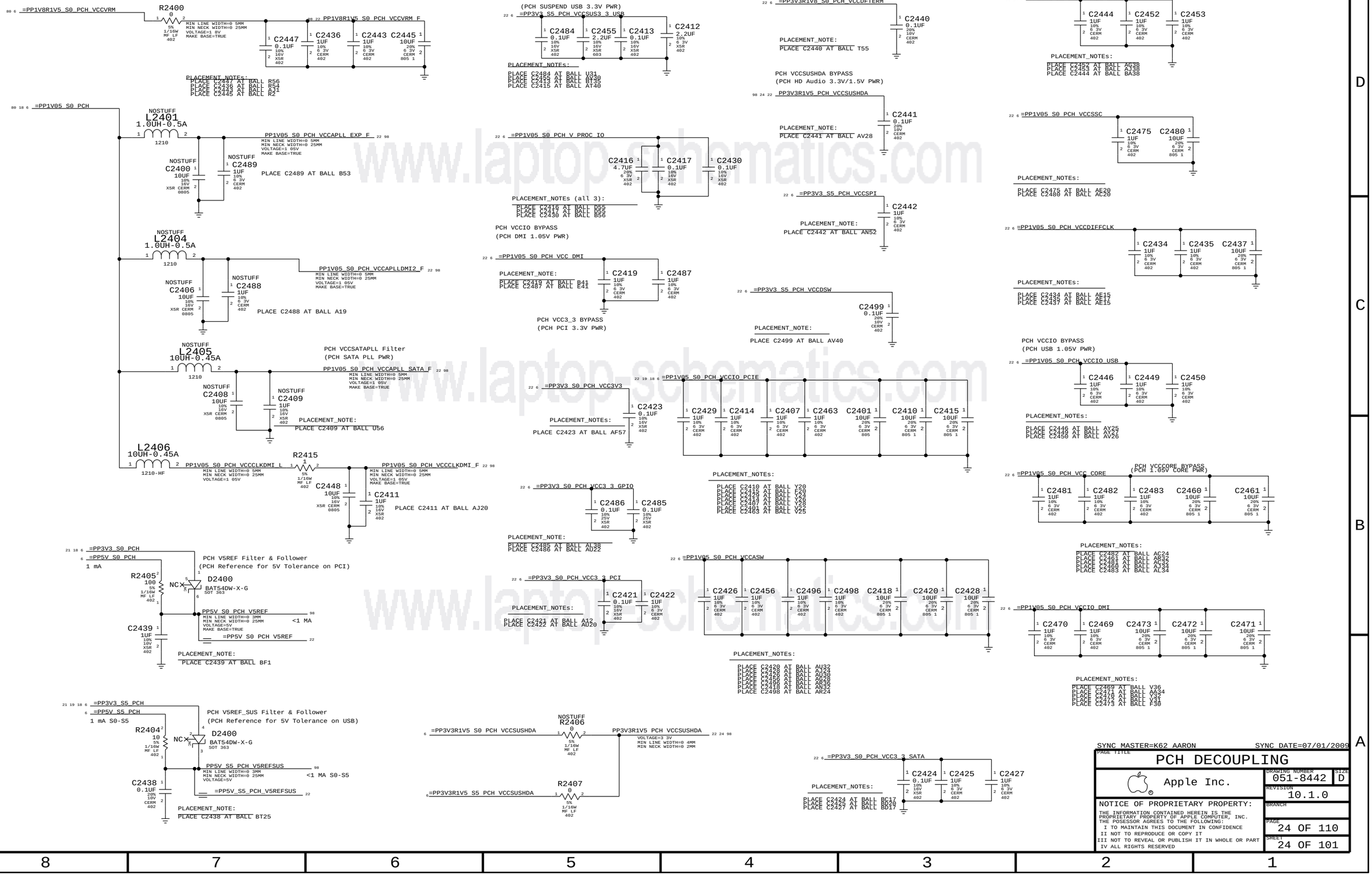

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PROCESSOR MINI XDP

PLACEMENT_NOTE=Place R2501 close to R2500 to minimize stubs

XDP_CPU_BPM
RP2500
XDP_BPM_L<4>
XDP_BPM_L<5>
XDP_BPM_L<6>
XDP_BPM_L<7>

XDP_CPU_CFG
RP2501
CPU_CFG<12>
CPU_CFG<13>
CPU_CFG<14>
CPU_CFG<15>

PLACEMENT NOTE=Place close to CPU
XDP R2500 1K MF LF 402 1/16W
CPU_PWRGD

PLACEMENT NOTE=Place close to SMC
XDP R2502 0 MF LF 402 1/16W
PM_PWRBTN_L

PLACEMENT NOTE=Place close to CPU
XDP R2501 1K MF LF 402 1/16W
CPU_CFG<0>

XDP R2504 0 MF LF 402 1/16W
PM_PGOOD_PVCORE_CPU

=PPVCCIO_S0_XDP

CRITICAL
XDP_CONN
J2500
DF40C-60DS-0.4V
F-ST-SM-HF
518S0774

XDP_CPU_PREQ_L
XDP_CPU_PRDY_L
XDP_BPM_L<0>
XDP_BPM_L<1>
XDP_BPM_L<2>
XDP_BPM_L<3>
CPU_CFG<10>
CPU_CFG<11>
XDP_OBSDATA_B<0>
XDP_OBSDATA_B<1>
XDP_OBSDATA_B<2>
XDP_OBSDATA_B<3>
XDP_CPU_PWRGD
XDP_CPU_PWRBTN_L
XDP_CPU_CFG<0>
XDP_VR_READY
=SMBUS_XDP_SDA
=SMBUS_XDP_SCL
XDP_CPU_TCK

OBSEN_A0 OBSEN_A1 OBSDATA_A0 OBSDATA_A1 OBSDATA_A2 OBSDATA_A3 OBSEN_B0 OBSEN_B1 OBSDATA_B0 OBSDATA_B1 OBSDATA_B2 OBSDATA_B3 PWRGD/HOOK0 HOOK1 VCC_OBS_AB HOOK2 HOOK3 SDA SCL TCK1 TCK0

OBSEN_C0 OBSEN_C1 OBSDATA_C0 OBSDATA_C1 OBSDATA_C2 OBSDATA_C3 OBSEN_D0 OBSEN_D1 OBSDATA_D0 OBSDATA_D1 OBSDATA_D2 OBSDATA_D3 ITPCLK/HOOK4 ITPCLK#/HOOK5 VCC_OBS_CD RESET#/HOOK6 DBR#/HOOK7 TDO TRSTn TDI TMS XDP_PRESENT#

CPU_CFG<16> CPU_CFG<17> OBSDATA_C0 CPU_CFG<0> OBSDATA_C1 CPU_CFG<1> OBSDATA_C2 CPU_CFG<2> OBSDATA_C3 CPU_CFG<3> OBSEN_D0 CPU_CFG<8> OBSEN_D1 CPU_CFG<9> OBSDATA_D0 CPU_CFG<4> OBSDATA_D1 CPU_CFG<5> OBSDATA_D2 CPU_CFG<6> OBSDATA_D3 CPU_CFG<7>

XDP_CPU_CLK100M_P
XDP_CPU_CLK100M_N
XDPCPU_PLTRST_L
XDP_DBRESET_L
XDP_CPU_TDO
XDP_CPU_TRST_L
XDP_CPU_TDI
XDP_CPU_TMS

XDP R2515 0 MF LF 402 1/16W ITPXDP_CLK100M_P
PLACEMENT NOTE=Place close to R1841
XDP R2516 0 MF LF 402 1/16W ITPXDP_CLK100M_N
PLACEMENT NOTE=Place close to R1840
<- 1K SERIES R ON PCH SUPPORT P. 28

XDP C2500 0.1uF 10% 16V X5R 402
XDP C2501 0.1uF 10% 16V X5R 402

DESIGN NOTE:
ODT AVAILABLE ON JTAG

PLACEMENT NOTE:
PLACE TDO TERM NEAR SNB XDP CONN
XDP R2510 51 XDP R2511 51 XDP R2512 51
PLACEMENT NOTE=Place close to CPU
PLACEMENT NOTE=Place close to J2500
XDP_CPU_TDO
XDP_CPU_TDI
XDP_CPU_TMS
XDP_CPU_TCK
XDP_CPU_TRST_L
XDP R2513 51 XDP R2514 51
PLACEMENT NOTE:
PLACE TCK/TDI/TMS/TRST* TERM NEAR CPU

PLACEMENT NOTE=Place close to SW2800
XDP R2506 0 5% 1/16W MF-LF 402
XDP_DBRESET_L
To Reset Button
PM_SYSRST_L

PCH MINI XDP

=PP3V3_S5_XDP

CRITICAL
XDP_CONN
J2550
DF40C-60DS-0.4V
F-ST-SM-HF
518S0774

TP_XDP_PCH_OBSFN_A<0>
TP_XDP_PCH_OBSFN_A<1>
XDP_PCH_AP_PWR_EN
XDP_PCH_USB_HUB_SOFT_RST_L
XDP_PCH_T29_DP_PORTA_PWR_EN
XDP_PCH_ENET_PWR_EN
TP_XDP_PCH_OBSFN_B<0>
TP_XDP_PCH_OBSFN_B<1>
XDP_PCH_T29_DP_PORTB_PWR_EN
XDP_PCH_SDCONN_CHANGE
PCH_GPIO10_OC6_L
PCH_GPIO14_OC7_L
XDP_PCH_S5_PWRGD
XDP_PCH_PWRBTN_L
XDP_XDPPCH_HOOK2
XDP_XDPPCH_HOOK3
=SMBUS_XDP_SDA
=SMBUS_XDP_SCL
XDP_PCH_TCK

OBSEN_A0 OBSEN_A1 OBSDATA_A0 OBSDATA_A1 OBSDATA_A2 OBSDATA_A3 OBSEN_B0 OBSEN_B1 OBSDATA_B0 OBSDATA_B1 OBSDATA_B2 OBSDATA_B3 PWRGD/HOOK0 HOOK1 VCC_OBS_AB HOOK2 HOOK3 SDA SCL TCK1 TCK0

OBSEN_C0 OBSEN_C1 OBSDATA_C0 OBSDATA_C1 OBSDATA_C2 OBSDATA_C3 OBSEN_D0 OBSEN_D1 OBSDATA_D0 OBSDATA_D1 OBSDATA_D2 OBSDATA_D3 ITPCLK/HOOK4 ITPCLK#/HOOK5 VCC_OBS_CD RESET#/HOOK6 DBR#/HOOK7 TDO TRSTn TDI TMS XDP_PRESENT#

XDP_PCH_GPIO15
PCH_GPIO9_BMBUSY_L
XDP_PCH_ISOLATE_CPU_MEM_L
XDP_PCH_MXM_GOOD
PCH_GPIO19_SATA1GP
TP_XDP_PCH_OBSFN_D<0>
TP_XDP_PCH_OBSFN_D<1>
PCH_GPIO36_SATA2GP
XDP_PCH_JTAG_T29_TCK
XDP_PCH_AUD_IPHS_SWITCH_EN
PCH_GPIO49_SATA5GP
TP_XDP_PCH_HOOK4
TP_XDP_PCH_HOOK5
XDPPCH_PLTRST_L
XDP_DBRESET_L
XDP_PCH_TDO
TP_XDP_PCH_TRST_L
XDP_PCH_TDI
XDP_PCH_TMS

XDP R2578 0 GPIO15 PCH_GPIO15
XDP R2576 0 MGPIO7/GPIO28 ISOLATE_CPU_MEM_L
XDP R2577 0 GPIO35 MXM_GOOD
XDP R2575 0 SATA0GP/GPIO21 DP_AUXCH_ISOL
XDP R2573 0 SATA3GP/GPIO37 JTAG_T29_TCK
XDP R2579 0 SATA4GP/GPIO16 AUD_IPHS_SWITCH_EN_PCH
PLACEMENT NOTE=Place close to PCH
<- 1K SERIES R ON PCH SUPPORT P. 28

XDP C2580 0.1uF 10% 16V X5R 402
XDP C2581 0.1uF 10% 16V X5R 402

=PP3V3_S5_XDP

PLACEMENT NOTE:
PLACE TDO TERM NEAR PCH XDP CONN
XDP R2550 200 XDP R2551 200 XDP R2552 200
PLACEMENT NOTE=Place close to PCH
PLACEMENT NOTE=Place close to J2550
XDP_PCH_TDO
XDP_PCH_TDI
XDP_PCH_TMS
XDP_PCH_TCK
XDP R2553 100 XDP R2554 100 XDP R2555 100 XDP R2556 51
This is to derive 1.05V SUS RAIL
PLACEMENT NOTE:
PLACE TCK/TDI/TMS/TRST* TERM NEAR PCH

SYNC_MASTER=K62_SIJI SYNC_DATE=01/09/2011

PAGE TITLE	CPU & PCH XDP
	Apple Inc.
DRAWING NUMBER	051-8442
SIZE	D
REVISION	10.1.0
BRANCH	
PAGE	25 OF 110
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R2605 OR R2606 CAN BE CHANGED TO "BUF_CLK" OPTION LATER
WHEN FCIM IS FULLY VALIDATED ->

STUFF THIS TO POWER DOWN CK505 ->

UNUSED clock terminations for FCIM MODE

PLACE R2699 NEAR PIN 26

PCH BCLK 133MHZ

PCH DMI/PCIe 100MHz

PCH SATA 100MHZ

PCH USB Clock 96MHz

SYNC MASTER=K62 ROSITA SYNC DATE=01/09/2011

PAGE TITLE: CLOCK (CK505)

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

REVISION: 10.1.0

BRANCH:

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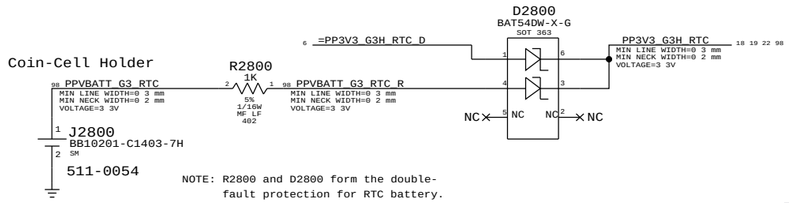
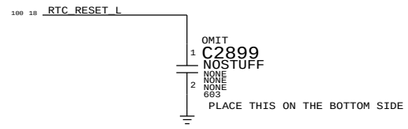
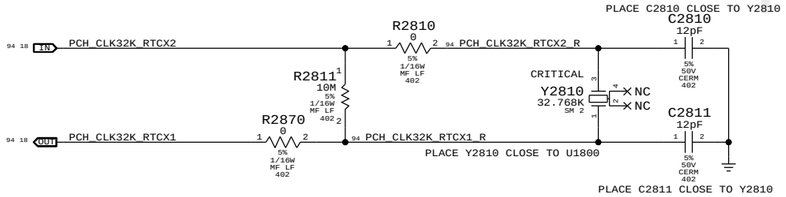
RTC Power Sources

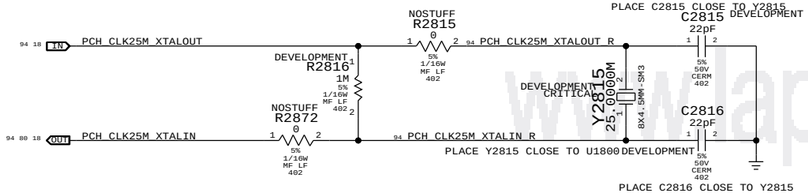




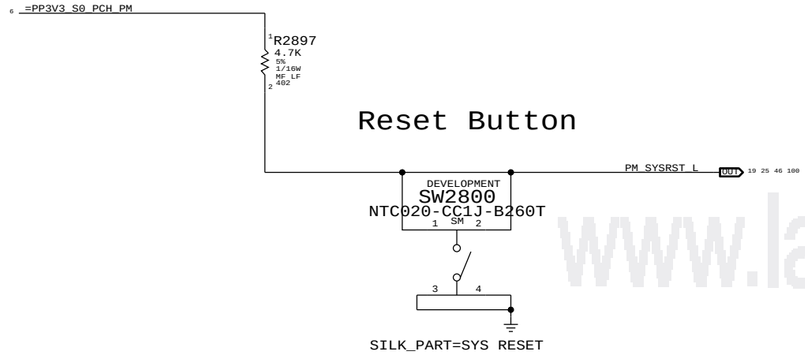
PCH RTC Crystal

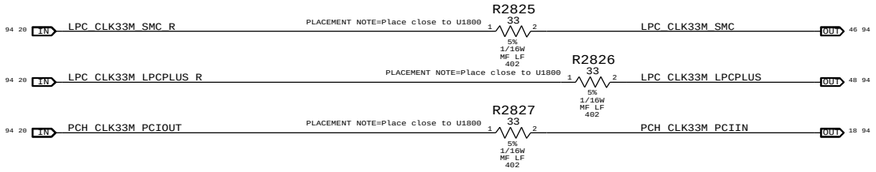


PCH 25MHZ CRYSTAL

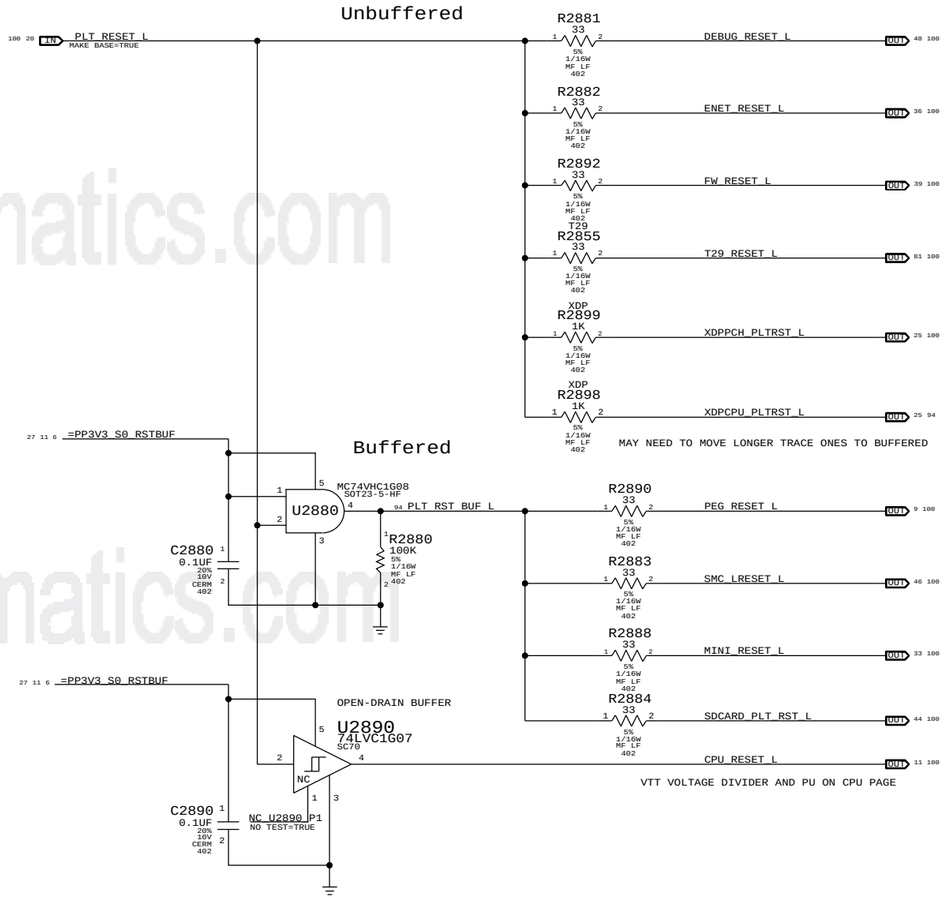


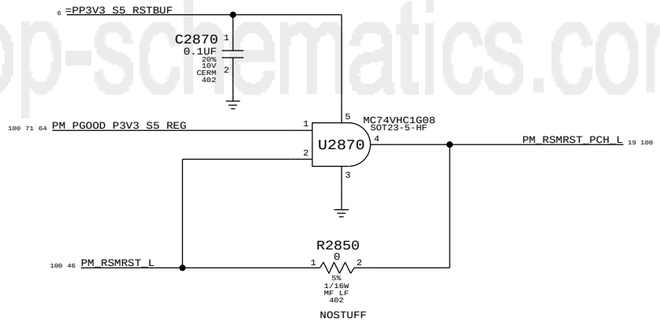
Reset Button





Platform Reset Connections





SMC PROVIDES RSMRST_L DE-ASSERTION DELAY UPON ENTRY TO S5
SMC PROVIDES RSMRST_L ASSERTION TIMING REQUIREMENTS UPON EXPECTED EXIT FROM S5
SMC MAY FORCE A RSMRST_L ASSERTION WITHOUT AN S5 POWER TRANSITION IN SOME ERROR CASES
PGOOD PROVIDES RSMRST_L ASSERTION TIMING REQUIREMENTS UPON AN UN-EXPECTED EXIT FROM S5 (POWER LOSS)

SYNC_MASTER=K62_SIJI SYNC_DATE=01/09/2011

PAGE_TITLE: CHIPSET SUPPORT

Apple Inc.

DRAWING_NUMBER: 051-8442 SIZE: D
REVISION: 10.1.0
BRANCH:
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DIMM VREFDQ

=PP1V5_S3_MEM_A
=PP3V3_S3_VREFMRGN
=I2C_VREFMRGN_A_SCL
=I2C_VREFMRGN_A_SDA
I2C_VREFMRGN_DIMMA_SCL
I2C_VREFMRGN_DIMMA_SDA
R2900 0 5% 1/16W MF-LF 402
R2901 0 5% 1/16W MF-LF 402
C2900 0.1UF 10% 16V X5R 402
U2900 ISL90727WIE627ZTK SC-70 353S2369
VREFMRGN_A
VDD SCL SDA GND RH RW
R2902 12.1K 1% 1/16W MF-LF 402
R2903 12.1K 1% 1/16W MF-LF 402
I2C ADDR = 0X5C (WRITE)
I2C ADDR = 0X5D (READ)
=PP5V_S3_VREFMRGN
R2909 10 1% 1/16W MF-LF 402
PP5V_S3_VREFMRGN_A
C2901 0.1UF 10% 16V X5R 402
U2901 LM321 SOT23-5 353S1961
VREFMARGIN_DIMMA_DACOUT
VREFMARGIN_DIMMA_OPFB
R2904 2.2 5% 1/16W MF-LF 402
R2905 1K 1% 1/16W MF-LF 402
C2902 1UF 10% 6.3V CERM 402
VREFMARGIN_DIMMA_DQ

PLACEMENT NOTE:
PLACE R2970, R2971 and C2950 close to DIMM PIN

=PP1V5_S3_MEM_A
R2970 1K 1% 1/16W MF-LF 402
R2958 0 5% 1/16W MF-LF 402
R2971 1K 1% 1/16W MF-LF 402
C2950 NOSTUFF 0.1UF 10% 16V X5R 402
PP0V75_S3_MEM_VREFDQ_A

=PP1V5_S3_MEM_B
=PP3V3_S3_VREFMRGN
=I2C_VREFMRGN_B_SCL
=I2C_VREFMRGN_B_SDA
I2C_VREFMRGN_DIMMB_SCL
I2C_VREFMRGN_DIMMB_SDA
R2910 0 5% 1/16W MF-LF 402
R2911 0 5% 1/16W MF-LF 402
C2910 0.1UF 10% 16V X5R 402
U2910 ISL90728WIE627ZTK SC-70 353S2370
VREFMRGN_B
VDD SCL SDA GND RH RW
R2912 12.1K 1% 1/16W MF-LF 402
R2913 12.1K 1% 1/16W MF-LF 402
I2C ADDR = 0X7C (WRITE)
I2C ADDR = 0X7D (READ)
=PP5V_S3_VREFMRGN
R2919 10 1% 1/16W MF-LF 402
PP5V_S3_VREFMRGN_B
C2911 0.1UF 10% 16V X5R 402
U2911 LM321 SOT23-5 353S1961
VREFMARGIN_DIMMB_DACOUT
VREFMARGIN_DIMMB_OPFB
R2914 2.2 5% 1/16W MF-LF 402
R2915 1K 1% 1/16W MF-LF 402
C2912 1UF 10% 6.3V CERM 402
VREFMARGIN_DIMMB_DQ

PLACEMENT NOTE:
PLACE R2975, R2976 and C2951 close to DIMM PIN

=PP1V5_S3_MEM_B
R2975 1K 1% 1/16W MF-LF 402
R2956 0 5% 1/16W MF-LF 402
R2976 1K 1% 1/16W MF-LF 402
C2951 NOSTUFF 0.1UF 10% 16V X5R 402
PP0V75_S3_MEM_VREFDQ_B
PLACE IT CLOSE TO DIMM CONNECTOR PIN

R2956 change to NOSTUFF if use VREFMARGIN_DIMMB_DQ to drive both VREFCA_A and VREFCA_B

DIMM VREFCA

=PP1V5_S3_MEM_A
R2988 1K 1% 1/16W MF-LF 402
R2995 NOSTUFF 0 5% 1/16W MF-LF 402
R2989 1K 1% 1/16W MF-LF 402
C2921 NOSTUFF 0.1UF 10% 16V X5R 402
VREFMARGIN_DIMMB_DQ
PP0V75_S3_MEM_VREFCA_A

PLACEMENT NOTE:
PLACE R2988, R2989 and C2921 close to DIMM PIN

=PP1V5_S3_MEM_B
R2978 1K 1% 1/16W MF-LF 402
R2996 NOSTUFF 0 5% 1/16W MF-LF 402
R2979 1K 1% 1/16W MF-LF 402
C2991 NOSTUFF 0.1UF 10% 16V X5R 402
VREFMARGIN_DIMMB_DQ
PP0V75_S3_MEM_VREFCA_B

PLACEMENT NOTE:
PLACE R2978, R2979 and C2991 close to DIMM PIN

CPU VREF

PLACEMENT NOTE:
PLACE R2968, R2969 and C2961 near CPU

=PP1V5_S0_CPU_MEM
R2968 100 1% 1/16W MF-LF 402
R2969 100 1% 1/16W MF-LF 402
C2961 0.1UF 10% 16V X5R 402
CPU_DDR_VREF

R2960 NOSTUFF 0 5% 1/16W MF-LF 402
PP0V75_S3_MEM_VREFDQ_A
PP0V75_S3_MEM_VREFDQ_B

EMPTY ONE SET OF OP-AMP & POT WHEN R2960 IS STUFF

SYNC_MASTER=K62_ROSITA
SYNC_DATE=01/09/2013
PAGE TITLE: DDR3 VREF MARGINING
Apple Inc.
DRAWING NUMBER: 051-8442
SIZE: D
REVISION: 10.1.0
BRANCH:
PAGE: 29 OF 110
SHEET: 28 OF 101

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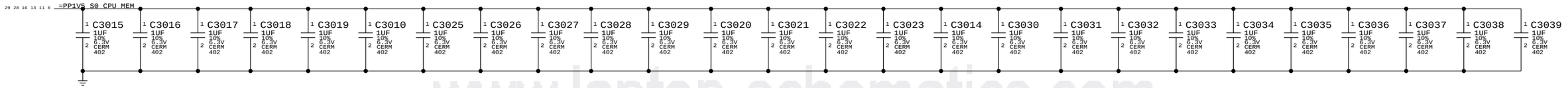
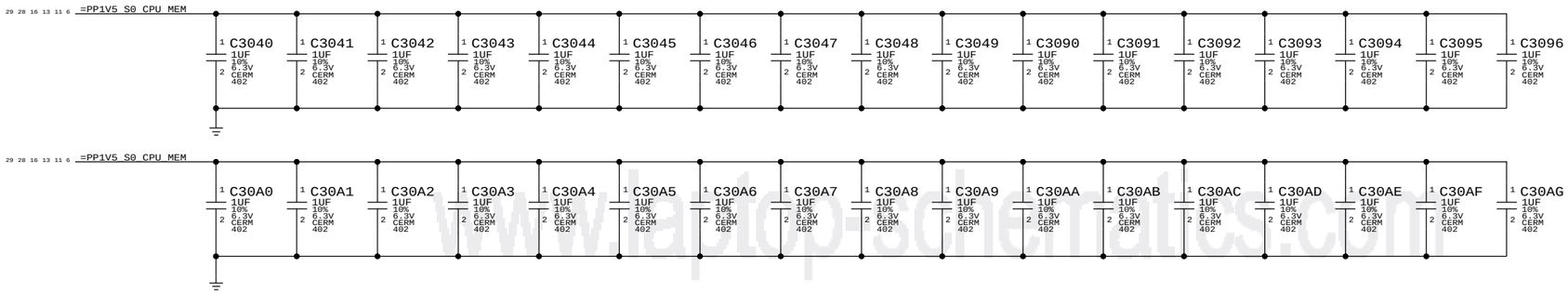
DIMM A (CLOSER TO CPU)

CAPS TO STITCH 1V5_CPU_MEM TO GND NEAR DIMM

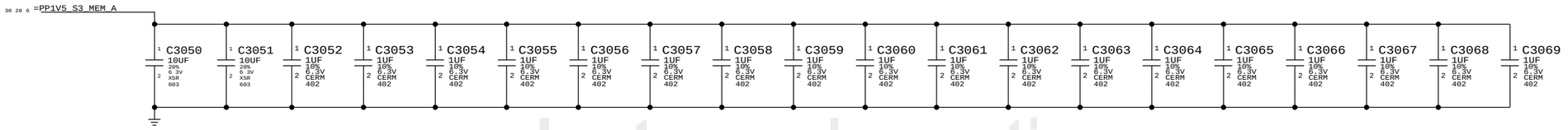
DIMM B (FURTHER FROM CPU)



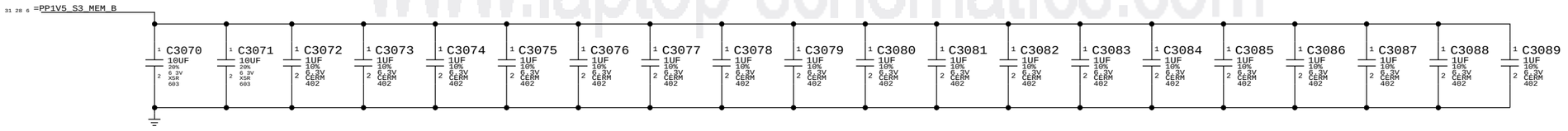
EXTRA DECOUPLING CAPS FOR 1V5_CPU_MEM RAIL



DECOUPLING CAPS FOR 1V5_S3_MEM AT CHANNEL A DIMM CONNECTOR



DECOUPLING CAPS FOR 1V5_S3_MEM AT CHANNEL B DIMM CONNECTOR



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SYNC MASTER=K62 ROSITA SYNC DATE=01/09/2011

PAGE TITLE: MEMORY CAPS

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

REVISION: 10.1.0

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DIMM 2

CRITICAL
J3100
F-RT-TH
(1 OF 2)
DDR3-SODIMM-DUAL

98 30 28 PP0V75_S3_MEM_VREFDQ_A	1A	VREFDQ	VSS_0	2A			
	3A	VSS_1	DQ4	4A	=MEM_A_DQ<4>	30 32	
32 30 =MEM_A_DQ<0>	5A	DQ0	DQ5	6A	=MEM_A_DQ<5>	30 32	
32 30 =MEM_A_DQ<1>	7A	DQ1	VSS_2	8A			
	9A	VSS_3	DQS0*	10A	=MEM_A_DQS_N<0>	30 32	
	11A	DM0	DQS0	12A	=MEM_A_DQS_P<0>	30 32	
	13A	VSS_4	VSS_5	14A			
32 30 =MEM_A_DQ<2>	15A	DQ2	DQ6	16A	=MEM_A_DQ<6>	30 32	
32 30 =MEM_A_DQ<3>	17A	DQ3	DQ7	18A	=MEM_A_DQ<7>	30 32	
	19A	VSS_6	VSS_7	20A			
32 30 =MEM_A_DQ<8>	21A	DQ8	DQ12	22A	=MEM_A_DQ<12>	30 32	
32 30 =MEM_A_DQ<9>	23A	DQ9	DQ13	24A	=MEM_A_DQ<13>	30 32	
	25A	VSS_8	VSS_9	26A			
32 30 =MEM_A_DQS_N<1>	27A	DQS1*	DM1	28A			
32 30 =MEM_A_DQS_P<1>	29A	DQS1	RESET*	30A	MEM_RESET_L	30 31 32 92 100	
	31A	VSS_10	VSS_11	32A			
32 30 =MEM_A_DQ<10>	33A	DQ10	DQ14	34A	=MEM_A_DQ<14>	30 32	
32 30 =MEM_A_DQ<11>	35A	DQ11	DQ15	36A	=MEM_A_DQ<15>	30 32	
	37A	VSS_12	VSS_13	38A			
32 30 =MEM_A_DQ<16>	39A	DQ16	DQ20	40A	=MEM_A_DQ<20>	30 32	
32 30 =MEM_A_DQ<17>	41A	DQ17	DQ21	42A	=MEM_A_DQ<21>	30 32	
	43A	VSS_14	VSS_15	44A			
32 30 =MEM_A_DQS_N<2>	45A	DQS2*	DM2	46A			
32 30 =MEM_A_DQS_P<2>	47A	DQS2	VSS_16	48A			
	49A	VSS_17	DQ22	50A	=MEM_A_DQ<22>	30 32	
32 30 =MEM_A_DQ<18>	51A	DQ18	DQ23	52A	=MEM_A_DQ<23>	30 32	
32 30 =MEM_A_DQ<19>	53A	DQ19	VSS_18	54A			
	55A	VSS_19	DQ28	56A	=MEM_A_DQ<28>	30 32	
32 30 =MEM_A_DQ<24>	57A	DQ24	DQ29	58A	=MEM_A_DQ<29>	30 32	
32 30 =MEM_A_DQ<25>	59A	DQ25	VSS_20	60A			
	61A	VSS_21	DQS3*	62A	=MEM_A_DQS_N<3>	30 32	
	63A	DM3	DQS3	64A	=MEM_A_DQS_P<3>	30 32	
	65A	VSS_22	VSS_23	66A			
32 30 =MEM_A_DQ<26>	67A	DQ26	DQ30	68A	=MEM_A_DQ<30>	30 32	
32 30 =MEM_A_DQ<27>	69A	DQ27	DQ31	70A	=MEM_A_DQ<31>	30 32	
	71A	VSS_24	VSS_25	72A			
92 12 MEM_A_CKE<2>	73A	CKE0	CKE1	74A	MEM_A_CKE<3>	12 92	
30 29 28 6 =PP1V5_S3_MEM_A	75A	VDD_0	VDD_1	76A	=PP1V5_S3_MEM_A	6 28 29 30	
	77A	NC_0	A15	78A	MEM_A_A<15>	12 30 92	
92 30 12 MEM_A_BA<2>	79A	BA2	A14	80A	MEM_A_A<14>	12 30 92	
	81A	VDD_2	VDD_3	82A			
92 30 12 MEM_A_A<12>	83A	A12/BC*	A11	84A	MEM_A_A<11>	12 30 92	
92 30 12 MEM_A_A<9>	85A	A9	A7	86A	MEM_A_A<7>	12 30 92	
	87A	VDD_4	VDD_5	88A			
92 30 12 MEM_A_A<8>	89A	A8	A6	90A	MEM_A_A<6>	12 30 92	
92 30 12 MEM_A_A<5>	91A	A5	A4	92A	MEM_A_A<4>	12 30 92	
	93A	VDD_6	VDD_7	94A			
92 30 12 MEM_A_A<3>	95A	A3	A2	96A	MEM_A_A<2>	12 30 92	
92 30 12 MEM_A_A<1>	97A	A1	A0	98A	MEM_A_A<0>	12 30 92	
	99A	VDD_8	VDD_9	100A			
32 =MEM_A_CLK_P<2>	101A	CK0	CK1	102A	=MEM_A_CLK_P<3>	32	
32 =MEM_A_CLK_N<2>	103A	CK0*	CK1*	104A	=MEM_A_CLK_N<3>	32	
	105A	VDD_10	VDD_11	106A			
92 30 12 MEM_A_A<10>	107A	A10_AP	BA1	108A	MEM_A_BA<1>	12 30 92	
92 30 12 MEM_A_BA<0>	109A	BA0	RAS*	110A	MEM_A_RAS_L	12 30 92	
	111A	VDD_12	VDD_13	112A			
92 30 12 MEM_A_WE_L	113A	WE*	S0*	114A	MEM_A_CS_L<2>	12 92	
92 30 12 MEM_A_CAS_L	115A	CAS*	ODT0	116A	MEM_A_ODT<2>	12 92	
	117A	VDD_14	VDD_15	118A			
92 30 12 MEM_A_A<13>	119A	A13	ODT1	120A	MEM_A_ODT<3>	12 92	
92 12 MEM_A_CS_L<3>	121A	S1*	NC_1	122A			
	123A	VDD_16	VDD_17	124A			
	125A	TEST	VREFCA	126A	PP0V75_S3_MEM_VREFCA_A	28 30 98	
	127A	VSS_26	VSS_27	128A			
32 30 =MEM_A_DQ<32>	129A	DQ32	DQ36	130A	=MEM_A_DQ<36>	30 32	
32 30 =MEM_A_DQ<33>	131A	DQ33	DQ37	132A	=MEM_A_DQ<37>	30 32	
	133A	VSS_28	VSS_29	134A			
32 30 =MEM_A_DQS_N<4>	135A	DQS4*	DM4	136A			
32 30 =MEM_A_DQS_P<4>	137A	DQS4	VSS_30	138A			
	139A	VSS_31	DQ38	140A	=MEM_A_DQ<38>	30 32	
32 30 =MEM_A_DQ<34>	141A	DQ34	DQ39	142A	=MEM_A_DQ<39>	30 32	
32 30 =MEM_A_DQ<35>	143A	DQ35	VSS_32	144A			
	145A	VSS_33	DQ44	146A	=MEM_A_DQ<44>	30 32	
32 30 =MEM_A_DQ<40>	147A	DQ40	DQ45	148A	=MEM_A_DQ<45>	30 32	
32 30 =MEM_A_DQ<41>	149A	DQ41	VSS_34	150A			
	151A	VSS_35	DQS5*	152A	=MEM_A_DQS_N<5>	30 32	
	153A	DM5	DQS5	154A	=MEM_A_DQS_P<5>	30 32	
	155A	VSS_36	VSS_37	156A			
32 30 =MEM_A_DQ<42>	157A	DQ42	DQ46	158A	=MEM_A_DQ<46>	30 32	
32 30 =MEM_A_DQ<43>	159A	DQ43	DQ47	160A	=MEM_A_DQ<47>	30 32	
	161A	VSS_38	VSS_39	162A			
32 30 =MEM_A_DQ<48>	163A	DQ48	DQ52	164A	=MEM_A_DQ<52>	30 32	
32 30 =MEM_A_DQ<49>	165A	DQ49	DQ53	166A	=MEM_A_DQ<53>	30 32	
	167A	VSS_40	VSS_41	168A			
32 30 =MEM_A_DQS_N<6>	169A	DQS6*	DM6	170A			
32 30 =MEM_A_DQS_P<6>	171A	DQS6	VSS_42	172A			
	173A	VSS_43	DQ54	174A	=MEM_A_DQ<54>	30 32	
32 30 =MEM_A_DQ<50>	175A	DQ50	DQ55	176A	=MEM_A_DQ<55>	30 32	
32 30 =MEM_A_DQ<51>	177A	DQ51	VSS_44	178A			
	179A	VSS_45	DQ60	180A	=MEM_A_DQ<60>	30 32	
32 30 =MEM_A_DQ<56>	181A	DQ56	DQ61	182A	=MEM_A_DQ<61>	30 32	
32 30 =MEM_A_DQ<57>	183A	DQ57	VSS_46	184A			
	185A	VSS_47	DQS7*	186A	=MEM_A_DQS_N<7>	30 32	
	187A	DM7	DQS7	188A	=MEM_A_DQS_P<7>	30 32	
	189A	VSS_48	VSS_49	190A			
32 30 =MEM_A_DQ<58>	191A	DQ58	DQ62	192A	=MEM_A_DQ<62>	30 32	
32 30 =MEM_A_DQ<59>	193A	DQ59	DQ63	194A	=MEM_A_DQ<63>	30 32	
	195A	VSS_50	VSS_51	196A			
30 MEM_DIMM2_SA<0>	197A	SA0	EVENT*	198A	MEM_EVENT_L	30 31 47	
47 30 6 =PPSPD_S0_MEM_A	199A	VDDSPD	SDA	200A	=I2C_SODIMMA_SDA	30 49	
30 MEM_DIMM2_SA<1>	201A	SA1	SCL	202A	=I2C_SODIMMA_SCL	30 49	
30 6 =PP0V75_S0_MEM_VTT_A	203A	VTT_0	VTT_1	204A	=PP0V75_S0_MEM_VTT_A	6 30	
	409	MTG PIN	MTG PIN	410			

DIMM 0

CRITICAL
J3100
F-RT-TH
(2 OF 2)
DDR3-SODIMM-DUAL

98 30 28 PP0V75_S3_MEM_VREFDQ_A	1B	VREFDQ	VSS_0	2B			
	3B	VSS_1	DQ4	4B	=MEM_A_DQ<4>	30 32	
32 30 =MEM_A_DQ<0>	5B	DQ0	DQ5	6B	=MEM_A_DQ<5>	30 32	
32 30 =MEM_A_DQ<1>	7B	DQ1	VSS_2	8B			
	9B	VSS_3	DQS0*	10B	=MEM_A_DQS_N<0>	30 32	
	11B	DM0	DQS0	12B	=MEM_A_DQS_P<0>	30 32	
	13B	VSS_4	VSS_5	14B			
32 30 =MEM_A_DQ<2>	15B	DQ2	DQ6	16B	=MEM_A_DQ<6>	30 32	
32 30 =MEM_A_DQ<3>	17B	DQ3	DQ7	18B	=MEM_A_DQ<7>	30 32	
	19B	VSS_6	VSS_7	20B			
32 30 =MEM_A_DQ<8>	21B	DQ8	DQ12	22B	=MEM_A_DQ<12>	30 32	
32 30 =MEM_A_DQ<9>	23B	DQ9	DQ13	24B	=MEM_A_DQ<13>	30 32	
	25B	VSS_8	VSS_9	26B			
32 30 =MEM_A_DQS_N<1>	27B	DQS1*	DM1	28B			
32 30 =MEM_A_DQS_P<1>	29B	DQS1	RESET*	30B	MEM_RESET_L	30 31 32 92 100	
	31B	VSS_10	VSS_11	32B			
32 30 =MEM_A_DQ<10>	33B	DQ10	DQ14	34B	=MEM_A_DQ<14>	30 32	
32 30 =MEM_A_DQ<11>	35B	DQ11	DQ15	36B	=MEM_A_DQ<15>	30 32	
	37B	VSS_12	VSS_13	38B			
32 30 =MEM_A_DQ<16>	39B	DQ16	DQ20	40B	=MEM_A_DQ<20>	30 32	
32 30 =MEM_A_DQ<17>	41B	DQ17	DQ21	42B	=MEM_A_DQ<21>	30 32	
	43B	VSS_14	VSS_15	44B			
32 30 =MEM_A_DQS_N<2>	45B	DQS2*	DM2	46B			
32 30 =MEM_A_DQS_P<2>	47B	DQS2	VSS_16	48B			
	49B	VSS_17	DQ22	50B	=MEM_A_DQ<22>	30 32	
32 30 =MEM_A_DQ<18>	51B	DQ18	DQ23	52B	=MEM_A_DQ<23>	30 32	
32 30 =MEM_A_DQ<19>	53B	DQ19	VSS_18	54B			
	55B	VSS_19	DQ28	56B	=MEM_A_DQ<28>	30 32	
32 30 =MEM_A_DQ<24>	57B	DQ24	DQ29	58B	=MEM_A_DQ<29>	30 32	
32 30 =MEM_A_DQ<25>	59B	DQ25	VSS_20	60B			
	61B	VSS_21	DQS3*	62B	=MEM_A_DQS_N<3>	30 32	
	63B	DM3	DQS3	64B	=MEM_A_DQS_P<3>	30 32	
	65B	VSS_22	VSS_23	66B			
32 30 =MEM_A_DQ<26>	67B	DQ26	DQ30	68B	=MEM_A_DQ<30>	30 32	
32 30 =MEM_A_DQ<27>	69B	DQ27	DQ31	70B	=MEM_A_DQ<31>	30 32	
	71B	VSS_24	VSS_25	72B			
92 12 MEM_A_CKE<0>	73B	CKE0	CKE1	74B	MEM_A_CKE<1>	12 92	
30 29 28 6 =PP1V5_S3_MEM_A	75B	VDD_0	VDD_1	76B	=PP1V5_S3_MEM_A	6 28 29 30	
	77B	NC_0	A15	78B	MEM_A_A<15>	12 30 92	
92 30 12 MEM_A_BA<2>	79B	BA2	A14	80B	MEM_A_A<14>	12 30 92	
	81B	VDD_2	VDD_3	82B			
92 30 12 MEM_A_A<12>	83B	A12/BC*	A11	84B	MEM_A_A<11>	12 30 92	
92 30 12 MEM_A_A<9>	85B	A9	A7	86B	MEM_A_A<7>	12 30 92	
	87B	VDD_4	VDD_5	88B			
92 30 12 MEM_A_A<8>	89B	A8	A6	90B	MEM_A_A<6>	12 30 92	
92 30 12 MEM_A_A<5>	91B	A5	A4	92B	MEM_A_A<4>	12 30 92	
	93B	VDD_6	VDD_7	94B			
92 30 12 MEM_A_A<3>	95B	A3	A2	96B	MEM_A_A<2>	12 30 92	
92 30 12 MEM_A_A<1>	97B	A1	A0	98B	MEM_A_A<0>	12 30 92	
	99B	VDD_8	VDD_9	100B			
32 =MEM_A_CLK_P<0>	101B	CK0	CK1	102B	=MEM_A_CLK_P<1>	32	
32 =MEM_A_CLK_N<0>	103B	CK0*	CK1*	104B	=MEM_A_CLK_N<1>	32	
	105B	VDD_10	VDD_11	106B			
92 30 12 MEM_A_A<10>	107B	A10_AP	BA1	108B	MEM_A_BA<1>	12 30 92	
92 30 12 MEM_A_BA<0>	109B	BA0	RAS*	110B	MEM_A_RAS_L	12 30 92	
	111B	VDD_12	VDD_13	112B			
92 30 12 MEM_A_WE_L	113B	WE*	S0*	114B	MEM_A_CS_L<0>	12 92	
92 30 12 MEM_A_CAS_L	115B	CAS*	ODT0	116B	MEM_A_ODT<0>	12 92	
	117B	VDD_14	VDD_15	118B			
92 30 12 MEM_A_A<13>	119B	A13	ODT1	120B	MEM_A_ODT<1>	12 92	
92 12 MEM_A_CS_L<1>	121B	S1*	NC_1	122B			
	123B	VDD_16	VDD_17	124B			
	125B	TEST	VREFCA	126B	PP0V75_S3_MEM_VREFCA_A	28 30 98	
	127B	VSS_26	VSS_27	128B			
32 30 =MEM_A_DQ<32>	129B	DQ32	DQ36	130B	=MEM_A_DQ<36>	30 32	
32 30 =MEM_A_DQ<33>	131B	DQ33	DQ37	132B	=MEM_A_DQ<37>	30 32	
	133B	VSS_28	VSS_29	134B			
32 30 =MEM_A_DQS_N<4>	135B	DQS4*	DM4	136B			
32 30 =MEM_A_DQS_P<4>	137B	DQS4	VSS_30	138B			
	139B	VSS_31	DQ38	140B	=MEM_A_DQ<38>	30 32	
32 30 =MEM_A_DQ<34>	141B	DQ34	DQ39	142B	=MEM_A_DQ<39>	30 32	
32 30 =MEM_A_DQ<35>	143B	DQ35	VSS_32	144B			
	145B	VSS_33	DQ44	146B	=MEM_A_DQ<44>	30 32	
32 30 =MEM_A_DQ<40>	147B	DQ40	DQ45	148B	=MEM_A_DQ<45>	30 32	
32 30 =MEM_A_DQ<41>	149B	DQ41	VSS_34	150B			
	151B	VSS_35	DQS5*	152B	=MEM_A_DQS_N<5>	30 32	
	153B	DM5	DQS5	154B	=MEM_A_DQS_P<5>	30 32	
	155B	VSS_36	VSS_37	156B			
32 30 =MEM_A_DQ<42>	157B	DQ42	DQ46	158B	=MEM_A_DQ<46>	30 32	
32 30 =MEM_A_DQ<43>	159B	DQ43	DQ47	160B	=MEM_A_DQ<47>	30 32	
	161B	VSS_38	VSS_39	162B			
32 30 =MEM_A_DQ<48>	163B	DQ48	DQ52	164B	=MEM_A_DQ<52>	30 32	
32 30 =MEM_A_DQ<49>	165B	DQ49	DQ53	166B	=MEM_A_DQ<53>	30 32	
	167B	VSS_40	VSS_41	168B			
32 30 =MEM_A_DQS_N<6>	169B	DQS6*	DM6	170B			
32 30 =MEM_A_DQS_P<6>	171B	DQS6	VSS_42	172B			
	173B	VSS_43	DQ54	174B	=MEM_A_DQ<54>	30 32	
32 30 =MEM_A_DQ<50>	175B	DQ50	DQ55	176B	=MEM_A_DQ<55>	30 32	
32 30 =MEM_A_DQ<51>	177B	DQ51	VSS_44	178B			
	179B	VSS_45	DQ60	180B	=MEM_A_DQ<60>	30 32	
32 30 =MEM_A_DQ<56>	181B	DQ56	DQ61	182B	=MEM_A_DQ<61>	30 32	
32 30 =MEM_A_DQ<57>	183B	DQ57	VSS_46	184B			
	185B	VSS_47	DQS7*	186B	=MEM_A_DQS_N<7>	30 32	
	187B	DM7	DQS7	188B	=MEM_A_DQS_P<7>	30 32	
	189B	VSS_48	VSS_49	190B			
32 30 =MEM_A_DQ<58>	191B	DQ58	DQ62	192B	=MEM_A_DQ<62>	30 32	
32 30 =MEM_A_DQ<59>	193B	DQ59	DQ63	194B	=MEM_A_DQ<63>	30 32	
	195B	VSS_50	VSS_51	196B			
30 MEM_DIMM0_SA<0>	197B	SA0	EVENT*	198B	MEM_EVENT_L	30 31 47	
47 30 6 =PPSPD_S0_MEM_A	199B	VDDSPD	SDA	200B	=I2C_SODIMMA_SDA	30 49	
30 MEM_DIMM0_SA<1>	201B	SA1	SCL	202B	=I2C_SODIMMA_SCL	30 49	
30 6 =PP0V75_S0_MEM_VTT_A	203B	VTT_0	VTT_1	204B	=PP0V75_S0_MEM_VTT_A	6 30	

DIMM0 SPD ADDR=0XA0(WR)/0XA1(RD)

30 MEM_DIMM0_SA<1>
30 MEM_DIMM0_SA<0>

R3140 10K 5% 1/16W MF LF 402
R3141 10K 5% 1/16W MF LF 402

DIMM2 SPD ADDR=0XA2(WR)/0XA3(RD)

47 30 6 =PPSPD_S0_MEM_A

R3142 10K 5% 1/16W MF LF 402
R3143 10K 5% 1/16W MF LF 402

30 MEM_DIMM2_SA<0>
30 MEM_DIMM2_SA<1>

47 30 6 =PPSPD_S0_MEM_A

C3140 2.2UF 20% 6.3V CERM 402 LF

98 30 28 PP0V75_S3_MEM_VREFCA_A

C3135 2.2UF 20% 6.3V CERM 402 LF
C3136 0.1UF 20% 10V CERM 402

98 30 28 PP0V75_S3_MEM_VREFDQ_A

C3130 2.2UF 20% 6.3V CERM 402 LF
C3131 0.1UF 20% 10V CERM 402

30 6 =PP0V75_S0_MEM_VTT_A

C3150 2.2UF 20% 6.3V CERM 402 LF
C3151 2.2UF 20% 6.3V CERM 402 LF

STACKED SO-DIMM CONN.

DIMM2 (Section A)
DIMM0 (Section B)

CPU - MEM Ch. A

Page Notes

Power aliases required by this page
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2 5 3 3V)

Signal aliases required by this page
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

ALL DQ DQS DM SIGNALS TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page
(NONE)

SYNC_MASTER=K62_ROSITA SYNC_DATE=01/09/2011

PAGE TITLE: DDR3 SO-DIMM 0 & 2

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D
REVISION: 10.1.0
BRANCH:
PAGE: 31 OF 110
SHEET: 30 OF 101

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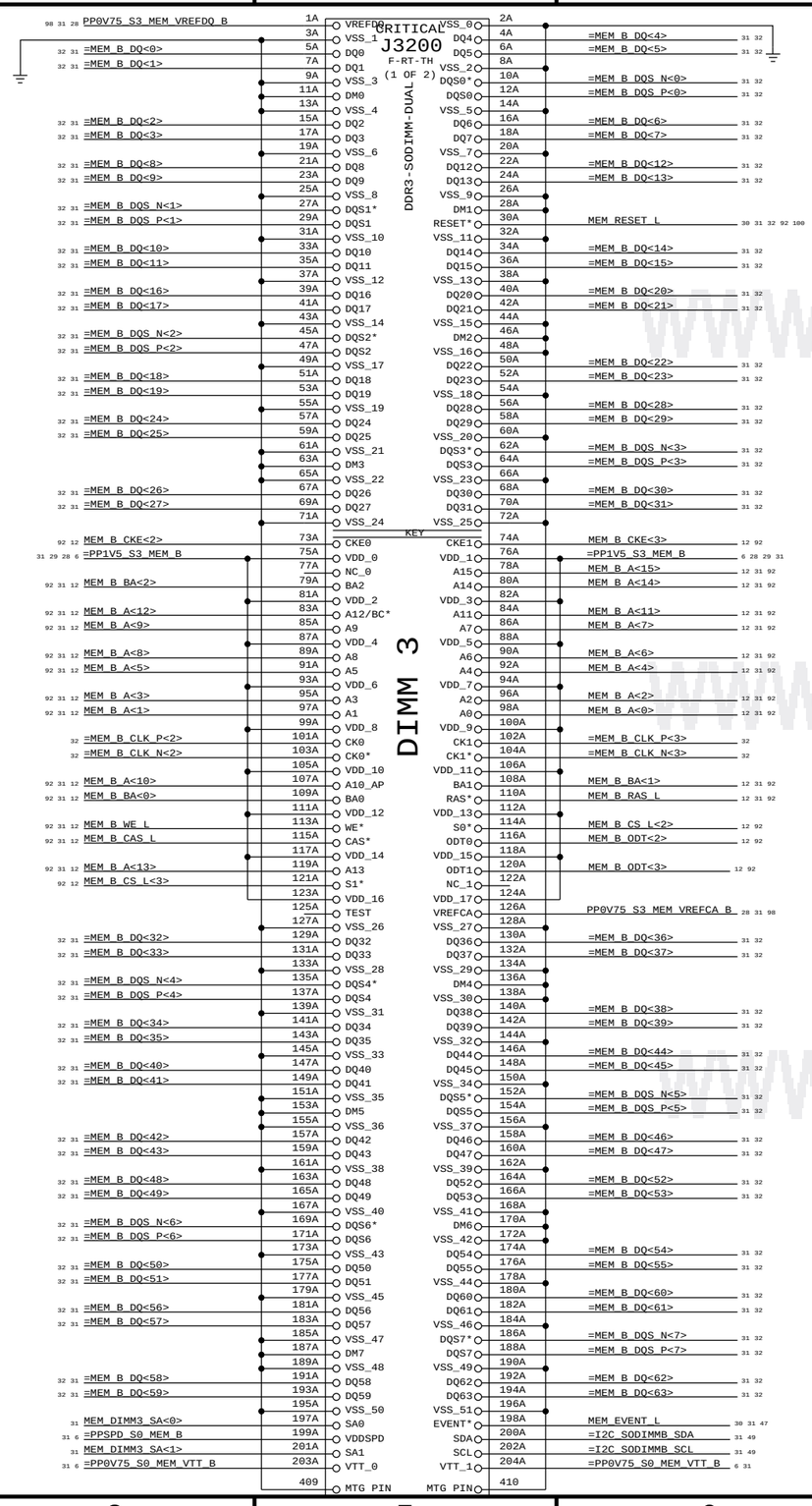

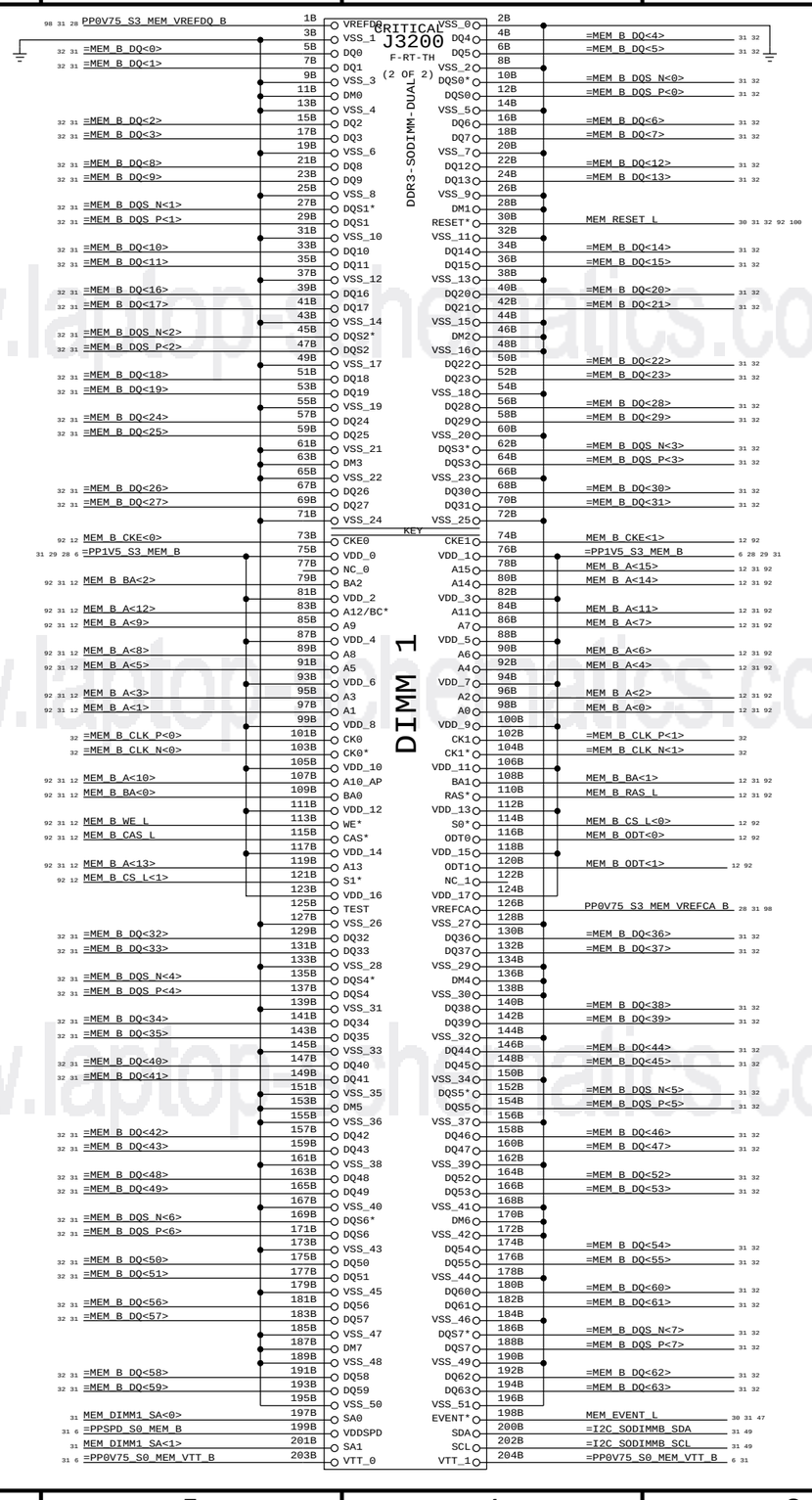

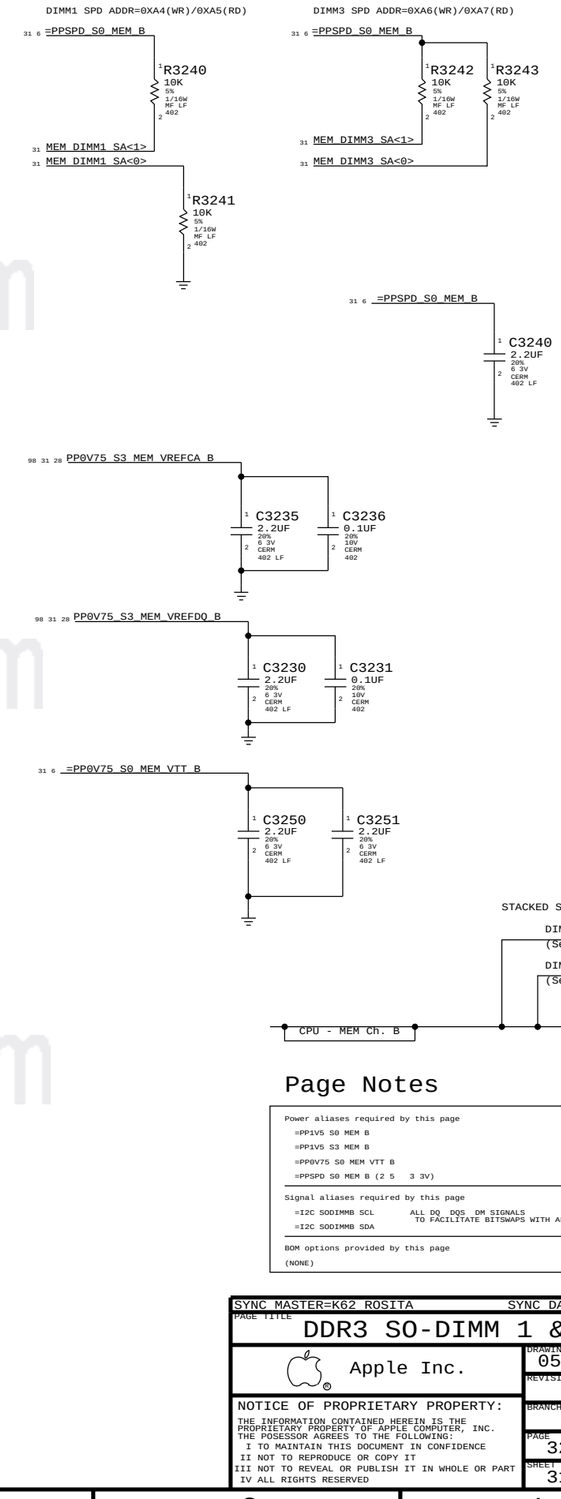

Page Notes

Power aliases required by this page
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2 5 3 3V)

Signal aliases required by this page
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

ALL DQ, DQS, DM SIGNALS TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page
(NONE)

SYNC MASTER=K62_ROSITA SYNC DATE=01/09/2011

PAGE TITLE: DDR3 SO-DIMM 1 & 3

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D
REVISION: 10.1.0
BRANCH:
PAGE: 32 OF 110
SHEET: 31 OF 101

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CPU CHANNEL A DQS 0 -> DIMM A DQS 7

MEM_A_DQS_N<0> — MAKE_BASE=TRUE — =MEM_A_DQS_N<7>
MEM_A_DQS_P<0> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_A_DQS_P<7>
MAKE_BASE=TRUE — NO_TEST=TRUE

MEM_A_DQ<7> — MAKE_BASE=TRUE — =MEM_A_DQ<57>
MEM_A_DQ<6> — MAKE_BASE=TRUE — =MEM_A_DQ<56>
MEM_A_DQ<5> — MAKE_BASE=TRUE — =MEM_A_DQ<58>
MEM_A_DQ<4> — MAKE_BASE=TRUE — =MEM_A_DQ<59>
MEM_A_DQ<3> — MAKE_BASE=TRUE — =MEM_A_DQ<60>
MEM_A_DQ<2> — MAKE_BASE=TRUE — =MEM_A_DQ<61>
MEM_A_DQ<1> — MAKE_BASE=TRUE — =MEM_A_DQ<62>
MEM_A_DQ<0> — MAKE_BASE=TRUE — =MEM_A_DQ<63>

CPU CHANNEL A DQS 1 -> DIMM A DQS 6

MEM_A_DQS_N<1> — MAKE_BASE=TRUE — =MEM_A_DQS_N<6>
MEM_A_DQS_P<1> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_A_DQS_P<6>
MAKE_BASE=TRUE — NO_TEST=TRUE

MEM_A_DQ<15> — MAKE_BASE=TRUE — =MEM_A_DQ<49>
MEM_A_DQ<14> — MAKE_BASE=TRUE — =MEM_A_DQ<52>
MEM_A_DQ<13> — MAKE_BASE=TRUE — =MEM_A_DQ<51>
MEM_A_DQ<12> — MAKE_BASE=TRUE — =MEM_A_DQ<50>
MEM_A_DQ<11> — MAKE_BASE=TRUE — =MEM_A_DQ<48>
MEM_A_DQ<10> — MAKE_BASE=TRUE — =MEM_A_DQ<53>
MEM_A_DQ<9> — MAKE_BASE=TRUE — =MEM_A_DQ<55>
MEM_A_DQ<8> — MAKE_BASE=TRUE — =MEM_A_DQ<54>

CPU CHANNEL A DQS 2 -> DIMM A DQS 5

MEM_A_DQS_N<2> — MAKE_BASE=TRUE — =MEM_A_DQS_N<5>
MEM_A_DQS_P<2> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_A_DQS_P<5>
MAKE_BASE=TRUE — NO_TEST=TRUE

MEM_A_DQ<23> — MAKE_BASE=TRUE — =MEM_A_DQ<40>
MEM_A_DQ<22> — MAKE_BASE=TRUE — =MEM_A_DQ<45>
MEM_A_DQ<21> — MAKE_BASE=TRUE — =MEM_A_DQ<46>
MEM_A_DQ<20> — MAKE_BASE=TRUE — =MEM_A_DQ<47>
MEM_A_DQ<19> — MAKE_BASE=TRUE — =MEM_A_DQ<41>
MEM_A_DQ<18> — MAKE_BASE=TRUE — =MEM_A_DQ<44>
MEM_A_DQ<17> — MAKE_BASE=TRUE — =MEM_A_DQ<43>
MEM_A_DQ<16> — MAKE_BASE=TRUE — =MEM_A_DQ<42>

CPU CHANNEL A DQS 3 -> DIMM A DQS 4

MEM_A_DQS_N<3> — MAKE_BASE=TRUE — =MEM_A_DQS_N<4>
MEM_A_DQS_P<3> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_A_DQS_P<4>
MAKE_BASE=TRUE — NO_TEST=TRUE

MEM_A_DQ<31> — MAKE_BASE=TRUE — =MEM_A_DQ<37>
MEM_A_DQ<30> — MAKE_BASE=TRUE — =MEM_A_DQ<33>
MEM_A_DQ<29> — MAKE_BASE=TRUE — =MEM_A_DQ<35>
MEM_A_DQ<28> — MAKE_BASE=TRUE — =MEM_A_DQ<34>
MEM_A_DQ<27> — MAKE_BASE=TRUE — =MEM_A_DQ<36>
MEM_A_DQ<26> — MAKE_BASE=TRUE — =MEM_A_DQ<32>
MEM_A_DQ<25> — MAKE_BASE=TRUE — =MEM_A_DQ<38>
MEM_A_DQ<24> — MAKE_BASE=TRUE — =MEM_A_DQ<39>

CPU CHANNEL A DQS 4 -> DIMM A DQS 3

MEM_A_DQS_N<4> — MAKE_BASE=TRUE — =MEM_A_DQS_N<3>
MEM_A_DQS_P<4> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_A_DQS_P<3>
MAKE_BASE=TRUE — NO_TEST=TRUE

MEM_A_DQ<39> — MAKE_BASE=TRUE — =MEM_A_DQ<28>
MEM_A_DQ<38> — MAKE_BASE=TRUE — =MEM_A_DQ<29>
MEM_A_DQ<37> — MAKE_BASE=TRUE — =MEM_A_DQ<27>
MEM_A_DQ<36> — MAKE_BASE=TRUE — =MEM_A_DQ<31>
MEM_A_DQ<35> — MAKE_BASE=TRUE — =MEM_A_DQ<25>
MEM_A_DQ<34> — MAKE_BASE=TRUE — =MEM_A_DQ<24>
MEM_A_DQ<33> — MAKE_BASE=TRUE — =MEM_A_DQ<26>
MEM_A_DQ<32> — MAKE_BASE=TRUE — =MEM_A_DQ<30>

CPU CHANNEL A DQS 5 -> DIMM A DQS 2

MEM_A_DQS_N<5> — MAKE_BASE=TRUE — =MEM_A_DQS_N<2>
MEM_A_DQS_P<5> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_A_DQS_P<2>
MAKE_BASE=TRUE — NO_TEST=TRUE

MEM_A_DQ<47> — MAKE_BASE=TRUE — =MEM_A_DQ<17>
MEM_A_DQ<46> — MAKE_BASE=TRUE — =MEM_A_DQ<16>
MEM_A_DQ<45> — MAKE_BASE=TRUE — =MEM_A_DQ<22>
MEM_A_DQ<44> — MAKE_BASE=TRUE — =MEM_A_DQ<23>
MEM_A_DQ<43> — MAKE_BASE=TRUE — =MEM_A_DQ<21>
MEM_A_DQ<42> — MAKE_BASE=TRUE — =MEM_A_DQ<20>
MEM_A_DQ<41> — MAKE_BASE=TRUE — =MEM_A_DQ<18>
MEM_A_DQ<40> — MAKE_BASE=TRUE — =MEM_A_DQ<19>

CPU CHANNEL A DQS 6 -> DIMM A DQS 1

MEM_A_DQS_N<6> — MAKE_BASE=TRUE — =MEM_A_DQS_N<1>
MEM_A_DQS_P<6> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_A_DQS_P<1>
MAKE_BASE=TRUE — NO_TEST=TRUE

MEM_A_DQ<55> — MAKE_BASE=TRUE — =MEM_A_DQ<12>
MEM_A_DQ<54> — MAKE_BASE=TRUE — =MEM_A_DQ<13>
MEM_A_DQ<53> — MAKE_BASE=TRUE — =MEM_A_DQ<10>
MEM_A_DQ<52> — MAKE_BASE=TRUE — =MEM_A_DQ<15>
MEM_A_DQ<51> — MAKE_BASE=TRUE — =MEM_A_DQ<8>
MEM_A_DQ<50> — MAKE_BASE=TRUE — =MEM_A_DQ<9>
MEM_A_DQ<49> — MAKE_BASE=TRUE — =MEM_A_DQ<11>
MEM_A_DQ<48> — MAKE_BASE=TRUE — =MEM_A_DQ<14>

CPU CHANNEL A DQS 7 -> DIMM A DQS 0

MEM_A_DQS_N<7> — MAKE_BASE=TRUE — =MEM_A_DQS_N<0>
MEM_A_DQS_P<7> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_A_DQS_P<0>
MAKE_BASE=TRUE — NO_TEST=TRUE

MEM_A_DQ<63> — MAKE_BASE=TRUE — =MEM_A_DQ<5>
MEM_A_DQ<62> — MAKE_BASE=TRUE — =MEM_A_DQ<4>
MEM_A_DQ<61> — MAKE_BASE=TRUE — =MEM_A_DQ<3>
MEM_A_DQ<60> — MAKE_BASE=TRUE — =MEM_A_DQ<2>
MEM_A_DQ<59> — MAKE_BASE=TRUE — =MEM_A_DQ<1>
MEM_A_DQ<58> — MAKE_BASE=TRUE — =MEM_A_DQ<0>
MEM_A_DQ<57> — MAKE_BASE=TRUE — =MEM_A_DQ<7>
MEM_A_DQ<56> — MAKE_BASE=TRUE — =MEM_A_DQ<6>

CPU CHANNEL B DQS 0 -> DIMM B DQS 7

MEM_B_DQS_N<0> — MAKE_BASE=TRUE — =MEM_B_DQS_N<7>
MEM_B_DQS_P<0> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_B_DQS_P<7>
MAKE_BASE=TRUE — NO_TEST=TRUE

MEM_B_DQ<7> — MAKE_BASE=TRUE — =MEM_B_DQ<61>
MEM_B_DQ<6> — MAKE_BASE=TRUE — =MEM_B_DQ<60>
MEM_B_DQ<5> — MAKE_BASE=TRUE — =MEM_B_DQ<62>
MEM_B_DQ<4> — MAKE_BASE=TRUE — =MEM_B_DQ<63>
MEM_B_DQ<3> — MAKE_BASE=TRUE — =MEM_B_DQ<56>
MEM_B_DQ<2> — MAKE_BASE=TRUE — =MEM_B_DQ<57>
MEM_B_DQ<1> — MAKE_BASE=TRUE — =MEM_B_DQ<58>
MEM_B_DQ<0> — MAKE_BASE=TRUE — =MEM_B_DQ<59>

CPU CHANNEL B DQS 1 -> DIMM B DQS 6

MEM_B_DQS_N<1> — MAKE_BASE=TRUE — =MEM_B_DQS_N<6>
MEM_B_DQS_P<1> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_B_DQS_P<6>
MAKE_BASE=TRUE — NO_TEST=TRUE

MEM_B_DQ<15> — MAKE_BASE=TRUE — =MEM_B_DQ<51>
MEM_B_DQ<14> — MAKE_BASE=TRUE — =MEM_B_DQ<54>
MEM_B_DQ<13> — MAKE_BASE=TRUE — =MEM_B_DQ<53>
MEM_B_DQ<12> — MAKE_BASE=TRUE — =MEM_B_DQ<52>
MEM_B_DQ<11> — MAKE_BASE=TRUE — =MEM_B_DQ<48>
MEM_B_DQ<10> — MAKE_BASE=TRUE — =MEM_B_DQ<49>
MEM_B_DQ<9> — MAKE_BASE=TRUE — =MEM_B_DQ<50>
MEM_B_DQ<8> — MAKE_BASE=TRUE — =MEM_B_DQ<55>

CPU CHANNEL B DQS 2 -> DIMM B DQS 5

MEM_B_DQS_N<2> — MAKE_BASE=TRUE — =MEM_B_DQS_N<5>
MEM_B_DQS_P<2> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_B_DQS_P<5>
MAKE_BASE=TRUE — NO_TEST=TRUE

MEM_B_DQ<23> — MAKE_BASE=TRUE — =MEM_B_DQ<45>
MEM_B_DQ<22> — MAKE_BASE=TRUE — =MEM_B_DQ<40>
MEM_B_DQ<21> — MAKE_BASE=TRUE — =MEM_B_DQ<42>
MEM_B_DQ<20> — MAKE_BASE=TRUE — =MEM_B_DQ<47>
MEM_B_DQ<19> — MAKE_BASE=TRUE — =MEM_B_DQ<44>
MEM_B_DQ<18> — MAKE_BASE=TRUE — =MEM_B_DQ<41>
MEM_B_DQ<17> — MAKE_BASE=TRUE — =MEM_B_DQ<46>
MEM_B_DQ<16> — MAKE_BASE=TRUE — =MEM_B_DQ<43>

CPU CHANNEL B DQS 3 -> DIMM B DQS 4

MEM_B_DQS_N<3> — MAKE_BASE=TRUE — =MEM_B_DQS_N<4>
MEM_B_DQS_P<3> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_B_DQS_P<4>
MAKE_BASE=TRUE — NO_TEST=TRUE

MEM_B_DQ<31> — MAKE_BASE=TRUE — =MEM_B_DQ<32>
MEM_B_DQ<30> — MAKE_BASE=TRUE — =MEM_B_DQ<39>
MEM_B_DQ<29> — MAKE_BASE=TRUE — =MEM_B_DQ<37>
MEM_B_DQ<28> — MAKE_BASE=TRUE — =MEM_B_DQ<38>
MEM_B_DQ<27> — MAKE_BASE=TRUE — =MEM_B_DQ<35>
MEM_B_DQ<26> — MAKE_BASE=TRUE — =MEM_B_DQ<34>
MEM_B_DQ<25> — MAKE_BASE=TRUE — =MEM_B_DQ<36>
MEM_B_DQ<24> — MAKE_BASE=TRUE — =MEM_B_DQ<33>

CPU CHANNEL B DQS 4 -> DIMM B DQS 3

MEM_B_DQS_N<4> — MAKE_BASE=TRUE — =MEM_B_DQS_N<3>
MEM_B_DQS_P<4> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_B_DQS_P<3>
MAKE_BASE=TRUE — NO_TEST=TRUE

MEM_B_DQ<39> — MAKE_BASE=TRUE — =MEM_B_DQ<28>
MEM_B_DQ<38> — MAKE_BASE=TRUE — =MEM_B_DQ<24>
MEM_B_DQ<37> — MAKE_BASE=TRUE — =MEM_B_DQ<31>
MEM_B_DQ<36> — MAKE_BASE=TRUE — =MEM_B_DQ<30>
MEM_B_DQ<35> — MAKE_BASE=TRUE — =MEM_B_DQ<29>
MEM_B_DQ<34> — MAKE_BASE=TRUE — =MEM_B_DQ<25>
MEM_B_DQ<33> — MAKE_BASE=TRUE — =MEM_B_DQ<27>
MEM_B_DQ<32> — MAKE_BASE=TRUE — =MEM_B_DQ<26>

CPU CHANNEL B DQS 5 -> DIMM B DQS 2

MEM_B_DQS_N<5> — MAKE_BASE=TRUE — =MEM_B_DQS_N<2>
MEM_B_DQS_P<5> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_B_DQS_P<2>
MAKE_BASE=TRUE — NO_TEST=TRUE

MEM_B_DQ<47> — MAKE_BASE=TRUE — =MEM_B_DQ<18>
MEM_B_DQ<46> — MAKE_BASE=TRUE — =MEM_B_DQ<20>
MEM_B_DQ<45> — MAKE_BASE=TRUE — =MEM_B_DQ<23>
MEM_B_DQ<44> — MAKE_BASE=TRUE — =MEM_B_DQ<22>
MEM_B_DQ<43> — MAKE_BASE=TRUE — =MEM_B_DQ<19>
MEM_B_DQ<42> — MAKE_BASE=TRUE — =MEM_B_DQ<21>
MEM_B_DQ<41> — MAKE_BASE=TRUE — =MEM_B_DQ<17>
MEM_B_DQ<40> — MAKE_BASE=TRUE — =MEM_B_DQ<16>

CPU CHANNEL B DQS 6 -> DIMM B DQS 1

MEM_B_DQS_N<6> — MAKE_BASE=TRUE — =MEM_B_DQS_N<1>
MEM_B_DQS_P<6> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_B_DQS_P<1>
MAKE_BASE=TRUE — NO_TEST=TRUE

MEM_B_DQ<55> — MAKE_BASE=TRUE — =MEM_B_DQ<8>
MEM_B_DQ<54> — MAKE_BASE=TRUE — =MEM_B_DQ<14>
MEM_B_DQ<53> — MAKE_BASE=TRUE — =MEM_B_DQ<10>
MEM_B_DQ<52> — MAKE_BASE=TRUE — =MEM_B_DQ<11>
MEM_B_DQ<51> — MAKE_BASE=TRUE — =MEM_B_DQ<9>
MEM_B_DQ<50> — MAKE_BASE=TRUE — =MEM_B_DQ<15>
MEM_B_DQ<49> — MAKE_BASE=TRUE — =MEM_B_DQ<12>
MEM_B_DQ<48> — MAKE_BASE=TRUE — =MEM_B_DQ<13>

CPU CHANNEL B DQS 7 -> DIMM B DQS 0

MEM_B_DQS_N<7> — MAKE_BASE=TRUE — =MEM_B_DQS_N<0>
MEM_B_DQS_P<7> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_B_DQS_P<0>
MAKE_BASE=TRUE — NO_TEST=TRUE

MEM_B_DQ<63> — MAKE_BASE=TRUE — =MEM_B_DQ<2>
MEM_B_DQ<62> — MAKE_BASE=TRUE — =MEM_B_DQ<1>
MEM_B_DQ<61> — MAKE_BASE=TRUE — =MEM_B_DQ<3>
MEM_B_DQ<60> — MAKE_BASE=TRUE — =MEM_B_DQ<7>
MEM_B_DQ<59> — MAKE_BASE=TRUE — =MEM_B_DQ<4>
MEM_B_DQ<58> — MAKE_BASE=TRUE — =MEM_B_DQ<5>
MEM_B_DQ<57> — MAKE_BASE=TRUE — =MEM_B_DQ<6>
MEM_B_DQ<56> — MAKE_BASE=TRUE — =MEM_B_DQ<0>

DDR3 RESET SUPPORT

SNB? CANNOT CONTROL THIS SIGNAL DIRECTLY SINCE IT MUST BE HIGH IN SLEEP AND CPU MEM RAILS ARE NOT POWERED IN SLEEP.

	CPU_RESET_L	ISOLATE_L	MEM_RESET_L
S5	0	3.3V	0
S0	0	3.3V	0
S0	1.5V	3.3V	1.5V
S3	0	0	1.5V
S0	1.5V	3.3V	1.5V
S5	0	3.3V	0

S	R	CLK	D	Q	QB
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	POSEDGE	L	L	H
H	H	POSEDGE	H	H	L

=PP3V3_S3_MEMRESET — R3350 20K 5% 1/16W MF-LF 402 — ISOLATE_CPU_MEM_L_R1
=PP5V_S3_MEMRESET — R3351 20K 5% 1/16W MF-LF 402 — ISOLATE_CPU_MEM
R3352 20K 5% 1/16W MF-LF 402
Q3306 2N7002DW-X-G SOT 363
Q3306 2N7002DW-X-G SOT 363
CPU_MEM_RESET_L — NOSTUFF R3355 0 5% 1/16W MF-LF 402
=PP1V5_S3_MEMRESET — C3353 0.0022UF 10% 16V CERM 402 — R3353 20K 5% 1/16W MF-LF 402 — MEM_RESET_L
Q3304 2N7002 SOT23-HF1 — ISOLATE_CPU_MEM_5V_L

=PP3V3_S5_MEMRESET — C3300 0.1UF 20% 16V CERM 402 — MEM_RESET_HW
U3300 74LVC74ABQ DHVQFN
PM_SLP_S4_L — 1SD*
PM_SYS_PWRGD — 1D
=PP3V3_S3_MEMRESET — 1CP
PM_SLP_S4_D_L — 1RD*
=PP3V3_S3_MEMRESET — 2SD*
CPU_MEM_RESET3V3_L — 2D
PM_SLP_S3_L — 2CP
2RD*
THRM GND_PAD
1Q* — PM_SLP_S4_D_L
1Q — TP_PM_SLP_S4_D
2Q* — ISOLATE_CPU_MEMHW_L
2Q — TP_ISOLATE_CPU
R3385 0 5% 1/16W MF-LF 402 — ISOLATE_CPU_MEM_L
NOSTUFF R3383 0 5% 1/16W MF-LF 402 — ISOLATE_CPU_MEM_L_R1
CPU_MEM_RESET_L — NOSTUFF R3380 10K 5% 1/16W MF-LF 402 — CPU_MEM_RESET_R_L

=PP3V3_S5_MEMRESET — MEM_RESET_HW R3381 10K 5% 1/16W MF-LF 402 — MEM_RESET_HW R3382 10K 5% 1/16W MF-LF 402
CPU_MEM_RESET3V3 — CPU_MEM_RESET3V3_L
MEM_RESET_HW Q3360 2N3904 SOT23-HF
MEM_RESET_HW Q3350 2N7002 SOT23-HF1

=PP3V3_S5_MEMRESET — NOSTUFF C3390 0.1UF 20% 16V CERM 402
ALL_SYS_PWRGD_R — NOSTUFF R3390 0 5% 1/16W MF-LF 402
NOSTUFF R3391 0 5% 1/16W MF-LF 402 — PM_EN_DDRVTT_S0_REG
DDRSYS_EN — U3390 NOSTUFF MC74VHC1G08 SOT23-5-HF — SLP_S3_CTL_L
NOSTUFF R3393 0 5% 1/16W MF-LF 402
R3394 0 5% 1/16W MF-LF 402 — PM_SLP_S3_L — PM_SLP_S3_5V_R2

=PP5V_S3_MEMRESET — R3387 20K 5% 1/16W MF-LF 402 — R3384 20K 5% 1/16W MF-LF 402
PM_SLP_S3_5V — PM_SLP_S3_5V_L
Q3370 2N7002DW-X-G SOT 363
Q3370 2N7002DW-X-G SOT 363

NOSTUFF R3386 0 5% 1/16W MF-LF 402
Q3375 FDMC8296 POWER33
=PP0V75_S0_MEM_VTT_S0FET — PPVTT_S0_DDR_FET
R3340 100K 5% 1/16W MF-LF 402 — PM_SLP_S3_5V_L
R3388 10 5% 1/16W MF-LF 402 — VTT_R
Q3380 2N7002 SOT23-HF1 — PM_SLP_S3_5V

MEMORY CLOCK ALIASING

MEM_A_CLK_P<0> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_A_CLK_P<0>
MEM_A_CLK_N<0> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_A_CLK_N<0>
MEM_A_CLK_P<1> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_A_CLK_P<1>
MEM_A_CLK_N<1> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_A_CLK_N<1>
MEM_A_CLK_P<2> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_A_CLK_P<2>
MEM_A_CLK_N<2> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_A_CLK_N<2>
MEM_A_CLK_P<3> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_A_CLK_P<3>
MEM_A_CLK_N<3> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_A_CLK_N<3>

MEM_B_CLK_P<0> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_B_CLK_P<0>
MEM_B_CLK_N<0> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_B_CLK_N<0>
MEM_B_CLK_P<1> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_B_CLK_P<1>
MEM_B_CLK_N<1> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_B_CLK_N<1>
MEM_B_CLK_P<2> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_B_CLK_P<2>
MEM_B_CLK_N<2> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_B_CLK_N<2>
MEM_B_CLK_P<3> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_B_CLK_P<3>
MEM_B_CLK_N<3> — MAKE_BASE=TRUE — NO_TEST=TRUE — =MEM_B_CLK_N<3>

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AP WAKE# ISOLATION

=PP3V3_S3_MINI_CONN 33

Q3470
SSM3K15FV
SOD-VESM-HF

R3470 10K 5% 1/16W MF-LF 402

100 79 36 19 OUT PCIE WAKE_L

NOSTUFF
R3400 0 5% 1/16W MF-LF 402

NOSTUFF
R3401 0 5% 1/16W MF-LF 402

3.3V S3 CURRENT	D0_D2_D2HOT	D3COLD
MAX CONT.	1760MA	750MA
MAX PEAK	2750MA	2750MA
1.5V CURRENT		
MAX CONT.	N/U	N/U
MAX PEAK	N/U	N/U

NOTE: CURRENT DATA PER APR 5,2010 PCIE MINI CEM ECN

CRITICAL
J3400
AS0B226-S40N-7F
F-RT-SM

AP_WAKE_L
RSVD MINI WLAN ACTIVE
RSVD MINI BT ACTIVE
33 OUT AP MINI CLKREQ_L
93 18 IN PCIE CLK100M MINI N
93 18 IN PCIE CLK100M MINI P

RESERVED
RESERVED

93 18 OUT PCIE MINI D2R N
93 18 OUT PCIE MINI D2R P

PLACEMENT_NOTE=PLACE CLOSE TO U1800.
C3431 0.1uF 10% 16V X5R 402
93 18 IN PCIE MINI R2D C N

PLACEMENT_NOTE=PLACE CLOSE TO U1800.
C3430 0.1uF 10% 16V X5R 402
93 18 IN PCIE MINI R2D C P

93 PCIE MINI R2D N
93 PCIE MINI R2D P

AP MINI RESET L 33 100 IN

SMB MINI SCL
SMB MINI SDA

TP USB MININ
TP USB MINIP

NO AVAILALBLE USB ON THIS PLATFORM
TARGET CARDS DO NOT USE IT

516S0457

=PP3V3_S3_MINI_CONN 33

C3410 0.1uF 20% 10V CERM 402
C3420 0.1uF 20% 10V CERM 402
C3421 10uF 20% 6.3V X5R 603

=PP1V5_S0_MINI 6

NOSTUFF C3400 0.1uF 20% 10V CERM 402
NOSTUFF C3401 10uF 20% 6.3V X5R 603

NOSTUFF
R3490 0 5% 1/16W MF-LF 402
=SMB_MINI_SCL 49

NOSTUFF
R3491 0 5% 1/16W MF-LF 402
=SMB_MINI_SDA 49

=PP3V3_S3_MINI_CONN 33

R3412 100K 1% 1/16W MF-LF 402

100 33 PM_PGOOD_MINI

VDD
Q3406
SLG4AP016V
TDFN

SENSE
0.7V
DLY
RESET*
MR*
EN
OUT (OD)
IN
THRM PAD
GND

100 33 OUT AP_MINI_RESET_L

33 IN AP_MINI_CLKREQ_L

RESET HAS 100MS DELAY ONCE ENABLE IS HIGH

MINI_RESET_L 27 100 IN
AP_PWR_EN_FET 33 IN
MINI_CLKREQ_L 15 100 OUT

=PP3V3_S3_MINI 6 33

C3408 0.1UF 10% 16V X5R 402

74 64 6 =PP12V_S5_PWRCTL

CRITICAL
Q3403
IRFH3702TRPBF
PQFN

C3461 0.1UF 10% 16V X5R 402

PP3V3_S3_MINI_CONN 98
VOLTAGE=3.3V
MIN LINE WIDTH=0.6MM
MIN NECK WIDTH=0.2MM
=PP3V3_S3_MINI_CONN 33

33 6 =PP3V3_S3_MINI

P3V3_S0_MINI_EN G 4

=PP3V3_S3_MINI
33 6

R3410 10K 5% 1/16W MF-LF 402

100 33 PM_PGOOD_MINI

VCC
U3404
SLG5AP001
TDFN

D
G
PG
ON
S
NC
CRITICAL
THRM PAD
GND

33 AP_PWR_EN_FET

AP PWR EN ISOLATION

=PP3V3_S3_MINI 6 33

Q3471
SSM3K15FV
SOD-VESM-HF
AP

R3471 10K 5% 1/16W MF-LF 402

100 25 20 AP_PWR_EN

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	REVISION: 10.1.0
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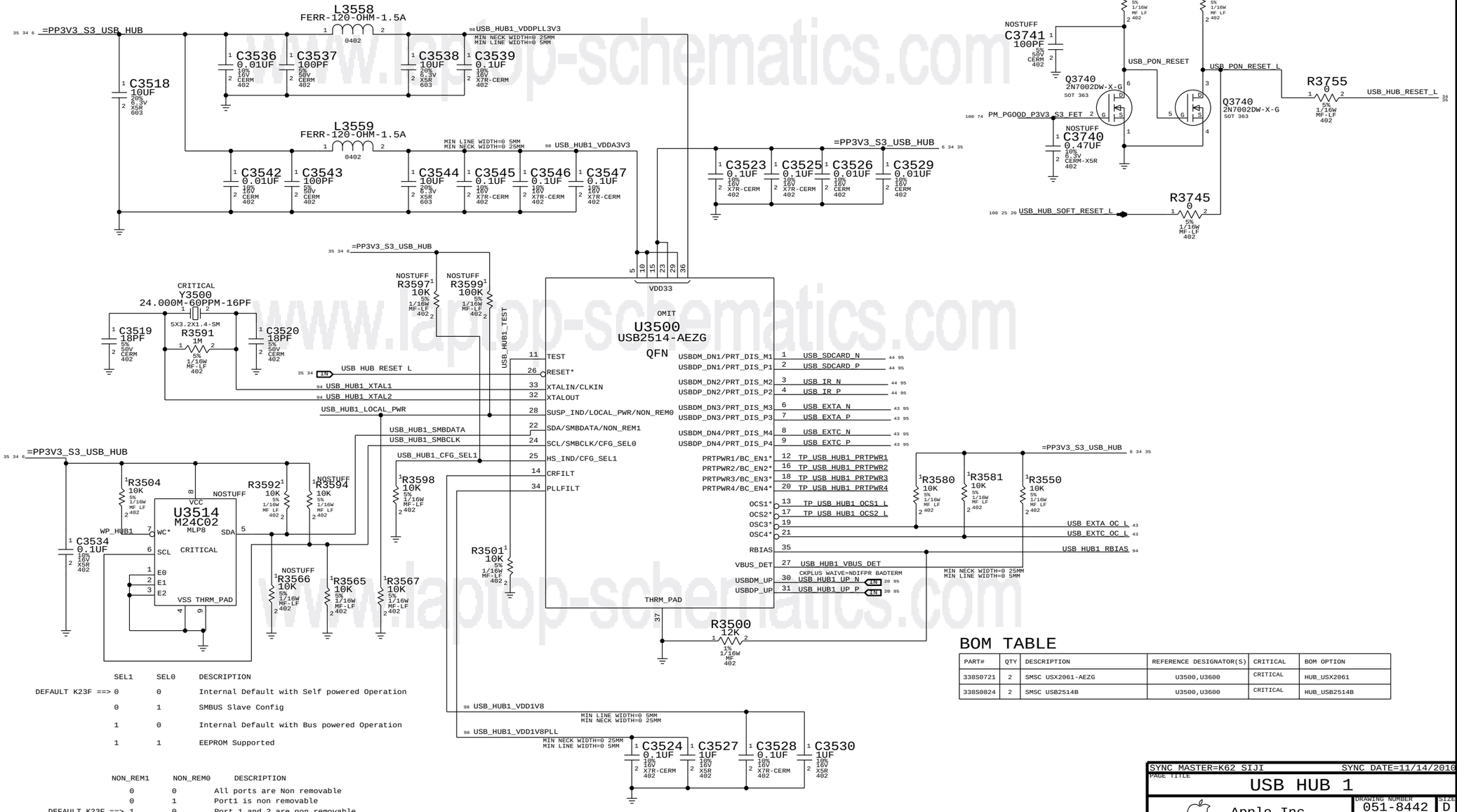
USB HUB-1



SEL1	SEL0	DESCRIPTION
DEFAULT K23F ==> 0	0	Internal Default with Self powered Operation
0	1	SMBUS Slave Config
1	0	Internal Default with Bus powered Operation
1	1	EEPROM Supported

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are Non removable
0	1	Port1 is non removable
DEFAULT K23F ==> 1	0	Port 1 and 2 are non removable
1	1	Port1,2 and 3 are non Removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0721	2	SMSC USX2061-AEZG	U3500,U3600	CRITICAL	HUB_USX2061
338S0824	2	SMSC USB2514B	U3500,U3600	CRITICAL	HUB_USB2514B

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PAGE TITLE: USB HUB 1

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

REVISION: 10.1.0

BRANCH:

PAGE: 35 OF 110

SHEET: 34 OF 101

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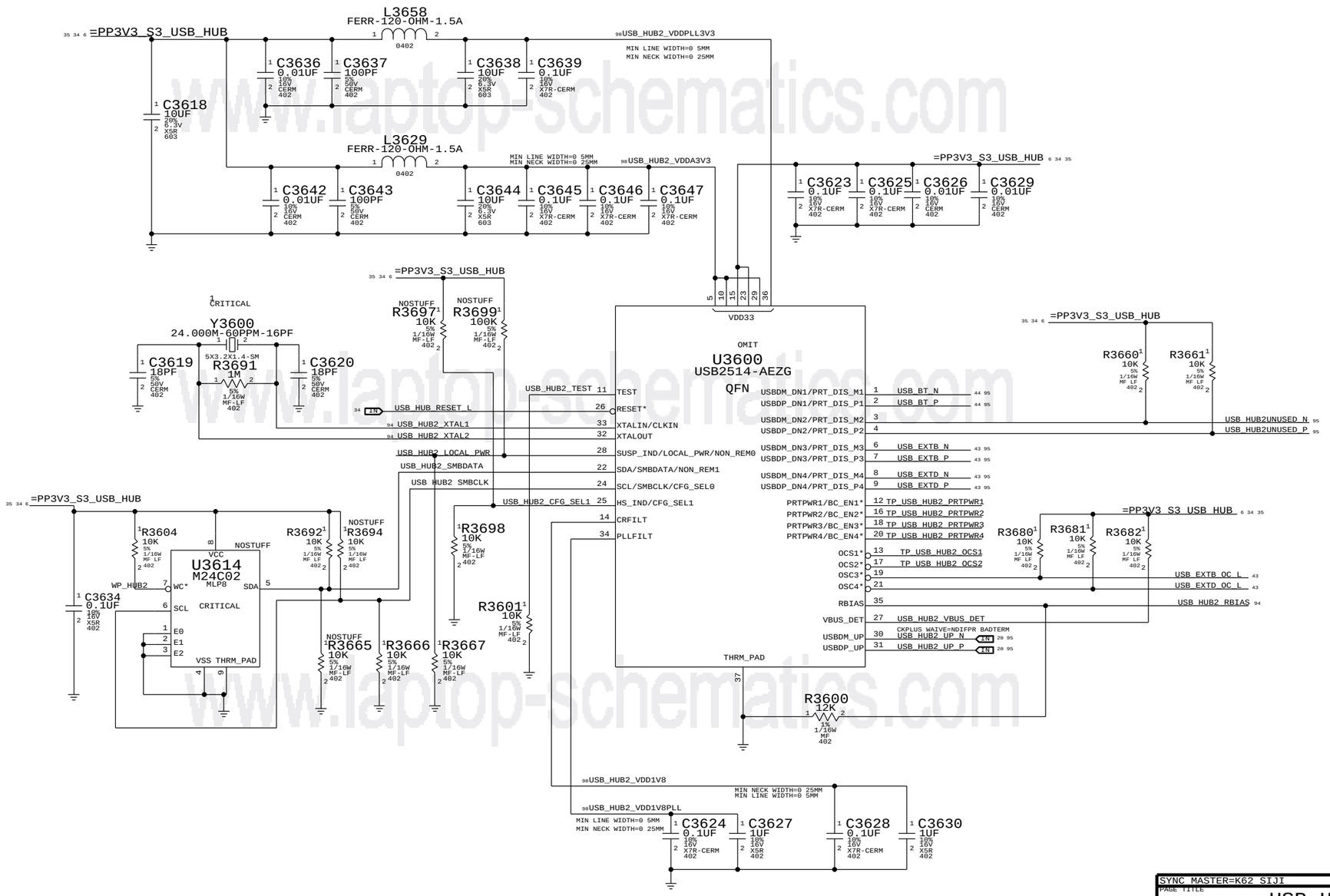
USB HUB-2



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SYNC MASTER=K62 SIJI SYNC DATE=11/14/2010

PAGE TITLE: USB HUB 2

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

REVISION: 10.1.0

BRANCH:

PAGE: 36 OF 110

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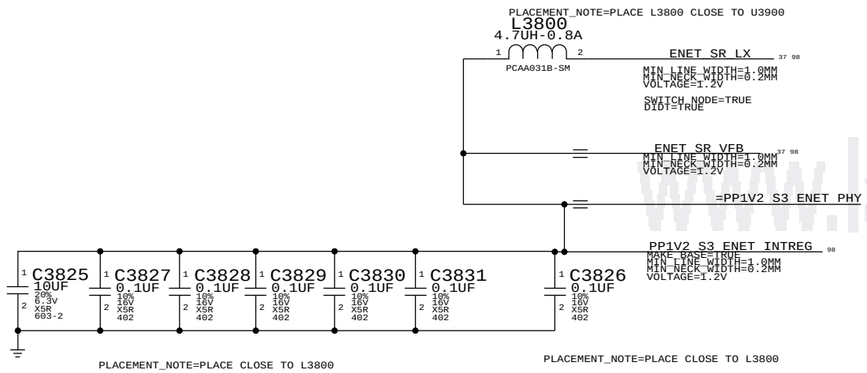
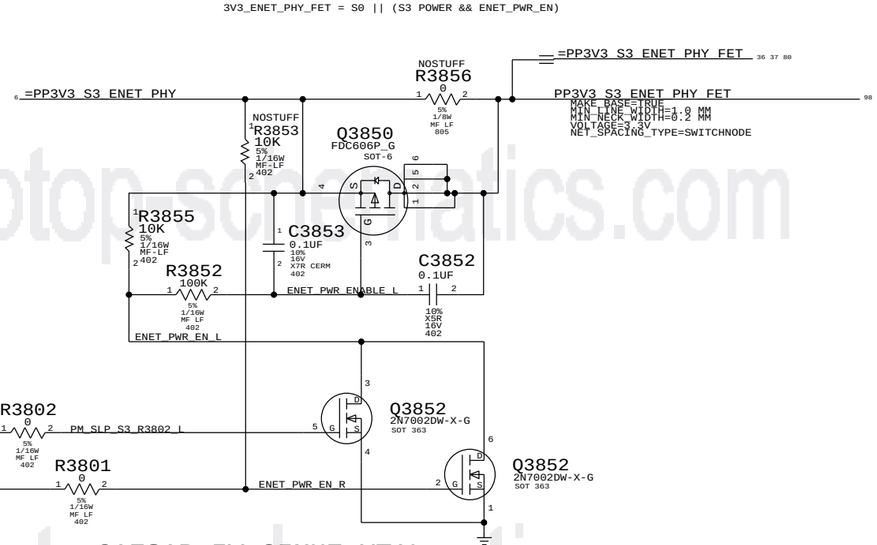
CAESAR IV 1.2V INT.VR CMPTS

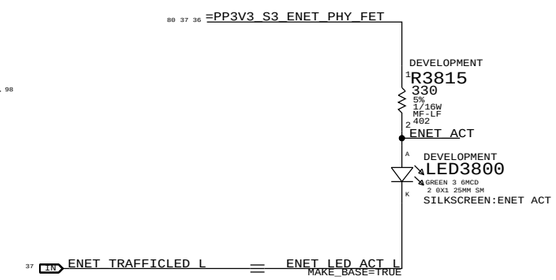


CAESAR IV POWER ENABLE CIRCUIT

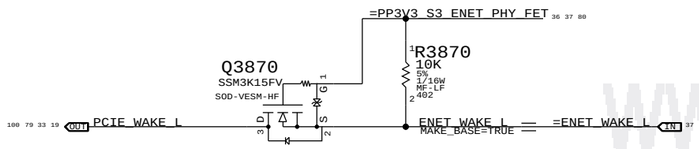
3V3_ENET_PHY_FET = S0 || (S3 POWER && ENET_PWR_EN)



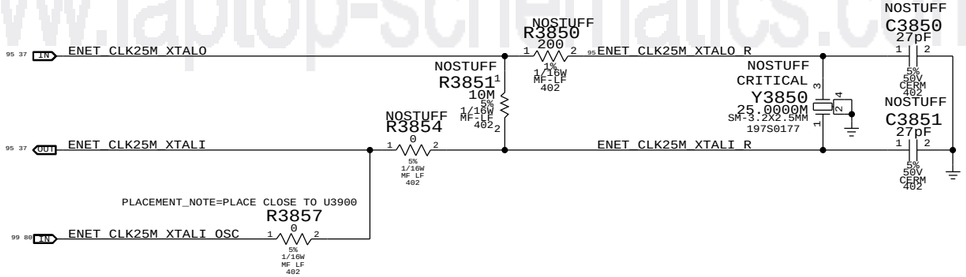
CAESAR IV ACTIVITY LED



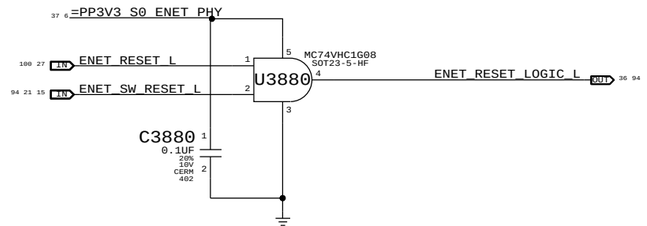
CAESAR IV WAKE# ISOLATION



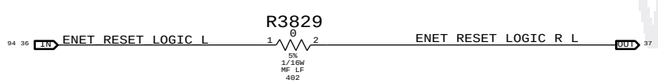
CAESAR IV 25MHZ XTAL



CAESAR IV SW RESET GATING

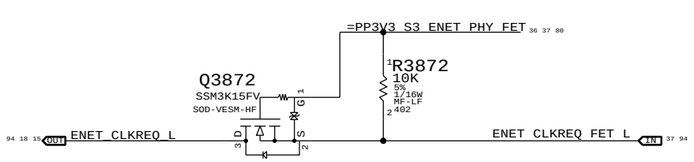


CAESAR IV RESET CONNECTION



CAESAR IV STRAPS (NONE)

CAESAR IV CLKREQ ISOLATION



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SYNC MASTER=K62 MARK SYNC DATE=01/09/2011

PAGE TITLE: CAESAR IV SUPPORT

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

281mA (1000base-T max power, Caesar IV)

=PP3V3_S3_ENET_PHY_FET

R3901 0 5% 1/16W MF LF 402 — ENET_3V3_S3_SR_IN
SWITCH NODE=TRUE
DIDT=TRUE
NET SPACING TYPE=SWITCHNODE
MIN LINE WIDTH 0 4 MM
MIN NECK WIDTH 0 2 MM
VOLTAGE 3 3V

C3979 4.7UF 20% 6.3V CERM 603

C3980 0.1UF 10% 16V X5R 402
C3981 0.1UF 10% 16V X5R 402

VDD for Card Reader I/O
=PP3V3R1V8_ENET_LR_OUT

CRITICAL L3900 FERR-600-OHM-0.5A SM — PP3V3_S3_ENET_PHY_XTALVDDH
MIN LINE WIDTH=0 4 mm
MIN NECK WIDTH=0 2 mm
VOLTAGE=3 3V

R3900 0 5% 1/16W MF LF 402 — ENET_XTALVDDH
MIN LINE WIDTH=0 4 mm
MIN NECK WIDTH=0 2 mm
VOLTAGE=3 3V

C3900 0.1UF 10% 16V X7R CERM 402

CRITICAL L3905 FERR-600-OHM-0.5A SM — PP3V3_S3_ENET_PHY_BIASVDDH
MIN LINE WIDTH=0 4 mm
MIN NECK WIDTH=0 2 mm
VOLTAGE=3 3V

C3905 0.1UF 10% 16V X7R CERM 402

CRITICAL L3910 FERR-600-OHM-0.5A SM — PP3V3_S3_ENET_PHY_AVDDH
MIN LINE WIDTH=0 4 mm
MIN NECK WIDTH=0 2 mm
VOLTAGE=3 3V

R3910 4.7K 5% 1/16W MF LF 402
C3910 0.1UF 10% 16V X7R CERM 402
C3911 0.1UF 10% 16V X7R CERM 402

R3940 4.7K 5% 1/16W MF LF 402
R3941 4.7K 5% 1/16W MF LF 402

C3917 0.1UF 10% 16V X7R CERM 402
C3918 0.1UF 10% 16V X7R CERM 402
C3915 4.7UF 10% 6.3V X5R CERM 603
C3916 0.1UF 10% 16V X7R CERM 402

ENET_SR_LX
ENET_SR_VFB

Internal 1.2V Switching Regulator pins.

=PP1V2_S3_ENET_PHY
396mA (1000base-T, Caesar II)

CRITICAL L3920 FERR-600-OHM-0.5A SM — PP1V2_S3_ENET_PHY_AVDDL
MIN LINE WIDTH=0 4 mm
MIN NECK WIDTH=0 2 mm
VOLTAGE=1 2V

C3921 0.1UF 10% 16V X7R CERM 402
C3920 4.7UF 10% 6.3V X5R CERM 603

CRITICAL L3925 FERR-600-OHM-0.5A SM — PP1V2_S3_ENET_PHY_PCIEPLL
MIN LINE WIDTH=0 4 mm
MIN NECK WIDTH=0 2 mm
VOLTAGE=1 2V

C3926 0.1UF 10% 16V X7R CERM 402
C3925 4.7UF 10% 6.3V X5R CERM 603

CRITICAL L3930 FERR-600-OHM-0.5A SM — PP1V2_S3_ENET_PHY_GPHYPLL
MIN LINE WIDTH=0 4 mm
MIN NECK WIDTH=0 2 mm
VOLTAGE=1 2V

C3931 0.1UF 10% 16V X7R CERM 402
C3930 4.7UF 10% 6.3V X5R CERM 603

C3936 0.1UF 10% 16V X7R CERM 402
C3935 10UF 10% 6.3V X5R 805

AVDDH (42, 48) — BIASVDDH (37) — XTALVDDH (17) — VDDO (7, 20, 56, 62) — SR_VDD (14) — SR_VDDP (15) — SR_LX (16) — SR_VFB (13) — AVDDL (39, 45, 51) — PCIE_PLLVDDL (29, 32) — GPHY_PLLVDDL (36) — VDDC (35, 61)

OMIT
U3900
BCM57765
QFN-8X8

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

=PP3V3R1V8_ENET_LR_OUT — PP3V3R1V8_ENET_LR_OUT_REG
MIN LINE WIDTH=0 3 mm
MIN NECK WIDTH=0 2 mm
VOLTAGE=1 8V

DEVELOPMENT: C3970 4.7UF 10% 6.3V X5R CERM 603; C3971 0.1UF 10% 16V X7R CERM 402; C3972 0.1UF 10% 16V X7R CERM 402; R3959 150 5% 1/16W MF LF 402; C3959 10PF 5% 50V CERM 402 — NOSTUFF

MUST DO: REMOVE C/R3959 AFTER PROTO 2

=PP3V3_S0_ENET_PHY

R3942 1K 5% 1/16W MF LF 402 — Current Limiting Resistor

C3950 0.1uF 10% 16V X5R 402
C3951 0.1uF 10% 16V X5R 402
C3955 0.1uF 10% 16V X5R 402
C3956 0.1uF 10% 16V X5R 402

PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_P
PCIE_ENET_R2D_C_N

R3943 0 5% 1/16W MF LF 402 — =ENET_WAKE_L (See note)

WAKE#

Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

ENET_VMAIN_PRSNT — VMAIN_PRSNT (IPD ENET)

PCIE_ENET_D2R_C_N — PCIE_TXD_N
PCIE_ENET_D2R_C_P — PCIE_TXD_P
PCIE_ENET_R2D_P — PCIE_RXD_P
PCIE_ENET_R2D_N — PCIE_RXD_N

PCIE_CLK100M_ENET_P — PCIE_REFCLK_P
PCIE_CLK100M_ENET_N — PCIE_REFCLK_N

ENET_RESET_LOGIC_R_L — PERST* (IPD)
ENET_CLKREQ_FET_L — CLKREQ* (OD)
ENET_WAKE_R_L — WAKE* (OD)
ENET_LOW_PWR — LOW_PWR (IPD)
ENET_SMB_CLK — SMB_CLK
ENET_SMB_DATA — SMD_DATA (IPD ENETM)

ENET_SCLK — SCLK
ENET_MISO — SI/LINKLED*
ENET_MOSI — SO
ENET_CS_L — CS*

TP_ENET_SPD100LED_L — SPD100LED*/SERIAL_DO (OD)
ENET_TRAFFICLED_L — TRAFFICLED*/SERIAL_DI (OD)

ENET_CLK25M_XTALI — XTALI
ENET_CLK25M_XTALO — XTALO
ENET_RDAC — RDAC

THRM_PAD 69

GPIO_0 — NC
GPIO_1/CR_BUS_PWR
RE*/GPIO_2 — ENET_MEDIA_SENSE

NOTE "IPx" == Programmable pull up/down
(IPx ENET) SD_DETECT/WE*
SD DETECT can only be used active low due to errata
(IPU ENET) CR_CMD/CLE
CR_CLK/RY_BY*
CR_DATA0
CR_DATA1
CR_DATA2
CR_DATA3
CR_DATA4
CR_DATA5
CR_DATA6
CR_DATA7
(IPU-ENET)
(IPU ENET) CE*/MS_INS*
(IPU ENET) CR_LED/ALE
(IPU ENET) CR_WP*/XD_WP*
(NO IPU OR IPD ENET) XD_DETECT

ENET_SD_DETECT_L — R3960 0 — SDCONN_DETECT_L
ENET_SD_CMD — R3961 33 — SDCONN_CMD
ENET_SD_CLK — R3979 33 — SDCONN_CLK
ENET_CR_DATA<0> — R3971 33 — SDCONN_DATA<0>
ENET_CR_DATA<1> — R3972 33 — SDCONN_DATA<1>
ENET_CR_DATA<2> — R3973 33 — SDCONN_DATA<2>
ENET_CR_DATA<3> — R3974 33 — SDCONN_DATA<3>
ENET_CR_DATA<4> — R3975 33 — SDCONN_DATA<4>
ENET_CR_DATA<5> — R3976 33 — SDCONN_DATA<5>
ENET_CR_DATA<6> — R3977 33 — SDCONN_DATA<6>
ENET_CR_DATA<7> — R3978 33 — SDCONN_DATA<7>
(all DEVELOPMENT, 5% 1/16W MF LF 402)
PLACEMENT NOTE=PLACE R3960 NEAR U3900
PLACEMENT NOTE=PLACE R3961 NEAR U3900
PLACEMENT NOTE=PLACE R3979 NEAR U3900
PLACEMENT NOTE=PLACE R3971 NEAR U3900
PLACEMENT NOTE=PLACE R3972 NEAR U3900
PLACEMENT NOTE=PLACE R3973 NEAR U3900
PLACEMENT NOTE=PLACE R3974 NEAR U3900
PLACEMENT NOTE=PLACE R3975 NEAR U3900
PLACEMENT NOTE=PLACE R3976 NEAR U3900
PLACEMENT NOTE=PLACE R3977 NEAR U3900
PLACEMENT NOTE=PLACE R3978 NEAR U3900

CE*/MS_INS* — NC_ENET_CE_L_MS_INS_L — NO_TEST=TRUE
CR_LED/ALE — ENET_CR_PWREN
CR_WP*/XD_WP* — SDCONN_WP
XD_DETECT — ENET_SR_DISABLE — R3980 1K — =PP3V3_S3_ENET_PHY_FET
R3981 1K

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

ENET SR IS ENABLED IF FLOATING. (See note)

ENET supports both active-levels for WP.

ENET_CR Signals

BCM requests SD CR[0:7], CMD, CLK termination.

ENET_SR_DISABLE

If ENET switching regulator is used, this pin can float (alias to TP_). If not used, must be pulled to 3.3V ENET via 1K resistor (not provided on this page).

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Avoids need for EFI to program at startup. (Required ROM size 1 Mbit)

=PP3V3_S3_ENET_PHY_FET

R3993 4.7K 5% 1/16W MF LF 402
R3992 4.7K 5% 1/16W MF LF 402
R3904 0 5% 1/16W MF LF 402

U3990 AT45DB021D SOIC-8S1 OMIT_TABLE
VCC, SCK, CS*, WP*, RESET*, SI, SO, GND

C3990 0.1UF 10% 16V X7R CERM 402

ENET_SCLK — ENET_SCLK_R
ENET_CS_L
ENET_SWP_L
ENET_SRESET_L
ENET_MOSI
ENET_MISO

NOSTUFF: R3990 4.7K 5% 1/16W MF LF 402; R3997 4.7K 5% 1/16W MF LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC_MASTER=K62_MARK SYNC_DATE=01/09/2013
PAGE TITLE
ETHERNET PHY (CAESAR IV)
Apple Inc.
DRAWING NUMBER 051-8442
SIZE D
REVISION 10.1.0
BRANCH
PAGE 39 OF 110
SHEET 37 OF 101

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THIS PAGE IS DIFFERENT BETWEEN K60 AND K62.

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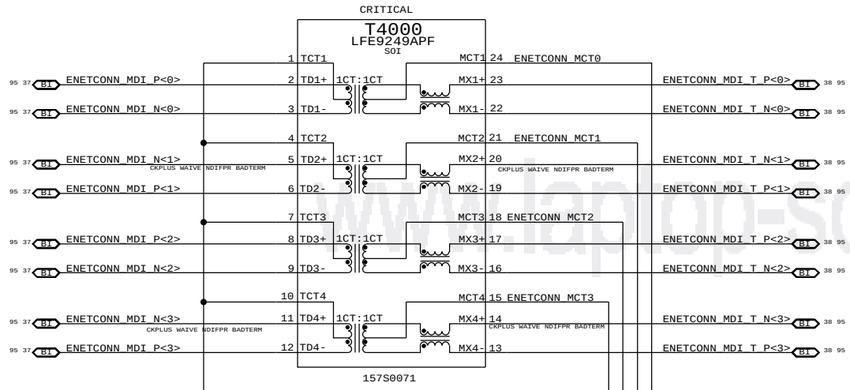
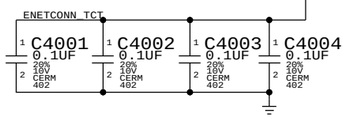
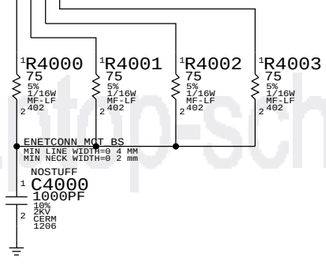


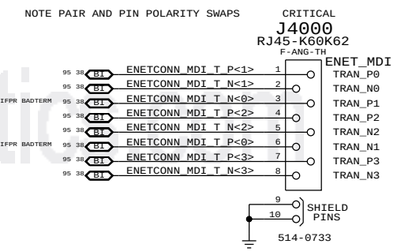


PLACE ONE CAP PER TCT PIN

NOTE: Check with PHY and Magnetics MFR to determine what to do with center taps.



NOTE: BOB SMITH TERMINATION FOR EMC.



SYNC MASTER=K62 MARK SYNC DATE=01/09/2011

PAGE TITLE: Ethernet Connector

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

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7 mA I/O

C4120 1UF 10% 6.3V CERM 402
C4121 1UF 10% 6.3V CERM 402
C4122 1UF 10% 6.3V CERM 402
C4123 1UF 10% 6.3V CERM 402
C4124 1UF 10% 6.3V CERM 402

=PP3V3_S0_FWPHY 6 39 40 41
138 mA

L4130 120-OHM-0.3A-EMI 0402 LF

114 mA FireWire PHY

C4130 1UF 10% 6.3V CERM 402
C4131 1UF 10% 6.3V CERM 402
C4132 1UF 10% 6.3V CERM 402

98 PP3V3_FW_FWPHY_VDDA
MIN LINE WIDTH=0.4 MM
MIN NECK WIDTH=0.2 MM
VOLTAGE=3.3V

K18 has 0.475-ohm upstream of L4110

L4110 120-OHM-0.3A-EMI 0402 LF

40 =PP1V0_S0_FWPHY
135 mA

98 PP1V0_FW_FWPHY_AVDD
MIN LINE WIDTH=0.4 MM
MIN NECK WIDTH=0.2 MM
VOLTAGE=1.0V

25 mA PCIe SerDes

C4110 1UF 10% 6.3V CERM 402
C4111 1UF 10% 6.3V CERM 402

17 mA PCIe SerDes

C4135 1UF 10% 6.3V CERM 402
C4136 1UF 10% 6.3V CERM 402

98 PP3V3_FW_FWPHY_VP25
MIN LINE WIDTH=0.4 MM
MIN NECK WIDTH=0.2 MM
VOLTAGE=3.3V

L4135 120-OHM-0.3A-EMI 0402 LF

110 mA Digital Core

C4100 1UF 10% 6.3V CERM 402
C4101 1UF 10% 6.3V CERM 402
C4102 1UF 10% 6.3V CERM 402
C4103 1UF 10% 6.3V CERM 402
C4104 1UF 10% 6.3V CERM 402
C4105 1UF 10% 6.3V CERM 402
C4106 1UF 10% 6.3V CERM 402

0 mA VReg PWR

C4141 0.1UF 20% 10V CERM 402
C4140 1UF 10% 6.3V CERM 402

APN: 338S0753 ->

OMIT
CRITICAL
U4100
FW643
BGA

VDD10 VDD33 VDDH VP VP25 VREG_PWR

NC ATBUSB B13
NC ATBUSH A13
NC ATBUSN A11

40 LN FW_PHY_DS0 → DS0 (IPD) NT-19 F12
40 LN FW_PHY_DS1 → DS1 (IPD) NT-20 E12
40 LN FW_PHY_DS2 → DS2 (IPD) NT-21 E13

40 B1 FW_P0_TPA_N → TPA0N B8
40 B1 FW_P0_TPA_P → TPA0P A8
95 40 B1 FW_P1_TPA_N → TPA1N B5
95 40 B1 FW_P1_TPA_P → TPA1P A5
95 40 B1 FW_P2_TPA_N → TPA2N B3
95 40 B1 FW_P2_TPA_P → TPA2P A3
40 B1 FW_P0_TPB_N → TPB0N B9
40 B1 FW_P0_TPB_P → TPB0P A9
95 40 B1 FW_P1_TPB_N → TPB1N B6
95 40 B1 FW_P1_TPB_P → TPB1P A6
95 40 B1 FW_P2_TPB_N → TPB2N B4
95 40 B1 FW_P2_TPB_P → TPB2P A4

40 B1 FW_P0_TPBIAS → TPBIAS0 B7
40 B1 FW_P1_TPBIAS → TPBIAS1 C3
40 B1 FW_P2_TPBIAS → TPBIAS2 A2

FW643_R0 → R0 B11
FW643_TPCPS → TPCPS B10

98 41 PPVP_FW_PHY_CPS
PLACEMENT NOTE=Place close to U4100 B10
R4160 200K 1% 1/16W MF LF 402

TP_FW643_NAND_TREE → NAND_TREE NT-OUT K1
FW643_REXT → REXT L8
95 FW_CLK24P576M_XO_R → XO F13
95 FW_CLK24P576M_XI → XI NT-9 G13

C4150 22PF 5% 50V CERM 402
95 FW_CLK24P576M_XO
CRITICAL
Y4150 24.576M HC49 USMD
C4151 22PF 5% 50V CERM 402
K18 has a different crystal
R4150 412 1% 1/16W MF LF 402

R4161 2.94K 1% 1/16W MF LF 402
R4170 191 1% 1/16W MF LF 402

TP_FW643_SE → SE (IPD) M13
TP_FW643_SM → SM (IPD) N13
TP_FW643_MODE_A → MODE_A (IPD) NT-18 J2
TP_FW643_CE → CE (IPD) L13
TP_FW643_FW620_L → FW620*(IPU) D12
TP_FW643_JASI_EN → JASI_EN (IPD) NT-11 D1
TP_FW643_AVREG → AVREG A10
TP_FW643_VBUF → VBUF H13
FW643_PU_RST_L → FW_RESET* (IPU) NT-8 K13
40 FW643_OCR10_CTL → OCR_CTL_V10 J12
NC OCR_CTL_V12 (Reserved) J13

NOTE: NT-xx notes show NAND tree order.

External power-on reset (IPU 100K):
Per LSI, R4162 and C4162 can be NOSTUFF ->

R4162 470K 5% 1/16W MF LF 402
C4162 0.33UF 10% 6.3V CERM X5R 402

VSS VREG_VSS

PCI EXPRESS PHY

PCIE_RXD0N N8 → 93 PCIE_FW_R2D_N
PCIE_RXD0P N7 → 93 PCIE_FW_R2D_P
PCIE_TXD0N N5 → 93 PCIE_FW_D2R_C_N
PCIE_TXD0P N6 → 93 PCIE_FW_D2R_C_P

C4170 0.1UF 10% 16V X5R 402 PCIE_FW_R2D_C_N IN 18 93
C4171 0.1UF 10% 16V X5R 402 PCIE_FW_R2D_C_P IN 18 93
C4175 0.1UF 10% 16V X5R 402 PCIE_FW_D2R_N OUT 18 93
C4176 0.1UF 10% 16V X5R 402 PCIE_FW_D2R_P OUT 18 93

PLACEMENT NOTE=Place C4170 close to U1800
PLACEMENT NOTE=Place C4171 close to U1800
PLACEMENT NOTE=PLACE C4175 CLOSE TO U4100
PLACEMENT NOTE=PLACE C4176 CLOSE TO U4100

REFCLKN N9 → PCIE_CLK100M_FW_N IN 18 93
REFCLKP N10 → PCIE_CLK100M_FW_P IN 18 93

1394 PHY

TEST CONTROLLER

NT-4 (IPU) TCK M4 → TP_FW643_TCK
NT-3 (IPU) TDI N2 → TP_FW643_TDI
(IPU) TDO M1 → TP_FW643_TDO
NT-1 (IPU) TMS M3 → TP_FW643_TMS
NT-2 (IPU) TRST* N1 → FW643_TRST_L

POWER MANAGEMENT
FIXME!!! TYPO IN SYMBOL REGCTL
FIXME!!! TYPO IN SYMBOL VAUX ENABLE

NT-10 (IPD) NT-12 (IPD) WAKE* C2 → FW_PME_L OUT 15 21 100
REGCLT D13 → FW643_REGCTL
VAUX_DETECT E1 → FW643_VAUX_DETECT
NT-13 VAUX_DISABLE D2 → TP_FW643_VAUX_ENABLE
(OD) CLKREQN L2 → FW_CLKREQ_L OUT 15 100

=PP3V3_S0_FWPHY 6 39 40 41
NOSTUFF R4165 10K 5% 1/16W MF LF 402
R4166 10K 5% 1/16W MF LF 402
R4164 10K 5% 1/16W MF LF 402

SCIF

NT-16 (IPD) SCIFCLK G2 → TP_FW643_SCIFCLK
NT-14 (IPD) SCIFDAIN G1 → TP_FW643_SCIFDAIN
NT-17 SCIFDOUT H1 → TP_FW643_SCIFDOUT
NT-15 (IPD) SCIFMC F2 → TP_FW643_SCIFMC

SERIAL EEPROM CONTROLLER

NT-7 SCL N12 → FW643_SCL
NT-6 SDA M11 → TP_FW643_SDA

CHIP RESET

NT-5 PERST* N4 → FW_RESET_L IN 27 100

R4163 10K 5% 1/16W MF LF 402

SYNC_MASTER=K62_ROSITA SYNC_DATE=01/09/2011

PAGE TITLE
FireWire LLC/PHY (FW643)

Apple Inc.

DRAWING NUMBER 051-8442 SIZE D
REVISION 10.1.0
BRANCH
PAGE 41 OF 110
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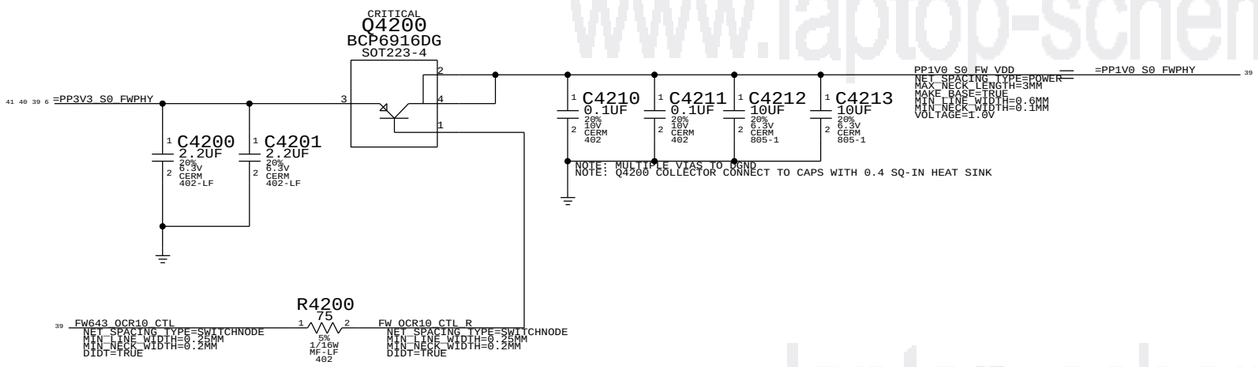
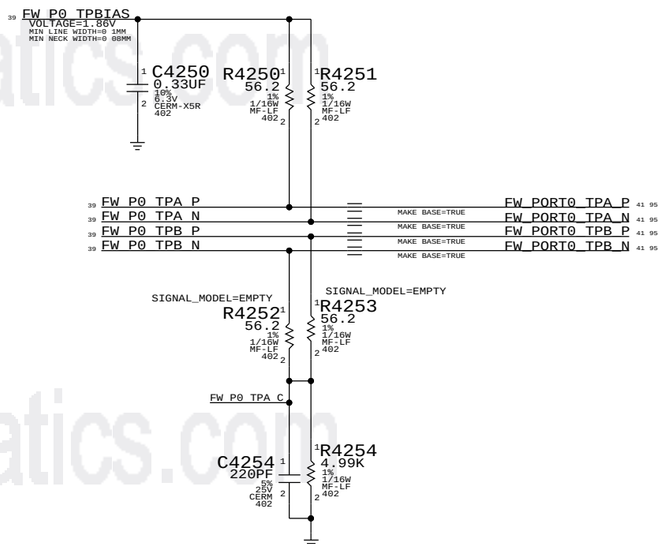
FW643 1.0V GENERATION

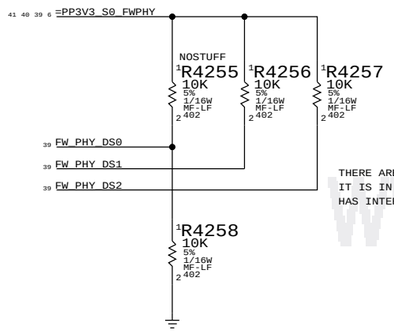


Termination

Place close to FireWire PHY



1394 PHY DATA/STROBE OPTIONS



THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE, FW643 HAS INTERNAL 100K PULL-DOWNS, ONLY PULL-UPS NECESSARY.

2ND & 3RD TPA/TPB PAIR UNUSED

FW_P1_TPBIAS		NC_FW_PORT1_TPBIAS
FW_P1_TPA_P		NC_FW_PORT1_TPA_P
FW_P1_TPA_N		NC_FW_PORT1_TPA_N
FW_P1_TPB_P		NC_FW_PORT1_TPB_P
FW_P1_TPB_N		NC_FW_PORT1_TPB_N
FW_P2_TPBIAS		NC_FW_PORT2_TPBIAS
FW_P2_TPA_P		NC_FW_PORT2_TPA_P
FW_P2_TPA_N		NC_FW_PORT2_TPA_N
FW_P2_TPB_P		NC_FW_PORT2_TPB_P
FW_P2_TPB_N		NC_FW_PORT2_TPB_N

MAKE_BASE=TRUE
NO TEST=TRUE

NOTE: AGERE'S RECOMMENDATION FOR UNUSED PORTS

SYNC_MASTER=K62_ROSITA SYNC_DATE=01/09/2011

PAGE TITLE: FireWire: 1394B MISC

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

REVISION: 10.1.0

BRANCH:

PAGE: 42 OF 110

SHEET: 40 OF 101

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12 VOLTS
14 WATTS MAX PER PORT

POUR COPPER TO SINK HEAT

CRITICAL
Q4350
FDC610PZ
SSOT6

=PP12V_S0_FW

R4351 1K 5% 1/16W MF-LF 402

NOSTUFF
C4351 0.001UF 20% 50V CERM 402

PP12V_S0_VG_OK
MIN LINE WIDTH=1 7MM
MIN NECK WIDTH=0 5MM
VOLTAGE=12V

FWPWR_ON_L

R4355 1K 5% 1/16W MF-LF 402

FWPWR_EN_L

Q4351
2N7002
SOT23-HF

INRUSH RESETABLE PTC

CRITICAL
F4301
0.3AMP-60V
SMD030F-SM

R4300 0.33 5% 1W MF 2512

P12V_FW_R
MIN LINE WIDTH=1 7MM
MIN NECK WIDTH=0 5MM
VOLTAGE=12V

POUR COPPER TO SINK HEAT

CRITICAL
Q4300
FDC610PZ
SSOT6

Q4301
MMBT2907AXG
60V-600MA
SOT23

5.1V
D4301
MMBZ5231BXG
SOT23

R4352 51.1K 1% 1/16W MF-LF 402

FW_CURRENT_LIMIT

R4301 10K 5% 1/16W MF-LF 402

FW_TURN_ON_V

R4302 15K 5% 1/16W MF-LF 603

R4303 20K 5% 1/16W MF-LF 402

FW_CURRENT_LIMIT_Q

Q4302
MMBT2222A7F
SOT23

FW_FET_LINEAR_LIMIT_OUT
FW_FET_LINEAR_LIMIT_IN

PLACE CLOSE TO COMPARATOR

C4302 0.01UF 20% 16V CERM 402

R4307 20K 5% 1/16W MF-LF 402

PLACEMENT NOTE=PLACE CLOSE TO F4300

XW4300
PPVP_FW_PHY_CPS
MIN LINE WIDTH=0 5MM
MIN NECK WIDTH=0 25MM
VOLTAGE=12V

P12V_FW_CL
MIN LINE WIDTH=1 7MM
MIN NECK WIDTH=0 5MM
VOLTAGE=12V

CRITICAL
D4300
SM
CRS08-1.5A-30V

P12V_FW_D
MIN LINE WIDTH=1 7MM
MIN NECK WIDTH=0 5MM
VOLTAGE=12V

NOSTUFF
D4305
MMBD914XG
SOT23

CRITICAL
F4300
3AMP-32V
603

FAST NON-RESETABLE FUSE
THIS FUSE WILL NOT BLOW
IT IS HERE FOR SAFETY ONLY

FW_PORT0_VP_F
MIN LINE WIDTH=1 7MM
MIN NECK WIDTH=0 5MM
VOLTAGE=12V

CRITICAL
L4300
FERR-250-OHM
SM

C4300 0.01UF 10% 50V X7R 603-1

FW_PORT0_VP
MIN LINE WIDTH=1 7MM
MIN NECK WIDTH=0 5MM
VOLTAGE=12V

SHOULD BE DONE AS A POWER STRIP(SUBPLANE)

PORT 0
1394B

CRITICAL
J4300
FWB-PL-K60-K62
F-ANG-TH

FW_PORT0_TPB_N
FW_PORT0_TPB_P
FW_PORT0_TPA_N
FW_PORT0_TPA_P
NO_TEST=TRUE

FW_PORT0_TPA_R

NC
SHIELD PINS
514-0769

NOSTUFF
C4332 0.001UF 10% 50V CERM 402

AREF needs to be isolated from all
local grounds per 1394b spec
When a billingual device is connected to a
beta-only device, there is no DC path
between them (to avoid ground offset issue)

BREF should be hard-connected to logic
ground for speed signaling and connection

R4335 1M 1% 1/16W MF-LF 402

C4335 0.1UF 10% 50V X7R 603-1

R4304 100K 5% 1/16W MF-LF 402

FW_FET_LINEAR_LIMIT_FB

D4302
BAS40XG
SOT23

C4304 0.1UF 10% 16V X7R-CERM 402

V+
U4300
LM393
SOI-HF
NC
GND

R4305 100K 5% 1/16W MF-LF 402

FW_CURRENT_LIMIT
FW_CURRENT_LIMIT_R
FW_CURRENT_LIMIT_RD
FW_FET_LINEAR_LIMIT_IN
FW_FET_LINEAR_LIMIT_OUT

5.1V
D4303
SOT23
MMBZ5231BXG

PLACE CLOSE TO COMPARATOR

C4305 2.2UF 10% 16V X5R 603

R4306 200K 5% 1/16W MF-LF 402

ACTIVE "LATE VG" + ESD PROTECTION

=PP3V3_S0_FWPHY

C4350 0.1UF 10% 10V X7R-CERM 402

PLACEMENT NOTE=PLACE U4350 CLOSE TO J4300

U4350
TPD4S1394
LLP
CRITICAL

TP_FW_LATEVG_VCLMP
FWPWR_EN

NOSTUFF
R4350 100K 5% 1/16W MF-LF 402

FW_PORT0_TPB_P
FW_PORT0_TPB_N
FW_PORT0_TPA_P
FW_PORT0_TPA_N

SYNC MASTER=K62 ROSITA	SYNC DATE=01/09/2011
PAGE TITLE: FIREWIRE CONNECTOR	
Apple Inc.	DRAWING NUMBER: 051-8442 SIZE: D
	REVISION: 10.1.0
	BRANCH:
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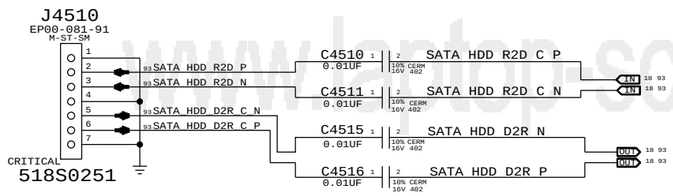
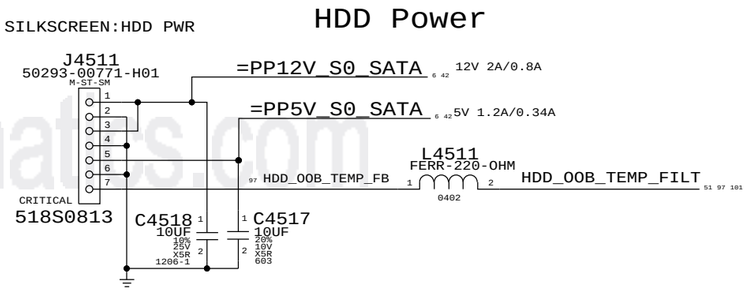
SATA PORT A0 FOR HDD

SILKSCREEN:SATA0



HDD Power

SILKSCREEN:HDD PWR



BOMOPTION OPTIONS FOR SATA PORT A1 AND A2

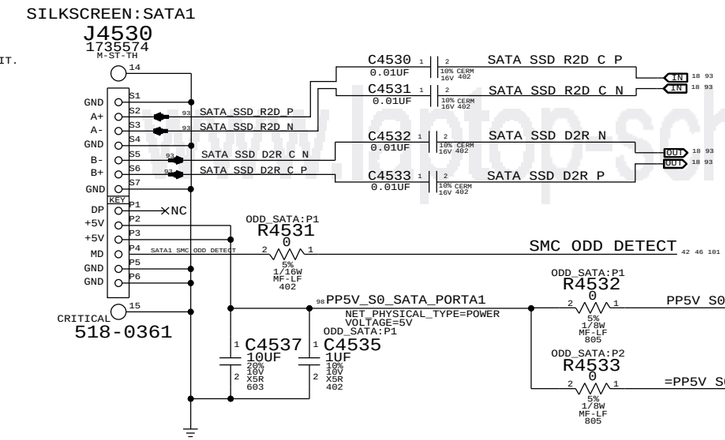
A1	A2	ODD SATA:P1	ODD SATA:P2
SSD	ODD		X
ODD		X	

USE OF PORT A2 FOR SSD IS NOT INTENDED VIA BOMOPTION THOUGH MLB SUPPORTS IT.

5V (SSD) 1.4A/0.8A/0.03A
5V (ODD) 1.5A/1A/0.14A

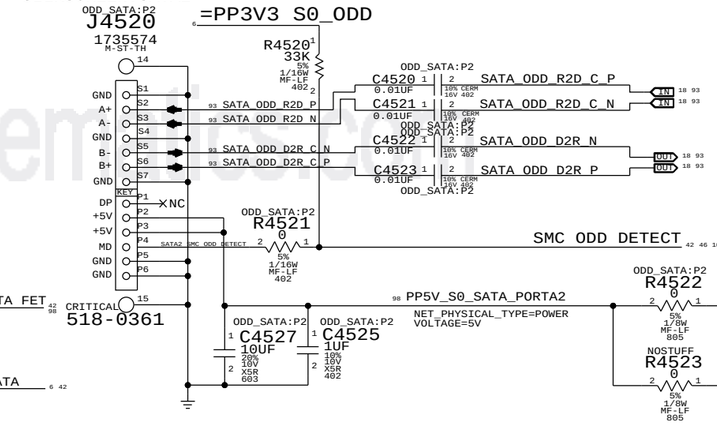
SATA PORT A1 FOR SSD/ODD

SILKSCREEN:SATA1

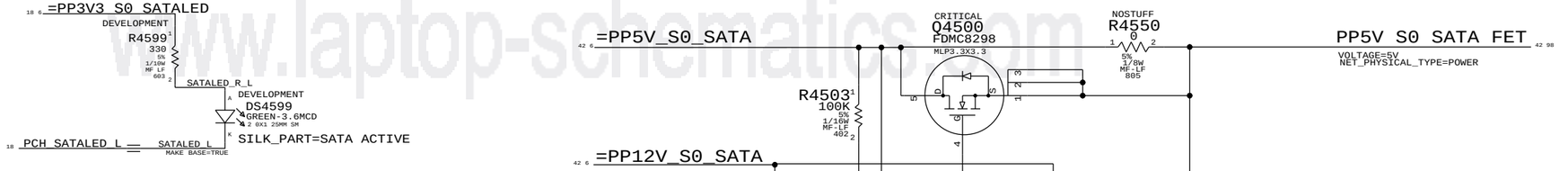


SATA PORT A2 FOR ODD

SILKSCREEN:SATA2



SATA Activity LED



SYNC_MASTER=K62_JERRY	SYNC_DATE=01/09/2011
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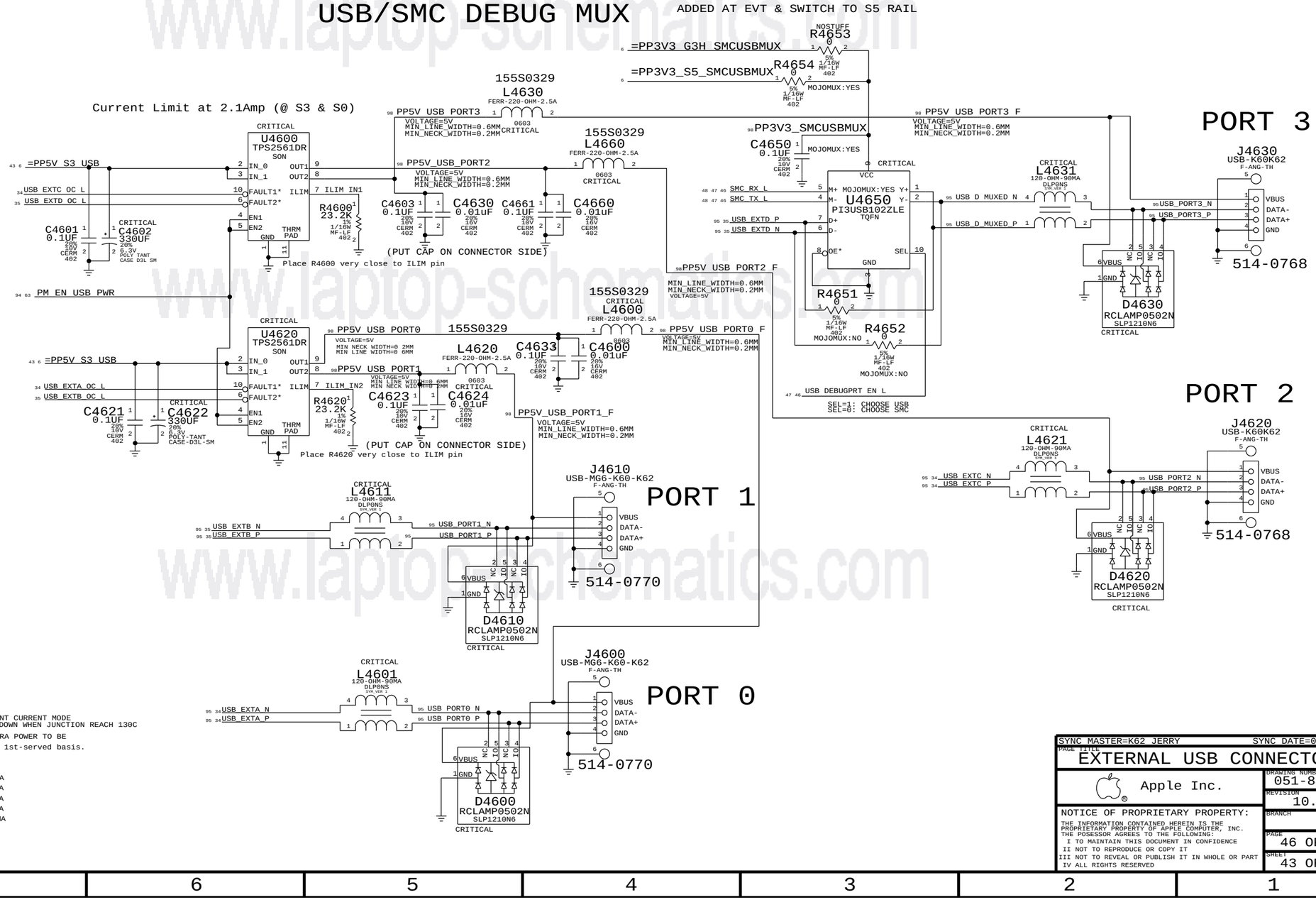
USB/SMC DEBUG MUX

ADDED AT EVT & SWITCH TO S5 RAIL



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USB PORT POWER:

EACH PORT IS HARDWARE Capable of :

STATE	MAX	MIN (WITHIN THE TOLERANCE)
S0, S3	2.7A	2.1A -- PER PORT

WHEN CURRENT HITS LIMIT, TPS2561 BECOME CONSTANT CURRENT MODE
AND STAY AT THE LIMIT LEVEL UNTIL THERMAL SHUTDOWN WHEN JUNCTION REACH 130C

SOFTWARE WILL ALOW 500MA/PORT, PLUS 2700MA EXTRA POWER TO BE distributed to approved devices on a 1st-come, 1st-served basis.

EXAMPLE:
- Port 1 - iPad fast charging = 2100mA
- Port 2 - Wired Keyboard = 1100mA
- Port 3 - iPhone fast charging = 1000mA
- PORT 4 - USB 2.0 500MA = 500MA

TOTAL: 4700MA

SYNC_MASTER=K62_JERRY SYNC_DATE=01/09/2011

PAGE TITLE: EXTERNAL USB CONNECTORS

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REVISION 10.1.0
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PAGE 46 OF 110
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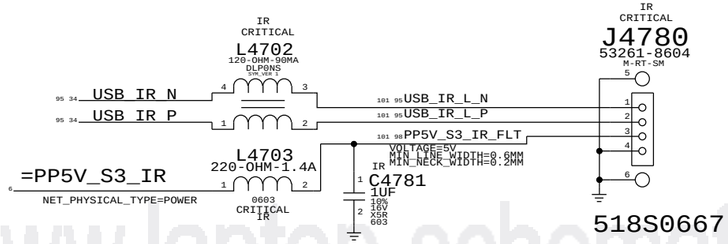
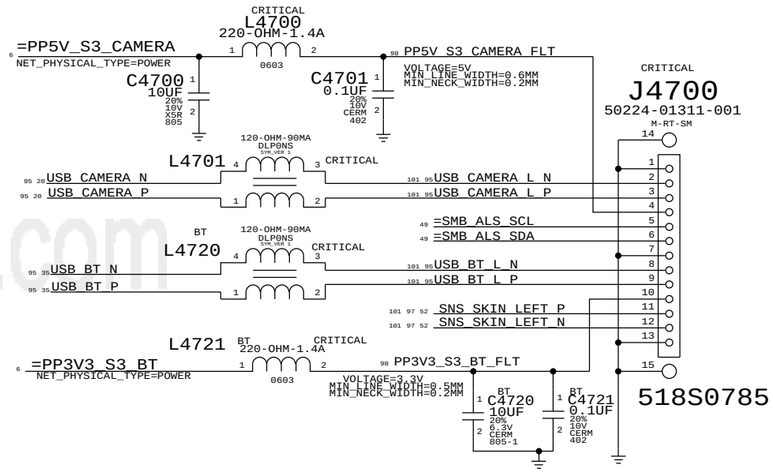
IR RECEIVER CONNECTOR

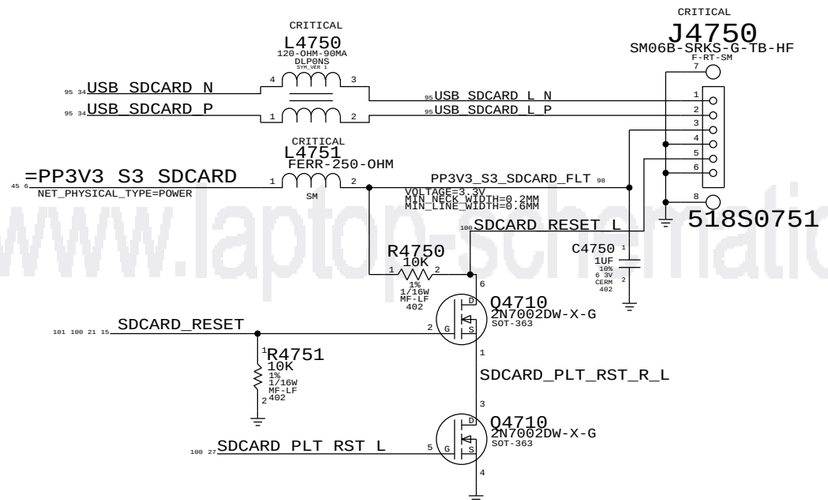


CAMERA/ALS & BLUETOOTH (K37A) CONNECTOR



Skin Temp sense at upper Left Screen corner

SD Card Reader Board (Lazarus)



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SYNC_MASTER=K62_JERRY SYNC_DATE=01/09/2011

PAGE TITLE

Internal USB Connections

Apple Inc.

DRAWING NUMBER	051-8442
SIZE	D
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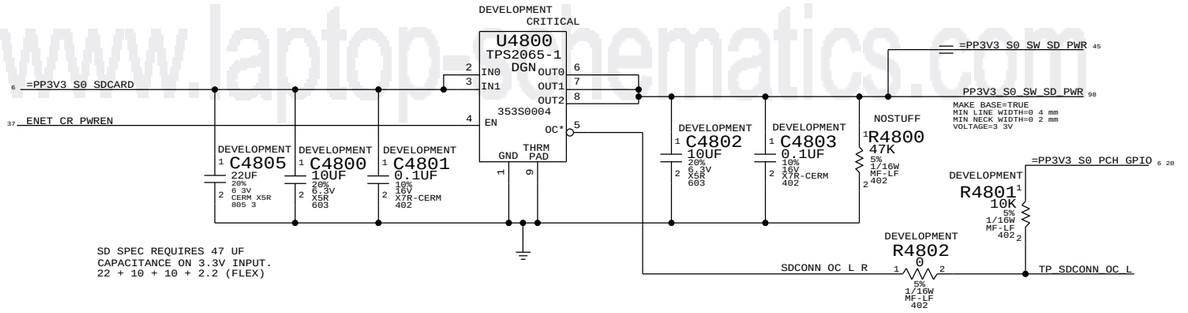
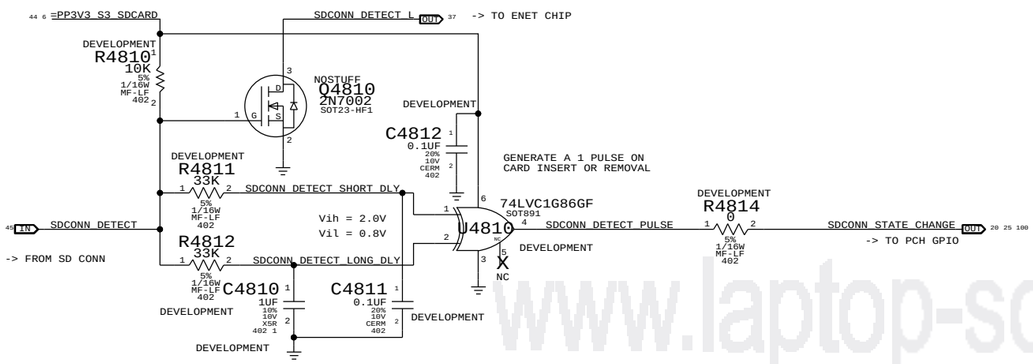
SD CARD 3.3V OVERCURRENT PROTECTION CHIP WITH ACTIVE LOAD DISCHARGE

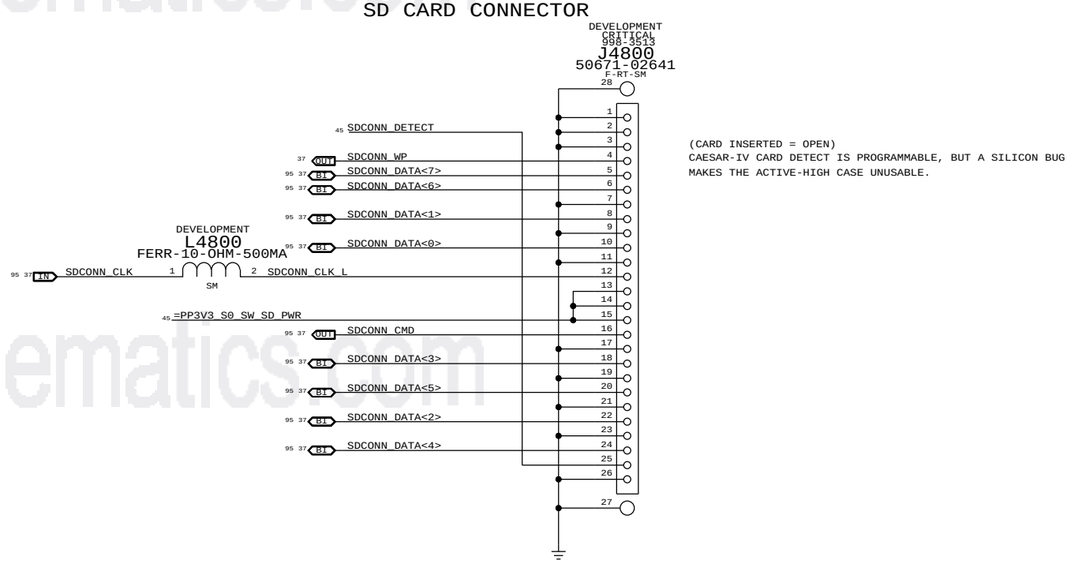
TPS2065-1 (1.0A LIMIT) HAS ACTIVE LOAD DISCHARGE SO R4800 IS NOSTUFF.



SDCONN DETECT DEBOUNCE, INVERSION, AND DETECT-CHANGED PCH GPIO CIRCUIT



SD CARD CONNECTOR



SYNC MASTER=K62 MARK SYNC DATE=01/09/2011

PAGE TITLE

SD READER CONNECTOR

Apple Inc.

DRAWING NUMBER 051-8442 SIZE D

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NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

338S0878

U4900
H8S2117
LFBGA
(1 OF 4)
OMIT

47 OUT	SMC_EXCARD_PWR_EN	B12	P10	
47 OUT	SMC_RSTGATE_L	C13	P11	
100 64 IN	ALL_SYS_PWRGD_SMC	A15	P12	
100 64 IN	RSMRST_PWRGD	B14	P13	
	NC	B15	P14	
100 27 OUT	PM_RSMRST_L	C14	P15	
47 OUT	CPUIMVP_VR_ON	D12	P16	
100 25 19 OUT	PM_PWRBTN_L	C15	P17	
K62 NEW:NOT USE	NC	D13	P20	
	NC	D14	P21	
	NC	D15	P22	
	NC	E12	P23	
K62 NEW:NOT USE	NC	E14	P24	
	NC	E15	P25	
K62 NEW:NOT USE	NC	E13	P26	
	NC	F14	P27	
94 48 18 BI	LPC_AD<0>	D9	P30	
94 48 18 BI	LPC_AD<1>	C9	P31	
94 48 18 BI	LPC_AD<2>	A9	P32	
94 48 18 BI	LPC_AD<3>	B9	P33	
94 48 18 IN	LPC_FRAME_L	D8	P34	
100 27 IN	SMC_LRESET_L	C8	P35	
94 27 IN	LPC_CLK33M_SMC	A8	P36	
48 18 BI	LPC_SERIRQ	D7	P37	
	NC	A5	P40	
K62 P1 NOT USED, WAS OOB_TEMP	NC	B5	P41	
49 BI	SMB_MGMT_DATA	D5	P42 (OC)	
47 OUT	SMS_ONOFF_L	C3	P43	
	NC	B1	P44	
	NC	C2	P45	
47 OUT	SMC_GFX_THROTTLE_L	D3	P46	
	NC	C1	P47	
48 47 46 43 OUT	SMC_TX_L	G1	P50	
48 47 46 43 IN	SMC_RX_L	G4	P51	
49 BI	SMB_0_S0_CLK	F2	P52 (OC)	

P60	L13	SMC_PM_G2_EN	OUT 75 100	
P61	L14	NC		
P62	L15	NC		
P63	K12	NC		
P64	K13	SMC_ADAPTER_EN	OUT 19 47 100	
P65	K14	NC		
P66	J12	SMC_PROCHOT_3_3_L	IN 47 100	
P67	J13	SMC_BIL_BUTTON_L	IN 47	
P70	N12	SMC_VCORE_ISENSE	IN 50 97 (IMON)	
P71	R13	SMC_VCORE_VSENSE	IN 50 97 (IMON)	
P72	P13	SMC_CPU_1V5_ISENSE	IN 50 97	
P73	R14	SMC_CPU_1V5_VSENSE	IN 50 97	
P74	P14	SMC_VCCSA_ISENSE	IN 50 97	
P75	R15	SMC_VCCSA_VSENSE	IN 50 97	
P76	N13	SMC_VAXG_ISENSE	IN 50 97 (IMON)	
P77	P15	SMC_VAXG_VSENSE	IN 50 97 (IMON)	
P80	C7	SMC_WAKE_SCI_L	OUT 15 18 21 100	PROTO-3, Change back to WAKE_SCI_L
P81	A7	NC		
P82	B7	PM_CLKRUN_L	OUT 15 19 48 100	
P83	D6	LPC_PWRDWN_L	IN 19 48 100	
P84	C6	SMC_TX_L	OUT 43 46 47 48	
P85	A6	SMC_RX_L	IN 43 46 47 48	
P86	B6	(OC) SMB_MGMT_CLK	BI 49	
P90	K4	SMC_ONOFF_L	IN 47 100	
P91	J2	SMC_BC_ACOK	IN 47	
P92	J1	NC		
P93	J3	PM_SLP_S3_L	IN 5 19 26 32 36 47 63 100	
P94	J4	PM_SLP_S4_L	IN 5 19 32 47 63 100	K60 New Change
P95	H2	PM_SLP_S5_L	IN 5 19 47 63 100	K60 New Change
P96	H1	PM_CLK32K_SUSCLK	IN 9 94 100	
P97	G2	(OC) SMB_0_S0_DATA	BI 49	

98 47 46 PP3V3_G3H_AVREF_SMC Peak/Ave/Standby = 2mA/1mA/5uA
47 46 6 =PP3V3_G3H_SMC Peak/Ave/Sleep/Standby = 40mA/25mA/20mA/50uA

C4902 22UF 20% 6.3V CERM 805
C4903 0.1UF 20% 10V CERM 402
C4904 0.1UF 20% 10V CERM 402
C4905 0.1UF 20% 10V CERM 402
C4906 0.1UF 20% 10V CERM 402

PLACEMENT NOTE=Place C4907 close to U4900 pin 13

R4999 4.7 5% 1/16W MF LF 402
Peak/Ave/Standby= 2mA/1mA/5uA
98 46 PP3V3_G3H_SMC_AVCC
MIN LINE WIDTH=0 25 MM
MIN NECK WIDTH=0 20 MM
VOLTAGE=3 4V

C4907 0.47UF 10% 6.3V CERM X5R 402
C4920 0.1UF 20% 10V CERM 402

PLACEMENT NOTE=Place R4999 close to U4900 pin 76
PLACEMENT NOTE=Place C4920 close to U4900 pin 76

U4900
H8S2117
LFBGA
(3 OF 4)
OMIT

100 48 47 IN	SMC_RESET_L	E3	RES*
97 47	SMC_XTAL	A2	XTAL
97 47	SMC_EXTAL	B2	EXTAL

R4909 10K 5% 1/16W MF LF 402
R4901 10K 5% 1/16W MF LF 402

MD1	E2	SMC_MD1	IN 48
MD2	K1	SMC_KBC_MDE	
NMI	F4	SMC_NMI	IN 48
ETRST*	L1	SMC_TRST_L	IN 48
AVSS	R12	NOSTUFF	

R4902 10K 5% 1/16W MF LF 402
R4998 10K 5% 1/16W MF LF 402
R4903 0 5% 1/16W MF LF 402

XW4900 SM

GND_SMC_AVSS 46 47 50 97

98 47 46 PP3V3_G3H_AVREF_SMC
47 46 6 =PP3V3_G3H_SMC
98 46 PP3V3_G3H_SMC_AVCC

U4900
H8S2117
LFBGA
(4 OF 4)
OMIT

	E4	PJ0	C5	NC
	N4	PJ1	B8	NC
	M9	PJ2	C10	NC
NC	M12	PJ3	C12	NC
	M13	PJ4	A14	NC
	L12	PJ5	F15	NC
	A3	PJ6	J14	NC
		PJ7	K15	NC
		PI0	N8	NC
		PI1	N7	NC
		PI2	M5	NC
		PI3	L3	NC
		PI4	K3	NC
		PI5	H3	NC
		PI6	H4	NC
		PI7	G3	NC

97 50 47 46 GND_SMC_AVSS

U4900
H8S2117
LFBGA
(2 OF 4)
OMIT

K62 NEW:NOT USE,PULLED UP	47 IN SMC_PA0	R3	PA0	
	100 18 OUT SPI_DESCRIPTOR_OVERRIDE_L (OC)	P3	PA1	
	100 27 25 19 OUT PM_SYSRST_L (OC)	R2	PA2	
	47 43 OUT USB_DEBUGPRT_EN_L (OC)	N3	PA3	
	47 IN MEM_EVENT_A_L (OC)	R1	PA4	
	47 IN MEM_EVENT_B_L (OC)	N2	PA5	
	47 BI SYS_ONEWIRE (OC)	M4	PA6	
	100 19 15 OUT PM_BATLOW_L (OC)	N1	PA7	
	NC	B10	PB0	
PROTO-3:back to K75F	100 47 23 OUT SMC_RUNTIME_SCI_L	A10	PB1	
	101 42 IN SMC_ODD_DETECT	D10	PB2	
K62 NEW:NOT USE,PULLED UP	47 IN (See below) SMC_PB3	A11	PB3	
	97 51 IN SMC_HDD_OOB_TEMP	B11	PB4	
	NC	C11	PB5	
K62 NEW:NOT USE,PULLED UP	IN SMC_PB6	A12	PB6	
	47 IN SMC_GFX_OVERTEMP_L	D11	PB7	
	53 OUT SMC_FAN_0_CTL	G14	PC0	
	53 OUT SMC_FAN_1_CTL	G15	PC1	
	NC	G13	PC2	
	54 OUT SMC_FAN_3_CTL	G12	PC3	
	53 IN SMC_FAN_0_TACH	H14	PC4	
	53 IN SMC_FAN_1_TACH	H15	PC5	
	NC	H13	PC6	
	54 IN SMC_FAN_3_TACH	H12	PC7	
(IMON)	97 50 IN SMC_1V05_ISENSE	M11	PD0	
(IMON)	97 50 IN SMC_1V05_VSENSE	P11	PD1	
	97 50 IN SMC_PCH_1V05_ISENSE	R11	PD2	
	97 50 IN SMC_PCH_1V05_VSENSE	N11	PD3	
	97 50 IN SMC_GPU_ISENSE	P10	PD4	
	97 50 IN SMC_GPU_VSENSE	R10	PD5	
	97 50 IN SMC_DIMM_ISENSE	N10	PD6	
	97 50 IN SMC_DIMM_VSENSE	M10	PD7	

PE0	M3	SMC_PE0	IN 47	K62 NEW:NOT USE,PULLED UP
PE1*	M2	SMC_TCK	IN 47 48	
PE2*	M1	SMC_TDI	IN 47 48	
PE3*	L4	SMC_TDO	OUT 47 48	
PE4*	L2	SMC_TMS	IN 47 48	
PF0	M7	G3_POWERON_L	IN 47	
PF1	P6	SMC_SYS_LED	OUT 47	
PF2	R6	SMC_LID	47	
PF3	N6	NC		
PF4	M6	NC		
PF5	R5	BDV_BKL_PWM	OUT 84 100	K62 PROTO-2:NEW
PF6	P5	NC		
PF7	N5	NC		
PG0	P9	NC		
PG1	R9	SMC_SMS_INT	IN 47	
PG2	N9	(OC) SMB_BSA_DATA	BI 49	
PG3	P8	(OC) SMB_BSA_CLK	BI 49	
PG4	R8	(OC) SMB_A_S3_DATA	BI 49	
PG5	M8	(OC) SMB_A_S3_CLK	BI 49	
PG6	P7	(OC) SMB_B_S0_DATA	BI 49	
PG7	R7	(OC) SMB_B_S0_CLK	BI 49	
PH0	E1	SMC_PROCHOT	OUT 47 100	
PH1	F3	SMC_THRMTRIP	OUT	
PH2	K2	NC		
PECI	PH3	C4	100 CPU_PECI_R	
PEVref	PH4	D4	PVCCIO_S0_SMC_R	
PEVSTP	PH5	B3	100 PM_PECI_PWRGD_R	

R4910 0 MF-LF 5% 402 1/16W — CPU_PECI 11 21 100
R4911 0 MF-LF 5% 402 1/16W — =PPVCCIO_S0_SMC 6 47
R4912 0 MF-LF 5% 402 1/16W — PM_PECI_PWRGD 64 100

C4910 0.1UF 20% 10V CERM 402

SMC PB3: SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)

SMC PG1: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC MASTER=K62 JERRY SYNC DATE=01/09/2011

PAGE TITLE: SMC

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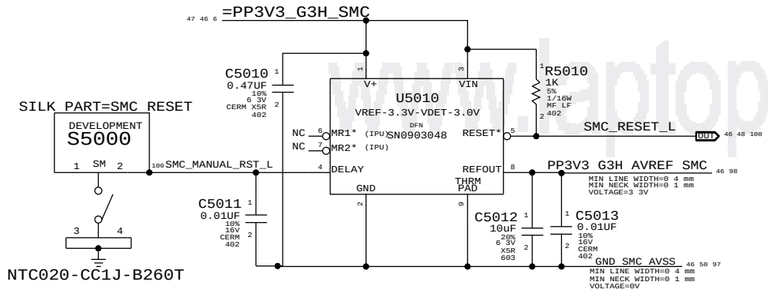
SMC Reset "Button", Supervisor & AVREF Supply



MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

MISC. SIGNAL ALIASES

SMC_GFX_OVERTEMP_L	MXM_ALERT_L	MAKE BASE=TRUE
SMC_GFX_THROTTLE_L	MXM_PWR_LEVEL	MAKE BASE=TRUE
CPUIMVP_VR_ON	SMC_DELAYED_PWRGD	MAKE BASE=TRUE

UNUSED PORT 7 ANALOG SENSORS

=PP3V3 G3H SMC

SMC_ONOFF_L	R5020	10K	5% 1/16W MF LF 402
SMC_TX_L	R5021	10K	5% 1/16W MF LF 402
SMC_RX_L	R5022	100K	5% 1/16W MF LF 402
SYS_ONEWIRE	R5023	2.0K	5% 1/16W MF LF 402
SMC_TMS	R5024	10K	5% 1/16W MF LF 402
SMC_TDO	R5025	10K	5% 1/16W MF LF 402
SMC_TDI	R5026	10K	5% 1/16W MF LF 402
SMC_TCK	R5027	10K	5% 1/16W MF LF 402
SMC_BIL_BUTTON_L	R5028	10K	5% 1/16W MF LF 402
SMC_BC_ACOK	R5029	10K	5% 1/16W MF LF 402
SMC_ADAPTER_EN	R5030	10K	5% 1/16W MF LF 402
USB_DEBUGPRT_EN_L	R5031	10K	5% 1/16W MF LF 402
G3_POWERON_L	R5034	10K	5% 1/16W MF LF 402
SMC_SMS_INT	R5032	10K	5% 1/16W MF LF 402
SMC_LID	R5033	10K	5% 1/16W MF LF 402
SMC_PA0	R5037	100K	5% 1/16W MF LF 402
SMC_PB6	R5038	100K	5% 1/16W MF LF 402
SMC_PE0	R5036	100K	5% 1/16W MF LF 402

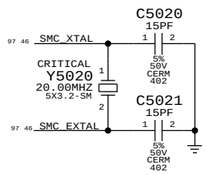
=PP3V3_S0_SMC_LS

SMC_GFX_OVERTEMP_L	R5035	10K	5% 1/16W MF LF 402
SMC_RUNTIME_SCI_L	R5044	10K	5% 1/16W MF LF 402

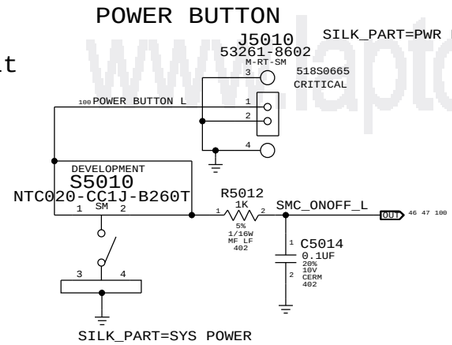
UNUSED TP/NC ALIASES

SMC_EXCARD_PWR_EN	TP_SMC_EXCARD_PWR_EN	MAKE BASE=TRUE
SMS_ONOFF_L	TP_SMS_ONOFF_L	MAKE BASE=TRUE
SMC_RSTGATE_L	TP_SMC_RSTGATE_L	MAKE BASE=TRUE
SMC_SYS_LED	TP_SMC_SYS_LED	MAKE BASE=TRUE
SMC_PB3	TP_SMC_PB3	MAKE BASE=TRUE

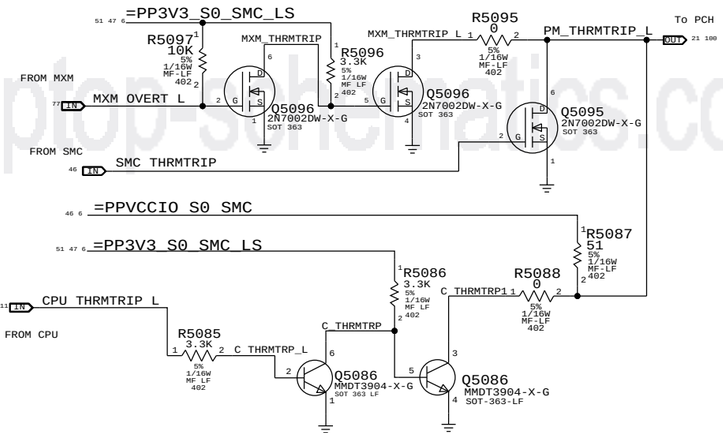
SMC Crystal Circuit



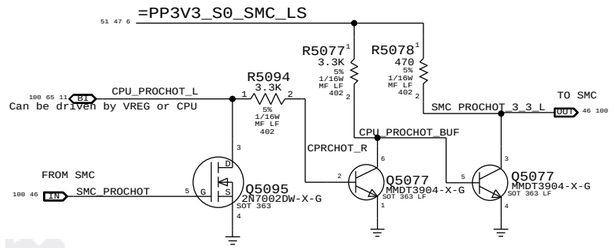
POWER BUTTON



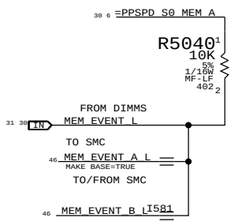
SMC & MXM THERMTRIP LEVEL SHIFTING



SMC PROCHOT 3.3V LEVEL SHIFTING



MEM_EVENT



SYNC MASTER=K62 JERRY	SYNC DATE=01/09/2011
PAGE TITLE	SMC Support
Apple Inc.	DRAWING NUMBER 051-8442 SIZE D
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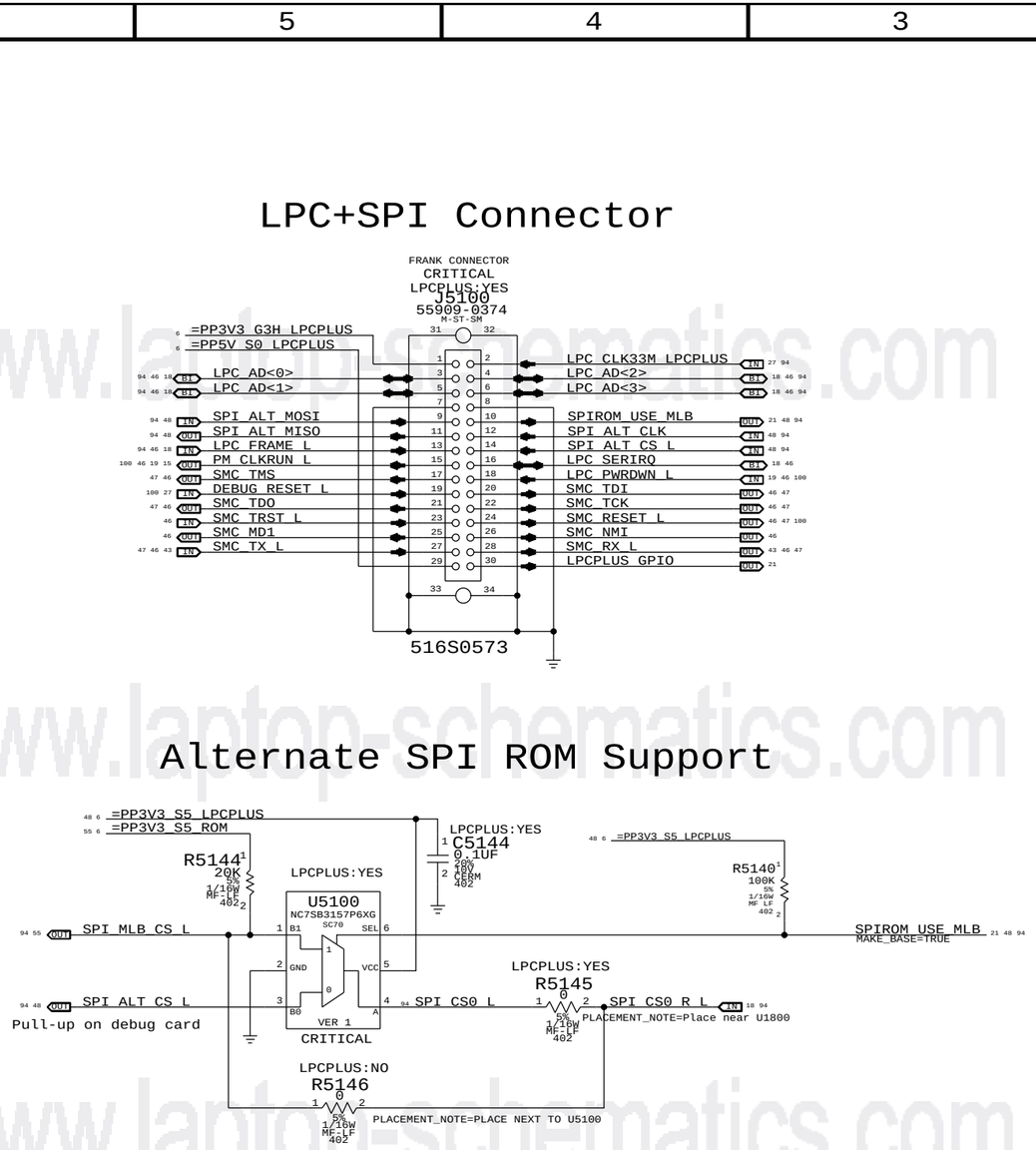
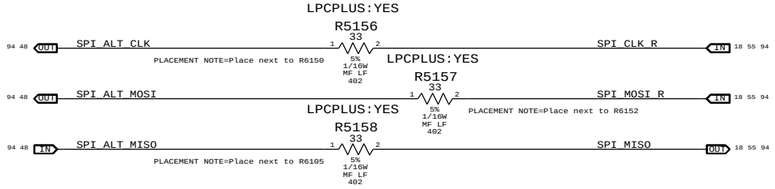
LPC+SPI Connector

Alternate SPI ROM Support



SPI Bus Series Resistance Option



SYNC_MASTER=K62_AARON SYNC_DATE=11/30/2009

PAGE TITLE: LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

REVISION: 10.1.0

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PCH "SMBUS" CONNECTIONS

=PP3V3_S0_SMBUS (49, 6)

PCH
U1800
(MASTER)

R5208 2.2K 5% 1/16W MF LF 402
R5209 2.2K 5% 1/16W MF LF 402

SMBUS_PCH_CLK (97, 18) MAKE_BASE=TRUE
SMBUS_PCH_DATA (97, 18) MAKE_BASE=TRUE

MEMORY A DIMMS
J3100-A/B
(DIMM0: WRITE: 0XA0 READ: 0XA1)
(DIMM2: WRITE: 0XA2 READ: 0XA3)
=I2C_SODIMMA_SCL (30)
=I2C_SODIMMA_SDA (30)

MEMORY B DIMMS
J3200-A/B
(DIMM1: WRITE: 0XA4 READ: 0XA5)
(DIMM3: WRITE: 0XA6 READ: 0XA7)
=I2C_SODIMMB_SCL (31)
=I2C_SODIMMB_SDA (31)

XDP (PCH)
J2550
=SMBUS_XDP_SCL (49, 25)
=SMBUS_XDP_SDA (49, 25)

MIKEY
U6806
(WRITE: 0X72 READ: 0X73)
=I2C_AUDIO_SCL (62)
=I2C_AUDIO_SDA (62)

XDP (CPU)
J2500
=SMBUS_XDP_SCL (49, 25)
=SMBUS_XDP_SDA (49, 25)

CK505
U2600
(WRITE: 0XD2 READ: 0XD3)
=SMBUS_CK505_SCL (26)
=SMBUS_CK505_SDA (26)

MEM VREF MARGIN A
U2900
(WRITE: 0X5C READ: 0X5D)
=I2C_VREFMRGN_A_SCL (28)
=I2C_VREFMRGN_A_SDA (28)

SPTX BLC MICRO
VIA J602
(WRITE: 0X6E READ: 0X6F)
=SMB_BLC_PCH_SCL (6)
=SMB_BLC_PCH_SDA (6)

MEM VREF MARGIN B
U2910
(WRITE: 0X7C READ: 0X7D)
=I2C_VREFMRGN_B_SCL (28)
=I2C_VREFMRGN_B_SDA (28)

NEED TO ADD PCH_SDA
ISOLATION CIRCUITRY

DP SDRV "A"
U9310, PS8301
(WRITE: 0X94, READ: 0X95)
=I2C_DPSDRVA_SCL (85)
=I2C_DPSDRVA_SDA (85)

DP SDRV "B"
U9510, PS8301
(WRITE: 0XB4, READ: 0XB5)
=I2C_DPSDRVB_SCL (87)
=I2C_DPSDRVB_SDA (87)

PCH "SML 0" CONNECTIONS

=PP3V3_S0_SMBUS (49, 6)

PCH
U1800
(MASTER)

R5202 8.2K 5% 1/16W MF LF 402
R5203 8.2K 5% 1/16W MF LF 402

SML_PCH_0_CLK (97, 18) MAKE_BASE=TRUE
SML_PCH_0_DATA (97, 18) MAKE_BASE=TRUE

THIS PAGE DIFFERENT BETWEEN K60 AND K62.

SMC SLAVE SMBUS "2" CONNECTIONS

USES INTERNAL SMC CONTROLLER CHANNEL 2 ONLY (NO CONNECTIONS, JUST PULLUP)

=PP3V3_S0_SMBUS_SMC_BSA (6)

SMC
U4900
(SLAVE)

R5280 100K 5% 1/16W MF LF 402
R5281 100K 5% 1/16W MF LF 402

SMB_BSA_CLK (46) — SMBUS_SMC_BSA_SCL (97) MAKE_BASE=TRUE
SMB_BSA_DATA (46) — SMBUS_SMC_BSA_SDA (97) MAKE_BASE=TRUE

SMC "B" SMBUS CONNECTIONS

BUS B CAN USE EITHER INTERNAL SMC CHANNEL 0 OR 1, K60/62 CHOOSES 0

=PP3V3_S0_SMBUS_SMC_B (6)

SMC
U4900
(MASTER)

R5260 2.0K 5% 1/16W MF LF 402
R5261 2.0K 5% 1/16W MF LF 402

SMB_B_S0_CLK (46) — SMBUS_SMC_B_S0_SCL (97) MAKE_BASE=TRUE
SMB_B_S0_DATA (46) — SMBUS_SMC_B_S0_SDA (97) MAKE_BASE=TRUE

AC/DC PS TEMPS
EMC1403-[1,2] : ACDC THRU J600
(WRITE 0X98 OR 0X9A READ 0X99 OR 0X9B)
3 SENSE POINTS PRIMARY SECONDARY AMB
=SMB_ACDC_SCL (6)
=SMB_ACDC_SDA (6)

AC/DC PS POWER
INA219: ACDC THRU J600
(WRITE 0X80 READ 0X81)
OUTPUT VOLTAGE CURRENT POWER

SMC "0" SMBUS CONNECTIONS

USES INTERNAL SMC CONTROLLER CHANNEL 0 ONLY

=PP3V3_S0_SMBUS_SMC_0 (6)

SMC
U4900
(MASTER)

R5250 2.2K 5% 1/16W MF LF 402
R5251 2.2K 5% 1/16W MF LF 402

SMB_0_S0_CLK (46) — SMBUS_SMC_0_S0_SCL (97) MAKE_BASE=TRUE
SMB_0_S0_DATA (46) — SMBUS_SMC_0_S0_SDA (97) MAKE_BASE=TRUE

Also reserve 0x56 and 0x32 per spec

MXM TEMP
GPU ON CARD - J8400
NV INSIDE (WRITE: 0X9E READ: 0X9F)
EMC1402 ON AMD MXM CARD (WRITE 0X98 READ 0X99)
=SMB_MXM_THRM_SCL (77)
=SMB_MXM_THRM_SDA (77)

EMC1414: U5520
DEV: CPU_D,CPU_HTSK
(WRITE: 0X78 READ: 0X79)
EMC1428: U5500
PROD: AMB_L_SKIN_R_SKIN_ODD, LCD,CPU_PROX,MXM_TEMPS
(WRITE: 0X92 READ:0X93)
=SMB_SNS1_SCL (52)
=SMB_SNS1_SDA (52)

PCIE MINI-CARD
X18 WI-FI MODULE
TMP106: J3400
(WRITE: 0X90 READ: 0X91)
=SMB_MINI_SCL (33)
=SMB_MINI_SDA (33)

PCH "SML 1" CONNECTIONS

=PP3V3_S0_SMBUS (49, 6)

PCH (FOR TEMP)
U1800
(SLAVE)
(WRITE: 0X86 READ: 0X89)
SML_PCH_1_CLK (97, 18) MAKE_BASE=TRUE
SML_PCH_1_DATA (97, 18) MAKE_BASE=TRUE

NOSTUFF R5204 8.2K 5% 1/16W MF LF 402
NOSTUFF R5205 8.2K 5% 1/16W MF LF 402

R5206 0 5% 1/10W MF-LF 402
R5207 0 5% 1/10W MF-LF 402

THE PCH address is user programmable by SPI ROM

SMC "A" SMBUS CONNECTIONS

NOTE: SMC RMT BUS REMAINS POWERED AND MAY BE ACTIVE IN S3 STATE
BUS A CAN USE EITHER INTERNAL SMC CHANNEL 0 OR 1, K74 CHOOSES 1

=PP3V3_S3_SMBUS_SMC_A (6)

SMC
U4900
(MASTER)

R5270 4.7K 5% 1/16W MF-LF 402
R5271 4.7K 5% 1/16W MF-LF 402

SMB_A_S3_CLK (46) — SMBUS_SMC_A_S3_SCL (97) MAKE_BASE=TRUE
SMB_A_S3_DATA (46) — SMBUS_SMC_A_S3_SDA (97) MAKE_BASE=TRUE

ALS
(WRITE: 0X52 READ: 0X53)
=SMB_ALS_SCL (44)
=SMB_ALS_SDA (44)

SMC "MANAGEMENT" SMBUS (BUS 1)

USES INTERNAL SMC CONTROLLER CHANNEL 1 ONLY

=PP3V3_S0_SMBUS_SMC_MGMT (6)

SMC
U4900
(MASTER)

R5290 2.2K 5% 1/16W MF LF 402
R5291 2.2K 5% 1/16W MF LF 402

SMB_MGMT_CLK (46) — SMBUS_SMC_MGMT_SCL (97) MAKE_BASE=TRUE
SMB_MGMT_DATA (46) — SMBUS_SMC_MGMT_SDA (97) MAKE_BASE=TRUE

PANEL TEMP SENSOR
TMP421 ON TCON BOARD VIA J9002
(SLAVE)
(WRITE: 0X9E READ: 0X9F)
SMB_DP_TCON_SLA_SCL (82)
SMB_DP_TCON_SLA_SDA (82)

DISPLAY TCON
PARADE ON TCON BOARD VIA J9002
(SLAVE)
(TBD WRITE: 0X1A READ: 0X1B)
(TO READ VENDOR ID AND PANEL ID)
TCON ALSO HAS MASTER BUS TO LUT ROM AND EDID ROM

DISPLAY TCON TO SPTX OR O2M BLC

=PP3V3_S0_SMBUS (49, 6)

DISPLAY TCON
VIA J9002
(MASTER)

R5210 2.2K 5% 1/16W MF LF 402
R5211 2.2K 5% 1/16W MF LF 402

=SMB_DP_TCON_SDA — MAKE_BASE=TRUE
=SMB_DP_TCON_SCL — MAKE_BASE=TRUE

BLC MICRO
VIA J602
(SLAVE)
(WRITE: 0X6E READ: 0X6F)
SMB_BLC_TCON_SDA (82, 6) MUX
SMB_BLC_TCON_SCL (97, 82) BT

NOTE: DISPLAY TCON HAS 4.7K PU.
NOTE: SPTX BLC HAS 4.7K PU.
NOTE: O2MICRO BLC HAS NO PU.

T29 I2C CONNECTIONS

=PP3V3_S0_T29I2C (6)

I2C BUS PULL-UP RAIL MUST REFLECT WHEN USB POWER (VBUS) IS VALID.

T29 IC
U9700
(MASTER)

T29 R5230 4.7K 5% 1/16W MF LF 402
T29 R5231 4.7K 5% 1/16W MF LF 402

I2C_T29_SCL (99, 89) MAKE_BASE=TRUE
I2C_T29_SDA (99, 89) MAKE_BASE=TRUE

T29 PORT A MCU
U9330
(WRITE: 0X26 READ: 0X27)
=I2C_T29AMCU_SCL (85)
=I2C_T29AMCU_SDA (85)

T29 PORT B MCU
U9530
(WRITE: 0X24 READ: 0X25)
=I2C_T29BMCU_SCL (87)
=I2C_T29BMCU_SDA (87)

SYNC_MASTER=K62_MARK
SYNC_DATE=01/09/2011
PAGE TITLE
SMBUS CONNECTIONS

Apple Inc.

DRAWING NUMBER 051-8442
SIZE D
REVISION 10.1.0
BRANCH
PAGE 52 OF 110
SHEET 49 OF 101

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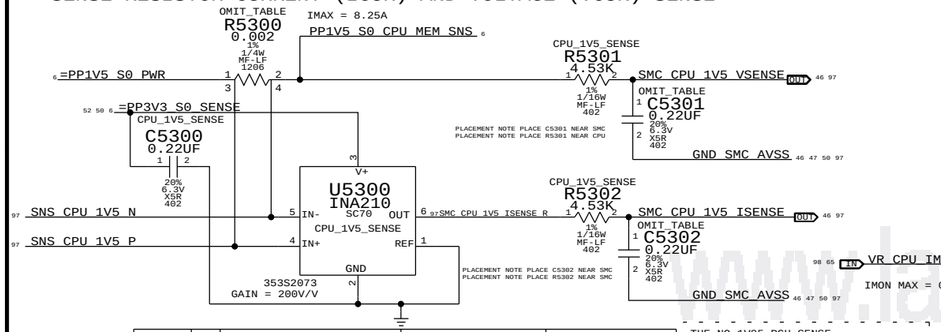
CPU VDD 1.5V

SENSE RESISTOR CURRENT (IC5R) AND VOLTAGE (VC5R) SENSE

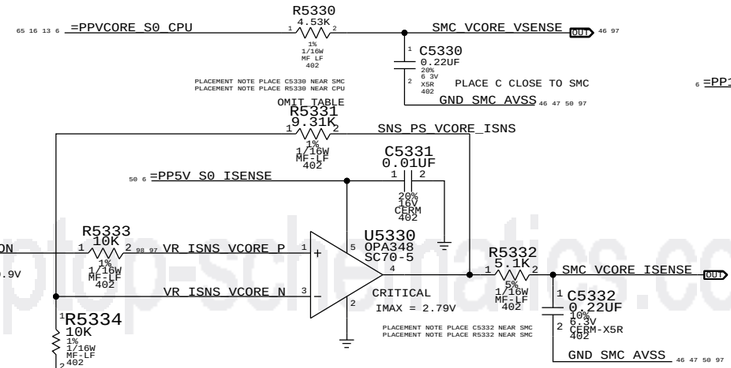


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
104S0018	1	RES,2 MILLIOHM,1206	R5300	CPU_1V5_SENSE
101S0414	1	RES,0 OHM,1206,20 MILLIOHM MAX	R5300	NO_CPU_1V5_SENSE
132S0080	2	CAP,0.22UF,402	C5301,C5302	CPU_1V5_SENSE
116S0004	2	RES,0 OHM,402	C5301,C5302	NO_CPU_1V5_SENSE

THE NO_1V05_PCH_SENSE, NO_CPU_VCCSA_SENSE, AND NO_CPU_1V5_SENSE COMPOPTIONS SHOULD IDEALLY NEVER BE USED AS TOTAL CPU POWER SENSING REQUIRES ALL 3 SENSORS.

CPU VCC (VCORE)

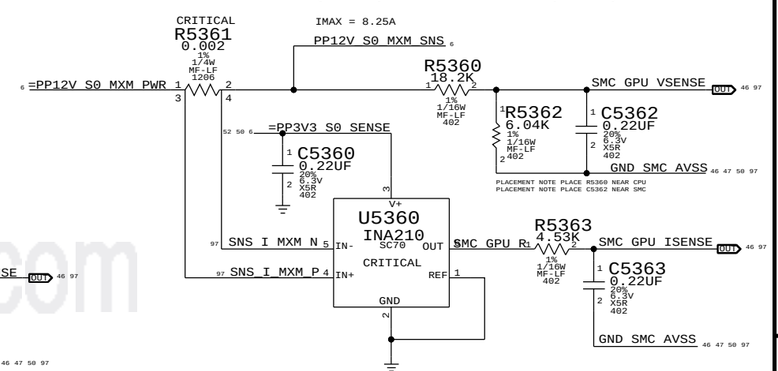
IMON CURRENT (IC0C) AND VOLTAGE (VC0C) SENSE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0312	1	RES,MTL FILM,1/16W,9.31K,0402	R5331	CPUVCORE-3PH
114S0345	1	RES,MTL FILM,1/16W,21K,0402	R5331	CPUVCORE-4PH

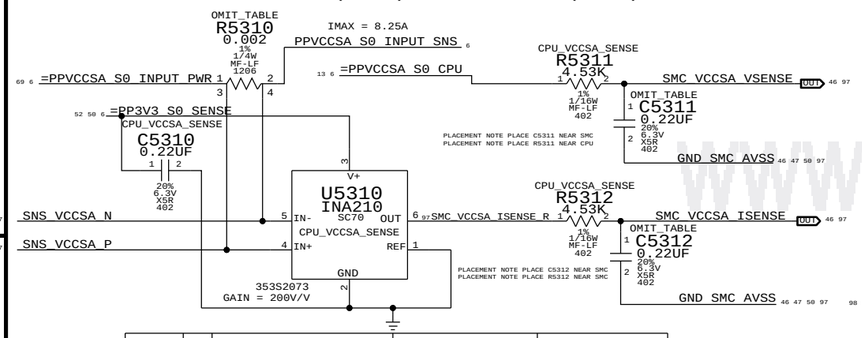
GPU MXM

SENSE RESISTOR CURRENT (IG0R) AND VOLTAGE (VG0R) SENSE



CPU VCCSA

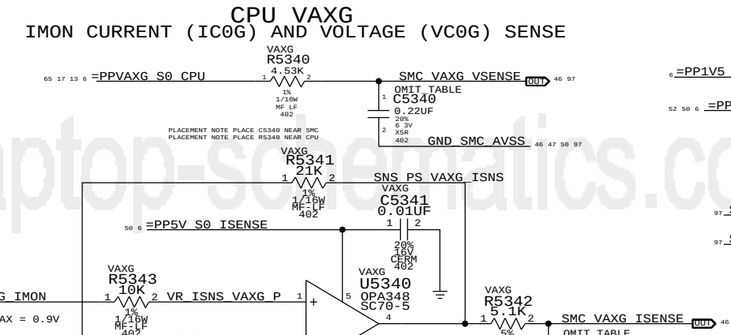
SENSE RESISTOR CURRENT (ICSR) AND VOLTAGE (VCSR) SENSE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
104S0018	1	RES,2 MILLIOHM,1206	R5310	CPU_VCCSA_SENSE
101S0414	1	RES,0 OHM,1206,20 MILLIOHM MAX	R5310	NO_CPU_VCCSA_SENSE
132S0080	2	CAP,0.22UF,402	C5311,C5312	CPU_VCCSA_SENSE
116S0004	2	RES,0 OHM,402	C5311,C5312	NO_CPU_VCCSA_SENSE

CPU VAXG

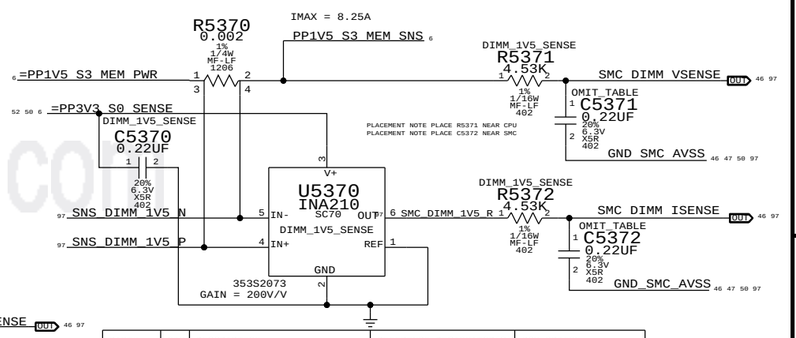
IMON CURRENT (IC0G) AND VOLTAGE (VC0G) SENSE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0080	2	CAP,0.22UF,402	C5340,C5342	VAXG
116S0004	2	RES,0 OHM,402	C5340,C5342	NO_VAXG

DIMM VDD 1.5V (LIKELY DEVELOPMENT ONLY)

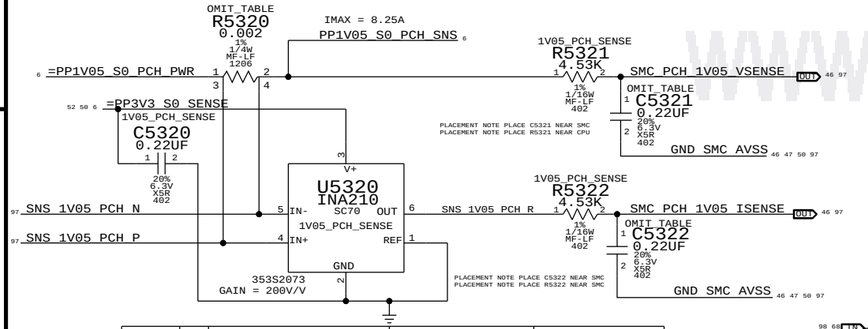
SENSE RESISTOR CURRENT (IM0R) AND VOLTAGE (VM0R) SENSE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0080	2	CAP,0.22UF,402	C5371,C5372	DIMM_1V5_SENSE
116S0004	2	RES,0 OHM,402	C5371,C5372	PRODUCTION

PCH 1.05V

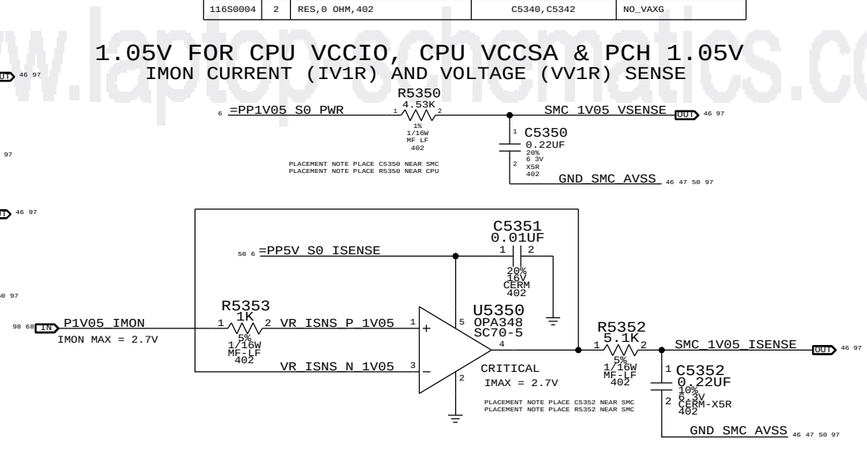
SENSE RESISTOR CURRENT (IN1R) AND VOLTAGE (VN1R) SENSE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
104S0018	1	RES,2 MILLIOHM,1206	R5320	1V05_PCH_SENSE
101S0414	1	RES,0 OHM,1206,20 MILLIOHM MAX	R5320	NO_1V05_PCH_SENSE
132S0080	2	CAP,0.22UF,402	C5321,C5322	1V05_PCH_SENSE
116S0004	2	RES,0 OHM,402	C5321,C5322	NO_1V05_PCH_SENSE

1.05V FOR CPU VCCIO, CPU VCCSA & PCH 1.05V

IMON CURRENT (IV1R) AND VOLTAGE (VV1R) SENSE



NOTE: TOTAL CPU POWER = VC0C+ICOC + VCSA+ICSA + VC0G+ICOG + VV1R+ICIR

where ICIR = IV1R - IN1R - ICSR

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SYNC_MASTER=K62_MARK SYNC_DATE=01/09/2011

PAGE TITLE
CPU/PCH/GPU POWER SENSE

Apple Inc.

DRAWING NUMBER 051-8442 SIZE D
REVISION 10.1.0
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PAGE 53 OF 110
SHEET 50 OF 101

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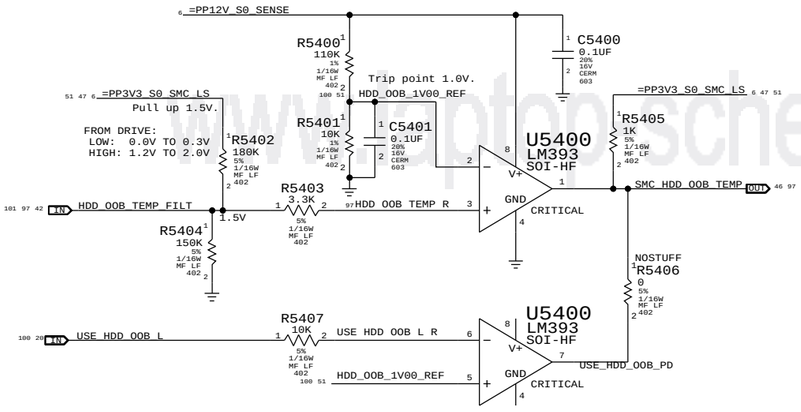
HDD OOB TEMPERATURE SENSING



DRIVE ACTIVE = VALID SIGNAL PROTOCOL BETWEEN 0-2.0V.
DRIVE ASLEEP = HDD DRIVES HDD_OOB_TEMP LOW
DRIVE ABSENT = OOB IS PULLED HIGH UNLESS PCH DETERMINES SSD PRESENT AND DRIVES USE_HDD_OOB_L LOW WHICH THEN PULLS HDD_OOB_TEMP LOW.

NOTE: WILL BE CONNECTED TO SATA PWR CONNECTOR PIN 11
THIS PIN IS ORIGINALLY INTENDED FOR HDD LED OUTPUT,
AND ALSO FOR HDD STAGGERED PIN UP (FLOATING) OR IMMEDIATE SPIN-UP (GROUND).
BOTH FUNCTIONS NOT USED.

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SYNC MASTER=K62 MARK SYNC DATE=01/09/2011

PAGE TITLE
HDD OOB SENSE

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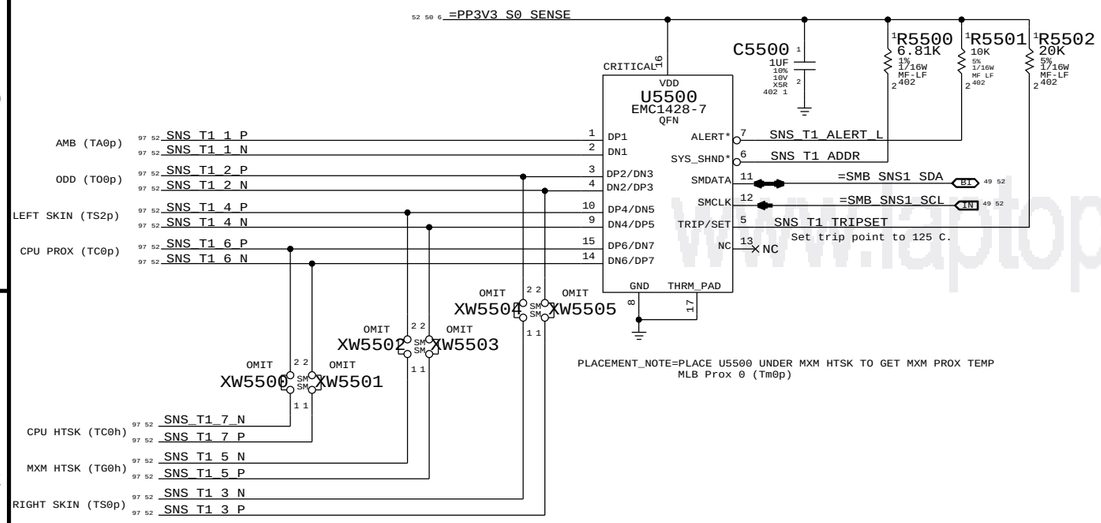
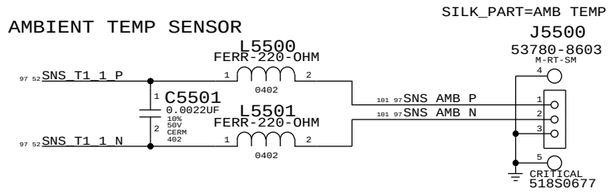
SNS T1: PRODUCTION TEMP SENSOR IC



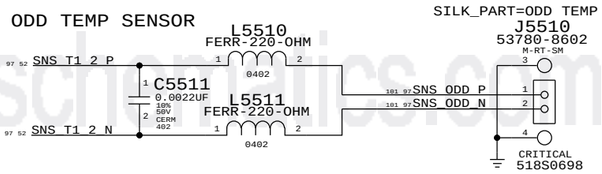
PLACEMENT_NOTE=PLACE U5500 UNDER MXM HTSK TO GET MXM PROX TEMP
MLB Prox 0 (Tm0p)

EMC1428-7: 6.8K PULL UP: I2C ADDRESS: WRITE: 0x92, READ: 0x93

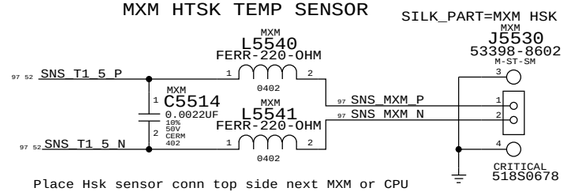
AMBIENT TEMP SENSOR



ODD TEMP SENSOR

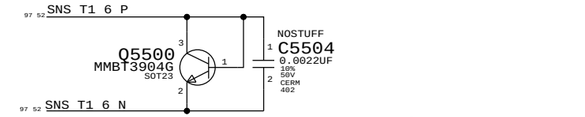


MXM HTSK TEMP SENSOR



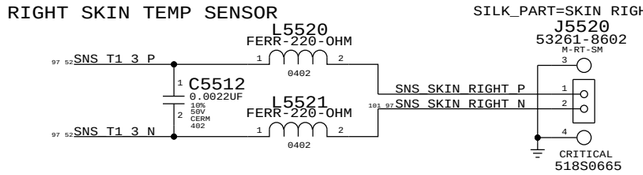
Place Hsk sensor conn top side next MXM or CPU

CPU PROXIMITY TEMP SENSOR

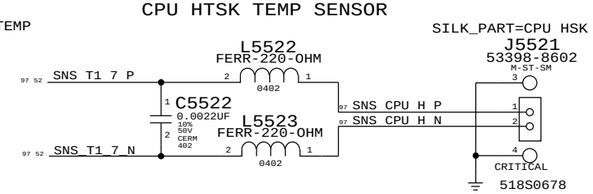


Place Q5500 (CPU Proximity Sensor) at the solder side
at edge near backer plate of CPU to replace HeatSink Temp Sensor

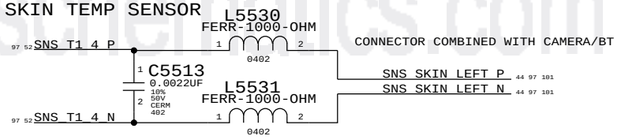
RIGHT SKIN TEMP SENSOR



CPU HTSK TEMP SENSOR

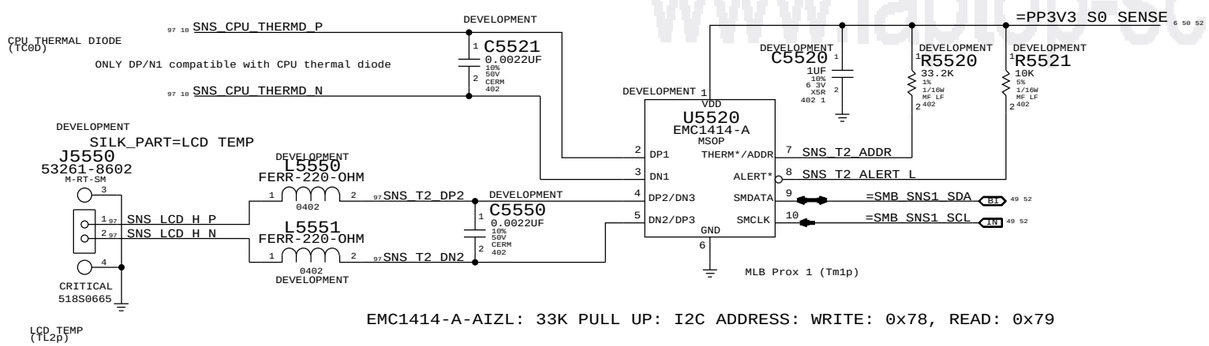


LEFT SKIN TEMP SENSOR



THIS PAGE DIFFERENT BETWEEN K60 AND K62.

SNS T2: DEVELOPMENT TEMP SENSOR IC



MLB Prox 1 (Tm1p)

EMC1414-A-AIZL: 33K PULL UP: I2C ADDRESS: WRITE: 0x78, READ: 0x79

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SYNC MASTER=K62 MARK | SYNC DATE=01/09/2011

PAGE TITLE: TEMP SENSORS

Apple Inc.

DRAWING NUMBER: 051-8442 | SIZE: D

REVISION: 10.1.0

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PAGE: 55 OF 110

SHEET: 52 OF 101

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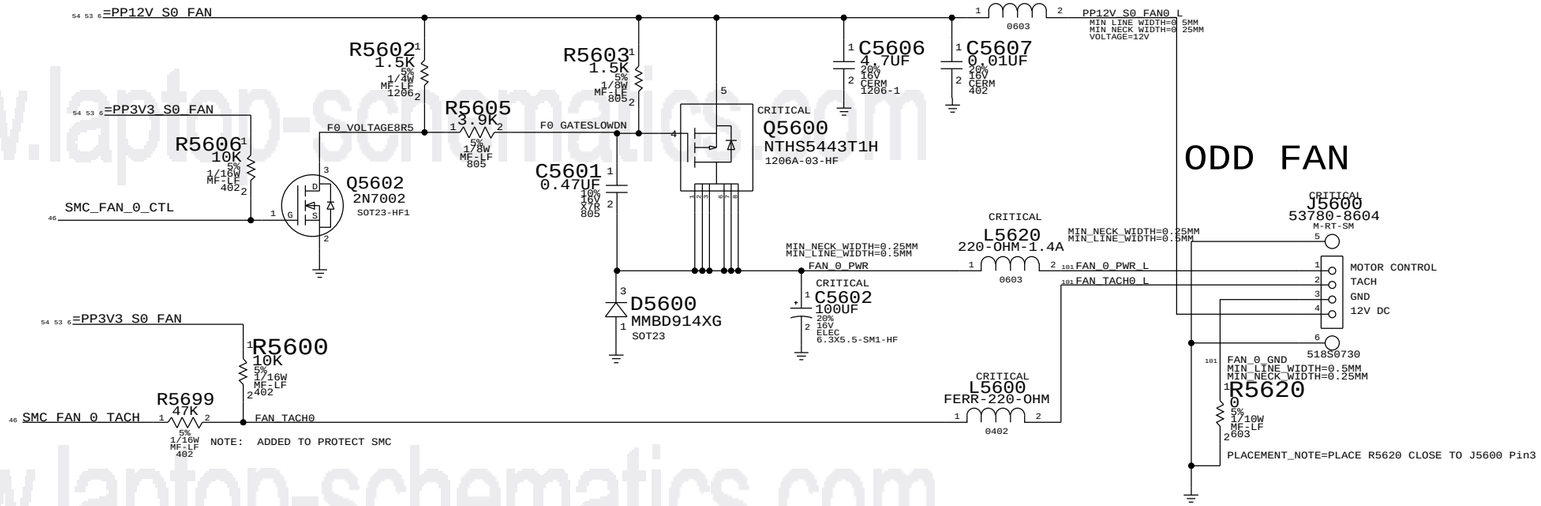
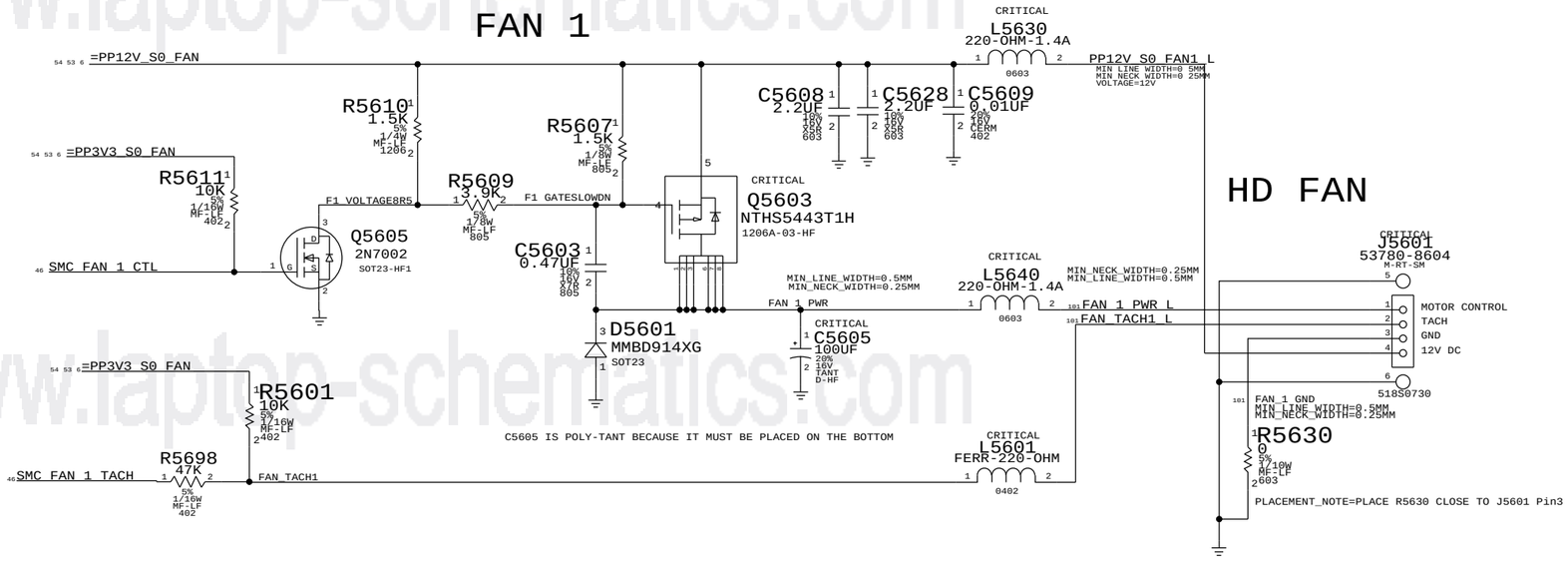
FAN 0



FAN 1



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SYNC_MASTER=K62_JERRY SYNC_DATE=01/09/2011

PAGE TITLE: HD AND OD FAN

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DRAWING NUMBER: 051-8442 SIZE: D

REVISION: 10.1.0

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SHEET: 53 OF 101

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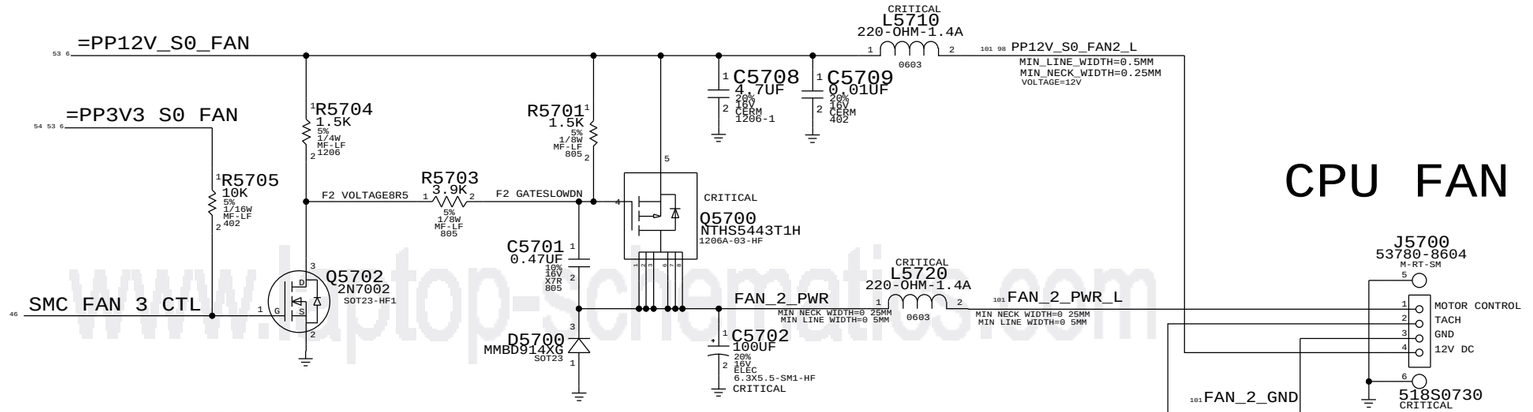
SMC'S FAN3 OUTPUT CONTROL FAN 2



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FAN 3 SMC CONTROL (UNUSED)

SYNC_MASTER=K62 JERRY SYNC_DATE=01/09/2011

PAGE TITLE: CPU FAN

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DRAWING NUMBER: 051-8442 SIZE: D

REVISION: 10.1.0

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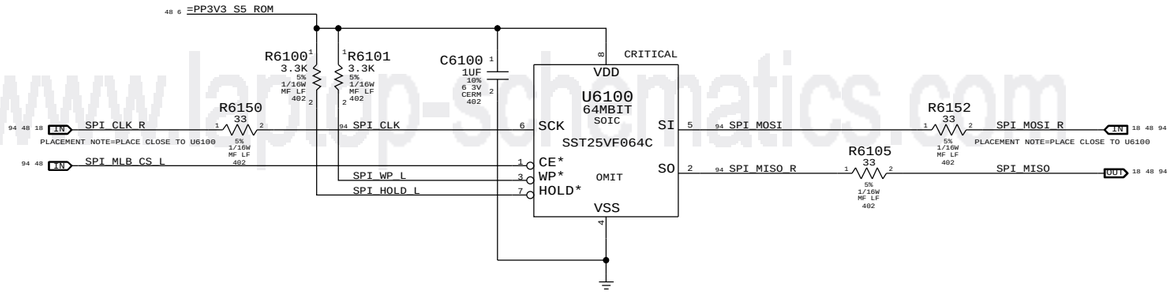

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SYNC MASTER=K62 AARON SYNC DATE=11/30/2009

PAGE TITLE

SPI ROM

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AUDIO CODEC

APPLE P/N 353S2592

PLACE C6200 AS CLOSE TO PIN 9 AS POSSIBLE

VD MUST BE LESS THAN OR EQUAL TO VL_HD

=PP1V5_S0_AUD_DIG

C6201 4.7UF 20% 4V X5R-1 402

C6200 0.47UF 10% 10V X5R 402

GND_AUDIO_HPAMP

PP4V5_AUDIO_ANALOG

R6200 2.67K 1% 1/16W MF-LF 402

C6209 2.2UF 20% 6.3V CERM 402-LF

C6210 2.2UF 20% 6.3V CERM 402-LF

C6208 10UF 20% 10V POLY-TANT CASE-B2-SM

C6202 0.47UF 10% 10V X5R 402

C6203 10UF 20% 10V POLY-TANT CASE-B2-SM

C6205 1UF 10% 10V X5R 402-1

C6204 0.47UF 10% 10V X5R 402

C6206 0.47UF 10% 10V X5R 402

CRITICAL C6207 10UF 20% 6.3V CERM-X5R 0402-1

PP5V_AUDIO_HPAMP

=PP3V3_S0_AUDIO

PP4V5_AUDIO_ANALOG

GND_AUDIO_CODEC

GND_AUDIO_HPAMP

R6205 0 5% 1/16W MF-LF 402

TWEETERS

VBIAS_DAC

CS4206_FP

CS4206_FN

CRITICAL U6201 CS4206B QFN

VBIAS_DAC	29	VBIAS_DAC	HPOUT_L	38	MIN_LINE_WIDTH=0.1MM MIN_NECK_WIDTH=0.1MM
CS4206_FP	44	VHP_FILT+	HPOUT_R	40	MIN_LINE_WIDTH=0.1MM MIN_NECK_WIDTH=0.1MM
CS4206_FN	41	VHP_FILT-	HPREF	39	MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.1MM

AUD_HP_PORT_L, AUD_HP_PORT_R, AUD_HP_PORT_REF

NC TP_AUD_DMIC_SDA1

NC TP_AUD_DMIC_SDA1

HP AMP SPEAKERS

AUD_GPIO_2

AUD_GPIO_3

AUD_SENSE_A

GPIO0/DMIC_SDA1, GPIO1/DMIC_SDA2, GPIO2/SPDIF_OUT2, GPIO3, SENSE_A

LINEOUT_L1+	35	AUD_LO1_L_P	HP AMP/LINE OUT
LINEOUT_L1-	34	AUD_LO1_L_N	
LINEOUT_R1+	36	AUD_LO1_R_P	
LINEOUT_R1-	37	AUD_LO1_R_N	
LINEOUT_L2+	31	AUD_LO2_L_P	WOOFERS
LINEOUT_L2-	30	AUD_LO2_L_N	
LINEOUT_R2+	32	AUD_LO2_R_P	
LINEOUT_R2-	33	AUD_LO2_R_N	

CS4206_FLYP

CS4206_FLYC

CS4206_FLYN

C6211 2.2UF 20% 6.3V CERM 402-LF

C6212 2.2UF 20% 6.3V CERM 402-LF

MICBIAS 16 — AUD_CODEC_MICBIAS (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM)

VCOM 28 — CS4206_VCOM (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM)

PLACE TP FOR ALL HDA SIGNALS NEAR CODEC

HDA_BIT_CLK	6	BITCLK	
HDA_SYNC	10	SYNC	
HDA_SDIN0	8	SDI	
	5	SDO	
HDA_SDOUT	11	RESET*	
HDA_RST_L			
AUD_SPDIF_IN_CODEC	47	SPDIF_IN	
AUD_SPDIF_CHIP	48	SPDIF_OUT	
AUD_SPDIF_OUT			

R6201 22 5% 1/16W MF-LF 402

R6202 22 5% 1/16W MF-LF 402

R6203 100K 1% 1/16W MF-LF 402

DGND THRM_PAD AGND

LINEIN_L+	21	AUD_LI_P_L	
LINEIN_C-	22	AUD_LI_COM	
LINEIN_R+	23	AUD_LI_P_R	
MICIN_L+	18	AUD_MIC_INP_L	
MICIN_L-	17	AUD_MIC_INN_L	
MICIN_R+	19	AUD_MIC_INR_P	
MICIN_R-	20	AUD_MIC_INR_N	
VREF+_ADC	27	CS4206_VREF_ADC NC (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM)	
DMIC_SCL	4	TP_CS4206_DMIC_SCL NC	

CRITICAL C6213 1UF 10% 20V TANT CASE-P3-MF

CRITICAL C6214 10UF 20% 10V POLY-TANT CASE-B2-SM

GND_AUDIO_HPAMP

GND_AUDIO_CODEC

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S2592	353S3199		U6201	CS4206A

APPLE P/N 353S2456
4.5V POWER SUPPLY FOR CODEC

XW6212 PP5V_AUDIO_HPAMP

L6210 FERR-220-OHM 0402

=PP5V_S0_AUDIO

R6220 0 5% 1/16W MF-LF 402

VR6201 TPS71745 SON CRITICAL

4V5_REG_IN, 4V5_REG_EN, 4V5_NR

PP4V5_AUDIO_ANALOG

C6221 1UF 10% 10V X5R 402-1

C6222 1UF 10% 10V X5R 402-1

C6223 0.1UF 10% 16V X7R-CERM 402

C6224 1UF 10% 10V X5R 402-1

R6212 0 5% 1/16W MF-LF 402

R6210 0 5% 1/16W MF-LF 603

XW6211 GND_AUDIO_HPAMP

GND_AUDIO_CODEC

ISOLATED 5 V POWER SUPPLY FOR HP AMP

APN 152S1314

=PP5V_S0_AUDIO

C6250 10UF 20% 10V X5R 603

CRITICAL Q6250 DMMT3906W-7-F SOT-363

R6258 1K 1% 1/16W MF-LF 402

CRITICAL C6256 1UF 10% 25V X5R 402

R6255 1.0K 1% 1/10W MF-LF 603

SC4503_SW

SC4503_SW_SNBR

SC4503_FB_DDROP

CRITICAL T6250 1.8UH-1.6A-243MOHM LPD3015-SM

AUD_XFRMR_SEC

D6252 DO222-SM STPS1L30MF

PP5V_AUDIO_ISO

CRITICAL C6258 150UF-.025-OHM 6.3V TANT CASE-B2-SM

APN 128S0271

C6259 10UF 20% 10V X5R 603

R6257 4.99K 1% 1/16W MF-LF 603

GND_AUDIO_ISO

D6250 SOD-523 BAT54XV2T1

C6257 0.1UF 10% 16V X7R-CERM 402

R6256 49.9K 1% 1/16W MF-LF 402

R6260 10 1% 1/16W MF-LF 603

APN 353S3080

Q6250 DMMT3906W-7-F SOT-363 CRITICAL

SC4503_FB_RDIV, SC4503_FB_PNP, SC4503_FB_FILT, SC4503_SW_D

R6253 43.2K 1% 1/16W MF-LF 402

D6251 SOD-523 BAT54XV2T1

R6254 20 1% 1/16W MF-LF 603

R6250 40.2K 1% 1/16W MF-LF 402

U6250 SC4503 TSOT-23 SYM_VER_2 CRITICAL

SC4503_SHDN, SC4503_FB

R6251 3.40K 1% 1/16W MF-LF 402

R6252 12.4K 1% 1/16W MF-LF 402

C6252 0.1UF 10% 16V X7R-CERM 402

C6251 0.1UF 10% 16V X7R-CERM 402

NOSTUFF C6253 1UF 10% 10V X5R 402-1

C6254 0.01UF 10% 16V CERM 402

NOSTUFF C6261 0.001UF 10% 50V X7R 402

NOSTUFF R6259 100K 1% 1/16W MF-LF 402

C6255 0.001UF 10% 50V X7R 402

SYNC MASTER=K62 DAVID	SYNC DATE=01/09/2011
PAGE TITLE	AUDIO: CODEC/REGULATOR
Apple Inc.	DRAWING NUMBER 051-8442, SIZE D
	REVISION 10.1.0
	BRANCH
	PAGE 62 OF 110
	SHEET 56 OF 101

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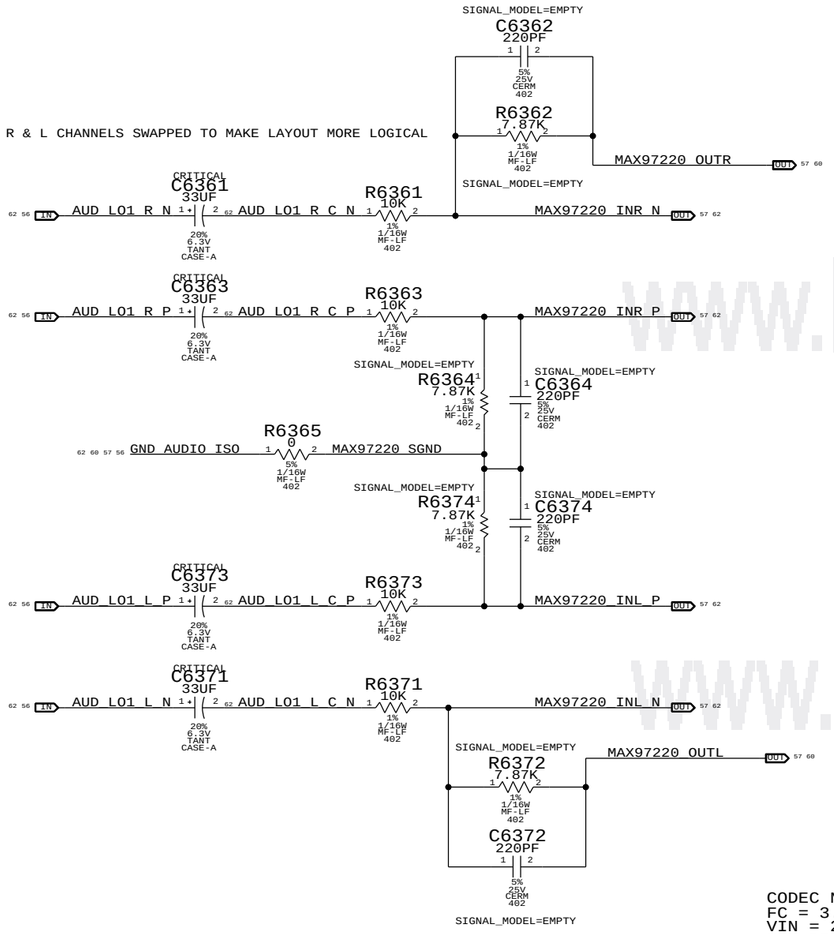
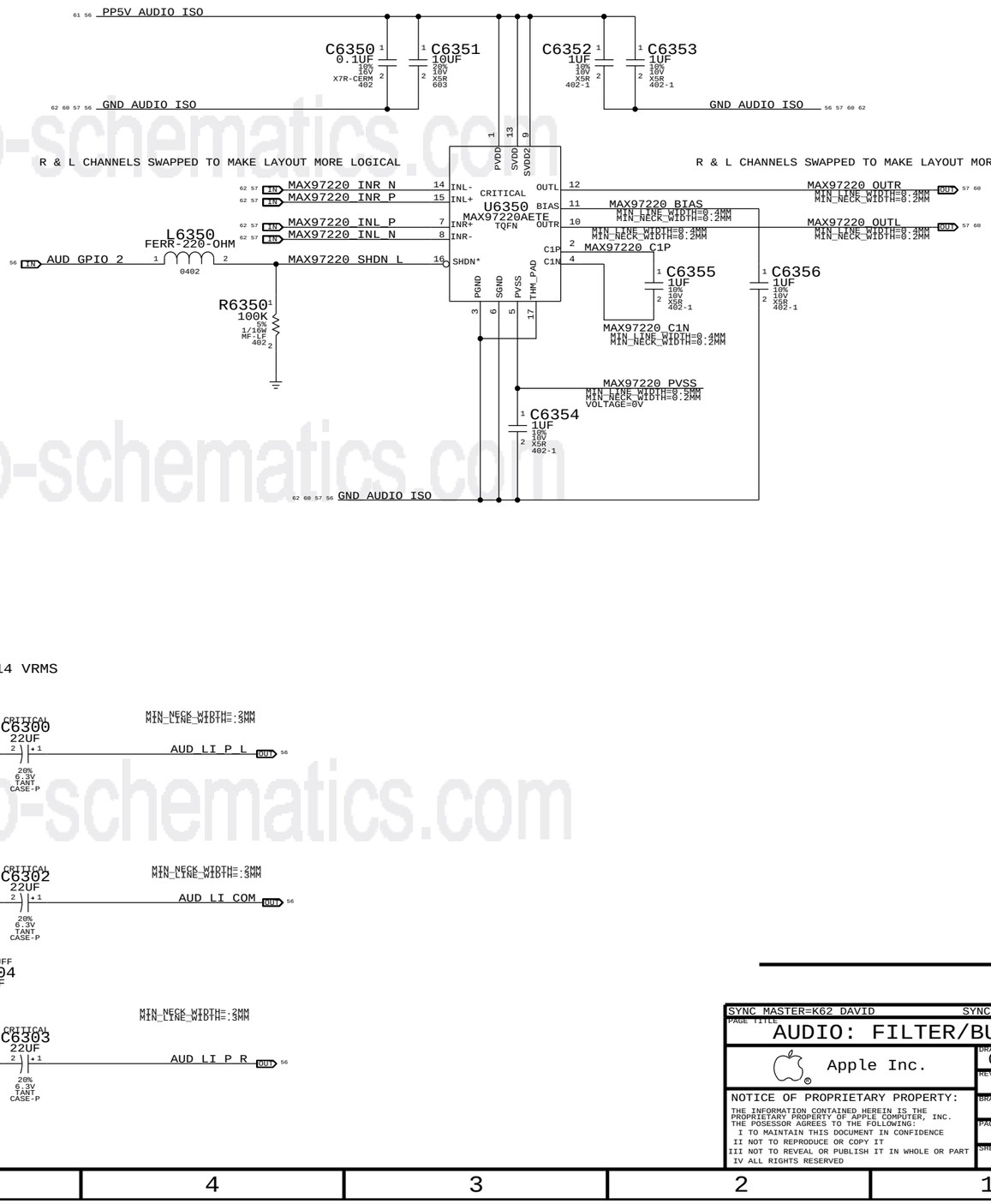
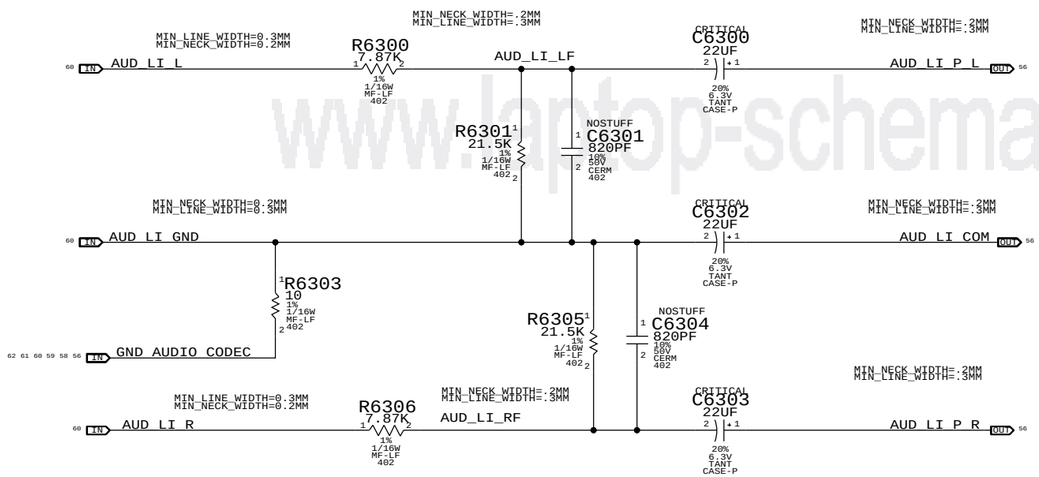




CODEC Nom SE RIN = 20K OHMS
FC = 3.62 HZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS
NET RIN = 18K OHMS



SYNC_MASTER=K62_DAVID SYNC_DATE=01/09/2011

PAGE TITLE
AUDIO: FILTER/BUFFER

Apple Inc.

DRAWING NUMBER 051-8442 SIZE D
REVISION 10.1.0
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RIGHT CH SPEAKER AMP
APPLE P/N 353S3069

=PP12V_S0_AUDIO_SPKRAMP

C6400 10UF 10% 25V X5R 805
C6401 0.1UF 10% 25V X5R 402

=PP3V3_S0_AUDIO

R6402 0 5% 1/10W MF-LF 402
NOSTUFF R6404 0 5% 1/10W MF-LF 402
NOSTUFF R6406 0 5% 1/16W MF-LF 402

AUD_RAMP_GAIN0
AUD_RAMP_GAIN1

R6405 0 5% 1/10W MF-LF 402
R6407 0 5% 1/16W MF-LF 402

C6402 0.1UF 10% 25V X5R 402
C6403 1UF 10% 25V X5R 603-1
C6404 0.1UF 10% 25V X5R 402
C6405 1UF 10% 25V X5R 603-1
CRITICAL C6406 220UF 20% 16V ELEC SM-CASE-C1-HF

R6402 = HIGH = 400 KHZ
SPEAKER AMP GAIN = +9 DB
SPEAKER AMP RIN = 210K NOMINAL W/ +9 DB GAIN
FC_HPF, TWEETERS = ~924 HZ (820 PF)
FC_HPF, WOOFERS = ~23 HZ (0.033 UF)

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

AUD_HP_R_N → L6400 FERR-1000-OHM 0402 → AUD_RAMP_RINC_P → C6408 820PF 10% 50V CERM 402 → AUD_RAMP_RIN_P
AUD_HP_R_P → L6401 FERR-1000-OHM 0402 → AUD_RAMP_RINC_N → C6409 820PF 10% 50V CERM 402 → AUD_RAMP_RIN_N
AUD_LO2_R_N → L6402 FERR-1000-OHM 0402 → AUD_RAMP_LINC_N → C6410 0.033UF 10% 16V X5R 402 → AUD_RAMP_LIN_N
AUD_LO2_R_P → L6403 FERR-1000-OHM 0402 → AUD_RAMP_LINC_P → C6411 0.033UF 10% 16V X5R 402 → AUD_RAMP_LIN_P

U6400 TPA3117D2 QFN CRITICAL

4	AVCC	BSPL	25
26	PVCCL	OUTPL	24
27	PVCCL	OUTNL	22
14	PVCCR	BSNL	21
15	PVCCR	BSPR	16
9	RINP	OUTPR	17
8	RINN	OUTNR	19
1	LINN	BSNR	20
32	LINP	NC	12, 13, 28, 29, 10
2	GAIN0		
3	GAIN1		
6	REG_OUT		
7	PLIMIT		
11	PBTL		
31	FSEL		
30	SD*		
5	AGND		
18	PGND		
23	PGND		
33	THRM PAD		

AUD_RAMP_BSPL → C6413 0.22UF 20% 25V X5R 603 → AUD_RAMP_OUTPL (MIN LINE WIDTH=0 6MM, MIN NECK WIDTH=0 25MM) → SIGNAL_MODEL=EMPTY CRITICAL L6404 220-OHM-25%-2.5A 0603 → AUD_SPKR_RWFR_OUT_P
AUD_RAMP_BSNL → C6414 0.22UF 20% 25V X5R 603 → AUD_RAMP_OUTNL (MIN LINE WIDTH=0 6MM, MIN NECK WIDTH=0 25MM) → SIGNAL_MODEL=EMPTY CRITICAL L6405 220-OHM-25%-2.5A 0603 → AUD_SPKR_RWFR_OUT_N
AUD_RAMP_BSPR → C6415 0.22UF 20% 25V X5R 603 → AUD_RAMP_OUTPR (MIN LINE WIDTH=0 6MM, MIN NECK WIDTH=0 25MM) → SIGNAL_MODEL=EMPTY CRITICAL L6406 220-OHM-25%-2.5A 0603 → AUD_SPKR_RTWT_OUT_N
AUD_RAMP_BSNR → C6416 0.22UF 20% 25V X5R 603 → AUD_RAMP_OUTNR (MIN LINE WIDTH=0 6MM, MIN NECK WIDTH=0 25MM) → SIGNAL_MODEL=EMPTY CRITICAL L6407 220-OHM-25%-2.5A 0603 → AUD_SPKR_RTWT_OUT_P

OUTPUT POLARITY FLIP TO MAKE LAYOUT MORE LOGICAL

PP5V_RAMP_VREG → R6408 10 1% 1/16W MF-LF 402 → AUD_RAMP_REG_OUT (MIN LINE WIDTH=0 40MM, MIN NECK WIDTH=0 20MM)
AUD_RAMP_PLIMIT
AUD_RAMP_FSEL
AUD_RAMP_PBTL

AUD_SPKRAMP_MUTE_L
AUD_GPIO_3 → R6400 0 5% 1/10W MF-LF 402

R6409 0 5% 1/16W MF-LF 402

R6401 100K 5% 1/10W MF-LF 402
NOSTUFF C6412 100PF 5% 50V CERM 402
C6417 2.2UF 20% 10V X5R-CERM 402
NOSTUFF R6410 10K 1% 1/10W MF-LF 402
C6418 1UF 10% 10V X5R 402
R6403 0 5% 1/16W MF-LF 402

CRITICAL C6420 1000PF 5% 25V NP0-C0G 402 → SIGNAL_MODEL=EMPTY
CRITICAL C6422 1000PF 5% 25V NP0-C0G 402 → SIGNAL_MODEL=EMPTY
CRITICAL C6419 1000PF 5% 25V NP0-C0G 402 → SIGNAL_MODEL=EMPTY
CRITICAL C6421 1000PF 5% 25V NP0-C0G 402 → SIGNAL_MODEL=EMPTY

SE-TO-DIFF CONVERTER

AUD_HP_PORT_R → CRITICAL C6453 3.3UF 10% 16V TANT SMA HF1 → AUD_R_SE_DIFF_IN → R6453 21K 1% 1/16W MF LF 402 → AUD_R_SE_DIFF_IN_R → SIGNAL_MODEL=EMPTY R6454 21K 1% 1/16W MF LF 402

AUD_SE_DIFF_SHDN_L

R6460 0 5% 1/16W MF-LF 402 → AUD_GPIO_3
R6461 100K 5% 1/16W MF-LF 402

U6450 MAX4253 UCSP CRITICAL

B4	V-
C3	+
C4	
C1	
C2	−
B1	V+
A2	−
B1	V+
A1	
A3	+
B4	V-
A4	

AUD_HP_R_P
AUD_HP_R_N

SIGNAL_MODEL=EMPTY R6455 2.21K 1% 1/16W MF LF 402
AUD_R_SE_DIFF_P_INV
SIGNAL_MODEL=EMPTY R6457 2.21K 1% 1/16W MF LF 402
SIGNAL_MODEL=EMPTY R6458 2.21K 1% 1/16W MF LF 402
AUD_R_SE_DIFF_N_INV
SIGNAL_MODEL=EMPTY R6456 2.21K 1% 1/16W MF LF 402

PP4V5_AUDIO_ANALOG
C6450 4.7UF 20% 6.3V X5R 402
C6451 0.47UF 10% 10V X5R 402
R6450 21K 1% 1/16W MF LF 402
AUD_SE_DIFF_VBIAS (MIN LINE WIDTH 0 20MM, MIN NECK WIDTH 0 15MM)
R6451 21K 1% 1/16W MF LF 402
CRITICAL C6452 3.3UF 10% 16V TANT SMA HF1
GND_AUDIO_CODEC

SYNC MASTER=K62 DAVID		SYNC DATE=01/09/2011	
PAGE TITLE	AUDIO: SPEAKER AMP 1		
Apple Inc.		DRAWING NUMBER	051-8442
		SIZE	D
		REVISION	10.1.0
		BRANCH	
		PAGE	64 OF 110
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LEFT CH SPEAKER AMP
APPLE P/N 353S3069

R6502 = LOW = 300 KHZ
SPEAKER AMP GAIN = +9 DB
SPEAKER AMP RIN = 210K NOMINAL W/ +9 DB GAIN
FC_HPF, TWEETERS = ~924 HZ (820 PF)
FC_HPF, WOOFERS = ~23 HZ (0.033 UF)

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

OUTPUT POLARITY FLIP TO MAKE LAYOUT MORE LOGICAL

U6500 TPA3117D2 QFN CRITICAL

SE-TO-DIFF CONVERTER

U6550 MAX4253 UCSP CRITICAL

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SYNC MASTER=K62 DAVID	SYNC DATE=01/09/2011
PAGE TITLE: AUDIO: SPEAKER AMP	
Apple Inc.	DRAWING NUMBER 051-8442 SIZE D
	REVISION 10.1.0
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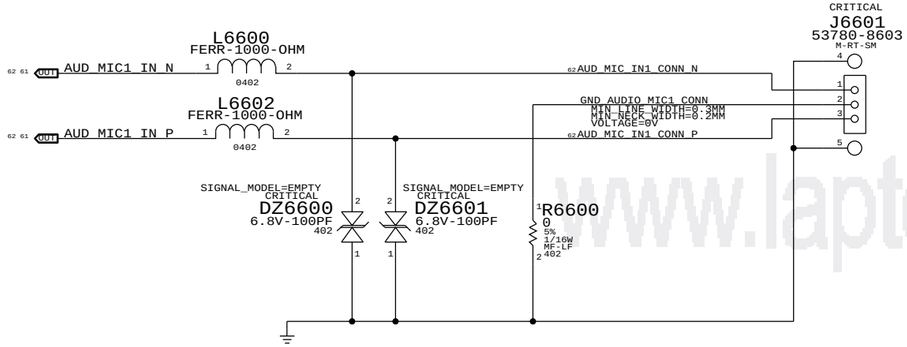
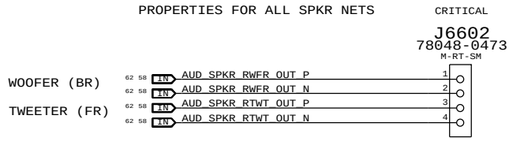
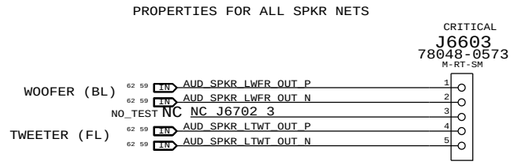
INTERNAL MIC CON
APPLE P/N 518S0677

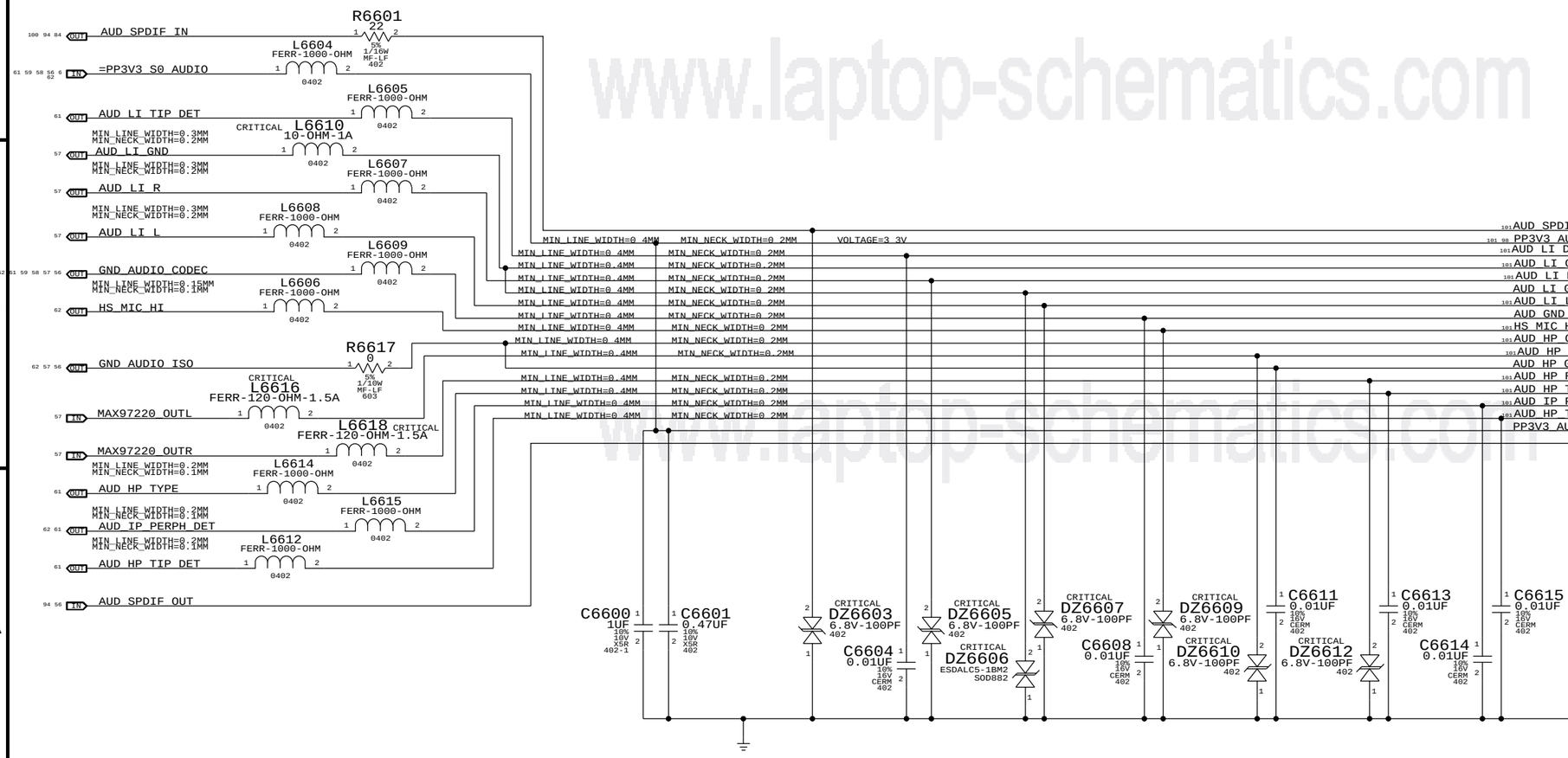


SPEAKER CABLE CONNECTORS
APPLE P/N 518S0748
APPLE P/N 518S0656





REMOTE I/O CONNECTOR
APPLE P/N 518S0723



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SYNC_MASTER=K62_DAVID SYNC_DATE=01/09/2011

PAGE TITLE
Audio: MLB to I/O Conn.

Apple Inc.

DRAWING NUMBER 051-8442 SIZE D
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BRANCH
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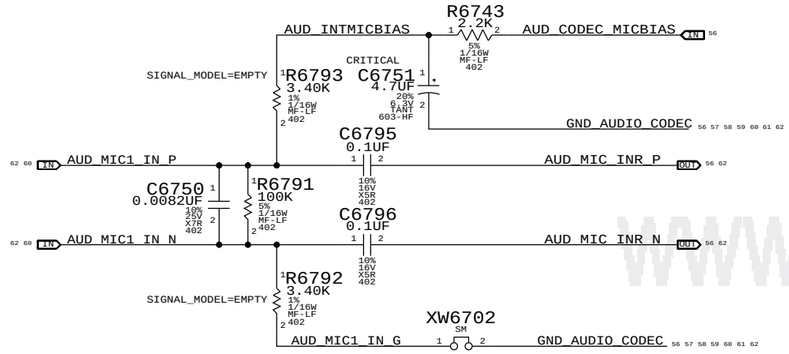
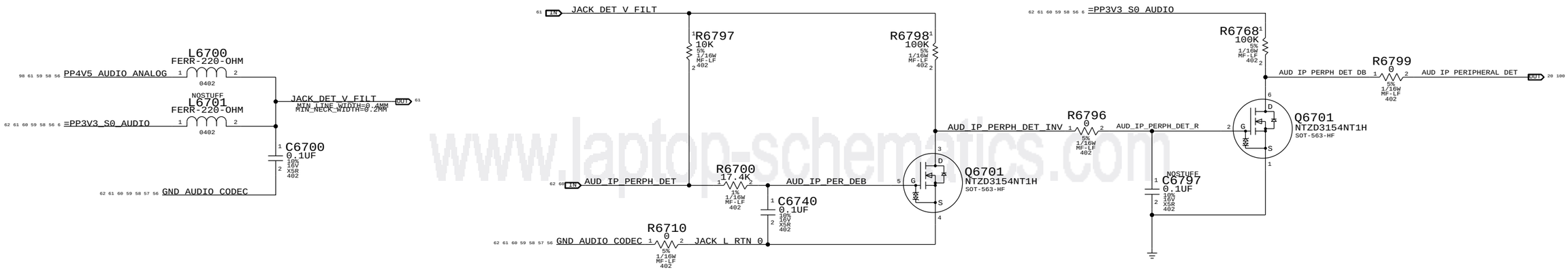
Internal Microphone Impedance Matching



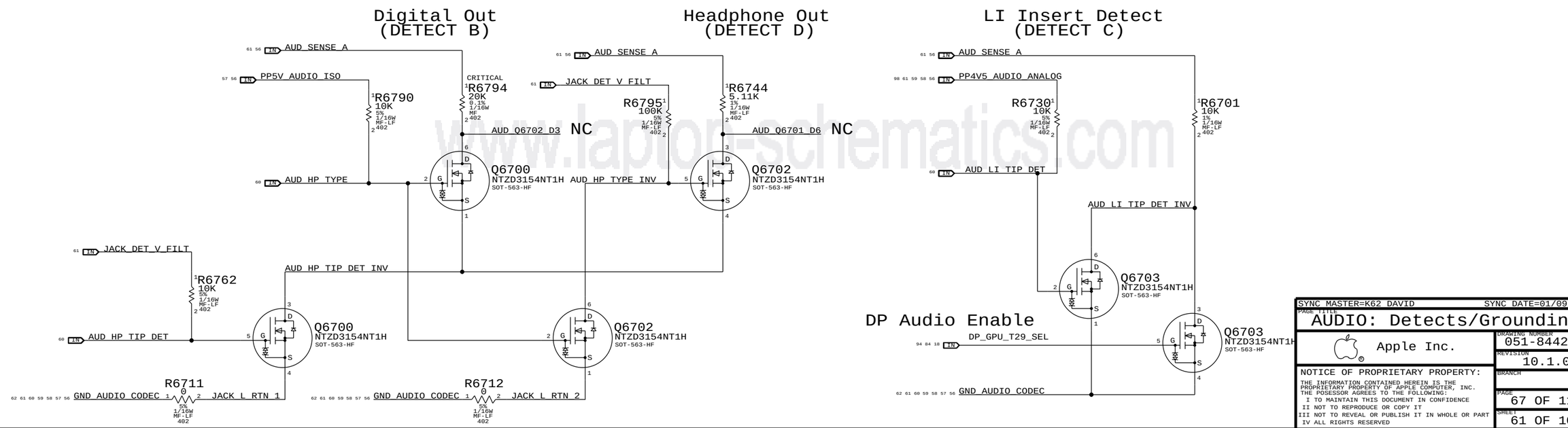
IPHS HS Detect Debounce CKT



Digital Out (DETECT B)

Headphone Out (DETECT D)

LI Insert Detect (DETECT C)



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SYNC MASTER=K62 DAVID SYNC DATE=01/09/2011

PAGE TITLE
AUDIO: Detects/Grounding

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DRAWING NUMBER 051-8442 SIZE D
REVISION 10.1.0
BRANCH
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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	SHDN	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	0X0A (D)
PRIMARY SPKRS (WFR)	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SECONDARY SPKRS (TWT)	0X02 (2)	0X02 (2)	0X09 (09)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	0X0D (B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
LINE IN	0X05 (5)	0X12 (12,C)	N/A	0X12 (C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
INTERNAL MIC	0X06 (6)	0X0E (14,LEFT & RIGHT)	N/A	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	COUGAR POINT GPIO 16	COUGAR POINT GPIO 5 (PCVR_INT) COUGAR POINT GPIO 3 (PERIPH DET)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	0 1 MM	?
SPKROUT	*	0 2 MM	?

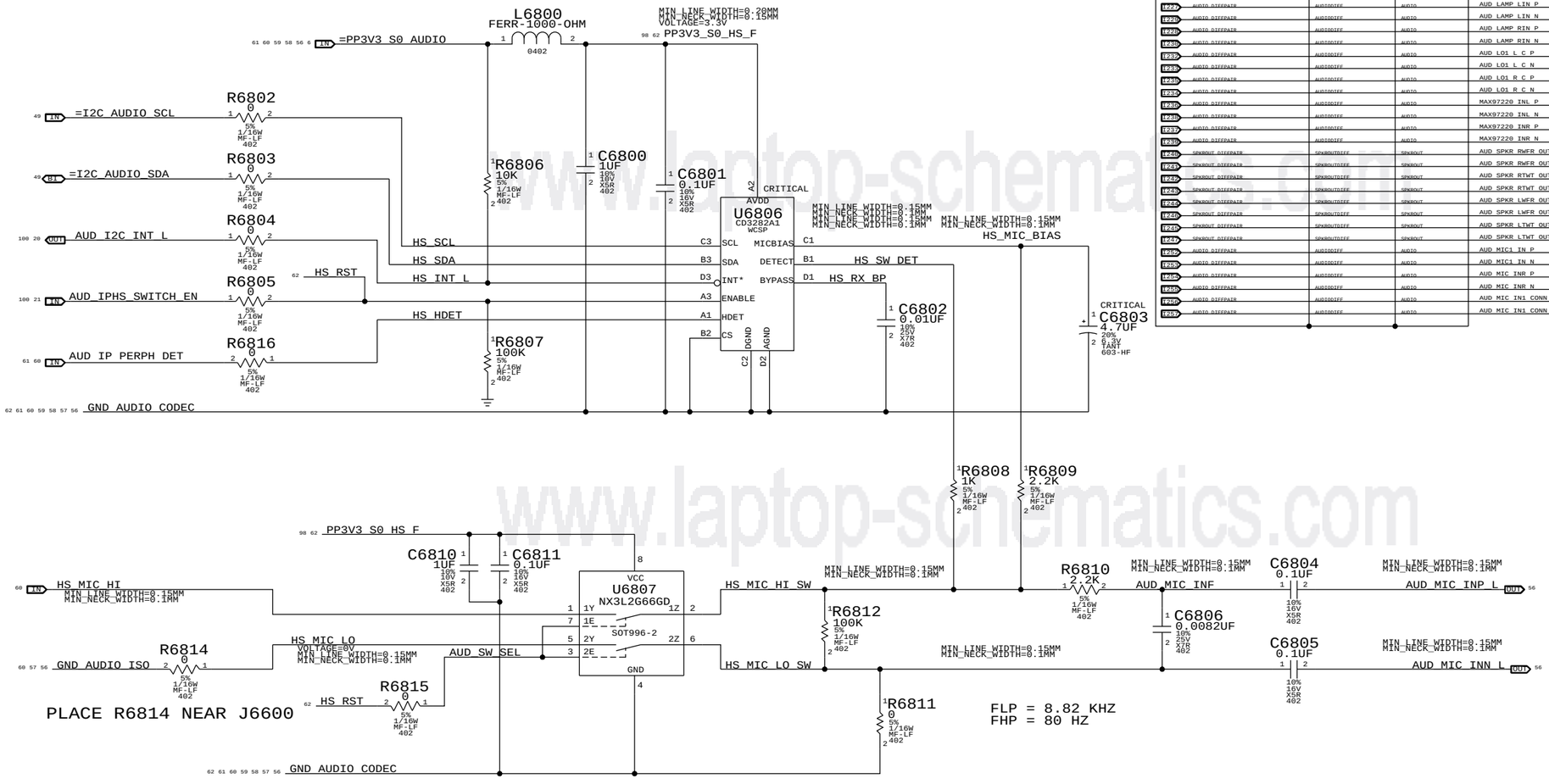
NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
SPKROUTDIFF	*	SPKROUTDIFF

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0 1 MM	0 1 MM	10 MM	0 1 MM	0 1 MM
SPKROUTDIFF	*	Y	0 6 MM	0 25 MM	10 MM	0 2 MM	0 2 MM

ELECTRICAL CONSTRAINT SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_HP_L_P	59
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_HP_L_N	59
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_HP_R_P	58
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_HP_R_N	58
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P	56 57
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_N	56 57
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	56 57
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_N	56 57
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	56 59
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	56 59
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	56 58
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	56 58
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_P	58
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_N	58
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_P	58
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_N	58
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_P	58
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_N	58
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_P	58
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_N	58
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_P	59
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_N	59
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_P	59
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_N	59
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_P	59
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_N	59
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_P	59
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_N	59
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_P	57
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_N	57
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_P	57
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_N	57
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INL_P	57
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INL_N	57
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INR_P	57
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INR_N	57
SPKROUT DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_P	58 60
SPKROUT DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_N	58 60
SPKROUT DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_P	58 60
SPKROUT DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_N	58 60
SPKROUT DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_P	59 60
SPKROUT DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_N	59 60
SPKROUT DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_P	59 60
SPKROUT DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_N	59 60
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC1_IN_P	60 61
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC1_IN_N	60 61
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INR_P	56 61
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INR_N	56 61
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_IN1_CONN_P	60
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_IN1_CONN_N	60

MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2640



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SYNC_MASTER=K62_DAVID SYNC_DATE=01/09/2011

PAGE TITLE: AUDIO: Mikey

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

REVISION: 10.1.0

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SLP_S4 ENABLES

MEMVTT_EN SEQUENCE

=PP3V3_S0_PWRCTL
R6951 10K 5% 1/16W MF-LF 402
R6952 10K 5% 1/16W MF-LF 402
NOSTUFF C6951 100PF 5% 50V CERM 402
PM_EN_DDRVTT_S0_REG 32 63 72 100
NOSTUFF C6953 0.1UF 10% 10V X5R 402
VTT_REG_PGOOD_L
Q6911 MMDT3904-X-G SOT 363 LF
R6950 10K 5% 1/16W MF-LF 402
64 63 PM_PGOOD_P1V05_S0_REG 100 68
CPUVTT_REG_PGOOD_R 100
Q6911 SOT 363 LF
MMDT3904-X-G
NOSTUFF C6952 0.47UF 10% 6.3V CERM-X5R 402

=PP3V3_S5_PWRCTL
R6971 0 5% 1/16W MF-LF 402
100 47 46 19 5 PM_SLP_S5_L
NOSTUFF R6972 0 5% 1/16W MF-LF 402
100 63 47 46 32 19 5 PM_SLP_S4_L
100 PM_SLP_S4_1_L_R
74LVC08 TSSOP-HF U6900 08
S4_ENABLES 100
R6911 33 5% 1/16W MF-LF 402
R6912 33 5% 1/16W MF-LF 402
PM_EN_P3V3_S3_FET 74 100
Enable FET
PM_EN_P5V_S3_REG 71 100
ENABLE REGULATOR

=PP3V3_S5_PWRCTL
R6916 100K 5% 1/16W MF-LF 402
R6915 10K 5% 1/16W MF-LF 402
CPU_SKTOCC 94
100 11 CPU_SKTOCC_L
Q6910 2N7002 SOT23-HF1
NOSTUFF R6917 10K 5% 1/16W MF-LF 402
PLACE TOP SIDE
REWORK TO POWER UP WITH NO CPU

NOSTUFF C6920 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6921 0.47UF 10% 6.3V CERM-X5R 402

100 83 71 63 PM_PGOOD_P5V_S3_REG
R6970 0 5% 1/16W MF-LF 402
PM_EN_USB_PWR 43 94
NOSTUFF C6924 0.47UF 10% 6.3V CERM-X5R 402

=PP3V3_S5_PWRCTL
74LVC08 TSSOP-HF U6900 08
100 63 47 46 32 19 5 PM_SLP_S4_L
100 83 71 63 PM_PGOOD_P5V_S3_REG
PM_EN_DDR1V5_S3_REG 72 100

NOSTUFF R6931 33 5% 1/16W MF-LF 402
100 74 64 63 PM_PGOOD_P3V3_S0_FET
PM_EN_P1V5_S0_FET 63 74 100

SLP_S3 ENABLES

64 63 11 6 =PP3V3_S5_PWRCTL
R6955 10K 5% 1/16W MF LF 402
P3V3_S5_PWRCTL_U6900_R
74LVC08 TSSOP-HF U6900 08
100 64 PGOOD_P12V_S0

OTHER RAILS ENABLED BY P3V3_S0 AND P5V_S0:
PP1V8_S0 VREG (CPU PLL)

NOSTUFF R6946 33 5% 1/16W MF-LF 402
PM_EN_P3V3_S0_FET
Enable FET
OUT 63 74 100
NOSTUFF R6947 33 5% 1/16W MF-LF 402
PM_EN_P5V_S0_FET
Enable FET
OUT 74 100

NOSTUFF R6944 33 5% 1/16W MF LF 402
NOSTUFF R6941 10K 5% 1/16W MF LF 402
PM_SLP_S3_BUF_L 100
Enable FET
PM_EN_P1V5_S0_FET 63 74 100
PM_EN_DDRVTT_S0_REG 32 63 72 100
Enable regulator

64 63 11 6 =PP3V3_S5_PWRCTL
R6934 82K 5% 1/16W MF-LF 402
PM_PGOOD_P5V_S0_FET 63 64 74 100
R6935 33K 5% 1/16W MF-LF 402
100 47 46 36 32 26 19 5 PM_SLP_S3_L
100 72 5 PM_PGOOD_DDR1V5_S3_REG
74LVC08 TSSOP-HF U6900 08
PM_EN_P12V_S0_FET 6 100

OPTION TO DELAY 1V8
100 74 64 63 PM_PGOOD_P3V3_S0_FET
R6932 33 5% 1/16W MF-LF 402
NOSTUFF R6990 33 5% 1/16W MF-LF 402
100 74 64 63 PM_PGOOD_P5V_S0_FET
PM_EN_P1V8_S0_REG 72 100
NOSTUFF C6994 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6947 0.47UF 10% 6.3V CERM-X5R 402

NOSTUFF C6944 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6941 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6945 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6946 0.47UF 10% 6.3V CERM-X5R 402

OPTIONAL SEQUENCE TO DELAY 3V,1V5
100 74 64 63 PM_PGOOD_P5V_S0_FET
R6930 33 5% 1/16W MF-LF 402
PM_EN_P3V3_S0_FET 63 74 100
100 74 64 63 PM_PGOOD_P5V_S0_FET
R6933 33 5% 1/16W MF-LF 402
PM_EN_P1V5_S0_FET 63 74 100

NOSTUFF R6942 33 5% 1/16W MF-LF 402
Enable regulator
PM_EN_P1V05_S0_REG
NOSTUFF C6942 1UF 10% 6.3V CERM 402
100 74 64 63 PM_PGOOD_P3V3_S0_FET
R6936 33 5% 1/16W MF-LF 402
OPTION TO DELAY 1V05

CPUVTT_VREG/ PCH CORE
68 100
100 68 64 63 PM_PGOOD_P1V05_S0_REG
NOTE: PM_PGOOD_P1V05_S0_REG ENABLES VCCSA REGULATOR CIRCUIT ON PAGE 70
PM_PGOOD_P1V05_S0_REG = =PM_EN_VCCSA_S0_CPU
MAKE_BASE=TRUE

VCCSA REGULATOR
100 64
PM_PGOOD_PVCCSA_S0_REG = Enable regulator PM_EN_PVCORE_CPU 65 100
MAKE_BASE=TRUE
TO ENABLE OF CPU VCORE

SYNC_MASTER=K62_SIJI SYNC_DATE=01/09/2011
PAGE TITLE
POWER SEQUENCING ENABLES

Apple Inc.

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SIZE D
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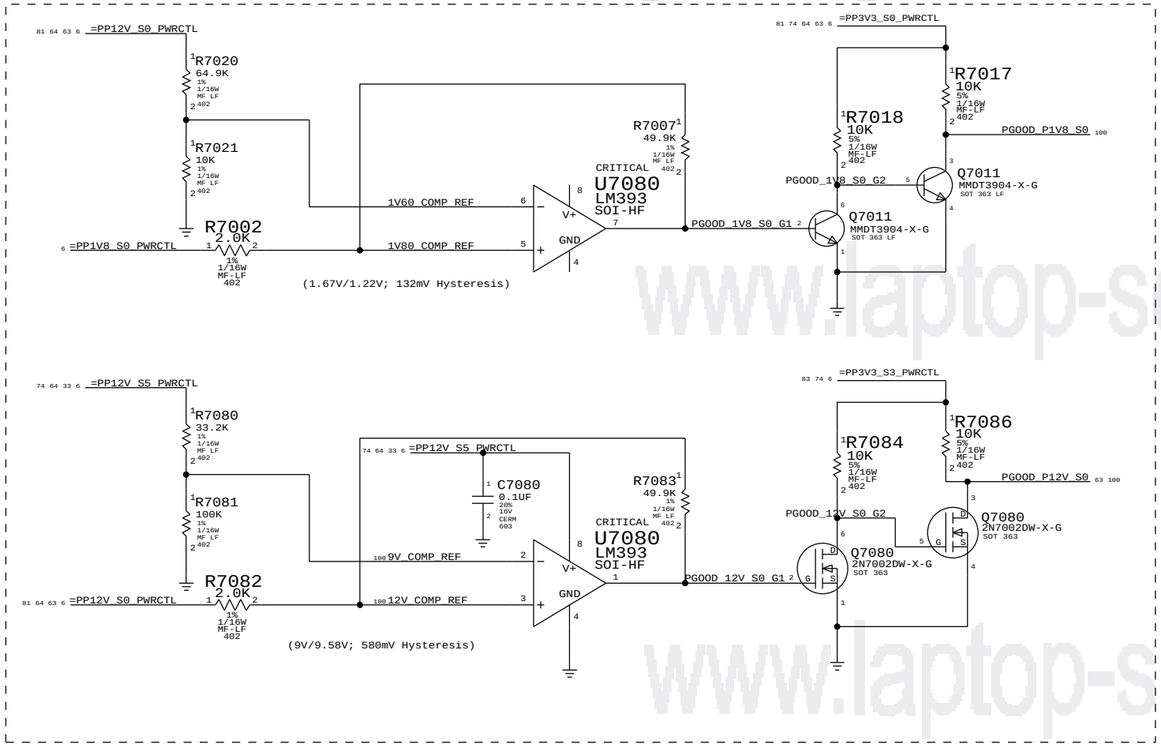
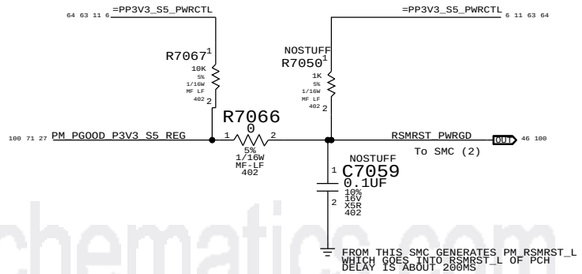
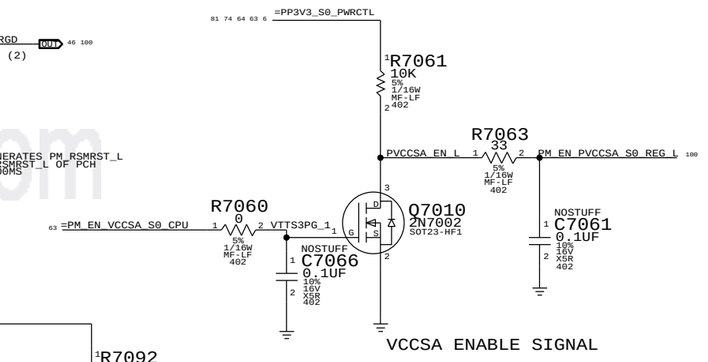
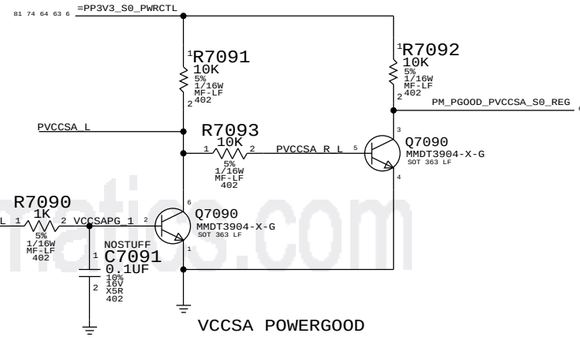
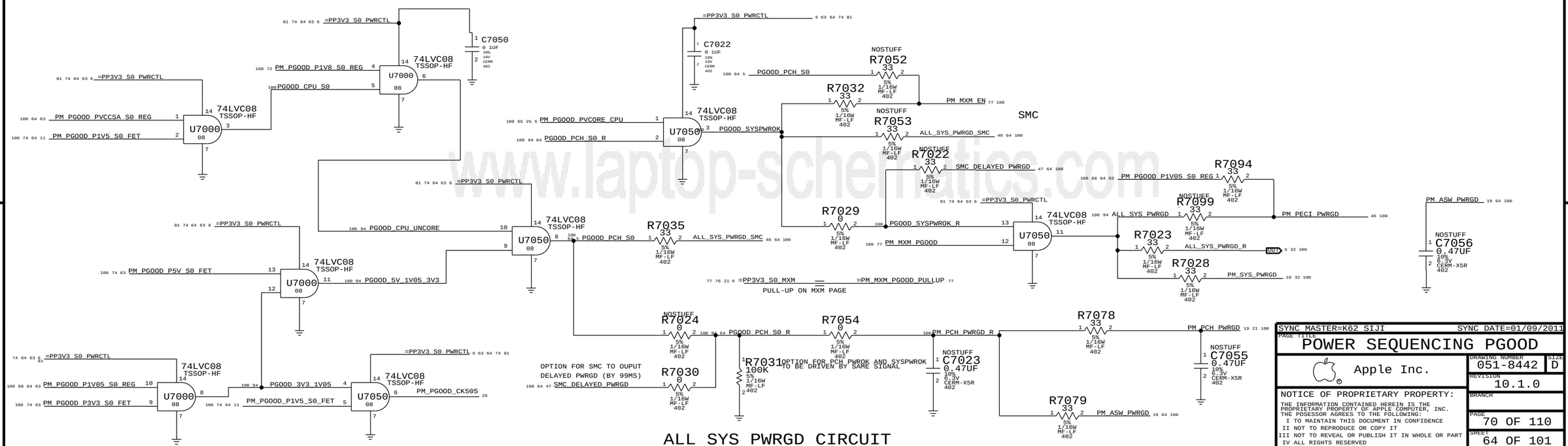
PGOOD COMPARATORS FOR PP1V8_S0 AND PP12V_S0











SYNC_MASTER=K62_SIJI SYNC_DATE=01/09/2011

PAGE TITLE: POWER SEQUENCING PGOOD

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

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CPU CORE/AXG REG 1.1V/75A O/P= PPVCORE_S0_CPU_REG

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=PPVAXG_S0_CPU
R7160 1K
R7162 10
R7161 0
VR_AXG_VSEN
SIGNAL_MODEL=EMPTY
CPU_VAXG_SENSE_P
CPU_VAXG_SENSE_N
1.25 mOhm loadline
NOSTUFF C7155 0.0022UF
R7163 0
R7164 10
VR_AXG_RGND
XW7130
R7165 1K
C7156 0.0022UF
C7157 0.0022UF
AGND_CPU
=PP5V_S0_VRD
R7127 2.2
PP5V_S0_CPU_VCORE_VCC
MAX_NECK_LENGTH=3MM
MIN_NECK_WIDTH=0.3MM
MIN_LINE_WIDTH=0.6MM
VOLTAGE=5V
=PP3V3_S0_VRD
R7195 10K
CPU VCORE
VOUT = VCORE
PEAK = 75A
AVG = 55A
R7157 1K
C7114 10UF
R7189 1K
R7103 6.8K
C7113 0.1UF
NOSTUFF R7101 0
NOSTUFF R7102 0
NOSTUFF R7104 0
CPUVCORE-3PH R7106 0
VR_AXG_PWM
R7107 0
C7116 0.0022UF
R7128 249
VR_SEN_R2
OMIT R7129 0
OMIT R7130 806
VR_SEN_R1
R7131 10
VR_SEN_R3
NOSTUFF R7103 0
NOSTUFF R7105 0
R7108 110
C7100 220PF
C7101 0.1UF
C7102 220PF
DIFFERENTIAL PAIR=VR AXG ISNS
VR_AXG_ISNS_P
VR_AXG_ISNS_N
R7132 9.09K
C7117 3900PF
VR_AXG_COMP_RC
C7118 39PF
NOSTUFF C7115 0.01UF
LOCAL 5V
VCC
U7100
ISL6364
QFN
R7100 0
VR_AXG_PWM_R
R7109 1.02K
R7141 OMIT 1.21K
VR_AXG_HFREQ_COMP
VR_AXG_FB
VR_AXG_COMP
PM_PGOOD_PVCORE_CPU
R7110 0
VR_CPU_PWM1
VR_CPU_ISNS1_P
VR_CPU_ISNS1_N
C7103 220PF
C7104 0.1UF
R7111 1.02K
C7119 4700PF
R7133 301
VR_CPU_PSICOMP2
VR_CPU_PSICOMP1
R7134 249
VR_CPU_FB_RC
C7120 390PF
PP5V_S0_CPU_VCORE_VCC
R7156 953K
R7140 953K
R7142 OMIT 16.5K
R7143 15.0K
CPU_VIDSCLK
CPU_VIDALERT_L
CPU_VIDSOUT
R7112 0
VR_CPU_PWM2
VR_CPU_ISNS2_P
VR_CPU_ISNS2_N
C7105 220PF
C7106 0.1UF
R7113 1.02K
R7135 1.33K
OMIT R7136 1.02K
R7121 10
VR_CPU_FB_R
R7144 OMIT 2.55K
VR_CPU_HFREQ_COMP
VR_CPU_FB
VR_CPU_PSICOMP
VR_CPU_COMP
VR_CPU_IAUTO
VR_CPU_IMON
R7114 0
VR_CPU_PWM3
VR_CPU_ISNS3_P
VR_CPU_ISNS3_N
C7107 220PF
C7108 0.1UF
R7115 1.02K
C7122 82PF
R7145 4.99K
OMIT C7123 820PF
VR_CPU_FB2
CPU_PROCHOT_L
R7199 0
VR_HOT_L
VR_CPU_TM
R7184 0
VR_CPU_PWM4
VR_CPU_ISNS4_P
VR_CPU_ISNS4_N
C7187 220PF
C7188 0.1UF
R7185 1.02K
R7149 30.1K
OMIT R7150 26.1K
R7151 255K
R7158 255K
R7120 124K
R7155 105K
R7118 1.18M
R7119 12.4K
R7122 100K
R7123 2.74K
R7124 6.65K
R7181 10K
R7180 100K
PP12V_S0_CPU_FLTRD
PP5V_S0_CPU_VCORE_VCC
R7146 110
NOSTUFF R7147 90.9
R7148 54.9
C7124 0.01UF
R7152 0
=PPVCCIO_S0_CPU
C7126 0.1UF
NOSTUFF R7179 100K
R7159 1K
R7104 6.8K
C7132 0.1UF
THRM PAD 49
R7153 845
C7127 27.0NF
OMIT R7154 9.76K
VR_CPU_IMON_R
VR_EN_PWR_OVP_R
C7112 0.1UF
=PPVCORE_S0_CPU
R7166 1K
R7167 10
VR_CPU_VSEN
SIGNAL_MODEL=EMPTY
R7168 0
VR_CPU_VSNS_R_P
CPU_VCC_SENSE_P
CPU_VCC_SENSE_N
1.25 mOhm loadline
NOSTUFF C7158 0.0022UF
R7169 0
R7170 10
VR_CPU_RGND
XW7133
R7171 1K
C7159 0.0022UF
C7160 0.0022UF
AGND_CPU
152-0118
CRITICAL
L7100
0.24UH+/-20%-0.000420HM-40A
SDP1108M-TH
=PP12V_S0_VRD
PP12V_S0_CPU_FLTRD
NET PHYSICAL_TYPE=POWER
VOLTAGE=12V
CPU CORE INPUT FILTER
OMIT XW7101 SM
R7125 1K
C7111 0.1UF
OMIT R7126 13.7K
VR_AXG_IMON_R
AGND_CPU

SYNC_MASTER=K62_AARON	SYNC_DATE=N/A
PAGE TITLE	VREG: PPVCORE S0 CPU
Apple Inc.	DRAWING NUMBER 051-8442 SIZE D
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PHASE 1

PP12V_S0_CPU_FLTRD
NET_SPACING_TYPE=POWER
CRITICAL C7272 220UF 20% 2V ALUM-POLY 8X7-TH
CRITICAL C7270 220UF 20% 2V ALUM-POLY 8X7-TH
CRITICAL C7271 220UF 20% 16V ALUM-POLY 8X7-TH
R7202 10 5% 1/10W MF-LF 603
R7205 0 5% 1/10W MF-LF 603
NOSTUFF R7201 10 5% 1/10W MF-LF 603
VR_CPU_DRV1_PVCC
NET_PHYSICAL_TYPE=POWER NO_TEST=TRUE
C7201 1UF 10% 16V X5R 603
VR_CPU_BOOT1_RC
NET_PHYSICAL_TYPE=VR_CTL_PHY NET_SPACING_TYPE=VR_CONTROL DIDT=TRUE NO_TEST=TRUE
R7204 0 5% 1/10W MF-LF 603
C7203 0.22UF 10% 16V X7R 603
VR_CPU_DRV1_VCC
NET_PHYSICAL_TYPE=POWER NO_TEST=TRUE
VR_CPU_DRV1_UVCC
NET_PHYSICAL_TYPE=POWER NO_TEST=TRUE
VR_CPU_DRV1_GDSEL
U7201 ISL6622 DFN
VCC UVCC LVCC GDSEL BOOT UGATE PHASE LGATE PWM GND THRML PAD
VR_CPU_DRV1_BOOT
NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=VR_CONTROL NO_TEST=TRUE
VR_CPU_DRV1_UGATE
NO_TEST=TRUE NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=VR_CONTROL
VR_CPU_PHASE1
NET_PHYSICAL_TYPE=POWER DIDT=TRUE NET_SPACING_TYPE=SWITCHNODE
VR_CPU_DRV1_LGATE
NO_TEST=TRUE NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=VR_CONTROL
C7202 1UF 10% 16V X5R 603
C7200 1UF 10% 16V X5R 603
NOSTUFF R7207 0 5% 1/10W MF-LF 603
VR_CPU_PWM1
CRITICAL Q7201 IRF6710 S1
376S0772
CRITICAL L7201 0.24UH+/-20%-0.000420HM-40A SDP1108M-TH
SWITCH_NODE=TRUE
PPVCORE_S0_CPU_REG1
CRITICAL C7205 220UF 20% 2V ALUM-POLY 8X7-TH
CRITICAL C7206 10UF 10% 16V X5R-CERM 0805
CRITICAL C7215 10UF 10% 16V X5R-CERM 0805
C7207 1UF 10% 16V X5R 603
C7281 1UF 10% 16V X5R 603
THESE TWO CAPS ARE FOR EMC
C7210 0.001UF 10% 50V X7R 402
C7211 1UF 10% 25V X5R 402
CRITICAL R7208 0.0005 1% 1W MF 0612
PPVCORE_S0_CPU_REG
NOSTUFF R7206 2.2 5% 1/8W MF-LF 805
VR_CPU_PH1_SNUB
NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=SWITCHNODE
C7208 0.001UF 10% 50V CERM 402 NOSTUFF
CRITICAL Q7202 IRF6795 DIRECTFET-MX
376S0771
VR_CPU_ISNS1_P
VR_CPU_ISNS1_N

PHASE 2

R7222 10 5% 1/10W MF-LF 603
NOSTUFF R7225 0 5% 1/10W MF-LF 603
R7221 10 5% 1/10W MF-LF 603
VR_CPU_DRV2_VCC
NET_PHYSICAL_TYPE=POWER NO_TEST=TRUE
VR_CPU_DRV2_UVCC
NET_PHYSICAL_TYPE=POWER
VR_CPU_DRV2_PVCC
NET_PHYSICAL_TYPE=POWER NO_TEST=TRUE
C7221 1UF 10% 16V X5R 603
VR_CPU_BOOT2_RC
NET_PHYSICAL_TYPE=VR_CTL_PHY NET_SPACING_TYPE=VR_CONTROL DIDT=TRUE NO_TEST=TRUE
R7224 0 5% 1/10W MF-LF 603
C7223 0.22UF 10% 16V X7R 603
C7222 1UF 10% 16V X5R 603
NOSTUFF C7220 1UF 10% 16V X5R 603
U7221 ISL6612 QFN1
VCC PVCC PWM BOOT UGATE PHASE LGATE GND THRML PAD
VR_CPU_DRV2_BOOT
NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=VR_CONTROL NO_TEST=TRUE
VR_CPU_DRV2_UGATE
NO_TEST=TRUE NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=VR_CONTROL
VR_CPU_PHASE2
NET_PHYSICAL_TYPE=POWER DIDT=TRUE NET_SPACING_TYPE=SWITCHNODE
VR_CPU_DRV2_LGATE
NO_TEST=TRUE NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=VR_CONTROL
VR_CPU_PWM2
VR_CPU_DRV2_GDSEL
NOSTUFF R7227 0 5% 1/10W MF-LF 603
376S0772
CRITICAL Q7221 IRF6710 S1
CRITICAL L7221 0.24UH+/-20%-0.000420HM-40A SDP1108M-TH 152-0118
SWITCH_NODE=TRUE
PPVCORE_S0_CPU_REG2
CRITICAL C7225 220UF 20% 2V ALUM-POLY 8X7-TH
CRITICAL C7226 10UF 10% 16V X5R-CERM 0805
CRITICAL C7229 10UF 10% 16V X5R-CERM 0805
C7282 1UF 10% 16V X5R 603
C7227 1UF 10% 16V X5R 603
THESE TWO CAPS ARE FOR EMC
C7230 0.001UF 10% 50V X7R 402
C7231 1UF 10% 25V X5R 402
CRITICAL R7228 0.0005 1% 1W MF 0612
PPVCORE S0 CPU REG
NOSTUFF R7226 2.2 5% 1/8W MF-LF 805
VR CPU PH2 SNUB
NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=SWITCHNODE
C7228 0.001UF 10% 50V CERM 402 NOSTUFF
CRITICAL Q7222 IRF6795 DIRECTFET-MX
376S0771
VR_CPU_ISNS2_P
VR_CPU_ISNS2_N

PHASE 3

376S0772
R7242 10 5% 1/10W MF-LF 603
NOSTUFF R7245 0 5% 1/10W MF-LF 603
R7241 10 5% 1/10W MF-LF 603
VR_CPU_DRV3_VCC
NO_TEST=TRUE NET_PHYSICAL_TYPE=POWER
VR_CPU_DRV3_UVCC
NET_PHYSICAL_TYPE=POWER
VR_CPU_DRV3_PVCC
NET_PHYSICAL_TYPE=POWER NO_TEST=TRUE
C7241 1UF 10% 16V X5R 603
VR_CPU_BOOT3_RC
NET_PHYSICAL_TYPE=VR_CTL_PHY NET_SPACING_TYPE=VR_CONTROL DIDT=TRUE NO_TEST=TRUE
R7244 0 5% 1/10W MF-LF 603
C7243 0.22UF 10% 16V X7R 603
C7242 1UF 10% 16V X5R 603
NOSTUFF C7240 1UF 10% 16V X5R 603
U7241 ISL6612 QFN1
VCC PVCC PWM BOOT UGATE PHASE LGATE GND THRML PAD
VR_CPU_DRV3_BOOT
NO_TEST=TRUE NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=VR_CONTROL
VR_CPU_DRV3_UGATE
NO_TEST=TRUE NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=VR_CONTROL
VR_CPU_PHASE3
NET_PHYSICAL_TYPE=POWER DIDT=TRUE NET_SPACING_TYPE=SWITCHNODE
VR_CPU_DRV3_LGATE
NO_TEST=TRUE NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=VR_CONTROL
VR_CPU_PWM3
VR_CPU_DRV3_GDSEL
NOSTUFF R7247 0 5% 1/10W MF-LF 603
CRITICAL Q7241 IRF6710 S1
CRITIICAL L7241 0.24UH+/-20%-0.000420HM-40A SDP1108M-TH 152-0118
SWITCH_NODE=TRUE
PPVCORE_S0_CPU_REG3
CRITICAL C7245 220UF 20% 2V ALUM-POLY 8X7-TH
CRITICAL C7246 10UF 10% 16V X5R-CERM 0805
CRITICAL C7249 10UF 10% 16V X5R-CERM 0805
C7283 1UF 10% 16V X5R 603
C7247 1UF 10% 16V X5R 603
THESE TWO CAPS ARE FOR EMC
C7250 0.001UF 10% 50V X7R 402
C7251 1UF 10% 25V X5R 402
CRITICAL R7248 0.0005 1% 1W MF 0612
PPVCORE_S0_CPU_REG
NOSTUFF R7246 2.2 5% 1/8W MF-LF 805
VR_CPU_PH3_SNUB
NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=SWITCHNODE
C7248 0.001UF 10% 50V CERM 402 NOSTUFF
CRITICAL Q7242 IRF6795 DIRECTFET-MX
376S0771
VR_CPU_ISNS3_P
VR_CPU_ISNS3_N

OUTPUT BULK DECOUPLING:

128S0209
PPVCORE S0 CPU REG
75A MAX
C7260 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM
C7261 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM
C7262 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM
C7263 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM
C7264 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM
C7265 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM

SYNC MASTER=K62 AARON
SYNC DATE=N/A
PAGE TITLE
VREG: CPU CORE - PHASES 1-3
Apple Inc.
DRAWING NUMBER 051-8442
SIZE D
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BRANCH
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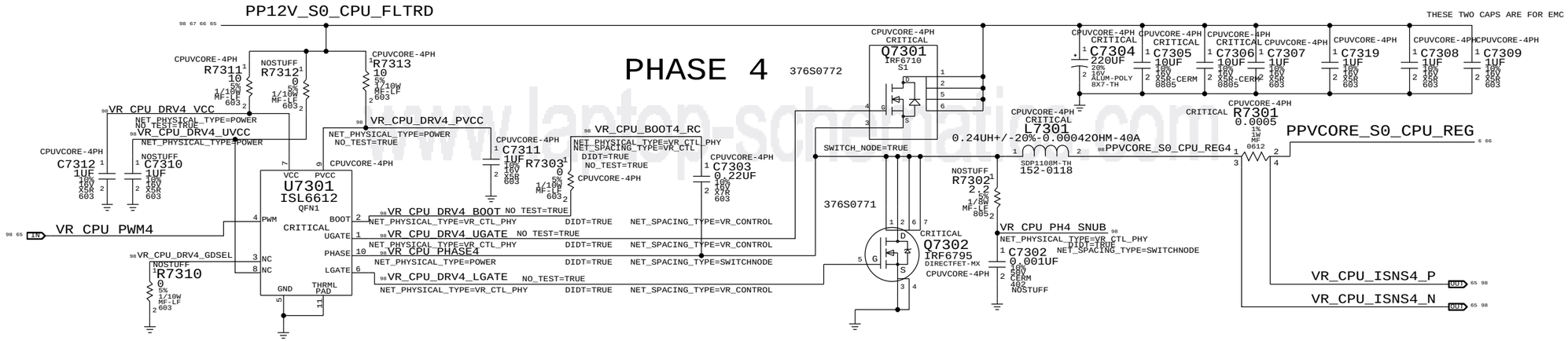
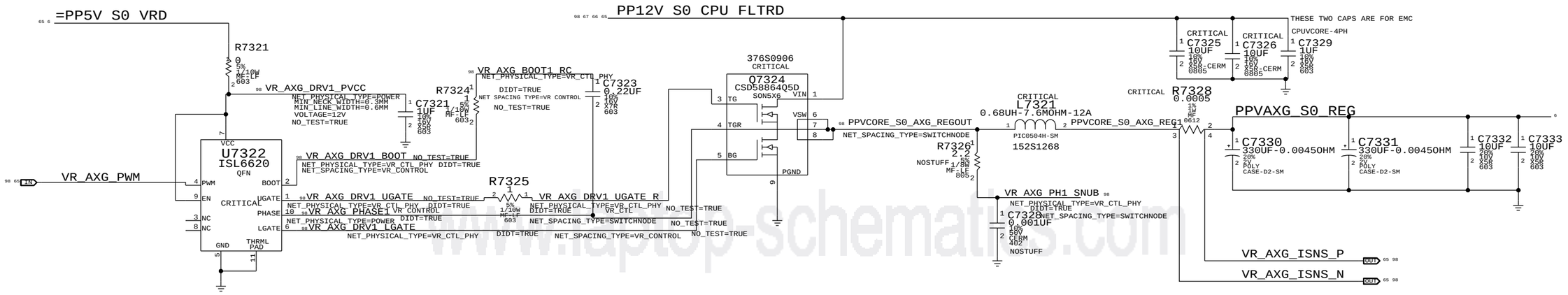


AXG PHASE (MAX 15A)



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SYNC_MASTER=K62_AARON SYNC_DATE=N/A

PAGE TITLE
VREG:AXG PHASE/CORE - CAPS

Apple Inc.

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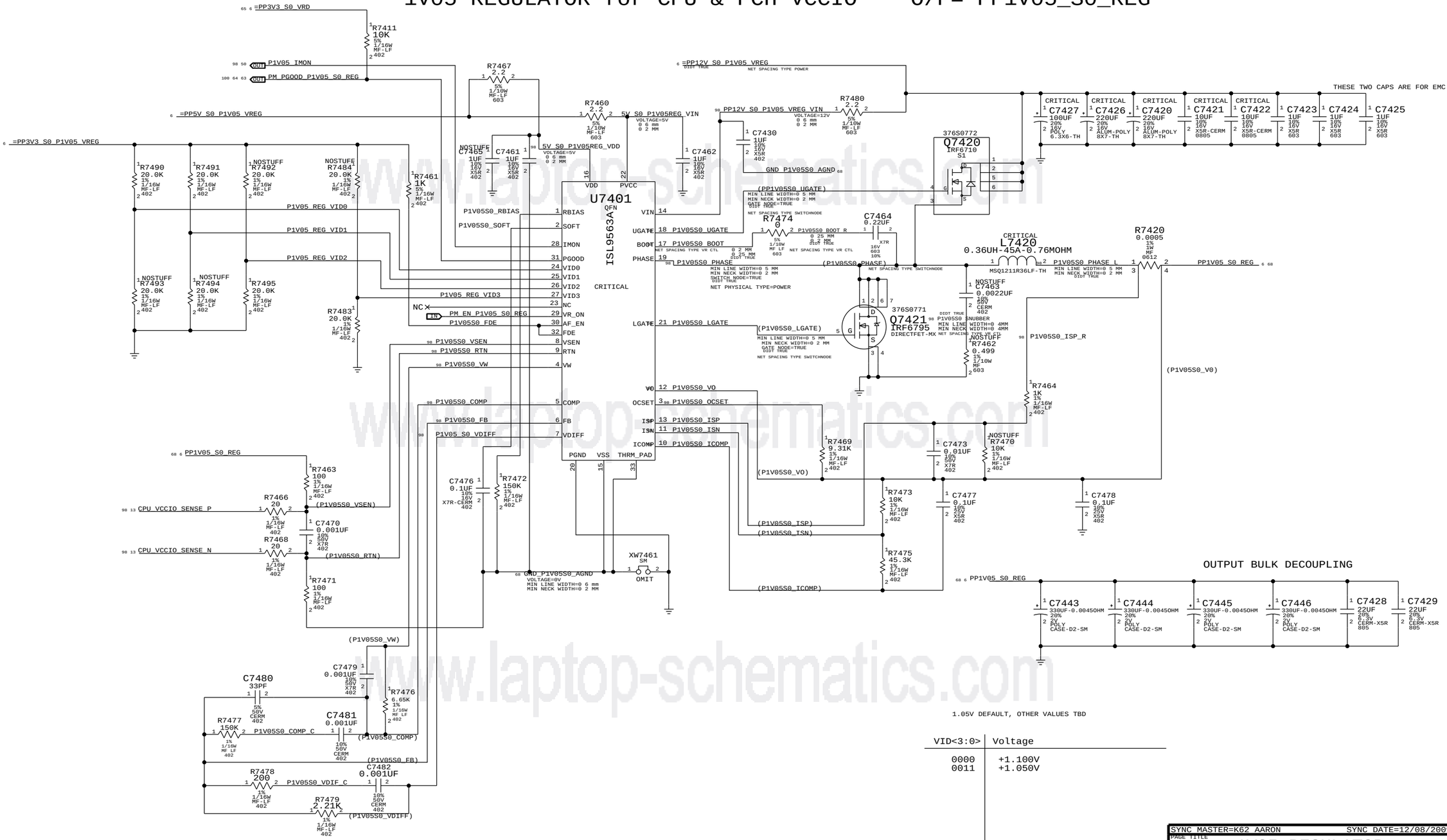
1V05 REGULATOR for CPU & PCH VCCIO O/P= PP1V05_S0_REG



VID<3:0>	Voltage
0000	+1.100V
0011	+1.050V

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SYNC MASTER=K62 AARON SYNC DATE=12/08/2009

PAGE TITLE: 1V05 REGULATOR

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DRAWING NUMBER: 051-8442 SIZE: D

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CPU VCCSA 0.925V (8.8A MAX)

=PP3V3_S5_CPU_VCCSA

R7531 100 5% 1/10W MF-LF 402

VCCSA_REF

CRITICAL
U7505 ISL21070 SOT23-3
VIN VOUT GND

C7515 1UF 10% 10V X5R 402

C7516 1UF 10% 10V X5R 402

C7551 10PF 5% 50V CERM 402

R7550 49.9K 1% 1/16W MF-LF 402

VCCSA_FIL

C7550 560PF 10% 50V CERM 402

=PPVCCIO_S0_CPU_VCCSA

NOTE: THIS RAIL IS COMING FROM PPVCCSA_S0_INPUT_SNS AFTER SENSE RES

R7505 0 5% 1/10W MF-LF 402

VCCSA_GATE

NET_PHYSICAL_TYPE=VR_CTL_PHY
DIDT=TRUE
NET_SPACING_TYPE=VR_CTL

Q7500 IRFH3702TRPBF PQFN
376S0910

VCCSA_CNTRL_INPUT1

LM358-SOI-HF U7501

VCCSA_OUT

NET_PHYSICAL_TYPE=VR_CTL_PHY
DIDT=TRUE
NET_SPACING_TYPE=VR_CTL

NOSTUFF
R7506 1K 5% 1/10W MF-LF 402

NET_PHYSICAL_TYPE=POWER
DIDT=TRUE
NET_SPACING_TYPE=POWER

PPVCCSA_S0_FET

CRITICAL
OMIT_TABLE
C7509 220UF-25MOHM 20% 6V POLY-TANT CASE-D2E-SM

CRITICAL
OMIT_TABLE
C7510 220UF-25MOHM 20% 6V POLY-TANT CASE-D2E-SM

C7507 10UF 10% 6.3V X5R 805

C7508 10UF 10% 6.3V X5R 805

Place C7507 inside cavity
Place C7508 inside cavity

=PP12V_S0_CPU_VCCSA

R7504 2.2 5% 1/10W MF-LF 603

VCCSA_PWR_RC

C7502 1UF 10% 25V X5R 603-1

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0330	2	POLYTANT,6V,220UF,25MOHM	C7509,C7510	

VCCSA_CNTRL_INPUT2

R7507 5.49K 1% 1/10W MF-LF 402

VCCSA_CNTRL_INPUT2_R

R7535 22 5% 1/10W MF-LF 402

R7533 10K 1% 1/16W MF-LF 402

NOSTUFF
C7512 10PF 5% 50V CERM 402

R7552 1K 5% 1/10W MF-LF 402

VCCSA_CRL

C7552 560PF 10% 50V CERM 402

CPU_VCCSA_SENSE

R7503 0 5% 1/10W MF-LF 402

C7501 100PF 5% 50V CERM 402

=PPVCCSA_S0_INPUT_PWR

CRITICAL
C7506 330UF-0.009OHM 20% 2V POLY CASE-D2-HF

C7504 4.7UF 20% 6.3V X5R-CERM1 402

C7505 0.1UF 20% 10V CERM 402

LM358-SOI-HF U7501

NOTE: THIS POWER RAIL IS BEFORE THE SENSE RES R5310

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CPU VCCSA REGULATOR

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CPU VCORE 3 PHASE/4 PHASE BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0066	1	RES,1K,5%,0402	R7125	CPUVCORE-4PH
114S0303	1	RES,7.5K,5%,0402	R7125	CPUVCORE-3PH
114S0327	1	RES,13.7K,1%,0402	R7126	CPUVCORE-4PH
114S0316	1	RES,10.2K,1%,0402	R7126	CPUVCORE-3PH
114S0323	1	RES,12.4K,1%,0402	R7119	CPUVCORE-4PH
114S0316	1	RES,10.2K,1%,0402	R7119	CPUVCORE-3PH
114S0355	1	RES,26.1K,1%,0402	R7150	CPUVCORE-4PH
114S0338	1	RES,17.8K,1%,0402	R7150	CPUVCORE-3PH
114S0211	1	RES,845,1%,0402	R7153	CPUVCORE-4PH
116S0004	1	RES,0,1%,0402	R7153	CPUVCORE-3PH
114S0314	1	RES,9.76K,1%,0402	R7154	CPUVCORE-4PH
114S0316	1	RES,10.2K,1%,0402	R7154	CPUVCORE-3PH
114S0225	1	RES,1.21K,1%,0402	R7141	CPUVCORE-4PH
114S0217	1	RES,976,1%,0402	R7141	CPUVCORE-3PH
114S0335	1	RES,16.5K,1%,0402	R7142	CPUVCORE-4PH
114S0349	1	RES,23.2K,1%,0402	R7142	CPUVCORE-3PH
114S0331	1	RES,15K,1%,0402	R7143	CPUVCORE-3PH
114S0257	1	RES,2.55K,1%,0402	R7144	CPUVCORE-4PH
114S0252	1	RES,2.32K,1%,0402	R7144	CPUVCORE-3PH
114S0209	1	RES,806,1%,0402	R7130	CPUVCORE-4PH
114S0188	1	RES,487,1%,0402	R7130	CPUVCORE-3PH
116S0004	1	RES,0R,1%,0402	R7129	CPUVCORE-4PH
114S0189	1	RES,499,1%,0402	R7129	CPUVCORE-3PH
114S0219	1	RES,1.02K,1%,0402	R7136	CPUVCORE-4PH
114S0131	1	RES,130,1%,0402	R7136	CPUVCORE-3PH
132S8221	1	CAP,820PF,10%,0402	C7123	CPUVCORE-4PH
132S1534	1	CAP,0.0012UF,10%,0402	C7123	CPUVCORE-3PH

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PAGE TITLE
CPU 3P/4P BOM OPTIONS

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3V3 S5 REGULATOR

5V S3 REGULATOR

Power Rating ?

3V3 OUTPUT

5V OUTPUT

=PP12V_S5_P5VS3_VREG

NET SPACING TYPE=POWER

EMC CAPS
PLACE CLOSE TO FET

C7718 100UF 20% 16V POLY 6 3X6 TH
C7712 10UF 10% 16V X5R CERM 0805
C7710 10UF 10% 16V X5R CERM 0805
C7711 1UF 10% 16V X5R 603
C7722 1UF 10% 16V X5R 603

NET_PHYSICAL_TYPE=POWER
DIDT TRUE

C7719 100UF 20% 16V POLY 6 3X6 TH
C7766 100UF 20% 16V POLY 6 3X6 TH
C7767 100UF 20% 16V POLY 6 3X6 TH
C7768 100UF 20% 16V POLY 6 3X6 TH
C7758 10UF 10% 16V X5R CERM 0805
C7765 10UF 10% 16V X5R CERM 0805

=PP3V3_S5_VRD 6

R7726 20K 5% 1/16W MF-LF 402

PP5V_S5_LDO 6

EMC: C7754,C7755
PLACE AT Q7330

C7754 1UF 10% 16V X5R 603
C7755 1UF 10% 16V X5R 603

=PP12V_S5_P5VS3_VREG 6 71

NOSTUFF
R7725 20K 5% 1/16W MF-LF 402

PP3V3_S5_REG

R7776 0.002 1% 1/4W MF LF 1206

CRITICAL
L7710 2.2UH-14A MMD06CZ-SM

PP3V3_S5_REG_R 98
NET_PHYSICAL_TYPE=POWER

C7790 0.01UF 10% 16V CERM 402
R7790 15.8K 1% 1/16W MF LF 402
R7791 15.8K 1% 1/16W MF LF 402

C7730 1000PF 5% 25V NP0-C0G 402 NOSTUFF
DIDT TRUE

NET SPACING TYPE=VR CTL
R7730 0.499 1% 1/10W MF 603 NOSTUFF

P3V3S5 REG SNUB 98
DIDT TRUE

C7714 0.1UF 10% 50V X7R 603
R7710 0 5% 1/10W MF LF 603

98 P3V3S5_REG_BOOT_R
MIN NECK WIDTH=0 2MM
MIN LINE WIDTH=0 6MM
DIDT TRUE
NET SPACING TYPE=VR CONTROL
(P3V3S5 PHASE)

NET SPACING TYPE=VR CONTROL
MIN NECK WIDTH=0 2MM
MIN LINE WIDTH=0 6MM
DIDT TRUE

MIN NECK WIDTH=0 2MM
MIN LINE WIDTH=0 6MM
NET SPACING TYPE=SWITCHNODE
NET PHYSICAL TYPE=POWER

Q7710 RJK0384DPA WPAK 376S0801
D1
G1 1 (P3V3S5 UGATE)
MIN NECK WIDTH=0 2MM
MIN LINE WIDTH=0 6MM
GATE NODE=TRUE
NET SPACING TYPE=VR CONTROL
S1/D2 7
G2 6 (P3V3S5_LGATE)
MIN NECK WIDTH=0 2MM
MIN LINE WIDTH=0 6MM
GATE NODE=TRUE
NET SPACING TYPE=VR CONTROL
S2

NET_PHYSICAL_TYPE=POWER

C7742 4.7UF 20% 6.3V CERM 603
R7740 2.2 5% 1/8W MF-LF 805
R7741 1 5% 1/8W MF-LF 805

P5V_S5_LDO_R
P5V_S5_VCC1

C7740 1UF 10% 16V X5R 603
C7741 1UF 10% 16V X5R 603
C7743 1UF 10% 16V X5R 603

PM_PGOOD_P5V_S3_REG 63 83 100

CRITICAL
Q7750 FDMS0346 POWER56 376S0875

MIN LINE WIDTH=0 6MM
MIN NECK WIDTH=0 2 MM
NET_SPACING_TYPE=VR_CONTROL

R7750 0 5% 1/10W MF-LF 603
DIDT TRUE
P5VS3_REG_BOOT_R
MIN NECK WIDTH=0 2 MM
MIN LINE WIDTH=0 6MM
NET_SPACING_TYPE=VR_CONTROL

C7756 0.1UF 10% 25V X5R 402

NET SPACING TYPE=SWITCHNODE
DIDT TRUE
NET_PHYSICAL_TYPE=POWER

NOSTUFF
C7757 0.001UF 10% 50V CERM 402

5V SNUBBER
DIDT TRUE
MIN LINE WIDTH=0 4MM
MIN NECK WIDTH=0 2 MM
NET SPACING TYPE=SWITCHNODE
R7752 0.499 1% 1/10W MF 603 NOSTUFF

CRITICAL
Q7751 FDMS0355S POWER56 376S0917

EMC: C7763,C7764
PLACE AT L7750.2

C7763 0.001UF 10% 50V X7R 402
C7764 0.001UF 10% 50V X7R 402

PP5V_S3_REG 6

R7775 0.002 1% 1/4W MF LF 1206

CRITICAL
L7750 2.2UH+/-20%-0.0069OHM-16A PIC1005H-SM

PP5V_S3_REG_R
NET_PHYSICAL_TYPE=POWER

R7770 9.76K 1% 1/16W MF-LF 402
C7770 27.0NF 10% 10V X5R 402
R7771 9.76K 1% 1/16W MF-LF 402

OUTPUT BULK DECOUPLING:

C7760 10UF 20% 6.3V CERM 805-1
C7769 10UF 20% 6.3V CERM 805-1

CRITICAL
C7761 330UF 20% 6.3V POLY-TANT CASE-D3L-SM

CRITICAL
C7762 330UF 20% 6.3V POLY-TANT CASE-D3L-SM

SM XW7751 OMIT

OUTPUT BULK DECOUPLING:

PLACEMENT NOTE=PLACE NEXT TO C7716

C7715 10UF 10% 16V X5R CERM 0805
C7717 10UF 10% 16V X5R CERM 0805

128S0237
CRITICAL
C7721 330UF 20% 6.3V POLY-TANT CASE-D3L-SM

SM XW7716 OMIT

R7720 45.3K 1% 1/16W MF-LF 402 <Ra>
R7721 10.0K 0.5% 1/16W MF 402 <Rb>

R7724 976 1% 1/10W MF-LF 402
P3V3S5_REG_FB_R

C7720 1000PF 5% 25V NP0 C0G 402

C7723 0.1UF 20% 16V CERM 603
C7716 0.1UF 20% 16V CERM 603

EMC CAPS
PLACE CLOSE
TO L

Vout = 0.6V * (1 + Ra / Rb)

R7722 68K 5% 1/16W MF-LF 402
R7723 33K 5% 1/16W MF-LF 402

100 PM_EN_P3V3_S5_REG

U7700
ISL62383
QFN
CRITICAL

LDO5	18		
VCC1	5		
VCC2	4		
VIN	17	VIN_5V_S5_REG_RC	
FCCM	3	TP_P5VS3_REG_FCCM	
PGOOD1	7	PM_PGOOD_P3V3_S5_REG	
UGATE1	14	P3V3S5_REG_UGATE	
BOOT1	15	P3V3S5_REG_BOOT	
PHASE1	13	P3V3S5_REG_PHASE	
LGATE1	16	P3V3S5_REG_LGATE	
ISEN1	10	P3V3S5_REG_ISEN	
OCSET1	11	P3V3S5_REG_OCSET	
VOUT1	9	P3V3S5_REG_VOUT1	
FB1	8	P3V3S5_REG_FB	
FSET1	6		
EN1	12		
PGOOD2	1		
UGATE2	22	P5VS3_REG_UGATE	
BOOT2	21	P5VS3_REG_BOOT	
PHASE2	23	P5VS3_REG_PHASE	
LGATE2	20	P5VS3_REG_LGATE	
ISEN2	26	P5VS3_REG_ISEN	
OCSET2	25	P5VS3_REG_OCSET	
VOUT2	27	P5VS3_REG_VOUT2	
FB2	28	P5VS3_REG_FB	
FSET2	2	P5VS3_REG_FSET2	
EN2	24		
THRM PAD	29	PGND	

P3V3S5_REG_FSET1

C7701 0.01UF 10% 16V CERM 402
R7701 16.5K 1% 1/16W MF-LF 402

C7747 0.01UF 10% 16V CERM 402
R7747 16.5K 1% 1/16W MF-LF 402

NOSTUFF
C7777 0.001UF 10% 50V CERM 402

R7759 976 1% 1/16W MF-LF 402
P5V55_REG_FB_R

C7759 1000PF 5% 25V NP0-C0G 402

R7755 75K 1% 1/16W MF-LF 402 RA
R7756 10K 1% 1/16W MF-LF 402 RB

PM_EN_P5V_S3_REG 100 63

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SYNC_MASTER=K62_AARON	SYNC_DATE=12/08/2009
PAGE TITLE	5V S3 / 3V3 S5 VREGS
Apple Inc.	DRAWING NUMBER 051-8442 SIZE D
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1.5 V DDR SUPPLY

PPDDR_S3_REG
VOUT = 1.5V
PEAK = 11A
AVG = 6.7A

=PP12V_S5_DDR_VREG
=PP5V_S3_DDR_VREG
NET_PHYSICAL_TYPE=POWER
=PP3V3_S3_VRD
R7801 4.7 5% 1/16W MF LF 402
PP5V_S3_DDR_REG_V5FILT
MIN LINE WIDTH=0 6 mm
MIN NECK WIDTH=0 2 mm
VOLTAGE=5V
R7820 10K 5% 1/16W MF LF 402
C7800 4.7UF 20% 6.3V CERM 603
C7801 1UF 10% 16V X5R 402
V5IN
V5FILT
VLDOIN
C7815 10UF 20% 6.3V X5R 603
R7810 3.57K 1% 1/16W MF LF 402
NET_PHYSICAL_TYPE=POWER
NET SPACING TYPE=POWER
DIDT TRUE
CRITICAL C7830 270UF 20% 16V ELEC 8X9-TH1
CRITICAL C7831 270UF 20% 16V ELEC 8X9-TH1
C7832 10UF 10% 16V X5R CERM 0805
EMC CAPS PLACE CLOSE TO FET
C7833 1UF 10% 16V X5R 603
C7834 1UF 10% 16V X5R 603
R7841 4.7 5% 1/16W MF LF 603
DDR_REG_UGATE_R
CRITICAL Q7830 CSD58864Q5D SON5X6
VIN
TG
TGR
VSW
BG
PGND
DDR_REG_PHASE_R
CRITICAL L7830 1.5UH-15%-22A-3.3MOHM SDP1182M-TH
NOSTUFF C7841 1000PF 5% 25V NP0-C0G 402
1V5 SNUBBER
NOSTUFF R7831 0.499 1% 1/10W MF 603
OMIT XW7830
PLACEMENT NOTE=PLACE NEXT TO L7830
EMC CAPS PLACE CLOSE TO L7830
C7838 0.001UF 10% 50V X7R 402
C7839 0.001UF 10% 50V X7R 402
PP1V5_S3_REG
NET_PHYSICAL_TYPE=POWER
OUTPUT BULK DECOUPLING:
CRITICAL C7835 330UF 20% 2.5V POLY-TANT CASE-D2E-SM3
CRITICAL C7836 330UF 20% 2.5V POLY-TANT CASE-D2E-SM3
C7837 10UF 20% 6.3V X5R 603
PM_EN_DDRVTT_S0_REG
PM_EN_DDR1V5_S3_REG
PM_PGOOD_DDR1V5_S3_REG
TP_PPVTT_S3_DDR_BUF
(NOT USED)
10mA max load
Vout = VDDQSNS/2
Vout = VTTREF
OMIT XW7803
PPVTT_S0_DDR_LDO
DDR_REG_VTTSNS
NO_TEST=TRUE
FEEDBACK THROUGH, SHORT SHOULD NOT NEED TP
CRITICAL C7804 22UF 20% 6.3V CERM X5R 805-3
CRITICAL C7803 22UF 20% 6.3V CERM X5R 805 3
C7805 0.033UF 10% 16V X5R 402
XW7800 OMIT
AGND_DDR_REG
MIN LINE WIDTH=0 6 mm
MIN NECK WIDTH=0 2 mm
VOLTAGE=0V

U7800
TPS51116
QFN
SYM (2 OF 2)

VTT Enable	S3
VDDQ/VTTREF Enable	S5
VDDQ PGOOD	PGOOD
VTTREF	5
VTT	24
VTTSNS	2
NC0	7
NC1	12
VTTGND	1
THRM_PAD GND	25
PGND	3
CS GND	18
	17
COMP	6
S3	10
S5	11
PGOOD	13
VDDQSNS	8
MODE	4
VBST	22
DRVH	23
LL	20
DRVL	19
CS	16
VDDQSET	9

DDR_REG_VDDQSNS
DDR_REG_BOOT
DDR_REG_UGATE
DDR_REG_PHASE
DDR_REG_LGATE
DDR_REG_CS
DDR_REG_FB
DDR_REG_CSGND
DDR_REG_PGND

R7840 0 5% 1/10W MF-LF 603
C7840 0.1UF 20% 25V CERM 603
(DDRREG DRVH)
(DDRREG LL)
(DDRREG DRVL)
NET SPACING TYPE=VR CONTROL
NET SPACING TYPE VR CONTROL
NET SPACING TYPE SWITCHNODE
MIN LINE WIDTH=0 4MM
MIN NECK WIDTH=0 4MM
SWITCHNODE
OMIT XW7831
PLACEMENT NOTE=PLACE NEXT TO Q7831
(DDRREG CSGND)
(DDRREG VDDQSNS)
(DDRREG FB)
NOSTUFF C7820 100PF 5% 50V CERM 402
R7832 15.0K 1% 1/16W MF LF 402 <Ra>
R7833 15.0K 1% 1/16W MF LF 402 <Rb>

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON
S3	LO	HI	ON	ON	OFF
S5	LO	LO	OFF	OFF	OFF

Vout = 0.75V * (1 + Ra / Rb)

1.8 V SUPPLY

1A Average current
Vo=0.8*(1+ Ra/Rb)
Vo=0.8*(1+ 59/47)=1.804V

=PP5V_S0_P1V8_REG
C7854 22UF 20% 6.3V X5R-CERM-1 603
C7855 22UF 20% 6.3V X5R-CERM-1 603
R7853 100K 5% 1/16W MF-LF 402
R7854 100K 5% 1/16W MF-LF 402
U7850
ISL8013A
QFN
CRITICAL
VIN
VDD
EN
PG
SYNCH
VFB
NC
SGND
PGND
THRM_PAD
LX0
LX1
LX2
PM_EN_P1V8_S0_REG
PM_PGOOD_P1V8_S0_REG
P1V8_REG_SYNC
CONTINUOUS MODE
P1V8_REG_PHASE
P1V8_REG_VFB
NOSTUFF R7860 100K 5% 1/16W MF-LF 402
CRITICAL L7850 1.5UH-4A MMD04BZ-SM
NET_PHYSICAL_TYPE=POWER
SWITCHNODE
C7850 47PF 5% 50V CERM 402
<Ra> R7850 59.0K 1% 1/16W MF-LF 402
<Rb> R7851 47.0K 1% 1/16W MF-LF 402
C7852 22UF 20% 6.3V X5R-CERM-1 603
C7853 22UF 20% 6.3V X5R-CERM-1 603
PP1V8_S0_REG

SYNC_MASTER=K62_AARON	SYNC_DATE=11/30/2009
PAGE TITLE	1.5V / 1.8V VREGS
Apple Inc.	DRAWING NUMBER 051-8442 SIZE D
	REVISION 10.1.0
	BRANCH
	PAGE 78 OF 110
	SHEET 72 OF 101

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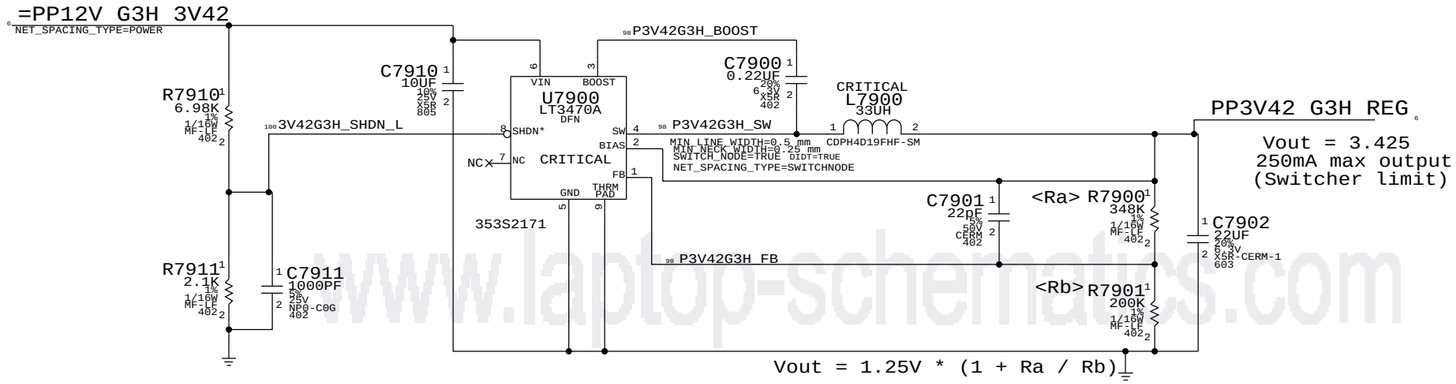
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



www.laptop-schematics.com

SYNC MASTER=K62 AARON SYNC DATE=N/A

PAGE TITLE: 3.42 G3HOT SUPPLY

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

REVISION: 10.1.0

BRANCH:

PAGE: 79 OF 110

SHEET: 73 OF 101

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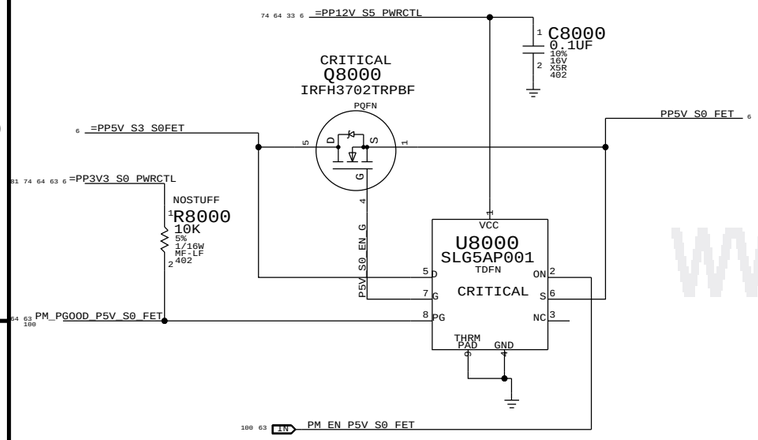
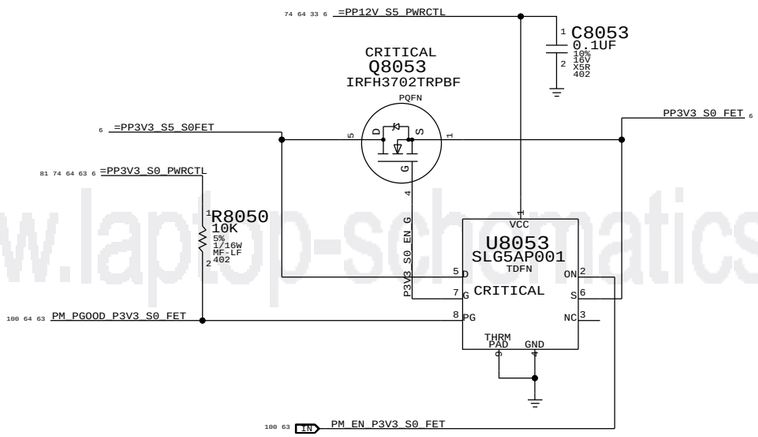
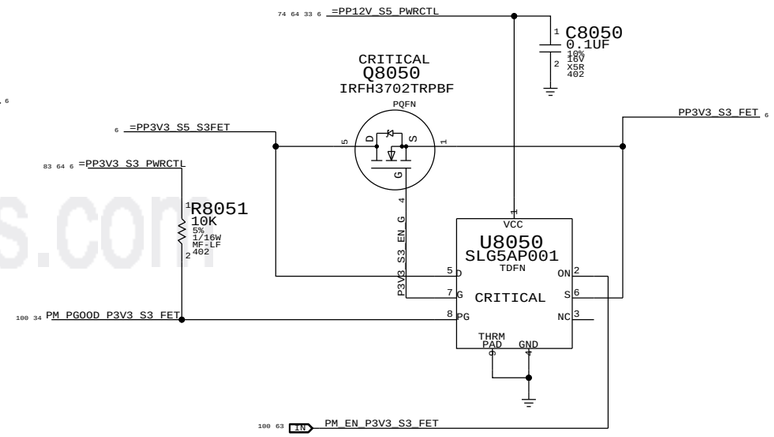
5V S0 FET (6.6A PK/3.1A AVG)



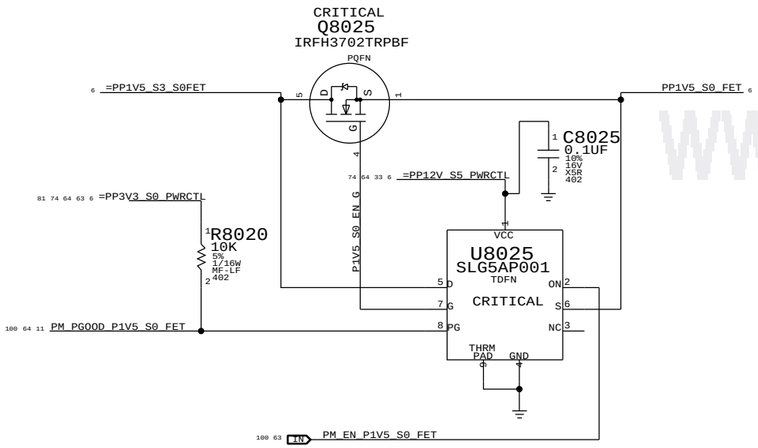
3.3V S0 FET (2.9APK / 2.0A AVG)



3.3V S3 FET (3.4A PK / 1.6A AVG)



1.5V S0 FET (4.8A PK / 4.8A AVG)



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SYNC MASTER=K62 AARON SYNC DATE=04/07/2010

PAGE TITLE: S3+S0 FETS

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

REVISION: 10.1.0

BRANCH:

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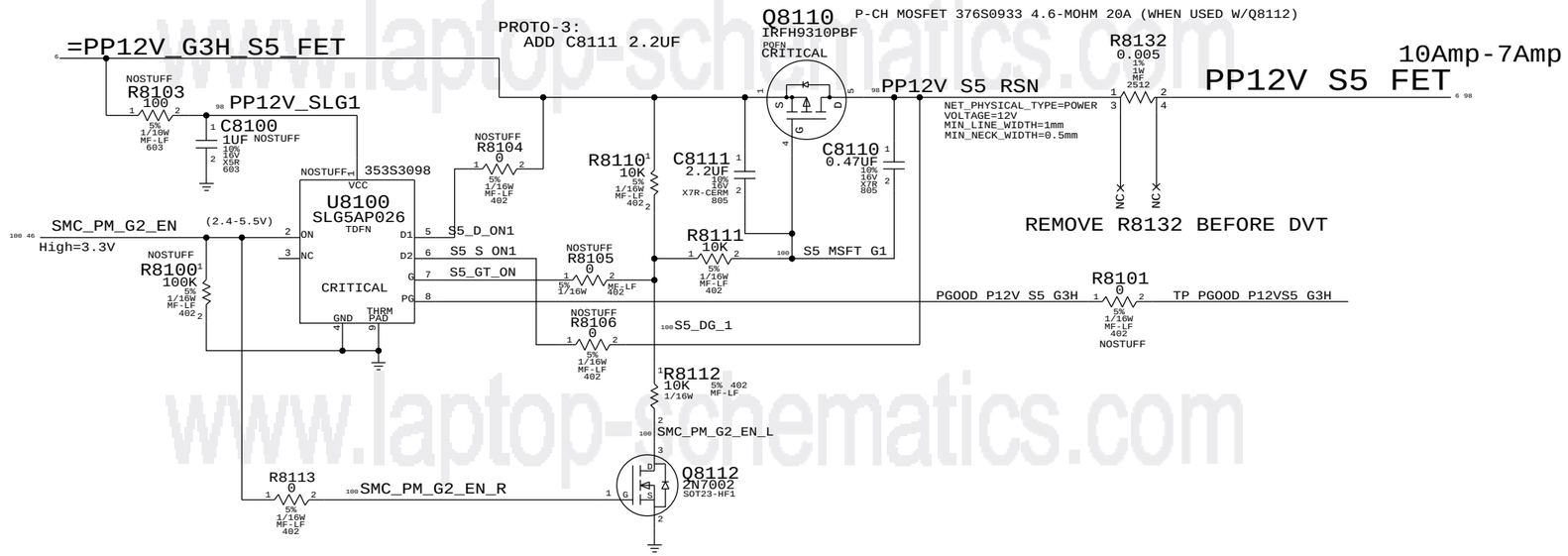
THE NMOS PMOS SHARING FOOTPRINT WILL NOT WORK DUE TO THE REVERSE POLARITY OF BODY DIODE.



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SYNC MASTER=K62 JERRY SYNC DATE=01/09/2011

PAGE TITLE
12V S0 & 12V S5 switch

Apple Inc.

DRAWING NUMBER 051-8442 SIZE D
REVISION 10.1.0
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SHEET 75 OF 101

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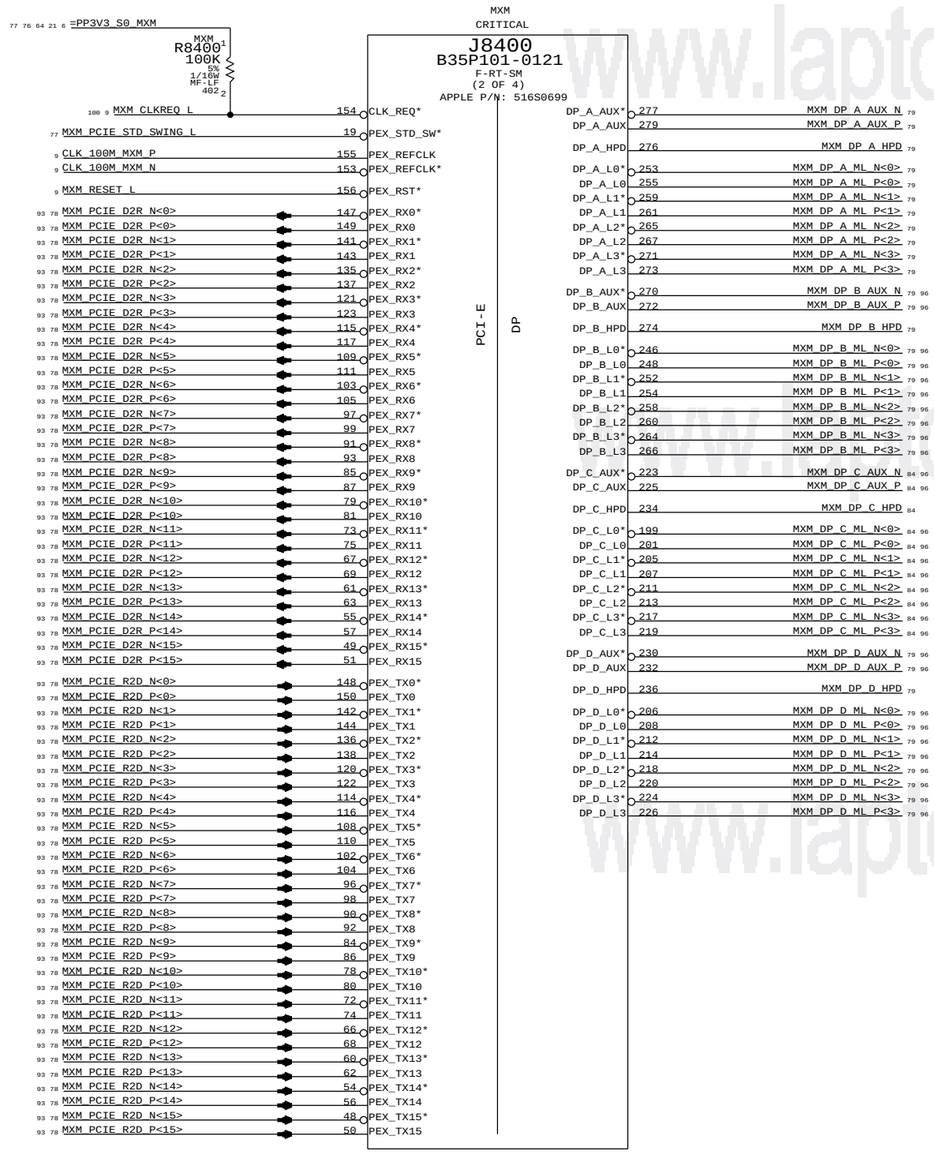
Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP5V_S0_MXM
- =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- MXM



MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.0 A	3.3 W
5V	2.5 A	12.5 W
PWR (7-20V)	UP TO 10 A	PLATFORM DEPENDENT

MXM DP PORT ROUTING

	K62	K60
DP A	EXT DP1	EXT DP1
DP B	T29 DP2	T29 DP2
DP C	INT DP	INT DP
DP D	T29 DP1	T29 DP1
DP E	EXT DP2	

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SYNC MASTER=K62_AARON SYNC DATE=N/A

PAGE TITLE
MXM PCIe, DP & Power

Apple Inc.

DRAWING NUMBER 051-8442 SIZE D
REVISION 10.1.0
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SHEET 76 OF 101

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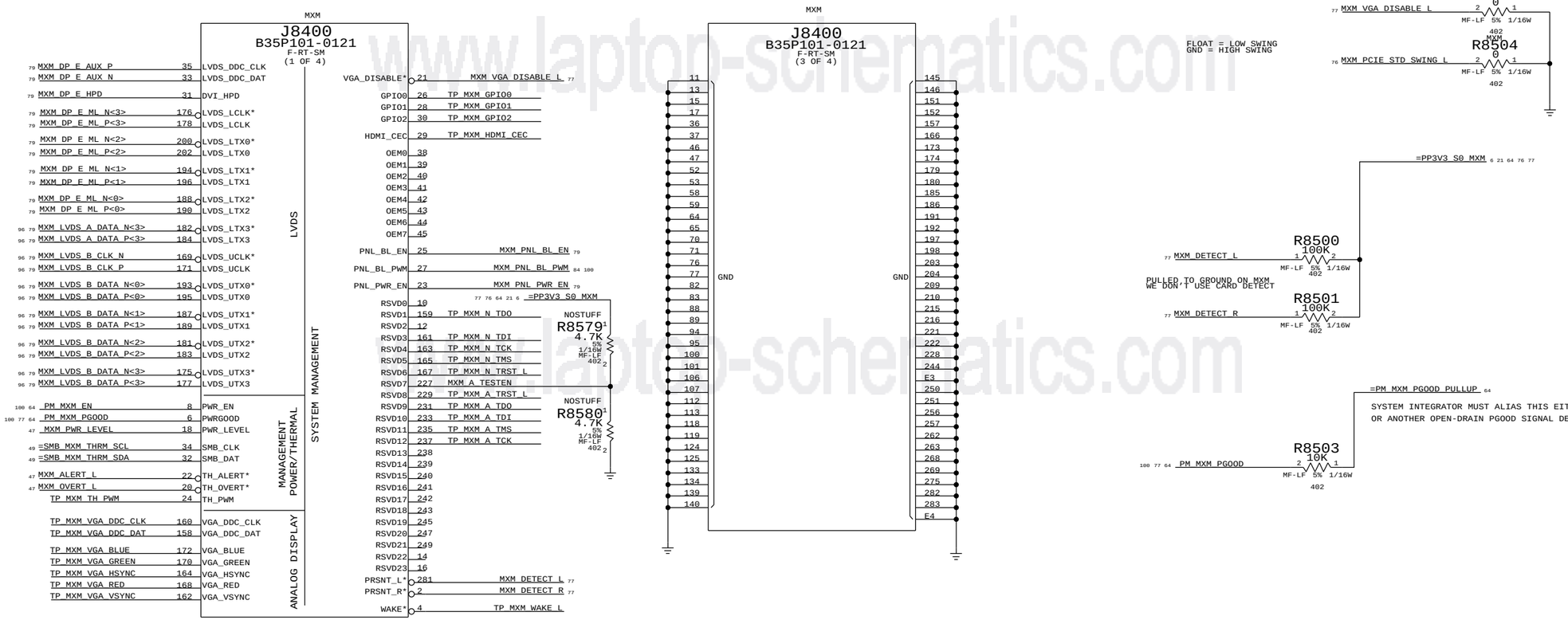
Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM

Signal aliases required by this page:
- =SMB_MXM_THRM_DATA
- =PM_MXM_PGOOD_PULLUP
- =SMB_MXM_THRM_CLK

BOM options provided by this page:

PULLUPS & PULLDOWNS AT MXM CONNECTOR



FLOAT = NORMAL VGA MODE
GND = SECONDARY DISPLAY CARD

NOSTUFF
R8510 0 MF-LF 5% 1/16W 402
MXM_VGA_DISABLE_L

FLOAT = LOW SWING
GND = HIGH SWING

R8504 0 MF-LF 5% 1/16W 402
MXM_PCIE_STD_SWING_L

=PP3V3_S0_MXM

R8500 100K MF-LF 5% 1/16W 402
MXM_DETECT_L

PULLED TO GROUND ON MXM
WE DON'T USE CARD DETECT

R8501 100K MF-LF 5% 1/16W 402
MXM_DETECT_R

=PM_MXM_PGOOD_PULLUP

SYSTEM INTEGRATOR MUST ALIAS THIS EITHER TO A VOLTAGE RAIL,
OR ANOTHER OPEN-DRAIN PGOOD SIGNAL DEPENDING ON DESIRED BEHAVIOR

R8503 10K MF-LF 5% 1/16W 402
PM_MXM_PGOOD

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SYNC MASTER=K62 AARON SYNC DATE=N/A

PAGE TITLE: MXM I/O

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D
REVISION: 10.1.0
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MXM TX CAPS

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MXM RX CAPS

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SYNC_MASTER=K62 SYNC_DATE=N/A

PAGE TITLE

MXM PCIE CAPS

Apple Inc.

DRAWING NUMBER 051-8442 SIZE D

REVISION 10.1.0

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PAGE 86 OF 110

SHEET 78 OF 101

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Page Notes

Power aliases required by this page:

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

MXM ALIAS

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76 MXM_DP_A_ML_P<0..3>      ==  DP_EXTA_ML_C_P<0..3>      85 96
                                MAKE_BASE=TRUE  NO_TEST=TRUE
76 MXM_DP_A_ML_N<0..3>      ==  DP_EXTA_ML_C_N<0..3>      85 96
                                MAKE_BASE=TRUE  NO_TEST=TRUE
76 MXM_DP_A_AUX_P           ==  DP_EXTA_AUXCH_C_P         79 85 96
                                MAKE_BASE=TRUE  NO_TEST=TRUE
76 MXM_DP_A_AUX_N           ==  DP_EXTA_AUXCH_C_N         79 85 96
                                MAKE_BASE=TRUE  NO_TEST=TRUE
76 MXM_DP_A_HPD             ==  DP_EXTA_HPD               85
                                MAKE_BASE=TRUE  NO_TEST=TRUE

77 MXM_DP_E_ML_P<0..3>      ==  DP_EXTB_ML_C_P<0..3>      87 96
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77 MXM_DP_E_ML_N<0..3>      ==  DP_EXTB_ML_C_N<0..3>      87 96
                                MAKE_BASE=TRUE  NO_TEST=TRUE
77 MXM_DP_E_AUX_P           ==  DP_EXTB_AUXCH_C_P         79 87 96
                                MAKE_BASE=TRUE  NO_TEST=TRUE
77 MXM_DP_E_AUX_N           ==  DP_EXTB_AUXCH_C_N         79 87 96
                                MAKE_BASE=TRUE  NO_TEST=TRUE
77 MXM_DP_E_HPD             ==  DP_EXTB_HPD               87
                                MAKE_BASE=TRUE  NO_TEST=TRUE
```

DDC/AUX ALIAS

```
96 85 79 DP_EXTA_AUXCH_C_P  ==  DP_EXTA_DDC_CLK           85
         MAKE_BASE=TRUE     ==
96 85 79 DP_EXTA_AUXCH_C_N  ==  DP_EXTA_DDC_DATA          85
         MAKE_BASE=TRUE     ==

96 87 79 DP_EXTB_AUXCH_C_P  ==  DP_EXTB_DDC_CLK           87
         MAKE_BASE=TRUE     ==
96 87 79 DP_EXTB_AUXCH_C_N  ==  DP_EXTB_DDC_DATA          87
         MAKE_BASE=TRUE     ==
```

NO_TEST T29 & DP DC BIAS

```
F03  T29_A_BIAS_R2D_P0      ==  T29_B_BIAS_R2D_P2         87 88
     NO_TEST=TRUE           ==  NO_TEST=TRUE
F02  T29_A_BIAS_R2D_N0      ==  T29_B_BIAS_R2D_N2         87 88
     NO_TEST=TRUE           ==  NO_TEST=TRUE
F04  T29_A_BIAS_R2D_P1      ==  T29_B_BIAS_R2D_P3         87 88
     NO_TEST=TRUE           ==  NO_TEST=TRUE
F04  T29_A_BIAS_R2D_N1      ==  T29_B_BIAS_R2D_N3         87 88
     NO_TEST=TRUE           ==  NO_TEST=TRUE
F04  T29_A_BIAS             ==  T29_B_BIAS                83 87 88 99
     NO_TEST=TRUE           ==  NO_TEST=TRUE
F03  T29_A_BIAS_P0          ==  T29_B_BIAS_P2             88
     NO_TEST=TRUE           ==  NO_TEST=TRUE
F03  T29_A_BIAS_N0          ==  T29_B_BIAS_N2             88
     NO_TEST=TRUE           ==  NO_TEST=TRUE
F03  DP_A_BIAS_P_0          ==  DP_B_BIAS_P_0             87 88
     NO_TEST=TRUE           ==  NO_TEST=TRUE
F03  DP_A_BIAS_N_0          ==  DP_B_BIAS_N_0             87 88
     NO_TEST=TRUE           ==  NO_TEST=TRUE
F02  DP_A_BIAS_P_2          ==  DP_B_BIAS_P_2             87 88
     NO_TEST=TRUE           ==  NO_TEST=TRUE
F01  DP_A_BIAS_N_2          ==  DP_B_BIAS_N_2             87 88
     NO_TEST=TRUE           ==  NO_TEST=TRUE
F04  DP_A_BIAS              ==  DP_B_BIAS                 85 99
     NO_TEST=TRUE           ==  NO_TEST=TRUE
```

T29 CONN POWER AND CONTROL ALIAS

```
0  =PP3V3_SW_DPAPWR         ==  PP3V3_SW_DPAPWR           85 98

0  =PP3V3_SW_DPBPWR         ==  PP3V3_SW_DPBPWR           87 98

100 36 33 19 PCIE_WAKE_L    ==  =T29_WAKE_L               85 87

96 76 MXM_DP_B_ML_P<0..3>   ==  DP_T29SNK1_ML_C_P<0..3>   89 99
                                MAKE_BASE=TRUE  NO_TEST=TRUE
96 76 MXM_DP_B_ML_N<0..3>   ==  DP_T29SNK1_ML_C_N<0..3>   89 99
                                MAKE_BASE=TRUE  NO_TEST=TRUE
96 76 MXM_DP_B_AUX_P        ==  DP_T29SNK1_AUXCH_C_P      89 99
                                MAKE_BASE=TRUE  NO_TEST=TRUE
96 76 MXM_DP_B_AUX_N        ==  DP_T29SNK1_AUXCH_C_N      89 99
                                MAKE_BASE=TRUE  NO_TEST=TRUE
76 MXM_DP_B_HPD             ==  DP_T29SNK1_HPD            89
                                MAKE_BASE=TRUE  NO_TEST=TRUE

96 76 MXM_DP_D_ML_P<0..3>   ==  DP_T29SNK0_ML_C_P<0..3>   89 99
                                MAKE_BASE=TRUE  NO_TEST=TRUE
96 76 MXM_DP_D_ML_N<0..3>   ==  DP_T29SNK0_ML_C_N<0..3>   89 99
                                MAKE_BASE=TRUE  NO_TEST=TRUE
96 76 MXM_DP_D_AUX_P        ==  DP_T29SNK0_AUXCH_C_P      89 99
                                MAKE_BASE=TRUE  NO_TEST=TRUE
96 76 MXM_DP_D_AUX_N        ==  DP_T29SNK0_AUXCH_C_N      89 99
                                MAKE_BASE=TRUE  NO_TEST=TRUE
76 MXM_DP_D_HPD             ==  DP_T29SNK0_HPD            89
                                MAKE_BASE=TRUE  NO_TEST=TRUE
```

UNUSED MXM CONTROL SIGNALS

```
77 MXM_PNL_BL_EN            ==  NC_MXM_PNL_BL_EN
                                MAKE_BASE=TRUE  NO_TEST=TRUE

77 MXM_PNL_PWR_EN           ==  NC_MXM_PNL_PWR_EN
                                MAKE_BASE=TRUE  NO_TEST=TRUE
```

Unused MXM Interfaces

```
96 77 MXM_LVDS_A_DATA_N<3>  ==  NC_MXM_LVDS_A_DATA_N<3>
                                MAKE_BASE=TRUE  NO_TEST=TRUE
96 77 MXM_LVDS_A_DATA_P<3>  ==  NC_MXM_LVDS_A_DATA_P<3>
                                MAKE_BASE=TRUE  NO_TEST=TRUE
96 77 MXM_LVDS_B_CLK_N      ==  NC_MXM_LVDS_B_CLK_N
                                MAKE_BASE=TRUE  NO_TEST=TRUE
96 77 MXM_LVDS_B_CLK_P      ==  NC_MXM_LVDS_B_CLK_P
                                MAKE_BASE=TRUE  NO_TEST=TRUE
96 77 MXM_LVDS_B_DATA_N<0>  ==  NC_MXM_LVDS_B_DATA_N<0>
                                MAKE_BASE=TRUE  NO_TEST=TRUE
96 77 MXM_LVDS_B_DATA_P<0>  ==  NC_MXM_LVDS_B_DATA_P<0>
                                MAKE_BASE=TRUE  NO_TEST=TRUE
96 77 MXM_LVDS_B_DATA_N<1>  ==  NC_MXM_LVDS_B_DATA_N<1>
                                MAKE_BASE=TRUE  NO_TEST=TRUE
96 77 MXM_LVDS_B_DATA_P<1>  ==  NC_MXM_LVDS_B_DATA_P<1>
                                MAKE_BASE=TRUE  NO_TEST=TRUE
96 77 MXM_LVDS_B_DATA_N<2>  ==  NC_MXM_LVDS_B_DATA_N<2>
                                MAKE_BASE=TRUE  NO_TEST=TRUE
96 77 MXM_LVDS_B_DATA_P<2>  ==  NC_MXM_LVDS_B_DATA_P<2>
                                MAKE_BASE=TRUE  NO_TEST=TRUE
96 77 MXM_LVDS_B_DATA_N<3>  ==  NC_MXM_LVDS_B_DATA_N<3>
                                MAKE_BASE=TRUE  NO_TEST=TRUE
96 77 MXM_LVDS_B_DATA_P<3>  ==  NC_MXM_LVDS_B_DATA_P<3>
                                MAKE_BASE=TRUE  NO_TEST=TRUE
```

SYNC MASTER=K62 AARON SYNC DATE=N/A

PAGE TITLE
DP ALIAS

Apple Inc.

DRAWING NUMBER 051-8442 SIZE D
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System RTC Power Source & 32kHz / 25MHz Clock Generator

GreenCLK Implementation Notes:

VBAT: Alias as appropriate (see note below & Desktop Example)
+V3.3A: Alias as appropriate (see note below)
VDD_25M: 3.3V matching 'highest' VDDIO power state (ENET)

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: T29 power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.

For Cougar Point Desktop: VDDIO = VCCVRM (1.8V), Vclk = 1.1V Max, Divider: 604 / 1000
For Cougar Point Mobile: VDDIO = VCCVRM (1.5V), Vclk = 1.1V Max, Divider: 332 / 1000
For Caesar-IV (BCM57765): VDDIO = XTALVDDH (3.3V), Vclk = 3.3V Max. No Divider Necessary

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6 =PP3V3_S3_SYSCLK

Coin-Cell & G3Hot: 3.42V G3Hot
Coin-Cell & No G3Hot: 3.3V S5
No Coin-Cell: 3.3V S5

80 37 36 =PP3V3_S3_ENET_PHY_FET

80 37 36 =PP3V3_S3_ENET_PHY_FET — R8812 0 5% 1/16W MF LF 402 — 98 PPVDDIO_25M_B
MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V

24 18 6 =PP1V05_S0_PCH — R8806 0 5% 1/16W MF LF 402 — NOSTUFF

80 24 6 =PP1V8R1V5_S0_PCH_VCCVRM — R8807 0 5% 1/16W MF LF 402 — 98 PPVDDIO_25M_A
MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.05V

No bypass necessary

90 89 81 6 =PP3V3_T29_RTR — R8810 0 5% 1/16W MF LF 402 — T29 — 98 PPVDDIO_25M_C

80 24 6 =PP1V8R1V5_S0_PCH_VCCVRM — R8809 0 5% 1/16W MF LF 402 — NOSTUFF
MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V

T29 C8824 0.1UF 20% 10V CERM 402
C8822 0.1UF 20% 10V CERM 402
C8820 0.1UF 20% 10V CERM 402
C8802 1UF 10% 6.3V CERM 402

C8805 12PF 5% 50V CERM 402
C8806 12PF 5% 50V CERM 402
NC NC CRITICAL Y8805 25.000MHZ-12PF-20PPM SM 3.2X2 5MM
NOTE: 30 PPM crystal required

99 SYSCLK_CLK25M_X2 — R8815 0 5% 1/16W MF LF 402 — 99 SYSCLK_CLK25M_X2_R
NOSTUFF R8816 1M 5% 1/16W MF LF 402
99 SYSCLK_CLK25M_X1

U8800 SLG3NB148V TQFN CRITICAL

11	VDDIO_25M_A	32KHZ_A	12 — TP_SYSCLK_CLK32K_RTC
6	VDDIO_25M_B		
14	VDDIO_25M_C	25MHZ_A	9 — 99 SYSCLK_CLK25M_SB
		25MHZ_B	8 — 99 SYSCLK_CLK25M_ENET
		25MHZ_C	15 — 99 SYSCLK_CLK25M_T29_CLK
3	X2		
4	X1		
		VDD_RTC_OUT	1 — TP_PPVRTC_G3_OUT
5	VDD_25M		
2	+V3.3A		
13	+3.42V		
7	GND		
10 16 17	THRM PAD		

VBAT and +V3.3A are internally ORed to create VDD_RTC_OUT.

+V3.3A should be first available ~3.3V power to reduce VBAT draw.

For SB RTC Power

C8810 1UF 10% 6.3V CERM 402

98 PPVBAT_G3_SYSCLK_R
MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
R8808 10K 5% 1/16W MF-LF 402

R8825 40.2 1% 1/16W MF LF 402 — PCH_CLK25M_XTALIN (1.1V) OUT 18 27 94
R8826 140 1% 1/16W MF LF 402

R8843 33 5% 1/16W MF LF 402
T29 R8845 47 5% 1/16W MF LF 402 — SYSCLK_CLK25M_T29 (1.8V) OUT 89 99
ENET_CLK25M_XTALI_OSC (3.3V) OUT 36 99

SYNC MASTER=K62_AARON SYNC_DATE=N/A
PAGE TITLE: GREEN CLOCK

Apple Inc.

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Page Notes

Power aliases required by this page:
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

Signal aliases required by this page:
- =T29_CLKREQ_L
- T29_RESET_L

BOM options provided by this page:
(NONE)

Supervisor & CLKREQ# Isolation

=PP3V3_S0_T29PWRCTL

R8906 10K 5% 1/16W MF LF 402

C8900 0.1UF 10% 25V X5R 402

U8900 SLG4AP016V TDFN — T29 CRITICAL

VDD

=PP3V3_T29_RTR

R8907 100K 5% 1/16W MF LF 402

=PP1V05_T29

SENSE 0.7V

Platform (PCIe) Reset

T29_RESET_L

R8903 10K 5% 1/16W MF LF 402

Open-Drain GPIO

T29_SW_RESET_L

DLY

MR*

RESET*

T29_RESET_RTR_L

DLY = 60 ms +/- 20%

EN

OUT (OD)

IN

=T29_CLKREQ_L

T29_CLKREQ_ISOL_L

MAKE BASE=TRUE

GND

THRM PAD

T29 CLKREQ# ISOLATION

=PP3V3_T29_RTR

T29 R8904 10K 5% 1/16W MF LF 402

T29 Q8950 SSM3K15FV SOD-VESM-HF

T29_CLKREQ_L

T29_CLKREQ_FET_L

Pull-up provided by SB page.

3.3V T29 Switch

=PP3V3_S0_P3V3T29FET

U8910 TPS22924 CSP — T29 CRITICAL

VIN VOUT ON GND

PP3V3_T29_FET

Max Current = 1.7A (85C)

C8910 1UF 10% 6.3V CERM 402

U8910

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

1.05V T29 Switch

=PP12V_S0_PWRCTL

C8930 0.1UF 10% 16V X5R 402

CRITICAL

Q8930 BSZ035N03MSG P-TSDSON-8 — T29

=PP1V05_S0_P1V05T29FET

PP1V05_T29_FET

=PP3V3_S0_PWRCTL

R8930 10K 5% 1/16W MF-LF 402

P1V05_S0_T29_EN

U8930 SLG5AP001 TDFN — T29 CRITICAL

VCC D ON G S PG NC THRM PAD GND

PM_PGOOD_P1V05_S0_T29_FET

T29_PWR_EN

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SYNC_MASTER=K62_AARON	SYNC_DATE=(MASTER)
PAGE TITLE	T29 POWER
Apple Inc.	DRAWING NUMBER 051-8442 SIZE D
	REVISION 10.1.0
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Page Notes

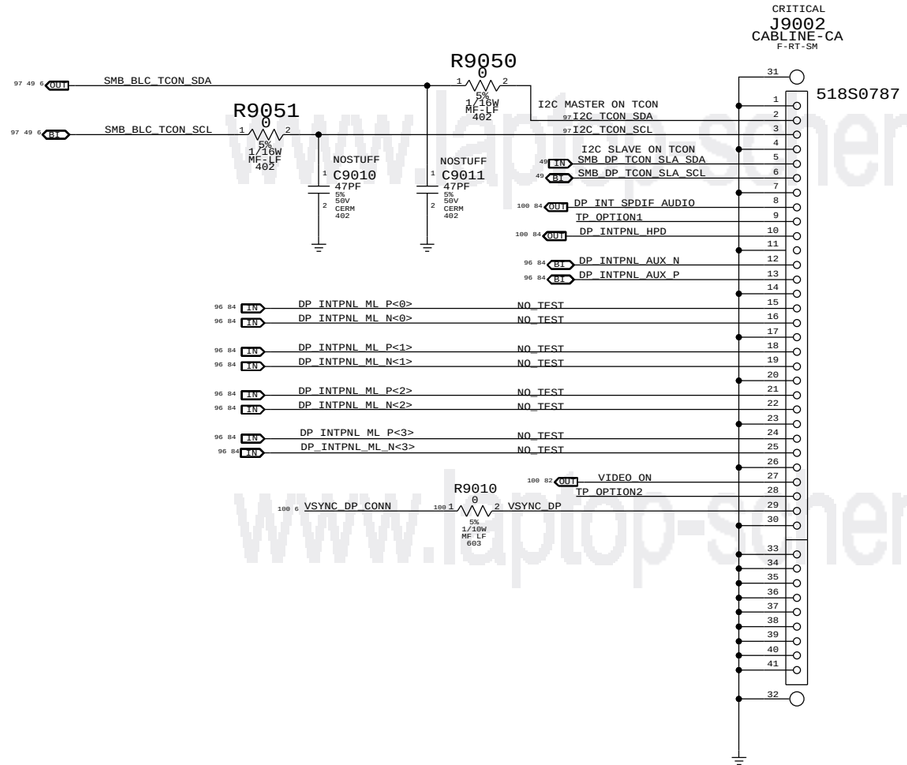
Power aliases required by this page:

- =PP12V_S0_LCD
- =PP3V3_S0_VIDEO

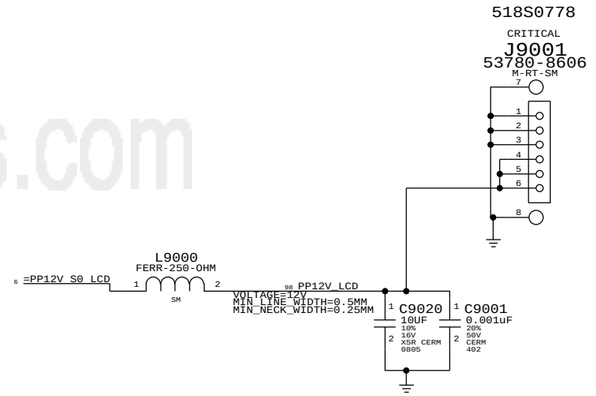
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
IG, MXM, MLB_PNL_PWR, LCD_PNL_PWR

INTERNAL DP INTERFACE

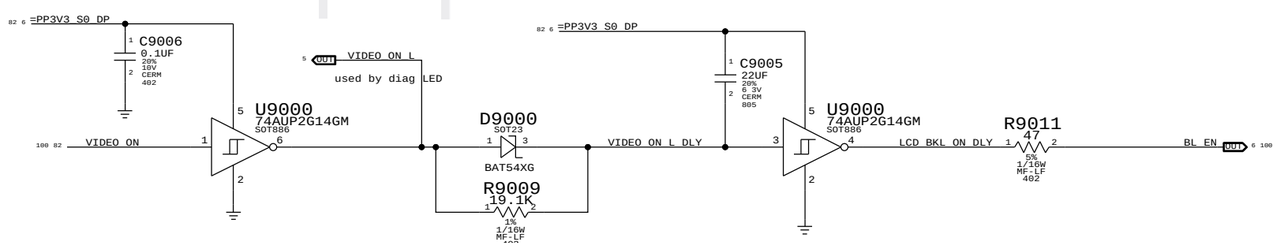


INTERNAL DP POWER



BACKLIGHT CONTROL SUPPORT

guarantee backlight is
only on when Panel has valid video



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SYNC_MASTER=K62_AARON
SYNC_DATE=N/A

PAGE TITLE
Display: Int DP Connector

Apple Inc.

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3V3(DP)/2V9(T29) PORTA SUPPLY

=PP5V_S3_P3V3R2V9_REG_A
C9120 10UF 10% 16V X5R-CERM 0805
U9101 ISL80101A DFN
CRITICAL
T29_DP_PORTA_PWR_EN_REG
3V3R2V9_SS_A
C9121 0.022UF 10% 16V CERM-X5R 402
R9130 25.5K 1/16W 1% MF-LF 402
80101A1 ISET
C9122 10UF 10% 16V X5R-CERM 0805
R9121 20K 1/10W 5% MF-LF 402
C9123 330PF 10% 50V 402 CERM
PP3V3R2V9_DPAPWR_D
NET_PHYSICAL_TYPE=POWER
MIN_LINE_WIDTH=0 5MM
MIN_NECK_WIDTH=0 2MM
VOLTAGE=3 3V
D9101 POWERDI-123 DFLS260
3V3R2V9_DPAPWR_ADJ
R9123 2.05K 1/16W 1% MF-LF 402
<RB2>
=PP3V3_S3_P3V3R2V9_REG_A
R9122 100K 1/16W 5% MF-LF 402
PM_PGOOD_P3V3_2V9_A
PP3V3R12V_SW_DPAPWR
NET_PHYSICAL_TYPE=POWER
MIN_LINE_WIDTH=0 38 MM
MIN_NECK_WIDTH=0 20 MM
VOLTAGE=12V
R9124 11.5K 1/16W 1% MF-LF 402
<RA>
C9124 10UF 10% 16V X5R-CERM 0805
NOSTUFF
C9125 10UF 10% 16V X5R-CERM 0805
R9150 2.2K 1/10W 5% MF-LF 603
R9125 15.0K 1/16W 1% MF-LF 402
<RB1>
VO=0.5*(1+ RA/RB)
VO=3.304V
DP_A_PWRDWN_INV
=PP3V3_S3_PWRCTL
R9126 10K 5% 1/16W MF-LF 402
DP_A_PWRDWN_FET_R
Q9120 2N7002DW-X-G SOT 363
=PP3V3_S5_P3V3R2V9_A
C9150 0.1UF 10% 16V X5R 402
T29_DP_PORTA_PWR_EN
PM_PGOOD_P5V_S3_REG
U9120 MC74VHC1G08 SOT23-5-HF
T29_DP_PORTA_PWR_EN_REG
T29_A_BIAS
LO: 3V3 FOR DP
HI: 2V9 FOR T29
2V9 MEASURED AT CDR

12V T29 PORTA SUPPLY

12 VOLTS
12 WATTS MAX PER PORT
=PP12V_S5_T29_A
T29 R9116 15K 5% 1/10W MF LF 402
T29 CRITICAL D9103 MMBZ5227BLT1H SOT23
NOSTUFF R9117 13K 5% 1/16W MF LF 402
T29 Q9115 SSM3K15FV SOD VESM HF
T29_A_HV_EN
DPAPWRSW_HVEN_L_R
T29 C9110 0.1UF 10% 50V X7R 603
T29 U9110 SN1010017 QFN
CRITICAL
EN* (IPU Weak!)
RTRY* (IPU Weak!)
CT
FLT*
ILIM
IFLT
GND
THRM PAD
DPAPWRSW_CT
T29 R9112 0 5% 1/16W MF LF 402
<CT>
DPAPWRSW_IFLT
TP_DPAPWRSW_FLT_L
T29 R9110 100K 1% 1/16W MF LF 402
<RFLT>
T29 R9111 174K 1% 1/16W MF LF 402
<RLIM>
T29 C9111 0.1UF 10% 50V X7R 603
T29 D9105 DSN2 NSR20F20NXT5G
PP3V3R12V_SW_DPAPWR_D
PP3V3R12V_SW_DPAPWR
MIN_LINE_WIDTH=0 38 MM
MIN_NECK_WIDTH=0 20 MM
VOLTAGE=12V

NEED TO UPDATE TABLE BELOW LATER

	Nominal	Min	Max
IFLT	885mA	876mA	894mA (*)
ILIM	935mA	925mA	944mA (*)
TFLT	18.3ms	13.4ms	26.7ms
TSD	470ms	235ms	724ms

(*) U9410 tolerance unknown

IFLT = 200K / RFLT = 2A
ILIM = 201K / RLIM = 1.155A.
TFLT = CCT * 38900
TSD = CCT * 100000

3V3(DP)/2V9(T29) PORTB SUPPLY

=PP5V_S3_P3V3R2V9_REG_B
C9130 10UF 10% 16V X5R-CERM 0805
U9131 ISL80101A DFN
CRITICAL
T29_DP_PORTB_PWR_EN_REG
3V3R2V9_SS_B
C9131 0.022UF 10% 16V CERM-X5R 402
R9129 25.5K 1/16W 1% MF-LF 402
80101A2 ISET
C9132 10UF 10% 16V X5R-CERM 0805
R9131 20K 1/10W 5% MF-LF 402
C9133 330PF 10% 50V 402 CERM
PP3V3R2V9_DPBPWR_D
NET_PHYSICAL_TYPE=POWER
MIN_LINE_WIDTH=0 5MM
VOLTAGE=3 3V
MIN_NECK_WIDTH=0 2MM
D9131 POWERD1-123 DFLS260
3V3R2V9_DPBPWR_ADJ
R9133 2.05K 1/16W 1% MF-LF 402
<RB2>
=PP3V3_S3_P3V3R2V9_REG_B
R9132 100K 1/16W 5% MF-LF 402
PM_PGOOD_P3V3_2V9_B
PP3V3R12V_SW_DPBPWR
NET_PHYSICAL_TYPE=POWER
MIN_LINE_WIDTH=0 38 MM
VOLTAGE=12V
MIN_NECK_WIDTH=0 20 MM
R9134 11.5K 1/16W 1% MF-LF 402
<RA>
C9134 10UF 10% 16V X5R-CERM 0805
NOSTUFF
C9135 10UF 10% 16V X5R-CERM 0805
R9151 2.2K 1/10W 5% MF-LF 603
R9135 15.0K 1/16W 1% MF-LF 402
<RB1>
DP_B_PWRDWN_INV
=PP3V3_S3_PWRCTL
R9136 10K 5% 1/16W MF-LF 402
DP_B_PWRDWN_FET_R
Q9130 2N7002DW-X-G SOT 363
=PP3V3_S5_P3V3R2V9_B
C9151 0.1UF 10% 16V X6R 402
T29_DP_PORTB_PWR_EN
PM_PGOOD_P5V_S3_REG
U9130 MC74VHC1G08 SOT23-5-HF
T29_DP_PORTB_PWR_EN_REG
T29_B_BIAS
LO: 3V3 FOR DP
HI: 2V9 FOR T29
2V9 MEASURED AT CDR

12V T29 PORTB SUPPLY

12 VOLTS
12 WATTS MAX PER PORT
=PP12V_S5_T29_B
T29 R9146 15K 5% 1/10W MF LF 402
(IPU Weak!)
T29 CRITICAL D9104 MMBZ5227BLT1H SOT23
NOSTUFF R9147 13K 5% 1/16W MF LF 402
T29 Q9145 SSM3K15FV SOD VESM HF
T29_B_HV_EN
DPBPWRSW_HVEN_L_R
T29 C9140 0.1UF 10% 50V X7R 603
T29 U9140 SN1010017 QFN
CRITICAL
EN* (IPU Weak!)
RTRY*
CT
FLT*
ILIM
IFLT
GND
THRM PAD
DPBPWRSW_CT
T29 R9142 0 5% 1/16W MF LF 402
<CT>
DPBPWRSW_IFLT
TP_DPBPWRSW_FLT_L
T29 R9140 100K 1% 1/16W MF LF 402
<RFLT>
T29 R9141 174K 1% 1/16W MF LF 402
<RLIM>
T29 C9141 0.1UF 10% 50V X7R 603
T29 D9106 DSN2 NSR20F20NXT5G
PP3V3R12V_SW_DPBPWR_D
PP3V3R12V_SW_DPBPWR
MIN_LINE_WIDTH=0 38 MM
MIN_NECK_WIDTH=0 20 MM
VOLTAGE=12V

	Nominal	Min	Max
IFLT	885mA	876mA	894mA (*)
ILIM	935mA	925mA	944mA (*)
TFLT	18.3ms	13.4ms	26.7ms
TSD	470ms	235ms	724ms

(*) U9410 tolerance unknown

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SYNC_MASTER=K62_AARON
SYNC_DATE=N/A
PAGE TITLE: 2V9/3V3/12V POWER SWITCH
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REVISION: 10.1.0
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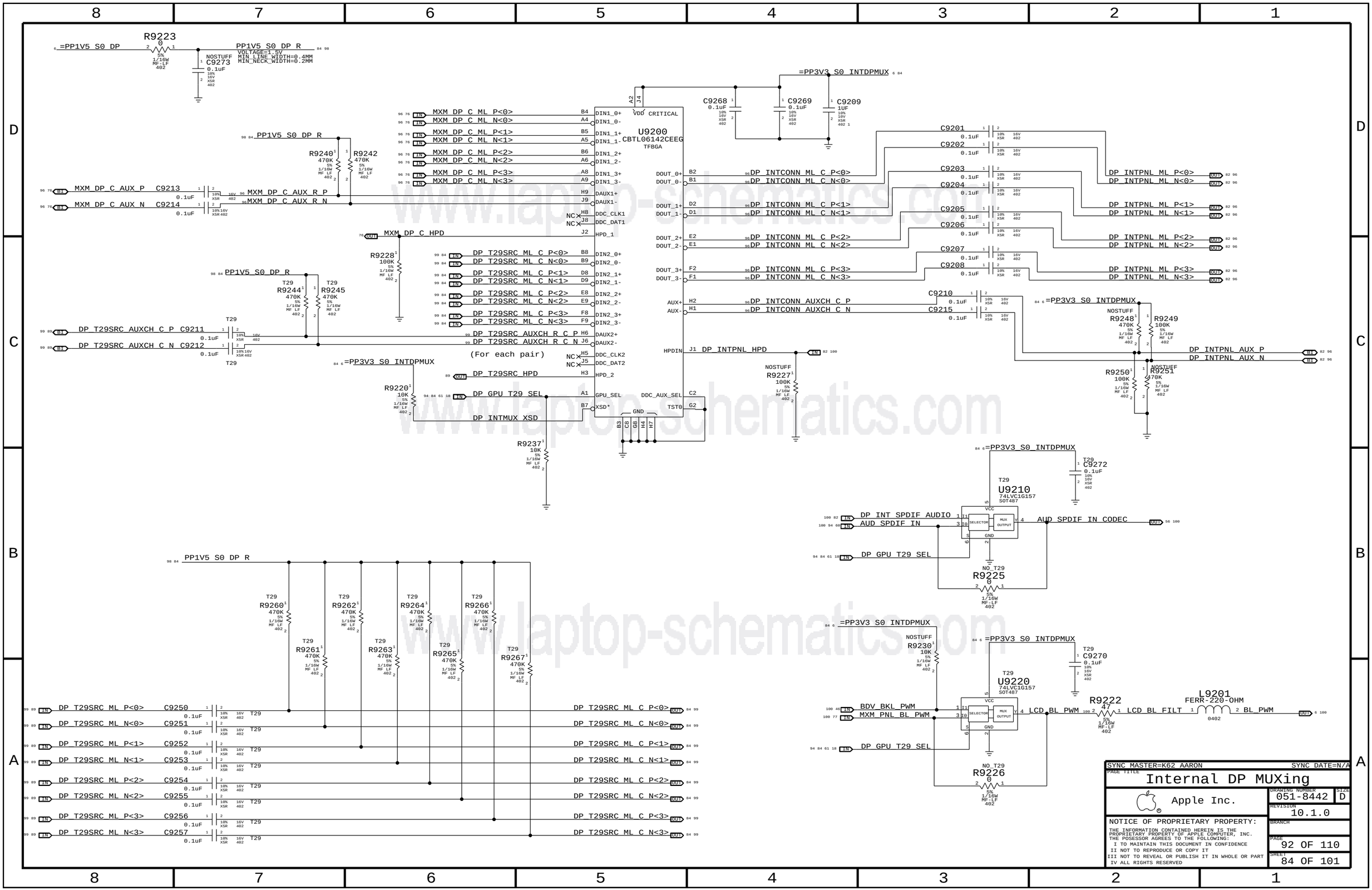

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DP A Super-Driver

DP_EXTA_ML_C_P<0> C9300 0.1uF DP_EXTA_ML_P<0>
DP_EXTA_ML_C_N<0> C9301 0.1uF DP_EXTA_ML_N<0>
DP_EXTA_ML_C_P<1> C9302 0.1uF DP_EXTA_ML_P<1>
DP_EXTA_ML_C_N<1> C9303 0.1uF DP_EXTA_ML_N<1>
DP_EXTA_ML_C_P<2> C9304 0.1uF DP_EXTA_ML_P<2>
DP_EXTA_ML_C_N<2> C9305 0.1uF DP_EXTA_ML_N<2>
DP_EXTA_ML_C_P<3> C9306 0.1uF DP_EXTA_ML_P<3>
DP_EXTA_ML_C_N<3> C9307 0.1uF DP_EXTA_ML_N<3>
DP_EXTA_AUXCH_C_P C9308 0.1uF DP_EXTA_AUXCH_P
DP_EXTA_AUXCH_C_N C9309 0.1uF DP_EXTA_AUXCH_N

=PP3V3_S0_DPSDRVA → R9309 1M → DP_EXTA_AUXCH_P
DP_EXTA_AUXCH_N → R9308 1M → GND

If GPU uses common pins for AUX_CH and DDC, alias nets together at GPU.

R9308/R9309 maintain bias on C9308/C9309 to prevent spikes when U9310 AUXDDC_OFF transitions from high to low.

=PP3V3_S0_DPSDRVA
C9310 2.2UF, C9311 0.1UF, C9312 0.1UF

PS8301 I2C Addresses:

A1	A0	Addr (W/R)
0	0	0x96/0x97
0	1	0xB6/0xB7
1	0	0x94/0x95
1	1	0xB4/0xB5

Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.

U9310 PS8301TQFN40GTR-A2 QFN CRITICAL

DP_EXTA_ML_P<0>	1	IN_D0P	OUT_D0P 30 DP_SDRVA_ML_C_P<0>
DP_EXTA_ML_N<0>	2	IN_D0N	OUT_D0N 29 DP_SDRVA_ML_C_N<0>
DP_EXTA_ML_P<1>	4	IN_D1P	OUT_D1P 28 DP_SDRVA_ML_C_P<1>
DP_EXTA_ML_N<1>	5	IN_D1N	OUT_D1N 27 DP_SDRVA_ML_C_N<1>
DP_EXTA_ML_P<2>	7	IN_D2P	OUT_D2P 25 DP_SDRVA_ML_C_P<2>
DP_EXTA_ML_N<2>	8	IN_D2N	OUT_D2N 24 DP_SDRVA_ML_C_N<2>
DP_EXTA_ML_P<3>	9	IN_D3P	OUT_D3P 23 DP_SDRVA_ML_C_P<3>
DP_EXTA_ML_N<3>	10	IN_D3N	OUT_D3N 22 DP_SDRVA_ML_C_N<3>
DP_EXTA_DDC_CLK	14	IN_SCL	AC_AUXP 20 DP_SDRVA_AUXCH_C_P
DP_EXTA_DDC_DATA	13	IN_SDA	AC_AUXN 19 DP_SDRVA_AUXCH_C_N
DP_EXTA_AUXCH_P	16	IN_AUXP	OUT_AUXP_SCL 18 (DP_SDRVA_AUXCH_P)
DP_EXTA_AUXCH_N	15	IN_AUXN	OUT_AUXN_SDA 17 (DP_SDRVA_AUXCH_N)
DP_EXTA_HPD	3	IN_HPD	(IPD) OUT_HPD 31 (DP_SDRVA_HPD)
DPSDRVA_I2C_CTL_EN	26	I2C_CTL_EN (IPU)	CA_DET 32 DP_A_CA_DET
DPSDRVA_I2C_ADDR0	36	I2C_ADDR0 (IPD)	CEXT 11 DPSDRVA_CEXT
DPSDRVA_I2C_ADDR1	35	I2C_ADDR1 (IPD)	PLACE_NEAR=U9310.11:2 mm
=I2C_DPSDRVA_SCL	38	SCL_CTL	C9319 2.2UF
=I2C_DPSDRVA_SDA	37	SDA_CTL	
DPSDRVA_REXT	12	REXT	
DP_AUXCH_ISOL	39	AUXDDC_OFF (IPD)	
DP_A_PWRDWN_R	34	PD (IPD)	
	6, 33, 41	GND THMPAD	

NOSTUFF R9311 1K, R9310 1K, R9312 1K

SDRV_PD R9318 0, R9319 4.02K 1%

PS8301 has internal ~150K pull-down on PD pin. Okay to drive this pin even when VCC=0V per Parade (pin is 5V-tolerant).

R9370 390, R9371 390, R9352 390, R9353 390

R9354 22, R9355 22, R9350 22, R9351 22

DP_SDRVA_ML_R_P<0> DP_SDRVA_ML_R_N<0> DP_SDRVA_ML_R_P<2> DP_SDRVA_ML_R_N<2>
→ C9364 0.22UF, C9365 0.22UF, C9360 0.22UF, C9361 0.22UF
→ DP_SDRVA_ML_P<0> DP_SDRVA_ML_N<0> DP_SDRVA_ML_P<2> DP_SDRVA_ML_N<2>

C9363 0.1UF, C9362 0.1UF, C9367 0.1UF, C9366 0.1UF, C9369 0.1UF, C9368 0.1UF

AUXCH Snoop Port, used by PS8301 during training.

T29 A High-Speed Signals

T29_D2R_N<0> T29_D2R_P<0>
T29_R2D_C_N<0> → L9372 1.0NH+/-0.1NH → T29_R2D_C_F_N<0> → C9372 0.47UF → T29_R2D_N<0>
T29_R2D_C_P<0> → L9373 1.0NH+/-0.1NH → T29_R2D_C_F_P<0> → C9373 0.47UF → T29_R2D_P<0>
OVERSIZE_PAD=0.875 mm^2 (Both L's)

T29 signals are P/N-swapped after AC caps to improve layout.

T29_D2R_N<1> T29_D2R_P<1>
T29_R2D_C_N<1> → L9382 1.0NH+/-0.1NH → T29_R2D_C_F_N<1> → C9382 0.47UF → T29_R2D_N<1>
T29_R2D_C_P<1> → L9383 1.0NH+/-0.1NH → T29_R2D_C_F_P<1> → C9383 0.47UF → T29_R2D_P<1>
OVERSIZE_PAD=0.875 mm^2 (Both L's)

(All 4 L's)

T29_A_BIAS_R2D_P0 VOLTAGE=3.3V → C9370 0.47UF → T29_R2D_P<0>
T29_A_BIAS_R2D_N0 VOLTAGE=3.3V → C9371 0.47UF → T29_R2D_N<0>
T29_A_BIAS_R2D_P1 VOLTAGE=3.3V GND_VOID=TRUE (C9380/C9381) → C9380 0.47UF → T29_R2D_P<1>
T29_A_BIAS_R2D_N1 VOLTAGE=3.3V → C9381 0.47UF → T29_R2D_N<1>
GND_VOID=TRUE (C9370/C9371)
(C9372.2) (C9373.2) (C9382.2) (C9383.2) GND_VOID=TRUE

T29 Path Biasing

T29_R2D_P<0> → R9372 1.5K → SIGNAL_MODEL=EMPTY
T29_R2D_N<0> → R9373 1.5K → SIGNAL_MODEL=EMPTY
T29_R2D_N<1> → R9382 1.5K → SIGNAL_MODEL=EMPTY
T29_R2D_P<1> → R9383 1.5K → SIGNAL_MODEL=EMPTY
GND_VOID=TRUE

D9364 D9372 D9373 D9365 BAR90-02LRH TSLP-2-7
GND_VOID=TRUE (D9364.2)
T29: TX_0 T29DPA_ML_C_P<0> T29DPA_ML_C_N<0>
GND_VOID=TRUE (D9372/D9373)
GND_VOID=TRUE (D9365.2)
CRITICAL (All 4 D's)
D9372/D9373: SIGNAL_MODEL=T29PIN
D9364/D9365: SIGNAL_MODEL=EMPTY
R9374 1.5K, R9375 1.5K → GND_VOID=TRUE SIGNAL_MODEL=EMPTY

T29_D2R_C_P<0> T29_D2R_C_N<0> T29_D2R_C_P<1> T29_D2R_C_N<1>

D9360 D9382 D9383 D9361 BAR90-02LRH TSLP-2-7
GND_VOID=TRUE (D9360.2)
T29: TX_1 T29DPA_ML_C_P<2> T29DPA_ML_C_N<2>
GND_VOID=TRUE (D9382/D9383)
GND_VOID=TRUE (D9361.2)
CRITICAL (All 4 D's)
SIGNAL_MODEL=T29PIN (D9382/D9383)
SIGNAL_MODEL=EMPTY (D9360/D9361)
R9384 1.5K, R9385 1.5K → GND_VOID=TRUE SIGNAL_MODEL=EMPTY

DP Path Biasing

DP_A_BIAS_N_2 → R9361 1.5K → R9362 2.51
DP_A_BIAS_P_2 → R9360 1.5K → R9363 2.51
DP_A_BIAS_N_0 → R9365 1.5K → R9366 2.51
DP_A_BIAS_P_0 → R9364 1.5K → R9367 2.51
VOLTAGE=3.3V 5% 1/20W MF 201
Both R's: C9358 0.1UF

=PP3V3_S0_DPSDRVA → C9359 0.1UF
DP_A_PWRDWN → CRITICAL U9359 74LVC1G04DBVCK SC70 → DP_A_BIAS
IC supports input high while Vcc = 0V.

DP/T29 A Low-Speed MUX

PP3V3_SW_DPAPWR Must be 3.3V DP A port power

U9390 CBTL04DP081 HVQFN CRITICAL OMIT

DP_SDRVA_ML_N<3>	31	DIN1_0+	DOUT_0+ 1 T29DPA_ML_N<3>
DP_SDRVA_ML_P<3>	30	DIN1_0-	DOUT_0- 2 T29DPA_ML_P<3>
DP_SDRVA_ML_N<1>	27	DIN1_1+	T29: Unused
DP_SDRVA_ML_P<1>	26	DIN1_1-	
DP_SDRVA_AUXCH_P	19	AUX1+	DOUT_1+ 4 T29DPA_ML_N<1>
DP_SDRVA_AUXCH_N	18	AUX1-	DOUT_1- 5 T29DPA_ML_P<1>
DP_SDRVA_HPD	17	HPD_1	T29: LSX_A_R2P/P2R (P/N)
CKPLUS_WAIVE=NdifPr_badTerm			
T29_A_RSVD_N	25	DIN2_0+	AUX+ 6 DP_A_EXT_AUXCH_P
T29_A_RSVD_P	24	DIN2_0-	AUX- 7 DP_A_EXT_AUXCH_N
(T29_A_LSX_P2R)	23	DIN2_1+	T29: RX_1 Bias Sink
(T29_A_LSX_R2P)	22	DIN2_1-	
T29_D2R1_BIASP	15	AUX2+	HPD_IN 8 DP_A_EXT_HPD
T29_D2R1_BIASN	14	AUX2-	
NC	13	HPD_2	
DP_A_PWRDWN	10	GPU_SEL	LO=Port A HI=Port B
T29_A_BIAS	32	AUX_SEL	
	11	NC	
	29, 20, 16, 12, 9, 3	VDD	
	33, 28, 21	THMPAD GND	

R9399 100K, R9398 100K

R9392 51, R9393 51

R9396 1K, R9397 1K

CBTL04DP081 (353S3151) and PI3VEDP212 (353S3055) are footprint-compatible parts with similar pinouts. NXP uses pin 10 for ML and HPD, Pericom uses pin 11 for HPD.

SIGNAL_MODEL=T29DP_MUX

Note: U9390 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9390 AUX defaults to DP mode because 100-ohm pull-downs would defeat DP Sink's detection of DP Source.

Port A MCU

PP3V3_SW_DPAPWR Must be 3.3V DP A port power
C9330 0.1UF, C9331 0.1UF

U9330 LPC1112A HVQFN25 CRITICAL OMIT_TABLE

DP_A_CA_DET	1	RESET#/PIO0_0	R/PIO1_0/AD1 16 T29DPA_CONFIG1_RC
	2	PIO0_1/CLKOUT	R/PIO1_1/AD2 17 T29DPA_CONFIG2_RC
T29_LSEO<0>	7	PIO0_2/SSEL/CT16B0_CAP0	R/PIO1_2/AD3 18 T29_A_HV_EN_R
=I2C_T29AMCU_SCL	8	PIO0_4/SCL (OD)	(IPU) SWDIO/PIO1_3/AD4 19 T29_A_UC_ADDR
=I2C_T29AMCU_SDA	9	PIO0_5/SDA (OD)	PIO1_4/AD5/WAKEUP 20 DP_A_EXT_HPD
T29DPA_HPD	10	PIO0_6/SCK	PIO1_6/RXD 23 T29_A_LSX_P2R (P2R = PLUG TO RECEPTACLE)
T29_A_BIAS	11	PIO0_7/CTS#	PIO1_7/TXD 24 T29_A_LSX_R2P (R2P = RECEPTACLE TO PLUG)
T29_LSOE<0>	12	PIO0_8/MISO/CT16B0_MAT0	PIO1_8/CT16B1_CAP0 6 T29_LSEO<1>
T29_LSOE<1>	13	PIO0_9/MOSI/CT16B0_MAT1	
	14	SWCLK/PIO0_10/SCK/CT16B0_MAT2 (OD)	
T29_MCU_INT_L	15	R/PIO0_11/AD0 (OD)	XTALIN 4
	3, 21, 25	VSS THRM PAD	

R9338 10K, R9334 10K, R9339 1M, R9335 1K, R9336 10K

I2C Addr: 0x26/0x27 (Wr/Rd)

=T29_WAKE_L:
Desktops use PCIe WAKE#
Mobiles use S4 WAKE#
=T29_WAKE_L → R9330 0 → SWCLK
T29_A_UC_ADDR → R9330 0 → SWDIO

R9330 provides pads for programming/debug of MCU, please make accessible. If project has space for 10-pin programming header it should be used.

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
PAGE TITLE: DisplayPort/T29 A MUXing
Apple Inc.
DRAWING NUMBER: 051-8442 SIZE: D
REVISION: 10.1.0
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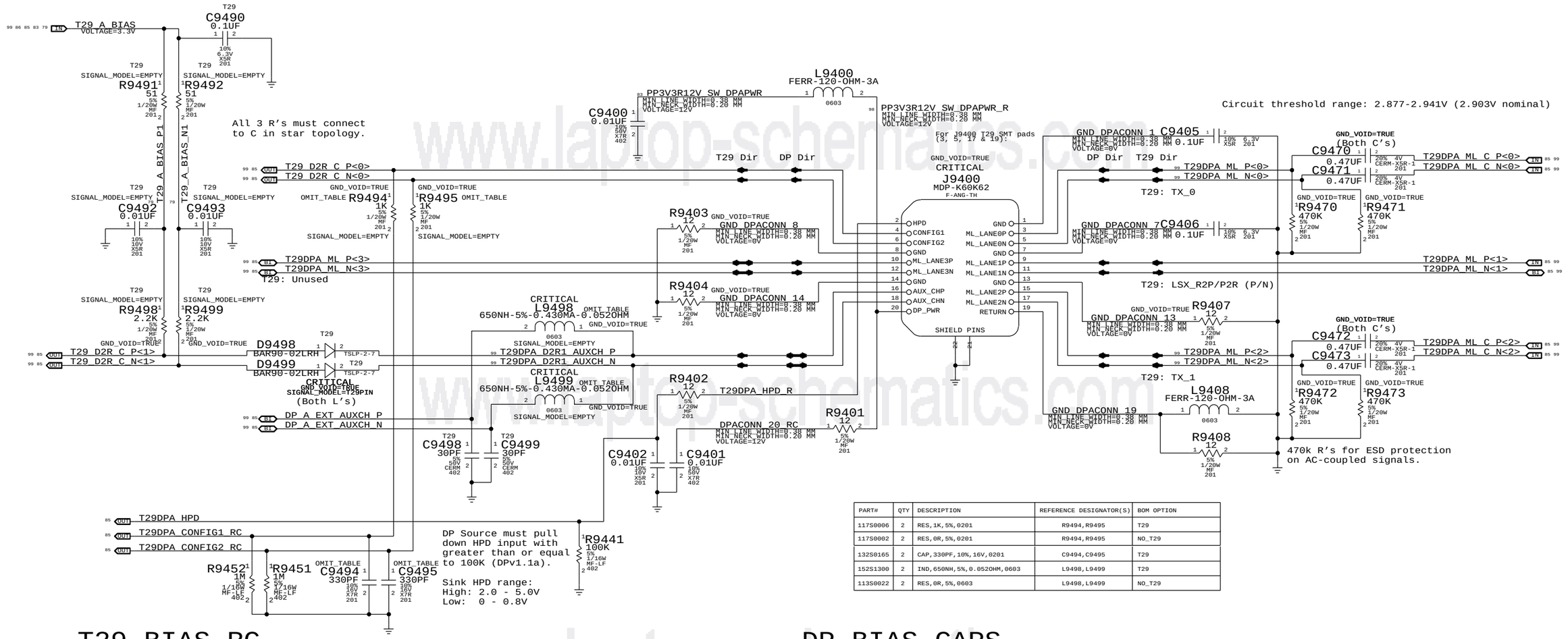
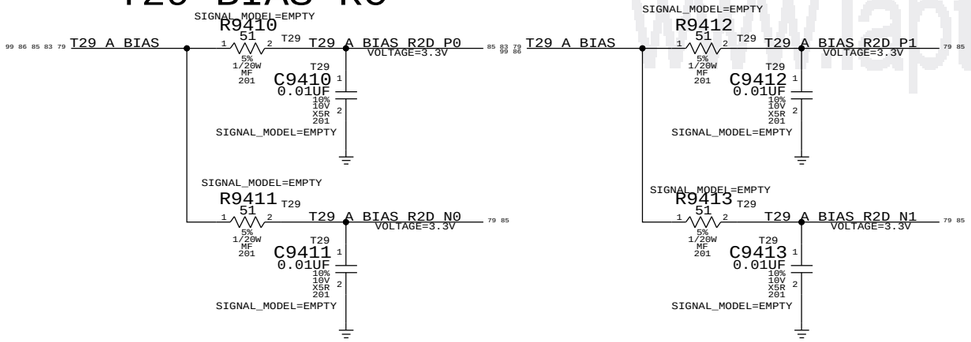
DisplayPort/T29 A Connector

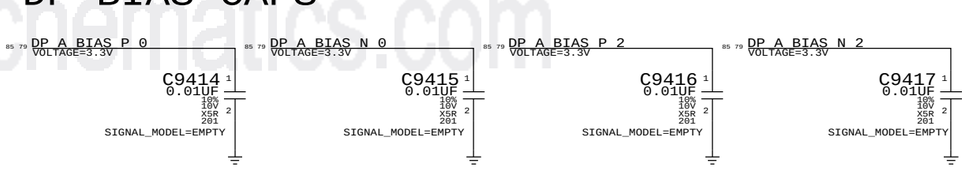


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
117S0006	2	RES,1K,5%,0201	R9494,R9495	T29
117S0002	2	RES,0R,5%,0201	R9494,R9495	NO_T29
132S0165	2	CAP,330PF,10%,16V,0201	C9494,C9495	T29
152S1300	2	IND,650NH,5%,0.052OHM,0603	L9498,L9499	T29
113S0022	2	RES,0R,5%,0603	L9498,L9499	NO_T29

T29 BIAS RC



DP BIAS CAPS



SYNC MASTER=(MASTER) SYNC DATE=(MASTER)

PAGE TITLE: DisplayPort/T29 A Connector

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

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T29 B High-Speed Signals

DP_EXTB_ML_C_P<0> C9500 0.1uF DP_EXTB_ML_P<0>
DP_EXTB_ML_C_N<0> C9501 0.1uF DP_EXTB_ML_N<0>
DP_EXTB_ML_C_P<1> C9502 0.1uF DP_EXTB_ML_P<1>
DP_EXTB_ML_C_N<1> C9503 0.1uF DP_EXTB_ML_N<1>
DP_EXTB_ML_C_P<2> C9504 0.1uF DP_EXTB_ML_P<2>
DP_EXTB_ML_C_N<2> C9505 0.1uF DP_EXTB_ML_N<2>
DP_EXTB_ML_C_P<3> C9506 0.1uF DP_EXTB_ML_P<3>
DP_EXTB_ML_C_N<3> C9507 0.1uF DP_EXTB_ML_N<3>
DP_EXTB_AUXCH_C_P C9508 0.1uF DP_EXTB_AUXCH_P
DP_EXTB_AUXCH_C_N C9509 0.1uF DP_EXTB_AUXCH_N

=PP3V3_S0_DPSDRVB
R9509 1M 5% MF-LF 1/16W 402 DP_EXTB_AUXCH_P
R9508 1M 5% MF-LF 1/16W 402 DP_EXTB_AUXCH_N

If GPU uses common pins for AUX_CH and DDC, alias nets together at GPU.

R9508/R9509 maintain bias on C9508/C9509 to prevent spikes when U9510 AUXDDC_OFF transitions from high to low.

T29_B_BIAS_R2D_P2 VOLTAGE=3.3V
GND_VOID=TRUE (C9570/C9571)
C9570 0.47uF CERM-X5R-1 201
C9571 0.47uF CERM-X5R-1 201
T29_D2R_N<2> T29_D2R_P<2>

OVERSIZE_PAD=0.875 mm^2 (Both L's)
L9572 1.0NH+/-0.1NH 0201-1
L9573 1.0NH+/-0.1NH 0201-1
T29_R2D_C_N<2> T29_R2D_C_P<2>
T29_R2D_C_F_N<2> T29_R2D_C_F_P<2>

(C9572.2) GND_VOID=TRUE
C9572 0.47uF CERM-X5R-1 201
C9573 0.47uF CERM-X5R-1 201
(C9573.2) GND_VOID=TRUE

R9572 1.5K 5% MF 1/20W 201 T29_R2D_P<2>
R9573 1.5K 5% MF 1/20W 201 T29_R2D_N<2>
GND_VOID=TRUE SIGNAL_MODEL=EMPTY

T29_B_BIAS_R2D_N2 VOLTAGE=3.3V
T29_B_BIAS_R2D_P3 VOLTAGE=3.3V
(All 4 L's)

T29 signals are P/N-swapped after AC caps to improve layout.

T29 Path Biasing

T29_D2R_C_P<2> T29_D2R_C_N<2>

D9564 D9572 D9573 D9565 BAR90-02LRH TSLP-2-7
GND_VOID=TRUE (D9564.2)
T29: TX_0
T29DPB_ML_C_P<0> T29DPB_ML_C_N<0>
GND_VOID=TRUE (D9572/D9573)
GND_VOID=TRUE (D9565.2)
CRITICAL (All 4 D's)
D9572/D9573: SIGNAL_MODEL=T29PIN
D9564/D9565: SIGNAL_MODEL=EMPTY
R9574 1.5K 5% MF 1/20W 201 SIGNAL_MODEL=EMPTY
R9575 1.5K 5% MF 1/20W 201 SIGNAL_MODEL=EMPTY

T29_D2R_C_P<3> T29_D2R_C_N<3>

D9560 D9582 D9583 D9561 BAR90-02LRH TSLP-2-7
GND_VOID=TRUE (D9560.2)
T29: TX_1
T29DPB_ML_C_P<2> T29DPB_ML_C_N<2>
GND_VOID=TRUE (D9582/D9583)
GND_VOID=TRUE (D9561.2)
CRITICAL (All 4 D's)
SIGNAL_MODEL=T29PIN (D9582/D9583)
SIGNAL_MODEL=EMPTY (D9560/D9561)
R9584 1.5K 5% MF 1/20W 201 SIGNAL_MODEL=EMPTY
R9585 1.5K 5% MF 1/20W 201 SIGNAL_MODEL=EMPTY

R9582 1.5K 5% MF 1/20W 201 T29_R2D_P<3>
R9583 1.5K 5% MF 1/20W 201 T29_R2D_N<3>
GND_VOID=TRUE SIGNAL_MODEL=EMPTY

T29_B_BIAS_R2D_N3 VOLTAGE=3.3V

T29_R2D_C_N<3> T29_R2D_C_P<3>

OVERSIZE_PAD=0.875 mm^2 (Both L's)
L9582 1.0NH+/-0.1NH 0201-1
L9583 1.0NH+/-0.1NH 0201-1

(C9583.2) GND_VOID=TRUE
C9582 0.47uF CERM-X5R-1 201
C9583 0.47uF CERM-X5R-1 201
(C9583.2) GND_VOID=TRUE

C9580 0.47uF CERM-X5R-1 201
C9581 0.47uF CERM-X5R-1 201
GND_VOID=TRUE (C9580/C9581)

DP Path Biasing

R9561 1.5K R9562 51
R9560 1.5K R9563 51
R9565 1.5K R9566 51
R9564 1.5K R9567 51
Both R's:
C9558 0.1uF

DP B Super-Driver

=PP3V3_S0_DPSDRVB
C9510 2.2UF 20% 6.3V CERM 402-LF
C9511 0.1UF 20% 10V CERM 402
C9512 0.1UF 20% 10V CERM 402

PS8301 I2C Addresses:

A1	A0	Addr (W/R)
0	0	0x96/0x97
0	1	0xB6/0xB7
1	0	0x94/0x95
1	1	0xB4/0xB5

Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.

R9511 1K 5% 1/16W MF-LF 402
R9510 1K 5% 1/16W MF-LF 402
R9512 1K 5% 1/16W MF-LF 402

U9510 PS8301TQFN40GTR-A2 QFN CRITICAL

DP_EXTB_ML_P<0>	1	IN_D0P	OUT_D0P 30 DP_SDRVB_ML_C_P<0>
DP_EXTB_ML_N<0>	2	IN_D0N	OUT_D0N 29 DP_SDRVB_ML_C_N<0>
DP_EXTB_ML_P<1>	4	IN_D1P	OUT_D1P 28 DP_SDRVB_ML_C_P<1>
DP_EXTB_ML_N<1>	5	IN_D1N	OUT_D1N 27 DP_SDRVB_ML_C_N<1>
DP_EXTB_ML_P<2>	7	IN_D2P	OUT_D2P 25 DP_SDRVB_ML_C_P<2>
DP_EXTB_ML_N<2>	8	IN_D2N	OUT_D2N 24 DP_SDRVB_ML_C_N<2>
DP_EXTB_ML_P<3>	9	IN_D3P	OUT_D3P 23 DP_SDRVB_ML_C_P<3>
DP_EXTB_ML_N<3>	10	IN_D3N	OUT_D3N 22 DP_SDRVB_ML_C_N<3>
DP_EXTB_DDC_CLK	14	IN_SCL	AC_AUXP 20 DP_SDRVB_AUXCH_C_P
DP_EXTB_DDC_DATA	13	IN_SDA	AC_AUXN 19 DP_SDRVB_AUXCH_C_N
DP_EXTB_AUXCH_P	16	IN_AUXP	OUT_AUXP_SCL 18 (DP_SDRVB_AUXCH_P)
DP_EXTB_AUXCH_N	15	IN_AUXN	OUT_AUXN_SDA 17 (DP_SDRVB_AUXCH_N)
DP_EXTB_HPD	3	IN_HPD	(IPD) OUT_HPD 31 (DP_SDRVB_HPD)
DPSDRVB_I2C_CTL_EN	26	I2C_CTL_EN (IPU)	CA_DET 32 DP_B_CA_DET
DPSDRVB_I2C_ADDR0	36	I2C_ADDR0 (IPD)	CEXT 11 DPSDRVB_CEXT
DPSDRVB_I2C_ADDR1	35	I2C_ADDR1 (IPD)	
=I2C_DPSDRVB_SCL	38	SCL_CTL	
=I2C_DPSDRVB_SDA	37	SDA_CTL	
DPSDRVB_REXT	12	REXT	
DP_AUXCH_ISOL	39	AUXDDC_OFF (IPD)	
DP_B_PWRDWN_R	34	PD (IPD)	
	6,33,41	GND THMPAD	

C9519 2.2UF 20% 6.3V CERM 402-LF

PS8301 has internal ~150K pull-down on PD pin. Okay to drive this pin even when VCC=0V per Parade (pin is 5V-tolerant).

SDRV_PD R9518 0 5% 1/16W MF-LF 402
R9519 4.02K 1% 1/16W MF-LF 402

R9570 390 5% 1/20W MF 201
R9571 390 5% 1/20W MF 201
R9552 390 5% 1/20W MF 201
R9553 390 5% 1/20W MF 201

R9554 22 5% 1/20W MF 201 DP_SDRVB_ML_R_P<0>
R9555 22 5% 1/20W MF 201 DP_SDRVB_ML_R_N<0>
R9550 22 5% 1/20W MF 201 DP_SDRVB_ML_R_P<2>
R9551 22 5% 1/20W MF 201 DP_SDRVB_ML_R_N<2>

C9564 0.22UF 20% 6.3V X5R 0201 DP_SDRVB_ML_P<0>
C9565 0.22UF 20% 6.3V X5R 0201 DP_SDRVB_ML_N<0>
C9560 0.22UF 20% 6.3V X5R 0201 DP_SDRVB_ML_P<2>
C9561 0.22UF 20% 6.3V X5R 0201 DP_SDRVB_ML_N<2>

C9563 0.1UF 10% 16V X5R-CERM 0201
C9562 0.1UF 10% 16V X5R-CERM 0201
C9567 0.1UF 10% 16V X5R-CERM 0201
C9566 0.1UF 10% 16V X5R-CERM 0201
C9569 0.1UF 10% 16V X5R 402
C9568 0.1UF 10% 16V X5R 402

AUXCH Snoop Port, used by PS8301 during training.

=PP3V3_S0_DPSDRVB
C9559 0.1UF 10% 16V X5R 402
U9559 74LVC1G04DBDCK SC70 CRITICAL
DP_B_PWRDWN DP_B_BIAS

IC supports input high while Vcc = 0V.

DP/T29 B Low-Speed MUX

PP3V3_SW_DPBPWR Must be 3.3V DP B port power
C9590 0.1UF 10% 16V X5R 402
C9591 0.1UF 10% 16V X5R 402
R9599 100K 5% 1/16W MF-LF 402

U9590 CBTL04DP081 HVQFN

DP_SDRVB_ML_N<3>	31	DIN1_0+	DOUT_0+ 1 T29DPB_ML_N<3>
DP_SDRVB_ML_P<3>	30	DIN1_0-	DOUT_0- 2 T29DPB_ML_P<3>
DP_SDRVB_ML_N<1>	27	DIN1_1+	T29: Unused
DP_SDRVB_ML_P<1>	26	DIN1_1-	DOUT_1+ 4 T29DPB_ML_N<1>
DP_SDRVB_AUXCH_P	19	AUX1+	DOUT_1- 5 T29DPB_ML_P<1>
DP_SDRVB_AUXCH_N	18	AUX1-	T29: LSX_B_R2P/P2R (P/N)
DP_SDRVB_HPD	17	HPD_1	AUX+ 6 DP_B_EXT_AUXCH_P
CKPLUS_WAIVE=NdifPr_badTerm			AUX- 7 DP_B_EXT_AUXCH_N
T29_B_RSVD_N	25	DIN2_0+	T29: RX_3 Bias Sink
T29_B_RSVD_P	24	DIN2_0-	HPD_IN 8 DP_B_EXT_HPD
(T29_B_LSX_P2R)	23	DIN2_1+	
(T29_B_LSX_R2P)	22	DIN2_1-	
T29_D2R3_BIASP	15	AUX2+	
T29_D2R3_BIASN	14	AUX2-	
	13	HPD_2	
DP_B_PWRDWN	10	GPU_SEL	
T29_B_BIAS	32	AUX_SEL	LO=Port A HI=Port B
	11	NC	
	29,20,16,12,9,3	VDD	
	33,28,21	THMPAD GND	

CRITICAL
OMIT
CRITICAL
SIGNAL_MODEL=T29DP_MUX

R9596 1K 5% 1/16W MF-LF 402
R9597 1K 5% 1/16W MF-LF 402
R9598 100K 5% 1/16W MF-LF 402

CBTL04DP081 (353S3151) and PI3vEDP212 (353S3055) are footprint-compatible parts with similar pinouts. NXP uses pin 10 for ML and HPD, Pericom uses pin 11 for HPD.

Port B MCU

PP3V3_SW_DPBPWR Must be 3.3V DP B port power
C9530 0.1UF 20% 10V CERM 402
C9531 0.1UF 20% 10V CERM 402
R9538 10K 5% 1/16W MF-LF 402

U9530 LPC1112A HVQFN25 CRITICAL OMIT_TABLE

DP_B_CA_DET	1	RESET#/PIO0_0	R/PIO1_0/AD1 16 T29DPB_CONFIG1_RC
T29_LSEO<2>	2	PIO0_1/CLKOUT	R/PIO1_1/AD2 17 T29DPB_CONFIG2_RC
	7	PIO0_2/SSEL/CT16B0_CAP0	R/PIO1_2/AD3 18 T29_B_HV_EN_R
=I2C_T29BMCU_SCL	8	PIO0_4/SCL (OD)	(IPU) SWDIO/PIO1_3/AD4 19 T29_B_UC_ADDR
=I2C_T29BMCU_SDA	9	PIO0_5/SDA (OD)	PIO1_4/AD5/WAKEUP 20 DP_B_EXT_HPD
T29DPB_HPD	10	PIO0_6/SCK	PIO1_6/RXD 23 T29_B_LSX_P2R
T29_B_BIAS	11	PIO0_7/CTS#	PIO1_7/TXD 24 T29_B_LSX_R2P
T29_LSOE<2>	12	PIO0_8/MISO/CT16B0_MAT0	PIO1_8/CT16B1_CAP0 6 T29_LSEO<3>
T29_LSOE<3>	13	PIO0_9/MOSI/CT16B0_MAT1	
	14	SWCLK/PIO0_10/SCK/CT16B0_MAT2 (OD)	
T29_MCU_INT_L	15	R/PIO0_11/AD0 (OD)	XTALIN 4
	3,21,25	VSS THRM PAD	

R9535 1K 5% 1/16W MF-LF 402
R9536 10K 5% 1/16W MF-LF 402
R9537 4.7K 5% 1/16W MF-LF 402

I2C Addr: 0x24/0x25 (Wr/Rd)

R9534 10K 5% 1/16W MF-LF 402 T29_B_HV_EN

P2R = Plug to Receptacle
R2P = Receptacle to Plug

R9539 1M 5% 1/16W MF-LF 402

=T29_WAKE_L:
Desktops use PCIe WAKE#
Mobiles use S4 WAKE#

=T29_WAKE_L
OMIT R9530 0 5% 1/16W MF-LF 402 SWCLK SWDIO
T29_B_UC_ADDR

R9530 provides pads for programming/debug of MCU, please make accessible.
If project has space for 10-pin programming header it should be used.

Note: U9590 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9590 AUX defaults to DP mode because 100-ohm pull-downs would defeat DP Sink's detection of DP Source.

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
PAGE TITLE: DisplayPort/T29 B MUXing
Apple Inc.
DRAWING NUMBER: 051-8442 SIZE: D
REVISION: 10.1.0
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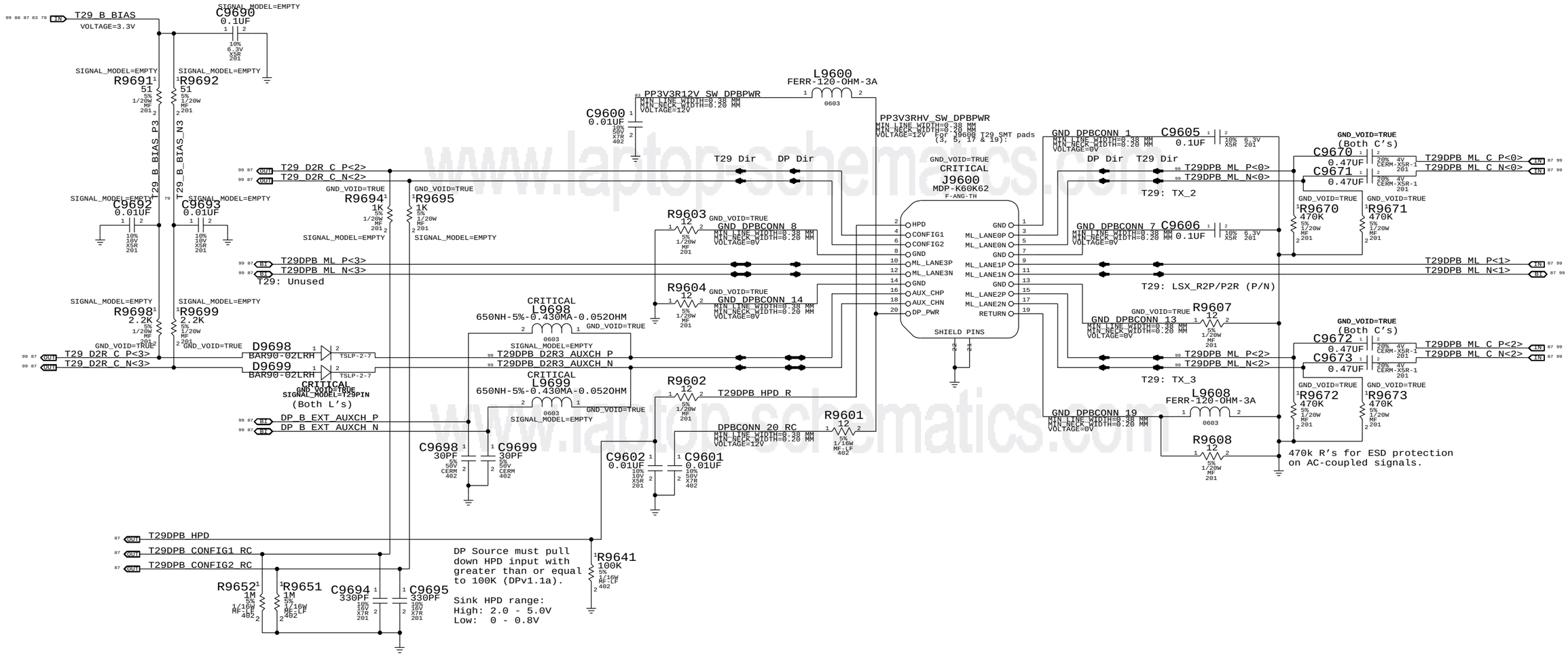
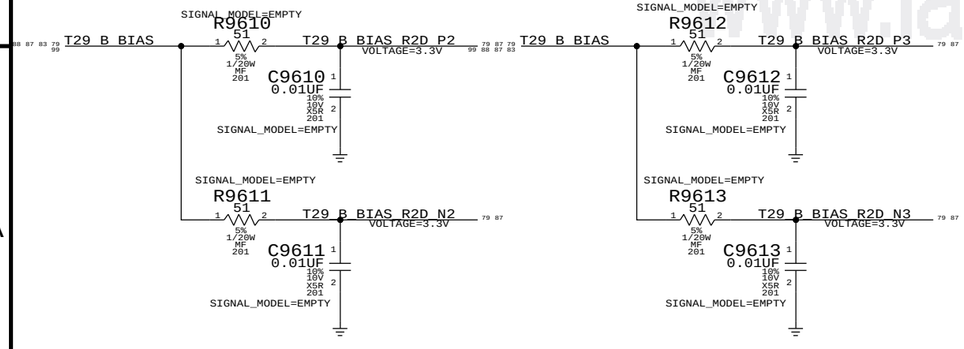
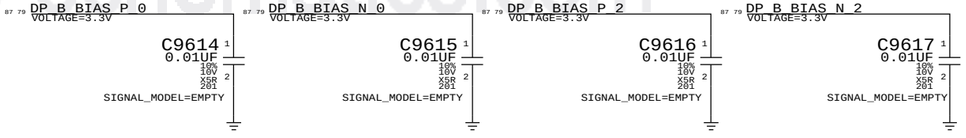
DisplayPort/T29 B Connector



T29 BIAS RC



DP BIAS CAPS



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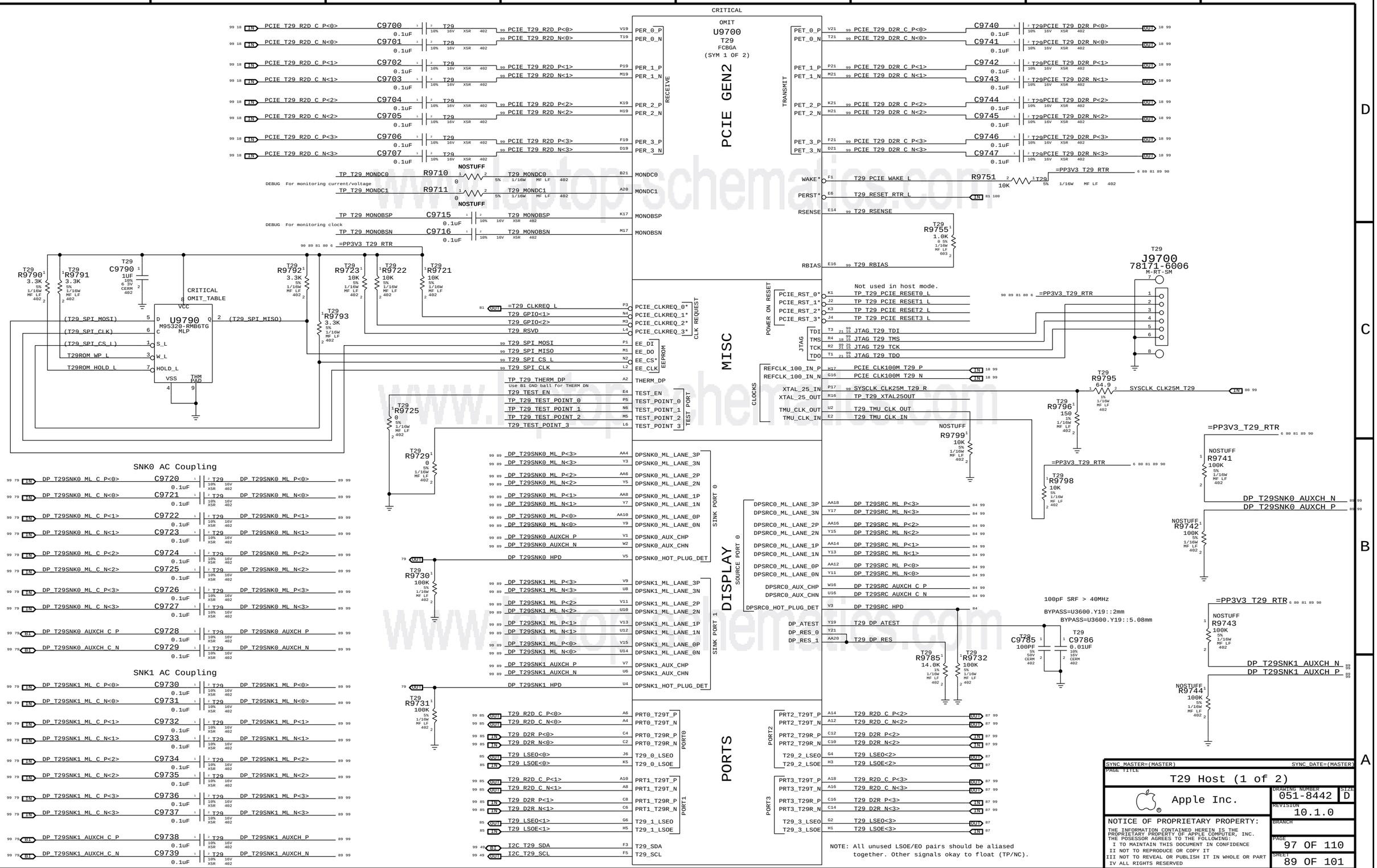

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6 =PP1V05_T29_RTR
2100 mA (Single Port)
2250 mA (Dual Port)
EDP: 3000 mA

CRITICAL

OMIT
U9700
T29
FCBGA
(SYM 2 OF 2)

VCC

H9	VCC1P0	VCC3P3	H7
H11	VCC1P0	VCC3P3	M7
H13	VCC1P0	VCC3P3	K7
K9	VCC1P0	VCC3P3_T29	G10
K11	VCC1P0	VCC3P3_T29	G12
K13	VCC1P0		
M9	VCC1P0		
M11	VCC1P0		
M13	VCC1P0	VCC3P3_DP_RX1	P7
		VCC3P3_DP_RX1	R6
H15	VCC1P0_PE	VCC3P3_DP_TXRX	P9
K15	VCC1P0_PE	VCC3P3_DP_TXRX	P11
M15	VCC1P0_PE		
E8	VCC1P0_PE		
E10	VCC1P0_PE		
E12	VCC1P0_PE		
G14	VCC1P0_PE		
R8	VDD1P0_DP_RX1	VDD3P3DP_PLL	P13
R10	VDD1P0_DP_TXRX		
R12	VDD1P0_DP_TXRX		
R14	VDD1P0_DP_PLL	VCC3P3_DP_TXRXBIAS	P15

GND

G8	VSS	VSSDP	T5
J8	VSS	VSSDP	T7
J10	VSS	VSSDP	T9
J12	VSS	VSSDP	T11
J14	VSS	VSSDP	T15
L8	VSS	VSSDP	T17
L10	VSS	VSSDP	V17
L12	VSS	VSSDP	W4
L14	VSS	VSSDP	W6
N8	VSS	VSSDP	W8
N10	VSS	VSSDP	W10
N12	VSS	VSSDP	W12
N14	VSS	VSSDP	W14
		VSSDP	Y1
		VSSDP	AA2
B1	VSSPE	VSSDP_PLL	T13
B3	VSSPE		
B5	VSSPE	VSSPE	F9
B7	VSSPE	VSSPE	F11
B9	VSSPE	VSSPE	F13
B11	VSSPE	VSSPE	F15
B13	VSSPE	VSSPE	F17
B15	VSSPE	VSSPE	G18
B17	VSSPE	VSSPE	G20
B19	VSSPE	VSSPE	J16
C18	VSSPE	VSSPE	J18
C20	VSSPE	VSSPE	J20
D1	VSSPE	VSSPE	L16
D3	VSSPE	VSSPE	L18
D5	VSSPE	VSSPE	L20
D7	VSSPE	VSSPE	N16
D9	VSSPE	VSSPE	N18
D11	VSSPE	VSSPE	N20
D13	VSSPE	VSSPE	R18
D15	VSSPE	VSSPE	R20
D17	VSSPE	VSSPE	U18
E18	VSSPE	VSSPE	U20
E20	VSSPE	VSSPE	W18
F7	VSSPE	VSSPE	W20

T29 C9800 10UF 20% 6.3V XSR 603
T29 C9801 10UF 20% 6.3V XSR 603
T29 C9805 1UF 10% 6.3V CERM 402
T29 C9806 1UF 10% 6.3V CERM 402
T29 C9807 1UF 10% 6.3V CERM 402
T29 C9808 1UF 10% 6.3V CERM 402
T29 C9809 1UF 10% 6.3V CERM 402
T29 C9810 1UF 10% 6.3V CERM 402
T29 C9811 1UF 10% 6.3V CERM 402
T29 C9812 1UF 10% 6.3V CERM 402
T29 C9813 1UF 10% 6.3V CERM 402
T29 C9814 1UF 10% 6.3V CERM 402

T29 R9820 0 5% 1/16W MF LF 402
PP1V05_T29_VDD_DP
MIN LINE WIDTH=0.4 mm
MIN NECK WIDTH=0.2 mm
VOLTAGE=1.05V

T29 C9820 1UF 10% 6.3V CERM 402
T29 C9821 1UF 10% 6.3V CERM 402
T29 C9822 1UF 10% 6.3V CERM 402

T29 L9830 FERR-120-OHM-1.5A 0402
PP1V05_T29_VDD_DPPLL
MIN LINE WIDTH=0.4 mm
MIN NECK WIDTH=0.2 mm
VOLTAGE=1.05V

T29 C9830 2.2UF 20% 6.3V CERM 402 LF

T29 C9844 1UF 10% 6.3V CERM 402
T29 C9843 1UF 10% 6.3V CERM 402
T29 C9845 1UF 10% 6.3V CERM 402
T29 C9846 10UF 20% 6.3V XSR 603
T29 C9847 10UF 20% 6.3V XSR 603

T29 C9853 1UF 10% 6.3V CERM 402
T29 C9852 1UF 10% 6.3V CERM 402
T29 C9851 1UF 10% 6.3V CERM 402
T29 C9850 1UF 10% 6.3V CERM 402

PP3V3_T29_DP
MIN LINE WIDTH=0.4 mm
MIN NECK WIDTH=0.2 mm
VOLTAGE=3.3V

T29 R9850 0 5% 1/16W MF LF 402

T29 C9860 2.2UF 20% 6.3V CERM 402 LF
PP3V3_T29_PLL
MIN LINE WIDTH=0.4 mm
MIN NECK WIDTH=0.2 mm
VOLTAGE=3.3V

T29 R9860 0 5% 1/16W MF LF 402

T29 C9870 2.2UF 20% 6.3V CERM 402 LF
PP3V3_T29_DPBIAS
MIN LINE WIDTH=0.4 mm
MIN NECK WIDTH=0.2 mm
VOLTAGE=3.3V

T29 L9870 FERR-120-OHM-1.5A 0402

=PP3V3_T29_RTR 6 80 81 89
135 mA (Single-Port)
152 mA (Dual-Port)
EDP: 200 mA

0-ohms are placeholders for now, replace with proper values after characterization.

Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

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K60/62 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OF MM)	ALLEGRO VERSION
TOP ISL2 ISL3 ISL4 ISL5 ISL6 ISL7 BOTTOM	NO TYPE BGA BGA P1MM	MM	15 5 1

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50 OHM SE	=50 OHM SE	100 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12 7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
34 OHM SE	TOP BOTTOM	Y	0 21 MM	0 090 MM	=STANDARD		
34 OHM SE	*	Y	0 19 MM	0 090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39 OHM SE	TOP BOTTOM	Y	0 175 MM	0 090 MM	=STANDARD		
39 OHM SE	*	Y	0 159 MM	0 090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42 OHM SE	TOP BOTTOM	Y	0 151 MM	0 090 MM	=STANDARD		
42 OHM SE	*	Y	0 135 MM	0 090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50 OHM SE	TOP BOTTOM	Y	0 1 MM	0 085 MM	15 MM		
50 OHM SE	*	Y	0 1 MM	0 085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55 OHM SE	TOP BOTTOM	Y	0 085 MM	0 085 MM	=STANDARD		
55 OHM SE	*	Y	0 076 MM	0 076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
68 OHM DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
68 OHM DIFF	ISL3 ISL6	Y	0 16 MM	0 090 MM	=STANDARD	0 13 MM	0 1 MM
68 OHM DIFF	TOP BOTTOM	Y	0 165 MM	0 090 MM	=STANDARD	0 13 MM	0 1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85 OHM DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85 OHM DIFF	ISL3 ISL6	Y	0 115 MM	0 085 MM	=STANDARD	0 2 MM	0 1 MM
85 OHM DIFF	TOP BOTTOM	Y	0 125 MM	0 085 MM	=STANDARD	0 2 MM	0 1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90 OHM DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90 OHM DIFF	ISL3 ISL6	Y	0 099 MM	0 085 MM	12 MM	0 2 MM	0 1 MM
90 OHM DIFF	TOP BOTTOM	Y	0 110 MM	0 085 MM	=STANDARD	0 2 MM	0 1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100 OHM DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100 OHM DIFF	ISL3 ISL6	Y	0 081 MM	0 081 MM	=STANDARD	0 25 MM	0 1 MM
100 OHM DIFF	TOP BOTTOM	Y	0 091 MM	0 085 MM	=STANDARD	0 25 MM	0 1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110 OHM DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110 OHM DIFF	ISL3 ISL6	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110 OHM DIFF	TOP BOTTOM	Y	0 075 MM	0 075 MM	=STANDARD	0 320 MM	0 15 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1 1 DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0 1 MM	0 085 MM
POWER WIDTH	*	Y	0 600 MM	0 200 MM	3 0 MM	=STANDARD	=STANDARD
POWER CTL	*	Y	0 300 MM	0 200 MM	3 0 MM	=STANDARD	=STANDARD

SPACING RULE SET

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0 1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2 1 SPACING	*	0 2 MM	?
2 5 1 SPACING	*	0 25 MM	?
3 1 SPACING	*	0 3 MM	?
3 5 1 SPACING	*	0 35 MM	?
4 1 SPACING	*	0 4 MM	?
5 1 SPACING	*	0 5 MM	?
6 1 SPACING	*	0 6 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X DIELECTRIC	*	0 155 MM	?
2X DIELECTRIC	TOP BOTTOM	0 145 MM	?
3X DIELECTRIC	*	0 230 MM	?
3X DIELECTRIC	TOP BOTTOM	0 215 MM	?
4X DIELECTRIC	*	0 305 MM	?
4X DIELECTRIC	TOP BOTTOM	0 285 MM	?
5X DIELECTRIC	*	0 380 MM	?
5X DIELECTRIC	TOP BOTTOM	0 355 MM	?
7X DIELECTRIC	*	0 532 MM	?
7X DIELECTRIC	TOP BOTTOM	0 497 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
GND P2MM	*	0 2 MM	1000
PWR P2MM	*	0 2 MM	1000
SWITCHNODE	*	0 8 MM	1000

CONSTRAINTS FOR BGA AREA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA P1MM	*	=DEFAULT	?
BGA P1P5MM	*	0 15 MM	?
BGA P2MM	*	0 2 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA P1MM	BGA P1MM
*	*	BGA	BGA P1MM
MEM CLK	*	BGA	BGA P1P5MM
CLK PCIE	*	BGA	BGA P1MM
CLK LPC	*	BGA	BGA P1MM
CLK PCI	*	BGA	BGA P1MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR CONTROL	*	*	SWITCHNODE
VR CONTROL	VR CONTROL	*	STANDARD
VR CONTROL	SWITCHNODE	*	STANDARD
VR CONTROL	GND	*	STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER	BGA_P1MM	POWER_CTL
POWER	*	POWER_WIDTH
VR_CTL_PHY	BGA_P1MM	DEFAULT
VR_CTL_PHY	*	POWER_CTL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	*	*	STANDARD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER	*	*	STANDARD

BOARD STACK-UP

TOP	HALF OZ	SIGNAL
	0.071	PREPREG
2	TWO OZ	GND
	0.076	PREPREG
3	ONE OZ	SIGNAL
	0.370	PREPREG
4	TWO OZ	POWER
	0.101	CORE
5	TWO OZ	POWER
	0.370	PREPREG
6	ONE OZ	SIGNAL
	0.076	PREPREG
7	TWO OZ	GND
	0.071	PREPREG
BOTTOM	HALF OZ	SIGNAL

BOARD THICKNESS = 62 MIL (1.5748 mm)

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PAGE TITLE: K60/K62 RULE DEFINITIONS

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MEMORY BUS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM 50S	*	=50 OHM SE	=50 OHM SE	=50 OHM SE	=50 OHM SE	=STANDARD	=STANDARD
MEM 42S	*	=42 OHM SE	=42 OHM SE	=42 OHM SE	=42 OHM SE	=STANDARD	=STANDARD
MEM 39S	*	=39 OHM SE	=39 OHM SE	=39 OHM SE	=39 OHM SE	=STANDARD	=STANDARD
MEM 34S	*	=34 OHM SE	=34 OHM SE	=34 OHM SE	=34 OHM SE	=STANDARD	=STANDARD
MEM 68D	*	=68 OHM DIFF	=68 OHM DIFF	=68 OHM DIFF	=68 OHM DIFF	=68 OHM DIFF	=68 OHM DIFF
MEM 42S D	*	=42 OHM SE	=42 OHM SE	=42 OHM SE	=42 OHM SE	0 1016 MM	0 1016 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM CLK2MEM	*	=5 1 SPACING	?
MEM CTRL2CTRL	*	=2 5 1 SPACING	?
MEM CTRL2MEM	*	=3 5 1 SPACING	?
MEM CMD2CMD	*	=2 1 SPACING	?
MEM CMD2MEM	*	=3 5 1 SPACING	?
MEM DQ SAMEBYTE	*	=3 1 SPACING	?
MEM DQ DIFFBYTE	*	=5 1 SPACING	?
MEM DATA2MEM	*	=4 1 SPACING	?
MEM DQS2MEM	*	=4 1 SPACING	?
MEM 2OTHER	*	=5 1 SPACING	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM CLK	MEM CLK	*	MEM CLK2MEM
MEM CLK	*	*	MEM 2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM CMD	MEM CTRL	*	MEM CMD2MEM
MEM CMD	MEM CMD	*	MEM CMD2CMD
MEM CMD	*	*	MEM 2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM CTRL	MEM CTRL	*	MEM CTRL2CTRL
MEM CTRL	*	*	MEM 2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM DQS	MEM CTRL	*	MEM DQS2MEM
MEM DQS	MEM CMD	*	MEM DQS2MEM
MEM DQS	MEM DQ BYTE0	*	MEM DQS2MEM
MEM DQS	MEM DQ BYTE1	*	MEM DQS2MEM
MEM DQS	MEM DQ BYTE2	*	MEM DQS2MEM
MEM DQS	MEM DQ BYTE3	*	MEM DQS2MEM
MEM DQS	MEM DQ BYTE4	*	MEM DQS2MEM
MEM DQS	MEM DQ BYTE5	*	MEM DQS2MEM
MEM DQS	MEM DQ BYTE6	*	MEM DQS2MEM
MEM DQS	MEM DQ BYTE7	*	MEM DQS2MEM
MEM DQS	*	*	MEM 2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM DQ BYTE5	MEM CTRL	*	MEM DATA2MEM
MEM DQ BYTE5	MEM CMD	*	MEM DATA2MEM
MEM DQ BYTE5	MEM DQ BYTE5	*	MEM DQ SAMEBYTE
MEM DQ BYTE5	MEM DQ BYTE6	*	MEM DQ DIFFBYTE
MEM DQ BYTE5	MEM DQ BYTE7	*	MEM DQ DIFFBYTE
MEM DQ BYTE5	*	*	MEM 2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM DQ BYTE6	MEM CTRL	*	MEM DATA2MEM
MEM DQ BYTE6	MEM CMD	*	MEM DATA2MEM
MEM DQ BYTE6	MEM DQ BYTE6	*	MEM DQ SAMEBYTE
MEM DQ BYTE6	MEM DQ BYTE7	*	MEM DQ DIFFBYTE
MEM DQ BYTE6	*	*	MEM 2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM DQ BYTE7	MEM CTRL	*	MEM DATA2MEM
MEM DQ BYTE7	MEM CMD	*	MEM DATA2MEM
MEM DQ BYTE7	MEM DQ BYTE7	*	MEM DQ SAMEBYTE
MEM DQ BYTE7	*	*	MEM 2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM DQ BYTE0	MEM CTRL	*	MEM DATA2MEM
MEM DQ BYTE0	MEM CMD	*	MEM DATA2MEM
MEM DQ BYTE0	MEM DQ BYTE0	*	MEM DQ SAMEBYTE
MEM DQ BYTE0	MEM DQ BYTE1	*	MEM DQ DIFFBYTE
MEM DQ BYTE0	MEM DQ BYTE2	*	MEM DQ DIFFBYTE
MEM DQ BYTE0	MEM DQ BYTE3	*	MEM DQ DIFFBYTE
MEM DQ BYTE0	MEM DQ BYTE4	*	MEM DQ DIFFBYTE
MEM DQ BYTE0	MEM DQ BYTE5	*	MEM DQ DIFFBYTE
MEM DQ BYTE0	MEM DQ BYTE6	*	MEM DQ DIFFBYTE
MEM DQ BYTE0	MEM DQ BYTE7	*	MEM DQ DIFFBYTE
MEM DQ BYTE0	*	*	MEM 2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM DQ BYTE1	MEM CTRL	*	MEM DATA2MEM
MEM DQ BYTE1	MEM CMD	*	MEM DATA2MEM
MEM DQ BYTE1	MEM DQ BYTE1	*	MEM DQ SAMEBYTE
MEM DQ BYTE1	MEM DQ BYTE2	*	MEM DQ DIFFBYTE
MEM DQ BYTE1	MEM DQ BYTE3	*	MEM DQ DIFFBYTE
MEM DQ BYTE1	MEM DQ BYTE4	*	MEM DQ DIFFBYTE
MEM DQ BYTE1	MEM DQ BYTE5	*	MEM DQ DIFFBYTE
MEM DQ BYTE1	MEM DQ BYTE6	*	MEM DQ DIFFBYTE
MEM DQ BYTE1	MEM DQ BYTE7	*	MEM DQ DIFFBYTE
MEM DQ BYTE1	*	*	MEM 2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM DQ BYTE2	MEM CTRL	*	MEM DATA2MEM
MEM DQ BYTE2	MEM CMD	*	MEM DATA2MEM
MEM DQ BYTE2	MEM DQ BYTE2	*	MEM DQ SAMEBYTE
MEM DQ BYTE2	MEM DQ BYTE3	*	MEM DQ DIFFBYTE
MEM DQ BYTE2	MEM DQ BYTE4	*	MEM DQ DIFFBYTE
MEM DQ BYTE2	MEM DQ BYTE5	*	MEM DQ DIFFBYTE
MEM DQ BYTE2	MEM DQ BYTE6	*	MEM DQ DIFFBYTE
MEM DQ BYTE2	MEM DQ BYTE7	*	MEM DQ DIFFBYTE
MEM DQ BYTE2	*	*	MEM 2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM DQ BYTE3	MEM CTRL	*	MEM DATA2MEM
MEM DQ BYTE3	MEM CMD	*	MEM DATA2MEM
MEM DQ BYTE3	MEM DQ BYTE3	*	MEM DQ SAMEBYTE
MEM DQ BYTE3	MEM DQ BYTE4	*	MEM DQ DIFFBYTE
MEM DQ BYTE3	MEM DQ BYTE5	*	MEM DQ DIFFBYTE
MEM DQ BYTE3	MEM DQ BYTE6	*	MEM DQ DIFFBYTE
MEM DQ BYTE3	MEM DQ BYTE7	*	MEM DQ DIFFBYTE
MEM DQ BYTE3	*	*	MEM 2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM DQ BYTE4	MEM CTRL	*	MEM DATA2MEM
MEM DQ BYTE4	MEM CMD	*	MEM DATA2MEM
MEM DQ BYTE4	MEM DQ BYTE4	*	MEM DQ SAMEBYTE
MEM DQ BYTE4	MEM DQ BYTE5	*	MEM DQ DIFFBYTE
MEM DQ BYTE4	MEM DQ BYTE6	*	MEM DQ DIFFBYTE
MEM DQ BYTE4	MEM DQ BYTE7	*	MEM DQ DIFFBYTE
MEM DQ BYTE4	*	*	MEM 2OTHER

Memory Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	NET TYPE SPACING		
	MEM 68D	MEM CLK	MEM_A_CLK_P<3..0>	12 32
	MEM 68D	MEM CLK	MEM_A_CLK_N<3..0>	12 32
	MEM 39S	MEM CTRL	MEM_A_CKE<3..0>	12 30
	MEM 39S	MEM CTRL	MEM_A_CS_L<3..0>	12 30
	MEM 39S	MEM CTRL	MEM_A_ODT<3..0>	12 30
	MEM 34S	MEM CMD	MEM_A_A<15..0>	12 30
	MEM 34S	MEM CMD	MEM_A_BA<2..0>	12 30
	MEM 34S	MEM CMD	MEM_A_RAS_L	12 30
	MEM 34S	MEM CMD	MEM_A_CAS_L	12 30
	MEM 34S	MEM CMD	MEM_A_WE_L	12 30
	MEM 42S	MEM DQ BYTE0	MEM_A_DQ<7..0>	12 32
	MEM 42S	MEM DQ BYTE1	MEM_A_DQ<15..8>	12 32
	MEM 42S	MEM DQ BYTE2	MEM_A_DQ<23..16>	12 32
	MEM 42S	MEM DQ BYTE3	MEM_A_DQ<31..24>	12 32
	MEM 42S	MEM DQ BYTE4	MEM_A_DQ<39..32>	12 32
	MEM 42S	MEM DQ BYTE5	MEM_A_DQ<47..40>	12 32
	MEM 42S	MEM DQ BYTE6	MEM_A_DQ<55..48>	12 32
	MEM 42S	MEM DQ BYTE7	MEM_A_DQ<63..56>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_P<0>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_N<0>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_P<1>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_N<1>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_P<2>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_N<2>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_P<3>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_N<3>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_P<4>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_N<4>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_P<5>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_N<5>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_P<6>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_N<6>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_P<7>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_N<7>	12 32
1177	MEM 50S	PM	MEM_RESET_L	30 31 32 100

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	NET TYPE SPACING		
	MEM 68D	MEM CLK	MEM_B_CLK_P<3..0>	12 32
	MEM 68D	MEM CLK	MEM_B_CLK_N<3..0>	12 32
	MEM 39S	MEM CTRL	MEM_B_CKE<3..0>	12 31
	MEM 39S	MEM CTRL	MEM_B_CS_L<3..0>	12 31
	MEM 39S	MEM CTRL	MEM_B_ODT<3..0>	12 31
	MEM 34S	MEM CMD	MEM_B_A<15..0>	12 31
	MEM 34S	MEM CMD	MEM_B_BA<2..0>	12 31
	MEM 34S	MEM CMD	MEM_B_RAS_L	12 31
	MEM 34S	MEM CMD	MEM_B_CAS_L	12 31
	MEM 34S	MEM CMD	MEM_B_WE_L	12 31
	MEM 42S	MEM DQ BYTE0	MEM_B_DQ<7..0>	12 32
	MEM 42S	MEM DQ BYTE1	MEM_B_DQ<15..8>	12 32
	MEM 42S	MEM DQ BYTE2	MEM_B_DQ<23..16>	12 32
	MEM 42S	MEM DQ BYTE3	MEM_B_DQ<31..24>	12 32
	MEM 42S	MEM DQ BYTE4	MEM_B_DQ<39..32>	12 32
	MEM 42S	MEM DQ BYTE5	MEM_B_DQ<47..40>	12 32
	MEM 42S	MEM DQ BYTE6	MEM_B_DQ<55..48>	12 32
	MEM 42S	MEM DQ BYTE7	MEM_B_DQ<63..56>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_P<0>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_N<0>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_P<1>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_N<1>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_P<2>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_N<2>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_P<3>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_N<3>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_P<4>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_N<4>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_P<5>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_N<5>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_P<6>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_N<6>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_P<7>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_N<7>	12 32

MEMORY MISC PROPERTIES

VOLTAGE	NET TYPE PHYSICAL	NET TYPE SPACING	VOLTAGE		
	MEM POWER PHY	MEM POWER		CPU_DIMM_VREF_A	
	MEM POWER PHY	MEM POWER		CPU_DIMM_VREF_B	
1167	MEM POWER PHY	MEM POWER		CPU_DDR_VREF	11 28
1168	MEM POWER PHY	MEM POWER		VREFMARGIN_DIMMA_DACOUT	28
1169	MEM POWER PHY	MEM POWER		VREFMARGIN_DIMMA_OPFB	28
1170	MEM POWER PHY	MEM POWER		VREFMARGIN_DIMMA_DQ	28
1171	MEM POWER PHY	MEM POWER		CPU_DIMM_VREF_A_SW	
1172	MEM POWER PHY	MEM POWER		VREFMARGIN_DIMMB_DACOUT	28
1173	MEM POWER PHY	MEM POWER		VREFMARGIN_DIMMB_OPFB	28
1174	MEM POWER PHY	MEM POWER		VREFMARGIN_DIMMB_DQ	28
1175	MEM POWER PHY	MEM POWER		CPU_DIMM_VREF_B_SW	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_POWER_WIDTH	*	Y	0.500 MM	0.250 MM	=STANDARD	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_POWER_PHY	*	MEM_POWER_WIDTH

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_POWER	*	=3:1_SPACING	?

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PAGE TITLE: Memory Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE 85D	*	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF
CLK PCIE 90D	*	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=4X DIELECTRIC	?
CLK PCIE	*	0 5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP BOTTOM	=4 1 SPACING	?

CPU

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU 50S	*	=50 OHM SE	=50 OHM SE	=50 OHM SE	=50 OHM SE	=STANDARD	=STANDARD
CPU RCOMP PHY	*	Y	0 254 MM	0 200 MM	3 0 MM	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU ITP	*	0 2 MM	?
CPU RCOMP	*	0 2 MM	?

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA 90D	*	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=6 1 SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP BOTTOM	=6 1 SPACING	?

NET TYPE

ELECTRICAL CONSTRAINT SET	PHYSICAL	SPACING		
SATA				
H50	SATA 90D	SATA	SATA_SSD_R2D_C_P	18 42
H49	SATA 90D	SATA	SATA_SSD_R2D_C_N	18 42
H47	SATA 90D	SATA	SATA_SSD_R2D_P	42
H46	SATA 90D	SATA	SATA_SSD_R2D_N	42
H45	SATA 90D	SATA	SATA_SSD_D2R_P	18 42
H44	SATA 90D	SATA	SATA_SSD_D2R_N	18 42
H43	SATA 90D	SATA	SATA_SSD_D2R_C_P	42
H42	SATA 90D	SATA	SATA_SSD_D2R_C_N	42
PCIE				
H31	PCIE 85D	PCIE	PCIE_USB3_1_R2D_P	
H30	PCIE 85D	PCIE	PCIE_USB3_1_R2D_N	
H29	PCIE 85D	PCIE	PCIE_USB3_1_R2D_C_P	
H28	PCIE 85D	PCIE	PCIE_USB3_1_R2D_C_N	
H27	PCIE 85D	PCIE	PCIE_USB3_1_D2R_P	
H26	PCIE 85D	PCIE	PCIE_USB3_1_D2R_N	
H25	PCIE 85D	PCIE	PCIE_USB3_1_D2R_C_P	
H24	PCIE 85D	PCIE	PCIE_USB3_1_D2R_C_N	
H23	PCIE 85D	PCIE	PCIE_USB3_2_R2D_P	
H22	PCIE 85D	PCIE	PCIE_USB3_2_R2D_N	
H21	PCIE 85D	PCIE	PCIE_USB3_2_R2D_C_P	
H20	PCIE 85D	PCIE	PCIE_USB3_2_R2D_C_N	
H19	PCIE 85D	PCIE	PCIE_USB3_2_D2R_P	
H18	PCIE 85D	PCIE	PCIE_USB3_2_D2R_N	
H17	PCIE 85D	PCIE	PCIE_USB3_2_D2R_C_P	
H16	PCIE 85D	PCIE	PCIE_USB3_2_D2R_C_N	
CPU ITP				
H51	CPU 50S	CPU ITP	XDP_BPM_L<7..0>	11 25
H52	CPU 50S	CPU ITP	CPU_CFG<17..0>	10 15 25
H44	CPU 50S	CPU ITP	XDP_OBSDATA_B<3..0>	25
H43	CPU 50S	CPU ITP	XDP_CPU_CFG<0>	25
H48	CPU 50S	CPU ITP	XDP_CPU_TDO	11 25
H47	CPU 50S	CPU ITP	XDP_CPU_TDI	11 25
H46	CPU 50S	CPU ITP	XDP_CPU_TMS	11 25
H45	CPU 50S	CPU ITP	XDP_CPU_TCK	11 25
H50	CPU 50S	CPU ITP	XDP_CPU_TRST_L	11 25
CPU_MISC				
	CPU RCOMP PHY	CPU RCOMP	CPU_PEG_COMP	10

ANY OTHER LYNNFIELD CONSTRAINTS NOT COVERED ON PAGES 101 AND 107 SHOULD GO ON THIS PAGE TOO

NET TYPE

ELECTRICAL CONSTRAINT SET	PHYSICAL	SPACING		
PCIE GRAPHICS				
	PCIE 85D	PCIE	PEG_R2D_C_P<15..0>	9 78
	PCIE 85D	PCIE	PEG_R2D_C_N<15..0>	9 78
	PCIE 85D	PCIE	PEG_D2R_P<15..0>	9 78
	PCIE 85D	PCIE	PEG_D2R_N<15..0>	9 78
	PCIE 85D	PCIE	MXM_PCIE_R2D_P<7..0>	76 78
	PCIE 85D	PCIE	MXM_PCIE_R2D_N<7..0>	76 78
	PCIE 85D	PCIE	MXM_PCIE_D2R_P<7..0>	76 78
	PCIE 85D	PCIE	MXM_PCIE_D2R_N<7..0>	76 78
PCIE I/O				
	PCIE 85D	PCIE	PCIE_MINI_R2D_P	33
	PCIE 85D	PCIE	PCIE_MINI_R2D_N	33
	PCIE 85D	PCIE	PCIE_MINI_R2D_C_P	18 33
	PCIE 85D	PCIE	PCIE_MINI_R2D_C_N	18 33
	PCIE 85D	PCIE	PCIE_MINI_D2R_P	18 33
	PCIE 85D	PCIE	PCIE_MINI_D2R_N	18 33
	PCIE 85D	PCIE	PCIE_FW_R2D_P	39
	PCIE 85D	PCIE	PCIE_FW_R2D_N	39
	PCIE 85D	PCIE	PCIE_FW_R2D_C_P	18 39
	PCIE 85D	PCIE	PCIE_FW_R2D_C_N	18 39
	PCIE 85D	PCIE	PCIE_FW_D2R_P	18 39
	PCIE 85D	PCIE	PCIE_FW_D2R_N	18 39
	PCIE 85D	PCIE	PCIE_FW_D2R_C_P	39
	PCIE 85D	PCIE	PCIE_FW_D2R_C_N	39
DMI				
H41	CLK PCIE 90D	CLK PCIE	DMI_MIDBUS_CLK100M_N	
H40	CLK PCIE 90D	CLK PCIE	DMI_MIDBUS_CLK100M_P	
H39	CLK PCIE 90D	CLK PCIE	DMI_CLK100M_CPU_N	11 18
H37	CLK PCIE 90D	CLK PCIE	DMI_CLK100M_CPU_P	11 18
	PCIE 85D	PCIE	DMI_S2N_P<3..0>	10 19
	PCIE 85D	PCIE	DMI_S2N_N<3..0>	10 19
	PCIE 85D	PCIE	DMI_N2S_P<3..0>	10 19
	PCIE 85D	PCIE	DMI_N2S_N<3..0>	10 19
PCIE REF CLOCKS				
	CLK PCIE 90D	CLK PCIE	GPU_CLK100M_PCIE_P	9
	CLK PCIE 90D	CLK PCIE	GPU_CLK100M_PCIE_N	9
	CLK PCIE 90D	CLK PCIE	PCIE_CLK100M_MINI_P	18 33
	CLK PCIE 90D	CLK PCIE	PCIE_CLK100M_MINI_N	18 33
	CLK PCIE 90D	CLK PCIE	PCIE_CLK100M_FW_P	18 39
	CLK PCIE 90D	CLK PCIE	PCIE_CLK100M_FW_N	18 39
	ENET 100D	ENET MII	PCIE_CLK100M_ENET_P	18 37
	ENET 100D	ENET MII	PCIE_CLK100M_ENET_N	18 37
SATA				
	SATA 90D	SATA	SATA_HDD_R2D_C_P	18 42
	SATA 90D	SATA	SATA_HDD_R2D_C_N	18 42
	SATA 90D	SATA	SATA_HDD_R2D_P	42
	SATA 90D	SATA	SATA_HDD_R2D_N	42
	SATA 90D	SATA	SATA_HDD_D2R_P	18 42
	SATA 90D	SATA	SATA_HDD_D2R_N	18 42
	SATA 90D	SATA	SATA_HDD_D2R_C_P	42
	SATA 90D	SATA	SATA_HDD_D2R_C_N	42
	SATA 90D	SATA	SATA_ODD_R2D_C_P	18 42
	SATA 90D	SATA	SATA_ODD_R2D_C_N	18 42
	SATA 90D	SATA	SATA_ODD_R2D_P	42
	SATA 90D	SATA	SATA_ODD_R2D_N	42
	SATA 90D	SATA	SATA_ODD_D2R_P	18 42
	SATA 90D	SATA	SATA_ODD_D2R_N	18 42
	SATA 90D	SATA	SATA_ODD_D2R_C_P	42
	SATA 90D	SATA	SATA_ODD_D2R_C_N	42
CLOCKS				
	CLK PCIE 90D	CLK PCIE	PCH_CLK100M_DMI_P	18 26
	CLK PCIE 90D	CLK PCIE	PCH_CLK100M_DMI_N	18 26
	CLK PCIE 90D	CLK PCIE	PCH_CLK96M_DOT_P	18 26
	CLK PCIE 90D	CLK PCIE	PCH_CLK96M_DOT_N	18 26
	CLK PCIE 90D	CLK PCIE	PCH_CLK100M_SATA_P	18 26
	CLK PCIE 90D	CLK PCIE	PCH_CLK100M_SATA_N	18 26
	CLK PCIE 90D	CLK PCIE	ITPXDP_CLK100M_N	18 25
	CLK PCIE 90D	CLK PCIE	ITPXDP_CLK100M_P	18 25
	CLK PCIE 90D	CLK PCIE	ITPCPU_CLK100M_N	11 18
	CLK PCIE 90D	CLK PCIE	ITPCPU_CLK100M_P	11 18
H33	CLK PCIE 90D	CLK PCIE	XDP_CPU_CLK100M_P	25
H38	CLK PCIE 90D	CLK PCIE	XDP_CPU_CLK100M_N	25
UNUSED CLOCKS				
H35	CLK PCIE 90D	CLK PCIE	TP_CLK133M_PCH_N	26
H36	CLK PCIE 90D	CLK PCIE	TP_CLK133M_PCH_P	26
UNUSED PCIE				
H38	PCIE 85D	PCIE	MXM_PCIE_R2D_P<8..15>	76 78
H40	PCIE 85D	PCIE	MXM_PCIE_R2D_N<8..15>	76 78
H42	PCIE 85D	PCIE	MXM_PCIE_D2R_P<8..15>	76 78
H41	PCIE 85D	PCIE	MXM_PCIE_D2R_N<8..15>	76 78

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PCIE/DMI/FDI/SATA CONSTRAINTS

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PCH CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD
CLK PCH 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK PCH	*	=4 1 SPACING	?
COMP PCH	*	0 2 MM	?
ITP PCH	*	0 2 MM	?

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD
CLK PCI 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK PCI	*	0 2 MM	?

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD
CLK LPC 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	0 15 MM	?
CLK LPC	*	0 2 MM	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x DIELECTRIC	?

SPI Interface Constraints

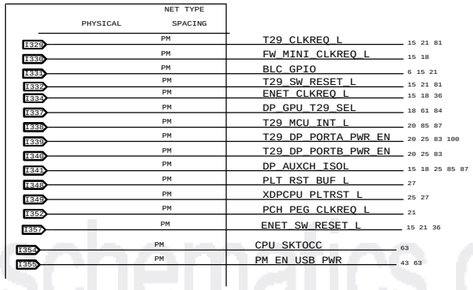
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD

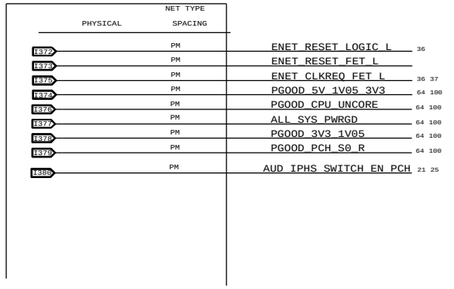
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	0 2 MM	?

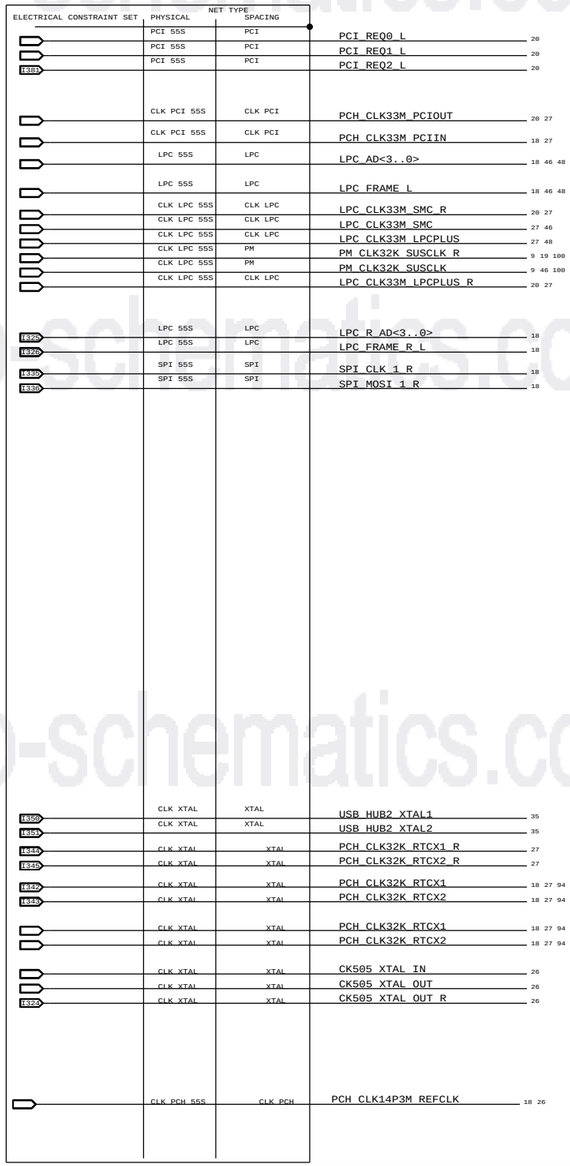
XTAL Constraints

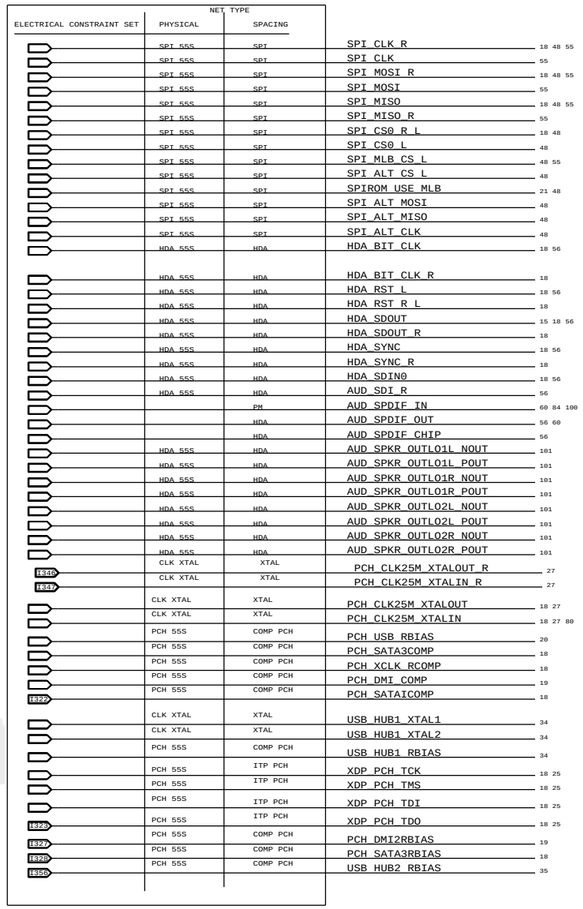
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK XTAL	*	100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X DIELECTRIC	?









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IBEX PEAK CONSTRAINTS

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CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET 50S	*	=50 OHM SE	=50 OHM SE	=50 OHM SE	=50 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET MII	*	0 3 MM	?
ENET SE	*	=STANDARD	?

SOURCE:BROADCOM 5764M-DS04-RDS. PAGE 38

CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET 100D	*	100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET DIFF	*	0 6 MM	?
ENET DIFF2DIFF	*	=3 1 SPACING	?
ENET 2OTHER	*	=50MIL SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
50MIL SPACING	*	1 27 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET DIFF	ENET DIFF	*	ENET DIFF2DIFF
ENET DIFF T	*	*	ENET 2OTHER

CAESAR IV (SD) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD 50S	*	=50 OHM SE	=50 OHM SE	=50 OHM SE	=50 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD	*	=3 1 SPACING	?

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW 110D	*	110 OHM DIFF	=110 OHM DIFF	=110 OHM DIFF	=110 OHM DIFF	=110 OHM DIFF	=110 OHM DIFF

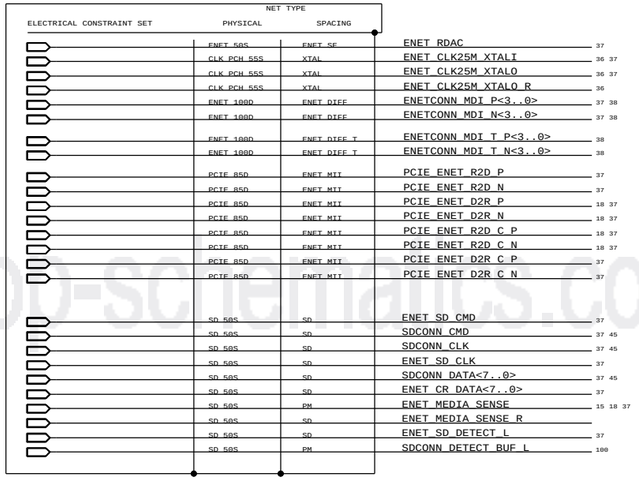
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW TP	*	=3 1 SPACING	?

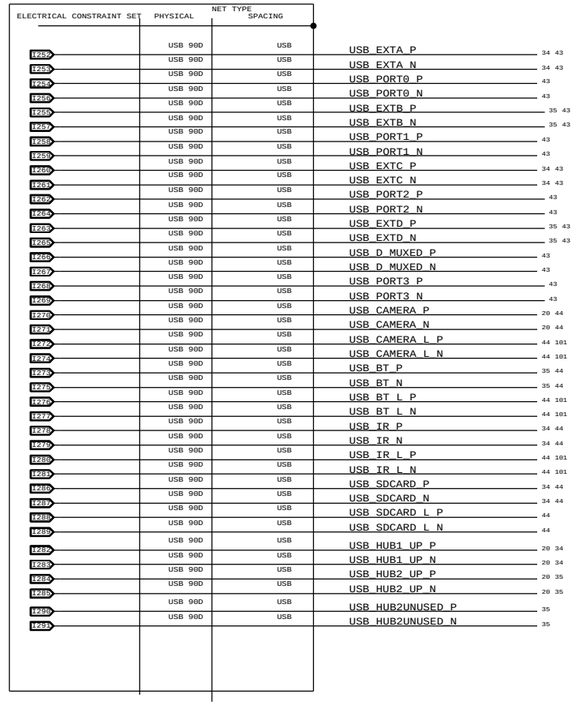
USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB 90D	*	90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF

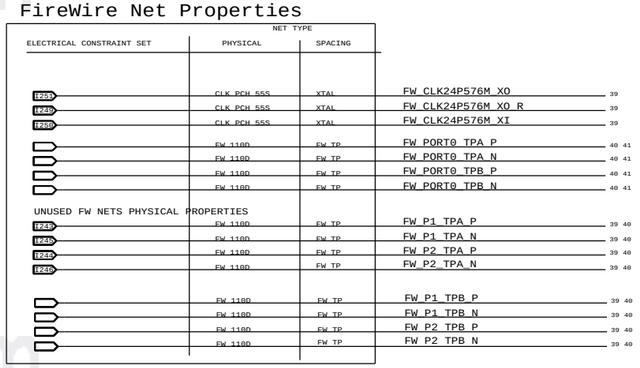
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=3 1 SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP BOTTOM	=4x DIELECTRIC	?





FireWire Net Properties



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USB/ENET/SD/FW/AUD CONSTRAINTS

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GRAPHICS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP 85D	*	85 OHM DIFF	=85 OHM DIFF	0 08MM	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3 1 SPACING	?

USE 5X_DIELECTRIC IN K62

PAIRS SHOULD BE WITHIN 100 MILS OF CLOCK LENGTH.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

ELECTRICAL CONSTRAINT SET
ASSINGED IN CONT. MGR. NET TYPE

	PHYSICAL	SPACING		
T16	DP 85D	DISPLAYPORT	DP_INTCONN_ML_C_P<3..0>	84
T17	DP 85D	DISPLAYPORT	DP_INTCONN_ML_C_N<3..0>	84
	DP 85D	DISPLAYPORT	DP_INTCONN_AUXCH_C_P	84
	DP 85D	DISPLAYPORT	DP_INTCONN_AUXCH_C_N	84
T15	DP 85D	DISPLAYPORT	DP_INTPNL_ML_P<3..0>	82 84
T14	DP 85D	DISPLAYPORT	DP_INTPNL_ML_N<3..0>	82 84
	DP 85D	DISPLAYPORT	DP_INTPNL_AUX_P	82 84
	DP 85D	DISPLAYPORT	DP_INTPNL_AUX_N	82 84
T18	DP 85D	DISPLAYPORT	DP_EXTA_ML_P<3..0>	85
T19	DP 85D	DISPLAYPORT	DP_EXTA_ML_N<3..0>	85
T18	DP 85D	DISPLAYPORT	DP_EXTA_AUXCH_P	85
T19	DP 85D	DISPLAYPORT	DP_EXTA_AUXCH_N	85
T17	DP 85D	DISPLAYPORT	DP_EXTA_ML_C_P<3..0>	79 85
T17	DP 85D	DISPLAYPORT	DP_EXTA_ML_C_N<3..0>	79 85
T17	DP 85D	DISPLAYPORT	DP_EXTA_AUXCH_C_P	79 85
T17	DP 85D	DISPLAYPORT	DP_EXTA_AUXCH_C_N	79 85
T19	DP 85D	DISPLAYPORT	DP_EXTB_ML_P<3..0>	87
T19	DP 85D	DISPLAYPORT	DP_EXTB_ML_N<3..0>	87
T19	DP 85D	DISPLAYPORT	DP_EXTB_AUXCH_P	87
T19	DP 85D	DISPLAYPORT	DP_EXTB_AUXCH_N	87
T19	DP 85D	DISPLAYPORT	DP_EXTB_ML_C_P<3..0>	79 87
T19	DP 85D	DISPLAYPORT	DP_EXTB_ML_C_N<3..0>	79 87
T19	DP 85D	DISPLAYPORT	DP_EXTB_AUXCH_C_P	79 87
T19	DP 85D	DISPLAYPORT	DP_EXTB_AUXCH_C_N	79 87
T19	DP 85D	DISPLAYPORT	MXM_DP_B_ML_P<3..0>	76 79
T20	DP 85D	DISPLAYPORT	MXM_DP_B_ML_N<3..0>	76 79
T20	DP 85D	DISPLAYPORT	MXM_DP_B_AUX_P	76 79
T20	DP 85D	DISPLAYPORT	MXM_DP_B_AUX_N	76 79
T20	DP 85D	DISPLAYPORT	MXM_DP_C_ML_P<3..0>	76 84
T20	DP 85D	DISPLAYPORT	MXM_DP_C_ML_N<3..0>	76 84
T20	DP 85D	DISPLAYPORT	MXM_DP_C_AUX_P	76 84
T20	DP 85D	DISPLAYPORT	MXM_DP_C_AUX_N	76 84
T21	DP 85D	DISPLAYPORT	MXM_DP_C_AUX_R_P	84
T21	DP 85D	DISPLAYPORT	MXM_DP_C_AUX_R_N	84
T20	DP 85D	DISPLAYPORT	MXM_DP_D_ML_P<3..0>	76 79
T20	DP 85D	DISPLAYPORT	MXM_DP_D_ML_N<3..0>	76 79
T20	DP 85D	DISPLAYPORT	MXM_DP_D_AUX_P	76 79
T21	DP 85D	DISPLAYPORT	MXM_DP_D_AUX_N	76 79

UNUSED VIDEO NET PHYSICAL CONSTRAINTS

DP 85D	DISPLAYPORT	MXM_LVDS_A_CLK_P	
DP 85D	DISPLAYPORT	MXM_LVDS_A_CLK_N	
DP 85D	DISPLAYPORT	MXM_LVDS_B_CLK_P	77 79
DP 85D	DISPLAYPORT	MXM_LVDS_B_CLK_N	77 79
DP 85D	DISPLAYPORT	MXM_LVDS_A_DATA_P<3..0>	77 79
DP 85D	DISPLAYPORT	MXM_LVDS_A_DATA_N<3..0>	77 79
DP 85D	DISPLAYPORT	MXM_LVDS_B_DATA_P<3..0>	77 79
DP 85D	DISPLAYPORT	MXM_LVDS_B_DATA_N<3..0>	77 79

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SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	4:1_SPACING
THERMAL	POWER	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR
SNS_DIFF	*	1:1_DIFFPAIR

SMC SMBus Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	NET TYPE SPACING		
	SMB_5S	SMB	SMBUS_SMC_A_S3_SCL	49
	SMB_5S	SMB	SMBUS_SMC_A_S3_SDA	49
	SMB_5S	SMB	SMBUS_SMC_B_S0_SCL	49
	SMB_5S	SMB	SMBUS_SMC_B_S0_SDA	49
	SMB_5S	SMB	SMBUS_SMC_0_S0_SCL	49
	SMB_5S	SMB	SMBUS_SMC_0_S0_SDA	49
	SMB_5S	SMB	SMBUS_SMC_BSA_SCL	49
	SMB_5S	SMB	SMBUS_SMC_BSA_SDA	49
	SMB_5S	SMB	SMBUS_SMC_MGMT_SCL	49 97
	SMB_5S	SMB	SMBUS_SMC_MGMT_SDA	49 97
	SMB_5S	SMB	SMBUS_SMC_MGMT_SCL	49 97
	SMB_5S	SMB	SMBUS_SMC_MGMT_SDA	49 97
	SMB_5S	SMB	SMBUS_PCH_CLK	18 49
	SMB_5S	SMB	SMBUS_PCH_DATA	18 49
	SMB_5S	SMB	SML_PCH_0_CLK	18 49
	SMB_5S	SMB	SML_PCH_0_DATA	18 49
	SMB_5S	SMB	SML_PCH_1_CLK	18 49
	SMB_5S	SMB	SML_PCH_1_DATA	18 49
	CLK_XTAL	XTAL	SMC_EXTAL	46 47
	CLK_XTAL	XTAL	SMC_XTAL	46 47
I254	SMB_5S	SMB	I2C_VREFMRGN_DIMMA_SCL	28
I253	SMB_5S	SMB	I2C_VREFMRGN_DIMMA_SDA	28
I255	SMB_5S	SMB	I2C_VREFMRGN_DIMMB_SCL	28
I254	SMB_5S	SMB	I2C_VREFMRGN_DIMMB_SDA	28
I265	SMB_5S	SMB	SMB_BLC_TCON_SCL	6 49 82
I264	SMB_5S	SMB	SMB_BLC_TCON_SDA	6 49 82
I268	SMB_5S	SMB	I2C_TCON_SCL	82
I269	SMB_5S	SMB	I2C_TCON_SDA	82
I266	SMB_5S	SMB	SMB_BLC_PCH_SCL_R	6
I267	SMB_5S	SMB	SMB_BLC_PCH_SDA_R	6

SMC THERMAL NET PROPERTIES

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	NET TYPE SPACING		
	THERM_DIFF	THERMAL	SNS_T1_1_P	52
	THERM_DIFF	THERMAL	SNS_T1_1_N	52
	THERM_DIFF	THERMAL	SNS_T2_DP2	52
	THERM_DIFF	THERMAL	SNS_T2_DN2	52
I209	THERM_DIFF	THERMAL	SNS_T1_2_P	52
I208	THERM_DIFF	THERMAL	SNS_T1_2_N	52
I207	THERM_DIFF	THERMAL	SNS_T1_3_P	52
I206	THERM_DIFF	THERMAL	SNS_T1_3_N	52
I211	THERM_DIFF	THERMAL	SNS_T1_4_P	52
I212	THERM_DIFF	THERMAL	SNS_T1_4_N	52
I213	THERM_DIFF	THERMAL	SNS_T1_5_P	52
I214	THERM_DIFF	THERMAL	SNS_T1_5_N	52
I215	THERM_DIFF	THERMAL	SNS_T1_6_P	52
I216	THERM_DIFF	THERMAL	SNS_T1_6_N	52
I217	THERM_DIFF	THERMAL	SNS_T1_7_P	52
I218	THERM_DIFF	THERMAL	SNS_T1_7_N	52
I224	THERM_DIFF	THERMAL	SNS_CPU_THERMD_P	10 52
I225	THERM_DIFF	THERMAL	SNS_CPU_THERMD_N	10 52
I219	THERM_DIFF	THERMAL	SNS_LCD_H_P	52
I210	THERM_DIFF	THERMAL	SNS_LCD_H_N	52
	THERM_DIFF	THERMAL	SNS_ODD_P	52 101
	THERM_DIFF	THERMAL	SNS_ODD_N	52 101
	THERM_DIFF	THERMAL	SNS_CPU_H_P	52
	THERM_DIFF	THERMAL	SNS_CPU_H_N	52
I227	THERM_DIFF	THERMAL	SNS_SKIN_RIGHT_P	52 101
I226	THERM_DIFF	THERMAL	SNS_SKIN_RIGHT_N	52 101
	THERM_DIFF	THERMAL	SNS_SKIN_LEFT_P	44 52 101
	THERM_DIFF	THERMAL	SNS_SKIN_LEFT_N	44 52 101
	THERM_DIFF	THERMAL	SNS_AMB_P	52 101
	THERM_DIFF	THERMAL	SNS_AMB_N	52 101
	THERM_DIFF	THERMAL	SNS_MXM_P	52
	THERM_DIFF	THERMAL	SNS_MXM_N	52
		THERMAL	HDD_OOB_TEMP_FILT	42 51 101
		THERMAL	HDD_OOB_TEMP_FB	42
		THERMAL	HDD_OOB_TEMP_R	51
		THERMAL	SMC_HDD_OOB_TEMP	46 51

SMC VOLTAGE/CURRENT NET PROPERTIES

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	NET TYPE SPACING		
	THERM_DIFF	THERMAL	SNS_I_MXM_P	50
	THERM_DIFF	THERMAL	SNS_I_MXM_N	50
	THERM_DIFF	THERMAL	SNS_DIMM_1V5_P	50
	THERM_DIFF	THERMAL	SNS_DIMM_1V5_N	50
	SNS_DIFF	THERMAL	VR_ISNS_VCORE_P	50 98
	SNS_DIFF	THERMAL	VR_ISNS_VCORE_N	50 98
	SNS_DIFF	THERMAL	VR_ISNS_VAXG_P	50 98
	SNS_DIFF	THERMAL	VR_ISNS_VAXG_N	50 98
I243	SNS_DIFF	THERMAL	VR_ISNS_1V05_P	98
I244	SNS_DIFF	THERMAL	VR_ISNS_1V05_N	98
I245	THERM_DIFF	THERMAL	SNS_CPU_1V5_P	50
I246	THERM_DIFF	THERMAL	SNS_CPU_1V5_N	50
I247	THERM_DIFF	THERMAL	SNS_VCCSA_P	50
I248	THERM_DIFF	THERMAL	SNS_VCCSA_N	50
I251	THERM_DIFF	THERMAL	SNS_1V05_PCH_P	50
I252	THERM_DIFF	THERMAL	SNS_1V05_PCH_N	50
I230		THERMAL	GND_SMC_AVSS	46 47 50 97
I241		THERMAL	SMC_CPU_1V5_ISENSE	46 50
I240		THERMAL	SMC_CPU_1V5_ISENSE_R	50
I242		THERMAL	SMC_CPU_1V5_VSENSE	46 50
I230		THERMAL	GND_SMC_AVSS	46 47 50 97
I238		THERMAL	SMC_DIMM_ISENSE	46 50
I239		THERMAL	SMC_DIMM_1V5_R	50
I231		THERMAL	SMC_DIMM_VSENSE	46 50
I230		THERMAL	GND_SMC_AVSS	46 47 50 97
I228		THERMAL	SMC_VCCSA_ISENSE	46 50
I229		THERMAL	SMC_VCCSA_ISENSE_R	50
I227		THERMAL	SMC_VCCSA_VSENSE	46 50
		THERMAL	GND_SMC_AVSS	46 47 50 97
		THERMAL	SMC_PCH_1V05_ISENSE	46 50
		THERMAL	SMC_VAXG_VSENSE	46 50
		THERMAL	SMC_PCH_1V05_VSENSE	46 50
I230		THERMAL	GND_SMC_AVSS	46 47 50 97
I235		THERMAL	SMC_1V05_ISENSE	46 50
I237		THERMAL	SMC_VAXG_ISENSE	46 50
I233		THERMAL	SMC_1V05_VSENSE	46 50
I232		THERMAL	SMC_GPU_ISENSE	46 50
		THERMAL	SMC_GPU_VSENSE	46 50
		THERMAL	SMC_VCORE_ISENSE	46 50
I234		THERMAL	SMC_VCORE_VSENSE	46 50
I236		THERMAL	SMC_CPU_VSENSE	

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NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SWITCHNODE	SWITCHNODE	BGA_P1MM	BGA_P2MM
SWITCHNODE	POWER	BGA_P1MM	BGA_P2MM
SWITCHNODE	GND	BGA_P1MM	BGA_P2MM
SWITCHNODE	*	BGA_P1MM	BGA_P2MM
SWITCHNODE	POWER	*	6:1_SPACING
SWITCHNODE	GND	*	6:1_SPACING
SWITCHNODE	*	*	SWITCHNODE

POWER NET PROPERTIES

PHYSICAL	SPACING	VOLTAGE		
POWER	SWITCHNODE	1 5V	VR_CPU_PHASE1	66
POWER	SWITCHNODE	1 5V	VR_CPU_PHASE2	66
POWER	SWITCHNODE	1 5V	VR_CPU_PHASE3	66
POWER	SWITCHNODE	1 5V	VR_CPU_PHASE4	67
POWER	SWITCHNODE	1 5V	VR_AXG_PHASE1	67
POWER	SWITCHNODE	3 3V	P3V3S5_REG_PHASE	71
POWER	SWITCHNODE	5V	P5VS3_REG_PHASE	71
POWER	SWITCHNODE	1 05V	P1V05S0_PHASE	68
POWER	SWITCHNODE	1 05V	P1V05_REG_PHASE	
POWER	SWITCHNODE	3 4V	P3V42G3H_SW	73
POWER	SWITCHNODE	3 3V	ENET_3V3_S3_SR_IN	37
POWER	SWITCHNODE	1 2V	ENET_SR_LX	36 37
POWER	SWITCHNODE	1 5V	DDR_REG_PHASE	72
POWER	SWITCHNODE	1 8V	P1V8_REG_PHASE	72
POWER	POWER	0 75V	PP0V75_S3_MEM_VREFCA_A	28 30
POWER	POWER	0 75V	PP0V75_S3_MEM_VREFCA_B	28 31
POWER	POWER	0 75V	PP0V75_S3_MEM_VREFDQ_A	28 30
POWER	POWER	0 75V	PP0V75_S3_MEM_VREFDQ_B	28 31
POWER	POWER	12V	PP12V_S0	6
POWER	POWER	12V	PP12V_S0_CPU_FLTRD	65 66 67
POWER	POWER	12V	PP12V_S0_FAN0_L	53 101
POWER	POWER	12V	PP12V_S0_FAN1_L	53 101
POWER	POWER	12V	PP12V_S0_FAN2_L	54 101
POWER	POWER	12V	VR_CPU_DRV1_PVCC	66
POWER	POWER	12V	VR_CPU_DRV1_UVCC	66
POWER	POWER	12V	VR_CPU_DRV2_PVCC	66
POWER	POWER	12V	VR_CPU_DRV2_UVCC	66
POWER	POWER	12V	VR_CPU_DRV3_PVCC	66
POWER	POWER	12V	VR_CPU_DRV3_UVCC	66
POWER	POWER	12V	VR_CPU_DRV4_PVCC	67
POWER	POWER	12V	VR_CPU_DRV4_UVCC	67
POWER	POWER	12V	VR_AXG_DRV1_PVCC	67
POWER	POWER	12V	VR_AXG_DRV1_UVCC	
POWER	POWER	12V	VR_CPU_DRV1_VCC	66
POWER	POWER	12V	VR_CPU_DRV2_VCC	66
POWER	POWER	12V	VR_CPU_DRV3_VCC	66
POWER	POWER	12V	VR_CPU_DRV4_VCC	67
POWER	POWER	12V	PP12V_S0_VG_OK	41
POWER	POWER	12V	P12V_FW_R	41
POWER	POWER	12V	P12V_FW_CL	41
POWER	POWER	12V	P12V_FW_D	41
POWER	POWER	12V	FW_PORT0_VP	41
POWER	POWER	12V	FW_PORT0_VP_F	41
POWER	POWER	12V	PPVP_FW_PHY_CPS	39 41
POWER	POWER	12V	PP12V_S0_P1V05_VREG_VIN	68
POWER	POWER	12V	VCCSA_PWR_RC	69
POWER	POWER	12V	PP12V_S0_BL_R	
POWER	POWER	12V	PP12V_S5_FET	6 75
POWER	POWER	12V	PP12V_LCD	82
POWER	POWER	12V	PP12V_G3H	6
POWER	POWER	12V	PP12V_S5	6
POWER	POWER	12V	PP12V_S5_RSN	75
POWER	POWER	0 75V	PPVTT_S0_DDR	6
POWER	POWER	0 75V	PP0V75_S0	6
POWER	POWER	0 925V	PPVCCSA_S0_CPU	6
POWER	POWER	1 0V	PP1V0_FW_FWPHY_AVDD	39
POWER	POWER	1 0V	PP1V0_S0_FW_VDD	40
POWER	POWER	1 05V	PP1V05_S0_T29	6
POWER	POWER	1 05V	PP1V05_S0_INPUT_VCCSA	6
POWER	POWER	1 05V	PPVAXG_S0	6
POWER	POWER	1 05V	PP1V05_S0	6
POWER	POWER	1 05V	PP1V05_S0_PCH	6
POWER	POWER	1 05V	PP1V05_S0_CK505_F	26
POWER	POWER	1 05V	PPVOUT_S5_PCH_DCPSUS	22
POWER	POWER	1 05V	PP1V05_S0_PCH_VCCADPLLA_F	17 22
POWER	POWER	1 05V	PP1V05_S0_PCH_VCCADPLLB_F	17 22
POWER	POWER	1 05V	PP1V05_S0_PCH_VCCAPLL_EXP_F	22 24
POWER	POWER	1 05V	PP1V05_S0_PCH_VCCAPLLDMI2_F	22 24
POWER	POWER	1 05V	PP1V05_S0_PCH_VCCAPLL_SATA_F	22 24
POWER	POWER	1 05V	PP1V05_S0_PCH_VCCCLKDMI_F	22 24
POWER	POWER	1 1V	PPVCORE_S0_AXG_REG1	67
POWER	POWER	1 1V	PPVCORE_S0_AXG_REGOUT	67
POWER	POWER	1 1V	PPVCORE_S0_CPU	6
POWER	POWER	1 1V	PPVCORE_S0_CPU_REG1	66
POWER	POWER	1 1V	PPVCORE_S0_CPU_REG2	66
POWER	POWER	1 1V	PPVCORE_S0_CPU_REG3	66
POWER	POWER	1 1V	PPVCORE_S0_CPU_REG4	67
VR_CTL_PHY	VR_CTL	1 2V	PP1V2_S3_ENET_INTREG	36
POWER	POWER	1 2V	PP1V2_S3_ENET_PHY_AVDDL	37
POWER	POWER	1 2V	PP1V2_S3_ENET_PHY_PCIEPLL	37
POWER	POWER	1 2V	PP1V2_S3_ENET_PHY_GPHYPLL	37
POWER	POWER	1 5V	PP1V5_S0	6
POWER	POWER	1 5V	PP1V5_S0_CK505_F	26
POWER	POWER	1 5V	PP1V5_S0_CK505_R	26
POWER	POWER	1 5V	PP1V5_S0_CPU_MEM	6
POWER	POWER	1 5V	PP1V5_S0_CPU_SNS	6
POWER	POWER	1 5V	PP1V5_S3	6
POWER	POWER	1 5V	PP1V5_S3_MEM	6

POWER NET PROPERTIES

PHYSICAL	SPACING	VOLTAGE		
POWER	POWER	12V	PP12V_S0_MXM	6
POWER	POWER	12V	PP12V_SLG1	75
POWER	POWER	12V	PP3V3R12V_SW_DPAPWR_1	
POWER	POWER	12V	PP3V3R12V_SW_DPBPWR_1	
POWER	POWER	1 8V	USB_HUB2_VDD1V8	35
POWER	POWER	1 8V	USB_HUB2_VDD1V8PLL	35
POWER	POWER	1 8V	PP1V8_S0	6
POWER	POWER	1 8V	PP1V8R1V5_S0_PCH_VCCVRM_F	22 24
POWER	POWER	1 8V	USB_HUB1_VDD1V8	34
POWER	POWER	1 8V	USB_HUB1_VDD1V8PLL	34
POWER	POWER	1 8V	PP3V3R1V8_ENET_LR_OUT_REG	37
POWER	POWER	3 3V	PPVBAT_G3_SYSCLK_R	80
POWER	POWER	3 3V	USB_HUB1_VDDPLL3V3	34
POWER	POWER	3 3V	USB_HUB1_VDDA3V3	34
POWER	POWER	3 3V	USB_HUB2_VDDPLL3V3	35
POWER	POWER	3 3V	USB_HUB2_VDDA3V3	35
POWER	POWER	3 3V	PP3V3R1V5_PCH_VCCSUSHDA	22 24
POWER	POWER	3 3V	PP3V3_S0_CK505_F	26
POWER	POWER	3 3V	PP3V3_S0_HS_F	62
POWER	POWER	3 3V	PP3V3_S0_SW_SD_PWR	45
POWER	POWER	3 3V	PP3V3_S0_PCH_VCCA_DAC_F	17 22
POWER	POWER	3 3V	PP3V3_S0	6
POWER	POWER	3 3V	PP3V3_SMCUSBMUX	43
POWER	POWER	3 3V	PP3V3_S3	6 101
POWER	POWER	3 3V	PP3V3_S3_BT_FLT	44
POWER	POWER	3 3V	PP3V3_S3_MINI_CONN	33
POWER	POWER	3 3V	PP3V3_S3_SDCARD_FLT	44
POWER	SWITCHNODE	3 3V	PP3V3_S3_ENET_PHY_FET	36
POWER	POWER	3 3V	PP3V3_S3_ENET_PHY_XTALVDDH	37
POWER	POWER	3 3V	PP3V3_S3_ENET_PHY_BIASVDDH	37
POWER	POWER	3 3V	PP3V3_S3_ENET_PHY_AVDDH	37
POWER	POWER	3 3V	ENET_XTALVDDH	37
POWER	POWER	3 3V	PP3V3_S5	6
POWER	POWER	3 3V	PP3V3_S5_REG_R	71
POWER	POWER	3 3V	PPVOUT_S0_PCH_DCPSST	22
POWER	POWER	3 3V	PPVOUT_PCH_DCPSUSBYP	22
POWER	POWER	3 3V	PPVOUT_G3_PCH_DCPRTC	22
POWER	POWER	3 3V	PPVBATT_G3_RTC	27
POWER	POWER	3 3V	PPVBATT_G3_RTC_R	27
POWER	POWER	3 3V	PP3V3_AUDIO_SPDIF_JACK	60 101
POWER	POWER	3 3V	PP3V3_FW_FWPHY_VDDA	39
POWER	POWER	3 3V	PP3V3_FW_FWPHY_VP25	39
POWER	POWER	3 3V	PP3V3_S0_T29	6
POWER	POWER	3 3V	PP3V3_SW_DPAPWR	79 85
POWER	POWER	3 3V	PP3V3_SW_DPBPWR	79 87
POWER	POWER	3 3V	PP3V3_G3H_RTC	18 19 22 27
POWER	POWER	3 3V	PP3V3_G3H_AVREF_SMC	46 47
POWER	POWER	3 4V	PP3V3_G3H_SMC_AVCC	46
POWER	POWER	3 42V	PP3V42_G3H	6
POWER	POWER	4 5V	4V5_REG_IN	56
POWER	POWER	4 5V	PP4V5_AUDIO_ANALOG	56 58 59 61
POWER	POWER	4 5V	PP5V_AUDIO_HPAMP	56
POWER	POWER	5V	PP5V_LAMP_VREG	59
POWER	POWER	5V	PP5V_RAMP_VREG	58
POWER	POWER	5V	PP5V_S0	6 101
POWER	POWER	5V	PP5V_S0_CPU_VCORE_VCC	65
POWER	POWER	5V	PP5V_S0_PCH_V5REF	24
POWER	POWER	5V	PP5V_S0_SATA_FET	42
POWER	POWER	5V	5V_S0_P1V05REG_VIN	68
POWER	POWER	5V	5V_S0_P1V05REG_VDD	68
POWER	POWER	5V	PP5V_S3	6 101
POWER	POWER	5V	PP5V_S3_VREFMRGN_A	28
POWER	POWER	5V	PP5V_S3_VREFMRGN_B	28
POWER	POWER	5V	PP5V_S3_DDR_REG_V5FILT	72
POWER	POWER	5V	PP5V_S3_CAMERA_FLT	44
POWER	POWER	5V	PP5V_S3_REG_R	71
POWER	POWER	5V	PP5V_S3_IR_FLT	44 101
POWER	POWER	5V	PP5V_S5	6
POWER	POWER	5V	PP5V_S5_PCH_V5REFSUS	24
POWER	POWER	5V	PP5V_USB_PORT0	43
POWER	POWER	5V	PP5V_USB_PORT0_F	43
POWER	POWER	5V	PP5V_USB_PORT1	43
POWER	POWER	5V	PP5V_USB_PORT1_F	43
POWER	POWER	5V	PP5V_USB_PORT2	43
POWER	POWER	5V	PP5V_USB_PORT2_F	43
POWER	POWER	5V	PP5V_USB_PORT3	43
POWER	POWER	5V	PP5V_USB_PORT3_F	43
POWER	POWER		DDR_REG_PGND	72
POWER	POWER		DDR_REG_CSGND	72
	POWER	3 3V	PPVDDIO_25M_B	80
	POWER	1 05V	PPVDDIO_25M_A	80
	POWER	3 3V	PPVDDIO_25M_C	80
	POWER	12V	PP3V3R12V_SW_DPAPWR_R	86
	POWER	12V	PP3V3R12V_SW_DPAPWR_D	83
	POWER	1 5V	PP1V5_S0_DP_R	84
POWER	POWER	5V	PP5V_S0_SATA_PORTA1	42
POWER	POWER	5V	PP5V_S0_SATA_PORTA2	42

SENSING NET PROPERTIES

PHYSICAL	SPACING		
SNS DIFF	THERMAL	VR_CPU_ISNS1_P	65 66
SNS DIFF	THERMAL	VR_CPU_ISNS1_N	65 66
SNS DIFF	THERMAL	VR_CPU_ISNS1_R_N	65
SNS DIFF	THERMAL	VR_CPU_ISNS2_P	65 66
SNS DIFF	THERMAL	VR_CPU_ISNS2_N	65 66
SNS DIFF	THERMAL	VR_CPU_ISNS2_R_N	65
SNS DIFF	THERMAL	VR_CPU_ISNS3_P	65 66
SNS DIFF	THERMAL	VR_CPU_ISNS3_N	65 66
SNS DIFF	THERMAL	VR_CPU_ISNS3_R_N	65
SNS DIFF	THERMAL	VR_CPU_ISNS4_P	65 67
SNS DIFF	THERMAL	VR_CPU_ISNS4_N	65 67
SNS DIFF	THERMAL	VR_CPU_ISNS4_R_N	65
SNS DIFF	THERMAL	P1V05S0_ISN	68
SNS DIFF	THERMAL	P1V05S0_ISP	68
SNS DIFF	THERMAL	VR_AXG_ISNS_R_P	65
SNS DIFF	THERMAL	VR_AXG_ISNS_R_N	65
SNS DIFF	THERMAL	VR_AXG_ISNS_N	65 67
SNS DIFF	THERMAL	VR_AXG_ISNS_P	65 67
SNS DIFF	THERMAL	VR_ISNS_1V05_N	97
SNS DIFF	THERMAL	VR_ISNS_1V05_P	97
SNS DIFF	THERMAL	VR_ISNS_VAXG_N	50 97
SNS DIFF	THERMAL	VR_ISNS_VAXG_P	50 97
SNS DIFF	THERMAL	VR_ISNS_VCORE_N	50 97
SNS DIFF	THERMAL	VR_ISNS_VCORE_P	50 97
SNS DIFF		CPU_VAXG_SENSE_P	13 65
SNS DIFF		CPU_VAXG_SENSE_N	13 65
SNS DIFF		VR_AXG_VSNS_R_N	65
SNS DIFF		VR_AXG_VSNS_R_P	65
SNS DIFF		VR_AXG_VSEN	65
SNS DIFF		VR_AXG_RGND	65
SNS DIFF		VR_AXG_VSNS_XW_N	65
SNS DIFF		VR_AXG_VSNS_XW_P	65
SNS DIFF		CPU_VCC_SENSE_N	13 65
SNS DIFF		CPU_VCC_SENSE_P	13 65
SNS DIFF		VR_CPU_VSEN	65
SNS DIFF		VR_CPU_RGND	65
SNS DIFF		VR_CPU_VSNS_R_N	65
SNS DIFF		VR_CPU_VSNS_R_P	65
SNS DIFF		VR_CPU_VSNS_XW_P	65
SNS DIFF		VR_CPU_VSNS_XW_N	65
SNS DIFF		CPU_VCCIO_SENSE_P	13 68
SNS DIFF		CPU_VCCIO_SENSE_N	13 68
SNS DIFF		P1V05S0_VSEN	68
SNS DIFF		P1V05S0_RTN	68

VR CTRL NET PROPERTIES

PHYSICAL	SPACING		
VR CTL PHY	SWITCHNODE	VR_CPU_PH1_SNUB	66
VR CTL PHY	SWITCHNODE	VR_CPU_PH2_SNUB	66
VR CTL PHY	SWITCHNODE	VR_CPU_PH3_SNUB	66
VR CTL PHY	SWITCHNODE	VR_CPU_PH4_SNUB	67
VR CTL PHY	VR CTL	VR_CPU_COMP	65
VR CTL PHY	VR CTL	VR_AXG_TM	65
VR CTL PHY	VR CTL	VR_AXG_PWM_R	65
VR CTL PHY	VR CTL	VR_AXG_PWM	65 67
VR CTL PHY	VR CTL	VR_CPU_PWM2	65 66
VR CTL PHY	VR CTL	VR_CPU_PWM1	65 66
VR CTL PHY	VR CTL	VR_CPU_PWM1_R	65
VR CTL PHY	VR CTL	VR_CPU_PWM2_R	65
VR CTL PHY	VR CTL	VR_CPU_PWM3	65 66
VR CTL PHY	VR CTL	VR_CPU_PWM3_R	65
VR CTL PHY	VR CTL	VR_CPU_PWM4	65 67
VR CTL PHY	VR CTL	VR_CPU_PWM4_R	65
VR CTL PHY	VR CTL	VR_AXG_SW_FREQ	65
VR CTL PHY	VR CTL	VR_EN_PWR_OVP	65
VR CTL PHY	VR CTL	VR_RSET	65
VR CTL PHY	VR CTL	VR_EN_PWR_OVP_R	65
VR CTL PHY	VR CONTROL	VR_CPU_BOOT1_RC	66
VR CTL PHY	VR CONTROL	VR_CPU_BOOT2_RC	66
VR CTL PHY	VR CONTROL	VR_CPU_BOOT3_RC	67
VR CTL PHY	VR CONTROL	VR_AXG_BOOT1_RC	67
VR CTL PHY	VR CTL	VR_CPU_BOOT4_RC	67
VR CTL PHY	VR CONTROL	VR_CPU_DRV1_BOOT	66
VR CTL PHY	VR CTL	VR_CPU_DRV1_GDSEL	66
VR CTL PHY	VR CONTROL	VR_CPU_DRV1_LGATE	66
VR CTL PHY	VR CONTROL	VR_CPU_DRV1_UGATE	66
VR CTL PHY	VR CONTROL	VR_CPU_DRV2_BOOT	66
VR CTL PHY	VR CTL	VR_CPU_DRV2_GDSEL	66
VR CTL PHY	VR CONTROL	VR_CPU_DRV2_LGATE	66
VR CTL PHY	VR CONTROL	VR_CPU_DRV2_UGATE	66
VR CTL PHY	VR CONTROL	VR_CPU_DRV3_BOOT	66
VR CTL PHY	VR CTL	VR_CPU_DRV3_GDSEL	66
VR CTL PHY	VR CONTROL	VR_CPU_DRV3_LGATE	66
VR CTL PHY	VR CONTROL	VR_CPU_DRV3_UGATE	66
VR CTL PHY	VR CONTROL	VR_CPU_DRV4_BOOT	67
VR CTL PHY	VR CTL	VR_CPU_DRV4_GDSEL	67
VR CTL PHY	VR CONTROL	VR_CPU_DRV4_LGATE	67
VR CTL PHY	VR CONTROL	VR_CPU_DRV4_UGATE	67
VR CTL PHY	VR CONTROL	VR_AXG_DRV1_BOOT	67
VR CTL PHY	VR CTL	VR_AXG_DRV1_UGATE_R	67
VR CTL PHY	VR CONTROL	VR_AXG_DRV1_UGATE	67
VR CTL PHY	VR CTL	VR_CPU_SW_FREQ	65
VR CTL PHY	VR CTL	VR_CPU_FB	65
VR CTL PHY	VR CTL	VR_CPU_FB_R	65
VR CTL PHY	VR CTL	VR_CPU_RAMP_ADJ	65
VR CTL PHY	VR CTL	VR_CPU_IMON	50 65
VR CTL PHY	VR CTL	VR_CPU_SUTH	65
VR CTL PHY	VR CTL	VR_CPU_N_PSI	65
VR CTL PHY	VR CTL	VR_CPU_FDVID	65
VR CTL PHY	VR CTL	VR_CPU_PSICOMP	65
VR CTL PHY	VR CTL	VR_CPU_IAUTO	65
VR CTL PHY	VR CTL	VR_CPU_PSICOMP1	65
VR CTL PHY	VR CTL	VR_CPU_PSICOMP2	65
VR CTL PHY	VR CTL	VR_CPU_FB_RC	65
VR CTL PHY	VR CTL	VR_CPU_FB2	65
VR CTL PHY	VR CTL	VR_CPU_IMON_R	65
VR CTL PHY	VR CTL	VR_CPU_HFREQ_COMP	65
VR CTL PHY	SWITCHNODE	VR_AXG_PH1_SNUB	67
VR CTL PHY	VR CTL	VR_AXG_IMON	50 65
VR CTL PHY	VR CTL	VR_AXG_IMON_R	65
VR CTL PHY	VR CTL	VR_AXG_HFREQ_COMP	65
VR CTL PHY	VR CTL	VR_AXG_FB	65
VR CTL PHY	VR CTL	VR_SEN_R1	65
VR CTL PHY	VR CTL	VR_SEN_R2	65
VR CTL PHY	VR CTL	VR_SEN_R3	65
VR CTL PHY	VR CTL	VR_AXG_COMP_RC	65
VR CTL PHY	VR CTL	VR_AXG_COMP	65
VR CTL PHY	VR CTL	VR_AXG_TCOMP	65
VR CTL PHY	SWITCHNODE	P1V05S0_UGATE	68
VR CTL PHY	SWITCHNODE	P1V05S0_LGATE	68
VR CTL PHY	VR CTL	P1V05S0_BOOT	68
VR CTL PHY	VR CTL	P1V05S0_BOOT_R	68
VR CTL PHY	VR CTL	P1V05_IMON	50 68
VR CTL PHY	VR CTL	P1V05S0_FB	68
VR CTL PHY	VR CTL	P1V05S0_PHASE_L	68
VR CTL PHY	VR CTL	P1V05S0_VW	68
VR CTL PHY	VR CTL	P1V05S0_COMP	68
VR CTL PHY	VR CTL	P1V05S0_ICOMP	68
VR CTL PHY	VR CTL	P1V05_S0_VDIFF	68
VR CTL PHY	VR CTL	P1V05S0_COMP_C	68
VR CTL PHY	VR CTL	P1V05S0_VDIF_C	68
VR CTL PHY	VR CTL	P1V05S0_VO	68
VR CTL PHY	VR CTL	P1V05S0_OCSET	68
VR CTL PHY	VR CTL	P1V05S0_SNUBBER	68
VR CTL PHY	VR CTL	P1V05_REG_VFB	
VR CTL PHY	VR CTL	ENET_SR_VFB	36 37
VR CTL PHY	VR CTL	P1V05S0_ISP_R	68
VR CTL PHY	VR CTL	VCCSA_CNTRL_INPUT2_R	69 98
VR CTL PHY	VR CTL	T29BST_FBX	
VR CTL PHY	VR CTL	P3V42G3H_BOOST	73
VR CTL PHY	VR CTL	P3V42G3H_FB	73

VR CTRL NET PROPERTIES

PHYSICAL	SPACING		
VR CTL PHY	VR CTL	DDR_REG_CS	72
VR CTL PHY	VR CTL	DDR_REG_FB	72
VR CTL PHY	VR CONTROL	DDR_REG_LGATE	72
VR CTL PHY	VR CONTROL	DDR_REG_UGATE	72
VR CTL PHY	VR CONTROL	DDR_REG_BOOT	72
VR CTL PHY	VR CONTROL	DDR_REG_BOOT_R	72
VR CTL PHY	VR CTL	DDR_REG_VDDQSNS	72
VR CTL PHY	VR CTL	DDR_REG_VTTSNS	72
VR CTL PHY	VR CTL	DDR_REG_PHASE_R	72
VR CTL PHY	VR CTL	DDR_REG_UGATE_R	72
VR CTL PHY	SWITCHNODE	1V5_SNUBBER	72
VR CTL PHY	VR CTL	P1V8_REG_VFB	72
VR CTL PHY	VR CTL	P1V8_REG_SYNC	72
VR CTL PHY	VR CONTROL	P3V3S5_REG_BOOT	71
VR CTL PHY	VR CONTROL	P3V3S5_REG_BOOT_R	71
VR CTL PHY	VR CTL	P3V3S5_REG_FB	71
VR CTL PHY	VR CTL	P3V3S5_REG_ISEN	71
VR CTL PHY	VR CONTROL	P3V3S5_REG_LGATE	71
VR CTL PHY	VR CTL	P3V3S5_REG_OCSET	71
VR CTL PHY	VR CONTROL	P3V3S5_REG_VOUT1	71
VR CTL PHY	VR CONTROL	P3V3S5_REG_FSET1	71
VR CTL PHY	VR CONTROL	P3V3S5_REG_UGATE	71
VR CTL PHY	VR CTL	P3V3S5_REG_SNUB	71
VR CTL PHY	VR CONTROL	P5VS3_REG_BOOT	71
VR CTL PHY	VR CTL	P5VS3_REG_FB	71
VR CTL PHY	VR CTL	P5VS3_REG_ISEN	71
VR CTL PHY	VR CONTROL	P5VS3_REG_LGATE	71
VR CTL PHY	VR CTL	P5VS3_REG_OCSET	71
VR CTL PHY	VR CTL	P5VS3_REG_FSET2	71
VR CTL PHY	VR CONTROL	P5VS3_REG_UGATE	71
VR CTL PHY	VR CONTROL	P5VS3_REG_VOUT2	71
VR CTL PHY	VR CTL	VCCSA_CNTRL_INPUT1	69
VR CTL PHY	VR CTL	VCCSA_CNTRL_INPUT2	69
VR CTL PHY	VR CTL	VCCSA_CNTRL_INPUT2_R	69 98
VR CTL PHY	VR CTL	VCCSA_OUT	69
VR CTL PHY	VR CTL	VCCSA_GATE	69
VR CTL PHY	VR CTL	VCCSA_REF	69
VR CTL PHY	VR CTL	VCCSA_CRL	69
VR CTL PHY	VR CTL	CPU_VCCSA_SENSE	13 69
VR CTL PHY	VR CTL	VR_CPU_TM	65
VR CTL PHY	PM	3V3R2V9_DPAPWR_ADJ	83 100

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
VID_PHY	*	50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL	*	0.35MM	?

VR VID NET PROPERTIES

PHYSICAL	SPACING		
VID PHY	VR CTL VIDS	CPU_VIDSCLK_R	13
VID PHY	VR CTL VIDS	CPU_VIDALERT_L_R	13
VID PHY	VR CTL VIDS	CPU_VIDSOUT_R	13
VID PHY	VR CTL VIDS	CPU_VIDSCLK	13 65
VID PHY	VR CTL VIDS	CPU_VIDALERT_L	13 65
VID PHY	VR CTL VIDS	CPU_VIDSOUT	13 65

PULL UP STUB < 1 INCH
VID LENGTH SKEW < 1 INCH
VID LENGTH RANGE< 1 TO 15 INCH

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL_VIDS	*	=4X_DIELECTRIC	?

SYNC MASTER=K62_JERRY SYNC DATE=01/09/2011

PAGE TITLE

POWER CONSTRAINTS

Apple Inc.

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T29 ELECTRICAL ROUTES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29 90D	*	90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29	*	=5X DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29	TOP BOTTOM	=7X DIELECTRIC	?

T29 PCI-EXPRESS (SAME RULE AS PCIE)

T29 SPI INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29 SPI 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29 SPI	*	0 2 MM	?

T29 XTAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29 XTAL 100D	*	100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29 XTAL	*	=4X DIELECTRIC	?

T29 SMBUS INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29 SMB 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29 SMB	*	=2x DIELECTRIC	?

GREEN CLOCK CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK 25M 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK 25M	*	=5X DIELECTRIC	?

T29 BIAS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29 COMP	*	0 2 MM	?

T29 NET PROPERTIES

ELECTRICAL CONSTRAINT SET	NET TYPE: PHYSICAL	NET TYPE: SPACING	
NO_TEST=TRUE	T29_90D	T29	T29_R2D_C_P<3..0> 85 87 89
NO_TEST=TRUE	T29_90D	T29	T29_R2D_C_N<3..0> 85 87 89
NO_TEST=TRUE	T29_90D	T29	T29_D2R_C_P<3..0> 85 86 87 88
NO_TEST=TRUE	T29_90D	T29	T29_D2R_C_N<3..0> 85 86 87 88
NO_TEST=TRUE	T29_90D	T29	T29_R2D_P<3..0> 85 87
NO_TEST=TRUE	T29_90D	T29	T29_R2D_N<3..0> 85 87
NO_TEST=TRUE	T29_90D	T29	T29_D2R_P<3..0> 85 87 89
NO_TEST=TRUE	T29_90D	T29	T29_D2R_N<3..0> 85 87 89
NO_TEST=TRUE	T29_90D	T29	T29_R2D_C_F_P<3..0> 85 87
NO_TEST=TRUE	T29_90D	T29	T29_R2D_C_F_N<3..0> 85 87
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_P<3..0> 85 86
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_N<3..0> 85 86
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_P<3..0> 87 88
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_N<3..0> 87 88
NO_TEST=TRUE	T29_90D	T29	DP_A_EXT_AUXCH_P 85 86
NO_TEST=TRUE	T29_90D	T29	DP_A_EXT_AUXCH_N 85 86
NO_TEST=TRUE	T29_90D	T29	DP_SDRVA_AUXCH_C_P 85
NO_TEST=TRUE	T29_90D	T29	DP_SDRVA_AUXCH_C_N 85
NO_TEST=TRUE	T29_90D	T29	DP_SDRVB_AUXCH_C_P 87
NO_TEST=TRUE	T29_90D	T29	DP_SDRVB_AUXCH_C_N 87
NO_TEST=TRUE	T29_90D	T29	DP_B_EXT_AUXCH_P 87 88
NO_TEST=TRUE	T29_90D	T29	DP_B_EXT_AUXCH_N 87 88
NO_TEST=TRUE	T29_90D	T29	T29DPA_D2R1_AUXCH_P 86
NO_TEST=TRUE	T29_90D	T29	T29DPA_D2R1_AUXCH_N 86
NO_TEST=TRUE	T29_90D	T29	T29DPB_D2R3_AUXCH_P 88
NO_TEST=TRUE	T29_90D	T29	T29DPB_D2R3_AUXCH_N 88
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_C_N<0> 85 86
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_C_P<0> 85 86
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_C_N<2> 85 86
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_C_P<2> 85 86
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_C_N<0> 87 88
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_C_P<0> 87 88
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_C_N<2> 87 88
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_C_P<2> 87 88
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_R2D_P<3..0> 89
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_R2D_N<3..0> 89
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_R2D_C_P<3..0> 18 89
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_R2D_C_N<3..0> 18 89
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_D2R_P<3..0> 18 89
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_D2R_N<3..0> 18 89
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_D2R_C_P<3..0> 89
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_D2R_C_N<3..0> 89
NO_TEST=TRUE	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_P 18 89
NO_TEST=TRUE	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_N 18 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_P<3..0> 84
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_N<3..0> 84
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_ML_P<3..0> 84 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_ML_N<3..0> 84 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_P<3..0> 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_N<3..0> 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_P 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_N 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_P<3..0> 79 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_N<3..0> 79 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_P 79 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_N 79 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_P<3..0> 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_N<3..0> 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_P 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_N 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_P<3..0> 79 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_N<3..0> 79 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_P 79 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_N 79 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_R_C_P 84
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_R_C_N 84
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_P 84 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_N 84 89
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_AUXCH_P 85
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_AUXCH_N 85
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_AUXCH_P 87
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_AUXCH_N 87
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_C_P<3..0> 85
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_C_N<3..0> 85
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_P<3..0> 85
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_N<3..0> 85
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_R_P<3..0> 85
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_R_N<3..0> 85
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_C_P<3..0> 87
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_C_N<3..0> 87
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_P<3..0> 87
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_N<3..0> 87
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_R_P<3..0> 87
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_R_N<3..0> 87
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29_A_RSVD_N 85
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29_A_RSVD_P 85
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29_B_RSVD_N 87
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29_B_RSVD_P 87

T29 NET PROPERTIES

ELECTRICAL CONSTRAINT SET	NET TYPE: PHYSICAL	NET TYPE: SPACING	
	T29_SPI_55S	T29_SPI	JTAG_T29_TDI 15 21 89
	T29_SPI_55S	T29_SPI	JTAG_T29_TMS 15 18 89
	T29_SPI_55S	T29_SPI	JTAG_T29_TCK 15 21 25 89
	T29_SPI_55S	T29_SPI	JTAG_T29_TDO 15 21 89
L43J	T29_SPI_55S	T29_SPI	T29_SPI_MOSI 89
L43H	T29_SPI_55S	T29_SPI	T29_SPI_MISO 89
L43G	T29_SPI_55S	T29_SPI	T29_SPI_CS_L 89
L44F	T29_SPI_55S	T29_SPI	T29_SPI_CLK 89
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29 80 89 99
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29_R 89 99
	T29_SMB_55S	T29_SMB	I2C_T29_SDA 49 89
	T29_SMB_55S	T29_SMB	I2C_T29_SCL 49 89
L42J	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB 80
L42G	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET 80
L42E	CLK_25M_55S	CLK_25M	ENET_CLK25M_XTALI_OSC 36 80
L42C	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29_CLK 80
L43K	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29 80 89 99
L42K	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29_R 89 99
L42H	T29_XTAL_100D	T29_XTAL	SYSCLK_CLK25M_X2 80
L42D	T29_XTAL_100D	T29_XTAL	SYSCLK_CLK25M_X2_R 80
L42F	T29_XTAL_100D	T29_XTAL	SYSCLK_CLK25M_X1 80
L43L	T29_55S	T29_COMP	T29_RSENSE 89
L43C	T29_55S	T29_COMP	T29_RBIAS 89
L43E		T29_COMP	T29_A_BIAS 79 83 85 86
L43D		T29_COMP	T29_B_BIAS 79 83 87 88
L42M		T29_COMP	DP_A_BIAS 79 85

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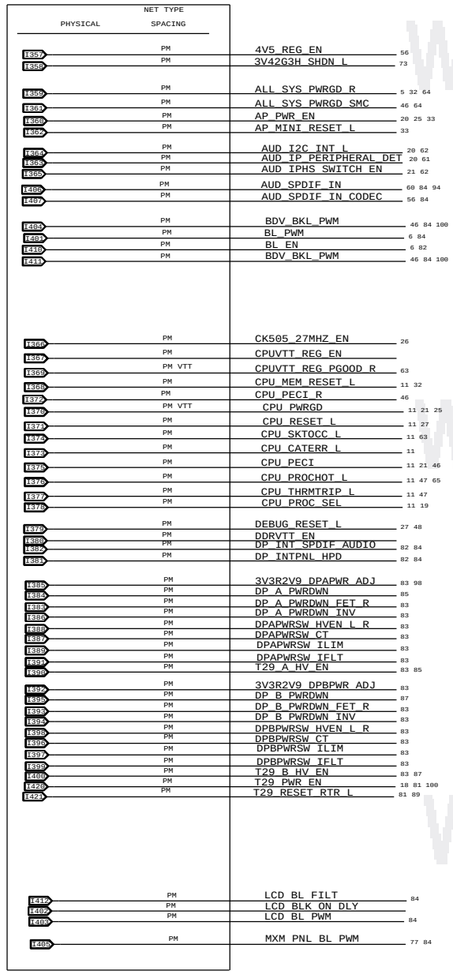
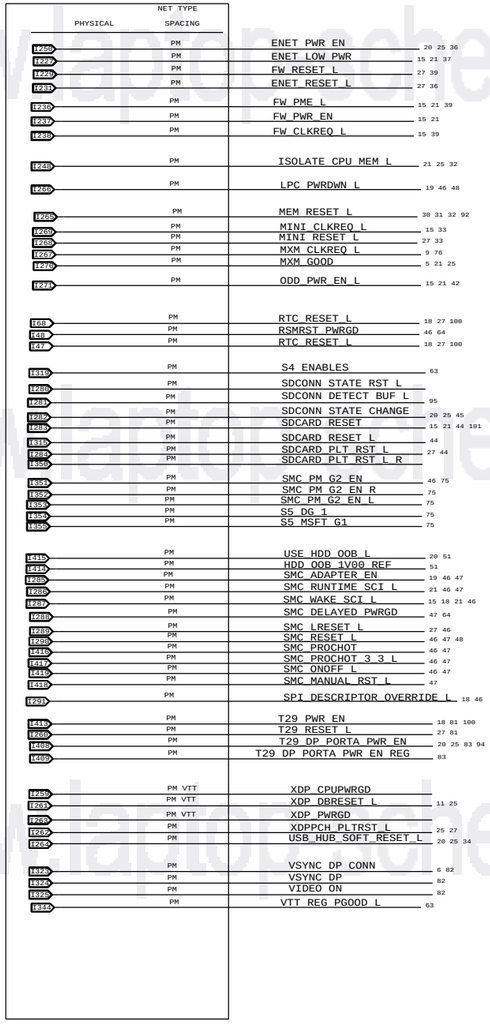
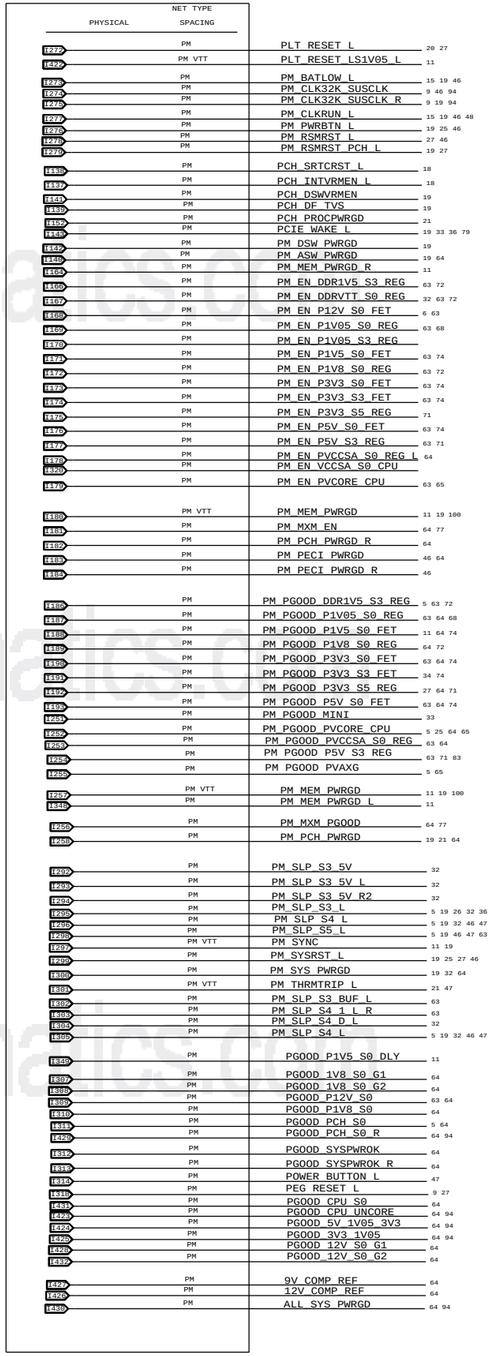
PM NET PROPERTIES
(PM, RESET, EN, PGOOD)

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PM	*	*	2 1 SPACING
PM VTT	PM VTT	*	2 1 SPACING
PM VTT	*	*	3 1 SPACING
PM VTT	GND	*	DEFAULT
PM	GND	*	DEFAULT







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FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT

J4700 USB CAMERA

98 6 IN PP5V_S3 FUNC_TEST_TRUE
MIN ALLOWED TPS=1
95 44 IN USB_CAMERA_L_P FUNC_TEST=TRUE
95 44 IN USB_CAMERA_L_N FUNC_TEST=TRUE

95 44 IN USB_BT_L_P FUNC_TEST_TRUE
95 44 IN USB_BT_L_N FUNC_TEST=TRUE

1 PP5V_S3_REG Testpoint near J4700
1 PP3V3_S3 TESTPOINT NEAR J4700
6 GROUND TESTPOINTS NEAR J4700

J4750 USB CARD READER

100 44 21 15 IN SDCARD_RESET FUNC_TEST=TRUE

1 PP3V3_S3 Testpoint near J4750
2 Ground Testpoints near J4750

J4780 IR BOARD

95 44 IN USB_IR_L_P FUNC_TEST_TRUE
95 44 IN USB_IR_L_N FUNC_TEST=TRUE
98 44 IN PP5V_S3_IR_FLT FUNC_TEST_TRUE

1 GROUND TESTPOINT NEAR J4780

J4520 SATA ODD (HIGH SPEED)

46 42 IN SMC_ODD_DETECT FUNC_TEST=TRUE

1 PP5V_S0 Testpoint near J4520
1 GROUND TESTPOINTS NEAR J4520

J5551 ODD TEMP SENSOR

97 52 IN SNS_ODD_P FUNC_TEST_TRUE
97 52 IN SNS_ODD_N FUNC_TEST_TRUE

J5600 ODD FAN

53 IN FAN_0_PWR_L FUNC_TEST_TRUE
53 IN FAN_TACH0_L FUNC_TEST_TRUE
98 53 IN PP12V_S0_FAN0_L FUNC_TEST_TRUE
53 IN FAN_0_GND FUNC_TEST=TRUE

J5700 CPU FAN

54 IN FAN_2_PWR_L FUNC_TEST_TRUE
54 IN FAN_TACH2_L FUNC_TEST=TRUE
98 54 IN PP12V_S0_FAN2_L FUNC_TEST=TRUE
54 IN FAN_2_GND FUNC_TEST=TRUE

97 52 IN SNS_AMB_P FUNC_TEST_TRUE
97 52 IN SNS_AMB_N FUNC_TEST=TRUE

1 GROUND TESTPOINT NEAR J5700

J5601 HD FAN

53 IN FAN_1_PWR_L FUNC_TEST=TRUE
53 IN FAN_TACH1_L FUNC_TEST=TRUE
98 53 IN PP12V_S0_FAN1_L FUNC_TEST=TRUE
53 IN FAN_1_GND FUNC_TEST_TRUE

J5400 HDD TEMP SENSOR

97 51 42 IN HDD_OOB_TEMP_FILT FUNC_TEST=TRUE

1 GROUND TESTPOINTS NEAR J5400

J5560 SKIN TEMP SENSOR

97 52 44 IN SNS_SKIN_LEFT_P FUNC_TEST_TRUE
97 52 44 IN SNS_SKIN_LEFT_N FUNC_TEST_TRUE

97 52 IN SNS_SKIN_RIGHT_P FUNC_TEST_TRUE
97 52 IN SNS_SKIN_RIGHT_N FUNC_TEST_TRUE

J6602 AUDIO RIGHT SPEAKER

94 IN AUD_SPKR_OUTLO2R_POUT FUNC_TEST_TRUE
94 IN AUD_SPKR_OUTLO2R_NOUT FUNC_TEST_TRUE
94 IN AUD_SPKR_OUTLO1R_POUT FUNC_TEST_TRUE
94 IN AUD_SPKR_OUTLO1R_NOUT FUNC_TEST_TRUE

J6603 AUDIO LEFT SPEAKER

94 IN AUD_SPKR_OUTLO2L_POUT FUNC_TEST_TRUE
94 IN AUD_SPKR_OUTLO2L_NOUT FUNC_TEST=TRUE
94 IN AUD_SPKR_OUTLO1L_POUT FUNC_TEST=TRUE
94 IN AUD_SPKR_OUTLO1L_NOUT FUNC_TEST=TRUE

J6600 AUDIO AUXILIARY CONNECTOR

2 TP'S
98 60 IN PP3V3_AUDIO_SPDIF_JACK FUNC_TEST=TRUE
MIN ALLOWED TPS=2

60 IN AUD_LI_DET_JACK FUNC_TEST_TRUE

60 IN AUD_LI_R_JACK FUNC_TEST=TRUE
60 IN AUD_LI_GND_JACK FUNC_TEST=TRUE
60 IN AUD_LI_L_JACK FUNC_TEST=TRUE

60 IN HS_MIC_HI_JACK FUNC_TEST_TRUE

60 IN AUD_HP_L_JACK FUNC_TEST=TRUE
60 IN AUD_HP_GND_JACK FUNC_TEST=TRUE
60 IN AUD_HP_R_JACK FUNC_TEST=TRUE
60 IN AUD_HP_TYPEDET_JACK FUNC_TEST=TRUE
60 IN AUD_IP_PERPH_JACK FUNC_TEST=TRUE
60 IN AUD_HP_TIPDET_JACK FUNC_TEST=TRUE

60 IN AUD_SPDIFIN_JACK FUNC_TEST=TRUE

4 GROUND TESTPOINTS NEAR J6600

GND 17 TP'S FUNC_TEST_TRUE
MIN ALLOWED TPS=17

98 6 IN PP3V3_S3 2 TP'S FUNC_TEST_TRUE
MIN ALLOWED TPS=2

98 6 IN PP5V_S0 FUNC_TEST_TRUE
MIN ALLOWED TPS=1

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