1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
A	0000891242	PRODUCTION RELEASED	2010-04-13

SCHEMATIC,MLB,"OLVIA"

LAST_MODIFIED=Tue Apr 13 17:17:57 2010

DRAWING
TITLE=K22
ABBREV=DRAWING
LAST_MODIFIED=Tue Apr 13 17:17:57 2010

DRAWING TITLE
SCHEMATIC,"OLVIA",MLB

Apple Inc.

DRAWING NUMBER 051-8337 | SIZE D
REVISION A.0.0
BRANCH
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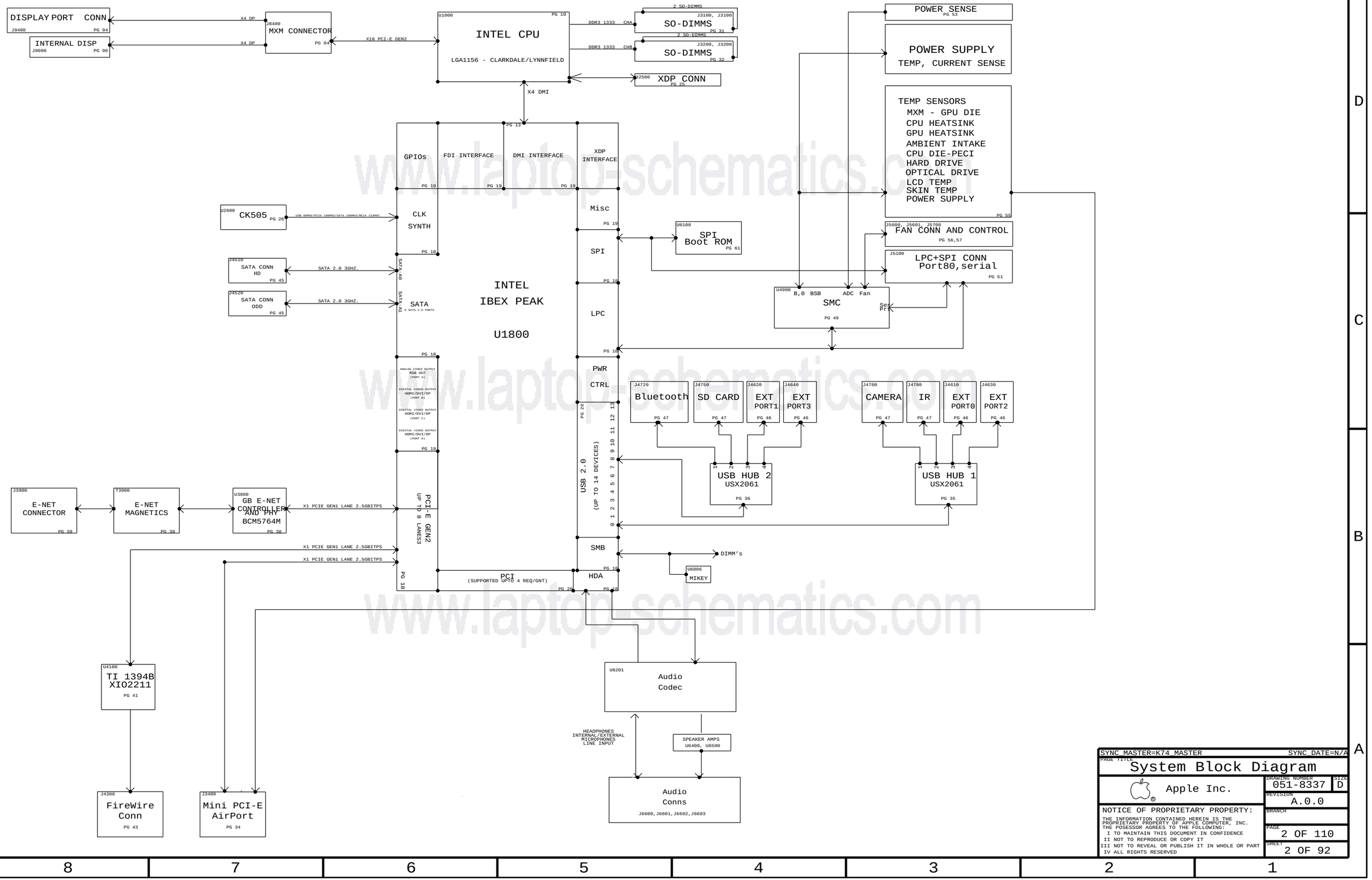
SHEET 1 OF 92



SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: System Block Diagram

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

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AC/DC POWER SUPPLY

12V_S5

TEMP SENSOR
CONTROL
DCM/FCM

SMBUS
PM_SLP_S3_OD
PP12V_S0_HDD
PPLED_PWR
PP12V_S0
LCD PANEL
HARD DRIVE
MXM
FANS
AUDIO

PP12V_G3H:

PM_SMC_G2_EN
PP12V_G3H
PP12V_S5

PP12V_S5:

PP5V_S3_REG
FET (10.3A)
PAGE 74
USB
CAMERA
IR
CARD READER
WM

P5VS0_EN

PP5V_S0
FET (6.9A)
PAGE 80
AUDIO
IBEX PEAK
OPTICAL
MXM
HDD

PP1V8_S0_REG
SW (1A)
PAGE 78
CPU PLL

PP12V_S0:

PPVCORE_CPU
.65-1.5V @ 90A
PAGE 71-72
CPU_CORE

PPVTT_S0
1.1V @ 30A
PAGE 76
CPU UNCORE

PP1V05_S0
1.05V @ 3A
PAGE 76
IBEX PEAK

PP3V42_G3H_REG
REG
PAGE 79
SMC

PP3V3_S5_AVREF_SMC
REG
PAGE 50
SMC VREF

12V S5 FET (7A)

CRITICAL
Q8040
FDS4465_G
SOI-HF

=PP12V_G3H_S5_FET
PP12V_S5_FET
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM

R8040
10K
5%
1/10W
MF-LF
402

C8040
0.47UF
10%
10V
X7R
805

R8041
10K
5%
1/10W
MF-LF
402

R8045
10K
5%
1/10W
MF-LF
402

P12V_S5_EN_D
P12V_S5_EN_G
P12V_S5_EN_R

Q8041
2N7002
SOT23-HF1

SMC_PM_G2_EN

R8042
100K
5%
1/16W
MF-LF
402

PP3V3_S5_REG
3.3V @ 6.2A
PAGE 76
BOOT ROM
IBEX PEAK

PP1V05_S5
1.05V @ 0.4A
PAGE 79
VCCME, PCH

P3V3S3_EN

PP3V3_S3
3.3V @ 2.8A
PAGE 80
ETHERNET
BT
AP

PP1V95_S3
1.0V @ 0.08A
PAGE 42
FW

P3V3S0_EN

PP3V3_S0
FET (2.8A)
PAGE 80
LCD PANEL
IBEX PEAK
AUDIO
MXM
DIRVT
FIREWIRE

PPDDR_S3_REG
13A (S3 & S0)
PAGE 75
MAIN MEMORY

PM_SLP_S3

PP1V5_S0
1.5V @ 4.9A
PAGE 78
CPU MEM
AUDIO
FIREWIRE

PP0V75_S0
0.75V @ 0.6A
PAGE 75
MEM_VTT

PP1V2_S3
1.2V @ 0.2A
PAGE 38
ENET

State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
Power Block Diagram

Apple Inc.

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
085-1107	PCBA,MLB,DEV,K74	DEVELOPMENT,DEV_GROUP
639-0698	PCBA,MLB,K74,2.93GHZ,CKD	K74,2P93GHZ_CKD_CPU,BASIC,CLARKDALE_73W
639-0707	PCBA,MLB,K74,3.06GHZ,CKD	K74,3P06GHZ_CKD_CPU,BASIC,CLARKDALE_73W
639-0808	PCBA,MLB,K74,3.20GHZ,CKD	K74,3P20GHZ_CKD_CPU,BASIC,CLARKDALE_73W
639-0695	PCBA,MLB,K74,3.46GHZ,CKD	K74,3P46GHZ_CKD_CPU,BASIC,CLARKDALE_73W
639-0991	PCBA,MLB,K74,3.60GHZ,CKD	K74,3P60GHZ_CKD_CPU,BASIC,CLARKDALE_73W
639-0694	PCBA,MLB,K74,2.53GHZ,LFD	K74,2P53GHZ_LFD_CPU,BASIC,LYNNFIELD_82W

BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE,XDP,MXM,XDP_CPU_BPM,PCH_VRM,BUF_CLK,HUB_USX2061,FW_TI_INT_VREG,BCM5764M,SD_USB,METAL_IO,PRODUCTION
DEV_GROUP	XDP_CONN,LPCPLUS,MOJOMUX,CPU_1V5_SENSE,VREFMRGN

CPU SOCKET & ILM SUB-BOMS

ALTERNATE SOCKET VENDORS MUST USE MATCHING ILM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0063	1	SOCKET,LGA1156,CPU-LF	U1000	CRITICAL	MOLEX_SOCKET
604-1161	1	ASSY,PURCHASED,ILM,MOLEX,K74	ILM	CRITICAL	MOLEX_SOCKET
511S0069	1	SOCKET,LGA1156,CPU-LF	U1000	CRITICAL	FOXCONN_SOCKET
604-1246	1	ASSY,PURCHASED,ILM,MOLEX,K74	ILM	CRITICAL	FOXCONN_SOCKET

BOM NUMBER	BOM NAME	BOM OPTIONS
607-6694	SUB ASSY,CPU SOCKET,K74,MOLEX	MOLEX_SOCKET
607-6693	SUB ASSY,CPU SOCKET,K74,FOXCONN	FOXCONN_SOCKET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
607-6694	1	MOLEX CPU SOCKET AND ILM	SKT_ILM	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
607-6693	607-6694		SKT_ILM	FOXCONN ALTERNATE

BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL
4	POWER
5	POWER
6	SIGNAL
7	GROUND
BOTTOM	SIGNAL

COMMON

RAW: 335S0663

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3828	1	IC,IBEX PEAK PRQ,DESKTOP,FCBGA,PCH,P42S	U1800	CRITICAL	
359S0157	1	IC,SLG2AP108,CLK GEN,CK505,QFN3	U2600	CRITICAL	BUF_CLK
341T0230	1	IC,EFI BOOTROM,K74/K75	U6100	CRITICAL	
338S0765	1	IC,XIO2211ZAY,1394B_PCIE,PHY/LINK	U4100	CRITICAL	
825-7122	1	MLB LABEL,48.0X4.8	X14	CRITICAL	
343S0493	1	IC,BCM5764M,ENET,8X8	U3900	CRITICAL	BCM5764M
343S0494	1	IC,BCM57765A,ENET&SD,8X8	U3900	CRITICAL	BCM57765
341T0269	1	ENET 1MBIT FLASH,CII,K74/K75	U3990	CRITICAL	BCM5764M
341T0246	1	ENET 1MBIT FLASH,CIV,K74/K75	U3990	CRITICAL	BCM57765

CPUS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3837	1	CKD,Q3GR,QS,2.93,73W,1333,C2,4M,LGA	CPU	CRITICAL	2P93GHZ_CKD_CPU
337S3912	1	CKD,SLBTD,PRQ,3.06,73W,1333,K0,4M,LGA	CPU	CRITICAL	3P06GHZ_CKD_CPU
337S3911	1	CKD,SLBUD,PRQ,3.20,73W,1333,K0,4M,LGA	CPU	CRITICAL	3P20GHZ_CKD_CPU
337S3900	1	CKD,SLBLT,PRQ,3.46,73W,1333,C2,4M,LGA	CPU	CRITICAL	3P46GHZ_CKD_CPU
337S3910	1	CKD,SLBTM,PRQ,3.60,73W,1333,K0,4M,LGA	CPU	CRITICAL	3P60GHZ_CKD_CPU
337S3862	1	LFD,Q3C6,QS,2.53,82W,1333,B1,8M,LGA	CPU	CRITICAL	2P53GHZ_LFD_CPU

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
337S3898	337S3912	3P06GHZ_CKD_CPU	CPU	C2,PRQ,3.06 GHZ CKD

K74 PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-8337	1	SCH,MLB,K74	SCH1		
820-2784	1	PCBF,MLB,K74	MLB1		
341T0231	1	IC,SMC,K74	U4900	CRITICAL	K74

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0339	197S0179		Y4190	FIREWIRE OSCILLATOR
128S0298	128S0293		C1670,C7260,C7444	

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: BOM Configuration

Apple Inc.

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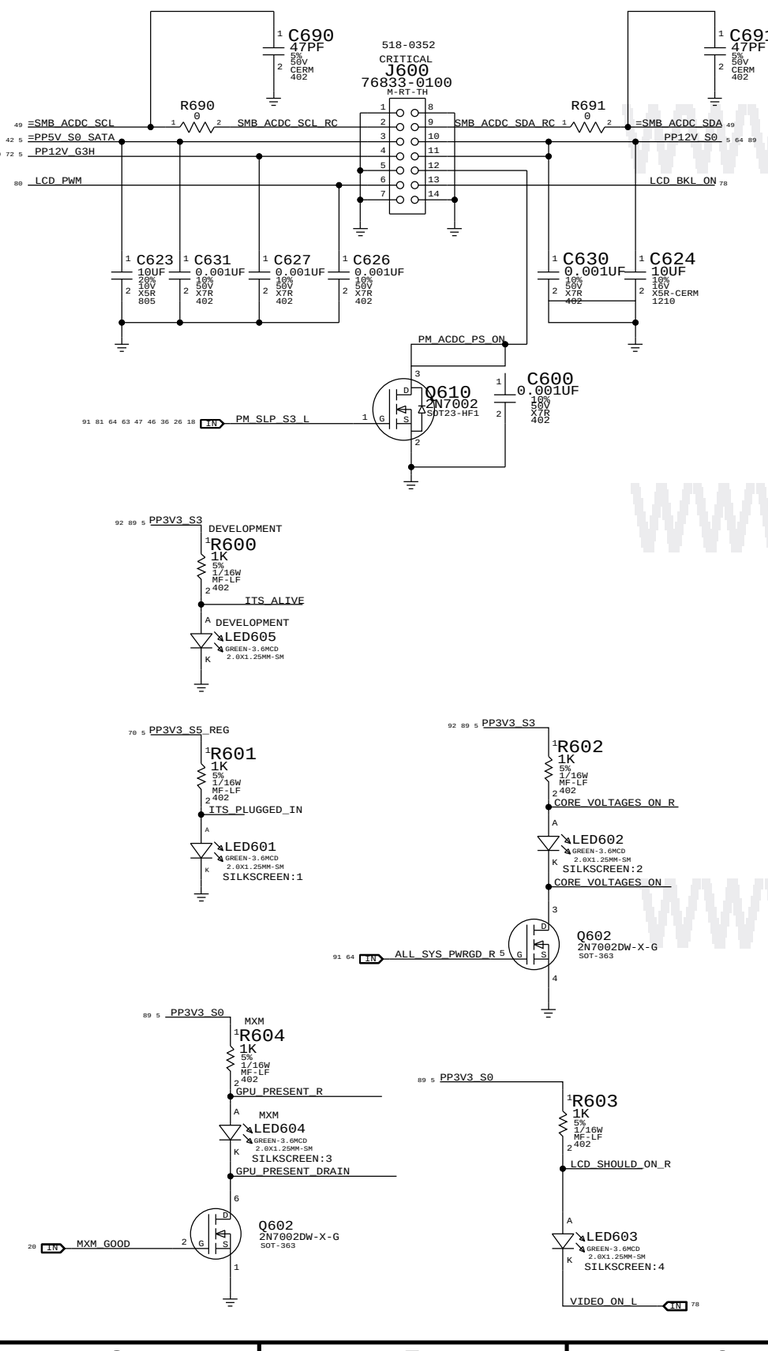
EMC: C600,C626,C627,C628,C629,C630,C631
PLACE AT J600.



"S0" RAILS

ONLY ON IN RUN

PPVTT_S0_DDR
MAKE_BASE=TRUE
VOLTAGE=0.75V
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
- PPVTT_S0_DDR_FET (26)
- =PP0V75_S0_MEM_VTT_B (31)
- =PP0V75_S0_MEM_VTT_A (30)

PPVCORE_S0_CPU
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
- PPVCORE_S0_CPU_REG (65 66 67)
- =PPVCORE_S0_CPU (12 15)

PPVTT_S0
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
- PPVTT_S0_CPU_REG (68)
- =PPVTT_S0_PCH_VCC_DMI (21 23)
- =PPVTT_S0_XDP (24)
- =PPVTT_S0_PCH_VCCP_CPU (21 23)
- =PPVTT_S0_CPU (10 12 15 47 65)

PP1V5_CPU_MEM
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
- =PP1V5_CPU_MEM (10 12 15 29)

PP1V5_S0
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
- PP1V5_S0_FET (50 73)
- =PP1V5_S0_AUD_DIG (56)
- =PP1V5_FWRS0_FWXIO (39)
- =PP1V5_S0_CK505 (25)
- =PP1V5_S0_MINI (33)

PP1V8_S0
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
- PP1V8_S0_REG (71)
- =PP3V3R1V8_S0_PCH_VCCPNAND (21 23)
- =PP1V8R1V5_S0_PCH_VCCVRM (23)
- =PP1V8_S0_CPU_PLL (12 15 64)

PP3V3_S0
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
- PP3V3_S0_FET (73)
- =PP3V3_S0_PCH (17 20 23 69)
- =PP3V3_S0_FAN (53 54)
- =PP3V3_S0_PCH_VCCADAC (16)
- =PPSPD_S0_MEM_A (30 47)
- =PPSPD_S0_MEM_B (31)
- =PP3V3_S0_VRD (65)
- =PP3V3_S0_AUDIO (56 58 59 60 61 62)
- =PP3V3R1V5_S0_PCH_VCCSUSHDA (21 23)
- =PP3V3_S0_SMBUS (49)
- =PP3V3_S0_SMC_LS (47 51)
- =PP3V3_S0_SMBUS_SMC_0_S0 (49)
- =PP3V3_S0_SMBUS_SMC_B_S0 (49)
- =PP3V3_S0_SMBUS_SMC_MGMT (49)
- =PP3V3_S0_DPCONN (81)
- =PP3V3_S0_TSENS (52)
- =PP3V3_S0_MXM (64 74 75)
- =PP3V3_S0_ODD (42)
- =PP3V3_S0_SATALED (17 42)
- =PP3V3_S0_SMC (47 50)
- =PP3V3_S0_PWRCTL (63 64 73)
- =PP3V3_S0_PCH_VCC3_3_CORE (21 23)
- =PP3V3_FW_FWPHY (39 40 41)
- =PP3V3_FWRS0_FWXIO (39)
- =PP3V3_S0_DP (78 79 80)
- =PP3V3_S0_PCH_VCC3_3_PCI (21 23)
- =PP3V3_S0_CK505 (25)
- =PP3V3_S0_PCH_GPIO (19)
- =PP3V3_S0_PCH_STRAPS (14)
- =PP3V3_S0_PCH_VCC3_3_SATA (21 23)
- =PP3V3_S0_RSTBUF (27)
- =PP3V3_S0_ENETPHY (37)
- =PP3V3_S0_PCH_PM (27)
- =PP3V3_S0_SMBUS_SMC_BSA (49)
- =PP3V3_SM_PCH_VCC_ME (21 23)
- =PP3V3_S0_SDCARD (45)
- =PP3V3_S0_CPU_VTT_VREG (68)

PP5V_S0
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
- PP5V_S0_FET (73)
- =PP5V_S0_AUDIO (56)
- =PP5V_S0_SATA (5 42)
- =PP5V_S0_MXM (74)
- =PP5V_S0_VRD (65)
- =PP5V_S0_ISENSE (50)
- =PP5V_S0_P1V8_VREG (71)
- =PP5V_S0_PCH (23)
- =PP5V_S0_CPU_VTT_VREG (68)
- =PP5V_S0_LPCPLUS (48)
- =PP5V_S0_PCH_CORE_VREG (69)
- =PP5V_S0_DP_AUX_MUX (80)

PP1V05_S0
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
- PP1V05_S0_REG (69)
- =PP1V05_S0_PCH_VCCADPLL (16)
- =PP1V05_S0_PCH_VCCIO_DMI (21 23)
- =PP1V05_S0_PCH_VCCIO_SATA (17 21 23)
- =PP1V05_S0_PCH_VCCIO_PCIE (17 18 21 23)
- =PP1V05_S0_PCH_VCC_CORE (21 23)
- =PP1V05_S0_PCH_VCCIO_USB (21 23)
- =PP1V05_S0_CK505 (25)
- =PP1V05_SM_PCH_VCC_ME (21 23)

PP1V05_SM_PCH_LAN
MAKE_BASE=TRUE
VOLTAGE=1.05V
- =PP1V05_SM_PCH_VCC_LAN (21 23)

UNUSED, GROUNDED ON CSA 24

PP0V75_S0
MAKE_BASE=TRUE
VOLTAGE=0.75V
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
- PPVTT_S0_DDR_LDO (71)
- =PP0V75_S0_MEM_VTT_S0FET (26)

PP12V_S0
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
- =PP12V_S0_FAN (53 54)
- =PP12V_S0_AUDIO_SPKRAMP (58 59)
- =PP12V_S0_VRD (65)
- =PPV_S0_MXM_PWR (50)
- =PP12V_S0_LCD (78)
- =PP12V_S0_PCH_CORE_VREG (69)
- =PP12V_S0_CPU_VTT_VREG (68)
- =PP12V_S0_PWRCTL (64)
- =PP12V_S0_SENSE (51)
- =PP12V_S0_FW (41)

"S3" RAILS

ON IN RUN AND SLEEP

PP1V5_S3
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
- PP1V5_S3_REG (71)
- =PP1V5_S3_MEMRESET (26)
- =PPDDR_S3_S0FET (73)
- =PP1V5_S3_MEM_A (28 29 30)
- =PP1V5_S3_MEM_B (28 29 31)

PP3V3_S3
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
- PP3V3_S3_FET (73)
- =PP3V3_S3_BT (44)
- =PP3V3_S3_SMBUS_SMC_A_S3 (49)
- =PP3V3_S3_MINI (33)
- =PP3V3_S3_PWRCTL (64 73)
- =PP3V3_S3_MEMRESET (26)
- =PP3V3_S3_USB_HUB (34 35)
- =PP3V3_S3_USB_RESET (34)
- =PP3V3_S3_SDCARD (44 45)
- =PP3V3_S3_VREFMRGN (28)
- =PP3V3_S3_ENETFET (36)

PP5V_S3
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
- PP5V_S3_REG (70 92)
- =PP5V_S3_USB (43)
- =PP5V_S3_S0FET (73)
- =PP5V_S3_CAMERA (44)
- =PP5V_S3_IR (44)
- =PP5V_S3_PWRCTL (63)
- =PP5V_S3_MEMRESET (26)
- =PP5V_S3_DDR_VREG (71)

ENET RAILS

PP3V3_ENET
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
- PP3V3_ENET_FET (36)
- =PP3V3_ENET_PHY (36 37 45)

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER AND IN S5

PP3V3_S5
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
- PP3V3_S5_REG (5 70)
- =PP3V3_S5_PCH (17 18 23)
- =PP3V3_S5_PCH_GPIO (19)
- =PP3V3_S5_ROM (48 55)
- =PP3V3_S5_PCH_VCCSUS3_3_USB (21 23)
- =PP3V3_S5_PWRCTL (10 63 64)
- =PP3V3_S5_S3FET (73)
- =PP3V3_S5_S0FET (73)
- =PP3V3_S5_PCH_STRAPS (14)
- =PP3V3_S5_CPURESET (10)
- =PP3V3_S5_XDP (24)
- =PP3V3_S5_LPCPLUS (48)

PP5V_S5
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
- PP5V_S5_LDO (70)
- =PP5V_S5_PCH (23)

PP12V_S5
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
- PP12V_S5_FET (3)
- =PP12V_S5_DDR_VREG (71)
- =PP12V_S5_P3V3S5_VREG (70)
- =PP12V_S5_P5VS3_VREG (70)
- =PP12V_S5_PWRCTL (64 73)

"G3H" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER AND IN G3HOT PER SMC

G3H: ALIASES

PP3V42_G3H
MAKE_BASE=TRUE
VOLTAGE=3.42V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
- PP3V42_G3H_REG (72)
- =PP3V3_S5_RTC_D (27)
- =PP3V3_G3H_SMC (46 47)
- =PP3V3_G3H_SMCUSBMUX (43)
- =PPVIN_S5_SMCVREF (47)
- =PP3V3_G3H_LPCPLUS (48)

PP12V_G3H
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
- =PP12V_G3H_S5_FET (3)

GND RAILS

GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V
NET_SPACING_TYPE=GND
MAKE_BASE=TRUE
MAX_NECK_LENGTH=4.1 MM
- =PPVAXG_S0_CPU (12)

SYNC_MASTER=K74_MASTER
SYNC_DATE=N/A

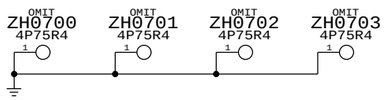
PAGE TITLE
Power Conn / Alias

Apple Inc.

DRAWING NUMBER 051-8337
SIZE D
REVISION A.0.0
BRANCH
PAGE 6 OF 110
SHEET 5 OF 92

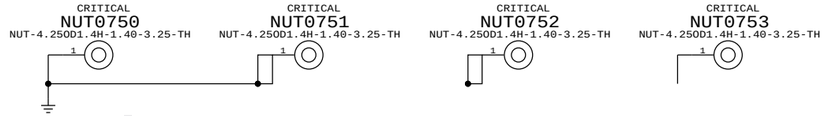
CPU Heatsink

4mm Plated Holes (998-0850)



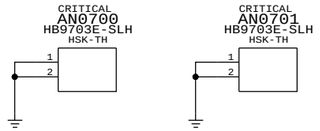
DIMM CONNECTOR NUTS

Nuts (805-9582)



PCH HEATSINK

MOUNTING ANCHORS (511-0057)

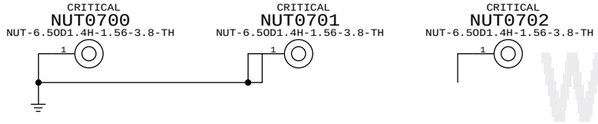


Rear Cover

Standoffs (860-1255)

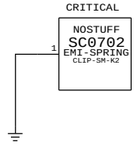
Backer Plate

Nuts (835-0269)



For EMC

EMC Spring (870-1577); Near DIMMs



SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: Holes

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 7 OF 110

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UNUSED CPU SIGNALS

TP_CPU_RSVD<41..29>	=	NC_CPU_RSVD<41..29>
TP_CPU_RSVD<26..1>	=	NC_CPU_RSVD<26..1>
TP_CPU_FC_AE38	=	NC_CPU_FC_AE38
TP_CPU_FC_AG40	=	NC_CPU_FC_AG40

MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED PCI ALIASES

TP_PCI_AD<31..0>	=	NC_PCI_AD<31..0>
TP_PCI_C_BE_L<3..0>	=	NC_PCI_C_BE_L<3..0>
TP_PCI_PAR	=	NC_PCI_PAR
TP_PCI_RESET_L	=	NC_PCI_RESET_L
TP_PCIE_CLK100M_XDPP	=	NC_PCIE_CLK100M_XDPP
TP_PCIE_CLK100M_XDPN	=	NC_PCIE_CLK100M_XDPN
TP_DMI_CLK100M_LAP	=	NC_DMI_CLK100M_LAP
TP_DMI_CLK100M_LAN	=	NC_DMI_CLK100M_LAN
TP_LPC_DREQ1_L	=	NC_LPC_DREQ1_L
TP_LPC_DREQ0_L	=	NC_LPC_DREQ0_L

MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED NAND ALIASES

TP_NV_CE_L<3..0>	=	NC_NV_CE_L<3..0>
TP_NV_DQS<1..0>	=	NC_NV_DQS<1..0>
TP_NV_DQ<15..0>	=	NC_NV_DQ<15..0>
TP_NV_RCOMP	=	NC_NV_RCOMP
TP_NV_RB_L	=	NC_NV_RB_L
TP_NV_WR_RE_L<1..0>	=	NC_NV_WR_RE_L<1..0>
TP_NV_WE_CK_L<1..0>	=	NC_NV_WE_CK_L<1..0>
TP_NV_ALE	=	NC_NV_ALE
TP_NV_CLE	=	NC_NV_CLE

MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED MEM ALIASES

TP_MEM_A_CS_L<7..4>	=	NC_MEM_A_CS_L<7..4>
TP_MEM_A_DQ_CB<7..0>	=	NC_MEM_A_DQ_CB<7..0>
TP_MEM_A_DQS_N<8>	=	NC_MEM_A_DQSN<8>
TP_MEM_A_DQS_P<8>	=	NC_MEM_A_DQSP<8>
TP_MEM_B_CS_L<7..4>	=	NC_MEM_B_CS_L<7..4>
TP_MEM_B_DQ_CB<7..0>	=	NC_MEM_B_DQ_CB<7..0>
TP_MEM_B_DQS_N<8>	=	NC_MEM_B_DQSN<8>
TP_MEM_B_DQS_P<8>	=	NC_MEM_B_DQSP<8>

MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED MISC ALIASES

TP_HDA_SDIN1	=	NC_HDA_SDIN1
TP_HDA_SDIN2	=	NC_HDA_SDIN2
TP_HDA_SDIN3	=	NC_HDA_SDIN3
TP_JTAG_XDP_TRST_L	=	NC_JTAG_XDP_TRST_L
TP_PCH_PWM0	=	NC_PCH_PWM0
TP_PCH_PWM1	=	NC_PCH_PWM1
TP_PCH_PWM2	=	NC_PCH_PWM2
TP_PCH_PWM3	=	NC_PCH_PWM3
TP_PCH_SST	=	NC_PCH_SST
SNS_CPU_THERMD_N	=	NC_SNS_CPU_THERMDN
SNS_CPU_THERMD_P	=	NC_SNS_CPU_THERMDP

MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED PCIE ALIASES

TP_PCIE_T28_D2R_N<3..0>	=	NC_PCIE_T28_D2RN<3..0>
TP_PCIE_T28_D2R_P<3..0>	=	NC_PCIE_T28_D2RP<3..0>
TP_PCIE_T28_R2D_C_N<3..0>	=	NC_PCIE_T28_R2D_CN<3..0>
TP_PCIE_T28_R2D_C_P<3..0>	=	NC_PCIE_T28_R2D_CP<3..0>
TP_PCIE_CLK100M_T28_N	=	NC_PCIE_CLK100M_T28N
TP_PCIE_CLK100M_T28_P	=	NC_PCIE_CLK100M_T28P
PCIE_EXCARD_D2R_P	=	NC_PCIE_EXCARD_D2RP
PCIE_EXCARD_D2R_N	=	NC_PCIE_EXCARD_D2RN
PCIE_EXCARD_R2D_C_P	=	NC_PCIE_EXCARD_R2D_CP
PCIE_EXCARD_R2D_C_N	=	NC_PCIE_EXCARD_R2D_CN
PCIE_CLK100M_EXCARD_P	=	NC_PCIE_CLK100M_EXCARDP
PCIE_CLK100M_EXCARD_N	=	NC_PCIE_CLK100M_EXCARDN
TP_PCIE_CLK100M_PE5P	=	NC_PCIE_CLK100M_PE5P
TP_PCIE_CLK100M_PE5N	=	NC_PCIE_CLK100M_PE5N
DMI_MIDBUS_CLK100M_P	=	NC_DMI_MIDBUS_CLK100MP
DMI_MIDBUS_CLK100M_N	=	NC_DMI_MIDBUS_CLK100MN

MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED USB ALIASES

TP_USB_1N	=	NC_USB_1N
TP_USB_1P	=	NC_USB_1P
TP_USB_2N	=	NC_USB_2N
TP_USB_2P	=	NC_USB_2P
TP_USB_3N	=	NC_USB_3N
TP_USB_3P	=	NC_USB_3P
TP_USB_4N	=	NC_USB_4N
TP_USB_4P	=	NC_USB_4P
TP_USB_5N	=	NC_USB_5N
TP_USB_5P	=	NC_USB_5P
TP_USB_6N	=	NC_USB_6N
TP_USB_6P	=	NC_USB_6P
TP_USB_7N	=	NC_USB_7N
TP_USB_7P	=	NC_USB_7P
TP_USB_9N	=	NC_USB_9N
TP_USB_9P	=	NC_USB_9P
TP_USB_10N	=	NC_USB_10N
TP_USB_10P	=	NC_USB_10P
TP_USB_11N	=	NC_USB_11N
TP_USB_11P	=	NC_USB_11P
TP_USB_12N	=	NC_USB_12N
TP_USB_12P	=	NC_USB_12P
TP_USB_13N	=	NC_USB_13N
TP_USB_13P	=	NC_USB_13P

MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED DISPLAY ALIASES

TP_CRT_IG_DDC_CLK	=	NC_CRT_IG_DDC_CLK
TP_CRT_IG_DDC_DATA	=	NC_CRT_IG_DDC_DATA
TP_CRT_IG_RED	=	NC_CRT_IG_RED
TP_CRT_IG_GREEN	=	NC_CRT_IG_GREEN
TP_CRT_IG_BLUE	=	NC_CRT_IG_BLUE
TP_CRT_IG_HSYNC	=	NC_CRT_IG_HSYNC
TP_CRT_IG_VSYNC	=	NC_CRT_IG_VSYNC
TP_DP_IG_B_MLN<3..0>	=	NC_DP_IG_B_MLN<3..0>
TP_DP_IG_B_MLP<3..0>	=	NC_DP_IG_B_MLP<3..0>
TP_DP_IG_B_AUX_N	=	NC_DP_IG_B_AUXN
TP_DP_IG_B_AUX_P	=	NC_DP_IG_B_AUXP
TP_DP_IG_B_HPD	=	NC_DP_IG_B_HPD
TP_DP_IG_B_DDC_CLK	=	NC_DP_IG_B_CTRL_CLK
TP_DP_IG_B_DDC_DATA	=	NC_DP_IG_B_CTRL_DATA
TP_DP_IG_C_MLN<3..0>	=	NC_DP_IG_C_MLN<3..0>
TP_DP_IG_C_MLP<3..0>	=	NC_DP_IG_C_MLP<3..0>
TP_DP_IG_C_AUX_N	=	NC_DP_IG_C_AUXN
TP_DP_IG_C_AUX_P	=	NC_DP_IG_C_AUXP
TP_DP_IG_C_HPD	=	NC_DP_IG_C_HPD
TP_DP_IG_C_CTRL_CLK	=	NC_DP_IG_C_CTRL_CLK
TP_DP_IG_C_CTRL_DATA	=	NC_DP_IG_C_CTRL_DATA
TP_DP_IG_D_MLN<3..0>	=	NC_DP_IG_D_MLN<3..0>
TP_DP_IG_D_MLP<3..0>	=	NC_DP_IG_D_MLP<3..0>
TP_DP_IG_D_AUXN	=	NC_DP_IG_D_AUXN
TP_DP_IG_D_AUXP	=	NC_DP_IG_D_AUXP
TP_DP_IG_D_HPD	=	NC_DP_IG_D_HPD
TP_DP_IG_D_CTRL_CLK	=	NC_DP_IG_D_CTRL_CLK
TP_DP_IG_D_CTRL_DATA	=	NC_DP_IG_D_CTRL_DATA
TP_GFX_VID<0..6>	=	NC_GFX_VID<0..6>
TP_GFX_VSENSE_N	=	NC_GFX_VSENSEN
TP_GFX_VSENSE_P	=	NC_GFX_VSENSEP
TP_SDVO_TVCLKINN	=	NC_SDVO_TVCLKINN
TP_SDVO_TVCLKINP	=	NC_SDVO_TVCLKINP
TP_SDVO_STALLN	=	NC_SDVO_STALLN
TP_SDVO_STALLP	=	NC_SDVO_STALLP
TP_SDVO_INTN	=	NC_SDVO_INTN
TP_SDVO_INTP	=	NC_SDVO_INTP

MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED FDI ALIASES

TP_CPU_FDI_TX_N<7..0>	=	NC_CPU_FDI_TXN<7..0>
TP_CPU_FDI_TX_P<7..0>	=	NC_CPU_FDI_TXP<7..0>
TP_PCH_FDI_RX_N<7..0>	=	NC_PCH_FDI_RXN<7..0>
TP_PCH_FDI_RX_P<7..0>	=	NC_PCH_FDI_RXP<7..0>
TP_CPU_FDI_FSYNC<1..0>	=	NC_CPU_FDI_FSYNC<1..0>
TP_PCH_FDI_FSYNC<1..0>	=	NC_PCH_FDI_FSYNC<1..0>
TP_CPU_FDI_LSYNC<1..0>	=	NC_CPU_FDI_LSYNC<1..0>
TP_PCH_FDI_LSYNC<1..0>	=	NC_PCH_FDI_LSYNC<1..0>
TP_CPU_FDI_INT	=	NC_CPU_FDI_INT
TP_PCH_FDI_INT	=	NC_PCH_FDI_INT

MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED SATA ALIASES

TP_SATA_D_D2RN	=	NC_SATA_D_D2RN
TP_SATA_D_D2RP	=	NC_SATA_D_D2RP
TP_SATA_D_R2D_CN	=	NC_SATA_D_R2D_CN
TP_SATA_D_R2D_CP	=	NC_SATA_D_R2D_CP
TP_SATA_E_D2RN	=	NC_SATA_E_D2RN
TP_SATA_E_D2RP	=	NC_SATA_E_D2RP
TP_SATA_E_R2D_CN	=	NC_SATA_E_R2D_CN
TP_SATA_E_R2D_CP	=	NC_SATA_E_R2D_CP
TP_SATA_F_D2RN	=	NC_SATA_F_D2RN
TP_SATA_F_D2RP	=	NC_SATA_F_D2RP
TP_SATA_F_R2D_CN	=	NC_SATA_F_R2D_CN
TP_SATA_F_R2D_CP	=	NC_SATA_F_R2D_CP
TP_SATA_SSD_D2R_N	=	NC_SATA_SSD_D2RN
TP_SATA_SSD_D2R_P	=	NC_SATA_SSD_D2RP
TP_SATA_SSD_R2D_C_N	=	NC_SATA_SSD_R2D_CN
TP_SATA_SSD_R2D_C_P	=	NC_SATA_SSD_R2D_CP

MAKE_BASE=TRUE NO_TEST=TRUE

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: UNUSED SIGNAL ALIAS

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

BRANCH:

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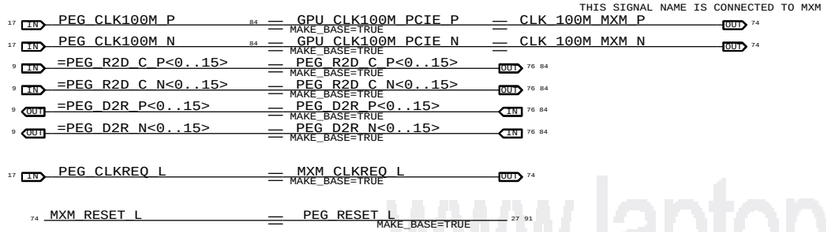
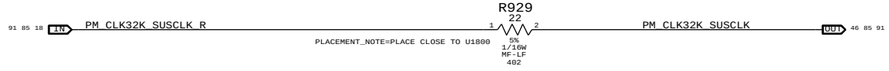
PEG Slot Support





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PAGE TITLE: Signal Aliases

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 9 OF 110

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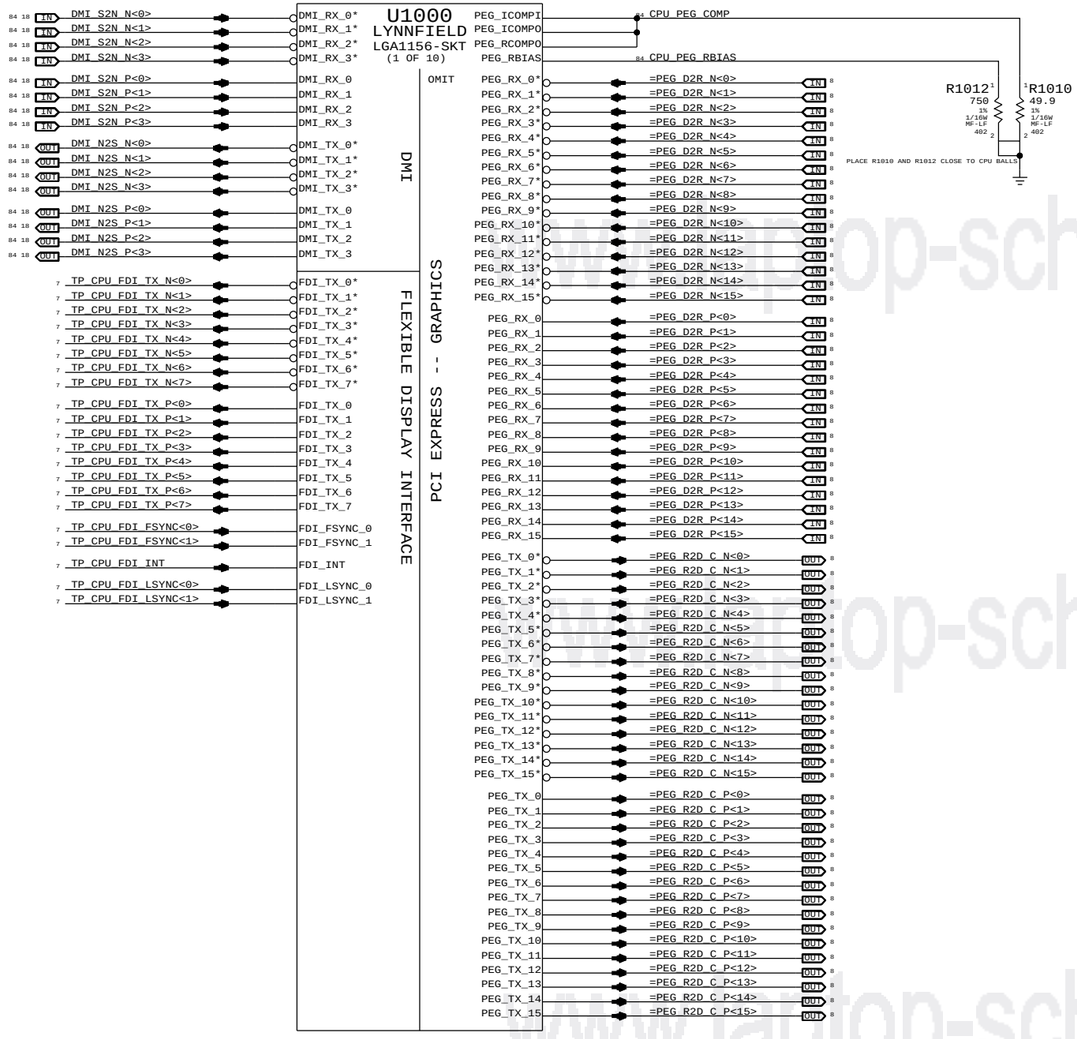
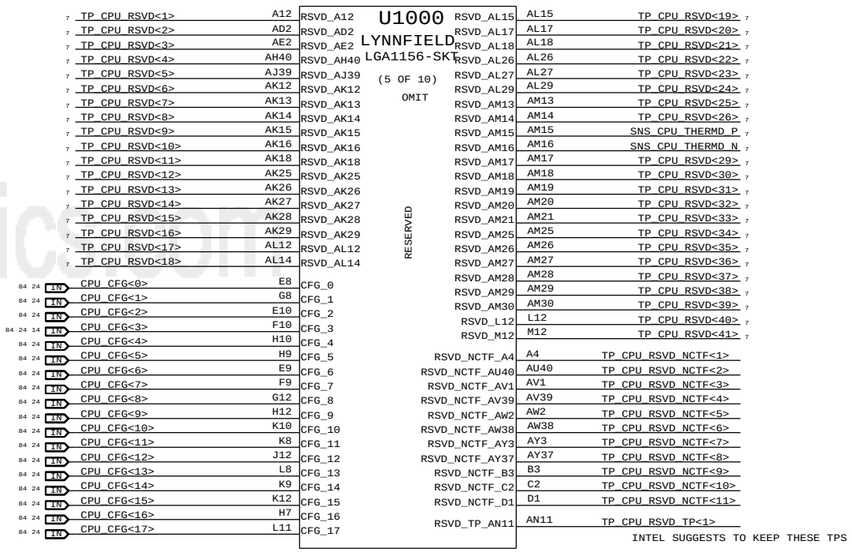




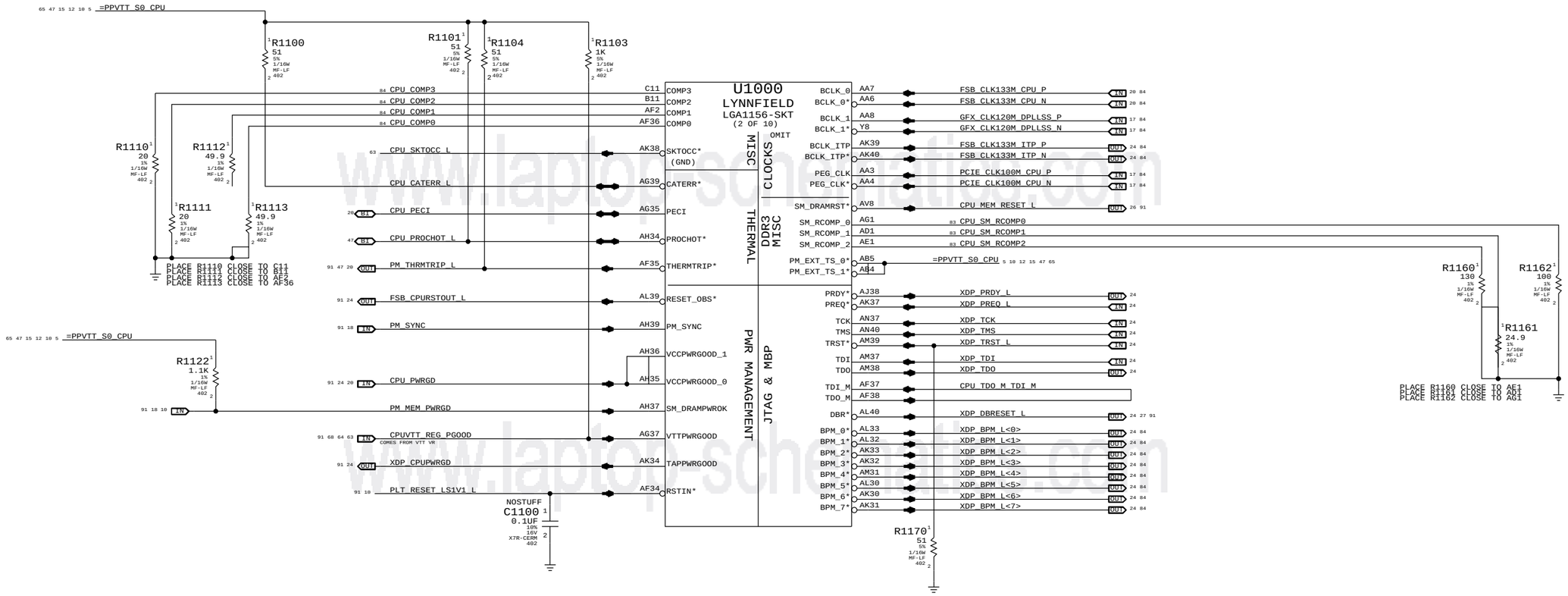
FOR LYNNFIELD PROCESSOR
CFG [1:0] :PCIE CONFIGURATION SELECT 11 = 1 X16 PCI EXPRESS 10 = 2 X8 PCI EXPRESS
FOR CLARKDALE PROCESSOR
CFG3 :PCIE LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED
CFG4 :NOT USED ON DESKTOP

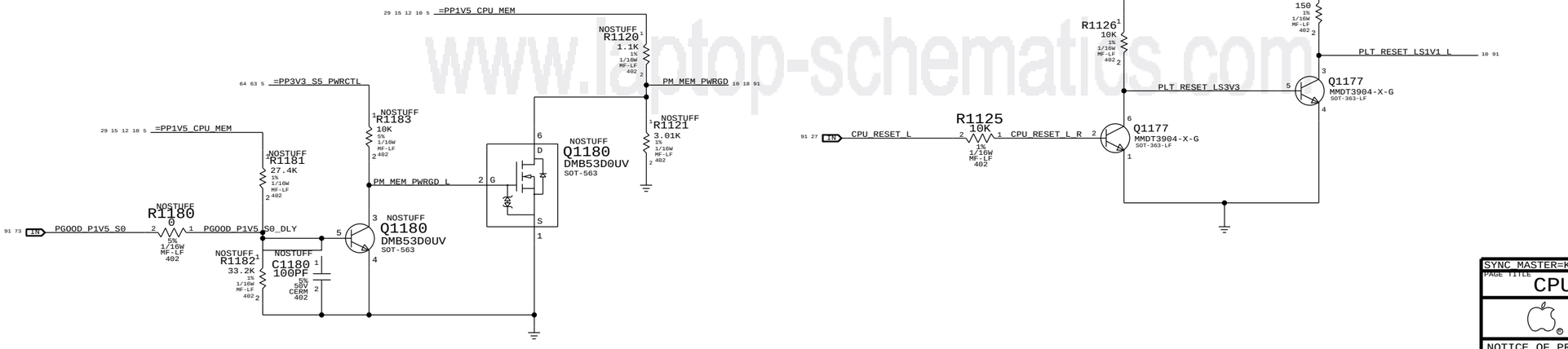
SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: CPU DMI/PEG/FDI/RSVD

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 10 OF 110
SHEET: 9 OF 92





SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
CPU CLOCK/MISC/JTAG

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D
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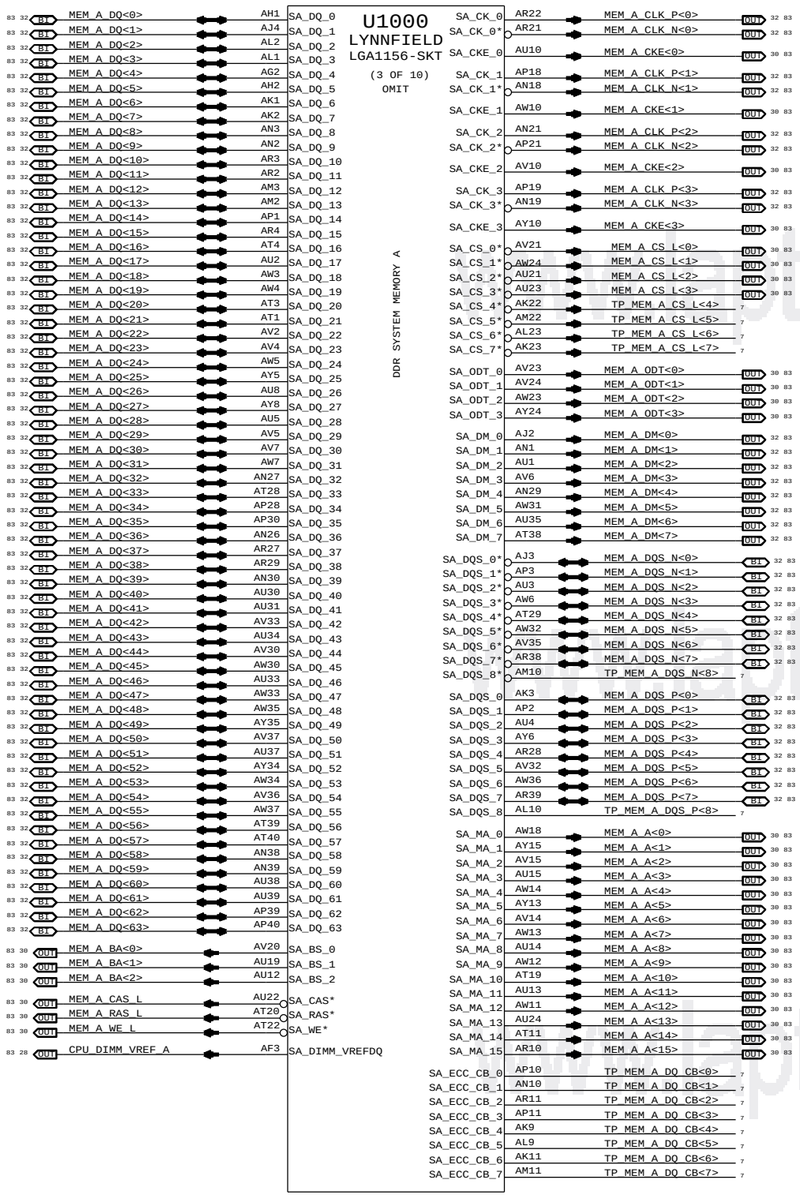
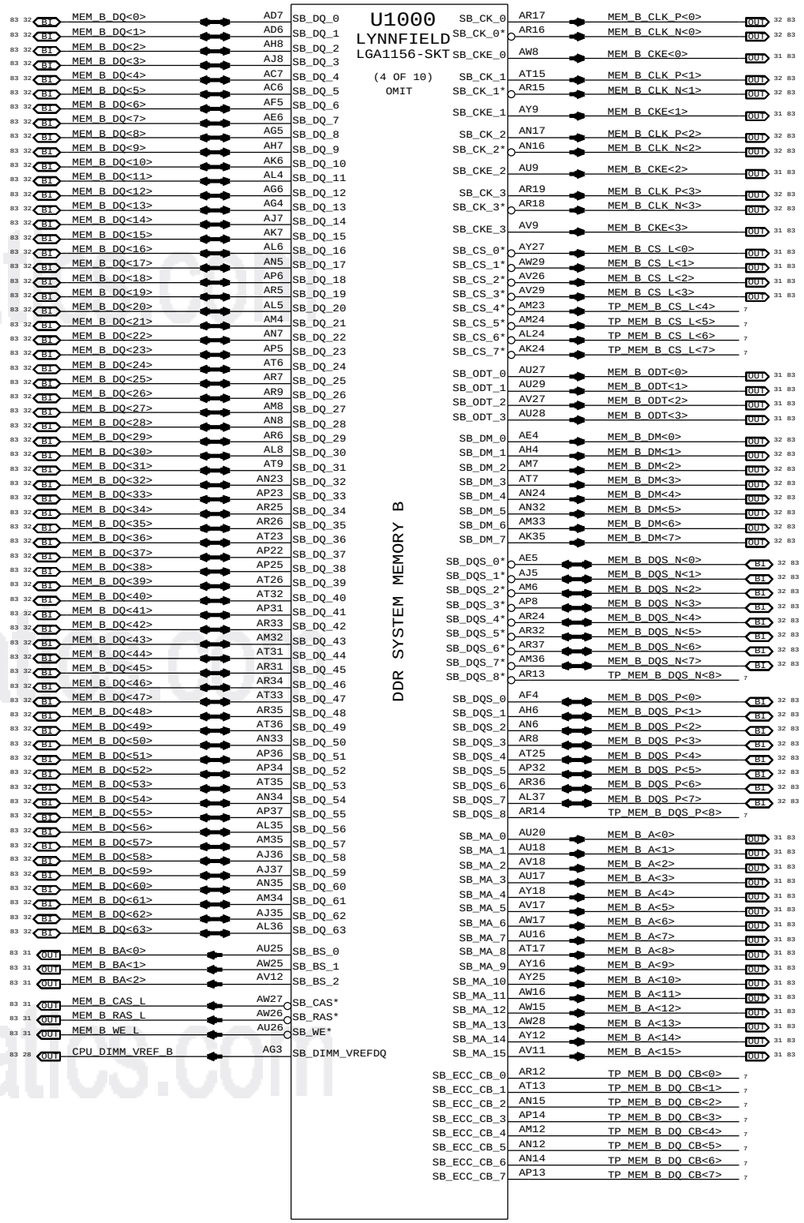
SHEET 10 OF 92





SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
CPU DDR3 INTERFACES

Apple Inc.

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REVISION A.0.0
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=PPVCORE_S0_CPU 5 12 15

U1000
LYNNFIELD
LGA1156-SKT
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OMIT

VCC

J21	VCC_100	
J22	VCC_101	
J24	VCC_102	
J25	VCC_103	
J27	VCC_104	
J28	VCC_105	
J30	VCC_106	
J31	VCC_107	
J33	VCC_108	
J34	VCC_109	
J36	VCC_110	
J37	VCC_111	
J39	VCC_112	
J40	VCC_113	
K17	VCC_114	
K18	VCC_115	
K20	VCC_116	
K21	VCC_117	
K23	VCC_118	
K24	VCC_119	
K26	VCC_120	
K27	VCC_121	
K29	VCC_122	
K30	VCC_123	
K32	VCC_124	
K33	VCC_125	
K35	VCC_126	
K36	VCC_127	
K38	VCC_128	
K39	VCC_129	
L17	VCC_130	
L19	VCC_131	
L20	VCC_132	
L22	VCC_133	
L23	VCC_134	
L25	VCC_135	
L26	VCC_136	
L28	VCC_137	
L29	VCC_138	
L31	VCC_139	
L32	VCC_140	
L34	VCC_141	
L35	VCC_142	
L37	VCC_143	
L38	VCC_144	
L40	VCC_145	
M17	VCC_146	
M19	VCC_147	
M21	VCC_148	
M22	VCC_149	
M24	VCC_150	
M25	VCC_151	
M27	VCC_152	
M28	VCC_153	
M30	VCC_154	
M33	VCC_155	
M34	VCC_156	
M36	VCC_157	
M37	VCC_158	
M39	VCC_159	
M40	VCC_160	
N33	VCC_161	
N35	VCC_162	
N36	VCC_163	
N38	VCC_164	
N39	VCC_165	
P33	VCC_166	
P34	VCC_167	
P35	VCC_168	
P36	VCC_169	
P37	VCC_170	
P38	VCC_171	
P39	VCC_172	
P40	VCC_173	
R33	VCC_174	
R34	VCC_175	
R35	VCC_176	
R36	VCC_177	
R37	VCC_178	
R38	VCC_179	
R39	VCC_180	
R40	VCC_181	

NCTF

CGC_TP_NCTF	B39	TP_CPU_CGC_NCTF
VCC_NCTF_0	A38	=PPVCORE_S0_CPU 5 12 15
VCC_NCTF_1	C40	
FC_AE38	AE38	TP_CPU_FC_AE38 7
FC_AG40	AG40	TP_CPU_FC_AG40 7

15 12 5 =PPVCORE_S0_CPU

U1000
LYNNFIELD
LGA1156-SKT
(6 OF 10)
OMIT

CPU CORE SUPPLY

A23	VCC_0	
A24	VCC_1	
A26	VCC_2	
A27	VCC_3	
A33	VCC_4	
A35	VCC_5	
A36	VCC_6	
B23	VCC_7	
B25	VCC_8	
B26	VCC_9	
B28	VCC_10	
B29	VCC_11	
B31	VCC_12	
B32	VCC_13	
B34	VCC_14	
B35	VCC_15	
B37	VCC_16	
B38	VCC_17	
C23	VCC_18	
C24	VCC_19	
C25	VCC_20	
C27	VCC_21	
C28	VCC_22	
C30	VCC_23	
C31	VCC_24	
C33	VCC_25	
C34	VCC_26	
C36	VCC_27	
C37	VCC_28	
C39	VCC_29	
D23	VCC_30	
D24	VCC_31	
D26	VCC_32	
D27	VCC_33	
D29	VCC_34	
D30	VCC_35	
D32	VCC_36	
D33	VCC_37	
D35	VCC_38	
D36	VCC_39	
D38	VCC_40	
D39	VCC_41	
E22	VCC_42	
E23	VCC_43	
E25	VCC_44	
E26	VCC_45	
E28	VCC_46	
E29	VCC_47	
E31	VCC_48	
E32	VCC_49	
E34	VCC_50	
E35	VCC_51	
E37	VCC_52	
E38	VCC_53	
E40	VCC_54	
F21	VCC_55	
F22	VCC_56	
F24	VCC_57	
F25	VCC_58	
F27	VCC_59	
F28	VCC_60	
F30	VCC_61	
F31	VCC_62	
F33	VCC_63	
F34	VCC_64	
F36	VCC_65	
F37	VCC_66	
F39	VCC_67	
F40	VCC_68	
G20	VCC_69	
G21	VCC_70	
G23	VCC_71	
G24	VCC_72	
G26	VCC_73	
G27	VCC_74	
G29	VCC_75	
G30	VCC_76	
G32	VCC_77	
G33	VCC_78	
G35	VCC_79	
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G38	VCC_81	
G39	VCC_82	
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H20	VCC_84	
H22	VCC_85	
H23	VCC_86	
H25	VCC_87	
H26	VCC_88	
H28	VCC_89	
H29	VCC_90	
H31	VCC_91	
H32	VCC_92	
H34	VCC_93	
H35	VCC_94	
H37	VCC_95	
H38	VCC_96	
H40	VCC_97	
J18	VCC_98	
J19	VCC_99	

POWER

1.1V RAIL POWER

VTT_0	AA33	
VTT_1	AA34	
VTT_2	AA35	
VTT_3	AA36	
VTT_4	AA37	
VTT_5	AA38	
VTT_6	AB7	
VTT_7	AC33	
VTT_8	AC34	
VTT_9	AC35	
VTT_10	AC36	
VTT_11	AC37	
VTT_12	AC38	
VTT_13	AC39	
VTT_14	AC40	
VTT_15	AC5	
VTT_16	AC8	
VTT_17	AD33	
VTT_18	AD34	
VTT_19	AD35	
VTT_20	AD36	
VTT_21	AD37	
VTT_22	AD38	
VTT_23	AD39	
VTT_24	AD40	
VTT_25	AE33	
VTT_26	AE34	
VTT_27	AE39	
VTT_28	AE40	
VTT_29	AE8	
VTT_30	AF33	
VTT_31	AG33	
VTT_32	AJ17	
VTT_33	AJ19	
VTT_34	AJ21	
VTT_35	AJ23	
VTT_36	AJ25	
VTT_37	AJ27	
VTT_38	AJ29	
VTT_39	AJ31	
VTT_40	AJ32	
VTT_41	AK19	
VTT_42	AK20	
VTT_43	AK21	
VTT_44	AL20	
VTT_45	AL21	
VTT_46	L10	
VTT_47	M10	
VTT_48	M11	
VTT_49	M9	
VTT_50	N7	
VTT_51	P6	
VTT_52	P7	
VTT_53	P8	
VTT_54	T2	
VTT_55	T6	
VTT_56	T7	
VTT_57	T8	
VTT_58	V2	
VTT_59	V33	
VTT_60	V34	
VTT_61	V35	
VTT_62	V36	
VTT_63	V37	
VTT_64	V38	
VTT_65	V39	
VTT_66	V40	
VTT_67	V6	
VTT_68	V7	
VTT_69	V8	
VTT_70	W1	
VTT_71	W6	
VTT_72	Y33	
VTT_73	Y34	
VTT_74	Y35	
VTT_75	Y36	
VTT_76	Y37	
VTT_77	Y38	

=PPVTT_S0_CPU 5 10 15 47 65

CPU VIDS

PSI*	AG38	CPU_PSI_L	OUT 65 89
VID_0/MSID_0	U40	CPU_VID<0>	OUT 15 65 89
VID_1/MSID_1	U39	CPU_VID<1>	OUT 15 65 89
VID_2/MSID_2	U38	CPU_VID<2>	OUT 15 65 89
VID_3/CSC_0	U37	CPU_VID<3>	OUT 15 65 89
VID_4/CSC_1	U36	CPU_VID<4>	OUT 15 65 89
VID_5/CSC_2	U35	CPU_VID<5>	OUT 15 65 89
VID_6	U34	CPU_VID<6>	OUT 15 65 89
VID_7	U33	CPU_VID<7>	OUT 15 65 89
VTT_SELECT	AF39	TP_CPU_VTTSELECT	

SENSE LINES

ISENSE	T40	VR_CPU_IOUT	CONNECTED TO THE IMON OUT FROM CPU REG IN 65 88
VCC_SENSE	T35	CPU_VCC_PKG_SENSE_P	OUT 50 65 89
VSS_SENSE	T34	CPU_VCC_PKG_SENSE_N	OUT 65 89
VTT_SENSE	AE35	CPU_VTTSENSE_P	OUT 68 89
VSS_SENSE_VTT	AE36	CPU_VTTSENSE_N	OUT 68 89

5 =PPVAXG_S0_CPU
THIS SUPPLY IS NEEDED ONLY FOR SYSTEM WITH DALE IG

U1000
LYNNFIELD
LGA1156-SKT
(7 OF 10)
OMIT

GRAPHICS

A14	VAXG_0	
A15	VAXG_1	
A17	VAXG_2	
A18	VAXG_3	
B14	VAXG_4	
B15	VAXG_5	
B17	VAXG_6	
B18	VAXG_7	
C14	VAXG_8	
C15	VAXG_9	
C17	VAXG_10	
C18	VAXG_11	
C20	VAXG_12	
C21	VAXG_13	
D14	VAXG_14	
D15	VAXG_15	
D17	VAXG_16	
D18	VAXG_17	
D20	VAXG_18	
D21	VAXG_19	
E14	VAXG_20	
E15	VAXG_21	
E17	VAXG_22	
E18	VAXG_23	
E20	VAXG_24	
F14	VAXG_25	
F15	VAXG_26	
F17	VAXG_27	
F18	VAXG_28	
F19	VAXG_29	
G14	VAXG_30	
G15	VAXG_31	
G17	VAXG_32	
G18	VAXG_33	
H14	VAXG_34	
H15	VAXG_35	
H17	VAXG_36	
J14	VAXG_37	
J15	VAXG_38	
J16	VAXG_39	
K14	VAXG_40	
K15	VAXG_41	
K16	VAXG_42	
L14	VAXG_43	
L15	VAXG_44	
L16	VAXG_45	
M14	VAXG_46	
M15	VAXG_47	
M16	VAXG_48	

SENSE LINES

VSSAXG_SENSE	B13	TP_GFX_VSENSE_N 7
VAXG_SENSE	A13	TP_GFX_VSENSE_P 7

GRAPHICS VIDS

GFX_VID_0	G10	TP_GFX_VID<0> 7
GFX_VID_1	B12	TP_GFX_VID<1> 7
GFX_VID_2	E12	TP_GFX_VID<2> 7
GFX_VID_3	E11	TP_GFX_VID<3> 7
GFX_VID_4	C12	TP_GFX_VID<4> 7
GFX_VID_5	G11	TP_GFX_VID<5> 7
GFX_VID_6	J11	TP_GFX_VID<6> 7
GFX_VR_EN	F12	TP_GFX_VR_EN
GFX_DPRSLPVR	J10	TP_GFX_DPRSLPVR
GFX_IMON	F6	

POWER

=PP1V5_CPU_MEM 5 10 15 29

DDR3-1.5V RAILS

VDDQ_0	AJ11	
VDDQ_1	AJ13	
VDDQ_2	AJ15	
VDDQ_3	AT10	
VDDQ_4	AT18	
VDDQ_5	AT21	
VDDQ_6	AU11	
VDDQ_7	AV13	
VDDQ_8	AV16	
VDDQ_9	AV19	
VDDQ_10	AV22	
VDDQ_11	AV25	
VDDQ_12	AV28	
VDDQ_13	AW9	
VDDQ_14	AY11	
VDDQ_15	AY14	
VDDQ_16	AY17	
VDDQ_17	AY23	
VDDQ_18	AY26	

=PP1V8_S0_CPU_PLL 5 15 64

1.8V

VCCPLL_0	AF7	
VCCPLL_1	AF8	
VCCPLL_2	AG8	

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
CPU POWER

Apple Inc.

DRAWING NUMBER 051-8337
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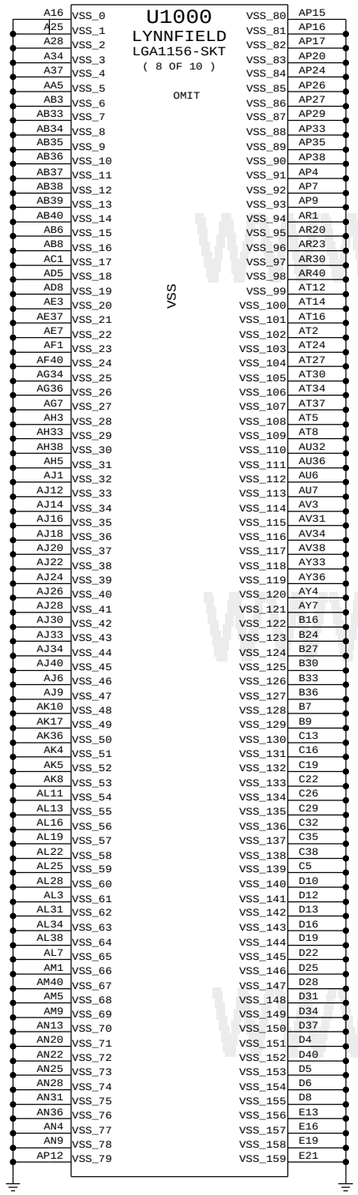

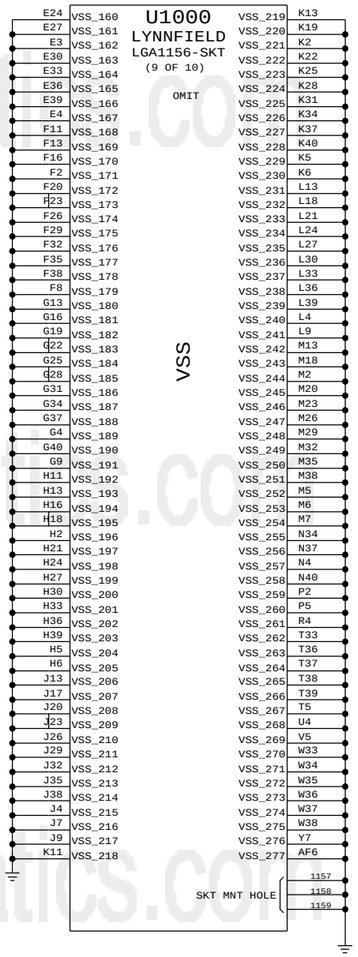

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE

CPU GROUNDS

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BRANCH

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84 24 9 CPU_CFG<3>

R1500 1.5K 5% 1/16W MF-LF 402

CPU_CFG<3> IS USED FOR PCIE LANE REVERSAL

CPU_CFG<3>	PCIE LANES
0	REVERSAL
1	NO REVERSAL

UNUSED GPIO SIGNALS

14 5 =PP3V3_S0_PCH_STRAPS

R1591 R1529 R1523 R1524 R1528 R1508 R1526 R1504 R1506 R1503 R1509 10K 5% 1/16W MF-LF 402

PCH_GPIO0_BMBUSY_L 20
PCH_GPIO21_SATA0GP 17
PCH_GPIO19_SATA1GP 17
PCH_GPIO37_SATA3GP 20
PCH_GPIO49_SATA5GP 20
PCH_GPIO6_TACH2 20
PCH_GPIO34_STP_PCI_L 20
PCH_GPIO38_SLOAD 20
PCH_GPIO39_SDATAOUT0 20
AP_PWR_EN 20
FW_PWR_EN 20

UNUSED GPIO SIGNALS

14 5 =PP3V3_S5_PCH_STRAPS

R1538 R1535 R1590 BUF_CLK R1517 10K 5% 1/16W MF-LF 402

PCH_GPIO8_FCIM_EN_L 20
PCH_GPIO24 20
BRCRYPT_PWR_EN 17
PCH_GPIO15 20

37 17 ENET_ENERGY_DET
37 20 ENET_LOW_PWR
91 18 PM_LAN_PWRGD

R1501 R1510 R1511 10K 5% 1/16W MF-LF 402

14 5 =PP3V3_S0_PCH_STRAPS

R1525 R1522 R1539 10K 5% 1/16W MF-LF 402

ENET_CLKREQ_L 17 37
FW_CLKREQ_L 17 40
MINI_CLKREQ_L 17 33

14 5 =PP3V3_S5_PCH_STRAPS

PCH_VRM R1530 R1515 10K 5% 1/16W MF-LF 402

PM_BATLOW_L 18 45 91
PCH_GPIO27_VRMEN 20

14 5 =PP3V3_S0_PCH_STRAPS

R1575 R1574 R1573 R1571 R1570 R1543 10K 5% 1/16W MF-LF 402

PCH_SPKR 17
PM_CLKRUN_L 18 46 48 91
SPI_DESCRIPTOR_OVERRIDE_L 17 46
BRCRYPT_RESET 17
PCH_CLKOUTFLEX1 17
PCH_CLKOUTFLEX2 17
PCH_CLKOUTFLEX3 17

R1572 10K 5% 1/16W MF-LF 402

UNUSED CLKREQS

14 5 =PP3V3_S0_PCH_STRAPS

R1536 R1532 R1533 10K 5% 1/16W MF-LF 402

EXCARD_CLKREQ_L 17
T28_CLKREQ_L 17
PEB_CLKREQ_L 17

NOSTUFF R1537 10K 5% 1/16W MF-LF 402

IF LIKE TO HAVE THE PEB CLOCKS ENABLED. STUFF R1535 AND UNSTUFF R1534

14 5 =PP3V3_S0_PCH_STRAPS

R1527 R1507 10K 5% 1/16W MF-LF 402

FW_PME_L 20 40
SMC_RUNTIME_SCI_L 20 46

20 ODD_PWR_EN_L
36 20 WOL_EN
20 PCH_INIT3V3_L

NOSTUFF R1550 1K 5% 1/16W MF-LF 402
R1555 R1512 10K 5% 1/16W MF-LF 402

BOOT STRAP OPTIONS

19 PCH_PCI_GNT3_L
19 PCH_PCI_GNT2_L
19 PCH_PCI_GNT1_L
19 PCH_PCI_GNT0_L

NOSTUFF R1551 R1552 R1553 R1554 10K 5% 1/16W MF-LF 402

SYNC_MASTER=NICK SYNC_DATE=12/08/2009

PAGE TITLE
STRAPS,PULL UPS,PULL DOWNS FOR PCH AND CPU

Apple Inc.

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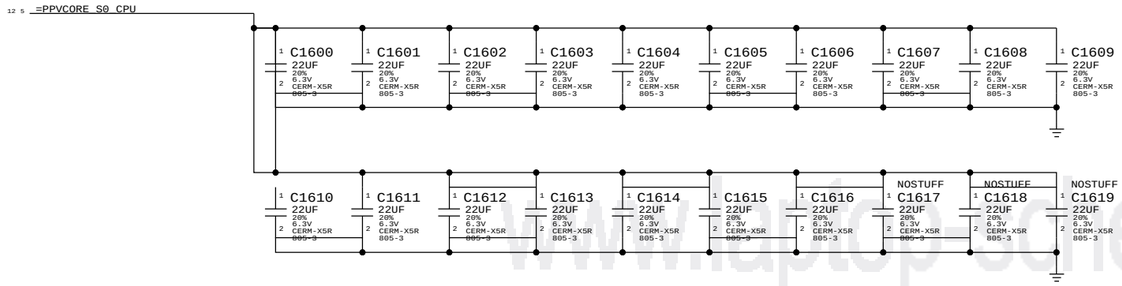
CPU VCORE DECOUPLING

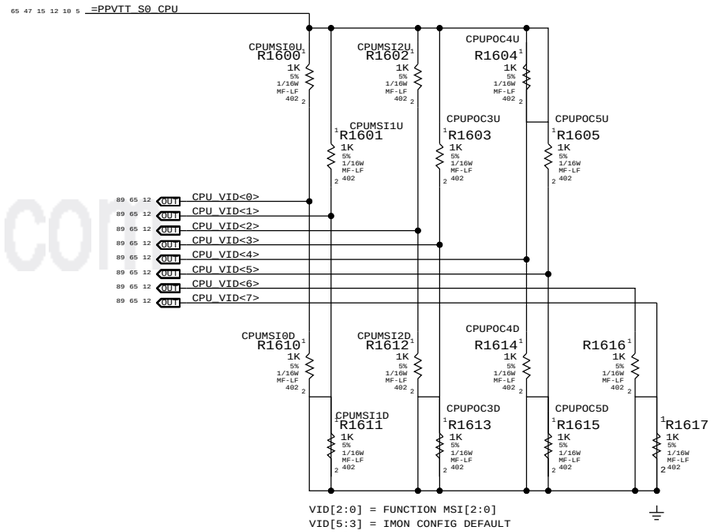
INTEL RECOMMENDATION 17X 22UF 0805



BULK CAPS ON CPU VREG PAGE 74

CPU Power On Configuration (POC) Straps

Intel recommends all option straps should be provided in layout



VID[2:0] = FUNCTION MSI[2:0]
VID[5:3] = IMON CONFIG DEFAULT
VID[6] = Reserved (0)
VID[7] = VRD SELECT (0)

MSI - MARKET SEGMENT IDENTIFICATION
PREVENTS THE PLATFORM BOOTING USING A HIGHER POWERED CPU

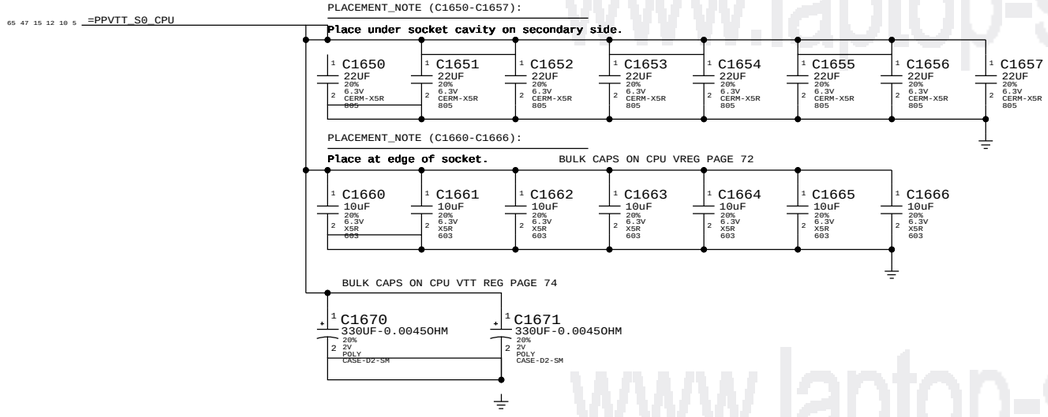
BOM GROUP	IMAX @ 900mV	CPU Gain Setting	BOM OPTIONS	Equivalent Gain
CPUPOC_IMAX_DIS		000	CPUPOC5D,CPUPOC4D,CPUPOC3D	
CPUPOC_IMAX_0_40	40A	001	CPUPOC5D,CPUPOC4D,CPUPOC3U	45
CPUPOC_IMAX_40_60	60A	010	CPUPOC5D,CPUPOC4U,CPUPOC3D	30
CPUPOC_IMAX_60_80	80A	011	CPUPOC5D,CPUPOC4U,CPUPOC3U	22.5
CPUPOC_IMAX_80_100	100A	100	CPUPOC5U,CPUPOC4D,CPUPOC3D	18
CPUPOC_IMAX_100_120	120A	101	CPUPOC5U,CPUPOC4D,CPUPOC3U	15
CPUPOC_IMAX_120_140	140A	110	CPUPOC5U,CPUPOC4U,CPUPOC3D	12.857
CPUPOC_IMAX_140_180	180A	111	CPUPOC5U,CPUPOC4U,CPUPOC3U	10

BOM GROUP	BOM OPTIONS
CLARKDALE_73W	CKD,CPUPOC_IMAX_60_80,CPUMSI2U,CPUMSI1D,CPUMSI0U
LYNNFIELD_82W	LFD,CPUPOC_IMAX_60_80,CPUMSI2U,CPUMSI1D,CPUMSI0U
LYNNFIELD_95W	LFD,CPUPOC_IMAX_100_120,CPUMSI2U,CPUMSI1U,CPUMSI0D

NOTE: BOM Configurations should not call out CPUPOCnU/D BOMOPTIONs directly.
Instead call out appropriate BOM GROUP defined in tables above.

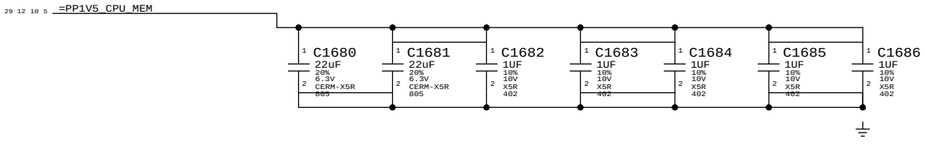
VTT (CPU Uncore) DECOUPLING

8X 22UF 0805, 7X 10UF 0805 INTEL RECOMMENDATION 9X22UF 0805



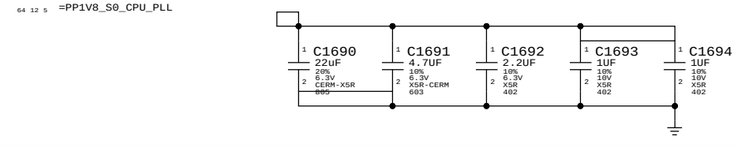
Memory (CPU VCCDDR) DECOUPLING

2x 22uF 0805, 5x 1uF 0402



PLL (CPU VCCSFR) DECOUPLING

1x 22uF 0805, 1x 4.7uF 0603, 1x 2.2uF 0402, 2x 1uF 0402



SYNC MASTER=NICK SYNC DATE=12/08/2009

PAGE TITLE
CPU NON-GFX DECOUPLING

Apple Inc.

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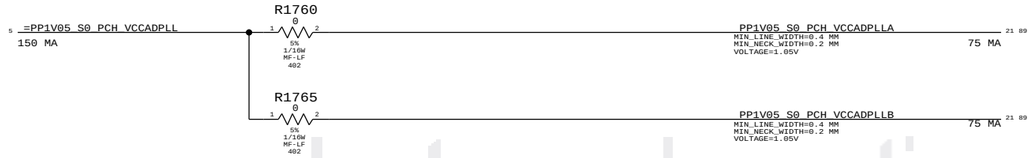

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
CPU/PCH GFX DECOUPLING

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D
REVISION A.0.0
BRANCH
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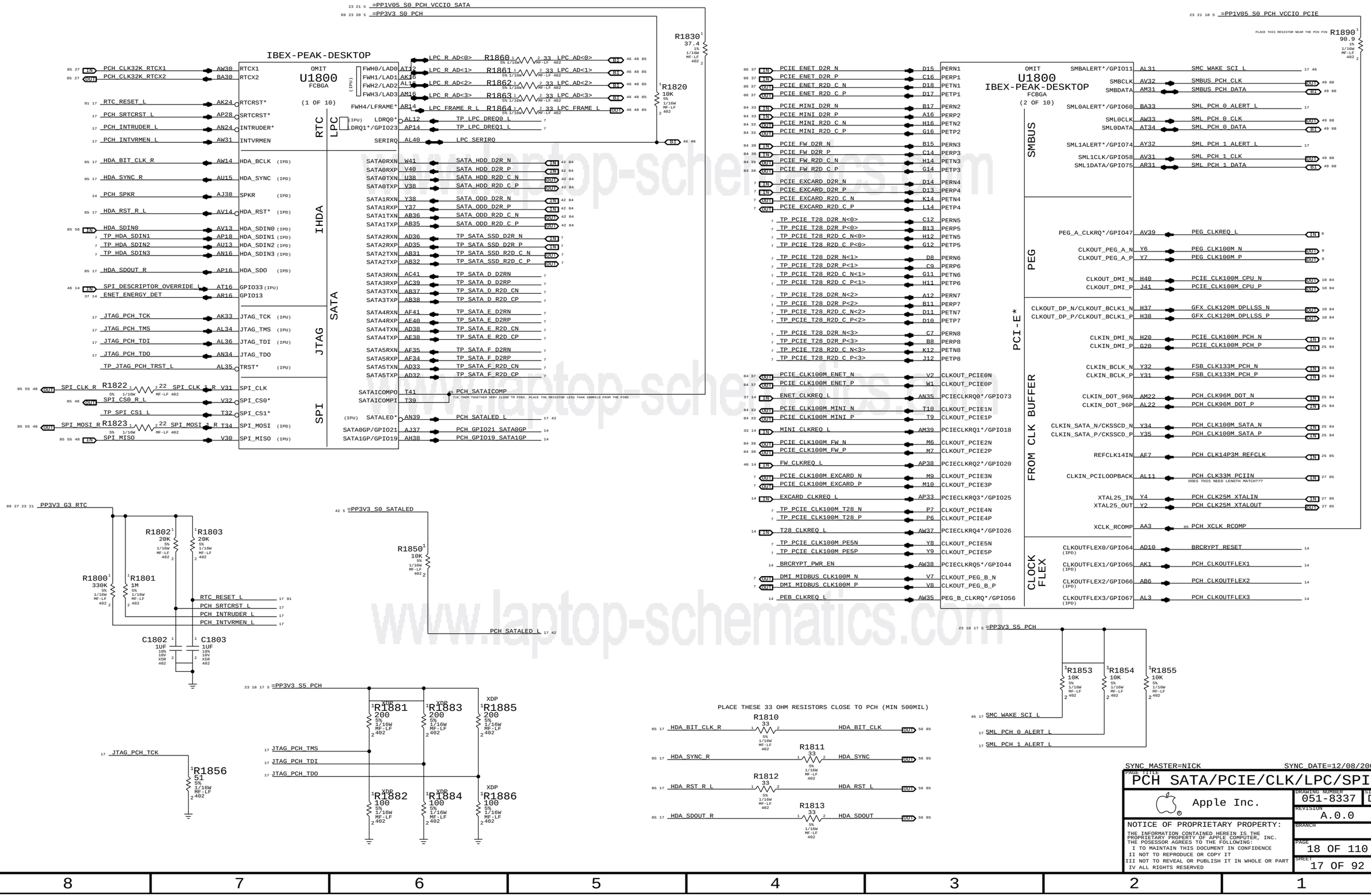

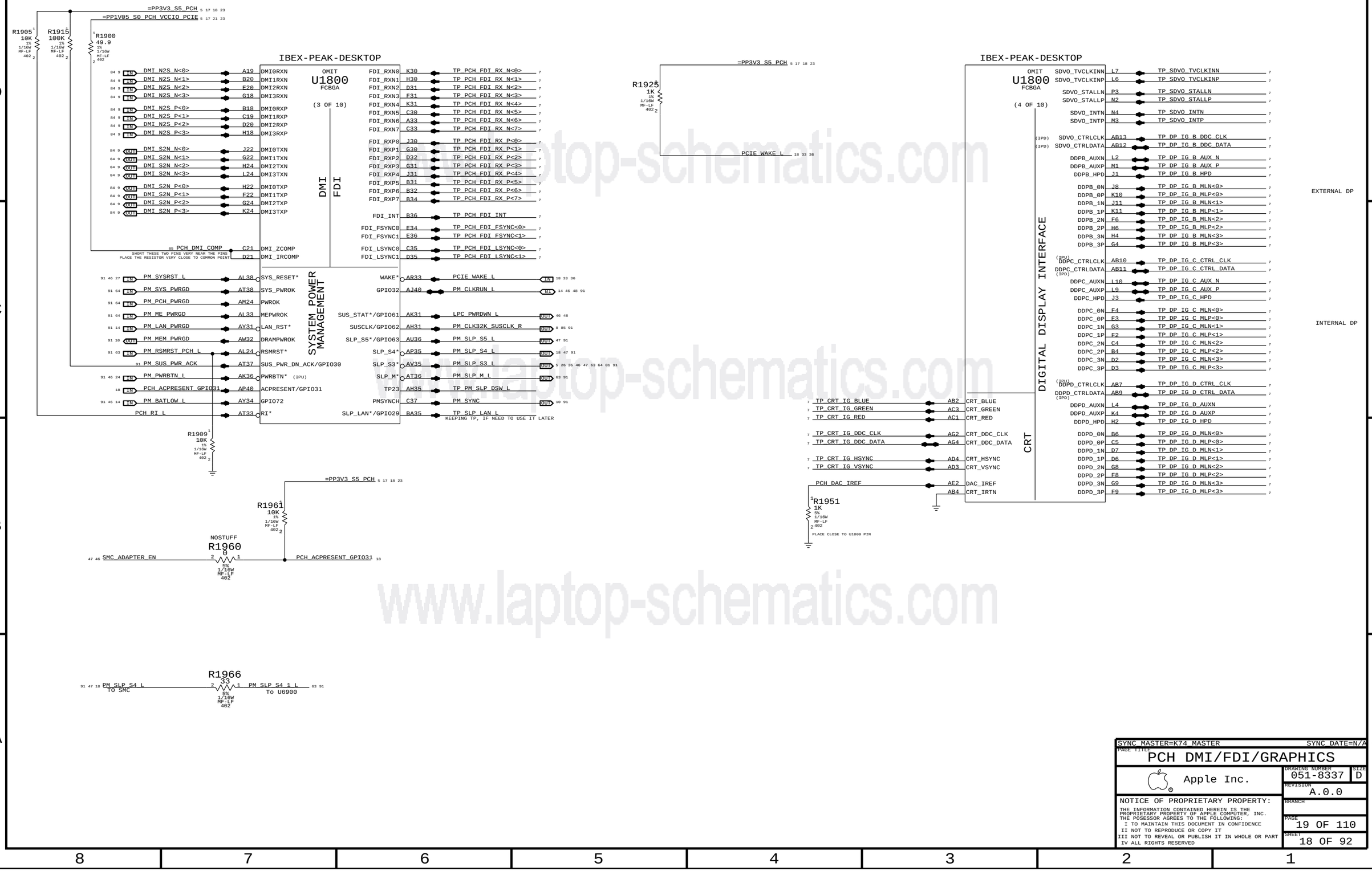

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
PCH DMI/FDI/GRAPHICS

Apple Inc.

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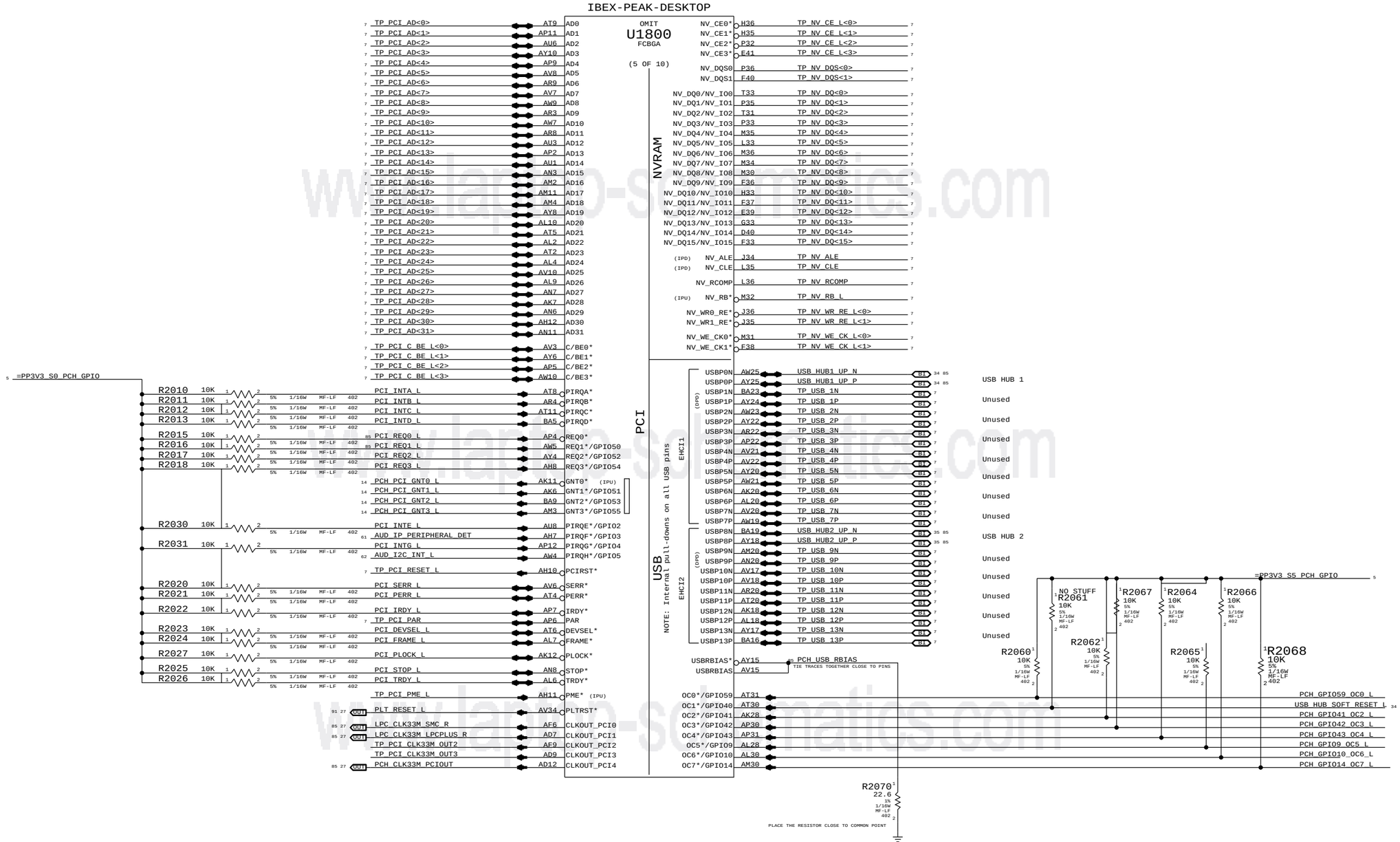

SYNC_MASTER=NICK SYNC_DATE=12/08/2009

PAGE TITLE
PCH PCI/FLASHCACHE/USB

Apple Inc.

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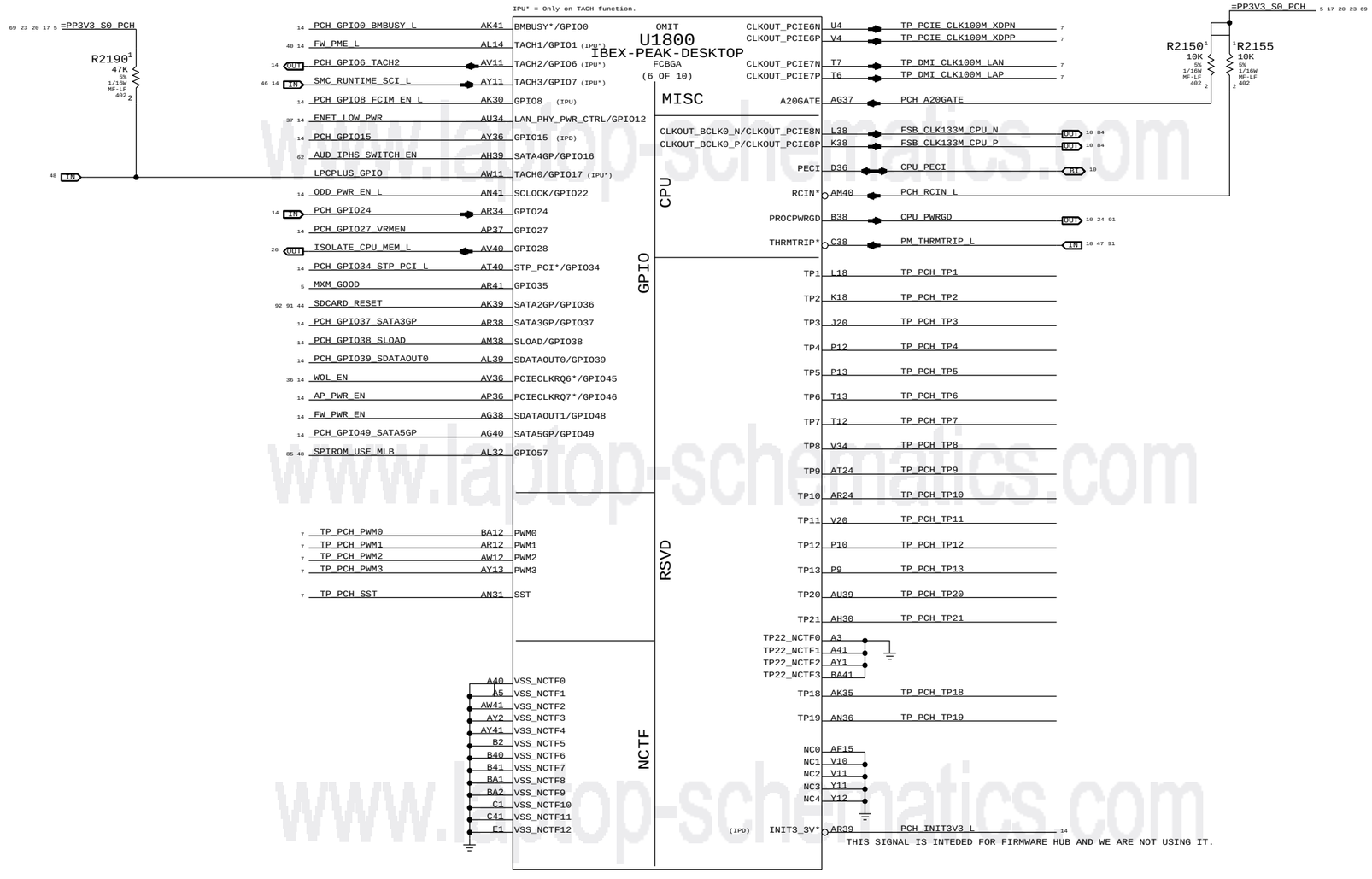

SYNC_MASTER=K23F SYNC_DATE=11/30/2009

PAGE TITLE: PCH MISC

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

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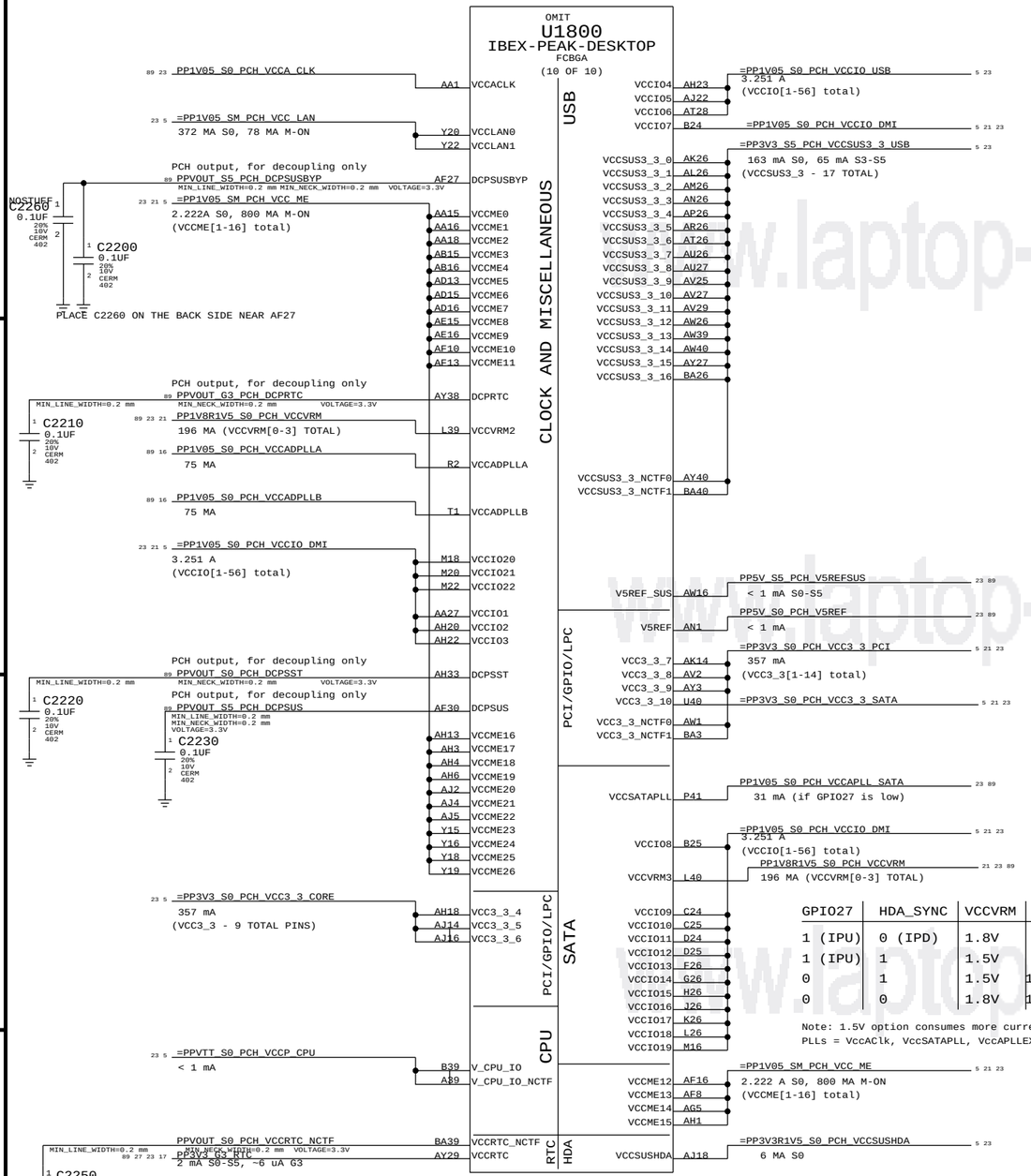

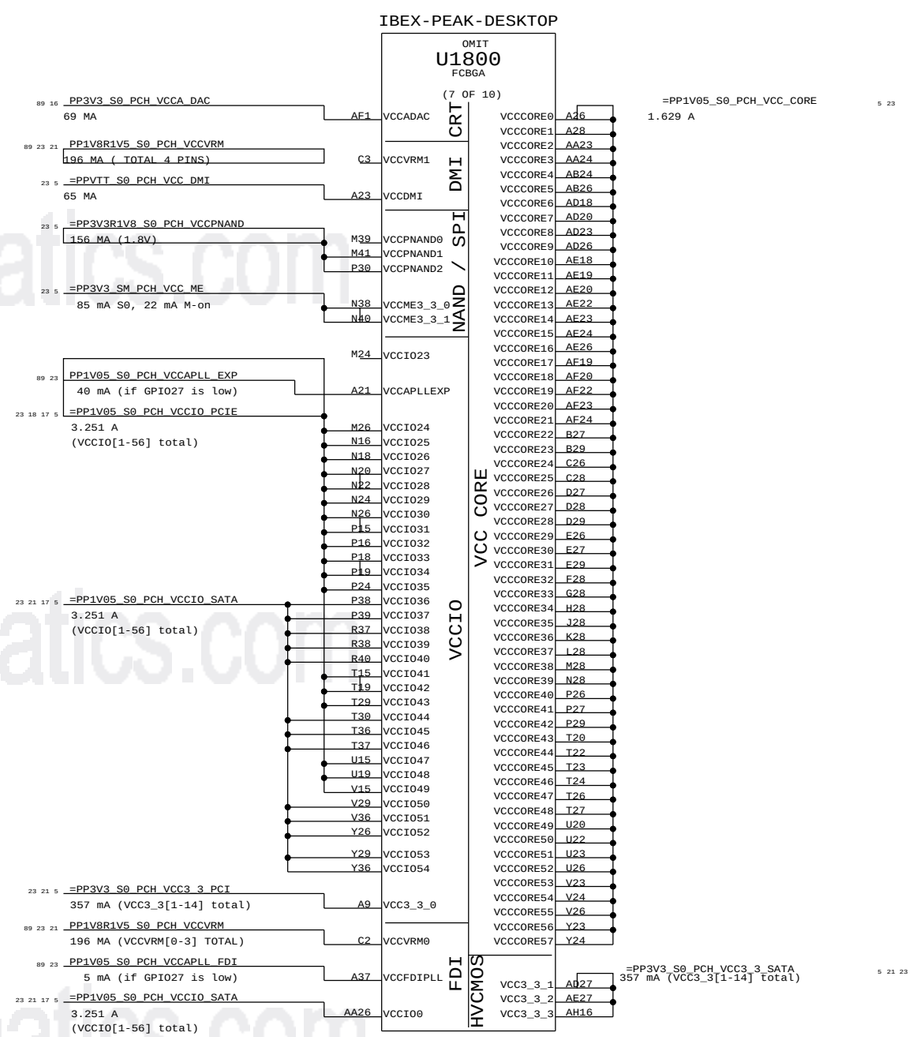

PAGE TITLE	PCH POWER
	Apple Inc.
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IBEX-PEAK-DESKTOP

OMIT
U1800
FCBGA
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A14			AJ24
A30			AJ26
A35			AJ28
A7			AK10
AA19			AK22
AA20			AK3
AA22			AK32
AA38			AK34
AA39			AK37
AA4			AK5
AA41			AK8
AB18			AK9
AB19			AL8
AB20			AM10
AB22			AM12
AB23			AM14
AB27			AM18
AB29			AM28
AB30			AM32
AB33			AN12
AB34			AN14
AB40			AN18
AB5			AN22
AB8			AN28
AC37			AN30
AC5			AN37
AD11			AN5
AD19			AP20
AD2			AP24
AD22			AR1
AD24			AR11
AD29			AR18
AD30	VSS	VSS	AR28
AD31			AR30
AD34			AT14
AD39			AT18
AD40			AT22
AD6			AU12
AD8			AU16
AE3			AU19
AE39			AU20
AE4			AU22
AE11			AU23
AE12			AU29
AE18			AU30
AE26			AU33
AE29			AU37
AE3			AU38
AE31			AU41
AE32			AU5
AE33			AU9
AE36			AV24
AE37			AV28
AE39			AV5
AE5			AW17
AH15			AW18
AH19			AW24
AH24			AW28
AH26			AW3
AH27			B10
AH29			B22
AH32			BA14
AH34			BA21
AH36			BA28
AH41			BA37
AH9			BA7
AJ20			C10

IBEX-PEAK-DESKTOP

OMIT
U1800
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C11			L22
C17			L3
C18			L30
C23			L31
C31			L32
C32			L34
C39			L8
D22			M11
D34			M12
D37			M14
D39			M33
E12			M37
E13			M5
E15			M8
E16			N14
E19			N37
E22			N5
E23			P1
E30			P11
E33			P20
E37			P22
E4			P23
E5			P31
E6			P34
E8			P4
E9			P8
F11			R4
F12			R5
F14			T11
F16			T16
F18	VSS	VSS	T18
F20			T3
F24			T35
F30			T5
F34			T8
F5			U16
G1			U18
G34			U2
G38			U24
G39			U27
G41			U3
H31			U39
H5			V12
H7			V13
H9			V16
J14			V18
J16			V19
J18			V22
J24			V27
J37			V3
J39			V33
J5			V35
J6			V39
J7			V6
K16			V9
K2			W3
K20			W37
K22			W39
K3			W5
K32			Y10
K39			Y13
K40			Y27
L11			Y30
L12			Y33
L16			Y40
L20			Y5

SYNC_MASTER=K23F SYNC_DATE=11/30/2009

PAGE TITLE
PCH GROUNDS

Apple Inc.

DRAWING NUMBER 051-8337
SIZE D
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PCH V5REF_SUS Filter & Follower
(PCH Reference for 5V Tolerance on USB)

=PP3V3_S5_PCH
=PP5V_S5_PCH
1 mA S0-S5

R2400 10 5% 1/16W MF-LF 402
D2400 BAT54DW-X-G SOT-363 (NC)
PP5V_S5_PCH_V5REFSUS (21 89)
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=5V
<1 MA S0-S5

C2400 0.1UF 20% 16V CERM 402

PLACEMENT_NOTE:
PLACE C2400 NEAR BALL AW16

PCH V5REF Filter & Follower
(PCH Reference for 5V Tolerance on PCI)

=PP3V3_S0_PCH
=PP5V_S0_PCH
1 mA

R2401 100 5% 1/16W MF-LF 402
D2400 BAT54DW-X-G SOT-363 (NC)
PP5V_S0_PCH_V5REF (21 89)
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=5V
<1 MA

C2401 1UF 10% 10V X5R 402

PLACEMENT_NOTE:
PLACE C2401 NEAR BALL AN1

PCH VCCRTC BYPASS
(PCH RTC 3.3V PWR)

PP3V3_G3_RTC (89 27 21 17)
2 mA S0-S5 /
6 uA G3

C2420 1UF 10% 6.3V CERM 402
C2421 0.1UF 10% 16V XSR 402
C2422 0.1UF 10% 16V XSR 402

PLACEMENT_NOTES (all 3):
PLACE C2421 NEAR BALL AY20
PLACE C2420 NEAR BALL AY29

PCH VCCSUS3_3 BYPASS
(PCH SUSPEND USB 3.3V PWR)

=PP3V3_S5_PCH_VCCSUS3_3_USB (23 21 5)

C2425 0.1UF 10% 16V XSR 402

PLACEMENT_NOTE:
PLACE C2425 NEAR BALL AV25

357 MA S0 /
88 MA S3-S5
(VCCSUS3_3 Total)

PCH USB/VCCSUS3_3 BYPASS
(PCH SUSPEND USB 3.3V PWR)

=PP3V3_S5_PCH_VCCSUS3_3_USB (23 21 5)

C2426 0.1UF 10% 16V XSR 402
C2427 0.1UF 10% 16V XSR 402

PLACEMENT_NOTES:
PLACE C2426 NEAR BALL AW39
PLACE C2427 NEAR BALL AJ18

PCH VCCME3_3 BYPASS
(PCH ME 3.3V PWR)

=PP3V3_SM_PCH_VCC_ME (21 5)

C2430 0.1UF 10% 16V XSR 402

PLACEMENT_NOTE:
PLACE C2430 NEAR BALL N38

PCH CORE/VCC3_3 BYPASS
(PCH MISC 3.3V PWR)

=PP3V3_S0_PCH_VCC3_3_CORE (21 5)

C2435 0.1UF 10% 16V XSR 402
C2439 0.1UF 10% 16V XSR 402

PLACEMENT_NOTE:
PLACE C2435 NEAR BALL AE27
PLACE C2439 NEAR BALL A9

PCH VCC3_3 BYPASS
(PCH PCI 3.3V PWR)

=PP3V3_S0_PCH_VCC3_3_PCI (21 5)

C2436 0.1UF 10% 16V XSR 402
C2437 0.1UF 10% 16V XSR 402
NOSTUFF
C2438 0.1UF 10% 16V XSR 402

PLACEMENT_NOTE:
PLACE C2436 NEAR BALL AV2
PLACE C2437 NEAR BALL AH16
PLACE C2438 NEAR BALL AH16

PCH VCC3_3 BYPASS
(PCH SATA 3.3V PWR)

=PP3V3_S0_PCH_VCC3_3_SATA (21 5)

C2446 0.1UF 10% 16V XSR 402

PLACEMENT_NOTE:
PLACE C2446 NEAR BALL U40

PCH VCCPNAND BYPASS
(PCH NAND 1.8V/3.3V PWR)

=PP3V3R1V8_S0_PCH_VCCPNAND (21 5)

C2440 0.1UF 10% 16V XSR 402
NOSTUFF
C2441 0.1UF 10% 16V XSR 402

PLACEMENT_NOTE:
PLACE C2440 NEAR BALL P30
PLACE C2441 NEAR BALL P30

PCH VCCSUSHDA BYPASS
(PCH HD Audio 3.3V/1.5V PWR)

=PP3V3R1V5_S0_PCH_VCCSUSHDA (21 5)
6 MA

C2445 1UF 10% 6.3V CERM 402

PLACEMENT_NOTE:
PLACE C2445 NEAR BALL AJ18

PCH V_CPU_IO BYPASS
(PCH 1.1V/1.05V CPU I/O PWR)

=PPVTT_S0_PCH_VCCP_CPU (21 5)
<1 MA

C2450 4.7UF 20% 6.3V X5R 603
C2451 0.1UF 10% 16V XSR 402
C2452 0.1UF 10% 16V XSR 402

PLACEMENT_NOTES (all 3):
PLACE C2450 NEAR BALL B39

PCH VCCIO BYPASS
(PCH DMI 1.05V PWR)

=PPVTT_S0_PCH_VCC_DMI (21 5)
65 MA

C2455 1UF 10% 6.3V CERM 402

PLACEMENT_NOTE:
PLACE C2455 NEAR BALL A23

PCH VCCLAN BYPASS
(PCH 1.05V LAN Core PWR)

=PP1V05_SM_PCH_VCC_LAN (21 5)
372 MA

R2460 1K 5% 1/10W MF-LF 402

PLACEMENT_NOTE:

PCH VCCME BYPASS
(PCH 1.05V ME Core PWR)

=PP1V05_SM_PCH_VCC_ME (21 5)
2.22 A

C2465 22UF 20% 6.3V CERM 805
C2466 22UF 20% 6.3V CERM 805
C2467 10UF 20% 6.3V X5R 603
C2468 1UF 10% 6.3V CERM 402
C2469 1UF 10% 6.3V CERM 402

PLACEMENT_NOTES:
PLACE C2465 NEAR BALL AB15
PLACE C2466 NEAR BALL AH4
PLACE C2467 NEAR BALL AH1
PLACE C2468 NEAR BALL AJ4
PLACE C2469 NEAR BALL AF10

PCH VCCIO BYPASS
(PCH CLK 1.05V PWR)

=PP1V05_S0_PCH_VCCIO_DMI (21 5)

C2475 1UF 10% 6.3V CERM 402
C2476 1UF 10% 6.3V CERM 402
C2477 1UF 10% 6.3V CERM 402

PLACEMENT_NOTES:
PLACE C2475 NEAR BALL D25
PLACE C2476 NEAR BALL H26
PLACE C2477 NEAR BALL AH22

3.251 A S0 /
369 MA IDLE
(VCCIO TOTAL)

PCH VCCIO BYPASS
(PCH USB 1.05V PWR)

=PP1V05_S0_PCH_VCCIO_USB (21 5)

C2488 4.7UF 20% 6.3V X5R 603
C2480 1UF 10% 6.3V CERM 402

PLACEMENT_NOTE:
PLACE C2480 NEAR BALL AJ22
PLACE C2488 NEAR BALL AH23

PCH VCCIO BYPASS
(PCH SATA 1.05V PWR)

=PP1V05_S0_PCH_VCCIO_SATA (21 17 5)

C2486 22UF 20% 6.3V CERM 805
C2485 1UF 10% 6.3V CERM 402

PLACEMENT_NOTE:
PLACE C2485 NEAR BALL Y26
PLACE C2485 NEAR BALL Y29

PCH VCCIO BYPASS
(PCH PCIE 1.05V PWR)

=PP1V05_S0_PCH_VCCIO_PCIE (21 18 17 5)

C2490 22UF 20% 6.3V CERM 805
C2491 1UF 10% 6.3V CERM 402
C2492 1UF 10% 6.3V CERM 402
C2493 1UF 10% 6.3V CERM 402
C2494 1UF 10% 6.3V CERM 402

PLACEMENT_NOTES (all 5):
PLACE C2465 NEAR BALL P18
PLACE C2491 NEAR BALL P18
PLACE C2492 NEAR BALL P15
PLACE C2493 NEAR BALL U15
PLACE C2465 NEAR BALL P24

=PP1V8R1V5_S0_PCH_VCCVRM (5)
196 MA

PCH_VRM
R2410 0 5% 1/10W MF-LF 402

PP1V8R1V5_S0_PCH_VCCVRM (21 89)
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
(OR 1.5V)
196 MA

GPIO27: 1 = enabled, 0 = disabled

NOTE: VccVRM input also supports
1.5V, but draws more current.
HDA_SYNC: 0 = 1.8V, 1 = 1.5V

PCH VCCAPLLEXP Filter
(PCH PCIe PLL PWR)

PP1V05_S0_PCH_VCCAPLL_EXP (21 89)
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.05V

C2413 1UF 10% 6.3V CERM 402

PLACEMENT_NOTES:
PLACE C2413 AT BALL A21

PCH VCCFDIPLL Filter
(PCH FDI PLL PWR)

PP1V05_S0_PCH_VCCAPLL_FDI (21 89)
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.05V

C2415 1UF 10% 6.3V CERM 402

PLACEMENT_NOTES:
PLACE C2415 AT BALL A37

PCH VCCSATAPLL Filter
(PCH SATA PLL PWR)

PP1V05_S0_PCH_VCCAPLL_SATA (21 89)
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.05V

C2417 1UF 10% 6.3V CERM 402

PLACEMENT_NOTES:
PLACE C2417 AT BALL P41

PCH VCCACLK Filter
(PCH Misc PLL PWR)

PP1V05_S0_PCH_VCCA_CLK (21 89)
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.05V

C2419 1UF 10% 6.3V CERM 402

PLACEMENT_NOTES:
PLACE C2419 AT BALL AA1

PCH VCCCORE BYPASS
(PCH 1.05V CORE PWR)

=PP1V05_S0_PCH_VCC_CORE (21 5)
1.629 A

C2470 10UF 20% 6.3V X5R 603
C2471 1UF 10% 6.3V CERM 402
C2472 4.7UF 20% 6.3V X5R 603
C2473 22UF 20% 6.3V CERM 805

PLACEMENT_NOTES:
PLACE C2470 NEAR BALL AE18
PLACE C2471 NEAR BALL AE18
PLACE C2472 NEAR BALL AE18
PLACE C2473 NEAR BALL AE18

Current numbers from Ibex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
PCH DECOUPLING

Apple Inc.

DRAWING NUMBER 051-8337
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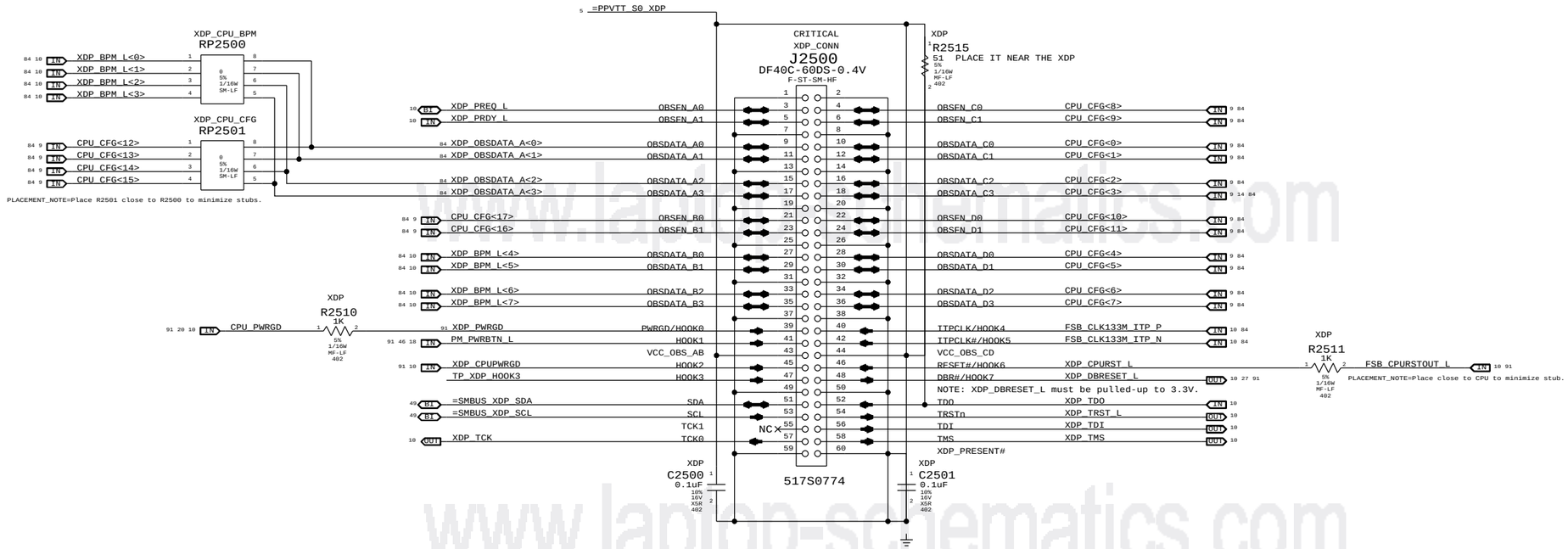
PROCESSOR MINI XDP



SYNC_MASTER=NICK SYNC_DATE=12/08/2009

PAGE TITLE
EXTENDED DEBUG PORT(XDP)

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D
REVISION A.0.0
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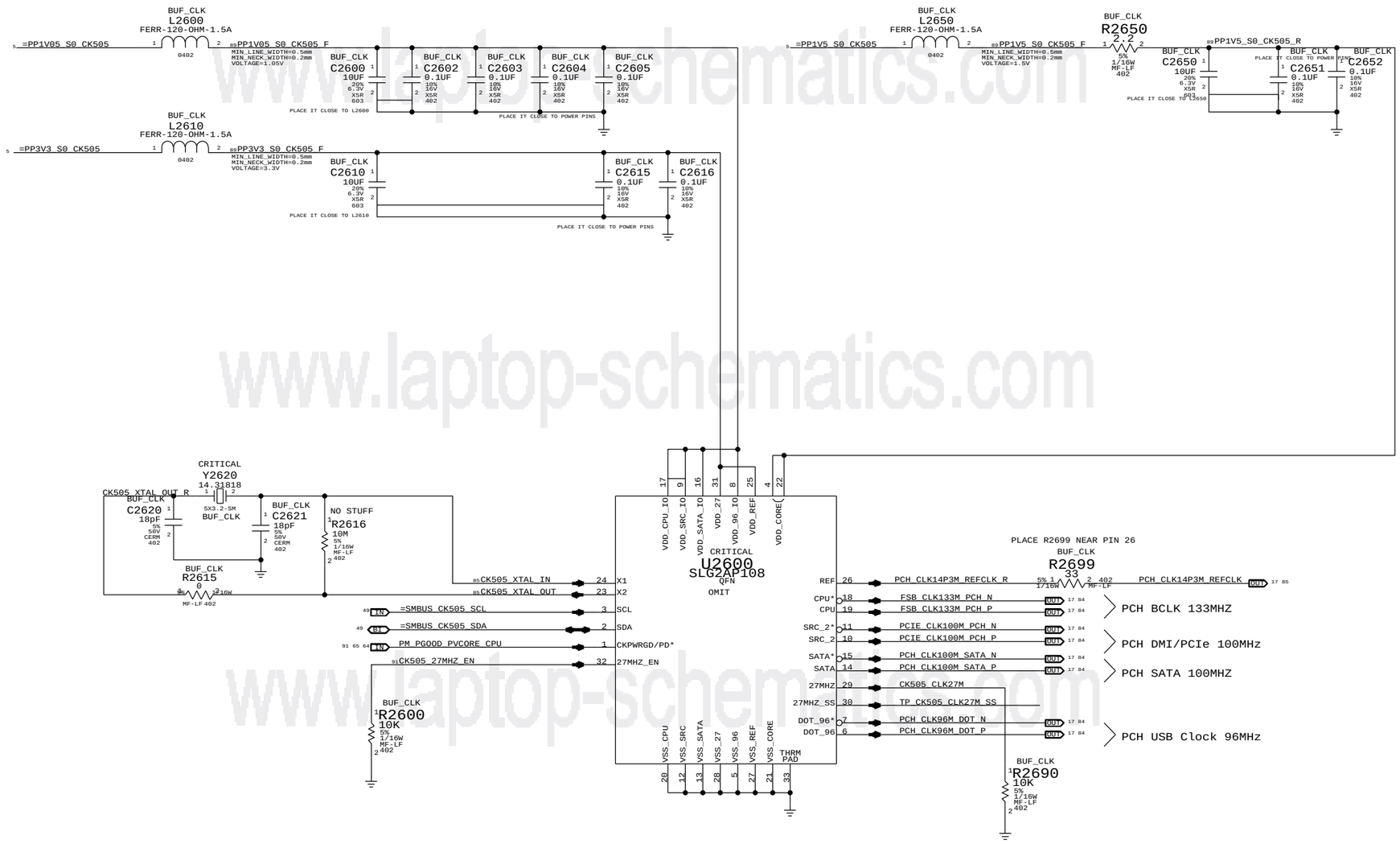

SYNC_MASTER=K23F SYNC_DATE=11/30/2009

PAGE TITLE: CLOCK (CK505)

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

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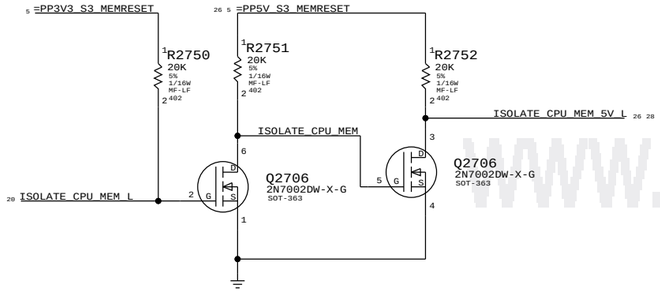
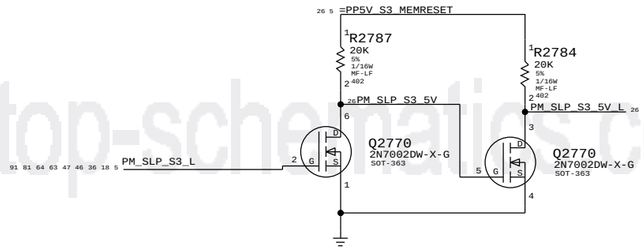
DDR3 RESET Support

LFD CANNOT CONTROL THIS SIGNAL DIRECTLY SINCE IT MUST BE HIGH IN SLEEP AND CPU MEM RAILS ARE NOT POWERED IN SLEEP.

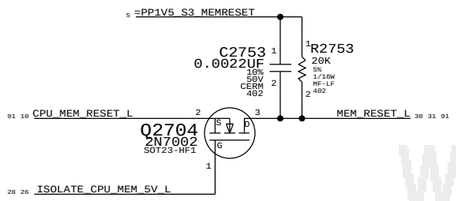
	CPU_RESET_L	ISOLATE_L	MEM_RESET_L
S5	0	3.3V	0
S0	0	3.3V	0
S0	1.5V	3.3V	1.5V
S3	0	0	1.5V
S0	1.5V	3.3V	1.5V
S5	0	3.3V	0

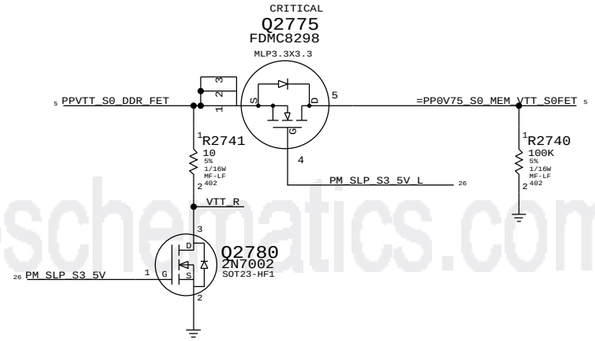
BUFFER ISOLATE_CPU_MEM_L TO 5V





MEM RESET ISOLATION





SYNC_MASTER=MATT SYNC_DATE=01/06/2010

PAGE TITLE: DDR3 RESET

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

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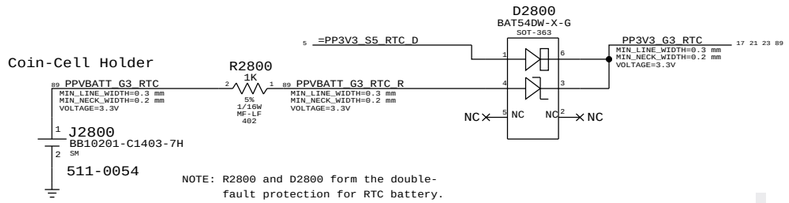
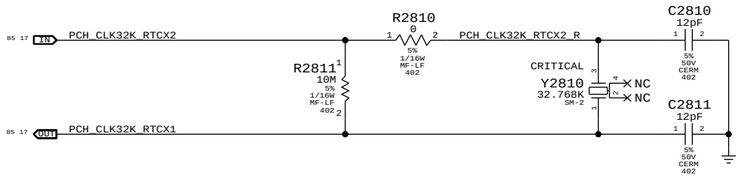
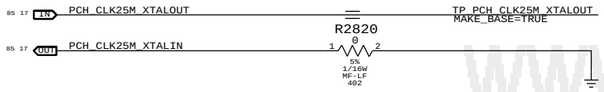
RTC Power Sources



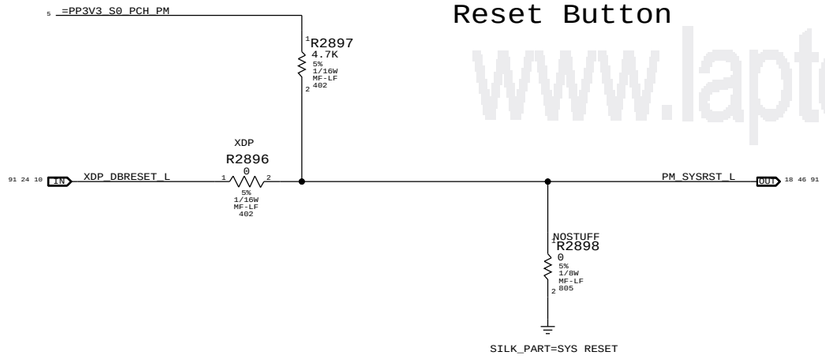
PCH RTC Crystal



UNUSED PCH 25MHZ CRYSTAL

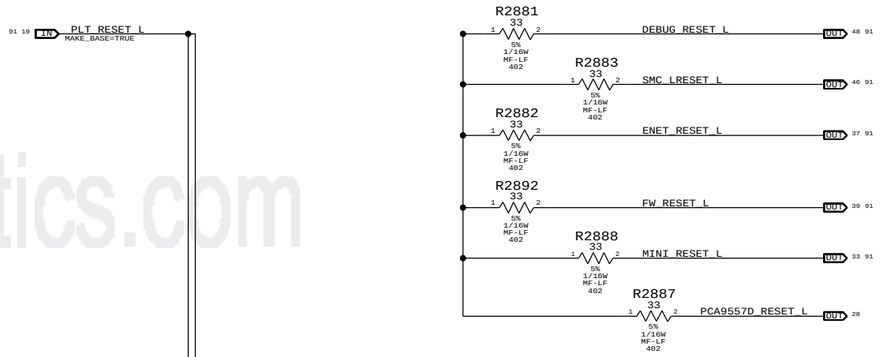


Reset Button

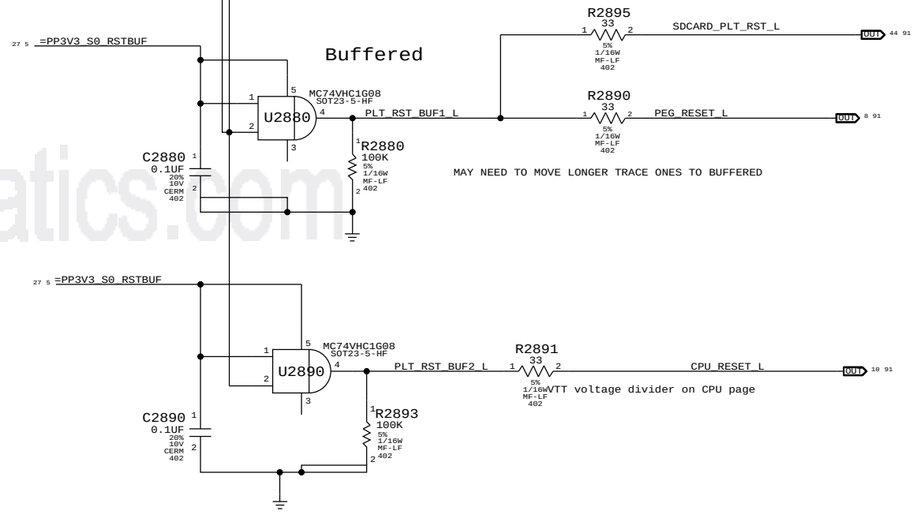


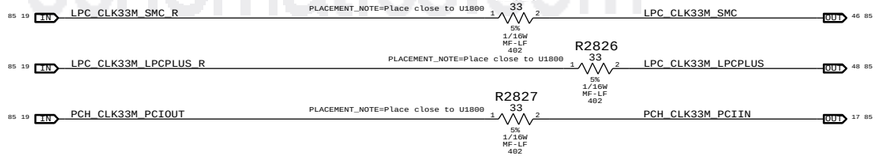
Platform Reset Connections

Unbuffered



Buffered





SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: CHIPSET SUPPORT

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

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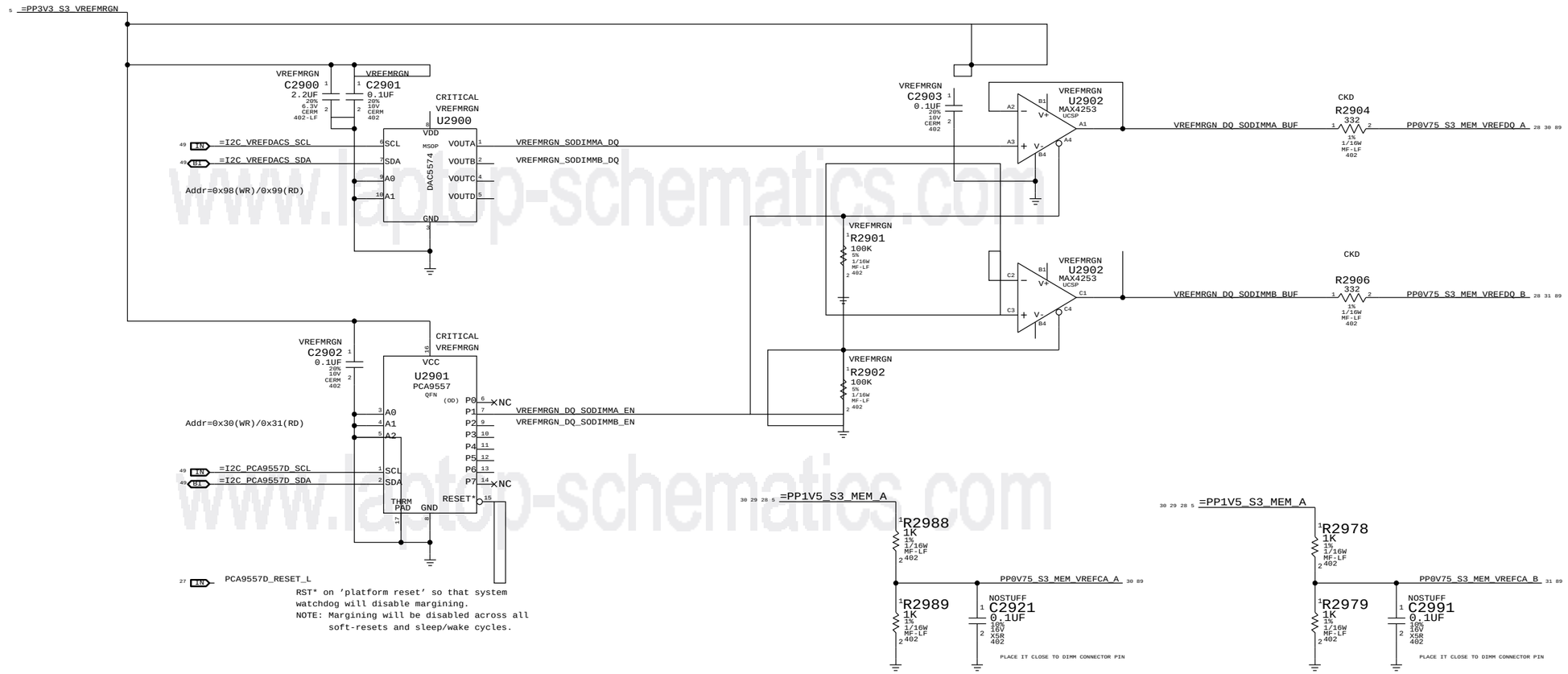
Page Notes

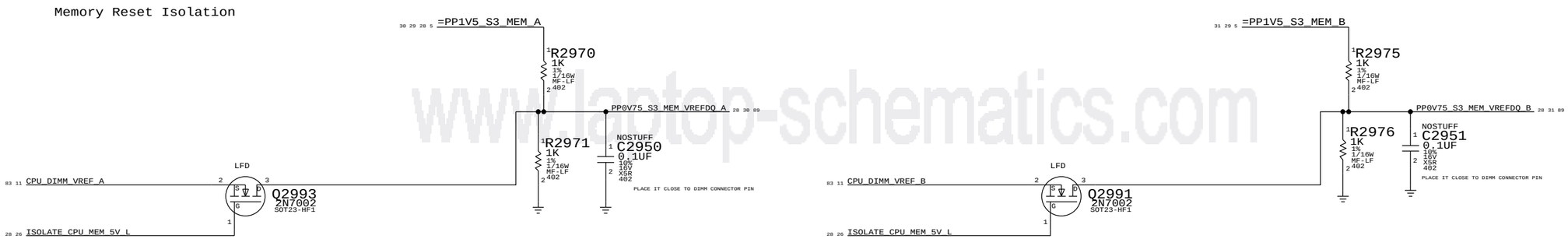
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.



Memory Reset Isolation



	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=MATT SYNC_DATE=01/06/2010

PAGE TITLE: DDR3 Vref Margining

Apple Inc.

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DIMM A (FURTHER FROM CPU) CAPS TO COUPLE CPU 1V5_MEM DIMM B (CLOSER TO CPU)

29 15 12 10 5 =PP1V5_CPU_MEM

C3016 1UF 10% 6.3V CERM 402
C3017 1UF 10% 6.3V CERM 402
C3018 1UF 10% 6.3V CERM 402
C3019 1UF 10% 6.3V CERM 402
C3010 1UF 10% 6.3V CERM 402
C3025 1UF 10% 6.3V CERM 402
C3026 1UF 10% 6.3V CERM 402
C3027 1UF 10% 6.3V CERM 402
C3028 1UF 10% 6.3V CERM 402
C3029 1UF 10% 6.3V CERM 402
C3020 1UF 10% 6.3V CERM 402
C3021 1UF 10% 6.3V CERM 402
C3022 1UF 10% 6.3V CERM 402
C3023 1UF 10% 6.3V CERM 402
C3014 1UF 10% 6.3V CERM 402
C3030 1UF 10% 6.3V CERM 402
C3031 1UF 10% 6.3V CERM 402
C3032 1UF 10% 6.3V CERM 402
C3033 1UF 10% 6.3V CERM 402

EXTRA DECOUPLING CAPS FOR CPU MEM RAIL

29 15 12 10 5 =PP1V5_CPU_MEM

C3041 1UF 10% 6.3V CERM 402
C3042 1UF 10% 6.3V CERM 402
C3044 1UF 10% 6.3V CERM 402
C3046 1UF 10% 6.3V CERM 402
C3040 1UF 10% 6.3V CERM 402
C3043 1UF 10% 6.3V CERM 402
C3045 1UF 10% 6.3V CERM 402
C3047 1UF 10% 6.3V CERM 402
C3048 1UF 10% 6.3V CERM 402
C3049 1UF 10% 6.3V CERM 402
C3090 1UF 10% 6.3V CERM 402
C3091 1UF 10% 6.3V CERM 402
C3092 1UF 10% 6.3V CERM 402
C3093 1UF 10% 6.3V CERM 402
C3094 1UF 10% 6.3V CERM 402

29 15 12 10 5 =PP1V5_CPU_MEM

C30A0 1UF 10% 6.3V CERM 402
C30A1 1UF 10% 6.3V CERM 402
C30A2 1UF 10% 6.3V CERM 402
C30A3 1UF 10% 6.3V CERM 402
C30A4 1UF 10% 6.3V CERM 402
C30A5 1UF 10% 6.3V CERM 402
C30A6 1UF 10% 6.3V CERM 402
C30A7 1UF 10% 6.3V CERM 402
C30A8 1UF 10% 6.3V CERM 402
C30A9 1UF 10% 6.3V CERM 402
C30AA 1UF 10% 6.3V CERM 402
C30AB 1UF 10% 6.3V CERM 402
C30AC 1UF 10% 6.3V CERM 402
C30AD 1UF 10% 6.3V CERM 402
C30AE 1UF 10% 6.3V CERM 402

DECOUPLING CAPS FOR DIMM ON CHANNEL A - AT CONNECTOR

30 28 5 =PP1V5_S3_MEM_A

C3050 10UF 20% 6.3V XSR 603
C3051 10UF 20% 6.3V XSR 603
C3052 1UF 10% 6.3V CERM 402
C3053 1UF 10% 6.3V CERM 402
C3054 1UF 10% 6.3V CERM 402
C3055 1UF 10% 6.3V CERM 402
C3056 1UF 10% 6.3V CERM 402
C3057 1UF 10% 6.3V CERM 402
C3058 1UF 10% 6.3V CERM 402
C3059 1UF 10% 6.3V CERM 402
C3060 1UF 10% 6.3V CERM 402
C3061 1UF 10% 6.3V CERM 402
C3062 1UF 10% 6.3V CERM 402
C3063 1UF 10% 6.3V CERM 402
C3064 1UF 10% 6.3V CERM 402
C3065 1UF 10% 6.3V CERM 402
C3066 1UF 10% 6.3V CERM 402
C3067 1UF 10% 6.3V CERM 402
C3068 1UF 10% 6.3V CERM 402
C3069 1UF 10% 6.3V CERM 402

DECOUPLING CAPS FOR DIMM ON CHANNEL B - AT CONNECTOR

31 28 5 =PP1V5_S3_MEM_B

C3070 10UF 20% 6.3V XSR 603
C3071 10UF 20% 6.3V XSR 603
C3072 1UF 10% 6.3V CERM 402
C3073 1UF 10% 6.3V CERM 402
C3074 1UF 10% 6.3V CERM 402
C3075 1UF 10% 6.3V CERM 402
C3076 1UF 10% 6.3V CERM 402
C3077 1UF 10% 6.3V CERM 402
C3078 1UF 10% 6.3V CERM 402
C3079 1UF 10% 6.3V CERM 402
C3080 1UF 10% 6.3V CERM 402
C3081 1UF 10% 6.3V CERM 402
C3082 1UF 10% 6.3V CERM 402
C3083 1UF 10% 6.3V CERM 402
C3084 1UF 10% 6.3V CERM 402
C3085 1UF 10% 6.3V CERM 402
C3086 1UF 10% 6.3V CERM 402
C3087 1UF 10% 6.3V CERM 402
C3088 1UF 10% 6.3V CERM 402
C3089 1UF 10% 6.3V CERM 402

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: MEMORY CAPS

Apple Inc.

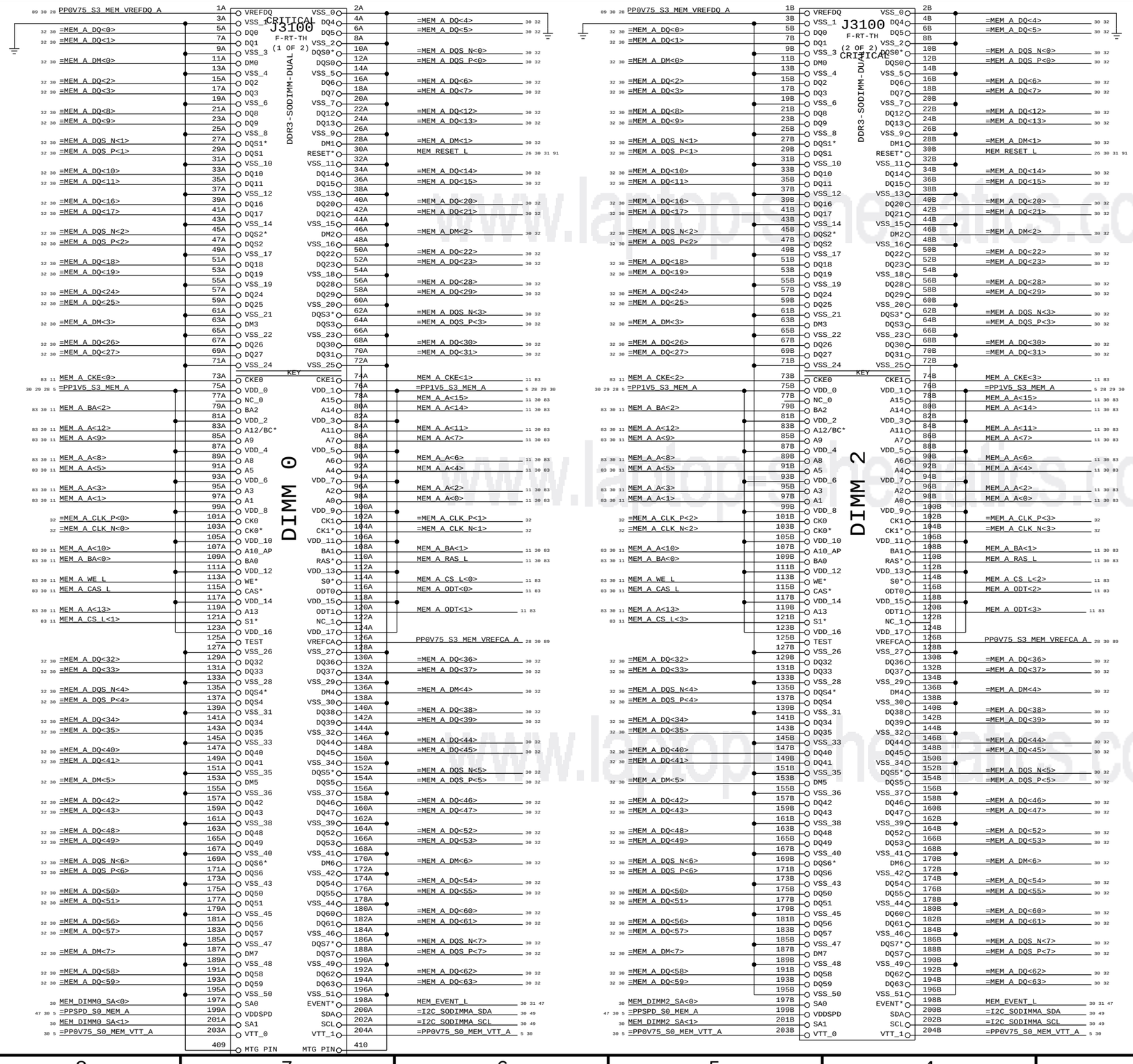
DRAWING NUMBER: 051-8337 SIZE: D

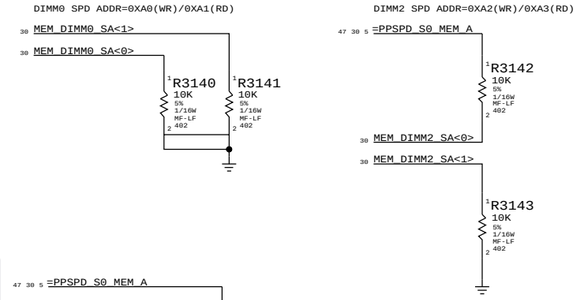
REVISION: A.0.0

BRANCH:

PAGE: 30 OF 110

SHEET: 29 OF 92





Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

ALL DQ, DQS, DM SIGNALS: TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page:
(NONE)

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: DDR3 SO-DIMMs 0 & 2

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 31 OF 110
SHEET: 30 OF 92

DIMM 1

J3200 CRITICAL F-RT-TH (1 OF 2) — DDR3-SODIMM-DUAL

89 31 28	PP0V75_S3_MEM_VREFDQ_B	1A	VREFDQ	VSS_0	2A		
		3A	VSS_1	DQ4	4A	=MEM_B_DQ<4>	31 32
32 31	=MEM_B_DQ<0>	5A	DQ0	DQ5	6A	=MEM_B_DQ<5>	31 32
32 31	=MEM_B_DQ<1>	7A	DQ1	VSS_2	8A		
		9A	VSS_3	DQS0*	10A	=MEM_B_DQS_N<0>	31 32
32 31	=MEM_B_DM<0>	11A	DM0	DQS0	12A	=MEM_B_DQS_P<0>	31 32
		13A	VSS_4	VSS_5	14A		
32 31	=MEM_B_DQ<2>	15A	DQ2	DQ6	16A	=MEM_B_DQ<6>	31 32
32 31	=MEM_B_DQ<3>	17A	DQ3	DQ7	18A	=MEM_B_DQ<7>	31 32
		19A	VSS_6	VSS_7	20A		
32 31	=MEM_B_DQ<8>	21A	DQ8	DQ12	22A	=MEM_B_DQ<12>	31 32
32 31	=MEM_B_DQ<9>	23A	DQ9	DQ13	24A	=MEM_B_DQ<13>	31 32
		25A	VSS_8	VSS_9	26A		
32 31	=MEM_B_DQS_N<1>	27A	DQS1*	DM1	28A	=MEM_B_DM<1>	31 32
32 31	=MEM_B_DQS_P<1>	29A	DQS1	RESET*	30A	MEM_RESET_L	26 30 31 91
		31A	VSS_10	VSS_11	32A		
32 31	=MEM_B_DQ<10>	33A	DQ10	DQ14	34A	=MEM_B_DQ<14>	31 32
32 31	=MEM_B_DQ<11>	35A	DQ11	DQ15	36A	=MEM_B_DQ<15>	31 32
		37A	VSS_12	VSS_13	38A		
32 31	=MEM_B_DQ<16>	39A	DQ16	DQ20	40A	=MEM_B_DQ<20>	31 32
32 31	=MEM_B_DQ<17>	41A	DQ17	DQ21	42A	=MEM_B_DQ<21>	31 32
		43A	VSS_14	VSS_15	44A		
32 31	=MEM_B_DQS_N<2>	45A	DQS2*	DM2	46A	=MEM_B_DM<2>	31 32
32 31	=MEM_B_DQS_P<2>	47A	DQS2	VSS_16	48A		
		49A	VSS_17	DQ22	50A	=MEM_B_DQ<22>	31 32
32 31	=MEM_B_DQ<18>	51A	DQ18	DQ23	52A	=MEM_B_DQ<23>	31 32
32 31	=MEM_B_DQ<19>	53A	DQ19	VSS_18	54A		
		55A	VSS_19	DQ28	56A	=MEM_B_DQ<28>	31 32
32 31	=MEM_B_DQ<24>	57A	DQ24	DQ29	58A	=MEM_B_DQ<29>	31 32
32 31	=MEM_B_DQ<25>	59A	DQ25	VSS_20	60A		
		61A	VSS_21	DQS3*	62A	=MEM_B_DQS_N<3>	31 32
32 31	=MEM_B_DM<3>	63A	DM3	DQS3	64A	=MEM_B_DQS_P<3>	31 32
		65A	VSS_22	VSS_23	66A		
32 31	=MEM_B_DQ<26>	67A	DQ26	DQ30	68A	=MEM_B_DQ<30>	31 32
32 31	=MEM_B_DQ<27>	69A	DQ27	DQ31	70A	=MEM_B_DQ<31>	31 32
		71A	VSS_24	VSS_25	72A		
	KEY						
83 11	MEM_B_CKE<0>	73A	CKE0	CKE1	74A	MEM_B_CKE<1>	11 83
31 29 28 5	=PP1V5_S3_MEM_B	75A	VDD_0	VDD_1	76A	=PP1V5_S3_MEM_B	5 28 29 31
		77A	NC_0	A15	78A	MEM_B_A<15>	11 31 83
83 31 11	MEM_B_BA<2>	79A	BA2	A14	80A	MEM_B_A<14>	11 31 83
		81A	VDD_2	VDD_3	82A		
83 31 11	MEM_B_A<12>	83A	A12/BC*	A11	84A	MEM_B_A<11>	11 31 83
83 31 11	MEM_B_A<9>	85A	A9	A7	86A	MEM_B_A<7>	11 31 83
		87A	VDD_4	VDD_5	88A		
83 31 11	MEM_B_A<8>	89A	A8	A6	90A	MEM_B_A<6>	11 31 83
83 31 11	MEM_B_A<5>	91A	A5	A4	92A	MEM_B_A<4>	11 31 83
		93A	VDD_6	VDD_7	94A		
83 31 11	MEM_B_A<3>	95A	A3	A2	96A	MEM_B_A<2>	11 31 83
83 31 11	MEM_B_A<1>	97A	A1	A0	98A	MEM_B_A<0>	11 31 83
		99A	VDD_8	VDD_9	100A		
32	=MEM_B_CLK_P<0>	101A	CK0	CK1	102A	=MEM_B_CLK_P<1>	32
32	=MEM_B_CLK_N<0>	103A	CK0*	CK1*	104A	=MEM_B_CLK_N<1>	32
		105A	VDD_10	VDD_11	106A		
83 31 11	MEM_B_A<10>	107A	A10_AP	BA1	108A	MEM_B_BA<1>	11 31 83
83 31 11	MEM_B_BA<0>	109A	BA0	RAS*	110A	MEM_B_RAS_L	11 31 83
		111A	VDD_12	VDD_13	112A		
83 31 11	MEM_B_WE_L	113A	WE*	S0*	114A	MEM_B_CS_L<0>	11 83
83 31 11	MEM_B_CAS_L	115A	CAS*	ODT0	116A	MEM_B_ODT<0>	11 83
		117A	VDD_14	VDD_15	118A		
83 31 11	MEM_B_A<13>	119A	A13	ODT1	120A	MEM_B_ODT<1>	11 83
83 11	MEM_B_CS_L<1>	121A	S1*	NC_1	122A		
		123A	VDD_16	VDD_17	124A		
		125A	TEST	VREFCA	126A	PP0V75_S3_MEM_VREFCA_B	28 31 89
		127A	VSS_26	VSS_27	128A		
32 31	=MEM_B_DQ<32>	129A	DQ32	DQ36	130A	=MEM_B_DQ<36>	31 32
32 31	=MEM_B_DQ<33>	131A	DQ33	DQ37	132A	=MEM_B_DQ<37>	31 32
		133A	VSS_28	VSS_29	134A		
32 31	=MEM_B_DQS_N<4>	135A	DQS4*	DM4	136A	=MEM_B_DM<4>	31 32
32 31	=MEM_B_DQS_P<4>	137A	DQS4	VSS_30	138A		
		139A	VSS_31	DQ38	140A	=MEM_B_DQ<38>	31 32
32 31	=MEM_B_DQ<34>	141A	DQ34	DQ39	142A	=MEM_B_DQ<39>	31 32
32 31	=MEM_B_DQ<35>	143A	DQ35	VSS_32	144A		
		145A	VSS_33	DQ44	146A	=MEM_B_DQ<44>	31 32
32 31	=MEM_B_DQ<40>	147A	DQ40	DQ45	148A	=MEM_B_DQ<45>	31 32
32 31	=MEM_B_DQ<41>	149A	DQ41	VSS_34	150A		
		151A	VSS_35	DQS5*	152A	=MEM_B_DQS_N<5>	31 32
32 31	=MEM_B_DM<5>	153A	DM5	DQS5	154A	=MEM_B_DQS_P<5>	31 32
		155A	VSS_36	VSS_37	156A		
32 31	=MEM_B_DQ<42>	157A	DQ42	DQ46	158A	=MEM_B_DQ<46>	31 32
32 31	=MEM_B_DQ<43>	159A	DQ43	DQ47	160A	=MEM_B_DQ<47>	31 32
		161A	VSS_38	VSS_39	162A		
32 31	=MEM_B_DQ<48>	163A	DQ48	DQ52	164A	=MEM_B_DQ<52>	31 32
32 31	=MEM_B_DQ<49>	165A	DQ49	DQ53	166A	=MEM_B_DQ<53>	31 32
		167A	VSS_40	VSS_41	168A		
32 31	=MEM_B_DQS_N<6>	169A	DQS6*	DM6	170A	=MEM_B_DM<6>	31 32
32 31	=MEM_B_DQS_P<6>	171A	DQS6	VSS_42	172A		
		173A	VSS_43	DQ54	174A	=MEM_B_DQ<54>	31 32
32 31	=MEM_B_DQ<50>	175A	DQ50	DQ55	176A	=MEM_B_DQ<55>	31 32
32 31	=MEM_B_DQ<51>	177A	DQ51	VSS_44	178A		
		179A	VSS_45	DQ60	180A	=MEM_B_DQ<60>	31 32
32 31	=MEM_B_DQ<56>	181A	DQ56	DQ61	182A	=MEM_B_DQ<61>	31 32
32 31	=MEM_B_DQ<57>	183A	DQ57	VSS_46	184A		
		185A	VSS_47	DQS7*	186A	=MEM_B_DQS_N<7>	31 32
32 31	=MEM_B_DM<7>	187A	DM7	DQS7	188A	=MEM_B_DQS_P<7>	31 32
		189A	VSS_48	VSS_49	190A		
32 31	=MEM_B_DQ<58>	191A	DQ58	DQ62	192A	=MEM_B_DQ<62>	31 32
32 31	=MEM_B_DQ<59>	193A	DQ59	DQ63	194A	=MEM_B_DQ<63>	31 32
		195A	VSS_50	VSS_51	196A		
31	MEM_DIMM1_SA<0>	197A	SA0	EVENT*	198A	MEM_EVENT_L	30 31 47
31 5	=PPSPD_S0_MEM_B	199A	VDDSPD	SDA	200A	=I2C_SODIMMB_SDA	31 49
31	MEM_DIMM1_SA<1>	201A	SA1	SCL	202A	=I2C_SODIMMB_SCL	31 49
31 5	=PP0V75_S0_MEM_VTT_B	203A	VTT_0	VTT_1	204A	=PP0V75_S0_MEM_VTT_B	5 31
		409	MTG PIN	MTG PIN	410		

DIMM 3

J3200 CRITICAL F-RT-TH (2 OF 2) — DDR3-SODIMM-DUAL

89 31 28	PP0V75_S3_MEM_VREFDQ_B	1B	VREFDQ	VSS_0	2B		
		3B	VSS_1	DQ4	4B	=MEM_B_DQ<4>	31 32
32 31	=MEM_B_DQ<0>	5B	DQ0	DQ5	6B	=MEM_B_DQ<5>	31 32
32 31	=MEM_B_DQ<1>	7B	DQ1	VSS_2	8B		
		9B	VSS_3	DQS0*	10B	=MEM_B_DQS_N<0>	31 32
32 31	=MEM_B_DM<0>	11B	DM0	DQS0	12B	=MEM_B_DQS_P<0>	31 32
		13B	VSS_4	VSS_5	14B		
32 31	=MEM_B_DQ<2>	15B	DQ2	DQ6	16B	=MEM_B_DQ<6>	31 32
32 31	=MEM_B_DQ<3>	17B	DQ3	DQ7	18B	=MEM_B_DQ<7>	31 32
		19B	VSS_6	VSS_7	20B		
32 31	=MEM_B_DQ<8>	21B	DQ8	DQ12	22B	=MEM_B_DQ<12>	31 32
32 31	=MEM_B_DQ<9>	23B	DQ9	DQ13	24B	=MEM_B_DQ<13>	31 32
		25B	VSS_8	VSS_9	26B		
32 31	=MEM_B_DQS_N<1>	27B	DQS1*	DM1	28B	=MEM_B_DM<1>	31 32
32 31	=MEM_B_DQS_P<1>	29B	DQS1	RESET*	30B	MEM_RESET_L	26 30 31 91
		31B	VSS_10	VSS_11	32B		
32 31	=MEM_B_DQ<10>	33B	DQ10	DQ14	34B	=MEM_B_DQ<14>	31 32
32 31	=MEM_B_DQ<11>	35B	DQ11	DQ15	36B	=MEM_B_DQ<15>	31 32
		37B	VSS_12	VSS_13	38B		
32 31	=MEM_B_DQ<16>	39B	DQ16	DQ20	40B	=MEM_B_DQ<20>	31 32
32 31	=MEM_B_DQ<17>	41B	DQ17	DQ21	42B	=MEM_B_DQ<21>	31 32
		43B	VSS_14	VSS_15	44B		
32 31	=MEM_B_DQS_N<2>	45B	DQS2*	DM2	46B	=MEM_B_DM<2>	31 32
32 31	=MEM_B_DQS_P<2>	47B	DQS2	VSS_16	48B		
		49B	VSS_17	DQ22	50B	=MEM_B_DQ<22>	31 32
32 31	=MEM_B_DQ<18>	51B	DQ18	DQ23	52B	=MEM_B_DQ<23>	31 32
32 31	=MEM_B_DQ<19>	53B	DQ19	VSS_18	54B		
		55B	VSS_19	DQ28	56B	=MEM_B_DQ<28>	31 32
32 31	=MEM_B_DQ<24>	57B	DQ24	DQ29	58B	=MEM_B_DQ<29>	31 32
32 31	=MEM_B_DQ<25>	59B	DQ25	VSS_20	60B		
		61B	VSS_21	DQS3*	62B	=MEM_B_DQS_N<3>	31 32
32 31	=MEM_B_DM<3>	63B	DM3	DQS3	64B	=MEM_B_DQS_P<3>	31 32
		65B	VSS_22	VSS_23	66B		
32 31	=MEM_B_DQ<26>	67B	DQ26	DQ30	68B	=MEM_B_DQ<30>	31 32
32 31	=MEM_B_DQ<27>	69B	DQ27	DQ31	70B	=MEM_B_DQ<31>	31 32
		71B	VSS_24	VSS_25	72B		
	KEY						
83 11	MEM_B_CKE<2>	73B	CKE0	CKE1	74B	MEM_B_CKE<3>	11 83
31 29 28 5	=PP1V5_S3_MEM_B	75B	VDD_0	VDD_1	76B	=PP1V5_S3_MEM_B	5 28 29 31
		77B	NC_0	A15	78B	MEM_B_A<15>	11 31 83
83 31 11	MEM_B_BA<2>	79B	BA2	A14	80B	MEM_B_A<14>	11 31 83
		81B	VDD_2	VDD_3	82B		
83 31 11	MEM_B_A<12>	83B	A12/BC*	A11	84B	MEM_B_A<11>	11 31 83
83 31 11	MEM_B_A<9>	85B	A9	A7	86B	MEM_B_A<7>	11 31 83
		87B	VDD_4	VDD_5	88B		
83 31 11	MEM_B_A<8>	89B	A8	A6	90B	MEM_B_A<6>	11 31 83
83 31 11	MEM_B_A<5>	91B	A5	A4	92B	MEM_B_A<4>	11 31 83
		93B	VDD_6	VDD_7	94B		
83 31 11	MEM_B_A<3>	95B	A3	A2	96B	MEM_B_A<2>	11 31 83
83 31 11	MEM_B_A<1>	97B	A1	A0	98B	MEM_B_A<0>	11 31 83
		99B	VDD_8	VDD_9	100B		
32	=MEM_B_CLK_P<2>	101B	CK0	CK1	102B	=MEM_B_CLK_P<3>	32
32	=MEM_B_CLK_N<2>	103B	CK0*	CK1*	104B	=MEM_B_CLK_N<3>	32
		105B	VDD_10	VDD_11	106B		
83 31 11	MEM_B_A<10>	107B	A10_AP	BA1	108B	MEM_B_BA<1>	11 31 83
83 31 11	MEM_B_BA<0>	109B	BA0	RAS*	110B	MEM_B_RAS_L	11 31 83
		111B	VDD_12	VDD_13	112B		
83 31 11	MEM_B_WE_L	113B	WE*	S0*	114B	MEM_B_CS_L<2>	11 83
83 31 11	MEM_B_CAS_L	115B	CAS*	ODT0	116B	MEM_B_ODT<2>	11 83
		117B	VDD_14	VDD_15	118B		
83 31 11	MEM_B_A<13>	119B	A13	ODT1	120B	MEM_B_ODT<3>	11 83
83 11	MEM_B_CS_L<3>	121B	S1*	NC_1	122B		
		123B	VDD_16	VDD_17	124B		
		125B	TEST	VREFCA	126B	PP0V75_S3_MEM_VREFCA_B	28 31 89
		127B	VSS_26	VSS_27	128B		
32 31	=MEM_B_DQ<32>	129B	DQ32	DQ36	130B	=MEM_B_DQ<36>	31 32
32 31	=MEM_B_DQ<33>	131B	DQ33	DQ37	132B	=MEM_B_DQ<37>	31 32
		133B	VSS_28	VSS_29	134B		
32 31	=MEM_B_DQS_N<4>	135B	DQS4*	DM4	136B	=MEM_B_DM<4>	31 32
32 31	=MEM_B_DQS_P<4>	137B	DQS4	VSS_30	138B		
		139B	VSS_31	DQ38	140B	=MEM_B_DQ<38>	31 32
32 31	=MEM_B_DQ<34>	141B	DQ34	DQ39	142B	=MEM_B_DQ<39>	31 32
32 31	=MEM_B_DQ<35>	143B	DQ35	VSS_32	144B		
		145B	VSS_33	DQ44	146B	=MEM_B_DQ<44>	31 32
32 31	=MEM_B_DQ<40>	147B	DQ40	DQ45	148B	=MEM_B_DQ<45>	31 32
32 31	=MEM_B_DQ<41>	149B	DQ41	VSS_34	150B		
		151B	VSS_35	DQS5*	152B	=MEM_B_DQS_N<5>	31 32
32 31	=MEM_B_DM<5>	153B	DM5	DQS5	154B	=MEM_B_DQS_P<5>	31 32
		155B	VSS_36	VSS_37	156B		
32 31	=MEM_B_DQ<42>	157B	DQ42	DQ46	158B	=MEM_B_DQ<46>	31 32
32 31	=MEM_B_DQ<43>	159B	DQ43	DQ47	160B	=MEM_B_DQ<47>	31 32
		161B	VSS_38	VSS_39	162B		
32 31	=MEM_B_DQ<48>	163B	DQ48	DQ52	164B	=MEM_B_DQ<52>	31 32
32 31	=MEM_B_DQ<49>	165B	DQ49	DQ53	166B	=MEM_B_DQ<53>	31 32
		167B	VSS_40	VSS_41	168B		
32 31	=MEM_B_DQS_N<6>	169B	DQS6*	DM6	170B	=MEM_B_DM<6>	31 32
32 31	=MEM_B_DQS_P<6>	171B	DQS6	VSS_42	172B		
		173B	VSS_43	DQ54	174B	=MEM_B_DQ<54>	31 32
32 31	=MEM_B_DQ<50>	175B	DQ50	DQ55	176B	=MEM_B_DQ<55>	31 32
32 31	=MEM_B_DQ<51>	177B	DQ51	VSS_44	178B		
		179B	VSS_45	DQ60	180B	=MEM_B_DQ<60>	31 32
32 31	=MEM_B_DQ<56>	181B	DQ56	DQ61	182B	=MEM_B_DQ<61>	31 32
32 31	=MEM_B_DQ<57>	183B	DQ57	VSS_46	184B		
		185B	VSS_47	DQS7*	186B	=MEM_B_DQS_N<7>	31 32
32 31	=MEM_B_DM<7>	187B	DM7	DQS7	188B	=MEM_B_DQS_P<7>	31 32
		189B	VSS_48	VSS_49	190B		
32 31	=MEM_B_DQ<58>	191B	DQ58	DQ62	192B	=MEM_B_DQ<62>	31 32
32 31	=MEM_B_DQ<59>	193B	DQ59	DQ63	194B	=MEM_B_DQ<63>	31 32
		195B	VSS_50	VSS_51	196B		
31	MEM_DIMM3_SA<0>	197B	SA0	EVENT*	198B	MEM_EVENT_L	30 31 47
31 5	=PPSPD_S0_MEM_B	199B	VDDSPD	SDA	200B	=I2C_SODIMMB_SDA	31 49
31	MEM_DIMM3_SA<1>	201B	SA1	SCL	202B	=I2C_SODIMMB_SCL	31 49
31 5	=PP0V75_S0_MEM_VTT_B	203B	VTT_0	VTT_1	204B	=PP0V75_S0_MEM_VTT_B	5 31

DIMM1 SPD ADDR=0XA4(WR)/0XA5(RD)

31 5 =PPSPD_S0_MEM_B

R3240 10K 5% 1/16W MF-LF 402

31 MEM_DIMM1_SA<1>

31 MEM_DIMM1_SA<0>

R3241 10K 5% 1/16W MF-LF 402

DIMM3 SPD ADDR=0XA6(WR)/0XA7(RD)

31 5 =PPSPD_S0_MEM_B

R3242 10K 5% 1/16W MF-LF 402

R3243 10K 5% 1/16W MF-LF 402

31 MEM_DIMM3_SA<1>

31 MEM_DIMM3_SA<0>

31 5 =PPSPD_S0_MEM_B

C3240 2.2UF 20% 6.3V CERM 402-LF

89 31 28 PP0V75_S3_MEM_VREFCA_B

C3235 2.2UF 20% 6.3V CERM 402-LF

C3236 0.1UF 20% 10V CERM 402

89 31 28 PP0V75_S3_MEM_VREFDQ_B

C3230 2.2UF 20% 6.3V CERM 402-LF

C3231 0.1UF 20% 10V CERM 402

31 5 =PP0V75_S0_MEM_VTT_B

C3250 2.2UF 20% 6.3V CERM 402-LF

C3251 2.2UF 20% 6.3V CERM 402-LF

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA
- ALL DQ, DQS, DM SIGNALS: TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page:
(NONE)

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: DDR3 SO-DIMM CONNECTOR B

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

BRANCH:

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CPU CHANNEL A DQS 0 -> DIMM A DQS 7

MEM_A_DQS_N<0>	MAKE_BASE=TRUE		=MEM_A_DQS_N<7>		
MEM_A_DQS_P<0>	MAKE_BASE=TRUE		=MEM_A_DQS_P<7>		
MEM_A_DM<0>	MAKE_BASE=TRUE		=MEM_A_DM<7>		
MEM_A_DQ<7>	MAKE_BASE=TRUE		=MEM_A_DQ<60>		
MEM_A_DQ<6>	MAKE_BASE=TRUE		=MEM_A_DQ<56>		
MEM_A_DQ<5>	MAKE_BASE=TRUE		=MEM_A_DQ<58>		
MEM_A_DQ<4>	MAKE_BASE=TRUE		=MEM_A_DQ<59>		
MEM_A_DQ<3>	MAKE_BASE=TRUE		=MEM_A_DQ<57>		
MEM_A_DQ<2>	MAKE_BASE=TRUE		=MEM_A_DQ<61>		
MEM_A_DQ<1>	MAKE_BASE=TRUE		=MEM_A_DQ<62>		
MEM_A_DQ<0>	MAKE_BASE=TRUE		=MEM_A_DQ<63>		

CPU CHANNEL A DQS 1 -> DIMM A DQS 6

MEM_A_DQS_N<1>	MAKE_BASE=TRUE		=MEM_A_DQS_N<6>		
MEM_A_DQS_P<1>	MAKE_BASE=TRUE		=MEM_A_DQS_P<6>		
MEM_A_DM<1>	MAKE_BASE=TRUE		=MEM_A_DM<6>		
MEM_A_DQ<15>	MAKE_BASE=TRUE		=MEM_A_DQ<49>		
MEM_A_DQ<14>	MAKE_BASE=TRUE		=MEM_A_DQ<52>		
MEM_A_DQ<13>	MAKE_BASE=TRUE		=MEM_A_DQ<51>		
MEM_A_DQ<12>	MAKE_BASE=TRUE		=MEM_A_DQ<50>		
MEM_A_DQ<11>	MAKE_BASE=TRUE		=MEM_A_DQ<48>		
MEM_A_DQ<10>	MAKE_BASE=TRUE		=MEM_A_DQ<53>		
MEM_A_DQ<9>	MAKE_BASE=TRUE		=MEM_A_DQ<55>		
MEM_A_DQ<8>	MAKE_BASE=TRUE		=MEM_A_DQ<54>		

CPU CHANNEL A DQS 2 -> DIMM A DQS 5

MEM_A_DQS_N<2>	MAKE_BASE=TRUE		=MEM_A_DQS_N<5>		
MEM_A_DQS_P<2>	MAKE_BASE=TRUE		=MEM_A_DQS_P<5>		
MEM_A_DM<2>	MAKE_BASE=TRUE		=MEM_A_DM<5>		
MEM_A_DQ<23>	MAKE_BASE=TRUE		=MEM_A_DQ<40>		
MEM_A_DQ<22>	MAKE_BASE=TRUE		=MEM_A_DQ<45>		
MEM_A_DQ<21>	MAKE_BASE=TRUE		=MEM_A_DQ<43>		
MEM_A_DQ<20>	MAKE_BASE=TRUE		=MEM_A_DQ<42>		
MEM_A_DQ<19>	MAKE_BASE=TRUE		=MEM_A_DQ<41>		
MEM_A_DQ<18>	MAKE_BASE=TRUE		=MEM_A_DQ<44>		
MEM_A_DQ<17>	MAKE_BASE=TRUE		=MEM_A_DQ<46>		
MEM_A_DQ<16>	MAKE_BASE=TRUE		=MEM_A_DQ<47>		

CPU CHANNEL A DQS 3 -> DIMM A DQS 4

MEM_A_DQS_N<3>	MAKE_BASE=TRUE		=MEM_A_DQS_N<4>		
MEM_A_DQS_P<3>	MAKE_BASE=TRUE		=MEM_A_DQS_P<4>		
MEM_A_DM<3>	MAKE_BASE=TRUE		=MEM_A_DM<4>		
MEM_A_DQ<31>	MAKE_BASE=TRUE		=MEM_A_DQ<37>		
MEM_A_DQ<30>	MAKE_BASE=TRUE		=MEM_A_DQ<33>		
MEM_A_DQ<29>	MAKE_BASE=TRUE		=MEM_A_DQ<35>		
MEM_A_DQ<28>	MAKE_BASE=TRUE		=MEM_A_DQ<34>		
MEM_A_DQ<27>	MAKE_BASE=TRUE		=MEM_A_DQ<36>		
MEM_A_DQ<26>	MAKE_BASE=TRUE		=MEM_A_DQ<32>		
MEM_A_DQ<25>	MAKE_BASE=TRUE		=MEM_A_DQ<38>		
MEM_A_DQ<24>	MAKE_BASE=TRUE		=MEM_A_DQ<39>		

CPU CHANNEL A DQS 4 -> DIMM A DQS 3

MEM_A_DQS_N<4>	MAKE_BASE=TRUE		=MEM_A_DQS_N<3>		
MEM_A_DQS_P<4>	MAKE_BASE=TRUE		=MEM_A_DQS_P<3>		
MEM_A_DM<4>	MAKE_BASE=TRUE		=MEM_A_DM<3>		
MEM_A_DQ<39>	MAKE_BASE=TRUE		=MEM_A_DQ<25>		
MEM_A_DQ<38>	MAKE_BASE=TRUE		=MEM_A_DQ<29>		
MEM_A_DQ<37>	MAKE_BASE=TRUE		=MEM_A_DQ<27>		
MEM_A_DQ<36>	MAKE_BASE=TRUE		=MEM_A_DQ<31>		
MEM_A_DQ<35>	MAKE_BASE=TRUE		=MEM_A_DQ<28>		
MEM_A_DQ<34>	MAKE_BASE=TRUE		=MEM_A_DQ<24>		
MEM_A_DQ<33>	MAKE_BASE=TRUE		=MEM_A_DQ<26>		
MEM_A_DQ<32>	MAKE_BASE=TRUE		=MEM_A_DQ<30>		

CPU CHANNEL A DQS 5 -> DIMM A DQS 2

MEM_A_DQS_N<5>	MAKE_BASE=TRUE		=MEM_A_DQS_N<2>		
MEM_A_DQS_P<5>	MAKE_BASE=TRUE		=MEM_A_DQS_P<2>		
MEM_A_DM<5>	MAKE_BASE=TRUE		=MEM_A_DM<2>		
MEM_A_DQ<47>	MAKE_BASE=TRUE		=MEM_A_DQ<17>		
MEM_A_DQ<46>	MAKE_BASE=TRUE		=MEM_A_DQ<16>		
MEM_A_DQ<45>	MAKE_BASE=TRUE		=MEM_A_DQ<22>		
MEM_A_DQ<44>	MAKE_BASE=TRUE		=MEM_A_DQ<23>		
MEM_A_DQ<43>	MAKE_BASE=TRUE		=MEM_A_DQ<21>		
MEM_A_DQ<42>	MAKE_BASE=TRUE		=MEM_A_DQ<20>		
MEM_A_DQ<41>	MAKE_BASE=TRUE		=MEM_A_DQ<18>		
MEM_A_DQ<40>	MAKE_BASE=TRUE		=MEM_A_DQ<19>		

CPU CHANNEL A DQS 6 -> DIMM A DQS 1

MEM_A_DQS_N<6>	MAKE_BASE=TRUE		=MEM_A_DQS_N<1>		
MEM_A_DQS_P<6>	MAKE_BASE=TRUE		=MEM_A_DQS_P<1>		
MEM_A_DM<6>	MAKE_BASE=TRUE		=MEM_A_DM<1>		
MEM_A_DQ<55>	MAKE_BASE=TRUE		=MEM_A_DQ<12>		
MEM_A_DQ<54>	MAKE_BASE=TRUE		=MEM_A_DQ<13>		
MEM_A_DQ<53>	MAKE_BASE=TRUE		=MEM_A_DQ<10>		
MEM_A_DQ<52>	MAKE_BASE=TRUE		=MEM_A_DQ<15>		
MEM_A_DQ<51>	MAKE_BASE=TRUE		=MEM_A_DQ<8>		
MEM_A_DQ<50>	MAKE_BASE=TRUE		=MEM_A_DQ<9>		
MEM_A_DQ<49>	MAKE_BASE=TRUE		=MEM_A_DQ<11>		
MEM_A_DQ<48>	MAKE_BASE=TRUE		=MEM_A_DQ<14>		

CPU CHANNEL A DQS 7 -> DIMM A DQS 0

MEM_A_DQS_N<7>	MAKE_BASE=TRUE		=MEM_A_DQS_N<0>		
MEM_A_DQS_P<7>	MAKE_BASE=TRUE		=MEM_A_DQS_P<0>		
MEM_A_DM<7>	MAKE_BASE=TRUE		=MEM_A_DM<0>		
MEM_A_DQ<63>	MAKE_BASE=TRUE		=MEM_A_DQ<5>		
MEM_A_DQ<62>	MAKE_BASE=TRUE		=MEM_A_DQ<4>		
MEM_A_DQ<61>	MAKE_BASE=TRUE		=MEM_A_DQ<3>		
MEM_A_DQ<60>	MAKE_BASE=TRUE		=MEM_A_DQ<2>		
MEM_A_DQ<59>	MAKE_BASE=TRUE		=MEM_A_DQ<1>		
MEM_A_DQ<58>	MAKE_BASE=TRUE		=MEM_A_DQ<0>		
MEM_A_DQ<57>	MAKE_BASE=TRUE		=MEM_A_DQ<7>		
MEM_A_DQ<56>	MAKE_BASE=TRUE		=MEM_A_DQ<6>		

CPU CHANNEL B DQS 0 -> DIMM B DQS 7

MEM_B_DQS_N<0>	MAKE_BASE=TRUE		=MEM_B_DQS_N<7>		
MEM_B_DQS_P<0>	MAKE_BASE=TRUE		=MEM_B_DQS_P<7>		
MEM_B_DM<0>	MAKE_BASE=TRUE		=MEM_B_DM<7>		
MEM_B_DQ<7>	MAKE_BASE=TRUE		=MEM_B_DQ<61>		
MEM_B_DQ<6>	MAKE_BASE=TRUE		=MEM_B_DQ<60>		
MEM_B_DQ<5>	MAKE_BASE=TRUE		=MEM_B_DQ<62>		
MEM_B_DQ<4>	MAKE_BASE=TRUE		=MEM_B_DQ<63>		
MEM_B_DQ<3>	MAKE_BASE=TRUE		=MEM_B_DQ<56>		
MEM_B_DQ<2>	MAKE_BASE=TRUE		=MEM_B_DQ<57>		
MEM_B_DQ<1>	MAKE_BASE=TRUE		=MEM_B_DQ<58>		
MEM_B_DQ<0>	MAKE_BASE=TRUE		=MEM_B_DQ<59>		

CPU CHANNEL B DQS 1 -> DIMM B DQS 6

MEM_B_DQS_N<1>	MAKE_BASE=TRUE		=MEM_B_DQS_N<6>		
MEM_B_DQS_P<1>	MAKE_BASE=TRUE		=MEM_B_DQS_P<6>		
MEM_B_DM<1>	MAKE_BASE=TRUE		=MEM_B_DM<6>		
MEM_B_DQ<15>	MAKE_BASE=TRUE		=MEM_B_DQ<51>		
MEM_B_DQ<14>	MAKE_BASE=TRUE		=MEM_B_DQ<54>		
MEM_B_DQ<13>	MAKE_BASE=TRUE		=MEM_B_DQ<53>		
MEM_B_DQ<12>	MAKE_BASE=TRUE		=MEM_B_DQ<52>		
MEM_B_DQ<11>	MAKE_BASE=TRUE		=MEM_B_DQ<48>		
MEM_B_DQ<10>	MAKE_BASE=TRUE		=MEM_B_DQ<49>		
MEM_B_DQ<9>	MAKE_BASE=TRUE		=MEM_B_DQ<50>		
MEM_B_DQ<8>	MAKE_BASE=TRUE		=MEM_B_DQ<55>		

CPU CHANNEL B DQS 2 -> DIMM B DQS 5

MEM_B_DQS_N<2>	MAKE_BASE=TRUE		=MEM_B_DQS_N<5>		
MEM_B_DQS_P<2>	MAKE_BASE=TRUE		=MEM_B_DQS_P<5>		
MEM_B_DM<2>	MAKE_BASE=TRUE		=MEM_B_DM<5>		
MEM_B_DQ<23>	MAKE_BASE=TRUE		=MEM_B_DQ<45>		
MEM_B_DQ<22>	MAKE_BASE=TRUE		=MEM_B_DQ<40>		
MEM_B_DQ<21>	MAKE_BASE=TRUE		=MEM_B_DQ<42>		
MEM_B_DQ<20>	MAKE_BASE=TRUE		=MEM_B_DQ<47>		
MEM_B_DQ<19>	MAKE_BASE=TRUE		=MEM_B_DQ<44>		
MEM_B_DQ<18>	MAKE_BASE=TRUE		=MEM_B_DQ<41>		
MEM_B_DQ<17>	MAKE_BASE=TRUE		=MEM_B_DQ<46>		
MEM_B_DQ<16>	MAKE_BASE=TRUE		=MEM_B_DQ<43>		

CPU CHANNEL B DQS 3 -> DIMM B DQS 4

MEM_B_DQS_N<3>	MAKE_BASE=TRUE		=MEM_B_DQS_N<4>		
MEM_B_DQS_P<3>	MAKE_BASE=TRUE		=MEM_B_DQS_P<4>		
MEM_B_DM<3>	MAKE_BASE=TRUE		=MEM_B_DM<4>		
MEM_B_DQ<31>	MAKE_BASE=TRUE		=MEM_B_DQ<32>		
MEM_B_DQ<30>	MAKE_BASE=TRUE		=MEM_B_DQ<39>		
MEM_B_DQ<29>	MAKE_BASE=TRUE		=MEM_B_DQ<37>		
MEM_B_DQ<28>	MAKE_BASE=TRUE		=MEM_B_DQ<38>		
MEM_B_DQ<27>	MAKE_BASE=TRUE		=MEM_B_DQ<35>		
MEM_B_DQ<26>	MAKE_BASE=TRUE		=MEM_B_DQ<34>		
MEM_B_DQ<25>	MAKE_BASE=TRUE		=MEM_B_DQ<36>		
MEM_B_DQ<24>	MAKE_BASE=TRUE		=MEM_B_DQ<33>		

CPU CHANNEL B DQS 4 -> DIMM B DQS 3

MEM_B_DQS_N<4>	MAKE_BASE=TRUE		=MEM_B_DQS_N<3>		
MEM_B_DQS_P<4>	MAKE_BASE=TRUE		=MEM_B_DQS_P<3>		
MEM_B_DM<4>	MAKE_BASE=TRUE		=MEM_B_DM<3>		
MEM_B_DQ<39>	MAKE_BASE=TRUE		=MEM_B_DQ<28>		
MEM_B_DQ<38>	MAKE_BASE=TRUE		=MEM_B_DQ<24>		
MEM_B_DQ<37>	MAKE_BASE=TRUE		=MEM_B_DQ<31>		
MEM_B_DQ<36>	MAKE_BASE=TRUE		=MEM_B_DQ<30>		
MEM_B_DQ<35>	MAKE_BASE=TRUE		=MEM_B_DQ<29>		
MEM_B_DQ<34>	MAKE_BASE=TRUE		=MEM_B_DQ<25>		
MEM_B_DQ<33>	MAKE_BASE=TRUE		=MEM_B_DQ<27>		
MEM_B_DQ<32>	MAKE_BASE=TRUE		=MEM_B_DQ<26>		

CPU CHANNEL B DQS 5 -> DIMM B DQS 2

MEM_B_DQS_N<5>	MAKE_BASE=TRUE		=MEM_B_DQS_N<2>		
MEM_B_DQS_P<5>	MAKE_BASE=TRUE		=MEM_B_DQS_P<2>		
MEM_B_DM<5>	MAKE_BASE=TRUE		=MEM_B_DM<2>		
MEM_B_DQ<47>	MAKE_BASE=TRUE		=MEM_B_DQ<18>		
MEM_B_DQ<46>	MAKE_BASE=TRUE		=MEM_B_DQ<20>		
MEM_B_DQ<45>	MAKE_BASE=TRUE		=MEM_B_DQ<23>		
MEM_B_DQ<44>	MAKE_BASE=TRUE		=MEM_B_DQ<22>		
MEM_B_DQ<43>	MAKE_BASE=TRUE		=MEM_B_DQ<19>		
MEM_B_DQ<42>	MAKE_BASE=TRUE		=MEM_B_DQ<21>		
MEM_B_DQ<41>	MAKE_BASE=TRUE		=MEM_B_DQ<17>		
MEM_B_DQ<40>	MAKE_BASE=TRUE		=MEM_B_DQ<16>		

CPU CHANNEL B DQS 6 -> DIMM B DQS 1

MEM_B_DQS_N<6>	MAKE_BASE=TRUE		=MEM_B_DQS_N<1>		
MEM_B_DQS_P<6>	MAKE_BASE=TRUE		=MEM_B_DQS_P<1>		
MEM_B_DM<6>	MAKE_BASE=TRUE		=MEM_B_DM<1>		
MEM_B_DQ<55>	MAKE_BASE=TRUE		=MEM_B_DQ<8>		
MEM_B_DQ<54>	MAKE_BASE=TRUE		=MEM_B_DQ<14>		
MEM_B_DQ<53>	MAKE_BASE=TRUE		=MEM_B_DQ<10>		
MEM_B_DQ<52>	MAKE_BASE=TRUE		=MEM_B_DQ<11>		
MEM_B_DQ<51>	MAKE_BASE=TRUE		=MEM_B_DQ<9>		
MEM_B_DQ<50>	MAKE_BASE=TRUE		=MEM_B_DQ<15>		
MEM_B_DQ<49>	MAKE_BASE=TRUE		=MEM_B_DQ<12>		
MEM_B_DQ<48>	MAKE_BASE=TRUE		=MEM_B_DQ<13>		

CPU CHANNEL B DQS 7 -> DIMM B DQS 0

MEM_B_DQS_N<7>	MAKE_BASE=TRUE		=MEM_B_DQS_N<0>		
MEM_B_DQS_P<7>	MAKE_BASE=TRUE		=MEM_B_DQS_P<0>		
MEM_B_DM<7>	MAKE_BASE=TRUE		=MEM_B_DM<0>		
MEM_B_DQ<63>	MAKE_BASE=TRUE		=MEM_B_DQ<2>		
MEM_B_DQ<62>	MAKE_BASE=TRUE		=MEM_B_DQ<1>		
MEM_B_DQ<61>	MAKE_BASE=TRUE		=MEM_B_DQ<3>		
MEM_B_DQ<60>	MAKE_BASE=TRUE		=MEM_B_DQ<7>		
MEM_B_DQ<59>	MAKE_BASE=TRUE		=MEM_B_DQ<4>		
MEM_B_DQ<58>	MAKE_BASE=TRUE		=MEM_B_DQ<5>		
MEM_B_DQ<57>	MAKE_BASE=TRUE		=MEM_B_DQ<6>		
MEM_B_DQ<56>	MAKE_BASE=TRUE		=MEM_B_DQ<0>		

MEMORY CLOCK ALIASING

MEM_A_CLK_P<0>	MAKE_BASE=TRUE		=MEM_A_CLK_P<0>		
MEM_A_CLK_N<0>	MAKE_BASE=TRUE		=MEM_A_CLK_N<0>		
MEM_A_CLK_P<1>	MAKE_BASE=TRUE		=MEM_A_CLK_P<1>		
MEM_A_CLK_N<1>	MAKE_BASE=TRUE		=MEM_A_CLK_N<1>		
MEM_A_CLK_P<2>	MAKE_BASE=TRUE		=MEM_A_CLK_P<2>		
MEM_A_CLK_N<2>	MAKE_BASE=TRUE		=MEM_A_CLK_N<2>		
MEM_A_CLK_P<3>	MAKE_BASE=TRUE		=MEM_A_CLK_P<3>		
MEM_A_CLK_N<3>	MAKE_BASE=TRUE		=MEM_A_CLK_N<3>		

MEM_B_CLK_P<0>			=MEM_B_CLK_P<0>		
MEM_B_CLK_N<0>	MAKE_BASE=TRUE		=MEM_B_CLK_N<0>		
MEM_B_CLK_P<1>	MAKE_BASE=TRUE		=MEM_B_CLK_P<1>		
MEM_B_CLK_N<1>	MAKE_BASE=TRUE		=MEM_B_CLK_N<1>		
MEM_B_CLK_P<2>	MAKE_BASE=TRUE		=MEM_B_CLK_P<2>		
MEM_B_CLK_N<2>	MAKE_BASE=TRUE		=MEM_B_CLK_N<2>		
MEM_B_CLK_P<3>	MAKE_BASE=TRUE		=MEM_B_CLK_P<3>		
MEM_B_CLK_N<3>	MAKE_BASE=TRUE		=MEM_B_CLK_N<3>		

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE

DDR3 ALIAS AND BITSWAPS

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D

REVISION A.0.0

BRANCH

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3.3V S3 CURRENT	D0:D2,D3HOT	D3COLD
MAX CONT:	1100MA	100MA
MAX PEAK:	2750MA	2750MA
1.5V CURRENT		
MAX CONT:	N/U	N/U
MAX PEAK:	N/U	N/U

NOTE: CURRENT DATA PER JAN 12,2008 PCIE MINI CEM ECN

NO STUFF
R3400
0
5%
1/16W
MF-LF
402

NO STUFF
R3401
0
5%
1/16W
MF-LF
402

CRITICAL
J3400
AS0B226-S40N-7F
F-RT-SM

36 18 OUT	PCIE_WAKE_L	1	2
	RSVD_MINI_WLAN_ACTIVE	3	4
	RSVD_MINI_BT_ACTIVE	5	6
17 14 OUT	MINI_CLKREQ_L	7	8 NC
		9	10 NC
84 17 IN	PCIE_CLK100M_MINI_N	11	12 NC
84 17 IN	PCIE_CLK100M_MINI_P	13	14 NC
		15	16 NC
	RESERVED	17	18
	RESERVED	19	20 NC
		21	22 MINI_RESET_L IN 27 91
		23	24
		25	26
		27	28
	SMB_MINI_SCL	29	30
	SMB_MINI_SDA	31	32
		33	34
	TP_USB_MININ	35	36
	TP_USB_MINIP	37	38
		39	40
		41	42 NC
		43	44 NC
	NC	45	46 NC
	NC	47	48
	NC	49	50
	NC	51	52
		53	
		54	

516S0457

NO AVAILALBLE USB ON THIS PLATFORM
TARGET CARDS DO NOT USE IT

=PP3V3_S3_MINI 5

C3410 0.1uF 20% 10V CERM 402
C3420 0.1uF 20% 10V CERM 402
C3421 10uF 20% 6.3V X5R 603

=PP1V5_S0_MINI 5

C3400 0.1uF 20% 10V CERM 402
C3401 10uF 20% 6.3V X5R 603

84 17 OUT PCIE_MINI_D2R_N
84 17 OUT PCIE_MINI_D2R_P

PLACEMENT_NOTE=PLACE CLOSE TO U1800.
C3431
0.1uF
84 17 IN PCIE_MINI_R2D_C_N
10% 16V X5R 402

84 PCIE_MINI_R2D_N
84 PCIE_MINI_R2D_P

PLACEMENT_NOTE=PLACE CLOSE TO U1800.
C3430
0.1uF
84 17 IN PCIE_MINI_R2D_C_P
10% 16V X5R 402

R3490 0 =SMB_MINI_SCL 49
R3491 0 =SMB_MINI_SDA 49

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
PCI-E MiniCard Connector

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D
REVISION A.0.0
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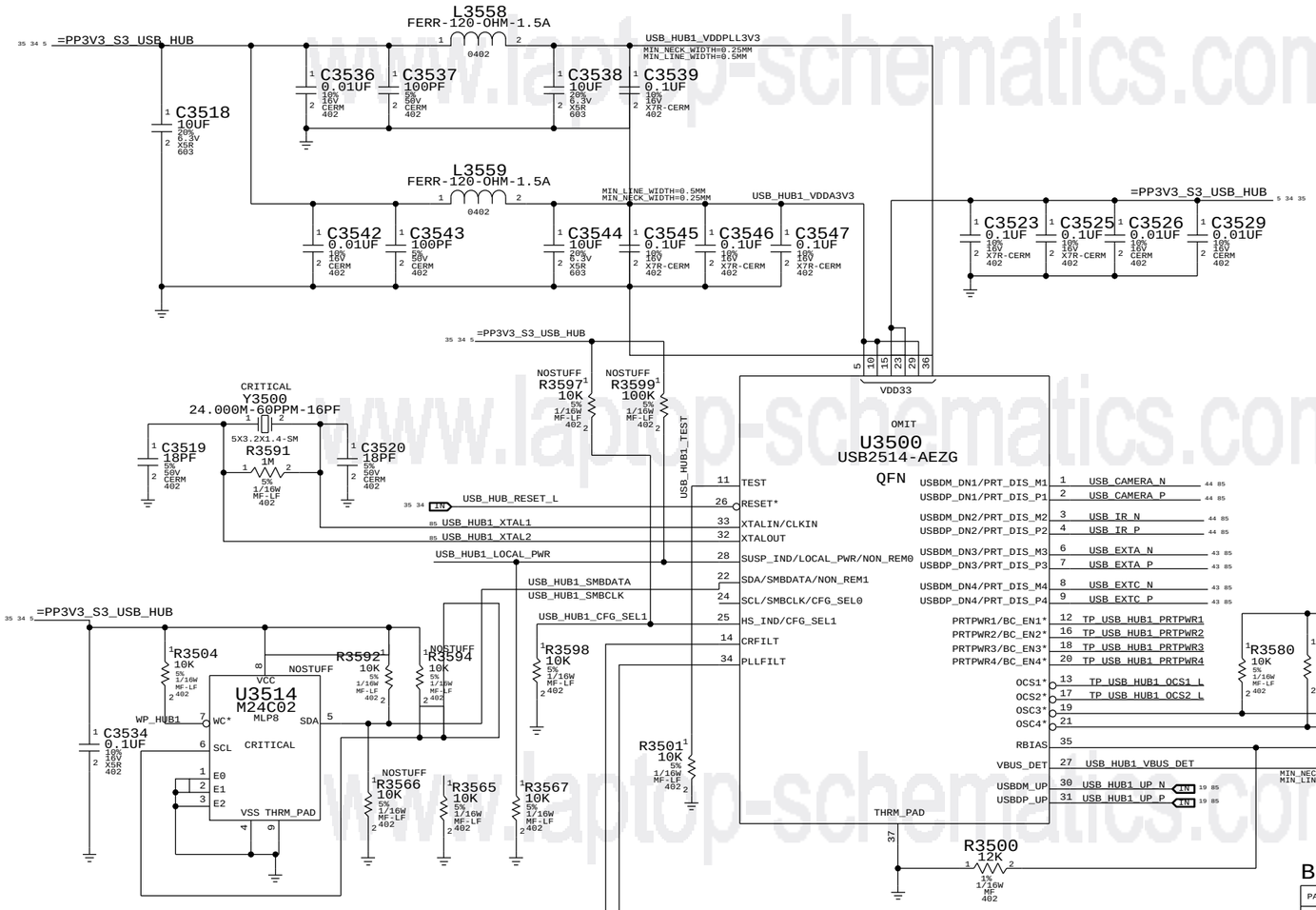
USB HUB-1



SEL1	SEL0	DESCRIPTION
DEFAULT K23F ==> 0	0	Internal Default with Self powered Operation
0	1	SMBUS Slave Config
1	0	Internal Default with Bus powered Operation
1	1	EEPROM Supported

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are Non removable
0	1	Port1 is non removable
DEFAULT K23F ==> 1	0	Port 1 and 2 are non removable
1	1	Port1,2 and 3 are non Removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0721	2	SMSC USX2061-AEZG	U3500,U3600	CRITICAL	HUB_USX2061
338S0824	2	SMSC USB2514B	U3500,U3600	CRITICAL	HUB_USB2514B

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: USB HUB 1

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

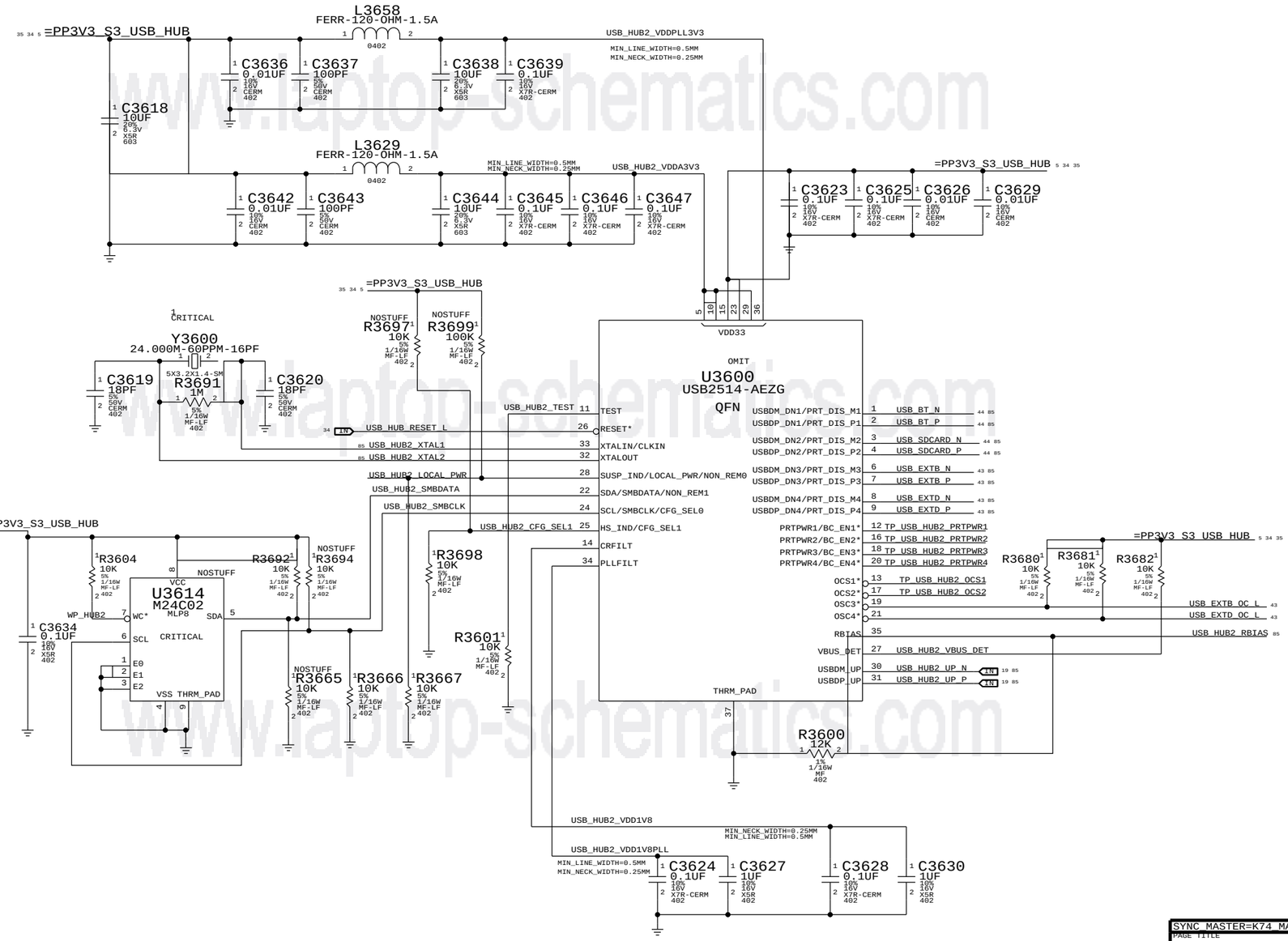
REVISION: A.0.0

BRANCH:

PAGE: 35 OF 110

SHEET: 34 OF 92

USB HUB-2



SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: USB HUB 2

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

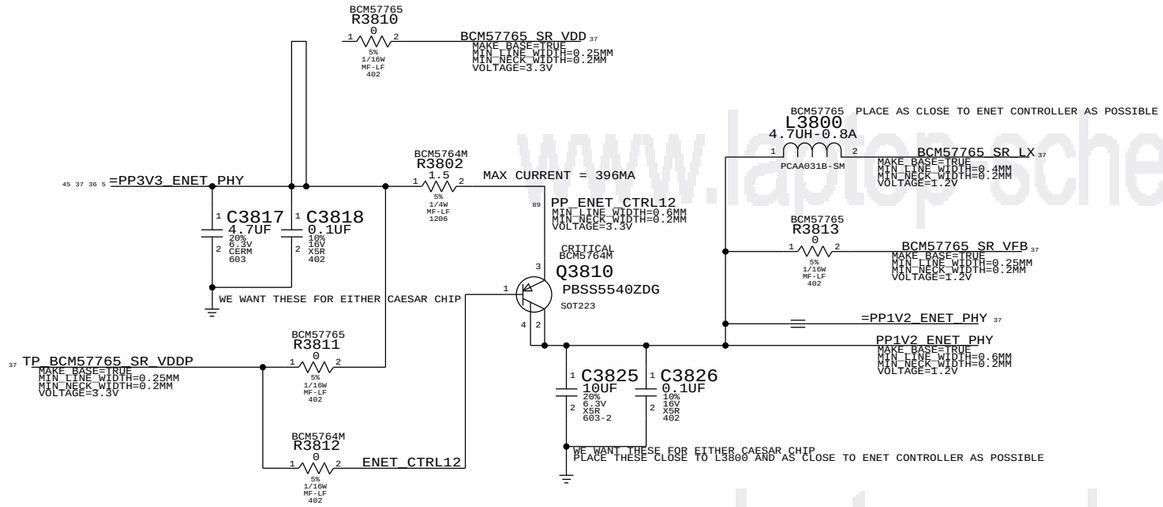
REVISION: A.0.0

BRANCH:

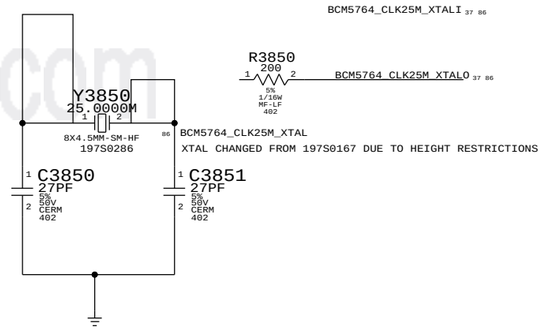
PAGE: 36 OF 110

SHEET: 35 OF 92

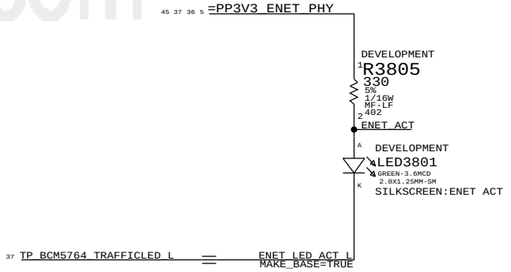
CAESAR II/IV 1V2 RAIL SUPPLY



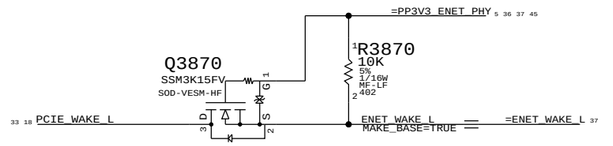
CAESAR II/IV 25MHZ XTAL



CAESAR II/IV ACTIVITY LED

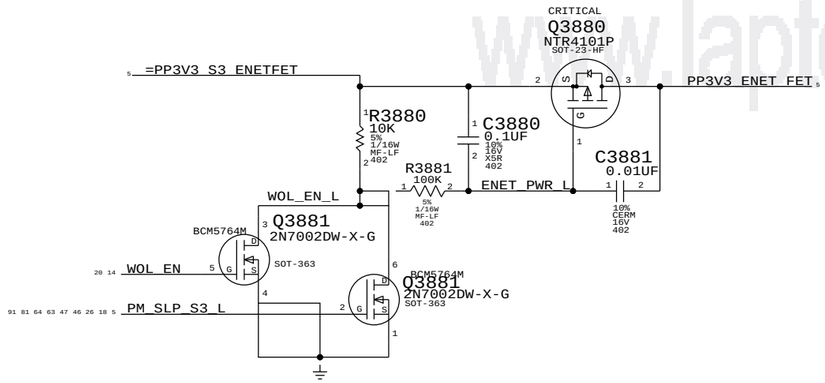


CAESAR II/IV WAKE# ISOLATION



3.3V ENET FET

ENET_PWR_ON = "S0" || (S3 power && WOL_EN)



CAESAR II/IV Support

SYNC_MASTER=MASTER	SYNC_DATE=N/A
PAGE TITLE: Caesar II/IV Support	
Apple Inc.	DRAWING NUMBER: 051-8337 SIZE: D
	REVISION: A.0.0
	BRANCH:
	PAGE: 38 OF 110
	SHEET: 36 OF 92

BCM57765 SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_ENET_PHY (add bypassing), LX connects to inductor.

=PP3V3_ENET_PHY
86mA (1000base-T, Caesar II)

PP3V3R1V8_SW_LR_OUT

BCM57765 R3915 0 5% 1/16W MF-LF 402

CRITICAL L3900 FERR-600-OHM-0.5A SM
PP3V3_ENET_PHY_XTALVDDH
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V

BCM57765 R3900 0 5% 1/16W MF-LF 402
BCM57765_XTALVDDH
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V

C3900 0.1UF 10% 16V X7R-CERM 402

CRITICAL L3905 FERR-600-OHM-0.5A SM
PP3V3_ENET_PHY_BIASVDDH
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V

C3905 0.1UF 10% 16V X7R-CERM 402

CRITICAL L3910 FERR-600-OHM-0.5A SM
PP3V3_ENET_PHY_AVDDH
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V

R3910 4.7K 5% 1/16W MF-LF 402
C3910 0.1UF 10% 16V X7R-CERM 402
C3911 0.1UF 10% 16V X7R-CERM 402

BCM57765 R3940 4.7K 5% 1/16W MF-LF 402
BCM57765 R3941 4.7K 5% 1/16W MF-LF 402

C3915 4.7UF 10% 6.3V X5R-CERM 603
C3916 0.1UF 10% 16V X7R-CERM 402

=PP3V3_S0_ENETPHY
BCM57765 R3942 1K 5% 1/16W MF-LF 402

C3950 0.1uF 10% 16V X5R 402
C3951 0.1uF 10% 16V X5R 402
C3955 0.1uF 10% 16V X5R 402
C3956 0.1uF 10% 16V X5R 402

BCM57765 R3943 0 5% 1/16W MF-LF 402
=ENET_WAKE_L
(See note)

WAKE#

Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

TP_BCM57765_SR_VDDP
BCM57765_SR_VDD
BCM57765_VDDOCR_PIN20
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V

BCM57765_SR_LX
BCM57765_SR_VFB

BCM57765 R3920 0 5% 1/16W MF-LF 402

=PP1V2_ENET_PHY
396mA (1000base-T, Caesar II)

CRITICAL L3920 FERR-600-OHM-0.5A SM
PP1V2_ENET_PHY_AVDDL
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V

C3921 0.1UF 10% 16V X7R-CERM 402
C3920 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL L3925 FERR-600-OHM-0.5A SM
PP1V2_ENET_PHY_PCIEPLL
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V

C3926 0.1UF 10% 16V X7R-CERM 402
C3925 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL L3930 FERR-600-OHM-0.5A SM
PP1V2_ENET_PHY_GPHYPLL
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V

C3931 0.1UF 10% 16V X7R-CERM 402
C3930 4.7UF 10% 6.3V X5R-CERM 603

C3936 0.1UF 10% 16V X7R-CERM 402
C3935 10UF 10% 6.3V X5R 805

AVDDH BIASVDDH VDDC VDDIO XTALVDDH VDDIO VDDIO VDDC REGCTL12 VDDIO WAKE* AVDDL PCIE_PLLVDDL GPHY_PLLVDDL VDDC VDDC

CRITICAL
OMIT
U3900
BCM5764M
QFN-8X8
VERSION 2

PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_P
PCIE_ENET_R2D_C_N
BCM57765_VMAIN_PRSNT
PCIE_ENET_D2R_C_N
PCIE_ENET_D2R_C_P
PCIE_ENET_R2D_P
PCIE_ENET_R2D_N
PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
ENET_RESET_L
ENET_CLKREQ_L
BCM57765_WAKE_L
ENET_LOW_PWR
BCM57765_SMB_CLK
BCM57765_SMB_DATA
BCM5764_SCLK
BCM5764_MISO
BCM5764_MOSI
BCM5764_CS_L
TP_BCM5764_SPD100LED_L
TP_BCM5764_TRAFFICLED_L
BCM5764_CLK25M_XTALI
BCM5764_CLK25M_XTALO
BCM5764_RDAC

SMB_DATA (IPD-BCM57765)
PCIE_TXD_N
PCIE_TXD_P
PCIE_RXD_P
PCIE_RXD_N
PCIE_REFCLK_P
PCIE_REFCLK_N
PERST* (IPD)
CLKREQ* (OD)
LINKLED* (OD)
LOW_PWR (IPD)
VDDC
UART_MODE (IPD-BCM5764M)
SCLK
SI
SO
CS*
SPD100LED*
TRAFFICLED*
XTALI
XTALO
RDAC

R3965 1.24K 1% 1/16W MF-LF 402

BCM57765_SR_DISABLE

If BCM57765 switching regulator is used, this pin can float (alias to TP_). If not used, must be pulled to 3.3V ENET via 1K resistor (not provided on this page).

THRM_PAD 69

TRD0_P TRD0_N TRD1_P TRD1_N TRD2_P TRD2_N TRD3_P TRD3_N
ENET_MDI_P<0> ENET_MDI_N<0> ENET_MDI_P<1> ENET_MDI_N<1> ENET_MDI_P<2> ENET_MDI_N<2> ENET_MDI_P<3> ENET_MDI_N<3>

GPIO_0/SERIAL_DO
GPIO_1/SERIAL_DI
GPIO_2
NC
PCIE_VDDL
DC0
DC4 DC3 DC2 DC1 NC VMAIN_PRSNT VAUX_PRSNT VDDC
SMB_CLK
ENERGY_DET
DC5
SPD1000LED*

NOTE: "IPx" == Programmable pull-up/down

BCM57765 R3972 0 5% 1/16W MF-LF 402 — ENET_ENERGY_DET
BCM57765 R3973 0 5% 1/16W MF-LF 402 — SDCONN_CD_L
BCM57765 R3974 0 5% 1/16W MF-LF 402 (PLACE_NEAR=L3999.1:1 mm) — SDCONN_CMD
SDCONN_CLK
SDCONN_DATA<0> SDCONN_DATA<1> SDCONN_DATA<2> SDCONN_DATA<3> SDCONN_DATA<4> SDCONN_DATA<5> SDCONN_DATA<6> SDCONN_DATA<7>
BCM57765 R3975 0 5% 1/16W MF-LF 402 — BCM57765_CR_DATA<4>
BCM57765 R3976 0 5% 1/16W MF-LF 402 — BCM57765_CR_DATA<5>
BCM57765 R3977 0 5% 1/16W MF-LF 402 — BCM57765_CR_DATA<6>
BCM57765 R3978 0 5% 1/16W MF-LF 402 — BCM57765_CR_DATA<7>
BCM57765_CE_L_MS_INS_L
BCM57765_CR_PWREN
BCM57765_SR_DISABLE
SDCONN_WP

All resistors above BOMOPTIONed BCM57765

BCM57765 supports both active-levels for WP.

GPIO1_LR_OUT is not for SD Card power, just decoupling for BCM57765 CR I/Os. Connect only to U3900 pins 9 and 20.

BCM57765 C3970 4.7UF 10% 6.3V X5R-CERM 603
BCM57765 C3971 0.1UF 10% 16V X7R-CERM 402
BCM57765 C3972 0.1UF 10% 16V X7R-CERM 402

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Required for proper PHY operation.
(Required ROM size TBD)

=PP3V3_ENET_PHY
C3990 0.1UF 10% 16V X7R-CERM 402
U3990 AT45DB011D SOIC-8S1 OMIT
VCC SCK CS* WP* RESET* GND SI SO
BCM5764_SCLK
BCM5764_CS_L
BCM5764_MOSI
BCM5764_MISO
NOSTUFF
R3990 4.7K 5% 1/16W MF-LF 402
R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures BCM57765 for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: BCM5764M requires SI pull-down instead of SO.

BCM5764M Support

All parts below BOMOPTIONed BCM5764M

BCM5764M pin-function

60-ENERGY_DET	BCM57765_CR_PWREN	R3980	0	ENET_ENERGY_DET
13-WAKE*	BCM57765_SR_VFB	R3981	0	=ENET_WAKE_L (See note)
53-VMAIN_PRSNT	BCM57765_CR_DATA<5>	R3982	1K	=PP3V3_S0_ENETPHY
59-SMB_CLK	BCM57765_CE_L_MS_INS_L	R3983	4.7K	=PP3V3_ENET_PHY
58-SMB_DATA	BCM57765_VMAIN_PRSNT	R3984	4.7K	
54-VAUX_PRSNT	BCM57765_CR_DATA<6>	R3985	1K	
16-VDDIO	BCM57765_SR_LX	R3986	0	
20-XTALVDDH	BCM57765_VDDOCR_PIN20	R3987	0	PP3V3_ENET_PHY_XTALVDDH
55-VDDC	BCM57765_CR_DATA<7>	R3988	0	=PP1V2_ENET_PHY
17-VDDC	BCM57765_XTALVDDH	R3989	0	
14-VDDC	BCM57765_SR_VDD	R3998	0	
06-VDDC	BCM57765_SMB_CLK	R3999	0	

L3999 FERR-600-OHM-0.5A SM CRITICAL (PLACE_NEAR=U3900.26:2 mm)

26-PCIE_VDDL — BCM57765_CR_CMD

Keep net short, with no stubs.

BCM5764M C3999 0.1UF 10% 16V X7R-CERM 402 (PLACE_NEAR=U3900.26:1 mm)
BCM5764M C3998 4.7UF 10% 6.3V X5R-CERM 603 (PLACE_NEAR=L3999.1:1 mm)

SYNC_MASTER=T27 SYNC_DATE=11/30/2009

PAGE TITLE
Ethernet PHY (Caesar II/IV)

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D
REVISION A.0.0
BRANCH
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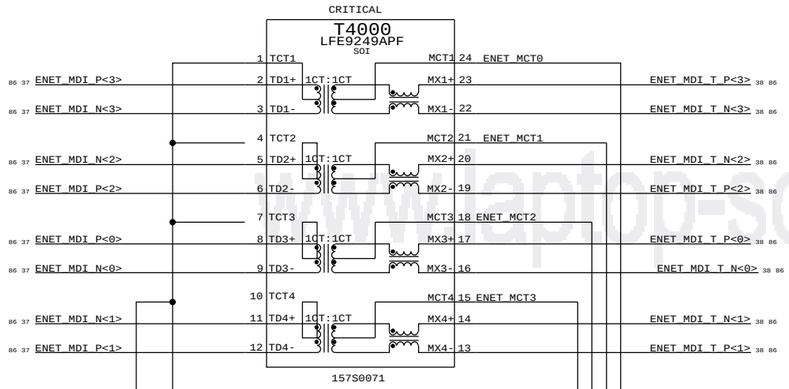
SHEET 37 OF 92

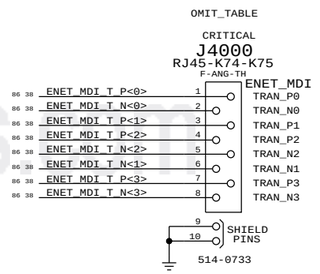


PLACE ONE CAP PER TCT PIN

NOTE: Check with PHY and Magnetics MFR to determine what to do with center taps.

NOTE: BOB SMITH TERMINATION FOR EMC.

OMIT_TABLE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0654	1	K22/K23 PROD. RJ45	J4000	CRITICAL	METAL_IO
514-0733	1	K74/K75 RJ45, PLASTIC, PD/NI	J4000	CRITICAL	PLASTIC_IO

SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE: Ethernet Connector

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 40 OF 110

SHEET: 38 OF 92

Power Aliases:

FW_FWPHY nets are PHY power, and for multi-port systems must come from bus power.

FWRS0_FWXIO nets are OHCI/PCIe power, and can be S0.

For single-port systems, all FW power should be tied together and powered by S0 or by the 5K pull-down device detect circuit.

PCI EXPRESS

1394B OHCI & PHY

Single-port:
PC[0:2] = '000'

Multiple-ports:
PC[0:2] = '100'

Alias =FWPHY_PC0 as appropriate

Unused Ports:

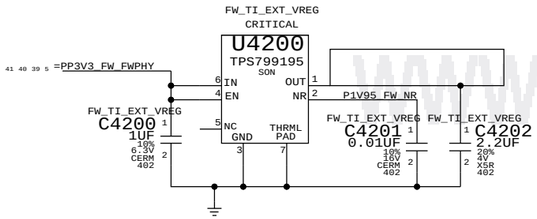
TP/NC TPBIASx
TP/NC TPAx_P/TPAx_N
Ground TPBx_P/TPBx_N

DS2 hard-strapped to 1, page assumes no more than 2 FW800 connectors

Strap DSx high on unused ports.

SYNC_MASTER=MASTER	SYNC_DATE=N/A
PAGE TITLE	FireWire LLC/PHY (XIO2213B)
Apple Inc.	DRAWING NUMBER 051-8337 · SIZE D
	REVISION A.0.0
	BRANCH
	PAGE 41 OF 110
	SHEET 39 OF 92

1394 PHY 1.95V SUPPLY



PP1V95_FW_FWPHY 39 89
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
VOLTAGE=1.95V
Peak Current: 100mA

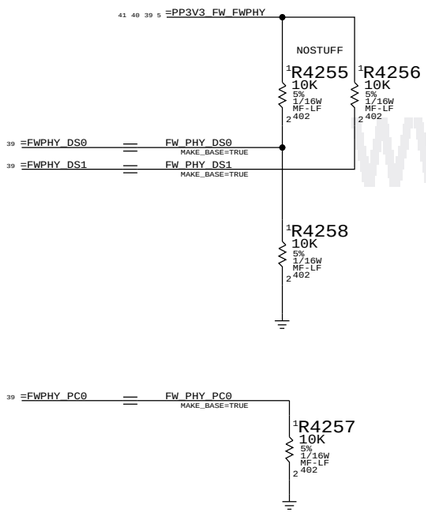
FireWire Aliases For Connectivity

39 =FW_CLKREQ_L — FW_CLKREQ_L 14 17
MAKE_BASE=TRUE

39 =FW_PME_L — FW_PME_L 14 20
MAKE_BASE=TRUE

39 =PPVP_FW_PHY_CPS — PPVP_FW_PHY_CPS 41 89
MAKE_BASE=TRUE

1394 PHY STRAPPING OPTIONS

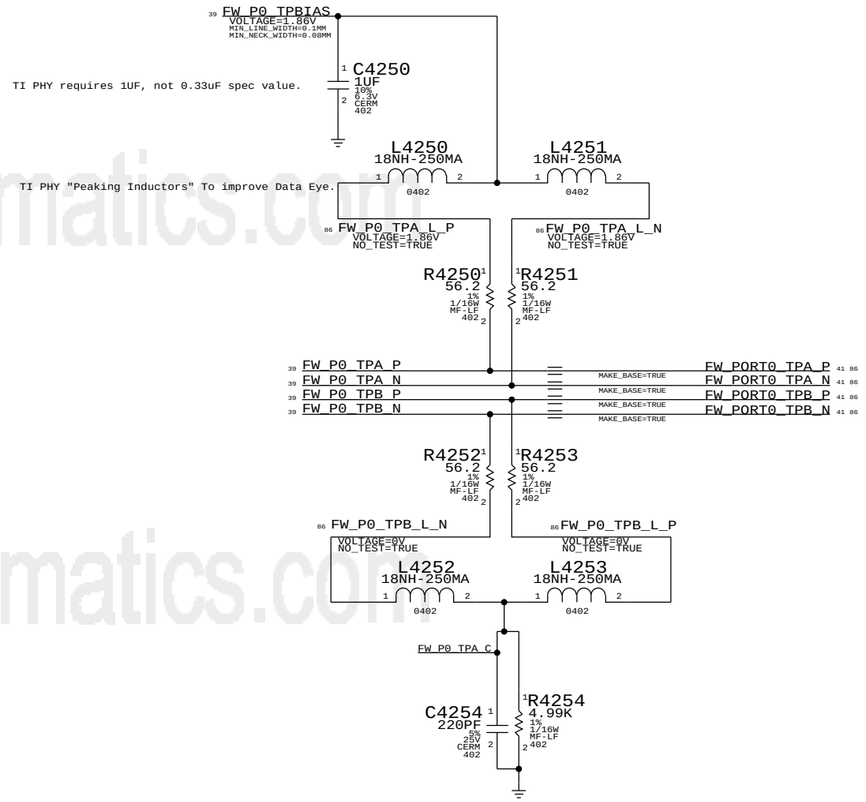


THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE.

iMacs are now one port only and have Power Code "000"

Termination

Place close to FireWire PHY



2ND & 3RD TPA/TPB PAIR UNUSED

39 FW_P1_TPBIAS — NC_FW_PORT1_TPBIAS
MAKE_BASE=TRUE
NO_TEST=TRUE

86 39 FW_P1_TPA_P — NC_FW_PORT1_TPA_P
MAKE_BASE=TRUE
NO_TEST=TRUE

86 39 FW_P1_TPA_N — NC_FW_PORT1_TPA_N
MAKE_BASE=TRUE
NO_TEST=TRUE

39 FW_P2_TPBIAS — NC_FW_PORT2_TPBIAS
MAKE_BASE=TRUE
NO_TEST=TRUE

86 39 FW_P2_TPA_P — NC_FW_PORT2_TPA_P
MAKE_BASE=TRUE
NO_TEST=TRUE

86 39 FW_P2_TPA_N — NC_FW_PORT2_TPA_N
MAKE_BASE=TRUE
NO_TEST=TRUE

SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE
FW: 1394B MISC

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D
REVISION A.0.0
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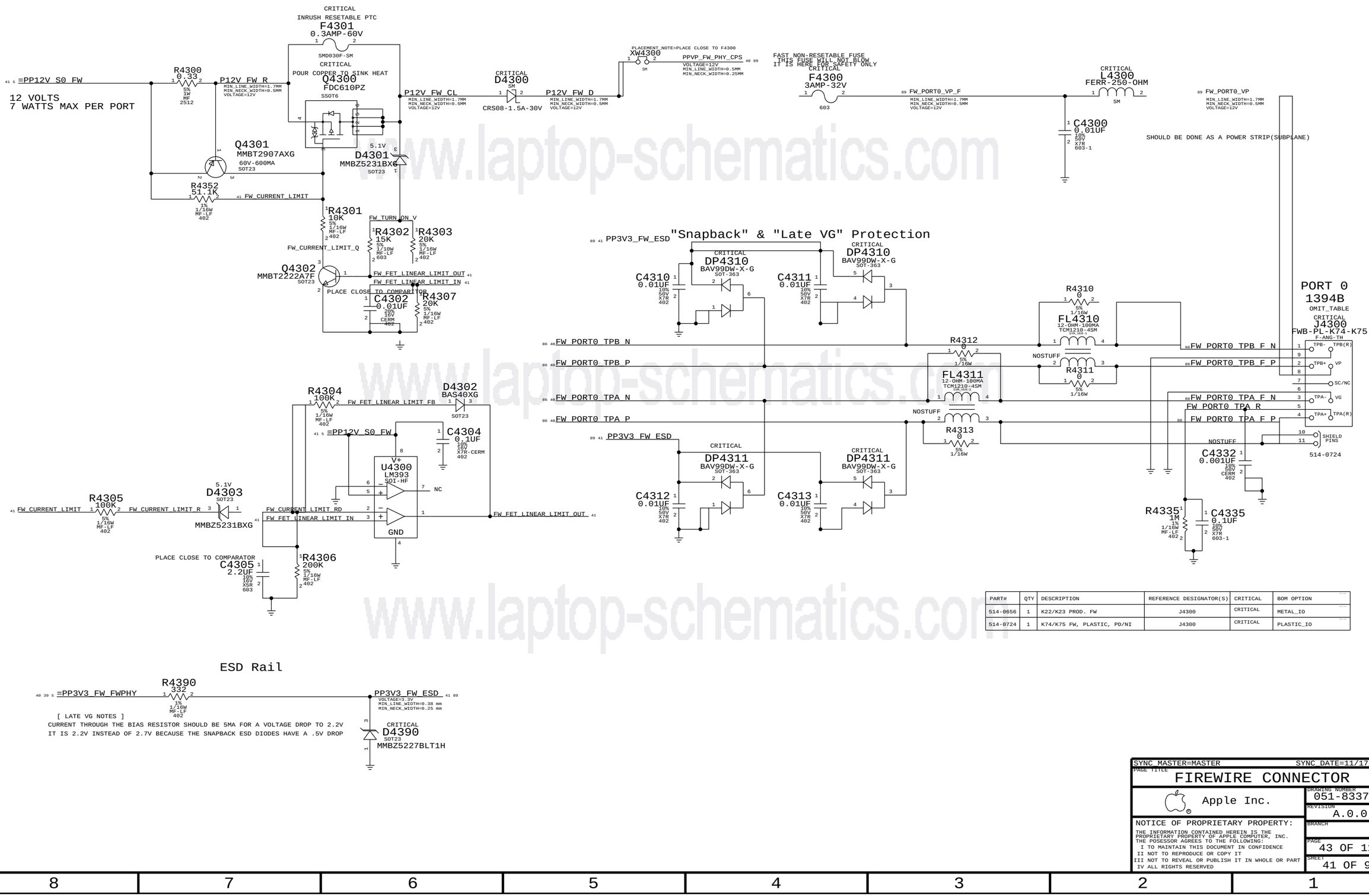

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0656	1	K22/K23 PROD. FW	J4300	CRITICAL	METAL_IO
514-0724	1	K74/K75 FW, PLASTIC, PD/NI	J4300	CRITICAL	PLASTIC_IO

SYNC_MASTER=MASTER SYNC_DATE=11/17/2009

PAGE TITLE: FIREWIRE CONNECTOR

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

BRANCH:

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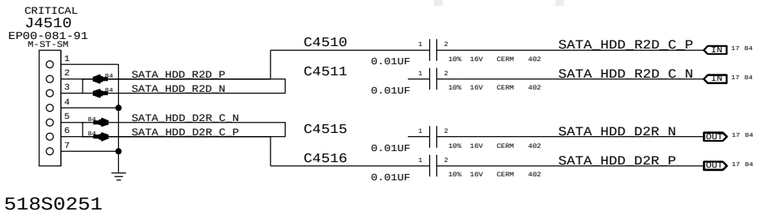
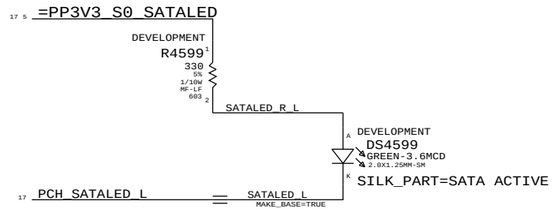
SATA PORT A0 FOR HDD

SILKSCREEN:HDD

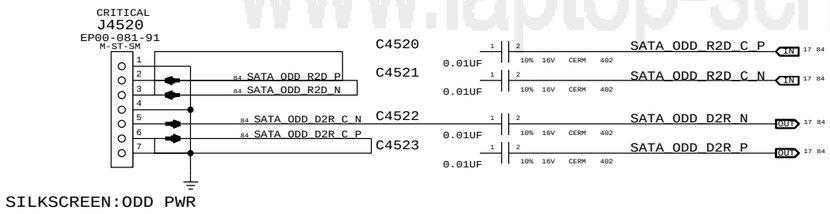


SATA Activity LED

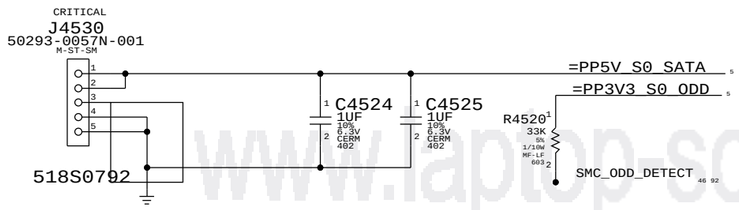


SATA PORT A1 FOR SLIMLINE ODD

SILKSCREEN:ODD



SILKSCREEN:ODD PWR



SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: SATA Connectors

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

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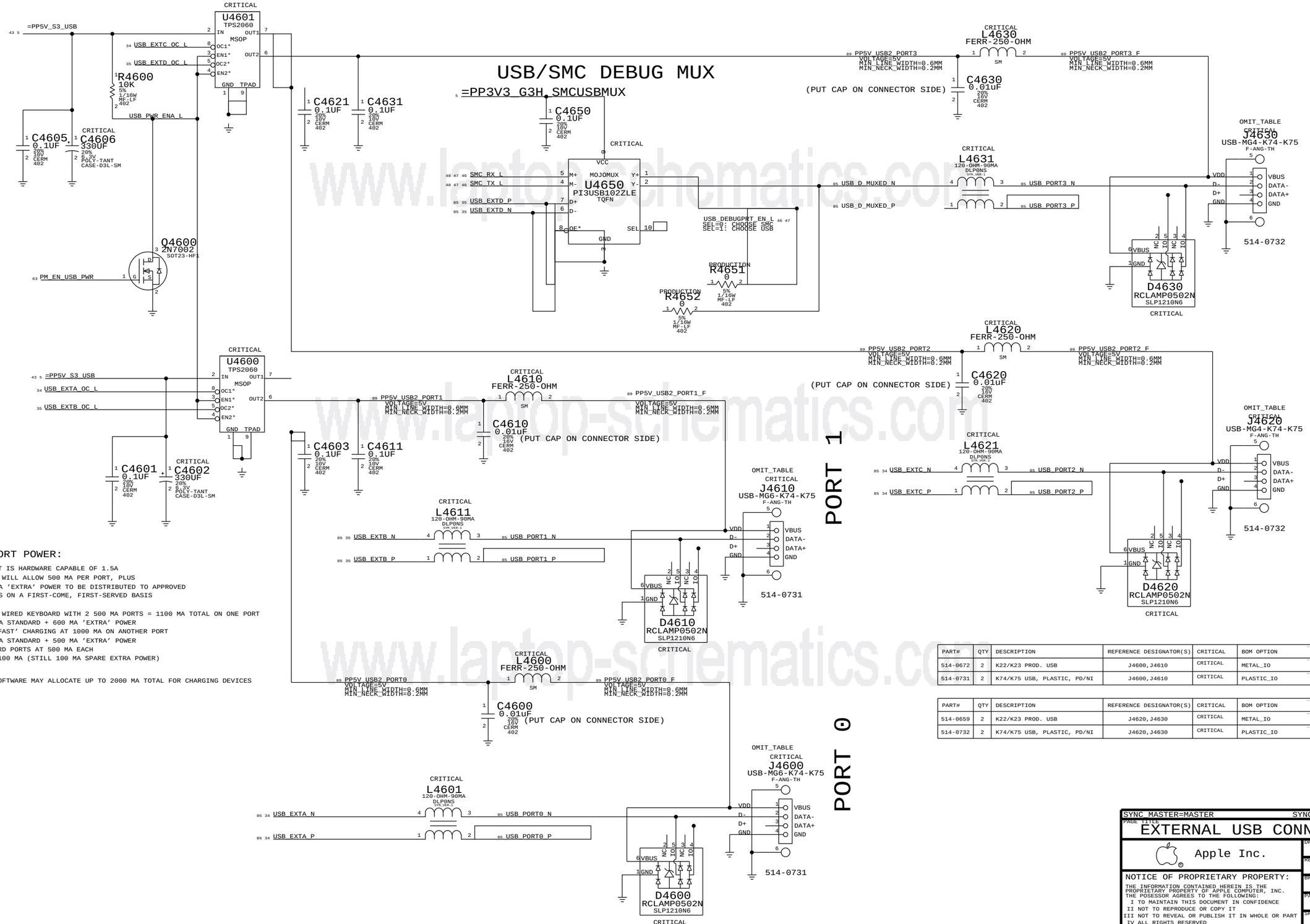
USB/SMC DEBUG MUX



USB PORT POWER:

EACH PORT IS HARDWARE CAPABLE OF 1.5A
SOFTWARE WILL ALLOW 500 MA PER PORT, PLUS
  1200 MA 'EXTRA' POWER TO BE DISTRIBUTED TO APPROVED
  DEVICES ON A FIRST-COME, FIRST-SERVED BASIS

EXAMPLE: WIRED KEYBOARD WITH 2 500 MA PORTS = 1100 MA TOTAL ON ONE PORT
   500 MA STANDARD + 600 MA 'EXTRA' POWER
IPHONE 'FAST' CHARGING AT 1000 MA ON ANOTHER PORT
   500 MA STANDARD + 500 MA 'EXTRA' POWER
2 STANDARD PORTS AT 500 MA EACH
TOTAL: 3100 MA (STILL 100 MA SPARE EXTRA POWER)

IN S3, SOFTWARE MAY ALLOCATE UP TO 2000 MA TOTAL FOR CHARGING DEVICES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0672	2	K22/K23 PROD. USB	J4600,J4610	CRITICAL	METAL_IO
514-0731	2	K74/K75 USB, PLASTIC, PD/NI	J4600,J4610	CRITICAL	PLASTIC_IO

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0659	2	K22/K23 PROD. USB	J4620,J4630	CRITICAL	METAL_IO
514-0732	2	K74/K75 USB, PLASTIC, PD/NI	J4620,J4630	CRITICAL	PLASTIC_IO

SYNC_MASTER=MASTER SYNC_DATE=11/30/2009

PAGE TITLE
EXTERNAL USB CONNECTORS

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D
REVISION A.0.0
BRANCH
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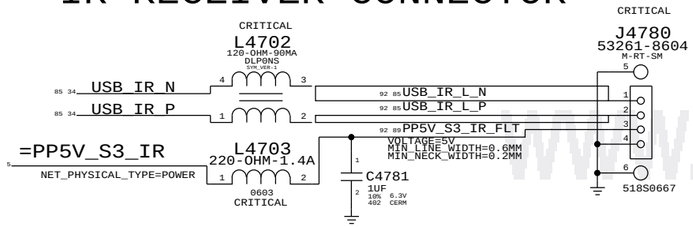
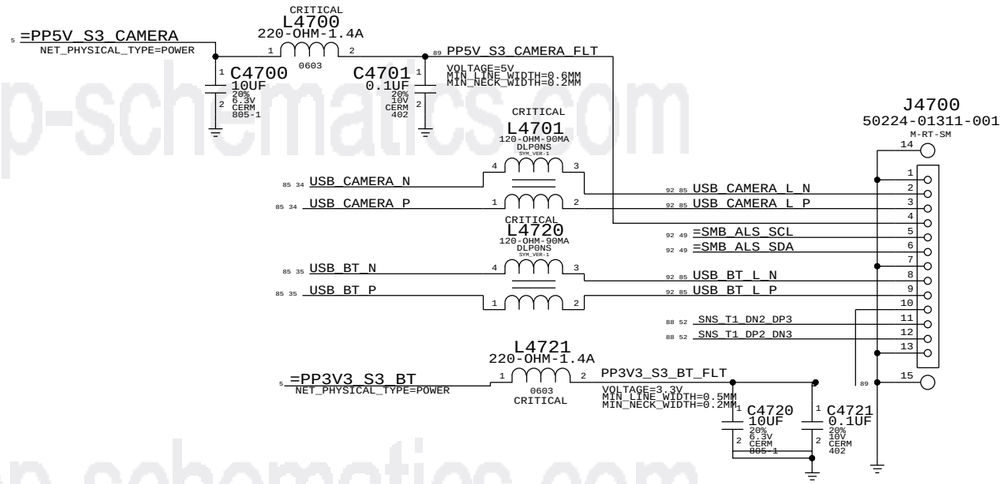
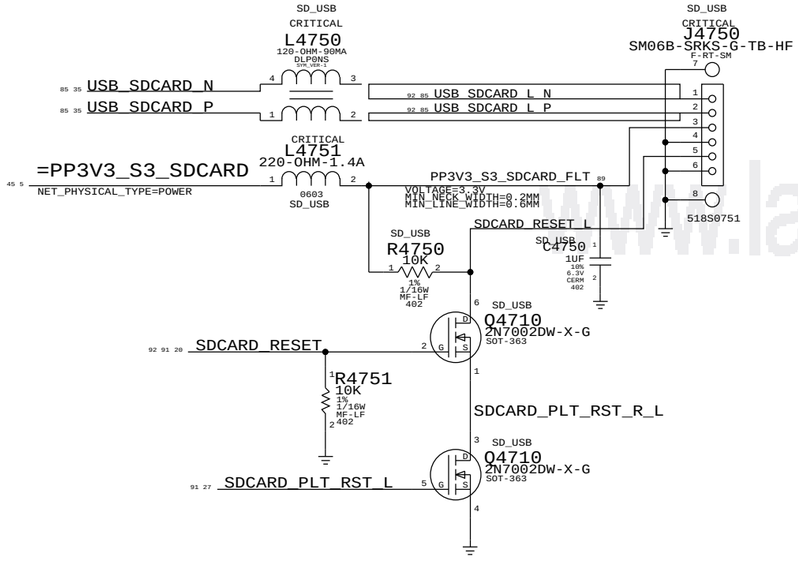
IR RECEIVER CONNECTOR



CAMERA/ALS & BLUETOOTH (K37A) CONNECTOR



LAZAURS SD CARD READER BOARD CONNECTOR
BACKUP TO CAESAR IV



SYNC_MASTER=MASTER SYNC_DATE=11/06/2009

PAGE TITLE: Internal USB Connections

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

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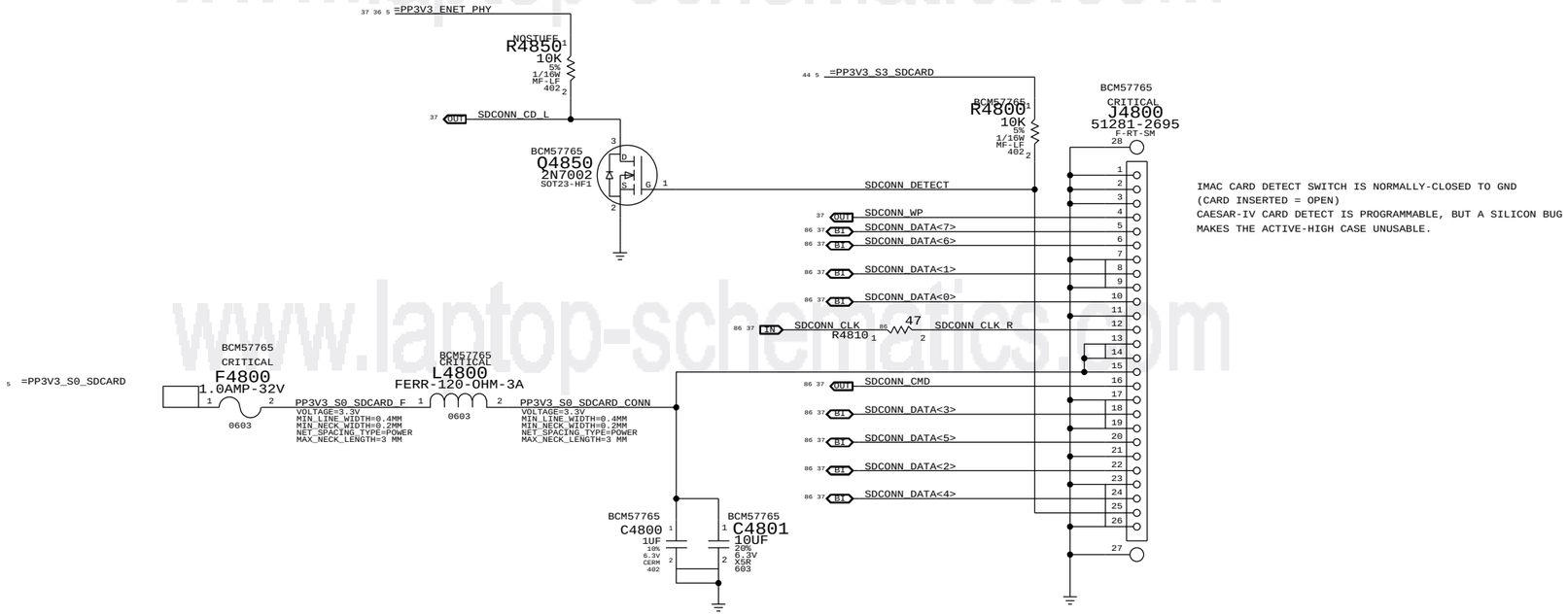

IMAC CARD DETECT SWITCH IS NORMALLY-CLOSED TO GND
(CARD INSERTED = OPEN)
CAESAR-IV CARD DETECT IS PROGRAMMABLE, BUT A SILICON BUG
MAKES THE ACTIVE-HIGH CASE UNUSABLE.

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
SD READER CONNECTOR

Apple Inc.

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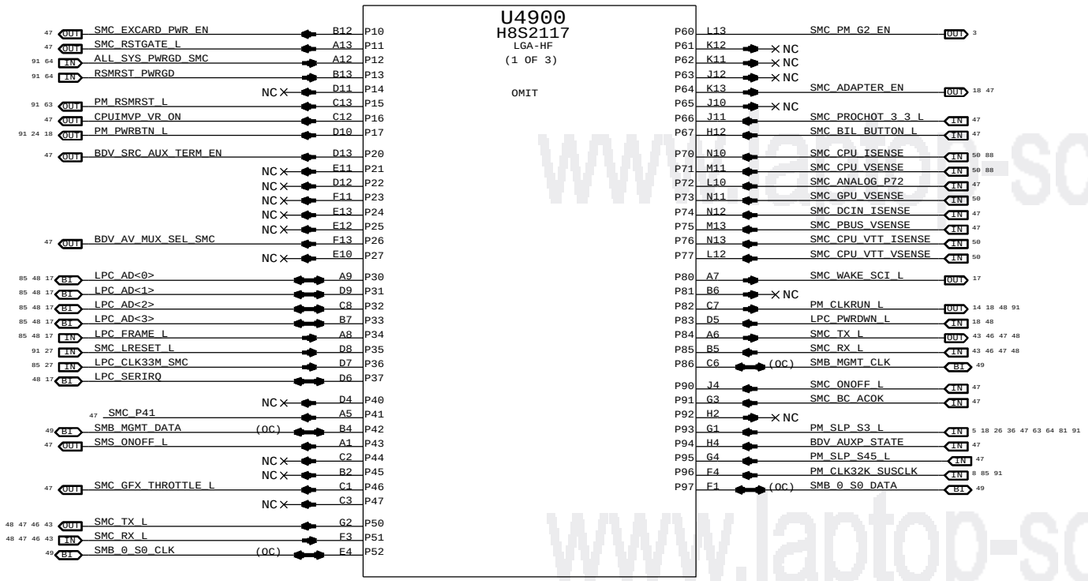
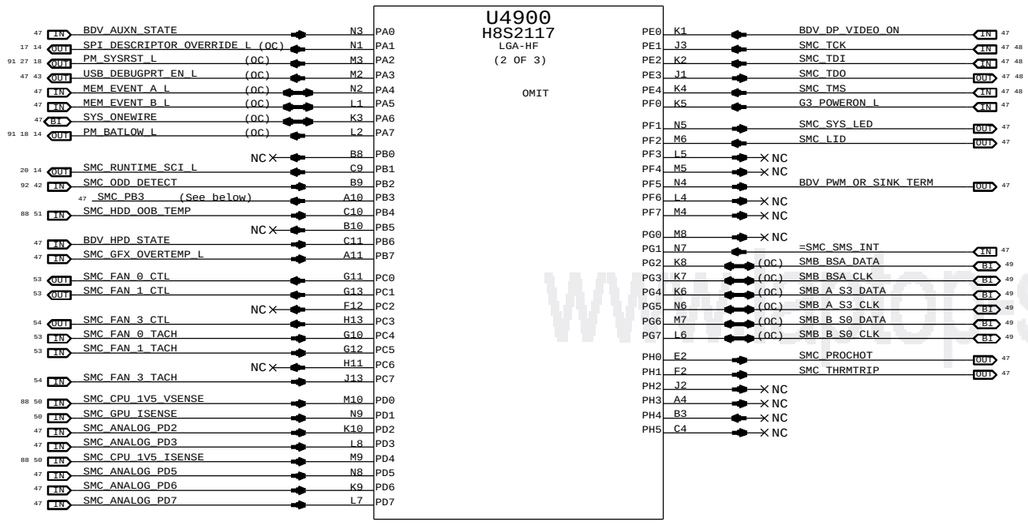
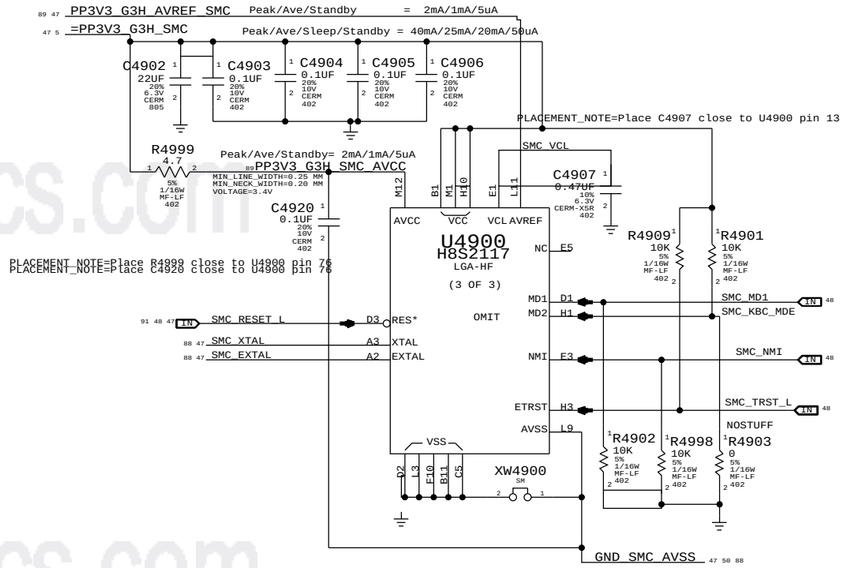
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: SMC

Apple Inc.

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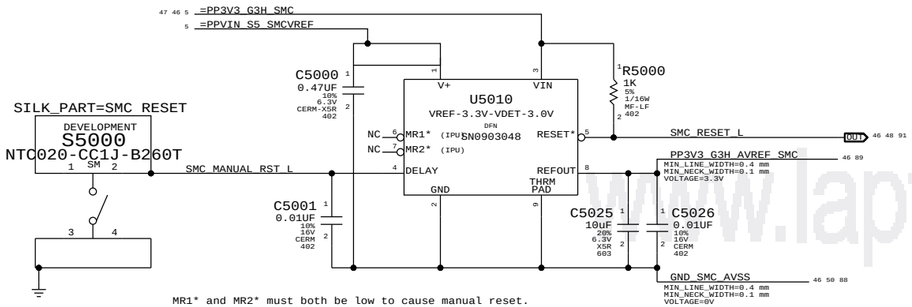
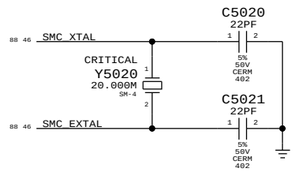
SMC Reset "Button", Supervisor & AVREF Supply



MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

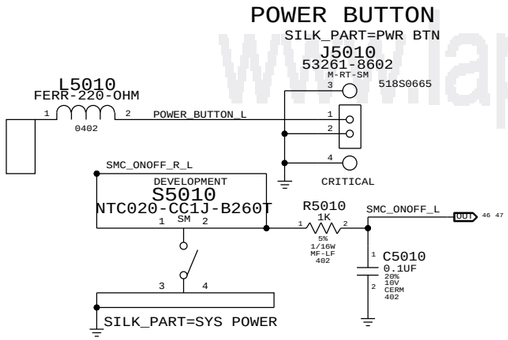
NOTE: Internal pull-ups are to VIN, not V+.

SMC Crystal Circuit

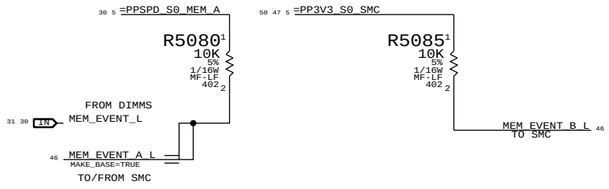


POWER BUTTON

SILK_PART=PWR BTN



MEM_EVENT



MISC. SIGNAL ALIASES

47 46 SMC_GFX_OVERTEMP_L — MXM_ALERT_L 75 (MAKE_BASE=TRUE)

46 SMC_GFX_THROTTLE_L — MXM_PWR_LEVEL 75 (MAKE_BASE=TRUE)

46 CPUIMVP_VR_ON — SMC_DELAYED_PWRGD 64 91 (MAKE_BASE=TRUE)

UNUSED PORT 7 ANALOG SENSORS

46 SMC_ANALOG_P72
46 SMC_DCIN_ISENSE
46 SMC_PBUS_VSENSE
SMC_UNUSED_ADC_PORT7 (MAKE_BASE=TRUE)
R5002 10K 5% 1/16W MF-LF 402

UNUSED PORT D ANALOG (INTERNAL PULLUPS)

46 SMC_ANALOG_PD2 — NC_SMC_ANALOG_PD2 (MAKE_BASE=TRUE, NO_TEST=TRUE)
46 SMC_ANALOG_PD3 — NC_SMC_ANALOG_PD3 (MAKE_BASE=TRUE, NO_TEST=TRUE)
46 SMC_ANALOG_PD5 — NC_SMC_ANALOG_PD5 (MAKE_BASE=TRUE, NO_TEST=TRUE)
46 SMC_ANALOG_PD6 — NC_SMC_ANALOG_PD6 (MAKE_BASE=TRUE, NO_TEST=TRUE)
46 SMC_ANALOG_PD7 — NC_SMC_ANALOG_PD7 (MAKE_BASE=TRUE, NO_TEST=TRUE)

UNUSED TP/NC ALIASES

46 SMC_EXCARD_PWR_EN — TP_SMC_EXCARD_PWR_EN (MAKE_BASE=TRUE)
46 SMS_ONOFF_L — TP_SMS_ONOFF_L (MAKE_BASE=TRUE)
46 SMC_RSTGATE_L — TP_SMC_RSTGATE_L (MAKE_BASE=TRUE)
46 SMC_P41 — TP_SMC_P41 (MAKE_BASE=TRUE)
46 SMC_SYS_LED — TP_SMC_SYS_LED (MAKE_BASE=TRUE)
46 SMC_PB3 — TP_SMC_PB3 (MAKE_BASE=TRUE)

46 BDV_PWM_OR_SINK_TERM — TP_BDV_PWM_OR_SINK_TERM (MAKE_BASE=TRUE)
46 BDV_SRC_AUX_TERM_EN — TP_BDV_SRC_AUX_TERM_EN (MAKE_BASE=TRUE)
46 BDV_AV_MUX_SEL_SMC — TP_BDV_AV_MUX_SEL_SMC (MAKE_BASE=TRUE)

TIES OFF AUDIO DETECT CIRCUIT WHEN BIDIVI IS NOT USED

61 BDV_AV_MUX_SEL — GND_AUDIO_CODEC 56 57 61 62 (MAKE_BASE=TRUE)

=PP3V3_G3H_SMC

47 46 5

47 46 SMC_ONOFF_L	R5032	10K	5%	1/16W	MF-LF	402	
48 46 43 SMC_TX_L	R5035	10K	5%	1/16W	MF-LF	402	
48 46 43 SMC_RX_L	R5036	100K	5%	1/16W	MF-LF	402	
46 SYS_ONEWIRE	R5037	2.0K	5%	1/16W	MF-LF	402	
48 46 SMC_TMS	R5039	10K	5%	1/16W	MF-LF	402	
48 46 SMC_TDO	R5040	10K	5%	1/16W	MF-LF	402	
48 46 SMC_TDI	R5041	10K	5%	1/16W	MF-LF	402	
48 46 SMC_TCK	R5042	10K	5%	1/16W	MF-LF	402	
46 SMC_BIL_BUTTON_L	R5092	10K	5%	1/16W	MF-LF	402	
46 SMC_BC_ACOK	R5047	10K	5%	1/16W	MF-LF	402	
46 18 SMC_ADAPTER_EN	R5049	10K	5%	1/16W	MF-LF	402	
46 43 USB_DEBUGPRT_EN_L	R5098	10K	5%	1/16W	MF-LF	402	
46 =SMC_SMS_INT — SMC_SMS_INT (MAKE_BASE=TRUE)	R5091	10K	5%	1/16W	MF-LF	402	
46 SMC_LID	R5087	10K	5%	1/16W	MF-LF	402	
46 G3_POWERON_L	R5086	10K	5%	1/16W	MF-LF	402	
46 BDV_AUXP_STATE	R5060	100K	5%	1/16W	MF-LF	402	
46 BDV_AUXN_STATE	R5061	100K	5%	1/16W	MF-LF	402	
46 BDV_HPD_STATE	R5062	100K	5%	1/16W	MF-LF	402	

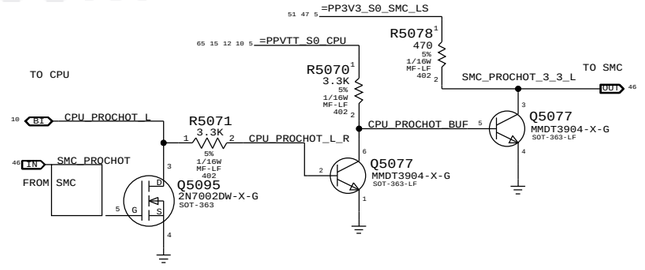
=PP3V3_S0_SMC

50 47 5

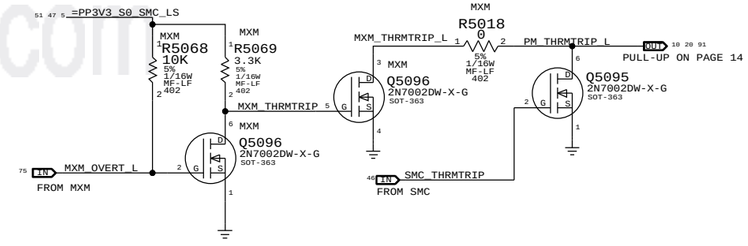
47 46 SMC_GFX_OVERTEMP_L — R5099 10K 5% 1/16W MF-LF 402

46 BDV_DP_VIDEO_ON	R5063	100K	5%	1/16W	MF-LF	402	
91 81 64 63 46 36 26 18 5 PM_SLP_S3_L	R5094	100K	5%	1/16W	MF-LF	402	
PM_SLP_S5_L	R5090	100K	5%	1/16W	MF-LF	402	
91 18 PM_SLP_S4_L	R5089	100K	5%	1/16W	MF-LF	402	
46 PM_SLP_S45_L							

SMC PROCHOT 3.3V LEVEL SHIFTING



SMC & MXM THERMTRIP LEVEL SHIFTING



SYNC_MASTER=K74_MASTER	SYNC_DATE=N/A
PAGE TITLE: SMC Support	
Apple Inc.	DRAWING NUMBER: 051-8337 SIZE: D
	REVISION: A.0.0
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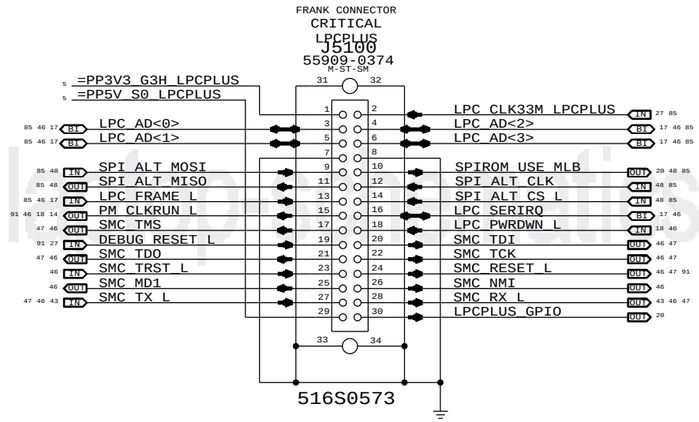
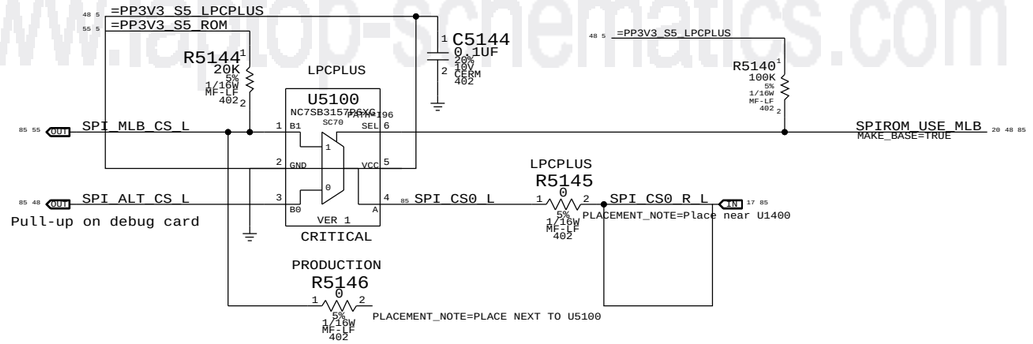
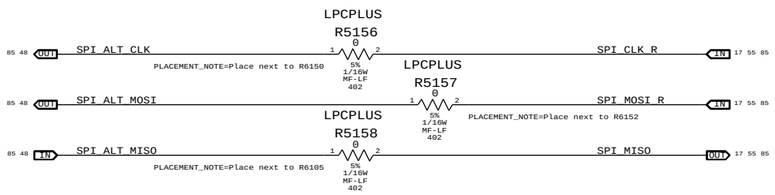
LPC+SPI Connector



Alternate SPI ROM Support



SPI Bus Series Resistance Option



SYNC_MASTER=K23F SYNC_DATE=11/30/2009

PAGE TITLE: LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

BRANCH:

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PCH "SMBUS" CONNECTIONS

49 5 =PP3V3_S0_SMBUS

R5208 1 2.2K 5% 1/16W MF-LF 402 2
R5209 1 2.2K 5% 1/16W MF-LF 402 2

PCH
U1800
(MASTER)

88 17 SMBUS_PCH_CLK MAKE_BASE=TRUE
88 17 SMBUS_PCH_DATA MAKE_BASE=TRUE

MEMORY A DIMMS
J3100-A/B
(Write: 0xA0 Read: 0xA1)
(WRITE: 0XA2 READ: 0XA5)
=I2C_SODIMMA_SCL 30
=I2C_SODIMMA_SDA 30

MEMORY B DIMMS
J3200-A/B
(WRITE: 0XA4 READ: 0XA3)
(WRITE: 0XA6 READ: 0XA7)
=I2C_SODIMMB_SCL 31
=I2C_SODIMMB_SDA 31

MIKEY
U6806
(WRITE: 0X72 READ: 0X73)
=I2C_AUDIO_SCL 62
=I2C_AUDIO_SDA 62

XDP
J2500
(MASTER)
24 =SMBUS_XDP_SCL
24 =SMBUS_XDP_SDA

CK505
U2600
(WRITE: 0XD2 READ: 0XD3)
=SMBUS_CK505_SCL 25
=SMBUS_CK505_SDA 25

MEMORY VREF DAC
U2900
(WRITE: 0X98 READ: 0X99)
=I2C_VREFDACS_SCL 28
=I2C_VREFDACS_SDA 28

MEMORY VREF MARGIN
U2910
(WRITE: 0X30 READ: 0X31)
=I2C_PCA9557D_SCL 28
=I2C_PCA9557D_SDA 28

PCH "SML 1" CONNECTIONS

49 5 =PP3V3_S0_SMBUS

NOSTUFF R5204 1 8.2K 5% 1/16W MF-LF 402 2
NOSTUFF R5205 1 8.2K 5% 1/16W MF-LF 402 2
R5206 0 5% 1/16W MF-LF 402 1 2
R5207 0 5% 1/16W MF-LF 402 1 2

PCH
U1800
(SLAVE)
(WRITE: 0X88 READ: 0X89)
88 17 SML_PCH_1_CLK MAKE_BASE=TRUE
88 17 SML_PCH_1_DATA MAKE_BASE=TRUE

PCH "SML 0" CONNECTIONS

49 5 =PP3V3_S0_SMBUS

R5202 1 8.2K 5% 1/16W MF-LF 402 2
R5203 1 8.2K 5% 1/16W MF-LF 402 2

PCH
U1800
(MASTER)
88 17 SML_PCH_0_CLK MAKE_BASE=TRUE
88 17 SML_PCH_0_DATA MAKE_BASE=TRUE

SMC "B" SMBus Connections

BUS B CAN USE EITHER INTERNAL SMC CHANNEL 0 OR 1, K74 CHOOSES 0

5 =PP3V3_S0_SMBUS_SMC_B_S0

R5260 1 2.2K 5% 1/16W MF-LF 402 2
R5261 1 2.2K 5% 1/16W MF-LF 402 2

SMC
U4900
(MASTER)
46 SMB_B_S0_CLK
46 SMB_B_S0_DATA
88 SMBUS_SMC_B_S0_SCL MAKE_BASE=TRUE
88 SMBUS_SMC_B_S0_SDA MAKE_BASE=TRUE

AC/DC PS TEMPS
EMC1403-[1,2]: ACDC THRU J600
(WRITE: 0X98 OR 0X9A, READ: 0X99 OR 0X9B)
3 SENSE POINTS - PRIMARY, SECONDARY, AMB
=SMB_ACDC_SCL 5
=SMB_ACDC_SDA 5

AC/DC PS POWER
INA219: ACDC THRU J600
(WRITE: 0X80, READ: 0X81))
OUTPUT VOLTAGE, CURRENT, POWER

SMC "0" SMBus Connections

USES INTERNAL SMC CONTROLLER CHANNEL 0 ONLY

5 =PP3V3_S0_SMBUS_SMC_0_S0

R5250 1 4.7K 5% 1/16W MF-LF 402 2
R5251 1 4.7K 5% 1/16W MF-LF 402 2

SMC
U4900
(MASTER)
46 SMB_0_S0_CLK
46 SMB_0_S0_DATA
88 SMBUS_SMC_0_S0_SCL MAKE_BASE=TRUE
88 SMBUS_SMC_0_S0_SDA MAKE_BASE=TRUE

Also reserve 0x56 and 0x32 per spec

MXM TEMP
GPU ON CARD - J8400
NV INSIDE (WRITE: 0X9E READ: 0X9F)
MXM CARD (WRITE: 0X98 READ: 0X99)
=SMB_MXM_THRM_SCL 75
=SMB_MXM_THRM_SDA 75

HEATSINK TEMPS
EMC1414: U5500
(WRITE: 0XD8 READ: 0XD9)
=SMB_SNS1_SCL 52
=SMB_SNS1_SDA 52

AMB,ODD,SKIN TEMPS
TMP423: U5550
(WRITE: 0X9A READ: 0X9B)
=SMB_SNS2_SCL 52
=SMB_SNS2_SDA 52

PCIE MINI-CARD X18 WI-FI MODULE
TMP106: J3400
(WRITE: 0X90 READ: 0X91)
=SMB_MINI_SCL 33
=SMB_MINI_SDA 33

SMC "A" SMBus Connections

NOTE: SMC RMT BUS REMAINS POWERED AND MAY BE ACTIVE IN S3 STATE
BUS A CAN USE EITHER INTERNAL SMC CHANNEL 0 OR 1, K74 CHOOSES 1

5 =PP3V3_S3_SMBUS_SMC_A_S3

R5270 1 4.7K 5% 1/16W MF-LF 402 2
R5271 1 4.7K 5% 1/16W MF-LF 402 2

SMC
U4900
(MASTER)
46 SMB_A_S3_CLK
46 SMB_A_S3_DATA
88 SMBUS_SMC_A_S3_SCL MAKE_BASE=TRUE
88 SMBUS_SMC_A_S3_SDA MAKE_BASE=TRUE

ALS
(WRITE: 0X52 READ: 0X53)
=SMB_ALS_SCL 44 92
=SMB_ALS_SDA 44 92

SMC SLAVE SMBUS "2" CONNECTIONS

USES INTERNAL SMC CONTROLLER CHANNEL 2 ONLY

5 =PP3V3_S0_SMBUS_SMC_BSA

R5280 1 4.7K 5% 1/16W MF-LF 402 2
R5281 1 4.7K 5% 1/16W MF-LF 402 2

SMC
U4900
(SLAVE)
46 SMB_BSA_CLK
46 SMB_BSA_DATA
88 SMBUS_SMC_BSA_SCL MAKE_BASE=TRUE
88 SMBUS_SMC_BSA_SDA MAKE_BASE=TRUE

DISPLAY TCON
DP RX MASTER FOR MCCS
SMC SLAVE ADDRESS TBD
=SMB_DP_TCON_SCL 78
=SMB_DP_TCON_SDA 78

SMC "MANAGEMENT" SMBUS (BUS 1)

USES INTERNAL SMC CONTROLLER CHANNEL 1 ONLY

5 =PP3V3_S0_SMBUS_SMC_MGMT

R5290 1 4.7K 5% 1/16W MF-LF 402 2
R5291 1 4.7K 5% 1/16W MF-LF 402 2

SMC
U4900
(MASTER)
46 SMB_MGMT_CLK
46 SMB_MGMT_DATA
88 SMBUS_SMC_MGMT_SCL MAKE_BASE=TRUE
88 SMBUS_SMC_MGMT_SDA MAKE_BASE=TRUE

DP TX REDRIVER
U9180
(WRITE: 0X9C, READ: 0X9D)
=I2C_DP_DRV_SCL 79
=I2C_DP_DRV_SDA 79

SYNC_MASTER=DAVE SYNC_DATE=01/07/2010

PAGE TITLE: SMBus Connections

Apple Inc.

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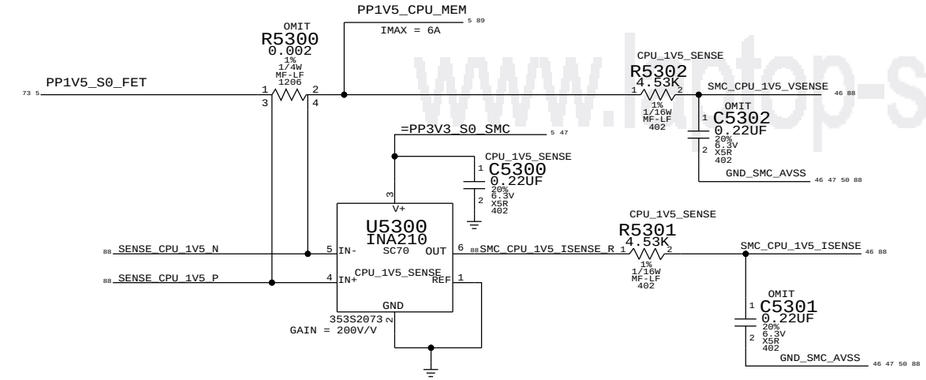
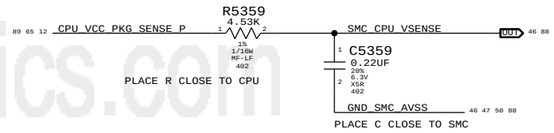
CPU 1.5V CURRENT SENSE

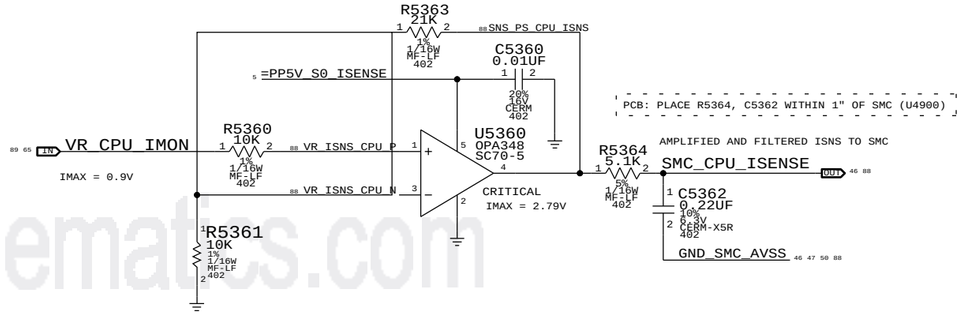


CPU 1.5V VOLTAGE SENSE

CPU Voltage Sense / Filter

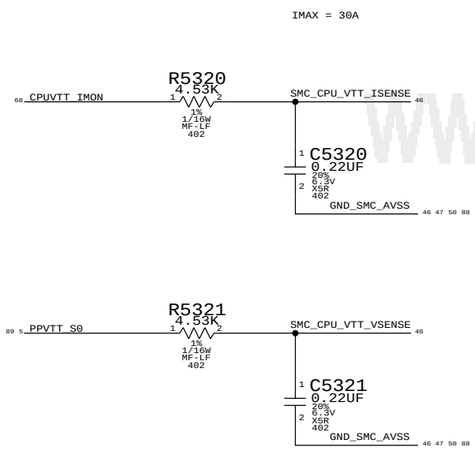


CPU CURRENT SENSE AMP & FILTER

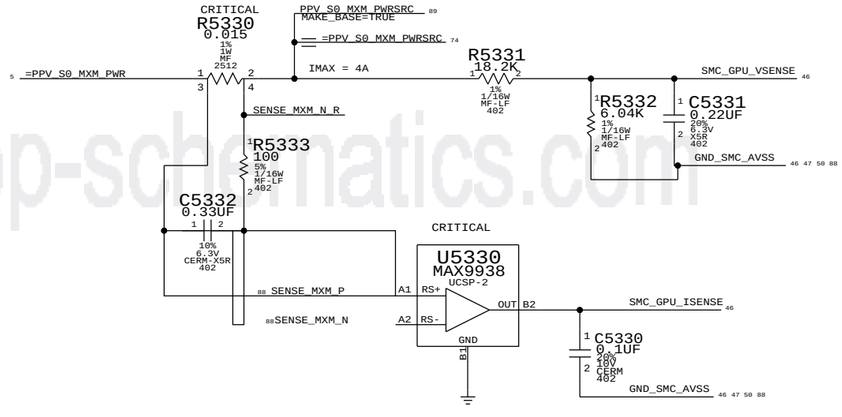


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
104S0018	1	RES,2 MILLIOHM,1206	R5300	CPU_1V5_SENSE
101S0414	1	RES,0 OHM,1206,20 MILLIOHM MAX	R5300	PRODUCTION
132S0080	2	CAP,0.22UF,402	C5301,C5302	CPU_1V5_SENSE
116S0004	2	RES,0 OHM,402	C5301,C5302	PRODUCTION

CPU VTT CURRENT SENSE



MXM PWRSRC CURRENT & VOLTAGE SENSE



SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
CPU/GPU POWER SENSE

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D
REVISION A.0.0
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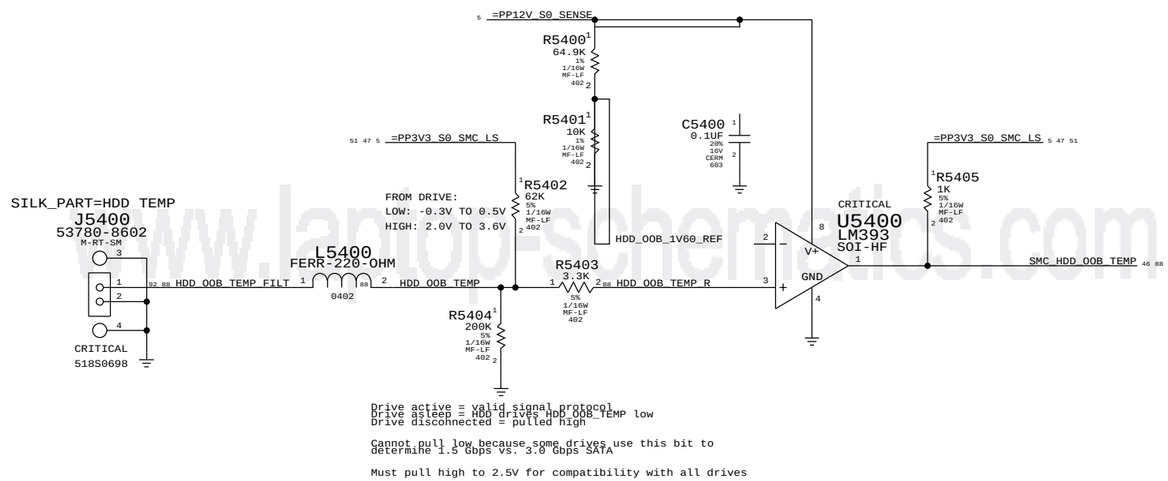
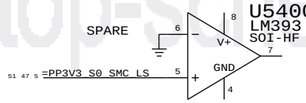
HDD OUT OF BAND TEMPERATURE SENSING LEVEL SHIFTING



Drive active = valid signal protocol
Drive asleep = HDD drives HDD_OOB_TEMP low
Drive disconnected = pulled high

Cannot pull low because some drives use this bit to determine 1.5 Gbps vs. 3.0 Gbps SATA

Must pull high to 2.5V for compatibility with all drives



SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: HDD TEMP SENSE

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

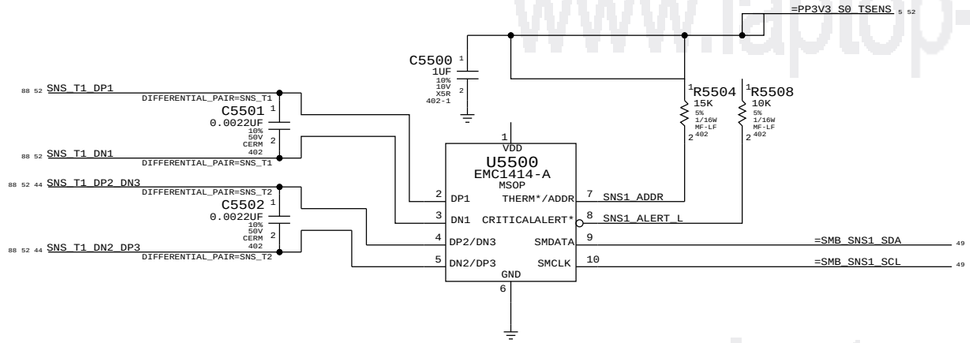
REVISION: A.0.0

BRANCH:

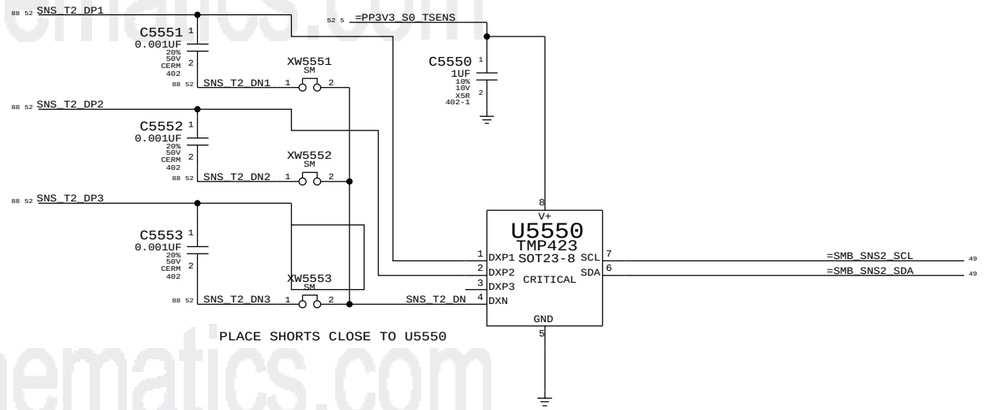
PAGE: 54 OF 110

SHEET: 51 OF 92

REMOTE HEATSINK SENSORS



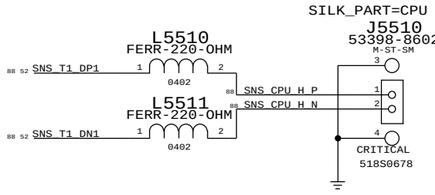
REMOTE SKIN & ODD THERMAL SENSORS



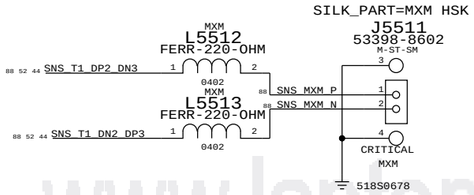
PLACE SHORTS CLOSE TO U5550

PLACE HSK SENSOR CONN. TOP SIDE NEAR MXM OR CPU

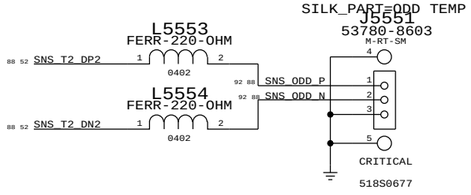
SILK_PART=CPU HSK



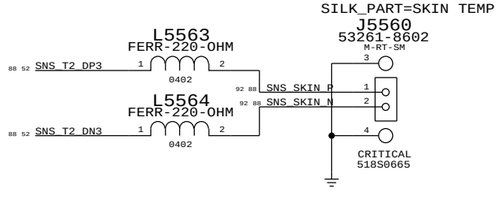
SILK_PART=MXM HSK



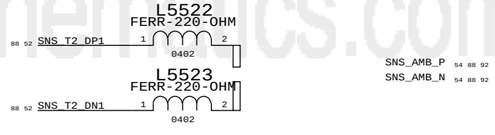
SILK_PART=ODD TEMP



SILK_PART=SKIN TEMP



AMBIENT SENSE CONNECTOR COMBINED WITH CPU FAN



SYNC_MASTER=NICK SYNC_DATE=11/06/2009

PAGE TITLE: REMOTE TEMP/POWER SENSORS

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

BRANCH:

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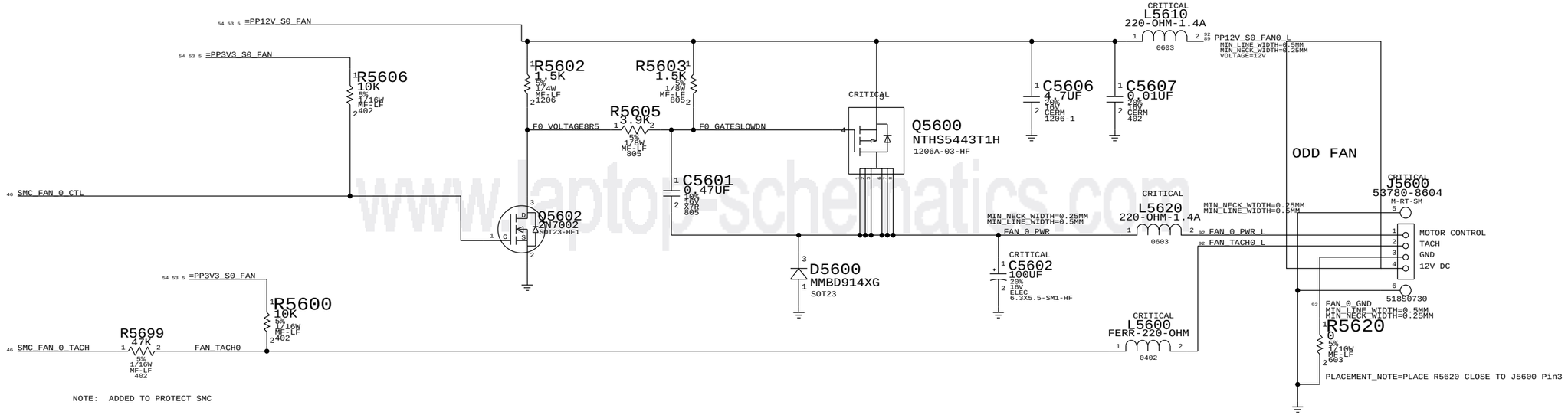
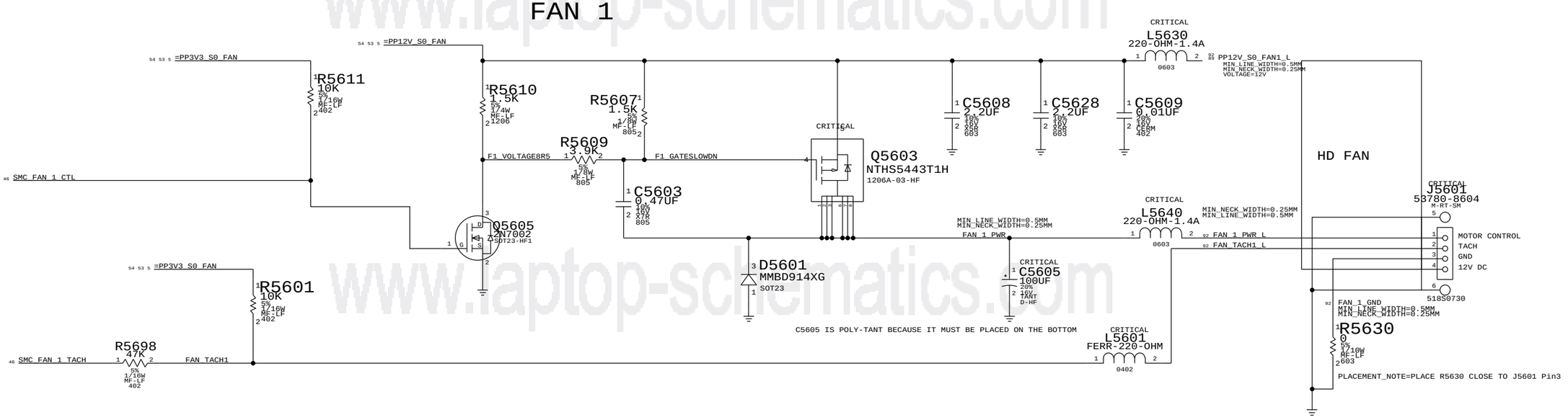
FAN 0



NOTE: ADDED TO PROTECT SMC

FAN 1



C5605 IS POLY-TANT BECAUSE IT MUST BE PLACED ON THE BOTTOM

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: HD AND OD FAN

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

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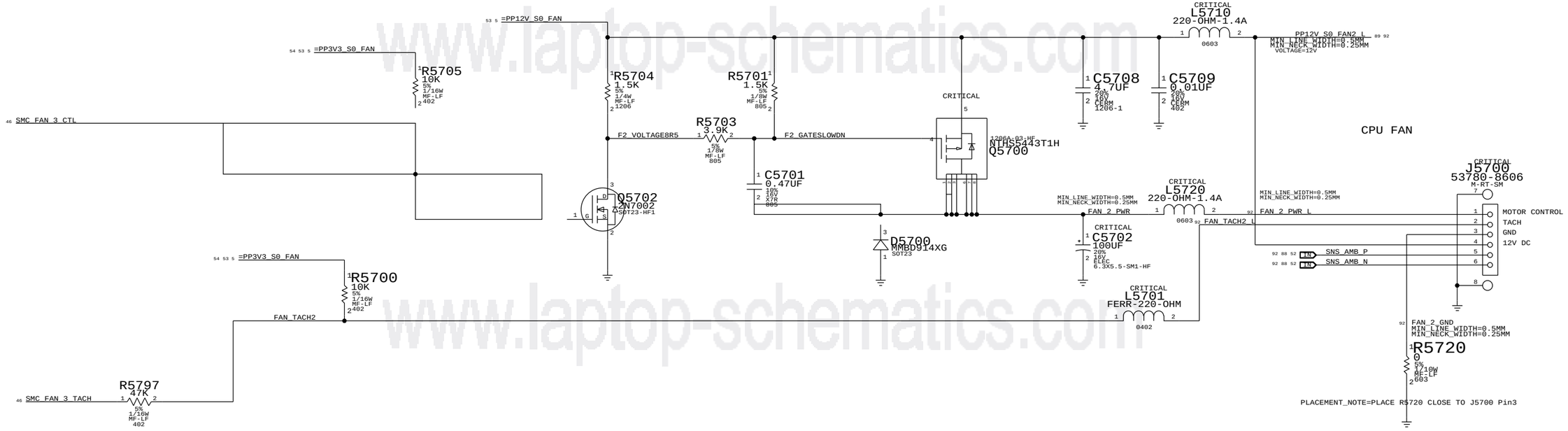
FAN 2 UNUSED

FAN 3



SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
CPU FAN & AMBIENT SENSE

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D
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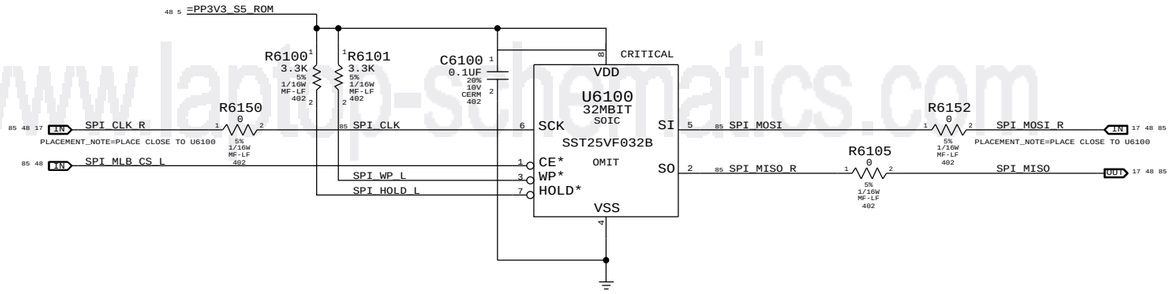

SYNC_MASTER=K23F SYNC_DATE=11/30/2009

PAGE TITLE
SPI ROM

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D
REVISION A.0.0
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AUDIO CODEC
APPLE P/N 353S2592

VD MUST BE LESS THAN OR EQUAL TO VL_HD

=PP1V5_S0_AUD_DIG

C6203 4.7UF 20% 4V X5R 402
C6258 0.47UF 10% 16V X5R 402
C6260 10UF 20% 16V POLY-TANT CASE-B2-SM
C6204 10UF 20% 6.3V X5R 603
C6205 10UF 20% 6.3V X5R 603
C6261 0.47UF 10% 16V X5R 402
C6262 10UF 20% 16V POLY-TANT CASE-B2-SM
C6259 1UF 10% 16V X5R 402-1
C6264 0.47UF 10% 16V X5R 402
C6265 0.47UF 10% 16V X5R 402
C6213 10UF 20% 6.3V X5R 603

=PP5V_S0_AUDIO
=PP3V3_S0_AUDIO
PP4V5_AUDIO_ANALOG (VOLTAGE=4.5V, MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.10MM)
GND_AUDIO_HP_AMP_L
GND_AUDIO_CODEC

GND_AUDIO_HP_AMP_L
PP4V5_AUDIO_ANALOG
R6255 2.67K 1% 1/10W MF-LF 402

U6201 CS4206ACNZC QFN

VBIAS_DAC	29	VBIAS_DAC	
CS4206_FP	44	VHP_FILT+	CRITICAL
CS4206_FN	41	VHP_FILT-	
	9	VD	
	24	VA_REF	
	46	VA_HP	
	25	VA	
	38	HPOUT_L	CRITICAL
	40	HPOUT_R	
	39	HPREF	
NC TP_AUD_GPIO0	2	GPIO0/DMIC_SDA1	
NC TP_AUD_GPIO_1	12	GPIO1/DMIC_SDA2	
NC TP_AUD_GPIO_2	14	GPIO2	/SPDIF_OUT2
NC AUD_GPIO_3	15	GPIO3	
AUD_SENSE_A	13	SENSE_A	
CS4206_FLYP	45	FLYP	
CS4206_FLYC	43	FLYC	
	42	FLYN	
CS4206_FLYN	3	VL_HD	
	1	VL_IF	
		LINEOUT_L1+	
		LINEOUT_L1-	
		LINEOUT_R1+	
		LINEOUT_R1-	
		LINEOUT_L2+	
		LINEOUT_L2-	
		LINEOUT_R2+	
		LINEOUT_R2-	
	16	MICBIAS	
CS4206_VCOM	28	VCOM	
	21	LINEIN_L+	
	22	LINEIN_C-	
	23	LINEIN_R+	
	18	MICIN_L+	
	17	MICIN_L-	
	19	MICIN_R+	
	20	MICIN_R-	
CS4206_VREF_ADC	27	VREF+_ADC	
	4	DMIC_SCL	
	6	BITCLK	
	10	SYNC	
	8	SDI	
	5	SDO	
	11	RESET*	
	47	SPDIF_IN	
	48	SPDIF_OUT	
	7	DGND	
	49	THRM_PAD	
	26	AGND	

MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.1MM

AUD_HP_L
AUD_HP_R
AUD_HP_PORT_REF
AUD_LO1_P_L
AUD_LO1_N_L
AUD_LO1_P_R
AUD_LO1_N_R
AUD_LO2_P_L
AUD_LO2_N_L
AUD_LO2_P_R
AUD_LO2_N_R
AUD_CODEC_MICBIAS
AUD_LI_P_L
AUD_LI_COM
AUD_LI_P_R
AUD_MIC_INP_L
AUD_MIC_INN_L
AUD_MIC_INP_R
AUD_MIC_INN_R
TP_AUD_DMIC_CLK NC
CS4206_VREF_ADC NC

PLACE TP FOR ALL HDA SIGNALS NEAR CODEC

HDA_BIT_CLK
HDA_SYNC
HDA_SDIN0
HDA_SDOUT
HDA_RST_L
AUD_SPDIF_IN_CODEC
AUD_SPDIF_OUT

R6254 22 5% 1/16W MF-LF 402 — AUD_SDI_R
R6257 22 5% 1/16W MF-LF 402 — AUD_SPDIF_CHIP
R6295 100K 1% 1/16W MF-LF 402
R6263 NOSTUFF 0 5% 1/16W MF-LF 402
R6267 NOSTUFF 100K 5% 1/16W MF-LF 402

C6211 CRITICAL 1UF 10% 25V TANT CASE-P3-HF
C6263 CRITICAL 10UF 20% 16V POLY-TANT CASE-B2-SM

GND_AUDIO_CODEC
MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

HP OUT ZOBEL NETWORK

MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM — AUD_HP_L
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM — AUD_HP_R

C6298 0.1UF 10% 16V X7R-CERM 402
C6297 0.1UF 10% 16V X7R-CERM 402
MIN_LINE_WIDTH=0.30MM MIN_NECK_WIDTH=0.20MM

AUD_Z_R NC
AUD_Z_L NC

R6296 39 5% 1/16W MF-LF 402
R6297 39 5% 1/16W MF-LF 402
MIN_LINE_WIDTH=0.30MM MIN_NECK_WIDTH=0.20MM

GND_AUDIO_HP_AMP_L

APPLE P/N 353S2456
4.5V POWER SUPPLY FOR CODEC

MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.10MM VOLTAGE=4.5V

L6201 FERR-220-OHM 0402
VR6201 TPS71745 SON CRITICAL
MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.10MM VOLTAGE=4.5V

=PP5V_S0_AUDIO — 4V5_REG_IN
R6201 2.21K 1% 1/16W MF-LF 402
=PP3V3_S0_AUDIO
4V5_REG_EN
4V5_NR
PP4V5_AUDIO_ANALOG

C6201 1UF 10% 10V X5R 402-1
C6202 1UF 10% 10V X5R 402-1
C6266 0.1UF 10% 10V X7R-CERM 402
C6207 1UF 10% 10V X5R 402-1

GND_AUDIO_CODEC

XW6201 SM
GND_AUDIO_HP_AMP_L
VOLTAGE=0V

SYNC_MASTER=BREECE	SYNC_DATE=02/02/2010
PAGE TITLE	AUDIO: CODEC/REGULATOR
Apple Inc.	DRAWING NUMBER 051-8337 · SIZE D
	REVISION A.0.0
	BRANCH
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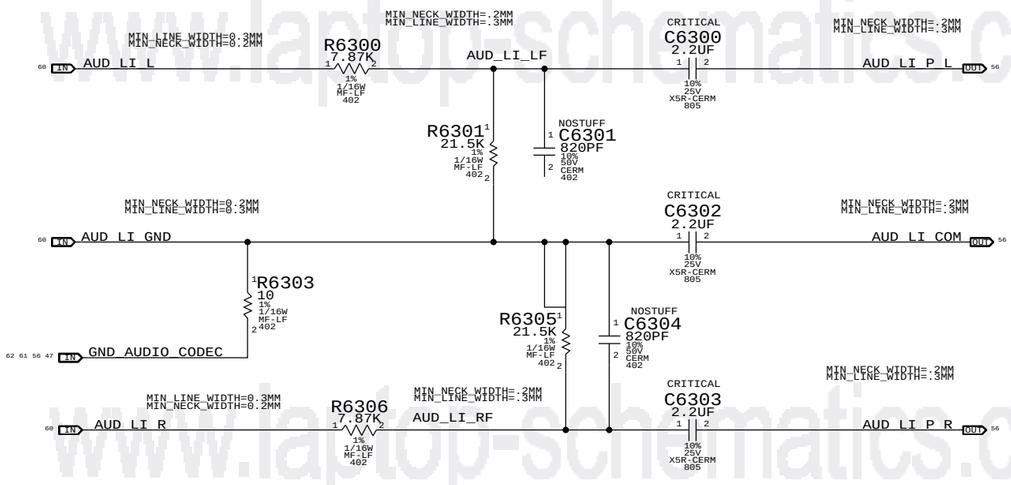
CODEC Nom SE RIN = 20K OHMS
FC = 3.62 HZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS
NET RIN = 18K OHMS



SYNC_MASTER=BREECE SYNC_DATE=02/02/2010

PAGE TITLE
AUDIO: FILTER/BUFFER

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D
REVISION A.0.0
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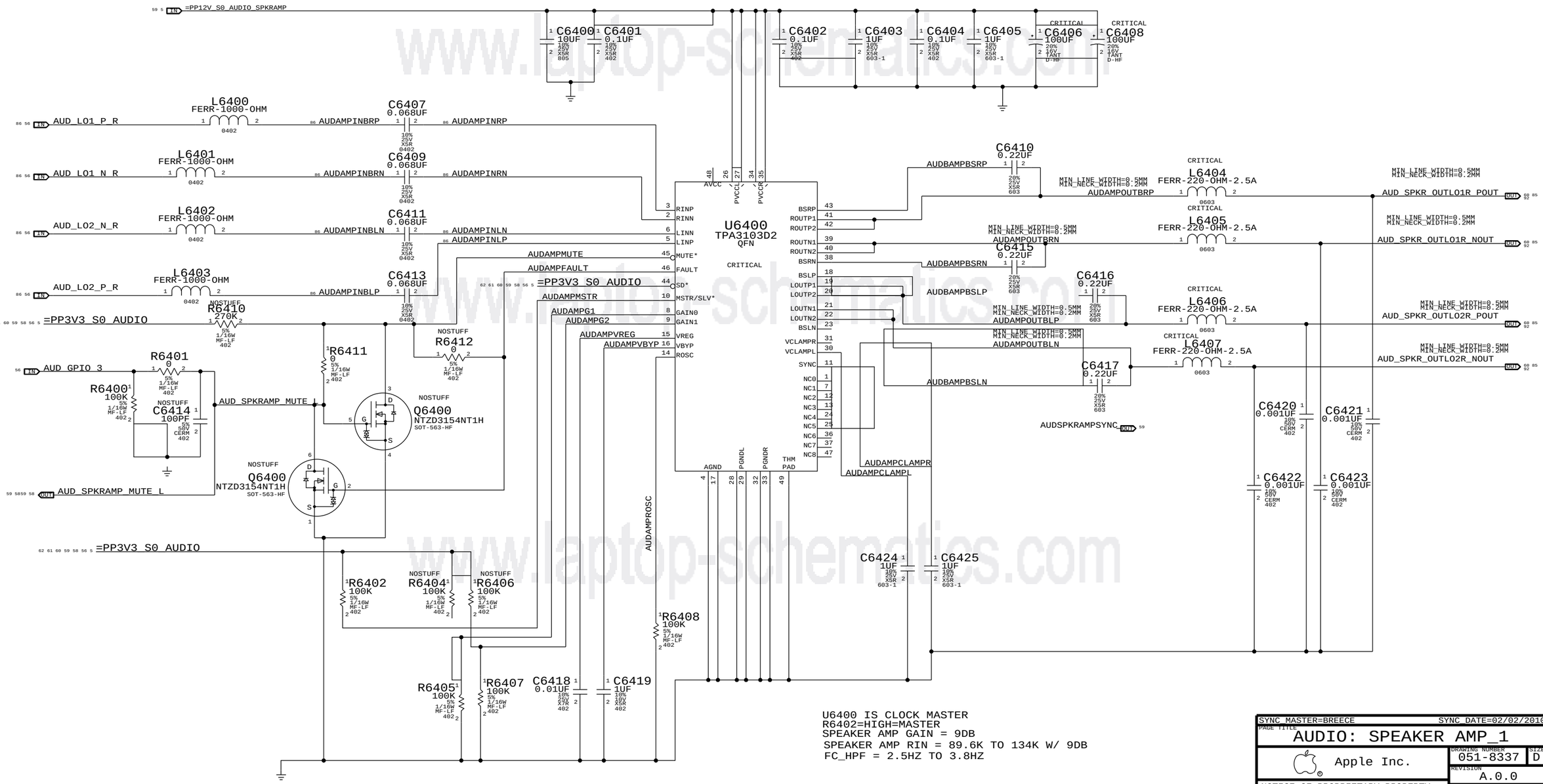
RIGHT CH. SPEAKER AMP
APPLE P/N 353S2768



U6400 IS CLOCK MASTER
R6402=HIGH=MASTER
SPEAKER AMP GAIN = 9DB
SPEAKER AMP RIN = 89.6K TO 134K W/ 9DB
FC_HPF = 2.5HZ TO 3.8HZ

SYNC_MASTER=BREECE SYNC_DATE=02/02/2010

PAGE TITLE
AUDIO: SPEAKER AMP_1

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D
REVISION A.0.0
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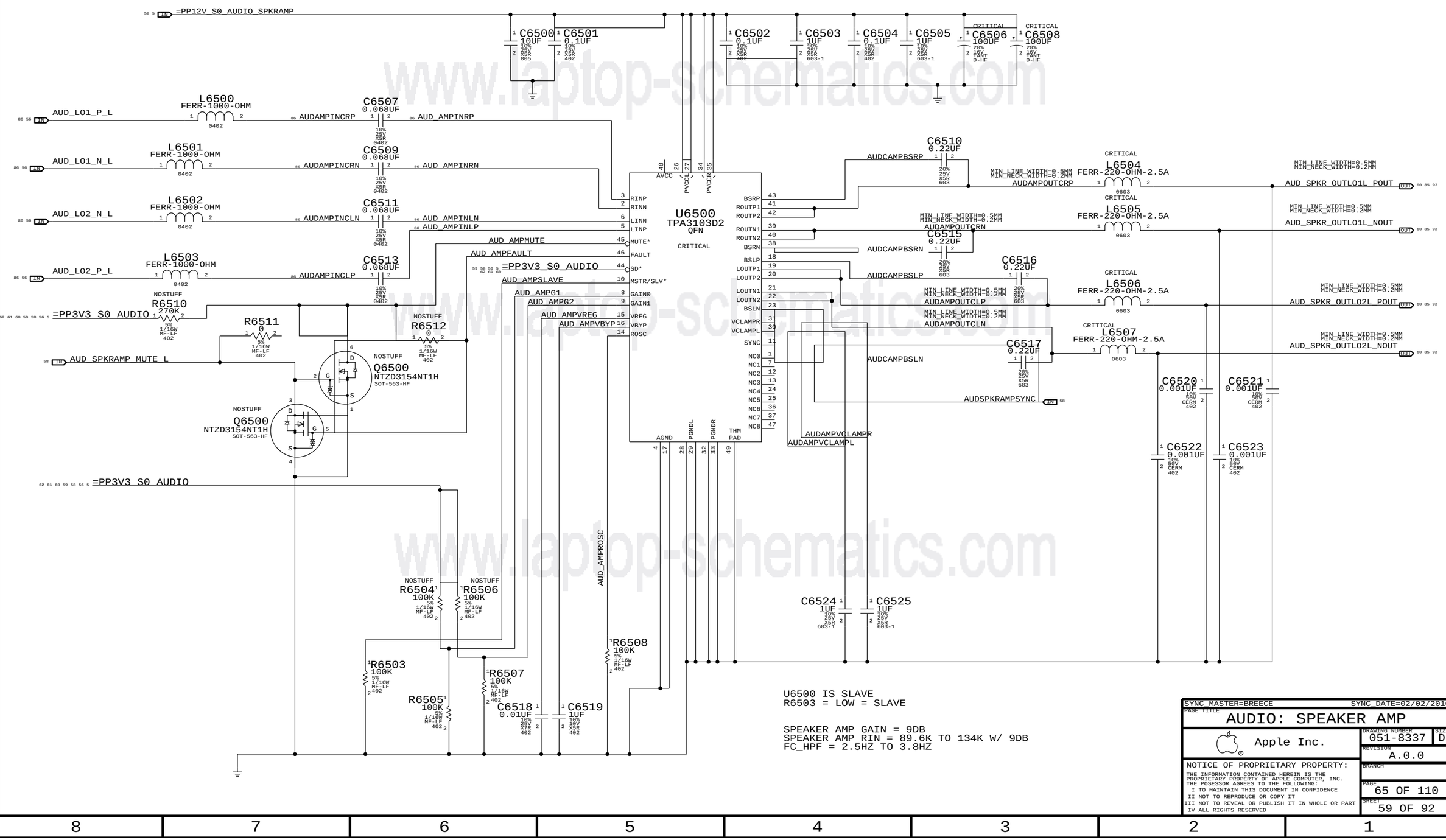
LEFT CH. SPEAKER AMP

APPLE P/N 353S2768



SYNC_MASTER=BREECE SYNC_DATE=02/02/2010

PAGE TITLE: AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

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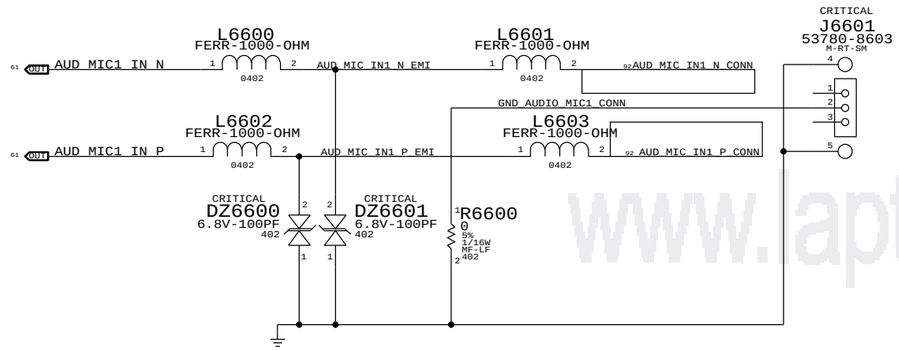
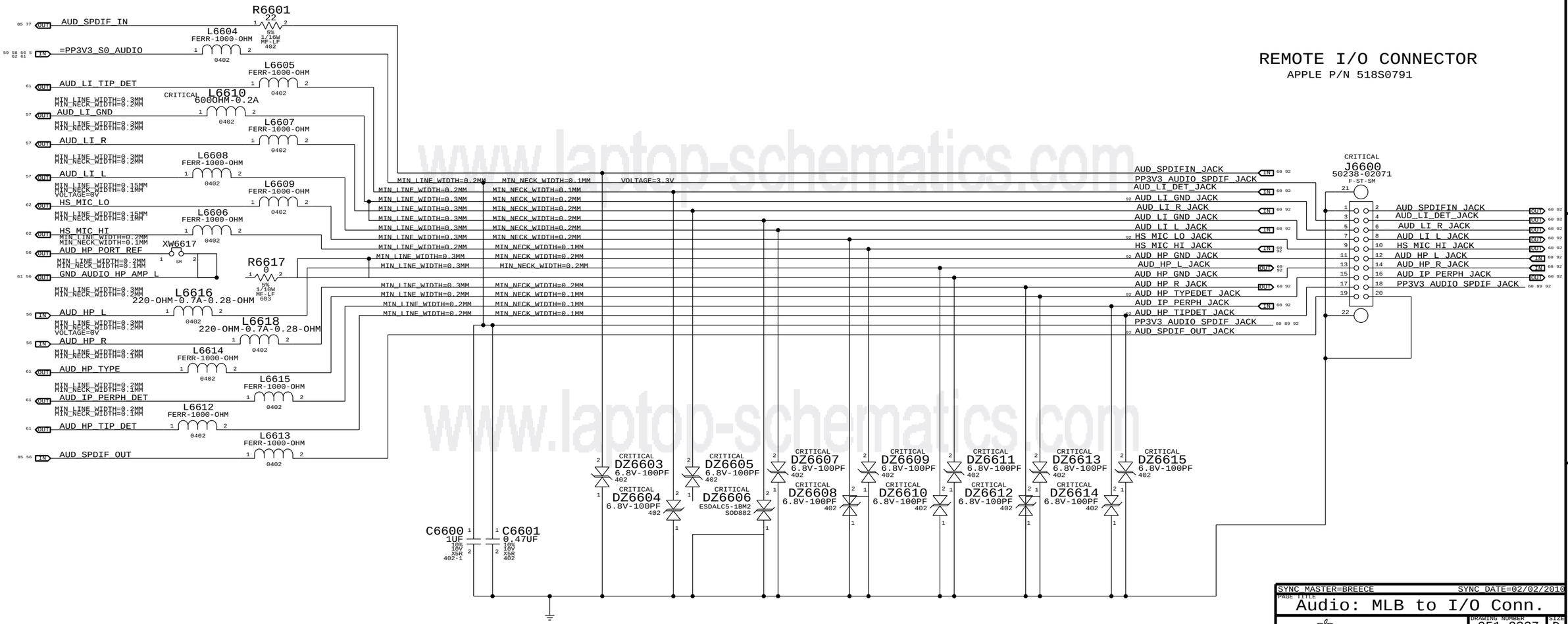
INTERNAL MIC CON
APPLE P/N 518S0677



SPEAKER CABLE CONNECTORS
APPLE P/N 518S0748
APPLE P/N 518S0656

REMOTE I/O CONNECTOR
APPLE P/N 518S0791



SYNC_MASTER=BREECE SYNC_DATE=02/02/2010

PAGE TITLE
Audio: MLB to I/O Conn.

Apple Inc.

DRAWING NUMBER 051-8337
SIZE D
REVISION A.0.0
BRANCH
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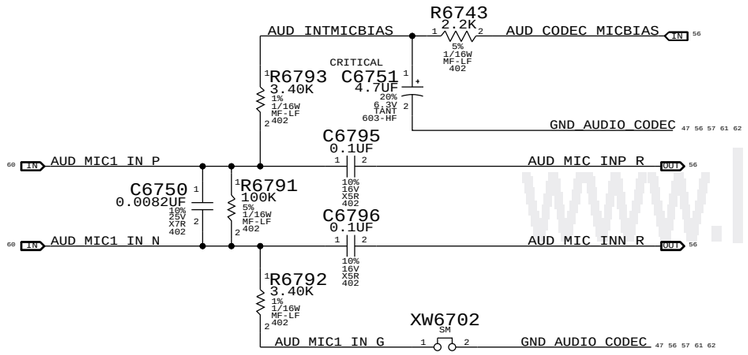
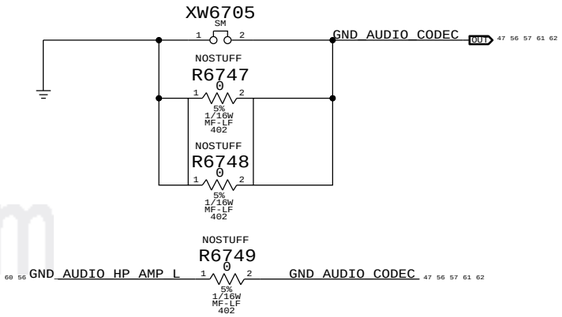
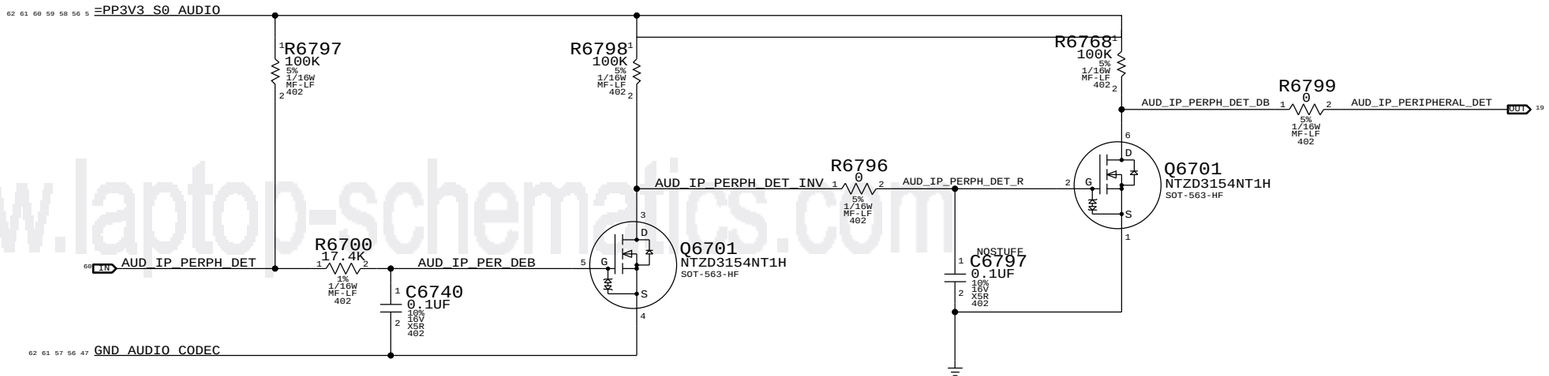
Internal Microphone Impedance Matching



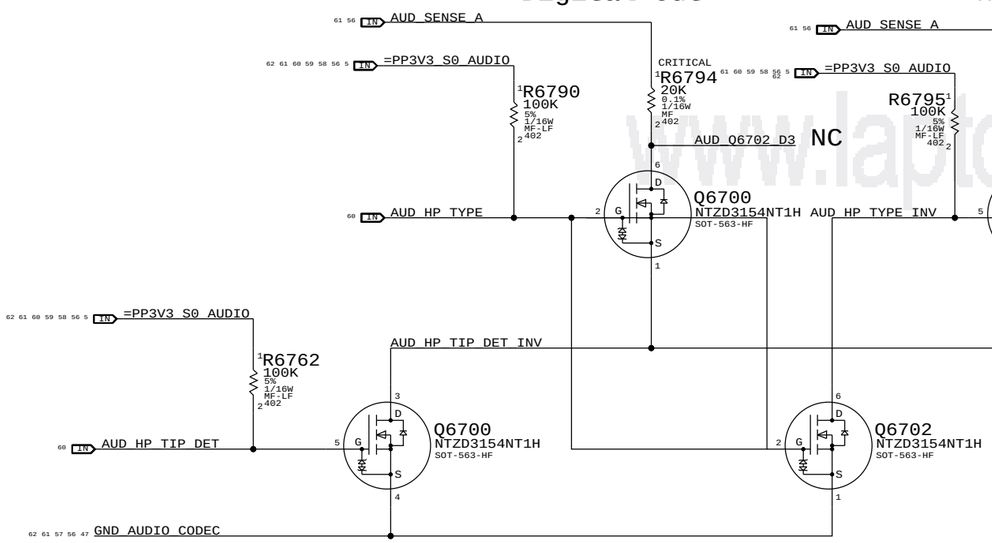
AUDIO STAR GND AND STUFFING OPTIONS



IPHS HS Detect Debounce CKT

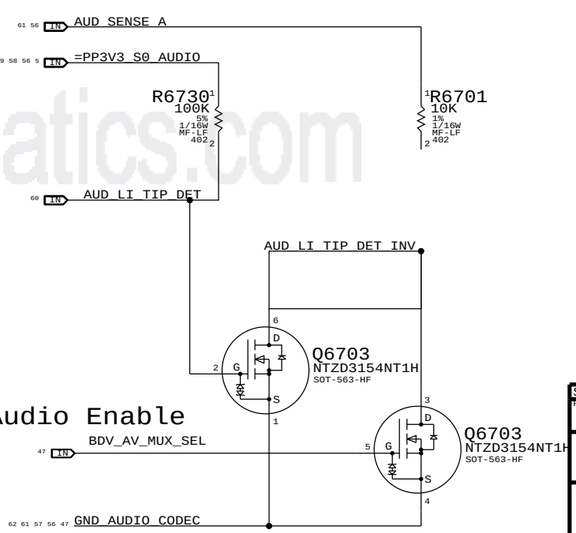


Digital Out



Headphone Out

LI Insert Detect



DP Audio Enable

47 IN BDV_AV_MUX_SEL

SYNC_MASTER=BREECE SYNC_DATE=02/02/2010

PAGE TITLE

AUDIO: Detects/Grounding

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D

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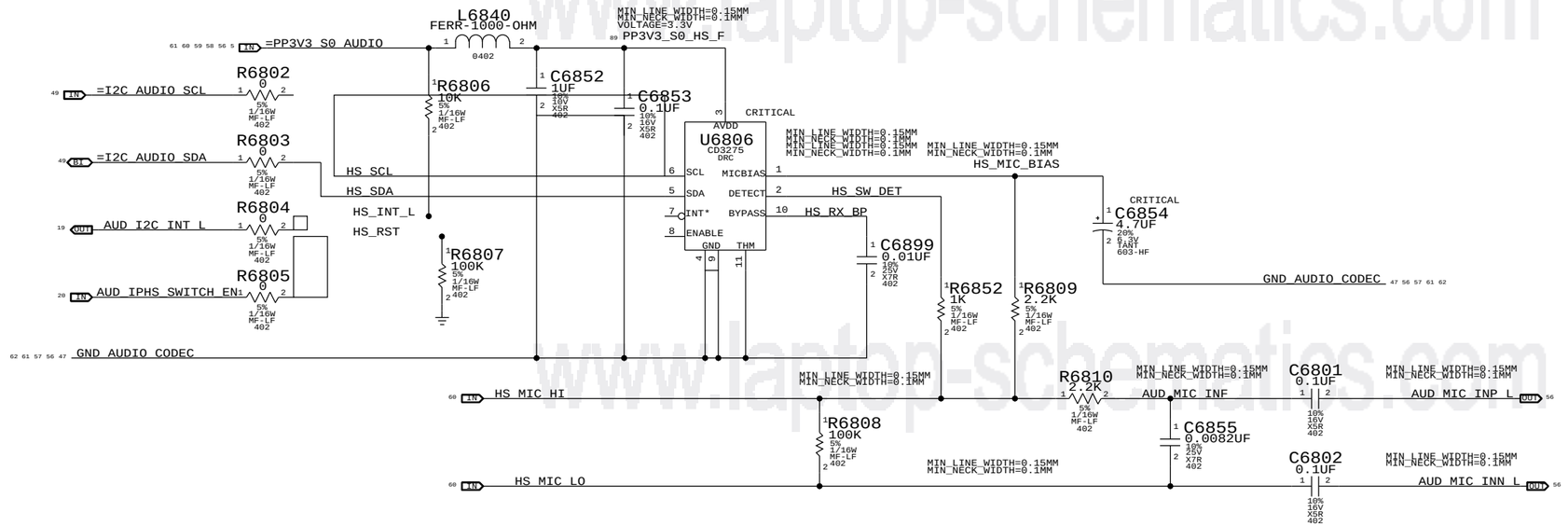
FUNCTION	PIN	CONVERTER	VOLUME	ENABLE/ CNTRL TYPE	DETECT/INTERRUPT
PRIMARY	0X0B	0X04	0X04	GPIO 3	N/A
SECONDARY	0X0A	0X03	0X03	GPIO 3	N/A
HEADPHONES	0X09	0X02	0X02	N/A	0X09 (A)
LINE INPUT	0X0C	0X05	0X05	N/A	LINE IN
BUILT-IN MICROPHONE	0X0D(13,B,RIGHT)	0X06	0X06	MICBIAS 80%	N/A
HEADSET MICROPHONE	0X0D (13,V22,B,LEFT)	0X06	0X06	MIKEY	MIKEY
SPDIF OUT	0X10	0X08	N/A	N/A	0X0D (B)
SPDIF IN	0X0F	0X07	N/A	N/A	N/A
MIKEY	N/A	N/A	N/A	MCP GPIO_38	MCP GPIO_5

MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2256



FLP = 8.82 KHZ
FHP = 80 HZ

SYNC_MASTER=BREECE SYNC_DATE=02/02/2010

PAGE TITLE: AUDIO: Mikey

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

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SLP_S4 ENABLES

State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

R6901 0 5% 1/16W MF-LF 402
PM_RSMRST_L (91 48 IN) → PM_RSMRST_PCH_L (OUT 10 91)

MEMVTT_EN SEQUENCE

=PP3V3_S0_PWRCTL (73 64 63 5)
R6951 10K 5% 1/16W MF-LF 402
R6952 10K 5% 1/16W MF-LF 402
NOSTUFF C6951 100PF 5% 25V C0G 402
DDRVTT_EN (63 71 91)
NOSTUFF C6953 0.1UF 10% 16V X5R 402
VTT_REG_PGOOD_L
Q6911 MMDT3904-X-G SOT-363-LF
R6950 100K 5% 1/16W MF-LF 402
CPUVTT_REG_PGOOD (91 68 64 63 10)
CPUVTT_REG_PGOOD_R
Q6911 MMDT3904-X-G SOT-363-LF
NOSTUFF C6952 0.47UF 10% 6.3V CERM-X5R 402

=PP3V3_S5_PWRCTL (64 63 10 5)
C6910 0.1UF 20% 10V CERM 402
74LVC08 TSSOP-HF U6900 08
PM_SLP_S4_1_L (91 18)
S4_ENABLES
R6911 33 5% 1/16W MF-LF 402 → P3V3S3_EN (73 91) Enable FET
R6912 33 5% 1/16W MF-LF 402 → P5VS3_EN (70 91) ENABLE REGULATOR

=PP3V3_S5_PWRCTL (64 63 10 5)
R6916 100K 5% 1/16W MF-LF 402
R6915 10K 5% 1/16W MF-LF 402
CPU_SKTOCC
CPU_SKTOCC_L (10)
Q6910 2N7002 SOT23-HF
NOSTUFF R6917 0 5% 1/10W MF-LF 402
PLACE TOP SIDE
REWORK TO POWER UP WITH NO CPU

NOSTUFF C6920 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6921 0.47UF 10% 6.3V CERM-X5R 402

=PP5V_S3_PWRCTL (5)
R6910 100K 5% 1/16W MF-LF 402
P5VS3_REG_PGOOD (70) MAKE_BASE=TRUE
NOSTUFF C6924 0.47UF 10% 6.3V CERM-X5R 402
PM_EN_USB_PWR (43)
=DDRREG_EN (71)

SLP_S3 ENABLES

UNUSED
=PP3V3_S5_PWRCTL (64 63 10 5)
74LVC08 TSSOP-HF U6900 08

ME RAILS TIED TO S0 ONLY
PM_SLP_M_L (91 18) — TP_PM_SLP_M_L MAKE_BASE=TRUE

=PP3V3_S5_PWRCTL (64 63 10 5)
PM_SLP_S3_L (91 81 64 47 46 36 26 18 5)
74LVC08 TSSOP-HF U6900 08
(PM_SLP_S3_L_BUF)
PM_SLP_S3_BUF_L MAKE_BASE=TRUE
R6946 33 5% 1/16W MF-LF 402 → P3V3S0_EN (73 91) OUT Enable FET
R6947 33 5% 1/16W MF-LF 402 → P5VS0_EN (73 91) OUT Enable FET
OTHER RAILS ENABLED BY P3V3_S0 AND P5V_S0:
PP1V8_S0 VREG (CPU PLL)
R6944 10K 1% 1/16W MF-LF 402
NOSTUFF R6941 10K 5% 1/16W MF-LF 402
PGOOD_P12V_S0 (64) MAKE_BASE=TRUE
PM_PGOOD_DDRREG_S3 (91 71)
PM_SLP_S3_BUF_L (63)
Enable FET P1V5_S0_EN (73 91)
DDRVTT_EN (63 71 91) Enable regulator
NOSTUFF C6947 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6944 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6941 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6945 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6946 0.47UF 10% 6.3V CERM-X5R 402

=PP3V3_S0_PWRCTL (73 64 63 5)
R6942 10K 5% 1/16W MF-LF 402
PGOOD_P5V_S0 (91 73) MAKE_BASE=TRUE
C6942 1UF 10% 6.3V CERM 402
Enable regulator PCHCORE_REG_EN → PCHCORE VREG (69 91 / 91 69 64) → PCHCORE_REG_PGOOD MAKE_BASE=TRUE → ENABLE FET P1V05_ME_S0_EN
Enable regulator CPUVTT_REG_EN → CPUVTT VREG (68 91 / 91 68 64 63 10) → CPUVTT_REG_PGOOD MAKE_BASE=TRUE → Enable regulator PM_EN_PVCORE_CPU (65) TO ENABLE OF CPU VREG

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A
PAGE TITLE: POWER SEQUENCING ENABLES
Apple Inc.
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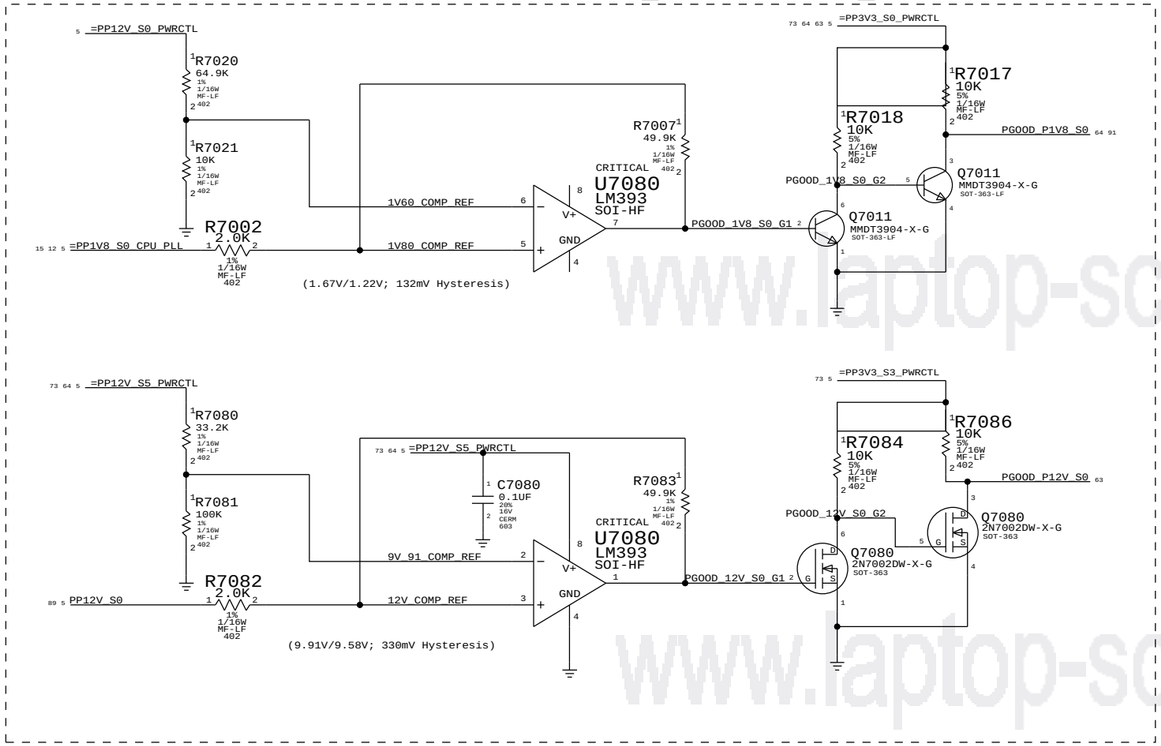
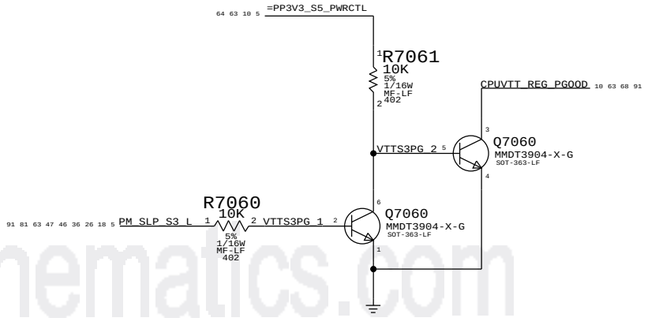
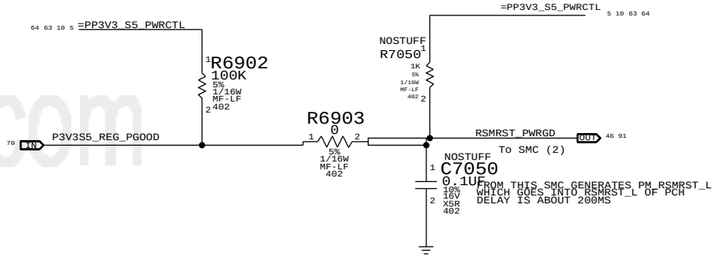
PGOOD COMPARATORS FOR PP1V8_S0 AND PP12V_S0

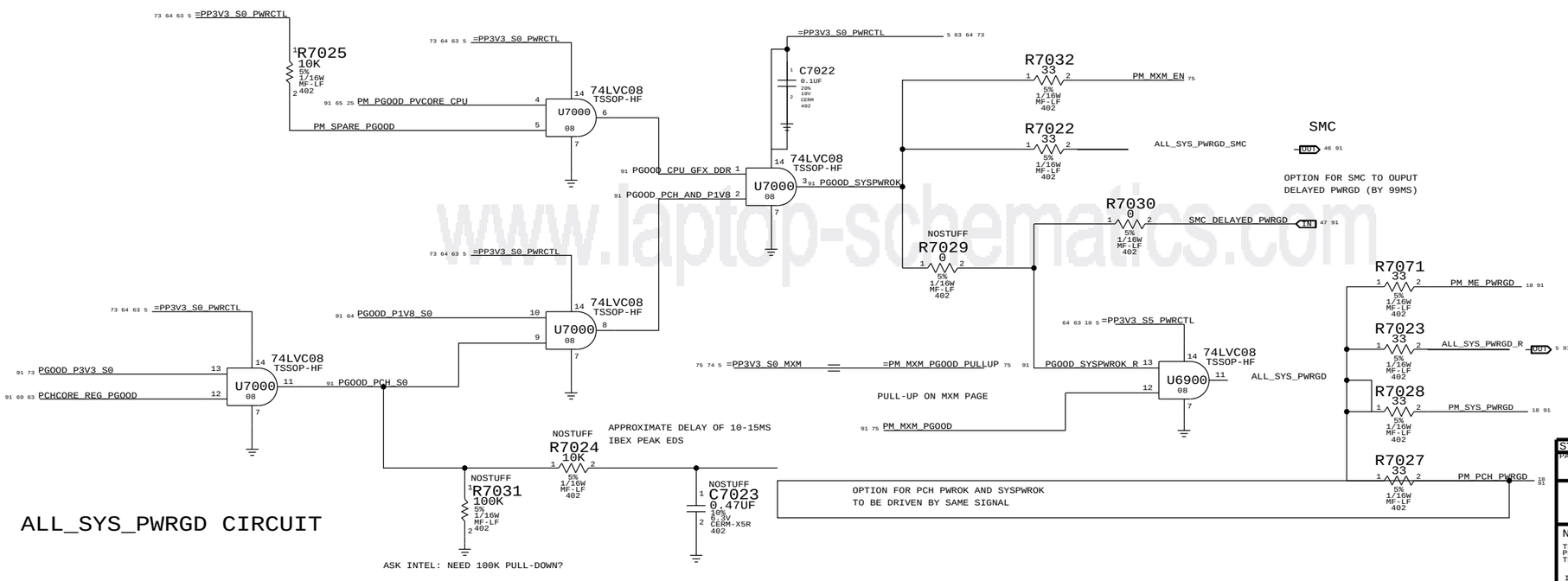


S0 RAILS PGOOD



DISABLE CPUVTT_REG_PGOOD WHEN SLP_S3_L = 0 (PER PIKETON PDG)





ALL_SYS_PWRGD CIRCUIT

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: POWER SEQUENCING PGOOD

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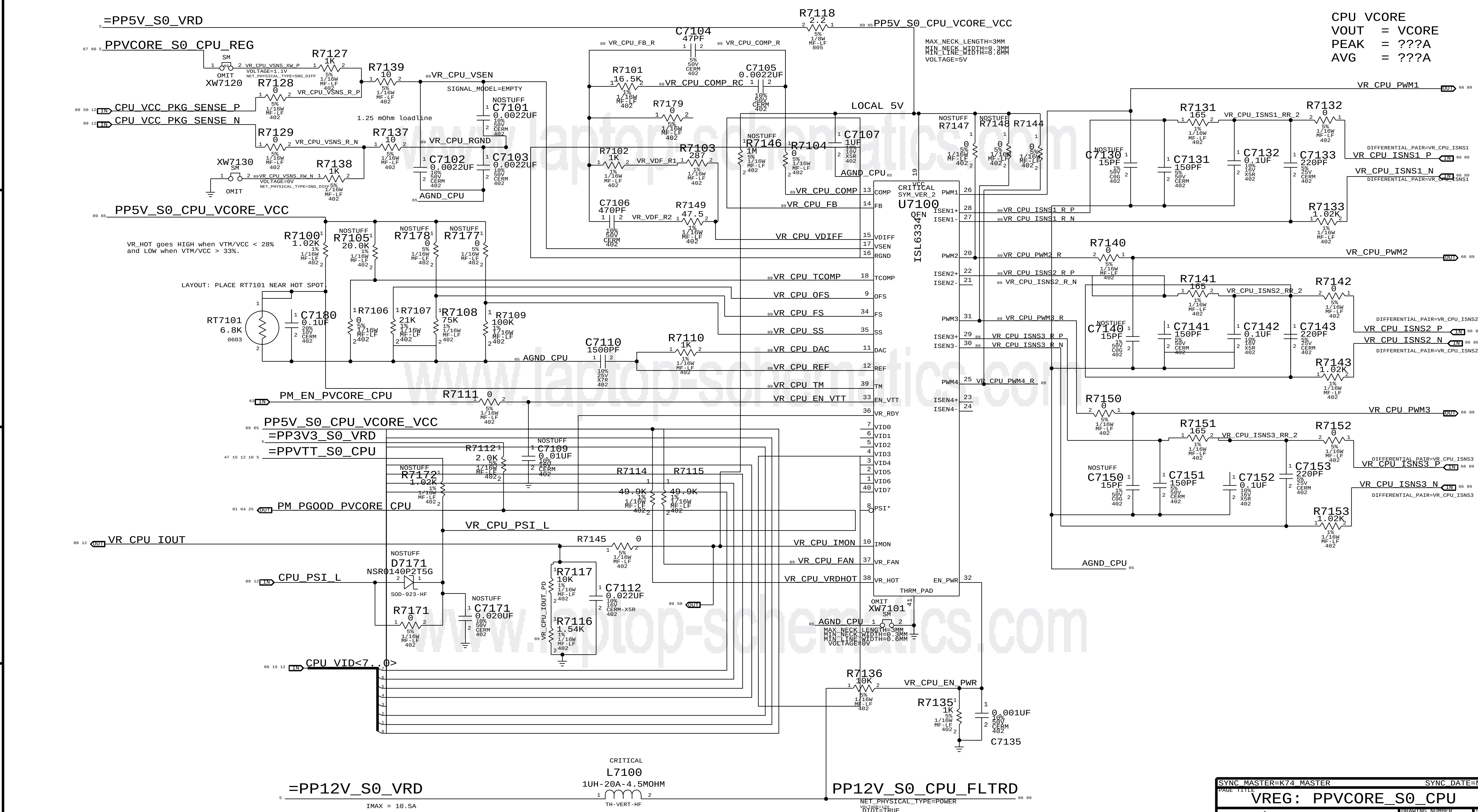
CPU CORE REG 1.1V/???A O/P= PPVCORE_S0_CPU_REG



CPU CORE INPUT Filtering

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: VREG: PPVCORE_S0_CPU

Apple Inc.

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PP12V_S0_CPU_FLTRD

PHASE 1

CRITICAL C7270 270UF 20% 16V ELEC 8X9-TH1
CRITICAL C7271 270UF 20% 16V ELEC 8X9-TH1
R7202 10 5% 1/10W MF-LF 603
R7205 0 5% 1/10W MF-LF 603
NOSTUFF R7201 10 5% 1/10W MF-LF 603

VR_CPU_DRV1_VCC
NET_PHYSICAL_TYPE=VR_CTL_PHY
VR_CPU_DRV1_UVCC
NET_PHYSICAL_TYPE=VR_CTL_PHY
VR_CPU_DRV1_PVCC
NET_PHYSICAL_TYPE=VR_CTL_PHY

C7201 1UF 10% 16V X5R 603

U7201 ISL6622 DFN
VCC UVCC LVCC
GDSEL
BOOT
CRITICAL
UGATE
PHASE
PWM
LGATE
GND
THRML PAD

VR_CPU_DRV1_GDSEL
NOSTUFF R7207 0 5% 1/10W MF-LF 603
C7202 1UF 10% 16V X5R 603
C7200 1UF 10% 16V X5R 603
VR_CPU_PWM1

VR_CPU_BOOT1_RC
NET_PHYSICAL_TYPE=VR_CTL_PHY
R7204 0 5% 1/10W MF-LF 603
C7203 0.22UF 10% 16V X7R 603

VR_CPU_DRV1_BOOT
NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE
VR_CPU_DRV1_UGATE
NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE
VR_CPU_PHASE1
NET_PHYSICAL_TYPE=POWER DIDT=TRUE
VR_CPU_DRV1_LGATE
NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE

376S0772
CRITICAL Q7201 IRF6710 S1
376S0771
CRITICAL Q7202 IRF6795 DIRECTFET-MX

CRITICAL C7205 270UF 20% 16V ELEC 8X9-TH1
CRITICAL C7206 10UF 10% 16V X5R-CERM 0805
CRITICAL C7215 10UF 10% 16V X5R-CERM 0805
C7207 1UF 10% 16V X5R 603
C7210 0.001UF 10% 50V X7R 402
C7211 0.001UF 10% 50V X7R 402
THESE TWO CAPS ARE FOR EMC

CRITICAL L7201 0.36UH-35A MSQ1208-TH 152-0114
CRITICAL R7208 0.0005 1% 1W MF 0612
PPVCORE_S0_CPU_REG1
PPVCORE_S0_CPU_REG

R7206 1 5% 1/8W MF-LF 805
VR_CPU_PH1_SNUB
NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE
C7208 1000PF 5% 25V NP0-C0G 402

VR_CPU_ISNS1_P
VR_CPU_ISNS1_N

PHASE 2

R7222 10 5% 1/10W MF-LF 603
R7225 0 5% 1/10W MF-LF 603
NOSTUFF R7221 10 5% 1/10W MF-LF 603

VR_CPU_DRV2_VCC
NET_PHYSICAL_TYPE=VR_CTL_PHY
VR_CPU_DRV2_UVCC
NET_PHYSICAL_TYPE=VR_CTL_PHY
VR_CPU_DRV2_PVCC
NET_PHYSICAL_TYPE=VR_CTL_PHY

C7221 1UF 10% 16V X5R 603

U7221 ISL6612 QFN1
VCC PVCC
PWM
CRITICAL
BOOT
UGATE
PHASE
LGATE
GND
THRML PAD

VR_CPU_DRV2_GDSEL
NOSTUFF R7227 0 5% 1/10W MF-LF 603
C7222 1UF 10% 16V X5R 603
NOSTUFF C7220 1UF 10% 16V X5R 603
VR_CPU_PWM2

VR_CPU_BOOT2_RC
NET_PHYSICAL_TYPE=VR_CTL_PHY
R7224 0 5% 1/10W MF-LF 603
C7223 0.22UF 10% 16V X7R 603

VR_CPU_DRV2_BOOT
NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE
VR_CPU_DRV2_UGATE
NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE
VR_CPU_PHASE2
NET_PHYSICAL_TYPE=POWER DIDT=TRUE
VR_CPU_DRV2_LGATE
NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE

376S0772
CRITICAL Q7221 IRF6710 S1
376S0771
CRITICAL Q7222 IRF6795 DIRECTFET-MX

CRITICAL C7225 270UF 20% 16V ELEC 8X9-TH1
CRITICAL C7226 10UF 10% 16V X5R-CERM 0805
CRITICAL C7229 10UF 10% 16V X5R-CERM 0805
C7227 1UF 10% 16V X5R 603
C7230 0.001UF 10% 50V X7R 402
C7231 0.001UF 10% 50V X7R 402
THESE TWO CAPS ARE FOR EMC

CRITICAL L7221 0.36UH-35A MSQ1208-TH 152-0114
CRITICAL R7228 0.0005 1% 1W MF 0612
PPVCORE_S0_CPU_REG2
PPVCORE_S0_CPU_REG

R7226 1 5% 1/8W MF-LF 805
VR_CPU_PH2_SNUB
NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE
C7228 1000PF 5% 25V NP0-C0G 402

VR_CPU_ISNS2_P
VR_CPU_ISNS2_N

PHASE 3

376S0772

R7242 10 5% 1/10W MF-LF 603
R7245 0 5% 1/10W MF-LF 603
NOSTUFF R7241 10 5% 1/10W MF-LF 603

VR_CPU_DRV3_VCC
NET_PHYSICAL_TYPE=VR_CTL_PHY
VR_CPU_DRV3_UVCC
NET_PHYSICAL_TYPE=VR_CTL_PHY
VR_CPU_DRV3_PVCC
NET_PHYSICAL_TYPE=VR_CTL_PHY

C7241 1UF 10% 16V X5R 603

U7241 ISL6612 QFN1
VCC PVCC
PWM
CRITICAL
BOOT
UGATE
PHASE
LGATE
GND
THRML PAD

VR_CPU_DRV3_GDSEL
NOSTUFF R7247 0 5% 1/10W MF-LF 603
C7242 1UF 10% 16V X5R 603
NOSTUFF C7240 1UF 10% 16V X5R 603
VR_CPU_PWM3

VR_CPU_BOOT3_RC
NET_PHYSICAL_TYPE=VR_CTL_PHY
R7244 0 5% 1/10W MF-LF 603
C7243 0.22UF 10% 16V X7R 603

VR_CPU_DRV3_BOOT
NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE
VR_CPU_DRV3_UGATE
NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE
VR_CPU_PHASE3
NET_PHYSICAL_TYPE=POWER DIDT=TRUE
VR_CPU_DRV3_LGATE
NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE

376S0771
CRITICAL Q7241 IRF6710 S1
CRITICAL Q7242 IRF6795 DIRECTFET-MX

CRITICAL C7245 270UF 20% 16V ELEC 8X9-TH1
CRITICAL C7246 10UF 10% 16V X5R-CERM 0805
CRITICAL C7249 10UF 10% 16V X5R-CERM 0805
C7247 1UF 10% 16V X5R 603
C7250 0.001UF 10% 50V X7R 402
C7251 0.001UF 10% 50V X7R 402
THESE TWO CAPS ARE FOR EMC

CRITICAL L7241 0.36UH-35A MSQ1208-TH 152-0114
CRITICAL R7248 0.0005 1% 1W MF 0612
PPVCORE_S0_CPU_REG3
PPVCORE_S0_CPU_REG

R7246 1 5% 1/8W MF-LF 805
VR_CPU_PH3_SNUB
NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE
C7248 1000PF 5% 25V NP0-C0G 402

VR_CPU_ISNS3_P
VR_CPU_ISNS3_N

OUTPUT BULK DECOUPLING:

128S0209
PPVCORE_S0_CPU_REG
???A MAX

C7260 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM
C7261 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM
C7262 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM
C7263 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM
C7264 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
VREG: CPU CORE - PHASES 1-3

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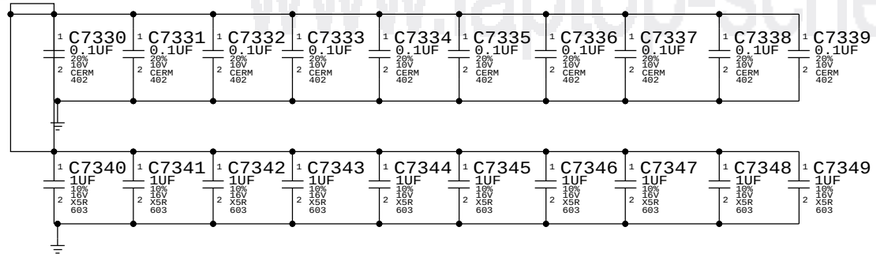
66 65 5 PPVCORE_S0_CPU_REG



SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE

VREG: CPU CORE - CAPS

Apple Inc.

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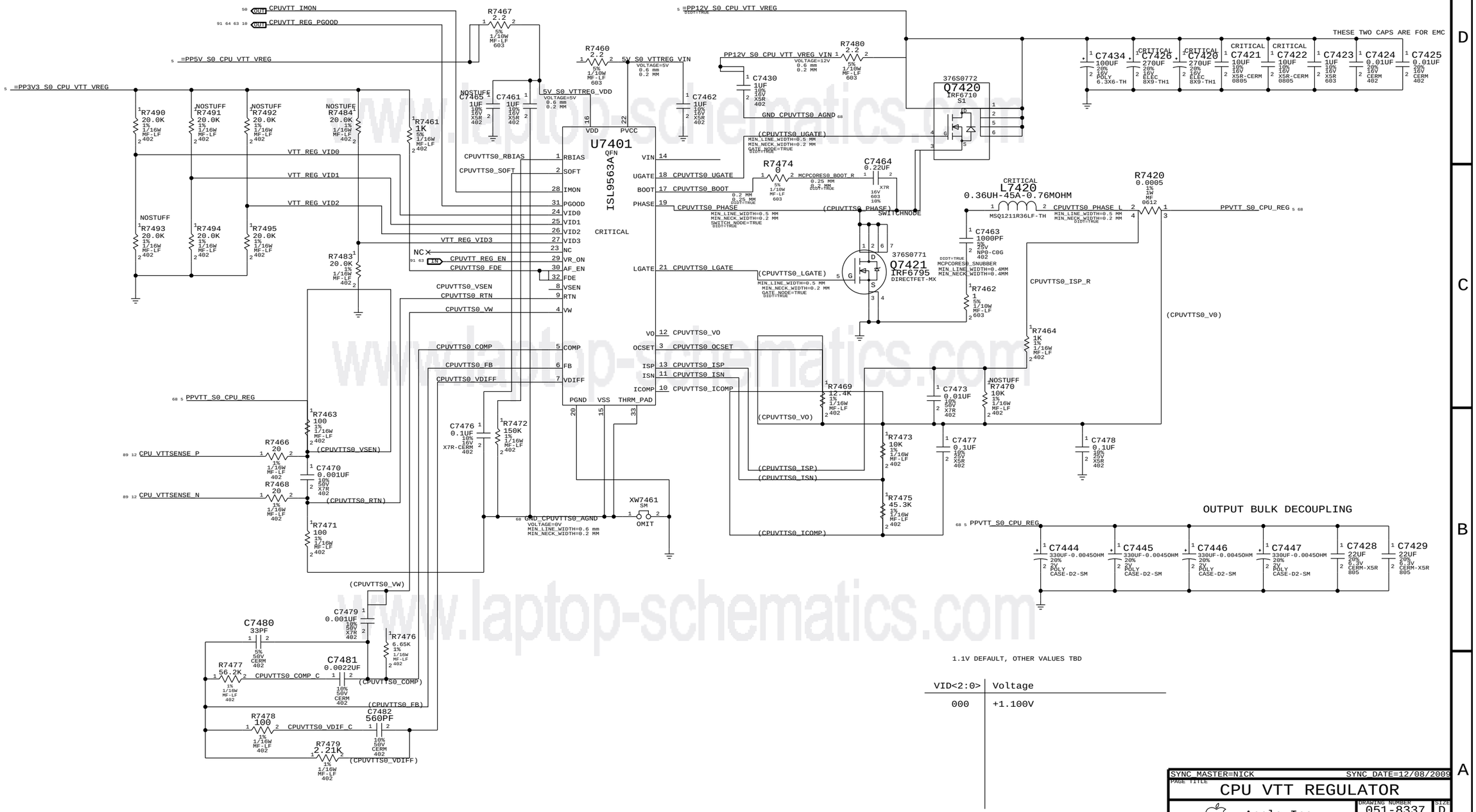
CPU VTT REG 1.1V O/P= PPVTT_S0_CPU_REG



1.1V DEFAULT, OTHER VALUES TBD

VID<2:0>	Voltage
000	+1.100V

SYNC_MASTER=NICK SYNC_DATE=12/08/2009

PAGE TITLE: CPU VTT REGULATOR

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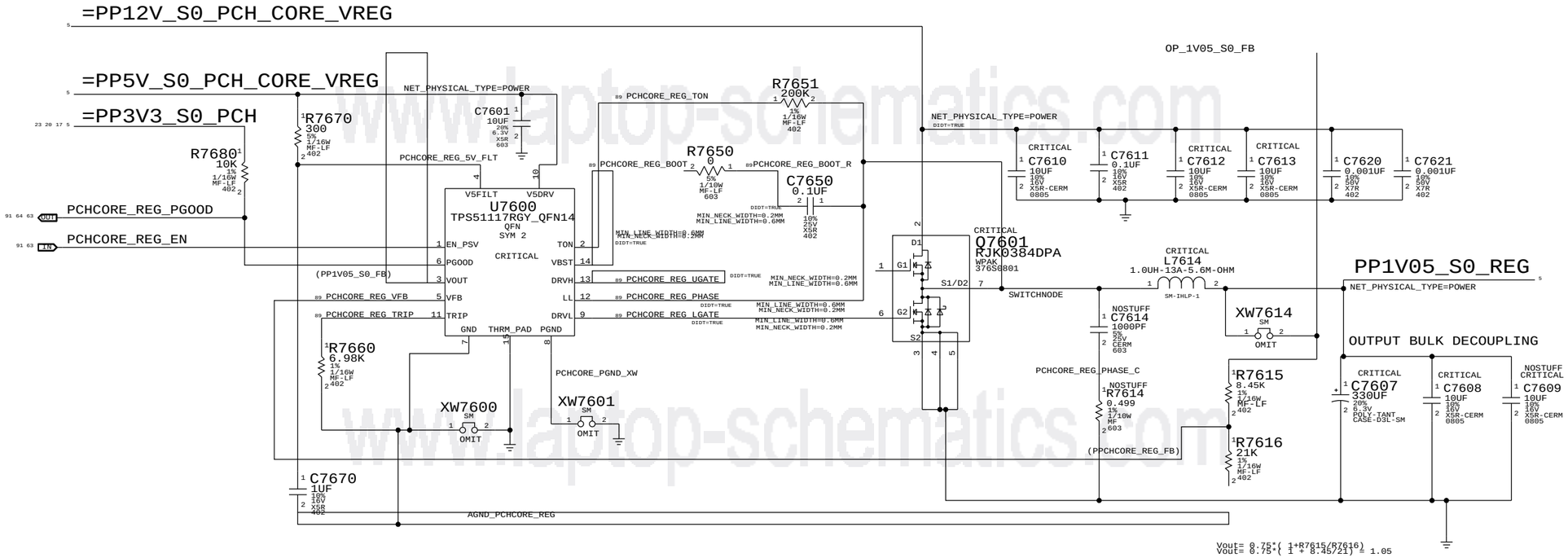
IBEX PEAK CORE REG 1.05V OUTPUT = PP1V05_S0_REG

PP1V05_S0_REG
VOUT = 1.05V
PEAK = 7.5A
AVG = 3A



SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: IBEX PEAK CORE

Apple Inc.

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3V3 S5 REGULATOR

5V S3 REGULATOR

Power Rating ?

3V3 OUTPUT

5V OUTPUT

=PP12V_S5_P5VS3_VREG

=PP12V_S5_P3V3S5_VREG

NET_PHYSICAL_TYPE=POWER

EMC CAPS
PLACE CLOSE TO FET

C7718 100UF 20% 16V POLY 6.3X6-TH
C7719 100UF 20% 16V POLY 6.3X6-TH
C7712 10UF 10% 16V X5R-CERM 0805
C7710 10UF 10% 16V X5R-CERM 0805
C7711 0.1UF 10% 16V X5R 402
C7722 0.1UF 10% 16V X5R 402

C7766 270UF 20% 16V ELEC 8X9-TH1
C7783 22UF 20% 16V X7R 1210
C7751 10UF 10% 16V X5R-CERM 0805
C7752 10UF 10% 16V X5R-CERM 0805
C7753 10UF 10% 16V X5R-CERM 0805
C7758 10UF 10% 16V X5R-CERM 0805
C7765 10UF 10% 16V X5R-CERM 0805

PP5V_S5_LDO

EMC: C7754,C7755
PLACE AT Q7330

C7754 0.1UF 10% 25V X5R 402
C7755 0.1UF 10% 25V X5R 402

DIDT=TRUE

PP3V3_S5_REG

CRITICAL
L7710 2.2UH-14A MMD06CZ-SM

SWITCHNODE

NET_PHYSICAL_TYPE=POWER

Q7710 RJK0384DPA WPAK 376S0801

D1 G1 S1/D2 G2 S2

1 (P3V3S5_UGATE) WIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.6MM GATE_NODE=TRUE

6 (P3V3S5_LGATE) MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.6MM GATE_NODE=TRUE

C7790 8200PF 10% 50V CERM 603
R7790 16.5K 1% 1/16W MF-LF 402

R7791 16.5K 1% 1/16W MF-LF 402

C7730 1000PF 5% 25V NP0-C0G 402 NOSTUFF

R7730 0.499 1% 1/10W MF 603 NOSTUFF

P3V3S5_REG_SNUB

C7714 0.1UF 10% 50V X7R 603-1

P3V3S5_REG_BOOT_R

R7710 0 5% 1/10W MF-LF 603

(P3V3S5_PHASE)

C7742 4.7UF 20% 6.3V CERM 603

R7740 2.2 5% 1/8W MF-LF 805

P5V_S5_LDO_R

P5V_S5_VCC1

C7740 1UF 10% 16V X5R 603

C7741 1UF 10% 16V X5R 603

U7700 ISL62383 QFN CRITICAL

LDO5	18	17	VIN
PGOOD1	7	1	PGOOD2
UGATE1	14	22	UGATE2
BOOT1	15	21	BOOT2
PHASE1	13	23	PHASE2
LGATE1	16	20	LGATE2
ISEN1	10	26	ISEN2
OCSET1	11	25	OCSET2
VOUT1	9	27	VOUT2
FB1	8	28	FB2
FSET1	6	2	FSET2
EN1	12	24	EN2
THRM PAD	19		PGND

FCCM 3 TP_P5VS3_REG_FCCM

P3V3S5_REG_PGOOD (OMIT)

P3V3S5_REG_UGATE
P3V3S5_REG_BOOT
P3V3S5_REG_PHASE
P3V3S5_REG_LGATE
P3V3S5_REG_ISEN
P3V3S5_REG_OCSET
P3V3S5_REG_VOUT1
P3V3S5_REG_FB

P5VS3_REG_UGATE
P5VS3_REG_BOOT
P5VS3_REG_PHASE
P5VS3_REG_LGATE
P5VS3_REG_ISEN
P5VS3_REG_OCSET
P5VS3_REG_VOUT2
P5VS3_REG_FB
P5VS3_REG_FSET2

P5VS3_REG_PGOOD

R7750 0 5% 1/10W MF-LF 603

C7756 0.1UF 10% 25V X5R 402

P5VS3_REG_BOOT_R

MIN_NECK_WIDTH=0.2 MM MIN_LINE_WIDTH=0.6MM

P5VS3_REG_FB_R

P5VS3_REG_PGOOD

OUT 63

CRITICAL
Q7750 CSD58851Q5A MLP5X6-LFPAK-Q5A 376S0631

CRITICAL
L7750 2.2UH-10A-12.5MOHM PAB0705AR-SM

SWITCHNODE

NOSTUFF C7757 0.001UF 10% 50V CERM 402

5V SNUBBER

CRITICAL
D7750 CTLSH3-30M833 TLM833

R7752 0.499 1% 1/10W MF 603 NOSTUFF

R7770 14.3K 1% 1/10W MF-LF 402

C7770 0.01UF 10% 16V CERM 402

R7771 14.3K 1% 1/16W MF-LF 402

SM XW7751 OMIT

EMC: C7763,C7764
PLACE AT L7750.2

C7763 0.001UF 10% 50V X7R 402
C7764 0.001UF 10% 50V X7R 402

PP5V_S3_REG

NET_PHYSICAL_TYPE=POWER

OUTPUT BULK DECOUPLING:

C7760 10UF 20% 6.3V CERM 805-1
C7761 330UF 20% 6.3V POLY-TANT CASE-D3L-SM
C7762 330UF 20% 6.3V POLY-TANT CASE-D3L-SM

CRITICAL

OUTPUT BULK DECOUPLING:

C7715 10UF 10% 16V X5R-CERM 0805
C7717 10UF 10% 16V X5R-CERM 0805
128S0237
C7721 330UF 20% 6.3V POLY-TANT CASE-D3L-SM

C7723 0.1UF 20% 16V CERM 603
C7716 0.1UF 20% 16V CERM 603

EMC CAPS
PLACE CLOSE TO L

PLACEMENT_NOTE=PLACE NEXT TO C7716

SM XW7716 OMIT

R7720 45.3K 1% 1/16W MF-LF 402 <Ra>

R7721 10.0K 0.5% 1/16W MF 402 <Rb>

R7724 976 1% 1/16W MF-LF 402

C7720 1000PF 5% 25V NP0-C0G 402

P3V3S5_REG_FB_R

Vout = 0.6V * (1 + Ra / Rb)

R7722 68K 5% 1/16W MF-LF 402

R7723 33K 5% 1/16W MF-LF 402

P3V3S5_12VE_EN1

P3V3S5_REG_FSET1

C7701 0.01UF 10% 16V CERM 402

R7701 16.5K 1% 1/16W MF-LF 402

P5VS3_EN

C7747 0.01UF 10% 16V CERM 402

R7747 16.5K 1% 1/16W MF-LF 402

NOSTUFF C7777 0.001UF 10% 50V CERM 402

R7759 976 1% 1/16W MF-LF 402

C7759 1000PF 5% 25V NP0-C0G 402

R7755 75K 1% 1/16W MF-LF 402 RA

R7756 10K 1% 1/16W MF-LF 402 RB

SYNC_MASTER=NICK	SYNC_DATE=12/08/2009
PAGE TITLE	5V_S3 / 3V3_S5 VREGS
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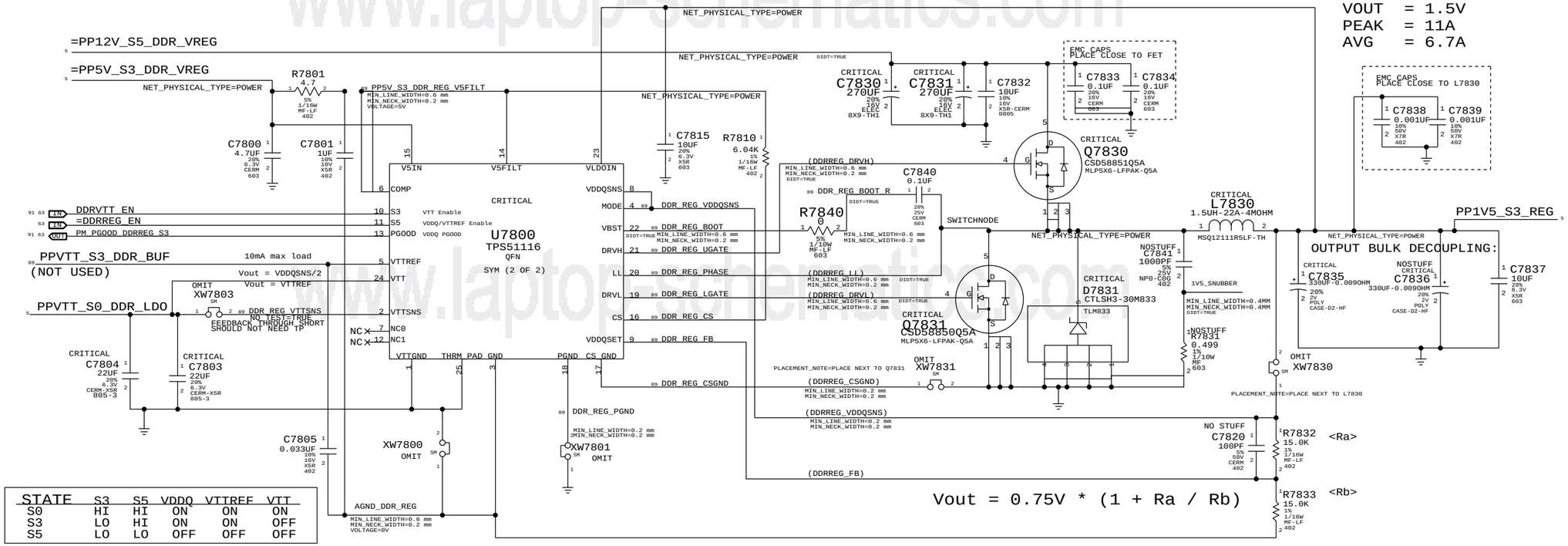
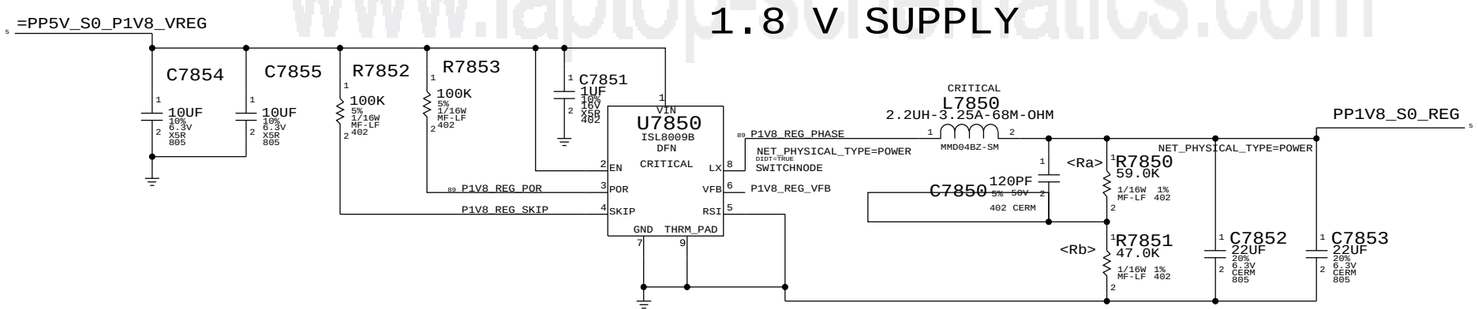
1.5 V DDR SUPPLY



STATE	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON
S3	LO	HI	ON	ON	OFF
S5	LO	LO	OFF	OFF	OFF

1.8 V SUPPLY



SYNC_MASTER=K23F SYNC_DATE=11/30/2009

PAGE TITLE: 1.5V / 1.8V VREGS

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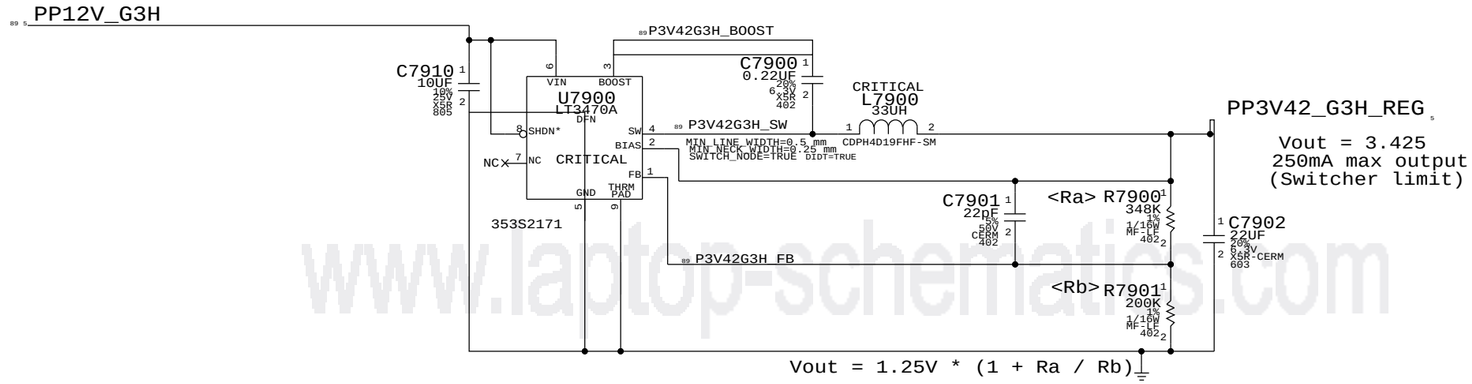
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



SYNC MASTER=K74 MASTER SYNC DATE=N/A

PAGE TITLE: 3.42 G3HOT SUPPLY

Apple Inc.

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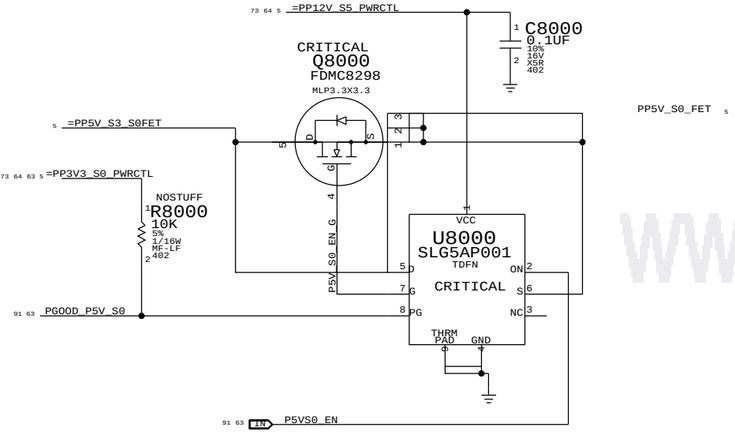
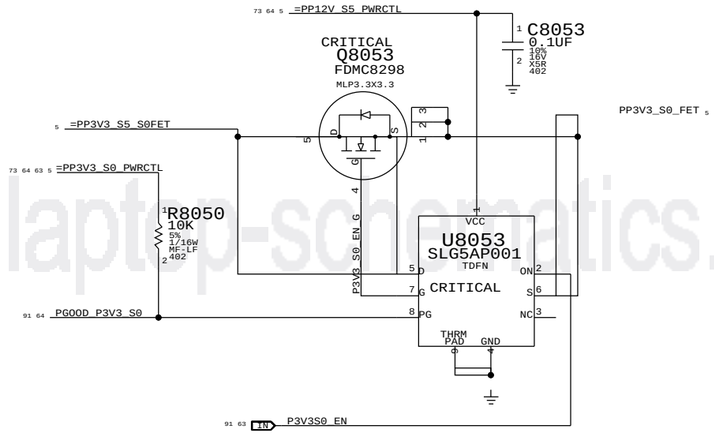
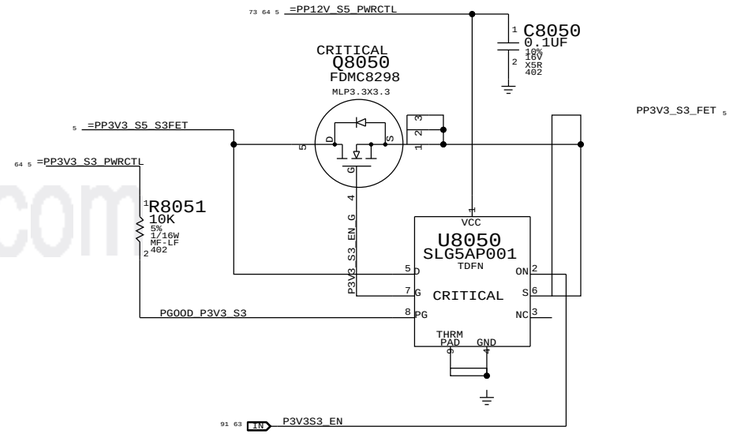
5V S0 FET (7A PK/2.7A AVG)



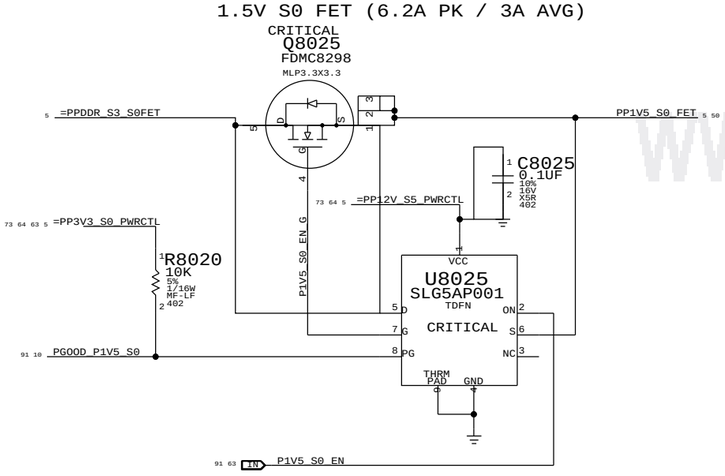
3.3V S0 FET (3.4APK / 1.9A AVG)



3.3V S3 FET (2.9A PK / 1.2A AVG)



1.5V S0 FET (6.2A PK / 3A AVG)



SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: S3+S0 FETS

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 80 OF 110

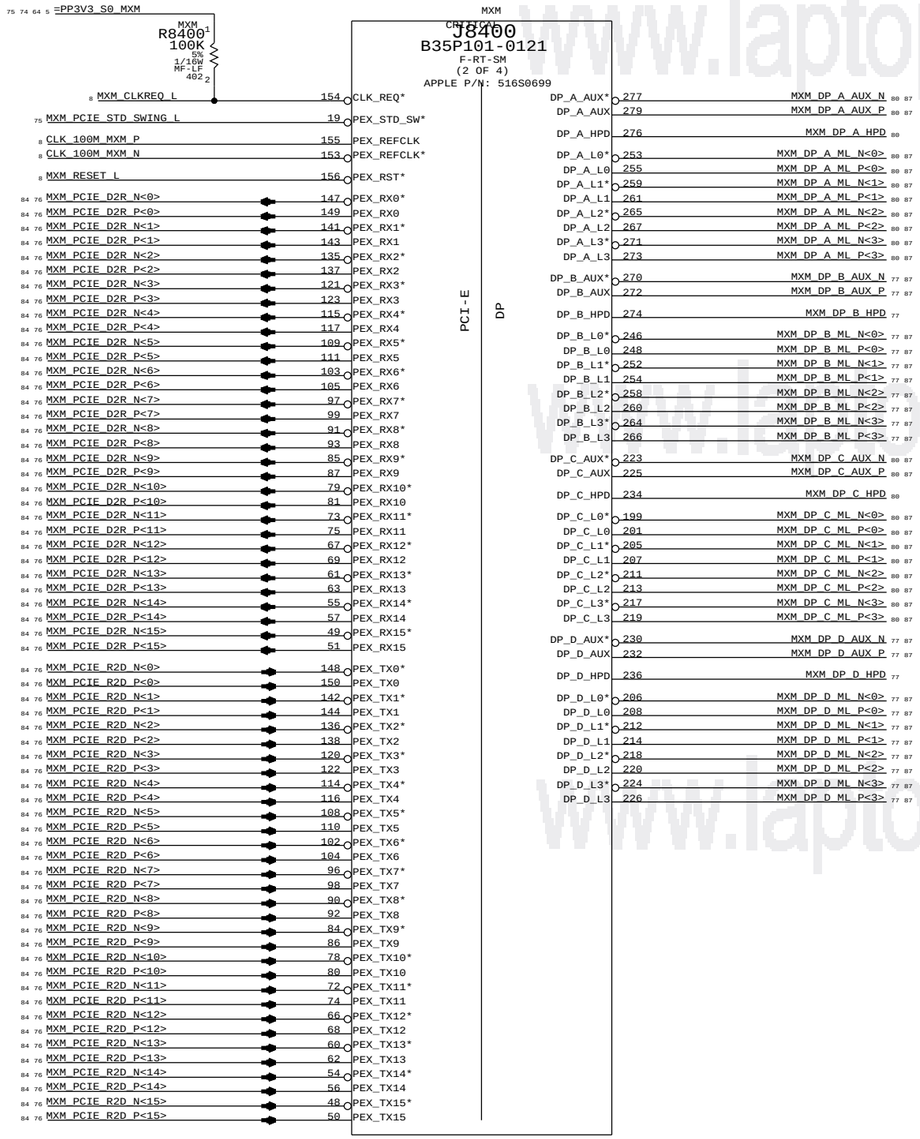
SHEET: 73 OF 92

Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP5V_S0_MXM
- =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- MXM



MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.0 A	3.3 W
5V	2.5 A	12.5 W
PWR (7-20V)	UP TO 10 A	PLATFORM DEPENDENT

SYNC_MASTER=K23F SYNC_DATE=11/30/2009

PAGE TITLE: MXM PCIe, DP & Power

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 84 OF 110

SHEET: 74 OF 92

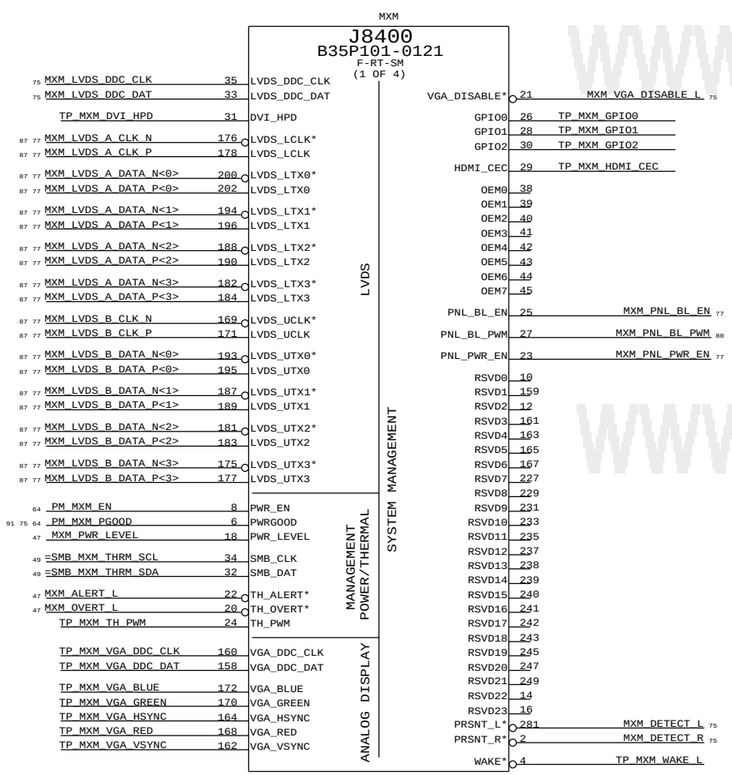
Page Notes

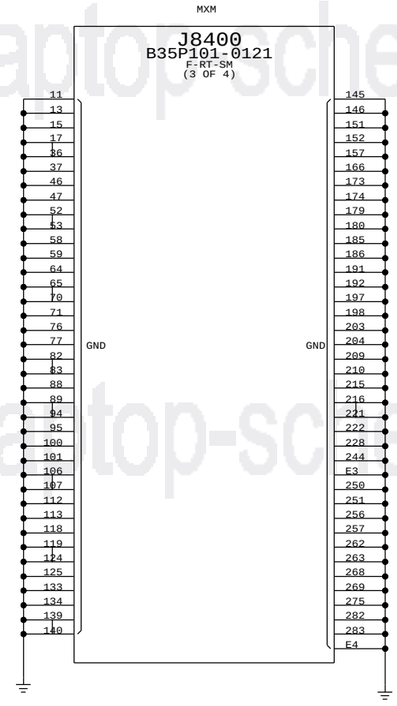
Power aliases required by this page:
- =PP3V3_S0_MXM

Signal aliases required by this page:
- =SMB_MXM_THRM_DATA
- =PM_MXM_PGOOD_PULLUP
- =SMB_MXM_THRM_CLK

BOM options provided by this page:

PULLUPS & PULLDOWNS AT MXM CONNECTOR





FLOAT = NORMAL VGA MODE
GND = SECONDARY DISPLAY CARD

FLOAT = LOW SWING
GND = HIGH SWING

NOSTUFF
R8510 0 MF-LF 5% 1/16W 402
MXM_VGA_DISABLE_L
NOSTUFF
R8504 0 MF-LF 5% 1/16W 402
MXM_PCIE_STD_SWING_L

=PP3V3_S0_MXM

R8500 100K MF-LF 5% 1/16W 402
MXM_DETECT_L
PULLED TO GROUND ON MXM
WE DON'T USE CARD DETECT
R8501 100K MF-LF 5% 1/16W 402
MXM_DETECT_R

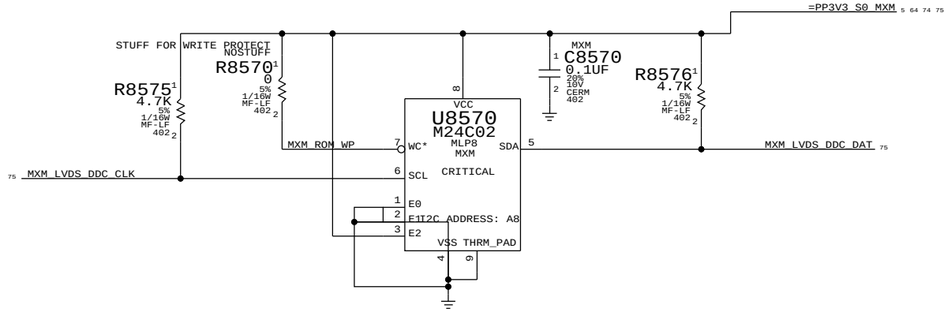
=PM_MXM_PGOOD_PULLUP

SYSTEM INTEGRATOR MUST ALIAS THIS EITHER TO A VOLTAGE RAIL,
OR ANOTHER OPEN-DRAIN PGOOD SIGNAL DEPENDING ON DESIRED BEHAVIOR

R8503 10K MF-LF 5% 1/16W 402
PM_MXM_PGOOD

MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J8400



SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: MXM I/O

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 85 OF 110
SHEET: 75 OF 92

MXM TX CAPS

PEG_R2D_C_P<0>	MXM	C8600	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<15>
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PEG_R2D_C_P<13>	MXM	C8627	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<2>
PEG_R2D_C_P<14>	MXM	C8628	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<1>
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MXM RX CAPS

MXM_PCIE_D2R_P<15>	MXM	C8632	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<0>
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MXM_PCIE_D2R_P<6>	MXM	C8650	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<9>
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MXM_PCIE_D2R_P<4>	MXM	C8654	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<11>
MXM_PCIE_D2R_N<4>	MXM	C8655	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<11>
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SYNC_MASTER=K23F SYNC_DATE=11/30/2009

PAGE TITLE
MXM PCIE CAPS

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D
REVISION A.0.0
BRANCH
PAGE 86 OF 110
SHEET 76 OF 92

Page Notes

Power aliases required by this page:

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Unused MXM Interfaces

87 75 MXM_LVDS_A_CLK_N = NC_MXM_LVDS_A_CLK_N
MAKE_BASE=TRUE NO_TEST=TRUE
87 75 MXM_LVDS_A_CLK_P = NC_MXM_LVDS_A_CLK_P
MAKE_BASE=TRUE NO_TEST=TRUE
87 75 MXM_LVDS_A_DATA_N<0> = NC_MXM_LVDS_A_DATA_N<0>
MAKE_BASE=TRUE NO_TEST=TRUE
87 75 MXM_LVDS_A_DATA_P<0> = NC_MXM_LVDS_A_DATA_P<0>
MAKE_BASE=TRUE NO_TEST=TRUE
87 75 MXM_LVDS_A_DATA_N<1> = NC_MXM_LVDS_A_DATA_N<1>
MAKE_BASE=TRUE NO_TEST=TRUE
87 75 MXM_LVDS_A_DATA_P<1> = NC_MXM_LVDS_A_DATA_P<1>
MAKE_BASE=TRUE NO_TEST=TRUE
87 75 MXM_LVDS_A_DATA_N<2> = NC_MXM_LVDS_A_DATA_N<2>
MAKE_BASE=TRUE NO_TEST=TRUE
87 75 MXM_LVDS_A_DATA_P<2> = NC_MXM_LVDS_A_DATA_P<2>
MAKE_BASE=TRUE NO_TEST=TRUE
87 75 MXM_LVDS_A_DATA_N<3> = NC_MXM_LVDS_A_DATA_N<3>
MAKE_BASE=TRUE NO_TEST=TRUE
87 75 MXM_LVDS_A_DATA_P<3> = NC_MXM_LVDS_A_DATA_P<3>
MAKE_BASE=TRUE NO_TEST=TRUE
87 75 MXM_LVDS_B_CLK_N = NC_MXM_LVDS_B_CLK_N
MAKE_BASE=TRUE NO_TEST=TRUE
87 75 MXM_LVDS_B_CLK_P = NC_MXM_LVDS_B_CLK_P
MAKE_BASE=TRUE NO_TEST=TRUE
87 75 MXM_LVDS_B_DATA_N<0> = NC_MXM_LVDS_B_DATA_N<0>
MAKE_BASE=TRUE NO_TEST=TRUE
87 75 MXM_LVDS_B_DATA_P<0> = NC_MXM_LVDS_B_DATA_P<0>
MAKE_BASE=TRUE NO_TEST=TRUE
87 75 MXM_LVDS_B_DATA_N<1> = NC_MXM_LVDS_B_DATA_N<1>
MAKE_BASE=TRUE NO_TEST=TRUE
87 75 MXM_LVDS_B_DATA_P<1> = NC_MXM_LVDS_B_DATA_P<1>
MAKE_BASE=TRUE NO_TEST=TRUE
87 75 MXM_LVDS_B_DATA_N<2> = NC_MXM_LVDS_B_DATA_N<2>
MAKE_BASE=TRUE NO_TEST=TRUE
87 75 MXM_LVDS_B_DATA_P<2> = NC_MXM_LVDS_B_DATA_P<2>
MAKE_BASE=TRUE NO_TEST=TRUE
87 75 MXM_LVDS_B_DATA_N<3> = NC_MXM_LVDS_B_DATA_N<3>
MAKE_BASE=TRUE NO_TEST=TRUE
87 75 MXM_LVDS_B_DATA_P<3> = NC_MXM_LVDS_B_DATA_P<3>
MAKE_BASE=TRUE NO_TEST=TRUE

Unused MXM DP Interfaces

87 74 MXM_DP_B_ML_P<0..3> = NC_MXM_DP_B_ML_P<0..3>
MAKE_BASE=TRUE NO_TEST=TRUE
87 74 MXM_DP_B_ML_N<0..3> = NC_MXM_DP_B_ML_N<0..3>
MAKE_BASE=TRUE NO_TEST=TRUE
87 74 MXM_DP_B_AUX_P = NC_MXM_DP_B_AUX_P
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87 74 MXM_DP_B_AUX_N = NC_MXM_DP_B_AUX_N
MAKE_BASE=TRUE NO_TEST=TRUE
74 MXM_DP_B_HPD = NC_MXM_DP_B_HPD
MAKE_BASE=TRUE NO_TEST=TRUE
87 74 MXM_DP_D_ML_P<0..3> = NC_MXM_DP_D_ML_P<0..3>
MAKE_BASE=TRUE NO_TEST=TRUE
87 74 MXM_DP_D_ML_N<0..3> = NC_MXM_DP_D_ML_N<0..3>
MAKE_BASE=TRUE NO_TEST=TRUE
87 74 MXM_DP_D_AUX_P = NC_MXM_DP_D_AUX_P
MAKE_BASE=TRUE NO_TEST=TRUE
87 74 MXM_DP_D_AUX_N = NC_MXM_DP_D_AUX_N
MAKE_BASE=TRUE NO_TEST=TRUE
74 MXM_DP_D_HPD = NC_MXM_DP_D_HPD
MAKE_BASE=TRUE NO_TEST=TRUE

UNUSED MXM CONTROL SIGNALS

75 MXM_PNL_BL_EN = NC_MXM_PNL_BL_EN
MAKE_BASE=TRUE NO_TEST=TRUE
75 MXM_PNL_PWR_EN = NC_MXM_PNL_PWR_EN
MAKE_BASE=TRUE NO_TEST=TRUE

DISPLAY AUDIO MUX NOT USED - SEND SPDIF TO CODEC

85 60 IN AUD_SPDIF_IN = AUD_SPDIF_IN_CODEC OUT 56
MAKE_BASE=TRUE
78 IN DP_INT_SPDIF_AUDIO = TP_DP_INT_SPDIF_AUDIO
MAKE_BASE=TRUE

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
Display: Aliases

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D
REVISION A.0.0
BRANCH
PAGE 87 OF 110
SHEET 77 OF 92

Page Notes

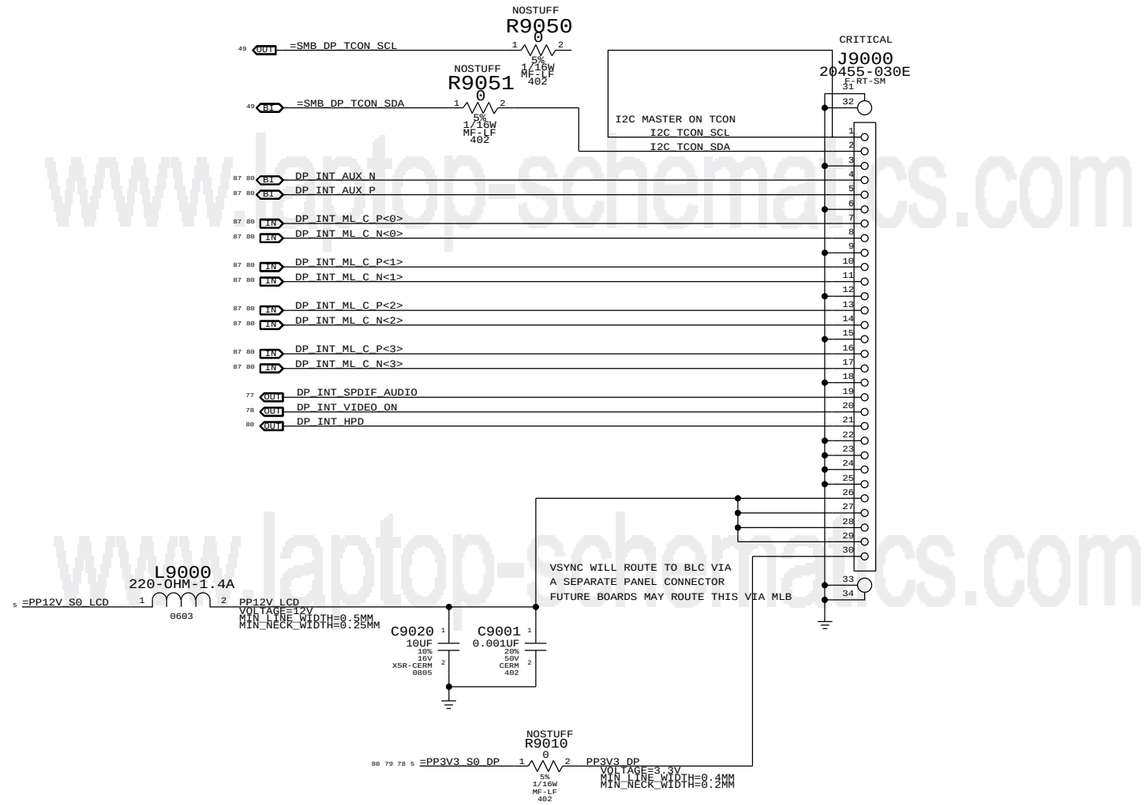
Power aliases required by this page:

- =PP12V_S0_LCD
- =PP3V3_S0_DP

Signal aliases required by this page:
- =SMB_DP_TCON_SCL, =SMB_DP_TCON_SDA

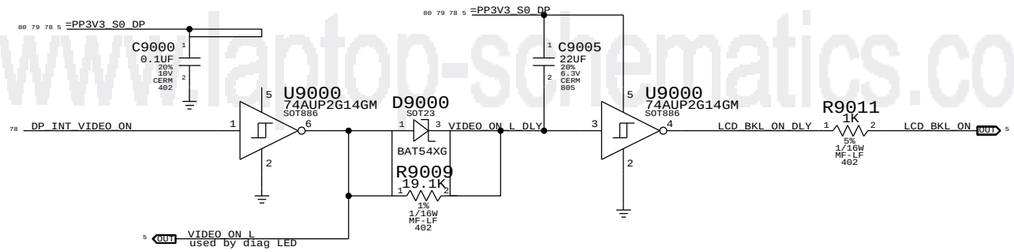
BOM options provided by this page:

INTERNAL DP INTERFACE



BACKLIGHT CONTROL SUPPORT

guarantee backlight is
only on when Panel has valid video



SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
Display: Int DP Connector

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D
REVISION A.0.0
BRANCH
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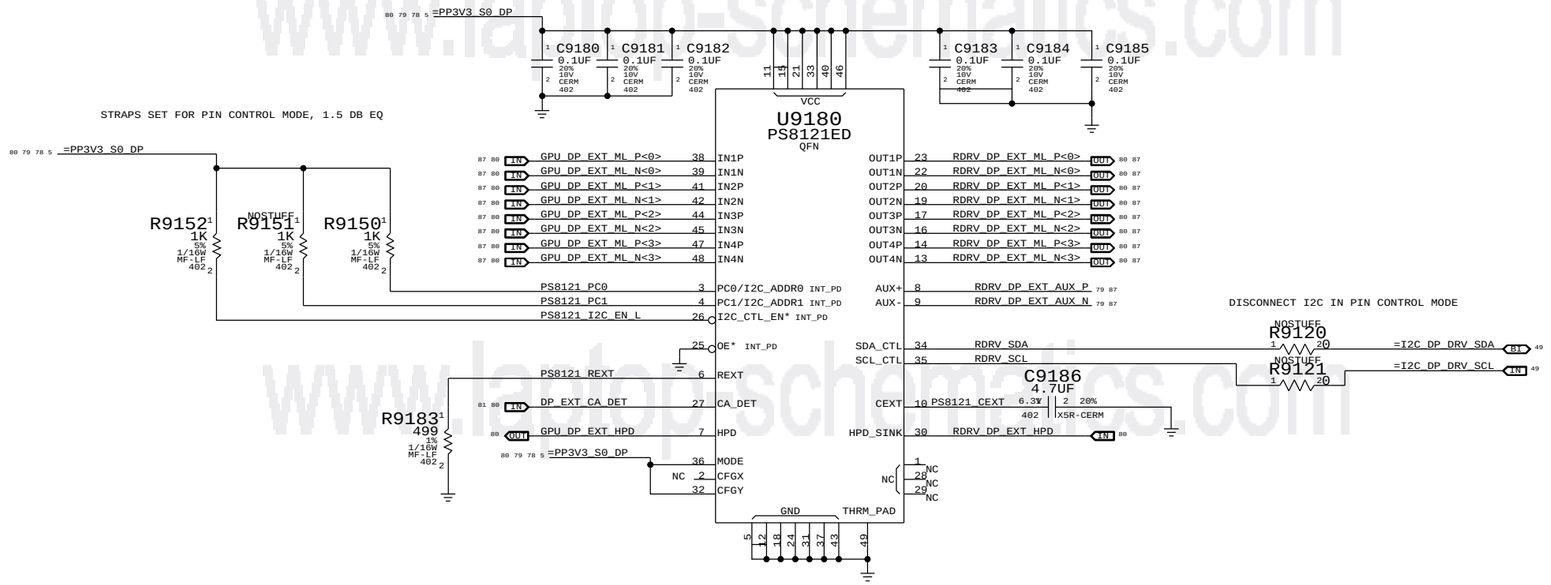
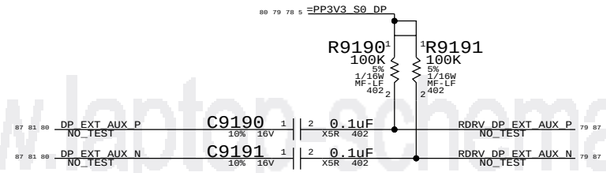
EQ & Re-Driver for DP source



COMMON MODE BIAS FOR PS8121ED AUX INTERCEPTION



SYNC_MASTER=DAVE SYNC_DATE=01/07/2010

PAGE TITLE: DISPLAY: DP REDRIVER

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 91 OF 110

SHEET: 79 OF 92

FROM GPU TO REDRIVER

MXM_DP_A_ML_P<0>	NO_TEST	C9212	0.1uF 10% 16V X5R 402	NO_TEST	GPU_DP_EXT_ML_P<0>		
MXM_DP_A_ML_N<0>	NO_TEST	C9213	0.1uF 10% 16V X5R 402	NO_TEST	GPU_DP_EXT_ML_N<0>		
MXM_DP_A_ML_P<1>	NO_TEST	C9214	0.1uF 10% 16V X5R 402	NO_TEST	GPU_DP_EXT_ML_P<1>		
MXM_DP_A_ML_N<1>	NO_TEST	C9215	0.1uF 10% 16V X5R 402	NO_TEST	GPU_DP_EXT_ML_N<1>		
MXM_DP_A_ML_P<2>	NO_TEST	C9216	0.1uF 10% 16V X5R 402	NO_TEST	GPU_DP_EXT_ML_P<2>		
MXM_DP_A_ML_N<2>	NO_TEST	C9217	0.1uF 10% 16V X5R 402	NO_TEST	GPU_DP_EXT_ML_N<2>		
MXM_DP_A_ML_P<3>	NO_TEST	C9218	0.1uF 10% 16V X5R 402	NO_TEST	GPU_DP_EXT_ML_P<3>		
MXM_DP_A_ML_N<3>	NO_TEST	C9219	0.1uF 10% 16V X5R 402	NO_TEST	GPU_DP_EXT_ML_N<3>		

MXM_DP_A_HPD = GPU_DP_EXT_HPD (MAKE_BASE=TRUE)

REDRIVER TO EXTERNAL CONNECTOR

RDRV_DP_EXT_ML_P<0>	NO_TEST	C9230	0.1uF 10% 16V X5R 402	NO_TEST	DP_EXT_ML_C_P<0>		
RDRV_DP_EXT_ML_N<0>	NO_TEST	C9231	0.1uF 10% 16V X5R 402	NO_TEST	DP_EXT_ML_C_N<0>		
RDRV_DP_EXT_ML_P<1>	NO_TEST	C9232	0.1uF 10% 16V X5R 402	NO_TEST	DP_EXT_ML_C_P<1>		
RDRV_DP_EXT_ML_N<1>	NO_TEST	C9233	0.1uF 10% 16V X5R 402	NO_TEST	DP_EXT_ML_C_N<1>		
RDRV_DP_EXT_ML_P<2>	NO_TEST	C9234	0.1uF 10% 16V X5R 402	NO_TEST	DP_EXT_ML_C_P<2>		
RDRV_DP_EXT_ML_N<2>	NO_TEST	C9235	0.1uF 10% 16V X5R 402	NO_TEST	DP_EXT_ML_C_N<2>		
RDRV_DP_EXT_ML_P<3>	NO_TEST	C9236	0.1uF 10% 16V X5R 402	NO_TEST	DP_EXT_ML_C_P<3>		
RDRV_DP_EXT_ML_N<3>	NO_TEST	C9237	0.1uF 10% 16V X5R 402	NO_TEST	DP_EXT_ML_C_N<3>		

RDRV_DP_EXT_HPD = DP_EXT_HPD (MAKE_BASE=TRUE)

AUX/DDC SELECTION FOR EXTERNAL PORT

=PP3V3_S0_DP

R9215 100K 5% 1/16W MF-LF 402

C9210 0.1UF 10% 16V X5R 402

MXM_DP_A_AUX_N — DP_EXT_AUX_N

=PP5V_S0_DP_AUX_MUX

R9252 100K 5% 1/16W MF-LF 402

Q9250 SSM6N15FEAPE SOT563

DDC_CA_DET_LS5V

Q9251 SSM3K15FV SOD-VESM-HF

=PP5V_S0_DP_AUX_MUX

R9202 100K 5% 1/16W MF-LF 402

DDC_CA_DET_LS5V_L

Q9201 SSM3K15FV SOD-VESM-HF

DP_EXT_CA_DET

Q9250 SSM6N15FEAPE SOT563

C9211 0.1UF 10% 16V X5R 402

MXM_DP_A_AUX_P — DP_EXT_AUX_P

R9216 100K 5% 1/16W MF-LF 402

GPU TO INTERNAL CONNECTOR

R9170 47 5% 1/16W MF-LF 402

CRITICAL L9170 FERR-220-OHM 0402

MXM_PNL_BL_PWM — LCD_PWM_FILT — LCD_PWM

MXM_DP_C_ML_P<0>	NO_TEST	C9220	0.1uF 10% 16V X5R 402	NO_TEST	DP_INT_ML_C_P<0>		
MXM_DP_C_ML_N<0>	NO_TEST	C9221	0.1uF 10% 16V X5R 402	NO_TEST	DP_INT_ML_C_N<0>		
MXM_DP_C_ML_P<1>	NO_TEST	C9222	0.1uF 10% 16V X5R 402	NO_TEST	DP_INT_ML_C_P<1>		
MXM_DP_C_ML_N<1>	NO_TEST	C9223	0.1uF 10% 16V X5R 402	NO_TEST	DP_INT_ML_C_N<1>		
MXM_DP_C_ML_P<2>	NO_TEST	C9224	0.1uF 10% 16V X5R 402	NO_TEST	DP_INT_ML_C_P<2>		
MXM_DP_C_ML_N<2>	NO_TEST	C9225	0.1uF 10% 16V X5R 402	NO_TEST	DP_INT_ML_C_N<2>		
MXM_DP_C_ML_P<3>	NO_TEST	C9226	0.1uF 10% 16V X5R 402	NO_TEST	DP_INT_ML_C_P<3>		
MXM_DP_C_ML_N<3>	NO_TEST	C9227	0.1uF 10% 16V X5R 402	NO_TEST	DP_INT_ML_C_N<3>		
MXM_DP_C_AUX_P	NO_TEST	C9200	0.1uF 10% 16V X5R 402	NO_TEST	DP_INT_AUX_P		
MXM_DP_C_AUX_N	NO_TEST	C9201	0.1uF 10% 16V X5R 402	NO_TEST	DP_INT_AUX_N		

R9200 100K 1% 1/16W MF-LF 402 — R9201 100K 1% 1/16W MF-LF 402 — =PP3V3_S0_DP

MXM_DP_C_HPD = DP_INT_HPD (MAKE_BASE=TRUE)

R9210 100K 1% 1/16W MF-LF 402

SYNC_MASTER=DAVE	SYNC_DATE=01/07/2010
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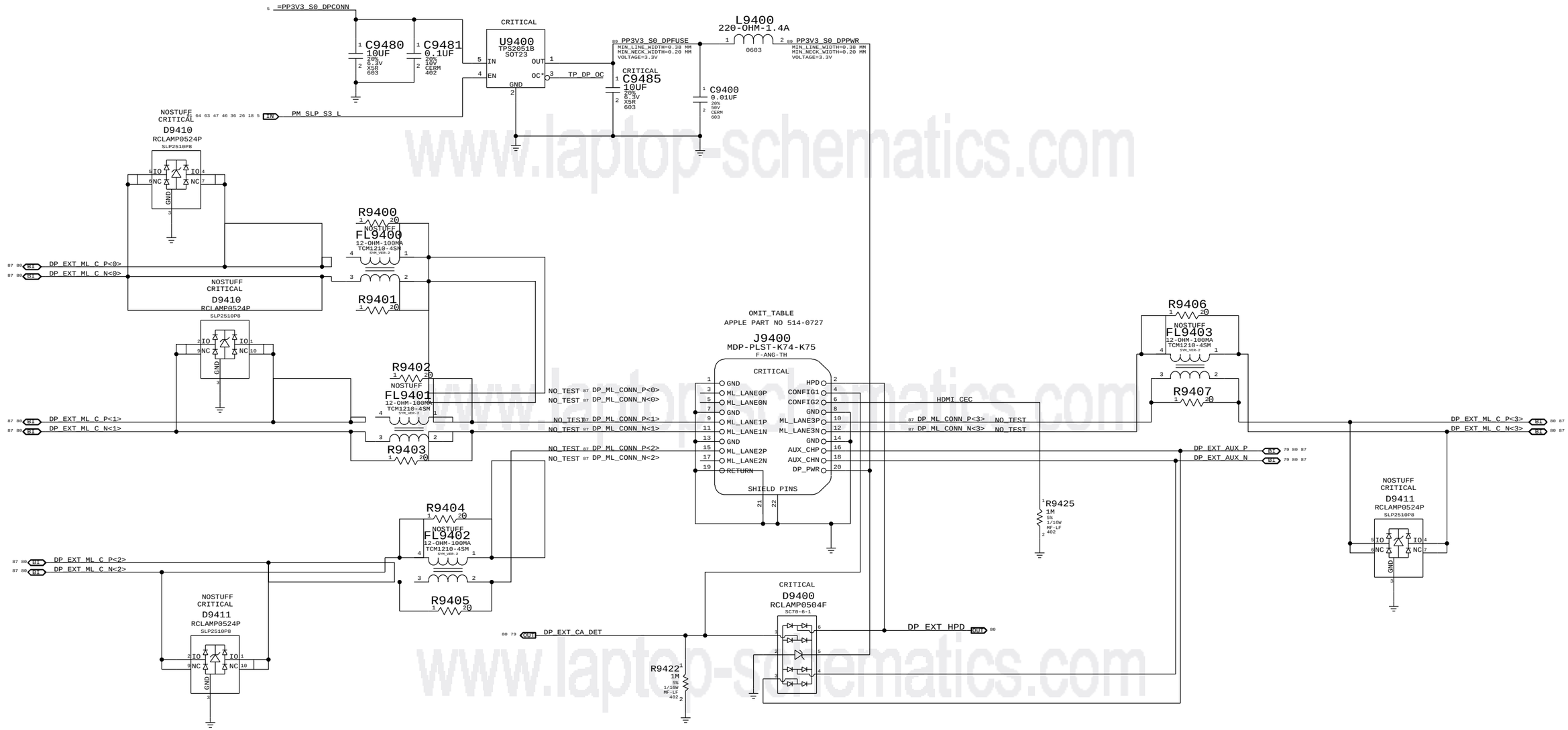

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0686	1	K22/K23 PROD. MDP	J9400	CRITICAL	METAL_IO
514-0727	1	K74/K75 MDP, PLASTIC, PD/NI	J9400	CRITICAL	PLASTIC_IO

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
Display: Ext DP Connector

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K74/K75 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OF MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	100 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.21 MM	0.085 MM	=STANDARD		
35_OHM_SE	*	Y	0.19 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39_OHM_SE	TOP,BOTTOM	Y	0.175 MM	0.085 MM	=STANDARD		
39_OHM_SE	*	Y	0.16 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.085 MM	=STANDARD		
45_OHM_SE	*	Y	0.12 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.1 MM	0.085 MM	15 MM		
50_OHM_SE	*	Y	0.1 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD		
55_OHM_SE	*	Y	0.076 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL6	Y	0.155 MM	0.085 MM	=STANDARD	0.135 MM	0.1 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.085 MM	=STANDARD	0.130 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL6	Y	0.115 MM	0.085 MM	=STANDARD	0.2 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.2 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL6	Y	0.099 MM	0.085 MM	12 MM	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.110 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL6	Y	0.081 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.085 MM	=STANDARD	0.320 MM	0.15 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM
POWER_WIDTH	*	Y	0.600 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
POWER_CTL	*	Y	0.300 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
RCOMP	*	Y	0.254 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER	BGA_P1MM	POWER_CTL
POWER	*	POWER_WIDTH
VR_CTL_PHY	BGA_P1MM	DEFAULT
VR_CTL_PHY	*	POWER_CTL

SPACING RULE SET

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?
6:1_SPACING	*	0.6 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000
SWITCHNODE	*	0.8 MM	1000

CONSTRAINTS FOR BGA AREA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	0.2 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P1MM
CLK_LPC	*	BGA_P1MM	BGA_P1MM
CLK_PCI	*	BGA_P1MM	BGA_P1MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.150 MM	?
2X_DIELECTRIC	TOP,BOTTOM	0.160 MM	?
3X_DIELECTRIC	*	0.220 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.240 MM	?
4X_DIELECTRIC	*	0.300 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.320 MM	?
5X_DIELECTRIC	*	0.380 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.400 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	*	*	STANDARD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER	*	*	STANDARD

SYNC MASTER=K74 MASTER SYNC DATE=N/A

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K74/K75 RULE DEFINITIONS

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_39S	*	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=STANDARD	=STANDARD
MEM_35S	*	=35_OHM_SE	=35_OHM_SE	=35_OHM_SE	=35_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DQ_ODD2DQ_ODD	*	=3:1_SPACING	?
MEM_DQ_ODD2MEM	*	=3:1_SPACING	?
MEM_DQ_EVEN2DQ_EVEN	*	=3:1_SPACING	?
MEM_DQ_EVEN2MEM	*	=3:1_SPACING	?
MEM_DQ_EVEN2DQ_ODD	*	=5:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	=3:1_SPACING	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DQ_ODD	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM
MEM_CLK	MEM_DQ_EVEN	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_ODD	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_EVEN	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_ODD	MEM_CLK	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_CTRL	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_CMD	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_DQ_ODD	*	MEM_DQ_ODD2DQ_ODD
MEM_DQ_ODD	MEM_DQS	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_DQ_EVEN	*	MEM_DQ_EVEN2DQ_ODD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_EVEN	MEM_CLK	*	MEM_DQ_EVEN2MEM
MEM_DQ_EVEN	MEM_CTRL	*	MEM_DQ_EVEN2MEM
MEM_DQ_EVEN	MEM_CMD	*	MEM_DQ_EVEN2MEM
MEM_DQ_EVEN	MEM_DQ_EVEN	*	MEM_DQ_EVEN2DQ_EVEN
MEM_DQ_EVEN	MEM_DQS	*	MEM_DQ_EVEN2MEM
MEM_DQ_EVEN	MEM_DQ_ODD	*	MEM_DQ_EVEN2DQ_ODD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQ_ODD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQ_EVEN	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DQ_ODD	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM
MEM_CMD	MEM_DQ_EVEN	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DQ_ODD	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER
MEM_DQ_EVEN	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_POWER_WIDTH	*	Y	0.500 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_POWER_PHY	*	MEM_POWER_WIDTH

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_POWER	*	0.2 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_RCOMP_PHY	*	Y	0.175 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_RCOMP	*	0.2 MM	?

Memory Net Properties

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
	MEM_70D	MEM_CLK	MEM_A_CLK_P<3..0>	11 32
	MEM_70D	MEM_CLK	MEM_A_CLK_N<3..0>	11 32
	MEM_39S	MEM_CTRL	MEM_A_CKE<3..0>	11 30
	MEM_39S	MEM_CTRL	MEM_A_CS_L<3..0>	11 30
	MEM_39S	MEM_CTRL	MEM_A_ODT<3..0>	11 30
	MEM_35S	MEM_CMD	MEM_A_A<15..0>	11 30
	MEM_35S	MEM_CMD	MEM_A_BA<2..0>	11 30
	MEM_35S	MEM_CMD	MEM_A_RAS_L	11 30
	MEM_35S	MEM_CMD	MEM_A_CAS_L	11 30
	MEM_35S	MEM_CMD	MEM_A_WE_L	11 30
	MEM_45S	MEM_DQ_EVEN	MEM_A_DQ<7..0>	11 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DM<0>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DQ<15..8>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DM<1>	11 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DQ<23..16>	11 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DM<2>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DQ<31..24>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DM<3>	11 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DQ<39..32>	11 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DM<4>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DQ<47..40>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DM<5>	11 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DQ<55..48>	11 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DM<6>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DQ<63..56>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DM<7>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	11 32
	MEM_70D	MEM_CLK	MEM_B_CLK_P<3..0>	11 32
	MEM_70D	MEM_CLK	MEM_B_CLK_N<3..0>	11 32
	MEM_39S	MEM_CTRL	MEM_B_CKE<3..0>	11 31
	MEM_39S	MEM_CTRL	MEM_B_CS_L<3..0>	11 31
	MEM_39S	MEM_CTRL	MEM_B_ODT<3..0>	11 31
	MEM_35S	MEM_CMD	MEM_B_A<15..0>	11 31
	MEM_35S	MEM_CMD	MEM_B_BA<2..0>	11 31
	MEM_35S	MEM_CMD	MEM_B_RAS_L	11 31
	MEM_35S	MEM_CMD	MEM_B_CAS_L	11 31
	MEM_35S	MEM_CMD	MEM_B_WE_L	11 31
	MEM_45S	MEM_DQ_EVEN	MEM_B_DQ<7..0>	11 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DM<0>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DQ<15..8>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DM<1>	11 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DQ<23..16>	11 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DM<2>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DQ<31..24>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DM<3>	11 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DQ<39..32>	11 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DM<4>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DQ<47..40>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DM<5>	11 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DQ<55..48>	11 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DM<6>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DQ<63..56>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DM<7>	11 32

MEMORY POWER PROPERTIES

NET_TYPE

VOLTAGE	PHYSICAL	SPACING		
	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_A	11 28
	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_B	11 28

Memory Net Properties

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	11 32
1.15V	MEM_RCOMP_PHY	MEM_RCOMP	CPU_SM_RCOMP0	10
1.15V	MEM_RCOMP_PHY	MEM_RCOMP	CPU_SM_RCOMP1	10
1.15V	MEM_RCOMP_PHY	MEM_RCOMP	CPU_SM_RCOMP2	10

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: Memory Constraints

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=4X_DIELECTRIC	?
CLK_PCIE	*	0.5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

CPU

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_RCOMP_PHY	*	Y	0.254 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_ITP	*	0.2 MM	?
CPU_RCOMP	*	0.2 MM	?

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=5X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=5X_DIELECTRIC	?

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
CPU ITP				
	CPU_50S	CPU_ITP	XDP_BPM_L<7..0>	10 24
	CPU_50S	CPU_ITP	CPU_CFG<17..0>	9 14 24
	CPU_50S	CPU_ITP	XDP_OBSDATA_A<3..0>	24
CPU_MISC				
	CPU_RCOMP_PHY	CPU_RCOMP	CPU_PEG_COMP	9
	CPU_RCOMP_PHY	CPU_RCOMP	CPU_PEG_RBIAS	9
	CPU_RCOMP_PHY	CPU_RCOMP	CPU_COMP3	10
	CPU_RCOMP_PHY	CPU_RCOMP	CPU_COMP2	10
	CPU_RCOMP_PHY	CPU_RCOMP	CPU_COMP1	10
	CPU_RCOMP_PHY	CPU_RCOMP	CPU_COMP0	10

ANY OTHER LYNNFIELD CONSTRAINTS NOT COVERED ON PAGES 101 AND 107 SHOULD GO ON THIS PAGE TOO

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
PCIE GRAPHICS				
	PCIE_85D	PCIE	PEG_R2D_C_P<15..0>	8 76
	PCIE_85D	PCIE	PEG_R2D_C_N<15..0>	8 76
	PCIE_85D	PCIE	PEG_D2R_P<15..0>	8 76
	PCIE_85D	PCIE	PEG_D2R_N<15..0>	8 76
	PCIE_85D	PCIE	MXM_PCIE_R2D_P<15..0>	74 76
	PCIE_85D	PCIE	MXM_PCIE_R2D_N<15..0>	74 76
	PCIE_85D	PCIE	MXM_PCIE_D2R_P<15..0>	74 76
	PCIE_85D	PCIE	MXM_PCIE_D2R_N<15..0>	74 76
PCIE I/O				
	PCIE_85D	PCIE	PCIE_MINI_R2D_P	33
	PCIE_85D	PCIE	PCIE_MINI_R2D_N	33
	PCIE_85D	PCIE	PCIE_MINI_R2D_C_P	17 33
	PCIE_85D	PCIE	PCIE_MINI_R2D_C_N	17 33
	PCIE_85D	PCIE	PCIE_MINI_D2R_P	17 33
	PCIE_85D	PCIE	PCIE_MINI_D2R_N	17 33
	PCIE_85D	PCIE	PCIE_FW_R2D_P	39
	PCIE_85D	PCIE	PCIE_FW_R2D_N	39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	17 39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	17 39
	PCIE_85D	PCIE	PCIE_FW_D2R_P	17 39
	PCIE_85D	PCIE	PCIE_FW_D2R_N	17 39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	39
DMI				
	PCIE_85D	PCIE	DMI_S2N_P<3..0>	9 18
	PCIE_85D	PCIE	DMI_S2N_N<3..0>	9 18
	PCIE_85D	PCIE	DMI_N2S_P<3..0>	9 18
	PCIE_85D	PCIE	DMI_N2S_N<3..0>	9 18
FDI				
PCIE REF CLOCKS				
	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_P	8
	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_N	8
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	17 33
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	17 33
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	17 39
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	17 39
	ENET_100D	ENET_MII	PCIE_CLK100M_ENET_P	17 37
	ENET_100D	ENET_MII	PCIE_CLK100M_ENET_N	17 37
SATA				
	SATA_85D	SATA	SATA_HDD_R2D_C_P	17 42
	SATA_85D	SATA	SATA_HDD_R2D_C_N	17 42
	SATA_85D	SATA	SATA_HDD_R2D_P	42
	SATA_85D	SATA	SATA_HDD_R2D_N	42
	SATA_85D	SATA	SATA_HDD_D2R_P	17 42
	SATA_85D	SATA	SATA_HDD_D2R_N	17 42
	SATA_85D	SATA	SATA_HDD_D2R_C_P	42
	SATA_85D	SATA	SATA_HDD_D2R_C_N	42
	SATA_85D	SATA	SATA_ODD_R2D_C_P	17 42
	SATA_85D	SATA	SATA_ODD_R2D_C_N	17 42
	SATA_85D	SATA	SATA_ODD_R2D_P	42
	SATA_85D	SATA	SATA_ODD_R2D_N	42
	SATA_85D	SATA	SATA_ODD_D2R_P	17 42
	SATA_85D	SATA	SATA_ODD_D2R_N	17 42
	SATA_85D	SATA	SATA_ODD_D2R_C_P	42
	SATA_85D	SATA	SATA_ODD_D2R_C_N	42
CLOCKS				
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_CPU_P	10 20
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_CPU_N	10 20
	CLK_PCIE_100D	CLK_PCIE	GFX_CLK120M_DPLLSS_P	10 17
	CLK_PCIE_100D	CLK_PCIE	GFX_CLK120M_DPLLSS_N	10 17
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_ITP_P	10 24
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_ITP_N	10 24
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_CPU_P	10 17
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_CPU_N	10 17
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_PCH_P	17 25
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_PCH_N	17 25
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_PCH_P	17 25
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_PCH_N	17 25
	CLK_PCIE_100D	CLK_PCIE	PCH_CLK96M_DOT_P	17 25
	CLK_PCIE_100D	CLK_PCIE	PCH_CLK96M_DOT_N	
	CLK_PCIE_100D	CLK_PCIE	PCH_CLK100M_SATA_P	17 25
	CLK_PCIE_100D	CLK_PCIE	PCH_CLK100M_SATA_N	17 25

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
PCIE/DMI/FDI/SATA CONSTRAINTS

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D
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PCH CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH	*	0.2 MM	?
COMP_PCH	*	0.2 MM	?

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	0.2 MM	?

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	0.15 MM	?
CLK_LPC	*	0.2 MM	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	0.2 MM	?

XTAL Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCI_55S	PCI	PCI_REQ0_L	19
	PCI_55S	PCI	PCI_REQ1_L	19
	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIOUT	19 27
	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIIN	17 27
	LPC_55S	LPC	LPC_AD<3..0>	17 46 48
	LPC_55S	LPC	LPC_FRAME_L	17 46 48
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	19 27
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	27 46
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	27 48
	CLK_LPC_55S	PM	PM_CLK32K_SUSCLK_R	8 18 91
	CLK_LPC_55S	PM	PM_CLK32K_SUSCLK	8 46 91
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	19 27
	USB_90D	USB	USB_EXTA_P	34 43
	USB_90D	USB	USB_EXTA_N	34 43
	USB_90D	USB	USB_PORT0_P	43
	USB_90D	USB	USB_PORT0_N	43
	USB_90D	USB	USB_EXTB_P	35 43
	USB_90D	USB	USB_EXTB_N	35 43
	USB_90D	USB	USB_PORT1_P	43
	USB_90D	USB	USB_PORT1_N	43
	USB_90D	USB	USB_EXTC_P	34 43
	USB_90D	USB	USB_EXTC_N	34 43
	USB_90D	USB	USB_PORT2_P	43
	USB_90D	USB	USB_PORT2_N	43
	USB_90D	USB	USB_EXTD_P	35 43
	USB_90D	USB	USB_EXTD_N	35 43
	USB_90D	USB	USB_D_MUXED_P	43
	USB_90D	USB	USB_D_MUXED_N	43
	USB_90D	USB	USB_PORT3_P	43
	USB_90D	USB	USB_PORT3_N	43
	USB_90D	USB	USB_CAMERA_P	34 44
	USB_90D	USB	USB_CAMERA_N	34 44
	USB_90D	USB	USB_CAMERA_L_P	44 92
	USB_90D	USB	USB_CAMERA_L_N	44 92
	USB_90D	USB	USB_BT_P	35 44
	USB_90D	USB	USB_BT_N	35 44
	USB_90D	USB	USB_BT_L_P	44 92
	USB_90D	USB	USB_BT_L_N	44 92
	USB_90D	USB	USB_IR_P	34 44
	USB_90D	USB	USB_IR_N	34 44
	USB_90D	USB	USB_IR_L_P	44 92
	USB_90D	USB	USB_IR_L_N	44 92
	USB_90D	USB	USB_SDCARD_P	35 44
	USB_90D	USB	USB_SDCARD_N	35 44
	USB_90D	USB	USB_SDCARD_L_P	44 92
	USB_90D	USB	USB_SDCARD_L_N	44 92
	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1	17 27
	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2	17 27
	CLK_XTAL	XTAL	CK505_XTAL_IN	25
	CLK_XTAL	XTAL	CK505_XTAL_OUT	25
	CLK_PCH_55S	CLK_PCH	PCH_CLK14P3M_REFCLK	17 25
	USB_90D	USB	USB_HUB1_UP_P	19 34
	USB_90D	USB	USB_HUB1_UP_N	19 34
	USB_90D	USB	USB_HUB2_UP_P	19 35
	USB_90D	USB	USB_HUB2_UP_N	19 35

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SPI_55S	SPI	SPI_CLK_R	17 48 55
	SPI_55S	SPI	SPI_CLK	55
	SPI_55S	SPI	SPI_MOSI_R	17 48 55
	SPI_55S	SPI	SPI_MOSI	55
	SPI_55S	SPI	SPI_MISO	17 48 55
	SPI_55S	SPI	SPI_MISO_R	55
	SPI_55S	SPI	SPI_CS0_R_L	17 48
	SPI_55S	SPI	SPI_CS0_L	48
	SPI_55S	SPI	SPI_MLB_CS_L	48 55
	SPI_55S	SPI	SPI_ALT_CS_L	48
	SPI_55S	SPI	SPIROM_USE_MLB	20 48
	SPI_55S	SPI	SPI_ALT_MOSI	48
	SPI_55S	SPI	SPI_ALT_MISO	48
	SPI_55S	SPI	SPI_ALT_CLK	48
	HDA_55S	HDA	HDA_BIT_CLK	17 56
	HDA_55S	HDA	HDA_BIT_CLK_R	17
	HDA_55S	HDA	HDA_RST_L	17 56
	HDA_55S	HDA	HDA_RST_R_L	17
	HDA_55S	HDA	HDA_SDOUT	17 56
	HDA_55S	HDA	HDA_SDOUT_R	17
	HDA_55S	HDA	HDA_SYNC	17 56
	HDA_55S	HDA	HDA_SYNC_R	17
	HDA_55S	HDA	HDA_SDIN0	17 56
	HDA_55S	HDA	AUD_SDI_R	56
		HDA	AUD_SPDIF_IN	60 77
		HDA	AUD_SPDIF_OUT	56 60
		HDA	AUD_SPDIF_CHIP	56
	HDA_55S	HDA	AUD_SPKR_OUTL01L_NOUT	59 60 92
	HDA_55S	HDA	AUD_SPKR_OUTL01L_POUT	59 60 92
	HDA_55S	HDA	AUD_SPKR_OUTL01R_NOUT	58 60 92
	HDA_55S	HDA	AUD_SPKR_OUTL01R_POUT	58 60 92
	HDA_55S	HDA	AUD_SPKR_OUTL02L_NOUT	59 60 92
	HDA_55S	HDA	AUD_SPKR_OUTL02L_POUT	59 60 92
	HDA_55S	HDA	AUD_SPKR_OUTL02R_NOUT	58 60 92
	HDA_55S	HDA	AUD_SPKR_OUTL02R_POUT	58 60 92
	CLK_XTAL	XTAL	PCH_CLK25M_XTALOUT	17 27
	CLK_XTAL	XTAL	PCH_CLK25M_XTALIN	17 27
	PCH_55S	COMP_PCH	PCH_USB_RBIAS	19
	PCH_55S	COMP_PCH	PCH_SATAICOMP	17
	PCH_55S	COMP_PCH	PCH_XCLK_RCOMP	17
	PCH_55S	COMP_PCH	PCH_DMI_COMP	18
	CLK_XTAL	XTAL	USB_HUB1_XTAL1	34
	CLK_XTAL	XTAL	USB_HUB1_XTAL2	34
	PCH_55S	COMP_PCH	USB_HUB1_RBIAS	34
	CLK_XTAL	XTAL	USB_HUB2_XTAL1	35
	CLK_XTAL	XTAL	USB_HUB2_XTAL2	35
	PCH_55S	COMP_PCH	USB_HUB2_RBIAS	35

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE

IBEX PEAK CONSTRAINTS

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D

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CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	0.3 MM	?
ENET_SE	*	=STANDARD	?

SOURCE:BROADCOM 5764M-DS04-RDS. PAGE 38

CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_DIFF	*	0.6 MM	?

CAESAR IV (SD) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD	*	=3:1_SPACING	?

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

AUDIO CONSTRAINTS

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	=3:1_SPACING	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUD_DIFF	*	1:1_DIFFPAIR

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	ENET_50S	ENET_SE	BCM5764_RDAC 37
	ENET_50S	BUF0_CLK	BCM5764_CLK25M_XTALI 36 37
	ENET_50S	BUF0_CLK	BCM5764_CLK25M_XTALO 36 37
	ENET_50S	BUF0_CLK	BCM5764_CLK25M_XTAL 36
	ENET_100D	ENET_DIFF	ENET_MDI_P<3..0> 37 38
	ENET_100D	ENET_DIFF	ENET_MDI_N<3..0> 37 38
	ENET_100D	ENET_DIFF	ENET_MDI_T_P<3..0> 38
	ENET_100D	ENET_DIFF	ENET_MDI_T_N<3..0> 38
	ENET_100D	ENET_MII	PCIE_ENET_R2D_P 37
	ENET_100D	ENET_MII	PCIE_ENET_R2D_N 37
	ENET_100D	ENET_MII	PCIE_ENET_D2R_P 17 37
	ENET_100D	ENET_MII	PCIE_ENET_D2R_N 17 37
	ENET_100D	ENET_MII	PCIE_ENET_R2D_C_P 17 37
	ENET_100D	ENET_MII	PCIE_ENET_R2D_C_N 17 37
	ENET_100D	ENET_MII	PCIE_ENET_D2R_C_P 37
	ENET_100D	ENET_MII	PCIE_ENET_D2R_C_N 37
	SD_50S	SD	SDCONN_CMD 37 45
	SD_50S	SD	SDCONN_CLK 37 45
	SD_50S	SD	SDCONN_CLK_R 45
	SD_50S	SD	SDCONN_DATA<7..0> 37 45
	SD_50S	SD	BCM57765_CR_DATA<7..4> 37

FireWire Net Properties

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	FW_110D	FW_TP	FW_PORT0_TPA_P 40 41
	FW_110D	FW_TP	FW_PORT0_TPA_N 40 41
	FW_110D	FW_TP	FW_PORT0_TPB_P 40 41
	FW_110D	FW_TP	FW_PORT0_TPB_N 40 41
	FW_110D	FW_TP	FW_PORT0_TPA_F_P 41
	FW_110D	FW_TP	FW_PORT0_TPA_F_N 41
	FW_110D	FW_TP	FW_PORT0_TPB_F_P 41
	FW_110D	FW_TP	FW_PORT0_TPB_F_N 41
PORT 1 & 2 NOT USED			
	FW_110D	FW_TP	FW_P0_TPA_L_P 40
	FW_110D	FW_TP	FW_P0_TPA_L_N 40
	FW_110D	FW_TP	FW_P0_TPB_L_P 40
	FW_110D	FW_TP	FW_P0_TPB_L_N 40
UNUSED FW NETS PHYSICAL PROPERTIES			
	FW_110D	FW_TP	FW_P1_TPA_P 39 40
	FW_110D	FW_TP	FW_P1_TPA_N 39 40
	FW_110D	FW_TP	FW_P2_TPA_P 39 40
	FW_110D	FW_TP	FW_P2_TPA_N 39 40

AUDIO NET PROPERTIES

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	AUD_DIFF	AUDIO	AUDAMPINBLN 58
	AUD_DIFF	AUDIO	AUDAMPINBLP 58
	AUD_DIFF	AUDIO	AUDAMPINLN 58
	AUD_DIFF	AUDIO	AUDAMPINLP 58
	AUD_DIFF	AUDIO	AUD_LO2_N_R 56 58
	AUD_DIFF	AUDIO	AUD_LO2_P_R 56 58
	AUD_DIFF	AUDIO	AUDAMPINBRN 58
	AUD_DIFF	AUDIO	AUDAMPINBRP 58
	AUD_DIFF	AUDIO	AUDAMPINRN 58
	AUD_DIFF	AUDIO	AUDAMPINRP 58
	AUD_DIFF	AUDIO	AUD_LO1_N_R 56 58
	AUD_DIFF	AUDIO	AUD_LO1_P_R 56 58
	AUD_DIFF	AUDIO	AUDAMPINCLN 59
	AUD_DIFF	AUDIO	AUDAMPINCLP 59
	AUD_DIFF	AUDIO	AUD_AMPINLN 59
	AUD_DIFF	AUDIO	AUD_AMPINLP 59
	AUD_DIFF	AUDIO	AUD_LO2_N_L 56 59
	AUD_DIFF	AUDIO	AUD_LO2_P_L 56 59
	AUD_DIFF	AUDIO	AUDAMPINCRN 59
	AUD_DIFF	AUDIO	AUDAMPINCRP 59
	AUD_DIFF	AUDIO	AUD_AMPINRN 59
	AUD_DIFF	AUDIO	AUD_AMPINRP 59
	AUD_DIFF	AUDIO	AUD_LO1_N_L 56 59
	AUD_DIFF	AUDIO	AUD_LO1_P_L 56 59

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
ENET/SD/FW/AUD CONSTRAINTS

Apple Inc.

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.08MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3:1_SPACING	?

PAIRS SHOULD BE WITHIN 100 MILS OF CLOCK LENGTH.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	
ASSINGED IN CONT. MGR.	PHYSICAL	SPACING
	DP_85D	DISPLAYPORT

MXM_DP_C_ML_P<3..0> 74 80
MXM_DP_C_ML_N<3..0> 74 80
DP_INT_ML_C_P<3..0> 78 80
DP_INT_ML_C_N<3..0> 78 80
MXM_DP_C_AUX_P 74 80
MXM_DP_C_AUX_N 74 80

DP_INT_AUX_P 78 80
DP_INT_AUX_N 78 80

MXM_DP_A_ML_P<3..0> 74 80
MXM_DP_A_ML_N<3..0> 74 80
GPU_DP_EXT_ML_P<3..0> 79 80
GPU_DP_EXT_ML_N<3..0> 79 80
RDRV_DP_EXT_ML_P<3..0> 79 80
RDRV_DP_EXT_ML_N<3..0> 79 80

DP_EXT_ML_C_P<3..0> 80 81
DP_EXT_ML_C_N<3..0> 80 81
DP_ML_CONN_P<3..0> 81
DP_ML_CONN_N<3..0> 81

MXM_DP_A_AUX_P 74 80
MXM_DP_A_AUX_N 74 80
RDRV_DP_EXT_AUX_P 79
RDRV_DP_EXT_AUX_N 79

DP_EXT_AUX_P 79 80 81
DP_EXT_AUX_N 79 80 81

UNUSED VIDEO NET PHYSICAL CONSTRAINTS

MXM_DP_B_AUX_P 74 77
MXM_DP_B_AUX_N 74 77

MXM_DP_D_AUX_P 74 77
MXM_DP_D_AUX_N 74 77
MXM_LVDS_A_CLK_P 75 77
MXM_LVDS_A_CLK_N 75 77

MXM_LVDS_B_CLK_P 75 77
MXM_LVDS_B_CLK_N 75 77
MXM_DP_B_ML_P<3..0> 74 77
MXM_DP_B_ML_N<3..0> 74 77
MXM_DP_D_ML_P<3..0> 74 77
MXM_DP_D_ML_N<3..0> 74 77
MXM_LVDS_A_DATA_P<3..0> 75 77
MXM_LVDS_A_DATA_N<3..0> 75 77
MXM_LVDS_B_DATA_P<3..0> 75 77
MXM_LVDS_B_DATA_N<3..0> 75 77

SYNC_MASTER=DAVE SYNC_DATE=01/07/2010

PAGE TITLE
GRAPHICS CONSTRAINTS

Apple Inc.

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SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_5S	*	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	4:1_SPACING
THERMAL	POWER	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR
SNS_DIFF	*	1:1_DIFFPAIR

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
SMB_5S	SMB	SMBUS_SMC_A_S3_SCL	49
SMB_5S	SMB	SMBUS_SMC_A_S3_SDA	49
SMB_5S	SMB	SMBUS_SMC_B_S0_SCL	49
SMB_5S	SMB	SMBUS_SMC_B_S0_SDA	49
SMB_5S	SMB	SMBUS_SMC_0_S0_SCL	49
SMB_5S	SMB	SMBUS_SMC_0_S0_SDA	49
SMB_5S	SMB	SMBUS_SMC_BSA_SCL	49
SMB_5S	SMB	SMBUS_SMC_BSA_SDA	49
SMB_5S	SMB	SMBUS_SMC_MGMT_SCL	49 88
SMB_5S	SMB	SMBUS_SMC_MGMT_SDA	49 88
SMB_5S	SMB	SMBUS_SMC_MGMT_SCL	49 88
SMB_5S	SMB	SMBUS_SMC_MGMT_SDA	49 88
SMB_5S	SMB	SMBUS_PCH_CLK	17 49
SMB_5S	SMB	SMBUS_PCH_DATA	17 49
SMB_5S	SMB	SML_PCH_0_CLK	17 49
SMB_5S	SMB	SML_PCH_0_DATA	17 49
SMB_5S	SMB	SML_PCH_1_CLK	17 49
SMB_5S	SMB	SML_PCH_1_DATA	17 49
CLK_XTAL	XTAL	SMC_EXTAL	46 47
CLK_XTAL	XTAL	SMC_XTAL	46 47

SMC THERMAL NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
THERM_DIFF	THERMAL	SNS_T1_DP1	52
THERM_DIFF	THERMAL	SNS_T1_DN1	52
THERM_DIFF	THERMAL	SNS_T1_DP2_DN3	44 52
THERM_DIFF	THERMAL	SNS_T1_DN2_DP3	44 52
THERM_DIFF	THERMAL	SNS_T2_DP1	52
THERM_DIFF	THERMAL	SNS_T2_DN1	52
THERM_DIFF	THERMAL	SNS_T2_DP2	52
THERM_DIFF	THERMAL	SNS_T2_DN2	52
THERM_DIFF	THERMAL	SNS_T2_DP3	52
THERM_DIFF	THERMAL	SNS_T2_DN3	52
THERM_DIFF	THERMAL	SNS_ODD_P	52 92
THERM_DIFF	THERMAL	SNS_ODD_N	52 92
THERM_DIFF	THERMAL	SNS_CPU_H_P	52
THERM_DIFF	THERMAL	SNS_CPU_H_N	52
THERM_DIFF	THERMAL	SNS_SKIN_P	52 92
THERM_DIFF	THERMAL	SNS_SKIN_N	52 92
THERM_DIFF	THERMAL	SNS_AMB_P	52 54 92
THERM_DIFF	THERMAL	SNS_AMB_N	52 54 92
THERM_DIFF	THERMAL	SNS_MXM_P	52
THERM_DIFF	THERMAL	SNS_MXM_N	52
	THERMAL	HDD_OOB_TEMP_FILT	51 92
	THERMAL	HDD_OOB_TEMP	51
	THERMAL	HDD_OOB_TEMP_R	51
	THERMAL	SMC_HDD_OOB_TEMP	46 51

SMC VOLTAGE/CURRENT NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
THERM_DIFF	THERMAL	SENSE_MXM_P	50
THERM_DIFF	THERMAL	SENSE_MXM_N	50
THERM_DIFF	THERMAL	SENSE_VTT_R_P	
THERM_DIFF	THERMAL	SENSE_VTT_R_N	
THERM_DIFF	THERMAL	SENSE_CPU_1V5_P	50
THERM_DIFF	THERMAL	SENSE_CPU_1V5_N	50
THERM_DIFF	THERMAL	SENSE_CPU_VTT_P	
THERM_DIFF	THERMAL	SENSE_CPU_VTT_N	
	THERMAL	GND_SMC_AVSS	46 47 50
	THERMAL	SMC_CPU_1V5_ISENSE	46 50
	THERMAL	SMC_CPU_1V5_ISENSE_R	50
	THERMAL	SMC_CPU_1V5_VSENSE	46 50
	THERMAL	SMC_CPU_VSENSE	46 50
VID_PHY	VR_CTL	VR_CPU_IOUT	12 65
THERM_DIFF	THERMAL	VR_ISNS_CPU_P	50
THERM_DIFF	THERMAL	VR_ISNS_CPU_N	50
	THERMAL	SNS_PS_CPU_ISNS	50
	THERMAL	SMC_CPU_ISENSE	46 50

SYNC_MASTER=TEMP SYNC_DATE=12/09/2009

PAGE TITLE: SMC Constraints

Apple Inc.

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NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SWITCHNODE	SWITCHNODE	BGA_P1MM	BGA_P2MM
SWITCHNODE	POWER	BGA_P1MM	BGA_P2MM
SWITCHNODE	GND	BGA_P1MM	BGA_P2MM
SWITCHNODE	*	BGA_P1MM	BGA_P2MM
SWITCHNODE	POWER	*	6:1_SPACING
SWITCHNODE	GND	*	6:1_SPACING
SWITCHNODE	*	*	SWITCHNODE

POWER NET PROPERTIES

NET_TYPE				
PHYSICAL	SPACING	VOLTAGE		
POWER	SWITCHNODE	1.5V	VR_CPU_PHASE1	66
POWER	SWITCHNODE	1.5V	VR_CPU_PHASE2	66
POWER	SWITCHNODE	1.5V	VR_CPU_PHASE3	66
POWER	SWITCHNODE	3.3V	P3V3S5_REG_PHASE	70
POWER	SWITCHNODE	5V	P5VS3_REG_PHASE	70
POWER	SWITCHNODE	1.1V	VTT_REG_PHASE	
POWER	SWITCHNODE	3.4V	P3V42G3H_SW	72
POWER	SWITCHNODE	1.05V	PCHCORE_REG_PHASE	69
POWER	SWITCHNODE	1.5V	DDR_REG_PHASE	71
POWER	SWITCHNODE	1.8V	P1V8_REG_PHASE	71
POWER	POWER	1.5V	PP0V75_S3_MEM_VREFCA_A	28 30
POWER	POWER	1.5V	PP0V75_S3_MEM_VREFCA_B	28 31
POWER	POWER	1.5V	PP0V75_S3_MEM_VREFDQ_A	28 30
POWER	POWER	1.5V	PP0V75_S3_MEM_VREFDQ_B	28 31
POWER	POWER	12V	PP12V_AUD_SPKRAMP_PLANE	
POWER	POWER	12V	PP12V_S0	5 64
POWER	POWER	12V	PP12V_S0_CPU_FLTRD	65 66
POWER	POWER	12V	PP12V_S0_FAN0_L	53 92
POWER	POWER	12V	PP12V_S0_FAN1_L	53 92
POWER	POWER	12V	PP12V_S0_FAN2_L	54 92
POWER	POWER	12V	PP12V_G3H	5 72
POWER	POWER	12V	PP12V_S5	5
POWER	POWER	12V	FW_PORT0_VP	41
POWER	POWER	12V	FW_PORT0_VP_F	41
POWER	POWER	12V	PPVP_FW_PHY_CPS	40 41
POWER	POWER	1.1V	PPVCORE_S0_CPU	5
POWER	POWER	1.1V	PPVCORE_S0_CPU_REG1	66
POWER	POWER	1.1V	PPVCORE_S0_CPU_REG2	66
POWER	POWER	1.1V	PPVCORE_S0_CPU_REG3	66
POWER	POWER	1.05V	PP1V05_S0	5
POWER	POWER	1.05V	PP1V05_S0_CK505_F	25
POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLA	16 21
POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLB	16 21
POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLB_F	
POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLL_EXP	21 23
POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLL_FDI	21 23
POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLL_SATA	21 23
POWER	POWER	1.05V	PP1V05_S0_PCH_VCCA_CLK	21 23
POWER	POWER	1.05V	PP1V05_SM_PCH_LAN	5
POWER	POWER	1.1V	PPVTT_S0	5 50
POWER	POWER	0.75V	PPVTT_S0_DDR	5
POWER	POWER	0.75V	PP0V75_S0	5
POWER	POWER	1.5V	PP1V5_S0	5
POWER	POWER	1.5V	PP1V5_S0_CK505_F	25
POWER	POWER	1.5V	PP1V5_S0_CK505_R	25
POWER	POWER	1.5V	PP1V5_S3	5
POWER	POWER	1.5V	PP1V5_CPU_MEM	5 50
POWER	POWER	1.5V	PP1V8R1V5_S0_PCH_VCCVRM	21 23
POWER	POWER	1.5V	PP1V5_FW_VDDA	39
POWER	POWER	1.5V	PP1V8_S0	5
POWER	POWER	1.96V	PP1V96_FW_PLLVDD	39
POWER	POWER	1.96V	PP1V95_FW_FWPHY	39 40

POWER NET PROPERTIES

NET_TYPE				
PHYSICAL	SPACING	VOLTAGE		
POWER	POWER	3.3V	PP3V3_S0	5
POWER	POWER	3.3V	PP3V3_S0_CK505_F	25
POWER	POWER	3.3V	PP3V3_S0_DPFUSE	81
POWER	POWER	3.3V	PP3V3_S0_DPPWR	81
POWER	POWER	3.3V	PP3V3_S0_HS_F	62
POWER	POWER	3.3V	PP3V3_S0_PCH_VCCA_DAC	16 21
POWER	POWER	3.3V	PP3V3_S0_TSENS_R	
POWER	POWER	3.3V	PP3V3_S3	5 92
POWER	POWER	3.3V	PP3V3_S3_BT_FLT	44
POWER	POWER	3.3V	PP3V3_S3_SDCARD_FLT	44
POWER	POWER	3.3V	PP3V3_S5	5
POWER	POWER	3.3V	PPVTT_S3_DDR_BUF	71
POWER	POWER	3.3V	PPV_S0_MXM_PWRSRC	60
POWER	POWER	3.3V	PPVOUT_S0_PCH_DCPSST	21
POWER	POWER	3.3V	PPVOUT_S5_PCH_DCPSUS	21
POWER	POWER	3.3V	PPVOUT_S5_PCH_DCPSUSBYP	21
POWER	POWER	3.3V	PPVOUT_G3_PCH_DCPRTC	21
POWER	POWER	3.3V	PPVOUT_S0_PCH_VCCRTC_NCTF	
POWER	POWER	3.3V	PPVBATT_G3_RTC	27
POWER	POWER	3.3V	PPVBATT_G3_RTC_R	27
POWER	POWER	3.3V	PP3V3_AUDIO_SPDIF_JACK	60 92
POWER	POWER	3.3V	PP3V3_FW_AVDD	39
POWER	POWER	3.3V	PP3V3_FW_ESD	41
POWER	POWER	3.3V	PP3V3_FW_PLLVDD	39
POWER	POWER	3.3V	PP3V3_FW_VDDA	39
POWER	POWER	3.3V	PP3V3_G3_RTC	17 21 23 27
POWER	POWER	3.3V	PP_ENET_CTRL12	36
POWER	POWER	3.4V	PP3V3_G3H_SMC_AVCC	46
POWER	POWER	3.3V	PP3V3_G3H_AVREF_SMC	46 47
POWER	POWER	3.42V	PP3V42_G3H	5
POWER	POWER	4.5V	4V5_REG_IN	56
POWER	POWER	4.5V	PP4V5_AUDIO_ANALOG	56
POWER	POWER	5V	PP5V_S0	5 92
POWER	POWER	5V	PP5V_S0_CPU_VCORE_VCC	65
POWER	POWER	5V	PP5V_S0_PCH_V5REF	21 23
POWER	POWER	5V	PP5V_S3	5 92
POWER	POWER	5V	PP5V_S3_DDR_REG_V5FILT	71
POWER	POWER	5V	PP5V_S3_CAMERA_FLT	44
POWER	POWER	5V	PP5V_S3_IR_FLT	44 92
POWER	POWER	5V	PP5V_S5	5
POWER	POWER	5V	PP5V_S5_PCH_V5REFSUS	21 23
POWER	POWER	5V	PP5V_USB2_PORT0	43
POWER	POWER	5V	PP5V_USB2_PORT0_F	43
POWER	POWER	5V	PP5V_USB2_PORT1	43
POWER	POWER	5V	PP5V_USB2_PORT1_F	43
POWER	POWER	5V	PP5V_USB2_PORT2	43
POWER	POWER	5V	PP5V_USB2_PORT2_F	43
POWER	POWER	5V	PP5V_USB2_PORT3	43
POWER	POWER	5V	PP5V_USB2_PORT3_F	43
POWER	POWER		DDR_REG_PGND	71
POWER	POWER		DDR_REG_CSGND	71

SENSING NET PROPERTIES

NET_TYPE			
PHYSICAL	SPACING		
SNS_DIFF	THERMAL	VR_CPU_ISNS1_P	65 66
SNS_DIFF	THERMAL	VR_CPU_ISNS1_N	65 66
SNS_DIFF	THERMAL	VR_CPU_ISNS1_R_P	65
SNS_DIFF	THERMAL	VR_CPU_ISNS1_R_N	65
SNS_DIFF	THERMAL	VR_CPU_ISNS2_P	65 66
SNS_DIFF	THERMAL	VR_CPU_ISNS2_N	65 66
SNS_DIFF	THERMAL	VR_CPU_ISNS2_R_P	65
SNS_DIFF	THERMAL	VR_CPU_ISNS2_R_N	65
SNS_DIFF	THERMAL	VR_CPU_ISNS3_P	65 66
SNS_DIFF	THERMAL	VR_CPU_ISNS3_N	65 66
SNS_DIFF	THERMAL	VR_CPU_ISNS3_R_P	65
SNS_DIFF	THERMAL	VR_CPU_ISNS3_R_N	65
SNS_DIFF		VR_CPU_VSEN	65
SNS_DIFF		VR_CPU_RGND	65
SNS_DIFF		VR_CPU_VSNS_R_N	65
SNS_DIFF		VR_CPU_VSNS_R_P	65
SNS_DIFF		VR_CPU_VSNS_XW_P	65
SNS_DIFF		VR_CPU_VSNS_XW_N	65
SNS_DIFF		CPU_VCC_PKG_SENSE_P	12 50 65
SNS_DIFF		CPU_VCC_PKG_SENSE_N	12 65
SNS_DIFF		VTT_REG_ISNS_P	
SNS_DIFF		VTT_REG_ISNS_N	
SNS_DIFF		CPU_VTTSENSE_P	12 68
SNS_DIFF		CPU_VTTSENSE_N	12 68
SNS_DIFF		CPU_VTTSENSE_R_P	
SNS_DIFF		CPU_VTTSENSE_R_N	
SNS_DIFF		VTT_REG_VSEN	
SNS_DIFF		VTT_REG_RGND	
SNS_DIFF		VTT_REG_RTO1	
SNS_DIFF		VTT_REG_RTR1	

VR CTRL NET PROPERTIES

NET_TYPE			
PHYSICAL	SPACING		
VR_CTL_PHY	VR_CTL	VR_CPU_PH1_SNUB	66
VR_CTL_PHY	VR_CTL	VR_CPU_PH2_SNUB	66
VR_CTL_PHY	VR_CTL	VR_CPU_PH3_SNUB	66
VR_CTL_PHY	VR_CTL	VR_CPU_PWM1	65 66
VR_CTL_PHY	VR_CTL	VR_CPU_PWM2	65 66
VR_CTL_PHY	VR_CTL	VR_CPU_PWM2_R	65
VR_CTL_PHY	VR_CTL	VR_CPU_PWM3	65 66
VR_CTL_PHY	VR_CTL	VR_CPU_PWM3_R	65
VR_CTL_PHY	VR_CTL	VR_CPU_PWM4_R	65
VR_CTL_PHY	VR_CTL	VR_CPU_REF	65
VR_CTL_PHY	VR_CTL	VR_CPU_SS	65
VR_CTL_PHY	VR_CTL	VR_CPU_TCOMP	65
VR_CTL_PHY	VR_CTL	VR_CPU_TM	65
VR_CTL_PHY	VR_CTL	VR_CPU_BOOT1_RC	66
VR_CTL_PHY	VR_CTL	VR_CPU_BOOT2_RC	66
VR_CTL_PHY	VR_CTL	VR_CPU_BOOT3_RC	66
VR_CTL_PHY	VR_CTL	VR_CPU_COMP	65
VR_CTL_PHY	VR_CTL	VR_CPU_COMP_R	65
VR_CTL_PHY	VR_CTL	VR_CPU_COMP_RC	65
VR_CTL_PHY	VR_CTL	VR_CPU_DAC	65
VR_CTL_PHY	VR_CTL	VR_CPU_DRV1_BOOT	66
VR_CTL_PHY	VR_CTL	VR_CPU_DRV1_GDSEL	66
VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV1_LGATE	66
VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV1_UGATE	66
VR_CTL_PHY	VR_CTL	VR_CPU_DRV2_BOOT	66
VR_CTL_PHY	VR_CTL	VR_CPU_DRV2_GDSEL	66
VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV2_LGATE	66
VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV2_UGATE	66
VR_CTL_PHY	VR_CTL	VR_CPU_DRV3_BOOT	66
VR_CTL_PHY	VR_CTL	VR_CPU_DRV3_GDSEL	66
VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV3_LGATE	66
VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV3_UGATE	66
VR_CTL_PHY	VR_CTL	VR_CPU_FAN	65
VR_CTL_PHY	VR_CTL	VR_CPU_FB	65
VR_CTL_PHY	VR_CTL	VR_CPU_FB_R	65
VR_CTL_PHY	VR_CTL	VR_CPU_FS	65
VR_CTL_PHY	VR_CTL	VR_CPU_IMON	50 65
VR_CTL_PHY	VR_CTL	VR_CPU_IOUT_PD	65
VR_CTL_PHY	SWITCHNODE	PCHCORE_REG_UGATE	69
VR_CTL_PHY	SWITCHNODE	PCHCORE_REG_LGATE	69
VR_CTL_PHY	VR_CTL	PCHCORE_REG_VFB	69
VR_CTL_PHY	VR_CTL	PCHCORE_REG_TON	69
VR_CTL_PHY	VR_CTL	PCHCORE_REG_TRIP	69
VR_CTL_PHY	VR_CTL	PCHCORE_REG_BOOT	69
VR_CTL_PHY	VR_CTL	PCHCORE_REG_BOOT_R	69
VR_CTL_PHY	VR_CTL	VTT_REG_BOOT	
VR_CTL_PHY	VR_CTL	VTT_REG_COMP	89
VR_CTL_PHY	VR_CTL	VTT_REG_FB	
VR_CTL_PHY	VR_CTL	VTT_REG_FS	
VR_CTL_PHY	VR_CTL	VTT_REG_COMP	89
VR_CTL_PHY	VR_CTL	VTT_REG_REF	89
VR_CTL_PHY	SWITCHNODE	VTT_REG_LGATE	
VR_CTL_PHY	VR_CTL	VTT_REG_OCSET	
VR_CTL_PHY	VR_CTL	VTT_OFS	
VR_CTL_PHY	VR_CTL	VTT_REG_REF	89
VR_CTL_PHY	VR_CTL	VTT_REG_UGATE	
VR_CTL_PHY	VR_CTL	VTT_REG_PH1_SNUB	
VR_CTL_PHY	VR_CTL	P3V42G3H_BOOST	72
VR_CTL_PHY	VR_CTL	P3V42G3H_FB	72

VR CTRL NET PROPERTIES

NET_TYPE			
PHYSICAL	SPACING		
VR_CTL_PHY	VR_CTL	DDR_REG_CS	71
VR_CTL_PHY	VR_CTL	DDR_REG_FB	71
VR_CTL_PHY	SWITCHNODE	DDR_REG_LGATE	71
VR_CTL_PHY	SWITCHNODE	DDR_REG_UGATE	71
VR_CTL_PHY	VR_CTL	DDR_REG_BOOT	71
VR_CTL_PHY	VR_CTL	DDR_REG_BOOT_R	71
VR_CTL_PHY	VR_CTL	DDR_REG_VDDQSNS	71
VR_CTL_PHY	VR_CTL	DDR_REG_VTTSNS	71
VR_CTL_PHY	VR_CTL	P1V8_REG_POR	71
VR_CTL_PHY	VR_CTL	P3V3S5_REG_BOOT	70
VR_CTL_PHY	VR_CTL	P3V3S5_REG_BOOT_R	70
VR_CTL_PHY	VR_CTL	P3V3S5_REG_FB	70
VR_CTL_PHY	VR_CTL	P3V3S5_REG_ISEN	70
VR_CTL_PHY	SWITCHNODE	P3V3S5_REG_LGATE	70
VR_CTL_PHY	VR_CTL	P3V3S5_REG_OCSET	70
VR_CTL_PHY	SWITCHNODE	P3V3S5_REG_UGATE	70
VR_CTL_PHY	VR_CTL	P3V3S5_REG_SNUB	70
VR_CTL_PHY	VR_CTL	P5VS3_REG_BOOT	70
VR_CTL_PHY	VR_CTL	P5VS3_REG_FB	70
VR_CTL_PHY	VR_CTL	P5VS3_REG_ISEN	70
VR_CTL_PHY	SWITCHNODE	P5VS3_REG_LGATE	70
VR_CTL_PHY	VR_CTL	P5VS3_REG_OCSET	70
VR_CTL_PHY	SWITCHNODE	P5VS3_REG_UGATE	70

VR VID NET PROPERTIES

NET_TYPE		
PHYSICAL	SPACING	
VID_PHY	VR_CTL	CPU_VID<0>
VID_PHY	VR_CTL	CPU_VID<1>
VID_PHY	VR_CTL	CPU_VID<2>
VID_PHY	VR_CTL	CPU_VID<3>
VID_PHY	VR_CTL	CPU_VID<4>
VID_PHY	VR_CTL	CPU_VID<5>
VID_PHY	VR_CTL	CPU_VID<6>
VID_PHY	VR_CTL	CPU_VID<7>
VID_PHY	VR_CTL	CPU_PSI_L

PULL-UP STUB < 1-INCH
VID LENGTH SKEW < 1-INCH
VID LENGTH RANGE< 1 TO 15-INCH

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
VID_PHY	*	39_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL	*	0.2MM	?

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

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POWER CONSTRAINTS

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PM NET PROPERTIES
(PM, RESET, EN, PGOOD)

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PM	*	*	2:1_SPACING
PM_VTT	PM_VTT	*	2:1_SPACING
PM_VTT	*	*	3:1_SPACING
PM_VTT	GND	*	DEFAULT
PM	GND	*	DEFAULT

	NET_TYPE PHYSICAL	NET_TYPE SPACING		
T2	PM	PLT_RESET_L	19 27	
T4	PM_VTT	PLT_RESET_LS1V1_L	10	
T5	PM	PM_ACDC_PS_ON	5	
T6	PM	PM_BATLOW_L	14 18 46	
T7	PM	PM_CLK32K_SUSCLK	8 46 85	
T8	PM	PM_CLK32K_SUSCLK_R	8 18 85	
T9	PM	PM_CLKRUN_L	14 18 46 48	
T10	PM	PM_EXT_TS_L<0>		
T11	PM	PM_EXT_TS_L<1>		
T12	PM	PM_LAN_PWRGD	14 18	
T13	PM_VTT	FSB_CPURSTOUT_L	10 24	
T25	PM_VTT	PM_MEM_PWRGD	10 18	
T24	PM	PM_ME_PWRGD	18 64	
T38	PM	PM_MXM_PGOOD	64 75	
T20	PM	PM_PCH_PWRGD	18 64	
T31	PM	PM_PGOOD_DDRREG_S3	63 71	
T33	PM	PM_PGOOD_PVCORE_CPU	25 64 65	
T32	PM	PM_PWRBTN_L	18 24 46	
T35	PM	PM_RSMRST_L	46 63	
T34	PM	PM_RSMRST_PCH_L	18 63	
T36	PM	PM_SLP_M_L	18 63	
T37	PM	PM_SLP_S3_L	5 18 26 36 46 47 63 64 81	
T120	PM	PM_SLP_S4_1_L	18 63	
T39	PM	PM_SLP_S4_L	18 47	
T43	PM	PM_SLP_S5_L	18 47	
T45	PM	PM_SUS_PWR_ACK	18	
T22	PM_VTT	PM_SYNC	10 18	
T192	PM	SDCARD_PLT_RST_L	27 44	
T46	PM	PM_SYSRST_L	18 27 46	
T44	PM	PM_SYS_PWRGD	18 64	
T40	PM_VTT	PM_THRMTRIP_L	10 20 47	
T48	PM	RSMRST_PWRGD	46 64	
T47	PM	RTC_RESET_L	17 91	
T50	PM_VTT	CPU_PWRGD	10 20 24	
T49	PM	CPU_RESET_L	10 27	
T55	PM	PGOOD_1V8_S0_G1	64	
T54	PM	PGOOD_1V8_S0_G2	64	
T56	PM	PGOOD_CPU_GFX_DDR	64	
T57	PM	PGOOD_P1V5_S0	10 73	
T58	PM	PGOOD_P1V8_S0	64	
T60	PM	PGOOD_P3V3_S0	64 73	
T63	PM	PGOOD_P3V3_S3	34 73	
T62	PM	PGOOD_P5V_S0	63 73	
T64	PM	PGOOD_PCH_AND_P1V8	64	
T66	PM	PGOOD_PCH_S0	64	
T65	PM	PGOOD_SYSPWROK	64	
T67	PM	PGOOD_SYSPWROK_R	64	
T68	PM	RTC_RESET_L	17 91	
T69	PM	P12V_S3_EN		
T70	PM	P1V5_S0_EN	63 73	
T74	PM	P3V3S0_EN	63 73	
T75	PM	P3V3S3_EN	63 73	
T76	PM	P5VS0_EN	63 73	
T78	PM	P5VS3_EN	63 70	
T77	PM	PCHCORE_REG_EN	63 69	
T79	PM	PCHCORE_REG_PGOOD	63 64 69	
T73	PM	PEG_RESET_L	8 27	
T80	PM	SDCARD_RESET	20 44 92	

	NET_TYPE PHYSICAL	NET_TYPE SPACING		
T82	PM	4V5_REG_EN	56	
T81	PM	ALL_SYS_PWRGD_R	5 64	
T84	PM	ALL_SYS_PWRGD_SMC	46 64	
T83	PM	CK505_27MHZ_EN	25	
T85	PM	CPUVTT_REG_EN	63 68	
T86	PM_VTT	CPUVTT_REG_PGOOD	10 63 64 68	
T87	PM	CPU_MEM_RESET_L	10 26	
T88	PM	DDRVTT_EN	63 71	
T89	PM	DEBUG_RESET_L	27 48	
T90	PM	FWPHY_RESET_L	39	
T91	PM	FWXIO_SNOOP_EN	39	
T92	PM	FW_RESET_L	27 39	
T95	PM	ENET_RESET_L	27 37	
T97	PM	MEM_RESET_L	26 30 31	
T98	PM	MINI_RESET_L	27 33	
T93	PM	SMC_DELAYED_PWRGD	47 64	
T100	PM	SMC_LRESET_L	27 46	
T99	PM	SMC_RESET_L	46 47 48	
T102	PM_VTT	XDP_CPUPWRGD	10 24	
T101	PM_VTT	XDP_DBRESET_L	10 24 27	
T103	PM_VTT	XDP_PWRGD	24	

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PM RESETS ENABLES PGOOD CONST

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FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT

J4700 USB CAMERA

89 5	IN	PP5V_S3	FUNC_TEST=TRUE MIN_ALLOWED_TPS=1
85 44	IN	USB_CAMERA_L_P	FUNC_TEST=TRUE
85 44	IN	USB_CAMERA_L_N	FUNC_TEST=TRUE
85 44	IN	USB_BT_L_P	FUNC_TEST=TRUE
85 44	IN	USB_BT_L_N	FUNC_TEST=TRUE
49 44	IN	=SMB_ALS_SCL	FUNC_TEST=TRUE
49 44	IN	=SMB_ALS_SDA	FUNC_TEST=TRUE

1 PP5V_S3_REG Testpoint near J4700
1 PP3V3_S3 TESTPOINT NEAR J4700
6 GROUND TESTPOINTS NEAR J4700

J4750 USB CARD READER

85 44	IN	USB_SDCARD_L_P	FUNC_TEST=TRUE
85 44	IN	USB_SDCARD_L_N	FUNC_TEST=TRUE
91 44 20	IN	SDCARD_RESET	FUNC_TEST=TRUE

1 PP3V3_S3 Testpoint near J4750
2 Ground Testpoints near J4750

J4780 IR BOARD

85 44	IN	USB_IR_L_P	FUNC_TEST=TRUE
85 44	IN	USB_IR_L_N	FUNC_TEST=TRUE
89 44	IN	PP5V_S3_IR_FLT	FUNC_TEST=TRUE

1 GROUND TESTPOINT NEAR J4780

J4520 SATA ODD (HIGH SPEED)

46 42	IN	SMC_ODD_DETECT	FUNC_TEST=TRUE

1 PP5V_S0 Testpoint near J4520
1 GROUND TESTPOINTS NEAR J4520

J5551 ODD TEMP SENSOR

88 52	IN	SNS_ODD_P	FUNC_TEST=TRUE
88 52	IN	SNS_ODD_N	FUNC_TEST=TRUE

J5600 ODD FAN

53	IN	FAN_0_PWR_L	FUNC_TEST=TRUE
53	IN	FAN_TACH0_L	FUNC_TEST=TRUE
89 53	IN	PP12V_S0_FAN0_L	FUNC_TEST=TRUE
53	IN	FAN_0_GND	FUNC_TEST=TRUE

J5700 CPU FAN

54	IN	FAN_2_PWR_L	FUNC_TEST=TRUE
54	IN	FAN_TACH2_L	FUNC_TEST=TRUE
89 54	IN	PP12V_S0_FAN2_L	FUNC_TEST=TRUE
54	IN	FAN_2_GND	FUNC_TEST=TRUE
88 54 52	IN	SNS_AMB_P	FUNC_TEST=TRUE
88 54 52	IN	SNS_AMB_N	FUNC_TEST=TRUE

1 GROUND TESTPOINT NEAR J5700

J5601 HD FAN

53	IN	FAN_1_PWR_L	FUNC_TEST=TRUE
53	IN	FAN_TACH1_L	FUNC_TEST=TRUE
89 53	IN	PP12V_S0_FAN1_L	FUNC_TEST=TRUE
53	IN	FAN_1_GND	FUNC_TEST=TRUE

J5400 HDD TEMP SENSOR

88 51	IN	HDD_OOB_TEMP_FILT	FUNC_TEST=TRUE

1 GROUND TESTPOINTS NEAR J5400

J5560 SKIN TEMP SENSOR

88 52	IN	SNS_SKIN_P	FUNC_TEST=TRUE
88 52	IN	SNS_SKIN_N	FUNC_TEST=TRUE

J6601 AUDIO MICROPHONE

60	IN	AUD_MIC_IN1_N_CONN	FUNC_TEST=TRUE
60	IN	GND_AUDIO_MIC1_CONN	FUNC_TEST=TRUE
60	IN	AUD_MIC_IN1_P_CONN	FUNC_TEST=TRUE

1 Ground Testpoint near J6601

J6602 AUDIO RIGHT SPEAKER

85 60 58	IN	AUD_SPKR_OUTLO2R_POUT	FUNC_TEST=TRUE
85 60 58	IN	AUD_SPKR_OUTLO2R_NOUT	FUNC_TEST=TRUE
85 60 58	IN	AUD_SPKR_OUTLO1R_POUT	FUNC_TEST=TRUE
85 60 58	IN	AUD_SPKR_OUTLO1R_NOUT	FUNC_TEST=TRUE

J6603 AUDIO LEFT SPEAKER

85 60 59	IN	AUD_SPKR_OUTLO2L_POUT	FUNC_TEST=TRUE
85 60 59	IN	AUD_SPKR_OUTLO2L_NOUT	FUNC_TEST=TRUE
85 60 59	IN	AUD_SPKR_OUTLO1L_POUT	FUNC_TEST=TRUE
85 60 59	IN	AUD_SPKR_OUTLO1L_NOUT	FUNC_TEST=TRUE

J6600 AUDIO AUXILIARY CONNECTOR

89 60	IN	PP3V3_AUDIO_SPDIF_JACK	2 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=2
60	IN	AUD_LI_DET_JACK	FUNC_TEST=TRUE
60	IN	AUD_LI_R_JACK	FUNC_TEST=TRUE
60	IN	AUD_LI_GND_JACK	FUNC_TEST=TRUE
60	IN	AUD_LI_L_JACK	FUNC_TEST=TRUE
60	IN	HS_MIC_LO_JACK	FUNC_TEST=TRUE
60	IN	HS_MIC_HI_JACK	FUNC_TEST=TRUE
60	IN	AUD_HP_L_JACK	FUNC_TEST=TRUE
60	IN	AUD_HP_GND_JACK	FUNC_TEST=TRUE
60	IN	AUD_HP_R_JACK	FUNC_TEST=TRUE
60	IN	AUD_HP_TYPEDET_JACK	FUNC_TEST=TRUE
60	IN	AUD_IP_PERPH_JACK	FUNC_TEST=TRUE
60	IN	AUD_HP_TIPDET_JACK	FUNC_TEST=TRUE
60	IN	AUD_SPDIFIN_JACK	FUNC_TEST=TRUE
60	IN	AUD_SPDIF_OUT_JACK	FUNC_TEST=TRUE

4 GROUND TESTPOINTS NEAR J6600

		GND	17 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=17
89 5	IN	PP3V3_S3	2 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=2
70 5	IN	PP5V_S3_REG	1 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=1
89 5	IN	PP5V_S0	FUNC_TEST=TRUE MIN_ALLOWED_TPS=1

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