1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
B	0000803841	PRODUCTION RELEASED	2009-10-09

SCHEMATIC,MLB,"Kalahari"

LAST_MODIFIED=Fri Oct 9 15:23:09 2009

DRAWING
TITLE=K22
ABBREV=DRAWING
LAST_MODIFIED=Fri Oct 9 15:23:09 2009

DRAWING TITLE

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DRAWING NUMBER 051-8233 SIZE D
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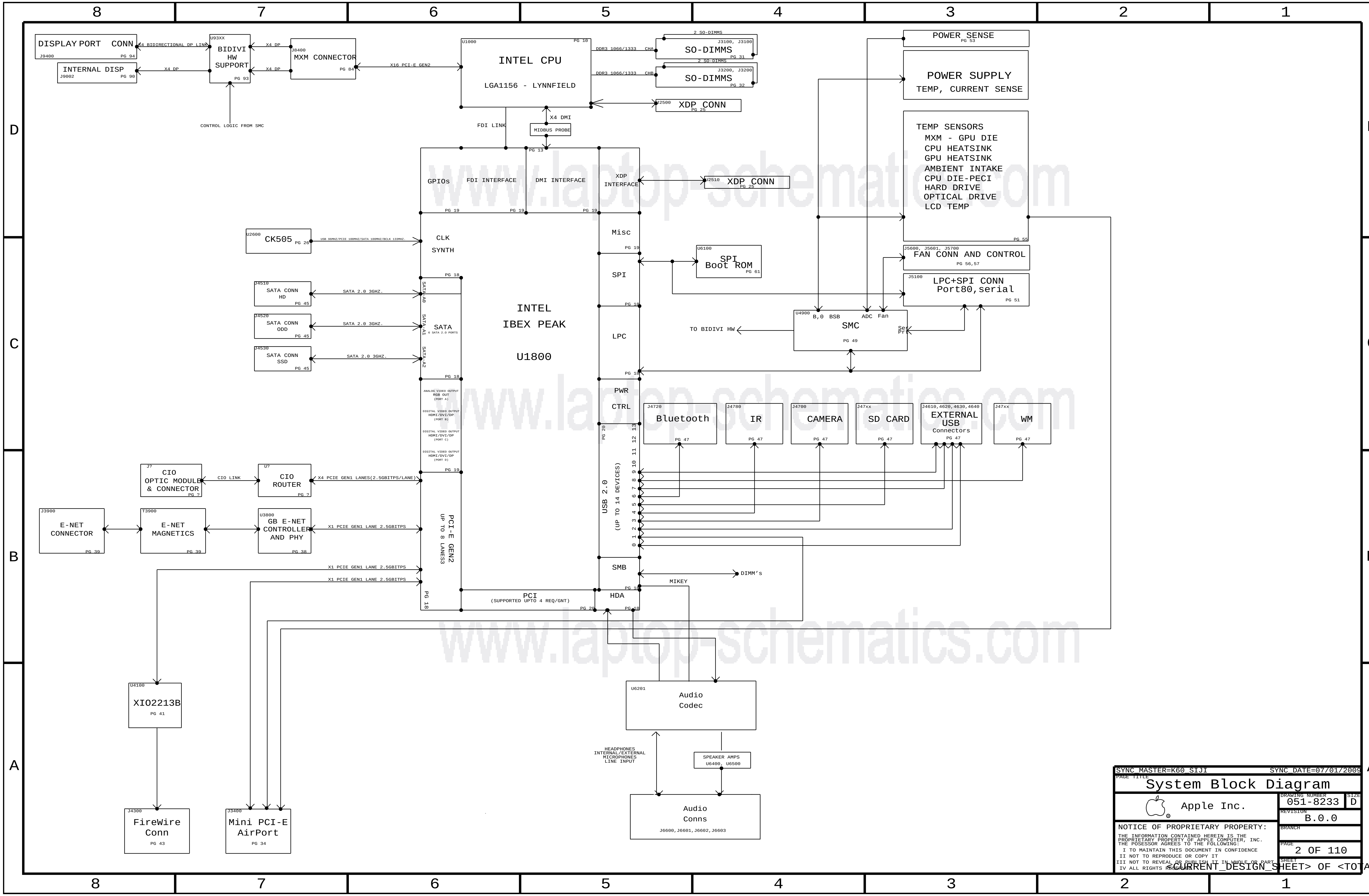

SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE
System Block Diagram

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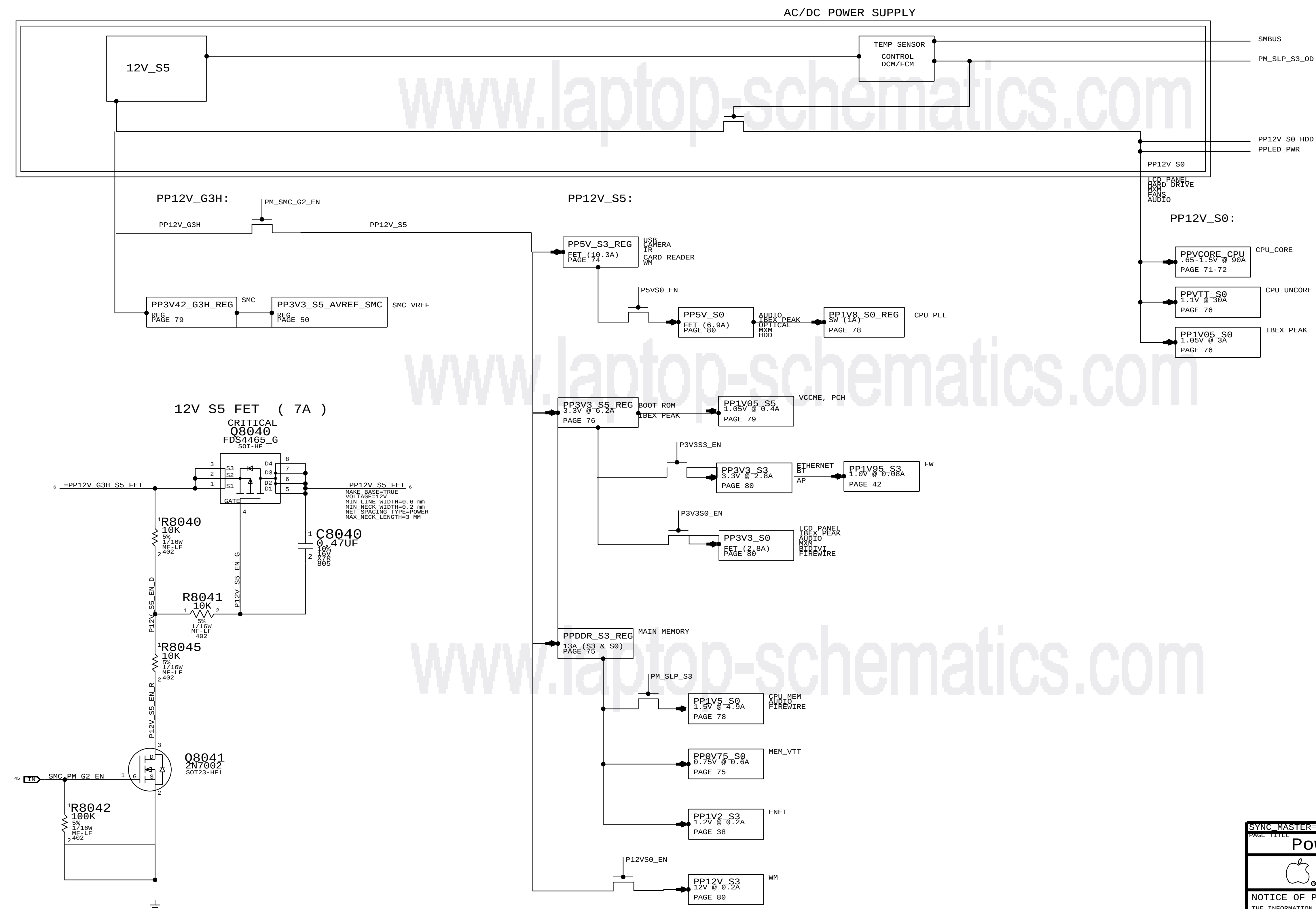

SYNC_MASTER=K60_MIKE SYNC_DATE=07/01/2009

PAGE TITLE

Power Block Diagram

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PAGE 3 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0439	PCBA,MLB,K23F,2.66GHZ	K23F,2P66GHZ_CPU,BASIC,CPUPOC_IMAX_100_120
639-0440	PCBA,MLB,K23F,2.80GHZ	K23F,2P80GHZ_CPU,BASIC,CPUPOC_IMAX_100_120
085-1023	PCBA,MLB,DEV,K23F	DEVELOPMENT,DEV_GROUP

BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE,XDP,BETTER,MXM,XDP_CPU_BPM,INT_VREF,PCH_VRM,BUF_CLK,PRODUCTION
DEV_GROUP	XDP_CONN,LPCPLUS,MOJOMUX,CPU_TDIODE,MEM_RESET_HW

COMMON

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	337S3823	1	IC,IBEX PEAK B3,DESKTOP,FCBGA,PCH,P425	U1800	CRITICAL	
	359S0157	1	IC,SLG2AP108,CLK GEN,CK505,QFN3	U2600	CRITICAL	BUF_CLK
	341T0211	1	IC,EFI BOOTROM,K23F	U6100	CRITICAL	
	338S0765	1	IC,XIO2211ZAY,1394B_PCIE,PHY/LINK	U4100	CRITICAL	
	343S0485	1	IC,BCM5764M,68PIN QFN	U3700	CRITICAL	
RAW: 335S0663	341T0213	1	IC,FLASH,45DB0011D,SOIC-8S1	U3701	CRITICAL	
	511S0063	1	SOCKET,LGA1156,CPU-LF	U1000	CRITICAL	
	825-7122	1	MLB LABEL,48.0X4.8	X14	CRITICAL	

CPUS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3810	1	LFD,SLBLC,PRQ,2.66,95W,1333,B1,8M,LGA	CPU	CRITICAL	2P66GHZ_CPU
337S3811	1	LFD,SLBJJ,PRQ,2.80,95W,1333,B1,8M,LGA	CPU	CRITICAL	2P80GHZ_CPU

BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL
4	POWER
5	POWER
6	SIGNAL
7	GROUND
BOTTOM	SIGNAL

K23F PARTS

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	051-8233	1	SCH,K23F,MLB	SCH1		K23F
	820-2733	1	PCBF,K23F,MLB	MLB1		K23F
(338S0489 - BLNK)	341T0212	1	IC,SMC,K23F	U4900	CRITICAL	K23F

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PAGE TITLE
BOM Configuration

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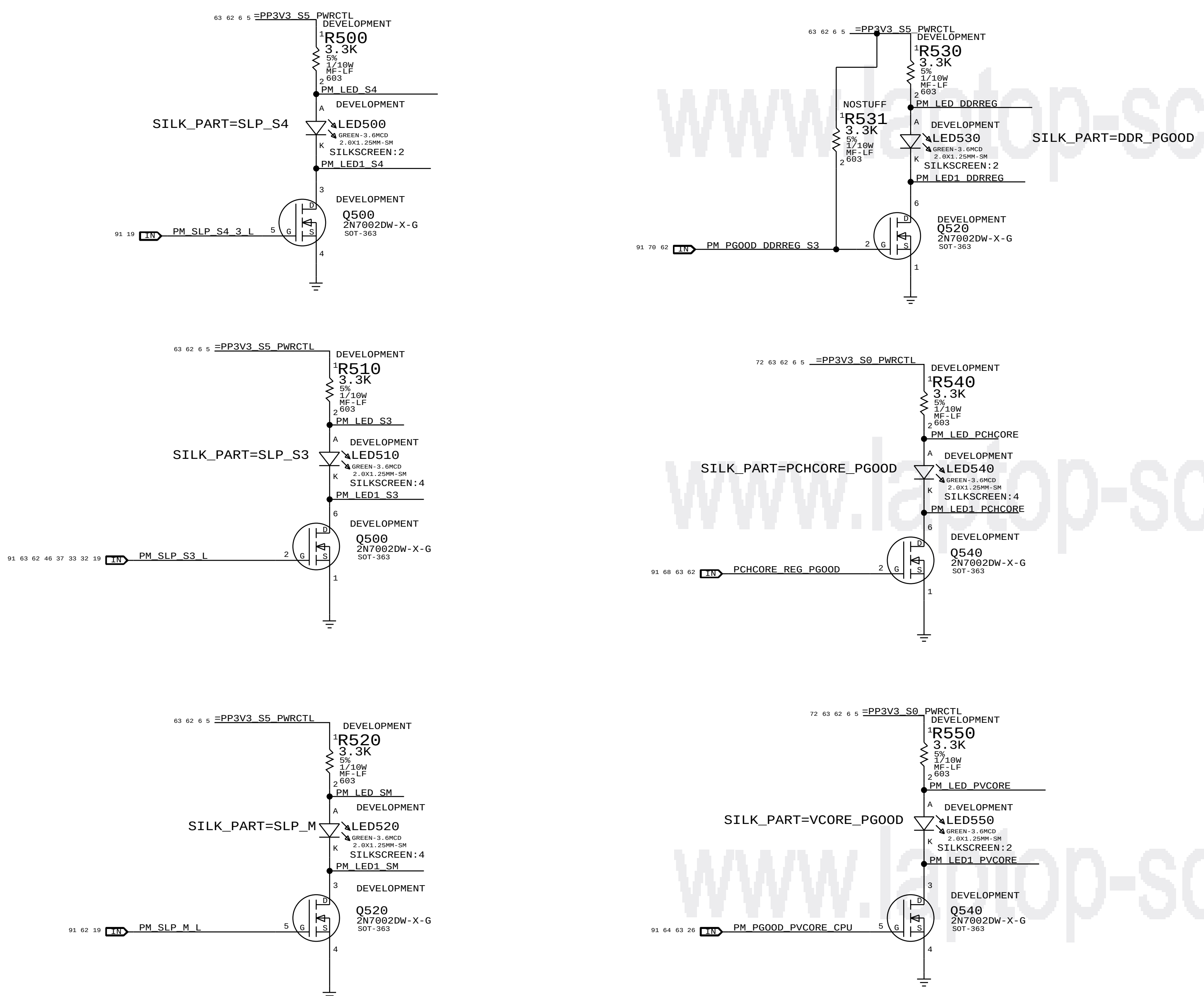

State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

SYNC_MASTER=K60_MIKE SYNC_DATE=07/01/2009

PAGE TITLE
PROTO 0 DEBUG LEDS

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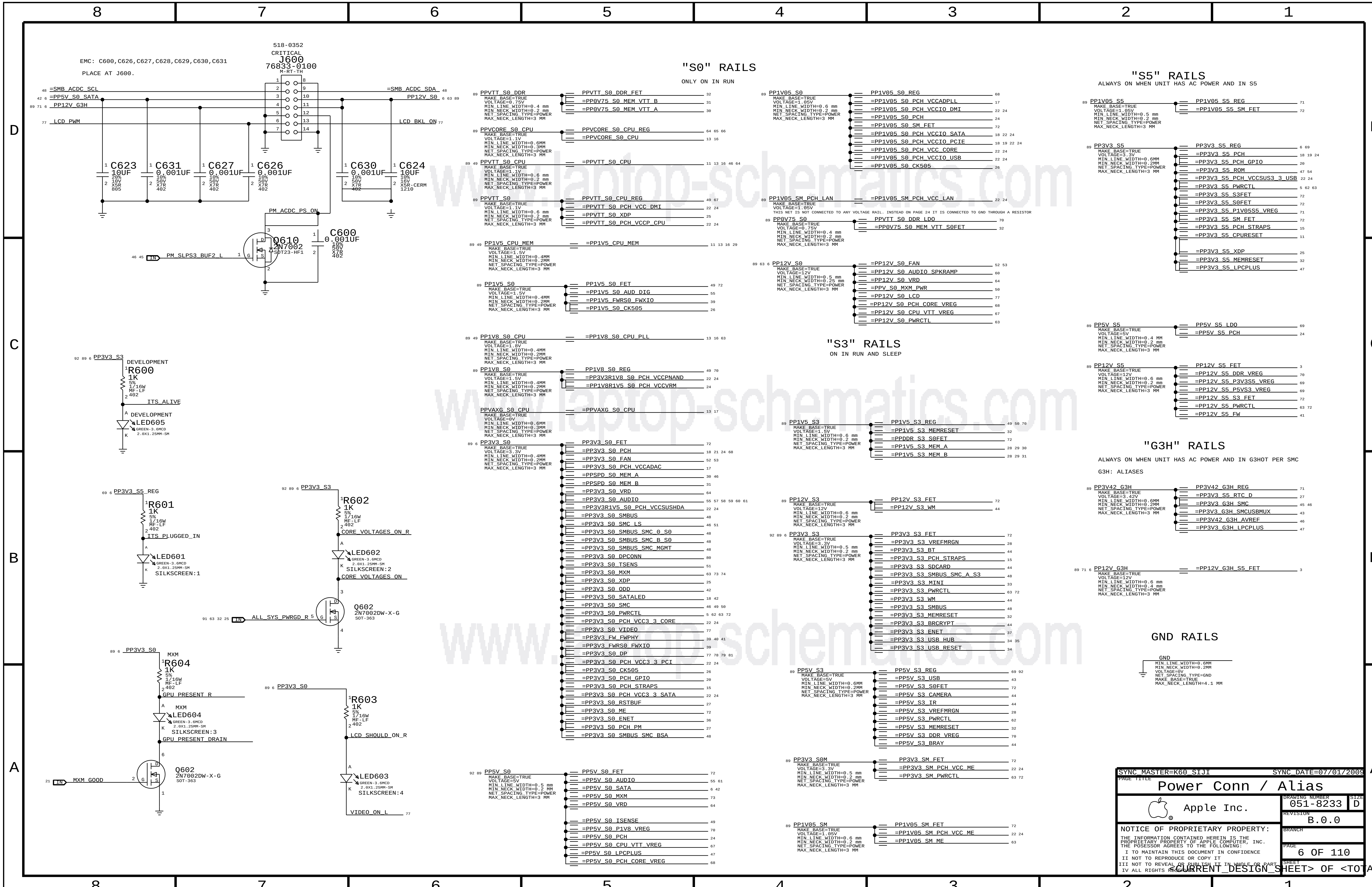

SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE: Power Conn / Alias

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DRAWING NUMBER: 051-8233 SIZE: D

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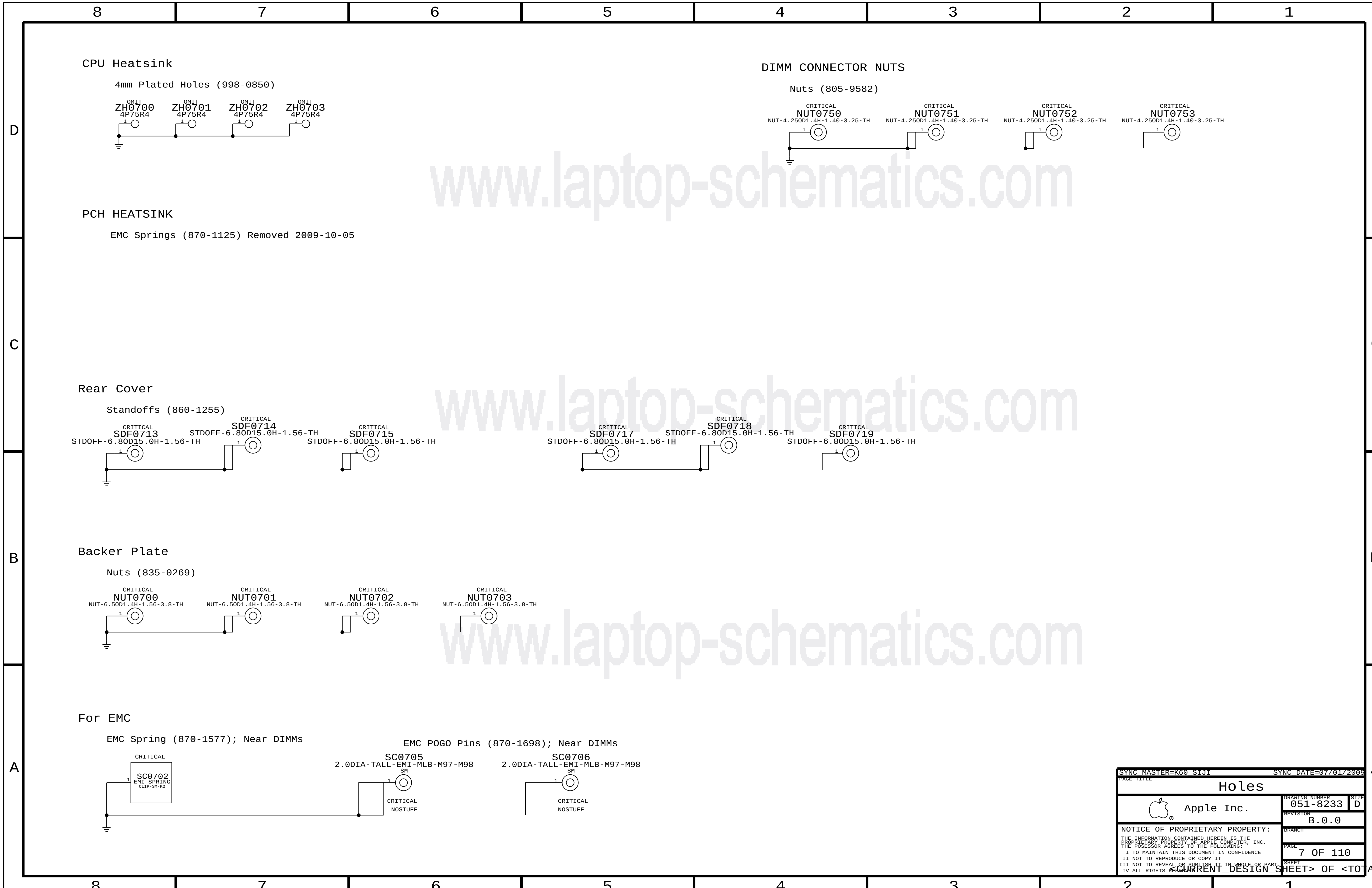
CPU Heatsink
4mm Plated Holes (998-0850)
OMIT ZH0700 4P75R4
OMIT ZH0701 4P75R4
OMIT ZH0702 4P75R4
OMIT ZH0703 4P75R4
DIMM CONNECTOR NUTS
Nuts (805-9582)
CRITICAL NUT0750 NUT-4.25OD1.4H-1.40-3.25-TH
CRITICAL NUT0751 NUT-4.25OD1.4H-1.40-3.25-TH
CRITICAL NUT0752 NUT-4.25OD1.4H-1.40-3.25-TH
CRITICAL NUT0753 NUT-4.25OD1.4H-1.40-3.25-TH
PCH HEATSINK
EMC Springs (870-1125) Removed 2009-10-05
Rear Cover
Standoffs (860-1255)
CRITICAL SDF0713 STDOFF-6.8OD15.0H-1.56-TH
CRITICAL SDF0714 STDOFF-6.8OD15.0H-1.56-TH
CRITICAL SDF0715 STDOFF-6.8OD15.0H-1.56-TH
CRITICAL SDF0717 STDOFF-6.8OD15.0H-1.56-TH
CRITICAL SDF0718 STDOFF-6.8OD15.0H-1.56-TH
CRITICAL SDF0719 STDOFF-6.8OD15.0H-1.56-TH
Backer Plate
Nuts (835-0269)
CRITICAL NUT0700 NUT-6.5OD1.4H-1.56-3.8-TH
CRITICAL NUT0701 NUT-6.5OD1.4H-1.56-3.8-TH
CRITICAL NUT0702 NUT-6.5OD1.4H-1.56-3.8-TH
CRITICAL NUT0703 NUT-6.5OD1.4H-1.56-3.8-TH
For EMC
EMC Spring (870-1577); Near DIMMs
CRITICAL SC0702 EMI-SPRING CLIP-SM-K2
EMC POGO Pins (870-1698); Near DIMMs
SC0705 2.0DIA-TALL-EMI-MLB-M97-M98 SM CRITICAL NOSTUFF
SC0706 2.0DIA-TALL-EMI-MLB-M97-M98 SM CRITICAL NOSTUFF
SYNC_MASTER=K60_SIJI
SYNC_DATE=07/01/2009
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Holes
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UNUSED CPU SIGNALS

- TP_CPU_RSVD<41..29> = NC_CPU_RSVD<41..29> MAKE_BASE=TRUE NO_TEST=TRUE
- TP_CPU_RSVD<26..1> = NC_CPU_RSVD<26..1> MAKE_BASE=TRUE NO_TEST=TRUE
- TP_CPU_FC_AE38 = NC_CPU_FC_AE38 MAKE_BASE=TRUE NO_TEST=TRUE
- TP_CPU_FC_AG40 = NC_CPU_FC_AG40 MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED PCI ALIASES

- TP_PCI_AD<31..0> = NC_PCI_AD<31..0> MAKE_BASE=TRUE NO_TEST=TRUE
- TP_PCI_C_BE_L<3..0> = NC_PCI_C_BE_L<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
- TP_PCI_PAR = NC_PCI_PAR MAKE_BASE=TRUE NO_TEST=TRUE
- TP_PCI_RESET_L = NC_PCI_RESET_L MAKE_BASE=TRUE NO_TEST=TRUE
- TP_PCIE_CLK100M_XDPP = NC_PCIE_CLK100M_XDPP MAKE_BASE=TRUE NO_TEST=TRUE
- TP_PCIE_CLK100M_XDPN = NC_PCIE_CLK100M_XDPN MAKE_BASE=TRUE NO_TEST=TRUE
- TP_DMI_CLK100M_LAP = NC_DMI_CLK100M_LAP MAKE_BASE=TRUE NO_TEST=TRUE
- TP_DMI_CLK100M_LAN = NC_DMI_CLK100M_LAN MAKE_BASE=TRUE NO_TEST=TRUE
- TP_LPC_DREQ1_L = NC_LPC_DREQ1_L MAKE_BASE=TRUE NO_TEST=TRUE
- TP_LPC_DREQ0_L = NC_LPC_DREQ0_L MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED NAND ALIASES

- TP_NV_CE_L<3..0> = NC_NV_CE_L<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
- TP_NV_DQS<1..0> = NC_NV_DQS<1..0> MAKE_BASE=TRUE NO_TEST=TRUE
- TP_NV_DQ<15..0> = NC_NV_DQ<15..0> MAKE_BASE=TRUE NO_TEST=TRUE
- TP_NV_RB_L = NC_NV_RB_L MAKE_BASE=TRUE NO_TEST=TRUE
- TP_NV_WR_RE_L<1..0> = NC_NV_WR_RE_L<1..0> MAKE_BASE=TRUE NO_TEST=TRUE
- TP_NV_WE_CK_L<1..0> = NC_NV_WE_CK_L<1..0> MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED MISC ALIASES

- TP_JTAG_XDP_TRST_L = NC_JTAG_XDP_TRST_L MAKE_BASE=TRUE NO_TEST=TRUE
- TP_PCH_PWM0 = NC_PCH_PWM0 MAKE_BASE=TRUE NO_TEST=TRUE
- TP_PCH_PWM1 = NC_PCH_PWM1 MAKE_BASE=TRUE NO_TEST=TRUE
- TP_PCH_PWM2 = NC_PCH_PWM2 MAKE_BASE=TRUE NO_TEST=TRUE
- TP_PCH_PWM3 = NC_PCH_PWM3 MAKE_BASE=TRUE NO_TEST=TRUE
- TP_PCH_SST = NC_PCH_SST MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED MEM ALIASES

- TP_MEM_A_CS_L<7..4> = NC_MEM_A_CS_L<7..4> MAKE_BASE=TRUE NO_TEST=TRUE
- TP_MEM_A_DQ_CB<7..0> = NC_MEM_A_DQ_CB<7..0> MAKE_BASE=TRUE NO_TEST=TRUE
- TP_MEM_A_DQS_N<8> = NC_MEM_A_DQS_N<8> MAKE_BASE=TRUE NO_TEST=TRUE
- TP_MEM_A_DQS_P<8> = NC_MEM_A_DQS_P<8> MAKE_BASE=TRUE NO_TEST=TRUE
- TP_MEM_B_CS_L<7..4> = NC_MEM_B_CS_L<7..4> MAKE_BASE=TRUE NO_TEST=TRUE
- TP_MEM_B_DQ_CB<7..0> = NC_MEM_B_DQ_CB<7..0> MAKE_BASE=TRUE NO_TEST=TRUE
- TP_MEM_B_DQS_N<8> = NC_MEM_B_DQS_N<8> MAKE_BASE=TRUE NO_TEST=TRUE
- TP_MEM_B_DQS_P<8> = NC_MEM_B_DQS_P<8> MAKE_BASE=TRUE NO_TEST=TRUE

- TP_PCI_T28_D2R_N<3..0> = NC_PCI_T28_D2R_N<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
- TP_PCI_T28_D2R_P<3..0> = NC_PCI_T28_D2R_P<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
- TP_PCI_T28_R2D_C_N<3..0> = NC_PCI_T28_R2D_C_N<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
- TP_PCI_T28_R2D_C_P<3..0> = NC_PCI_T28_R2D_C_P<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
- TP_HDA_SDIN1 = NC_HDA_SDIN1 MAKE_BASE=TRUE NO_TEST=TRUE
- TP_HDA_SDIN2 = NC_HDA_SDIN2 MAKE_BASE=TRUE NO_TEST=TRUE
- TP_HDA_SDIN3 = NC_HDA_SDIN3 MAKE_BASE=TRUE NO_TEST=TRUE
- TP_PCIE_CLK100M_PE5P = NC_PCIE_CLK100M_PE5P MAKE_BASE=TRUE NO_TEST=TRUE
- TP_PCIE_CLK100M_PE5N = NC_PCIE_CLK100M_PE5N MAKE_BASE=TRUE NO_TEST=TRUE
- TP_NV_RCOMP = NC_NV_RCOMP MAKE_BASE=TRUE NO_TEST=TRUE
- PCIE_CLK100M_EXCARD_P = NC_PCIE_CLK100M_EXCARD_P MAKE_BASE=TRUE NO_TEST=TRUE
- PCIE_CLK100M_EXCARD_N = NC_PCIE_CLK100M_EXCARD_N MAKE_BASE=TRUE NO_TEST=TRUE
- TP_USB_7N = NC_USB_7N MAKE_BASE=TRUE NO_TEST=TRUE
- TP_USB_7P = NC_USB_7P MAKE_BASE=TRUE NO_TEST=TRUE
- TP_USB_6N = NC_USB_6N MAKE_BASE=TRUE NO_TEST=TRUE
- TP_USB_6P = NC_USB_6P MAKE_BASE=TRUE NO_TEST=TRUE
- TP_USB_1N = NC_USB_1N MAKE_BASE=TRUE NO_TEST=TRUE
- TP_USB_1P = NC_USB_1P MAKE_BASE=TRUE NO_TEST=TRUE
- TP_USB_3N = NC_USB_3N MAKE_BASE=TRUE NO_TEST=TRUE
- TP_USB_3P = NC_USB_3P MAKE_BASE=TRUE NO_TEST=TRUE
- TP_USB_5N = NC_USB_5N MAKE_BASE=TRUE NO_TEST=TRUE
- TP_USB_5P = NC_USB_5P MAKE_BASE=TRUE NO_TEST=TRUE
- TP_USB_9N = NC_USB_9N MAKE_BASE=TRUE NO_TEST=TRUE
- TP_USB_9P = NC_USB_9P MAKE_BASE=TRUE NO_TEST=TRUE
- TP_USB_10N = NC_USB_10N MAKE_BASE=TRUE NO_TEST=TRUE
- TP_USB_10P = NC_USB_10P MAKE_BASE=TRUE NO_TEST=TRUE
- TP_USB_11N = NC_USB_11N MAKE_BASE=TRUE NO_TEST=TRUE
- TP_USB_11P = NC_USB_11P MAKE_BASE=TRUE NO_TEST=TRUE
- TP_USB_12N = NC_USB_12N MAKE_BASE=TRUE NO_TEST=TRUE
- TP_USB_12P = NC_USB_12P MAKE_BASE=TRUE NO_TEST=TRUE
- TP_USB_13N = NC_USB_13N MAKE_BASE=TRUE NO_TEST=TRUE
- TP_USB_13P = NC_USB_13P MAKE_BASE=TRUE NO_TEST=TRUE
- PCIE_EXCARD_D2R_P = NC_PCIE_EXCARD_D2R_P MAKE_BASE=TRUE NO_TEST=TRUE
- PCIE_EXCARD_D2R_N = NC_PCIE_EXCARD_D2R_N MAKE_BASE=TRUE NO_TEST=TRUE
- PCIE_EXCARD_R2D_C_P = NC_PCIE_EXCARD_R2D_C_P MAKE_BASE=TRUE NO_TEST=TRUE
- PCIE_EXCARD_R2D_C_N = NC_PCIE_EXCARD_R2D_C_N MAKE_BASE=TRUE NO_TEST=TRUE
- TP_SDVO_TVCLKINN = NC_SDVO_TVCLKINN MAKE_BASE=TRUE NO_TEST=TRUE
- TP_SDVO_TVCLKINP = NC_SDVO_TVCLKINP MAKE_BASE=TRUE NO_TEST=TRUE
- TP_SDVO_STALLN = NC_SDVO_STALLN MAKE_BASE=TRUE NO_TEST=TRUE
- TP_SDVO_STALLP = NC_SDVO_STALLP MAKE_BASE=TRUE NO_TEST=TRUE
- TP_SDVO_INTN = NC_SDVO_INTN MAKE_BASE=TRUE NO_TEST=TRUE
- TP_SDVO_INTP = NC_SDVO_INTP MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED SATA ALIASES

- TP_SATA_D_D2RN = NC_SATA_D_D2RN MAKE_BASE=TRUE NO_TEST=TRUE
- TP_SATA_D_D2RP = NC_SATA_D_D2RP MAKE_BASE=TRUE NO_TEST=TRUE
- TP_SATA_D_R2D_CN = NC_SATA_D_R2D_CN MAKE_BASE=TRUE NO_TEST=TRUE
- TP_SATA_D_R2D_CP = NC_SATA_D_R2D_CP MAKE_BASE=TRUE NO_TEST=TRUE
- TP_SATA_E_D2RN = NC_SATA_E_D2RN MAKE_BASE=TRUE NO_TEST=TRUE
- TP_SATA_E_D2RP = NC_SATA_E_D2RP MAKE_BASE=TRUE NO_TEST=TRUE
- TP_SATA_E_R2D_CN = NC_SATA_E_R2D_CN MAKE_BASE=TRUE NO_TEST=TRUE
- TP_SATA_E_R2D_CP = NC_SATA_E_R2D_CP MAKE_BASE=TRUE NO_TEST=TRUE
- TP_SATA_F_D2RN = NC_SATA_F_D2RN MAKE_BASE=TRUE NO_TEST=TRUE
- TP_SATA_F_D2RP = NC_SATA_F_D2RP MAKE_BASE=TRUE NO_TEST=TRUE
- TP_SATA_F_R2D_CN = NC_SATA_F_R2D_CN MAKE_BASE=TRUE NO_TEST=TRUE
- TP_SATA_F_R2D_CP = NC_SATA_F_R2D_CP MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED DISPLAY ALIASES

- TP_CRT_IG_DDC_CLK = NC_CRT_IG_DDC_CLK MAKE_BASE=TRUE NO_TEST=TRUE
- TP_CRT_IG_DDC_DATA = NC_CRT_IG_DDC_DATA MAKE_BASE=TRUE NO_TEST=TRUE
- TP_CRT_IG_RED = NC_CRT_IG_RED MAKE_BASE=TRUE NO_TEST=TRUE
- TP_CRT_IG_GREEN = NC_CRT_IG_GREEN MAKE_BASE=TRUE NO_TEST=TRUE
- TP_CRT_IG_BLUE = NC_CRT_IG_BLUE MAKE_BASE=TRUE NO_TEST=TRUE
- TP_CRT_IG_HSYNC = NC_CRT_IG_HSYNC MAKE_BASE=TRUE NO_TEST=TRUE
- TP_CRT_IG_VSYNC = NC_CRT_IG_VSYNC MAKE_BASE=TRUE NO_TEST=TRUE
- TP_DP_IG_B_MLN<3..0> = NC_DP_IG_B_MLN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
- TP_DP_IG_B_MLP<3..0> = NC_DP_IG_B_MLP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
- TP_DP_IG_B_AUX_N = NC_DP_IG_B_AUXN MAKE_BASE=TRUE NO_TEST=TRUE
- TP_DP_IG_B_AUX_P = NC_DP_IG_B_AUXP MAKE_BASE=TRUE NO_TEST=TRUE
- TP_DP_IG_B_HPD = NC_DP_IG_B_HPD MAKE_BASE=TRUE NO_TEST=TRUE
- TP_DP_IG_B_DDC_CLK = NC_DP_IG_B_CTRL_CLK MAKE_BASE=TRUE NO_TEST=TRUE
- TP_DP_IG_B_DDC_DATA = NC_DP_IG_B_CTRL_DATA MAKE_BASE=TRUE NO_TEST=TRUE
- TP_DP_IG_C_MLN<3..0> = NC_DP_IG_C_MLN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
- TP_DP_IG_C_MLP<3..0> = NC_DP_IG_C_MLP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
- TP_DP_IG_C_AUX_N = NC_DP_IG_C_AUXN MAKE_BASE=TRUE NO_TEST=TRUE
- TP_DP_IG_C_AUX_P = NC_DP_IG_C_AUXP MAKE_BASE=TRUE NO_TEST=TRUE
- TP_DP_IG_C_HPD = NC_DP_IG_C_HPD MAKE_BASE=TRUE NO_TEST=TRUE
- TP_DP_IG_C_CTRL_CLK = NC_DP_IG_C_CTRL_CLK MAKE_BASE=TRUE NO_TEST=TRUE
- TP_DP_IG_C_CTRL_DATA = NC_DP_IG_C_CTRL_DATA MAKE_BASE=TRUE NO_TEST=TRUE
- TP_DP_IG_D_MLN<3..0> = NC_DP_IG_D_MLN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
- TP_DP_IG_D_MLP<3..0> = NC_DP_IG_D_MLP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
- TP_DP_IG_D_AUXN = NC_DP_IG_D_AUXN MAKE_BASE=TRUE NO_TEST=TRUE
- TP_DP_IG_D_AUXP = NC_DP_IG_D_AUXP MAKE_BASE=TRUE NO_TEST=TRUE
- TP_DP_IG_D_HPD = NC_DP_IG_D_HPD MAKE_BASE=TRUE NO_TEST=TRUE
- TP_DP_IG_D_CTRL_CLK = NC_DP_IG_D_CTRL_CLK MAKE_BASE=TRUE NO_TEST=TRUE
- TP_DP_IG_D_CTRL_DATA = NC_DP_IG_D_CTRL_DATA MAKE_BASE=TRUE NO_TEST=TRUE
- TP_GFX_VID<0..6> = NC_GFX_VID<0..6> MAKE_BASE=TRUE NO_TEST=TRUE
- TP_GFX_VSENSE_N = NC_GFX_VSENSE_N MAKE_BASE=TRUE NO_TEST=TRUE
- TP_GFX_VSENSE_P = NC_GFX_VSENSE_P MAKE_BASE=TRUE NO_TEST=TRUE

SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE: UNUSED SIGNAL ALIAS

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DRAWING NUMBER: 051-8233 SIZE: D

REVISION: B.0.0

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SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8 7 6 5 4 3 2 1

PEG Slot Support

THIS SIGNAL NAME IS CONNECTED TO MXM

18 IN PEG_CLK100M_P — 84 GPU_CLK100M_PCIE_P (MAKE_BASE=TRUE) — CLK_100M_MXM_P OUT 73

18 IN PEG_CLK100M_N — 84 GPU_CLK100M_PCIE_N (MAKE_BASE=TRUE) — CLK_100M_MXM_N OUT 73

10 IN =PEG_R2D_C_P<0..15> — PEG_R2D_C_P<0..15> (MAKE_BASE=TRUE) OUT 75 84

10 IN =PEG_R2D_C_N<0..15> — PEG_R2D_C_N<0..15> (MAKE_BASE=TRUE) OUT 75 84

10 OUT =PEG_D2R_P<0..15> — PEG_D2R_P<0..15> (MAKE_BASE=TRUE) IN 75 84

10 OUT =PEG_D2R_N<0..15> — PEG_D2R_N<0..15> (MAKE_BASE=TRUE) IN 75 84

18 IN PEG_CLKREQ_L — MXM_CLKREQ_L (MAKE_BASE=TRUE) OUT 73

73 MXM_RESET_L — PEG_RESET_L (MAKE_BASE=TRUE) 27 91

91 85 19 IN PM_CLK32K_SUSCLK_R — 1 R929 2 — PM_CLK32K_SUSCLK OUT 45 85 91

R929: 22, 5%, 1/16W, MF-LF, 402

PLACEMENT_NOTE=PLACE CLOSE TO U1800

SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE

Signal Aliases

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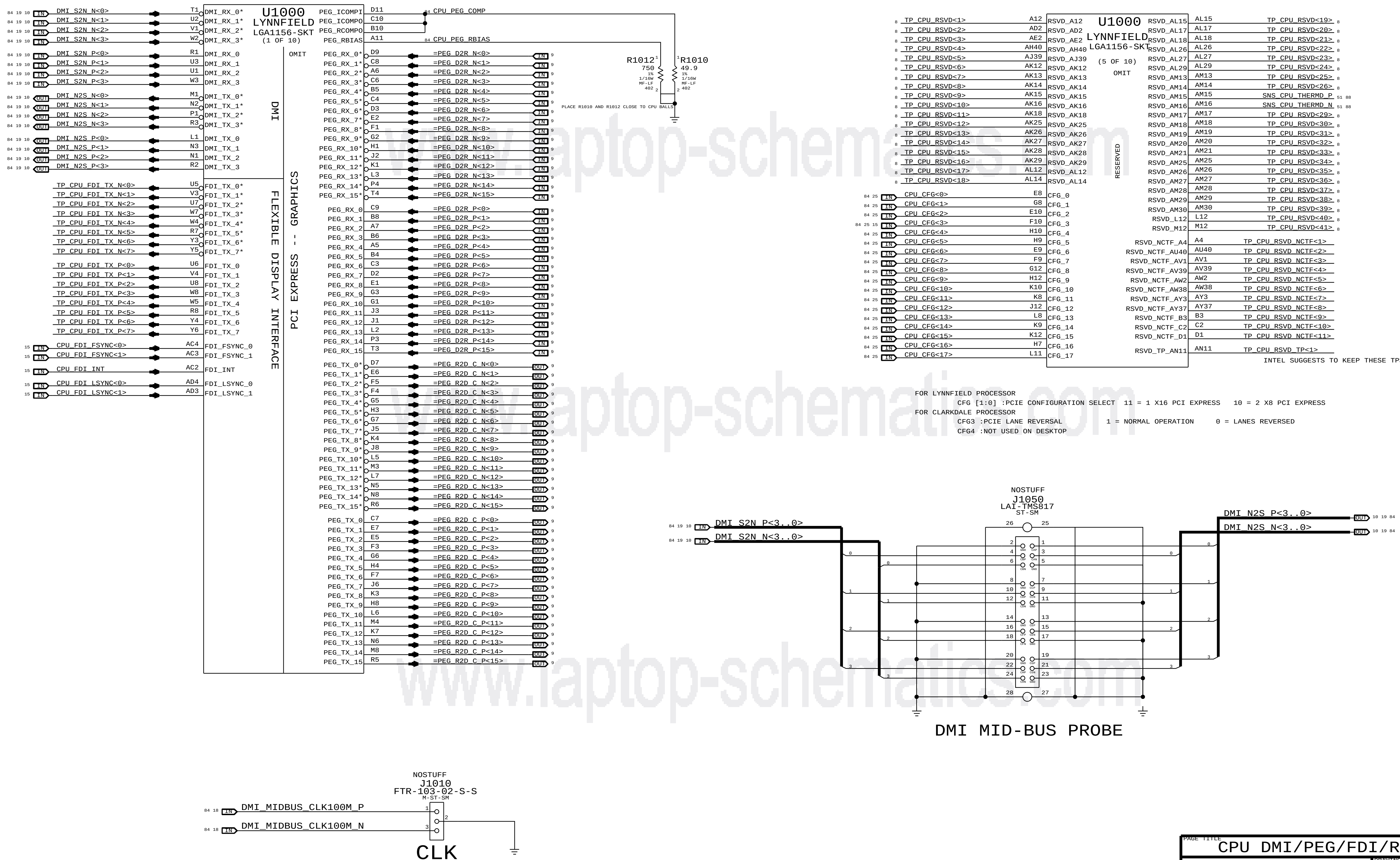

PAGE TITLE
CPU DMI/PEG/FDI/RSVD

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

REVISION B.0.0

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PAGE 10 OF 110

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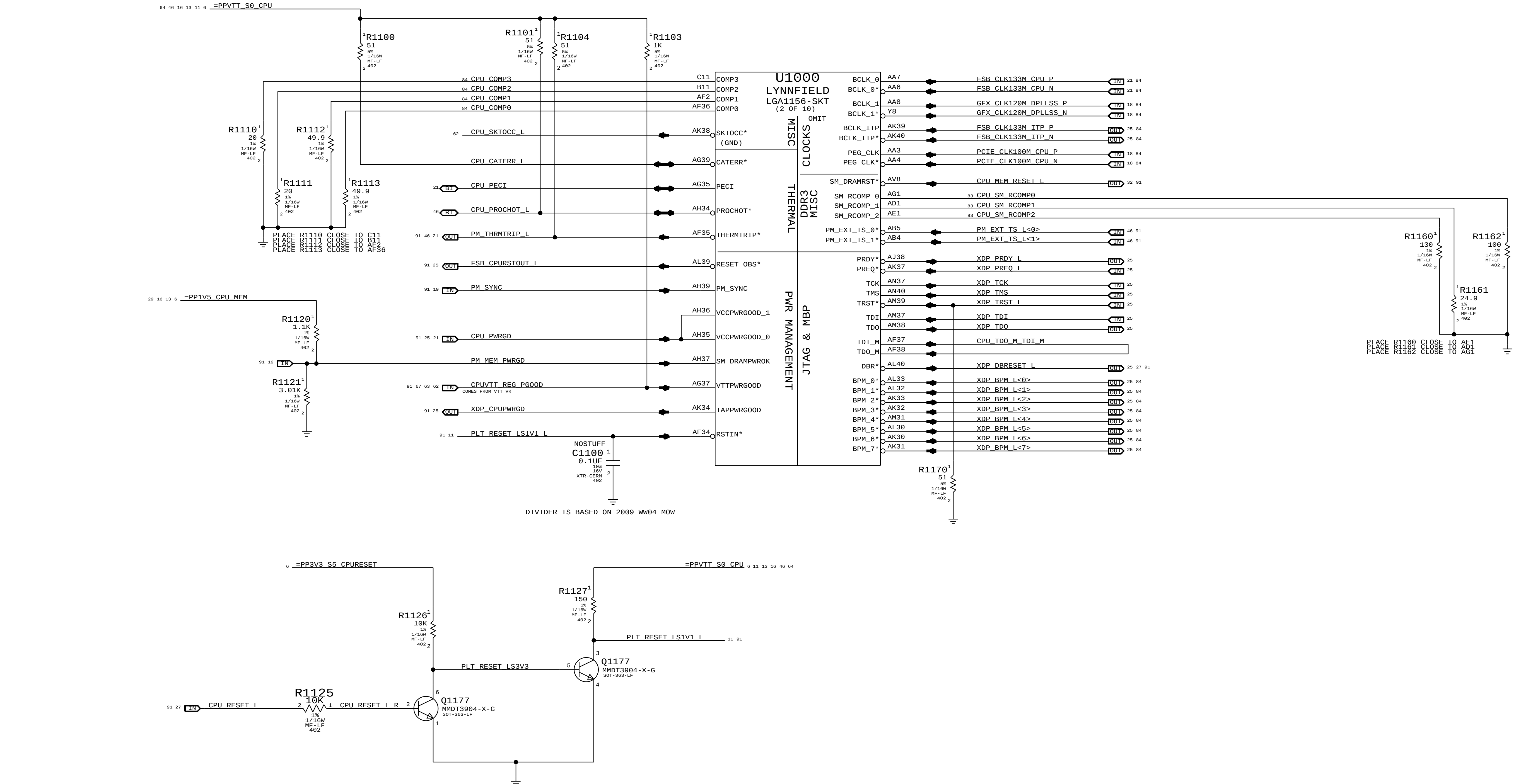

PAGE TITLE

CPU CLOCK/MISC/JTAG

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

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PAGE 11 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE

CPU DDR3 INTERFACES

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

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PAGE 12 OF 110

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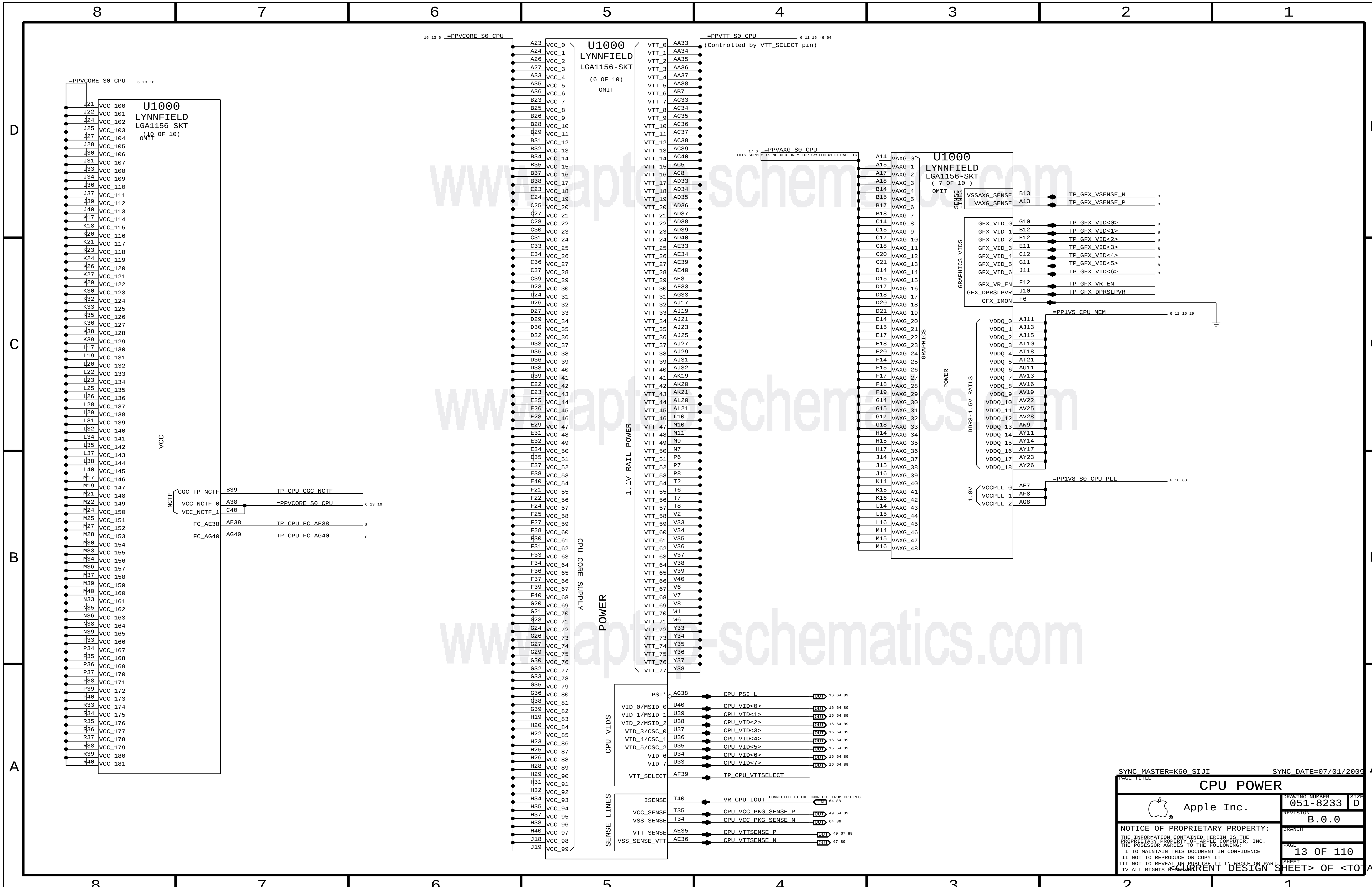

U1000
LYNNFIELD
LGA1156-SKT
(10 OF 10)
OMIT
=PPVCORE_S0_CPU
VCC
NCTF
CGC_TP_NCTF
VCC_NCTF_0
VCC_NCTF_1
FC_AE38
FC_AG40
TP_CPU_CGC_NCTF
TP_CPU_FC_AE38
TP_CPU_FC_AG40
U1000
LYNNFIELD
LGA1156-SKT
(6 OF 10)
OMIT
=PPVTT_S0_CPU
(Controlled by VTT_SELECT pin)
CPU CORE SUPPLY
POWER
1.1V RAIL POWER
CPU VIDS
PSI*
VID_0/MSID_0
VID_1/MSID_1
VID_2/MSID_2
VID_3/CSC_0
VID_4/CSC_1
VID_5/CSC_2
VID_6
VID_7
VTT_SELECT
CPU_PSI_L
CPU_VID<0>
CPU_VID<1>
CPU_VID<2>
CPU_VID<3>
CPU_VID<4>
CPU_VID<5>
CPU_VID<6>
CPU_VID<7>
TP_CPU_VTTSELECT
SENSE LINES
ISENSE
VCC_SENSE
VSS_SENSE
VTT_SENSE
VSS_SENSE_VTT
VR_CPU_IOUT
CONNECTED TO THE IMON OUT FROM CPU REG
CPU_VCC_PKG_SENSE_P
CPU_VCC_PKG_SENSE_N
CPU_VTTSENSE_P
CPU_VTTSENSE_N
=PPVAXG_S0_CPU
THIS SUPPLY IS NEEDED ONLY FOR SYSTEM WITH DALE IG
U1000
LYNNFIELD
LGA1156-SKT
(7 OF 10)
OMIT
GRAPHICS
POWER
SENSE LINES
VSSAXG_SENSE
VAXG_SENSE
TP_GFX_VSENSE_N
TP_GFX_VSENSE_P
GRAPHICS VIDS
GFX_VID_0
GFX_VID_1
GFX_VID_2
GFX_VID_3
GFX_VID_4
GFX_VID_5
GFX_VID_6
GFX_VR_EN
GFX_DPRSLPVR
GFX_IMON
TP_GFX_VID<0>
TP_GFX_VID<1>
TP_GFX_VID<2>
TP_GFX_VID<3>
TP_GFX_VID<4>
TP_GFX_VID<5>
TP_GFX_VID<6>
TP_GFX_VR_EN
TP_GFX_DPRSLPVR
=PP1V5_CPU_MEM
DDR3-1.5V RAILS
=PP1V8_S0_CPU_PLL
1.8V
VCCPLL_0
VCCPLL_1
VCCPLL_2
SYNC_MASTER=K60_SIJI
SYNC_DATE=07/01/2009
PAGE TITLE
CPU POWER
Apple Inc.
DRAWING NUMBER
051-8233
SIZE
D
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BRANCH
PAGE
13 OF 110
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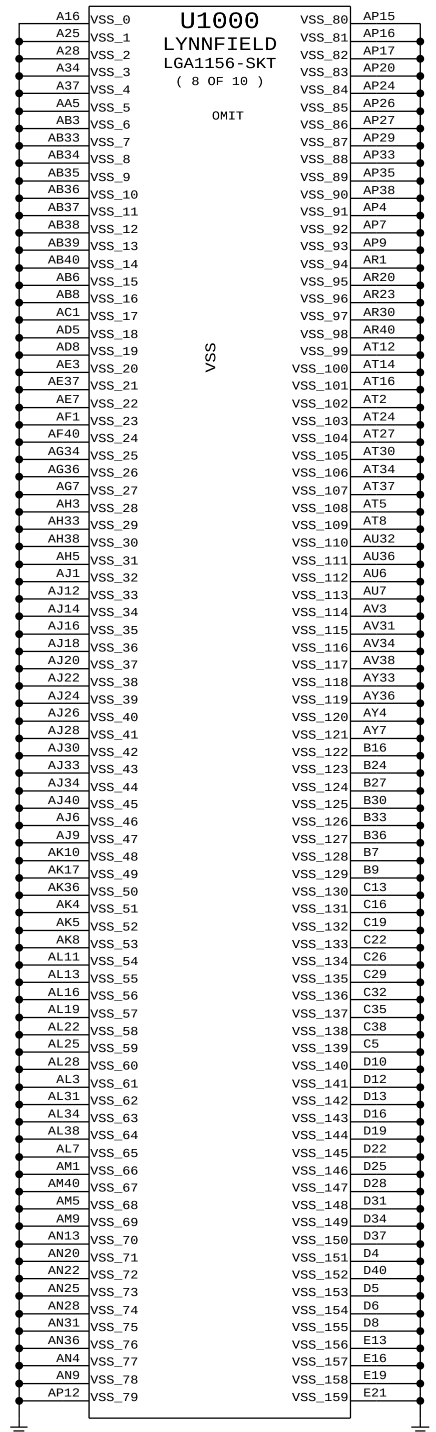

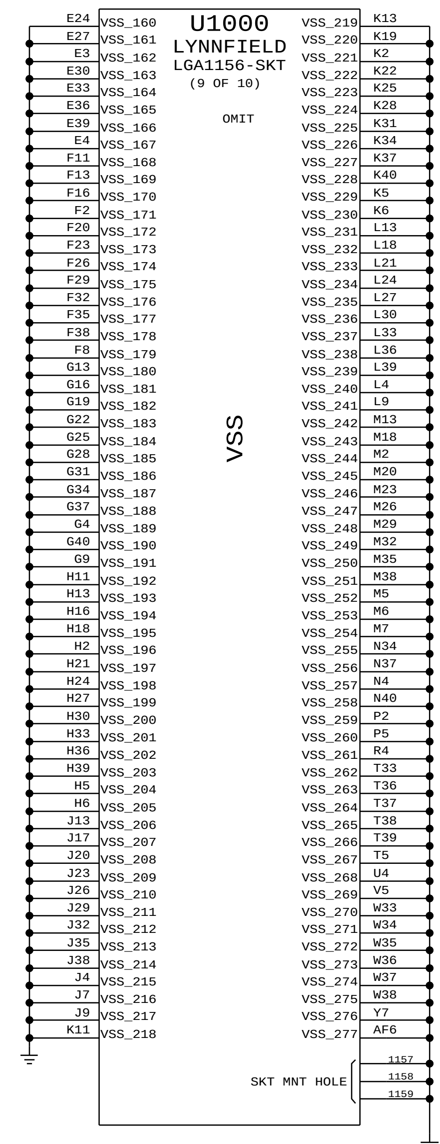

PAGE TITLE
CPU GROUNDS

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

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PAGE 14 OF 110

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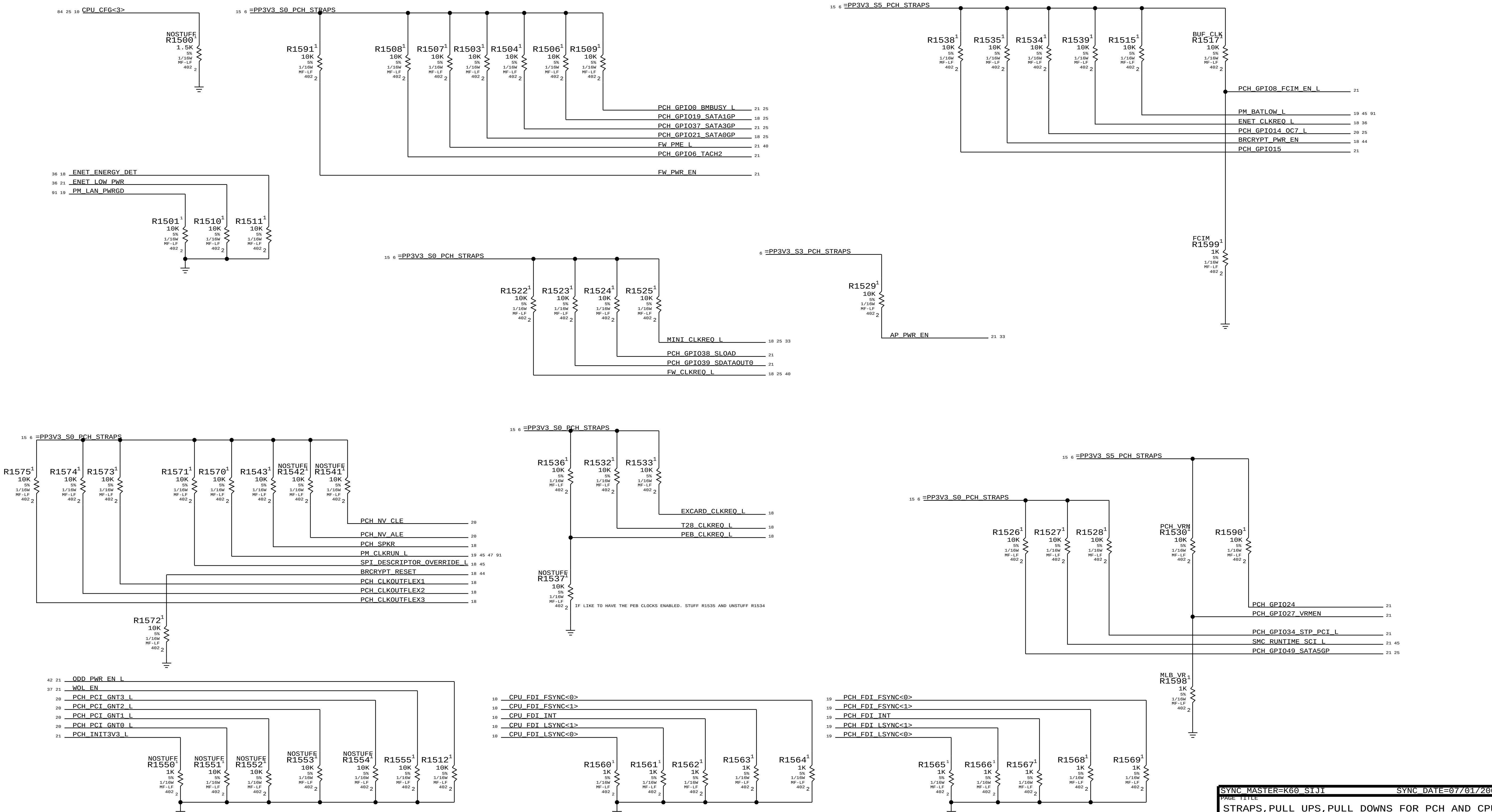

SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE

STRAPS,PULL UPS,PULL DOWNS FOR PCH AND CPU

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

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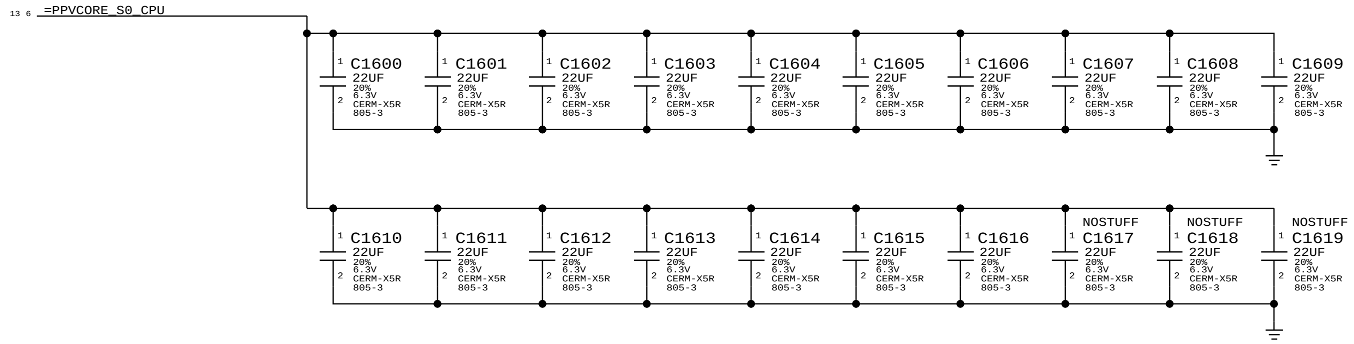
PAGE 15 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

CPU VCORE DECOUPLING

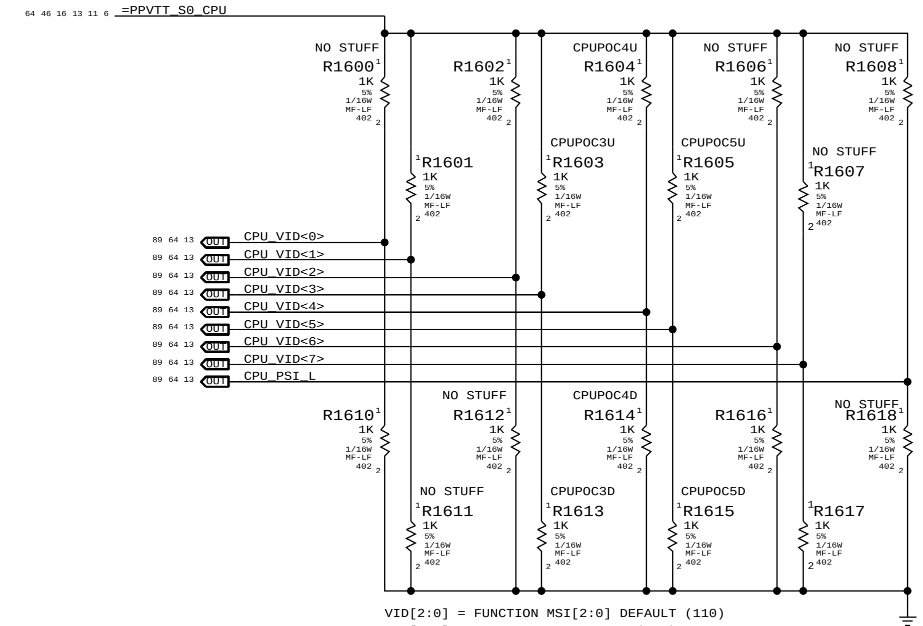
INTEL RECOMMENDATION 17X 22UF 0805



BULK CAPS ON CPU VREG PAGE 74

CPU Power On Configuration (POC) Straps

Intel recommends all option straps should be provided in layout



VID[2:0] = FUNCTION MSI[2:0] DEFAULT (110)
VID[5:3] = IMON CONFIG DEFAULT (101)
VID[6] = Reserved (0)
VID[7] = VRD SELECT (0)
PSI# = Reserved (0)

VTT (CPU Uncore) DECOUPLING

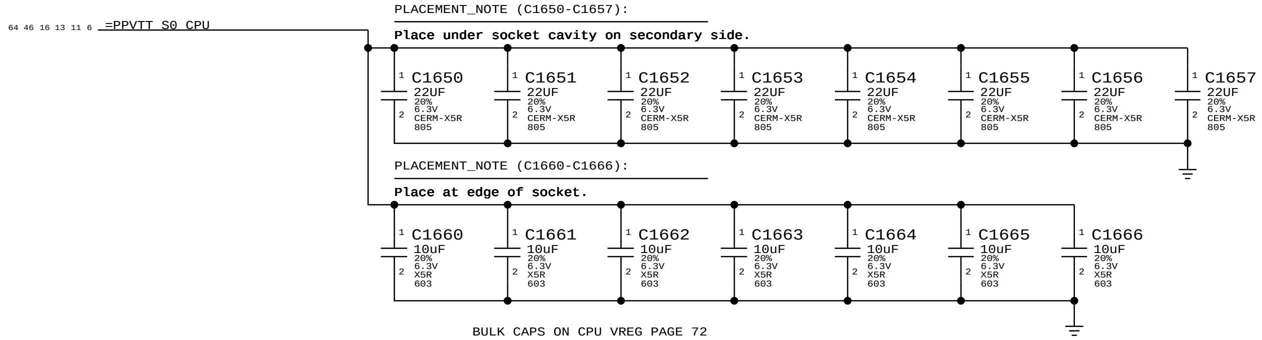
8X 22UF 0805, 7X 10UF 0805 INTEL RECOMMENDATION 9X22UF 0805

PLACEMENT_NOTE (C1650-C1657):

Place under socket cavity on secondary side.

PLACEMENT_NOTE (C1660-C1666):

Place at edge of socket.



BULK CAPS ON CPU VREG PAGE 72

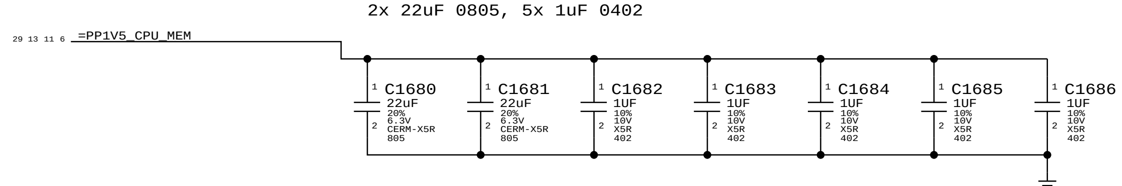
MSI - MARKET SEGMENT IDENTIFICATION
PREVENTS THE PLATFORM BOOTING USING A HIGHER POWERED CPU

BOM GROUP	IMAX @ 900mV	CPU Gain Setting	BOM OPTIONS	Equivalent Gain
CPUPOC_IMAX_DIS		000	CPUPOC3D,CPUPOC4D,CPUPOC5D	
CPUPOC_IMAX_0_40	40A	001	CPUPOC3D,CPUPOC4D,CPUPOC5U	45
CPUPOC_IMAX_40_60	60A	010	CPUPOC3D,CPUPOC4U,CPUPOC5D	30
CPUPOC_IMAX_60_80	80A	011	CPUPOC3D,CPUPOC4U,CPUPOC5U	22.5
CPUPOC_IMAX_80_100	100A	100	CPUPOC3U,CPUPOC4D,CPUPOC5D	18
CPUPOC_IMAX_100_120	120A	101	CPUPOC3U,CPUPOC4D,CPUPOC5U	15
CPUPOC_IMAX_120_140	140A	110	CPUPOC3U,CPUPOC4U,CPUPOC5D	12.857
CPUPOC_IMAX_140_180	180A	111	CPUPOC3U,CPUPOC4U,CPUPOC5U	10

NOTE: BOM Configurations should not call out CPUPOCnU/D BOMOPTIONs directly.
Instead call out appropriate BOM GROUP defined in tables above.

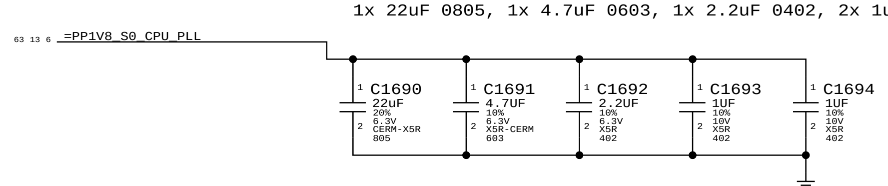
Memory (CPU VCCDDR) DECOUPLING

2x 22uF 0805, 5x 1uF 0402



PLL (CPU VCCSFR) DECOUPLING

1x 22uF 0805, 1x 4.7uF 0603, 1x 2.2uF 0402, 2x 1uF 0402



SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE
CPU NON-GFX DECOUPLING

Apple Inc.

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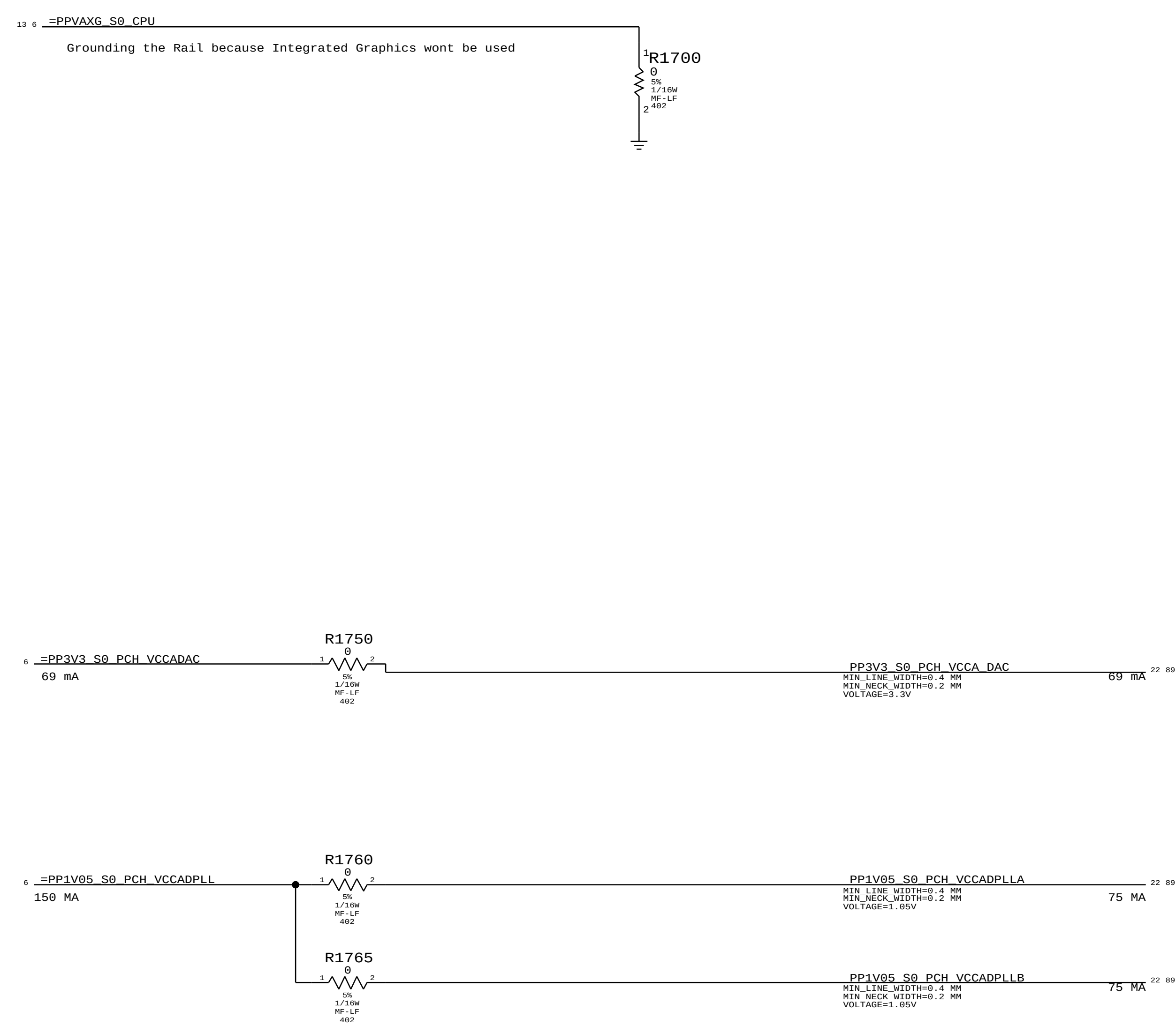

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PAGE TITLE

CPU/PCH GFX DECOUPLING

Apple Inc.

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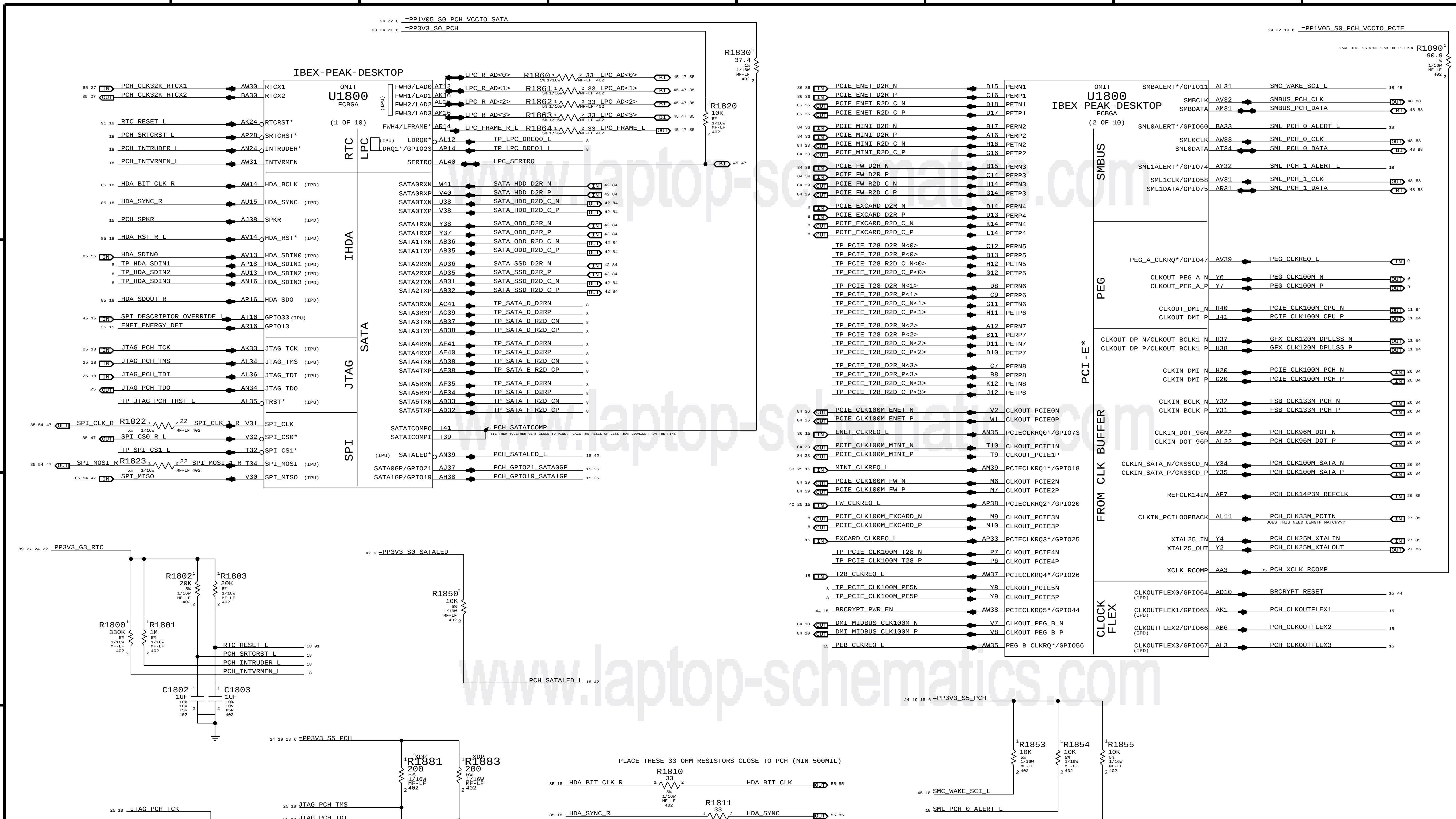

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SYNC_DATE=07/01/2009

PAGE TITLE
PCH SATA/PCIE/CLK/LPC/SPI

Apple Inc.

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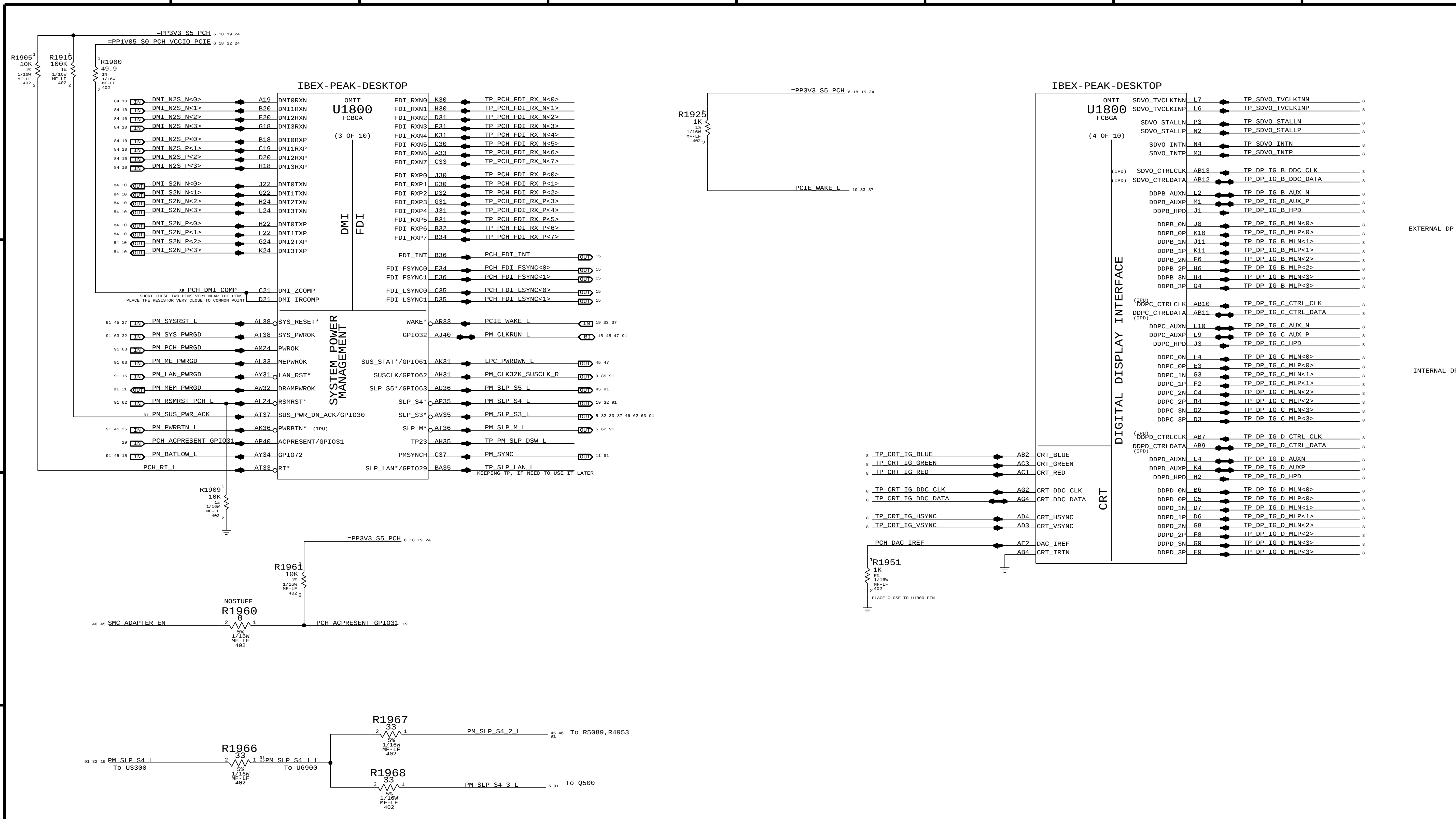

PAGE TITLE
PCH DMI/FDI/GRAPHICS

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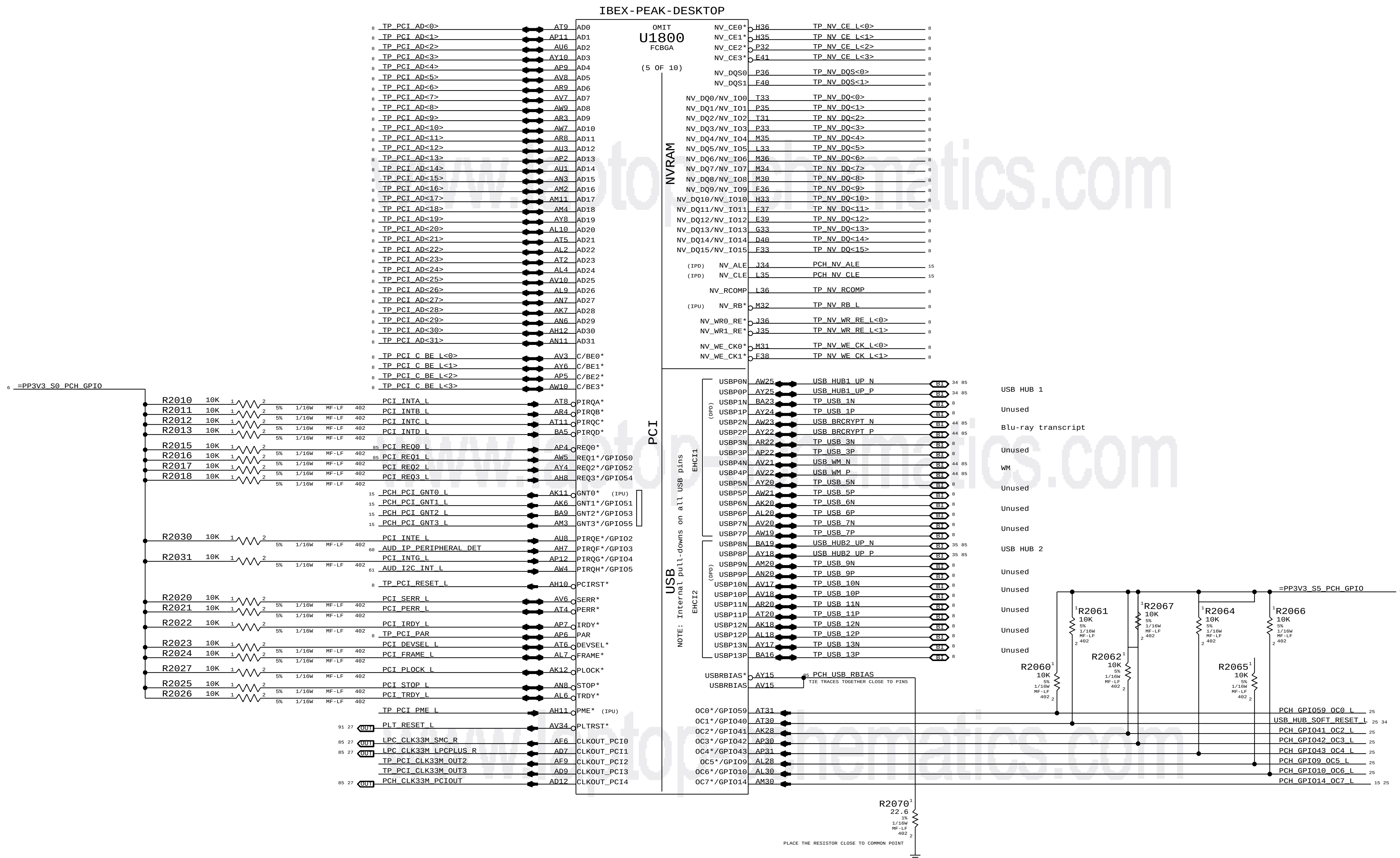

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PAGE TITLE

PCH PCI/FLASHCACHE/USB

Apple Inc.

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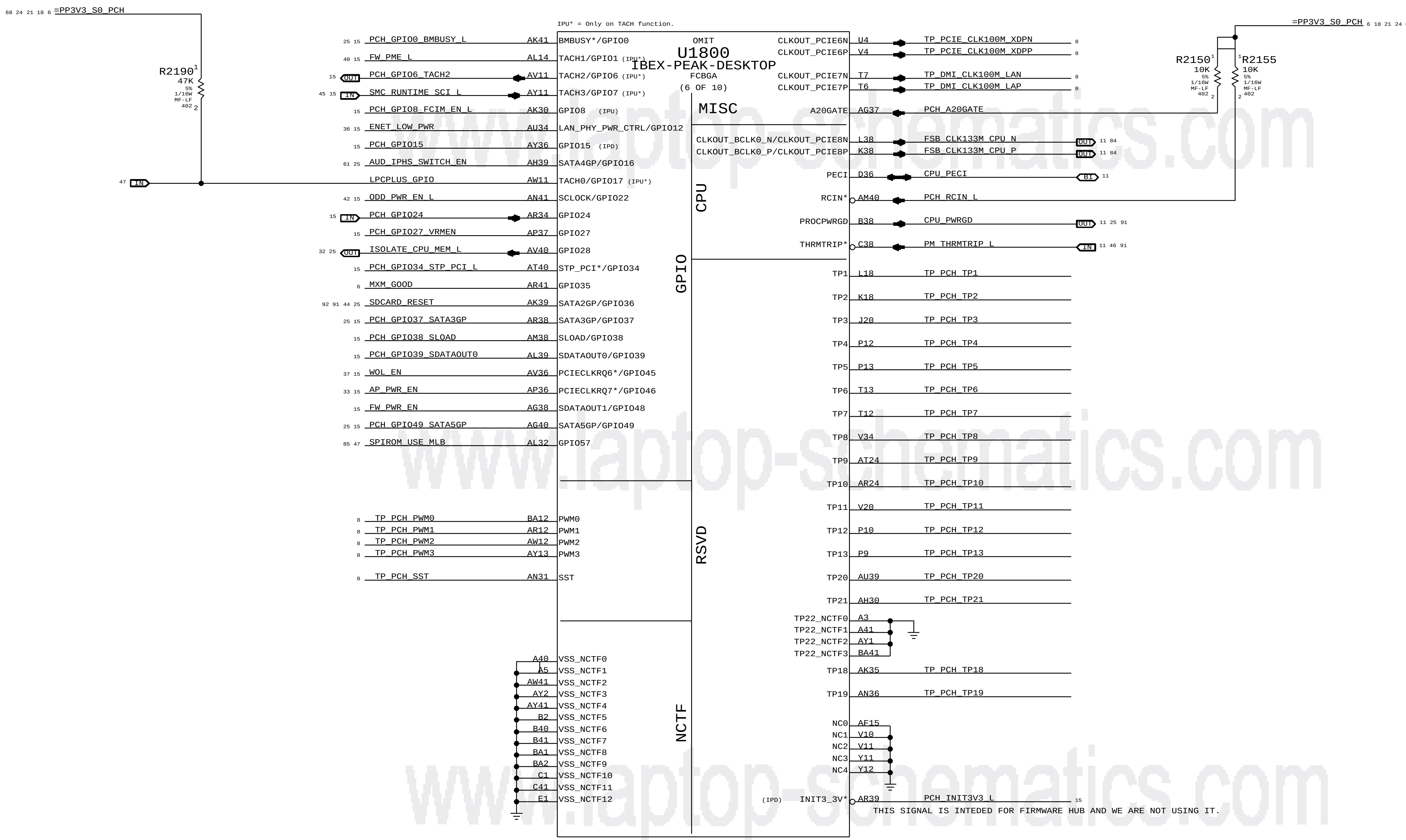

SYNC_MASTER=K60_SIJI

SYNC_DATE=07/01/2009

PAGE TITLE

PCH MISC

Apple Inc.

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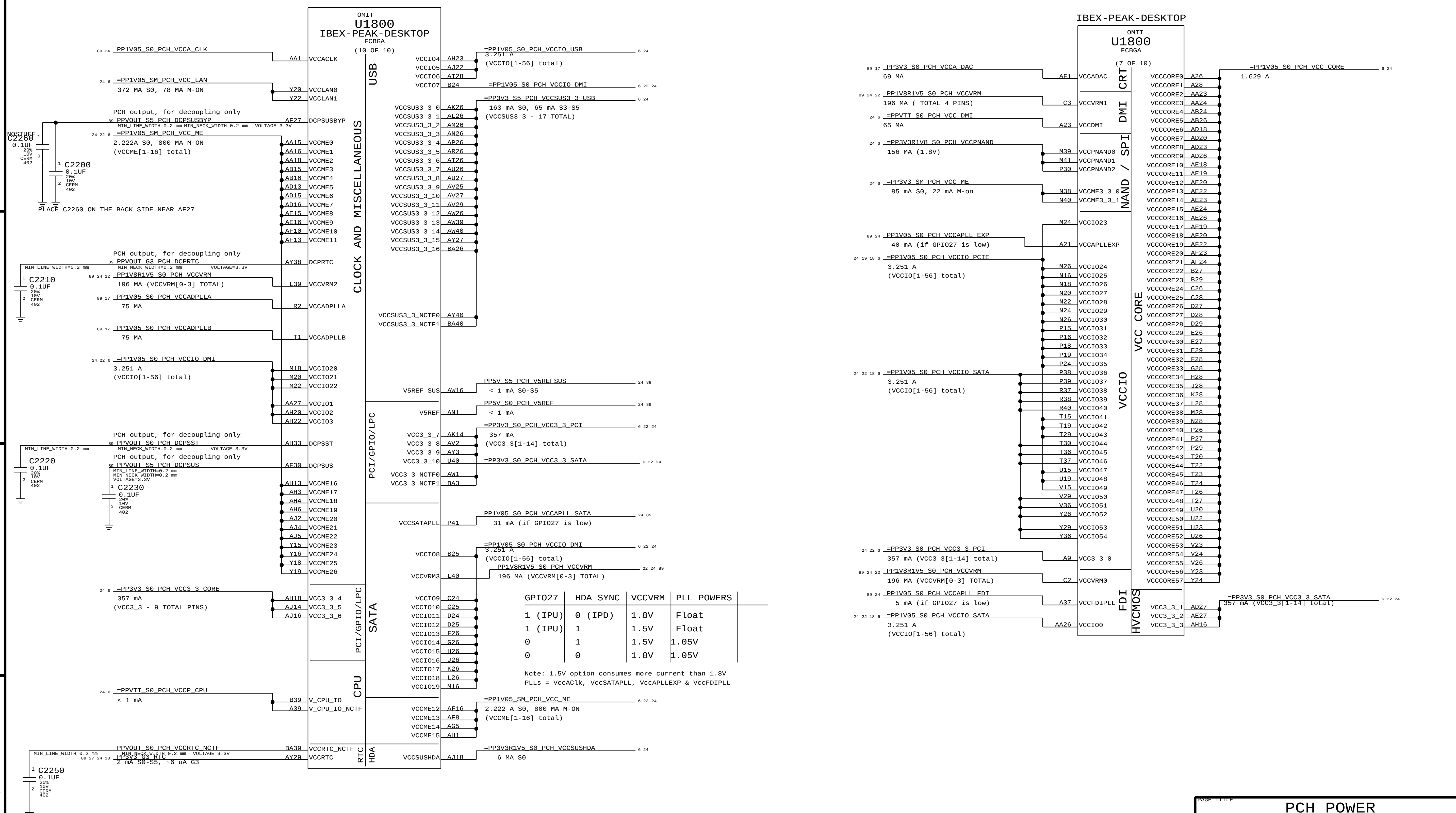

GPIO27	HDA_SYNC	VCCVRM	PLL POWERS
1 (IPU)	0 (IPD)	1.8V	Float
1 (IPU)	1	1.5V	Float
0	1	1.5V	1.05V
0	0	1.8V	1.05V

Note: 1.5V option consumes more current than 1.8V
PLLs = VccAClk, VccSATAPLL, VccAPLLEXP & VccFDIPLL

PAGE TITLE
PCH POWER

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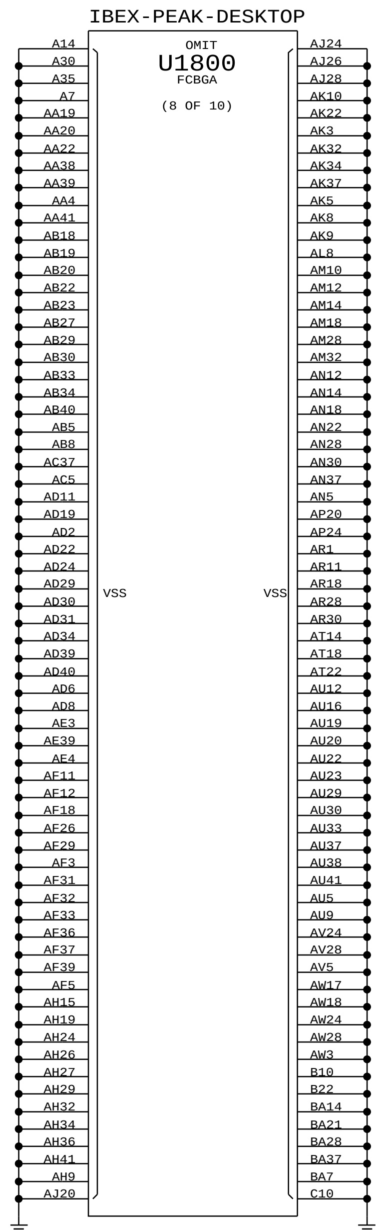

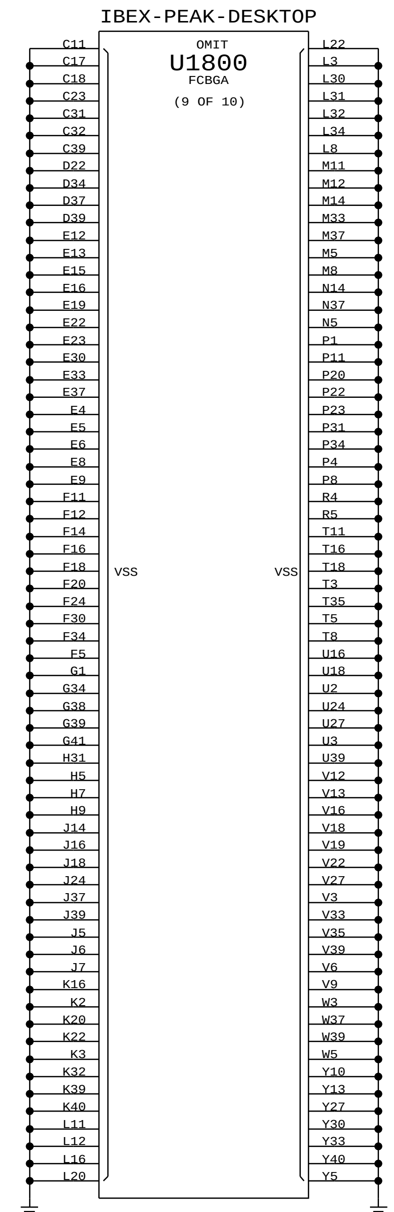

SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE

PCH GROUNDS

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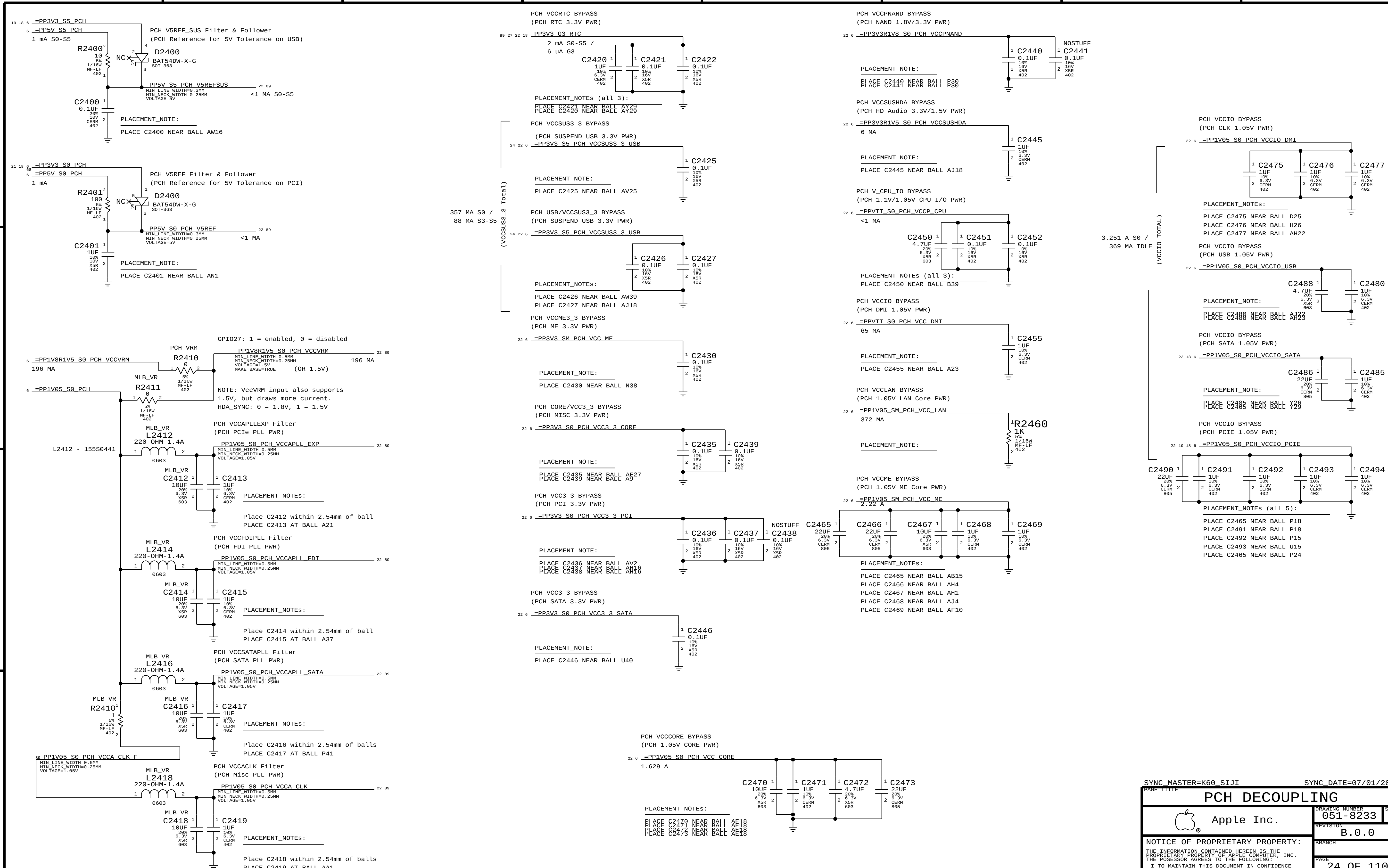

Current numbers from Ibex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE
PCH DECOUPLING

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PAGE 24 OF 110

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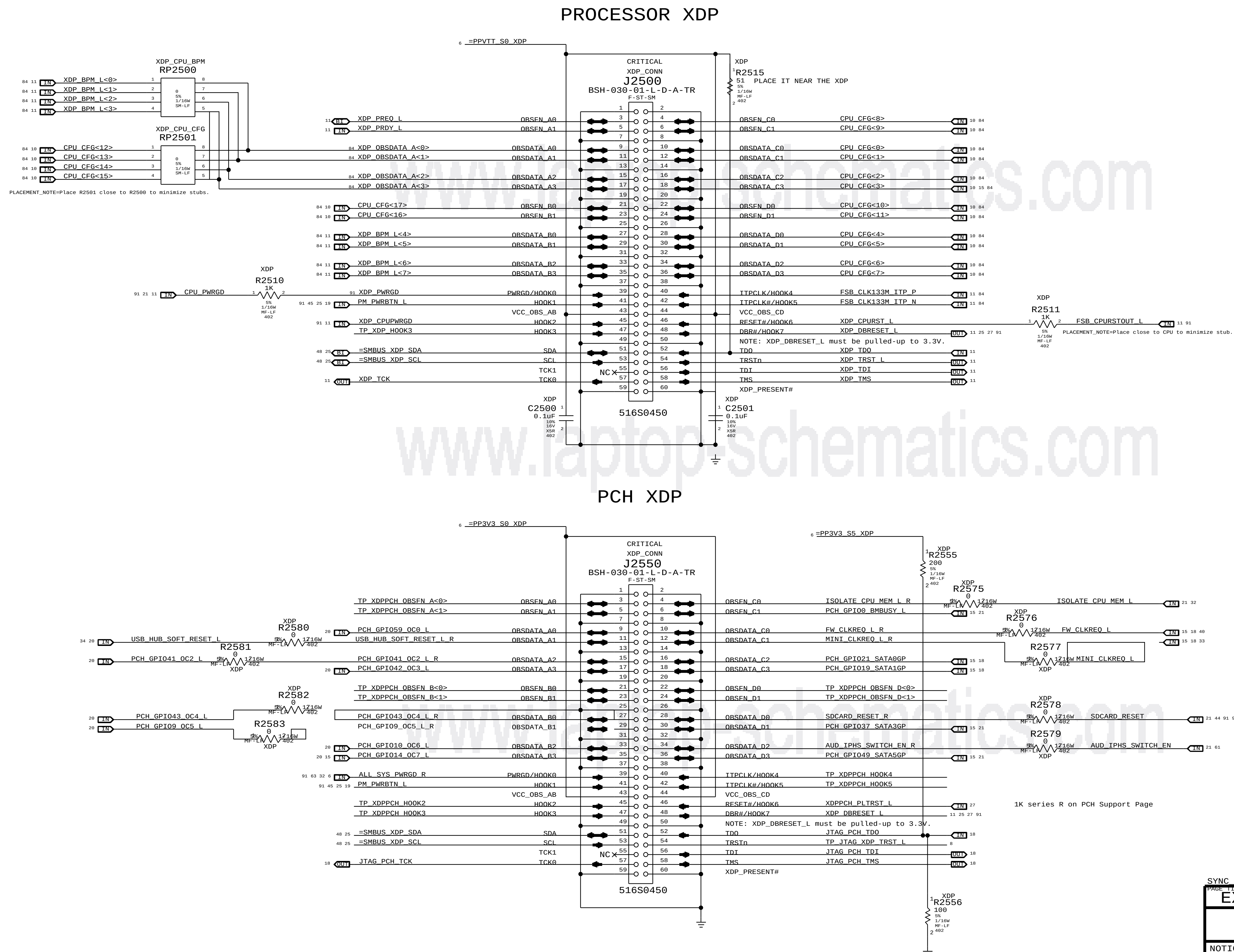

SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE
EXTENDED DEBUG PORT(XDP)

Apple Inc.

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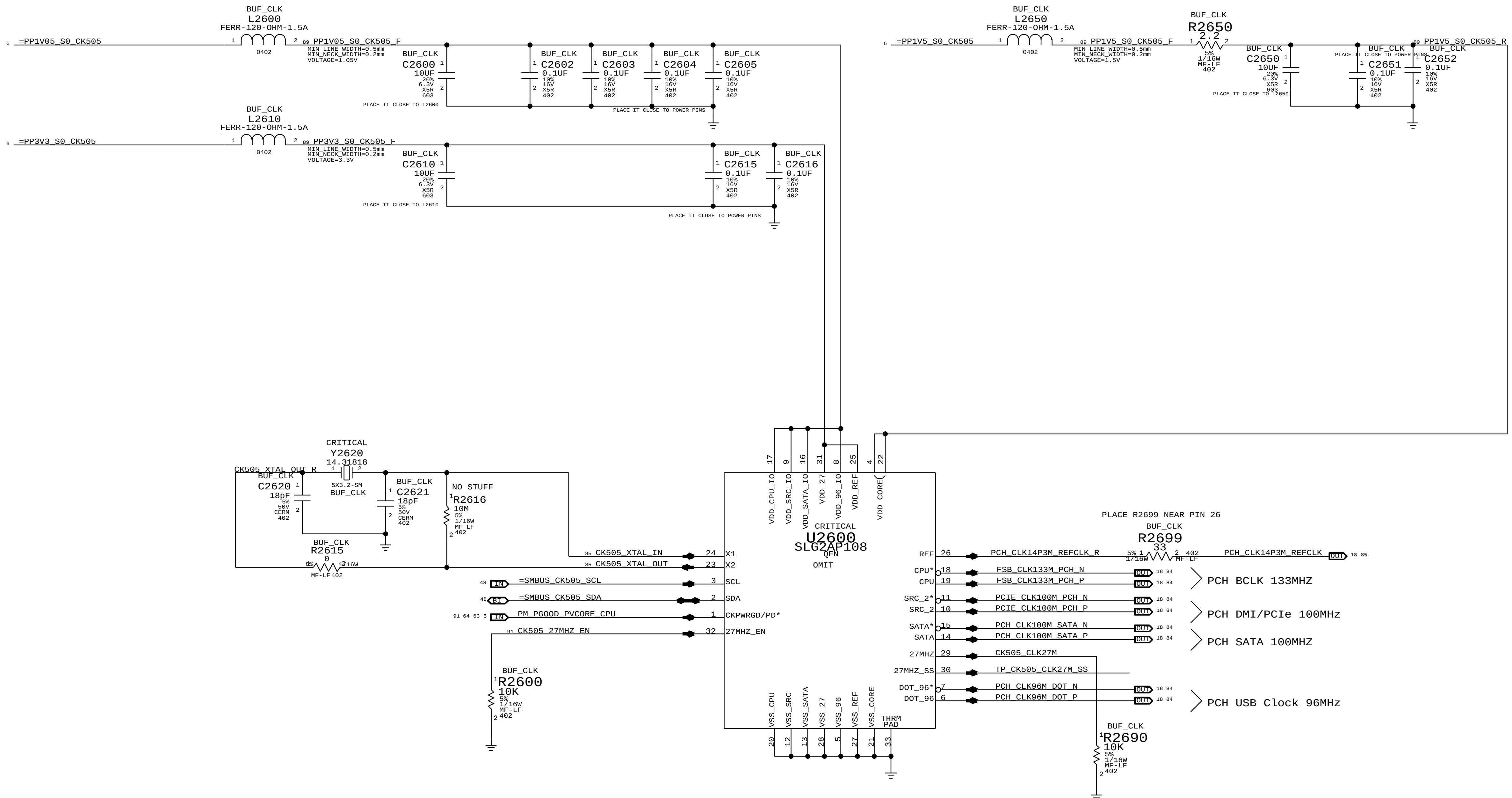
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE

CLOCK (CK505)

Apple Inc.

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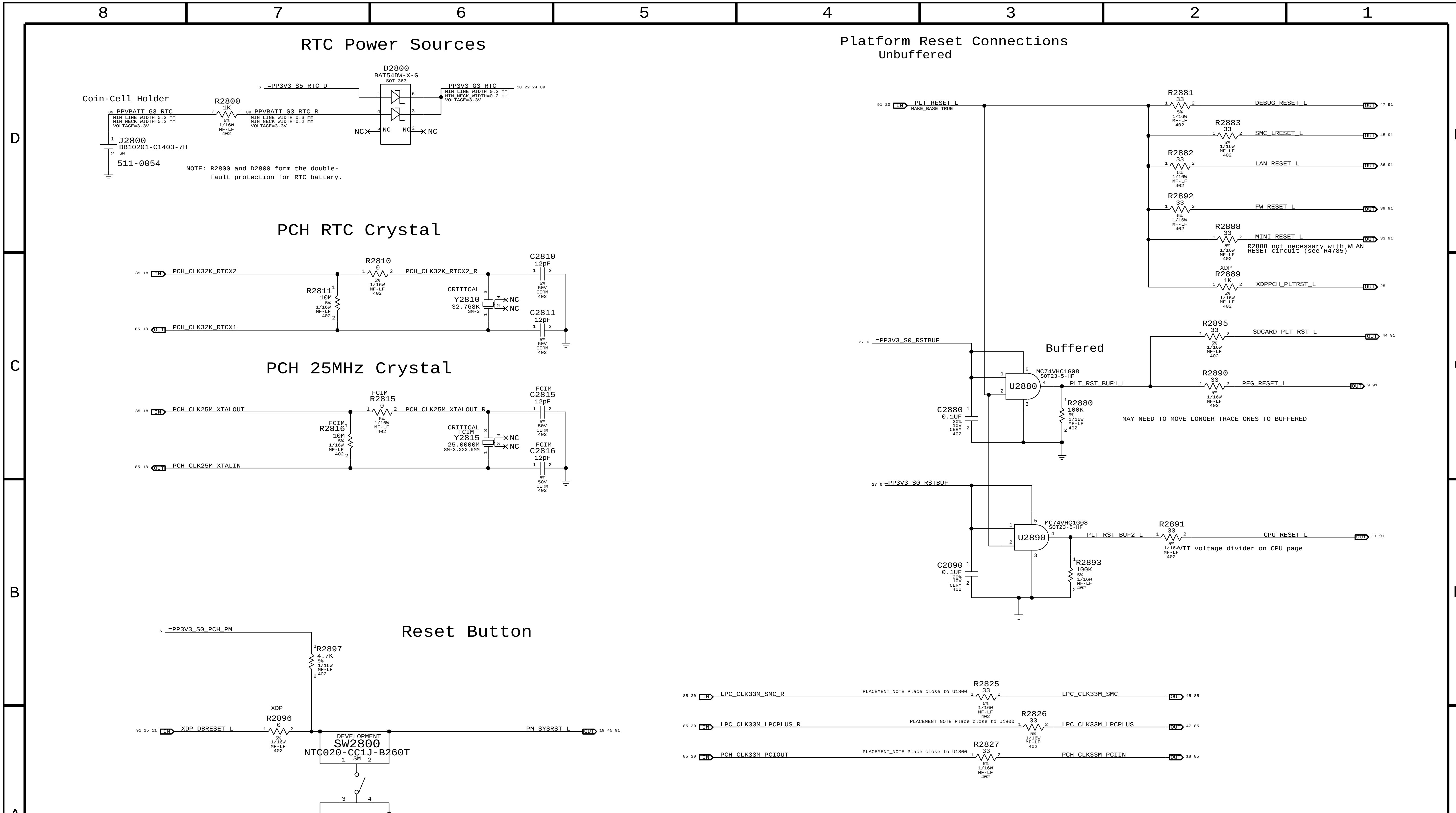

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PAGE TITLE

CHIPSET SUPPORT

Apple Inc.

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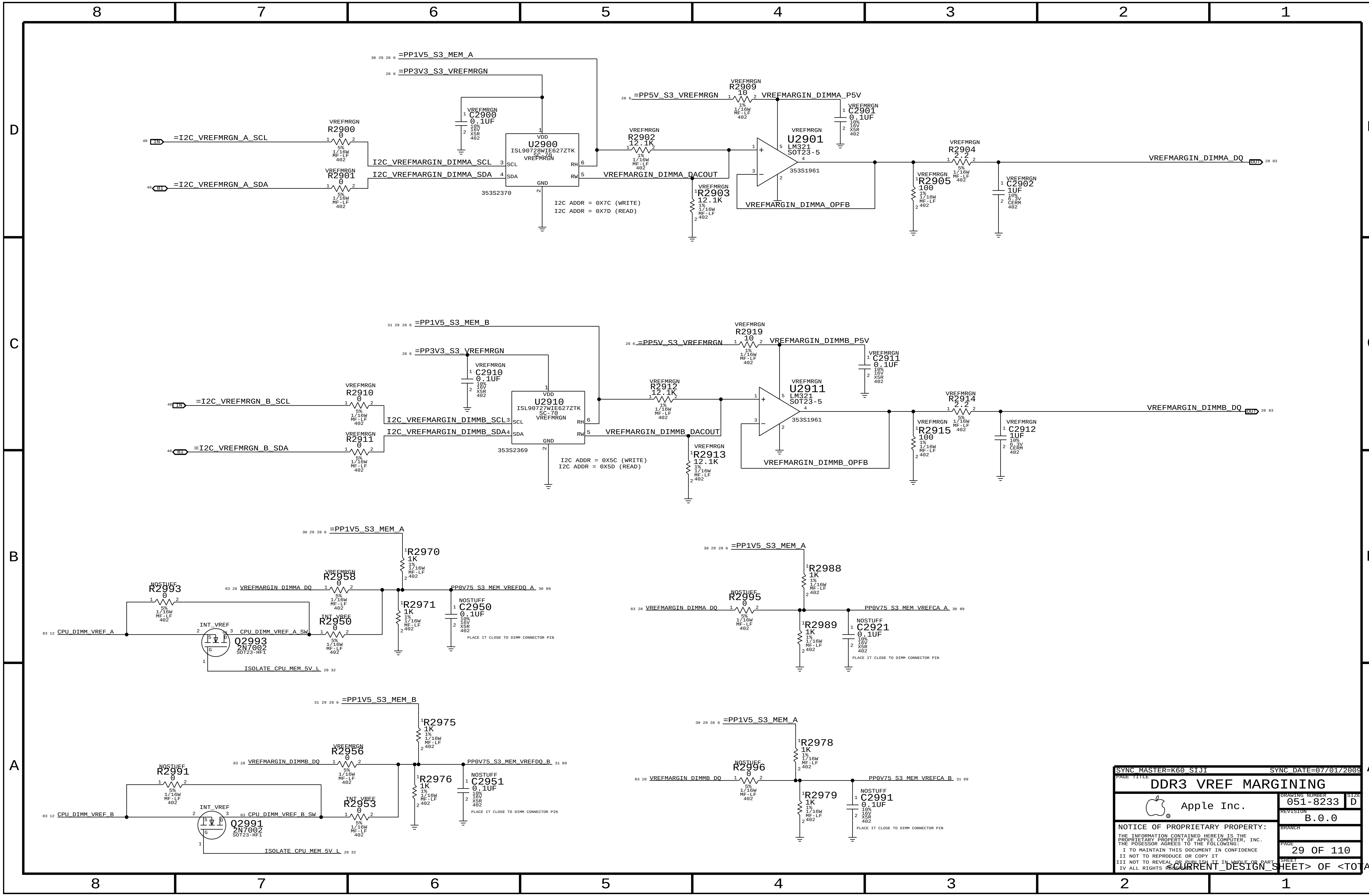

SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE

DDR3 VREF MARGINING

Apple Inc.

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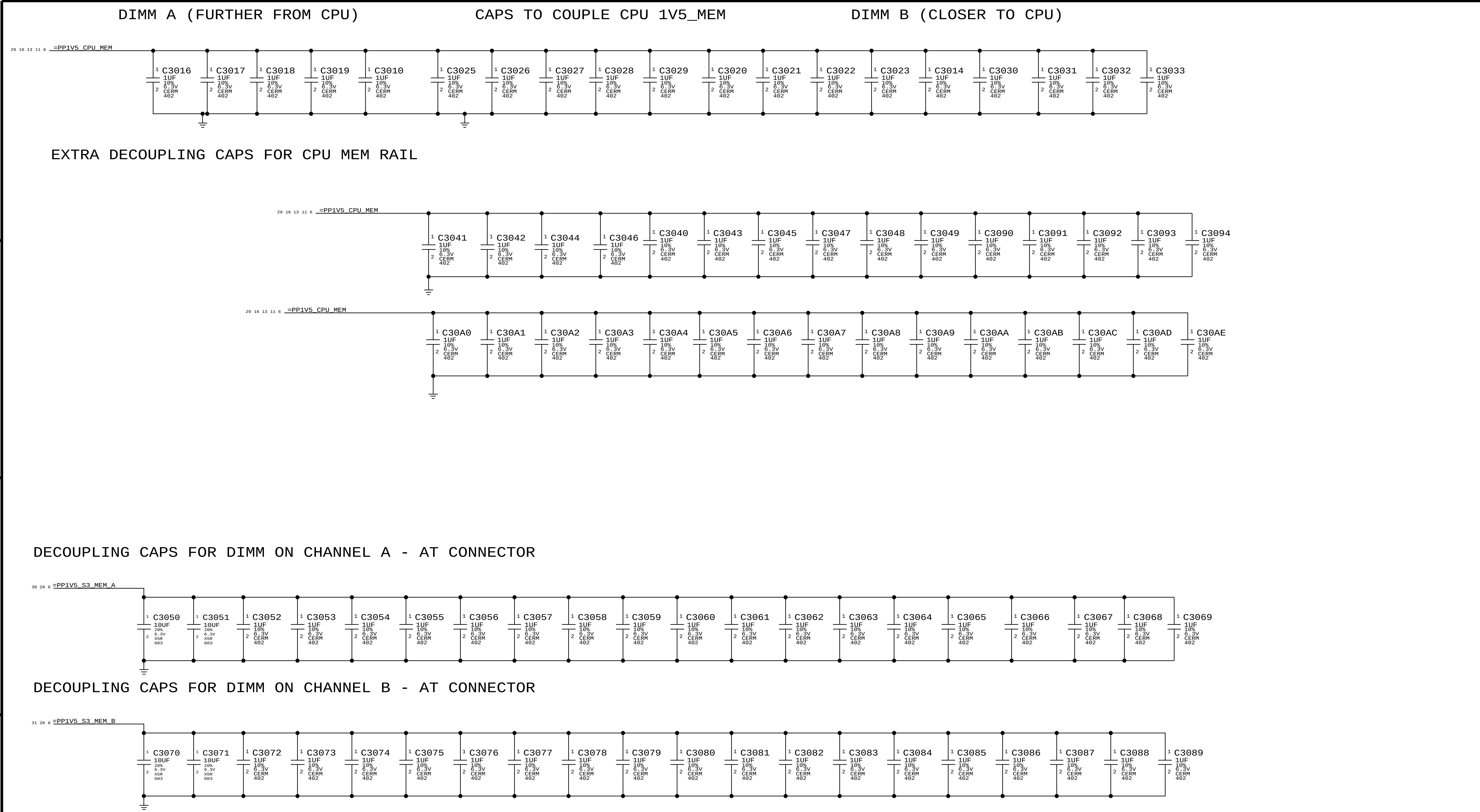

SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE
MEMORY CAPS

Apple Inc.

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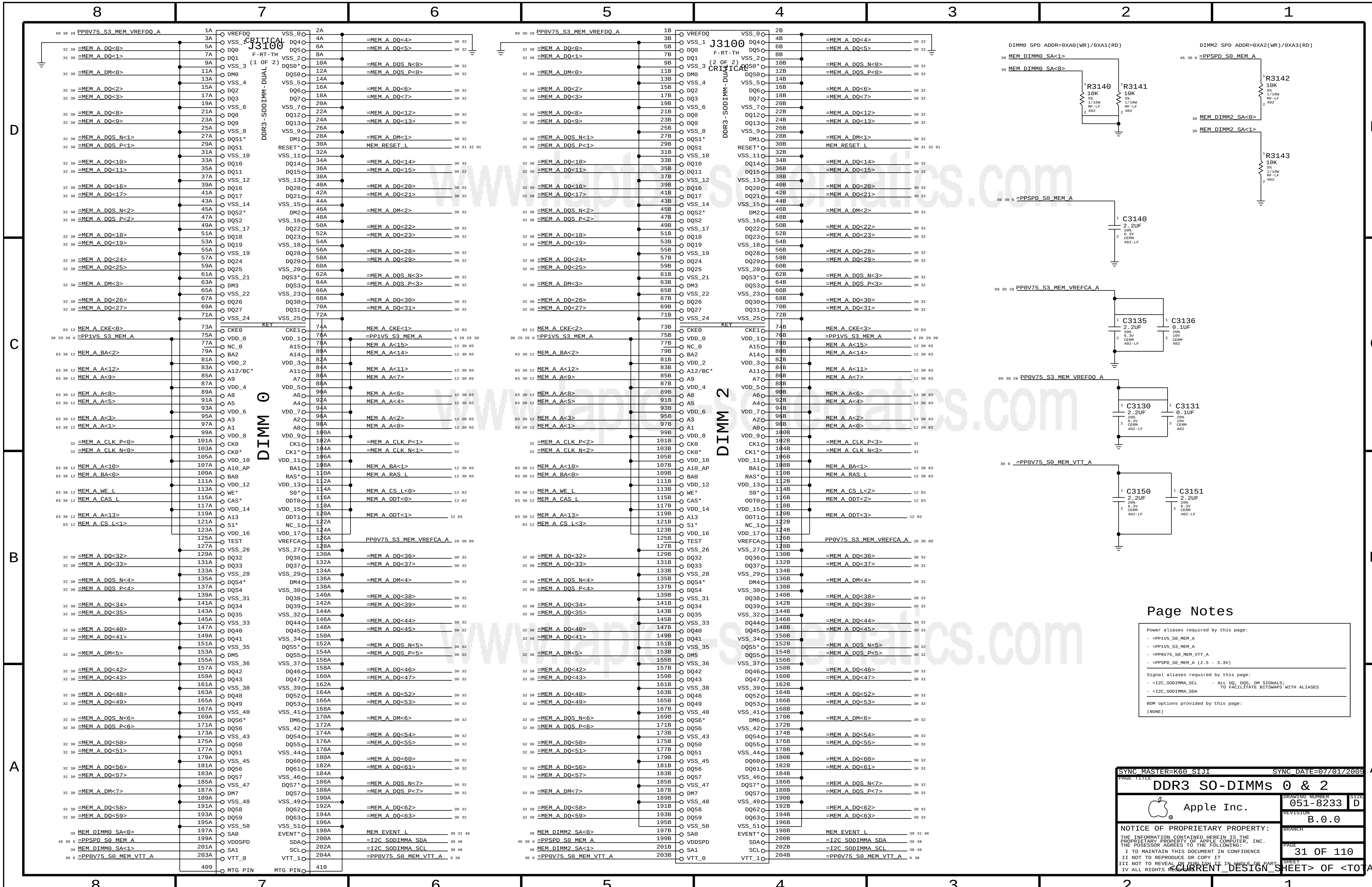

SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE

DDR3 SO-DIMMs 0 & 2

Apple Inc.

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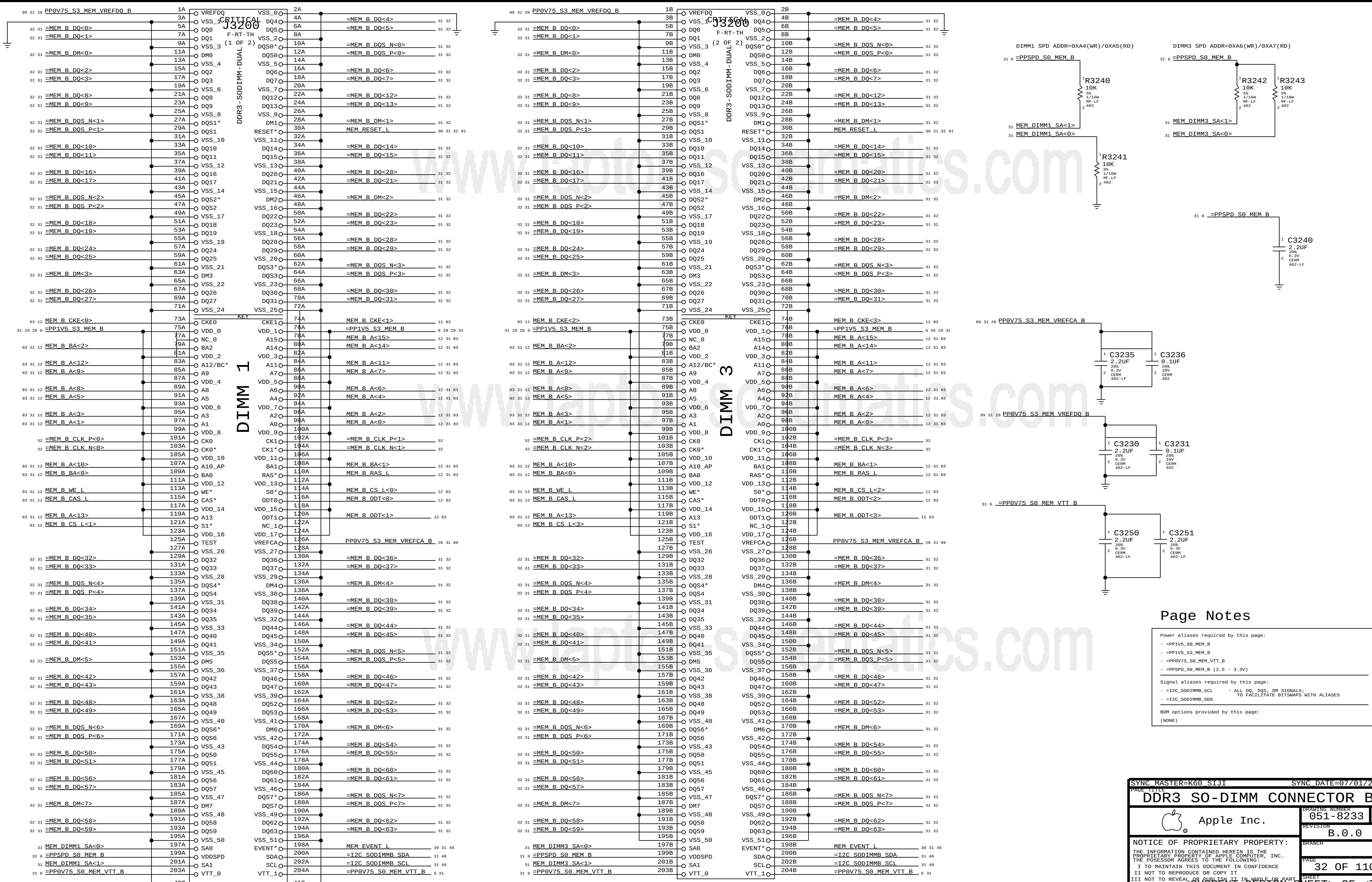

Page Notes

Power aliases required by this page:

- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMB_SCL — - ALL DQ, DQS, DM SIGNALS; TO FACILITATE BITSWAPS WITH ALIASES
- =I2C_SODIMMB_SDA

BOM options provided by this page:

(NONE)

SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE

DDR3 SO-DIMM CONNECTOR B

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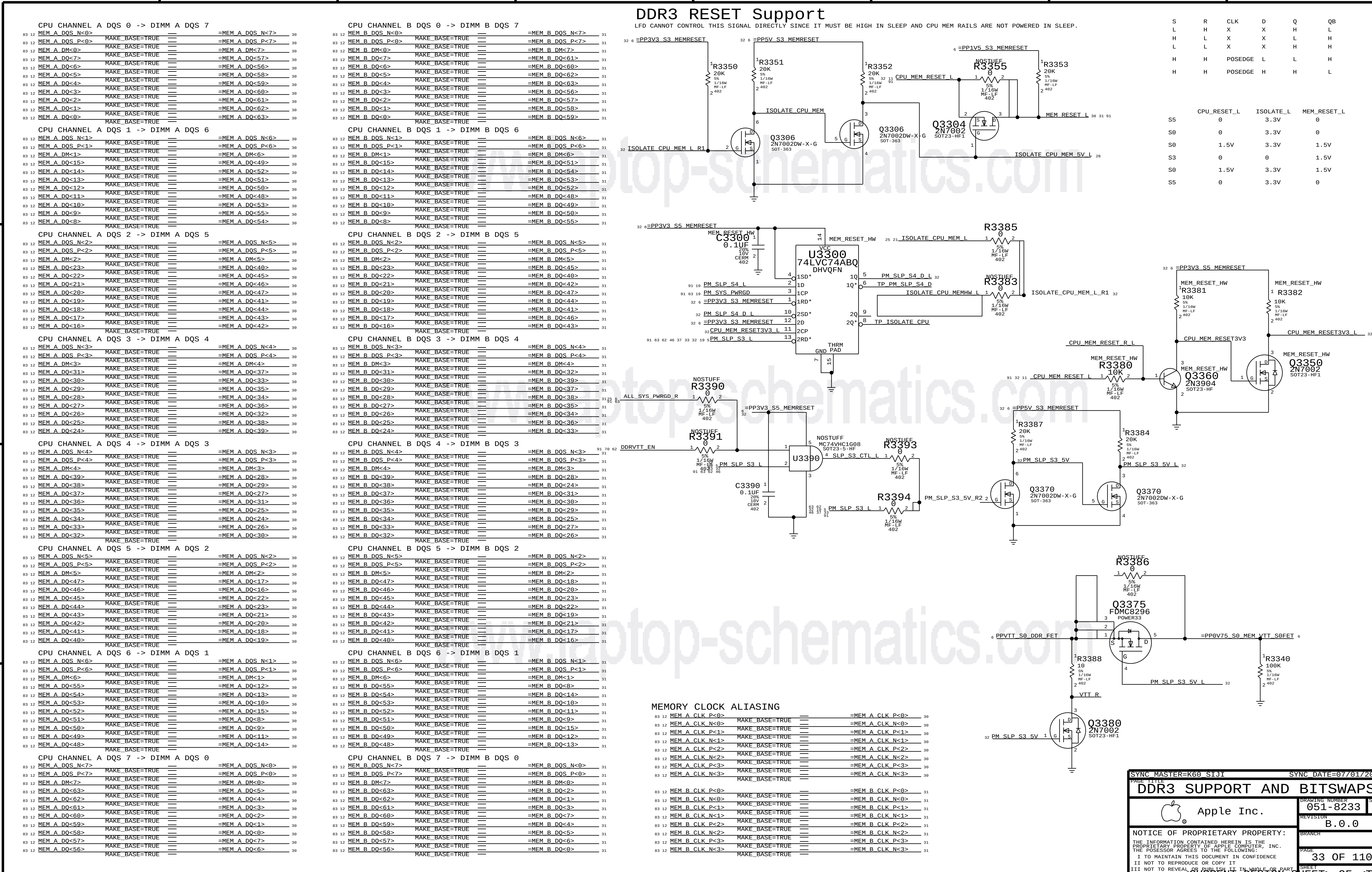

SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE

DDR3 SUPPORT AND BITSWAPS

Apple Inc.

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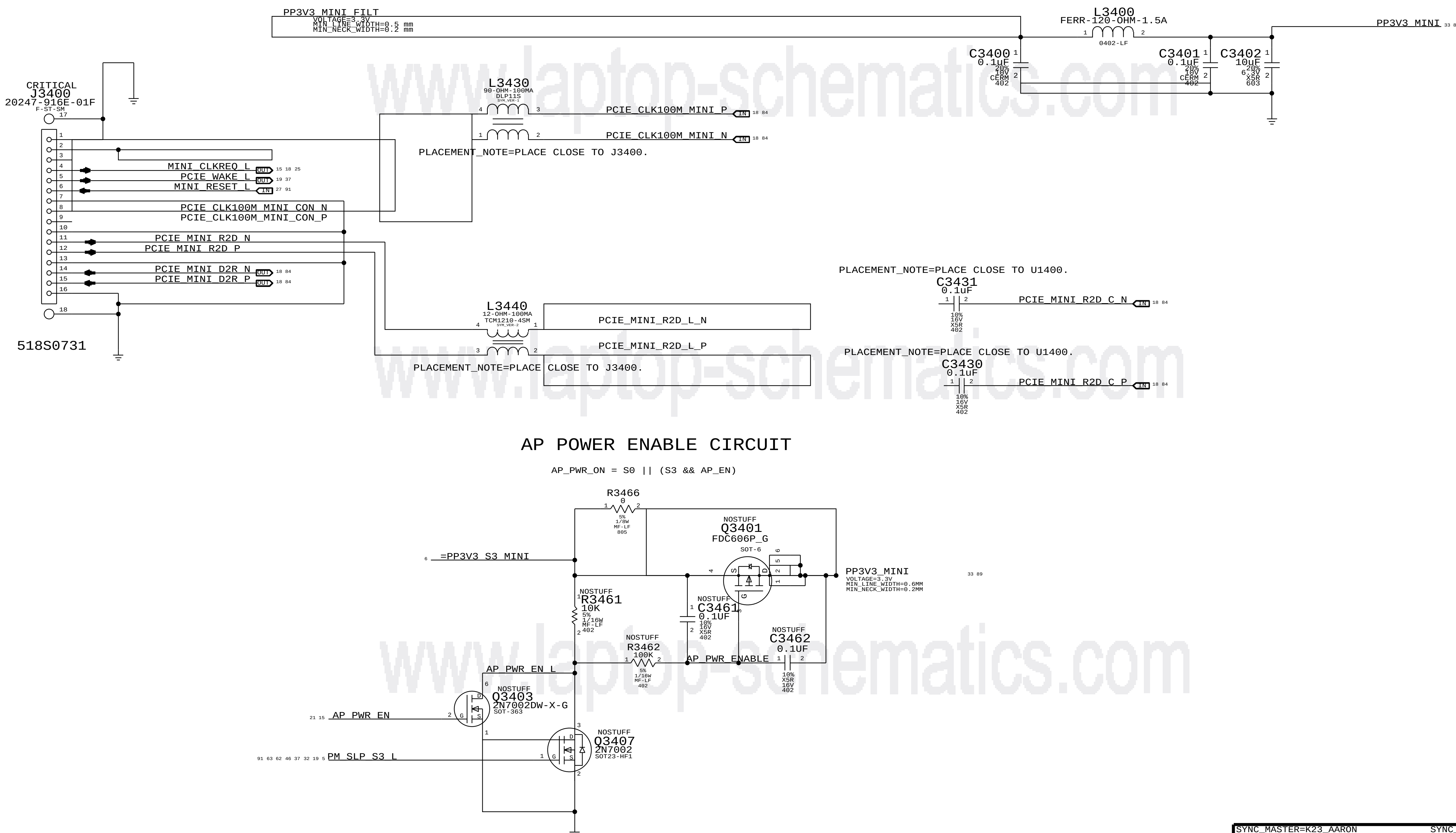

SYNC_MASTER=K23_AARON SYNC_DATE=07/16/2009

PAGE TITLE

PCI-E Wireless Connector

Apple Inc.

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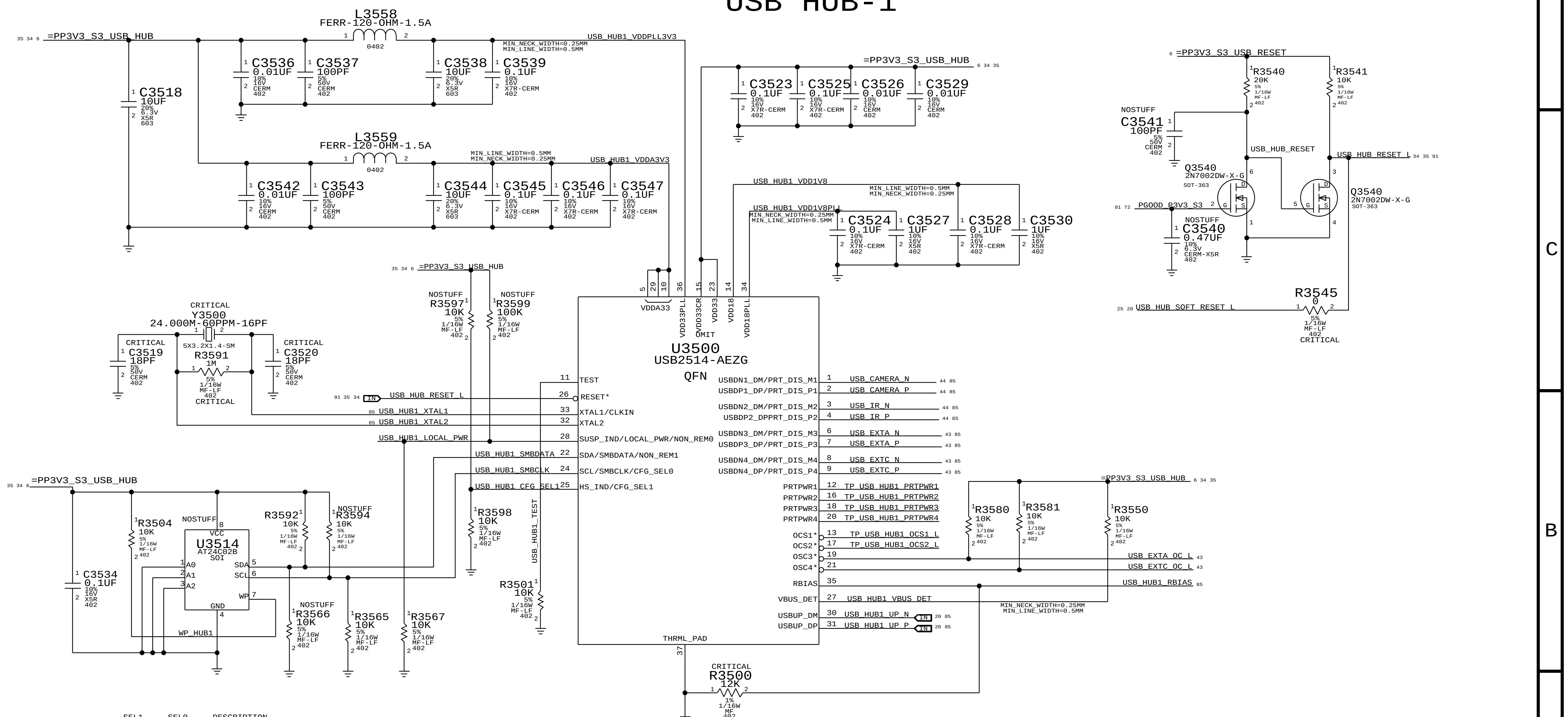
USB HUB-1



	SEL1	SEL0	DESCRIPTION
DEFAULT K23F ==>	0	0	Internal Default with Self powered Operation
	0	1	SMBUS Slave Config
	1	0	Internal Default with Bus powered Operation
	1	1	EEPROM Supported

	NON_REM1	NON_REM0	DESCRIPTION
	0	0	All ports are Non removable
	0	1	Port1 is non removable
DEFAULT K23F ==>	1	0	Port 1 and 2 are non removable
	1	1	Port1,2 and 3 are non Removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	SMSC USB2514	U3500,U3600	CRITICAL	

SYNC_MASTER=K60_AARON SYNC_DATE=07/01/2009

PAGE TITLE
USB HUB 1

Apple Inc.

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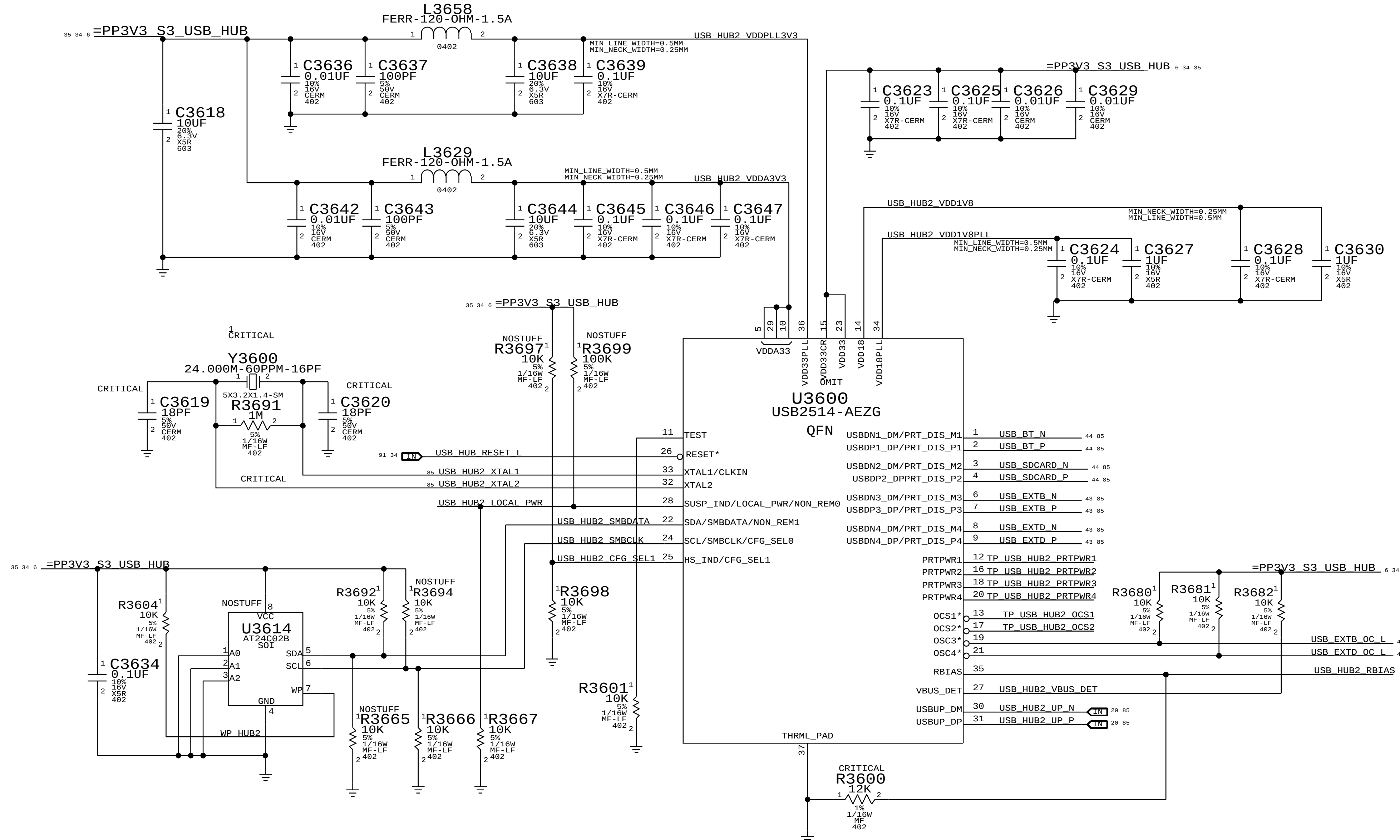
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

USB HUB-2



SYNC_MASTER=K60_AARON SYNC_DATE=07/01/2009

PAGE TITLE

USB HUB 2

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

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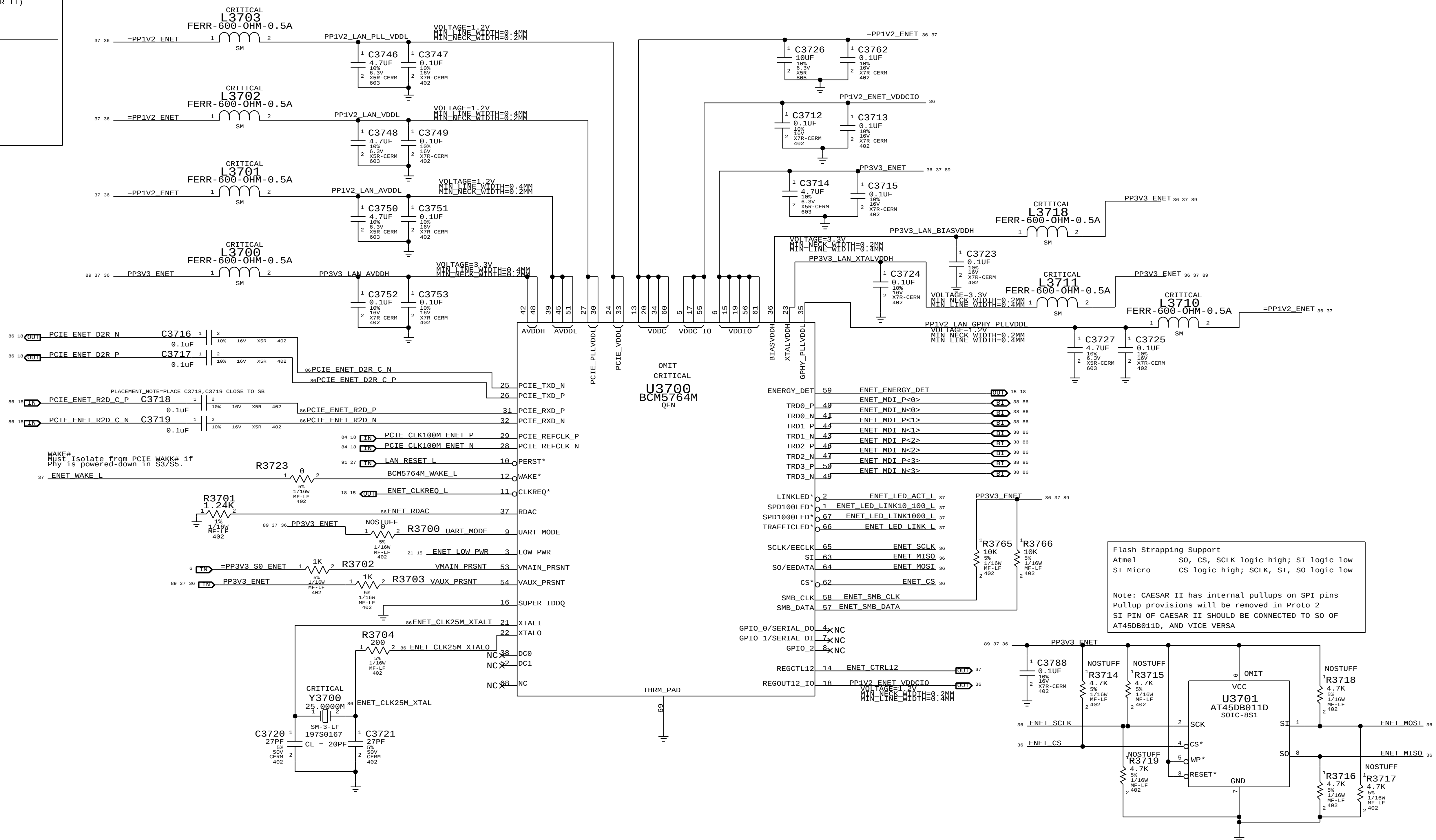
Page Notes

Power aliases required by this page:
- PP3V3_ENET (CAESAR II)
- =PP1V2_ENET



Flash Strapping Support

Atmel	SO, CS, SCLK logic high; SI logic low
ST Micro	CS logic high; SCLK, SI, SO logic low

Note: CAESAR II has internal pullups on SPI pins
Pullup provisions will be removed in Proto 2
SI PIN OF CAESAR II SHOULD BE CONNECTED TO SO OF
AT45DB011D, AND VICE VERSA

SYNC_MASTER=K60_AARON SYNC_DATE=07/01/2009

PAGE TITLE
ETHERNET (CAESAR II)

Apple Inc.

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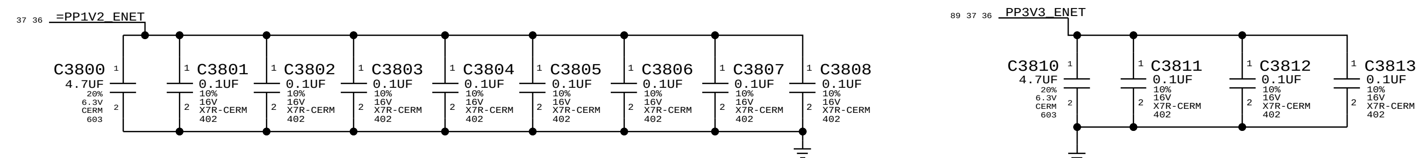
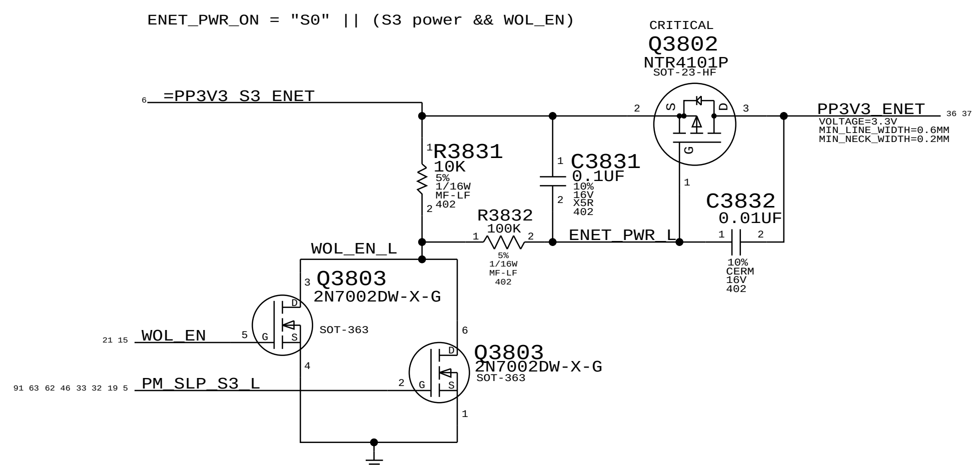
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

CAESAR II DECOUPLING

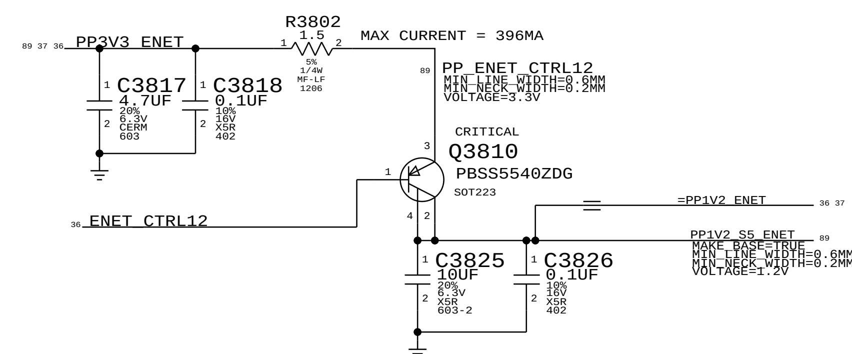


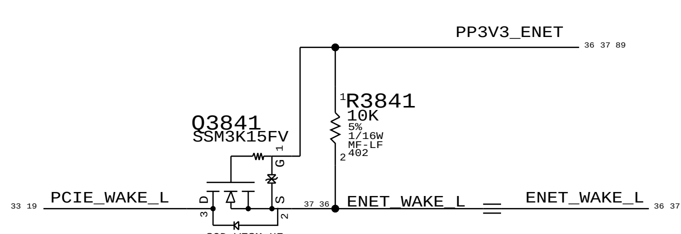
ENET POWER ENABLE CIRCUIT

ENET_PWR_ON = "S0" || (S3 power && WOL_EN)

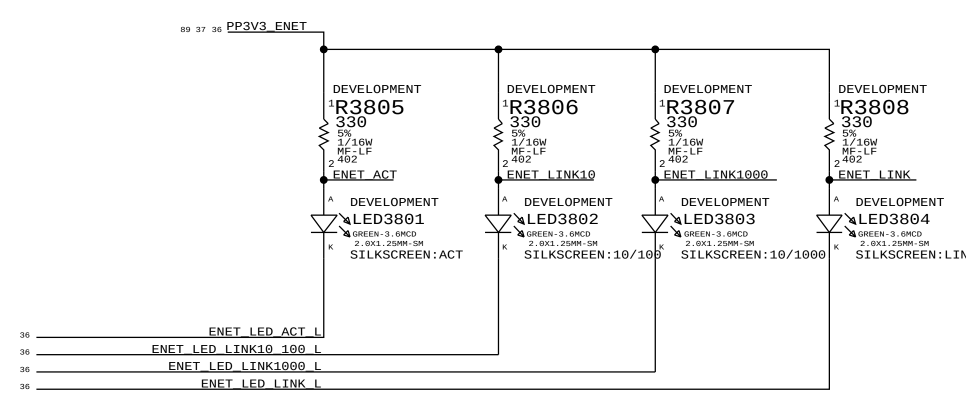


CAESAR II 1V2 RAIL SUPPLY





CAESAR II LED SUPPORT



SYNC_MASTER=K60_AARON SYNC_DATE=07/01/2009

PAGE TITLE: CAESAR II SUPPORT

Apple Inc.

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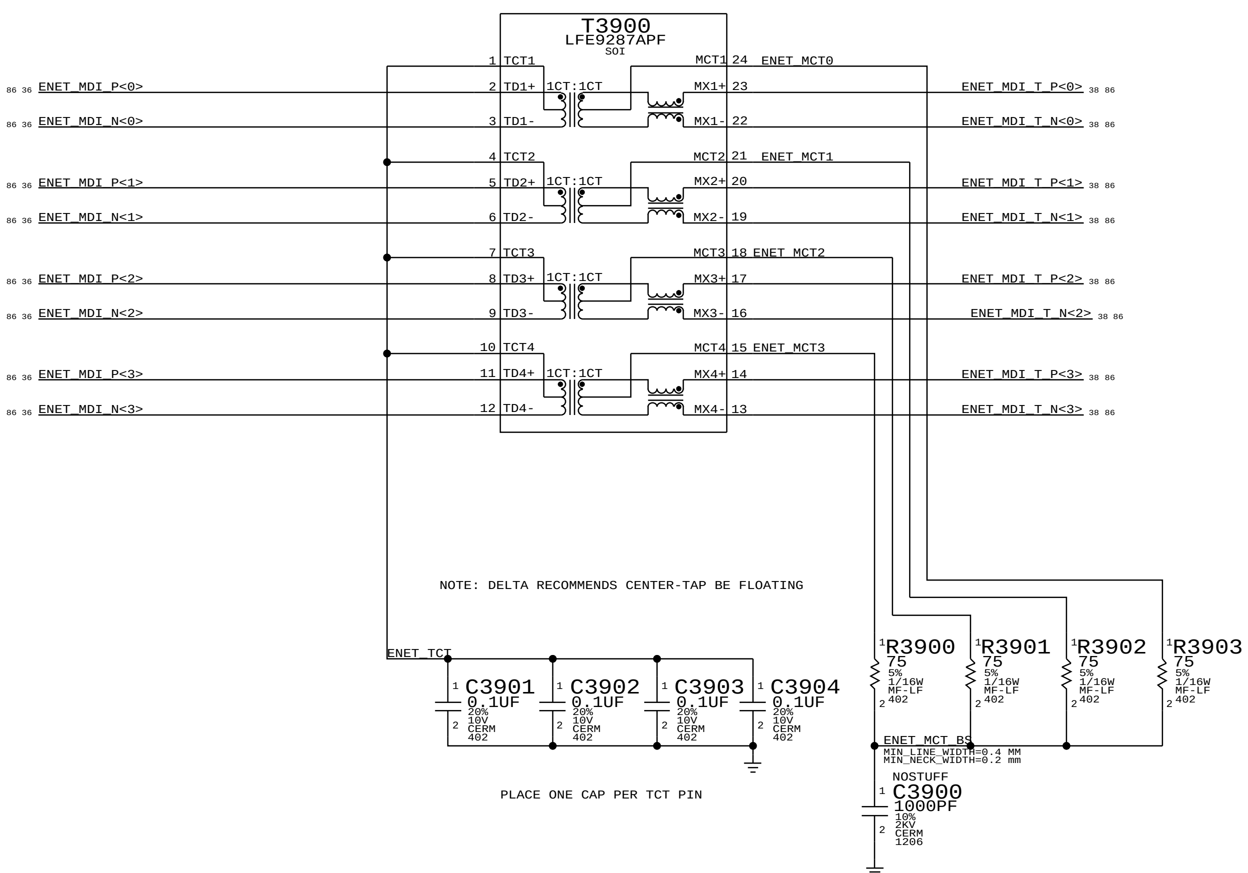
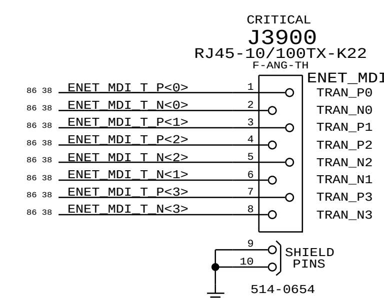
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>





SYNC_MASTER=K60_AARON SYNC_DATE=07/01/2009

PAGE TITLE

ETHERNET CONNECTOR

Apple Inc.

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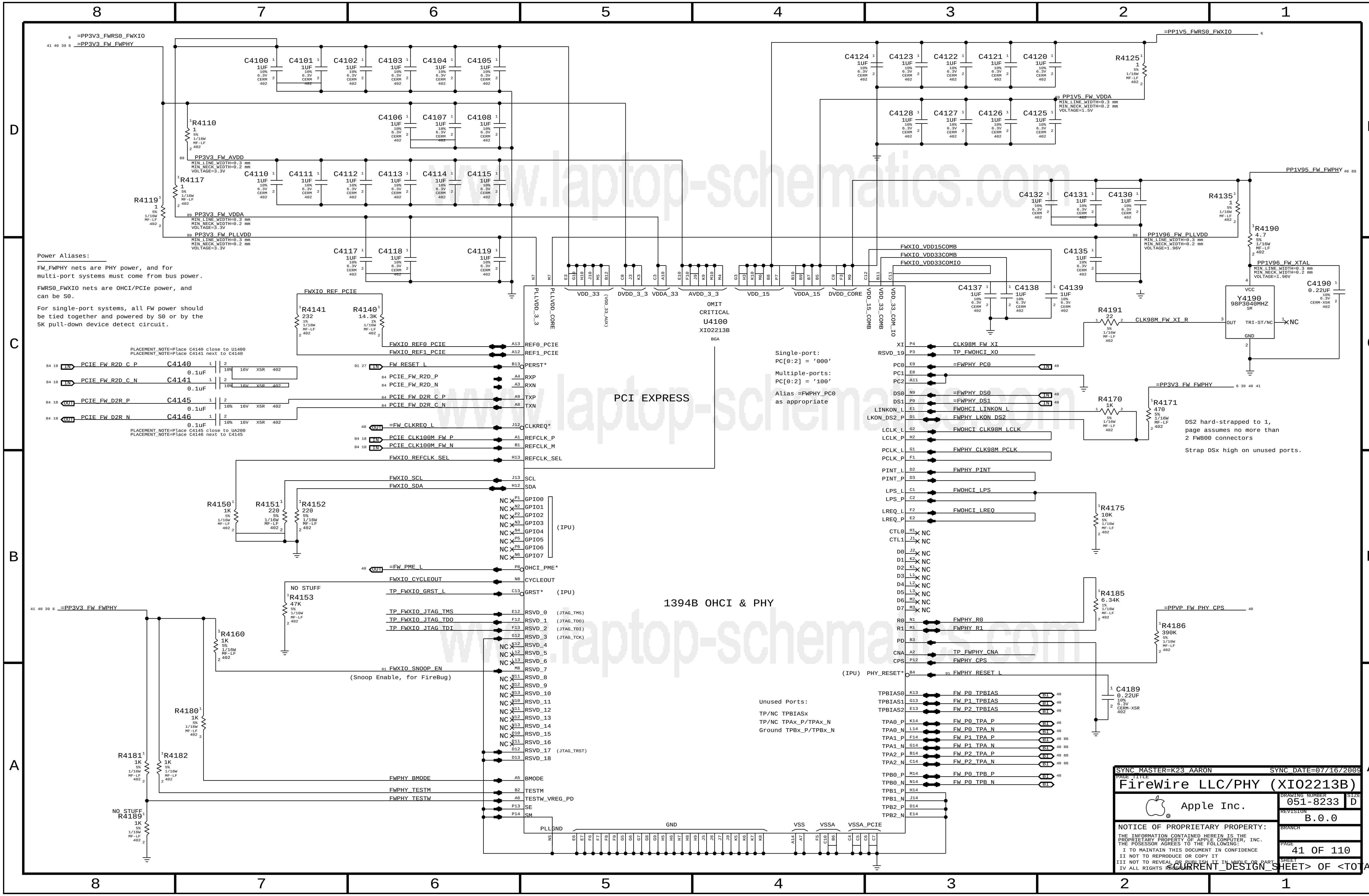
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC_MASTER=K23_AARON SYNC_DATE=07/16/2009

PAGE TITLE

FireWire LLC/PHY (XIO2213B)

Apple Inc.

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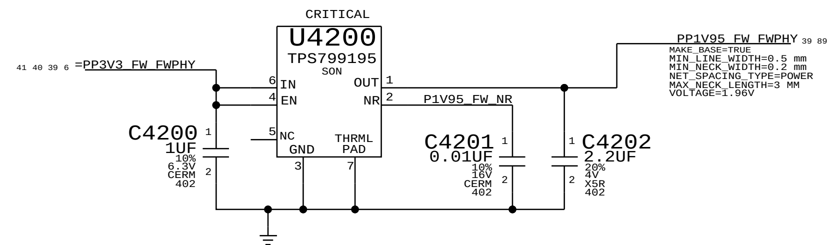
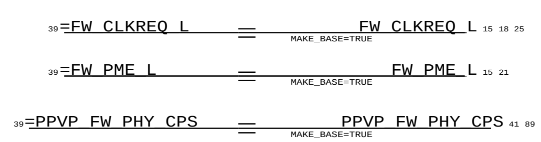
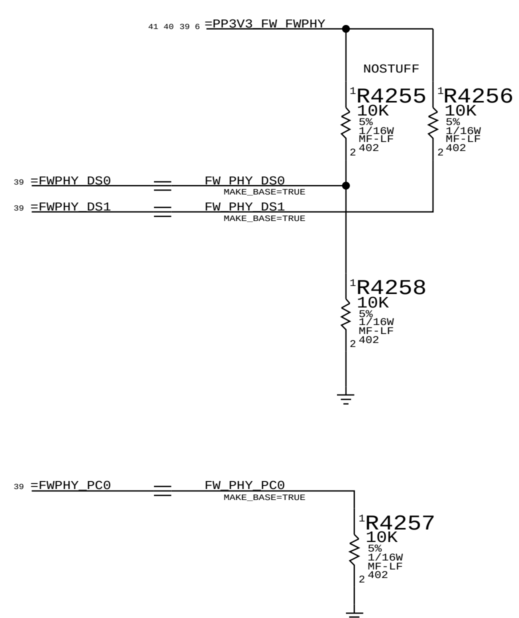
1394 PHY 1.95V SUPPLY



FireWire Aliases For Connectivity



1394 PHY STRAPPING OPTIONS



THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE.

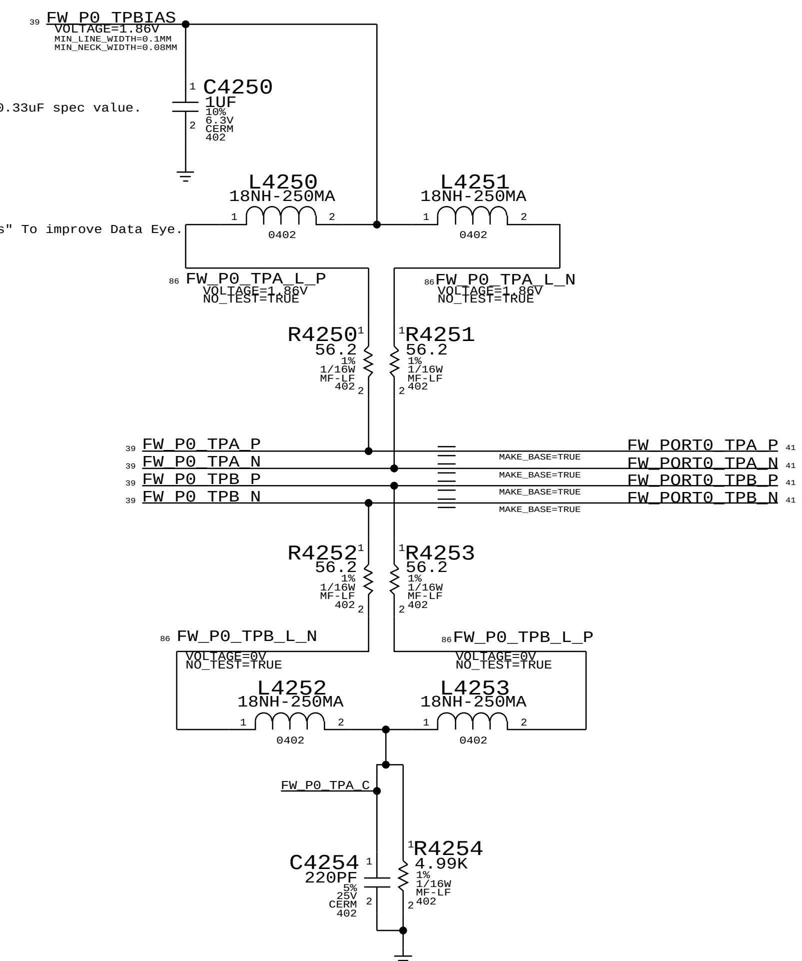
iMacs are now one port only and have Power Code "000"

Termination

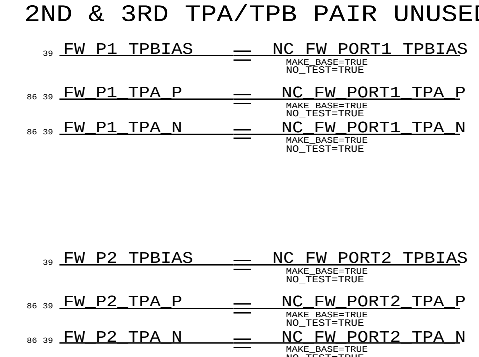
Place close to FireWire PHY

TI PHY requires 1UF, not 0.33uF spec value.

TI PHY "Peaking Inductors" To improve Data Eye.



2ND & 3RD TPA/TPB PAIR UNUSED



SYNC_MASTER=K23_AARON SYNC_DATE=07/16/2009

PAGE TITLE

FW: 1394B MISC

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

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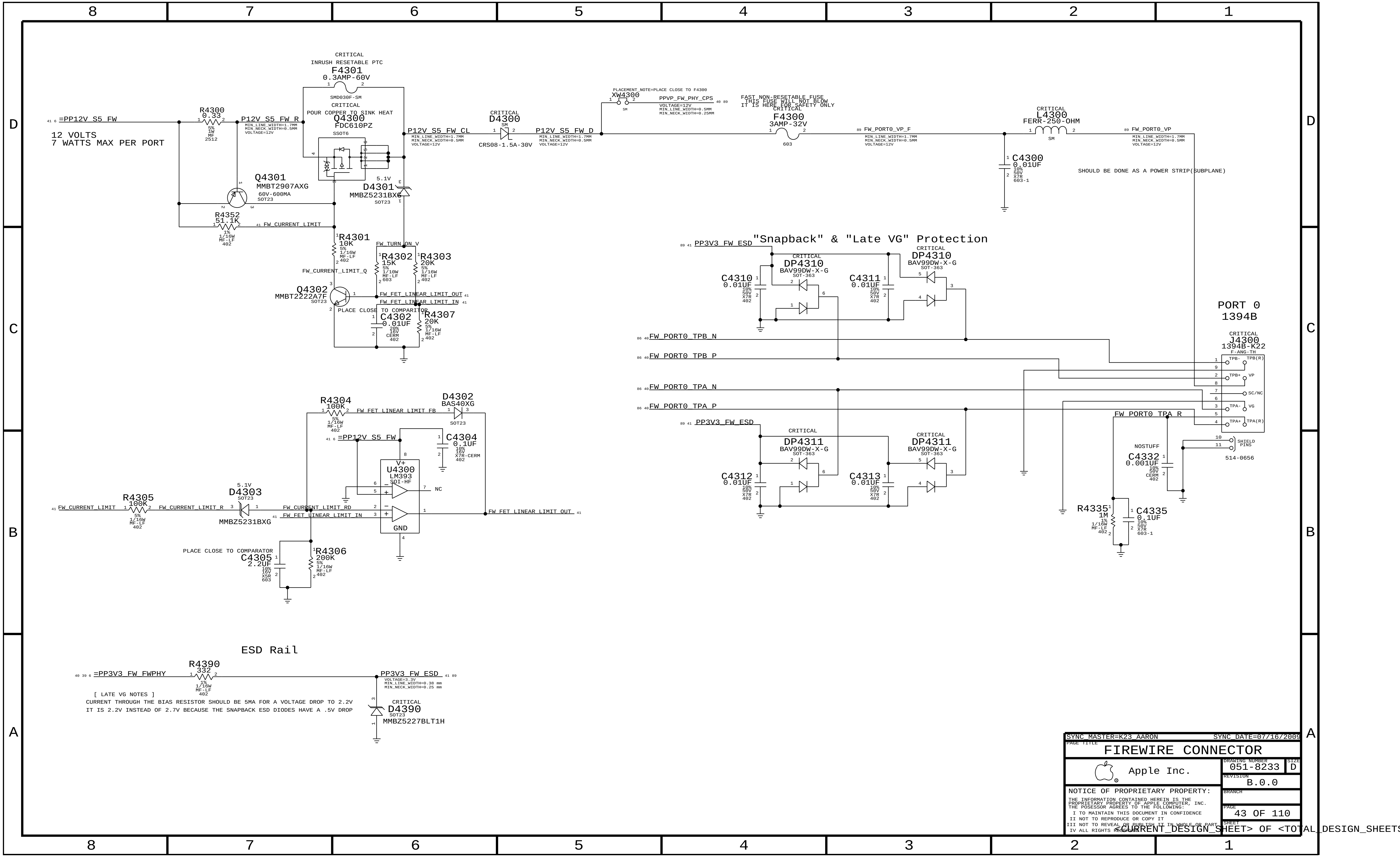

CRITICAL
INRUSH RESETABLE PTC
F4301
0.3AMP-60V
SMD030F-SM
CRITICAL
POUR COPPER TO SINK HEAT
Q4300
FDC610PZ
SSOT6
=PP12V_S5_FW
R4300
0.33
5%
1W
MF
2512
P12V_S5_FW_R
MIN_LINE_WIDTH=1.7MM
MIN_NECK_WIDTH=0.5MM
VOLTAGE=12V
12 VOLTS
7 WATTS MAX PER PORT
Q4301
MMBT2907AXG
60V-600MA
SOT23
R4352
51.1K
1%
1/16W
MF-LF
402
FW_CURRENT_LIMIT
5.1V
D4301
MMBZ5231BXG
SOT23
P12V_S5_FW_CL
CRITICAL
D4300
SM
CRS08-1.5A-30V
P12V_S5_FW_D
PLACEMENT_NOTE=PLACE CLOSE TO F4300
XW4300
SM
PPVP_FW_PHY_CPS
VOLTAGE=12V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
FAST NON-RESETABLE FUSE
THIS FUSE WILL NOT BLOW
IT IS HERE FOR SAFETY ONLY
CRITICAL
F4300
3AMP-32V
603
FW_PORT0_VP_F
CRITICAL
L4300
FERR-250-OHM
SM
FW_PORT0_VP
C4300
0.01UF
10%
50V
X7R
603-1
SHOULD BE DONE AS A POWER STRIP(SUBPLANE)
R4301
10K
5%
1/16W
MF-LF
402
FW_TURN_ON_V
R4302
15K
5%
1/10W
MF-LF
603
R4303
20K
5%
1/16W
MF-LF
402
FW_CURRENT_LIMIT_Q
Q4302
MMBT2222A7F
SOT23
FW_FET_LINEAR_LIMIT_OUT
FW_FET_LINEAR_LIMIT_IN
PLACE CLOSE TO COMPARITOR
C4302
0.01UF
20%
16V
CERM
402
R4307
20K
5%
1/16W
MF-LF
402
"Snapback" & "Late VG" Protection
PP3V3_FW_ESD
CRITICAL
DP4310
BAV99DW-X-G
SOT-363
C4310
0.01UF
C4311
0.01UF
FW_PORT0_TPB_N
FW_PORT0_TPB_P
FW_PORT0_TPA_N
FW_PORT0_TPA_P
PORT 0
1394B
CRITICAL
J4300
1394B-K22
F-ANG-TH
TPB- TPB(R) TPB+ VP SC/NC TPA- VG TPA+ TPA(R)
SHIELD PINS
514-0656
FW_PORT0_TPA_R
NOSTUFF
C4332
0.001UF
10%
50V
CERM
402
R4335
1M
1%
1/16W
MF-LF
402
C4335
0.1UF
10%
50V
X7R
603-1
CRITICAL
DP4311
BAV99DW-X-G
SOT-363
C4312
0.01UF
C4313
0.01UF
R4304
100K
5%
1/16W
MF-LF
402
FW_FET_LINEAR_LIMIT_FB
D4302
BAS40XG
SOT23
=PP12V_S5_FW
C4304
0.1UF
10%
16V
X7R-CERM
402
V+
U4300
LM393
SOI-HF
NC
GND
R4305
100K
5%
1/16W
MF-LF
402
FW_CURRENT_LIMIT
FW_CURRENT_LIMIT_R
5.1V
D4303
SOT23
MMBZ5231BXG
FW_CURRENT_LIMIT_RD
FW_FET_LINEAR_LIMIT_IN
FW_FET_LINEAR_LIMIT_OUT
PLACE CLOSE TO COMPARATOR
C4305
2.2UF
10%
16V
X5R
603
R4306
200K
5%
1/16W
MF-LF
402
ESD Rail
=PP3V3_FW_FWPHY
R4390
332
1%
1/16W
MF-LF
402
PP3V3_FW_ESD
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
CRITICAL
D4390
SOT23
MMBZ5227BLT1H
[LATE VG NOTES]
CURRENT THROUGH THE BIAS RESISTOR SHOULD BE 5MA FOR A VOLTAGE DROP TO 2.2V
IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A .5V DROP
SYNC_MASTER=K23_AARON
SYNC_DATE=07/16/2009
PAGE TITLE
FIREWIRE CONNECTOR
Apple Inc.
DRAWING NUMBER
051-8233
SIZE
D
REVISION
B.0.0
BRANCH
PAGE
43 OF 110
SHEET
<CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>
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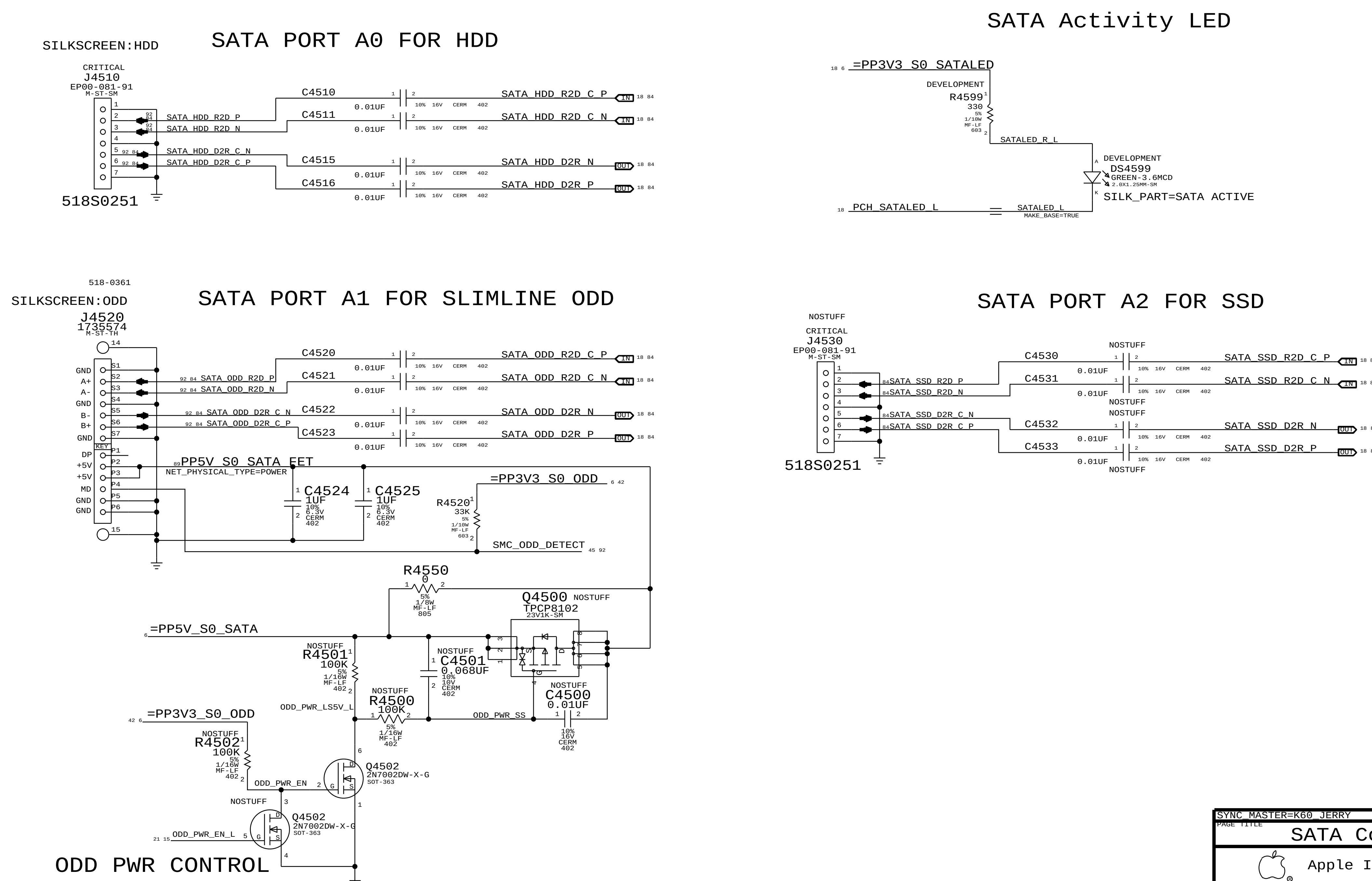

SYNC_MASTER=K60_JERRY SYNC_DATE=07/01/2009

PAGE TITLE

SATA Connectors

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

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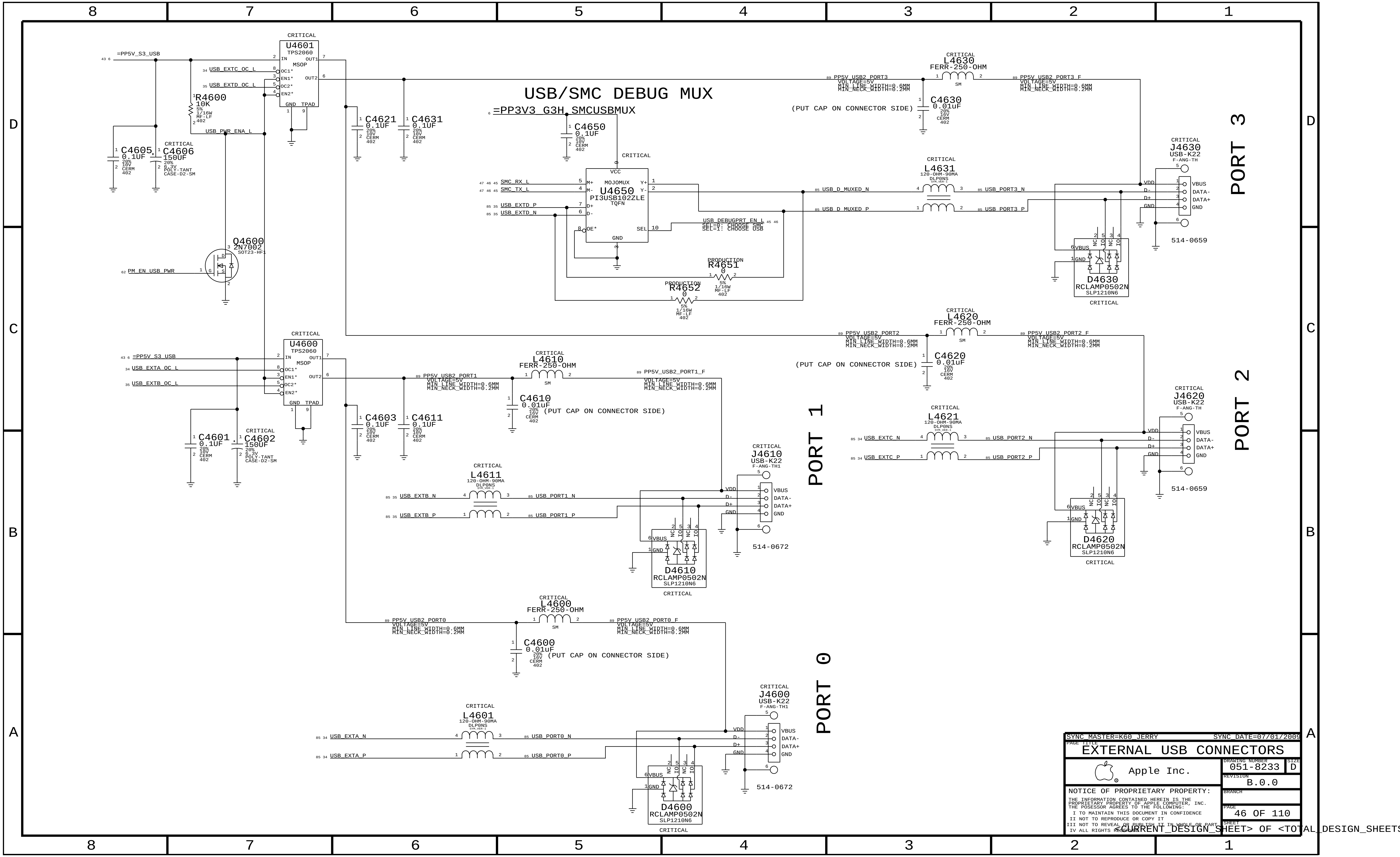
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



USB/SMC DEBUG MUX
=PP3V3_G3H_SMCUSBMUX
=PP5V_S3_USB
U4601
TPS2060
MSOP
CRITICAL
USB_EXTC_OC_L
USB_EXTD_OC_L
USB_PWR_ENA_L
R4600
10K
5%
1/16W
MF-LF
402
C4605
0.1UF
C4606
150UF
20%
6.3V
POLY-TANT
CASE-D2-SM
Q4600
2N7002
SOT23-HF1
PM_EN_USB_PWR
C4621
0.1UF
C4631
0.1UF
C4650
0.1UF
U4650
MOJOMUX
PI3USB102ZLE
TQFN
SMC_RX_L
SMC_TX_L
USB_EXTD_P
USB_EXTD_N
USB_D_MUXED_N
USB_D_MUXED_P
USB_DEBUGPRT_EN_L
SEL=0: CHOOSE SMC
SEL=1: CHOOSE USB
PRODUCTION
R4651
R4652
PP5V_USB2_PORT3
L4630
FERR-250-OHM
PP5V_USB2_PORT3_F
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
C4630
0.01UF
(PUT CAP ON CONNECTOR SIDE)
L4631
120-OHM-90MA
DLP0NS
USB_PORT3_N
USB_PORT3_P
J4630
USB-K22
F-ANG-TH
VBUS
DATA-
DATA+
GND
514-0659
D4630
RCLAMP0502N
SLP1210N6
PORT 3
PP5V_USB2_PORT2
L4620
FERR-250-OHM
PP5V_USB2_PORT2_F
C4620
0.01UF
L4621
USB_EXTC_N
USB_EXTC_P
USB_PORT2_N
USB_PORT2_P
J4620
D4620
PORT 2
U4600
TPS2060
=PP5V_S3_USB
USB_EXTA_OC_L
USB_EXTB_OC_L
C4601
0.1UF
C4602
150UF
C4603
0.1UF
C4611
0.1UF
PP5V_USB2_PORT1
L4610
FERR-250-OHM
PP5V_USB2_PORT1_F
C4610
0.01UF
L4611
USB_EXTB_N
USB_EXTB_P
USB_PORT1_N
USB_PORT1_P
J4610
514-0672
D4610
PORT 1
PP5V_USB2_PORT0
L4600
FERR-250-OHM
PP5V_USB2_PORT0_F
C4600
0.01UF
L4601
USB_EXTA_N
USB_EXTA_P
USB_PORT0_N
USB_PORT0_P
J4600
D4600
PORT 0
SYNC_MASTER=K60_JERRY
SYNC_DATE=07/01/2009
PAGE TITLE
EXTERNAL USB CONNECTORS
Apple Inc.
DRAWING NUMBER
051-8233
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REVISION
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SHEET
<CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>
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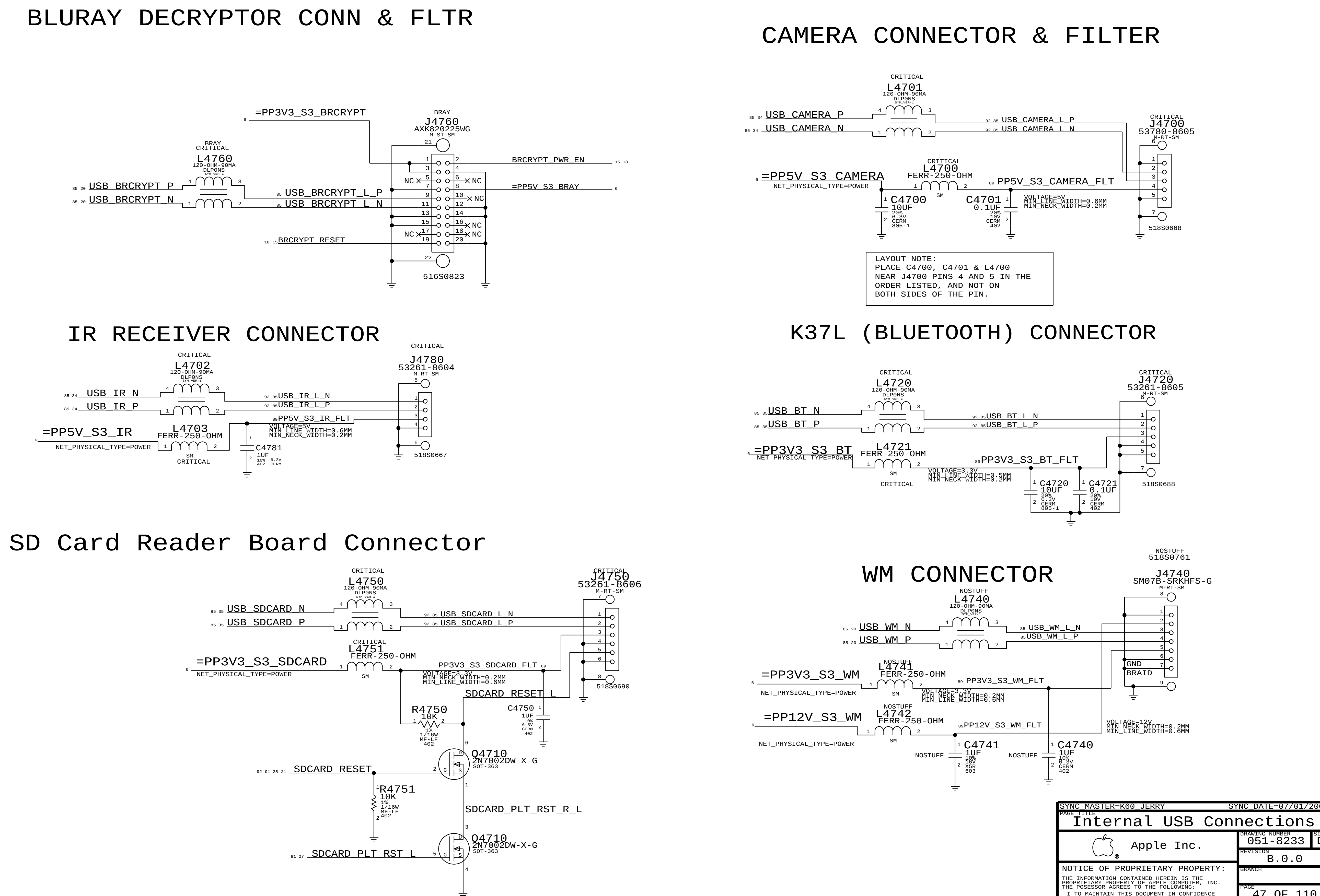

SYNC_MASTER=K60_JERRY SYNC_DATE=07/01/2009

PAGE TITLE

Internal USB Connections

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

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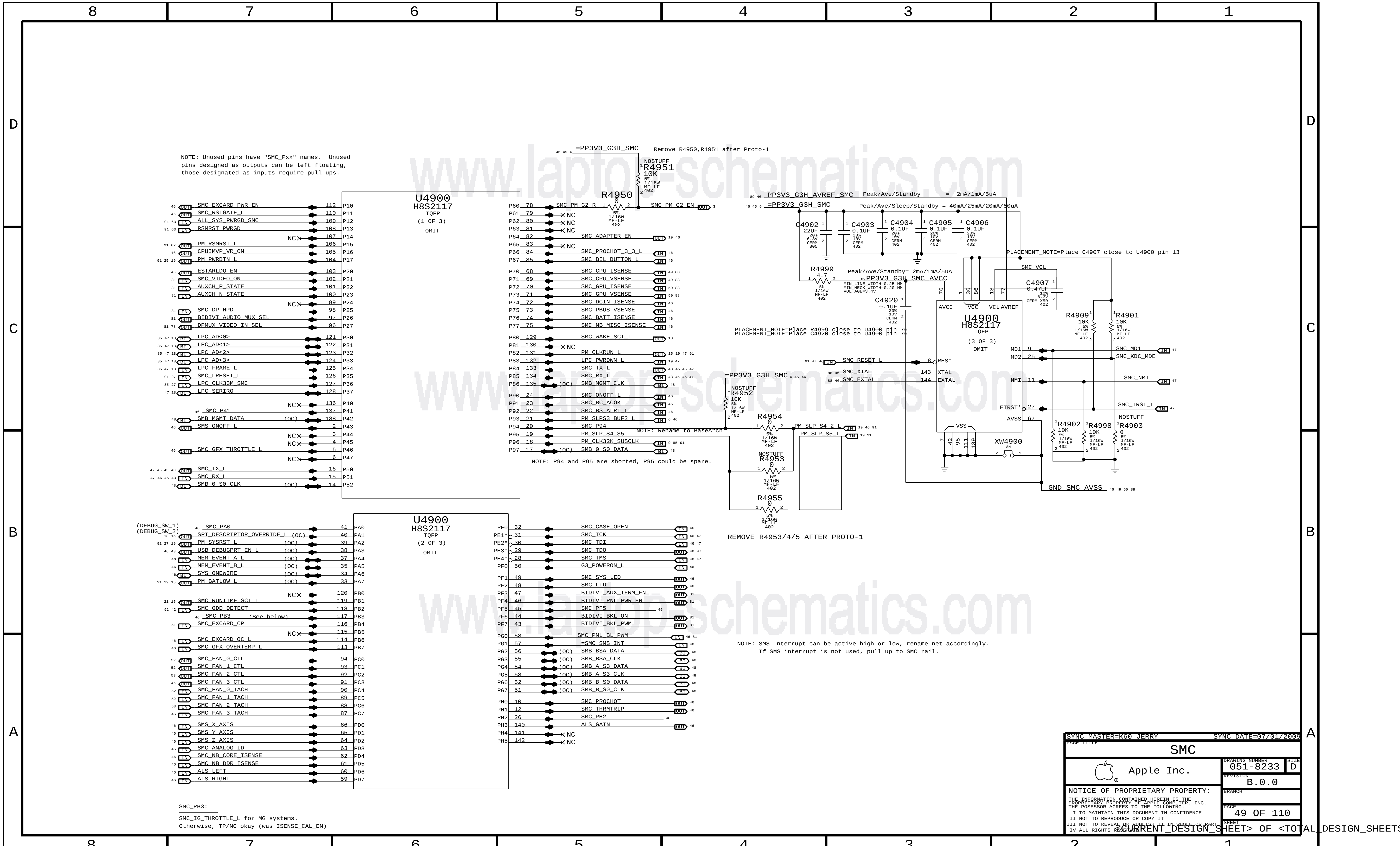

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.
=PP3V3_G3H_SMC
Remove R4950,R4951 after Proto-1
NOSTUFF
R4951
10K
5%
1/16W
MF-LF
402
R4950
0
SMC_PM_G2_EN
U4900
H8S2117
TQFP
(1 OF 3)
OMIT
SMC_EXCARD_PWR_EN
SMC_RSTGATE_L
ALL_SYS_PWRGD_SMC
RSMRST_PWRGD
PM_RSMRST_L
CPUIMVP_VR_ON
PM_PWRBTN_L
ESTARLDO_EN
SMC_VIDEO_ON
AUXCH_P_STATE
AUXCH_N_STATE
SMC_DP_HPD
BIDIVI_AUDIO_MUX_SEL
DPMUX_VIDEO_IN_SEL
LPC_AD<0>
LPC_AD<1>
LPC_AD<2>
LPC_AD<3>
LPC_FRAME_L
SMC_LRESET_L
LPC_CLK33M_SMC
LPC_SERIRQ
SMC_P41
SMB_MGMT_DATA
SMS_ONOFF_L
SMC_GFX_THROTTLE_L
SMC_TX_L
SMC_RX_L
SMB_0_S0_CLK
SMC_PM_G2_R
SMC_ADAPTER_EN
SMC_PROCHOT_3_3_L
SMC_BIL_BUTTON_L
SMC_CPU_ISENSE
SMC_CPU_VSENSE
SMC_GPU_ISENSE
SMC_GPU_VSENSE
SMC_DCIN_ISENSE
SMC_PBUS_VSENSE
SMC_BATT_ISENSE
SMC_NB_MISC_ISENSE
SMC_WAKE_SCI_L
PM_CLKRUN_L
LPC_PWRDWN_L
SMC_TX_L
SMC_RX_L
SMB_MGMT_CLK
SMC_ONOFF_L
SMC_BC_ACOK
SMC_BS_ALRT_L
PM_SLPS3_BUF2_L
SMC_P94
PM_SLP_S4_S5
PM_CLK32K_SUSCLK
SMB_0_S0_DATA
NOTE: Rename to BaseArch
NOTE: P94 and P95 are shorted, P95 could be spare.
=PP3V3_G3H_SMC
NOSTUFF
R4952
10K
R4954
0
PM_SLP_S4_2_L
PM_SLP_S5_L
NOSTUFF
R4953
0
R4955
0
REMOVE R4953/4/5 AFTER PROTO-1
PP3V3_G3H_AVREF_SMC
Peak/Ave/Standby = 2mA/1mA/5uA
=PP3V3_G3H_SMC
Peak/Ave/Sleep/Standby = 40mA/25mA/20mA/50uA
C4902
22UF
C4903
0.1UF
C4904
0.1UF
C4905
0.1UF
C4906
0.1UF
PLACEMENT_NOTE=Place C4907 close to U4900 pin 13
SMC_VCL
C4907
0.47UF
R4999
4.7
Peak/Ave/Standby= 2mA/1mA/5uA
PP3V3_G3H_SMC_AVCC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.4V
C4920
0.1UF
PLACEMENT_NOTE=Place R4999 close to U4900 pin 76
PLACEMENT_NOTE=Place C4920 close to U4900 pin 76
U4900
H8S2117
TQFP
(3 OF 3)
OMIT
AVCC
VCC
VCL
AVREF
MD1
MD2
RES*
XTAL
EXTAL
NMI
ETRST*
AVSS
VSS
R4909
10K
R4901
10K
SMC_MD1
SMC_KBC_MDE
SMC_RESET_L
SMC_XTAL
SMC_EXTAL
SMC_NMI
SMC_TRST_L
NOSTUFF
R4902
10K
R4998
10K
R4903
0
XW4900
GND_SMC_AVSS
(DEBUG_SW_1)
(DEBUG_SW_2)
U4900
H8S2117
TQFP
(2 OF 3)
OMIT
SMC_PA0
SPI_DESCRIPTOR_OVERRIDE_L
PM_SYSRST_L
USB_DEBUGPRT_EN_L
MEM_EVENT_A_L
MEM_EVENT_B_L
SYS_ONEWIRE
PM_BATLOW_L
SMC_RUNTIME_SCI_L
SMC_ODD_DETECT
SMC_PB3
(See below)
SMC_EXCARD_CP
SMC_EXCARD_OC_L
SMC_GFX_OVERTEMP_L
SMC_FAN_0_CTL
SMC_FAN_1_CTL
SMC_FAN_2_CTL
SMC_FAN_3_CTL
SMC_FAN_0_TACH
SMC_FAN_1_TACH
SMC_FAN_2_TACH
SMC_FAN_3_TACH
SMS_X_AXIS
SMS_Y_AXIS
SMS_Z_AXIS
SMC_ANALOG_ID
SMC_NB_CORE_ISENSE
SMC_NB_DDR_ISENSE
ALS_LEFT
ALS_RIGHT
SMC_CASE_OPEN
SMC_TCK
SMC_TDI
SMC_TDO
SMC_TMS
G3_POWERON_L
SMC_SYS_LED
SMC_LID
BIDIVI_AUX_TERM_EN
BIDIVI_PNL_PWR_EN
SMC_PF5
BIDIVI_BKL_ON
BIDIVI_BKL_PWM
SMC_PNL_BL_PWM
=SMC_SMS_INT
SMB_BSA_DATA
SMB_BSA_CLK
SMB_A_S3_DATA
SMB_A_S3_CLK
SMB_B_S0_DATA
SMB_B_S0_CLK
SMC_PROCHOT
SMC_THRMTRIP
SMC_PH2
ALS_GAIN
NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.
SMC_PB3:
SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)
SYNC_MASTER=K60_JERRY
SYNC_DATE=07/01/2009
PAGE TITLE
SMC
Apple Inc.
DRAWING NUMBER
051-8233
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SHEET
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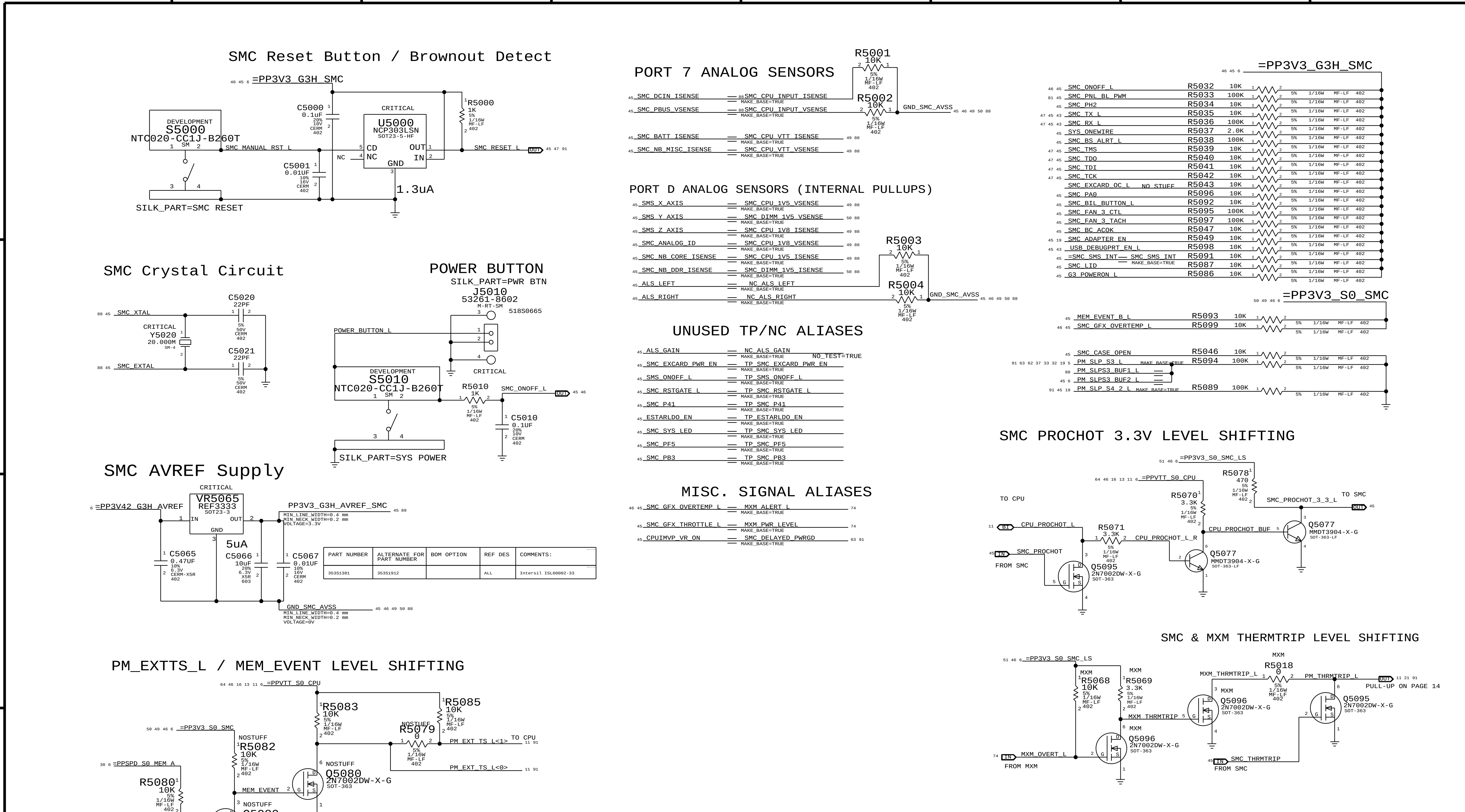


SYNC_MASTER=K60_JERRY SYNC_DATE=07/01/2009

PAGE TITLE

SMC Support

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

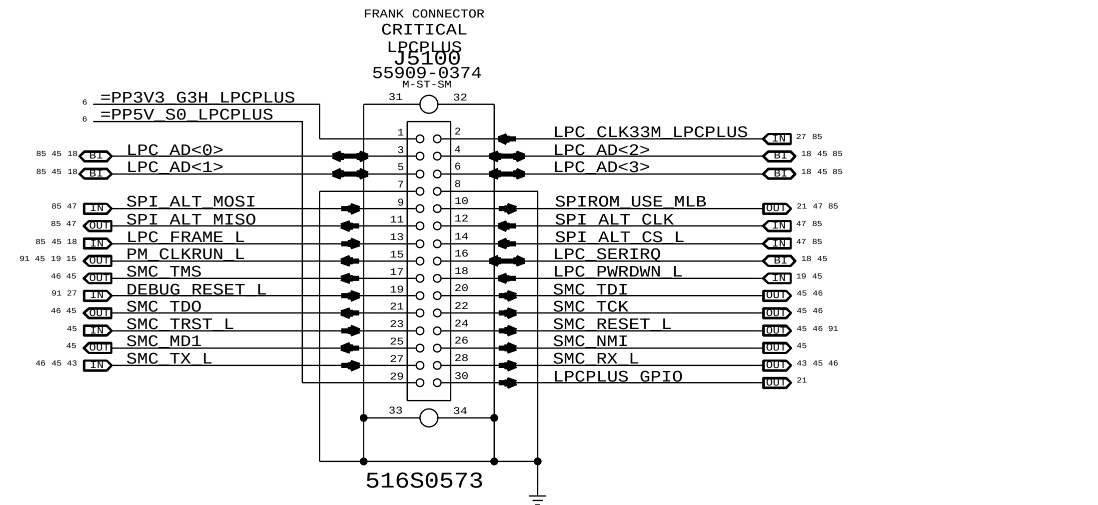
REVISION B.0.0

BRANCH

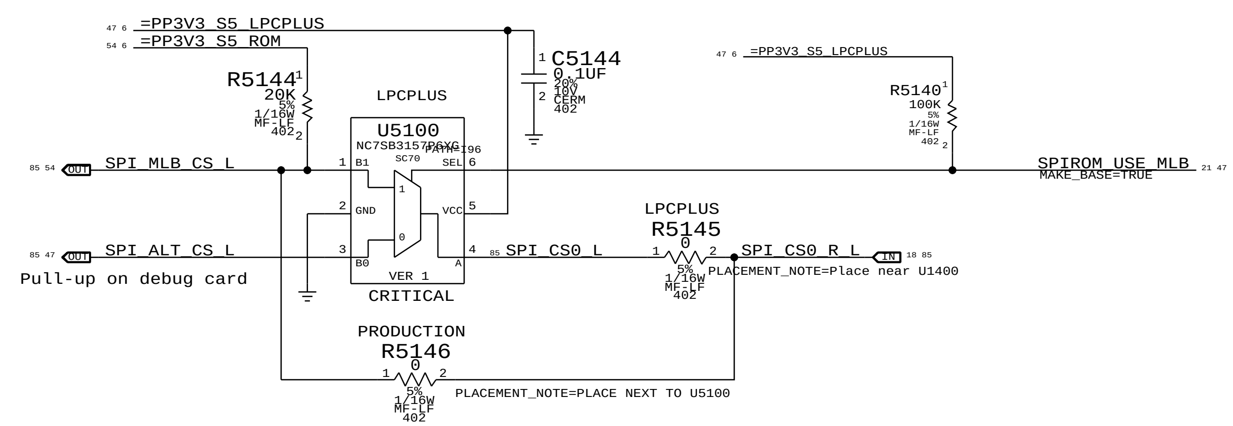
PAGE 50 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

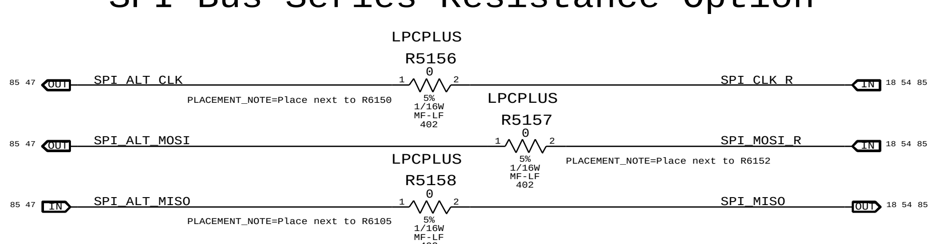
LPC+SPI Connector



Alternate SPI ROM Support



SPI Bus Series Resistance Option



SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE

LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

REVISION B.0.0

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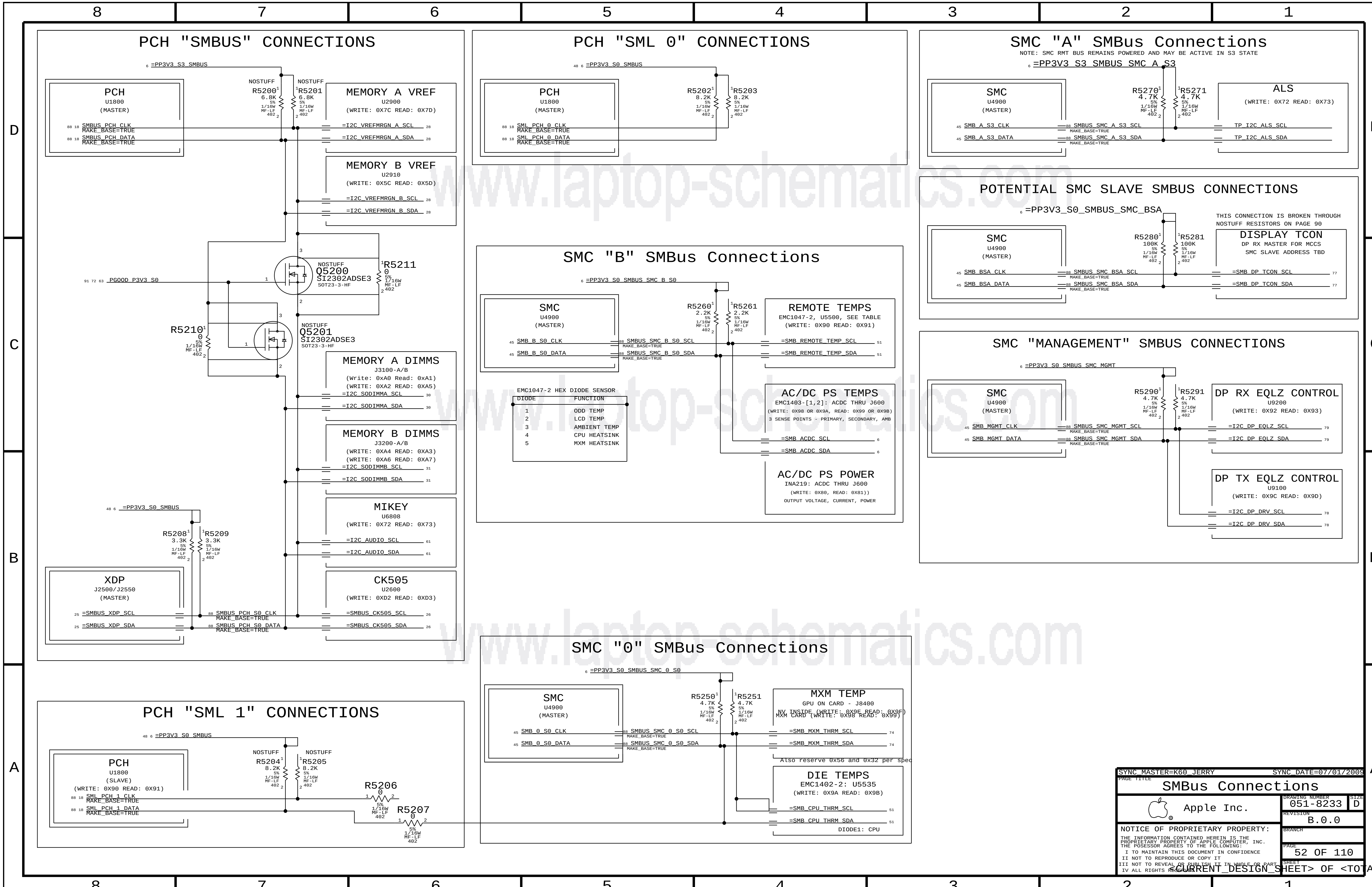
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>


PCH "SMBUS" CONNECTIONS
=PP3V3_S3_SMBUS
PCH
U1800
(MASTER)
SMBUS_PCH_CLK
MAKE_BASE=TRUE
SMBUS_PCH_DATA
MAKE_BASE=TRUE
NOSTUFF
R5200
6.8K
R5201
6.8K
5%
1/16W
MF-LF
402
MEMORY A VREF
U2900
(WRITE: 0X7C READ: 0X7D)
=I2C_VREFMRGN_A_SCL
=I2C_VREFMRGN_A_SDA
MEMORY B VREF
U2910
(WRITE: 0X5C READ: 0X5D)
=I2C_VREFMRGN_B_SCL
=I2C_VREFMRGN_B_SDA
PGOOD_P3V3_S0
Q5200
SI2302ADSE3
SOT23-3-HF
R5211
0
Q5201
SI2302ADSE3
SOT23-3-HF
R5210
0
MEMORY A DIMMS
J3100-A/B
(Write: 0XA0 Read: 0XA1)
(WRITE: 0XA2 READ: 0XA5)
=I2C_SODIMMA_SCL
=I2C_SODIMMA_SDA
MEMORY B DIMMS
J3200-A/B
(WRITE: 0XA4 READ: 0XA3)
(WRITE: 0XA6 READ: 0XA7)
=I2C_SODIMMB_SCL
=I2C_SODIMMB_SDA
MIKEY
U6808
(WRITE: 0X72 READ: 0X73)
=I2C_AUDIO_SCL
=I2C_AUDIO_SDA
=PP3V3_S0_SMBUS
R5208
3.3K
R5209
3.3K
XDP
J2500/J2550
(MASTER)
=SMBUS_XDP_SCL
=SMBUS_XDP_SDA
SMBUS_PCH_S0_CLK
MAKE_BASE=TRUE
SMBUS_PCH_S0_DATA
MAKE_BASE=TRUE
CK505
U2600
(WRITE: 0XD2 READ: 0XD3)
=SMBUS_CK505_SCL
=SMBUS_CK505_SDA
PCH "SML 0" CONNECTIONS
=PP3V3_S0_SMBUS
PCH
U1800
(MASTER)
SML_PCH_0_CLK
MAKE_BASE=TRUE
SML_PCH_0_DATA
MAKE_BASE=TRUE
R5202
8.2K
R5203
8.2K
SMC "B" SMBus Connections
=PP3V3_S0_SMBUS_SMC_B_S0
SMC
U4900
(MASTER)
SMB_B_S0_CLK
SMB_B_S0_DATA
SMBUS_SMC_B_S0_SCL
MAKE_BASE=TRUE
SMBUS_SMC_B_S0_SDA
MAKE_BASE=TRUE
R5260
2.2K
R5261
2.2K
REMOTE TEMPS
EMC1047-2, U5500, SEE TABLE
(WRITE: 0X90 READ: 0X91)
=SMB_REMOTE_TEMP_SCL
=SMB_REMOTE_TEMP_SDA
EMC1047-2 HEX DIODE SENSOR
DIODE FUNCTION
1 ODD TEMP
2 LCD TEMP
3 AMBIENT TEMP
4 CPU HEATSINK
5 MXM HEATSINK
AC/DC PS TEMPS
EMC1403-[1,2]: ACDC THRU J600
(WRITE: 0X98 OR 0X9A, READ: 0X99 OR 0X9B)
3 SENSE POINTS - PRIMARY, SECONDARY, AMB
=SMB_ACDC_SCL
=SMB_ACDC_SDA
AC/DC PS POWER
INA219: ACDC THRU J600
(WRITE: 0X80, READ: 0X81)
OUTPUT VOLTAGE, CURRENT, POWER
SMC "A" SMBus Connections
NOTE: SMC RMT BUS REMAINS POWERED AND MAY BE ACTIVE IN S3 STATE
=PP3V3_S3_SMBUS_SMC_A_S3
SMC
U4900
(MASTER)
SMB_A_S3_CLK
SMB_A_S3_DATA
SMBUS_SMC_A_S3_SCL
MAKE_BASE=TRUE
SMBUS_SMC_A_S3_SDA
MAKE_BASE=TRUE
R5270
4.7K
R5271
4.7K
ALS
(WRITE: 0X72 READ: 0X73)
TP_I2C_ALS_SCL
TP_I2C_ALS_SDA
POTENTIAL SMC SLAVE SMBUS CONNECTIONS
=PP3V3_S0_SMBUS_SMC_BSA
THIS CONNECTION IS BROKEN THROUGH
NOSTUFF RESISTORS ON PAGE 90
SMC
U4900
(MASTER)
SMB_BSA_CLK
SMB_BSA_DATA
SMBUS_SMC_BSA_SCL
MAKE_BASE=TRUE
SMBUS_SMC_BSA_SDA
MAKE_BASE=TRUE
R5280
100K
R5281
100K
DISPLAY TCON
DP RX MASTER FOR MCCS
SMC SLAVE ADDRESS TBD
=SMB_DP_TCON_SCL
=SMB_DP_TCON_SDA
SMC "MANAGEMENT" SMBUS CONNECTIONS
=PP3V3_S0_SMBUS_SMC_MGMT
SMC
U4900
(MASTER)
SMB_MGMT_CLK
SMB_MGMT_DATA
SMBUS_SMC_MGMT_SCL
MAKE_BASE=TRUE
SMBUS_SMC_MGMT_SDA
MAKE_BASE=TRUE
R5290
4.7K
R5291
4.7K
DP RX EQLZ CONTROL
U9200
(WRITE: 0X92 READ: 0X93)
=I2C_DP_EQLZ_SCL
=I2C_DP_EQLZ_SDA
DP TX EQLZ CONTROL
U9100
(WRITE: 0X9C READ: 0X9D)
=I2C_DP_DRV_SCL
=I2C_DP_DRV_SDA
PCH "SML 1" CONNECTIONS
=PP3V3_S0_SMBUS
PCH
U1800
(SLAVE)
(WRITE: 0X90 READ: 0X91)
SML_PCH_1_CLK
MAKE_BASE=TRUE
SML_PCH_1_DATA
MAKE_BASE=TRUE
NOSTUFF
R5204
8.2K
R5205
8.2K
R5206
0
R5207
0
SMC "0" SMBus Connections
=PP3V3_S0_SMBUS_SMC_0_S0
SMC
U4900
(MASTER)
SMB_0_S0_CLK
SMB_0_S0_DATA
SMBUS_SMC_0_S0_SCL
MAKE_BASE=TRUE
SMBUS_SMC_0_S0_SDA
MAKE_BASE=TRUE
R5250
4.7K
R5251
4.7K
MXM TEMP
GPU ON CARD - J8400
NV INSIDE (WRITE: 0X9E READ: 0X9F)
MXM CARD (WRITE: 0X98 READ: 0X99)
=SMB_MXM_THRM_SCL
=SMB_MXM_THRM_SDA
Also reserve 0x56 and 0x32 per spec
DIE TEMPS
EMC1402-2: U5535
(WRITE: 0X9A READ: 0X9B)
=SMB_CPU_THRM_SCL
=SMB_CPU_THRM_SDA
DIODE1: CPU
SYNC_MASTER=K60_JERRY
SYNC_DATE=07/01/2009
PAGE TITLE
SMBus Connections
Apple Inc.
DRAWING NUMBER
051-8233
SIZE
D
REVISION
B.0.0
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PAGE
52 OF 110
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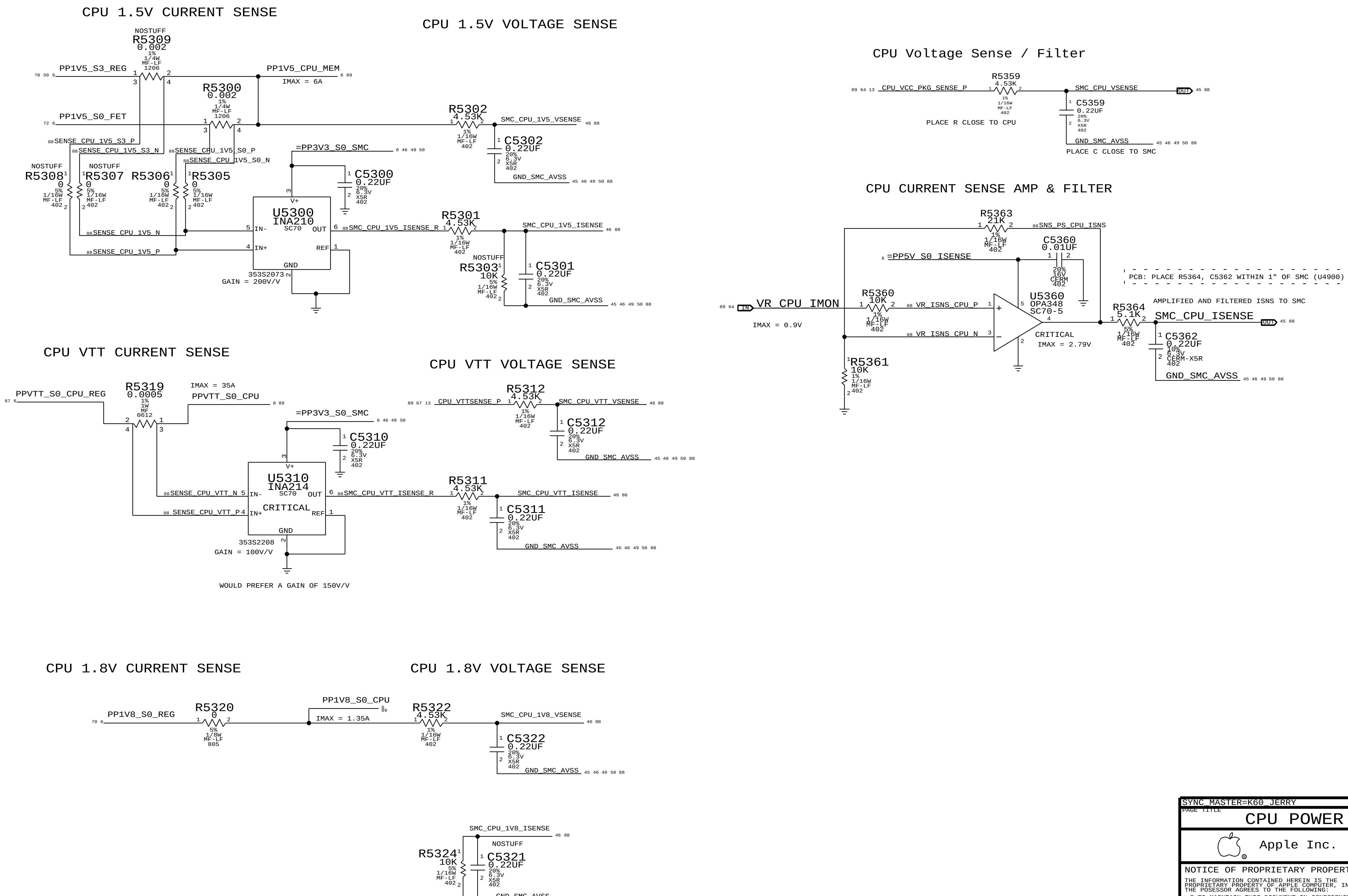

SYNC_MASTER=K60_JERRY SYNC_DATE=07/01/2009

PAGE TITLE

CPU POWER SENSE

Apple Inc.

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051-8233	D

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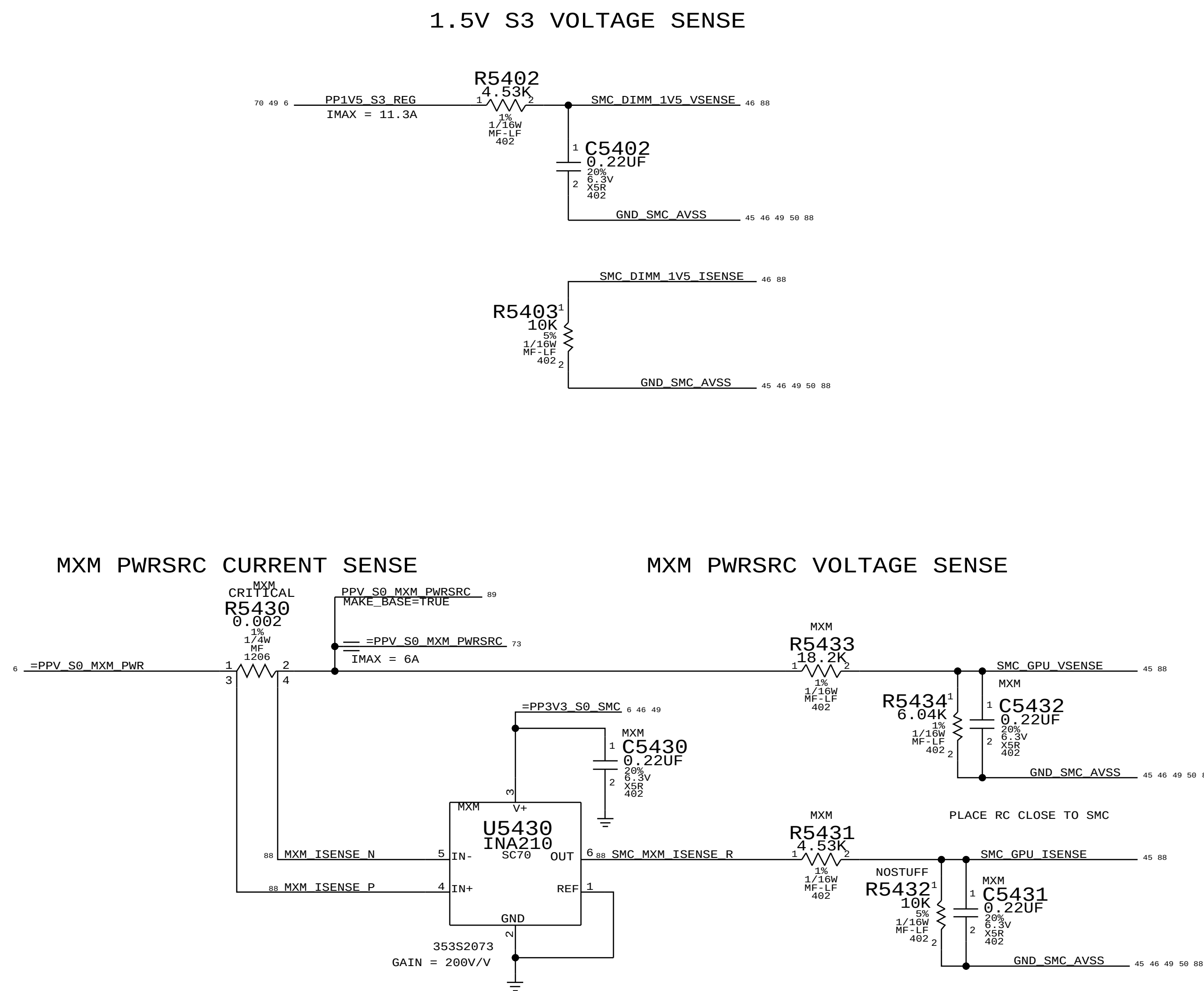
PAGE 53 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC_MASTER=K60_JERRY SYNC_DATE=07/01/2009

PAGE TITLE

GRAPHICS / DIMM POWER SENSE

Apple Inc.

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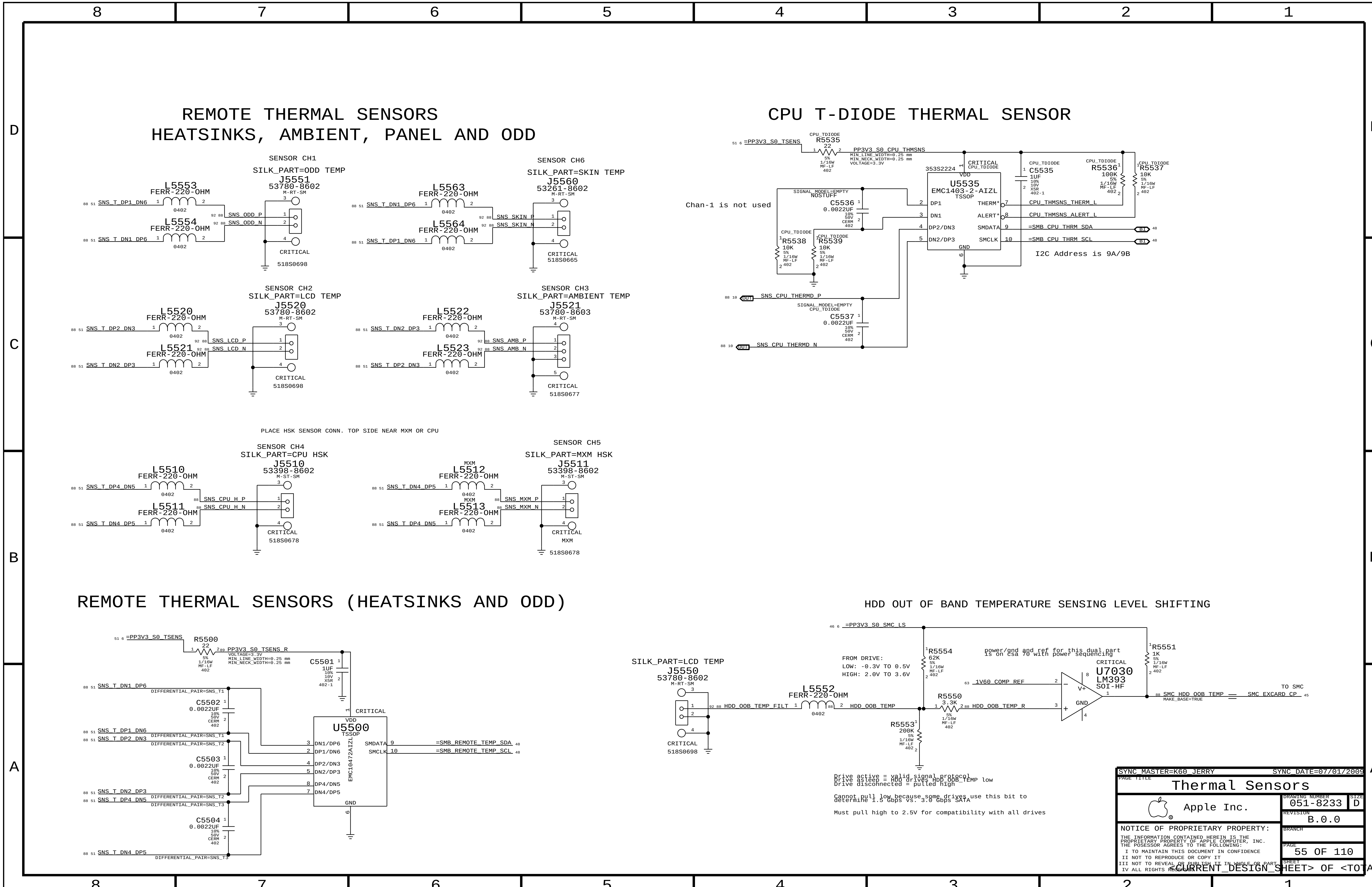
PAGE 54 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC_MASTER=K60_JERRY SYNC_DATE=07/01/2009

PAGE TITLE

Thermal Sensors

Apple Inc.

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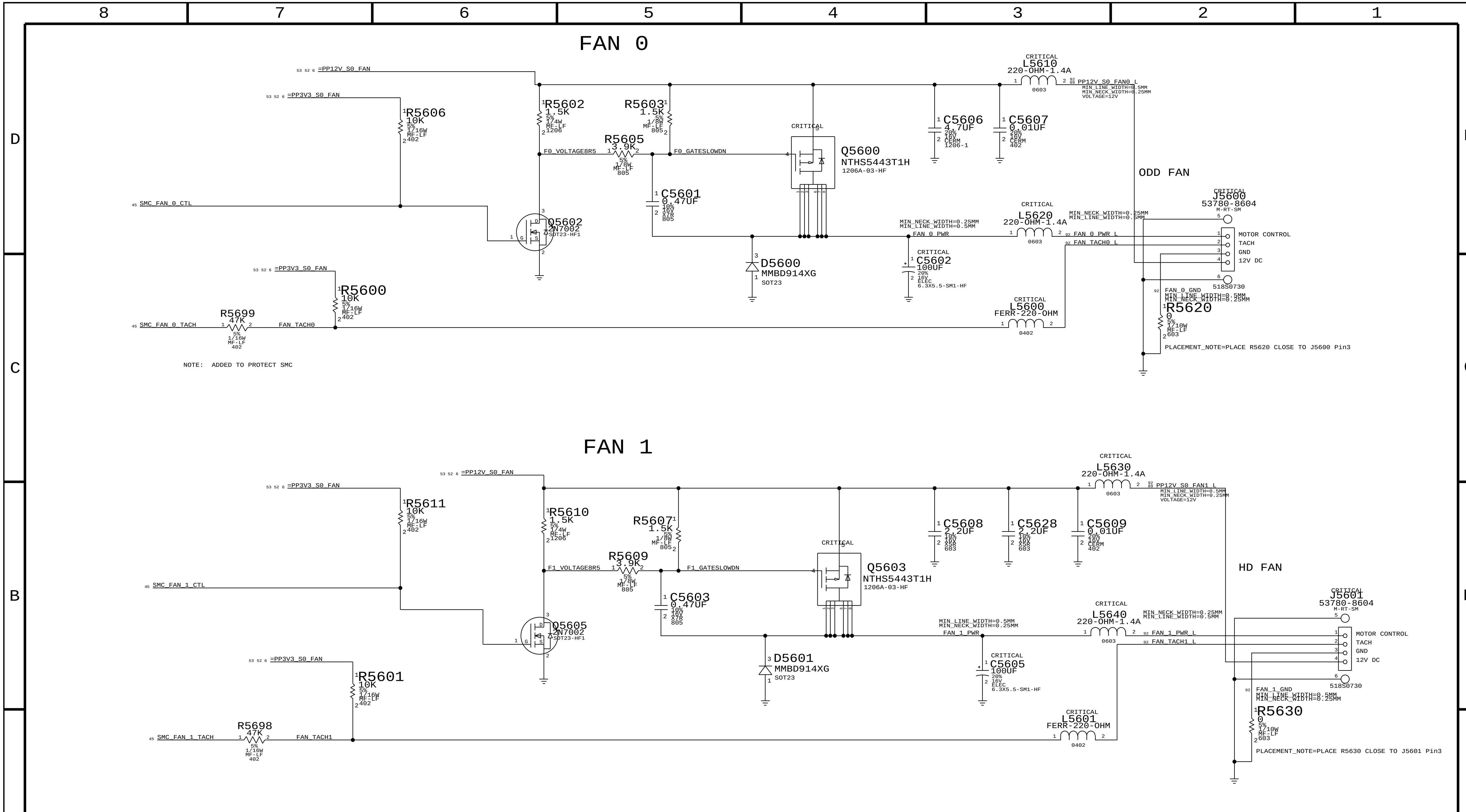
PAGE 55 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC_MASTER=K60_DEREK SYNC_DATE=07/01/2009

PAGE TITLE

HD AND OD FAN

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

REVISION B.0.0

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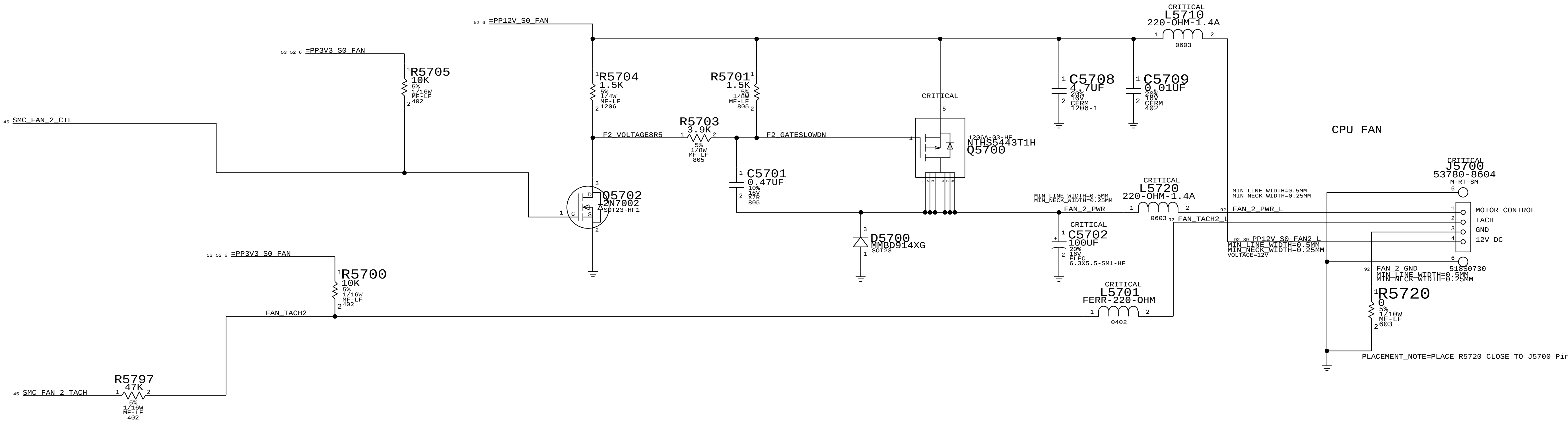
PAGE 56 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

FAN 2



SYNC_MASTER=K60_DEREK SYNC_DATE=07/01/2009

PAGE TITLE

CPU FAN

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

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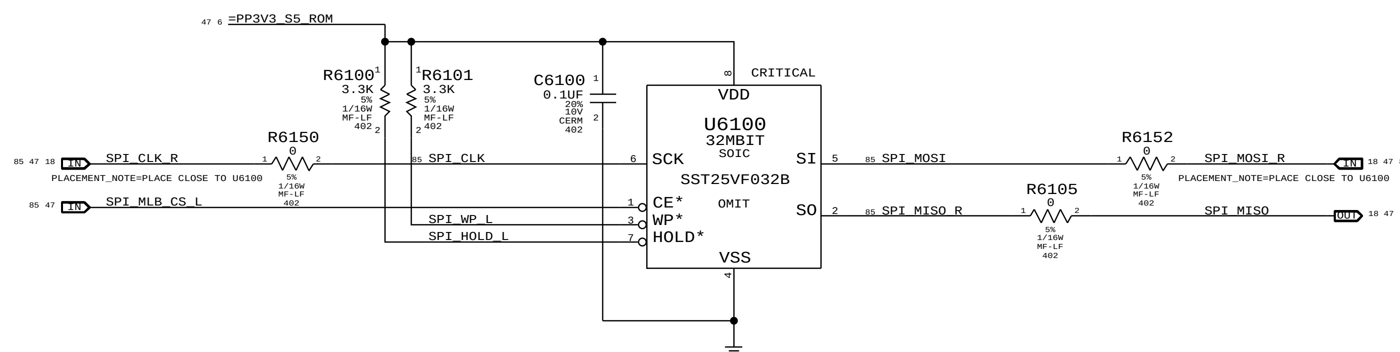
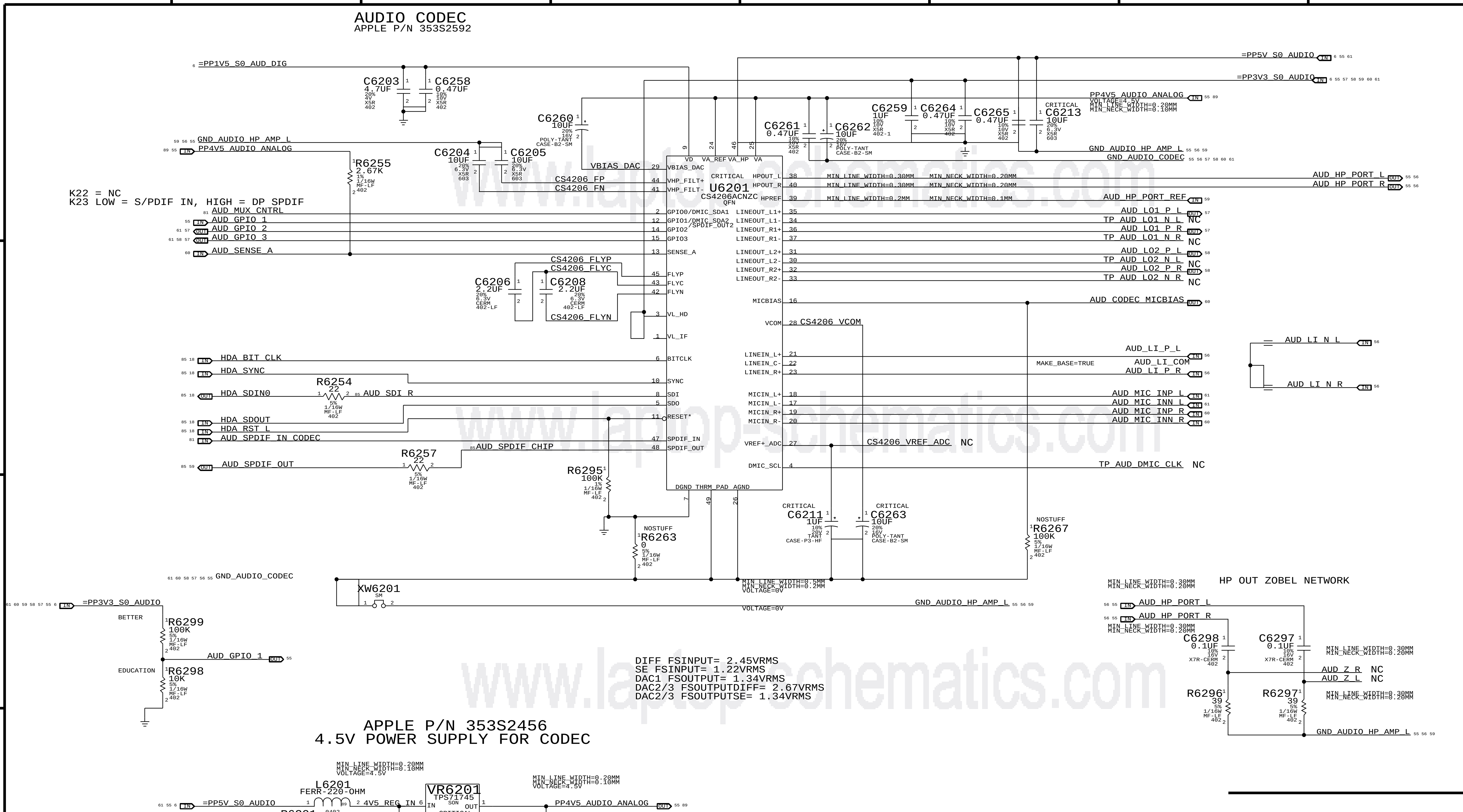
PAGE 57 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC_MASTER=K60_SIJI	SYNC_DATE=07/01/2009
PAGE TITLE: SPI ROM	
Apple Inc.	DRAWING NUMBER: 051-8233 — SIZE: D
	REVISION: B.0.0
	BRANCH:
	PAGE: 61 OF 110
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC_MASTER=K23_SKIP SYNC_DATE=07/16/2009

PAGE TITLE: AUDIO: CODEC/REGULATOR

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D

REVISION: B.0.0

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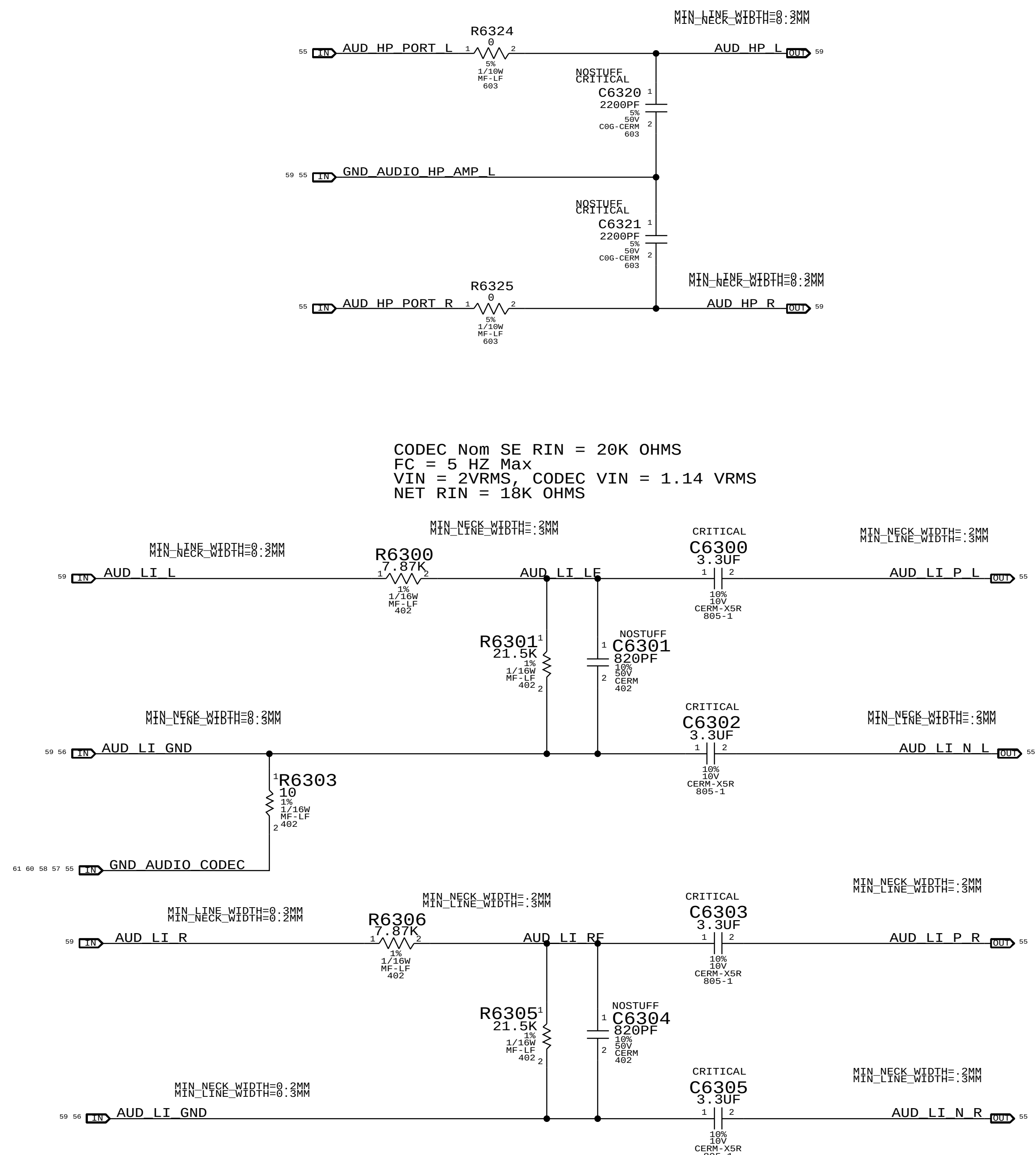
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

1ST ORDER DAC FILTER PLACEHOLDER



SYNC_MASTER=K23_SKIP SYNC_DATE=07/16/2009

PAGE TITLE

AUDIO: FILTER/BUFFER

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

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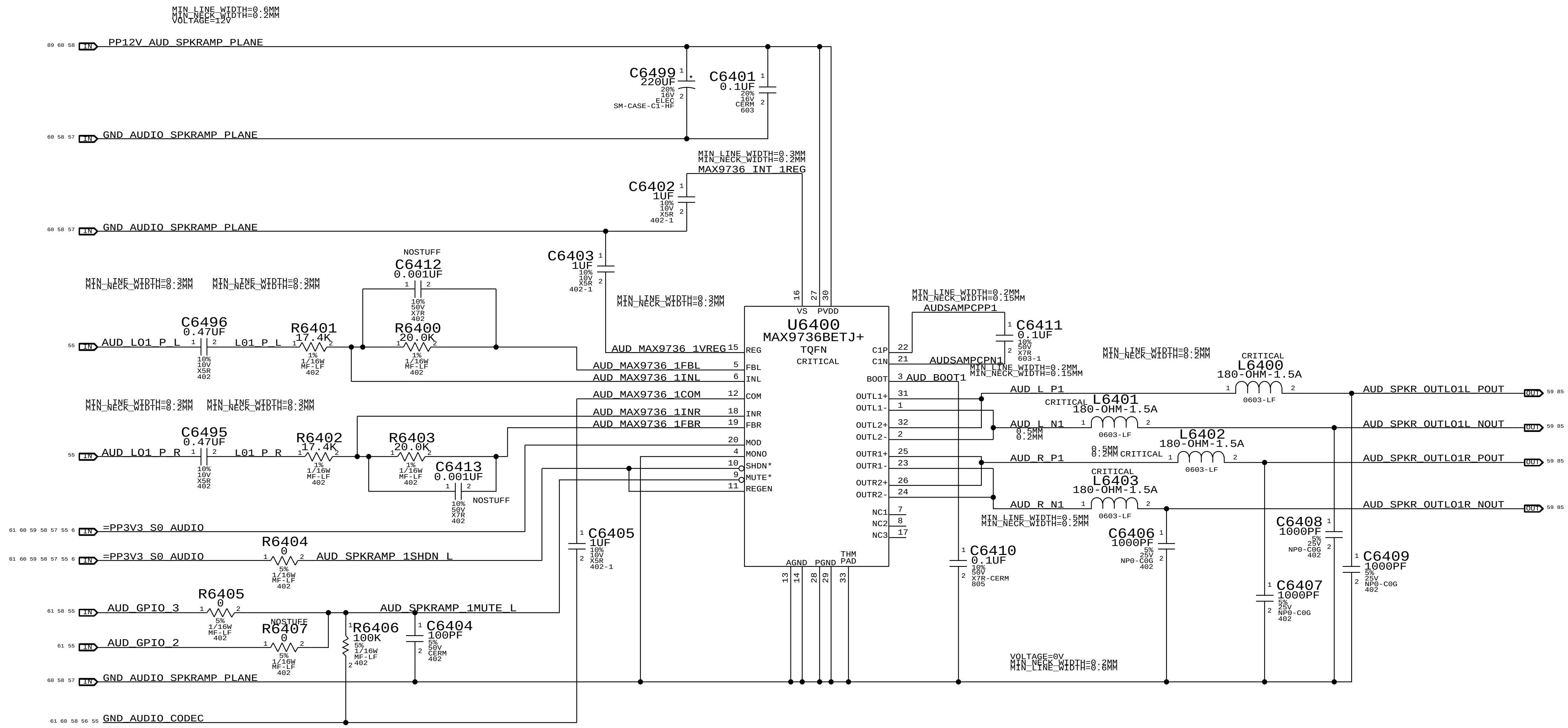
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

TWEETER SPEAKER AMPLIFIER

MAX9736B APN:353S2042

GAIN = -4.8(20K/17.4K)
CODEC OUT = 1.335VRMS
AMP VOUT = 7.355VRMS
POUT = 6.76 W INTO 8 OHMS @ 1% THD+N

TURN ON TIME: 110MS
TURN ON DELAY: 150MS
RIN = 17.4 OHMS
FC = 19.5 HZ



SYNC_MASTER=K23_SKIP SYNC_DATE=07/16/2009

PAGE TITLE

AUDIO: Tweeter Amp 1

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

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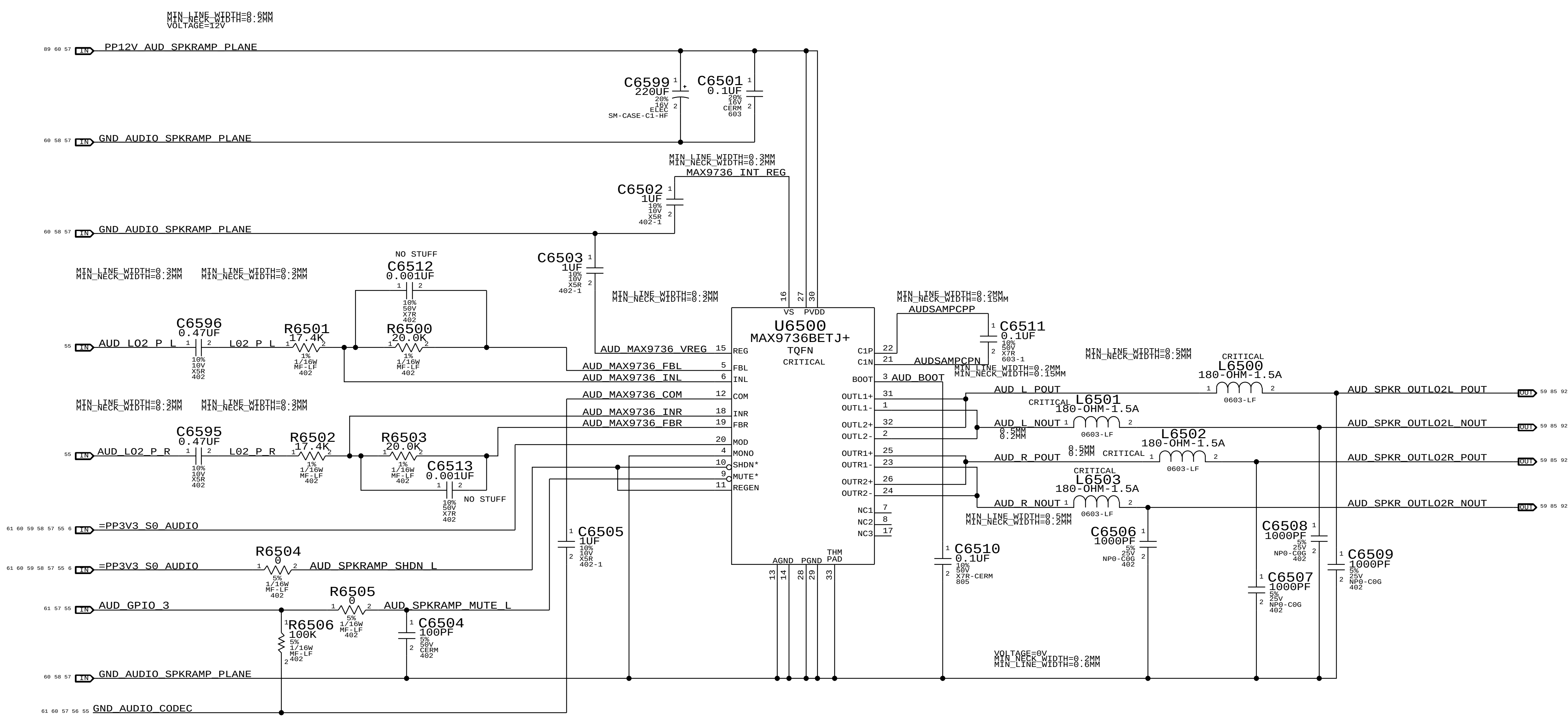
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

WOOFER SPEAKER AMPLIFIER

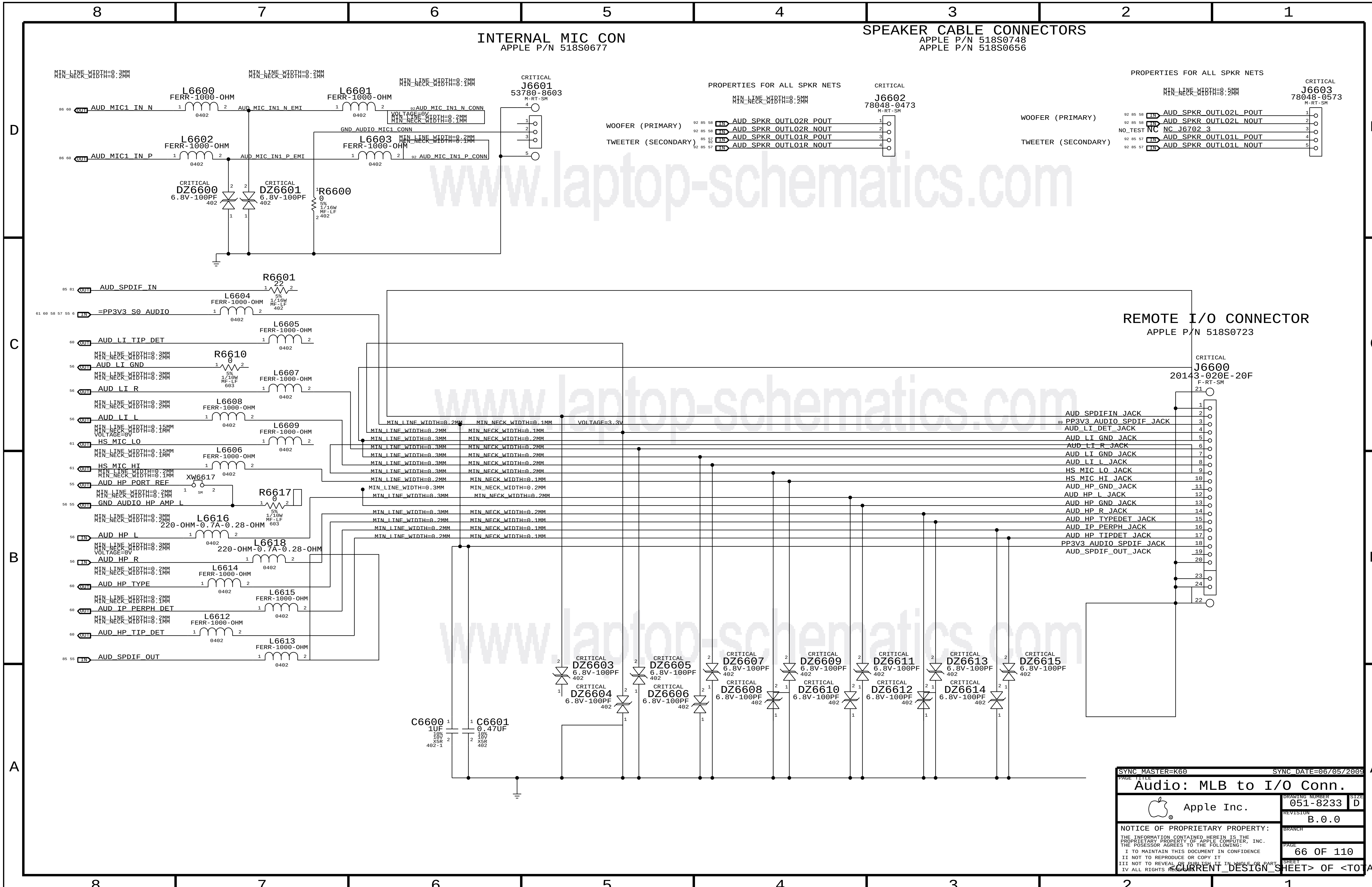
MAX9736B APN:353S2042

GAIN = -4.8(20K/17.4K)
CODEC OUT = 1.335VRMS
AMP VOUT = 7.355VRMS
POUT = 6.76 W INTO 8 OHMS @ 1% THD+N

TURN ON TIME: 110MS
TURN ON DELAY: 150MS
RIN = 17.4 OHMS
FC = 19.5 HZ



SYNC_MASTER=K23_SKIP	SYNC_DATE=07/16/2009
PAGE TITLE	AUDIO: Woofer Amp
Apple Inc.	DRAWING NUMBER 051-8233 SIZE D
	REVISION B.0.0
	BRANCH
	PAGE 65 OF 110
	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>


INTERNAL MIC CON
APPLE P/N 518S0677
SPEAKER CABLE CONNECTORS
APPLE P/N 518S0748
APPLE P/N 518S0656
REMOTE I/O CONNECTOR
APPLE P/N 518S0723
CRITICAL J6601 53780-8603 M-RT-SM
CRITICAL J6602 78048-0473 M-RT-SM
CRITICAL J6603 78048-0573 M-RT-SM
CRITICAL J6600 20143-020E-20F F-RT-SM
PROPERTIES FOR ALL SPKR NETS
WOOFER (PRIMARY)
TWEETER (SECONDARY)
AUD_SPKR_OUTL02R_POUT
AUD_SPKR_OUTL02R_NOUT
AUD_SPKR_OUTL01R_POUT
AUD_SPKR_OUTL01R_NOUT
AUD_SPKR_OUTL02L_POUT
AUD_SPKR_OUTL02L_NOUT
NO_TEST NC NC_J6702_3
AUD_SPKR_OUTL01L_POUT
AUD_SPKR_OUTL01L_NOUT
AUD_MIC1_IN_N
AUD_MIC1_IN_P
AUD_MIC_IN1_N_EMI
AUD_MIC_IN1_P_EMI
AUD_MIC_IN1_N_CONN
AUD_MIC_IN1_P_CONN
GND_AUDIO_MIC1_CONN
L6600 FERR-1000-OHM
L6601 FERR-1000-OHM
L6602 FERR-1000-OHM
L6603 FERR-1000-OHM
CRITICAL DZ6600 6.8V-100PF
CRITICAL DZ6601 6.8V-100PF
R6600 0 5% 1/16W MF-LF 402
AUD_SPDIF_IN
=PP3V3_S0_AUDIO
AUD_LI_TIP_DET
AUD_LI_GND
AUD_LI_R
AUD_LI_L
HS_MIC_LO
HS_MIC_HI
AUD_HP_PORT_REF
XW6617
GND_AUDIO_HP_AMP_L
AUD_HP_L
AUD_HP_R
AUD_HP_TYPE
AUD_IP_PERPH_DET
AUD_HP_TIP_DET
AUD_SPDIF_OUT
R6601 22
R6610 0
R6617 0
L6604 FERR-1000-OHM
L6605 FERR-1000-OHM
L6606 FERR-1000-OHM
L6607 FERR-1000-OHM
L6608 FERR-1000-OHM
L6609 FERR-1000-OHM
L6612 FERR-1000-OHM
L6613 FERR-1000-OHM
L6614 FERR-1000-OHM
L6615 FERR-1000-OHM
L6616 220-OHM-0.7A-0.28-OHM
L6618 220-OHM-0.7A-0.28-OHM
AUD_SPDIFIN_JACK
PP3V3_AUDIO_SPDIF_JACK
AUD_LI_DET_JACK
AUD_LI_GND_JACK
AUD_LI_R_JACK
AUD_LI_L_JACK
HS_MIC_LO_JACK
HS_MIC_HI_JACK
AUD_HP_GND_JACK
AUD_HP_L_JACK
AUD_HP_R_JACK
AUD_HP_TYPEDET_JACK
AUD_IP_PERPH_JACK
AUD_HP_TIPDET_JACK
AUD_SPDIF_OUT_JACK
CRITICAL DZ6603 – DZ6615 6.8V-100PF 402
C6600 1UF 10V X5R 402-1
C6601 0.47UF 10V X5R 402
SYNC_MASTER=K60
SYNC_DATE=06/05/2009
Audio: MLB to I/O Conn.
Apple Inc.
051-8233 D
B.0.0
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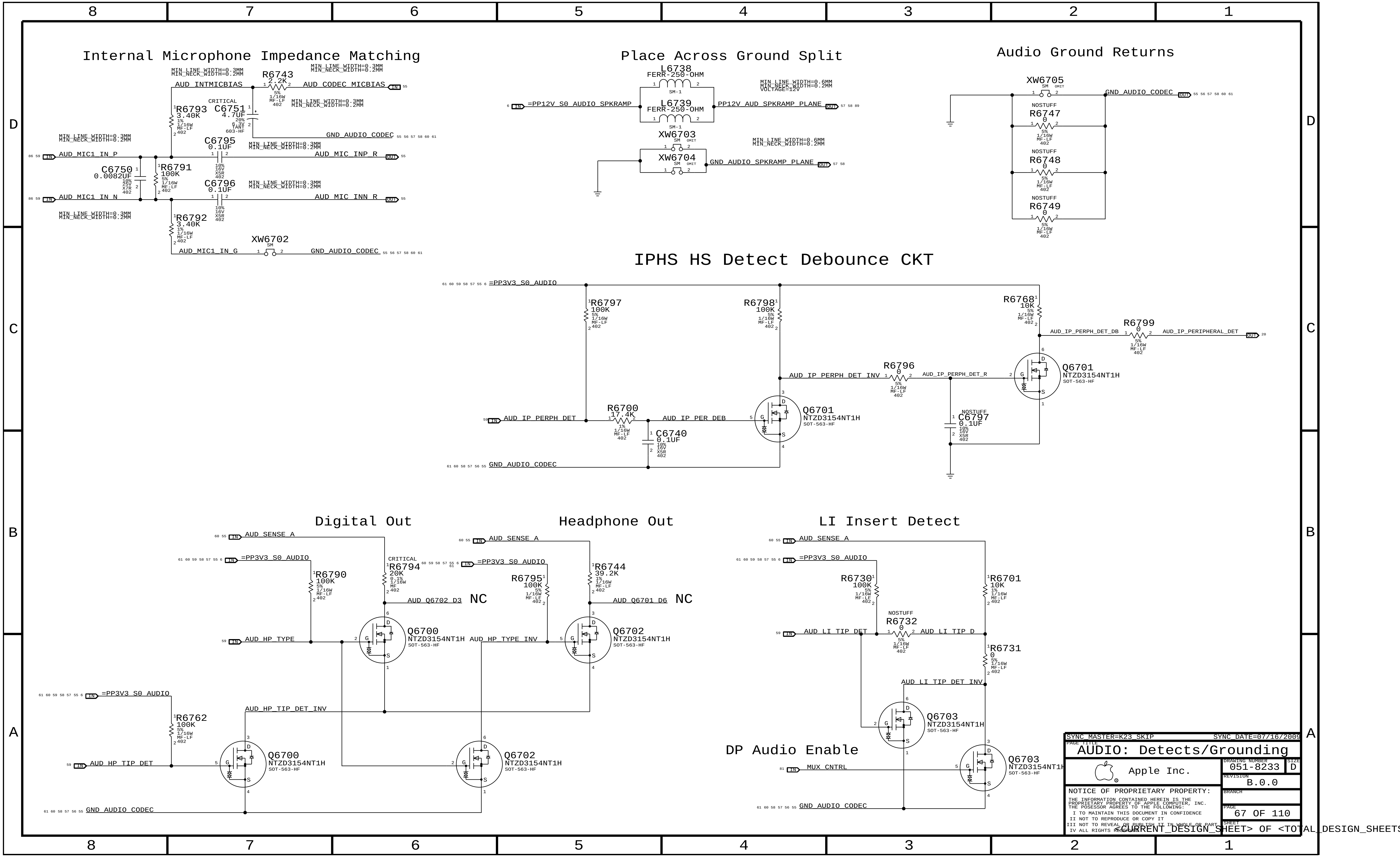
Internal Microphone Impedance Matching
Place Across Ground Split
Audio Ground Returns
IPHS HS Detect Debounce CKT
Digital Out
Headphone Out
LI Insert Detect
DP Audio Enable
AUD_INTMICBIAS
R6743 2.2K
AUD_CODEC_MICBIAS
R6793 3.40K
CRITICAL C6751 4.7UF
GND_AUDIO_CODEC
C6795 0.1UF
AUD_MIC1_IN_P
AUD_MIC_INP_R
C6750 0.0082UF
R6791 100K
C6796 0.1UF
AUD_MIC1_IN_N
AUD_MIC_INN_R
R6792 3.40K
XW6702
AUD_MIC1_IN_G
L6738 FERR-250-OHM
L6739 FERR-250-OHM
=PP12V_S0_AUDIO_SPKRAMP
PP12V_AUD_SPKRAMP_PLANE
XW6703
XW6704
GND_AUDIO_SPKRAMP_PLANE
XW6705
NOSTUFF R6747 0
NOSTUFF R6748 0
NOSTUFF R6749 0
=PP3V3_S0_AUDIO
R6797 100K
R6798 100K
R6768 10K
R6799 0
AUD_IP_PERPH_DET_DB
AUD_IP_PERIPHERAL_DET
R6796 0
AUD_IP_PERPH_DET_INV
AUD_IP_PERPH_DET_R
Q6701 NTZD3154NT1H SOT-563-HF
NOSTUFF C6797 0.1UF
AUD_IP_PERPH_DET
R6700 17.4K
AUD_IP_PER_DEB
C6740 0.1UF
AUD_SENSE_A
R6790 100K
CRITICAL R6794 20K
AUD_Q6702_D3 NC
Q6700 NTZD3154NT1H SOT-563-HF
AUD_HP_TYPE
AUD_HP_TYPE_INV
R6795 100K
R6744 39.2K
AUD_Q6701_D6 NC
Q6702 NTZD3154NT1H SOT-563-HF
R6762 100K
AUD_HP_TIP_DET_INV
AUD_HP_TIP_DET
R6730 100K
R6701 10K
NOSTUFF R6732 0
AUD_LI_TIP_DET
AUD_LI_TIP_D
R6731 0
AUD_LI_TIP_DET_INV
Q6703 NTZD3154NT1H SOT-563-HF
MUX_CNTRL
SYNC_MASTER=K23_SKIP
SYNC_DATE=07/16/2009
AUDIO: Detects/Grounding
Apple Inc.
051-8233
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B.0.0
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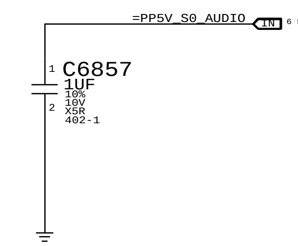
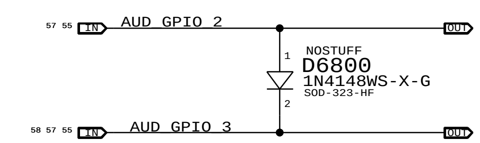
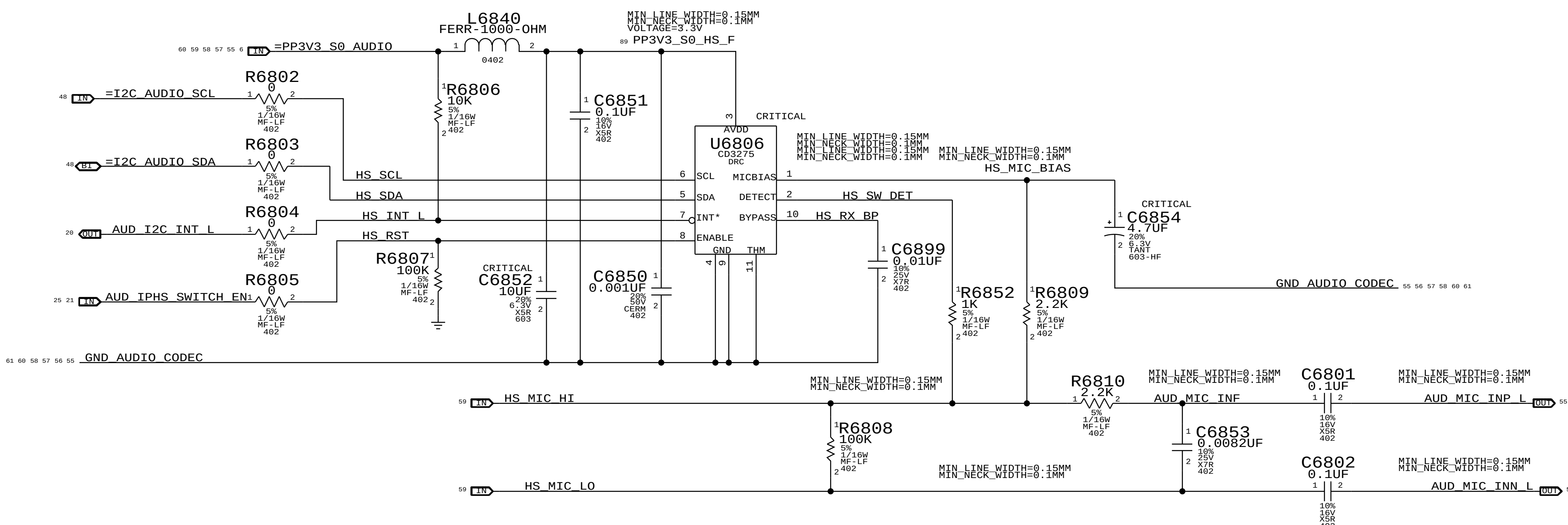
FUNCTION	PIN	CONVERTER	VOLUME	ENABLE/ CNTRL TYPE	DETECT/INTERRUPT
PRIMARY	0X0B	0X04	0X04	GPIO 3	N/A
SECONDARY	0X0A	0X03	0X03	GPIO 3	N/A
HEADPHONES	0X09	0X02	0X02	N/A	0X09 (A)
LINE INPUT	0X0C	0X05	0X05	N/A	LINE IN
BUILT-IN MICROPHONE	0X0D(13,B,RIGHT)	0X06	0X06	MICBIAS 80%	N/A
HEADSET MICROPHONE	0X0D (13,V22,B,LEFT)	0X06	0X06	MIKEY	MIKEY
SPDIF OUT	0X10	0X08	N/A	N/A	0X0C (B)
SPDIF IN	0X0F	0X07	N/A	N/A	N/A
MIKEY	N/A	N/A	N/A	MCP GPIO_38	MCP GPIO_5





MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2256



FLP = 8.82 KHZ
FHP = 80 HZ

SYNC_MASTER=K23_SKIP SYNC_DATE=07/16/2009

PAGE TITLE
AUDIO: Mikey

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

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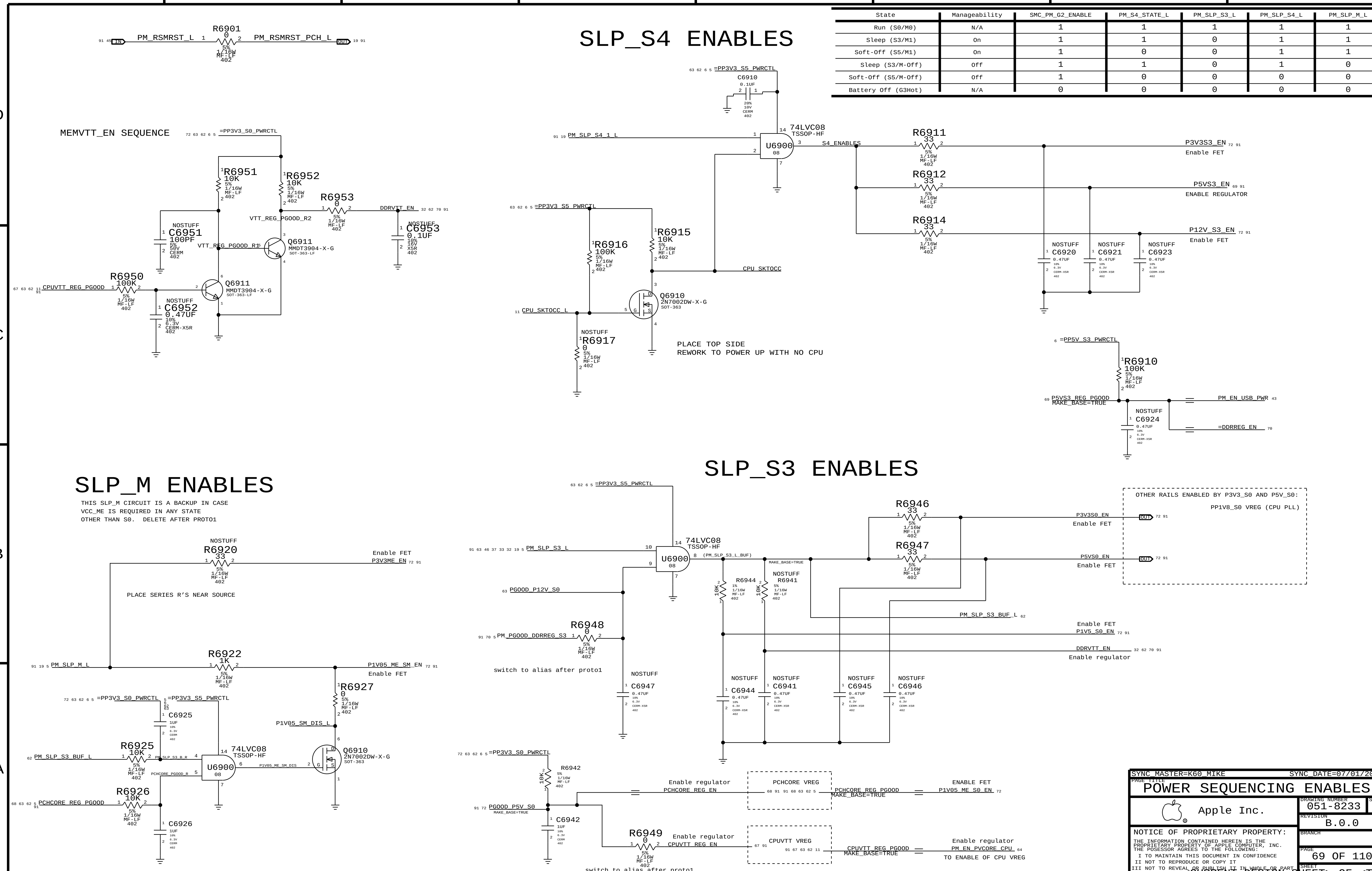
SLP_S4 ENABLES

State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0



SYNC_MASTER=K60_MIKE SYNC_DATE=07/01/2009

PAGE TITLE

POWER SEQUENCING ENABLES

Apple Inc.

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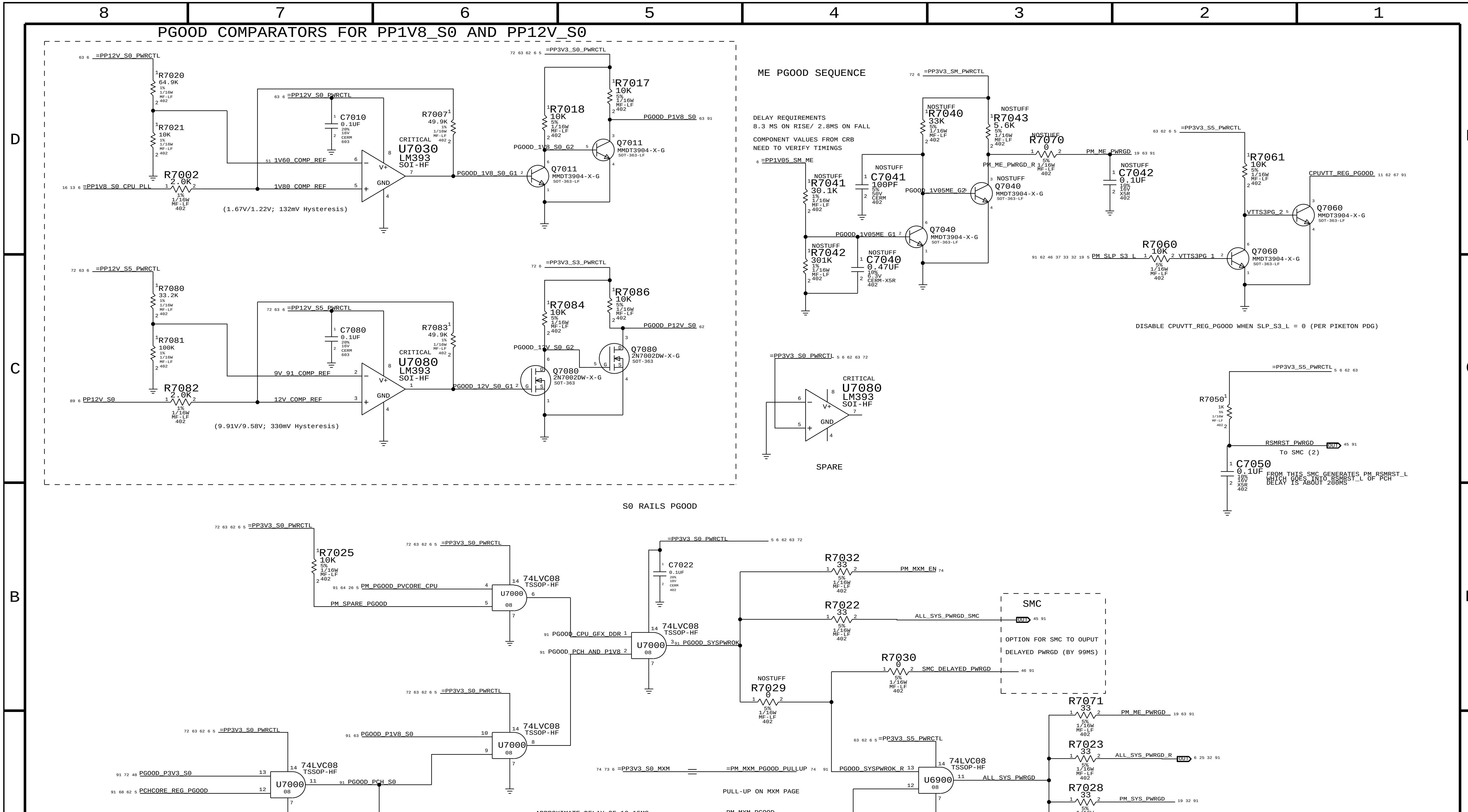
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC_MASTER=K60_MIKE SYNC_DATE=07/01/2009

PAGE TITLE: POWER SEQUENCING PGOOD

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D

REVISION: B.0.0

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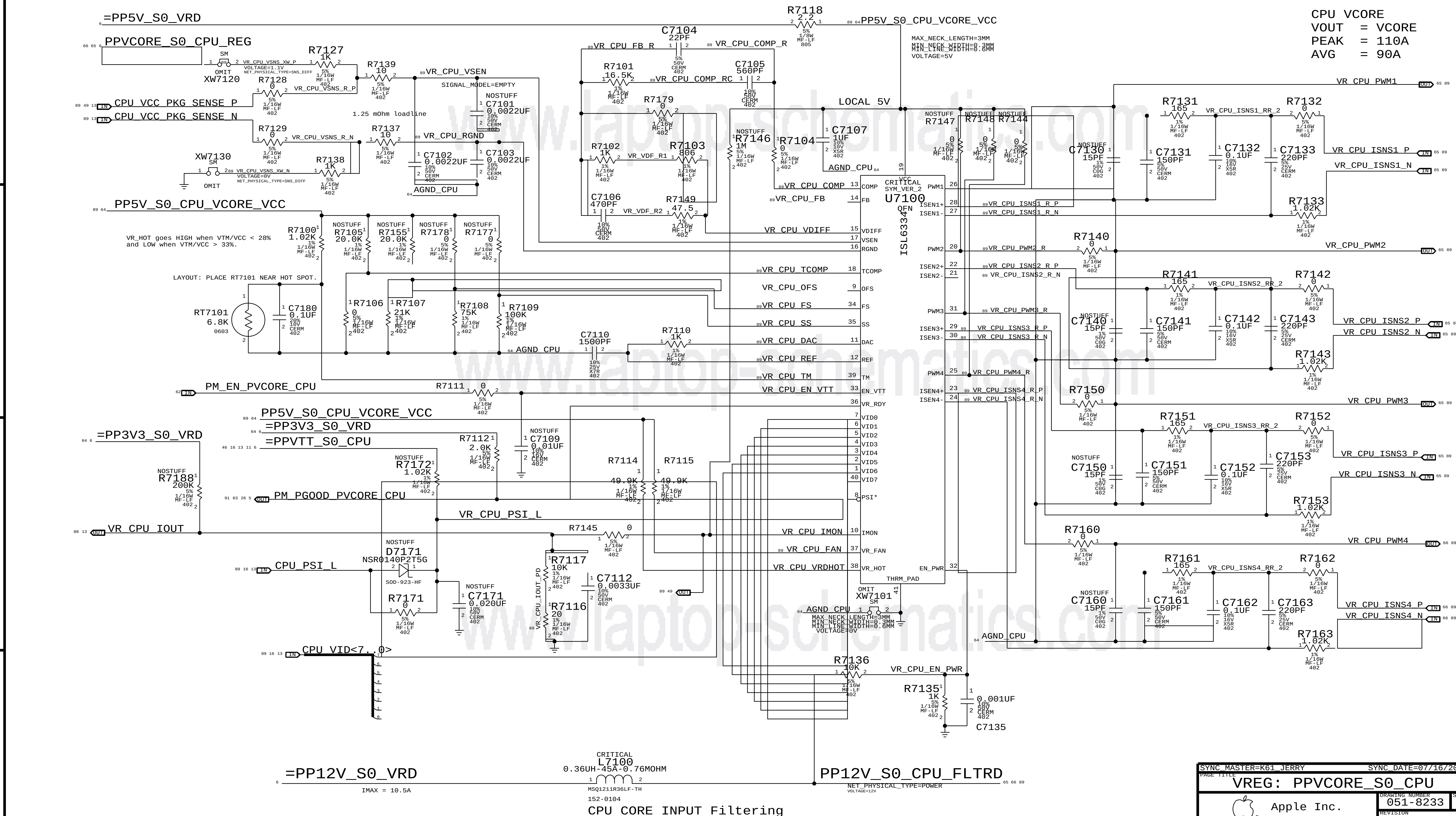
PAGE: 70 OF 110

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8	7	6	5	4	3	2	1

CPU CORE REG 1.1V/110A O/P= PPVCORE_S0_CPU_REG



SYNC_MASTER=K61_JERRY SYNC_DATE=07/16/2009

PAGE TITLE
VREG: PPVCORE_S0_CPU

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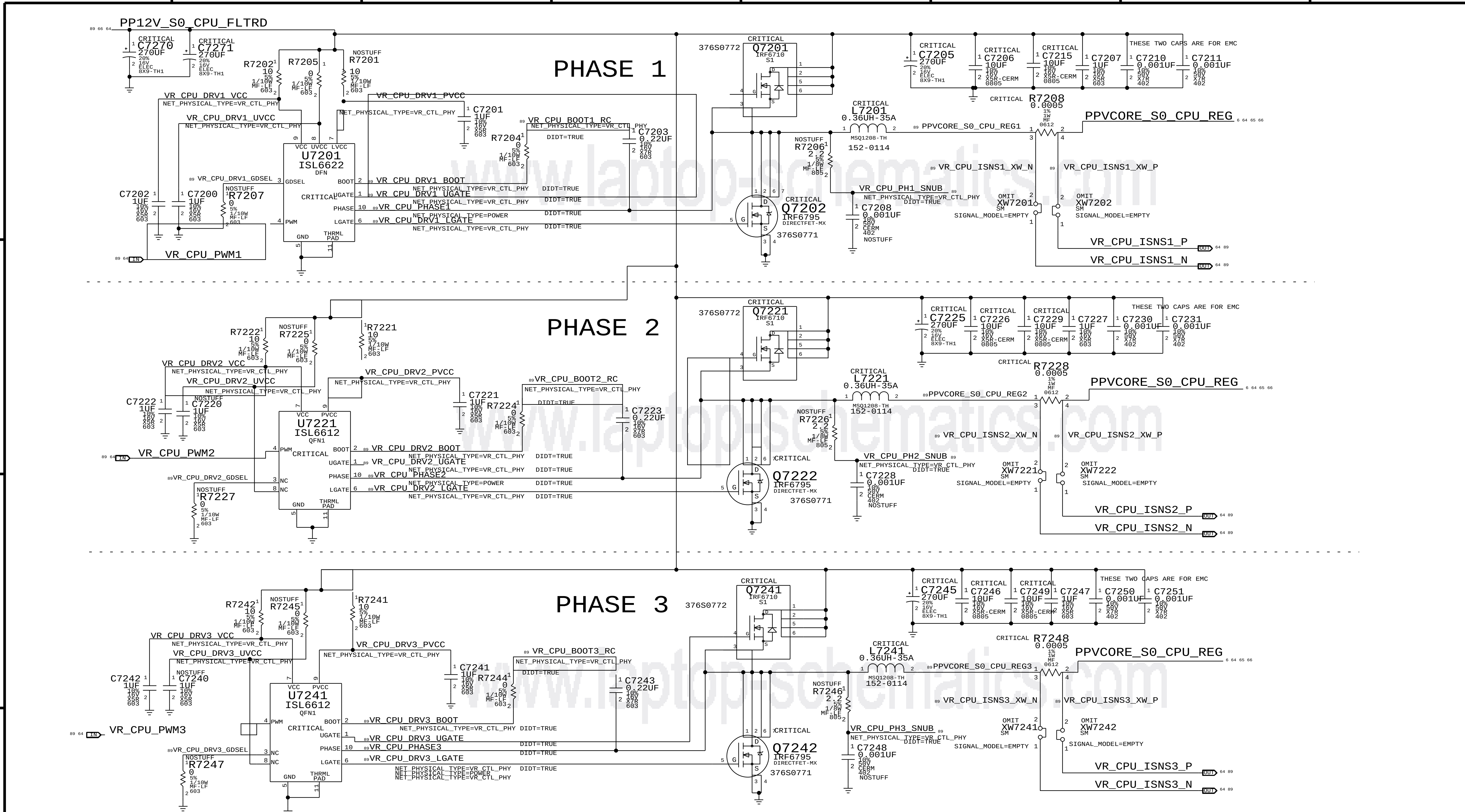
PAGE 71 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8	7	6	5	4	3	2	1



SYNC_MASTER=K60_JERRY SYNC_DATE=07/01/2009

PAGE TITLE

VREG: CPU CORE - PHASES 1-3

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DRAWING NUMBER 051-8233 SIZE D

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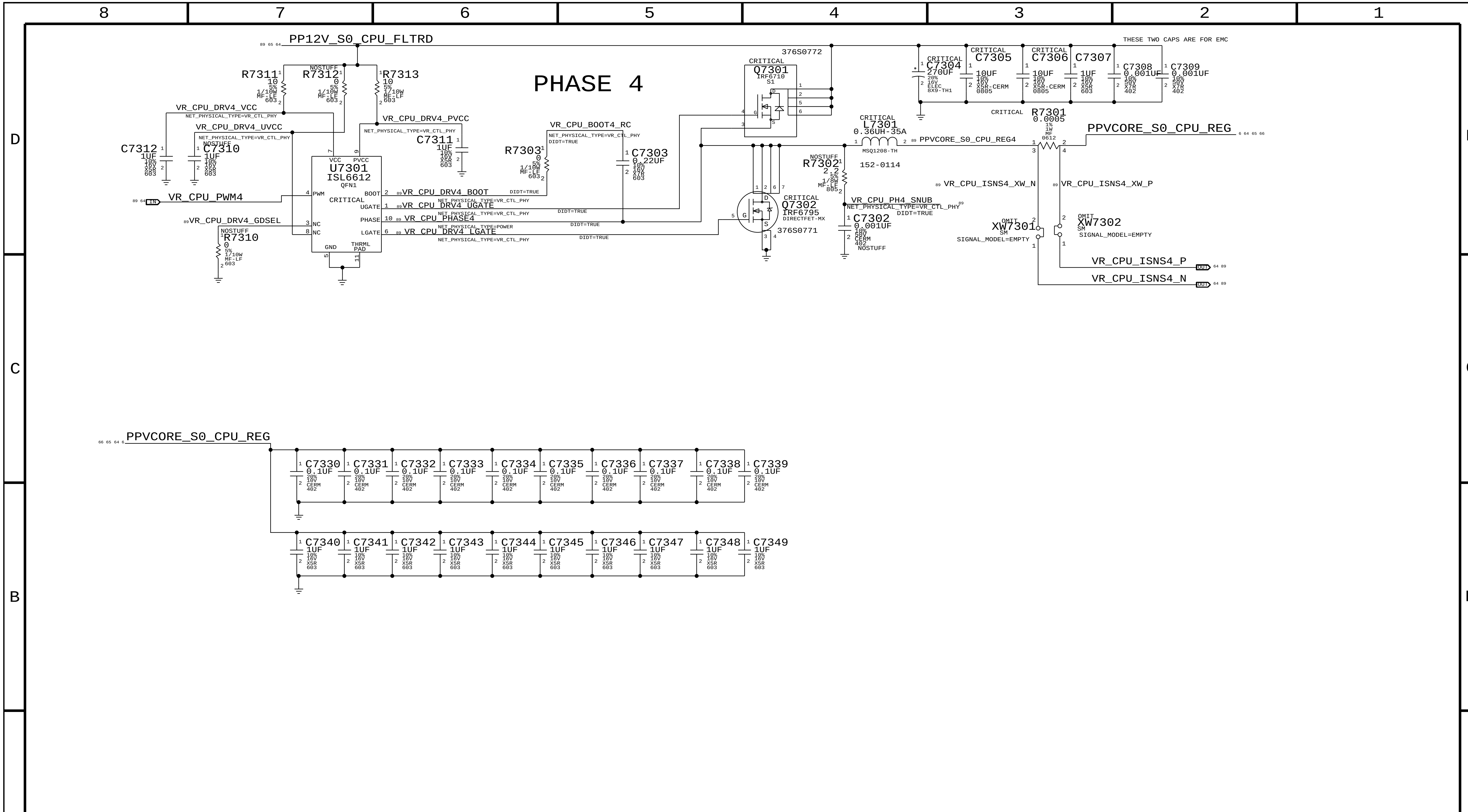
PAGE 72 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC_MASTER=K61_JERRY SYNC_DATE=07/16/2009

PAGE TITLE: VREG: CPU CORE - PHASE 4

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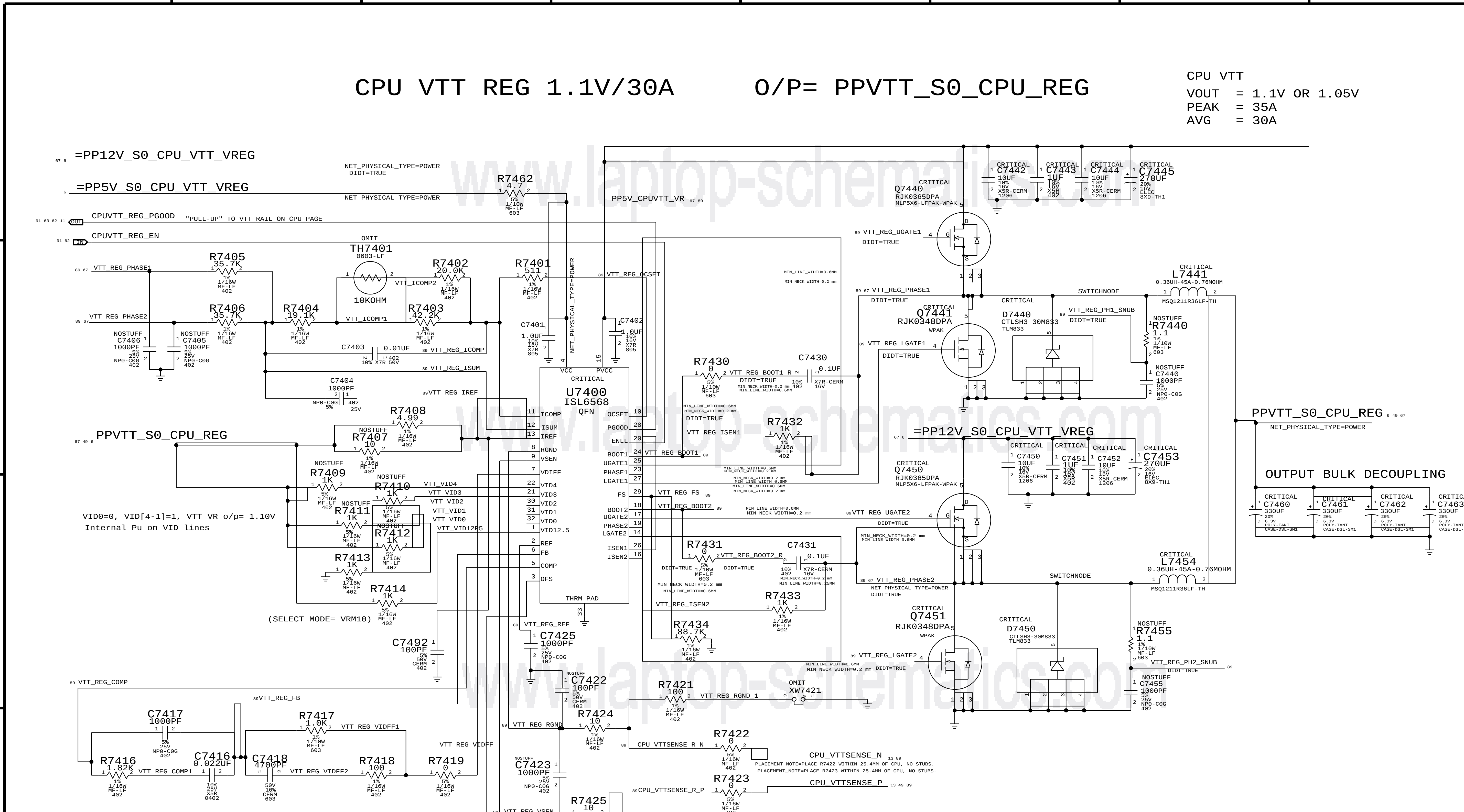
DRAWING NUMBER: 051-8233 SIZE: D

REVISION: B.0.0

BRANCH

PAGE: 73 OF 110

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
113S0127	1	RES,68k,0603,5%	TH7401	

SYNC_MASTER=K61_JERRY SYNC_DATE=07/16/2009

PAGE TITLE

CPU VTT REGULATOR

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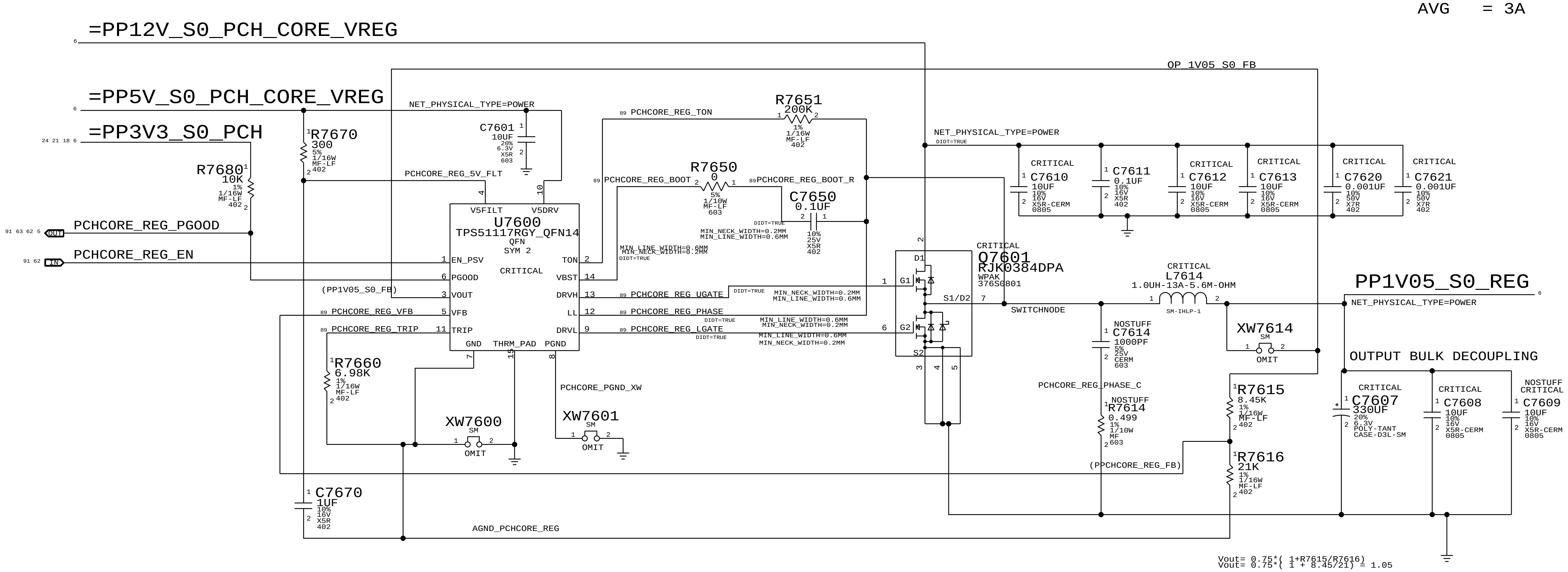
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

IBEX PEAK CORE REG 1.05V OUTPUT = PP1V05_S0_REG

PP1V05_S0_REG

VOUT = 1.05V
PEAK = 7.5A
AVG = 3A



PAGE TITLE
IBEX PEAK CORE

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DRAWING NUMBER 051-8233 SIZE D

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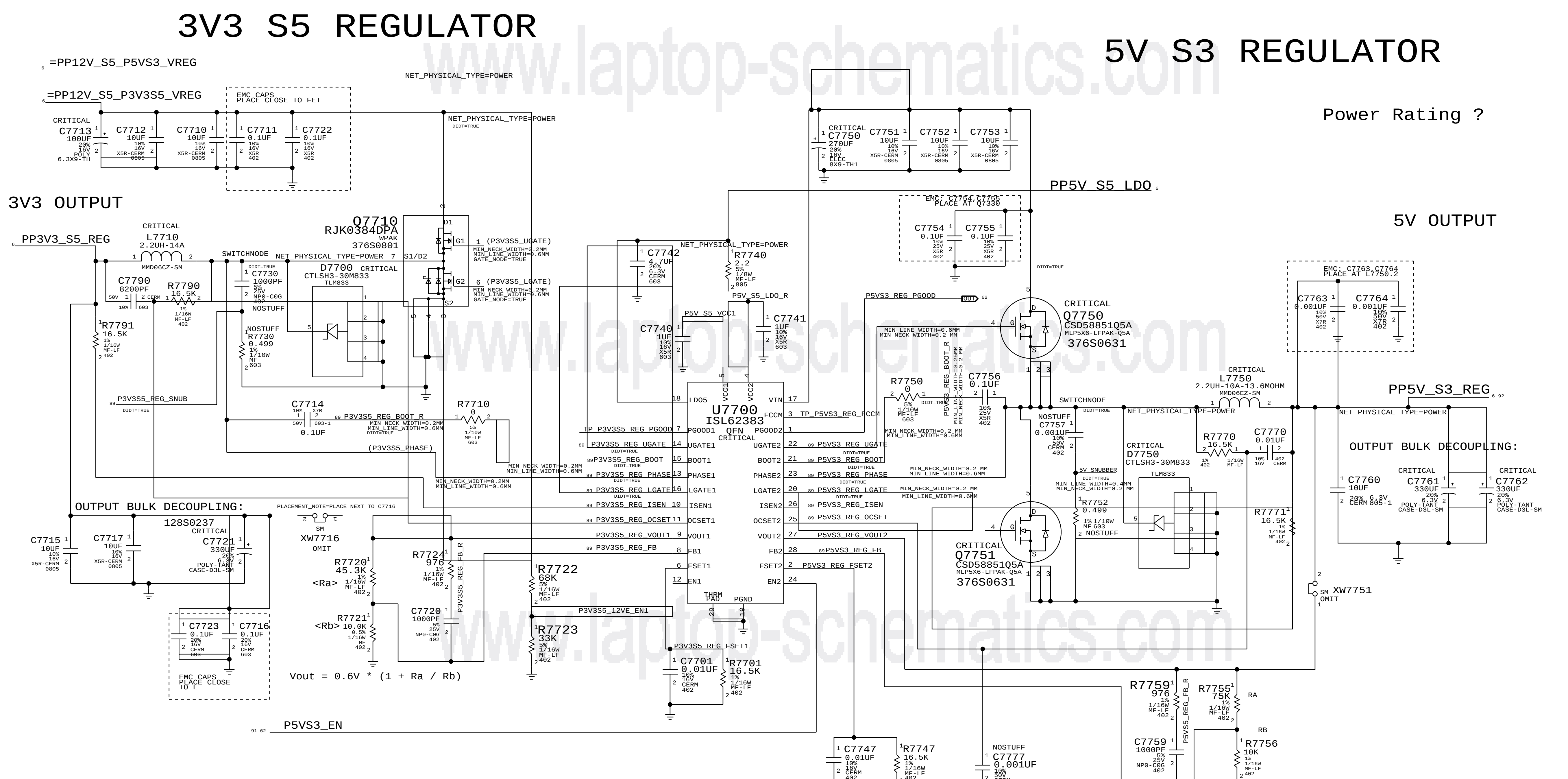

SYNC_MASTER=K60_JERRY	SYNC_DATE=07/01/2009
PAGE TITLE	5V_S3 / 3V3_S5 VREGS
Apple Inc.	DRAWING NUMBER 051-8233 SIZE D
	REVISION B.0.0
	BRANCH
	PAGE 77 OF 110
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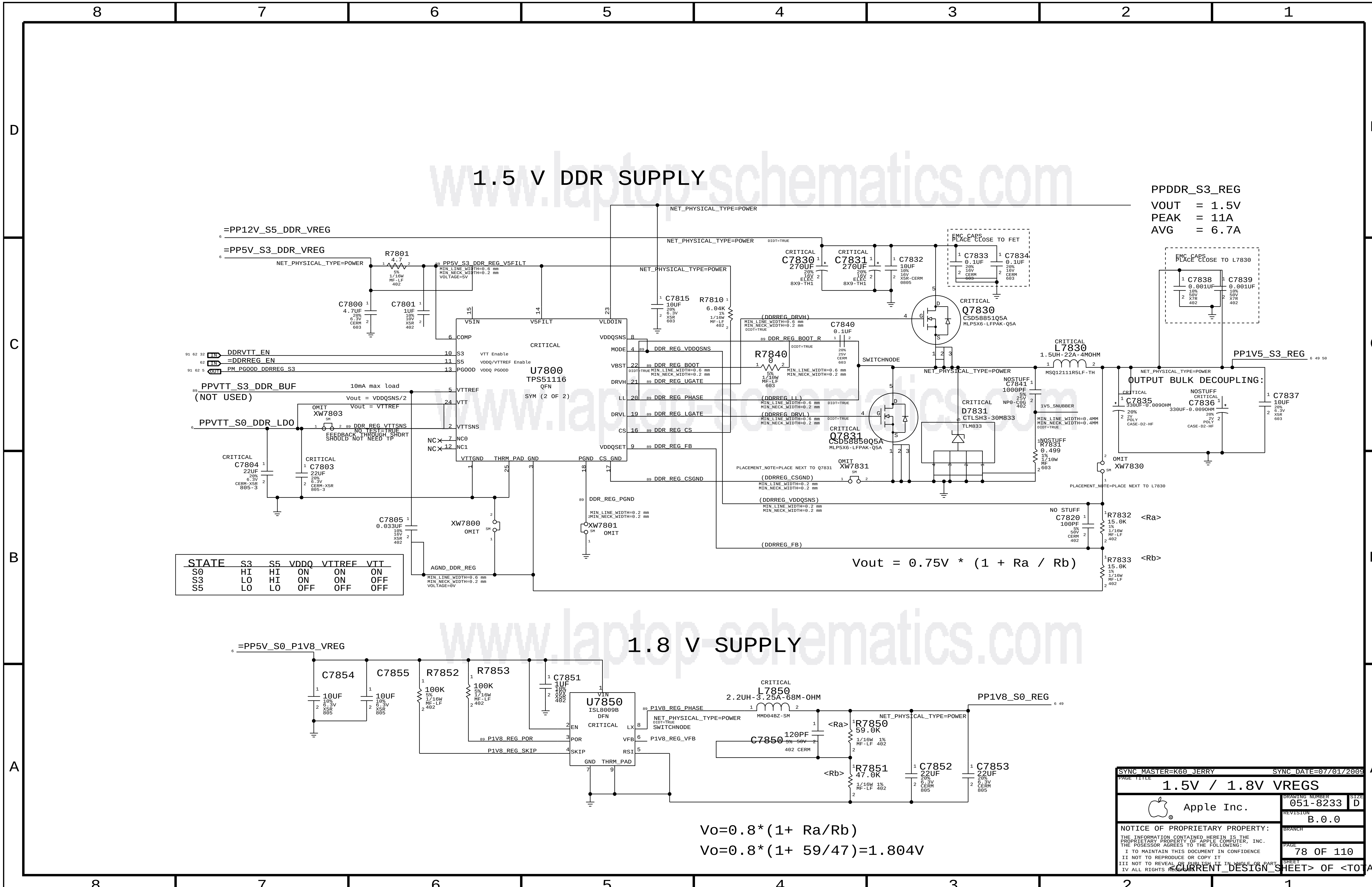

1.5 V DDR SUPPLY
PPDDR_S3_REG
VOUT = 1.5V
PEAK = 11A
AVG = 6.7A
=PP12V_S5_DDR_VREG
=PP5V_S3_DDR_VREG
NET_PHYSICAL_TYPE=POWER
R7801
PP5V_S3_DDR_REG_V5FILT
C7800
C7801
C7815
R7810
CRITICAL
C7830
270UF
C7831
270UF
C7832
10UF
EMC CAPS
PLACE CLOSE TO FET
C7833
0.1UF
C7834
0.1UF
PLACE CLOSE TO L7830
C7838
0.001UF
C7839
0.001UF
Q7830
CSD58851Q5A
MLP5X6-LFPAK-Q5A
DDRVTT_EN
=DDRREG_EN
PM_PGOOD_DDRREG_S3
U7800
TPS51116
QFN
SYM (2 OF 2)
V5IN
V5FILT
VLDOIN
COMP
S3
S5
PGOOD
VTTREF
VTT
VTTSNS
NC0
NC1
VTTGND
THRM_PAD GND
PGND
CS_GND
VDDQSNS
MODE
VBST
DRVH
LL
DRVL
CS
VDDQSET
VTT Enable
VDDQ/VTTREF Enable
VDDQ PGOOD
PPVTT_S3_DDR_BUF
(NOT USED)
10mA max load
Vout = VDDQSNS/2
Vout = VTTREF
PPVTT_S0_DDR_LDO
OMIT
XW7803
DDR_REG_VTTSNS
NO_TEST=TRUE
FEEDBACK THROUGH SHORT
SHOULD NOT NEED TP
C7804
22UF
C7803
22UF
DDR_REG_VDDQSNS
C7840
0.1UF
R7840
0
DDR_REG_BOOT
DDR_REG_BOOT_R
DDR_REG_UGATE
DDR_REG_PHASE
DDR_REG_LGATE
DDR_REG_CS
DDR_REG_FB
SWITCHNODE
L7830
1.5UH-22A-4MOHM
MSQ12111R5LF-TH
PP1V5_S3_REG
OUTPUT BULK DECOUPLING:
C7835
C7836
330UF-0.009OHM
C7837
10UF
NOSTUFF
C7841
1000PF
R7831
0.499
1V5_SNUBBER
D7831
CTLSH3-30M833
Q7831
CSD58850Q5A
XW7831
DDR_REG_CSGND
PLACEMENT_NOTE=PLACE NEXT TO Q7831
OMIT
XW7830
PLACEMENT_NOTE=PLACE NEXT TO L7830
DDR_REG_PGND
XW7801
OMIT
C7805
0.033UF
XW7800
OMIT
AGND_DDR_REG
NO STUFF
C7820
100PF
R7832
15.0K
<Ra>
R7833
15.0K
<Rb>
Vout = 0.75V * (1 + Ra / Rb)
STATE S3 S5 VDDQ VTTREF VTT
S0 HI HI ON ON ON
S3 LO HI ON ON OFF
S5 LO LO OFF OFF OFF
1.8 V SUPPLY
=PP5V_S0_P1V8_VREG
C7854
10UF
C7855
10UF
R7852
100K
R7853
100K
C7851
1UF
U7850
ISL8009B
DFN
EN
POR
SKIP
VIN
LX
VFB
RSI
GND
THRM_PAD
P1V8_REG_PHASE
P1V8_REG_POR
P1V8_REG_SKIP
P1V8_REG_VFB
L7850
2.2UH-3.25A-68M-OHM
MMD04BZ-SM
PP1V8_S0_REG
C7850
120PF
R7850
59.0K
R7851
47.0K
C7852
22UF
C7853
22UF
Vo=0.8*(1+ Ra/Rb)
Vo=0.8*(1+ 59/47)=1.804V
SYNC_MASTER=K60_JERRY
SYNC_DATE=07/01/2009
1.5V / 1.8V VREGS
Apple Inc.
051-8233
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B.0.0
78 OF 110
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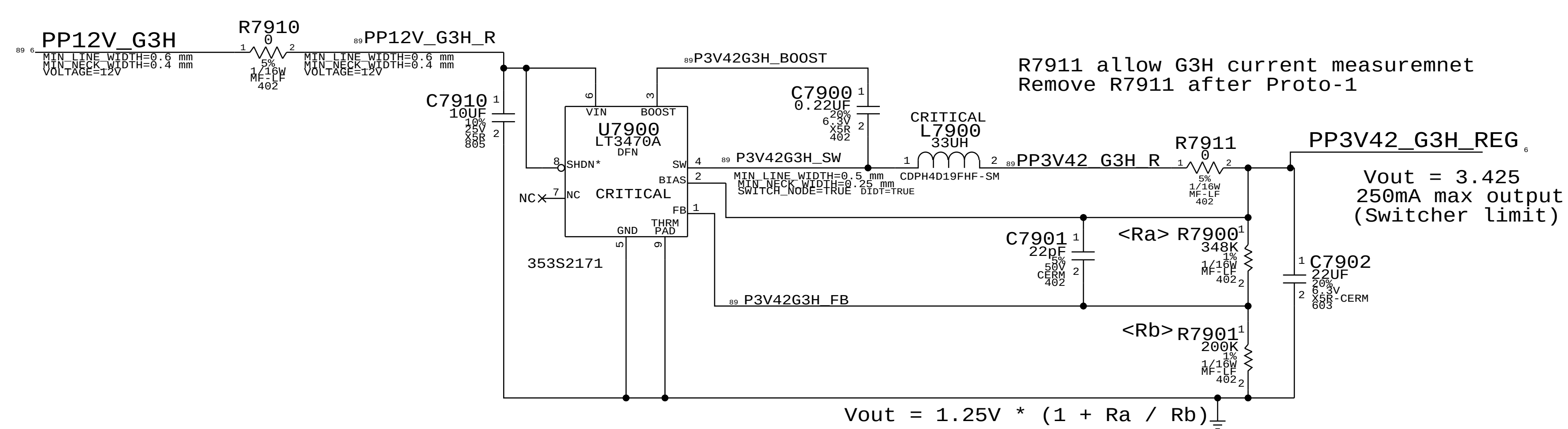
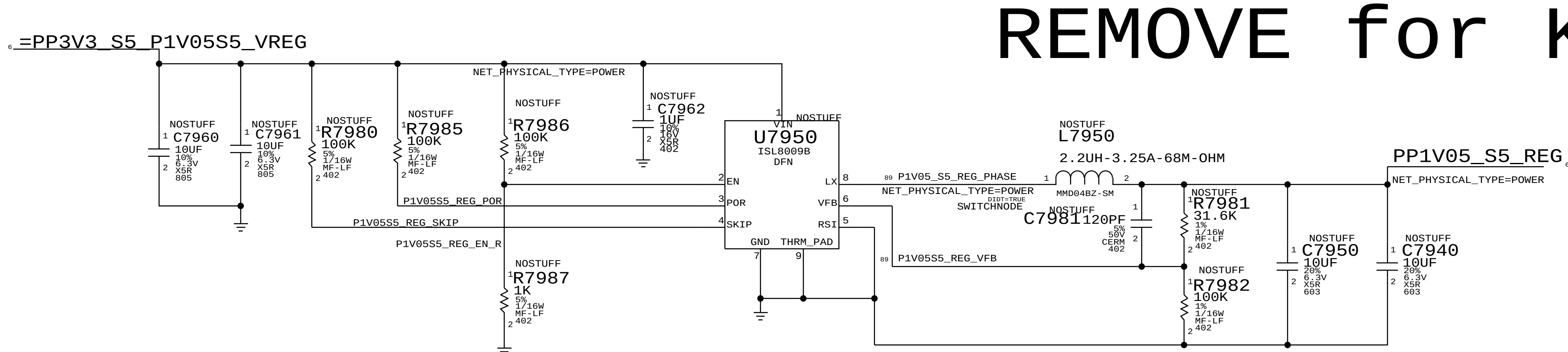
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



1.05V S5 SUPPLY

REMOVE for K60/K61



SYNC_MASTER=K60_JERRY SYNC_DATE=07/01/2009

PAGE TITLE

1.05 S5 SUPPLY

Apple Inc.

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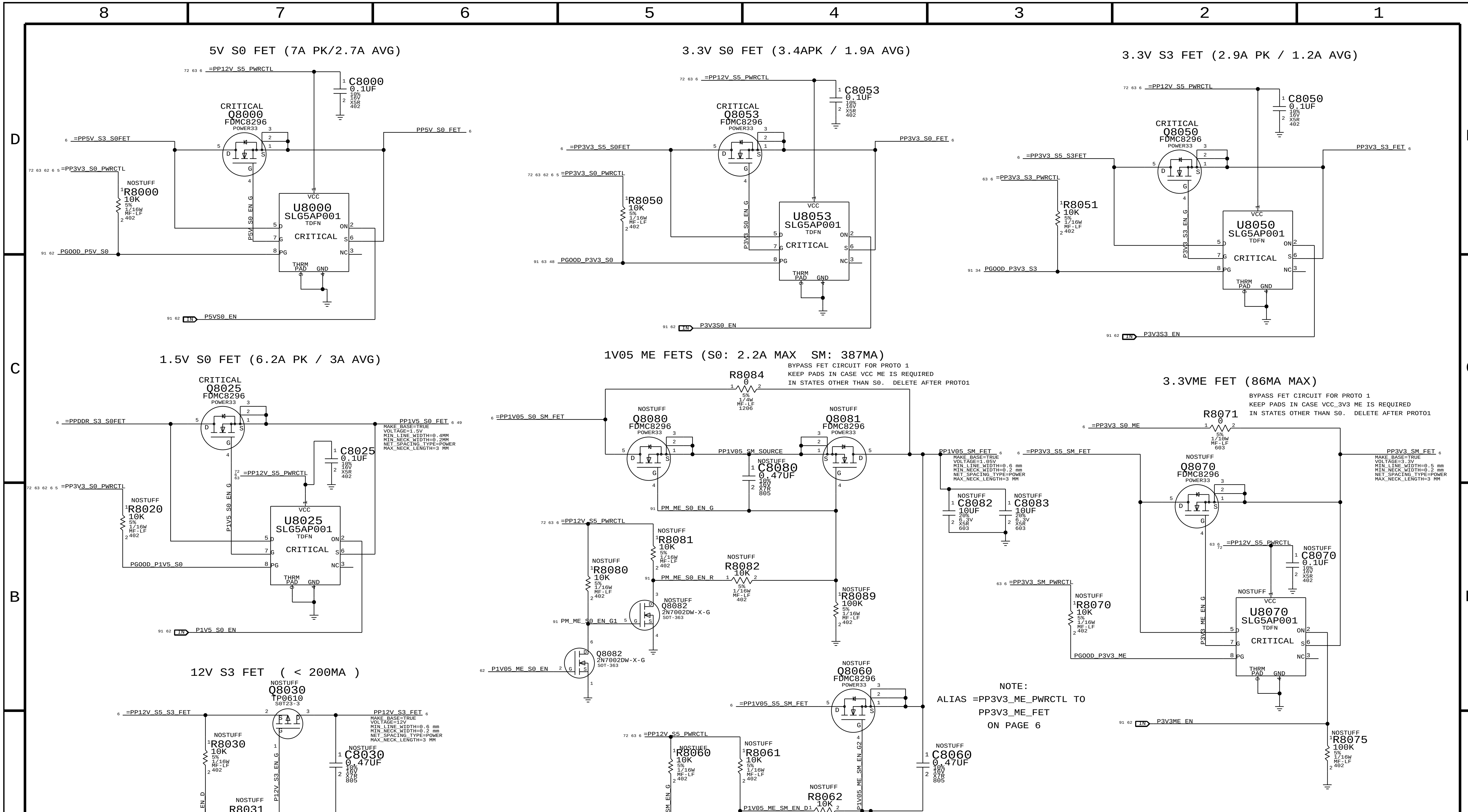
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC_MASTER=K60_MIKE SYNC_DATE=07/01/2009

PAGE TITLE

S3+S0 FETS

Apple Inc.

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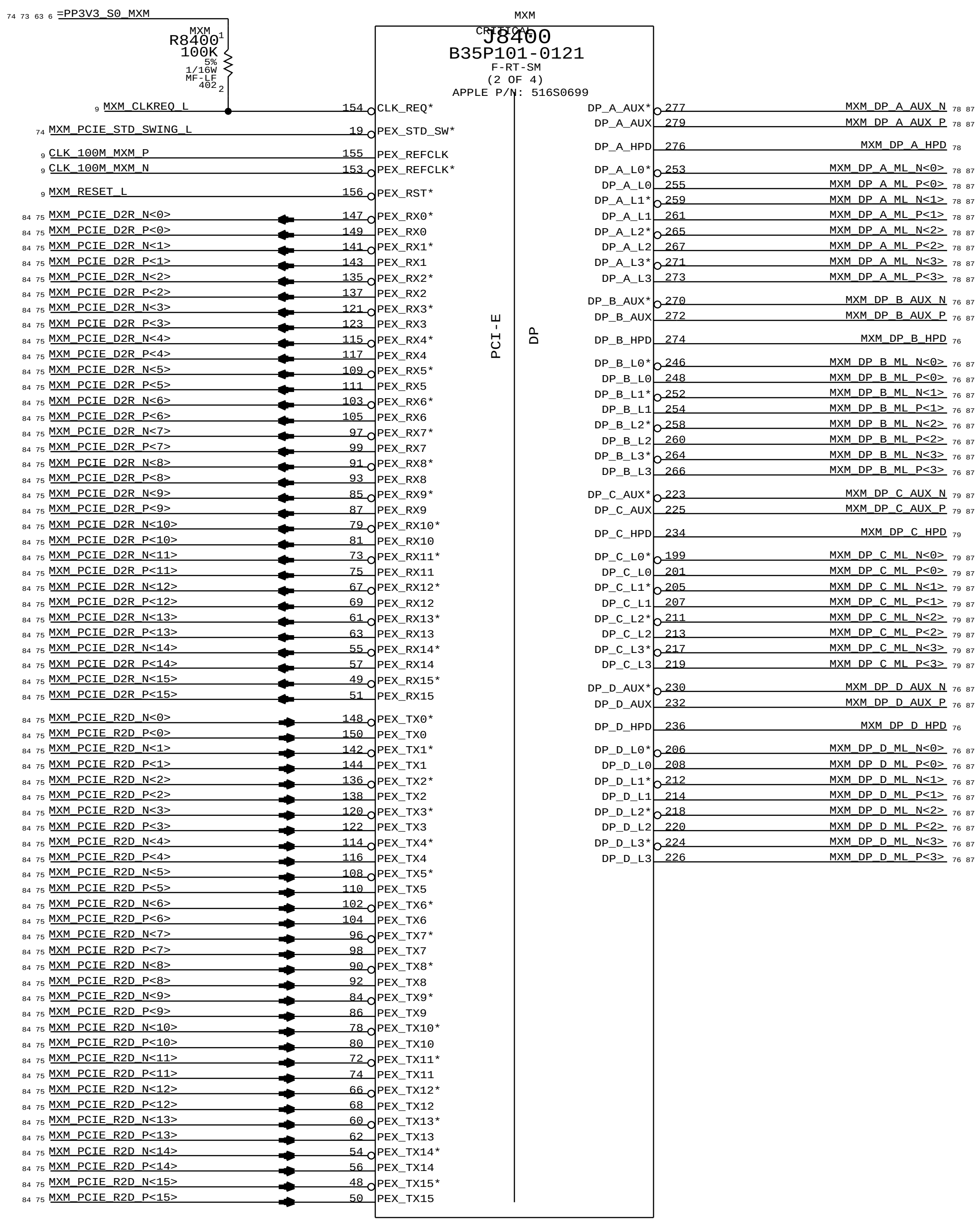
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

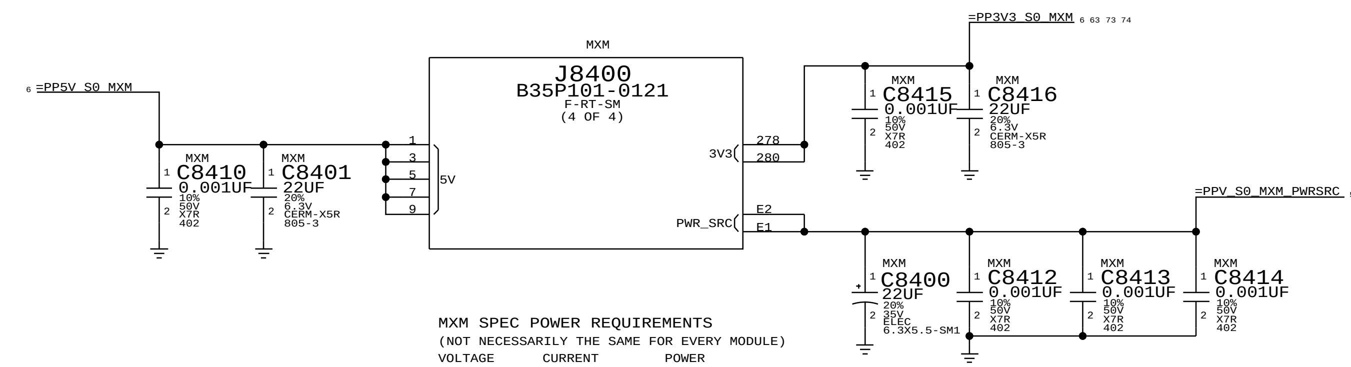
Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP5V_S0_MXM
- =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- MXM





MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.0 A	3.3 W
5V	2.5 A	12.5 W
PWR (7-20V)	UP TO 10 A	PLATFORM DEPENDENT

SYNC_MASTER=K23_AARON SYNC_DATE=07/16/2009

PAGE TITLE
MXM PCIe, DP & Power

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

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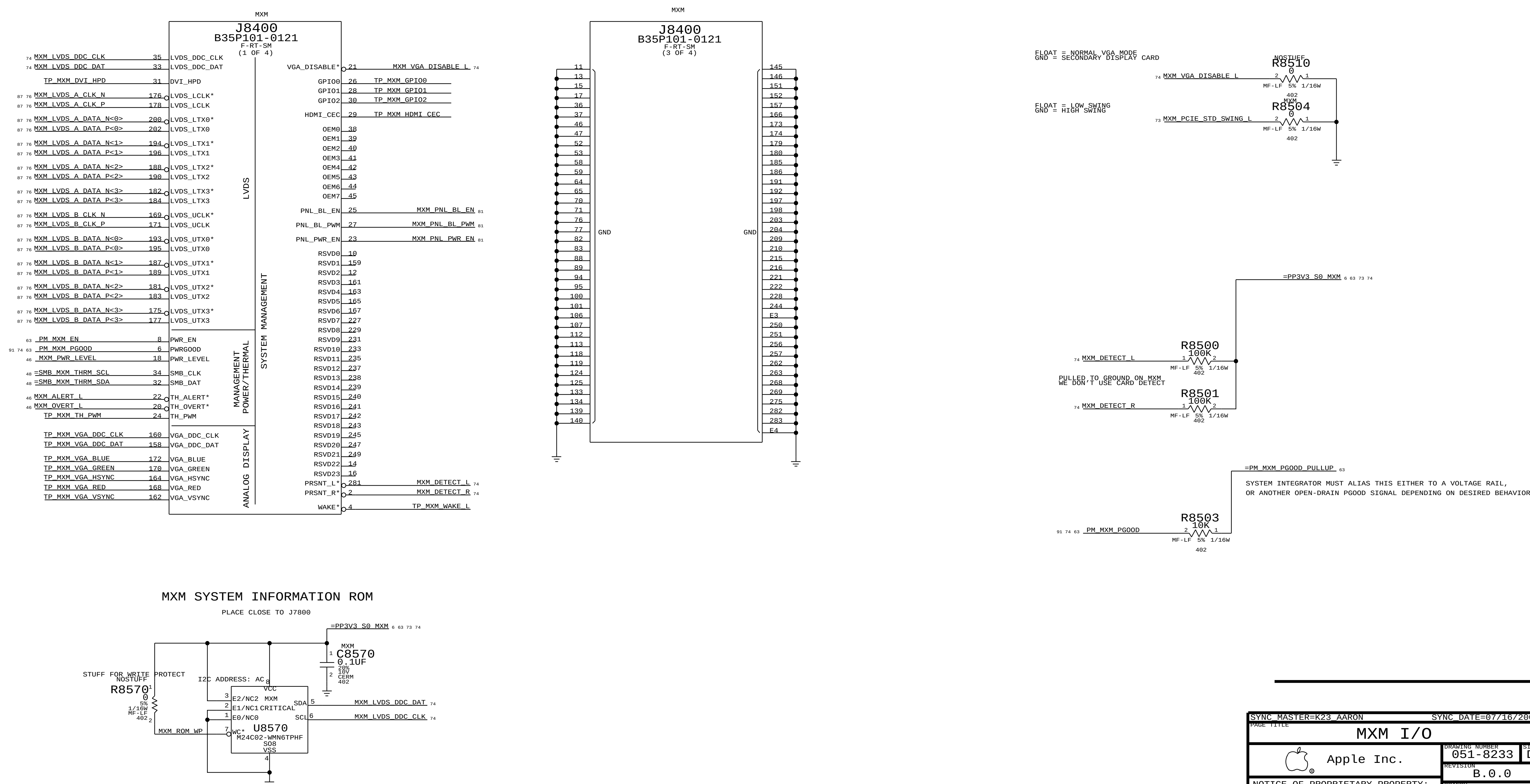
Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM

Signal aliases required by this page:
- =SMB_MXM_THRM_DATA - =PM_MXM_PGOOD_PULLUP
- =SMB_MXM_THRM_CLK

BOM options provided by this page:



SYNC_MASTER=K23_AARON SYNC_DATE=07/16/2009

PAGE TITLE

MXM I/O

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MXM TX CAPS

MXM RX CAPS

SYNC_MASTER=K60_AARON SYNC_DATE=07/01/2009

PAGE TITLE: MXM PCIE CAPS

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D

REVISION: B.0.0

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Page Notes

Power aliases required by this page:
- =PP3V3_S0_DP

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Unused MXM Interfaces

87 74	MXM_LVDS_A_CLK_N	NC_MXM_LVDS_A_CLK_N	MAKE_BASE=TRUE	NO_TEST=TRUE
87 74	MXM_LVDS_A_CLK_P	NC_MXM_LVDS_A_CLK_P	MAKE_BASE=TRUE	NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_N<0>	NC_MXM_LVDS_A_DATA_N<0>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_P<0>	NC_MXM_LVDS_A_DATA_P<0>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_N<1>	NC_MXM_LVDS_A_DATA_N<1>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_P<1>	NC_MXM_LVDS_A_DATA_P<1>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_N<2>	NC_MXM_LVDS_A_DATA_N<2>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_P<2>	NC_MXM_LVDS_A_DATA_P<2>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_N<3>	NC_MXM_LVDS_A_DATA_N<3>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_P<3>	NC_MXM_LVDS_A_DATA_P<3>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 74	MXM_LVDS_B_CLK_N	NC_MXM_LVDS_B_CLK_N	MAKE_BASE=TRUE	NO_TEST=TRUE
87 74	MXM_LVDS_B_CLK_P	NC_MXM_LVDS_B_CLK_P	MAKE_BASE=TRUE	NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_N<0>	NC_MXM_LVDS_B_DATA_N<0>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_P<0>	NC_MXM_LVDS_B_DATA_P<0>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_N<1>	NC_MXM_LVDS_B_DATA_N<1>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_P<1>	NC_MXM_LVDS_B_DATA_P<1>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_N<2>	NC_MXM_LVDS_B_DATA_N<2>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_P<2>	NC_MXM_LVDS_B_DATA_P<2>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_N<3>	NC_MXM_LVDS_B_DATA_N<3>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_P<3>	NC_MXM_LVDS_B_DATA_P<3>	MAKE_BASE=TRUE	NO_TEST=TRUE

Unused MXM DP Interfaces

87 73	MXM_DP_B_ML_P<0..3>	NC_MXM_DP_B_ML_P<0..3>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 73	MXM_DP_B_ML_N<0..3>	NC_MXM_DP_B_ML_N<0..3>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 73	MXM_DP_B_AUX_P	NC_MXM_DP_B_AUX_P	MAKE_BASE=TRUE	NO_TEST=TRUE
87 73	MXM_DP_B_AUX_N	NC_MXM_DP_B_AUX_N	MAKE_BASE=TRUE	NO_TEST=TRUE
73	MXM_DP_B_HPD	NC_MXM_DP_B_HPD	MAKE_BASE=TRUE	NO_TEST=TRUE
87 73	MXM_DP_D_ML_P<0..3>	NC_MXM_DP_D_ML_P<0..3>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 73	MXM_DP_D_ML_N<0..3>	NC_MXM_DP_D_ML_N<0..3>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 73	MXM_DP_D_AUX_P	NC_MXM_DP_D_AUX_P	MAKE_BASE=TRUE	NO_TEST=TRUE
87 73	MXM_DP_D_AUX_N	NC_MXM_DP_D_AUX_N	MAKE_BASE=TRUE	NO_TEST=TRUE
73	MXM_DP_D_HPD	NC_MXM_DP_D_HPD	MAKE_BASE=TRUE	NO_TEST=TRUE

Display: Aliases

SYNC_MASTER=K61_AARON SYNC_DATE=07/01/2009

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D	051-7997	3.0.0

Page Notes

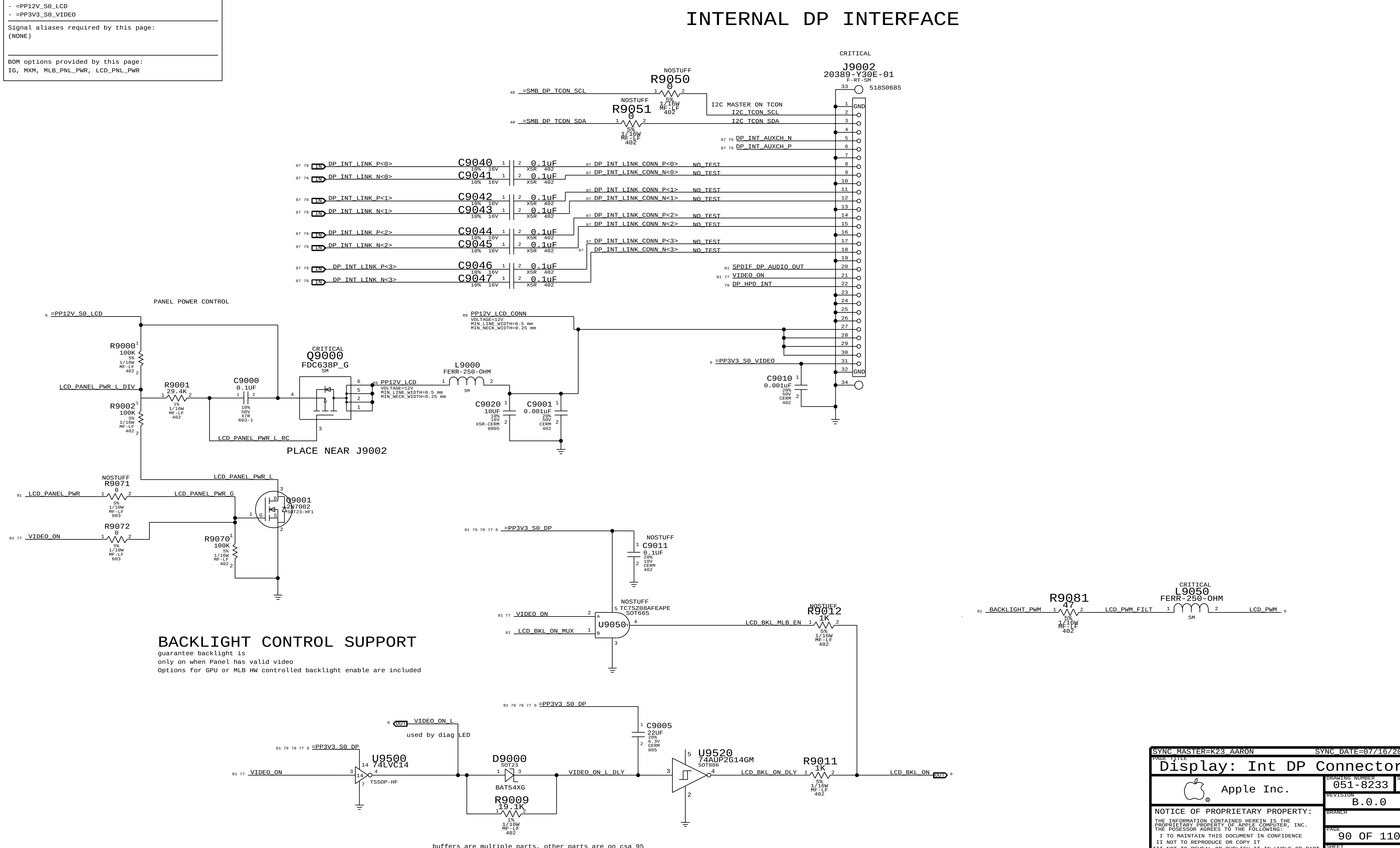
Power aliases required by this page:

- =PP12V_S0_LCD
- =PP3V3_S0_VIDEO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
IG, MXM, MLB_PNL_PWR, LCD_PNL_PWR

INTERNAL DP INTERFACE



SYNC_MASTER=K23_AARON SYNC_DATE=07/16/2009

PAGE TITLE
Display: Int DP Connector

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DRAWING NUMBER 051-8233 SIZE D

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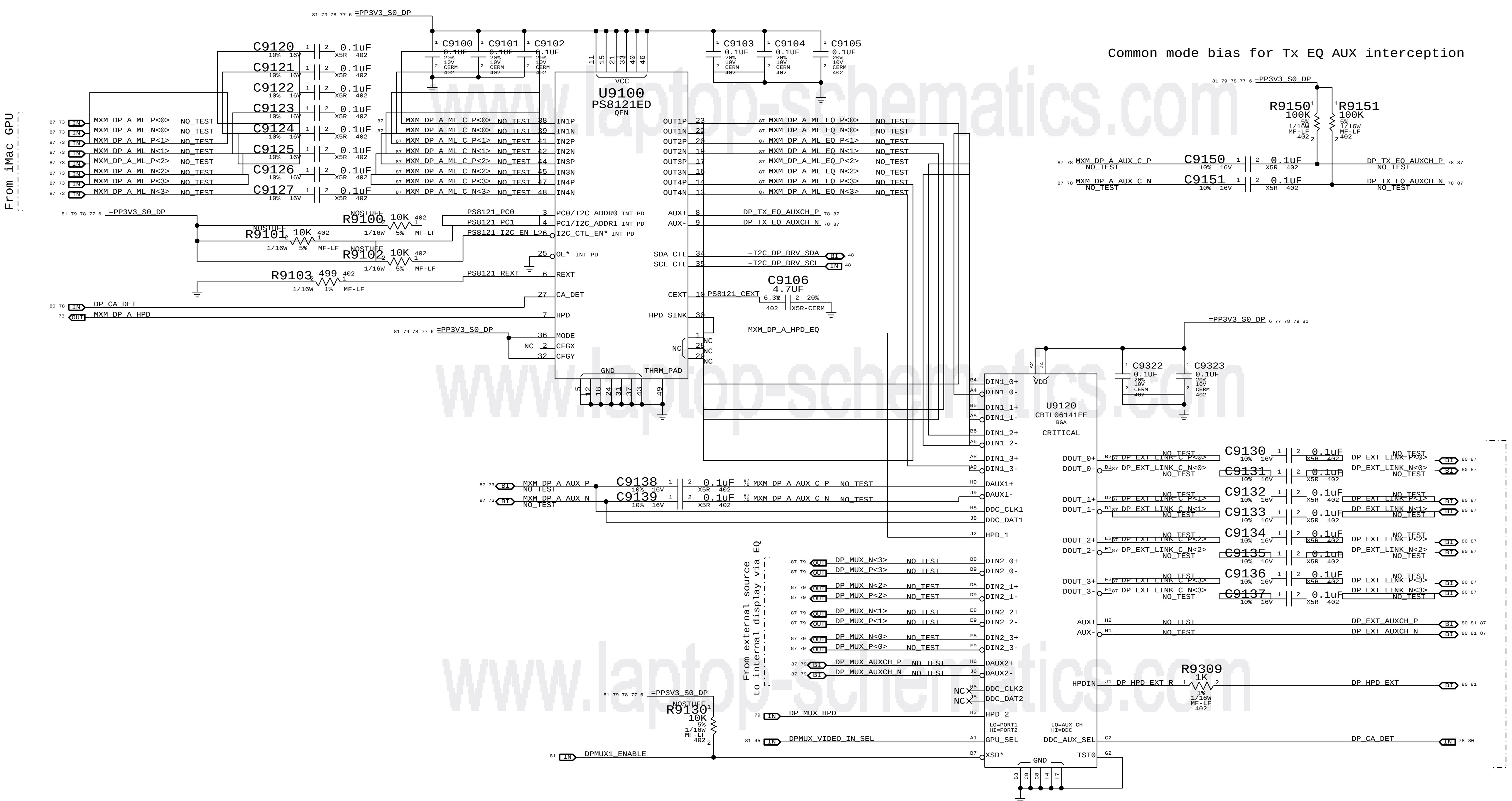
EQ & Re-Driver for DP source

Common mode bias for Tx EQ AUX interception



DisplayPort Mux 1
Analog mux at External Connector

SYNC_MASTER=K23_AARON	SYNC_DATE=07/16/2009
PAGE TITLE: Display: BiDiVi Mux1	
Apple Inc.	DRAWING NUMBER: 051-8233 SIZE: D
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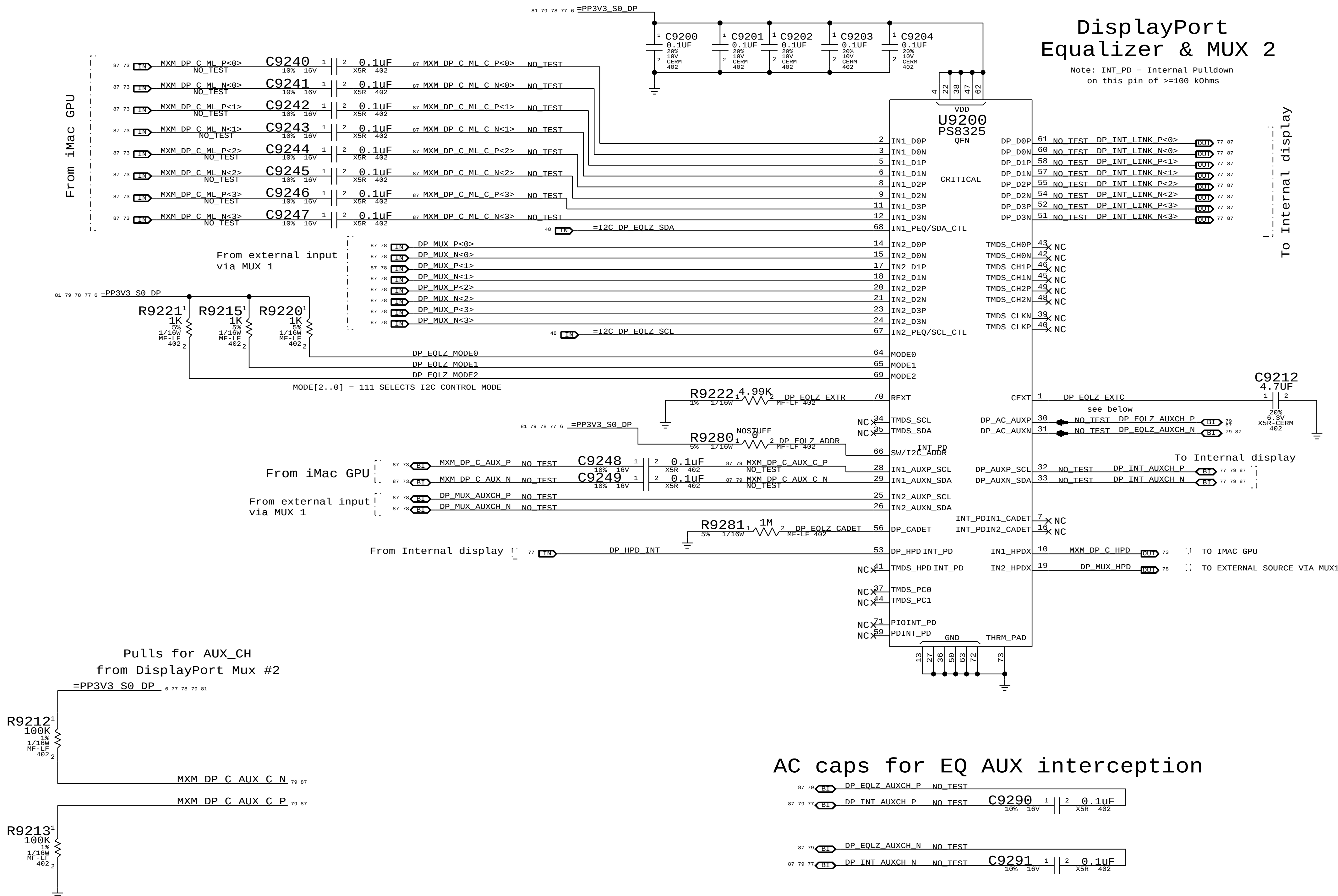

SYNC_MASTER=K23_AARON SYNC_DATE=07/16/2009

PAGE TITLE

BIDIVI DP MUX2

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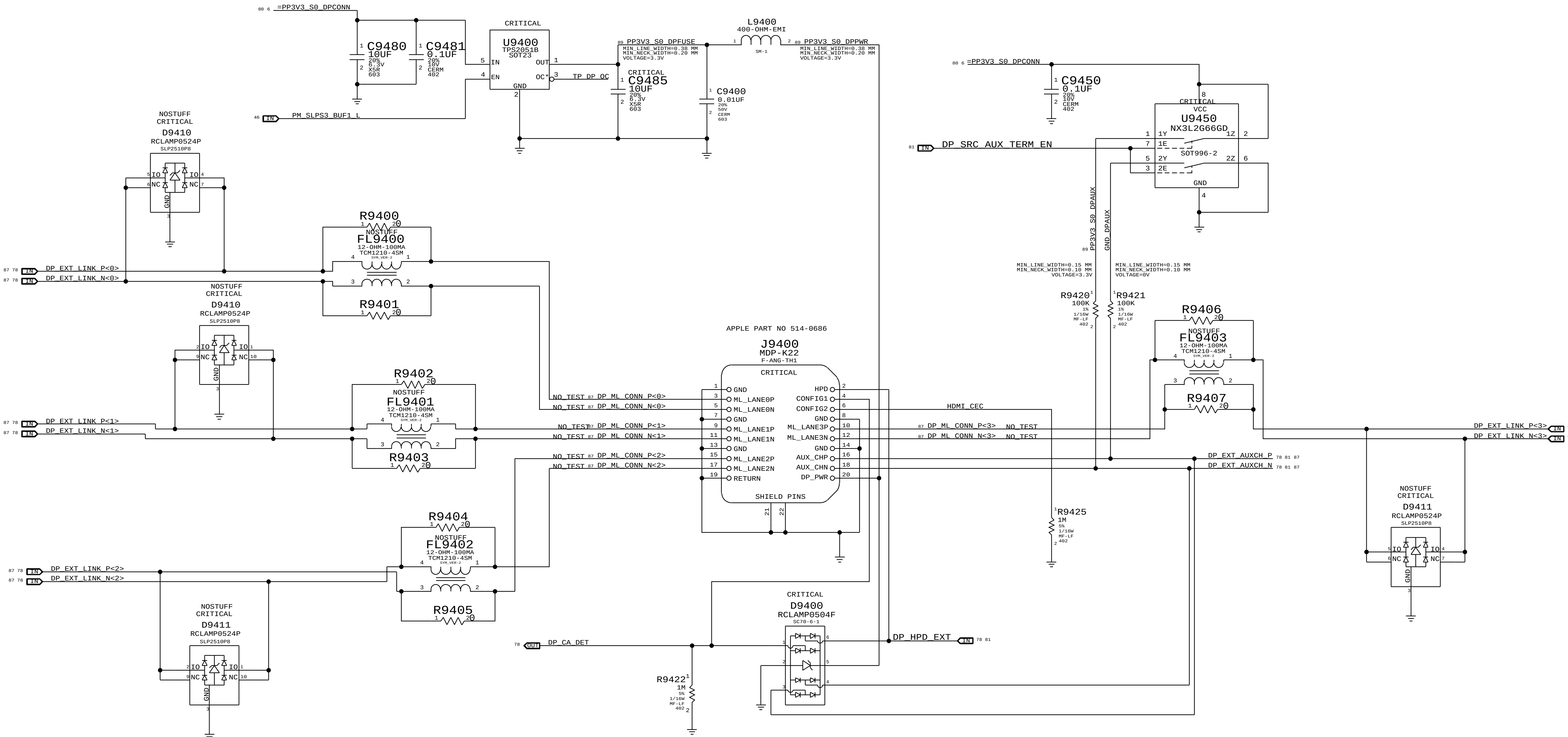
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC_MASTER=K23_AARON SYNC_DATE=07/16/2009

PAGE TITLE

Display: Ext DP Connector

DRAWING NUMBER 051-8233 SIZE D

REVISION B.0.0

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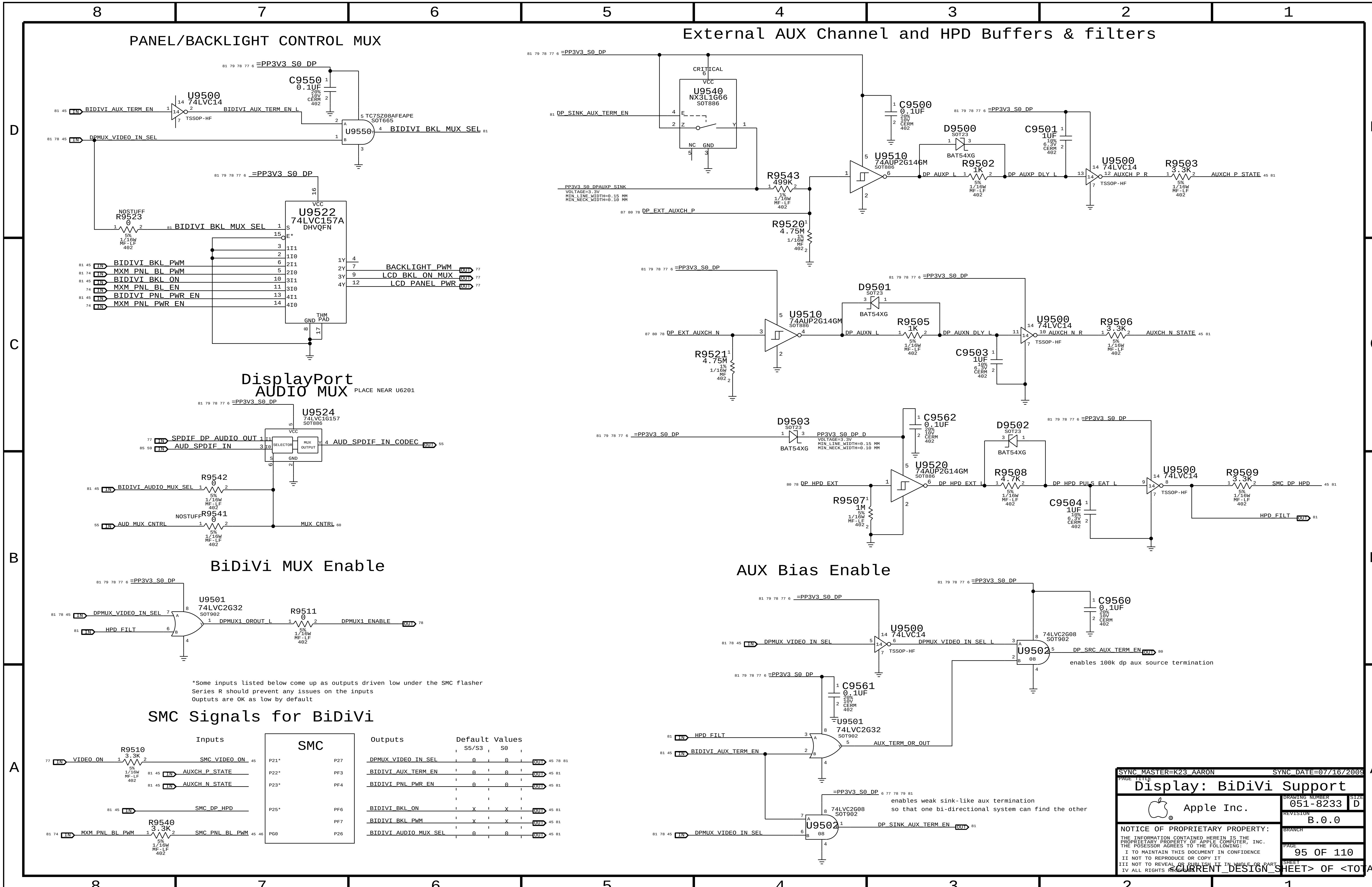

SYNC_MASTER=K23_AARON SYNC_DATE=07/16/2009

PAGE TITLE

Display: BiDiVi Support

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

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K60/K61 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	100 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.21 MM	0.085 MM	=STANDARD		
35_OHM_SE	*	Y	0.19 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39_OHM_SE	TOP,BOTTOM	Y	0.175 MM	0.085 MM	=STANDARD		
39_OHM_SE	*	Y	0.16 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.085 MM	=STANDARD		
45_OHM_SE	*	Y	0.12 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.1 MM	0.085 MM	15 MM		
50_OHM_SE	*	Y	0.1 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD		
55_OHM_SE	*	Y	0.076 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL6	Y	0.155 MM	0.085 MM	=STANDARD	0.135 MM	0.1 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.085 MM	=STANDARD	0.130 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL6	Y	0.115 MM	0.085 MM	=STANDARD	0.2 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.2 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL6	Y	0.099 MM	0.085 MM	12 MM	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.110 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL6	Y	0.081 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.085 MM	=STANDARD	0.320 MM	0.15 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM
POWER_WIDTH	*	Y	0.600 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
POWER_CTL	*	Y	0.300 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER	BGA_P1MM	POWER_CTL
POWER	*	POWER_WIDTH
VR_CTL_PHY	BGA_P1MM	DEFAULT
VR_CTL_PHY	*	POWER_CTL

SPACING RULE SET

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?
6:1_SPACING	*	0.6 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000
SWITCHNODE	*	0.8 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.150 MM	?
2X_DIELECTRIC	TOP,BOTTOM	0.160 MM	?
3X_DIELECTRIC	*	0.220 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.240 MM	?
4X_DIELECTRIC	*	0.300 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.320 MM	?
5X_DIELECTRIC	*	0.380 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.400 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	*	*	STANDARD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER	*	*	STANDARD

CONSTRAINTS FOR BGA AREA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	0.2 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P1MM
CLK_LPC	*	BGA_P1MM	BGA_P1MM
CLK_PCI	*	BGA_P1MM	BGA_P1MM

K60/K61 RULE DEFINITIONS

SYNC_MASTER=K60_DEREK SYNC_DATE=07/01/2009

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7997	3.0.0

SCALE	SHT	OF
NONE	82	92

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_39S	*	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=STANDARD	=STANDARD
MEM_35S	*	=35_OHM_SE	=35_OHM_SE	=35_OHM_SE	=35_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DQ_ODD2DQ_ODD	*	=3:1_SPACING	?
MEM_DQ_ODD2MEM	*	=3:1_SPACING	?
MEM_DQ_EVEN2DQ_EVEN	*	=3:1_SPACING	?
MEM_DQ_EVEN2MEM	*	=3:1_SPACING	?
MEM_DQ_EVEN2DQ_ODD	*	=5:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	=3:1_SPACING	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DQ_ODD	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM
MEM_CLK	MEM_DQ_EVEN	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_ODD	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_EVEN	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_ODD	MEM_CLK	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_CTRL	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_CMD	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_DQ_ODD	*	MEM_DQ_ODD2DQ_ODD
MEM_DQ_ODD	MEM_DQS	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_DQ_EVEN	*	MEM_DQ_EVEN2DQ_ODD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_EVEN	MEM_CLK	*	MEM_DQ_EVEN2MEM
MEM_DQ_EVEN	MEM_CTRL	*	MEM_DQ_EVEN2MEM
MEM_DQ_EVEN	MEM_CMD	*	MEM_DQ_EVEN2MEM
MEM_DQ_EVEN	MEM_DQ_EVEN	*	MEM_DQ_EVEN2DQ_EVEN
MEM_DQ_EVEN	MEM_DQS	*	MEM_DQ_EVEN2MEM
MEM_DQ_EVEN	MEM_DQ_ODD	*	MEM_DQ_EVEN2DQ_ODD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQ_ODD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQ_EVEN	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DQ_ODD	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM
MEM_CMD	MEM_DQ_EVEN	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DQ_ODD	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER
MEM_DQ_EVEN	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_POWER_WIDTH	*	Y	0.500 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_POWER_PHY	*	MEM_POWER_WIDTH

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_POWER	*	0.2 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_RCOMP_PHY	*	Y	0.175 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_RCOMP	*	0.2 MM	?

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
	MEM_70D	MEM_CLK	MEM_A_CLK_P<3..0>	12 32
	MEM_70D	MEM_CLK	MEM_A_CLK_N<3..0>	12 32
	MEM_39S	MEM_CTRL	MEM_A_CKE<3..0>	12 30
	MEM_39S	MEM_CTRL	MEM_A_CS_L<3..0>	12 30
	MEM_39S	MEM_CTRL	MEM_A_ODT<3..0>	12 30
	MEM_35S	MEM_CMD	MEM_A_A<15..0>	12 30
	MEM_35S	MEM_CMD	MEM_A_BA<2..0>	12 30
	MEM_35S	MEM_CMD	MEM_A_RAS_L	12 30
	MEM_35S	MEM_CMD	MEM_A_CAS_L	12 30
	MEM_35S	MEM_CMD	MEM_A_WE_L	12 30
	MEM_45S	MEM_DQ_EVEN	MEM_A_DQ<7..0>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DM<0>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DQ<15..8>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DM<1>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DQ<23..16>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DM<2>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DQ<31..24>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DM<3>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DQ<39..32>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DM<4>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DQ<47..40>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DM<5>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DQ<55..48>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DM<6>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DQ<63..56>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DM<7>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	12 32
	MEM_70D	MEM_CLK	MEM_B_CLK_P<3..0>	12 32
	MEM_70D	MEM_CLK	MEM_B_CLK_N<3..0>	12 32
	MEM_39S	MEM_CTRL	MEM_B_CKE<3..0>	12 31
	MEM_39S	MEM_CTRL	MEM_B_CS_L<3..0>	12 31
	MEM_39S	MEM_CTRL	MEM_B_ODT<3..0>	12 31
	MEM_35S	MEM_CMD	MEM_B_A<15..0>	12 31
	MEM_35S	MEM_CMD	MEM_B_BA<2..0>	12 31
	MEM_35S	MEM_CMD	MEM_B_RAS_L	12 31
	MEM_35S	MEM_CMD	MEM_B_CAS_L	12 31
	MEM_35S	MEM_CMD	MEM_B_WE_L	12 31
	MEM_45S	MEM_DQ_EVEN	MEM_B_DQ<7..0>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DM<0>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DQ<15..8>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DM<1>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DQ<23..16>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DM<2>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DQ<31..24>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DM<3>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DQ<39..32>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DM<4>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DQ<47..40>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DM<5>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DQ<55..48>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DM<6>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DQ<63..56>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DM<7>	12 32

MEMORY POWER PROPERTIES

VOLTAGE	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
I155	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_A	12 28
I154	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_B	12 28
I166	MEM_POWER_PHY	MEM_POWER	VREFMARGIN_DIMMA_DQ	28
I167	MEM_POWER_PHY	MEM_POWER	VREFMARGIN_DIMMB_DQ	28
I169	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_A_SW	28
I168	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_B_SW	28

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	12 32
I160	MEM_RCOMP_PHY	MEM_RCOMP	CPU_SM_RCOMP0	11
I159	MEM_RCOMP_PHY	MEM_RCOMP	CPU_SM_RCOMP1	11
I161	MEM_RCOMP_PHY	MEM_RCOMP	CPU_SM_RCOMP2	11
I162	MEM_70D	MEM_DQS	TP_MEM_B_DQS_P<8>	8 12
I163	MEM_70D	MEM_DQS	TP_MEM_B_DQS_N<8>	8 12
I164	MEM_70D	MEM_DQS	TP_MEM_A_DQS_P<8>	8 12
I165	MEM_70D	MEM_DQS	TP_MEM_A_DQS_N<8>	8 12

ADD RULES TO NC_DQS<8>
TO CLEAR CHECK_PLUS ERRORS

SYNC_MASTER=K60_MIKE SYNC_DATE=07/01/2009

PAGE TITLE
Memory Constraints

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

REVISION B.0.0

BRANCH

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=4X_DIELECTRIC	?
CLK_PCIE	*	0.5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

CPU

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_ITP	*	0.2 MM	?
CPU_RCOMP	*	0.2 MM	?

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=5X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=5X_DIELECTRIC	?

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
FDI_MISC	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	
	CPU_50S	CPU_AGTL	FDI_INT	
SATA SSD	SATA_85D	SATA	SATA_SSD_R2D_C_P	18 42
	SATA_85D	SATA	SATA_SSD_R2D_C_N	18 42
	SATA_85D	SATA	SATA_SSD_R2D_P	42
	SATA_85D	SATA	SATA_SSD_R2D_N	42
	SATA_85D	SATA	SATA_SSD_D2R_P	18 42
	SATA_85D	SATA	SATA_SSD_D2R_N	18 42
	SATA_85D	SATA	SATA_SSD_D2R_C_P	42
	SATA_85D	SATA	SATA_SSD_D2R_C_N	42
CLOCKS	CLK_PCIE_100D	CLK_PCIE	DMI_MIDBUS_CLK100M_P	10 18
	CLK_PCIE_100D	CLK_PCIE	DMI_MIDBUS_CLK100M_N	10 18
CPU ITP	CPU_50S	CPU_ITP	XDP_BPM_L<7..0>	11 25
	CPU_50S	CPU_ITP	CPU_CFG<17..0>	10 15 25
	CPU_50S	CPU_ITP	XDP_OBSDATA_A<3..0>	25
CPU_MISC	CPU_50S	CPU_RCOMP	CPU_PEG_COMP	10
	CPU_50S	CPU_RCOMP	CPU_PEG_RBIAS	10
	CPU_50S	CPU_RCOMP	CPU_COMP3	11
	CPU_50S	CPU_RCOMP	CPU_COMP2	11
	CPU_50S	CPU_RCOMP	CPU_COMP1	11
	CPU_50S	CPU_RCOMP	CPU_COMP0	11

ANY OTHER LYNNFIELD CONSTRAINTS NOT COVERED ON PAGES 101 AND 107 SHOULD GO ON THIS PAGE TOO

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
PCIE GRAPHICS	PCIE_85D	PCIE	PEG_R2D_C_P<15..0>	9 75
	PCIE_85D	PCIE	PEG_R2D_C_N<15..0>	9 75
	PCIE_85D	PCIE	PEG_D2R_P<15..0>	9 75
	PCIE_85D	PCIE	PEG_D2R_N<15..0>	9 75
	PCIE_85D	PCIE	MXM_PCIE_R2D_P<15..0>	73 75
	PCIE_85D	PCIE	MXM_PCIE_R2D_N<15..0>	73 75
	PCIE_85D	PCIE	MXM_PCIE_D2R_P<15..0>	73 75
	PCIE_85D	PCIE	MXM_PCIE_D2R_N<15..0>	73 75
PCIE I/O	PCIE_85D	PCIE	PCIE_MINI_R2D_P	33
	PCIE_85D	PCIE	PCIE_MINI_R2D_N	33
	PCIE_85D	PCIE	PCIE_MINI_R2D_C_P	18 33
	PCIE_85D	PCIE	PCIE_MINI_R2D_C_N	18 33
	PCIE_85D	PCIE	PCIE_MINI_D2R_P	18 33
	PCIE_85D	PCIE	PCIE_MINI_D2R_N	18 33
	PCIE_85D	PCIE	PCIE_MINI_R2D_L_P	33
	PCIE_85D	PCIE	PCIE_MINI_R2D_L_N	33
	PCIE_85D	PCIE	PCIE_FW_R2D_P	39
	PCIE_85D	PCIE	PCIE_FW_R2D_N	39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	18 39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_P	18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_N	18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	39
DMI	PCIE_85D	PCIE	DMI_S2N_P<3..0>	10 19
	PCIE_85D	PCIE	DMI_S2N_N<3..0>	10 19
	PCIE_85D	PCIE	DMI_N2S_P<3..0>	10 19
	PCIE_85D	PCIE	DMI_N2S_N<3..0>	10 19
FDI	PCIE_85D	PCIE	FDI_DATA_N<7..0>	
	PCIE_85D	PCIE	FDI_DATA_P<15..0>	
PCIE REF CLOCKS	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_P	9
	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_N	9
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CON_P	33
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CON_N	33
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	18 33
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	18 33
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	18 39
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	18 39
	ENET_100D	ENET_MII	PCIE_CLK100M_ENET_P	18 36
	ENET_100D	ENET_MII	PCIE_CLK100M_ENET_N	18 36
SATA	SATA_85D	SATA	SATA_HDD_R2D_C_P	18 42
	SATA_85D	SATA	SATA_HDD_R2D_C_N	18 42
	SATA_85D	SATA	SATA_HDD_R2D_P	42 92
	SATA_85D	SATA	SATA_HDD_R2D_N	42 92
	SATA_85D	SATA	SATA_HDD_D2R_P	18 42
	SATA_85D	SATA	SATA_HDD_D2R_N	18 42
	SATA_85D	SATA	SATA_HDD_D2R_C_P	42 92
	SATA_85D	SATA	SATA_HDD_D2R_C_N	42 92
	SATA_85D	SATA	SATA_ODD_R2D_C_P	18 42
	SATA_85D	SATA	SATA_ODD_R2D_C_N	18 42
	SATA_85D	SATA	SATA_ODD_R2D_P	42 92
	SATA_85D	SATA	SATA_ODD_R2D_N	42 92
	SATA_85D	SATA	SATA_ODD_D2R_P	18 42
	SATA_85D	SATA	SATA_ODD_D2R_N	18 42
	SATA_85D	SATA	SATA_ODD_D2R_C_P	42 92
	SATA_85D	SATA	SATA_ODD_D2R_C_N	42 92
CLOCKS	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_CPU_P	11 21
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_CPU_N	11 21
	CLK_PCIE_100D	CLK_PCIE	GFX_CLK120M_DPLLSS_P	11 18
	CLK_PCIE_100D	CLK_PCIE	GFX_CLK120M_DPLLSS_N	11 18
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_ITP_P	11 25
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_ITP_N	11 25
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_CPU_P	11 18
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_CPU_N	11 18
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_PCH_P	18 26
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_PCH_N	18 26
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_PCH_P	18 26
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_PCH_N	18 26
	CLK_PCIE_100D	CLK_PCIE	PCH_CLK96M_DOT_P	18 26
	CLK_PCIE_100D	CLK_PCIE	PCH_CLK96M_DOT_N	
	CLK_PCIE_100D	CLK_PCIE	PCH_CLK100M_SATA_P	18 26
	CLK_PCIE_100D	CLK_PCIE	PCH_CLK100M_SATA_N	18 26

SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE
PCIE/DMI/FDI/SATA CONSTRAINTS

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
REVISION B.0.0
BRANCH

PCH CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH	*	0.2 MM	?
COMP_PCH	*	0.2 MM	?

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	0.2 MM	?

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	0.15 MM	?
CLK_LPC	*	0.2 MM	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	0.2 MM	?

XTAL Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
	PCI_55S	PCI	PCI_REQ0_L	20
	PCI_55S	PCI	PCI_REQ1_L	20
	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIOUT	20 27
	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIIN	18 27
	LPC_55S	LPC	LPC_AD<3..0>	18 45 47
	LPC_55S	LPC	LPC_FRAME_L	18 45 47
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	20 27
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	27 45
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	27 47
	CLK_LPC_55S	PM	PM_CLK32K_SUSCLK_R	9 19 91
	CLK_LPC_55S	PM	PM_CLK32K_SUSCLK	9 45 91
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	20 27
	USB_90D	USB	USB_EXTA_P	34 43
	USB_90D	USB	USB_EXTA_N	34 43
	USB_90D	USB	USB_PORT0_P	43
	USB_90D	USB	USB_PORT0_N	43
	USB_90D	USB	USB_EXTB_P	35 43
	USB_90D	USB	USB_EXTB_N	35 43
	USB_90D	USB	USB_PORT1_P	43
	USB_90D	USB	USB_PORT1_N	43
	USB_90D	USB	USB_EXTC_P	34 43
	USB_90D	USB	USB_EXTC_N	34 43
	USB_90D	USB	USB_PORT2_P	43
	USB_90D	USB	USB_PORT2_N	43
	USB_90D	USB	USB_EXTD_P	35 43
	USB_90D	USB	USB_EXTD_N	35 43
	USB_90D	USB	USB_D_MUXED_P	43
	USB_90D	USB	USB_D_MUXED_N	43
	USB_90D	USB	USB_PORT3_P	43
	USB_90D	USB	USB_PORT3_N	43
	USB_90D	USB	USB_CAMERA_P	34 44
	USB_90D	USB	USB_CAMERA_N	34 44
	USB_90D	USB	USB_CAMERA_L_P	44 92
	USB_90D	USB	USB_CAMERA_L_N	44 92
	USB_90D	USB	USB_BT_P	35 44
	USB_90D	USB	USB_BT_N	35 44
	USB_90D	USB	USB_BT_L_P	44 92
	USB_90D	USB	USB_BT_L_N	44 92
	USB_90D	USB	USB_IR_P	34 44
	USB_90D	USB	USB_IR_N	34 44
	USB_90D	USB	USB_IR_L_P	44 92
	USB_90D	USB	USB_IR_L_N	44 92
	USB_90D	USB	USB_SDCARD_P	35 44
	USB_90D	USB	USB_SDCARD_N	35 44
	USB_90D	USB	USB_SDCARD_L_P	44 92
	USB_90D	USB	USB_SDCARD_L_N	44 92
	USB_90D	USB	USB_WM_P	20 44
	USB_90D	USB	USB_WM_N	20 44
	USB_90D	USB	USB_WM_L_P	44
	USB_90D	USB	USB_WM_L_N	44
	USB_90D	USB	USB_MINI_P	
	USB_90D	USB	USB_MINI_N	
	USB_90D	USB	USB_BRCRYPT_P	20 44
	USB_90D	USB	USB_BRCRYPT_N	20 44
	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1	18 27
	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2	18 27
	CLK_XTAL	XTAL	CK505_XTAL_IN	26
	CLK_XTAL	XTAL	CK505_XTAL_OUT	26
	CLK_PCH_55S	CLK_PCH	PCH_CLK14P3M_REFCLK	18 26
	USB_90D	USB	USB_BRCRYPT_L_P	44
	USB_90D	USB	USB_BRCRYPT_L_N	44
	USB_90D	USB	USB_HUB1_UP_P	20 34
	USB_90D	USB	USB_HUB1_UP_N	20 34
	USB_90D	USB	USB_HUB2_UP_P	20 35
	USB_90D	USB	USB_HUB2_UP_N	20 35

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
	SPI_55S	SPI	SPI_CLK_R	18 47 54
	SPI_55S	SPI	SPI_CLK	54
	SPI_55S	SPI	SPI_MOSI_R	18 47 54
	SPI_55S	SPI	SPI_MOSI	54
	SPI_55S	SPI	SPI_MISO	18 47 54
	SPI_55S	SPI	SPI_MISO_R	54
	SPI_55S	SPI	SPI_CS0_R_L	18 47
	SPI_55S	SPI	SPI_CS0_L	47
	SPI_55S	SPI	SPI_MLB_CS_L	47 54
	SPI_55S	SPI	SPI_ALT_CS_L	47
	SPI_55S	SPI	SPIROM_USE_MLB	21 47
	SPI_55S	SPI	SPI_ALT_MOSI	47
	SPI_55S	SPI	SPI_ALT_MISO	47
	SPI_55S	SPI	SPI_ALT_CLK	47
	HDA_55S	HDA	HDA_BIT_CLK	18 55
	HDA_55S	HDA	HDA_BIT_CLK_R	18
	HDA_55S	HDA	HDA_RST_L	18 55
	HDA_55S	HDA	HDA_RST_R_L	18
	HDA_55S	HDA	HDA_SDOUT	18 55
	HDA_55S	HDA	HDA_SDOUT_R	18
	HDA_55S	HDA	HDA_SYNC	18 55
	HDA_55S	HDA	HDA_SYNC_R	18
	HDA_55S	HDA	HDA_SDIN0	18 55
	HDA_55S	HDA	AUD_SDI_R	55
		HDA	AUD_SPDIF_IN	59 81
		HDA	AUD_SPDIF_OUT	55 59
		HDA	AUD_SPDIF_CHIP	55
	HDA_55S	HDA	AUD_SPKR_OUTL01L_NOUT	57 59 92
	HDA_55S	HDA	AUD_SPKR_OUTL01L_POUT	57 59 92
	HDA_55S	HDA	AUD_SPKR_OUTL01R_NOUT	57 59 92
	HDA_55S	HDA	AUD_SPKR_OUTL01R_POUT	57 59 92
	HDA_55S	HDA	AUD_SPKR_OUTL02L_NOUT	58 59 92
	HDA_55S	HDA	AUD_SPKR_OUTL02L_POUT	58 59 92
	HDA_55S	HDA	AUD_SPKR_OUTL02R_NOUT	58 59 92
	HDA_55S	HDA	AUD_SPKR_OUTL02R_POUT	58 59 92
	CLK_XTAL	XTAL	PCH_CLK25M_XTALOUT	18 27
	CLK_XTAL	XTAL	PCH_CLK25M_XTALIN	18 27
	PCH_55S	COMP_PCH	PCH_USB_RBIAS	20
	PCH_55S	COMP_PCH	PCH_SATAICOMP	18
	PCH_55S	COMP_PCH	PCH_XCLK_RCOMP	18
	PCH_55S	COMP_PCH	PCH_DMI_COMP	19
	CLK_XTAL	XTAL	USB_HUB1_XTAL1	34
	CLK_XTAL	XTAL	USB_HUB1_XTAL2	34
	PCH_55S	COMP_PCH	USB_HUB1_RBIAS	34
	CLK_XTAL	XTAL	USB_HUB2_XTAL1	35
	CLK_XTAL	XTAL	USB_HUB2_XTAL2	35
	PCH_55S	COMP_PCH	USB_HUB2_RBIAS	35

SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE
IBEX PEAK CONSTRAINTS

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
REVISION B.0.0
BRANCH

CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	0.3 MM	?
ENET_SE	*	=STANDARD	?

SOURCE:BROADCOM 5764M-DS04-RDS. PAGE 38

CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_DIFF	*	0.6 MM	?

SOURCE: BROADCOM 5764-DS04-RDS. PAGE 38

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
	ENET_50S	ENET_SE	ENET_RDAC	36
	ENET_50S	BUF0_CLK	ENET_CLK25M_XTALI	36
	ENET_50S	BUF0_CLK	ENET_CLK25M_XTALO	36
	ENET_50S	BUF0_CLK	ENET_CLK25M_XTAL	36
	ENET_100D	ENET_DIFF	ENET_MDI_P<3..0>	36 38
	ENET_100D	ENET_DIFF	ENET_MDI_N<3..0>	36 38
	ENET_100D	ENET_DIFF	ENET_MDI_T_P<3..0>	38
	ENET_100D	ENET_DIFF	ENET_MDI_T_N<3..0>	38
	ENET_100D	ENET_MII	PCIE_ENET_R2D_P	36
	ENET_100D	ENET_MII	PCIE_ENET_R2D_N	36
	ENET_100D	ENET_MII	PCIE_ENET_D2R_P	18 36
	ENET_100D	ENET_MII	PCIE_ENET_D2R_N	18 36
	ENET_100D	ENET_MII	PCIE_ENET_R2D_C_P	18 36
	ENET_100D	ENET_MII	PCIE_ENET_R2D_C_N	18 36
	ENET_100D	ENET_MII	PCIE_ENET_D2R_C_P	36
	ENET_100D	ENET_MII	PCIE_ENET_D2R_C_N	36

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
	FW_110D	FW_TP	FW_PORT0_TPA_P	40 41
	FW_110D	FW_TP	FW_PORT0_TPA_N	40 41
	FW_110D	FW_TP	FW_PORT0_TPB_P	40 41
	FW_110D	FW_TP	FW_PORT0_TPB_N	40 41

PORT 1 & 2 NOT USED

	FW_110D	FW_TP	FW_P0_TPA_L_P	40
	FW_110D	FW_TP	FW_P0_TPA_L_N	40
	FW_110D	FW_TP	FW_P0_TPB_L_P	40
	FW_110D	FW_TP	FW_P0_TPB_L_N	40

UNUSED FW NETS PHYSICAL PROPERTIES

	FW_110D	FW_TP	FW_P1_TPA_P	39 40
	FW_110D	FW_TP	FW_P1_TPA_N	39 40
	FW_110D	FW_TP	FW_P2_TPA_P	39 40
	FW_110D	FW_TP	FW_P2_TPA_N	39 40

AUDIO MIC PHYSICAL PROPERTIES

	AUDIO_PHY	AUDIO	AUD_MIC1_IN_N	59 60
	AUDIO_PHY	AUDIO	AUD_MIC1_IN_P	59 60

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIO_PHY	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	=STANDARD	?

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ENET/FIREWIRE CONSTRAINTS

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.08MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3:1_SPACING	?

PAIRS SHOULD BE WITHIN 100 MILS OF CLOCK LENGTH.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
ASSINGED IN CONT. MGR.				
	DP_85D	DISPLAYPORT	DP_ML_CONN_P<3..0>	80
	DP_85D	DISPLAYPORT	DP_ML_CONN_N<3..0>	80
	DP_85D	DISPLAYPORT	DP_INT_LINK_CONN_P<3..0>	77
	DP_85D	DISPLAYPORT	DP_INT_LINK_CONN_N<3..0>	77
	DP_85D	DISPLAYPORT	DP_INT_LINK_P<3..0>	77 79
	DP_85D	DISPLAYPORT	DP_INT_LINK_N<3..0>	77 79
	DP_85D	DISPLAYPORT	DP_INT_AUXCH_P	77 79
	DP_85D	DISPLAYPORT	DP_INT_AUXCH_N	77 79
	DP_85D	DISPLAYPORT	DP_EXT_LINK_P<3..0>	78 80
	DP_85D	DISPLAYPORT	DP_EXT_LINK_N<3..0>	78 80
	DP_85D	DISPLAYPORT	DP_EXT_AUXCH_P	78 80 81
	DP_85D	DISPLAYPORT	DP_EXT_AUXCH_N	78 80 81
	DP_85D	DISPLAYPORT	DP_EXT_LINK_C_P<3..0>	78
	DP_85D	DISPLAYPORT	DP_EXT_LINK_C_N<3..0>	78
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_P<3..0>	73 78
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_N<3..0>	73 78
	DP_85D	DISPLAYPORT	MXM_DP_A_AUX_C_P	78
	DP_85D	DISPLAYPORT	MXM_DP_A_AUX_C_N	78
	DP_85D	DISPLAYPORT	MXM_DP_A_AUX_P	73 78
	DP_85D	DISPLAYPORT	MXM_DP_A_AUX_N	73 78
	DP_85D	DISPLAYPORT	MXM_DP_C_ML_P<3..0>	73 79
	DP_85D	DISPLAYPORT	MXM_DP_C_ML_N<3..0>	73 79
	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_P	73 79
	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_N	73 79
	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_C_P	79
	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_C_N	79
	DP_85D	DISPLAYPORT	DP_MUX_P<3..0>	78 79
	DP_85D	DISPLAYPORT	DP_MUX_N<3..0>	78 79
	DP_85D	DISPLAYPORT	DP_MUX_AUXCH_P	78 79
	DP_85D	DISPLAYPORT	DP_MUX_AUXCH_N	78 79
	DP_85D	DISPLAYPORT	DP_EQLZ_AUXCH_P	79
	DP_85D	DISPLAYPORT	DP_EQLZ_AUXCH_N	79
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_C_P<3..0>	78
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_C_N<3..0>	78
	DP_85D	DISPLAYPORT	MXM_DP_C_ML_C_P<3..0>	79
	DP_85D	DISPLAYPORT	MXM_DP_C_ML_C_N<3..0>	79
	DP_85D	DISPLAYPORT	DP_TX_EQ_AUXCH_P	78
	DP_85D	DISPLAYPORT	DP_TX_EQ_AUXCH_N	78
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_EQ_P<3..0>	78
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_EQ_N<3..0>	78
UNUSED VIDEO NET PHYSICAL CONSTRAINTS				
	DP_85D	DISPLAYPORT	MXM_DP_B_AUX_P	73 76
	DP_85D	DISPLAYPORT	MXM_DP_B_AUX_N	73 76
	DP_85D	DISPLAYPORT	MXM_DP_D_AUX_P	73 76
	DP_85D	DISPLAYPORT	MXM_DP_D_AUX_N	73 76
	DP_85D	DISPLAYPORT	MXM_LVDS_A_CLK_P	74 76
	DP_85D	DISPLAYPORT	MXM_LVDS_A_CLK_N	74 76
	DP_85D	DISPLAYPORT	MXM_LVDS_B_CLK_P	74 76
	DP_85D	DISPLAYPORT	MXM_LVDS_B_CLK_N	74 76
	DP_85D	DISPLAYPORT	MXM_DP_B_ML_P<3..0>	73 76
	DP_85D	DISPLAYPORT	MXM_DP_B_ML_N<3..0>	73 76
	DP_85D	DISPLAYPORT	MXM_DP_D_ML_P<3..0>	73 76
	DP_85D	DISPLAYPORT	MXM_DP_D_ML_N<3..0>	73 76
	DP_85D	DISPLAYPORT	MXM_LVDS_A_DATA_P<3..0>	74 76
	DP_85D	DISPLAYPORT	MXM_LVDS_A_DATA_N<3..0>	74 76
	DP_85D	DISPLAYPORT	MXM_LVDS_B_DATA_P<3..0>	74 76
	DP_85D	DISPLAYPORT	MXM_LVDS_B_DATA_N<3..0>	74 76

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SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	4:1_SPACING
THERMAL	POWER	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR
SNS_DIFF	*	1:1_DIFFPAIR

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	48
	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	48
	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	48
	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	48
	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	48
	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	48
	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	48
	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	48
	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	48 88
	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	48 88
	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	48 88
	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	48 88
I136	SMB_55S	SMB	SMBUS_PCH_S0_CLK	48
I135	SMB_55S	SMB	SMBUS_PCH_S0_DATA	48
I160	SMB_55S	SMB	SMBUS_PCH_CLK	18 48
I161	SMB_55S	SMB	SMBUS_PCH_DATA	18 48
I137	SMB_55S	SMB	SML_PCH_0_CLK	18 48
I139	SMB_55S	SMB	SML_PCH_0_DATA	18 48
I138	SMB_55S	SMB	SML_PCH_1_CLK	18 48
I140	SMB_55S	SMB	SML_PCH_1_DATA	18 48
I197	CLK_XTAL	XTAL	SMC_EXTAL	45 46
I196	CLK_XTAL	XTAL	SMC_XTAL	45 46

SMC THERMAL NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
I87	THERM_DIFF	THERMAL	SNS_T_DP1_DN6	51 88
I88	THERM_DIFF	THERMAL	SNS_T_DN1_DP6	51 88
I89	THERM_DIFF	THERMAL	SNS_T_DP2_DN3	51
I90	THERM_DIFF	THERMAL	SNS_T_DN2_DP3	51
I200	THERM_DIFF	THERMAL	SNS_T_DN1_DP6	51 88
I201	THERM_DIFF	THERMAL	SNS_T_DP1_DN6	51 88
I93	THERM_DIFF	THERMAL	SNS_T_DP4_DN5	51
I94	THERM_DIFF	THERMAL	SNS_T_DN4_DP5	51
I101	THERM_DIFF	THERMAL	SNS_LCD_P	51 92
I102	THERM_DIFF	THERMAL	SNS_LCD_N	51 92
I103	THERM_DIFF	THERMAL	SNS_ODD_P	51 92
I105	THERM_DIFF	THERMAL	SNS_ODD_N	51 92
I104	THERM_DIFF	THERMAL	SNS_CPU_H_P	51
I106	THERM_DIFF	THERMAL	SNS_CPU_H_N	51
I198	THERM_DIFF	THERMAL	SNS_SKIN_P	51 92
I199	THERM_DIFF	THERMAL	SNS_SKIN_N	51 92
I109	THERM_DIFF	THERMAL	SNS_AMB_P	51 92
I110	THERM_DIFF	THERMAL	SNS_AMB_N	51 92
I111	THERM_DIFF	THERMAL	SNS_MXM_P	51
I112	THERM_DIFF	THERMAL	SNS_MXM_N	51
I194	THERM_DIFF	THERMAL	SNS_CPU_THERMD_P	10 51
I195	THERM_DIFF	THERMAL	SNS_CPU_THERMD_N	10 51
I115		THERMAL	HDD_OOB_TEMP_FILT	51 92
I133		THERMAL	HDD_OOB_TEMP	51
I134		THERMAL	HDD_OOB_TEMP_R	51
I132		THERMAL	SMC_HDD_OOB_TEMP	51

SMC VOLTAGE/CURRENT NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
I97	THERM_DIFF	THERMAL	MXM_ISENSE_P	50
I98	THERM_DIFF	THERMAL	MXM_ISENSE_N	50
I99	THERM_DIFF	THERMAL	SENSE_CPU_1V5_S3_P	49
I100	THERM_DIFF	THERMAL	SENSE_CPU_1V5_S3_N	49
I148	THERM_DIFF	THERMAL	SENSE_CPU_1V5_S0_P	49
I149	THERM_DIFF	THERMAL	SENSE_CPU_1V5_S0_N	49
I150	THERM_DIFF	THERMAL	SENSE_CPU_1V5_P	49
I151	THERM_DIFF	THERMAL	SENSE_CPU_1V5_N	49
I152	THERM_DIFF	THERMAL	SENSE_CPU_VTT_P	49
I153	THERM_DIFF	THERMAL	SENSE_CPU_VTT_N	49
I181	THERM_DIFF	THERMAL	SENSE_CPU_VTT1_P	
I182	THERM_DIFF	THERMAL	SENSE_CPU_VTT1_N	
I183	THERM_DIFF	THERMAL	SENSE_CPU_VTT2_P	
I184	THERM_DIFF	THERMAL	SENSE_CPU_VTT2_N	
I162		THERMAL	GND_SMC_AVSS	45 46 49 50
I124		THERMAL	SMC_CPU_1V5_ISENSE	46 49
I123		THERMAL	SMC_CPU_1V5_ISENSE_R	49
I122		THERMAL	SMC_CPU_1V5_VSENSE	46 49
I163		THERMAL	SMC_CPU_VTT_ISENSE	46 49
I164		THERMAL	SMC_CPU_VTT_ISENSE_R	49
I165		THERMAL	SMC_CPU_VTT_VSENSE	46 49
I166		THERMAL	SMC_CPU_1V8_ISENSE	46 49
I167		THERMAL	SMC_CPU_1V8_ISENSE_R	
I168		THERMAL	SMC_CPU_1V8_VSENSE	46 49
I128		THERMAL	SMC_CPU_VSENSE	45 49
I113	VID_PHY	VR_CTL	VR_CPU_IOUT	13 64
I131	THERM_DIFF	THERMAL	VR_ISNS_CPU_P	49
I130	THERM_DIFF	THERMAL	VR_ISNS_CPU_N	49
I129		THERMAL	SNS_PS_CPU_ISNS	49
I114		THERMAL	SMC_CPU_ISENSE	45 49
I169		THERMAL	SMC_CPU_INPUT_ISENSE	46
I171		THERMAL	SMC_CPU_INPUT_VSENSE	46
I172		THERMAL	SMC_DIMM_1V5_ISENSE	46 50
I173		THERMAL	SMC_1V5_S3_ISENSE_R	
I174		THERMAL	SMC_DIMM_1V5_VSENSE	46 50
I178		THERMAL	SMC_GPU_ISENSE	45 50
I179		THERMAL	SMC_MXM_ISENSE_R	50
I180		THERMAL	SMC_GPU_VSENSE	45 50

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NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SWITCHNODE	SWITCHNODE	BGA_P1MM	BGA_P2MM
SWITCHNODE	POWER	BGA_P1MM	BGA_P2MM
SWITCHNODE	GND	BGA_P1MM	BGA_P2MM
SWITCHNODE	*	BGA_P1MM	BGA_P2MM
SWITCHNODE	POWER	*	6:1_SPACING
SWITCHNODE	GND	*	6:1_SPACING
SWITCHNODE	*	*	SWITCHNODE

POWER NET PROPERTIES

PHYSICAL	SPACING	VOLTAGE	NET	PAGES
POWER	SWITCHNODE	1.5V	VR_CPU_PHASE1	65
POWER	SWITCHNODE	1.5V	VR_CPU_PHASE2	65
POWER	SWITCHNODE	1.5V	VR_CPU_PHASE3	65
POWER	SWITCHNODE	1.5V	VR_CPU_PHASE4	66
POWER	SWITCHNODE	3.3V	P3V3S5_REG_PHASE	69
POWER	SWITCHNODE	5V	P5VS3_REG_PHASE	69
POWER	SWITCHNODE	1.1V	VTT_REG_PHASE1	67
POWER	SWITCHNODE	1.1V	VTT_REG_PHASE2	67
POWER	SWITCHNODE	3.4V	P3V42G3H_SW	71
POWER	SWITCHNODE	1.05V	PCHCORE_REG_PHASE	68
POWER	SWITCHNODE	1.05V	P1V05_S5_REG_PHASE	71
POWER	SWITCHNODE	1.5V	DDR_REG_PHASE	70
POWER	SWITCHNODE	1.8V	P1V8_REG_PHASE	70
POWER	POWER	1.5V	PP0V75_S3_MEM_VREFCA_A	28 30
POWER	POWER	1.5V	PP0V75_S3_MEM_VREFCA_B	28 31
POWER	POWER	1.5V	PP0V75_S3_MEM_VREFDQ_A	28 30
POWER	POWER	1.5V	PP0V75_S3_MEM_VREFDQ_B	28 31
POWER	POWER	12V	PP12V_S0_CPUVTT_FLTD	
POWER	POWER	12V	PP12V_AUD_SPKRAMP_PLANE	57 58 60
POWER	POWER	12V	PP12V_LCD	77
POWER	POWER	12V	PP12V_LCD_CONN	77
POWER	POWER	12V	PP12V_S0	6 63
POWER	POWER	12V	PP12V_S0_CPU_FLTRD	64 65 66
POWER	POWER	12V	PP12V_S0_FAN0_L	52 92
POWER	POWER	12V	PP12V_S0_FAN1_L	52 92
POWER	POWER	12V	PP12V_S0_FAN2_L	53 92
POWER	POWER	12V	PP12V_G3H	6 71
POWER	POWER	12V	PP12V_G3H_R	71
POWER	POWER	12V	PP12V_S5	6
POWER	POWER	12V	P12V_S0_FW	
POWER	POWER	12V	P12V_S0_FW_CL	
POWER	POWER	12V	P12V_S0_FW_D	
POWER	POWER	12V	P12V_S0_FW_R	
POWER	POWER	12V	FW_PORT0_VP	41
POWER	POWER	12V	FW_PORT0_VP_F	41
POWER	POWER	12V	PPVP_FW_PHY_CPS	40 41
POWER	POWER	12V	PP12V_S3	6
POWER	POWER	12V	PP12V_S3_WM_FLT	44
POWER	POWER	1.1V	PPVCORE_S0_CPU	6
POWER	POWER	1.1V	PPVCORE_S0_CPU_REG1	65
POWER	POWER	1.1V	PPVCORE_S0_CPU_REG2	65
POWER	POWER	1.1V	PPVCORE_S0_CPU_REG3	65
POWER	POWER	1.1V	PPVCORE_S0_CPU_REG4	66
POWER	POWER	1.05V	PP1V05_SM_SOURCE	72
POWER	POWER	1.05V	PP1V05_S0	6
POWER	POWER	1.05V	PP1V05_S0_CK505_F	26
POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLA	17 22
POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLA_F	
POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLB	17 22
POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLB_F	
POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLL_EXP	22 24
POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLL_FDI	22 24
POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLL_SATA	22 24
POWER	POWER	1.05V	PP1V05_S0_PCH_VCCA_CLK	22 24
POWER	POWER	1.05V	PP1V05_S0_PCH_VCCA_CLK_F	
POWER	POWER	1.05V	PP1V05_S0_CIO_VDD1P0_DP	
POWER	POWER	1.05V	PP1V05_S0_CIO_VDD1P0_DP_PLL	
POWER	POWER	1.05V	PP1V05_SM_PCH_LAN	
POWER	POWER	1.05V	PP1V05_S5	6
POWER	POWER	1.05V	PP1V05_SM	6
POWER	POWER	1.1V	PPVTT_S0	6
POWER	POWER	1.1V	PPVTT_S0_CPU	6 49
POWER	POWER	0.75V	PPVTT_S0_DDR	6
POWER	POWER	0.75V	PP0V75_S0	6
POWER	POWER	1.2V	PP1V2_S5_ENET	37
POWER	POWER	1.5V	PP1V5_S0	6
POWER	POWER	1.5V	PP1V5_S0_CK505_F	26
POWER	POWER	1.5V	PP1V5_S0_CK505_R	26
POWER	POWER	1.5V	PP1V5_S3	6
POWER	POWER	1.5V	PP1V5_CPU_MEM	6 49
POWER	POWER	1.5V	PP1V8R1V5_S0_PCH_VCCVRM	22 24
POWER	POWER	1.5V	PP1V5_FW_VDDA	39
POWER	POWER	1.5V	PP1V8_S0	6
POWER	POWER	1.8V	PP1V8_S0_CPU	6 49
POWER	POWER	1.96V	PP1V96_FW_PLLVDD	39
POWER	POWER	1.96V	PP1V95_FW_FWPHY	39 40

POWER NET PROPERTIES

PHYSICAL	SPACING	VOLTAGE	NET	PAGES
POWER	POWER	3.3V	PP3V3_S0	6
POWER	POWER	3.3V	PP3V3_S0_CK505_F	26
POWER	POWER	3.3V	PP3V3_S0_DPAUX	80
POWER	POWER	3.3V	PP3V3_S0_DPFUSE	80
POWER	POWER	3.3V	PP3V3_S0_DPPWR	80
POWER	POWER	3.3V	PP3V3_S0_HS_F	61
POWER	POWER	3.3V	PP3V3_S0M	6
POWER	POWER	3.3V	PP3V3_MINI	33
POWER	POWER	3.3V	PP3V3_ENET	36 37
POWER	POWER	3.3V	PP3V3_S0_PCH_VCCA_DAC	17 22
POWER	POWER	3.3V	PP3V3_S0_PCH_VCCA_DAC_F	
POWER	POWER	3.3V	PP3V3_S0_TSENS_R	51
POWER	POWER	3.3V	PP3V3_S3	6 92
POWER	POWER	3.3V	PP3V3_S3_BT_FLT	44
POWER	POWER	3.3V	PP3V3_S3_SDCARD_FLT	44
POWER	POWER	3.3V	PP3V3_S3_WM_FLT	44
POWER	POWER	3.3V	PP3V3_S5	6
POWER	POWER	3.3V	PPVTT_S3_DDR_BUF	70
POWER	POWER	3.3V	PPV_S0_MXM_PWRSRC	50
POWER	POWER	3.3V	PPVOUT_S0_PCH_DCPSST	22
POWER	POWER	3.3V	PPVOUT_S5_PCH_DCPSUS	22
POWER	POWER	3.3V	PPVOUT_S5_PCH_DCPSUSBYP	22
POWER	POWER	3.3V	PPVOUT_G3_PCH_DCPRTC	22
POWER	POWER	3.3V	PPVOUT_S0_PCH_VCCRTC_NCTF	
POWER	POWER	3.3V	PPVBATT_G3_RTC	27
POWER	POWER	3.3V	PPVBATT_G3_RTC_R	27
POWER	POWER	3.3V	PP3V3_AUDIO_SPDIF_JACK	59
POWER	POWER	3.3V	PP3V3_FW_AVDD	39
POWER	POWER	3.3V	PP3V3_FW_ESD	41
POWER	POWER	3.3V	PP3V3_FW_PLLVDD	39
POWER	POWER	3.3V	PP3V3_FW_VDDA	39
POWER	POWER	3.3V	PP3V3_G3_RTC	18 22 24 27
POWER	POWER	3.3V	PP_ENET_CTRL12	37
POWER	POWER	3.4V	PP3V3_G3H_SMC_AVCC	45
POWER	POWER	3.3V	PP3V3_G3H_AVREF_SMC	45 46
POWER	POWER	3.42V	PP3V42_G3H	6
POWER	POWER	3.42V	PP3V42_G3H_R	71
POWER	POWER	4.5V	4V5_REG_IN	55
POWER	POWER	4.5V	PP4V5_AUDIO_ANALOG	55
POWER	POWER	5V	PP5V_S0	6 92
POWER	POWER	5V	PP5V_S0_CPU_VCORE_VCC	64
POWER	POWER	5V	PP5V_S0_PCH_V5REF	22 24
POWER	POWER	5V	PP5V_S0_SATA_FET	42
POWER	POWER	5V	PP5V_S3	6
POWER	POWER	5V	PP5V_S3_DDR_REG_V5FILT	70
POWER	POWER	5V	PP5V_S3_CAMERA_FLT	44
POWER	POWER	5V	PP5V_S3_IR_FLT	44
POWER	POWER	5V	VREFMARGIN_DIMMA_P5V	28
POWER	POWER	5V	VREFMARGIN_DIMMB_P5V	28
POWER	POWER	5V	PP5V_S5	6
POWER	POWER	5V	PP5V_S5_PCH_V5REFSUS	22 24
POWER	POWER	5V	PP5V_S5_CPUVTT_VR	67
POWER	POWER	5V	PP5V_USB2_PORT0	43
POWER	POWER	5V	PP5V_USB2_PORT0_F	43
POWER	POWER	5V	PP5V_USB2_PORT1	43
POWER	POWER	5V	PP5V_USB2_PORT1_F	43
POWER	POWER	5V	PP5V_USB2_PORT2	43
POWER	POWER	5V	PP5V_USB2_PORT2_F	43
POWER	POWER	5V	PP5V_USB2_PORT3	43
POWER	POWER	5V	PP5V_USB2_PORT3_F	43
POWER	POWER		DDR_REG_PGND	70
POWER	POWER		DDR_REG_CSGND	70

SENSING NET PROPERTIES

PHYSICAL	SPACING	NET	PAGES
SNS_DIFF	THERMAL	VR_CPU_ISNS1_P	64 65
SNS_DIFF	THERMAL	VR_CPU_ISNS1_N	64 65
SNS_DIFF	THERMAL	VR_CPU_ISNS1_R_P	64
SNS_DIFF	THERMAL	VR_CPU_ISNS1_R_N	64
SNS_DIFF	THERMAL	VR_CPU_ISNS2_P	64 65
SNS_DIFF	THERMAL	VR_CPU_ISNS2_N	64 65
SNS_DIFF	THERMAL	VR_CPU_ISNS2_R_P	64
SNS_DIFF	THERMAL	VR_CPU_ISNS2_R_N	64
SNS_DIFF	THERMAL	VR_CPU_ISNS3_P	64 65
SNS_DIFF	THERMAL	VR_CPU_ISNS3_N	64 65
SNS_DIFF	THERMAL	VR_CPU_ISNS3_R_P	64
SNS_DIFF	THERMAL	VR_CPU_ISNS3_R_N	64
SNS_DIFF	THERMAL	VR_CPU_ISNS4_P	64 66
SNS_DIFF	THERMAL	VR_CPU_ISNS4_N	64 66
SNS_DIFF	THERMAL	VR_CPU_ISNS4_R_P	64
SNS_DIFF	THERMAL	VR_CPU_ISNS4_R_N	64
SNS_DIFF	THERMAL	VR_CPU_ISNS1_XW_P	65
SNS_DIFF	THERMAL	VR_CPU_ISNS1_XW_N	65
SNS_DIFF	THERMAL	VR_CPU_ISNS2_XW_P	65
SNS_DIFF	THERMAL	VR_CPU_ISNS2_XW_N	65
SNS_DIFF	THERMAL	VR_CPU_ISNS3_XW_P	65
SNS_DIFF	THERMAL	VR_CPU_ISNS3_XW_N	65
SNS_DIFF	THERMAL	VR_CPU_ISNS4_XW_P	66
SNS_DIFF	THERMAL	VR_CPU_ISNS4_XW_N	66
SNS_DIFF		CPU_VCC_PKG_SENSE_P	13 49 64
SNS_DIFF		CPU_VCC_PKG_SENSE_N	13 64
SNS_DIFF		CPU_VTTSENSE_P	13 49 67
SNS_DIFF		CPU_VTTSENSE_N	13 67
SNS_DIFF		CPU_VTTSENSE_R_P	67
SNS_DIFF		CPU_VTTSENSE_R_N	67
SNS_DIFF		VR_CPU_VSEN	64
SNS_DIFF		VR_CPU_RGND	64
SNS_DIFF		VR_CPU_VSNS_R_N	64
SNS_DIFF		VR_CPU_VSNS_R_P	64
SNS_DIFF		VR_CPU_VSNS_XW_P	64
SNS_DIFF		VR_CPU_VSNS_XW_N	64

VR CTRL NET PROPERTIES

PHYSICAL	SPACING	NET	PAGES
VR_CTL_PHY	VR_CTL	VR_CPU_PH1_SNUB	65
VR_CTL_PHY	VR_CTL	VR_CPU_PH2_SNUB	65
VR_CTL_PHY	VR_CTL	VR_CPU_PH3_SNUB	65
VR_CTL_PHY	VR_CTL	VR_CPU_PH4_SNUB	66
VR_CTL_PHY	VR_CTL	VR_CPU_PWM1	64 65
VR_CTL_PHY	VR_CTL	VR_CPU_PWM2	64 65
VR_CTL_PHY	VR_CTL	VR_CPU_PWM2_R	64
VR_CTL_PHY	VR_CTL	VR_CPU_PWM3	64 65
VR_CTL_PHY	VR_CTL	VR_CPU_PWM3_R	64
VR_CTL_PHY	VR_CTL	VR_CPU_PWM4	64 66
VR_CTL_PHY	VR_CTL	VR_CPU_PWM4_R	64
VR_CTL_PHY	VR_CTL	VR_CPU_REF	64
VR_CTL_PHY	VR_CTL	VR_CPU_SS	64
VR_CTL_PHY	VR_CTL	VR_CPU_TCOMP	64
VR_CTL_PHY	VR_CTL	VR_CPU_TM	64
VR_CTL_PHY	VR_CTL	VR_CPU_BOOT1_RC	65
VR_CTL_PHY	VR_CTL	VR_CPU_BOOT2_RC	65
VR_CTL_PHY	VR_CTL	VR_CPU_BOOT3_RC	65
VR_CTL_PHY	VR_CTL	VR_CPU_COMP	64
VR_CTL_PHY	VR_CTL	VR_CPU_COMP_R	64
VR_CTL_PHY	VR_CTL	VR_CPU_COMP_RC	64
VR_CTL_PHY	VR_CTL	VR_CPU_DAC	64
VR_CTL_PHY	VR_CTL	VR_CPU_DRV1_BOOT	65
VR_CTL_PHY	VR_CTL	VR_CPU_DRV1_GDSEL	65
VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV1_LGATE	65
VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV1_UGATE	65
VR_CTL_PHY	VR_CTL	VR_CPU_DRV2_BOOT	65
VR_CTL_PHY	VR_CTL	VR_CPU_DRV2_GDSEL	65
VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV2_LGATE	65
VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV2_UGATE	65
VR_CTL_PHY	VR_CTL	VR_CPU_DRV3_BOOT	65
VR_CTL_PHY	VR_CTL	VR_CPU_DRV3_GDSEL	65
VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV3_LGATE	65
VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV3_UGATE	65
VR_CTL_PHY	VR_CTL	VR_CPU_DRV4_BOOT	66
VR_CTL_PHY	VR_CTL	VR_CPU_DRV4_GDSEL	66
VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV4_LGATE	66
VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV4_UGATE	66
VR_CTL_PHY	VR_CTL	VR_CPU_FAN	64
VR_CTL_PHY	VR_CTL	VR_CPU_FB	64
VR_CTL_PHY	VR_CTL	VR_CPU_FB_R	64
VR_CTL_PHY	VR_CTL	VR_CPU_FS	64
VR_CTL_PHY	VR_CTL	VR_CPU_IMON	49 64
VR_CTL_PHY	VR_CTL	VR_CPU_IOUT_PD	64
VR_CTL_PHY	SWITCHNODE	PCHCORE_REG_UGATE	68
VR_CTL_PHY	SWITCHNODE	PCHCORE_REG_LGATE	68
VR_CTL_PHY	VR_CTL	PCHCORE_REG_VFB	68
VR_CTL_PHY	VR_CTL	PCHCORE_REG_TON	68
VR_CTL_PHY	VR_CTL	PCHCORE_REG_TRIP	68
VR_CTL_PHY	VR_CTL	PCHCORE_REG_BOOT	68
VR_CTL_PHY	VR_CTL	PCHCORE_REG_BOOT_R	68
VR_CTL_PHY	VR_CTL	VTT_REG_BOOT1	67
VR_CTL_PHY	VR_CTL	VTT_REG_BOOT2	67
VR_CTL_PHY	VR_CTL	VTT_REG_COMP	67
VR_CTL_PHY	VR_CTL	VTT_REG_FB	67
VR_CTL_PHY	VR_CTL	VTT_REG_FS	67
VR_CTL_PHY	VR_CTL	VTT_REG_ICOMP	67
VR_CTL_PHY	VR_CTL	VTT_REG_IREF	67
VR_CTL_PHY	VR_CTL	VTT_REG_ISUM	67
VR_CTL_PHY	SWITCHNODE	VTT_REG_LGATE1	67
VR_CTL_PHY	SWITCHNODE	VTT_REG_LGATE2	67
VR_CTL_PHY	VR_CTL	VTT_REG_OCSET	67
VR_CTL_PHY	VR_CTL	VTT_OFST	67
VR_CTL_PHY	VR_CTL	VTT_REG_REF	67
VR_CTL_PHY	VR_CTL	VTT_REG_RGND	67
VR_CTL_PHY	VR_CTL	VTT_SEL	67
VR_CTL_PHY	VR_CTL	VTT_REG_UGATE2	67
VR_CTL_PHY	VR_CTL	VTT_REG_UGATE1	67
VR_CTL_PHY	VR_CTL	VTT_REG_PH1_SNUB	67
VR_CTL_PHY	VR_CTL	VTT_REG_PH2_SNUB	67
VR_CTL_PHY	VR_CTL	VTT_REG_VSEN	67
VR_CTL_PHY	VR_CTL	P1V05S5_REG_VFB	71
VR_CTL_PHY	VR_CTL	P3V42G3H_BOOST	71
VR_CTL_PHY	VR_CTL	P3V42G3H_FB	71

VR CTRL NET PROPERTIES

PHYSICAL	SPACING	NET	PAGES
VR_CTL_PHY	VR_CTL	DDR_REG_CS	70
VR_CTL_PHY	VR_CTL	DDR_REG_FB	70
VR_CTL_PHY	SWITCHNODE	DDR_REG_LGATE	70
VR_CTL_PHY	SWITCHNODE	DDR_REG_UGATE	70
VR_CTL_PHY	VR_CTL	DDR_REG_BOOT	70
VR_CTL_PHY	VR_CTL	DDR_REG_BOOT_R	70
VR_CTL_PHY	VR_CTL	DDR_REG_VDDQSNS	70
VR_CTL_PHY	VR_CTL	DDR_REG_VTTSNS	70
VR_CTL_PHY	VR_CTL	P1V8_REG_POR	70
VR_CTL_PHY	VR_CTL	P3V3S5_REG_BOOT	69
VR_CTL_PHY	VR_CTL	P3V3S5_REG_BOOT_R	69
VR_CTL_PHY	VR_CTL	P3V3S5_REG_FB	69
VR_CTL_PHY	VR_CTL	P3V3S5_REG_ISEN	69
VR_CTL_PHY	SWITCHNODE	P3V3S5_REG_LGATE	69
VR_CTL_PHY	VR_CTL	P3V3S5_REG_OCSET	69
VR_CTL_PHY	SWITCHNODE	P3V3S5_REG_UGATE	69
VR_CTL_PHY	VR_CTL	P3V3S5_REG_SNUB	69
VR_CTL_PHY	VR_CTL	P5VS3_REG_BOOT	69
VR_CTL_PHY	VR_CTL	P5VS3_REG_FB	69
VR_CTL_PHY	VR_CTL	P5VS3_REG_ISEN	69
VR_CTL_PHY	SWITCHNODE	P5VS3_REG_LGATE	69
VR_CTL_PHY	VR_CTL	P5VS3_REG_OCSET	69
VR_CTL_PHY	SWITCHNODE	P5VS3_REG_UGATE	69

VR VID NET PROPERTIES

PULL-UP STUB < 1-INCH
VID LENGTH SKEW < 1-INCH
VID LENGTH RANGE< 1 TO 15-INCH

PHYSICAL	SPACING	NET	PAGES
VID_PHY	VR_CTL	CPU_VID<0>	13 16 64
VID_PHY	VR_CTL	CPU_VID<1>	13 16 64
VID_PHY	VR_CTL	CPU_VID<2>	13 16 64
VID_PHY	VR_CTL	CPU_VID<3>	13 16 64
VID_PHY	VR_CTL	CPU_VID<4>	13 16 64
VID_PHY	VR_CTL	CPU_VID<5>	13 16 64
VID_PHY	VR_CTL	CPU_VID<6>	13 16 64
VID_PHY	VR_CTL	CPU_VID<7>	13 16 64
VID_PHY	VR_CTL	CPU_PSI_L	13 16 64

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
VID_PHY	*	39_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL	*	0.2MM	?

SYNC_MASTER=K60_JERRY SYNC_DATE=07/01/2009

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POWER CONSTRAINTS

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PM NET PROPERTIES
(PM, RESET, EN, PGOOD)

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PM	*	*	2:1_SPACING
PM_VTT	PM_VTT	*	2:1_SPACING
PM_VTT	*	*	3:1_SPACING
PM_VTT	GND	*	DEFAULT
PM	GND	*	DEFAULT

	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
I2		PM	PLT_RESET_L	20 27
I1		PM_VTT	PLT_RESET_LS1V1_L	11
I4		PM	PM_ACDC_PS_ON	6
I3		PM	PM_BATLOW_L	15 19 45
I5		PM	PM_CLK32K_SUSCLK	9 45 85
I7		PM	PM_CLK32K_SUSCLK_R	9 19 85
I6		PM	PM_CLKRUN_L	15 19 45 47
I10		PM	PM_EXT_TS_L<0>	11 46
I9		PM	PM_EXT_TS_L<1>	11 46
I12		PM	PM_LAN_PWRGD	15 19
I117		PM_VTT	FSB_CPURSTOUT_L	11 25
I123		PM	USB_HUB_RESET_L	34 35
I25		PM_VTT	PM_MEM_PWRGD	11 19
I24		PM	PM_ME_PWRGD	19 63
I27		PM	PM_ME_S0_EN_G	72
I26		PM	PM_ME_S0_EN_G1	72
I28		PM	PM_ME_S0_EN_R	72
I30		PM	PM_MXM_PGOOD	63 74
I29		PM	PM_PCH_PWRGD	19 63
I31		PM	PM_PGOOD_DDRREG_S3	5 62 70
I33		PM	PM_PGOOD_PVCORE_CPU	5 26 63 64
I32		PM	PM_PWRBTN_L	19 25 45
I35		PM	PM_RSMRST_L	45 62
I34		PM	PM_RSMRST_PCH_L	19 62
I36		PM	PM_SLP_M_L	5 19 62
I38		PM	PM_SLP_M_R	
I37		PM	PM_SLP_S3_L	5 19 32 33 37 46 62 63
I40		PM	PM_SLP_S3_L_AND_S0_RDY	
I120		PM	PM_SLP_S4_1_L	19 62
I119		PM	PM_SLP_S4_2_L	19 45 46
I118		PM	PM_SLP_S4_3_L	5 19
I39		PM	PM_SLP_S4_L	19 32
I41		PM	PM_SLP_S5_L	19 45
I43		PM	PM_SUS_PWR_ACK	19
I42		PM_VTT	PM_SYNC	11 19
I122		PM	SDCARD_PLT_RST_L	27 44
I45		PM	PM_SYSRST_L	19 27 45
I44		PM	PM_SYS_PWRGD	19 32 63
I46		PM_VTT	PM_THRMTRIP_L	11 21 46
I48		PM	RSMRST_PWRGD	45 63
I47		PM	RTC_RESET_L	18 91
I50		PM_VTT	CPU_PWRGD	11 21 25
I49		PM	CPU_RESET_L	11 27
I51		PM	PGOOD_1V05ME_G1	63
I53		PM	PGOOD_1V05ME_G2	63
I52		PM	PGOOD_1V8_S0_G1	63
I54		PM	PGOOD_1V8_S0_G2	63
I56		PM	PGOOD_CPU_GFX_DDR	63
I55		PM	PGOOD_P12V_S3	
I58		PM	PGOOD_P1V05_ME_S5	
I57		PM	PGOOD_P1V5_S0	72
I59		PM	PGOOD_P1V8_S0	63
I61		PM	PGOOD_P3V3_ME	72
I60		PM	PGOOD_P3V3_S0	48 63 72
I63		PM	PGOOD_P3V3_S3	34 72
I62		PM	PGOOD_P5V_S0	62 72
I64		PM	PGOOD_PCH_AND_P1V8	63
I66		PM	PGOOD_PCH_S0	63
I65		PM	PGOOD_SYSPWROK	63
I67		PM	PGOOD_SYSPWROK_R	63
I68		PM	RTC_RESET_L	18 91
I69		PM	P12V_S3_EN	62 72
I71		PM	P1V05_ME_SM_EN	62 72
I70		PM	P1V5_S0_EN	62 72
I72		PM	P3V3ME_EN	62 72
I74		PM	P3V3S0_EN	62 72
I73		PM	P3V3S3_EN	62 72
I76		PM	P5VS0_EN	62 72
I75		PM	P5VS3_EN	62 69
I77		PM	PCHCORE_REG_EN	62 68
I79		PM	PCHCORE_REG_PGOOD	5 62 63 68
I78		PM	PEG_RESET_L	9 27
I80		PM	SDCARD_RESET	21 25 44 92

	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
I82		PM	4V5_REG_EN	55
I81		PM	ALL_SYS_PWRGD_R	6 25 32 63
I84		PM	ALL_SYS_PWRGD_SMC	45 63
I83		PM	CK505_27MHZ_EN	26
I85		PM	CPUVTT_REG_EN	62 67
I86		PM_VTT	CPUVTT_REG_PGOOD	11 62 63 67
I87		PM	CPU_MEM_RESET_L	11 32
I88		PM	DDRVTT_EN	32 62 70
I89		PM	DEBUG_RESET_L	27 47
I90		PM	FWPHY_RESET_L	39
I91		PM	FWXIO_SNOOP_EN	39
I92		PM	FW_RESET_L	27 39
I93		PM	GFX_VR_EN	
I94		PM	GFX_VR_PGOOD	
I95		PM	LAN_RESET_L	27 36
I97		PM	MEM_RESET_L	30 31 32
I96		PM	MINI_RESET_L	27 33
I98		PM	SMC_DELAYED_PWRGD	46 63
I100		PM	SMC_LRESET_L	27 45
I99		PM	SMC_RESET_L	45 46 47
I102		PM	T28_RESET_L	
I101		PM_VTT	XDP_CPUPWRGD	11 25
I103		PM_VTT	XDP_DBRESET_L	11 25 27
I104		PM_VTT	XDP_PWRGD	25

NET PHYSICAL FOR NC NETS
REMOVE WHEN CHECKPLUS IS FIXED

PCIE GRAPHICS

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET
I105		PCIE_85D	PCIE	NC_PCIE_CLK100M_EXCARD_N
I106		PCIE_85D	PCIE	NC_PCIE_CLK100M_EXCARD_P
I107		PCIE_85D	PCIE	NC_PCIE_EXCARD_D2R_N
I108		PCIE_85D	PCIE	NC_PCIE_EXCARD_D2R_P
I109		PCIE_85D	PCIE	NC_PCIE_EXCARD_R2D_C_N
I110		PCIE_85D	PCIE	NC_PCIE_EXCARD_R2D_C_P
I112	NO_TEST=TRUE	USB_90D	USB	NC_USB_EXCARD_N
I111	NO_TEST=TRUE	USB_90D	USB	NC_USB_EXCARD_P
I114	NO_TEST=TRUE	USB_90D	USB	NC_USB_EXTE_N
I113	NO_TEST=TRUE	USB_90D	USB	NC_USB_EXTE_P
I116	NO_TEST=TRUE	USB_90D	USB	NC_USB_TPAD_N
I115	NO_TEST=TRUE	USB_90D	USB	NC_USB_TPAD_P

SYNC_MASTER=K60_MIKE SYNC_DATE=07/01/2009

PAGE TITLE
PM RESETS ENABLES PGOOD CONST

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FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT

J4700 USB CAMERA

IN PP5V_S3_CAMERA FUNC_TEST=TRUE MIN_ALLOWED_TPS=1
85 44 IN USB_CAMERA_L_P FUNC_TEST=TRUE
85 44 IN USB_CAMERA_L_N FUNC_TEST=TRUE
1 PP5V_S3_REG Testpoint near J4700
2 Ground Testpoints near J4700

J4750 USB CARD READER

85 44 IN USB_SDCARD_L_P FUNC_TEST=TRUE
85 44 IN USB_SDCARD_L_N FUNC_TEST=TRUE
91 44 25 21 IN SDCARD_RESET FUNC_TEST=TRUE
1 PP3V3_S3 Testpoint near J4750
2 Ground Testpoints near J4750

J4720 USB BLUETOOTH

85 44 IN USB_BT_L_P FUNC_TEST=TRUE
85 44 IN USB_BT_L_N FUNC_TEST=TRUE
1 PP3V3_S3 Testpoint near J4720
2 Ground Testpoints near J4720

J4780 IR BOARD

85 44 IN USB_IR_L_P FUNC_TEST=TRUE
85 44 IN USB_IR_L_N FUNC_TEST=TRUE
1 PP5V_S3_REG Testpoint near J4780
2 Ground Testpoints near J4780

J4520 SATA ODD (HIGH SPEED)

84 42 IN SATA_ODD_R2D_P FUNC_TEST=TRUE
84 42 IN SATA_ODD_R2D_N FUNC_TEST=TRUE
84 42 IN SATA_ODD_D2R_C_N FUNC_TEST=TRUE
84 42 IN SATA_ODD_D2R_C_P FUNC_TEST=TRUE
45 42 IN SMC_ODD_DETECT FUNC_TEST=TRUE
1 PP5V_S0 Testpoint near J4520
5 Ground Testpoints near J4520

J4510 SATA HDD (HIGH SPEED)

84 42 IN SATA_HDD_R2D_P FUNC_TEST=TRUE
84 42 IN SATA_HDD_R2D_N FUNC_TEST=TRUE
84 42 IN SATA_HDD_D2R_C_N FUNC_TEST=TRUE
84 42 IN SATA_HDD_D2R_C_P FUNC_TEST=TRUE
3 Ground Testpoints near J4510

J5520 ANALOG LCD TEMP SENSOR

88 51 IN SNS_LCD_P FUNC_TEST=TRUE
88 51 IN SNS_LCD_N FUNC_TEST=TRUE

J5521 AMBIENT TEMP SENSOR

88 51 IN SNS_AMB_P FUNC_TEST=TRUE
88 51 IN SNS_AMB_N FUNC_TEST=TRUE

J5551 ODD TEMP SENSOR

88 51 IN SNS_ODD_P FUNC_TEST=TRUE
88 51 IN SNS_ODD_N FUNC_TEST=TRUE

J5600 ODD FAN

52 IN FAN_0_PWR_L FUNC_TEST=TRUE
52 IN FAN_TACH0_L FUNC_TEST=TRUE
89 52 IN PP12V_S0_FAN0_L FUNC_TEST=TRUE
52 IN FAN_0_GND FUNC_TEST=TRUE

J5700 CPU FAN

53 IN FAN_2_PWR_L FUNC_TEST=TRUE
53 IN FAN_TACH2_L FUNC_TEST=TRUE
89 53 IN PP12V_S0_FAN2_L FUNC_TEST=TRUE
53 IN FAN_2_GND FUNC_TEST=TRUE

J5601 HD FAN

52 IN FAN_1_PWR_L FUNC_TEST=TRUE
52 IN FAN_TACH1_L FUNC_TEST=TRUE
89 52 IN PP12V_S0_FAN1_L FUNC_TEST=TRUE
52 IN FAN_1_GND FUNC_TEST=TRUE

J5550 HDD TEMP SENSOR

88 51 IN HDD_OOB_TEMP_FILT FUNC_TEST=TRUE

J5560 SKIN TEMP SENSOR

88 51 IN SNS_SKIN_P FUNC_TEST=TRUE
88 51 IN SNS_SKIN_N FUNC_TEST=TRUE

J6601 AUDIO MICROPHONE

59 IN AUD_MIC_IN1_N_CONN FUNC_TEST=TRUE
59 IN GND_AUDIO_MIC1_CONN FUNC_TEST=TRUE
59 IN AUD_MIC_IN1_P_CONN FUNC_TEST=TRUE
1 Ground Testpoint near J6601

J6602 AUDIO RIGHT SPEAKER

85 59 58 IN AUD_SPKR_OUTLO2R_POUT FUNC_TEST=TRUE
85 59 58 IN AUD_SPKR_OUTLO2R_NOUT FUNC_TEST=TRUE
85 59 57 IN AUD_SPKR_OUTLO1R_POUT FUNC_TEST=TRUE
85 59 57 IN AUD_SPKR_OUTLO1R_NOUT FUNC_TEST=TRUE

J6603 AUDIO LEFT SPEAKER

85 59 58 IN AUD_SPKR_OUTLO2L_POUT FUNC_TEST=TRUE
85 59 58 IN AUD_SPKR_OUTLO2L_NOUT FUNC_TEST=TRUE
85 59 57 IN AUD_SPKR_OUTLO1L_POUT FUNC_TEST=TRUE
85 59 57 IN AUD_SPKR_OUTLO1L_NOUT FUNC_TEST=TRUE

GND 16 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=16
89 6 IN PP3V3_S3 2 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=2
69 6 IN PP5V_S3_REG 2 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=1
89 6 IN PP5V_S0 FUNC_TEST=TRUE MIN_ALLOWED_TPS=1

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SYNC_MASTER=K60_DEREK SYNC_DATE=07/01/2009

PAGE TITLE: K22/K23 ICT/FCT

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DRAWING NUMBER: 051-8233 SIZE: D
REVISION: B.0.0
BRANCH:
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