1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

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5	Power Conn / Alias	MASTER N/A
6	HOLES & STANDOFFS	MASTER N/A
7	UNUSED SIGNAL ALIAS	MASTER N/A
8	SIGNAL ALIASES	MASTER N/A
9	CPU FSB	MASTER N/A
10	CPU TEST & MISC.	MASTER N/A
11	CPU POWER, GND, DECAPS	MASTER N/A
12	eXtended Debug Port (XDP)	MASTER N/A
13	MCP CPU Interface	MASTER N/A
14	MCP Memory Interface	MASTER N/A
15	MCP MEMORY CNTRL & MISC	MASTER N/A
16	MCP PCIe Interfaces	MASTER N/A
17	MCP Ethernet & Graphics	MASTER N/A
18	MCP PCI & LPC	MASTER N/A
19	MCP SATA & USB	MASTER N/A
20	MCP HDA & MISC	MASTER N/A
21	MCP Power & Ground	MASTER N/A
22	MCP Standard Decoupling	K51 12/08/2008
23	MCP Graphics Support	MASTER N/A
24	SB Misc	MASTER N/A
25	FSB/DDR3 Vref Margining	MASTER MASTER
26	MEMORY CAPS	MASTER N/A
27	DDR3 SO-DIMMs 0 & 2	MASTER N/A
28	DDR3 SO-DIMM CONNECTOR B	MASTER N/A
29	DDR3 SUPPORT AND BITSWAPS	K51 10/13/2008
30	PCI-E Wireless Connector	MASTER N/A
31	Ethernet PHY (RTL8211CL)	K51 12/08/2008
32	Ethernet Support	MASTER N/A
33	ETHERNET CONNECTOR	MASTER N/A
34	FireWire LLC/PHY (XIO2213B)	MASTER N/A
35	FW: 1394B MISC	MASTER N/A
36	FIREWIRE CONNECTOR	MASTER N/A
37	SATA Connectors	MASTER N/A
38	EXTERNAL USB CONNECTORS	MASTER N/A
39	Internal USB Connections	MASTER MASTER
40	SMC	MASTER N/A
41	SMC Support	MASTER N/A
42	LPC+SPI Debug Connector	MASTER N/A
43	SMBUS CONNECTIONS	MASTER N/A
44	CPU/MXM CURRENT AND VOLTAGE SENSE	MASTER N/A
45	MCP CURRENT AND VOLTAGE SENSE	K51 12/08/2008
46	Thermal Sensors	MASTER N/A
47	HD AND OD FAN	MASTER N/A
48	CPU FAN	MASTER N/A
49	SPI ROM	K51 12/08/2008
50	AUDIO: CODEC/REGULATOR	SKIPAUDIO 06/01/2009
51	AUDIO: FILTER/BUFFER	SKIPAUDIO 06/01/2009
52	AUDIO: SPEAKER AMP	SKIPAUDIO 06/01/2009
53	AUDIO: SPEAKER AMP	SKIPAUDIO 06/01/2009
54	Audio: MLB to I/O Conn.	SKIPAUDIO 06/01/2009
55	AUDIO: Detects/Grounding	SKIPAUDIO 06/01/2009
56	AUDIO: Mikey	SKIPAUDIO 06/01/2009
57	POWER SEQUENCING BLOCK DIAGRAM	K51 12/08/2008
58	PGOOD and Power Sequencing	MASTER N/A
59	VREG: PPVCORE_S0_CPU	MASTER N/A
60	VREG: PPVCORE_S0_CPU	MASTER N/A
61	5V_S3 REGULATOR	MASTER N/A
62	MCP CORE REGULATOR	MASTER N/A
63	1.5V DDR SUPPLY	MASTER N/A
64	FSB VTT/3.3V S5 SUPPLIES	MASTER N/A
65	S3 & S0 FETs	MASTER N/A
66	1V1 S5 POWER SUPPLY	K51 10/31/2008
67	1V8 POWER SUPPLY	MASTER N/A
68	MXM PCIe, DP & Power	K51 10/31/2008
69	MXM I/O	K51 10/31/2008
70	MXM PCIE CAPS	MASTER N/A
71	MXM ALIASES	MASTER N/A
72	LCD MUX & CHOKES	MASTER MASTER
73	INTERNAL DISPLAY	MASTER MASTER
74	DP MUX SUPPORT	MASTER N/A
75	DISPLAYPORT SUPPORT	MASTER N/A
76	DisplayPort Connector	MASTER N/A
77	CPU/FSB Constraints	MASTER N/A
78	Memory Constraints	MASTER N/A
79	MCP Constraints 1	MASTER N/A
80	MCP Constraints 2	MASTER N/A
81	Ethernet Constraints	MASTER N/A
82	FireWire Constraints	MASTER N/A
83	SMC Constraints	MASTER N/A
84	GRAPHICS CONSTRAINTS	MASTER N/A
85	K22/K23 SPECIFIC CONSTRAINTS	MASTER N/A
86	K22/K23 RULE DEFINITIONS	MASTER N/A
87	K22/K23 ICT/FCT	MASTER N/A

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Jul 23 2009

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
820-2494	1	PCBF,K22,MLB	MLB1		K22

DRAWING
TITLE=K22
ABBREV=DRAWING
LAST_MODIFIED=Wed Jun 3 10:42:53 2009

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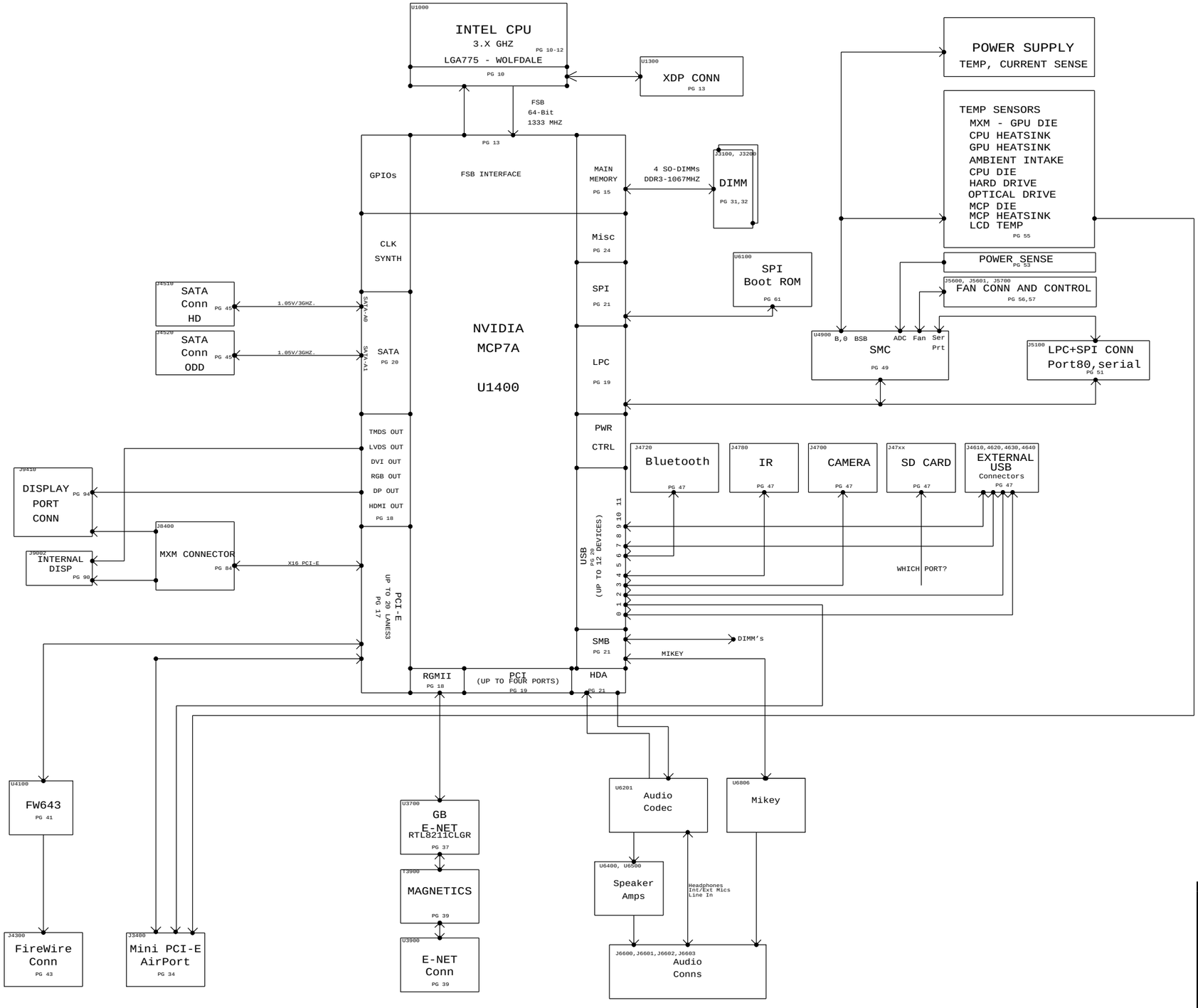

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System Block Diagram

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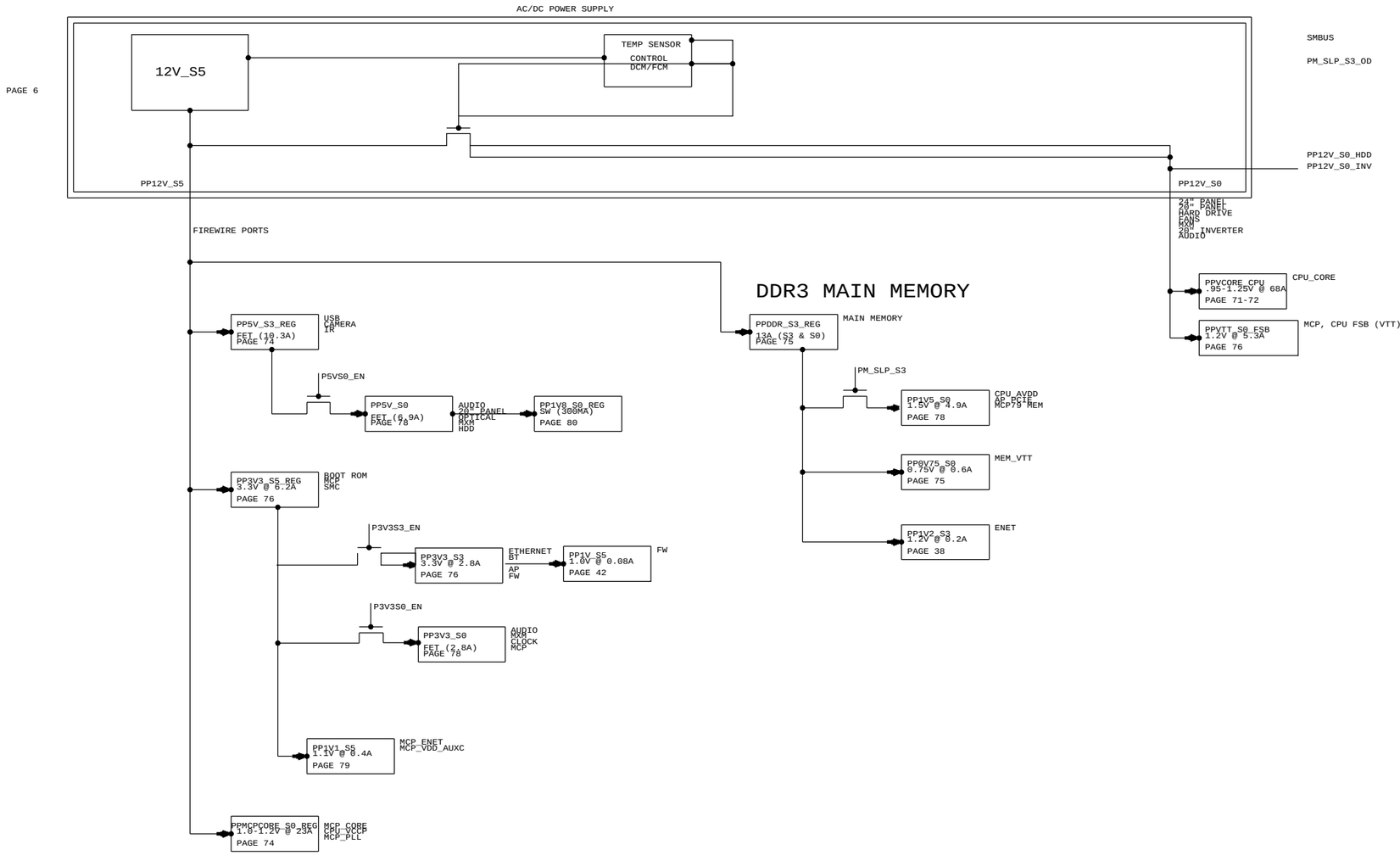

PAGE TITLE

Power Block Diagram

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BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL
4	POWER
5	POWER
6	SIGNAL
7	GROUND
BOTTOM	SIGNAL

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8 7 6 5 4 3 2 1

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EMC: C600,C626,C627,C628,C629,C630,C631
PLACE AT J600.

518-0352
CRITICAL
J600
76833-0100
M-RT-TH

=SMB_ACDC_SCL
=PP5V_S0_SATA
PP12V_S5
LCD_PWM
=SMB_ACDC_SDA
PP12V_S0
LCD_BKL_ON

C623 10UF 20% 10V X5R 805
C631 0.001UF 10% 50V X7R 402
C627 0.001UF 10% 50V X7R 402
C626 0.001UF 10% 50V X7R 402
C630 0.001UF 10% 50V X7R 402
C624 10UF 10% 16V X5R-CERM 1210

PM_ACDC_PS_ON
70 50 49 9 PM_SLPS3_BUF2_L
Q610 2N7002 SOT23-HF1
C600 0.001UF 10% 50V X7R 402

110 78 6 PP3V3_S3
DEVELOPMENT
R600 1K 5% 1/16W MF-LF 402
ITS_ALIVE
DEVELOPMENT
LED605 GREEN-3.6MCD 2.0X1.25MM-SM

76 6 PP3V3_S5_REG
R601 1K 5% 1/16W MF-LF 402
ITS_PLUGGED_IN
LED601 GREEN-3.6MCD 2.0X1.25MM-SM SILKSCREEN:1

110 78 6 PP3V3_S3
R602 1K 5% 1/16W MF-LF 402
CORE_VOLTAGES_ON_R
LED602 GREEN-3.6MCD 2.0X1.25MM-SM SILKSCREEN:2
CORE_VOLTAGES_ON
70 IN ALL_SYS_PWRGD_R
Q602 2N7002 SOT23-HF1

78 6 PP3V3_S0
MXM
R604 1K 5% 1/10W MF-LF 402
GPU_PRESENT_R
MXM
LED604 GREEN-3.6MCD 2.0X1.25MM-SM SILKSCREEN:3
GPU_PRESENT_DRAIN
MXM
Q604 2N7002 SOT23-HF1
9 IN MXM_GOOD

90 PP5V_LCD_CONN
R603 1.5K 5% 1/16W MF-LF 402
LCD_SHOULD_ON
LED603 GREEN-3.6MCD 2.0X1.25MM-SM SILKSCREEN:4

"S0" RAILS
ONLY ON IN RUN

75 PPVTT_S0_DDR_LDO
MAKE_BASE=TRUE
VOLTAGE=0.75V
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP0V75_S0_MEM_VTT_A 31
=PP0V75_S0_MEM_VTT_B 32
=PPVTT_S0_VTTCLAMP 78

72 71 PPVCORE_S0_CPU
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PPVCORE_S0_CPU 12

74 54 PPMCPCORE_S0_REG
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PPVCORE_S0_MCP 22 25
=PP1V05_S0_MCP_AVDD_UF 25
=PP1V05_S0_MCP_PEX_DVDD 25 28
=PP1V05_S0_MCP_PLL_UF 25
=PP1V05_S0_MCP_SATA_DVDD0 20 28
=PP1V05_S0_MCP_HDMI_VDD_R 26

76 PPVTT_S0_FSB_REG
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PPVTT_S0_CPU 10 50 55 71
=PPVTT_S0_FSB_CPU 11 12
=PPVTT_S0_XDP 13
=PP1V05_S0_MCP_FSB 14 22 25

54 PP1V5_S0
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.15MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP1V5_S0_CPU_VCCPLL 12
=PP1V8R1V5_S0_MCP_MEM 16 25 30
=PP1V5_S0_AUD_DIG 62
=PP1V5_FWRS0_FWXIO 41

80 PP1V8_S0_REG
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP3V3R1V8_S0_MCP_IFP_VDD_R 26
=PP1V8_S0_PGCMP 70

78 6 PP3V3_S0
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.10MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP3V3_S0_FAN 56 57
=PP3V3_S0_MCP 21 22 25
=PP3V3_S0_MCP_VPLL_UF 26
=PP3V3_S0_MCP_GPIO 18 19 21
=PP3V3_S0_MCP_PLL_UF 25
=PPSPD_S0_MEM_A 31
=PPSPD_S0_MEM_B 32
=PP3V3_S0_VRD 71
=PP3V3_S0_AUDIO 62 64 65 66 67 68
=PP3V3R1V5_S0_MCP_HDA 21 25
=PP3V3_S0_SMBUS 52
=PP3V3_S0_SMC_LS 50 55
=PP3V3_S0_SMBUS_SMC_0_S0 52
=PP3V3_S0_SMBUS_SMC_B_S0 52
=PP3V3_S0_SMBUS_SMC_MGMT 52
=PP3V3_S0_DPCONN 94
=PP3V3_S0_TSENS 55
=PP3V3_S0_MXM 84 85
=PP3V3_S0_XDP 13
=PP3V3_S0_ODD 45
=PP3V3_S0_SATALED 45
=PP3V3_S0_SMC 50 53 54
=PP3V3_S0_PWRCTL 70
=PP3V3_S0_MCPTHMSNS 55
=PP3V3_S0_VIDEO 89 90
=PP3V3_FW_FWPHY 41 42 43
=PP3V3_FWRS0_FWXIO 41

110 78 PP5V_S0
MAKE_BASE=TRUE
VOLTAGE=5.0V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP5V_S0_LPCPLUS 51
=PP5V_S0_AUDIO 62 68
=PP5V_S0_SATA 6 45
=PP5V_S0_MXM 84
=PP5V_S0_VRD 71
=PP5V_S0_DP_AUX_MUX 93
=PP5V_S0_ISENSE 53
=PP5V_S0_PWRCTL 80
=PP5V_S0_LCD 90

70 6 PP12V_S0
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=AUDIO
MAX_NECK_LENGTH=3 MM
=PP12V_S0_FAN 56 57
=PP12V_S0_AUDIO_SPKRAMP 67
=PP12V_S0_VRD 70 71
=PPV_S0_MXM_PWR 53
=PPVIN_S0_PPVTT_FSB 76
=PPVIN_S0_MCPCORE 74

"S3" RAILS
ON IN RUN AND SLEEP

75 PPDDR_S3_REG
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PPDDR_MEM
MAX_NECK_LENGTH=3 MM
=PP1V5_S3_MEM_A 30 31 108
=PP1V5_S3_MEM_B 30 32 108
=PP1V5_S3_MEMRESET 33
=PPDDR_S3_S0FET 78
=PPDDR_S3_PGCMP 70

75 PPVTT_S3_DDR_BUF
MAKE_BASE=TRUE
VOLTAGE=0.75V
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 mm
=PPVTT_S3_DDR_BUF 29

110 78 6 PP3V3_S3
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP3V3_S3_MINI 34
=PP3V3_S3_BT 47
=PP3V3_S3_VREFMRGN 29
=PP3V3_S3_SDCARD 47
=PP3V3_S3_MCP_GPIO 21
=PP3V3_S3_SMC 47
=PP3V3_S3_SMBUS_SMC_A_S3 52
=PP3V3_S3_MCPREG 74

110 73 PP5V_S3_REG
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP5V_S3_DDRREG 30 75
=PP5V_S3_USB 46
=PP5V_S3_VTTCLAMP 78
=PP5V_S3_PWRCTL 70
=PP5V_S3_S0FET 78
=PP5V_S3_MCPREG 74
=PP5V_S3_CAMERA 47
=PP5V_S3_IR 47
=PP5V_S3_1V8 80

"S5" RAILS
ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

79 PP1V1_S5_REG
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP1V05_S5_MCP_VDD_AUXC 22 25
=PP1V1_S5_ENET_FET 38

76 6 PP3V3_S5_REG
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP3V3_S5_MCP 22 25
=PP3V3_S5_MCP_GPIO 18 20
=PP3V3_S5_SMC 49 50
=PP3V3_S5_ROM 51 61
=PP3V3_S5_RTC_D 28
=PP3V3_S5_LPCPLUS 51
=PP3V3_S5_SMBUS_SMC_BSA 52
=PP3V3_S5_SMCUSBMUX 46
=PP3V3_S5_MEMRESET 33
=PP3V3_S5_P1V1S5 79
=PP3V3_S5_PWRCTL 70
=PP3V3_S5_S3FET 78
=PP3V3_S5_S0FET 78
=PP3V3_S5_ENET_FET 38

76 PP5V_S5_LDO
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP5V_S5_AVREF 50

6 PP12V_S5
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP12V_S5_FW 43
=PPVIN_S5_DDRREG 75
=PPVIN_S5_P3V3S5 76
=PPVIN_S5_P5VS3 73
=PP12V_S5_REG 76
=PP12V_S5_PWRCTL 38 70 78

GND RAILS

GND
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V
NET_SPACING_TYPE=AUDIO
MAKE_BASE=TRUE
MAX_NECK_LENGTH=4.1 MM

PAGE TITLE: Power Conn / Alias
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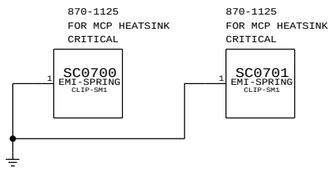
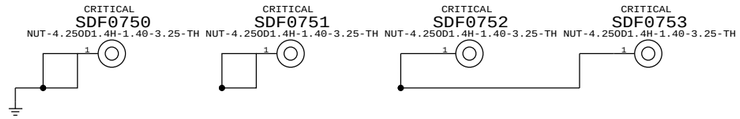
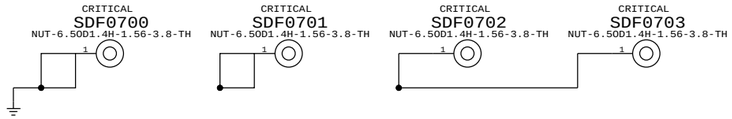


DIMM CONNECTOR NUTS

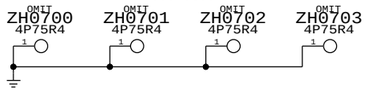


BACKER PLATE NUTS

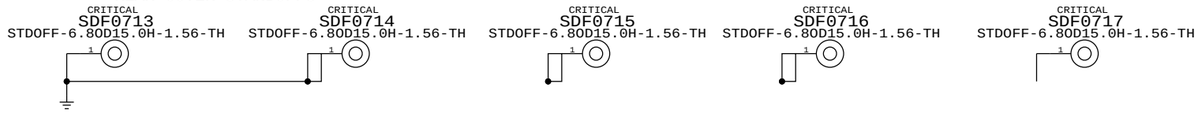


4 MM PLATED HOLES FOR CPU HEATSINK

998-0850



REAR COVER STANDOFFS



PAGE TITLE: HOLES & STANDOFFS

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SHEET

NC ON UNUSED ALIASES

18	MCP_TV_DAC_RSET	=	NC_MCP_TV_DAC_RSET	MAKE_BASE=TRUE NO_TEST=TRUE
18	MCP_TV_DAC_VREF	=	NC_MCP_TV_DAC_VREF	MAKE_BASE=TRUE NO_TEST=TRUE
18	MCP_CLK27M_XTALIN	=	NC_MCP_CLK27M_XTALIN	MAKE_BASE=TRUE NO_TEST=TRUE
18	MCP_CLK27M_XTALOUT	=	NC_MCP_CLK27M_XTALOUT	MAKE_BASE=TRUE NO_TEST=TRUE
18	CRT_IG_R_C_PR	=	NC_CRT_IG_R_C_PR	MAKE_BASE=TRUE NO_TEST=TRUE
18	CRT_IG_G_Y_Y	=	NC_CRT_IG_G_Y_Y	MAKE_BASE=TRUE NO_TEST=TRUE
18	CRT_IG_B_COMP_PB	=	NC_CRT_IG_B_COMP_PB	MAKE_BASE=TRUE NO_TEST=TRUE
18	CRT_IG_HSYNC	=	NC_CRT_IG_HSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
18	CRT_IG_VSYNC	=	NC_CRT_IG_VSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_MCP_RGB_HSYNC	=	NC_MCP_RGB_HSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_MCP_RGB_VSYNC	=	NC_MCP_RGB_VSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_AD<31..15>	=	NC_PCI_AD<31..15>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_IRDY_L	=	NC_PCI_IRDY_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_C_BE_L<1..0>	=	NC_PCI_C_BE_L<1..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_SERR_L	=	NC_PCI_SERR_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_DEVSEL_L	=	NC_PCI_DEVSEL_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_PERR_L	=	NC_PCI_PERR_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_LPC_DRQ0_L	=	NC_LPC_DRQ0_L	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_MCP_BUF_SIO_CLK	=	NC_MCP_BUF_SIO_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_ENET_INTR_L	=	NC_ENET_INTR_L	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_ENET_PWRDWN_L	=	NC_ENET_PWDWN_L	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_MCP_KBDRSTIN_L	=	NC_MCP_KBDRSTIN_L	MAKE_BASE=TRUE NO_TEST=TRUE
	TP_MCP_GPIO_18	=	NC_MCP_GPIO_18	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_MLB_RAM_SIZE	=	NC_MLB_RAM_SIZE	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_C_BE_L<3>	=	NC_PCI_C_BE_L<3>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_CLK0	=	NC_PCI_CLK0	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_CLK1	=	NC_PCI_CLK1	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_FRAME_L	=	NC_PCI_FRAME_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_GNT0_L	=	NC_MCP_PCI_GNT0_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_GNT1_L	=	NC_PCI_GNT1_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_INTW_L	=	NC_PCI_INTW_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_INTX_L	=	NC_PCI_INTX_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_INTY_L	=	NC_PCI_INTY_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_INTZ_L	=	NC_PCI_INTZ_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_PAR	=	NC_PCI_PAR	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_RESET1_L	=	NC_PCI_RESET1_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_STOP_L	=	NC_PCI_STOP_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_TRDY_L	=	NC_PCI_TRDY_L	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE4N	=	NC_PCIE_CLK100M_PE4N	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE4P	=	NC_PCIE_CLK100M_PE4P	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE5N	=	NC_PCIE_CLK100M_PE5N	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE5P	=	NC_PCIE_CLK100M_PE5P	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE6P	=	NC_PCIE_CLK100M_PE6P	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE6N	=	NC_PCIE_CLK100M_PE6N	MAKE_BASE=TRUE NO_TEST=TRUE
17	PCIE_EXCARD_PRSNT_L	=	NC_PCIE_EXCARD_PRSNT_L	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PE4_CLKREQ_L	=	NC_PE4_CLKREQ_L	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PE4_PRSNT_L	=	NC_PE4_PRSNT_L	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_SB_A20GATE	=	NC_SB_A20GATE	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_10N	=	NC_USB_10N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_10P	=	NC_USB_10P	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_MINI_N	=	NC_USB_MINI_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_MINI_P	=	NC_USB_MINI_P	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_EXCARD_N	=	NC_USB_EXCARD_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_EXCARD_P	=	NC_USB_EXCARD_P	MAKE_BASE=TRUE NO_TEST=TRUE
21	ODD_PWR_EN_L	=	NC_ODD_PWR_EN_L	MAKE_BASE=TRUE NO_TEST=TRUE
17	PCIE_CLK100M_EXCARD_P	=	NC_PCIE_CLK100M_EXCARD_P	MAKE_BASE=TRUE NO_TEST=TRUE
17	PCIE_CLK100M_EXCARD_N	=	NC_PCIE_CLK100M_EXCARD_N	MAKE_BASE=TRUE NO_TEST=TRUE
17	EXCARD_CLKREQ_L	=	NC_EXCARD_CLKREQ_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_AD<12..10>	=	NC_PCI_AD<12..10>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_AD<8>	=	NC_PCI_AD<8>	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PCIE_PE4_R2D_CP	=	NC_PCIE_PE4_R2D_CP	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PCIE_PE4_R2D_CN	=	NC_PCIE_PE4_R2D_CN	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PCIE_PE4_D2RP	=	NC_PCIE_PE4_D2RP	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PCIE_PE4_D2RN	=	NC_PCIE_PE4_D2RN	MAKE_BASE=TRUE NO_TEST=TRUE
17	PCIE_EXCARD_D2R_P	=	NC_PCIE_EXCARD_D2R_P	MAKE_BASE=TRUE NO_TEST=TRUE
17	PCIE_EXCARD_D2R_N	=	NC_PCIE_EXCARD_D2R_N	MAKE_BASE=TRUE NO_TEST=TRUE
17	PCIE_EXCARD_R2D_C_P	=	NC_PCIE_EXCARD_R2D_C_P	MAKE_BASE=TRUE NO_TEST=TRUE
17	PCIE_EXCARD_R2D_C_N	=	NC_PCIE_EXCARD_R2D_C_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_TPAD_N	=	NC_USB_TPAD_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_TPAD_P	=	NC_USB_TPAD_P	MAKE_BASE=TRUE NO_TEST=TRUE

MCP HAS INTERNAL 15K PULL-DOWNS

UNUSED MEMORY SIGNALS

15	TP_MEM_A_CLK2P	=	NC_MEM_A_CLK2P	MAKE_BASE=TRUE NO_TEST=TRUE
15	TP_MEM_A_CLK2N	=	NC_MEM_A_CLK2N	MAKE_BASE=TRUE NO_TEST=TRUE
16	TP_MEM_A_CLK5P	=	NC_MEM_A_CLK5P	MAKE_BASE=TRUE NO_TEST=TRUE
16	TP_MEM_A_CLK5N	=	NC_MEM_A_CLK5N	MAKE_BASE=TRUE NO_TEST=TRUE
15	TP_MEM_B_CLK2P	=	NC_MEM_B_CLK2P	MAKE_BASE=TRUE NO_TEST=TRUE
15	TP_MEM_B_CLK2N	=	NC_MEM_B_CLK2N	MAKE_BASE=TRUE NO_TEST=TRUE
16	TP_MEM_B_CLK5P	=	NC_MEM_B_CLK5P	MAKE_BASE=TRUE NO_TEST=TRUE
16	TP_MEM_B_CLK5N	=	NC_MEM_B_CLK5N	MAKE_BASE=TRUE NO_TEST=TRUE

UNUSED GMUX JTAG FROM MCP

17	GMUX_JTAG_TCK_L	=	NC_GMUX_JTAG_TCK_L	MAKE_BASE=TRUE NO_TEST=TRUE
17	GMUX_JTAG_TDO	=	NC_GMUX_JTAG_TDO	MAKE_BASE=TRUE NO_TEST=TRUE
19	GMUX_JTAG_TDI	=	NC_GMUX_JTAG_TDI	MAKE_BASE=TRUE NO_TEST=TRUE
19	GMUX_JTAG_TMS	=	NC_GMUX_JTAG_TMS	MAKE_BASE=TRUE NO_TEST=TRUE

PAGE TITLE: UNUSED SIGNAL ALIAS

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SHEET

SIGNAL ALIAS

TP_MLB_RAM_VENDOR = MXM_GOOD (MAKE_BASE=TRUE)

PM_SLP_S3_L → R910 15 → PM_SLPS3_BUF2_L (MAKE_BASE=TRUE)
(P50 HAS A 100K TO GROUND)

R911 15 → PM_SLPS3_BUF1_L (MAKE_BASE=TRUE)
R912 100K

USB_EXTC_OC_L = USB_EXTD_OC_L (MAKE_BASE=TRUE)

K22/K23 Use one GPIO for both ports 2&3 OC
USB PORT 2 AND 3 (C AND D) SHARE OVER-CURRENT WITH PORT 2
PREVIOUSLY, PORT 3 HAD ITS OWN BUT EFI MAPS THAT TO EXPRESSCARD
SEE RDAR://6250424

PEG Slot Support

PEG_CLK100M_P	GPU_CLK100M_PCIE_P
PEG_CLK100M_N	GPU_CLK100M_PCIE_N
=PEG_R2D_C_P<0..15>	PEG_R2D_C_P<0..15>
=PEG_R2D_C_N<0..15>	PEG_R2D_C_N<0..15>
=PEG_D2R_P<0..15>	PEG_D2R_P<0..15>
=PEG_D2R_N<0..15>	PEG_D2R_N<0..15>
PEG_PRSNT_L	MXM_DETECT_L

(all MAKE_BASE=TRUE)

DisplayPort / TMDS Support

=MCP_HDMI_TXC_P	DP_IG_ML_P<3>
=MCP_HDMI_TXC_N	DP_IG_ML_N<3>
=MCP_HDMI_TXD_P<0..2>	DP_IG_ML_P<2..0>
=MCP_HDMI_TXD_N<0..2>	DP_IG_ML_N<2..0>
=MCP_HDMI_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	DP_IG_HPD

(all MAKE_BASE=TRUE)

=DVI_HPD_GMUX_INT = HPLUG_DET2 (MAKE_BASE=TRUE) → R900 20K

MCP79 PCIe PRSNT# Straps

PCIE_FW_PRSNT_L
PCIE_MINI_PRSNT_L

Audio Mux aliasing

AUD_SPDIF_IN = AUD_SPDIF_IN_CODEC (MAKE_BASE=TRUE)

this alias connects spdif directly from the I/O port to the codec
K23 uses a mux between the DP audio source and the audio in port

AUD_MUX_CNTRL = TP_AUD_MUX_CNTRL (MAKE_BASE=TRUE)

K23 Uses this to control the DP audio mux. K22 does not need this signal

Platform Reset Connections

LPC Reset (Unbuffered)

LPC_RESET_L → R981 33 (PLACEMENT_NOTE=Place close to U1400) → DEBUG_RESET_L
R983 33 (PLACEMENT_NOTE=Place close to U1400) → SMC_LRESET_L

PCIE Reset (Unbuffered)

PCIE_RESET_L → R992 0 → FW_RESET_L
R991 0 → MINI_RESET_L
R990 0 → PEG_RESET_L
R971 0 → PCA9557D_RESET_L
R993 0 → CARDREADER_PLT_RST_L

MEM_VTT_EN_R → R972 33 → DDRVTT_EN
NO STUFF C973 0.47UF

LPC_CLK33M_SMC_R → R925 33 (PLACEMENT_NOTE=Place close to U1400) → LPC_CLK33M_SMC
R926 33 (PLACEMENT_NOTE=Place close to U1400) → LPC_CLK33M_LPCPLUS

PM_CLK32K_SUSCLK_R → R929 22 (PLACEMENT_NOTE=Place close to U1400) → PM_CLK32K_SUSCLK

MCP_CPUVDD_EN WILL ASSERT AFTER MCP_PS_PWRGD IS UP

MCP_CPUVDD_EN → R930 22 (PLACEMENT_NOTE=Place close to U1400) → MCP_CPU_VLD

=MCP_MII_RXER = MCP_MII_NU (MAKE_BASE=TRUE)
=MCP_MII_COL
=MCP_MII_CRS
→ R955 47K

PAGE TITLE	SIGNAL ALIASES
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CRITICAL

J1000
WOLFDALE-SKT-1
BGA-NOHSK
CPU
(1 OF 7)

ADDR GROUP0
CONTROL
SB
ADDR GROUP1
CLK

FSB_A_L<3>	L5	A_3*	
FSB_A_L<4>	P6	A_4*	
FSB_A_L<5>	M5	A_5*	
FSB_A_L<6>	L4	A_6*	
FSB_A_L<7>	M4	A_7*	
FSB_A_L<8>	R4	A_8*	
FSB_A_L<9>	T5	A_9*	
FSB_A_L<10>	U6	A_10*	
FSB_A_L<11>	T4	A_11*	
FSB_A_L<12>	U5	A_12*	
FSB_A_L<13>	U4	A_13*	
FSB_A_L<14>	V5	A_14*	
FSB_A_L<15>	V4	A_15*	
FSB_A_L<16>	W5	A_16*	
FSB_ADSTB_L<0>	R6	ADSTB_0*	
FSB_REQ_L<0>	K4	REQ_0*	
FSB_REQ_L<1>	J5	REQ_1*	
FSB_REQ_L<2>	M6	REQ_2*	
FSB_REQ_L<3>	K6	REQ_3*	
FSB_REQ_L<4>	J6	REQ_4*	
FSB_A_L<17>	AB6	A_17*	
FSB_A_L<18>	W6	A_18*	
FSB_A_L<19>	Y6	A_19*	
FSB_A_L<20>	Y4	A_20*	
FSB_A_L<21>	AA4	A_21*	
FSB_A_L<22>	AD6	A_22*	
FSB_A_L<23>	AA5	A_23*	
FSB_A_L<24>	AB5	A_24*	
FSB_A_L<25>	AC5	A_25*	
FSB_A_L<26>	AB4	A_26*	
FSB_A_L<27>	AF5	A_27*	
FSB_A_L<28>	AF4	A_28*	
FSB_A_L<29>	AG6	A_29*	
FSB_A_L<30>	AG4	A_30*	
FSB_A_L<31>	AG5	A_31*	
FSB_A_L<32>	AH4	A_32*	
FSB_A_L<33>	AH5	A_33*	
FSB_A_L<34>	AJ5	A_34*	
FSB_A_L<35>	AJ6	A_35*	
FSB_ADSTB_L<1>	AD5	ADSTB_1*	

ADS*	D2	FSB_ADS_L	
BNR*	C2	FSB_BNR_L	
BPRI*	G8	FSB_BPRI_L	
DEFER*	G7	FSB_DEFER_L	
DRDY*	C1	FSB_DRDY_L	
DBSY*	B2	FSB_DBSY_L	
BR_0*	F3	FSB_BREQ0_L	
IERR*	AB2	CPU_IERR_L	
INIT*	P3	CPU_INIT_L	
LOCK*	C3	FSB_LOCK_L	
RESET*	G23	FSB_CPURST_L	
RS_0*	B3	FSB_RS_L<0>	
RS_1*	F5	FSB_RS_L<1>	
RS_2*	A3	FSB_RS_L<2>	
TRDY*	E3	FSB_TRDY_L	
HIT*	D4	FSB_HIT_L	
HITM*	E4	FSB_HITM_L	
A20M*	K3	CPU_A20M_L	
FERR_PBE*	R3	CPU_FERR_L	
IGNNE*	N2	CPU_IGNNE_L	
STPCLK*	M3	CPU_STPCLK_L	
LINT0	K1	CPU_INTR	
LINT1	L1	CPU_NMI	
SMI*	P2	CPU_SMI_L	
BCLK_0	F28	FSB_CLK_CPU_P	
BCLK_1	G28	FSB_CLK_CPU_N	

PPCPU_VTT_OUT_LEFT 10 11 12

R1003 62 5% 1/16W MF-LF 402

=PPVTT_S0_CPU 6 50 55 71

R1004 200 5% 1/16W MF-LF 402

PPCPU_VTT_OUT_RIGHT 10 11 12

R1000 62 5% 1/16W MF-LF 402

PLACE W/ A TESTPOINT W/ A GND NEARBY

PPCPU_VTT_OUT_RIGHT 10 11 12

R1001 62 5% 1/16W MF-LF 402

CRITICAL

J1000
WOLFDALE-SKT-1
BGA-NOHSK
CPU
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FSB_D_L<0>	B4	D_0*	
FSB_D_L<1>	C5	D_1*	
FSB_D_L<2>	A4	D_2*	
FSB_D_L<3>	C6	D_3*	
FSB_D_L<4>	A5	D_4*	
FSB_D_L<5>	B6	D_5*	
FSB_D_L<6>	B7	D_6*	
FSB_D_L<7>	A7	D_7*	
FSB_D_L<8>	A10	D_8*	
FSB_D_L<9>	A11	D_9*	
FSB_D_L<10>	B10	D_10*	
FSB_D_L<11>	C11	D_11*	
FSB_D_L<12>	D8	D_12*	
FSB_D_L<13>	B12	D_13*	
FSB_D_L<14>	C12	D_14*	
FSB_D_L<15>	D11	D_15*	
FSB_DINV_L<0>	A8	DBI_0*	
FSB_DSTB_L_N<0>	C8	DSTBN_0*	
FSB_DSTB_L_P<0>	B9	DSTBP_0	
FSB_D_L<16>	G9	D_16*	
FSB_D_L<17>	F8	D_17*	
FSB_D_L<18>	F9	D_18*	
FSB_D_L<19>	E9	D_19*	
FSB_D_L<20>	D7	D_20*	
FSB_D_L<21>	E10	D_21*	
FSB_D_L<22>	D10	D_22*	
FSB_D_L<23>	F11	D_23*	
FSB_D_L<24>	F12	D_24*	
FSB_D_L<25>	D13	D_25*	
FSB_D_L<26>	E13	D_26*	
FSB_D_L<27>	G13	D_27*	
FSB_D_L<28>	F14	D_28*	
FSB_D_L<29>	G14	D_29*	
FSB_D_L<30>	F15	D_30*	
FSB_D_L<31>	G15	D_31*	
FSB_DINV_L<1>	G11	DBI_1*	
FSB_DSTB_L_N<1>	G12	DSTBN_1*	
FSB_DSTB_L_P<1>	E12	DSTBP_1	

D_32*	G16	FSB_D_L<32>	
D_33*	E15	FSB_D_L<33>	
D_34*	E16	FSB_D_L<34>	
D_35*	G18	FSB_D_L<35>	
D_36*	G17	FSB_D_L<36>	
D_37*	F17	FSB_D_L<37>	
D_38*	F18	FSB_D_L<38>	
D_39*	E18	FSB_D_L<39>	
D_40*	E19	FSB_D_L<40>	
D_41*	F20	FSB_D_L<41>	
D_42*	E21	FSB_D_L<42>	
D_43*	F21	FSB_D_L<43>	
D_44*	G21	FSB_D_L<44>	
D_45*	E22	FSB_D_L<45>	
D_46*	D22	FSB_D_L<46>	
D_47*	G22	FSB_D_L<47>	
DBI_2*	D19	FSB_DINV_L<2>	
DSTBN_2*	G20	FSB_DSTB_L_N<2>	
DSTBP_2	G19	FSB_DSTB_L_P<2>	
D_48*	D20	FSB_D_L<48>	
D_49*	D17	FSB_D_L<49>	
D_50*	A14	FSB_D_L<50>	
D_51*	C15	FSB_D_L<51>	
D_52*	C14	FSB_D_L<52>	
D_53*	B15	FSB_D_L<53>	
D_54*	C18	FSB_D_L<54>	
D_55*	B16	FSB_D_L<55>	
D_56*	A17	FSB_D_L<56>	
D_57*	B18	FSB_D_L<57>	
D_58*	C21	FSB_D_L<58>	
D_59*	B21	FSB_D_L<59>	
D_60*	B19	FSB_D_L<60>	
D_61*	A19	FSB_D_L<61>	
D_62*	A22	FSB_D_L<62>	
D_63*	B22	FSB_D_L<63>	
DBI_3*	C20	FSB_DINV_L<3>	
DSTBN_3*	A16	FSB_DSTB_L_N<3>	
DSTBP_3	C17	FSB_DSTB_L_P<3>	

CPU GTLREF

GTLREF VOLTAGE SHOULD BE 0.635 * VTT
(63.5% OF 1.2V) = 0.762V

12 11 10 PPCPU_VTT_OUT_LEFT

R1040 57.6 1% 1/16W MF-LF 402

R1042 10 1% 1/16W MF-LF 402

CPU_GTLREF_DIV0

CPU_GTLREF0 11 29 100

R1041 100 1% 1/16W MF-LF 402

C1040 1UF 10% 6.3V CERM 402

NOSTUFF C1041 220PF 10% 50V X7R-CERM 402

12 11 10 PPCPU_VTT_OUT_LEFT

R1043 57.6 1% 1/16W MF-LF 402

R1045 10 1% 1/16W MF-LF 402

CPU_GTLREF_DIV1

CPU_GTLREF1 11 29 100

R1044 100 1% 1/16W MF-LF 402

C1042 1UF 10% 6.3V CERM 402

NOSTUFF C1043 220PF 10% 50V X7R-CERM 402

PAGE TITLE
CPU FSB

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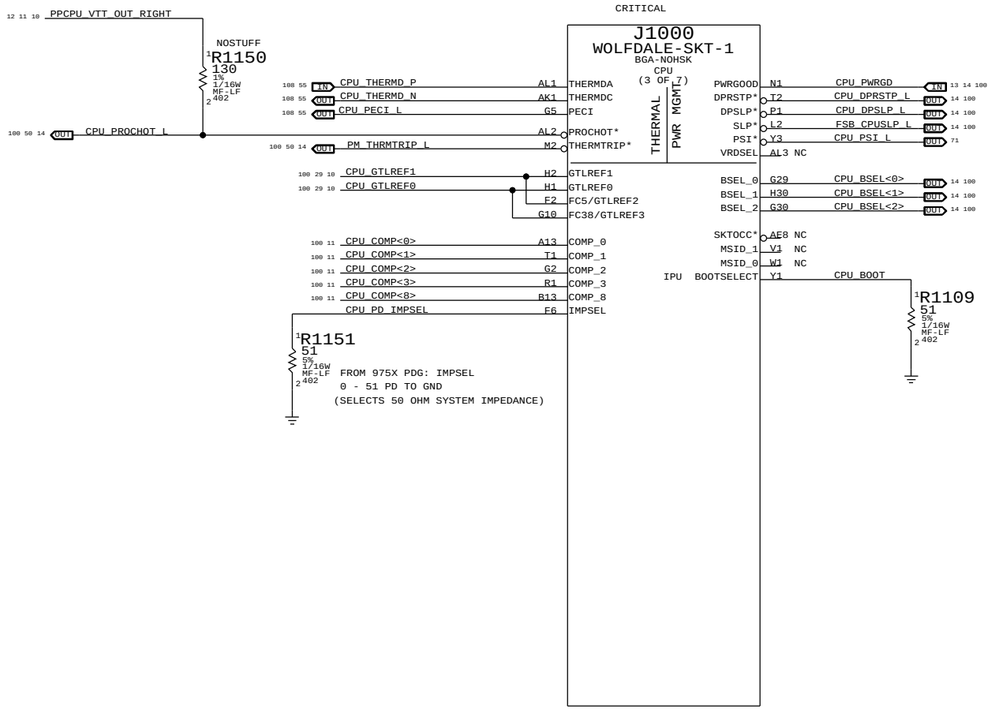
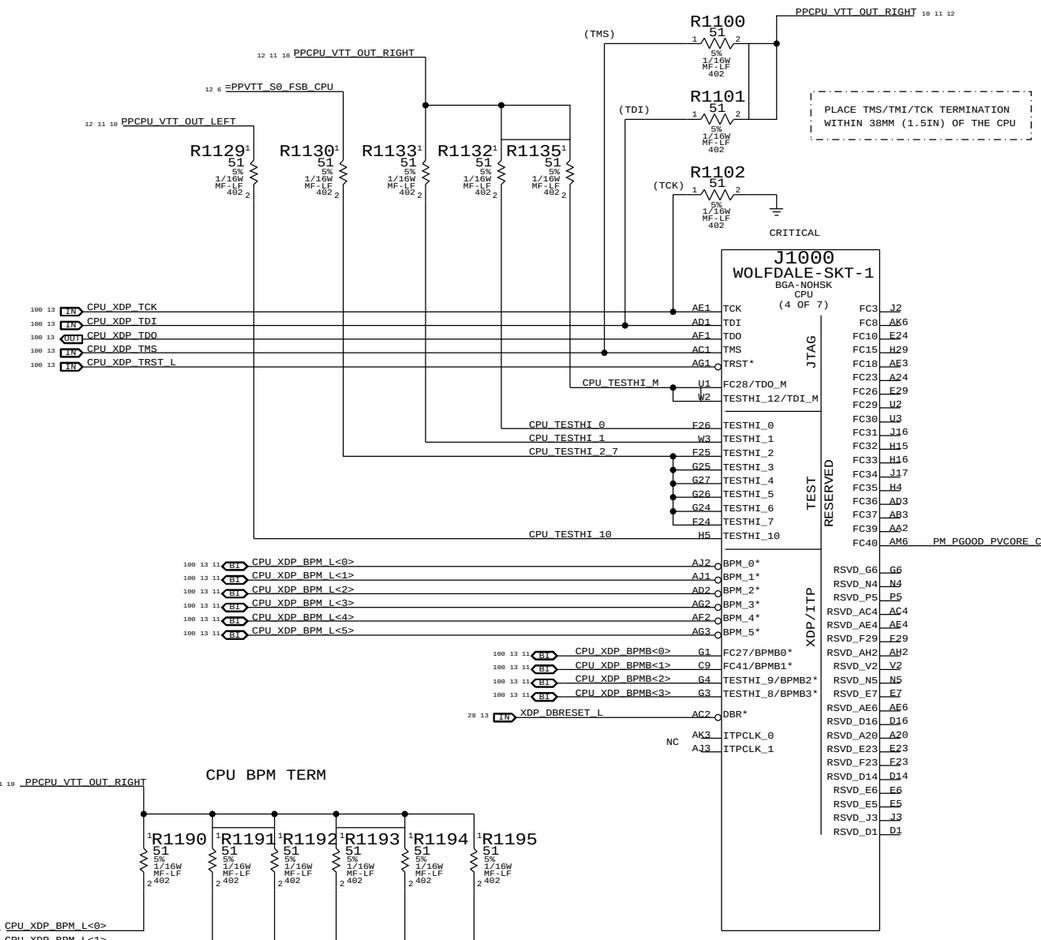
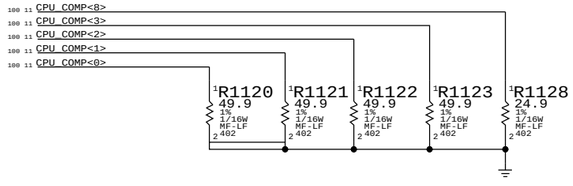
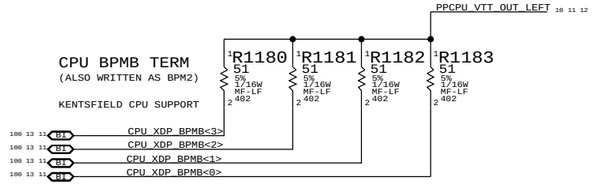
SHEET









PAGE TITLE
CPU TEST & MISC.

Apple Inc.

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POWER

VID PULLUPS WITH VREG

=PPVCORE_S0_CPU

CPU_VID<0>	AM2	VID_0
CPU_VID<1>	AL5	VID_1
CPU_VID<2>	AM3	VID_2
CPU_VID<3>	AL6	VID_3
CPU_VID<4>	AK4	VID_4
CPU_VID<5>	AL4	VID_5
CPU_VID<6>	AM5	VID_6
CPU_VID<7>	AM7	VID_7
CPU_VCCA	A23	VCCA
CPU_VSSA	B23	VSSA
CPU_VCCIOPLL	C23	VCCIOPLL
	D23	VCCPLL
CPU_VCC_SENSE	AN3	VCC_SENSE
CPU_VCC_PKG_SENSE_P	AN5	VCC_MB_REGULATION
CPU_VID_SELECT	AN7	VID_SELECT
TP_CPU_VSS_SENSE	AN4	VSS_SENSE
CPU_VCC_PKG_SENSE_N	AN6	VSS_MB_REGULATION

=PPVTT_S0_FSB_CPU

A25	VTT_A25
A26	VTT_A26
A27	VTT_A27
A28	VTT_A28
A29	VTT_A29
A30	VTT_A30
B25	VTT_B25
B26	VTT_B26
B27	VTT_B27
B28	VTT_B28
B29	VTT_B29
B30	VTT_B30
C25	VTT_C25
C26	VTT_C26
C27	VTT_C27
C28	VTT_C28
C29	VTT_C29
C30	VTT_C30
D25	VTT_D25
D26	VTT_D26
D27	VTT_D27
D28	VTT_D28
D29	VTT_D29
D30	VTT_D30

PPCPU_VTT_OUT_RIGHT
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR

PPCPU_VTT_OUT_LEFT
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR

AA1	VTT_OUT_RIGHT
J1	VTT_OUT_LEFT
F27	VTT_SEL

TP_VTT_SEL

AC8	
AD23	
AD24	
AD25	
AD26	
AD27	
AD28	
AD29	
AD30	
AD8	
AE11	
AE12	
AE14	
AE15	
AE18	
AE19	
AE21	
AE22	
AE23	
AE9	
AF11	
AF12	
AF14	
AF15	
AF18	
AF19	

VCCP

AC30 AC29 AC28 AC27 AC26 AC25 AC24 AC23 AB8 AA8 AL18 AL19 AL21 AL22 AL25 AL26 AL29 AL30 AL9 AM11 AM12 AM14 AM15 AM18 AM19 AM21 AM22 AM25 AM26 AM29 AM30 AM8 AM9 AN11 AN12 AN14 AN15 AN18 AN19 AN21 AN22 AN25 AN26 AN29 AN30 AN8 AN9 J10 J11 J12 J13 J14 J15 J18 J19 J20 J21 J22 J23 J24

VCCP

J25	
J26	
J27	
J28	
J29	
J30	
J8	
J9	
K23	
K24	
K25	
K26	
K27	
K28	
K29	
K30	
K8	
L8	
M23	
M24	
M25	
M26	
M27	
M28	
M29	
M30	
M8	
N23	
N24	
N25	
N26	
N27	
N28	
N29	
N30	
N8	
P8	
R8	
T23	
T24	
T25	
T26	
T27	
T28	
T29	
T30	
T8	
U23	
U24	
U25	
U26	
U27	
U28	
U29	
U30	
U8	
V8	
W23	
W24	
W25	
W26	
W27	
W28	
Y27	
Y26	
Y25	
Y24	
Y23	
W8	
W30	
Y8	
Y30	
Y29	
Y28	
W29	
AL15	
AL8	
AL11	
AL12	
AL14	

VCCP

AF21 AE22 AE8 AE9 AG11 AG12 AG14 AG15 AG18 AG19 AG21 AG22 AG25 AG26 AG27 AG28 AG29 AG30 AG8 AG9 AH11 AH12 AH14 AH15 AH18 AH19 AH21 AH22 AH25 AH26 AH27 AH28 AH29 AH30 AH8 AH9 AJ10 AJ11 AJ12 AJ14 AJ15 AJ18 AJ19 AJ21 AJ22 AJ25 AJ26 AK8 AK9 AK11 AK12 AK14 AK15 AK18 AK19 AK21 AK22 AK25 AK26

CRITICAL
J1000
WOLFDALE-SKT-1
BGA-NOHSK
CPU
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THIS IS FOR OLDER CPU SUPPORT
WILL PLACE FILTER BUT NOT CONNECT FOR WOLFDALE

CONROE
~125MA CURRENT

=PPVTT_S0_FSB_CPU
L1210 FERR-120-OHM-0.2A 0603
R1210 0 5% 1/10W MF-LF 603
R1211 0 5% 1/10W MF-LF 603

CPU_VCCIOPLL
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

CPU_VCCA_FLT
C1210 22UF 20% 6.3V CERM-X5R 805-3
C1213 10UF 20% 6.3V X5R 603
NOSTUFF C1211 1UF 10% 6.3V CERM 402
NOSTUFF C1212 1UF 10% 6.3V CERM 402

CPU_VCCA
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

CPU_VSSA
VOLTAGE=0V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

VCC PLL DECOUPLING

=PP1V5_S0_CPU_VCCPLL
C1280 10UF 20% 6.3V X5R 603
C1281 0.01UF 10% 16V CERM 402

PPCPU_VTT_OUT_LEFT
PPCPU_VTT_OUT_RIGHT
C1200 0.1UF 20% 10V CERM 402
C1201 0.1UF 20% 10V CERM 402

FSB VTT DECOUPLING

=PPVTT_S0_FSB_CPU
C1226 0.1UF 20% 10V CERM 402
C1234 0.1UF 20% 10V CERM 402
C1235 0.1UF 20% 10V CERM 402
C1236 0.1UF 20% 10V CERM 402
C1237 0.1UF 20% 10V CERM 402
C1238 0.1UF 20% 10V CERM 402

VCCP CORE DECOUPLING

(SEE VREG PAGE)

PPCPU_VTT_OUT_RIGHT
R1200 680 5% 1/16W MF-LF 402
CPU_VID_SELECT

CRITICAL
J1000
WOLFDALE-SKT-1
BGA-NOHSK
CPU
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A12	AG17
A15	AG20
A18	AG23
A2	AG24
A21	AG7
A6	AH1
A9	AH10
AA23	AH13
AA24	AH16
AA25	AH17
AA26	AH20
AA27	AH23
AA28	AH24
AA29	AH3
AA3	AH6
AA30	AJ10
AA6	AJ13
AA7	AJ16
AB1	AJ17
AB23	AJ20
AB24	AJ23
AB25	AJ24
AB26	AJ27
AB27	AJ28
AB28	AJ29
AB29	AJ30
AB30	AJ4
AB7	AK10
AC3	AK13
AC6	AK16
AC7	AK17
AD4	AK2
AD7	AK20
AE10	AK23
AE13	AK24
AE16	AK27
AE17	AK28
AE2	AK29
AE20	AK30
AE24	AK5
AE25	AK7
AE26	AL10
AE27	AL13
AE28	AL16
AE29	AL17
AE30	AL20
AE5	AL23
AE7	AL24
AF10	AL27
AF13	AL28
AF16	AM1
AF17	AM10
AF20	AM13
AF23	AM16
AF24	AM17
AF25	AM20
AF26	AM23
AF27	AM24
AF28	AM27
AF29	AM28
AF3	AM4
AF30	AN1
AF6	AN10
AF7	AN13
AG10	AN16
AG13	AN17
AG16	AH7
AL7	AJ7

GND GND

GND

CRITICAL
J1000
WOLFDALE-SKT-1
BGA-NOHSK
CPU
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AN2	H6
AN20	H7
AN23	H8
AN24	H9
AN27	J4
AN28	J7
B1	K2
B11	K5
B14	K7
B17	L23
B20	L24
B24	L25
B5	L26
B8	L27
C10	L28
C13	L29
C16	L3
C19	L30
C22	L6
C24	L7
C4	M1
C7	M7
D12	N3
D15	N6
D18	N7
D21	P23
D24	P24
D3	P25
D5	P26
D6	P27
D9	P28
E11	P29
E14	P30
E17	P4
E2	P7
E20	R2
E25	R23
E26	R24
E27	R25
E28	R26
E8	R27
F10	R28
F13	R29
F16	R30
F19	R5
F22	R7
F4	T3
F7	T6
H10	T7
H11	U7
H12	V23
H13	V24
H14	V25
H17	V26
H18	V27
H19	V28
H20	V29
H21	V3
H22	V30
H23	V6
H24	V7
H25	W4
H26	W7
H27	Y2
H28	Y5
H3	Y7

GND GND

GND

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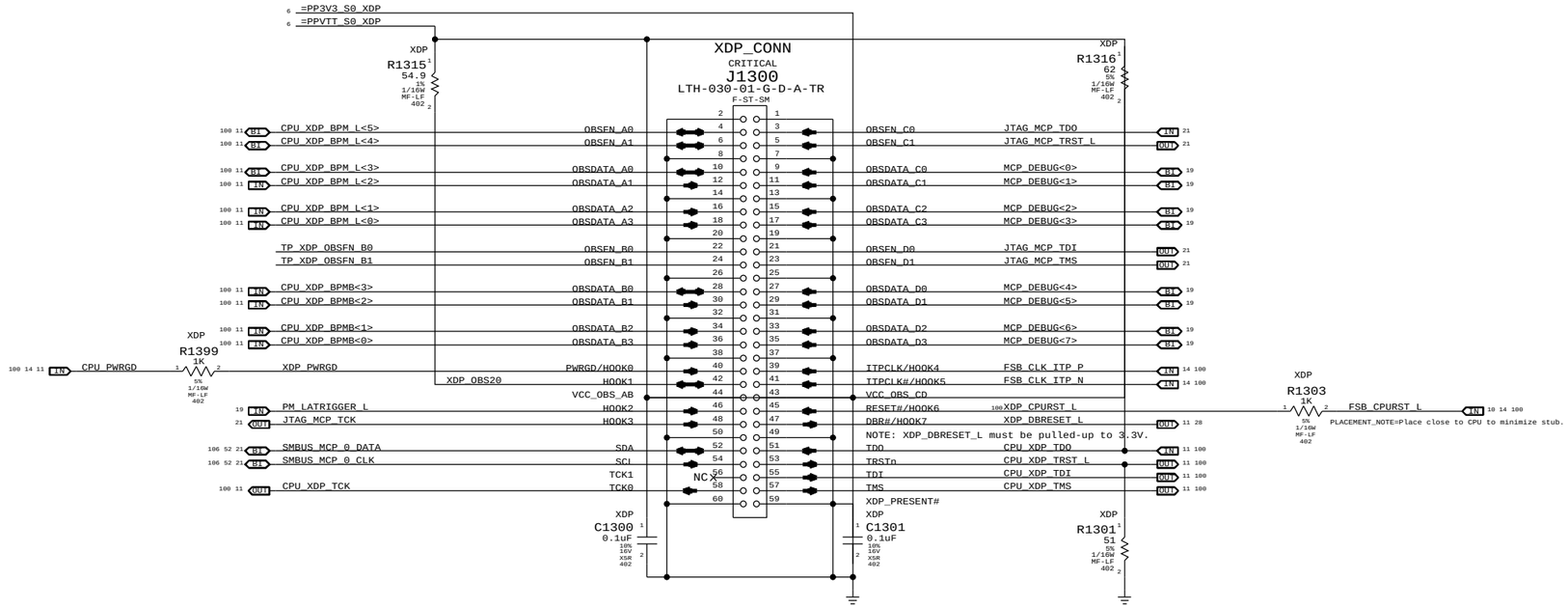
MCP79-specific pinout



PAGE TITLE
eXtended Debug Port (XDP)

Apple Inc.

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FSB

FSB_DSTB_L_P<0>	T40	CPU_DSTBP0*	
FSB_DSTB_L_N<0>	U40	CPU_DSTBN0*	
FSB_DINV_L<0>	V41	CPU_DBI0*	
FSB_DSTB_L_P<1>	W39	CPU_DSTBP1*	
FSB_DSTB_L_N<1>	W37	CPU_DSTBN1*	
FSB_DINV_L<1>	V35	CPU_DBI1*	
FSB_DSTB_L_P<2>	N37	CPU_DSTBP2*	
FSB_DSTB_L_N<2>	L36	CPU_DSTBN2*	
FSB_DINV_L<2>	N35	CPU_DBI2*	
FSB_DSTB_L_P<3>	M39	CPU_DSTBP3*	
FSB_DSTB_L_N<3>	M41	CPU_DSTBN3*	
FSB_DINV_L<3>	J41	CPU_DBI3*	
FSB_A_L<3>	AB35	CPU_A3*	
FSB_A_L<4>	AE37	CPU_A4*	
FSB_A_L<5>	AC33	CPU_A5*	
FSB_A_L<6>	AC35	CPU_A6*	
FSB_A_L<7>	AC34	CPU_A7*	
FSB_A_L<8>	AE35	CPU_A8*	
FSB_A_L<9>	AE34	CPU_A9*	
FSB_A_L<10>	AG39	CPU_A10*	
FSB_A_L<11>	AE33	CPU_A11*	
FSB_A_L<12>	AG38	CPU_A12*	
FSB_A_L<13>	AG37	CPU_A13*	
FSB_A_L<14>	AF35	CPU_A14*	
FSB_A_L<15>	AG35	CPU_A15*	
FSB_A_L<16>	AG34	CPU_A16*	
FSB_A_L<17>	AJ34	CPU_A17*	
FSB_A_L<18>	AG33	CPU_A18*	
FSB_A_L<19>	AJ38	CPU_A19*	
FSB_A_L<20>	AJ37	CPU_A20*	
FSB_A_L<21>	AJ35	CPU_A21*	
FSB_A_L<22>	AL37	CPU_A22*	
FSB_A_L<23>	AJ36	CPU_A23*	
FSB_A_L<24>	AL39	CPU_A24*	
FSB_A_L<25>	AL38	CPU_A25*	
FSB_A_L<26>	AJ33	CPU_A26*	
FSB_A_L<27>	AL35	CPU_A27*	
FSB_A_L<28>	AL34	CPU_A28*	
FSB_A_L<29>	AN37	CPU_A29*	
FSB_A_L<30>	AL33	CPU_A30*	
FSB_A_L<31>	AN38	CPU_A31*	
FSB_A_L<32>	AN35	CPU_A32*	
FSB_A_L<33>	AN36	CPU_A33*	
FSB_A_L<34>	AR39	CPU_A34*	
FSB_A_L<35>	AN34	CPU_A35*	
FSB_ADSTB_L<0>	AE36	CPU_ADSTB0*	
FSB_ADSTB_L<1>	AK35	CPU_ADSTB1*	
FSB_REQ_L<0>	AC38	CPU_REQ0*	
FSB_REQ_L<1>	AA33	CPU_REQ1*	
FSB_REQ_L<2>	AE38	CPU_REQ2*	
FSB_REQ_L<3>	AC37	CPU_REQ3*	
FSB_REQ_L<4>	AC39	CPU_REQ4*	
FSB_ADS_L	AD42	CPU_ADS*	
FSB_BNR_L	AD43	CPU_BNR*	
FSB_BREQ0_L	AE40	CPU_BR0*	
FSB_BREQ1_L	AL32	CPU_BR1*	
FSB_DBSY_L	AD39	CPU_DBSY*	
FSB_DRDY_L	AD41	CPU_DRDY*	
FSB_HIT_L	AB42	CPU_HIT*	
FSB_HITM_L	AD40	CPU_HITM*	
FSB_LOCK_L	AC43	CPU_LOCK*	
FSB_TRDY_L	AE41	CPU_TRDY*	
CPU_PECI_MCP	E41	CPU_PECI	
CPU_PROCHOT_L	AJ41	CPU_PROCHOT*	
	AG43	CPU_THERMTRIP*	
CPU_FERR_L	AH40	CPU_FERR*	
	F42	CPU_BSEL2	
	D42	CPU_BSEL1	
	F41	CPU_BSEL0	
FSB_RS_L<0>	AC41	CPU_RS0*	
FSB_RS_L<1>	AB41	CPU_RS1*	
FSB_RS_L<2>	AC42	CPU_RS2*	
	AG27	V1P1_DLLDLCELL_AVDD	206 mA
	AH27	V1P1_PLL_MCLK	20 mA
	AG28	V1P1_PLL_FSB	29 mA
	AH28	V1P1_PLL_CPU	15 mA
MCP_BCLK_VML_COMP_VDD	AM39	BCLK_VML_COMP_VDD	
MCP_BCLK_VML_COMP_GND	AM40	BCLK_VML_COMP_GND	
MCP_CPU_COMP_VCC	AM43	CPU_COMP_VCC	
MCP_CPU_COMP_GND	AM42	CPU_COMP_GND	

CPU_D0*	Y41	FSB_D_L<0>	
CPU_D1*	Y43	FSB_D_L<1>	
CPU_D2*	Y40	FSB_D_L<2>	
CPU_D3*	W42	FSB_D_L<3>	
CPU_D4*	Y42	FSB_D_L<4>	
CPU_D5*	Y39	FSB_D_L<5>	
CPU_D6*	V42	FSB_D_L<6>	
CPU_D7*	W41	FSB_D_L<7>	
CPU_D8*	T41	FSB_D_L<8>	
CPU_D9*	T43	FSB_D_L<9>	
CPU_D10*	T42	FSB_D_L<10>	
CPU_D11*	T39	FSB_D_L<11>	
CPU_D12*	U41	FSB_D_L<12>	
CPU_D13*	R41	FSB_D_L<13>	
CPU_D14*	P42	FSB_D_L<14>	
CPU_D15*	R42	FSB_D_L<15>	
CPU_D16*	AA38	FSB_D_L<16>	
CPU_D17*	AA35	FSB_D_L<17>	
CPU_D18*	AA36	FSB_D_L<18>	
CPU_D19*	AA37	FSB_D_L<19>	
CPU_D20*	AA34	FSB_D_L<20>	
CPU_D21*	W33	FSB_D_L<21>	
CPU_D22*	W34	FSB_D_L<22>	
CPU_D23*	W35	FSB_D_L<23>	
CPU_D24*	W38	FSB_D_L<24>	
CPU_D25*	U33	FSB_D_L<25>	
CPU_D26*	U34	FSB_D_L<26>	
CPU_D27*	U35	FSB_D_L<27>	
CPU_D28*	U36	FSB_D_L<28>	
CPU_D29*	U37	FSB_D_L<29>	
CPU_D30*	R33	FSB_D_L<30>	
CPU_D31*	U38	FSB_D_L<31>	
CPU_D32*	R35	FSB_D_L<32>	
CPU_D33*	R34	FSB_D_L<33>	
CPU_D34*	P35	FSB_D_L<34>	
CPU_D35*	N34	FSB_D_L<35>	
CPU_D36*	R38	FSB_D_L<36>	
CPU_D37*	R37	FSB_D_L<37>	
CPU_D38*	N33	FSB_D_L<38>	
CPU_D39*	R39	FSB_D_L<39>	
CPU_D40*	N36	FSB_D_L<40>	
CPU_D41*	N38	FSB_D_L<41>	
CPU_D42*	L37	FSB_D_L<42>	
CPU_D43*	L38	FSB_D_L<43>	
CPU_D44*	L39	FSB_D_L<44>	
CPU_D45*	J37	FSB_D_L<45>	
CPU_D46*	J38	FSB_D_L<46>	
CPU_D47*	J39	FSB_D_L<47>	
CPU_D48*	H40	FSB_D_L<48>	
CPU_D49*	L42	FSB_D_L<49>	
CPU_D50*	P41	FSB_D_L<50>	
CPU_D51*	M40	FSB_D_L<51>	
CPU_D52*	N40	FSB_D_L<52>	
CPU_D53*	N41	FSB_D_L<53>	
CPU_D54*	K42	FSB_D_L<54>	
CPU_D55*	M42	FSB_D_L<55>	
CPU_D56*	M43	FSB_D_L<56>	
CPU_D57*	L41	FSB_D_L<57>	
CPU_D58*	H42	FSB_D_L<58>	
CPU_D59*	H41	FSB_D_L<59>	
CPU_D60*	J40	FSB_D_L<60>	
CPU_D61*	K41	FSB_D_L<61>	
CPU_D62*	H43	FSB_D_L<62>	
CPU_D63*	H39	FSB_D_L<63>	
CPU_BPRI*	AA41	FSB_BPRI_L	
CPU_DEFER*	AA40	FSB_DEFER_L	
BCLK_OUT_CPU_P	G42	FSB_CLK_CPU_P	
BCLK_OUT_CPU_N	G41	FSB_CLK_CPU_N	
BCLK_OUT_ITP_P	AL43	FSB_CLK_ITP_P	
BCLK_OUT_ITP_N	AL42	FSB_CLK_ITP_N	
BCLK_OUT_NB_P	AL41	FSB_CLK_MCP_P	
BCLK_OUT_NB_N	AK42	FSB_CLK_MCP_N	
BCLK_IN_N	AK41		
BCLK_IN_P	AJ40		
CPU_A20M*	AF41	CPU_A20M_L	
CPU_IGNNE*	AH39	CPU_IGNNE_L	
CPU_INIT*	AH42	CPU_INIT_L	
CPU_INTR	AF42	CPU_INTR	
CPU_NMI	AG41	CPU_NMI	
CPU_SMI*	AH41	CPU_SMI_L	
CPU_PWRGD	AH43	CPU_PWRGD	
CPU_RESET*	H38	FSB_CPURST_L	
CPU_SLP*	AM33	FSB_CPUSLP_L	
CPU_DPSLP*	AN33	CPU_DPSLP_L	
CPU_DPWR*	AM32	NC	
CPU_STPCLK*	AG42	CPU_STPCLK_L	
CPU_DPRSTP*	AN32	CPU_DPRSTP_L	

=PP1V05_S0_MCP_FSB
R1410 62 5% 1/16W MF-LF 402
R1416 62 5% 1/16W MF-LF 402
PM_THRMTRIP_L
R1420 470 5% 1/16W MF-LF 402
R1421 470 5% 1/16W MF-LF 402
R1422 470 5% 1/16W MF-LF 402
CPU_BSEL<2>
CPU_BSEL<1>
CPU_BSEL<0>
PP1V05_S0_MCP_PLL_FSB
270 mA (A01)
R1430 49.9 1% 1/16W MF-LF 402
R1435 49.9 1% 1/16W MF-LF 402
R1431 49.9 1% 1/16W MF-LF 402
R1436 49.9 1% 1/16W MF-LF 402

Loop-back clock for delay matching.

=PP1V05_S0_MCP_FSB
NO STUFF
R1440 150 5% 1/16W MF-LF 402

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

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Apple Inc.

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MEMORY PARTITION 0

MEM_A_DQ<63>	AL8	MDQ0_63	MDQS0_7_P	AL10	MEM_A_DQS_P<7>	33	101
MEM_A_DQ<62>	AL9	MDQ0_62	MDQS0_7_N	AL11	MEM_A_DQS_N<7>	33	101
MEM_A_DQ<61>	AP9	MDQ0_61	MDQS0_6_P	AR8	MEM_A_DQS_P<6>	33	101
MEM_A_DQ<60>	AN9	MDQ0_60	MDQS0_6_N	AR9	MEM_A_DQS_N<6>	33	101
MEM_A_DQ<59>	AL6	MDQ0_59	MDQS0_5_P	AW7	MEM_A_DQS_P<5>	33	101
MEM_A_DQ<58>	AL7	MDQ0_58	MDQS0_5_N	AW8	MEM_A_DQS_N<5>	33	101
MEM_A_DQ<57>	AN6	MDQ0_57	MDQS0_4_P	AP13	MEM_A_DQS_P<4>	33	101
MEM_A_DQ<56>	AN7	MDQ0_56	MDQS0_4_N	AR13	MEM_A_DQS_N<4>	33	101
MEM_A_DQ<55>	AR6	MDQ0_55	MDQS0_3_P	AV25	MEM_A_DQS_P<3>	33	101
MEM_A_DQ<54>	AR7	MDQ0_54	MDQS0_3_N	AW25	MEM_A_DQS_N<3>	33	101
MEM_A_DQ<53>	AV6	MDQ0_53	MDQS0_2_P	AU30	MEM_A_DQS_P<2>	33	101
MEM_A_DQ<52>	AW5	MDQ0_52	MDQS0_2_N	AU29	MEM_A_DQS_N<2>	33	101
MEM_A_DQ<51>	AN10	MDQ0_51	MDQS0_1_P	AT35	MEM_A_DQS_P<1>	33	101
MEM_A_DQ<50>	AR5	MDQ0_50	MDQS0_1_N	AU35	MEM_A_DQS_N<1>	33	101
MEM_A_DQ<49>	AU6	MDQ0_49	MDQS0_0_P	AU39	MEM_A_DQS_P<0>	33	101
MEM_A_DQ<48>	AV5	MDQ0_48	MDQS0_0_N	AT39	MEM_A_DQS_N<0>	33	101
MEM_A_DQ<47>	AU7	MDQ0_47					
MEM_A_DQ<46>	AU8	MDQ0_46					
MEM_A_DQ<45>	AW9	MDQ0_45					
MEM_A_DQ<44>	AP11	MDQ0_44					
MEM_A_DQ<43>	AW6	MDQ0_43					
MEM_A_DQ<42>	AY5	MDQ0_42					
MEM_A_DQ<41>	AU9	MDQ0_41					
MEM_A_DQ<40>	AV9	MDQ0_40					
MEM_A_DQ<39>	AU11	MDQ0_39					
MEM_A_DQ<38>	AV11	MDQ0_38					
MEM_A_DQ<37>	AV13	MDQ0_37					
MEM_A_DQ<36>	AW13	MDQ0_36					
MEM_A_DQ<35>	AR11	MDQ0_35					
MEM_A_DQ<34>	AT11	MDQ0_34					
MEM_A_DQ<33>	AR14	MDQ0_33					
MEM_A_DQ<32>	AU13	MDQ0_32					
MEM_A_DQ<31>	AR26	MDQ0_31					
MEM_A_DQ<30>	AU25	MDQ0_30					
MEM_A_DQ<29>	AT27	MDQ0_29					
MEM_A_DQ<28>	AU27	MDQ0_28					
MEM_A_DQ<27>	AP25	MDQ0_27					
MEM_A_DQ<26>	AR25	MDQ0_26					
MEM_A_DQ<25>	AP27	MDQ0_25					
MEM_A_DQ<24>	AR27	MDQ0_24					
MEM_A_DQ<23>	AP29	MDQ0_23					
MEM_A_DQ<22>	AR29	MDQ0_22					
MEM_A_DQ<21>	AP31	MDQ0_21					
MEM_A_DQ<20>	AR31	MDQ0_20					
MEM_A_DQ<19>	AV27	MDQ0_19					
MEM_A_DQ<18>	AN29	MDQ0_18					
MEM_A_DQ<17>	AV29	MDQ0_17					
MEM_A_DQ<16>	AN31	MDQ0_16					
MEM_A_DQ<15>	AU31	MDQ0_15					
MEM_A_DQ<14>	AR33	MDQ0_14					
MEM_A_DQ<13>	AV37	MDQ0_13					
MEM_A_DQ<12>	AW37	MDQ0_12					
MEM_A_DQ<11>	AT31	MDQ0_11					
MEM_A_DQ<10>	AV31	MDQ0_10					
MEM_A_DQ<9>	AT37	MDQ0_9					
MEM_A_DQ<8>	AU37	MDQ0_8					
MEM_A_DQ<7>	AW39	MDQ0_7					
MEM_A_DQ<6>	AV39	MDQ0_6					
MEM_A_DQ<5>	AR37	MDQ0_5					
MEM_A_DQ<4>	AR38	MDQ0_4					
MEM_A_DQ<3>	AV38	MDQ0_3					
MEM_A_DQ<2>	AW38	MDQ0_2					
MEM_A_DQ<1>	AR35	MDQ0_1					
MEM_A_DQ<0>	AP35	MDQ0_0					
MEM_A_DM<7>	AN5	MDQM0_7					
MEM_A_DM<6>	AU5	MDQM0_6					
MEM_A_DM<5>	AR10	MDQM0_5					
MEM_A_DM<4>	AN13	MDQM0_4					
MEM_A_DM<3>	AN27	MDQM0_3					
MEM_A_DM<2>	AW29	MDQM0_2					
MEM_A_DM<1>	AV35	MDQM0_1					
MEM_A_DM<0>	AR34	MDQM0_0					

MRAS0*	AV17	MEM_A_RAS_L			
MCAS0*	AP17	MEM_A_CAS_L			
MWE0*	AR17	MEM_A_WE_L			
MBA0_2	AP23	MEM_A_BA<2>			
MBA0_1	AP19	MEM_A_BA<1>			
MBA0_0	AW17	MEM_A_BA<0>			
MA0_14	AR23	MEM_A_A<14>			
MA0_13	AU15	MEM_A_A<13>			
MA0_12	AN23	MEM_A_A<12>			
MA0_11	AW21	MEM_A_A<11>			
MA0_10	AN19	MEM_A_A<10>			
MA0_9	AV21	MEM_A_A<9>			
MA0_8	AR22	MEM_A_A<8>			
MA0_7	AU21	MEM_A_A<7>			
MA0_6	AP21	MEM_A_A<6>			
MA0_5	AR21	MEM_A_A<5>			
MA0_4	AN21	MEM_A_A<4>			
MA0_3	AV19	MEM_A_A<3>			
MA0_2	AU19	MEM_A_A<2>			
MA0_1	AT19	MEM_A_A<1>			
MA0_0	AR19	MEM_A_A<0>			

MEMORY CONTROL 0A

MCLK0A_2_P	AW33	TP_MEM_A_CLK2P	8		
MCLK0A_2_N	AV33	TP_MEM_A_CLK2N	8		
MCLK0A_1_P	BA24	MEM_A_CLK_P<1>			
MCLK0A_1_N	AY24	MEM_A_CLK_N<1>			
MCLK0A_0_P	BB20	MEM_A_CLK_P<0>			
MCLK0A_0_N	BC20	MEM_A_CLK_N<0>			
MCS0A_1*	AT15	MEM_A_CS_L<1>			
MCS0A_0*	AR18	MEM_A_CS_L<0>			
MODT0A_1	AP15	MEM_A_ODT<1>			
MODT0A_0	AV15	MEM_A_ODT<0>			
MCKE0A_1	AU23	MEM_A_CKE<1>			
MCKE0A_0	AT23	MEM_A_CKE<0>			

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MEMORY PARTITION 1

MEM_B_DQ<63>	AT4	MDQ1_63	MDQS1_7_P	AT2	MEM_B_DQS_P<7>	33	101
MEM_B_DQ<62>	AT3	MDQ1_62	MDQS1_7_N	AT1	MEM_B_DQS_N<7>	33	101
MEM_B_DQ<61>	AV2	MDQ1_61	MDQS1_6_P	AY2	MEM_B_DQS_P<6>	33	101
MEM_B_DQ<60>	AV3	MDQ1_60	MDQS1_6_N	AY1	MEM_B_DQS_N<6>	33	101
MEM_B_DQ<59>	AR4	MDQ1_59	MDQS1_5_P	BB6	MEM_B_DQS_P<5>	33	101
MEM_B_DQ<58>	AR3	MDQ1_58	MDQS1_5_N	BA6	MEM_B_DQS_N<5>	33	101
MEM_B_DQ<57>	AU2	MDQ1_57	MDQS1_4_P	BA10	MEM_B_DQS_P<4>	33	101
MEM_B_DQ<56>	AU3	MDQ1_56	MDQS1_4_N	AY11	MEM_B_DQS_N<4>	33	101
MEM_B_DQ<55>	AY4	MDQ1_55	MDQS1_3_P	BB33	MEM_B_DQS_P<3>	33	101
MEM_B_DQ<54>	AY3	MDQ1_54	MDQS1_3_N	BA33	MEM_B_DQS_N<3>	33	101
MEM_B_DQ<53>	BB3	MDQ1_53	MDQS1_2_P	BB37	MEM_B_DQS_P<2>	33	101
MEM_B_DQ<52>	BC3	MDQ1_52	MDQS1_2_N	BA37	MEM_B_DQS_N<2>	33	101
MEM_B_DQ<51>	AW4	MDQ1_51	MDQS1_1_P	BA43	MEM_B_DQS_P<1>	33	101
MEM_B_DQ<50>	AW3	MDQ1_50	MDQS1_1_N	AY42	MEM_B_DQS_N<1>	33	101
MEM_B_DQ<49>	BA3	MDQ1_49	MDQS1_0_P	AT42	MEM_B_DQS_P<0>	33	101
MEM_B_DQ<48>	BB2	MDQ1_48	MDQS1_0_N	AT43	MEM_B_DQS_N<0>	33	101
MEM_B_DQ<47>	BB5	MDQ1_47					
MEM_B_DQ<46>	BA5	MDQ1_46					
MEM_B_DQ<45>	BA8	MDQ1_45					
MEM_B_DQ<44>	BC8	MDQ1_44					
MEM_B_DQ<43>	BB4	MDQ1_43					
MEM_B_DQ<42>	BC4	MDQ1_42					
MEM_B_DQ<41>	BA7	MDQ1_41					
MEM_B_DQ<40>	AY8	MDQ1_40					
MEM_B_DQ<39>	BA9	MDQ1_39					
MEM_B_DQ<38>	BB10	MDQ1_38					
MEM_B_DQ<37>	BB12	MDQ1_37					
MEM_B_DQ<36>	AW12	MDQ1_36					
MEM_B_DQ<35>	BB8	MDQ1_35					
MEM_B_DQ<34>	BB9	MDQ1_34					
MEM_B_DQ<33>	AY12	MDQ1_33					
MEM_B_DQ<32>	BA12	MDQ1_32					
MEM_B_DQ<31>	BC32	MDQ1_31					
MEM_B_DQ<30>	AW32	MDQ1_30					
MEM_B_DQ<29>	BA35	MDQ1_29					
MEM_B_DQ<28>	AY36	MDQ1_28					
MEM_B_DQ<27>	BA32	MDQ1_27					
MEM_B_DQ<26>	BB32	MDQ1_26					
MEM_B_DQ<25>	BA34	MDQ1_25					
MEM_B_DQ<24>	AY35	MDQ1_24					
MEM_B_DQ<23>	BC36	MDQ1_23					
MEM_B_DQ<22>	AW36	MDQ1_22					
MEM_B_DQ<21>	BA39	MDQ1_21					
MEM_B_DQ<20>	AY40	MDQ1_20					
MEM_B_DQ<19>	BA36	MDQ1_19					
MEM_B_DQ<18>	BB36	MDQ1_18					
MEM_B_DQ<17>	BA38	MDQ1_17					
MEM_B_DQ<16>	AY39	MDQ1_16					
MEM_B_DQ<15>	BB40	MDQ1_15					
MEM_B_DQ<14>	AW40	MDQ1_14					
MEM_B_DQ<13>	AV42	MDQ1_13					
MEM_B_DQ<12>	AV41	MDQ1_12					
MEM_B_DQ<11>	BA40	MDQ1_11					
MEM_B_DQ<10>	BC40	MDQ1_10					
MEM_B_DQ<9>	AW42	MDQ1_9					
MEM_B_DQ<8>	AW41	MDQ1_8					
MEM_B_DQ<7>	AT40	MDQ1_7					
MEM_B_DQ<6>	AT41	MDQ1_6					
MEM_B_DQ<5>	AP41	MDQ1_5					
MEM_B_DQ<4>	AN40	MDQ1_4					
MEM_B_DQ<3>	AU40	MDQ1_3					
MEM_B_DQ<2>	AU41	MDQ1_2					
MEM_B_DQ<1>	AR41	MDQ1_1					
MEM_B_DQ<0>	AP42	MDQ1_0					
MEM_B_DM<7>	AT5	MDQM1_7					
MEM_B_DM<6>	BA2	MDQM1_6					
MEM_B_DM<5>	AY7	MDQM1_5					
MEM_B_DM<4>	BA11	MDQM1_4					
MEM_B_DM<3>	BB34	MDQM1_3					
MEM_B_DM<2>	BB38	MDQM1_2					
MEM_B_DM<1>	AY43	MDQM1_1					
MEM_B_DM<0>	AR42	MDQM1_0					

MRAS1*	AW16	MEM_B_RAS_L			
MCAS1*	BA15	MEM_B_CAS_L			
MWE1*	BA16	MEM_B_WE_L			
MBA1_2	BB29	MEM_B_BA<2>			
MBA1_1	BB18	MEM_B_BA<1>			
MBA1_0	BB17	MEM_B_BA<0>			
MA1_14	BA29	MEM_B_A<14>			
MA1_13	BA14	MEM_B_A<13>			
MA1_12	AW28	MEM_B_A<12>			
MA1_11	BC28	MEM_B_A<11>			
MA1_10	BA17	MEM_B_A<10>			
MA1_9	BB28	MEM_B_A<9>			
MA1_8	AY28	MEM_B_A<8>			
MA1_7	BA28	MEM_B_A<7>			
MA1_6	AY27	MEM_B_A<6>			
MA1_5	BA27	MEM_B_A<5>			
MA1_4	BA26	MEM_B_A<4>			
MA1_3	BB26	MEM_B_A<3>			
MA1_2	BA25	MEM_B_A<2>			
MA1_1	BB25	MEM_B_A<1>			
MA1_0	BA18	MEM_B_A<0>			

MEMORY CONTROL 1A

MCLK1A_2_P	BA42	TP_MEM_B_CLK2P	8		
MCLK1A_2_N	BB42	TP_MEM_B_CLK2N	8		
MCLK1A_1_P	BB22	MEM_B_CLK_P<1>			
MCLK1A_1_N	BA22	MEM_B_CLK_N<1>			
MCLK1A_0_P	BA19	MEM_B_CLK_P<0>			
MCLK1A_0_N	AY19	MEM_B_CLK_N<0>			
MCS1A_1*	BB14	MEM_B_CS_L<1>			
MCS1A_0*	BB16	MEM_B_CS_L<0>			
MODT1A_1	BB13	MEM_B_ODT<1>			
MODT1A_0	AY15	MEM_B_ODT<0>			
MCKE1A_1	AY31	MEM_B_CKE<1>			
MCKE1A_0	BB30	MEM_B_CKE<0>			

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MEMORY CONTROL 0B

8 TP_MEM_A_CLK5P	AU33	MCLK0B_2_P	
8 TP_MEM_A_CLK5N	AU34	MCLK0B_2_N	
101 33 MEM_A_CLK_P<4>	BB24	MCLK0B_1_P	
101 33 MEM_A_CLK_N<4>	BC24	MCLK0B_1_N	
101 33 MEM_A_CLK_P<3>	BA21	MCLK0B_0_P	
101 33 MEM_A_CLK_N<3>	BB21	MCLK0B_0_N	
101 31 MEM_A_CS_L<2>	AU17	MCS0B_0*	
101 31 MEM_A_CS_L<3>	AR15	MCS0B_1*	
101 31 MEM_A_ODT<2>	AN17	MODT0B_0	
101 31 MEM_A_ODT<3>	AN15	MODT0B_1	
101 31 MEM_A_CKE<2>	AV23	MCKE0B_0	
101 31 MEM_A_CKE<3>	AN25	MCKE0B_1	

MEMORY CONTROL 1B

MCLK1B_2_P	BA41	TP_MEM_B_CLK5P	8
MCLK1B_2_N	BB41	TP_MEM_B_CLK5N	8
MCLK1B_1_P	AY23	MEM_B_CLK_P<4>	33 101
MCLK1B_1_N	BA23	MEM_B_CLK_N<4>	33 101
MCLK1B_0_P	BA20	MEM_B_CLK_P<3>	33 101
MCLK1B_0_N	AY20	MEM_B_CLK_N<3>	33 101
MCS1B_0*	BC16	MEM_B_CS_L<2>	32 101
MCS1B_1*	BA13	MEM_B_CS_L<3>	32 101
MODT1B_0	AY16	MEM_B_ODT<2>	32 101
MODT1B_1	BC13	MEM_B_ODT<3>	32 101
MCKE1B_0	BA30	MEM_B_CKE<2>	32 101
MCKE1B_1	BA31	MEM_B_CKE<3>	32 101

25 PP1V05_S0_MCP_PLL_CORE
87 mA (A01)

17 mA	T28	V1P1_PLL_V
12 mA	U28	V1P1_PLL_DP
19 mA	U27	V1P1_PLL_CORE
39 mA	T27	V1P1_PLL_XREF_XS

MRESET0* AY32 — MCP_MEM_RESET_L → ODT 33
TP or NC for DDR2.

30 25 16 6 =PP1V8R1V5_S0_MCP_MEM

R1610[1] 40.2 1% 1/16W MF-LF 402 [2]

R1611[1] 40.2 1% 1/16W MF-LF 402 [2]

101 MCP_MEM_COMP_GND	AM41	MEM_COMP_GND
101 MCP_MEM_COMP_VDD	AN41	MEM_COMP_1P8V

=PP1V8R1V5_S0_MCP_MEM 6 16 25 30
4771 mA (A01, DDR3)

GND

AA22 AP12 G30 P10 T10 T6 V10 V34 W5 AA39 AB22 AB7 AD22 AE20 AE24 AG24 AH35 AK7 AM28 AT25 AP30 AR36 AU10 F28 BC21 AY9 BC9 D34 F24 G32 H31 K7 M38 M5 M6 M7 M9 N39 N8 P33 P34 P37 P4 P40 P7 R36 R40 R43 R5 T18 T20 AK11 T24 T26

V1P8_MEM_VDDP

AM17 AN20 AN24 AT17 AP16 AN22 AP20 AP24 AV16 AR16 AR20 AM19 AR24 AW15 AB22 AP18 AU16 AN18 AU24 AT21 AY29 AV24 AM21 AU20 AU22 AW27 BC17 AV20 AY17 AY18 AM15 AU18 AY25 AM23 AY26 AW19 AW24 BC25 AL30 AM31 AM25 AM27 AM29 AN16 BC29

GND

T33 T34 T35 T37 T38 T7 T9 U18 U20 U22

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MCP MEMORY CNTRL & MISC

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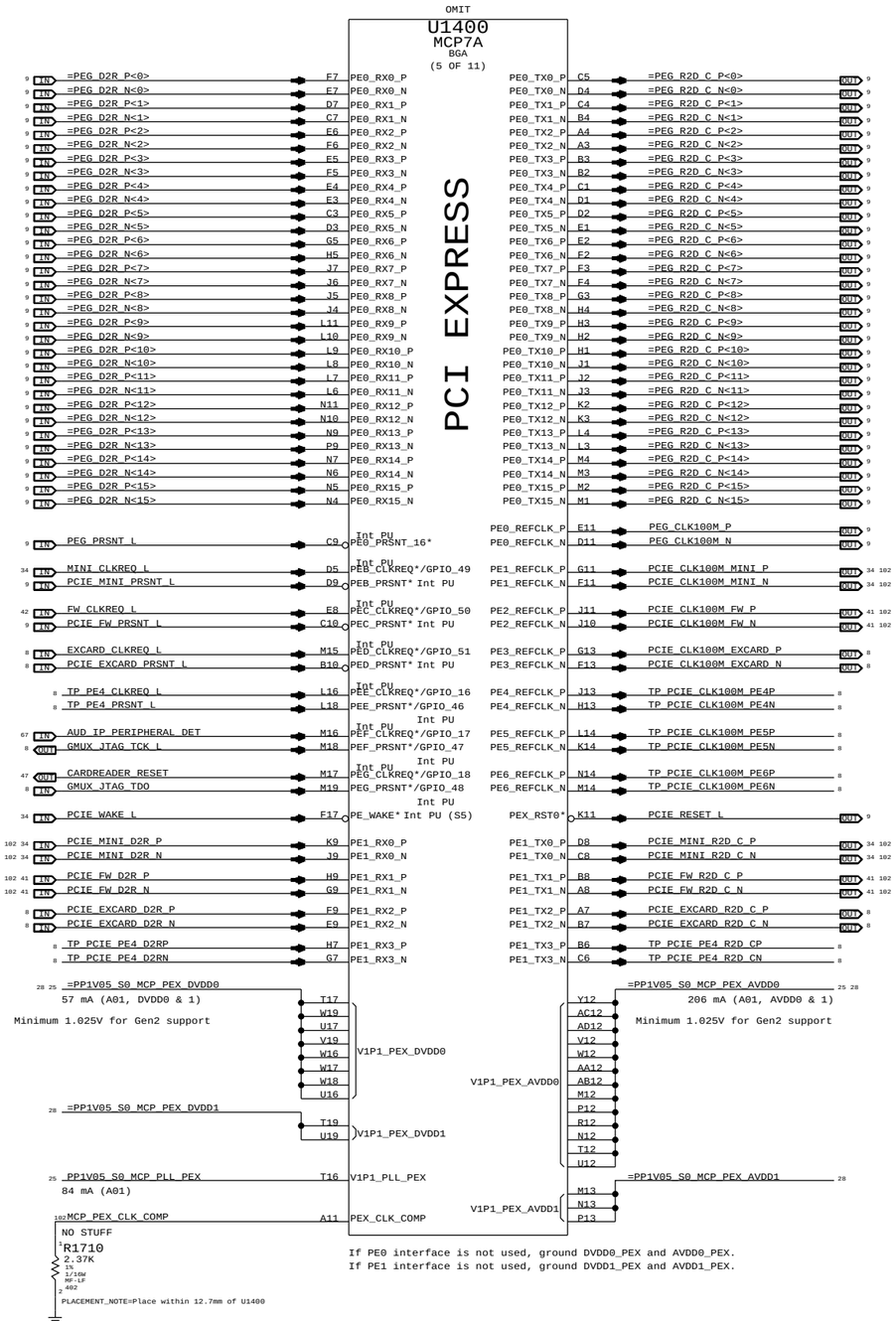

PAGE TITLE
MCP PCIe Interfaces

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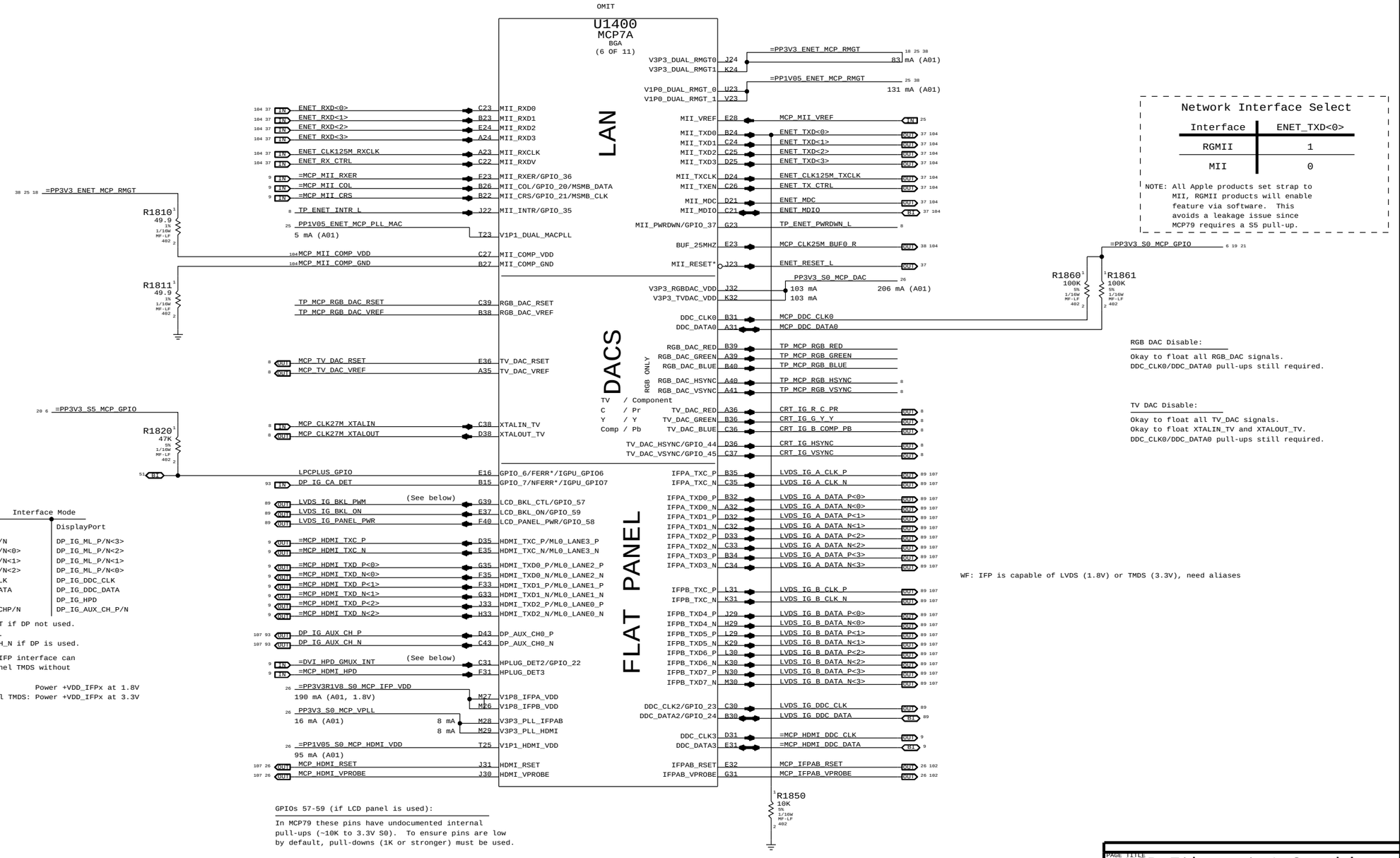

Network Interface Select	
Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:

Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

MCP Signal	Interface Mode: TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CHP/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.

NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

GPIOs 57-59 (if LCD panel is used):

In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:

Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.

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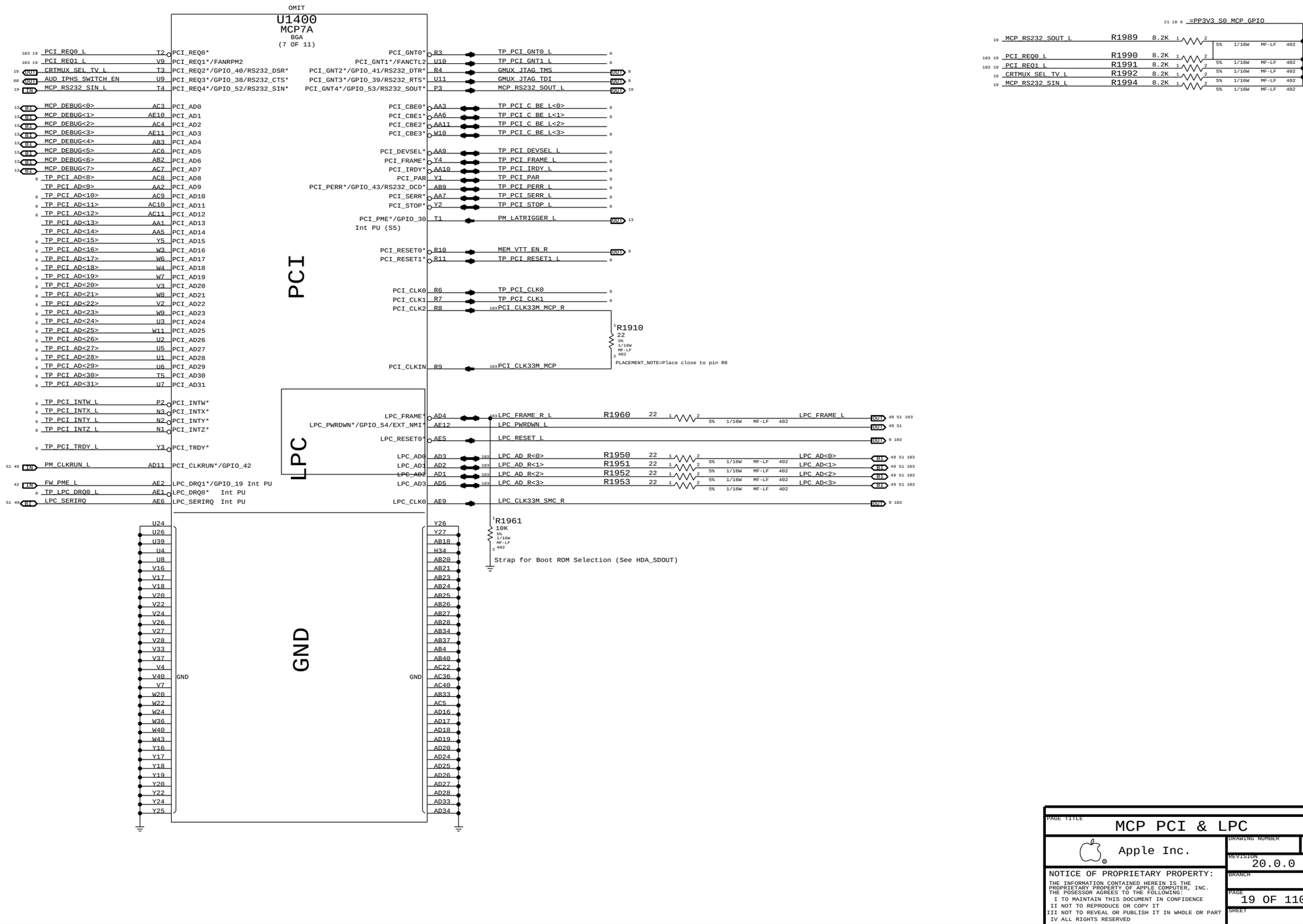

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SATA

102 45 OUT	SATA_HDD_R2D_C_P	AJ7	SATA_A0_TX_P
102 45 OUT	SATA_HDD_R2D_C_N	AJ6	SATA_A0_TX_N
102 45 IN	SATA_HDD_D2R_N	AJ5	SATA_A0_RX_N
102 45 IN	SATA_HDD_D2R_P	AJ4	SATA_A0_RX_P
102 45 OUT	SATA_ODD_R2D_C_P	AJ11	SATA_A1_TX_P
102 45 OUT	SATA_ODD_R2D_C_N	AJ10	SATA_A1_TX_N
102 45 IN	SATA_ODD_D2R_N	AJ9	SATA_A1_RX_N
102 45 IN	SATA_ODD_D2R_P	AK9	SATA_A1_RX_P
	TP_SATA_C_R2D_CP	AK2	SATA_B0_TX_P
	TP_SATA_C_R2D_CN	AJ3	SATA_B0_TX_N
	TP_SATA_C_D2RN	AJ2	SATA_B0_RX_N
	TP_SATA_C_D2RP	AJ1	SATA_B0_RX_P
	TP_SATA_D_R2D_CP	AM4	SATA_B1_TX_P
	TP_SATA_D_R2D_CN	AL3	SATA_B1_TX_N
	TP_SATA_D_D2RN	AL4	SATA_B1_RX_N
	TP_SATA_D_D2RP	AK3	SATA_B1_RX_P
	TP_SATA_E_R2D_CP	AN1	SATA_C0_TX_P
	TP_SATA_E_R2D_CN	AM1	SATA_C0_TX_N
	TP_SATA_E_D2RN	AM2	SATA_C0_RX_N
	TP_SATA_E_D2RP	AM3	SATA_C0_RX_P
	TP_SATA_F_R2D_CP	AP3	SATA_C1_TX_P
	TP_SATA_F_R2D_CN	AP2	SATA_C1_TX_N
	TP_SATA_F_D2RN	AN3	SATA_C1_RX_N
	TP_SATA_F_D2RP	AN2	SATA_C1_RX_P
45	TP_MCP_SATALED_L	E12	SATA_LED*

25	PP1V05_S0_MCP_PLL_SATA 84 mA (A01)	AE16	V1P1_PLL_SATA
28 6	=PP1V05_S0_MCP_SATA_DVDD0 43 mA (A01, DVDD0 & 1) Minimum 1.025V for Gen2 support	AF19 AG16 AG17 AG19	V1P1_SATA_DVDD0
28	=PP1V05_S0_MCP_SATA_DVDD1	AH17 AH19	V1P1_SATA_DVDD1
28	=PP1V05_S0_MCP_SATA_AVDD0 127 mA (A01, AVDD0 & 1) Minimum 1.025V for Gen2 support	AJ12 AN11 AK12 AK13 AL12 AM11 AM12 AN12 AL13	V1P1_SATA_AVDD0
28	=PP1V05_S0_MCP_SATA_AVDD1	AN14 AL14 AM13 AM14	V1P1_SATA_AVDD1
102	MCP_SATA_TERMP	AE3	SATA_TERMP

R2010 2.49K 1% 1/16W MF-LF 402

If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.

USB

	External A		
USB0_P	C29	USB_EXTA_P	83 46 103
USB0_N	D29	USB_EXTA_N	83 46 103
	AirPort (PCIe Mini-Card)		
USB1_P	C28	USB_MINI_P	83 8
USB1_N	D28	USB_MINI_N	83 8
	External D		
USB2_P	A28	USB_EXTD_P	83 46 103
USB2_N	B28	USB_EXTD_N	83 46 103
	Camera		
USB3_P	F29	USB_CAMERA_P	83 47 103
USB3_N	G29	USB_CAMERA_N	83 47 103
	IR		
USB4_P	K27	USB_IR_P	83 47 103
USB4_N	L27	USB_IR_N	83 47 103
	Geyser Trackpad/Keyboard		
USB5_P	J26	USB_TPAD_P	83 8
USB5_N	J27	USB_TPAD_N	83 8
	Bluetooth		
USB6_P	F27	USB_BT_P	83 47 103
USB6_N	G27	USB_BT_N	83 47 103
	External B		
USB7_P	D27	USB_EXTB_P	83 46 103
USB7_N	E27	USB_EXTB_N	83 46 103
	ExpressCard		
USB8_P	K25	USB_EXCARD_P	83 8
USB8_N	L25	USB_EXCARD_N	83 8
	External C		
USB9_P	H25	USB_EXTC_P	83 46 103
USB9_N	J25	USB_EXTC_N	83 46 103
USB10_P	F25	TP_USB_10P	8
USB10_N	G25	TP_USB_10N	8
USB11_P	K23	USB_SDCARD_P	83 47 103
USB11_N	L23	USB_SDCARD_N	83 47 103

USB_OC0*/GPIO_25	L21	USB_EXTA_OC_L	46
USB_OC1*/GPIO_26	K21	USB_EXTB_OC_L	46
USB_OC2*/GPIO_27/MGPIO	J21	USB_EXTC_OC_L	8 46
USB_OC3*/GPIO_28/MGPIO	H21	EXCARD_OC_L	

=PP3V3_S5_MCP_GPIO 6 18

R2051 8.2K 5% 1/16W MF-LF 402
R2053 8.2K 5% 1/16W MF-LF 402
R2050 8.2K 5% 1/16W MF-LF 402
R2052 8.2K 5% 1/16W MF-LF 402

V3P3_PLL_USB	L28	PP3V3_S0_MCP_PLL_USB 19 mA (A01)	25
USB_RBIAS_GND	A27	103 MCP_USB_RBIAS_GND	

R2060 806 1% 1/16W MF-LF 402

GND	AD35	AD37	AD38
	AE22	AE24	AE39
	AE4	AD6	AE16
	AF17	AF18	AE20
	AE22	AE26	AE27
	AE28	AE33	AE34
	AE37	AF40	AG18
	AG20	AG22	AG26
	AG36	AG40	AH18
	AH20	AH22	AH24

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

PAGE TITLE: MCP SATA & USB

Apple Inc.

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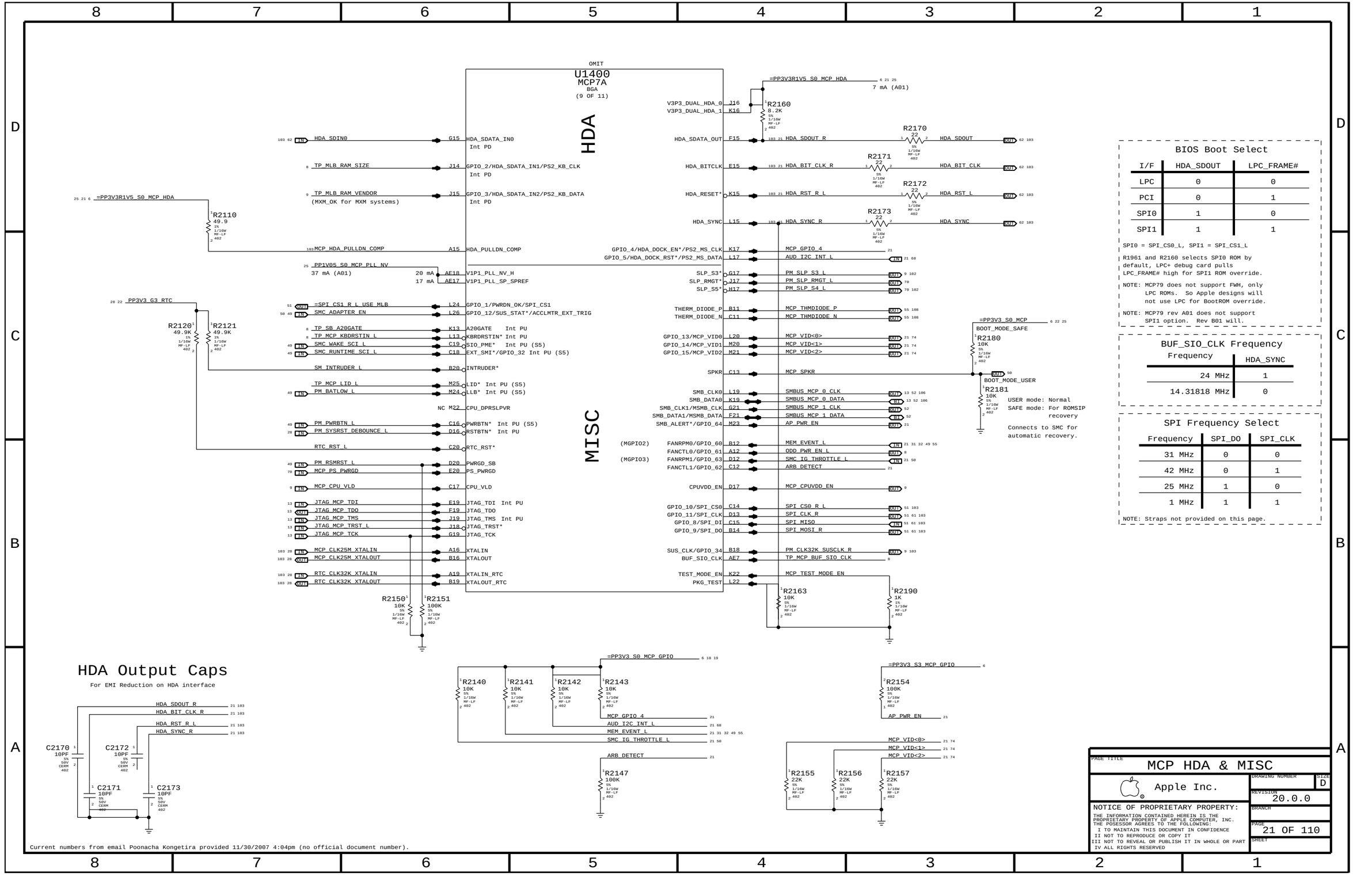

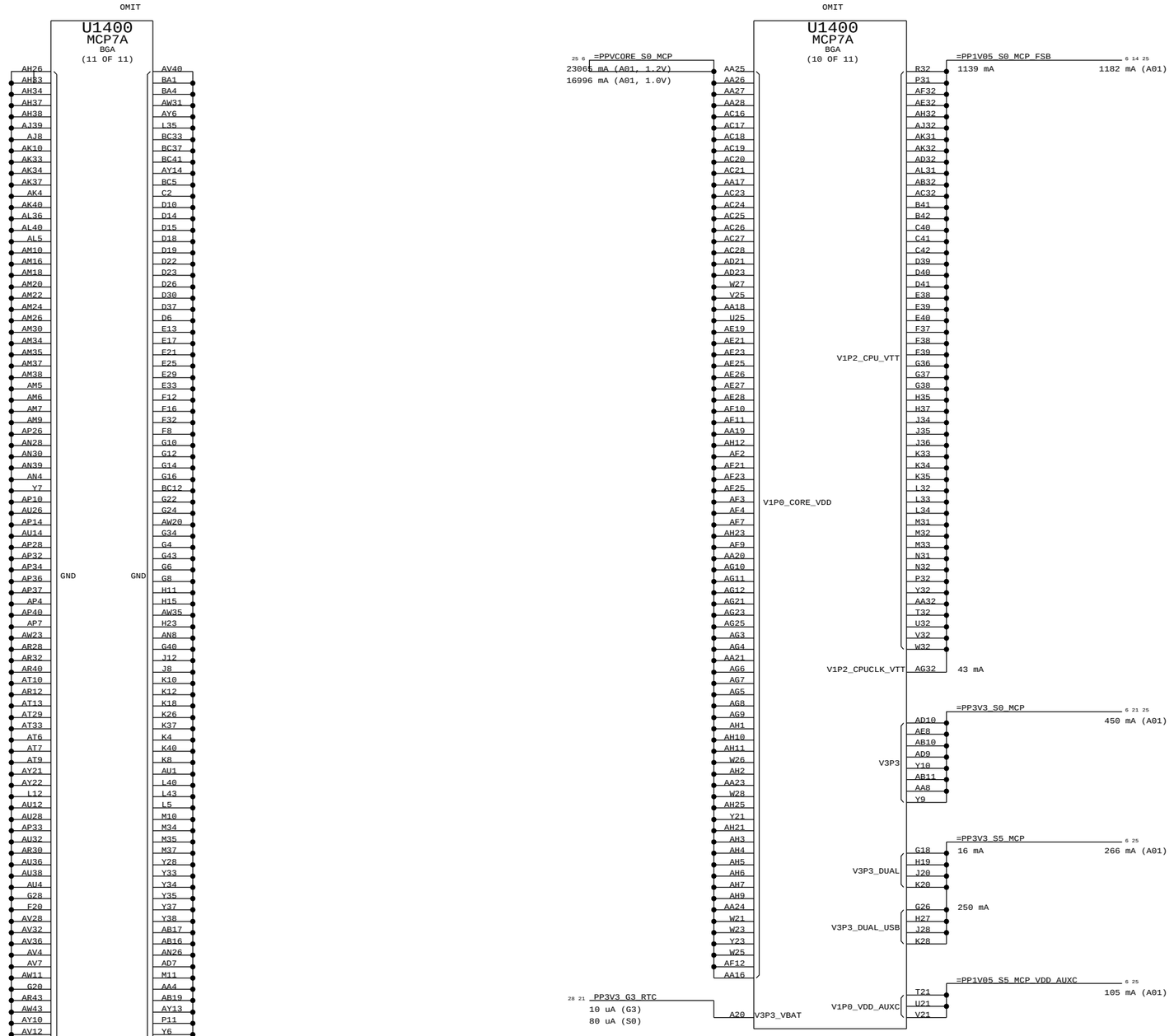

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

PAGE TITLE
MCP Power & Ground

Apple Inc.

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REVISION 20.0.0

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SHEET

MCP Core Power

=PPVCORE_S0_MCP

23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)

(No IG vs. EG data)

NV: 1x 10uF 0805, 2x 4.7uF 0402, 3x 1uF 0402, 9x 0.1uF 0402 (23.3 uF)
APPLE: 4X 4.7UF 0402, 4X 1UF 0402, 6X 0.1UF 0402 (23.4 uF)

C2500 4.7UF 20% 4V X5R 402
C2501 4.7UF 20% 4V X5R 402
C2502 4.7UF 20% 4V X5R 402
C2503 4.7UF 20% 4V X5R 402
C2504 1UF 10% 10V X5R 402-1
C2505 1UF 10% 10V X5R 402-1
C2506 1UF 10% 10V X5R 402-1
C2507 1UF 10% 10V X5R 402-1
C2508 1UF 10% 10V X5R 402-1
C2509 1UF 10% 10V X5R 402-1
C2510 1UF 10% 10V X5R 402-1
C2511 1UF 10% 10V X5R 402-1
C2512 1UF 10% 10V X5R 402-1
C2513 1UF 10% 10V X5R 402-1

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0004	2	RES,0,5%,0402	C2574,C2518	IG

MCP PCIE (DVDD) Power
DIFFERENT THAN ON T18

=PP1V05_S0_MCP_PEX_DVDD

57 mA (A01)

PEX_DVDD RAIL SPLIT BASED ON T8 VS. E6. 8 OUT OF 18 BALLS FOR DVDD0 SO 80% OF CAPACITANCE ON DVDD0

NV: 1X 4.7UF 0402, 2X 1UF 0402, 2X 0.1UF 0402 (6.9UF)
K50: 2X 2.2UF 0402, 2X 1UF 0402, (6.4 UF)

=PP1V05_S0_MCP_PEX_DVDD0

C2516 1UF 10% 10V X5R 402-1
C2515 2.2UF 20% 6.3V CERM 402-LF
C2517 1UF 10% 10V X5R 402-1
C2518 2.2UF 20% 6.3V CERM 402-LF

MCP SATA (DVDD) Power

=PP1V05_S0_MCP_SATA_DVDD

43 mA (A01)

C2520 4.7UF 20% 4V X5R 402
C2521 0.1UF 20% 10V CERM 402

MCP 1.05V AUX Power

=PP1V05_S5_MCP_VDD_AUXC

105 mA (A01)

C2525 0.1UF 20% 10V CERM 402
C2526 0.1UF 20% 10V CERM 402

MCP 1.05V RMGT Power

=PP1V05_ENET_MCP_RMGT

131 mA (A01)

C2528 4.7UF 20% 4V X5R 402
C2529 0.1UF 20% 10V CERM 402

MCP FSB (VTT) Power

=PP1V05_S0_MCP_FSB

1182 mA (A01)

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 7x 2.2uF 0402 (15.4 uF)

C2530 2.2UF 20% 6.3V CERM 402-LF
C2531 2.2UF 20% 6.3V CERM 402-LF
C2532 2.2UF 20% 6.3V CERM 402-LF
C2533 2.2UF 20% 6.3V CERM 402-LF
C2534 2.2UF 20% 6.3V CERM 402-LF
C2535 2.2UF 20% 6.3V CERM 402-LF
C2536 2.2UF 20% 6.3V CERM 402-LF

MCP Memory Power

=PP1V8R1V5_S0_MCP_MEM

4771 mA (A01, DDR3)

C2540 4.7UF 20% 4V X5R 402
C2541 0.1UF 20% 10V CERM 402
C2542 0.1UF 20% 10V CERM 402
C2543 0.1UF 20% 10V CERM 402
C2544 0.1UF 20% 10V CERM 402
C2545 0.1UF 20% 10V CERM 402
C2546 0.1UF 20% 10V CERM 402
C2547 0.1UF 20% 10V CERM 402
C2548 0.1UF 20% 10V CERM 402
C2549 0.1UF 20% 10V CERM 402

MCP 3.3V Power

=PP3V3_S0_MCP

450 mA (A01)

NV: 1x 4.7uF 0603, 4x 0.1uF 0402 (5.1 uF)
Apple: 4x 2.2uF 0402 (8.8 uF)

C2550 2.2UF 20% 6.3V CERM 402-LF
C2551 2.2UF 20% 6.3V CERM 402-LF
C2552 2.2UF 20% 6.3V CERM 402-LF
C2553 2.2UF 20% 6.3V CERM 402-LF

=PP3V3_S0_MCP_PLL_UF

19 mA (A01)

L2555 30-OHM-1.7A 0402

PP3V3_S0_MCP_PLL_USB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
19 mA (A01)

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

C2555 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V AUX/USB Power

=PP3V3_S5_MCP

266 mA (A01)

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

C2560 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V Ethernet Power

=PP3V3_ENET_MCP_RMGT

83 mA (A01)

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

C2564 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V/1.5V HDA Power

=PP3V3R1V5_S0_MCP_HDA

7 mA (A01)

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

C2562 2.2UF 20% 6.3V CERM 402-LF

MCP79 Ethernet VRef

=PP3V3_ENET_MCP_RMGT

R2591 1.47K 1% 1/16W MF-LF 402
R2590 1.47K 1% 1/16W MF-LF 402

MCP_MII_VREF (OUT)

C2591 0.1UF 20% 10V CERM 402

=PP1V05_ENET_MCP_PLL_MAC

5 mA (A01)

L2595 30-OHM-1.7A 0402

PP1V05_ENET_MCP_PLL_MAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
5 mA (A01)

C2595 4.7UF 20% 4V X5R 402
C2596 4.7UF 20% 4V X5R 402

=PP1V05_S0_MCP_AVDD_UF

333 mA (A01)

L2570 30-OHM-5A 0603

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 1uF 0402, 2x 0.1uF 0402 (16.9 uF)
Apple: 5x 2.2uF 0402 (11 uF)

PP1V05_S0_MCP_PEX_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
206 mA (A01)

C2570 2.2UF 20% 6.3V CERM 402-LF
C2571 2.2UF 20% 6.3V CERM 402-LF
C2572 2.2UF 20% 6.3V CERM 402-LF
C2573 2.2UF 20% 6.3V CERM 402-LF
C2574 2.2UF 20% 6.3V CERM 402-LF

=PP1V05_S0_MCP_PEX_AVDD0

PEX_AVDD RAIL SPLIT BASED ON IG VS. E6. 12 OUT OF 15 BALLS FOR AVDD0 SO 80% OF CAPACITANCE ON AVDD0

L2575 30-OHM-5A 0603

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)

PP1V05_S0_MCP_SATA_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
127 mA (A01)

C2575 2.2UF 20% 6.3V CERM 402-LF
C2576 2.2UF 20% 6.3V CERM 402-LF

=PP1V05_S0_MCP_PLL_UF

562 mA (A01)

L2580 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_FSB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
270 mA (A01)

C2580 4.7UF 20% 4V X5R 402
C2581 4.7UF 20% 4V X5R 402

L2582 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_PEX
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
84 mA (A01)

C2582 4.7UF 20% 4V X5R 402
C2583 4.7UF 20% 4V X5R 402

L2584 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_SATA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
84 mA (A01)

C2584 4.7UF 20% 4V X5R 402
C2585 4.7UF 20% 4V X5R 402

L2586 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_CORE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
87 mA (A01)

C2586 4.7UF 20% 4V X5R 402
C2597 4.7UF 20% 4V X5R 402
C2587 4.7UF 20% 4V X5R 402

L2588 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_NV
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
37 mA (A01)

C2588 4.7UF 20% 4V X5R 402
C2589 4.7UF 20% 4V X5R 402
C2590 2.2UF 20% 6.3V X5R 402

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PAGE TITLE
MCP Standard Decoupling

Apple Inc.

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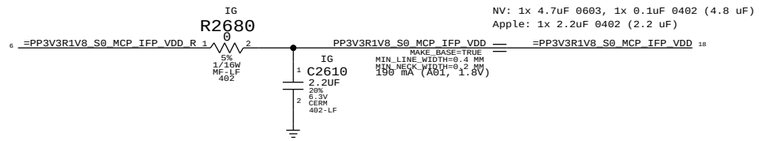
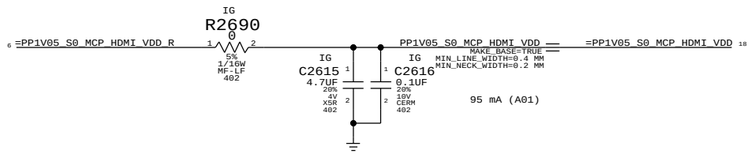
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

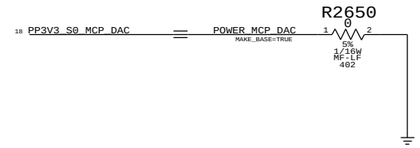


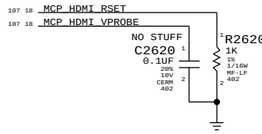
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

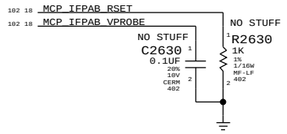
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES,0,5%,402	C2610		MXM



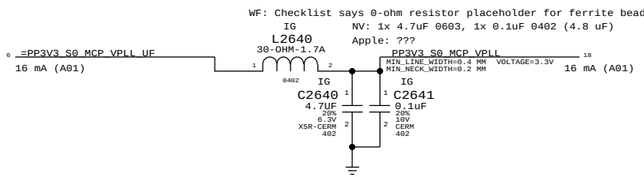
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES,0,5%,402	C2616		MXM







WF: Checklist says 0-ohm resistor placeholder for ferrite bead.



NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: ???

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES,0,5%,402	C2641		MXM

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PAGE TITLE: MCP Graphics Support

Apple Inc.

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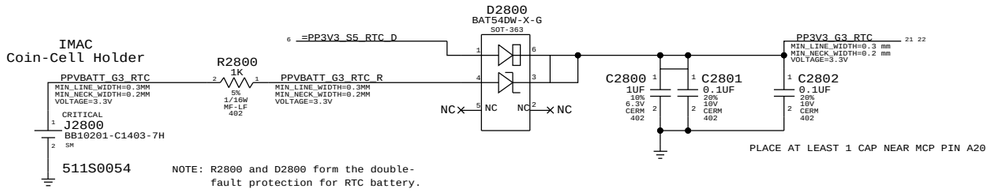
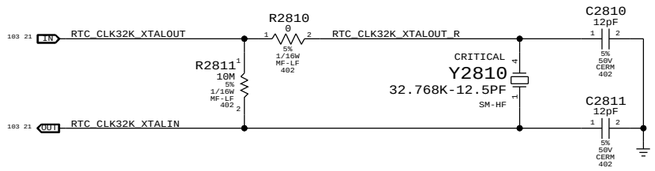
RTC Power Sources

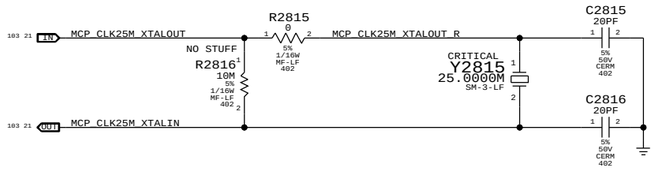


NOTE: R2800 and D2800 form the double-fault protection for RTC battery.

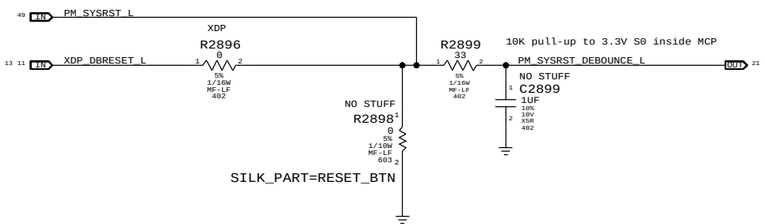
RTC Crystal



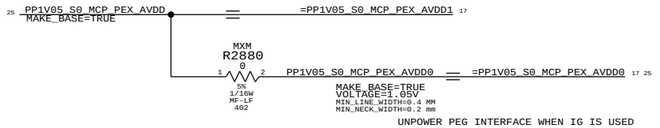
MCP 25MHz Crystal



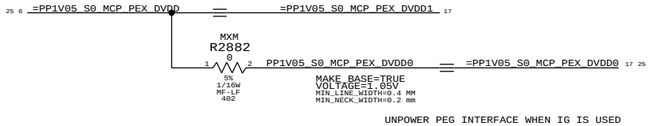
Reset Button



PEG POWER ALIAS/OPTION TO GND UNUSED POWER PIN

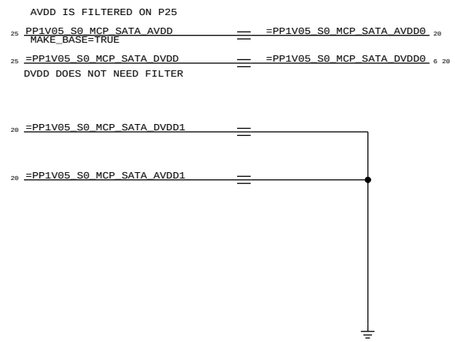


UNPOWER PEG INTERFACE WHEN IG IS USED



UNPOWER PEG INTERFACE WHEN IG IS USED

SATA ALIAS/GROUNDING UNUSED DVDD1 AND AVDD1



PAGE TITLE: SB Misc

Apple Inc.

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Page Notes

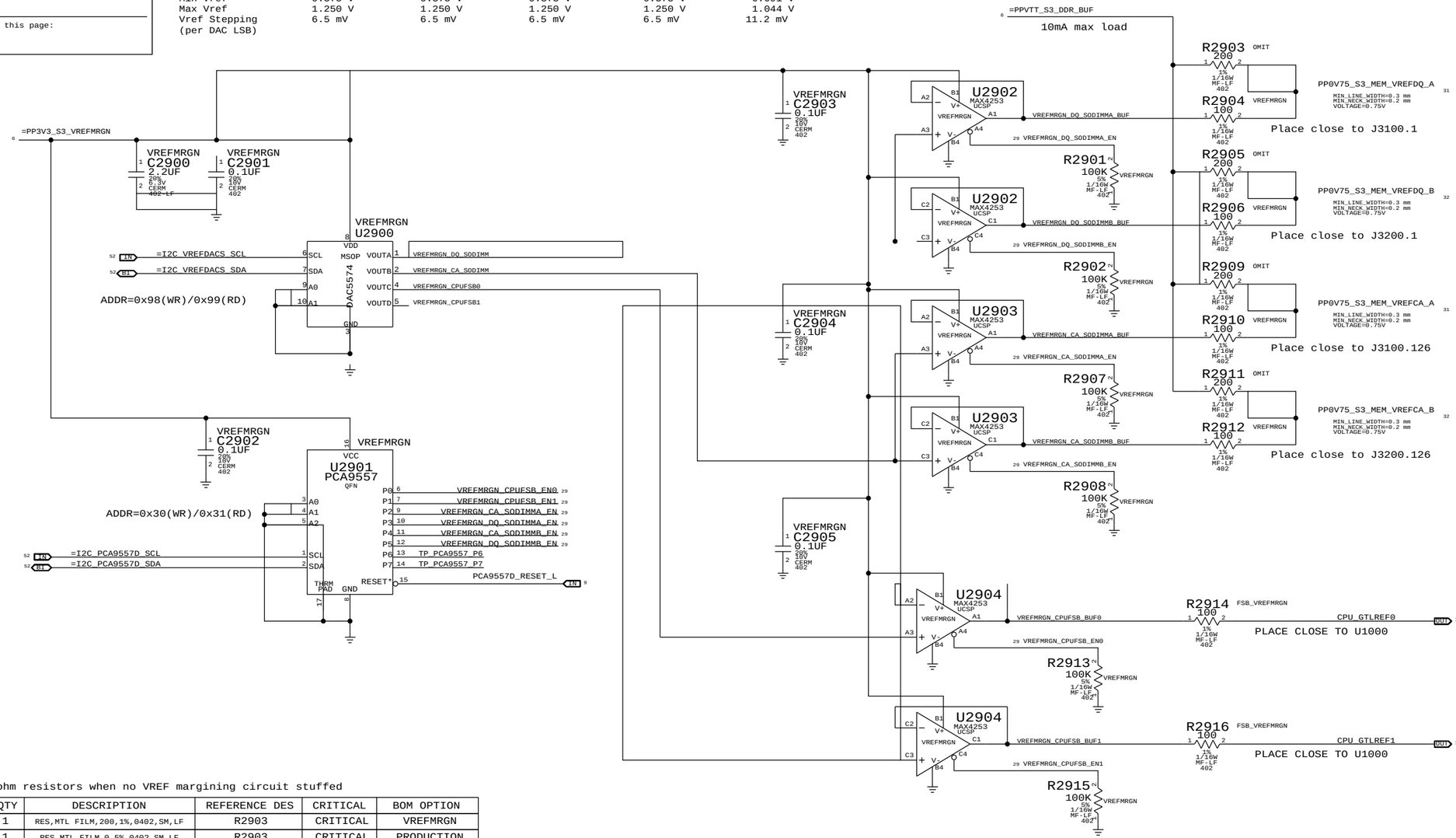
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
PRODUCTION

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF
DAC channel	A	B	A	B	C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2903	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	PRODUCTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2905	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	PRODUCTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2909	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	PRODUCTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2911	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	PRODUCTION

PAGE TITLE: FSB/DDR3 Vref Margining

Apple Inc.

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REVISION: 20.0.0

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DIMM A (FURTHER FROM MCP)

CAPS TO COUPLE MCP 1V5_S0_MEM

DIMM B (CLOSER TO MCP)

30 25 16 6 =PP1V8R1V5_S0_MCP_MEM

C3016 0.1UF 20% 10V CERM 402
C3017 0.1UF 20% 10V CERM 402
C3018 0.1UF 20% 10V CERM 402
C3019 0.1UF 20% 10V CERM 402
C3010 0.1UF 20% 10V CERM 402

30 25 16 6 =PP1V8R1V5_S0_MCP_MEM

C3025 0.1UF 20% 10V CERM 402
C3026 0.1UF 20% 10V CERM 402
C3027 0.1UF 20% 10V CERM 402
C3028 0.1UF 20% 10V CERM 402
C3029 0.1UF 20% 10V CERM 402
C3020 0.1UF 20% 10V CERM 402
C3021 0.1UF 20% 10V CERM 402
C3022 0.1UF 20% 10V CERM 402
C3023 0.1UF 20% 10V CERM 402
C3014 0.1UF 20% 10V CERM 402
C3030 0.1UF 20% 10V CERM 402
C3031 0.1UF 20% 10V CERM 402
C3032 0.1UF 20% 10V CERM 402
C3033 0.1UF 20% 10V CERM 402
C3034 0.1UF 20% 10V CERM 402
C3035 0.1UF 20% 10V CERM 402

EXTRA DECOUPLING CAPS FOR MCP MEM RAIL

30 25 16 6 =PP1V8R1V5_S0_MCP_MEM
4771 mA (A01, DDR3)

C3041 0.1UF 20% 10V CERM 402
C3042 0.1UF 20% 10V CERM 402
C3044 0.1UF 20% 10V CERM 402
C3046 0.1UF 20% 10V CERM 402
C3040 1UF 10% 6.3V CERM 402
C3043 1UF 10% 6.3V CERM 402
C3045 1UF 10% 6.3V CERM 402
C3047 1UF 10% 6.3V CERM 402
C3048 1UF 10% 6.3V CERM 402
C3049 1UF 10% 6.3V CERM 402
C3090 1UF 10% 6.3V CERM 402
C3091 1UF 10% 6.3V CERM 402
C3092 1UF 10% 6.3V CERM 402
C3093 1UF 10% 6.3V CERM 402
C3094 1UF 10% 6.3V CERM 402
C3095 1UF 10% 6.3V CERM 402
C3096 1UF 10% 6.3V CERM 402
C3097 1UF 10% 6.3V CERM 402
C3098 1UF 10% 6.3V CERM 402
C3099 1UF 10% 6.3V CERM 402
C3000 1UF 10% 6.3V CERM 402
C3001 1UF 10% 6.3V CERM 402
C3002 1UF 10% 6.3V CERM 402

16 6 =PP1V8R1V5_S0_MCP_MEM
30 25 4771 mA (A01, DDR3)

C30A0 1UF 10% 6.3V CERM 402
C30A1 1UF 10% 6.3V CERM 402
C30A2 1UF 10% 6.3V CERM 402
C30A3 1UF 10% 6.3V CERM 402
C30A4 1UF 10% 6.3V CERM 402
C30A5 1UF 10% 6.3V CERM 402

CAPS TO COUPLE PP5V_S3 UNDER DIMM CONNECTORS

75 30 6 =PP5V_S3_DDRREG

C30B0 1UF 10% 6.3V CERM 402
C30B1 1UF 10% 6.3V CERM 402
C30B2 1UF 10% 6.3V CERM 402
C30B3 1UF 10% 6.3V CERM 402
C30B4 1UF 10% 6.3V CERM 402
C30B5 1UF 10% 6.3V CERM 402
C30B6 1UF 10% 6.3V CERM 402
C30B7 1UF 10% 6.3V CERM 402
C30B8 1UF 10% 6.3V CERM 402
C30B9 1UF 10% 6.3V CERM 402
C30BA 1UF 10% 6.3V CERM 402
C30BB 1UF 10% 6.3V CERM 402
C30BC 1UF 10% 6.3V CERM 402
C30BD 1UF 10% 6.3V CERM 402
C30BE 1UF 10% 6.3V CERM 402
C30BF 1UF 10% 6.3V CERM 402
C30D0 1UF 10% 6.3V CERM 402
C30D1 1UF 10% 6.3V CERM 402
C30D2 1UF 10% 6.3V CERM 402
C30D3 1UF 10% 6.3V CERM 402

75 30 6 =PP5V_S3_DDRREG

C30C0 1UF 10% 6.3V CERM 402
C30C1 1UF 10% 6.3V CERM 402
C30C2 1UF 10% 6.3V CERM 402
C30C3 1UF 10% 6.3V CERM 402
C30C4 1UF 10% 6.3V CERM 402
C30C5 1UF 10% 6.3V CERM 402
C30C6 1UF 10% 6.3V CERM 402
C30C7 1UF 10% 6.3V CERM 402
C30C8 1UF 10% 6.3V CERM 402
C30C9 1UF 10% 6.3V CERM 402
C30CA 1UF 10% 6.3V CERM 402
C30CB 1UF 10% 6.3V CERM 402
C30CC 1UF 10% 6.3V CERM 402
C30CD 1UF 10% 6.3V CERM 402
C30CE 1UF 10% 6.3V CERM 402
C30CF 1UF 10% 6.3V CERM 402
C30E0 1UF 10% 6.3V CERM 402
C30E1 1UF 10% 6.3V CERM 402
C30E2 1UF 10% 6.3V CERM 402
C30E3 1UF 10% 6.3V CERM 402

DECOUPLING CAPS FOR DIMM ON CHANNEL A - AT CONNECTOR

108 31 6 =PP1V5_S3_MEM_A

C3050 10UF 20% 6.3V X5R 603
C3051 10UF 20% 6.3V X5R 603
C3052 1UF 10% 6.3V CERM 402
C3053 1UF 10% 6.3V CERM 402
C3054 1UF 10% 6.3V CERM 402
C3055 1UF 10% 6.3V CERM 402
C3056 1UF 10% 6.3V CERM 402
C3057 1UF 10% 6.3V CERM 402
C3058 1UF 10% 6.3V CERM 402
C3059 1UF 10% 6.3V CERM 402
C3060 1UF 10% 6.3V CERM 402
C3061 1UF 10% 6.3V CERM 402
C3062 1UF 10% 6.3V CERM 402
C3063 1UF 10% 6.3V CERM 402
C3064 1UF 10% 6.3V CERM 402
C3065 1UF 10% 6.3V CERM 402

DECOUPLING CAPS FOR DIMM ON CHANNEL B - AT CONNECTOR

108 32 6 =PP1V5_S3_MEM_B

C3070 10UF 20% 6.3V X5R 603
C3071 10UF 20% 6.3V X5R 603
C3072 1UF 10% 6.3V CERM 402
C3073 1UF 10% 6.3V CERM 402
C3074 1UF 10% 6.3V CERM 402
C3075 1UF 10% 6.3V CERM 402
C3076 1UF 10% 6.3V CERM 402
C3077 1UF 10% 6.3V CERM 402
C3078 1UF 10% 6.3V CERM 402
C3079 1UF 10% 6.3V CERM 402
C3080 1UF 10% 6.3V CERM 402
C3081 1UF 10% 6.3V CERM 402
C3082 1UF 10% 6.3V CERM 402
C3083 1UF 10% 6.3V CERM 402
C3084 1UF 10% 6.3V CERM 402
C3085 1UF 10% 6.3V CERM 402

PAGE TITLE: MEMORY CAPS

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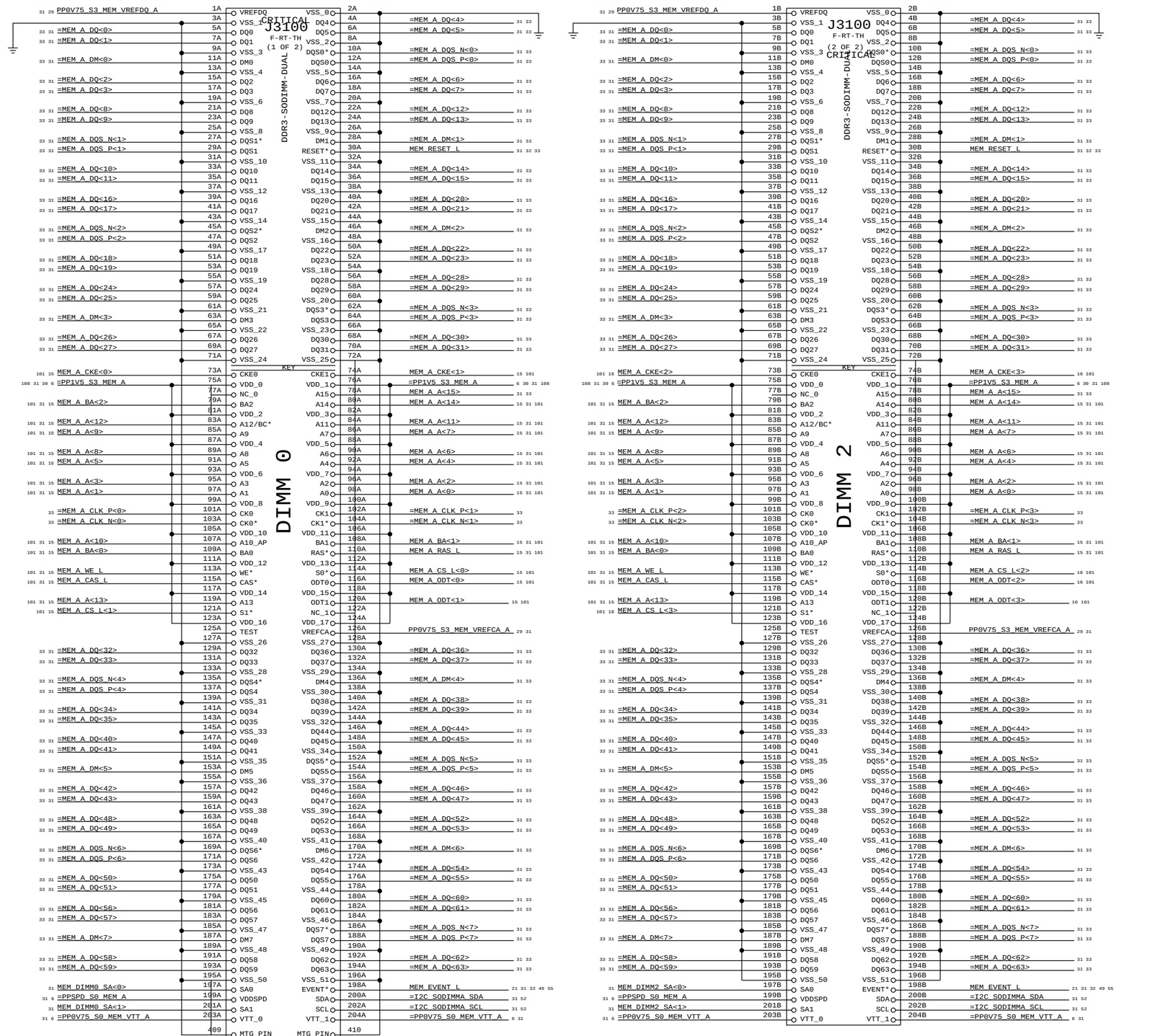

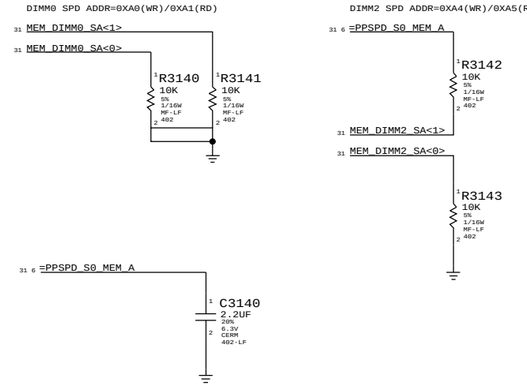

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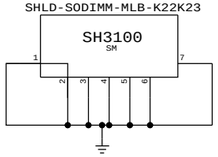
SHLD-SODIMM-MLB-K22K23



Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA
- ALL DQ, DQS, DM SIGNALS; TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page:
(NONE)

PAGE TITLE: DDR3 SO-DIMMs 0 & 2

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REVISION: 20.0.0

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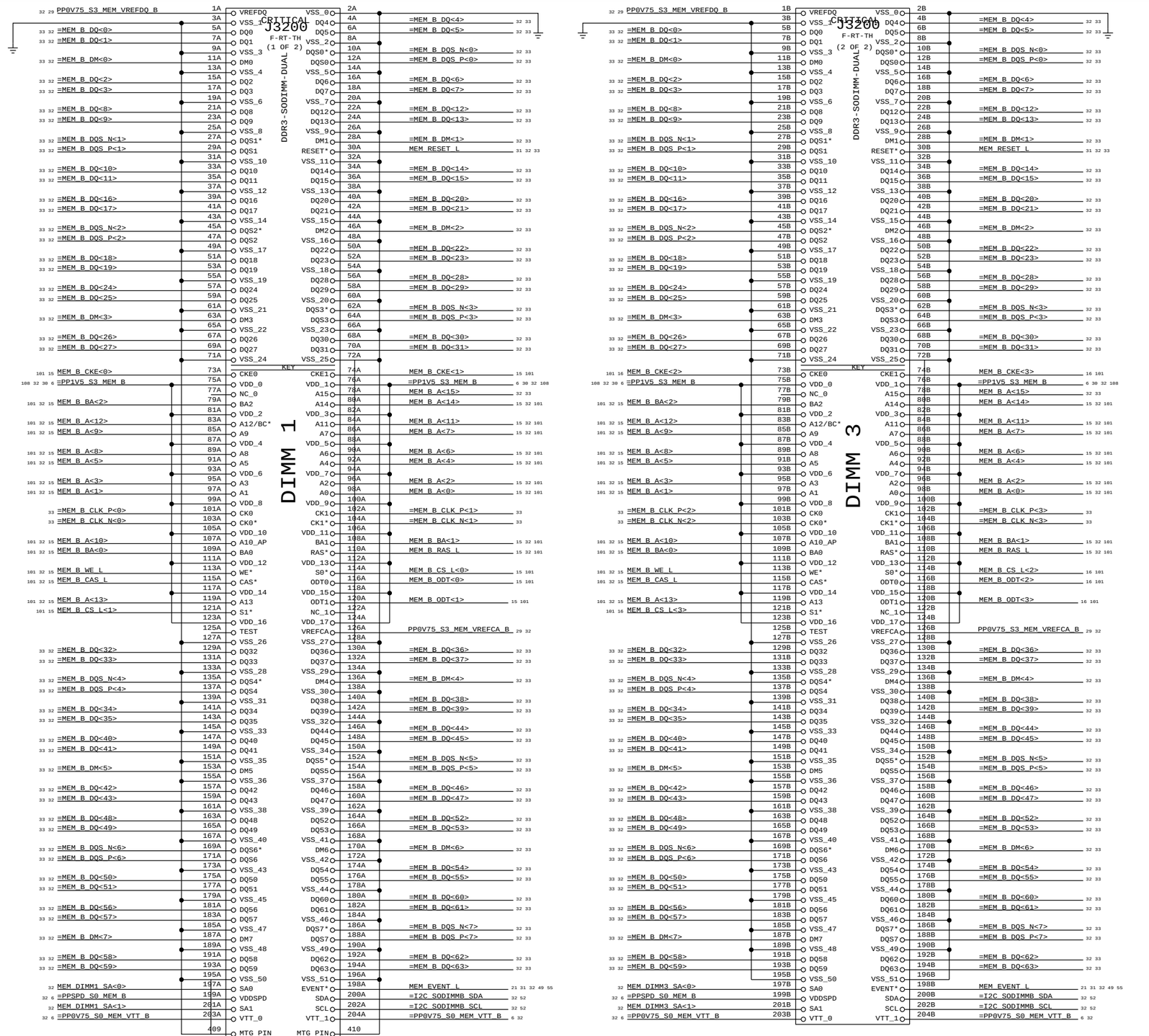

Page Notes

Power aliases required by this page:

- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA
- ALL DQ, DQS, DM SIGNALS; TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page:

(NONE)

PAGE TITLE: DDR3 SO-DIMM CONNECTOR B

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SIZE: D

REVISION: 20.0.0

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MCP CHANNEL A DQS 0 -> DIMM A DQS 0

MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=MEM_A_DQS_N<0>	31
MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=MEM_A_DQS_P<0>	31
MEM_A_DM<0>	MAKE_BASE=TRUE	=MEM_A_DM<0>	31
MEM_A_DQ<7>	MAKE_BASE=TRUE	=MEM_A_DQ<7>	31
MEM_A_DQ<6>	MAKE_BASE=TRUE	=MEM_A_DQ<6>	31
MEM_A_DQ<5>	MAKE_BASE=TRUE	=MEM_A_DQ<4>	31
MEM_A_DQ<4>	MAKE_BASE=TRUE	=MEM_A_DQ<5>	31
MEM_A_DQ<3>	MAKE_BASE=TRUE	=MEM_A_DQ<3>	31
MEM_A_DQ<2>	MAKE_BASE=TRUE	=MEM_A_DQ<2>	31
MEM_A_DQ<1>	MAKE_BASE=TRUE	=MEM_A_DQ<0>	31
MEM_A_DQ<0>	MAKE_BASE=TRUE	=MEM_A_DQ<1>	31

MCP CHANNEL A DQS 1 -> DIMM A DQS 1

MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=MEM_A_DQS_N<1>	31
MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=MEM_A_DQS_P<1>	31
MEM_A_DM<1>	MAKE_BASE=TRUE	=MEM_A_DM<1>	31
MEM_A_DQ<15>	MAKE_BASE=TRUE	=MEM_A_DQ<15>	31
MEM_A_DQ<14>	MAKE_BASE=TRUE	=MEM_A_DQ<14>	31
MEM_A_DQ<13>	MAKE_BASE=TRUE	=MEM_A_DQ<13>	31
MEM_A_DQ<12>	MAKE_BASE=TRUE	=MEM_A_DQ<12>	31
MEM_A_DQ<11>	MAKE_BASE=TRUE	=MEM_A_DQ<11>	31
MEM_A_DQ<10>	MAKE_BASE=TRUE	=MEM_A_DQ<10>	31
MEM_A_DQ<9>	MAKE_BASE=TRUE	=MEM_A_DQ<8>	31
MEM_A_DQ<8>	MAKE_BASE=TRUE	=MEM_A_DQ<9>	31

MCP CHANNEL A DQS 2 -> DIMM A DQS 2

MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=MEM_A_DQS_N<2>	31
MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=MEM_A_DQS_P<2>	31
MEM_A_DM<2>	MAKE_BASE=TRUE	=MEM_A_DM<2>	31
MEM_A_DQ<23>	MAKE_BASE=TRUE	=MEM_A_DQ<23>	31
MEM_A_DQ<22>	MAKE_BASE=TRUE	=MEM_A_DQ<22>	31
MEM_A_DQ<21>	MAKE_BASE=TRUE	=MEM_A_DQ<16>	31
MEM_A_DQ<20>	MAKE_BASE=TRUE	=MEM_A_DQ<20>	31
MEM_A_DQ<19>	MAKE_BASE=TRUE	=MEM_A_DQ<19>	31
MEM_A_DQ<18>	MAKE_BASE=TRUE	=MEM_A_DQ<17>	31
MEM_A_DQ<17>	MAKE_BASE=TRUE	=MEM_A_DQ<18>	31
MEM_A_DQ<16>	MAKE_BASE=TRUE	=MEM_A_DQ<21>	31

MCP CHANNEL A DQS 3 -> DIMM A DQS 3

MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=MEM_A_DQS_N<3>	31
MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=MEM_A_DQS_P<3>	31
MEM_A_DM<3>	MAKE_BASE=TRUE	=MEM_A_DM<3>	31
MEM_A_DQ<31>	MAKE_BASE=TRUE	=MEM_A_DQ<31>	31
MEM_A_DQ<30>	MAKE_BASE=TRUE	=MEM_A_DQ<30>	31
MEM_A_DQ<29>	MAKE_BASE=TRUE	=MEM_A_DQ<29>	31
MEM_A_DQ<28>	MAKE_BASE=TRUE	=MEM_A_DQ<28>	31
MEM_A_DQ<27>	MAKE_BASE=TRUE	=MEM_A_DQ<27>	31
MEM_A_DQ<26>	MAKE_BASE=TRUE	=MEM_A_DQ<26>	31
MEM_A_DQ<25>	MAKE_BASE=TRUE	=MEM_A_DQ<25>	31
MEM_A_DQ<24>	MAKE_BASE=TRUE	=MEM_A_DQ<24>	31

MCP CHANNEL A DQS 4 -> DIMM A DQS 4

MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=MEM_A_DQS_N<4>	31
MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=MEM_A_DQS_P<4>	31
MEM_A_DM<4>	MAKE_BASE=TRUE	=MEM_A_DM<4>	31
MEM_A_DQ<39>	MAKE_BASE=TRUE	=MEM_A_DQ<39>	31
MEM_A_DQ<38>	MAKE_BASE=TRUE	=MEM_A_DQ<38>	31
MEM_A_DQ<37>	MAKE_BASE=TRUE	=MEM_A_DQ<37>	31
MEM_A_DQ<36>	MAKE_BASE=TRUE	=MEM_A_DQ<36>	31
MEM_A_DQ<35>	MAKE_BASE=TRUE	=MEM_A_DQ<35>	31
MEM_A_DQ<34>	MAKE_BASE=TRUE	=MEM_A_DQ<34>	31
MEM_A_DQ<33>	MAKE_BASE=TRUE	=MEM_A_DQ<33>	31
MEM_A_DQ<32>	MAKE_BASE=TRUE	=MEM_A_DQ<32>	31

MCP CHANNEL A DQS 5 -> DIMM A DQS 5

MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=MEM_A_DQS_N<5>	31
MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=MEM_A_DQS_P<5>	31
MEM_A_DM<5>	MAKE_BASE=TRUE	=MEM_A_DM<5>	31
MEM_A_DQ<47>	MAKE_BASE=TRUE	=MEM_A_DQ<47>	31
MEM_A_DQ<46>	MAKE_BASE=TRUE	=MEM_A_DQ<46>	31
MEM_A_DQ<45>	MAKE_BASE=TRUE	=MEM_A_DQ<45>	31
MEM_A_DQ<44>	MAKE_BASE=TRUE	=MEM_A_DQ<44>	31
MEM_A_DQ<43>	MAKE_BASE=TRUE	=MEM_A_DQ<43>	31
MEM_A_DQ<42>	MAKE_BASE=TRUE	=MEM_A_DQ<42>	31
MEM_A_DQ<41>	MAKE_BASE=TRUE	=MEM_A_DQ<41>	31
MEM_A_DQ<40>	MAKE_BASE=TRUE	=MEM_A_DQ<40>	31

MCP CHANNEL A DQS 6 -> DIMM A DQS 6

MEM_A_DQS_N<6>	MAKE_BASE=TRUE	=MEM_A_DQS_N<6>	31
MEM_A_DQS_P<6>	MAKE_BASE=TRUE	=MEM_A_DQS_P<6>	31
MEM_A_DM<6>	MAKE_BASE=TRUE	=MEM_A_DM<6>	31
MEM_A_DQ<55>	MAKE_BASE=TRUE	=MEM_A_DQ<55>	31
MEM_A_DQ<54>	MAKE_BASE=TRUE	=MEM_A_DQ<54>	31
MEM_A_DQ<53>	MAKE_BASE=TRUE	=MEM_A_DQ<53>	31
MEM_A_DQ<52>	MAKE_BASE=TRUE	=MEM_A_DQ<52>	31
MEM_A_DQ<51>	MAKE_BASE=TRUE	=MEM_A_DQ<51>	31
MEM_A_DQ<50>	MAKE_BASE=TRUE	=MEM_A_DQ<50>	31
MEM_A_DQ<49>	MAKE_BASE=TRUE	=MEM_A_DQ<49>	31
MEM_A_DQ<48>	MAKE_BASE=TRUE	=MEM_A_DQ<48>	31

MCP CHANNEL A DQS 7 -> DIMM A DQS 7

MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=MEM_A_DQS_N<7>	31
MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=MEM_A_DQS_P<7>	31
MEM_A_DM<7>	MAKE_BASE=TRUE	=MEM_A_DM<7>	31
MEM_A_DQ<63>	MAKE_BASE=TRUE	=MEM_A_DQ<63>	31
MEM_A_DQ<62>	MAKE_BASE=TRUE	=MEM_A_DQ<62>	31
MEM_A_DQ<61>	MAKE_BASE=TRUE	=MEM_A_DQ<57>	31
MEM_A_DQ<60>	MAKE_BASE=TRUE	=MEM_A_DQ<56>	31
MEM_A_DQ<59>	MAKE_BASE=TRUE	=MEM_A_DQ<59>	31
MEM_A_DQ<58>	MAKE_BASE=TRUE	=MEM_A_DQ<58>	31
MEM_A_DQ<57>	MAKE_BASE=TRUE	=MEM_A_DQ<61>	31
MEM_A_DQ<56>	MAKE_BASE=TRUE	=MEM_A_DQ<60>	31

MCP CHANNEL B DQS 0 -> DIMM B DQS 0

MEM_B_DQS_N<0>	MAKE_BASE=TRUE	=MEM_B_DQS_N<0>	32
MEM_B_DQS_P<0>	MAKE_BASE=TRUE	=MEM_B_DQS_P<0>	32
MEM_B_DM<0>	MAKE_BASE=TRUE	=MEM_B_DM<0>	32
MEM_B_DQ<7>	MAKE_BASE=TRUE	=MEM_B_DQ<7>	32
MEM_B_DQ<6>	MAKE_BASE=TRUE	=MEM_B_DQ<6>	32
MEM_B_DQ<5>	MAKE_BASE=TRUE	=MEM_B_DQ<1>	32
MEM_B_DQ<4>	MAKE_BASE=TRUE	=MEM_B_DQ<0>	32
MEM_B_DQ<3>	MAKE_BASE=TRUE	=MEM_B_DQ<3>	32
MEM_B_DQ<2>	MAKE_BASE=TRUE	=MEM_B_DQ<2>	32
MEM_B_DQ<1>	MAKE_BASE=TRUE	=MEM_B_DQ<5>	32
MEM_B_DQ<0>	MAKE_BASE=TRUE	=MEM_B_DQ<4>	32

MCP CHANNEL B DQS 1 -> DIMM B DQS 1

MEM_B_DQS_N<1>	MAKE_BASE=TRUE	=MEM_B_DQS_N<1>	32
MEM_B_DQS_P<1>	MAKE_BASE=TRUE	=MEM_B_DQS_P<1>	32
MEM_B_DM<1>	MAKE_BASE=TRUE	=MEM_B_DM<1>	32
MEM_B_DQ<15>	MAKE_BASE=TRUE	=MEM_B_DQ<15>	32
MEM_B_DQ<14>	MAKE_BASE=TRUE	=MEM_B_DQ<14>	32
MEM_B_DQ<13>	MAKE_BASE=TRUE	=MEM_B_DQ<13>	32
MEM_B_DQ<12>	MAKE_BASE=TRUE	=MEM_B_DQ<12>	32
MEM_B_DQ<11>	MAKE_BASE=TRUE	=MEM_B_DQ<11>	32
MEM_B_DQ<10>	MAKE_BASE=TRUE	=MEM_B_DQ<10>	32
MEM_B_DQ<9>	MAKE_BASE=TRUE	=MEM_B_DQ<9>	32
MEM_B_DQ<8>	MAKE_BASE=TRUE	=MEM_B_DQ<8>	32

MCP CHANNEL B DQS 2 -> DIMM B DQS 2

MEM_B_DQS_N<2>	MAKE_BASE=TRUE	=MEM_B_DQS_N<2>	32
MEM_B_DQS_P<2>	MAKE_BASE=TRUE	=MEM_B_DQS_P<2>	32
MEM_B_DM<2>	MAKE_BASE=TRUE	=MEM_B_DM<2>	32
MEM_B_DQ<23>	MAKE_BASE=TRUE	=MEM_B_DQ<23>	32
MEM_B_DQ<22>	MAKE_BASE=TRUE	=MEM_B_DQ<22>	32
MEM_B_DQ<21>	MAKE_BASE=TRUE	=MEM_B_DQ<21>	32
MEM_B_DQ<20>	MAKE_BASE=TRUE	=MEM_B_DQ<20>	32
MEM_B_DQ<19>	MAKE_BASE=TRUE	=MEM_B_DQ<19>	32
MEM_B_DQ<18>	MAKE_BASE=TRUE	=MEM_B_DQ<18>	32
MEM_B_DQ<17>	MAKE_BASE=TRUE	=MEM_B_DQ<17>	32
MEM_B_DQ<16>	MAKE_BASE=TRUE	=MEM_B_DQ<16>	32

MCP CHANNEL B DQS 3 -> DIMM B DQS 3

MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=MEM_B_DQS_N<3>	32
MEM_B_DQS_P<3>	MAKE_BASE=TRUE	=MEM_B_DQS_P<3>	32
MEM_B_DM<3>	MAKE_BASE=TRUE	=MEM_B_DM<3>	32
MEM_B_DQ<31>	MAKE_BASE=TRUE	=MEM_B_DQ<31>	32
MEM_B_DQ<30>	MAKE_BASE=TRUE	=MEM_B_DQ<30>	32
MEM_B_DQ<29>	MAKE_BASE=TRUE	=MEM_B_DQ<29>	32
MEM_B_DQ<28>	MAKE_BASE=TRUE	=MEM_B_DQ<28>	32
MEM_B_DQ<27>	MAKE_BASE=TRUE	=MEM_B_DQ<27>	32
MEM_B_DQ<26>	MAKE_BASE=TRUE	=MEM_B_DQ<26>	32
MEM_B_DQ<25>	MAKE_BASE=TRUE	=MEM_B_DQ<25>	32
MEM_B_DQ<24>	MAKE_BASE=TRUE	=MEM_B_DQ<24>	32

MCP CHANNEL B DQS 4 -> DIMM B DQS 4

MEM_B_DQS_N<4>	MAKE_BASE=TRUE	=MEM_B_DQS_N<4>	32
MEM_B_DQS_P<4>	MAKE_BASE=TRUE	=MEM_B_DQS_P<4>	32
MEM_B_DM<4>	MAKE_BASE=TRUE	=MEM_B_DM<4>	32
MEM_B_DQ<39>	MAKE_BASE=TRUE	=MEM_B_DQ<39>	32
MEM_B_DQ<38>	MAKE_BASE=TRUE	=MEM_B_DQ<38>	32
MEM_B_DQ<37>	MAKE_BASE=TRUE	=MEM_B_DQ<37>	32
MEM_B_DQ<36>	MAKE_BASE=TRUE	=MEM_B_DQ<36>	32
MEM_B_DQ<35>	MAKE_BASE=TRUE	=MEM_B_DQ<35>	32
MEM_B_DQ<34>	MAKE_BASE=TRUE	=MEM_B_DQ<34>	32
MEM_B_DQ<33>	MAKE_BASE=TRUE	=MEM_B_DQ<33>	32
MEM_B_DQ<32>	MAKE_BASE=TRUE	=MEM_B_DQ<32>	32

MCP CHANNEL B DQS 5 -> DIMM B DQS 5

MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=MEM_B_DQS_N<5>	32
MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=MEM_B_DQS_P<5>	32
MEM_B_DM<5>	MAKE_BASE=TRUE	=MEM_B_DM<5>	32
MEM_B_DQ<47>	MAKE_BASE=TRUE	=MEM_B_DQ<47>	32
MEM_B_DQ<46>	MAKE_BASE=TRUE	=MEM_B_DQ<46>	32
MEM_B_DQ<45>	MAKE_BASE=TRUE	=MEM_B_DQ<45>	32
MEM_B_DQ<44>	MAKE_BASE=TRUE	=MEM_B_DQ<44>	32
MEM_B_DQ<43>	MAKE_BASE=TRUE	=MEM_B_DQ<43>	32
MEM_B_DQ<42>	MAKE_BASE=TRUE	=MEM_B_DQ<42>	32
MEM_B_DQ<41>	MAKE_BASE=TRUE	=MEM_B_DQ<41>	32
MEM_B_DQ<40>	MAKE_BASE=TRUE	=MEM_B_DQ<40>	32

MCP CHANNEL B DQS 6 -> DIMM B DQS 6

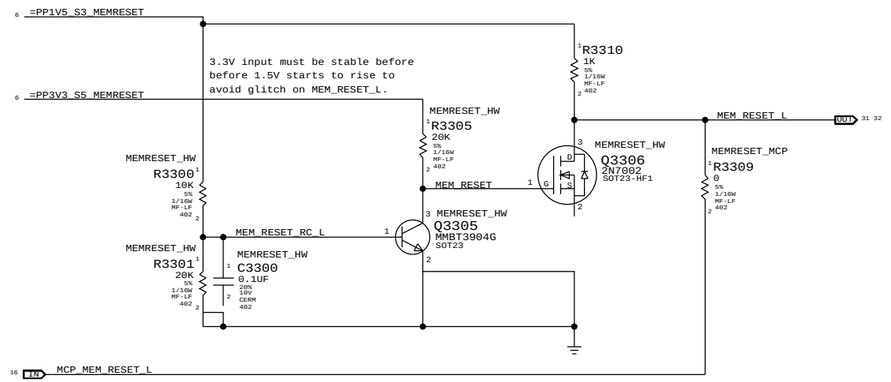
MEM_B_DQS_N<6>	MAKE_BASE=TRUE	=MEM_B_DQS_N<6>	32
MEM_B_DQS_P<6>	MAKE_BASE=TRUE	=MEM_B_DQS_P<6>	32
MEM_B_DM<6>	MAKE_BASE=TRUE	=MEM_B_DM<6>	32
MEM_B_DQ<55>	MAKE_BASE=TRUE	=MEM_B_DQ<55>	32
MEM_B_DQ<54>	MAKE_BASE=TRUE	=MEM_B_DQ<54>	32
MEM_B_DQ<53>	MAKE_BASE=TRUE	=MEM_B_DQ<53>	32
MEM_B_DQ<52>	MAKE_BASE=TRUE	=MEM_B_DQ<52>	32
MEM_B_DQ<51>	MAKE_BASE=TRUE	=MEM_B_DQ<51>	32
MEM_B_DQ<50>	MAKE_BASE=TRUE	=MEM_B_DQ<50>	32
MEM_B_DQ<49>	MAKE_BASE=TRUE	=MEM_B_DQ<49>	32
MEM_B_DQ<48>	MAKE_BASE=TRUE	=MEM_B_DQ<48>	32

MCP CHANNEL B DQS 7 -> DIMM B DQS 7

MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=MEM_B_DQS_N<7>	32
MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=MEM_B_DQS_P<7>	32
MEM_B_DM<7>	MAKE_BASE=TRUE	=MEM_B_DM<7>	32
MEM_B_DQ<63>	MAKE_BASE=TRUE	=MEM_B_DQ<63>	32
MEM_B_DQ<62>	MAKE_BASE=TRUE	=MEM_B_DQ<62>	32
MEM_B_DQ<61>	MAKE_BASE=TRUE	=MEM_B_DQ<61>	32
MEM_B_DQ<60>	MAKE_BASE=TRUE	=MEM_B_DQ<60>	32
MEM_B_DQ<59>	MAKE_BASE=TRUE	=MEM_B_DQ<59>	32
MEM_B_DQ<58>	MAKE_BASE=TRUE	=MEM_B_DQ<58>	32
MEM_B_DQ<57>	MAKE_BASE=TRUE	=MEM_B_DQ<57>	32
MEM_B_DQ<56>	MAKE_BASE=TRUE	=MEM_B_DQ<56>	32

DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



MCP MEMORY CLOCK ALIASES

MEM_A_CLK_P<0>	MAKE_BASE=TRUE	=MEM_A_CLK_P<0>	31
MEM_A_CLK_N<0>	MAKE_BASE=TRUE	=MEM_A_CLK_N<0>	31
MEM_A_CLK_P<1>	MAKE_BASE=TRUE	=MEM_A_CLK_P<1>	31
MEM_A_CLK_N<1>	MAKE_BASE=TRUE	=MEM_A_CLK_N<1>	31
MEM_A_CLK_P<3>	MAKE_BASE=TRUE	=MEM_A_CLK_P<2>	31
MEM_A_CLK_N<3>	MAKE_BASE=TRUE	=MEM_A_CLK_N<2>	31
MEM_A_CLK_P<4>	MAKE_BASE=TRUE	=MEM_A_CLK_P<3>	31
MEM_A_CLK_N<4>	MAKE_BASE=TRUE	=MEM_A_CLK_N<3>	31

MEM_B_CLK_P<0>	MAKE_BASE=TRUE	=MEM_B_CLK_P<0>	32
MEM_B_CLK_N<0>	MAKE_BASE=TRUE	=MEM_B_CLK_N<0>	32
MEM_B_CLK_P<1>	MAKE_BASE=TRUE	=MEM_B_CLK_P<1>	32
MEM_B_CLK_N<1>	MAKE_BASE=TRUE	=MEM_B_CLK_N<1>	32
MEM_B_CLK_P<3>	MAKE_BASE=TRUE	=MEM_B_CLK_P<2>	32
MEM_B_CLK_N<3>	MAKE_BASE=TRUE	=MEM_B_CLK_N<2>	32
MEM_B_CLK_P<4>	MAKE_BASE=TRUE	=MEM_B_CLK_P<3>	32
MEM_B_CLK_N<4>	MAKE_BASE=TRUE	=MEM_B_CLK_N<3>	32

MCP MEMORY TEST POINT ALIASES

TP_MEM_A_A<15>	MAKE_BASE=TRUE	MEM_A_A<15>	31
TP_MEM_B_A<15>	MAKE_BASE=TRUE	MEM_B_A<15>	32

PAGE TITLE
DDR3 SUPPORT AND BITSWAPS

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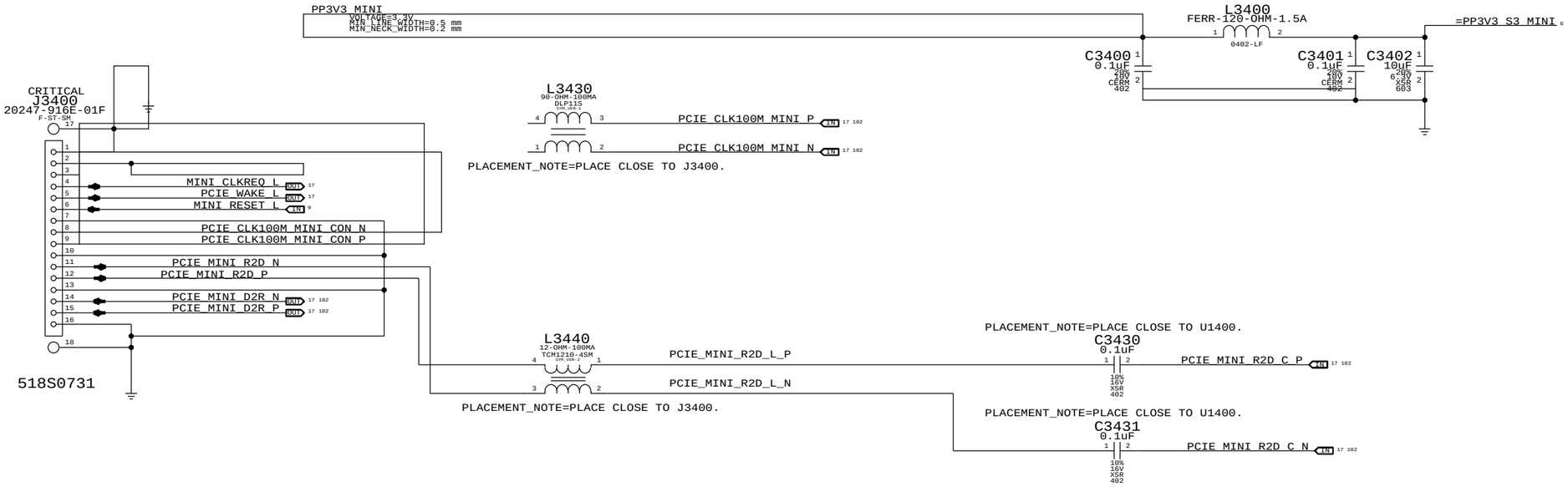

PAGE TITLE
PCI-E Wireless Connector

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8 7 6 5 4 3 2 1

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8 7 6 5 4 3 2 1

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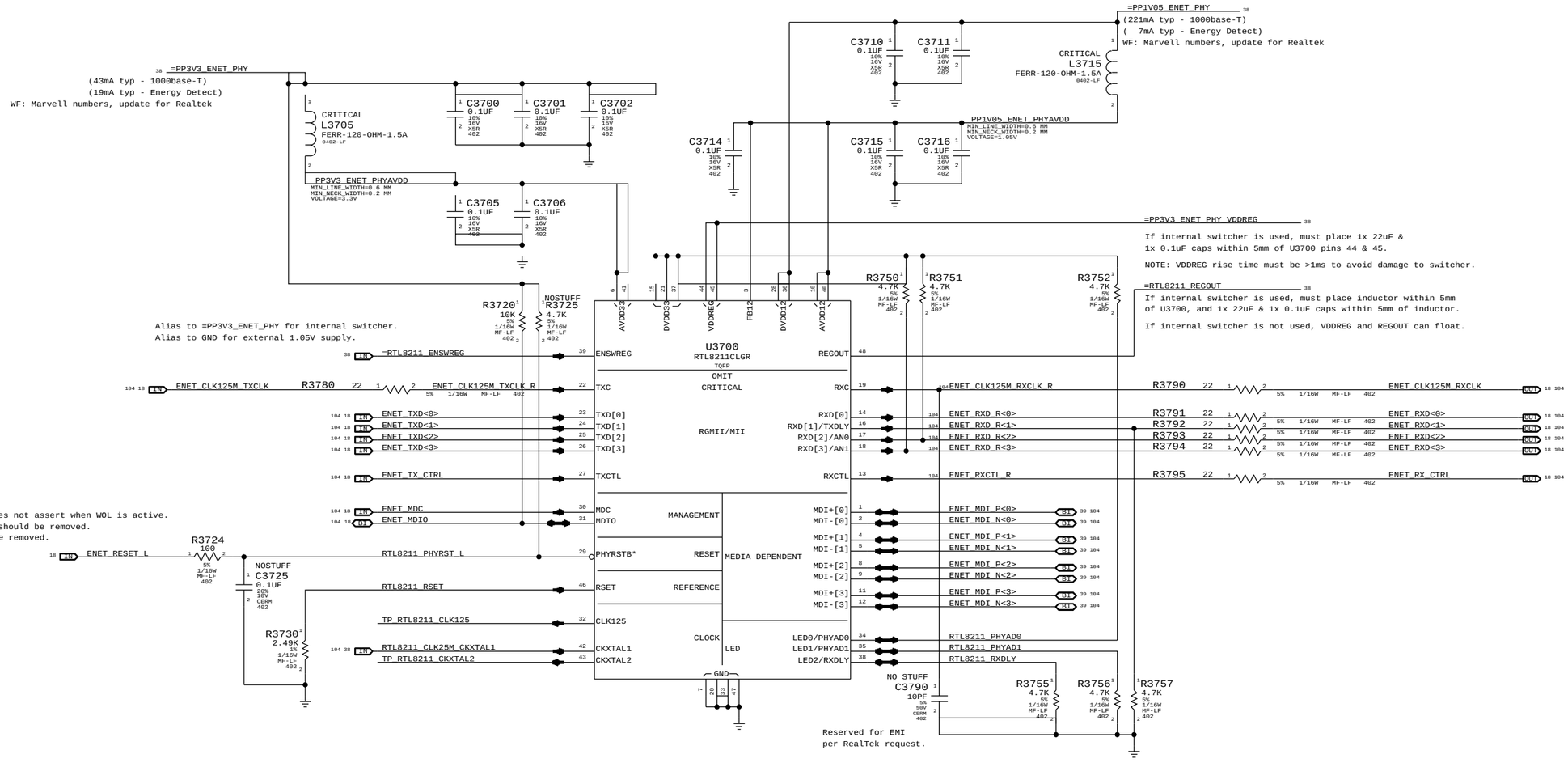

Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

PAGE TITLE: Ethernet PHY (RTL8211CL)

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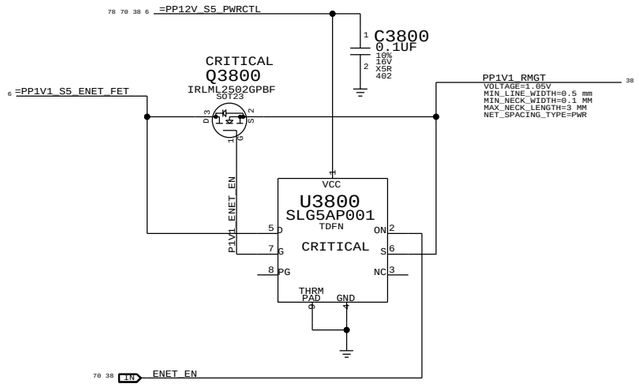
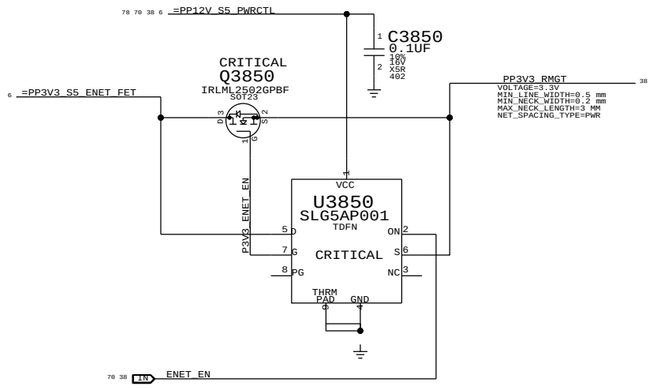
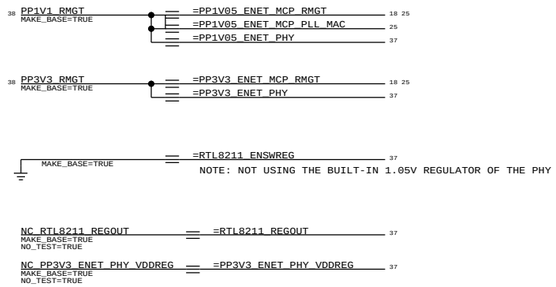
1.1V ENET FET



3.3V ENET FET



ENET ALIASES



RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.

PAGE TITLE: Ethernet Support

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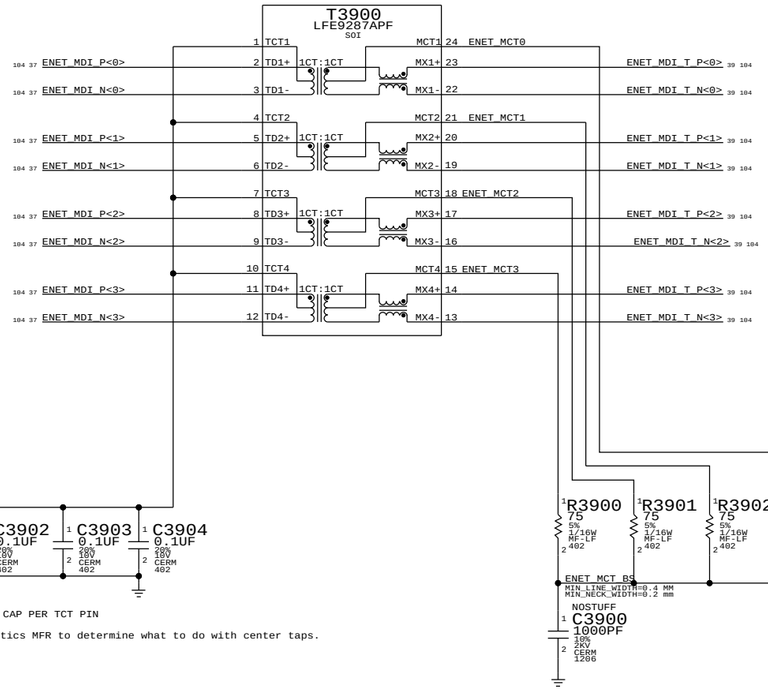
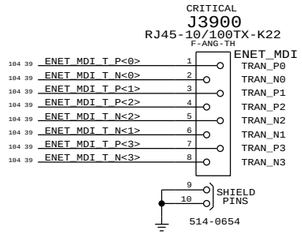


PLACE ONE CAP PER TCT PIN

NOTE: Check with PHY and Magnetics MFR to determine what to do with center taps.

NOTE: BOB SMITH TERMINATION FOR EMC.



PAGE TITLE: ETHERNET CONNECTOR

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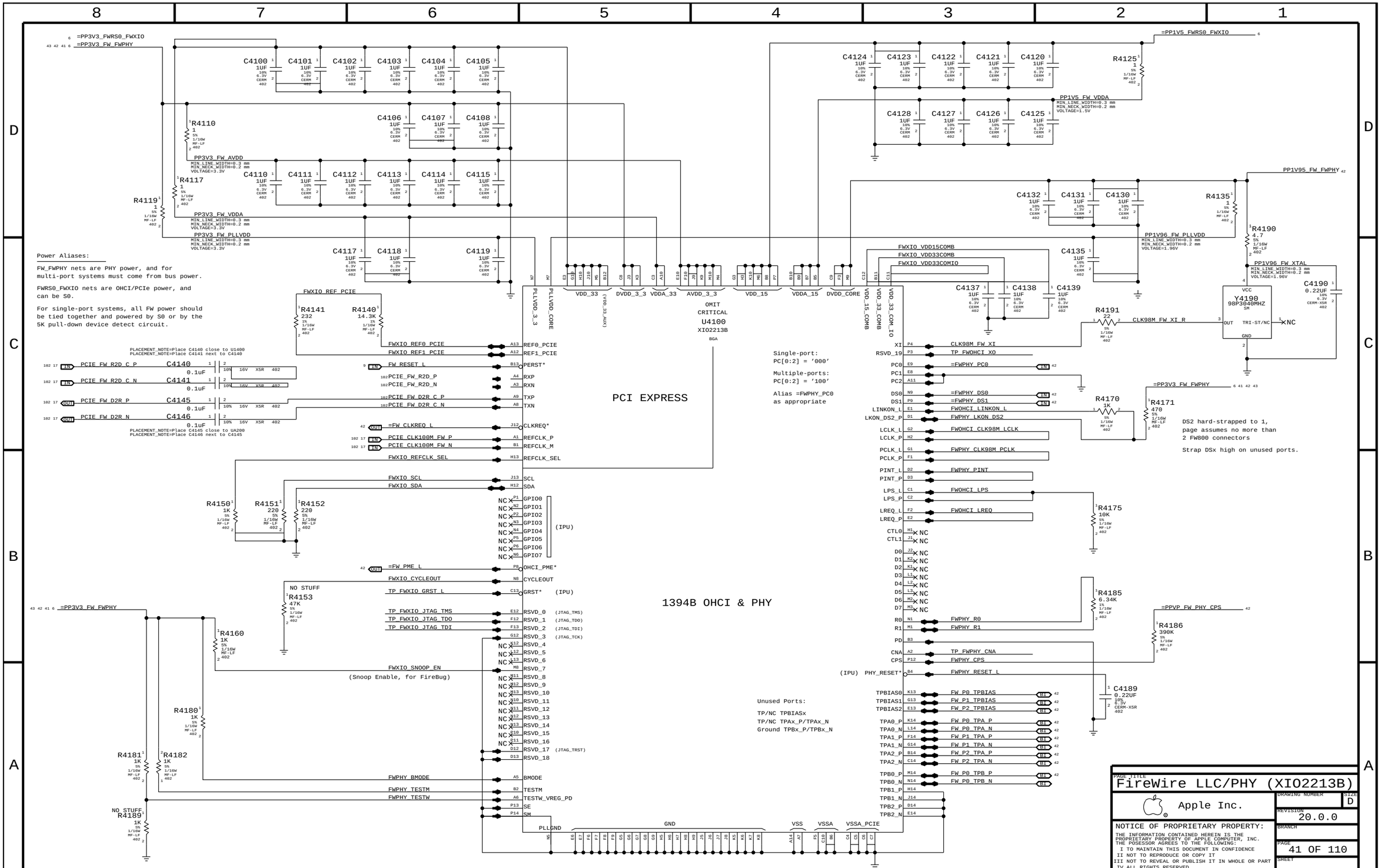
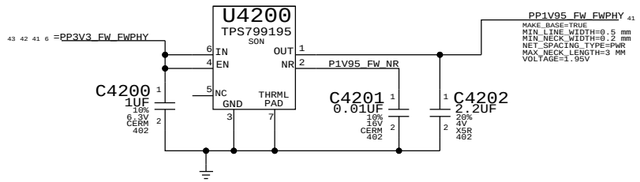


1394 PHY 1.95V SUPPLY



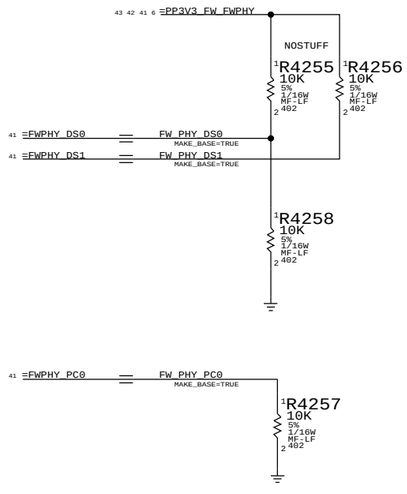
FireWire Aliases For Connectivity

=FW_CLKREQ_L = FW_CLKREQ_L 17 (MAKE_BASE=TRUE)

=FW_PME_L = FW_PME_L 19 (MAKE_BASE=TRUE)

=PPVP_FW_PHY_CPS = PPVP_FW_PHY_CPS 43 (MAKE_BASE=TRUE)

1394 PHY STRAPPING OPTIONS

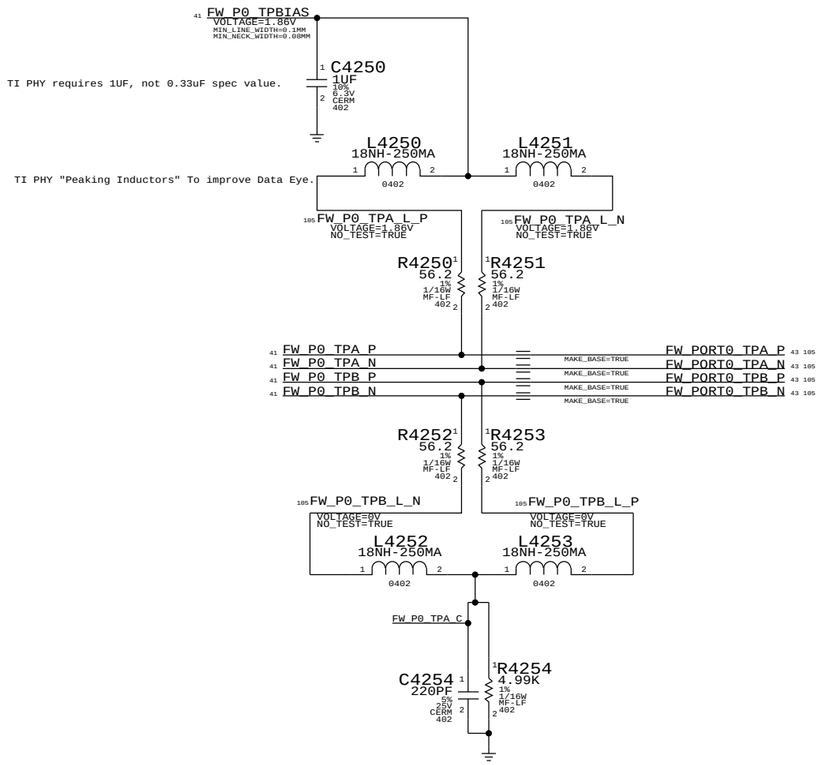


THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE.

iMacs are now one port only and have Power Code "000"

Termination

Place close to FireWire PHY



2ND & 3RD TPA/TPB PAIR UNUSED

FW_P1_TPBIAS = NC_FW_PORT1_TPBIAS (MAKE_BASE=TRUE, NO_TEST=TRUE)

FW_P1_TPA_P = NC_FW_PORT1_TPA_P (MAKE_BASE=TRUE, NO_TEST=TRUE)

FW_P1_TPA_N = NC_FW_PORT1_TPA_N (MAKE_BASE=TRUE, NO_TEST=TRUE)

FW_P2_TPBIAS = NC_FW_PORT2_TPBIAS (MAKE_BASE=TRUE, NO_TEST=TRUE)

FW_P2_TPA_P = NC_FW_PORT2_TPA_P (MAKE_BASE=TRUE, NO_TEST=TRUE)

FW_P2_TPA_N = NC_FW_PORT2_TPA_N (MAKE_BASE=TRUE, NO_TEST=TRUE)

PAGE TITLE: FW: 1394B MISC

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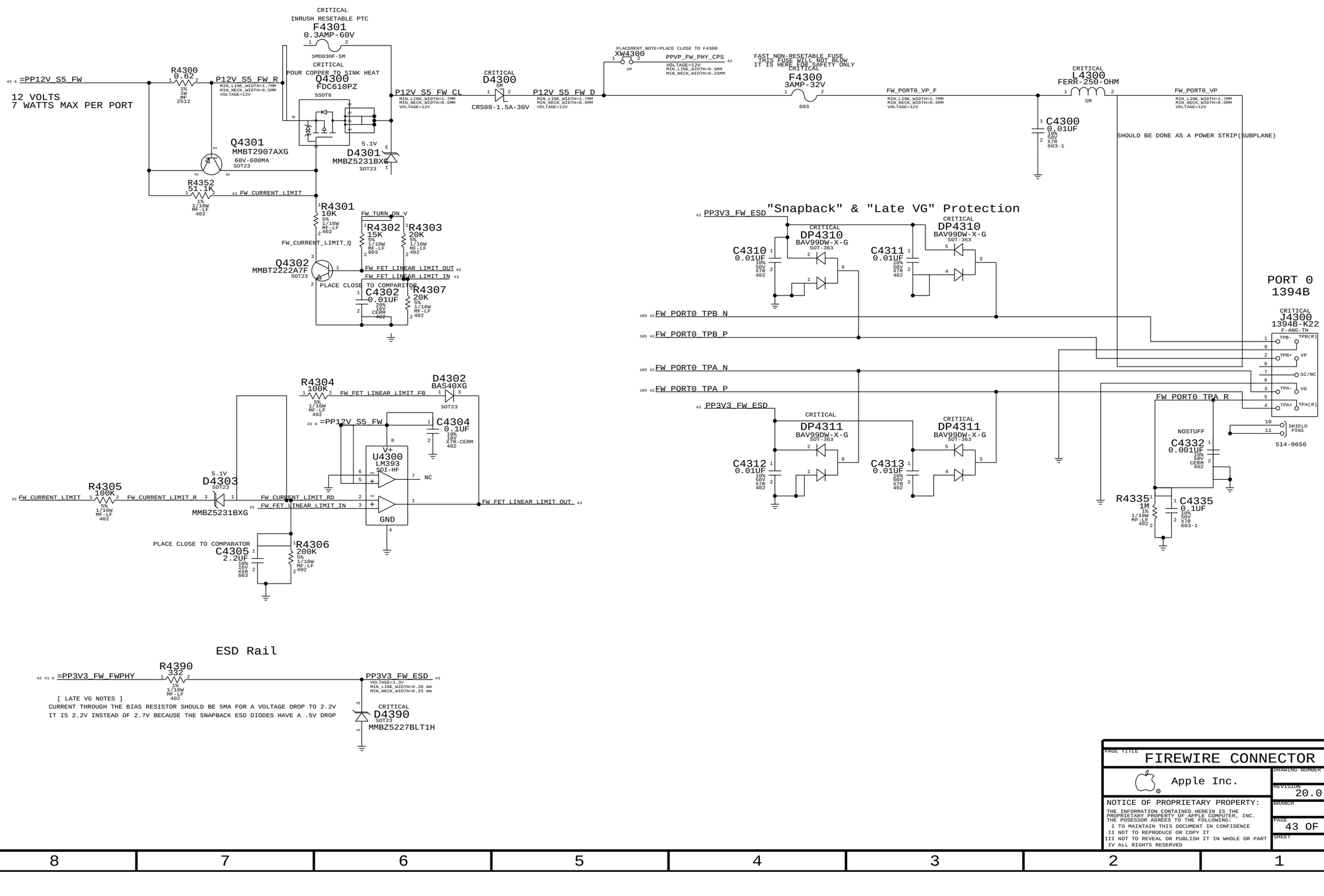

PAGE TITLE: FIREWIRE CONNECTOR

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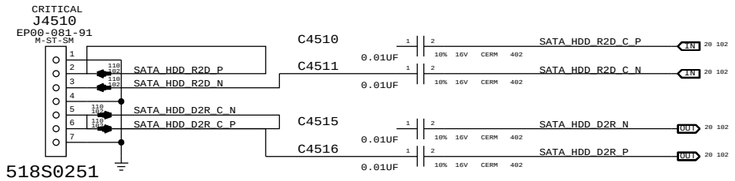
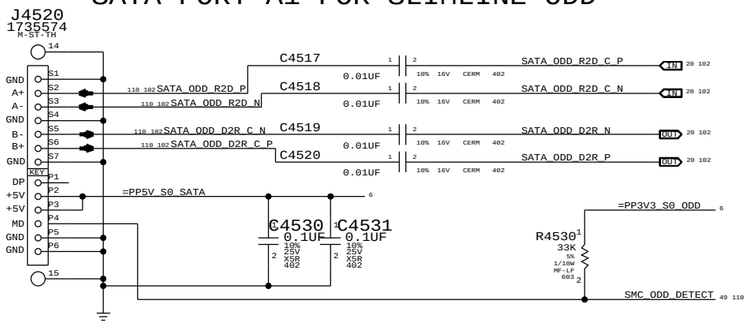
SATA PORT A0 FOR HDD

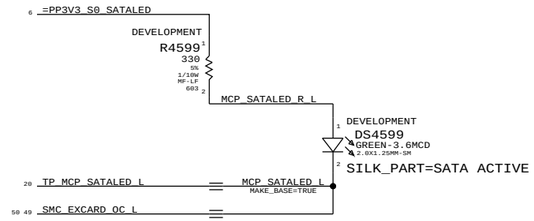


518-0361

SATA PORT A1 FOR SLIMLINE ODD



SATA Activity LED



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SATA Connectors

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USB/SMC DEBUG MUX

PORT 3

=PP5V_S3_USB
U4601 TPS2060 MSOP
USB_EXTC_OC_L
USB_EXTD_OC_L
R4600 10K 5% 1/16W MF-LF 402
USB_PWR_ENA_L
C4605 0.1UF 20% 16V CERM 402
C4606 150UF 20% 6.3V POLY-TANT CASE-D2-SM NOSTUFF
Q4600 2N7002 SOT23-HF
PM_EN_USB_PWR
C4621 0.1UF 20% 16V CERM 402
C4631 0.1UF 20% 16V CERM 402
=PP3V3_S5_SMCUSBMUX
C4650 0.1UF 20% 16V CERM 402
SMC_RX_L
SMC_TX_L
USB_EXTD_P
USB_EXTD_N
U4650 PI3USB102ZLE TQFN MOJOMUX
USB_DEBUGPRT_EN_L
SEL=0: CHOOSE SMC
SEL=1: CHOOSE USB
R4651 0 PRODUCTION 5% 1/10W MF-LF 402
R4652 0 PRODUCTION 5% 1/10W MF-LF 402
USB_D_MUXED_N
USB_D_MUXED_P
L4630 FERR-250-OHM SM
PP5V_USB2_PORT3 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
PP5V_USB2_PORT3_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
C4630 0.01UF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)
L4631 120-OHM-90MA DLP0NS
USB_PORT3_N
USB_PORT3_P
J4630 USB-K22 F-ANG-TH
VDD D- D+ GND VBUS DATA- DATA+ GND
514-0659
D4630 RCLAMP0502N SLP1210N6
NC NC NC IO IO VBUS GND

PORT 2

L4620 FERR-250-OHM SM
PP5V_USB2_PORT2 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
PP5V_USB2_PORT2_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
C4620 0.01UF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)
L4621 120-OHM-90MA DLP0NS
USB_EXTC_N
USB_EXTC_P
USB_PORT2_N
USB_PORT2_P
J4620 USB-K22 F-ANG-TH
514-0659
D4620 RCLAMP0502N SLP1210N6

PORT 1

U4600 TPS2060 MSOP
=PP5V_S3_USB
USB_EXTA_OC_L
USB_EXTB_OC_L
C4601 0.1UF 20% 16V CERM 402
C4602 150UF 20% 6.3V POLY-TANT CASE-D2-SM NOSTUFF
C4603 0.1UF 20% 16V CERM 402
C4611 0.1UF 20% 16V CERM 402
L4610 FERR-250-OHM SM
PP5V_USB2_PORT1 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
PP5V_USB2_PORT1_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
C4610 0.01UF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)
L4611 120-OHM-90MA DLP0NS
USB_EXTB_N
USB_EXTB_P
USB_PORT1_N
USB_PORT1_P
J4610 USB-K22 F-ANG-TH1
514-0672
D4610 RCLAMP0502N SLP1210N6

PORT 0

L4600 FERR-250-OHM SM
PP5V_USB2_PORT0 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
PP5V_USB2_PORT0_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
C4600 0.01UF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)
L4601 120-OHM-90MA DLP0NS
USB_EXTA_N
USB_EXTA_P
USB_PORT0_N
USB_PORT0_P
J4600 USB-K22 F-ANG-TH1
514-0672
D4600 RCLAMP0502N SLP1210N6

PAGE TITLE
EXTERNAL USB CONNECTORS

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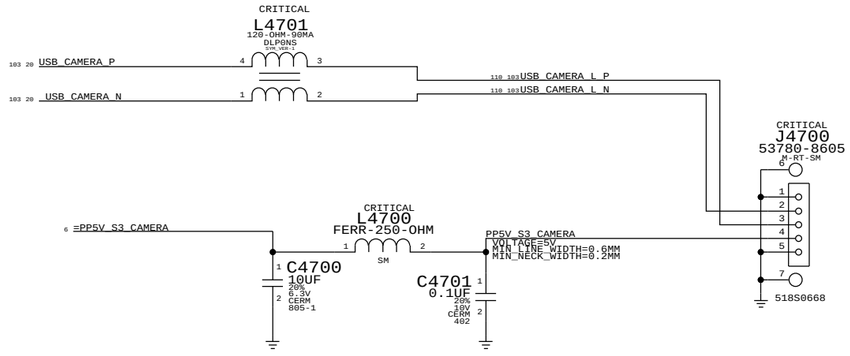
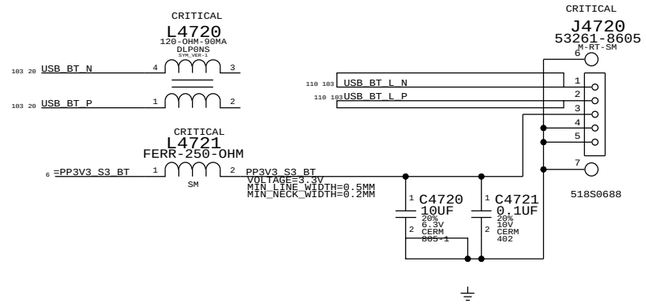
CAMERA CONNECTOR & FILTER

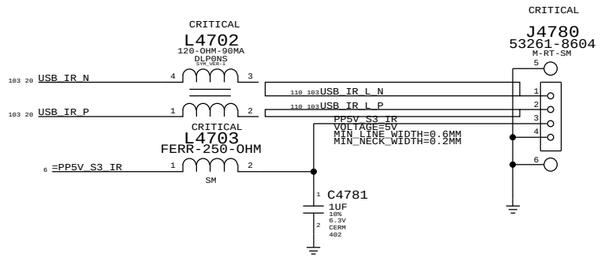


LAYOUT NOTE:
PLACE C4700, C4701 & L4700
NEAR J4700 PINS 4 AND 5 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.

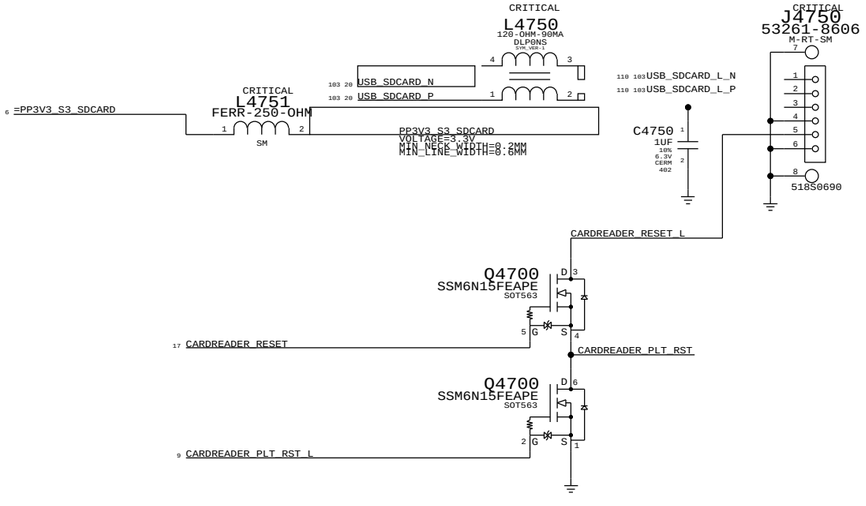
K37L (BLUETOOTH) CONNECTOR



IR RECEIVER CONNECTOR



SD Card Reader Board Connector



PAGE TITLE	Internal USB Connections
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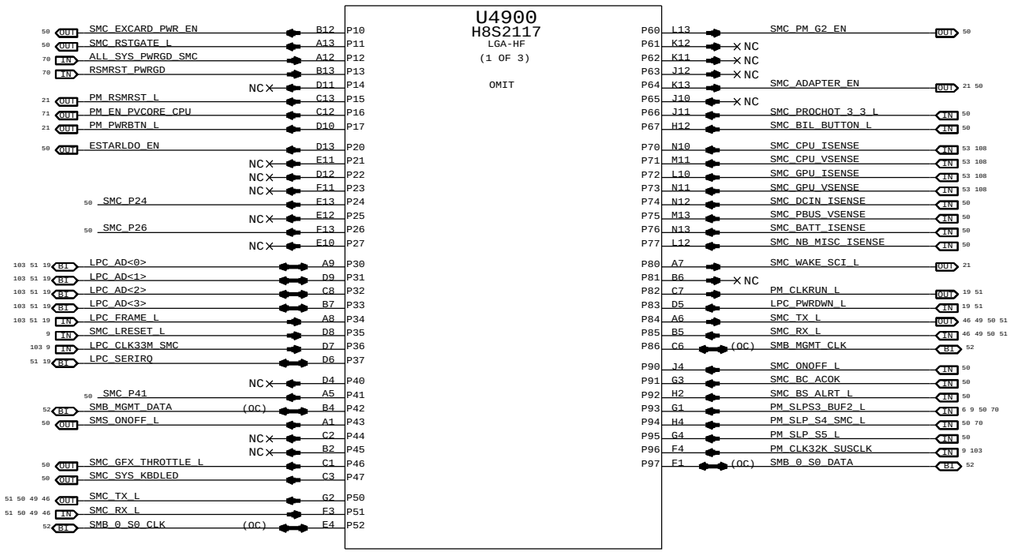
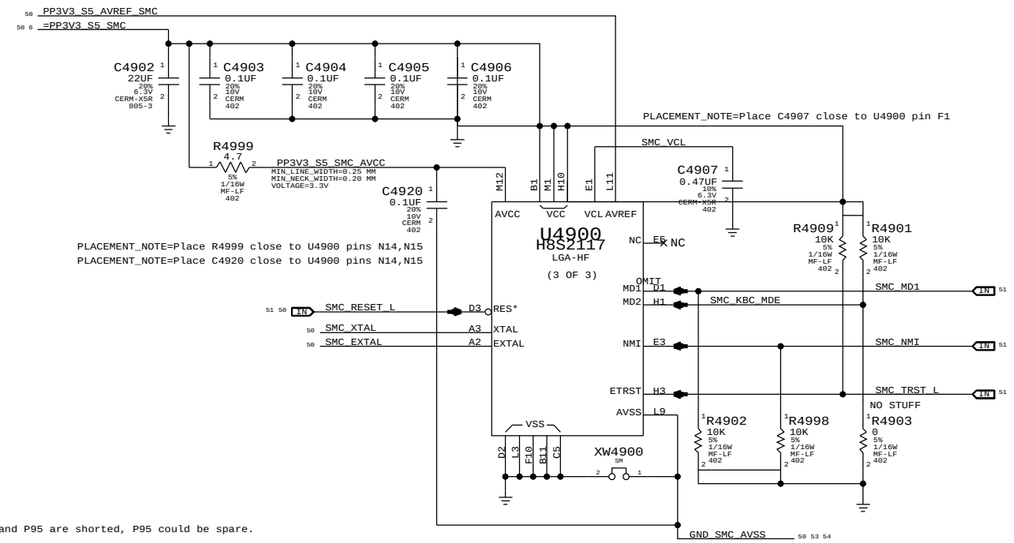
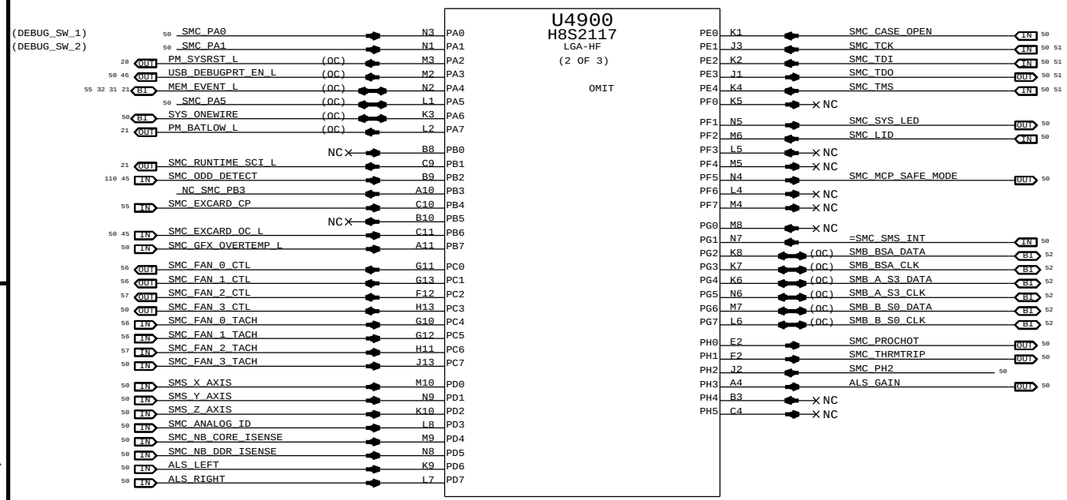
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





NOTE: P94 and P95 are shorted, P95 could be spare.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

PAGE TITLE: SMC

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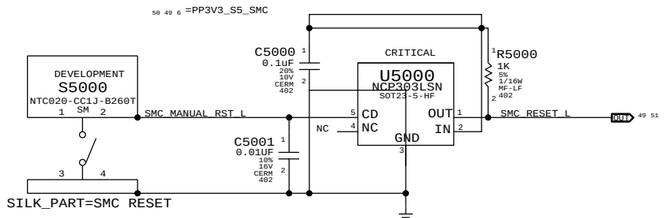
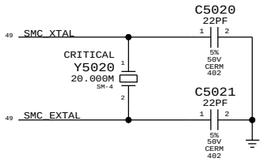
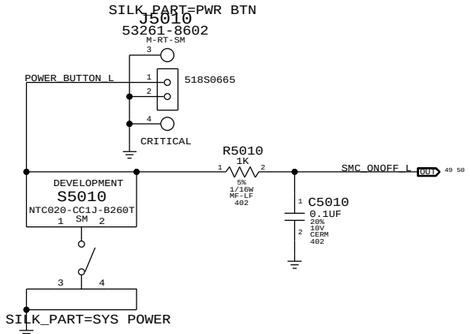
SMC Reset Button / Brownout Detect



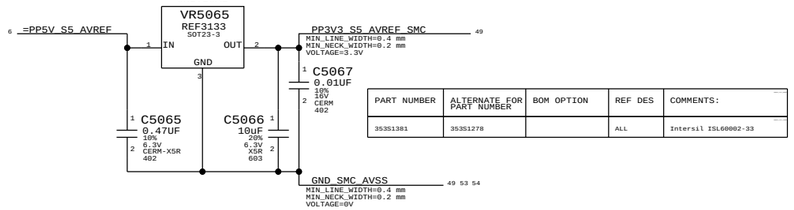
SMC Crystal Circuit



POWER BUTTON



SMC AVREF Supply



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		ALL	Intersil ISL60002-33

UNUSED TP/NC ALIASES - PORT D - INTERNAL PULLUPS

SMS_Z_AXIS	NC_SMS_Z_AXIS	MAKE_BASE=TRUE	NO_TEST=TRUE
ALS_LEFT	NC_ALS_LEFT	MAKE_BASE=TRUE	NO_TEST=TRUE
ALS_RIGHT	NC_ALS_RIGHT	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_ANALOG_ID	NC_SMC_ANALOG_ID	MAKE_BASE=TRUE	NO_TEST=TRUE

UNUSED TP/NC ALIASES

SMC_SYS_LED	TP_SMC_SYS_LED	MAKE_BASE=TRUE	
ALS_GAIN	NC_ALS_GAIN	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_PM_G2_EN	TP_SMC_PM_G2_EN	MAKE_BASE=TRUE	
SMC_SYS_KBDLED	TP_SMC_SYS_KBDLED	MAKE_BASE=TRUE	
SMC_EXCARD_PWR_EN	TP_SMC_EXCARD_PWR_EN	MAKE_BASE=TRUE	
SMS_ONOFF_L	TP_SMS_ONOFF_L	MAKE_BASE=TRUE	
SMC_RSTGATE_L	TP_SMC_RSTGATE_L	MAKE_BASE=TRUE	
SMC_P24	TP_SMC_P24	MAKE_BASE=TRUE	
SMC_P26	TP_SMC_P26	MAKE_BASE=TRUE	
SMC_P41	TP_SMC_P41	MAKE_BASE=TRUE	
ESTARLDO_EN	TP_ESTARLDO_EN	MAKE_BASE=TRUE	

ANALOG SENSORS

SMC_DCIN_ISENSE	SMC_CPU_INPUT_ISENSE	MAKE_BASE=TRUE	53
SMC_PBUS_VSENSE	SMC_CPU_INPUT_VSENSE	MAKE_BASE=TRUE	53
SMS_X_AXIS	SMC_1V5_S0_VSENSE	MAKE_BASE=TRUE	54 108
SMS_Y_AXIS	SMC_MCP_CORE_VSENSE	MAKE_BASE=TRUE	54 108
SMC_NB_DDR_ISENSE	SMC_1V5_S0_ISENSE	MAKE_BASE=TRUE	54 108
SMC_NB_CORE_ISENSE	SMC_MCP_CORE_ISENSE	MAKE_BASE=TRUE	54 108
SMC_BATT_ISENSE	SMC_UNUSED_ADC_PORT7	MAKE_BASE=TRUE	
SMC_NB_MISC_ISENSE			

R5050 10K 5% 1/10W MF-LF 402

MISC. SIGNAL ALIASES

SMC_GFX_OVERTEMP_L	MXM_ALERT_L	MAKE_BASE=TRUE	85
SMC_GFX_THROTTLE_L	MXM_PWR_LEVEL	MAKE_BASE=TRUE	85

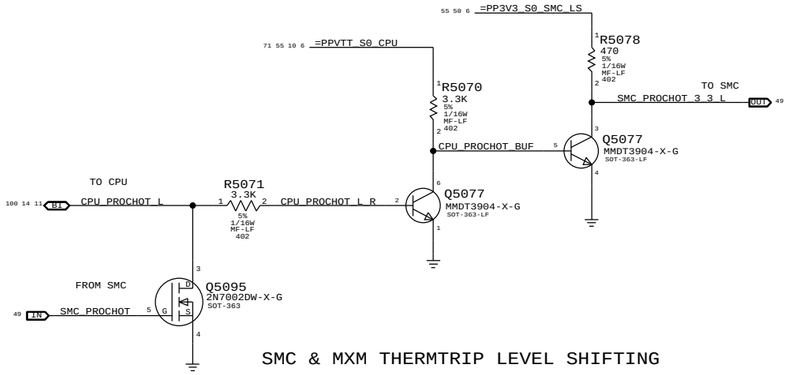
IG R5020 51 5% 1/16W MF-LF 402 — SMC_IG_THROTTLE_L (MAKE_BASE=TRUE) 21

R5019 0 5% 1/16W MF-LF 402

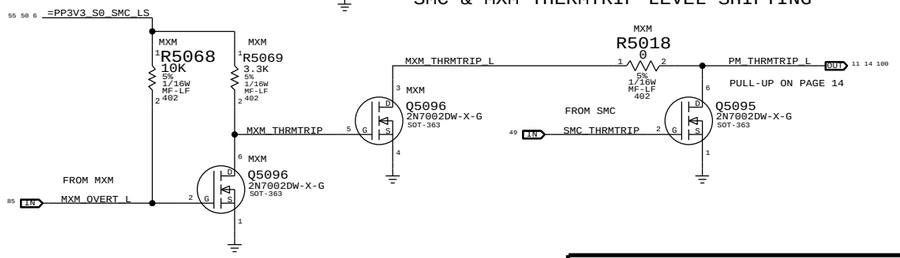
SMC_MCP_SAFE_MODE — MCP_SPKR 21

FOR <RDAR://PROBLEM/5925345>

SMC PROCHOT 3.3V LEVEL SHIFTING



SMC & MXM THERMTRIP LEVEL SHIFTING



SMC PROCHOT 3.3V LEVEL SHIFTING

SMC_ONOFF_L	R5032	10K		
SMC_LID	R5033	100K		
SMC_PH2	R5034	10K		
SMC_TX_L	R5035	10K		
SMC_RX_L	R5036	100K		
SYS_ONEWIRE	R5037	2.0K		
SMC_BS_ALRT_L	R5038	100K		
SMC_TMS	R5039	10K		
SMC_TDO	R5040	10K		
SMC_TDI	R5041	10K		
SMC_TCK	R5042	10K		
SMC_EXCARD_OC_L	R5043	10K	NO STUFF	
SMC_PA0	R5096	10K		
SMC_PA1	R5090	10K		
SMC_BIL_BUTTON_L	R5092	10K		
SMC_FAN_3_CTL	R5095	100K		
SMC_FAN_3_TACH	R5097	100K		
SMC_BC_ACOK	R5047	10K		
SMC_ADAPTER_EN	R5049	10K		
USB_DEBUGPRT_EN_L	R5098	10K		
=SMC_SMS_INT — SMC_SMS_INT	R5091	10K		

All: 5% 1/16W MF-LF 402

=PP3V3_S5_SMC

SMC_PA5	R5093	10K	
SMC_GFX_OVERTEMP_L	R5099	10K	
SMC_CASE_OPEN	R5046	10K	
PM_SLP3_BUF2_L	R5094	100K	
PM_SLP_S4_SMC_L	R5089	100K	MAKE_BASE=TRUE
PM_SLP_S5_L			

All: 5% 1/16W MF-LF 402

=PP3V3_S0_SMC

PLACEMENT_NOTE=PLACE CLOSE TO U4900(SMC)

PAGE TITLE	SMC Support
	Apple Inc.
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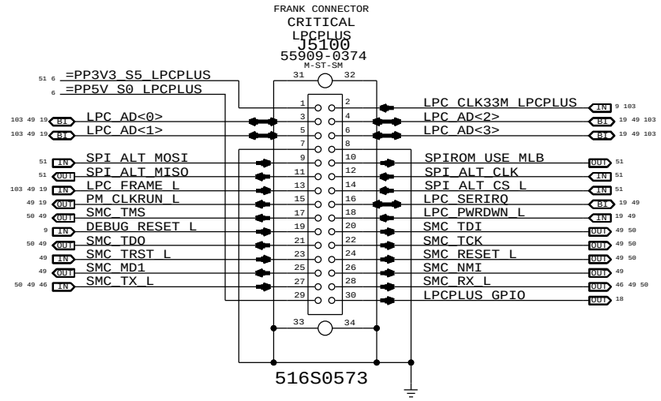
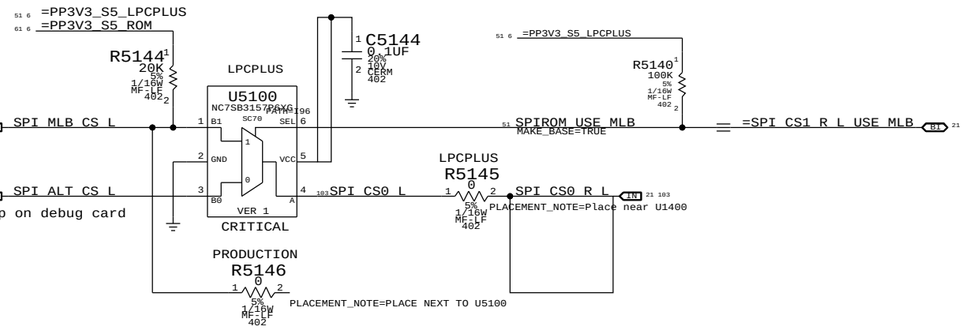
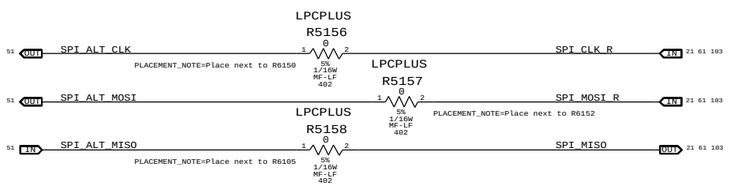
LPC+SPI Connector



Alternate SPI ROM Support



SPI Bus Series Resistance Option



PAGE TITLE
LPC+SPI Debug Connector

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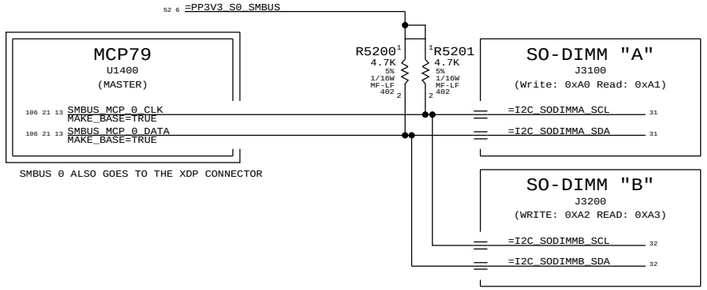
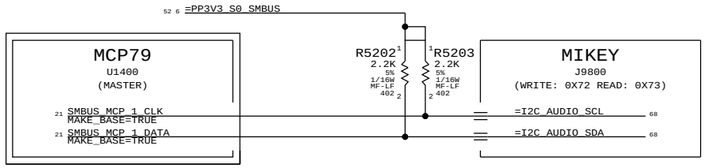
MCP79 SMBUS "0" CONNECTIONS

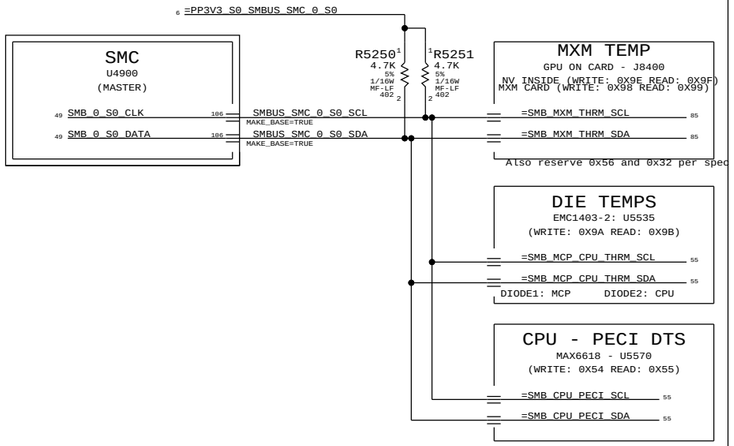


SMBUS 0 ALSO GOES TO THE XDP CONNECTOR

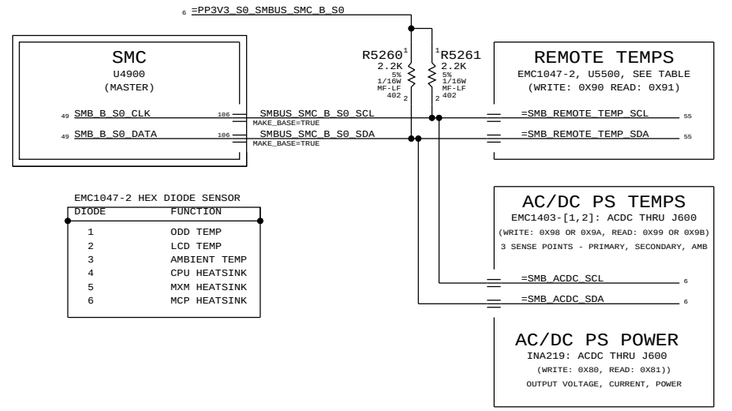
MCP79 SMBUS "1" CONNECTIONS



SMC "0" SMBus Connections



SMC "B" SMBus Connections

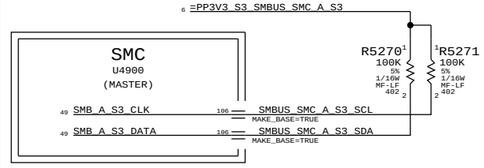


EMC1047-2 HEX DIODE SENSOR

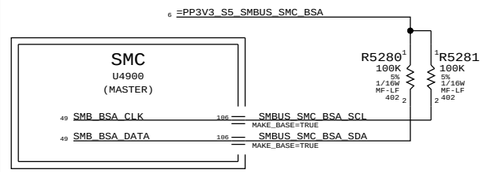
DIODE	FUNCTION
1	ODD TEMP
2	LCD TEMP
3	AMBIENT TEMP
4	CPU HEATSINK
5	MXM HEATSINK
6	MCP HEATSINK

SMC "A" SMBus Connections

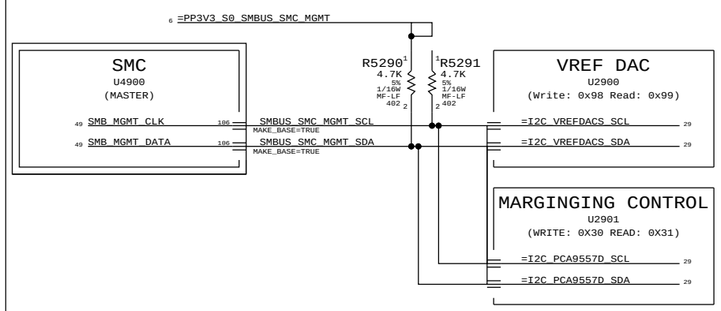
NOTE: SMC RMT BUS REMAINS POWERED AND MAY BE ACTIVE IN S3 STATE



UNUSED SMC "BATTERY A" SMBUS CONNECTIONS



SMC "MANAGEMENT" SMBUS CONNECTIONS



PAGE TITLE	SMBUS CONNECTIONS
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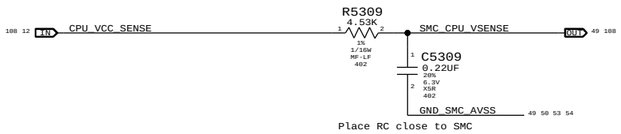
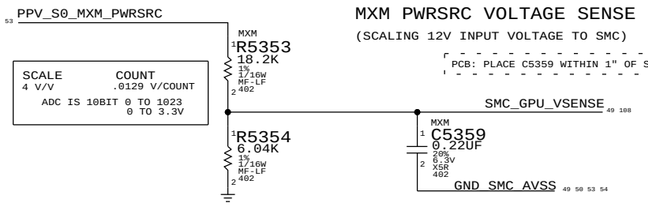
CPU Voltage Sense / Filter



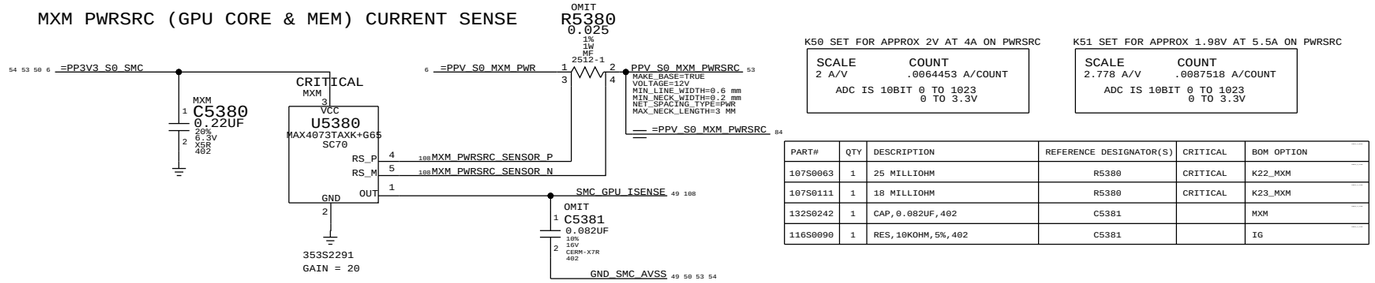
Place RC close to SMC

MXM PWRSRC VOLTAGE SENSE

(SCALING 12V INPUT VOLTAGE TO SMC)



MXM PWRSRC (GPU CORE & MEM) CURRENT SENSE



K50 SET FOR APPROX 2V AT 4A ON PWRSRC

SCALE	COUNT
2 A/V	.0064453 A/COUNT

ADC IS 10BIT 0 TO 1023
0 TO 3.3V

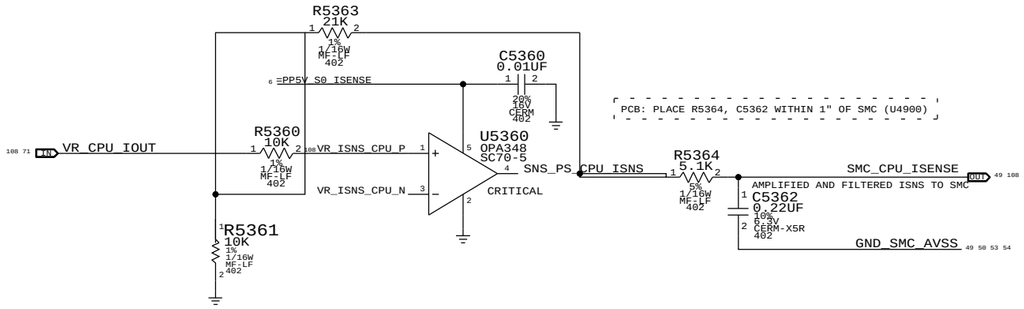
K51 SET FOR APPROX 1.98V AT 5.5A ON PWRSRC

SCALE	COUNT
2.778 A/V	.0087518 A/COUNT

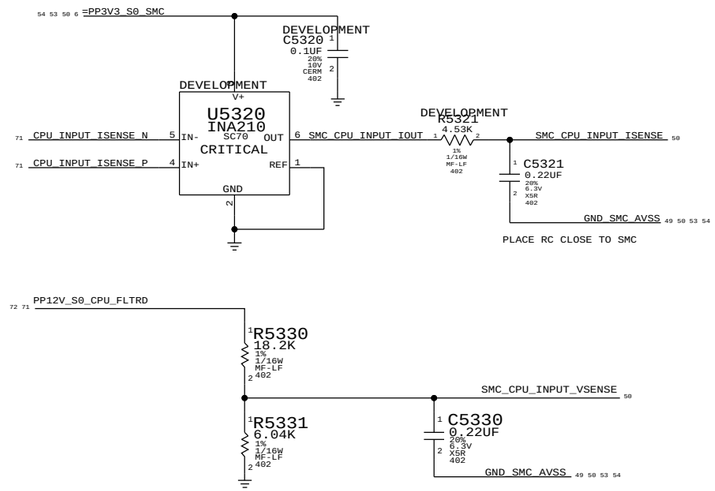
ADC IS 10BIT 0 TO 1023
0 TO 3.3V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
107S0063	1	25 MILLIOHM	R5380	CRITICAL	K22_MXM
107S0111	1	18 MILLIOHM	R5380	CRITICAL	K23_MXM
132S0242	1	CAP,0.082UF,402	C5381		MXM
116S0090	1	RES,10KOHM,5%,402	C5381		IG

CPU CURRENT SENSE AMP & FILTER



CPU CORE INPUT SIDE CURRENT & VOLTAGE SENSE



PAGE TITLE	CPU/MXM CURRENT AND VOLTAGE SENSE
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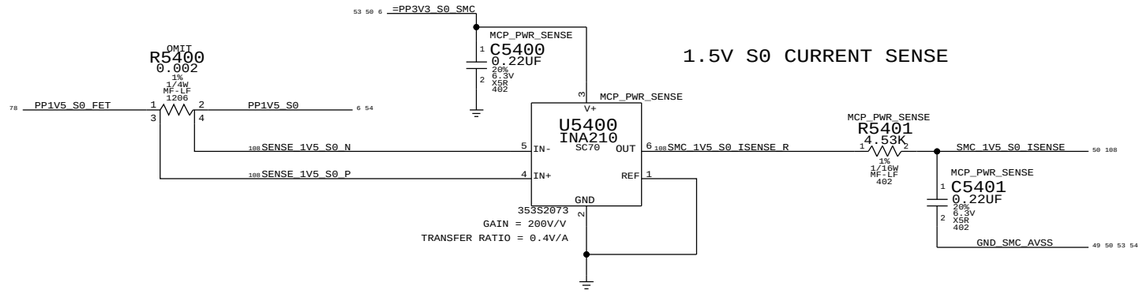
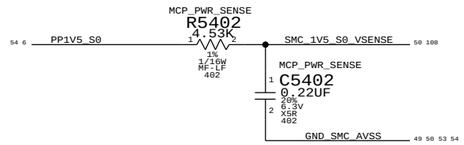
1.5V S0 CURRENT SENSE

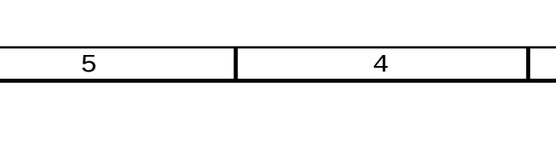


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
104S0018	1	RES,2 MILLIOHM,1206	R5400	CRITICAL	MCP_PWR_SENSE
101S0414	1	RES,0 OHM,1206,20MILLIOHM MAX	R5400	CRITICAL	PRODUCTION

1.5V S0 VOLTAGE SENSE

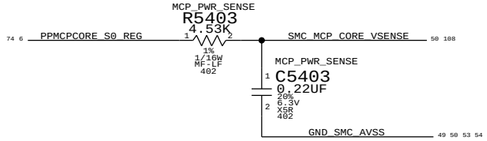


MCP CORE CURRENT SENSE



SCALE IS 0.116 V/A

MCP CORE VOLTAGE SENSE



PAGE TITLE
MCP CURRENT AND VOLTAGE SENSE

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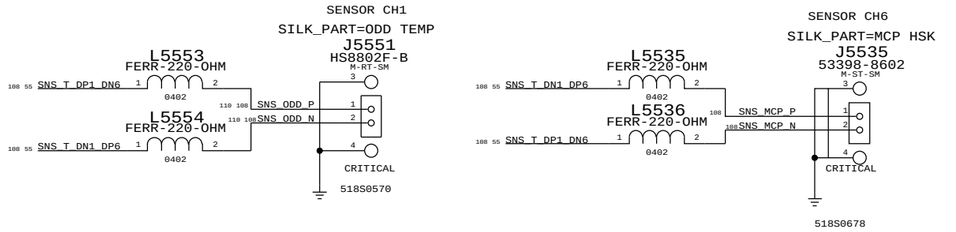
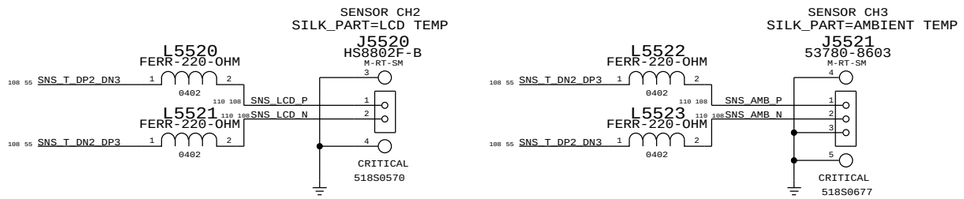
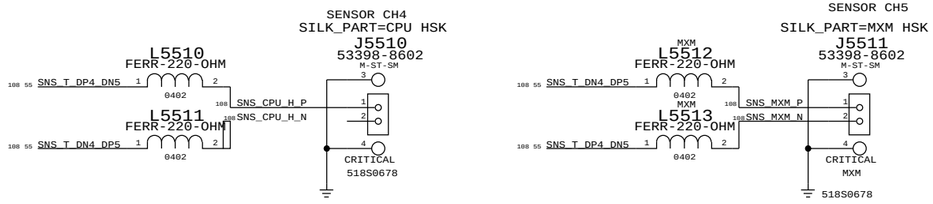
REMOTE THERMAL SENSORS
HEATSINKS, AMBIENT, PANEL AND ODD

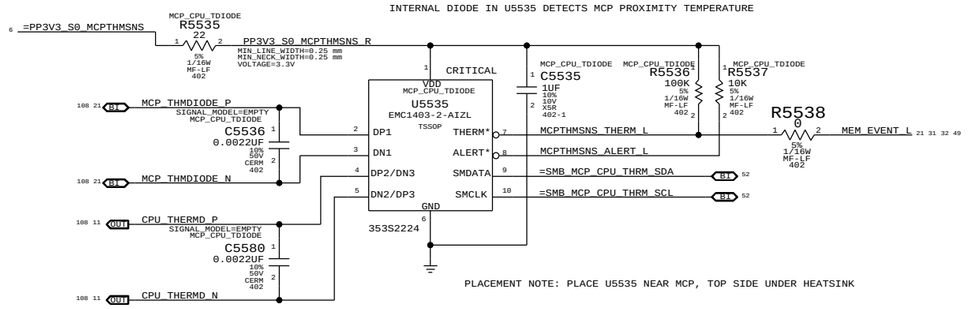




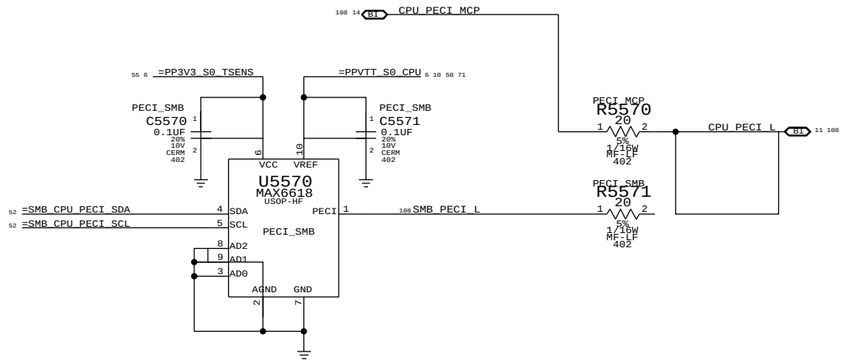
PLACE HSK SENSOR CONN. TOP SIDE NEAR MXM OR CPU



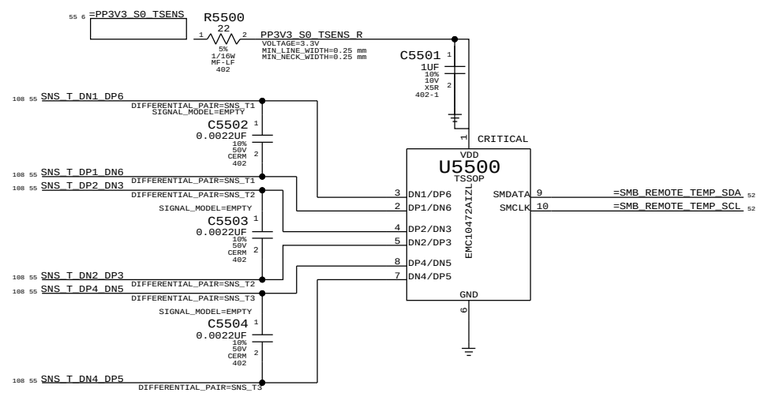
MCP & CPU T-Diode Thermal Sensor



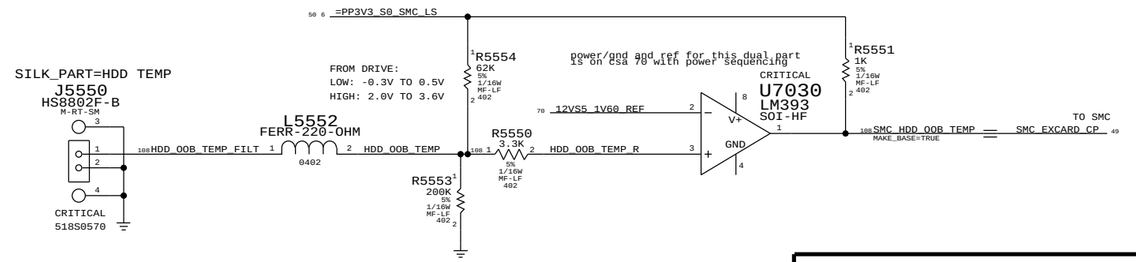
CPU PECI DTS OPTIONS



REMOTE THERMAL SENSORS (HEATSINKS AND ODD)



HDD OUT OF BAND TEMPERATURE SENSING LEVEL SHIFTING



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	Apple Inc.
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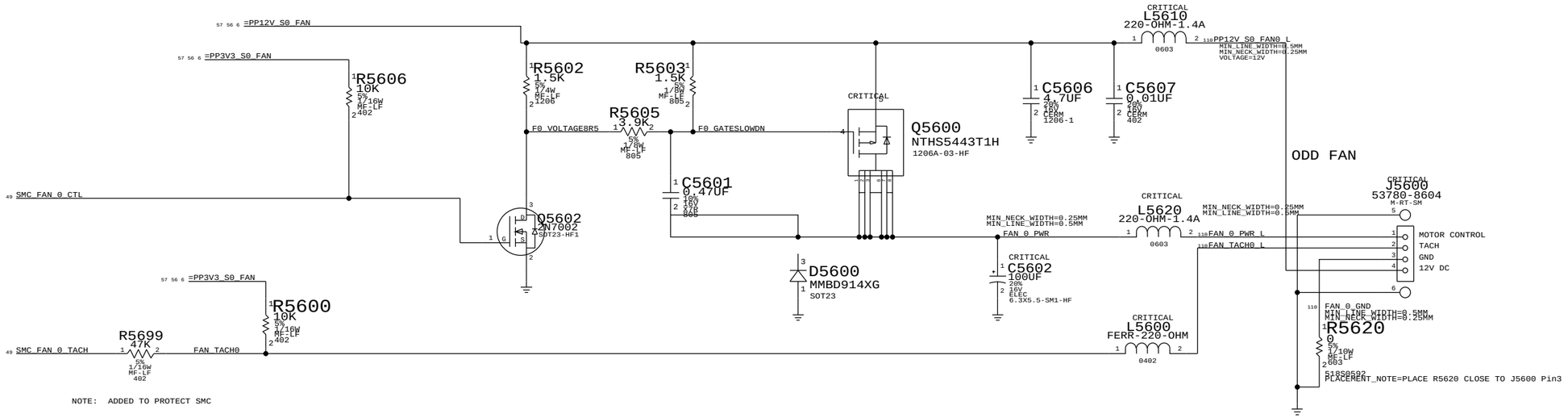
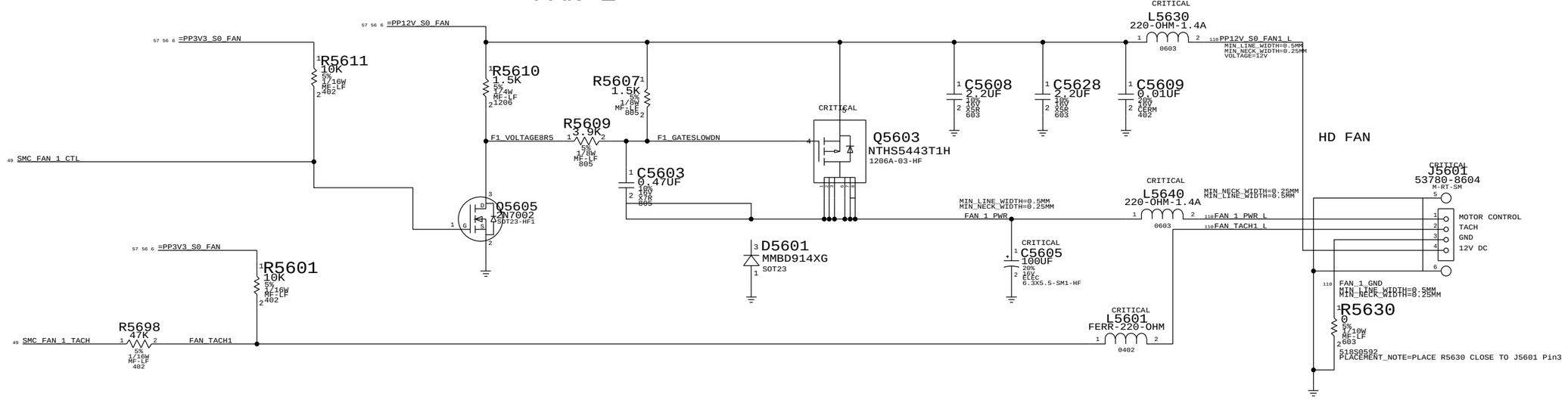
FAN 0



FAN 1



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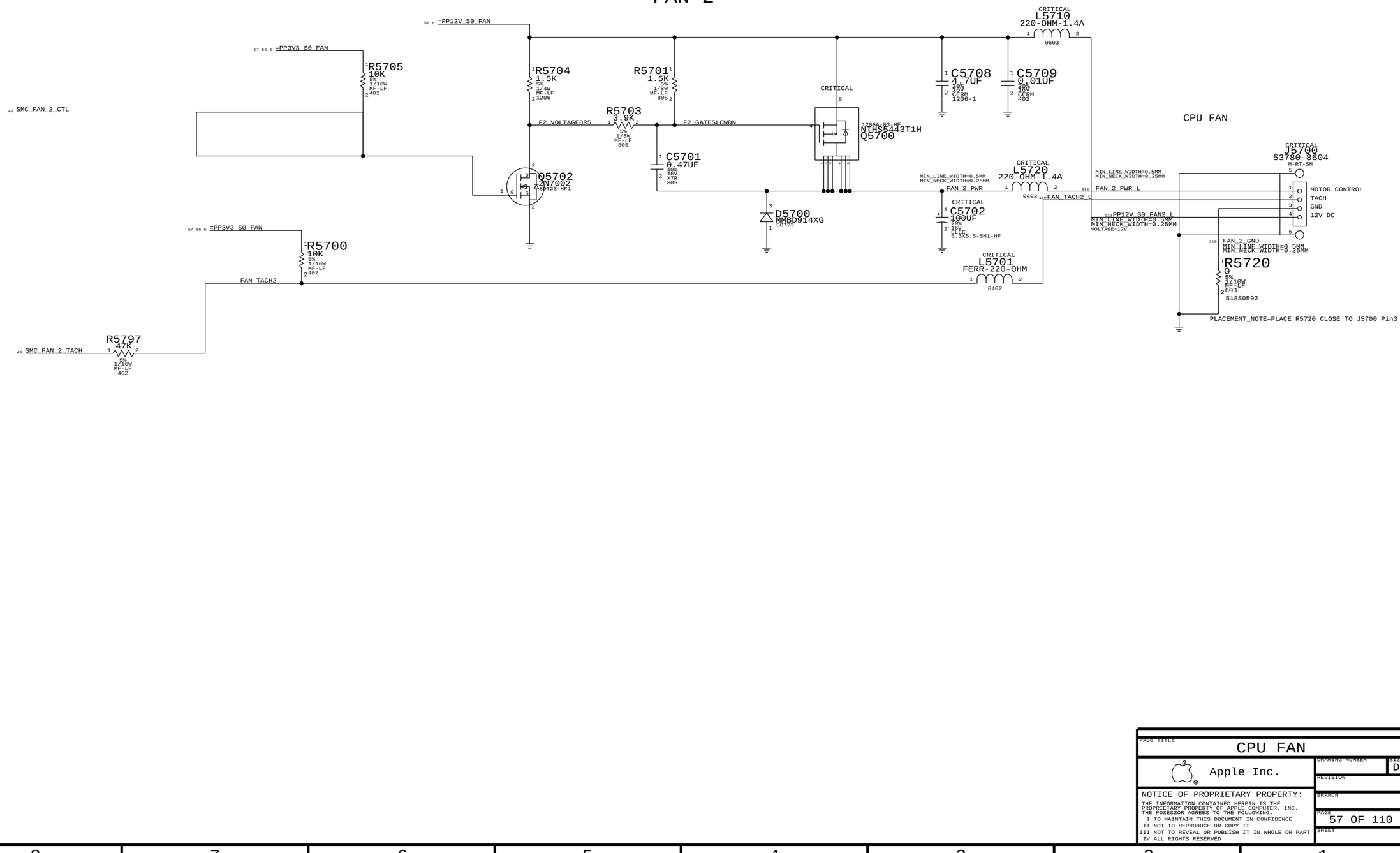
FAN 2



PAGE TITLE	CPU FAN
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8 7 6 5 4 3 2 1

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D C B A

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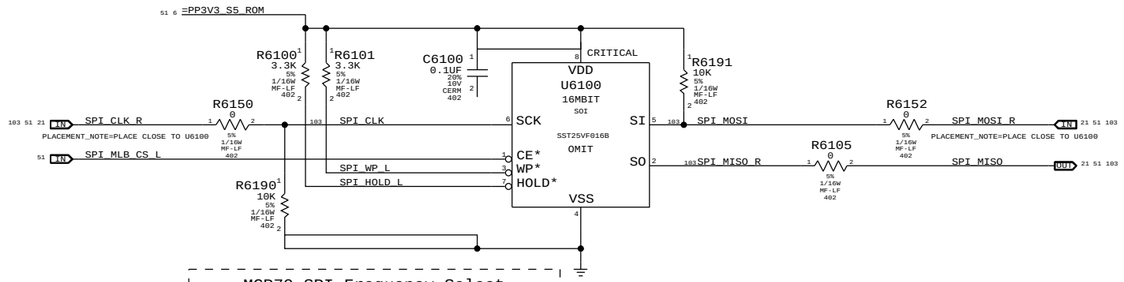

MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: MCP79 only issues ‘READ’ (0x03) commands not ‘READ_FAST’ (0x0B). Limits SPI bus frequency and part selection.

SST25VF016B max speed for READ command is 25MHz.

PAGE TITLE: SPI ROM

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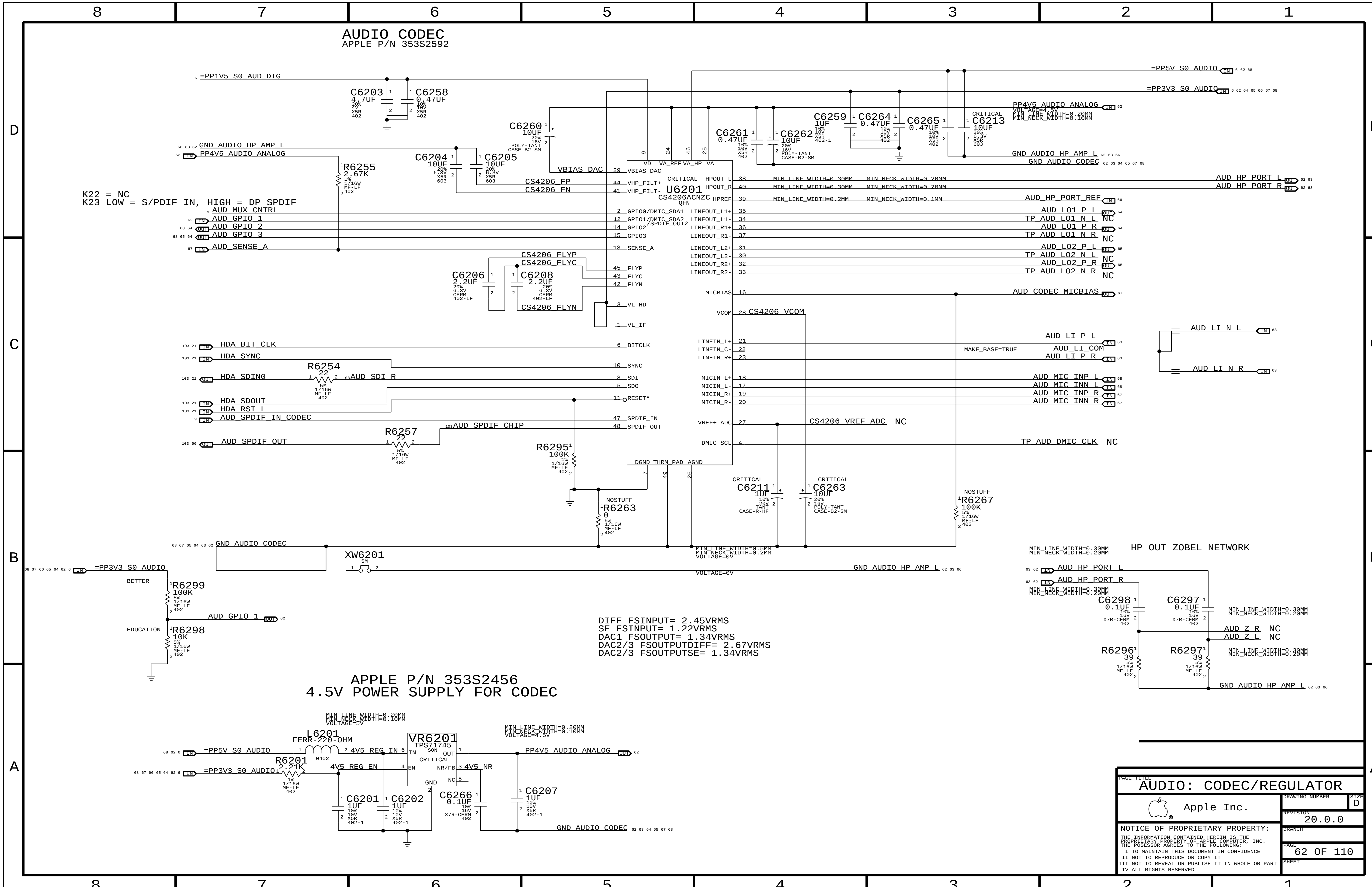

PAGE TITLE
AUDIO: CODEC/REGULATOR

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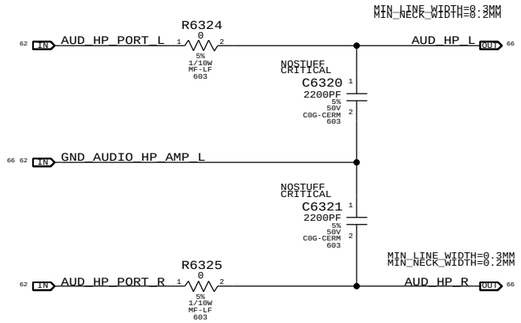
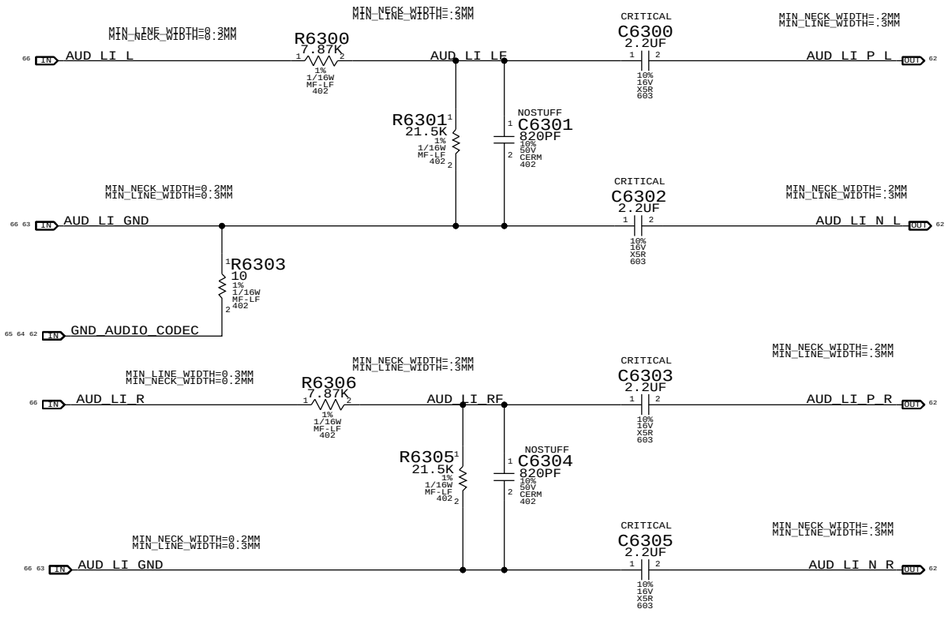
1ST ORDER DAC FILTER PLACEHOLDER



CODEC Nom SE RIN = 20K OHMS
FC = 5 HZ Max
VIN = 2VRMS, CODEC VIN = 1.14 VRMS
NET RIN = 18K OHMS



PAGE TITLE
AUDIO: FILTER/BUFFER

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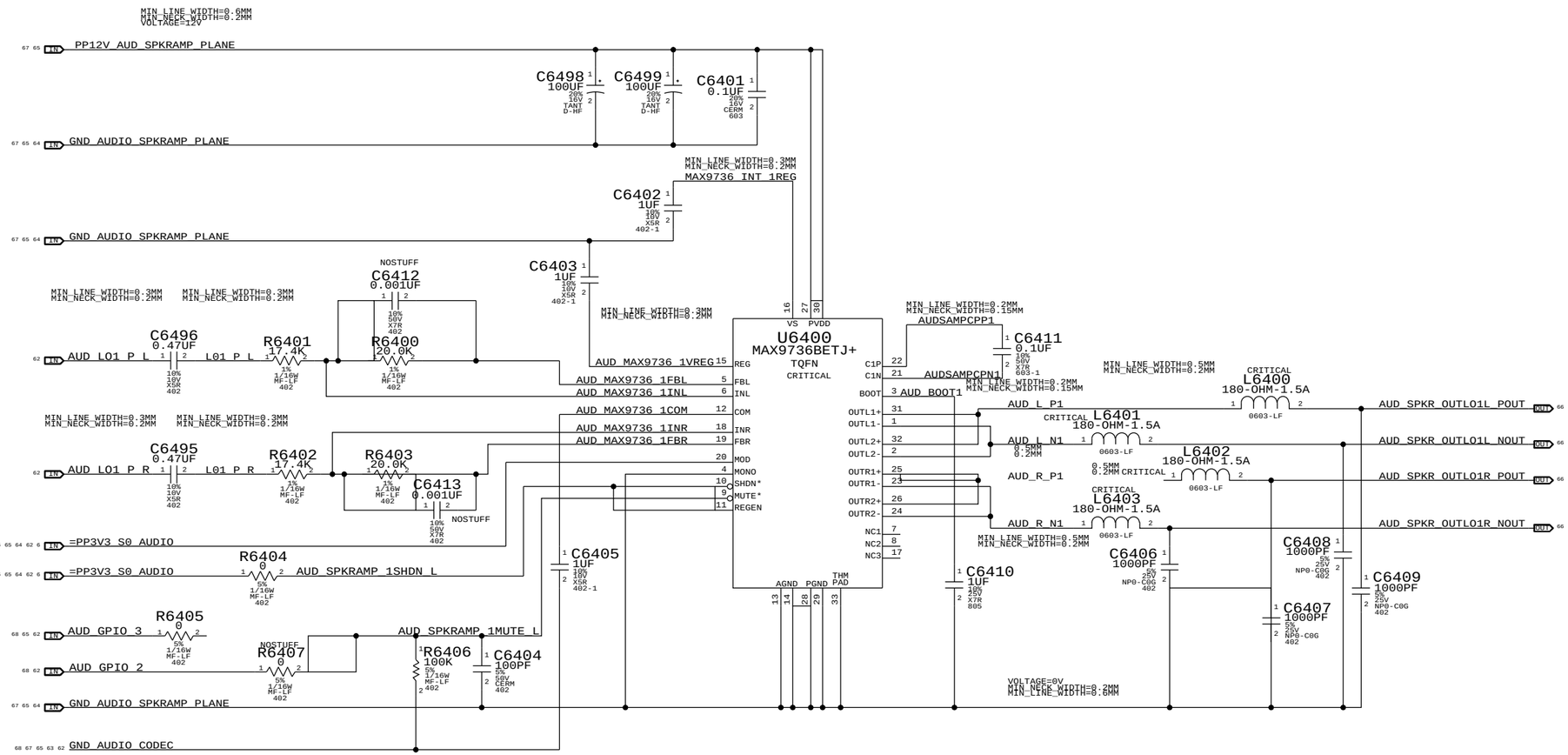
TWEETER SPEAKER AMPLIFIER

MAX9736B APN:353S2042

GAIN = -4.8(20K/17.4K)
CODEC OUT = 1.335VRMS
AMP VOUT = 7.355VRMS

TURN ON TIME: 110MS
TURN ON DELAY: 150MS
RIN = 17.4 OHMS
FC = 19.5 HZ

POUT = 6.76 W INTO 8 OHMS @ 1% THD+N



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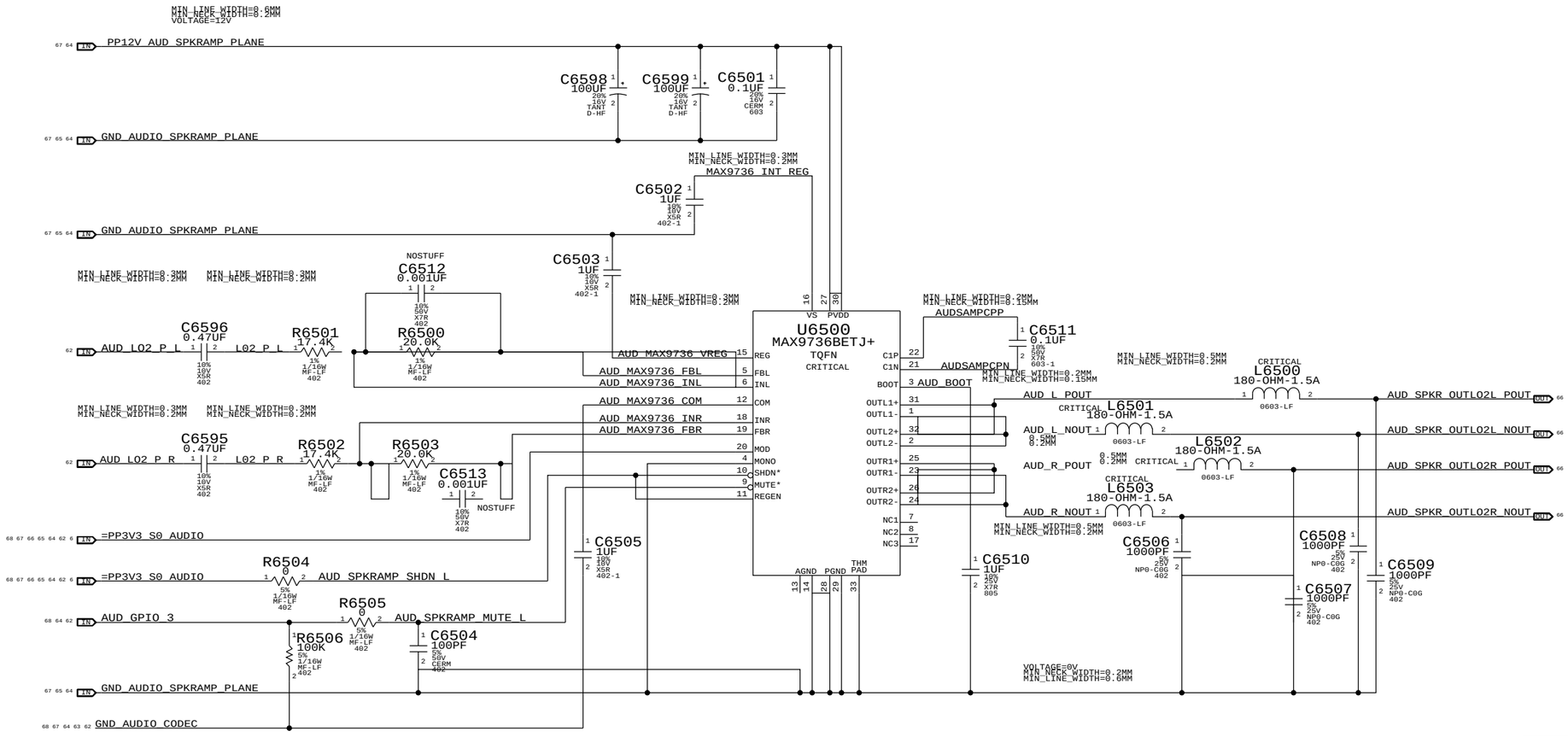
WOOFER SPEAKER AMPLIFIER

MAX9736B APN:353S2042

GAIN = -4.8(20K/17.4K)
CODEC OUT = 1.335VRMS
AMP VOUT = 7.355VRMS
POUT = 6.76 W INTO 8 OHMS @ 1% THD+N

TURN ON TIME: 110MS
TURN ON DELAY: 150MS
RIN = 17.4 OHMS
FC = 19.5 HZ



PAGE TITLE: AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER
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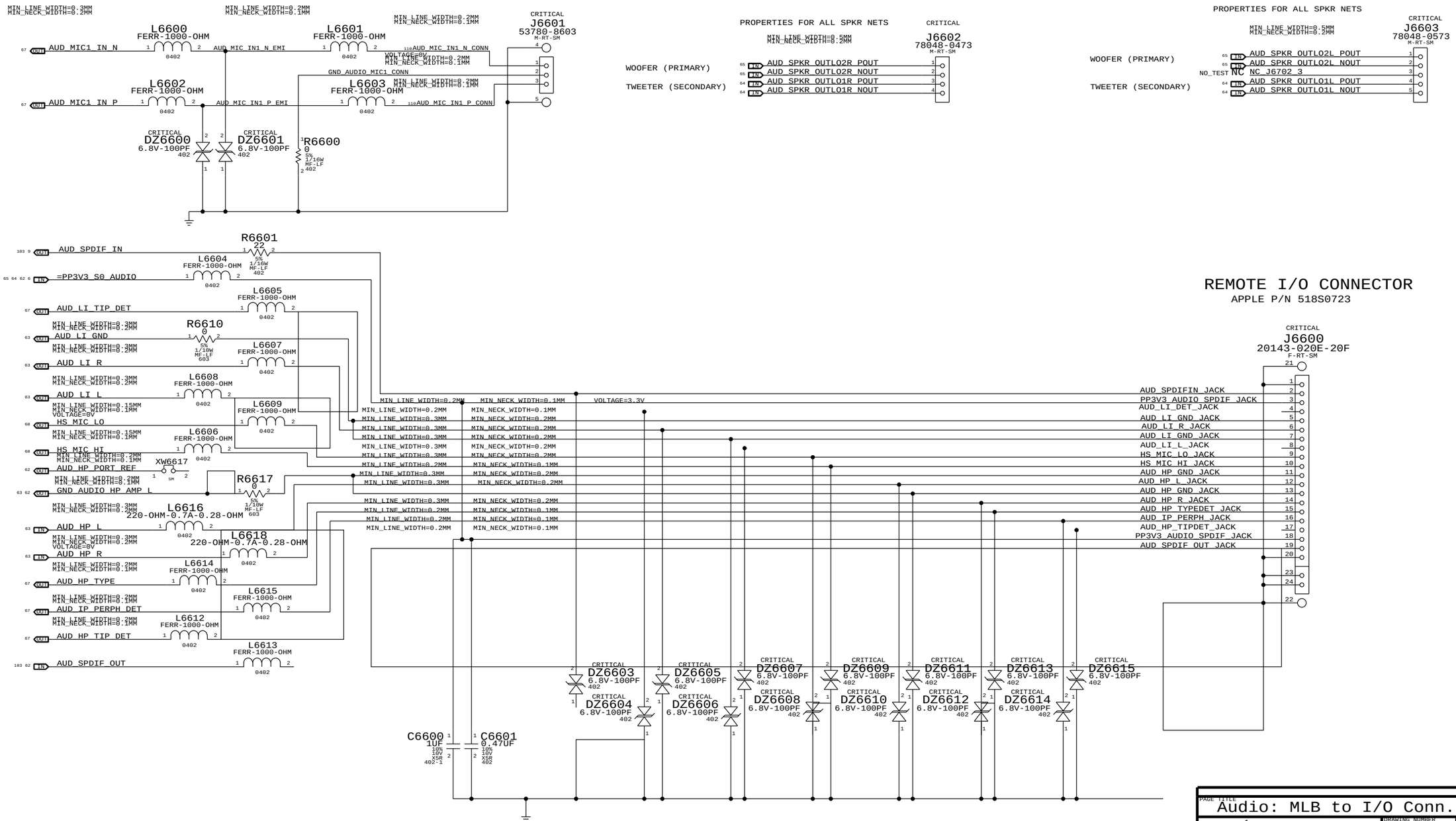
INTERNAL MIC CON
APPLE P/N 518S0677

SPEAKER CABLE CONNECTORS
APPLE P/N 518S0748
APPLE P/N 518S0656



REMOTE I/O CONNECTOR
APPLE P/N 518S0723

PAGE TITLE
Audio: MLB to I/O Conn.

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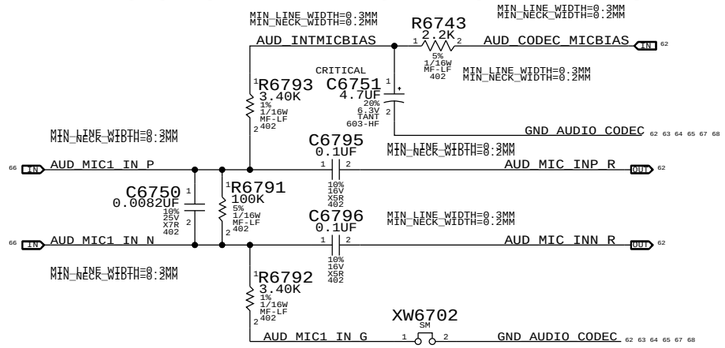
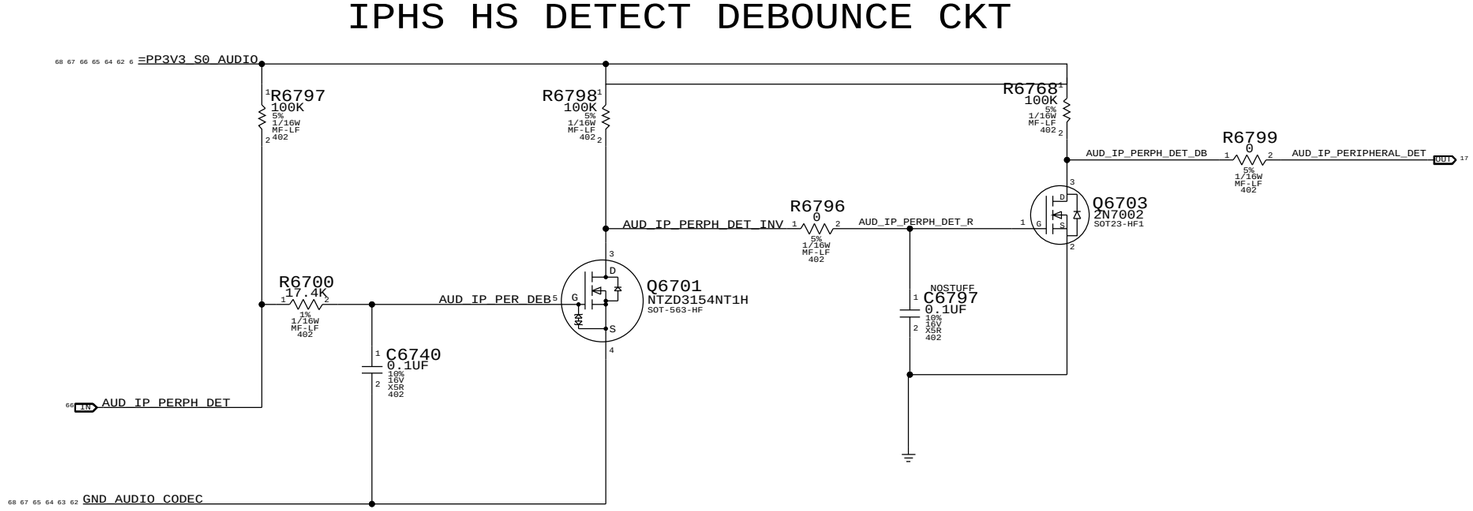
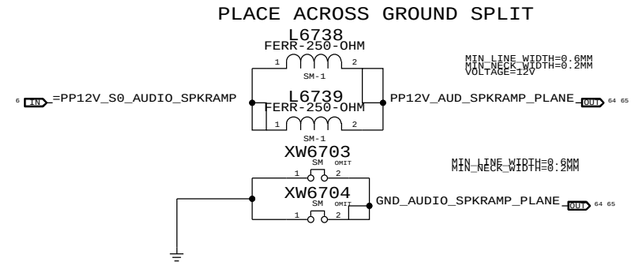
MICROPHONE IMPEDANCE MATCHING CIRCUIT



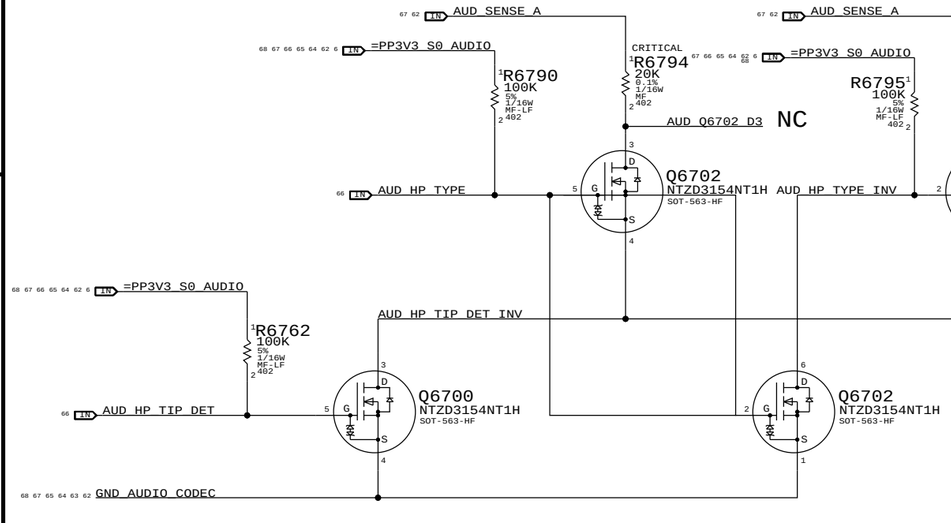
IPHS HS DETECT DEBOUNCE CKT



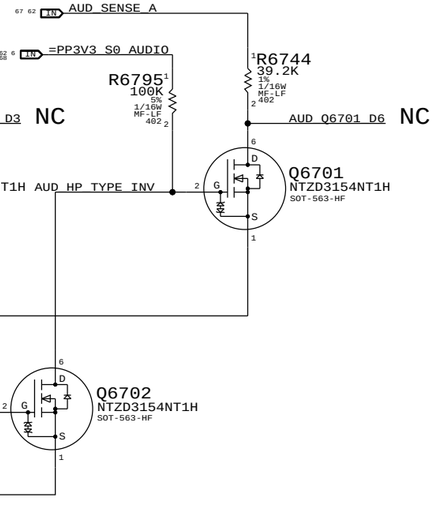
PLACE ACROSS GROUND SPLIT



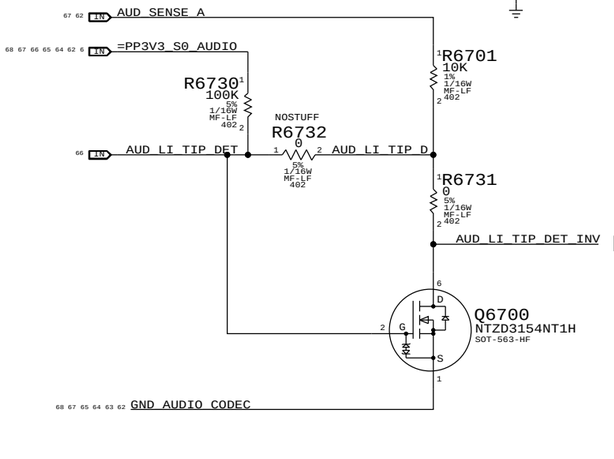
DIGITAL OUT



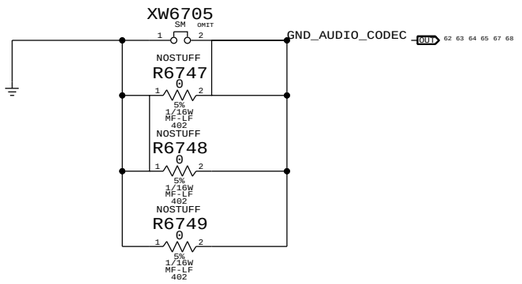
HEADPHONE OUT



LI INSERT DETECT



AUDIO GROUND RETURNS



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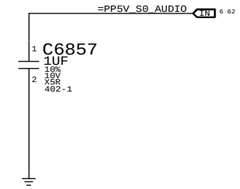
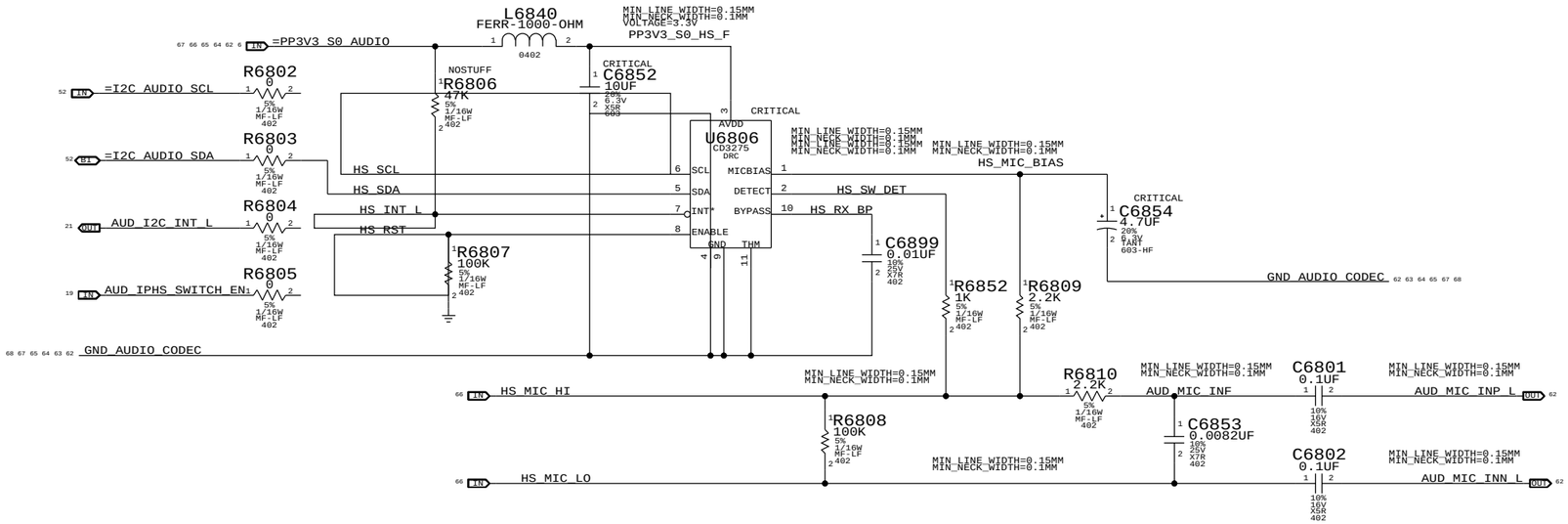
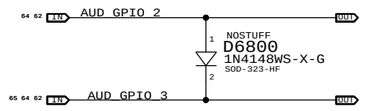
FUNCTION	PIN	CONVERTER	VOLUME	ENABLE/ CNTRL TYPE	DETECT/INTERRUPT
PRIMARY	0X0B	0X04	0X04	GPIO 3	N/A
SECONDARY	0X0A	0X03	0X03	GPIO 3	N/A
HEADPHONES	0X09	0X02	0X02	N/A	0X09 (A)
LINE INPUT	0X0C	0X05	0X05	N/A	LINE IN
BUILT-IN MICROPHONE	0X0D(13,B,RIGHT)	0X06	0X06	MICBIAS 80%	N/A
HEADSET MICROPHONE	0X0D (13,V22,B,LEFT)	0X06	0X06	MIKEY	MIKEY
SPDIF OUT	0X10	0X08	N/A	N/A	0X0C (B)
SPDIF IN	0X0F	0X07	N/A	N/A	N/A
MIKEY	N/A	N/A	N/A	MCP GPIO_38	MCP GPIO_5



MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2256





FLP = 8.82 KHZ
FHP = 80 HZ

PAGE TITLE: AUDIO: Mikey

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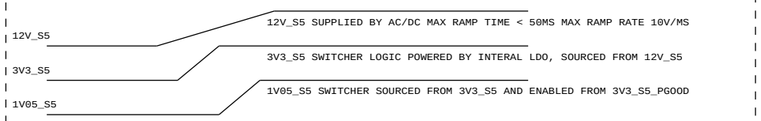
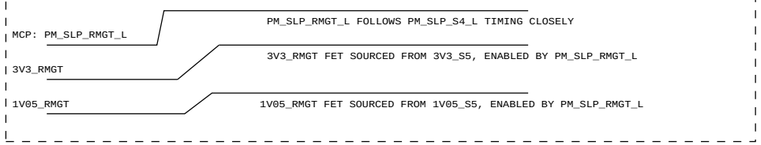
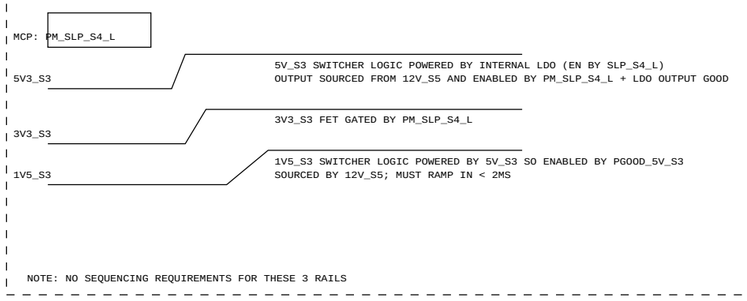
S5 POWER RAIL SEQUENCING



RMGT POWER RAIL SEQUENCING

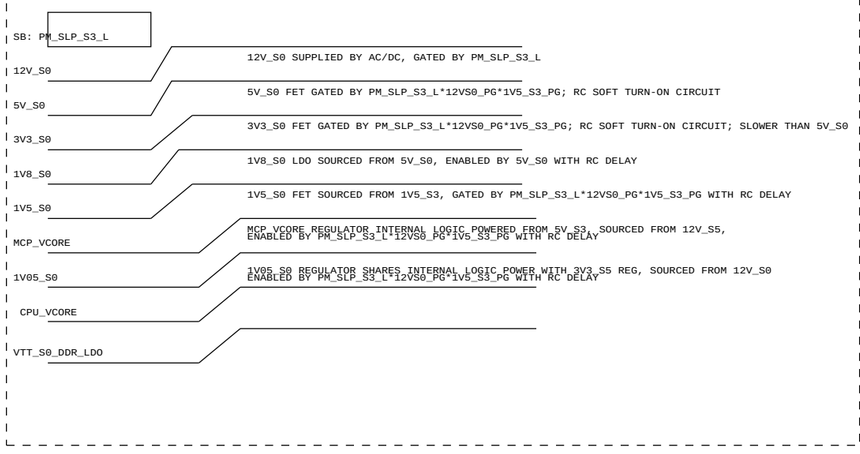


S3 POWER RAIL SEQUENCING

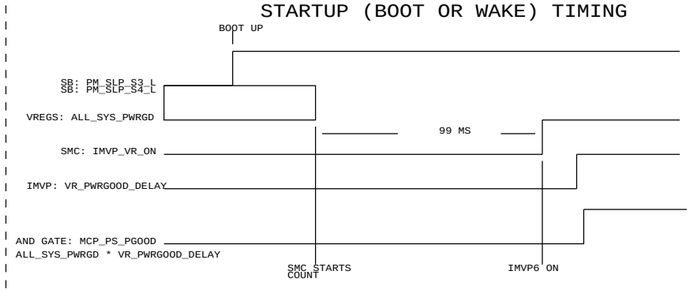


NOTE: NO SEQUENCING REQUIREMENTS FOR THESE 3 RAILS

S0 POWER RAIL SEQUENCING

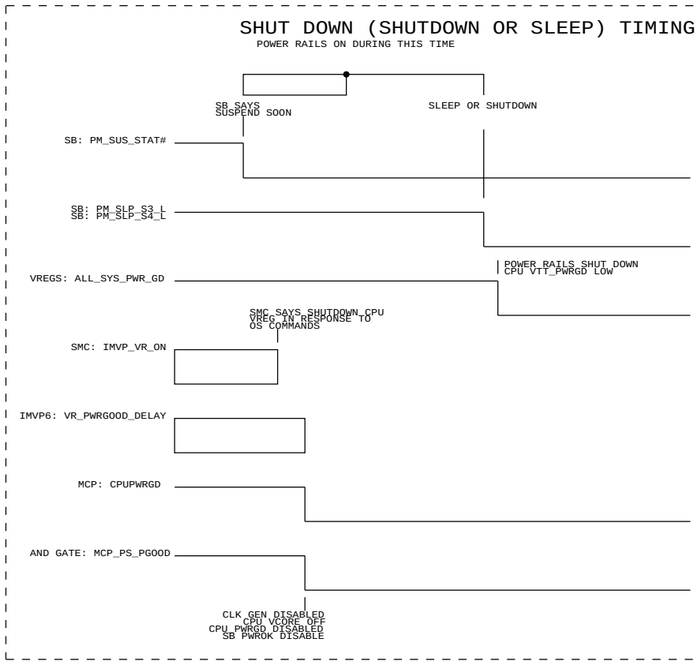


STARTUP (BOOT OR WAKE) TIMING



State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

SHUT DOWN (SHUTDOWN OR SLEEP) TIMING



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POWER SEQUENCING BLOCK DIAGRAM

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Power Control Signals
3.3V,5V S3 enable

State	SMC_PM_G2_ENABLE (PORTABLES)	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

FROM MCP (6)
PM_SLP_RMGT_L → R7050 0 → ENET_EN (OUT 38)
PM_SLP_S4_L (PM_S4_STATE_L)
NOSTUFF R7051 33 — PLACEMENT_NOTE=Place close to U1400
R7052 33 → P3V3S3_EN (OUT 78) — Enable FET — PLACEMENT_NOTE=Place close to U1400
R7053 33 → 5VREG_EN (OUT 73) — ENABLE REGULATOR — PLACEMENT_NOTE=Place close to U1400
R7054 33 → PM_SLP_S4_SMC_L (OUT 49 50) — To SMC — PLACEMENT_NOTE=Place close to U1400

=PP5V_S3_PWRCTL (6) → R7072 100K → PGOOD_5V_S3 (70) MAKE_BASE=TRUE → =DDRREG_EN (OUT 75) — Enable regulator

PGOOD_5V_S3 (IN 70) → PM_EN_USB_PWR (OUT 46) — USB Port Switch

MXM POWER SEQUENCE

=PM_MXM_PGOOD_PULLUP (IN 85) → ALL_SYS_PWRGD_R (6 70) MAKE_BASE=TRUE → PM_MXM_EN (OUT 85)

MXM CARD INPUT POWER ARE 12V_S0, 3V3_S0, 5V_S0
ALL_SYS_PWRGD ENABLES MXM REGULATORS
PM_MXM_PGOOD IS OPEN DRAIN SIGNAL, IT'S PULLED UP TO ALL_SYS_PWRGD

=PP3V3_S5_PWRCTL (70 6) → C7058 0.1UF
R7040 10K
FROM COMPARATOR PGOOD_1V5_S3 (78)
FROM COMPARATOR PGOOD_12V_S0 (78) → S0_RDY MAKE_BASE=TRUE
U7059 TC7SZ08AFEAPE SOT665
PM_SLPS3_BUF2_L (IN 50 49 9 6) ← From SMC (6)
PM_SLP_S3_L (PM_SLP_S3_L_BUF)
PM_SLP_S3_L_AND_S0_RDY → R7085 33 — PLACEMENT_NOTE=Place close to U7059 → P5VS0_EN MAKE_BASE=TRUE → =P5VS0_EN (OUT 78) — Enable FET

R7080 30K (5% 1/16W MF-LF 402)
R7081 43K (5% 1/16W MF-LF 402)
R7082 10K (5% 1/16W MF-LF 402)
R7083 2.2K (5% 1/16W MF-LF 402)
C7080 0.47UF (10% 6.3V CERM-X5R 402)
C7081 0.47UF (10% 6.3V CERM-X5R 402)
C7082 0.47UF (10% 6.3V CERM-X5R 402)
C7083 0.47UF (10% 6.3V CERM-X5R 402)

P3V3S0_EN MAKE_BASE=TRUE → =P3V3S0_EN (OUT 78) — Enable FET
MCPDDR_EN MAKE_BASE=TRUE → =MCPDDR_EN (OUT 78) — Enable FET DELAY OF ~15MS FROM PM_SLP_S3_L
CPUVTTS0_EN MAKE_BASE=TRUE → =PVTT_S0_EN (OUT 76) — Enable regulator DELAY OF ~18MS FROM PM_SLP_S3_L
MCPCORES0_EN MAKE_BASE=TRUE → =MCPCORES0_EN (OUT 74) — Enable regulator DELAY OF ~16MS FROM PM_SLP_S3_L

1.5V_S3 NEED TO BE ON BEFORE S0 FET ON
12V_S0 NEED TO BE ON BEFORE MCP REG AND 1.05_S0 REG EN

=PP3V3_S5_PWRCTL (6 70) → R7031 1K (5% 1/16W MF-LF 402)
PGOOD_1V1_S5 (79) 1V05V_S0 DERIVES FROM 3.3V_S5
RSMRST_PWRGD (OUT 49) — To SMC (2)
C7031 0.1UF (10% 16V X5R 402)
FROM THIS SMC GENERATES PM_RSMRST_L WHICH GOES INTO PGOOD_S8 OF MCP
DELAY IS ABOUT 200MS

PGOOD Comparators

HYSTERESIS NUMBERS CALCULATED BASED ON OUPTPUT PULL UP OF 3.3V

=PP12V_S5_PWRCTL (78 38 6)
R7013 33.2K (1% 1/16W MF-LF 402)
R7018 84.5K (1% 1/16W MF-LF 402)
C7010 0.1UF (20% 16V CERM 603)
R7014 100K (1% 1/16W MF-LF 402)
R7019 10K (1% 1/16W MF-LF 402)
PLACE SHORTS CLOSE TO PLANE CUTS

PP12V_S0 (6) → XW7000 OMIT (SM) → R7000 4.99K (1% 1/16W MF-LF 402) → 12VS0_PG_CMP1
(9.91V/9.58V; 330MV HYSTERESIS)
=PPDDR_S3_PGCMP (6) → XW7001 OMIT (SM) → R7001 1.21K (1% 1/16W MF-LF 402) → 1V5S3_PG_CMP
(1.30V/1.22V; 80MV HYSTERESIS)

U7010 LM393 SOI-HF (CRITICAL)
12VS5_9V00_REF
12VS0_COMP_REF
12VS5_1V27_REF
1V5S3_COMP_REF
R7007 49.9K (1% 1/16W MF-LF 402)
R7008 49.9K (1% 1/16W MF-LF 402)
PGOOD_12V_S0 (OUT 70)
PGOOD_1V5_S3 (OUT 70)

USING COMPARTOR INSTEAD OF REGULATOR PGOOD OUTPUT BECAUSE IF 5V S3 DOES NOT COME UP, PPDDR REGULATOR HAS NO INTERNAL POWER TO PULL PGOOD LOW

(PULLUPS ARE NEAR LOADS)

=PP12V_S0_VRD (71 6)
MXM R7022 100K (5% 1/16W MF-LF 402)
R7020 64.9K (1% 1/16W MF-LF 402)
(1.67V/1.53V; 132MV HYSTERESIS)
12VS5_1V60_REF (55)
U7030 LM393 SOI-HF (CRITICAL)
R7006 49.9K (1% 1/16W MF-LF 402)
C7025 0.1UF (10% 16V CERM 603)
=PP1V8_S0_PGCMP (6) → XW7002 OMIT (SM) → R7002 2.0K (IG) (1% 1/16W MF-LF 402) → 1V8S0_PG_CMP
1V8S0_COMP_REF
R7021 10K (1% 1/16W MF-LF 402)
PGOOD_1V8_S0 (OUT 70)

S0 RAILS PGOOD

=PP3V3_S5_PWRCTL (70 6) → R7033 10K (1% 1/16W MF-LF 402)
PGOOD_1V8_S0 (70) (IN)
PGOOD_1V5_S0 (78) (IN)
PGOOD_5V_S0 (78) (IN)
=PP3V3_S0_PWRCTL (6) → R7030 10K (1% 1/16W MF-LF 402)
PGOOD_MCPCORE_S0 (74) (IN)
PGOOD_1V05_S0 (78) (IN)
S0_PWR_CMP_PGOOD MAKE_BASE=TRUE
S0_PWR_REG_PGOOD MAKE_BASE=TRUE
U7020 TC7SZ08AFEAPE SOT665
ALL_SYS_PWRGD

=PP3V3_S5_PWRCTL (6 70) → C7020 0.1UF (10% 16V CERM 402)

PLACE RESISTORS CLOSE TO U7020
R7098 33 (5% 1/16W MF-LF 402) → ALL_SYS_PWRGD_SMC (OUT 49)
R7099 33 (5% 1/16W MF-LF 402) → ALL_SYS_PWRGD_R (OUT 6 70)

	I	Rds(on)	Vgs +/-
IRF7410	13A	7mOHM	8V
IRF7413	9.6A	18mOHM	20V
FDS4435	8.8A	35mOHM	25V
IRF7406	5.8A	70mOHM	20V
IRF6402	3.7A	65mOHM	12V
SI2302	1.6A	115mOHM	8V

=PP3V3_S5_PWRCTL (70 6) → C7056 0.1uF (20% 10V CERM 402)
PM_MXM_PGOOD (85) (IN)
PM_PGOOD_PVCORE_CPU (71 11) (IN)
U7056 MC74VHC1G08 SOT23-5-HF → MCP_PS_PWRGD (OUT 21)

ALL_SYS_PWRGD IS ALSO AN INPUT TO THIS AND GATE BY THE EARLY TRAY
PM_MXM_PGOOD IS PULLED UP TO IT

PAGE TITLE
PGOOD and Power Sequencing

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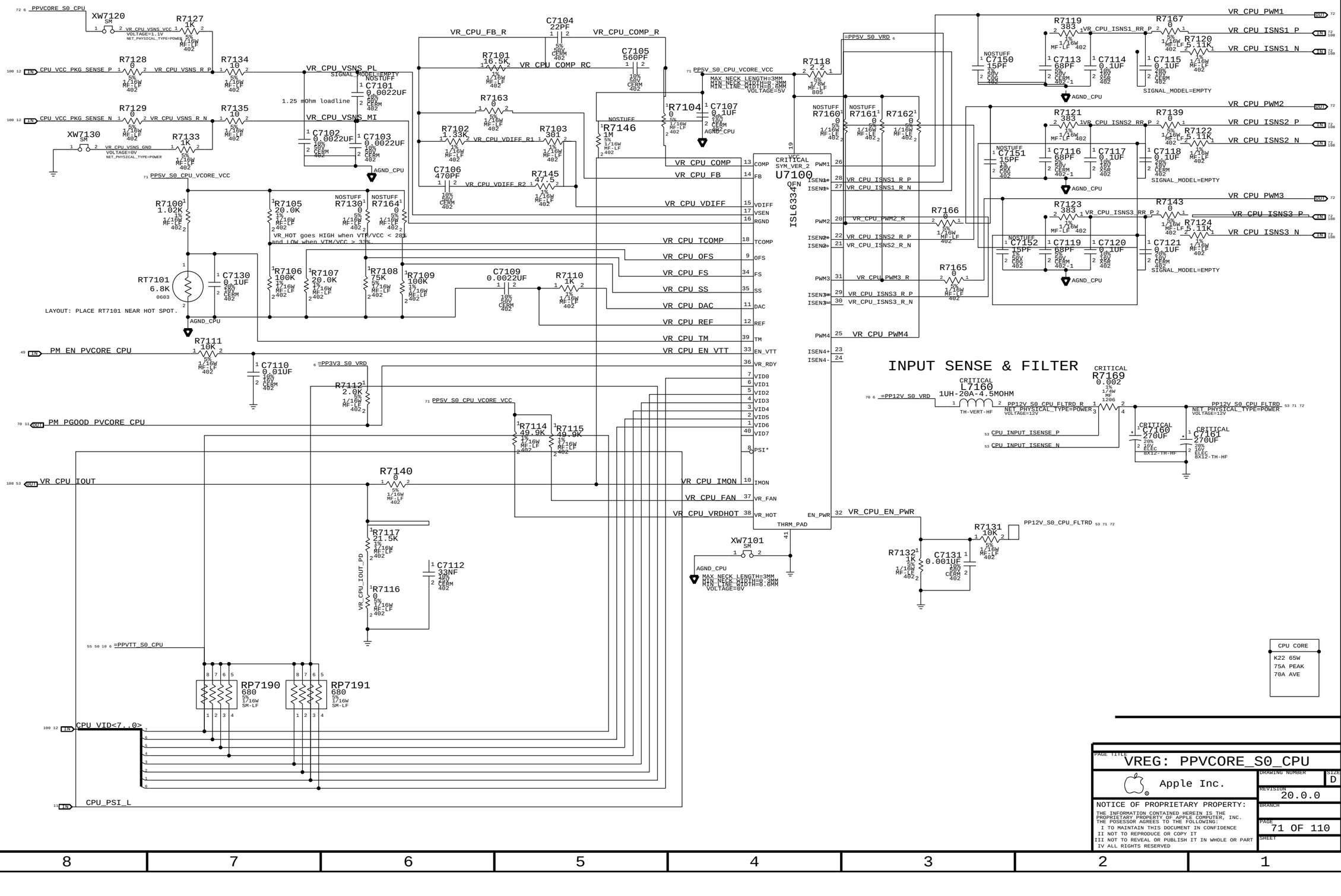

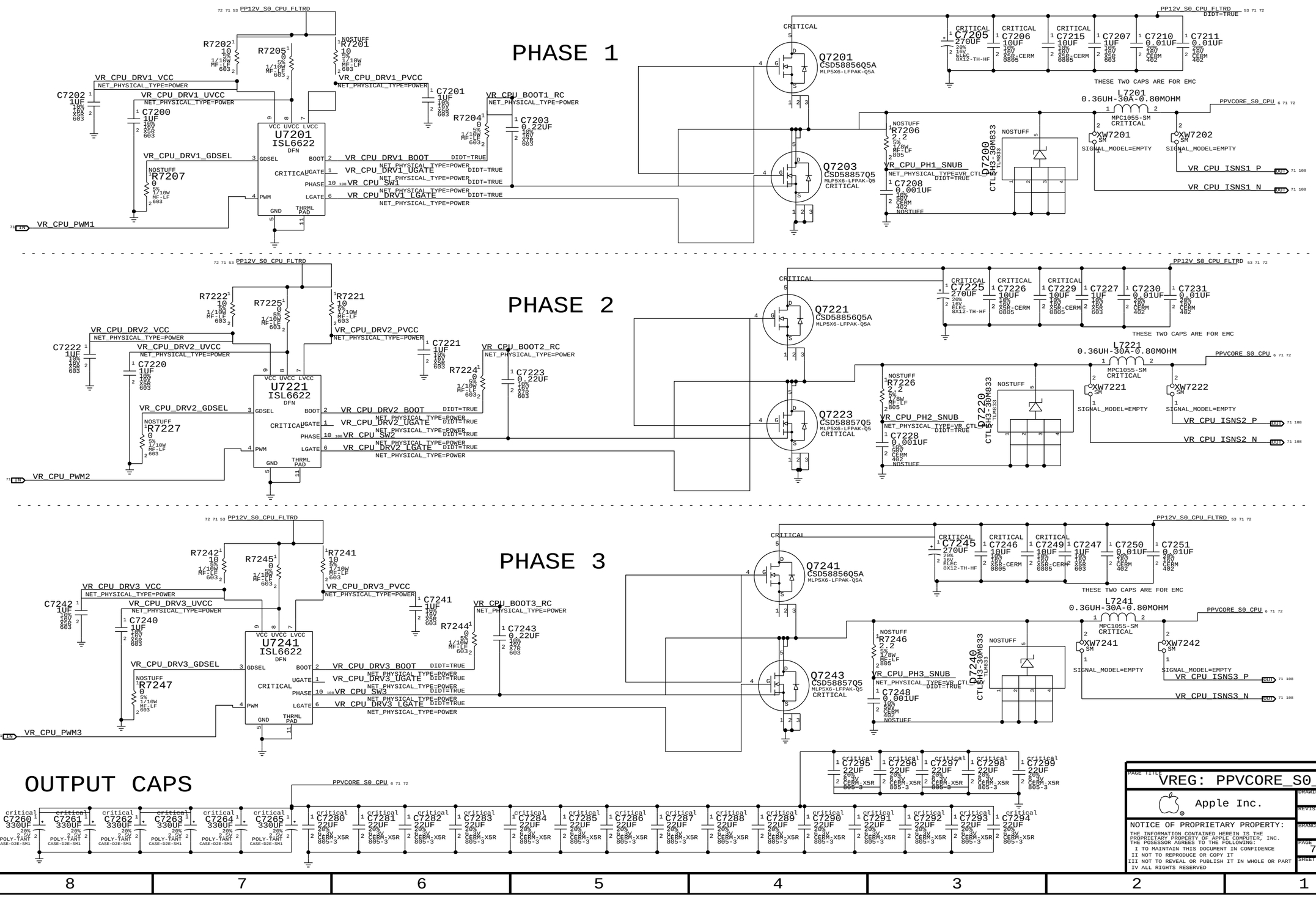

PAGE TITLE: VREG: PPVCORE_S0_CPU

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5V S3 REGULATOR

=PPVIN_S5_P5VS3 6 73
DIDT=TRUE
CRITICAL
C7342 270UF 20% 16V ELEC 8X12-TH-HF
C7300 10UF 10% 16V X5R-CERM 0805
C7335 10UF 10% 16V X5R-CERM 0805
C7332 10UF 10% 16V X5R-CERM 0805
EMC: C7353,C7354 PLACE AT Q7330
C7354 0.1UF 10% 25V X5R 402
C7353 0.1UF 10% 25V X5R 402
=PPVIN_S5_P5VS3 6 73
C7345 2.2UF 10% 16V X5R 603
C7334 4.7UF 10% 35V X5R-CERM 0805
D7301 B0530WXG SOD-123-HF
CRITICAL
Q7330 CSD58856Q5A MLP5X6-LFPAK-Q5A
5VS3_TG MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE
5VS3_SW MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE
INTVCC VIN
U7300 LTC3851EUD QFN
CRITICAL
OSCILLATED AT APPR. 330KHZ
LTCINTVCC 73
5VS3_FREQ
5VREG_EN
5VS3_TK_SS
SOFT START TIME 8MS
5VS3_ITH
LTCMODE 73
THRM GND PAD
ILIM
FREQ/PLLFLTR
RUN
TK/SS
ITH
MODE/PLLIN
TG 13
SW 14
BOOST 12
BG 9
SENSE+ 6
SENSE- 5
FB 4
5VS3_BG MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE
5VS3_SENSEP
5V_BOOT1 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE
5V_BOOT1_R
R7324 0 5% 1/10W MF-LF 603
C7326 0.1UF 10% 25V X5R 402
SWITCHNODE
CRITICAL
Q7335 CSD58856Q5A MLP5X6-LFPAK-Q5A
5VS3_SENSEN
C7315 100PF 5% 50V CERM 402
R7304 0 5% 1/10W MF-LF 402
PLACE_XW_CLOSE_TO_L7320
OMIT
XW7300
NOSTUFF
C7363 0.0022UF 10% 50V CERM 402
5V_SNUBBER MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.4MM DIDT=TRUE
R7336 1.5K 1% 1/10W MF-LF 402
R7362 0.499 1% 1/10W MF 603
NOSTUFF
5VS3_SENSE
CRITICAL
L7320 2.2UH-10A-11.6M-OHM SM
CRITICAL
D7300 CTLSH3-30M833 TLM833
PLACE_XW_CLOSE_TO_L7320
XW7301 SM OMIT (5VS3_VOUT)
EMC: C7304,C7356 PLACE AT L7320.1
C7356 0.1UF 10% 25V X5R 402
C7304 0.1UF 10% 25V X5R 402
5V_S3 K507K51 POWER BUDGET PEAK=8.86A AVE=7.3A
PP5V_S3_REG 6 110
RA
R7305 43.2K 1% 1/10W MF-LF 402
C7309 100PF 5% 50V CERM 402
RB
R7306 8.06K 1% 1/10W MF-LF 402
C7301 10UF 20% 6.3V CERM 805-1
CRITICAL
C7302 330UF 20% 6.3V POLY-TANT CASE-D3L-SM
CRITICAL
C7305 330UF 20% 6.3V POLY-TANT CASE-D3L-SM
C7322 10UF 20% 6.3V CERM 805-1
C7306 0.001UF 10% 50V CERM 402
C7307 100PF 5% 50V CERM 402
5VS3_ITH_R
R7302 24.9K 1% 1/16W MF-LF 402
C7325 20PF 5% 50V CERM 402
5VS3_FB
C7317 0.22UF 10% 10V CERM 402
R7307 1.24K 1% 1/10W MF-LF 402
5VS3_SENSEN_R
(5VS3_FB)

STATE	PM_SLP3_BUF1_L	5VREG_PS_L	LTCMODE	Mode
S0	1	0	1	CONT MODE
S3	0	1	0	BURST MODE

LTCINTVCC 73
R7311 100K 5% 1/10W MF-LF 402
Q7303 SI2301BDS SM-HF CRITICAL
5VREG_PS_L
R7312 100K 5% 1/10W MF-LF 402
R7310 10K 5% 1/16W MF-LF 402
94 9 PM_SLPS3_BUF1_L
PM_SLPS3_BUF1_R_L
Q7360 MMBT3904G SOT23
LTCMODE 73

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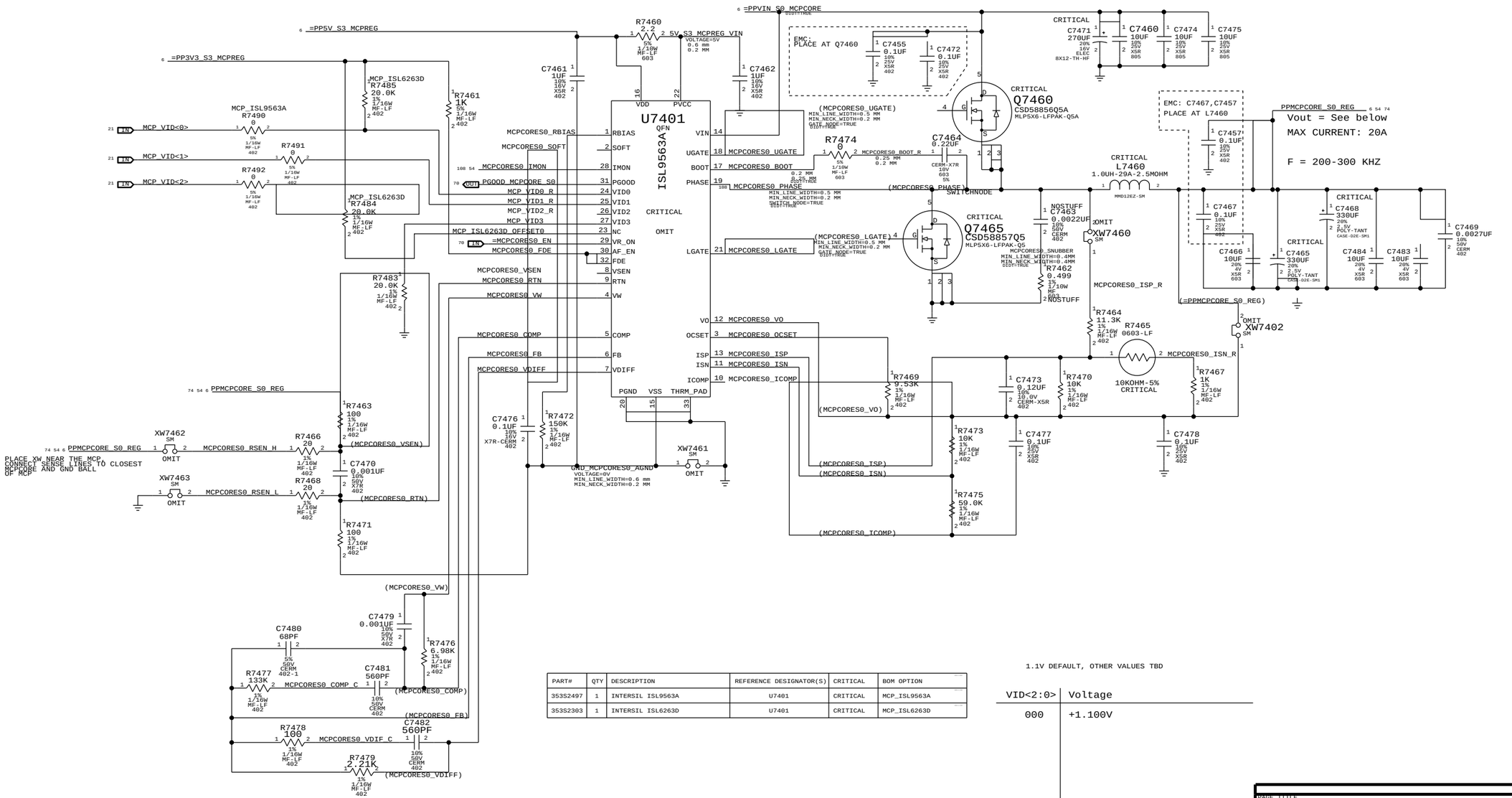
MCP CORE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S2497	1	INTERSIL ISL9563A	U7401	CRITICAL	MCP_ISL9563A
353S2303	1	INTERSIL ISL6263D	U7401	CRITICAL	MCP_ISL6263D

1.1V DEFAULT, OTHER VALUES TBD

VID<2:0>	Voltage
000	+1.100V

PAGE TITLE: MCP CORE REGULATOR

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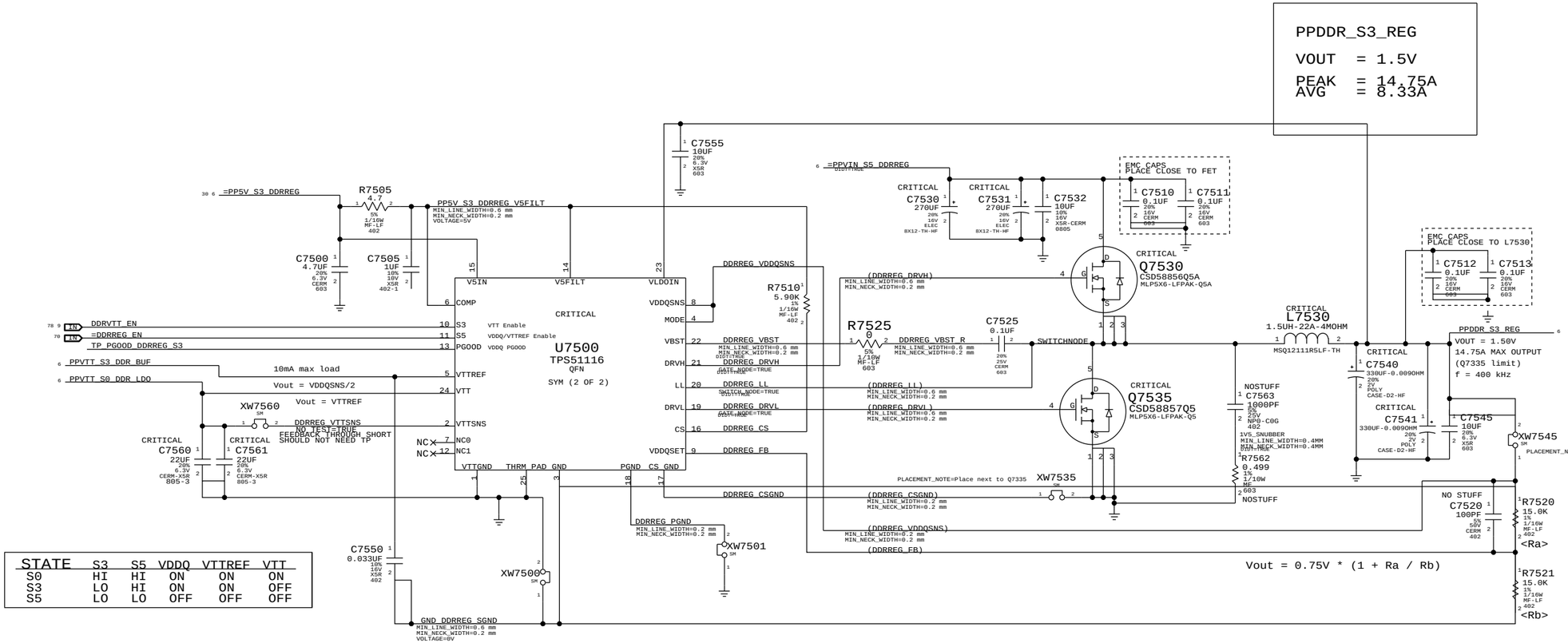
1.5 V DDR SUPPLY

PPDDR_S3_REG
VOUT = 1.5V
PEAK = 14.75A
AVG = 8.33A



STATE	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON
S3	LO	HI	ON	ON	OFF
S5	LO	LO	OFF	OFF	OFF

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FSB VTT AND 3.3V S5 RAILS

INPUT POWER OF 12V_S0

INPUT POWER OF 12V_S5

Vout = 1.212V for Wolfdale
6.7A MAX OUTPUT
(R7614 LIMIT)
f = 200 kHz

Vout = 0.7V * (1 + Ra / Rb)

VTT_FSB_S0
K22/K23
POWER BUDGET
PEAK=5.3A
AVE=2.9A

SEL A3V3 S5
K507/K51
POWER BUDGET
K50 PEAK=4.94A
K50 AVE=2.18A

SELECTS SWITCHING FREQUENCY

EN_LDO TIED TO 12V_S5 TO EN LDO FIRST & REGULATOR INTERNAL LOGIC GETS POWER
EN2 (3V3_S5) IS TIED TO VCC, TIED INTERNALLY TO PVCC
TIED EXTERNALLY TO LDO OUT. SO REGULATOR IS ENABLED
AS SOON AS LDO OUTPUT IS GOOD

EN1 (PPVTT_S0) CONTROLLED SEPARATELY

PAGE TITLE: FSB VTT/3.3V S5 SUPPLIES

Apple Inc.

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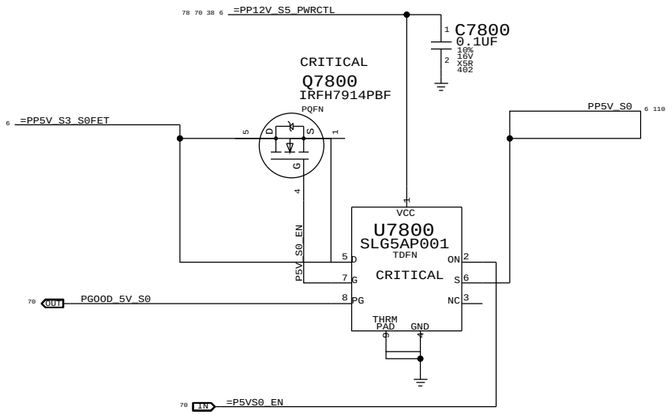
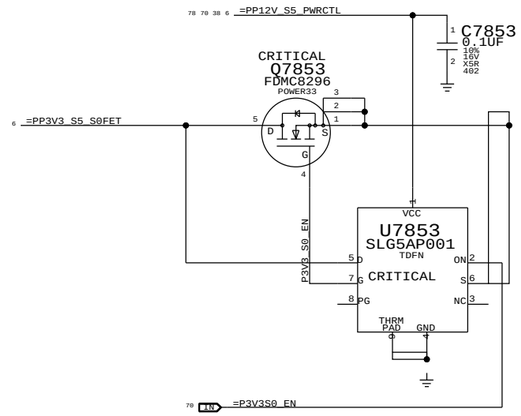
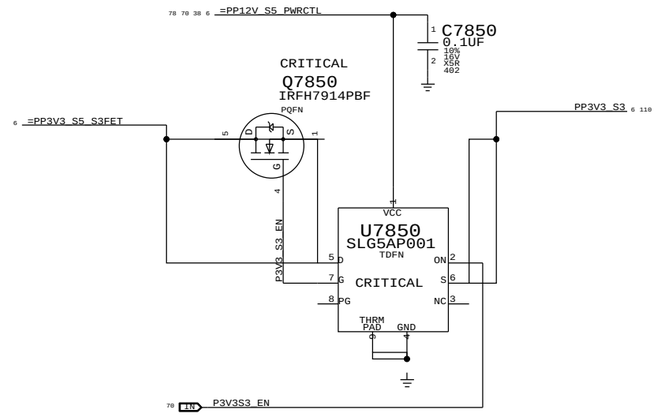
5V S0 FET



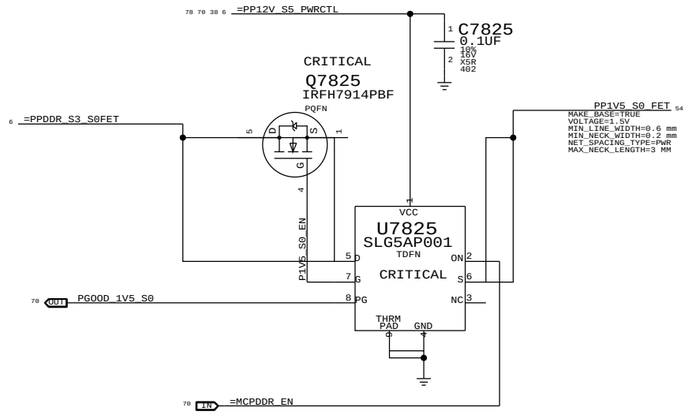
3.3V S0 FET



3.3V S3 FET

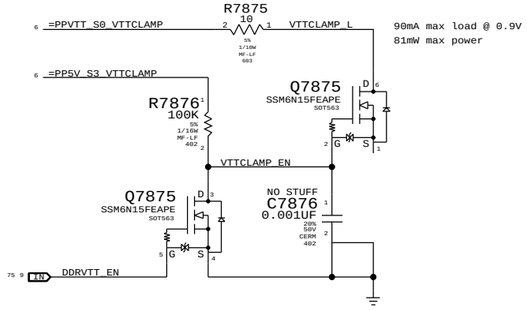


1.5V S0 FET



MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT
NVIDIA RECOMMENDS UNPOWERING DURING SLEEP.
IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE
MUST GUARANTEE MEM_CKE SIGNALS ARE LOW
BEFORE RAIL IS TURNED OFF, AND REMAINS LOW
UNTIL AFTER RAIL TURNS BACK ON OR DIMMS
WILL EXIT SELF-REFRESH PREMATURELY.
MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP
ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS
LOW THROUGH VTT TERMINATION RESISTORS.



PAGE TITLE	S3 & S0 FETs
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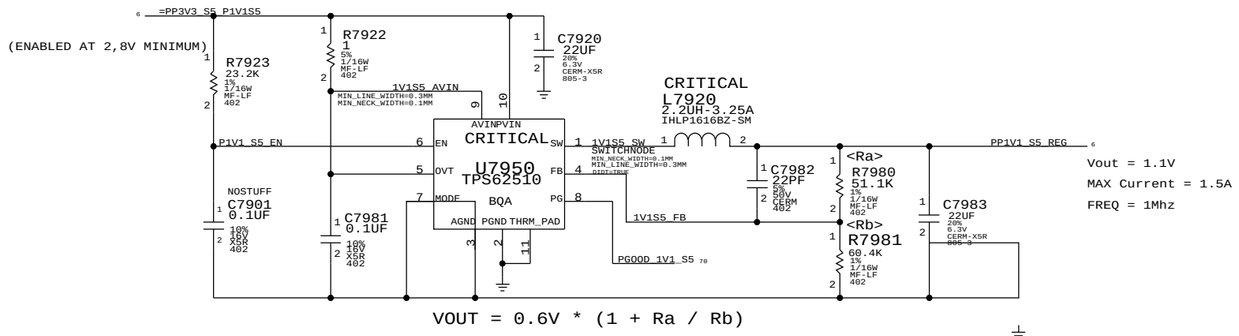
MCP 1.1V_S5 AUXC SUPPLY



PAGE TITLE	1V1 S5 POWER SUPPLY
Apple Inc.	DRAWING NUMBER / SIZE D
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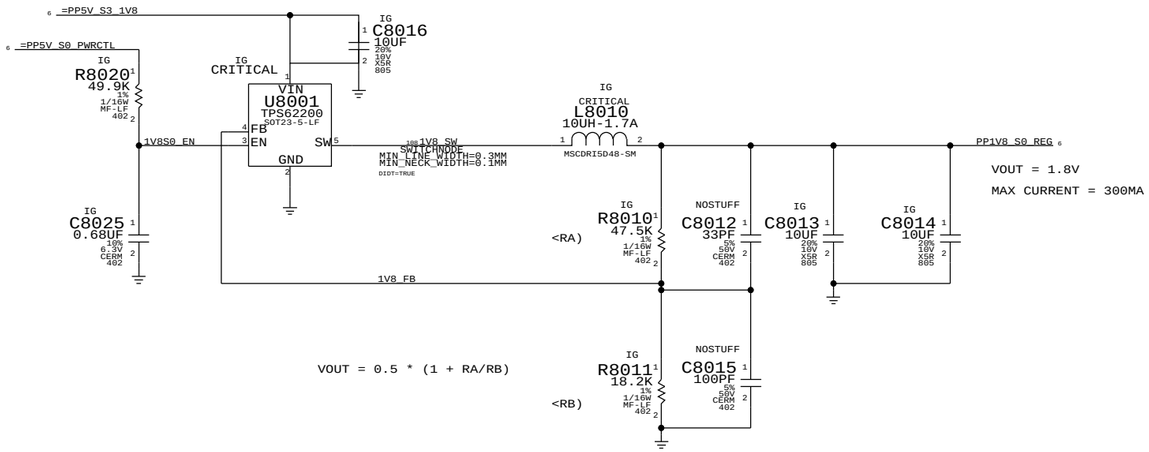
MCP ONLY 1.8V_S0 POWER SUPPLY



PAGE TITLE	1V8 POWER SUPPLY
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8 7 6 5 4 3 2 1

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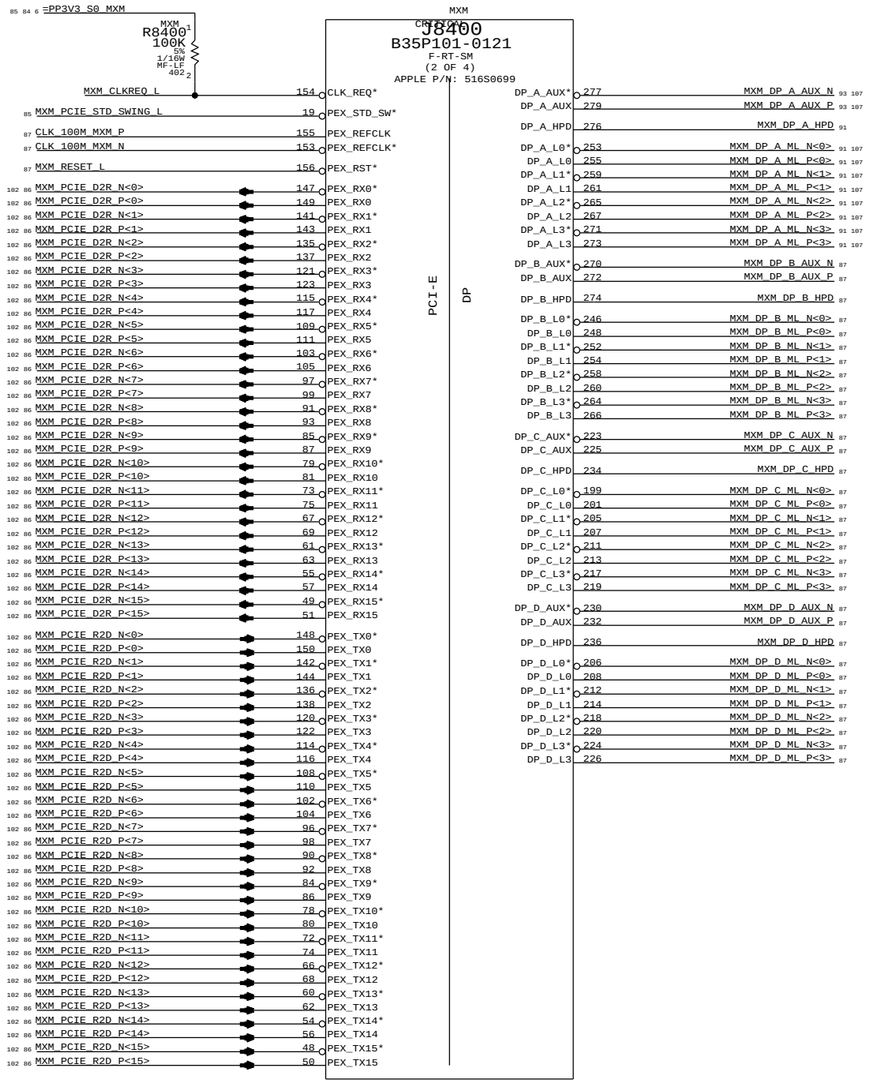
Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP5V_S0_MXM
- =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- MXM



MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.0 A	3.3 W
5V	2.5 A	12.5 W
PWR (7-20V)	UP TO 10 A	PLATFORM DEPENDENT

PAGE TITLE: MXM PCIe, DP & Power

Apple Inc.

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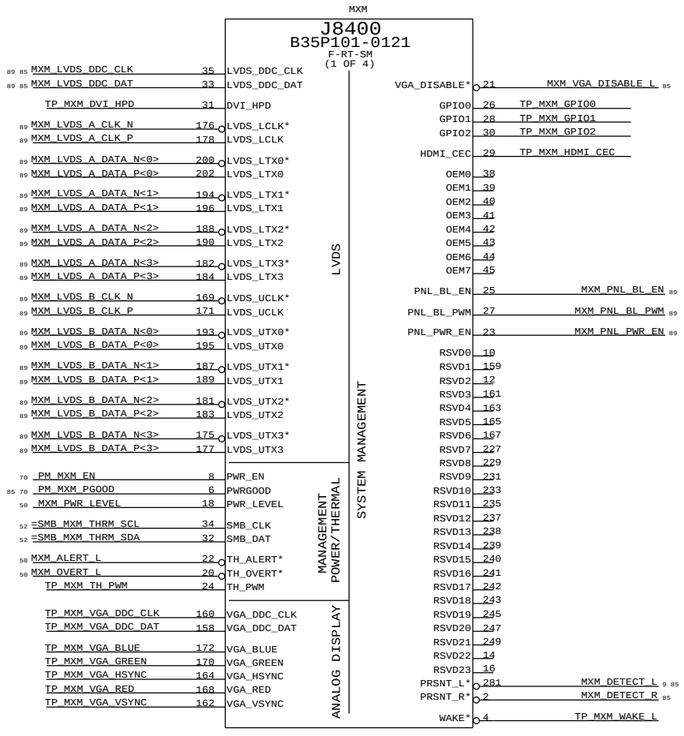
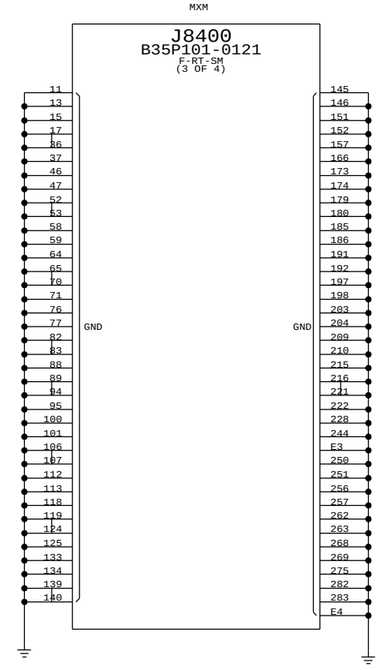
Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM

Signal aliases required by this page:
- =SMB_MXM_THRM_DATA
- =SMB_MXM_THRM_CLK
- =PM_MXM_PGOOD_PULLUP

BOM options provided by this page:





PULLUPS & PULLDOWNS AT MXM CONNECTOR

FLOAT = NORMAL VGA MODE
GND = SECONDARY DISPLAY CARD

R8510 0 NOSTUFF
MXM_VGA_DISABLE_L
MF-LF 5% 1/16W 402

FLOAT = LOW SWING
GND = HIGH SWING

R8504 0 NOSTUFF
MXM_PCIE_STD_SWING_L
MF-LF 5% 1/16W 402

=PP3V3_S0_MXM

R8500 100K
MXM_DETECT_L
MF-LF 5% 1/16W 402

PULLED TO GROUND ON MXM
WE DON'T USE CARD DETECT

R8501 100K
MXM_DETECT_R
MF-LF 5% 1/16W 402

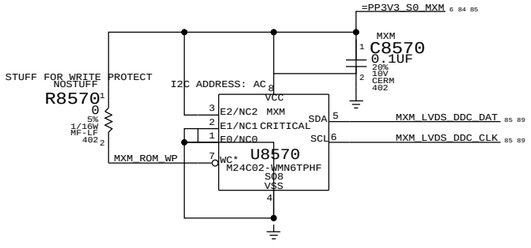
=PM_MXM_PGOOD_PULLUP

SYSTEM INTEGRATOR MUST ALIAS THIS EITHER TO A VOLTAGE RAIL,
OR ANOTHER OPEN-DRAIN PGOOD SIGNAL DEPENDING ON DESIRED BEHAVIOR

R8503 10K
PM_MXM_PGOOD
MF-LF 5% 1/16W 402

MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J7800



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MXM TX CAPS

102 9	IN	PEG_R2D_C_N<0>	MXM	C8600	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<15>	OUT	84 102
102 9	IN	PEG_R2D_C_P<0>	MXM	C8601	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<15>	OUT	84 102
102 9	IN	PEG_R2D_C_P<1>	MXM	C8602	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<14>	OUT	84 102
102 9	IN	PEG_R2D_C_N<1>	MXM	C8603	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<14>	OUT	84 102
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102 9	IN	PEG_R2D_C_N<3>	MXM	C8606	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<12>	OUT	84 102
102 9	IN	PEG_R2D_C_P<3>	MXM	C8607	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<12>	OUT	84 102
102 9	IN	PEG_R2D_C_N<4>	MXM	C8608	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<11>	OUT	84 102
102 9	IN	PEG_R2D_C_P<4>	MXM	C8609	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<11>	OUT	84 102
102 9	IN	PEG_R2D_C_N<5>	MXM	C8610	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<10>	OUT	84 102
102 9	IN	PEG_R2D_C_P<5>	MXM	C8611	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<10>	OUT	84 102
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102 9	IN	PEG_R2D_C_P<6>	MXM	C8613	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<9>	OUT	84 102
102 9	IN	PEG_R2D_C_N<7>	MXM	C8614	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<8>	OUT	84 102
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MXM RX CAPS

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102 84	IN	MXM_PCIE_D2R_N<15>	MXM	C8633	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<0>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_P<14>	MXM	C8634	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<1>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_N<14>	MXM	C8635	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<1>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_P<13>	MXM	C8636	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<2>	OUT	9 102
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102 84	IN	MXM_PCIE_D2R_P<12>	MXM	C8638	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<3>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_N<12>	MXM	C8639	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<3>	OUT	9 102
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102 84	IN	MXM_PCIE_D2R_P<7>	MXM	C8648	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<8>	OUT	9 102
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102 84	IN	MXM_PCIE_D2R_N<5>	MXM	C8653	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<10>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_P<4>	MXM	C8654	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<11>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_N<4>	MXM	C8655	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<11>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_P<3>	MXM	C8656	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<12>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_N<3>	MXM	C8657	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<12>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_P<2>	MXM	C8658	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<13>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_N<2>	MXM	C8659	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<13>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_P<1>	MXM	C8662	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<14>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_N<1>	MXM	C8663	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<14>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_P<0>	MXM	C8660	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<15>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_N<0>	MXM	C8661	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<15>	OUT	9 102

PAGE TITLE: MXM PCIE CAPS

Apple Inc.

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Page Notes

Power aliases required by this page:
- =PP5V_DP_AUX

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

MCP CONNECTIONS

84 CLK_100M_MXM_P — GPU_CLK100M_PCIE_P 9 102
MAKE_BASE=TRUE
84 CLK_100M_MXM_N — GPU_CLK100M_PCIE_N 9 102
MAKE_BASE=TRUE

84 MXM_RESET_L — PEG_RESET_L 9 90
MAKE_BASE=TRUE

UNUSED DP INTERFACES

84 MXM_DP_C_ML_N<0..3> — NC_MXM_DP_C_ML_N<0..3>
MAKE_BASE=TRUE
NO_TEST=TRUE
84 MXM_DP_C_ML_P<0..3> — NC_MXM_DP_C_ML_P<0..3>
MAKE_BASE=TRUE
NO_TEST=TRUE

84 MXM_DP_C_AUX_N — NC_MXM_DP_C_AUX_N
MAKE_BASE=TRUE
NO_TEST=TRUE
84 MXM_DP_C_AUX_P — NC_MXM_DP_C_AUX_P
MAKE_BASE=TRUE
NO_TEST=TRUE

84 MXM_DP_C_HPD — TP_MXM_DP_C_HPD
MAKE_BASE=TRUE

84 MXM_DP_B_ML_N<0..3> — NC_MXM_DP_B_ML_N<0..3>
MAKE_BASE=TRUE
NO_TEST=TRUE
84 MXM_DP_B_ML_P<0..3> — NC_MXM_DP_B_ML_P<0..3>
MAKE_BASE=TRUE
NO_TEST=TRUE

84 MXM_DP_B_AUX_N — NC_MXM_DP_B_AUX_N
MAKE_BASE=TRUE
NO_TEST=TRUE
84 MXM_DP_B_AUX_P — NC_MXM_DP_B_AUX_P
MAKE_BASE=TRUE
NO_TEST=TRUE

84 MXM_DP_B_HPD — TP_MXM_DP_B_HPD
MAKE_BASE=TRUE

84 MXM_DP_D_ML_N<0..3> — NC_MXM_DP_D_ML_N<0..3>
MAKE_BASE=TRUE
NO_TEST=TRUE
84 MXM_DP_D_ML_P<0..3> — NC_MXM_DP_D_ML_P<0..3>
MAKE_BASE=TRUE
NO_TEST=TRUE

84 MXM_DP_D_AUX_N — NC_MXM_DP_D_AUX_N
MAKE_BASE=TRUE
NO_TEST=TRUE
84 MXM_DP_D_AUX_P — NC_MXM_DP_D_AUX_P
MAKE_BASE=TRUE
NO_TEST=TRUE

84 MXM_DP_D_HPD — TP_MXM_DP_D_HPD
MAKE_BASE=TRUE

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MXM ALIASES

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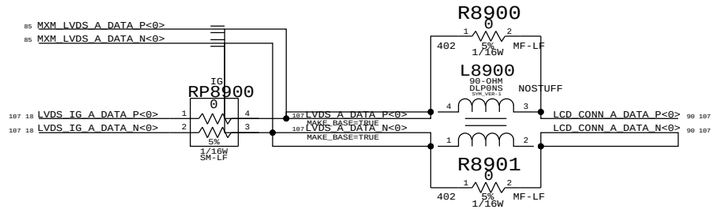
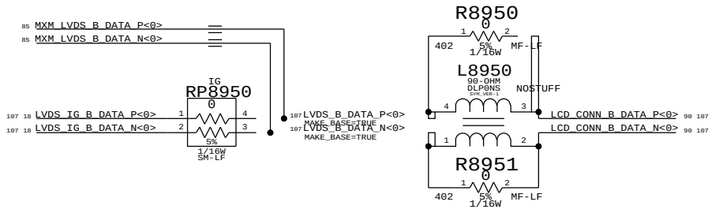
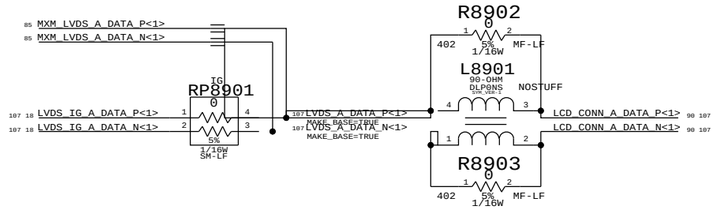
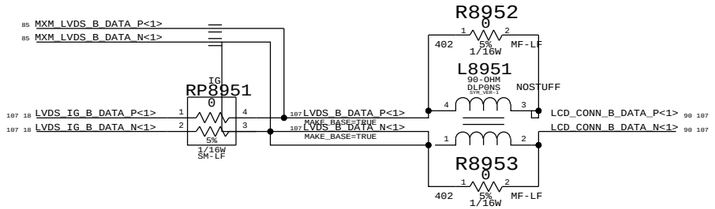
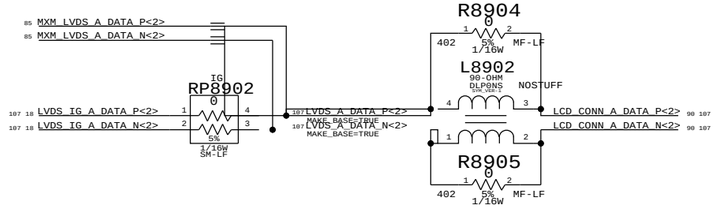
PLACE CHOKES CLOSE TO J9002
SHARE 0-OHM RES WITH CHOKE PADS

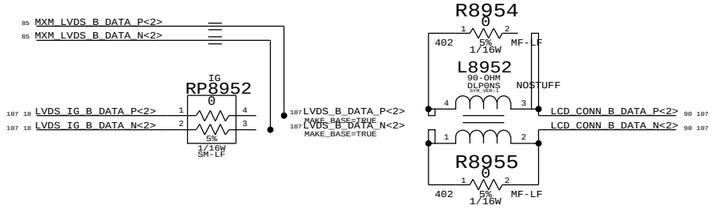


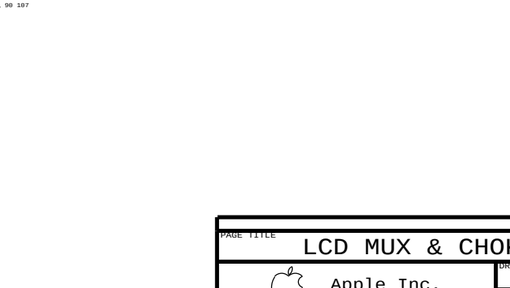


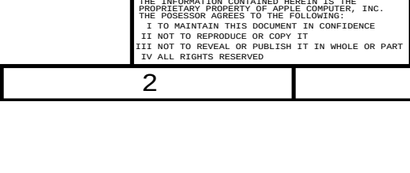


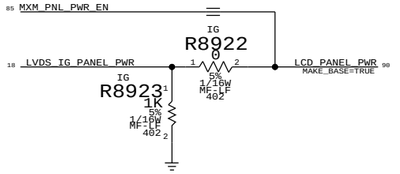


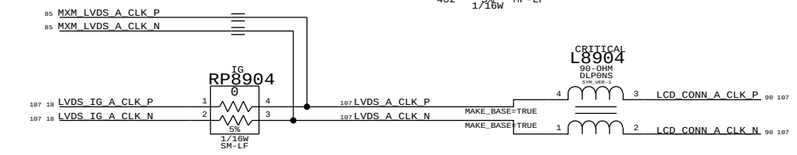


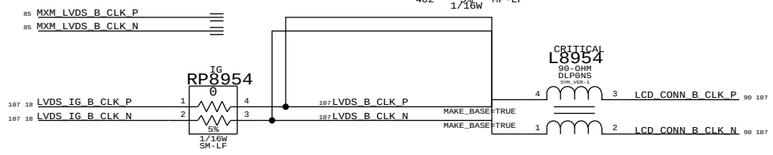


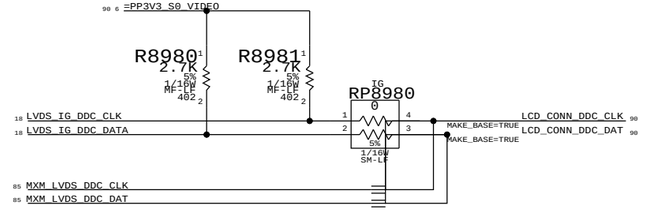












IN MXM CONFIG, PULL-UPS ON CARD
IG pullups always stuffed to prevent floating inputs

THESE RESISTOR OPTIONS SELECT BETWEEN MCP AND MXM TO DRIVE THE INTERNAL DISPLAY

IG-ONLY O-OHM RESISTORS NEED TO BE PLACED AT THE MXM CONNECTOR TO AVOID STUBS
WE WILL ROUTE FROM MCP TO THE 0-OHM RESISTORS, THEN ON THROUGH MXM TO THE LCD CONNECTOR

IF THIS ROUTING IS NOT FEASIBLE, MXM ALIASES WILL BE REPLACED WITH ADDITIONAL 0-OHM RESISTORS

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Page Notes

Power aliases required by this page:

- =PP12V_S0_LCD
- =PP3V3_S0_VIDEO

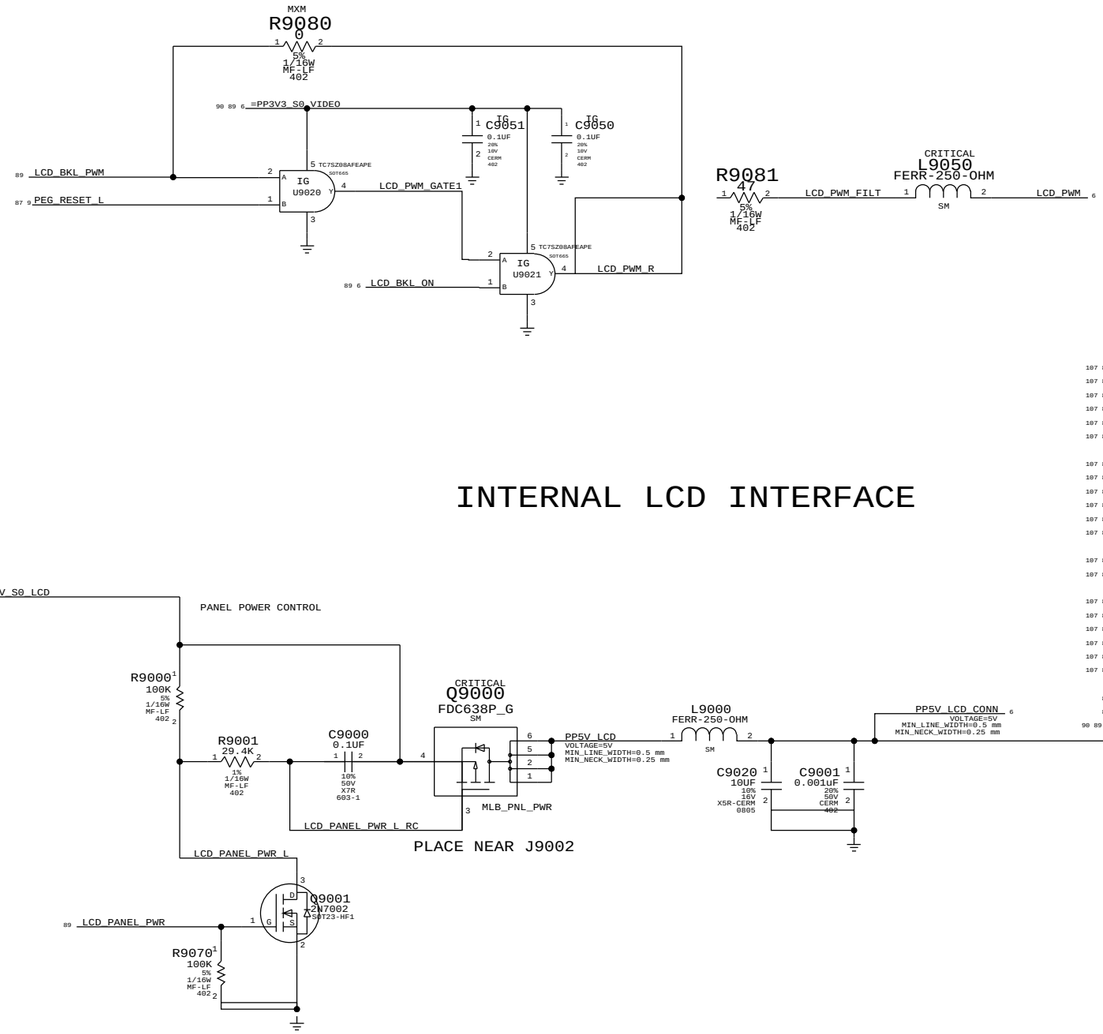
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
IG, MXM

BACKLIGHT CONTROL SUPPORT

THIS AND GATE CIRCUIT PROVIDES BACKLIGHT GLITCH PREVENTION WHEN MCP GLITCHES GPIOS ON POWERUP
IT MAY BE BYPASSED IF THE PWM SOURCE IS THE MXM

IF NOT BYPASSED, THIS CAN BE USED TO FORCE THE USE OF THE BACKLIGHT ENABLE SIGNAL EVEN IF THE INVERTER DOES NOT TAKE THIS AS AN INPUT



INTERNAL LCD INTERFACE

PAGE TITLE	INTERNAL DISPLAY
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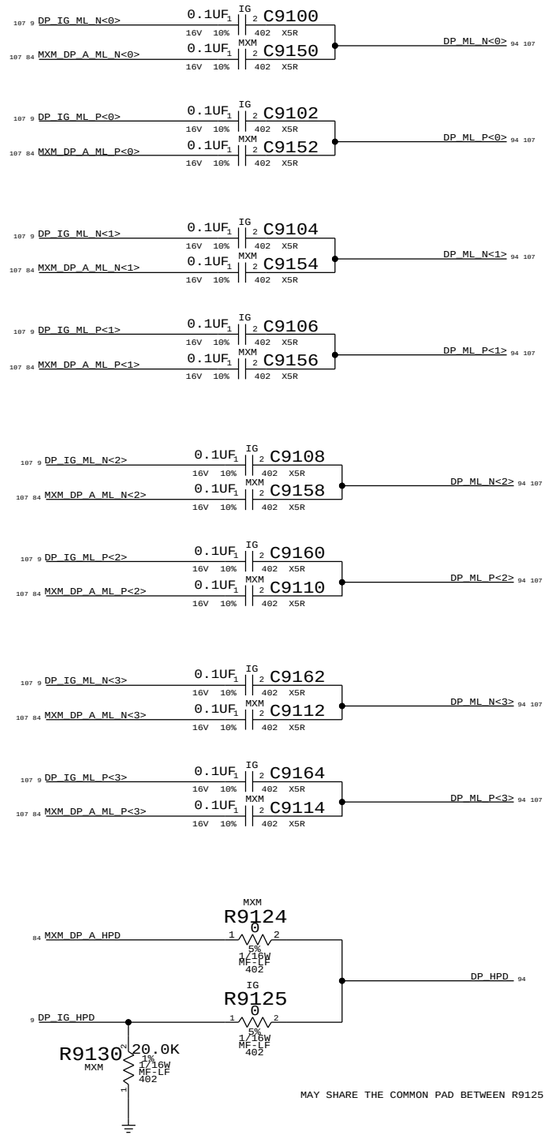
K50 NOTE: PLACE THESE CAPACITORS ATLEAST 1INCH AWAY FROM DP CONNECTOR

DCOX: PLACE AT MXM CONNECTOR IF THERE IS ROOM



MAY SHARE THE COMMON PAD BETWEEN R9125 AND R9130

PAGE TITLE: DP MUX SUPPORT

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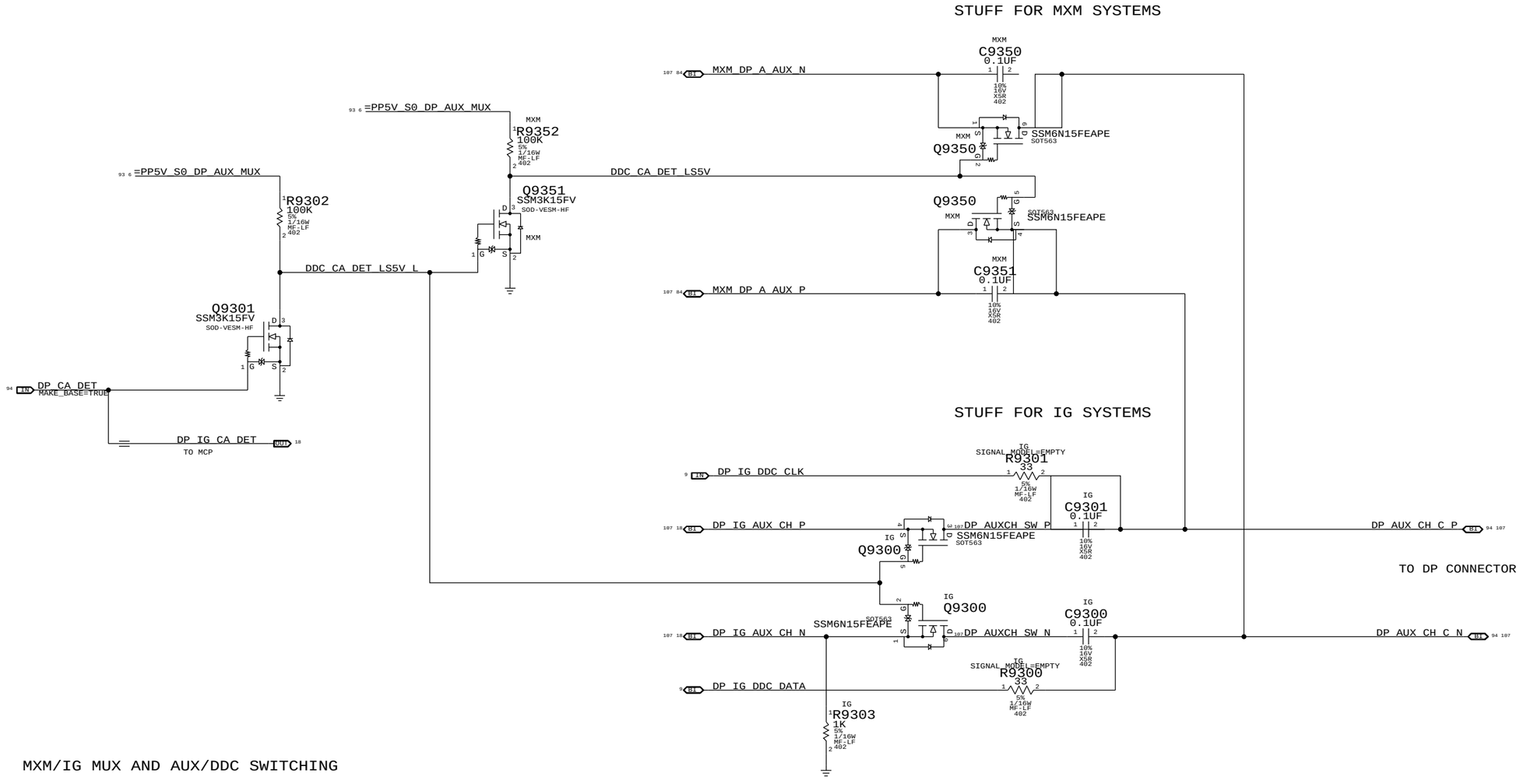

MXM/IG MUX AND AUX/DDC SWITCHING

FOR MXM, Q9350 BYPASSES THE AC COUPLING CAPS
THE CARD IS RESPONSIBLE FOR SWITCHING DDC SIGNALS ONTO THE AUX PAIR

FOR IG SYSTEMS, Q9300 SWITCHES BETWEEN AC COUPLED AUX
AND DC-COUPLED DDC

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DISPLAYPORT SUPPORT

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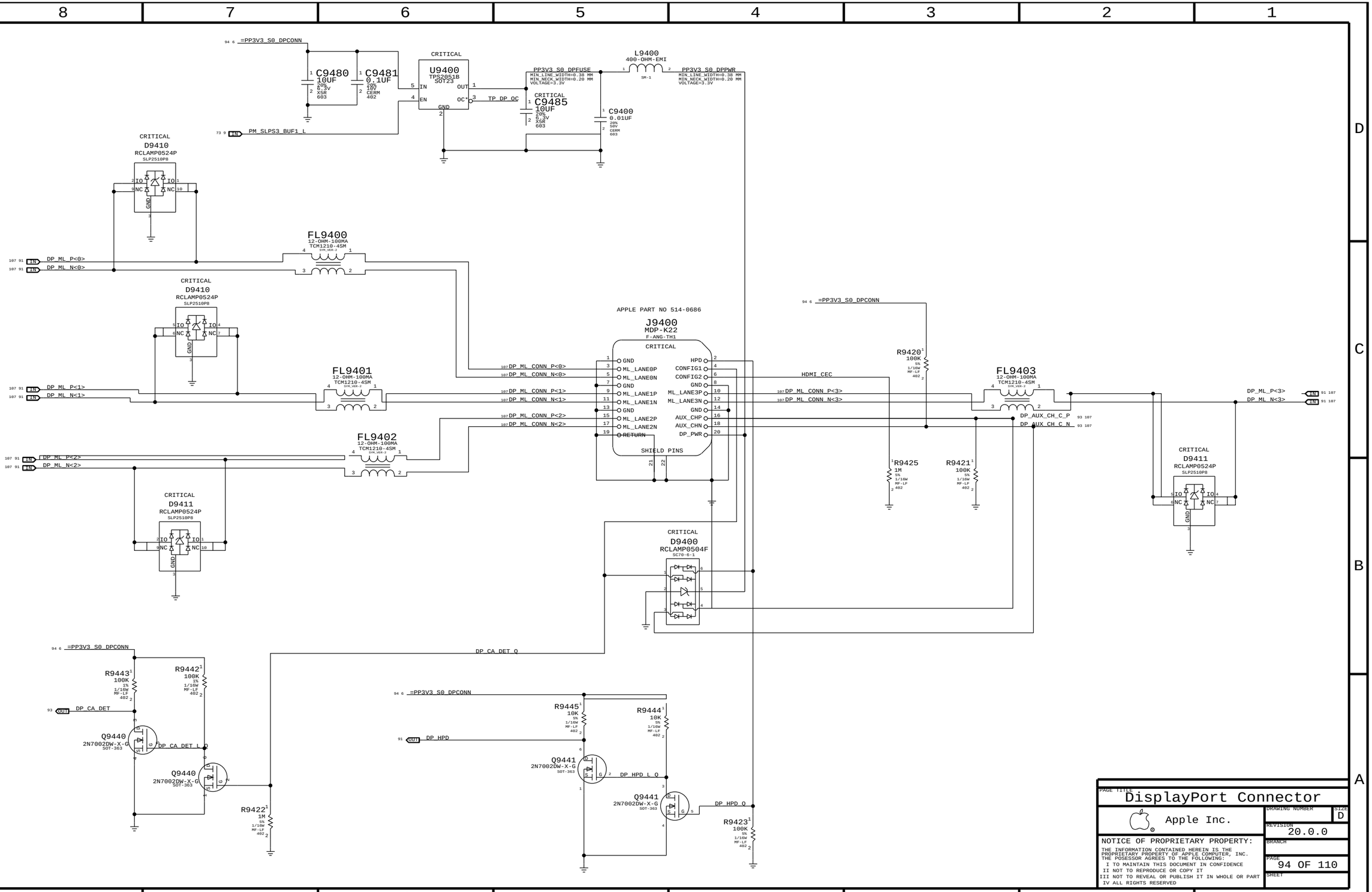

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DisplayPort Connector

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 2x/1x/Async FSB signals with impedance requirements are 50-ohm single-ended.
All 4x FSB signals with impedance requirements are 42-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 90 ps. (Tighther than MCP79)
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommmends each strobe/signal group is routed on the same layer.
Intel Design Guide recommmends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.175 MM	0.175 MM

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_BMIL	*	0.2 MM	?
CPU_COMP	*	0.6 MM	?
CPU_GTLREF	*	0.6 MM	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	0.6 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

MOST CPU SIGNALS WITH IMPEDANCE REQUIREMENTS ARE 50-OHM SINGLE-ENDED.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB 4X Signal Groups	Group 0	FSB_42S	FSB_DATA	FSB_D_L<15..0>	10 14
		FSB_42S	FSB_DATA	FSB_DINV_L<0>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_P<0>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_N<0>	10 14
	Group 1	FSB_42S	FSB_DATA	FSB_D_L<31..16>	10 14
		FSB_42S	FSB_DATA	FSB_DINV_L<1>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_P<1>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_N<1>	10 14
	Group 2	FSB_42S	FSB_DATA	FSB_D_L<47..32>	10 14
		FSB_42S	FSB_DATA	FSB_DINV_L<2>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_P<2>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_N<2>	10 14
	Group 3	FSB_42S	FSB_DATA	FSB_D_L<63..48>	10 14
		FSB_42S	FSB_DATA	FSB_DINV_L<3>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_P<3>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_N<3>	10 14
FSB 2X Signals	Group 0	FSB_50S	FSB_ADDR	FSB_A_L<16..3>	10 14
		FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	10 14
		FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	10 14
	Group 1	FSB_50S	FSB_ADDR	FSB_A_L<35..17>	10 14
		FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	10 14
FSB 1X Signals		FSB_50S	FSB_1X	FSB_ADS_L	10 14
		FSB_50S	FSB_1X	FSB_BREQ0_L	10 14
		FSB_50S	FSB_1X	FSB_BREQ1_L	14
		FSB_50S	FSB_1X	FSB_BNR_L	10 14
		FSB_50S	FSB_1X	FSB_BPRI_L	10 14
		FSB_50S	FSB_1X	FSB_DBSY_L	10 14
		FSB_50S	FSB_1X	FSB_DEFER_L	10 14
		FSB_50S	FSB_1X	FSB_DRDY_L	10 14
		FSB_50S	FSB_1X	FSB_HIT_L	10 14
		FSB_50S	FSB_1X	FSB_HITM_L	10 14
		FSB_50S	FSB_1X	FSB_LOCK_L	10 14
		FSB_50S	FSB_1X	FSB_CPURST_L	10 13 14
		FSB_50S	FSB_1X	FSB_RS_L<2..0>	10 14
		FSB_50S	FSB_1X	FSB_TRDY_L	10 14
		CPU_50S	CPU_AGTL	CPU_A20M_L	10 14
		CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	11 14
		CPU_50S	CPU_BMIL	CPU_FERR_L	10 14
		CPU_50S	CPU_AGTL	CPU_IGNNE_L	10 14
		CPU_50S	CPU_AGTL	CPU_INIT_L	10 14
		CPU_50S	CPU_AGTL	CPU_INTR	10 14
		CPU_50S	CPU_AGTL	CPU_NMI	10 14
		CPU_50S	CPU_AGTL	CPU_PROCHOT_L	11 14 50
		CPU_50S	CPU_AGTL	CPU_PWRGD	11 13 14
		CPU_50S	CPU_AGTL	CPU_SMI_L	10 14
		CPU_50S	CPU_AGTL	CPU_STPCLK_L	10 14
		CPU_50S	CPU_BMIL	PM_THRMTRIP_L	11 14 50
		CPU_50S	CPU_AGTL	FSB_CPUSLP_L	11 14
		CPU_50S	CPU_AGTL	CPU_DPSLP_L	11 14
		CPU_50S	CPU_AGTL	CPU_DPRSTP_L	11 14
		MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	14
		MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	14
		MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	14
		MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	14
		CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10 14
		CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10 14
		CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	13 14
		CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	13 14
		CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	14
		CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	14
		CPU_50S	CPU_AGTL	CPU_IERR_L	10
		CPU_50S	CPU_GTLREF	CPU_GTLREF0	10 11 29
		CPU_50S	CPU_GTLREF	CPU_GTLREF1	10 11 29
		CPU_27P4S	CPU_COMP	CPU_COMP<8>	11
		CPU_27P4S	CPU_COMP	CPU_COMP<3>	11
		CPU_27P4S	CPU_COMP	CPU_COMP<2>	11
		CPU_27P4S	CPU_COMP	CPU_COMP<1>	11
		CPU_27P4S	CPU_COMP	CPU_COMP<0>	11
		CPU_50S	CPU_ITP	CPU_XDP_TDI	11 13
		CPU_50S	CPU_ITP	CPU_XDP_TDO	11 13
		CPU_50S	CPU_ITP	CPU_XDP_TMS	11 13
		CPU_50S	CPU_ITP	CPU_XDP_TCK	11 13
		CPU_50S	CPU_ITP	CPU_XDP_TRST_L	11 13
		CPU_50S	CPU_ITP	CPU_XDP_BPM_L<5..0>	11 13
		CPU_50S	CPU_ITP	CPU_XDP_BPMB<3..0>	11 13
		CPU_50S	CPU_ITP	XDP_CPURST_L	13
		CPU_50S	CPU_BMIL	CPU_VID<7..0>	12 71
		CPU_27P4S	CPU_VCCSENSE	CPU_VCC_PKG_SENSE_P	12 71
		CPU_27P4S	CPU_VCCSENSE	CPU_VCC_PKG_SENSE_N	12 71
		CPU_27P4S	CPU_VCCSENSE	VR_CPU_VSNS_R_P	71
		CPU_27P4S	CPU_VCCSENSE	VR_CPU_VSNS_R_N	71

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	=3:1_SPACING	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:
DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:
DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	0.175 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<1..0>	15 33
	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<1..0>	15 33
	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<4..3>	16 33
	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<4..3>	16 33
	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>	15 16 31
	MEM_40S_VDD	MEM_CTRL	MEM_A_CS_L<3..0>	15 16 31
	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>	15 16 31
	MEM_40S_VDD	MEM_CMD	MEM_A_A<14..0>	15 31
	MEM_40S_VDD	MEM_CMD	MEM_A_BA<2..0>	15 31
	MEM_40S_VDD	MEM_CMD	MEM_A_RAS_L	15 31
	MEM_40S_VDD	MEM_CMD	MEM_A_CAS_L	15 31
	MEM_40S_VDD	MEM_CMD	MEM_A_WE_L	15 31
	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<0>	15 33
	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<1>	15 33
	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<2>	15 33
	MEM_40S	MEM_DATA	MEM_A_DQ<31..24>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<3>	15 33
	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<4>	15 33
	MEM_40S	MEM_DATA	MEM_A_DQ<47..40>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<5>	15 33
	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<6>	15 33
	MEM_40S	MEM_DATA	MEM_A_DQ<63..56>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<7>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	15 33
	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<1..0>	15 33
	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<1..0>	15 33
	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<4..3>	16 33
	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<4..3>	16 33
	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>	15 16 32
	MEM_40S_VDD	MEM_CTRL	MEM_B_CS_L<3..0>	15 16 32
	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>	15 16 32
	MEM_40S_VDD	MEM_CMD	MEM_B_A<14..0>	15 32
	MEM_40S_VDD	MEM_CMD	MEM_B_BA<2..0>	15 32
	MEM_40S_VDD	MEM_CMD	MEM_B_RAS_L	15 32
	MEM_40S_VDD	MEM_CMD	MEM_B_CAS_L	15 32
	MEM_40S_VDD	MEM_CMD	MEM_B_WE_L	15 32
	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<0>	15 33
	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<1>	15 33
	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<2>	15 33
	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<3>	15 33
	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<4>	15 33
	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<5>	15 33
	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<6>	15 33
	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<7>	15 33

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	15 33
	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	16
	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	16

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	0.5 MM	?
MCP_PEX_COMP	*	0.2 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	0.2 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE GRAPHICS				
	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>	9 86
	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>	9 86
	PCIE_90D	PCIE	PEG_D2R_P<15..0>	9 86
	PCIE_90D	PCIE	PEG_D2R_N<15..0>	9 86
	PCIE_90D	PCIE	MXM_PCIE_R2D_P<15..0>	84 86
	PCIE_90D	PCIE	MXM_PCIE_R2D_N<15..0>	84 86
	PCIE_90D	PCIE	MXM_PCIE_D2R_P<15..0>	84 86
	PCIE_90D	PCIE	MXM_PCIE_D2R_N<15..0>	84 86
PCIE I/O				
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	34
	PCIE_90D	PCIE	PCIE_MINI_R2D_N	34
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P	17 34
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N	17 34
	PCIE_90D	PCIE	PCIE_MINI_R2D_L_P	34
	PCIE_90D	PCIE	PCIE_MINI_R2D_L_N	34
	PCIE_90D	PCIE	PCIE_MINI_D2R_P	17 34
	PCIE_90D	PCIE	PCIE_MINI_D2R_N	17 34
	PCIE_90D	PCIE	PCIE_FW_R2D_P	41
	PCIE_90D	PCIE	PCIE_FW_R2D_N	41
	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	17 41
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	17 41
	PCIE_90D	PCIE	PCIE_FW_D2R_P	17 41
	PCIE_90D	PCIE	PCIE_FW_D2R_N	17 41
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	41
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	41
PCIE REF CLOCKS				
	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_P	9 87
	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_N	9 87
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	17 34
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	17 34
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CON_P	34
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CON_N	34
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	17 41
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	17 41
SATA				
	SATA_100D	SATA	SATA_HDD_R2D_C_P	20 45
	SATA_100D	SATA	SATA_HDD_R2D_C_N	20 45
	SATA_100D	SATA	SATA_HDD_R2D_P	45 110
	SATA_100D	SATA	SATA_HDD_R2D_N	45 110
	SATA_100D	SATA	SATA_HDD_D2R_P	20 45
	SATA_100D	SATA	SATA_HDD_D2R_N	20 45
	SATA_100D	SATA	SATA_HDD_D2R_C_P	45 110
	SATA_100D	SATA	SATA_HDD_D2R_C_N	45 110
	SATA_100D	SATA	SATA_ODD_R2D_C_P	20 45
	SATA_100D	SATA	SATA_ODD_R2D_C_N	20 45
	SATA_100D	SATA	SATA_ODD_R2D_P	45 110
	SATA_100D	SATA	SATA_ODD_R2D_N	45 110
	SATA_100D	SATA	SATA_ODD_D2R_P	20 45
	SATA_100D	SATA	SATA_ODD_D2R_N	20 45
	SATA_100D	SATA	SATA_ODD_D2R_C_P	45 110
	SATA_100D	SATA	SATA_ODD_D2R_C_N	45 110
	MCP_SGS	SATA_TERMP	MCP_SATA_TERMP	20
MISC				
	MCP_SGS	MCP_PEX_COMP	MCP_PEX_CLK_COMP	17
	MCP_DV_COMP	MCP_PEX_COMP	MCP_IFPAB_RSET	18 26
	MCP_SGS	MCP_PEX_COMP	MCP_IFPAB_VPROBE	18 26
			PM_SLP_S3_L	9 21
			PM_SLP_S4_L	21 70

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	0.15 MM	?
CLK_LPC	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	0.2 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

XTAL Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_MCP_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	PCI_55S	PCI	PCI_REQ0_L 19
	PCI_55S	PCI	PCI_REQ1_L 19
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R 19
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP 19
	LPC_55S	LPC	LPC_AD<3..0> 19 49 51
	LPC_55S	LPC	LPC_AD_R<3..0> 19
	LPC_55S	LPC	LPC_FRAME_L 19 49 51
	LPC_55S	LPC	LPC_FRAME_R_L 19
	LPC_55S	LPC	LPC_RESET_L 9 19
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R 9 19
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC 9 49
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS 9 51
	CLK_LPC_55S	CLK_LPC	PM_CLK32K_SUSCLK_R 9 21
	CLK_LPC_55S	CLK_LPC	PM_CLK32K_SUSCLK 9 49
	MCP_USB_RBIAS		MCP_USB_RBIAS_GND 20
	USB_90D	USB	USB_EXTA_P 20 46
	USB_90D	USB	USB_EXTA_N 20 46
	USB_90D	USB	USB_PORT0_P 46
	USB_90D	USB	USB_PORT0_N 46
	USB_90D	USB	USB_EXTB_P 20 46
	USB_90D	USB	USB_EXTB_N 20 46
	USB_90D	USB	USB_PORT1_P 46
	USB_90D	USB	USB_PORT1_N 46
	USB_90D	USB	USB_EXTC_P 20 46
	USB_90D	USB	USB_EXTC_N 20 46
	USB_90D	USB	USB_PORT2_P 46
	USB_90D	USB	USB_PORT2_N 46
	USB_90D	USB	USB_EXTD_P 20 46
	USB_90D	USB	USB_EXTD_N 20 46
	USB_90D	USB	USB_D_MUXED_P 46
	USB_90D	USB	USB_D_MUXED_N 46
	USB_90D	USB	USB_PORT3_P 46
	USB_90D	USB	USB_PORT3_N 46
	USB_90D	USB	USB_CAMERA_P 20 47
	USB_90D	USB	USB_CAMERA_N 20 47
	USB_90D	USB	USB_CAMERA_L_P 47 110
	USB_90D	USB	USB_CAMERA_L_N 47 110
	USB_90D	USB	USB_BT_P 20 47
	USB_90D	USB	USB_BT_N 20 47
	USB_90D	USB	USB_BT_L_P 47 110
	USB_90D	USB	USB_BT_L_N 47 110
	USB_90D	USB	USB_IR_P 20 47
	USB_90D	USB	USB_IR_N 20 47
	USB_90D	USB	USB_IR_L_P 47 110
	USB_90D	USB	USB_IR_L_N 47 110
	USB_90D	USB	USB_SDCARD_P 20 47
	USB_90D	USB	USB_SDCARD_N 20 47
	USB_90D	USB	USB_SDCARD_L_P 47 110
	USB_90D	USB	USB_SDCARD_L_N 47 110
	MCP_50S	SPI	SPI_CLK_R 21 51 61
	MCP_50S	SPI	SPI_CLK 61
	MCP_50S	SPI	SPI_MOSI_R 21 51 61
	MCP_50S	SPI	SPI_MOSI 61
	MCP_50S	SPI	SPI_MISO 21 51 61
	MCP_50S	SPI	SPI_MISO_R 61
	MCP_50S	SPI	SPI_CS0_R_L 21 51
	MCP_50S	SPI	SPI_CS0_L 51
	HDA_55S	HDA	HDA_BIT_CLK 21 62
		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP 21
	HDA_55S	HDA	HDA_BIT_CLK_R 21
	HDA_55S	HDA	HDA_RST_L 21 62
	HDA_55S	HDA	HDA_RST_R_L 21
	HDA_55S	HDA	HDA_SDOUT 21 62
	HDA_55S	HDA	HDA_SDOUT_R 21
	HDA_55S	HDA	HDA_SYNC 21 62
	HDA_55S	HDA	HDA_SYNC_R 21
	HDA_55S	HDA	HDA_SDIN0 21 62
	HDA_55S	HDA	AUD_SDI_R 62
		HDA	AUD_SPDIF_IN 9 66
		HDA	AUD_SPDIF_OUT 62 66
		HDA	AUD_SPDIF_CHIP 62
	CLK_MCP_XTAL	XTAL	MCP_CLK25M_XTALOUT 21 28
	CLK_MCP_XTAL	XTAL	MCP_CLK25M_XTALIN 21 28
	CLK_MCP_XTAL	XTAL	RTC_CLK32K_XTALOUT 21 28
	CLK_MCP_XTAL	XTAL	RTC_CLK32K_XTALIN 21 28

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	0.2 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	0.3 MM	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

RTL8211CLGR (ETHERNET PHY) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
MCP_MII_COMP		MCP_MII_COMP_VDD	18
MCP_MII_COMP		MCP_MII_COMP_GND	18
ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	18 38
ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	37 38
ENET_MII_55S	ENET_MII	ENET_MDIO	18 37
ENET_MII_55S	ENET_MII	ENET_MDC	18 37
ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	18 37
ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	37
ENET_MII_55S	ENET_MII	ENET_RXD<0>	18 37
ENET_MII_55S	ENET_MII	ENET_RXD_R<0>	37
ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	18 37
ENET_MII_55S	ENET_MII	ENET_RXD_R<3..1>	37
ENET_MII_55S	ENET_MII	ENET_RX_CTRL	18 37
ENET_MII_55S	ENET_MII	ENET_RXCTL_R	37
ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	18 37
ENET_MII_55S	ENET_MII	ENET_TXD<0>	18 37
ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	18 37
ENET_MII_55S	ENET_MII	ENET_TX_CTRL	18 37
ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	37 39
ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	37 39
ENET_MDI_100D	ENET_MDI	ENET_MDI_T_P<3..0>	39
ENET_MDI_100D	ENET_MDI	ENET_MDI_T_N<3..0>	39

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
	FW_110D	FW_TP	FW_PORT0_TPA_P	42 43
	FW_110D	FW_TP	FW_PORT0_TPA_N	42 43
	FW_110D	FW_TP	FW_PORT0_TPB_P	42 43
	FW_110D	FW_TP	FW_PORT0_TPB_N	42 43
PORT 1 & 2 NOT USED				
	FW_110D	FW_TP	FW_P0_TPA_L_P	42
	FW_110D	FW_TP	FW_P0_TPA_L_N	42
	FW_110D	FW_TP	FW_P0_TPB_L_P	42
	FW_110D	FW_TP	FW_P0_TPB_L_N	42

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SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_5SS	*	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SMB_5SS	SMB	SMBUS_SMC_A_S3_SCL	52
	SMB_5SS	SMB	SMBUS_SMC_A_S3_SDA	52
	SMB_5SS	SMB	SMBUS_SMC_B_S0_SCL	52
	SMB_5SS	SMB	SMBUS_SMC_B_S0_SDA	52
	SMB_5SS	SMB	SMBUS_SMC_0_S0_SCL	52
	SMB_5SS	SMB	SMBUS_SMC_0_S0_SDA	52
	SMB_5SS	SMB	SMBUS_SMC_BSA_SCL	52
	SMB_5SS	SMB	SMBUS_SMC_BSA_SDA	52
	SMB_5SS	SMB	SMBUS_SMC_MGMT_SCL	52 106
	SMB_5SS	SMB	SMBUS_SMC_MGMT_SDA	52 106
	SMB_5SS	SMB	SMBUS_SMC_MGMT_SCL	52 106
	SMB_5SS	SMB	SMBUS_SMC_MGMT_SDA	52 106
	SMB_5SS	SMB	SMBUS_MCP_0_CLK	13 21 52
	SMB_5SS	SMB	SMBUS_MCP_0_DATA	13 21 52

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	0.08 MM	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	0.5 MM	0.5 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
ASSINGED IN CONT. MGR.	PHYSICAL	SPACING		
	DP_100D	DISPLAYPORT	MXM_DP_A_ML_P<3..0>	84 91
	DP_100D	DISPLAYPORT	DP_IG_ML_P<3..0>	9 91
	DP_100D	DISPLAYPORT	MXM_DP_A_ML_N<3..0>	84 91
	DP_100D	DISPLAYPORT	DP_IG_ML_N<3..0>	9 91
	DP_100D	DISPLAYPORT	DP_ML_P<3..0>	91 94
	DP_100D	DISPLAYPORT	DP_ML_N<3..0>	91 94
	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0>	84
	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0>	94
	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P	18 93
	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N	18 93
	DP_100D	DISPLAYPORT	DP_AUXCH_SW_P	93
	DP_100D	DISPLAYPORT	DP_AUXCH_SW_N	93
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P	93 94
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N	93 94
	DP_100D	DISPLAYPORT	MXM_DP_A_AUX_P	84 93
	DP_100D	DISPLAYPORT	MXM_DP_A_AUX_N	84 93
	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	18 89
	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	18 89
	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<3..0>	18 89
	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<3..0>	18 89
	LVDS_100D	LVDS	LVDS_IG_B_CLK_P	18 89
	LVDS_100D	LVDS	LVDS_IG_B_CLK_N	18 89
	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<3..0>	18 89
	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<3..0>	18 89
	LVDS_100D	LVDS	LVDS_A_DATA_P<3..0>	89
	LVDS_100D	LVDS	LVDS_A_DATA_N<3..0>	89
	LVDS_100D	LVDS	LVDS_B_DATA_P<3..0>	89
	LVDS_100D	LVDS	LVDS_B_DATA_N<3..0>	89
	LVDS_100D	LVDS	LCD_CONN_A_DATA_P<3..0>	89 90
	LVDS_100D	LVDS	LCD_CONN_A_DATA_N<3..0>	89 90
	LVDS_100D	LVDS	LCD_CONN_B_DATA_P<3..0>	89 90
	LVDS_100D	LVDS	LCD_CONN_B_DATA_N<3..0>	89 90
	LVDS_100D	LVDS	LVDS_A_CLK_P	89
	LVDS_100D	LVDS	LVDS_A_CLK_N	89
	LVDS_100D	LVDS	LVDS_B_CLK_P	89
	LVDS_100D	LVDS	LVDS_B_CLK_N	89
	LVDS_100D	LVDS	LCD_CONN_A_CLK_P	89 90
	LVDS_100D	LVDS	LCD_CONN_A_CLK_N	89 90
	LVDS_100D	LVDS	LCD_CONN_B_CLK_P	89 90
	LVDS_100D	LVDS	LCD_CONN_B_CLK_N	89 90
	MCP_DV_COMP		MCP_HDMI_RSET	18 26
	MCP_DV_COMP		MCP_HDMI_VPROBE	18 26

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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PPDDR_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PPDDR_MEM	*	PWR_P2MM
MEM_CMD	PPDDR_MEM	*	PWR_P2MM
MEM_CTRL	PPDDR_MEM	*	PWR_P2MM
MEM_DATA	PPDDR_MEM	*	PWR_P2MM
MEM_DQS	PPDDR_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	PWR	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	4:1_SPACING
SWITCHNODE	*	*	SWITCHNODE
THERMAL	PWR	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM
AUDIO	*	*	AUDIO

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR
SNS_DIFF	*	1:1_DIFFPAIR

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	TOP			0.1 MM	600 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD	TOP			0.1 MM	600 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D	TOP			0.1 MM	600 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
PCIE_90D	TOP				500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
USB_90D	TOP				500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP	*			0.25 MM	250 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

SPECIFIC NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
		PPDDR_MEM	=PP1V5_S3_MEM_A	6 30 31
		PPDDR_MEM	=PP1V5_S3_MEM_B	6 30 32
		SWITCHNODE	VR_CPU_SW1	72
		SWITCHNODE	VR_CPU_SW2	72
		SWITCHNODE	VR_CPU_SW3	72
		SWITCHNODE	1V8_SW	80
		SWITCHNODE	1V1S5_SW	79
		SWITCHNODE	PVTTS0_PHASE	76
		SWITCHNODE	3V3S5_SW	76
		SWITCHNODE	5VS3_SW	73
		SWITCHNODE	MCPCORES0_PHASE	74
	THERM_DIFF	THERMAL	SNS_T_DP1_DN6	55
	THERM_DIFF	THERMAL	SNS_T_DN1_DP6	55
	THERM_DIFF	THERMAL	SNS_T_DP2_DN3	55
	THERM_DIFF	THERMAL	SNS_T_DN2_DP3	55
	THERM_DIFF	THERMAL	CPU_THERMD_P	11 55
	THERM_DIFF	THERMAL	CPU_THERMD_N	11 55
	THERM_DIFF	THERMAL	SNS_T_DP4_DN5	55
	THERM_DIFF	THERMAL	SNS_T_DN4_DP5	55
	THERM_DIFF	THERMAL	MCP_THMDIODE_P	21 55
	THERM_DIFF	THERMAL	MCP_THMDIODE_N	21 55
	THERM_DIFF	THERMAL	MXM_PWRSRC_SENSOR_P	53
	THERM_DIFF	THERMAL	MXM_PWRSRC_SENSOR_N	53
	THERM_DIFF	THERMAL	SENSE_1V5_S0_P	54
	THERM_DIFF	THERMAL	SENSE_1V5_S0_N	54
	THERM_DIFF	THERMAL	SNS_LCD_P	55 110
	THERM_DIFF	THERMAL	SNS_LCD_N	55 110
	THERM_DIFF	THERMAL	SNS_ODD_P	55 110
	THERM_DIFF	THERMAL	SNS_ODD_N	55 110
	THERM_DIFF	THERMAL	SNS_CPU_H_P	55
	THERM_DIFF	THERMAL	SNS_CPU_H_N	55
	THERM_DIFF	THERMAL	SNS_MCP_P	55
	THERM_DIFF	THERMAL	SNS_MCP_N	55
	THERM_DIFF	THERMAL	SNS_AMB_P	55 110
	THERM_DIFF	THERMAL	SNS_AMB_N	55 110
	THERM_DIFF	THERMAL	SNS_MXM_P	55
	THERM_DIFF	THERMAL	SNS_MXM_N	55
	SNS_DIFF	THERMAL	VR_CPU_ISNS1_P	71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS1_N	71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS1_R_P	71
	SNS_DIFF	THERMAL	VR_CPU_ISNS1_R_N	71
	SNS_DIFF	THERMAL	VR_CPU_ISNS2_P	71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS2_N	71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS2_R_P	71
	SNS_DIFF	THERMAL	VR_CPU_ISNS2_R_N	71
	SNS_DIFF	THERMAL	VR_CPU_ISNS3_P	71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS3_N	71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS3_R_P	71
	SNS_DIFF	THERMAL	VR_CPU_ISNS3_R_N	71
1234		THERMAL	SMC_CPU_ISENSE	49 53
1235		THERMAL	VR_CPU_IOUT	53 71
1236		THERMAL	VR_ISNS_CPU_P	53
1237		THERMAL	VR_ISNS_CPU_N	53
1238		THERMAL	SNS_PS_CPU_ISNS	53
1239		THERMAL	SMC_CPU_VSENSE	49 53
1240		THERMAL	CPU_VCC_SENSE	12 53
1241		THERMAL	SMC_GPU_VSENSE	49 53
1242		THERMAL	SMC_GPU_ISENSE	49 53
1243		THERMAL	SMC_1V5_S0_ISENSE	50 54
1244		THERMAL	SMC_1V5_S0_ISENSE_R	54
1245		THERMAL	SMC_1V5_S0_VSENSE	50 54
1246		THERMAL	SMC_MCP_CORE_ISENSE	50 54
1247		THERMAL	SMC_MCP_CORE_VSENSE	50 54
1248		THERMAL	MCPCORES0_IMON	54 74
1249		THERMAL	CPU_PECI_L	11 55
1250		THERMAL	SMB_PECI_L	55
1251		THERMAL	CPU_PECI_MCP	14 55
		THERMAL	HDD_OOB_TEMP_FILT	55
1252		THERMAL	HDD_OOB_TEMP	55
1253		THERMAL	HDD_OOB_TEMP_R	55
1254		THERMAL	SMC_HDD_OOB_TEMP	55

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SPECIFIC CONSTRAINTS

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BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	100 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.300 MM	0.085 MM	=STANDARD		
27P4_OHM_SE	*	Y	0.275 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.085 MM	=STANDARD		
40_OHM_SE	*	Y	0.15 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SE	TOP,BOTTOM	Y	0.151 MM	0.085 MM	=STANDARD		
42_OHM_SE	*	Y	0.136 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.1 MM	0.085 MM	15 MM		
50_OHM_SE	*	Y	0.1 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD		
55_OHM_SE	*	Y	0.076 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL6	Y	0.155 MM	0.085 MM	=STANDARD	0.135 MM	0.1 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.085 MM	=STANDARD	0.130 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL6	Y	0.099 MM	0.085 MM	12 MM	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.110 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL6	Y	0.081 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.085 MM	=STANDARD	0.320 MM	0.15 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM
POWER_WIDTH	*	Y	0.600 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER	*	POWER_WIDTH
VR_CTL_PHY	*	POWER_WIDTH

SPACING RULE SET

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SPACING_0.5MM	*	0.5 MM	?
CLK_SPACING_0.6MM	*	0.6 MM	?
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000
SWITCHNODE	*	0.6 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.150 MM	?
2X_DIELECTRIC	TOP,BOTTOM	0.160 MM	?
3X_DIELECTRIC	*	0.220 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.240 MM	?
4X_DIELECTRIC	*	0.300 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.320 MM	?
5X_DIELECTRIC	*	0.380 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.400 MM	?

CONSTRAINTS FOR BGA AREA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P1MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P1MM
CLK_LPC	*	BGA_P1MM	BGA_P1MM
CLK_PCI	*	BGA_P1MM	BGA_P1MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MCP_FSB_COMP	*	BGA_P1MM	BGA_P2MM
MCP_MEM_COMP	*	BGA_P1MM	BGA_P2MM
MCP_PEX_COMP	*	BGA_P1MM	BGA_P2MM

CONSTRAINTS ARE BASED ON MCP79 DESIGN GUIDE DG-03328-001_V06
PCI,LPC,SMB,HDA,SPI,RGMII,SMBUS ARE ROUTED AS 55 OHM SE SIGNALS

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RULE DEFINITIONS

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FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT

J4700 USB CAMERA

103 47	IN	USB_CAMERA_L_P	FUNC_TEST=TRUE
103 47	IN	USB_CAMERA_L_N	FUNC_TEST=TRUE

1 PP5V_S3_REG Testpoint near J4700
2 Ground Testpoints near J4700

J4750 USB CARD READER

103 47	IN	USB_SDCARD_L_P	FUNC_TEST=TRUE
103 47	IN	USB_SDCARD_L_N	FUNC_TEST=TRUE

1 PP3V3_S3 Testpoint near J4750
2 Ground Testpoints near J4750

J4720 USB BLUETOOTH

103 47	IN	USB_BT_L_P	FUNC_TEST=TRUE
103 47	IN	USB_BT_L_N	FUNC_TEST=TRUE

1 PP3V3_S3 Testpoint near J4720
2 Ground Testpoints near J4720

J4780 IR BOARD

103 47	IN	USB_IR_L_P	FUNC_TEST=TRUE
103 47	IN	USB_IR_L_N	FUNC_TEST=TRUE

1 PP5V_S3_REG Testpoint near J4780
2 Ground Testpoints near J4780

J4520 SATA ODD (HIGH SPEED)

102 45	IN	SATA_ODD_R2D_P	FUNC_TEST=TRUE
102 45	IN	SATA_ODD_R2D_N	FUNC_TEST=TRUE
102 45	IN	SATA_ODD_D2R_C_N	FUNC_TEST=TRUE
102 45	IN	SATA_ODD_D2R_C_P	FUNC_TEST=TRUE
49 45	IN	SMC_ODD_DETECT	FUNC_TEST=TRUE

1 PP5V_S0 Testpoint near J4520
5 Ground Testpoints near J4520

J4510 SATA HDD (HIGH SPEED)

102 45	IN	SATA_HDD_R2D_P	FUNC_TEST=TRUE
102 45	IN	SATA_HDD_R2D_N	FUNC_TEST=TRUE
102 45	IN	SATA_HDD_D2R_C_N	FUNC_TEST=TRUE
102 45	IN	SATA_HDD_D2R_C_P	FUNC_TEST=TRUE

3 Ground Testpoints near J4510

J5520 ANALOG LCD TEMP SENSOR

108 55	IN	SNS_LCD_P	FUNC_TEST=TRUE
108 55	IN	SNS_LCD_N	FUNC_TEST=TRUE

J5521 AMBIENT TEMP SENSOR

108 55	IN	SNS_AMB_P	FUNC_TEST=TRUE
108 55	IN	SNS_AMB_N	FUNC_TEST=TRUE

J5551 ODD TEMP SENSOR

108 55	IN	SNS_ODD_P	FUNC_TEST=TRUE
108 55	IN	SNS_ODD_N	FUNC_TEST=TRUE

J5600 ODD FAN

56	IN	FAN_0_PWR_L	FUNC_TEST=TRUE
56	IN	FAN_TACH0_L	FUNC_TEST=TRUE
56	IN	PP12V_S0_FAN0_L	FUNC_TEST=TRUE
56	IN	FAN_0_GND	FUNC_TEST=TRUE

J5700 CPU FAN

57	IN	FAN_2_PWR_L	FUNC_TEST=TRUE
57	IN	FAN_TACH2_L	FUNC_TEST=TRUE
57	IN	PP12V_S0_FAN2_L	FUNC_TEST=TRUE
57	IN	FAN_2_GND	FUNC_TEST=TRUE

J5601 HD FAN

56	IN	FAN_1_PWR_L	FUNC_TEST=TRUE
56	IN	FAN_TACH1_L	FUNC_TEST=TRUE
56	IN	PP12V_S0_FAN1_L	FUNC_TEST=TRUE
56	IN	FAN_1_GND	FUNC_TEST=TRUE

J6601 AUDIO MICROPHONE

66	IN	AUD_MIC_IN1_N_CONN	FUNC_TEST=TRUE
66	IN	GND_AUDIO_MIC1_CONN	FUNC_TEST=TRUE
66	IN	AUD_MIC_IN1_P_CONN	FUNC_TEST=TRUE

1 Ground Testpoint near J6601

J6602 AUDIO RIGHT SPEAKER

	IN	AUD_SPKR_OUTL02R_P	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTL02R_N	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTL01R_P	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTL01R_N	FUNC_TEST=TRUE

J6603 AUDIO LEFT SPEAKER

	IN	AUD_SPKR_OUTL02L_P	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTL02L_N	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTL01L_P	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTL01L_N	FUNC_TEST=TRUE

		GND	16 TP'S	FUNC_TEST=TRUE MIN_ALLOWED_TPS=16
78 6	IN	PP3V3_S3	2 TP'S	FUNC_TEST=TRUE MIN_ALLOWED_TPS=2
73 6	IN	PP5V_S3_REG	2 TP'S	FUNC_TEST=TRUE MIN_ALLOWED_TPS=2
78 6	IN	PP5V_S0		FUNC_TEST=TRUE MIN_ALLOWED_TPS=1

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