1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,TAUPO,M87

10/13/2007

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
?		?	?	?	?

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7413	1	SCHEM,TAUPO,M87	SCH	CRITICAL	
820-2249	1	PCBF,TAUPO,M87	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Fri Oct 12 18:10:11 2007

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES °
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER / DESIGN CK
ENG APPD / MFG APPD
QA APPD / DESIGNER
RELEASE / SCALE NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

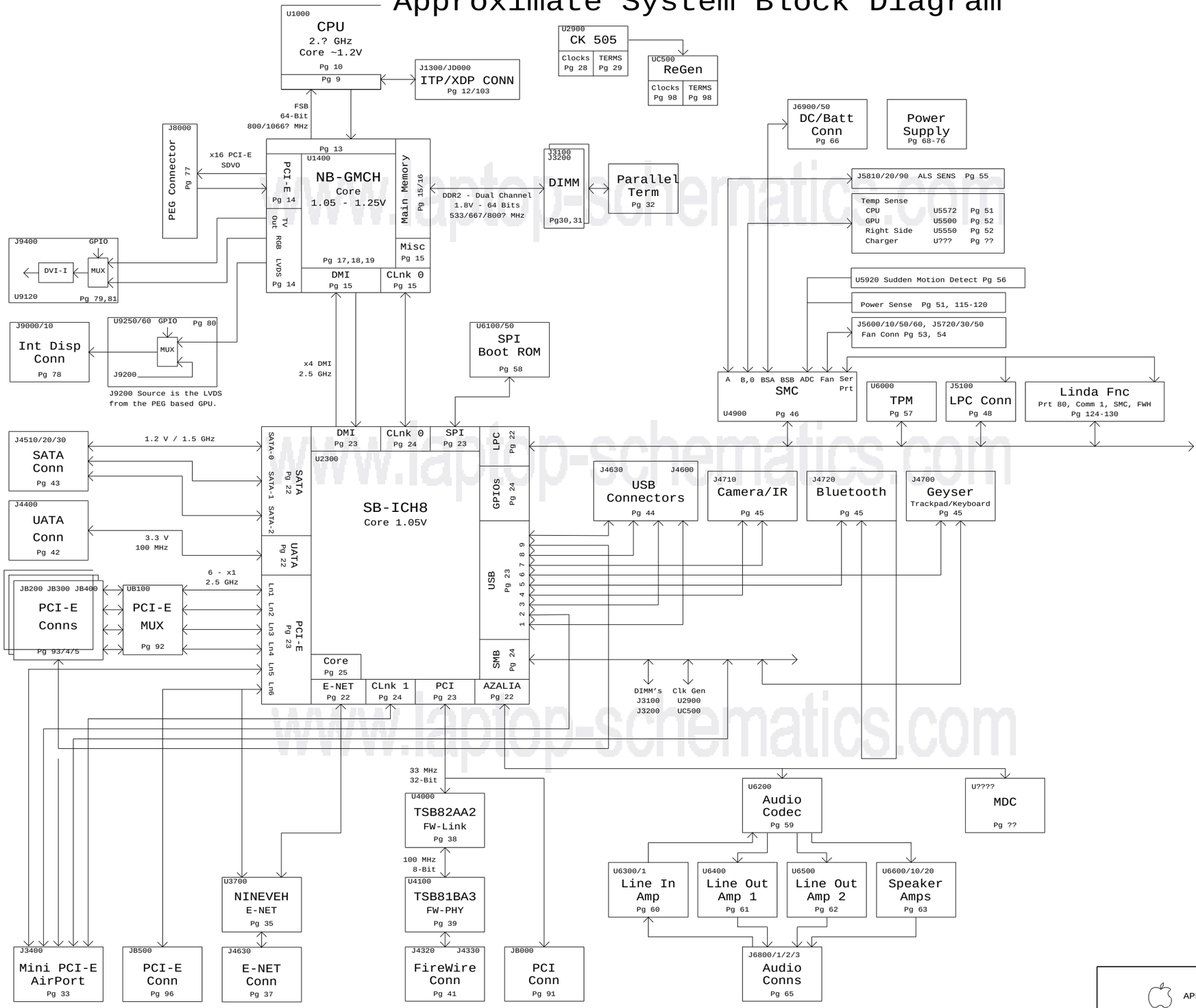
APPLE INC.

TITLE
SCHEM,TAUPO,M87

DRAWING NUMBER 051-7413 REV. 11.0.0

SHT 1 OF 89

Approximate System Block Diagram



System Block Diagram

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/23/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 2 OF 89	

M87 POWER SYSTEM ARCHITECTURE

J6990
CRITICAL
87438-0832
01
6A FUSE
518S0456
PP18V5_DCIN
PPDCIN_G3H
Energy Star LDO
MAX8719
U7950
(PAGE 17, LIO)
PBUS_LDO_EN
SHDN*
VOUT
VIN
PBUS SUPPLY / BATTERY CHARGER
ISL6257
U7900
(PAGE 17, LIO)
U5705
A
LIO_DCIN_ISENSE
Q6950
INRUSH LIMITER
(PAGE 15, LIO)
PP18V5_G3H_CHGR
SMC_BC_ACOK
SMC_ADAPTER_EN
CHGR_EN
ENABLE
J6950
CRITICAL
87438-1043
518S0457
Q7970
BATT_POS
PPVBATT_G3H_FET_F
8A FUSE
PPVBATT_G3H_FET
BATTERY CHARGER FETS
(PAGE 17)
U5715
A
LIO_BATT_ISENSE
PPVBAT_G3H_CHGR_OUT
SMC_PBUS_VSENSE
Q5315
PPBUS_G3H
03
PM_SLP_S3_DELAY_L
1.5V
TPS51117
U7600
(PAGE 62)
(4.5A MAX CURRENT)
PP1V5_S0
1.05V
TPS51117
U7450
(PAGE 60)
PP1V05_S0(10A MAX CURRENT)
U5420
A
NBCORE_IOUT
PPVCORE_S0_NB_R
SMC_GPU_VSENSE
U8995
V
A
PPVCORE_GPU
(18A MAX CURRENT)
GPUVCORE_IOUT
ISL6263B
U8900
(PAGE 73)
VR_ON
PGOOD
GPUVCORE_PGOOD
PM_GPUVCORE_EN
18
SMC_CPU_VSENSE
U5400
V
A
CPUVCORE_IOUT
P1V8S3_PGOOD
PPVCORE_S0_CPU
(44A MAX CURRENT)
CPUVCORE
ISL9504
U7100
(PAGE 58)
IMVP_VR_ON
CLKEN*
VR_PWRGD_CLKEN_L
VR_PWRGOOD_DELAY
04
05
SMC_PM_G2_EN
PP3V42_G3H
U7858
U7859
5V
3.3V
TPS51120
U7300
(PAGE 59)
EN1
EN2
EN3
EN5
PGOOD1
PGOOD2
PP5V_S5
(8A MAX CURRENT)
PP3V3_S5
(5.5A MAX) CURRENT)
06
RSMRST_PWRGD
07
Q7002
Q7012
P5VS3_SS
P3V3S3_SS
P1V8S3_EN
PM_S4_STATE_L
LIO_S3_EN
ICH8M
U2300
S4_STATE*
Q7851
PM_GPUVCORE_EN
SLP_S3*
PM_SLP_S3_L
PM_SLP_S3_LS5V
GPUVCORE_PGOOD
Q7850
PM_P1V8_S0GPU_EN
Q4261
FWPWR_EN_L_DIV
Q3800
SMC_ADAPTER_EN
WOL_EN
PM_ENET_EN
P3V3ENET_SS
Q3801
U7850
PM_SLP_S3_DELAY_L
PP3V3_S5
13
PM_SLP_S3_L
0.9V
1.8V
TPS511160
U7500
(PAGE 61)
P1V8S3_EN
12
PP1V8_S3
(12A MAX CURRENT)
U5440
A
P1V8_S3_IOUT
PP1V8_S3_ISNS
1V8S3_PGOOD
(10mA MAX CURRENT)
PP0V9_S0
Q7030
15
PP3V3_S0
P3V3S0_SS
Q7070
PP3V3_S0GPU
17
P3V3GPU_SS
Q3810
PP3V3_ENET
Q7010
11
P3V3ENET_SS
PP3V3_S3
P3V3S3_SS
U3850
TPS79501
(PAGE 36)
PP1V9_ENET
Q7610
PP5V_S0_AUDIO
10a
PP5V_S3_LIO
PM_SLP_S3_LS5V
LIO_S3_EN
5V
3.3V
TPS51120
U7600
(PAGE 16, LIO)
11a
PP3V3_S3_LIO
PP3V3_S0_LIO
4.5V
TPS79501
U6201
(PAGE 10, LIO)
PP4V5_AUDIO_ANALOG
Q7611
PP3V3_S0_LIO
PM_SLP_S3_LS5V
Q7072
PM_P3V3GPU_EN
P3V3GPU_SS
U7860
MAX6838
(PAGE 64)
U5430
A
PP1V25_S0_ISNS
P1V25_S0_IOUT
PM_ENET_EN
(6A MAX CURRENT)
TPS51117
U7400
(PAGE 60)
PP1V25_ENET
Q7095
PP1V25_S0
16
P1V25S0_SS
TP_P1V2ENET_PGOOD
(UNUSED)
PM_P1V8_S0GPU_EN
19
(10A MAX CURRENT)
PP1V8_S0GPU_ISNS_R
ISL6269
U9300
(PAGE 77)
U5410
A
P1V8_S0GPU_IOUT
PP1V8_S0GPU_ISNS
TP_P1V8_S0GPU_PGOOD
(UNUSED)
Q7000
PP5V_S3
10
Q7020
PP5V_S0
14
PP5V_S5
P5VS0_SS
Q7002
Q7012
P5VS0_SS
P3V3S0_SS
Q7096
Q7096
P1V25S0_SS
Q4260
PPBUS_FW_FWPWRSW_F
1.5A FUSE
PPVP_FW
PPVIN_FW_3V3FW
FWPWR_EN_L_DIV
LT3470
U7700
(PAGE 63)
PP3V3_FW
(0.2A MAX CURRENT)
TPS799195
U7720
(PAGE 63)
PP1V95_FW
3.425V"G3HOT"
LT3470
U7800
(PAGE 64)
(0.2A MAX CURRENT)
PP3V42_G3H
02
SMC RESET "BUTTON"
RN5VD30A-F
U5000
(PAGE 46)
SMC_RESET_L
U2830
VR_PWRGD_CLKEN
U2840
PM_SB_PWROK
ICH8M
U2300
VRMPWRGD
PWRBTN*
PLTRST*
RSMRST*
PWROK
CLPWROK
CPUPWRGD(GPIO49)
PLT_RST_L
CPU_PWRGD
CPU
PWRGOOD
RESET*
U1000
MCH
PWROK
H_CPURST*
FSB_CPURST_L
U1400
SMC
U4900
(PAGE 45)
08
PM_RSMRST_L
IMVP_VR_ON
LRESET*
PM_PWRBTN_L
RES
PM_SLP_S5_L
PM_S4_STATE_L
PM_SLP_S3_L
SMC_PM_G2_EN
U7880
P1V8P1V5P1V05S0_PGOOD
ALL_SYS_PWRGD
S0PGOOD_PWROK
09
RSMRST_PWRGD
SMC_ONOFF_L
LTC2900
U7870
(PAGE 64)
V1(5V)
V2(3.3V)
V4(1.25V)
V3(1.8V)
RST*

SIGNAL DELAY TIME

IMVP_VR_ON	99ms
S0PWRGD_OK	200ms
VR_PWRGOOD_DELAY	7ms

POWER ON SEQUENCE LIST

PWR/RST STATUS	STEP
G3H POWER ON	01-04
S5 POWER ON	01,05-09
S3 POWER ON	10-13
S0 SYSTEM POWER ON	14-18
S0 CPU POWER ON	17,19-24
PLATFORM,CPU RESET	25-27

STEP 06 (S5 POWER STATUS)TRUTH TABLE

NO AC/BATTERY	L(S5 OFF)
BATTERY ONLY	L(S5 OFF
ACIN WITH/WITHOUT BATTERY	H(S5 ON)
BATTERY ONLY,PRESS PWR BUTTON	H(S5 ON)

Power Block Diagram

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/23/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 3 OF 89	

Power Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0

SCALE	SHT	OF
NONE	4	89

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9089	PCBA,2.5GHZ,512SAM_VRAM,M87	M87_COMMON,EEE_Z3G,CPU_2_5GHZ,FB_512_SAMSUNG
630-9091	PCBA,2.6GHZ,512SAM_VRAM,M87	M87_COMMON,EEE_Z3J,CPU_2_6GHZ,FB_512_SAMSUNG
630-9088	PCBA,2.5GHZ,512HY_VRAM,M87	M87_COMMON,EEE_Z3F,CPU_2_5GHZ,FB_512_HYNIX
630-9090	PCBA,2.6GHZ,512HY_VRAM,M87	M87_COMMON,EEE_Z3H,CPU_2_6GHZ,FB_512_HYNIX
630-9213	PCBA,2.4GHZ,256SAM_VRAM,M87	M87_COMMON,EEE_ZUP,CPU_2_4GHZ,FB_256_SAMSUNG
630-9238	PCBA,2.4GHZ,256HY_VRAM,M87	M87_COMMON,EEE_043,CPU_2_4GHZ,FB_256_HYNIX

M75 BOM Groups

BOM GROUP	BOM OPTIONS
M87_COMMON	ALTERNATE,COMMON,M87_COMMON1,M87_COMMON2,M87_DEBUG,M87_PROGPARTS
M87_COMMON1	ISL9504B,ONEWIRE_PU
M87_COMMON2	GPUVID_1P13V,P1V8S3_1V8,SMS_MOT_DIS,YUKON_ULTRA,VGA_TERM_CONN,GPU_TMP401
M87_DEBUG	SMC_DEBUG_YES,XDP,XDP_CONN,LPCPLUS
M87_PROGPARTS	BOOTROM_PROG,SMC_PROG

BOM GROUP	BOM OPTIONS
FB_512_SAMSUNG	VRAM8,VRAM_16M,VRAM_SAMSUNG,VRAM_512_SAMSUNG
FB_512_HYNIX	VRAM8,VRAM_16M,VRAM_HYNIX,VRAM_512_HYNIX
FB_256_SAMSUNG	VRAM4,VRAM_16M,VRAM_SAMSUNG,VRAM_256_SAMSUNG
FB_256_HYNIX	VRAM4,VRAM_16M,VRAM_HYNIX,VRAM_256_HYNIX

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:Z3F]	CRITICAL	EEE_Z3F
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:Z3G]	CRITICAL	EEE_Z3G
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:Z3H]	CRITICAL	EEE_Z3H
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:Z3J]	CRITICAL	EEE_Z3J
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZUP]	CRITICAL	EEE_ZUP
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:043]	CRITICAL	EEE_043

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3540	1	IC,PDC,SR,QS,C0,2.5G,35W,800FSB,6M,BGA	U1000	CRITICAL	CPU_2_5GHZ
337S3541	1	IC,PDC,SR,QS,C0,2.6G,35W,800FSB,6M,BGA	U1000	CRITICAL	CPU_2_6GHZ
338S0509	1	IC,GPU,NV G84M,BGA,LOW LEAK	U8000	CRITICAL	
338S0432	1	IC,NB,CRESTLINE,GM,C0,PRQ,965PM	U1400	CRITICAL	
338S0434	1	IC,SB,ICH8M,B1,PRQ,BGA	U2300	CRITICAL	
353S1651	1	IC,ISL9504B,2PH IMVP6 REG,PMON,QFN48	U7100	CRITICAL	ISL9504B
359S0130	1	IC,SLG2AP101,LW PWR CLCK GEN,CK505,QFN68	U2900	CRITICAL	
338S0386	1	IC,88E8058,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	
338S0274	1	IC,SMC,HS8/2116	U4900	CRITICAL	SMC_BLANK
341S2193	1	IC,SMC,DEVELOPMENT,M75	U4900	CRITICAL	SMC_PROG
335S0384	1	IC,16MBIT 8-PIN SPI SERIAL FLASH,SOIC8	U6100	CRITICAL	BOOTROM_BLANK
341S2192	1	IC,EFI ROM,DEVELOPMENT,M75	U6100	CRITICAL	BOOTROM_PROG
337S3556	1	IC,PDC,SR,QS,C0,2.4G,35W,800FSB,3M,BGA	U1000	CRITICAL	CPU_2_4GHZ

333S0423	8	IC,SGRAM,GDDR3,16Mx32,800MHZ,136 FBGA	U8400,U8450,U8500,U8550,U9100,U9150,U9200,U9250	CRITICAL	VRAM_512_SAMSUNG
333S0424	8	IC,SGRAM,GDDR3,16Mx32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550,U9100,U9150,U9200,U9250	CRITICAL	VRAM_512_HYNIX
333S0423	4	IC,SGRAM,GDDR3,16Mx32,800MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_SAMSUNG
333S0424	4	IC,SGRAM,GDDR3,16Mx32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_HYNIX

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0011	157S0030		ALL	E&E alt to TDK/BI-Tech magnetics
152S0476	152S0276		ALL	Inductor alternate
353S1681	353S1294		ALL	TI alt to National
138S0603	138S0602		ALL	Murata alt to Samsung
353S1681	353S1294		ALL	LMV2011,QFAMP, GBW
152S0684	152S0368		ALL	Maglayers alt to Dale/Vishay
152S0683	152S0276		ALL	Maglayers alt to Dale/Vishay
104S0023	104S0018		ALL	Cyntec alt to sense resistor
104S0024	104S0017		ALL	Panasonic alt to FW resistor

BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0

SCALE NONE SHT 5 OF 89

PROTO

0.1.0:
04/26/07 -- Design branched from 051-7225-A
04/26/07 -- Clock Termination: Removed support for SLG8LP537 device (GPU_CLK_27M/27MSS muxes, etc)
04/26/07 -- Clock Termination: Added S0-powered AND gate between GPU_PGOOD and SLG2AP101 enable pin to eliminate leakage path (rdar://5086613)
04/26/07 -- SB Misc: Removed EXTGPU_RST_L support for reseting the GPU (hardware control only)
04/26/07 -- Power Control: Removed U7858 and R7860. Tied SMC_PM_G2_EN/PM_G2_EN directly to S5 regulators
04/26/07 -- SB Decoupling: Replaced L2700 with 155S0333 for AVL updates
04/26/07 -- FW Port Power: Replaced D4260 with proper symbol (instead of table)
04/30/07 -- FW Port Power: Updated U4210 to 353S1744 for AVL updates
05/01/07 -- Current Sensors: Changed R5425/35/45 to RES_SENSE symbol which implements kelvin sensing without the need for XW shorts
0.1.2:
05/08/07 -- SB Decoupling: Changed C2703 to 138S0578 per Intel recommendations (rdar://5185100)
05/08/07 -- GPU Straps: Stuffed R8728 to put GPU PEG I/F into mobile mode (rdar://5188253)
0.2.0:
05/10/07 -- Thermal Sensors: Added SIGNAL_MODEL=EMPTY properties to thermal sense diff pairs (rdar://5192397)
05/10/07 -- Current Sensors: Added SIGNAL_MODEL=EMPTY properties to current sense diff pairs (rdar://5192397)
0.3.0:
05/14/07 -- Power Control: Added U7858,U7859 to properly enable/disable S5 regulators (rdar://TBD)
05/14/07 -- 5V/3.3V Regulators: Added C7307,C7308 to allow soft-start control of S5 regulators (rdar://TBD)
0.4.0:
05/22/07 -- Power Control: Added C7858 to decouple U7858/59
05/22/07 -- GPU Vcore: Removed Power Control circuitry
05/22/07 -- GPU Straps: Added R8734 to get PCIDEVID3 pullup
0.5.0:
06/06/07 -- GPU FB: Reassigned CS1/BA2 for future memory expansion
06/06/07 -- GPU FB: Changed 22uF, 0805 caps to 10uF, 0603 for future memory expansion
06/06/07 -- GPU FB: Reworked/added FB device Vrefs (with smaller FETs) for future memory expansion
06/06/07 -- Left Clutch I/C: Removed SIM I/F connector
0.6.0:
06/07/07 -- GPU Straps: U8700 changed to TS3V340 only
06/18/07 -- GPU FB: Added support for 1Gb density ICs (added MA<12> and CS1)
06/18/07 -- Left Clutch I/C: Added alternate camera connections (CCP2 I/F)
06/18/07 -- DFM: Added NC nets to allow copper on BGA corner balls (CPU and GPU)
06/19/07 -- GPU FB: Added 4 more 16Mx32 VRAM devices
06/20/07 -- Muxed Gfx: Began removing support for this feature
0.7.0:
06/25/07 -- GPU VCORE: U8900 Changed to IMVP6
06/25/07 -- FB REGULATOR: Added U9300
06/25/07 -- Muxed Gfx: Removed LVDS/BKLT muxes and support
06/25/07 -- Power Fet: Removed 1V8 and 1V25 Fets
06/25/07 -- Current Sense: Removed U5410 NBGfx Sense
06/25/07 -- Regulators: Changed Q7320,Q7360,Q7410,Q7460,Q7620 to SI7110N
0.8.0:
06/27/07 -- Power Fet: Removed 1v8 S0 Fet, cleaned up aliasing
0.9.0:
06/27/07 -- Current Sense: Added 1v8 FB current sense
06/27/07 -- GPU VCORE: Added additional High side Input Cap
0.10.0:
06/27/07 -- MUX Gfx: Delete GPU PGOOD Monitor
0.11.0:
06/27/07 -- Aliasing:Cleanup
06/27/07 -- BOM: Changed BOM option table for M87
0.12.0:
07/02/07 -- Power CTL:Added 1.25 PGOOD/3V3 GPU EN,Moved 1V8_S3 to pgood chain
07/02/07 -- LCC: Added Camera/MIC pins
07/02/07 -- DVI: Removed SB Hotplug Detect support(muxed gfx)
0.13.0:
07/05/07 -- Aliasing: Moved pages back in sync with T9, aliasing now on separate page
07/05/07 -- Regulators: Changed L7100,L7101 to 4mm 152S0433
1.2.0:
08/02/07 -- USB: Change to active enable USB ports
08/02/07 -- Regulators: Changed U8900 to use VID instead of Feedback resistors

EVT

4.1.0:
08/09/07 -- Current Sense: Change Q5322 TO FDN337 to accommodate TH1H
08/09/07 -- Ethernet: Change T3900,T3901 to 157S0053
5.1.0:
08/13/07 -- Regulators: Change GPUVCORE VID pullup/pulldowns to 2.2K

DVT

10.0.0:
09/21/07 -- BOM OPTION: Add 2.4Ghz 256MB VRAM Config, change 2.5Ghz Conifgs to 512MB VRAM

Revision History

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0

SCALE	SHT	OF
NONE	6	89

Functional Test Points

Fan Connectors

FUNC_TEST

TRUE	=PP5V_S0_FAN_LT	8 52
TRUE	FAN_LT_PWM	52
TRUE	FAN_LT_TACH	52
TRUE	FAN_RT_PWM	52
TRUE	FAN_RT_TACH	52

LPC+ Debug Connector

FUNC_TEST

TRUE	=PP3V3_S5_LPCPLUS	8 47
TRUE	=PP5V_S0_LPCPLUS	8 47
TRUE	LPC_AD<0>	23 45 47
TRUE	LPC_AD<1>	23 45 47
TRUE	LPC_FRAME_L	23 45 47
TRUE	PM_CLKRUN_L	25 45 47
TRUE	BOOT_LPC_SPI_L	24 47
TRUE	SMC_TMS	45 46 47
TRUE	DEBUG_RESET_L	28 47
TRUE	SMC_TRST_L	45 47
TRUE	SMC_TDO	45 46 47
TRUE	SMC_MD1	45 47
TRUE	SMC_TX_L	43 45 46 47
TRUE	FWH_INIT_L	47
TRUE	PCI_CLK33M_LPCPLUS	30 47 85
TRUE	LPC_AD<2>	23 45 47
TRUE	LPC_AD<3>	23 45 47
TRUE	INT_SERIRQ	25 45 47
TRUE	PM_SUS_STAT_L	25 45 46 47
TRUE	SMC_TDI	45 46 47
TRUE	SMC_TCK	45 46 47
TRUE	SMC_RESET_L	45 46 47
TRUE	SMC_NMI	45 47
TRUE	SMC_RX_L	43 45 46 47
TRUE	LINDACARD_GPIO	25 47

Left ALS Connector

FUNC_TEST

TRUE	=PP3V3_S3_LTALS	8 79
TRUE	ALS_GAIN	45 53 79
TRUE	LTALS_OUT	53 79
TRUE	GND	

Thermal Diode Connectors

FUNC_TEST

E55	TRUE	HSTHMSNS_D_P	51 88
E55	TRUE	HSTHMSNS_D_N	51 88
	TRUE	RSFSTHMSNS_D_P	51 88
	TRUE	RSFSTHMSNS_D_N	51 88
		CPUTHMSNS_D2_P	51 88
		CPUTHMSNS_D2_N	51 88

CPUTHMSNS can not be supported due to layout constraints

Battery Digital Connector

FUNC_TEST

TRUE	SMC_BS_ALRT_L	45 46 56
TRUE	=SMBUS_BATT_SCL	48 56
TRUE	=SMBUS_BATT_SDA	48 56
TRUE	GND_BATT	56

Left I/O Power Connector

FUNC_TEST

TRUE	=PPBUS_G3H_LIO_CONN	8 56
TRUE	GND	

Request for at least 10 GND test points

NOTE: 10 additional GND test points are called out separately in these notes.

RTC Battery Connector

FUNC_TEST

TRUE	PPVBATT_G3_RTC	28
TRUE	GND	

Current Sense Calibration

FUNC_TEST

TRUE	ISENSE_CAL_EN	45 49
TRUE	=PP5V_S0_ISENSECAL	8 49
TRUE	=PPVCORE_S0_CPU_REG	8 49 58
TRUE	=PPVCORE_GPU_REG	8 49 73
TRUE	GND	

2 TPs per

6 TPs, 2 with each of above TP pairs

Left Clutch Barrel Connector

FUNC_TEST

TRUE	=PP5V_S3_CAMERA	8 44
TRUE	USB_CAMERA_N	24 44 83
TRUE	USB_CAMERA_P	24 44 83
TRUE	=PP5V_S3_WWAN	8

Other Func Test Points

FUNC_TEST

TRUE	PM_SYSRST_L	25 28 45
TRUE	SMC_ONOFF_L	45 46 79

System Validation TPs

FUNC_TEST

TRUE	CPU_PWRGD	10 13 23 80
TRUE	CPU_DPSLP_L	7 10 23 80
TRUE	PM_DPRSLPVR	16 25 58 80
TRUE	CPU_DPSLP_L	7 10 23 80
TRUE	PM_LAN_ENABLE	25 45
TRUE	PCI_RST_L	24 28
TRUE	PM_RSMRST_L	25 45
TRUE	PM_SB_PWROK	9 25 28
TRUE	SB_RTC_RST_L	23 28
TRUE	PM_STPCPU_L	25 29 30
TRUE	PM_STPPCI_L	25 29 30
TRUE	VR_PWRGD_CLKEN	25 28
TRUE	VR_PWRGOOD_DELAY	9 16 28 58
TRUE	FSB_CPURST_L	10 13 14 80
TRUE	FSB_CPUSLP_L	10 14 80
	FSB_DPWR_L	10 14 80
TRUE	NB_SB_SYNC_L	16 25

FUNC_TEST

TRUE	IMVP_VR_ON	45 58
TRUE	IMVP_DPRSLPVR	58 80
TRUE	PM_SLP_S3_L	25 36 40 45 64
TRUE	PM_S4_STATE_L	25 45 64
TRUE	PM_SLP_S5_L	25 45 46
TRUE	PM_ENET_EN	36 64
TRUE	P1V8P1V5P1V05S0_PGOOD	64
TRUE	CPU_DPRSTP_L	10 16 23 58 80
TRUE	IMVP6_VID<6..0>	12 58 80
TRUE	PLT_RST_L	24 28
	NB_RESET_L	16 28
TRUE	GPU_RESET_L	28 65
TRUE	SMC_LRESET_L	28 45
TRUE	CPU_STPCLK_L	10 23 80
TRUE	FSB_CLK_NB_P	14 30 85
TRUE	FSB_CLK_NB_N	14 30 85
TRUE	NB_CLKREQ_L	16 29
TRUE	NB_CLK100M_PCIE_P	16 30 85
TRUE	NB_CLK100M_PCIE_N	16 30 85

TRUE	CPU_THERMTRIP_R	23

ICT Test Points

CPU FSB NO_TESTs

NO_TEST

TRUE	FSB_A_L<31..3>	10 14 80
TRUE	FSB_ADS_L	10 14 80
TRUE	FSB_ADSTB_L<1..0>	10 14 80
TRUE	FSB_BNR_L	10 14 80
TRUE	FSB_BREQ0_L	10 14 80
TRUE	FSB_D_L<63..0>	10 14 80
TRUE	FSB_DBSY_L	10 14 80
TRUE	FSB_DINV_L<3..0>	10 14 80
TRUE	FSB_DRDY_L	10 14 80
TRUE	FSB_DSTB_L_N<3..0>	10 14 80
TRUE	FSB_DSTB_L_P<3..0>	10 14 80
TRUE	FSB_HIT_L	10 14 80
TRUE	FSB_HITM_L	10 14 80
TRUE	FSB_LOCK_L	10 14 80
TRUE	FSB_REQ_L<4..0>	10 14 80

GPU NO_TESTs

NB NO_TESTs

NO_TEST

TRUE	NC_NB_NC<1..16>	TP_NB_NC<1..16> 16

Functional / ICT Test

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 7 OF 89	

"G3Hot" (Always-Present) Rails

=PPBUS_G3H_LIO_CONN
PPBUS_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPBUS_S5_FWPWRSW
=PPBUS_S5_P1V25S0FET
=PPVIN_S5_CPU_IMVP_VIN
=PPVIN_S5_CPU_IMVP
=PPVIN_S5_P5VP3V3
=PPVIN_S5_P5VS5
=PPVIN_S5_P3V3S5
=PPVIN_ENET_P1V25ENET
=PPVIN_S3_P1V8S3
=PPVIN_S0_P1V5S0
=PPVIN_S0_P1V8FB
=PPVIN_S0_P1V05S0
=PPVIN_GPU_GPUVCORE

=PPDCIN_G3H_LIO_CONN
PPDCIN_G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V
MAKE_BASE=TRUE
=PPVIN_G3H_P3V42G3H

=PP3V42_G3H_REG
PP3V42_G3H
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.42V
MAKE_BASE=TRUE
=PP3V42_G3H_SB_RTC
=PP3V42_G3H_LIO
=PP3V42_G3H_SMCUSBMUX
=PP3V42_G3H_SMBUS_SMC_BSA
=PP3V42_G3H_LIDSWITCH
=PP3V3_S5_SMC
=PP3V3_S5_LPCPLUS
=PPVIN_S5_SMCVREF
=PP3V42_G3H_PWRCTL

5V Rails

=PP5V_S5_REG
PP5V_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S5_SB
=PP5V_S5_P1V8FB
=PP5V_S5_P1V25S0FET
=PP5V_S5_P1V25ENET
=PP5V_S5_P1V05S0
=PP5V_S5_P1V8DDRREG
=PP5V_S5_PWRCTL
=PP5V_S5_GPUVCORE
=PP5V_S3_RTUSB
=PP5V_S3_P5VS3FET
=PP5V_S0_P5VS0FET

=PP5V_S3_FET
PP5V_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S3_SYSLED
=PP5V_S3_CAMERA
=PP5V_S3_WWAN
=PP5V_S3_IR
=PP5V_S3_TOPCASE
=PP5V_S0_KBDLED
=PP5V_S0_ISENSECAL
=PP5V_S5_P1V5S0

=PP5V_S0_FET
PP5V_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S0_SB
=PP5V_S0_ODD
=PP5V_S0_LPCPLUS
=PP5V_S0_FAN_LT
=PP5V_S0_FAN_RT
=PP5V_S0_CPU_IMVP
=PP5V_S0_DVI_DDC
=PP5V_S0_HDD
=PP5V_S0_ODDPWREN
=PP5V_S0_PCIREQFIX
=PP5V_S0_MIC

Chipset "VCore" Rails

=PPVCORE_S0_CPU_REG
PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.3 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
=PPVCORE_S0_CPU

=PPVCORE_S0_NB_GFX

3.3V-2.5V Rails

=PP3V3_S5_REG
PP3V3_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S5_SB_PM
=PP3V3_S5_SB_USB
=PP3V3_S5_SB
=PP3V3_S5_SB_CLINK1
=PP3V3_S5_SB_GPIO
=PP3V3_S5_SB_3V3_VCCSUSHDA
=PP3V3_S5_SB_VCCSUS3_3
=PP3V3_S5_SB_VCCSUS3_3_USB
=PP3V3_S5_S5PWRGD
=PP3V3_S5_SMBUS_SB_ME
=PP3V3_S5_ROM
=PP3V3_S5_P1V5P1V05PG
=PP3V3_S3_P3V3S3FET
=PP3V3_S0_LCD
=PP3V3_S0_P3V3S0FET
=PP3V3_GPU_P3V3GPUFET
=PP3V3_S5_PWRCTL

=PP3V3_S3_FET
PP3V3_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S3_P3V3ENETFET
=PP3V3_S3_FW
=PP3V3_S3_PCI
=PP3V3_S3_SMBUS_SMC_A_S3
=PP3V3_S3_RTALS
=PP3V3_S3_SMS
=PP3V3_S3_SMBUS_SMC_MGMT
=PP3V3_S3_P1V8ISNS
=PP3V3_S3_LTALS
=PP3V3_S3_TOPCASE
=PP3V3_S3_REMTHMSNS
=PP3V3_S3_PWRCTL

=PP3V3_S0_FET
PP3V3_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S0_NB_VCCHV
=PP3V3_S0_NB_VCCA_PEG_BG
=PP3V3_S0_NB_FOLLOW
=PP3V3_S0_SB_GPIO
=PP3V3_S0_SB_PCI
=PP3V3_S0_SB_VCC3_3_IDE
=PP3V3_S0_SB_VCC3_3_PCI
=PP3V3R1V5_S0_SB_VCCHDA
=PP3V3_S0_SB_VCC3_3_DMI
=PP3V3_S0_SB_VCC3_3_VCCPCORE
=PP3V3_S0_SB_VCCGLAN3_3
=PP3V3_S0_SB_VCC3_3_SATA
=PP3V3_S0_SB
=PP3V3_S0_SB_PM
=PP3V3_S0_RSTBUF
=PP3V3_S0_CK505
=PP3V3_S0_IDE
=PP3V3_S0_SMC
=PP3V3_S0_LPCPLUS
=PP3V3_S0_SMBUS_SB
=PP3V3_S0_SMBUS_SMC_B_S0
=PP3V3_S0_CPUCOREISNS
=PP3V3_S0_GPU1V8ISNS
=PP3V3_S0_CPUTHMSNS
=PP3V3_S0_GPUTHMSNS
=PP3V3_S0_FAN_LT
=PP3V3_S0_FAN_RT
=PP3V3_S0_IMVP
=PP3V3_S0_NBCOREISNS
=PP3V3_S0_ALLSYSPG
=PP3V3_S0_DDC_LCD
=PP3V3R5V_GPU_GPUISENS
=PP3V3_S0_XDP
=PP3V3_S0M_CK505
=PPSPD_S0M_MEM_A
=PPSPD_S0M_MEM_B
=PP3V3_S0MWOL_SB_CLINK0
=PP3V3_S0MWOL_SB_VCCCL3_3
=PP3V3_S0MWOL_SB_VCCLAN3_3
=PP3V3_S0_PWRCTL
=PP3V3_S0_CCP2
=PP3V3_S0_P1V25ISNS

=PP1V25_S0_FET
PP1V25_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
=PP1V25_S0_ISNS_R

1.8V-0.9V Rails

=PP1V8_S3_REG
PP1V8_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP1V8_S3_FW
=PP1V8_S3M_MEM_A
=PP1V8_S3M_MEM_B
=PP1V8_S3_ISNS_R

=PP1V8_S3_ISNS
PP1V8_S3_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP1V8_S3M_NB_VCC
=PP1V8_S3M_MEM_NB

=PP1V5_S0_REG
MAX I = ?.??A
PP1V5_S0
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S0_CPU
=PP1V5_S0_NB_TVDAC
=PP1V5_S0_SB
=PP1V5_S0_SB_VCC1_5_A_ARX
=PP1V5_S0_SB_VCC1_5_A_ATX
=PP1V5_S0_SB_VCC1_5_A
=PP1V5_S0_SB_VCCUSBPLL
=PP1V5_S0_SB_VCC1_5_A_USB_CORE
=PP1V5_S0_LIO

=PP1V25_S0_ISNS
PP1V25_S0_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
=PP1V25_S0M_NB_PLL
=PP1V25_S0M_NB_VCC
=PP1V25_S0M_NB_VCCA
=PP1V25_S0_NB_VCCDMI
=PP1V25_S0_NB_PLL
=PP1V25_S0_NB_VCC
=PP1V25_S0_SB_DMI
=PP1V2_GPU_PEX_IOVDDQ
=PP1V2_GPU_PEX_IOVDD
=PP1V2_GPU_PEX_PLLXVDD
=PP1V2_GPU_PLLVDD
=PP1V2_GPU_H_PLLVDD
=PP1V2_GPU_VID_PLLVDD
=PP1V2_GPU_FBPLLAVDD

=PP1V05_S0_REG
PP1V05_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0M_NB_VCCAXM
=PP1V05_S0_CPU
=PP1V05_S0_NB_FOLLOW
=PP1V05_S0_NB_PCIE
=PP1V05_S0_SB_CPU_IO
=PP1V05_S0_SMC_LS
=PP1V25R1V05_S0_FSB_NB
=PP1V25R1V05_S0_NB_VTT
=PPVCORE_S0_NBCOREISNS
=PPVCORE_S0_NB_FOLLOW
=PPVCORE_S0_SB

=PPVCORE_S0_NB_R
PPVCORE_S0_NB_R
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
=PPVCORE_S0_NB

=PP0V9_S3_VTTR_BUF
PP0V9_S3_MEM_VREF
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
=PP0V9_S3M_MEM_NBVREFA
=PP0V9_S3M_MEM_NBVREFB
=PP0V9_S3M_MEM_DIMMVREFA
=PP0V9_S3M_MEM_DIMMVREFB

=PP0V9_S0_VTT_LDO
PP0V9_S0
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
=PP0V9_S0M_MEM_TERM

"ENET" Rails

=PP3V3_ENET_FET
PP3V3_ENET
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_ENET_PHY
=PP3V3_ENET_AVDDLDO

=PPVOUT_ENET_AVDDLDO
PP1V9_ENET
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.9V
MAKE_BASE=TRUE
=PP1V8R2V5_ENET_PHY

=PP1V25_ENET_REG
PP1V25_ENET
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
=PP1V2_ENET_PHY
=PP1V25_S0_P1V25S0FET

=YUKON_EC_PP2V5_ENET
Yukon EC will not be supported

"FW" (FireWire) Rails

=PPBUS_FW_FWPWRSW_F
MAKE_BASE=TRUE
=PPBU_S0_P3V3FW

=PPBUS_S5_FW_FET
PPVP_FW
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.3 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PPVP_FW_SUMNODE
=PPVP_FW_CPS
=PPVP_FW_P3V3FW

=PPVP_FW_PORTA_UF
MAKE_BASE=TRUE
=PPVP_FW_PORT0

=PPVP_FW_PORTB_UF
MAKE_BASE=TRUE
=PPVP_FW_PORT1

=PP3V3_FW_REG
PP3V3_FW
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_FW_PHY
=PP3V3_FW_LATEVG_ACTIVE
=PP3V3_FW_LATEVG
=PPVIN_FW_P1V95FW

=PP1V95_FW_LDO
PP1V95_FW
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.95V
MAKE_BASE=TRUE
=PP1V95_FW_PHY
=PP1V8_FW_PHYOSC

"GPU" Rails

=PP3V3_S0GPU_FET
PP3V3_S0GPU
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_GPU_VDD33
=PP3V3_GPU_MIO
=PP3V3_GPU_DAC
=PP3V3_GPU_DVI
=PP3V3_GPU_VGASYNC
=PP3V3_GPU_TMDS
=PP3V3_GPU_VIDEOMUX
=PP3V3_GPU_SMBUS_SMC_0_S0
=PP3V3_GPU_PWRCTL
=PP3V3_GPU_VCORELOGIC
=PP3V3_GPU_HDCP

=PP3V3_S0GPU_TMDS_FET
PP3V3_S0GPU_TMDS
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_GPU_TMDSBIAS
=PP3V3_GPU_IFPCD_IOVDD

=PP1V8_S0GPU_ISNS
PP1V8_S0GPU_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP1V8_GPU_FB_VDD
=PP1V8_GPU_FB_VDDQ
=PP1V8_GPU_FBVDDQ
=PP1V8_GPU_FBIO
=PP1V8_GPU_IFPX

=PPVCORE_GPU_REG
PPVCORE_GPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
MAKE_BASE=TRUE
=PPVCORE_GPU

=PP1V8_S0GPU_REG
PP1V8_S0GPU_ISNS_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP1V8_S0GPU_ISNS_R

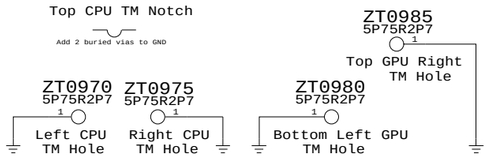
Power Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 8 OF 89	

Thermal Module Holes



RAM Door (Torx) Holes

ZT0930 3P7R3P2 — GND_CHASSIS_RAMDOOR_HOLE_0

ZT0935 3P7R3P2 — GND_CHASSIS_RAMDOOR_HOLE_1

Frame Holes

ZT0920 3P2R2P7 — GND_CHASSIS_LVDS_HOLE

ZT0940 3P7R3P2 — GND_CHASSIS_RIGHT_FAN_HOLE

Board Edge Notches (Can't be PTH)

ZT0945 HOLE-VIA-P5RP25 — GND_CHASSIS_RIGHT_FAN_NOTCH

ZT0950 HOLE-VIA-P5RP25 — GND_CHASSIS_DIMM_NOTCH

ZT0955 3P2R2P7 — GND_CHASSIS_LIOFLEX_HOLE

ZT0965 3P2R2P7 — GND_CHASSIS_LINDACARD_HOLE

Tooling Holes (Can't be PTH)

ZT0960 HOLE-VIA-P5RP25 — GND_CHASSIS_BATTCONN_HOLE

ZT0990 HOLE-VIA-P5RP25 — GND_CHASSIS_DVI_HOLE

SH0925 0G-503040 SHLD-SM-LF

EXTGPU_PWR_EN (23) — TP_EXTGPU_PWR_EN (MAKE_BASE=TRUE)

TP_USB_EXTDP (MAKE_BASE=TRUE) — USB_EXTD_P (24 83)

TP_USB_EXTDN (MAKE_BASE=TRUE) — USB_EXTD_N (24 83)

PM_SB_PWROK (28 25 7) — =SB_CLINK_MPWROK (25)

VR_PWRGOOD_DELAY (58 28 16 7) — =NB_CLINK_MPWROK (16)

SMC_SMS_INT (54) — =SMC_SMS_INT (45)

PEG_CLK100M_GPU_P (65 30) — PEG_CLK100M_P (85)

PEG_CLK100M_GPU_N (65 30) — PEG_CLK100M_N (85)

TP_MEM_A_A<15> — MEM_A_A<15> (31)

TP_MEM_B_A<15> — MEM_B_A<15> (32)

TP_USB_EXTCP — USB_EXTC_P (24 83)

TP_USB_EXTCN — USB_EXTC_N (24 83)

INT_PIRQE_L (84 24) — IPHS_SW_INT (34)

SB_SLOAD (25) — IPHS_SW_BIAS_EN_L (34)

Digital Ground

GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

Signal Aliases

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/23/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 9 OF 89	

OMIT

U1000
PENRYN
FCBGA
1 OF 4

ADDR GROUP0
FSB_A_L<3> J4 A3*
FSB_A_L<4> L5 A4*
FSB_A_L<5> L4 A5*
FSB_A_L<6> K5 A6*
FSB_A_L<7> M3 A7*
FSB_A_L<8> N2 A8*
FSB_A_L<9> J1 A9*
FSB_A_L<10> N3 A10*
FSB_A_L<11> P5 A11*
FSB_A_L<12> P2 A12*
FSB_A_L<13> L2 A13*
FSB_A_L<14> P4 A14*
FSB_A_L<15> P1 A15*
FSB_A_L<16> R1 A16*
FSB_ADSTB_L<0> M1 ADSTB0*

REQ0*
FSB_REQ_L<0> K3
FSB_REQ_L<1> H2 REQ1*
FSB_REQ_L<2> K2 REQ2*
FSB_REQ_L<3> J3 REQ3*
FSB_REQ_L<4> L1 REQ4*

ADDR GROUP1
FSB_A_L<17> Y2 A17*
FSB_A_L<18> U5 A18*
FSB_A_L<19> R3 A19*
FSB_A_L<20> W6 A20*
FSB_A_L<21> U4 A21*
FSB_A_L<22> Y5 A22*
FSB_A_L<23> U1 A23*
FSB_A_L<24> R4 A24*
FSB_A_L<25> T5 A25*
FSB_A_L<26> T3 A26*
FSB_A_L<27> W2 A27*
FSB_A_L<28> W5 A28*
FSB_A_L<29> Y4 A29*
FSB_A_L<30> U2 A30*
FSB_A_L<31> V4 A31*
FSB_A_L<32> W3 A32*
FSB_A_L<33> AA4 A33*
FSB_A_L<34> AB2 A34*
FSB_A_L<35> AA3 A35*
FSB_ADSTB_L<1> V1 ADSTB1*

ICH
CPU_A20M_L A6 A20M*
CPU_FERR_L A5 FERR*
CPU_IGNNE_L C4 IGNNE*
CPU_STPCLK_L D5 STPCLK*
CPU_INTR C6 LINT0
CPU_NMI B4 LINT1
CPU_SMI_L A3 SMI*

RESERVED
TP_CPU_RSVD0 M4 RSVD0
TP_CPU_RSVD1 N5 RSVD1
TP_CPU_RSVD2 T2 RSVD2
TP_CPU_RSVD3 V3 RSVD3
TP_CPU_RSVD4 B2 RSVD4
TP_CPU_RSVD5 F6 RSVD5
TP_CPU_RSVD6 D2 RSVD6
TP_CPU_RSVD7 D22 RSVD7
TP_CPU_RSVD8 D3 RSVD8

CONTROL
ADS* H1 FSB_ADS_L
BNR* E2 FSB_BNR_L
BPRI* G5 FSB_BPRI_L
DEFER* H5 FSB_DEFER_L
DRDY* F21 FSB_DRDY_L
DBSY* E1 FSB_DBSY_L
BR0* F1 FSB_BREQ0_L
IERR* D20 CPU_IERR_L
INIT* B3 CPU_INIT_L
LOCK* H4 FSB_LOCK_L
RESET* C1 FSB_CPURST_L
RS0* F3 FSB_RS_L<0>
RS1* F4 FSB_RS_L<1>
RS2* G3 FSB_RS_L<2>
TRDY* G2 FSB_TRDY_L
HIT* G6 FSB_HIT_L
HITM* E4 FSB_HITM_L

XDP/ITP SIGNALS
BPM0* AD4 XDP_BPM_L<0>
BPM1* AD3 XDP_BPM_L<1>
BPM2* AD1 XDP_BPM_L<2>
BPM3* AC4 XDP_BPM_L<3>
PRDY* AC2 XDP_BPM_L<4>
PREQ* AC1 XDP_BPM_L<5>
TCK AC5 XDP_TCK
TDI AA6 XDP_TDI
TDO AB3 XDP_TDO
TMS AB5 XDP_TMS
TRST* AB6 XDP_TRST_L
DBR* C20 XDP_DBRESET_L

THERMAL
PROCHOT* D21 CPU_PROCHOT_L
THERMDA A24 CPU_THERMD_P
THERMDC B25 CPU_THERMD_N
THERMTRIP* C7 PM_THRMTRIP_L

H CLK
BCLK0 A22 FSB_CLK_CPU_P
BCLK1 A21 FSB_CLK_CPU_N

=PP1V05_S0_CPU
R1002 54.9 1% 1/16W MF-LF 402
PLACE TESTPOINT ON FSB_IERR_L WITH A GND 0.1" AWAY

=PP1V05_S0_CPU
R1003 54.9 1% 1/16W MF-LF 402
R1004 68 5% 1/16W MF-LF 402
PM_THRMTRIP# SHOULD CONNECT TO ICH AND GMCH WITHOUT T (NO STUB)

=PP1V05_S0_CPU
R1005 1K 1% 1/16W MF-LF 402
R1006 2.0K 1% 1/16W MF-LF 402
0.5" MAX LENGTH FOR CPU_GTLREF

CPU_GTLREF AD26 GTLREF
CPU_TEST1 C23 TEST1
CPU_TEST2 D25 TEST2
TP_CPU_TEST3 C24 TEST3
CPU_TEST4 AF26 TEST4
TP_CPU_TEST5 AF1 TEST5
TP_CPU_TEST6 A26 TEST6
TP_CPU_TEST7 C3 TEST7
CPU_BSEL<0> B22 BSEL0
CPU_BSEL<1> B23 BSEL1
CPU_BSEL<2> C21 BSEL2

NOSTUFF C1000 0.1uF 10V X5R 402
PLACE C1000 CLOSE TO CPU_TEST4 PIN. MAKE SURE CPU_TEST4 IS REFERENCED TO GND

R1020 54.9 1% 1/16W MF-LF 402 =PP1V05_S0_CPU
R1021 54.9 1% 1/16W MF-LF 402
R1024 54.9 1% 1/16W MF-LF 402
R1022 54.9 1% 1/16W MF-LF 402
R1023 649 1% 1/16W MF-LF 402
XDP_TMS
XDP_TDI
XDP_TDO
XDP_TCK
XDP_TRST_L
PLACEMENT_NOTE=Place R1024 near ITP connector (if present)

NOSTUFF R1030 0 5% 1/16W MF-LF 402
NOSTUFF R1012 1K 5% 1/16W MF-LF 402
NOSTUFF R1007 1K 5% 1/16W MF-LF 402

OMIT

U1000
PENRYN
FCBGA
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DATA GRP 0
FSB_D_L<0> E22 D0*
FSB_D_L<1> F24 D1*
FSB_D_L<2> E26 D2*
FSB_D_L<3> G22 D3*
FSB_D_L<4> F23 D4*
FSB_D_L<5> G25 D5*
FSB_D_L<6> E25 D6*
FSB_D_L<7> E23 D7*
FSB_D_L<8> K24 D8*
FSB_D_L<9> G24 D9*
FSB_D_L<10> J24 D10*
FSB_D_L<11> J23 D11*
FSB_D_L<12> H22 D12*
FSB_D_L<13> F26 D13*
FSB_D_L<14> K22 D14*
FSB_D_L<15> H23 D15*
FSB_DSTB_L_N<0> J26 DSTBN0*
FSB_DSTB_L_P<0> H26 DSTBP0*
FSB_DINV_L<0> H25 DINV0*

DATA GRP 2
DSTBN2* Y26 FSB_DSTB_L_N<2>
DSTBP2* AA26 FSB_DSTB_L_P<2>
DINV2* U22 FSB_DINV_L<2>

DATA GRP 1
FSB_D_L<16> N22 D16*
FSB_D_L<17> K25 D17*
FSB_D_L<18> P26 D18*
FSB_D_L<19> R23 D19*
FSB_D_L<20> L23 D20*
FSB_D_L<21> M24 D21*
FSB_D_L<22> L22 D22*
FSB_D_L<23> M23 D23*
FSB_D_L<24> P25 D24*
FSB_D_L<25> P23 D25*
FSB_D_L<26> P22 D26*
FSB_D_L<27> T24 D27*
FSB_D_L<28> R24 D28*
FSB_D_L<29> L25 D29*
FSB_D_L<30> T25 D30*
FSB_D_L<31> N25 D31*
FSB_DSTB_L_N<1> L26 DSTBN1*
FSB_DSTB_L_P<1> M26 DSTBP1*
FSB_DINV_L<1> N24 DINV1*

DATA GRP 3
D32* Y22 FSB_D_L<32>
D33* AB24 FSB_D_L<33>
D34* V24 FSB_D_L<34>
D35* V26 FSB_D_L<35>
D36* V23 FSB_D_L<36>
D37* T22 FSB_D_L<37>
D38* U25 FSB_D_L<38>
D39* U23 FSB_D_L<39>
D40* Y25 FSB_D_L<40>
D41* W22 FSB_D_L<41>
D42* Y23 FSB_D_L<42>
D43* W24 FSB_D_L<43>
D44* W25 FSB_D_L<44>
D45* AA23 FSB_D_L<45>
D46* AA24 FSB_D_L<46>
D47* AB25 FSB_D_L<47>
D48* AE24 FSB_D_L<48>
D49* AD24 FSB_D_L<49>
D50* AA21 FSB_D_L<50>
D51* AB22 FSB_D_L<51>
D52* AB21 FSB_D_L<52>
D53* AC26 FSB_D_L<53>
D54* AD20 FSB_D_L<54>
D55* AE22 FSB_D_L<55>
D56* AF23 FSB_D_L<56>
D57* AC25 FSB_D_L<57>
D58* AE21 FSB_D_L<58>
D59* AD21 FSB_D_L<59>
D60* AC22 FSB_D_L<60>
D61* AD23 FSB_D_L<61>
D62* AF22 FSB_D_L<62>
D63* AD23 FSB_D_L<63>
DSTBN3* AE25 FSB_DSTB_L_N<3>
DSTBP3* AF24 FSB_DSTB_L_P<3>
DINV3* AC20 FSB_DINV_L<3>

MISC
COMP0 R26 CPU_COMP<0>
COMP1 U26 CPU_COMP<1>
COMP2 AA1 CPU_COMP<2>
COMP3 Y1 CPU_COMP<3>
DPRSTP* E5 CPU_DPRSTP_L
DPSLP* B5 CPU_DPSLP_L
DPWR* D24 FSB_DPWR_L
PWRGOOD D6 CPU_PWRGD
SLP* D7 FSB_CPUSLP_L
PSI* AE6 CPU_PSI_L

R1016 27.4 1% 1/16W MF-LF 402
R1017 54.9 1% 1/16W MF-LF 402
R1018 27.4 1% 1/16W MF-LF 402
R1019 54.9 1% 1/16W MF-LF 402

LAYOUT NOTE:
COMP0,2 CONNECT WITH ZO=27.4OHM,
MAKE TRACE LENGTH SHORTER THAN 0.5".
COMP1,3 CONNECT WITH ZO=55OHM,
MAKE TRACE LENGTH SHORTER THAN 0.5".

CPU FSB

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

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SCALE: NONE	SHT 10 OF 89	

(CPU CORE POWER)
=PPVCORE_S0_CPU 8 11 12 49

Standard Voltage:	Low Voltage:	Ultra Low Voltage:
44.0 A (Design Target)	23.0 A (Design Target)	17.0 A (Design Target)
41.0 A (HFM)	21.0 A (HFM)	TBD A (HFM)
30.4 A (LFM)	18.7 A (LFM)	TBD A (LFM)
25.5 A (SuperLFM)	TBD A (SuperLFM)	
27.4 A (Auto-Halt/Stop-Grant HFM)	TBD A (Auto-Halt/Stop-Grant HFM)	TBD A (Auto-Halt/Stop-Grant HFM)
17.0 A (Auto-Halt/Stop-Grant SuperLFM)	TBD A (Auto-Halt/Stop-Grant SuperLFM)	TBD A (Auto-Halt/Stop-Grant LFM)
27.4 A (Sleep HFM)	TBD A (Sleep HFM)	TBD A (Sleep HFM)
16.8 A (Sleep SuperLFM)	TBD A (Sleep SuperLFM)	TBD A (Sleep LFM)
25.0 A (Deep Sleep HFM)	TBD A (Deep Sleep HFM)	TBD A (Deep Sleep HFM)
16.0 A (Deep Sleep SuperLFM)	TBD A (Deep Sleep SuperLFM)	TBD A (Deep Sleep LFM)
11.5 A (Deeper Sleep)	TBD A (Deeper Sleep)	TBD A (Deeper Sleep)
9.4 A (Enhanced Deeper Sleep)	TBD A (Enhanced Deeper Sleep)	TBD A (Enhanced Deeper Sleep)

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VCC: A7, A9, A10, A12, A13, A15, A17, A18, A20, B7, B9, B10, B12, B14, B15, B17, B18, B20, C9, C10, C12, C13, C15, C17, C18, D9, D10, D12, D14, D15, D17, D18, E7, E9, E10, E12, E13, E15, E17, E18, E20, F7, F9, F10, F12, F14, F15, F17, F18, F20, AA7, AA9, AA10, AA12, AA13, AA15, AA17, AA18, AA20, AB9, AB10, AB12, AB14, AB15, AB17, AB18

VCC: AB20, AB7, AC7, AC9, AC12, AC13, AC15, AC17, AC18, AD7, AD9, AD10, AD12, AD14, AD15, AD17, AD18, AE9, AE10, AE12, AE13, AE15, AE17, AE18, AE20, AF9, AF10, AF12, AF14, AF15, AF17, AF18, AF20

(CPU IO POWER 1.05V)
=PP1V05_S0_CPU 8 10 12 13

4500 mA (before VCC stable)
2500 mA (after VCC stable)

VCCP: G21, V6, J6, K6, M6, J21, K21, M21, N21, N6, R21, R6, T21, T6, V21, W21

(CPU INTERNAL PLL POWER 1.5V)
=PP1V5_S0_CPU 8 12

130 mA

VCCA: B26, C26

VID0	AD6	CPU_VID<0>	OUT 12 80
VID1	AF5	CPU_VID<1>	OUT 12 80
VID2	AE5	CPU_VID<2>	OUT 12 80
VID3	AF4	CPU_VID<3>	OUT 12 80
VID4	AE3	CPU_VID<4>	OUT 12 80
VID5	AF3	CPU_VID<5>	OUT 12 80
VID6	AE2	CPU_VID<6>	OUT 12 80
VCCSENSE	AF7	CPU_VCCSENSE_P	OUT 58 80
VSSSENSE	AE7	CPU_VCCSENSE_N	OUT 58 80

=PPVCORE_S0_CPU 8 11 12 49

R1100
100
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

R1101
100
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

OMIT
U1000
PENRYN
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VSS: A4, A8, A11, A14, A16, A19, A23, AF2, B6, B8, B11, B13, B16, B19, B21, B24, C5, C8, C11, C14, C16, C19, C2, C22, C25, D1, D4, D8, D11, D13, D16, D19, D23, D26, E3, E6, E8, E11, E14, E16, E19, E21, E24, F5, F8, F11, F13, F16, F19, F2, F22, F25, G4, G1, G23, G26, H3, H6, H21, H24, J2, J5, J22, J25, K1, K4, K23, K26, L3, L6, L21, L24, M2, M5, M22, M25, N1, N4, N23, N26, P3, B1

VSS: P6, P21, P24, R2, R5, R22, R25, T1, T4, T23, T26, U3, U6, U21, U24, V2, V5, V22, V25, W1, W4, W23, W26, Y3, Y6, Y21, Y24, AA2, AA5, AA8, AA11, AA14, AA16, AA19, AA22, AA25, AB1, AB4, AB8, AB11, AB13, AB16, AB19, AB23, AB26, AC3, AC6, AC8, AC11, AC14, AC16, AC19, AC21, AC24, AD2, AD5, AD8, AD11, AD13, AD16, AD19, AD22, AD25, AE1, AE4, AE8, AE11, AE14, AE16, AE19, AE23, AE26, A2, AF6, AF8, AF11, AF13, AF16, AF19, AF21, A25, AF25

CPU Power & Ground

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

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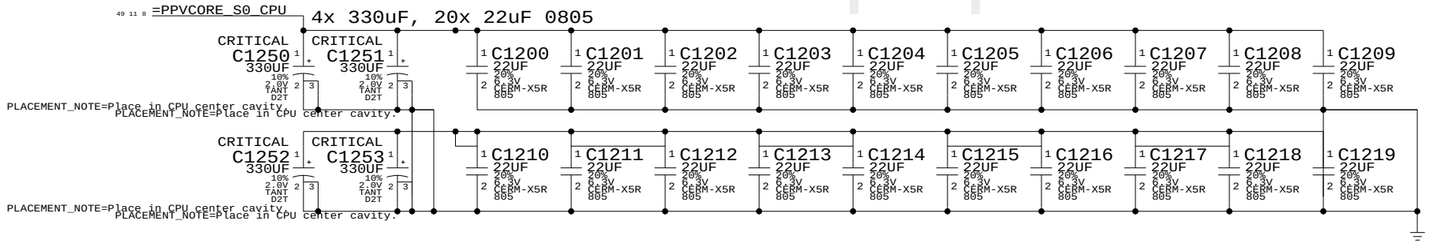
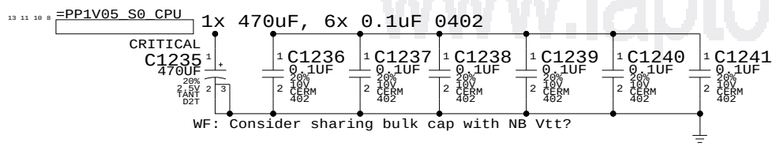
SCALE: NONE	SHT 11 OF 89	

Current numbers from Merom for Santa Rosa EMTS, doc #22221.

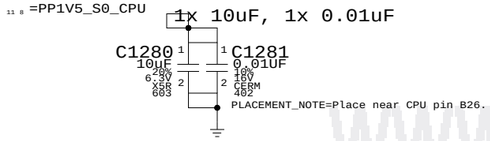
CPU VCORE HF AND BULK DECOUPLING



VCCP (CPU I/O) DECOUPLING



VCCA (CPU AVdd) DECOUPLING



CPU VCORE VID CONNECTIONS

80 11 CPU_VID<0..6> = IMVP6_VID<0..6> 7 58 80
MAKE_BASE=TRUE

CPU Decoupling & VID

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

APPLE INC.

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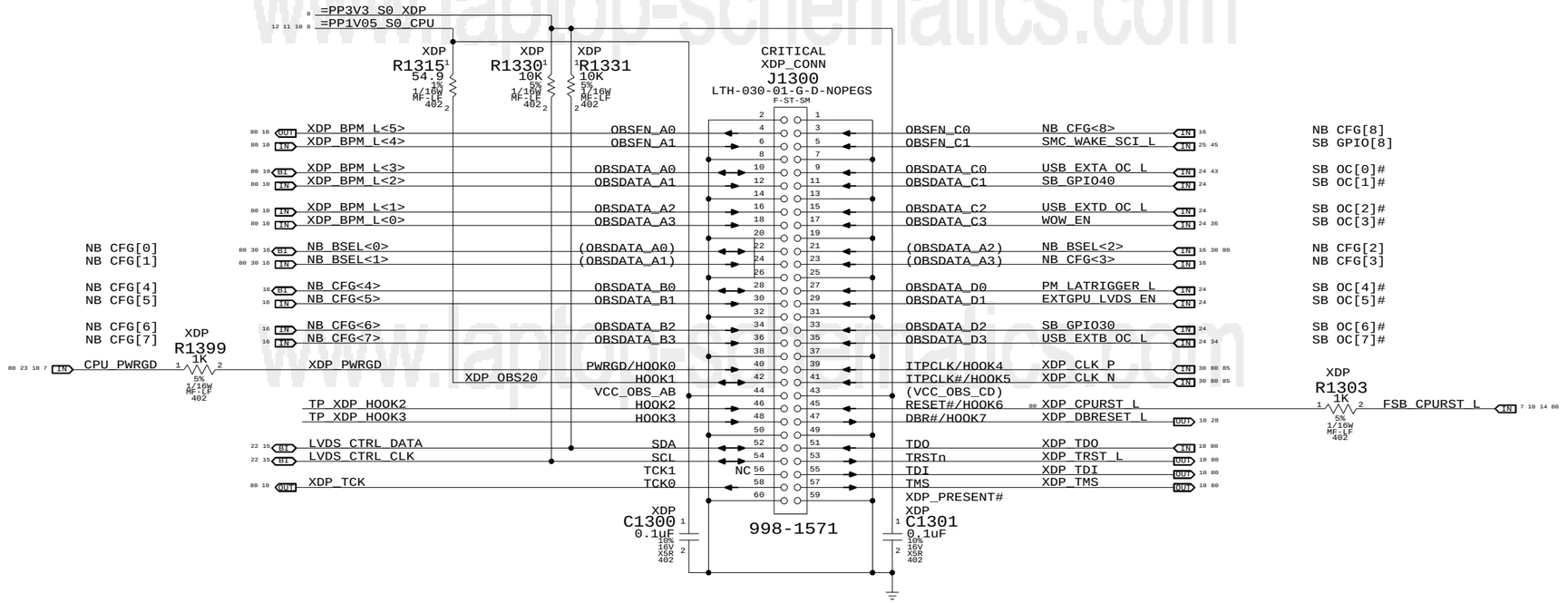
SCALE: NONE	SHT 12 OF 89	

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with 920-0451 adapter board to support CPU, NB & SB debugging.



Direction of XDP module

Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port (XDP)

SYNC_MASTER=T9_NOME SYNC_DATE=12/12/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
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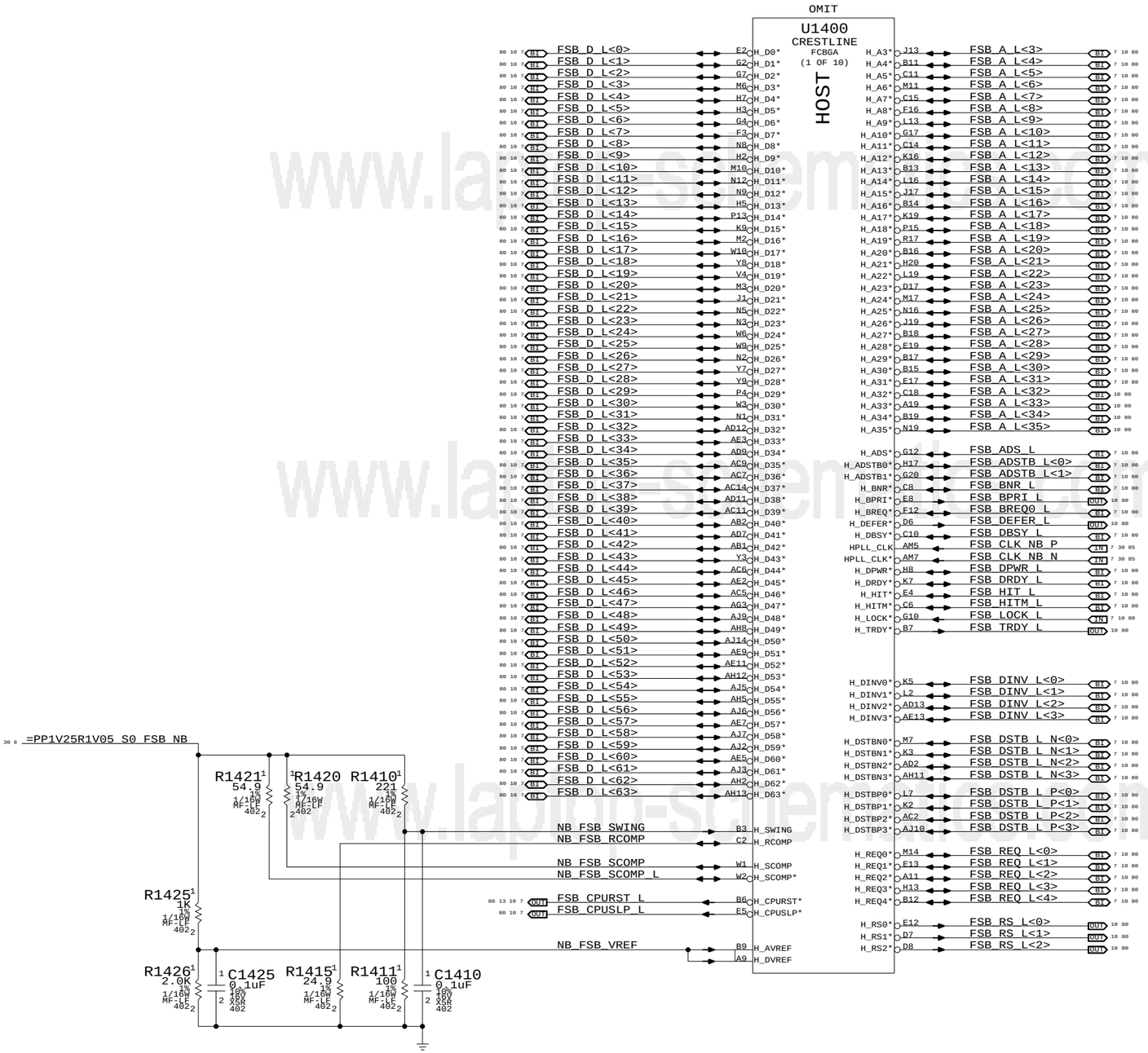
SCALE: NONE	SHT 13 OF 89	



NB CPU Interface

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

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SCALE: NONE	SHT 14 OF 89	

LVDS Disable

Can leave all signals NC if LVDS is not implemented.
Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

Note: SR DG says to tie LVDS_VREFH/L to GND. This causes a glitch during wake-up on LVDS DATA/CLK pairs. New recommendation is to float both signals, see Radar #5067636.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

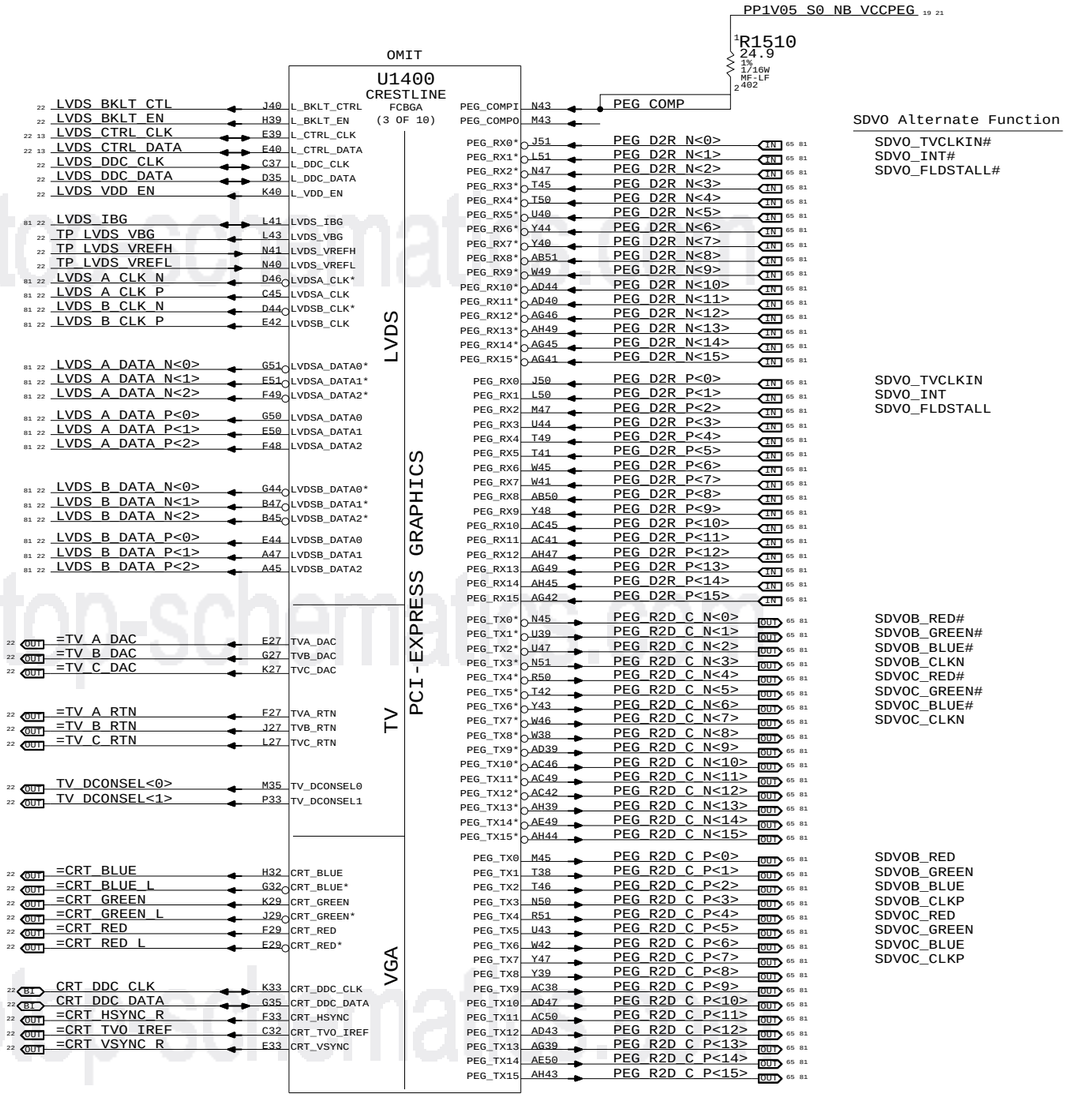
CRT & TV-Out Disable

Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TVO_IREF to GND.
Can tie the following rails to GND:
VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above.
Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and TV_DCONSELx to GND.
Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.



NB PEG / Video Interfaces

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
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NB_CFG<3>	RESERVED
NB_CFG<4>	RESERVED
NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2
NB_CFG<6>	RESERVED
NB_CFG<7>	RESERVED
NB_CFG<8>	RESERVED
NB_CFG<9> PCIe Graphics Lane Reversal	High = Normal Low = Reversed
NB_CFG<10>	RESERVED
NB_CFG<11>	RESERVED
NB_CFG<12>	See Below
NB_CFG<13>	See Below
NB_CFG<14>	RESERVED
NB_CFG<15>	RESERVED
NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled
NB_CFG<17>	RESERVED
NB_CFG<18>	RESERVED
NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal
NB_CFG<20> Concurrent SDVO/PCIe x1	High = Both active Low = Only SDVO or PCIe x16

NB_CFG<13:12>

00 = RESERVED
01 = XOR Mode Enabled
10 = All-Z Mode Enabled
11 = Normal Operation

NB_CFG<5> 13 16
NBCFG_DMI_X2
R1655 3.9K 5% 1/16W MF-LF 402

NB_CFG<9> 16
NBCFG_PEG_REVERSE
R1659 3.9K 5% 1/16W MF-LF 402

NB_CFG<16> 16
NBCFG_DYN_ODT_DISABLE
R1666 3.9K 5% 1/16W MF-LF 402

=PP3V3_S0_NB_VCCHV 8 16 19 21
NBCFG_DMI_REVERSE
R1669 3.9K 5% 1/16W MF-LF 402
NB_CFG<19> 16

=PP3V3_S0_NB_VCCHV 8 16 19 21
NBCFG_SDVO_AND_PCIE
R1670 3.9K 5% 1/16W MF-LF 402
NB_CFG<20> 16

NB CFG<8:0> used for debug access

NB CFG<13:12> require ICT access

21 19 16 8 =PP3V3_S0_NB_VCCHV
R1630 10K 5% 1/16W MF-LF 402
R1631 10K 5% 1/16W MF-LF 402
45 31 IN PM_EXTTS_L<0>
45 32 IN PM_EXTTS_L<1>

OMIT

U1400
CRESTLINE
FCBGA
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TP_NB_RSVD<1>	P36	RSVD1		
TP_NB_RSVD<2>	P37	RSVD2		
TP_NB_RSVD<3>	R35	RSVD3		
TP_NB_RSVD<4>	N35	RSVD4		
TP_NB_RSVD<5>	AR12	RSVD5		
TP_NB_RSVD<6>	AR13	RSVD6		
TP_NB_RSVD<7>	AM12	RSVD7		
TP_NB_RSVD<8>	AN13	RSVD8		
TP_NB_RSVD<9>	J12	RSVD9		
TP_NB_RSVD<10>	AR37	RSVD10		
TP_NB_RSVD<11>	AM36	RSVD11		
TP_NB_RSVD<12>	AL36	RSVD12		
TP_NB_RSVD<13>	AM37	RSVD13		
TP_NB_RSVD<14>	D20	RSVD14		
TP_NB_RSVD<20>	H10	RSVD20		
TP_NB_RSVD<21>	B51	RSVD21		
TP_NB_RSVD<22>	BJ20	RSVD22		
TP_NB_RSVD<23>	BK22	RSVD23		
TP_NB_RSVD<24>	BF19	RSVD24		
TP_NB_RSVD<25>	BH20	RSVD25		
TP_NB_RSVD<26>	BK18	RSVD26		
TP_NB_RSVD<27>	BJ18	RSVD27		
TP_MEM_CLKP2	BF23	SM_CK2		
TP_MEM_CLKN2	BG23	SM_CK2*		
TP_MEM_CLKP5	BC23	SM_CK5		
TP_MEM_CLKN5	BD24	SM_CK5*		
82 33 31 OUT MEM_A_A<14>	BJ29	SA_MA14		
82 33 32 OUT MEM_B_A<14>	BE24	SB_MA14		
TP_NB_RSVD<34>	BH39	RSVD34		
TP_NB_RSVD<35>	AW20	RSVD35		
TP_NB_RSVD<36>	BK20	RSVD36		
TP_LVDS_A_DATAN3	C48	RSVD37		
TP_LVDS_A_DATAP3	D47	RSVD38		
TP_LVDS_B_DATAN3	B44	RSVD39		
TP_LVDS_B_DATAP3	C44	RSVD40		
TP_NB_RSVD<41>	A35	RSVD41		
TP_NB_RSVD<42>	B37	RSVD42		
TP_NB_RSVD<43>	B36	RSVD43		
TP_NB_RSVD<44>	B34	RSVD44		
TP_NB_RSVD<45>	C34	RSVD45		
80 30 13 IN NB_BSEL<0>	P27	CFG0		
80 30 13 IN NB_BSEL<1>	N27	CFG1		
80 30 13 IN NB_BSEL<2>	N24	CFG2		
13 OUT NB_CFG<3>	C21	CFG3	IPU	CFG
13 OUT NB_CFG<4>	C23	CFG4	IPU	
16 13 BI NB_CFG<5>	F23	CFG5	IPU	
13 OUT NB_CFG<6>	N23	CFG6	IPU	
13 OUT NB_CFG<7>	G23	CFG7	IPU	
13 OUT NB_CFG<8>	J20	CFG8	IPU	
16 NB_CFG<9>	C20	CFG9	IPU	
TP_NB_CFG<10>	R24	CFG10	IPU	
TP_NB_CFG<11>	L23	CFG11	IPU	
TP_NB_CFG<12>	J23	CFG12	IPU	
TP_NB_CFG<13>	E23	CFG13	IPU	
TP_NB_CFG<14>	E20	CFG14	IPU	
TP_NB_CFG<15>	K23	CFG15	IPU	
16 NB_CFG<16>	M20	CFG16	IPU	
TP_NB_CFG<17>	M24	CFG17	IPU	
TP_NB_CFG<18>	L32	CFG18	IPD	
16 NB_CFG<19>	N33	CFG19	IPD	
16 NB_CFG<20>	L35	CFG20	IPD	
25 OUT PM_BMBUSY_L	G41	PM_BM_BUSY*		PM
80 58 23 10 7 IN CPU_DPRSTP_L	L39	PM_DPRSTP*		
	L36	PM_EXT_TS0*		
	J35	PM_EXT_TS1*		
58 28 9 7 IN VR_PWRGOOD_DELAY	AW49	PWROK		
28 7 IN NB_RESET_L	AV20	RSTIN*		
80 46 23 10 OUT PM_THRMTRIP_L	N20	THERMTRIP*		
80 58 25 7 IN PM_DPRSLPVR	G36	DPRSLPVR		
7 TP_NB_NC<1>	BJ51	NC1		NC
7 TP_NB_NC<2>	BK51	NC2		
7 TP_NB_NC<3>	BK50	NC3		
7 TP_NB_NC<4>	BL50	NC4		
7 TP_NB_NC<5>	BL49	NC5		
7 TP_NB_NC<6>	BL3	NC6		
7 TP_NB_NC<7>	BL2	NC7		
7 TP_NB_NC<8>	BK1	NC8		
7 TP_NB_NC<9>	BJ1	NC9		
7 TP_NB_NC<10>	E1	NC10		
7 TP_NB_NC<11>	A5	NC11		
7 TP_NB_NC<12>	C51	NC12		
7 TP_NB_NC<13>	B50	NC13		
7 TP_NB_NC<14>	A50	NC14		
7 TP_NB_NC<15>	A49	NC15		
7 TP_NB_NC<16>	BK2	NC16		

SM_CK0	AV29	MEM_CLK_P<0>	OUT 31 82
SM_CK1	BB23	MEM_CLK_P<1>	OUT 31 82
SM_CK3	BA25	MEM_CLK_P<3>	OUT 32 82
SM_CK4	AV23	MEM_CLK_P<4>	OUT 32 82
SM_CK0*	AW30	MEM_CLK_N<0>	OUT 31 82
SM_CK1*	BA23	MEM_CLK_N<1>	OUT 31 82
SM_CK3*	AW25	MEM_CLK_N<3>	OUT 32 82
SM_CK4*	AW23	MEM_CLK_N<4>	OUT 32 82
SM_CKE0	BE29	MEM_CKE<0>	OUT 31 33 82
SM_CKE1	AY32	MEM_CKE<1>	OUT 31 33 82
SM_CKE3	BD39	MEM_CKE<3>	OUT 32 33 82
SM_CKE4	BG37	MEM_CKE<4>	OUT 32 33 82
SM_CS0*	BG20	MEM_CS_L<0>	OUT 31 33 82
SM_CS1*	BK16	MEM_CS_L<1>	OUT 31 33 82
SM_CS2*	BG16	MEM_CS_L<2>	OUT 32 33 82
SM_CS3*	BE13	MEM_CS_L<3>	OUT 32 33 82
SM_ODT0	BH18	MEM_ODT<0>	OUT 31 33 82
SM_ODT1	BJ15	MEM_ODT<1>	OUT 31 33 82
SM_ODT2	BJ14	MEM_ODT<2>	OUT 32 33 82
SM_ODT3	BE16	MEM_ODT<3>	OUT 32 33 82
SM_RCOMP	BL15	MEM_RCOMP	
SM_RCOMP*	BK14	MEM_RCOMP_L	
SM_RCOMP_VOH	BK31	MEM_RCOMP_VOH	
SM_RCOMP_VOL	BL31	MEM_RCOMP_VOL	
SM_VREF0	AR49	=PP0V9_S3M_MEM_NBVREFA	IN 8
SM_VREF1	AW4	=PP0V9_S3M_MEM_NBVREFB	IN 8
DPLL_REF_CLK	B42	=NB_CLK96M_DOT_P	IN 22
DPLL_REF_CLK*	C42	=NB_CLK96M_DOT_N	IN 22
DPLL_REF_SSCLK	H48	=NB_CLK100M_DPLLSS_P	IN 22
DPLL_REF_SSCLK*	H47	=NB_CLK100M_DPLLSS_N	IN 22
PEG_CLK	K44	NB_CLK100M_PCIE_P	IN 7 30 85
PEG_CLK*	K45	NB_CLK100M_PCIE_N	IN 7 30 85
DMI_RXN0	AN47	DMI_S2N_N<0>	IN 24 81
DMI_RXN1	AJ38	DMI_S2N_N<1>	IN 24 81
DMI_RXN2	AN42	DMI_S2N_N<2>	IN 24 81
DMI_RXN3	AN46	DMI_S2N_N<3>	IN 24 81
DMI_RXP0	AM47	DMI_S2N_P<0>	IN 24 81
DMI_RXP1	AJ39	DMI_S2N_P<1>	IN 24 81
DMI_RXP2	AN41	DMI_S2N_P<2>	IN 24 81
DMI_RXP3	AN45	DMI_S2N_P<3>	IN 24 81
DMI_TXN0	AJ46	DMI_N2S_N<0>	OUT 24 81
DMI_TXN1	AJ41	DMI_N2S_N<1>	OUT 24 81
DMI_TXN2	AM40	DMI_N2S_N<2>	OUT 24 81
DMI_TXN3	AM44	DMI_N2S_N<3>	OUT 24 81
DMI_TXP0	AJ47	DMI_N2S_P<0>	OUT 24 81
DMI_TXP1	AJ42	DMI_N2S_P<1>	OUT 24 81
DMI_TXP2	AM39	DMI_N2S_P<2>	OUT 24 81
DMI_TXP3	AM43	DMI_N2S_P<3>	OUT 24 81
GFX_VID0	E35	GFX_VID<0>	OUT
GFX_VID1	A39	GFX_VID<1>	OUT 22
GFX_VID2	C38	GFX_VID<2>	OUT 22
GFX_VID3	B39	GFX_VID<3>	OUT 22
GFX_VR_EN	E36	GFX_VID<4>	OUT 22
		=GFX_VR_EN	OUT 22
CL_CLK	AM49	CLINK_NB_CLK	BI 25 84
CL_DATA	AK50	CLINK_NB_DATA	BI 25 84
CL_PWROK	AT43	=NB_CLINK_MPWROK	IN 9
CL_RST*	AN49	CLINK_NB_RESET_L	OUT 25 84
CL_VREF	AM50	84 NB_CLINK_VREF	
SDVO_CTRL_CLK	H35	SDVO_CTRLCLK	BI 22
SDVO_CTRL_DATA	K36	SDVO_CTRLDATA	BI 22
CLKREQ*	G39	NB_CLKREQ_L	OUT 7 29
ICH_SYNC*	G40	NB_SB_SYNC_L	OUT 7 25
TEST1	A37	NB_TEST1	
TEST2	R32	NB_TEST2	

Clk used for PEG and DMI

21 18 8 =PP1V8_S3M_MEM_NB
R1610 20 1% 1/10W MF-LF 402
R1620 1K 1% 1/16W MF-LF 402
C1623 0.01UF 10% 16V CERM 402
C1622 2.2UF 20% 6.3V CERM1 603
R1622 3.01K 1% 1/16W MF-LF 402
R1611 20 1% 1/10W MF-LF 402
C1625 0.01UF 10% 16V CERM 402
C1624 2.2UF 20% 6.3V CERM1 603
R1624 1K 1% 1/10W MF-LF 402
C1615 0.1UF 20% 10V CERM 402
C1616 0.1UF 20% 10V CERM 402

PP1V25_S0M_NB_VCCAXD 19 21
R1640 1K 1% 1/16W MF-LF 402
C1640 0.1uF 20% 10V CERM 402
R1641 392 1% 1/16W MF-LF 402

R1691 20K 5% 1/16W MF-LF 402
R1690 0 5% 1/16W MF-LF 402

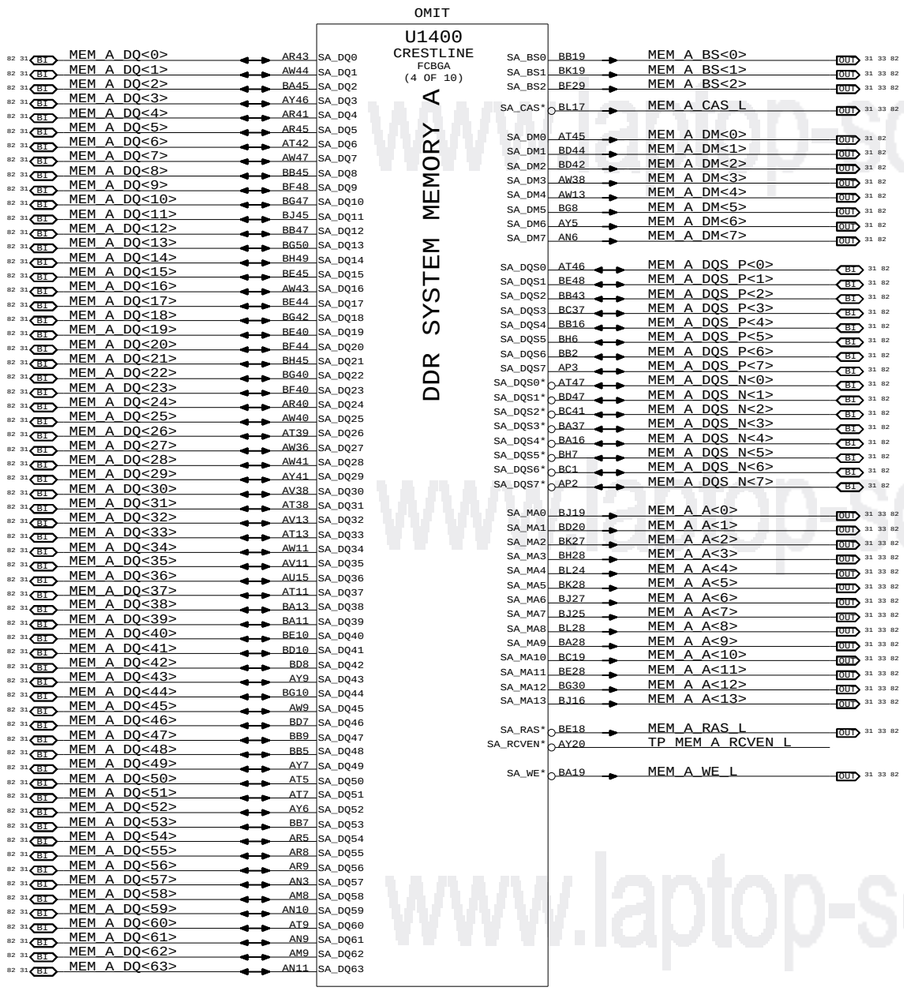
NOTE: GMCH CL_PWROK input must be PWRGD signal for PP3V3_S0M, PP3V3_S0MWOL, PP1V8_S3M, PP1V25_S0M, PP1V05_S0M, PP0V9_S3M and PP0V9_S0M.
If ME/AMT is not used, short CL_PWROK to PWROK.

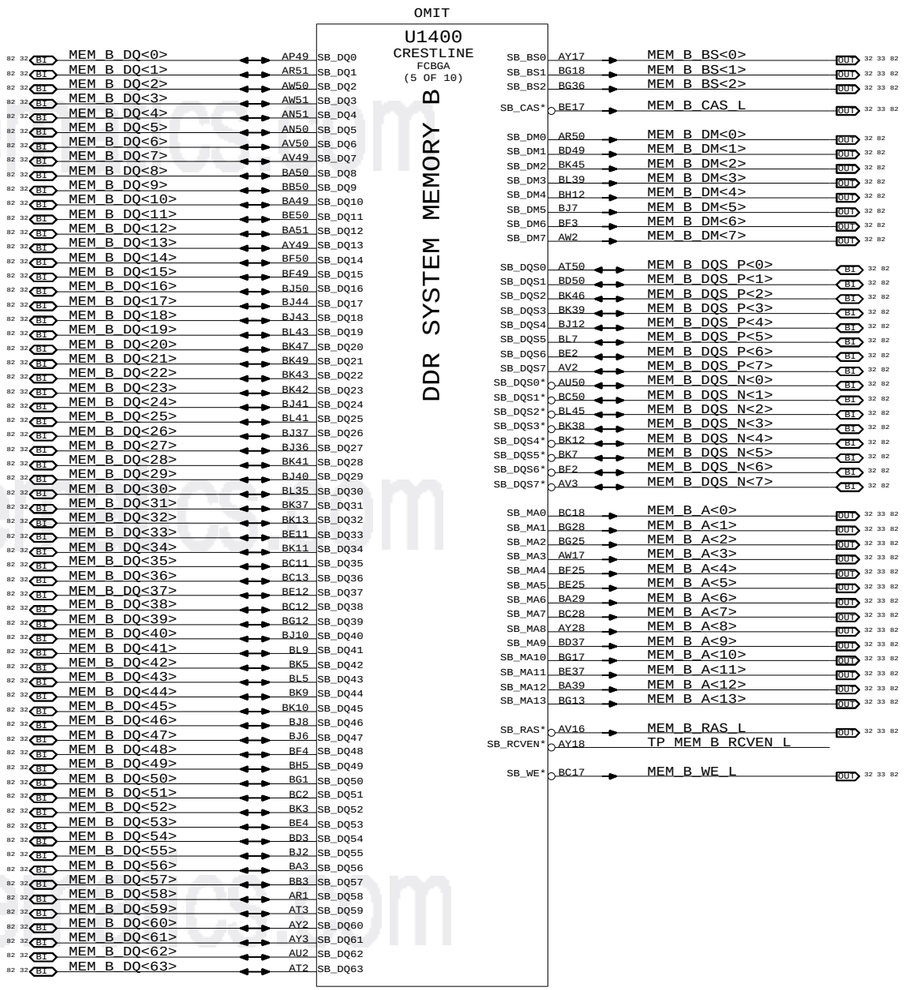
NB Misc Interfaces

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 16 OF 89	





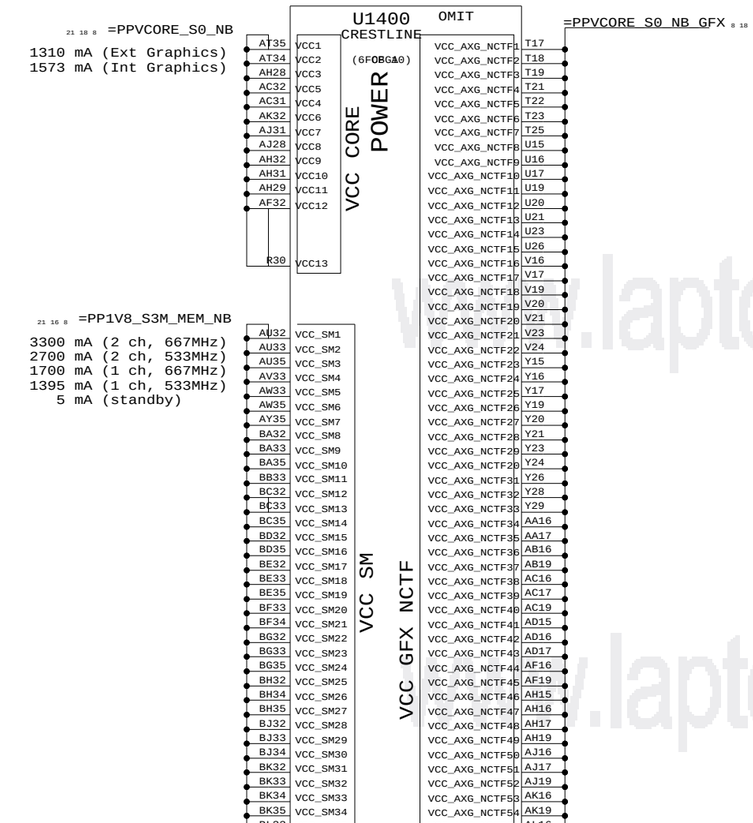
NB DDR2 Interfaces

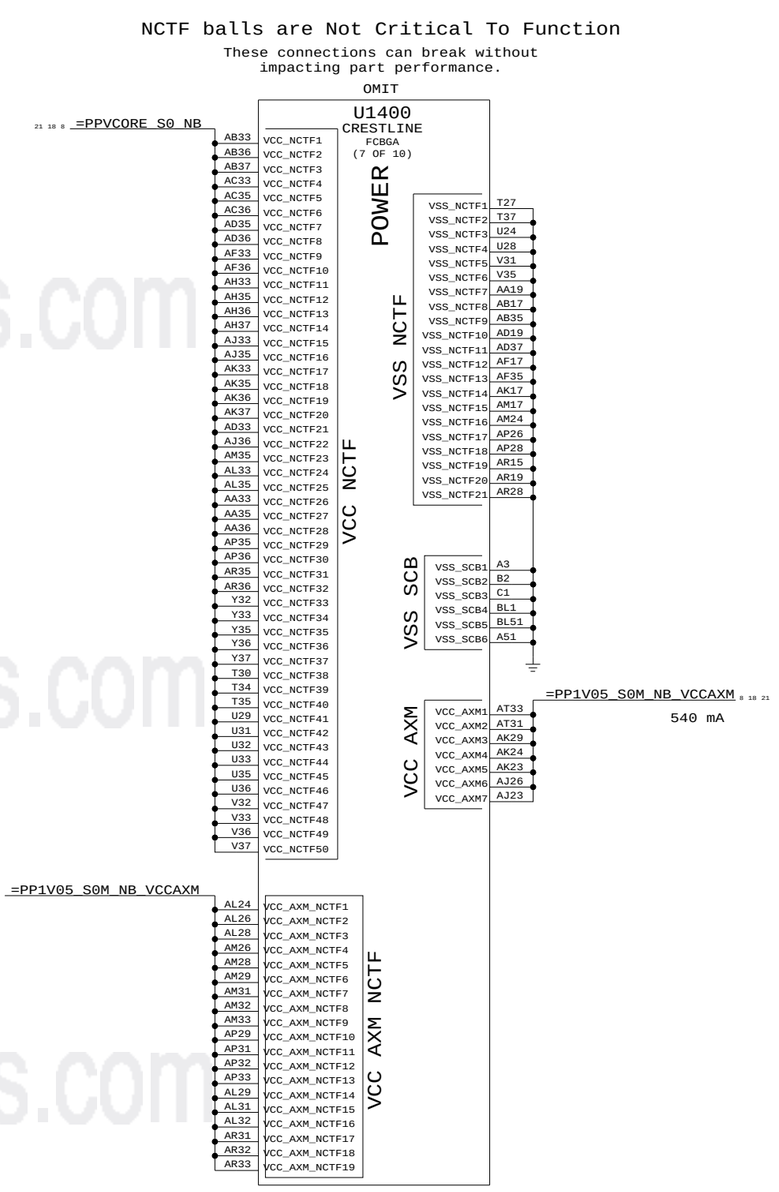
SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0

SCALE	SHT	OF
NONE	17	89





Current numbers from Crestline EDS, doc #21749.

NB Power 1

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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APPLE INC.

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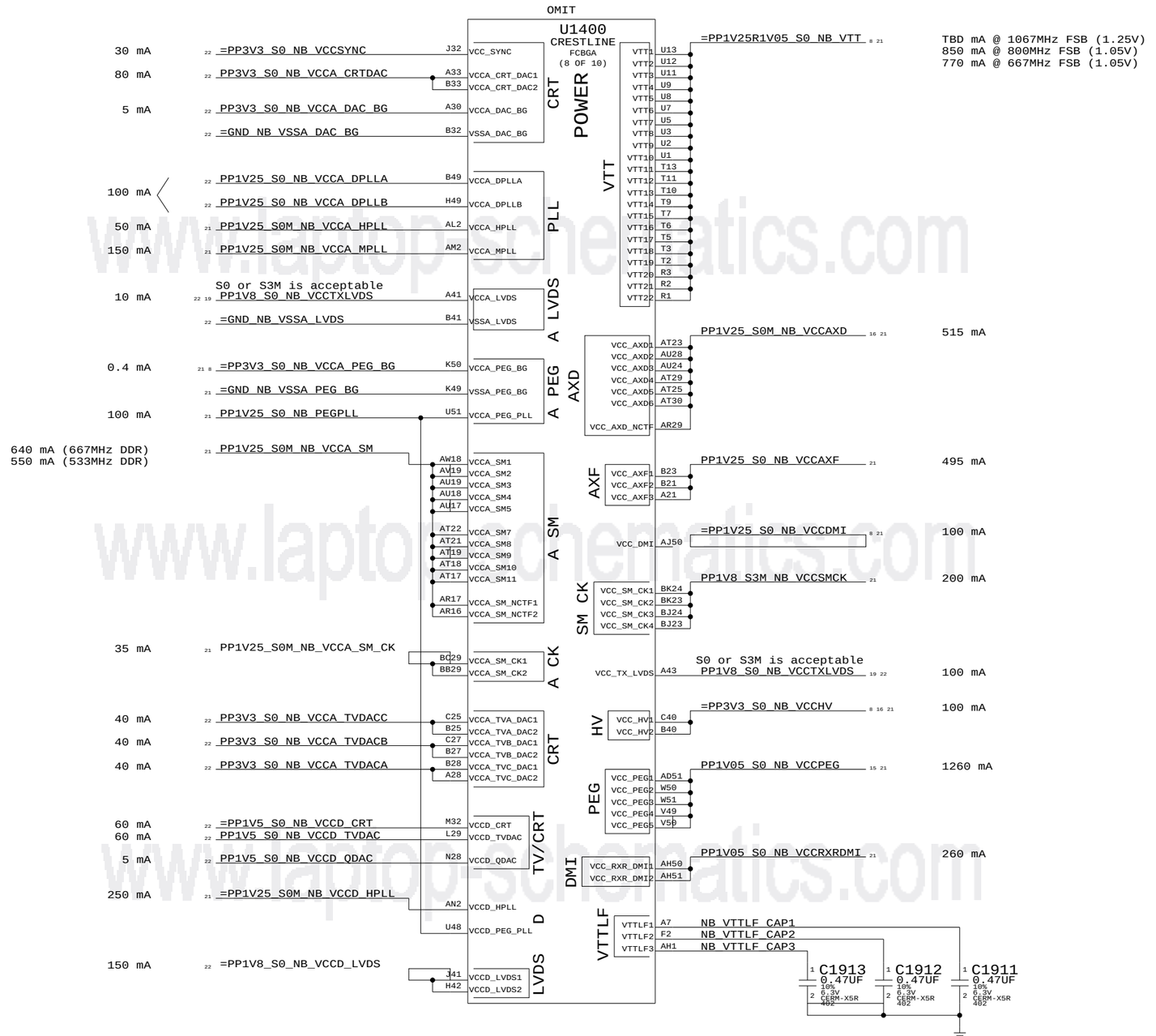
D	051-7413	11.0.0
SCALE: NONE	SHT 18 OF 89	



Current numbers from Crestline EDS, doc #21749.

NB Power 2

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0

SCALE: NONE SHT 19 OF 89

OMIT

U1400
CRESTLINE
FCBGA
(9 OF 10)
VSS

A13	VSS1	VSS100	AW24
A15	VSS2	VSS101	AW29
A17	VSS3	VSS102	AW32
A24	VSS4	VSS103	AW5
AA21	VSS5	VSS104	AW7
AA24	VSS6	VSS105	AY10
AA29	VSS7	VSS106	AY24
AB20	VSS8	VSS107	AY37
AB23	VSS9	VSS108	AY42
AB26	VSS10	VSS109	AY43
AB28	VSS11	VSS110	AY45
AB31	VSS12	VSS111	AY47
AC10	VSS13	VSS112	AY50
AC13	VSS14	VSS113	B10
AC3	VSS15	VSS114	B20
AC39	VSS16	VSS115	B24
AC43	VSS17	VSS116	B29
AC47	VSS18	VSS117	B30
AD1	VSS19	VSS118	B35
AD21	VSS20	VSS119	B38
AD26	VSS21	VSS120	B43
AD29	VSS22	VSS121	B46
AD3	VSS23	VSS122	B5
AD41	VSS24	VSS123	B8
AD45	VSS25	VSS124	BA1
AD49	VSS26	VSS125	BA17
AD5	VSS27	VSS126	BA18
AD50	VSS28	VSS127	BA2
AD8	VSS29	VSS128	BA24
AE10	VSS30	VSS129	BB12
AE14	VSS31	VSS130	BB25
AE6	VSS32	VSS131	BB40
AF20	VSS33	VSS132	BB44
AF23	VSS34	VSS133	BB49
AF24	VSS35	VSS134	BB8
AF31	VSS36	VSS135	BC16
AG2	VSS37	VSS136	BC24
AG38	VSS38	VSS137	BC25
AG43	VSS39	VSS138	BC36
AG47	VSS40	VSS139	BC40
AG50	VSS41	VSS140	BC51
AH3	VSS42	VSS141	BD13
AH40	VSS43	VSS142	BD2
AH41	VSS44	VSS143	BD28
AH7	VSS45	VSS144	BD45
AH9	VSS46	VSS145	BD48
AJ11	VSS47	VSS146	BD5
AJ13	VSS48	VSS147	BE1
AJ21	VSS49	VSS148	BE19
AJ24	VSS50	VSS149	BE23
AJ29	VSS51	VSS150	BE30
AJ32	VSS52	VSS151	BE42
AJ43	VSS53	VSS152	BE51
AJ45	VSS54	VSS153	BE8
AJ49	VSS55	VSS154	BF12
AK20	VSS56	VSS155	BF16
AK21	VSS57	VSS156	BF36
AK26	VSS58	VSS157	BG19
AK28	VSS59	VSS158	BG2
AK31	VSS60	VSS159	BG24
AK51	VSS61	VSS160	BG29
AL1	VSS62	VSS161	BG39
AM11	VSS63	VSS162	BG48
AM13	VSS64	VSS163	BG5
AM3	VSS65	VSS164	BG51
AM4	VSS66	VSS165	BH17
AM41	VSS67	VSS166	BH30
AM45	VSS68	VSS167	BH44
AN1	VSS69	VSS168	BH46
AN38	VSS70	VSS169	BH8
AN39	VSS71	VSS170	BJ11
AN43	VSS72	VSS171	BJ13
AN5	VSS73	VSS172	BJ38
AN7	VSS74	VSS173	BJ4
AP4	VSS75	VSS174	BJ42
AP48	VSS76	VSS175	BJ46
AP50	VSS77	VSS176	BK15
AR11	VSS78	VSS177	BK17
AR2	VSS79	VSS178	BK25
AR39	VSS80	VSS179	BK29
AR44	VSS81	VSS180	BK36
AR47	VSS82	VSS181	BK40
AR7	VSS83	VSS182	BK44
AT10	VSS84	VSS183	BK6
AT14	VSS85	VSS184	BK8
AT41	VSS86	VSS185	BL11
AT49	VSS87	VSS186	BL13
AU1	VSS88	VSS187	BL19
AU23	VSS89	VSS188	BL22
AU29	VSS90	VSS189	BL37
AU3	VSS91	VSS190	BL47
AU36	VSS92	VSS191	C12
AU49	VSS93	VSS192	C16
AU51	VSS94	VSS193	C19
AV39	VSS95	VSS194	C28
AV48	VSS96	VSS195	C29
AW1	VSS97	VSS196	C33
AW12	VSS98	VSS197	C36
AW16	VSS99	VSS198	C41

OMIT

U1400
CRESTLINE
FCBGA
(10 OF 10)
VSS

C46	VSS199	VSS287	W11
C50	VSS200	VSS288	W39
C7	VSS201	VSS289	W43
D13	VSS202	VSS290	W47
D24	VSS203	VSS291	W5
D3	VSS204	VSS292	W7
D32	VSS205	VSS293	Y13
D39	VSS206	VSS294	Y2
D45	VSS207	VSS295	Y41
D49	VSS208	VSS296	Y45
E10	VSS209	VSS297	Y49
E16	VSS210	VSS298	Y5
E24	VSS211	VSS299	Y50
E28	VSS212	VSS300	Y11
E32	VSS213	VSS301	P29
E47	VSS214		
F19	VSS215		
F36	VSS216	TDE_SENSE VSS302	T29
F4	VSS217		
F40	VSS218	TDE_FORCE VSS303	T31
F50	VSS219		
G1	VSS220		
G13	VSS221		
G16	VSS222	TDB_FORCE VSS304	T33
G19	VSS223		
G24	VSS224		
G28	VSS225	TDB_SENSE VSS305	R28
G29	VSS226		
G33	VSS227		
G42	VSS228		
G45	VSS229	VSS306	AA32
G48	VSS230	VSS307	AB32
G8	VSS231	VSS308	AD32
H24	VSS232	VSS309	AF28
H28	VSS233	VSS310	AF29
H4	VSS234	VSS311	AT27
H45	VSS235	VSS312	AV25
J11	VSS236	VSS313	H50
J16	VSS237		
J2	VSS238		
J24	VSS239		
J28	VSS240		
J33	VSS241		
J35	VSS242		
J39	VSS243		
K12	VSS245		
K47	VSS246		
K8	VSS247		
L1	VSS248		
L17	VSS249		
L20	VSS250		
L24	VSS251		
L28	VSS252		
L3	VSS253		
L33	VSS254		
L49	VSS255		
M28	VSS256		
M42	VSS257		
M46	VSS258		
M49	VSS259		
M5	VSS260		
M50	VSS261		
M9	VSS262		
N11	VSS263		
N14	VSS264		
N17	VSS265		
N29	VSS266		
N32	VSS267		
N36	VSS268		
N39	VSS269		
N44	VSS270		
N49	VSS271		
N7	VSS272		
P19	VSS273		
P2	VSS274		
P23	VSS275		
P3	VSS276		
P50	VSS277		
R49	VSS278		
T39	VSS279		
T43	VSS280		
T47	VSS281		
U41	VSS282		
U45	VSS283		
U50	VSS284		
V2	VSS285		
V3	VSS286		

Crestline Thermal Diode Pins

Mainly for investigation. If not used, alias these nets directly to GND.

TDE_SENSE T29 =NB_TDE_SENSE 51

NOTE: TDE = _P

TDE_FORCE T31 =NB_TDE_FORCE 51

TDB_FORCE T33 =NB_TDB_FORCE 51

NOTE: TDB = _N

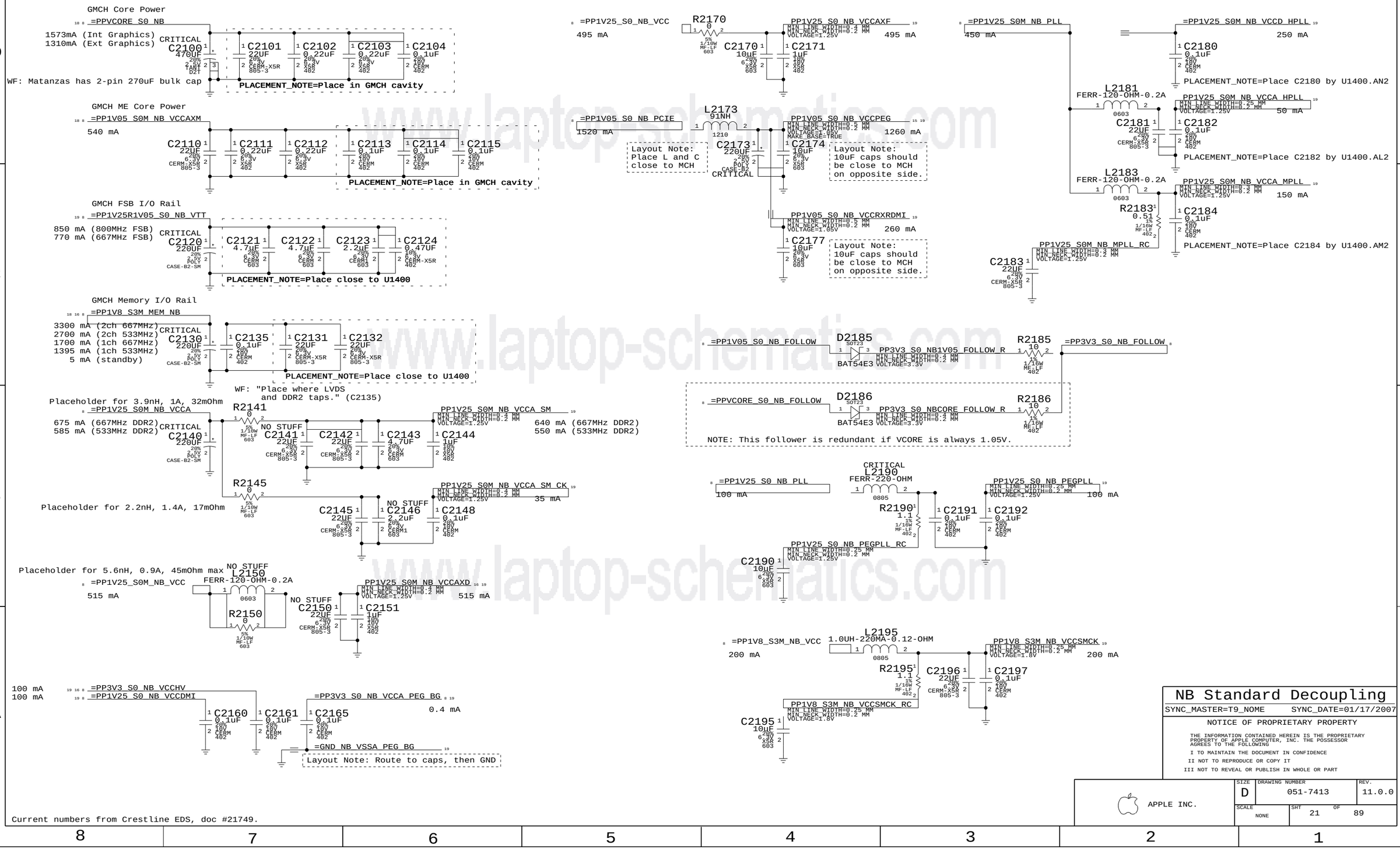
TDB_SENSE R28 =NB_TDB_SENSE 51

NB Grounds

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

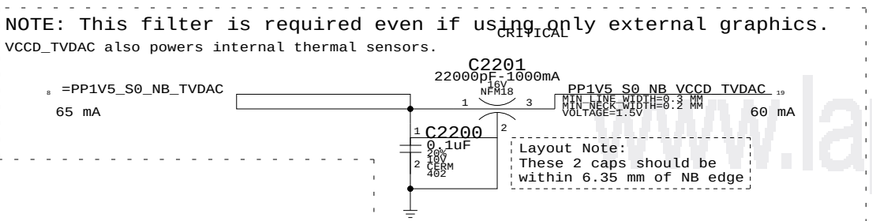
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 20 OF 89	



Crestline LVDS Strapping

NOTE: This filter is required even if using only external graphics.
VCCD_TVDAC also powers internal thermal sensors.



15	LVDS_DDC_CLK	
15	LVDS_DDC_DATA	
15 13	LVDS_CTRL_CLK	
15 13	LVDS_CTRL_DATA	
15	=CRT_RED	
15	=CRT_RED_L	
15	=CRT_GREEN	
15	=CRT_GREEN_L	
15	=CRT_BLUE	
15	=CRT_BLUE_L	
15	=CRT_HSYNC_R	
15	=CRT_VSYNC_R	
15	=CRT_TVO_IREF	
15	=TV_A_DAC	
15	=TV_A_RTN	
15	=TV_B_DAC	
15	=TV_B_RTN	
15	=TV_C_DAC	
15	=TV_C_RTN	
15	CRT_DDC_CLK	
15	CRT_DDC_DATA	
16	SDVO_CTRLCLK	
16	SDVO_CTRLDATA	
15	TV_DCONSEL<0>	
15	TV_DCONSEL<1>	
16	=NB_CLK96M_DOT_N	
16	=NB_CLK96M_DOT_P	
16	=NB_CLK100M_DPLLSS_P	
16	=NB_CLK100M_DPLLSS_N	

	=GND_NB_VSSA_LVDS	19
	PP1V8_S0_NB_VCCTXLVDS	19
	PP1V25_S0_NB_VCCA_DPLLB	19
	PP1V25_S0_NB_VCCA_DPLLA	19
	=PP1V8_S0_NB_VCCD_LVDS	19
	=PP1V5_S0_NB_VCCD_CRT	19
	PP3V3_S0_NB_VCCA_CRTDAC	19
	=PP3V3_S0_NB_VCCSYNC	19
	PP1V5_S0_NB_VCCD_QDAC	19
	PP3V3_S0_NB_VCCA_DAC_BG	19
	=GND_NB_VSSA_DAC_BG	19
	PP3V3_S0_NB_VCCA_TVDACA	19
	PP3V3_S0_NB_VCCA_TVDACB	19
	PP3V3_S0_NB_VCCA_TVDACC	19

15	LVDS_BKLT_CTL	NC_LVDS_BKLT_CTL
15	LVDS_BKLT_EN	NC_LVDS_BKLT_EN
15	LVDS_VDD_EN	NC_LVDS_VDD_EN
81 15	LVDS_IBG	NC_LVDS_IBG
15	TP_LVDS_VBG	NC_LVDS_VBG
81 15	LVDS_A_CLK_N	NC_LVDS_A_CLKN
81 15	LVDS_A_CLK_P	NC_LVDS_A_CLKP
81 15	LVDS_B_CLK_N	NC_LVDS_B_CLKN
81 15	LVDS_B_CLK_P	NC_LVDS_B_CLKP
81 15	LVDS_A_DATA_N<0>	NC_LVDS_A_DATAN<0>
81 15	LVDS_A_DATA_N<1>	NC_LVDS_A_DATAN<1>
81 15	LVDS_A_DATA_N<2>	NC_LVDS_A_DATAN<2>
81 15	LVDS_A_DATA_P<0>	NC_LVDS_A_DATAP<0>
81 15	LVDS_A_DATA_P<1>	NC_LVDS_A_DATAP<1>
81 15	LVDS_A_DATA_P<2>	NC_LVDS_A_DATAP<2>
81 15	LVDS_B_DATA_N<0>	NC_LVDS_B_DATAN<0>
81 15	LVDS_B_DATA_N<1>	NC_LVDS_B_DATAN<1>
81 15	LVDS_B_DATA_N<2>	NC_LVDS_B_DATAN<2>
81 15	LVDS_B_DATA_P<0>	NC_LVDS_B_DATAP<0>
81 15	LVDS_B_DATA_P<1>	NC_LVDS_B_DATAP<1>
81 15	LVDS_B_DATA_P<2>	NC_LVDS_B_DATAP<2>
15	TP_LVDS_VREFH	NC_LVDS_VREFH
15	TP_LVDS_VREFL	NC_LVDS_VREFL
16	GFX_VID<1>	TP_GFX_VID<1>
16	GFX_VID<2>	TP_GFX_VID<2>
16	GFX_VID<3>	TP_GFX_VID<3>
16	GFX_VID<4>	TP_GFX_VID<4>
16	=GFX_VR_EN	TP_GFX_VR_EN

MAKE_BASE=TRUE NO_TEST=TRUE

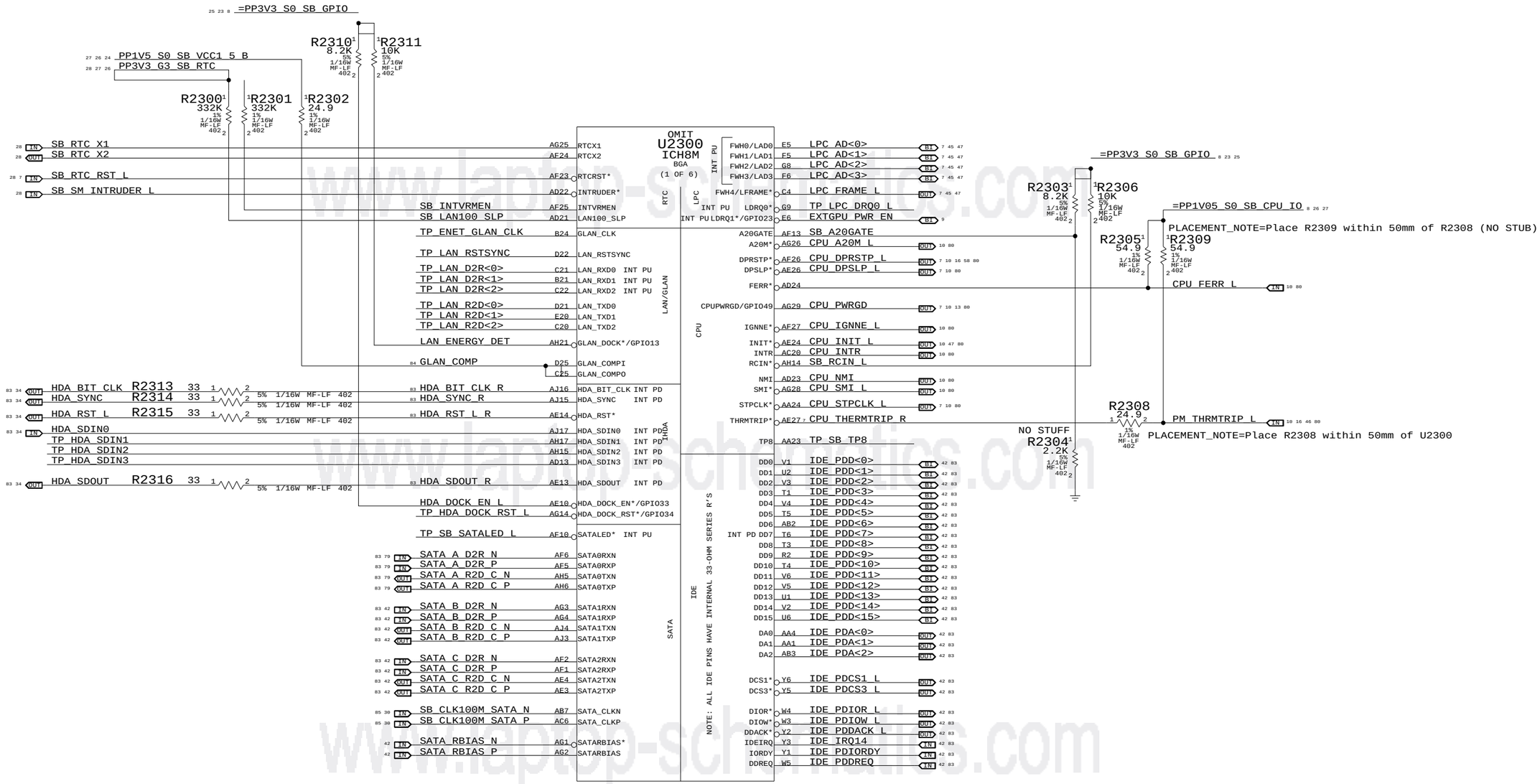
Current numbers from Crestline EDS Addendum, doc #20127.

NB Graphics Decoupling

SYNC_MASTER=M76_MLB SYNC_DATE=03/12/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 22 OF 89	



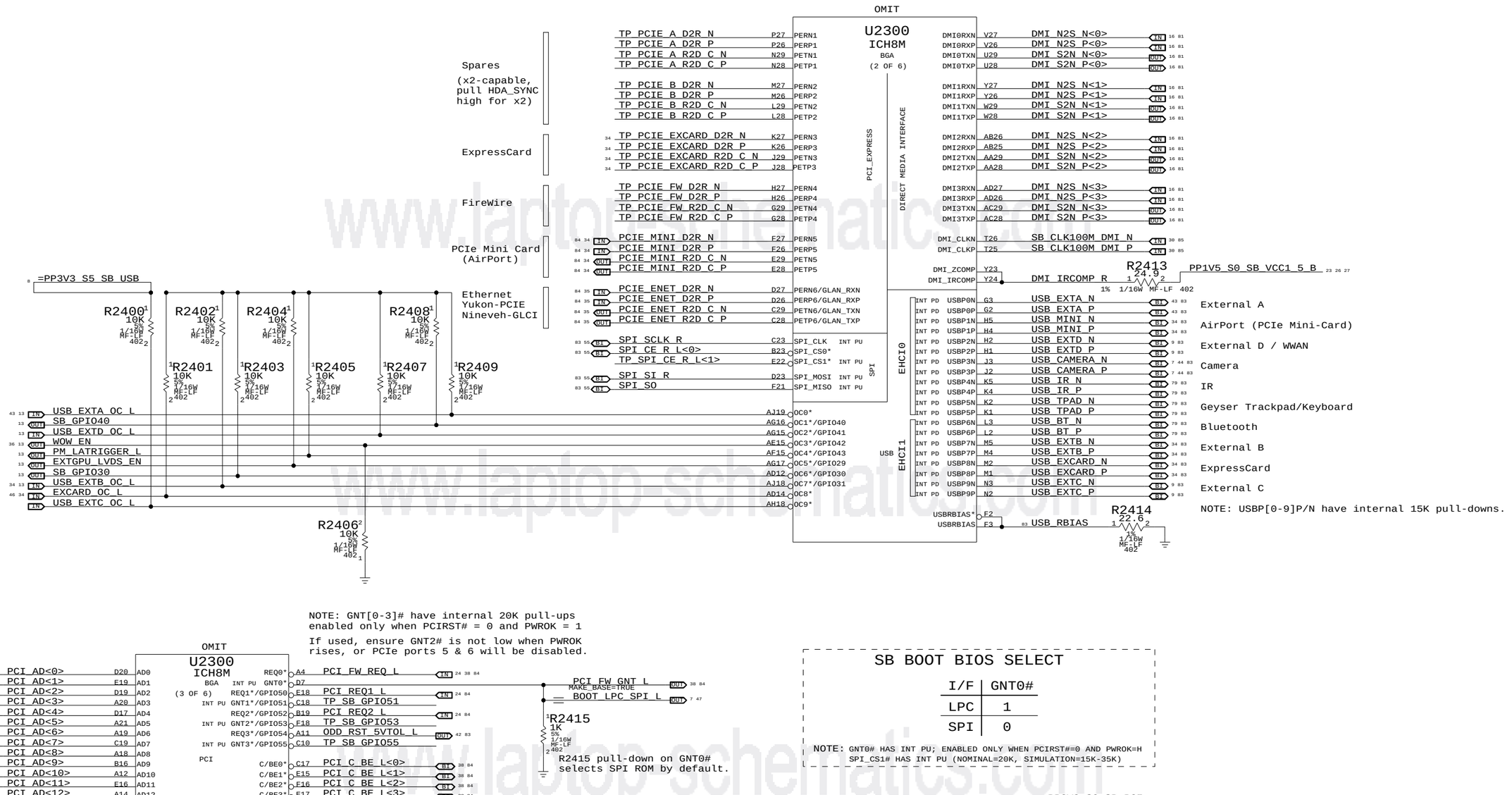
	HDA
HDA_BIT_CLK	24.000MHZ CLOCK W/INTERNAL WEAK PD
HDA_RST#	
HDA_SDIN[0-2]	INTEGRATED PDs
HDA_SDOUT	INTEGRATED PD
ACZ_SYNC	INTEGRATED PD

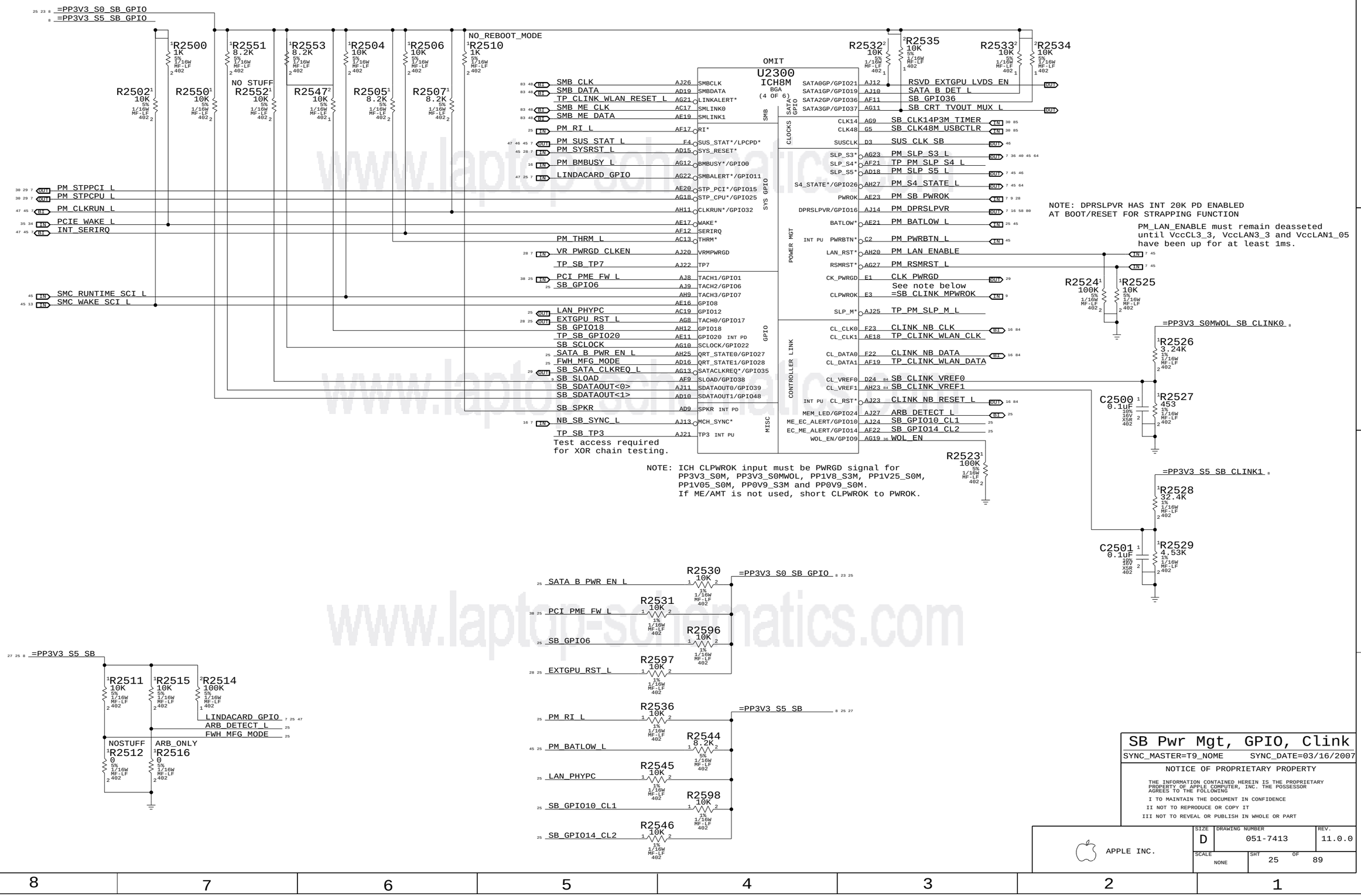
SB Enet, Disk, FSB, LPC

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 23 OF 89	



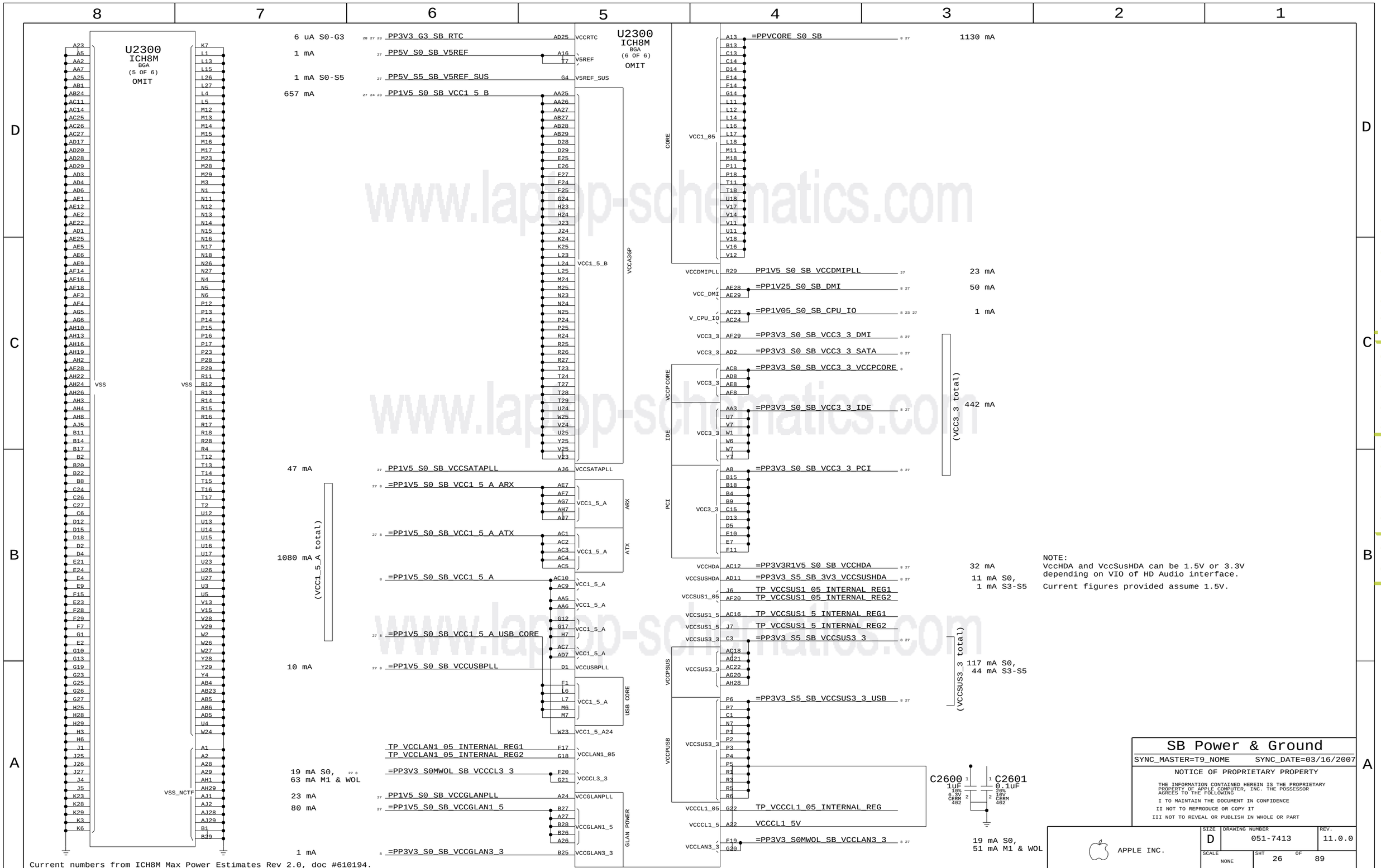


SB Pwr Mgt, GPIO, Clink

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 25 OF 89	



=PP3V3_S5_SB
=PP5V_S5_SB
1 mA S0-S5
ICH V5REF_SUS Filter & Follower
(ICH Reference for 5V Tolerance on Resume Well Inputs)
R2701 10 5% 1/10W MF-LF 402
D2702 BAT54DW SOT-363
PP5V_S5_SB_V5REF_SUS
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=5V
C2704 0.1UF 10% 16V X5R 402
1 mA S0-S5
PLACEMENT NOTE:
PLACE C2704 < 2.54MM OF PIN G4 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY

=PP3V3_S0_SB
=PP5V_S0_SB
1 mA
ICH V5REF Filter & Follower
(ICH Reference for 5V Tolerance on Core Well Inputs)
R2702 100 5% 1/10W MF-LF 402
D2702 BAT54DW SOT-363
PP5V_S0_SB_V5REF
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=5V
C2703 1UF 10% 16V X5R 402
1 mA
PLACEMENT NOTE:
PLACE C2703 < 2.54MM OF PIN A16..T7 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY

PLACEMENT NOTE:
PLACE C2700 & C2705-07 < 2.54MM OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
DISTRIBUTED BETWEEN AA25..V23

ICH VCC1_5_B BYPASS
(ICH IO,LOGIC 1.5V PWR)
=PP1V5_S0_SB
837 mA
L2700 FERR-330-OHM-1.5A 0805-1
C2700 220UF 20% 6.3V CASE-D2 CRITICAL
C2705 22UF 20% 6.3V CERM-X5R 805-3
C2706 22UF 20% 6.3V CERM-X5R 805-3
C2707 2.2UF 20% 6.3V CERM1 603
PP1V5_S0_SB_VCC1_5_B
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
657 mA
=PP1V5_S0_SB_VCCGLAN1_5
80 mA
C2736 4.7UF 20% 6.3V CERM 603
PLACEMENT NOTE:
PLACE C2736 NEAR PIN B27..A26

ICH VCCGLANPLL Filter
(ICH GLAN PLL PWR)
PP1V5_S0_SB_VCCGLANPLL
33 mA
C2732 2.2uF 20% 6.3V CERM1 603
33 mA
PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN A24

ICH VCCSATAPLL Filter
(ICH SATA PLL PWR)
R2735 0 5% 1/10W MF-LF 402
PP1V5_S0_SB_VCCSATAPLL_F
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.5V
47 mA
L2702 10UH-100MA 0805
C2735 10UF 20% 6.3V X6S 603
PP1V5_S0_SB_VCCSATAPLL
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.5V
47 mA
C2717 1UF 10% 6.3V CERM 402
PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AJ6

ICH VCCDMIPLL Filter
(ICH DMI PLL PWR)
R2700 1 5% 1/10W MF-LF 603
PP1V5_S0_SB_VCCDMIPLL_F
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.5V
23 mA
L2703 1.0UH-0.5A 1210
C2708 10UF 20% 6.3V X6S 603
PP1V5_S0_SB_VCCDMIPLL
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.5V
23 mA
C2701 0.01UF 10% 16V CERM 402
PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON
SECONDARY SIDE OR 3.56MM ON PRIMARY

Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.

ICH VCCRTC BYPASS
(ICH RTC 3.3V PWR)
0.6 uA G3
PP3V3_G3_SB_RTC
C2729 0.1UF 10% 16V X5R 402
C2730 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE CAPS NEAR PIN AD25 OF SB

ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
=PP3V3_S5_SB_VCCSUS3_3
(VCCSUS3_3 Total)
117 mA S0 /
44 mA S3-S5
C2731 0.1UF 10% 16V X5R 402
C2734 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE CAPS NEAR PINS AC18..AH28

ICH USB/VCCSUS3_3 BYPASS
(ICH SUSPEND USB 3.3V PWR)
=PP3V3_S5_SB_VCCSUS3_3_USB
C2733 4.7uF 20% 6.3V CERM 603
PLACEMENT NOTE:
PLACE CAP NEAR PINS
P6..R6

ICH VCC_PAUX/VCCLAN3_3 BYPASS
(ICH LAN I/F BUFFER 3.3V PWR)
38 mA S0 /
114 mA M1 & WOL
=PP3V3_S0MWOL_SB_VCCLAN3_3
=PP3V3_S0MWOL_SB_VCCCL3_3
C2719 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE CAP UNDER SB NEAR PINS
F19 AND G20

ICH IDE/VCC3_3 BYPASS
(ICH IDE I/O 3.3V PWR)
=PP3V3_S0_SB_VCC3_3_IDE
C2725 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AA3...Y7

=PP3V3_S0_SB_VCC3_3_SATA
C2738 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AD2

(VCC3_3 Total)
442 mA
=PP3V3_S0_SB_VCC3_3_DMI
C2737 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE CAP < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AF29

ICH PCI/VCC3_3 BYPASS
(ICH PCI I/O 3.3V PWR)
=PP3V3_S0_SB_VCC3_3_PCI
C2726 0.1UF 10% 16V X5R 402
C2727 0.1UF 10% 16V X5R 402
C2728 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
DISTRIBUTE IN PCI SECTION OF SB
NEAR PINS A8 ... F11

ICH VCCHDA BYPASS
(ICH INTEL HDA CORE 3.3V/1.5V PWR)
32 mA
(@ 1.5V)
=PP3V3R1V5_S0_SB_VCCHDA
C2721 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AC12

ICH VCCSUSHDA BYPASS
(ICH INTEL HDA SUSPEND 3.3V/1.5V PWR)
11 mA S0 /
1 mA S3-S5
(@ 1.5V)
=PP3V3_S5_SB_3V3_VCCSUSHDA
C2741 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AD11

ICH VCC1_5_A/ARX BYPASS
(ICH LOGIC&IO[ARX] 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_ARX
C2711 1UF 10% 6.3V CERM 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AE7..AJ7

ICH VCC1_5_A/ATX BYPASS
(ICH LOGIC&IO[ATX] 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_ATX
1080 mA
(VCC1_5_A Total)
C2714 1UF 10% 6.3V CERM 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AC1..AC5

ICH USB CORE/VCC1_5_A BYPASS
(ICH USB CORE 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_USB_CORE
C2712 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS F1..M7

ICH VCCUSBPLL BYPASS
(ICH USB PLL 1.5V PWR)
10 mA
=PP1V5_S0_SB_VCCUSBPLL
C2715 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE C2715 NEAR PIN D1 OF SB

50 mA
=PP1V25_S0_SB_DMI
C2739 22UF 20% 6.3V CERM-X5R 805-3
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AE29

ICH CORE/VCC1_05 BYPASS
(ICH CORE 1.05V PWR)
1130 mA
=PPVCORE_S0_SB
C2718 0.1UF 10% 16V X5R 402
C2702 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE CAPS AT EDGE OF SB

ICH V_CPU_IO BYPASS
(ICH CPU I/O 1.05V PWR)
1 mA
=PP1V05_S0_SB_CPU_IO
C2724 4.7UF 20% 6.3V CERM 603
C2723 0.1UF 10% 16V X5R 402
C2722 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE NEAR PINS AC23,AC24 OF SB

SB Decoupling

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

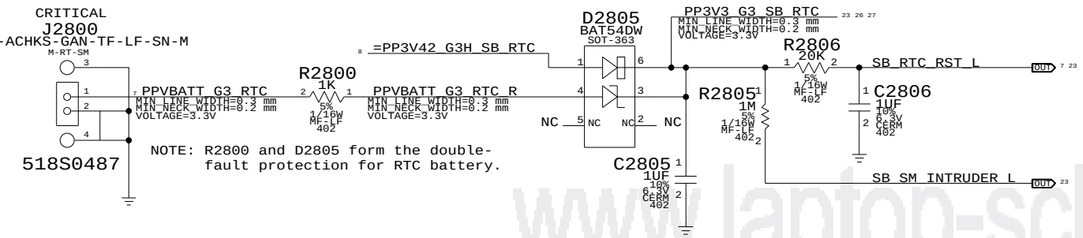
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 27 OF 89	

RTC Power Sources

Coin-Cell Connector

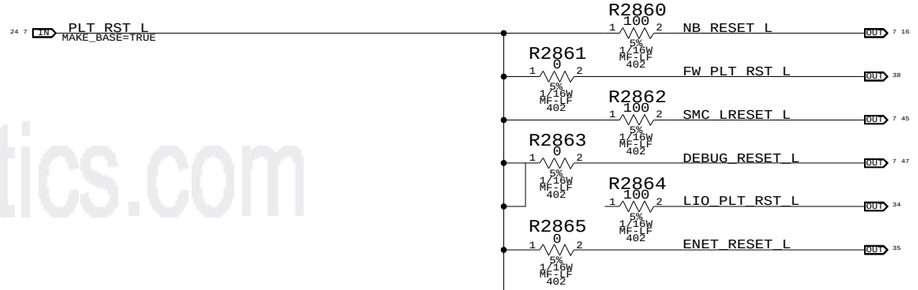
CRITICAL
J2800
BM02B-ACHKS-GAN-TF-LF-SN-M
M-RT-SM
518S0487



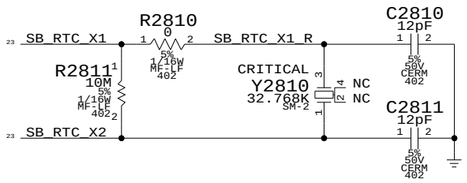
NOTE: R2800 and D2805 form the double-fault protection for RTC battery.

Platform Reset Connections

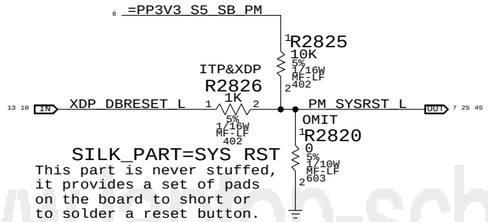
Unbuffered



SB RTC Crystal

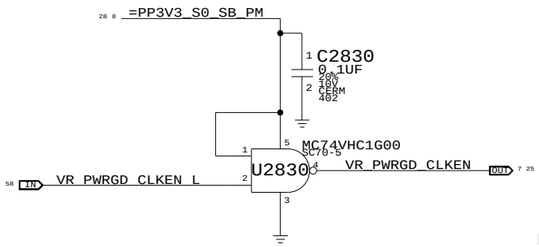


System Reset "Button"

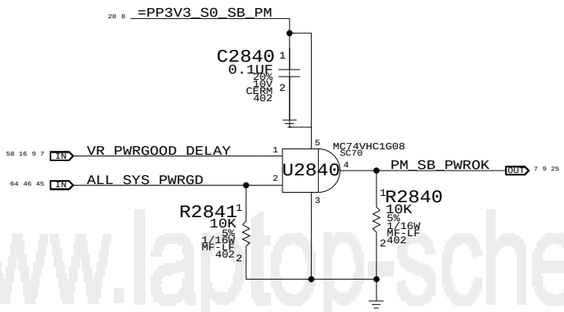


SILK_PART=SYS_RST
This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

VRMPWRGD Inverter

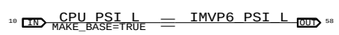


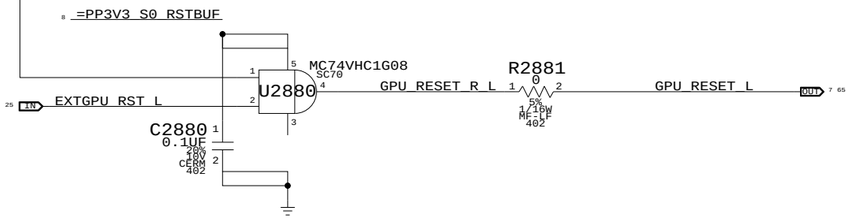
PWROK Circuit



PCI Reset Connections

CPU VCore ForcePSI



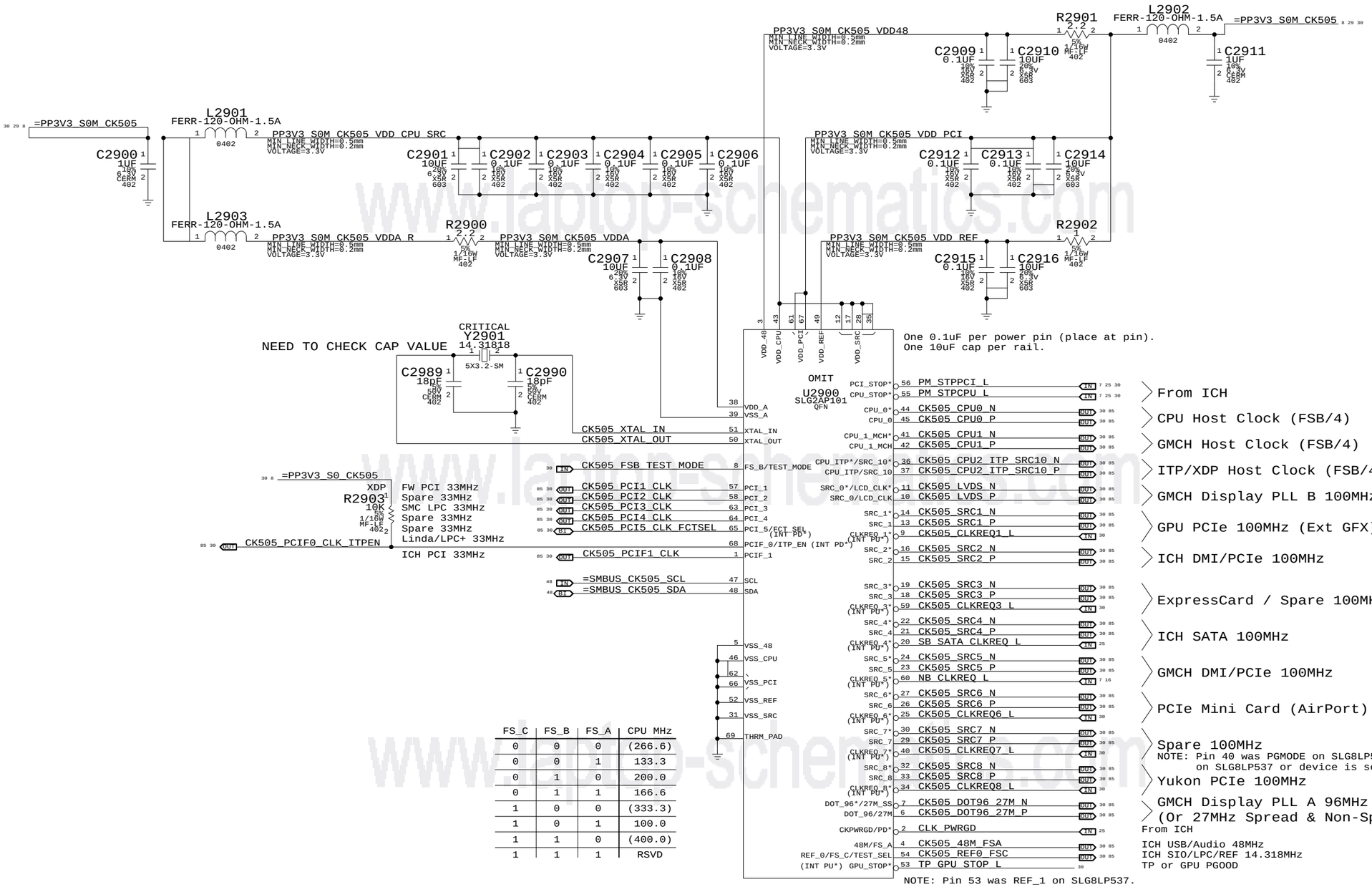


SB Misc

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/24/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 28 OF 89	



FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

FCT_SEL	PIN 6	PIN 7	PIN 10	PIN 11	
0	DOT_96+	DOT_96-	LCD_CLK+	LCD_CLK-	(For Internal Graphics)
1	27M	27M w/SS	SRC_0+	SRC_0-	(For External Graphics)

Clock (CK505)

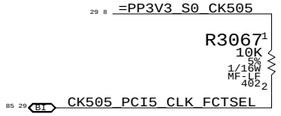
SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

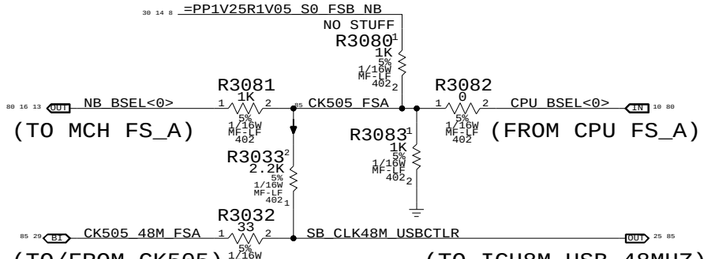
SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE	SHT	OF
NONE	29	89

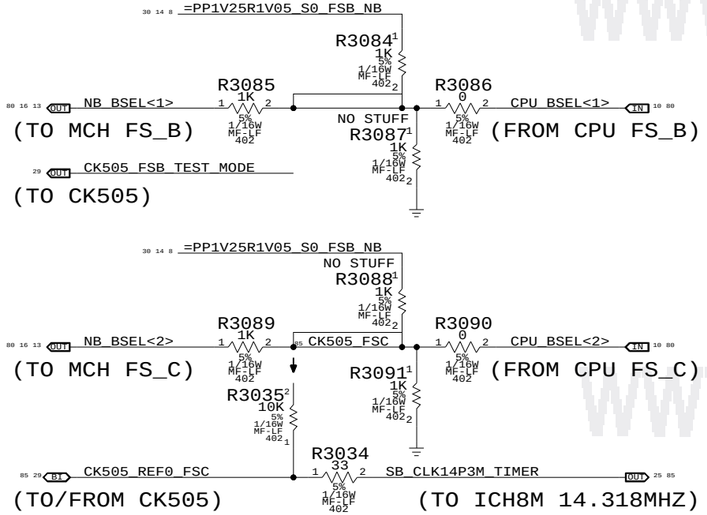
CK505 Configuration Straps

FCT_SEL (GFX clock select)



FS_A, FS_B, FS_C (Host clock freq select)





FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

NO STUFF R3082, R3086 & R3090 for manual CPU clk frequency.

(Only 100-200MHz supported by SLG8LP536 and CY28545-5)

CLK Termination

(Note: HOST/SRC/GFX clock termination removed. Silego SL8GLP536 or equiv. support only)

85 29 IN CK505_CPU0_P = FSB_CLK_CPU_P OUT 10 85 (MAKE_BASE=TRUE)
85 29 IN CK505_CPU0_N = FSB_CLK_CPU_N OUT 10 85 (MAKE_BASE=TRUE)
(CPU HOST 167/200MHZ)

85 29 IN CK505_CPU1_P = FSB_CLK_NB_P OUT 7 14 85 (MAKE_BASE=TRUE)
85 29 IN CK505_CPU1_N = FSB_CLK_NB_N OUT 7 14 85 (MAKE_BASE=TRUE)
(GMCH HOST 167/200MHZ)

85 29 IN CK505_CPU2_ITP_SRC10_P = XDP_CLK_P OUT 13 80 85 (MAKE_BASE=TRUE)
85 29 IN CK505_CPU2_ITP_SRC10_N = XDP_CLK_N OUT 13 80 85 (MAKE_BASE=TRUE)
(ITP HOST 167/200MHZ)

85 29 IN CK505_LVDS_P = TP_NB_CLK100M_DPLLSS_P (MAKE_BASE=TRUE)
85 29 IN CK505_LVDS_N = TP_NB_CLK100M_DPLLSS_N (MAKE_BASE=TRUE)
(Int Gfx LVDS 100MHz)

85 29 IN CK505_SRC1_P = PEG_CLK100M_GPU_P OUT 9 65 (MAKE_BASE=TRUE)
85 29 IN CK505_SRC1_N = PEG_CLK100M_GPU_N OUT 9 65 (MAKE_BASE=TRUE)
(GPU PCIe 100MHz)

85 29 IN CK505_SRC2_P = SB_CLK100M_DMI_P OUT 24 85 (MAKE_BASE=TRUE)
85 29 IN CK505_SRC2_N = SB_CLK100M_DMI_N OUT 24 85 (MAKE_BASE=TRUE)
(ICH8M DMI 100MHZ)

85 29 IN CK505_SRC3_P = PCIE_CLK100M_EXCARD_P OUT 34 85 (MAKE_BASE=TRUE)
85 29 IN CK505_SRC3_N = PCIE_CLK100M_EXCARD_N OUT 34 85 (MAKE_BASE=TRUE)
(ExpressCard 100MHz)

85 29 IN CK505_SRC4_P = SB_CLK100M_SATA_P OUT 23 85 (MAKE_BASE=TRUE)
85 29 IN CK505_SRC4_N = SB_CLK100M_SATA_N OUT 23 85 (MAKE_BASE=TRUE)
(ICH8M SATA 100MHZ)

85 29 IN CK505_SRC5_P = NB_CLK100M_PCIE_P OUT 7 16 85 (MAKE_BASE=TRUE)
85 29 IN CK505_SRC5_N = NB_CLK100M_PCIE_N OUT 7 16 85 (MAKE_BASE=TRUE)
(GMCH PEG/DMI 100MHZ)

85 29 IN CK505_SRC6_P = PCIE_CLK100M_MINI_P OUT 34 85 (MAKE_BASE=TRUE)
85 29 IN CK505_SRC6_N = PCIE_CLK100M_MINI_N OUT 34 85 (MAKE_BASE=TRUE)
(WIRELESS PCIe MINI 100MHZ)

85 29 IN CK505_SRC7_P = TP_PCIE_CLK100M_SRC7P (MAKE_BASE=TRUE)
85 29 IN CK505_SRC7_N = TP_PCIE_CLK100M_SRC7N (MAKE_BASE=TRUE)
(FW 100MHz)

85 29 IN CK505_SRC8_P = PCIE_CLK100M_ENET_P OUT 35 85 (MAKE_BASE=TRUE)
85 29 IN CK505_SRC8_N = PCIE_CLK100M_ENET_N OUT 35 85 (MAKE_BASE=TRUE)
(ENET 100MHZ)

85 29 IN CK505_DOT96_27M_P — CK505_CLK27M (MAKE_BASE=TRUE) — R3024 33 5% 1/16W MF-LF 402 — GPU_CLK27M OUT 71 87
(Ext GFX 27MHz)

85 29 IN CK505_DOT96_27M_N — CK505_CLK27M_SS (MAKE_BASE=TRUE) — R3025 33 5% 1/16W MF-LF 402 — GPU_CLK27M_SS OUT 71 87
(Ext GFX Spread 27MHz)

85 29 IN CK505_PCIF0_CLK_ITPEN — R3026 33 5% 1/16W MF-LF 402 — PCI_CLK33M_LPCPLUS OUT 7 47 85
(LINDA/LPC+ LPC 33MHZ)

85 29 IN CK505_PCIF1_CLK — R3027 33 5% 1/16W MF-LF 402 — PCI_CLK33M_SB OUT 24 85
(ICH8M PCI 33MHZ)

85 29 IN CK505_PCI1_CLK — R3028 33 5% 1/16W MF-LF 402 — PCI_CLK33M_FW OUT 38 85
(FIREWIRE PCI 33MHZ)

85 29 IN CK505_PCI3_CLK — R3030 33 5% 1/16W MF-LF 402 — PCI_CLK33M_SMC OUT 45 85
(SMC PCI 33MHZ)

CLKREQ Controls

29 8 =PP3V3_S0M_CK505
NO STUFF R3046 10K 5% 1/16W MF-LF 402
29 25 7 OUT PM_STPPCI_L
NO STUFF R3047 10K 5% 1/16W MF-LF 402
29 25 7 OUT PM_STPCPU_L

Silego SLG2AP101 has internal pull-ups on all CLKREQ# pins. Support for SL8GLP537 or equiv. only. NB and SATA CLKREQs are not remappable (and thus are not shown here).

34 IN EXCARD_CLKREQ_L (MAKE_BASE=TRUE) = CK505_CLKREQ3_L OUT 29
34 IN MINI_CLKREQ_L (MAKE_BASE=TRUE) = CK505_CLKREQ6_L OUT 29
35 IN =ENET_CLKREQ_L = ENET_CLKREQ_L (MAKE_BASE=TRUE) = CK505_CLKREQ8_L OUT 29
TP_CK505_CLKREQ7_L (MAKE_BASE=TRUE) = CK505_CLKREQ7_L OUT 29
TP_CK505_CLKREQ1_L (MAKE_BASE=TRUE) = CK505_CLKREQ1_L OUT 29

GPU Clock Gating

64 S0PGOOD_PWROK (MAKE_BASE=TRUE) = TP_GPU_STOP_L OUT 29

Unused Clocks

85 29 IN CK505_PCI2_CLK = TP_CK505_PCI2_CLK (MAKE_BASE=TRUE)
(Reserved for TPM PCI 33MHZ)
85 29 IN CK505_PCI4_CLK = TP_CK505_PCI4_CLK (MAKE_BASE=TRUE)
(Spare 33MHZ)

Clock Termination

SYNC_MASTER=(MASTER) SYNC_DATE=08/23/2006

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 30 OF 89	

Page Notes

Power aliases required by this page:
- =PP1V8_S3M_MEM_A
- =PP0V9_S3M_MEM_DIMMVREFA
- =PPSPD_S0M_MEM_A (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

"Factory" (thru-hole) slot

=PP0V9_S3M_MEM_DIMMVREFA

C3101 2.2uF 20% 6.3V CERM 603

C3100 0.1uF 20% 10V CERM 402

=PP1V8_S3M_MEM_A

CRITICAL
J3100
F-RT-TH1
DDR2-SODIMM-DUAL

		VREF	1B	2B	VSS0		
		VSS1	3B	4B	DQ4	MEM_A_DQ<9>	17 82
82 17	MEM_A_DQ<14>	DQ0	5B	6B	DQ5	MEM_A_DQ<15>	17 82
82 17	MEM_A_DQ<13>	DQ1	7B	8B	VSS2		
		VSS4	9B	10B	DM0	MEM_A_DM<1>	17 82
82 17	MEM_A_DQS_N<1>	DQS0*	11B	12B	VSS5		
82 17	MEM_A_DQS_P<1>	DQS0	13B	14B	DQ6	MEM_A_DQ<8>	17 82
		VSS6	15B	16B	DQ7	MEM_A_DQ<12>	17 82
82 17	MEM_A_DQ<10>	DQ2	17B	18B	VSS7		
82 17	MEM_A_DQ<11>	DQ3	19B	20B	DQ12	MEM_A_DQ<2>	17 82
		VSS8	21B	22B	DQ13	MEM_A_DQ<3>	17 82
82 17	MEM_A_DQ<7>	DQ8	23B	24B	VSS9		
82 17	MEM_A_DQ<0>	DQ9	25B	26B	DM1	MEM_A_DM<0>	17 82
		VSS10	27B	28B	VSS11		
82 17	MEM_A_DQS_N<0>	DQS1*	29B	30B	CK0	MEM_CLK_P<0>	16 82
82 17	MEM_A_DQS_P<0>	DQS1	31B	32B	CK0*	MEM_CLK_N<0>	16 82
		VSS12	33B	34B	VSS13		
82 17	MEM_A_DQ<6>	DQ10	35B	36B	DQ14	MEM_A_DQ<1>	17 82
82 17	MEM_A_DQ<4>	DQ11	37B	38B	DQ15	MEM_A_DQ<5>	17 82
		VSS14	39B	40B	VSS15		
		VSS16	41B	KEY			
82 17	MEM_A_DQ<17>	DQ16	43B	42B	VSS17		
82 17	MEM_A_DQ<21>	DQ17	45B	44B	DQ20	MEM_A_DQ<18>	17 82
		VSS18	47B	46B	DQ21	MEM_A_DQ<20>	17 82
82 17	MEM_A_DQS_N<2>	DQS2*	49B	48B	VSS19		
82 17	MEM_A_DQS_P<2>	DQS2	51B	50B	NC0	PM_EXTTS_L<0>	16 45
		VSS21	53B	52B	DM2	MEM_A_DM<2>	17 82
82 17	MEM_A_DQ<23>	DQ18	55B	54B	VSS22		
82 17	MEM_A_DQ<16>	DQ19	57B	56B	DQ22	MEM_A_DQ<22>	17 82
		VSS23	59B	58B	DQ23	MEM_A_DQ<19>	17 82
82 17	MEM_A_DQ<31>	DQ24	61B	60B	VSS24		
82 17	MEM_A_DQ<27>	DQ25	63B	62B	DQ28	MEM_A_DQ<26>	17 82
		VSS25	65B	64B	DQ29	MEM_A_DQ<24>	17 82
82 17	MEM_A_DM<3>	DM3	67B	66B	VSS26		
	NC	NC1	69B	68B	DQS3*	MEM_A_DQS_N<3>	17 82
		VSS27	71B	70B	DQS3	MEM_A_DQS_P<3>	17 82
82 17	MEM_A_DQ<30>	DQ26	73B	72B	VSS28		
82 17	MEM_A_DQ<28>	DQ27	75B	74B	DQ30	MEM_A_DQ<25>	17 82
		VSS29	77B	76B	DQ31	MEM_A_DQ<29>	17 82
82 33 16	MEM_CKE<0>	CKE0	79B	78B	VSS30		
		VDD0	81B	80B	NC/CKE1	MEM_CKE<1>	16 33 82
	NC	NC2	83B	82B	VDD1		
82 33 17	MEM_A_BS<2>	BA2	85B	84B	NC/A15	MEM_A_A<15>	9
		VDD2	87B	86B	NC/A14	MEM_A_A<14>	16 33 82
82 33 17	MEM_A_A<12>	A12	89B	88B	VDD3		
82 33 17	MEM_A_A<9>	A9	91B	90B	A11	MEM_A_A<11>	17 33 82
82 33 17	MEM_A_A<8>	A8	93B	92B	A7	MEM_A_A<7>	17 33 82
		VDD4	95B	94B	A6	MEM_A_A<6>	17 33 82
82 33 17	MEM_A_A<5>	A5	97B	96B	VDD5		
82 33 17	MEM_A_A<3>	A3	99B	98B	A4	MEM_A_A<4>	17 33 82
82 33 17	MEM_A_A<1>	A1	101B	100B	A2	MEM_A_A<2>	17 33 82
		VDD6	103B	102B	A0	MEM_A_A<0>	17 33 82
82 33 17	MEM_A_A<10>	A10/AP	105B	104B	VDD7		
82 33 17	MEM_A_BS<0>	BA0	107B	106B	BA1	MEM_A_BS<1>	17 33 82
82 33 17	MEM_A_WE_L	WE*	109B	108B	RAS*	MEM_A_RAS_L	17 33 82
		VDD8	111B	110B	S0*	MEM_CS_L<0>	16 33 82
82 33 17	MEM_A_CAS_L	CAS*	113B	112B	VDD9		
82 33 16	MEM_CS_L<1>	NC/S1*	115B	114B	ODT0	MEM_ODT<0>	16 33 82
		VDD10	117B	116B	NC/A13	MEM_A_A<13>	17 33 82
82 33 16	MEM_ODT<1>	NC/ODT1	119B	118B	VDD11		
		VSS31	121B	120B	NC3	NC	
82 17	MEM_A_DQ<36>	DQ32	123B	122B	VSS32		
82 17	MEM_A_DQ<38>	DQ33	125B	124B	DQ36	MEM_A_DQ<35>	17 82
		VSS33	127B	126B	DQ37	MEM_A_DQ<39>	17 82
82 17	MEM_A_DQS_N<4>	DQS4*	129B	128B	VSS34		
82 17	MEM_A_DQS_P<4>	DQS4	131B	130B	DM4	MEM_A_DM<4>	17 82
		VSS36	133B	132B	VSS35		
82 17	MEM_A_DQ<37>	DQ34	135B	134B	DQ38	MEM_A_DQ<33>	17 82
82 17	MEM_A_DQ<34>	DQ35	137B	136B	DQ39	MEM_A_DQ<32>	17 82
		VSS38	139B	138B	VSS37		
82 17	MEM_A_DQ<56>	DQ40	141B	140B	DQ44	MEM_A_DQ<63>	17 82
82 17	MEM_A_DQ<59>	DQ41	143B	142B	DQ45	MEM_A_DQ<62>	17 82
		VSS40	145B	144B	VSS39		
82 17	MEM_A_DM<7>	DM5	147B	146B	DQS5*	MEM_A_DQS_N<7>	17 82
		VSS41	149B	148B	DQS5	MEM_A_DQS_P<7>	17 82
82 17	MEM_A_DQ<58>	DQ42	151B	150B	VSS42		
82 17	MEM_A_DQ<60>	DQ43	153B	152B	DQ46	MEM_A_DQ<57>	17 82
		VSS43	155B	154B	DQ47	MEM_A_DQ<61>	17 82
82 17	MEM_A_DQ<51>	DQ48	157B	156B	VSS44		
82 17	MEM_A_DQ<54>	DQ49	159B	158B	DQ52	MEM_A_DQ<55>	17 82
		VSS45	161B	160B	DQ53	MEM_A_DQ<50>	17 82
	NC	NC_TEST	163B	162B	VSS46		
		VSS47	165B	164B	CK1	MEM_CLK_P<1>	16 82
82 17	MEM_A_DQS_N<6>	DQS6*	167B	166B	CK1*	MEM_CLK_N<1>	16 82
82 17	MEM_A_DQS_P<6>	DQS6	169B	168B	VSS48		
		VSS49	171B	170B	DM6	MEM_A_DM<6>	17 82
82 17	MEM_A_DQ<48>	DQ50	173B	172B	VSS50		
82 17	MEM_A_DQ<53>	DQ51	175B	174B	DQ54	MEM_A_DQ<49>	17 82
		VSS51	177B	176B	DQ55	MEM_A_DQ<52>	17 82
82 17	MEM_A_DQ<43>	DQ56	179B	178B	VSS52		
82 17	MEM_A_DQ<42>	DQ57	181B	180B	DQ60	MEM_A_DQ<45>	17 82
		VSS53	183B	182B	DQ61	MEM_A_DQ<40>	17 82
82 17	MEM_A_DM<5>	DM7	185B	184B	VSS54		
		VSS55	187B	186B	DQS7*	MEM_A_DQS_N<5>	17 82
82 17	MEM_A_DQ<46>	DQ58	189B	188B	DQS7	MEM_A_DQS_P<5>	17 82
82 17	MEM_A_DQ<41>	DQ59	191B	190B	VSS56		
8	=PPSPD_S0M_MEM_A	VSS57	193B	192B	DQ62	MEM_A_DQ<44>	17 82
48	=I2C_SODIMMA_SDA	SDA	195B	194B	DQ63	MEM_A_DQ<47>	17 82
48	=I2C_SODIMMA_SCL	SCL	197B	196B	VSS58		
		VDDSPD	199B	198B	SA0		
				200B	SA1	ADDR=0xA0(WR)/0xA1(RD)	

516-0140 202

DDR2 Bypass Caps
(For return current)

=PP1V8_S3M_MEM_A

C3108 10UF 20% 6.3V X5R 603

C3109 10UF 20% 6.3V X5R 603

C3110 1UF 10% 6.3V CERM 402

C3111 1UF 10% 6.3V CERM 402

C3112 1UF 10% 6.3V CERM 402

C3113 1UF 10% 6.3V CERM 402

C3114 1UF 10% 6.3V CERM 402

C3115 1UF 10% 6.3V CERM 402

C3116 1UF 10% 6.3V CERM 402

C3117 1UF 10% 6.3V CERM 402

C3118 1UF 10% 6.3V CERM 402

C3119 1UF 10% 6.3V CERM 402

C3120 1UF 10% 6.3V CERM 402

C3121 1UF 10% 6.3V CERM 402

DDR2 SO-DIMM Connector A

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 31 OF 89	

Page Notes

Power aliases required by this page:
- =PP1V8_S3M_MEM_B
- =PP0V9_S3M_MEM_DIMMVREFB
- =PPSPD_S0M_MEM_B (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

=PP0V9_S3M_MEM_DIMMVREFB

C3201 2.2uF 20% 6.3V CERM 603
C3200 0.1uF 20% 10V CERM 402

"Expansion" (surface-mount) slot

=PP1V8_S3M_MEM_B

CRITICAL
J3200
F-RT-SM-M9
DDR2-SODIMM-DUAL

1A	VREF		2A	VSS0	
3A	VSS1		4A	DQ4	MEM_B_DQ<9>
5A	DQ0	MEM_B_DQ<15>	6A	DQ5	MEM_B_DQ<11>
7A	DQ1	MEM_B_DQ<14>	8A	VSS2	
9A	VSS4		10A	DM0	MEM_B_DM<1>
11A	DQS0*	MEM_B_DQS_N<1>	12A	VSS5	
13A	DQS0	MEM_B_DQS_P<1>	14A	DQ6	MEM_B_DQ<12>
15A	VSS6		16A	DQ7	MEM_B_DQ<8>
17A	DQ2	MEM_B_DQ<10>	18A	VSS7	
19A	DQ3	MEM_B_DQ<13>	20A	DQ12	MEM_B_DQ<3>
21A	VSS8		22A	DQ13	MEM_B_DQ<6>
23A	DQ8	MEM_B_DQ<7>	24A	VSS9	
25A	DQ9	MEM_B_DQ<2>	26A	DM1	MEM_B_DM<0>
27A	VSS10		28A	VSS11	
29A	DQS1*	MEM_B_DQS_N<0>	30A	CK0	MEM_CLK_P<4>
31A	DQS1	MEM_B_DQS_P<0>	32A	CK0*	MEM_CLK_N<4>
33A	VSS12		34A	VSS13	
35A	DQ10	MEM_B_DQ<1>	36A	DQ14	MEM_B_DQ<0>
37A	DQ11	MEM_B_DQ<4>	38A	DQ15	MEM_B_DQ<5>
39A	VSS14		40A	VSS15	
KEY					
41A	VSS16		42A	VSS17	
43A	DQ16	MEM_B_DQ<21>	44A	DQ20	MEM_B_DQ<22>
45A	DQ17	MEM_B_DQ<19>	46A	DQ21	MEM_B_DQ<18>
47A	VSS18		48A	VSS19	
49A	DQS2*	MEM_B_DQS_N<2>	50A	NC0	PM_EXTTS_L<1>
51A	DQS2	MEM_B_DQS_P<2>	52A	DM2	MEM_B_DM<2>
53A	VSS21		54A	VSS22	
55A	DQ18	MEM_B_DQ<20>	56A	DQ22	MEM_B_DQ<17>
57A	DQ19	MEM_B_DQ<23>	58A	DQ23	MEM_B_DQ<16>
59A	VSS23		60A	VSS24	
61A	DQ24	MEM_B_DQ<29>	62A	DQ28	MEM_B_DQ<26>
63A	DQ25	MEM_B_DQ<24>	64A	DQ29	MEM_B_DQ<28>
65A	VSS25		66A	VSS26	
67A	DM3	MEM_B_DM<3>	68A	DQS3*	MEM_B_DQS_N<3>
69A	NC1	NC	70A	DQS3	MEM_B_DQS_P<3>
71A	VSS27		72A	VSS28	
73A	DQ26	MEM_B_DQ<27>	74A	DQ30	MEM_B_DQ<31>
75A	DQ27	MEM_B_DQ<25>	76A	DQ31	MEM_B_DQ<30>
77A	VSS29		78A	VSS30	
79A	CKE0	MEM_CKE<3>	80A	NC/CKE1	MEM_CKE<4>
81A	VDD0		82A	VDD1	
83A	NC2	NC	84A	NC/A15	MEM_B_A<15>
85A	BA2	MEM_B_BS<2>	86A	NC/A14	MEM_B_A<14>
87A	VDD2		88A	VDD3	
89A	A12	MEM_B_A<12>	90A	A11	MEM_B_A<11>
91A	A9	MEM_B_A<9>	92A	A7	MEM_B_A<7>
93A	A8	MEM_B_A<8>	94A	A6	MEM_B_A<6>
95A	VDD4		96A	VDD5	
97A	A5	MEM_B_A<5>	98A	A4	MEM_B_A<4>
99A	A3	MEM_B_A<3>	100A	A2	MEM_B_A<2>
101A	A1	MEM_B_A<1>	102A	A0	MEM_B_A<0>
103A	VDD6		104A	VDD7	
105A	A10/AP	MEM_B_A<10>	106A	BA1	MEM_B_BS<1>
107A	BA0	MEM_B_BS<0>	108A	RAS*	MEM_B_RAS_L
109A	WE*	MEM_B_WE_L	110A	S0*	MEM_CS_L<2>
111A	VDD8		112A	VDD9	
113A	CAS*	MEM_B_CAS_L	114A	ODT0	MEM_ODT<2>
115A	NC/S1*	MEM_CS_L<3>	116A	NC/A13	MEM_B_A<13>
117A	VDD10		118A	VDD11	
119A	NC/ODT1	MEM_ODT<3>	120A	NC3	NC
121A	VSS31		122A	VSS32	
123A	DQ32	MEM_B_DQ<36>	124A	DQ36	MEM_B_DQ<32>
125A	DQ33	MEM_B_DQ<33>	126A	DQ37	MEM_B_DQ<37>
127A	VSS33		128A	VSS34	
129A	DQS4*	MEM_B_DQS_N<4>	130A	DM4	MEM_B_DM<4>
131A	DQS4	MEM_B_DQS_P<4>	132A	VSS35	
133A	VSS36		134A	DQ38	MEM_B_DQ<38>
135A	DQ34	MEM_B_DQ<34>	136A	DQ39	MEM_B_DQ<39>
137A	DQ35	MEM_B_DQ<35>	138A	VSS37	
139A	VSS38		140A	DQ44	MEM_B_DQ<56>
141A	DQ40	MEM_B_DQ<57>	142A	DQ45	MEM_B_DQ<59>
143A	DQ41	MEM_B_DQ<60>	144A	VSS39	
145A	VSS40		146A	DQS5*	MEM_B_DQS_N<7>
147A	DM5	MEM_B_DM<7>	148A	DQS5	MEM_B_DQS_P<7>
149A	VSS41		150A	VSS42	
151A	DQ42	MEM_B_DQ<61>	152A	DQ46	MEM_B_DQ<63>
153A	DQ43	MEM_B_DQ<62>	154A	DQ47	MEM_B_DQ<58>
155A	VSS43		156A	VSS44	
157A	DQ48	MEM_B_DQ<48>	158A	DQ52	MEM_B_DQ<54>
159A	DQ49	MEM_B_DQ<51>	160A	DQ53	MEM_B_DQ<53>
161A	VSS45		162A	VSS46	
163A	NC_TEST	NC	164A	CK1	MEM_CLK_P<3>
165A	VSS47		166A	CK1*	MEM_CLK_N<3>
167A	DQS6*	MEM_B_DQS_N<6>	168A	VSS48	
169A	DQS6	MEM_B_DQS_P<6>	170A	DM6	MEM_B_DM<6>
171A	VSS49		172A	VSS50	
173A	DQ50	MEM_B_DQ<50>	174A	DQ54	MEM_B_DQ<52>
175A	DQ51	MEM_B_DQ<55>	176A	DQ55	MEM_B_DQ<49>
177A	VSS51		178A	VSS52	
179A	DQ56	MEM_B_DQ<40>	180A	DQ60	MEM_B_DQ<46>
181A	DQ57	MEM_B_DQ<47>	182A	DQ61	MEM_B_DQ<43>
183A	VSS53		184A	VSS54	
185A	DM7	MEM_B_DM<5>	186A	DQS7*	MEM_B_DQS_N<5>
187A	VSS55		188A	DQS7	MEM_B_DQS_P<5>
189A	DQ58	MEM_B_DQ<42>	190A	VSS56	
191A	DQ59	MEM_B_DQ<45>	192A	DQ62	MEM_B_DQ<41>
193A	VSS57		194A	DQ63	MEM_B_DQ<44>
195A	SDA	=I2C_SODIMMB_SDA	196A	VSS58	
197A	SCL	=I2C_SODIMMB_SCL	198A	SA0	Resistor prevents pwr-gnd short
199A	VDDSPD	=PPSPD_S0M_MEM_B	200A	SA1	SODIMM_B_SA1

202 204 516S0471

203 201

ADDR=0xA4(WR)/0xA5(RD)

R3200 10K 5% 1/16W MF-LF 402 =PPSPD_S0M_MEM_B

DDR2 Bypass Caps

(For return current)

=PP1V8_S3M_MEM_B

C3208 10UF 20% 6.3V X5R 603
C3209 10UF 20% 6.3V X5R 603
C3210 1UF 10% 6.3V CERM 402
C3211 0.1UF 20% 10V CERM 402
C3212 1UF 10% 6.3V CERM 402
C3213 1UF 10% 6.3V CERM 402
C3214 1UF 10% 6.3V CERM 402
C3215 1UF 10% 6.3V CERM 402
C3216 1UF 10% 6.3V CERM 402
C3217 0.1UF 20% 10V CERM 402
C3218 0.1UF 20% 10V CERM 402
C3219 0.1UF 20% 10V CERM 402
C3220 0.1UF 20% 10V CERM 402
C3221 0.1UF 20% 10V CERM 402

DDR2 SO-DIMM Connector B

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

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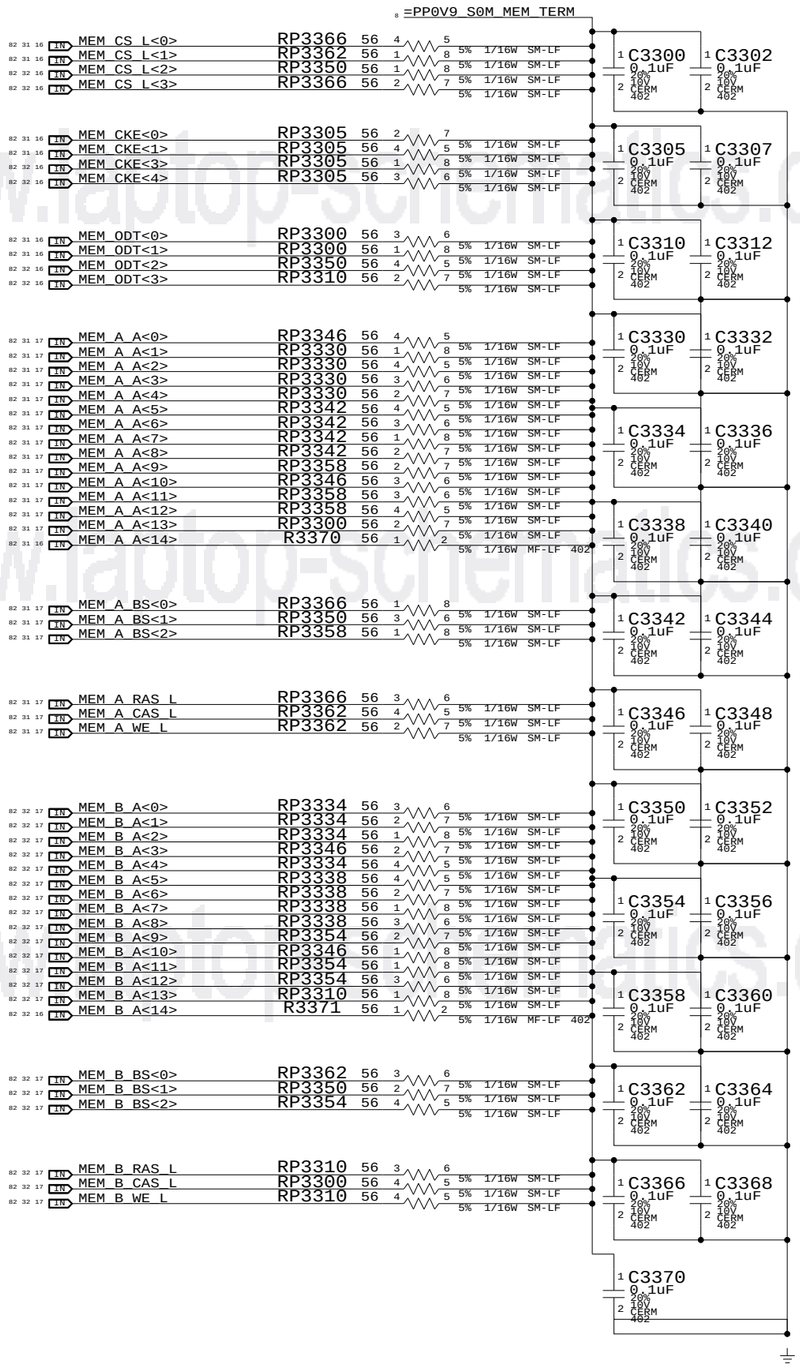
SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 32 OF 89	

One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=(T9_NOME) SYNC_DATE=11/14/2006

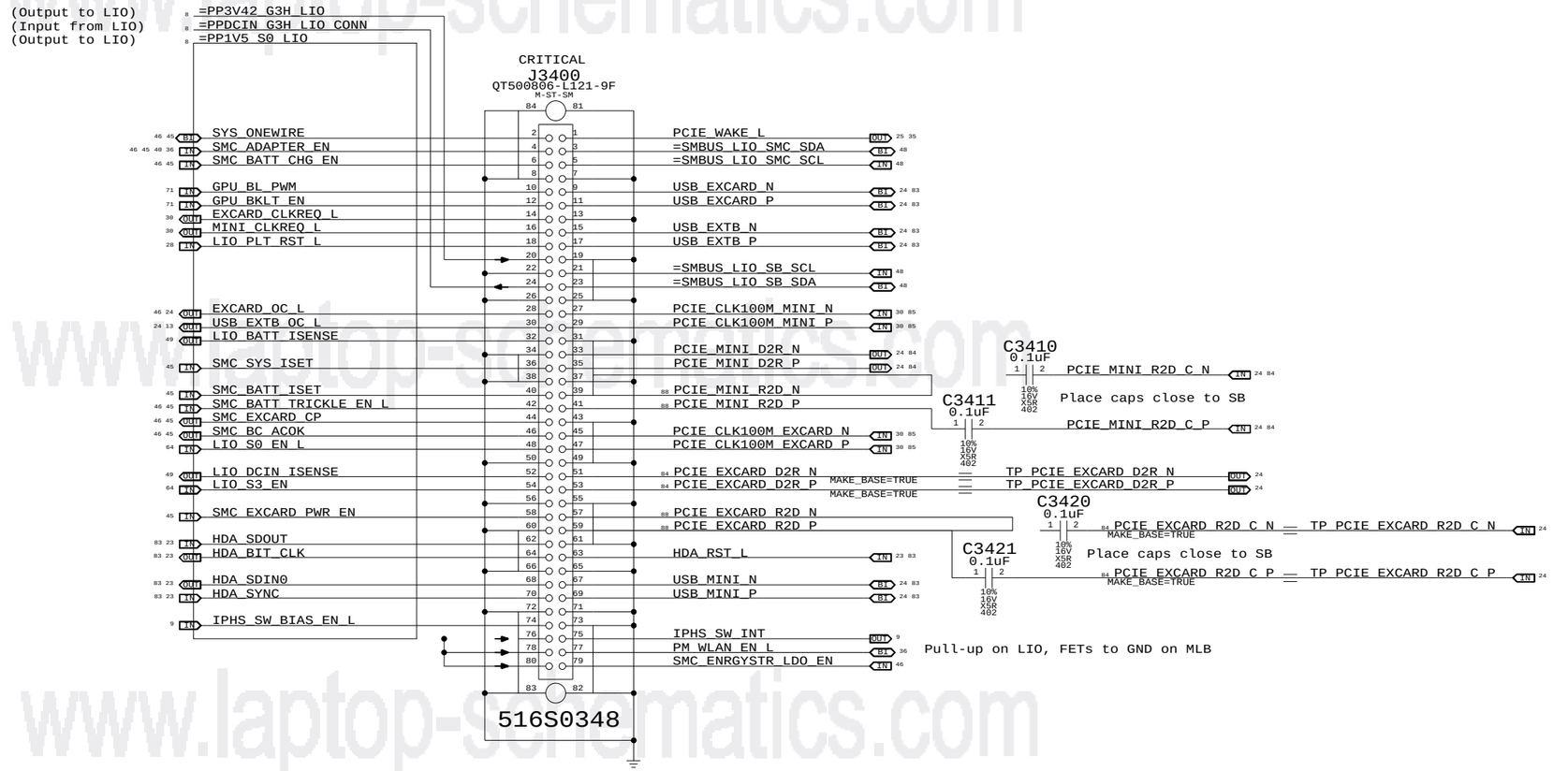
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0

SCALE: NONE

SHT 33 OF 89

Left I/O Board Connector



Left I/O Board Connector

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 34 OF 89	

Page Notes

Power aliases required by this page:
- =PP3V3_ENET_PHY (EC / Ultra)
- =PP1V8R2V5_ENET_PHY (2.5V / 1.8V)
- =YUKON_EC_PP2V5_ENET (2.5V / GND)
- =PP1V2_ENET_PHY

Signal aliases required by this page:
- =ENET_CLKREQ_L (NC/TP for Yukon EC)
- =ENET_VMAIN_AVLBL (See note by pin)

BOM options provided by this page:
YUKON_EC - Selects Yukon EC RSET value.
YUKON_ULTRA - Selects Yukon Ultra RSET.

NOTE: See bottom of page for instructions for dual Yukon EC / Yukon Ultra schematic support.

=PP1V2_ENET_PHY

Yukon EC		Yukon Ultra	
No link:	171 mA	No link:	130 mA
10 Mbps:	179 mA	10 Mbps:	130 mA
100 Mbps:	203 mA	100 Mbps:	150 mA
1000 Mbps:	426 mA	1000 Mbps:	290 mA

C3700 4.7UF 20% 6.3V CERM 603; C3701 0.1UF 10% 16V X5R 402; C3702 0.1UF 10% 16V X5R 402; C3703 0.1UF 10% 16V X5R 402; C3704 0.1UF 10% 16V X5R 402; C3705 0.1UF 10% 16V X5R 402; C3706 0.001UF 10% 50V CERM 402; C3707 0.001UF 10% 50V CERM 402; C3708 0.001UF 10% 50V CERM 402

=PP3V3_ENET_PHY

Yukon EC		Yukon Ultra	
No link:	4 mA	No link:	60 mA
10 Mbps:	4 mA	10 Mbps:	70 mA
100 Mbps:	4 mA	100 Mbps:	70 mA
1000 Mbps:	4 mA	1000 Mbps:	80 mA

C3710 4.7UF 20% 6.3V CERM 603; C3711 0.1UF 10% 16V X5R 402; C3712 0.1UF 10% 16V X5R 402; C3713 0.1UF 10% 16V X5R 402; C3714 0.001UF 10% 50V CERM 402; C3715 0.001UF 10% 50V CERM 402

=PP1V8R2V5_ENET_PHY L3720 FERR-120-OHM-1.5A 0402 PP1V8R2V5_ENET_PHY_AVDD MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.8V

Yukon EC (2.5V)		Yukon Ultra (1.8V)	
No link:	82 mA	No link:	0 mA
10 Mbps:	108 mA	10 Mbps:	30 mA
100 Mbps:	126 mA	100 Mbps:	40 mA
1000 Mbps:	218 mA	1000 Mbps:	150 mA

(EC:2.5V)

C3720 4.7UF 20% 6.3V CERM 603; C3721 0.1UF 10% 16V X5R 402; C3722 0.1UF 10% 16V X5R 402; C3723 0.1UF 10% 16V X5R 402; C3724 0.001UF 10% 50V CERM 402

=YUKON_EC_PP2V5_ENET

Yukon EC: Alias to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF & 1x 0.001uF caps
Yukon Ultra: Alias to GND

PCIE_ENET_D2R_P
PCIE_ENET_D2R_N
PCIE_ENET_R2D_C_P
PCIE_ENET_R2D_C_N
C3735 0.1UF 10% 16V X5R 402
C3736 0.1UF 10% 16V X5R 402
C3730 0.1UF 10% 16V X5R 402 PLACEMENT_NOTE=Place C3730 close to southbridge.
C3731 0.1UF 10% 16V X5R 402 PLACEMENT_NOTE=Place C3731 close to southbridge.
PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
Yukon EC: Pin 42 should be NC (or TP) net.
=ENET_CLKREQ_L
PCIE_WAKE_L
ENET_RESET_L
ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>

SIGNAL_MODEL=EMPTY R3740 R3741 R3742 R3743 R3744 R3745 R3746 R3747 49.9 1% 1/16W MF-LF 402
ENET_MDI0 ENET_MDI1 ENET_MDI2 ENET_MDI3
C3740 C3742 C3744 C3746 0.001UF 10% 50V CERM 402

ENET_CLK25M_XTALI
ENET_CLK25M_XTALO

U3700 88E8058 QFN CRITICAL OMIT

PCIE_ENET_D2R_C_P	49	TX_P	
PCIE_ENET_D2R_C_N	50	TX_N	
PCIE_ENET_R2D_P	54	RX_P	
PCIE_ENET_R2D_N	53	RX_N	
	55	REFCLKP	
	56	REFCLKN	
	42	CLKREQ*	EC:NO CONNECT
	6	WAKE*	
	5	PERST*	
	17	MDIP0	
	18	MDIN0	
	20	MDIP1	
	21	MDIN1	
	26	MDIP2	
	27	MDIN2	
	30	MDIP3	
	31	MDIN3	
ENET_CLK25M_XTALI	15	XTALI	
ENET_CLK25M_XTALO	14	XTALO	
	65	THRML_PAD	

PCI EXPRESS

ANALOG: EC:CTRL25 CTRL18 4 TP_YUKON_CTRL18; CTRL12 3 TP_YUKON_CTRL12; RSET 16 YUKON_RSET

LED: LED_ACT* 59 NC; LED_LINK10/100* 60 NC; LED_LINK1000* 62 NC; LED_DUPLEX* 63 NC

SPI: (IPU) SPI_DO 34 NC; SPI_DI 35 NC; SPI_CLK 37 NC; SPI_CS 36 NC

MEDIA

TWSI: (IPU) VPD_CLK 38 YUKON_VPD_CLK; (IPU) VPD_DATA 41 YUKON_VPD_DATA

TEST/RSVD: (IPD) TESTMODE 46; RSVD_24 24 NC; RSVD_25 25 NC; RSVD_29 29 NC; RSVD_43 43 NC

MAIN CLK

R3760 4.7K 5% 1/10W MF-LF 402

LOM_DISABLE* 10 ENET_LOM_DIS_L

VAUX_AVLBL 12
SWITCH_VAUX 9 NC
VMAIN_AVLBL 47 Must be high in S0 state (can use PP3V3_S0 as input) =ENET_VMAIN_AVLBL
SWITCH_VCC 11 NC

YUKON_ULTRA R3765 4.99K 1% 1/10W MF-LF 402

VPD ROM
C3780 0.1UF 10% 16V X5R 402
R3780 4.7K 5% 1/10W MF-LF 402
R3781 4.7K 5% 1/10W MF-LF 402
U3780 M24C08 SO8 CRITICAL
E2 NC1 NC0 WC* VCC SDA SCL VSS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0386	1	IC,88E8058,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	YUKON_ULTRA
341S2060	1	IC,FLASH,88E8058 ETHERNET VPD,IIC,SO8	U3780	CRITICAL	YUKON_ULTRA
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	YUKON_EC
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U3780	CRITICAL	YUKON_EC
114S0285	1	RES,4.87K,1%,1/16W,0402,LF	R3760		YUKON_EC

To support Yukon EC and Ultra on the same board:
- Alias =YUKON_EC_PP2V5_ENET to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF and 1x 0.001uF caps
- Use 0-ohm resistors or variable supply to provide 1.8V or 2.5V to =PP1V8R2V5_ENET_PHY and magnetics. Can also use BCP69T1 connected to CTRL18 pin 4 for internal VR.
- Connect =ENET_CLKREQ_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON_ULTRA)
- Use YUKON_EC and YUKON_ULTRA BOMOPTIONs to select stuffed part

Ethernet (Yukon)

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 35 OF 89	

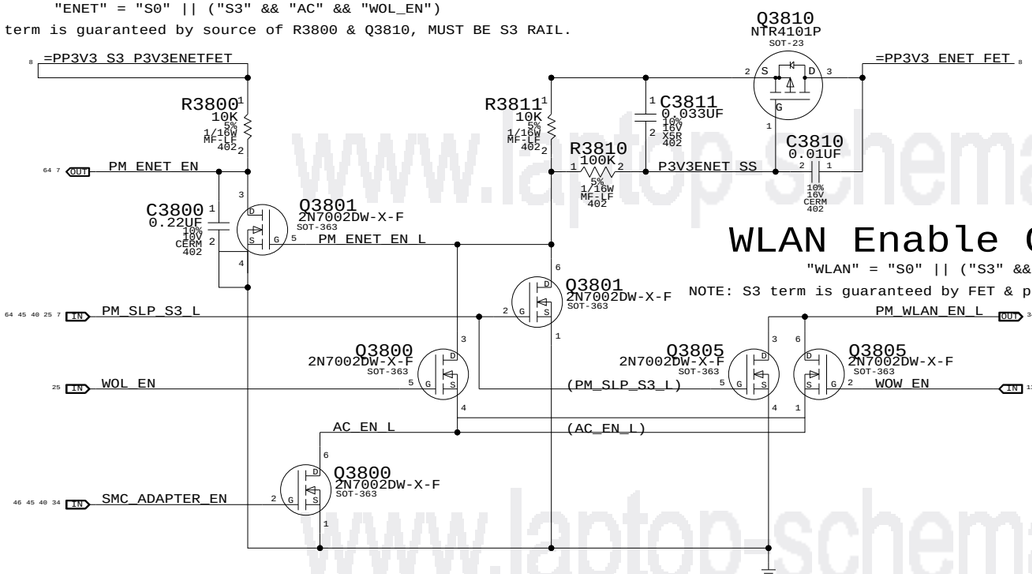
ENET Enable Generation

"ENET" = "S0" || ("S3" && "AC" && "WOL_EN")

NOTE: S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.

3.3V ENET FET

CRITICAL



WLAN Enable Generation

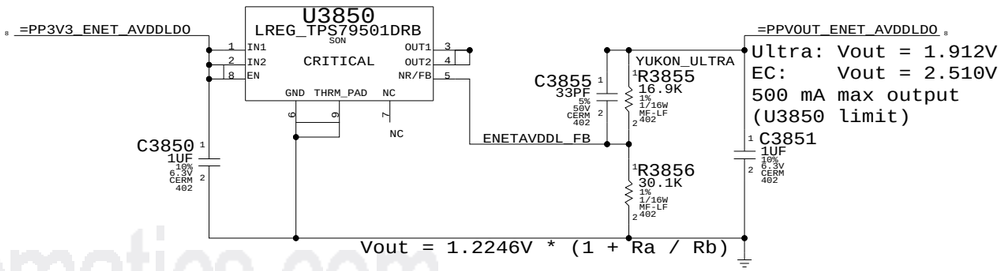
"WLAN" = "S0" || ("S3" && "AC" && "WOW_EN")

NOTE: S3 term is guaranteed by FET & pull-up source, MUST BE S3 RAIL.

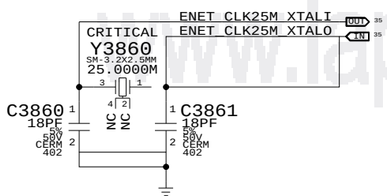
Yukon AVDDL LDO

1.9V for Yukon Ultra, 2.5V for Yukon EC

Yukon Ultra requires 1.9V on its magnetics to pass compliance tests



Yukon Crystal



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0363	1	RES,31.6K,1%,1/16W,402,LF	R3855		YUKON_EC

Yukon Power Control

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0

SCALE: NONE

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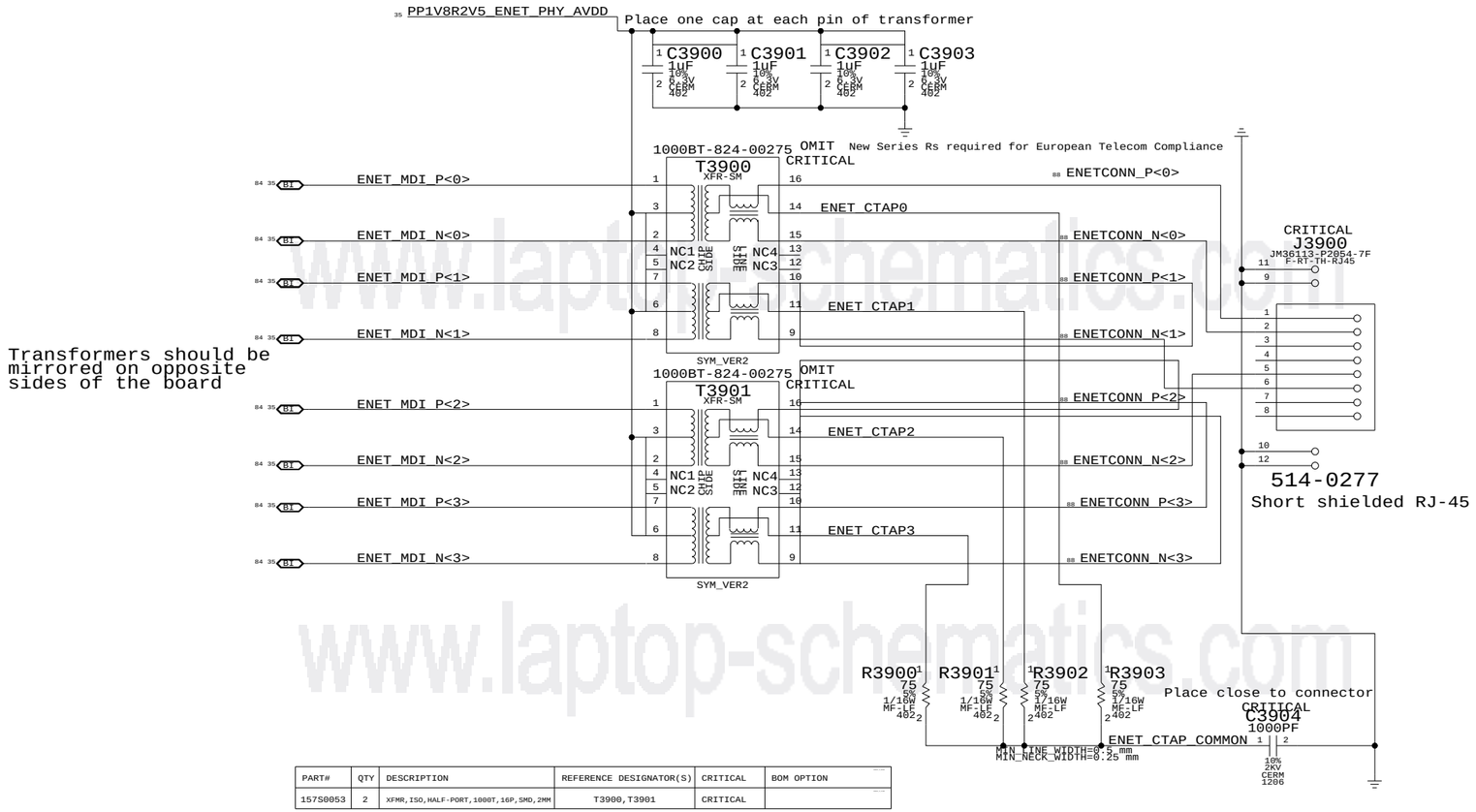
Page Notes

Power aliases required by this page:
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Transformers should be mirrored on opposite sides of the board

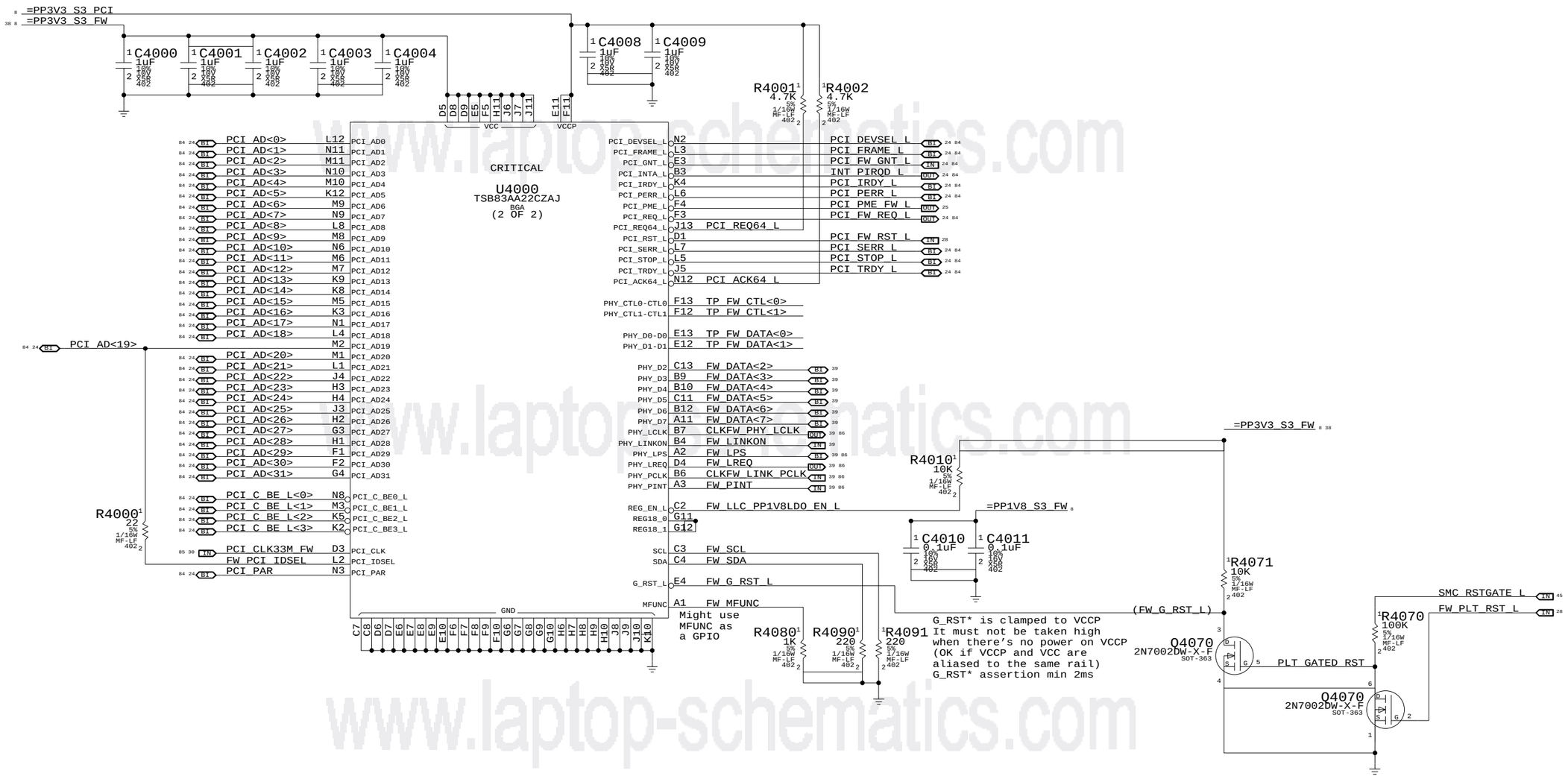
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
157S0053	2	XFMR,ISO,HALF-PORT,1000T,16P,SMD,2MM	T3900,T3901	CRITICAL	

Ethernet Connector

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 37 OF 89	



FireWire Link (TSB83AA22)

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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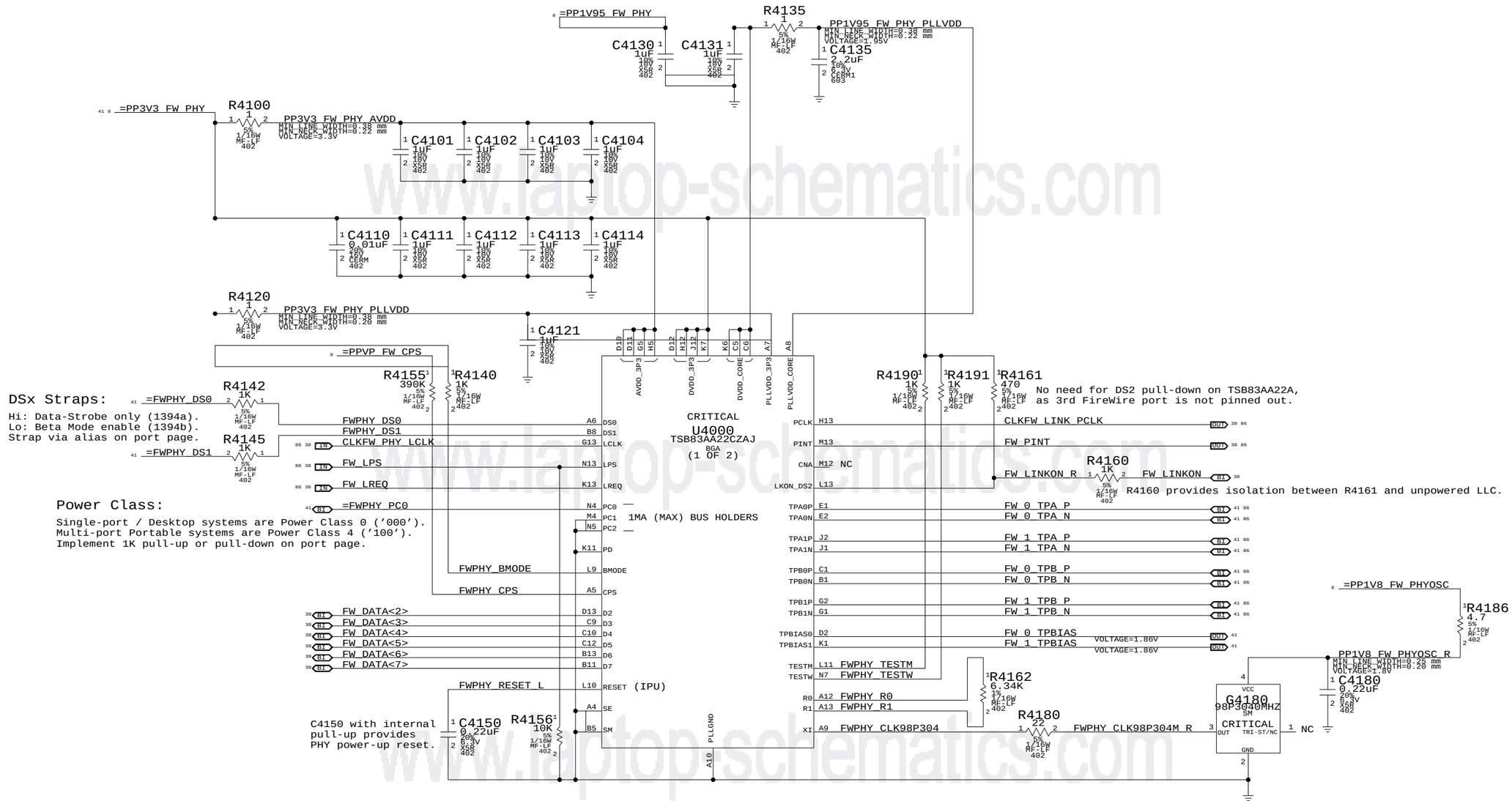
SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0

SCALE: NONE

SHT 38 OF 89



FireWire PHY (TSB83AA22)

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 39 OF 89	

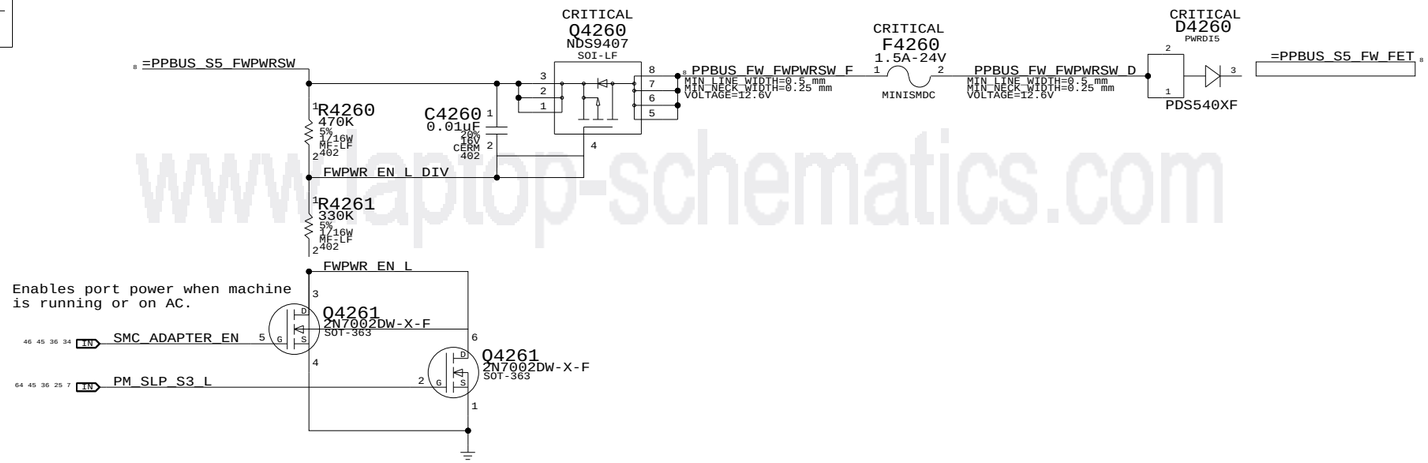
Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

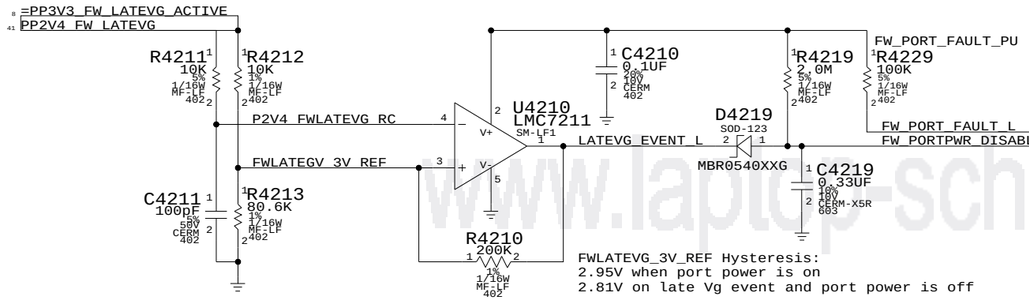
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- FW_PORT_FAULT_PU

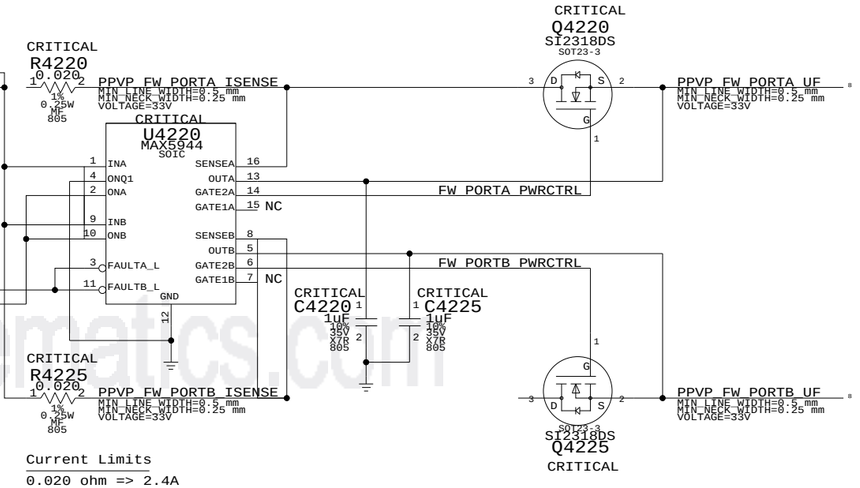
FireWire Port Power Switch



Late-VG Event Detection



Current Limit/Active Late-VG Protection



Current Limits

0.020 ohm => 2.4A
0.025 ohm => 2A
0.030 ohm => 1.66A (Ideal)
0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

FireWire Port Power

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 40 OF 89	

Page Notes

Power aliases required by this page:
- =PPVP_FW_PORT0
- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG
- =GND_CHASSIS_FW_PORT0L
- =GND_CHASSIS_FW_PORT0U
- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:
- 2-port Portable Power Class (4)
- Port "0" Data-Strobe only (1394A)
- Port "1" Bilingual (1394B)

39 8 =PP3V3_FW_PHY
39 =FWPHY_PC0
39 =FWPHY_DS0
39 =FWPHY_DS1

Termination

Place close to FireWire PHY

TI PHYs require 1uF even though FW spec calls out 0.33uF

39 FW_1_TPBIAS
39 FW_0_TPBIAS
C4350 1uF 10% 6.3V CERM 402
C4360 1uF 10% 6.3V CERM 402
CRITICAL L4360 18NH-250MA 0402
CRITICAL L4361 18NH-250MA 0402
FW_B_TPA_L_P
FW_B_TPA_L_N
R4350 56.2 1% 1/16W MF-LF 402
R4351 56.2 1% 1/16W MF-LF 402
R4360 56.2 1% 1/16W MF-LF 402
R4361 56.2 1% 1/16W MF-LF 402
86 39 FW_0_TPA_P
86 39 FW_0_TPA_N
86 39 FW_0_TPB_P
86 39 FW_0_TPB_N
86 39 FW_1_TPA_P
86 39 FW_1_TPA_N
86 39 FW_1_TPB_P
86 39 FW_1_TPB_N
FW_PORT0_TPA_P MAKE_BASE=TRUE 41
FW_PORT0_TPA_N MAKE_BASE=TRUE 41
FW_PORT0_TPB_P MAKE_BASE=TRUE 41
FW_PORT0_TPB_N MAKE_BASE=TRUE 41
FW_PORT1_TPA_P MAKE_BASE=TRUE 41
FW_PORT1_TPA_N MAKE_BASE=TRUE 41
FW_PORT1_TPB_P MAKE_BASE=TRUE 41
FW_PORT1_TPB_N MAKE_BASE=TRUE 41
SIGNAL_MODEL=EMPTY
R4352 56.2 1% 1/16W MF-LF 402
R4353 56.2 1% 1/16W MF-LF 402
R4362 56.2 1% 1/16W MF-LF 402
R4363 56.2 1% 1/16W MF-LF 402
FW_B_TPB_L_N
FW_B_TPB_L_P
CRITICAL L4362 18NH-250MA 0402 SIGNAL_MODEL=EMPTY
CRITICAL L4363 18NH-250MA 0402 SIGNAL_MODEL=EMPTY
FW_PORT0_TPB_C
FW_PORT1_TPB_C
C4354 220pF 5% 50V CERM 402
R4354 4.99K 1% 1/16W MF-LF 402
C4364 220pF 5% 50V CERM 402
R4364 4.99K 1% 1/16W MF-LF 402

Late-VG Protection Power

8 =PP3V3_FW_LATEVG
R4390 332 1% 1/16W MF-LF 402
PP2V4_FW_LATEVG 40 41
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=2.4V
CRITICAL D4390 MMBZ5227B SOT23

PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4390 should be 390 Ohms max for a 3.3V rail

ESD and late-VG rail for snap-back diodes (Common to all ports)

Cable Power

"Snapback" & "Late VG" Protection

8 =PPVP_FW_PORT0
CRITICAL L4300 FERR-250-OHM SM
PPVP_FW_PORT0
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=33V
Note: Trace PPVP_FW_PORT0 must handle up to 5A
C4304 0.01UF 10% 50V X7R 402
41 40 PP2V4_FW_LATEVG
DP4300 BAV99DW-X-F SOT-363
C4300 0.01uF 10% 50V X7R 402
C4301 0.01uF 10% 50V X7R 402
41 FW_PORT0_TPA_P
41 FW_PORT0_TPA_N
41 FW_PORT0_TPB_P
41 FW_PORT0_TPB_N
DP4301 BAV99DW-X-F SOT-363
C4302 0.01uF 10% 50V X7R 402
C4303 0.01uF 10% 50V X7R 402
CRITICAL FL4300 90-OHM-100MA 1210-4SM1
CRITICAL FL4301 90-OHM-100MA 1210-4SM1
88 FW_PORT0_TPA_FL_P
88 FW_PORT0_TPA_FL_N
88 FW_PORT0_TPB_FL_P
88 FW_PORT0_TPB_FL_N
(GND_FW_PORT0_VG)

PORT 0
1394A
CRITICAL J4300 1394A F-RT-TH-LF
6 TPO (TPA+)
5 TPO# (TPA-)
4 TPI (TPB+)
3 TPI# (TPB-)
1 VP
2 VGND
7 8 9 10
514-0255

Cable Power

"Snapback" & "Late VG" Protection

8 =PPVP_FW_PORT1
CRITICAL L4310 FERR-250-OHM SM
PPVP_FW_PORT1
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=33V
Note: Trace PPVP_FW_PORT1 must handle up to 5A
C4314 0.01UF 10% 50V X7R 402
41 40 PP2V4_FW_LATEVG
DP4310 BAV99DW-X-F SOT-363
C4311 0.01uF 10% 50V X7R 402
C4310 0.01uF 10% 50V X7R 402
41 FW_PORT1_TPB_N
41 FW_PORT1_TPB_P
41 FW_PORT1_TPA_N
41 FW_PORT1_TPA_P
DP4311 BAV99DW-X-F SOT-363
C4312 0.01uF 10% 50V X7R 402
C4313 0.01uF 10% 50V X7R 402
C4319 0.1uF 10% 50V X7R 603-1
R4319 1M 5% 1/16W MF-LF 402
(FW_PORT1_BREF)
(GND_FW_PORT1_VG)
FW_PORT1_AREF

PORT 1
BILINGUAL
CRITICAL J4310 1394B-UG31903 F-RT-SM1
10 11
1 TPB-
9 TPB<R> OUTPUT
2 TPB+
8 VP
NC 7 NC
6 VG
3 TPA-
5 TPA<R> INPUT
4 TPA+
514S0133

PLACEMENT_NOTE=Place C4319 close to connector pin 5.

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

FireWire Ports

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 41 OF 89	

IDE (ODD) Connector

=PP3V3_S0_IDE

CRITICAL
Q4420
FDC606P
SOT-6

PP5V_ODD
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=5V

=PP5V_S0_ODD

R4420 10K 5% 1/16W MF-LF 402

C4422 0.068UF 10% 10V CERM 402

R4421 47K 5% 1/16W MF-LF 402

C4421 0.01UF 10% 16V CERM 402

P5VODD_SS

R4402 4.7K 5% 1/16W MF-LF 402

=PP5V_S0_ODDPWREN

R4422 100K 5% 1/16W MF-LF 402

R4410 33K 5% 1/16W MF-LF 402

P5VODD_EN_L

ODD_PWR_EN

Q4421
2N7002DW-X-F
SOT-363

Q4421
2N7002DW-X-F
SOT-363

IN ODD_PWR_EN_L

(ODD has internal 100K pull-up to 5V)

CRITICAL
J4400
M-ST-SM1-LF

ODD_RST_BUF_L

IDE_PDD<7>	IDE_PDD<6>	IDE_PDD<5>	IDE_PDD<4>
IDE_PDD<3>	IDE_PDD<2>	IDE_PDD<1>	IDE_PDD<0>
IDE_PDIOW_L	IDE_PDIOR_L	IDE_PDDACK_L	IDE_PDA<1>
IDE_PDCS1_L	IDE_PDA<2>		

IDE_PDD<8>	IDE_PDD<9>	IDE_PDD<10>	IDE_PDD<11>
IDE_PDD<12>	IDE_PDD<13>	IDE_PDD<14>	IDE_PDD<15>
IDE_PDDREQ	IDE_PDIORDY	IDE_IRQ14	IDE_PDA<0>
IDE_PDCS3_L			

NC

(SB has internal pulldown 5.7k-23.5k)
(UATA_DSTROBE)
(UATA_STOP)
(UATA_HSTROBE)
(UATA_CS0*)
(UATA_CS1*)

Indicates disk presence
SMC_ODD_DETECT

516S0335

R4403 6.2K 5% 1/16W MF-LF 402

=PP5V_S0_PCIREQFIX

R4430 100K 5% 1/16W MF-LF 402

U4430 MC74VHC1G09 SC70

IN ODD_RST_5VTOL_L

ODD_RST_BUF_L

Unused SATA Ports

SATA_B_R2D_C_P	TP_SATA_B_R2DP	MAKE_BASE=TRUE
SATA_B_R2D_C_N	TP_SATA_B_R2DN	MAKE_BASE=TRUE
SATA_B_D2R_P	TP_SATA_B_D2RP	MAKE_BASE=TRUE
SATA_B_D2R_N	TP_SATA_B_D2RN	MAKE_BASE=TRUE
SATA_C_R2D_C_P	TP_SATA_C_R2DP	MAKE_BASE=TRUE
SATA_C_R2D_C_N	TP_SATA_C_R2DN	MAKE_BASE=TRUE
SATA_C_D2R_P	TP_SATA_C_D2RP	MAKE_BASE=TRUE
SATA_C_D2R_N	TP_SATA_C_D2RN	MAKE_BASE=TRUE

SATA_RBIAS_P
SATA_RBIAS_N
SATA_RBIAS
MAKE_BASE=TRUE

R4460 24.9 1% 1/16W MF-LF 402

Placement note
Place within 12.7mm
from ball of SB

PATA Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

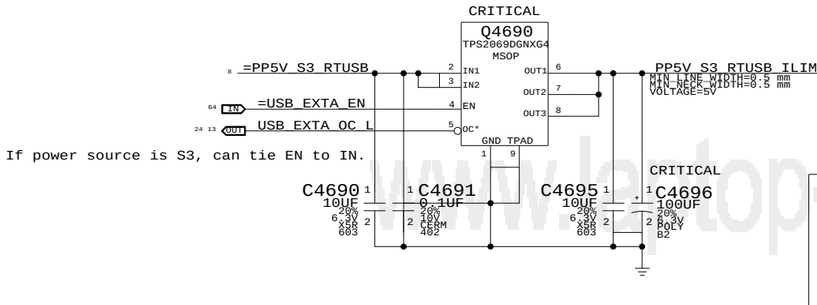
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0

SCALE: NONE

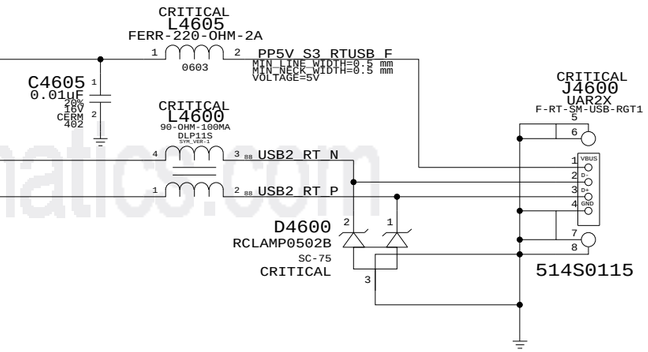
SHT 42 OF 89

Port Power Switch



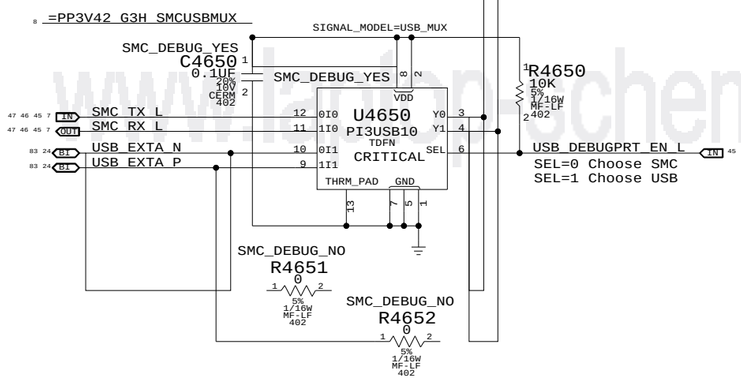
If power source is S3, can tie EN to IN.

Right USB Port



Place L4600 and L4605 at connector pin

USB/SMC Debug Mux



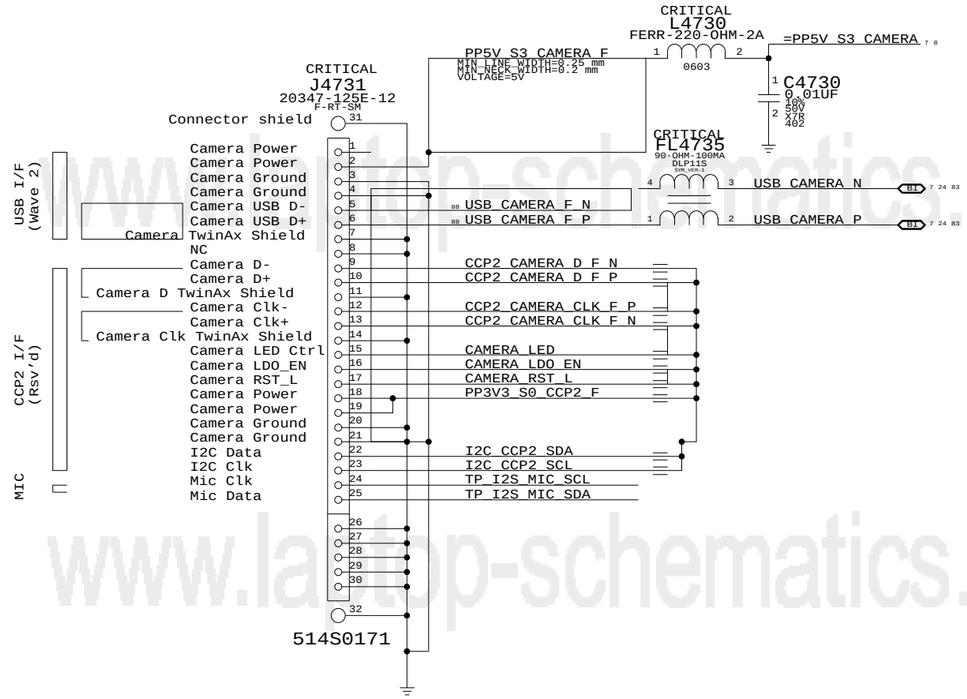
External USB Connector

SYNC_MASTER=M88 SYNC_DATE=08/02/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 43 OF 89	

Left Clutch Barrel Interconnect



Left Clutch Barrel Interconnect

SYNC_MASTER=M87 SYNC_DATE=07/16/2007

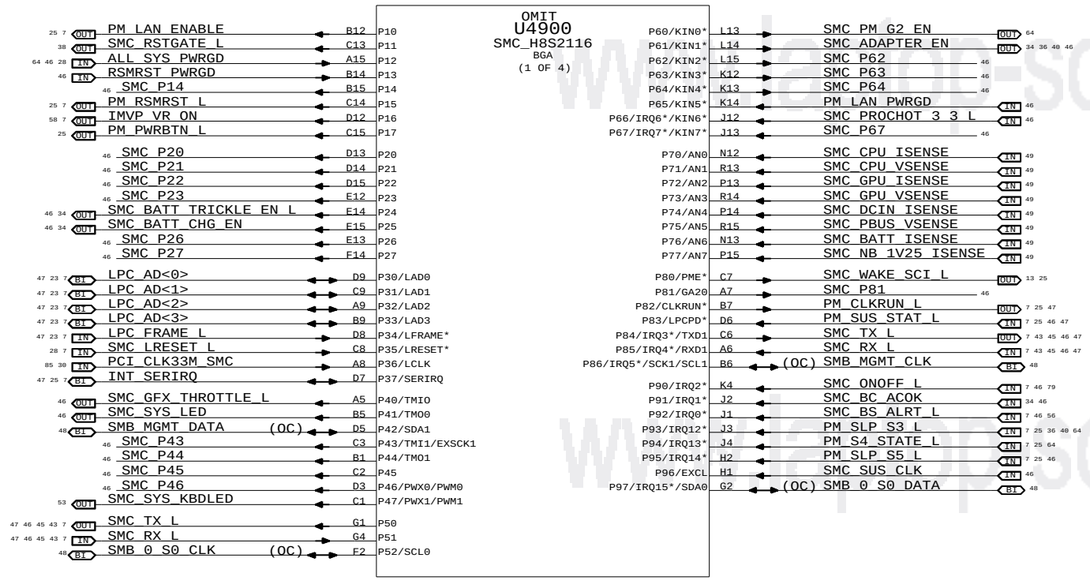
APPLE INC.

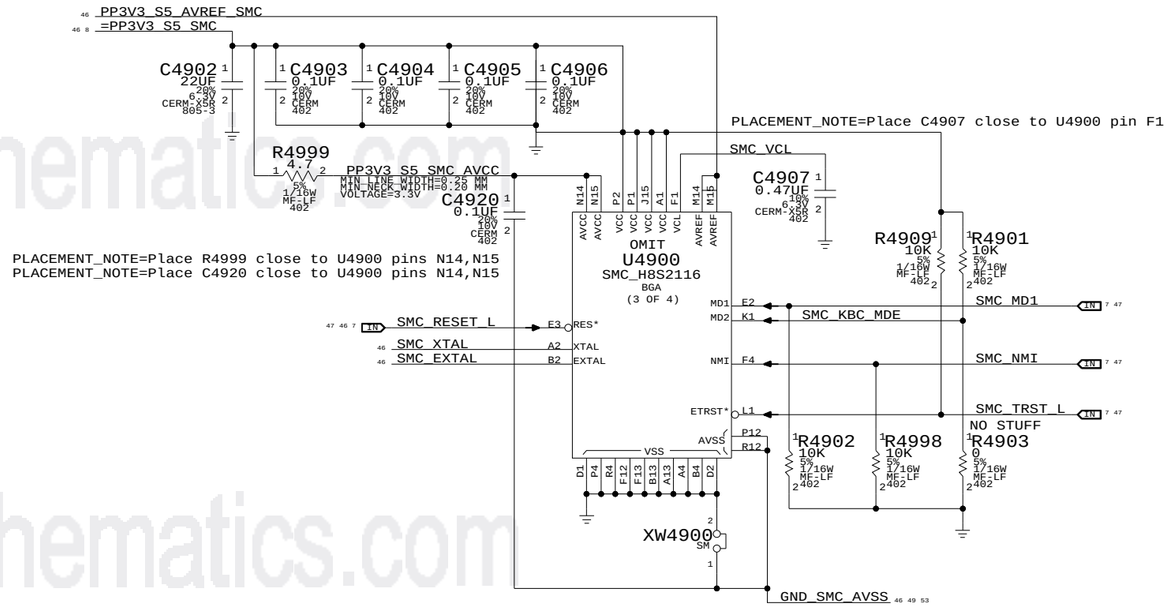
SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0

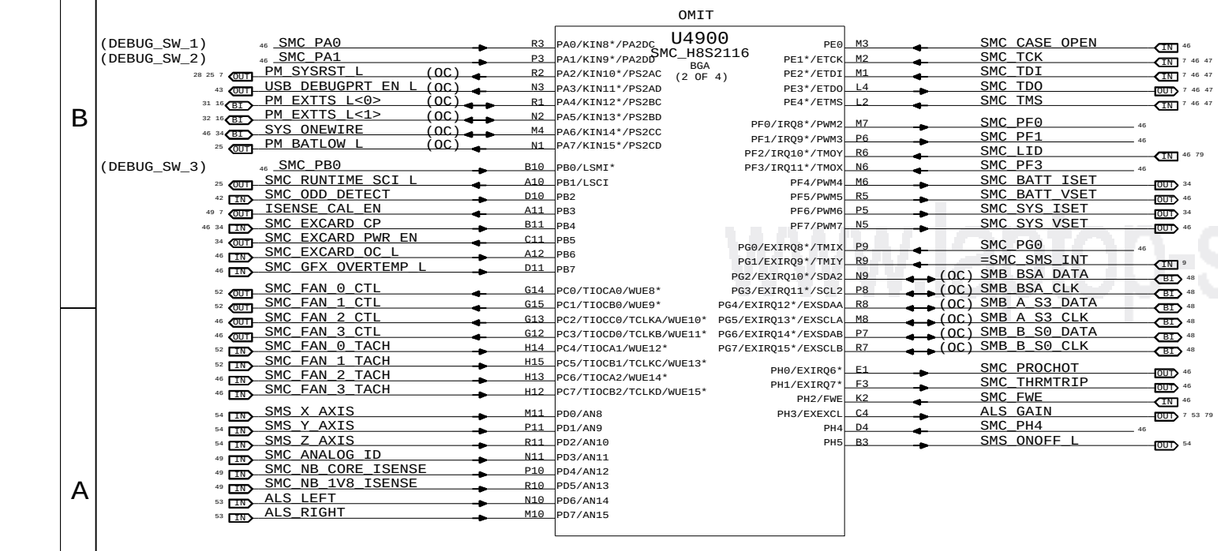
SCALE NONE

SHT 44 OF 89

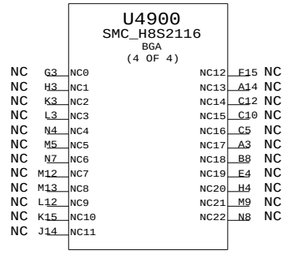
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.







NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.



SMC			
SYNC_MASTER=T9_NOME	SYNC_DATE=01/17/2007		
NOTICE OF PROPRIETARY PROPERTY			
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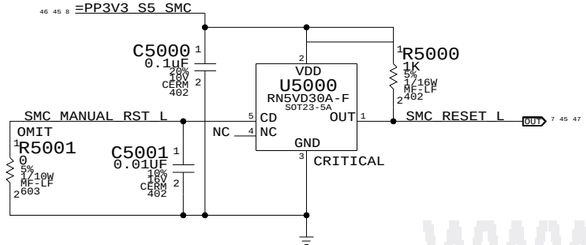
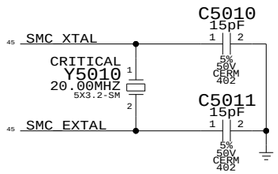
APPLE INC.	SIZE D	DRAWING NUMBER 051-7413	REV. 11.0.0
	SCALE NONE	SHT 45 OF 89	

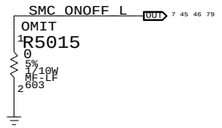
SMC Reset "Button" / Brownout Detect



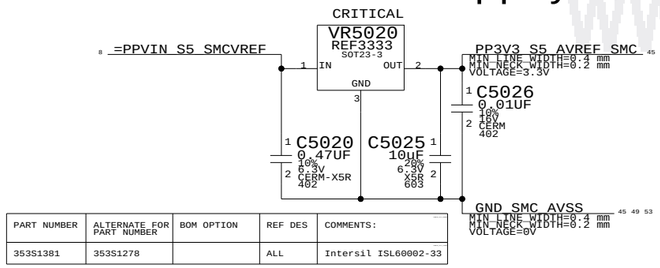
SMC Crystal Circuit



Debug Power "Button"

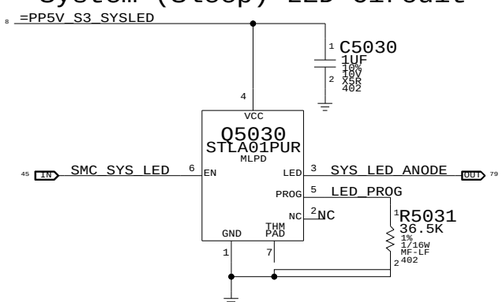


SMC AVREF Supply

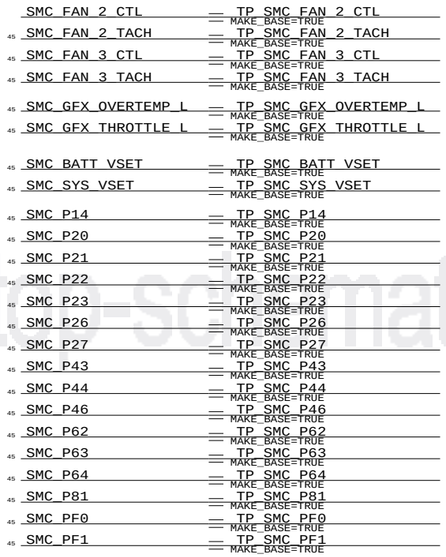


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		ALL	Intersil ISL60002-33

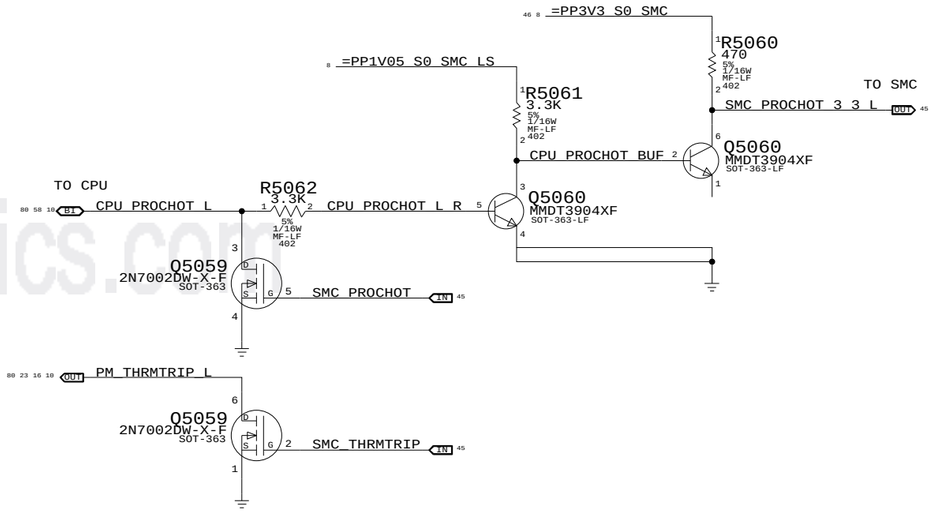
System (Sleep) LED Circuit



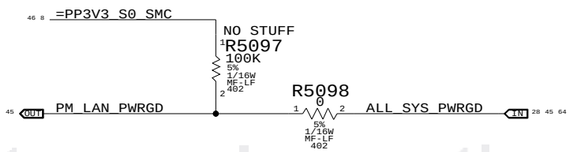
SMC_FAN_2_CTL … SMC_PF1



SMC FSB to 3.3V Level Shifting

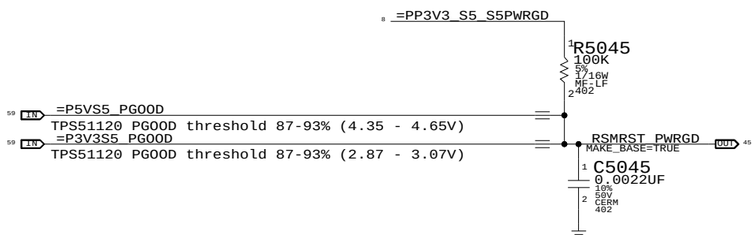


LAN PWRGD Circuit



S5 Rail PWRGD Circuit

Reports when 5V S5 and 3.3V S5 are in regulation

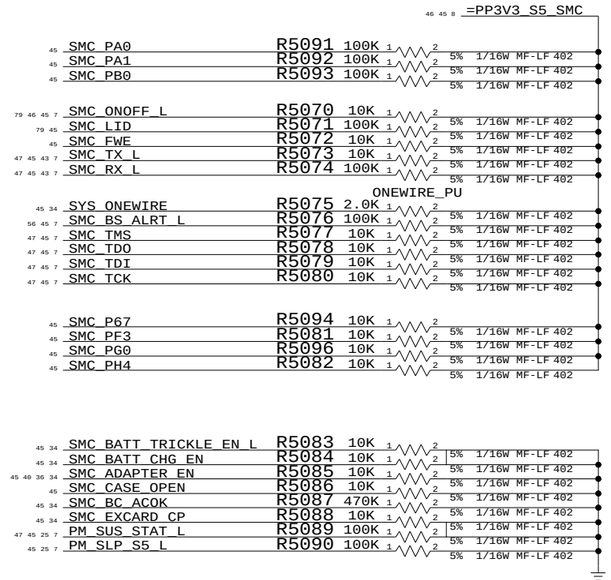


SMC_EXCARD_OC_L

SMC_SUS_CLK

SMC_P45

=PP3V3_S5_SMC



SMC Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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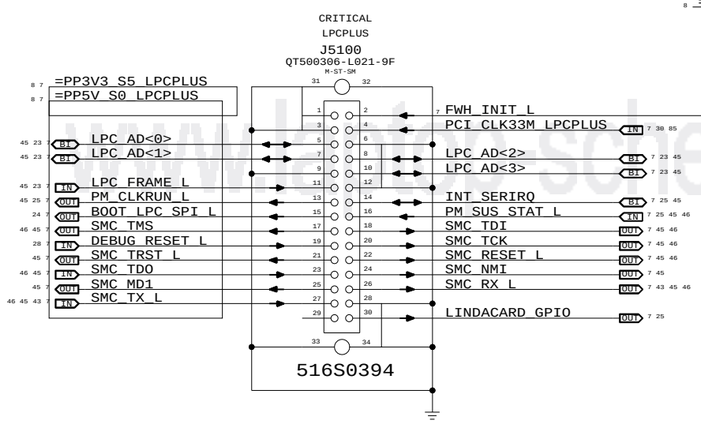
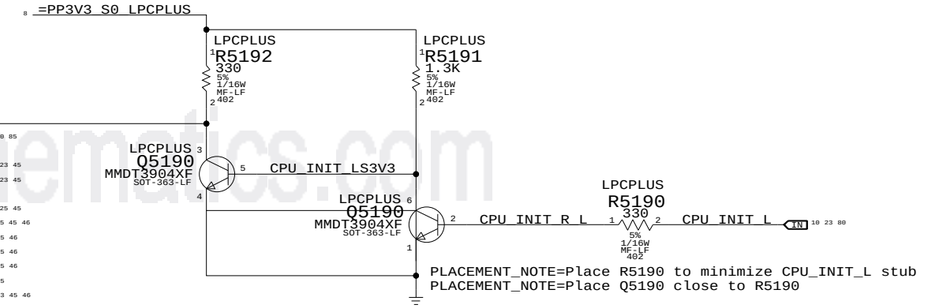
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 46 OF 89	

LPC+ Connector



FWH_INIT_L Generation



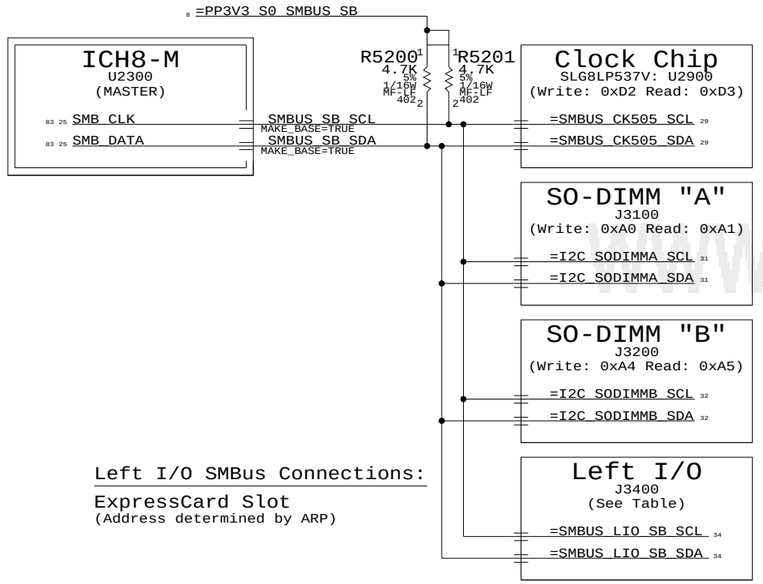
LPC+ Debug Connector

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

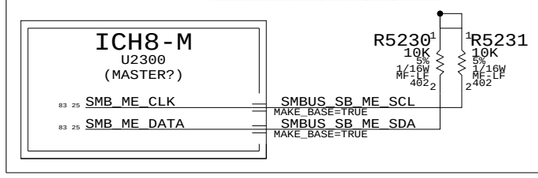
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 47 OF 89	

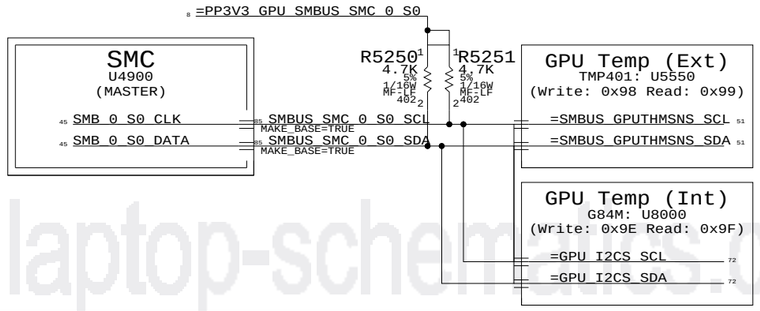
ICH8-M SMBus Connections



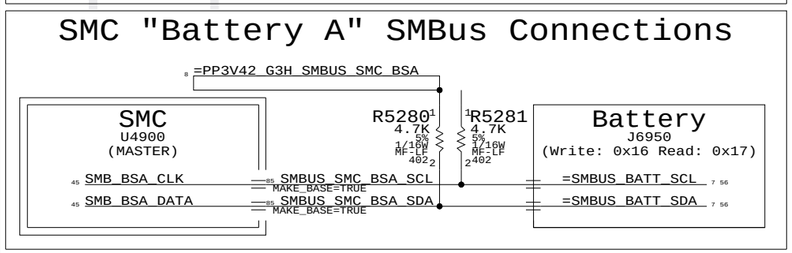
ICH8-M ME SMBus Connections



SMC "0" SMBus Connections

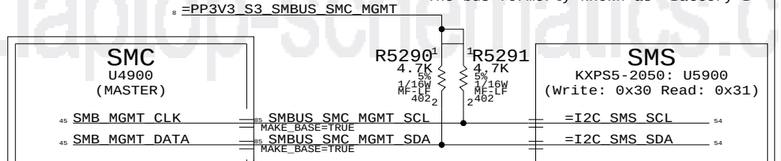


SMC "Battery A" SMBus Connections



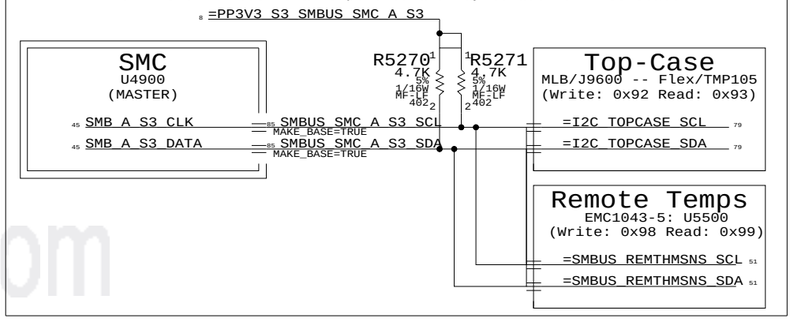
SMC "Management" SMBus Connections

The bus formerly known as "Battery B"

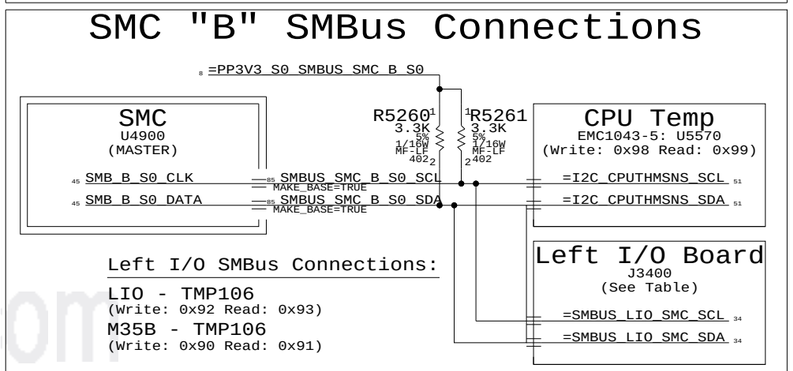


SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state



SMC "B" SMBus Connections



Left I/O SMBus Connections:

LIO - TMP106
(Write: 0x92 Read: 0x93)

M35B - TMP106
(Write: 0x90 Read: 0x91)

SMBus Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

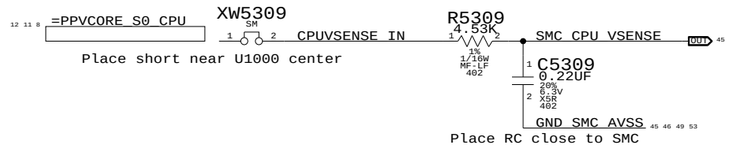
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0

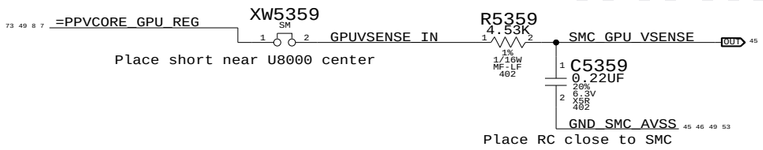
SCALE: NONE

SHT 48 OF 89

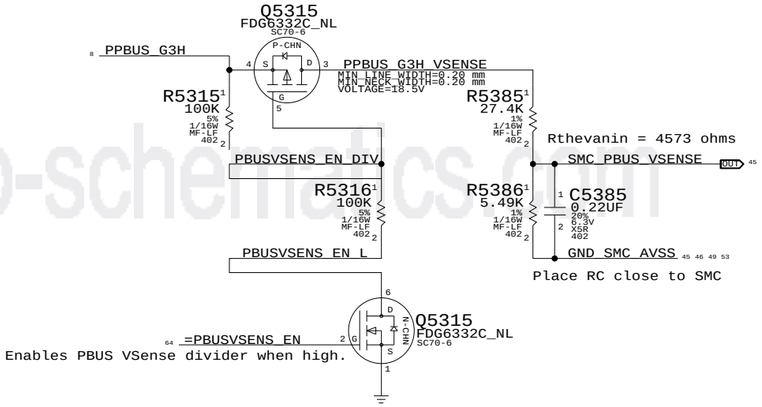
CPU Voltage Sense / Filter



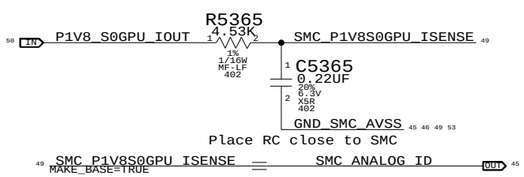
GPU Voltage Sense / Filter



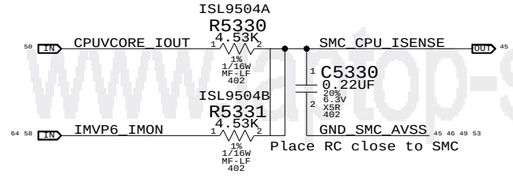
PBUS Voltage Sense & Filter



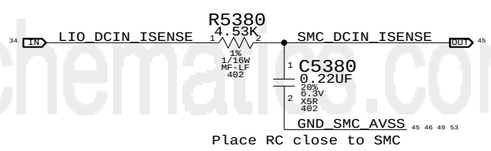
1.8V FB Current Sense Filter



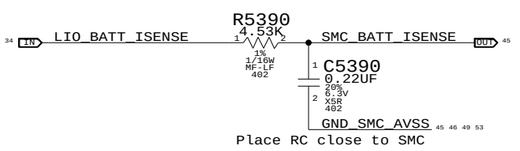
CPU Current Sense Filter



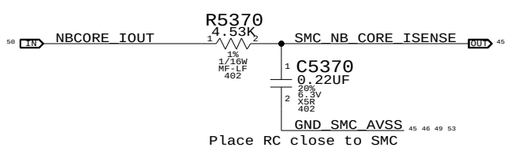
DCIN Current Sense Filter



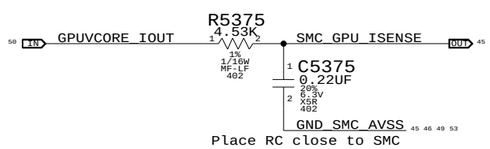
Battery (PBUS) Current Sense Filter



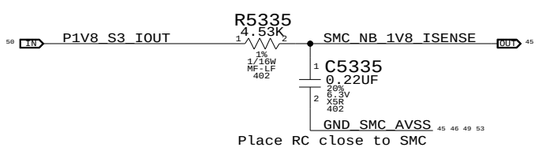
NB Core Current Sense Filter



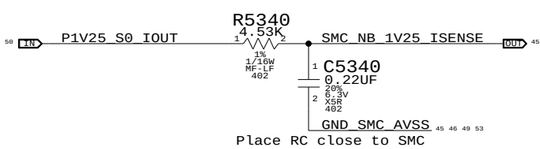
GPU Current Sense Filter



NB 1.8V Current Sense Filter

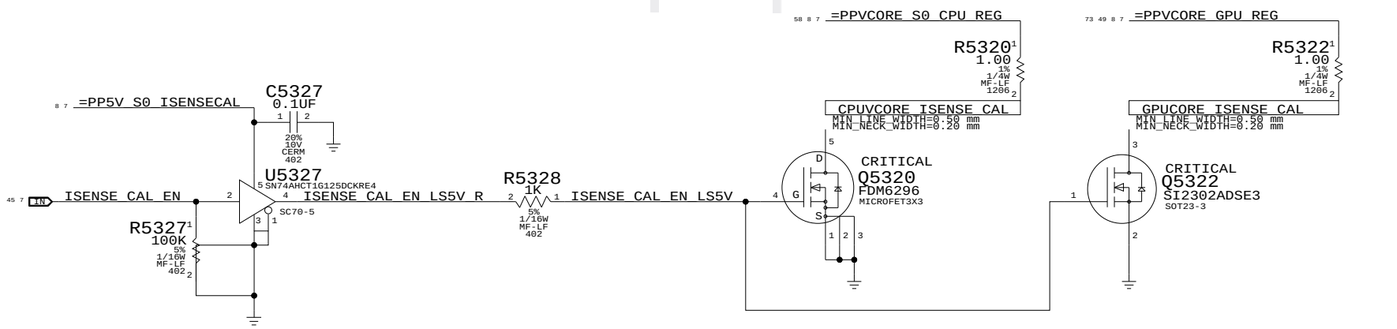


S0/GPU 1.25V Current Sense Filter



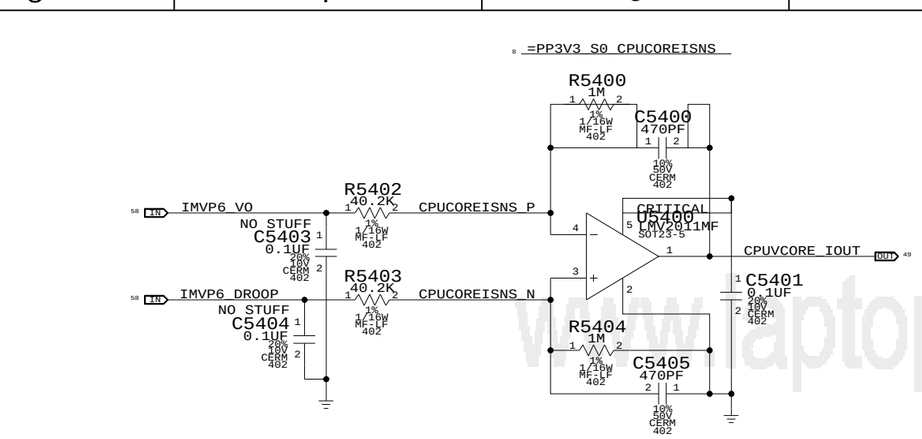
Current Sense Calibration Circuit

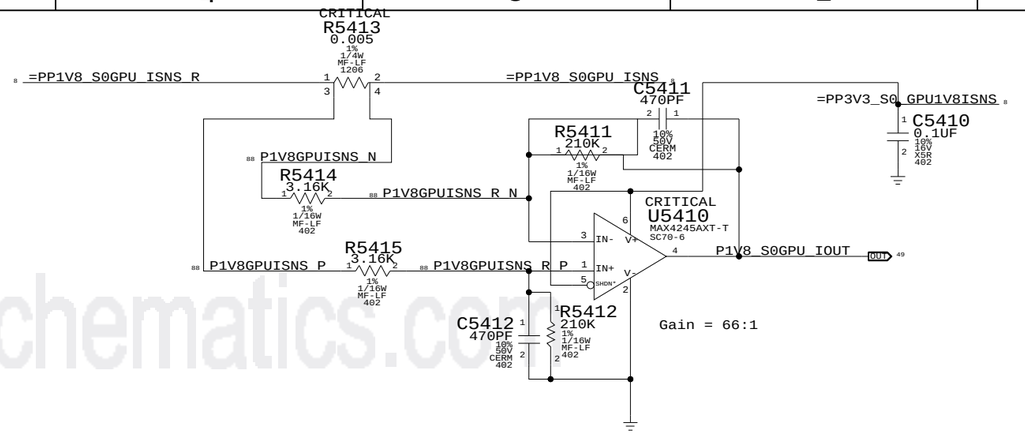
Switches in fixed load on power supplies to calibrate current sense circuits

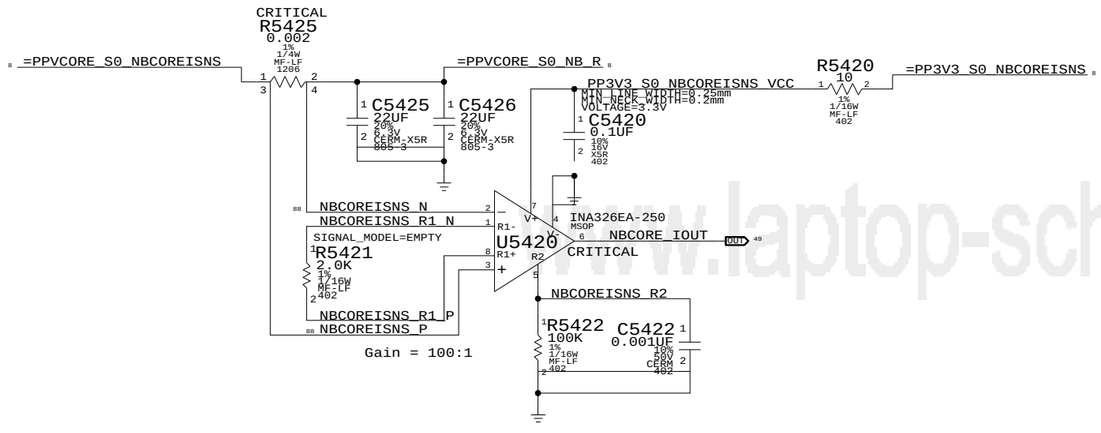


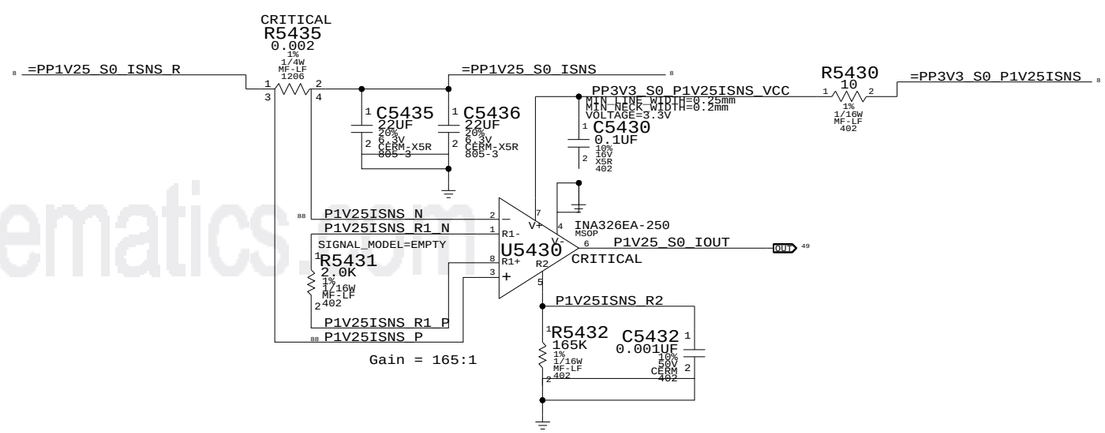
Current & Voltage Sensing		
SYNC_MASTER=M87_MLB	SYNC_DATE=05/22/2007	

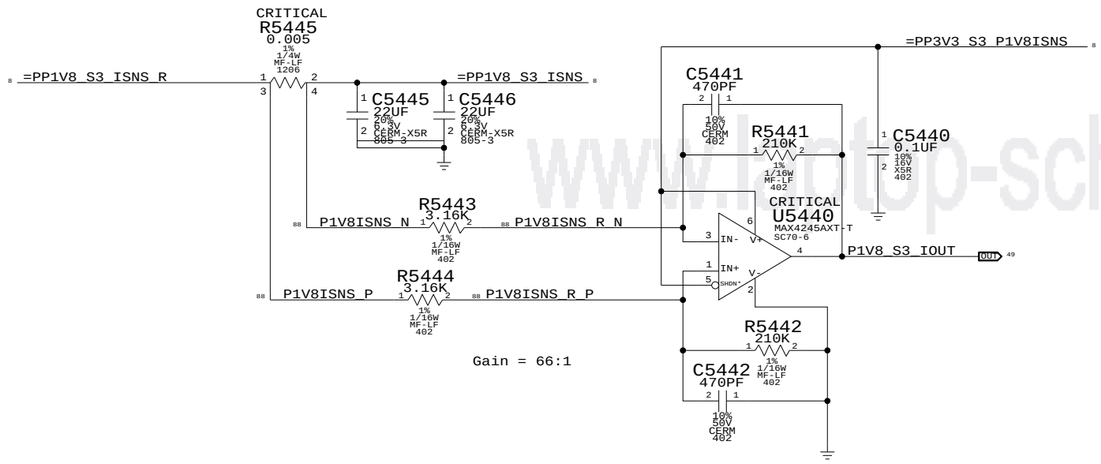
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	11.0.0
	SCALE: NONE	SHT 49 OF 89	

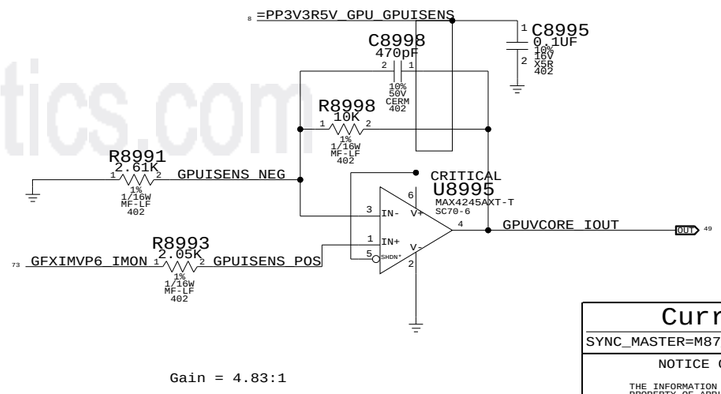












GPU VCore Current Sense

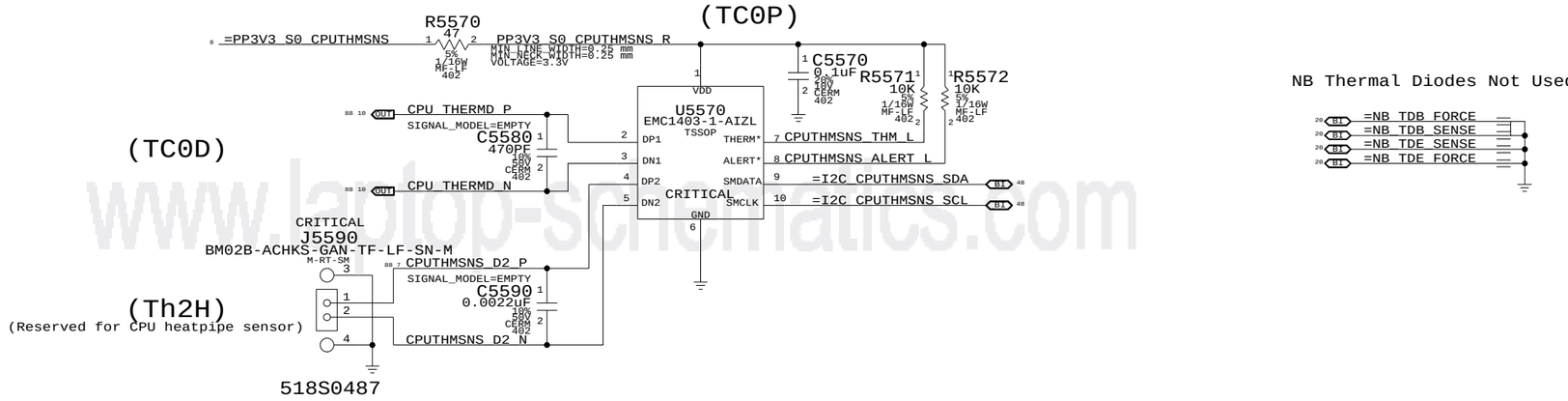
Current Sensing

SYNC_MASTER=M87_MLB SYNC_DATE=05/22/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 50 OF 89	

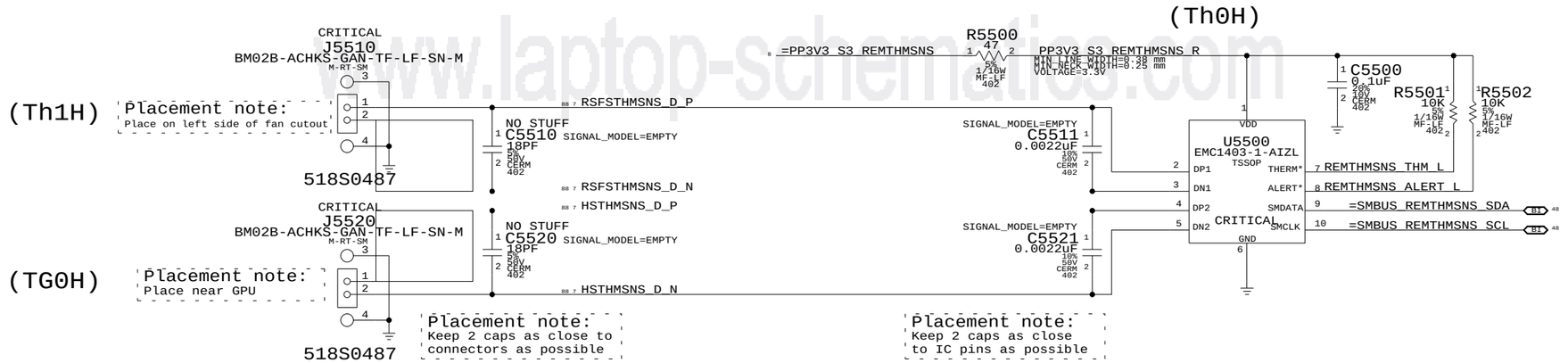
CPU T-Diode Thermal Sensor



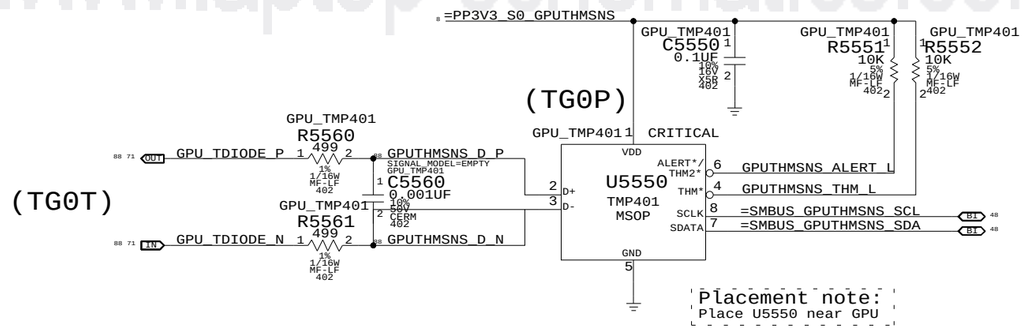
NB Thermal Diodes Not Used

=NB_TDB_FORCE
=NB_TDB_SENSE
=NB_TDE_SENSE
=NB_TDE_FORCE

GPU/Heat Pipe & Bottom Case Skin Thermal Sensor



GPU Die Thermal Sensor



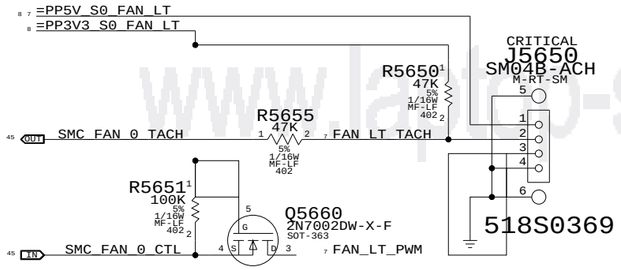
Thermal Sensors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

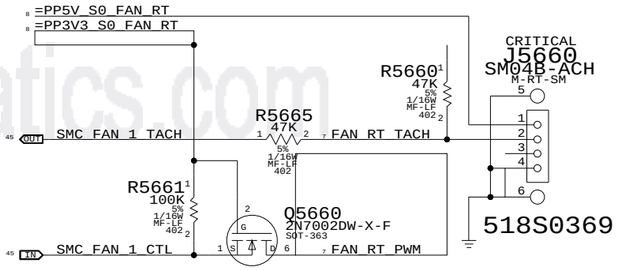
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 51 OF 89	

Left Fan



Right Fan



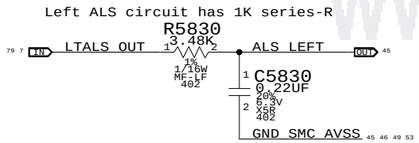
Fan Connectors

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

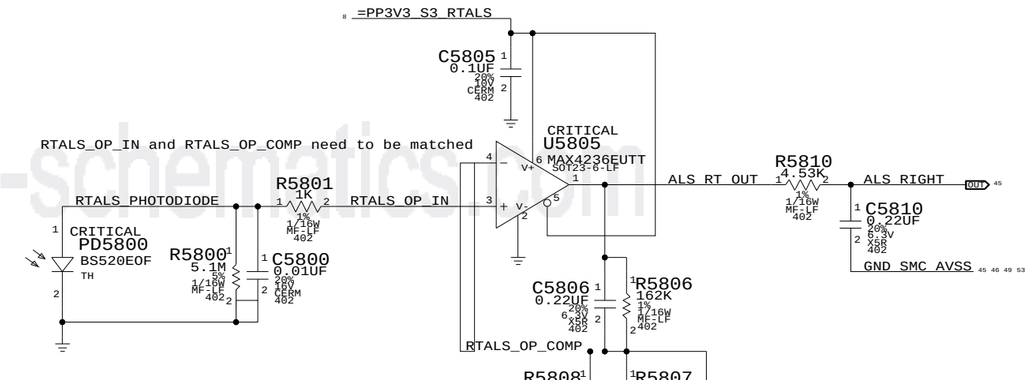
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 52 OF 89	

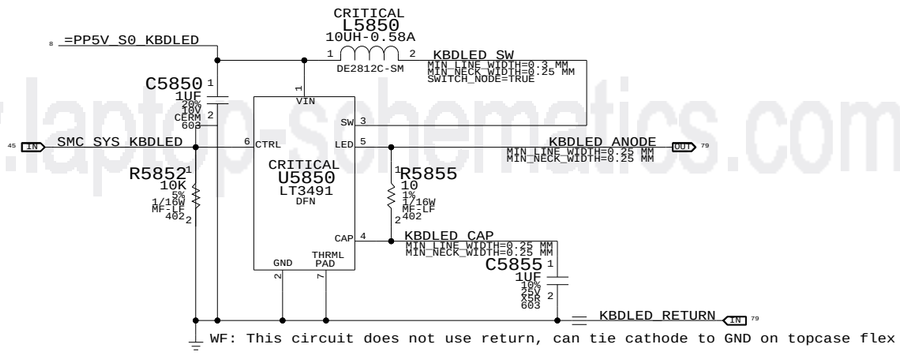
Left ALS Filter



Right ALS Circuit

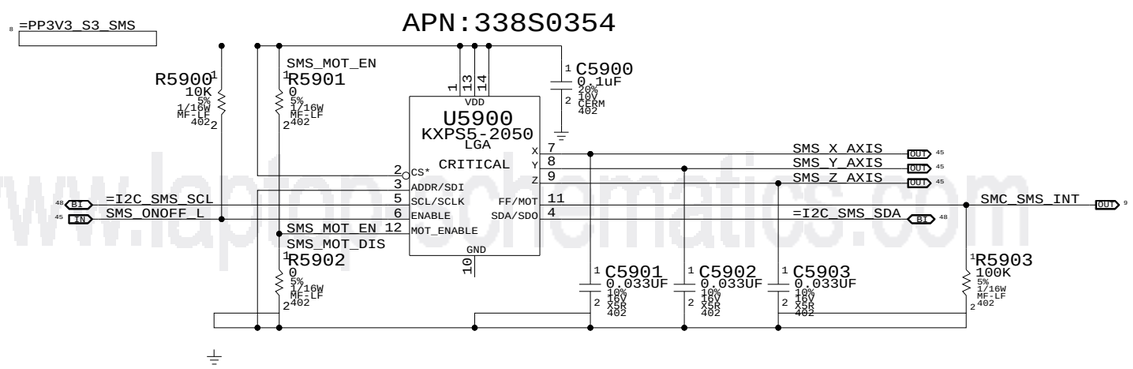


Keyboard LED Driver



ALS Support			
SYNC_MASTER=M76_MLB	SYNC_DATE=03/19/2007		
NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART			
APPLE INC.	SIZE: D	DRAWING NUMBER: 051-7413	REV: 11.0.0
	SCALE: NONE	SHT: 53 OF 89	

APN:338S0354

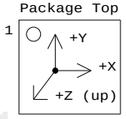


I2C addresses:

ADDR low => 0x30, 0x31
ADDR high => 0x32, 0x33
Alias SCL/SDA to GND if using analog outputs only

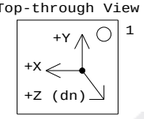
Desired orientation when placed on board top-side:

Package Top



Desired orientation when placed on board bottom-side:

Top-through View



Sudden Motion Sensor (SMS)

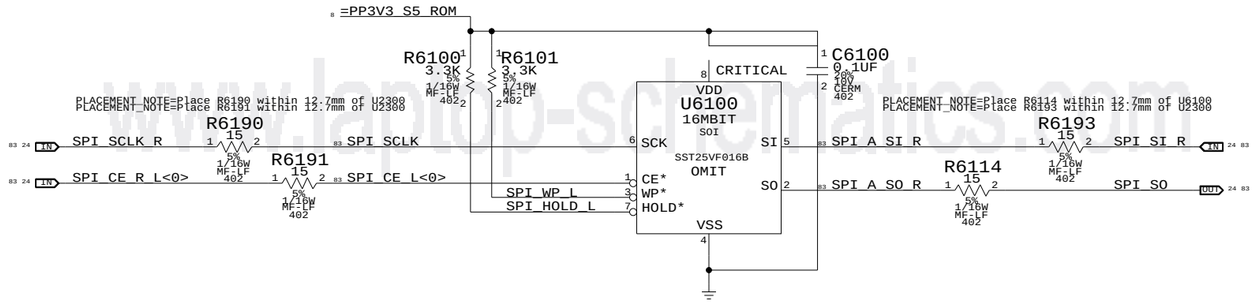
SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0

SCALE: NONE

SHT 54 OF 89



SPI BootROM

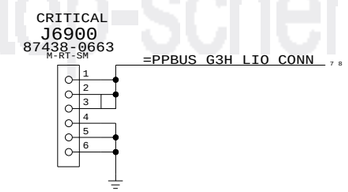
SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0

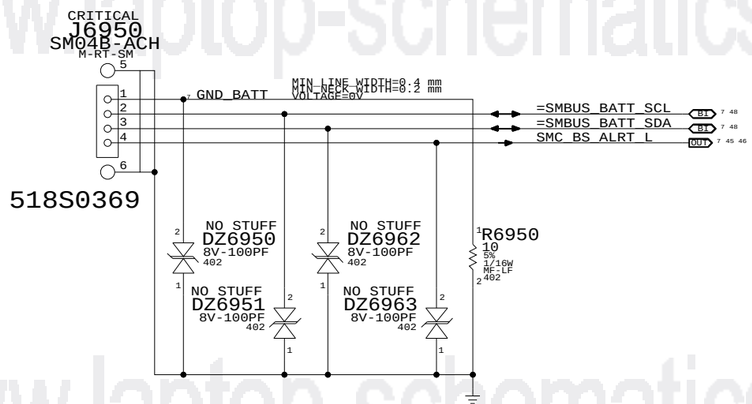
SCALE	SHT	OF
NONE	55	89

Left I/O Power Connector



518S0458

Battery Connector (Digital Signals)



518S0369

PBus-In & Battery Connectors

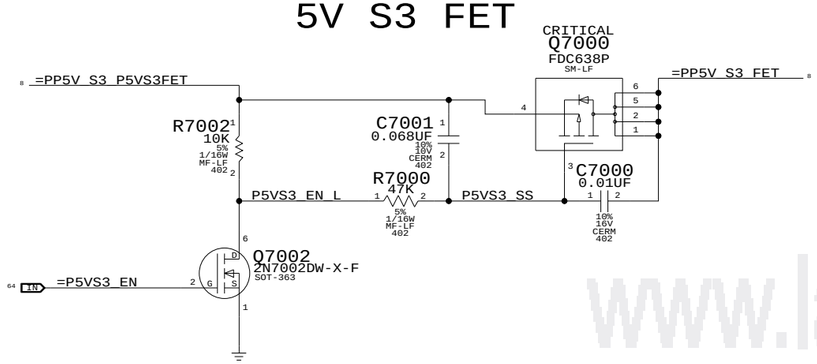
SYNC_MASTER=(M59_SYNC) SYNC_DATE=09/09/2006

APPLE INC.

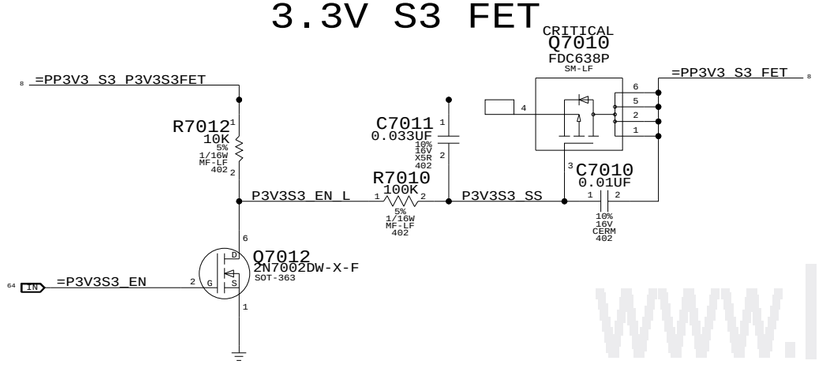
SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0

SCALE	SHT	OF
NONE	56	89

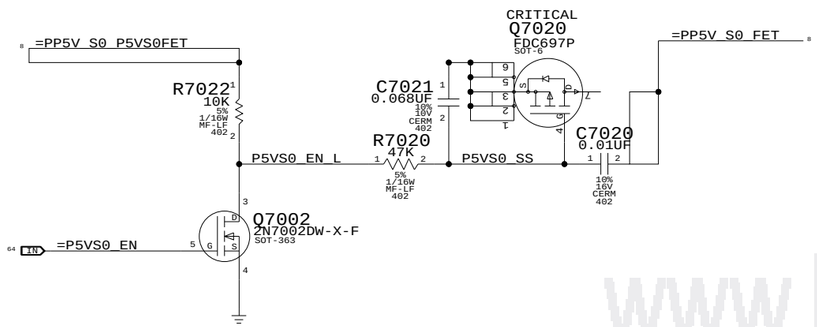
5V S3 FET



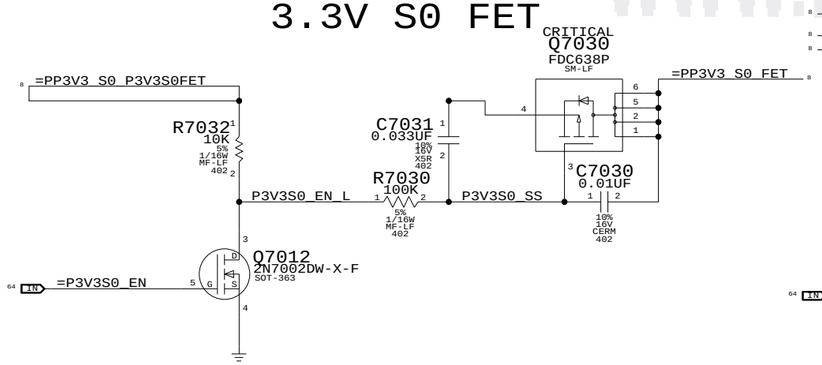
3.3V S3 FET



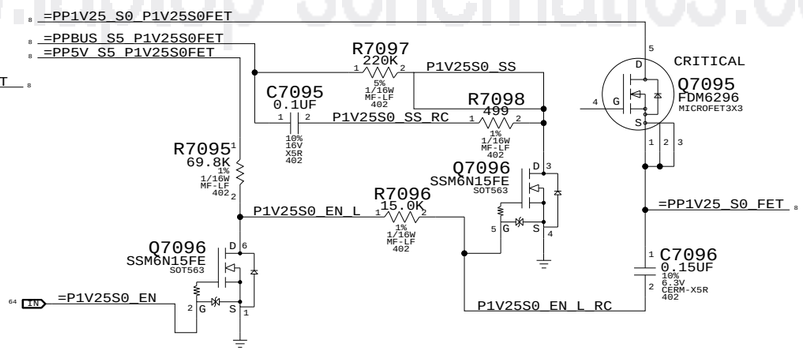
5V S0 FET



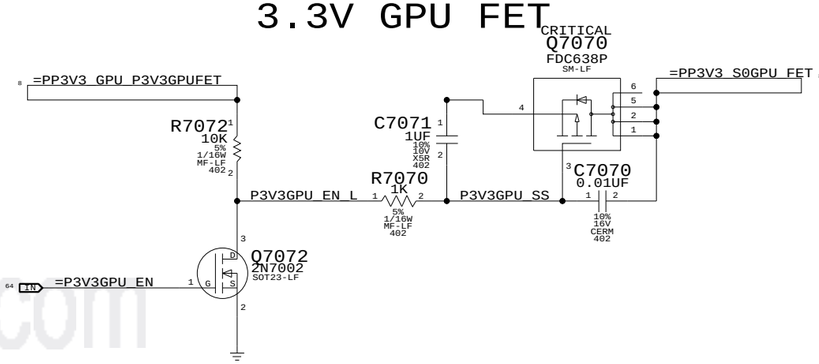
3.3V S0 FET



1.25V S0 FET



3.3V GPU FET



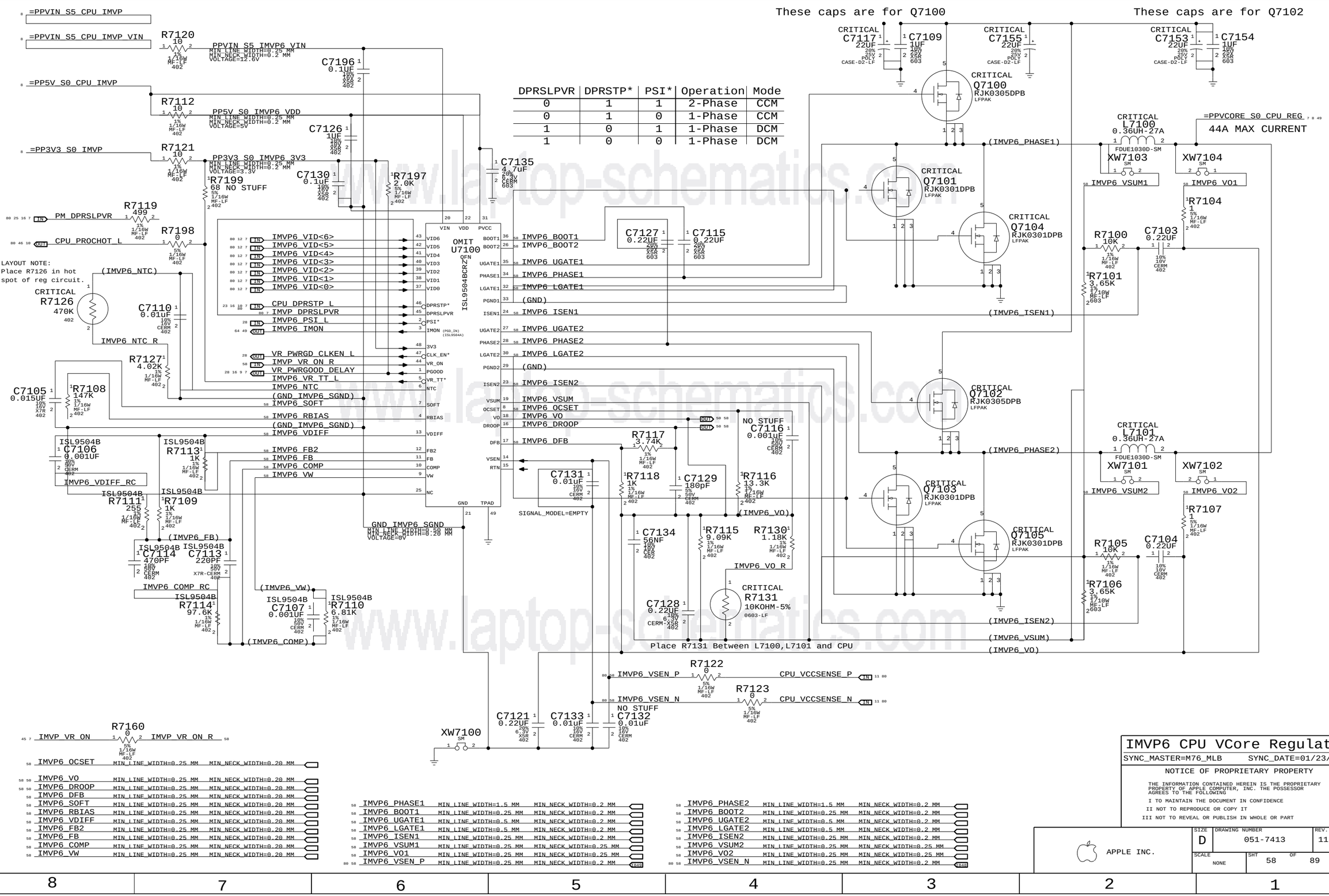
Power FETs

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

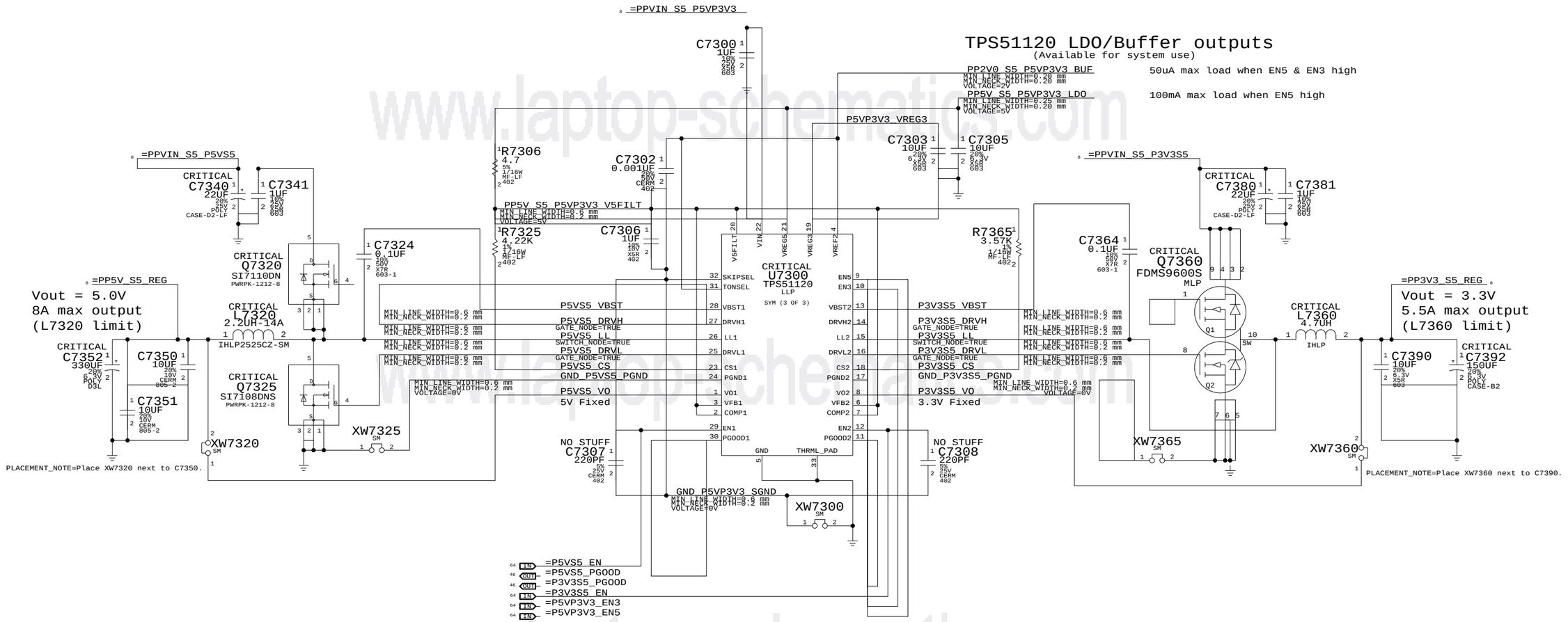
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0

SCALE	SHT	OF
NONE	57	89



DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM



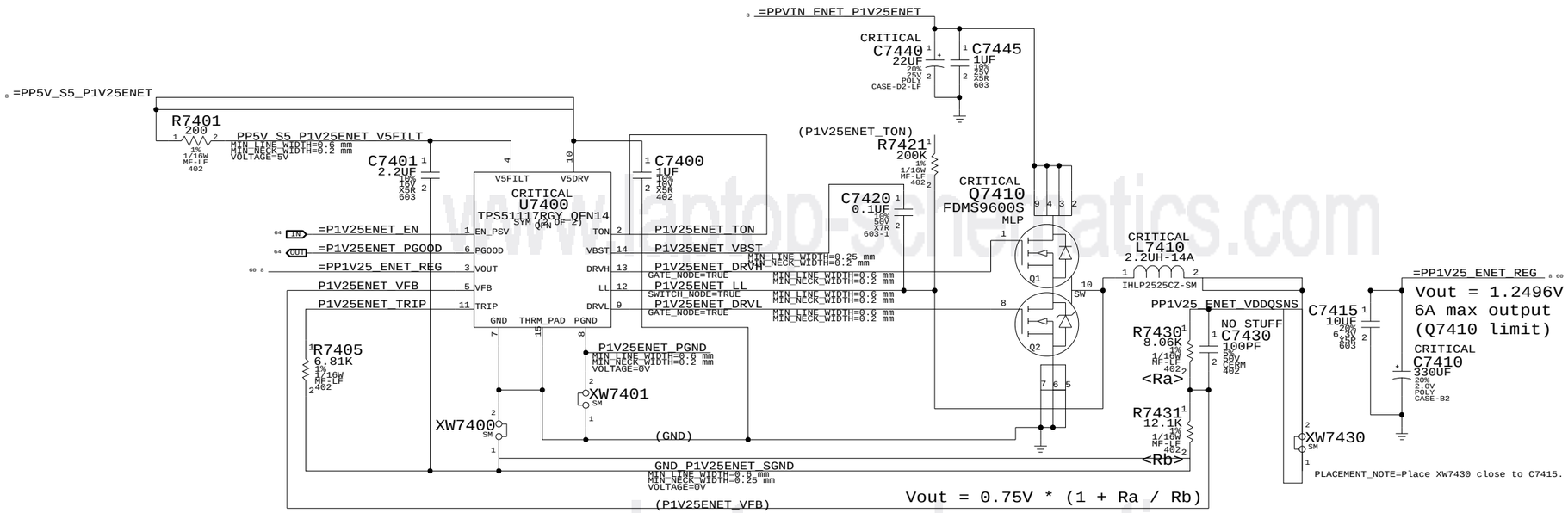
5V / 3.3V Power Supply

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0

SCALE: NONE SHT 59 OF 89

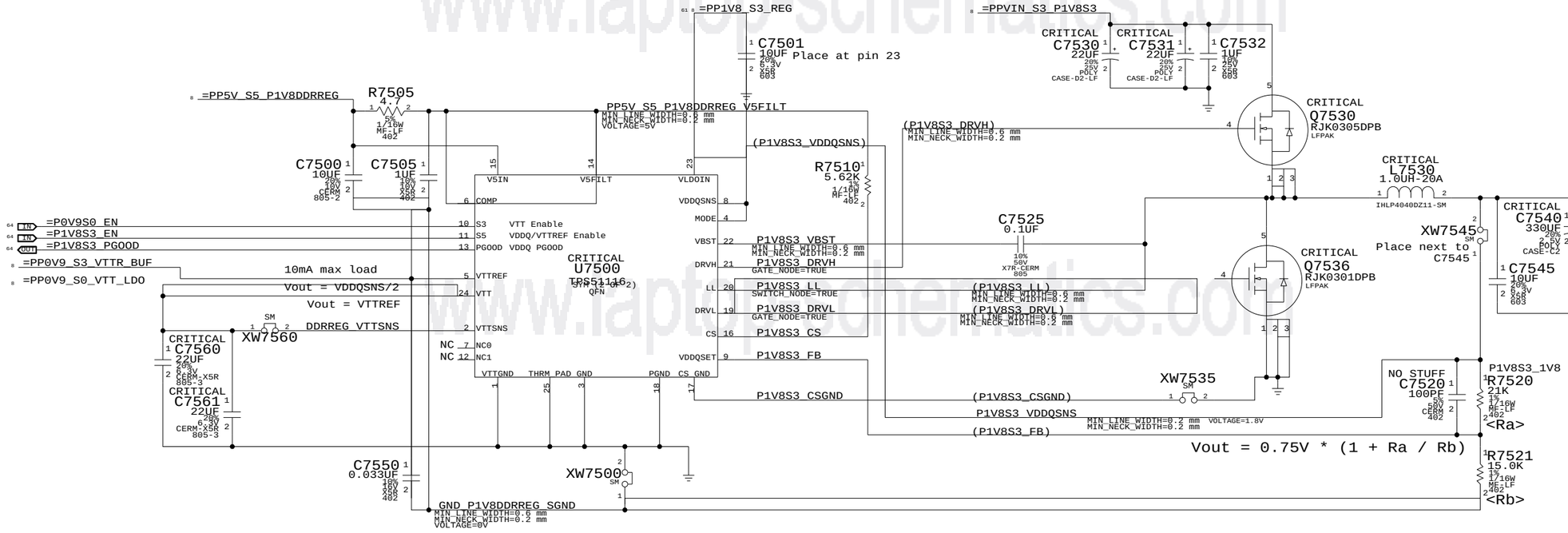


1.25V / 1.05V Power Supply

SYNC_MASTER=M76_MLB SYNC_DATE=03/12/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 60 OF 89	



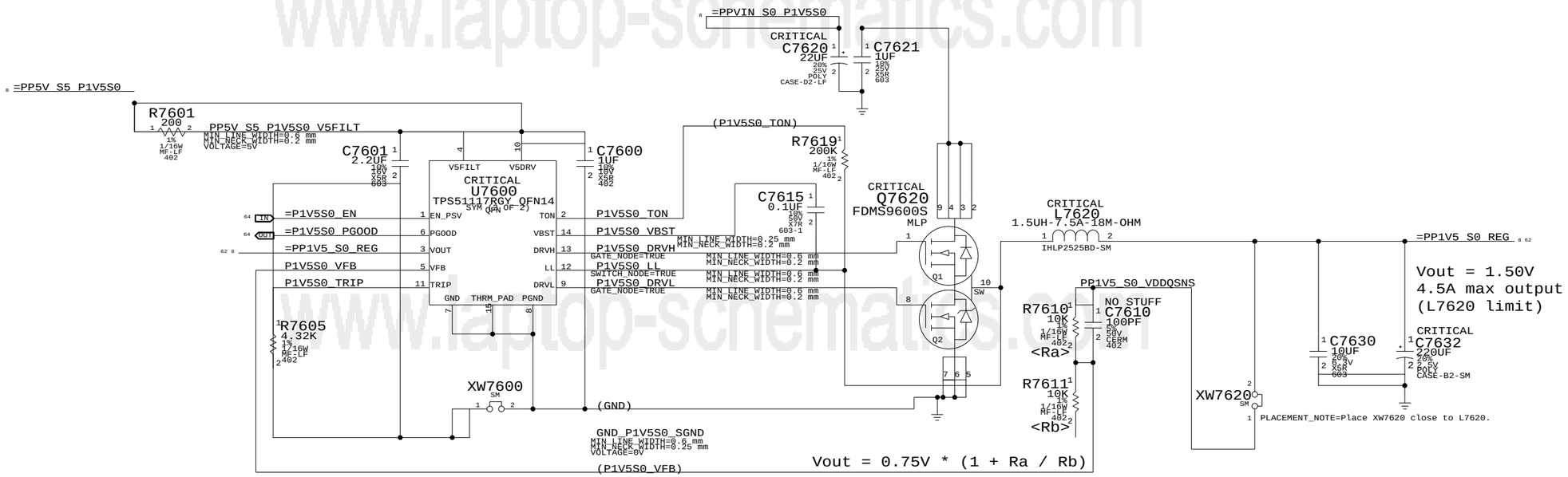
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0346	1	RES,MTL FILM,21.5K,1%,0402,SM,LF	R7520	CRITICAL	P1V8S3_1V825

1.8V DDR2 Supply

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 61 OF 89	



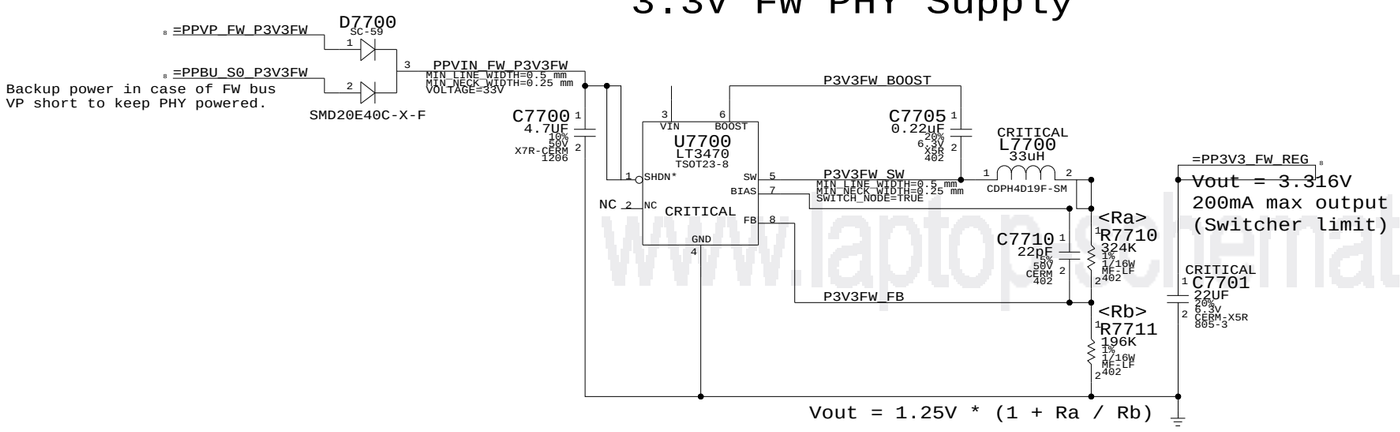
1.5V Power Supply

SYNC_MASTER=M76_MLB SYNC_DATE=03/12/2007

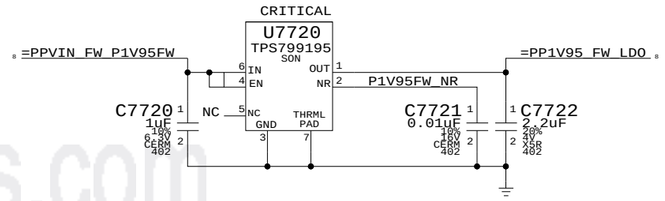
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 62 OF 89	

3.3V FW PHY Supply



1.95V FW PHY Supply



FW PHY Power Supplies

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 63 OF 89	

Power Control Signals

=PP5V_S5_PWRCTL

=PP3V3_GPU_PWRCTL

G84M GPU requires rails to come up in the following order:
1) 1.2V
2) 3.3V
3) Vcore
4) 1.8V

R7850 10K 5% 1/16W MF-LF 402
R7851 10K 5% 1/16W MF-LF 402
R7852 100K 5% 1/16W MF-LF 402
R7854 10K 5% 1/16W MF-LF 402

=GPUVCORE_PGOOD

Need to ensure that TPS51117 PGOOD does not deassert while GPU VIDs are changing GPU core voltage.

Q7850 2N7002DW-X-F SOT-363
Q7851 2N7002DW-X-F SOT-363
Q7851 2N7002DW-X-F SOT-363

PM_P1V8_S0GPU_EN MAKE_BASE=TRUE — =P1V8_S0GPU_EN
PM_GPUVCORE_EN MAKE_BASE=TRUE — =GPUVCORE_EN

C7851 0.1UF 20% 16V CERM 402

PVCOREGPU_EN_L

PM_SLP_S3_LS5V MAKE_BASE=TRUE — LIO_S0_EN_L

Q7850 2N7002DW-X-F SOT-363

PM_SLP_S3_L

R7856 100K 5% 1/16W MF-LF 402

(PM_SLP_S3_L) MAKE_BASE=TRUE
- =PVCOREGPU_EN
- =P5VS0_EN
- =P3V3S0_EN
- =P1V25S0_EN
- =P0V9S0_EN
- =PBUSVSENS_EN
- =ENET_VMAIN_AVLBL
- =PM_SLP_S3_DELAY_L

=PP3V3_S0_PWRCTL

=PP3V3_S5_PWRCTL

U7850 MC74VHC1G09 SC70

PM_SLP_S3_DELAY_L MAKE_BASE=TRUE

R7859 10K 5% 1/16W MF-LF 402

NO STUFF
C7859 0.047UF 10% 16V CERM 402

=P1V5S0_EN
=P1V05S0_EN

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

=PPVIN_G3H_P3V42G3H

P3V42G3H5_BOOST

C7800 10UF 10% 16V X5R 1206-1

U7800 LT3470 TSOT23-8
- VIN
- BOOST
- SHDN*
- SW
- BIAS
- NC
- NC CRITICAL
- FB
- GND

C7805 0.22UF 10% 6.3V X5R 402

CRITICAL
L7810 33UH CDPH4D19F-SM

P3V42G3H_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE

=PP3V42_G3H_REG

Vout = 3.425
200mA max output
(Switcher limit)

C7810 22PF 5% 50V CERM 402

<Ra> R7810 348K 1% 1/16W MF-LF 402

<Rb> R7811 200K 1% 1/16W MF-LF 402

C7815 22UF 20% 6.3V CERM-X5R 805-3

P3V42G3H_FB

Vout = 1.25V * (1 + Ra / Rb)

Unused PGOOD Signals

=P1V25ENET_PGOOD — TP_P1V25ENET_PGOOD MAKE_BASE=TRUE

=P1V8_S0GPU_PGOOD — TP_P1V8_S0GPU_PGOOD MAKE_BASE=TRUE

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

IMVP6_IMON — To CPU IMVP6

ISL9504A
R7866 0 5% 1/16W MF-LF 402

=PP3V3_S5_P1V5P1V05PG

R7865 100K 5% 1/16W MF-LF 402

=P1V5S0_PGOOD
TPS51117 PGOOD threshold 92.5-97.5% (1.36 - 1.46V)
=P1V05S0_PGOOD
TPS51117 PGOOD threshold 92.5-97.5% (0.98 - 1.02V)
=P1V8S3_PGOOD

P1V8P1V5P1V05S0_PGOOD MAKE_BASE=TRUE

=PP3V3_S0_ALLSYSPG

C7880 0.1UF 20% 16V CERM 402

U7880 MC74VHC1G08 SC70

ALL_SYS_PWRGD

PP1V25_S0_ISNS

=PP3V3_S3_PWRCTL

R7860 154K 1% 1/16W MF-LF 402

MAX6838 threshold is 93.5% @ 1.120V

U7860 MAX6838XSD0 SC70-4
- VCC
- RESET-IN
- RESET*
- GND

S0PGOOD_1V2_DIV

R7861 100K 1% 1/16W MF-LF 402

C7860 0.0047UF 10% 16V CERM 402

R7862 100K 5% 1/16W MF-LF 402

PM_P3V3GPU_EN MAKE_BASE=TRUE — =P3V3GPU_EN

=P1V25_PWRGD

PM_ENET_EN — (PM_ENET_EN) MAKE_BASE=TRUE — =P1V25ENET_EN

PM_S4_STATE_L — (PM_S4_STATE_L) MAKE_BASE=TRUE
- =P3V3S3_EN
- =P5VS3_EN
- =USB_EXTA_EN
- LIO_S3_EN

R7857 10K 5% 1/16W MF-LF 402

R7855 10K 5% 1/16W MF-LF 402

P1V8S3_EN MAKE_BASE=TRUE — =P1V8S3_EN

C7855 0.47UF 10% 6.3V CERM-X5R 402

NOTE: 0.9V is not checked!

Other S0 Rails PWRGD Circuit

PP3V3GPU_EN IS A PROXY FOR 1.2V

PP5V_S0
PP3V3_S0
PP1V8_S0GPU_ISNS
=P1V25_PWRGD

C7872 0.1UF 20% 10V CERM 402

C7871 0.1UF 20% 10V CERM 402

C7870 0.1UF 20% 10V CERM 402

R7875 10K 5% 1/16W MF-LF 402

U7870 LTC2900 DFN
- V1
- V2
- CRITICAL
- V3
- V4
- VREF
- VPG
- PBR*
- RST*
- CRT
- GND
- THRM_PAD
- NC

S0PGOOD_VREF

R7870 9.53K 1% 1/16W MF-LF 402

S0PGOOD_VPG

R7871 93.1K 1% 1/16W MF-LF 402

S0PGOOD_PWROK

S0PGOOD_CRT

C7875 0.047UF 10% 16V CERM 402

Trst = 4.6ms/nF
Trst = 216ms

LTC2900 typical threshold is 93.5% (4.675V, 3.086V, 1.685V,1.120V)

SMC_PM_G2_EN — PM_G2_EN MAKE_BASE=TRUE
- =P5VP3V3_EN5
- =P5VP3V3_EN3

=PP3V42_G3H_PWRCTL

C7858 0.1UF 20% 10V CERM 402

U7858 MC74VHC1G09 SC70

PM_G2_P5VS5_EN MAKE_BASE=TRUE — =P5VS5_EN

R7858 100K 5% 1/16W MF-LF 402

U7859 MC74VHC1G09 SC70

PM_G2_P3V3S5_EN MAKE_BASE=TRUE — =P3V3S5_EN

3.425V G3Hot Supply & Power Control

SYNC_MASTER=M88 SYNC_DATE=08/02/2007

APPLE INC.

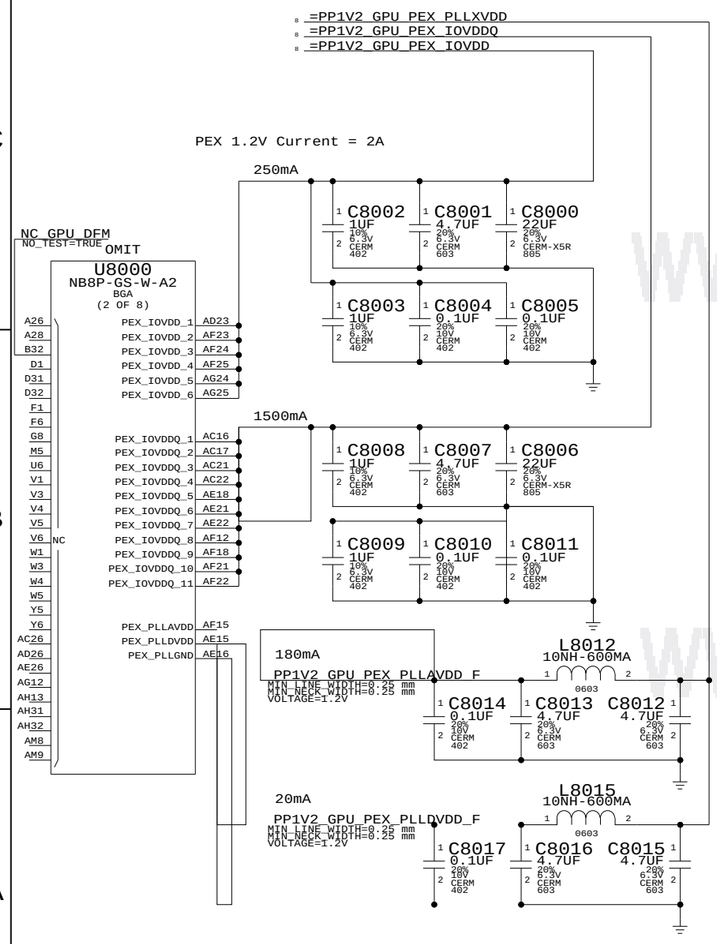
SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 64 OF 89	

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



OMIT
U8000
NB8P-GS-W-A2
BGA
(1 OF 8)

PCI-EXPRESS BUS INTERFACE

PEG_R2D_C_P<0>	C8020 0.1uF	PEG_R2D_P<0>	AK13 PEX_RX0	PEX_TX0 AJ15	PEG_D2R_C_P<0>	C8055 0.1uF	PEG_D2R_P<0>
PEG_R2D_C_N<0>	C8021 0.1uF	PEG_R2D_N<0>	AK14 PEX_RX0_L	PEX_TX0_L AK15	PEG_D2R_C_N<0>	C8056 0.1uF	PEG_D2R_N<0>
PEG_R2D_C_P<1>	C8022 0.1uF	PEG_R2D_P<1>	AM14 PEX_RX1	PEX_TX1 AH16	PEG_D2R_C_P<1>	C8057 0.1uF	PEG_D2R_P<1>
PEG_R2D_C_N<1>	C8023 0.1uF	PEG_R2D_N<1>	AM15 PEX_RX1_L	PEX_TX1_L AG16	PEG_D2R_C_N<1>	C8058 0.1uF	PEG_D2R_N<1>
PEG_R2D_C_P<2>	C8024 0.1uF	PEG_R2D_P<2>	AL15 PEX_RX2	PEX_TX2 AG17	PEG_D2R_C_P<2>	C8059 0.1uF	PEG_D2R_P<2>
PEG_R2D_C_N<2>	C8025 0.1uF	PEG_R2D_N<2>	AL16 PEX_RX2_L	PEX_TX2_L AH17	PEG_D2R_C_N<2>	C8060 0.1uF	PEG_D2R_N<2>
PEG_R2D_C_P<3>	C8026 0.1uF	PEG_R2D_P<3>	AK16 PEX_RX3	PEX_TX3 AG18	PEG_D2R_C_P<3>	C8061 0.1uF	PEG_D2R_P<3>
PEG_R2D_C_N<3>	C8027 0.1uF	PEG_R2D_N<3>	AK17 PEX_RX3_L	PEX_TX3_L AH18	PEG_D2R_C_N<3>	C8062 0.1uF	PEG_D2R_N<3>
PEG_R2D_C_P<4>	C8028 0.1uF	PEG_R2D_P<4>	AL17 PEX_RX4	PEX_TX4 AK18	PEG_D2R_C_P<4>	C8063 0.1uF	PEG_D2R_P<4>
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PEG_R2D_C_P<5>	C8030 0.1uF	PEG_R2D_P<5>	AM18 PEX_RX5	PEX_TX5 AJ19	PEG_D2R_C_P<5>	C8065 0.1uF	PEG_D2R_P<5>
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PEG_R2D_C_N<15>	C8051 0.1uF	PEG_R2D_N<15>	AL29 PEX_RX15_L	PEX_TX15_L AH27	PEG_D2R_C_N<15>	C8086 0.1uF	PEG_D2R_N<15>

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PEG_CLK100M_GPU_N	AJ14 PEX_REFCLK_L	PEX_TSTCLK_OUT_L AM11 TP_GPU_PEXTSTCLK_N
GPU_RESET_L	AH15 PEX_RST_L	

NV G84M PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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D	051-7413	11.0.0
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Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

=PPVCORE_GPU

???A @ ???/???MHz Core/Mem Clk for VDD

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C8101 1UF 20% 6.3V CERM 402
C8102 1UF 20% 6.3V CERM 402
C8103 0.1UF 20% 10V CERM 402
C8104 0.1UF 20% 10V CERM 402
C8105 0.1UF 20% 10V CERM 402
C8106 0.1UF 20% 10V CERM 402
C8107 0.1UF 20% 10V CERM 402
C8108 0.1UF 20% 10V CERM 402
C8109 0.1UF 20% 10V CERM 402
C8110 0.1UF 20% 10V CERM 402
C8111 0.1UF 20% 10V CERM 402
C8112 0.1UF 20% 10V CERM 402
C8113 0.1UF 20% 10V CERM 402
C8114 0.1UF 20% 10V CERM 402
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C8117 0.1UF 20% 10V CERM 402
C8118 0.1UF 20% 10V CERM 402
C8119 0.1UF 20% 10V CERM 402
C8120 0.1UF 20% 10V CERM 402
C8121 0.1UF 20% 10V CERM 402
C8122 0.1UF 20% 10V CERM 402

OMIT
U8000
NB8P-GS-W-A2
BGA
(7 OF 8)

K16 K17 N13 N14 N16 N17 N19 R13 P14 R16 P17 P19 R16 R17 T13 T14 T15 T18 T19 U13 U14 U15 U18 U19 V16 V17 W13 W14 W16 W17 W19 Y13 Y14 Y16 V17 Y19 Y20 → VDD

P20 T20 T23 U20 U23 W20 → VDD_LP

A12 A18 A21 A24 A27 A3 A30 A6 A9 AA32 AD32 AG32 AK32 C32 F32 J32 M32 R32 → FBVDD

AA25 AA26 AB25 AB26 G11 G12 G15 G18 G21 G22 H11 H12 H15 H18 H21 H22 L25 L26 M25 M26 R25 R26 V25 V26 → FBVDDQ

AA23 AB23 H16 H17 J10 J23 J24 J9 K11 K12 K21 K22 K24 K9 L23 M23 T25 U25 → NC

FBVTT

TP_GPU_VDD_SENSE N20 → VDD_SENSE
TP_GPU_GND_SENSE M21 → GND_SENSE

=PP1V8_GPU_FBVDDQ

???A @ ???MHz 1.8V GDDR3

C8150 4.7UF 20% 6.3V CERM 603
C8151 4.7UF 20% 6.3V CERM 603
C8156 0.1UF 20% 10V CERM 402
C8157 0.1UF 20% 10V CERM 402
C8158 0.1UF 20% 10V CERM 402
C8159 0.1UF 20% 10V CERM 402
C8160 0.47UF 10% 6.3V CERM-X5R 402
C8161 0.47UF 10% 6.3V CERM-X5R 402
C8162 0.1UF 20% 10V CERM 402
C8163 0.1UF 20% 10V CERM 402
C8164 0.1UF 20% 10V CERM 402
C8165 0.1UF 20% 10V CERM 402
C8166 0.47UF 10% 6.3V CERM-X5R 402
C8167 0.47UF 10% 6.3V CERM-X5R 402
C8168 0.47UF 10% 6.3V CERM-X5R 402
C8169 0.47UF 10% 6.3V CERM-X5R 402
C8170 0.47UF 10% 6.3V CERM-X5R 402
C8171 0.47UF 10% 6.3V CERM-X5R 402

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AE17 AE27 AE6 AF11 AF26 AF29 AF4 AF7 AG10 AG11 AB27 AB6 AD10 AC23 AD29 AC4 AD16 AD17 AD2 AD31 AA12 AA2 AA21 AA31 AG13 AG14 AG15 AG19 AG2 AG22 AD31 AG8 AH24 AJ10 AJ13 AJ16 AJ17 AJ20 AJ23 AJ26 AJ29 AJ4 AJ7 AK2 AK28 AK31 AL10 AL11 AL14 AL19 AL22 AL25 AL3 AL6 AL9 AM10 AM13 AM16 AM17 AM20 AM23 AM26 AM29 B12 B15 B18 B21 B24 B27 B3 B30 B6 B9 C2 C31 D10 D13 → GND

D16 D17 D20 D23 D26 D29 D4 D7 F11 F14 F19 F2 F22 F25 F31 F8 G26 G29 G4 G7 H27 H6 J16 J17 J2 J31 K19 K23 K29 K4 L27 L6 M12 M2 M31 N15 N18 N29 N4 P15 P18 P27 P6 R13 R14 R15 R18 R19 R2 R20 R31 T16 T17 T24 T29 T4 U16 U17 U24 U29 U8 V13 V14 V15 V18 V19 V2 V20 V31 W15 W18 W27 W6 Y15 Y18 Y29 Y4 → GND

NV G84M Core/FB Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

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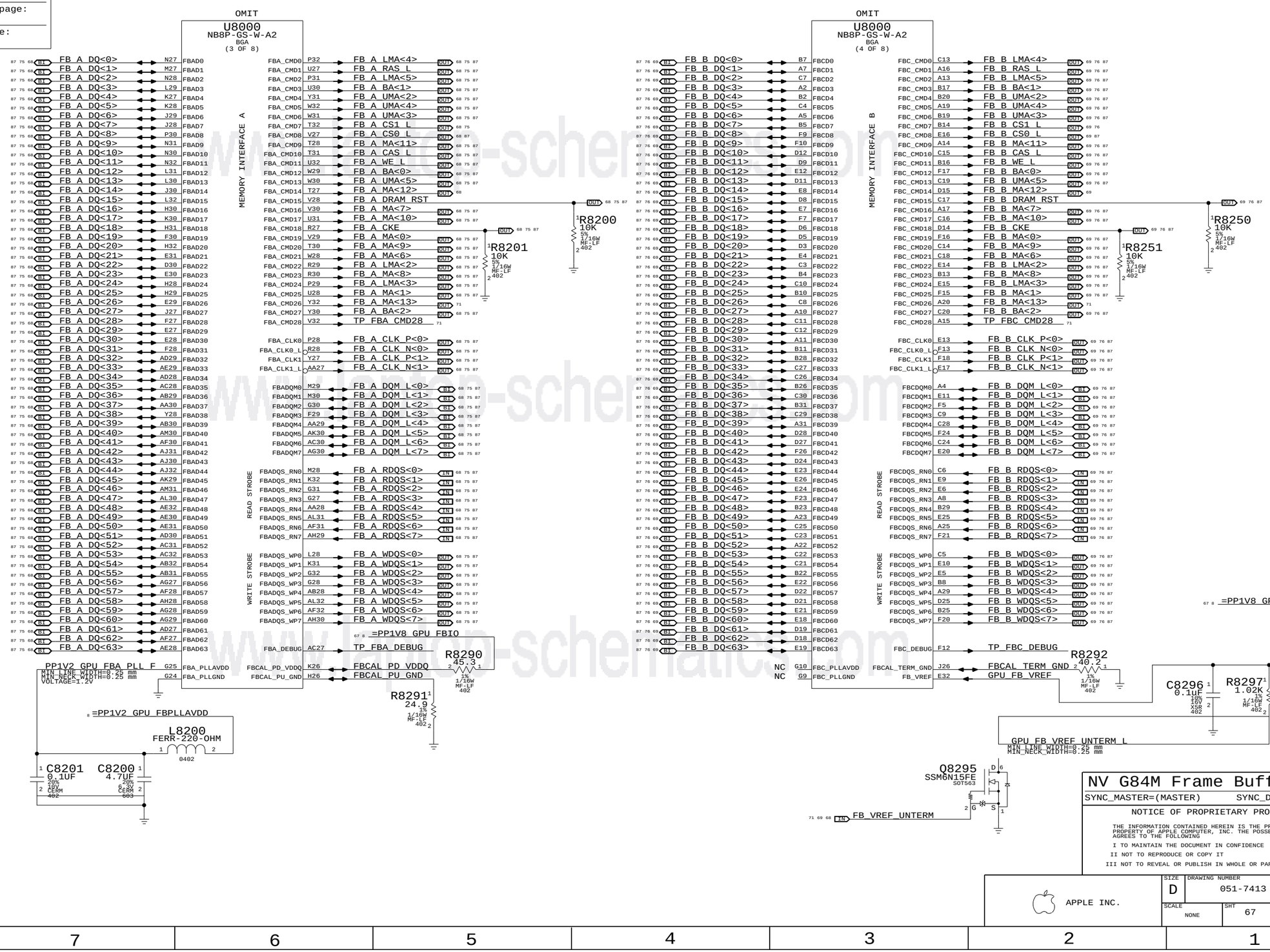
Page Notes

Power aliases required by this page:
- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G84M Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 67 OF 89	

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

=PP1V8_GPU_FB_VDD

=PP1V8_GPU_FB_VDDQ

CRITICAL OMIT

U8400 FBGA (2 OF 2) 16MX32-GDDR3-500MHZ K4J52324QC-BC20

U8450 FBGA (2 OF 2) 16MX32-GDDR3-500MHZ K4J52324QC-BC20

Connect to designated pin, then GND

C8400 C8401 C8402 C8403 C8404 C8410 C8415 C8420 C8421 C8422 C8423 C8424 C8425 C8426 C8430 C8431 C8432 C8433 C8434 C8435 C8440 C8442 C8444 C8446 C8447 C8448 C8449

C8450 C8451 C8452 C8453 C8454 C8460 C8465 C8470 C8471 C8472 C8473 C8474 C8475 C8476 C8480 C8481 C8482 C8483 C8484 C8485 C8490 C8492 C8494 C8496 C8497 C8498 C8499

R8443 R8445 R8493 R8495

Q8400 SSM6N15FE SOT563

Q8450 SSM6N15FE SOT563

FB_A_CLK0_TERM VOLTAGE=0.9V

FB_A_CLK1_TERM VOLTAGE=0.9V

FB_VREF_UNTERM

FB_A0_VREF

FB_A2_VREF

FB_A1_VREF

FB_A3_VREF

FB_A2_VREF_UNTERM_L
FB_A0_VREF_UNTERM_L

FB_A3_VREF_UNTERM_L
FB_A1_VREF_UNTERM_L

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FB_A0_MF
FB_A0_SEN

FB_A1_ZQ
FB_A1_MF
FB_A1_SEN

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(For 32Mx32 support)

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(For 32Mx32 support)

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GDDR3 Frame Buffer A (Top)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
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Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

=PP1V8_GPU_FB_VDD

=PP1V8_GPU_FB_VDDQ

CRITICAL
OMIT

U8500
FBGA
(2 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

U8550
FBGA
(2 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

Connect to designated pin, then GND

C8500 C8501 C8502 C8503 C8504 C8510 C8515
C8520 C8521 C8522 C8523 C8524 C8525 C8526
C8550 C8551 C8552 C8553 C8554 C8560 C8565
C8570 C8571 C8572 C8573 C8574 C8575 C8576
0.1uF

R8530 R8533 R8531 R8532 R8534 R8535
R8580 R8583 R8581 R8582 R8584 R8585
C8531 C8532 C8581 C8582
0.01uF

FB_B0_VREF
FB_B2_VREF
FB_B1_VREF
FB_B3_VREF

FB_B2_VREF_UNTERM_L
FB_B0_VREF_UNTERM_L
FB_B3_VREF_UNTERM_L
FB_B1_VREF_UNTERM_L

FB_B_CLK0_TERM
FB_B_CLK1_TERM
VOLTAGE=0.9V
C8546 C8596
0.01UF

FB_VREF_UNTERM

Q8500 SSM6N15FE SOT563
Q8550 SSM6N15FE SOT563

R8540 R8542 R8544 R8546 R8543 R8545 R8547
R8590 R8592 R8594 R8596 R8593 R8595 R8597
121

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FB_B_MA<10>
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FB_B_RAS_L
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FB_B_RDQS<3>
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FB_B_CS1_L
(For 32Mx32 support)

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FB_B_CS1_L
(For 32Mx32 support)

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FB_B_DQ<34>
FB_B_DQ<32>
FB_B_DQ<35>
FB_B_DQ<33>
FB_B_DQ<63>
FB_B_DQ<58>
FB_B_DQ<61>
FB_B_DQ<59>
FB_B_DQ<62>
FB_B_DQ<56>
FB_B_DQ<60>
FB_B_DQ<57>

FB_B0_ZQ
FB_B0_MF
FB_B0_SEN
FB_B1_ZQ
FB_B1_MF
FB_B1_SEN

R8548 R8549 R8598 R8599
243 100

VRAM4

MFHIGH

GDDR3 Frame Buffer B (Top)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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Page Notes

Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP3V3_GPI_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

OMIT
U8000
NB8P-GS-W-A2
BGA
(6 OF 8)

=PP3V3_GPU_VDD33
Typically <??mA
C8600 0.47UF 10% 6.3V CERM-X5R 402
C8601 0.47UF 10% 6.3V CERM-X5R 402
C8602 0.47UF 10% 6.3V CERM-X5R 402

AC11 VDD33_1
AC12 VDD33_2
AC24 VDD33_3
AD24 VDD33_4
AE11 VDD33_5
AE12 VDD33_6
H7 VDD33_7
J7 VDD33_8
K7 VDD33_9
L10 VDD33_10
L7 VDD33_11
L8 VDD33_12
M10 VDD33_13

GPIO0 K3 GPU_GPIO_0
GPIO1 H1 GPU_GPIO_1
GPIO2 K5 GPU_GPIO_2
GPIO3 G5 GPU_GPIO_3
GPIO4 E2 GPU_GPIO_4
GPIO5 J5 GPU_GPIO_5
GPIO6 G6 GPU_GPIO_6
GPIO7 K6 GPU_GPIO_7
GPIO8 E1 GPU_GPIO_8
GPIO9 D2 GPU_GPIO_9
GPIO10 H5 GPU_GPIO_10
GPIO11 F4 GPU_GPIO_11
GPIO12 E3 GPU_GPIO_12
GPIO13 U3 GPU_GPIO_13
GPIO14 U4 GPU_GPIO_14

GPU_ROM_CS_L AA4 ROMCS_L
GPU_ROM_SCLK AA7 ROM_SCLK
GPU_ROM_SI W2 ROM_SI
GPU_ROM_SO AA6 ROM_SO

R8695 100K 5% 1/16W MF-LF 402
R8696 10K 5% 1/16W MF-LF 402

GPU_TESTMODE_PD H2 TESTMODE
GPU_SWAPRDY_A M6 SWAPRDY_A

SPDIF J6 GPU_SPDIF
STEREO T3 GPU_STEREO
BUFRST_L F3 TP_GPU_BUFRST_L

JTAG_TCK AJ11 TP_GPU_JTAG_TCK
JTAG_TDI AK12 TP_GPU_JTAG_TDI
JTAG_TDO AL12 TP_GPU_JTAG_TDO
JTAG_TMS AK11 TP_GPU_JTAG_TMS
(IPD) JTAG_TRST_L AL13 TP_GPU_JTAG_TRST_L

=PP3V3_GPU_MIO
C8610 1UF 10% 6.3V CERM 402
C8611 1UF 10% 6.3V CERM 402

M7 MIOA_VDDQ_1
M8 MIOA_VDDQ_2
R8 MIOA_VDDQ_3
T8 MIOA_VDDQ_4
U9 MIOA_VDDQ_5
AA8 MIOB_VDDQ_1
AB7 MIOB_VDDQ_2
AB8 MIOB_VDDQ_3
AC6 MIOB_VDDQ_4
AC7 MIOB_VDDQ_5

MIOA_CLKOUT R4 GPU_MIOA_CLKOUT_P
MIOA_CLKOUT_L P4 GPU_MIOA_CLKOUT_N
MIOA_CTL3 P3 GPU_MIOA_CTL3
MIOA_DE P1 GPU_MIOA_DE
MIOAD0 P2 GPU_MIOA_D<0>
MIOAD1 N2 GPU_MIOA_D<1>
MIOAD2 N1 GPU_MIOA_D<2>
MIOAD3 N3 GPU_MIOA_D<3>
MIOAD4 M1 GPU_MIOA_D<4>
MIOAD5 M3 GPU_MIOA_D<5>
MIOAD6 P5 GPU_MIOA_D<6>
MIOAD7 N6 GPU_MIOA_D<7>
MIOAD8 N5 GPU_MIOA_D<8>
MIOAD9 M4 GPU_MIOA_D<9>
MIOAD10 L4 GPU_MIOA_D<10>
MIOAD11 L5 GPU_MIOA_D<11>
MIOA_HSYNC R3 GPU_MIOA_HSYNC
MIOA_VSYNC R1 GPU_MIOA_VSYNC

=PP3V3_GPU_MIO
R8620 49.9 1% 1/10W MF-LF 402
R8621 49.9 1% 1/16W MF-LF 402
GPU_MIOA_PD_VDDQ
GPU_MIOB_PD_VDDQ
GPU_MIOA_PU_GND
GPU_MIOB_PU_GND
R8622 49.9 1% 1/10W MF-LF 402
R8623 49.9 1% 1/16W MF-LF 402

R8616 10K 5% 1/16W MF-LF 402
R8618 10K 5% 1/16W MF-LF 402
R8617 10K 5% 1/16W MF-LF 402
R8619 10K 5% 1/16W MF-LF 402
C8617 0.1uF 10% 16V X5R 402
C8619 0.1uF 10% 16V X5R 402

GPU_MIOA_VREF L2 MIOA_VREF
GPU_MIOB_VREF Y2 MIOB_VREF
GPU_MIOA_PD_VDDQ L1 MIOACAL_PD_VDDQ
GPU_MIOA_PU_GND L3 MIOACAL_PU_GND
GPU_MIOB_PD_VDDQ Y1 MIOBCAL_PD_VDDQ
GPU_MIOB_PU_GND Y3 MIOBCAL_PU_GND

MIOB_CLKIN AE4 GPU_MIOB_CLKIN
MIOB_CLKOUT AD4 GPU_MIOB_CLKOUT_P
MIOB_CLKOUT_L AD5 GPU_MIOB_CLKOUT_N
MIOB_CTL3 AD3 GPU_MIOB_CTL3
MIOB_DE AD1 GPU_MIOB_DE
MIOBD0 AC3 GPU_MIOB_D<0>
MIOBD1 AC1 GPU_MIOB_D<1>
MIOBD2 AC2 GPU_MIOB_D<2>
MIOBD3 AB2 GPU_MIOB_D<3>
MIOBD4 AB1 GPU_MIOB_D<4>
MIOBD5 AA1 GPU_MIOB_D<5>
MIOBD6 AB3 GPU_MIOB_D<6>
MIOBD7 AA3 GPU_MIOB_D<7>
MIOBD8 AC5 GPU_MIOB_D<8>
MIOBD9 AB5 GPU_MIOB_D<9>
MIOBD10 AB4 GPU_MIOB_D<10>
MIOBD11 AA5 GPU_MIOB_D<11>
MIOB_HSYNC AF3 GPU_MIOB_HSYNC
MIOB_VSYNC AE3 GPU_MIOB_VSYNC

GPU_XTALIN U1 XTALIN
GPU_XTALOUT U2 XTALOUT
GPU_XTALOUTBUFF T2 XTALOUTBUFF
GPU_XTALSSIN T1 XTALSSIN

THERMDP K1 GPU_THERMD_P
THERMDN J1 GPU_THERMD_N

=PP1V2_GPU_PLLVDD
L8630 FERR-220-OHM 0402
PP1V2_GPU_PLLVDD_F MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V 40mA
C8633 4.7UF 20% 6.3V CERM 603
C8630 4.7UF 20% 6.3V CERM 603
C8631 0.1uF 10% 16V X5R 402

T9 PLLVDD
U10 PLLGND
G23 H_PLLVDD
T10 VID_PLLVDD

=PP1V2_GPU_H_PLLVDD
L8635 FERR-220-OHM 0402
PP1V2_GPU_H_PLLVDD_F MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V 40mA
C8637 4.7UF 20% 6.3V CERM 603
C8635 4.7UF 20% 6.3V CERM 603
C8636 0.1uF 10% 16V X5R 402

=PP1V2_GPU_VID_PLLVDD
L8640 FERR-220-OHM 0402
PP1V2_GPU_VID_PLLVDD_F MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V 40mA
C8643 4.7UF 20% 6.3V CERM 603
C8640 4.7UF 20% 6.3V CERM 603
C8641 0.1uF 10% 16V X5R 402

NV G84M GPIO/MIO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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GPIOs

	Native Func		
GPU_GPIO_0	HPD0	GPU_HPD	IN
GPU_GPIO_1	HPD1	NC_GPU_GPIO_1	
GPU_GPIO_2	LCD0_BL_PWM	GPU_BL_PWM	OUT
GPU_GPIO_3	LCD0_VDD	GPU_PANEL_EN	OUT
GPU_GPIO_4	LCD0_BL_EN	GPU_BKLT_EN	OUT
GPU_GPIO_5	VID0	TP_GPU_GSTATE<0>	
GPU_GPIO_6	VID1	TP_GPU_GSTATE<1>	
GPU_GPIO_7	MEM_VID	GPU_VGA_EN_L	
GPU_GPIO_8	THERM	NC_GPU_GPIO_8	
GPU_GPIO_9	FAN_PWM	NC_GPU_GPIO_9	
GPU_GPIO_10	MEM_VREF	FB_VREF_UNTERM	OUT
GPU_GPIO_11	SLI_SYNC	GPU_VCORE_VID0	OUT
GPU_GPIO_12	AC_DET	GPU_VCORE_VID1	OUT
GPU_GPIO_13	PWR_CTL0	GPU_VCORE_VID2	OUT
GPU_GPIO_14	PWR_CTL1	GPU_VCORE_VID3	OUT

Renamed signals

GPU_CLK27M	GPU_XTALIN
GPU_CLK27M_SS	GPU_XTALSSIN
GPU_TDIODE_P	GPU_THERMD_P
GPU_TDIODE_N	GPU_THERMD_N
GPU_DVI_DDC_CLK	GPU_I2CB_SCL
GPU_DVI_DDC_DATA	GPU_I2CB_SDA
GPU_PANEL_DDC_CLK	GPU_I2CC_SCL
GPU_PANEL_DDC_DATA	GPU_I2CC_SDA
GPU_VDD_SENSE	TP_GPU_VDD_SENSE
GPU_GND_SENSE	TP_GPU_GND_SENSE

Unused I2C Buses

NC_GPU_I2CA_SCL	GPU_I2CA_SCL
NC_GPU_I2CA_SDA	GPU_I2CA_SDA

I2CS ties into SMBus connection page
(I2CS requires pullups even if not used)

Unused signals

NC_GPU_XTALOUT	GPU_XTALOUT
NC_GPU_SPDIF	GPU_SPDIF
NC_GPU_STEREO	GPU_STEREO
NC_FBA_MA<13>	FB_A_MA<13>
NC_FBB_MA<13>	FB_B_MA<13>
NC_FBA_CMD28	TP_FBA_CMD28
NC_FBC_CMD28	TP_FBC_CMD28
NC_GPU_ROM_CS_L	GPU_ROM_CS_L
NC_GPU_ROM_SCLK	GPU_ROM_SCLK
NC_GPU_ROM_SI	GPU_ROM_SI
NC_GPU_ROM_SO	GPU_ROM_SO
NC_GPU_CSYNC	GPU_CSYNC
NC_GPU_R2	GPU_R2
NC_GPU_G2	GPU_G2
NC_GPU_B2	GPU_B2
NC_GPU_H2SYNC	GPU_H2SYNC
NC_GPU_V2SYNC	GPU_V2SYNC
NC_LVDS_U_DATAP<3>	LVDS_U_DATA_P<3>
NC_LVDS_U_DATAN<3>	LVDS_U_DATA_N<3>
NC_LVDS_L_DATAP<3>	LVDS_L_DATA_P<3>
NC_LVDS_L_DATAN<3>	LVDS_L_DATA_N<3>
TP_GPU_MIOA_CLKOUT_P	GPU_MIOA_CLKOUT_P
TP_GPU_MIOA_CLKOUT_N	GPU_MIOA_CLKOUT_N
TP_GPU_MIOA_CTL3	GPU_MIOA_CTL3
TP_GPU_MIOA_DE	GPU_MIOA_DE
TP_GPU_MIOA_D<5..2>	GPU_MIOA_D<5..2>
TP_GPU_MIOA_D<7>	GPU_MIOA_D<7>
TP_GPU_MIOA_D<11..10>	GPU_MIOA_D<11..10>
TP_GPU_MIOA_HSYNC	GPU_MIOA_HSYNC
TP_GPU_MIOA_VSYNC	GPU_MIOA_VSYNC
TP_GPU_MIOB_CLKIN	GPU_MIOB_CLKIN
TP_GPU_MIOB_CLKOUT_P	GPU_MIOB_CLKOUT_P
TP_GPU_MIOB_CLKOUT_N	GPU_MIOB_CLKOUT_N
TP_GPU_MIOB_CTL3	GPU_MIOB_CTL3
TP_GPU_MIOB_DE	GPU_MIOB_DE
TP_GPU_MIOB_D<2>	GPU_MIOB_D<2>
TP_GPU_MIOB_D<7..6>	GPU_MIOB_D<7..6>
TP_GPU_MIOB_D<10>	GPU_MIOB_D<10>
TP_GPU_MIOB_VSYNC	GPU_MIOB_VSYNC
NC_GPU_IFPD_CLK_P	GPU_IFPD_CLK_P
NC_GPU_IFPD_CLK_N	GPU_IFPD_CLK_N

Config Straps

=PP3V3_GPU_MIO

VRAM_SAMSUNG	VRAM_8M	VRAM8	NO STUFF	NO STUFF	NO STUFF	NO STUFF		
R8720	R8722	R8724	R8726	R8728	R8729	R8730	R8731	R8732
10K	10K	10K	10K	2.2K	2.2K	2.2K	2.2K	2.2K

RAMCFG0	GPU_MIOB_D<0>
RAMCFG1	GPU_MIOB_D<1>
RAMCFG2	GPU_MIOB_D<8>
RAMCFG3	GPU_MIOB_D<9>
3GIO_PADCFG0	GPU_MIOA_D<6>
3GIO_PADCFG1	GPU_MIOA_D<8>
3GIO_PADCFG2	GPU_MIOA_D<9>
3GIO_PADCFG3	GPU_MIOB_HSYNC
PEX_PLL_EN_TERM	GPU_MIOA_D<0>
SUBVENDOR (BIOS ROM PRESENT)	GPU_MIOA_D<1>
PCI_DEVID<3..0>	

VRAM_HYNIX	NO STUFF	VRAM_16M	VRAM4	
R8721	R8723	R8725	R8727	R8733
10K	10K	10K	10K	2.2K

=PP3V3_GPU_MIO

NO STUFF			
R8734	R8735	R8736	R8737
2.2K	2.2K	2.2K	2.2K

PCI_DEVID3	GPU_MIOB_D<11>
PCI_DEVID2	GPU_MIOB_D<3>
PCI_DEVID1	GPU_MIOB_D<5>
PCI_DEVID0	GPU_MIOB_D<4>

Straps not supported:

USER<3..0>	MIOA_D<5..2>
ROMTYPE<1..0>	MIOB_VSYNC, MIOB_D<10>
SLOT_CLOCK_CFG	MIOA_HSYNC
PCI_IOBAR	MIOB_D<7>
BAR2_SIZE	MIOB_DE
PCI_DEVID<4>	MIOB_CTL3

HDCP Support

=PP3V3_GPU_HDCP

HDCP R8770 10K — CRITICAL HDCP U8770 190-00001-0001 SOI — HDCP C8770 0.1UF

GPU_I2CH_SCL, GPU_I2CH_SCL

HDCP R8771 10K — NC

Analog Video Mux

=PP3V3_GPU_VIDEOMUX

C8700 0.1UF

CRITICAL U8700 TS3V340 QFN

GPU_VGA_R	S1A	DA → GPU_TV_C_VGA_R
GPU_VGA_G	S2A	
GPU_VGA_B	S1B	DB → GPU_TV_Y_VGA_G
	S2B	
GPU_TV_C	S1C	DC → GPU_TV_COMP_VGA_B
GPU_TV_Y	S2C	
GPU_TV_COMP	S1D	DD → NC
	S2D	IN ← GPU_VGA_EN_L
	THRML PAD	EN_L, GND

R8740 / R8741 / R8742 150 — Place Rs near GPU

R8743 / R8744 / R8745 150 — Place Rs near GPU

R8700 10K

TMDS Backdrive Protection

=PP3V3_GPU_TMDS — Q8790 SI2305DS SOT-23 — =PP3V3_S0GPU_TMDS_FET

R8790 10K

GPU_TMDS_PWREN_L

Q8791 SSM6N15FE SOT563

=GPUVCORE_EN

R8791 100K

Unused Clocks

GPU_XTALSSIN, GPU_XTALOUTBUFF

R8780 10K — GPU_SS_INT — R8781 10K

GPU Straps

SYNC_MASTER=M88 SYNC_DATE=08/02/2007

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Power aliases required by this page:
- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD
- =PP3V3_GPU_DAC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents: 240mA

=PP1V8_GPU_IFPX

L8800 FERR-220-OHM 0402 — 20mA peak per diff pair, 160mA peak for all pairs
C8800 4.7UF 20% 6.3V CERM 603
C8801 0.1UF 20% 10V CERM 402 — Place at AF9
C8803 0.1UF 20% 10V CERM 402 — Place at AF8

PP1V8_GPU_IFPAB_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

L8805 FERR-220-OHM 0402 — 40mA peak
C8805 4.7UF 20% 6.3V CERM 603
C8806 0.1UF 20% 10V CERM 402

PP1V8_GPU_IFPAB_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

=PP3V3_GPU_IFPCD_IOVDD

L8810 FERR-220-OHM 0402 — 20mA peak per diff pair, 200mA peak for all pairs
C8810 4.7UF 20% 6.3V CERM 603
C8811 0.1UF 20% 10V CERM 402 — Place at AD6
C8813 0.1UF 20% 10V CERM 402 — Place at AE7

PP3V3_GPU_IFPCD_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

L8815 FERR-220-OHM 0402 — 40mA peak
C8815 4.7UF 20% 6.3V CERM 603
C8816 0.1UF 20% 10V CERM 402

PP1V8_GPU_IFPCD_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

Sum of peak currents: 390mA

=PP3V3_GPU_DAC

L8820 FERR-220-OHM 0402 — 120mA peak
C8820 4.7UF 20% 6.3V CERM 603
C8821 0.1UF 20% 10V CERM 402

PP3V3_GPU_DACA_VDD_F
MIN_LINE_WIDTH=0.35 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

L8830 FERR-220-OHM 0402 — 150mA peak
C8830 4.7UF 20% 6.3V CERM 603
C8831 0.1UF 20% 10V CERM 402

PP3V3_GPU_DACB_VDD_F
MIN_LINE_WIDTH=0.35 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

NO STUFF
L8840 FERR-220-OHM 0402 — 120mA peak
C8845 4.7UF 20% 6.3V CERM 603
NO STUFF
C8840 4.7UF 20% 6.3V CERM 603
C8841 0.1UF 20% 10V CERM 402

PP3V3_GPU_DACC_VDD_F
MIN_LINE_WIDTH=0.35 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

OMIT
U8000 NB8P-GS-W-A2 BGA (5 OF 8)

AF9	IFPA_IOVDD	IFPA_TXC	AK9
AF8	IFPB_IOVDD	IFPA_TXC_L	AJ9
AC9	IFPAB_PLLVDD	IFPA_TXD0	AH6
AD9	IFPAB_PLLGND	IFPA_TXD0_L	AJ6
AM4	IFPAB_VPROBE	IFPA_TXD1	AH8
AL5	IFPAB_RSET	IFPA_TXD1_L	AH7
AD6	IFPC_IOVDD	IFPA_TXD2	AJ8
AE7	IFPD_IOVDD	IFPA_TXD2_L	AK8
AA10	IFPCD_PLLVDD	IFPA_TXD3	AJ5
AB10	IFPCD_PLLGND	IFPA_TXD3_L	AH5
AK3	IFPCD_VPROBE	IFPB_TXC	AK4
AH3	IFPCD_RSET	IFPB_TXC_L	AL4
AD10	DACA_VDD	IFPB_TXD4	AM6
AG9	DACA_IDUMP	IFPB_TXD4_L	AM5
AH10	DACA_VREF	IFPB_TXD5	AM7
AH9	DACA_RSET	IFPB_TXD5_L	AL7
V8	DACB_VDD	IFPB_TXD6	AK6
V7	DACB_IDUMP	IFPB_TXD6_L	AK5
R5	DACB_VREF	IFPB_TXD7	AK7
R7	DACB_RSET	IFPB_TXD7_L	AL8
AD7	DACC_VDD	IFPC_TXC	AM2
AG4	DACC_IDUMP	IFPC_TXC_L	AM3
AH4	DACC_VREF	IFPC_TXD0	AE2
AF5	DACC_RSET	IFPC_TXD0_L	AE1
G2	I2CC_SCL	IFPC_TXD1	AF1
G1	I2CC_SDA	IFPC_TXD1_L	AF2
G3	I2CH_SCL	IFPC_TXD2	AG1
H3	I2CH_SDA	IFPC_TXD2_L	AH1
C1	I2CS_SCL	IFPD_TXC	AG3
B1	I2CS_SDA	IFPD_TXC_L	AH2
		IFPD_TXD4	AK1
		IFPD_TXD4_L	AJ1
		IFPD_TXD5	AL2
		IFPD_TXD5_L	AL1
		IFPD_TXD6	AJ2
		IFPD_TXD6_L	AJ3
		DACA_RED	AH11
		DACA_GREEN	AJ12
		DACA_BLUE	AH12
		DACA_HSYNC	AF10
		DACA_VSYNC	AK10
		DACB_RED	R6
		DACB_GREEN	T5
		DACB_BLUE	T6
		DACB_CSYNC	U5
		DACC_RED	AF6
		DACC_GREEN	AG6
		DACC_BLUE	AE5
		DACC_HSYNC	AG7
		DACC_VSYNC	AG5
		I2CA_SCL	K2
		I2CA_SDA	J3
		I2CB_SCL	H4
		I2CB_SDA	J4

LVDS_L_CLK_P	OUT 74 87
LVDS_L_CLK_N	OUT 74 87
LVDS_L_DATA_P<0>	OUT 74 87
LVDS_L_DATA_N<0>	OUT 74 87
LVDS_L_DATA_P<1>	OUT 74 87
LVDS_L_DATA_N<1>	OUT 74 87
LVDS_L_DATA_P<2>	OUT 74 87
LVDS_L_DATA_N<2>	OUT 74 87
LVDS_L_DATA_P<3>	OUT 71 87
LVDS_L_DATA_N<3>	OUT 71 87
LVDS_U_CLK_P	OUT 74 87
LVDS_U_CLK_N	OUT 74 87
LVDS_U_DATA_P<0>	OUT 74 87
LVDS_U_DATA_N<0>	OUT 74 87
LVDS_U_DATA_P<1>	OUT 74 87
LVDS_U_DATA_N<1>	OUT 74 87
LVDS_U_DATA_P<2>	OUT 74 87
LVDS_U_DATA_N<2>	OUT 74 87
LVDS_U_DATA_P<3>	OUT 71 87
LVDS_U_DATA_N<3>	OUT 71 87
TMDS_CLK_P	OUT 78 87
TMDS_CLK_N	OUT 78 87
TMDS_DATA_P<0>	OUT 78 87
TMDS_DATA_N<0>	OUT 78 87
TMDS_DATA_P<1>	OUT 78 87
TMDS_DATA_N<1>	OUT 78 87
TMDS_DATA_P<2>	OUT 78 87
TMDS_DATA_N<2>	OUT 78 87
GPU_IFPD_CLK_P	OUT 71
GPU_IFPD_CLK_N	OUT 71
TMDS_DATA_P<3>	OUT 78 87
TMDS_DATA_N<3>	OUT 78 87
TMDS_DATA_P<4>	OUT 78 87
TMDS_DATA_N<4>	OUT 78 87
TMDS_DATA_P<5>	OUT 78 87
TMDS_DATA_N<5>	OUT 78 87
GPU_VGA_R	OUT 71 87
GPU_VGA_G	OUT 71 87
GPU_VGA_B	OUT 71 87
GPU_VGA_HSYNC	OUT 78 87
GPU_VGA_VSYNC	OUT 78 87
GPU_TV_C	OUT 71 87
GPU_TV_Y	OUT 71 87
GPU_TV_COMP	OUT 71 87
GPU_CSYNC	OUT 71
GPU_R2	OUT 71
GPU_G2	OUT 71
GPU_B2	OUT 71
GPU_H2SYNC	OUT 71
GPU_V2SYNC	OUT 71
GPU_I2CA_SCL	B1 71
GPU_I2CA_SDA	B1 71
GPU_I2CB_SCL	B1 71
GPU_I2CB_SDA	B1 71

Composite/S-Video	VGA	Component
C	R	Pr
Y	G	Y
Comp	B	Pb

I2CS must be pulled up if not used
I2CS addr fixed at 0x9E,0x9F

GPU_IFPAB_RSET 72
GPU_IFPCD_RSET 72
GPU_DACA_RSET 72
GPU_DACB_RSET 72
GPU_DACC_RSET 72

NO STUFF R8850 1K 1% 1/16W MF-LF 402
NO STUFF R8851 1K 1% 1/16W MF-LF 402
R8852 124 1% 1/16W MF-LF 402
R8853 124 1% 1/16W MF-LF 402
R8854 124 1% 1/16W MF-LF 402

GPU_DACA_VREF 72
GPU_DACB_VREF 72
GPU_DACC_VREF 72

C8852 0.1UF 20% 10V CERM 402
C8853 0.1UF 20% 10V CERM 402
C8854 0.1UF 20% 10V CERM 402

GPU_IFPAB_VPROBE 72
GPU_IFPCD_VPROBE 72

NO STUFF C8855 0.01UF 20% 16V CERM 402
NO STUFF C8856 0.01UF 20% 16V CERM 402

NV G84M Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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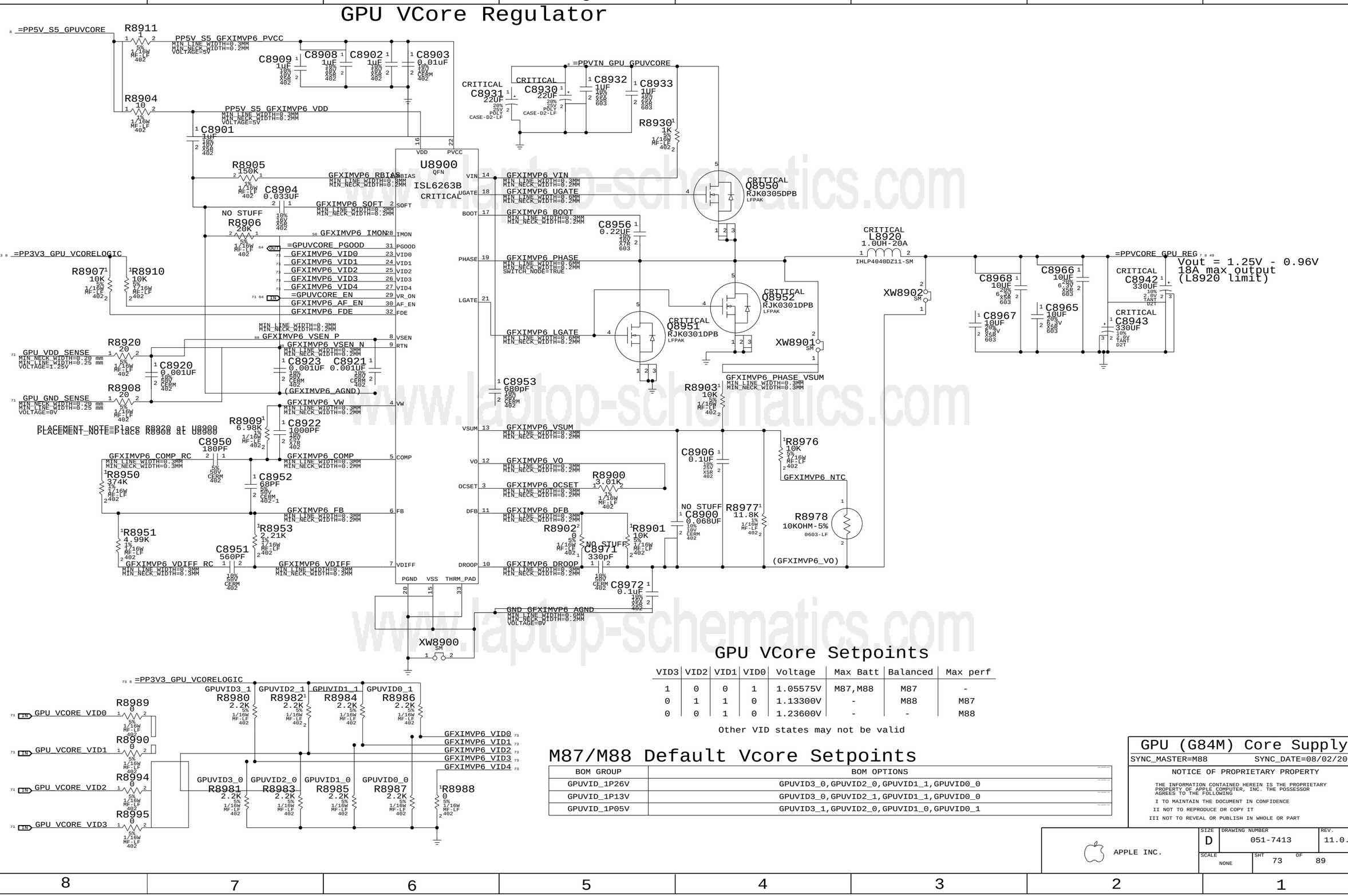
SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 72 OF 89	

GPU VCore Regulator



GPU VCore Setpoints

VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	0	0	1	1.05575V	M87,M88	M87	-
0	1	1	0	1.13300V	-	M88	M87
0	0	1	0	1.23600V	-	-	M88

Other VID states may not be valid

M87/M88 Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_1P26V	GPUVID3_0,GPUVID2_0,GPUVID1_1,GPUVID0_0
GPUVID_1P13V	GPUVID3_0,GPUVID2_1,GPUVID1_1,GPUVID0_0
GPUVID_1P05V	GPUVID3_1,GPUVID2_0,GPUVID1_0,GPUVID0_1

GPU (G84M) Core Supply

SYNC_MASTER=M88 SYNC_DATE=08/02/2007

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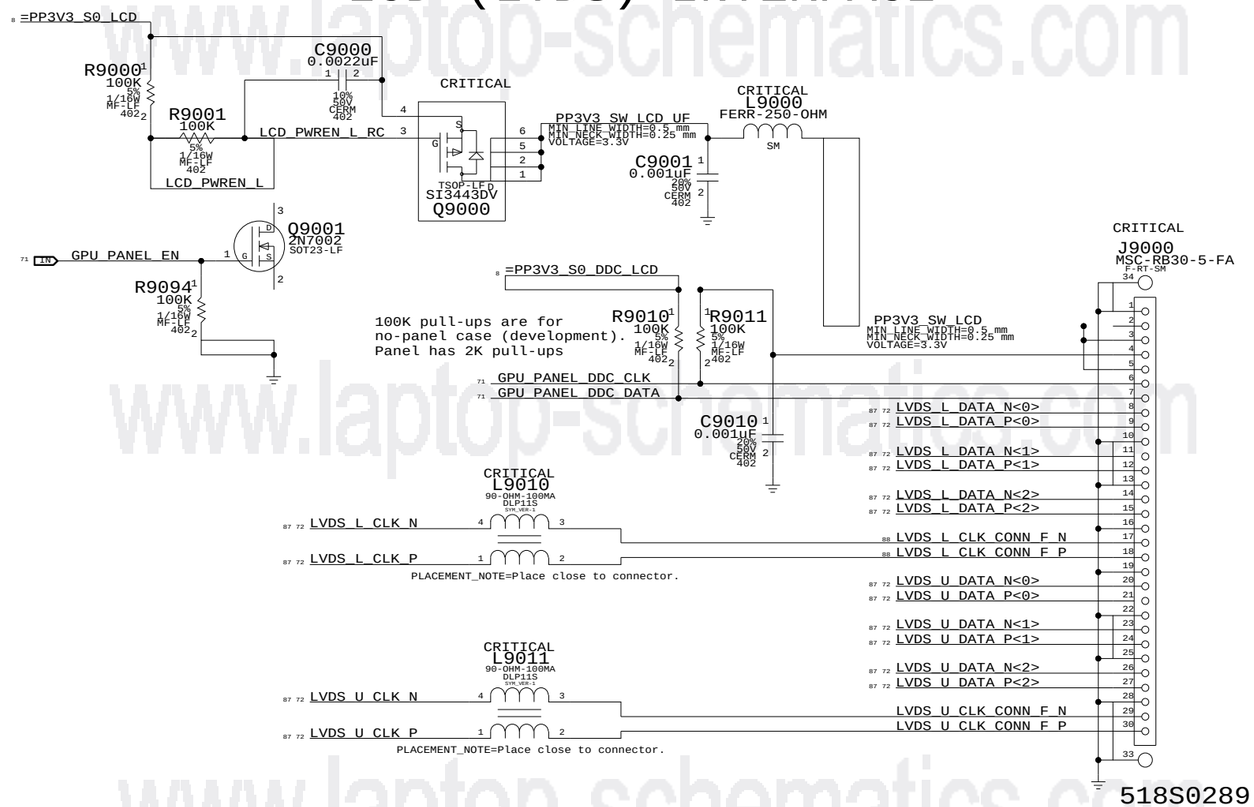
SCALE: NONE	SHT 73 OF 89	

LCD (LVDS) INTERFACE



LVDS Display Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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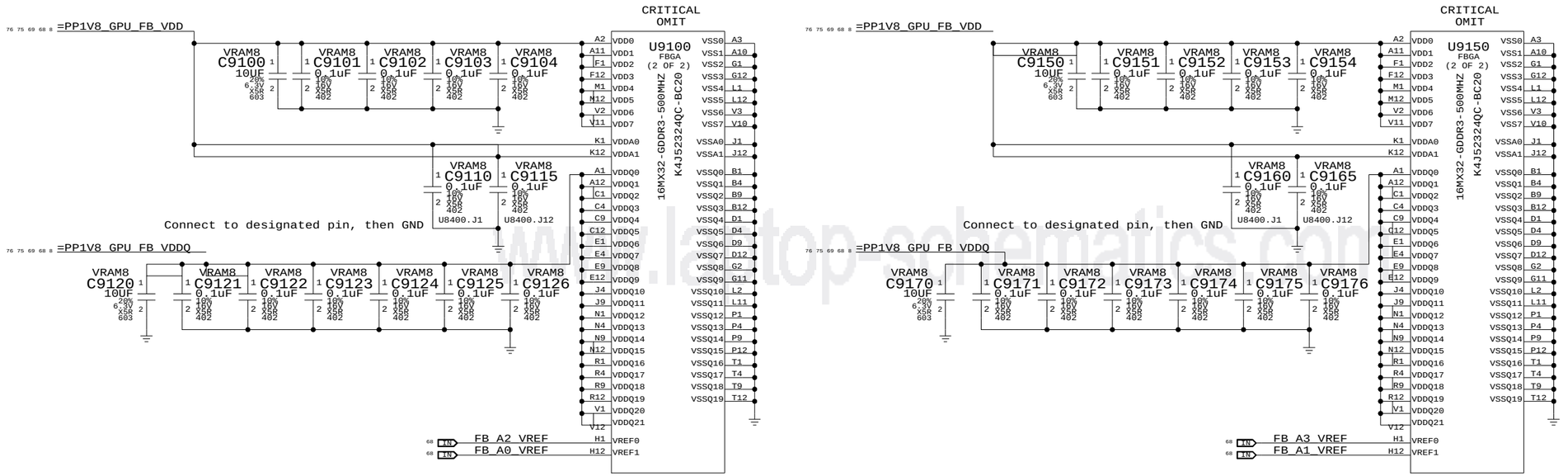
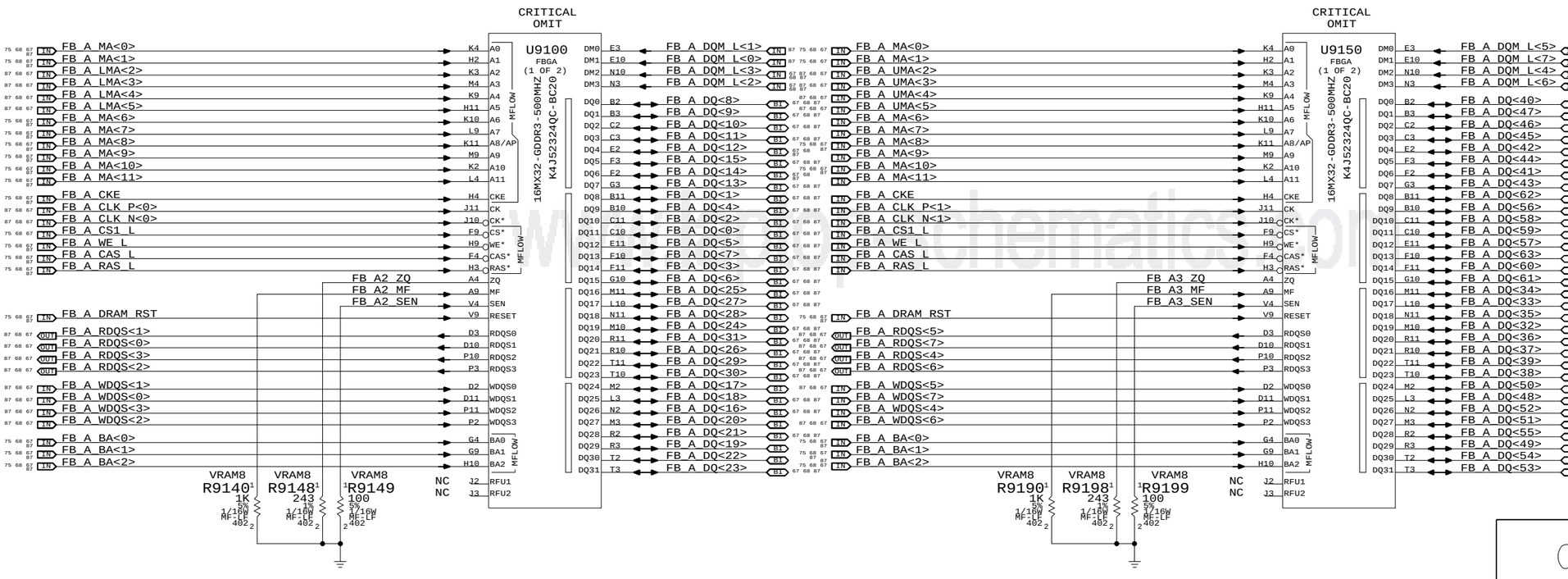
SCALE: NONE

SHT 74 OF 89





Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer A (Bot)

SYNC_MASTER=M88_MLB_VRAMSUB SYNC_DATE=06/19/2007

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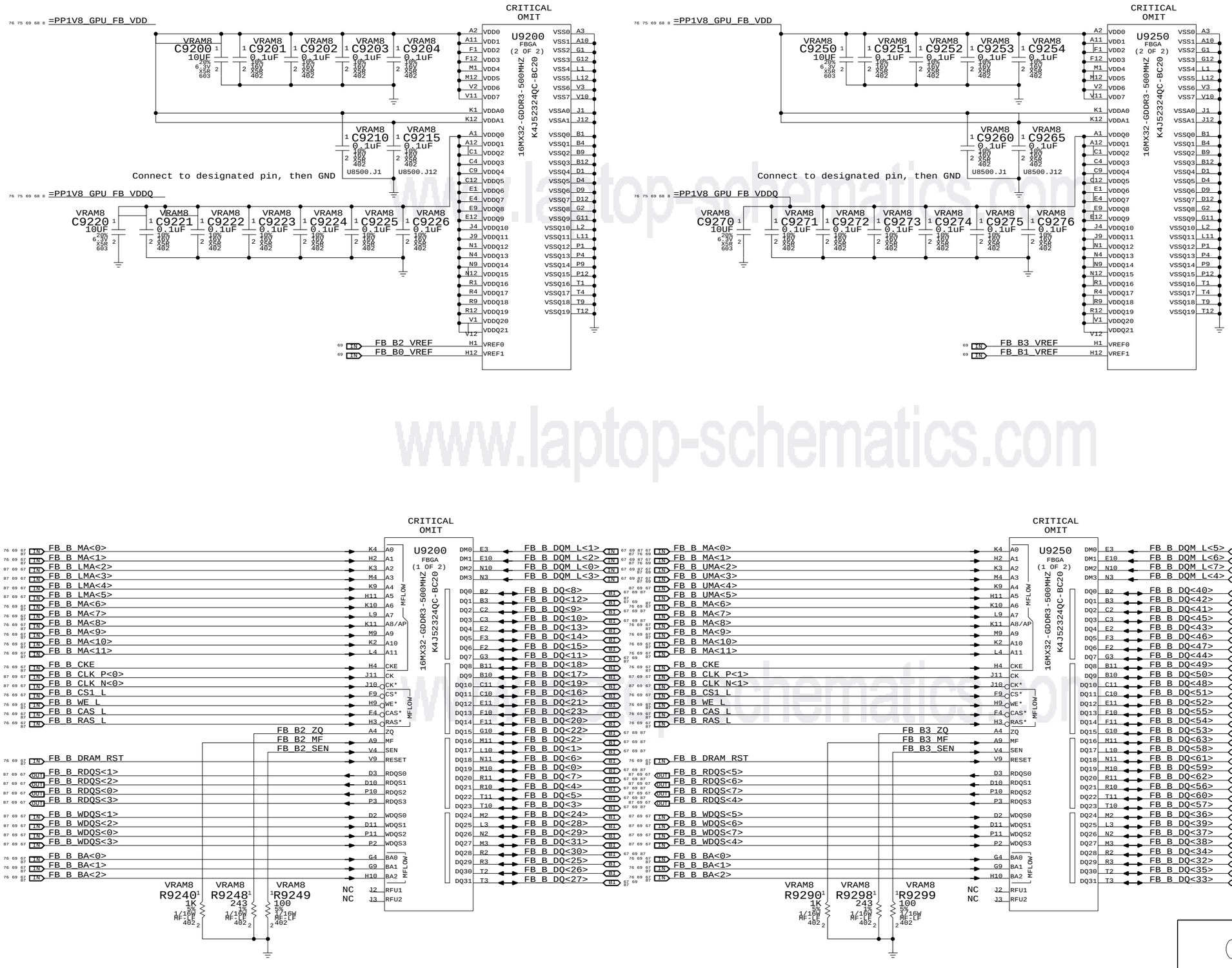
SCALE: NONE	SHT 75 OF 89	



Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer B (Bot)

SYNC_MASTER=M88_MLB_VRAM_SCH SYNC_DATE=06/19/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
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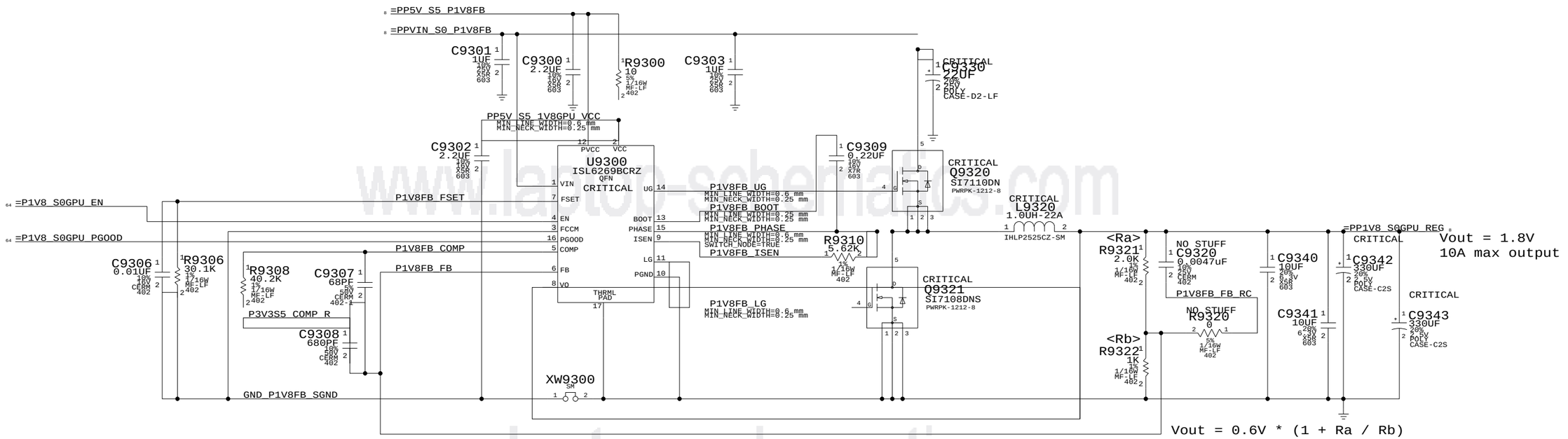
1.8V Frame Buffer Regulator



1.8V FB Power Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0

SCALE	SHT	OF
NONE	77	89

TMDS Filtering

(Place close to GPU) (Place close to connector)

TMDS_DATA_N<0> — NO STUFF R9462 49.9 1% 1/16W MF-LF 402 — CRITICAL L9460 90-OHM-100MA 1210-4SM1 — TMDS_DATA_F_N<0>
=PP3V3_GPU_TMDSBIAS — NO STUFF C9462 0.01UF 10% 16V CERM 402
SIGNAL_MODEL=EMPTY TMDS_DATA_R0
NO STUFF R9463 49.9 1% 1/16W MF-LF 402
TMDS_DATA_P<0> — TMDS_DATA_F_P<0>
PLACEMENT_NOTE=Place close to connector.

TMDS_DATA_N<1> — NO STUFF R9466 49.9 1% 1/16W MF-LF 402 — CRITICAL L9464 90-OHM-100MA 1210-4SM1 — TMDS_DATA_F_N<1>
=PP3V3_GPU_TMDSBIAS — NO STUFF C9466 0.01UF 10% 16V CERM 402
SIGNAL_MODEL=EMPTY TMDS_DATA_R1
NO STUFF R9467 49.9 1% 1/16W MF-LF 402
TMDS_DATA_P<1> — TMDS_DATA_F_P<1>
PLACEMENT_NOTE=Place close to connector.

TMDS_DATA_N<2> — NO STUFF R9470 49.9 1% 1/16W MF-LF 402 — CRITICAL L9468 90-OHM-100MA 1210-4SM1 — TMDS_DATA_F_N<2>
=PP3V3_GPU_TMDSBIAS — NO STUFF C9470 0.01UF 10% 16V CERM 402
SIGNAL_MODEL=EMPTY TMDS_DATA_R2
NO STUFF R9471 49.9 1% 1/16W MF-LF 402
TMDS_DATA_P<2> — TMDS_DATA_F_P<2>
PLACEMENT_NOTE=Place close to connector.

TMDS_CLK_N — R9472 0 5% 1/16W MF-LF 402 — TMDS_CLK_R_N — CRITICAL L9472 370-OHM SM — TMDS_CLK_F_N
=PP3V3_GPU_TMDSBIAS — NO STUFF C9474 0.01UF 10% 16V CERM 402
SIGNAL_MODEL=EMPTY TMDS_CLK_CMF
NO STUFF R9475 49.9 1% 1/16W MF-LF 402
TMDS_CLK_P — R9473 0 5% 1/16W MF-LF 402 — TMDS_CLK_R_P — TMDS_CLK_F_P
PLACEMENT_NOTE=Place close to connector.

TMDS_DATA_N<3> — NO STUFF R9478 49.9 1% 1/16W MF-LF 402 — CRITICAL L9476 90-OHM-100MA 1210-4SM1 — TMDS_DATA_F_N<3>
=PP3V3_GPU_TMDSBIAS — NO STUFF C9478 0.01UF 10% 16V CERM 402
SIGNAL_MODEL=EMPTY TMDS_DATA_R3
NO STUFF R9479 49.9 1% 1/16W MF-LF 402
TMDS_DATA_P<3> — TMDS_DATA_F_P<3>
PLACEMENT_NOTE=Place close to connector.

TMDS_DATA_N<4> — NO STUFF R9482 49.9 1% 1/16W MF-LF 402 — CRITICAL L9480 90-OHM-100MA 1210-4SM1 — TMDS_DATA_F_N<4>
=PP3V3_GPU_TMDSBIAS — NO STUFF C9482 0.01UF 10% 16V CERM 402
SIGNAL_MODEL=EMPTY TMDS_DATA_R4
NO STUFF R9483 49.9 1% 1/16W MF-LF 402
TMDS_DATA_P<4> — TMDS_DATA_F_P<4>
PLACEMENT_NOTE=Place close to connector.

TMDS_DATA_N<5> — NO STUFF R9486 49.9 1% 1/16W MF-LF 402 — CRITICAL L9484 90-OHM-100MA 1210-4SM1 — TMDS_DATA_F_N<5>
=PP3V3_GPU_TMDSBIAS — NO STUFF C9486 0.01UF 10% 16V CERM 402
SIGNAL_MODEL=EMPTY TMDS_DATA_R5
NO STUFF R9487 49.9 1% 1/16W MF-LF 402
TMDS_DATA_P<5> — TMDS_DATA_F_P<5>
PLACEMENT_NOTE=Place close to connector.

VGA SYNC Buffers

=PP3V3_GPU_VGASYNC — PLACEMENT_NOTE=Place close to connector. — U9450 MC74VHC1G08 SC70 — R9450 33 5% 1/16W MF-LF 402
GPU_VGA_VSYNC — C9450 0.1UF 10% 25V CERM 402 — VGA_VSYNC_R — VGA_VSYNC

=PP3V3_GPU_VGASYNC — PLACEMENT_NOTE=Place close to connector. — U9451 MC74VHC1G08 SC70 — R9451 33 5% 1/16W MF-LF 402
GPU_VGA_HSYNC — C9451 0.1UF 10% 25V CERM 402 — VGA_HSYNC_R — VGA_HSYNC

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

GPU_TV_COMP_VGA_B — VGA_TERM_FILTER R9440 150 1% 1/16W MF-LF 402 — CRITICAL FL9440 210MHZ MEA2010P-SM — C9440 3.3PF 0.25PF 50V CERM 402 — VGA_B (DACB TV COMP)
GPU_TV_Y_VGA_G — VGA_TERM_FILTER R9441 150 1% 1/16W MF-LF 402 — C9441 3.3PF 0.25PF 50V CERM 402 — VGA_G (DACB TV Y)
GPU_TV_C_VGA_R — VGA_TERM_FILTER R9442 150 1% 1/16W MF-LF 402 — C9442 3.3PF 0.25PF 50V CERM 402 — VGA_R (DACB TV C)

DVI INTERFACE

DVI DDC Current Limit
(55mA requirement per DVI spec)

=PP5V_S0_DVI_DDC — CRITICAL F9410 0.5AMP-13.2V SM-LF — PP5V_S0_DDC_F (MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V) — CRITICAL L9410 400-OHM-EMI SM-1 — PP5V_S0_DDC (MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V)
C9410 0.01UF 10% 25V CERM 603
CRITICAL J9400 QH11121-RIG02-4F F-RT-TH-DVI

TMDS_DATA_F_N<0>	17	1	TMDS_DATA_F_N<2>
	9	2	TMDS_DATA_F_N<1>
TMDS_DATA_F_P<0>	18	10	TMDS_DATA_F_P<1>
	19	3	
TMDS_DATA_F_N<5>	20	4	TMDS_DATA_F_N<4>
	12		TMDS_DATA_F_N<3>
TMDS_DATA_F_P<5>	21	5	TMDS_DATA_F_P<4>
	13		TMDS_DATA_F_P<3>
	22	6	DVI_DDC_CLK_R
	14	7	(PP5V_S0_DDC)
	15		DVI_DDC_DATA_R
TMDS_CLK_F_P	23	8	VGA_VSYNC
TMDS_CLK_F_N	24	16	DVI_HPD_R
VGA_B	C3	C1	VGA_R
	C5B	C5A	
VGA_HSYNC	C4	C2	VGA_G
	33	31	
	34	32	

514-0278

VGA_TERM_CONN R9445 150 1% 1/16W MF-LF 402
VGA_TERM_CONN R9443 150 1% 1/16W MF-LF 402
VGA_TERM_CONN R9444 150 1% 1/16W MF-LF 402

Isolation required for DVI->ADC Adapter

PP5V_S0_DDC_PULLUPS (MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V) — D9410 SOD-123 B0530WXF
R9410 4.7K 5% 1/16W MF-LF 402 — R9412 4.7K 5% 1/16W MF-LF 402
R9411 100 5% 1/16W MF-LF 402 — DVI_DDC_CLK
C9411 100pF 5% 50V CERM 402
R9413 100 5% 1/16W MF-LF 402 — DVI_DDC_DATA
C9413 100pF 5% 50V CERM 402
R9414 100 5% 1/16W MF-LF 402 — DVI_HPD
C9414 100pF 5% 50V CERM 402
R9415 20K 5% 1/16W MF-LF 402

GPU Isolation / Level-Shift

=PP3V3_GPU_DVI
Q9411 2N7002DW-X-F SOT-363 — R9420 10K 5% 1/16W MF-LF 402 — GPU_DVI_DDC_CLK
Q9411 2N7002DW-X-F SOT-363 — R9421 10K 5% 1/16W MF-LF 402 — GPU_DVI_DDC_DATA
Q9414 2N7002DW-X-F SOT-363 — R9422 100K 5% 1/16W MF-LF 402 — GPU_HPD
R9416 10K 5% 1/16W MF-LF 402 — DVI_HOTPLUG_DET

DVI Display Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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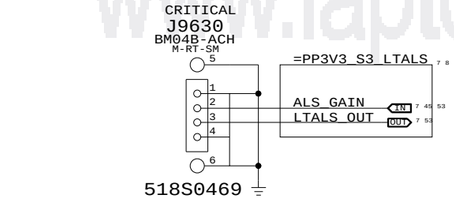
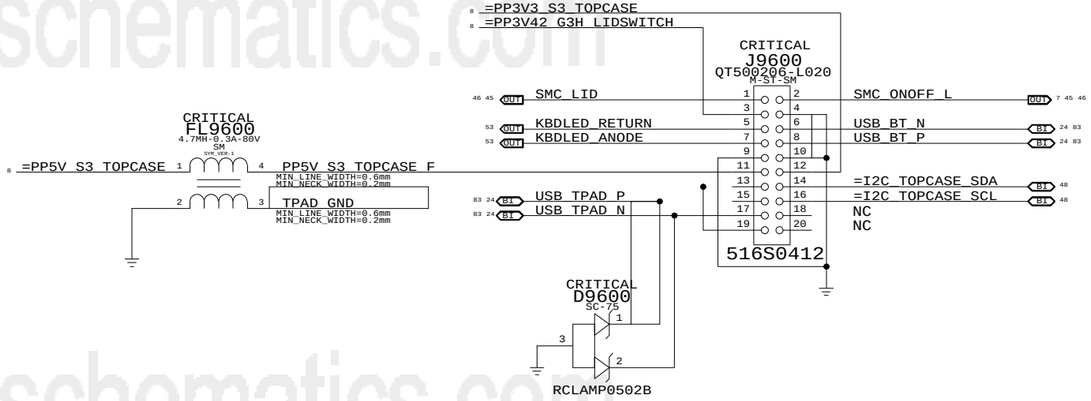
SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 78 OF 89	

Left ALS Connector

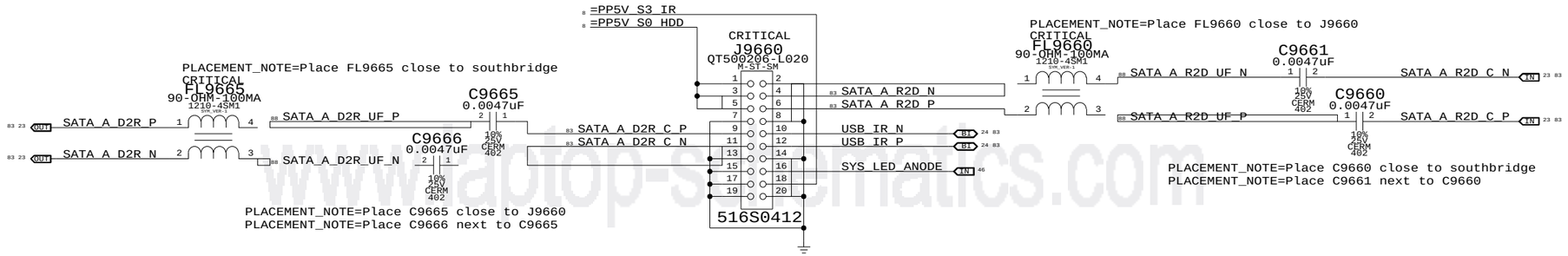


White colored version of 518S0369

Top-Case Connector



SATA HDD & IR & SIL Flex Connector



Project Specific Connectors

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

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SCALE: NONE	SHT 79 OF 89	

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	?
FSB_DATA2DATA	*	=2:1_SPACING	?
FSB_DSTB	*	=3:1_SPACING	?
FSB_DATA2DSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_ADS_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BNR_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BPRI_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BREQ0_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DBSY_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DEFER_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DPWR_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DRDY_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HIT_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HITM_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_LOCK_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_TRDY_L	10 14
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB_CPURST_L	7 10 13 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_D_L<15..0>	7 10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_DINV_L<0>	7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<0>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<0>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_D_L<31..16>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_DINV_L<1>	7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<1>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<1>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_D_L<47..32>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_DINV_L<2>	7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<2>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<2>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_D_L<63..48>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_DINV_L<3>	7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<3>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_A_L<16..3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	7 10 14
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<0>	7 10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB_A_L<35..17>	7 10 14
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<1>	7 10 14
CPU_IERR_L	CPU_55S		CPU_IERR_L	10
CPU_FERR_L	CPU_55S		CPU_FERR_L	10 23
CPU_PROCHOT_L	CPU_55S	CPU_2TO1	CPU_PROCHOT_L	10 46 58
CPU_PWRGD	CPU_55S		CPU_PWRGD	7 10 13 23
CPU_FROM_SB	CPU_55S		CPU_INTR	10 23
CPU_FROM_SB	CPU_55S		CPU_NMI	10 23
CPU_FROM_SB	CPU_55S		CPU_A20M_L	10 23
CPU_FROM_SB	CPU_55S		CPU_DPSLP_L	7 10 23
CPU_FROM_SB	CPU_55S		CPU_IGNNE_L	10 23
CPU_INIT_L	CPU_55S		CPU_INIT_L	10 23 47
CPU_FROM_SB	CPU_55S		CPU_SMI_L	10 23
CPU_FROM_SB	CPU_55S		CPU_STPCLK_L	7 10 23
PM_THRMTRIP_L	CPU_55S	CPU_2TO1	PM_THRMTRIP_L	10 16 23 46
FSB_CPUSLP_L	CPU_55S		FSB_CPUSLP_L	7 10 14
PM_DPRSLPVR	CPU_55S	CPU_2TO1	PM_DPRSLPVR	7 16 25 58
(See above)	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	7 58
CPU_BSEL0	CPU_55S	CPU_2TO1	CPU_BSEL<0>	10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<0>	13 16 30
CPU_BSEL1	CPU_55S	CPU_2TO1	CPU_BSEL<1>	10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<1>	13 16 30
CPU_BSEL2	CPU_55S	CPU_2TO1	CPU_BSEL<2>	10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<2>	13 16 30
CPU_DPRSTP_L	CPU_55S	CPU_2TO1	CPU_DPRSTP_L	7 10 16 23 58
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU_GTLREF	10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<3>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<1>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10
XDP_TDI	CPU_55S	CPU_ITP	XDP_TDI	10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP_TDO	10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP_TMS	10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP_TCK	10 13
XDP_TRST_L	CPU_55S	CPU_ITP	XDP_TRST_L	10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP_BPM_L<4..0>	10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP_BPM_L<5>	10 13
	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 30 85
	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 30 85
(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP_CPURST_L	13
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	11 12
	CPU_55S	CPU_2TO1	IMVP6_VID<6..0>	7 12 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 58
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	58
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	58

CPU/FSB Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0

SCALE: NONE SHT 80 OF 89

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CRT_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	
LVDS	*	20 MIL	?	
CRT	*	25 MIL	?	DG Says 40 mil spacing minimum
CRT_2CRT	*	20 MIL	?	
CRT_SYNC	*	25 MIL	?	DG Says 30 mil spacing minimum
CRT_SYNC2SYNC	*	20 MIL	?	
TVDAC	*	25 MIL	?	DG Says 40 mil spacing minimum
TVDAC_2TVDAC	*	20 MIL	?	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT
CRT_SYNC	CRT_SYNC	*	CRT_SYNC2SYNC
TVDAC	TVDAC	*	TVDAC_2TVDAC

LVDS signals are 100-ohm +/- 20% differential impedence.
CRT & TVDAC signal single-ended impedence varies by location:
- 37.5-ohm +/- 15% from GMCH to first termination resistor.
- 50-ohm +/- 15% from first to second termination resistor.
- 55-ohm +/- 15% from second termination resistor to connector.

CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedence.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PEG_R2D	PCIE_100D	PCIE	PEG_R2D_P<15..0>	65
	PCIE_100D	PCIE	PEG_R2D_N<15..0>	65
	PCIE_100D	PCIE	PEG_R2D_C_P<15..0>	15 65
	PCIE_100D	PCIE	PEG_R2D_C_N<15..0>	15 65
PEG_D2R	PCIE_100D	PCIE	PEG_D2R_P<15..0>	15 65
	PCIE_100D	PCIE	PEG_D2R_N<15..0>	15 65
	PCIE_100D	PCIE	PEG_D2R_C_P<15..0>	65
	PCIE_100D	PCIE	PEG_D2R_C_N<15..0>	65
DMI_N2S	DMI_100D	DMI	DMI_N2S_P<3..0>	16 24
	DMI_100D	DMI	DMI_N2S_N<3..0>	16 24
DMI_S2N	DMI_100D	DMI	DMI_S2N_P<3..0>	16 24
	DMI_100D	DMI	DMI_S2N_N<3..0>	16 24
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_P	15 22
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_N	15 22
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_P<2..0>	15 22
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_N<2..0>	15 22
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS_A_DATA_P<3>	
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS_A_DATA_N<3>	
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_P	15 22
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_N	15 22
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_P<2..0>	15 22
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_N<2..0>	15 22
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS_B_DATA_P<3>	
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS_B_DATA_N<3>	
LVDS_IBG		LVDS	LVDS_IBG	15 22
CRT_TVO_IREF		CRT	CRT_TVO_IREF	
CRT_RED	CRT_50S	CRT	CRT_RED	
CRT_GREEN	CRT_50S	CRT	CRT_GREEN	
CRT_BLUE	CRT_50S	CRT	CRT_BLUE	
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_HSYNC_R	
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_VSYNC_R	
TV_A_DAC	CRT_50S	TVDAC	TV_A_DAC	
TV_B_DAC	CRT_50S	TVDAC	TV_B_DAC	
TV_C_DAC	CRT_50S	TVDAC	TV_C_DAC	

NB Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0

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DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM_*-style wildcards!

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_CLK_P<2..0>	16 31
	MEM_70D	MEM_CLK	MEM_CLK_N<2..0>	16 31
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<1..0>	16 31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CS_L<1..0>	16 31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_ODT<1..0>	16 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_A<14..0>	16 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_BS<2..0>	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_RAS_L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_CAS_L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_WE_L	17 31 33
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A_DQ<7..0>	17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DQ<15..8>	17 31
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A_DQ<23..16>	17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DQ<31..24>	17 31
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A_DQ<39..32>	17 31
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A_DQ<47..40>	17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DQ<55..48>	17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DQ<63..56>	17 31
MEM_A_DM0	MEM_55S	MEM_DATA	MEM_A_DM<0>	17 31
MEM_A_DM1	MEM_55S	MEM_DATA	MEM_A_DM<1>	17 31
MEM_A_DM2	MEM_55S	MEM_DATA	MEM_A_DM<2>	17 31
MEM_A_DM3	MEM_55S	MEM_DATA	MEM_A_DM<3>	17 31
MEM_A_DM4	MEM_55S	MEM_DATA	MEM_A_DM<4>	17 31
MEM_A_DM5	MEM_55S	MEM_DATA	MEM_A_DM<5>	17 31
MEM_A_DM6	MEM_55S	MEM_DATA	MEM_A_DM<6>	17 31
MEM_A_DM7	MEM_55S	MEM_DATA	MEM_A_DM<7>	17 31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	17 31
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_CLK_P<5..3>	16 32
	MEM_70D	MEM_CLK	MEM_CLK_N<5..3>	16 32
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<4..3>	16 32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CS_L<3..2>	16 32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_ODT<3..2>	16 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_A<14..0>	16 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_BS<2..0>	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_RAS_L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_CAS_L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_WE_L	17 32 33
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DQ<7..0>	17 32
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B_DQ<15..8>	17 32
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B_DQ<23..16>	17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DQ<31..24>	17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DQ<39..32>	17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DQ<47..40>	17 32
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B_DQ<55..48>	17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DQ<63..56>	17 32
MEM_B_DM0	MEM_55S	MEM_DATA	MEM_B_DM<0>	17 32
MEM_B_DM1	MEM_55S	MEM_DATA	MEM_B_DM<1>	17 32
MEM_B_DM2	MEM_55S	MEM_DATA	MEM_B_DM<2>	17 32
MEM_B_DM3	MEM_55S	MEM_DATA	MEM_B_DM<3>	17 32
MEM_B_DM4	MEM_55S	MEM_DATA	MEM_B_DM<4>	17 32
MEM_B_DM5	MEM_55S	MEM_DATA	MEM_B_DM<5>	17 32
MEM_B_DM6	MEM_55S	MEM_DATA	MEM_B_DM<6>	17 32
MEM_B_DM7	MEM_55S	MEM_DATA	MEM_B_DM<7>	17 32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	17 32

Memory Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 82 OF 89	

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_60S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	20 MIL	?
USB_2CLK	*	25 MIL	?

DG says minimum spacing 50 mils to clocks

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
IDE_PDD	IDE_55S	IDE	IDE_PDD<15..0>	23 42
IDE_PDA	IDE_55S	IDE	IDE_PDA<2..0>	23 42
IDE_PDCS	IDE_55S	IDE	IDE_PDCS1_L	23 42
IDE_PDCS	IDE_55S	IDE	IDE_PDCS3_L	23 42
IDE_CNTL	IDE_55S	IDE	IDE_PDIOW_L	23 42
IDE_PDIOR_L	IDE_55S	IDE	IDE_PDIOR_L	23 42
IDE_CNTL	IDE_55S	IDE	IDE_PDDACK_L	23 42
IDE_CNTL	IDE_55S	IDE	IDE_PDDREQ	23 42
IDE_PDIORDY	IDE_55S	IDE	IDE_PDIORDY	23 42
IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14	23 42
IDE_RST_L	IDE_55S	IDE	ODD_RST_5VTOL_L	24 42
SATA_A_R2D	SATA_100D	SATA	SATA_A_R2D_C_P	23 79
	SATA_100D	SATA	SATA_A_R2D_C_N	23 79
	SATA_100D	SATA	SATA_A_R2D_P	79
	SATA_100D	SATA	SATA_A_R2D_N	79
SATA_A_D2R	SATA_100D	SATA	SATA_A_D2R_P	23 79
	SATA_100D	SATA	SATA_A_D2R_N	23 79
	SATA_100D	SATA	SATA_A_D2R_C_P	79
	SATA_100D	SATA	SATA_A_D2R_C_N	79
SATA_B_R2D	SATA_100D	SATA	SATA_B_R2D_C_P	23 42
	SATA_100D	SATA	SATA_B_R2D_C_N	23 42
	SATA_100D	SATA	SATA_B_R2D_P	
	SATA_100D	SATA	SATA_B_R2D_N	
SATA_B_D2R	SATA_100D	SATA	SATA_B_D2R_P	23 42
	SATA_100D	SATA	SATA_B_D2R_N	23 42
	SATA_100D	SATA	SATA_B_D2R_C_P	
	SATA_100D	SATA	SATA_B_D2R_C_N	
SATA_C_R2D	SATA_100D	SATA	SATA_C_R2D_C_P	23 42
	SATA_100D	SATA	SATA_C_R2D_C_N	23 42
	SATA_100D	SATA	SATA_C_R2D_P	
	SATA_100D	SATA	SATA_C_R2D_N	
SATA_C_D2R	SATA_100D	SATA	SATA_C_D2R_P	23 42
	SATA_100D	SATA	SATA_C_D2R_N	23 42
	SATA_100D	SATA	SATA_C_D2R_C_P	
	SATA_100D	SATA	SATA_C_D2R_C_N	
SATA_RBIAS	SATA_55S		SATA_RBIAS	42
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	23 34
	HDA_55S	HDA	HDA_BIT_CLK_R	23
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	23 34
	HDA_55S	HDA	HDA_SYNC_R	23
HDA_RST_L	HDA_55S	HDA	HDA_RST_L	23 34
	HDA_55S	HDA	HDA_RST_L_R	23
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	23 34
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	23 34
	HDA_55S	HDA	HDA_SDOUT_R	23
USB_EXTA	USB_90D	USB	USB_EXTA_P	24 43
	USB_90D	USB	USB_EXTA_N	24 43
	USB_90D	USB	USB_EXTA_MUXED_P	
	USB_90D	USB	USB_EXTA_MUXED_N	
USB_MINI	USB_90D	USB	USB_MINI_P	24 34
	USB_90D	USB	USB_MINI_N	24 34
USB_EXTD	USB_90D	USB	USB_EXTD_P	9 24
	USB_90D	USB	USB_EXTD_N	9 24
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	7 24 44
	USB_90D	USB	USB_CAMERA_N	7 24 44
USB_BT	USB_90D	USB	USB_BT_P	24 79
	USB_90D	USB	USB_BT_N	24 79
USB_TPAD	USB_90D	USB	USB_TPAD_P	24 79
	USB_90D	USB	USB_TPAD_N	24 79
USB_IR	USB_90D	USB	USB_IR_P	24 79
	USB_90D	USB	USB_IR_N	24 79
USB_EXTB	USB_90D	USB	USB_EXTB_P	24 34
	USB_90D	USB	USB_EXTB_N	24 34
USB_EXCARD	USB_90D	USB	USB_EXCARD_P	24 34
	USB_90D	USB	USB_EXCARD_N	24 34
USB_EXTC	USB_90D	USB	USB_EXTC_P	9 24
	USB_90D	USB	USB_EXTC_N	9 24
USB_RBIAS	USB_60S		USB_RBIAS	24
SMB_SB_SCL	SMB_55S	SMB	SMB_CLK	25 48
SMB_SB_SDA	SMB_55S	SMB	SMB_DATA	25 48
SMB_SB_ME_SCL	SMB_55S	SMB	SMB_ME_CLK	25 48
SMB_SB_ME_SDA	SMB_55S	SMB	SMB_ME_DATA	25 48
SPI_SCLK	SPI_55S	SPI	SPI_SCLK_R	24 55
	SPI_55S	SPI	SPI_SCLK	55
	SPI_55S	SPI	SPI_A_SCLK_R	
	SPI_55S	SPI	SPI_B_SCLK_R	
SPI_SI	SPI_55S	SPI	SPI_SI_R	24 55
	SPI_55S	SPI	SPI_SI	
	SPI_55S	SPI	SPI_A_SI_R	55
	SPI_55S	SPI	SPI_B_SI_R	
SPI_SO	SPI_55S	SPI	SPI_SO	24 55
	SPI_55S	SPI	SPI_A_SO_R	55
	SPI_55S	SPI	SPI_B_SO	
	SPI_55S	SPI	SPI_B_SO_R	
SPI_CE_L0	SPI_55S	SPI	SPI_CE_R_L<0>	24 55
	SPI_55S	SPI	SPI_CE_L<0>	55
SPI_CE_L1	SPI_55S	SPI	SPI_CE_R_L<1>	
	SPI_55S	SPI	SPI_CE_L<1>	

SB Constraints (1 of 2)

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 83 OF 89	

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Controller Link (AMT) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLINK_12MIL	*	=STANDARD	12 MILS	5 MILS	300 MILS	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLINK	*	=1.8:1_SPACING	?
CLINK_VREF	*	12 MILS	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Ethernet (Yukon) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MILS	?

SOURCE: Based on Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
PCI_AD	PCI_55S	PCI	PCI_AD<18..0> 24 38
PCI_AD19	PCI_55S	PCI	PCI_AD<19> 24 38
PCI_AD20	PCI_55S	PCI	PCI_AD<20> 24 38
PCI_AD	PCI_55S	PCI	PCI_AD<31..21> 24 38
PCI_AD	PCI_55S	PCI	PCI_PAR 24 38
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0> 24 38
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L 24 38
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L 24 38
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L 24 38
PCI_LOCK_L	PCI_55S	PCI	PCI_LOCK_L 24
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L 24 38
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L 24 38
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L 24 38
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L 24 38
PCI_FW_REQ_L	PCI_55S	PCI	PCI_FW_REQ_L 24 38
PCI_FW_GNT_L	PCI_55S	PCI	PCI_FW_GNT_L 24 38
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L 24
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L
PCI_REQ2_L	PCI_55S	PCI	PCI_REQ2_L 24
PCI_GNT2_L	PCI_55S	PCI	PCI_GNT2_L
INT_PIRQA_L	PCI_55S	PCI	INT_PIRQA_L 24
INT_PIRQB_L	PCI_55S	PCI	INT_PIRQB_L 24
INT_PIRQC_L	PCI_55S	PCI	INT_PIRQC_L 24
INT_PIRQD_L	PCI_55S	PCI	INT_PIRQD_L 24 38
INT_PIRQE_L	PCI_55S	PCI	INT_PIRQE_L 9 24
INT_PIRQF_L	PCI_55S	PCI	INT_PIRQF_L 24
PCIE_A_R2D	PCIE_100D	PCIE	PCIE_A_R2D_C_P
	PCIE_100D	PCIE	PCIE_A_R2D_C_N
PCIE_A_D2R	PCIE_100D	PCIE	PCIE_A_D2R_P
	PCIE_100D	PCIE	PCIE_A_D2R_N
PCIE_B_R2D	PCIE_100D	PCIE	PCIE_B_R2D_C_P
	PCIE_100D	PCIE	PCIE_B_R2D_C_N
PCIE_B_D2R	PCIE_100D	PCIE	PCIE_B_D2R_P
	PCIE_100D	PCIE	PCIE_B_D2R_N
PCIE_EXCARD_R2D	PCIE_100D	PCIE	PCIE_EXCARD_R2D_C_P 34
	PCIE_100D	PCIE	PCIE_EXCARD_R2D_C_N 34
PCIE_EXCARD_D2R	PCIE_100D	PCIE	PCIE_EXCARD_D2R_P 34
	PCIE_100D	PCIE	PCIE_EXCARD_D2R_N 34
PCIE_FW_R2D	PCIE_100D	PCIE	PCIE_FW_R2D_C_P
	PCIE_100D	PCIE	PCIE_FW_R2D_C_N
PCIE_FW_D2R	PCIE_100D	PCIE	PCIE_FW_D2R_P
	PCIE_100D	PCIE	PCIE_FW_D2R_N
PCIE_MINI_R2D	PCIE_100D	PCIE	PCIE_MINI_R2D_C_P 24 34
	PCIE_100D	PCIE	PCIE_MINI_R2D_C_N 24 34
PCIE_MINI_D2R	PCIE_100D	PCIE	PCIE_MINI_D2R_P 24 34
	PCIE_100D	PCIE	PCIE_MINI_D2R_N 24 34
GLAN_COMP			GLAN_COMP 23
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_CLK 16 25
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_DATA 16 25
CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK_NB_RESET_L 16 25
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_CLK
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_DATA
CLINK_WLAN_RESET_L	CLINK_55S	CLINK	CLINK_WLAN_RESET_L
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB_CLINK_VREF 16
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF0 25
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF1 25
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE_ENET_R2D_C_P 24 35
	PCIE_100D	PCIE	PCIE_ENET_R2D_C_N 24 35
	PCIE_100D	PCIE	PCIE_ENET_R2D_P 35
	PCIE_100D	PCIE	PCIE_ENET_R2D_N 35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE_ENET_D2R_P 24 35
	PCIE_100D	PCIE	PCIE_ENET_D2R_N 24 35
	PCIE_100D	PCIE	PCIE_ENET_D2R_C_P 35
	PCIE_100D	PCIE	PCIE_ENET_D2R_C_N 35
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<0> 35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<0> 35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<1> 35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<1> 35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<2> 35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<2> 35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3> 35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<3> 35 37

SB Constraints (2 of 2)

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0

SCALE	SHT	OF
NONE	84	89

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_P	29 30
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_N	29 30
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_P	29 30
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_N	29 30
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_P	29 30
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_N	29 30
CK505_PCIF0	CLK_MED_55S	CLK_MED	CK505_PCIF0_CLK_ITPEN	29 30
CK505_PCIF1	CLK_MED_55S	CLK_MED	CK505_PCIF1_CLK	29 30
CK505_PCI1	CLK_MED_55S	CLK_MED	CK505_PCI1_CLK	29 30
CK505_PCI2	CLK_MED_55S	CLK_MED	CK505_PCI2_CLK	29 30
CK505_PCI3	CLK_MED_55S	CLK_MED	CK505_PCI3_CLK	29 30
CK505_PCI4	CLK_MED_55S	CLK_MED	CK505_PCI4_CLK	29 30
CK505_PCI5	CLK_MED_55S	CLK_MED	CK505_PCI5_CLK_FCTSEL	29 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_48M_FSA	29 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_REF0_FSC	29 30
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_N	29 30
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_N	29 30
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_N	29 30
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_N	29 30
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_N	29 30
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_N	29 30
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_N	29 30
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_N	29 30
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_N	29 30
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_N	29 30
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10 30
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10 30
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	7 14 30
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	7 14 30
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 30 80
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 30 80
(CK505_PCIF0)	CLK_MED_55S	CLK_MED	PCI_CLK33M_LPCPLUS	7 30 47
(CK505_PCIF1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SB	24 30
(CK505_PCI1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_FW	30 38
(CK505_PCI2)	CLK_MED_55S	CLK_MED	PCI_CLK33M_TPM	
(CK505_PCI3)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SMC	30 45
			CK505_PCI4 is project-specific	
			CK505_PCI5 is project-specific	
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB_CLK48M_USBCTLR	25 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB_CLK14P3M_TIMER	25 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_FSA	30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_FSC	30
(CK505_DOT96)	CRT_50S	GND	NB_CLK96M_DOT_P	
(CK505_DOT96)	CRT_50S	GND	NB_CLK96M_DOT_N	
(CK505_LVDS)	CRT_50S	GND	NB_CLK100M_DPLLSS_P	
(CK505_LVDS)	CRT_50S	GND	NB_CLK100M_DPLLSS_N	
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	9
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	9
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	24 30
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	24 30
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	30 34
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	30 34
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_P	23 30
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_N	23 30
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	7 16 30
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	7 16 30
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	30 34
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	30 34
			CK505_SRC7 is project-specific	
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	30 35
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	30 35

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	48
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	48
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	48
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	48
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	48
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	48
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	48
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	48
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	48
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	48

Clock & SMC Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 85 OF 89	

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW	*	=2:1_SPACING	?
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

NET_TYPE ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
FW_D_CTL	FW_55S	FW	FW_LINK<7..0>	
FW_D_CTL	FW_55S	FW	FW_CTL<1..0>	
FW_LCLK	CLK_MED_55S	CLK_MED	CLKFW_LINK_LCLK	
	CLK_MED_55S	CLK_MED	CLKFW_PHY_LCLK	38 39
FW_PCLK	CLK_MED_55S	CLK_MED	CLKFW_LINK_PCLK	38 39
	CLK_MED_55S	CLK_MED	CLKFW_PHY_PCLK	
FW_LKON	FW_55S	FW	FW_LKON	
	FW_55S	FW	FW_LKON_R	
FW_LPS	FW_55S	FW	FW_LPS	38 39
FW_LREQ	FW_55S	FW	FW_LREQ	38 39
FW_PINT	FW_55S	FW	FW_PINT	38 39
FWPHY_CLK98P304M_XI	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI_R	
	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI	
FW_0_TPA	FW_110D	FW_TP	FW_0_TPA_P	39 41
FW_0_TPA	FW_110D	FW_TP	FW_0_TPA_N	39 41
FW_0_TPB	FW_110D	FW_TP	FW_0_TPB_P	39 41
FW_0_TPB	FW_110D	FW_TP	FW_0_TPB_N	39 41
FW_1_TPA	FW_110D	FW_TP	FW_1_TPA_P	39 41
FW_1_TPA	FW_110D	FW_TP	FW_1_TPA_N	39 41
FW_1_TPB	FW_110D	FW_TP	FW_1_TPB_P	39 41
FW_1_TPB	FW_110D	FW_TP	FW_1_TPB_N	39 41

Port 2 Not Used

FireWire Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0

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GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R55SE	*	=55_OHM_SE	=40_OHM_SE	=55_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR3_46SE	*	=46_OHM_SE	=46_OHM_SE	=46_OHM_SE	=46_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TMDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
VGA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TMDS	*	20 MIL	?
VGA	*	20 MIL	?
VGA_SYNC	*	20 MIL	?

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_A_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<0>	67 68 75
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<0>	67 68 75
FB_B_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<1>	67 68 75
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<1>	67 68 75
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<1..0>	67 68 75
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<11..6>	67 68 75
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_BA<2..0>	67 68 75
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_RAS_L	67 68 75
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_CAS_L	67 68 75
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_WE_L	67 68 75
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_CKE	67 68 75
FB_AB_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_A_CS0_L	67 68
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_DRAM_RST	67 68 75
FB_A_CMD	GDDR3_46SE	GDDR3_CMD	FB_A_LMA<5..2>	67 68 75
FB_B_CMD	GDDR3_46SE	GDDR3_CMD	FB_A_UMA<5..2>	67 68 75
FB_A_WDQS0	GDDR3_46SE	GDDR3_DQS	FB_A_WDQS<0>	67 68 75
FB_A_WDQS1	GDDR3_46SE	GDDR3_DQS	FB_A_WDQS<1>	67 68 75
FB_A_WDQS2	GDDR3_46SE	GDDR3_DQS	FB_A_WDQS<2>	67 68 75
FB_A_WDQS3	GDDR3_46SE	GDDR3_DQS	FB_A_WDQS<3>	67 68 75
FB_A_RDQS0	GDDR3_46SE	GDDR3_DQS	FB_A_RDQS<0>	67 68 75
FB_A_RDQS1	GDDR3_46SE	GDDR3_DQS	FB_A_RDQS<1>	67 68 75
FB_A_RDQS2	GDDR3_46SE	GDDR3_DQS	FB_A_RDQS<2>	67 68 75
FB_A_RDQS3	GDDR3_46SE	GDDR3_DQS	FB_A_RDQS<3>	67 68 75
FB_A_DQ_BYTE0	GDDR3_46SE	GDDR3_DATA	FB_A_DQ<7..0>	67 68 75
FB_A_DQ_BYTE1	GDDR3_46SE	GDDR3_DATA	FB_A_DQ<15..8>	67 68 75
FB_A_DQ_BYTE2	GDDR3_46SE	GDDR3_DATA	FB_A_DQ<23..16>	67 68 75
FB_A_DQ_BYTE3	GDDR3_46SE	GDDR3_DATA	FB_A_DQ<31..24>	67 68 75
FB_A_DQM0	GDDR3_46SE	GDDR3_DATA	FB_A_DQM_L<0>	67 68 75
FB_A_DQM1	GDDR3_46SE	GDDR3_DATA	FB_A_DQM_L<1>	67 68 75
FB_A_DQM2	GDDR3_46SE	GDDR3_DATA	FB_A_DQM_L<2>	67 68 75
FB_A_DQM3	GDDR3_46SE	GDDR3_DATA	FB_A_DQM_L<3>	67 68 75
FB_B_WDQS0	GDDR3_46SE	GDDR3_DQS	FB_A_WDQS<4>	67 68 75
FB_B_WDQS1	GDDR3_46SE	GDDR3_DQS	FB_A_WDQS<5>	67 68 75
FB_B_WDQS2	GDDR3_46SE	GDDR3_DQS	FB_A_WDQS<6>	67 68 75
FB_B_WDQS3	GDDR3_46SE	GDDR3_DQS	FB_A_WDQS<7>	67 68 75
FB_B_RDQS0	GDDR3_46SE	GDDR3_DQS	FB_A_RDQS<4>	67 68 75
FB_B_RDQS1	GDDR3_46SE	GDDR3_DQS	FB_A_RDQS<5>	67 68 75
FB_B_RDQS2	GDDR3_46SE	GDDR3_DQS	FB_A_RDQS<6>	67 68 75
FB_B_RDQS3	GDDR3_46SE	GDDR3_DQS	FB_A_RDQS<7>	67 68 75
FB_B_DQ_BYTE0	GDDR3_46SE	GDDR3_DATA	FB_A_DQ<39..32>	67 68 75
FB_B_DQ_BYTE1	GDDR3_46SE	GDDR3_DATA	FB_A_DQ<47..40>	67 68 75
FB_B_DQ_BYTE2	GDDR3_46SE	GDDR3_DATA	FB_A_DQ<55..48>	67 68 75
FB_B_DQ_BYTE3	GDDR3_46SE	GDDR3_DATA	FB_A_DQ<63..56>	67 68 75
FB_B_DQM0	GDDR3_46SE	GDDR3_DATA	FB_A_DQM_L<4>	67 68 75
FB_B_DQM1	GDDR3_46SE	GDDR3_DATA	FB_A_DQM_L<5>	67 68 75
FB_B_DQM2	GDDR3_46SE	GDDR3_DATA	FB_A_DQM_L<6>	67 68 75
FB_B_DQM3	GDDR3_46SE	GDDR3_DATA	FB_A_DQM_L<7>	67 68 75

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_C_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<0>	67 69 76
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<0>	67 69 76
FB_D_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<1>	67 69 76
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<1>	67 69 76
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<1..0>	67 69 76
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<11..6>	67 69 76
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_BA<2..0>	67 69 76
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_RAS_L	67 69 76
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_CAS_L	67 69 76
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_WE_L	67 69 76
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_CKE	67 69 76
FB_CD_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_B_CS0_L	67 69
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_DRAM_RST	67 69 76
FB_C_CMD	GDDR3_46SE	GDDR3_CMD	FB_B_LMA<5..2>	67 69 76
FB_D_CMD	GDDR3_46SE	GDDR3_CMD	FB_B_UMA<5..2>	67 69 76
FB_C_WDQS0	GDDR3_46SE	GDDR3_DQS	FB_B_WDQS<0>	67 69 76
FB_C_WDQS1	GDDR3_46SE	GDDR3_DQS	FB_B_WDQS<1>	67 69 76
FB_C_WDQS2	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<2>	67 69 76
FB_C_WDQS3	GDDR3_46SE	GDDR3_DQS	FB_B_WDQS<3>	67 69 76
FB_C_RDQS0	GDDR3_46SE	GDDR3_DQS	FB_B_RDQS<0>	67 69 76
FB_C_RDQS1	GDDR3_46SE	GDDR3_DQS	FB_B_RDQS<1>	67 69 76
FB_C_RDQS2	GDDR3_46SE	GDDR3_DQS	FB_B_RDQS<2>	67 69 76
FB_C_RDQS3	GDDR3_46SE	GDDR3_DQS	FB_B_RDQS<3>	67 69 76
FB_C_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<7..0>	67 69 76
FB_C_DQ_BYTE1	GDDR3_46SE	GDDR3_DATA	FB_B_DQ<15..8>	67 69 76
FB_C_DQ_BYTE2	GDDR3_46SE	GDDR3_DATA	FB_B_DQ<23..16>	67 69 76
FB_C_DQ_BYTE3	GDDR3_46SE	GDDR3_DATA	FB_B_DQ<31..24>	67 69 76
FB_C_DQM0	GDDR3_46SE	GDDR3_DATA	FB_B_DQM_L<0>	67 69 76
FB_C_DQM1	GDDR3_46SE	GDDR3_DATA	FB_B_DQM_L<1>	67 69 76
FB_C_DQM2	GDDR3_46SE	GDDR3_DATA	FB_B_DQM_L<2>	67 69 76
FB_C_DQM3	GDDR3_46SE	GDDR3_DATA	FB_B_DQM_L<3>	67 69 76
FB_D_WDQS0	GDDR3_46SE	GDDR3_DQS	FB_B_WDQS<4>	67 69 76
FB_D_WDQS1	GDDR3_46SE	GDDR3_DQS	FB_B_WDQS<5>	67 69 76
FB_D_WDQS2	GDDR3_46SE	GDDR3_DQS	FB_B_WDQS<6>	67 69 76
FB_D_WDQS3	GDDR3_46SE	GDDR3_DQS	FB_B_WDQS<7>	67 69 76
FB_D_RDQS0	GDDR3_46SE	GDDR3_DQS	FB_B_RDQS<4>	67 69 76
FB_D_RDQS1	GDDR3_46SE	GDDR3_DQS	FB_B_RDQS<5>	67 69 76
FB_D_RDQS2	GDDR3_46SE	GDDR3_DQS	FB_B_RDQS<6>	67 69 76
FB_D_RDQS3	GDDR3_46SE	GDDR3_DQS	FB_B_RDQS<7>	67 69 76
FB_D_DQ_BYTE0	GDDR3_46SE	GDDR3_DATA	FB_B_DQ<39..32>	67 69 76
FB_D_DQ_BYTE1	GDDR3_46SE	GDDR3_DATA	FB_B_DQ<47..40>	67 69 76
FB_D_DQ_BYTE2	GDDR3_46SE	GDDR3_DATA	FB_B_DQ<55..48>	67 69 76
FB_D_DQ_BYTE3	GDDR3_46SE	GDDR3_DATA	FB_B_DQ<63..56>	67 69 76
FB_D_DQM0	GDDR3_46SE	GDDR3_DATA	FB_B_DQM_L<4>	67 69 76
FB_D_DQM1	GDDR3_46SE	GDDR3_DATA	FB_B_DQM_L<5>	67 69 76
FB_D_DQM2	GDDR3_46SE	GDDR3_DATA	FB_B_DQM_L<6>	67 69 76
FB_D_DQM3	GDDR3_46SE	GDDR3_DATA	FB_B_DQM_L<7>	67 69 76

G84M Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
(CK505_DOT96)	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M	30 71
CK505_CLK27MSS	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS	30 71
LVDS_L_CLK	LVDS_100D	LVDS	LVDS_L_CLK_P	72 74
	LVDS_100D	LVDS	LVDS_L_CLK_N	72 74
LVDS_L_DATA	LVDS_100D	LVDS	LVDS_L_DATA_P<2..0>	72 74
	LVDS_100D	LVDS	LVDS_L_DATA_N<2..0>	72 74
U127	LVDS_100D	LVDS	LVDS_L_DATA_P<3>	71 72
U126	LVDS_100D	LVDS	LVDS_L_DATA_N<3>	71 72
LVDS_U_CLK	LVDS_100D	LVDS	LVDS_U_CLK_P	72 74
	LVDS_100D	LVDS	LVDS_U_CLK_N	72 74
LVDS_U_DATA	LVDS_100D	LVDS	LVDS_U_DATA_P<2..0>	72 74
	LVDS_100D	LVDS	LVDS_U_DATA_N<2..0>	72 74
U128	LVDS_100D	LVDS	LVDS_U_DATA_P<3>	71 72
U129	LVDS_100D	LVDS	LVDS_U_DATA_N<3>	71 72
TMDS_CLK	TMDS_100D	TMDS	TMDS_CLK_P	72 78
TMDS_CLK	TMDS_100D	TMDS	TMDS_CLK_N	72 78
TMDS_DATA	TMDS_100D	TMDS	TMDS_DATA_P<5..0>	72 78
TMDS_DATA	TMDS_100D	TMDS	TMDS_DATA_N<5..0>	72 78
VGA_R_TV_C	VGA_50S	VGA	GPU_TV_C_VGA_R	71 78
VGA_G_TV_Y	VGA_50S	VGA	GPU_TV_Y_VGA_G	71 78
VGA_B_TV_COMP	VGA_50S	VGA	GPU_TV_COMP_VGA_B	71 78
	VGA_50S	VGA	GPU_VGA_R	71 72
	VGA_50S	VGA	GPU_VGA_G	71 72
	VGA_50S	VGA	GPU_VGA_B	71 72
	VGA_50S	VGA	GPU_TV_C	71 72
	VGA_50S	VGA	GPU_TV_Y	71 72
	VGA_50S	VGA	GPU_TV_COMP	71 72
VGA_SYNC	VGA_55S	VGA_SYNC	GPU_VGA_HSYNC	72 78
VGA_SYNC	VGA_55S	VGA_SYNC	GPU_VGA_VSYNC	72 78

GPU (G84M) Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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D	051-7413	11.0.0

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PP1V8_MEM	*	PWR_P2MM
MEM_CMD	PP1V8_MEM	*	PWR_P2MM
MEM_CTRL	PP1V8_MEM	*	PWR_P2MM
MEM_DATA	PP1V8_MEM	*	PWR_P2MM
MEM_DQS	PP1V8_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLINK_VREF	GND	*	GND_P2MM
CLK_MED	GND	*	GND_P2MM
CLK_PCIE	GND	*	GND_P2MM
DMI	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
DMI	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM
ENET_MDI	ENET_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_MED	FW_POWER	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_70D	BOTTOM			0.127 MM	6.35 MM		

Allow 0.1 mm necks for >0.1 mm lines between thru-hole SO-DIMM pins.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*			0.100 MM	2.54 MM		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D	ISL10			0.100 MM	2.54 MM		
MEM_85D	ISL4,ISL10			0.100 MM	2.54 MM		

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	BGA	100_DIFF_BGA
TMDS_100D	BGA	100_DIFF_BGA
SATA_100D	BGA	100_DIFF_BGA

M87 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
(PCIE_EXCARD)	PCIE_100D	PCIE	PCIE_EXCARD_R2D_P 34
(PCIE_EXCARD)	PCIE_100D	PCIE	PCIE_EXCARD_R2D_N 34
(PCIE_MINI)	PCIE_100D	PCIE	PCIE_MINI_R2D_P 34
(PCIE_MINI)	PCIE_100D	PCIE	PCIE_MINI_R2D_N 34
	ENET_100D	ENET_MDI	ENET_MDI_R_P<3..0>
	ENET_100D	ENET_MDI	ENET_MDI_R_N<3..0>
	ENET_100D	ENETCONN	ENETCONN_P<3..0> 37
	ENET_100D	ENETCONN	ENETCONN_N<3..0> 37
	FW_110D	FW_TP	FW_PORT0_TPA_FL_P 41
	FW_110D	FW_TP	FW_PORT0_TPA_FL_N 41
	FW_110D	FW_TP	FW_PORT0_TPB_FL_P 41
	FW_110D	FW_TP	FW_PORT0_TPB_FL_N 41
(SATA_A_R2D)	SATA_100D	SATA	SATA_A_R2D_UF_P 79
(SATA_A_R2D)	SATA_100D	SATA	SATA_A_R2D_UF_N 79
(SATA_A_D2R)	SATA_100D	SATA	SATA_A_D2R_UF_P 79
(SATA_A_D2R)	SATA_100D	SATA	SATA_A_D2R_UF_N 79
(USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_P 43
(USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_N 43
(USB_EXTA)	USB_90D	USB	USB2_RT_P 43
(USB_EXTA)	USB_90D	USB	USB2_RT_N 43
(USB_EXTD)	USB_90D	USB	USB_WWAN_F_P
(USB_EXTD)	USB_90D	USB	USB_WWAN_F_N
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(USB_CAMERA)	USB_90D	USB	USB_CAMERA_F_N 44
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	SENSE_1TO1_55S	SENSE	GFXIMVP6_VSEN_N 73
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	NBCOREISNS_P 50
	SENSE_1TO1_55S	SENSE	NBCOREISNS_N 50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8ISNS_P 50
	SENSE_1TO1_55S	SENSE	P1V8ISNS_N 50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V25ISNS_P 50
	SENSE_1TO1_55S	SENSE	P1V25ISNS_N 50
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	THERM_1TO1_55S	THERM	CPU_THERMD_N 10 51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P 51
	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N 51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P 51 71
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THERM_DIFFPAIR	THERM_1TO1_55S	THERM	RSFSTHMSNS_D_P 7 51
	THERM_1TO1_55S	THERM	RSFSTHMSNS_D_N 7 51
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	SENSE_1TO1_55S	SENSE	P1V8ISNS_R_N 50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_R_P 50
	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_R_N 50
	TMDS_100D	TMDS	TMDS_CLK_R_P 78
	TMDS_100D	TMDS	TMDS_CLK_R_N 78
	TMDS_100D	TMDS	TMDS_CLK_F_P 78
	TMDS_100D	TMDS	TMDS_CLK_F_N 78
	TMDS_100D	TMDS	TMDS_DATA_F_P<5..0> 78
	TMDS_100D	TMDS	TMDS_DATA_F_N<5..0> 78
(VGA_R_TV_Y)	VGA_50S	VGA	VGA_R 78
(VGA_G_TV_C)	VGA_50S	VGA	VGA_G 78
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(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_HSYNC_R 78
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_VSYNC_R 78
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_HSYNC 78
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_VSYNC 78
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		PP1V8_MEM	=PP1V8_S3M_MEM_B 8 32
		GND	GND
		ENET_POWER	
		SB_POWER	PP3V3_S5 8
		SB_POWER	PP3V3_S0 8 64
		SB_POWER	PP1V5_S0 8
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	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_N 50
		FW_POWER	

Project Specific Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE: NONE	SHT 88 OF 89	

M75 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	ISL2,ISL11	Y	0.250 MM	0.076 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.125 MM	0.125 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
46_OHM_SE	TOP,BOTTOM	Y	0.126 MM	0.126 MM			
46_OHM_SE	*	Y	0.100 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.131 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL9,ISL10	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL2,ISL11	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM
80_OHM_DIFF	ISL9,ISL10	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM
85_OHM_DIFF	ISL9,ISL10	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PCB Rule Definitions

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0

SCALE	SHT	OF
NONE	89	89