1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

M42B MLB SCHEMATIC

10/2/2007

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
C		536501	PRODUCTION RELEASED	10/02/07	?

EE DRIS:

RX-RAYMOND XU
DK-DINESH KUMAR
RC-RAY CHANG
MK-MARC KLINGELHOFER
LT-LAWRENCE TAN
LD-LINDA DUNN

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES °
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

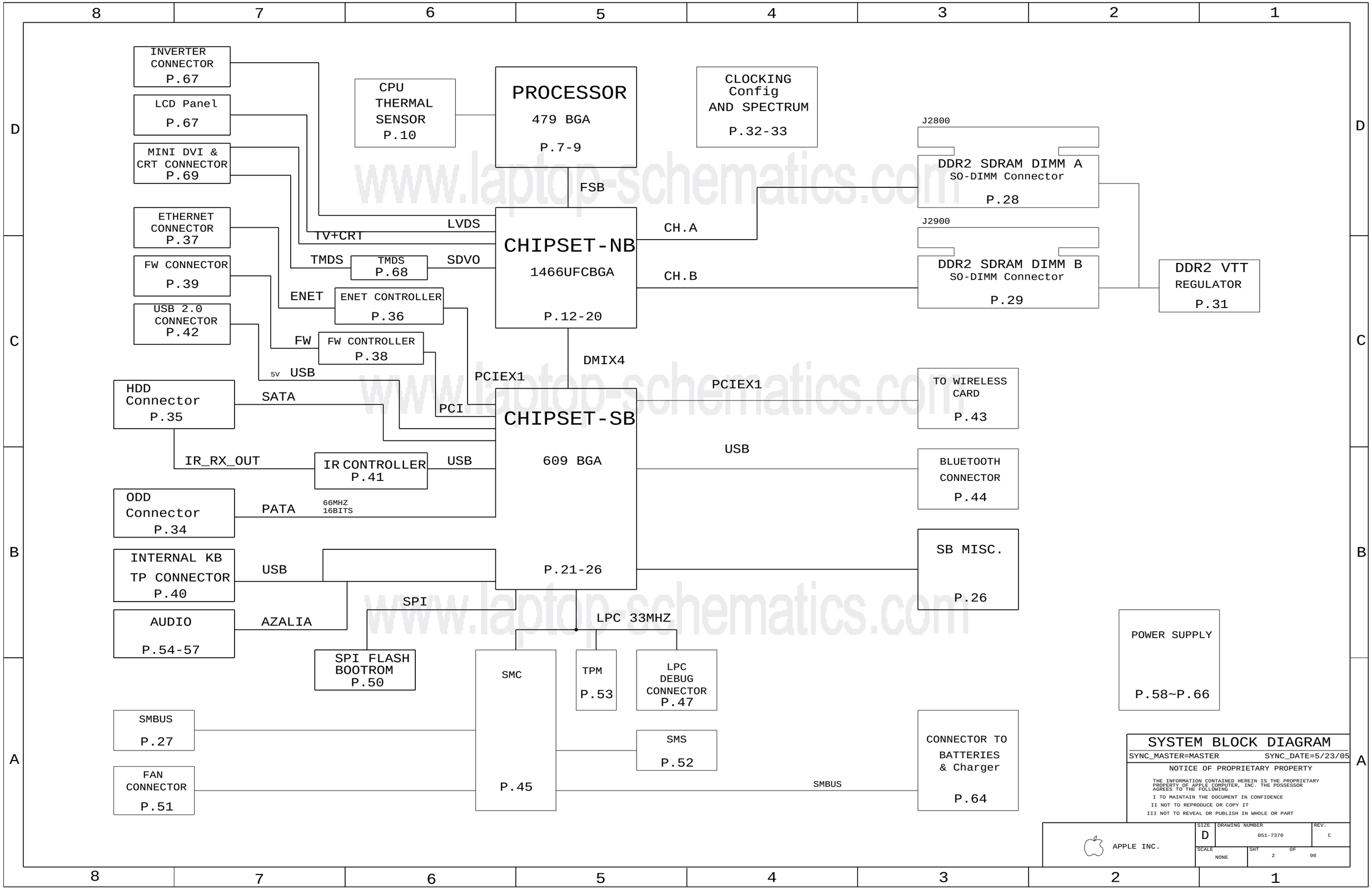
MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

APPLE INC.

TITLE
SCHEM,MLB,M42B

DRAWING NUMBER 051-7370
REV. C
SHT 1 OF 98



SYSTEM BLOCK DIAGRAM

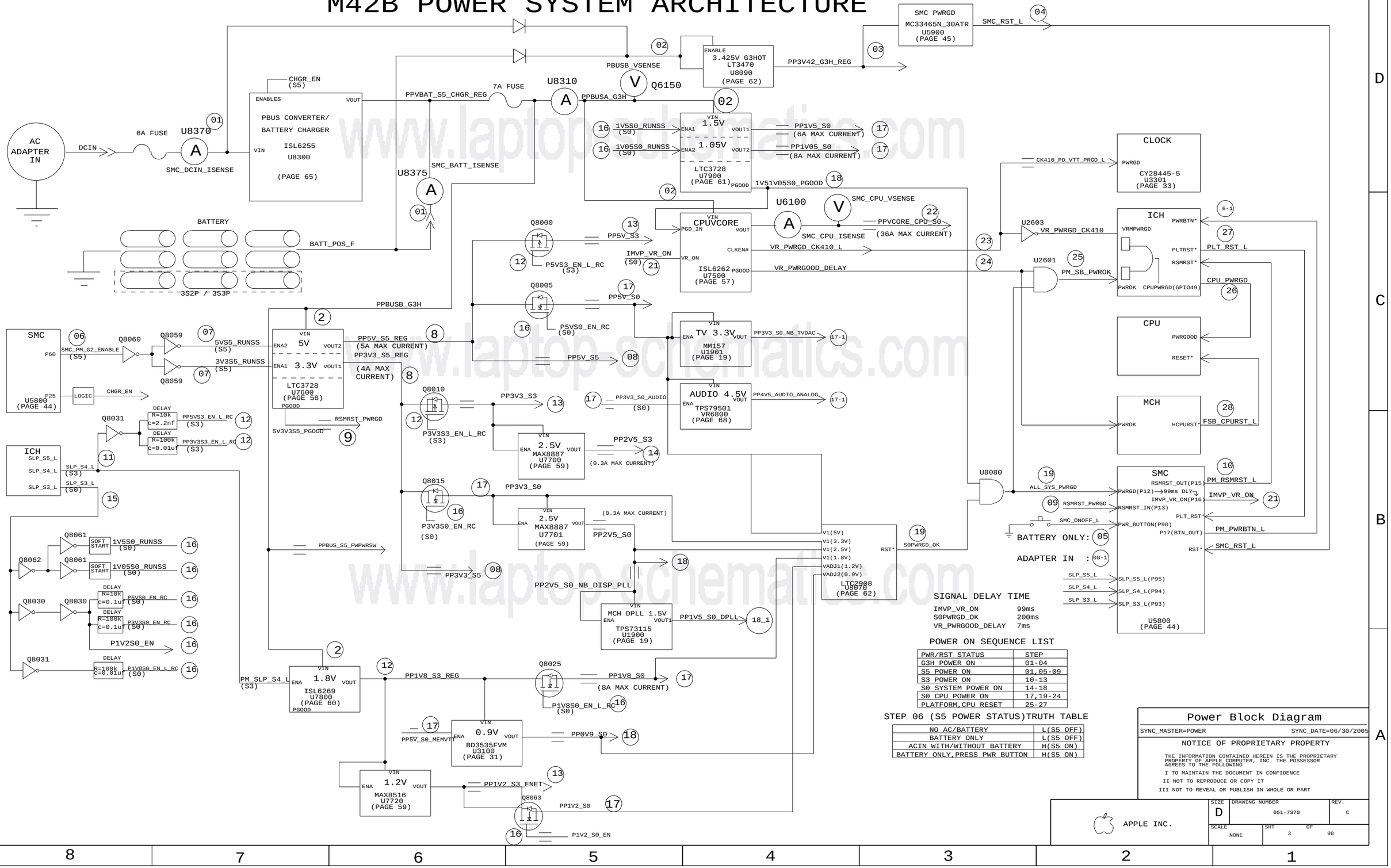
SYNC_MASTER=MASTER SYNC_DATE=5/23/05

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE	SHT	OF
NONE	2	98

M42B POWER SYSTEM ARCHITECTURE



Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

BOM OPTION

BOMOPTION	M42A GOOD ST MICRO 630-7795 EVT	M42A BETTER ST MICRO 630-7796 EVT	M42A BEST KIONIX 630-7799 EVT	M42A GOOD KIONIX 630-7798 EVT	M42A BETTER KIONIX 630-7736 EVT	M42A BEST ST MICRO 630-7797 EVT
1V51V05S0_CONT						
1V51V05S0_SKIP	V	V	V	V	V	V
5V3V3S3_CONT						
5V3V3S3_SKIP	V	V	V	V	V	V
ACCEL_KIONIX			V	V	V	
ACCEL_ST	V	V				V
INVERTER_BUF	V	V	V	V	V	V
INVERTER_UNBUF						
ITP						
LEMENU	V	V	V	V	V	V
MEMVTT_EN_PU	V	V	V	V	V	V
NBCFG_DMI_REVERSE						
NBCFG_DMI_X2						
NBCFG_DYN_ODT_DISABLE						
NBCFG_PEG_REVERSE						
NBCFG_SDVO_AND_PCIE						
NBCFG_VCC_1V5						
NO_REBOOT_MODE						
USB_C_OC_PU	V	V	V	V	V	V
USB_D_OC_PU	V	V	V	V	V	V
USB_E_OC_PU	V	V	V	V	V	V
GOOD	V			V		
BETTER		V			V	
BEST			V			V
M42A_PGM	V	V	V	V	V	V
ONEWIRE_PULLUP	V	V	V	V	V	V
ONEWIRE_PULLUP_OLD						
ONEWIRE_PU_PROT	V	V	V	V	V	V
ONEWIRE_PU_ACOK						
ONEWIRE_PWRCTL	V	V	V	V	V	V
ONEWIRE_ALWAYSON						
3V3_IND_2MM8	V	V	V	V	V	V
3V3_IND_3MM						
NORMAL	V	V		V	V	
FANCY			V			V
STANDOFF	V	V	V	V	V	V
FET_FDN6296	V	V	V	V	V	V
FET_STL8NH3LL						
GOOD-ST	V					
BETTER-ST		V				
BEST-KIONIX			V			
GOOD-KIONIX				V		
BETTER-KIONIX					V	
BEST-ST						V
TPM						
PVT-DIMM						
POST-RAMP-DIMM35	V	V	V	V	V	V
M42A	V	V	V	V	V	V
M42B	V	V	V	V	V	V

BOARD STACK-UP AND CONSTRUCTION

Top		SIGNAL
2		GROUND
3		SIGNAL(High Speed)
4		SIGNAL(High Speed)
5		GROUND
6		POWER
7		POWER
8		GROUND
9		SIGNAL(High Speed)
10		SIGNAL(High Speed)
11		GROUND
BOTTOM		SIGNAL

MLB STACKUP

LAYER	THICKNESS (MM)	TRACE WIDTH (MM)
CONFORMAL_COAT	0.018	
L1 SIGNAL(TOP)	0.047	0.1
L1-L2	0.07	
L2 GROUND	0.014	---
L2-L3	0.076	
L3 SIGNAL	0.014	0.079
L3-L4	0.156	
L4 SIGNAL	0.014	0.079
L4-L5	0.076	
L5 GND	0.014	---
L5-L6	0.07	
L6 POWER	0.031	---
L6-L7	0.076	
L7 POWER	0.031	---
L7-L8	0.07	
L8 GROUND	0.014	---
L8-L9	0.076	
L9 SIGNAL	0.014	0.1
L9-L10	0.156	
L10 SIGNAL	0.014	0.1
L10-L11	0.076	
L11 GROUND	0.014	0.1
L11-L12	0.07	
L12 SIGNAL(BOTTOM)	0.047	0.1
CONFORMAL_COAT	0.018	
TOTAL	1.276	---

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
337S3389	1	IC,MEROM,CPU 2.0GHZ,479 PGA	U0700	GOOD
337S3391	1	IC,MEROM,CPU 2.16GHZ,479 PGA	U0700	BETTER
337S3391	1	IC,MEROM,CPU 2.16GHZ,479 PGA	U0700	BEST

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S0268	1	IC,FW32306,1394A LINK,BGA,129P	U4400	LEMENU
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN, NO	U4101	LEMENU
359S0109	1	IC,SLG8LP436,CLOCK GEN,68PIN QFN	U3301	LEMENU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S2132	1	IC, 16MBIT 8-PIN SPI SERIAL FLASH,SOIC8	U6301	M42A_PGM
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U4102	M42A_PGM
341S2133	1	IC,SMC,176P BGA,HS8/2116	U5800	M42A_PGM
341S1890	1	IC,PSOC+W/USB,56P,MLF,CY8C24794	U5100	M42A_PGM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MMX6MM	EEE:YCN	CRITICAL	BEST-KIONIX
826-4393	1	LBL,P/N LABEL,PCB,28MMX6MM	EEE:YCM	CRITICAL	BETTER-KIONIX
826-4393	1	LBL,P/N LABEL,PCB,28MMX6MM	EEE:YCL	CRITICAL	GOOD-KIONIX

Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-7370	1	SCHEM,M42B,MLB	SCH	
820-2213	1	PCBF,M42B,MLB	PCB	

CONFIGURATION OPTIONS

SYNC_MASTER=SMC SYNC_DATE=07/18/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 4 OF 98	

Functional Test Points

Power Supply NO_TESTs

NO_TEST

I93		IMVP6_RBIAS	58A4 58B7
I94		IMVP6_COMP	58A4 58B7
I95		5VS5_RUNSS	59B4 63C7
I96		1V5S0_RUNSS	62B5 63B7
I101		1V8S3_COMP	61B6
I102		1V8S3_FSET	61C6
I103	TRUE	3V3S5_COMP	
I104	TRUE	3V3S5_FSET	
I106	TRUE	1V05S0_COMP	
I105	TRUE	1V05S0_FSET	
I107	TRUE	P3V42G3H_FB	63D2

CLOCK NO_TESTS

NO_TEST

I111	TRUE	CK410_CPU0_N	32C4 33D5
I112	TRUE	CK410_CPU0_P	32C4 33D5
I113	TRUE	CK410_CPU1_N	32C4 33D5
I114	TRUE	CK410_CPU1_P	32C4 33D5
I115	TRUE	CK410_CPU2_ITP_SRC10_N	32C4 33D5
I116	TRUE	CK410_CPU2_ITP_SRC10_P	32C4 33D5
I117	TRUE	CK410_DOT96_27M_N	32A4 33B5
I118	TRUE	CK410_DOT96_27M_P	32A4 33B5
I119	TRUE	CK410_LVDS_N	32B4 33A5
I120	TRUE	CK410_LVDS_P	32B4 33A5
I122	TRUE	CK410_PCI4_CLK_SPN	
I122	TRUE	CK410_PCIF1_CLK	32B6 33D8
I123	TRUE	CK410_SRC1_N_SPN	6B3
I122	TRUE	CK410_SRC1_P_SPN	6B3
I123	TRUE	CK410_SRC2_N	32B4 33C5
I183	TRUE	CK410_SRC2_P	32B4 33C5
I184	TRUE	CK410_SRC3_N_SPN	6B3
I185	TRUE	CK410_SRC3_P_SPN	6B3
I186	TRUE	CK410_SRC4_N	32B4 33B5
I187	TRUE	CK410_SRC4_P	32B4 33B5
I188	TRUE	CK410_SRC5_N	32B4 33C5
I189	TRUE	CK410_SRC5_P	32B4 33C5
I190	TRUE	CK410_SRC6_N	32B4 33C5
I191	TRUE	CK410_SRC6_P	32B4 33D5
I192	TRUE	CK410_SRC7_N_SPN	6B3
I193	TRUE	CK410_SRC7_P_SPN	6B3
I194	TRUE	CK410_SRC8_N	32A4 33C5
I195	TRUE	CK410_SRC8_P	32A4 33C5
I196	TRUE	CK410_SRC_CLKREQ1_L_SPN	6B3
I197	TRUE	CK410_SRC_CLKREQ3_L_SPN	6B3
I198	TRUE	CK410_SRC_CLKREQ8_L	32A4 33A5

FIREWARE NO_TESTS

NO_TEST

I199	TRUE	FW_B_TPA_N_SPN	6D1
I200	TRUE	FW_B_TPA_P_SPN	6D1
I201	TRUE	FW_B_TPBIAS_SPN	6D1
I202	TRUE	FW_B_TPB_N_SPN	6D1
I203	TRUE	FW_B_TPB_P_SPN	6D1
I204	TRUE	FW_C_TPA_N_SPN	6D1
I205	TRUE	FW_C_TPA_P_SPN	6D1
I206	TRUE	FW_C_TPBIAS_SPN	6D1
I207	TRUE	FW_C_TPB_N_SPN	6D1
I208	TRUE	FW_C_TPB_P_SPN	6D1

LVDS NO_TESTS

NO_TEST

I209	TRUE	LVDS_B_CLK_N_SPN	6D5
I210	TRUE	LVDS_B_CLK_P_SPN	6D5
I211	TRUE	LVDS_B_DATA_N0_SPN	6D5
I212	TRUE	LVDS_B_DATA_N1_SPN	6D5
I213	TRUE	LVDS_B_DATA_N2_SPN	6D5
I214	TRUE	LVDS_B_DATA_P1_SPN	6D5
I215	TRUE	LVDS_B_DATA_P2_SPN	6D5

ETHERNET NO_TESTS

NO_TEST

I216	TRUE	ENET_MDI_TRAN_P<2>	37B5
I217	TRUE	ENET_MDI_TRAN_N<2>	37B5
I218	TRUE	ENET_MDI_TRAN_P<3>	37B5

NO_TEST

I219	TRUE	SMC_FAN_3_TACH	45B8 46C3
I220	TRUE	ALS_LEFT	45A8 46C3

Fan Connectors

FUNC_TEST

I12	TRUE	=PP5V_S0_FAN_RT	51C4 64D3
I15	TRUE	FAN_RT_PWM	51B3
I16	TRUE	FAN_RT_TACH	51C3
I17	TRUE	=PP3V3_S0_FAN_RT	51C4 64A6
I150	TRUE	SMC_FAN_1_CTL	45B8 51B4
I149	TRUE	SMC_FAN_1_TACH	45B8 51C4

LPC+ Debug Connector

FUNC_TEST

I20	TRUE	=PP3V42_G3H_LPCPLUS	47C6 64D1
I19	TRUE	=PP5V_S0_LPCPLUS	47C6 64D3
I18	TRUE	LPC_AD<0>	21D4 45D8 47C6 53C6
I17	TRUE	LPC_AD<1>	21D4 45D8 47C6 53C6
I71	TRUE	LPC_FRAME_L	21C5 45C8 47C6 53C6
I72	TRUE	PM_CLKRUN_L	23C8 38A5 45D5 47C6 53C6
I73	TRUE	BOOT_LPC_SPI_L	22B3 45C8 47C6
I74	TRUE	SMC_TMS	45B5 46C6 47C6
I75	TRUE	DEBUG_RST_L	26B1 47C6
I76	TRUE	SMC_TRST_L	45C1 47C6
I77	TRUE	SMC_TDO	45C5 46C6 47B6
I78	TRUE	SMC_MD1	45C2 47B6
I79	TRUE	SMC_TX_L	45C8 46B2 46D6 47B6
I80	TRUE	FWH_INIT_L	6B2 21C4 47C5
I81	TRUE	PCI_CLK_PORT80_LPC	33D6 47C5
I82	TRUE	LPC_AD<2>	21D4 45D8 47C5 53C6
I83	TRUE	LPC_AD<3>	21D4 45D8 47C5 53C6
I84	TRUE	INT_SERIRQ	23C8 45C8 47C5 53C6
I85	TRUE	PM_SUS_STAT_L	23C5 45D5 46D3 47C5 53C6
I86	TRUE	SMC_TDI	45C5 46C6 47C5
I87	TRUE	SMC_TCK	45C5 46C6 47C5
I88	TRUE	SMC_RST_L	45C3 46D7 47C5
I89	TRUE	SMC_NMI	45C1 47B5
I91	TRUE	SMC_RX_L	45C8 46B2 46D6 47B5
I90	TRUE	SV_SET_UP	23B6 23C3 47B5

Other Func Test Points

FUNC_TEST

I62	TRUE	=PP1V05_S0_REG	62B1 64D8

SMBus FUNC_TEST

I182

	TRUE	SMBUS_SMC_MLB_SCL	27C5
I183	TRUE	SMBUS_SMC_MLB_SDA	27B5

FIREWIRE FUNC_TEST

I192	TRUE	PPFW_SWITCH	39D4

SLEEP LED FUNC_TEST

I155	TRUE	SYS_LED_ANODE	35C5 46A3

SMC FUNC_TEST

I145	TRUE	SMC_LID	40C4 45B5 46C6 65A8
I146	TRUE	SMC_MANUAL_RST_L	46D8
I156	TRUE	SMC_CPU_VSENSE	45D5 48B1

Power Supply FUNC_TEST

I160	TRUE	ALL_SYS_PWRGD	26A5 45D8 63B1
I161	TRUE	PPVCORE_CPU_S0	64D7
I162	TRUE	PP1V05_S0	64D7
I163	TRUE	PP1V5_S0	64C7
I164	TRUE	PP1V8_S0	64C7
I165	TRUE	PP2V5_S0	64B7
I166	TRUE	PP3V3_S0	64B7
I167	TRUE	PP5V_S0	64D4
I168	TRUE	PP1V2_S3	64C4
I169	TRUE	PP1V8_S3	64C4
I170	TRUE	PP2V5_S3	64C4
I172	TRUE	PP3V3_S3	64B4
I171	TRUE	PP5V_S3	64B4
I177	TRUE	PP3V3_S5	64A4
I178	TRUE	PP5V_S5	64A4
I176	TRUE	PP3V42_G3H	64D1
I174	TRUE	PPBUSA_G3H	
I175	TRUE	PPBUSB_G3H	64C1
I179	TRUE	PP18V5_G3H	64C1
I181	TRUE	PP0V9_S0	64D7

Battery Digital Connector

FUNC_TEST

I1	TRUE	SMC_BS_ALRT_L	45C5 46C6 65A2
I3	TRUE	SMBUS_BATT_SCL_F	65B6
I4	TRUE	SMBUS_BATT_SDA_F	65A6
I2	TRUE	BATT_IN	
I177	TRUE	BATT_POS	65A6
I160	TRUE	BATT_NEG	65A6

Audio FUNC_TEST

I9	TRUE	PP5V_S0_AUDIO_PWR	
I11	TRUE	PP5V_S0_AUDIO	
I10	TRUE	GND_AUDIO_PWR	64B2
I21	TRUE	GND_AUDIO_CODEC	64B2
I22	TRUE	ACZ_SDATAIN<0>	21C7 54D7
I24	TRUE	ACZ_SDATAOUT	21C7 54D7
I23	TRUE	ACZ_BITCLK	21C7 54D7
I26	TRUE	ACZ_RST_L	21C7 54C7 57C3
I25	TRUE	ACZ_SYNC	21C7 54D7

Battery FUNC_TEST

I29	TRUE	SMC_BATT_ISET	45B5 66B7
I32	TRUE	SMC_BATT_CHG_EN	45D8 46B6 66A4
I31	TRUE	SMC_BC_ACOK	45C5 46B6 65C3 65C7 66A5
I33	TRUE	SMC_PS_ON	39C6 45D5 46B3 65C3
I36	TRUE	SMC_BATT_TRICKLE_EN_L	45D8 46B6 66A3
I38	TRUE	SYS_ONEWIRE	45B8 46D6 65C8

USB FUNC_TEST

I44	TRUE	TP_USBP_E	6C2
I47	TRUE	TP_USBN_E	6C2
I46	TRUE	TP_USBP_F	
I48	TRUE	TP_USBN_F	

DC-JACK FUNC_TEST

I57	TRUE	ACIN_ENABLE_GATE	65C3

Battery charger FUNC_TEST

I58	TRUE	PPVBAT_G3H_CHGR_OUT	66B5 66C2

INVERTER CONNECTOR FUNC_TEST

I60	TRUE	PPBUS_ALL_INV_CONN	67D3
I59	TRUE	INV_GND	67D2
I61	TRUE	PP5V_INV_F	67D3
I63	TRUE	INV_BKLIGHT_PWM_L	67D2

FUNC TEST 1 OF 2

APPLE INC.	SIZE D	DRAWING NUMBER 051-7370	REV. C
	SCALE NONE	SHT 5 OF 98	

(EMI PAD FOR INVERTER GONNECTOR)

67C2 INVT_CHGND — 1 — ZS0620 EMI-SPRING CLIP-SM-M42

SPKR-MIC-CLIP-M42

NC — 1 — ZS0621 SM

CHASSIS GND

BATTERY,AUDIO,DIP DIMM CONNECTOR CHASSIS GND

GND_CHASSIS_IO 6C7 — OMIT Z0606 5R2P3-7SQB

65A6 =GND_BATT_CHGND
56B8 =GND_CHASSIS_AUDIO_JACK
=GND_CHASSIS_AUDIO_SPKRCONN
57A6 =GND_CHASSIS_AUDIO_MIC
=GND_CHASSIS_AUDIO_SHIELD1
=GND_CHASSIS_AUDIO_SHIELD2
=GND_CHASSIS_AUDIO_SHIELD3
28A5 =GND_CHASSIS_DIPDIMM_LEFT

SATA,LVDS CONNECTOR CHASSIS GND

GND_CHASSIS_SATA 35C8 — OMIT Z0607 6P5R2P6-5P5B
VOLTAGE=0V MAKE_BASE=TRUE

67B2 67A2 =GND_CHASSIS_LVDS

C0607 0.1UF 10% 16V X5R 402
C0608 0.01UF 10% 16V CERM 402

DCIN CONNECTOR CHASSIS GND

GND_CHASSIS_DCIN — OMIT Z0602 5R2P3-7SQB
VOLTAGE=0V MAKE_BASE=TRUE

65C8 =GND_DCIN_CHGND
37A4 =GND_CHASSIS_RJ45
69C3 69A4 =GND_CHASSIS_TMDS_UPPER

C0630 0.1UF 10% 16V X5R 402

I/O CONNECTOR CHASSIS GND

GND_CHASSIS_IO 607 — OMIT Z0608 5P0R2P3-7BLB
VOLTAGE=0V MAKE_BASE=TRUE

39A1 =GND_CHASSIS_FW_DOWN
42C4 42C2 42A4 42A2 =GND_CHASSIS_USB

C0610 0.1UF 10% 16V X5R 402
C0611 0.01UF 10% 16V CERM 402

DIP DIMM CONNECTOR CHASSIS GND

GND_CHASSIS_CENTER — OMIT Z0610 5R2P3-7SQB
VOLTAGE=0V MAKE_BASE=TRUE

29A5 28D5 =GND_CHASSIS_DIPDIMM_CENTER

C0616 0.1UF 10% 16V X5R 402
C0617 0.01UF 10% 16V CERM 402

DIP DIMM CONNECTOR CHASSIS GND

GND_CHASSIS_RIGHT — OMIT Z0609 5R2P3-7SQB
VOLTAGE=0V MAKE_BASE=TRUE

29D4 =GND_CHASSIS_DIPDIMM_RIGHT

C0614 0.1UF 10% 16V X5R 402
C0615 0.01UF 10% 16V CERM 402

OMIT Z0601 5R2P3-7SQB — GND_CHASSIS_CPU

C0612 0.1UF 10% 16V X5R 402
C0613 0.01UF 10% 16V CERM 402

OMIT Z0611 5R2P3-7B — GND_CHASSIS_FANSCREW

C0618 0.1UF 10% 16V X5R 402
C0619 0.01UF 10% 16V CERM 402

DIGITAL GND SCREW HOLE OMIT

OMIT Z0603 STDOFF-4.5OD3.95H-1.1-3.7-TH1 — NB_RIGHT_DOWN_SCREW
R0612 0 5% 1/16W MF-LF 402

OMIT Z0604 STDOFF-4.5OD3.95H-1.1-3.7-TH1 — CPU_THERMAL_SCREW_UP
R0610 0 5% 1/16W MF-LF 402

OMIT Z0605 STDOFF-4.5OD3.95H-1.1-3.7-TH1 — CPU_THERMAL_SCREW_DOWN
R0611 0 5% 1/16W MF-LF 402

OMIT Z0621 STDOFF-4.5OD3.95H-1.1-3.7-TH1 — CPU_THERMAL_SCREW_RIGHT
R0621 0 5% 1/16W MF-LF 402

LVDS ALIASES

NO-CONNECT UNUSED LVDS INTERFACE PORTS

13C5	LVDS_B_CLK_N	LVDS_B_CLK_N_SPN	5A7
13C5	LVDS_B_CLK_P	LVDS_B_CLK_P_SPN	MAKE_BASE=TRUE 5A7
13C5	LVDS_B_DATA_N<0>	LVDS_B_DATA_N0_SPN	MAKE_BASE=TRUE 5A7
13C5	LVDS_B_DATA_N<1>	LVDS_B_DATA_N1_SPN	MAKE_BASE=TRUE 5A7
13C5	LVDS_B_DATA_N<2>	LVDS_B_DATA_N2_SPN	MAKE_BASE=TRUE 5A7
13C5	LVDS_B_DATA_P<0>	LVDS_B_DATA_P0_SPN	MAKE_BASE=TRUE 5A7
13C5	LVDS_B_DATA_P<1>	LVDS_B_DATA_P1_SPN	MAKE_BASE=TRUE 5A7
13C5	LVDS_B_DATA_P<2>	LVDS_B_DATA_P2_SPN	MAKE_BASE=TRUE 5A7 MAKE_BASE=TRUE

PCI_EXPRESS GRAPHICS ALIASES

NO-CONNECT UNUSED SDVO INTERFACE PORTS

13D3	PEG_D2R_N<0>	PEG_D2R_N0_SPN	MAKE_BASE=TRUE
13D3	PEG_D2R_N<2>	PEG_D2R_N2_SPN	MAKE_BASE=TRUE
13D3	PEG_D2R_N<3>	PEG_D2R_N3_SPN	MAKE_BASE=TRUE
13D3	PEG_D2R_N<4>	PEG_D2R_N4_SPN	MAKE_BASE=TRUE
13D3	PEG_D2R_N<5>	PEG_D2R_N5_SPN	MAKE_BASE=TRUE
13D3	PEG_D2R_N<6>	PEG_D2R_N6_SPN	MAKE_BASE=TRUE
13D3	PEG_D2R_N<7>	PEG_D2R_N7_SPN	MAKE_BASE=TRUE
13D3	PEG_D2R_N<8>	PEG_D2R_N8_SPN	MAKE_BASE=TRUE
13D3	PEG_D2R_N<9>	PEG_D2R_N9_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_N<10>	PEG_D2R_N10_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_N<11>	PEG_D2R_N11_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_N<12>	PEG_D2R_N12_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_N<13>	PEG_D2R_N13_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_N<14>	PEG_D2R_N14_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_N<15>	PEG_D2R_N15_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<0>	PEG_D2R_P0_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<2>	PEG_D2R_P2_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<3>	PEG_D2R_P3_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<4>	PEG_D2R_P4_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<5>	PEG_D2R_P5_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<6>	PEG_D2R_P6_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<7>	PEG_D2R_P7_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<8>	PEG_D2R_P8_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<9>	PEG_D2R_P9_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<10>	PEG_D2R_P10_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<11>	PEG_D2R_P11_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<12>	PEG_D2R_P12_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<13>	PEG_D2R_P13_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<14>	PEG_D2R_P14_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<15>	PEG_D2R_P15_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<4>	PEG_R2D_C_N4_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<5>	PEG_R2D_C_N5_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<6>	PEG_R2D_C_N6_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<7>	PEG_R2D_C_N7_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<8>	PEG_R2D_C_N8_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<9>	PEG_R2D_C_N9_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<10>	PEG_R2D_C_N10_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<11>	PEG_R2D_C_N11_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<12>	PEG_R2D_C_N12_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<13>	PEG_R2D_C_N13_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<14>	PEG_R2D_C_N14_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<15>	PEG_R2D_C_N15_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_P<4>	PEG_R2D_C_P4_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_P<5>	PEG_R2D_C_P5_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_P<6>	PEG_R2D_C_P6_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_P<7>	PEG_R2D_C_P7_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_P<8>	PEG_R2D_C_P8_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_P<9>	PEG_R2D_C_P9_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_P<10>	PEG_R2D_C_P10_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_P<11>	PEG_R2D_C_P11_SPN	MAKE_BASE=TRUE
13A3	PEG_R2D_C_P<12>	PEG_R2D_C_P12_SPN	MAKE_BASE=TRUE
13A3	PEG_R2D_C_P<13>	PEG_R2D_C_P13_SPN	MAKE_BASE=TRUE
13A3	PEG_R2D_C_P<14>	PEG_R2D_C_P14_SPN	MAKE_BASE=TRUE
13A3	PEG_R2D_C_P<15>	PEG_R2D_C_P15_SPN	MAKE_BASE=TRUE

69A3 =GND_CHASSIS_TMDS_DOWN
39A1 =GND_CHASSIS_FW_UPPER
I393
GND_CHASSIS_IO1 — VOLTAGE=0V MAKE_BASE=TRUE

OMIT Z0612 STDOFF-4.2OD2.15H-1.2-TH — NC

OMIT Z0613 STDOFF-4.2OD2.15H-1.2-TH — NC

NB CFG ALIASES

NO-CONNECT UNUSED CFG INTERFACE PORTS

14C6	NB_CFG<3>	TP_NB_CFG3	
14C6	NB_CFG<4>	TP_NB_CFG4	MAKE_BASE=TRUE
14C6	NB_CFG<6>	TP_NB_CFG6	MAKE_BASE=TRUE
14C6	NB_CFG<8>	TP_NB_CFG8	MAKE_BASE=TRUE
14C6	NB_CFG<10>	TP_NB_CFG10	MAKE_BASE=TRUE
14C6	NB_CFG<11>	TP_NB_CFG11	MAKE_BASE=TRUE
14C6	NB_CFG<12>	TP_NB_CFG12	MAKE_BASE=TRUE
14C6	NB_CFG<13>	TP_NB_CFG13	MAKE_BASE=TRUE
14C6	NB_CFG<14>	TP_NB_CFG14	MAKE_BASE=TRUE
14C6	NB_CFG<15>	TP_NB_CFG15	MAKE_BASE=TRUE
14C6	NB_CFG<17>	TP_NB_CFG17	MAKE_BASE=TRUE MAKE_BASE=TRUE

SATA ALIASES

NO-CONNECT UNUSED SATA INTERFACE PORTS

21B6	SATA_A_D2R_N	SATA_A_D2R_N_SPN	MAKE_BASE=TRUE
21B6	SATA_A_D2R_P	SATA_A_D2R_P_SPN	MAKE_BASE=TRUE
21B6	SATA_A_R2D_C_N	SATA_A_R2D_C_N_SPN	MAKE_BASE=TRUE
21B6	SATA_A_R2D_C_P	SATA_A_R2D_C_P_SPN	MAKE_BASE=TRUE MAKE_BASE=TRUE

PCI_EXP ALIASES

NO-CONNECT UNUSED PCI_EXP INTERFACE PORTS

22D4	PCIE_C_D2R_N	PCIE_C_D2R_N_SPN	
22D4	PCIE_C_D2R_P	PCIE_C_D2R_P_SPN	MAKE_BASE=TRUE
22D4	PCIE_C_R2D_C_N	PCIE_C_R2D_C_N_SPN	MAKE_BASE=TRUE
22D4	PCIE_C_R2D_C_P	PCIE_C_R2D_C_P_SPN	MAKE_BASE=TRUE
22D4	PCIE_D_D2R_N	PCIE_D_D2R_N_SPN	MAKE_BASE=TRUE
22D4	PCIE_D_D2R_P	PCIE_D_D2R_P_SPN	MAKE_BASE=TRUE
22D4	PCIE_D_R2D_C_N	PCIE_D_R2D_C_N_SPN	MAKE_BASE=TRUE
22D4	PCIE_D_R2D_C_P	PCIE_D_R2D_C_P_SPN	MAKE_BASE=TRUE
22C4	PCIE_E_D2R_N	PCIE_E_D2R_N_SPN	MAKE_BASE=TRUE
22C4	PCIE_E_D2R_P	PCIE_E_D2R_P_SPN	MAKE_BASE=TRUE
22C4	PCIE_E_R2D_C_N	PCIE_E_R2D_C_N_SPN	MAKE_BASE=TRUE
22C4	PCIE_E_R2D_C_P	PCIE_E_R2D_C_P_SPN	MAKE_BASE=TRUE
22C4	PCIE_F_D2R_N	PCIE_F_D2R_N_SPN	MAKE_BASE=TRUE
22C4	PCIE_F_D2R_P	PCIE_F_D2R_P_SPN	MAKE_BASE=TRUE
22C4	PCIE_F_R2D_C_N	PCIE_F_R2D_C_N_SPN	MAKE_BASE=TRUE
22C4	PCIE_F_R2D_C_P	PCIE_F_R2D_C_P_SPN	MAKE_BASE=TRUE MAKE_BASE=TRUE

CLOCK ALIASES

NO-CONNECT UNUSED CLOCK INTERFACE PORTS

32B4	CK410_SRC1_N	CK410_SRC1_N_SPN	5C7
32B4	CK410_SRC1_P	CK410_SRC1_P_SPN	MAKE_BASE=TRUE 5C7
32B4	CK410_SRC3_N	CK410_SRC3_N_SPN	MAKE_BASE=TRUE 5C7
32B4	CK410_SRC3_P	CK410_SRC3_P_SPN	MAKE_BASE=TRUE 5C7
32B4	CK410_SRC7_N	CK410_SRC7_N_SPN	MAKE_BASE=TRUE 5C7
32B4	CK410_SRC7_P	CK410_SRC7_P_SPN	MAKE_BASE=TRUE 5C7
32B4	CK410_SRC_CLKREQ1_L	CK410_SRC_CLKREQ1_L_SPN	MAKE_BASE=TRUE 5B7
32B4	CK410_SRC_CLKREQ3_L	CK410_SRC_CLKREQ3_L_SPN	MAKE_BASE=TRUE 5B7 MAKE_BASE=TRUE

SB ALIASES

NO-CONNECT UNUSED CLOCK INTERFACE PORTS

23C3	SUS_CLK_SB	SUS_CLK_SB_SPN	MAKE_BASE=TRUE

SO-DIMM ALIASES

NO-CONNECT UNUSED ADDRESS INTERFACE PORTS

28C4	MEM_A_A<15>	MEM_A_A15_SPN	
28C4	MEM_A_A<14>	MEM_A_A14_SPN	MAKE_BASE=TRUE
29C4	MEM_B_A<15>	MEM_B_A15_SPN	MAKE_BASE=TRUE
29C4	MEM_B_A<14>	MEM_B_A14_SPN	MAKE_BASE=TRUE MAKE_BASE=TRUE

Ethernet ALIASES

36C8	ENET_CTRL12	ENET_CTRL12_SPN	
36C8	ENET_CTRL25	ENET_CTRL25_SPN	MAKE_BASE=TRUE MAKE_BASE=TRUE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
860-0722	4	THERMAL STANDOFF	Z0603,Z0604,Z0605,Z0621	STANDOFF
860-0723	1	STANDOFF WIRELESS	Z0612	STANDOFF
860-0749	1	STANDOFF W/THRU HOLES,WIRELESS	Z0613	STANDOFF

FIREWIRE ALIASES

NO-CONNECT UNUSED FIREWIRE INTERFACE PORTS

38B3	FW_B_TPBIAS	FW_B_TPBIAS_SPN	5B7
38B3	FW_B_TPA_P	FW_B_TPA_P_SPN	MAKE_BASE=TRUE 5B7
38B3	FW_B_TPA_N	FW_B_TPA_N_SPN	MAKE_BASE=TRUE 5B7
38B3	FW_B_TPB_P	FW_B_TPB_P_SPN	MAKE_BASE=TRUE 5B7
38B3	FW_B_TPB_N	FW_B_TPB_N_SPN	MAKE_BASE=TRUE 5B7
38B3	FW_C_TPBIAS	FW_C_TPBIAS_SPN	MAKE_BASE=TRUE 5B7
38B3	FW_C_TPA_P	FW_C_TPA_P_SPN	MAKE_BASE=TRUE 5B7
38B3	FW_C_TPA_N	FW_C_TPA_N_SPN	MAKE_BASE=TRUE 5B7
38B3	FW_C_TPB_P	FW_C_TPB_P_SPN	MAKE_BASE=TRUE 5B7
38B3	FW_C_TPB_N	FW_C_TPB_N_SPN	MAKE_BASE=TRUE 5B7 MAKE_BASE=TRUE

39C6 =FWPWR_PWRON — NC_FWPWR_PWRON
NO_TEST=TRUE MAKE_BASE=TRUE

USB PORT A = External USB2.0 Port

42C5	=USB2_EXTA_P	USB2_EXTA_P	USB_A_P	22C2
42C5	=USB2_EXTA_N	MAKE_BASE=TRUE USB2_EXTA_N	MAKE_BASE=TRUE USB_A_N	22C2
42C8	=EXTAUSB_OC_L	MAKE_BASE=TRUE EXTAUSB_OC_L	MAKE_BASE=TRUE USB_A_OC_L	22C4 22D8

USB PORT B = Trackpad(Geyser)

40C7	=USB2_GEYSER_P	USB2_GEYSER_P	USB_B_P	22C2
40C7	=USB2_GEYSER_N	MAKE_BASE=TRUE USB2_GEYSER_N	MAKE_BASE=TRUE USB_B_N	22C2

USB PORT C = External USB2.0 Port B

42B5	=USB2_EXTB_P	USB2_EXTB_P	USB_C_P	22C2
42B5	=USB2_EXTB_N	MAKE_BASE=TRUE USB2_EXTB_N	MAKE_BASE=TRUE USB_C_N	22C2
42C8	=EXTBUSB_OC_L	MAKE_BASE=TRUE EXTBUSB_OC_L	MAKE_BASE=TRUE USB_C_OC_L	22C4 22D8

USB PORT D = CAMERA

67B4	=USB2_CAMERA_P	USB2_CAMERA_P	USB_D_P	22C2
67A4	=USB2_CAMERA_N	MAKE_BASE=TRUE USB2_CAMERA_N	MAKE_BASE=TRUE USB_D_N	22C2

USB PORT "E" = Unused

5C1	TP_USBP_E		USB_E_P	22C2
5C1	TP_USBN_E	MAKE_BASE=TRUE	USB_E_N	22C2

USB PORT "F" = IR CONTROLLER

41C6	=USB2_IR_P	USB_IR_P	USB_F_P	22C2
41C6	=USB2_IR_N	USB_IR_N	MAKE_BASE=TRUE USB_F_N	22C2

USB PORT "G" = BLUETOOTH

44C6	=USB2_BT_P	USB_BT_P	USB_G_P	22C2
44C6	=USB2_BT_N	MAKE_BASE=TRUE USB_BT_N	MAKE_BASE=TRUE USB_G_N	22C2

USB PORT "H" = PCI-E Mini Card

43B4	=USB2_AIRPORT_P	USB2_AIRPORT_P	USB_H_P	22C2
43B4	=USB2_AIRPORT_N	MAKE_BASE=TRUE USB2_AIRPORT_N	MAKE_BASE=TRUE USB_H_N	22C2

ANALOG SWITCH GPIO

69A6 =SB_GPIO22 — SB_GPIO22 — TP_SB_GPIO22 22B6

45B8 14B7 PM_EXTTS_L<0> — DIMM_OVERTEMP_L 28C4 29C4

47C5 21C4 5C2 FWH_INIT_L — SMC_CPU_INIT_3_3_L 45D5

SIGNAL ALIAS /RESET

SYNC_MASTER=ENET — SYNC_DATE=08/19/2005

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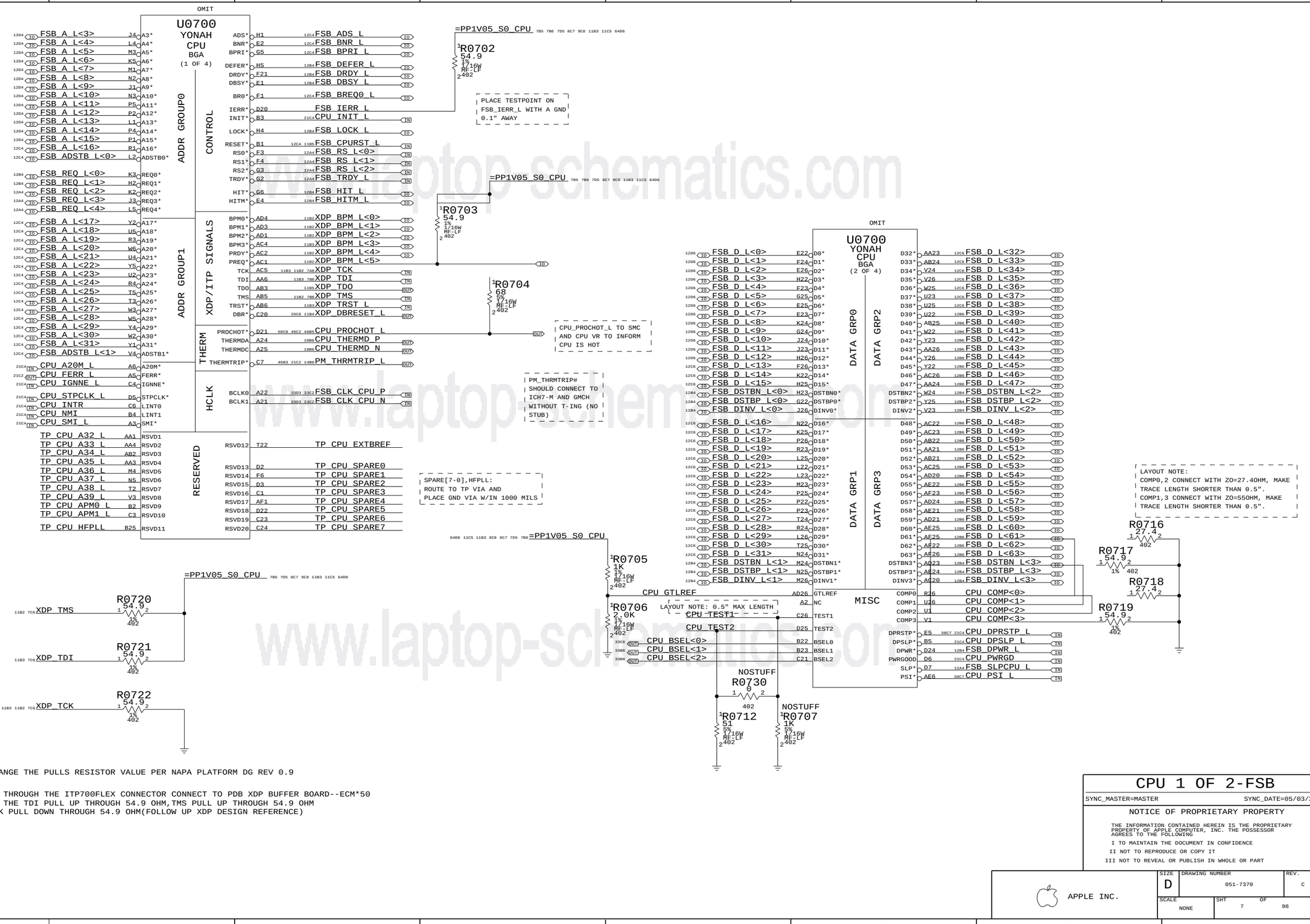
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 6 OF 98	


OMIT
U0700
YONAH
CPU
BGA
(1 OF 4)
ADDR GROUP0
CONTROL
XDP/ITP SIGNALS
ADDR GROUP1
THERM
HCLK
RESERVED
FSB_A_L<3>
FSB_A_L<4>
FSB_A_L<5>
FSB_A_L<6>
FSB_A_L<7>
FSB_A_L<8>
FSB_A_L<9>
FSB_A_L<10>
FSB_A_L<11>
FSB_A_L<12>
FSB_A_L<13>
FSB_A_L<14>
FSB_A_L<15>
FSB_A_L<16>
FSB_ADSTB_L<0>
FSB_REQ_L<0>
FSB_REQ_L<1>
FSB_REQ_L<2>
FSB_REQ_L<3>
FSB_REQ_L<4>
FSB_A_L<17>
FSB_A_L<18>
FSB_A_L<19>
FSB_A_L<20>
FSB_A_L<21>
FSB_A_L<22>
FSB_A_L<23>
FSB_A_L<24>
FSB_A_L<25>
FSB_A_L<26>
FSB_A_L<27>
FSB_A_L<28>
FSB_A_L<29>
FSB_A_L<30>
FSB_A_L<31>
FSB_ADSTB_L<1>
CPU_A20M_L
CPU_FERR_L
CPU_IGNNE_L
CPU_STPCLK_L
CPU_INTR
CPU_NMI
CPU_SMI_L
TP_CPU_A32_L
TP_CPU_A33_L
TP_CPU_A34_L
TP_CPU_A35_L
TP_CPU_A36_L
TP_CPU_A37_L
TP_CPU_A38_L
TP_CPU_A39_L
TP_CPU_APM0_L
TP_CPU_APM1_L
TP_CPU_HFPLL
ADS*
BNR*
BPRI*
DEFER*
DRDY*
DBSY*
BR0*
IERR*
INIT*
LOCK*
RESET*
RS0*
RS1*
RS2*
TRDY*
HIT*
HITM*
BPM0*
BPM1*
BPM2*
BPM3*
PRDY*
PREQ*
TCK
TDI
TDO
TMS
TRST*
DBR*
PROCHOT*
THERMDA
THERMDC
THERMTRIP*
BCLK0
BCLK1
RSVD12
RSVD13
RSVD14
RSVD15
RSVD16
RSVD17
RSVD18
RSVD19
RSVD20
FSB_ADS_L
FSB_BNR_L
FSB_BPRI_L
FSB_DEFER_L
FSB_DRDY_L
FSB_DBSY_L
FSB_BREQ0_L
FSB_IERR_L
CPU_INIT_L
FSB_LOCK_L
FSB_CPURST_L
FSB_RS_L<0>
FSB_RS_L<1>
FSB_RS_L<2>
FSB_TRDY_L
FSB_HIT_L
FSB_HITM_L
XDP_BPM_L<0>
XDP_BPM_L<1>
XDP_BPM_L<2>
XDP_BPM_L<3>
XDP_BPM_L<4>
XDP_BPM_L<5>
XDP_TCK
XDP_TDI
XDP_TDO
XDP_TMS
XDP_TRST_L
XDP_DBRESET_L
CPU_PROCHOT_L
CPU_THERMD_P
CPU_THERMD_N
PM_THRMTRIP_L
FSB_CLK_CPU_P
FSB_CLK_CPU_N
TP_CPU_EXTBREF
TP_CPU_SPARE0
TP_CPU_SPARE1
TP_CPU_SPARE2
TP_CPU_SPARE3
TP_CPU_SPARE4
TP_CPU_SPARE5
TP_CPU_SPARE6
TP_CPU_SPARE7
=PP1V05_S0_CPU
R0702 54.9 1% 1/16W MF-LF 402
PLACE TESTPOINT ON FSB_IERR_L WITH A GND 0.1" AWAY
R0703 54.9 1% 1/16W MF-LF 402
R0704 68 5% 1/16W MF-LF 402
CPU_PROCHOT_L TO SMC AND CPU VR TO INFORM CPU IS HOT
PM_THRMTRIP# SHOULD CONNECT TO ICH7-M AND GMCH WITHOUT T-ING (NO STUB)
SPARE[7-0],HFPLL: ROUTE TO TP VIA AND PLACE GND VIA W/IN 1000 MILS
R0720 54.9 1% 402
R0721 54.9 1% 402
R0722 54.9 1% 402
R0705 1K 1% 1/16W MF-LF 402
R0706 2.0K 1% 1/16W MF-LF 402
LAYOUT NOTE: 0.5" MAX LENGTH
CPU_GTLREF
CPU_TEST1
CPU_TEST2
CPU_BSEL<0>
CPU_BSEL<1>
CPU_BSEL<2>
NOSTUFF R0730 0 402
R0712 51 5% 1/16W MF-LF 402
NOSTUFF R0707 1K 5% 1/16W MF-LF 402
OMIT
U0700
YONAH
CPU
BGA
(2 OF 4)
DATA GRP0
DATA GRP1
DATA GRP2
DATA GRP3
MISC
FSB_D_L<0>
FSB_D_L<1>
FSB_D_L<2>
FSB_D_L<3>
FSB_D_L<4>
FSB_D_L<5>
FSB_D_L<6>
FSB_D_L<7>
FSB_D_L<8>
FSB_D_L<9>
FSB_D_L<10>
FSB_D_L<11>
FSB_D_L<12>
FSB_D_L<13>
FSB_D_L<14>
FSB_D_L<15>
FSB_DSTBN_L<0>
FSB_DSTBP_L<0>
FSB_DINV_L<0>
FSB_D_L<16>
FSB_D_L<17>
FSB_D_L<18>
FSB_D_L<19>
FSB_D_L<20>
FSB_D_L<21>
FSB_D_L<22>
FSB_D_L<23>
FSB_D_L<24>
FSB_D_L<25>
FSB_D_L<26>
FSB_D_L<27>
FSB_D_L<28>
FSB_D_L<29>
FSB_D_L<30>
FSB_D_L<31>
FSB_DSTBN_L<1>
FSB_DSTBP_L<1>
FSB_DINV_L<1>
FSB_D_L<32>
FSB_D_L<33>
FSB_D_L<34>
FSB_D_L<35>
FSB_D_L<36>
FSB_D_L<37>
FSB_D_L<38>
FSB_D_L<39>
FSB_D_L<40>
FSB_D_L<41>
FSB_D_L<42>
FSB_D_L<43>
FSB_D_L<44>
FSB_D_L<45>
FSB_D_L<46>
FSB_D_L<47>
FSB_DSTBN_L<2>
FSB_DSTBP_L<2>
FSB_DINV_L<2>
FSB_D_L<48>
FSB_D_L<49>
FSB_D_L<50>
FSB_D_L<51>
FSB_D_L<52>
FSB_D_L<53>
FSB_D_L<54>
FSB_D_L<55>
FSB_D_L<56>
FSB_D_L<57>
FSB_D_L<58>
FSB_D_L<59>
FSB_D_L<60>
FSB_D_L<61>
FSB_D_L<62>
FSB_D_L<63>
FSB_DSTBN_L<3>
FSB_DSTBP_L<3>
FSB_DINV_L<3>
CPU_COMP<0>
CPU_COMP<1>
CPU_COMP<2>
CPU_COMP<3>
CPU_DPRSTP_L
CPU_DPSLP_L
FSB_DPWR_L
CPU_PWRGD
FSB_SLPCPU_L
CPU_PSI_L
LAYOUT NOTE: COMP0,2 CONNECT WITH ZO=27.4OHM, MAKE TRACE LENGTH SHORTER THAN 0.5". COMP1,3 CONNECT WITH ZO=55OHM, MAKE TRACE LENGTH SHORTER THAN 0.5".
R0716 27.4 1% 402
R0717 54.9 1% 402
R0718 27.4 1% 402
R0719 54.9 1% 402
CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9
WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50
SO THE TDI PULL UP THROUGH 54.9 OHM,TMS PULL UP THROUGH 54.9 OHM
TCK PULL DOWN THROUGH 54.9 OHM(FOLLOW UP XDP DESIGN REFERENCE)
CPU 1 OF 2-FSB
SYNC_MASTER=MASTER
SYNC_DATE=05/03/2005
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SHT 7 OF 98

OMIT

U0700
YONAH
CPU
BGA
(3 OF 4)

A7	VCC_1	VCC_68	AB20
A9	VCC_2	VCC_69	AB7
A10	VCC_3	VCC_70	AC7
A12	VCC_4	VCC_71	AC9
A13	VCC_5	VCC_72	AC12
A15	VCC_6	VCC_73	AC13
A17	VCC_7	VCC_74	AC15
A18	VCC_8	VCC_75	AC17
A20	VCC_9	VCC_76	AC18
B7	VCC_10	VCC_77	AD7
B9	VCC_11	VCC_78	AD9
B10	VCC_12	VCC_79	AD10
B12	VCC_13	VCC_80	AD12
B14	VCC_14	VCC_81	AD14
B15	VCC_15	VCC_82	AD15
B17	VCC_16	VCC_83	AD17
B18	VCC_17	VCC_84	AD18
B20	VCC_18	VCC_85	AE9
C9	VCC_19	VCC_86	AE10
C10	VCC_20	VCC_87	AE12
C12	VCC_21	VCC_88	AE13
C13	VCC_22	VCC_89	AE15
C15	VCC_23	VCC_90	AE17
C17	VCC_24	VCC_91	AE18
C18	VCC_25	VCC_92	AE20
D9	VCC_26	VCC_93	AF9
D10	VCC_27	VCC_94	AF10
D12	VCC_28	VCC_95	AF12
D14	VCC_29	VCC_96	AF14
D15	VCC_30	VCC_97	AF15
D17	VCC_31	VCC_98	AF17
D18	VCC_32	VCC_99	AF18
E7	VCC_33	VCC_100	AF20
E9	VCC_34		
E10	VCC_35	VCCP_1	V6
E12	VCC_36	VCCP_2	G21
E13	VCC_37	VCCP_3	J6
E15	VCC_38	VCCP_4	K6
E17	VCC_39	VCCP_5	M6
E18	VCC_40	VCCP_6	J21
E20	VCC_41	VCCP_7	K21
F7	VCC_42	VCCP_8	M21
F9	VCC_43	VCCP_9	N21
F10	VCC_44	VCCP_10	N6
F12	VCC_45	VCCP_11	R21
F14	VCC_46	VCCP_12	R6
F15	VCC_47	VCCP_13	T21
F17	VCC_48	VCCP_14	T6
F18	VCC_49	VCCP_15	V21
F20	VCC_50	VCCP_16	W21
AA7	VCC_51		
AA9	VCC_52		
AA10	VCC_53		
AA12	VCC_54		
AA13	VCC_55		
AA15	VCC_56		
AA17	VCC_57		
AA18	VCC_58		
AA20	VCC_59		
AB9	VCC_60		
AB10	VCC_61		
AB12	VCC_62		
AB14	VCC_63		
AB15	VCC_64		
AB17	VCC_65		
AB18	VCC_66		
AB18	VCC_67		

=PPVCORE_S0_CPU 8B5 9B8 48A5 48B3 64D6
(CPU CORE POWER)

=PP1V05_S0_CPU 7B5 7B6 7D5 9C8 11B3 11C5 64D6
(CPU IO POWER 1.05V)

VCCA=1.5 ONLY

VCCA B26 =PP1V5_S0_CPU 8D8 64C6
(CPU INTERNAL PLL POWER 1.5V)

VID0	AD6	CPU_VID<0>	OUT 9C3
VID1	AF5	CPU_VID<1>	OUT 9C3
VID2	AE5	CPU_VID<2>	OUT 9C3
VID3	AF4	CPU_VID<3>	OUT 9C3
VID4	AE3	CPU_VID<4>	OUT 9C3
VID5	AF2	CPU_VID<5>	OUT 9D3
VID6	AE2	CPU_VID<6>	OUT 9D3

VID FOR CPU POWER SUPPLY
IF NO USE, NEED PULL-UP OR
PULL-DOWN

=PPVCORE_S0_CPU 8D7 9B8 48A5 48B3 64D6

R0802
100
1%
1/16W
MF-LF
402

VCCSENSE	AF7	CPU_VCCSENSE_P	OUT 58A4 58A5
VSSSENSE	AE7	CPU_VCCSENSE_N	OUT 58A4 58A5

LAYOUT NOTE:
PROVIDE A TEST POINT (WITH NO STUB)
TO CONNECT A DIFFERENCTIAL PROBE
BETWEEN VCCSENSE AND VSSSENSE AT THE
LOCATION WHERE THE TWO 54.9 OHM
RESISTORS TERMINATE THE 55 OHM
TRANSMISSION LINE.

R0803
100
1%
1/16W
MF-LF
402

LAYOUT NOTE: CONNECT R0803
TO TP_VSSSENSE WITH NO
STUB.

LAYOUT NOTE:
CPU_VCCSENSE_P/CPU_VCCSENSE_N USE
Z0=27.4 OHM DIFFERNTIAL TRACE ROUTING.

LAYOUT NOTE:
VCCSENSE AND VSSSENSE LINES
SHOULD BE OF EQUAL LENGTH

OMIT

U0700
YONAH
CPU
BGA
(4 OF 4)

A4	VSS_1	VSS_82	P6
A8	VSS_2	VSS_83	P21
A11	VSS_3	VSS_84	P24
A14	VSS_4	VSS_85	R2
A16	VSS_5	VSS_86	R5
A19	VSS_6	VSS_87	R22
A23	VSS_7	VSS_88	R25
A26	VSS_8	VSS_89	T1
B6	VSS_9	VSS_90	T4
B8	VSS_10	VSS_91	T23
B11	VSS_11	VSS_92	T26
B13	VSS_12	VSS_93	U3
B16	VSS_13	VSS_94	U6
B19	VSS_14	VSS_95	U21
B21	VSS_15	VSS_96	U24
B24	VSS_16	VSS_97	V2
C5	VSS_17	VSS_98	V5
C8	VSS_18	VSS_99	V22
C11	VSS_19	VSS_100	V25
C14	VSS_20	VSS_101	W1
C16	VSS_21	VSS_102	W4
C19	VSS_22	VSS_103	W23
C2	VSS_23	VSS_104	W26
C22	VSS_24	VSS_105	Y3
C25	VSS_25	VSS_106	Y6
D1	VSS_26	VSS_107	Y21
D4	VSS_27	VSS_108	Y24
D8	VSS_28	VSS_109	AA2
D11	VSS_29	VSS_110	AA5
D13	VSS_30	VSS_111	AA8
D16	VSS_31	VSS_112	AA11
D19	VSS_32	VSS_113	AA14
D23	VSS_33	VSS_114	AA16
D26	VSS_34	VSS_115	AA19
E3	VSS_35	VSS_116	AA22
E6	VSS_36	VSS_117	AA25
E8	VSS_37	VSS_118	AB1
E11	VSS_38	VSS_119	AB4
E14	VSS_39	VSS_120	AB8
E16	VSS_40	VSS_121	AB11
E19	VSS_41	VSS_122	AB13
E21	VSS_42	VSS_123	AB16
E24	VSS_43	VSS_124	AB19
F5	VSS_44	VSS_125	AB23
F8	VSS_45	VSS_126	AB26
F11	VSS_46	VSS_127	AC3
F13	VSS_47	VSS_128	AC6
F16	VSS_48	VSS_129	AC8
F19	VSS_49	VSS_130	AC11
F2	VSS_50	VSS_131	AC14
F22	VSS_51	VSS_132	AC16
F25	VSS_52	VSS_133	AC19
G4	VSS_53	VSS_134	AC21
G1	VSS_54	VSS_135	AC24
G23	VSS_55	VSS_136	AD2
G26	VSS_56	VSS_137	AD5
H3	VSS_57	VSS_138	AD8
H6	VSS_58	VSS_139	AD11
H21	VSS_59	VSS_140	AD13
H24	VSS_60	VSS_141	AD16
J2	VSS_61	VSS_142	AD19
J5	VSS_62	VSS_143	AD22
J22	VSS_63	VSS_144	AD25
J25	VSS_64	VSS_145	AE1
K1	VSS_65	VSS_146	AE4
K4	VSS_66	VSS_147	AE8
K23	VSS_67	VSS_148	AE11
K26	VSS_68	VSS_149	AE14
L3	VSS_69	VSS_150	AE16
L6	VSS_70	VSS_151	AE19
L21	VSS_71	VSS_152	AE23
L24	VSS_72	VSS_153	AE26
M2	VSS_73	VSS_154	AF3
M5	VSS_74	VSS_155	AF6
M22	VSS_75	VSS_156	AF8
M25	VSS_76	VSS_157	AF11
N1	VSS_77	VSS_158	AF13
N4	VSS_78	VSS_159	AF16
N23	VSS_79	VSS_160	AF19
N26	VSS_80	VSS_161	AF21
P3	VSS_81	VSS_162	AF24

CPU 2 OF 2-PWR/GND

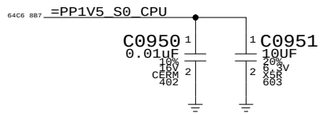
SYNC_MASTER=MASTER SYNC_DATE=05/03/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

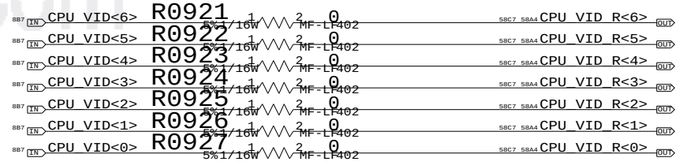
SCALE	SHT	OF
NONE	8	98

VCCA DECOUPLING
(CPU INTERNAL PLL POWER 1.5V)



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602	?	ALL	USE SAMSUNG AND MURATA ONLY
138S0606	138S0602	?	ALL	USE TAIYO

CPU CORE VID<> SETTINGS

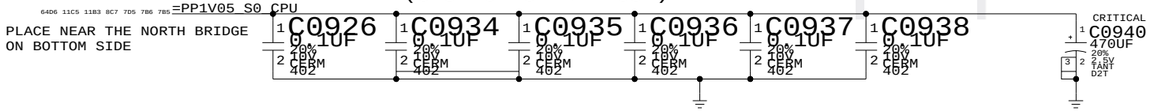


R0921~R0927 FOR CPU VOLTAGE MANUAL SETTING

VCCP CORE DECOUPLING
(CPU IO POWER 1.05V)

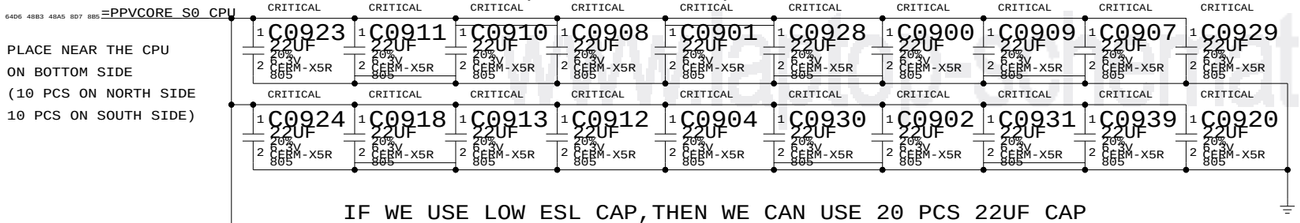
THIS 470UF FOR CPU,GMCH FSB BUS 1.05V

PLACE NEAR THE NORTH BRIDGE
ON BOTTOM SIDE



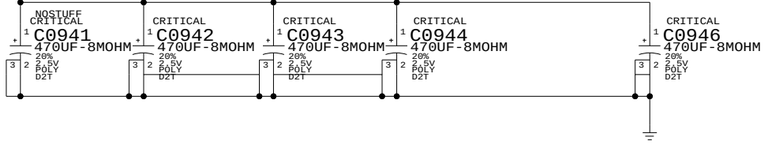
VCC CORE DECOUPLING
(CPU CORE POWER)

PLACE NEAR THE CPU
ON BOTTOM SIDE
(10 PCS ON NORTH SIDE
10 PCS ON SOUTH SIDE)



IF WE USE LOW ESL CAP,THEN WE CAN USE 20 PCS 22UF CAP

(2 PCS ON NORTH SIDE
2 PCS ON SOUTH SIDE)



		MIN	TYP	MAX
DUAL CORE SV CPU	VCCHFM	1.1625		1.30
	VCCLFM	TBD		TBD
SINGLE CORE SV CPU	VCCHFM	1.1625		1.30
	VCCLFM		TBD	
DUAL CORE LV CPU	VCCHFM	1.0		1.1625
	VCCLFM		TBD	
ULV CPU	VCCHFM	TBD		TBD
	VCCLFM		TBD	

UNIT: V

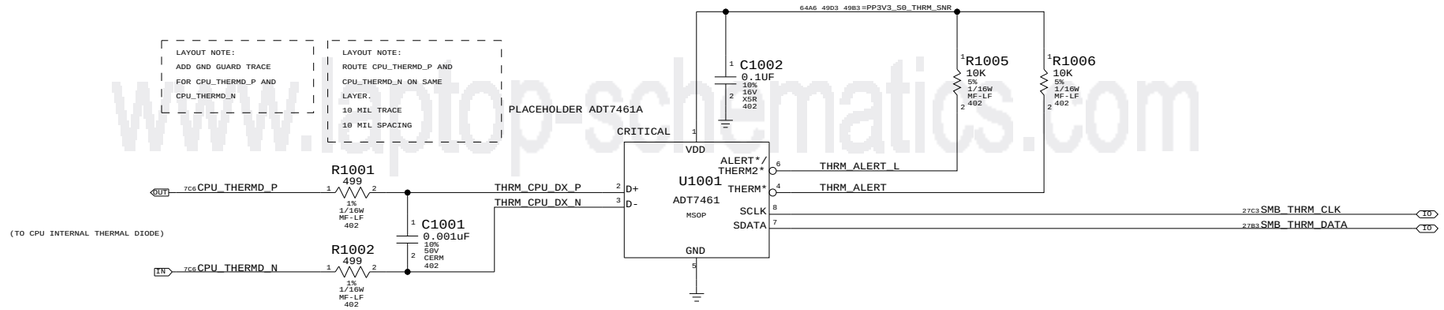
ALL PROCESSOR DEFAULT VCORE FOR INITIAL POWER UP IS 1.2V
TWO PROCESSORS AT THE SAME FREQUENCY MAY HAVE DIFFERENT SETTING WITH THE VID RANGE(VCORE VOLTAGE)!
REFER TO YONAH PROCESSOR EMTS REV 1.0
VCCHFM: VCORE AT HIGHEST FREQUENCY MODE
VCCLFM: VCORE AT LOWEST FREQUENCY MODE

CPU DECAPS & VID<>

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 9 OF 98	

CPU ZONE THERMAL SENSOR



PLACE U1001 NEAR THE U1200

CPU MISC1-TEMP SENSOR

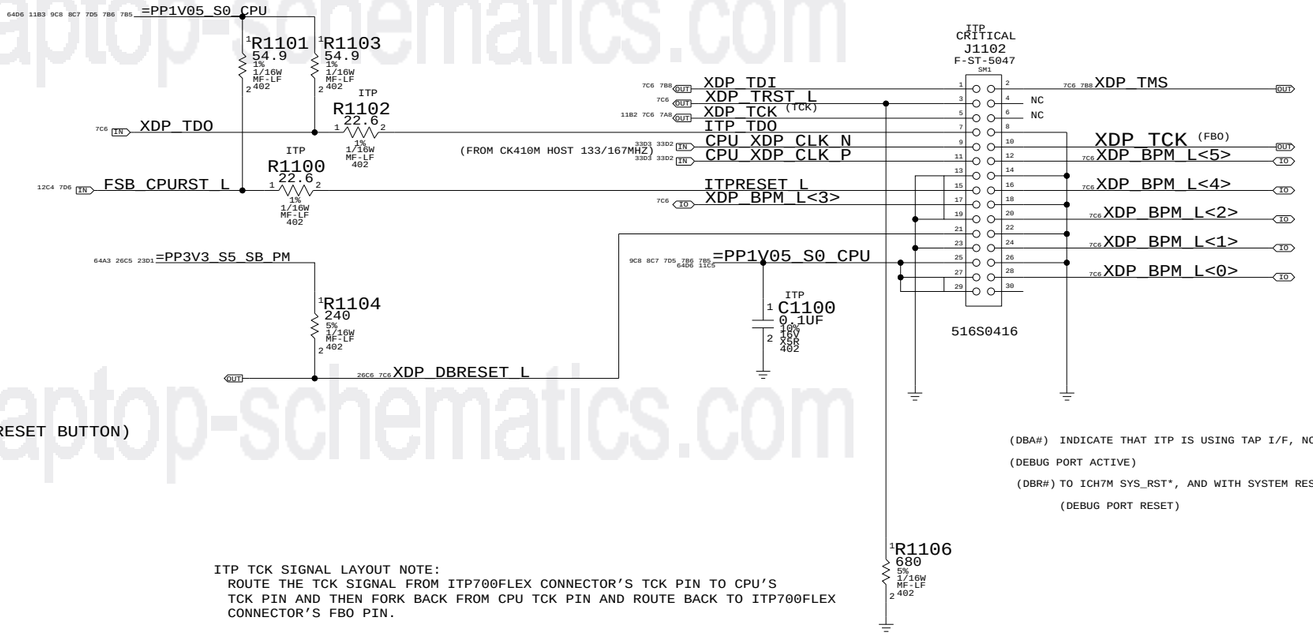
SYNC_MASTER=ENET SYNC_DATE=08/19/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE	SHT	OF
NONE	10	98

CPU ITP700FLEX DEBUG SUPPORT



(AND WITH RESET BUTTON)

ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

(DBA#) INDICATE THAT ITP IS USING TAP I/F, NC IN 945GM CHIPSET SYSTEM.

(DEBUG PORT ACTIVE)

(DBR#) TO ICH7M SYS_RST*, AND WITH SYSTEM RESET LOGIC

(DEBUG PORT RESET)

CPU ITP700FLEX DEBUG

SYNC_MASTER=MASTER SYNC_DATE=5/23/05

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 11 OF 98	

NB CPU Interface

SYNC_MASTER=NB SYNC_DATE=07/25/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 12 OF 98	

LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

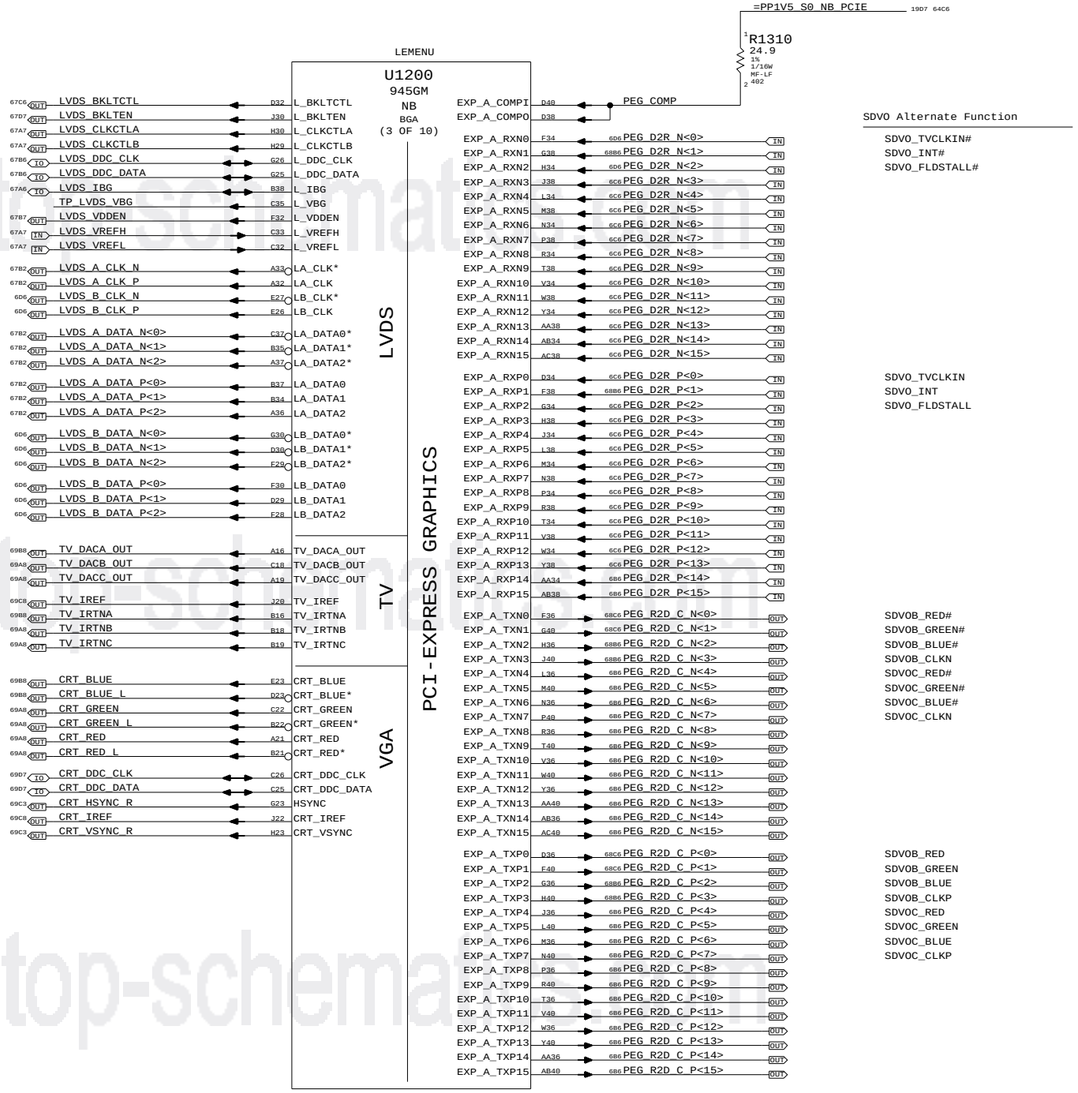
Unused DAC outputs must remain powered, but can omit
filtering components. Unused DAC outputs should
connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.

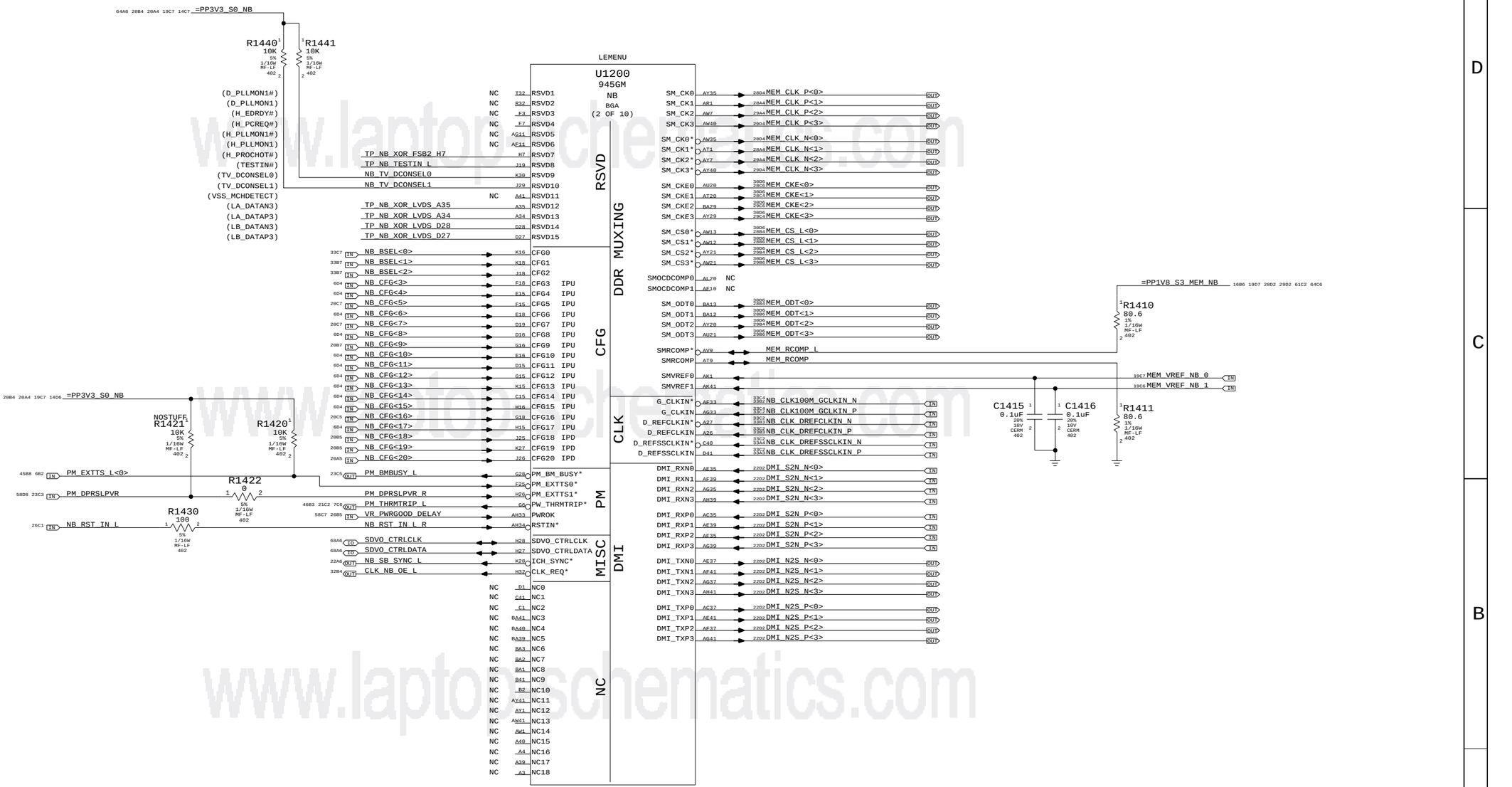


NB PEG / Video Interfaces

SYNC_MASTER=NB SYNC_DATE=07/25/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 13 OF 98	

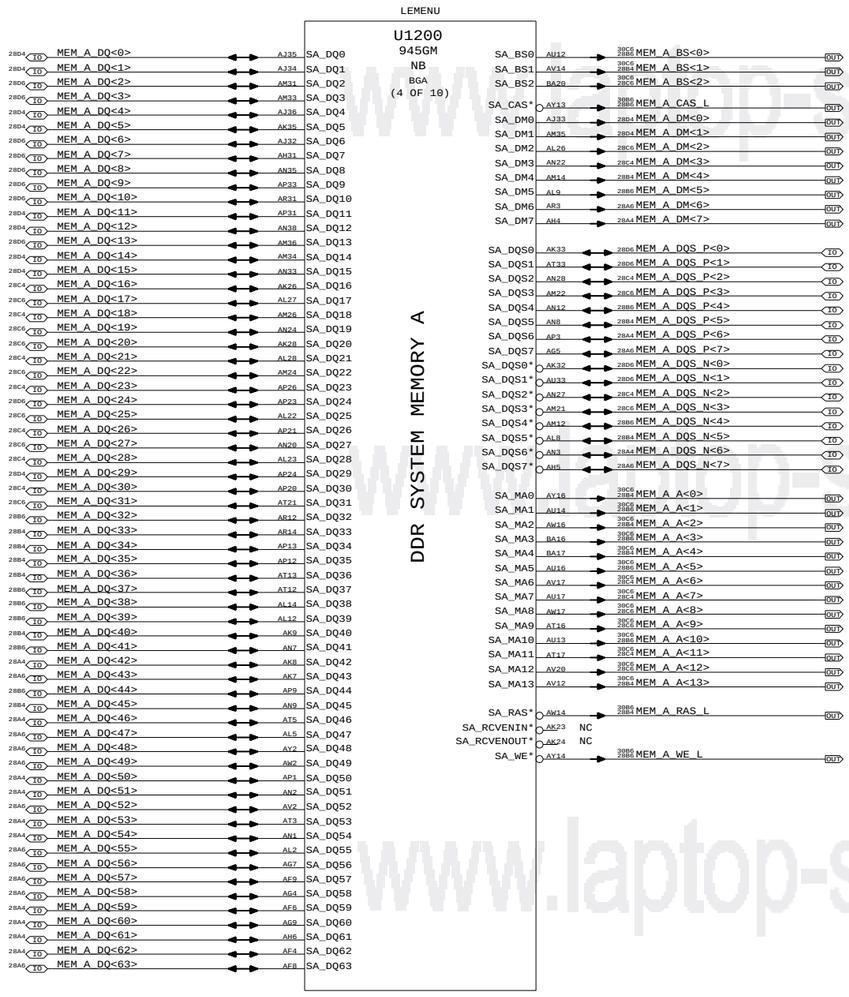


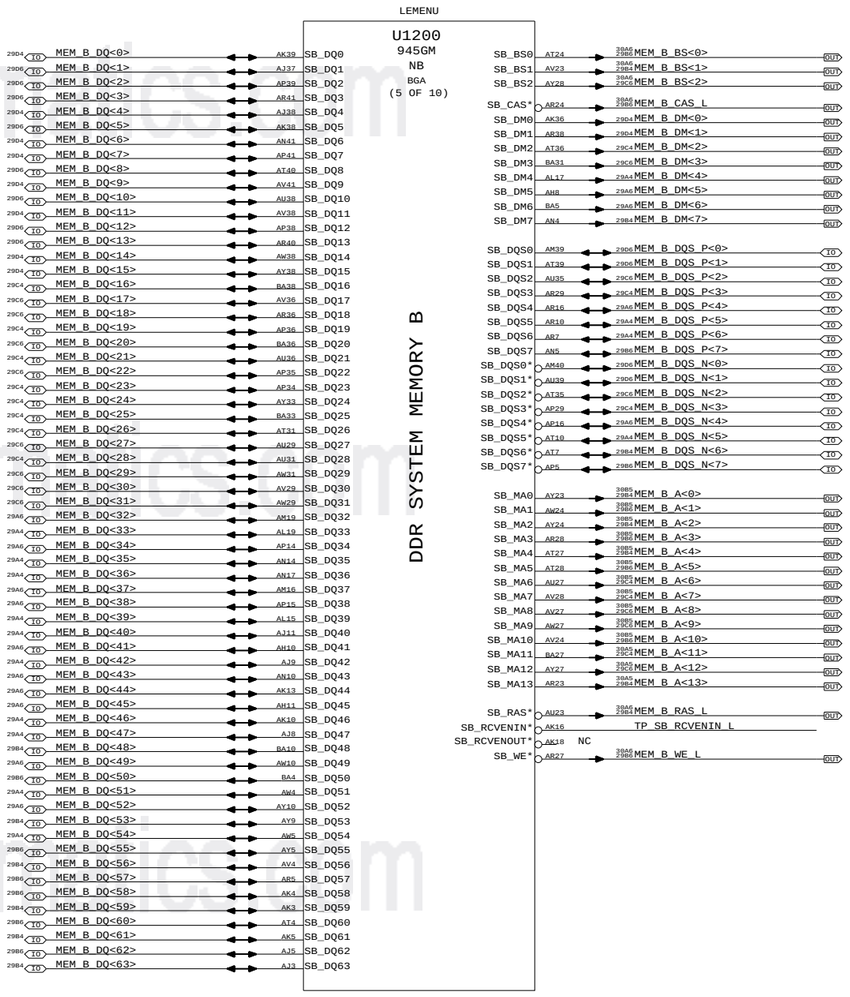
NB Misc Interfaces

SYNC_MASTER=NB SYNC_DATE=08/15/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 14 OF 98	





NB DDR2 Interfaces

SYNC_MASTER=NB SYNC_DATE=07/25/2005

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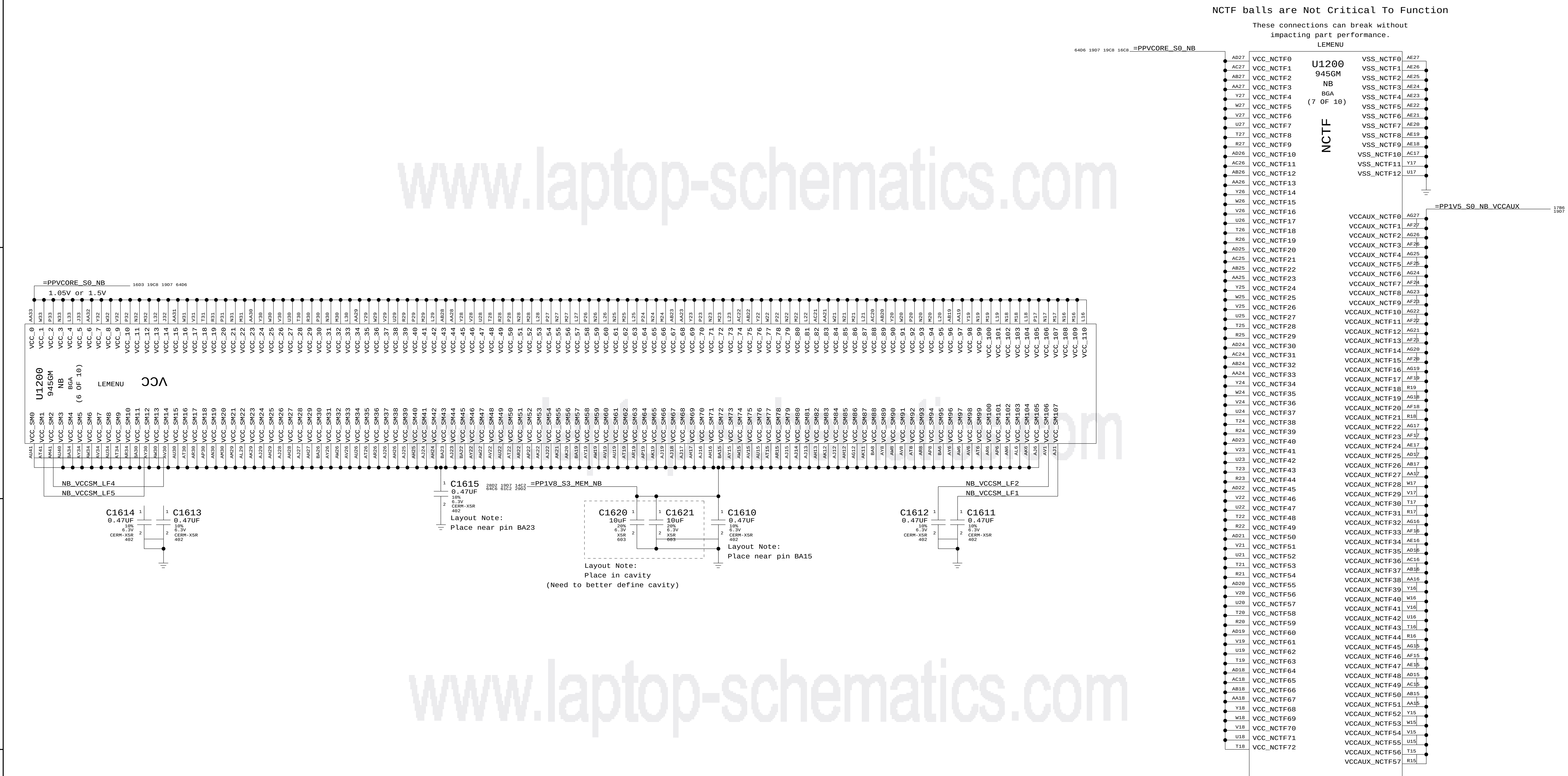
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 15 OF 98	



NB Power 1

SYNC_MASTER=NB SYNC_DATE=07/25/2005

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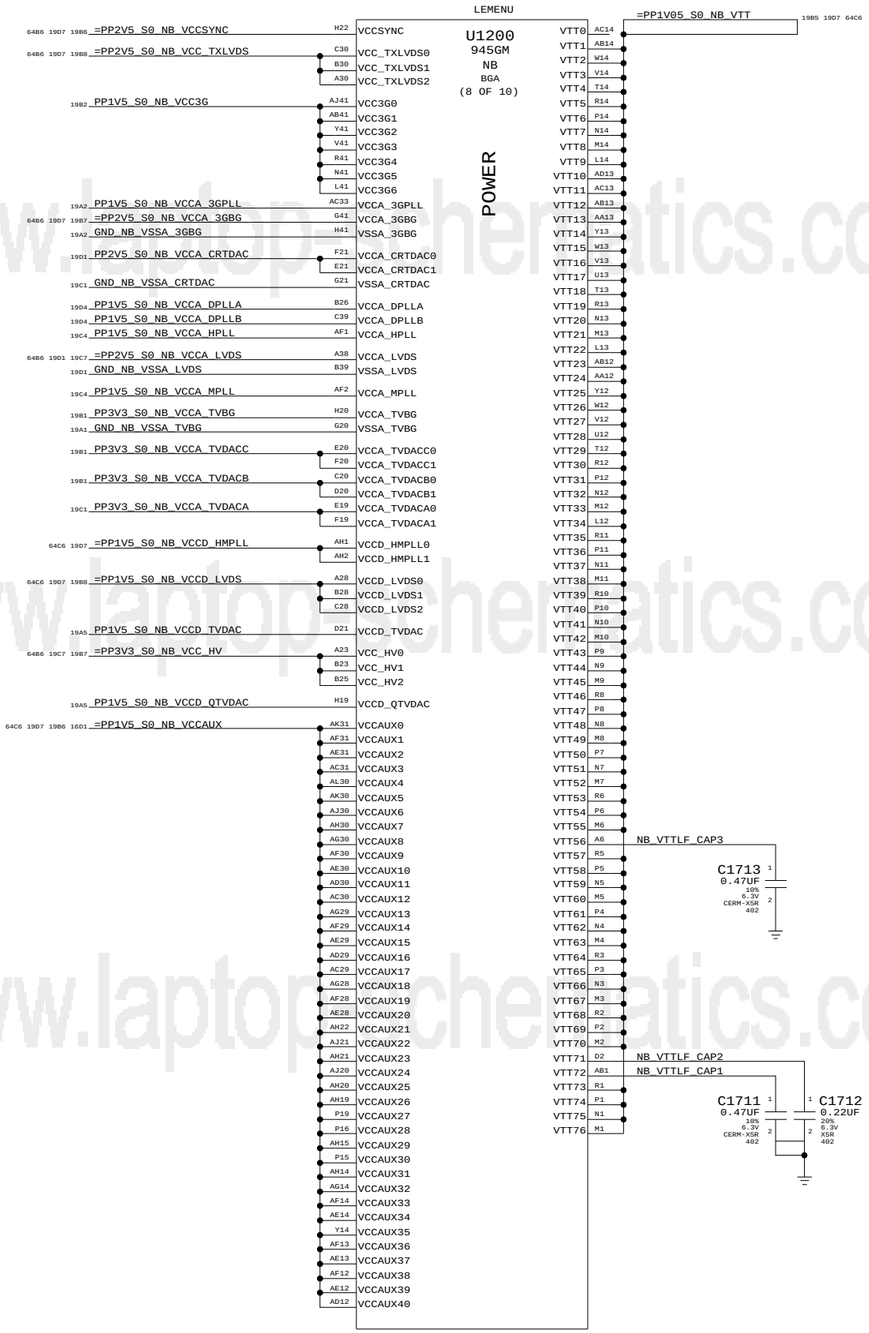
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE NONE	SHT 16	OF 98

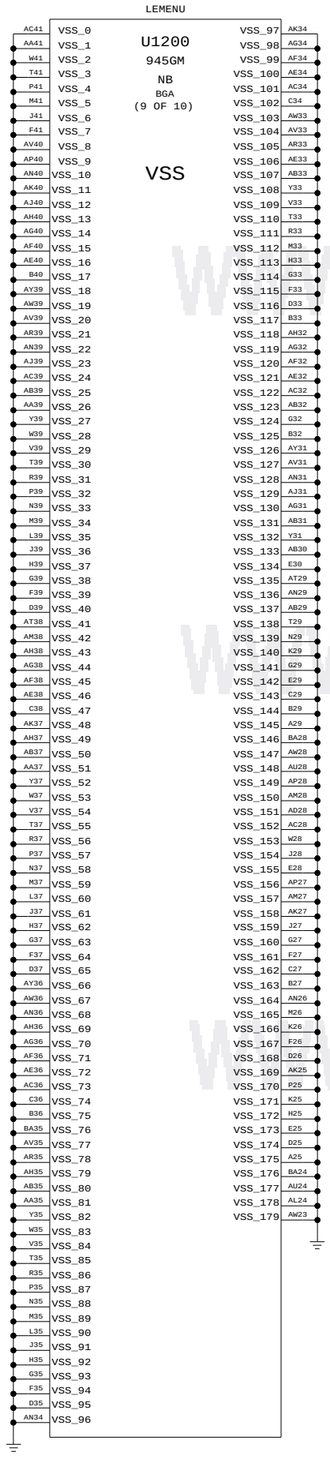


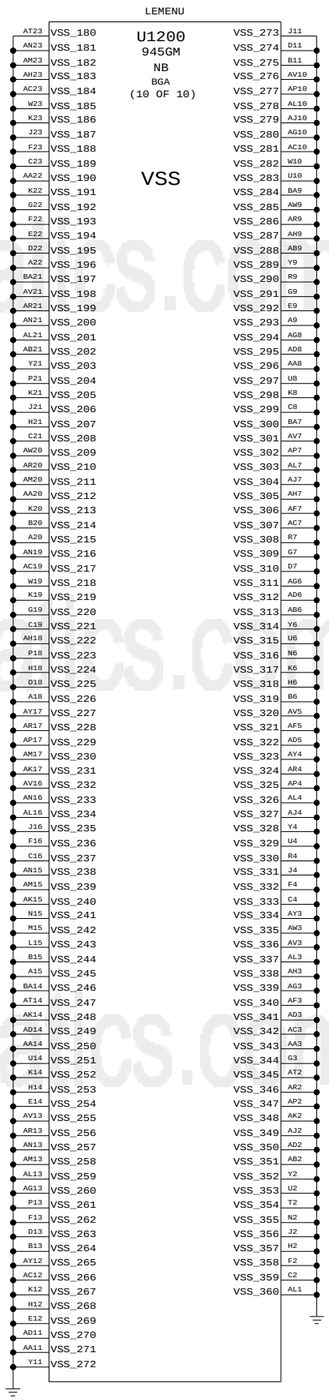
NB Power 2

SYNC_MASTER=NB SYNC_DATE=07/25/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 17 OF 98	





NB Grounds

SYNC_MASTER=NB SYNC_DATE=07/25/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 18 OF 98	

Power Interface

These are the power signals that leave the NB "block"

IN =PP1V05_S0_FSB_NB 12A7 12B7 12C2 33B8 33C7 33C8 64D6
IN =PPVCORE_S0_NB 16C8 16D3 19C8 64D6
IN =PP1V05_S0_NB 19D1 64C6
IN =PP1V05_S0_NB_VTT 17D3 19B5 64C6

IN =PP1V5_S0_NB 19C1 64C6
IN =PP1V5_S0_NB_PCIE 13D2 64C6
IN =PP1V5_S0_NB_PLL 19C6 64C6
IN =PP1V5_S0_NB_TVDAC 19A8 64C6
IN =PP1V5_S0_NB_VCCD_HMPLL 17C6 64C6
IN =PP1V5_S0_NB_VCCD_LVDS 17C6 19B8 64C6
IN =PP1V5_S0_NB_VCCAUX 16D1 17B6 19B6 64C6
IN =PP1V8_S3_MEM_NB 14C2 16B6 28D2 29D2 61C2 64C6

IN =PP2V5_S0_NB_CRTDAC 19D4 64B6

IN =PP2V5_S0_NB_VCCSYNC 17D6 19B6 64B6
IN =PP2V5_S0_NB_VCC_TXLVDS 17D6 19B8 64B6
IN =PP2V5_S0_NB_VCCA_3GBG 17D6 19B7 64B6
IN =PP2V5_S0_NB_VCCA_LVDS 17C6 19D1 64B6

IN =PP3V3_S0_NB 14C7 14D6 28A4 28B4 64A6
IN =PP3V3_S0_NB_VCC_HV 17C6 19B7 64B6

IN =PP5V_S0_NB_TVDAC 19C4 64D3

MCH DISPLAY PLL POWER LDO

CRITICAL
U1900
TPS73115
SOT23-5
64B6 =PP2V5_S0_NB_DISP_PLL
IN
EN
OUT PP1V5_S0_DPLL
NR/FB TPS73115_NR
GND
C1950 1UF 10% 6.3V CERM 402
C1951 0.01uF 10% 16V CERM 402
C1952 10uF 20% 6.3V X5R 603

R1950 0 5% 1/16W MF-LF 402
MCH VCCA_DPLLA FILTER
(MCH DISPLAY A PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_DPLLA 17C6
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
C1953 0.1uF 20% 10V CERM 402

R1951 0 5% 1/16W MF-LF 402
GMCH VCCA_DPLL_B FILTER
(MCH DISPLAY B PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_DPLLB 17C6
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
C1954 0.1uF 20% 10V CERM 402

Layout Note:
THESE 4 0.1UF CAPS SHOULD
be within 5 mm of NB edge

MCH VCCA_LVDS FILTER

(MCH LVDS ANALOG 2.5V PWR)
=PP2V5_S0_NB_VCCA_LVDS 17C6 19C7 64B6
C1980 0.1uF 20% 10V CERM 402
C1981 0.01uF 10% 16V CERM 402
GND_NB_VSSA_LVDS 17C6

Layout Note:
This 0.1uF cap should
be within 5 mm of NB edge

Layout Note: Route to caps, then GND

64B6 19D7 =PP2V5_S0_NB_CRTDAC
R1985 10 1% 1/16W MF-LF 402
PP2V5_S0_NB_CRTDAC_FOLLOW
VOLTAGE=2.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
D1986 BAT54DW SOT-363
=PP1V05_S0_NB 19D7 64C6
L1985 180-OHM-1.5A 0603
PP2V5_S0_NB_CRTDAC_F
C1986 22000pF-1000mA 16V NFM18

MCH VCCA_CRTDAC BYPASS
(MCH CRTDAC ANALOG 2.5V PWR)
PP2V5_S0_NB_VCCA_CRTDAC 17D6
VOLTAGE=2.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
C1985 0.1uF 20% 10V CERM 402

Layout Note:
These 2 caps should be
within 6.35 mm of NB edge

GND_NB_VSSA_CRTDAC 17D6
Layout Note: Route to caps, then GND

GMCH CORE PWR 1.05V BYPASS

THIS 470UF FOR GMCH CORE 1.05V

19D7 16D3 19C8 64D6 =PPVCORE_S0_NB
CRITICAL
C1900 470UF 20% 2.5V TANT D2T
C1902 10uF 20% 6.3V X5R 603
C1903 10uF 20% 6.3V X5R 603
C1904 1UF 10% 6.3V CERM 402
C1905 0.22uF 20% 6.3V X5R 402
C1906 0.22uF 20% 6.3V X5R 402
C1907 0.22uF 20% 6.3V X5R 402

64C3 29D6 29D4 29B2 28D6 28D4 28B2 19C8 =PP1V8_S3_MEM
29B2 28D6 28D4 28B2 19C8 64C3 29D6 29D4 =PP1V8_S3_MEM
PLACE THOSE COMPONENT
CLOSE TO GMCH
R1988 1K 1% 1/16W MF-LF 402
MEM_VREF_NB_0 14C2
VOLTAGE=0.9V
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
R1989 1K 1% 1/16W MF-LF 402
R1986 1K 1% 1/16W MF-LF 402
MEM_VREF_NB_1 14C2
VOLTAGE=0.9V
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
R1987 1K 1% 1/16W MF-LF 402

64C6 19D7 =PP1V5_S0_NB_PLL
L1934 FERR-120-OHM-0.2A 0603
CRITICAL
C1934 22UF 20% 6.3V CERM-X5R 805
C1935 0.1uF 20% 10V CERM 402

GMCH VCCA_HPLL FILTER
(HOST PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_HPLL 17C6
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm

L1936 FERR-120-OHM-0.2A 0603
CRITICAL
C1936 22UF 20% 6.3V CERM-X5R 805
C1937 0.1uF 20% 10V CERM 402

GMCH VCCA_MPLL FILTER
(MCH MEMORY PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_MPLL 17C6
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm

64D3 19C7 =PP5V_S0_NB_TVDAC
CRITICAL
U1901
MM157
SOT23-5-LF
VIN
CONT
GND
NOISE
VOUT PP3V3_S0_NB_TVDAC
MM1573DN_NR
C1940 1UF 10% 6.3V CERM 402
C1941 0.01uF 10% 16V CERM 402
C1942 1UF 10% 6.3V CERM 402

R1990 10 1% 1/16W MF-LF 402
PP3V3_S0_NB_TVDAC_FOLLOW
VOLTAGE=3.3V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
D1986 BAT54DW SOT-363
=PP1V5_S0_NB 19D7 64C6
L1990 180-OHM-1.5A 0603
PP3V3_S0_NB_TVDAC_F
C1992 22000pF-1000mA 16V NFM18

MCH VCCA_TVDACC FILTER
(MCH TV OUT CHANNEL A 3.3V PWR)
PP3V3_S0_NB_VCCA_TVDACA 17C6
VOLTAGE=3.3V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
C1990 10uF 20% 6.3V X5R 603
C1991 0.1uF 20% 10V CERM 402

C1994 22000pF-1000mA 16V NFM18

MCH VCCA_TVDACC FILTER
(MCH TV OUT CHANNEL B 3.3V PWR)
PP3V3_S0_NB_VCCA_TVDACB 17C6
VOLTAGE=3.3V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
C1993 0.1uF 20% 10V CERM 402

Layout Note:
These 8 caps should be
within 6.35 mm of NB edge

C1996 22000pF-1000mA 16V NFM18

MCH VCCA_TVDACC FILTER
(MCH TV OUT CHANNEL C 3.3V PWR)
PP3V3_S0_NB_VCCA_TVDACC 17C6
VOLTAGE=3.3V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
C1995 0.1uF 20% 10V CERM 402

C1998 22000pF-1000mA 16V NFM18

MCH VCCA_TVBG FILTER
(MCH TV DAC BAND GAP 3.3V PWR)
PP3V3_S0_NB_VCCA_TVBG 17C6
VOLTAGE=3.3V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
C1997 0.1uF 20% 10V CERM 402

GND_NB_VSSA_TVBG 17C6
Layout Note: Route to caps, then GND

GMCH VCCD_LVDS BYPASS

(MCH LVDS DIGITAL 1.5V PWR)
64C6 19D7 17C6 =PP1V5_S0_NB_VCCD_LVDS
C1910 10uF 20% 6.3V X5R 603
C1911 0.1uF 20% 10V CERM 402

945 EDS: 5 mOhm, 1nH (1210?)

GMCH VCCTX_LVDS BYPASS

(MCH LVDS DATA/CLK TX 2.5V PWR)
64B6 19D7 17D6 =PP2V5_S0_NB_VCC_TXLVDS
C1912 4.7uF 20% 6.3V CERM 603
C1913 0.1uF 20% 10V CERM 402

945 EDS: 1210?

MCH VCC_HV BYPASS

(MCH HV BUFFER 3.3V PWR)
64B6 19C7 17C6 =PP3V3_S0_NB_VCC_HV
C1914 10uF 20% 6.3V X5R 603
C1915 0.1uF 20% 10V CERM 402

MCH VCCSYNC BYPASS

(MCH H/V SYNC 2.5V PWR)
19D7 17D6 64B6 =PP2V5_S0_NB_VCCSYNC
C1917 0.1uF 20% 10V CERM 402

MCH VTT BYPASS

(MCH FSB 1.05V PWR) (SHARE C0940 470UF)
64C6 19D7 17D3 =PP1V05_S0_NB_VTT
C1965 4.7uF 20% 6.3V CERM 603
C1966 2.2uF 20% 6.3V CERM1 603

Layout Note:
Place in cavity

C1967 0.22uF 20% 6.3V X5R 402

Layout Note:
Place on the edge

MCH VCCA_3GBG BYPASS

(MCH PCIE/DMI BAND GAP 2.5V PWR)
64B6 19D7 17D6 =PP2V5_S0_NB_VCCA_3GBG
C1916 0.1uF 20% 10V CERM 402

GMCH VCCAUX FILTER

(MCH DDR DLL&IO, FSB HSIO&IO PWR 1.5V)
64C6 19D7 17B6 16D1 =PP1V5_S0_NB_VCCAUX
C1918 0.1uF 20% 10V CERM 402

91NH, 20%, 20MOHM, 1.5A (1210 TYP)
CRITICAL
L1970 91nH 1210
64C6 =PP1V5_S0_NB_3G
CRITICAL
C1970 220UF 20% 2.5V POLY CASE-B2

Layout Note:
Place L and C
close to MCH

GMCH VCC3G FILTER

(PCI-E/DMI ANALOG 1.5V PWR)
PP1V5_S0_NB_VCC3G 17D6
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
C1971 10uF 20% 6.3V CERM 603
C1972 10uF 20% 6.3V X5R 603

Layout Note:
10uF caps should
be close to MCH
on opposite side.

64C6 19D7 =PP1V5_S0_NB_TVDAC
C1921 22000pF-1000mA 16V NFM18

GMCH VCCD_TVDAC FILTER
(MCH TVDAC DEDICATED PWR 1.5V)
PP1V5_S0_NB_VCCD_TVDAC 17C6
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
C1920 0.1uF 20% 10V CERM 402

Layout Note:
These 4 caps should be
within 6.35 mm of NB edge

L1922 180-OHM-1.5A 0603
PP1V5_S0_NB_QTVDAC
C1923 22000pF-1000mA 16V NFM18

GMCH VCCD_QTVDAC FILTER
(MCH TVDAC DIGITAL QUIET 1.5V PWR)
PP1V5_S0_NB_VCCD_QTVDAC 17B6
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
C1922 0.1uF 20% 10V CERM 402

1uH, 20%
64C6 =PP1V5_S0_NB_3GPLL
L1975 1.0UH-220MA-0.12-OHM 0805
PP1V5_S0_NB_3GPLL_F
R1975 0.51 1% 1/16W MF-LF 402

GMCH VCCA_3GPLL FILTER

(3GIO PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_3GPLL 17D6
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
C1975 10uF 20% 6.3V X5M 603
C1976 0.1uF 20% 10V CERM 402

Layout Note:
3GPLL 10uF cap should
be placed in cavity

GND_NB_VSSA_3GBG 17D6
Layout Note: Route to caps, then GND

NB (GM) Decoupling

SYNC_MASTER=NB SYNC_DATE=06/22/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 19 OF 98	

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14C6 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
R2075
2.2K
5%
1/16W
MF-LF
402

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14C6 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
R2077
2.2K
5%
1/16W
MF-LF
402

NB_CFG<8>	RESERVED

14C6 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
R2079
2.2K
5%
1/16W
MF-LF
402

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14C6 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5%
1/16W
MF-LF
402

NB_CFG<17>	RESERVED

=PP3V3_S0_NB 14C7 14D6 19C7 20A4 20B4 64A6
NBCFG_VCC_1V5

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

R2058
2.2K
5%
1/16W
MF-LF
402

14C6 NB_CFG<18>
Internal pull-down

=PP3V3_S0_NB 14C7 14D6 19C7 20A4 20B4 64A6
NBCFG_DMI_REVERSE

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

R2059
2.2K
5%
1/16W
MF-LF
402

14C6 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

=PP3V3_S0_NB 14C7 14D6 19C7 20A4 20B4 64A6
NBCFG_SDVO_AND_PCIE

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

R2060
2.2K
5%
1/16W
MF-LF
402

14B6 NB_CFG<20>
Internal pull-down

PROBABLY NOT NEEDED

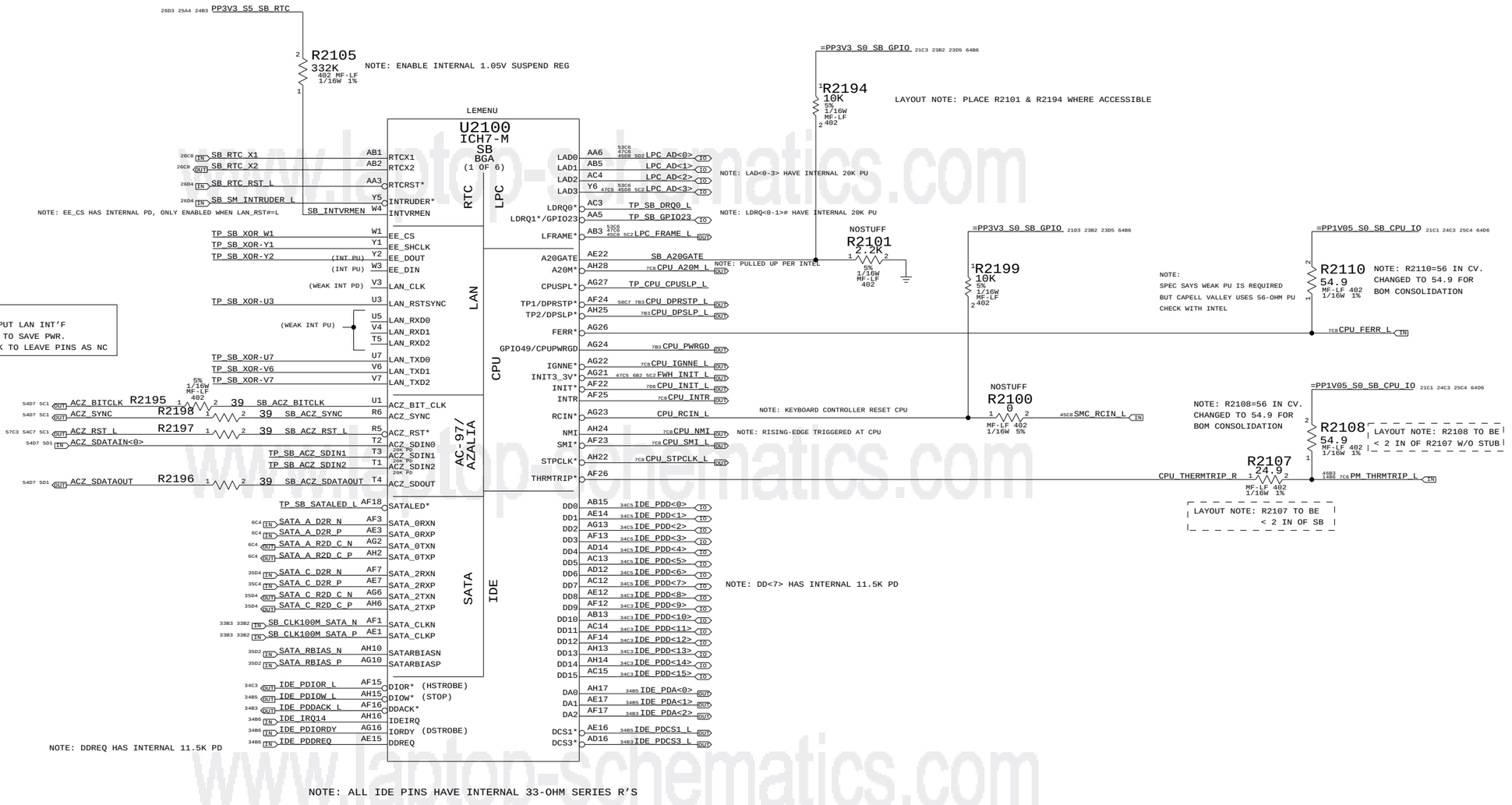
NB Config Straps

SYNC_MASTER=NB SYNC_DATE=06/28/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE	SHT	OF
NONE	20	98

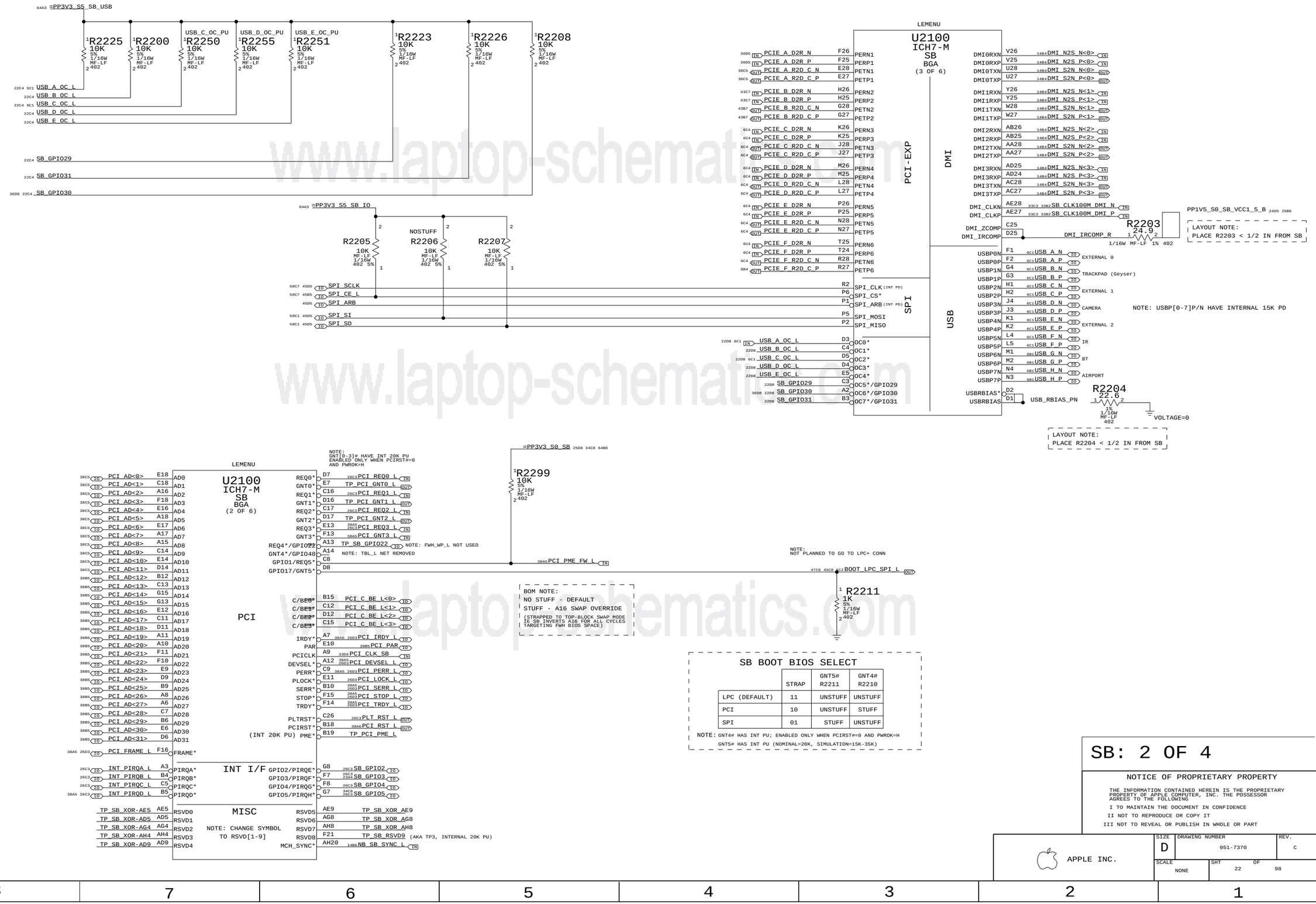


	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#		NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 21 OF 98	


=PP3V3_S5_SB_USB
R2225 10K 5% 1/16W MF-LF 402
R2200 10K 5% 1/16W MF-LF 402
R2250 10K 5% 1/16W MF-LF 402
R2255 10K 5% 1/16W MF-LF 402
R2251 10K 5% 1/16W MF-LF 402
R2223 10K 5% 1/16W MF-LF 402
R2226 10K 5% 1/16W MF-LF 402
R2208 10K 5% 1/16W MF-LF 402
USB_C_OC_PU
USB_D_OC_PU
USB_E_OC_PU
USB_A_OC_L
USB_B_OC_L
USB_C_OC_L
USB_D_OC_L
USB_E_OC_L
SB_GPIO29
SB_GPIO31
SB_GPIO30
=PP3V3_S5_SB_IO
R2205 10K MF-LF 1/16W 402 5%
NOSTUFF
R2206 10K MF-LF 1/16W 402 5%
R2207 10K MF-LF 1/16W 402 5%
SPI_SCLK
SPI_CE_L
SPI_ARB
SPI_SI
SPI_SO
LEMENU
U2100
ICH7-M
SB
BGA
(3 OF 6)
PCIE_A_D2R_N
PCIE_A_D2R_P
PCIE_A_R2D_C_N
PCIE_A_R2D_C_P
PCIE_B_D2R_N
PCIE_B_D2R_P
PCIE_B_R2D_C_N
PCIE_B_R2D_C_P
PCIE_C_D2R_N
PCIE_C_D2R_P
PCIE_C_R2D_C_N
PCIE_C_R2D_C_P
PCIE_D_D2R_N
PCIE_D_D2R_P
PCIE_D_R2D_C_N
PCIE_D_R2D_C_P
PCIE_E_D2R_N
PCIE_E_D2R_P
PCIE_E_R2D_C_N
PCIE_E_R2D_C_P
PCIE_F_D2R_N
PCIE_F_D2R_P
PCIE_F_R2D_C_N
PCIE_F_R2D_C_P
PCI-EXP
DMI
DMI0RXN
DMI0RXP
DMI0TXN
DMI0TXP
DMI1RXN
DMI1RXP
DMI1TXN
DMI1TXP
DMI2RXN
DMI2RXP
DMI2TXN
DMI2TXP
DMI3RXN
DMI3RXP
DMI3TXN
DMI3TXP
DMI_CLKN
DMI_CLKP
DMI_ZCOMP
DMI_IRCOMP
DMI_IRCOMP_R
R2203 24.9 1/16W MF-LF 1% 402
PP1V5_S0_SB_VCC1_5_B
LAYOUT NOTE: PLACE R2203 < 1/2 IN FROM SB
SPI
SPI_CLK
SPI_CS*
SPI_ARB
SPI_MOSI
SPI_MISO
USB
USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USBRBIAS*
USBRBIAS
USB_RBIAS_PN
R2204 22.6 1% 1/16W MF-LF 402
VOLTAGE=0
LAYOUT NOTE: PLACE R2204 < 1/2 IN FROM SB
EXTERNAL 0
TRACKPAD (Geyser)
EXTERNAL 1
CAMERA
EXTERNAL 2
IR
BT
AIRPORT
NOTE: USBP[0-7]P/N HAVE INTERNAL 15K PD
OC0*
OC1*
OC2*
OC3*
OC4*
OC5*/GPIO29
OC6*/GPIO30
OC7*/GPIO31
NOTE: GNT[0-3]# HAVE INT 20K PU ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
=PP3V3_S0_SB
R2299 10K 5% 1/16W MF-LF 402
NOTE: FWH_WP_L NOT USED
NOTE: TBL_L NET REMOVED
PCI_PME_FW_L
NOTE: NOT PLANNED TO GO TO LPC+ CONN
BOOT_LPC_SPI_L
R2211 1K 5% 1/16W MF-LF 402
BOM NOTE:
NO STUFF - DEFAULT
STUFF - A16 SWAP OVERRIDE
(STRAPPED TO TOP-BLOCK SWAP MODE IE SB INVERTS A16 FOR ALL CYCLES TARGETING FWH BIOS SPACE)
PCI
PCI_AD<0>
PCI_AD<1>
PCI_AD<2>
PCI_AD<3>
PCI_AD<4>
PCI_AD<5>
PCI_AD<6>
PCI_AD<7>
PCI_AD<8>
PCI_AD<9>
PCI_AD<10>
PCI_AD<11>
PCI_AD<12>
PCI_AD<13>
PCI_AD<14>
PCI_AD<15>
PCI_AD<16>
PCI_AD<17>
PCI_AD<18>
PCI_AD<19>
PCI_AD<20>
PCI_AD<21>
PCI_AD<22>
PCI_AD<23>
PCI_AD<24>
PCI_AD<25>
PCI_AD<26>
PCI_AD<27>
PCI_AD<28>
PCI_AD<29>
PCI_AD<30>
PCI_AD<31>
PCI_FRAME_L
INT I/F
INT_PIRQA_L
INT_PIRQB_L
INT_PIRQC_L
INT_PIRQD_L
MISC
NOTE: CHANGE SYMBOL TO RSVD[1-9]
TP_SB_XOR-AE5
TP_SB_XOR-AD5
TP_SB_XOR-AG4
TP_SB_XOR-AH4
TP_SB_XOR-AD9
PCI_REQ0_L
TP_PCI_GNT0_L
PCI_REQ1_L
TP_PCI_GNT1_L
PCI_REQ2_L
TP_PCI_GNT2_L
PCI_REQ3_L
PCI_GNT3_L
TP_SB_GPIO22
PCI_C_BE_L<0>
PCI_C_BE_L<1>
PCI_C_BE_L<2>
PCI_C_BE_L<3>
PCI_IRDY_L
PCI_PAR
PCI_CLK_SB
PCI_DEVSEL_L
PCI_PERR_L
PCI_LOCK_L
PCI_SERR_L
PCI_STOP_L
PCI_TRDY_L
PLT_RST_L
PCI_RST_L
TP_PCI_PME_L
SB_GPIO02
SB_GPIO03
SB_GPIO04
SB_GPIO05
TP_SB_XOR_AE9
TP_SB_XOR_AG8
TP_SB_XOR_AH8
TP_SB_RSVD9
NB_SB_SYNC_L
SB BOOT BIOS SELECT
STRAP
GNT5# R2211
GNT4# R2210
LPC (DEFAULT) 11 UNSTUFF UNSTUFF
PCI 10 UNSTUFF STUFF
SPI 01 STUFF UNSTUFF
NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)
SB: 2 OF 4
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SIZE D
DRAWING NUMBER 051-7370
REV. C
SCALE NONE
SHT 22 OF 98

NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING @ PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

=PP3V3_S0_SB_GPIO 21C3 21D3 23B2 64B6

=PP3V3_S5_SB 23A7 23B7 23D8 25C8 64A3

64A3 25C8 23D4 23B7 23A7 =PP3V3_S5_SB

R2318 10K 1/16W 402 MF-LF 5%
R2395 8.2K 1/16W 402 MF-LF 5%
R2396 10K 1/16W 402 MF-LF 5%
R2397 8.2K 1/16W 402 MF-LF 5%
R2327 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2326 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2323 NO_REBOOT_MODE 1K 1/16W 402 MF-LF 5%

RP2300 10K 5% 1/16W SM-LF

R2398 1K 1/16W 402 MF-LF 5%
R2320 10K 1/16W 402 MF-LF 5%
R2317 10K 1/16W 402 MF-LF 5%
R2316 10K 1/16W 402 MF-LF 5%

LEMENU

U2100
ICH7-M
SB
BGA
(4 OF 6)

SMB

27D8 TO SMB_CLK — C22 SMBCLK
27D8 TO SMB_DATA — B22 SMBDATA
SMB_LINK_ALERT_L — A26 LINKALERT*
SMLINK<0> — B25 SMLINK0
NOT USED — SMLINK<1> — A25 SMLINK1
PM_RI_L — A28 RI*
SB_SPKR — A19 SPKR (INT WEAK PD)
53C6 47C5 46D3 45D5 5C2 OUT PM_SUS_STAT_L — A27 SUS_STAT*
45C8 26C5 IN PM_SYSRST_L — A22 SYS_RST*
14B6 IN PM_BMBUSY_L — AB18 GPIO0/BM_BUSY*
SMB_ALERT_L — B23 GPIO11/SMBALERT*
NOTE: RESERVED FOR FUTURE

SYS GPIO

32C4 OUT PM_STPPCI_L — AC20 GPIO18/STPPCI*
32C4 OUT PM_STPCPU_L — AF21 GPIO20/STPCPU*
IN SB_GPIO26 — A21 GPIO26
23A6 BIOS_REC — B21 GPIO27
23A6 FWH_MFG_MODE — E23 GPIO28
53C6 47C6 45D5 38A5 5C2 TO PM_CLKRUN_L — AG18 GPIO32/CLKRUN*
RESERVED FOR MOBILE AZALIA DOCKING INT'F
TP_AZ_DOCK_EN_L — AC19 GPIO33/AZ_DOCK_EN*
TP_AZ_DOCK_RST_L — U2 GPIO34/AZ_DOCK_RST*
43C6 36C6 IN PCIE_WAKE_L — F20 WAKE*
53C6 47C5 45C8 5C2 TO INT_SERIRQ — AH21 SERIRQ
45B8 IN PM_THRM_L — AE20 THRM*
26A8 IN VR_PWRGD_CK410 — AD22 VRMPWRGD
TO TP_SB_GPIO6 — AC21 GPIO6
SB_RUNTIME_SCI_L — AC18 GPIO7
E21 GPIO8

PWR MNGT

SATA GPIO

AF19 SB_GPIO21 — 100 — R2302
AH18 SB_GPIO19 — 100 — R2303
AH19
AE19 SB_GPIO37 — 100 — R2305
35D2 SATA_C_DET_L IN

CLKS

AC1 CLK14 — 33A6 SB_CLK14P3M_TIMER IN
B2 CLK48 — 33C7 SB_CLK48M_USBCTLR IN
C20 SUSCLK — 68A4 SUS_CLK_SB OUT

B24 SLP_S3* — 63A7 63B8 45C5 PM_SLP_S3_L OUT
D23 SLP_S4* — 63D6 61B8 60C8 45C5 PM_SLP_S4_L OUT
F22 SLP_S5* — 46D3 45C5 PM_SLP_S5_L OUT
AA4 PWROK — 26A6 PM_SB_PWROK IN
AC22 GPIO16/DPRSLPVR — 58D8 14B7 PM_DPRSLPVR OUT
C21 TP0/BATLOW* — NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN — 45B8 PM_BATLOW_L IN
(INT 20K PU) C23 PWRBTN* — 45D8 PM_PWRBTN_L IN
C19 LAN_RST* — 45D8 PM_LAN_ENABLE IN — NOTE: SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F IN RESET STATE TO SAVE PWR
Y4 RSMRST* — 45D8 PM_RSMRST_L IN

R2319 10K 1/16W 402 MF-LF 5%
R2343 8.2K 5% 1/16W 402 MF-LF
=PP3V3_S5_SB_PM 11B5 26C5 64A3

R2399 100K 5% 1/16W 402 MF-LF

GPIO

E20 GPIO9 — 46D6 45B5 SMS_INT_L IN — NOTE: PATA_DET IS ACTUALLY CABLE TYPE DETECT
A20 GPIO10 — 45D8 SMC_SB_NMI IN
DEF=GPI F19 GPIO12 — 23B3 PATA_PWR_EN_L OUT
E19 GPIO13 — 45D5 SMC_WAKE_SCI_L IN
DEF=GPI R4 GPIO14 — 23A4 SB_GPIO14 OUT
E22 GPIO15 — SV_SET_UP 5C2 23B6 47B5
GPIO24 R3 — CRB_SV_DET 23B6
D20 GPIO25 — TP_SB_GPIO25_DO_NOT_USE
OD AD21 GPIO35 — 32B4 SB_CLK100M_SATA_OE_L OUT
AD20 GPIO38 — TO TP_SB_GPIO38
DEF=GPI AE20 GPIO39 — 23A3 SATA_C_PWR_EN_L OUT

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

R2300 0

45B8 IN SMC_RUNTIME_SCI_L
45B8 IN SMC_EXTSMI_L

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

64A3 25C8 23D8 23D4 23A7 =PP3V3_S5_SB

R2306 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2308 10K 1/16W 402 MF-LF 5%
R2307 10K 1/16W 402 MF-LF 5%
R2309 NOSTUFF 0 1/16W 402 MF-LF 5%

SV_SET_UP 5C2 23C3 47B5
CRB_SV_DET 23C3

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

64A3 25C8 23D8 23D4 23B7 =PP3V3_S5_SB

R2313 10K 1/16W 402 MF-LF 5%
R2310 10K 1/16W 402 MF-LF 5%
R2314 NOSTUFF 0 1/16W 402 MF-LF 5%
R2311 NOSTUFF 10K 1/16W 402 MF-LF 5%

FWH_MFG_MODE 23C5
BIOS_REC 23C5

=PP3V3_S0_SB_GPIO 21C3 21D3 23D5 64B6

R2390 10K 5% 1/16W MF-LF 402
R2388 10K 5% 1/16W MF-LF 402

23C3 PATA_PWR_EN_L
23B3 SATA_C_PWR_EN_L

NOSTUFF R2312 0 5% 1/16W MF-LF 402
26C3 22A6 SB_GPIO3
IDE_RESET_L 34C5

R2315 0 5% 1/16W MF-LF 402
23C3 SB_GPIO14

R2389 15K 5% 1/10W MF-LF 402

R2312,R2315 and R2389 close to SB

SB: 3 OF 4

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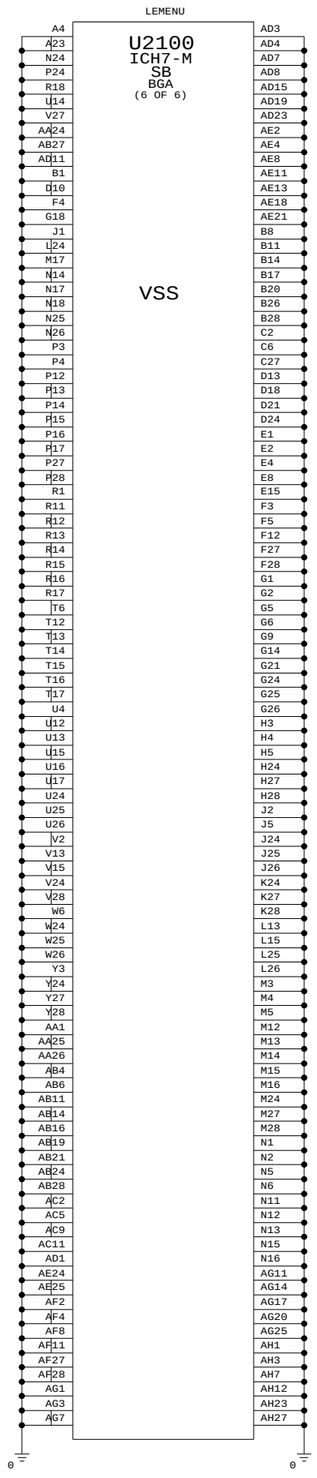
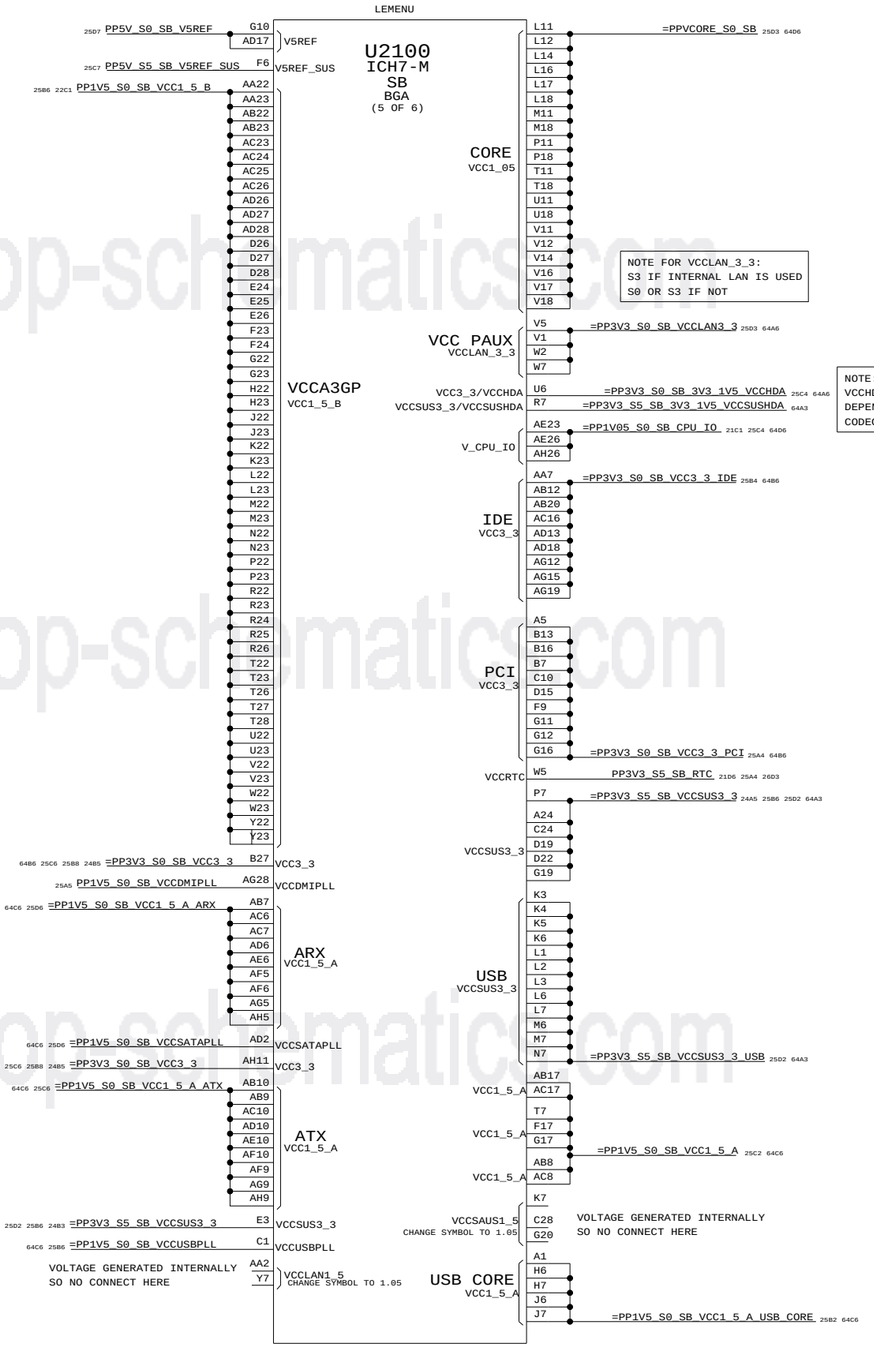
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 23 OF 98	





SB: 4 OF 4

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 24 OF 98	

ICH V5REF BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON CORE WELL INPUT)
64B6 34C8 22B5 =PP3V3_S0_SB
64D3 =PP5V_S0_SB
R2502 100 1/16W MF-LF 402 5%
D2502 BAT54DW SOT-363
PP5V_S0_SB_V5REF 24D5
VOLTAGE=5V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C2503 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE C2503 < 2.54MM OF PIN AD17 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY

ICH V5REF_SUS BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON RESUME WELL LOGIC)
64A3 23D8 23D4 23B7 23A7 =PP3V3_S5_SB
64A3 =PP5V_S5_SB
R2501 10 1/16W MF-LF 402 5%
D2502 BAT54DW SOT-363
PP5V_S5_SB_V5REF_SUS 24D5
VOLTAGE=5V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C2504 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE C2504 < 2.54MM OF PIN F6 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY

ICH VCCA3GP(VCC1_5_B BYPASS
(ICH IO,LOGIC 1.5V PWR)
25A8 64C6 =PP1V5_S0_SB
L2500 100-OHM-EMI SM-3
PP1V5_S0_SB_VCC1_5_B 22C1 24D5
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
CRITICAL
C2500 220UF 20% 2.5V POLY CASE-B2
C2505 0.1UF 10% 16V X5R 402
C2506 0.1UF 10% 16V X5R 402
C2507 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE C2500 & C2505-07 < 2.54MM OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
NEAR PINS D28, T28, AD28

ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
64B6 25C6 24B5 =PP3V3_S0_SB_VCC3_3
C2509 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE C2509 NEAR PIN B27 OF SB

ICH VCC1_5_A/ARX BYPASS
(ICH LOGIC&IO[ARX] 1.5V PWR)
64C6 24B5 =PP1V5_S0_SB_VCC1_5_A_ARX
C2511 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AG5

ICH VCCSATAPLL BYPASS
(ICH SATA PLL 1.5V PWR)
64C6 24B5 =PP1V5_S0_SB_VCCSATAPLL
C2517 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AD2

ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
64B6 25B8 24B5 =PP3V3_S0_SB_VCC3_3
C2513 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AH11

ICH VCC1_5_A/ATX BYPASS
(ICH LOGIC&IO[ATX] 1.5V PWR)
64C6 24A5 =PP1V5_S0_SB_VCC1_5_A_ATX
C2514 1UF 10% 6.3V CERM 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AG9

ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
64A3 25D2 24B3 24A5 =PP3V3_S5_SB_VCCSUS3_3
C2520 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE C2520 NEAR PIN E3 OF SB

ICH VCCUSBPLL BYPASS
(ICH USB PLL 1.5V PWR)
64C6 24A5 =PP1V5_S0_SB_VCCUSBPLL
C2515 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE C2520 NEAR PIN C1 OF SB

ICH VCCDMIPLL BYPASS
(ICH DMI PLL 1.5V PWR)
64C6 25C8 =PP1V5_S0_SB
R2500 1 1/10W 5% MF-LF 603
PP1V5_S0_SB_VCCDMIPLL_F
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
L2507 0.28-OHM 1206
PP1V5_S0_SB_VCCDMIPLL 24B5
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C2501 0.01UF 10% 16V CERM 402
C2508 10UF 20% 6.3V X5R 603
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON
SECONDARY SIDE OR 3.56MM ON PRIMARY

ICH CORE/VCC1_05 BYPASS
(ICH CORE 1.05V PWR)
PLACEMENT NOTE:
PLACE CAPS AT EDGE OF SB
=PPVCORE_S0_SB 24D3 64D6
C2518 0.1UF 10% 16V X5R 402
C2502 1UF 10% 6.3V CERM 402
CRITICAL
C2516 330UF 20% 2.5V POLY CASE-C2
PLACEHOLDER FOR 270UF

ICH VCC_PAUX/VCCLAN3_3 BYPASS
(ICH LAN I/F BUFFER 3.3V PWR)
=PP3V3_S0_SB_VCCLAN3_3 24D3 64A6
PLACEMENT NOTE:
PLACE CAP UNDER SB NEAR PINS V1,
V5, W2, OR W7
C2519 0.1UF 10% 16V X5R 402

ICH VCC3_3/VCCHDA BYPASS
(ICH INTEL HDA CORE 3.3V PWR)
64A6 24C3 =PP3V3_S0_SB_3V3_1V5_VCCHDA
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN U6
C2521 0.1UF 10% 16V X5R 402

ICH V_CPU_IO BYPASS
(ICH CPU I/O 1.05V PWR)
64D6 24C3 21C1 =PP1V05_S0_SB_CPU_IO
PLACEMENT NOTE:
PLACE NEAR PINS AE23, AE26 & AH26 OF SB
C2523 0.1UF 10% 16V X5R 402
C2522 0.1UF 10% 16V X5R 402
C2524 4.7UF 20% 6.3V CERM 603

ICH IDE/VCC3_3 BYPASS
(ICH IDE I/O 3.3V PWR)
64B6 24C3 =PP3V3_S0_SB_VCC3_3_IDE
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AA7 ... AG19
C2525 0.1UF 10% 16V X5R 402

ICH PCI/VCC3_3 BYPASS
(ICH PCI I/O 3.3V PWR)
64B6 24B3 =PP3V3_S0_SB_VCC3_3_PCI
PLACEMENT NOTE:
DISTRIBUTE IN PCI SECTION OF SB
NEAR PINS A5 ... G16
C2526 0.1UF 10% 16V X5R 402
C2527 0.1UF 10% 16V X5R 402
C2528 0.1UF 10% 16V X5R 402

ICH VCCRTC BYPASS
(ICH RTC 3.3V PWR)
26D3 24B3 21D6 =PP3V3_S5_SB_RTC
PLACEMENT NOTE:
PLACE CAPS NEAR PIN W5 OF SB
C2530 0.1UF 10% 16V X5R 402
C2529 0.1UF 10% 16V X5R 402

ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
64A3 25B6 24B3 24A5 =PP3V3_S5_SB_VCCSUS3_3
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
A24 ... G19 AND P7 OF SB
C2531 0.1UF 10% 16V X5R 402
C2534 0.1UF 10% 16V X5R 402

ICH USB/VCCSUS3_3 BYPASS
(ICH SUSPEND USB 3.3V PWR)
64A3 24B3 =PP3V3_S5_SB_VCCSUS3_3_USB
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
K3 ... N7 OF SB
C2533 0.1UF 10% 16V X5R 402
C2532 0.1UF 10% 16V X5R 402

ICH VCC1_5A BYPASS
(ICH LOGIC&IO 1.5V PWR)
64C6 24A3 =PP1V5_S0_SB_VCC1_5_A
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
AB8 AND AC8 OF SB
C2510 0.1UF 10% 16V X5R 402

ICH USB CORE/VCC1_5_A BYPASS
(ICH USB CORE 1.5V PWR)
64C6 24A3 =PP1V5_S0_SB_VCC1_5_A_USB_CORE
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS A1 ... J7
C2512 0.1UF 10% 16V X5R 402

SB: 4 OF 4

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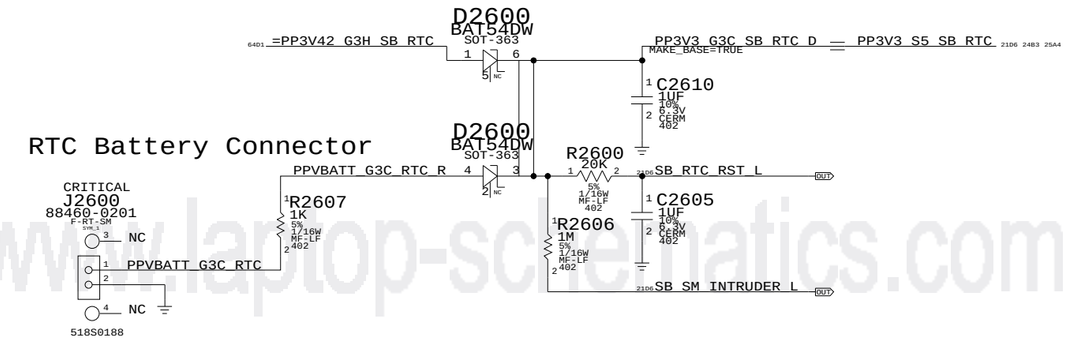
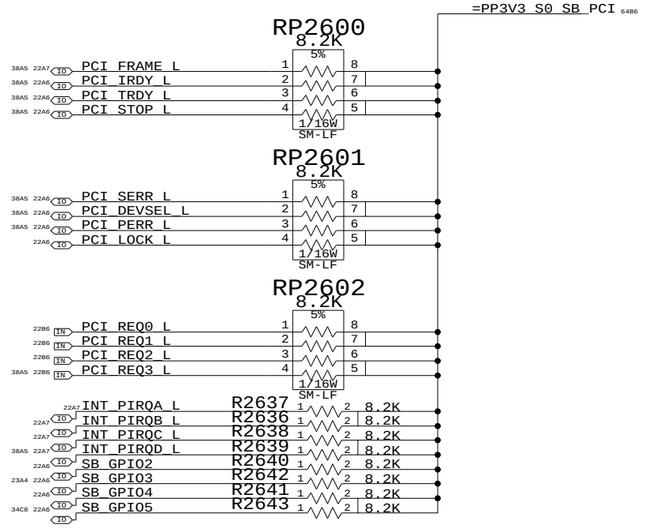
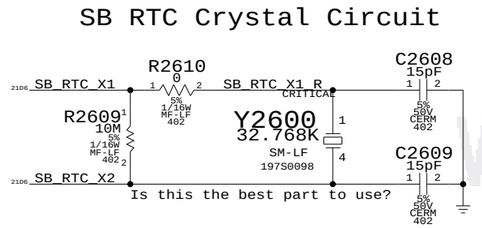
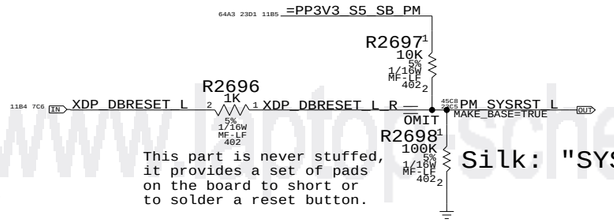
APPLE INC.

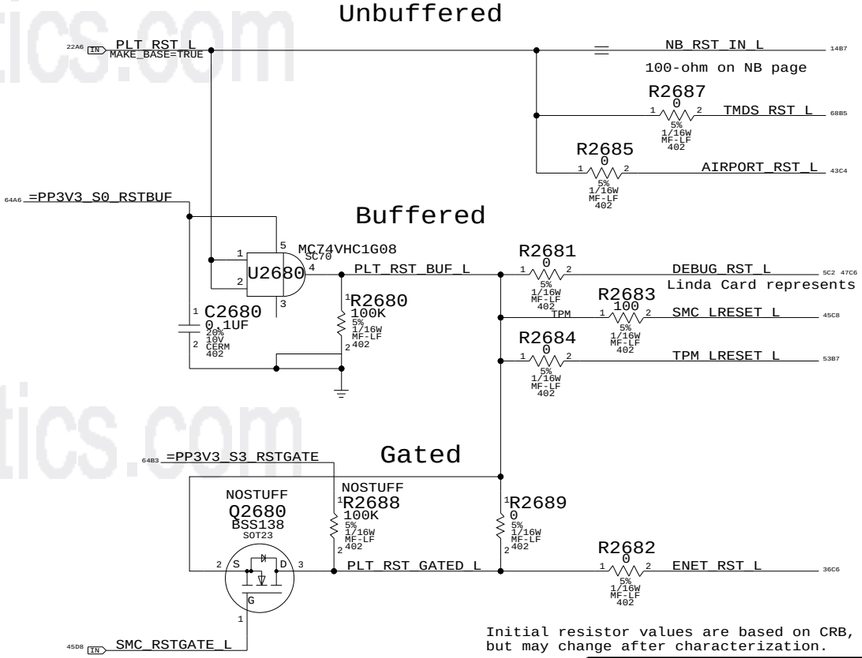
SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 25 OF 98	

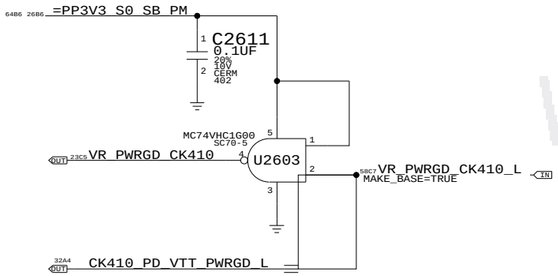


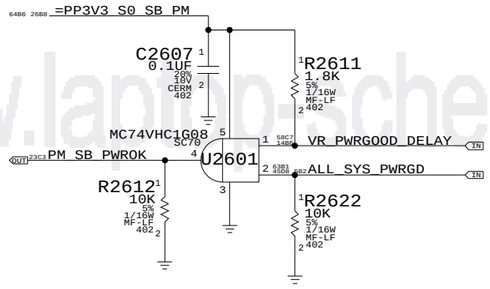








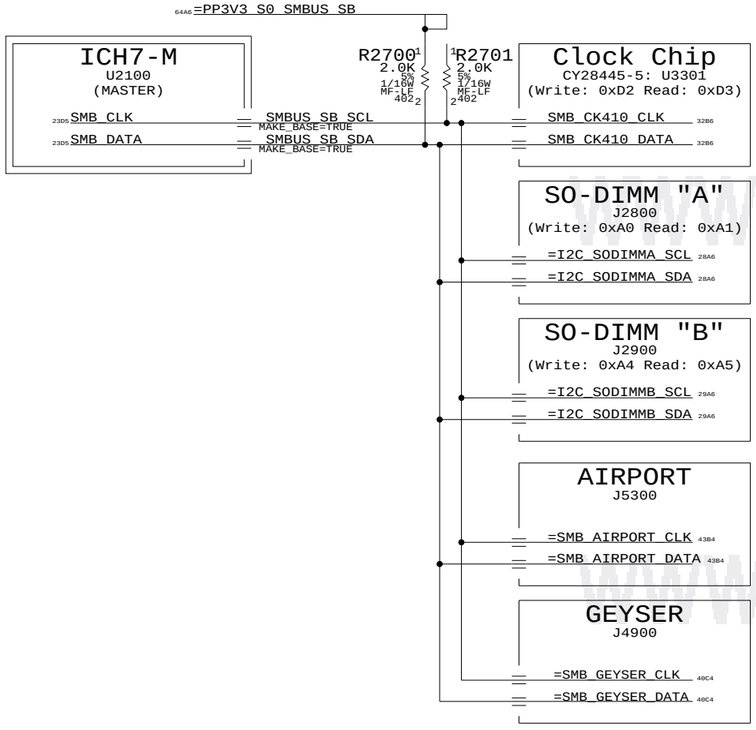




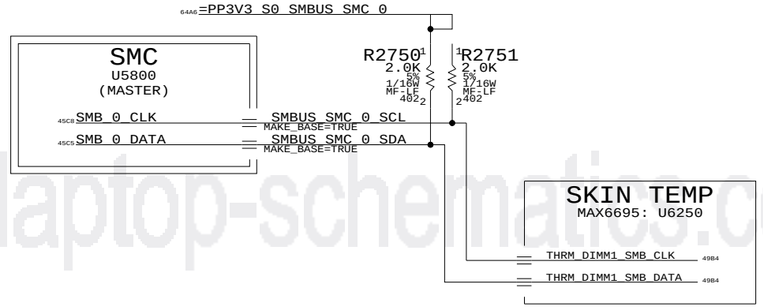
SB Misc	
SYNC_MASTER=NB	SYNC_DATE=07/26/2005

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7370	C
	SCALE: NONE	SHT 26 OF 98	

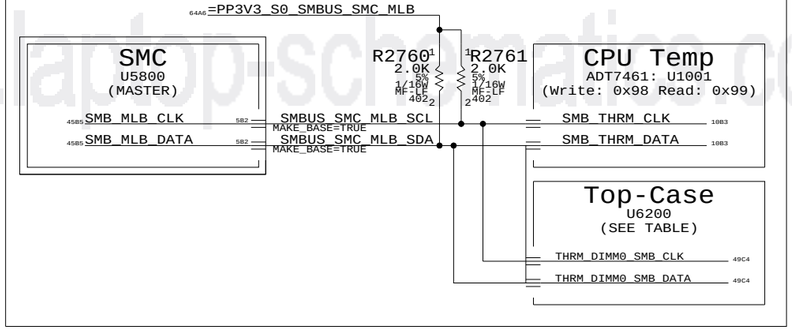
ICH7-M SMBus Connections



SMC "0" SMBus Connections

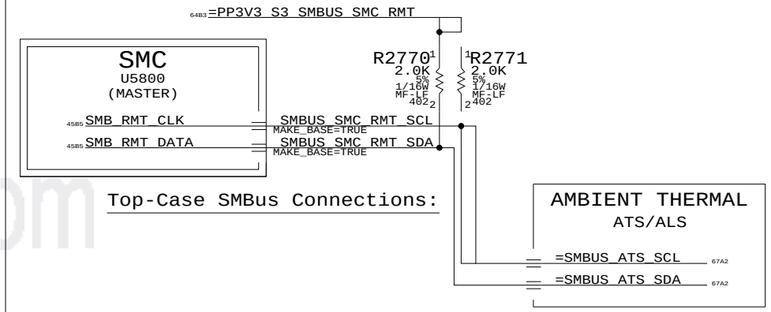


SMC "MLB" SMBus Connections

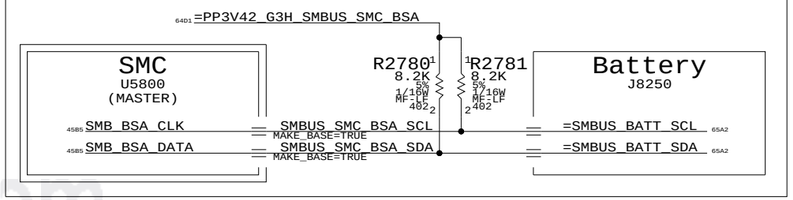


SMC "RMT" SMBus Connections

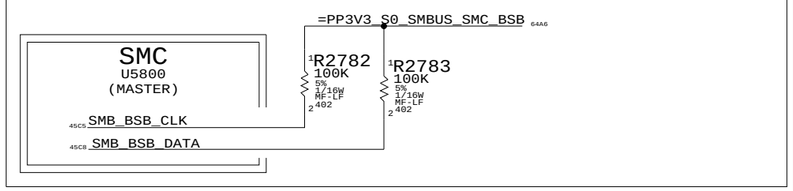
NOTE: SMC RMT bus remains powered and may be active in S3 state



SMC "Battery A" SMBus Connections



SMC "Battery B" SMBus Connections



M42 SMBUS CONNECTIONS

SYNC_MASTER=ENET SYNC_DATE=08/30/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE	SHT	OF
NONE	27	98

DIP DIMM CONN

64C3 29D6 29D4 29B2 28D4 28B2 19C8 19C7 =PP1V8_S3_MEM

28D1 MEM_VREF_A

C2820 2.2UF 20% 4V X5R 402

C2800 0.1uF 20% 16V CERM 402

OMIT CRITICAL J2801 F-RT-TH2

201 =GND_CHASSIS_DIPDIMM_CENTER 6B8 29A5

DDR2-SODIMM-STD

1	VREF		2	VSS0			
3	VSS1		4	DQ4	MEM_A_DQ<5>	15D7	
5	DQ0	15D7 MEM_A_DQ<6>	6	DQ5	MEM_A_DQ<1>	15D7	
7	DQ1	15D7 MEM_A_DQ<7>	8	VSS2			
9	VSS4		10	DM0	MEM_A_DM<0>	15D5	
11	DQS0*	15C5 MEM_A_DQS_N<0>	12	VSS5			
13	DQS0	15C5 MEM_A_DQS_P<0>	14	DQ6	MEM_A_DQ<0>	15D7	
15	VSS6		16	DQ7	MEM_A_DQ<4>	15D7	
17	DQ2	15D7 MEM_A_DQ<3>	18	VSS7			
19	DQ3	15D7 MEM_A_DQ<2>	20	DQ12	MEM_A_DQ<12>	15C7	
21	VSS8		22	DQ13	MEM_A_DQ<14>	15C7	
23	DQ8	15C7 MEM_A_DQ<13>	24	VSS9			
25	DQ9	15C7 MEM_A_DQ<8>	26	DM1	MEM_A_DM<1>	15D5	
27	VSS10		28	VSS11			
29	DQS1*	15C5 MEM_A_DQS_N<1>	30	CK0	MEM_CLK_P<0>	14D4	
31	DQS1	15C5 MEM_A_DQS_P<1>	32	CK0*	MEM_CLK_N<0>	14D4	
33	VSS12		34	VSS13			
35	DQ10	15C7 MEM_A_DQ<10>	36	DQ14	MEM_A_DQ<11>	15C7	
37	DQ11	15C7 MEM_A_DQ<9>	38	DQ15	MEM_A_DQ<15>	15C7	
39	VSS14		40	VSS15			
KEY							
41	VSS16		42	VSS17			
43	DQ16	15C7 MEM_A_DQ<24>	44	DQ20	MEM_A_DQ<29>	15C7	
45	DQ17	15C7 MEM_A_DQ<25>	46	DQ21	MEM_A_DQ<28>	15C7	
47	VSS18		48	VSS19			
49	DQS2*	15C5 MEM_A_DQS_N<3>	50	NC0	DIMM_OVERTEMP_L	6B1 29C4	
51	DQS2	15C5 MEM_A_DQS_P<3>	52	DM2	MEM_A_DM<3>	15C5	
53	VSS21		54	VSS22			
55	DQ18	15C7 MEM_A_DQ<31>	56	DQ22	MEM_A_DQ<26>	15C7	
57	DQ19	15C7 MEM_A_DQ<27>	58	DQ23	MEM_A_DQ<30>	15C7	
59	VSS23		60	VSS24			
61	DQ24	15C7 MEM_A_DQ<22>	62	DQ28	MEM_A_DQ<18>	15C7	
63	DQ25	15C7 MEM_A_DQ<19>	64	DQ29	MEM_A_DQ<23>	15C7	
65	VSS25		66	VSS26			
67	DM3	15D5 MEM_A_DM<2>	68	DQS3*	MEM_A_DQS_N<2>	15C5	
NC 69	NC1		70	DQS3	MEM_A_DQS_P<2>	15C5	
71	VSS27		72	VSS28			
73	DQ26	15C7 MEM_A_DQ<20>	74	DQ30	MEM_A_DQ<16>	15C7	
75	DQ27	15C7 MEM_A_DQ<17>	76	DQ31	MEM_A_DQ<21>	15C7	
77	VSS29		78	VSS30			
79	CKE0	30D6 14C4 MEM_CKE<0>	80	NC/CKE1	MEM_CKE<1>	14C4 30D6	
81	VDD0		82	VDD1			
NC 83	NC2		84	NC/A15	NC MEM_A_A<15>	6A4	
85	BA2	30C6 15D5 MEM_A_BS<2>	86	NC/A14	NC MEM_A_A<14>	6A4	
87	VDD2		88	VDD3			
89	A12	30C6 15B5 MEM_A_A<12>	90	A11	MEM_A_A<11>	15B5 30C6	
91	A9	30C6 15B5 MEM_A_A<9>	92	A7	MEM_A_A<7>	15B5 30C6	
93	A8	30C6 15B5 MEM_A_A<8>	94	A6	MEM_A_A<6>	15B5 30C6	
95	VDD4		96	VDD5			
97	A5	30C6 15B5 MEM_A_A<5>	98	A4	MEM_A_A<4>	15B5 30C6	
99	A3	30C6 15B5 MEM_A_A<3>	100	A2	MEM_A_A<2>	15C5 30C6	
101	A1	30C6 15C5 MEM_A_A<1>	102	A0	MEM_A_A<0>	15C5 30C6	
103	VDD6		104	VDD7			
105	A10/AP	30C6 15B5 MEM_A_A<10>	106	BA1	MEM_A_BS<1>	15D5 30C6	
107	BA0	30C6 15D5 MEM_A_BS<0>	108	RAS*	MEM_A_RAS_L	15B5 30B6	
109	WE*	30B6 15B5 MEM_A_WE_L	110	S0*	MEM_CS_L<0>	14C4 30D6	
111	VDD8		112	VDD9			
113	CAS*	30B6 15D5 MEM_A_CAS_L	114	ODT0	MEM_ODT<0>	14C4 30D6	
115	NC/S1*	30D6 14C4 MEM_CS_L<1>	116	NC/A13	MEM_A_A<13>	15B5 30C6	
117	VDD10		118	VDD11			
119	NC/ODT1	30D6 14C4 MEM_ODT<1>	120	NC3	NC		
121	VSS31		122	VSS32			
123	DQ32	15B7 MEM_A_DQ<37>	124	DQ36	MEM_A_DQ<36>	15B7	
125	DQ33	15C7 MEM_A_DQ<32>	126	DQ37	MEM_A_DQ<34>	15B7	
127	VSS33		128	VSS34			
129	DQS4*	15C5 MEM_A_DQS_N<4>	130	DM4	MEM_A_DM<4>	15C5	
131	DQS4	15C5 MEM_A_DQS_P<4>	132	VSS35			
133	VSS36		134	DQ38	MEM_A_DQ<35>	15B7	
135	DQ34	15B7 MEM_A_DQ<38>	136	DQ39	MEM_A_DQ<33>	15C7	
137	DQ35	15B7 MEM_A_DQ<39>	138	VSS37			
139	VSS38		140	DQ44	MEM_A_DQ<40>	15B7	
141	DQ40	15B7 MEM_A_DQ<44>	142	DQ45	MEM_A_DQ<45>	15B7	
143	DQ41	15B7 MEM_A_DQ<41>	144	VSS39			
145	VSS40		146	DQS5*	MEM_A_DQS_N<5>	15C5	
147	DM5	15C5 MEM_A_DM<5>	148	DQS5	MEM_A_DQS_P<5>	15C5	
149	VSS41		150	VSS42			
151	DQ42	15B7 MEM_A_DQ<47>	152	DQ46	MEM_A_DQ<42>	15B7	
153	DQ43	15B7 MEM_A_DQ<43>	154	DQ47	MEM_A_DQ<46>	15B7	
155	VSS43		156	VSS44			
157	DQ48	15A7 MEM_A_DQ<63>	158	DQ52	MEM_A_DQ<60>	15A7	
159	DQ49	15B7 MEM_A_DQ<56>	160	DQ53	MEM_A_DQ<61>	15A7	
161	VSS45		162	VSS46			
NC 163	NC_TEST		164	CK1	MEM_CLK_P<1>	14D4	
165	VSS47		166	CK1*	MEM_CLK_N<1>	14D4	
167	DQS6*	15C5 MEM_A_DQS_N<7>	168	VSS48			
169	DQS6	15C5 MEM_A_DQS_P<7>	170	DM6	MEM_A_DM<7>	15C5	
171	VSS49		172	VSS50			
173	DQ50	15B7 MEM_A_DQ<58>	174	DQ54	MEM_A_DQ<62>	15A7	
175	DQ51	15B7 MEM_A_DQ<57>	176	DQ55	MEM_A_DQ<59>	15B7	
177	VSS51		178	VSS52			
179	DQ56	15B7 MEM_A_DQ<48>	180	DQ60	MEM_A_DQ<51>	15B7	
181	DQ57	15B7 MEM_A_DQ<49>	182	DQ61	MEM_A_DQ<53>	15B7	
183	VSS53		184	VSS54			
185	DM7	15C5 MEM_A_DM<6>	186	DQS7*	MEM_A_DQS_N<6>	15C5	
187	VSS55		188	DQS7	MEM_A_DQS_P<6>	15C5	
189	DQ58	15B7 MEM_A_DQ<52>	190	VSS56			
191	DQ59	15B7 MEM_A_DQ<55>	192	DQ62	MEM_A_DQ<50>	15B7	
193	VSS57		194	DQ63	MEM_A_DQ<54>	15B7	
195	SDA	27C6 =I2C_SODIMMA_SDA	196	VSS58			
197	SCL	27D6 =I2C_SODIMMA_SCL	198	SA0			
199	VDDSPD		200	SA1			

64A6 29A7 29A3 =PPSPD_S0_MEM

C2822 2.2UF 20% 4V X5R 402

C2821 0.1uF 20% 10V CERM 402

516-0135

202 =GND_CHASSIS_DIPDIMM_LEFT 6D8

ADDR=0xA0(WR)/0xA1(RD)

DDR2 VRef

One 0.1uF per connector

64C6 61C2 29D2 19D7 16B6 14C2 =PP1V8_S3_MEM_NB

R2800 1K 1% 1/16W MF-LF 402

MEM_VREF_A 28D7

VOLTAGE=0.9V
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

R2801 1K 1% 1/16W MF-LF 402

Yellow uses 10K divider and TLV2463
to drive MCH and DIMM connectors.
(See Capell Valley pg 47)

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

DDR2 Bypass Caps

(For return current)

64C3 29D6 29D4 29B2 28D6 28D4 19C8 19C7 =PP1V8_S3_MEM

C2809 4.7uF 20% 6.3V CERM 603

C2810 0.1uF 20% 10V CERM 402

C2811 0.1uF 20% 10V CERM 402

C2812 0.1uF 20% 10V CERM 402

C2813 0.1uF 20% 10V CERM 402

C2814 0.1uF 20% 10V CERM 402

C2815 0.1uF 20% 10V CERM 402

C2816 1uF 10% 6.3V CERM 402

C2817 1uF 10% 6.3V CERM 402

C2830 1uF 10% 6.3V CERM 402

C2831 1uF 10% 6.3V CERM 402

C2832 1uF 10% 6.3V CERM 402

The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps,
when they get cheaper.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516-0149	1	CONN,200P STD SODIMM OLD REV	J2801	CRITICAL	PVT-DIMM
516-0154	1	CONN,200P STD SODIMM NEW REV 3.5	J2801	CRITICAL	POST-RAMP-DIMM35

DDR2 SO-DIMM Connector A

SYNC_MASTER=MEMORY SYNC_DATE=06/20/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 28 OF 98	

DDR2 VREF (FOR CONNECTOR B)

One 0.1uF per connector

64C6 61C2 28D2 19D7 16B6 14C2 =PP1V8_S3_MEM_NB

R2901 1K 1% 1/16W MF-LF 402

MEM_VREF_B 29D7
VOLTAGE=0.9V
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

R2902 1K 1% 1/16W MF-LF 402

Yellow uses 10K divider and TLV2463
to drive MCH and DIMM connectors.
(See Capell Valley pg 47)

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

DDR2 Bypass Caps

(For return current)

64C3 29D6 29D4 28D6 28D4 28B2 19C8 19C7 =PP1V8_S3_MEM

C2909 4.7uF 20% 6.3V CERM 603

C2910 0.1uF 20% 10V CERM 402
C2911 0.1uF 20% 10V CERM 402
C2912 0.1uF 20% 10V CERM 402
C2913 0.1uF 20% 10V CERM 402

C2914 0.1uF 20% 10V CERM 402
C2915 0.1uF 20% 10V CERM 402
C2916 1uF 10% 6.3V CERM 402
C2917 1uF 10% 6.3V CERM 402

C2930 1uF 10% 6.3V CERM 402
C2931 1uF 10% 6.3V CERM 402
C2932 1uF 10% 6.3V CERM 402

The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps,
when they get cheaper.

29D1 MEM_VREF_B

C2920 2.2UF 20% 4V X5R 402

C2900 0.1uF 20% 10V CERM 402

64C3 29D4 29B2 28D6 28D4 28B2 19C8 19C7 =PP1V8_S3_MEM

DIP DIMM CONN

J2901 (201) OMIT CRITICAL — F-RT-TH2 — DDR2-SODIMM-STD

=GND_CHASSIS_DIPDIMM_RIGHT 6B8

1	VREF		2	VSS0	
3	VSS1		4	DQ4	MEM_B_DQ<0> 15D4
5	DQ0	15D4 MEM_B_DQ<1>	6	DQ5	MEM_B_DQ<4> 15D4
7	DQ1	15D4 MEM_B_DQ<5>	8	VSS2	
9	VSS4		10	DM0	MEM_B_DM<0> 15D2
11	DQS0*	15C2 MEM_B_DQS_N<0>	12	VSS5	
13	DQS0	15C2 MEM_B_DQS_P<0>	14	DQ6	MEM_B_DQ<6> 15D4
15	VSS6		16	DQ7	MEM_B_DQ<7> 15D4
17	DQ2	15D4 MEM_B_DQ<2>	18	VSS7	
19	DQ3	15D4 MEM_B_DQ<3>	20	DQ12	MEM_B_DQ<15> 15C4
21	VSS8		22	DQ13	MEM_B_DQ<14> 15C4
23	DQ8	15C4 MEM_B_DQ<12>	24	VSS9	
25	DQ9	15C4 MEM_B_DQ<13>	26	DM1	MEM_B_DM<1> 15D2
27	VSS10		28	VSS11	
29	DQS1*	15C2 MEM_B_DQS_N<1>	30	CK0	MEM_CLK_P<3> 14D4
31	DQS1	15C2 MEM_B_DQS_P<1>	32	CK0*	MEM_CLK_N<3> 14D4
33	VSS12		34	VSS13	
35	DQ10	15C4 MEM_B_DQ<8>	36	DQ14	MEM_B_DQ<11> 15C4
37	DQ11	15C4 MEM_B_DQ<10>	38	DQ15	MEM_B_DQ<9> 15C4
39	VSS14		40	VSS15	
KEY					
41	VSS16		42	VSS17	
43	DQ16	15C4 MEM_B_DQ<17>	44	DQ20	MEM_B_DQ<21> 15C4
45	DQ17	15C4 MEM_B_DQ<20>	46	DQ21	MEM_B_DQ<16> 15C4
47	VSS18		48	VSS19	
49	DQS2*	15C2 MEM_B_DQS_N<2>	50	NC0	DIMM_OVERTEMP_L 6B1 28C4
51	DQS2	15C2 MEM_B_DQS_P<2>	52	DM2	MEM_B_DM<2> 15D2
53	VSS21		54	VSS22	
55	DQ18	15C4 MEM_B_DQ<22>	56	DQ22	MEM_B_DQ<23> 15C4
57	DQ19	15C4 MEM_B_DQ<18>	58	DQ23	MEM_B_DQ<19> 15C4
59	VSS23		60	VSS24	
61	DQ24	15C4 MEM_B_DQ<29>	62	DQ28	MEM_B_DQ<25> 15C4
63	DQ25	15C4 MEM_B_DQ<27>	64	DQ29	MEM_B_DQ<24> 15C4
65	VSS25		66	VSS26	
67	DM3	15C2 MEM_B_DM<3>	68	DQS3*	MEM_B_DQS_N<3> 15C2
69	NC1	NC	70	DQS3	MEM_B_DQS_P<3> 15C2
71	VSS27		72	VSS28	
73	DQ26	15C4 MEM_B_DQ<30>	74	DQ30	MEM_B_DQ<28> 15C4
75	DQ27	15C4 MEM_B_DQ<31>	76	DQ31	MEM_B_DQ<26> 15C4
77	VSS29		78	VSS30	
79	CKE0	30D6 14C4 MEM_CKE<2>	80	NC/CKE1	MEM_CKE<3> 14C4 30D6
81	VDD0		82	VDD1	
83	NC2	NC	84	NC/A15	MEM_B_A<15> 6A4
85	BA2	30A6 15D2 MEM_B_BS<2>	86	NC/A14	MEM_B_A<14> 6A4
87	VDD2		88	VDD3	
89	A12	30A5 15B2 MEM_B_A<12>	90	A11	MEM_B_A<11> 15B2 30A5
91	A9	30B5 15B2 MEM_B_A<9>	92	A7	MEM_B_A<7> 15B2 30B5
93	A8	30B5 15B2 MEM_B_A<8>	94	A6	MEM_B_A<6> 15B2 30B5
95	VDD4		96	VDD5	
97	A5	30B5 15B2 MEM_B_A<5>	98	A4	MEM_B_A<4> 15B2 30B5
99	A3	30B5 15B2 MEM_B_A<3>	100	A2	MEM_B_A<2> 15C2 30B5
101	A1	30B5 15C2 MEM_B_A<1>	102	A0	MEM_B_A<0> 15C2 30B5
103	VDD6		104	VDD7	
105	A10/AP	30B5 15B2 MEM_B_A<10>	106	BA1	MEM_B_BS<1> 15D2 30A6
107	BA0	30A6 15D2 MEM_B_BS<0>	108	RAS*	MEM_B_RAS_L 15B2 30A6
109	WE*	30A6 15B2 MEM_B_WE_L	110	S0*	MEM_CS_L<2> 14C4 30D6
111	VDD8		112	VDD9	
113	CAS*	30A6 15D2 MEM_B_CAS_L	114	ODT0	MEM_ODT<2> 14C4 30D6
115	NC/S1*	30D6 14C4 MEM_CS_L<3>	116	NC/A13	MEM_B_A<13> 15B2 30A5
117	VDD10		118	VDD11	
119	NC/ODT1	30D6 14C4 MEM_ODT<3>	120	NC3	NC
121	VSS31		122	VSS32	
123	DQ32	15A4 MEM_B_DQ<58>	124	DQ36	MEM_B_DQ<63> 15A4
125	DQ33	15A4 MEM_B_DQ<62>	126	DQ37	MEM_B_DQ<59> 15B4
127	VSS33		128	VSS34	
129	DQS4*	15C2 MEM_B_DQS_N<7>	130	DM4	MEM_B_DM<7> 15C2
131	DQS4	15C2 MEM_B_DQS_P<7>	132	VSS35	
133	VSS36		134	DQ38	MEM_B_DQ<61> 15A4
135	DQ34	15B4 MEM_B_DQ<57>	136	DQ39	MEM_B_DQ<56> 15B4
137	DQ35	15A4 MEM_B_DQ<60>	138	VSS37	
139	VSS38		140	DQ44	MEM_B_DQ<53> 15B4
141	DQ40	15B4 MEM_B_DQ<55>	142	DQ45	MEM_B_DQ<48> 15B4
143	DQ41	15B4 MEM_B_DQ<50>	144	VSS39	
145	VSS40		146	DQS5*	MEM_B_DQS_N<6> 15C2
147	DM5	15C2 MEM_B_DM<6>	148	DQS5	MEM_B_DQS_P<6> 15C2
149	VSS41		150	VSS42	
151	DQ42	15B4 MEM_B_DQ<52>	152	DQ46	MEM_B_DQ<54> 15B4
153	DQ43	15B4 MEM_B_DQ<49>	154	DQ47	MEM_B_DQ<51> 15B4
155	VSS43		156	VSS44	
157	DQ48	15C4 MEM_B_DQ<32>	158	DQ52	MEM_B_DQ<33> 15C4
159	DQ49	15B4 MEM_B_DQ<37>	160	DQ53	MEM_B_DQ<36> 15B4
161	VSS45		162	VSS46	
163	NC_TEST	NC	164	CK1	MEM_CLK_P<2>
165	VSS47		166	CK1*	MEM_CLK_N<2> 14D4
167	DQS6*	15C2 MEM_B_DQS_N<4>	168	VSS48	
169	DQS6	15C2 MEM_B_DQS_P<4>	170	DM6	MEM_B_DM<4> 15C2
171	VSS49		172	VSS50	
173	DQ50	15B4 MEM_B_DQ<38>	174	DQ54	MEM_B_DQ<35> 15B4
175	DQ51	15B4 MEM_B_DQ<34>	176	DQ55	MEM_B_DQ<39> 15B4
177	VSS51		178	VSS52	
179	DQ56	15B4 MEM_B_DQ<45>	180	DQ60	MEM_B_DQ<40> 15B4
181	DQ57	15B4 MEM_B_DQ<44>	182	DQ61	MEM_B_DQ<42> 15B4
183	VSS53		184	VSS54	
185	DM7	15C2 MEM_B_DM<5>	186	DQS7*	MEM_B_DQS_N<5> 15C2
187	VSS55		188	DQS7	MEM_B_DQS_P<5> 15C2
189	DQ58	15B4 MEM_B_DQ<41>	190	VSS56	
191	DQ59	15B4 MEM_B_DQ<43>	192	DQ62	MEM_B_DQ<46> 15B4
193	VSS57		194	DQ63	MEM_B_DQ<47> 15B4
195	SDA	27C6 =I2C_SODIMMB_SDA	196	VSS58	
197	SCL	27C6 =I2C_SODIMMB_SCL	198	SA0	
199	VDDSPD		200	SA1	J2900_SA1

516-0135

202 =GND_CHASSIS_DIPDIMM_CENTER 6B8 28D5

ADDR=0xA4(WR)/0xA5(RD)

64A6 29A3 28A7 =PPSPD_S0_MEM

C2922 2.2UF 20% 4V X5R 402

C2921 0.1uF 20% 10V CERM 402

=PPSPD_S0_MEM 28A7 29A7 64A6

R2900 10K 5% 1/16W MF-LF 402

Resistor prevents pwr-gnd short

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516-0149	1	CONN,200P STD SODIMM OLD REV	J2901	CRITICAL	PVT-DIMM
516-0154	1	CONN,200P STD SODIMM NEW REV 3.5	J2901	CRITICAL	POST-RAMP-DIMM35

DDR2 SO-DIMM Connector B

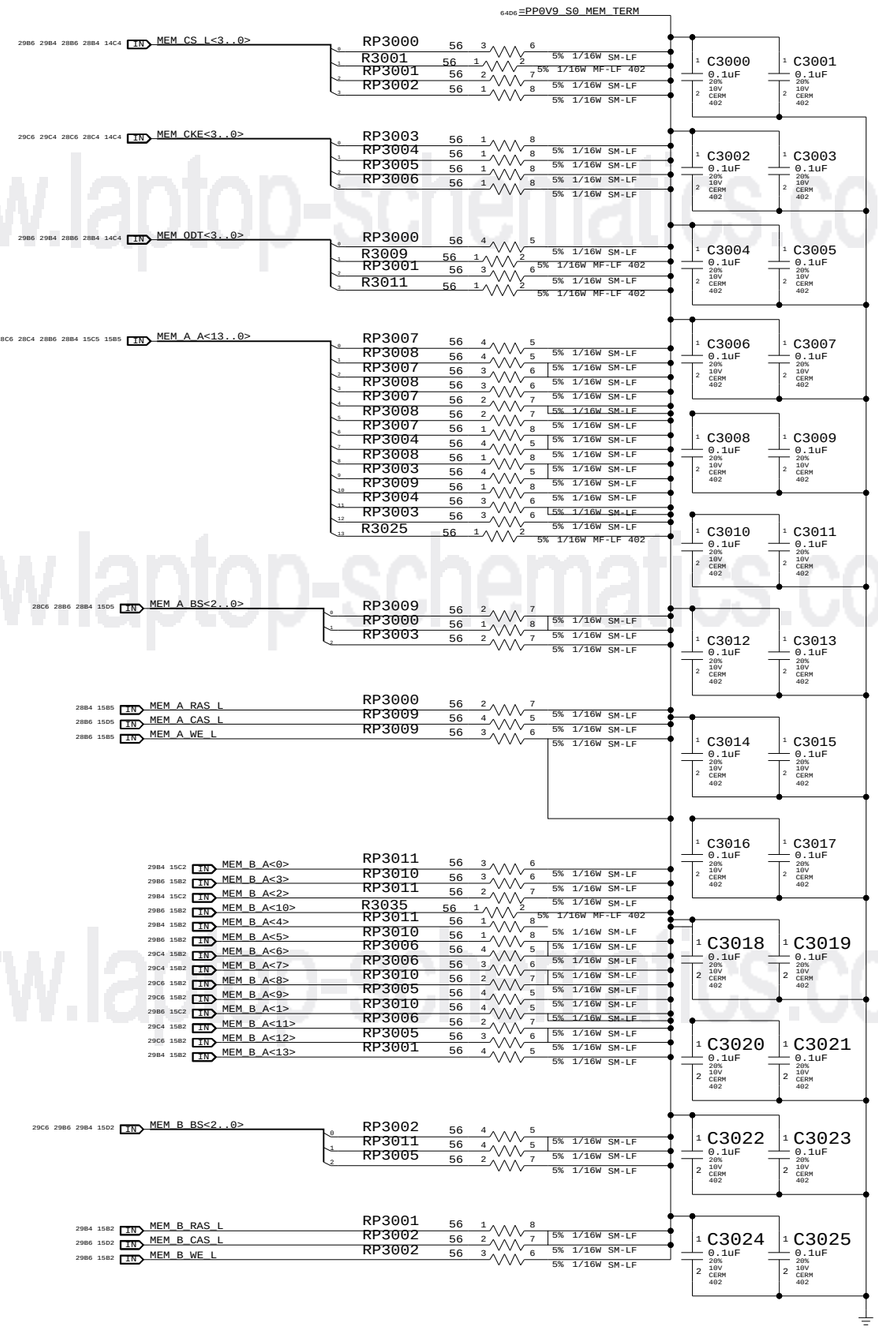
SYNC_MASTER=MEMORY SYNC_DATE=06/20/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE	SHT	OF
NONE	29	98

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



LAYOUT NOTE:PLACE ONE CAP CLOSE TO EVERY TWO PULLUP RESISTORS TERMINATED TO PP0V9_S0_MEM_TERM

Memory Active Termination

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 30 OF 98	

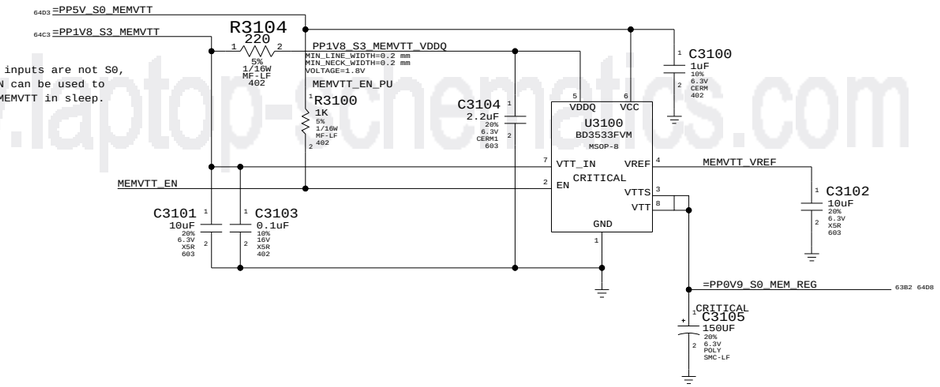
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator

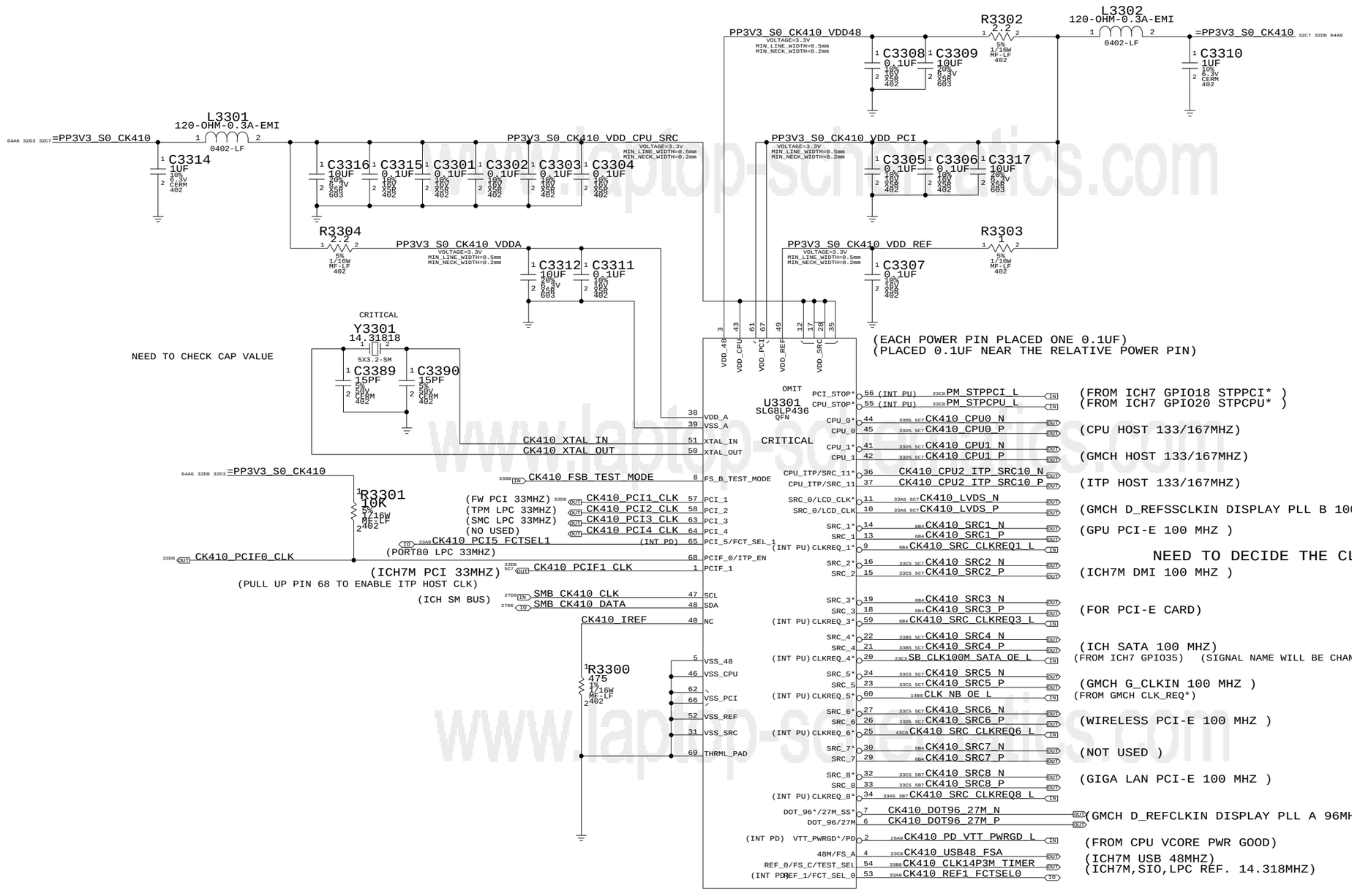


Memory Vtt Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 31 OF 98	



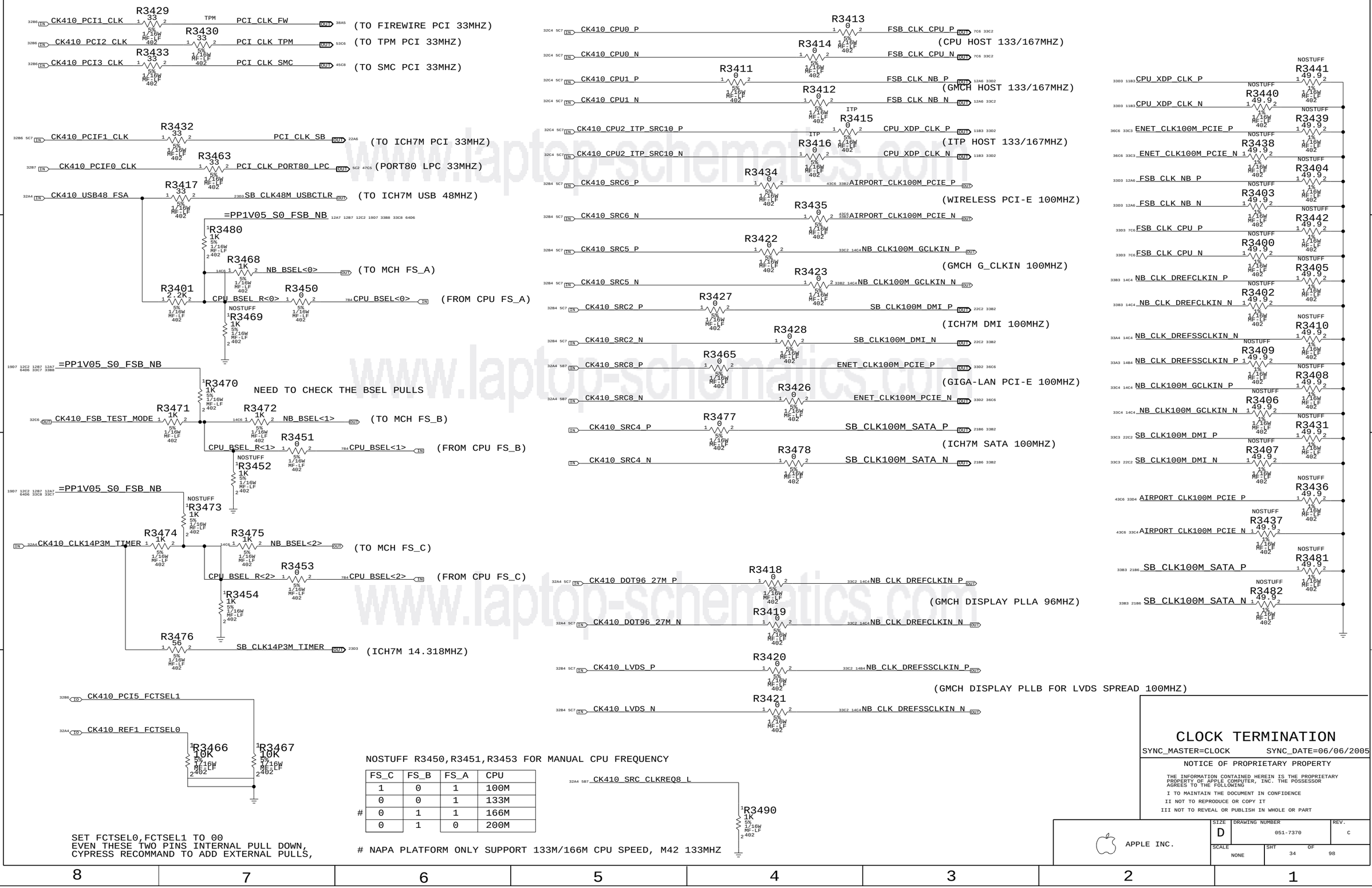
FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

CLOCKS

SYNC_MASTER=CLOCK SYNC_DATE=06/03/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 33 OF 98	



FS_C	FS_B	FS_A	CPU
1	0	1	100M
0	0	1	133M
# 0	1	1	166M
0	1	0	200M

=PP3V3_S0_SB
64B6 25D8 22B5

R3876 10K 5% 1/16W MF-LF 402

SB_GPIO5 IS PULLED HIGH

SB_GPIO5
26C3 22A6

ODD_PWR_EN_L
MAKE_BASE=TRUE

Q3875 2N7002DW-X-F SOT-363

C3875 0.47UF 10% 6.3V CERM-X5R 402

R3877 100K 5% 1/16W MF-LF 402

ODD_PWR_EN_SLOW_START

ODD detect need less than 100ms include OS latency

=PP5V_S5_PATA
64A3

R3865 6.2K 5% 1/16W MF-LF 402

Q3810 FDC638P SM-LF

C3876 0.1UF 20% 10V CERM 402

R3825 10K 5% 1/16W MF-LF 402

ODD_PWR_EN_SLOW_START_L

ODD_PWR_EN_SLOW_START_L_R

Q3875 2N7002DW-X-F SOT-363

=PP5V_S0_IDE_PATA

PP5V_S0_IDE_PATA
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.35MM
MIN_NECK_WIDTH=0.25MM

NOSTUFF
R3824 10K 5% 1/16W MF-LF 402

R3851 4.7K 5% 1/16W MF-LF 402

Per ATA Spec

CRITICAL
J3801
5-1775184-0
M-ST-SM

	51	NC	
NC	2	1	NC
NC	4	3	
IDE_RESET_L	6	5	IDE_PDD<8>
IDE_PDD<7>	8	7	IDE_PDD<9>
IDE_PDD<6>	10	9	IDE_PDD<10>
IDE_PDD<5>	12	11	IDE_PDD<11>
IDE_PDD<4>	14	13	IDE_PDD<12>
IDE_PDD<3>	16	15	IDE_PDD<13>
IDE_PDD<2>	18	17	IDE_PDD<14>
IDE_PDD<1>	20	19	IDE_PDD<15>
IDE_PDD<0>	22	21	
	24	23	IDE_PDIOR_L
IDE_PDIOW_L	26	25	
IDE_PDIORDY	28	27	IDE_PDDACK_L
IDE_IRQ14	30	29	SMC_ODD_DETECT
IDE_PDA<1>	32	31	NC
IDE_PDA<0>	34	33	IDE_PDA<2>
IDE_PDCS1_L	36	35	IDE_PDCS3_L
NC	38	37	
	40	39	
	42	41	
	44	43	
	46	45	
	48	47	
NC	50	49	NC
		52	NC

516S0339

=PP3V3_S0_PATA
64A6

R3853 33K 5% 1/16W MF-LF 402

Indicates disk presence, to SMC

NO STUFF
C3804 10pF 5% 50V CERM 402

IDE_CSEL_PD

IDE_PDDREQ

R3858 0 5% 1/16W MF-LF 402
PER ATA SPEC

R3859 6.2K 5% 1/16W MF-LF 402
PER ATA7 SPEC

NOSTUFF
C3805 0.1uF 20% 10V CERM 402

NOSTUFF
C3806 10uF 20% 6.3V X5R 603

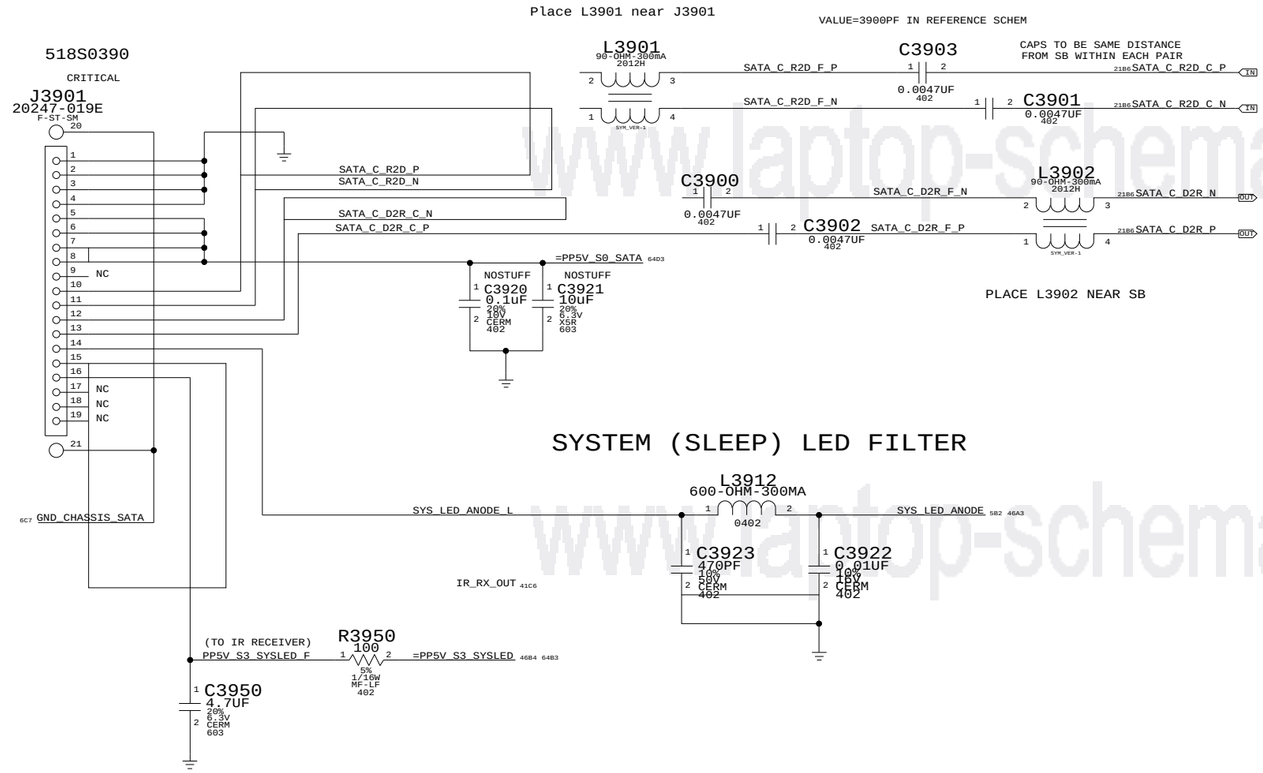
PLACE C3805/C3806 CLOSE TO JC901 FOR PP5V_PATA.
APPLY A WIDE TRACE SHAPE FROM JC901 TO C3805/C3806.
MIN_NECK & MIN_LINE_WIDTH
ARE CONTROLLED BY PP5V_RUN 1MM / 0.6MM.

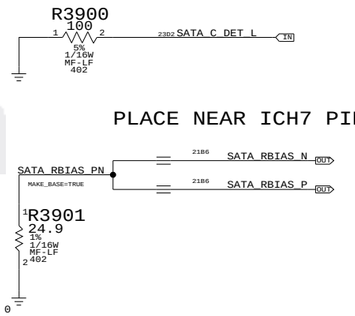
PATA CONNECTOR

APPLE INC.

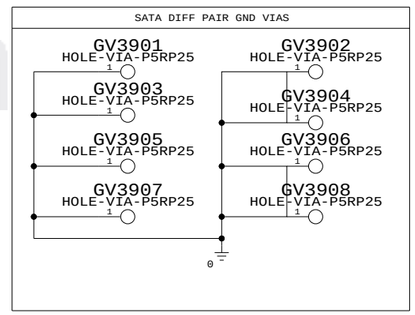
SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 38 OF 98	

SATA CONNECTOR





SYSTEM (SLEEP) LED FILTER



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0227	155S0164	?	L3901,L3902	KEEP MAG.LAYER IN BOM

SATA CONNECTOR

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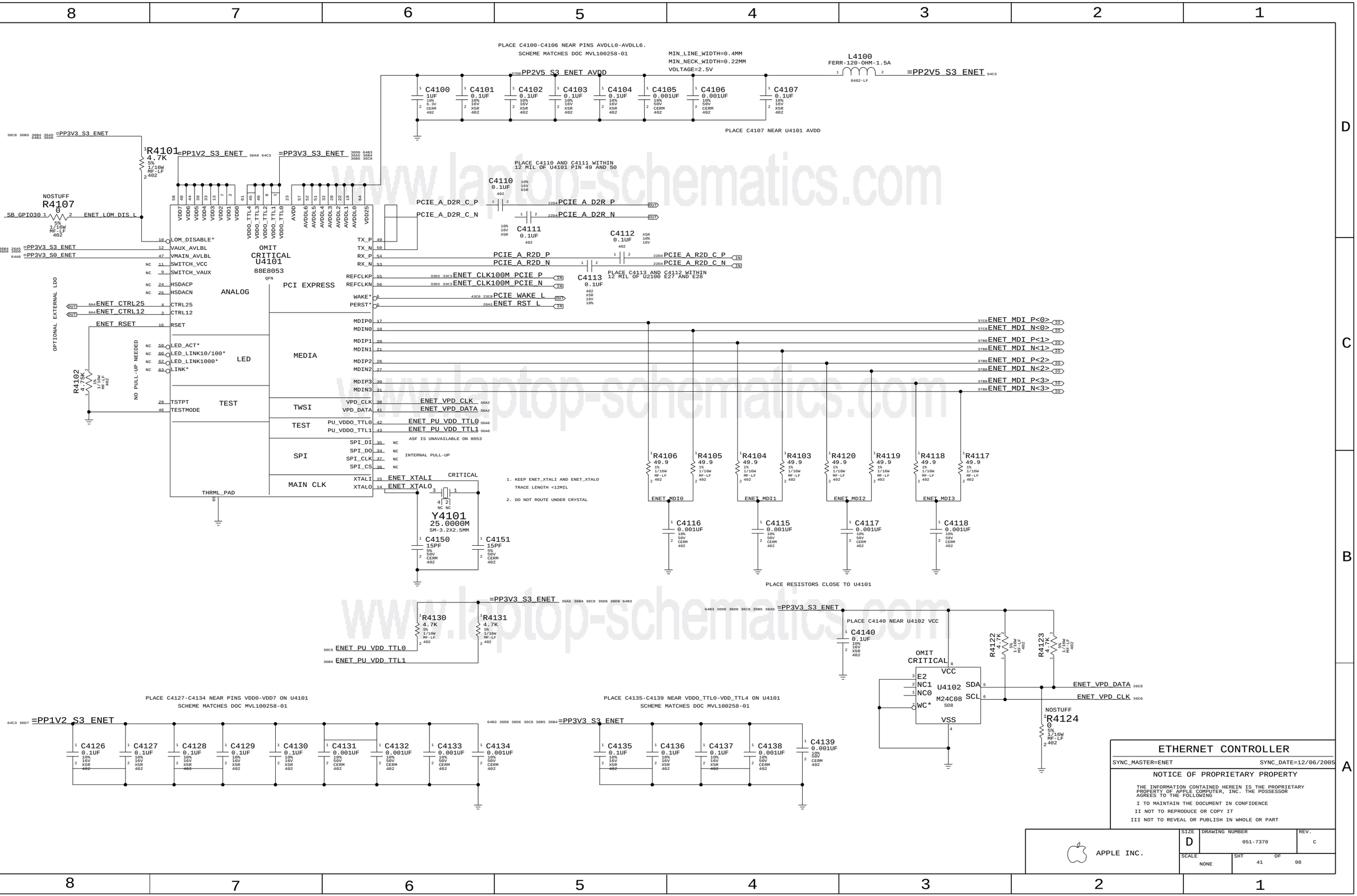
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 39 OF 98	


PLACE C4100-C4106 NEAR PINS AVDLL0-AVDLL6.
SCHEME MATCHES DOC MVL100258-01
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.22MM
VOLTAGE=2.5V
PP2V5_S3_ENET_AVDD
L4100
FERR-120-OHM-1.5A
=PP2V5_S3_ENET
C4100 1UF
C4101 0.1UF
C4102 0.1UF
C4103 0.1UF
C4104 0.1UF
C4105 0.001UF
C4106 0.001UF
C4107 0.1UF
PLACE C4107 NEAR U4101 AVDD
=PP3V3_S3_ENET
R4101 4.7K
=PP1V2_S3_ENET
NOSTUFF
R4107 0
SB_GPIO30
ENET_LOM_DIS_L
PLACE C4110 AND C4111 WITHIN
12 MIL OF U4101 PIN 49 AND 50
C4110 0.1UF
C4111 0.1UF
PCIE_A_D2R_C_P
PCIE_A_D2R_C_N
PCIE_A_D2R_P
PCIE_A_D2R_N
C4112 0.1UF
C4113 0.1UF
PLACE C4113 AND C4112 WITHIN
12 MIL OF U2100 E27 AND E28
PCIE_A_R2D_P
PCIE_A_R2D_N
PCIE_A_R2D_C_P
PCIE_A_R2D_C_N
OMIT
CRITICAL
U4101
88E8053
QFN
LOM_DISABLE*
VAUX_AVLBL
VMAIN_AVLBL
SWITCH_VCC
SWITCH_VAUX
HSDACP
HSDACN
CTRL25
CTRL12
RSET
LED_ACT*
LED_LINK10/100*
LED_LINK1000*
LINK*
TSTPT
TESTMODE
TX_P
TX_N
RX_P
RX_N
REFCLKP
REFCLKN
WAKE*
PERST*
ENET_CLK100M_PCIE_P
ENET_CLK100M_PCIE_N
PCIE_WAKE_L
ENET_RST_L
MDIP0
MDIN0
MDIP1
MDIN1
MDIP2
MDIN2
MDIP3
MDIN3
ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>
VPD_CLK
VPD_DATA
ENET_VPD_CLK
ENET_VPD_DATA
PU_VDDO_TTL0
PU_VDDO_TTL1
ENET_PU_VDD_TTL0
ENET_PU_VDD_TTL1
ASF IS UNAVAILABLE ON 8053
SPI_DI
SPI_DO
SPI_CLK
SPI_CS
INTERNAL PULL-UP
XTALI
XTALO
ENET_XTALI
ENET_XTALO
Y4101
25.0000M
SM-3.2X2.5MM
C4150 15PF
C4151 15PF
1. KEEP ENET_XTALI AND ENET_XTALO
TRACE LENGTH <12MIL
2. DO NOT ROUTE UNDER CRYSTAL
THRML_PAD
R4106 49.9
R4105 49.9
R4104 49.9
R4103 49.9
R4120 49.9
R4119 49.9
R4118 49.9
R4117 49.9
ENET_MDI0
ENET_MDI1
ENET_MDI2
ENET_MDI3
C4116 0.001UF
C4115 0.001UF
C4117 0.001UF
C4118 0.001UF
PLACE RESISTORS CLOSE TO U4101
R4130 4.7K
R4131 4.7K
PLACE C4140 NEAR U4102 VCC
C4140 0.1UF
OMIT
CRITICAL
U4102
M24C08
SO8
R4122 4.7K
R4123 4.7K
NOSTUFF
R4124 0
PLACE C4127-C4134 NEAR PINS VDD0-VDD7 ON U4101
SCHEME MATCHES DOC MVL100258-01
C4126 0.1UF
C4127 0.1UF
C4128 0.1UF
C4129 0.1UF
C4130 0.1UF
C4131 0.001UF
C4132 0.001UF
C4133 0.001UF
C4134 0.001UF
PLACE C4135-C4139 NEAR VDDO_TTL0-VDD_TTL4 ON U4101
SCHEME MATCHES DOC MVL100258-01
C4135 0.1UF
C4136 0.1UF
C4137 0.1UF
C4138 0.001UF
C4139 0.001UF
OPTIONAL EXTERNAL LDO
NO PULL-UP NEEDED
ANALOG
LED
TEST
PCI EXPRESS
MEDIA
TWSI
TEST
SPI
MAIN CLK
ETHERNET CONTROLLER
SYNC_MASTER=ENET
SYNC_DATE=12/06/2005
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APPLE INC.
SIZE D
DRAWING NUMBER 051-7370
REV. C
SCALE NONE
SHT 41 OF 98

L4250
120-OHM-0.3A-EMI
0402-LF

36D5 PP2V5_S3_ENET_AVDD 1 — 2 PP2V5_S3_ENET_AVDD_F

PLACE ONE CAP AT EACH PIN 3 AND 6 OF TRANSFORMERS

C4200 0.1UF 10% 16V X5R 402
C4201 0.1UF 10% 16V X5R 402
C4202 0.1UF 10% 16V X5R 402
C4203 0.1UF 10% 16V X5R 402

PLACE ONE CAP NEAR EACH PIN 3 AND 6 OF TRANSFORMERS

C4204 0.001UF 10% 50V CERM 402
C4205 0.001UF 10% 50V CERM 402
C4206 0.001UF 10% 50V CERM 402
C4207 0.001UF 10% 50V CERM 402

CROSS-OVERS ARE IN SCHEMATIC TO EASE ROUTING

CRITICAL
1000BT-824-00275
T4201
XFR-SM

36C3 IO ENET_MDI_P<0>
36C3 IO ENET_MDI_N<0>
ENET_MDI_TRAN_P<0>
ENET_MDI_TRAN_N<0>
ENET_CENTER_TAP<0>
NC1 NC2 NC4 NC3 (SIDE / SIDE)
ENET_CENTER_TAP<1>
36C3 IO ENET_MDI_P<1>
36C3 IO ENET_MDI_N<1>
ENET_MDI_TRAN_P<1>
ENET_MDI_TRAN_N<1>

CRITICAL
1000BT-824-00275
T4202
XFR-SM

36C3 IO ENET_MDI_P<3>
36C3 IO ENET_MDI_N<3>
5A7 ENET_MDI_TRAN_P<3>
ENET_MDI_TRAN_N<3>
ENET_CENTER_TAP<2>
NC1 NC2 NC4 NC3 (SIDE / SIDE)
ENET_CENTER_TAP<3>
36C3 IO ENET_MDI_P<2>
36C3 IO ENET_MDI_N<2>
5A7 ENET_MDI_TRAN_P<2>
5A7 ENET_MDI_TRAN_N<2>

OMIT
CRITICAL
J4200
RJ45
819B-3608-M280
F-RT-SM
SYM_VER-2
514S0119

R4200 75 1% 1/16W MF-LF 402
R4201 75 1% 1/16W MF-LF 402
R4202 75 1% 1/16W MF-LF 402
R4203 75 1% 1/16W MF-LF 402

ENET_BOB_SMITH_CAP
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM

C4210 0.001UF 20% 2KV CERM 1808

6C6 =GND_CHASSIS_RJ45 OUT

C4211 0.001UF 10% 50V CERM 402
C4212 0.001UF 10% 50V CERM 402

PLACE C4211 AND C4212
ON EACH SIDE OF J4200

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0037	157S0011	?	T4201,T4202	E&E AND DELTA TRANSFORMER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S0143	1	CONN,8P RJ-45 JACK,MIDPLANE,MG3,LF	J4200	CRITICAL	NORMAL
514S0144	1	CONN,8P RJ-45 JACK,MIDPLANE,BLACK,LF	J4200	CRITICAL	FANCY

ETHERNET CONNECTOR

SYNC_MASTER=ENET SYNC_DATE=11/14/2005

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 42 OF 98	

PAGE NOTES

INPUT

=PP3V3_S0_FW - 3.3V POWER FOR FIREWIRE (MOBILE: OFF DURING SLEEP)
=PP3V3_S0_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)
PCI_GNT3_L - PCI GRANT FROM SB
PCI_CLK_FW - NEED TO REFERENCE TO ALIAS PAGE
PCI_RST_L - PCI RESET FROM SB
FW_PC0 - FIREWIRE POWER CLASS IDENTIFIER

INPUT/OUTPUT

PCI_AD<0..31>,PCI_C_BE_L<0..3>,PCI_FRAME_L,PCI_IRDY_L,PCI_TRDY_L,
PCI_DEVSEL_L, PCI_STOP_L, PCI_PAR, PCI_PERR_L, PCI_SERR_L
FW_A_TPA_P/N, FW_A_TPB_P/N, FW_A_TPBIAS - PORT 0 FIREWIRE DIFF PAIRS
FW_B_TPA_P/N, FW_B_TPB_P/N, FW_B_TPBIAS - PORT 1 FIREWIRE DIFF PAIRS
FW_C_TPA_P/N, FW_C_TPB_P/N, FW_C_TPBIAS - PORT 2 FIREWIRE DIFF PAIRS

OUTPUT

PCI_REQ3_L - PCI REQUEST TO SB
PM_CLKRUN_L - CLOCK-RUN PCI PROTOCOL
INT_PIRQD_L - INTERRUPT TO SB
PCI_PME_FW_L - DEDICATED PME FOR FIREWIRE (SB GPIO1)

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
6/20/2005 - BGA VERSION OF FW323-06 ADDED
6/21/2005 - CHANGED INT* TO INT_PIRQD_L (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED PCI_ID TO AD19 (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED REQ/GNT TO REQ3/GNT3 (PER ARCHITECTURAL DEFINITION)
6/22/2005 - ADDED 510R PULL-DOWN ON RST* AND REMOVED CONNECTION TO PLT_RST_L
6/22/2005 - CHANGED CLK_PME_DIFF_PAIR NAMES TO BE RE-USE COMPLIANT
6/22/2005 - REMOVED CONSTRAINT SETS AS THEY WILL BE MANAGED ON BOARD SIDE
6/22/2005 - REMOVED C4421 - REDUNDANT
6/22/2005 - BRING OUT PCB CONNECTION TO BE CONNECTED ON PORT PAGE
7/26/2005 - CONNECTED PIN E10 TO GND

MOBILE TURNS OFF CONTROLLER POWER DURING SLEEP
0.001A DURING SLEEP

64B3 =PP3V3_S3_FW

PLACE ONE CAP PER TWO PINS STARTING WITH C4424 ON VDD0

C4424 10UF 20% 6.3V X5R 603
C4418 0.1UF 10% 10V X5R CERM 402
C4422 0.1UF 10% 10V X5R CERM 402
C4426 0.1UF 10% 10V X5R CERM 402
C4428 0.1UF 10% 10V X5R CERM 402
C4430 0.1UF 10% 10V X5R CERM 402
C4432 0.1UF 10% 10V X5R CERM 402

L4400
600-OHM-300MA
0402

PLACE ONE CAP PER TWO PINS STARTING WITH C4416 ON VDDA0

PP3V3_S3_FW_AVDD
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM

C4416 10UF 20% 6.3V X5R 603
C4417 0.1UF 10% 10V X5R 402
C4429 0.1UF 10% 10V X5R 402
C4425 0.1UF 10% 10V X5R 402

64B3 =PP3V3_S3_PCI

G4 VDD0, M1 VDD1, M2 VDD2, K5 VDD3, K7 VDD4, L13 VDD5, H13 VDD6, F13 VDD7, A2 VDD9
D10 VDDA0, A13 VDDA1, B18 VDDA2, A7 VDDA3, A8 VDDA4, D6 VDDA5

CONNECT TO VDD FOR 3.3V OPERATION

G13 PCI_VIOS

PCI_AD<0>	F10	PCI_AD0
PCI_AD<1>	G10	PCI_AD1
PCI_AD<2>	H10	PCI_AD2
PCI_AD<3>	H12	PCI_AD3
PCI_AD<4>	J13	PCI_AD4
PCI_AD<5>	J12	PCI_AD5
PCI_AD<6>	K13	PCI_AD6
PCI_AD<7>	K10	PCI_AD7
PCI_AD<8>	L12	PCI_AD8
PCI_AD<9>	M13	PCI_AD9
PCI_AD<10>	L11	PCI_AD10
PCI_AD<11>	M12	PCI_AD11
PCI_AD<12>	M11	PCI_AD12
PCI_AD<13>	N12	PCI_AD13
PCI_AD<14>	M10	PCI_AD14
PCI_AD<15>	N11	PCI_AD15
PCI_AD<16>	M4	PCI_AD16
PCI_AD<17>	N5	PCI_AD17
PCI_AD<18>	N4	PCI_AD18
PCI_AD<19>	M3	PCI_AD19
PCI_AD<20>	M2	PCI_AD20
PCI_AD<21>	N3	PCI_AD21
PCI_AD<22>	K4	PCI_AD22
PCI_AD<23>	M1	PCI_AD23
PCI_AD<24>	K2	PCI_AD24
PCI_AD<25>	J4	PCI_AD25
PCI_AD<26>	K1	PCI_AD26
PCI_AD<27>	J2	PCI_AD27
PCI_AD<28>	J1	PCI_AD28
PCI_AD<29>	H2	PCI_AD29
PCI_AD<30>	H4	PCI_AD30
PCI_AD<31>	H1	PCI_AD31
PCI_C_BE_L<0>	K12	PCI_CBE0*
PCI_C_BE_L<1>	M9	PCI_CBE1*
PCI_C_BE_L<2>	L3	PCI_CBE2*
PCI_C_BE_L<3>	L1	PCI_CBE3*
PCI_PAR	N10	PCI_PAR
PCI_FRAME_L	N6	PCI_FRAME*
PCI_IRDY_L	M6	PCI_IRDY*
PCI_TRDY_L	N7	PCI_TRDY*
PCI_DEVSEL_L	N8	PCI_DEVSEL*
PCI_STOP_L	M7	PCI_STOP*
FW_PCI_IDSEL	L2	PCI_IDSEL
PCI_REQ3_L	E2	PCI_REQ*
PCI_GNT3_L	E1	PCI_GNT*
PCI_PERR_L	M8	PCI_PERR*
PCI_SERR_L	N9	PCI_SERR*
PCI_CLK_FW	G2	PCI_CLK
PM_CLKRUN_L	D1	CLKRUN*
FW_PCI_RST_L	F1	PCI_RST*
INT_PIRQD_L	D2	PCI_INTA*
PCI_PME_FW_L	F2	PCI_PME*

R4431 22 5% 1/16W MF-LF 402

R4432 100 1% 1/16W MF-LF 402

THIS IS FROM ICH-7M

PLACE R4432 VERY CLOSE TO PIN B18 OF U2100

OMIT
CRITICAL
U4400
FW32306
BGA

197S0030 3.2MMX2.5MM
CRITICAL
Y4403
SM-3.2X2.5MM
24.576MHZ

R4400 390 5% 1/16W MF-LF 402
C4411 15PF 5% 50V CERM 402
C4412 15PF 5% 50V CERM 402

NEED TO CHECK CRYSTAL LOAD CAPACITANCE

XI	A5	FW_XI
XO	B5	FW_XO
RESET*	B4	FW_PWRON_RST_L
R1	A6	FW_R1
R0	B7	FW_R0

SPEC RECOMMENDS 2.49K

R4452 2.1K 1% 1/16W MF-LF 402
C4420 0.1UF 10% 10V X5R 402
R4420 510K 5% 1/10W MF-LF 402

TPBIAS0	B8	FW_A_TPBIAS
TPA0_P	A9	FW_A_TPA_P
TPA0_N	B9	FW_A_TPA_N
TPB0_P	B10	FW_A_TPB_P
TPB0_N	A10	FW_A_TPB_N
TPBIAS1	D8	FW_B_TPBIAS
TPA1_P	A11	FW_B_TPA_P
TPA1_N	B11	FW_B_TPA_N
TPB1_P	B12	FW_B_TPB_P
TPB1_N	A12	FW_B_TPB_N
TPBIAS2	C13	FW_C_TPBIAS
TPA2_P	C11	FW_C_TPA_P
TPA2_N	C12	FW_C_TPA_N
TPB2_P	D13	FW_C_TPB_P
TPB2_N	D12	FW_C_TPB_N

MODE_420	M5	MODE FOR EXTERNAL LINK
MODE_A	B6	
PC0	E12	FW_PC0
PC1	F13	
PC2	F12	
CONTENDER	G12	LOW = NOT BUS MANAGER
CARDBUSN	B1	LOW = PCI OPERATION
MPCI_ACTN_323	E10	

DUAL PORT DEVICES ARE POWER CLASS 4 (’100’)
SINGLE PORT DEVICES ARE POWER CLASS 0 (’000’)

MANUFACTURING TEST PINS

TEST0	C2
TEST1	C1
PTEST	A4
SE	A3
SM	B3

A1 VSS0, B2 VSS1, C3 VSS2, D4 VSS3, E4 VSS4, E5 VSS5, F4 VSS6, F6 VSS7, F7 VSS8, F8 VSS9, G1 VSS10, G6 VSS11, G7 VSS12, G8 VSS13, H6 VSS14, H7 VSS15, H8 VSS16, J5 VSS17, J9 VSS18, J10 VSS19, K8 VSS20, K9 VSS21, N13 VSS22
E13 VSSA0, E9 VSSA1, D9 VSSA2, D7 VSSA3, D5 VSSA4

FIREWIRE CONTROLLER

SYNC_MASTER=ENET SYNC_DATE=08/30/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 44 OF 98	

Page Notes

INPUT:

=PPBUS_FW - PORT POWER

=PP3V3_S5_FW - DIGITAL POWER

=GND_CHASSIS_FW_PORT0 - CHASSIS GROUND

=FWPWR_PWRON - ADDITIONAL POWER CONTROL

INPUT/OUTPUT:

FW_TPA0_P/N,FW_TPB0_P/N,FW_TPBIAS0 - FIREWIRE DIFF PAIRS

OUTPUT:

FW_PC0 - POWER CLASS IDENTIFIER (SINGLE PORT - TIE LOW)

PAGE HISTORY

5/19/05 - INITIAL REVISION
6/22/05 - CHANGED DIFF PAIR NAMES TO MATCH REUSE
6/22/05 - REMOVED CONSTRAINTS BECAUSE USING ALLEGRO CONST MANAGER
6/22/05 - CONNECTED FW_PC0 FOR SINGLE PORT
7/26/05 - UPDATED LATE-VG POWER RAIL CIRCUIT FROM M1
7/26/05 - CHANGED CONNECTOR PORT NAMING TO PORT0
7/26/05 - SWITCHED TO 514-0124 FOR PRE-PROTO CONNECTOR
7/26/05 - REMOVED R4520 - IT HASN'T BEEN STUFFED FOR MANY PRODUCTS
7/26/05 - CHANGED FL4590 TO 1.1A VERSION
7/26/05 - REMOVED ETHERNET LOW-POWER MODE CIRCUIT
7/26/05 - UPDATED SIGNAL NAMES FOR FW PORT POWER ENABLE

1394b implementation based on Apple
FireWire Design Guide (FWDG 0.6, 5/14/03)

PORT POWER CLASS

0 FOR SINGLE PORT
1 FOR DUAL PORT

38A3 OUT FW_PC0

PPBUS_S5_FWPWRSW_F
VOLTAGE=18.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

64C1 =PPBUS_S5_FWPWRSW

FL4590
1.1A-24V
MINISMDC

Q4590
FDC638P
SM-LF

PPFW_SWITCH 58Z
VOLTAGE=18V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

D4590
SMB
B340LBXF

64A6 =PP3V3_S0_FW

R4590 470K 5% 1/16W MF-LF 402
C4590 0.01uF 10% 16V CERM 402

FWPWR_EN_L_DIV
MIN_LINE_WIDTH=0.05MM
MIN_NECK_WIDTH=0.05MM

R4593 100K 5% 1/16W MF-LF 402

R4591 330K 5% 1/16W MF-LF 402

D4591 BAS16TW-X-F SOT-363

IF =FWPWR_PWRON IS NC:
ENABLES PORT POWER WHEN MACHINE IS RUNNING OR ON AC
IF =FWPWR_PWRON LOW WHEN OFF:
ENABLES PORT POWER WHEN MACHINE IS RUNNING OR ON AC AND NOT SHUTDOWN

FWPWR_RUN

6D2 =FWPWR_PWRON

FWPWR_EN_L 60C8
MIN_LINE_WIDTH=0.05MM
MIN_NECK_WIDTH=0.05MM

Q4591
2N7002
SOT23-LF

FWPWR_EN

65C3 46B3 45D5 5C1 SMC_PS_ON

R4594 10K 5% 1/16W MF-LF 402

FWPWR_ACIN

R4595 470K 5% 1/16W MF-LF 402

Enables port power whenever
machine AC Adapter is plugged
or system at run state with battery only

"Snapback" & "Late VG" Protection

Cable Power

PPFW_PORT0_VP_F
VOLTAGE=16.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

L4510 FERR-250-OHM SM

PPFW_PORT0_VP
VOLTAGE=16.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

C4510 0.001uF 10% 50V CERM 402

39A6 PP3V3_S5_FWLATEVG

D4520 BAV99DW-X-F SOT-363

C4520 0.01UF 10% 16V CERM 402

C4521 0.01UF 10% 16V CERM 402

D4521 BAV99DW-X-F SOT-363

C4522 0.01UF 10% 16V CERM 402

C4523 0.01UF 10% 16V CERM 402

120-OHM 2012 SYM_VER-2

FL4520

FL4521

FW_PORT0_TPA_P
FW_PORT0_TPA_N
FW_PORT0_TPB_P
FW_PORT0_TPB_N

FW_PORT0_TPA_P_FL
FW_PORT0_TPA_N_FL
FW_PORT0_TPB_P_FL
FW_PORT0_TPB_N_FL
(PPFW_PORT0_VP)
(GND_FW_PORT0_VGND)

C4524 0.01uF 10% 50V X7R 603-1

C4525 0.01uF 10% 16V CERM 402

PORT 0
1394A
OMIT
CRITICAL
J4500
1394A
F-RT-TH1

TPO (TPA+)
TPO# (TPA-)
TPI (TPB+)
TPI# (TPB-)
VP
VGND

=GND_CHASSIS_FW_UPPER 6A6
Plexi: 514-0124
Enclosure: 514-0289
=GND_CHASSIS_FW_DOWN 6C8

[LATE VG NOTES]
CURRENT THROUGH THE BIAS RESISTOR SHOULD BE 5MA FOR A VOLTAGE DROP TO 2.2V
IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A 0.5V DROP

IO 38B3 FW_A_TPBIAS

R4500 56.2 1% 1/16W MF-LF 402

R4501 56.2 1% 1/16W MF-LF 402

C4500 0.33UF 10% 6.3V CERM-X5R 402

IO 38B3 FW_A_TPA_P
IO 38B3 FW_A_TPA_N
IO 38B3 FW_A_TPB_P
IO 38B3 FW_A_TPB_N

R4502 56.2 1% 1/16W MF-LF 402

R4503 56.2 1% 1/16W MF-LF 402

FW_PORT0_TPB

C4501 220PF 5% 25V CERM 402

R4504 4.99K 1% 1/16W MF-LF 402

LATE-VG PROTECTION POWER

64A3 =PP3V3_S5_FWLATEVG

R4550 330 5% 1/16W MF-LF 402

PP3V3_S5_FWLATEVG_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.35MM
MIN_NECK_WIDTH=0.25MM

L4550 400-OHM-EMI SM-1

PP3V3_S5_FWLATEVG 39B5
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.35MM
MIN_NECK_WIDTH=0.25MM

NO STUFF
C4551 0.1uF 20% 16V CERM 402

NO STUFF
C4552 0.001uF 10% 50V CERM 402

D4550 SOT23 MMBZ5227B

CAPS MAY NOT BE NECESSARY.
NO STUFF FOR NOW THOUGH

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0359	1	CONN,6P 1394A RCPT,MIDPLANE,MG3,LF	J4500	CRITICAL	NORMAL
514-0316	1	CONN,6P 1394A RCPT,MIDPLANE,BLACK,LF	J4500	CRITICAL	FANCY

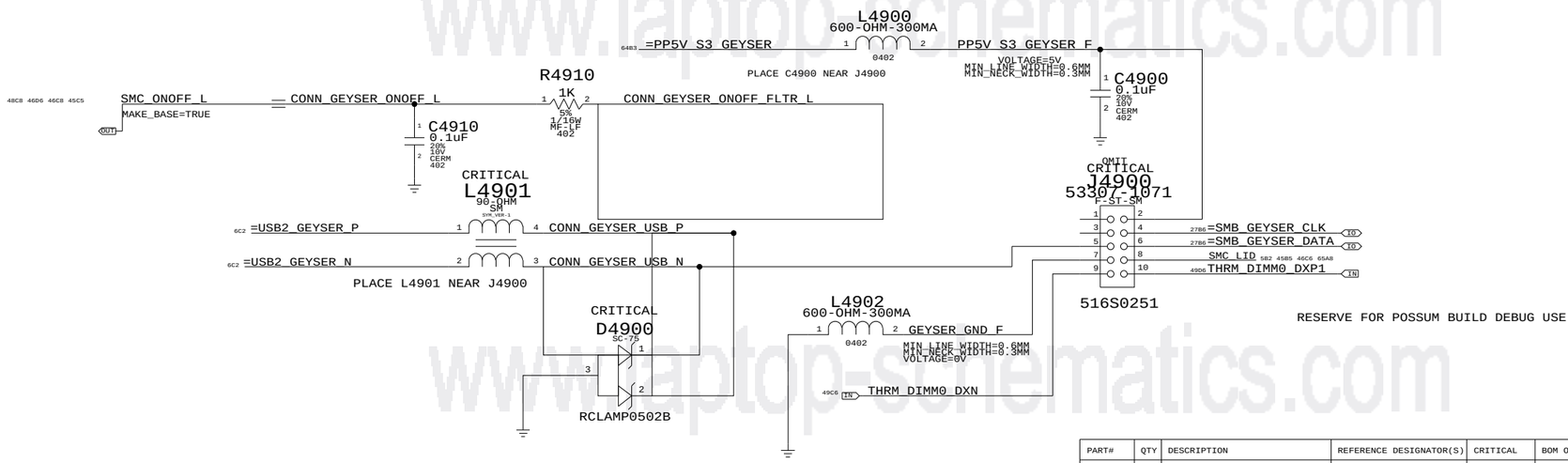
FIREWIRE PORT

SYNC_MASTER=ENET
SYNC_DATE=11/16/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 45 OF 98	

GEYSER AND DIMM0 REMOTE TEMP SENSORS



RESERVE FOR POSSUM BUILD DEBUG USE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0482	1	ACES 88646-1071-NS	J4900	CRITICAL	NORMAL
516S0482	1	ACES 88646-1071-NS	J4900	CRITICAL	FANCY

CONNECTOR MISC

SYNC_MASTER=ENET SYNC_DATE=11/16/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE	SHT	OF
NONE	49	98

PLACE C5100 AND C5101
NEAR U5100 PIN 22 AND 49

64B3 =PP5V_S3_IR

C5100 0.1UF 20% 10V CERM 402

C5101 0.1UF 20% 10V CERM 402

22 49 VDD

OMIT

U5100 CY8C24794 MLF

6C2 =USB2_IR_P — 20 D+

6C2 =USB2_IR_N — 21 D-

45	P0_0	P1_0	25
54	P0_1	P1_1	18
46	P0_2	P1_2	26
53	P0_3	P1_3	17
47	P0_4	P1_4	27
52	P0_5	P1_5	16
48	P0_6	P1_6	28
51	P0_7	P1_7	15
41	P2_0	P3_0	33
2	P2_1	P3_1	10
42	P2_2	P3_2	34
1	P2_3	P3_3	9
43	P2_4	P3_4	35
56	P2_5	P3_5	8
44	P2_6	P3_6	36
55	P2_7	P3_7	7
37	P4_0	P5_0	29
6	P4_1	P5_1	14
38	P4_2	P5_2	30
5	P4_3	P5_3	13
39	P4_4	P5_4	31
4	P4_5	P5_5	12
40	P4_6	P5_6	32
3	P4_7	P5_7	11
24	P7_0	THRML PAD	57
23	P7_7		

35C6 IR_RX_OUT — R5100 100 5% 1/16W MF-LF 402 — IR_RX_OUT_F

C5102 0.001UF 10% 50V CERM 402

C5102 CLOSE TO U5100 PIN 2

VSS 19 50

IR CONTROLLER

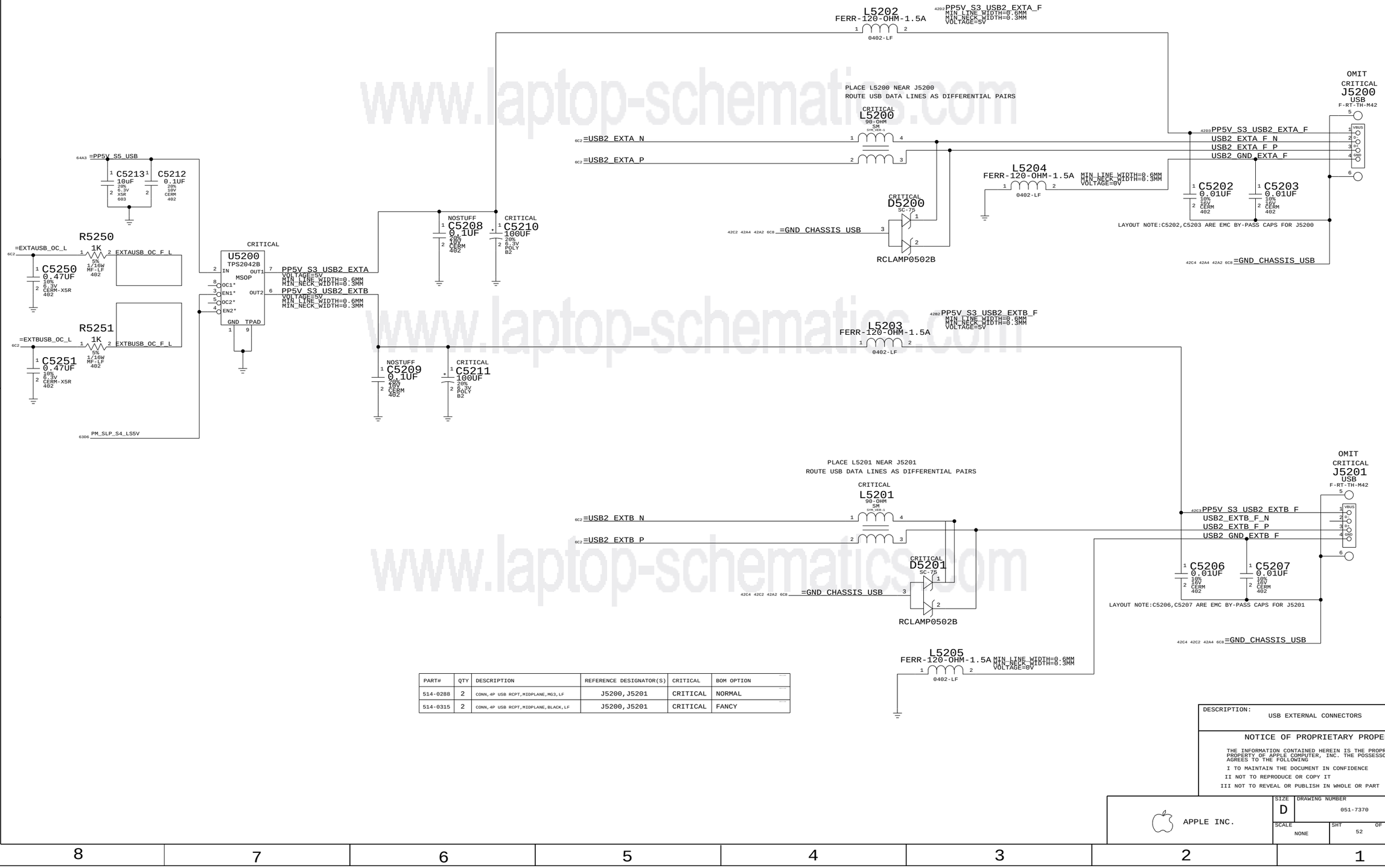
SYNC_MASTER=ENET SYNC_DATE=11/09/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE NONE — SHT 51 OF 98

USB 2.0 CONNECTORS

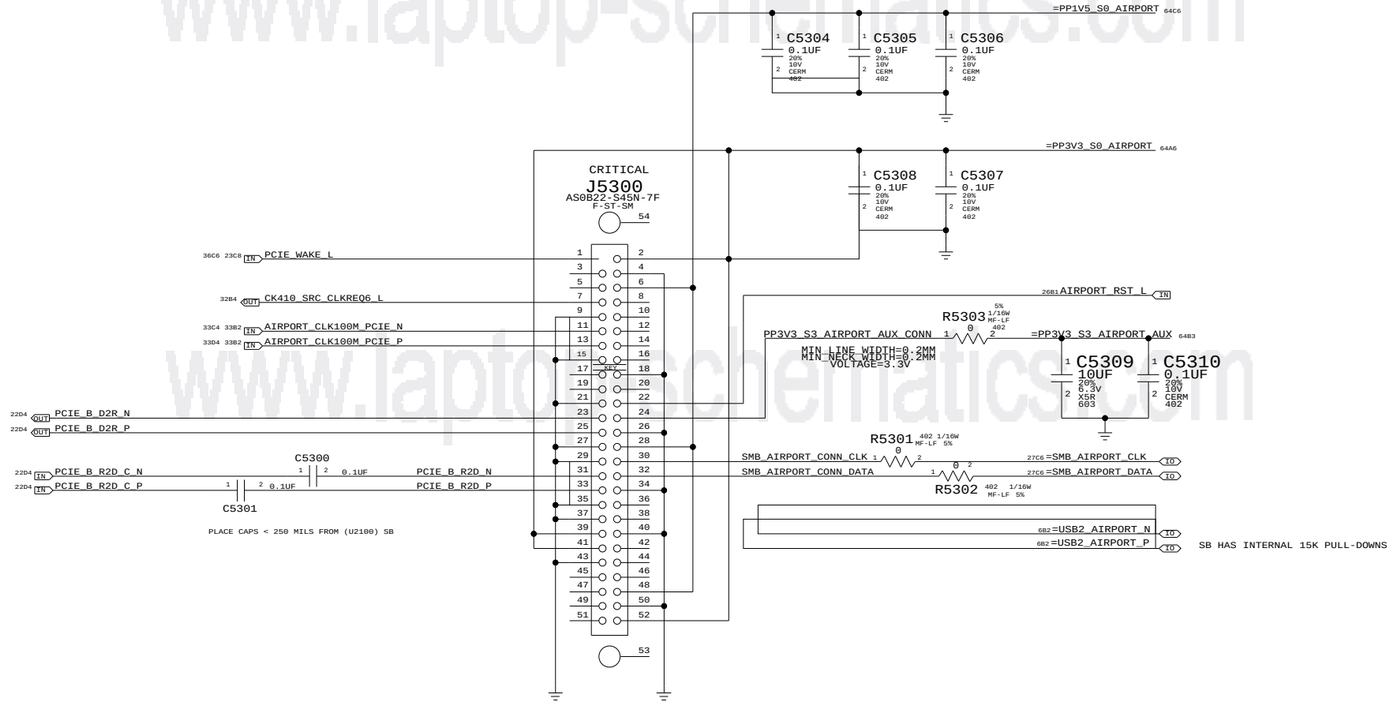


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0288	2	CONN,4P USB RCPT,MIDPLANE,MG3,LF	J5200,J5201	CRITICAL	NORMAL
514-0315	2	CONN,4P USB RCPT,MIDPLANE,BLACK,LF	J5200,J5201	CRITICAL	FANCY

DESCRIPTION:
USB EXTERNAL CONNECTORS

APPLE INC.

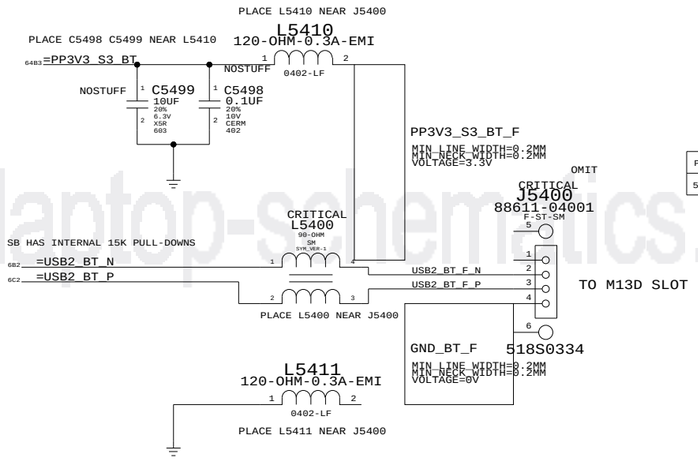
SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 52 OF 98	



AIRPORT CONN

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE	SHT	OF
NONE	53	98



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
518S0486	1	IMPROVED ACES CONNECTOR	J5400	CRITICAL	M42B

BLUETOOTH INTERFACE

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 54 OF 98	

OMIT

U5800
SMC_H8S2116
BGA
(1 OF 4)

23C3	PM_LAN_ENABLE	B12	P10	P60/KIN0*	L13	63C8	SMC_PM_G2_EN
26A3	SMC_RSTGATE_L	C13	P11	P61/KIN1*	L14	65C3 46B3 39C6 5C1	SMC_PS_ON (Enable AC adapter PWR)
63B1 26A5 5B2	ALL_SYS_PWRGD	A15	P12	P62/KIN2*	L15	22C6	SPI_ARB
59A1 46D6	RSMRST_PWRGD	B14	P13	P63/KIN3*	K12	50C7 22C6	SPI_SCLK
23C3	SMC_SB_NMI	B15	P14	P64/KIN4*	K13	50C1 22C6	SPI_SI
23C1	PM_RSMRST_L	C14	P15	P65/KIN5*	K14	50C1 22C6	SPI_SO
58C7	IMVP_VR_ON	D12	P16	P66/IRQ6*/KIN6*	J12	46C1	SMC_PROCHOT_3_3_L
23C3	PM_PWRBTN_L	C15	P17	P67/IRQ7*/KIN7*	J13	6B1	SMC_CPU_INIT_3_3_L
46C6	SMC_P20	D13	P20	P70/AN0	N12	48C1	SMC_CPU_ISENSE
46C6	SMC_P21	D14	P21	P71/AN1	R13	48B1 5B2	SMC_CPU_VSENSE
46C6	SMC_P22	D15	P22	P72/AN2	P13	46C6	SMC_GPU_ISENSE
46C6	SMC_P23	E12	P23	P73/AN3	R14	46C6	SMC_GPU_VSENSE
66A3 46B6 5C1	SMC_BATT_TRICKLE_EN_L	E14	P24	P74/AN4	P14	66C2	SMC_DCIN_ISENSE
66A4 46B6 5C1	SMC_BATT_CHG_EN	E15	P25	P75/AN5	R15	48C1	SMC_PBUS_VSENSE
46C6	SMC_P26	E13	P26	P76/AN6	N13	66B1	SMC_BATT_ISENSE
46C6	SMC_P27	F14	P27	P77/AN7	P15	46B1	SMC_FWIRE_ISENSE
53C6 47C6 21D4 5D2	LPC_AD<0>	D9	P30/LAD0	P80/PME*	C7	23C1	SMC_WAKE_SCI_L
53C6 47C6 21D4 5D2	LPC_AD<1>	C9	P31/LAD1	P81/GA20	A7	46B2	SMC_TPM_GPIO
53C6 47C5 21D4 5C2	LPC_AD<2>	A9	P32/LAD2	P82/CLKRUN*	B7	47C6 38A5 53C6 23C8 5C2	PM_CLKRUN_L
53C6 47C5 21D4 5C2	LPC_AD<3>	B9	P33/LAD3	P83/LPCPD*	D6	47C5 46D3 53C6 23C5 5C2	PM_SUS_STAT_L
53C6 47C6 21C5 5C2	LPC_FRAME_L	D8	P34/LFRAME*	P84/IRQ3*/TXD1	C6	46B1	SC_TX_L (Serial Port Transmit)
26B1	SMC_LRESET_L	C8	P35/LRESET*	P85/IRQ4*/RXD1	A6	46B1	SC_RX_L (Serial Port Receive)
33D6	PCI_CLK_SMC	A8	P36/LCLK	P86/IRQ5*/SCK1/SCL1	B6	27B3	SMB_BSB_CLK (BAT B SMBUS CLK)
53C6 47C5 23C8 5C2	INT_SERIRQ	D7	P37/SERIRQ	P90/IRQ2*	K4	48C8 46D6 46C8 46C8	SMC_ONOFF_L
	SMC_DISPLAY_ENABLE	A5	P40/TMI0	P91/IRQ1*	J2	65C7 65C3 46B6 5C1	SMC_BC_ACOK (AC I/P detect)
46A4	SMC_SYS_LED_16B	B5	P41/TMO0	P92/IRQ0*	J1	65A2 46C6 5D1	SMC_BS_ALRT_L
27B3	SMB_BSB_DATA (BAT B SMBUS DATA)	D5	P42/SDA1	P93/IRQ12*	J3	63B8 63A7 23C3	PM_SLP_S3_L
53C7	SMC_TPM_PP (TPM physical presence)	C3	P43/TMI1/EXSCK1	P94/IRQ13*	J4	63D6 61B8 60C8 23C3	PM_SLP_S4_L
46C6	SMC_P44	B1	P44/TMO1	P95/IRQ14*	H2	46D3 23C3	PM_SLP_S5_L
	SMC_BKLIGHT_ENABLE	C2	P45	P96/EXCL	H1	46A6	SMC_SUS_CLK
46C6	SMC_P46	D3	P46/PWX0/PWM0	P97/IRQ15*/SDA0	G2	27D6	SMB_0_DATA
46C6	SMC_SYS_KBDLED	C1	P47/PWX1/PWM1				
47B6 46D6 46B2 5C2	SMC_TX_L (Debug feature,16550 Transmit)	G1	P50				
47B5 46D6 46B2 5C2	SMC_RX_L (Debug feature,16550 Receive)	G4	P51				
27D6	SMB_0_CLK	F2	P52/SCL0				

OMIT

U5800
SMC_H8S2116
BGA
(2 OF 4)

21C3	SMC_RCIN_L	R3	PA0/KIN8*/PA2DC	PE0	M3		SMC_CASE_OPEN (CASE OPEN/CLOSE DETECT) 46B3
47C6 22B3 5C2	BOOT_LPC_SPI_L	P3	PA1/KIN9*/PA2DD	PE1*/ETCK	M2	47C5 46C6 5C2	SMC_TCK
26C5 23C5	PM_SYSRST_L	R2	PA2/KIN10*/PS2AC	PE2*/ETDI	M1	47C5 46C6 5C2	SMC_TDI
53B7 46D6	SMC_TPM_RESET_L	N3	PA3/KIN11*/PS2AD	PE3*/ETDO	L4	47B6 46C6 5C2	SMC_TDO
14B7 6B2	PM_EXTTS_L<0>	R1	PA4/KIN12*/PS2BC	PE4*/ETMS	L2	47C6 46C6 5C2	SMC_TMS
23C8	PM_THRM_L	N2	PA5/KIN13*/PS2BD	PF0/IRQ8*/PWM2	M7		SMC_DISP_BKLT_B 46C3
65C8 46D6 5C1	SYS_ONEWIRE	M4	PA6/KIN14*/PS2CC	PF1/IRQ9*/PWM3	P6		SMC_DISP_BKLT_A
23C1	PM_BATLOW_L	N1	PA7/KIN15*/PS2CD	PF2/IRQ10*/TMOY	R6	65A8 46C6 40C4 5B2	SMC_LID (LID OPEN/CLOSE SW)
23B8	SMC_EXTSMI_L	B10	PB0/LSMI*	PF3/IRQ11*/TMOX	N6	46C1	SMC_CPU_RESET_3_3_L
23C8	SMC_RUNTIME_SCI_L	A10	PB1/LSCI	PF4/PWM4	M6	66B7 5C1	SMC_BATT_ISET
34B3	SMC_ODD_DETECT (Optical Disk Insert detect)	D10	PB2	PF5/PWM5	R5		SMC_BATT_VSET 46C3
48A8	ISENSE_CAL_EN	A11	PB3	PF6/PWM6	P5	66D7	SMC_SYS_ISET
46C3	SMC_EXCARD_CP	B11	PB4	PF7/PWM7	N5		SMC_SYS_VSET 46C3
46C3	SMC_EXCARD_PWR_EN	C11	PB5				
46D3	SMC_EXCARD_PWR_OC_L	A12	PB6	PG0/EXIRQ8*/TMIX	P9	58C7 22C6	SPI_CE_L
45B3	SMC_PB7	D11	PB7	PG1/EXIRQ9*/TMIY	R9		SMC_PG1 45B3
46C3	SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*	PG2/EXIRQ10*/SDA2	N9	27C3	SMB_BSA_DATA
51B4 5D2	SMC_FAN_1_CTL	G15	PC1/TIOCB0/WUE9*	PG3/EXIRQ11*/SCL2	P8	27C3	SMB_BSA_CLK
46C3	SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*	PG4/EXIRQ12*/EXSDAA	R8	27D3	SMB_RMT_DATA
46C3	SMC_FAN_3_CTL	G12	PC3/TIOCD0/TCLKB/WUE11*	PG5/EXIRQ13*/EXSCLA	M8	27D3	SMB_RMT_CLK
46C3	SMC_FAN_0_TACH	H14	PC4/TIOCA1/WUE12*	PG6/EXIRQ14*/EXSDAB	P7	27B6	SMB_MLB_DATA
51C4 5D2	SMC_FAN_1_TACH	H15	PC5/TIOCB1/TCLKC/WUE13*	PG7/EXIRQ15*/EXSCLB	R7	27C6	SMB_MLB_CLK
46C3	SMC_FAN_2_TACH	H13	PC6/TIOCA2/WUE14*	PH0/EXIRQ6*	E1	46B6	SMC_PROCHOT
46C3 5A7	SMC_FAN_3_TACH	H12	PC7/TIOCB2/TCLKD/WUE15*	PH1/EXIRQ7*	F3	46B5	SMC_THRMTRIP
52C2	SMS_X_AXIS	M11	PD0/AN8	PH2/FWE	K2		SMC_FWE 46C6
52C2	SMS_Y_AXIS	P11	PD1/AN9	PH3/EXEXCL	C4		ALS_GAIN 46C6
52C2	SMS_Z_AXIS	R11	PD2/AN10	PH4	D4	46D6 23C3	SMS_INT_L
46C3	SMC_PD3 (ANALOG_ID)	N11	PD3/AN11	PH5	B3	52C7	SMS_ONOFF_L
62A5 46B3	SMC_NB_ISENSE	P10	PD4/AN12				
61C1 46B3	SMC_MEM_ISENSE	R10	PD5/AN13				
46C3 5A7	ALS_LEFT	N10	PD6/AN14				
46C3	ALS_RIGHT	M10	PD7/AN15				

OMIT

U5800
SMC_H8S2116
BGA
(4 OF 4)

NC	G3	NC0	NC12	F15	NC
NC	H3	NC1	NC13	A14	NC
NC	K3	NC2	NC14	C12	NC
NC	L3	NC3	NC15	C10	NC
NC	N4	NC4	NC16	C5	NC
NC	M5	NC5	NC17	A3	NC
NC	N7	NC6	NC18	B8	NC
NC	M12	NC7	NC19	E4	NC
NC	M13	NC8	NC20	H4	NC
NC	L12	NC9	NC21	M9	NC
NC	K15	NC10	NC22	N8	NC
NC	J14	NC11			

64D1 48C8 46D8 46D5 46D1 45D3 45D2 =PP3V42_G3H_SMC

CRITICAL
C5802 22UF 20% 6.3V CERM-X5R 805
C5803 0.1UF 20% 10V CERM 402
C5804 0.1UF 20% 10V CERM 402
C5805 0.1UF 20% 10V CERM 402
C5806 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE R5899, C5820 NEAR SMC PIN N14, N15

(VCL IS INTERNAL RAIL)
SMC_VCL

64D1 48C8 46D8 46D5 46D1 45D3 45D2 =PP3V42_G3H_SMC

R5899 4.7 5% 1/16W MF-LF 402

C5807 0.47UF 10% 6.3V CERM-X5R 402

LAYOUT NOTE:
PLACE C5807 NEAR PIN F1

SMC_AVCC_RC

C5820 0.1UF 10% 16V CERM 402

66C2 66B1 62A5 61C1 48C1 48B5 48A1 46B6 45C2 GND_SMC_AVSS

PP3V3_AVREF_SMC 46C6

R5809 10K 5% 1/16W MF-LF 402

R5801 10K 5% 1/16W MF-LF 402

47B6 5C2 SMC_MD1 (Should PD) (To debug card for mode select)
KBC_MDE (Should PU)

R5802 10K 5% 1/16W MF-LF 402

R5803 0 5% 1/16W MF-LF 402 NOSTUFF

OMIT
U5800
SMC_H8S2116
BGA
(3 OF 4)

47C5 46D7 5C2 SMC_RST_L
46C7 SMC_XTAL
46C7 SMC_EXTAL

MD1 E2
MD2 K1
NMI F4 (Should PD) (To debug card for mode select) 47B5 5C2 SMC_NMI
ETRST* L1 47C6 5C2 SMC_TRST_L

R5898 10K 5% 1/16W MF-LF 402

XW5800 SM

45C4 46B6 48A1 48B5 48C1 61C1 62A5 66B1 66C2 GND_SMC_AVSS

45B8 SMC_PB7 = MAKE_BASE=TRUE SMC_ENRGYSTR_LDO_EN 46C6 66D2

45B5 SMC_PG1 = MAKE_BASE=TRUE SMC_ENRGYSTR_LDO_PGOOD 46C6 66C1

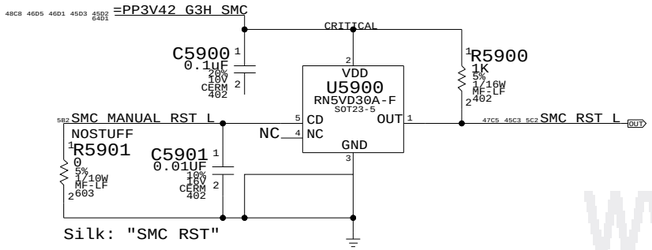
SMC

SYNC_MASTER=SMC SYNC_DATE=08/18/2005

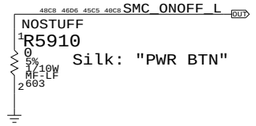
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 58 OF 98	

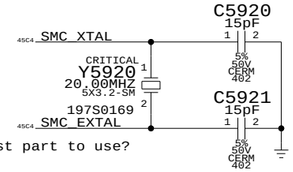
SMC Reset Button / Brownout Detect



Debug Power Button

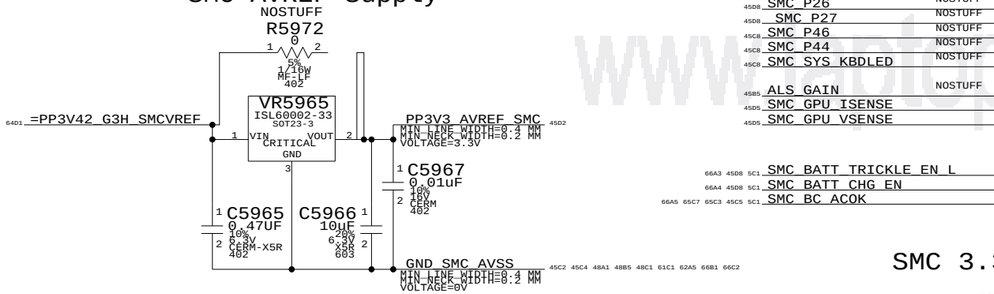


SMC Crystal Circuit



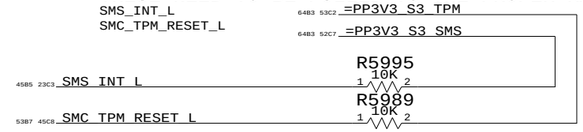
Is this the best part to use?

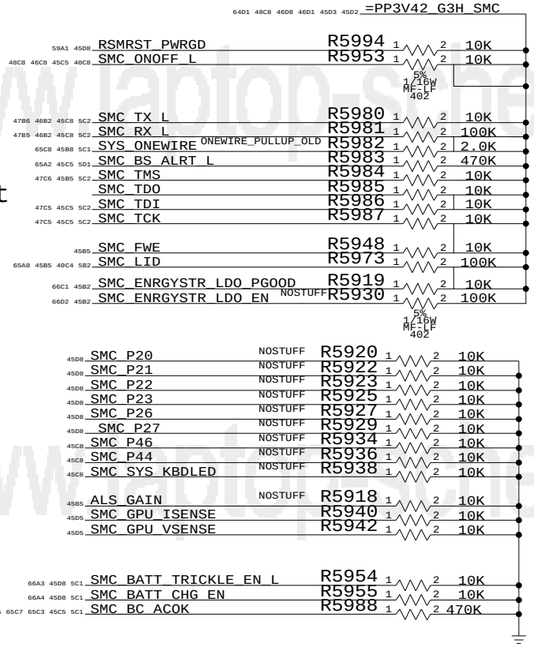
SMC AVREF Supply



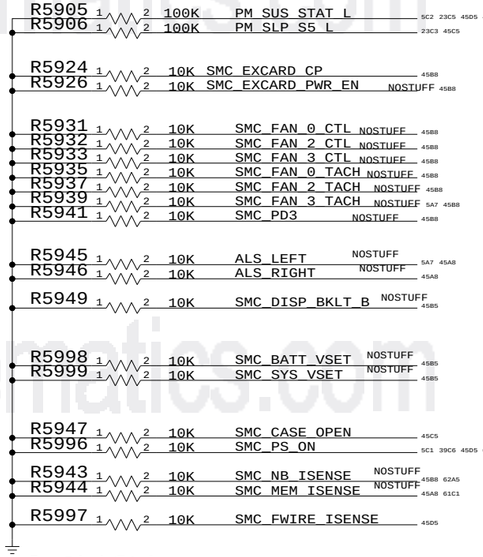
THESE NEED TO BE PULLED TO THE PROPER RAIL:

SMS_INT_L
SMC_TPM_RESET_L

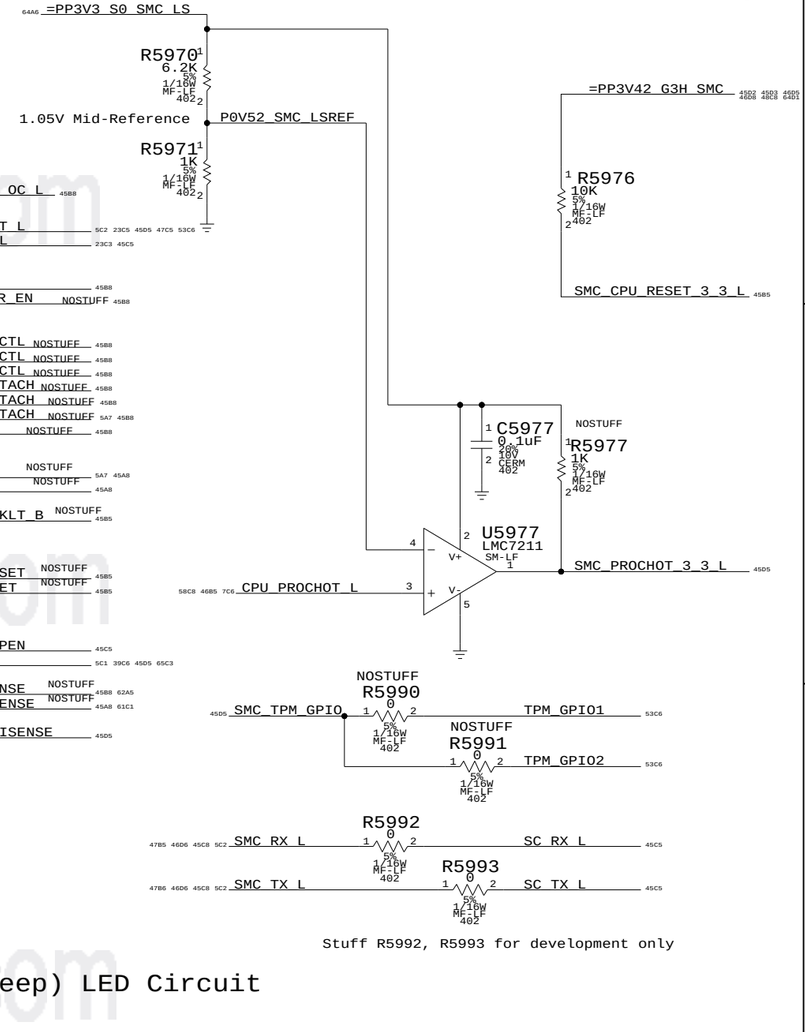




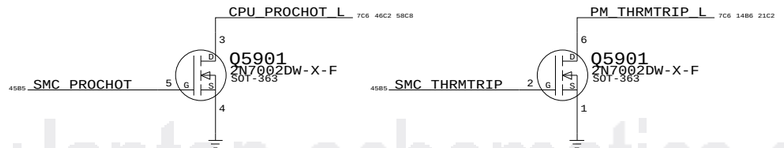
R5928 10K SMC_EXCARD_PWR_OC_L



SMC 1.05V to 3.3V Level Shifting



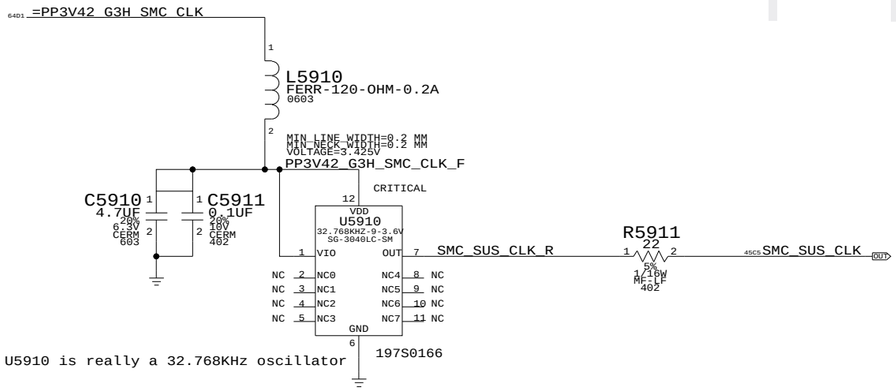
SMC 3.3V to 1.05V Level Shifting



Stuff R5992, R5993 for development only

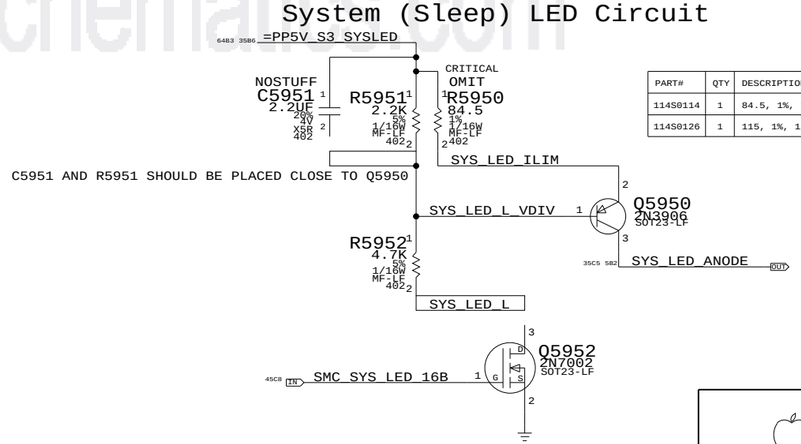
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1278	353S1381	?	VR5965	TI REF3133

SMC G3HOT OSCILLATOR



U5910 is really a 32.768KHz oscillator

System (Sleep) LED Circuit



C5951 AND R5951 SHOULD BE PLACED CLOSE TO Q5950

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0114	1	84.5, 1%, 1/16W, MF-LF, 402	R5950	NORMAL
114S0126	1	115, 1%, 1/16W, MF-LF, 402	R5950	FANCY

SMC SUPPORT

SYNC_MASTER=SMC SYNC_DATE=08/23/2005

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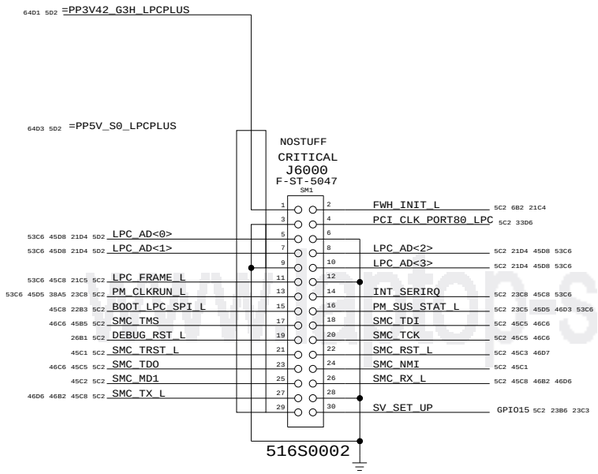
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 59 OF 98	



LPC+ Debug Connector

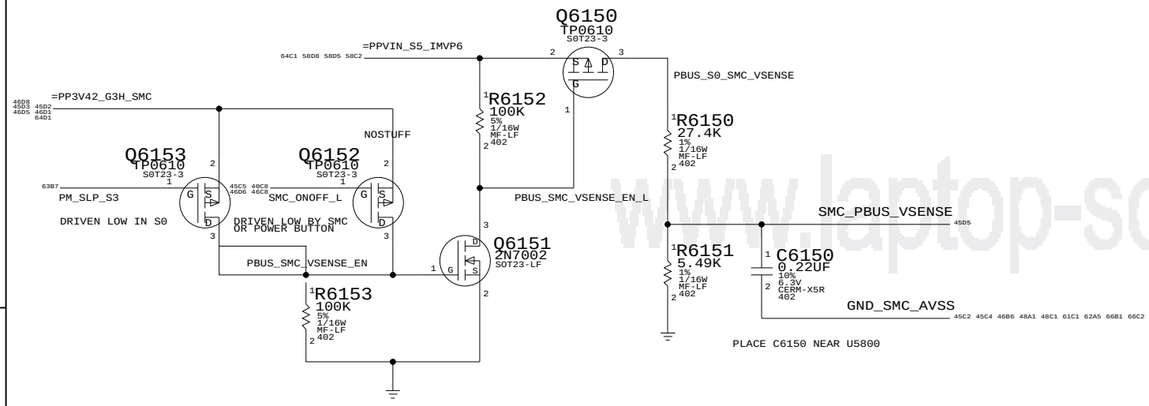
SYNC_MASTER=NB SYNC_DATE=06/30/2005

APPLE INC.

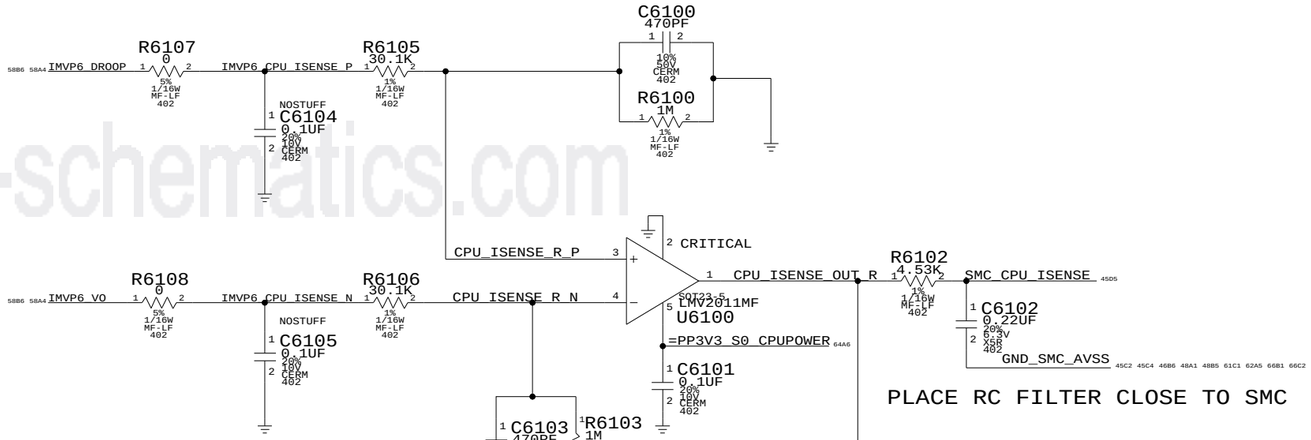
SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE	SHT	OF
NONE	60	98

PROCESSOR DCIN VOLTAGE SENSE



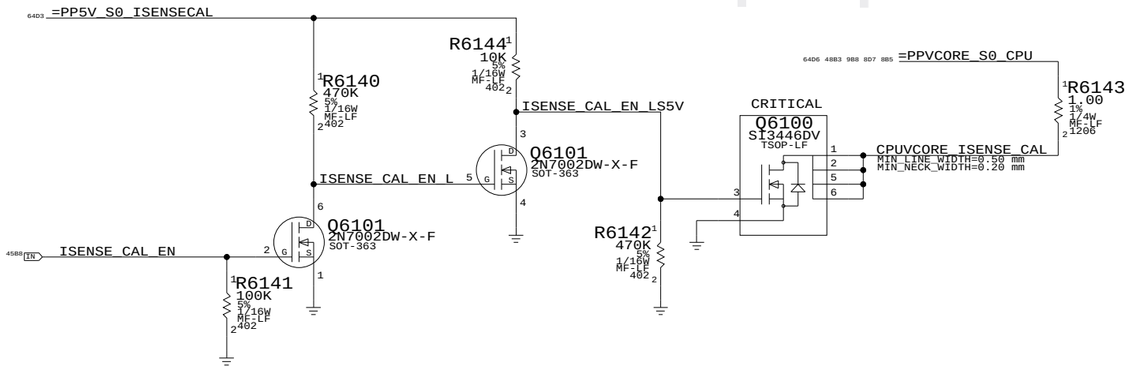
CPU CURRENT SENSE



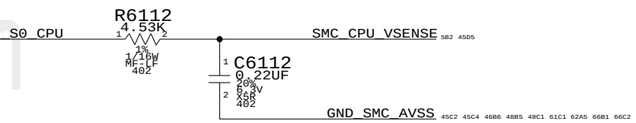
PLACE RC FILTER CLOSE TO SMC

Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



CPU VOLTAGE SENSE



PLACE RC FILTER CLOSE TO SMC

CPU Current & Voltage Sense

SYNC_MASTER=ENET SYNC_DATE=08/30/2005

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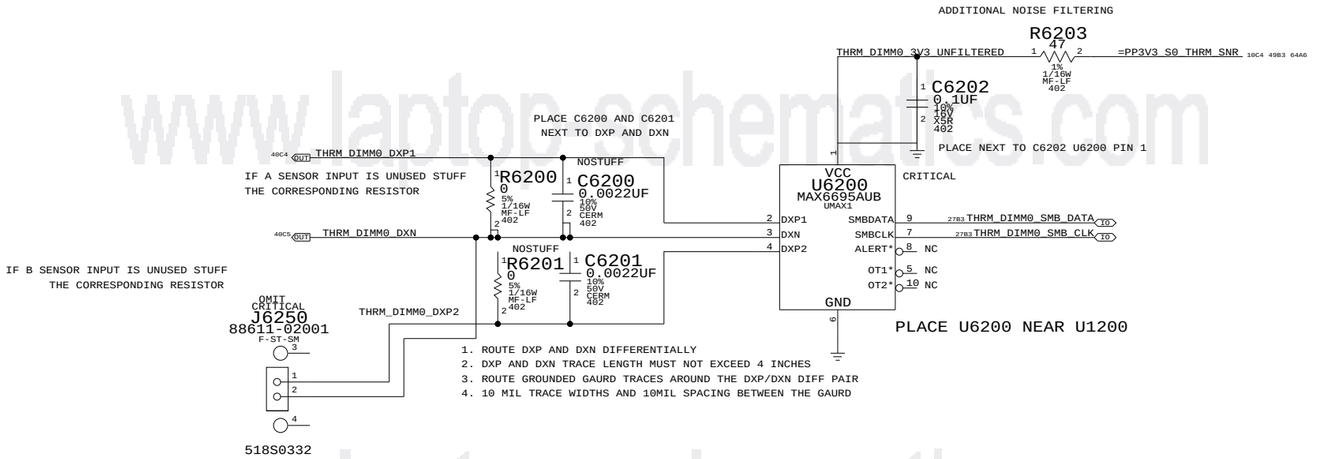
APPLE INC.

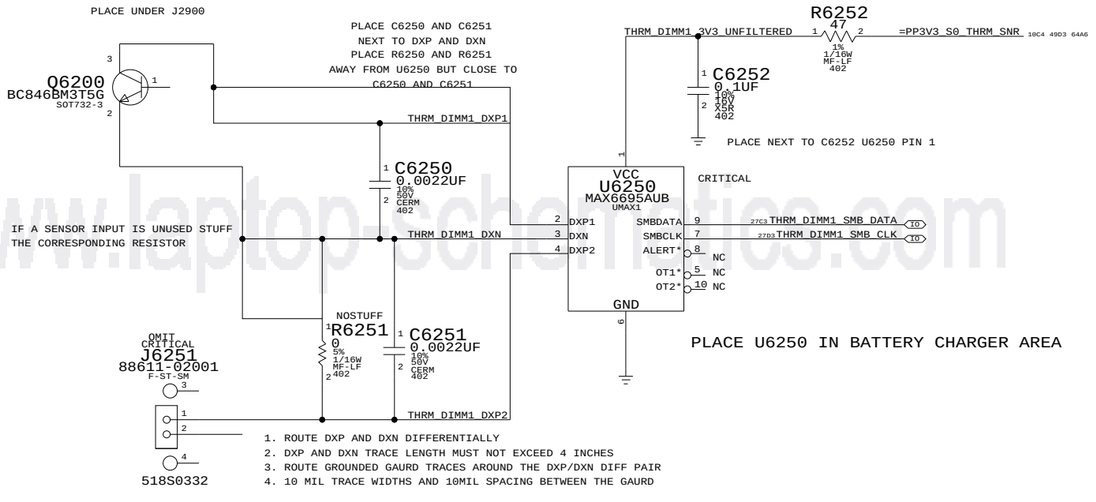
SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 61 OF 98	

DIMM0 TEMPERATURE ZONE



NOTE: REPLACE J6250 AND J6251 FROM 518S0332 TO 518S0487
AFTER THIS CHANGE, THE PCB WILL USE 518S0332 LANDPATTERN, BUT BOM WILL STUFF 518S0487 PART

DIMM1 TEMPERATURE ZONE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
518S0487	2	JST 2-PIN CONNECTOR	J6250,J6251	M42B

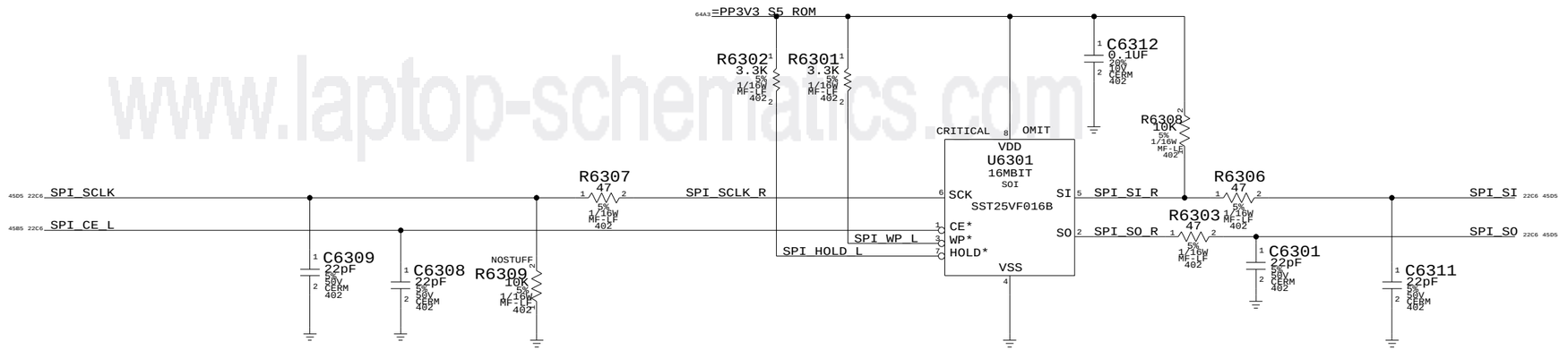
NOTE: REPLACE J6250 AND J6251 FROM 518S0332 TO 518S0487
AFTER THIS CHANGE, THE PCB WILL USE 518S0332 LANDPATTERN, BUT BOM WILL STUFF 518S0487 PART

TEMPERATURE SENSE

SYNC_MASTER=ENET SYNC_DATE=11/09/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 62 OF 98	



R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M

R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

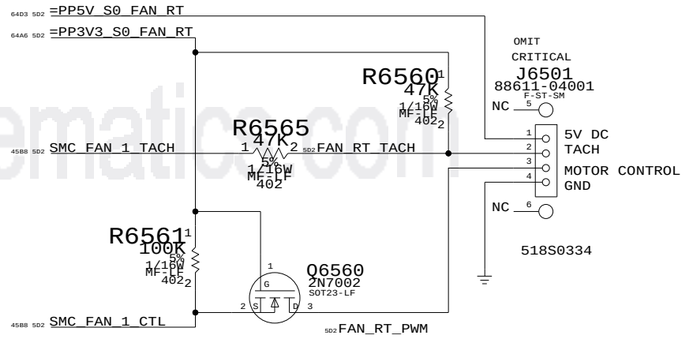
SPI BOOTROM

SYNC_MASTER=MASTER SYNC_DATE=5/23/05

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE	SHT	OF
NONE	63	98



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
518S0486	1	IMPROVED ACES CONNECTOR	J6501	CRITICAL	M42B

Fan

SYNC_MASTER=ENET SYNC_DATE=11/10/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 65 OF 98	

PAGE NOTES

INPUT

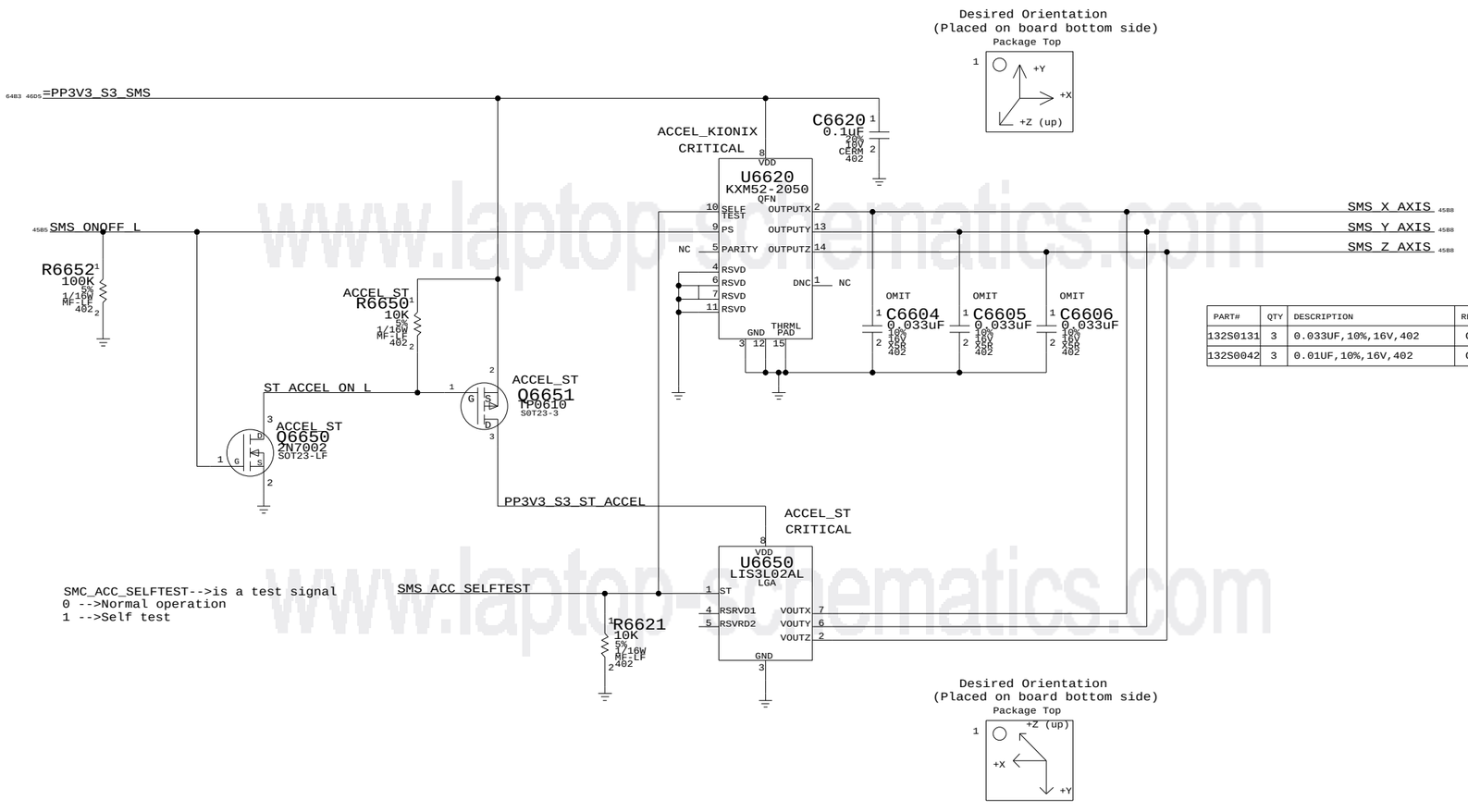
=PP3V3_S3_SMS - 3.3V POWER FOR SMS (STAYS ALIVE IN SLEEP)
SMS_ONOFF_L - CONNECT TO SMC TO BE ABLE TO PUT SMS INTO LOW-POWER MODE

OUTPUT

SMS_ACC_*_AXIS - ACCELEROMETER OUTPUT TO SCU

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
7/26/2005 - REMOVED BOM TABLE AND UPDATED SYMBOL TO KXM52-2050
7/26/2005 - CONNECTED PD PIN TO SMC'S SMS_ONOFF_L
7/26/2005 -



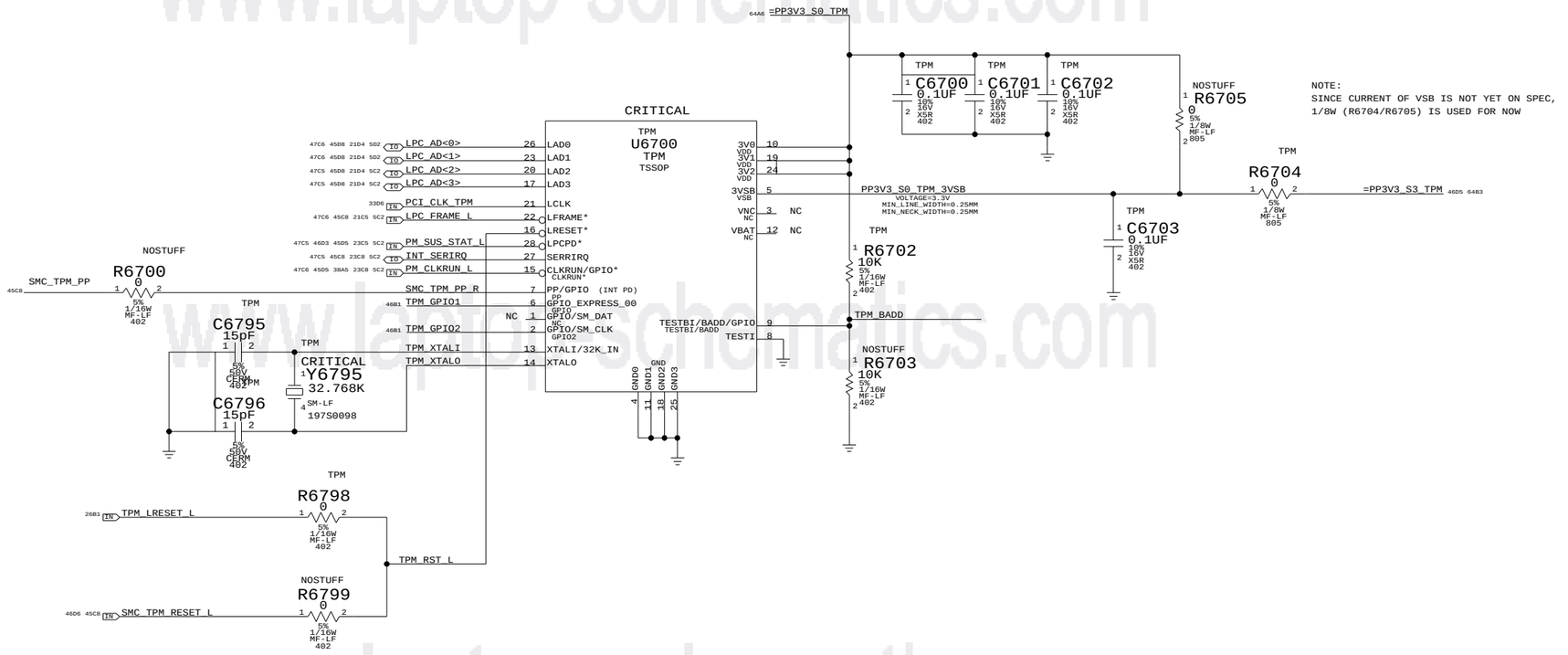
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0131	3	0.033UF,10%,16V,402	C6604,C6605,C6606		ACCEL_KIONIX
132S0042	3	0.01UF,10%,16V,402	C6604,C6605,C6606		ACCEL_ST

SMS

SYNC_MASTER=SMC SYNC_DATE=08/23/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 66 OF 98	



TPM

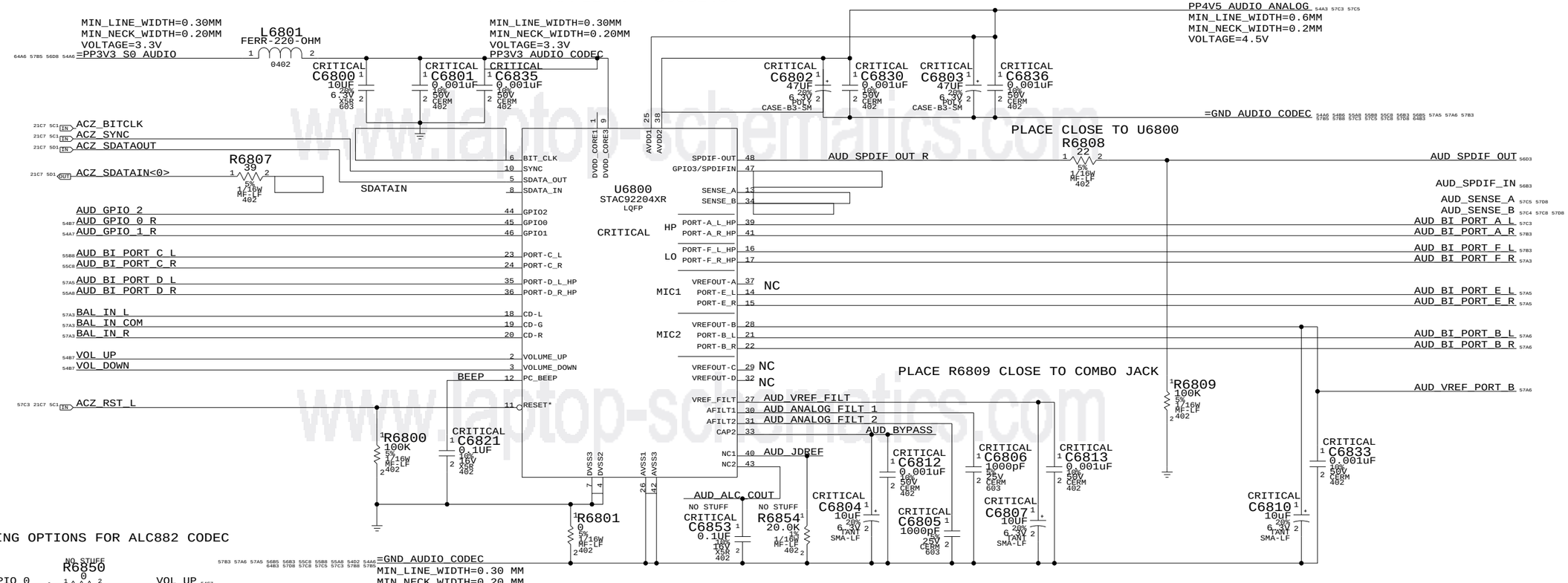
SYNC_MASTER=SMC SYNC_DATE=07/18/2005

APPLE INC.

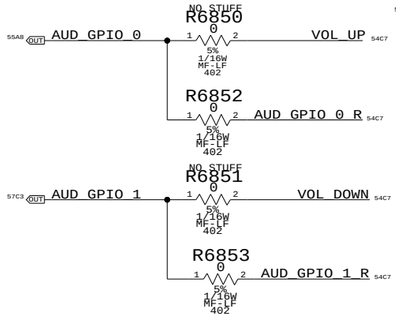
SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 67 OF 98	

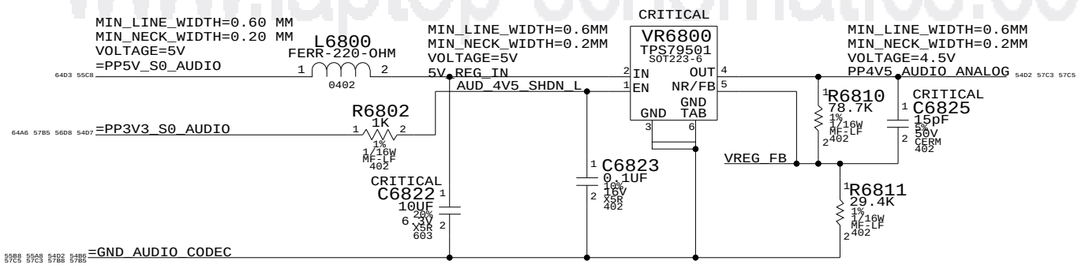
AUDIO CODEC

APPLE P/N 353S1458



STUFFING OPTIONS FOR ALC882 CODEC





4.5V POWER SUPPLY FOR CODEC

AUDIO: CODEC

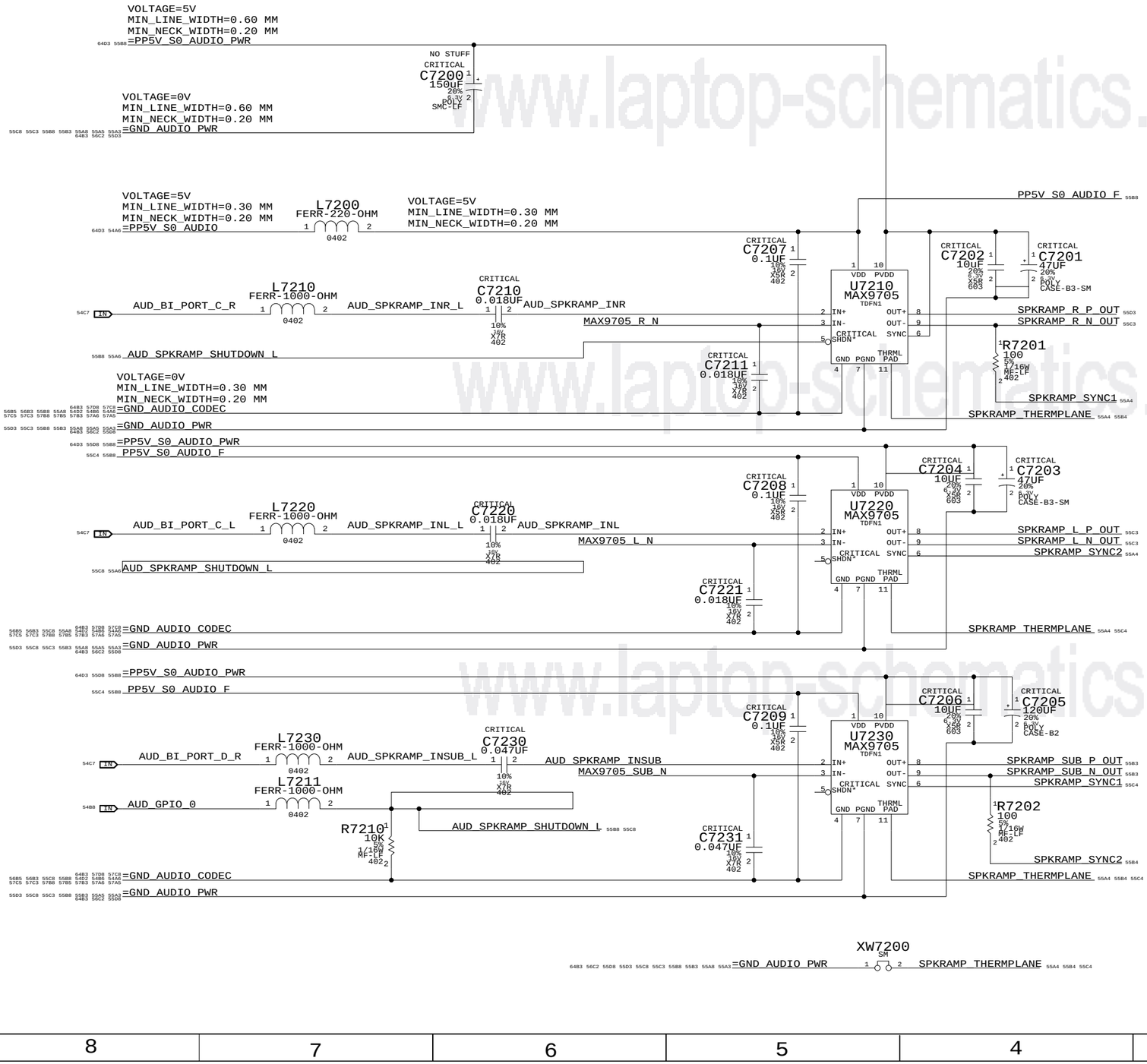
SYNC_MASTER=M42AUDIO SYNC_DATE=08/05/2006

APPLE INC.

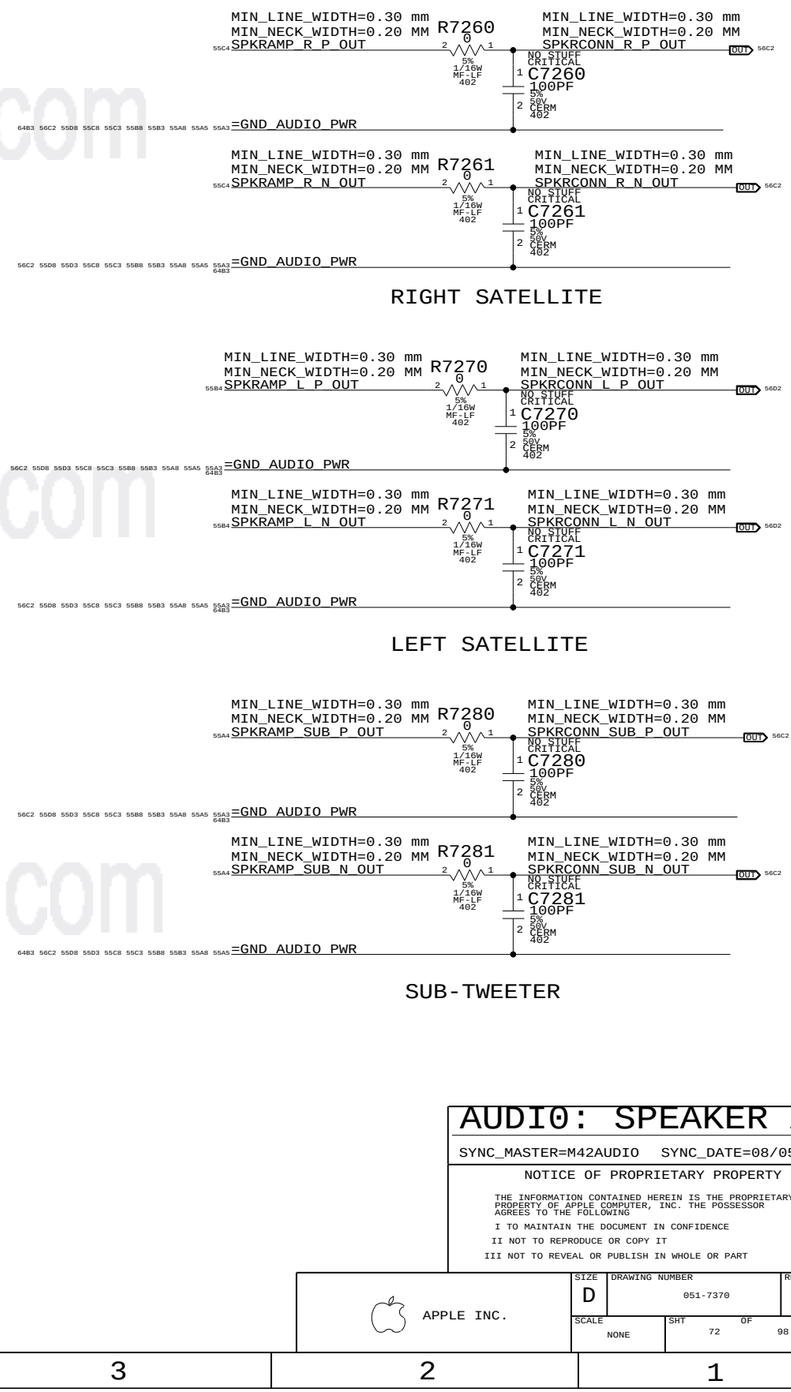
SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 68 OF 98	

SATELLITE & SUB TWEETER AMPLIFIER APN:353S1595

SATELLITE 442 Hz < FC < 736 Hz
SUB 169 Hz < FC < 282 Hz



SPEAKER OUTPUT EMI FILTERS



AUDIO: SPEAKER AMP

SYNC_MASTER=M42AUDIO SYNC_DATE=08/05/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE	SHT	OF
NONE	72	98

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
518S0491	518S0332	?	J7302	IMPROVED TWO PIN CONNECTOR

AUDIO JACK 1: LO/HP CONNECTOR, SPDIF TX

L7390 FERR-220-OHM 0402 =PP3V3_S0_AUDIO

PP3V3_S0_AUDIO_SPDIF

APN:514-0290
APN:514-0317
OMIT
CRITICAL
J7300 AUDIO-OUT F-RT-TH

NO STUFF R7321 0 5% 1/16W MF-LF 402 AUD_CONNJ1_SLEEVE

AUD_CONNJ1_TIPDET

AUD_CONNJ1_RING

AUD_CONNJ1_TIP

AUD_CONNJ1_SLEEVEDET

VCC GND VIN SHLD_PIN SHLD_PIN

NO STUFF C7306 100PF 5% 50V CERM 402

C7300 1UF 10% 6.3V CERM 402

GND_AUDIO_SPDIF_DGND

R7391 0 5% 1/16W MF-LF 402

CRITICAL DZ7300 5.6V-15A 0405

CRITICAL DZ7301 5.6V-15A 0405

CHASSIS_AUDIO_JACK_ISOL

C7307 0.047uF 10% 10V X7R 402

C7308 0.047uF 10% 10V X7R 402

L7300 FERR-120-OHM-1.5A 0402-LF AUD_CONNJ1_SLEEVE_F

L7301 FERR-120-OHM-1.5A 0402-LF

L7302 FERR-1000-OHM 0402 AUD_CONNJ1_TIPDET_F

L7303 FERR-1000-OHM 0402 AUD_CONNJ1_RING_F

L7304 FERR-1000-OHM 0402 AUD_PORTA_R

L7305 FERR-1000-OHM 0402 AUD_CONNJ1_TIP_F

L7306 FERR-1000-OHM 0402 AUD_PORTA_L

L7307 FERR-1000-OHM 0402 AUD_CONNJ1_SLEEVEDET_F

R7300 10K 5% 1/16W MF-LF 402 AUD_J1_SLEEVEDET_R

R7301 4.7 5% 1/16W MF-LF 402 AUD_J1_TIPDET_R

C7302 100PF 5% 50V CERM 402

C7304 100PF 5% 50V CERM 402

C7301 100PF 5% 50V CERM 402

C7303 0.001uF 10% 50V CERM 402

C7305 100PF 5% 50V CERM 402

AUD_SPDIF_OUT

XW7300 SM AUD_J1_COM

XW7301 SM AUD_J2_COM =GND_AUDIO_CODEC

XW7305 SM =GND_CHASSIS_AUDIO_JACK CHASSIS_AUDIO_JACK_ISOL

NO STUFF R7320 0 5% 1/16W MF-LF 402 CHASSIS_AUDIO_JACK_ISOL =GND_AUDIO_CODEC

AUDIO JACK 2: LINE IN CONNECTOR, SPDIF RX

PP3V3_S0_AUDIO_SPDIF

APN:514-0291
APN:514-0318
OMIT
CRITICAL
J7350 AUDIO-IN F-RT-TH

R7349 10 5% 1/16W MF-LF 402 AUD_J2_OPT_OUT

NO STUFF R7322 0 5% 1/16W MF-LF 402 AUD_CONNJ2_SLEEVE

AUD_CONNJ2_TIP

AUD_CONNJ2_TIPDET

AUD_CONNJ2_RING

AUD_CONNJ2_SLEEVEDET

VCC GND VOUT SHLD_PIN SHLD_PIN

NO STUFF C7357 100PF 5% 50V CERM 402

C7350 1UF 10% 6.3V CERM 402

C7351 10uF 20% 6.3V X5R 603

GND_AUDIO_SPDIF_DGND

CRITICAL DZ7350 5.6V-15A 0405

CRITICAL DZ7351 5.6V-15A 0405

CHASSIS_AUDIO_JACK_ISOL

L7350 FERR-220-OHM 0402 AUD_CONNJ2_SLEEVE_F

L7351 FERR-220-OHM 0402

L7352 FERR-1000-OHM 0402 AUD_CONNJ2_TIPDET_F

L7353 FERR-1000-OHM 0402 AUD_CONNJ2_RING_F

L7354 FERR-1000-OHM 0402 AUD_PORTF_R

L7355 FERR-1000-OHM 0402 AUD_CONNJ2_TIP_F

L7356 FERR-1000-OHM 0402 AUD_PORTF_L

L7357 FERR-1000-OHM 0402 AUD_CONNJ2_SLEEVEDET_F

R7350 10K 5% 1/16W MF-LF 402 AUD_J2_SLEEVEDET_R

R7351 4.7 5% 1/16W MF-LF 402 AUD_J2_TIPDET_R

C7353 100PF 5% 50V CERM 402

C7355 100PF 5% 50V CERM 402

C7352 100PF 5% 50V CERM 402

C7354 0.001uF 10% 50V CERM 402

C7356 100PF 5% 50V CERM 402

AUD_SPDIF_IN

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0409	1	CONN,3.5MM COMBO AUDIO OUT,RA,MG3,LF	J7300	CRITICAL	NORMAL
514-0408	1	CONN,3.5MM COMBO AUDIO IN,RA,MG3,LF	J7350	CRITICAL	NORMAL
514-0411	1	CONN,3.5MM COMBO AUDIO OUT,RA,BLACK,LF	J7300	CRITICAL	FANCY
514-0410	1	CONN,3.5MM COMBO AUDIO IN,RA,BLACK,LF	J7350	CRITICAL	FANCY

MIC CONNECTOR

APN:514S0392

CRITICAL J7301 48227-0301 M-RT-SM1

MIC_LO_CONN
MIC_HI_CONN
MIC_SHLD_CONN

SPEAKER CONNECTOR

APN:518S0332

CRITICAL J7302 88611-02001 F-ST-SM

SPKRCONN_L_P_OUT
SPKRCONN_L_N_OUT

NO STUFF R7380 0 5% 1/16W MF-LF 402 =GND_AUDIO_PWR SPKR_SHIELD

OMIT CRITICAL J7303 88611-04001 F-ST-SM

SPKRCONN_SUB_P_OUT
SPKRCONN_SUB_N_OUT
SPKRCONN_R_P_OUT
SPKRCONN_R_N_OUT

APN:518S0334

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
518S0486	1	IMPROVED ACES CONNECTOR	J7303	CRITICAL	M42B

AUDIO SHIELD FILL

AUDIO_SHIELD_PLANE

XW7302 SM CHASSIS_AUDIO_JACK_ISOL
XW7303 SM CHASSIS_AUDIO_JACK_ISOL
XW7304 SM CHASSIS_AUDIO_JACK_ISOL

NO STUFF R7382 0 5% 1/16W MF-LF 402

MIC EMI FILTER

MIC_LO L7370 FERR-1000-OHM 0402 MIC_LO_F L7371 FERR-1000-OHM 0402 MIC_LO_CONN

MIC_HI L7372 FERR-1000-OHM 0402 MIC_HI_F L7373 FERR-1000-OHM 0402 MIC_HI_CONN

MIC_SHIELD L7374 FERR-1000-OHM 0402 MIC_SHIELD_F L7375 FERR-1000-OHM 0402 MIC_SHLD_CONN

C7370 100PF 5% 50V CERM 402

C7371 100PF 5% 50V CERM 402

C7372 100PF 5% 50V CERM 402

CHASSIS_AUDIO_JACK_ISOL

AUDIO: JACK

SYNC_MASTER=M42AUDIO SYNC_DATE=08/05/2006

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE: NONE SHT 73 OF 98

PORT A DETECT

PORT E DETECT(E TELLS H TO TURN ON)

AUD_SENSE_B
AUD_SENSE_A
PP3V3_S0_AUDIO_F
R7401 470K 5% 1/16W MF-LF 402
R7402 47K 5% 1/10W MF-LF 402
AUD_J1_TIPDET_R
AUD_J1_DET_RC
C7401 0.1UF 20% 10V CERM 402
AUD_OUTJACK_INSERT_L
Q7400 2N7002DW-X-F SOT-363
R7406 39.2K 1% 1/16W MF-LF 402
AUD_PORTA_DET_L
NC
R7405 39.2K 1% 1/16W MF-LF 402
AUD_PORTE_DET_L
NC
Q7401 2N7002DW-X-F SOT-363
Q7401 2N7002DW-X-F SOT-363
=GND_AUDIO_CODEC
R7403 100K 5% 1/16W MF-LF 402
AUD_J1_SLEEVEDET_INV
R7461 270K 5% 1/16W MF-LF 402
AUD_J1_SLEEVEDET_R
Q7400 2N7002DW-X-F SOT-363
C7402 0.01UF 10% 16V CERM 402
AUD_J1_SLEEVEDET_R
=GND_AUDIO_CODEC

CODEC PORT ASSIGNMENTS

PORT A :HEADPHONE/LINE OUT
PORT B :MICROPHONE ON BOTH CH (ADC 0)
PORT C :SPEAKER AMP
PORT D :UNUSED
PORT E :SW USES TO TRIGGER DIGITAL OUT
PORT F :LINE IN (ADC 1)
CD INPUT :UNUSED

PORT A HP/LO

PP4V5_AUDIO_ANALOG
R7404 5.11K 1% 1/16W MF-LF 402
R7414 5.11K 1% 1/16W MF-LF 402
AUD_SENSE_A
AUD_SENSE_B
C7404 0.1UF 20% 10V CERM 402
C7414 0.1UF 20% 10V CERM 402
=GND_AUDIO_CODEC
CRITICAL C7430 100UF 20% 6.3V POLY B2
AUD_PORTA_L_R
AUD_PORTA_L
R7434 47.0K 1% 1/16W MF-LF 402
CRITICAL C7431 100UF 20% 6.3V POLY B2
AUD_PORTA_R_R
AUD_PORTA_R
R7435 47.0K 1% 1/16W MF-LF 402

PORT F DETECT

PORT G DETECT

AUD_SENSE_B
PP3V3_S0_AUDIO_F
R7411 470K 5% 1/16W MF-LF 402
R7412 47K 5% 1/10W MF-LF 402
AUD_J2_TIPDET_R
AUD_J2_DET_RC
C7411 0.1UF 20% 10V CERM 402
AUD_INJACK_INSERT_L
Q7402 2N7002DW-X-F SOT-363
R7413 20.0K 1% 1/16W MF-LF 402
NO STUFF
R7460 270K 5% 1/16W MF-LF 402
NO STUFF
R7415 20.0K 1% 1/16W MF-LF 402
AUD_PORTG_DET_L
NC
Q7402 2N7002DW-X-F SOT-363
NO STUFF
C7412 0.01UF 10% 16V CERM 402
=GND_AUDIO_CODEC
AUD_J2_SLEEVEDET_R

HP/LO DE-POP SWITCH APN:353S1459

PP4V5_AUDIO_ANALOG
NO STUFF
R7438 0 5% 1/16W MF-LF 402
ACZ_RST_L
AUD_GPIO_1
R7430 4.7 5% 1/10W MF-LF 603
AUD_BI_PORT_A_L
R7431 4.7 5% 1/10W MF-LF 603
AUD_BI_PORT_A_R
MAX9890_INL
MAX9890_INR
U7400 MAX9890 SHDN* INL INR GND VCC CEXT OUTL OUTR UCSP1
C3 MAX9890_CEXT
AUD_PORTA_L_R
AUD_PORTA_R_R
C7435 0.1UF 20% 10V CERM 402
R7439 10K 5% 1/16W MF-LF 402
=GND_AUDIO_CODEC

L7400

FERR-1000-OHM 0402
=PP3V3_S0_AUDIO
PP3V3_S0_AUDIO_F
CRITICAL C7400 0.1UF 20% 10V CERM 402
=GND_AUDIO_CODEC

PORT F LI

AUD_BI_PORT_F_L
R7432 4.7 5% 1/16W MF-LF 402
AUD_PORTF_L_R
CRITICAL C7432 3.3UF 10% 10V CERM-X5R 805-1
AUD_PORTF_L
R7436 47.0K 1% 1/16W MF-LF 402
=GND_AUDIO_CODEC
R7437 47.0K 1% 1/16W MF-LF 402
AUD_BI_PORT_F_R
R7433 4.7 5% 1/16W MF-LF 402
AUD_PORTF_R_R
CRITICAL C7433 3.3UF 10% 10V CERM-X5R 805-1
AUD_PORTF_R

MIC INPUT CIRCUITRY

R7450 6.8K 1/16W MF-LF 5%
AUD_VREF_PORT_B
MIC_HI
R7451 330 1/16W MF-LF 5%
MIC_IN
C7450 0.1UF 10% 16V X5R 402
AUD_BI_PORT_B_L
MAKE_BASE=TRUE
AUD_BI_PORT_B_R
CRITICAL C7451 0.001UF 10% 16V CERM 402
R7452 100K 5% 1/16W MF-LF 402
CRITICAL C7452 0.001UF 10% 50V CERM 402
NO STUFF
PLACE C7452 NEAR U6800
MIC_LO
XW7400 SM
=GND_AUDIO_CODEC
NO STUFF
R7453 0 5% 1/16W MF-LF 402
MIC_SHIELD
R7454 0 5% 1/16W MF-LF 402
=GND_CHASSIS_AUDIO_MIC

UNUSED CODEC ANALOG PORT TERMINATIONS

AUD_BI_PORT_E_L
AUD_BI_PORT_E_R
AUD_BI_PORT_D_L
R7440 20K 5% 1/16W MF-LF 402
CRITICAL C7440 0.1UF 10% 16V X5R 402
CRITICAL C7441 0.1UF 10% 16V X5R 402
=GND_AUDIO_CODEC
BAL_IN_COM
BAL_IN_R
BAL_IN_L
CRITICAL C7445 0.1UF 10% 16V X5R 402
CRITICAL C7446 0.1UF 10% 16V X5R 402
CRITICAL C7447 0.1UF 10% 16V X5R 402

AUDIO: JACK TRANSLATORS

SYNC_MASTER=M42AUDIO
SYNC_DATE=08/05/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE	SHT	OF
NONE	74	98

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7501,C7508	KEMET T520V336M016ATE045?650
128S0093	128S0092	?	C7509,C7517	KEMET T520V336M016ATE045?650

DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

Note 1: C7532,C7533 = 27.4 Ohm For Validating CPU Only.

R0802/R0803 **on the CPU page** protect the IMVP6 if the CPU is not installed

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1465	1	ISL6262	U7500		M42
353S1461	1	ISL9504	U7500		M42A

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_FET_RC1	0.25 MM	0.25 MM
IMVP6_VSUM_R1	0.25 MM	0.25 MM
IMVP6_VO_R1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM
IMVP6_FET_RC2	0.25 MM	0.25 MM
IMVP6_VSUM_R2	0.25 MM	0.25 MM
IMVP6_VO_R2	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
CPU_VID_R<0..6>	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
CPU_VCCSENSE_P	0.25 MM	0.25 MM
CPU_VCCSENSE_N	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCORE REGULATOR

IMVP6 CPU VCore Regulator

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

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II NOT TO REPRODUCE OR COPY IT

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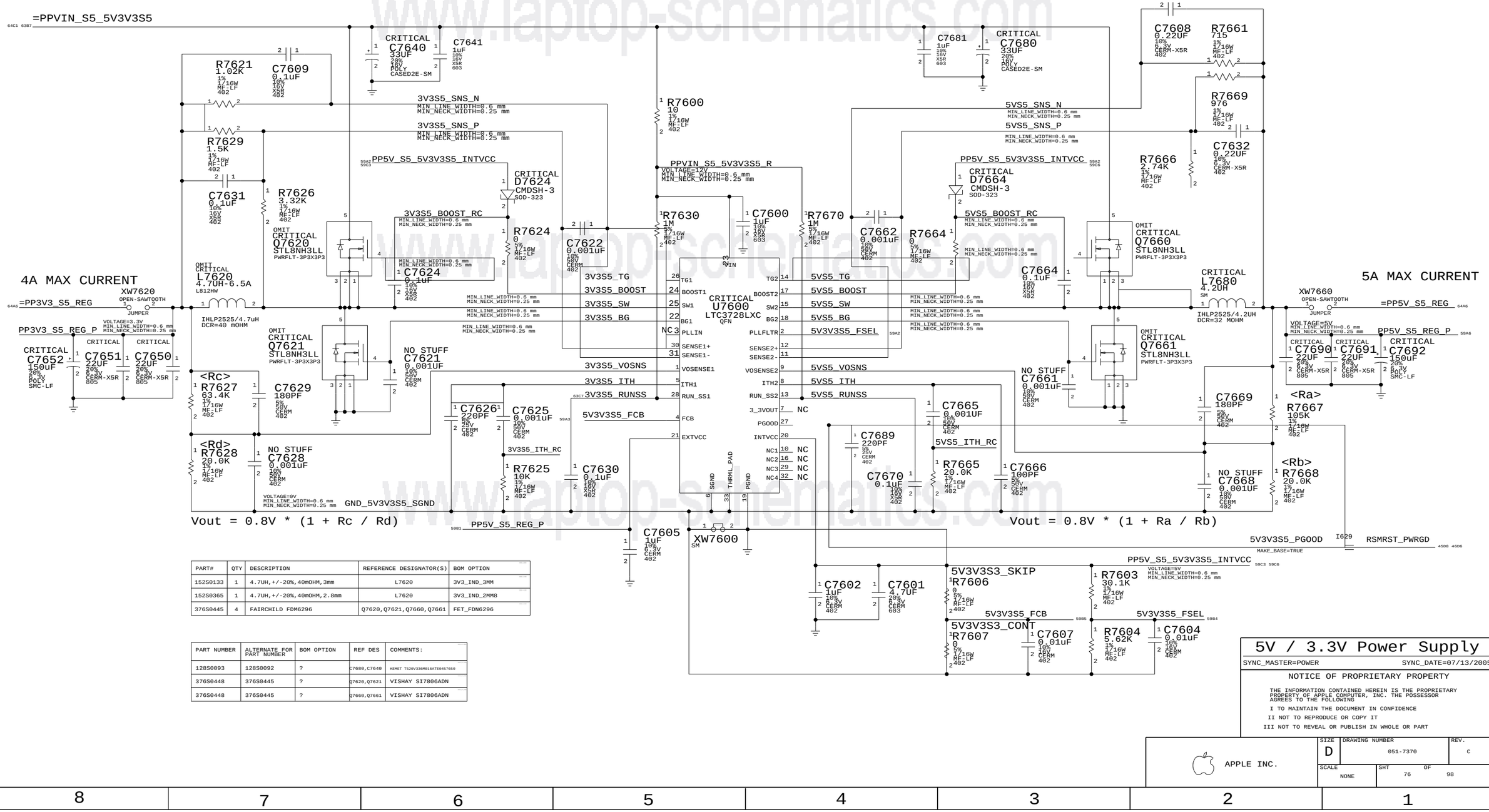
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 75 OF 98	

5V/3.3V POWER SUPPLY



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S0133	1	4.7UH,+/-20%,40mOHM,3mm	L7620	3V3_IND_3MM
152S0365	1	4.7UH,+/-20%,40mOHM,2.8mm	L7620	3V3_IND_2MM8
376S0445	4	FAIRCHILD FDM6296	Q7620,Q7621,Q7660,Q7661	FET_FDN6296

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7680,C7640	KEMET T520V336M016ATE045 7650
376S0448	376S0445	?	Q7620,Q7621	VISHAY SI7806ADN
376S0448	376S0445	?	Q7660,Q7661	VISHAY SI7806ADN

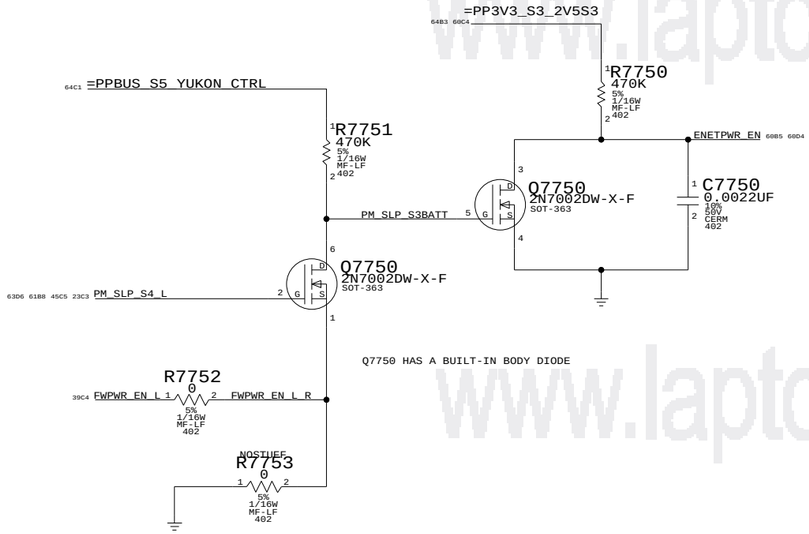
5V / 3.3V Power Supply

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 76 OF 98	

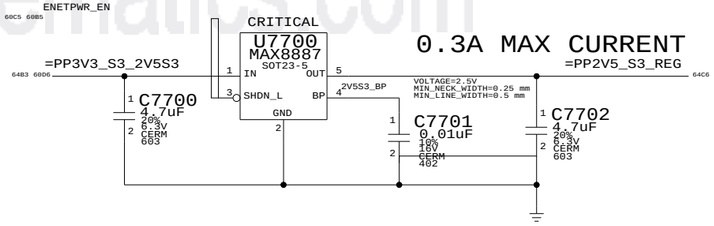
YUKON POWER CONTROL

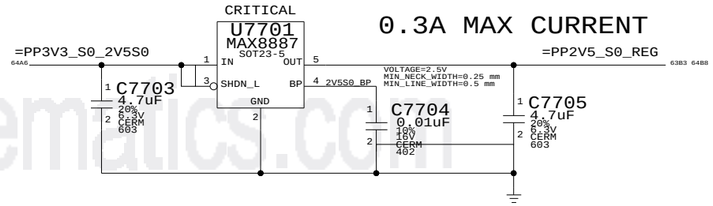


NAME	PM_SLP_S4_L	FWPWR_EN_L	PM_SLP_S3BATT	ENETPWR_EN
LOGIC	S3 | S0	~S0 | ~SMC_PS_ON		POWER YUKON
S3 ON BATTERY	TRUE (3.3V)	TRUE (PBUS 12.6V)	TRUE (PBUS 12.6V)	FALSE (0V)
S0 OR S3 ON AC	TRUE (3.3V)	FALSE (0V)	FALSE (0V)	TRUE (3.3V)
S5 ON AC	FALSE (0V)	TRUE (PBUS 12.6V)	TRUE (PBUS 12.6V)	FALSE (0V)
S5 ON BATT	FALSE (0V)	FALSE (0V)	TRUE (PBUS 12.6V)	FALSE (0V)

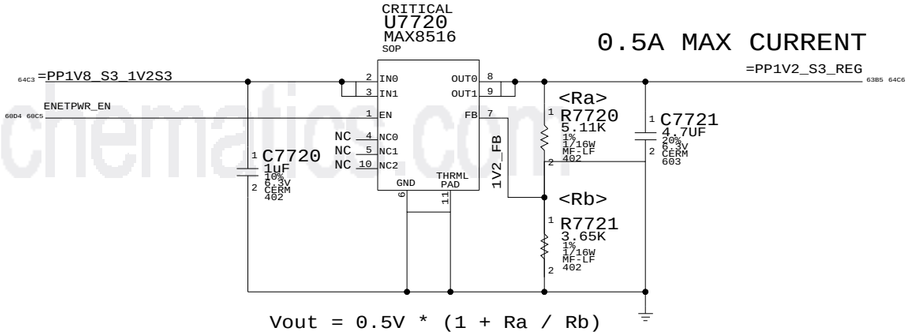
NOTE: IF CHANGE TO STUFFING R7753 THEN ENETPWR_EN IS BUFFERED PM_SLP_S4_L

2.5V REGULATORS





1.2V REGULATOR



Vout = 0.5V * (1 + Ra / Rb)

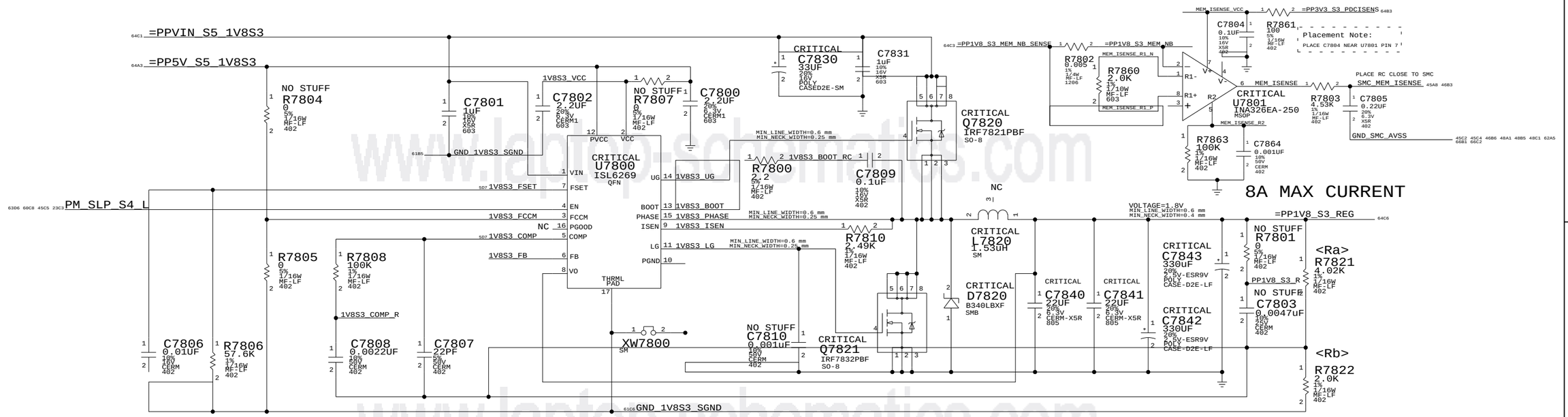
2.5V/1.2V Regulator

SYNC_MASTER=ENET SYNC_DATE=12/06/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 77 OF 98	

1.8V POWER SUPPLY



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7830	KEMET T520V336M016ATE045760

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0094	128S0060	?	C7842,C7843	PANASONIC EEFSX0D331ER
128S0095	128S0060	?	C7842,C7843	PANASONIC EEFSX0D331XE

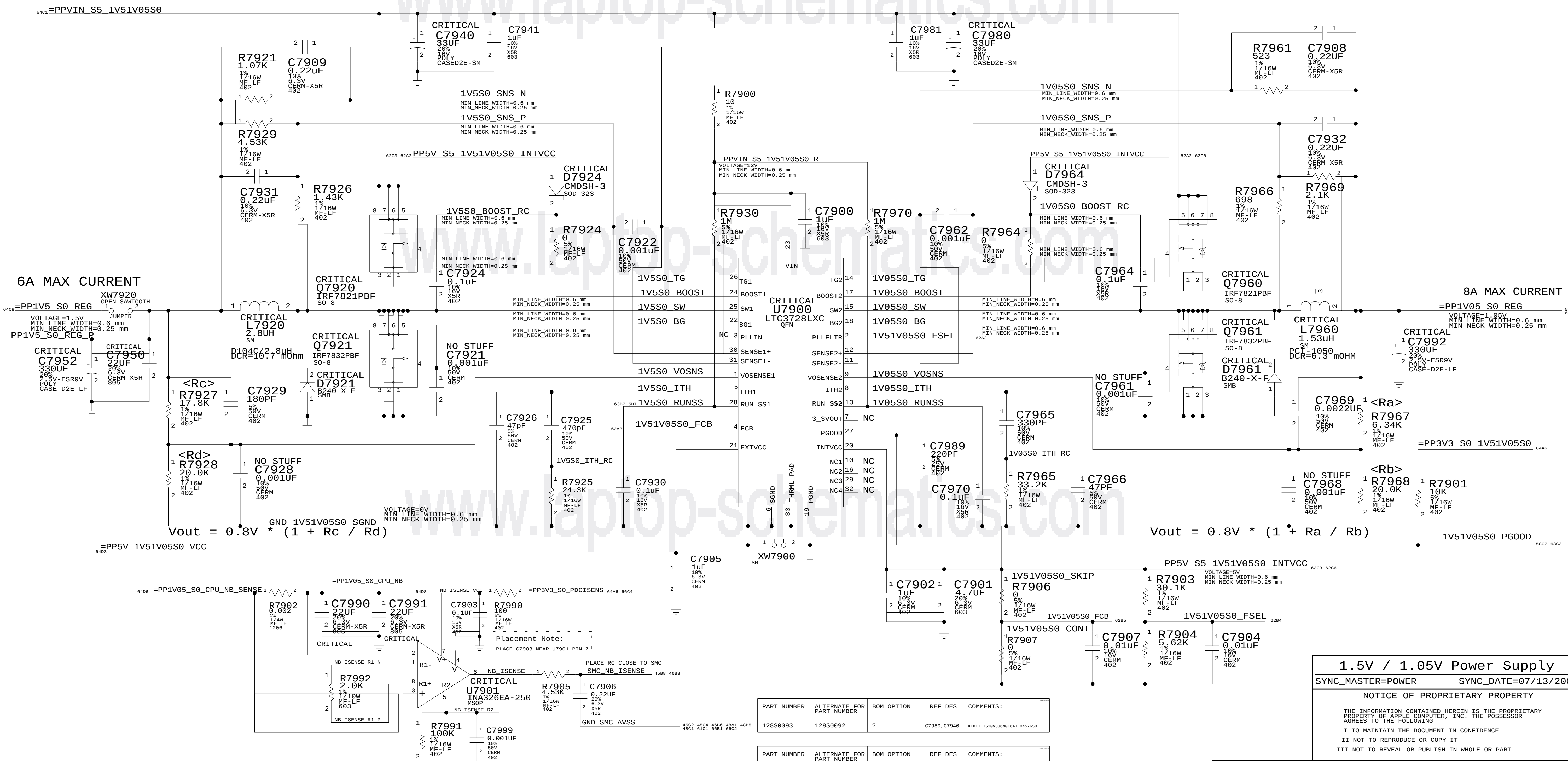
1.8V Supply

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 78 OF 98	

1.5V/1.05V POWER SUPPLY



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7980,C7940	KEMET T520V336M016ATE0457650

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0094	128S0060	?	C7952,C7992	PANASONIC EEFSX0D331ER
128S0095	128S0060	?	C7952,C7992	PANASONIC EEFSX0D331XE

1.5V / 1.05V Power Supply

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

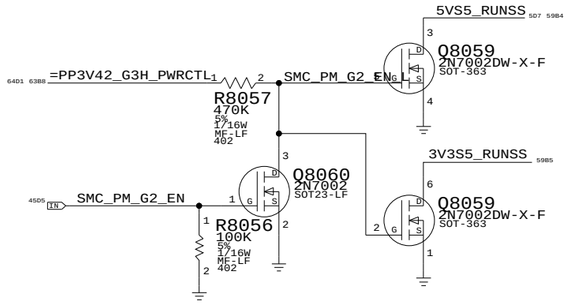
SCALE	SHT	OF
NONE	79	98

POWER CONTROL SIGNALS

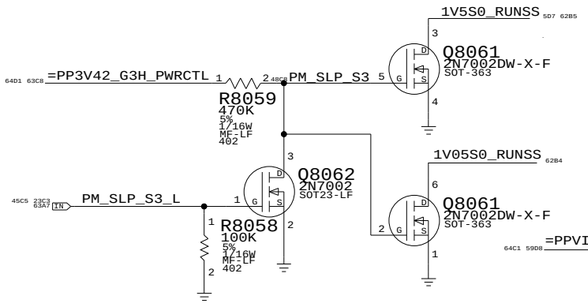
These rails are monitored by LTC2908

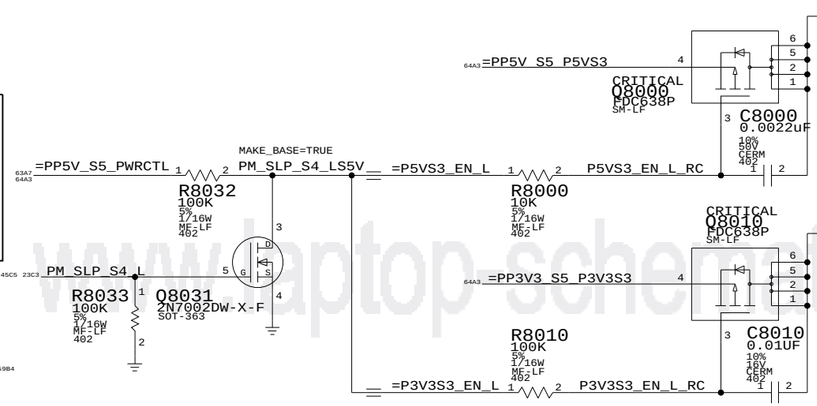
State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

5V/3.3V S5 RUN/SS CONTROL



1.5V/1.05V S0 RUN/SS CONTROL





5V S3 FET

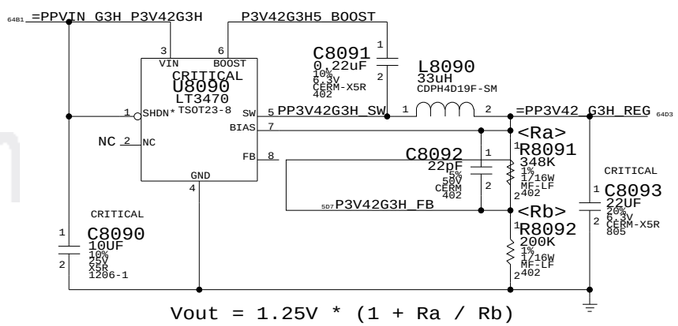
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	100 mA

3.3V S3 FET

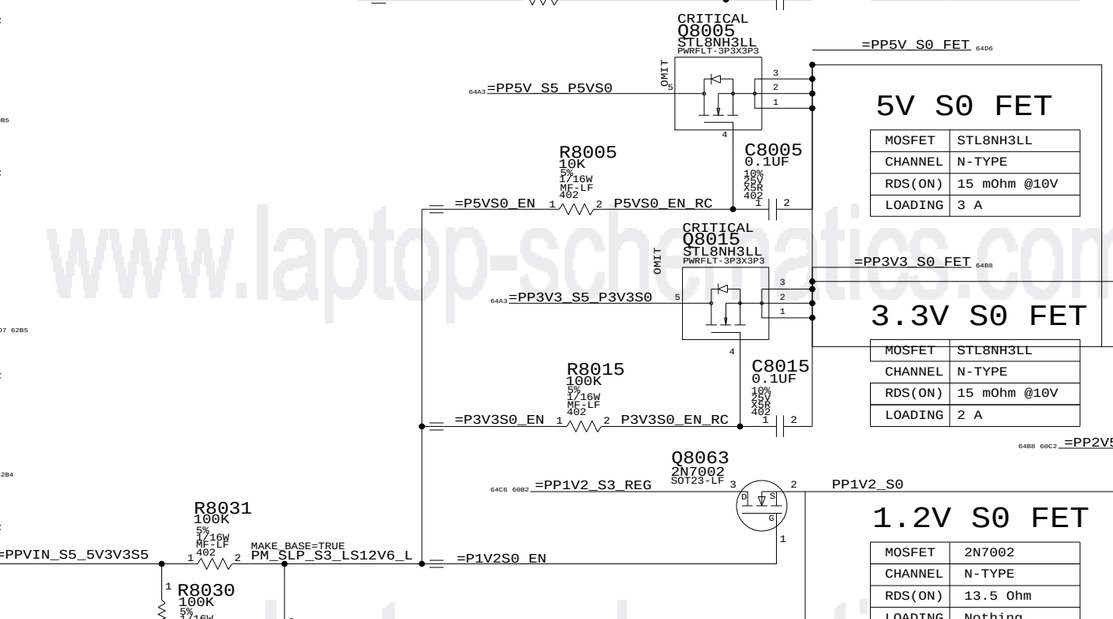
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	65 mOhm @2.5V
LOADING	1 A

3.425V "G3Hot" SUPPLY

Supply needs to guarantee 3.31V delivered to SMC VRef generator



Vout = 1.25V * (1 + Ra / Rb)



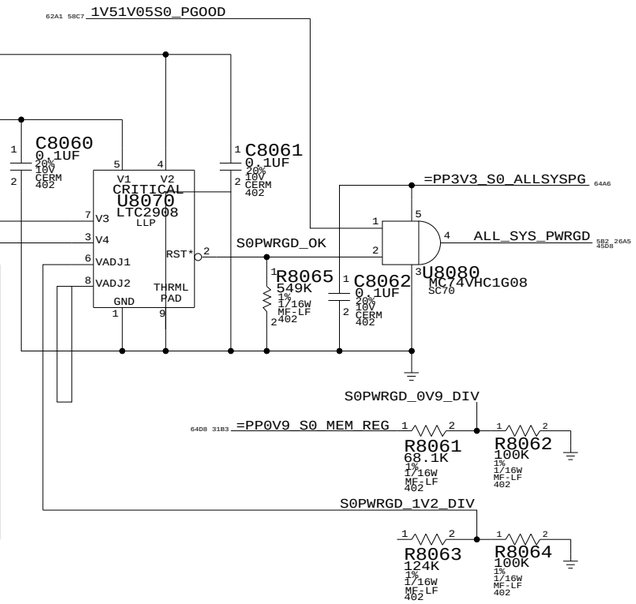
5V S0 FET

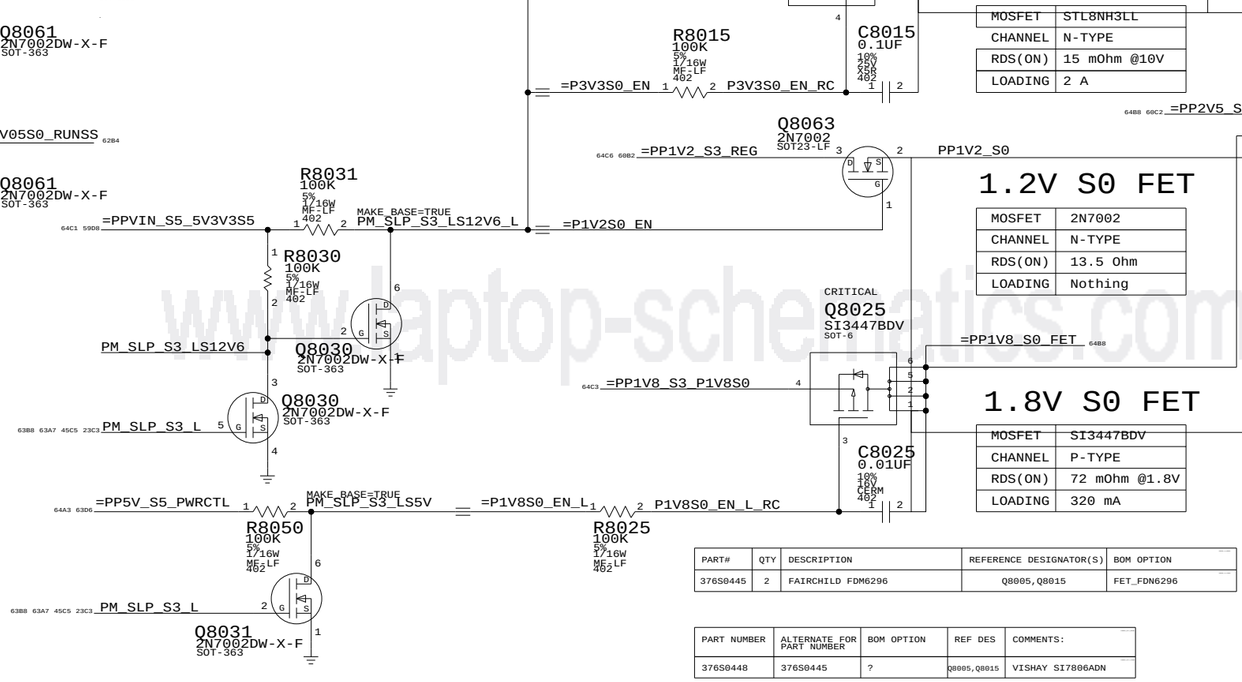
MOSFET	STL8NH3LL
CHANNEL	N-TYPE
RDS(ON)	15 mOhm @10V
LOADING	3 A

3.3V S0 FET

MOSFET	STL8NH3LL
CHANNEL	N-TYPE
RDS(ON)	15 mOhm @10V
LOADING	2 A

ALL SYSTEM PWRGD CIRCUIT





1.2V S0 FET

MOSFET	2N7002
CHANNEL	N-TYPE
RDS(ON)	13.5 Ohm
LOADING	Nothing

1.8V S0 FET

MOSFET	SI3447BDV
CHANNEL	P-TYPE
RDS(ON)	72 mOhm @1.8V
LOADING	320 mA

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S0445	2	FAIRCHILD FDM6296	Q8005,Q8015	FET_FDN6296

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0448	376S0445	?	Q8005,Q8015	VISHAY SI7806ADN

S3/S0 FETS, G3H SUPPLY

SYNC_MASTER=ENET SYNC_DATE=08/30/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE: NONE SHT 80 OF 98

"S0" RAILS ONLY ON IN RUN

PPVCORE_CPU_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.4MM
VOLTAGE=0.9V

(REGULATOR OUTPUT CPU VCORE PWR) =PPVOUT_S0_IMVP6_REG (CPU VCORE PWR) =PPVCORE_S0_CPU

PP0V9_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.4MM
VOLTAGE=0.9V

(LDO OUTPUT 0.9V PWR) =PP0V9_S0_MEM_REG (DDR2 TERMINATION 0.9V PWR) =PP0V9_S0_MEM_TERM

PP1V05_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.05V

(REGULATOR OUTPUT 1.05V PWR) =PP1V05_S0_REG
(ICH CPU I/O 1.05V PWR) =PP1V05_S0_SB_CPU_IO
(ICH VCORE 1.05V PWR) =PPVCORE_S0_SB
=PP1V05_S0_CPU_NB_SENSE

PP1V05_S0_CPU_NB
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.4MM
VOLTAGE=1.05V

=PP1V05_S0_CPU_NB
(MCH CORE 1.05V PWR) =PPVCORE_S0_NB
(CPU FSB 1.05V PWR) =PP1V05_S0_CPU
(MCH FSB 1.05V PWR) =PP1V05_S0_FSB_NB
=PP1V05_S0_NB_VTT
(MCH FSB 1.05V PWR) =PP1V05_S0_NB

PP1V5_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.4MM
VOLTAGE=1.5V

(REGULATOR OUTPUT 1.5V PWR) =PP1V5_S0_REG
(CPU AVDD 1.5V PWR) =PP1V5_S0_CPU
(MCH PCIE GRAPHICS O/P COMPENSATION 1.5V PWR) =PP1V5_S0_NB_PCIE
(MCH DDR DLL&IO, FSB HSIO&IO PWR 1.5V) =PP1V5_S0_NB_VCCAUX
(MCH DIGITAL DIVIDER IN HMPLL 1.5V PWR) =PP1V5_S0_NB_VCCD_HMPLL
(MCH LVDS DIGITAL 1.5V PWR) =PP1V5_S0_NB_VCCD_LVDS
(HOST/MEMORY PLL 1.5V PWR) =PP1V5_S0_NB_PLL
=PP1V5_S0_NB
(MCH TVDAC DEDICATED/QUIET PWR 1.5V) =PP1V5_S0_NB_TVDAC
(MCH 3GIO[PCIE/DMI] 1.5V PWR) =PP1V5_S0_NB_3G
(MCH 3GIO PLL 1.5V PWR) =PP1V5_S0_NB_3GPLL
(ICH LOGIC&IO[ARX] 1.5V PWR) =PP1V5_S0_SB_VCC1_5_A_ARX
(ICH SATA PLL 1.5V PWR) =PP1V5_S0_SB_VCCSATAPLL
(ICH LOGIC&IO[ATX] 1.5V PWR) =PP1V5_S0_SB_VCC1_5_A_ATX
(ICH USB PLL 1.5V PWR) =PP1V5_S0_SB_VCCUSBPLL
(ICH USB CORE 1.5V PWR) =PP1V5_S0_SB_VCC1_5_A_USB_CORE
(ICH LOGIC&IO 1.5V PWR) =PP1V5_S0_SB_VCC1_5_A
=PP1V5_S0_SB
(WIRELESS CARD 1.5V PWR) =PP1V5_S0_AIRPORT

PP1V8_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.4MM
VOLTAGE=1.8V

(COME FROM S3 TO S0 MOSFET) =PP1V8_S0_FET (DDR2 TERMINATION REGULATOR 1.8V SWITCH PWR)
(TMDS 1.8V PWR) =PP1V8_S0_TMDS

PP2V5_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=2.5V

(COME FROM S3 TO S0 MOSFET) =PP2V5_S0_REG
(MCH H/V SYNC 2.5V PWR) =PP2V5_S0_NB_VCCSYNC
(MCH LVDS DATA/CLK TX 2.5V PWR) =PP2V5_S0_NB_VCC_TXLVDS
(MCH PCIE/DMI BAND GAP 2.5V PWR) =PP2V5_S0_NB_VCCA_3GBG
(MCH LVDS ANALOG 2.5V PWR) =PP2V5_S0_NB_VCCA_LVDS
(MCH CRTDAC ANALOG 2.5V PWR) =PP2V5_S0_NB_CRTDAC
(TMDS 2.5V PWR) =PP2V5_S0_TMDS
=PP2V5_S0_NB_DISP_PLL

PP3V3_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V

(COME FROM S5 TO S0 MOSFET) =PP3V3_S0_FET
(MCH HV BUFFER 3.3V PWR) =PP3V3_S0_NB_VCC_HV
=PP3V3_S0_SB
(ICH GPIO PULLS 3.3V PWR) =PP3V3_S0_SB_GPIO
(ICH IO BUFFER 3.3V PWR) =PP3V3_S0_SB_VCC3_3
(ICH PCI I/O 3.3V PWR) =PP3V3_S0_SB_VCC3_3_PCI
(ICH IDE I/O 3.3V PWR) =PP3V3_S0_SB_VCC3_3_IDE
(ICH PCI PULLS 3.3V PWR) =PP3V3_S0_SB_PCI
(ICH PM PULLS 3.3V PWR) =PP3V3_S0_SB_PM
(PATA PULLS 3.3V PWR) =PP3V3_S0_PATA
(SATA 3.3V PWR) =PP3V3_S0_SMC_LS
(MCH PULLS 3.3V PWR) =PP3V3_S0_NB
(ICH LAN I/F 3.3V PWR, NEED TO CHECK INTEL) =PP3V3_S0_SB_VCCLAN3_3
(ICH INTEL HDA CORE 3.3V PWR) =PP3V3_S0_SB_3V3_1V5_VCCHDA
(DIMM SPD 3.3V PWR) =PPSPD_S0_MEM
(CLOCK GENERATOR 3.3V PWR) =PP3V3_S0_CK410
(WIRELESS CARD 3.3V PWR) =PP3V3_S0_AIRPORT
(TPM 3.3V PWR) =PP3V3_S0_TPM
(AUDIO 3.3V PWR) =PP3V3_S0_AUDIO
(TMDS 3.3V PWR) =PP3V3_S0_TMDS
(CPU THERMAL SENSOR 3.3V PWR) =PP3V3_S0_THRM_SNR
(ISL6262 3V3) =PP3V3_S0_IMVP6
=PP3V3_S0_RSTBUF
=PP3V3_S0_SMBUS_SB
=PP3V3_S0_SMBUS_SMC_0
=PP3V3_S0_SMBUS_SMC_MLB
=PP3V3_S0_ALLSYSPG
=PP3V3_S0_FAN_RT
=PP3V3_S0_LCD
=PP3V3_S0_PBATTISENS
=PP3V3_S0_PDCISENS
=PP3V3_S0_CPUPOWER
=PP3V3_S0_SMBUS_SMC_BSA
=PP3V3_S0_1V51V05S0
=PP3V3_S0_2V5S0
(FIREWIRE DIGITAL 3.3V PWR) =PP3V3_S0_FW
=PP3V3_S0_ENET

PP5V_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=5V

(COME FROM S5 TO S0 MOSFET) =PP5V_S0_FET
=PP5V_S0_SB
(SATA 5V PWR) =PP5V_S0_SATA
(DDR2 TERMINATION) =PP5V_S0_MEMVTT
(AUDIO 5V PWR) =PP5V_S0_AUDIO
(AUDIO SPEAKER 5V PWR) =PP5V_S0_AUDIO_PWR
(LPC DEBUG BOARD 5V PWR) =PP5V_S0_LPCPLUS
(MCH TV 3.3V LDO) =PP5V_S0_NB_TVDAC
(ISL6262 VDD) =PP5V_S0_IMVP6
(LTC3728LXC EXTVCC) =PP5V_1V51V05S0_VCC
(TMDS 5V PWR) =PP5V_S0_TMDS
=PP5V_S0_FAN_RT
=PP5V_S0_LCD
=PP5V_S0_ISENSECAL

"S3" RAILS
ON IN RUN AND SLEEP

PP1V2_S3
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.32MM
VOLTAGE=1.2V

(LDO OUTPUT 1.2V PWR) =PP1V2_S3_REG (ENET 1.2V PWR) =PP1V2_S3_ENET

PP1V8_S3
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=1.8V

(REGULATOR OUTPUT 1.8V PWR) =PP1V8_S3_REG (DDR2 DIMM 1.8V PWR) =PP1V8_S3_MEM
=PP1V8_S3_P1V8S0
=PP1V8_S3_MEMVTT
=PP1V8_S3_MEM_NB_SENSE
=PP1V8_S3_1V2S3

PP1V8_S3_MEM_NB
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.4MM
VOLTAGE=1.8V

=PP1V8_S3_MEM_NB (MCH DDR2 1.8V PWR)

PP2V5_S3
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=2.5V

(REGULATOR OUTPUT 2.5V PWR) =PP2V5_S3_REG (ENET 2.5V PWR) =PP2V5_S3_ENET

PP3V3_S3
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.16 MM
VOLTAGE=3.3V

(COME FROM S5 TO S3 MOSFET) =PP3V3_S3_FET
=PP3V3_S3_SMBUS_SMC_RMT
(ETHERNET 3.3V PWR) =PP3V3_S3_ENET
(BLUETOOTH 3.3V PWR) =PP3V3_S3_BT
(ACCELEROMETER 3.3V PWR) =PP3V3_S3_SMS
(TPM 3.3V SUSPEND PWR) =PP3V3_S3_TPM
(TPS62050 VIN) =PP3V3_S3_2V5S3
(FIREWIRE CHIP PCI SIGNAL INDICATOR) =PP3V3_S3_PCI
=PP3V3_S3_RSTGATE
=PP3V3_S3_AIRPORT_AUX
=PP3V3_S3_FW
=PP3V3_S3_PDCISENS

PP5V_S3
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
VOLTAGE=5V

(COME FROM S5 TO S3 MOSFET) =PP5V_S3_FET
(ISL6269 PVCC)
(SYSTEM LED PWR) =PP5V_S3_SYSLED
(USB IO PORT 5V PWR) =PP5V_S3_CAMERA
(USB IR CONTROLLER 5V PWR) =PP5V_S3_IR
=PP5V_S3_GEYSER

"S5" RAILS
ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

PP3V3_S5
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
VOLTAGE=3.3V

(REGULATOR OUTPUT 3.3V PWR) =PP3V3_S5_REG
=PP3V3_S5_SB
(ICH USB CTL PULLS 3.3V PWR) =PP3V3_S5_SB_USB
(ICH PM 3.3V PWR) =PP3V3_S5_SB_PM
(ICH SUSPEND 3.3V PWR) =PP3V3_S5_SB_VCCSUS3_3
(ICH SUSPEND USB 3.3V PWR) =PP3V3_S5_SB_VCCSUS3_3_USB
(ICH SUSPEND PULLS 3.3V PWR) =PP3V3_S5_SB_IO
(ICH INTEL HDA SUSPEND 3.3V PWR) =PP3V3_S5_SB_3V3_1V5_VCCSUSHDA
(SPI BOOTROM PWR) =PP3V3_S5_ROM
=PP3V3_S5_P3V3S3
=PP3V3_S5_P3V3S0
=PP3V3_S5_FWLATEVG
=PP3V3_S5_LCD

PP5V_S5
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
VOLTAGE=5V

(REGULATOR OUTPUT 5 PWR) =PP5V_S5_REG
=PP5V_S5_SB
=PP5V_S5_P5VS3
=PP5V_S5_PWRCTL
=PP5V_S5_P5VS0
=PP5V_S5_USB
=PP5V_S5_PATA (PATA 5V PWR)
=PP5V_S5_1V8S3

G3 HOT

PP3V42_G3H
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.425V

=PP3V42_G3H_REG
=PP3V42_G3H_SMCVREF
=PP3V42_G3H_SMBUS_SMC_BSA
=PP3V42_G3H_PWRCTL
=PP3V42_G3H_LIDSWITCH
(LPC DEBUG BOARD) =PP3V42_G3H_LPCPLUS
=PP3V42_G3H_SB_RTC
=PP3V42_G3H_ACIN
(SMC 32.768KHz OSC) =PP3V42_G3H_SMC_CLK
(SMC 3.3V PWR) =PP3V42_G3H_SMC

PBUS HOT

PPBUSB_G3H
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
VOLTAGE=12.6V

=PPBUSA_G3H (INVERTER PBUS PWR)
(ISL6262 VIN)
(LTC3728 VIN) =PPBUS_S5_INV
=PPVIN_S5_IMVP6
=PPVIN_S5_1V51V05S0

=PPBUSB_G3H (LTC3728 VIN)
(ISL6269 VIN) =PPVIN_S5_5V3V3S5
=PPVIN_S5_1V8S3
(FIREWIRE PORT PBUS PWR) =PPBUS_S5_FWPWRSW
(YUKON POWER CONTROL) =PPBUS_S5_YUKON_CTRL

PP18V5_G3H
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.5V

=PP18V5_G3H_INRUSH (DC-IN OUTPUT 18.5V PWR)
(CHARGER INPUT 18.5V PWR) =PP18V5_G3H_CHGR
(SMC INPUT 18.5V PWR)

DCIN G3HOT

PPDCIN_G3H
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
VOLTAGE=18.5V

=PPDCIN_G3H
=PPVBATT_G3H
=PPVIN_G3H_P3V42G3H

GND RAILS

XW8101 SM
XW8102 SM

=GND_AUDIO_CODEC GND_AUDIO_CODEC MAKE_BASE=TRUE
=GND_AUDIO_PWR GND_AUDIO_PWR MAKE_BASE=TRUE

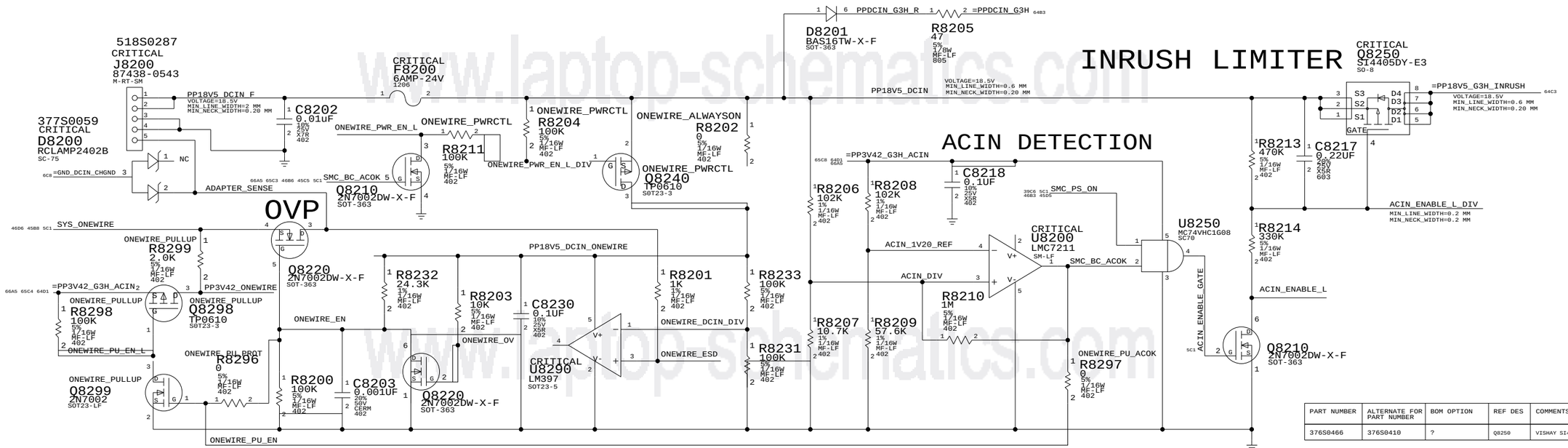
Power Conn / Alias

SYNC_MASTER=ENET SYNC_DATE=11/16/2005

APPLE INC.

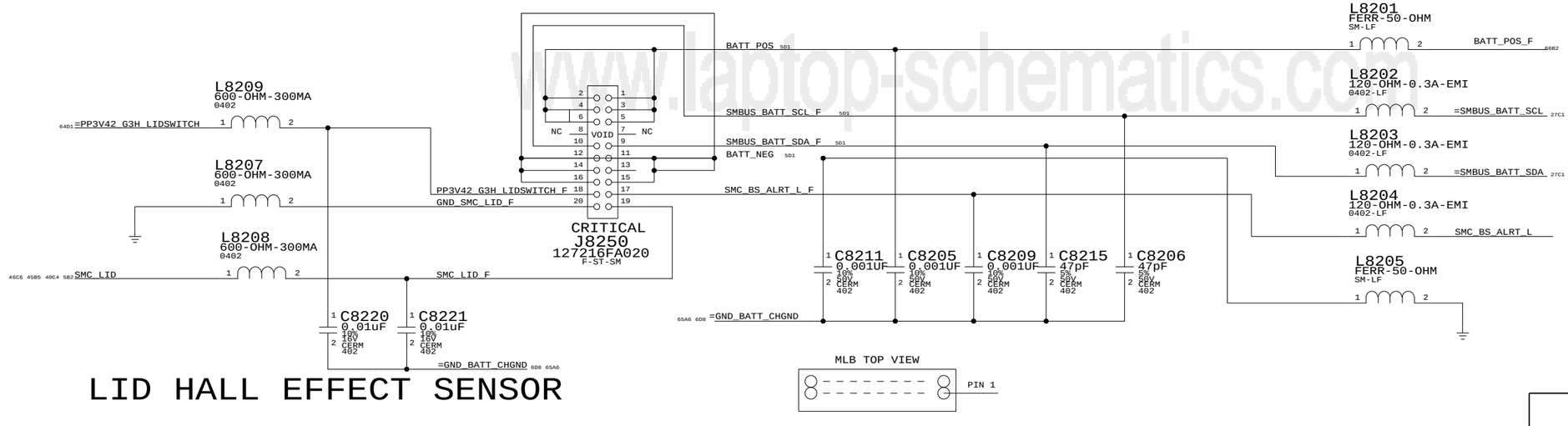
SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 81 OF 98	

DC-JACK INTERFACE



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0466	376S0410	?	Q8250	VISHAY SI4413ADY

BATTERY INTERFACE



LID HALL EFFECT SENSOR

DC-In & Battery Connectors

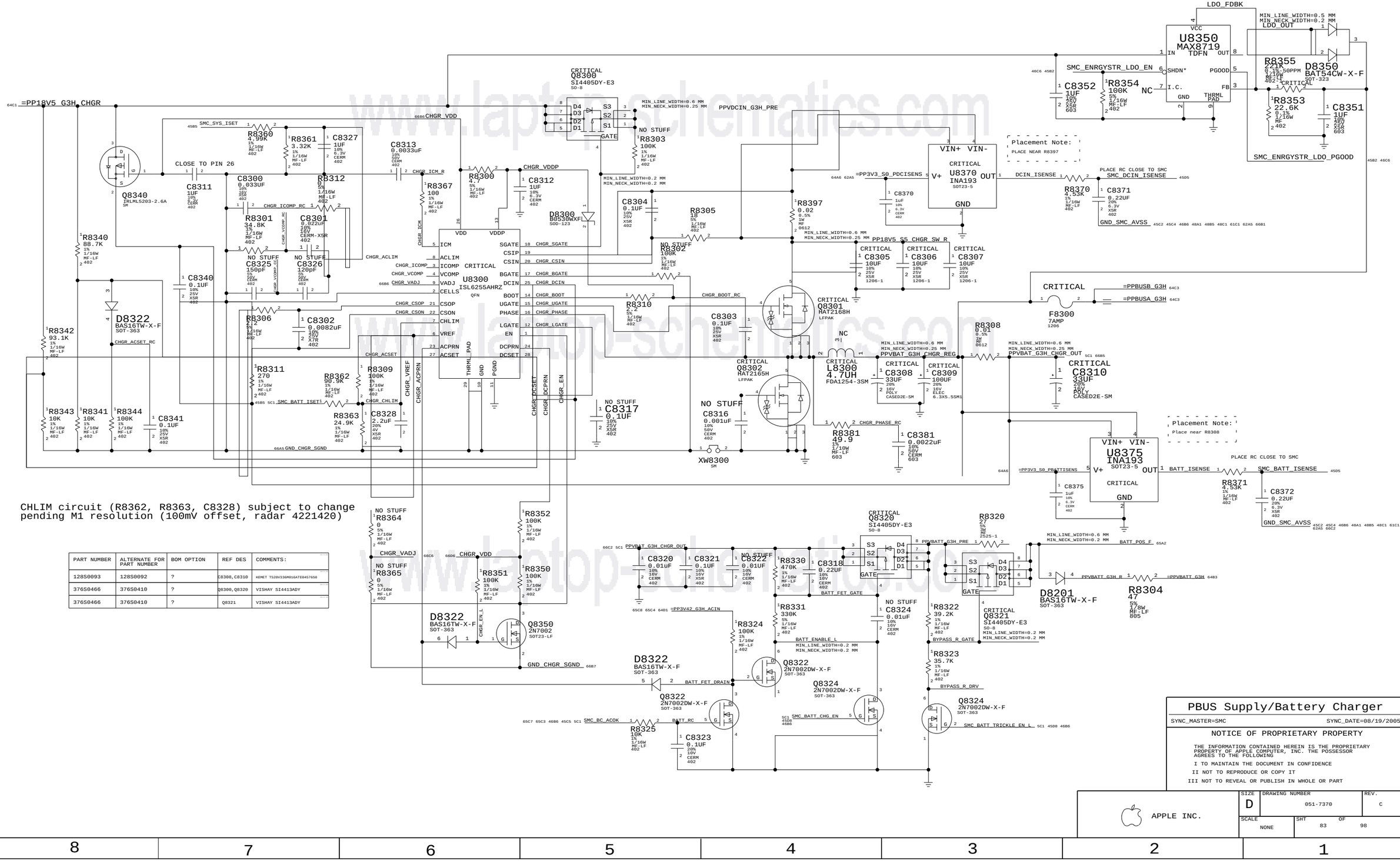
SYNC_MASTER=POWER SYNC_DATE=07/13/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE: NONE SHT 82 OF 98

PBUS SUPPLY / BATTERY CHARGER



CHLIM circuit (R8362, R8363, C8328) subject to change pending M1 resolution (100mV offset, radar 4221420)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C8308,C8310	KEMET T520V336M016ATE0457650
376S0466	376S0410	?	Q8300,Q8320	VISHAY SI4413ADY
376S0466	376S0410	?	Q8321	VISHAY SI4413ADY

PBUS Supply/Battery Charger

SYNC_MASTER=SMC SYNC_DATE=08/19/2005

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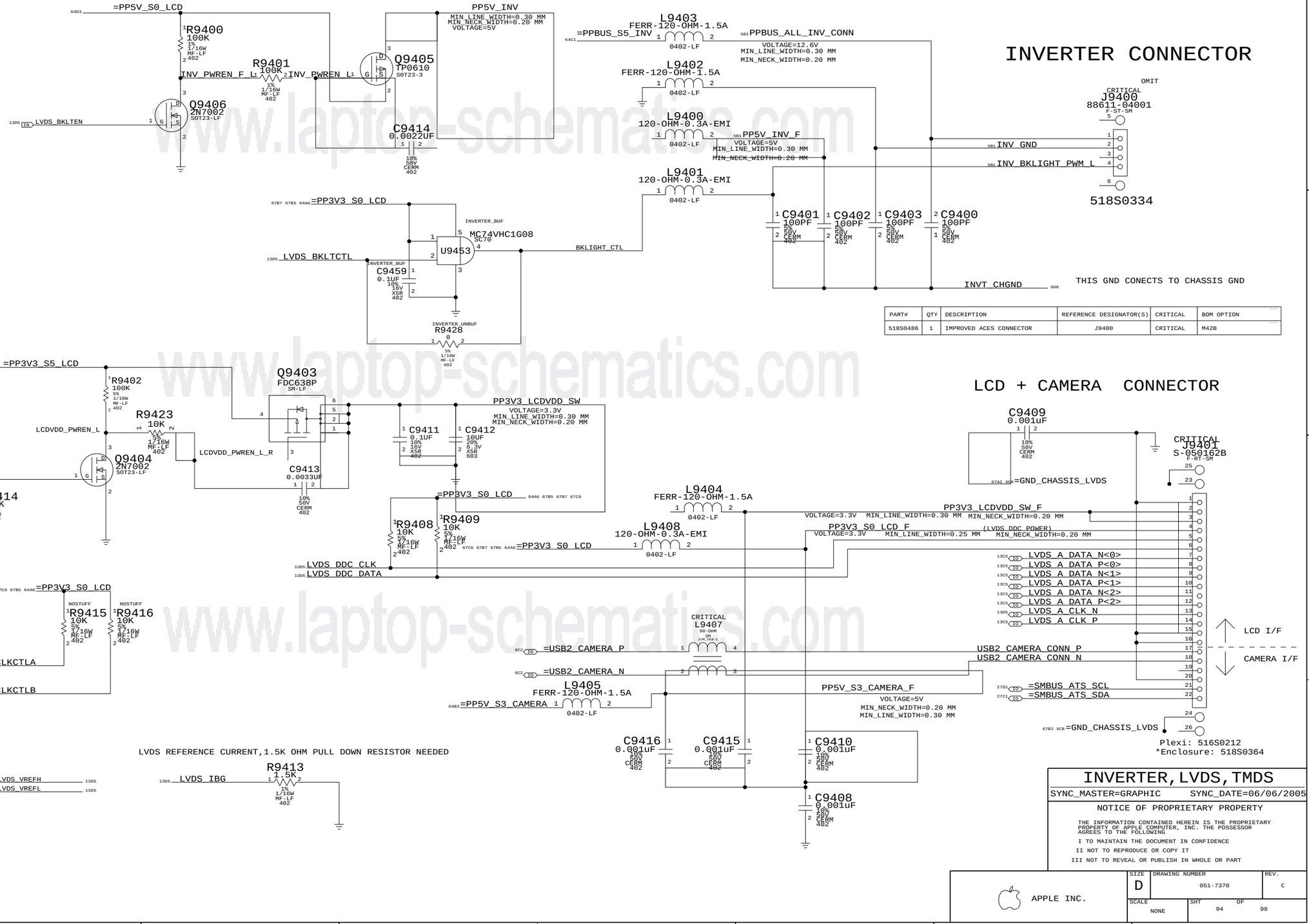
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 83 OF 98	



INVERTER CONNECTOR

LCD + CAMERA CONNECTOR

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
518S0486	1	IMPROVED ACES CONNECTOR	J9400	CRITICAL	M42B

INVERTER,LVDS,TMDS

SYNC_MASTER=GRAPHIC SYNC_DATE=06/06/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 94 OF 98	

L9506 120-OHM-0.3A-EMI
=PP3V3_S0_TMDS → 0402-LF → PP3V3_S0_ANALOG_TMDS_F (68B1 68B4)
VOLTAGE=3.3V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
C9536 0.001UF 10% 50V CERM 402
C9537 0.001UF 10% 50V CERM 402
C9538 0.1UF 10% 16V X5R 402
C9539 0.1UF 10% 16V X5R 402
C9540 10UF 20% 6.3V X5R 603
ONE 0.1UF AND 0.001UF FOR EACH PIN

L9501 120-OHM-0.3A-EMI
=PP1V8_S0_TMDS (68D6 64B6) → 0402-LF → PP1V8_S0_TMDS_F (68B4)
VOLTAGE=1.8V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
C9507 0.1UF 10% 16V X5R 402
C9508 0.001UF 10% 50V CERM 402
C9509 0.1UF 10% 16V X5R 402
C9510 0.001UF 10% 50V CERM 402
C9511 0.1UF 10% 16V X5R 402
C9512 0.001UF 10% 50V CERM 402
C9513 10UF 20% 6.3V X5R 603
ONE 0.1UF AND 0.001UF FOR EACH PIN

L9503 120-OHM-0.3A-EMI
=PP3V3_S0_TMDS → 0402-LF → PP3V3_S0_ANALOG_SDVO_F (68C4)
VOLTAGE=3.3V MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.25MM
C9530 0.001UF 10% 50V CERM 402
C9531 0.1UF 10% 16V X5R 402
C9514 0.1UF 10% 16V X5R 402

L9500 120-OHM-0.3A-EMI
=PP1V8_S0_TMDS (68D6 64B6) → 0402-LF → PP1V8_S0_ANALOG_SDVO_F (68C4)
VOLTAGE=1.8V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
C9500 0.001UF 10% 50V CERM 402
C9501 0.001UF 10% 50V CERM 402
C9502 0.1UF 10% 16V X5R 402
C9503 0.1UF 10% 16V X5R 402
C9504 10UF 20% 6.3V X5R 603
ONE 0.1UF AND 0.001UF FOR EACH PIN

L9504 120-OHM-0.3A-EMI
=PP3V3_S0_TMDS → 0402-LF → PP3V3_S0_PVCC1_TMDS_F (68C4)
VOLTAGE=3.3V MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.25MM
C9532 0.001UF 10% 50V CERM 402
C9533 0.1UF 10% 16V X5R 402
C9506 0.1UF 10% 16V X5R 402

L9505 120-OHM-0.3A-EMI
=PP3V3_S0_TMDS → 0402-LF → PP3V3_S0_PVCC2_TMDS_F (68C4)
VOLTAGE=3.3V MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.25MM
C9534 0.001UF 10% 50V CERM 402
C9535 0.1UF 10% 16V X5R 402

R9507 49.9 1% 1/16W MF-LF 402 — TMDS_TX_P<0> → TMDS_TX<0> → TMDS_TX_N<0>
R9508 49.9 1% 1/16W MF-LF 402 — TMDS_TX_P<1> → TMDS_TX<1> → TMDS_TX_N<1>
R9509 49.9 1% 1/16W MF-LF 402 — TMDS_TX_P<2> → TMDS_TX<2> → TMDS_TX_N<2>
R9510 49.9 1% 1/16W MF-LF 402 — TMDS_TX_CLK_P → TMDS_TX_CLK → TMDS_TX_CLK_N
C9522 0.001UF 10% 50V CERM 402
C9523 0.001UF 10% 50V CERM 402
C9524 0.001UF 10% 50V CERM 402
C9525 0.001UF 10% 50V CERM 402
R9538 49.9 1% 1/16W MF-LF 402
R9539 49.9 1% 1/16W MF-LF 402
R9540 49.9 1% 1/16W MF-LF 402
C9526 10pF 5% 50V CERM 402 NOSTUFF
C9527 10pF 5% 50V CERM 402 NOSTUFF

C9526,C9527 close to CHIP

MCH SDVO CHANNEL R,G,B,CLK SIGNAL TO TMDS CHIP
PLACE THE CAP NEAR THE NB SIDE

PEG_R2D_C_P<0> (13B3)
PEG_R2D_C_N<0> (13C3)
PEG_R2D_C_P<1> (13B3)
PEG_R2D_C_N<1> (13C3)
PEG_R2D_C_P<2> (13B3)
PEG_R2D_C_N<2> (13C3)
PEG_R2D_C_P<3> (13B3)
PEG_R2D_C_N<3> (13B3)

C9541 0.1UF 10% 16V X5R 402
C9542 0.1UF 10% 16V X5R 402
C9543 0.1UF 10% 16V X5R 402
C9544 0.1UF 10% 16V X5R 402
C9545 0.1UF 10% 16V X5R 402
C9546 0.1UF 10% 16V X5R 402
C9547 0.1UF 10% 16V X5R 402
C9548 0.1UF 10% 16V X5R 402

PP3V3_S0_ANALOG_SDVO_F (68D6)
PP1V8_S0_ANALOG_SDVO_F (68D3)
PP3V3_S0_PVCC2_TMDS_F (68C7)
PP3V3_S0_PVCC1_TMDS_F (68C6)
PP3V3_S0_ANALOG_TMDS_F (68D6 68B1)
PP1V8_S0_TMDS_F (68D3)

U9500 CRITICAL SIL1362ACLU LQFP

VCC0	10	TMDS_SDR_P	37 SDR_P
VCC1	28	TMDS_SDR_N	38 SDR_N
VCC2	34	TMDS_SDG_P	40 SDG_P
AVCC0	15	TMDS_SDG_N	41 SDG_N
AVCC1	21	TMDS_SDB_P	43 SDB_P
PVCC1	11	TMDS_SDB_N	44 SDB_N
PVCC2	26	TMDS_SDC_P	46 SDC_P
SVCC0	36	TMDS_SDC_N	47 SDC_N
SVCC1	42	TMDS_INT_P	32 SDI_P
SPVCC	48	TMDS_INT_N	33 SDI_N
OVCC	1	TMDS_EXT_RES	35 EXT_RES
			2 RESET*
			5 SDSCL
			4 SDSDA
			6 A1
			29 HTPLG
			30 TEST
GND0	7		
GND1	31		
AGND0	12		
AGND1	18		
AGND2	24		
PGND2	27		
SGND0	39		
SGND1	45		
SPGND	3		

SDVO RCVR CORE
DIFF SIG DATA
I2C MASTER INTER
CONFIG/ PRGRM
TEXT MODE

TX0_P	17	TMDS_TX_P<0> (69B2 68D3) OUT
TX0_N	16	TMDS_TX_N<0> (69B2 68D1) OUT
TX1_P	20	TMDS_TX_P<1> (69B2 68D3) OUT
TX1_N	19	TMDS_TX_N<1> (69B2 68D1) OUT
TX2_P	23	TMDS_TX_P<2> (69B2 68C3) OUT
TX2_N	22	TMDS_TX_N<2> (69B2 68C1) OUT
TXC_P	14	TMDS_TX_CLK_P (69A2 68C3) OUT
TXC_N	13	TMDS_TX_CLK_N (69A2 68C1) OUT
EXT_SWING	25	TMDS_EXT_SWING
SCLDDC	8	TMDS_I2C_SCL
SDADDC	9	TMDS_I2C_SDA

=PP3V3_S0_TMDS (64A6 68B1 68C8 68D8 69B7 69D1 69D5)
C9521 0.1UF 10% 16V X5R 402
C9505 10UF 20% 6.3V X5R 603

PP3V3_S0_ANALOG_TMDS_F (68B4 68D6)
R9504 249 1% 1/16W MF-LF 402
=PP3V3_S0_TMDS (64A6 68B2 68C8 68D8 69B7 69D1 69D5)
R9505 10K 5% 1/16W MF-LF 402
R9506 10K 5% 1/16W MF-LF 402

TMDS_I2C_SCL AND TMDS_I2C_SDA DON'T NEED TO CONNECT

PLACE IT CLOSE TO CONNECTOR
=PP5V_S0_TMDS (69C6 64D3)
D9500 BAV99DW-X-F SOT-363
=PP2V5_S0_TMDS (64B6)
R9501 3.3K 5% 1/16W MF-LF 402
R9502 3.3K 5% 1/16W MF-LF 402
C9519 0.1UF 10% 16V X5R 402
C9520 0.1UF 10% 16V X5R 402
PEG_D2R_P<1> (13C3) OUT → TMDS_INT_P
PEG_D2R_N<1> (13D3) OUT → TMDS_INT_N
TMDS CHIP SDVO INPUT INTERRUPT SIGNAL TO MCH
TMDS_RST_L (26B1)
SDVO_CTRLCLK (14B6) TO
SDVO_CTRLDATA (14B6) TO
R9500 2.2K 5% 1/16W MF-LF 402
TMDS_HTPLG (69C6) IN → TMDS_HTPLG_R
R9503 1K 5% 1/16W MF-LF 402
ADDRESS=0X70 NC IF HIGH, ADDRESS=0X72

NC
D9500 BAV99DW-X-F SOT-363
PP5V_S0_DVIPORT (69B4 69C3)
PP5V_S0_DVIPORT_D (69C5)

EXTERNAL TMDS

SYNC_MASTER=GRAPHIC SYNC_DATE=06/06/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 95 OF 98	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0227	155S0164	?	L9805, L9806, L9807	KEEP MAG.LAYER IN BOM

Video Connectors

EXTERNAL VIDEO (VGA) INTERFACE

Isolation required for DVI power switch

=PP3V3_S0_TMDS 64A6 68B1 68B2 68C8 68D8 69B7 69D1

Q9801 2N7002DW-X-F SOT-363

R9821 2.2K 5% 1/16W MF-LF 402

R9822 2.2K 5% 1/16W MF-LF 402

GPU_CRT_DDC_CLK 69B6

GPU_CRT_DDC_DATA 69B6

13B5 CRT_DDC_CLK

13B5 CRT_DDC_DATA

TMDS(MINI DVI) INTERFACE

=PP5V_S0_TMDS 68B7 64D3

F9804 0.5AMP-13.2V SM-LF

VOLTAGE=5V MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM

PP5V_S0_TMDS_FUSE

L9844 400-OHM-EMI SM-1

VOLTAGE=5V MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM

PP5V_S0_DVIPORT 68A6 69B4

C9804 0.1UF 20% 16V CERM 402

=GND_CHASSIS_TMDS_UPPER 6C8 69A4

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR CONNECTOR

=PP3V3_S0_TMDS 64A6 68B1 68B2 68C8 68D8 69B7 69D5

C9860 0.1UF 20% 16V CERM 402

13B5 CRT_HSYNC_R

R9860 39 5% 1/16W MF-LF 402

CRT_HSYNC_LS_R

U9804 SN74LVC2G125DCU

CRT_HSYNC_LS

R9870 39 5% 1/16W MF-LF 402

VGA_HSYNC 69B4

NOSTUFF C9842 33PF 50V CERM 402

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR THE CONNECTOR

13B5 CRT_VSYNC_R

R9861 39 5% 1/16W MF-LF 402

CRT_VSYNC_LS_R

U9804 SN74LVC2G125DCU

CRT_VSYNC_LS

R9871 39 5% 1/16W MF-LF 402

VGA_VSYNC 69B4

NOSTUFF C9843 33PF 50V CERM 402

A 255 OHM 1% RESISTOR IS REQUIRED BETWEEN CRT_IREF AND GROUND

13B5 CRT_IREF

R9869 255 1% 1/16W MF-LF 402

TV REFERENCE CURRENT,USES AN EXTERNAL RESISTOR OF 5K OHM 1% TO SET INTERNAL VOLTAGE LEVELS

13C5 TV_IREF

R9868 4.99K 1% 1/16W MF-LF 402

PP5V_S0_DVIPORT_D 68A8

DVI power DIODE on page 95 (D9500)

R9862 2.2K 5% 1/16W MF-LF 402

R9863 2.2K 5% 1/16W MF-LF 402

68A7 TMDS_HTPLG

C9808 0.001uF 10% 50V CERM 402

69D5 GPU_CRT_DDC_CLK

C9809 100pF 5% 50V CERM 402

69D5 GPU_CRT_DDC_DATA

C9812 100pF 5% 50V CERM 402

OMIT CRITICAL

J9801 MINI-DVI RT-TH

PP5V_S0_DVIPORT 68A6 69C3

TMDS_TX_CONN_P<2>

TMDS_TX_CONN_N<2>

TMDS_TX_CONN_P<1>

TMDS_TX_CONN_N<1>

TMDS_TX_CONN_P<0>

TMDS_TX_CONN_N<0>

TMDS_TX_CONN_CLK_P

TMDS_TX_CONN_CLK_N

NC

CRITICAL L9805 90-OHM-300MA 2012H

TMDS_TX_P<2> 68B2 68C3

TMDS_TX_N<2> 68B2 68C1

CRITICAL L9807 90-OHM-300MA 2012H

TMDS_TX_P<1> 68B2 68D3

TMDS_TX_N<1> 68B2 68D1

CRITICAL L9806 90-OHM-300MA 2012H

TMDS_TX_P<0> 68B2 68D3

TMDS_TX_N<0> 68B2 68D1

CRITICAL L9804 370-OHM-280MA SM1

TMDS_TX_CLK_P 68B2 68C3

TMDS_TX_CLK_N 68B2 68C1

PLACE THE RESISTOR CLOSE TO GMCH

13C5 TV_DACA_OUT

13B5 CRT_BLUE

R9850 75 1% 1/16W MF-LF 402

R9851 75 1% 1/16W MF-LF 402

13C5 TV_IRTNA

13B5 CRT_BLUE_L

68B2 68B1 69D5 64A6 68D1 68D8 68C8 =PP3V3_S0_TMDS

C9839 0.1UF 10% 16V X5R 402

EXT_COMPVID_B

FL9800 LCFILTER SM-220MHZ-LF

NOSTUFF R9856 150 1% 1/16W MF-LF 402

VGA_B 69C1

C9824 3.3PF 0.25% 50V CERM 402

CRITICAL U9801 TS3V330 SOP

VCC 16

S1A 2 S2A 3 S1B 5 S2B 6 S1C 11 S2C 10 S1D 14 S2D 13

DA 4 DB 7 DC 9 DD 12

IN 1 EN_L 15

GND 8

EXT_Y_G

FL9801 LCFILTER SM-220MHZ-LF

NOSTUFF R9864 150 1% 1/16W MF-LF 402

VGA_G 69C1

VGA_VSYNC 69C1

C9834 3.3PF 0.25% 50V CERM 402

VGA_R

PLACE THE RESISTOR CLOSE TO GMCH

13C5 TV_DACB_OUT

13B5 CRT_GREEN

R9852 75 1% 1/16W MF-LF 402

R9853 75 1% 1/16W MF-LF 402

13C5 TV_IRTNB

13B5 CRT_GREEN_L

EXT_C_R

FL9802 LCFILTER SM-220MHZ-LF

NOSTUFF R9859 150 1% 1/16W MF-LF 402

6C8 =GND_CHASSIS_TMDS_UPPER 69C3

6A6 =GND_CHASSIS_TMDS_DOWN

C9820 3.3PF 0.25% 50V CERM 402

NOSTUFF C9821 0.1UF 10% 16V X5R 402

PLACE THE RESISTOR CLOSE TO GMCH

13C5 TV_DACC_OUT

13B5 CRT_RED

R9854 75 1% 1/16W MF-LF 402

R9855 75 1% 1/16W MF-LF 402

13C5 TV_IRTNC

13B5 CRT_RED_L

=SB_GPIO22 6B2

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0292	1	CONN,32P MINI-DVI RCPT,RA,MG3,LF	J9801	CRITICAL	NORMAL
514-0319	1	CONN,32P MINI-DVI RCPT,RA,BLACK,LF	J9801	CRITICAL	FANCY

MINI-DVI CONNECTOR

SYNC_MASTER=EUGENE SYNC_DATE=05/21/05

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 98 OF 98	