1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,MLB,MBP17

10/24/2007

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
B		541479	PRODUCTION RELEASED	10/25/07	

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7520	1	SCHEM,MLB,MBP17	SCH	CRITICAL	
820-2132	1	PCBF,MLB,MBP17	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Wed Oct 24 17:05:14 2007

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

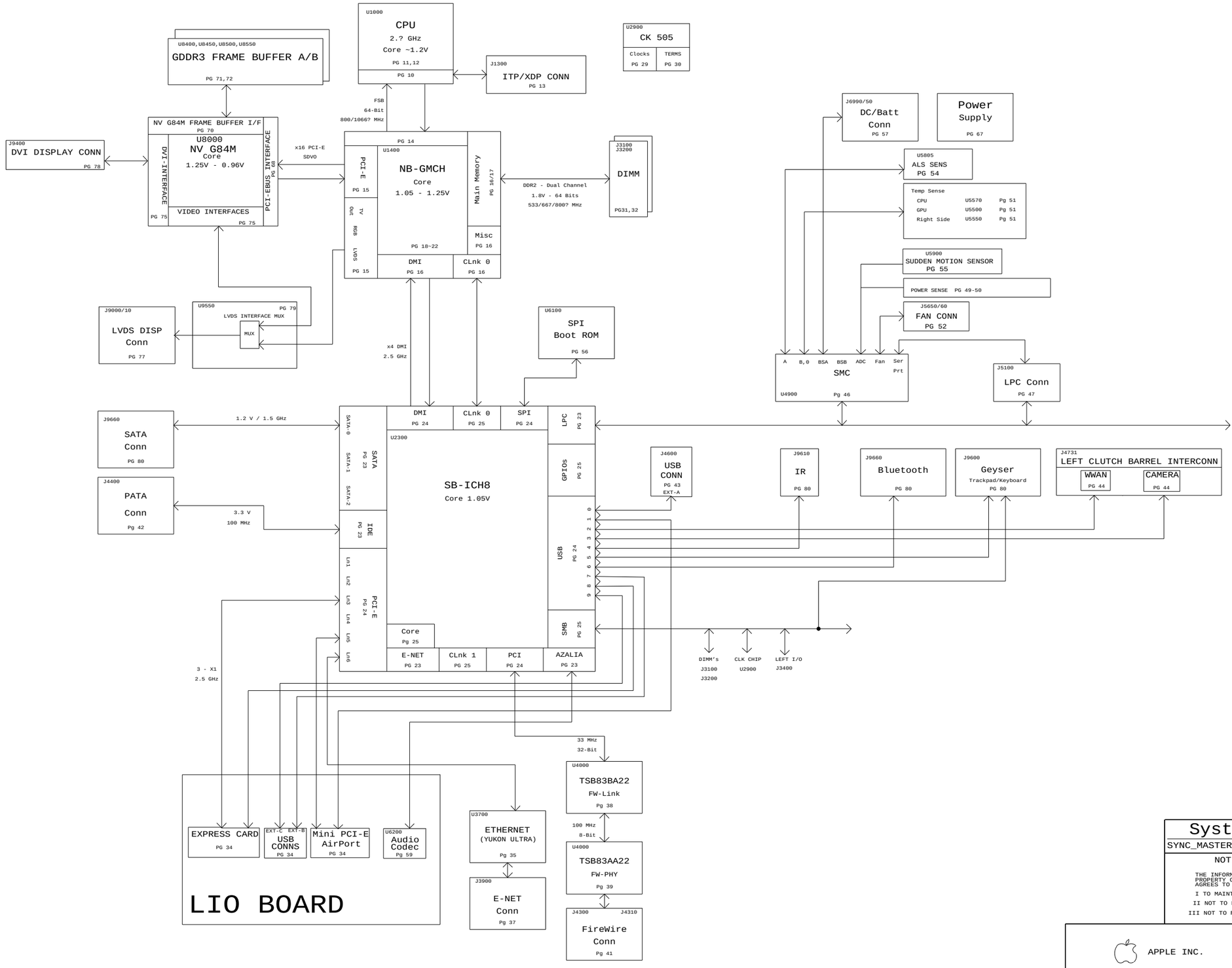
SIZE D

APPLE INC.

TITLE
SCHEM,MLB,MBP17

DRAWING NUMBER 051-7520 REV. B

SHT 1 OF 109



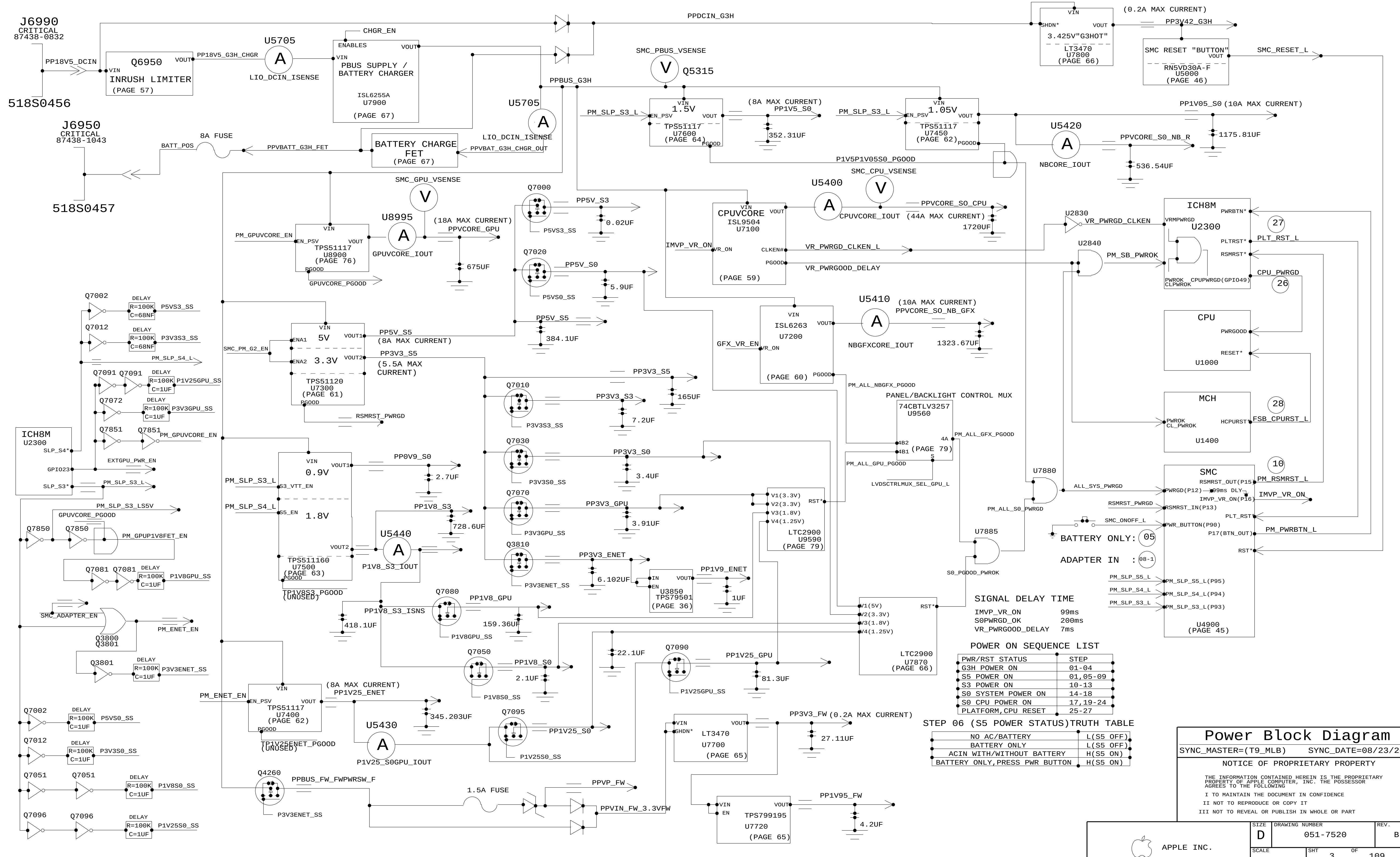
System Block Diagram

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/23/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 2 OF 109	

M76 POWER SYSTEM ARCHITECTURE



SIGNAL DELAY TIME

IMVP_VR_ON	99ms
S0PWRGD_OK	200ms
VR_PWRGOOD_DELAY	7ms

POWER ON SEQUENCE LIST

PWR/RST STATUS	STEP
G3H POWER ON	01-04
S5 POWER ON	01,05-09
S3 POWER ON	10-13
S0 SYSTEM POWER ON	14-18
S0 CPU POWER ON	17,19-24
PLATFORM,CPU RESET	25-27

STEP 06 (S5 POWER STATUS)TRUTH TABLE

NO AC/BATTERY	L(S5 OFF)
BATTERY ONLY	L(S5 OFF)
ACIN WITH/WITHOUT BATTERY	H(S5 ON)
BATTERY ONLY,PRESS PWR BUTTON	H(S5 ON)

Power Block Diagram

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/23/2006

APPLE INC.

SIZE D | DRAWING NUMBER 051-7520 | REV. B | SCALE NONE | SHT 3 OF 109

Power Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE	SHT	OF
NONE	4	109

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9174	PCBA,G0,2.4GHZ,BTR,VRAM-SAM,MBP17	M76_COMMON,CPU_2_4GHZ,FB_256_SAMSUNG,INV_BYPASS,EEE_ZF7
630-9173	PCBA,G0,2.4GHZ,BTR,VRAM-HY,MBP17	M76_COMMON,CPU_2_4GHZ,FB_256_HYNIX,INV_BYPASS,EEE_ZF6
630-9177	PCBA,G0,2.6GHZ,CTO,VRAM-SAM,MBP17	M76_COMMON,CPU_2_6GHZ,FB_256_SAMSUNG,INV_BYPASS,EEE_ZFA
630-9178	PCBA,G0,2.6GHZ,CTO,VRAM-HY,MBP17	M76_COMMON,CPU_2_6GHZ,FB_256_HYNIX,INV_BYPASS,EEE_ZFB

M76 BOM Groups

BOM GROUP	BOM OPTIONS
M76_COMMON	COMMON,ALTERNATE,M76_COMMON1,M76_COMMON2,M76_DEBUG,M76_PROGPARTS,ISL6257H
M76_COMMON1	EXTGPU_RST_HW,ISL9504B,LVDS_SEL_RESUME,ONEWIRE_PU,CPU_NTC_A,GPU_XW1
M76_COMMON2	P1V8S3_1V825_GPUFB,SLG2AP101,SMS_MOT_DIS,YUKON_ULTRA,VGA_TERM_CONN
M76_CTO	INV_SPLIT,INV_17INCH
M76_DEBUG	SMC_DEBUG_NO,XDP,LPCPLUS
M76_PROGPARTS	BOOTROM_PROG,SMC_PROG

BOM GROUP	BOM OPTIONS
FB_256_SAMSUNG	VRAM_256,VRAM_SAMSUNG,VRAM_256_SAMSUNG
FB_256_HYNIX	VRAM_256,VRAM_HYNIX,VRAM_256_HYNIX

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZF6]	CRITICAL	EEE_ZF6
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZF7]	CRITICAL	EEE_ZF7
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZFA]	CRITICAL	EEE_ZFA
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZFB]	CRITICAL	EEE_ZFB

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0388	1	IC,GPU,NV G84M,BGA	U8000	CRITICAL	
338S0432	1	IC,NB,CRESTLINE,GM,C0,PRQ,ROHS-SPECIAL,965PM	U1400	CRITICAL	
338S0434	1	IC,SB,ICH8M,B1,PRQ,BGA	U2300	CRITICAL	
353S1461	1	IC,ISL9504,SYNC REG CTRL,2PHAS,QFN48,LF	U7100	CRITICAL	ISL9504A
353S1651	1	IC,ISL9504B,2PH IMVP6 REG,PMON,QFN48	U7100	CRITICAL	ISL9504B

359S0127	1	IC,68 PIN,CK505,LOW POWER CLOCK GENER	U2900	CRITICAL	SLG8LP537
359S0130	1	IC,SLG2AP101,LW PWR CLK GEN,CK505,QFN68	U2900	CRITICAL	SLG2AP101
338S0386	1	IC,88E8058,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	
338S0274	1	IC,SMC,HS8/2116	U4900	CRITICAL	SMC_BLANK
341S2258	1	IC,SMC,V1.18F4,M76A	U4900	CRITICAL	SMC_PROG
335S0384	1	IC,16MBIT 8-PIN SPI SERIAL FLASH,SOIC8	U6100	CRITICAL	BOOTROM_BLANK
341S2243	1	IC,EFI ROM,DEVELOPMENT,M75A/M76A	U6100	CRITICAL	BOOTROM_PROG

333S0382	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_SAMSUNG
333S0401	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_HYNIX
337S3503	1	IC,MDC,SR,G0,PRQ,2.4G,35W,800FSB,4M,BGA	U1000	CRITICAL	CPU_2_4GHZ
337S3527	1	IC,MDC,SR,G0,PRQ,2.6G,35W,800FSB,4M,BGA	U1000	CRITICAL	CPU_2_6GHZ

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0011	157S0030		ALL	E&E alt to TDK/BiTech magnetics
152S0476	152S0276		ALL	Inductor alternate
138S0603	138S0602		ALL	Murata alt to Samsung 22uF acoustic caps
353S1681	353S1294		ALL	TI alternate to National
376S0543	376S0466		ALL	AOS alternate to Siliconix Si4413
376S0526	376S0451		ALL	Fairchild FDW6530P alternate to IRF7707

BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 5 OF 109	

DVT

13.1.0:
3/05/07 -- Integrated m75/mlb pages 22,25,28,30-32,50,53-55,72,74,76,78,80-82,84-90,94,95 through:
Change 46833 by cerickso@m75_mlb_051-7225_12.5.0_tmp.Ecad on 2007/03/02 09:49:13
Changes since previous major release (12.3.0):
- LVDS Connector: Changed pin 5 of connector from NC to PP3V3_SW_LCD (in case we add extra cable for power - rdar://5024882)
- NB GFX Decoupling: Added R2260 (0.3 ohm, 0603) to bring ESR of regulator output cap in spec (rdar://5000272)
Changes since previous major release (12.2.0):
- Left Clutch IC: Updated both I-PEX connectors to new APN (part update for shell plating)
- NB GFX Core: Changed Vcore controller to ISL6263B (part consolidation effort between Apple/Intersil - rdar://5009109)
- Power Supplies: Replaced APN 152S0511 with 152S0368 (duplicate APNs for same part - rdar://5009109)
- Thermal Sensors: Updated topology of EMC1033 sensors (removed shorts, changed connector caps to 18pF)
- NB GFX Decoupling/Power Aliases: Connected VCCD_CRT of NB to GND per CRT disable guidelines
Changes since previous bom release (12.0.0):
- GPU FB: Changed cal resistors per NVidia PUN (R8290 to 45.3 ohm and R8291 to 24.9 ohm)
- GPU FB: Changed unterminated-mode reference voltage to 40% (R8297 -> 1.02k, R8432/82, R8532/82 -> 2.21K)
- Power Sequencing: Removed U7885/C7885 to take GFX_PGOOD out of PWR_OK chain (rdar://4974927)
- GPU Vcore: NO STUFFed all PWRCTL related components (feature not to be supported)
- GPU Vcore: Updated voltage setpoints to 1.000/1.070/1.125V
- SB GPIOs: Sync'd page25.csa to T9_MLB to get pullup updates
- Thermal Sensors: Updated topology of EMC1033 filter caps (added C5515 next to IC, moved other caps to connectors)
3/5/07 -- Added GPU Vcore VFB resistor BOM table and GCORE_M76 BOM Option to M76_COMMON BOM group.
3/5/07 -- Removed RX3920-RX3927.
3/5/07 -- FireWire: Changed to Rev C of TI FireWire MCM (APN: 338S0435)
3/5/07 -- ODD Conn: Changed ODD power FET to FDC606P (from FDC638P) for reduced Rds(on)
3/5/07 -- Changed 1.8V supply feedback resistors R7520 to 21.5K 0.1% and R7521 15.0K 0.1%.%
13.2.0
3/07/07 -- Integrated m75/mlb pages 25,42,70 through:
Change 47192 by cerickso@m75_mlb_051-7225_12.7.0_tmp.Ecad on 2007/03/06 18:36:54
Changes since previous major release (12.6.0):
- FireWire Ports: Changed D4260 to PDS540 for higher current capacity
- SB GPIOs: Changed R2514 from pulldown to pulldown to correct auto power-on issue (Linda card detect GPIO)
3/07/07 -- Q7080 PP1V8_GPU FET changed for lower Rds on from FDM6296 to RJK0301DPB
13.3.0
3/08/07 -- Removed =PP1V5_S0_NB_VCCD_CRT alias to PP1V5_S0 since VCCD_CRT is GNDed per CRT disable guidelines.
3/08/07 -- Battery charge current limit circuit changes.
3/08/07 -- Changed R9811 from 15.0K to 14.0K. This is so that M57 inverter and split inverter can use same backlight table.
3/08/07 -- Changed R9950 from 220K to NOSTUFF to improve current and voltage asymmetry ratio.
3/08/07 -- Changed BOM option on R9960 511K from NOSTUFF to INV_SPLIT to improve current and voltage asymmetry ratio.
3/08/07 -- Integrated CSA pg. 55 through:
Change 47450 by cerickso@m75_mlb_051-7225_12.8.0_tmp.Ecad on 2007/03/08 10:49:26
Changes since previous major release (12.7.0):
- Thermal Sensors: Added R5515/R5516 in case low pass filter is needed for EMC1033
3/08/07 -- Integrated CSA pg. 79 through:
Change 47440 by xyang@m75_lio_051-7226_7.9.0_tmp.Ecad on 2007/03/08 10:25:46
Changed Charger PWM limit resistor according to MARC K.'S M70 values
13.4.0
3/12/07 -- Added BOM option P1V8S3_1V825 to M76_COMMON2 BOM group.
3/12/07 -- Modified R7520 and R7521 to use symbols for 0.1% resistors.
Removed OMIT BOM option from R7521.
Changed BOM options for R7520 to choose between 1.8V or 1.825V 0.1% resistors.
14.0.0
3/14/07 -- Removed BOM option for HDCP as feature is removed.
3/14/07 -- Moved =PP1V8_GPU_P1V8GPUFET from PP1V8_S3_ISNS to PP1V8_S3. This is to remove the current sense resistor from the GPU 1.8V path.
Cleaned up unused aliases.
3/14/07 -- Constraints: Constrained WWAN_SIM signals to 50 ohms
3/14/07 -- Integrated m75/mlb CSA pages 55 & 78 through:
Change 48122 by cerickso@cerickso_m75.Ecad on 2007/03/14 15:27:36
- Thermal Sensors/Aliases: Changed mounting pads of Th2H sensor connector to left clutch chassis gnd
- Power Control: Corrected alias connections for 5V/3V3 S5 enable signals
14.1.0
3/14/07 -- Moved =PP1V8_S0_P1V8S0FET from PP1V8_S3_ISNS to PP1V8_S3.
14.2.0
3/15/07 -- Changes to low voltage inverter for M76 piezo.
14.5.0
3/19/07 --
Integrated m75/mlb CSA pgs. 28,30-32,50,53-55,80-82,84-88,90,94,95 through:
Change 48405 by cerickso@m75_mlb_051-7225_13.3.0_tmp.Ecad on 2007/03/16 12:18:46
Changes since previous major release (13.2.0):
- Thermal Sensors: Moved remote sensor U5500 to SMC SMBus A and S3 power rail to clear I2C addr clash
3/19/07 --Integrated t9/mlb_noME CSA pgs. 15 & 38 through:
Change 48372 by wferry@wferry_projects.Ecad on 2007/03/16 09:11:01
Quick submit of T9 noME branch. Major release will follow once changes are properly documented in Radar and revision history.
Page 15: Sync from main-line (renamed LVDS_VREFx nets).
Page 38: Changed Yukon crystal load caps to 18pF per radar://4946795 (really radar://4945362).
3/19/07 -- Added OMIT BOM option to L4731 and L4741.
3/19/07 -- Added BOM table with 0 Ohm 0603 resistors at L4731,L4741.
3/19/07 -- SMBus: moved Remote Temps from SMC B to SMC A in order to use EMC1043-5.
3/19/07 --
<rdar://problem/5070179> BOM update: boost circuit open causes MLB & SIMM damage (see 5064997)
Deleted R7364 and made C7364 0603 size, still 0.1uF (132S0100).
Deleted R7420 and R7470 and made C7420 and C7470 0603 size, still 0.1uF (132S0100).
Deleted R7525 and made C7525 0805 size, still 0.1uF (132S0201).
Deleted R7615 and made C7615 0603 size, still 0.1uF (132S0100).
Deleted R8915 and made C8915 0603 size, still 0.1uF (132S0100).
3/19/07 -- Changes to low voltage inverter for M76 piezo.
L9950 changed from 152S0527 (15uH, 2.8A, 115mOhm) to 152S0585 (22uH, 2.8A, 129mOhm).
14.6.0
3/19/07 -- Integrated m75/mlb CSA pgs. 55 & 78 through:
Change 48590 by cerickso@m75_mlb_051-7225_13.4.0_tmp.Ecad on 2007/03/19 14:26:14
Changes since previous major release (13.3.0):
- Thermal Sensors: Updated U5500 power alias to indicate device should be on S3 rail
- Power Control: Added U7858 to level shift PM_G2_EN to 3.42V to 5V
3/19/07 -- Updated SMC A SMBus information for Left I/O Board and Top-Case.
3/19/07 -- Deleted R7324 and made C7324 0603 size, still 0.1uF (132S0100).
14.7.0
3/19/07 -- Added three 0603 0 ohm resistors R4740-R4742 for EMC return current path.
3/19/07 -- Battery charge current limit circuit changes for max charge current of 4.5A.
3/19/07 -- Integrated m75/mlb CSA pgs. 22 & 78 through:
Change 48660 by cerickso@m75_mlb_051-7225_13.5.0_tmp.Ecad on 2007/03/19 20:17:1 Changes since previous major release (13.4.0):
- Power Control: Tied all 4 5V/3.3V enables (EN1, EN2, EN3 and EN5) together as part of PM_G2_EN
14.8.0
3/21/07 -- Integrated m75/mlb CSA pgs. 84,85 & 89 through:
Change 48885 by cerickso@m75_mlb_051-7225_14.0.0_tmp.Ecad on 2007/03/20 21:27:14
This fab release is for DVT!
Changes since previous major release (13.5.0):
- GPU Vcore: Updated setpoints for GPU Vcore based upon Nvidia Vmin (i.e. 1.05V, 1.05V, 1.05V, 1.125V)
- FB: Changed FB VREF caps to 2x0.0047uF as required by Nvidia PUN 02736-001-v07 (which requests 1x0.01uF)
3/21/07 -- <rdar://problem/4838347> EMC - M76 MLB changes
Change BOM option on L4764 to OMIT and added BOM table entry for 0 ohm resistor at L4764.
3/21/07 -- <rdar://problem/5073301> M76: Change GPU Vmin
Changed resistors for M76 Vcore setpoints (i.e. 1.05V, 1.05V, 1.125V, 1.25V)
Removed NOSTUFF BOM option from R8924.
Changed R8924 to 28K.
Changed R8925 to 16.9K.
Changed table text notes.
3/22/07 -- Items relating to <rdar://problem/5061583> Task: Current Surge When Insert Battery Without AC Plugged-In
3/22/07 -- Added D7903 for voltage ripple on ISL6257 BOOT and PHASE pins.
3/22/07 -- Added Q7970 for potential battery inrush current.
15.0.0
3/26/07 -- Removed C7930 and R7903 for space reasons.
15.2.0
3/28/07 -- Change BOM option for 1.8V regulator feedback to 1.8V GPU FET input.
3/28/07 -- Added XW7580 and R7580 for option to tie 1.8V S3 regulator feedback point to input of 1.8V GPU FET.
3/28/07 -- Integrated m75/mlb CSA pg. 87 through
Change 49919 by cerickso@cerickso_m75.Ecad on 2007/03/28 14:28:29
Changes since previous fab release (14.0.0):
- GPU Straps: Added PCI_DEVID<3..0> pullup straps
15.3.0
3/29/07-- Moved XW7580 to XW0980, and R7580 to R0980.
15.4.0
3/31/97 -- Changed C9950 from 22uF to 10uF for acoustic noise per Flo Kim.
3/31/97 --Added C9951 B2 case size as placeholder for new cap for acoustic noise per Flo Kim.

B

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B

SCALE	SHT	OF
NONE	6	109

Functional Test Points

Fan Connectors

FUNC_TEST

I498	TRUE	=PP5V_S0_FAN_LT	8 52
I497	TRUE	FAN_LT_PWM	52
I496	TRUE	FAN_LT_TACH	52
I495	TRUE	FAN_RT_PWM	52
I494	TRUE	FAN_RT_TACH	52

LPC+ Debug Connector

FUNC_TEST

I490	TRUE	=PP3V3_S5_LPCPLUS	8 47
I491	TRUE	=PP5V_S0_LPCPLUS	8 47
I492	TRUE	LPC_AD<0>	23 45 47
I493	TRUE	LPC_AD<1>	23 45 47
I424	TRUE	LPC_FRAME_L	23 45 47
I423	TRUE	PM_CLKRUN_L	25 45 47
I422	TRUE	BOOT_LPC_SPI_L	24 47
I421	TRUE	SMC_TMS	45 46 47
I420	TRUE	DEBUG_RESET_L	28 47
I419	TRUE	SMC_TRST_L	45 47
I418	TRUE	SMC_TDO	45 46 47
I417	TRUE	SMC_MD1	45 47
I416	TRUE	SMC_TX_L	43 45 46 47
I415	TRUE	FWH_INIT_L	47
I414	TRUE	PCI_CLK33M_LPCPLUS	30 47 88
I413	TRUE	LPC_AD<2>	23 45 47
I412	TRUE	LPC_AD<3>	23 45 47
I411	TRUE	INT_SERIRQ	25 45 47
I410	TRUE	PM_SUS_STAT_L	25 45 46 47
I409	TRUE	SMC_TDI	45 46 47
I408	TRUE	SMC_TCK	45 46 47
I407	TRUE	SMC_RESET_L	45 46 47
I406	TRUE	SMC_NMI	45 47
I405	TRUE	SMC_RX_L	43 45 46 47
I403	TRUE	LINDACARD_GPIO	25 47

Left ALS

FUNC_TEST

I448	TRUE	ALS_GAIN	34 45 54
I447	TRUE	LTALS_OUT	34 54
	TRUE	GND	

Thermal Diode Connectors

FUNC_TEST

I568	TRUE	HSTHMSNS_D_P	51 91
I567	TRUE	HSTHMSNS_D_N	51
I443	TRUE	RSFSTHMSNS_D_P	51 91
I442	TRUE	RSFSTHMSNS_D_N	51
I520	TRUE	CPUTHMSNS_D2_P	51 91
I521	TRUE	CPUTHMSNS_D2_N	51

Battery Digital Connector

FUNC_TEST

I606	TRUE	SMC_BS_ALRT_L	45 46 57
I607	TRUE	=SMBUS_BATT_SCL	48 57
I608	TRUE	=SMBUS_BATT_SDA	48 57
I611	TRUE	=BATT_POS	57 67
I610	TRUE	=BATT_NEG	57 67
	TRUE	GND (HOST_DETECT_L)	

Left I/O Power Connector

FUNC_TEST

I620	TRUE	PP18V5_DCIN	57
I430	TRUE	=PPBUS_G3H_LIO_CONN	8 57
	TRUE	GND	

Request for 2 test points
Request for 3 test points

Request for at least 10 GND test points

NOTE: 10 additional GND test points are called out separately in these notes.

RTC Battery Connector

FUNC_TEST

I615	TRUE	PPVBATT_G3_RTC	28
	TRUE	GND	

Current Sense Calibration

FUNC_TEST

I431	TRUE	ISENSE_CAL_EN	45 49
I430	TRUE	=PP5V_S0_ISENSECAL	8 49
I429	TRUE	=PPVCORE_S0_NBGFX_REG	8 60
I427	TRUE	=PPVCORE_S0_CPU_REG	8 49 59
I426	TRUE	=PPVCORE_GPU_REG	8 49 76
	TRUE	GND	

2 TPs per

6 TPs, 2 with each of above TP pairs

Left Clutch Barrel Connector

FUNC_TEST

I616	TRUE	PP5V_S3_CAMERA_F	44
I617	TRUE	USB_CAMERA_F_N	44 91
I618	TRUE	USB_CAMERA_F_P	44 91
I619	TRUE	PP5V_S3_WWAN_F	44
I602	TRUE	USB_WWAN_F_N	44 91
I624	TRUE	USB_WWAN_F_P	44 91

Other Func Test Points

FUNC_TEST

I433	TRUE	PM_SYSRST_L	25 28 45
I432	TRUE	SMC_ONOFF_L	45 46 80

Inverter Connector

FUNC_TEST

I633	TRUE	PPBUS_S0_LCDBKLT_FUSED	82
I632	TRUE	=GND_CHASSIS_INVERTER	9 82
I630	TRUE	PP5V_SW_LCDBKLT	81 82
I631	TRUE	LCDBKLT_PWM	81 82
	TRUE	GND	

IR & Sleep LED Connector

FUNC_TEST

I639	TRUE	=PP5V_S3_IR	8 80
I640	TRUE	USB_IR_N	24 80 86
I642	TRUE	USB_IR_P	24 80 86
I641	TRUE	SYS_LED_ANODE	46 80
	TRUE	GND	

System Validation TPs

FUNC_TEST

	TRUE	CPU_PWRGD	10 13 23 83
	TRUE	CPU_DPSLP_L	7 10 23 83
	TRUE	PM_DPRSLPVR	16 25 59 83
	TRUE	CPU_DPSLP_L	7 10 23 83
	TRUE	PM_LAN_ENABLE	25 45
	TRUE	PCI_RST_L	24 28
	TRUE	PM_RSMRST_L	25 45
	TRUE	PM_SB_PWROK	9 25 28
	TRUE	SB_RTC_RST_L	23 28
	TRUE	PM_STPCPU_L	25 29 30
	TRUE	PM_STPPCI_L	25 29 30
	TRUE	VR_PWRGD_CLKEN	25 28
	TRUE	VR_PWRGOOD_DELAY	9 16 28 59
	TRUE	FSB_CPURST_L	10 13 14 83
	TRUE	FSB_CPUSLP_L	10 14 83
	TRUE	FSB_DPWR_L	10 14 83
	TRUE	NB_SB_SYNC_L	16 25
I561	TRUE	PM_BMBUSY_L	16 25

FUNC_TEST

	TRUE	IMVP_VR_ON	45 59
	TRUE	IMVP_DPRSLPVR	59 83
	TRUE	PM_SLP_S3_L	25 36 40 45 66
	TRUE	PM_S4_STATE_L	25 45 66
	TRUE	PM_SLP_S5_L	25 45 46
	TRUE	PM_ENET_EN	36 66
	TRUE	P1V5P1V05S0_PGOOD	66
	TRUE	CPU_DPRSTP_L	10 16 23 59 83
	TRUE	IMVP6_VID<6..0>	12 59 83
	TRUE	FSB_CLK_CPU_N	10 30 88
	TRUE	FSB_CLK_CPU_P	10 30 88
	TRUE	PLT_RST_L	9 24 28 79
	TRUE	NB_RESET_L	16 28
	TRUE	GPU_RESET_L	28 68
	TRUE	SMC_LRESET_L	28 45
	TRUE	CPU_STPCLK_L	10 23 83
	TRUE	FSB_CLK_NB_P	14 30 88
	TRUE	FSB_CLK_NB_N	14 30 88
	TRUE	NB_CLKREQ_L	16 29
	TRUE	NB_CLK100M_PCIE_P	16 30 88
	TRUE	NB_CLK100M_PCIE_N	16 30 88
	TRUE	NB_CLK96M_DOT_P	88
	TRUE	NB_CLK96M_DOT_N	88
	TRUE	NB_CLK100M_DPLLSS_P	22 30 88
	TRUE	NB_CLK100M_DPLLSS_N	22 30 88
	TRUE	CPU_THERMTRIP_R	23

ICT Test Points

CPU FSB NO_TESTs

MAKE BASE	NO_TEST			
I638	TRUE	FSB_A_L<31..3>		10 14 83
I557	TRUE	FSB_ADS_L		10 14 83
I556	TRUE	FSB_ADSTB_L<1..0>		10 14 83
I555	TRUE	FSB_BNR_L		10 14 83
I554	TRUE	FSB_BREQ0_L		10 14 83
I552	TRUE	FSB_D_L<63..0>		10 14 83
I553	TRUE	FSB_DBSY_L		10 14 83
I636	TRUE	FSB_DINV_L<3..0>		10 14 83
I551	TRUE	FSB_DRDY_L		10 14 83
I640	TRUE	FSB_DSTB_L_N<3..0>		10 14 83
I647	TRUE	FSB_DSTB_L_P<3..0>		10 14 83
I648	TRUE	FSB_HIT_L		10 14 83
I649	TRUE	FSB_HITM_L		10 14 83
I644	TRUE	FSB_LOCK_L		10 14 83
I634	TRUE	FSB_REQ_L<4..0>		10 14 83
I573	TRUE	TRUE NC_CPU_RSVD5	TP_CPU_RSVD5	10

NB NO_TESTs

MAKE BASE	NO_TEST			
I655	TRUE	TRUE NC_NB_NC<1..16>	TP_NB_NC<1..16>	16
I566	TRUE	TRUE NC_NB_RSVD<26..27>	TP_NB_RSVD<26..27>	16
I570	TRUE	TRUE NC_NB_RSVD<24>	TP_NB_RSVD<24>	16

GPU NO_TESTs

NO_TEST

I583	TRUE	LVDS_L_CLK_P	75 79 90
I582	TRUE	LVDS_L_DATA_P<0>	75 79 90
I564	TRUE	TP_GPU_MIOB_CLKIN	74
I565	TRUE	TP_GPU_MIOB_CLKOUT_P	74
I566	TRUE	TP_GPU_MIOB_CTL3	74
I576	TRUE	NC_GPUVCORE_VFB_PC0	76
I577	TRUE	NC_GPUVCORE_VFB_PC1	76

Functional / ICT Test

SYNC_MASTER=MASTER SYNC_DATE=MASTER

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B

SCALE: NONE SHT 7 OF 109

"G3Hot" (Always-Present) Rails

=PPVBAT_G3H_CHGR_REG → PPBUS_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
- =PPBUS_S5_FWPWRSW
- =PPBUS_S5_P1V8GPUFET
- =PPVIN_S5_CPU_IMVP_VIN
- =PPVIN_S5_CPU_IMVP
- =PPVIN_S5_P5VP3V3
- =PPVIN_S5_P5VS5
- =PPVIN_S5_P3V3S5
- =PPVIN_ENET_P1V25ENET
- =PPVIN_S3_P1V8S3
- =PPVIN_S0_P1V5S0
- =PPBUS_S0_LCDBKLT
- =PPVIN_S0_GFXIMVP6
- =PPVIN_S0_P1V05S0
- =PPVIN_GPU_GPUVCORE
- =PPBUS_G3H_LIO_CONN
- =PPBUS_S5_P1V25S0FET

=PPDCIN_G3H → PPDCIN_G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V
MAKE_BASE=TRUE
- =PPVIN_G3H_P3V42G3H
- =PPVBATT_G3H_LIO_CONN

=PP3V42_G3H_REG → PP3V42_G3H
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.42V
MAKE_BASE=TRUE
- =PP3V42_G3H_SB_RTC
- =PP3V42_G3H_ACIN
- =PP3V42_G3H_SMCUSBMUX
- =PP3V42_G3H_SMBUS_SMC_BSA
- =PP3V42_G3H_LIDSWITCH
- =PP3V3_S5_SMC
- =PP3V3_S5_LPCPLUS
- =PPVIN_S5_SMCVREF
- =PP3V42_G3H_PWRCTL

5V Rails

=PP5V_S5_REG → PP5V_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S5_SB
- =PP5V_S5_P1V8GPUFET
- =PP5V_S5_P1V8S0FET
- =PP5V_S5_P1V25GPUFET
- =PP5V_S5_P1V25S0FET
- =PP5V_S5_P1V25ENET
- =PP5V_S5_P1V05S0
- =PP5V_S5_P1V8DDRREG
- =PP5V_S5_P1V5S0
- =PP5V_S5_PWRCTL
- =PP5V_S5_GPUVCORE
- =PP5V_S3_RTUSB
- =PP5V_S3_P5VS3FET
- =PP5V_S0_P5VS0FET
- =PP5V_S0_ODD

=PP5V_S3_FET → PP5V_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S3_SYSLED
- =PP5V_S3_CAMERA
- =PP5V_S3_WWAN
- =PP5V_S3_IR
- =PP5V_S3_TOPCASE

=PP5V_S0_FET → PP5V_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S0_SB
- =PP5V_S0_ODDPWREN
- =PP5V_S0_LPCPLUS
- =PP5V_S0_ISENSECAL
- =PP5V_S0_FAN_LT
- =PP5V_S0_FAN_RT
- =PP5V_S0_KBDLED
- =PP5V_S0_CPU_IMVP
- =PP5V_S0_GFXIMVP6
- =PP5V_S0_LCDBKLT
- =PP5V_S0_DVI_DDC
- =PP5V_S0_SB_HPD
- =PP5V_S0_HDD
- =PP5V_S0_PCIREQFIX

Chipset "VCore" Rails

=PPVCORE_S0_CPU_REG → PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.3 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
- =PPVCORE_S0_CPU

=PPVCORE_S0_NBGFX_REG → PPVCORE_S0_NB_GFX
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
- =PPVCORE_S0_NB_GFX
- =PPVCORE_S0_NBGFX_VSEN

3.3V-2.5V Rails

=PP3V3_S5_REG → PP3V3_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_S5_SB_PM
- =PP3V3_S5_SB_USB
- =PP3V3_S5_SB
- =PP3V3_S5_SB_CLINK1
- =PP3V3_S5_SB_GPIO
- =PP3V3_S5_SB_3V3_VCCSUSHDA
- =PP3V3_S5_SB_VCCSUS3_3
- =PP3V3_S5_SB_VCCSUS3_3_USB
- =PP3V3_S5_S5PWRGD
- =PP3V3_S5_SMBUS_SB_ME
- =PP3V3_S5_ROM
- =PP3V3_S5_P1V5P1V05PG
- =PP3V3_S5_PWRCTL
- =PP3V3_S3_P3V3S3FET
- =PP3V3_S0_P3V3S0FET
- =PP3V3_S0_LCD
- =PP3V3_GPU_P3V3GPUFET

=PP3V3_S3_FET → PP3V3_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_S3_P3V3ENETFET
- =PP3V3_S3_FW
- =PP3V3_S3_PCI
- =PP3V3_S3_SMBUS_SMC_A_S3
- =PP3V3_S3_RTALS
- =PP3V3_S3_SMS
- =PP3V3_S3_BT
- =PP3V3_S3_TOPCASE
- =PP3V3_S3_SMBUS_SMC_MGMT
- =PP3V3_S3_P1V25ISNS
- =PP3V3_S3_P1V8ISNS
- =PP3V3_S3_REMTHMSNS

=PP3V3_S0_FET → PP3V3_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_S0_NB_VCCHV
- =PP3V3_S0_NB_VCCA_PEG_BG
- =PP3V3_S0_NB_FOLLOW
- =PP3V3_S0_SB_GPIO
- =PP3V3_S0_SB_PCI
- =PP3V3_S0_SB_VCC3_3_IDE
- =PP3V3_S0_SB_VCC3_3_PCI
- =PP3V3R1V5_S0_SB_VCCHDA
- =PP3V3_S0_SB_VCC3_3_DMI
- =PP3V3_S0_SB_VCC3_3_VCCPCORE
- =PP3V3_S0_SB_VCCGLAN3_3
- =PP3V3_S0_SB_VCC3_3_SATA
- =PP3V3_S0_SB
- =PP3V3_S0_SB_PM
- =PP3V3_S0_RSTBUF
- =PP3V3_S0_CK505
- =PP3V3_S0_IDE
- =PP3V3_S0_SMC
- =PP3V3_S0_LPCPLUS
- =PP3V3_S0_SMBUS_SB
- =PP3V3_S0_SMBUS_SMC_B_S0
- =PP3V3_S0_CPUCOREISNS
- =PP3V3_S0_NBGFXCOREISNS
- =PP3V3_S0_CPUTHMSNS
- =PP3V3_S0_GPUTHMSNS
- =PP3V3_S0_FAN_LT
- =PP3V3_S0_FAN_RT
- =PP3V3_S0_IMVP
- =PP3V3_S0_GFXIMVP6
- =PP3V3_S0_NBCOREISNS
- =PP3V3_S0_ALLSYSPG
- =PP3V3_S0_DDC_LCD
- =PP3V3_S0_LCDBKLT
- =PP3V3_S0_LVDS_MUX
- =PP3V3R5V_GPU_GPUISENS
- =PP3V3_S0_XDP
- =PP3V3_S0M_CK505
- =PP3V3_S0_GPUCLKGATE
- =PPSPD_S0M_MEM_A
- =PPSPD_S0M_MEM_B
- =PP3V3_S0MWOL_SB_CLINK0
- =PP3V3_S0MWOL_SB_VCCCL3_3
- =PP3V3_S0MWOL_SB_VCCLAN3_3
- =PP3V3_S0_PBATTISENS
- =PP3V3_S0_PDCISENS
- =PP3V3_S0_TMPSNSR
- =PP3V3_S0_PWRCTL

=PP1V25_ENET_ISNS → PP1V25_ENET_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
- =PP1V25_S0_P1V25S0FET
- =PP1V25_GPU_P1V25GPUFET

1.8V-0.9V Rails

=PP1V8_S3_REG → PP1V8_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
- =PP1V8_S3_FW
- =PP1V8_S3M_MEM_A
- =PP1V8_S3M_MEM_B
- =PP1V8_S3_ISNS_R
- =PP1V8_GPU_P1V8GPUFET
- =PP1V8_S0_P1V8S0FET

=PP1V8_S3_ISNS → PP1V8_S3_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
- =PP1V8_S3M_MEM_NB
- =PP1V8_S3M_NB_VCC

=PP1V8_S0_FET → PP1V8_S0
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
MAX I = 0.36A
- =PP1V8_S0_NB_LVDS
- =PPVIN_S0_NB_DPLL

=PP1V5_S0_REG → PP1V5_S0
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
MAX I = ?.??A
- =PP1V5_S0_CPU
- =PP1V5_S0_NB_TVDAC
- =PP1V5_S0_SB
- =PP1V5_S0_SB_VCC1_5_A_ARX
- =PP1V5_S0_SB_VCC1_5_A_ATX
- =PP1V5_S0_SB_VCC1_5_A
- =PP1V5_S0_SB_VCCUSBPLL
- =PP1V5_S0_SB_VCC1_5_A_USB_CORE
- =PP1V5_S0_LIO

=PP1V25_S0_FET → PP1V25_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
- =PP1V25_S0M_NB_PLL
- =PP1V25_S0M_NB_VCC
- =PP1V25_S0M_NB_VCCA
- =PP1V25_S0_NB_VCCDMI
- =PP1V25_S0_NB_PLL
- =PP1V25_S0_NB_VCC
- =PP1V25_S0_SB_DMI

=PP1V05_S0_REG → PP1V05_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_S0M_NB_VCCAXM
- =PP1V05_S0_CPU
- =PP1V05_S0_NB_FOLLOW
- =PP1V05_S0_NB_PCIE
- =PP1V05_S0_SB_CPU_IO
- =PP1V05_S0_SMC_LS
- =PP1V25R1V05_S0_FSB_NB
- =PP1V25R1V05_S0_NB_VTT
- =PPVCORE_S0_NBCOREISNS
- =PPVCORE_S0_NB_FOLLOW
- =PPVCORE_S0_SB

=PPVCORE_S0_NB_R → PPVCORE_S0_NB_R
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
- =PPVCORE_S0_NB

=PP0V9_S3_VTTR_BUF → PP0V9_S3_MEM_VREF
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
- =PP0V9_S3M_MEM_NBVREFA
- =PP0V9_S3M_MEM_NBVREFB
- =PP0V9_S3M_MEM_DIMMVREFA
- =PP0V9_S3M_MEM_DIMMVREFB

=PP0V9_S0_VTT_LDO → PP0V9_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
- =PP0V9_S0M_MEM_TERM

"ENET" Rails

=PP3V3_ENET_FET → PP3V3_ENET
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_ENET_PHY
- =PP3V3_ENET_AVDDLDO

=PPVOUT_ENET_AVDDLDO → PP1V9_ENET
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.9V
MAKE_BASE=TRUE
- =PP1V8R2V5_ENET_PHY

=YUKON_EC_PP2V5_ENET
Yukon EC will not be supported

=PP1V25_ENET_REG → PP1V25_ENET
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
- =PP1V2_ENET_PHY
- =PP1V25_ENET_ISNS_R

"FW" (FireWire) Rails

PPBUS_FW_FWPWRSW_F → =PPBU_S0_P3V3FW
MAKE_BASE=TRUE

=PPBUS_S5_FW_FET → PPVP_FW
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.3 mm
VOLTAGE=8.5V
MAKE_BASE=TRUE
- =PPVP_FW_SUMNODE
- =PPVP_FW_CPS
- =PPVP_FW_P3V3FW

PPVP_FW_PORTA_UF → =PPVP_FW_PORT0
MAKE_BASE=TRUE

PPVP_FW_PORTB_UF → =PPVP_FW_PORT1
MAKE_BASE=TRUE

=PP3V3_FW_REG → PP3V3_FW
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_FW_PHY
- =PP3V3_FW_LATEVG_ACTIVE
- =PP3V3_FW_LATEVG
- =PPVIN_FW_P1V95FW

=PP1V95_FW_LDO → PP1V95_FW
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.95V
MAKE_BASE=TRUE
- =PP1V95_FW_PHY
- =PP1V8_FW_PHYOSC

"GPU" Rails

=PP3V3_GPU_FET → PP3V3_GPU
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_GPU_VDD33
- =PP3V3_GPU_MIO
- =PP3V3_GPU_DAC
- =PP3V3_GPU_DVI
- =PP3V3_GPU_LVDS_DDC
- =PP3V3_GPU_VGASYNC
- =PP3V3_GPU_TMDS
- =PP3V3_GPU_VIDEOMUX
- =PP2V5_GPU_LTC2900
- =PP3V3_GPU_SMBUS_SMC_0_S0
- =PP3V3_GPU_PWRCTL
- =PP3V3_GPU_VCORELOGIC
- =PP3V3_GPU_HDCP

=PP3V3_GPU_TMDS_FET → PP3V3_GPU_TMDS
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_GPU_TMDSBIAS
- =PP3V3_GPU_IFPCD_IOVDD

=PP1V8_GPU_FET → PP1V8_GPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
- =PP1V8_GPU_FB_VDD
- =PP1V8_GPU_FB_VDDQ
- =PP1V8_GPU_FBVDDQ
- =PP1V8_GPU_FBIO
- =PP1V8_GPU_IFPX

=PP1V25_GPU_FET → PP1V25_GPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD
- =PP1V2_GPU_FBPLLAVDD
- =PP1V2_GPU_VCOREPWRCTL

=PPVCORE_GPU_REG → PPVCORE_GPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
MAKE_BASE=TRUE
- =PPVCORE_GPU

Power Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

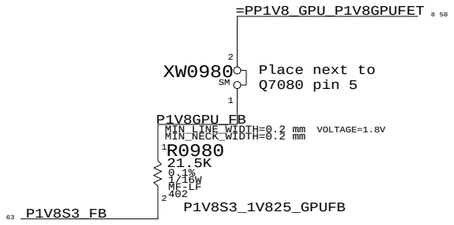
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 8 OF 109	



Stuff either R7520 or R0980.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
103S0192	1	RES,MTL FILM,21K,0.1,0402,SM,LF	R7580	CRITICAL	P1V8S3_1V8_GPUFB

28 25 7 PM_SB_PWROK = =SB_CLINK_MPWROK 25
MAKE_BASE=TRUE

59 28 16 7 VR_PWRGOOD_DELAY = =NB_CLINK_MPWROK 16
MAKE_BASE=TRUE

68 30 PEG_CLK100M_GPU_P = PEG_CLK100M_P 88
MAKE_BASE=TRUE

68 30 PEG_CLK100M_GPU_N = PEG_CLK100M_N 88
MAKE_BASE=TRUE

55 SMC_SMS_INT = =SMC_SMS_INT 45
MAKE_BASE=TRUE

60 GFX_VR_EN = =GFX_VR_EN 16
MAKE_BASE=TRUE

79 PM_ALL_NBGFX_PGOOD = GFXIMVP6_PGOOD 60
MAKE_BASE=TRUE

60 GFXIMVP6_VID<4..0> = GFX_VID<4..0> 16
MAKE_BASE=TRUE

79 28 24 7 PLT_RST_L = PLT_RESET_L 81
MAKE_BASE=TRUE

46 SMC_ENRGYSTR_LDO_EN = PBUS_LDO_EN 67

TP_MEM_A_A<15> = MEM_A_A<15> 31
MAKE_BASE=TRUE

TP_MEM_B_A<15> = MEM_B_A<15> 32
MAKE_BASE=TRUE

Thermal Module Holes

Top CPU TM "Hole"

Add 8 blind vias per side to GND

OMIT ZT0970 195R106 — Left CPU TM Hole

OMIT ZT0975 195R106 — Right CPU TM Hole

Top Right GPU TM Hole

OMIT ZT0985 195R106

OMIT ZT0980 195R106 — Bottom Left GPU TM Hole

All holes are plated through holes with two exceptions:

GND_CHASSIS_RIGHT_FAN_NOTCH (to the left of small well on lower board edge near USB)

GND_CHASSIS_BATTCONN_HOLE (to the left of DIMM cutout near board edge)

Chassis GNDs

OMIT ZT0901 195R106

GND_CHASSIS_RTIO
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE

= =GND_CHASSIS_FW_PORT0L 41
= =GND_CHASSIS_RTUSB 43

OMIT ZT0900 195R106

= =GND_CHASSIS_DVI_TOP 78

= =GND_CHASSIS_DVI_BOT 78

= =GND_CHASSIS_ENET 37
= =GND_CHASSIS_FW_PORT1 41
= =GND_CHASSIS_FW_PORT0U 41

Chassis connection to be made at the mounting hole east of the LVDS connector

GND_CHASSIS_LVDS
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
VOLTAGE=0V
MAKE_BASE=TRUE

SH0925
OG-503040
SHLD-SM-LF

GND_CHASSIS_INVERTER
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE

= =GND_CHASSIS_INVERTER 7 82
= =GND_CHASSIS_LEFTCLUTCH 44 80
= =GND_CHASSIS_J5590 51

Digital Ground

GND
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
VOLTAGE=0V

RAM door (Torx) holes

OMIT ZT0930 235R126

GND_CHASSIS_RAMDOOR_HOLE_0
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
VOLTAGE=0V

OMIT ZT0935 235R126

GND_CHASSIS_RAMDOOR_HOLE_1
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
VOLTAGE=0V

Frame holes

GND_CHASSIS_RIGHT_FAN_HOLE
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
VOLTAGE=0V

GND_CHASSIS_RIGHT_FAN_NOTCH
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
VOLTAGE=0V

GND_CHASSIS_DIMM_NOTCH
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
VOLTAGE=0V

OMIT ZT0955 195R106

GND_CHASSIS_LIOFLEX_HOLE
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
VOLTAGE=0V

9 GND_CHASSIS_BATTCONN_HOLE
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
VOLTAGE=0V

OMIT ZT0965 195R106

GND_CHASSIS_LNDACARD_HOLE
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
VOLTAGE=0V

9 GND_CHASSIS_BATTCONN_HOLE = =GND_BATT_CHGND 67
MAKE_BASE=TRUE

Signal Aliases

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/23/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

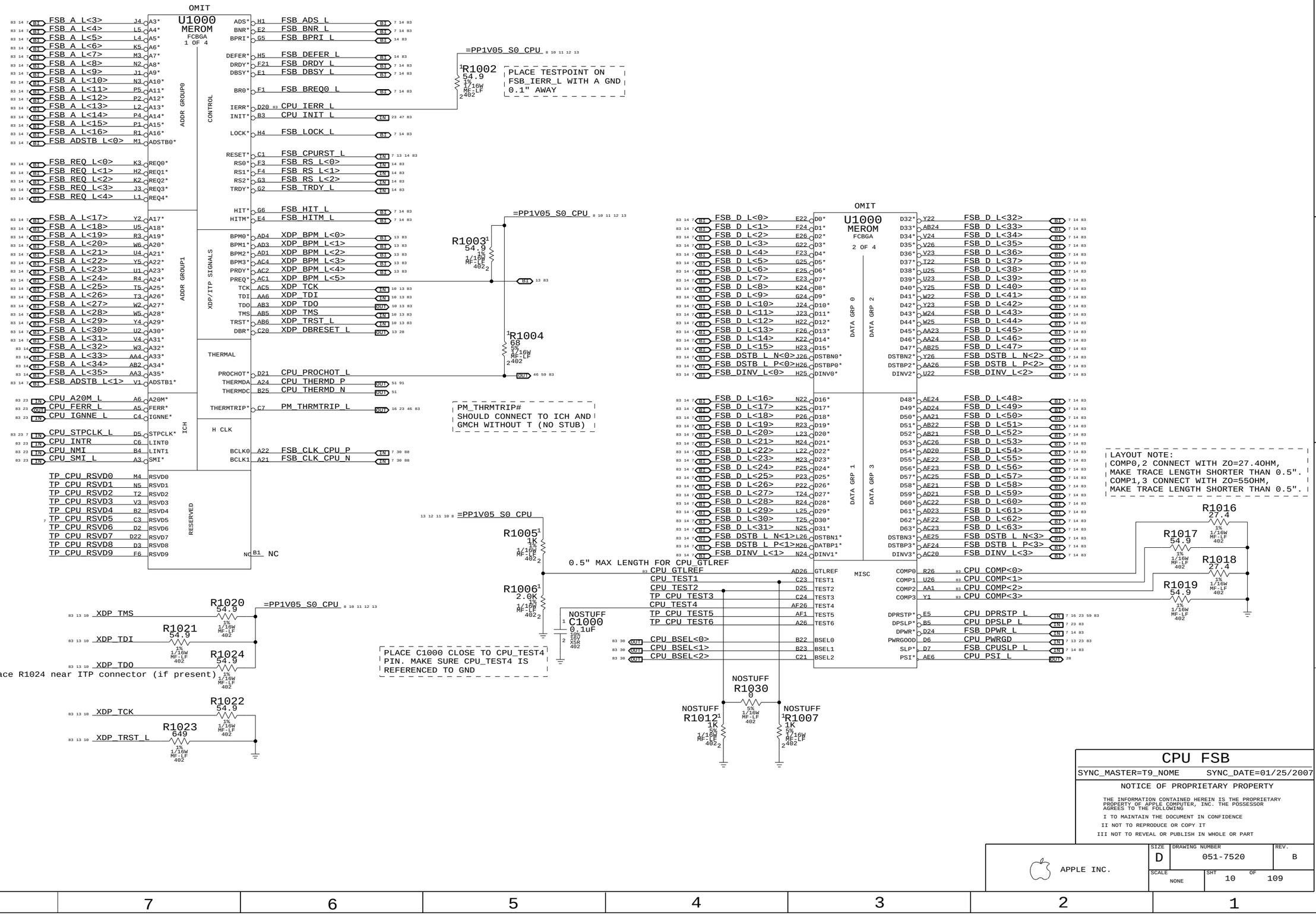
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 9 OF 109	



CPU FSB

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 10 OF 109	

(CPU CORE POWER)
=PPVCORE_S0_CPU 8 11 12 49

Standard Voltage:	Low Voltage:	Ultra Low Voltage:
44.0 A (Design Target)	23.0 A (Design Target)	17.0 A (Design Target)
41.0 A (HFM) 30.4 A (LFM) 25.5 A (SuperLFM)	21.0 A (HFM) 18.7 A (LFM) TBD A (SuperLFM)	TBD A (HFM) TBD A (LFM)
27.4 A (Auto-Halt/Stop-Grant HFM) 17.0 A (Auto-Halt/Stop-Grant SuperLFM)	TBD A (Auto-Halt/Stop-Grant HFM) TBD A (Auto-Halt/Stop-Grant SuperLFM)	TBD A (Auto-Halt/Stop-Grant HFM) TBD A (Auto-Halt/Stop-Grant LFM)
27.4 A (Sleep HFM) 16.8 A (Sleep SuperLFM)	TBD A (Sleep HFM) TBD A (Sleep SuperLFM)	TBD A (Sleep HFM) TBD A (Sleep LFM)
25.0 A (Deep Sleep HFM) 16.0 A (Deep Sleep SuperLFM)	TBD A (Deep Sleep HFM) TBD A (Deep Sleep SuperLFM)	TBD A (Deep Sleep HFM) TBD A (Deep Sleep LFM)
11.5 A (Deeper Sleep)	TBD A (Deeper Sleep)	TBD A (Deeper Sleep)
9.4 A (Enhanced Deeper Sleep)	TBD A (Enhanced Deeper Sleep)	TBD A (Enhanced Deeper Sleep)

OMIT
U1000
MEROM
FCBGA
3 OF 4

VCC: A7, A9, A10, A12, A13, A15, A17, A18, A20, B7, B9, B10, B12, B14, B15, B17, B18, B20, C9, C10, C12, C13, C15, C17, C18, D9, D10, D12, D14, D15, D17, D18, E7, E9, E10, E12, E13, E15, E17, E18, E20, F7, F9, F10, F12, F14, F15, F17, F18, F20, AA7, AA9, AA10, AA12, AA13, AA15, AA17, AA18, AA20, AB9, AC10, AB10, AB12, AB14, AB15, AB17, AB18

VCC: AB20, AB7, AC7, AC9, AC12, AC13, AC15, AC17, AC18, AD7, AD9, AD10, AD12, AD14, AD15, AD17, AD18, AE9, AE10, AE12, AE13, AE15, AE17, AE18, AE20, AF9, AF10, AF12, AF14, AF15, AF17, AF18, AF20

VCCP: G21, V6, J6, K6, M6, J21, K21, M21, N21, N6, R21, R6, T21, T6, V21, W21

(CPU IO POWER 1.05V)
=PP1V05_S0_CPU 8 10 12 13

4500 mA (before VCC stable)
2500 mA (after VCC stable)

(CPU INTERNAL PLL POWER 1.5V)
=PP1V5_S0_CPU 8 12

130 mA

VCCA: B26, C26

VID0	AD6	CPU_VID<0>	OUT 12 83
VID1	AF5	CPU_VID<1>	OUT 12 83
VID2	AE5	CPU_VID<2>	OUT 12 83
VID3	AF4	CPU_VID<3>	OUT 12 83
VID4	AE3	CPU_VID<4>	OUT 12 83
VID5	AF3	CPU_VID<5>	OUT 12 83
VID6	AE2	CPU_VID<6>	OUT 12 83
VCCSENSE	AF7	CPU_VCCSENSE_P	OUT 59 83
VSSSENSE	AE7	CPU_VCCSENSE_N	OUT 59 83

=PPVCORE_S0_CPU 8 11 12 49

R1100
100
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

R1101
100
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

OMIT
U1000
MEROM
FCBGA
4 OF 4

VSS: A4, A8, A11, A14, A16, A19, A23, AF2, B6, B8, B11, B13, B16, B19, B21, B24, C5, C8, C11, C14, C16, C19, C2, C22, C25, D1, D4, D8, D11, D13, D16, D19, D23, D26, E3, E6, E8, E11, E14, E16, E19, E21, E24, F5, F8, F11, F13, F16, F19, F2, F22, F25, G4, G1, G23, G26, H3, H6, H21, H24, J2, J5, J22, J25, K1, K4, K23, K26, L3, L6, L21, L24, M2, M5, M22, M25, N1, N4, N23, N26, P3

VSS: P6, P21, P24, R2, R5, R22, R25, T1, T4, T23, T26, U3, U6, U21, U24, V2, V5, V22, V25, W1, W4, W23, W26, Y3, Y6, Y21, Y24, AA2, AA5, AA8, AA11, AA14, AA16, AA19, AA22, AA25, AB1, AB4, AB8, AB11, AB13, AB16, AB19, AB23, AB26, AC3, AC6, AC8, AC11, AC14, AC16, AC19, AC21, AC24, AD2, AD5, AD8, AD11, AD13, AD16, AD19, AD22, AD25, AE1, AE4, AE8, AE11, AE14, AE16, AE19, AE23, AE26, A2, AF6, AF8, AF11, AF13, AF16, AF19, AF21, A25, AF25

CPU Power & Ground

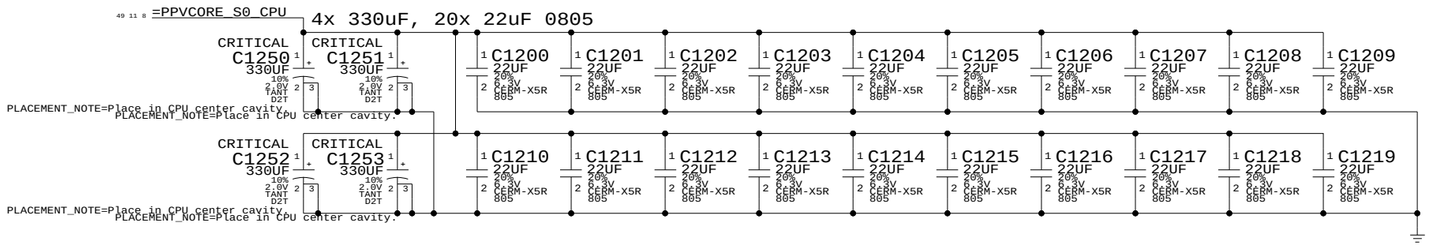
SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 11 OF 109	

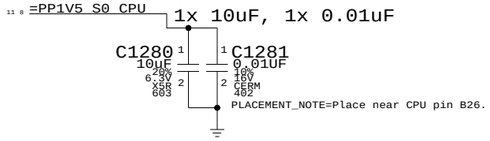
Current numbers from Merom for Santa Rosa EMTS, doc #22221.

CPU VCORE HF AND BULK DECOUPLING



VCCP (CPU I/O) DECOUPLING

VCCA (CPU AVdd) DECOUPLING



CPU VCORE VID CONNECTIONS

83 11 CPU_VID<0..6> = IMVP6_VID<0..6> 7 59 83
MAKE_BASE=TRUE

CPU Decoupling & VID

SYNC_MASTER=M75_MLB SYNC_DATE=12/07/2006

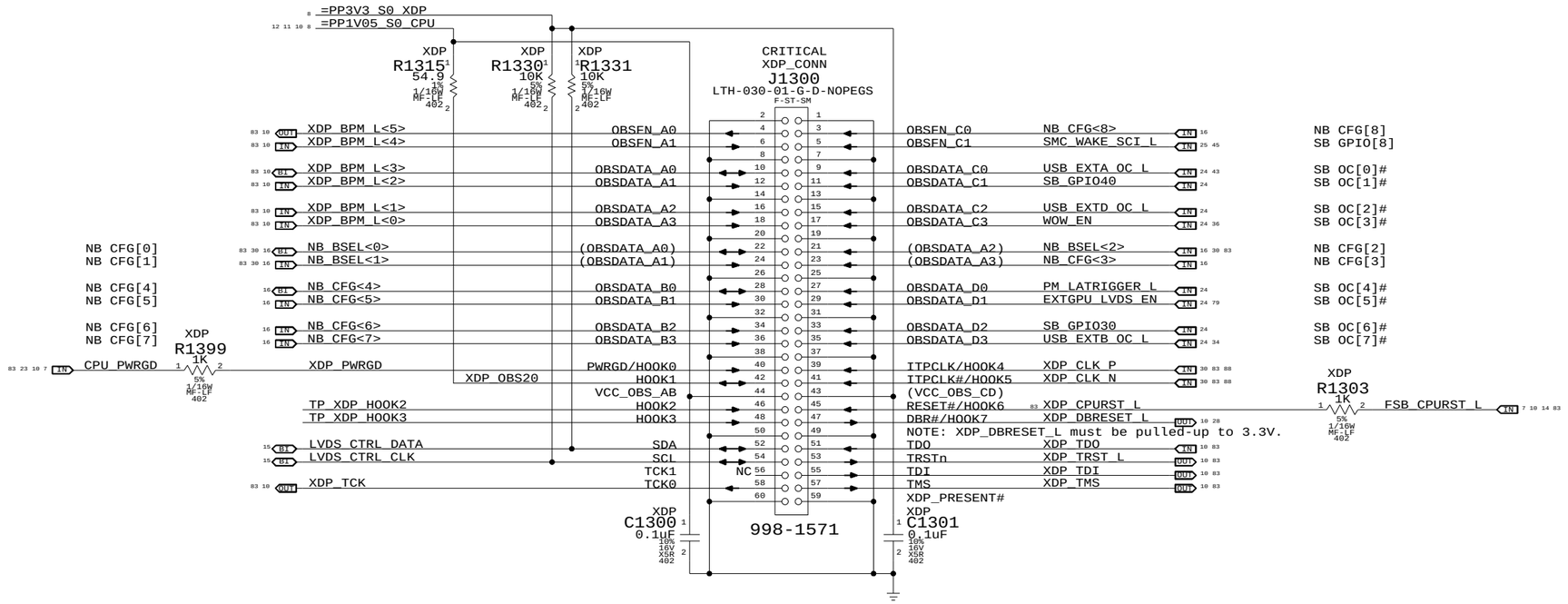
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 12 OF 109	

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0451 adapter board to support CPU, NB & SB debugging.



Direction of XDP module

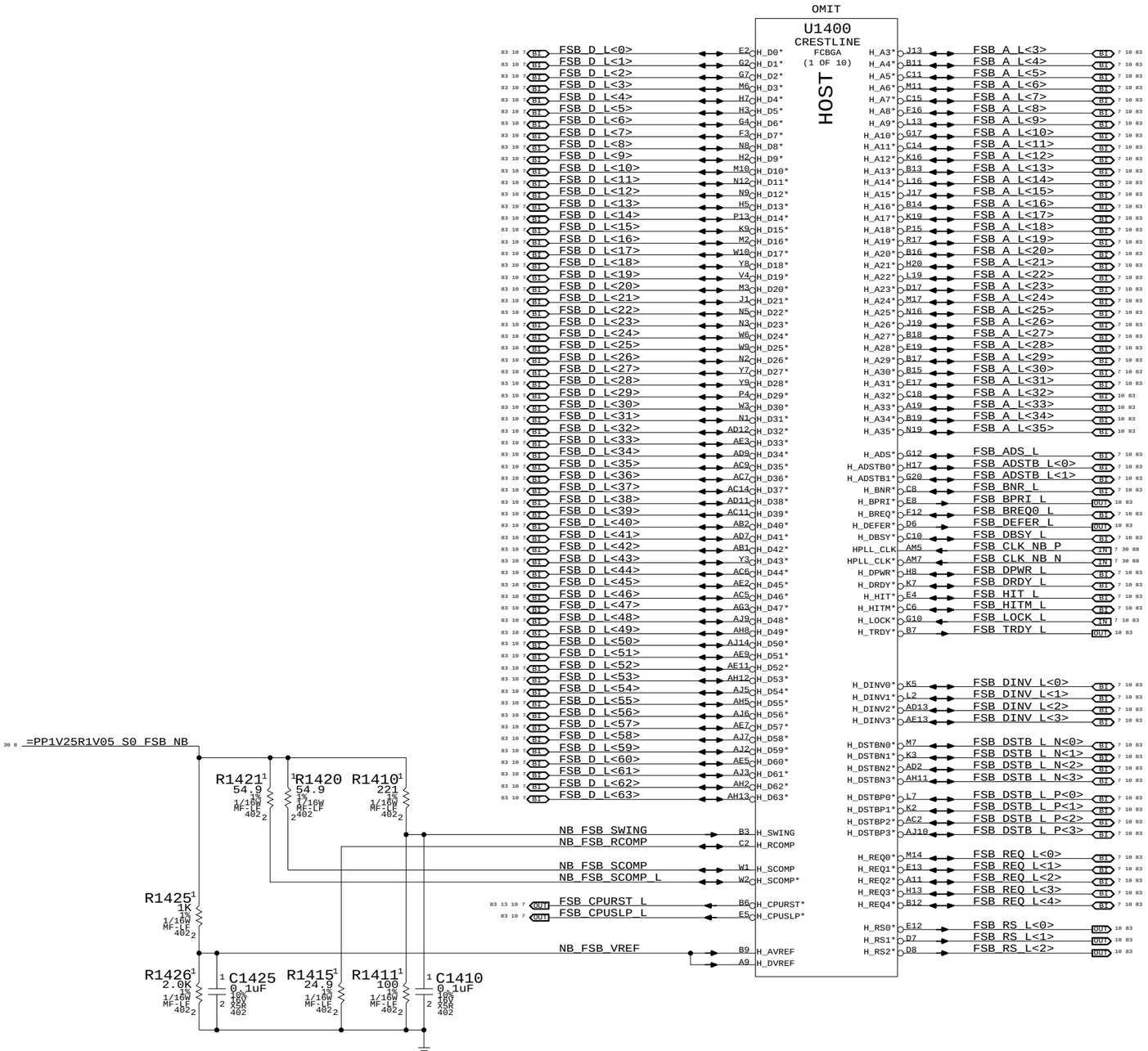
Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port (XDP)

SYNC_MASTER=T9_NOME SYNC_DATE=01/22/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE	SHT	OF
NONE	13	109



NB CPU Interface

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 14 OF 109	

LVDS Disable

Can leave all signals NC if LVDS is not implemented.
Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

Note: SR DG says to tie LVDS_VREFH/L to GND. This causes a glitch during wake-up on LVDS DATA/CLK pairs. New recommendation is to float both signals, see Radar #5067636.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

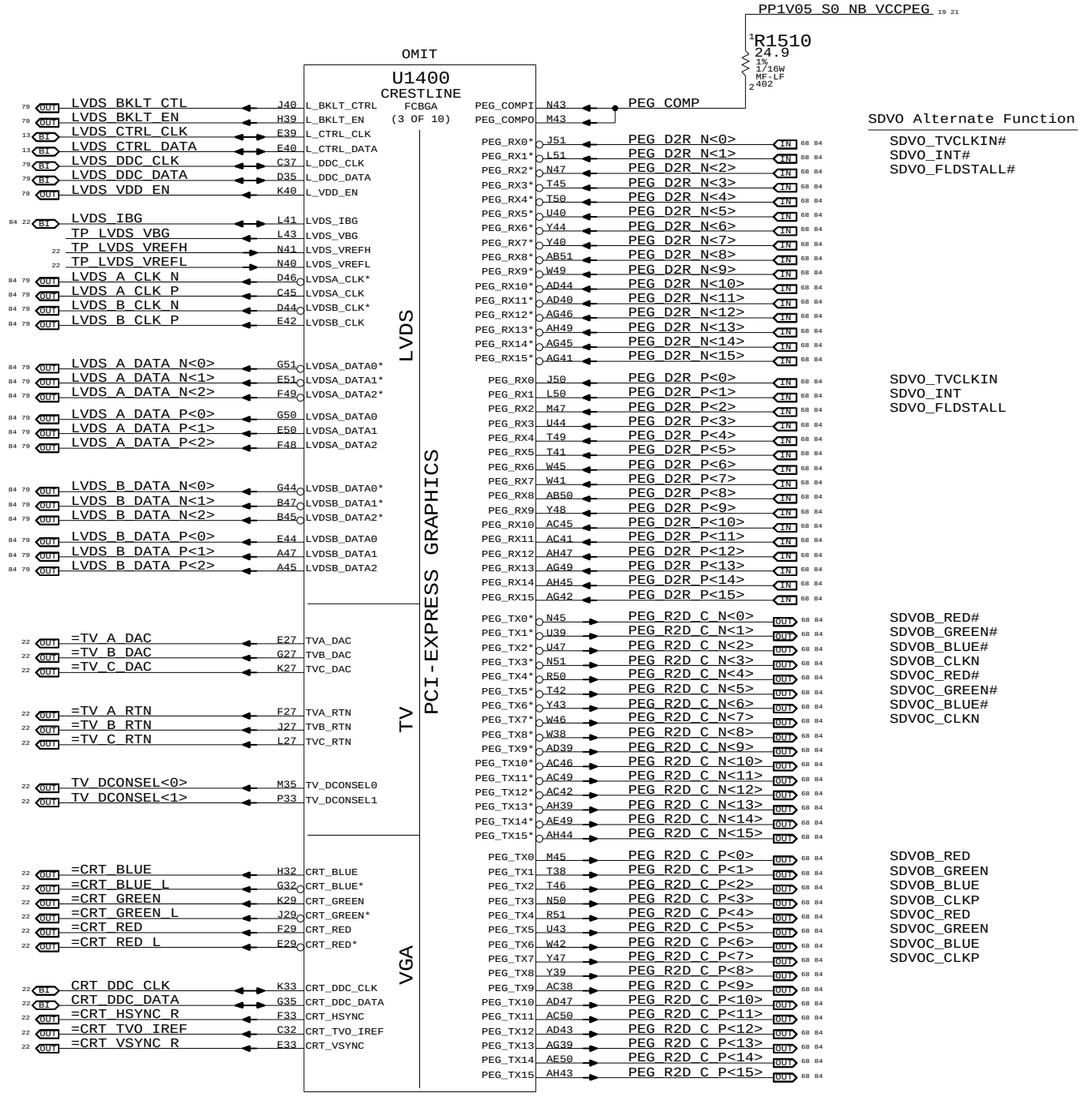
CRT & TV-Out Disable

Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TVO_IREF to GND.
Can tie the following rails to GND:
VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above.
Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and TV_DCONSELx to GND.
Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.



NB PEG / Video Interfaces

SYNC_MASTER=T9_NOME SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 15 OF 109	

NB_CFG<3>	RESERVED
NB_CFG<4>	RESERVED
NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2
NB_CFG<6>	RESERVED
NB_CFG<7>	RESERVED
NB_CFG<8>	RESERVED
NB_CFG<9> PCIe Graphics Lane Reversal	High = Normal Low = Reversed
NB_CFG<10>	RESERVED
NB_CFG<11>	RESERVED
NB_CFG<12>	See Below
NB_CFG<13>	See Below
NB_CFG<14>	RESERVED
NB_CFG<15>	RESERVED
NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled
NB_CFG<17>	RESERVED
NB_CFG<18>	RESERVED
NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal
NB_CFG<20> Concurrent SDVO/PCIe x1	High = Both active Low = Only SDVO or PCIe x16

NB_CFG<13:12>

00 = RESERVED
01 = XOR Mode Enabled
10 = All-Z Mode Enabled
11 = Normal Operation

NB_CFG<5> 13 16
NBCFG_DMI_X2
R1655 3.9K 5% 1/16W MF-LF 402

NB_CFG<9> 16
NBCFG_PEG_REVERSE
R1659 3.9K 5% 1/16W MF-LF 402

NB_CFG<16> 16
NBCFG_DYN_ODT_DISABLE
R1666 3.9K 5% 1/16W MF-LF 402

=PP3V3_S0_NB_VCCHV 8 16 19 21
NBCFG_DMI_REVERSE
R1669 3.9K 5% 1/16W MF-LF 402
NB_CFG<19> 16

=PP3V3_S0_NB_VCCHV 8 16 19 21
NBCFG_SDVO_AND_PCIE
R1670 3.9K 5% 1/16W MF-LF 402
NB_CFG<20> 16

NB CFG<8:0> used for debug access

NB CFG<13:12> require ICT access

21 19 16 8 =PP3V3_S0_NB_VCCHV
R1630 10K 5% 1/16W MF-LF 402
R1631 10K 5% 1/16W MF-LF 402
45 31 IN PM_EXTTS_L<0>
45 32 IN PM_EXTTS_L<1>

OMIT

U1400
CRESTLINE
FCBGA
(2 OF 10)

RSVD

TP_NB_RSVD<1>	P36	RSVD1
TP_NB_RSVD<2>	P37	RSVD2
TP_NB_RSVD<3>	R35	RSVD3
TP_NB_RSVD<4>	N35	RSVD4
TP_NB_RSVD<5>	AR12	RSVD5
TP_NB_RSVD<6>	AR13	RSVD6
TP_NB_RSVD<7>	AM12	RSVD7
TP_NB_RSVD<8>	AN13	RSVD8
TP_NB_RSVD<9>	J12	RSVD9
TP_NB_RSVD<10>	AR37	RSVD10
TP_NB_RSVD<11>	AM36	RSVD11
TP_NB_RSVD<12>	AL36	RSVD12
TP_NB_RSVD<13>	AM37	RSVD13
TP_NB_RSVD<14>	D20	RSVD14
TP_NB_RSVD<20>	H10	RSVD20
TP_NB_RSVD<21>	B51	RSVD21
TP_NB_RSVD<22>	BJ20	RSVD22
TP_NB_RSVD<23>	BK22	RSVD23
7 TP_NB_RSVD<24>	BF19	RSVD24
TP_NB_RSVD<25>	BH20	RSVD25
7 TP_NB_RSVD<26>	BK18	RSVD26
7 TP_NB_RSVD<27>	BJ18	RSVD27
TP_MEM_CLKP2	BF23	SM_CK2
TP_MEM_CLKN2	BG23	SM_CK2*
TP_MEM_CLKP5	BC23	SM_CK5
TP_MEM_CLKN5	BD24	SM_CK5*
85 33 31 OUT MEM_A_A<14>	BJ29	SA_MA14
85 33 32 OUT MEM_B_A<14>	BE24	SB_MA14
TP_NB_RSVD<34>	BH39	RSVD34
TP_NB_RSVD<35>	AW20	RSVD35
TP_NB_RSVD<36>	BK20	RSVD36
TP_LVDS_A_DATAN3	C48	RSVD37
TP_LVDS_A_DATAP3	D47	RSVD38
TP_LVDS_B_DATAN3	B44	RSVD39
TP_LVDS_B_DATAP3	C44	RSVD40
TP_NB_RSVD<41>	A35	RSVD41
TP_NB_RSVD<42>	B37	RSVD42
TP_NB_RSVD<43>	B36	RSVD43
TP_NB_RSVD<44>	B34	RSVD44
TP_NB_RSVD<45>	C34	RSVD45

CFG

83 30 13 IN NB_BSEL<0>	P27	CFG0	
83 30 13 IN NB_BSEL<1>	N27	CFG1	
83 30 13 IN NB_BSEL<2>	N24	CFG2	
13 OUT NB_CFG<3>	C21	CFG3	IPU
13 BI NB_CFG<4>	C23	CFG4	IPU
16 13 BI NB_CFG<5>	F23	CFG5	IPU
13 OUT NB_CFG<6>	N23	CFG6	IPU
13 OUT NB_CFG<7>	G23	CFG7	IPU
13 OUT NB_CFG<8>	J20	CFG8	IPU
16 NB_CFG<9>	C20	CFG9	IPU
TP_NB_CFG<10>	R24	CFG10	IPU
TP_NB_CFG<11>	L23	CFG11	IPU
TP_NB_CFG<12>	J23	CFG12	IPU
TP_NB_CFG<13>	E23	CFG13	IPU
TP_NB_CFG<14>	E20	CFG14	IPU
TP_NB_CFG<15>	K23	CFG15	IPU
16 NB_CFG<16>	M20	CFG16	IPU
TP_NB_CFG<17>	M24	CFG17	IPU
TP_NB_CFG<18>	L32	CFG18	IPD
16 NB_CFG<19>	N33	CFG19	IPD
16 NB_CFG<20>	L35	CFG20	IPD

PM

25 7 OUT PM_BMBUSY_L	G41	PM_BM_BUSY*
83 59 23 10 7 IN CPU_DPRSTP_L	L39	PM_DPRSTP*
	L36	PM_EXT_TS0*
	J36	PM_EXT_TS1*
59 28 9 7 IN VR_PWRGOOD_DELAY	AW49	PWROK
28 7 IN NB_RESET_L	AV20	RSTIN*
83 46 23 10 OUT PM_THRMTRIP_L	N20	THERMTRIP*
83 59 25 7 IN PM_DPRSLPVR	G36	DPRSLPVR

NC

7 TP_NB_NC<1>	BJ51	NC1
7 TP_NB_NC<2>	BK51	NC2
7 TP_NB_NC<3>	BK50	NC3
7 TP_NB_NC<4>	BL50	NC4
7 TP_NB_NC<5>	BL49	NC5
7 TP_NB_NC<6>	BL3	NC6
7 TP_NB_NC<7>	BL2	NC7
7 TP_NB_NC<8>	BK1	NC8
7 TP_NB_NC<9>	BJ1	NC9
7 TP_NB_NC<10>	E1	NC10
7 TP_NB_NC<11>	A5	NC11
7 TP_NB_NC<12>	C51	NC12
7 TP_NB_NC<13>	B50	NC13
7 TP_NB_NC<14>	A50	NC14
7 TP_NB_NC<15>	A49	NC15
7 TP_NB_NC<16>	BK2	NC16

DDR MUXING

SM_CK0	AV29	MEM_CLK_P<0>	OUT 31 85
SM_CK1	BB23	MEM_CLK_P<1>	OUT 31 85
SM_CK3	BA25	MEM_CLK_P<3>	OUT 32 85
SM_CK4	AV23	MEM_CLK_P<4>	OUT 32 85
SM_CK0*	AW30	MEM_CLK_N<0>	OUT 31 85
SM_CK1*	BA23	MEM_CLK_N<1>	OUT 31 85
SM_CK3*	AW25	MEM_CLK_N<3>	OUT 32 85
SM_CK4*	AW23	MEM_CLK_N<4>	OUT 32 85
SM_CKE0	BE29	MEM_CKE<0>	OUT 31 33 85
SM_CKE1	AY32	MEM_CKE<1>	OUT 31 33 85
SM_CKE3	BD39	MEM_CKE<3>	OUT 32 33 85
SM_CKE4	BG37	MEM_CKE<4>	OUT 32 33 85
SM_CS0*	BG20	MEM_CS_L<0>	OUT 31 33 85
SM_CS1*	BK16	MEM_CS_L<1>	OUT 31 33 85
SM_CS2*	BG16	MEM_CS_L<2>	OUT 32 33 85
SM_CS3*	BE13	MEM_CS_L<3>	OUT 32 33 85
SM_ODT0	BH18	MEM_ODT<0>	OUT 31 33 85
SM_ODT1	BJ15	MEM_ODT<1>	OUT 31 33 85
SM_ODT2	BJ14	MEM_ODT<2>	OUT 32 33 85
SM_ODT3	BE16	MEM_ODT<3>	OUT 32 33 85
SM_RCOMP	BL15	MEM_RCOMP	
SM_RCOMP*	BK14	MEM_RCOMP_L	
SM_RCOMP_VOH	BK31	MEM_RCOMP_VOH	
SM_RCOMP_VOL	BL31	MEM_RCOMP_VOL	
SM_VREF0	AR49	=PP0V9_S3M_MEM_NBVREFA	IN 8
SM_VREF1	AW4	=PP0V9_S3M_MEM_NBVREFB	IN 8

21 18 8 =PP1V8_S3M_MEM_NB
R1610 20 1% 1/10W MF-LF 402
R1611 20 1% 1/10W MF-LF 402
R1620 1K 1% 1/16W MF-LF 402
R1622 3.01K 1% 1/16W MF-LF 402
R1624 1K 1% 1/16W MF-LF 402
C1623 0.01UF 10% 16V CERM 402
C1622 2.2UF 20% 6.3V CERM1 603
C1625 0.01UF 10% 16V CERM 402
C1624 2.2UF 20% 6.3V CERM1 603
C1615 0.1UF 20% 10V CERM 402
C1616 0.1UF 20% 10V CERM 402

CLK

DPLL_REF_CLK	B42	=NB_CLK96M_DOT_P	IN 22
DPLL_REF_CLK*	C42	=NB_CLK96M_DOT_N	IN 22
DPLL_REF_SSCLK	H48	=NB_CLK100M_DPLLSS_P	IN 22
DPLL_REF_SSCLK*	H47	=NB_CLK100M_DPLLSS_N	IN 22
PEG_CLK	K44	NB_CLK100M_PCIE_P	IN 7 30 88
PEG_CLK*	K45	NB_CLK100M_PCIE_N	IN 7 30 88

Clk used for PEG and DMI

DMI

DMI_RXN0	AN47	DMI_S2N_N<0>	IN 24 84
DMI_RXN1	AJ38	DMI_S2N_N<1>	IN 24 84
DMI_RXN2	AN42	DMI_S2N_N<2>	IN 24 84
DMI_RXN3	AN46	DMI_S2N_N<3>	IN 24 84
DMI_RXP0	AM47	DMI_S2N_P<0>	IN 24 84
DMI_RXP1	AJ39	DMI_S2N_P<1>	IN 24 84
DMI_RXP2	AN41	DMI_S2N_P<2>	IN 24 84
DMI_RXP3	AN45	DMI_S2N_P<3>	IN 24 84
DMI_TXN0	AJ46	DMI_N2S_N<0>	OUT 24 84
DMI_TXN1	AJ41	DMI_N2S_N<1>	OUT 24 84
DMI_TXN2	AM40	DMI_N2S_N<2>	OUT 24 84
DMI_TXN3	AM44	DMI_N2S_N<3>	OUT 24 84
DMI_TXP0	AJ47	DMI_N2S_P<0>	OUT 24 84
DMI_TXP1	AJ42	DMI_N2S_P<1>	OUT 24 84
DMI_TXP2	AM39	DMI_N2S_P<2>	OUT 24 84
DMI_TXP3	AM43	DMI_N2S_P<3>	OUT 24 84

GRAPHICS VID

GFX_VID0	E35	GFX_VID<0>	OUT 9
GFX_VID1	A39	GFX_VID<1>	OUT 9
GFX_VID2	C38	GFX_VID<2>	OUT 9
GFX_VID3	B39	GFX_VID<3>	OUT 9
GFX_VR_EN	E36	GFX_VID<4>	OUT 9
		=GFX_VR_EN	OUT 9

MISC

CL_CLK	AM49	CLINK_NB_CLK	BI 25 87
CL_DATA	AK50	CLINK_NB_DATA	BI 25 87
CL_PWROK	AT43	=NB_CLINK_MPWROK	IN 9
CL_RST*	AN49	CLINK_NB_RESET_L	OUT 25 87
CL_VREF	AM50	87 NB_CLINK_VREF	
SDVO_CTRL_CLK	H35	SDVO_CTRLCLK	BI 22
SDVO_CTRL_DATA	K36	SDVO_CTRLDATA	BI 22
CLKREQ*	G39	NB_CLKREQ_L	OUT 7 29
ICH_SYNC*	G40	NB_SB_SYNC_L	OUT 7 25
TEST1	A37	NB_TEST1	
TEST2	R32	NB_TEST2	

R1691 20K 5% 1/16W MF-LF 402
R1690 0 5% 1/16W MF-LF 402

PP1V25_S0M_NB_VCCAXD 19 21
R1640 1K 1% 1/16W MF-LF 402
C1640 0.1UF 20% 10V CERM 402
R1641 392 1% 1/16W MF-LF 402

NOTE: GMCH CL_PWROK input must be PWRGD signal for PP3V3_S0M, PP3V3_S0MWOL, PP1V8_S3M, PP1V25_S0M, PP1V05_S0M, PP0V9_S3M and PP0V9_S0M.
If ME/AMT is not used, short CL_PWROK to PWROK.

NB Misc Interfaces

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 16 OF 109	

OMIT

U1400
CRESTLINE
FCBGA
(4 OF 10)

DDR SYSTEM MEMORY A

MEM_A_DQ<0>	AR43	SA_DQ0	SA_BS0	BB19	MEM_A_BS<0>	OUT
MEM_A_DQ<1>	AW44	SA_DQ1	SA_BS1	BK19	MEM_A_BS<1>	OUT
MEM_A_DQ<2>	BA45	SA_DQ2	SA_BS2	BF29	MEM_A_BS<2>	OUT
MEM_A_DQ<3>	AY46	SA_DQ3	SA_CAS*	BL17	MEM_A_CAS_L	OUT
MEM_A_DQ<4>	AR41	SA_DQ4				
MEM_A_DQ<5>	AR45	SA_DQ5	SA_DM0	AT45	MEM_A_DM<0>	OUT
MEM_A_DQ<6>	AT42	SA_DQ6	SA_DM1	BD44	MEM_A_DM<1>	OUT
MEM_A_DQ<7>	AW47	SA_DQ7	SA_DM2	BD42	MEM_A_DM<2>	OUT
MEM_A_DQ<8>	BB45	SA_DQ8	SA_DM3	AW38	MEM_A_DM<3>	OUT
MEM_A_DQ<9>	BF48	SA_DQ9	SA_DM4	AW13	MEM_A_DM<4>	OUT
MEM_A_DQ<10>	BG47	SA_DQ10	SA_DM5	BG8	MEM_A_DM<5>	OUT
MEM_A_DQ<11>	BJ45	SA_DQ11	SA_DM6	AY5	MEM_A_DM<6>	OUT
MEM_A_DQ<12>	BB47	SA_DQ12	SA_DM7	AN6	MEM_A_DM<7>	OUT
MEM_A_DQ<13>	BG50	SA_DQ13				
MEM_A_DQ<14>	BH49	SA_DQ14	SA_DQS0	AT46	MEM_A_DQS_P<0>	BI
MEM_A_DQ<15>	BE45	SA_DQ15	SA_DQS1	BE48	MEM_A_DQS_P<1>	BI
MEM_A_DQ<16>	AW43	SA_DQ16	SA_DQS2	BB43	MEM_A_DQS_P<2>	BI
MEM_A_DQ<17>	BE44	SA_DQ17	SA_DQS3	BC37	MEM_A_DQS_P<3>	BI
MEM_A_DQ<18>	BG42	SA_DQ18	SA_DQS4	BB16	MEM_A_DQS_P<4>	BI
MEM_A_DQ<19>	BE40	SA_DQ19	SA_DQS5	BH6	MEM_A_DQS_P<5>	BI
MEM_A_DQ<20>	BF44	SA_DQ20	SA_DQS6	BB2	MEM_A_DQS_P<6>	BI
MEM_A_DQ<21>	BH45	SA_DQ21	SA_DQS7	AP3	MEM_A_DQS_P<7>	BI
MEM_A_DQ<22>	BG40	SA_DQ22	SA_DQS0*	AT47	MEM_A_DQS_N<0>	BI
MEM_A_DQ<23>	BF40	SA_DQ23	SA_DQS1*	BD47	MEM_A_DQS_N<1>	BI
MEM_A_DQ<24>	AR40	SA_DQ24	SA_DQS2*	BC41	MEM_A_DQS_N<2>	BI
MEM_A_DQ<25>	AW40	SA_DQ25	SA_DQS3*	BA37	MEM_A_DQS_N<3>	BI
MEM_A_DQ<26>	AT39	SA_DQ26	SA_DQS4*	BA16	MEM_A_DQS_N<4>	BI
MEM_A_DQ<27>	AW36	SA_DQ27	SA_DQS5*	BH7	MEM_A_DQS_N<5>	BI
MEM_A_DQ<28>	AW41	SA_DQ28	SA_DQS6*	BC1	MEM_A_DQS_N<6>	BI
MEM_A_DQ<29>	AY41	SA_DQ29	SA_DQS7*	AP2	MEM_A_DQS_N<7>	BI
MEM_A_DQ<30>	AV38	SA_DQ30				
MEM_A_DQ<31>	AT38	SA_DQ31	SA_MA0	BJ19	MEM_A_A<0>	OUT
MEM_A_DQ<32>	AV13	SA_DQ32	SA_MA1	BD20	MEM_A_A<1>	OUT
MEM_A_DQ<33>	AT13	SA_DQ33	SA_MA2	BK27	MEM_A_A<2>	OUT
MEM_A_DQ<34>	AW11	SA_DQ34	SA_MA3	BH28	MEM_A_A<3>	OUT
MEM_A_DQ<35>	AV11	SA_DQ35	SA_MA4	BL24	MEM_A_A<4>	OUT
MEM_A_DQ<36>	AU15	SA_DQ36	SA_MA5	BK28	MEM_A_A<5>	OUT
MEM_A_DQ<37>	AT11	SA_DQ37	SA_MA6	BJ27	MEM_A_A<6>	OUT
MEM_A_DQ<38>	BA13	SA_DQ38	SA_MA7	BJ25	MEM_A_A<7>	OUT
MEM_A_DQ<39>	BA11	SA_DQ39	SA_MA8	BL28	MEM_A_A<8>	OUT
MEM_A_DQ<40>	BE10	SA_DQ40	SA_MA9	BA28	MEM_A_A<9>	OUT
MEM_A_DQ<41>	BD10	SA_DQ41	SA_MA10	BC19	MEM_A_A<10>	OUT
MEM_A_DQ<42>	BD8	SA_DQ42	SA_MA11	BE28	MEM_A_A<11>	OUT
MEM_A_DQ<43>	AY9	SA_DQ43	SA_MA12	BG30	MEM_A_A<12>	OUT
MEM_A_DQ<44>	BG10	SA_DQ44	SA_MA13	BJ16	MEM_A_A<13>	OUT
MEM_A_DQ<45>	AW9	SA_DQ45				
MEM_A_DQ<46>	BD7	SA_DQ46	SA_RAS*	BE18	MEM_A_RAS_L	OUT
MEM_A_DQ<47>	BB9	SA_DQ47	SA_RCVEN*	AY20	TP_MEM_A_RCVEN_L	
MEM_A_DQ<48>	BB5	SA_DQ48				
MEM_A_DQ<49>	AY7	SA_DQ49	SA_WE*	BA19	MEM_A_WE_L	OUT
MEM_A_DQ<50>	AT5	SA_DQ50				
MEM_A_DQ<51>	AT7	SA_DQ51				
MEM_A_DQ<52>	AY6	SA_DQ52				
MEM_A_DQ<53>	BB7	SA_DQ53				
MEM_A_DQ<54>	AR5	SA_DQ54				
MEM_A_DQ<55>	AR8	SA_DQ55				
MEM_A_DQ<56>	AR9	SA_DQ56				
MEM_A_DQ<57>	AN3	SA_DQ57				
MEM_A_DQ<58>	AM8	SA_DQ58				
MEM_A_DQ<59>	AN10	SA_DQ59				
MEM_A_DQ<60>	AT9	SA_DQ60				
MEM_A_DQ<61>	AN9	SA_DQ61				
MEM_A_DQ<62>	AM9	SA_DQ62				
MEM_A_DQ<63>	AN11	SA_DQ63				

OMIT

U1400
CRESTLINE
FCBGA
(5 OF 10)

DDR SYSTEM MEMORY B

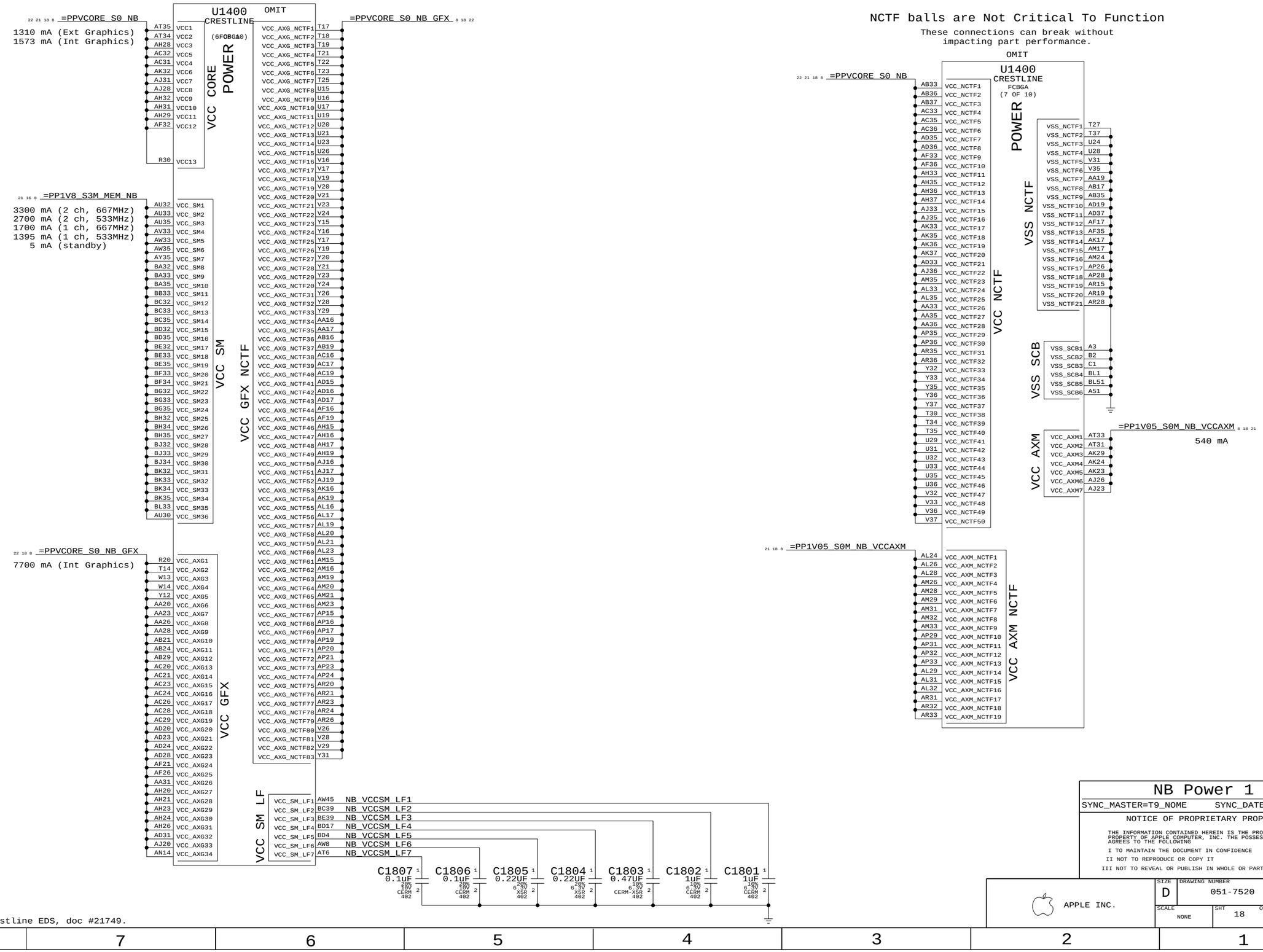
MEM_B_DQ<0>	AP49	SB_DQ0	SB_BS0	AY17	MEM_B_BS<0>	OUT
MEM_B_DQ<1>	AR51	SB_DQ1	SB_BS1	BG18	MEM_B_BS<1>	OUT
MEM_B_DQ<2>	AW50	SB_DQ2	SB_BS2	BG36	MEM_B_BS<2>	OUT
MEM_B_DQ<3>	AW51	SB_DQ3	SB_CAS*	BE17	MEM_B_CAS_L	OUT
MEM_B_DQ<4>	AN51	SB_DQ4				
MEM_B_DQ<5>	AN50	SB_DQ5	SB_DM0	AR50	MEM_B_DM<0>	OUT
MEM_B_DQ<6>	AV50	SB_DQ6	SB_DM1	BD49	MEM_B_DM<1>	OUT
MEM_B_DQ<7>	AV49	SB_DQ7	SB_DM2	BK45	MEM_B_DM<2>	OUT
MEM_B_DQ<8>	BA50	SB_DQ8	SB_DM3	BL39	MEM_B_DM<3>	OUT
MEM_B_DQ<9>	BB50	SB_DQ9	SB_DM4	BH12	MEM_B_DM<4>	OUT
MEM_B_DQ<10>	BA49	SB_DQ10	SB_DM5	BJ7	MEM_B_DM<5>	OUT
MEM_B_DQ<11>	BE50	SB_DQ11	SB_DM6	BF3	MEM_B_DM<6>	OUT
MEM_B_DQ<12>	BA51	SB_DQ12	SB_DM7	AW2	MEM_B_DM<7>	OUT
MEM_B_DQ<13>	AY49	SB_DQ13				
MEM_B_DQ<14>	BF50	SB_DQ14	SB_DQS0	AT50	MEM_B_DQS_P<0>	BI
MEM_B_DQ<15>	BF49	SB_DQ15	SB_DQS1	BD50	MEM_B_DQS_P<1>	BI
MEM_B_DQ<16>	BJ50	SB_DQ16	SB_DQS2	BK46	MEM_B_DQS_P<2>	BI
MEM_B_DQ<17>	BJ44	SB_DQ17	SB_DQS3	BK39	MEM_B_DQS_P<3>	BI
MEM_B_DQ<18>	BJ43	SB_DQ18	SB_DQS4	BJ12	MEM_B_DQS_P<4>	BI
MEM_B_DQ<19>	BL43	SB_DQ19	SB_DQS5	BL7	MEM_B_DQS_P<5>	BI
MEM_B_DQ<20>	BK47	SB_DQ20	SB_DQS6	BE2	MEM_B_DQS_P<6>	BI
MEM_B_DQ<21>	BK49	SB_DQ21	SB_DQS7	AV2	MEM_B_DQS_P<7>	BI
MEM_B_DQ<22>	BK43	SB_DQ22	SB_DQS0*	AU50	MEM_B_DQS_N<0>	BI
MEM_B_DQ<23>	BK42	SB_DQ23	SB_DQS1*	BC50	MEM_B_DQS_N<1>	BI
MEM_B_DQ<24>	BJ41	SB_DQ24	SB_DQS2*	BL45	MEM_B_DQS_N<2>	BI
MEM_B_DQ<25>	BL41	SB_DQ25	SB_DQS3*	BK38	MEM_B_DQS_N<3>	BI
MEM_B_DQ<26>	BJ37	SB_DQ26	SB_DQS4*	BK12	MEM_B_DQS_N<4>	BI
MEM_B_DQ<27>	BJ36	SB_DQ27	SB_DQS5*	BK7	MEM_B_DQS_N<5>	BI
MEM_B_DQ<28>	BK41	SB_DQ28	SB_DQS6*	BF2	MEM_B_DQS_N<6>	BI
MEM_B_DQ<29>	BJ40	SB_DQ29	SB_DQS7*	AV3	MEM_B_DQS_N<7>	BI
MEM_B_DQ<30>	BL35	SB_DQ30				
MEM_B_DQ<31>	BK37	SB_DQ31	SB_MA0	BC18	MEM_B_A<0>	OUT
MEM_B_DQ<32>	BK13	SB_DQ32	SB_MA1	BG28	MEM_B_A<1>	OUT
MEM_B_DQ<33>	BE11	SB_DQ33	SB_MA2	BG25	MEM_B_A<2>	OUT
MEM_B_DQ<34>	BK11	SB_DQ34	SB_MA3	AW17	MEM_B_A<3>	OUT
MEM_B_DQ<35>	BC11	SB_DQ35	SB_MA4	BF25	MEM_B_A<4>	OUT
MEM_B_DQ<36>	BC13	SB_DQ36	SB_MA5	BE25	MEM_B_A<5>	OUT
MEM_B_DQ<37>	BE12	SB_DQ37	SB_MA6	BA29	MEM_B_A<6>	OUT
MEM_B_DQ<38>	BC12	SB_DQ38	SB_MA7	BC28	MEM_B_A<7>	OUT
MEM_B_DQ<39>	BG12	SB_DQ39	SB_MA8	AY28	MEM_B_A<8>	OUT
MEM_B_DQ<40>	BJ10	SB_DQ40	SB_MA9	BD37	MEM_B_A<9>	OUT
MEM_B_DQ<41>	BL9	SB_DQ41	SB_MA10	BG17	MEM_B_A<10>	OUT
MEM_B_DQ<42>	BK5	SB_DQ42	SB_MA11	BE37	MEM_B_A<11>	OUT
MEM_B_DQ<43>	BL5	SB_DQ43	SB_MA12	BA39	MEM_B_A<12>	OUT
MEM_B_DQ<44>	BK9	SB_DQ44	SB_MA13	BG13	MEM_B_A<13>	OUT
MEM_B_DQ<45>	BK10	SB_DQ45				
MEM_B_DQ<46>	BJ8	SB_DQ46	SB_RAS*	AV16	MEM_B_RAS_L	OUT
MEM_B_DQ<47>	BJ6	SB_DQ47	SB_RCVEN*	AY18	TP_MEM_B_RCVEN_L	
MEM_B_DQ<48>	BF4	SB_DQ48				
MEM_B_DQ<49>	BH5	SB_DQ49	SB_WE*	BC17	MEM_B_WE_L	OUT
MEM_B_DQ<50>	BG1	SB_DQ50				
MEM_B_DQ<51>	BC2	SB_DQ51				
MEM_B_DQ<52>	BK3	SB_DQ52				
MEM_B_DQ<53>	BE4	SB_DQ53				
MEM_B_DQ<54>	BD3	SB_DQ54				
MEM_B_DQ<55>	BJ2	SB_DQ55				
MEM_B_DQ<56>	BA3	SB_DQ56				
MEM_B_DQ<57>	BB3	SB_DQ57				
MEM_B_DQ<58>	AR1	SB_DQ58				
MEM_B_DQ<59>	AT3	SB_DQ59				
MEM_B_DQ<60>	AY2	SB_DQ60				
MEM_B_DQ<61>	AY3	SB_DQ61				
MEM_B_DQ<62>	AU2	SB_DQ62				
MEM_B_DQ<63>	AT2	SB_DQ63				

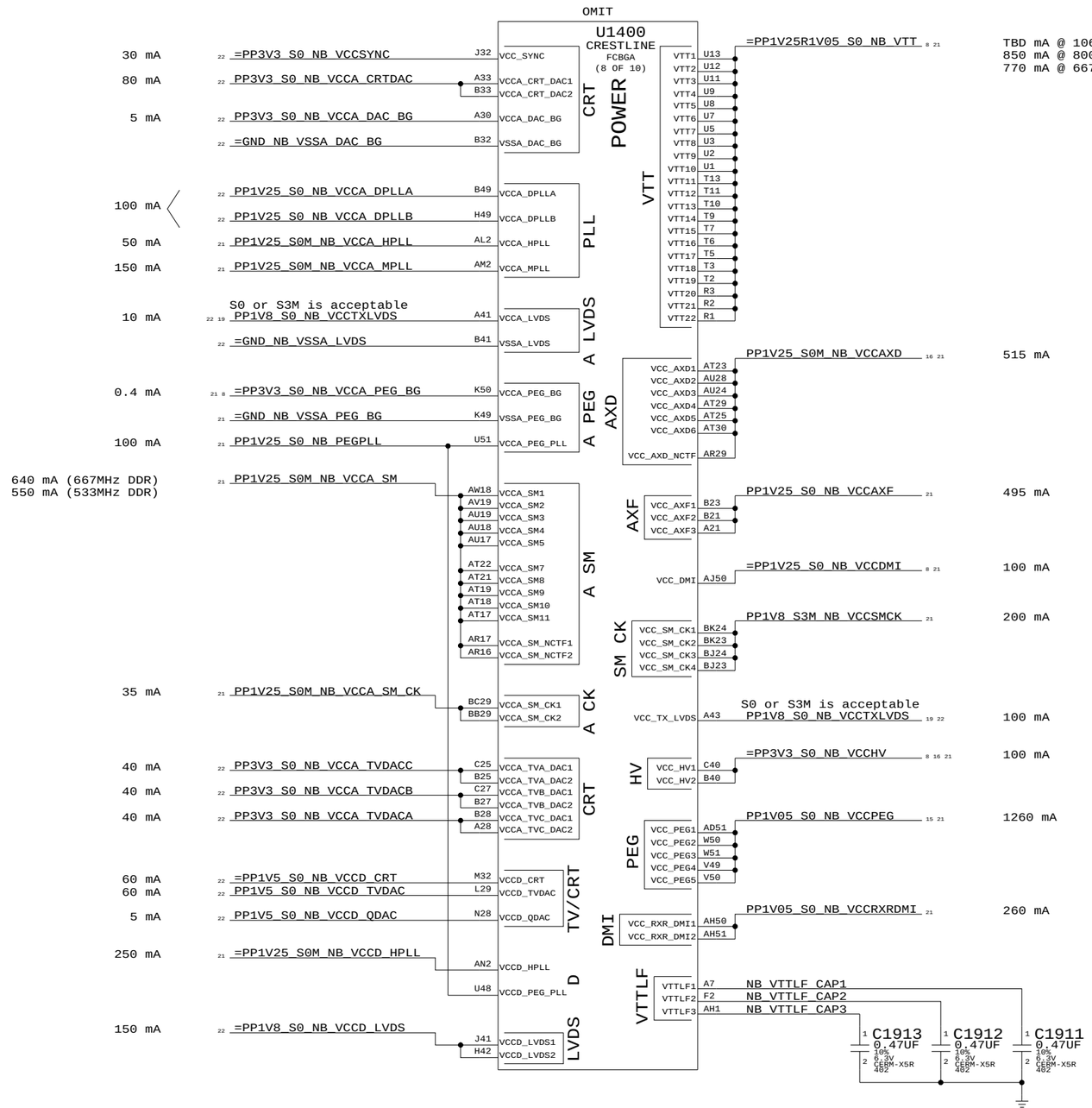
NB DDR2 Interfaces

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 17 OF 109	





Current numbers from Crestline EDS, doc #21749.

NB Power 2

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B

SCALE	SHT	OF
NONE	19	109

OMIT

U1400
CRESTLINE
FCBGA
(9 OF 10)
VSS

A13	VSS1	VSS100	AW24
A15	VSS2	VSS101	AW29
A17	VSS3	VSS102	AW32
A24	VSS4	VSS103	AW5
AA21	VSS5	VSS104	AW7
AA24	VSS6	VSS105	AY10
AA29	VSS7	VSS106	AY24
AB20	VSS8	VSS107	AY37
AB23	VSS9	VSS108	AY42
AB26	VSS10	VSS109	AY43
AB28	VSS11	VSS110	AY45
AB31	VSS12	VSS111	AY47
AC10	VSS13	VSS112	AY50
AC13	VSS14	VSS113	B10
AC3	VSS15	VSS114	B20
AC39	VSS16	VSS115	B24
AC43	VSS17	VSS116	B29
AC47	VSS18	VSS117	B30
AD1	VSS19	VSS118	B35
AD21	VSS20	VSS119	B38
AD26	VSS21	VSS120	B43
AD29	VSS22	VSS121	B46
AD3	VSS23	VSS122	B5
AD41	VSS24	VSS123	B8
AD45	VSS25	VSS124	BA1
AD49	VSS26	VSS125	BA17
AD5	VSS27	VSS126	BA18
AD50	VSS28	VSS127	BA2
AD8	VSS29	VSS128	BA24
AE10	VSS30	VSS129	BB12
AE14	VSS31	VSS130	BB25
AE6	VSS32	VSS131	BB40
AF20	VSS33	VSS132	BB44
AF23	VSS34	VSS133	BB49
AF24	VSS35	VSS134	BB8
AF31	VSS36	VSS135	BC16
AG2	VSS37	VSS136	BC24
AG38	VSS38	VSS137	BC25
AG43	VSS39	VSS138	BC36
AG47	VSS40	VSS139	BC40
AG50	VSS41	VSS140	BC51
AH3	VSS42	VSS141	BD13
AH40	VSS43	VSS142	BD2
AH41	VSS44	VSS143	BD28
AH7	VSS45	VSS144	BD45
AH9	VSS46	VSS145	BD48
AJ11	VSS47	VSS146	BD5
AJ13	VSS48	VSS147	BE1
AJ21	VSS49	VSS148	BE19
AJ24	VSS50	VSS149	BE23
AJ29	VSS51	VSS150	BE30
AJ32	VSS52	VSS151	BE42
AJ43	VSS53	VSS152	BE51
AJ45	VSS54	VSS153	BE8
AJ49	VSS55	VSS154	BF12
AK20	VSS56	VSS155	BF16
AK21	VSS57	VSS156	BF36
AK26	VSS58	VSS157	BG19
AK28	VSS59	VSS158	BG2
AK31	VSS60	VSS159	BG24
AK51	VSS61	VSS160	BG29
AL1	VSS62	VSS161	BG39
AM11	VSS63	VSS162	BG48
AM13	VSS64	VSS163	BG5
AM3	VSS65	VSS164	BG51
AM4	VSS66	VSS165	BH17
AM41	VSS67	VSS166	BH30
AM45	VSS68	VSS167	BH44
AN1	VSS69	VSS168	BH46
AN38	VSS70	VSS169	BH8
AN39	VSS71	VSS170	BJ11
AN43	VSS72	VSS171	BJ13
AN5	VSS73	VSS172	BJ38
AN7	VSS74	VSS173	BJ4
AP4	VSS75	VSS174	BJ42
AP48	VSS76	VSS175	BJ46
AP50	VSS77	VSS176	BK15
AR11	VSS78	VSS177	BK17
AR2	VSS79	VSS178	BK25
AR39	VSS80	VSS179	BK29
AR44	VSS81	VSS180	BK36
AR47	VSS82	VSS181	BK40
AR7	VSS83	VSS182	BK44
AT10	VSS84	VSS183	BK6
AT14	VSS85	VSS184	BK8
AT41	VSS86	VSS185	BL11
AT49	VSS87	VSS186	BL13
AU1	VSS88	VSS187	BL19
AU23	VSS89	VSS188	BL22
AU29	VSS90	VSS189	BL37
AU3	VSS91	VSS190	BL47
AU36	VSS92	VSS191	C12
AU49	VSS93	VSS192	C16
AU51	VSS94	VSS193	C19
AV39	VSS95	VSS194	C28
AV48	VSS96	VSS195	C29
AW1	VSS97	VSS196	C33
AW12	VSS98	VSS197	C36
AW16	VSS99	VSS198	C41

OMIT

U1400
CRESTLINE
FCBGA
(10 OF 10)
VSS

C46	VSS199	VSS287	W11
C50	VSS200	VSS288	W39
C7	VSS201	VSS289	W43
D13	VSS202	VSS290	W47
D24	VSS203	VSS291	W5
D3	VSS204	VSS292	W7
D32	VSS205	VSS293	Y13
D39	VSS206	VSS294	Y2
D45	VSS207	VSS295	Y41
D49	VSS208	VSS296	Y45
E10	VSS209	VSS297	Y49
E16	VSS210	VSS298	Y5
E24	VSS211	VSS299	Y50
E28	VSS212	VSS300	Y11
E32	VSS213	VSS301	P29
E47	VSS214		
F19	VSS215		
F36	VSS216	TDE_SENSE VSS302	T29
F4	VSS217		
F40	VSS218		
F50	VSS219	TDE_FORCE VSS303	T31
G1	VSS220		
G13	VSS221		
G16	VSS222	TDB_FORCE VSS304	T33
G19	VSS223		
G24	VSS224		
G28	VSS225	TDB_SENSE VSS305	R28
G29	VSS226		
G33	VSS227		
G42	VSS228		
G45	VSS229	VSS306	AA32
G48	VSS230	VSS307	AB32
G8	VSS231	VSS308	AD32
H24	VSS232	VSS309	AF28
H28	VSS233	VSS310	AF29
H4	VSS234	VSS311	AT27
H45	VSS235	VSS312	AV25
J11	VSS236	VSS313	H50
J16	VSS237		
J2	VSS238		
J24	VSS239		
J28	VSS240		
J33	VSS241		
J35	VSS242		
J39	VSS243		
K12	VSS245		
K47	VSS246		
K8	VSS247		
L1	VSS248		
L17	VSS249		
L20	VSS250		
L24	VSS251		
L28	VSS252		
L3	VSS253		
L33	VSS254		
L49	VSS255		
M28	VSS256		
M42	VSS257		
M46	VSS258		
M49	VSS259		
M5	VSS260		
M50	VSS261		
M9	VSS262		
N11	VSS263		
N14	VSS264		
N17	VSS265		
N29	VSS266		
N32	VSS267		
N36	VSS268		
N39	VSS269		
N44	VSS270		
N49	VSS271		
N7	VSS272		
P19	VSS273		
P2	VSS274		
P23	VSS275		
P3	VSS276		
P50	VSS277		
R49	VSS278		
T39	VSS279		
T43	VSS280		
T47	VSS281		
U41	VSS282		
U45	VSS283		
U50	VSS284		
V2	VSS285		
V3	VSS286		

Crestline Thermal Diode Pins

Mainly for investigation. If not used, alias these nets directly to GND.

TDE_SENSE T29 =NB_TDE_SENSE 51

NOTE: TDE = _P

TDE_FORCE T31 =NB_TDE_FORCE 51

TDB_FORCE T33 =NB_TDB_FORCE 51

NOTE: TDB = _N

TDB_SENSE R28 =NB_TDB_SENSE 51

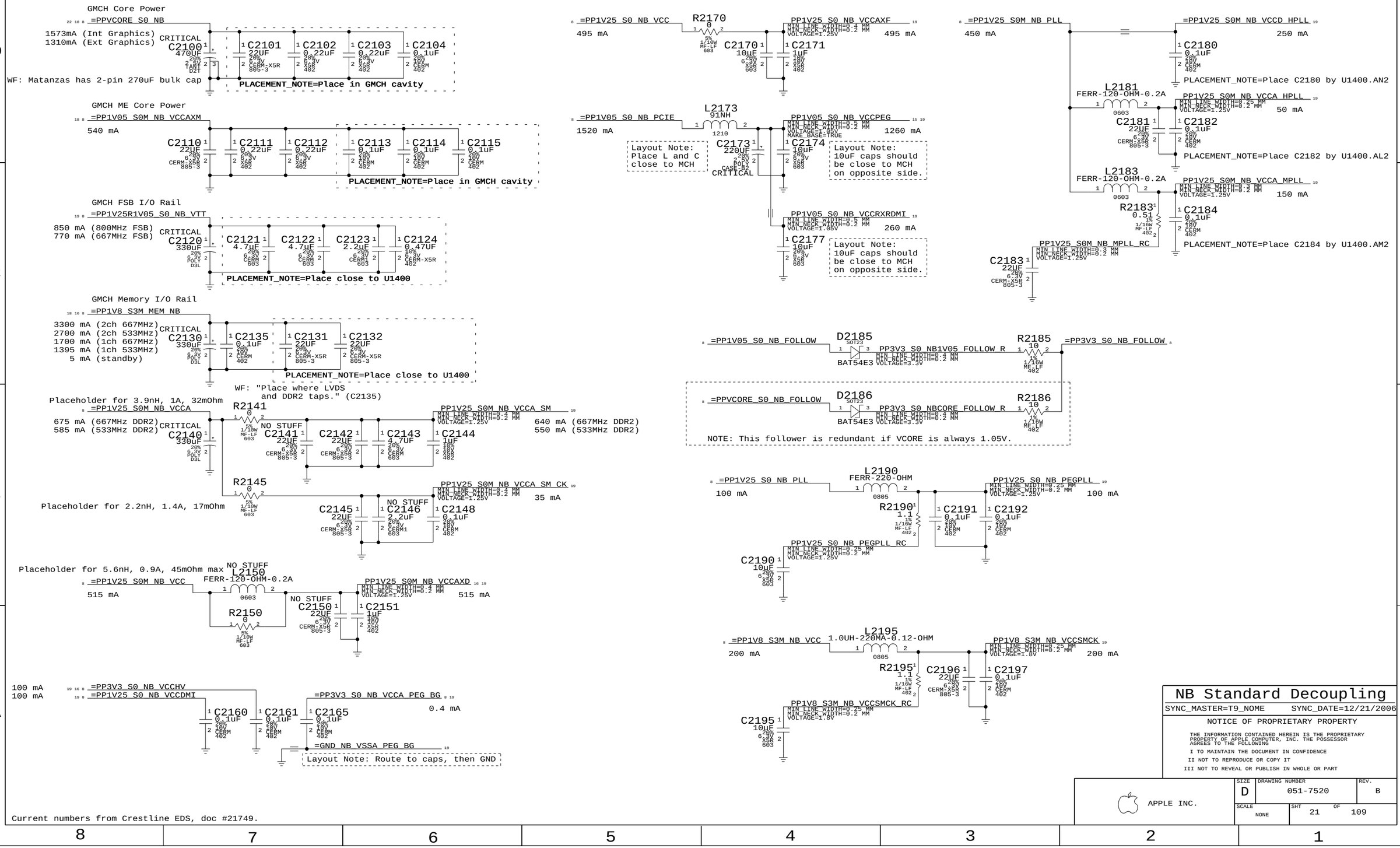
NB Grounds

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

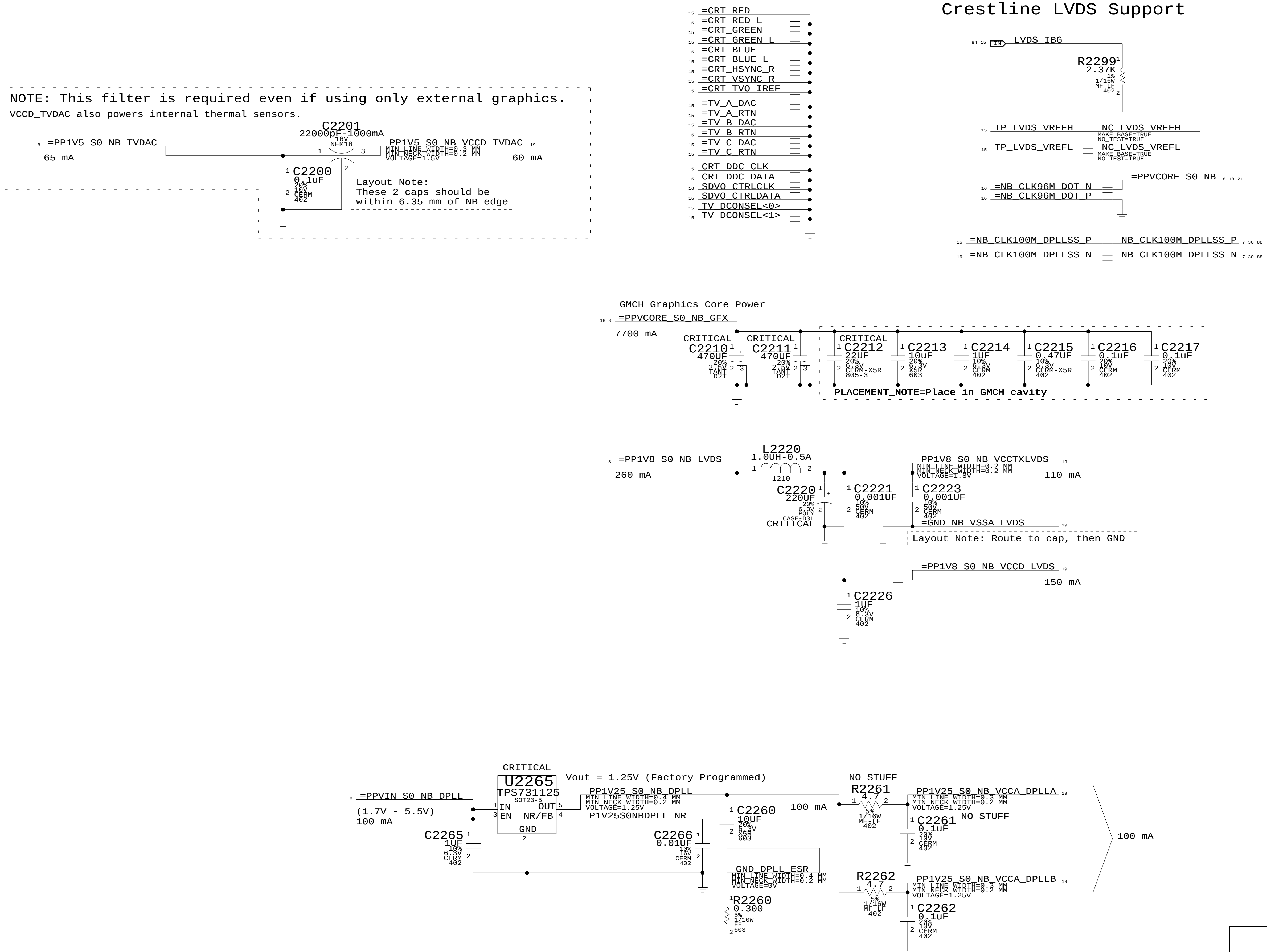
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B

SCALE	SHT	OF
NONE	20	109



Crestline LVDS Support



NOTE: This filter is required even if using only external graphics.
VCCD_TVDAC also powers internal thermal sensors.
=PP1V5_S0_NB_TVDAC
65 mA
C2201
22000pF-1000mA
16V
NFM18
PP1V5_S0_NB_VCCD_TVDAC
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
60 mA
C2200
0.1uF
20%
10V
CERM
402
Layout Note:
These 2 caps should be
within 6.35 mm of NB edge
=CRT_RED
=CRT_RED_L
=CRT_GREEN
=CRT_GREEN_L
=CRT_BLUE
=CRT_BLUE_L
=CRT_HSYNC_R
=CRT_VSYNC_R
=CRT_TVO_IREF
=TV_A_DAC
=TV_A_RTN
=TV_B_DAC
=TV_B_RTN
=TV_C_DAC
=TV_C_RTN
CRT_DDC_CLK
CRT_DDC_DATA
SDVO_CTRLCLK
SDVO_CTRLDATA
TV_DCONSEL<0>
TV_DCONSEL<1>
LVDS_IBG
R2299
2.37K
1%
1/16W
MF-LF
402
TP_LVDS_VREFH
NC_LVDS_VREFH
MAKE_BASE=TRUE
NO_TEST=TRUE
TP_LVDS_VREFL
NC_LVDS_VREFL
MAKE_BASE=TRUE
NO_TEST=TRUE
=PPVCORE_S0_NB
=NB_CLK96M_DOT_N
=NB_CLK96M_DOT_P
=NB_CLK100M_DPLLSS_P
NB_CLK100M_DPLLSS_P
=NB_CLK100M_DPLLSS_N
NB_CLK100M_DPLLSS_N
=PP1V5_S0_NB_VCCD_CRT
PP3V3_S0_NB_VCCA_CRTDAC
=PP3V3_S0_NB_VCCSYNC
PP1V5_S0_NB_VCCD_QDAC
PP3V3_S0_NB_VCCA_DAC_BG
=GND_NB_VSSA_DAC_BG
PP3V3_S0_NB_VCCA_TVDACA
PP3V3_S0_NB_VCCA_TVDACB
PP3V3_S0_NB_VCCA_TVDACC
GMCH Graphics Core Power
=PPVCORE_S0_NB_GFX
7700 mA
CRITICAL
C2210
470UF
20%
2.5V
TANT
D2T
CRITICAL
C2211
470UF
20%
2.5V
TANT
D2T
CRITICAL
C2212
22UF
20%
6.3V
CERM-X5R
805-3
C2213
10uF
20%
6.3V
X5R
603
C2214
1UF
10%
6.3V
CERM
402
C2215
0.47UF
10%
6.3V
CERM-X5R
402
C2216
0.1uF
20%
10V
CERM
402
C2217
0.1uF
20%
10V
CERM
402
PLACEMENT_NOTE=Place in GMCH cavity
=PP1V8_S0_NB_LVDS
260 mA
L2220
1.0UH-0.5A
1210
PP1V8_S0_NB_VCCTXLVDS
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
110 mA
C2220
220UF
20%
6.3V
POLY
CASE-D3L
CRITICAL
C2221
0.001UF
10%
50V
CERM
402
C2223
0.001UF
10%
50V
CERM
402
=GND_NB_VSSA_LVDS
Layout Note: Route to cap, then GND
=PP1V8_S0_NB_VCCD_LVDS
150 mA
C2226
1UF
10%
6.3V
CERM
402
CRITICAL
U2265
TPS731125
SOT23-5
IN
EN
OUT
NR/FB
GND
Vout = 1.25V (Factory Programmed)
=PPVIN_S0_NB_DPLL
(1.7V - 5.5V)
100 mA
C2265
1UF
10%
6.3V
CERM
402
PP1V25_S0_NB_DPLL
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
P1V25S0NBDPLL_NR
C2260
10UF
20%
6.3V
X5R
603
100 mA
C2266
0.01UF
10%
16V
CERM
402
GND_DPLL_ESR
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0V
R2260
0.300
5%
1/10W
FF
603
NO STUFF
R2261
4.7
5%
1/16W
MF-LF
402
PP1V25_S0_NB_VCCA_DPLLA
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
C2261
0.1uF
20%
10V
CERM
402
NO STUFF
R2262
4.7
5%
1/16W
MF-LF
402
PP1V25_S0_NB_VCCA_DPLLB
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
C2262
0.1uF
20%
10V
CERM
402
100 mA

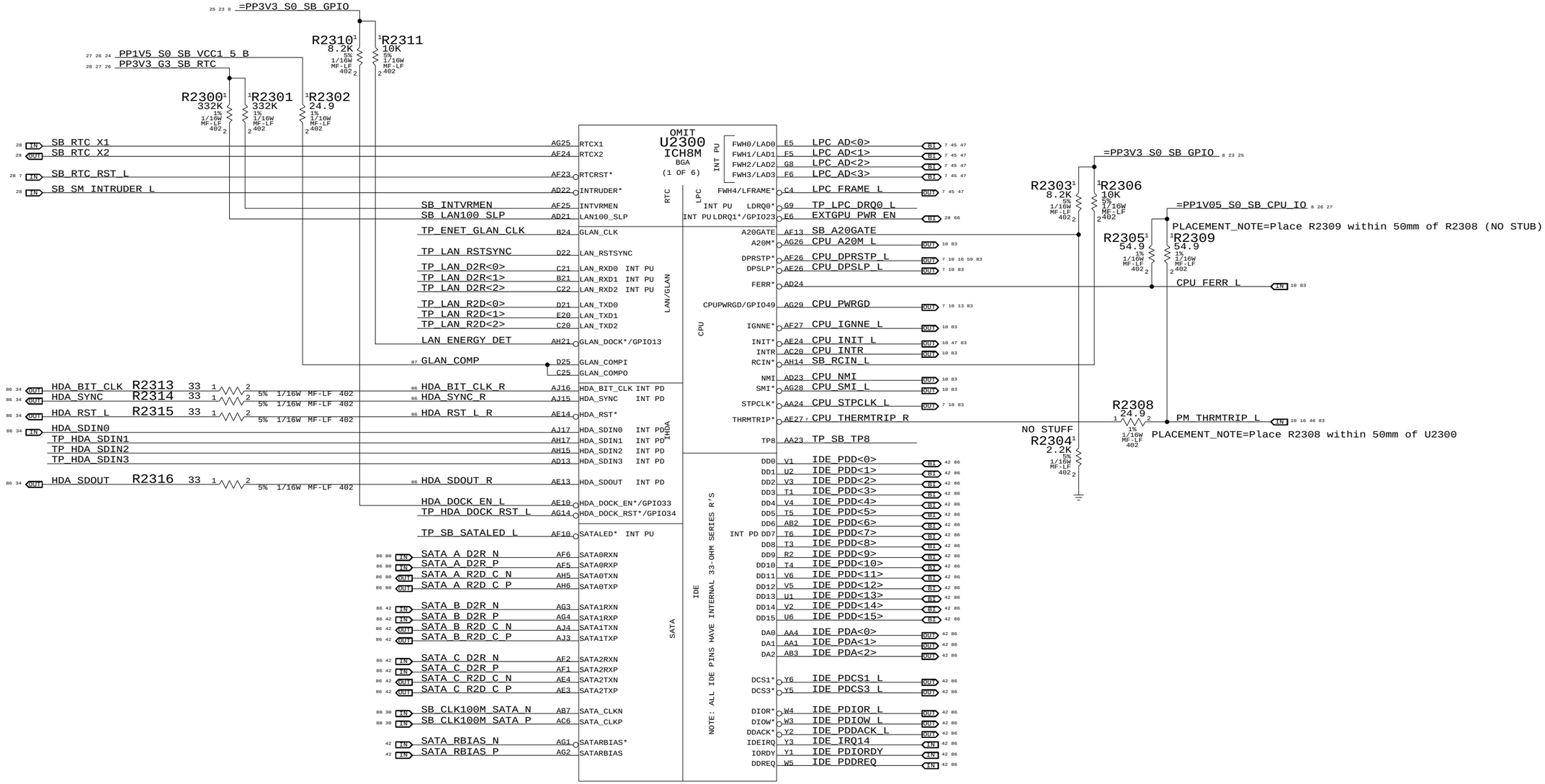
Current numbers from Crestline EDS Addendum, doc #20127.

NB Graphics Decoupling

SYNC_MASTER=M75_MLB SYNC_DATE=03/20/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE NONE	SHT 22	OF 109



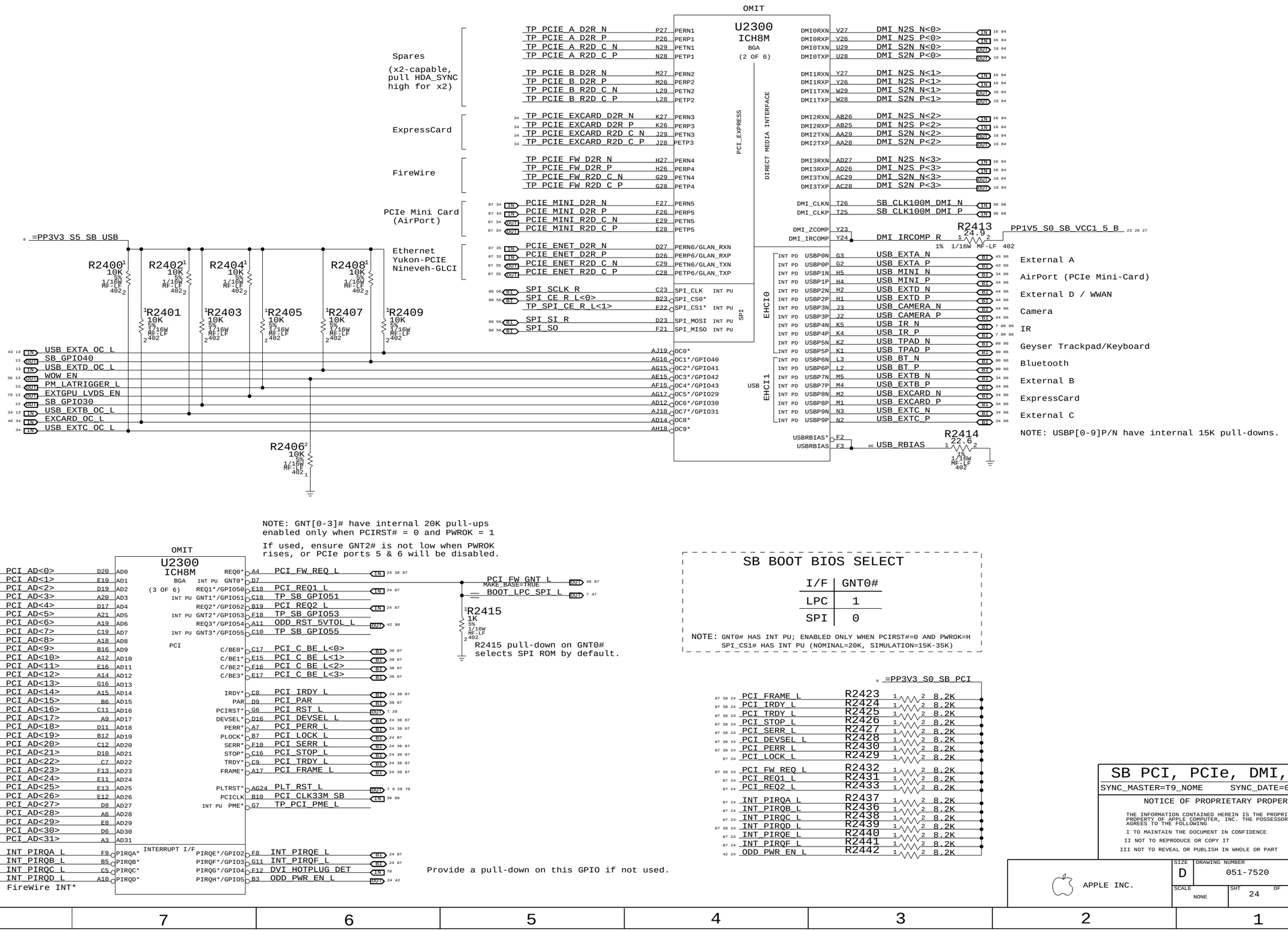
	HDA
HDA_BIT_CLK	24.000MHZ CLOCK W/INTERNAL WEAK PD
HDA_RST#	
HDA_SDIN[0-2]	INTEGRATED PDs
HDA_SDOUT	INTEGRATED PD
ACZ_SYNC	INTEGRATED PD

SB Enet, Disk, FSB, LPC

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 23 OF 109	



=PP3V3_S0_SB_GPIO
=PP3V3_S5_SB_GPIO

NO_REBOOT_MODE

R2500 1K 5% 1/16W MF-LF 402
R2551 8.2K 5% 1/16W MF-LF 402
R2553 8.2K 5% 1/16W MF-LF 402
R2504 10K 5% 1/16W MF-LF 402
R2506 10K 5% 1/16W MF-LF 402
R2510 1K 5% 1/16W MF-LF 402

R2502 10K 5% 1/16W MF-LF 402
R2550 10K 5% 1/16W MF-LF 402
R2552 10K 5% 1/16W MF-LF 402
R2547 10K 5% 1/16W MF-LF 402
R2505 8.2K 5% 1/16W MF-LF 402
R2507 8.2K 5% 1/16W MF-LF 402

R2532 10K 5% 1/16W MF-LF 402
R2535 10K 5% 1/16W MF-LF 402
R2533 10K 5% 1/16W MF-LF 402
R2534 10K 5% 1/16W MF-LF 402

OMIT
U2300
ICH8M
BGA
(4 OF 6)

SMB
- SMB_CLK — AJ26 SMBCLK
- SMB_DATA — AD19 SMBDATA
- TP_CLINK_WLAN_RESET_L — AG21 LINKALERT*
- SMB_ME_CLK — AC17 SMLINK0
- SMB_ME_DATA — AE19 SMLINK1

CLOCKS
- PM_RI_L — AF17 RI*
- PM_SUS_STAT_L — F4 SUS_STAT*/LPCPD*
- PM_SYSRST_L — AD15 SYS_RESET*

SYS GPIO
- PM_BMBUSY_L — AG12 BMBUSY*/GPIO0
- LINDACARD_GPIO — AG22 SMBALERT*/GPIO11
- PM_STPPCI_L — AE20 STP_PCI*/GPIO15
- PM_STPCPU_L — AG18 STP_CPU*/GPIO25
- PM_CLKRUN_L — AH11 CLKRUN*/GPIO32
- PCIE_WAKE_L — AE17 WAKE*
- INT_SERIRQ — AF12 SERIRQ
- PM_THRM_L — AC13 THRM*
- VR_PWRGD_CLKEN — AJ20 VRMPWRGD
- TP_SB_TP7 — AJ22 TP7

GPIO
- PCI_PME_FW_L — AJ8 TACH1/GPIO1
- SB_GPIO6 — AJ9 TACH2/GPIO6
- AH9 TACH3/GPIO7
- AE16 GPIO8
- LAN_PHYPC — AC19 GPIO12
- EXTGPU_RST_L — AG8 TACH0/GPIO17
- SB_GPIO18 — AH12 GPIO18
- TP_SB_GPIO20 — AE11 GPIO20 INT PD
- SB_SCLOCK — AG10 SCLOCK/GPIO22
- SATA_B_PWR_EN_L — AH25 QRT_STATE0/GPIO27
- FWH_MFG_MODE — AD16 QRT_STATE1/GPIO28
- SB_SATA_CLKREQ_L — AG13 SATACLKREQ*/GPIO35
- SB_SLOAD — AF9 SLOAD/GPIO38
- SB_SDATAOUT<0> — AJ11 SDATAOUT0/GPIO39
- SB_SDATAOUT<1> — AD10 SDATAOUT1/GPIO48

MISC
- SB_SPKR — AD9 SPKR INT PD
- NB_SB_SYNC_L — AJ13 MCH_SYNC*
- TP_SB_TP3 — AJ21 TP3 INT PU

Test access required for XOR chain testing.

SATA GPIO
- SATA0GP/GPIO21 — AJ12 — RSVD_EXTGPU_LVDS_EN
- SATA1GP/GPIO19 — AJ10 — SATA_B_DET_L
- SATA2GP/GPIO36 — AF11 — SB_GPIO36
- SATA3GP/GPIO37 — AG11 — SB_CRT_TVOUT_MUX_L

CLOCKS
- CLK14 — AG9 — SB_CLK14P3M_TIMER
- CLK48 — G5 — SB_CLK48M_USBCTLR
- SUSCLK — D3 — SUS_CLK_SB

POWER MGT
- SLP_S3* — AG23 — PM_SLP_S3_L
- SLP_S4* — AF21 — TP_PM_SLP_S4_L
- SLP_S5* — AD18 — PM_SLP_S5_L
- S4_STATE*/GPIO26 — AH27 — PM_S4_STATE_L
- PWROK — AE23 — PM_SB_PWROK
- DPRSLPVR/GPIO16 — AJ14 — PM_DPRSLPVR
- BATLOW* — AE21 — PM_BATLOW_L
- INT PU PWRBTN* — C2 — PM_PWRBTN_L
- LAN_RST* — AH20 — PM_LAN_ENABLE
- RSMRST* — AG27 — PM_RSMRST_L
- CK_PWRGD — E1 — CLK_PWRGD
- CLPWROK — E3 — See note below =SB_CLINK_MPWROK
- SLP_M* — AJ25 — TP_PM_SLP_M_L

CONTROLLER LINK
- CL_CLK0 — F23 — CLINK_NB_CLK
- CL_CLK1 — AE18 — TP_CLINK_WLAN_CLK
- CL_DATA0 — F22 — CLINK_NB_DATA
- CL_DATA1 — AF19 — TP_CLINK_WLAN_DATA
- CL_VREF0 — D24 — SB_CLINK_VREF0
- CL_VREF1 — AH23 — SB_CLINK_VREF1
- INT PU CL_RST* — AJ23 — CLINK_NB_RESET_L
- MEM_LED/GPIO24 — AJ27 — ARB_DETECT_L
- ME_EC_ALERT/GPIO10 — AJ24 — SB_GPIO10_CL1
- EC_ME_ALERT/GPIO14 — AF22 — SB_GPIO14_CL2
- WOL_EN/GPIO9 — AG19 — WOL_EN

NOTE: DPRSLPVR HAS INT 20K PD ENABLED AT BOOT/RESET FOR STRAPPING FUNCTION

PM_LAN_ENABLE must remain deasseted until VccCL3_3, VccLAN3_3 and VccLAN1_05 have been up for at least 1ms.

R2524 100K 5% 1/16W MF-LF 402
R2525 10K 5% 1/16W MF-LF 402

R2523 100K 5% 1/16W MF-LF 402

NOTE: ICH CLPWROK input must be PWRGD signal for PP3V3_S0M, PP3V3_S0MWOL, PP1V8_S3M, PP1V25_S0M, PP1V05_S0M, PP0V9_S3M and PP0V9_S0M. If ME/AMT is not used, short CLPWROK to PWROK.

=PP3V3_S0MWOL_SB_CLINK0
R2526 3.24K 1% 1/16W MF-LF 402
C2500 0.1uF 10% 16V X5R 402
R2527 453 1% 1/16W MF-LF 402

=PP3V3_S5_SB_CLINK1
R2528 32.4K 1% 1/16W MF-LF 402
C2501 0.1uF 10% 16V X5R 402
R2529 4.53K 1% 1/16W MF-LF 402

=PP3V3_S5_SB
- R2511 10K 5% 1/16W MF-LF 402
- R2515 10K 5% 1/16W MF-LF 402
- R2514 100K 5% 1/16W MF-LF 402 — LINDACARD_GPIO, ARB_DETECT_L, FWH_MFG_MODE
- NOSTUFF R2512 0 5% 1/16W MF-LF 402
- ARB_ONLY R2516 0 5% 1/16W MF-LF 402

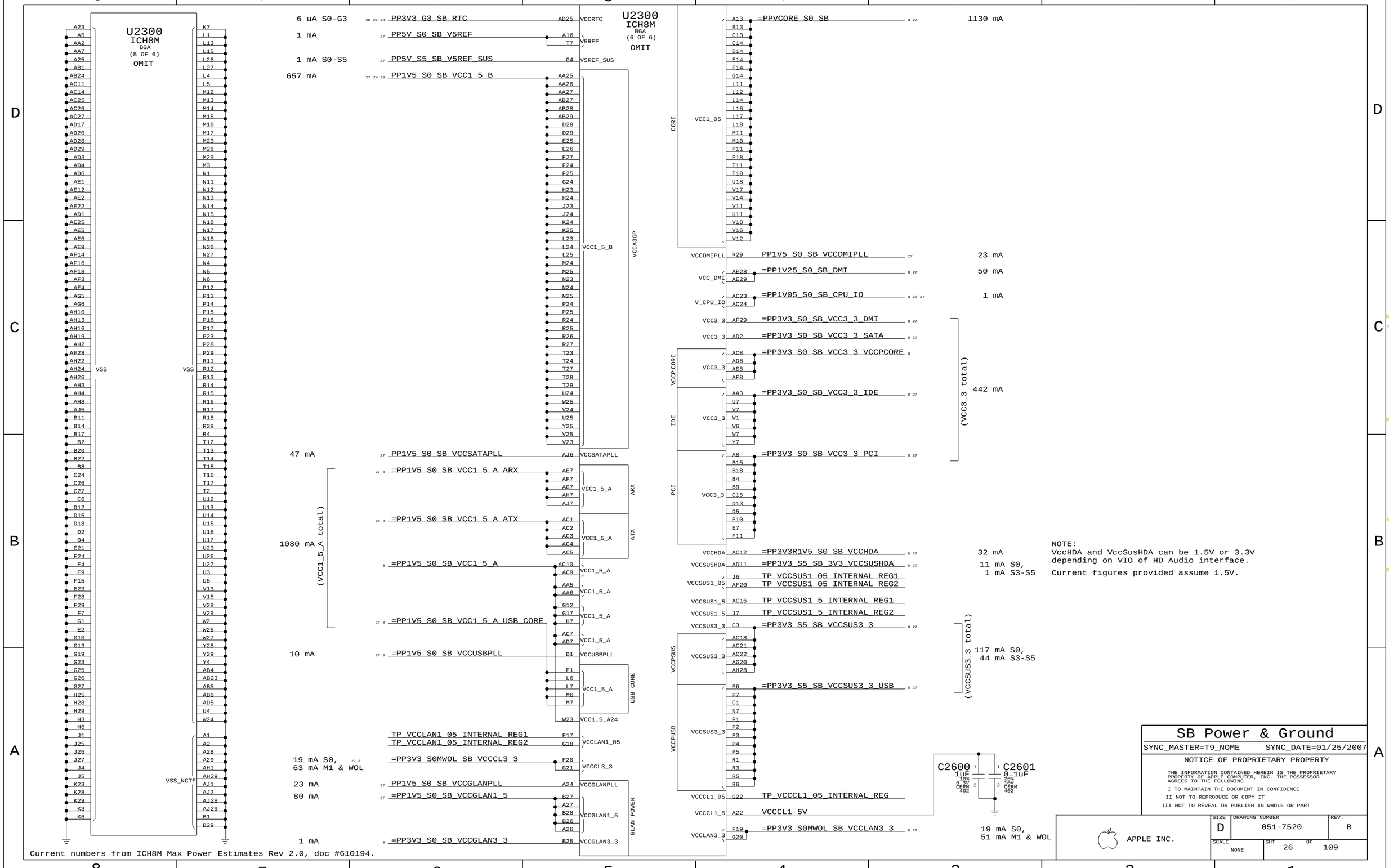
- SATA_B_PWR_EN_L — R2530 10K 1% 1/16W MF-LF 402 — =PP3V3_S0_SB_GPIO
- PCI_PME_FW_L — R2531 10K 1% 1/16W MF-LF 402
- SB_GPIO6 — R2596 10K 1% 1/16W MF-LF 402
- EXTGPU_RST_L — R2597 10K 1% 1/16W MF-LF 402
- PM_RI_L — R2536 10K 1% 1/16W MF-LF 402 — =PP3V3_S5_SB
- PM_BATLOW_L — R2544 8.2K 5% 1/16W MF-LF 402
- LAN_PHYPC — R2545 10K 1% 1/16W MF-LF 402
- SB_GPIO10_CL1 — R2598 10K 1% 1/16W MF-LF 402
- SB_GPIO14_CL2 — R2546 10K 1% 1/16W MF-LF 402

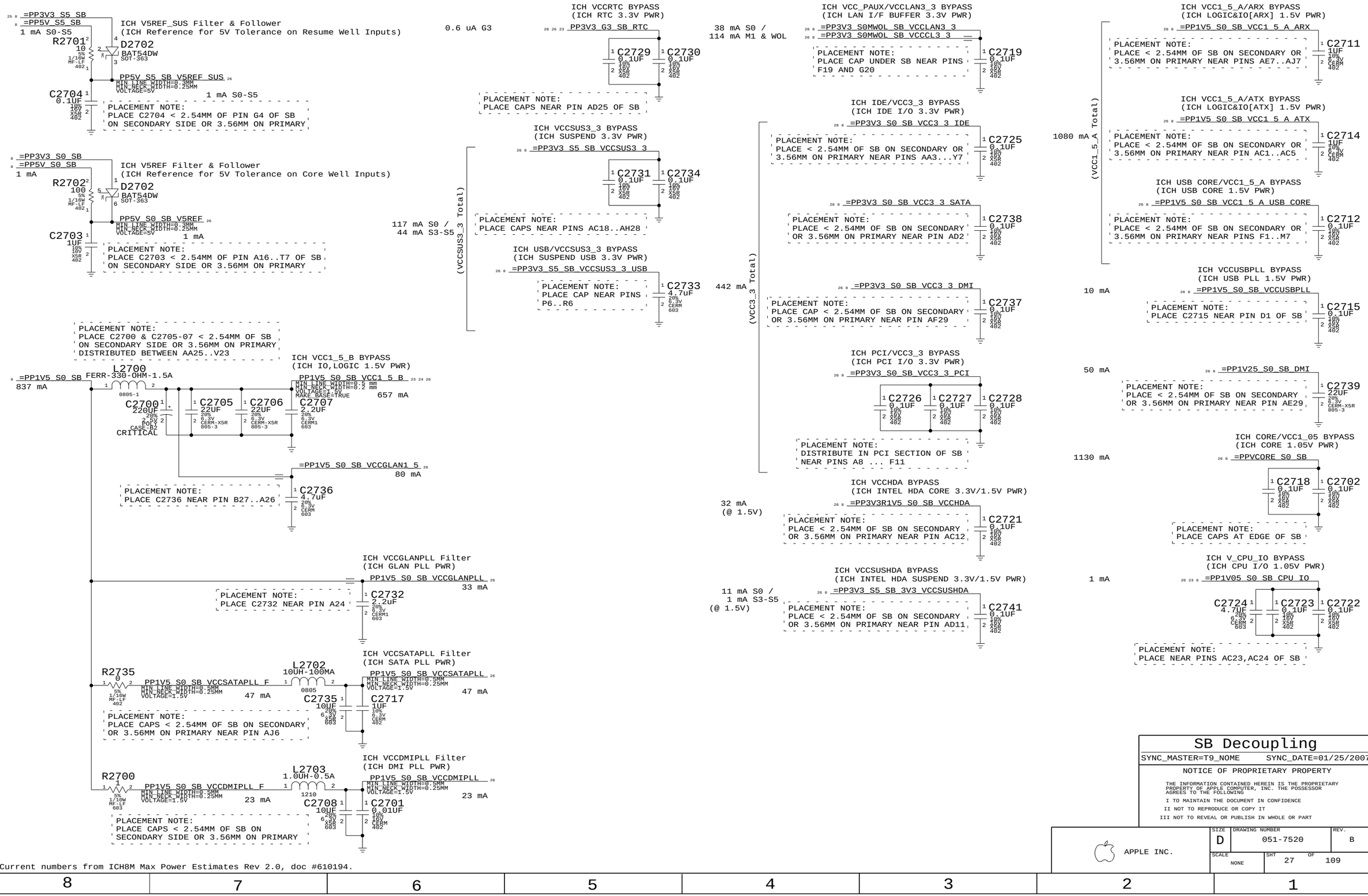
SB Pwr Mgt, GPIO, Clink

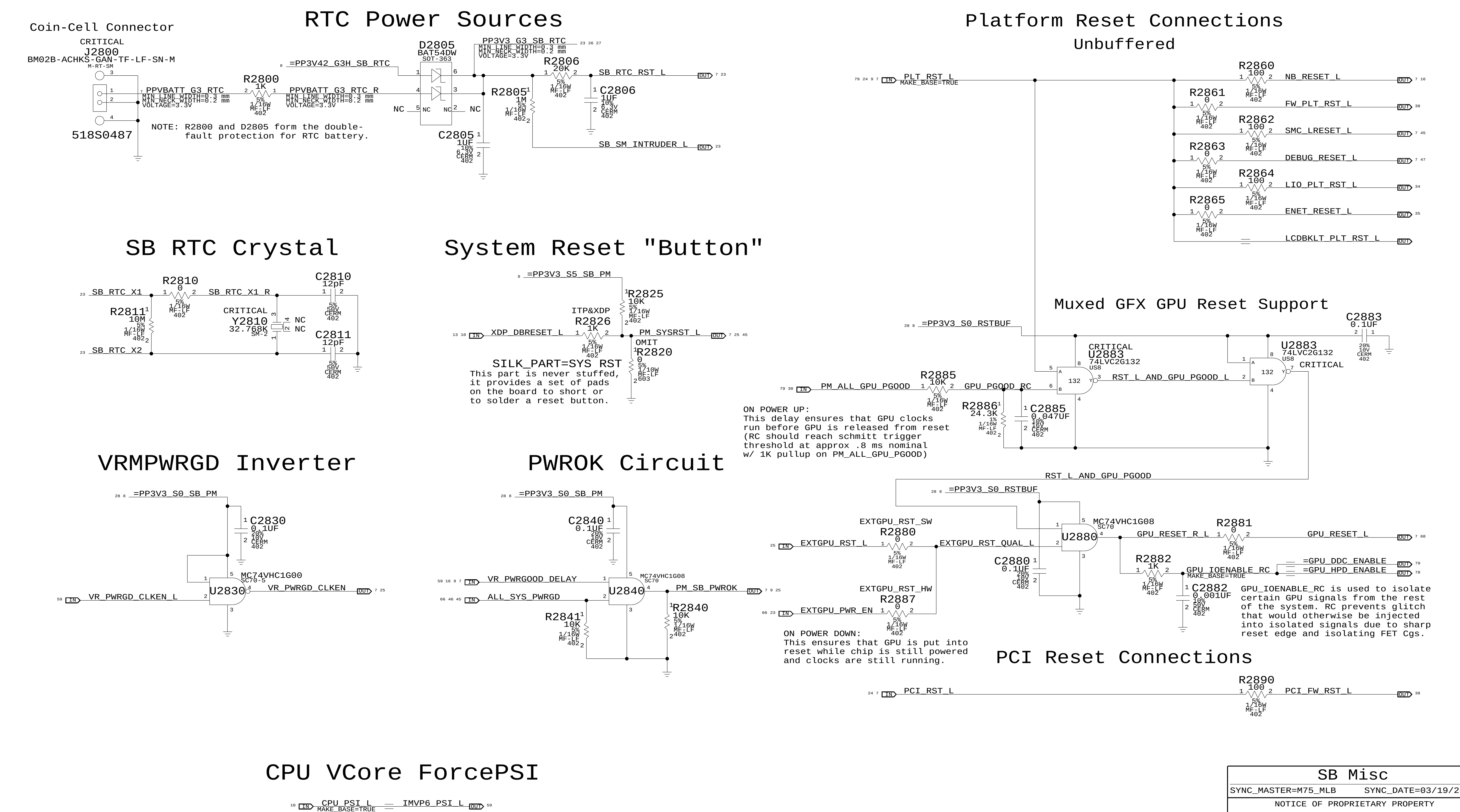
SYNC_MASTER=M75_MLB SYNC_DATE=04/02/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 25 OF 109	





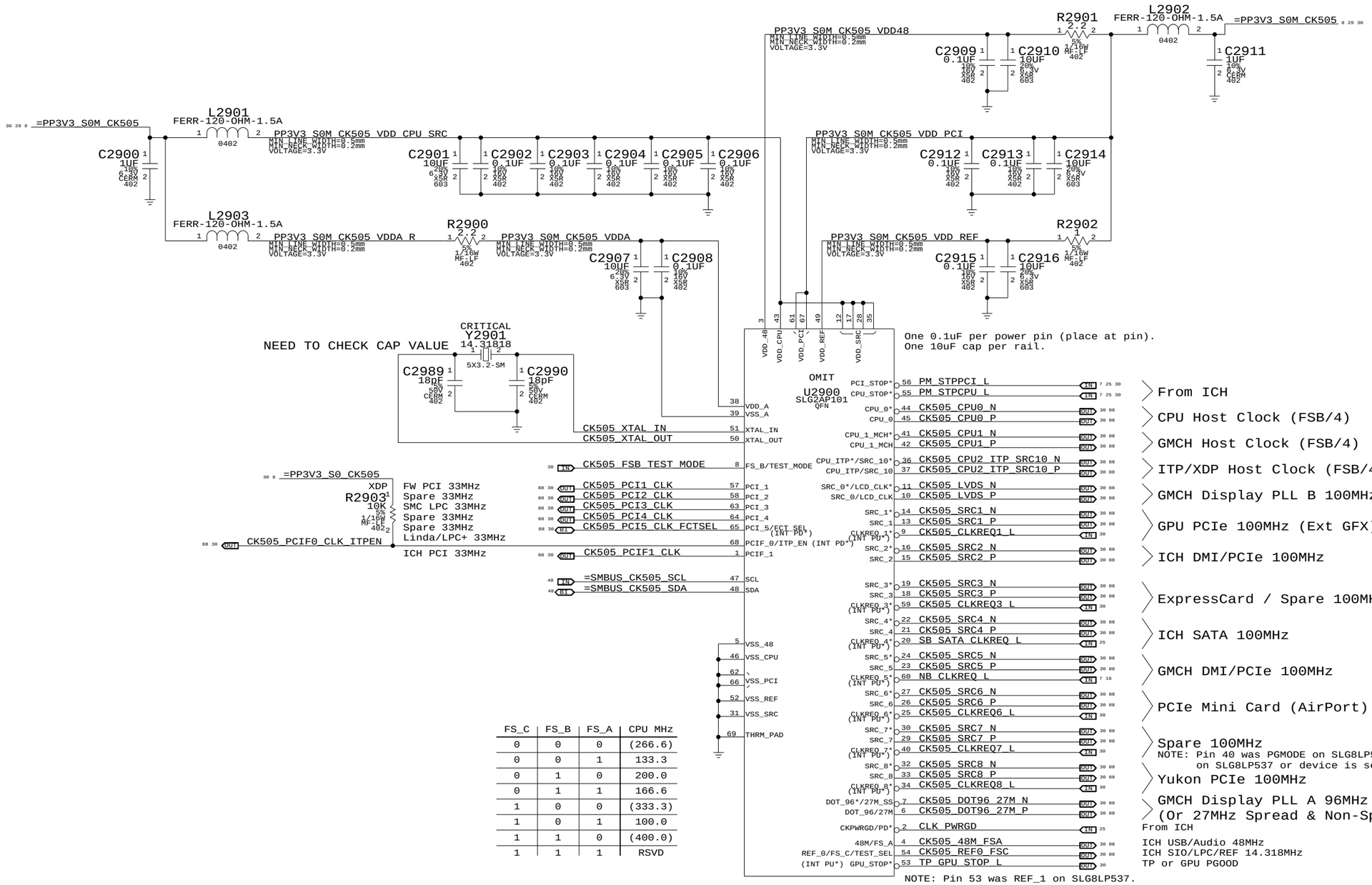

RTC Power Sources
Coin-Cell Connector
CRITICAL
J2800
BM02B-ACHKS-GAN-TF-LF-SN-M
518S0487
PPVBATT_G3_RTC
R2800
1K
PPVBATT_G3_RTC_R
=PP3V42_G3H_SB_RTC
D2805
BAT54DW
SOT-363
PP3V3_G3_SB_RTC
R2806
20K
SB_RTC_RST_L
C2806
1UF
R2805
1M
C2805
1UF
SB_SM_INTRUDER_L
NOTE: R2800 and D2805 form the double-fault protection for RTC battery.
Platform Reset Connections
Unbuffered
PLT_RST_L
MAKE_BASE=TRUE
R2860 100 NB_RESET_L
R2861 0 FW_PLT_RST_L
R2862 100 SMC_LRESET_L
R2863 0 DEBUG_RESET_L
R2864 100 LIO_PLT_RST_L
R2865 0 ENET_RESET_L
LCDBKLT_PLT_RST_L
SB RTC Crystal
SB_RTC_X1
R2810
0
SB_RTC_X1_R
C2810
12pF
R2811
10M
CRITICAL
Y2810
32.768K
SM-2
C2811
12pF
SB_RTC_X2
System Reset "Button"
=PP3V3_S5_SB_PM
R2825
10K
ITP&XDP
R2826
1K
XDP_DBRESET_L
PM_SYSRST_L
OMIT
R2820
0
SILK_PART=SYS RST
This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.
Muxed GFX GPU Reset Support
=PP3V3_S0_RSTBUF
CRITICAL
U2883
74LVC2G132
C2883
0.1UF
R2885
10K
PM_ALL_GPU_PGOOD
GPU_PGOOD_RC
RST_L_AND_GPU_PGOOD_L
R2886
24.3K
C2885
0.047UF
ON POWER UP:
This delay ensures that GPU clocks run before GPU is released from reset (RC should reach schmitt trigger threshold at approx .8 ms nominal w/ 1K pullup on PM_ALL_GPU_PGOOD)
VRMPWRGD Inverter
=PP3V3_S0_SB_PM
C2830
0.1UF
U2830
MC74VHC1G00
SC70-5
VR_PWRGD_CLKEN_L
VR_PWRGD_CLKEN
PWROK Circuit
=PP3V3_S0_SB_PM
C2840
0.1UF
U2840
MC74VHC1G08
SC70
VR_PWRGOOD_DELAY
ALL_SYS_PWRGD
PM_SB_PWROK
R2841
10K
R2840
10K
RST_L_AND_GPU_PGOOD
=PP3V3_S0_RSTBUF
EXTGPU_RST_SW
R2880
0
EXTGPU_RST_L
EXTGPU_RST_QUAL_L
U2880
MC74VHC1G08
SC70
GPU_RESET_R_L
R2881
0
GPU_RESET_L
C2880
0.1UF
EXTGPU_RST_HW
R2887
0
EXTGPU_PWR_EN
R2882
1K
GPU_IOENABLE_RC
MAKE_BASE=TRUE
C2882
0.001UF
=GPU_DDC_ENABLE
=GPU_HPD_ENABLE
GPU_IOENABLE_RC is used to isolate certain GPU signals from the rest of the system. RC prevents glitch into isolated signals due to sharp reset edge and isolating FET Cgs.
ON POWER DOWN:
This ensures that GPU is put into reset while chip is still powered and clocks are still running.
PCI Reset Connections
PCI_RST_L
R2890
100
PCI_FW_RST_L
CPU VCore ForcePSI
CPU_PSI_L
MAKE_BASE=TRUE
IMVP6_PSI_L

SB Misc

SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE NONE	SHT 28	OF 109



FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

FCT_SEL	PIN 6	PIN 7	PIN 10	PIN 11	
0	DOT_96+	DOT_96-	LCD_CLK+	LCD_CLK-	(For Internal Graphics)
1	27M	27M w/SS	SRC_0+	SRC_0-	(For External Graphics)

Clock (CK505)

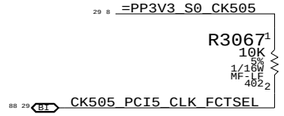
SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

APPLE INC.

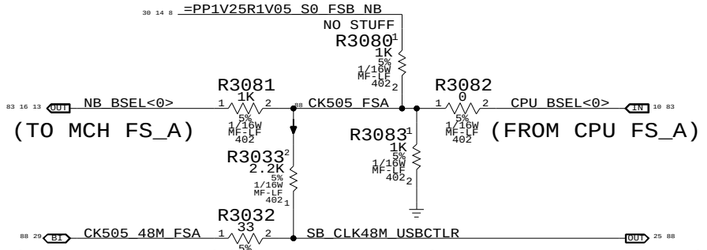
SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 29 OF 109	

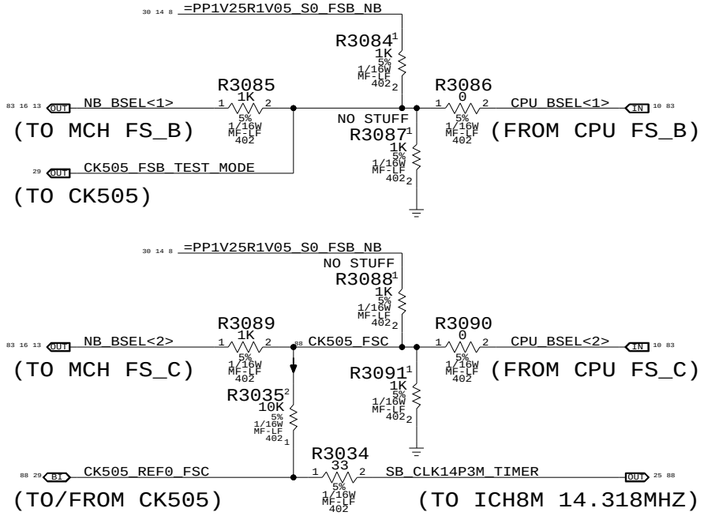
CK505 Configuration Straps

FCT_SEL (GFX clock select)



FS_A, FS_B, FS_C (Host clock freq select)





FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

NO STUFF R3082, R3086 & R3090 for manual CPU clk frequency.

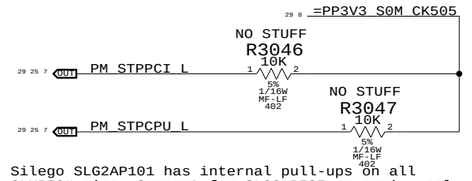
(Only 100-200MHz supported by SLG8LP536 and CY28545-5)

CLK Termination

(Note: HOST/SRC/GFX clock termination removed. Silego SL8GLP536 or equiv. support only)

CK505_CPU0_P	FSB_CLK_CPU_P	(CPU HOST 167/200MHZ)
CK505_CPU0_N	FSB_CLK_CPU_N	
CK505_CPU1_P	FSB_CLK_NB_P	(GMCH HOST 167/200MHZ)
CK505_CPU1_N	FSB_CLK_NB_N	
CK505_CPU2_ITP_SRC10_P	XDP_CLK_P	(ITP HOST 167/200MHZ)
CK505_CPU2_ITP_SRC10_N	XDP_CLK_N	
CK505_LVDS_P	NB_CLK100M_DPLLSS_P	(Int Gfx LVDS 100MHz)
CK505_LVDS_N	NB_CLK100M_DPLLSS_N	
CK505_SRC1_P	PEG_CLK100M_GPU_P	(GPU PCIe 100MHz)
CK505_SRC1_N	PEG_CLK100M_GPU_N	
CK505_SRC2_P	SB_CLK100M_DMI_P	(ICH8M DMI 100MHZ)
CK505_SRC2_N	SB_CLK100M_DMI_N	
CK505_SRC3_P	PCIE_CLK100M_EXCARD_P	(ExpressCard 100MHz)
CK505_SRC3_N	PCIE_CLK100M_EXCARD_N	
CK505_SRC4_P	SB_CLK100M_SATA_P	(ICH8M SATA 100MHZ)
CK505_SRC4_N	SB_CLK100M_SATA_N	
CK505_SRC5_P	NB_CLK100M_PCIE_P	(GMCH PEG/DMI 100MHZ)
CK505_SRC5_N	NB_CLK100M_PCIE_N	
CK505_SRC6_P	PCIE_CLK100M_MINI_P	(WIRELESS PCIe MINI 100MHZ)
CK505_SRC6_N	PCIE_CLK100M_MINI_N	
CK505_SRC7_P	TP_PCIE_CLK100M_SRC7P	(FW 100MHz)
CK505_SRC7_N	TP_PCIE_CLK100M_SRC7N	
CK505_SRC8_P	PCIE_CLK100M_ENET_P	(ENET 100MHZ)
CK505_SRC8_N	PCIE_CLK100M_ENET_N	
CK505_DOT96_27M_P	R3024 33 → GPU_CLK27M	(Ext GFX 27MHz)
CK505_CLK27M		
CK505_DOT96_27M_N	R3025 33 → GPU_CLK27M_SS	(Ext GFX Spread 27MHz)
CK505_CLK27M_SS		
CK505_PCIF0_CLK_ITPEN	R3026 33 → PCI_CLK33M_LPCPLUS	(LINDA/LPC+ LPC 33MHZ)
CK505_PCIF1_CLK	R3027 33 → PCI_CLK33M_SB	(ICH8M PCI 33MHZ)
CK505_PCI1_CLK	R3028 33 → PCI_CLK33M_FW	(FIREWIRE PCI 33MHZ)
CK505_PCI3_CLK	R3030 33 → PCI_CLK33M_SMC	(SMC PCI 33MHZ)

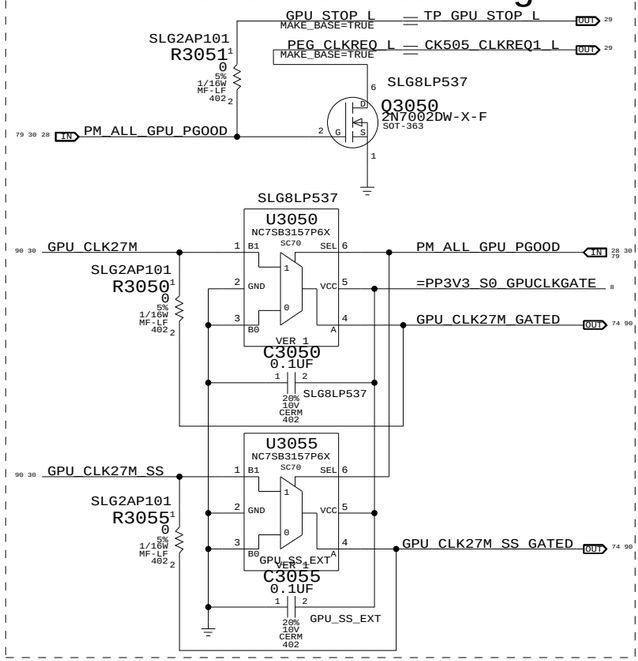
CLKREQ Controls



Silego SLG2AP101 has internal pull-ups on all CLKREQ# pins. Support for SL8GLP537 or equiv. only. NB and SATA CLKREQs are not remappable (and thus are not shown here).

EXCARD_CLKREQ_L	CK505_CLKREQ3_L	
MINI_CLKREQ_L	CK505_CLKREQ6_L	
=ENET_CLKREQ_L	ENET_CLKREQ_L	CK505_CLKREQ8_L
TP_CK505_CLKREQ7_L	CK505_CLKREQ7_L	

GPU Clock Gating



Unused Clocks

CK505_PCI2_CLK	TP_CK505_PCI2_CLK	(Reserved for TPM PCI 33MHZ)
CK505_PCI4_CLK	TP_CK505_PCI4_CLK	(Spare 33MHZ)

Clock Termination

SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 30 OF 109	

Page Notes

Power aliases required by this page:
- =PP1V8_S3M_MEM_A
- =PP0V9_S3M_MEM_DIMMVREFA
- =PPSPD_S0M_MEM_A (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

"Factory" (thru-hole) slot

8 =PP0V9_S3M_MEM_DIMMVREFA

C3101 2.2uF 20% 6.3V CERM 603
C3100 0.1uF 20% 10V CERM 402

91 31 8 =PP1V8_S3M_MEM_A

CRITICAL
J3100
F-RT-TH1
DDR2-SODIMM-DUAL
201

	1B	VREF		VSS0	2B		
	3B	VSS1		DQ4	4B	MEM_A_DQ<9>	17 85
85 17 MEM_A_DQ<14>	5B	DQ0		DQ5	6B	MEM_A_DQ<15>	17 85
85 17 MEM_A_DQ<13>	7B	DQ1		VSS2	8B		
	9B	VSS4		DM0	10B	MEM_A_DM<1>	17 85
85 17 MEM_A_DQS_N<1>	11B	DQS0*		VSS5	12B		
85 17 MEM_A_DQS_P<1>	13B	DQS0		DQ6	14B	MEM_A_DQ<8>	17 85
	15B	VSS6		DQ7	16B	MEM_A_DQ<12>	17 85
85 17 MEM_A_DQ<10>	17B	DQ2		VSS7	18B		
85 17 MEM_A_DQ<11>	19B	DQ3		DQ12	20B	MEM_A_DQ<2>	17 85
	21B	VSS8		DQ13	22B	MEM_A_DQ<3>	17 85
85 17 MEM_A_DQ<7>	23B	DQ8		VSS9	24B		
85 17 MEM_A_DQ<0>	25B	DQ9		DM1	26B	MEM_A_DM<0>	17 85
	27B	VSS10		VSS11	28B		
85 17 MEM_A_DQS_N<0>	29B	DQS1*		CK0	30B	MEM_CLK_P<0>	16 85
85 17 MEM_A_DQS_P<0>	31B	DQS1		CK0*	32B	MEM_CLK_N<0>	16 85
	33B	VSS12		VSS13	34B		
85 17 MEM_A_DQ<6>	35B	DQ10		DQ14	36B	MEM_A_DQ<1>	17 85
85 17 MEM_A_DQ<4>	37B	DQ11		DQ15	38B	MEM_A_DQ<5>	17 85
	39B	VSS14		VSS15	40B		
			KEY				
	41B	VSS16		VSS17	42B		
85 17 MEM_A_DQ<17>	43B	DQ16		DQ20	44B	MEM_A_DQ<18>	17 85
85 17 MEM_A_DQ<21>	45B	DQ17		DQ21	46B	MEM_A_DQ<20>	17 85
	47B	VSS18		VSS19	48B		
85 17 MEM_A_DQS_N<2>	49B	DQS2*		NC0	50B	PM_EXTTS_L<0>	16 45
85 17 MEM_A_DQS_P<2>	51B	DQS2		DM2	52B	MEM_A_DM<2>	17 85
	53B	VSS21		VSS22	54B		
85 17 MEM_A_DQ<23>	55B	DQ18		DQ22	56B	MEM_A_DQ<22>	17 85
85 17 MEM_A_DQ<16>	57B	DQ19		DQ23	58B	MEM_A_DQ<19>	17 85
	59B	VSS23		VSS24	60B		
85 17 MEM_A_DQ<31>	61B	DQ24		DQ28	62B	MEM_A_DQ<26>	17 85
85 17 MEM_A_DQ<27>	63B	DQ25		DQ29	64B	MEM_A_DQ<24>	17 85
	65B	VSS25		VSS26	66B		
85 17 MEM_A_DM<3>	67B	DM3		DQS3*	68B	MEM_A_DQS_N<3>	17 85
NC	69B	NC1		DQS3	70B	MEM_A_DQS_P<3>	17 85
	71B	VSS27		VSS28	72B		
85 17 MEM_A_DQ<30>	73B	DQ26		DQ30	74B	MEM_A_DQ<25>	17 85
85 17 MEM_A_DQ<28>	75B	DQ27		DQ31	76B	MEM_A_DQ<29>	17 85
	77B	VSS29		VSS30	78B		
85 33 16 MEM_CKE<0>	79B	CKE0		NC/CKE1	80B	MEM_CKE<1>	16 33 85
	81B	VDD0		VDD1	82B		
NC	83B	NC2		NC/A15	84B	MEM_A_A<15>	9
85 33 17 MEM_A_BS<2>	85B	BA2		NC/A14	86B	MEM_A_A<14>	16 33 85
	87B	VDD2		VDD3	88B		
85 33 17 MEM_A_A<12>	89B	A12		A11	90B	MEM_A_A<11>	17 33 85
85 33 17 MEM_A_A<9>	91B	A9		A7	92B	MEM_A_A<7>	17 33 85
85 33 17 MEM_A_A<8>	93B	A8		A6	94B	MEM_A_A<6>	17 33 85
	95B	VDD4		VDD5	96B		
85 33 17 MEM_A_A<5>	97B	A5		A4	98B	MEM_A_A<4>	17 33 85
85 33 17 MEM_A_A<3>	99B	A3		A2	100B	MEM_A_A<2>	17 33 85
85 33 17 MEM_A_A<1>	101B	A1		A0	102B	MEM_A_A<0>	17 33 85
	103B	VDD6		VDD7	104B		
85 33 17 MEM_A_A<10>	105B	A10/AP		BA1	106B	MEM_A_BS<1>	17 33 85
85 33 17 MEM_A_BS<0>	107B	BA0		RAS*	108B	MEM_A_RAS_L	17 33 85
85 33 17 MEM_A_WE_L	109B	WE*		S0*	110B	MEM_CS_L<0>	16 33 85
	111B	VDD8		VDD9	112B		
85 33 17 MEM_A_CAS_L	113B	CAS*		ODT0	114B	MEM_ODT<0>	16 33 85
85 33 16 MEM_CS_L<1>	115B	NC/S1*		NC/A13	116B	MEM_A_A<13>	17 33 85
	117B	VDD10		VDD11	118B		
85 33 16 MEM_ODT<1>	119B	NC/ODT1		NC3	120B	NC	
	121B	VSS31		VSS32	122B		
85 17 MEM_A_DQ<36>	123B	DQ32		DQ36	124B	MEM_A_DQ<35>	17 85
85 17 MEM_A_DQ<38>	125B	DQ33		DQ37	126B	MEM_A_DQ<39>	17 85
	127B	VSS33		VSS34	128B		
85 17 MEM_A_DQS_N<4>	129B	DQS4*		DM4	130B	MEM_A_DM<4>	17 85
85 17 MEM_A_DQS_P<4>	131B	DQS4		VSS35	132B		
	133B	VSS36		DQ38	134B	MEM_A_DQ<33>	17 85
85 17 MEM_A_DQ<37>	135B	DQ34		DQ39	136B	MEM_A_DQ<32>	17 85
85 17 MEM_A_DQ<34>	137B	DQ35		VSS37	138B		
	139B	VSS38		DQ44	140B	MEM_A_DQ<63>	17 85
85 17 MEM_A_DQ<56>	141B	DQ40		DQ45	142B	MEM_A_DQ<62>	17 85
85 17 MEM_A_DQ<59>	143B	DQ41		VSS39	144B		
	145B	VSS40		DQS5*	146B	MEM_A_DQS_N<7>	17 85
85 17 MEM_A_DM<7>	147B	DM5		DQS5	148B	MEM_A_DQS_P<7>	17 85
	149B	VSS41		VSS42	150B		
85 17 MEM_A_DQ<58>	151B	DQ42		DQ46	152B	MEM_A_DQ<57>	17 85
85 17 MEM_A_DQ<60>	153B	DQ43		DQ47	154B	MEM_A_DQ<61>	17 85
	155B	VSS43		VSS44	156B		
85 17 MEM_A_DQ<51>	157B	DQ48		DQ52	158B	MEM_A_DQ<55>	17 85
85 17 MEM_A_DQ<54>	159B	DQ49		DQ53	160B	MEM_A_DQ<50>	17 85
	161B	VSS45		VSS46	162B		
NC	163B	NC_TEST		CK1	164B	MEM_CLK_P<1>	16 85
	165B	VSS47		CK1*	166B	MEM_CLK_N<1>	16 85
85 17 MEM_A_DQS_N<6>	167B	DQS6*		VSS48	168B		
85 17 MEM_A_DQS_P<6>	169B	DQS6		DM6	170B	MEM_A_DM<6>	17 85
	171B	VSS49		VSS50	172B		
85 17 MEM_A_DQ<48>	173B	DQ50		DQ54	174B	MEM_A_DQ<49>	17 85
85 17 MEM_A_DQ<53>	175B	DQ51		DQ55	176B	MEM_A_DQ<52>	17 85
	177B	VSS51		VSS52	178B		
85 17 MEM_A_DQ<43>	179B	DQ56		DQ60	180B	MEM_A_DQ<45>	17 85
85 17 MEM_A_DQ<42>	181B	DQ57		DQ61	182B	MEM_A_DQ<40>	17 85
	183B	VSS53		VSS54	184B		
85 17 MEM_A_DM<5>	185B	DM7		DQS7*	186B	MEM_A_DQS_N<5>	17 85
	187B	VSS55		DQS7	188B	MEM_A_DQS_P<5>	17 85
85 17 MEM_A_DQ<46>	189B	DQ58		VSS56	190B		
85 17 MEM_A_DQ<41>	191B	DQ59		DQ62	192B	MEM_A_DQ<44>	17 85
8 =PPSPD_S0M_MEM_A	193B	VSS57		DQ63	194B	MEM_A_DQ<47>	17 85
48 =I2C_SODIMMA_SDA	195B	SDA		VSS58	196B		
48 =I2C_SODIMMA_SCL	197B	SCL		SA0	198B		
	199B	VDDSPD		SA1	200B	ADDR=0xA0(WR)/0xA1(RD)	

516-0140 202

DDR2 Bypass Caps

(For return current)

91 31 8 =PP1V8_S3M_MEM_A

C3108 10UF 20% 6.3V X5R 603
C3109 10UF 20% 6.3V X5R 603
C3110 1UF 10% 6.3V CERM 402
C3111 1UF 10% 6.3V CERM 402
C3112 1UF 10% 6.3V CERM 402
C3113 1UF 10% 6.3V CERM 402
C3114 1UF 10% 6.3V CERM 402
C3115 1UF 10% 6.3V CERM 402
C3116 1UF 10% 6.3V CERM 402
C3117 1UF 10% 6.3V CERM 402
C3118 1UF 10% 6.3V CERM 402
C3119 1UF 10% 6.3V CERM 402
C3120 1UF 10% 6.3V CERM 402
C3121 1UF 10% 6.3V CERM 402

DDR2 SO-DIMM Connector A

SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE	SHT	OF
NONE	31	109

Page Notes

Power aliases required by this page:
- =PP1V8_S3M_MEM_B
- =PP0V9_S3M_MEM_DIMMVREFB
- =PPSPD_S0M_MEM_B (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

=PP0V9_S3M_MEM_DIMMVREFB

C3201 2.2uF 20% 6.3V CERM 603

C3200 0.1uF 20% 10V CERM 402

"Expansion" (surface-mount) slot

DDR2-SODIMM-DUAL

CRITICAL
J3200
F-RT-SM-M9

	=PP1V8_S3M_MEM_B	1A	VREF	VSS0	2A	=PP1V8_S3M_MEM_B
		3A	VSS1	DQ4	4A	MEM_B_DQ<9>
MEM_B_DQ<15>		5A	DQ0	DQ5	6A	MEM_B_DQ<11>
MEM_B_DQ<14>		7A	DQ1	VSS2	8A	
		9A	VSS4	DM0	10A	MEM_B_DM<1>
MEM_B_DQS_N<1>		11A	DQS0*	VSS5	12A	
MEM_B_DQS_P<1>		13A	DQS0	DQ6	14A	MEM_B_DQ<12>
		15A	VSS6	DQ7	16A	MEM_B_DQ<8>
MEM_B_DQ<10>		17A	DQ2	VSS7	18A	
MEM_B_DQ<13>		19A	DQ3	DQ12	20A	MEM_B_DQ<3>
		21A	VSS8	DQ13	22A	MEM_B_DQ<6>
MEM_B_DQ<7>		23A	DQ8	VSS9	24A	
MEM_B_DQ<2>		25A	DQ9	DM1	26A	MEM_B_DM<0>
		27A	VSS10	VSS11	28A	
MEM_B_DQS_N<0>		29A	DQS1*	CK0	30A	MEM_CLK_P<4>
MEM_B_DQS_P<0>		31A	DQS1	CK0*	32A	MEM_CLK_N<4>
		33A	VSS12	VSS13	34A	
MEM_B_DQ<1>		35A	DQ10	DQ14	36A	MEM_B_DQ<0>
MEM_B_DQ<4>		37A	DQ11	DQ15	38A	MEM_B_DQ<5>
		39A	VSS14	VSS15	40A	
		41A	VSS16	VSS17	42A	KEY
MEM_B_DQ<21>		43A	DQ16	DQ20	44A	MEM_B_DQ<22>
MEM_B_DQ<19>		45A	DQ17	DQ21	46A	MEM_B_DQ<18>
		47A	VSS18	VSS19	48A	
MEM_B_DQS_N<2>		49A	DQS2*	NC0	50A	PM_EXTTS_L<1>
MEM_B_DQS_P<2>		51A	DQS2	DM2	52A	MEM_B_DM<2>
		53A	VSS21	VSS22	54A	
MEM_B_DQ<20>		55A	DQ18	DQ22	56A	MEM_B_DQ<17>
MEM_B_DQ<23>		57A	DQ19	DQ23	58A	MEM_B_DQ<16>
		59A	VSS23	VSS24	60A	
MEM_B_DQ<29>		61A	DQ24	DQ28	62A	MEM_B_DQ<26>
MEM_B_DQ<24>		63A	DQ25	DQ29	64A	MEM_B_DQ<28>
		65A	VSS25	VSS26	66A	
MEM_B_DM<3>		67A	DM3	DQS3*	68A	MEM_B_DQS_N<3>
	NC	69A	NC1	DQS3	70A	MEM_B_DQS_P<3>
		71A	VSS27	VSS28	72A	
MEM_B_DQ<27>		73A	DQ26	DQ30	74A	MEM_B_DQ<31>
MEM_B_DQ<25>		75A	DQ27	DQ31	76A	MEM_B_DQ<30>
		77A	VSS29	VSS30	78A	
MEM_CKE<3>		79A	CKE0	NC/CKE1	80A	MEM_CKE<4>
		81A	VDD0	VDD1	82A	
	NC	83A	NC2	NC/A15	84A	MEM_B_A<15>
MEM_B_BS<2>		85A	BA2	NC/A14	86A	MEM_B_A<14>
		87A	VDD2	VDD3	88A	
MEM_B_A<12>		89A	A12	A11	90A	MEM_B_A<11>
MEM_B_A<9>		91A	A9	A7	92A	MEM_B_A<7>
MEM_B_A<8>		93A	A8	A6	94A	MEM_B_A<6>
		95A	VDD4	VDD5	96A	
MEM_B_A<5>		97A	A5	A4	98A	MEM_B_A<4>
MEM_B_A<3>		99A	A3	A2	100A	MEM_B_A<2>
MEM_B_A<1>		101A	A1	A0	102A	MEM_B_A<0>
		103A	VDD6	VDD7	104A	
MEM_B_A<10>		105A	A10/AP	BA1	106A	MEM_B_BS<1>
MEM_B_BS<0>		107A	BA0	RAS*	108A	MEM_B_RAS_L
MEM_B_WE_L		109A	WE*	S0*	110A	MEM_CS_L<2>
		111A	VDD8	VDD9	112A	
MEM_B_CAS_L		113A	CAS*	ODT0	114A	MEM_ODT<2>
MEM_CS_L<3>		115A	NC/S1*	NC/A13	116A	MEM_B_A<13>
		117A	VDD10	VDD11	118A	
MEM_ODT<3>		119A	NC/ODT1	NC3	120A	NC
		121A	VSS31	VSS32	122A	
MEM_B_DQ<36>		123A	DQ32	DQ36	124A	MEM_B_DQ<32>
MEM_B_DQ<33>		125A	DQ33	DQ37	126A	MEM_B_DQ<37>
		127A	VSS33	VSS34	128A	
MEM_B_DQS_N<4>		129A	DQS4*	DM4	130A	MEM_B_DM<4>
MEM_B_DQS_P<4>		131A	DQS4	VSS35	132A	
		133A	VSS36	DQ38	134A	MEM_B_DQ<38>
MEM_B_DQ<34>		135A	DQ34	DQ39	136A	MEM_B_DQ<39>
MEM_B_DQ<35>		137A	DQ35	VSS37	138A	
		139A	VSS38	DQ44	140A	MEM_B_DQ<56>
MEM_B_DQ<57>		141A	DQ40	DQ45	142A	MEM_B_DQ<59>
MEM_B_DQ<60>		143A	DQ41	VSS39	144A	
		145A	VSS40	DQS5*	146A	MEM_B_DQS_N<7>
MEM_B_DM<7>		147A	DM5	DQS5	148A	MEM_B_DQS_P<7>
		149A	VSS41	VSS42	150A	
MEM_B_DQ<61>		151A	DQ42	DQ46	152A	MEM_B_DQ<63>
MEM_B_DQ<62>		153A	DQ43	DQ47	154A	MEM_B_DQ<58>
		155A	VSS43	VSS44	156A	
MEM_B_DQ<48>		157A	DQ48	DQ52	158A	MEM_B_DQ<54>
MEM_B_DQ<51>		159A	DQ49	DQ53	160A	MEM_B_DQ<53>
		161A	VSS45	VSS46	162A	
	NC	163A	NC_TEST	CK1	164A	MEM_CLK_P<3>
		165A	VSS47	CK1*	166A	MEM_CLK_N<3>
MEM_B_DQS_N<6>		167A	DQS6*	VSS48	168A	
MEM_B_DQS_P<6>		169A	DQS6	DM6	170A	MEM_B_DM<6>
		171A	VSS49	VSS50	172A	
MEM_B_DQ<50>		173A	DQ50	DQ54	174A	MEM_B_DQ<52>
MEM_B_DQ<55>		175A	DQ51	DQ55	176A	MEM_B_DQ<49>
		177A	VSS51	VSS52	178A	
MEM_B_DQ<40>		179A	DQ56	DQ60	180A	MEM_B_DQ<46>
MEM_B_DQ<47>		181A	DQ57	DQ61	182A	MEM_B_DQ<43>
		183A	VSS53	VSS54	184A	
MEM_B_DM<5>		185A	DM7	DQS7*	186A	MEM_B_DQS_N<5>
		187A	VSS55	DQS7	188A	MEM_B_DQS_P<5>
MEM_B_DQ<42>		189A	DQ58	VSS56	190A	
MEM_B_DQ<45>		191A	DQ59	DQ62	192A	MEM_B_DQ<41>
=PPSPD_S0M_MEM_B		193A	VSS57	DQ63	194A	MEM_B_DQ<44>
=I2C_SODIMMB_SDA		195A	SDA	VSS58	196A	
=I2C_SODIMMB_SCL		197A	SCL	SA0	198A	Resistor prevents pwr-gnd short
		199A	VDDSPD	SA1	200A	SODIMM_B_SA1
						ADDR=0xA4(WR)/0xA5(RD)

203 201 202 204 516S0471

=PPSPD_S0M_MEM_B

R3200 10K 5% 1/16W MF-LF 402

DDR2 Bypass Caps

(For return current)

=PP1V8_S3M_MEM_B

C3208 10UF 20% 6.3V X5R 603

C3209 10UF 20% 6.3V X5R 603

C3210 1UF 10% 6.3V CERM 402

C3211 0.1UF 20% 10V CERM 402

C3212 1UF 10% 6.3V CERM 402

C3213 1UF 10% 6.3V CERM 402

C3214 1UF 10% 6.3V CERM 402

C3215 1UF 10% 6.3V CERM 402

C3216 1UF 10% 6.3V CERM 402

C3217 0.1UF 20% 10V CERM 402

C3218 0.1UF 20% 10V CERM 402

C3219 0.1UF 20% 10V CERM 402

C3220 0.1UF 20% 10V CERM 402

C3221 0.1UF 20% 10V CERM 402

DDR2 SO-DIMM Connector B

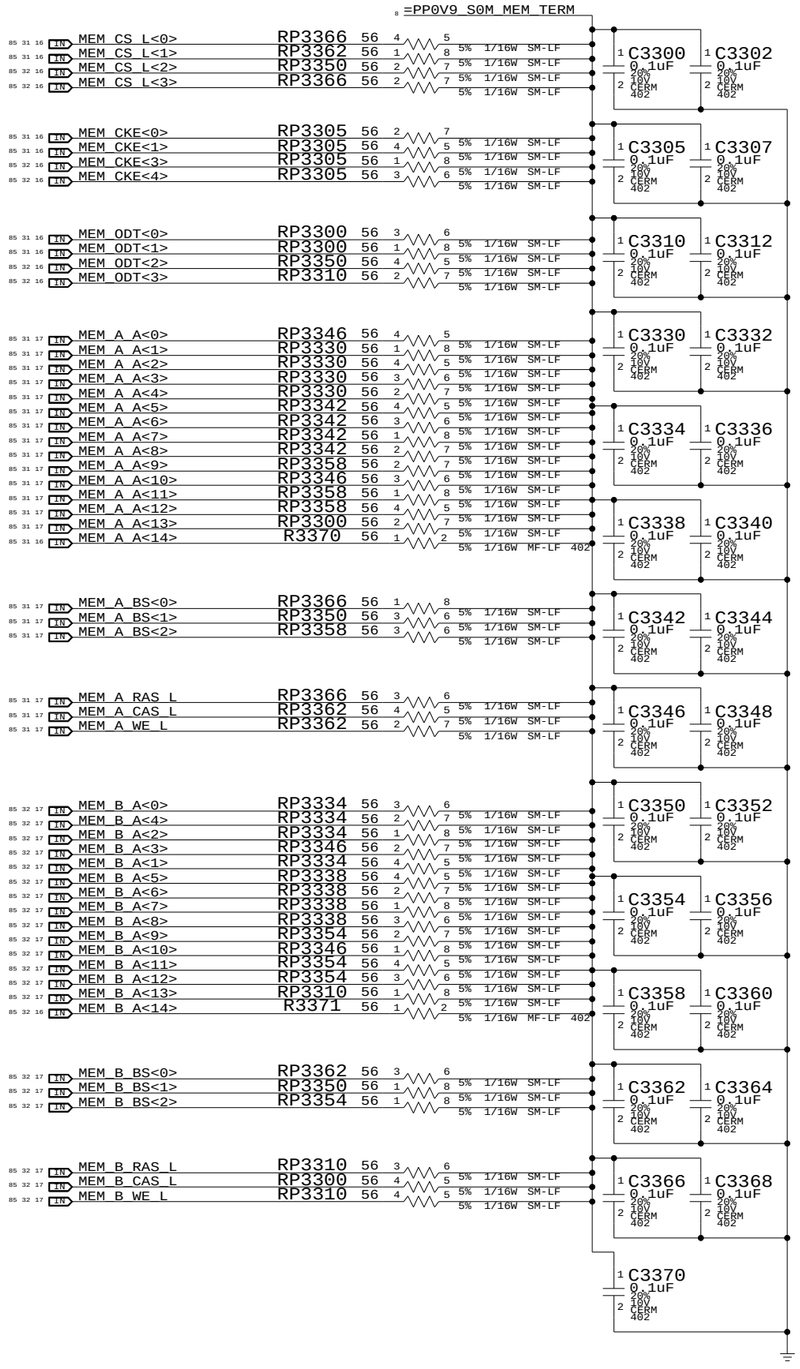
SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 32 OF 109	

One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

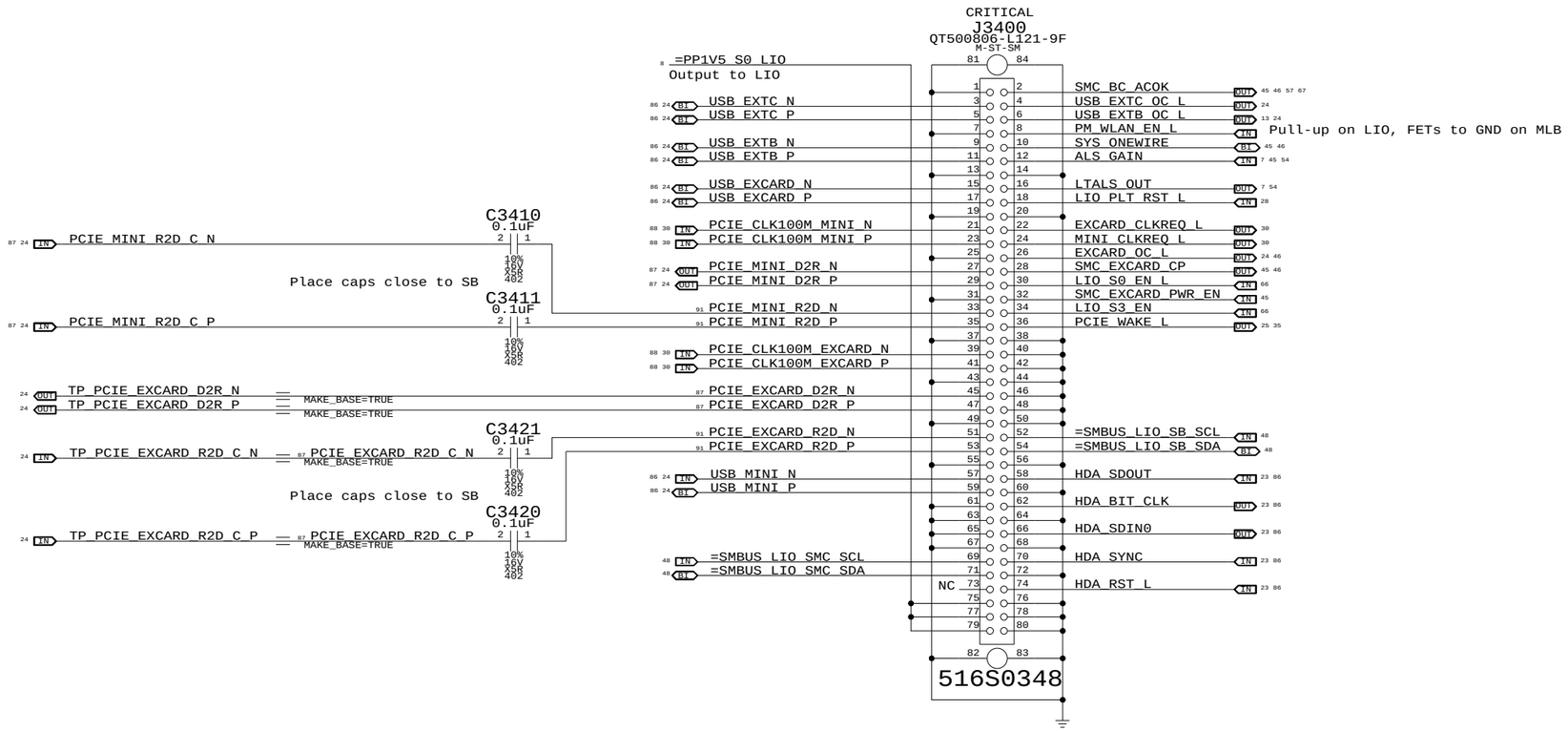
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B

SCALE	SHT	OF
NONE	33	109

Left I/O Board Connector



Left I/O Board Connector	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7520	B
	SCALE: NONE	SHT 34 OF 109	

Page Notes

Power aliases required by this page:
- =PP3V3_ENET_PHY (EC / Ultra)
- =PP1V8R2V5_ENET_PHY (2.5V / 1.8V)
- =YUKON_EC_PP2V5_ENET (2.5V / GND)
- =PP1V2_ENET_PHY

Signal aliases required by this page:
- =ENET_CLKREQ_L (NC/TP for Yukon EC)
- =ENET_VMAIN_AVLBL (See note by pin)

BOM options provided by this page:
YUKON_EC - Selects Yukon EC RSET value.
YUKON_ULTRA - Selects Yukon Ultra RSET.

NOTE: See bottom of page for instructions for dual Yukon EC / Yukon Ultra schematic support.

=PP1V2_ENET_PHY

Yukon EC		Yukon Ultra	
No link:	171 mA	No link:	130 mA
10 Mbps:	179 mA	10 Mbps:	130 mA
100 Mbps:	203 mA	100 Mbps:	150 mA
1000 Mbps:	426 mA	1000 Mbps:	290 mA

C3700 4.7UF 20% 6.3V CERM 603; C3701 0.1UF 10% 16V X5R 402; C3702 0.1UF 10% 16V X5R 402; C3703 0.1UF 10% 16V X5R 402; C3704 0.1UF 10% 16V X5R 402; C3705 0.1UF 10% 16V X5R 402; C3706 0.001UF 10% 50V CERM 402; C3707 0.001UF 10% 50V CERM 402; C3708 0.001UF 10% 50V CERM 402

=PP3V3_ENET_PHY

Yukon EC		Yukon Ultra	
No link:	4 mA	No link:	60 mA
10 Mbps:	4 mA	10 Mbps:	70 mA
100 Mbps:	4 mA	100 Mbps:	70 mA
1000 Mbps:	4 mA	1000 Mbps:	80 mA

C3710 4.7UF 20% 6.3V CERM 603; C3711 0.1UF 10% 16V X5R 402; C3712 0.1UF 10% 16V X5R 402; C3713 0.1UF 10% 16V X5R 402; C3714 0.001UF 10% 50V CERM 402; C3715 0.001UF 10% 50V CERM 402

=PP1V8R2V5_ENET_PHY L3720 FERR-120-OHM-1.5A 0402 PP1V8R2V5_ENET_PHY_AVDD
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

Yukon EC (2.5V)		Yukon Ultra (1.8V)	
No link:	82 mA	No link:	0 mA
10 Mbps:	108 mA	10 Mbps:	30 mA
100 Mbps:	126 mA	100 Mbps:	40 mA
1000 Mbps:	218 mA	1000 Mbps:	150 mA

(EC:2.5V)

C3720 4.7UF 20% 6.3V CERM 603; C3721 0.1UF 10% 16V X5R 402; C3722 0.1UF 10% 16V X5R 402; C3723 0.1UF 10% 16V X5R 402; C3724 0.001UF 10% 50V CERM 402

=YUKON_EC_PP2V5_ENET
Yukon EC: Alias to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF & 1x 0.001uF caps
Yukon Ultra: Alias to GND

PCIE_ENET_D2R_P
PCIE_ENET_D2R_N
PCIE_ENET_R2D_C_P
PCIE_ENET_R2D_C_N
C3735 0.1UF 10% 16V X5R 402
C3736 0.1UF 10% 16V X5R 402
C3730 0.1UF 10% 16V X5R 402
C3731 0.1UF 10% 16V X5R 402
PLACEMENT_NOTE=Place C3730 close to southbridge.
PLACEMENT_NOTE=Place C3731 close to southbridge.

PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
=ENET_CLKREQ_L
PCIE_WAKE_L
ENET_RESET_L
Yukon EC: Pin 42 should be NC (or TP) net.

ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>

SIGNAL_MODEL=EMPTY
R3740 R3741 R3742 R3743 R3744 R3745 R3746 R3747 49.9 1% 1/16W MF-LF 402
ENET_MDI0 ENET_MDI1 ENET_MDI2 ENET_MDI3
C3740 C3742 C3744 C3746 0.001UF 10% 50V CERM 402

ENET_CLK25M_XTALI
ENET_CLK25M_XTALO

U3700 88E8058 QFN
CRITICAL
BOMOPTION=OMIT

NC_32	32		
NC_51	51		
NC_52	52		
NC_57	57		
NC_64	64		
AVDD0	19		
AVDD1	22		
AVDD2	23		
AVDD3	28		
		EC:AVDD 2.5V	
VDDO_TTL0	1		
VDDO_TTL1	40		
VDDO_TTL2	45		
VDDO_TTL3	61		
AVDDH	8		
VDD0	2		
VDD1	7		
VDD2	13		
VDD3	33		
VDD4	39		
VDD5	44		
VDD6	48		
VDD7	58		
TX_P	49	PCIE_ENET_D2R_C_P	
TX_N	50	PCIE_ENET_D2R_C_N	
RX_P	54	PCIE_ENET_R2D_P	
RX_N	53	PCIE_ENET_R2D_N	
REFCLKP	55		
REFCLKN	56		
CLKREQ*	42	EC:NO CONNECT	
WAKE*	6		
PERST*	5		
MDIP0	17		
MDIN0	18		
MDIP1	20		
MDIN1	21		
MDIP2	26		
MDIN2	27		
MDIP3	30		
MDIN3	31		
XTALI	15		
XTALO	14		
THRML_PAD	65		

PCI EXPRESS
MEDIA
MAIN CLK

ANALOG

LOM_DISABLE*	10	ENET_LOM_DIS_L	
VAUX_AVLBL	12		
SWITCH_VAUX	9	NC	
VMAIN_AVLBL	47	=ENET_VMAIN_AVLBL	IN 66
SWITCH_VCC	11	NC	
EC:CTRL25 CTRL18	4	TP_YUKON_CTRL18	OUT
CTRL12	3	TP_YUKON_CTRL12	OUT
RSET	16	YUKON_RSET	

Must be high in S0 state (can use PP3V3_S0 as input)

R3760 4.7K 5% 1/10W MF-LF 402

YUKON_ULTRA
R3765 4.99K 1% 1/10W MF-LF 402

LED

LED_ACT*	59	NC
LED_LINK10/100*	60	NC
LED_LINK1000*	62	NC
LED_DUPLEX*	63	NC

SPI

(IPU) SPI_DO	34	NC
(IPU) SPI_DI	35	NC
(IPU) SPI_CLK	37	NC
(IPU) SPI_CS	36	NC

TWSI

(IPU) VPD_CLK	38	YUKON_VPD_CLK
(IPU) VPD_DATA	41	YUKON_VPD_DATA

TEST/RSVD

(IPD) TESTMODE	46	
RSVD_24	24	NC
RSVD_25	25	NC
RSVD_29	29	NC
RSVD_43	43	NC

VPD ROM
C3780 0.1UF 10% 16V X5R 402
R3780 4.7K 5% 1/10W MF-LF 402
R3781 4.7K 5% 1/10W MF-LF 402
U3780 M24C08 SO8 CRITICAL
E2 NC1 NC0 WC* VCC OMIT SDA SCL VSS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0386	1	IC,88E8058,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	YUKON_ULTRA
341S2060	1	IC,FLASH,88E8058 ETHERNET VPD,IIC,SO8	U3780	CRITICAL	YUKON_ULTRA
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	YUKON_EC
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U3780	CRITICAL	YUKON_EC
114S0285	1	RES,4.87K,1%,1/16W,0402,LF	R3760		YUKON_EC

To support Yukon EC and Ultra on the same board:

- Alias =YUKON_EC_PP2V5_ENET to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF and 1x 0.001uF caps
- Use 0-ohm resistors or variable supply to provide 1.8V or 2.5V to =PP1V8R2V5_ENET_PHY and magnetics. Can also use BCP69T1 connected to CTRL18 pin 4 for internal VR.
- Connect =ENET_CLKREQ_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON_ULTRA)
- Use YUKON_EC and YUKON_ULTRA BOMOPTIONs to select stuffed part

Ethernet (Yukon)

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

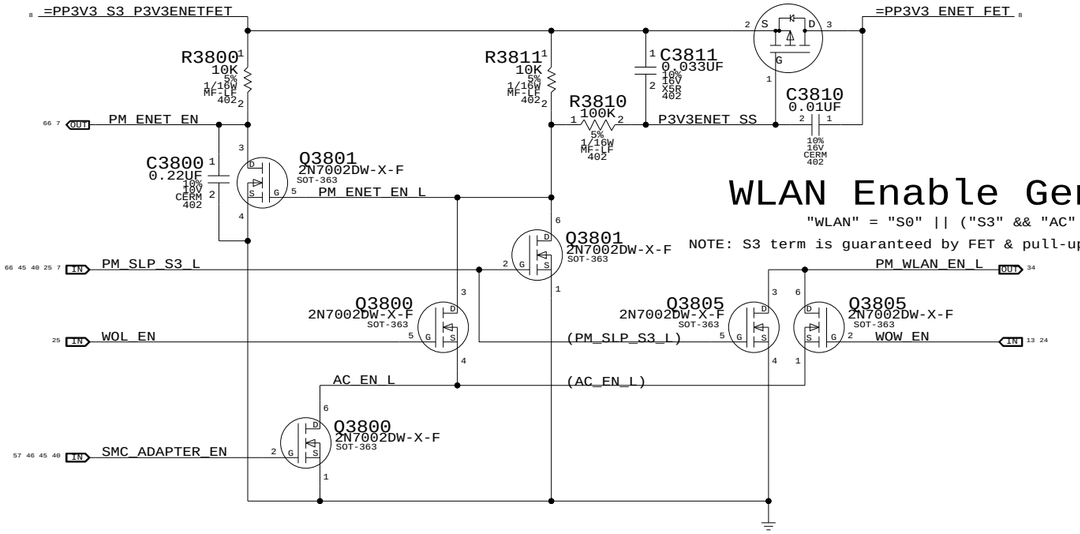
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 37 OF 109	

ENET Enable Generation

"ENET" = "S0" || ("S3" && "AC" && "WOL_EN")

NOTE: S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.



3.3V ENET FET

WLAN Enable Generation

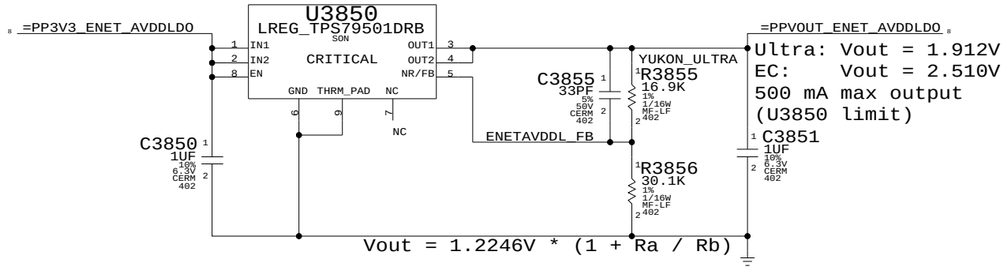
"WLAN" = "S0" || ("S3" && "AC" && "WOW_EN")

NOTE: S3 term is guaranteed by FET & pull-up source, MUST BE S3 RAIL.

Yukon AVDDL LDO

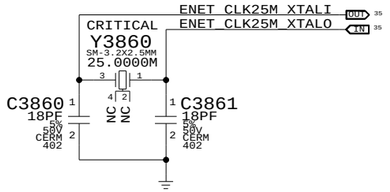
1.9V for Yukon Ultra, 2.5V for Yukon EC

Yukon Ultra requires 1.9V on its magnetics to pass compliance tests



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0363	1	RES,31.6K,1%,1/16W,402,LF	R3855		YUKON_EC

Yukon Crystal



Yukon Power Control

SYNC_MASTER=T9_NOME SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 38 OF 109	

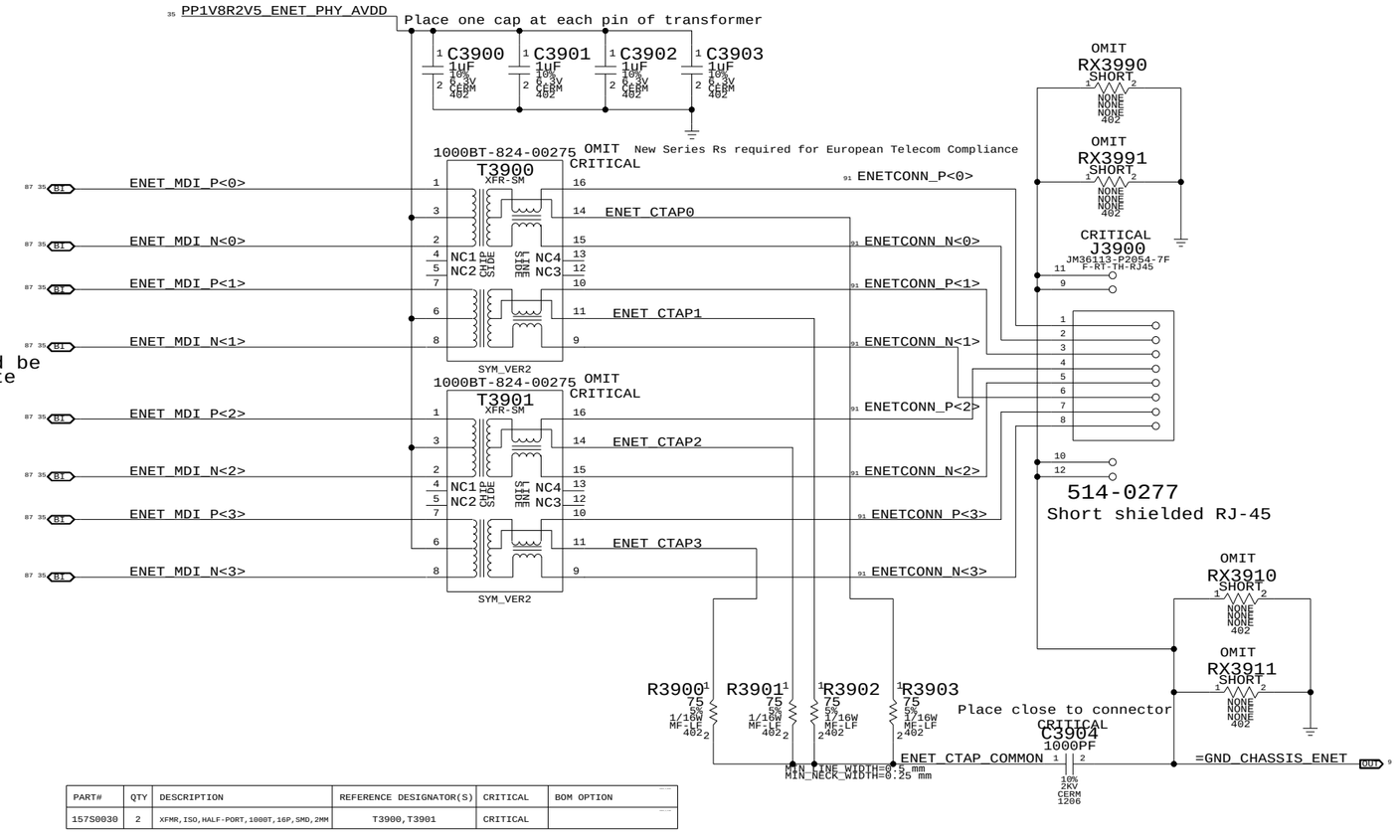
Page Notes

Power aliases required by this page:
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Transformers should be mirrored on opposite sides of the board



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
157S0030	2	XFMR,ISO,HALF-PORT,1000T,16P,SMD,2MM	T3900,T3901	CRITICAL	

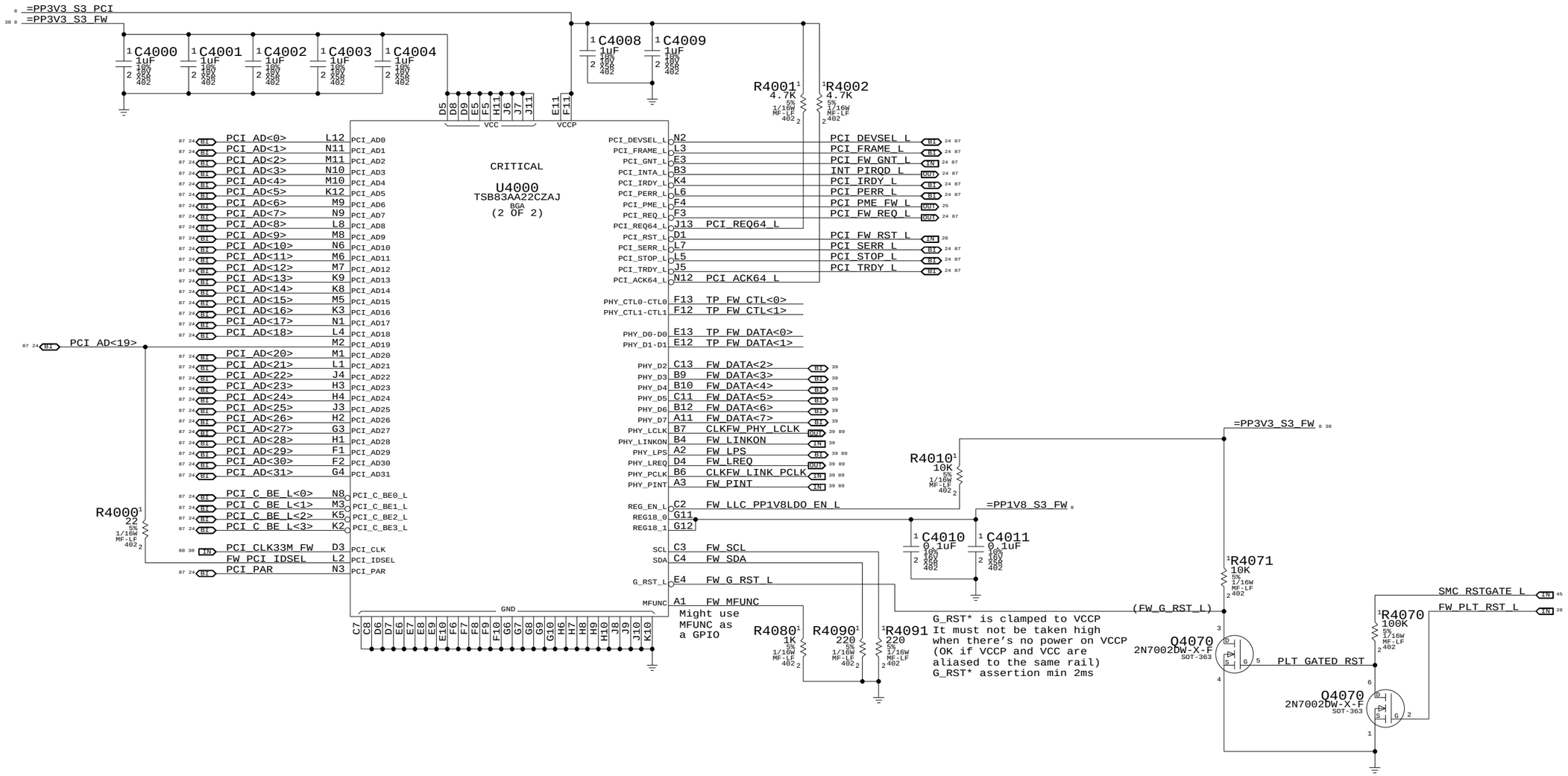
Ethernet Connector

SYNC_MASTER=M75_MLB SYNC_DATE=12/21/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B

SCALE: NONE SHT 39 OF 109



FireWire Link (TSB83AA22)

SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

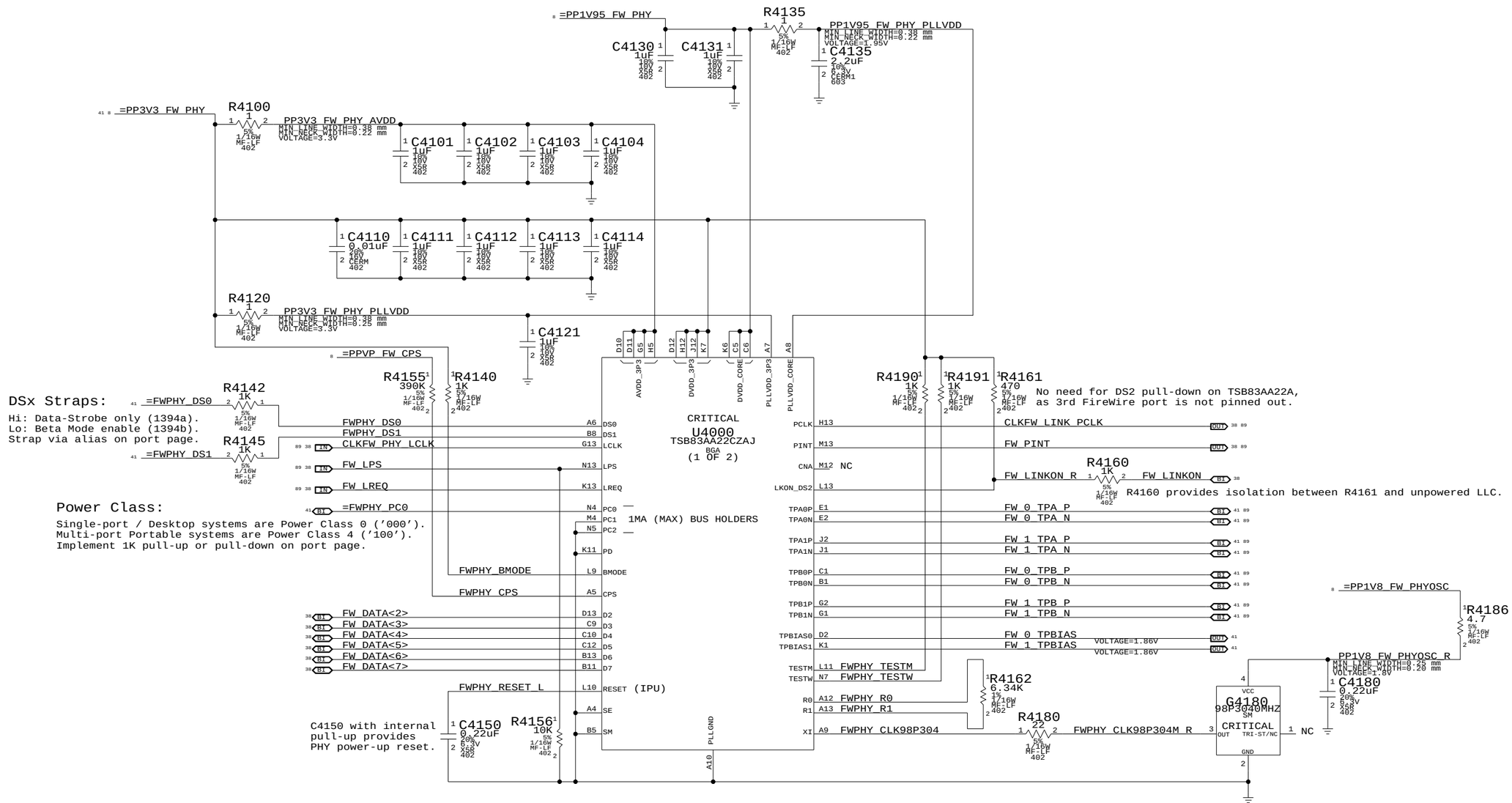
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 40 OF 109	



FireWire PHY (TSB83AA22)

SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 41 OF 109	

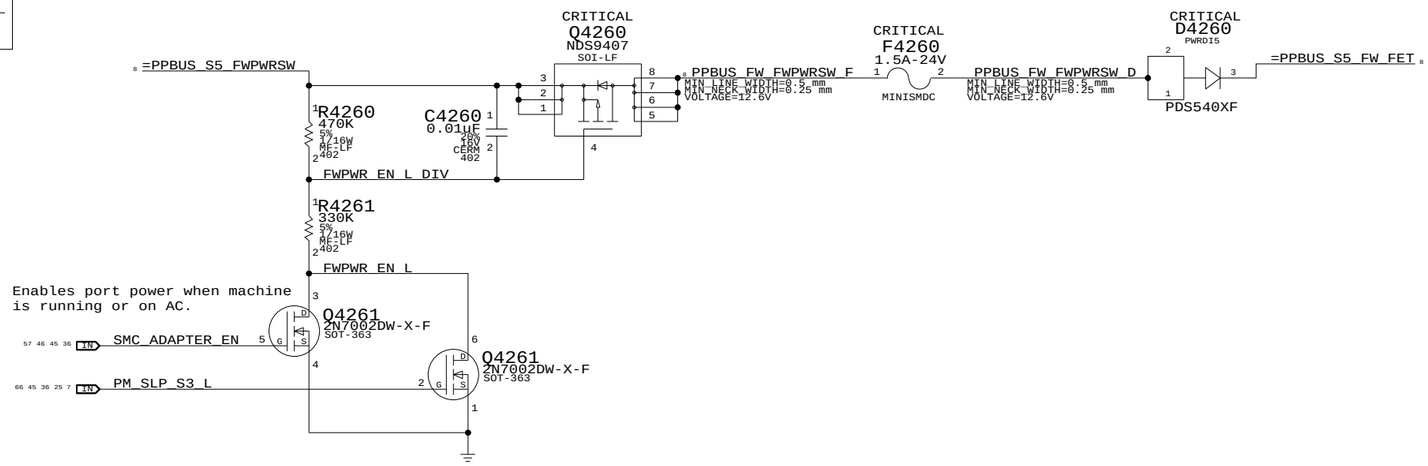
Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

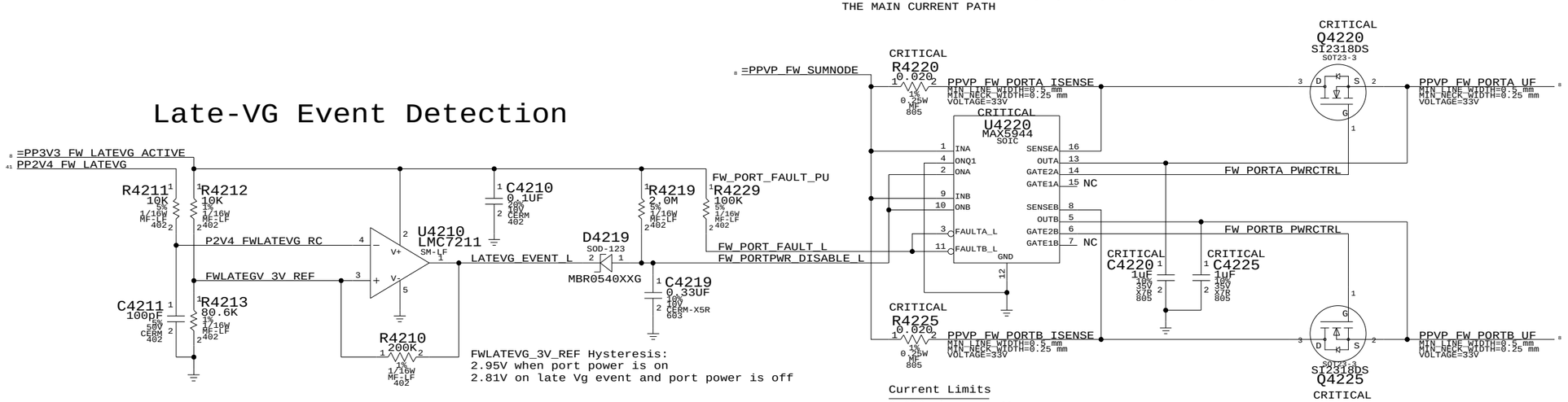
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- FW_PORT_FAULT_PU

FireWire Port Power Switch



Current Limit/Active Late-VG Protection



Current Limits

0.020 ohm => 2.4A
0.025 ohm => 2A
0.030 ohm => 1.66A (Ideal)
0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

FireWire Port Power

SYNC_MASTER=M75_MLB SYNC_DATE=03/07/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE	SHT	OF
NONE	42	109

Page Notes

Power aliases required by this page:
- =PPVP_FW_PORT0
- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG
- =GND_CHASSIS_FW_PORT0L
- =GND_CHASSIS_FW_PORT0U
- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:
- 2-port Portable Power Class (4)
- Port "0" Data-Strobe only (1394A)
- Port "1" Bilingual (1394B)

39 8 =PP3V3_FW_PHY
39 =FWPHY_PC0
39 =FWPHY_DS0
39 =FWPHY_DS1

Termination

Place close to FireWire PHY

TI PHYs require 1uF even though FW spec calls out 0.33uF

39 FW_1_TPBIAS
39 FW_0_TPBIAS
C4350 1uF 10% 6.3V CERM 402
C4360 1uF 10% 6.3V CERM 402
CRITICAL L4360 18NH-250MA 0402 FW_B_TPA_L_P
CRITICAL L4361 18NH-250MA 0402 FW_B_TPA_L_N
R4350 56.2 1% 1/16W MF-LF 402
R4351 56.2 1% 1/16W MF-LF 402
R4360 56.2 1% 1/16W MF-LF 402
R4361 56.2 1% 1/16W MF-LF 402

89 39 FW_0_TPA_P — FW_PORT0_TPA_P 41 MAKE_BASE=TRUE
89 39 FW_0_TPA_N — FW_PORT0_TPA_N 41 MAKE_BASE=TRUE
89 39 FW_0_TPB_P — FW_PORT0_TPB_P 41 MAKE_BASE=TRUE
89 39 FW_0_TPB_N — FW_PORT0_TPB_N 41 MAKE_BASE=TRUE
89 39 FW_1_TPA_P — FW_PORT1_TPA_P 41 MAKE_BASE=TRUE
89 39 FW_1_TPA_N — FW_PORT1_TPA_N 41 MAKE_BASE=TRUE
89 39 FW_1_TPB_P — FW_PORT1_TPB_P 41 MAKE_BASE=TRUE
89 39 FW_1_TPB_N — FW_PORT1_TPB_N 41 MAKE_BASE=TRUE

SIGNAL_MODEL=EMPTY
R4352 56.2 1% 1/16W MF-LF 402
R4353 56.2 1% 1/16W MF-LF 402
R4362 56.2 1% 1/16W MF-LF 402
R4363 56.2 1% 1/16W MF-LF 402
FW_B_TPB_L_N
FW_B_TPB_L_P
CRITICAL L4362 18NH-250MA 0402 SIGNAL_MODEL=EMPTY FW_PORT1_TPB_C
CRITICAL L4363 18NH-250MA 0402 SIGNAL_MODEL=EMPTY
FW_PORT0_TPB_C
C4354 220pF 5% 25V CERM 402
R4354 4.99K 1% 1/16W MF-LF 402
C4364 220pF 5% 25V CERM 402
R4364 4.99K 1% 1/16W MF-LF 402

Late-VG Protection Power

8 =PP3V3_FW_LATEVG
R4390 332 1% 1/16W MF-LF 402
PP2V4_FW_LATEVG MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=2.4V 40 41
CRITICAL D4390 MMBZ5227B SOT23

ESD and late-VG rail for snap-back diodes (Common to all ports)

PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4390 should be 390 Ohms max for a 3.3V rail

Cable Power

CRITICAL Note: Trace PPVP_FW_PORT0 must handle up to 5A
8 =PPVP_FW_PORT0
CRITICAL L4300 FERR-250-OHM SM
C4304 0.001uF 20% 50V CERM 402
PPVP_FW_PORT0 MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=33V

41 9 =GND_CHASSIS_FW_PORT0L
OMIT CX4300 SHORT NONE NONE NONE 402
OMIT CX4301 SHORT NONE NONE NONE 402

"Snapback" & "Late VG" Protection

41 40 PP2V4_FW_LATEVG
DP4300 BAV99DW-X-F SOT-363
C4300 0.01uF 10% 50V X7R 402
C4301 0.01uF 10% 50V X7R 402
DP4300 BAV99DW-X-F SOT-363

41 FW_PORT0_TPA_P
41 FW_PORT0_TPA_N
41 FW_PORT0_TPB_P
41 FW_PORT0_TPB_N

CRITICAL FL4300 90-OHM-100MA 1210-4SM1
CRITICAL FL4301 90-OHM-100MA 1210-4SM1

91 FW_PORT0_TPA_FL_P
91 FW_PORT0_TPA_FL_N
91 FW_PORT0_TPB_FL_P
91 FW_PORT0_TPB_FL_N
(PPFW_PORT0_VP)
(GND_FW_PORT0_VG)

DP4301 BAV99DW-X-F SOT-363
C4302 0.01uF 10% 50V X7R 402
C4303 0.01uF 10% 50V X7R 402
DP4301 BAV99DW-X-F SOT-363
C4305 0.01uF 20% 50V CERM 603

PORT 0
1394A
CRITICAL J4300 1394A F-RT-TH-LF
6 TPO (TPA+)
5 TPO# (TPA-)
4 TPI (TPB+)
3 TPI# (TPB-)
1 VP
2 VGND
7 8 9 10
514-0255

=GND_CHASSIS_FW_PORT0L
=GND_CHASSIS_FW_PORT0U
OMIT CX4302 SHORT NONE NONE NONE 402
OMIT CX4303 SHORT NONE NONE NONE 402

Cable Power

8 =PPVP_FW_PORT1
CRITICAL L4310 FERR-250-OHM SM
C4314 0.001uF 20% 50V CERM 402
PPVP_FW_PORT1 MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=33V
Note: Trace PPVP_FW_PORT1 must handle up to 5A

41 9 =GND_CHASSIS_FW_PORT1
OMIT CX4304 SHORT NONE NONE NONE 402
OMIT CX4305 SHORT NONE NONE NONE 402

"Snapback" & "Late VG" Protection

41 40 PP2V4_FW_LATEVG
DP4310 BAV99DW-X-F SOT-363
C4311 0.01uF 10% 50V X7R 402
DP4310 BAV99DW-X-F SOT-363
C4310 0.01uF 10% 50V X7R 402

41 FW_PORT1_TPB_N
41 FW_PORT1_TPB_P
41 FW_PORT1_TPA_N
41 FW_PORT1_TPA_P

DP4311 BAV99DW-X-F SOT-363
C4312 0.01uF 10% 50V X7R 402
C4313 0.01uF 10% 50V X7R 402
DP4311 BAV99DW-X-F SOT-363

C4319 0.1uF 10% 50V X7R 603-1
R4319 1M 5% 1/16W MF-LF 402
NO STUFF C4317 0.01uF 20% 50V CERM 402
C4315 0.01uF 20% 50V CERM 603

PORT 1
BILINGUAL
CRITICAL J4310 1394B-UG31903 F-RT-SM1
10 TPB- TPB<R> TPB+ OUTPUT
9 2
8 VP
7 NC
6 VG
3 TPA- TPA<R> TPA+ INPUT
5 4
11
514S0133

(FW_PORT1_BREF)
(PPVP_FW_PORT1)
(GND_FW_PORT1_VG)
FW_PORT1_AREF

=GND_CHASSIS_FW_PORT1
OMIT CX4306 SHORT NONE NONE NONE 402
OMIT CX4307 SHORT NONE NONE NONE 402

PLACEMENT_NOTE=Place C4319 close to connector pin 5.

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

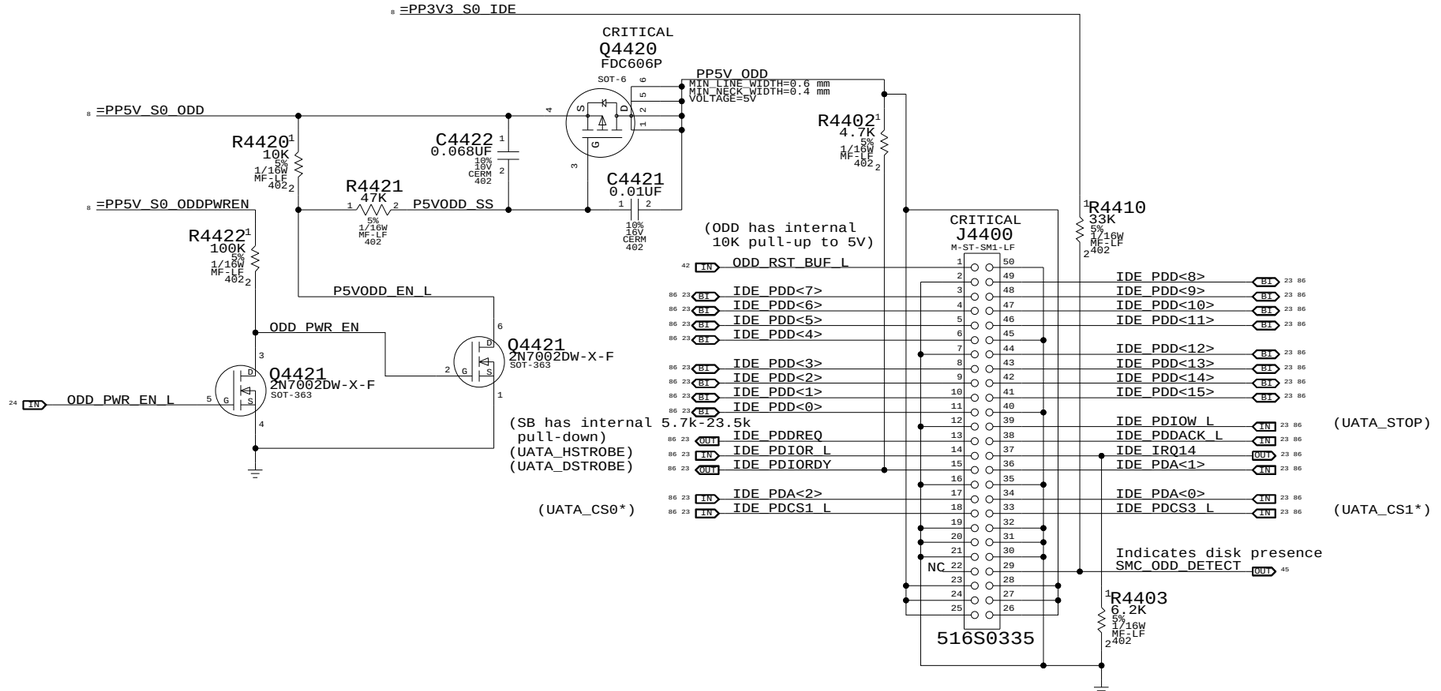
FireWire Ports

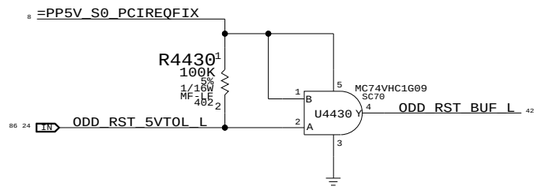
SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006

APPLE INC.

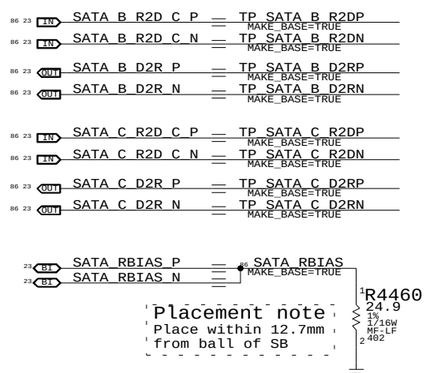
SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 43 OF 109	

IDE (ODD) Connector





Unused SATA Ports



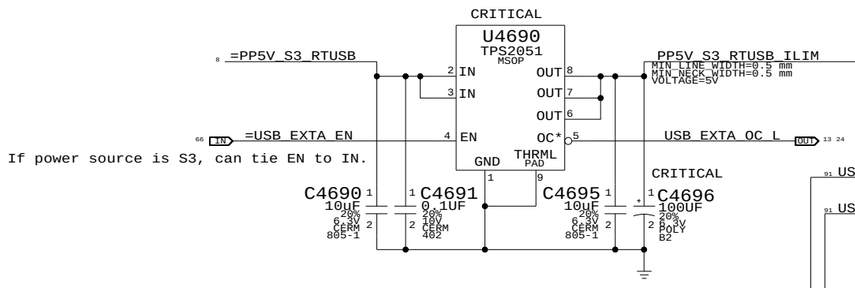
PATA Connector

SYNC_MASTER=M75_MLB SYNC_DATE=12/07/2006

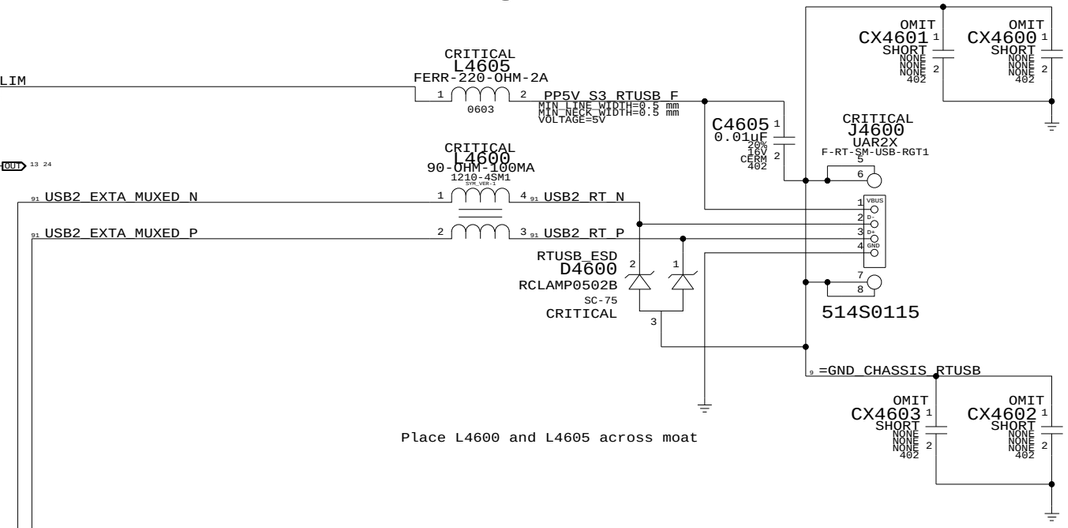
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 44 OF 109	

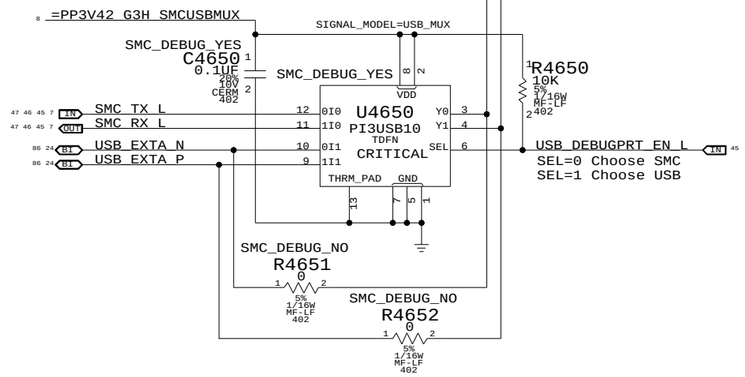
Port Power Switch



Right USB Port



USB/SMC Debug Mux



External USB Connector

SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

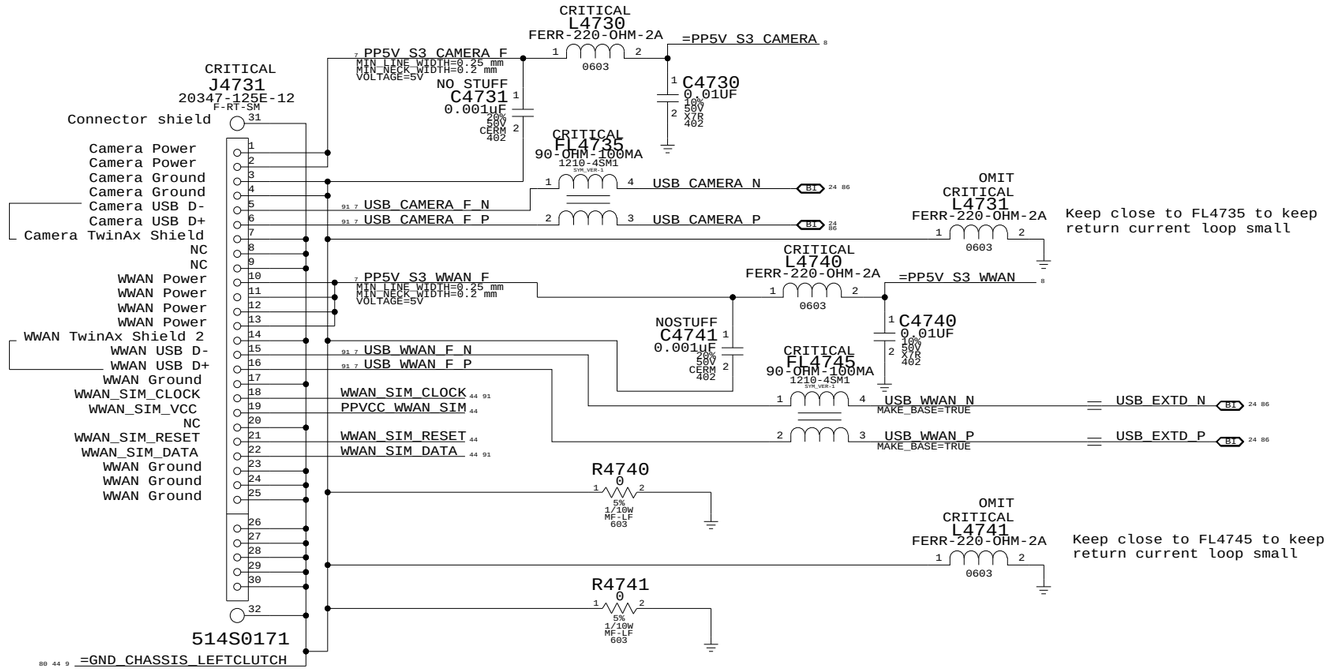
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

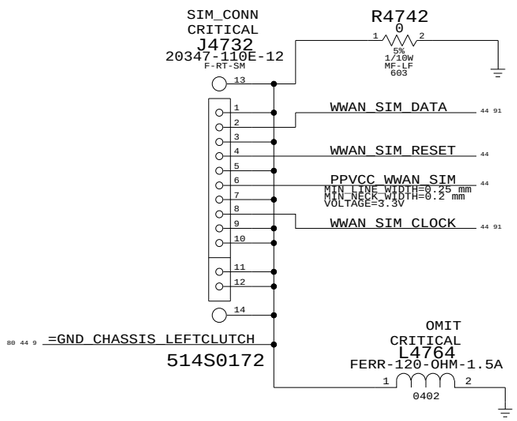
SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 46 OF 109	

Left Clutch Barrel Interconnect



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
113S0022	2	RES,MF,1/10W,0OHM,5,0603,SM,LF	L4731,L4741	CRITICAL	
116S0004	1	RES,MF,1/16W,0OHM,5,0402,SM,LF	L4764	CRITICAL	

SIM Interconnect



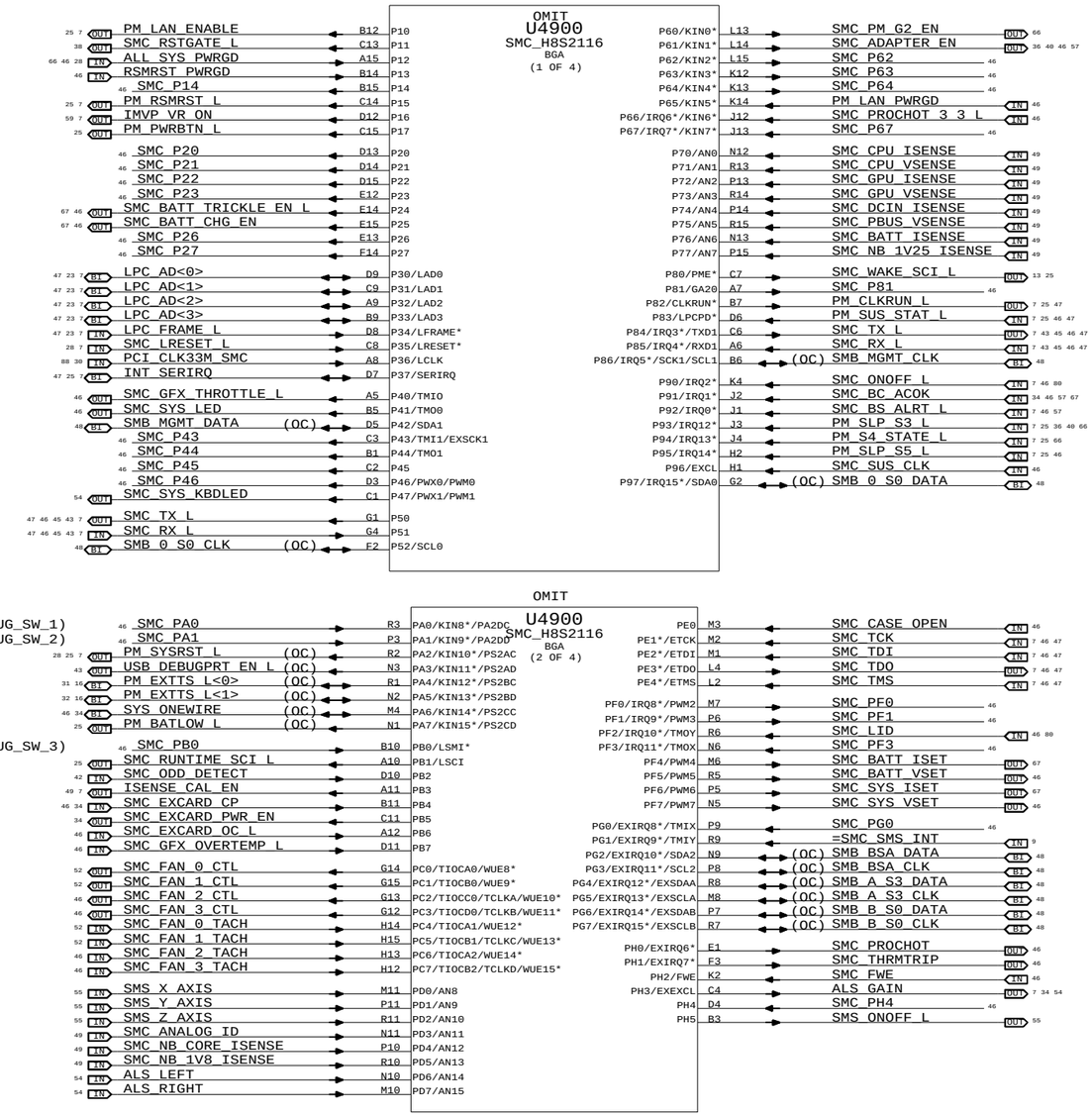
Left Clutch Barrel Interconnect

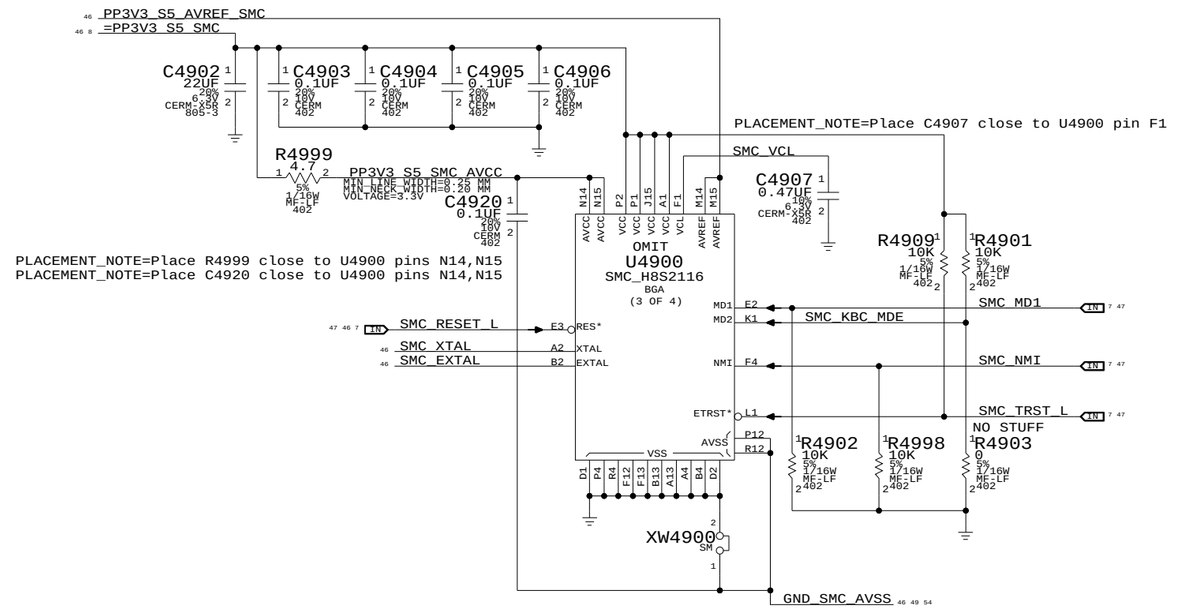
SYNC_MASTER=M75_MLB SYNC_DATE=12/21/2006

APPLE INC.

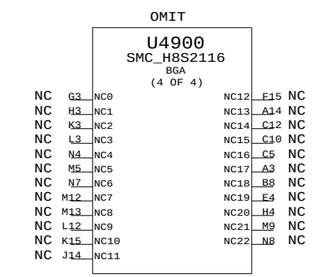
SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 47 OF 109	

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.



SMC	
SYNC_MASTER=T9_NOME	SYNC_DATE=12/21/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

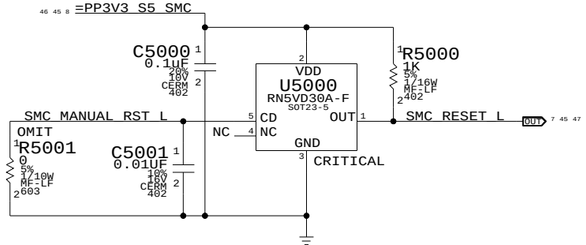
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

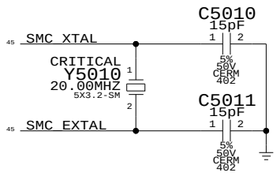
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 49 OF 109	

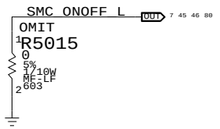
SMC Reset "Button" / Brownout Detect



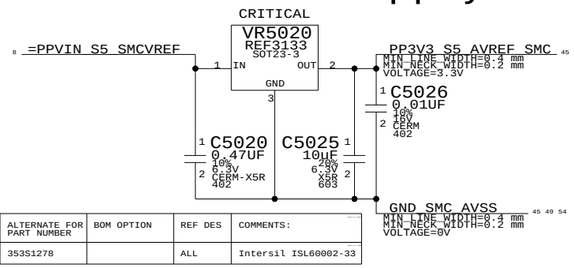
SMC Crystal Circuit



Debug Power "Button"

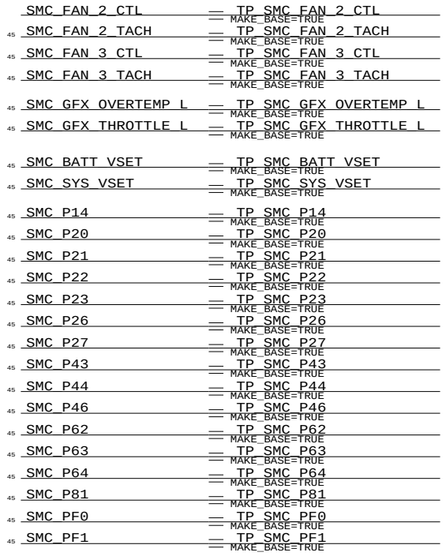


SMC AVREF Supply

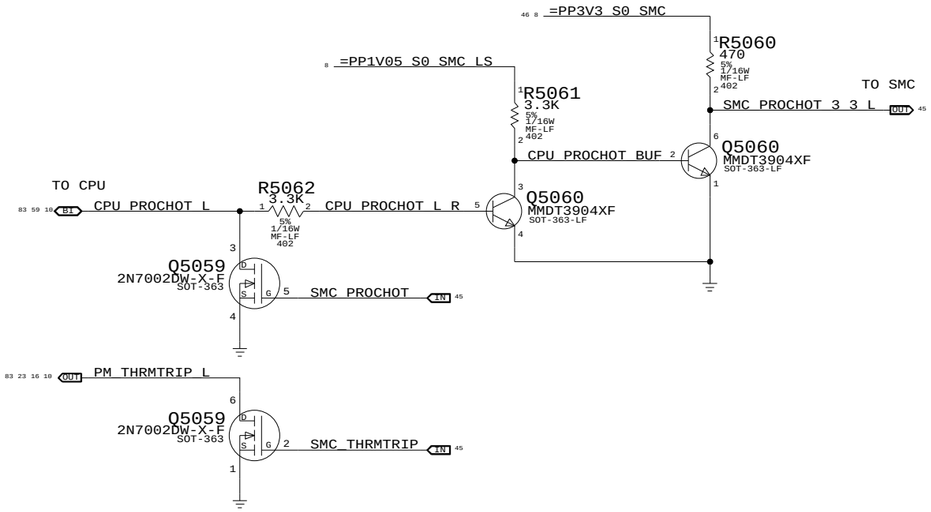


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		ALL	Intersil ISL60002-33

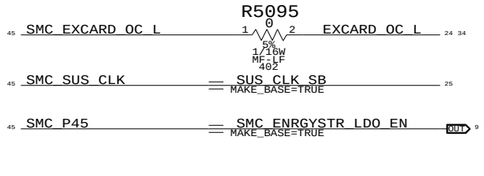
SMC_FAN / SMC_FSB / SMC_P / SMC_PF



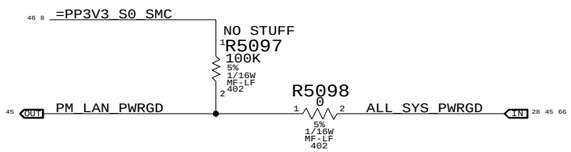
SMC FSB to 3.3V Level Shifting



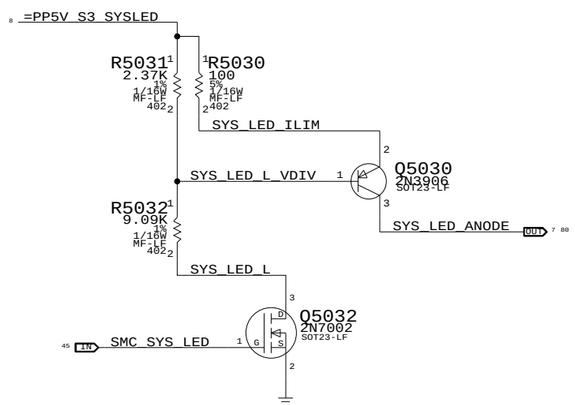
R5095 / SMC_EXCARD_OC_L / SMC_SUS_CLK / SMC_P45



LAN PWRGD Circuit

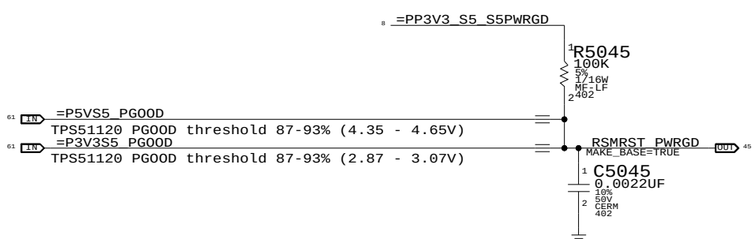


System (Sleep) LED Circuit

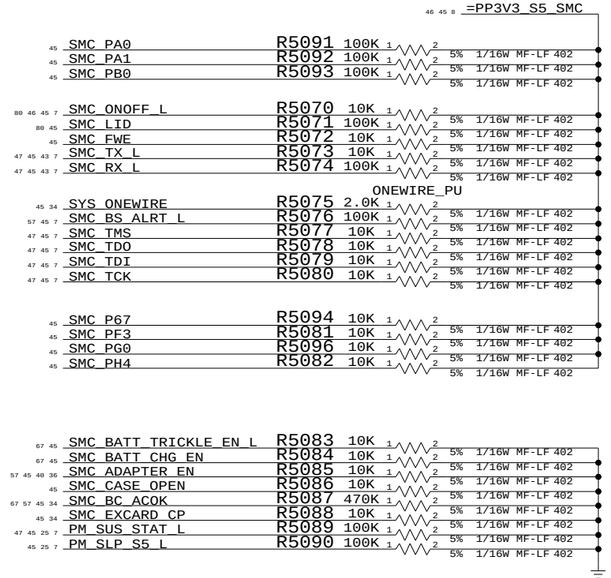


S5 Rail PWRGD Circuit

Reports when 5V S5 and 3.3V S5 are in regulation



SMC_PA / SMC_PB / SMC_ONOFF / SMC_LID / SMC_FWE / SMC_TX_L / SMC_RX_L / SMC_P67 / SMC_PF3 / SMC_PG0 / SMC_PH4 / SMC_BATT_TRICKLE_EN_L / SMC_BATT_CHG_EN / SMC_ADAPTER_EN / SMC_CASE_OPEN / SMC_BC_ACOK / SMC_EXCARD_CP / PM_SUS_STAT_L / PM_SLP_S5_L



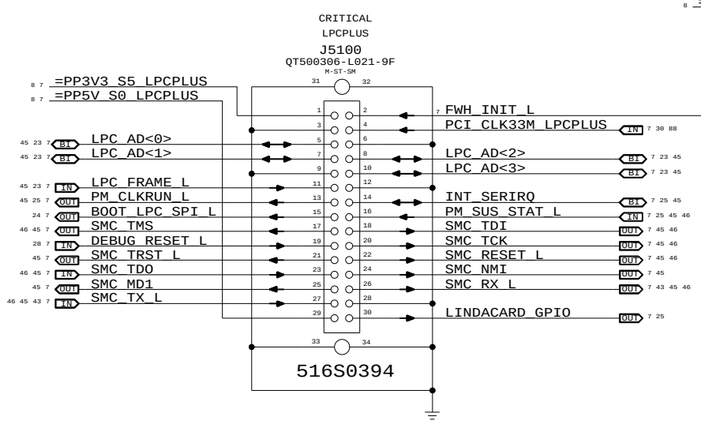
SMC Support

SYNC_MASTER=M75_MLB SYNC_DATE=04/25/2007

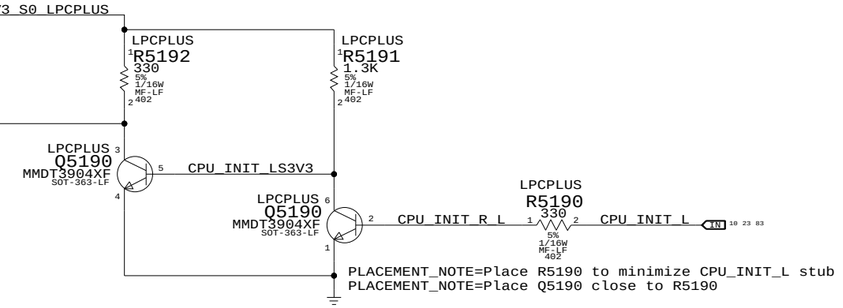
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 50 OF 109	

LPC+ Connector



FWH_INIT_L Generation



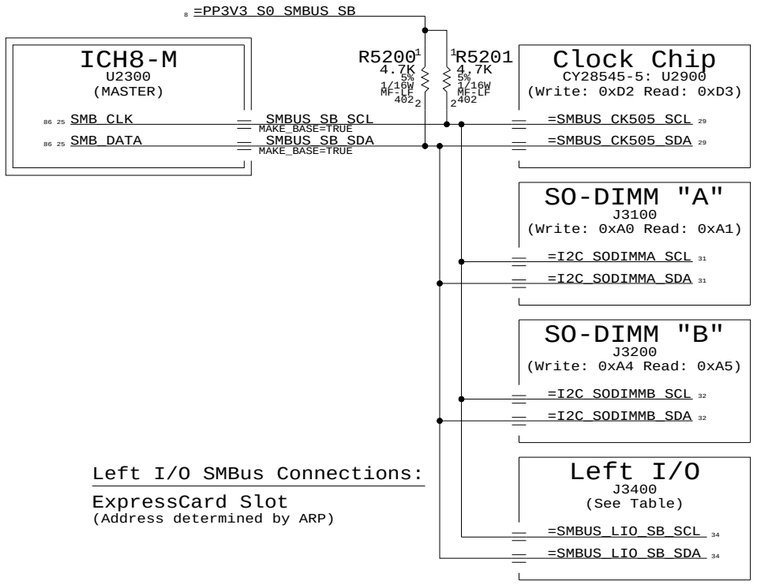
LPC+ Debug Connector

SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006

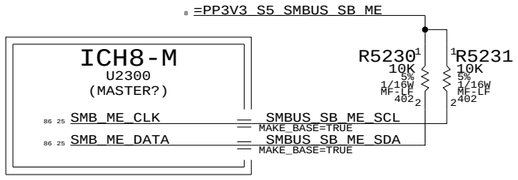
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 51 OF 109	

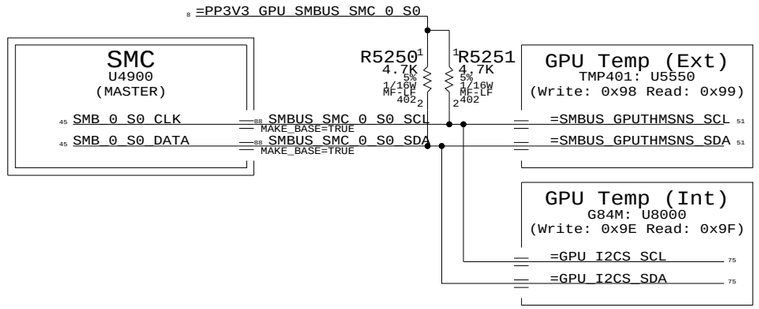
ICH8-M SMBus Connections



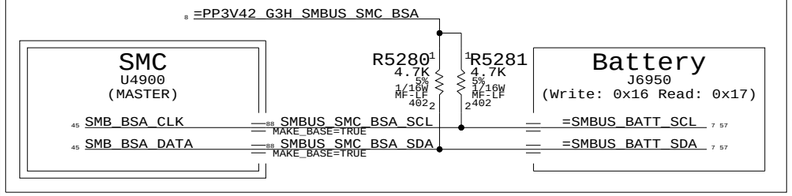
ICH8-M ME SMBus Connections



SMC "0" SMBus Connections

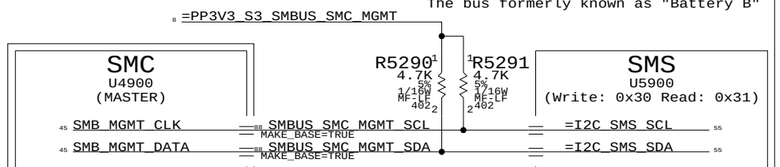


SMC "Battery A" SMBus Connections



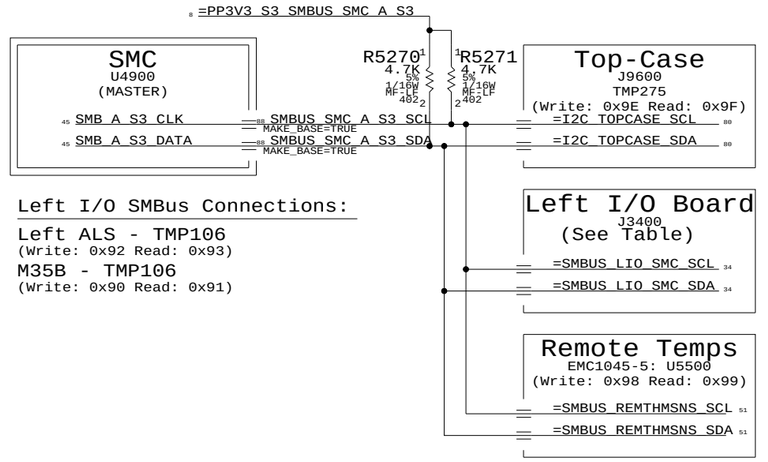
SMC "Management" SMBus Connections

The bus formerly known as "Battery B"

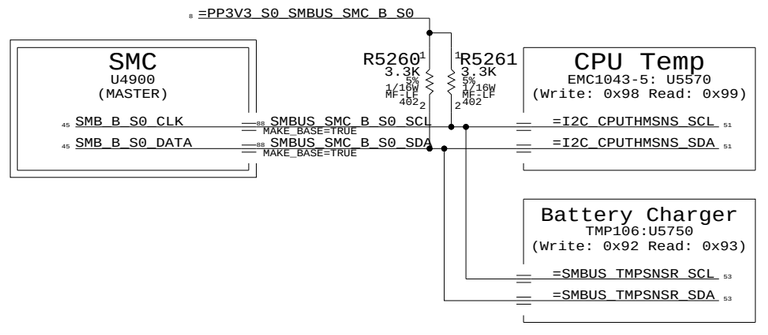


SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state



SMC "B" SMBus Connections



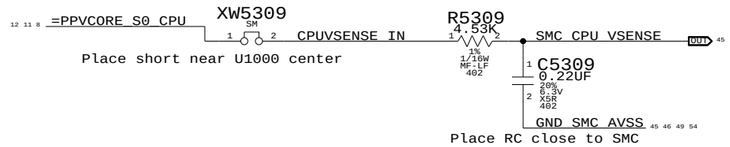
SMBus Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

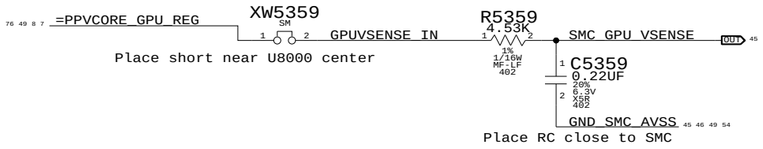
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 52 OF 109	

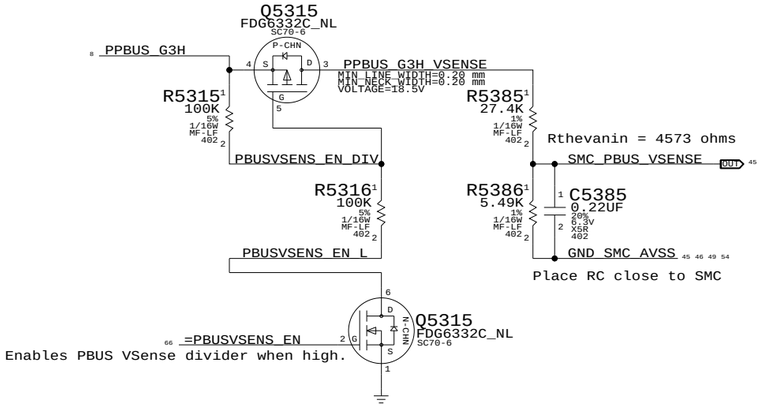
CPU Voltage Sense / Filter



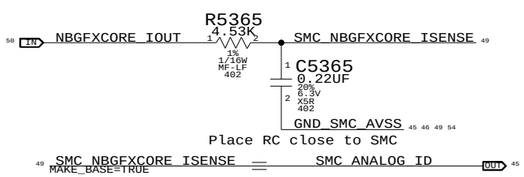
GPU Voltage Sense / Filter



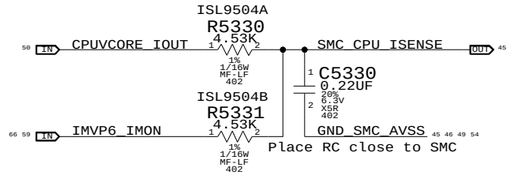
PBUS Voltage Sense & Filter



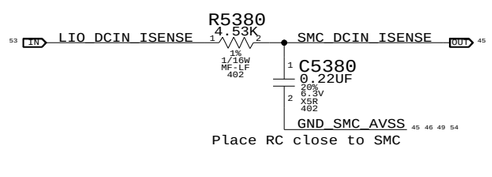
NB GFX Current Sense Filter



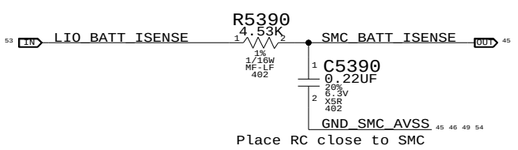
CPU Current Sense Filter



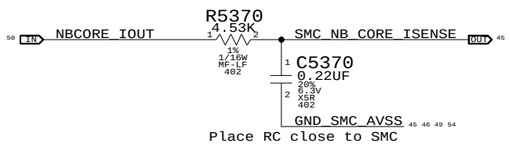
DCIN Current Sense Filter



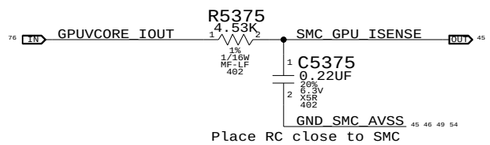
Battery (PBUS) Current Sense Filter



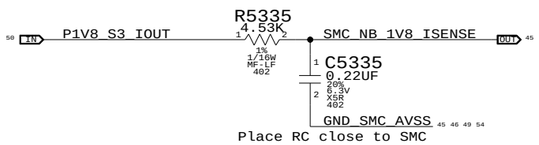
NB Core Current Sense Filter



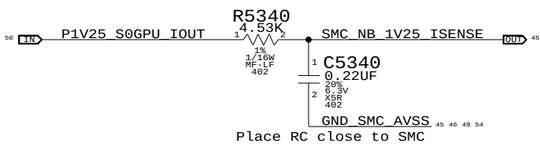
GPU Current Sense Filter



NB 1.8V Current Sense Filter

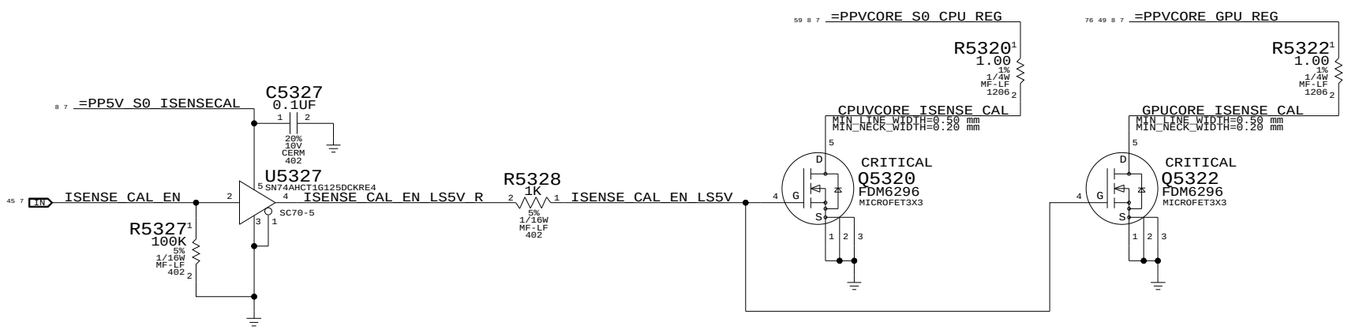


S0/GPU 1.25V Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits

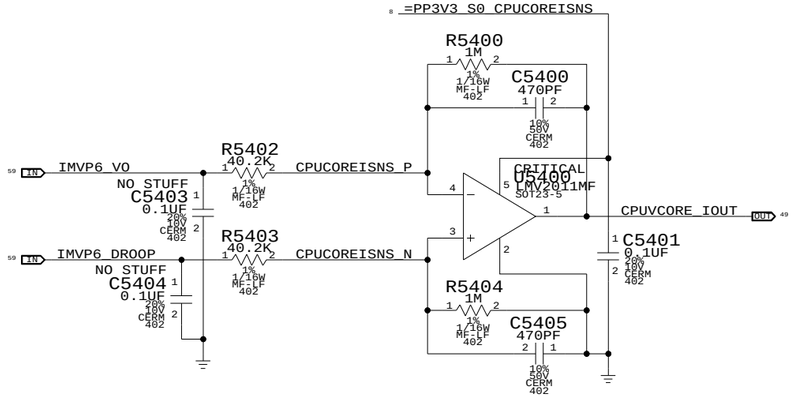


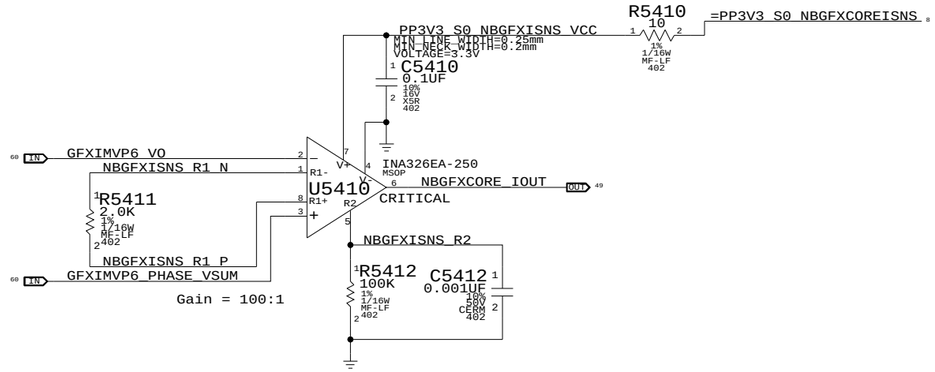
Current & Voltage Sensing

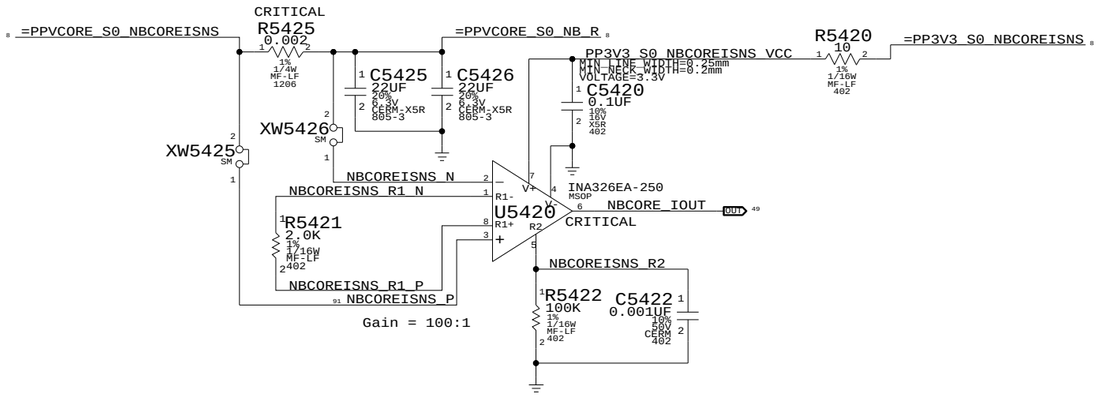
SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

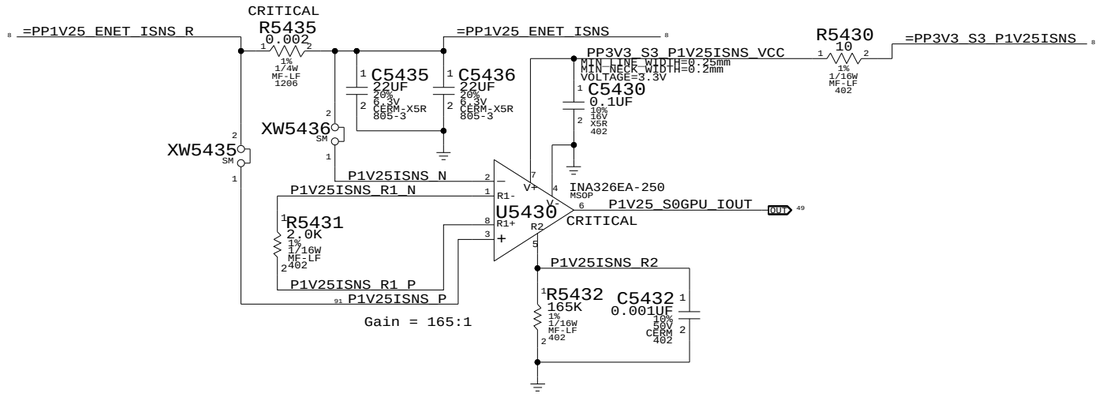
APPLE INC.

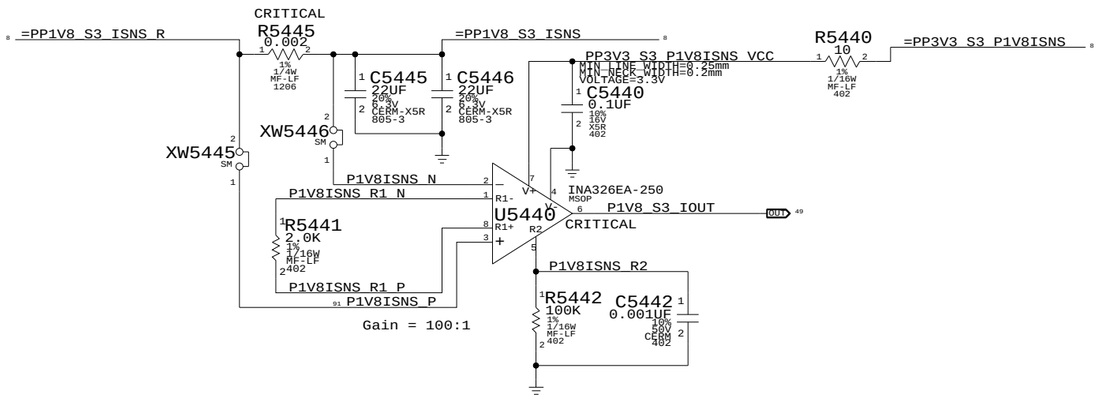
SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 53 OF 109	











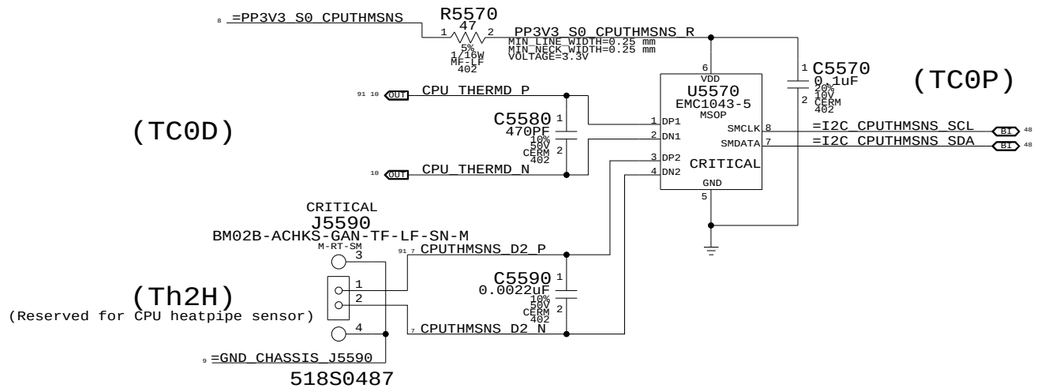
Current Sensing

SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 54 OF 109	

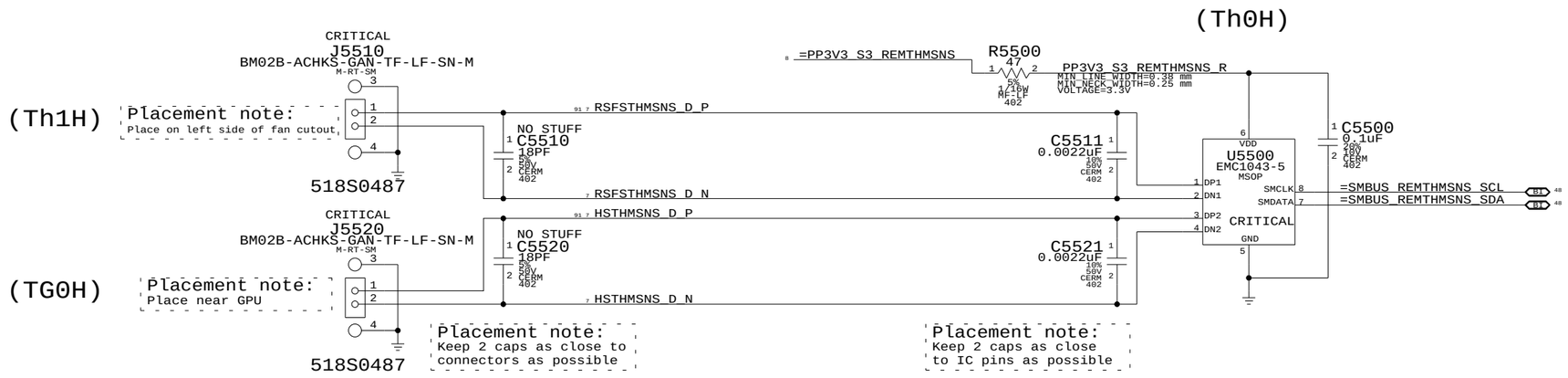
CPU T-Diode Thermal Sensor



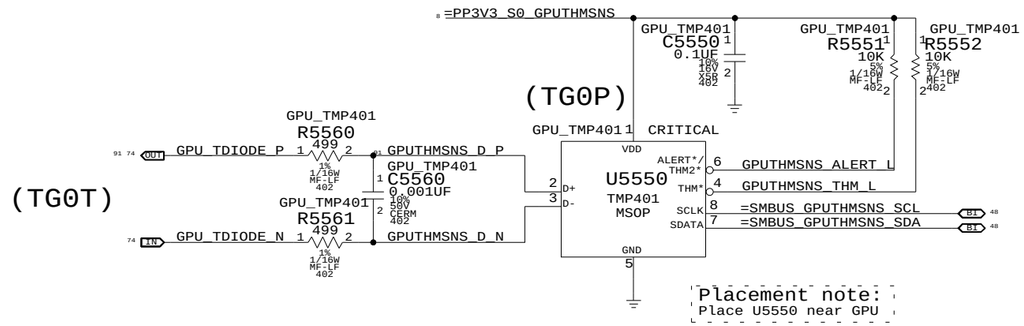
NB Thermal Diodes Not Used

=NB_TDB_FORCE
=NB_TDB_SENSE
=NB_TDE_SENSE
=NB_TDE_FORCE

GPU/Heat Pipe & Bottom Case Skin Thermal Sensor



GPU Die Thermal Sensor



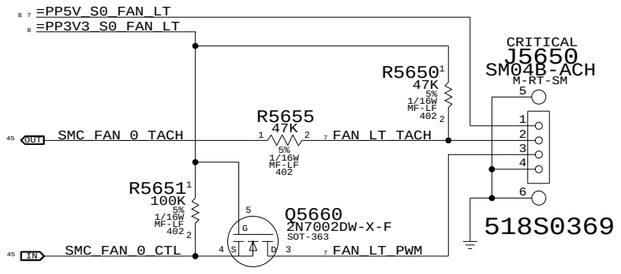
Thermal Sensors

SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

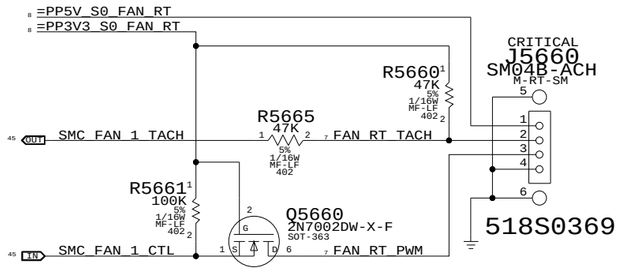
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 55 OF 109	

Left Fan



Right Fan



Fan Connectors

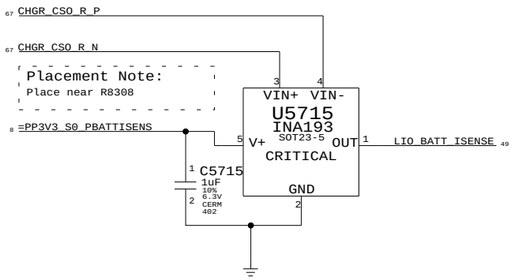
SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006

APPLE INC.

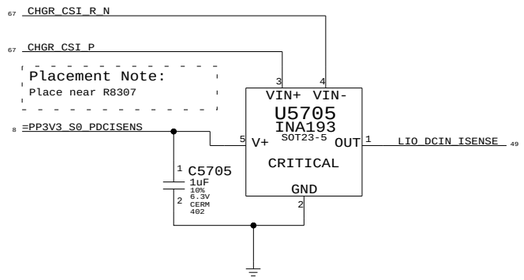
SIZE	DRAWING NUMBER	REV.
D	051-7520	B

SCALE	SHT	OF
NONE	56	109

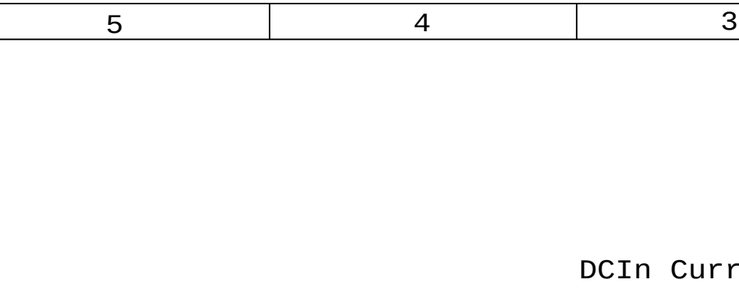
Battery Current Sense



DCIn Current Sense



Battery Charger Thermal Sensor



(Tm0P) R:0x93,W:0x92

Current & Thermal Sensors

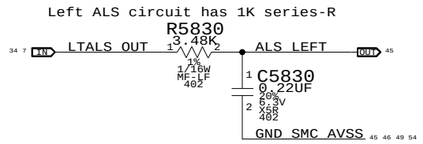
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

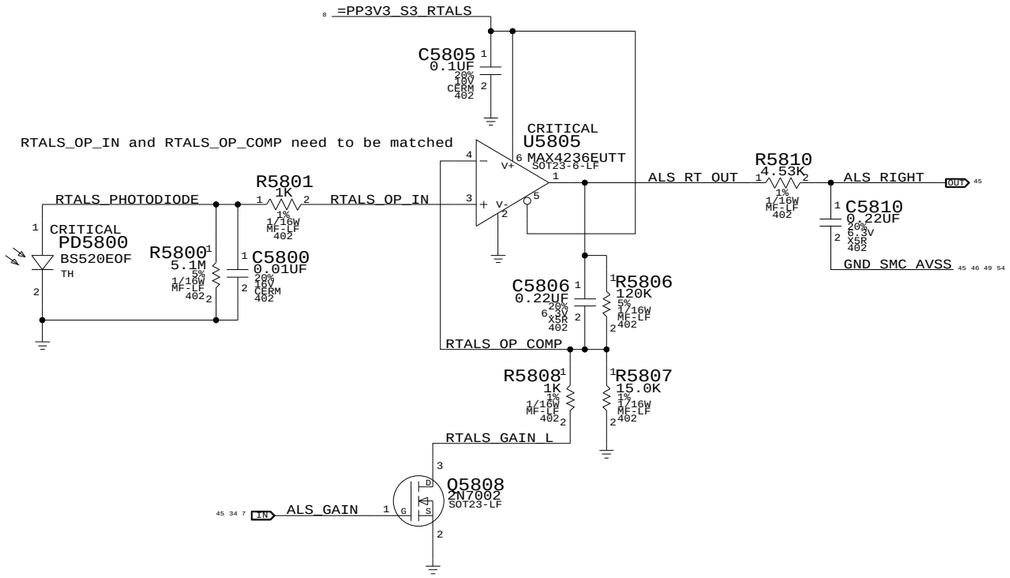
SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 57 OF 109	

Left ALS Filter

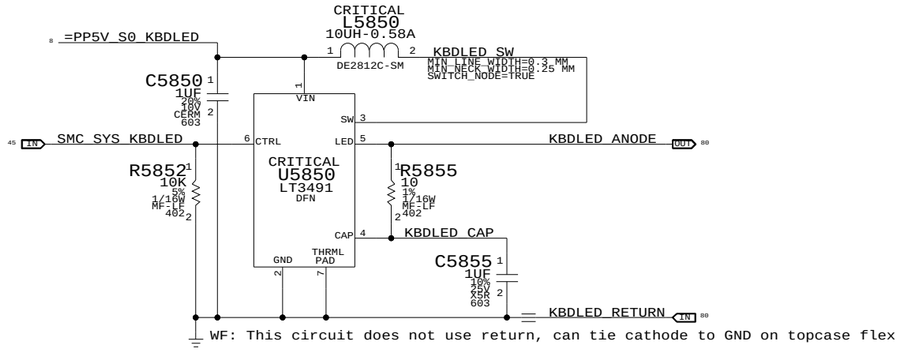
Left ALS circuit has 1K series-R



Right ALS Circuit



Keyboard LED Driver



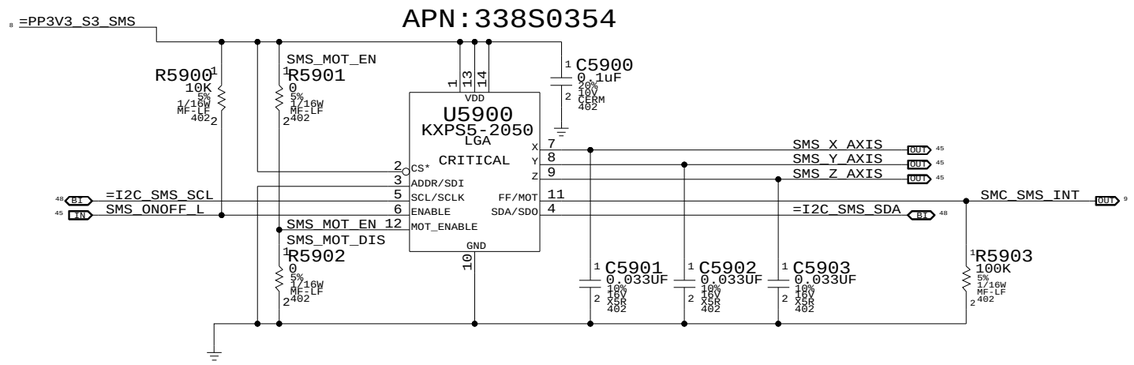
ALS Support

SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 58 OF 109	

APN:338S0354

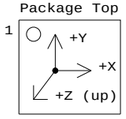


I2C addresses:

ADDR low => 0x30, 0x31
ADDR high => 0x32, 0x33
Alias SCL/SDA to GND if using analog outputs only

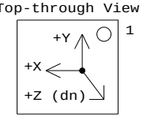
Desired orientation when placed on board top-side:

Package Top



Desired orientation when placed on board bottom-side:

Top-through View



Sudden Motion Sensor (SMS)

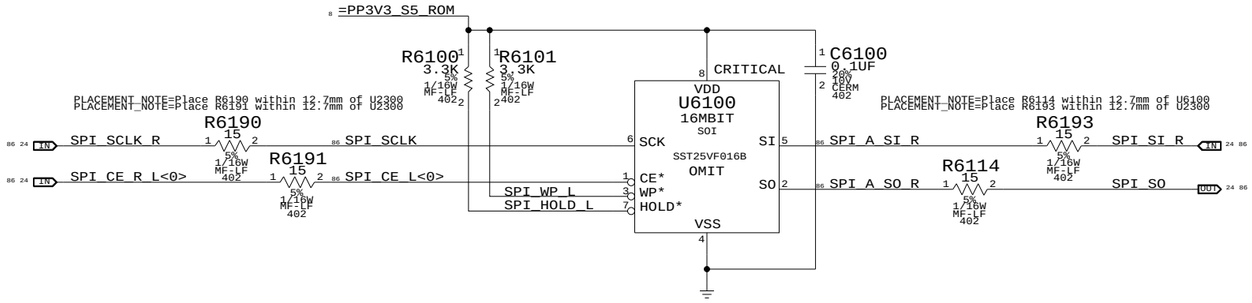
SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B

SCALE: NONE

SHT 59 OF 109



SPI BootROM

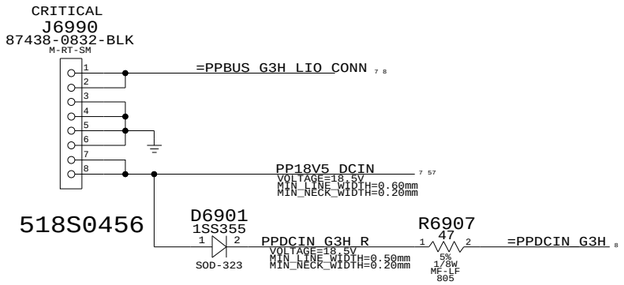
SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

APPLE INC.

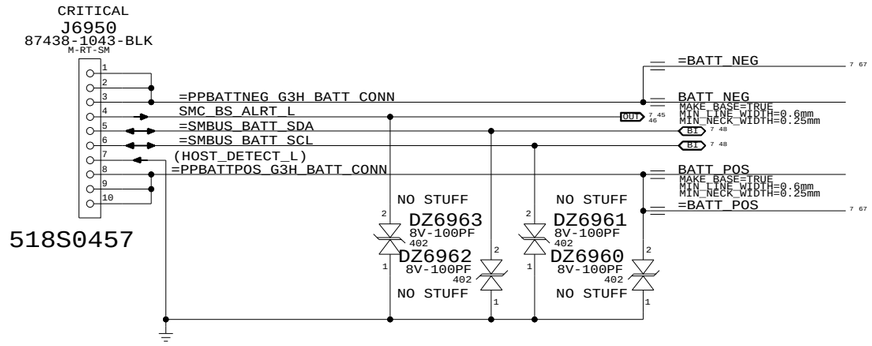
SIZE	DRAWING NUMBER	REV.
D	051-7520	B

SCALE	SHT	OF
NONE	61	109

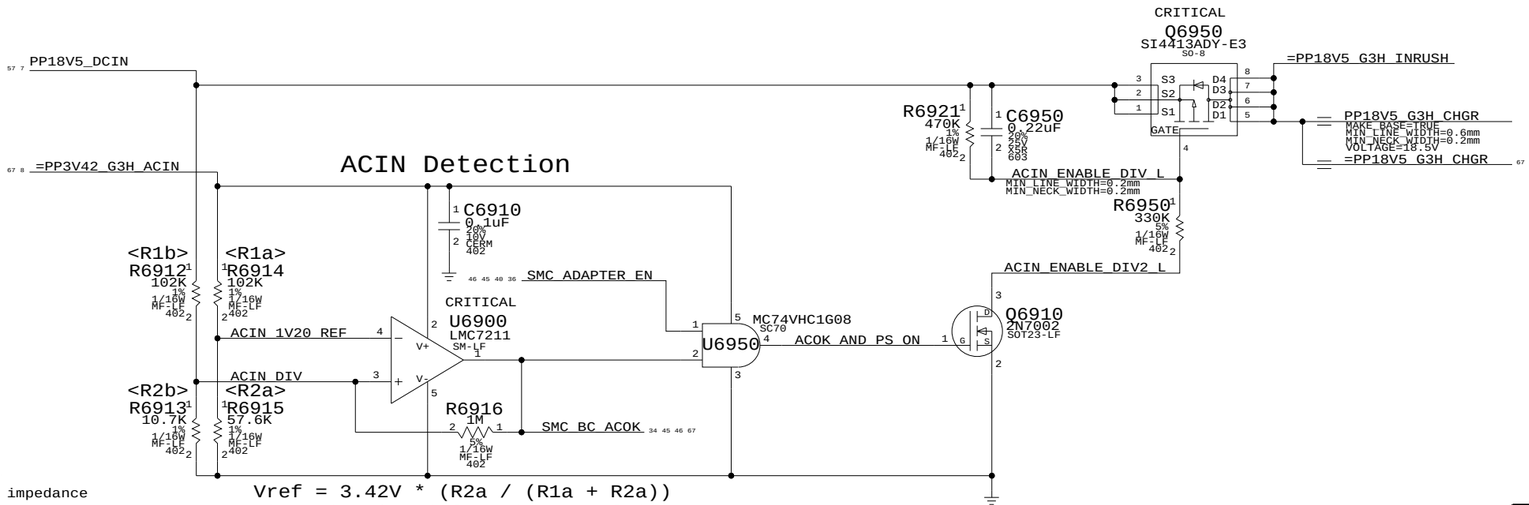
DC-In Connector



Battery Connector



Inrush Limiter



NOTE: R6910 is on LIO.
System must provide 10K-70K impedance
to A52 adapter for system load detection.
REQ of R6910 (on LIO), R6912, & R6913 is 36.9K.

Vref = 3.42V * (R2a / (R1a + R2a))
Vth = (Vref / (R2b / (R1b + R2b))

Vref = 1.23V
Vth = 13.0V

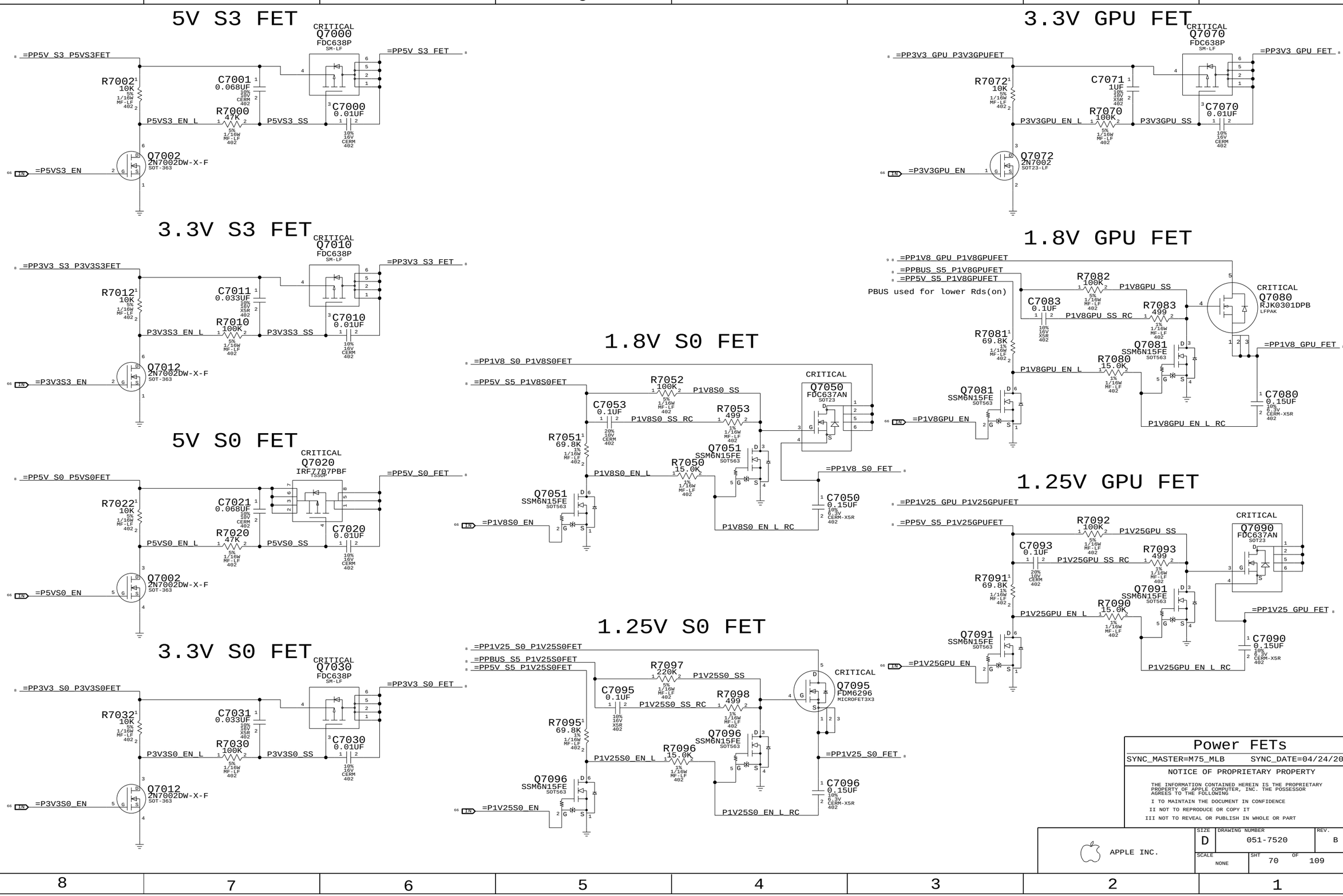
Assuming 1% variance for R6910-R6915 and 3.42V:
Worst case Vth: min:12.47V, max: 13.54V

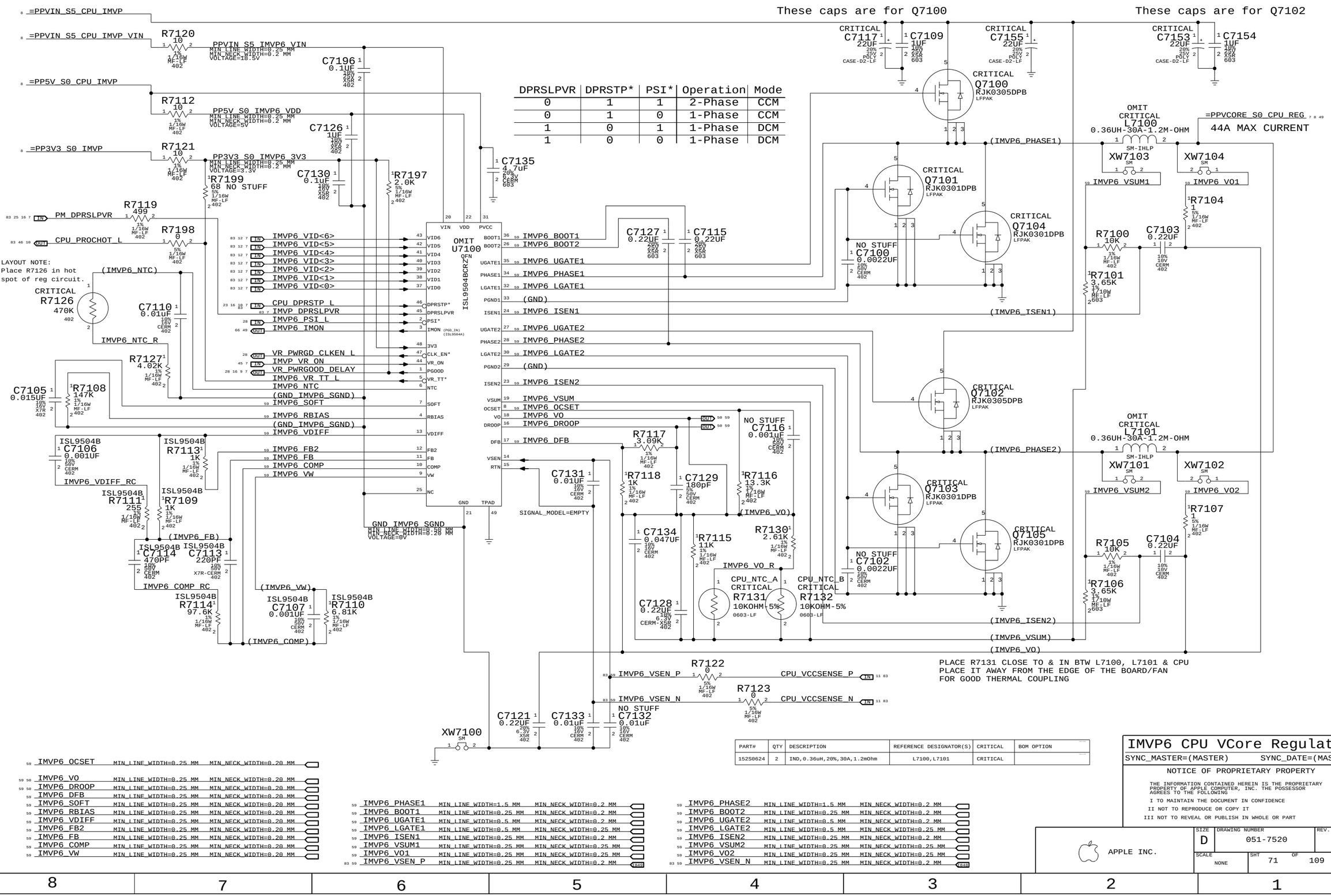
DC-In & Battery Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 69 OF 109	





DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM

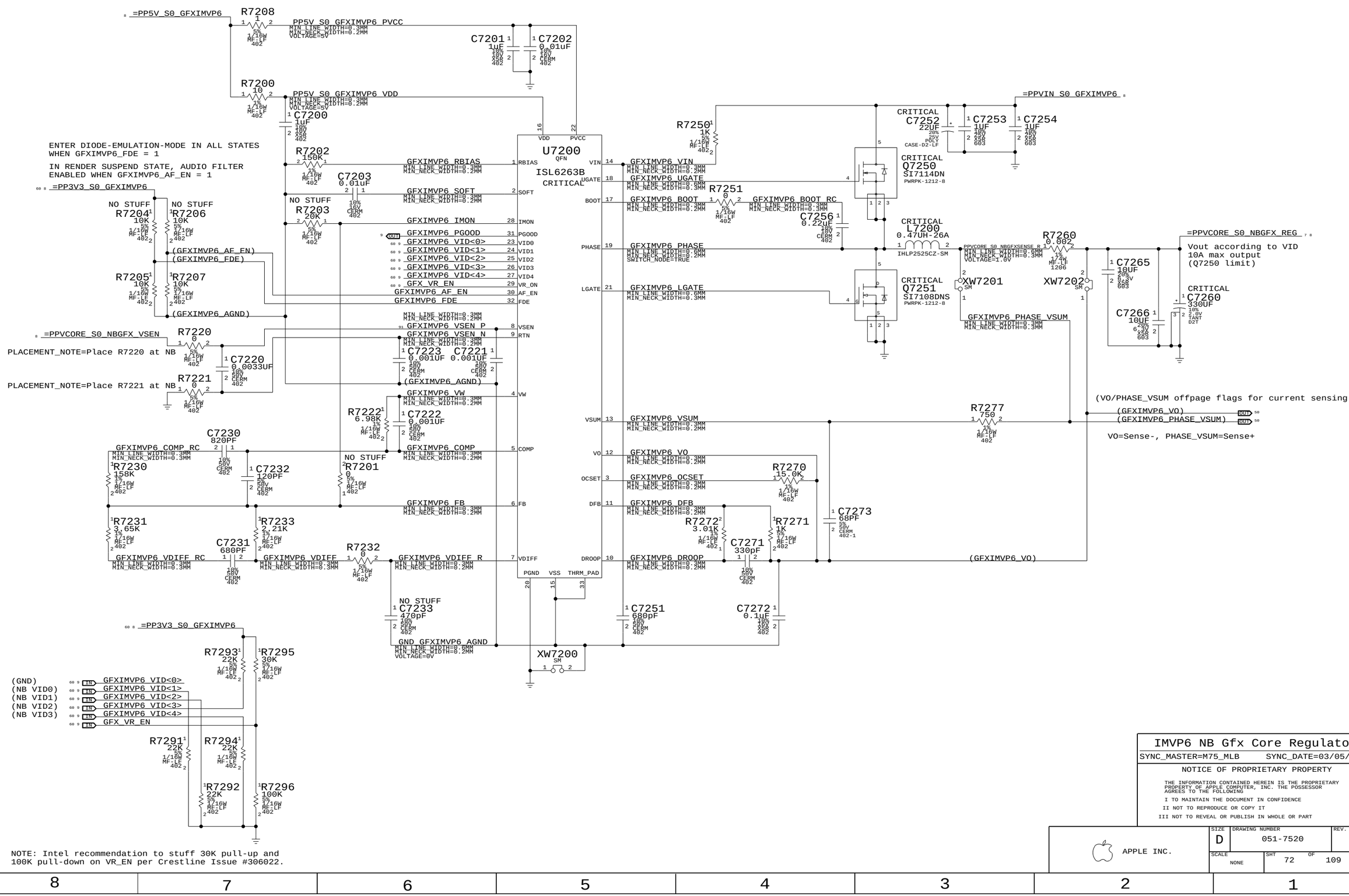
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S0624	2	IND,0.36uH,20%,30A,1.2mOhm	L7100,L7101	CRITICAL	

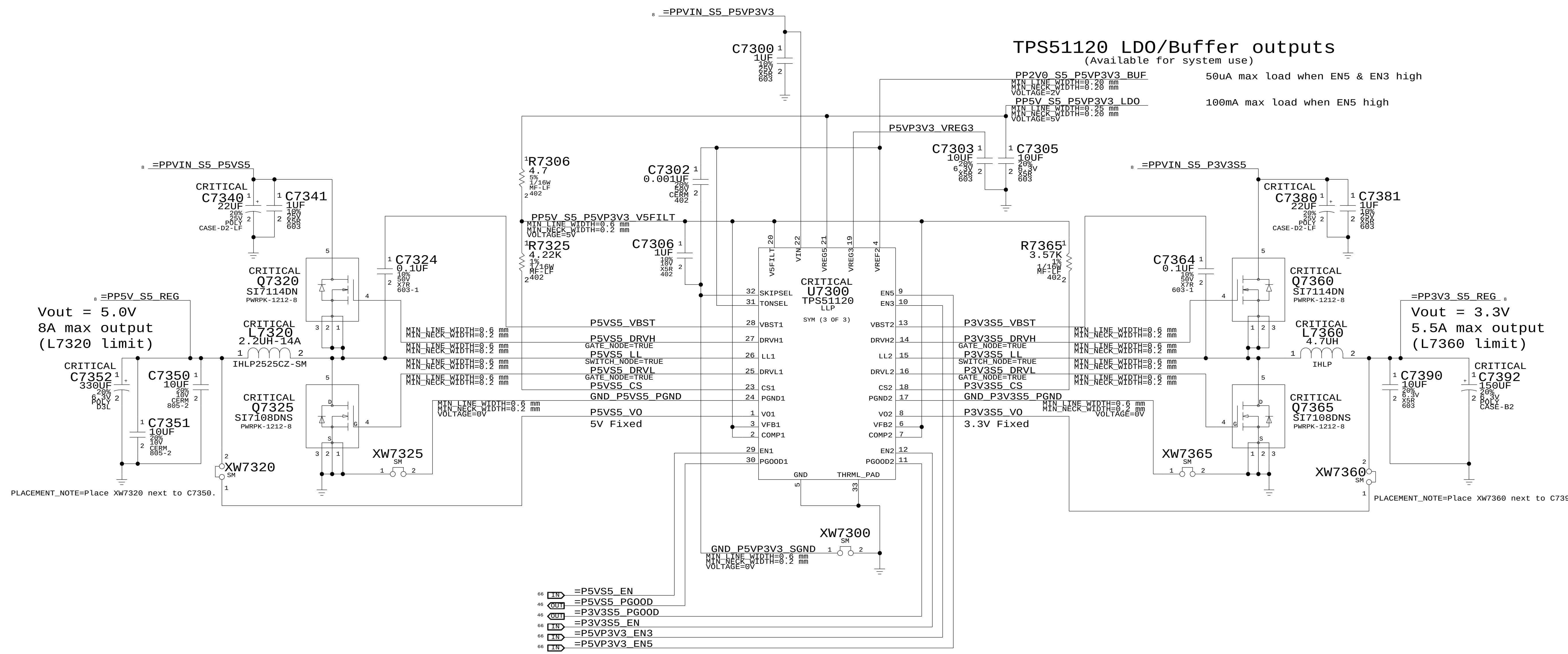
IMVP6 CPU VCore Regulator

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 71 OF 109	





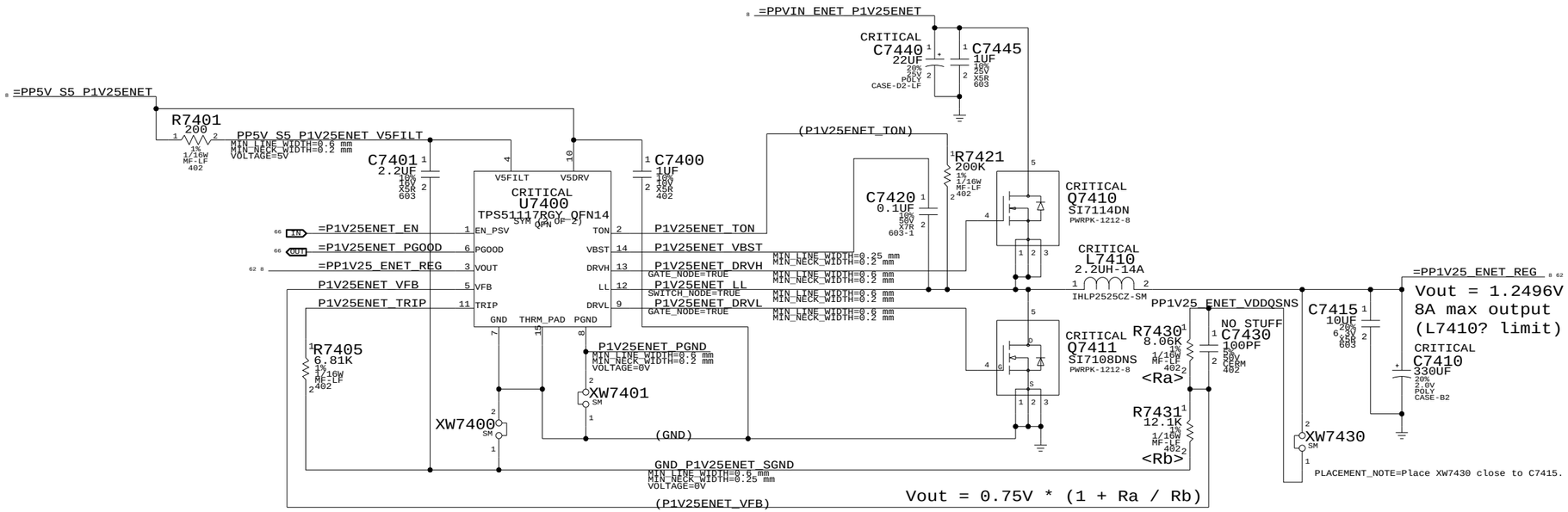
NOTE: EN5 can float or tie to VIN for automatic 5V LDO enable
EN3 can float or tie to VREG5 for automatic 3.3V LDO enable
When both are low TPS51120 VIN current drops from 100-150uA to 10-20uA.

5V / 3.3V Power Supply

SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE NONE	SHT 73	OF 109

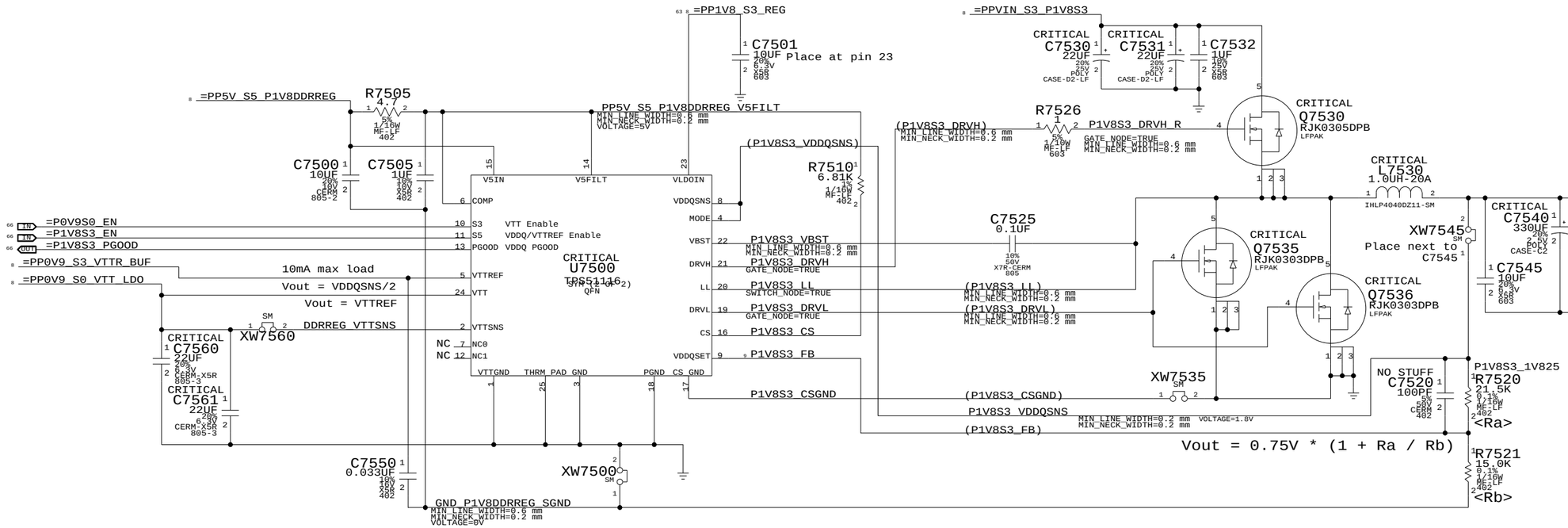


1.25V / 1.05V Power Supply

SYNC_MASTER=M75_MLB SYNC_DATE=03/05/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE	SHT	OF
NONE	74	109



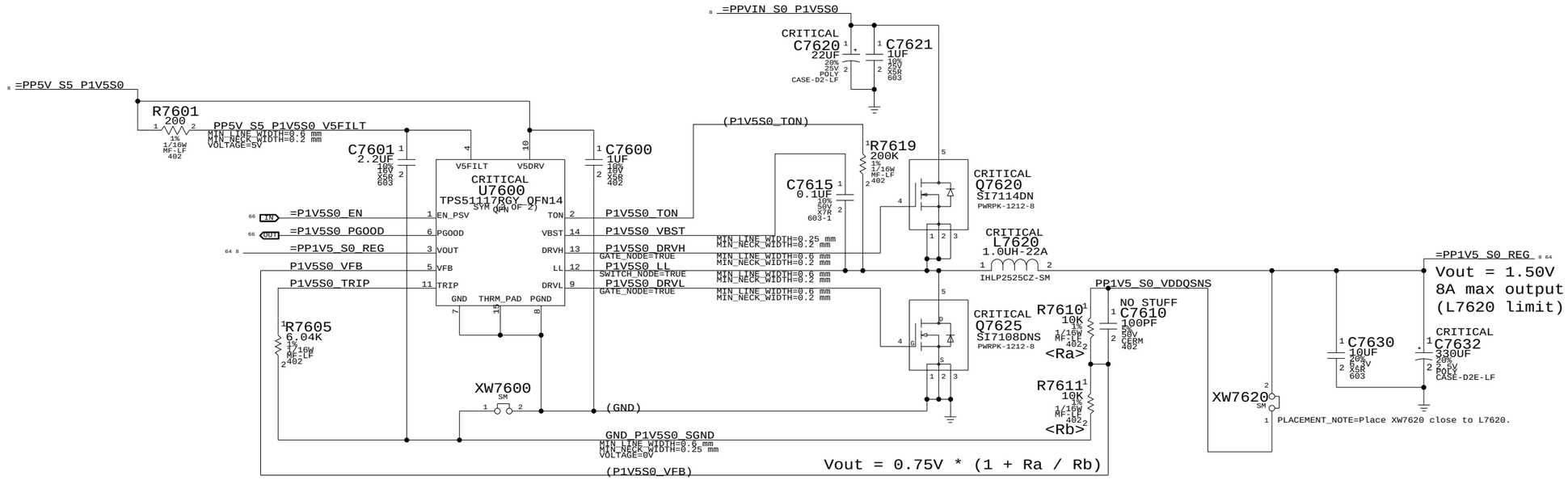
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
103S0192	1	RES,MTL FILM,21K,0.1,0402,SM,LF	R7520	CRITICAL	P1V8S3_1V8

1.8V DDR2 Supply

SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 75 OF 109	



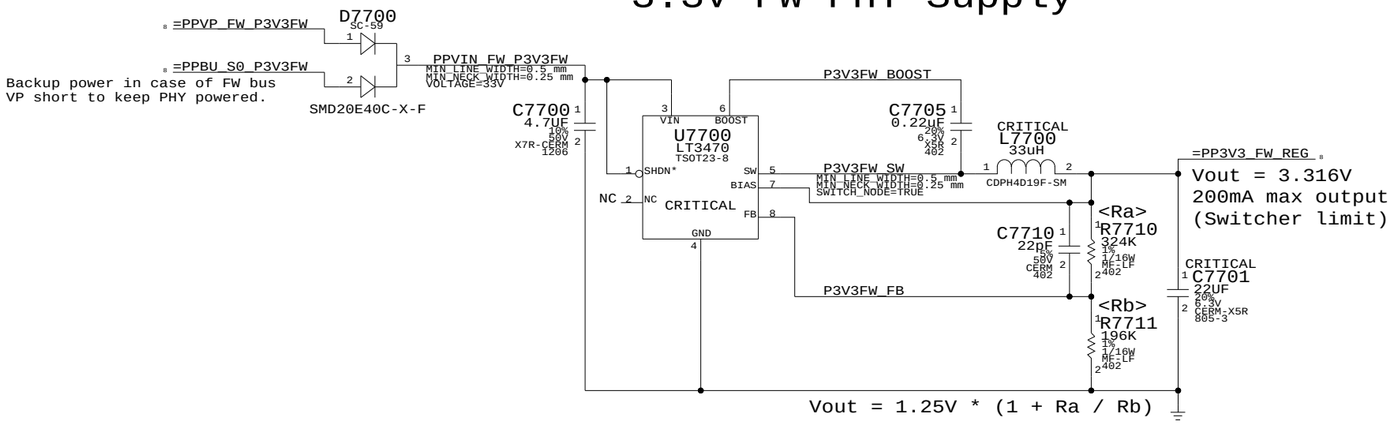
1.5V Power Supply

SYNC_MASTER=M75_MLB SYNC_DATE=03/05/2007

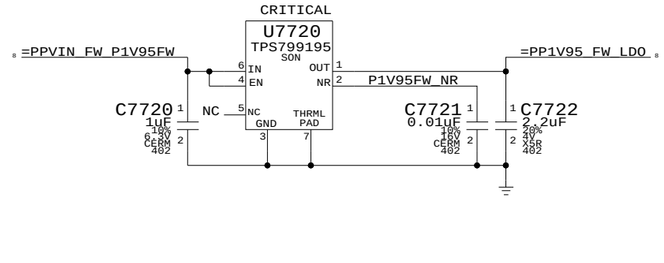
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 76 OF 109	

3.3V FW PHY Supply



1.95V FW PHY Supply



FW PHY Power Supplies

SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B

SCALE	SHT	OF
NONE	77	109

Power Control Signals

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

=PP5V_S5_PWRCTL

=PP3V3_GPU_PWRCTL

G84M GPU requires rails to come up in the following order:
1) 1.2V
2) 3.3V
3) Vcore
4) 1.8V

R7850 10K 5% 1/16W MF-LF 402
R7851 100K 5% 1/16W MF-LF 402
R7852 100K 5% 1/16W MF-LF 402
R7854 10K 5% 1/16W MF-LF 402

=GPUVCORE_PGOOD

Need to ensure that TPS51117 PGOOD does not deassert while GPU VIDs are changing GPU core voltage.

PM_GPUP1V8FET_EN — MAKE_BASE=TRUE — =P1V8GPU_EN

PM_GPUVCORE_EN — MAKE_BASE=TRUE — =GPUVCORE_EN

Q7850 2N7002DW-X-F SOT-363

Q7851 2N7002DW-X-F SOT-363

PVCOREGPU_EN_L

Q7851 2N7002DW-X-F SOT-363

PM_SLP_S3_LS5V — MAKE_BASE=TRUE — LIO_S0_EN_L

Q7850 2N7002DW-X-F SOT-363

PM_SLP_S3_L

R7856 100K 5% 1/16W MF-LF 402

(PM_SLP_S3_L) — MAKE_BASE=TRUE

=P5VS0_EN
=P3V3S0_EN
=P1V8S0_EN
=P1V25S0_EN
=P0V9S0_EN
=PBUSVSENS_EN
=ENET_VMAIN_AVLBL
=PM_SLP_S3_DELAY_L

R7853 10K 5% 1/16W MF-LF 402

=PP3V3_S0_PWRCTL

=PP3V3_S5_PWRCTL

U7850 MC74VHC1G09 SC70

PM_SLP_S3_DELAY_L — MAKE_BASE=TRUE

R7859 10K 5% 1/16W MF-LF 402

NO STUFF C7859 0.047UF 10% 10V CERM 402

=P1V5S0_EN
=P1V05S0_EN

EXTGPU_PWR_EN

(EXTGPU_PWR_EN) — MAKE_BASE=TRUE

=PVCOREGPU_EN
=P3V3GPU_EN
=P1V25GPU_EN

SB GPIO has ability to force all GPU rails off
R7853 acts as pull-up for open-drain GPIO.

NO STUFF C7853 0.047UF 10% 10V CERM 402

Fast wake glitch filter. Should not be necessary to stuff if GPU supplies and PGOOD revalidate before 99ms SMC timer expires.

PP1V2_GPU needs to ramp first via RC control

PM_ENET_EN

(PM_ENET_EN) — MAKE_BASE=TRUE

=P3V3ENET_EN
=P1V25ENET_EN

PM_S4_STATE_L

(PM_S4_STATE_L) — MAKE_BASE=TRUE

=P3V3S3_EN
=P5VS3_EN
=USB_EXTA_EN
LIO_S3_EN

R7857 10K 5% 1/16W MF-LF 402

R7855 10K 5% 1/16W MF-LF 402

P1V8S3_EN — MAKE_BASE=TRUE — =P1V8S3_EN

C7855 0.47UF 10% 6.3V CERM-X5R 402

=PP3V42_G3H_PWRCTL

NO STUFF

SMC_PM_G2_EN

U7858 MC74VHC1G09 SC70

PM_G2_EN — MAKE_BASE=TRUE

=P5VS5_EN
=P3V3S5_EN
=P5VP3V3_EN5
=P5VP3V3_EN3

R7858 100K 5% 1/16W MF-LF 402

R7860 0 5% 1/16W MF-LF 402

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

=PPVIN_G3H_P3V42G3H

P3V42G3H5_BOOST

C7800 10UF 20% 16V X5R 1206-1

U7800 LT3470 TSOT23-8

C7805 0.22UF 20% 50V X5R 402

CRITICAL L7810 33UH-0.39A S1024AS-SM

=PP3V42_G3H_REG

Vout = 3.425
200mA max output
(Switcher limit)

SHDN*
NC
NC CRITICAL
VIN
BOOST
SW
BIAS
FB
GND

P3V42G3H_SW — MIN_LINE_WIDTH=0.5 mm — MIN_NECK_WIDTH=0.25 mm — SWITCH_NODE=TRUE

C7810 22PF 5% 50V CERM 402

<Ra> R7810 348K 1% 1/16W MF-LF 402

<Rb> R7811 200K 1% 1/16W MF-LF 402

C7815 22UF 20% 6.3V CERM-X5R 805-3

P3V42G3H_FB

Vout = 1.25V * (1 + Ra / Rb)

Unused PGOOD Signals

=P1V25ENET_PGOOD — MAKE_BASE=TRUE — TP_P1V25ENET_PGOOD

=P1V8S3_PGOOD — MAKE_BASE=TRUE — TP_P1V8S3_PGOOD

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

IMVP6_IMON — To CPU IMVP6

=PP3V3_S5_P1V5P1V05PG

ISL9504A

R7865 100K 5% 1/16W MF-LF 402

R7866 0 5% 1/16W MF-LF 402

=PP3V3_S0_ALLSYSPG

C7880 0.1UF 20% 16V CERM 402

=P1V5S0_PGOOD
TPS51117 PGOOD threshold 92.5-97.5% (1.36 - 1.46V)

=P1V05S0_PGOOD
TPS51117 PGOOD threshold 92.5-97.5% (0.98 - 1.02V)

P1V5P1V05S0_PGOOD — MAKE_BASE=TRUE

U7880 MC74VHC1G08 SC70

ALL_SYS_PWRGD

NOTE: 0.9V/2.5V is not checked!

Other S0 Rails PWRGD Circuit

Does not include GFX rails

PP5V_S0
PP3V3_S0
PP1V8_S0
PP1V25_S0

R7873 124K 1% 1/16W MF-LF 402

C7872 0.1UF 20% 10V CERM 402

C7871 0.1UF 20% 10V CERM 402

C7870 0.1UF 20% 10V CERM 402

R7875 10K 5% 1/16W MF-LF 402

CRITICAL U7870 LTC2900 DFN

V1 V2 V3 V4 VREF VPG GND THRM_PAD PBR* RST* CRT

NC

S0PGOOD_P1V2_DIV

S0PGOOD_VREF

S0PGOOD_VPG

S0PGOOD_PWROK

S0PGOOD_CRT

R7874 100K 1% 1/16W MF-LF 402

R7870 9.53K 1% 1/16W MF-LF 402

R7871 93.1K 1% 1/16W MF-LF 402

C7873 0.1UF 20% 10V CERM 402

C7875 0.047UF 10% 6.3V CERM 402

Trst = 4.6ms/nF
Trst = 216ms

LTC2900 typical threshold is 93.5% (4.675V, 3.086V, 1.685V, 1.120V)

3.425V G3Hot Supply & Power Control		
SYNC_MASTER=M75_MLB	SYNC_DATE=04/02/2007	

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7520	B
	SCALE: NONE	SHT 78 OF 109	

PBus Supply & Battery Charger

Energy Star LDO

Battery Charge FETs

Adapter Input Current Limit

As shown, Isys =~4.6A max

Battery Charge Current Limit

As shown, Ichg = 4.5A max

VOLTAGE FOLLOWER GUARANTEES CURRENT LIMIT CIRCUITS ARE PROVIDED WITH SUFFICIENT CURRENT WITHOUT SINKING CURRENT FROM VREF.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1510	1	ISL6257H,BATT CHGR,28P,QFN,LF	U7900	CRITICAL	ISL6257H
116S0004	1	0 OHM,5%,1/16W,0402,SMD,LF	R7904		ISL6257H

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
107S0110	1	RES,MTL FILM,27OHM,5%,3W	R7920	CRITICAL	

PBus Supply & Batt. Charger

SYNC_MASTER=M75_LIO SYNC_DATE=03/08/2007

APPLE INC.

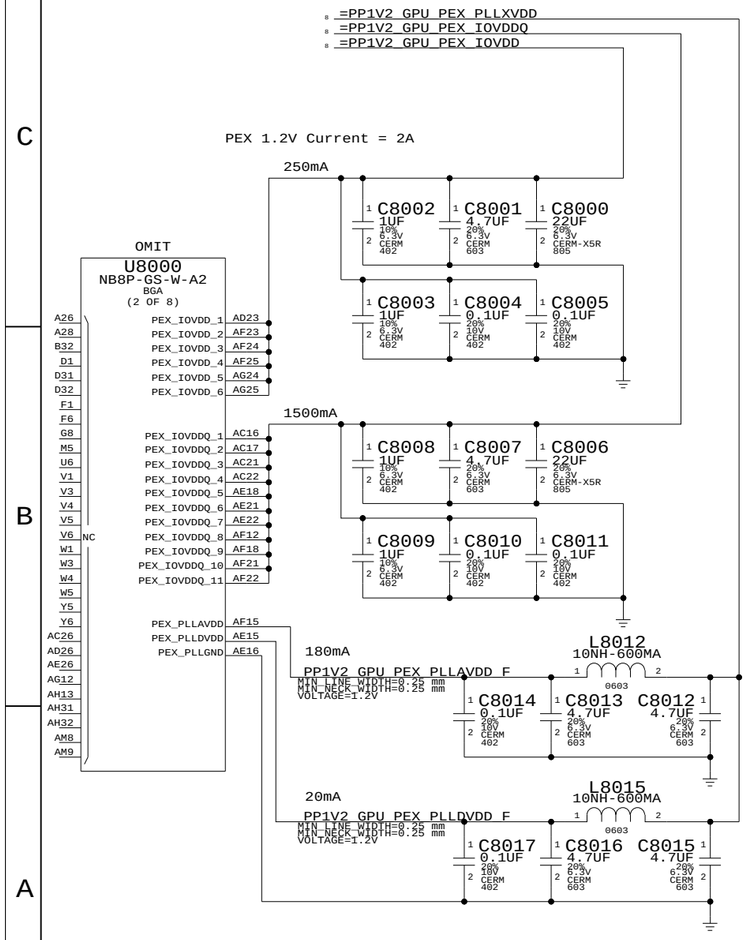
SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 79 OF 109	

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



OMIT
U8000
NB8P-GS-W-A2
BGA
(1 OF 8)

PCI-EXPRESS BUS INTERFACE

PEG_R2D_C_P<0>	C8020 0.1uF	PEG_R2D_P<0>	AK13	PEX_RX0	PEX_TX0	AJ15	PEG_D2R_C_P<0>
PEG_R2D_C_N<0>	C8021 0.1uF	PEG_R2D_N<0>	AK14	PEX_RX0_L	PEX_TX0_L	AK15	PEG_D2R_C_N<0>
PEG_R2D_C_P<1>	C8022 0.1uF	PEG_R2D_P<1>	AM14	PEX_RX1	PEX_TX1	AH16	PEG_D2R_C_P<1>
PEG_R2D_C_N<1>	C8023 0.1uF	PEG_R2D_N<1>	AM15	PEX_RX1_L	PEX_TX1_L	AG16	PEG_D2R_C_N<1>
PEG_R2D_C_P<2>	C8024 0.1uF	PEG_R2D_P<2>	AL15	PEX_RX2	PEX_TX2	AG17	PEG_D2R_C_P<2>
PEG_R2D_C_N<2>	C8025 0.1uF	PEG_R2D_N<2>	AL16	PEX_RX2_L	PEX_TX2_L	AH17	PEG_D2R_C_N<2>
PEG_R2D_C_P<3>	C8026 0.1uF	PEG_R2D_P<3>	AK16	PEX_RX3	PEX_TX3	AG18	PEG_D2R_C_P<3>
PEG_R2D_C_N<3>	C8027 0.1uF	PEG_R2D_N<3>	AK17	PEX_RX3_L	PEX_TX3_L	AH18	PEG_D2R_C_N<3>
PEG_R2D_C_P<4>	C8028 0.1uF	PEG_R2D_P<4>	AL17	PEX_RX4	PEX_TX4	AK18	PEG_D2R_C_P<4>
PEG_R2D_C_N<4>	C8029 0.1uF	PEG_R2D_N<4>	AL18	PEX_RX4_L	PEX_TX4_L	AJ18	PEG_D2R_C_N<4>
PEG_R2D_C_P<5>	C8030 0.1uF	PEG_R2D_P<5>	AM18	PEX_RX5	PEX_TX5	AJ19	PEG_D2R_C_P<5>
PEG_R2D_C_N<5>	C8031 0.1uF	PEG_R2D_N<5>	AM19	PEX_RX5_L	PEX_TX5_L	AH19	PEG_D2R_C_N<5>
PEG_R2D_C_P<6>	C8032 0.1uF	PEG_R2D_P<6>	AK19	PEX_RX6	PEX_TX6	AG20	PEG_D2R_C_P<6>
PEG_R2D_C_N<6>	C8033 0.1uF	PEG_R2D_N<6>	AK20	PEX_RX6_L	PEX_TX6_L	AH20	PEG_D2R_C_N<6>
PEG_R2D_C_P<7>	C8034 0.1uF	PEG_R2D_P<7>	AL20	PEX_RX7	PEX_TX7	AG21	PEG_D2R_C_P<7>
PEG_R2D_C_N<7>	C8035 0.1uF	PEG_R2D_N<7>	AL21	PEX_RX7_L	PEX_TX7_L	AH21	PEG_D2R_C_N<7>
PEG_R2D_C_P<8>	C8036 0.1uF	PEG_R2D_P<8>	AM21	PEX_RX8	PEX_TX8	AK21	PEG_D2R_C_P<8>
PEG_R2D_C_N<8>	C8037 0.1uF	PEG_R2D_N<8>	AM22	PEX_RX8_L	PEX_TX8_L	AJ21	PEG_D2R_C_N<8>
PEG_R2D_C_P<9>	C8038 0.1uF	PEG_R2D_P<9>	AK22	PEX_RX9	PEX_TX9	AJ22	PEG_D2R_C_P<9>
PEG_R2D_C_N<9>	C8039 0.1uF	PEG_R2D_N<9>	AK23	PEX_RX9_L	PEX_TX9_L	AH22	PEG_D2R_C_N<9>
PEG_R2D_C_P<10>	C8040 0.1uF	PEG_R2D_P<10>	AL23	PEX_RX10	PEX_TX10	AG23	PEG_D2R_C_P<10>
PEG_R2D_C_N<10>	C8041 0.1uF	PEG_R2D_N<10>	AL24	PEX_RX10_L	PEX_TX10_L	AH23	PEG_D2R_C_N<10>
PEG_R2D_C_P<11>	C8042 0.1uF	PEG_R2D_P<11>	AM24	PEX_RX11	PEX_TX11	AK24	PEG_D2R_C_P<11>
PEG_R2D_C_N<11>	C8043 0.1uF	PEG_R2D_N<11>	AM25	PEX_RX11_L	PEX_TX11_L	AJ24	PEG_D2R_C_N<11>
PEG_R2D_C_P<12>	C8044 0.1uF	PEG_R2D_P<12>	AK25	PEX_RX12	PEX_TX12	AJ25	PEG_D2R_C_P<12>
PEG_R2D_C_N<12>	C8045 0.1uF	PEG_R2D_N<12>	AK26	PEX_RX12_L	PEX_TX12_L	AH25	PEG_D2R_C_N<12>
PEG_R2D_C_P<13>	C8046 0.1uF	PEG_R2D_P<13>	AL26	PEX_RX13	PEX_TX13	AH26	PEG_D2R_C_P<13>
PEG_R2D_C_N<13>	C8047 0.1uF	PEG_R2D_N<13>	AL27	PEX_RX13_L	PEX_TX13_L	AG26	PEG_D2R_C_N<13>
PEG_R2D_C_P<14>	C8048 0.1uF	PEG_R2D_P<14>	AM27	PEX_RX14	PEX_TX14	AK27	PEG_D2R_C_P<14>
PEG_R2D_C_N<14>	C8049 0.1uF	PEG_R2D_N<14>	AM28	PEX_RX14_L	PEX_TX14_L	AJ27	PEG_D2R_C_N<14>
PEG_R2D_C_P<15>	C8050 0.1uF	PEG_R2D_P<15>	AL28	PEX_RX15	PEX_TX15	AJ28	PEG_D2R_C_P<15>
PEG_R2D_C_N<15>	C8051 0.1uF	PEG_R2D_N<15>	AL29	PEX_RX15_L	PEX_TX15_L	AH27	PEG_D2R_C_N<15>
PEG_CLK100M_GPU_P			AH14	PEX_REFCLK	PEX_TSTCLK_OUT	AM12	TP_GPU_PEXTSTCLK_P
PEG_CLK100M_GPU_N			AJ14	PEX_REFCLK_L	PEX_TSTCLK_OUT_L	AM11	TP_GPU_PEXTSTCLK_N
GPU_RESET_L			AH15	PEX_RST_L			

All C8055–C8086 0.1uF: 10% 16V X5R 402

NV G84M PCI-E

SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 80 OF 109	

Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

=PPVCORE_GPU

???A @ ???/???MHz Core/Mem Clk for VDD

C8100 1UF 20% 10V CERM 402
C8101 1UF 20% 10V CERM 402
C8102 1UF 20% 10V CERM 402
C8103 0.1UF 20% 10V CERM 402
C8104 0.1UF 20% 10V CERM 402
C8105 0.1UF 20% 10V CERM 402
C8106 0.1UF 20% 10V CERM 402
C8107 0.1UF 20% 10V CERM 402
C8108 0.1UF 20% 10V CERM 402
C8109 0.1UF 20% 10V CERM 402
C8110 0.1UF 20% 10V CERM 402
C8111 0.1UF 20% 10V CERM 402
C8112 0.1UF 20% 10V CERM 402
C8113 0.1UF 20% 10V CERM 402
C8114 0.1UF 20% 10V CERM 402
C8115 0.1UF 20% 10V CERM 402
C8116 0.1UF 20% 10V CERM 402
C8117 0.1UF 20% 10V CERM 402
C8118 0.1UF 20% 10V CERM 402
C8119 0.1UF 20% 10V CERM 402
C8120 0.1UF 20% 10V CERM 402
C8121 0.1UF 20% 10V CERM 402
C8122 0.1UF 20% 10V CERM 402

OMIT
U8000
NB8P-GS-W-A2
BGA
(7 OF 8)

K16 K17 N13 N14 N16 N17 N19 P13 P14 P16 P17 P19 R16 R17 T13 T14 T15 T18 T19 U13 U14 U15 U18 U19 V16 V17 W13 W14 W16 W17 W19 Y13 Y14 Y16 Y17 Y19 Y20 → VDD

P20 T20 T23 U20 U23 W20 → VDD_LP

TP_GPU_VDD_SENSE N20 → VDD_SENSE
TP_GPU_GND_SENSE M21 → GND_SENSE

A12 A18 A21 A24 A27 A3 A30 A6 A9 AA32 AD32 AG32 AK32 C32 F32 J32 M32 R32 → FBVDD

AA25 AA26 AB25 AB26 G11 G12 G15 G18 G21 G22 H11 H12 H15 H18 H21 H22 L25 L26 M25 M26 R25 R26 V25 V26 → FBVDDQ

AA23 NC
AB23 NC
H16 NC
H17 NC
J10 NC
J23 NC
J24 NC
J9 NC
K11 NC
K12 NC
K21 NC
K22 NC
K24 NC
K9 NC
L23 NC
M23 NC
T25 NC
U25 NC

=PP1V8_GPU_FBVDDQ

???A @ ???MHz 1.8V GDDR3

C8150 4.7UF 20% 6.3V CERM 603
C8151 4.7UF 20% 6.3V CERM 603
C8156 0.1UF 10% 10V CERM 402
C8157 0.1UF 10% 10V CERM 402
C8158 0.1UF 10% 10V CERM 402
C8159 0.1UF 10% 10V CERM 402
C8160 0.47UF 10% 6.3V CERM-X5R 402
C8161 0.47UF 10% 6.3V CERM-X5R 402
C8162 0.1UF 10% 10V CERM 402
C8163 0.1UF 10% 10V CERM 402
C8164 0.1UF 10% 10V CERM 402
C8165 0.1UF 10% 10V CERM 402
C8166 0.47UF 10% 6.3V CERM-X5R 402
C8167 0.47UF 10% 6.3V CERM-X5R 402
C8168 0.47UF 10% 6.3V CERM-X5R 402
C8169 0.47UF 10% 6.3V CERM-X5R 402
C8170 0.47UF 10% 6.3V CERM-X5R 402
C8171 0.47UF 10% 6.3V CERM-X5R 402

OMIT
U8000
NB8P-GS-W-A2
BGA
(8 OF 8)

AE17 AE27 AE6 AF11 AF26 AF29 AF4 AF7 AG10 AG11 AB27 AB6 AC10 AC23 AC29 AC4 AD16 AD17 AD2 AD31 AA12 AA2 AA21 AA31 AG13 AG14 AG15 AG19 AG2 AG22 AG31 AG8 AH24 AJ10 AJ13 AJ16 AJ17 AJ20 AJ23 AJ26 AJ29 AJ4 AJ7 AK2 AK28 AK31 AL10 AL11 AL14 AL19 AL22 AL25 AL3 AL6 AL9 AM10 AM13 AM16 AM17 AM20 AM23 AM26 AM29 B12 B15 B18 B21 B24 B27 B3 B30 B6 B9 C2 C31 D10 D13 → GND

D16 D17 D20 D23 D26 D29 D4 D7 F11 F14 F19 F2 F22 F25 F31 F8 G26 G29 G4 G7 H27 H6 J16 J17 J2 J31 K10 K23 K29 K4 L27 L6 M12 M2 M31 N15 N18 N29 N4 P15 P18 P27 P6 R13 R14 R15 R18 R19 R2 R20 R31 T16 T17 T24 T29 T4 U16 U17 U24 U29 U8 V13 V14 V15 V18 V19 V2 V20 V31 W15 W18 W27 W6 Y15 Y18 Y29 Y4 → GND

NV G84M Core/FB Power

SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

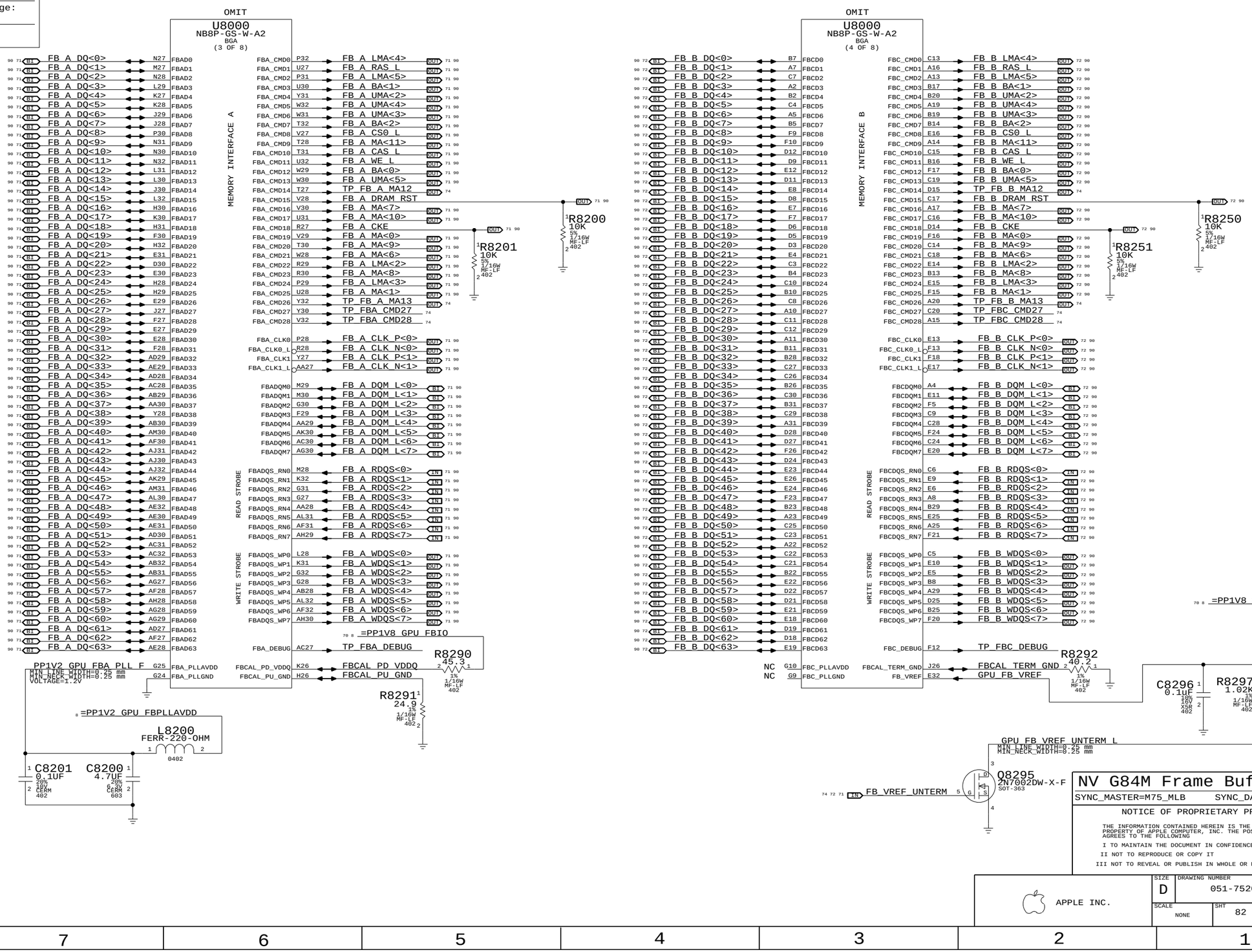
SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 81 OF 109	

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G84M Frame Buffer I/F

SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE	SHT 82 OF 109	
NONE		

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

=PP1V8_GPU_FB_VDD

=PP1V8_GPU_FB_VDDQ

CRITICAL
OMIT

U8400
FBGA
(2 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

U8450
FBGA
(1 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

Connect to designated pin, then GND

C8400 C8401 C8402 C8403 C8404 C8410 C8415
C8420 C8421 C8422 C8423 C8424 C8425 C8426
C8450 C8451 C8452 C8453 C8454 C8460 C8465
C8470 C8471 C8472 C8473 C8474 C8475 C8476

FB_A0_VREF
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

FB_A1_VREF
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

R8430 2.37K
R8431 5.49K
R8432 2.21K
C8431 C8433
R8480 2.37K
R8481 5.49K
R8482 2.21K
C8481 C8483

FB_A0_VREF_UNTERM_L
FB_A1_VREF_UNTERM_L
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

FB_A_CLK0_TERM
FB_A_CLK1_TERM

R8440 R8442 R8444 R8446 C8446
R8490 R8492 R8494 R8496 C8496

Q8400
2N7002DW-X-F
SOT-363

FB_VREF_UNTERM

R8443 R8445 R8447
R8493 R8495 R8497

CRITICAL
OMIT

FB_A_MA<0>
FB_A_MA<1>
FB_A_MA<2>
FB_A_MA<3>
FB_A_MA<4>
FB_A_MA<5>
FB_A_MA<6>
FB_A_MA<7>
FB_A_MA<8>
FB_A_MA<9>
FB_A_MA<10>
FB_A_MA<11>
FB_A_CKE
FB_A_CLK_P<0>
FB_A_CLK_N<0>
FB_A_CS0_L
FB_A_WE_L
FB_A_CAS_L
FB_A_RAS_L

FB_A_DQM_L<0>
FB_A_DQM_L<1>
FB_A_DQM_L<2>
FB_A_DQM_L<3>
FB_A_DQM_L<7>
FB_A_DQM_L<5>
FB_A_DQM_L<6>
FB_A_DQM_L<4>

FB_A_DQ<0> … FB_A_DQ<63>

FB_A_DRAM_RST

FB_A_RDQS<0>
FB_A_RDQS<1>
FB_A_RDQS<2>
FB_A_RDQS<3>
FB_A_RDQS<7>
FB_A_RDQS<5>
FB_A_RDQS<6>
FB_A_RDQS<4>

FB_A_WDQS<0>
FB_A_WDQS<1>
FB_A_WDQS<2>
FB_A_WDQS<3>
FB_A_WDQS<7>
FB_A_WDQS<5>
FB_A_WDQS<6>
FB_A_WDQS<4>

FB_A_BA<0>
FB_A_BA<1>
FB_A_BA<2>

FB_A0_ZQ
FB_A0_MF
FB_A0_SEN
FB_A1_ZQ
FB_A1_MF
FB_A1_SEN

R8448 243
R8449 100
R8498 243
R8499 100

NC J2 RFU1
NC J3 RFU2

GDDR3 Frame Buffer A

SYNC_MASTER=M75_MLB SYNC_DATE=04/02/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B

SCALE	SHT	OF
NONE	84	109

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

=PP1V8_GPU_FB_VDD

=PP1V8_GPU_FB_VDDQ

Connect to designated pin, then GND

CRITICAL
OMIT

U8500
FBGA
(2 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

U8550
FBGA
(1 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

C8500 C8501 C8502 C8503 C8504 C8510 C8515
C8520 C8521 C8522 C8523 C8524 C8525 C8526
C8530 C8531 C8533
C8540 C8542 C8544 C8546 C8543 C8545 C8547 C8548 C8549
C8550 C8551 C8552 C8553 C8554 C8560 C8565
C8570 C8571 C8572 C8573 C8574 C8575 C8576
C8580 C8581 C8583
C8590 C8592 C8594 C8596 C8593 C8595 C8597 C8598 C8599

FB_B0_VREF
FB_B1_VREF
FB_B0_VREF_UNTERM_L
FB_B1_VREF_UNTERM_L
FB_B_CLK0_TERM
FB_B_CLK1_TERM
FB_VREF_UNTERM
FB_B0_ZQ
FB_B0_MF
FB_B0_SEN
FB_B1_ZQ
FB_B1_MF
FB_B1_SEN

Q8500
2N7002DW-X-F
SOT-363

FB_B_MA<0>
FB_B_MA<1>
FB_B_LMA<2>
FB_B_LMA<3>
FB_B_LMA<4>
FB_B_LMA<5>
FB_B_MA<6>
FB_B_MA<7>
FB_B_MA<8>
FB_B_MA<9>
FB_B_MA<10>
FB_B_MA<11>
FB_B_CKE
FB_B_CLK_P<0>
FB_B_CLK_N<0>
FB_B_CS0_L
FB_B_WE_L
FB_B_CAS_L
FB_B_RAS_L
FB_B_DRAM_RST
FB_B_RDQS<2>
FB_B_RDQS<1>
FB_B_RDQS<3>
FB_B_RDQS<0>
FB_B_WDQS<2>
FB_B_WDQS<1>
FB_B_WDQS<3>
FB_B_WDQS<0>
FB_B_BA<0>
FB_B_BA<1>
FB_B_BA<2>
FB_B_DQM_L<2>
FB_B_DQM_L<1>
FB_B_DQM_L<3>
FB_B_DQM_L<0>
FB_B_DQ<18>
FB_B_DQ<17>
FB_B_DQ<19>
FB_B_DQ<16>
FB_B_DQ<21>
FB_B_DQ<23>
FB_B_DQ<20>
FB_B_DQ<22>
FB_B_DQ<8>
FB_B_DQ<12>
FB_B_DQ<9>
FB_B_DQ<10>
FB_B_DQ<13>
FB_B_DQ<14>
FB_B_DQ<15>
FB_B_DQ<11>
FB_B_DQ<24>
FB_B_DQ<28>
FB_B_DQ<29>
FB_B_DQ<31>
FB_B_DQ<30>
FB_B_DQ<25>
FB_B_DQ<26>
FB_B_DQ<27>
FB_B_DQ<2>
FB_B_DQ<1>
FB_B_DQ<6>
FB_B_DQ<0>
FB_B_DQ<7>
FB_B_DQ<4>
FB_B_DQ<5>
FB_B_DQ<3>
FB_B_UMA<2>
FB_B_UMA<3>
FB_B_UMA<4>
FB_B_UMA<5>
FB_B_MA<6>
FB_B_MA<7>
FB_B_MA<8>
FB_B_MA<9>
FB_B_MA<10>
FB_B_MA<11>
FB_B_CKE
FB_B_CLK_P<1>
FB_B_CLK_N<1>
FB_B_CS0_L
FB_B_WE_L
FB_B_CAS_L
FB_B_RAS_L
FB_B_DRAM_RST
FB_B_RDQS<6>
FB_B_RDQS<5>
FB_B_RDQS<4>
FB_B_RDQS<7>
FB_B_WDQS<6>
FB_B_WDQS<5>
FB_B_WDQS<4>
FB_B_WDQS<7>
FB_B_BA<0>
FB_B_BA<1>
FB_B_BA<2>
FB_B_DQM_L<6>
FB_B_DQM_L<5>
FB_B_DQM_L<4>
FB_B_DQM_L<7>
FB_B_DQ<49>
FB_B_DQ<50>
FB_B_DQ<48>
FB_B_DQ<51>
FB_B_DQ<52>
FB_B_DQ<55>
FB_B_DQ<54>
FB_B_DQ<53>
FB_B_DQ<40>
FB_B_DQ<42>
FB_B_DQ<41>
FB_B_DQ<45>
FB_B_DQ<43>
FB_B_DQ<46>
FB_B_DQ<47>
FB_B_DQ<44>
FB_B_DQ<36>
FB_B_DQ<39>
FB_B_DQ<37>
FB_B_DQ<38>
FB_B_DQ<34>
FB_B_DQ<32>
FB_B_DQ<35>
FB_B_DQ<33>
FB_B_DQ<63>
FB_B_DQ<58>
FB_B_DQ<61>
FB_B_DQ<59>
FB_B_DQ<62>
FB_B_DQ<56>
FB_B_DQ<60>
FB_B_DQ<57>

GDDR3 Frame Buffer B

SYNC_MASTER=M75_MLB SYNC_DATE=04/02/2007

APPLE INC.

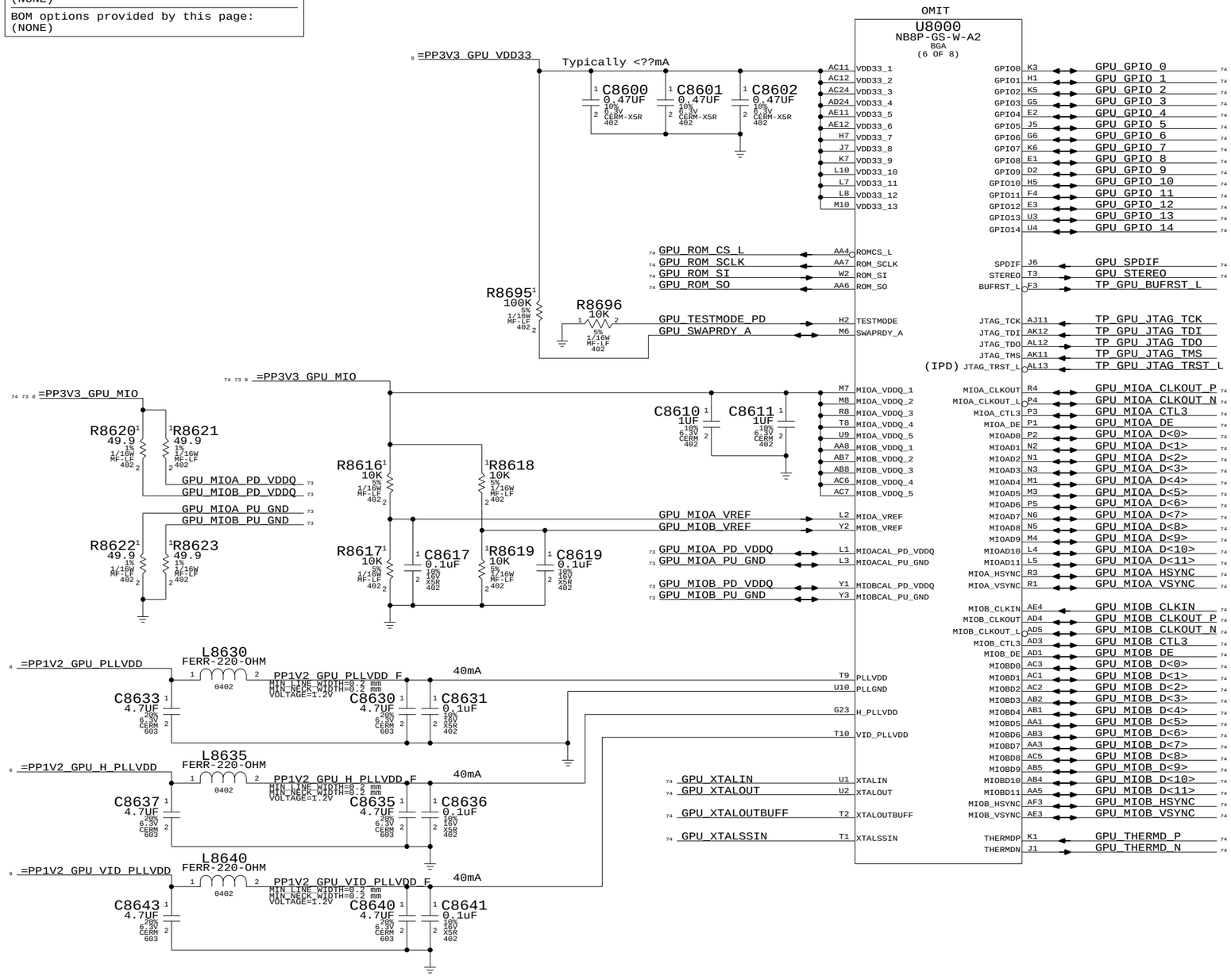
SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 85 OF 109	

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP3V3_GPI_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G84M GPIO/MIO/Misc

SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 86 OF 109	

GPIOs

	Native Func			
GPU_GPIO_0	HPD0	GPU_HPD	IN	78
GPU_GPIO_1	HPD1	NC_GPU_GPIO_1		
GPU_GPIO_2	LCD0_BL_PWM	GPU_BL_PWM	OUT	79
GPU_GPIO_3	LCD0_VDD	GPU_PANEL_EN	OUT	79
GPU_GPIO_4	LCD0_BL_EN	GPU_BKLT_EN	OUT	79
GPU_GPIO_5	VID0	GPU_VCORE_VID0	OUT	76
GPU_GPIO_6	VID1	GPU_VCORE_VID1	OUT	76
GPU_GPIO_7	MEM_VID	GPU_VGA_EN_L		74
GPU_GPIO_8	THERM	NC_GPU_GPIO_8		
GPU_GPIO_9	FAN_PWM	TP_GPU_GSTATE<0>		
GPU_GPIO_10	MEM_VREF	FB_VREF_UNTERM	OUT	70 71 72
GPU_GPIO_11	SLI_SYNC	GPU_VCORE_VID2	OUT	76
GPU_GPIO_12	AC_DET	TP_GPU_GSTATE<1>		
GPU_GPIO_13	PWR_CTL0	GPU_VCORE_PWRCTL0	OUT	76
GPU_GPIO_14	PWR_CTL1	GPU_VCORE_PWRCTL1	OUT	76

Config Straps

=PP3V3_GPU_MIO

	VRAM_SAMSUNG		VRAM_128	NO STUFF		NO STUFF	NO STUFF	NO STUFF	NO STUFF
	R8720	R8722	R8724	R8726	R8728	R8729	R8730	R8731	R8732
	10K	10K	10K	10K	1K	1K	1K	1K	1K
Supported straps:									
RAMCFG0	GPU_MIOB_D<0>								
RAMCFG1		GPU_MIOB_D<1>							
RAMCFG2			GPU_MIOB_D<8>						
RAMCFG3				GPU_MIOB_D<9>					
3GIO_PADCFG0					GPU_MIOA_D<6>				
3GIO_PADCFG1						GPU_MIOA_D<8>			
3GIO_PADCFG2							GPU_MIOA_D<9>		
3GIO_PADCFG3								GPU_MIOB_HSYNC	
PEX_PLL_EN_TERM									GPU_MIOA_D<0>
SUBVENDOR (BIOS ROM PRESENT)									GPU_MIOA_D<1>

	VRAM_HYNIX	NO STUFF	VRAM_256		
	R8721	R8723	R8725	R8727	R8733
	10K	10K	10K	10K	1K
PCI_DEVID3					
PCI_DEVID0					

=PP3V3_GPU_MIO

	NO STUFF			
	R8734	R8735	R8736	R8737
	1K	1K	1K	1K
PCI_DEVID3	GPU_MIOB_D<11>	GPU_MIOB_D<3>		
PCI_DEVID0			GPU_MIOB_D<5>	GPU_MIOB_D<4>

Straps not supported:

USER<3..0>	MIOA_D<5..2>
ROMTYPE<1..0>	MIOB_VSYNC, MIOB_D<10>
SLOT_CLOCK_CFG	MIOA_HSYNC
PCI_IOBAR	MIOB_D<7>
BAR2_SIZE	MIOB_DE
PCI_DEVID<4>	MIOB_CTL3, MIOB_D<3,5>

Analog Video Mux

=PP3V3_GPU_VIDEOMUX

C8700 0.1UF 20% 10V CERM 402

GPU_VGA_R
GPU_VGA_G
GPU_VGA_B

R8740 150 1% 1/10W MF-LF 402
R8741 150 1% 1/10W MF-LF 402
R8742 150 1% 1/10W MF-LF 402
Place Rs near GPU

GPU_TV_C
GPU_TV_Y
GPU_TV_COMP

R8743 150 1% 1/10W MF-LF 402
R8744 150 1% 1/10W MF-LF 402
R8745 150 1% 1/10W MF-LF 402
Place Rs near GPU

CRITICAL OMIT

U8700 TS3V330 QFN 16

S1A	2	DA	4
S2A	3	DB	7
S1B	5	DC	9
S2B	6	DD	12
S1C	11	IN	1
S2C	10	EN_L	15
S1D	14	VCC	16
S2D	13	THRML PAD	17
		GND	8

GPU_TV_C_VGA_R OUT 78 90
GPU_TV_Y_VGA_G OUT 78 90
GPU_TV_COMP_VGA_B OUT 78 90
NC
GPU_VGA_EN_L 74

R8700 10K 5% 1/16W MF-LF 402

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1718	1	IC,TS3V340,QUAD VIDEO SW,QFN16	U8700	CRITICAL	

PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1579	353S1718		ALL (U8700)	TS3V330 alt to TS3V340

Renamed signals

GPU_CLK27M_GATED	=	GPU_XTALIN
GPU_CLK27M_SS_GATED	=	GPU_XTALSSIN
GPU_TDIODE_P	=	GPU_THERMD_P
GPU_TDIODE_N	=	GPU_THERMD_N
GPU_DVI_DDC_CLK	=	GPU_I2CB_SCL
GPU_DVI_DDC_DATA	=	GPU_I2CB_SDA
GPU_PANEL_DDC_CLK	=	GPU_I2CC_SCL
GPU_PANEL_DDC_DATA	=	GPU_I2CC_SDA

Unused I2C Buses

NC_GPU_I2CA_SCL	=	GPU_I2CA_SCL
NC_GPU_I2CA_SDA	=	GPU_I2CA_SDA

I2CS ties into SMBus connection page
(I2CS requires pullups even if not used)

HDCP Support

=PP3V3_GPU_HDCP

HDCP C8770 0.1UF 20% 10V CERM 402

HDCP R8770 10K 5% 1/16W MF-LF 402

HDCP CRITICAL

U8770 AT88SC080C SO1

GPU_I2CH_SCL
GPU_I2CH_SDA

HDCP R8771 10K 5% 1/16W MF-LF 402

NC

TMDS Backdrive Protection

CRITICAL Q8790 SI2305DS SOT-23

=PP3V3_GPU_TMDS
=PP3V3_GPU_TMDS_FET

R8790 10K 5% 1/16W MF-LF 402

GPU_TMDS_PWREN_L

Q8925 2N7002DW-X-F SOT-363

=GPUVCORE_EN

R8791 100K 5% 1/10W MF-LF 402

Unused signals

NC_GPU_XTALOUT	=	GPU_XTALOUT
NC_GPU_SPDIF	=	GPU_SPDIF
NC_GPU_STEREO	=	GPU_STEREO
NC_FB_A_MA12	=	TP_FB_A_MA12
NC_FB_B_MA12	=	TP_FB_B_MA12
NC_FB_A_MA13	=	TP_FB_A_MA13
NC_FB_B_MA13	=	TP_FB_B_MA13
NC_FBA_CMD27	=	TP_FBA_CMD27
NC_FBC_CMD27	=	TP_FBC_CMD27
NC_FBA_CMD28	=	TP_FBA_CMD28
NC_FBC_CMD28	=	TP_FBC_CMD28
NC_GPU_ROM_CS_L	=	GPU_ROM_CS_L
NC_GPU_ROM_SCLK	=	GPU_ROM_SCLK
NC_GPU_ROM_SI	=	GPU_ROM_SI
NC_GPU_ROM_SO	=	GPU_ROM_SO
NC_GPU_CSYNC	=	GPU_CSYNC
NC_GPU_R2	=	GPU_R2
NC_GPU_G2	=	GPU_G2
NC_GPU_B2	=	GPU_B2
NC_GPU_H2SYNC	=	GPU_H2SYNC
NC_GPU_V2SYNC	=	GPU_V2SYNC
NC_LVDS_U_DATAP<3>	=	LVDS_U_DATA_P<3>
NC_LVDS_U_DATAN<3>	=	LVDS_U_DATA_N<3>
NC_LVDS_L_DATAP<3>	=	LVDS_L_DATA_P<3>
NC_LVDS_L_DATAN<3>	=	LVDS_L_DATA_N<3>
TP_GPU_MIOA_CLKOUT_P	=	GPU_MIOA_CLKOUT_P
TP_GPU_MIOA_CLKOUT_N	=	GPU_MIOA_CLKOUT_N
TP_GPU_MIOA_CTL3	=	GPU_MIOA_CTL3
TP_GPU_MIOA_DE	=	GPU_MIOA_DE
TP_GPU_MIOA_D<5..2>	=	GPU_MIOA_D<5..2>
TP_GPU_MIOA_D<7>	=	GPU_MIOA_D<7>
TP_GPU_MIOA_D<11..10>	=	GPU_MIOA_D<11..10>
TP_GPU_MIOA_HSYNC	=	GPU_MIOA_HSYNC
TP_GPU_MIOA_VSYNC	=	GPU_MIOA_VSYNC
TP_GPU_MIOB_CLKIN	=	GPU_MIOB_CLKIN
TP_GPU_MIOB_CLKOUT_P	=	GPU_MIOB_CLKOUT_P
TP_GPU_MIOB_CLKOUT_N	=	GPU_MIOB_CLKOUT_N
TP_GPU_MIOB_CTL3	=	GPU_MIOB_CTL3
TP_GPU_MIOB_DE	=	GPU_MIOB_DE
TP_GPU_MIOB_D<2>	=	GPU_MIOB_D<2>
TP_GPU_MIOB_D<7..6>	=	GPU_MIOB_D<7..6>
TP_GPU_MIOB_D<10>	=	GPU_MIOB_D<10>
TP_GPU_MIOB_VSYNC	=	GPU_MIOB_VSYNC
NC_GPU_IFPD_CLK_P	=	GPU_IFPD_CLK_P
NC_GPU_IFPD_CLK_N	=	GPU_IFPD_CLK_N

Unused Clocks

GPU_XTALSSIN
GPU_XTALOUTBUFF

R8780 10K 5% 1/16W MF-LF 402
GPU_SS_INT
R8781 10K 5% 1/16W MF-LF 402

GPU Straps

SYNC_MASTER=M75_MLB SYNC_DATE=04/02/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 87 OF 109	

Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD
- =PP3V3_GPU_DAC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents: 240mA

=PP1V8_GPU_IFPX

L8800 FERR-220-OHM 0402

20mA peak per diff pair
160mA peak for all pairs

C8800 4.7UF 20% 6.3V CERM 603
C8801 0.1UF 20% 10V CERM 402
C8803 0.1UF 20% 10V CERM 402

Place at AF9 Place at AF8

PP1V8_GPU_IFPAB_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

L8805 FERR-220-OHM 0402

40mA peak

C8805 4.7UF 20% 6.3V CERM 603
C8806 0.1UF 20% 10V CERM 402

PP1V8_GPU_IFPAB_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

75 GPU_IFPAB_VPROBE
75 GPU_IFPAB_RSET

=PP3V3_GPU_IFPCD_IOVDD

L8810 FERR-220-OHM 0402

20mA peak per diff pair
200mA peak for all pairs

C8810 4.7UF 20% 6.3V CERM 603
C8811 0.1UF 20% 10V CERM 402
C8813 0.1UF 20% 10V CERM 402

Place at AD6 Place at AE7

PP3V3_GPU_IFPCD_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

L8815 FERR-220-OHM 0402

40mA peak

C8815 4.7UF 20% 6.3V CERM 603
C8816 0.1UF 20% 10V CERM 402

PP1V8_GPU_IFPCD_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

75 GPU_IFPCD_VPROBE
75 GPU_IFPCD_RSET

Sum of peak currents: 390mA

8 =PP3V3_GPU_DAC

L8820 FERR-220-OHM 0402

120mA peak

C8820 4.7UF 20% 6.3V CERM 603
C8821 0.1UF 20% 10V CERM 402

PP3V3_GPU_DACA_VDD_F
MIN_LINE_WIDTH=0.35 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

75 GPU_DACA_VREF
75 GPU_DACA_RSET

L8830 FERR-220-OHM 0402

150mA peak

C8830 4.7UF 20% 6.3V CERM 603
C8831 0.1UF 20% 10V CERM 402

PP3V3_GPU_DACB_VDD_F
MIN_LINE_WIDTH=0.35 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

75 GPU_DACB_VREF
75 GPU_DACB_RSET

NO STUFF
L8840 FERR-220-OHM 0402

120mA peak

C8845 4.7UF 20% 6.3V CERM 603
NO STUFF C8840 4.7UF 20% 6.3V CERM 603
C8841 0.1UF 20% 10V CERM 402

PP3V3_GPU_DACC_VDD_F
MIN_LINE_WIDTH=0.35 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

75 GPU_DACC_VREF
75 GPU_DACC_RSET

74 GPU_I2CC_SCL
74 GPU_I2CC_SDA
74 GPU_I2CH_SCL
74 GPU_I2CH_SDA
=GPU_I2CS_SCL
=GPU_I2CS_SDA

I2CS must be pulled up if not used
I2CS addr fixed at 0x9E,0x9F

OMIT
U8000
NB8P-GS-W-A2
BGA
(5 OF 8)

AF9	IFPA_IOVDD	IFPA_TXC	AK9
AF8	IFPB_IOVDD	IFPA_TXC_L	AJ9
AC9	IFPAB_PLLVDD	IFPA_TXD0	AH6
AD9	IFPAB_PLLGND	IFPA_TXD0_L	AJ6
AM4	IFPAB_VPROBE	IFPA_TXD1	AH8
AL5	IFPAB_RSET	IFPA_TXD1_L	AH7
		IFPA_TXD2	AJ8
		IFPA_TXD2_L	AK8
		IFPA_TXD3	AJ5
		IFPA_TXD3_L	AH5
		IFPB_TXC	AK4
		IFPB_TXC_L	AL4
		IFPB_TXD4	AM6
		IFPB_TXD4_L	AM5
		IFPB_TXD5	AM7
		IFPB_TXD5_L	AL7
		IFPB_TXD6	AK6
		IFPB_TXD6_L	AK5
		IFPB_TXD7	AK7
		IFPB_TXD7_L	AL8
AD6	IFPC_IOVDD	IFPC_TXC	AM2
AE7	IFPD_IOVDD	IFPC_TXC_L	AM3
AA10	IFPCD_PLLVDD	IFPC_TXD0	AE2
AB10	IFPCD_PLLGND	IFPC_TXD0_L	AE1
AK3	IFPCD_VPROBE	IFPC_TXD1	AF1
AH3	IFPCD_RSET	IFPC_TXD1_L	AF2
		IFPC_TXD2	AG1
		IFPC_TXD2_L	AH1
		IFPD_TXC	AG3
		IFPD_TXC_L	AH2
		IFPD_TXD4	AK1
		IFPD_TXD4_L	AJ1
		IFPD_TXD5	AL2
		IFPD_TXD5_L	AL1
		IFPD_TXD6	AJ2
		IFPD_TXD6_L	AJ3
AD10	DACA_VDD	DACA_RED	AH11
AG9	DACA_IDUMP	DACA_GREEN	AJ12
AH10	DACA_VREF	DACA_BLUE	AH12
AH9	DACA_RSET	DACA_HSYNC	AF10
		DACA_VSYNC	AK10
V8	DACB_VDD	DACB_RED	R6
V7	DACB_IDUMP	DACB_GREEN	T5
R5	DACB_VREF	DACB_BLUE	T6
R7	DACB_RSET	DACB_CSYNC	U5
AD7	DACC_VDD	DACC_RED	AF6
AG4	DACC_IDUMP	DACC_GREEN	AG6
AH4	DACC_VREF	DACC_BLUE	AE5
AF5	DACC_RSET	DACC_HSYNC	AG7
		DACC_VSYNC	AG5
G2	I2CC_SCL	I2CA_SCL	K2
G1	I2CC_SDA	I2CA_SDA	J3
G3	I2CH_SCL	I2CB_SCL	H4
H3	I2CH_SDA	I2CB_SDA	J4
C1	I2CS_SCL		
B1	I2CS_SDA		

LVDS_L_CLK_P	7 79 90
LVDS_L_CLK_N	79 90
LVDS_L_DATA_P<0>	7 79 90
LVDS_L_DATA_N<0>	79 90
LVDS_L_DATA_P<1>	79 90
LVDS_L_DATA_N<1>	79 90
LVDS_L_DATA_P<2>	79 90
LVDS_L_DATA_N<2>	79 90
LVDS_L_DATA_P<3>	74 90
LVDS_L_DATA_N<3>	74 90
LVDS_U_CLK_P	79 90
LVDS_U_CLK_N	79 90
LVDS_U_DATA_P<0>	79 90
LVDS_U_DATA_N<0>	79 90
LVDS_U_DATA_P<1>	79 90
LVDS_U_DATA_N<1>	79 90
LVDS_U_DATA_P<2>	79 90
LVDS_U_DATA_N<2>	79 90
LVDS_U_DATA_P<3>	74 90
LVDS_U_DATA_N<3>	74 90
TMDS_CLK_P	78 90
TMDS_CLK_N	78 90
TMDS_DATA_P<0>	78 90
TMDS_DATA_N<0>	78 90
TMDS_DATA_P<1>	78 90
TMDS_DATA_N<1>	78 90
TMDS_DATA_P<2>	78 90
TMDS_DATA_N<2>	78 90
GPU_IFPD_CLK_P	74
GPU_IFPD_CLK_N	74
TMDS_DATA_P<3>	78 90
TMDS_DATA_N<3>	78 90
TMDS_DATA_P<4>	78 90
TMDS_DATA_N<4>	78 90
TMDS_DATA_P<5>	78 90
TMDS_DATA_N<5>	78 90
GPU_VGA_R	74 90
GPU_VGA_G	74 90
GPU_VGA_B	74 90
GPU_VGA_HSYNC	78 90
GPU_VGA_VSYNC	78 90
GPU_TV_C	74 90
GPU_TV_Y	74 90
GPU_TV_COMP	74 90
GPU_CSYNC	74
GPU_R2	74
GPU_G2	74
GPU_B2	74
GPU_H2SYNC	74
GPU_V2SYNC	74
GPU_I2CA_SCL	74
GPU_I2CA_SDA	74
GPU_I2CB_SCL	74
GPU_I2CB_SDA	74

Composite/S-Video	VGA	Component
C	R	Pr
Y	G	Y
Comp	B	Pb

GPU_IFPAB_RSET 75
GPU_IFPCD_RSET 75
GPU_DACA_RSET 75
GPU_DACB_RSET 75
GPU_DACC_RSET 75

NO STUFF R8850 1K 1% 1/16W ME-LF 402
NO STUFF R8851 1K 1% 1/16W ME-LF 402
R8852 124 1% 1/16W ME-LF 402
R8853 124 1% 1/16W ME-LF 402
R8854 124 1% 1/16W ME-LF 402

GPU_DACA_VREF 75
GPU_DACB_VREF 75
GPU_DACC_VREF 75

C8852 0.1UF 20% 10V CERM 402
C8853 0.1UF 20% 10V CERM 402
C8854 0.1UF 20% 10V CERM 402

GPU_IFPAB_VPROBE 75
GPU_IFPCD_VPROBE 75

NO STUFF C8855 0.01UF 20% 16V CERM 402
NO STUFF C8856 0.01UF 20% 16V CERM 402

NV G84M Video Interfaces

SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

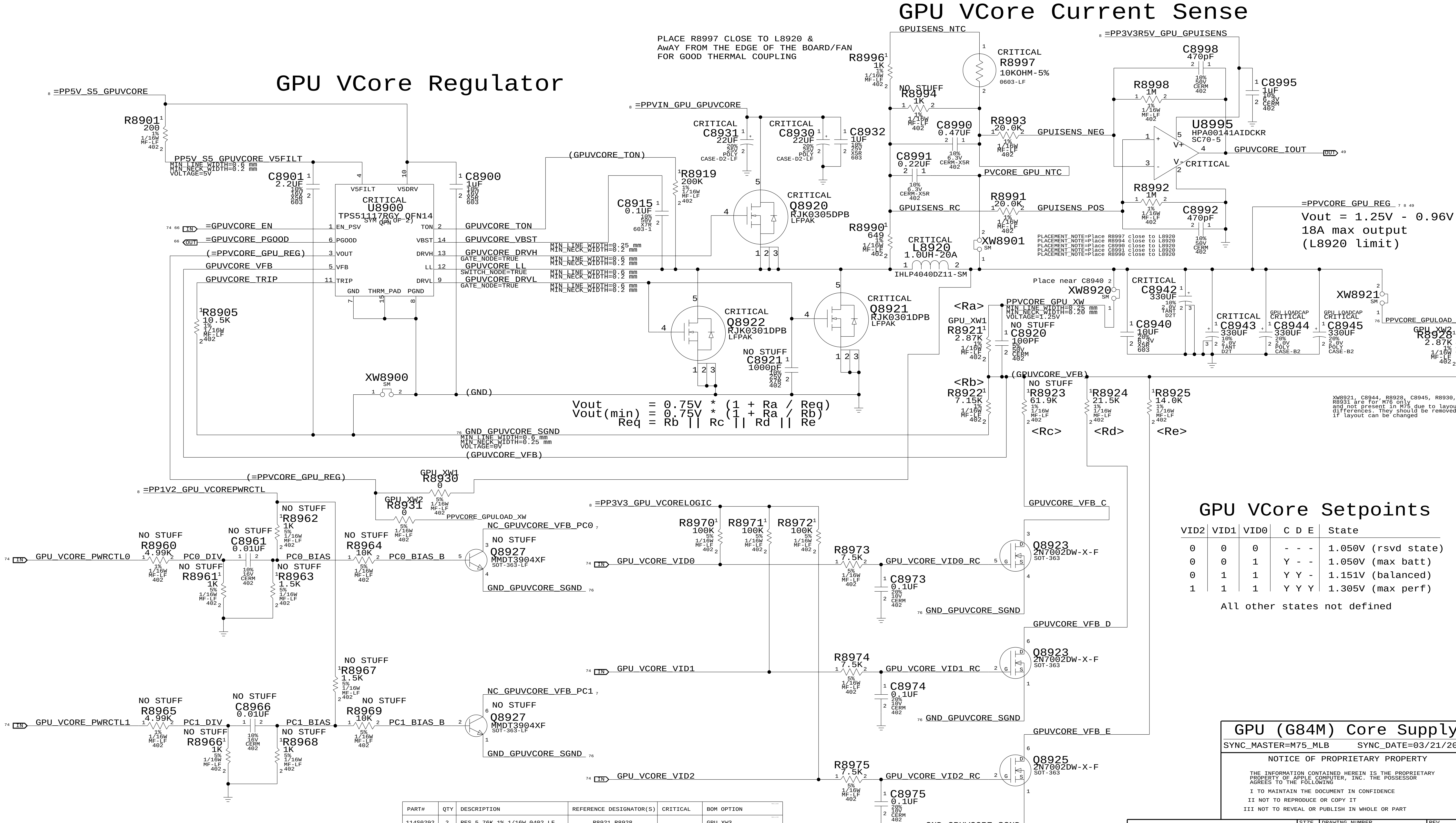
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B

SCALE	SHT	OF
NONE	88	109

GPU VCore Regulator

GPU VCore Current Sense



GPU VCore Setpoints

VID2	VID1	VID0	C D E	State
0	0	0	- - -	1.050V (rsvd state)
0	0	1	Y - -	1.050V (max batt)
0	1	1	Y Y -	1.151V (balanced)
1	1	1	Y Y Y	1.305V (max perf)

All other states not defined

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0292	2	RES,5.76K,1%,1/16W,0402,LF	R8921,R8928		GPU_XW3

GPU (G84M) Core Supply

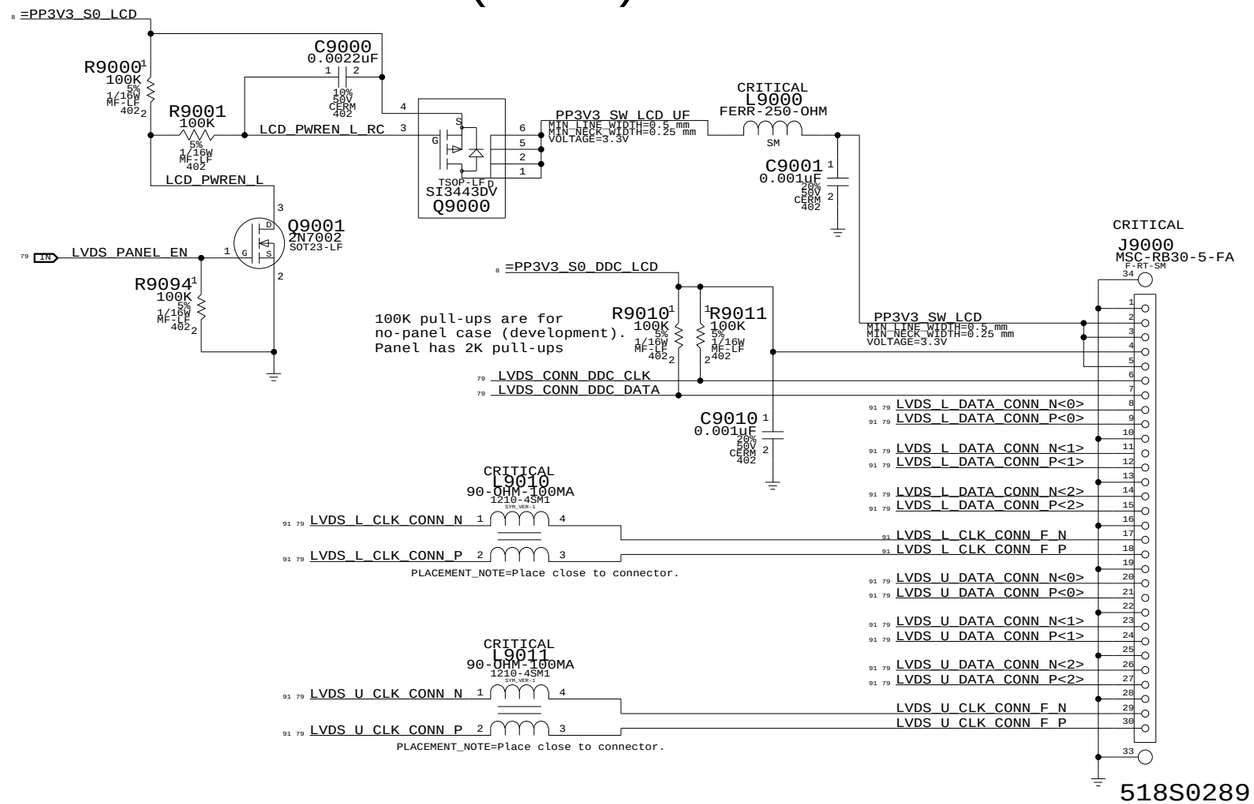
SYNC_MASTER=M75_MLB SYNC_DATE=03/21/2007

SIZE	DRAWING NUMBER	REV.
D	051-7520	B

APPLE INC.

SCALE NONE | SHT 89 OF 109

LCD (LVDS) INTERFACE



LVDS Display Connector

SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B

SCALE	SHT	OF
NONE	90	109

TMDS Filtering

(Place close to GPU) (Place close to connector)

TMDS_DATA_N<0> — NO STUFF R9462 49.9 1% 1/16W MF-LF 402 — SIGNAL_MODEL=EMPTY TMDS_DATA_R0 — NO STUFF R9463 49.9 1% 1/16W MF-LF 402 — TMDS_DATA_P<0>
=PP3V3_GPU_TMDSBIAS — NO STUFF C9462 0.01UF 10% 16V CERM 402
CRITICAL L9460 90-OHM-100MA 1210-4SM1 — TMDS_DATA_F_N<0> / TMDS_DATA_F_P<0>
PLACEMENT_NOTE=Place close to connector.

TMDS_DATA_N<1> — NO STUFF R9466 49.9 1% 1/16W MF-LF 402 — SIGNAL_MODEL=EMPTY TMDS_DATA_R1 — NO STUFF R9467 49.9 1% 1/16W MF-LF 402 — TMDS_DATA_P<1>
=PP3V3_GPU_TMDSBIAS — NO STUFF C9466 0.01UF 10% 16V CERM 402
CRITICAL L9464 90-OHM-100MA 1210-4SM1 — TMDS_DATA_F_N<1> / TMDS_DATA_F_P<1>
PLACEMENT_NOTE=Place close to connector.

TMDS_DATA_N<2> — NO STUFF R9470 49.9 1% 1/16W MF-LF 402 — SIGNAL_MODEL=EMPTY TMDS_DATA_R2 — NO STUFF R9471 49.9 1% 1/16W MF-LF 402 — TMDS_DATA_P<2>
=PP3V3_GPU_TMDSBIAS — NO STUFF C9470 0.01UF 10% 16V CERM 402
CRITICAL L9468 90-OHM-100MA 1210-4SM1 — TMDS_DATA_F_N<2> / TMDS_DATA_F_P<2>
PLACEMENT_NOTE=Place close to connector.

TMDS_CLK_N — R9472 0 5% 1/16W MF-LF 402 — TMDS_CLK_R_N — CRITICAL L9472 370-OHM SM — TMDS_CLK_F_N / TMDS_CLK_F_P
PLACEMENT_NOTE=Place close to connector.
=PP3V3_GPU_TMDSBIAS — NO STUFF C9474 0.01UF 10% 16V CERM 402 — SIGNAL_MODEL=EMPTY TMDS_CLK_CMF — NO STUFF R9475 49.9 1% 1/16W MF-LF 402
TMDS_CLK_P — R9473 0 5% 1/16W MF-LF 402 — TMDS_CLK_R_P

TMDS_DATA_N<3> — NO STUFF R9478 49.9 1% 1/16W MF-LF 402 — SIGNAL_MODEL=EMPTY TMDS_DATA_R3 — NO STUFF R9479 49.9 1% 1/16W MF-LF 402 — TMDS_DATA_P<3>
=PP3V3_GPU_TMDSBIAS — NO STUFF C9478 0.01UF 10% 16V CERM 402
CRITICAL L9476 90-OHM-100MA 1210-4SM1 — TMDS_DATA_F_N<3> / TMDS_DATA_F_P<3>
PLACEMENT_NOTE=Place close to connector.

TMDS_DATA_N<4> — NO STUFF R9482 49.9 1% 1/16W MF-LF 402 — SIGNAL_MODEL=EMPTY TMDS_DATA_R4 — NO STUFF R9483 49.9 1% 1/16W MF-LF 402 — TMDS_DATA_P<4>
=PP3V3_GPU_TMDSBIAS — NO STUFF C9482 0.01UF 10% 16V CERM 402
CRITICAL L9480 90-OHM-100MA 1210-4SM1 — TMDS_DATA_F_N<4> / TMDS_DATA_F_P<4>
PLACEMENT_NOTE=Place close to connector.

TMDS_DATA_N<5> — NO STUFF R9486 49.9 1% 1/16W MF-LF 402 — SIGNAL_MODEL=EMPTY TMDS_DATA_R5 — NO STUFF R9487 49.9 1% 1/16W MF-LF 402 — TMDS_DATA_P<5>
=PP3V3_GPU_TMDSBIAS — NO STUFF C9486 0.01UF 10% 16V CERM 402
CRITICAL L9484 90-OHM-100MA 1210-4SM1 — TMDS_DATA_F_N<5> / TMDS_DATA_F_P<5>
PLACEMENT_NOTE=Place close to connector.

VGA SYNC Buffers

=PP3V3_GPU_VGASYNC — U9450 MC74VHC1G08 SC70 — PLACEMENT_NOTE=Place close to connector.
GPU_VGA_VSYNC — C9450 0.1UF 10% 16V CERM 402 — R9450 33 5% 1/16W MF-LF 402 — VGA_VSYNC_R — VGA_VSYNC

=PP3V3_GPU_VGASYNC — U9451 MC74VHC1G08 SC70 — PLACEMENT_NOTE=Place close to connector.
GPU_VGA_HSYNC — C9451 0.1UF 10% 16V CERM 402 — R9451 33 5% 1/16W MF-LF 402 — VGA_HSYNC_R — VGA_HSYNC

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

GPU_TV_COMP_VGA_B — VGA_TERM_FILTER R9440 150 1% 1/16W MF-LF 402 — VGA_B (DACB TV COMP) — C9440 3.3PF 0.25PF 50V CERM 402
GPU_TV_Y_VGA_G — VGA_TERM_FILTER R9441 150 1% 1/16W MF-LF 402 — VGA_G (DACB TV Y) — C9441 3.3PF 0.25PF 50V CERM 402
GPU_TV_C_VGA_R — VGA_TERM_FILTER R9442 150 1% 1/16W MF-LF 402 — VGA_R (DACB TV C) — C9442 3.3PF 0.25PF 50V CERM 402
CRITICAL FL9440 210MHZ MEA2010P-SM

DVI INTERFACE

DVI DDC Current Limit
(55mA requirement per DVI spec)

=PP5V_S0_DVI_DDC — CRITICAL F9410 0.5AMP-13.2V SM-LF — PP5V_S0_DDC_F — CRITICAL L9410 400-OHM-EMI SM-1 — PP5V_S0_DDC
MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=5V

Isolation required for DVI->ADC Adapter
D9410 SOD-123 B0530WXF — PP5V_S0_DDC_PULLUPS
R9410 4.7K 5% 1/16W MF-LF 402 — R9412 4.7K 5% 1/16W MF-LF 402
R9411 100 5% 1/16W MF-LF 402 — DVI_DDC_CLK
R9413 100 5% 1/16W MF-LF 402 — DVI_DDC_DATA
R9414 100 5% 1/16W MF-LF 402 — DVI_HPD
C9411 100PF 5% 50V CERM 402
C9413 100PF 5% 50V CERM 402
C9414 100PF 5% 50V CERM 402

=GND_CHASSIS_DVI_BOT — CRITICAL J9400 QH11121-RIG02-4F F-RT-TH-DVI

TMDS_DATA_F_N<0>	17	1	TMDS_DATA_F_N<2>
TMDS_DATA_F_P<0>	18	9	TMDS_DATA_F_N<1>
	19	2	TMDS_DATA_F_P<2>
TMDS_DATA_F_N<5>	20	10	TMDS_DATA_F_P<1>
TMDS_DATA_F_P<5>	21	3	
	22	11	TMDS_DATA_F_N<4>
TMDS_CLK_F_P	23	4	TMDS_DATA_F_N<3>
TMDS_CLK_F_N	24	12	TMDS_DATA_F_P<4>
		5	TMDS_DATA_F_P<3>
		13	DVI_DDC_CLK_R
		6	(PP5V_S0_DDC)
		14	DVI_DDC_DATA_R
		7	
		15	VGA_VSYNC
		8	DVI_HPD_R
VGA_B	C3	16	VGA_R
	C5B	C1	
VGA_HSYNC	C4	C5A	VGA_G
		C2	

J9400 pin 34 — 514-0278 — J9400 pin 32

VGA_TERM_CONN R9445 150 1% 1/16W MF-LF 402
VGA_TERM_CONN R9443 150 1% 1/16W MF-LF 402
VGA_TERM_CONN R9444 150 1% 1/16W MF-LF 402
C9410 0.01UF 10% 50V CERM 603

OMIT CX9490 SHORT NONE NONE NONE 402 — OMIT CX9491 SHORT NONE NONE NONE 402 — OMIT CX9492 SHORT NONE NONE NONE 402 — OMIT CX9493 SHORT NONE NONE NONE 402
=GND_CHASSIS_DVI_TOP
OMIT CX9400 SHORT NONE NONE NONE 402 — OMIT CX9401 SHORT NONE NONE NONE 402 — OMIT CX9402 SHORT NONE NONE NONE 402 — OMIT CX9403 SHORT NONE NONE NONE 402
=GND_CHASSIS_DVI_BOT

GPU Isolation / Level-Shift

=PP3V3_GPU_DVI
Q9411 2N7002DW-X-F SOT-363 — DVI_DDC_CLK — R9420 10K 5% 1/16W MF-LF 402 — GPU_DVI_DDC_CLK (OUT)
Q9411 2N7002DW-X-F SOT-363 — DVI_DDC_DATA — R9421 10K 5% 1/16W MF-LF 402 — GPU_DVI_DDC_DATA (OUT)
GPU_HPD_BILAT — =GPU_HPD_ENABLE (IN)
Q9414 2N7002DW-X-F SOT-363 — DVI_HPD — R9422 270K 5% 1/16W MF-LF 402 — GPU_HPD (OUT)
=PP5V_S0_SB_HPD
Q9415 2N7002DW-X-F SOT-363 — R9423 270K 5% 1/16W MF-LF 402 — DVI_HOTPLUG_DET (OUT)
R9415 20K 5% 1/16W MF-LF 402

DVI Display Connector

SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

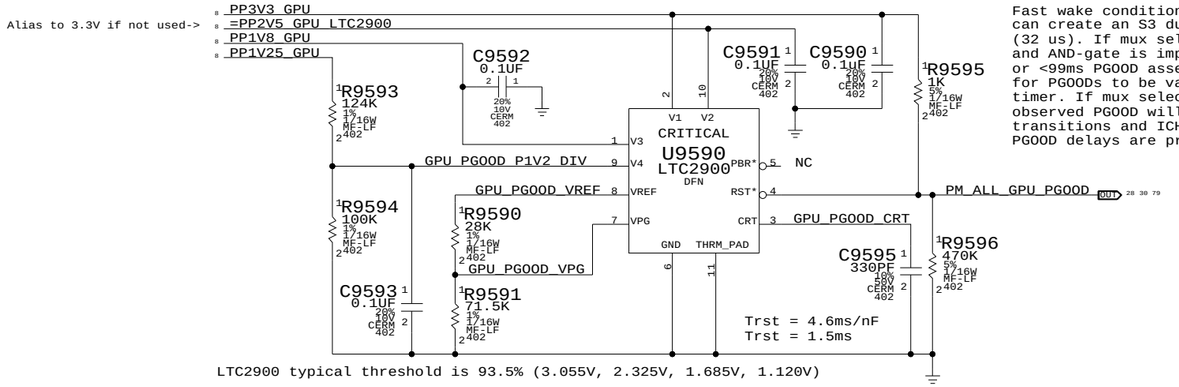
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 94 OF 109	

PGOOD Monitor for GPU Rails

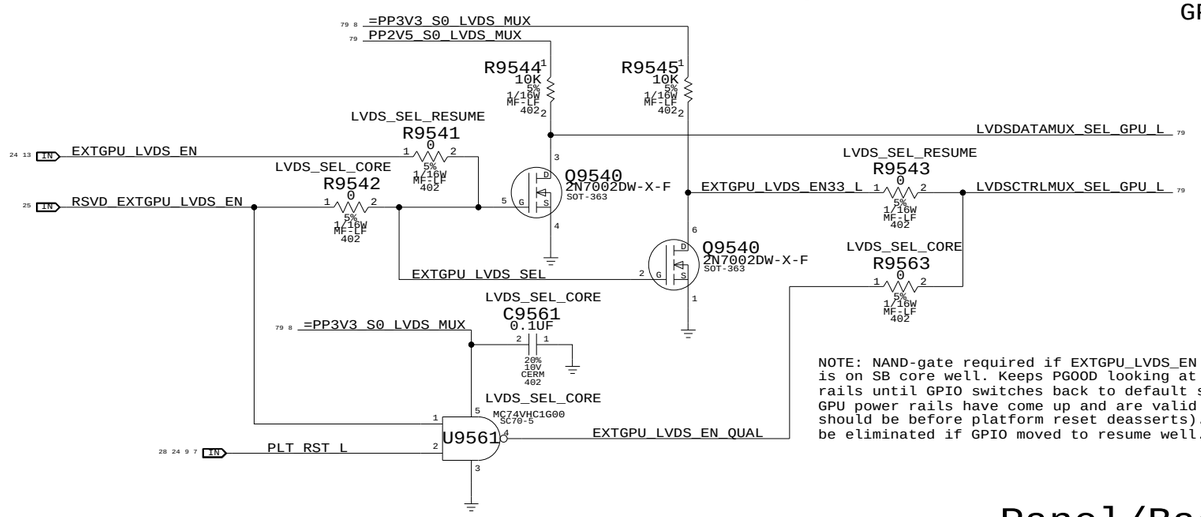
LTC2900 provides programmable reset delay which is required to play nice with ICHx PGOOD circuit



LTC2900 typical threshold is 93.5% (3.055V, 2.325V, 1.685V, 1.120V)

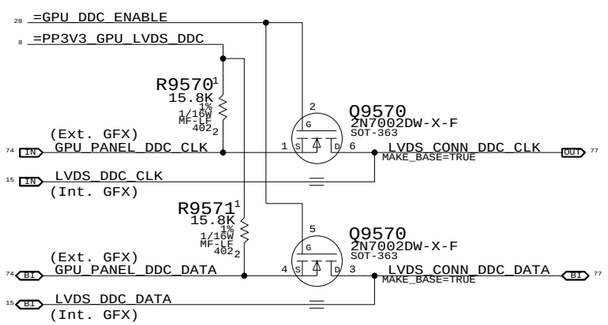
Fast wake condition is worst case. ICHx can create an S3 duration of 1 RTC clock (32 us). If mux select is on core well and AND-gate is implemented, glitch filter or <99ms PGOOD assertion time is required for PGOODs to be valid at end of 99 ms SMC timer. If mux select on resume well, then observed PGOOD will not change during S3 transitions and ICHx will honor whatever PGOOD delays are provided.

Mux Select Conditioning

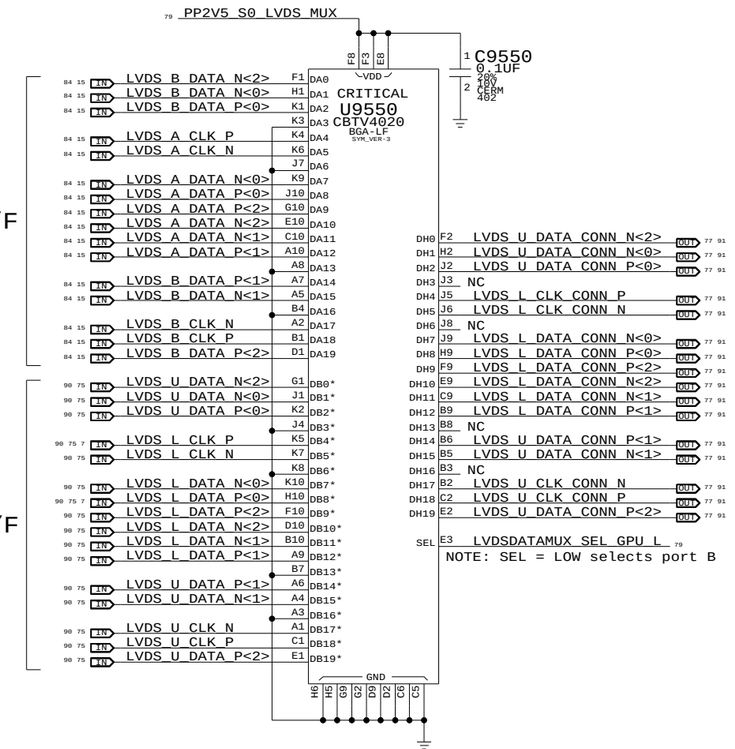


NOTE: NAND-gate required if EXTGPU_LVDS_EN GPIO is on SB core well. Keeps PGOOD looking at non-GPU rails until GPIO switches back to default state and GPU power rails have come up and are valid (which should be before platform reset deasserts). Could be eliminated if GPIO moved to resume well.

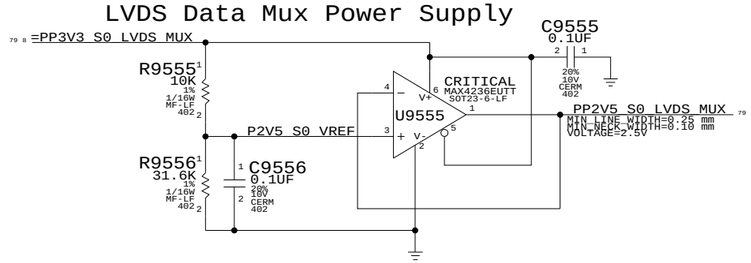
GPU DDC Pass FETs



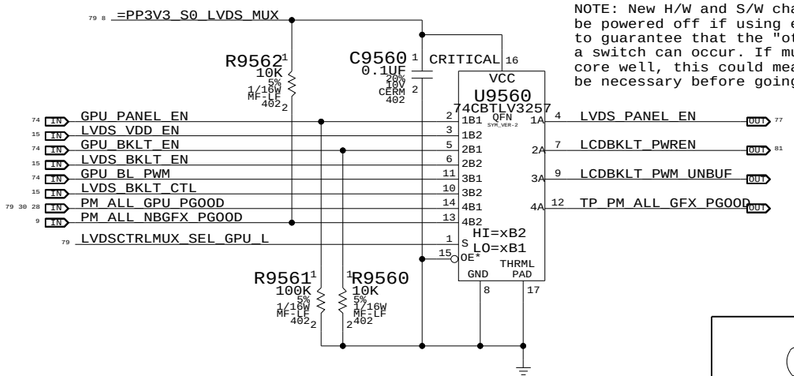
LVDS I/F Mux



LVDS Data Mux Power Supply



Panel/Backlight Control Mux



NOTE: New H/W and S/W challenge since NB gfx might be powered off if using external GPU. S/W will have to guarantee that the "other" device is ready before a switch can occur. If mux select GPIO is still on a core well, this could mean powering up IG supply will be necessary before going to sleep to keep PGOODs valid.

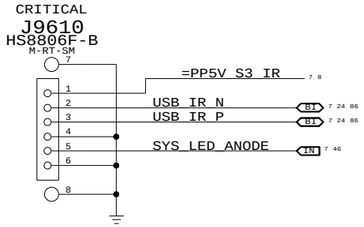
LVDS Interface Mux

SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

APPLE INC.

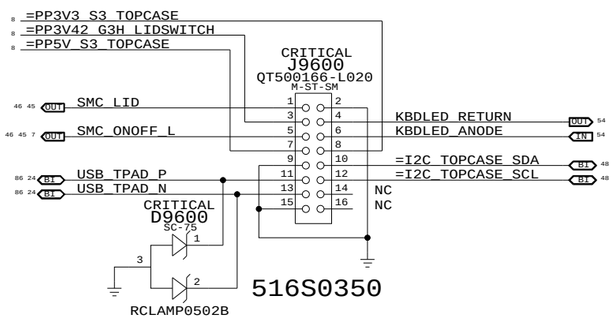
SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 95 OF 109	

IR & Sleep LED Connector



518S0474

Top-Case Connector



516S0350

Inverter Connectors

518S0369

BOM Options:
INV_SPLIT
INV_15INCH
INV_17INCH?
INV_BYPASS

J9650
SM04B-ACH
M-RT-SM

Split Inverter	Classic Inverter
INV_PWR_HV	Bridge 2	PBUS
INV_GND_HV	Bridge 1	GND
INV_P5V_HV_IFB	IFB (Current Sense)	+5V
INV_PWM_HV_VFB	VFB (Voltage Sense)	PWM

=GND_CHASSIS_LEFTCLUTCH

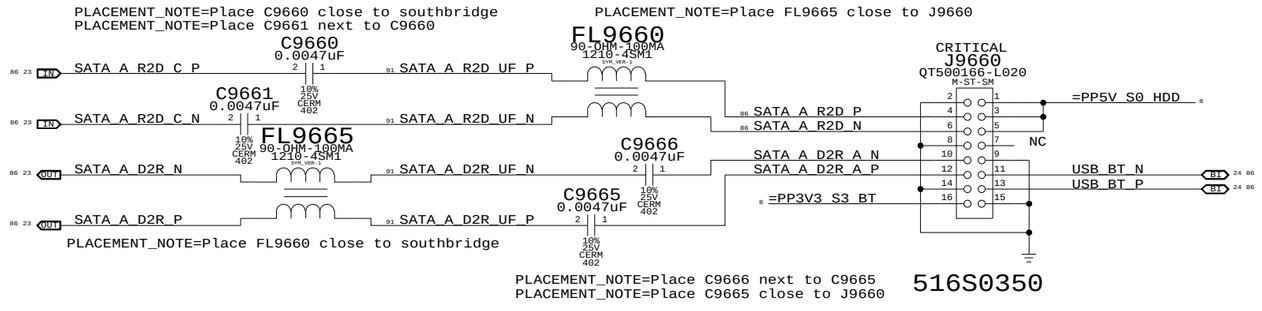
INV_SPLIT
J9655
BM02B-ACHKS-GAN-TF-LF-SN-M
M-RT-SM

INV_HV_PIN5	"Antenna" Pad	No Connect
NC	No Connect	No Connect

=GND_CHASSIS_LEFTCLUTCH

518S0487

Bluetooth (M13P) & SATA HDD Flex Connector



516S0350

M76 Specific Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

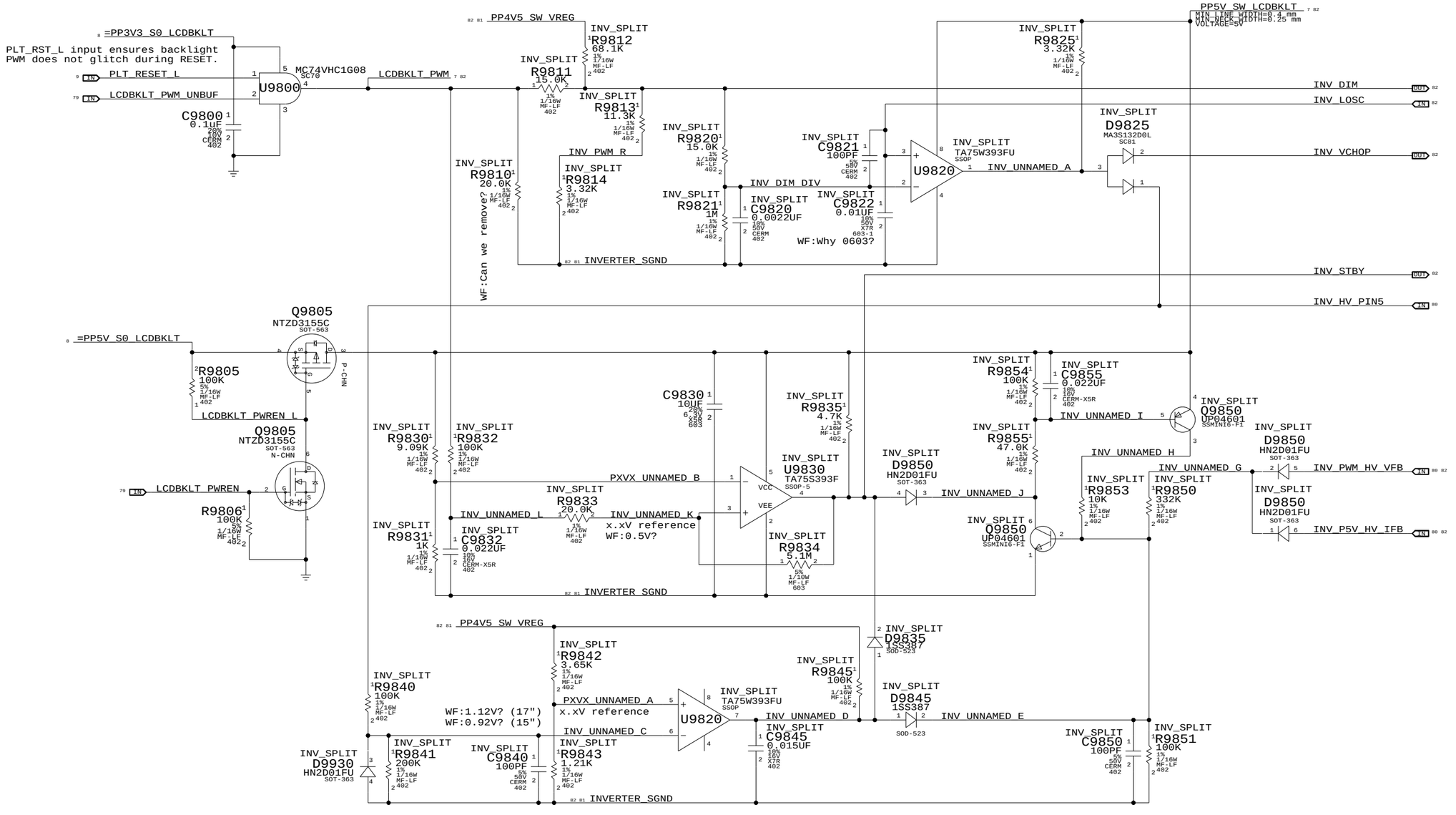
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B

SCALE: NONE

SHT 96 OF 109



Inverter Support

SYNC_MASTER=M75_LIO SYNC_DATE=01/23/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

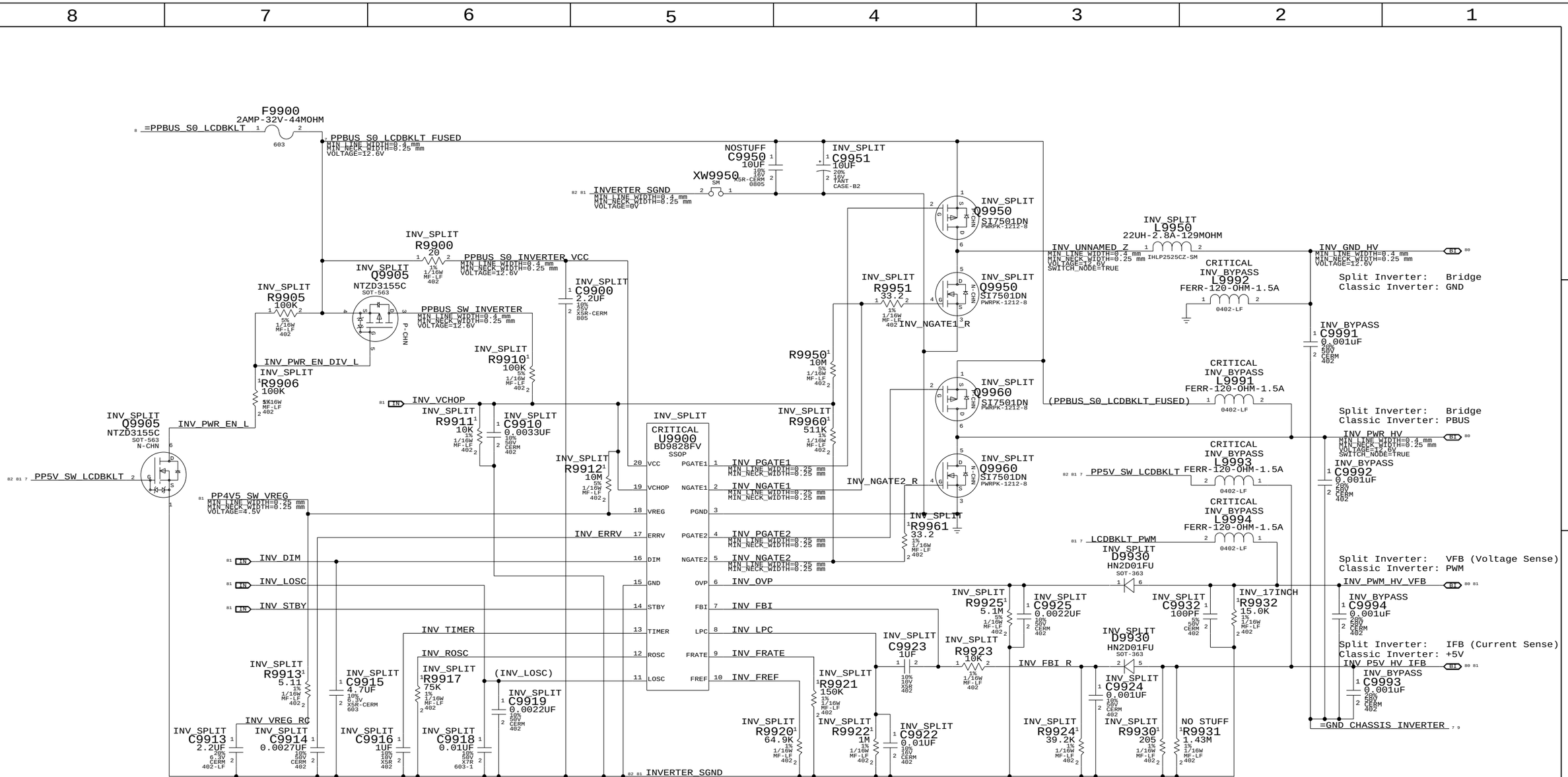
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 98 OF 109	



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0319	1	RES,11.3K,1%,1/16W,MF,402,LF	R9932		INV_15INCH

Inverter Control IC

SYNC_MASTER=M75_LIO SYNC_DATE=01/23/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B

SCALE	SHT	OF
NONE	99	109

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	?
FSB_DATA2DATA	*	=2:1_SPACING	?
FSB_DSTB	*	=3:1_SPACING	?
FSB_DATA2DSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_ADS_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BNR_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BPRI_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BREQ0_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DBSY_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DEFER_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DPWR_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DRDY_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HIT_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HITM_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_LOCK_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_TRDY_L	10 14
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB_CPURST_L	7 10 13 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_D_L<15..0>	7 10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_DINV_L<0>	7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<0>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<0>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_D_L<31..16>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_DINV_L<1>	7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<1>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<1>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_D_L<47..32>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_DINV_L<2>	7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<2>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<2>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_D_L<63..48>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_DINV_L<3>	7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<3>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_A_L<16..3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	7 10 14
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<0>	7 10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB_A_L<35..17>	7 10 14
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<1>	7 10 14
CPU_IERR_L	CPU_55S		CPU_IERR_L	10
CPU_FERR_L	CPU_55S		CPU_FERR_L	10 23
CPU_PROCHOT_L	CPU_55S	CPU_2TO1	CPU_PROCHOT_L	10 46 59
CPU_PWRGD	CPU_55S		CPU_PWRGD	7 10 13 23
CPU_FROM_SB	CPU_55S		CPU_INTR	10 23
CPU_FROM_SB	CPU_55S		CPU_NMI	10 23
CPU_FROM_SB	CPU_55S		CPU_A20M_L	10 23
CPU_FROM_SB	CPU_55S		CPU_DPSLP_L	7 10 23
CPU_FROM_SB	CPU_55S		CPU_IGNNE_L	10 23
CPU_INIT_L	CPU_55S		CPU_INIT_L	10 23 47
CPU_FROM_SB	CPU_55S		CPU_SMI_L	10 23
CPU_FROM_SB	CPU_55S		CPU_STPCLK_L	7 10 23
PM_THRMTRIP_L	CPU_55S	CPU_2TO1	PM_THRMTRIP_L	10 16 23 46
FSB_CPUSLP_L	CPU_55S		FSB_CPUSLP_L	7 10 14
PM_DPRSLPVR	CPU_55S	CPU_2TO1	PM_DPRSLPVR	7 16 25 59
(See above)	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	7 59
CPU_BSEL0	CPU_55S	CPU_2TO1	CPU_BSEL<0>	10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<0>	13 16 30
CPU_BSEL1	CPU_55S	CPU_2TO1	CPU_BSEL<1>	10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<1>	13 16 30
CPU_BSEL2	CPU_55S	CPU_2TO1	CPU_BSEL<2>	10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<2>	13 16 30
CPU_DPRSTP_L	CPU_55S	CPU_2TO1	CPU_DPRSTP_L	7 10 16 23 59
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU_GTLREF	10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<3>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<1>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10
XDP_TDI	CPU_55S	CPU_ITP	XDP_TDI	10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP_TDO	10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP_TMS	10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP_TCK	10 13
XDP_TRST_L	CPU_55S	CPU_ITP	XDP_TRST_L	10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP_BPM_L<4..0>	10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP_BPM_L<5>	10 13
	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 30 88
	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 30 88
(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP_CPURST_L	13
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	11 12
	CPU_55S	CPU_2TO1	IMVP6_VID<6..0>	7 12 59
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 59
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 59
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	59
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	59

CPU/FSB Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B

SCALE NONE SHT 100 OF 109

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CRT_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	
LVDS	*	20 MIL	?	
CRT	*	25 MIL	?	DG Says 40 mil spacing minimum
CRT_2CRT	*	20 MIL	?	
CRT_SYNC	*	25 MIL	?	DG Says 30 mil spacing minimum
CRT_SYNC2SYNC	*	20 MIL	?	
TVDAC	*	25 MIL	?	DG Says 40 mil spacing minimum
TVDAC_2TVDAC	*	20 MIL	?	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT
CRT_SYNC	CRT_SYNC	*	CRT_SYNC2SYNC
TVDAC	TVDAC	*	TVDAC_2TVDAC

LVDS signals are 100-ohm +/- 20% differential impedence.
CRT & TVDAC signal single-ended impedence varies by location:
- 37.5-ohm +/- 15% from GMCH to first termination resistor.
- 50-ohm +/- 15% from first to second termination resistor.
- 55-ohm +/- 15% from second termination resistor to connector.

CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedence.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PEG_R2D	PCIE_100D	PCIE	PEG_R2D_P<15..0>	68
	PCIE_100D	PCIE	PEG_R2D_N<15..0>	68
	PCIE_100D	PCIE	PEG_R2D_C_P<15..0>	15 68
	PCIE_100D	PCIE	PEG_R2D_C_N<15..0>	15 68
PEG_D2R	PCIE_100D	PCIE	PEG_D2R_P<15..0>	15 68
	PCIE_100D	PCIE	PEG_D2R_N<15..0>	15 68
	PCIE_100D	PCIE	PEG_D2R_C_P<15..0>	68
	PCIE_100D	PCIE	PEG_D2R_C_N<15..0>	68
DMI_N2S	DMI_100D	DMI	DMI_N2S_P<3..0>	16 24
	DMI_100D	DMI	DMI_N2S_N<3..0>	16 24
DMI_S2N	DMI_100D	DMI	DMI_S2N_P<3..0>	16 24
	DMI_100D	DMI	DMI_S2N_N<3..0>	16 24
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_P	15 79
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_N	15 79
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_P<2..0>	15 79
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_N<2..0>	15 79
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS_A_DATA_P<3>	
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS_A_DATA_N<3>	
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_P	15 79
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_N	15 79
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_P<2..0>	15 79
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_N<2..0>	15 79
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS_B_DATA_P<3>	
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS_B_DATA_N<3>	
LVDS_IBG		LVDS	LVDS_IBG	15 22
CRT_TVO_IREF		CRT	CRT_TVO_IREF	
CRT_RED	CRT_50S	CRT	CRT_RED	
CRT_GREEN	CRT_50S	CRT	CRT_GREEN	
CRT_BLUE	CRT_50S	CRT	CRT_BLUE	
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_HSYNC_R	
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_VSYNC_R	
TV_A_DAC	CRT_50S	TVDAC	TV_A_DAC	
TV_B_DAC	CRT_50S	TVDAC	TV_B_DAC	
TV_C_DAC	CRT_50S	TVDAC	TV_C_DAC	

NB Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B

SCALE NONE SHT 101 OF 109

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM_*-style wildcards!

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_CLK_P<2..0>	16 31
	MEM_70D	MEM_CLK	MEM_CLK_N<2..0>	16 31
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<1..0>	16 31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CS_L<1..0>	16 31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_ODT<1..0>	16 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_A<14..0>	16 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_BS<2..0>	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_RAS_L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_CAS_L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_WE_L	17 31 33
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A_DQ<7..0>	17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DQ<15..8>	17 31
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A_DQ<23..16>	17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DQ<31..24>	17 31
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A_DQ<39..32>	17 31
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A_DQ<47..40>	17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DQ<55..48>	17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DQ<63..56>	17 31
MEM_A_DM0	MEM_55S	MEM_DATA	MEM_A_DM<0>	17 31
MEM_A_DM1	MEM_55S	MEM_DATA	MEM_A_DM<1>	17 31
MEM_A_DM2	MEM_55S	MEM_DATA	MEM_A_DM<2>	17 31
MEM_A_DM3	MEM_55S	MEM_DATA	MEM_A_DM<3>	17 31
MEM_A_DM4	MEM_55S	MEM_DATA	MEM_A_DM<4>	17 31
MEM_A_DM5	MEM_55S	MEM_DATA	MEM_A_DM<5>	17 31
MEM_A_DM6	MEM_55S	MEM_DATA	MEM_A_DM<6>	17 31
MEM_A_DM7	MEM_55S	MEM_DATA	MEM_A_DM<7>	17 31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	17 31
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_CLK_P<5..3>	16 32
	MEM_70D	MEM_CLK	MEM_CLK_N<5..3>	16 32
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<4..3>	16 32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CS_L<3..2>	16 32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_ODT<3..2>	16 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_A<14..0>	16 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_BS<2..0>	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_RAS_L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_CAS_L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_WE_L	17 32 33
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DQ<7..0>	17 32
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B_DQ<15..8>	17 32
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B_DQ<23..16>	17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DQ<31..24>	17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DQ<39..32>	17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DQ<47..40>	17 32
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B_DQ<55..48>	17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DQ<63..56>	17 32
MEM_B_DM0	MEM_55S	MEM_DATA	MEM_B_DM<0>	17 32
MEM_B_DM1	MEM_55S	MEM_DATA	MEM_B_DM<1>	17 32
MEM_B_DM2	MEM_55S	MEM_DATA	MEM_B_DM<2>	17 32
MEM_B_DM3	MEM_55S	MEM_DATA	MEM_B_DM<3>	17 32
MEM_B_DM4	MEM_55S	MEM_DATA	MEM_B_DM<4>	17 32
MEM_B_DM5	MEM_55S	MEM_DATA	MEM_B_DM<5>	17 32
MEM_B_DM6	MEM_55S	MEM_DATA	MEM_B_DM<6>	17 32
MEM_B_DM7	MEM_55S	MEM_DATA	MEM_B_DM<7>	17 32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	17 32

Memory Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE	SHT	OF
NONE	102	109

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_60S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	20 MIL	?
USB_2CLK	*	25 MIL	?

DG says minimum spacing 50 mils to clocks

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
IDE_PDD	IDE_55S	IDE	IDE_PDD<15..0>	23 42
IDE_PDA	IDE_55S	IDE	IDE_PDA<2..0>	23 42
IDE_PDCS	IDE_55S	IDE	IDE_PDCS1_L	23 42
IDE_PDCS	IDE_55S	IDE	IDE_PDCS3_L	23 42
IDE_CNTL	IDE_55S	IDE	IDE_PDIOW_L	23 42
IDE_PDIOR_L	IDE_55S	IDE	IDE_PDIOR_L	23 42
IDE_CNTL	IDE_55S	IDE	IDE_PDDACK_L	23 42
IDE_CNTL	IDE_55S	IDE	IDE_PDDREQ	23 42
IDE_PDIORDY	IDE_55S	IDE	IDE_PDIORDY	23 42
IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14	23 42
IDE_RST_L	IDE_55S	IDE	ODD_RST_5VTOL_L	24 42
SATA_A_R2D	SATA_100D	SATA	SATA_A_R2D_C_P	23 80
	SATA_100D	SATA	SATA_A_R2D_C_N	23 80
	SATA_100D	SATA	SATA_A_R2D_P	80
	SATA_100D	SATA	SATA_A_R2D_N	80
SATA_A_D2R	SATA_100D	SATA	SATA_A_D2R_P	23 80
	SATA_100D	SATA	SATA_A_D2R_N	23 80
	SATA_100D	SATA	SATA_A_D2R_C_P	
	SATA_100D	SATA	SATA_A_D2R_C_N	
SATA_B_R2D	SATA_100D	SATA	SATA_B_R2D_C_P	23 42
	SATA_100D	SATA	SATA_B_R2D_C_N	23 42
	SATA_100D	SATA	SATA_B_R2D_P	
	SATA_100D	SATA	SATA_B_R2D_N	
SATA_B_D2R	SATA_100D	SATA	SATA_B_D2R_P	23 42
	SATA_100D	SATA	SATA_B_D2R_N	23 42
	SATA_100D	SATA	SATA_B_D2R_C_P	
	SATA_100D	SATA	SATA_B_D2R_C_N	
SATA_C_R2D	SATA_100D	SATA	SATA_C_R2D_C_P	23 42
	SATA_100D	SATA	SATA_C_R2D_C_N	23 42
	SATA_100D	SATA	SATA_C_R2D_P	
	SATA_100D	SATA	SATA_C_R2D_N	
SATA_C_D2R	SATA_100D	SATA	SATA_C_D2R_P	23 42
	SATA_100D	SATA	SATA_C_D2R_N	23 42
	SATA_100D	SATA	SATA_C_D2R_C_P	
	SATA_100D	SATA	SATA_C_D2R_C_N	
SATA_RBIAS	SATA_55S		SATA_RBIAS	42
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	23 34
	HDA_55S	HDA	HDA_BIT_CLK_R	23
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	23 34
	HDA_55S	HDA	HDA_SYNC_R	23
HDA_RST_L	HDA_55S	HDA	HDA_RST_L	23 34
	HDA_55S	HDA	HDA_RST_L_R	23
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	23 34
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	23 34
	HDA_55S	HDA	HDA_SDOUT_R	23
USB_EXTA	USB_90D	USB	USB_EXTA_P	24 43
	USB_90D	USB	USB_EXTA_N	24 43
	USB_90D	USB	USB_EXTA_MUXED_P	
	USB_90D	USB	USB_EXTA_MUXED_N	
USB_MINI	USB_90D	USB	USB_MINI_P	24 34
	USB_90D	USB	USB_MINI_N	24 34
USB_EXTD	USB_90D	USB	USB_EXTD_P	24 44
	USB_90D	USB	USB_EXTD_N	24 44
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	24 44
	USB_90D	USB	USB_CAMERA_N	24 44
USB_BT	USB_90D	USB	USB_BT_P	24 80
	USB_90D	USB	USB_BT_N	24 80
USB_TPAD	USB_90D	USB	USB_TPAD_P	24 80
	USB_90D	USB	USB_TPAD_N	24 80
USB_IR	USB_90D	USB	USB_IR_P	7 24 80
	USB_90D	USB	USB_IR_N	7 24 80
USB_EXTB	USB_90D	USB	USB_EXTB_P	24 34
	USB_90D	USB	USB_EXTB_N	24 34
USB_EXCARD	USB_90D	USB	USB_EXCARD_P	24 34
	USB_90D	USB	USB_EXCARD_N	24 34
USB_EXTC	USB_90D	USB	USB_EXTC_P	24 34
	USB_90D	USB	USB_EXTC_N	24 34
USB_RBIAS	USB_60S		USB_RBIAS	24
SMB_SB_SCL	SMB_55S	SMB	SMB_CLK	25 48
SMB_SB_SDA	SMB_55S	SMB	SMB_DATA	25 48
SMB_SB_ME_SCL	SMB_55S	SMB	SMB_ME_CLK	25 48
SMB_SB_ME_SDA	SMB_55S	SMB	SMB_ME_DATA	25 48
SPI_SCLK	SPI_55S	SPI	SPI_SCLK_R	24 56
	SPI_55S	SPI	SPI_SCLK	56
	SPI_55S	SPI	SPI_A_SCLK_R	
	SPI_55S	SPI	SPI_B_SCLK_R	
SPI_SI	SPI_55S	SPI	SPI_SI_R	24 56
	SPI_55S	SPI	SPI_SI	
	SPI_55S	SPI	SPI_A_SI_R	56
	SPI_55S	SPI	SPI_B_SI_R	
SPI_SO	SPI_55S	SPI	SPI_SO	24 56
	SPI_55S	SPI	SPI_A_SO_R	56
	SPI_55S	SPI	SPI_B_SO	
	SPI_55S	SPI	SPI_B_SO_R	
SPI_CE_L0	SPI_55S	SPI	SPI_CE_R_L<0>	24 56
	SPI_55S	SPI	SPI_CE_L<0>	56
SPI_CE_L1	SPI_55S	SPI	SPI_CE_R_L<1>	
	SPI_55S	SPI	SPI_CE_L<1>	

SB Constraints (1 of 2)

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B

SCALE	SHT	OF
NONE	103	109

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Controller Link (AMT) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLINK_12MIL	*	=STANDARD	12 MILS	5 MILS	300 MILS	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLINK	*	=1.8:1_SPACING	?
CLINK_VREF	*	12 MILS	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Ethernet (Yukon) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MILS	?

SOURCE: Based on Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCI_AD	PCI_55S	PCI	PCI_AD<18..0>	24 38
PCI_AD19	PCI_55S	PCI	PCI_AD<19>	24 38
PCI_AD20	PCI_55S	PCI	PCI_AD<20>	24 38
PCI_AD	PCI_55S	PCI	PCI_AD<31..21>	24 38
PCI_AD	PCI_55S	PCI	PCI_PAR	24 38
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>	24 38
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L	24 38
PCI_LOCK_L	PCI_55S	PCI	PCI_LOCK_L	24
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L	24 38
PCI_FW_REQ_L	PCI_55S	PCI	PCI_FW_REQ_L	24 38
PCI_FW_GNT_L	PCI_55S	PCI	PCI_FW_GNT_L	24 38
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	24
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L	
PCI_REQ2_L	PCI_55S	PCI	PCI_REQ2_L	24
PCI_GNT2_L	PCI_55S	PCI	PCI_GNT2_L	
INT_PIRQA_L	PCI_55S	PCI	INT_PIRQA_L	24
INT_PIRQB_L	PCI_55S	PCI	INT_PIRQB_L	24
INT_PIRQC_L	PCI_55S	PCI	INT_PIRQC_L	24
INT_PIRQD_L	PCI_55S	PCI	INT_PIRQD_L	24 38
INT_PIRQE_L	PCI_55S	PCI	INT_PIRQE_L	24
INT_PIRQF_L	PCI_55S	PCI	INT_PIRQF_L	24
PCIE_A_R2D	PCIE_100D	PCIE	PCIE_A_R2D_C_P	
	PCIE_100D	PCIE	PCIE_A_R2D_C_N	
PCIE_A_D2R	PCIE_100D	PCIE	PCIE_A_D2R_P	
	PCIE_100D	PCIE	PCIE_A_D2R_N	
PCIE_B_R2D	PCIE_100D	PCIE	PCIE_B_R2D_C_P	
	PCIE_100D	PCIE	PCIE_B_R2D_C_N	
PCIE_B_D2R	PCIE_100D	PCIE	PCIE_B_D2R_P	
	PCIE_100D	PCIE	PCIE_B_D2R_N	
PCIE_EXCARD_R2D	PCIE_100D	PCIE	PCIE_EXCARD_R2D_C_P	34
	PCIE_100D	PCIE	PCIE_EXCARD_R2D_C_N	34
PCIE_EXCARD_D2R	PCIE_100D	PCIE	PCIE_EXCARD_D2R_P	34
	PCIE_100D	PCIE	PCIE_EXCARD_D2R_N	34
PCIE_FW_R2D	PCIE_100D	PCIE	PCIE_FW_R2D_C_P	
	PCIE_100D	PCIE	PCIE_FW_R2D_C_N	
PCIE_FW_D2R	PCIE_100D	PCIE	PCIE_FW_D2R_P	
	PCIE_100D	PCIE	PCIE_FW_D2R_N	
PCIE_MINI_R2D	PCIE_100D	PCIE	PCIE_MINI_R2D_C_P	24 34
	PCIE_100D	PCIE	PCIE_MINI_R2D_C_N	24 34
PCIE_MINI_D2R	PCIE_100D	PCIE	PCIE_MINI_D2R_P	24 34
	PCIE_100D	PCIE	PCIE_MINI_D2R_N	24 34
GLAN_COMP			GLAN_COMP	23
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_CLK	16 25
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_DATA	16 25
CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK_NB_RESET_L	16 25
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_CLK	
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_DATA	
CLINK_WLAN_RESET_L	CLINK_55S	CLINK	CLINK_WLAN_RESET_L	
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB_CLINK_VREF	16
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF0	25
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF1	25
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE_ENET_R2D_C_P	24 35
	PCIE_100D	PCIE	PCIE_ENET_R2D_C_N	24 35
	PCIE_100D	PCIE	PCIE_ENET_R2D_P	35
	PCIE_100D	PCIE	PCIE_ENET_R2D_N	35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE_ENET_D2R_P	24 35
	PCIE_100D	PCIE	PCIE_ENET_D2R_N	24 35
	PCIE_100D	PCIE	PCIE_ENET_D2R_C_P	35
	PCIE_100D	PCIE	PCIE_ENET_D2R_C_N	35
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<0>	35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<0>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<1>	35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<1>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<2>	35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<2>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3>	35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<3>	35 37

SB Constraints (2 of 2)

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B

SCALE	SHT	OF
NONE	104	109

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_P	29 30
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_N	29 30
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_P	29 30
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_N	29 30
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_P	29 30
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_N	29 30
CK505_PCIF0	CLK_MED_55S	CLK_MED	CK505_PCIF0_CLK_ITPEN	29 30
CK505_PCIF1	CLK_MED_55S	CLK_MED	CK505_PCIF1_CLK	29 30
CK505_PCI1	CLK_MED_55S	CLK_MED	CK505_PCI1_CLK	29 30
CK505_PCI2	CLK_MED_55S	CLK_MED	CK505_PCI2_CLK	29 30
CK505_PCI3	CLK_MED_55S	CLK_MED	CK505_PCI3_CLK	29 30
CK505_PCI4	CLK_MED_55S	CLK_MED	CK505_PCI4_CLK	29 30
CK505_PCI5	CLK_MED_55S	CLK_MED	CK505_PCI5_CLK_FCTSEL	29 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_48M_FSA	29 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_REF0_FSC	29 30
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_N	29 30
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_N	29 30
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_N	29 30
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_N	29 30
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_N	29 30
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_N	29 30
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_N	29 30
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_N	29 30
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_N	29 30
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_N	29 30
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	7 10 30
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	7 10 30
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	7 14 30
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	7 14 30
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 30 83
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 30 83
(CK505_PCIF0)	CLK_MED_55S	CLK_MED	PCI_CLK33M_LPCPLUS	7 30 47
(CK505_PCIF1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SB	24 30
(CK505_PCI1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_FW	30 38
(CK505_PCI2)	CLK_MED_55S	CLK_MED	PCI_CLK33M_TPM	
(CK505_PCI3)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SMC	30 45
			CK505 PCI4 is project-specific CK505 PCI5 is project-specific	
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB_CLK48M_USBCTLR	25 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB_CLK14P3M_TIMER	25 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_FSA	30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_FSC	30
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_P	7
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_N	7
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_P	7 22 30
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_N	7 22 30
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	9
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	9
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	24 30
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	24 30
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	30 34
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	30 34
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_P	23 30
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_N	23 30
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	7 16 30
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	7 16 30
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	30 34
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	30 34
			CK505 SRC7 is project-specific	
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	30 35
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	30 35

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	48
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	48
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	48
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	48
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	48
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	48
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	48
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	48
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	48
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	48

Clock & SMC Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 105 OF 109	

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW	*	=2:1_SPACING	?
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FW_D_CTL	FW_55S	FW	FW_LINK<7..0>	
FW_D_CTL	FW_55S	FW	FW_CTL<1..0>	
FW_LCLK	CLK_MED_55S	CLK_MED	CLKFW_LINK_LCLK	
	CLK_MED_55S	CLK_MED	CLKFW_PHY_LCLK	38 39
FW_PCLK	CLK_MED_55S	CLK_MED	CLKFW_LINK_PCLK	38 39
	CLK_MED_55S	CLK_MED	CLKFW_PHY_PCLK	
FW_LKON	FW_55S	FW	FW_LKON	
	FW_55S	FW	FW_LKON_R	
FW_LPS	FW_55S	FW	FW_LPS	38 39
FW_LREQ	FW_55S	FW	FW_LREQ	38 39
FW_PINT	FW_55S	FW	FW_PINT	38 39
FWPHY_CLK98P304M_XI	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI_R	
	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI	
FW_0_TPA	FW_110D	FW_TP	FW_0_TPA_P	39 41
FW_0_TPA	FW_110D	FW_TP	FW_0_TPA_N	39 41
FW_0_TPB	FW_110D	FW_TP	FW_0_TPB_P	39 41
FW_0_TPB	FW_110D	FW_TP	FW_0_TPB_N	39 41
FW_1_TPA	FW_110D	FW_TP	FW_1_TPA_P	39 41
FW_1_TPA	FW_110D	FW_TP	FW_1_TPA_N	39 41
FW_1_TPB	FW_110D	FW_TP	FW_1_TPB_P	39 41
FW_1_TPB	FW_110D	FW_TP	FW_1_TPB_N	39 41

Port 2 Not Used

FireWire Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B

SCALE	SHT	OF
NONE	106	109

GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R50SE	*	=50_OHM_SE	=40_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR3_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TMDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
VGA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TMDS	*	20 MIL	?
VGA	*	20 MIL	?
VGA_SYNC	*	20 MIL	?

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FB_A_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<0> 70 71
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<0> 70 71
FB_B_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<1> 70 71
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<1> 70 71
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_A_MA<1..0> 70 71
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_A_MA<11..6> 70 71
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_A_BA<2..0> 70 71
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_A_RAS_L 70 71
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_A_CAS_L 70 71
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_A_WE_L 70 71
FB_AB_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB_A_CKE 70 71
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_A_CS0_L 70 71
FB_AB_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB_A_DRAM_RST 70 71
FB_A_CMD	GDDR3_50SE	GDDR3_CMD	FB_A_LMA<5..2> 70 71
FB_B_CMD	GDDR3_50SE	GDDR3_CMD	FB_A_UMA<5..2> 70 71
FB_A_WDQS0	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<0> 70 71
FB_A_WDQS1	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<1> 70 71
FB_A_WDQS2	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<2> 70 71
FB_A_WDQS3	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<3> 70 71
FB_A_RDQS0	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<0> 70 71
FB_A_RDQS1	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<1> 70 71
FB_A_RDQS2	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<2> 70 71
FB_A_RDQS3	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<3> 70 71
FB_A_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<7..0> 70 71
FB_A_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<15..8> 70 71
FB_A_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<23..16> 70 71
FB_A_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<31..24> 70 71
FB_A_DQM0	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<0> 70 71
FB_A_DQM1	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<1> 70 71
FB_A_DQM2	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<2> 70 71
FB_A_DQM3	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<3> 70 71
FB_B_WDQS0	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<4> 70 71
FB_B_WDQS1	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<5> 70 71
FB_B_WDQS2	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<6> 70 71
FB_B_WDQS3	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<7> 70 71
FB_B_RDQS0	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<4> 70 71
FB_B_RDQS1	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<5> 70 71
FB_B_RDQS2	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<6> 70 71
FB_B_RDQS3	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<7> 70 71
FB_B_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<39..32> 70 71
FB_B_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<47..40> 70 71
FB_B_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<55..48> 70 71
FB_B_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<63..56> 70 71
FB_B_DQM0	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<4> 70 71
FB_B_DQM1	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<5> 70 71
FB_B_DQM2	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<6> 70 71
FB_B_DQM3	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<7> 70 71

G84M Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
(CK505_DOT96)	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M 30
	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_GATED 30 74
CK505_CLK27MSS	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS 30
	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS_GATED 30 74
	LVDS_100D	LVDS	LVDS_L_CLK_P 7 75 79
	LVDS_100D	LVDS	LVDS_L_CLK_N 75 79
	LVDS_100D	LVDS	LVDS_L_DATA_P<3..0> 7 74 75 79
	LVDS_100D	LVDS	LVDS_L_DATA_N<3..0> 74 75 79
	LVDS_100D	LVDS	LVDS_U_CLK_P 75 79
	LVDS_100D	LVDS	LVDS_U_CLK_N 75 79
	LVDS_100D	LVDS	LVDS_U_DATA_P<3..0> 74 75 79
	LVDS_100D	LVDS	LVDS_U_DATA_N<3..0> 74 75 79
TMDS_CLK	TMDS_100D	TMDS	TMDS_CLK_P 75 78
TMDS_CLK	TMDS_100D	TMDS	TMDS_CLK_N 75 78
TMDS_DATA	TMDS_100D	TMDS	TMDS_DATA_P<5..0> 75 78
TMDS_DATA	TMDS_100D	TMDS	TMDS_DATA_N<5..0> 75 78
VGA_R_TV_C	VGA_50S	VGA	GPU_TV_C_VGA_R 74 78
VGA_G_TV_Y	VGA_50S	VGA	GPU_TV_Y_VGA_G 74 78
VGA_B_TV_COMP	VGA_50S	VGA	GPU_TV_COMP_VGA_B 74 78
	VGA_50S	VGA	GPU_VGA_R 74 75
	VGA_50S	VGA	GPU_VGA_G 74 75
	VGA_50S	VGA	GPU_VGA_B 74 75
	VGA_50S	VGA	GPU_TV_C 74 75
	VGA_50S	VGA	GPU_TV_Y 74 75
	VGA_50S	VGA	GPU_TV_COMP 74 75
VGA_SYNC	VGA_55S	VGA_SYNC	GPU_VGA_HSYNC 75 78
VGA_SYNC	VGA_55S	VGA_SYNC	GPU_VGA_VSYNC 75 78

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FB_C_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<0> 70 72
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<0> 70 72
FB_D_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<1> 70 72
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<1> 70 72
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_B_MA<1..0> 70 72
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_B_MA<11..6> 70 72
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_B_BA<2..0> 70 72
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_B_RAS_L 70 72
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_B_CAS_L 70 72
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_B_WE_L 70 72
FB_CD_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB_B_CKE 70 72
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_B_CS0_L 70 72
FB_CD_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB_B_DRAM_RST 70 72
FB_C_CMD	GDDR3_50SE	GDDR3_CMD	FB_B_LMA<5..2> 70 72
FB_D_CMD	GDDR3_50SE	GDDR3_CMD	FB_B_UMA<5..2> 70 72
FB_C_WDQS0	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<0> 70 72
FB_C_WDQS1	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<1> 70 72
FB_C_WDQS2	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<2> 70 72
FB_C_WDQS3	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<3> 70 72
FB_C_RDQS0	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<0> 70 72
FB_C_RDQS1	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<1> 70 72
FB_C_RDQS2	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<2> 70 72
FB_C_RDQS3	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<3> 70 72
FB_C_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<7..0> 70 72
FB_C_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<15..8> 70 72
FB_C_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<23..16> 70 72
FB_C_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<31..24> 70 72
FB_C_DQM0	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<0> 70 72
FB_C_DQM1	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<1> 70 72
FB_C_DQM2	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<2> 70 72
FB_C_DQM3	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<3> 70 72
FB_D_WDQS0	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<4> 70 72
FB_D_WDQS1	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<5> 70 72
FB_D_WDQS2	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<6> 70 72
FB_D_WDQS3	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<7> 70 72
FB_D_RDQS0	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<4> 70 72
FB_D_RDQS1	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<5> 70 72
FB_D_RDQS2	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<6> 70 72
FB_D_RDQS3	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<7> 70 72
FB_D_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<39..32> 70 72
FB_D_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<47..40> 70 72
FB_D_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<55..48> 70 72
FB_D_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<63..56> 70 72
FB_D_DQM0	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<4> 70 72
FB_D_DQM1	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<5> 70 72
FB_D_DQM2	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<6> 70 72
FB_D_DQM3	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<7> 70 72

GPU (G84M) Constraints

SYNC_MASTER=M75_MLB SYNC_DATE=01/26/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B

SCALE	SHT	OF
NONE	107	109

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PP1V8_MEM	*	PWR_P2MM
MEM_CMD	PP1V8_MEM	*	PWR_P2MM
MEM_CTRL	PP1V8_MEM	*	PWR_P2MM
MEM_DATA	PP1V8_MEM	*	PWR_P2MM
MEM_DQS	PP1V8_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLINK_VREF	GND	*	GND_P2MM
CLK_MED	GND	*	GND_P2MM
CLK_PCIE	GND	*	GND_P2MM
DMI	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
DMI	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM
ENET_MDI	ENET_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_MED	FW_POWER	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_70D	BOTTOM			0.127 MM	6.35 MM		

Allow 0.1 mm necks for >0.1 mm lines between thru-hole SO-DIMM pins.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	2.54 MM OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D	ISL10			0.100 MM	2.54 MM		
MEM_85D	ISL4,ISL10			0.100 MM	2.54 MM		

Graphics Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE_100D	*	100_DIFF_BGA
LVDS_100D	*	100_DIFF_BGA
TMDS_100D	*	100_DIFF_BGA

SIM Card Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
WWAN_SIM	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
WWAN_SIM	*	=2:1_SPACING	?

M76 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
(PCIE_EXCARD)	PCIE_100D	PCIE	PCIE_EXCARD_R2D_P 34
(PCIE_EXCARD)	PCIE_100D	PCIE	PCIE_EXCARD_R2D_N 34
(PCIE_MINI)	PCIE_100D	PCIE	PCIE_MINI_R2D_P 34
(PCIE_MINI)	PCIE_100D	PCIE	PCIE_MINI_R2D_N 34
	ENET_100D	ENET_MDI	ENET_MDI_R_P<3..0>
	ENET_100D	ENET_MDI	ENET_MDI_R_N<3..0>
	ENET_100D	ENETCONN	ENETCONN_P<3..0> 37
	ENET_100D	ENETCONN	ENETCONN_N<3..0> 37
	FW_110D	FW_TP	FW_PORT0_TPA_FL_P 41
	FW_110D	FW_TP	FW_PORT0_TPA_FL_N 41
	FW_110D	FW_TP	FW_PORT0_TPB_FL_P 41
	FW_110D	FW_TP	FW_PORT0_TPB_FL_N 41
(SATA_A_R2D)	SATA_100D	SATA	SATA_A_R2D_UF_P 80
(SATA_A_R2D)	SATA_100D	SATA	SATA_A_R2D_UF_N 80
(SATA_A_D2R)	SATA_100D	SATA	SATA_A_D2R_UF_P 80
(SATA_A_D2R)	SATA_100D	SATA	SATA_A_D2R_UF_N 80
(USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_P 43
(USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_N 43
(USB_EXTA)	USB_90D	USB	USB2_RT_P 43
(USB_EXTA)	USB_90D	USB	USB2_RT_N 43
(USB_EXTD)	USB_90D	USB	USB_WWAN_F_P 7 44
(USB_EXTD)	USB_90D	USB	USB_WWAN_F_N 7 44
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_F_P 7 44
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_F_N 7 44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFXIMVP6_VSEN_P 60
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	NBCOREISNS_P 50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8ISNS_P 50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V25ISNS_P 50
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P 7 51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P 10 51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P 51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P 51 74
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	HSTHMSNS_D_P 7 51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	REMTHMSNS_DX_P
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	RSFSTHMSNS_D_P 7 51
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_F_P 77
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_F_N 77
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_P 77 79
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_N 77 79
	LVDS_100D	LVDS	LVDS_L_DATA_CONN_P<3..0> 77 79
	LVDS_100D	LVDS	LVDS_L_DATA_CONN_N<3..0> 77 79
	LVDS_100D	LVDS	LVDS_U_CLK_CONN_P 77 79
	LVDS_100D	LVDS	LVDS_U_CLK_CONN_N 77 79
	LVDS_100D	LVDS	LVDS_U_DATA_CONN_P<3..0> 77 79
	LVDS_100D	LVDS	LVDS_U_DATA_CONN_N<3..0> 77 79
	TMDS_100D	TMDS	TMDS_CLK_R_P 78
	TMDS_100D	TMDS	TMDS_CLK_R_N 78
	TMDS_100D	TMDS	TMDS_CLK_F_P 78
	TMDS_100D	TMDS	TMDS_CLK_F_N 78
	TMDS_100D	TMDS	TMDS_DATA_F_P<5..0> 78
	TMDS_100D	TMDS	TMDS_DATA_F_N<5..0> 78
(VGA_R_TV_Y)	VGA_50S	VGA	VGA_R 78
(VGA_G_TV_C)	VGA_50S	VGA	VGA_G 78
(VGA_B_TV_COMP)	VGA_50S	VGA	VGA_B 78
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_HSYNC_R 78
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_VSYNC_R 78
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_HSYNC 78
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_VSYNC 78
		PP1V8_MEM	=PP1V8_S3M_MEM_A 8 31
		PP1V8_MEM	=PP1V8_S3M_MEM_B 8 32
		GND	GND
		SB_POWER	PP3V3_S5 8
		SB_POWER	PP3V3_S0 8 66
		SB_POWER	PP1V5_S0 8
(SIM)	WWAN_SIM	WWAN_SIM	WWAN_SIM_CLOCK 44
(SIM)	WWAN_SIM	WWAN_SIM	WWAN_SIM_DATA 44

ENET_POWER

FW_POWER

M76 Specific Constraints

SYNC_MASTER=M76_MLB SYNC_DATE=02/02/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B
SCALE: NONE	SHT 108 OF 109	

M75/M76 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	ISL2,ISL11	Y	0.250 MM	0.076 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.125 MM	0.125 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.131 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL9,ISL10	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL2,ISL11	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM
80_OHM_DIFF	ISL9,ISL10	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM
85_OHM_DIFF	ISL9,ISL10	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y		0.075 MM			0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y		0.075 MM			0.125 MM
100_DIFF_BGA	ISL2,ISL11	Y		0.085 MM			0.140 MM
100_DIFF_BGA	TOP,BOTTOM	Y		0.085 MM			0.140 MM

NOTE: 100_DIFF_BGA is for select 100-ohm differential pairs with routing difficulties through BGAs.
Default width/spacing is 100-ohm differential, but pairs can neck to 95-ohms without DRC.

M75/M76 Rule Definitions

SYNC_MASTER=M76_MLB SYNC_DATE=02/02/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7520	B

SCALE NONE SHT 109 OF 109