1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

Mullet

M1 MLB
09/26/2005

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
?		?	?	?	?

Page (.csa)	Contents	Sync Date
1 1	Table of Contents	N/A N/A
2 2	System Block Diagram	N/A N/A
3 3	Power Block Diagram	N/A N/A
4 4	BOM Configuration	N/A N/A
5 5	Functional / ICT Test	N/A N/A
6 6	Signal Aliases	N/A N/A
7 7	CPU 1 OF 2-FSB	M42 09/08/2005
8 8	CPU 2 OF 2-PWR/GND	M42 09/08/2005
9 9	CPU Decoupling & VID	(MASTER) (MASTER)
10 10	CPU MISC1-TEMP SENSOR	M42 09/08/2005
11 11	CPU ITP700FLEX DEBUG	M42 09/08/2005
12 12	NB CPU Interface	(MASTER) (MASTER)
13 13	NB PEG / Video Interfaces	(MASTER) (MASTER)
14 14	NB Misc Interfaces	(MASTER) (MASTER)
15 15	NB DDR2 Interfaces	(MASTER) (MASTER)
16 16	NB Power 1	(MASTER) (MASTER)
17 17	NB Power 2	(MASTER) (MASTER)
18 18	NB Grounds	(MASTER) (MASTER)
19 19	NB (GM) Decoupling	(MASTER) (MASTER)
20 20	NB Config Straps	(MASTER) (MASTER)
21 21		M38 09/08/2005
22 22		M38 09/08/2005
23 23		M38 09/08/2005
24 24		M38 09/08/2005
25 25		M42 09/08/2005
26 26	SB Misc	(MASTER) (MASTER)
27 27	M1 SMBus Connections	(MASTER) (MASTER)
28 28	DDR2 SO-DIMM Connector A	(MASTER) (MASTER)
29 29	DDR2 SO-DIMM Connector B	(MASTER) (MASTER)
30 30	Memory Active Termination	(MASTER) (MASTER)
31 31	Memory Vtt Supply	(MASTER) (MASTER)
32 32	DDR2 VRef	(MASTER) (MASTER)
33 33	CLOCKS	M42 09/08/2005
34 34	Clock Termination	(MASTER) (MASTER)
35 37	Mobile Clocking	(MASTER) (MASTER)
36 38	PATA Connector	(MASTER) (MASTER)
37 41	ETHERNET CONTROLLER	M42 09/08/2005
38 42	Ethernet Connector	(MASTER) (MASTER)
39 44	FIREWIRE CONTROLLER	M42 08/29/2005
40 45	FireWire Port Power	(MASTER) (MASTER)
41 46	FireWire Ports	(MASTER) (MASTER)
42 49	Internal USB Connections	(MASTER) (MASTER)
43 52	External USB Connector	(MASTER) (MASTER)
44 55	Left I/O Board Connector	(MASTER) (MASTER)
45 57	PCI-E Connections	(MASTER) (MASTER)
46 58		M38 09/08/2005
47 59	SMC Support	(MASTER) (MASTER)
48 60	LPC+ Debug Connector	M42 07/20/2005
49 61	Thermal Sensors	(MASTER) (MASTER)
50 62	Current & Voltage Sensing	(MASTER) (MASTER)
51 63	SPI BOOTROM	(M42) 07/26/2005
52 64	ALS Support	(MASTER) (MASTER)
53 65	Fan Connectors	(MASTER) (MASTER)
54 66	SMS	(M42) 07/26/2005
55 67		M38 09/08/2005
56 75	IMVP6 CPU VCore Regulator	(MASTER) (MASTER)
57 76	5V / 1.5V Power Supply	(MASTER) (MASTER)
58 77	2.5V & 1.2V Regulators	(MASTER) (MASTER)
59 78	1.8V Supply	(MASTER) (MASTER)
60 79	3.3V / 1.05V Power Supplies	(MASTER) (MASTER)
61 80	3.3V G3Hot Supply	(MASTER) (MASTER)
62 81	Power Aliases	(MASTER) (MASTER)
63 82	PBus-In & Battery Connectors	(MASTER) (MASTER)
64 83	S3/S0 FETs & Power Control	(MASTER) (MASTER)
65 84	ATI M56 PCI-E	(MASTER) (MASTER)
66 85	GPU (M56) Core Supplies	(MASTER) (MASTER)
67 86	ATI M56 Core Power	(MASTER) (MASTER)
68 87	ATI M56 Frame Buffer I/F	(MASTER) (MASTER)
69 88	GPU Straps	(MASTER) (MASTER)
70 89	GDDR3 Frame Buffer A	(MASTER) (MASTER)
71 90	GDDR3 Frame Buffer B	(MASTER) (MASTER)
72 91	ATI M56 GPIO/DVO/Misc	(MASTER) (MASTER)
73 93	ATI M56 Video Interfaces	(MASTER) (MASTER)
74 94	Internal Display Connectors	(MASTER) (MASTER)
75 97	External Display Connector	(MASTER) (MASTER)
76 99	Physical Security	(MASTER) (MASTER)
77 100	Revision History	N/A N/A
78 101	Napa Platform Constraints	(MASTER) (MASTER)
79 102	More System Constraints	(MASTER) (MASTER)
80 103	M1 Spacing & Physical Constraints	(MASTER) (MASTER)
81 104	M1 Net Properties	(MASTER) (MASTER)

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-6941	1	SCHEM,MULLET,M1	SCH		
820-1881	1	PCBF,MULLET,M1	PCB		
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:TSQ]	CRITICAL	VRAM_128
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:TYY]	CRITICAL	VRAM_256

DRAWING
TITLE=MULLET
ABBREV=DRAWING
LAST_MODIFIED=Mon Sep 26 13:38:08 2005

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

TITLE
SCHEM,MULLET,M1

DRAWING NUMBER 051-6941 REV. 07001

SHT 1 OF 81

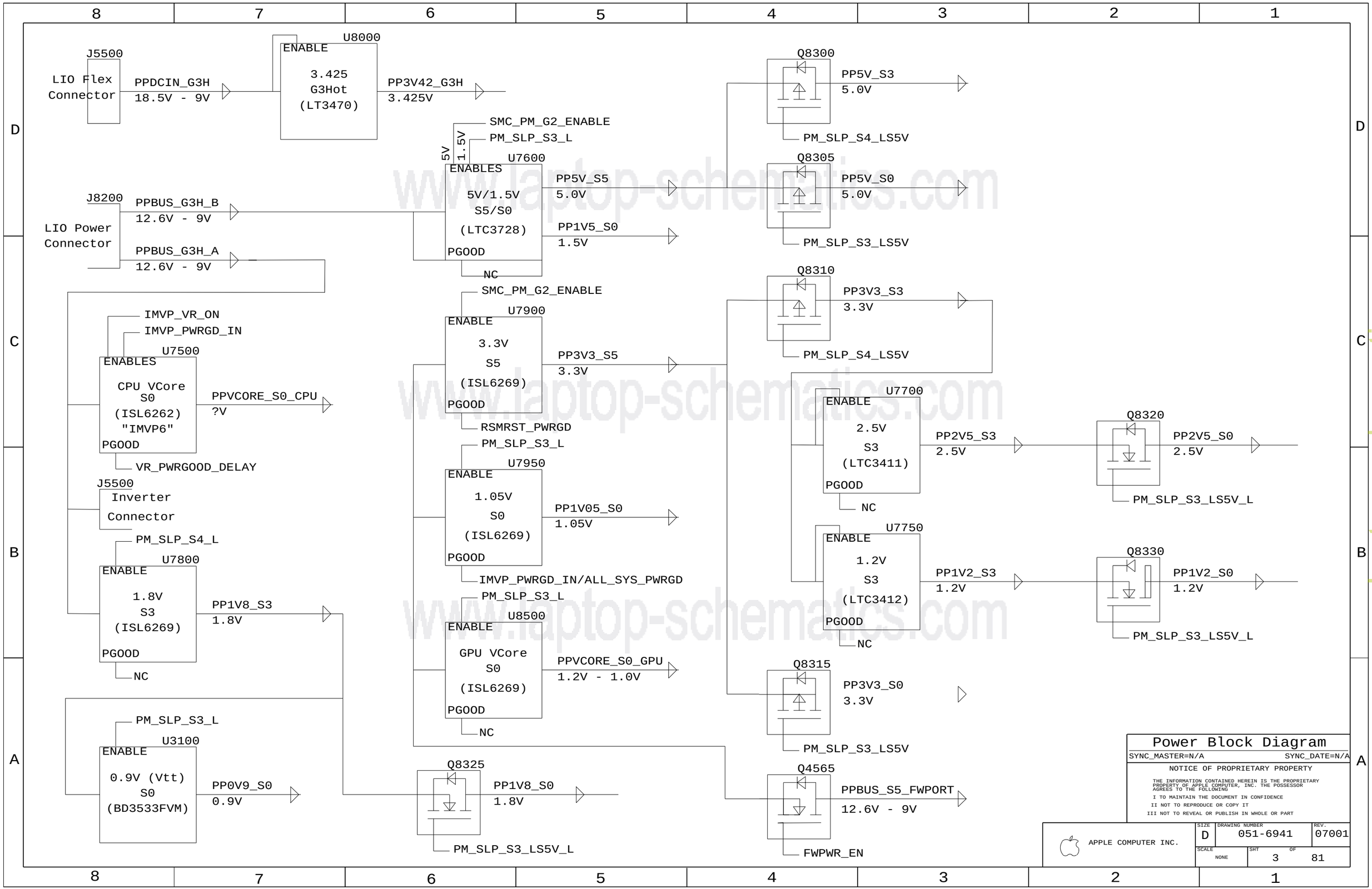
System Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	2	81



Power Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	3	81

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7207	PCBA,MULLET_128,M1	075-0137,075-0139,075-0140
630-7254	PCBA,MULLET_256,M1	075-0138,075-0139,075-0140
075-0137	128,MULLET,M1	VRAM_128
075-0138	256,MULLET,M1	VRAM_256,GPU_MEM_256M
075-0139	PROJ_PTS,MULLET,M1	COMMON,M1_COMMON1,M1_COMMON2,M1_DEBUG
075-0140	LEMENU_PTS,MULLET,M1	LEMENU_STAGE2,LEMENU_STAGE3

BOM GROUP	BOM OPTIONS
M1_COMMON1	GPU_BB_CTL,GPUTHM_A_GPU,HSTHMSNS_HAS,INVERTER_BUF,KBDLED_HAS,LEMENU_STAGE1
M1_COMMON2	MEMVREF_S3,MEMVTT_EN_PU,PLTRST_GATE_STUFF,USB_C_OC_PU,USB_D_OC_PU,USB_E_OC_PU
M1_DEBUG	DEVELOPMENT,ITP,LPCPLUS

Phantom BOM #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
075-0137	1	128,MULLET,M1	BOM1		075-0137
075-0138	1	256,MULLET,M1	BOM2		075-0138
075-0139	1	PROJ PTS,MULLET,M1	BOM3		075-0139
075-0140	1	LeMENU PTS,MULLET,M1	BOM4		075-0140

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0354	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128
333S0350	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256

"LeMenu Stage #1" Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
338S0266	1	IC,ATI,M56P,GRPHSCTRL,880BGA,LF	U8400	CRITICAL	LEMENU_STAGE1	
338S0268	1	IC,FW32306,1394A LINK,BGA,129P	U4400	CRITICAL	LEMENU_STAGE1	
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN, NO	U4101	CRITICAL	LEMENU_STAGE1	
338S0274	1	IC,SMC,HS8/2116	U5800	CRITICAL	LEMENU_STAGE1	
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U4102	CRITICAL	LEMENU_STAGE1	
341S1812	1	IC,EFI,BOOTROM DEVELOPMENT,M1	U6301	CRITICAL	LEMENU_STAGE1	341S1813 is production BootROM
353S1235	1	IC,CPU VOLTAGE REGULATOR,IMVP,TWO PHASE	U7530	CRITICAL	LEMENU_STAGE1	
359S0101	1	IC,CY28445-5,CLOCK GEN,68PIN QFN	U3301	CRITICAL	LEMENU_STAGE1	

"LeMenu Stage #2" Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S1789	1	IC, TPM, 28-PIN TSSOP	U6700	CRITICAL	LEMENU_STAGE2

"LeMenu Stage #3" Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3208	1	IC,YONAH CPU,479 BGA	U0700	CRITICAL	LEMENU_STAGE3
338S0269	1	IC,945GM,SOUTHBRIDGE	U1200	CRITICAL	LEMENU_STAGE3
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	LEMENU_STAGE3

BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE NONE SHT 4 OF 81

Functional Test Points

Power Supply NO_TESTs

NO_TEST

TRUE	IMVP6_RBIAS	56
TRUE	IMVP6_COMP	56
TRUE	P5VS5_RUNSS	57 64
TRUE	P1V5S0_RUNSS	57 64
TRUE	P2V5S3_MODE	58
TRUE	P2V5S3_SHDNRT	58 64
TRUE	P1V2S3_RT	58
TRUE	P1V2S3_RUNSS	58 64
TRUE	P1V8S3_COMP	59
TRUE	P1V8S3_FSET	59
TRUE	P3V3S5_COMP	60
TRUE	P3V3S5_FSET	60
TRUE	P1V05S0_COMP	60
TRUE	P1V05S0_FSET	60
TRUE	P3V42G3H_FB	61
TRUE	GPUVCORE_COMP	66
TRUE	GPUVCORE_FSET	66
TRUE	GPUBBP_ADJ	66

CPU FSB NO_TESTs

NO_TEST

TRUE	FSB_A_L<31..3>	7 12 81
TRUE	FSB_ADS_L	7 12 81
TRUE	FSB_ADSTB_L<1..0>	7 12 81
TRUE	FSB_BNR_L	7 12 81
TRUE	FSB_BREQ0_L	7 12 81
TRUE	FSB_D_L<63..0>	7 12 81
TRUE	FSB_DBSY_L	7 12 81
TRUE	FSB_DINV_L<3..0>	7 12 81
TRUE	FSB_DRDY_L	7 12 81
TRUE	FSB_DSTBN_L<3..0>	7 12 81
TRUE	FSB_DSTBP_L<3..0>	7 12 81
TRUE	FSB_HIT_L	7 12 81
TRUE	FSB_HITM_L	7 12 81
TRUE	FSB_LOCK_L	7 12 81
TRUE	FSB_REQ_L<4..0>	7 12 81

FUNC_TEST property removed since these test points are not on the proper side for Functional Test points.

Fan Connectors

FUNC_TEST

	=PP5V_S0_FAN_LT	53 62
	FAN_LT_PWM	53
	FAN_LT_TACH	53
	FAN_RT_PWM	53
	FAN_RT_TACH	53

LPC+ Debug Connector

FUNC_TEST

TRUE	=PP3V3_S5_LPCPLUS	48 62
TRUE	=PP5V_S0_LPCPLUS	48 62
TRUE	LPC_AD<0>	21 46 48 55
TRUE	LPC_AD<1>	21 46 48 55
TRUE	LPC_FRAME_L	21 46 48 55
TRUE	PM_CLKRUN_L	23 39 46 48 55
TRUE	BOOT_LPC_SPI_L	22 46 48 76
TRUE	SMC_TMS	46 47 48
TRUE	DEBUG_RST_L	26 48
TRUE	SMC_TRST_L	46 48
TRUE	SMC_TDO	46 47 48
TRUE	SMC_MD1	46 48
TRUE	SMC_TX_L	46 47 48
TRUE	FWH_INIT_L	21 47 48
TRUE	PCI_CLK_PORT80_LPC	34 48
TRUE	LPC_AD<2>	21 46 48 55
TRUE	LPC_AD<3>	21 46 48 55
TRUE	INT_SERIRQ	23 46 48 55
TRUE	PM_SUS_STAT_L	23 46 48 55
TRUE	SMC_TDI	46 47 48
TRUE	SMC_TCK	46 47 48
TRUE	SMC_RST_L	46 47 48
TRUE	SMC_NMI	46 48
TRUE	SMC_RX_L	46 47 48
TRUE	SV_SET_UP	23 48

Other Func Test Points

FUNC_TEST

TRUE	=PP1V05_S0_REG	50 60 62

Battery Digital Connector

FUNC_TEST

TRUE	SMC_BS_ALRT_L	46 47 63
TRUE	=SMBUS_BATT_SCL	27 63
TRUE	=SMBUS_BATT_SDA	27 63
TRUE	GND_BATT	63

Left I/O Data Connector

FUNC_TEST

TRUE	=PP1V5_S0_LIO	44 62
TRUE	=PPDCIN_G3H_LIO	44 62
TRUE	=PP5V_S5_LIO	44 62
TRUE	=PP3V42_G3H_LIO	44 62
TRUE	PP5V_S0_AUDIO_PWR	44
TRUE	PP5V_S0_AUDIO	44
TRUE	GND_AUDIO_PWR	44
TRUE	GND_AUDIO	44
TRUE	ACZ_SDATAIN<0>	21 44 81
TRUE	ACZ_SDATAOUT	21 44 81
TRUE	ACZ_BITCLK	21 44 81
TRUE	ACZ_RST_L	21 44 81
TRUE	EXCARD_OC_L	6 44 47
TRUE	LTUSB_OC_L	6 44
TRUE	LIO_BATT_ISENSE	44 50
TRUE	SMC_SYS_ISET	44 46
TRUE	SMC_BATT_ISET	44 46
TRUE	SMC_BATT_CHG_EN	44 46 47
TRUE	SMC_BC_ACOK	44 46 47
TRUE	SMC_ADAPTER_EN	40 44 46 47
TRUE	LIO_P3V3S0_EN_L	44 64
TRUE	LIO_DCIN_ISENSE	44 50
TRUE	LIO_P3V3S3_EN	44 64
TRUE	SMC_BATT_TRICKLE_EN_L	44 46 47
TRUE	SYS_ONEWIRE	44 46 47
TRUE	MINI_CLKREQ_L	34 44
TRUE	SMC_EXCARD_CP	44 46 47
TRUE	EXCARD_CLKREQ_L	34 44
TRUE	SMC_EXCARD_PWR_EN	44 46
TRUE	LIO_PLT_RESET_L	26 44
TRUE	ACZ_SYNC	21 44 81
TRUE	=USB2_LT_N	6 44
TRUE	=USB2_LT_P	6 44
TRUE	=USB2_EXCARD_N	6 44
TRUE	=USB2_EXCARD_P	6 44
TRUE	=PCIE_EXCARD_R2D_N	44 45
TRUE	=PCIE_EXCARD_R2D_P	44 45
TRUE	=PCIE_EXCARD_D2R_N	44 45
TRUE	=PCIE_EXCARD_D2R_P	44 45
TRUE	PCIE_CLK100M_EXCARD_P	34 44
TRUE	PCIE_CLK100M_EXCARD_N	34 44
TRUE	=USB2_MINI_N	6 44
TRUE	=USB2_MINI_P	6 44
TRUE	=PCIE_MINI_R2D_N	44 45
TRUE	=PCIE_MINI_R2D_P	44 45
TRUE	=PCIE_MINI_D2R_N	44 45
TRUE	=PCIE_MINI_D2R_P	44 45
TRUE	PCIE_CLK100M_MINI_P	34 44
TRUE	PCIE_CLK100M_MINI_N	34 44
TRUE	=SMBUS_LIO_SMC_SCL	27 44
TRUE	=SMBUS_LIO_SMC_SDA	27 44
TRUE	=SMBUS_LIO_SB_SCL	27 44
TRUE	=SMBUS_LIO_SB_SDA	27 44
TRUE	PCIE_WAKE_L	23 37 44

Left I/O Power Connector

FUNC_TEST

TRUE	=PPBUS_G3H_LIO_CONN	62 63
TRUE	GND	

Request for at least 10 GND test points

Functional / ICT Test

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	5	81

NC_CPU_A32_L — TP_CPU_A32_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_A33_L — TP_CPU_A33_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_A34_L — TP_CPU_A34_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_A35_L — TP_CPU_A35_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_A36_L — TP_CPU_A36_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_A37_L — TP_CPU_A37_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_A38_L — TP_CPU_A38_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_A39_L — TP_CPU_A39_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_APM0_L — TP_CPU_APM0_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_APM1_L — TP_CPU_APM1_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_EXTBREF — TP_CPU_EXTBREF (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_HFPLL — TP_CPU_HFPLL (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_SPARE0 — TP_CPU_SPARE0 (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_SPARE1 — TP_CPU_SPARE1 (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_SPARE2 — TP_CPU_SPARE2 (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_SPARE4 — TP_CPU_SPARE4 (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_MEM_A_A<15..14> — MEM_A_A<15..14> (28)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_MEM_B_A<15..14> — MEM_B_A<15..14> (29)
MAKE_BASE=TRUE, NO_TEST=TRUE

TP_NB_CFG<4..3> — NB_CFG<4..3> (14)
MAKE_BASE=TRUE

TP_NB_CFG<6> — NB_CFG<6> (14)
MAKE_BASE=TRUE

TP_NB_CFG<8> — NB_CFG<8> (14)
MAKE_BASE=TRUE

TP_NB_CFG<11..10> — NB_CFG<11..10> (14)
MAKE_BASE=TRUE

TP_NB_CFG<15..14> — NB_CFG<15..14> (14)
MAKE_BASE=TRUE

TP_NB_CFG<17> — NB_CFG<17> (14)
MAKE_BASE=TRUE

NOTE: NB_CFG<13..12> require test access

TP_NB_CFG<13..12> — NB_CFG<13..12> (14)
MAKE_BASE=TRUE

TP_SB_SUS_CLK — SUS_CLK_SB (23)
MAKE_BASE=TRUE

NC_ENET_CTRL12 — ENET_CTRL12 (37)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_ENET_CTRL25 — ENET_CTRL25 (37)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_FWPWR_PWRON — =FWPWR_PWRON (40)
MAKE_BASE=TRUE, NO_TEST=TRUE

USB Port "A" (Debug Port) = Right USB 2.0 Port

=USB2_RT_P (43) — USB2_RT_P (MAKE_BASE=TRUE) — USB_A_P (22)
=USB2_RT_N (43) — USB2_RT_N (MAKE_BASE=TRUE) — USB_A_N (22)
=RTUSB_OC_L (43) — RTUSB_OC_L (MAKE_BASE=TRUE) — USB_A_OC_L (22)

USB Port "B" = PCI-E Mini Card

=USB2_MINI_P (44,5) — USB2_MINI_P (MAKE_BASE=TRUE) — USB_B_P (22)
=USB2_MINI_N (44,5) — USB2_MINI_N (MAKE_BASE=TRUE) — USB_B_N (22)
UNUSED_USB_B_OC_L (MAKE_BASE=TRUE) — USB_B_OC_L (22)

USB Port "C" = Left USB 2.0 Port

=USB2_LT_P (44,5) — USB2_LT_P (MAKE_BASE=TRUE) — USB_C_P (22)
=USB2_LT_N (44,5) — USB2_LT_N (MAKE_BASE=TRUE) — USB_C_N (22)
LTUSB_OC_L (44,5) (MAKE_BASE=TRUE) — USB_C_OC_L (22)

USB Port "D" = Camera

=USB2_CAMERA_P (42) — USB2_CAMERA_P (MAKE_BASE=TRUE) — USB_D_P (22)
=USB2_CAMERA_N (42) — USB2_CAMERA_N (MAKE_BASE=TRUE) — USB_D_N (22)
UNUSED_USB_D_OC_L (MAKE_BASE=TRUE) — USB_D_OC_L (22)

USB Port "E" = ExpressCard

=USB2_EXCARD_P (44,5) — USB2_EXCARD_P (MAKE_BASE=TRUE) — USB_E_P (22)
=USB2_EXCARD_N (44,5) — USB2_EXCARD_N (MAKE_BASE=TRUE) — USB_E_N (22)
EXCARD_OC_L (47,44,5) (MAKE_BASE=TRUE) — USB_E_OC_L (22)

USB Port "F" = IR Receiver

=USB_IR_P — TP_USB_IRP (MAKE_BASE=TRUE) — USB_F_P (22)
=USB_IR_N — TP_USB_IRN (MAKE_BASE=TRUE) — USB_F_N (22)

USB Port "G" = Bluetooth (M13P)

=USB_BT_P (42) — USB_BT_P (MAKE_BASE=TRUE) — USB_G_P (22)
=USB_BT_N (42) — USB_BT_N (MAKE_BASE=TRUE) — USB_G_N (22)

USB Port "H" = Trackpad (Geyser)

=USB_TRACKPAD_P (42) — USB_TRACKPAD_P (MAKE_BASE=TRUE) — USB_H_P (22)
=USB_TRACKPAD_N (42) — USB_TRACKPAD_N (MAKE_BASE=TRUE) — USB_H_N (22)

Chassis connection to be made at the mounting hole northwest of the DVI connector

ZT0600
HOLE-VIA-P5RP25
1 — GND_CHASSIS_DVI_TOP
MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE
— =GND_CHASSIS_DVI2 (75)
— =GND_CHASSIS_DVI4 (75)

Chassis connection to be made at the mounting hole southwest of the USB connector

ZT0601
HOLE-VIA-P5RP25
1 — GND_CHASSIS_DVI_BOT
MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE
— =GND_CHASSIS_DVI1 (75)
— =GND_CHASSIS_DVI3 (75)
— =GND_CHASSIS_ENET (38)
— =GND_CHASSIS_FW_EMI (41)
— =GND_CHASSIS_FW_PORT1 (41)
— =GND_CHASSIS_RTUSB (43)

Chassis connection to be made at the mounting hole east of the LVDS connector

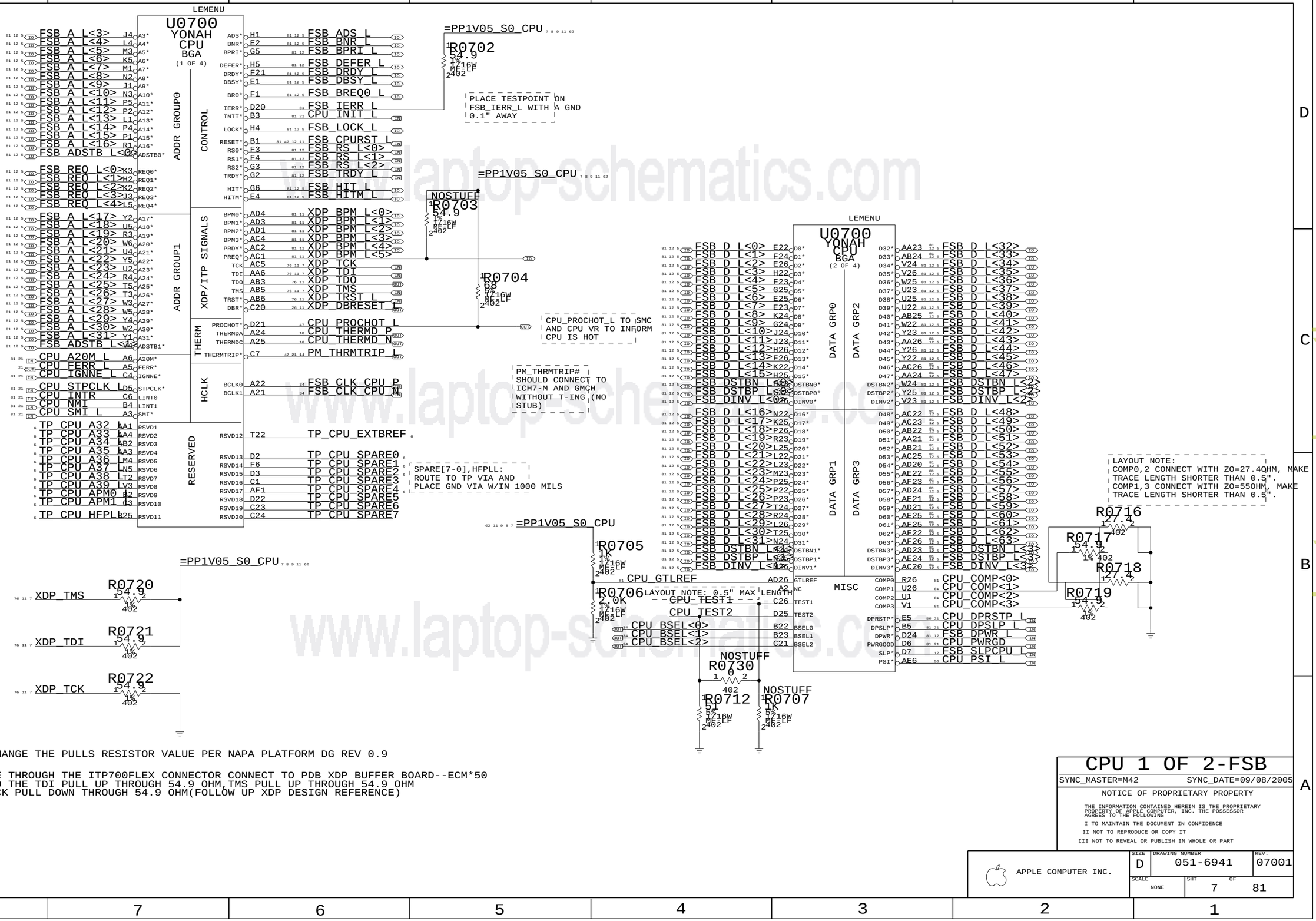
ZT0602
HOLE-VIA-P5RP25
1 — GND_CHASSIS_LVDS
MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE
— =GND_CHASSIS_LCD1 (74)
— =GND_CHASSIS_LCD2 (74)
— =GND_CHASSIS_LCD3 (74)
— =GND_CHASSIS_LCD4 (74)

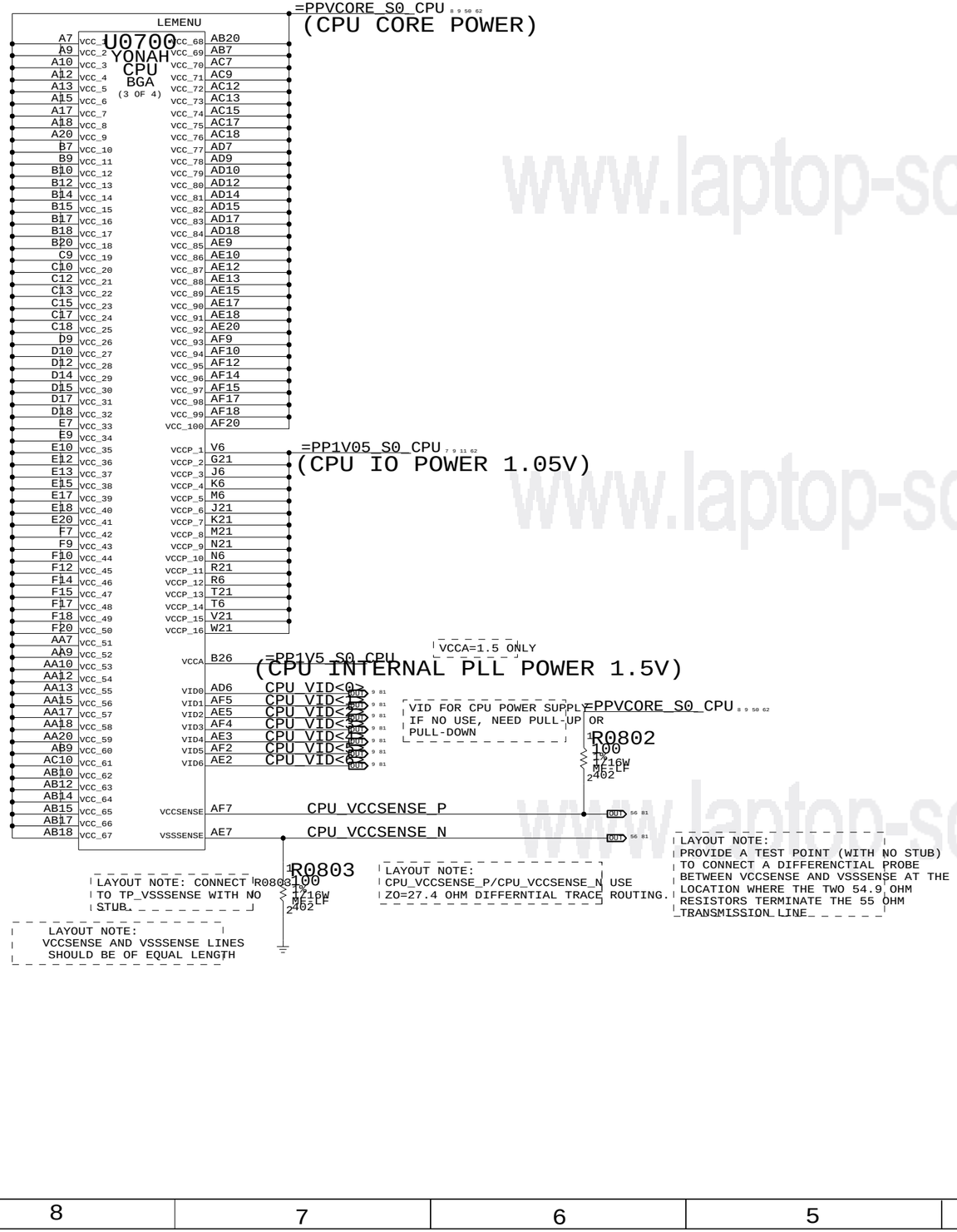
SH0600
OG-503040
SHLD-SM-LF
1 — GND_CHASSIS_INVERTER
2 — VOLTAGE=0V
3
MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, MAKE_BASE=TRUE
— =GND_CHASSIS_INVERTER (74)

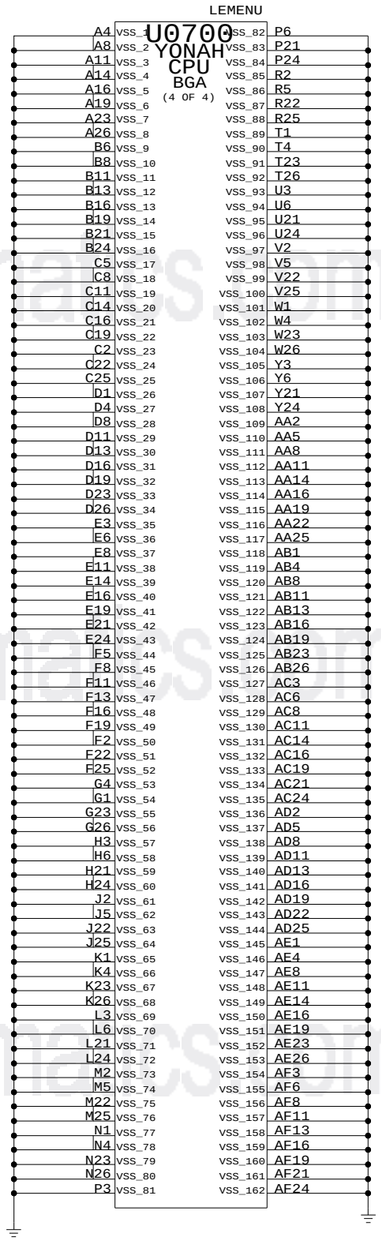
Signal Aliases

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-6941 | REV. 07001
SCALE NONE | SHT 6 OF 81







CPU 2 OF 2-PWR/GND

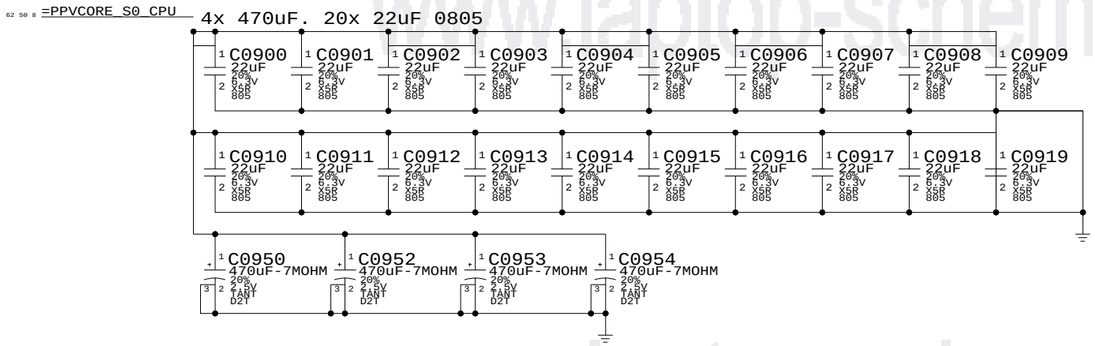
SYNC_MASTER=M42 SYNC_DATE=09/08/2005

APPLE COMPUTER INC.

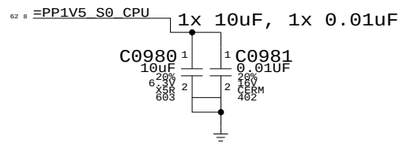
SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	8	81

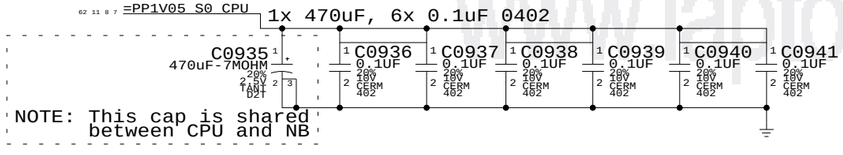
CPU VCORE HF AND BULK DECOUPLING



VCCA (CPU AVdd) Decoupling

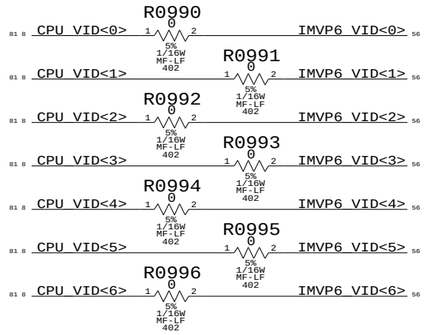


VCCP (CPU I/O) Decoupling



CPU VCORE VID Connections

Resistors to allow for override of CPU VID
Will probably be removed before production



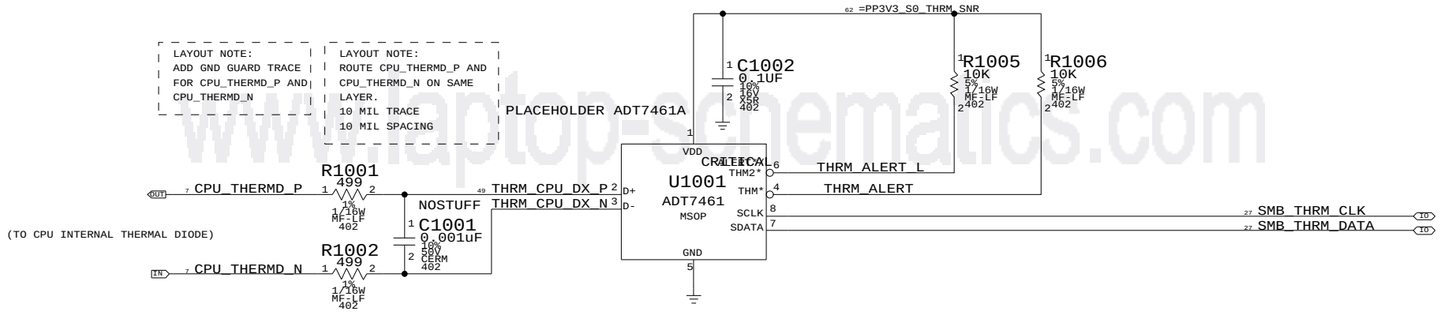
CPU Decoupling & VID

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001
SCALE: NONE	SHT 9 OF 81	

CPU ZONE THERMAL SENSOR



PLACE U1001 NEAR THE U1200

CPU MISC1-TEMP SENSOR

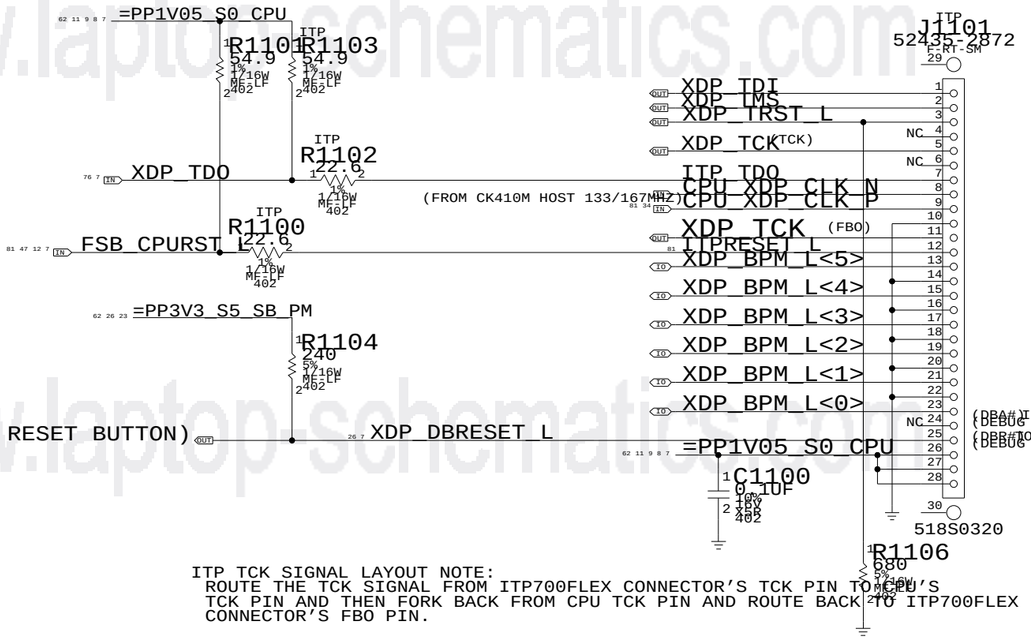
SYNC_MASTER=M42 SYNC_DATE=09/08/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	10	81

CPU ITP700FLEX DEBUG SUPPORT

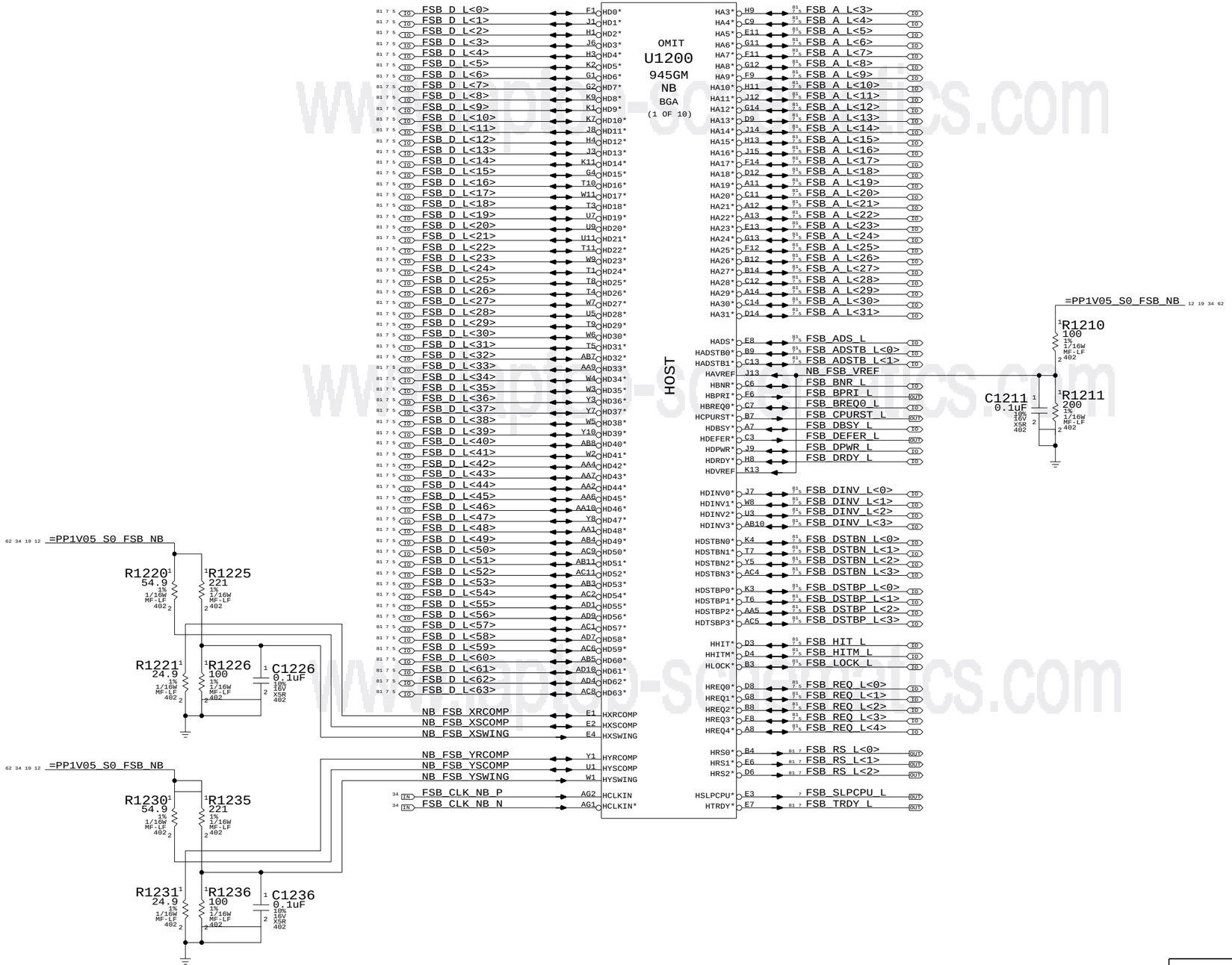


ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG

SYNC_MASTER=M52 SYNC_DATE=09/08/2005

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	07001
	SCALE	SHT OF	
	NONE	11 81	



NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	12	81

LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit
filtering components. Unused DAC outputs should
connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.

=PP1V5_S0_NB_PCIE 19 62

R1310 24.9 1% 1/16W MF-LF 2 402

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LVDS

LVDS_BKLTCTL	D32	L_BKLTCTL	
LVDS_BKLTEN	J30	L_BKLTEN	
LVDS_CLKCTLA	H30	L_CLKCTLA	
LVDS_CLKCTLB	H29	L_CLKCTLB	
LVDS_DDC_CLK	G26	L_DDC_CLK	
LVDS_DDC_DATA	G25	L_DDC_DATA	
LVDS_IBG	B38	L_IBG	
TP_LVDS_VBG	C35	L_VBG	
LVDS_VDDEN	F32	L_VDDEN	
LVDS_VREFH	C33	L_VREFH	
LVDS_VREFL	C32	L_VREFL	
LVDS_A_CLK_N	A33	LA_CLK*	
LVDS_A_CLK_P	A32	LA_CLK	
LVDS_B_CLK_N	E27	LB_CLK*	
LVDS_B_CLK_P	E26	LB_CLK	
LVDS_A_DATA_N<0>	C37	LA_DATA0*	
LVDS_A_DATA_N<1>	B35	LA_DATA1*	
LVDS_A_DATA_N<2>	A37	LA_DATA2*	
LVDS_A_DATA_P<0>	B37	LA_DATA0	
LVDS_A_DATA_P<1>	B34	LA_DATA1	
LVDS_A_DATA_P<2>	A36	LA_DATA2	
LVDS_B_DATA_N<0>	G30	LB_DATA0*	
LVDS_B_DATA_N<1>	D30	LB_DATA1*	
LVDS_B_DATA_N<2>	F29	LB_DATA2*	
LVDS_B_DATA_P<0>	F30	LB_DATA0	
LVDS_B_DATA_P<1>	D29	LB_DATA1	
LVDS_B_DATA_P<2>	F28	LB_DATA2	

TV

TV_DACA_OUT	A16	TV_DACA_OUT
TV_DACB_OUT	C18	TV_DACB_OUT
TV_DACC_OUT	A19	TV_DACC_OUT
TV_IREF	J20	TV_IREF
TV_IRTNA	B16	TV_IRTNA
TV_IRTNB	B18	TV_IRTNB
TV_IRTNC	B19	TV_IRTNC

VGA

CRT_BLUE	E23	CRT_BLUE
CRT_BLUE_L	D23	CRT_BLUE*
CRT_GREEN	C22	CRT_GREEN
CRT_GREEN_L	B22	CRT_GREEN*
CRT_RED	A21	CRT_RED
CRT_RED_L	B21	CRT_RED*
CRT_DDC_CLK	C26	CRT_DDC_CLK
CRT_DDC_DATA	C25	CRT_DDC_DATA
CRT_HSYNC_R	G23	HSYNC
CRT_IREF	J22	CRT_IREF
CRT_VSYNC_R	H23	CRT_VSYNC

PCI-EXPRESS GRAPHICS

			SDVO Alternate Function
EXP_A_COMPI	D40	PEG_COMP	
EXP_A_COMPO	D38		
EXP_A_RXN0	F34	PEG_D2R_N<0>	SDVO_TVCLKIN#
EXP_A_RXN1	G38	PEG_D2R_N<1>	SDVO_INT#
EXP_A_RXN2	H34	PEG_D2R_N<2>	SDVO_FLDSTALL#
EXP_A_RXN3	J38	PEG_D2R_N<3>	
EXP_A_RXN4	L34	PEG_D2R_N<4>	
EXP_A_RXN5	M38	PEG_D2R_N<5>	
EXP_A_RXN6	N34	PEG_D2R_N<6>	
EXP_A_RXN7	P38	PEG_D2R_N<7>	
EXP_A_RXN8	R34	PEG_D2R_N<8>	
EXP_A_RXN9	T38	PEG_D2R_N<9>	
EXP_A_RXN10	V34	PEG_D2R_N<10>	
EXP_A_RXN11	W38	PEG_D2R_N<11>	
EXP_A_RXN12	Y34	PEG_D2R_N<12>	
EXP_A_RXN13	AA38	PEG_D2R_N<13>	
EXP_A_RXN14	AB34	PEG_D2R_N<14>	
EXP_A_RXN15	AC38	PEG_D2R_N<15>	
EXP_A_RXP0	D34	PEG_D2R_P<0>	SDVO_TVCLKIN
EXP_A_RXP1	F38	PEG_D2R_P<1>	SDVO_INT
EXP_A_RXP2	G34	PEG_D2R_P<2>	SDVO_FLDSTALL
EXP_A_RXP3	H38	PEG_D2R_P<3>	
EXP_A_RXP4	J34	PEG_D2R_P<4>	
EXP_A_RXP5	L38	PEG_D2R_P<5>	
EXP_A_RXP6	M34	PEG_D2R_P<6>	
EXP_A_RXP7	N38	PEG_D2R_P<7>	
EXP_A_RXP8	P34	PEG_D2R_P<8>	
EXP_A_RXP9	R38	PEG_D2R_P<9>	
EXP_A_RXP10	T34	PEG_D2R_P<10>	
EXP_A_RXP11	V38	PEG_D2R_P<11>	
EXP_A_RXP12	W34	PEG_D2R_P<12>	
EXP_A_RXP13	Y38	PEG_D2R_P<13>	
EXP_A_RXP14	AA34	PEG_D2R_P<14>	
EXP_A_RXP15	AB38	PEG_D2R_P<15>	
EXP_A_TXN0	F36	PEG_R2D_C_N<0>	SDVOB_RED#
EXP_A_TXN1	G40	PEG_R2D_C_N<1>	SDVOB_GREEN#
EXP_A_TXN2	H36	PEG_R2D_C_N<2>	SDVOB_BLUE#
EXP_A_TXN3	J40	PEG_R2D_C_N<3>	SDVOB_CLKN
EXP_A_TXN4	L36	PEG_R2D_C_N<4>	SDVOC_RED#
EXP_A_TXN5	M40	PEG_R2D_C_N<5>	SDVOC_GREEN#
EXP_A_TXN6	N36	PEG_R2D_C_N<6>	SDVOC_BLUE#
EXP_A_TXN7	P40	PEG_R2D_C_N<7>	SDVOC_CLKN
EXP_A_TXN8	R36	PEG_R2D_C_N<8>	
EXP_A_TXN9	T40	PEG_R2D_C_N<9>	
EXP_A_TXN10	V36	PEG_R2D_C_N<10>	
EXP_A_TXN11	W40	PEG_R2D_C_N<11>	
EXP_A_TXN12	Y36	PEG_R2D_C_N<12>	
EXP_A_TXN13	AA40	PEG_R2D_C_N<13>	
EXP_A_TXN14	AB36	PEG_R2D_C_N<14>	
EXP_A_TXN15	AC40	PEG_R2D_C_N<15>	
EXP_A_TXP0	D36	PEG_R2D_C_P<0>	SDVOB_RED
EXP_A_TXP1	F40	PEG_R2D_C_P<1>	SDVOB_GREEN
EXP_A_TXP2	G36	PEG_R2D_C_P<2>	SDVOB_BLUE
EXP_A_TXP3	H40	PEG_R2D_C_P<3>	SDVOB_CLKP
EXP_A_TXP4	J36	PEG_R2D_C_P<4>	SDVOC_RED
EXP_A_TXP5	L40	PEG_R2D_C_P<5>	SDVOC_GREEN
EXP_A_TXP6	M36	PEG_R2D_C_P<6>	SDVOC_BLUE
EXP_A_TXP7	N40	PEG_R2D_C_P<7>	SDVOC_CLKP
EXP_A_TXP8	P36	PEG_R2D_C_P<8>	
EXP_A_TXP9	R40	PEG_R2D_C_P<9>	
EXP_A_TXP10	T36	PEG_R2D_C_P<10>	
EXP_A_TXP11	V40	PEG_R2D_C_P<11>	
EXP_A_TXP12	W36	PEG_R2D_C_P<12>	
EXP_A_TXP13	Y40	PEG_R2D_C_P<13>	
EXP_A_TXP14	AA36	PEG_R2D_C_P<14>	
EXP_A_TXP15	AB40	PEG_R2D_C_P<15>	

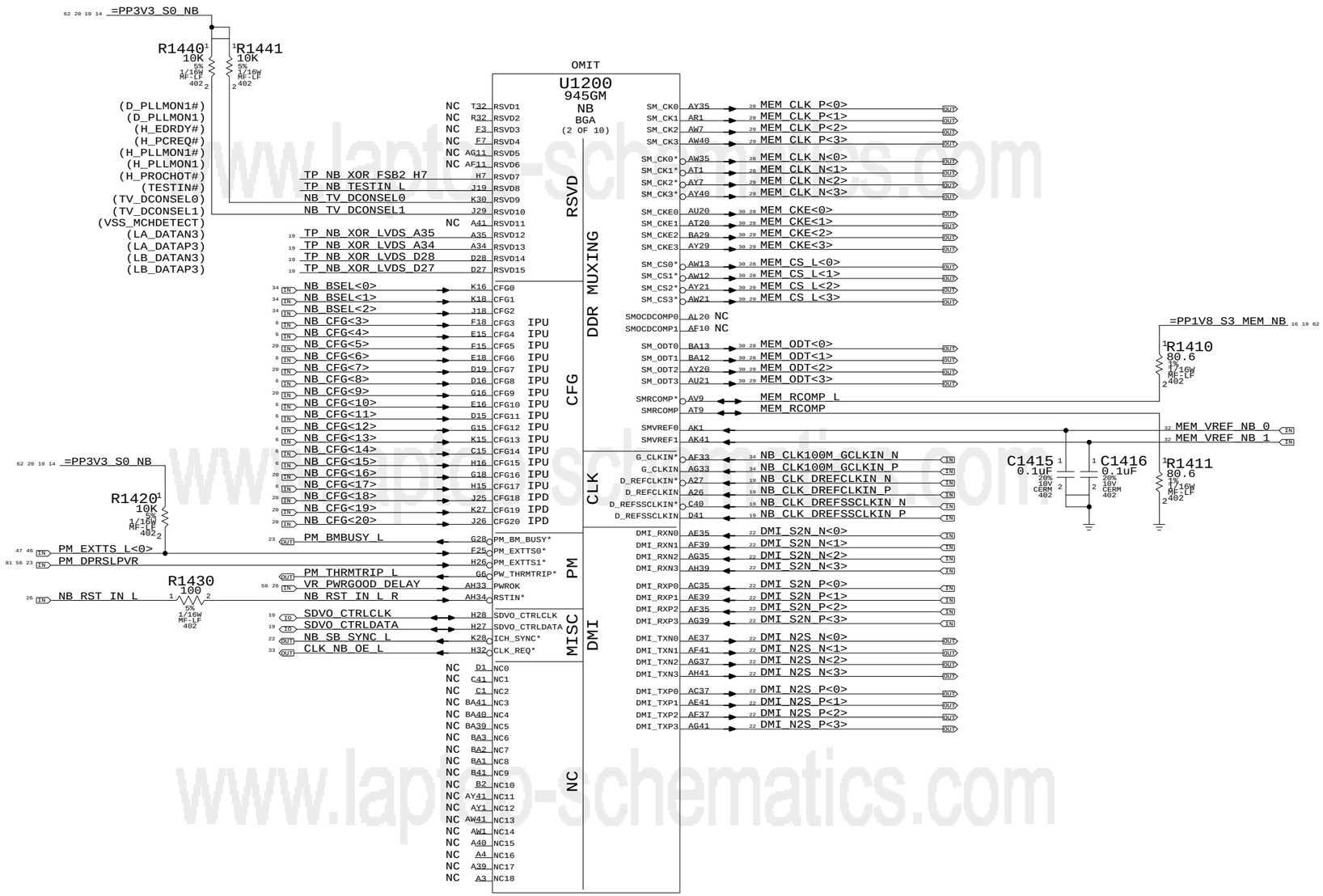
NB PEG / Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE: NONE SHT 13 OF 81

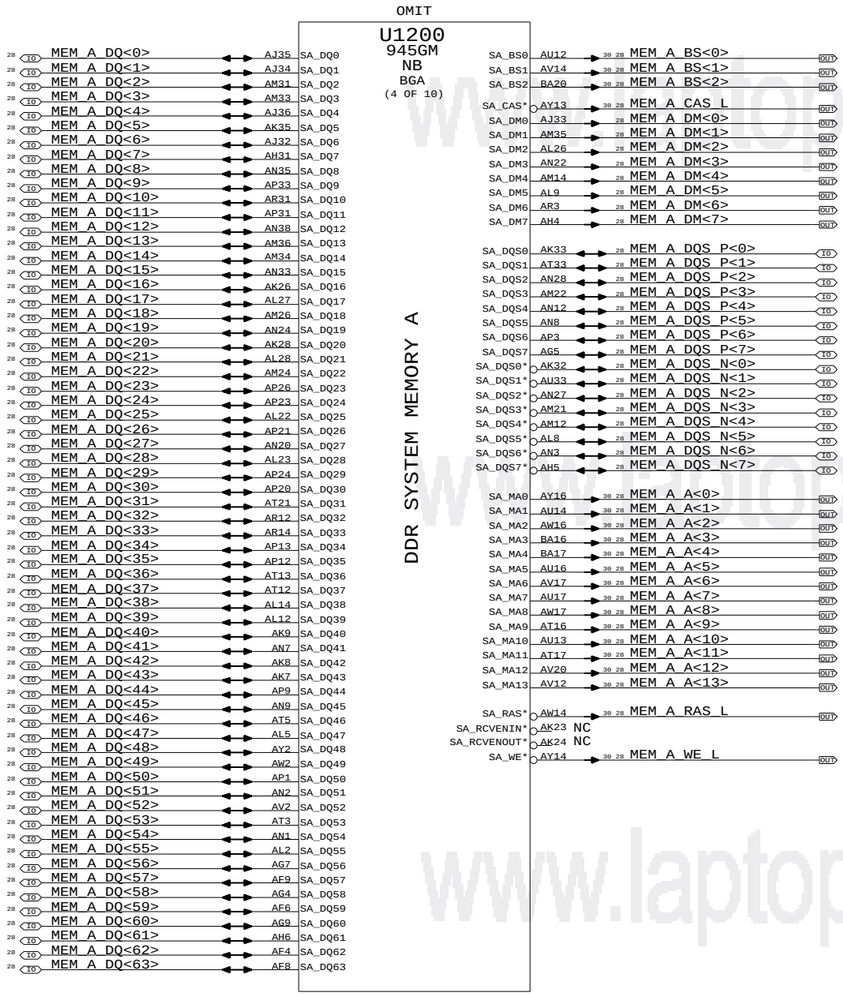


NB Misc Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001
SCALE: NONE	SHT 14 OF 81	



NB DDR2 Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.

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D	051-6941	07001

SCALE	SHT	OF
NONE	15	81

=PPVCORE_S0_NB 16 19 62

1.05V or 1.5V

1.05V, Internal Graphics: 3500mA Max
1.05V, External Graphics: 1500mA Max
1.5V, Internal Graphics: 5500mA Max

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NB
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OMIT

VCC

1.8V Max Current

Speed	1 Channel	2 Channel
400MTs	1300mA	2400mA
533MTs	1500mA	2800mA
667MTs	1700mA	3200mA

NB_VCCSM_LF4
NB_VCCSM_LF5

C1614 0.47uF 20% 6.3V CERM-X5R 402
C1613 0.47uF 20% 6.3V CERM-X5R 402

C1615 0.47uF 20% 6.3V CERM-X5R 402
62 19 14 =PP1V8_S3_MEM_NB
Layout Note: Place near pin BA23

C1620 10uF 20% 6.3V X5R 603
C1621 10uF 20% 6.3V X5R 603
Layout Note: Place in cavity

C1610 0.47uF 20% 6.3V CERM-X5R 402
Layout Note: Place near pin BA15

C1612 0.47uF 20% 6.3V CERM-X5R 402
C1611 0.47uF 20% 6.3V CERM-X5R 402

NB_VCCSM_LF2
NB_VCCSM_LF1

NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

62 19 16 =PPVCORE_S0_NB

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NCTF

=PP1V5_S0_NB_VCCAUX 17 19 62

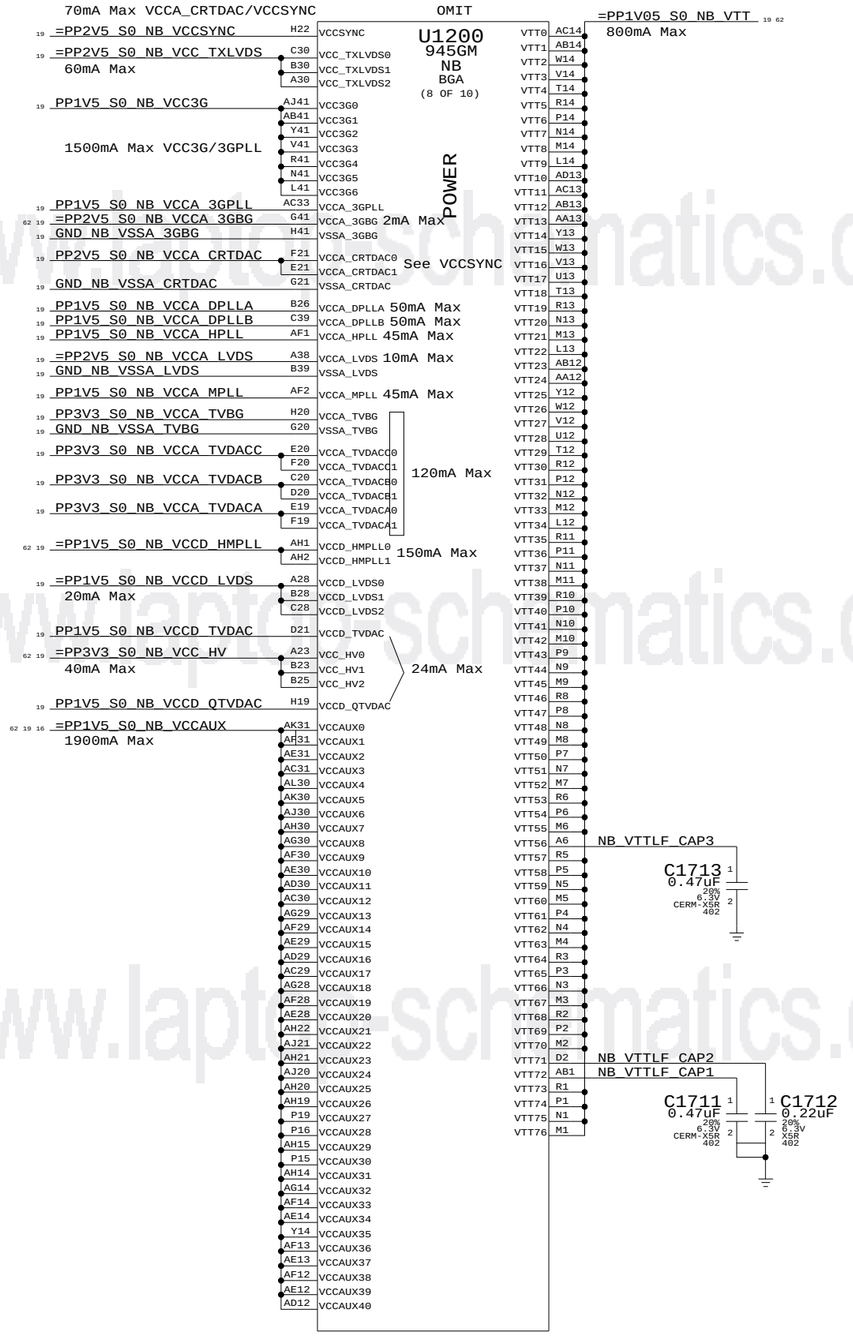
NB Power 1

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	16	81



NB Power 2

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	17	81

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VSS

AC41	VSS_0	VSS_97	AK34
A41	VSS_1	VSS_98	AG34
W41	VSS_2	VSS_99	AF34
T41	VSS_3	VSS_100	AE34
P41	VSS_4	VSS_101	AC34
M41	VSS_5	VSS_102	C34
J41	VSS_6	VSS_103	AW33
F41	VSS_7	VSS_104	AV33
AV40	VSS_8	VSS_105	AR33
AP40	VSS_9	VSS_106	AE33
AN40	VSS_10	VSS_107	AB33
AK40	VSS_11	VSS_108	Y33
AJ40	VSS_12	VSS_109	V33
AH40	VSS_13	VSS_110	T33
AG40	VSS_14	VSS_111	R33
AF40	VSS_15	VSS_112	M33
AE40	VSS_16	VSS_113	H33
B40	VSS_17	VSS_114	G33
AY39	VSS_18	VSS_115	F33
AW39	VSS_19	VSS_116	D33
AV39	VSS_20	VSS_117	B33
AR39	VSS_21	VSS_118	AH32
AN39	VSS_22	VSS_119	AG32
AJ39	VSS_23	VSS_120	AF32
AC39	VSS_24	VSS_121	AE32
AB39	VSS_25	VSS_122	AC32
AA39	VSS_26	VSS_123	AB32
Y39	VSS_27	VSS_124	G32
W39	VSS_28	VSS_125	B32
V39	VSS_29	VSS_126	AY31
T39	VSS_30	VSS_127	AV31
R39	VSS_31	VSS_128	AN31
P39	VSS_32	VSS_129	AJ31
N39	VSS_33	VSS_130	AG31
M39	VSS_34	VSS_131	AB31
L39	VSS_35	VSS_132	Y31
J39	VSS_36	VSS_133	AB30
H39	VSS_37	VSS_134	E30
G39	VSS_38	VSS_135	AT29
F39	VSS_39	VSS_136	AN29
D39	VSS_40	VSS_137	AB29
AT38	VSS_41	VSS_138	T29
AM38	VSS_42	VSS_139	N29
AH38	VSS_43	VSS_140	K29
AG38	VSS_44	VSS_141	G29
AF38	VSS_45	VSS_142	E29
AE38	VSS_46	VSS_143	C29
C38	VSS_47	VSS_144	B29
AK37	VSS_48	VSS_145	A29
AH37	VSS_49	VSS_146	BA28
AB37	VSS_50	VSS_147	AW28
AA37	VSS_51	VSS_148	AU28
Y37	VSS_52	VSS_149	AP28
W37	VSS_53	VSS_150	AM28
V37	VSS_54	VSS_151	AD28
T37	VSS_55	VSS_152	AC28
R37	VSS_56	VSS_153	W28
P37	VSS_57	VSS_154	J28
N37	VSS_58	VSS_155	E28
M37	VSS_59	VSS_156	AP27
L37	VSS_60	VSS_157	AM27
J37	VSS_61	VSS_158	AK27
H37	VSS_62	VSS_159	J27
G37	VSS_63	VSS_160	G27
F37	VSS_64	VSS_161	F27
D37	VSS_65	VSS_162	C27
AY36	VSS_66	VSS_163	B27
AW36	VSS_67	VSS_164	AN26
AN36	VSS_68	VSS_165	M26
AH36	VSS_69	VSS_166	K26
AG36	VSS_70	VSS_167	F26
AF36	VSS_71	VSS_168	D26
AE36	VSS_72	VSS_169	AK25
AC36	VSS_73	VSS_170	P25
C36	VSS_74	VSS_171	K25
B36	VSS_75	VSS_172	H25
BA35	VSS_76	VSS_173	E25
AV35	VSS_77	VSS_174	D25
AR35	VSS_78	VSS_175	A25
AH35	VSS_79	VSS_176	BA24
AB35	VSS_80	VSS_177	AU24
AA35	VSS_81	VSS_178	AL24
Y35	VSS_82	VSS_179	AW23
W35	VSS_83		
V35	VSS_84		
T35	VSS_85		
R35	VSS_86		
P35	VSS_87		
N35	VSS_88		
M35	VSS_89		
L35	VSS_90		
J35	VSS_91		
H35	VSS_92		
G35	VSS_93		
F35	VSS_94		
D35	VSS_95		
AN34	VSS_96		

OMIT

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945GM
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VSS

AT23	VSS_180	VSS_273	J11
AN23	VSS_181	VSS_274	D11
AM23	VSS_182	VSS_275	B11
AH23	VSS_183	VSS_276	AV10
AC23	VSS_184	VSS_277	AP10
W23	VSS_185	VSS_278	AL10
K23	VSS_186	VSS_279	AJ10
J23	VSS_187	VSS_280	AG10
F23	VSS_188	VSS_281	AC10
C23	VSS_189	VSS_282	W10
AA22	VSS_190	VSS_283	U10
K22	VSS_191	VSS_284	BA9
G22	VSS_192	VSS_285	AW9
F22	VSS_193	VSS_286	AR9
E22	VSS_194	VSS_287	AH9
D22	VSS_195	VSS_288	AB9
A22	VSS_196	VSS_289	Y9
BA21	VSS_197	VSS_290	R9
AV21	VSS_198	VSS_291	G9
AR21	VSS_199	VSS_292	E9
AN21	VSS_200	VSS_293	A9
AL21	VSS_201	VSS_294	AG8
AB21	VSS_202	VSS_295	AD8
Y21	VSS_203	VSS_296	AA8
P21	VSS_204	VSS_297	U8
K21	VSS_205	VSS_298	K8
J21	VSS_206	VSS_299	C8
H21	VSS_207	VSS_300	BA7
C21	VSS_208	VSS_301	AV7
AW20	VSS_209	VSS_302	AP7
AR20	VSS_210	VSS_303	AL7
AM20	VSS_211	VSS_304	AJ7
AA20	VSS_212	VSS_305	AH7
K20	VSS_213	VSS_306	AF7
B20	VSS_214	VSS_307	AC7
A20	VSS_215	VSS_308	R7
AN19	VSS_216	VSS_309	G7
AC19	VSS_217	VSS_310	D7
W19	VSS_218	VSS_311	AG6
K19	VSS_219	VSS_312	AD6
G19	VSS_220	VSS_313	AB6
C19	VSS_221	VSS_314	Y6
AH18	VSS_222	VSS_315	U6
P18	VSS_223	VSS_316	N6
H18	VSS_224	VSS_317	K6
D18	VSS_225	VSS_318	H6
A18	VSS_226	VSS_319	B6
AY17	VSS_227	VSS_320	AV5
AR17	VSS_228	VSS_321	AF5
AP17	VSS_229	VSS_322	AD5
AM17	VSS_230	VSS_323	AY4
AK17	VSS_231	VSS_324	AR4
AV16	VSS_232	VSS_325	AP4
AN16	VSS_233	VSS_326	AL4
AL16	VSS_234	VSS_327	AJ4
J16	VSS_235	VSS_328	Y4
F16	VSS_236	VSS_329	U4
C16	VSS_237	VSS_330	R4
AN15	VSS_238	VSS_331	J4
AM15	VSS_239	VSS_332	F4
AK15	VSS_240	VSS_333	C4
N15	VSS_241	VSS_334	AY3
M15	VSS_242	VSS_335	AW3
L15	VSS_243	VSS_336	AV3
B15	VSS_244	VSS_337	AL3
A15	VSS_245	VSS_338	AH3
BA14	VSS_246	VSS_339	AG3
AT14	VSS_247	VSS_340	AF3
AK14	VSS_248	VSS_341	AD3
AD14	VSS_249	VSS_342	AC3
AA14	VSS_250	VSS_343	AA3
U14	VSS_251	VSS_344	G3
K14	VSS_252	VSS_345	AT2
H14	VSS_253	VSS_346	AR2
E14	VSS_254	VSS_347	AP2
AV13	VSS_255	VSS_348	AK2
AR13	VSS_256	VSS_349	AJ2
AN13	VSS_257	VSS_350	AD2
AM13	VSS_258	VSS_351	AB2
AL13	VSS_259	VSS_352	Y2
AG13	VSS_260	VSS_353	U2
P13	VSS_261	VSS_354	T2
F13	VSS_262	VSS_355	N2
D13	VSS_263	VSS_356	J2
B13	VSS_264	VSS_357	H2
AY12	VSS_265	VSS_358	F2
AC12	VSS_266	VSS_359	C2
K12	VSS_267	VSS_360	AL1
H12	VSS_268		
E12	VSS_269		
AD11	VSS_270		
AA11	VSS_271		
Y11	VSS_272		

NB Grounds

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

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SCALE	SHT	OF
NONE	18	81

Power Interface

These are the power signals that leave the NB "block"

Rail Totals:

2310mA Max?	=PPVCORE_S0_NB	1500mA Max
	=PP1V05_S0_FSB_NB	10mA Max?
	=PP1V05_S0_NB_VTT	800mA Max
	=PP1V05_S0_NB_CRT	?mA Max
3674mA Max	=PP1V5_S0_NB	?mA Max
	=PP1V5_S0_NB_3G	1500mA Max
	=PP1V5_S0_NB_3GPLL	
	=PP1V5_S0_NB_PCIE	?mA Max
	=PP1V5_S0_NB_PLL	100mA Max
	=PP1V5_S0_NB_TVDAC	24mA Max
	=PP1V5_S0_NB_VCCD_HMPLL	150mA Max
	=PP1V5_S0_NB_VCCAUX	1900mA Max
3200mA Max	=PP1V8_S3_MEM_NB	3200mA Max
	=PP2V5_S0_NB_VCCSYNC	70mA Max
132mA Max	=PP2V5_S0_NB_VCC_TXLVDS	60mA Max
	=PP2V5_S0_NB_VCCA_3GBG	2mA Max
	=PP3V3_S0_NB	?mA Max
40mA Max?	=PP3V3_S0_NB_VCC_HV	40mA Max

=PP1V05_S0_NB_CRT
- CRT_RED
- CRT_GREEN
- CRT_BLUE
- CRT_RED_L
- CRT_GREEN_L
- CRT_BLUE_L
- CRT_IREF
- CRT_HSYNC_R
- CRT_VSYNC_R

TP_CRT_DDC_CLK (MAKE_BASE=TRUE) — CRT_DDC_CLK
TP_CRT_DDC_DATA (MAKE_BASE=TRUE) — CRT_DDC_DATA

=PP1V5_S0_NB_TVDAC
- TV_DACA_OUT
- TV_DACB_OUT
- TV_DACC_OUT
- TV_IREF
- TV_IRTNA
- TV_IRTNB
- TV_IRTNC

TP_LVDS_BKLTCTL (MAKE_BASE=TRUE) — LVDS_BKLTCTL
TP_LVDS_BKLTEN (MAKE_BASE=TRUE) — LVDS_BKLTEN
TP_LVDS_CLKCTLA (MAKE_BASE=TRUE) — LVDS_CLKCTLA
TP_LVDS_CLKCTLB (MAKE_BASE=TRUE) — LVDS_CLKCTLB
TP_LVDS_DDC_CLK (MAKE_BASE=TRUE) — LVDS_DDC_CLK
TP_LVDS_DDC_DATA (MAKE_BASE=TRUE) — LVDS_DDC_DATA
NC_LVDS_IBG (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_IBG
TP_LVDS_VDDEN (MAKE_BASE=TRUE) — LVDS_VDDEN
NC_LVDS_VREFH (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_VREFH
TP_LVDS_VREFL (MAKE_BASE=TRUE) — LVDS_VREFL
NC_LVDS_A_CLKP (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_CLK_P
NC_LVDS_A_CLKN (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_CLK_N
NC_LVDS_A_DATAP<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_DATA_P<2..0>
NC_LVDS_A_DATAN<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_DATA_N<2..0>
NC_LVDS_B_CLKP (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_CLK_P
NC_LVDS_B_CLKN (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_CLK_N
NC_LVDS_B_DATAP<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_DATA_P<2..0>
NC_LVDS_B_DATAN<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_DATA_N<2..0>
NC_NB_XOR_LVDS_A34 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_A34
NC_NB_XOR_LVDS_A35 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_A35
NC_NB_XOR_LVDS_D27 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_D27
NC_NB_XOR_LVDS_D28 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_D28
TP_SDVO_CTRLCLK (MAKE_BASE=TRUE) — SDVO_CTRLCLK
TP_SDVO_CTRLDATA (MAKE_BASE=TRUE) — SDVO_CTRLDATA

(MCH LVDS DATA/CLK TX 2.5V PWR) =PP2V5_S0_NB_VCC_TXLVDS
(MCH LVDS DIGITAL 1.5V PWR) =PP1V5_S0_NB_VCCD_LVDS
(MCH LVDS ANALOG 2.5V PWR) =PP2V5_S0_NB_VCCA_LVDS
NC_GND_NB_VSSA_LVDS (MAKE_BASE=TRUE NO_TEST=TRUE) — GND_NB_VSSA_LVDS

=PPVCORE_S0_NB
- (MCH CRTDAC ANALOG 2.5V PWR) PP2V5_S0_NB_VCCA_CRTDAC
- GND_NB_VSSA_CRTDAC

(MCH H/V SYNC 2.5V PWR) =PP2V5_S0_NB_VCCSYNC

=PP1V5_S0_NB_TVDAC
- (MCH TV OUT CHANNEL A 3.3V PWR) PP3V3_S0_NB_VCCA_TVDACA
- (MCH TV OUT CHANNEL B 3.3V PWR) PP3V3_S0_NB_VCCA_TVDACB
- (MCH TV OUT CHANNEL C 3.3V PWR) PP3V3_S0_NB_VCCA_TVDACC
- (MCH TV DAC BAND GAP 3.3V PWR) PP3V3_S0_NB_VCCA_TVBG
- GND_NB_VSSA_TVBG

(MCH DISPLAY A PLL 1.5V PWR) TP_NB_VCCA_DPLLA (MAKE_BASE=TRUE) — PP1V5_S0_NB_VCCA_DPLLA
(MCH DISPLAY B PLL 1.5V PWR) TP_NB_VCCA_DPLLB (MAKE_BASE=TRUE) — PP1V5_S0_NB_VCCA_DPLLB

- NB_CLK_DREFCLKIN_P
- NB_CLK_DREFCLKIN_N
- NB_CLK_DREFSSCLKIN_P
- NB_CLK_DREFSSCLKIN_N

=PPVCORE_S0_NB 1500mA Max — GMCH CORE PWR 1.05V BYPASS
C1900 470uF-7MOHM 20% 2.5V TANT D2T
C1902 10uF 20% 6.3V X5R 603
C1903 10uF 20% 6.3V X5R 603
C1904 1uF 10% 6.3V CERM 402
C1905 0.22uF 10% 6.3V X5R 402
C1906 0.22uF 10% 6.3V X5R 402
C1907 0.22uF 10% 6.3V X5R 402

=PP1V05_S0_NB_VTT 800mA Max — MCH VTT BYPASS (MCH FSB 1.05V PWR) (SHARE C0940 470UF)
C1965 4.7uF 20% 6.3V CERM 603
C1966 2.2uF 20% 6.3V CERM1 603
Layout Note: Place in cavity
C1967 0.22uF 20% 6.3V X5R 402
Layout Note: Place on the edge

=PP3V3_S0_NB_VCC_HV 40mA Max — MCH VCC_HV BYPASS (MCH HV BUFFER 3.3V PWR)
C1914 10uF 20% 6.3V X5R 603
C1915 0.1uF 20% 10V CERM 402

=PP2V5_S0_NB_VCCA_3GBG 2mA Max — MCH VCCA_3GBG BYPASS (MCH PCIE/DMI BAND GAP 2.5V PWR)
C1916 0.1uF 20% 10V CERM 402

=PP1V5_S0_NB_VCCAUX 1900mA Max — GMCH VCCAUX FILTER (MCH DDR DLL&IO, FSB HSIO&IO PWR 1.5V)
C1918 0.1uF 20% 10V CERM 402

=PP1V5_S0_NB_TVDAC 24mA Max
C1921 22000pF-1000mA 10V NPM18 — GMCH VCCD_TVDAC FILTER (MCH TVDAC DEDICATED PWR 1.5V) PP1V5_S0_NB_VCCD_TVDAC (MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V) 24mA Max TVDAC/QTVDAC
C1920 0.1uF 20% 10V CERM 402
Layout Note: These 4 caps should be within 6.35 mm of NB edge
L1922 180-OHM-1.5A 0603 — PP1V5_S0_NB_QTVDAC (MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V)
C1923 22000pF-1000mA 10V NPM18 — GMCH VCCD_QTVDAC FILTER (MCH TVDAC DIGITAL QUIET 1.5V PWR) PP1V5_S0_NB_VCCD_QTVDAC (MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V)
C1922 0.1uF 20% 10V CERM 402

=PP1V5_S0_NB_3G 1500mA Max — L1970 91nH 1210 — GMCH VCC3G FILTER (PCI-E/DMI ANALOG 1.5V PWR) PP1V5_S0_NB_VCC3G (MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V) 1500mA Max
Layout Note: Place L and C close to MCH
C1970 220UF 20% 2.5V POLY SMB2
C1971 10uF 20% 6.3V X5R 603
C1972 10uF 20% 6.3V X5R 603
Layout Note: 10uF caps should be close to MCH on opposite side.

=PP1V5_S0_NB_3GPLL 1.0UH-220MA-0.12-OHM 0805 — PP1V5_S0_NB_3GPLL_F (MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.4 mm VOLTAGE=1.5V)
R1975 0.51 1% 1/10W MF-LF 402 — GMCH VCCA_3GPLL FILTER (3GIO PLL 1.5V PWR) PP1V5_S0_NB_VCCA_3GPLL (MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V)
C1975 10uF 20% 6.3V X5R 603
C1976 0.1uF 20% 10V CERM 402
GND_NB_VSSA_3GBG
Layout Note: 3GPLL 10uF cap should be placed in cavity
Layout Note: Route to caps, then GND

=PP1V5_S0_NB_PLL 100mA Max
L1934 FERR-120-OHM-0.2A 0603 — GMCH VCCA_HPLL FILTER (HOST PLL 1.5V PWR) PP1V5_S0_NB_VCCA_HPLL (MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V) 45mA Max
C1934 22uF 20% 6.3V X5R 805
C1935 0.1uF 20% 10V CERM 402
L1936 FERR-120-OHM-0.2A 0603 — GMCH VCCA_MPLL FILTER (MCH MEMORY PLL 1.5V PWR) PP1V5_S0_NB_VCCA_MPLL (MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V) 45mA Max
C1936 22uF 20% 6.3V X5R 805
C1937 0.1uF 20% 10V CERM 402

NB (GM) Decoupling

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

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D	051-6941	07001

SCALE: NONE — SHT 19 OF 81

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
1 R2075 2.2K 5% 1/16W MF-LF 402 2

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
1 R2077 2.2K 5% 1/16W MF-LF 402 2

NB_CFG<8>	RESERVED

14 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
1 R2079 2.2K 5% 1/16W MF-LF 402 2

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
1 R2085 2.2K 5% 1/16W MF-LF 402 2

NB_CFG<17>	RESERVED

=PP3V3_S0_NB 14 19 20 62
NBCFG_VCC_1V5
1 R2058 2.2K 5% 1/16W MF-LF 402 2

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14 NB_CFG<18>
Internal pull-down

=PP3V3_S0_NB 14 19 20 62
NBCFG_DMI_REVERSE
1 R2059 2.2K 5% 1/16W MF-LF 402 2

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

=PP3V3_S0_NB 14 19 20 62
NBCFG_SDVO_AND_PCIE
1 R2060 2.2K 5% 1/16W MF-LF 402 2

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14 NB_CFG<20>
Internal pull-down

PROBABLY NOT NEEDED

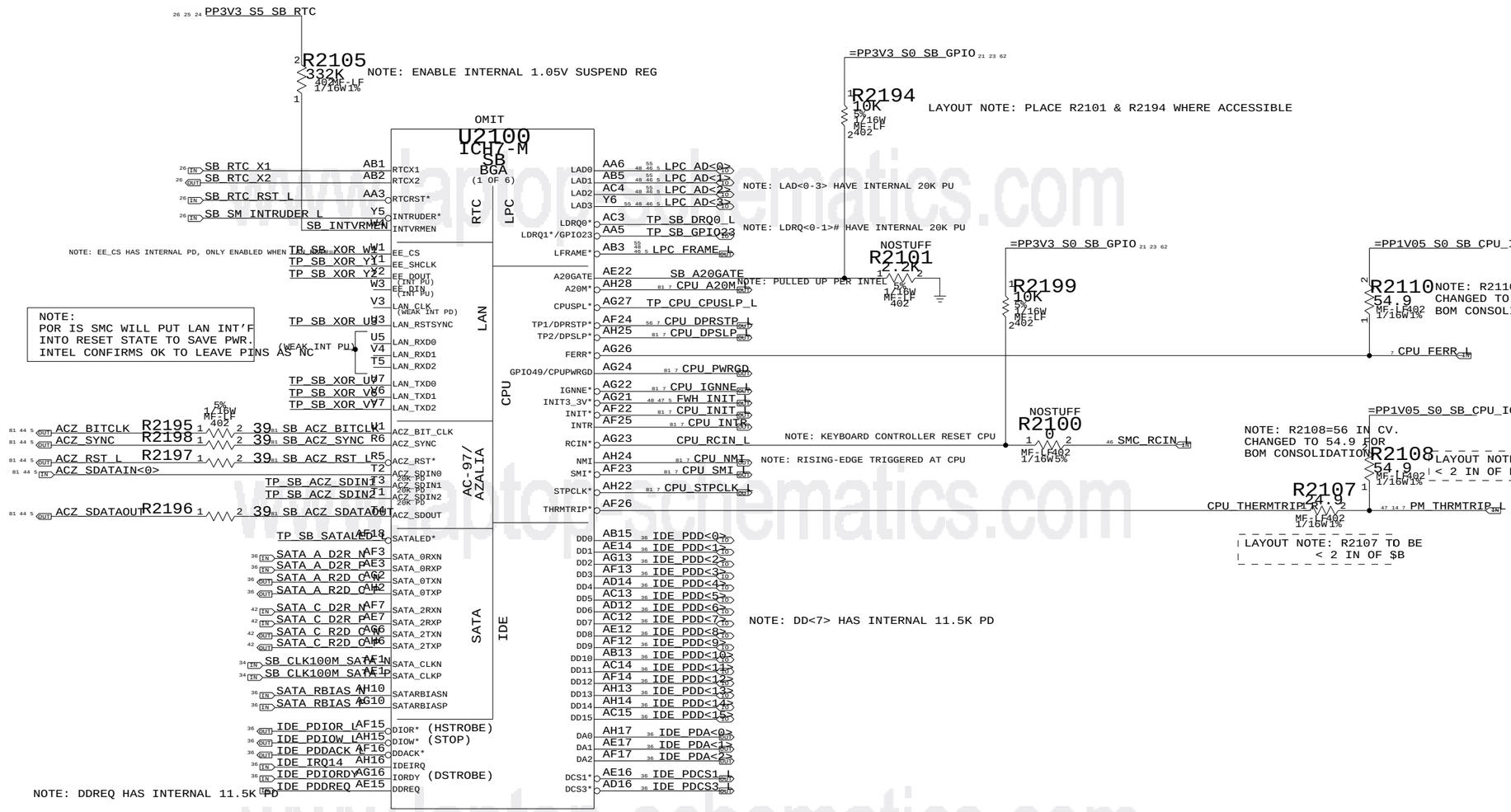
NB Config Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	20	81



	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

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SCALE: NONE	SHT: 21 OF: 81	

=PP3V3_S5_SB_USB

R2225 10K 5% 1/16W MF-LF 402
R2200 10K 5% 1/16W MF-LF 402
R2250 10K 5% 1/16W MF-LF 402
R2255 10K 5% 1/16W MF-LF 402
R2251 10K 5% 1/16W MF-LF 402
R2224 10K 5% 1/16W MF-LF 402
R2223 10K 5% 1/16W MF-LF 402
R2226 10K 5% 1/16W MF-LF 402

USB_C_OC_PU
USB_D_OC_PU
USB_E_OC_PU

USB_A_OC_L
USB_B_OC_L
USB_C_OC_L
USB_D_OC_L
USB_E_OC_L

SB_GPIO29
SB_GPIO30
SB_GPIO31

=PP3V3_S5_SB_IO

R2205 10K 5% 1/16W MF-LF 402
R2206 NOSTUFF 10K 5% 1/16W MF-LF 402
R2207 10K 5% 1/16W MF-LF 402

SPI_SCLK
SPI_CE_L
SPI_ARB
SPI_SI
SPI_SO

OMIT
U2100
ICH7-M SB BGA
(3 OF 6)

PCI-EXP
DMI
SPI
USB

PCIE_A_D2R_N F26
PCIE_A_D2R_P F25
PCIE_A_R2D_C_N G28
PCIE_A_R2D_C_P G27
PCIE_B_D2R_N H26
PCIE_B_D2R_P H25
PCIE_B_R2D_C_N G28
PCIE_B_R2D_C_P G27
PCIE_C_D2R_N K26
PCIE_C_D2R_P K25
PCIE_C_R2D_C_N J28
PCIE_C_R2D_C_P J27
PCIE_D_D2R_N M26
PCIE_D_D2R_P M25
PCIE_D_R2D_C_N L28
PCIE_D_R2D_C_P L27
PCIE_E_D2R_N P26
PCIE_E_D2R_P P25
PCIE_E_R2D_C_N N28
PCIE_E_R2D_C_P N27
PCIE_F_D2R_N T25
PCIE_F_D2R_P T24
PCIE_F_R2D_C_N R28
PCIE_F_R2D_C_P R27

SPI_CLK (INT PD) R2
SPI_CS* P6
SPI_ARB (INT PU) P1
SPI_MOSI P5
SPI_MISO P2

USB_A_OC_L D3
USB_B_OC_L C4
USB_C_OC_L D5
USB_D_OC_L D4
USB_E_OC_L E5
SB_GPIO29 C3
SB_GPIO30 A2
SB_GPIO31 B3

OC0*
OC1*
OC2*
OC3*
OC4*
OC5*/GPIO29
OC6*/GPIO30
OC7*/GPIO31

DMI0RXN V26 DMI_N2S_N<0>
DMI0RXP V25 DMI_N2S_P<0>
DMI0TXN U28 DMI_S2N_N<0>
DMI0TXP U27 DMI_S2N_P<0>
DMI1RXN Y26 DMI_N2S_N<1>
DMI1RXP Y25 DMI_N2S_P<1>
DMI1TXN W28 DMI_S2N_N<1>
DMI1TXP W27 DMI_S2N_P<1>
DMI2RXN AB26 DMI_N2S_N<2>
DMI2RXP AB25 DMI_N2S_P<2>
DMI2TXN AA28 DMI_S2N_N<2>
DMI2TXP AA27 DMI_S2N_P<2>
DMI3RXN AD25 DMI_N2S_N<3>
DMI3RXP AD24 DMI_N2S_P<3>
DMI3TXN AC28 DMI_S2N_N<3>
DMI3TXP AC27 DMI_S2N_P<3>
DMI_CLKN AE28 SB_CLK100M_DMI_N
DMI_CLKP AE27 SB_CLK100M_DMI_P

R2203 24.9 1/16W MF-LF 1% 402
DMI_ZCOMP C25
DMI_IRCOMP D25
DMI_IRCOMP_R

PP1V5_S0_SB_VCC1_5_B

LAYOUT NOTE:
PLACE R2203 < 1/2 IN FROM SB

USBP0N F1 USB_A_N
USBP0P F2 USB_A_P
USBP1N G4 USB_B_N
USBP1P G3 USB_B_P
USBP2N H1 USB_C_N
USBP2P H2 USB_C_P
USBP3N J4 USB_D_N
USBP3P J3 USB_D_P
USBP4N K1 USB_E_N
USBP4P K2 USB_E_P
USBP5N L4 USB_F_N
USBP5P L5 USB_F_P
USBP6N M1 USB_G_N
USBP6P M2 USB_G_P
USBP7N N4 USB_H_N
USBP7P N3 USB_H_P

EXTERNAL 0
AIRPORT (MINI-PCIE)
EXTERNAL 1
CAMERA
EXTERNAL 2
CF/SD
BT
IR

NOTE: USBP[0-7]P/N HAVE INTERNAL 15K PD

R2204 22.6 1/16W MF-LF 1% 402
USBRBIAS* D2
USBRBIAS D1
USB_RBIAS_PN

VOLTAGE=0V

LAYOUT NOTE:
PLACE R2204 < 1/2 IN FROM SB

NOTE: GNT0_3]# HAVE INT 20K PU ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H

=PP3V3_S0_SB

R2298 10K 5% 1/16W MF-LF 402
R2299 10K 5% 1/16W MF-LF 402

SB_CRT_TVOUT_MUX
NOTE: FWH_WP_L NOT USED
PCI_PME_FW_L
BOOT_LPC_SPI_L

R2211 1K 5% 1/16W MF-LF 402

BOM NOTE FOR PD ON PCI_GNT3_L:
NO STUFF - DEFAULT
STUFF - A16 SWAP OVERRIDE
(STRAPPED TO TOP-BLOCK SWAP MODE IF SB INVERTS A16 FOR ALL CYCLES TARGETING FWH BIOS SPACE)

OMIT
U2100
ICH7-M SB BGA
(2 OF 6)

PCI

PCI_AD<0> E18 AD0
PCI_AD<1> C18 AD1
PCI_AD<2> A16 AD2
PCI_AD<3> F18 AD3
PCI_AD<4> E16 AD4
PCI_AD<5> A18 AD5
PCI_AD<6> E17 AD6
PCI_AD<7> A17 AD7
PCI_AD<8> A15 AD8
PCI_AD<9> C14 AD9
PCI_AD<10> E14 AD10
PCI_AD<11> D14 AD11
PCI_AD<12> B12 AD12
PCI_AD<13> C13 AD13
PCI_AD<14> A13 AD14
PCI_AD<15> G13 AD15
PCI_AD<16> E12 AD16
PCI_AD<17> F11 AD17
PCI_AD<18> D11 AD18
PCI_AD<19> A11 AD19
PCI_AD<20> A10 AD20
PCI_AD<21> F11 AD21
PCI_AD<22> F10 AD22
PCI_AD<23> E9 AD23
PCI_AD<24> D9 AD24
PCI_AD<25> B9 AD25
PCI_AD<26> A8 AD26
PCI_AD<27> A6 AD27
PCI_AD<28> C7 AD28
PCI_AD<29> B6 AD29
PCI_AD<30> E6 AD30
PCI_AD<31> D6 AD31
PCI_FRAME# F16 FRAME*

REQ0* D7 PCI_REQ0_L
GNT0* E7 TP_PCI_GNT0_L
REQ1* C16 PCI_REQ1_L
GNT1* D16 PCI_GNT1_L
REQ2* C17 PCI_REQ2_L
GNT2* D17 TP_PCI_GNT2_L
REQ3* E13 PCI_REQ3_L
GNT3* F13 NC
REQ4*/GPIO22 A13
GNT4*/GPIO48 A14 NC
GPIO1/REQ5* C8
GPIO17/GNT5* D8

C/BE0* B15 PCI_C_BE_L<0>
C/BE1* C12 PCI_C_BE_L<1>
C/BE2* D12 PCI_C_BE_L<2>
C/BE3* C15 PCI_C_BE_L<3>
IRDY* A7 PCI_IRDY
PAR E10 PCI_PAR
PCICLK A9 PCI_CLK_SB
DEVSEL* A12 PCI_DEVSEL_L
PERR* C9 PCI_PERR
PLOCK* E11 PCI_LOCK
SERR* B10 PCI_SERR
STOP* F15 PCI_STOP
TRDY* F14 PCI_TRDY
PLTRST* C26 PLT_RST
PCIRST* B18 PCI_RST
(INT 20K PU) B19 TP_PCI_PME_L

INT I/F

INT_PIRQA A3 PIRQA*
INT_PIRQB B4 PIRQB*
INT_PIRQC C5 PIRQC*
INT_PIRQD B5 PIRQD*

GPIO2/PIRQE* G8 SB_GPIO2
GPIO3/PIRQF* F7 SB_GPIO3
GPIO4/PIRQG* F8 SB_GPIO4
GPIO5/PIRQH* G7 SB_GPIO5

MISC

NOTE: CHANGE SYMBOL TO RSVD[1-9]

TP_SB_XOR_AE5 AE5 RSVD0
TP_SB_XOR_AD5 AD5 RSVD1
TP_SB_XOR_AG4 AG4 RSVD2
TP_SB_XOR_AH4 AH4 RSVD3
TP_SB_XOR_AD9 AD9 RSVD4

RSVD5 AE9 TP_SB_XOR_AE9
RSVD6 AG8 TP_SB_XOR_AG8
RSVD7 AH8 TP_SB_XOR_AH8
RSVD8 F21 TP_SB_RSVD8 (AKA TP3, INTERNAL 20K PU)
MCH_SYNC* AH20 NB_SB_SYNC_L

SB BOOT BIOS SELECT

STRAP	GNT5# R2211	GNT4# R2210
LPC (DEFAULT) 11	UNSTUFF	UNSTUFF
PCI 10	UNSTUFF	STUFF
SPI 01	STUFF	UNSTUFF

NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

NOTE: R2210 WAS PD ON PIN A14 = FWH_TBL_L

SB: 2 OF 4

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SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	22	81

NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING @ PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

=PP3V3_S0_SB_GPIO 21 23 62

=PP3V3_S5_SB 23 25 62

NO_REBOOT_MODE

R2318 10K 1/16W 402 2MF-LF 5%
R2395 8.2K 1/16W 402 2MF-LF 5%
R2396 10K 1/16W 402 2MF-LF 5%
R2397 8.2K 1/16W 402 2MF-LF 5%
R2327 NOSTUFF 10K 1/16W 402 2MF-LF 5%
R2326 NOSTUFF 10K 1/16W 402 2MF-LF 5%
R2323 1K 1/16W 402 2MF-LF 5%

RP2300 10K 5% 1/16W 5M-LF

=PP3V3_S5_SB 62 25 23

R2398 1K 1/16W 402 2MF-LF 5%
R2320 10K 1/16W 402 2MF-LF 5%
R2317 10K 1/16W 402 2MF-LF 5%
R2316 10K 1/16W 402 2MF-LF 5%

OMIT
U2100
ICH7-M SB
BGA
(4 OF 6)

SMB_CLK 27 IO — C22 SMBCLK
SMB_DATA 27 IO — B22 SMBDATA
SMB_LINK_ALERT_L — A16 SMLINKALERT*
SMLINK<0> — B25 SMLINK0
SMLINK<1> — A25 SMLINK1
NOT USED
PM_RI_L — A28 RI*
SB_SPKR — A19 SPKR (INT WEAK PD)
PM_SUS_STAT_L 55 48 46 5 OUT — A27 SUS_STAT*
PM_SYSRST_L 46 26 IN — A22 SYS_RST*
PM_BMBUSY_L 14 IN — AB18 GPIO0/BM_BUSY*
SMB_ALERT_L — B23 GPIO11/SMBALERT*
NOTE: RESERVED FOR FUTURE
PM_STPPCI_L 33 OUT — AC20 GPIO18/STPPCI*
PM_STPCPU_L 33 OUT — AF21 GPIO20/STPCPU*
SB_GPIO26 — A21 GPIO26
BIOS_REC 23 — B21 GPIO27
FWH_MFG_MODE 23 — E23 GPIO28
PM_CLKRUN_L 55 48 46 39 5 IO — AG18 GPIO32/CLKRUN*
RESERVED FOR MOBILE AZALIA DOCKING INTF
TP_AZ_DOCK_EN — AG19 GPIO33/AZ_DOCK_EN*
TP_AZ_DOCK_RST — U2 GPIO34/AZ_DOCK_RST*
PCIE_WAKE_L 44 37 5 IN — F20 WAKE*
INT_SERIRQ 55 48 46 5 IO — AH21 SERIRQ
PM_THRM_L 46 IN — AF20 THRM*
VR_PWRGD_CK410 26 IN — AD22 VRMPWRGD
TP_SB_GPIO6 IO — AG21 GPIO6
SB_RUNTIME_SCI_L — AC18 GPIO7
E21 GPIO8

SMB
CLKS
SYS GPIO
PWR MNGT
GPIO

SATA GPIO
GPIO21/SATA0GP — AF19 SB_GPIO21 100 1 2 R2302
GPIO19/SATA1GP — AH18 SB_GPIO19 100 1 2 R2303
GPIO36/SATA2GP — AH19
GPIO37/SATA3GP — AE19 SB_GPIO37 100 1 2 R2305
SATA_C_DET_L 36 IN

CLK14 — AC1 SB_CLK14P3M_TIMER 34 IN
CLK48 — B2 SB_CLK48M_USBCTLR 34 IN
SUSCLK — C20 SUS_CLK_SB 8 OUT

SLP_S3* — B24 PM_SLP_S3_L 64 46 OUT
SLP_S4* — D23 PM_SLP_S4_L 64 46 OUT
SLP_S5* — F22 PM_SLP_S5_L 46 OUT
PWROK — AA4 PM_SB_PWROK 26 IN
AC22 PM_DPRSLPVR 81 56 14 OUT
GPIO16/DPRSLPVR — C21 NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
TP0/BATLOW* — PM_BATLOW_L 46 IN
PWRBTN* (INT 20K PUP) — C23 PM_PWRBTN_L 46 IN
LAN_RST* — C19 PM_LAN_ENABLE 46 IN
NOTE: SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F IN RESET STATE TO SAVE PWR
RSMRST* — Y4 PM_RSMRST_L 46 IN

GPIO9 — E20 SMS_INT_L 47 46 IN
GPIO10 — A20 SMC_SB_NMI 46 IN
DEF=GPI GPIO12 — F19 PATA_PWR_EN_L 23 OUT
GPIO13 — E19
DEF=GPI GPIO14 — R4 IDE_RESET_L 36 OUT
GPIO15 — E22 SV_SET_UP 5 23 48
GPIO24 — R3 CRB_SV_DET 23
GPIO25 — D20 TP_SB_GPIO25_DO_NOT_USE
OD GPIO35 — AD21 SB_CLK100M_SATA_OE_L 33 OUT
GPIO38 — AD20 TP_SB_GPIO38 NOA
DEF=GPI GPIO39 — AE20 SATA_C_PWR_EN_L 23 OUT

GPIO

=PP3V3_S5_SB_PM 11 26 62

R2319 10K 1/16W 402 2MF-LF 5%
R2343 8.2K 1/16W 402 2MF-LF 5%

R2399 100K 5% 1/16W 402 2MF-LF

SMC_WAKE_SCI_L 46 IN

NOSTUFF
R2300 0

SMC_RUNTIME_SCI_L 46 IN
SMC_EXTSMI_L 46 IN

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

=PP3V3_S5_SB 62 25 23

R2306 NOSTUFF 10K 1/16W 402 2MF-LF 5%
R2308 10K 1/16W 402 2MF-LF 5%

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

SV_SET_UP 5 23 48
CRB_SV_DET 23

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

R2307 10K 1/16W 402 2MF-LF 5%
R2309 NOSTUFF 0 1/16W 402 2MF-LF 5%

=PP3V3_S5_SB 62 25 23

R2313 10K 1/16W 402 2MF-LF 5%
R2310 10K 1/16W 402 2MF-LF 5%

FWH_MFG_MODE 23
BIOS_REC 23

R2314 NOSTUFF 0 1/16W 402 2MF-LF 5%
R2311 NOSTUFF 10K 1/16W 402 2MF-LF 5%

=PP3V3_S5_SB 23 25 62

R2390 10K 5% 1/16W 2MF-LF 402

PATA_PWR_EN_L 23

=PP3V3_S0_SB_GPIO 21 23 62

R2388 10K 5% 1/16W 2MF-LF 402

SATA_C_PWR_EN_L 23

SB: 3 OF 4

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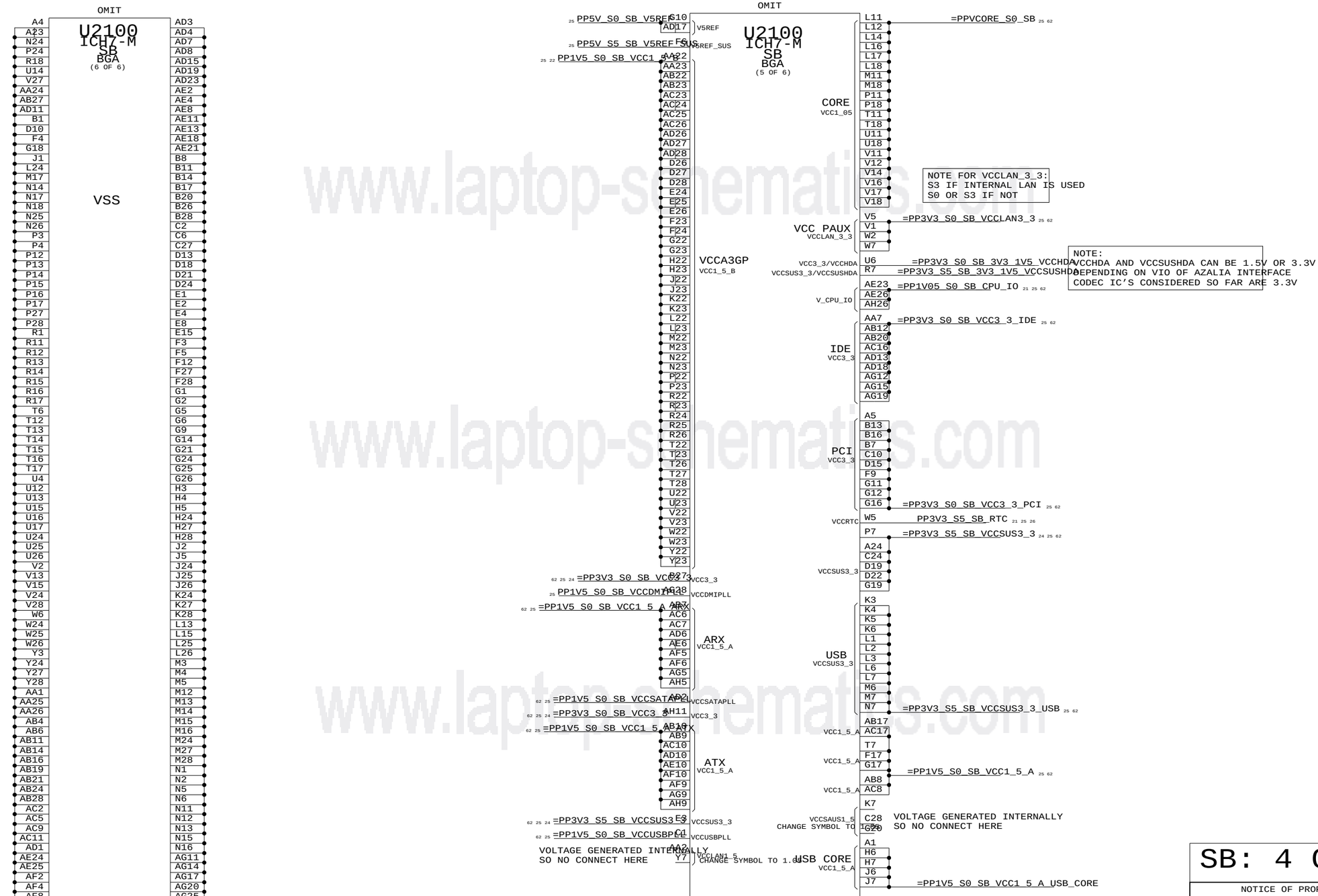
SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	23	81



SB: 4 OF 4

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	24	81

=PP3V3_S0_SB
=PP5V_S0_SB
R2502 100 1/16W MF-LF 402 5%
D2502 BAT54DW SOT-363
ICH V5REF BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON CORE WELL INPUT)
PP5V_S0_SB_V5REF
VOLTAGE=5V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C2503 0.1UF 10% 16V X5R 402
0V
PLACEMENT NOTE:
PLACE C2503 < 2.54MM OF PIN AD17 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY

=PP3V3_S5_SB
=PP5V_S5_SB
R2501 10 1/16W MF-LF 402 5%
D2502 BAT54DW SOT-363
ICH V5REF_SUS BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON RESUME WELL LOGIC)
PP5V_S5_SB_V5REF_SUS
VOLTAGE=5V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C2504 0.1UF 10% 16V X5R 402
0V
PLACEMENT NOTE:
PLACE C2504 < 2.54MM OF PIN F6 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY

=PP1V5_S0_SB
L2500 100-OHM-EMI SM-3
ICH VCCA3GP(VCC1_5_B BYPASS
(ICH IO,LOGIC 1.5V PWR)
PP1V5_S0_SB_VCC1_5_B
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C2500 270UF 20% 2.5V POLY SMB2
C2505 0.1UF 10% 16V X5R 402
C2506 0.1UF 10% 16V X5R 402
C2507 0.1UF 10% 16V X5R 402
0V
PLACEMENT NOTE:
PLACE C2500 & C2505-07 < 2.54MM OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
NEAR PINS D28, T28, AD28

=PP3V3_S0_SB_VCC3_3
ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
C2509 0.1UF 10% 16V X5R 402
0V
PLACEMENT NOTE:
PLACE C2509 NEAR PIN B27 OF SB

=PP1V5_S0_SB
R2500 1/10W5% MF-LF003
L2507 0.28-OHM 1206
PP1V5_S0_SB_VCCDMIPLL
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
ICH VCCDMIPLL BYPASS
(ICH DMI PLL 1.5V PWR)
C2501 0.01UF 10% 16V CERM 402
C2508 10UF 20% 6.3V X5R 603
0V
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON
SECONDARY SIDE OR 3.56MM ON PRIMARY

ICH VCC1_5_A/ARX BYPASS
(ICH LOGIC&IO[ARX] 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_ARX
C2511 0.1UF 10% 16V X5R 402
0V
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AG5

ICH VCCSATAPLL BYPASS
(ICH SATA PLL 1.5V PWR)
=PP1V5_S0_SB_VCCSATAPLL
C2517 0.1UF 10% 16V X5R 402
0V
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AD2

ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
=PP3V3_S0_SB_VCC3_3
C2513 0.1UF 10% 16V X5R 402
0V
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AH11

ICH VCC1_5_A/ATX BYPASS
(ICH LOGIC&IO[ATX] 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_ATX
C2514 1UF 10% 6.3V CERM 402
0V
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AG9

ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
=PP3V3_S5_SB_VCCSUS3_3
C2520 0.1UF 10% 16V X5R 402
0V
PLACEMENT NOTE:
PLACE C2520 NEAR PIN E3 OF SB

ICH VCCUSBPLL BYPASS
(ICH USB PLL 1.5V PWR)
=PP1V5_S0_SB_VCCUSBPLL
C2515 0.1UF 10% 16V X5R 402
0V
PLACEMENT NOTE:
PLACE C2520 NEAR PIN C1 OF SB

PLACEMENT NOTE:
PLACE CAPS AT EDGE OF SB
ICH CORE/VCC1_05 BYPASS
(ICH CORE 1.05V PWR)
=PPVCORE_S0_SB
C2518 0.1UF 10% 16V X5R 402
C2502 1UF 10% 6.3V CERM 402
C2516 330UF 20% 2.5V POLY CASE-C2
PLACEHOLDER FOR 270UF
0V

ICH VCC_PAUX/VCCLAN3_3 BYPASS
(ICH LAN I/F BUFFER 3.3V PWR)
=PP3V3_S0_SB_VCCLAN3_3
C2519 0.1UF 10% 16V X5R 402
0V
PLACEMENT NOTE:
PLACE CAP UNDER SB NEAR PINS
V5, W2, OR W7

ICH VCC3_3/VCCHDA BYPASS
(ICH INTEL HDA CORE 3.3V PWR)
=PP3V3_S0_SB_3V3_1V5_VCCHDA
C2521 0.1UF 10% 16V X5R 402
0V
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN U6

ICH V_CPU_IO BYPASS
(ICH CPU I/O 1.05V PWR)
=PP1V05_S0_SB_CPU_IO
C2523 0.1UF 10% 16V X5R 402
C2522 0.1UF 10% 16V X5R 402
C2524 4.7UF 20% 6.3V CERM 603
0V
PLACEMENT NOTE:
PLACE NEAR PINS AE23, AE26 & AH26 OF SB

ICH IDE/VCC3_3 BYPASS
(ICH IDE I/O 3.3V PWR)
=PP3V3_S0_SB_VCC3_3_IDE
C2525 0.1UF 10% 16V X5R 402
0V
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AA7

ICH PCI/VCC3_3 BYPASS
(ICH PCI I/O 3.3V PWR)
=PP3V3_S0_SB_VCC3_3_PCI
C2526 0.1UF 10% 16V X5R 402
C2527 0.1UF 10% 16V X5R 402
C2528 0.1UF 10% 16V X5R 402
0V
PLACEMENT NOTE:
DISTRIBUTE IN PCI SECTION OF SB
NEAR PINS A5 ... G16

ICH VCCRTC BYPASS
(ICH RTC 3.3V PWR)
=PP3V3_S5_SB_RTC
C2530 0.1UF 10% 16V X5R 402
C2529 0.1UF 10% 16V X5R 402
0V
PLACEMENT NOTE:
PLACE CAPS NEAR PIN W5 OF SB

ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
=PP3V3_S5_SB_VCCSUS3_3
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
A24 ... G19 AND P7 OF SB
C2531 0.1UF 10% 16V X5R 402
C2534 0.1UF 10% 16V X5R 402
0V

ICH USB/VCCSUS3_3 BYPASS
(ICH SUSPEND USB 3.3V PWR)
=PP3V3_S5_SB_VCCSUS3_3_USB
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
K3 ... N7 OF SB
C2533 0.1UF 10% 16V X5R 402
C2532 0.1UF 10% 16V X5R 402
0V

ICH VCC1_5A BYPASS
(ICH LOGIC&IO 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
AB8 AND AC8 OF SB
C2510 0.1UF 10% 16V X5R 402
0V

ICH USB CORE/VCC1_5_A BYPASS
(ICH USB CORE 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_USB_CORE
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS A1 ... A7
C2512 0.1UF 10% 16V X5R 402
0V

SB: 4 OF 4

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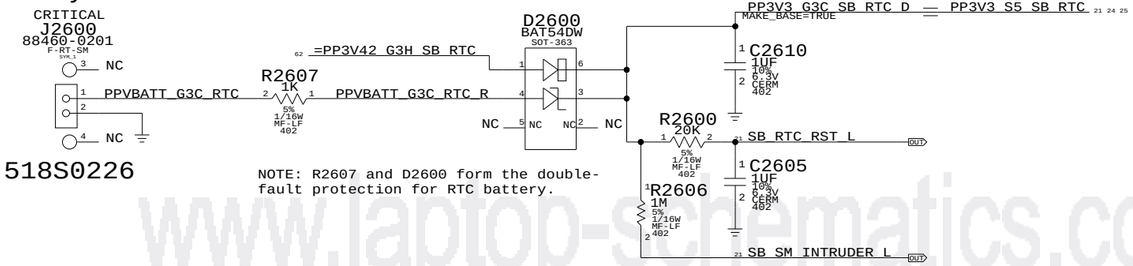
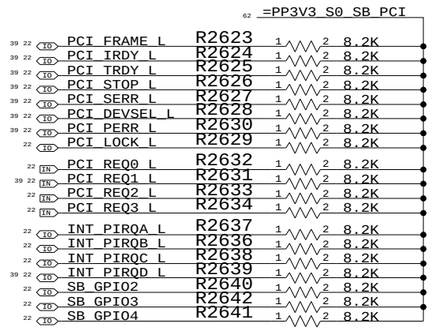
SIZE	DRAWING NUMBER	REV.
D	051-6941	07001
SCALE: NONE	SHT 25 OF 81	

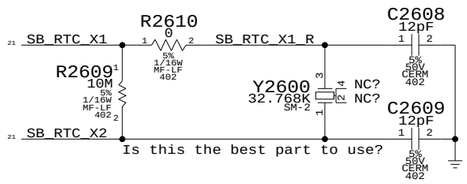
RTC Battery Connector



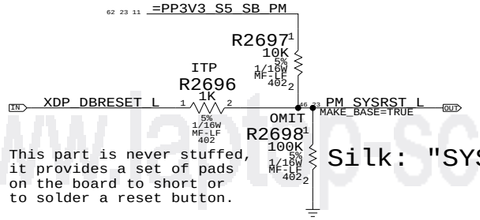
NOTE: R2607 and D2600 form the double-fault protection for RTC battery.



SB RTC Crystal Circuit



Is this the best part to use?

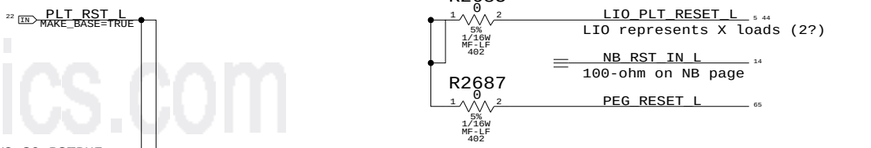


This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

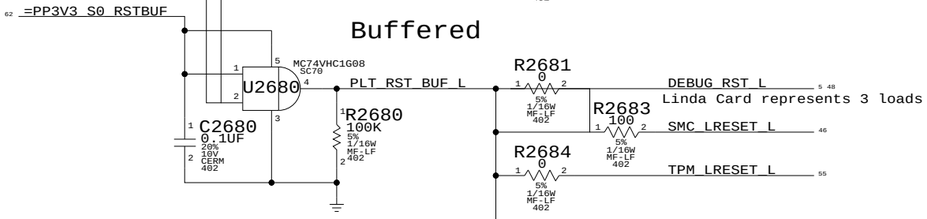
Silk: "SYS RST"

Platform Reset Connections

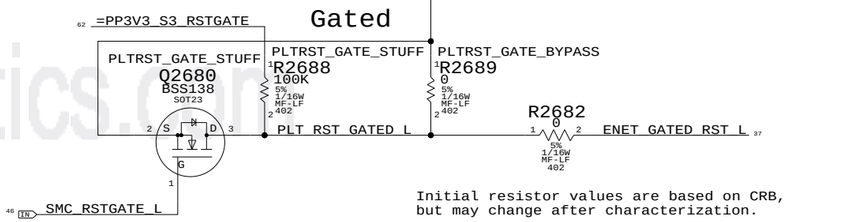
Unbuffered



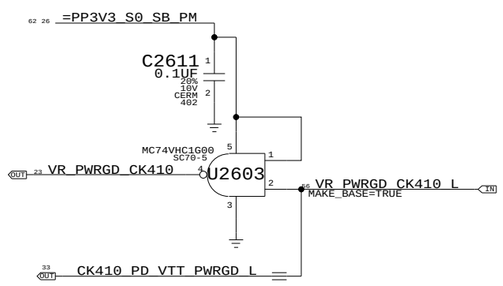
Buffered



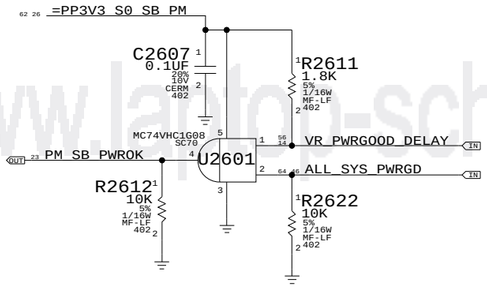
Gated



Initial resistor values are based on CRB, but may change after characterization.



1G00 used as small & cheap inverter



SB Misc

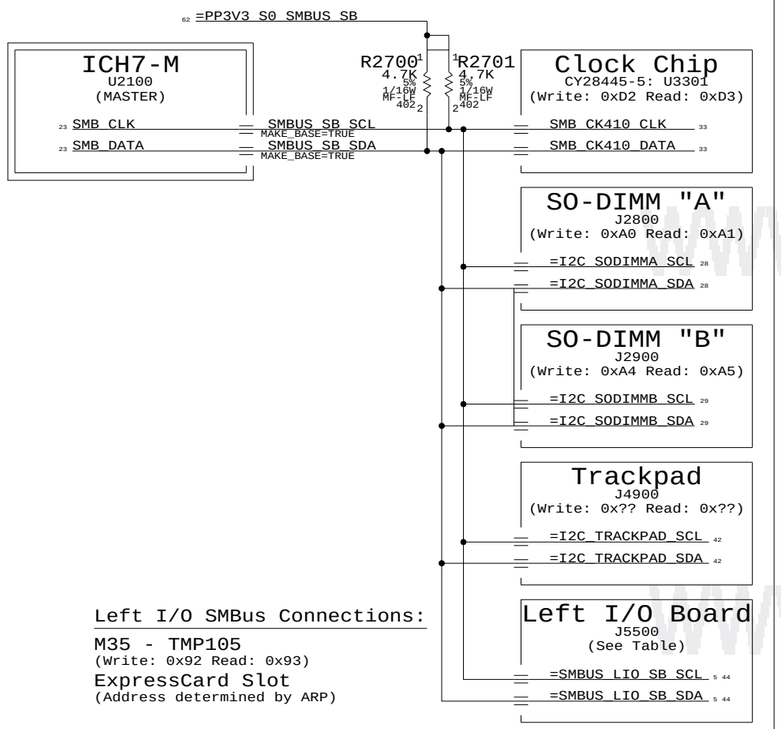
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

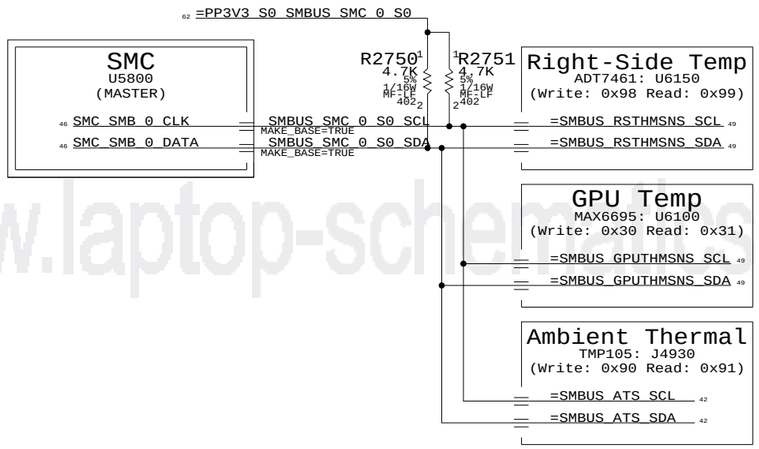
SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	26	81

ICH7-M SMBus Connections

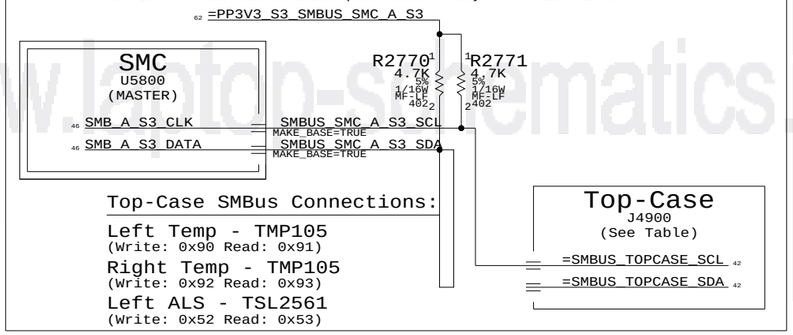


SMC "0" SMBus Connections

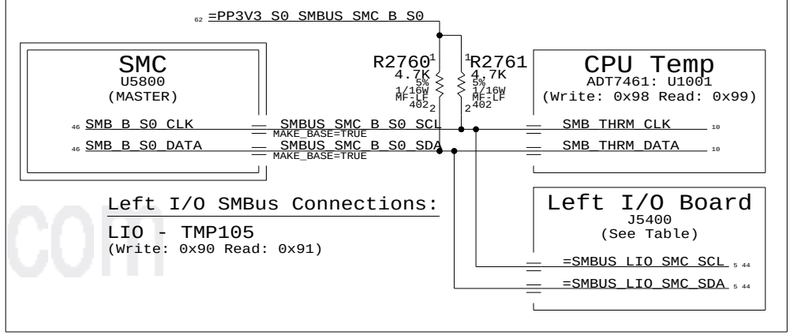


SMC "A" SMBus Connections

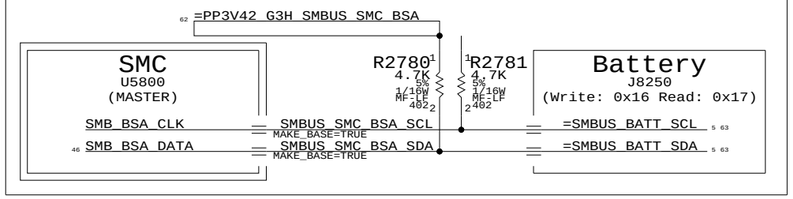
NOTE: SMC RMT bus remains powered and may be active in S3 state



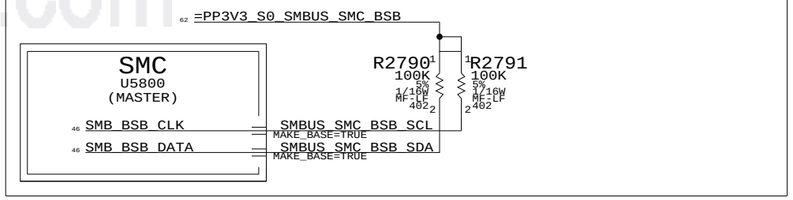
SMC "B" SMBus Connections



SMC "Battery A" SMBus Connections



SMC "Battery B" SMBus Connections



M1 SMBus Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	27	81

Page Notes

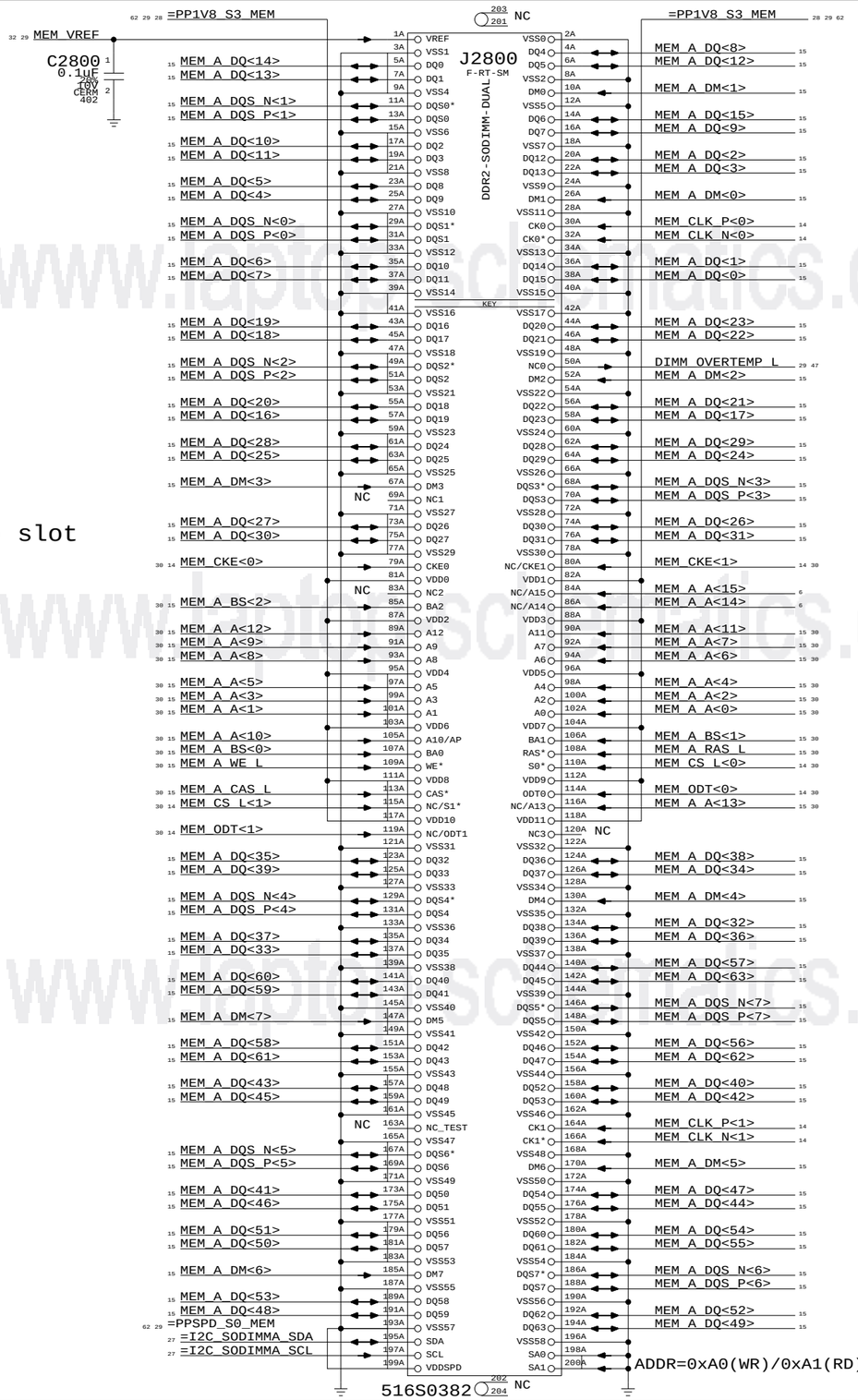
Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

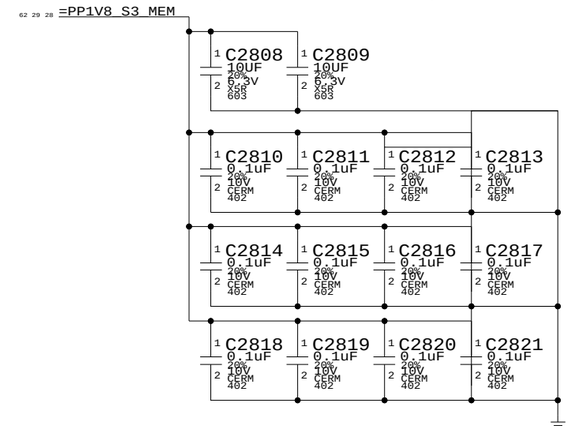
Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

"Upper" (surface-mount) slot





DDR2 SO-DIMM Connector A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001
SCALE: NONE	SHT 28 OF 81	

Page Notes

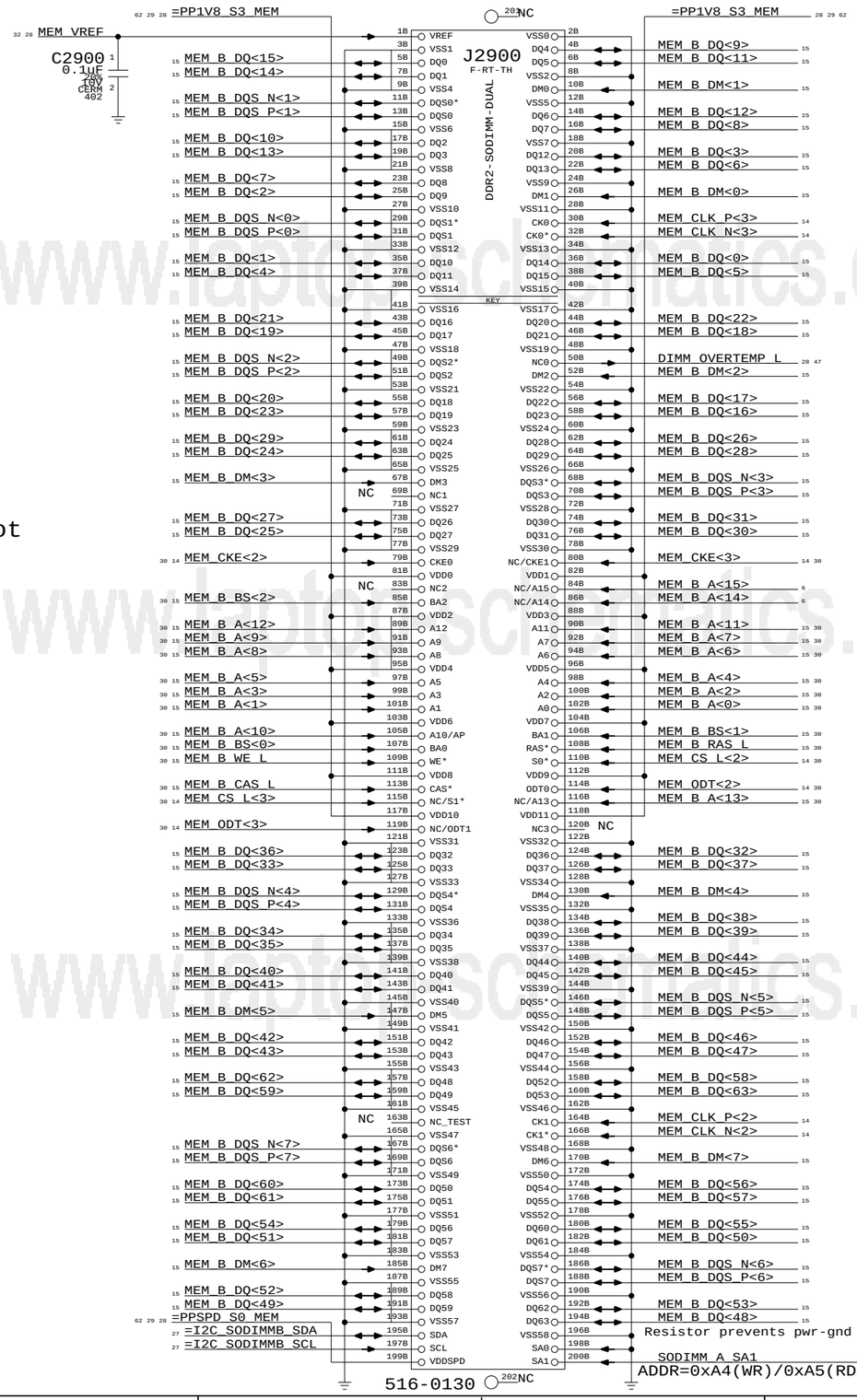
Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

"Lower" (thru-hole) slot



DDR2 Bypass Caps

(For return current)

DDR2 SO-DIMM Connector B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

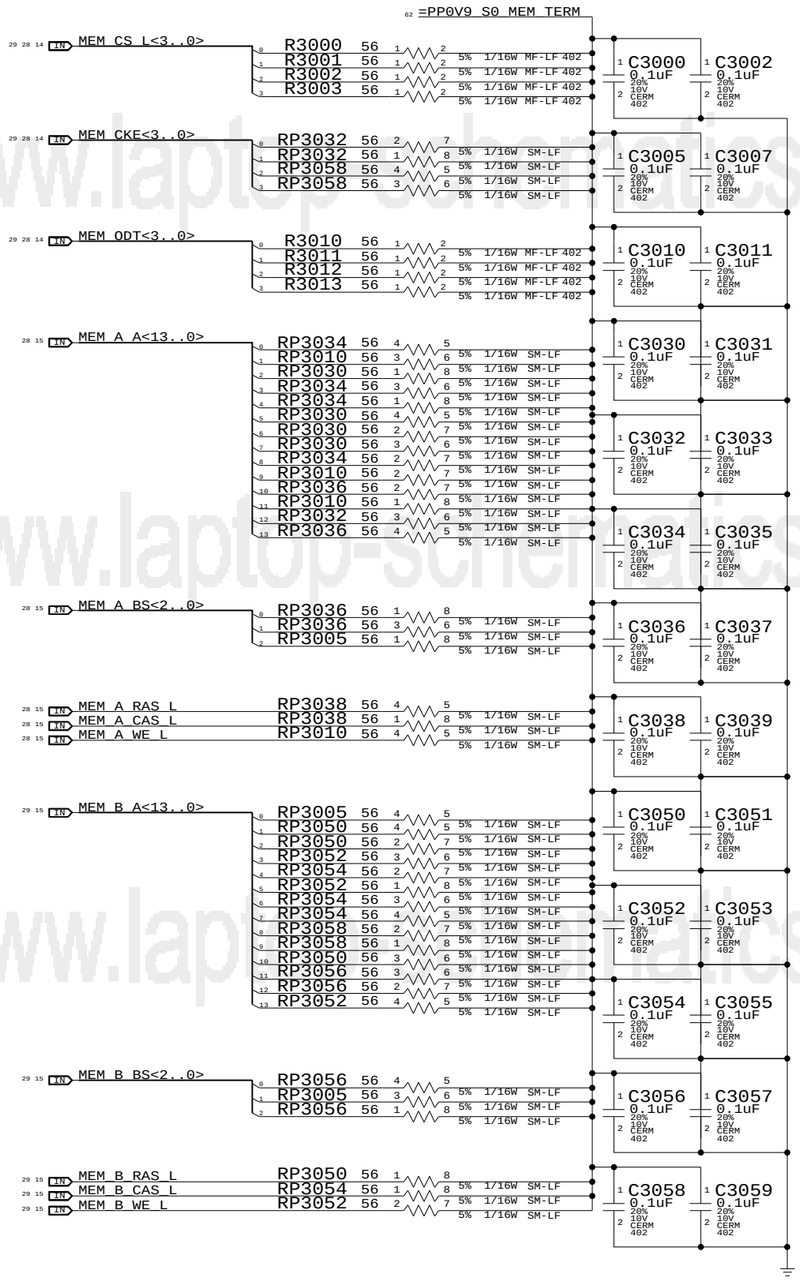
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	29	81

One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	30	81

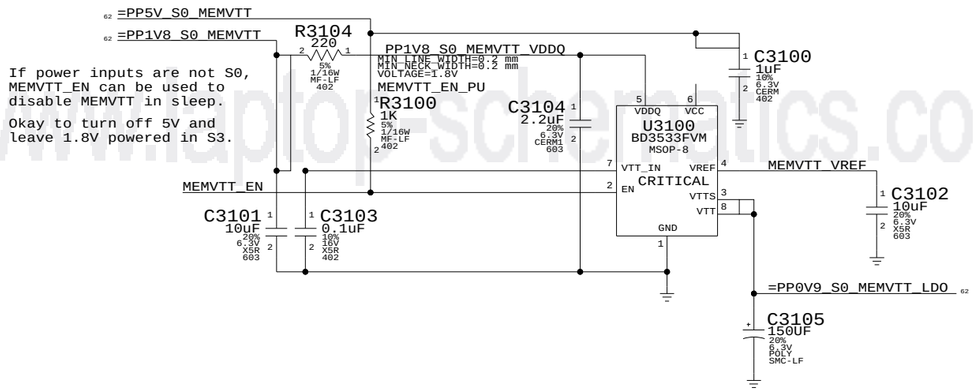
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



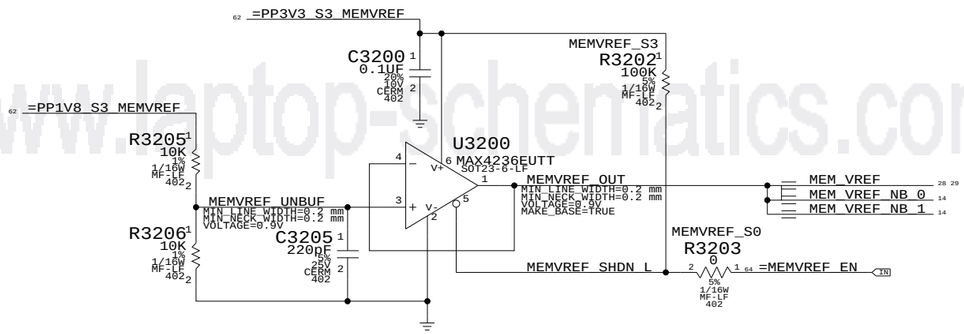
Memory Vtt Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	31	81



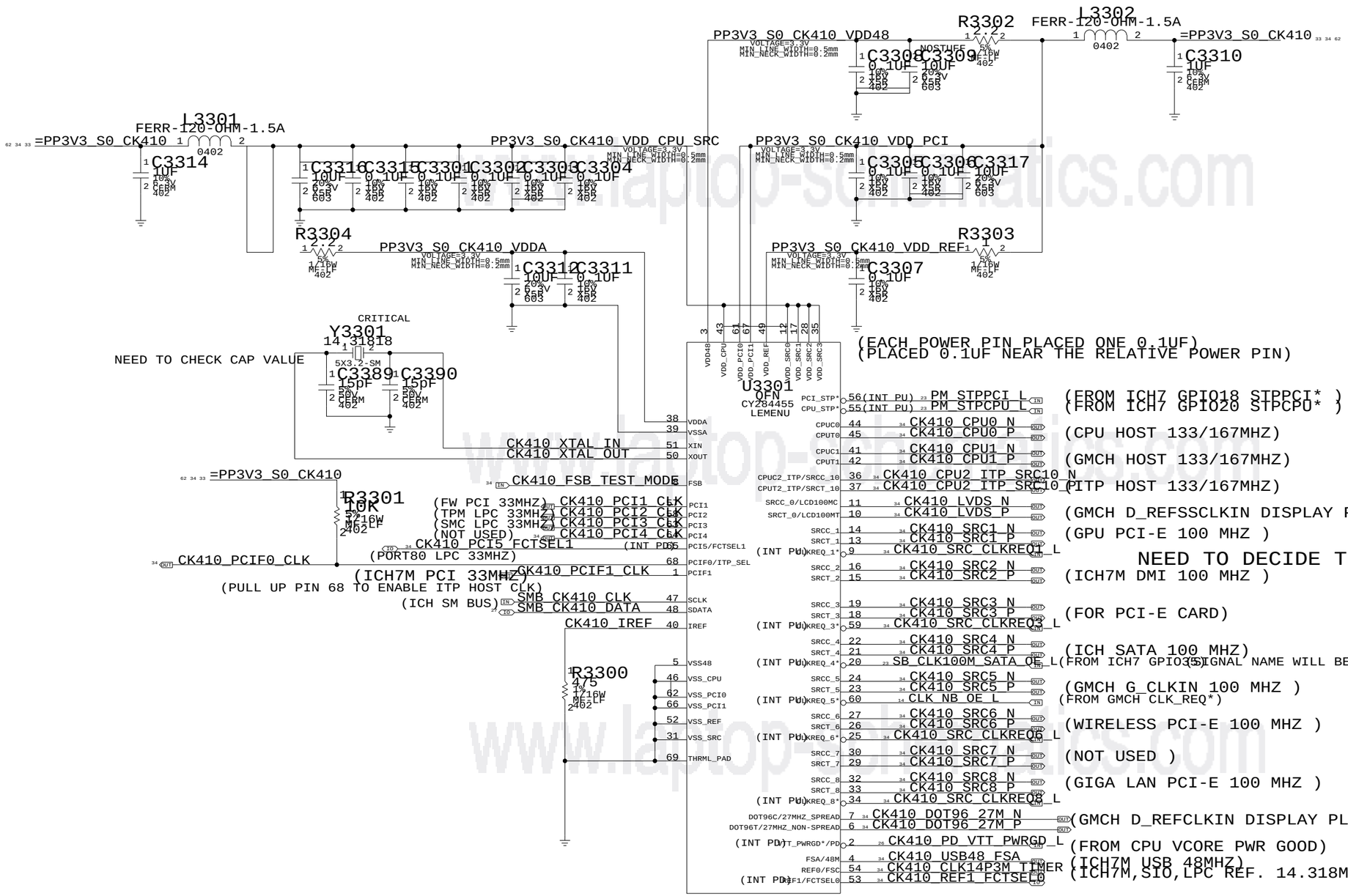
DDR2 VRef

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	32	81



FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M_NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	BD	SRCT0	SRCC0	

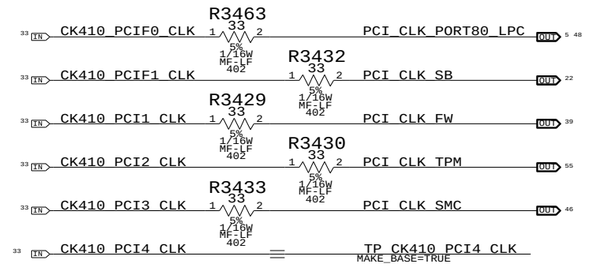
CLOCKS

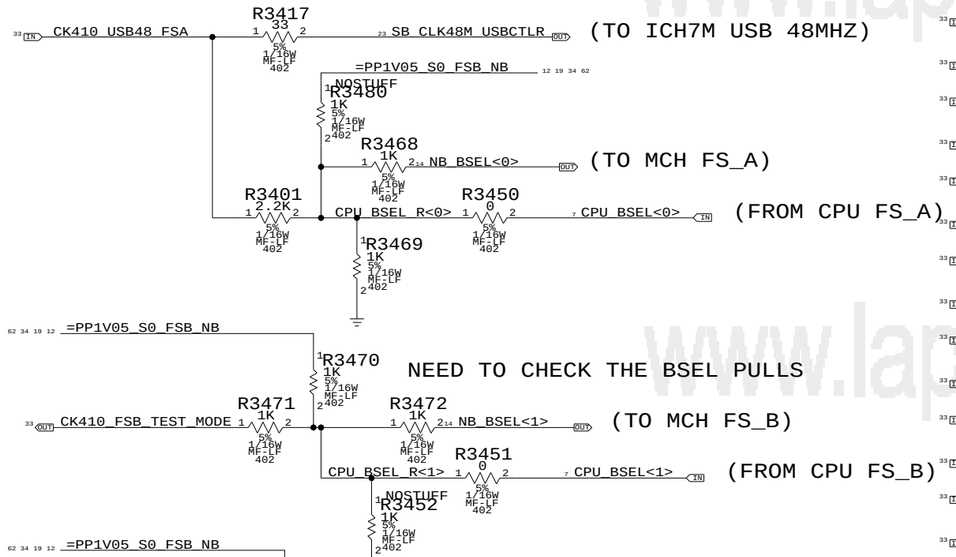
SYNC_MASTER=MAY SYNC_DATE=09/08/2005

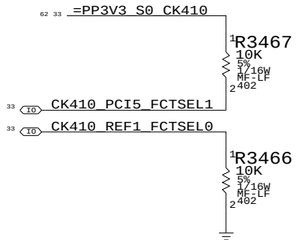
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	33	81



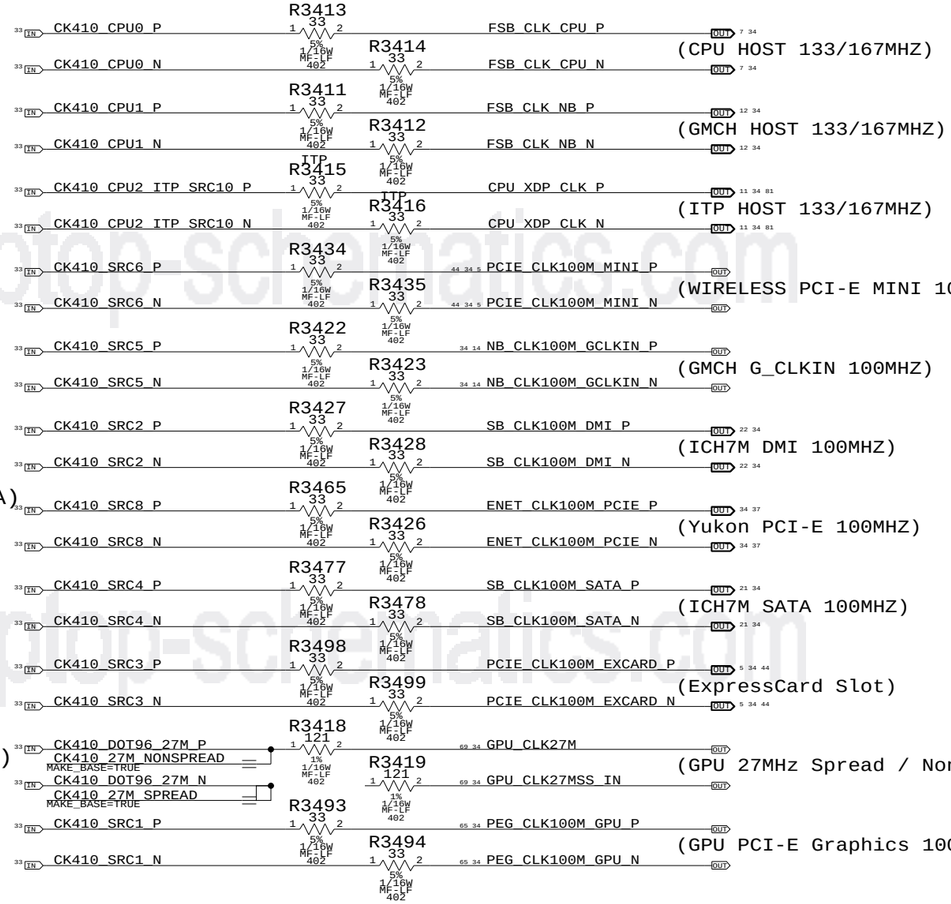


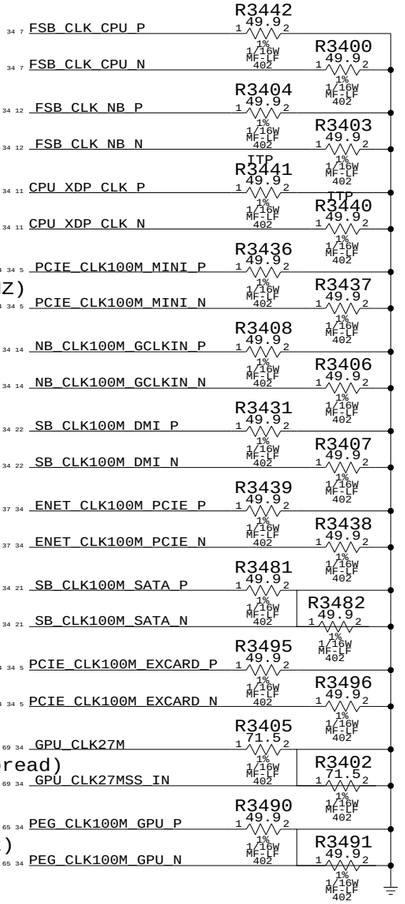


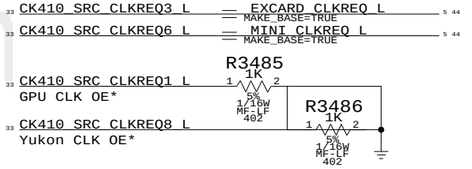
NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

	FS_C	FS_B	FS_A	CPU
	0	0	0	266M
#	0	0	1	133M
#	0	1	0	166M
	0	1	1	200M
	1	0	0	100M
	1	0	1	333M
	1	1	0	400M
	1	1	1	RESERVED

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED







Clock Termination

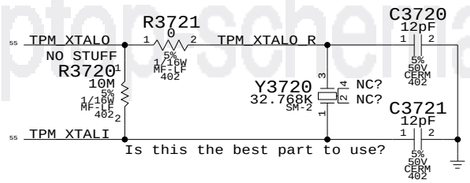
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

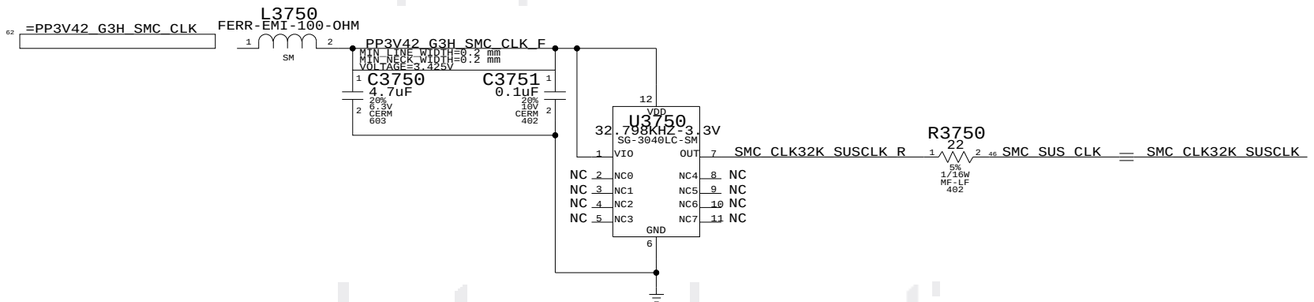
SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	34	81

TPM Crystal Circuit



SMC G3Hot Oscillator



Mobile Clocking

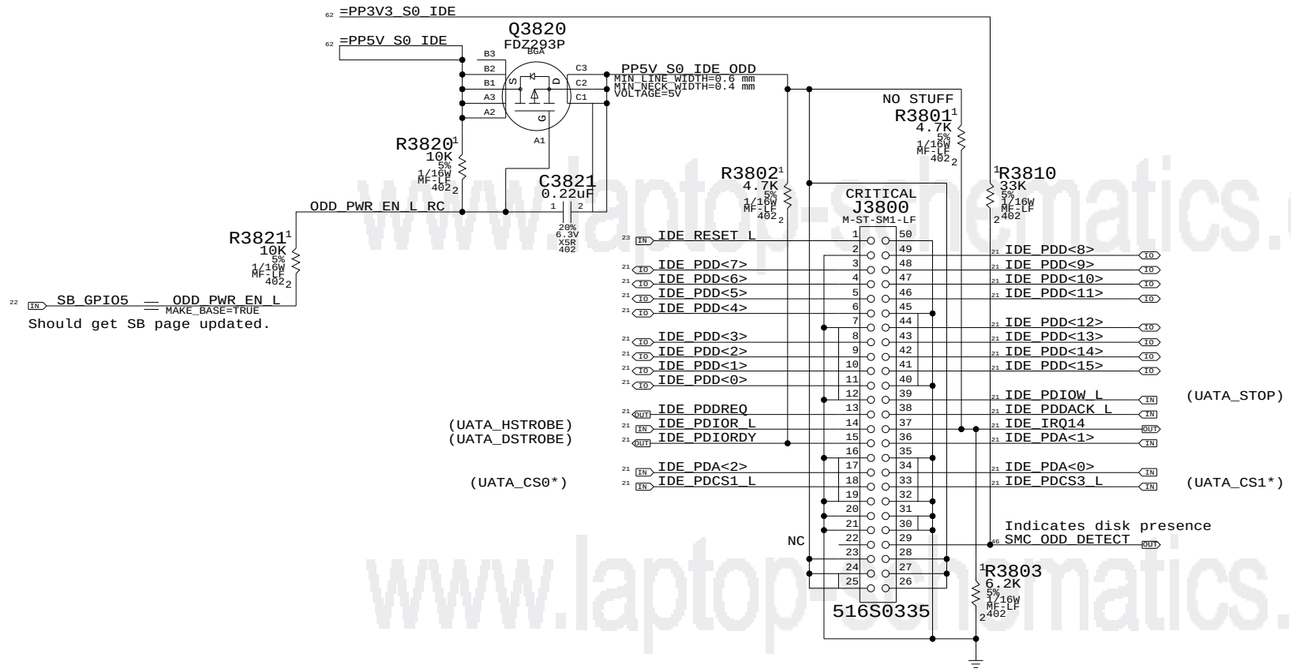
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

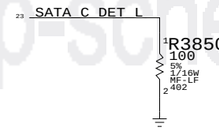
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	35	81

IDE (ODD) Connector





21 SATA_A_R2D_C_P — TP_SATA_A_R2DP (MAKE_BASE=TRUE)
21 SATA_A_R2D_C_N — TP_SATA_A_R2DN (MAKE_BASE=TRUE)
21 SATA_A_D2R_P — TP_SATA_A_D2RP (MAKE_BASE=TRUE)
21 SATA_A_D2R_N — TP_SATA_A_D2RN (MAKE_BASE=TRUE)

21 SATA_RBIAS_P
21 SATA_RBIAS_N
SATA_RBIAS (MAKE_BASE=TRUE)

Placement note
Place within 12.7mm
from ball of SB

R3860 24.9 1% 1/16W MF-LF 402

PATA Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	36	81

PLACE C4100-C4106 NEAR PINS AVDLL0-AVDLL6.
SCHEME MATCHES DOC MVL100258-01

MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=2.5V

PP2V5_S3_ENET_AVDD

C4100 1UF 10% 6.3V CERM 402
C4101 0.1UF 10% 16V X5R 402
C4102 0.1UF 10% 16V X5R 402
C4103 0.1UF 10% 16V X5R 402
C4104 0.1UF 10% 16V X5R 402
C4105 0.001UF 10% 50V CERM 402
C4106 0.001UF 10% 50V CERM 402
C4107 0.1UF 10% 16V X5R 402

L4100 FERR-120-OHM-1.5A 0402 =PP2V5_S3_ENET

PLACE C4107 NEAR U4101 AVDD

=PP3V3_S3_ENET
=PP1V2_S3_ENET
=PP3V3_S3_ENET

R4101 4.7K 5% 1/16W MF-LF 402

PLACE C4110 AND C4111 WITHIN
12 MIL OF U4101 PIN 49 AND 50

C4110 0.1UF 10% 16V X5R 402
C4111 0.1UF 10% 16V X5R 402
C4112 0.1UF 10% 16V X5R 402

PCIE_A_D2R_C_P
PCIE_A_D2R_C_N
PCIE_A_D2R_P
PCIE_A_D2R_N

PCIE_A_R2D_P
PCIE_A_R2D_N
PCIE_A_R2D_C_P
PCIE_A_R2D_C_N

C4113 0.1UF 10% 16V X5R 402
PLACE C4113 AND C4112 WITHIN
12 MIL OF U2100 E27 AND E28

ENET_CLK100M_PCIE_P
ENET_CLK100M_PCIE_N
PCIE_WAKE_L
ENET_GATED_RST_L

LEMENU
U4101
88E8053
QFN

OPTIONAL EXTERNAL LDO

ANALOG
PCI EXPRESS
LED
MEDIA
TEST
TWSI
SPI
MAIN CLK

NO PULL-UP NEEDED

R4102 4.87K 1% 1/16W MF-LF 402

ENET_CTRL25
ENET_CTRL12
ENET_RSET

ENET_MDI P<0>
ENET_MDI N<0>
ENET_MDI P<1>
ENET_MDI N<1>
ENET_MDI P<2>
ENET_MDI N<2>
ENET_MDI P<3>
ENET_MDI N<3>

R4106 49.9 1% 1/16W MF-LF 402
R4105 49.9 1% 1/16W MF-LF 402
R4104 49.9 1% 1/16W MF-LF 402
R4103 49.9 1% 1/16W MF-LF 402
R4120 49.9 1% 1/16W MF-LF 402
R4119 49.9 1% 1/16W MF-LF 402
R4118 49.9 1% 1/16W MF-LF 402
R4117 49.9 1% 1/16W MF-LF 402

ENET_MDI0
ENET_MDI1
ENET_MDI2
ENET_MDI3

C4116 0.001UF 10% 50V CERM 402
C4115 0.001UF 10% 50V CERM 402
C4117 0.001UF 10% 50V CERM 402
C4118 0.001UF 10% 50V CERM 402

PLACE RESISTORS CLOSE TO U4101

ENET_VPD_CLK
ENET_VPD_DATA
ENET_PU_VDD_TTL0
ENET_PU_VDD_TTL1

ASF IS UNAVAILABLE ON 8053

INTERNAL PULL-UP

CRITICAL

1. KEEP ENET_XTALI AND ENET_XTALO TRACE LENGTH <12MIL
2. DO NOT ROUTE UNDER CRYSTAL

Y4101 25.0000M SM-3
C4150 22pF 5% 50V CERM 402
C4151 22pF 5% 50V CERM 402

THRML_PAD

=PP3V3_S3_ENET

R4130 4.7K 5% 1/16W MF-LF 402
R4131 4.7K 5% 1/16W MF-LF 402

PLACE C4140 NEAR U4102 VCC

C4140 0.1UF 10% 16V X5R 402

U4102 M24C08 SO8

R4122 4.7K 5% 1/16W MF-LF 402
R4123 4.7K 5% 1/16W MF-LF 402

PLACE C4127-C4134 NEAR PINS VDD0-VDD7 ON U4101
SCHEME MATCHES DOC MVL100258-01

=PP1V2_S3_ENET

C4126 0.1UF 10% 16V X5R 402
C4127 0.1UF 10% 16V X5R 402
C4128 0.1UF 10% 16V X5R 402
C4129 0.1UF 10% 16V X5R 402
C4130 0.1UF 10% 16V X5R 402
C4131 0.001UF 10% 50V CERM 402
C4132 0.001UF 10% 50V CERM 402
C4133 0.001UF 10% 50V CERM 402
C4134 0.001UF 10% 50V CERM 402

PLACE C4135-C4139 NEAR VDDO_TTL0-VDD_TTL4 ON U4101
SCHEME MATCHES DOC MVL100258-01

=PP3V3_S3_ENET

C4135 0.1UF 10% 16V X5R 402
C4136 0.1UF 10% 16V X5R 402
C4137 0.1UF 10% 16V X5R 402
C4138 0.001UF 10% 50V CERM 402
C4139 0.001UF 10% 50V CERM 402

ETHERNET CONTROLLER

SYNC_MASTER=M42 SYNC_DATE=09/08/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001
SCALE: NONE	SHT 37 OF 81	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED BY ETHERNET PHY	ENETCONN	ENET_100D	ENETCONN_P<0>
	ENETCONN	ENET_100D	ENETCONN_N<0>
	ENETCONN	ENET_100D	ENETCONN_P<1>
	ENETCONN	ENET_100D	ENETCONN_N<1>
	ENETCONN	ENET_100D	ENETCONN_P<2>
	ENETCONN	ENET_100D	ENETCONN_N<2>
	ENETCONN	ENET_100D	ENETCONN_P<3>
	ENETCONN	ENET_100D	ENETCONN_N<3>

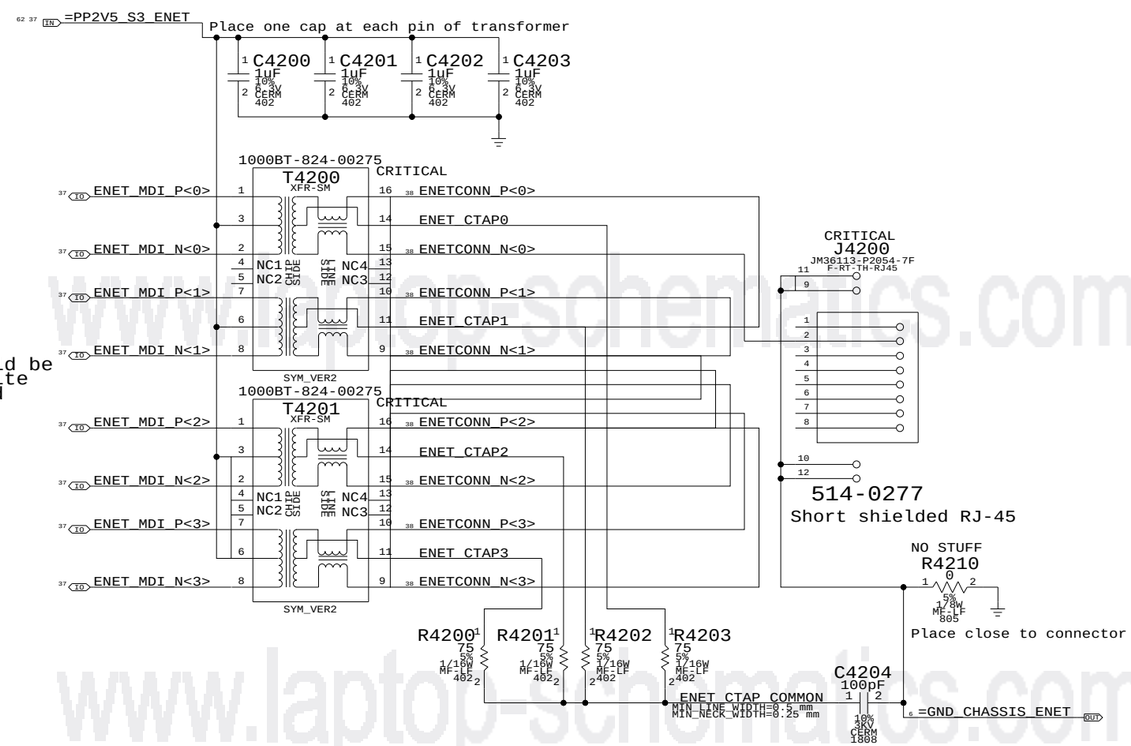
Page Notes

Power aliases required by this page:
- =PP2V5_ENET
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Transformers should be mirrored on opposite sides of the board



Ethernet Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	38	81

PAGE NOTES

INPUT

=PP3V3_S0_FW - 3.3V POWER FOR FIREWIRE (MOBILE: OFF DURING SLEEP)
=PP3V3_S0_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)
PCI_GNT3_L - PCI GRANT FROM SB
PCI_CLK_FW - NEED TO REFERENCE TO ALIAS PAGE
PCI_RST_L - PCI RESET FROM SB
FW_PC0 - FIREWIRE POWER CLASS IDENTIFIER

INPUT/OUTPUT

PCI_AD<0..31>,PCI_C_BE_L<0..3>,PCI_FRAME_L,PCI_IRDY_L,PCI_TRDY_L,
PCI_DEVSEL_L, PCI_STOP_L, PCI_PAR, PCI_PERR_L, PCI_SERR_L
FW_A_TPA_P/N, FW_A_TPB_P/N, FW_A_TPBIAS - PORT 0 FIREWIRE DIFF PAIRS
FW_B_TPA_P/N, FW_B_TPB_P/N, FW_B_TPBIAS - PORT 1 FIREWIRE DIFF PAIRS
FW_C_TPA_P/N, FW_C_TPB_P/N, FW_C_TPBIAS - PORT 2 FIREWIRE DIFF PAIRS

OUTPUT

PCI_REQ3_L - PCI REQUEST TO SB
PM_CLKRUN_L - CLOCK-RUN PCI PROTOCOL
INT_PIRQD_L - INTERRUPT TO SB
PCI_PME_FW_L - DEDICATED PME FOR FIREWIRE (SB GPIO1)

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
6/20/2005 - BGA VERSION OF FW23256 ADDED
6/21/2005 - CHANGED INT_PIRQD_L TO INT_PIRQD_L (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED PCI_IO TO ADD 3 (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED REQ/GNT TO REQ3/GNT3 (PER ARCHITECTURAL DEFINITION)
6/22/2005 - ADDED 510K PULL-DOWN ON RST* AND REMOVED CONNECTION TO PLT_RST_L
6/22/2005 - CHANGED CLK_FW DIFF PAIR NAMES TO BE RE-USE COMPLIANT
6/22/2005 - REMOVED CONSTRAINT SETS AS THEY WILL BE MANAGED ON BOARD SIDE
6/22/2005 - REMOVED C4421 - REDUNDANT
6/22/2005 - BRING OUT PC0 CONNECTION TO BE CONNECTED ON PORT PAGE
7/26/2005 - CONNECTED PIN E10 TO GND

MOBILE TURNS OFF CONTROLLER POWER DURING SLEEP
0.001A DURING SLEEP

62 =PP3V3_S3_FW

PLACE ONE CAP PER TWO PINS STARTING WITH C4424 ON VDD0

C4424 10UF 20% 6.3V X5R 603
C4418 0.1UF 10% 16V X5R 402
C4422 0.1UF 10% 16V CERM 402
C4426 0.1UF 10% 16V CERM 402
C4428 0.1UF 10% 16V CERM 402
C4430 0.1UF 10% 16V CERM 402
C4432 0.1UF 10% 16V CERM 402

L4400
600-OHM-300MA
0402

PLACE ONE CAP PER TWO PINS STARTING WITH C4416 ON VDDA0

C4416 10UF 20% 6.3V X5R 603
C4417 0.1UF 10% 16V X5R 402
C4429 0.1UF 10% 16V X5R 402
C4425 0.1UF 10% 16V X5R 402

PP3V3_S3_FW_AVDD
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM

62 =PP3V3_S3_PCI

CONNECT TO VDD FOR 3.3V OPERATION

G4 VDD0
M1 VDD1
M2 VDD2
K5 VDD3
K6 VDD4
J7 VDD5
L13 VDD6
H10 VDD7
A2 VDD9
D10 VDDA0
A13 VDDA1
B13 VDDA2
A7 VDDA3
A8 VDDA4
D6 VDDA5

197S0030_3.2MMX2.5MM
CRITICAL

R4400 390 5% 1/16W MF-LF 402
Y4403 SM-2 24.576MHZ
C4411 15pF 5% 50V CERM 402
C4412 15pF 5% 50V CERM 402
NEED TO CHECK CRYSTAL LOAD CAPACITANCE

U4400
FW32306
BGA
LEMENU

		A10	PCI_VIOS
10	22 PCI_AD<0>	F10	PCI_AD0
10	22 PCI_AD<1>	G10	PCI_AD1
10	22 PCI_AD<2>	H10	PCI_AD2
10	22 PCI_AD<3>	H12	PCI_AD3
10	22 PCI_AD<4>	J13	PCI_AD4
10	22 PCI_AD<5>	J12	PCI_AD5
10	22 PCI_AD<6>	K13	PCI_AD6
10	22 PCI_AD<7>	K10	PCI_AD7
10	22 PCI_AD<8>	L12	PCI_AD8
10	22 PCI_AD<9>	M13	PCI_AD9
10	22 PCI_AD<10>	L11	PCI_AD10
10	22 PCI_AD<11>	M12	PCI_AD11
10	22 PCI_AD<12>	M11	PCI_AD12
10	22 PCI_AD<13>	N12	PCI_AD13
10	22 PCI_AD<14>	M10	PCI_AD14
10	22 PCI_AD<15>	N11	PCI_AD15
10	22 PCI_AD<16>	M4	PCI_AD16
10	22 PCI_AD<17>	N5	PCI_AD17
10	22 PCI_AD<18>	N4	PCI_AD18
10	22 PCI_AD<19>	M3	PCI_AD19
10	22 PCI_AD<20>	M2	PCI_AD20
10	22 PCI_AD<21>	N3	PCI_AD21
10	22 PCI_AD<22>	K4	PCI_AD22
10	22 PCI_AD<23>	M1	PCI_AD23
10	22 PCI_AD<24>	K2	PCI_AD24
10	22 PCI_AD<25>	J4	PCI_AD25
10	22 PCI_AD<26>	K1	PCI_AD26
10	22 PCI_AD<27>	J2	PCI_AD27
10	22 PCI_AD<28>	J1	PCI_AD28
10	22 PCI_AD<29>	H2	PCI_AD29
10	22 PCI_AD<30>	H4	PCI_AD30
10	22 PCI_AD<31>	H1	PCI_AD31
22 10	PCI_C_BE_L<0>	K12	PCI_CBE0*
22 10	PCI_C_BE_L<1>	M9	PCI_CBE1*
22 10	PCI_C_BE_L<2>	L3	PCI_CBE2*
22 10	PCI_C_BE_L<3>	L1	PCI_CBE3*
10	22 PCI_PAR	N10	PCI_PAR
10	22 25 PCI_FRAME_L	N6	PCI_FRAME*
10	22 25 PCI_IRDY_L	M6	PCI_IRDY*
10	22 25 PCI_TRDY_L	N7	PCI_TRDY*
10	22 25 PCI_DEVSEL_L	N8	PCI_DEVSEL*
10	22 25 PCI_STOP_L	M7	PCI_STOP*
	FW_PCI_IDSEL	L2	PCI_IDSEL
OUT	26 22 PCI_REQ1_L	E2	PCI_REQ*
IN	22 PCI_GNT1_L	E1	PCI_GNT*
10	22 25 PCI_PERR_L	M8	PCI_PERR*
10	22 25 PCI_SERR_L	N9	PCI_SERR*
IN	34 PCI_CLK_FW	G2	PCI_CLK
10	PM_CLKRUN_L	D1	CLKRUN*
	FW_PCI_RST_L	F1	PCI_RST*
OUT	26 22 INT_PIRQD_L	D2	PCI_INTA*
OUT	22 PCI_PME_FW_L	F2	PCI_PME*

R4431 22 5% 1/16W MF-LF 402

THIS IS FROM ICH-7M
22 PCI_RST_L
R4432 100 5% 1/16W MF-LF 402

XI	A5	FW_XI
XO	B5	FW_XO
RESET*	B4	FW_PWRON_RST_L
R1	A6	FW_R1
R0	B7	FW_R0

SPEC RECOMMENDS 2.49K
R4452 2.49K 1% 1/16W MF-LF 402
C4420 0.1UF 10% 16V X5R 402
R4420 510K 5% 1/16W MF-LF 402

TPBIAS0	B8	41 FW_A_TPBIAS
TPA0_P	A9	41 FW_A_TPA_P
TPA0_N	B9	41 FW_A_TPA_N
TPB0_P	B10	41 FW_A_TPB_P
TPB0_N	A10	41 FW_A_TPB_N
TPBIAS1	D8	41 FW_B_TPBIAS
TPA1_P	A11	41 FW_B_TPA_P
TPA1_N	B11	41 FW_B_TPA_N
TPB1_P	B12	41 FW_B_TPB_P
TPB1_N	A12	41 FW_B_TPB_N
TPBIAS2	C13	41 FW_C_TPBIAS
TPA2_P	C11	41 FW_C_TPA_P
TPA2_N	C12	41 FW_C_TPA_N
TPB2_P	D13	41 FW_C_TPB_P
TPB2_N	D12	41 FW_C_TPB_N

MODE FOR EXTERNAL LINK

MODE_420	M5	
MODE_A	B6	
PC0	E12	41 FW_PC0
PC1	F13	
PC2	F12	
CONTENDER	G12	LOW = NOT BUS MANAGER
CARDBUSN	B1	LOW = PCI OPERATION
MPCI_ACTN_323	E10	

10 DUAL PORT DEVICES ARE POWER CLASS 4 (‘100’)
SINGLE PORT DEVICES ARE POWER CLASS 0 (‘000’)

MANUFACTURING TEST PINS

TEST0	C2
TEST1	C1
TEST	A4
SE	A3
SM	B3

VSS0 A1
VSS1 B2
VSS2 C3
VSS3 D4
VSS4 E4
VSS5 E5
VSS6 F4
VSS7 F6
VSS8 F7
VSS9 F8
VSS10 G1
VSS11 H6
VSS12 G7
VSS13 G8
VSS14 H6
VSS15 H7
VSS16 H8
VSS17 J5
VSS18 J9
VSS19 J10
VSS20 K8
VSS21 K9
VSS22 N13
VSSA0 E13
VSSA1 E9
VSSA2 D9
VSSA3 D7
VSSA4 D5

FIREWIRE CONTROLLER

SYNC_MASTER=MSX SYNC_DATE=08/29/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001
SCALE: NONE	SHT 39 OF 81	

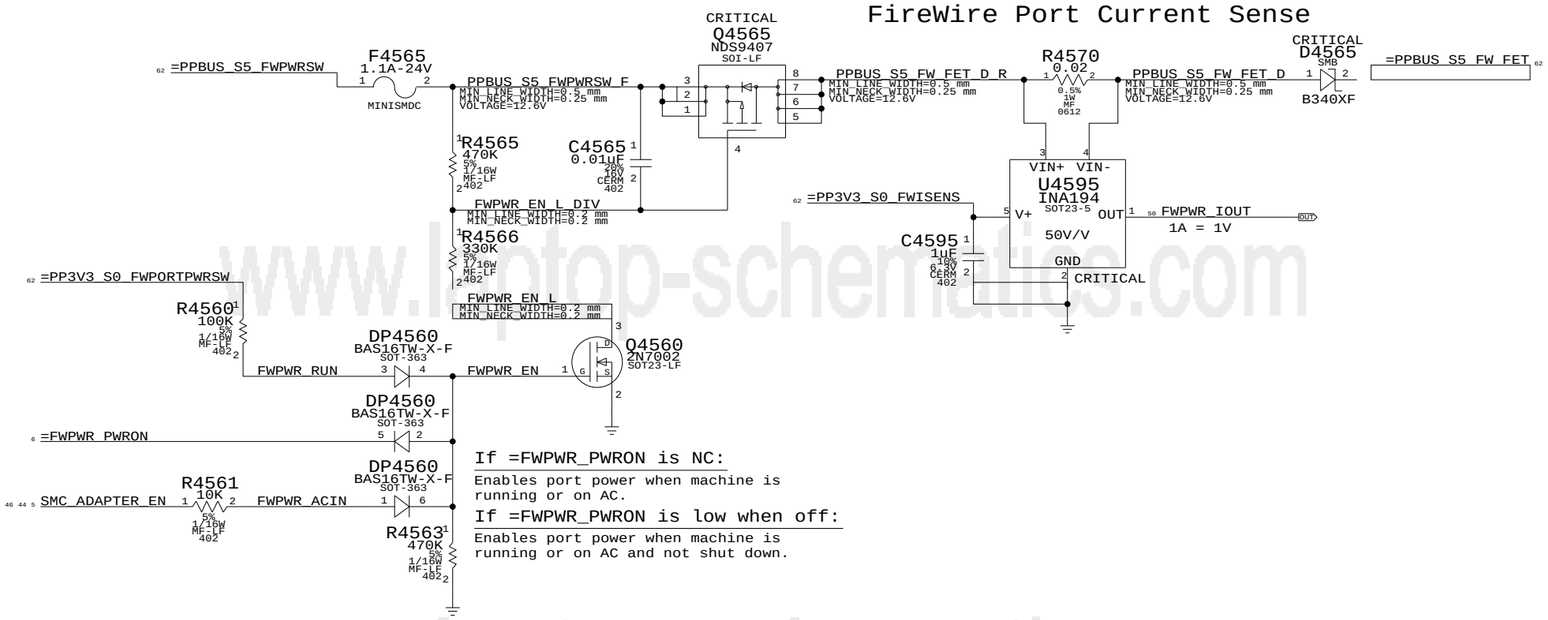
Page Notes

Power aliases required by this page:
- =PPBUS_S0_FWPWRSW (system supply for bus power)
- =PP3V3_S0_FWPORTPWRSW

Signal aliases required by this page:
- =FWPWR_PWRON (see related text note below)

BOM options provided by this page:
(NONE)

Port Power Switch



If =FWPWR_PWRON is NC:

Enables port power when machine is running or on AC.

If =FWPWR_PWRON is low when off:

Enables port power when machine is running or on AC and not shut down.

FireWire Port Current Sense

FireWire Port Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	40	81

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED BY PHY PAGE	FW	FW_110D	FW_PORT1_TPA_FL_P 41
	FW	FW_110D	FW_PORT1_TPA_FL_N 41
	FW	FW_110D	FW_PORT1_TPB_FL_P 41
	FW	FW_110D	FW_PORT1_TPB_FL_N 41

Page Notes

Power aliases required by this page:
- =PPFW_PORT1
- =PP3V3_S5_FWLATEVG
- =GND_CHASSIS_FW_PORT1

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

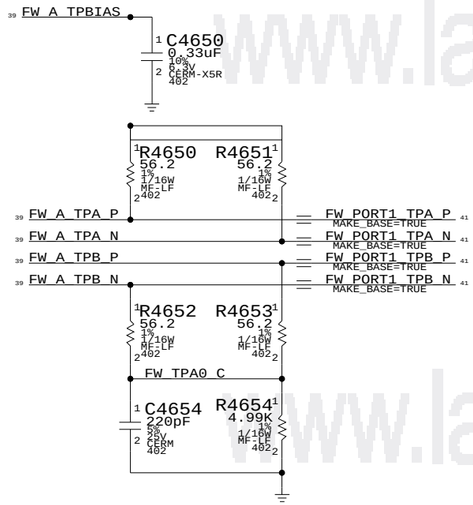
BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

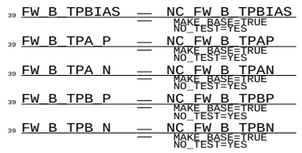
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

Termination

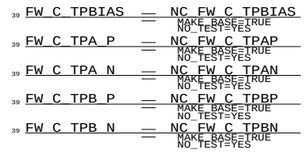
Place close to FireWire PHY



2nd TPA/TPB pair unused

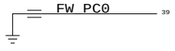


3rd TPA/TPB pair unused

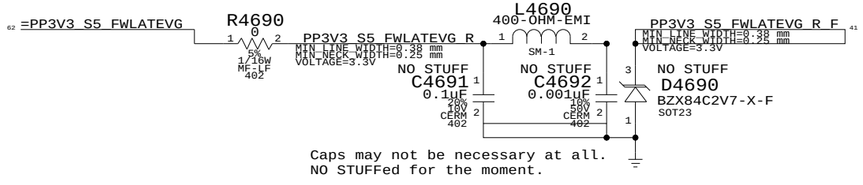


FW Power Class Strap

Single-port system sets PC=0

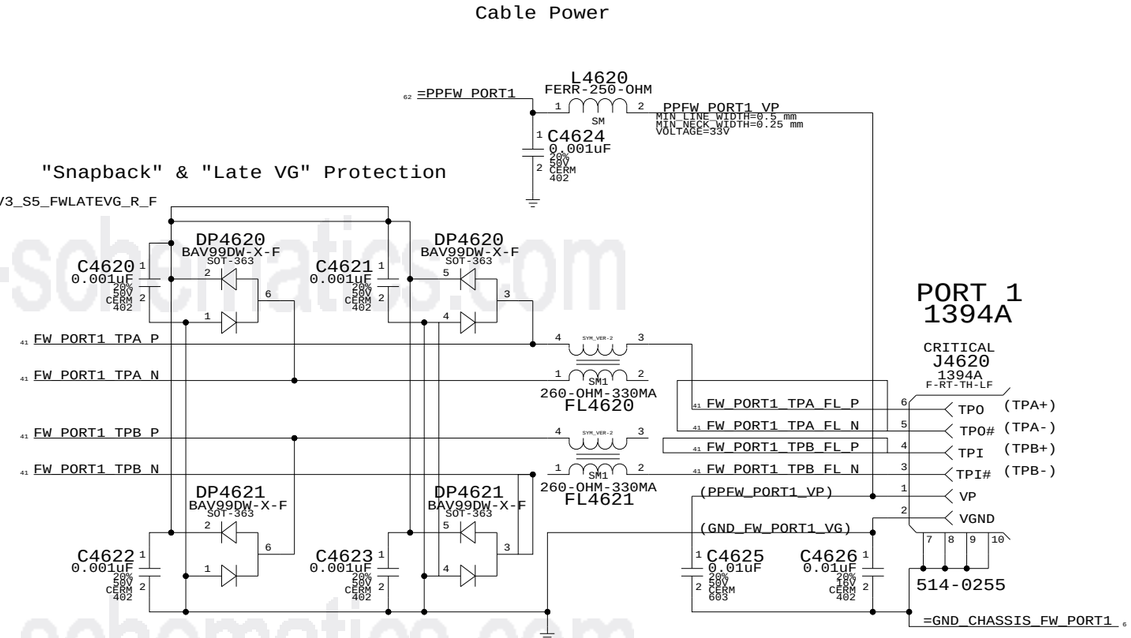


Late-VG Protection Power



Caps may not be necessary at all.
NO STUFFed for the moment.

Cable Power



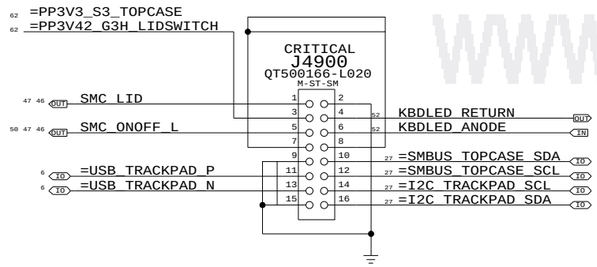
R4699 0 5% 1/16W MF-LF 402 — =GND_CHASSIS_FW_EMI 6

FireWire Ports

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

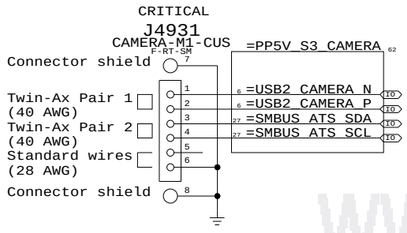
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	07001
	SCALE NONE	SHT 41 OF 81	

Top-Case Connector



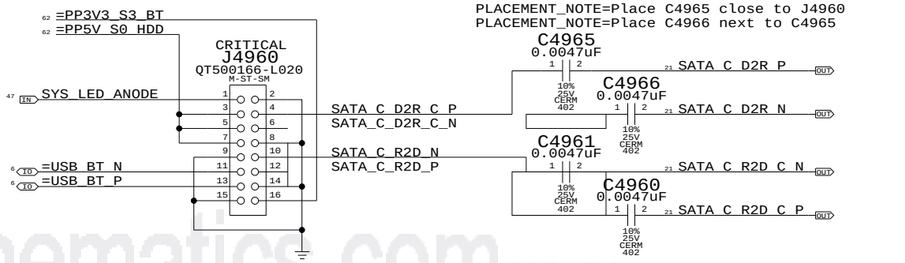
516S0350

Camera Connector



518S0371

Bluetooth (M13P) & SATA HDD Flex Connector



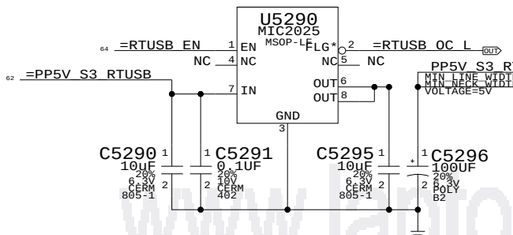
516S0350

Internal USB Connections

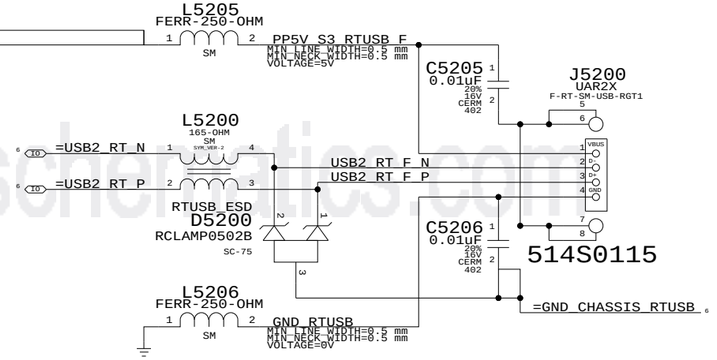
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	07001
	SCALE	SHT	OF
	NONE	42	81

Port Power Switch



Right USB Port



Place L5200, L5205 and L5206 across moat

External USB Connector

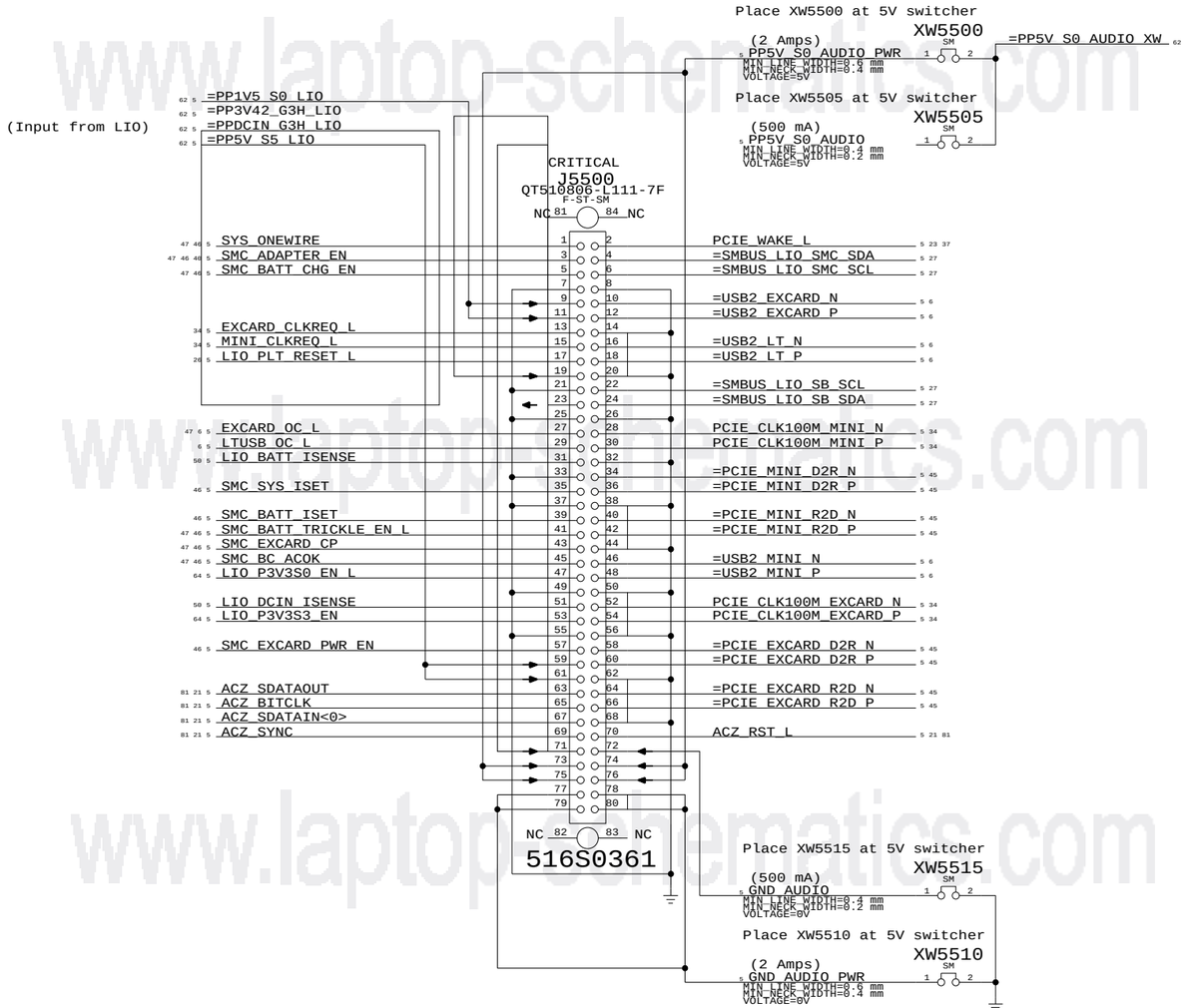
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	43	81

Left I/O Board Connector



Left I/O Board Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	44	81

PCI-E x1 Port "A" = Ethernet (Yukon)

PCI-E x1 Port "B" = PCI-E Mini Card

C5710 0.1uF 10% 16V X5R 402

C5711 0.1uF 10% 16V X5R 402 Place caps close to SB

=PCIE_MINI_R2D_P	PCIE_MINI_R2D_C_P	MAKE_BASE=TRUE	PCIE_B_R2D_C_P
=PCIE_MINI_R2D_N	PCIE_MINI_R2D_C_N	MAKE_BASE=TRUE	PCIE_B_R2D_C_N
=PCIE_MINI_D2R_P	PCIE_MINI_D2R_P	MAKE_BASE=TRUE	PCIE_B_D2R_P
=PCIE_MINI_D2R_N	PCIE_MINI_D2R_N	MAKE_BASE=TRUE	PCIE_B_D2R_N

PCI-E x1 Port "C" = ExpressCard

C5720 0.1uF 10% 16V X5R 402

C5721 0.1uF 10% 16V X5R 402 Place caps close to SB

=PCIE_EXCARD_R2D_P	PCIE_EXCARD_R2D_C_P	MAKE_BASE=TRUE	PCIE_C_R2D_C_P
=PCIE_EXCARD_R2D_N	PCIE_EXCARD_R2D_C_N	MAKE_BASE=TRUE	PCIE_C_R2D_C_N
=PCIE_EXCARD_D2R_P	PCIE_EXCARD_D2R_P	MAKE_BASE=TRUE	PCIE_C_D2R_P
=PCIE_EXCARD_D2R_N	PCIE_EXCARD_D2R_N	MAKE_BASE=TRUE	PCIE_C_D2R_N

PCI-E x1 Port "D" = Unused

TP_PCIE_D_R2DP		MAKE_BASE=TRUE	PCIE_D_R2D_C_P
TP_PCIE_D_R2DN		MAKE_BASE=TRUE	PCIE_D_R2D_C_N
TP_PCIE_D_D2RP		MAKE_BASE=TRUE	PCIE_D_D2R_P
TP_PCIE_D_D2RN		MAKE_BASE=TRUE	PCIE_D_D2R_N

PCI-E x1 Port "E" = Unused

TP_PCIE_E_R2DP		MAKE_BASE=TRUE	PCIE_E_R2D_C_P
TP_PCIE_E_R2DN		MAKE_BASE=TRUE	PCIE_E_R2D_C_N
TP_PCIE_E_D2RP		MAKE_BASE=TRUE	PCIE_E_D2R_P
TP_PCIE_E_D2RN		MAKE_BASE=TRUE	PCIE_E_D2R_N

PCI-E x1 Port "F" = Unused

TP_PCIE_F_R2DP		MAKE_BASE=TRUE	PCIE_F_R2D_C_P
TP_PCIE_F_R2DN		MAKE_BASE=TRUE	PCIE_F_R2D_C_N
TP_PCIE_F_D2RP		MAKE_BASE=TRUE	PCIE_F_D2R_P
TP_PCIE_F_D2RN		MAKE_BASE=TRUE	PCIE_F_D2R_N

PCI-E Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	45	81

UNUSED PINS HAVE THE FORMAT
SMC_XXX_WHERE XXX IS THE PORT NUMBER.
THEY ARE SET BY SOFTWARE TO BE
DRIVEN OUTPUTS ALWAYS SO THEY
CAN BE LEFT NO-CONNECTED.

OMIT
U5800
SMC_H8S2116
BGA
(1 OF 4)

PM_LAN_ENABLE	B12	P10	P60/KIN0*	L13		SMC_PM_G2_EN	
SMC_RSTGATE_L	C13	P11	P61/KIN1*	L14	47 44 40 5	SMC_ADAPTER_EN	
ALL_SYS_PWRGD	A15	P12	P62/KIN2*	L15	76 22	SPI_ARB	
RSMRST_PWRGD	B14	P13	P63/KIN3*	K12	51 22	SPI_SCLK	
SMC_SB_NMI	B15	P14	P64/KIN4*	K13	76 51 22	SPI_SI	
PM_RSMRST_L	C14	P15	P65/KIN5*	K14	76 51 22	SPI_SO	
IMVP_VR_ON	D12	P16	P66/IRQ6*/KIN6*	J12	47	SMC_PROCHOT_3_3_L	
PM_PWRBTN_L	C15	P17	P67/IRQ7*/KIN7*	J13	47	SMC_CPU_INIT_3_3_L	
SMC_P20	D13	P20	P70/AN0	N12	50	SMC_CPU_ISENSE	
SMC_P21	D14	P21	P71/AN1	R13	50	SMC_CPU_VSENSE	
SMC_P22	D15	P22	P72/AN2	P13	50	SMC_GPU_ISENSE	
SMC_P23	E12	P23	P73/AN3	R14	50	SMC_GPU_VSENSE	
SMC_BATT_TRICKLE_EN	E14	P24	P74/AN4	P14	50	SMC_DCIN_ISENSE	
SMC_BATT_CHG_EN	E15	P25	P75/AN5	R15	50	SMC_PBUS_VSENSE	
SMC_P26	E13	P26	P76/AN6	N13	50	SMC_BATT_ISENSE	
SMC_P27	F14	P27	P77/AN7	P15	50	SMC_FWIRE_ISENSE	
LPC_AD<0>	D9	P30/LAD0	P80/PME*	C7	23	SMC_WAKE_SCI_L	
LPC_AD<1>	C9	P31/LAD1	P81/GA20	A7	47	SMC_TPM_GPIO	
LPC_AD<2>	A9	P32/LAD2	P82/CLKRUN*	B7	55 48 39 23 5	PM_CLKRUN_L	
LPC_AD<3>	B9	P33/LAD3	P83/LPCPD*	D6	55 48 23 5	PM_SUS_STAT_L	
LPC_FRAME_L	D8	P34/LFRAME*	P84/IRQ3*/TXD1	C6	47	SC_TX_L	
SMC_LRESET_L	C8	P35/LRESET*	P85/IRQ4*/RXD1	A6	47	SC_RX_L	
PCI_CLK_SMC	A8	P36/LCLK	P86/IRQ5*/SCK1/SCL1	B6	27	SMB_BSB_CLK	
INT_SERIRQ	D7	P37/SERIRQ	P90/IRQ2*	K4	50 47 42	SMC_ONOFF_L	
SMC_XDP_TMS_L	A5	P40/TMI0	P91/IRQ1*	J2	47 44 5	SMC_BC_ACOK	
SMC_XDP_TDI_L	B5	P41/TMO0	P92/IRQ0*	J1	63 47 5	SMC_BS_ALRT_L	
SMB_BSB_DATA	D5	P42/SDA1	P93/IRQ12*	J3	64 23	PM_SLP_S3_L	
SMC_TPM_PP	C3	P43/TMI1/EXSCK1	P94/IRQ13*	J4	64 23	PM_SLP_S4_L	
SMC_XDP_TRST_L	B1	P44/TMO1	P95/IRQ14*	H2	23	PM_SLP_S5_L	
SMC_XDP_TCK	C2	P45	P96/EXCL	H1	35	SMC_SUS_CLK	
SMC_SYS_LED	D3	P46/PWX0/PWM0	P97/IRQ15*/SDA0	G2	27	SMC_SMB_0_DATA	
SMC_SYS_KBDLED	C1	P47/PWX1/PWM1					
SMC_TX_L	G1	P50					
SMC_RX_L	G4	P51					
SMC_SMB_0_CLK	F2	P52/SCL0					

OMIT
U5800
SMC_H8S2116
BGA
(2 OF 4)

SMC_RCIN_L	R3	PA0/KIN8*/PA2PC	PE0	M3	47	SMC_CASE_OPEN	
BOOT_LPC_SPI_L	P3	PA1/KIN9*/PA2DD	PE1*/ETCK	M2	48 47 5	SMC_TCK	
PM_SYSRST_L	R2	PA2/KIN10*/PS2AC	PE2*/ETDI	M1	48 47 5	SMC_TDI	
SMC_TPM_RESET_L	N3	PA3/KIN11*/PS2AD	PE3*/ETDO	L4	48 47 5	SMC_TDO	
PM_EXTTS_L<0>	R1	PA4/KIN12*/PS2BC	PE4*/ETMS	L2	48 47 5	SMC_TMS	
PM_THRM_L	N2	PA5/KIN13*/PS2BD	PF0/IRQ8*/PWM2	M7		SMC_PF0	47
SYS_ONEWIRE	M4	PA6/KIN14*/PS2CC	PF1/IRQ9*/PWM3	P6		SMC_PF1	47
PM_BATLOW_L	N1	PA7/KIN15*/PS2CD	PF2/IRQ10*/TMOY	R6	47 42	SMC_LID	
SMC_EXTSMI_L	B10	PB0/LSMI*	PF3/IRQ11*/TMOX	N6	47	SMC_CPU_RESET_3_3_L	
SMC_RUNTIME_SCI_L	A10	PB1/LSCI	PF4/PWM4	M6	44 5	SMC_BATT_ISET	
SMC_ODD_DETECT	D10	PB2	PF5/PWM5	R5	47	SMC_BATT_VSET	
ISENSE_CAL_EN	A11	PB3	PF6/PWM6	P5	44 5	SMC_SYS_ISET	
SMC_EXCARD_CP	B11	PB4	PF7/PWM7	N5	47	SMC_SYS_VSET	
SMC_EXCARD_PWR_EN	C11	PB5	PG0/EXIRQ8*/TMIX	P9	76 51 22	SPI_CE_L	
SMC_EXCARD_PWR_OC_L	A12	PB6	PG1/EXIRQ9*/TMIY	R9	76	SMC_XDP_TCK_3_3	
SMC_XDP_TDO_3_3_L	D11	PB7	PG2/EXIRQ10*/SDA2	N9	27	SMB_BSA_DATA	
SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*	PG3/EXIRQ11*/SCL2	P8	27	SMB_BSA_CLK	
SMC_FAN_1_CTL	G15	PC1/TIOCB0/WUE9*	PG4/EXIRQ12*/EXSDAA	R8	27	SMB_A_S3_DATA	
SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*	PG5/EXIRQ13*/EXSCLA	M8	27	SMB_A_S3_CLK	
SMC_FAN_3_CTL	G12	PC3/TIOCD0/TCLKB/WUE11*	PG6/EXIRQ14*/EXSDAB	P7	27	SMB_B_S0_DATA	
SMC_FAN_0_TACH	H14	PC4/TIOCA1/WUE12*	PG7/EXIRQ15*/EXSCLB	R7	27	SMB_B_S0_CLK	
SMC_FAN_1_TACH	H15	PC5/TIOCB1/TCLKC/WUE13*	PH0/EXIRQ6*	E1	47	SMC_PROCHOT	
SMC_FAN_2_TACH	H13	PC6/TIOCA2/WUE14*	PH1/EXIRQ7*	F3	47	SMC_THRMTRIP	
SMC_FAN_3_TACH	H12	PC7/TIOCB2/TCLKD/WUE15*	PH2/FWE	K2	47	SMC_FWE	
SMS_X_AXIS	M11	PD0/AN8	PH3/EXEXCL	C4	52	ALS_GAIN	
SMS_Y_AXIS	P11	PD1/AN9	PH4	D4	47 23	SMS_INT_L	
SMS_Z_AXIS	R11	PD2/AN10	PH5	B3	54	SMS_ONOFF_L	
SMC_ANALOG_ID	N11	PD3/AN11					
SMC_NB_ISENSE	P10	PD4/AN12					
SMC_MEM_ISENSE	R10	PD5/AN13					
ALS_LEFT	N10	PD6/AN14					
ALS_RIGHT	M10	PD7/AN15					

OMIT
U5800
SMC_H8S2116
BGA
(4 OF 4)

G3	NC0	NC12	E15
H3	NC1	NC13	A14
K3	NC2	NC14	C12
L3	NC3	NC15	C10
N4	NC4	NC16	C5
M5	NC5	NC17	A3
N7	NC6	NC18	B8
M12	NC7	NC19	E4
M13	NC8	NC20	H4
L12	NC9	NC21	M9
K15	NC10	NC22	N8
J14	NC11		

LAYOUT NOTE:
PLACE C5807 NEAR RIN F1

=PP3V3_S5_SMC
C5802 22UF 20% 6.3V X5R 805
C5803 0.1UF 20% 10V CERM 402
C5804 0.1UF 20% 10V CERM 402
C5805 0.1UF 20% 10V CERM 402
C5806 0.1UF 20% 10V CERM 402

SMC_VCL
C5807 0.47UF 20% 6.3V CERM-X5R 402

LAYOUT NOTE:
PLACE R5899 AND C5820 NEAR SMC PIN N14,N15

VCL IS INTERNAL RAIL

=PP3V3_S5_SMC
R5899 4.7 5% 1/10W MF 402
PP3V3_AVCC_SMC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.20 MM
C5820 0.1UF 20% 10V CERM 402
GND_SMC_AVSS

PP3V3_AVREF_SMC
=PP3V3_S5_SMC
R5809 10K 5% 1/16W MF 402
R5801 10K 5% 1/16W MF 402

OMIT
U5800
SMC_H8S2116
BGA
(3 OF 4)

SMC_RST_L
SMC_XTAL
SMC_EXTAL
KBC_MDE
SMC_MD1
SMC_NMI
SMC_TRST_L
NOSTUFF
R5898 10K 5% 1/16W MF 402
R5803 10K 5% 1/16W MF 402
R5802 10K 5% 1/16W MF 402

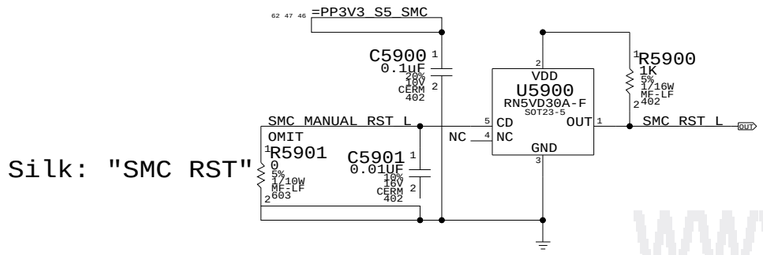
XW5800
SM
GND_SMC_AVSS

SMC

APPLE COMPUTER INC.

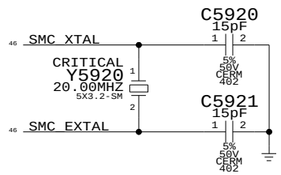
SIZE	DRAWING NUMBER	REV.
D	051-6941	07001
SCALE: NONE	SHT 46 OF 81	

SMC Reset Button / Brownout Detect

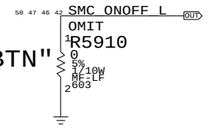


Silk: "SMC RST"

SMC Crystal Circuit

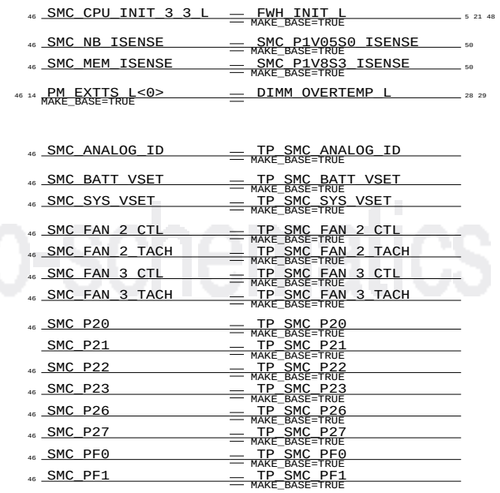


Debug Power Button

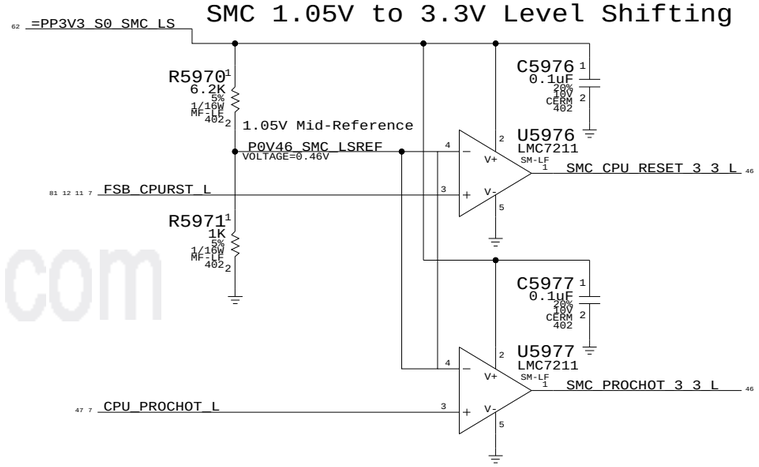


Silk: "PWR BTN"

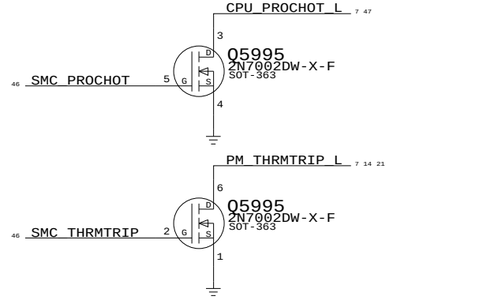
SMC CPU Init / Memory Signals



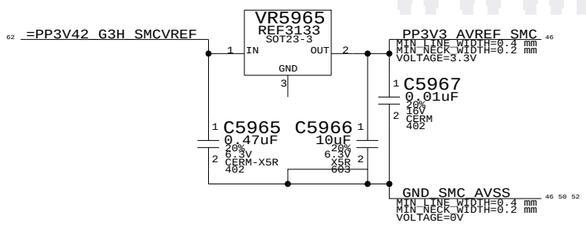
SMC 1.05V to 3.3V Level Shifting



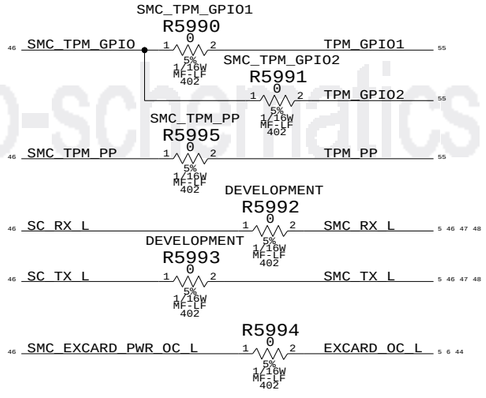
SMC 3.3V to 1.05V Level Shifting



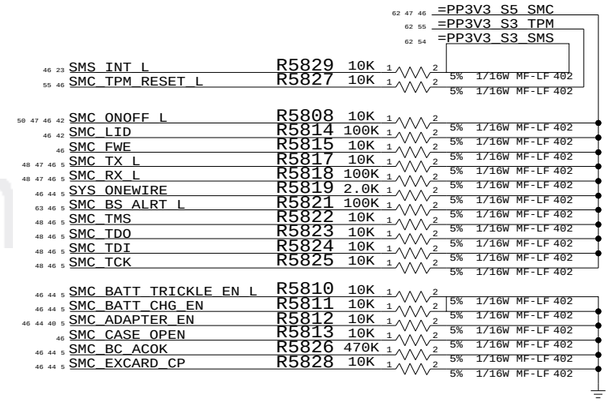
SMC AVREF Supply



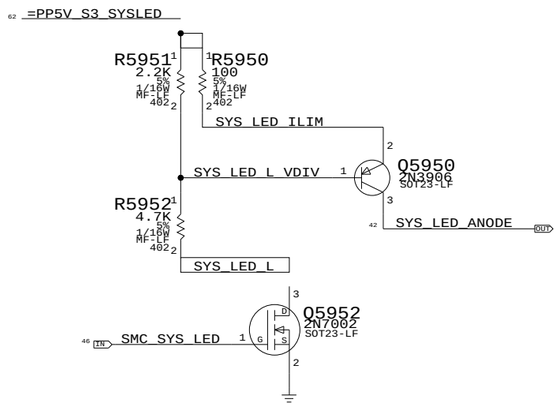
SMC TPM / Development Signals



SMC Support Pull-ups

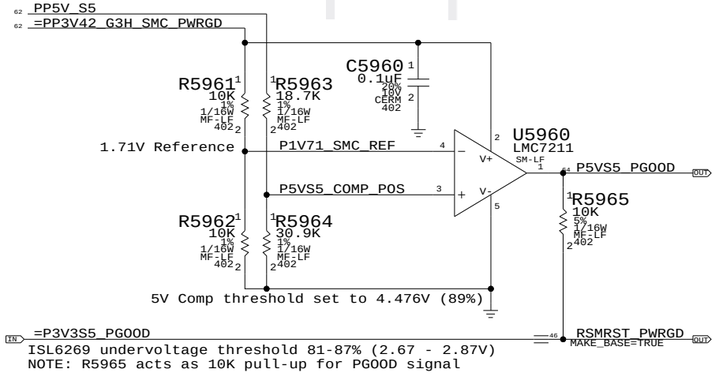


System (Sleep) LED Circuit



SMC PWRGD Circuit

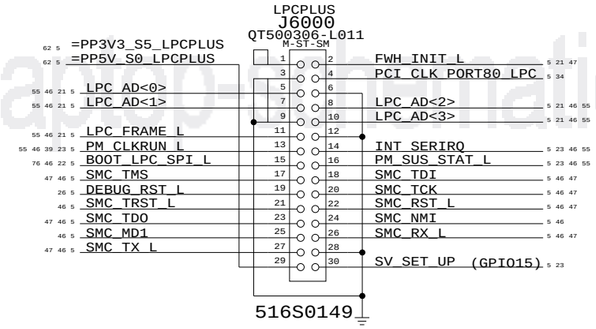
Reports when 5V S5 and 3.3V S5 are in regulation



SMC Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	07001
	SCALE: NONE	SHT 47 OF 81	



LPC+ Debug Connector

SYNC_MASTER=M42 SYNC_DATE=07/20/2005

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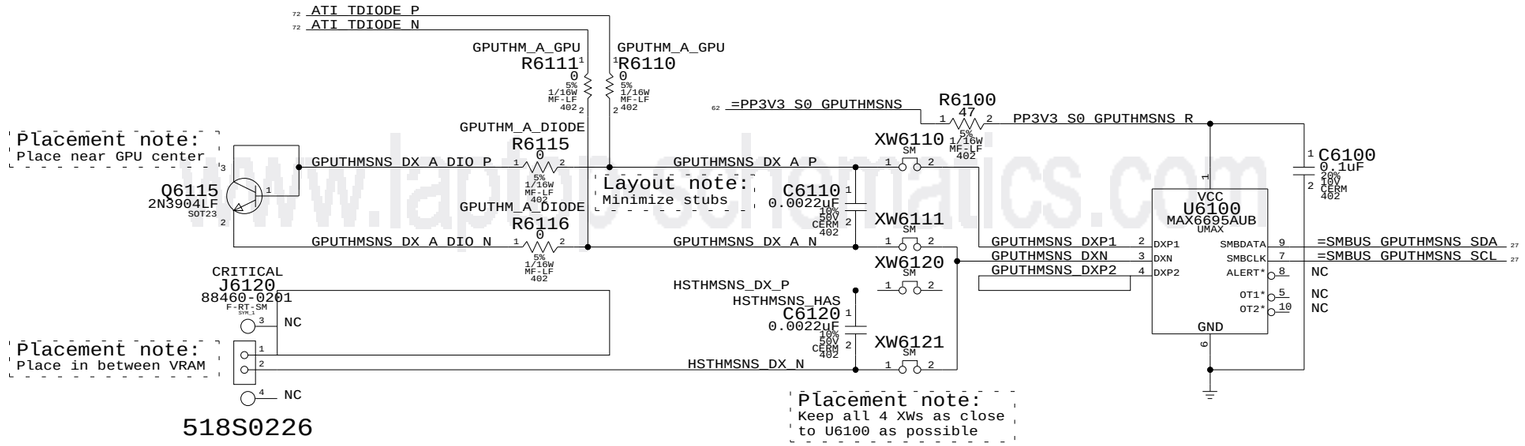
SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

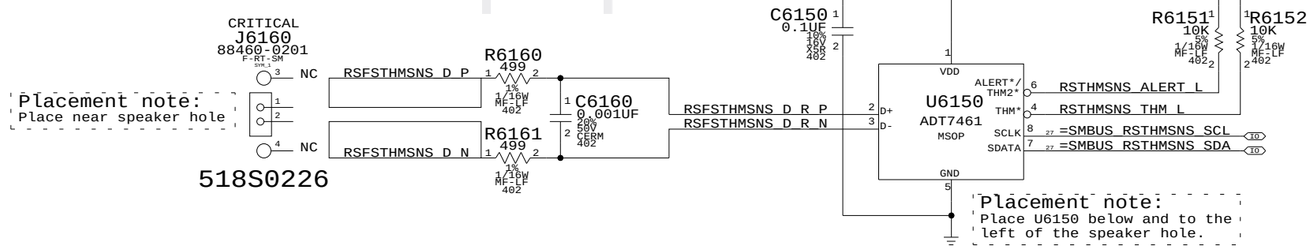
SCALE	SHT	OF
NONE	48	81

GPU / Heat Pipe Thermal Sensor

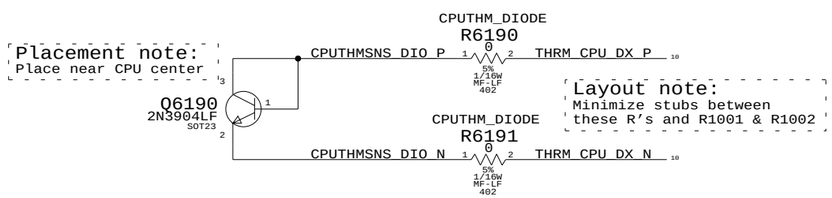


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,0,1/16W,0402	C6120		HSTHMSNS_NOT

Right-Side/Fin Stack Thermal Sensor



CPU Back-Up Thermal Diode



R1001 / R1002 are not currently BOMOPTIONed. Can not programatically unstuff those parts to stuff these.

Thermal Sensors

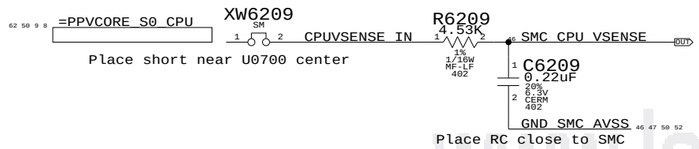
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

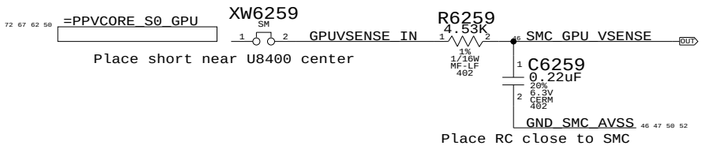
SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	49	81

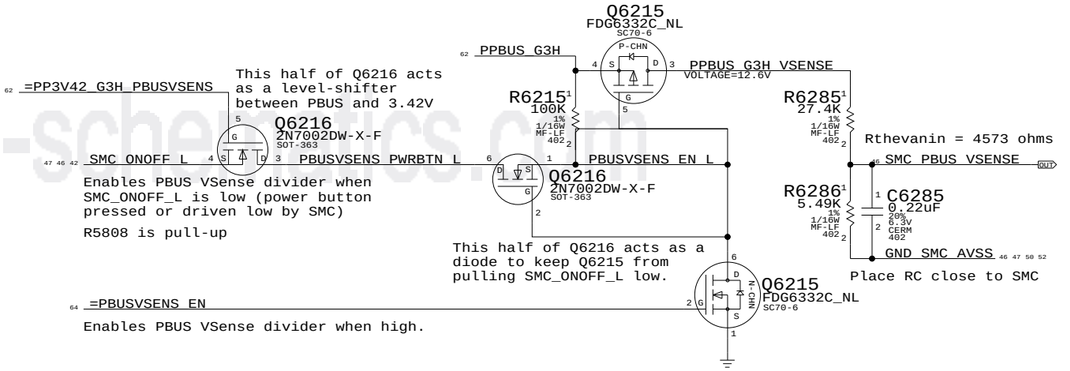
CPU Voltage Sense / Filter



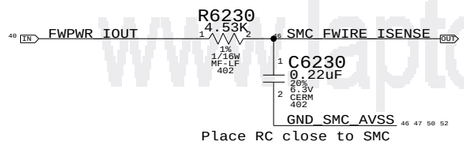
GPU Voltage Sense / Filter



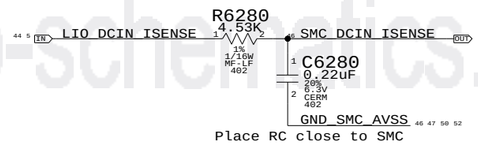
PBUS Voltage Sense Enable & Filter



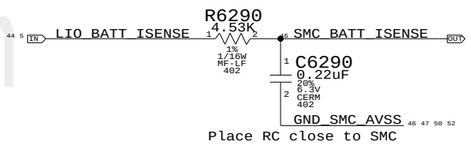
FireWire Current Sense Filter



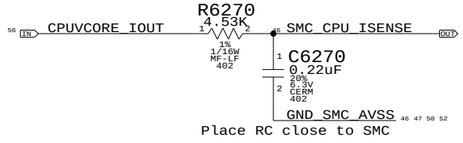
DCIN Current Sense Filter



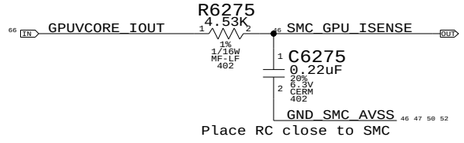
Battery Current Sense Filter



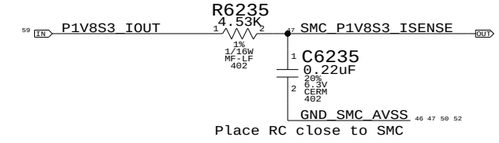
CPU Current Sense Filter



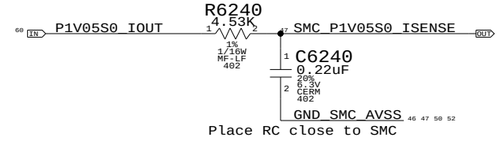
GPU Current Sense Filter



1.8V S3 (Memory) Current Sense Filter

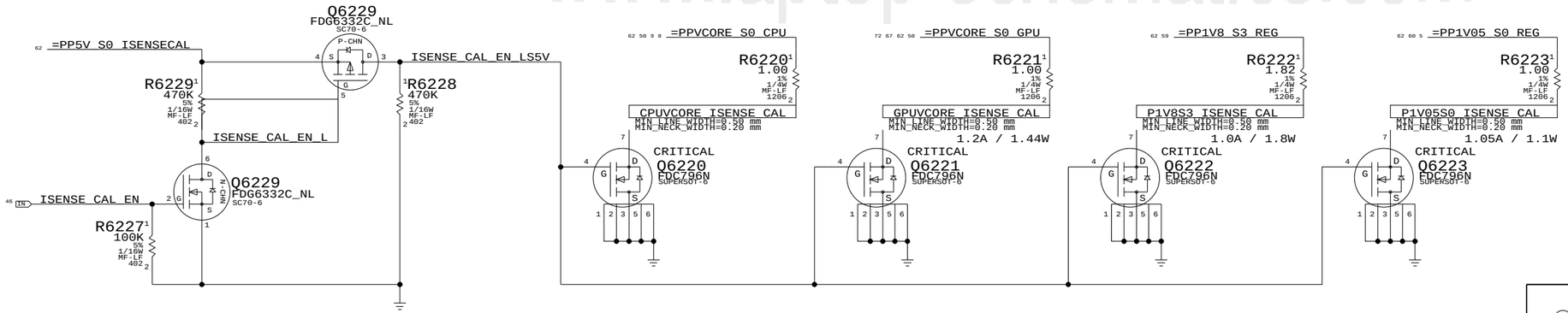


1.05V S0 (NB) Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



Current & Voltage Sensing

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
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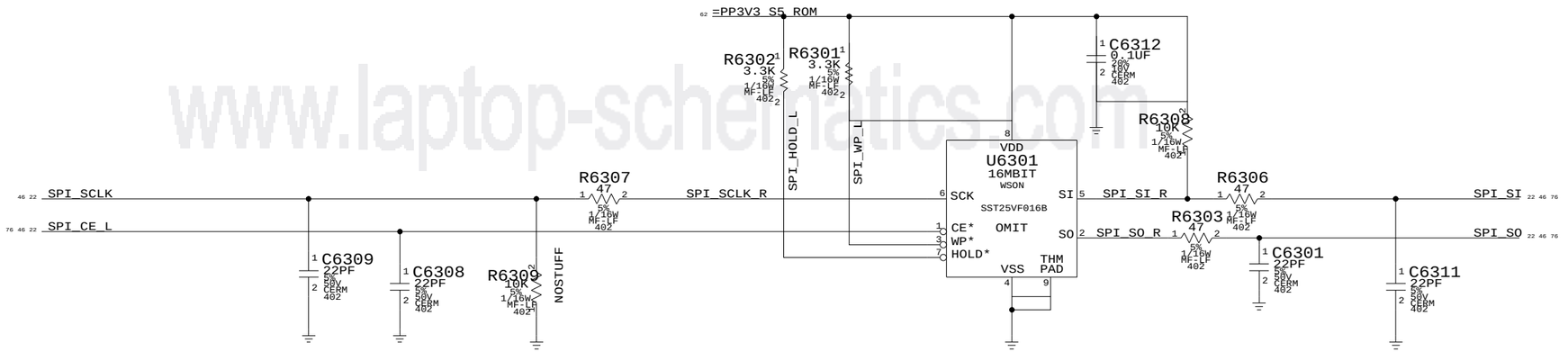
SCALE	SHT	OF
NONE	50	81



R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M

R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

SPI BOOTROM

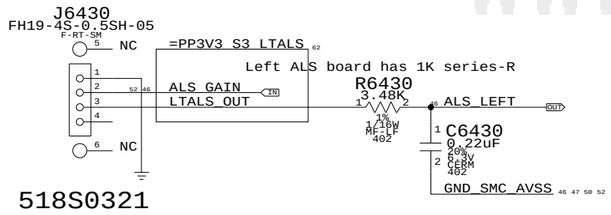
SYNC_MASTER=(M42) SYNC_DATE=07/26/2005

APPLE COMPUTER INC.

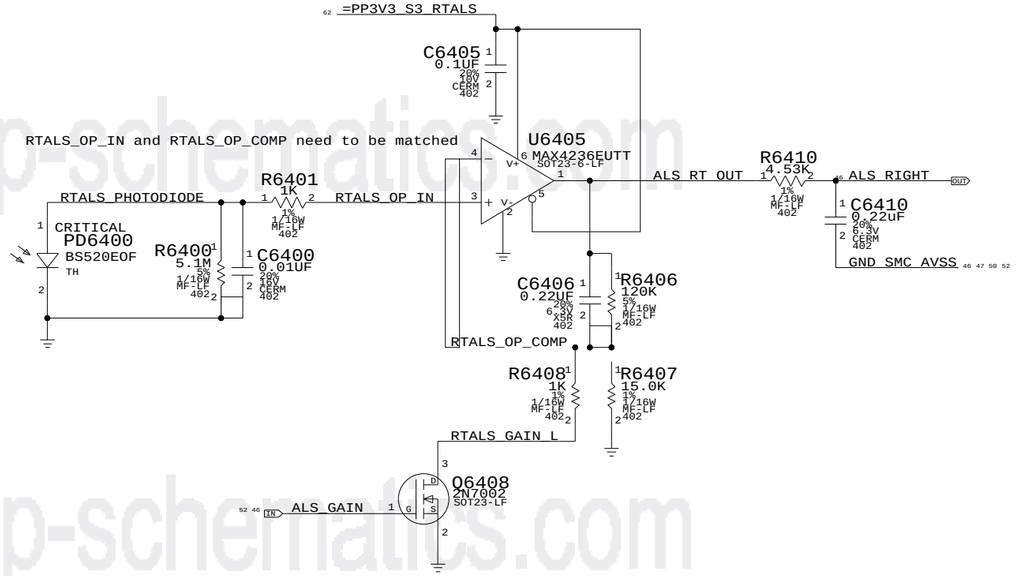
SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	51	81

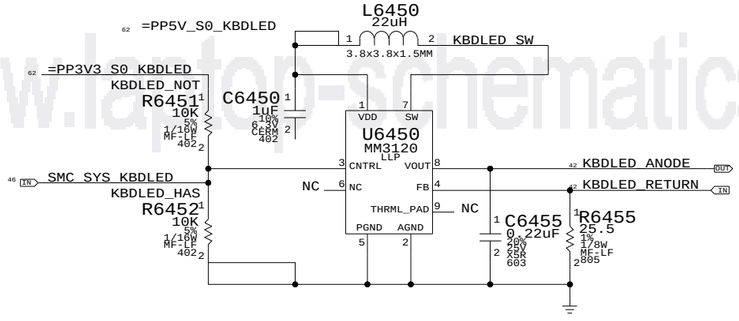
Left ALS "Connector"



Right ALS Circuit



Keyboard LED Driver



ALS Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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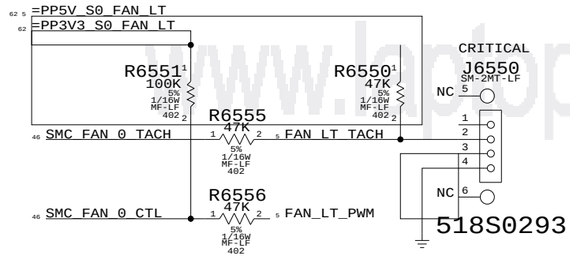
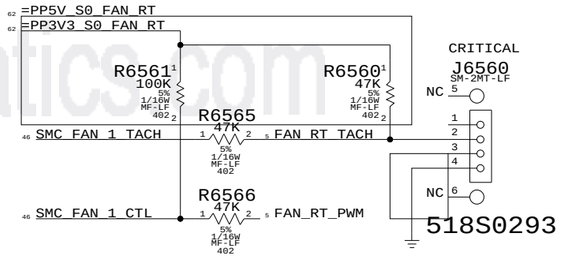
SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	52	81

Left Fan



Right Fan



Fan Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	53	81

PAGE NOTES

INPUT

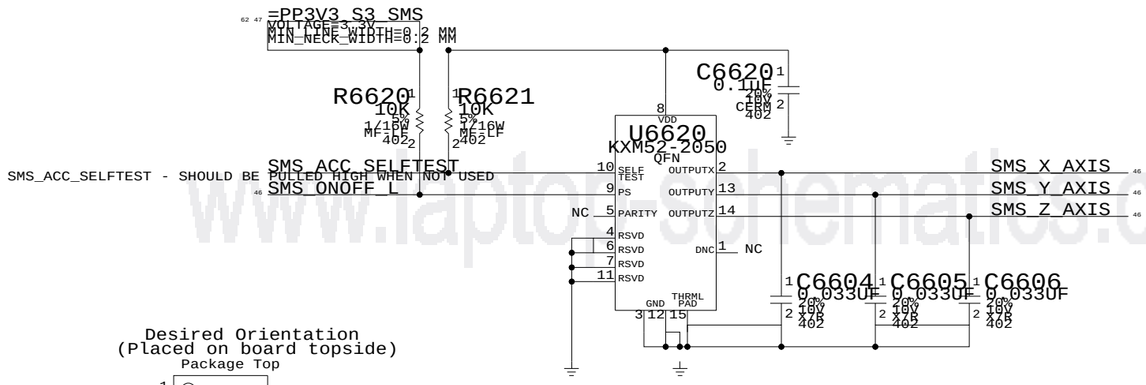
=PP3V3_S3_SMS - 3.3V POWER FOR SMS (STAYS ALIVE IN SLEEP)
SMS_ONOFF_L - CONNECT TO SMC TO BE ABLE TO PUT SMS INTO LOW-POWER MODE

OUTPUT

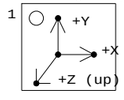
SMS_ACC_*_AXIS - ACCELEROMETER OUTPUT TO SCU

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
7/26/2005 - REMOVED BOM TABLE AND UPDATED SYMBOL TO KXM52-2050
7/26/2005 - CONNECTED PD PIN TO SMC'S SMS_ONOFF_L
7/26/2005 -



Desired Orientation
(Placed on board topside)



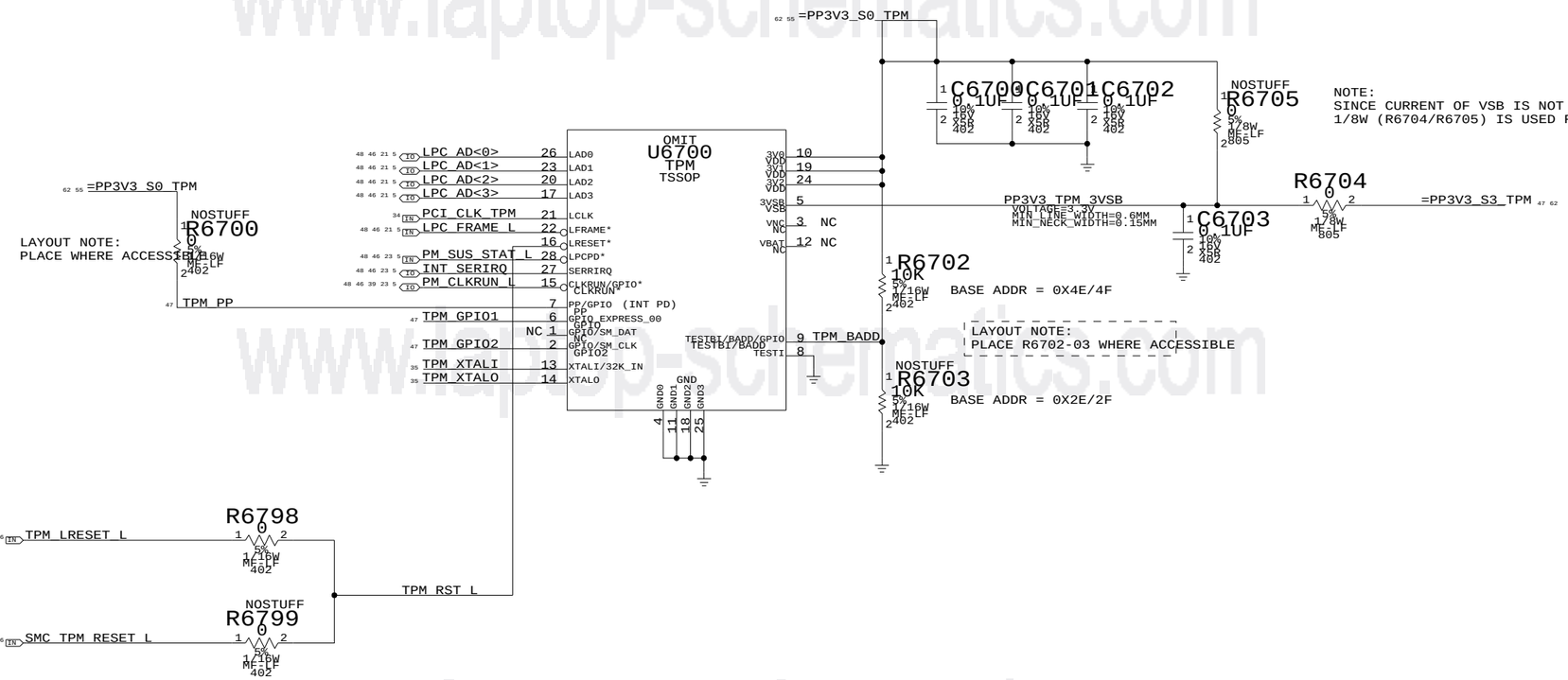
SMS

SYNC_MASTER=(M42) SYNC_DATE=07/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	54	81



TPM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	55	81

DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	1	0	1-Phase	DCM

=PPVOUT_S0_IMVP6_REG
Vout = Variable
36A max output
(Inductors limit)

These caps for Q7500

These caps for Q7550

CPU VCore Current Sense

Vout = Gain * ((2.1 mV/A * Iload) + Voffset)
Voffset = (Vdrp_offset * Kdroop) + Vamp_offset
Gain = Rc / (Ra + Rb)
Voffset worst-case ~2.3mV (+/- ~1A offset)
Vout @ 36A = 2.44V-2.60V

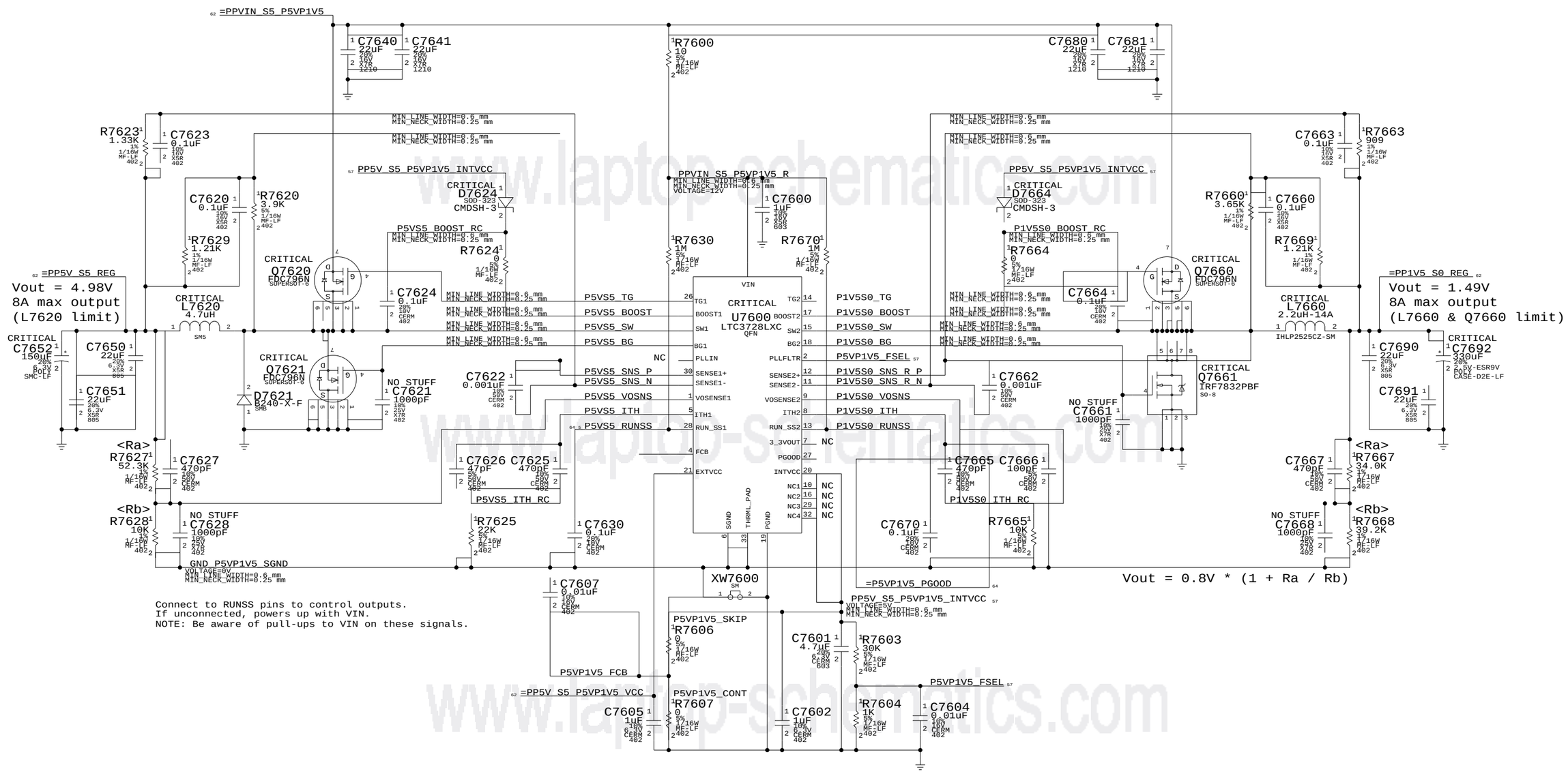
IMVP6 CPU VCore Regulator

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	56	81



5V / 1.5V Power Supply

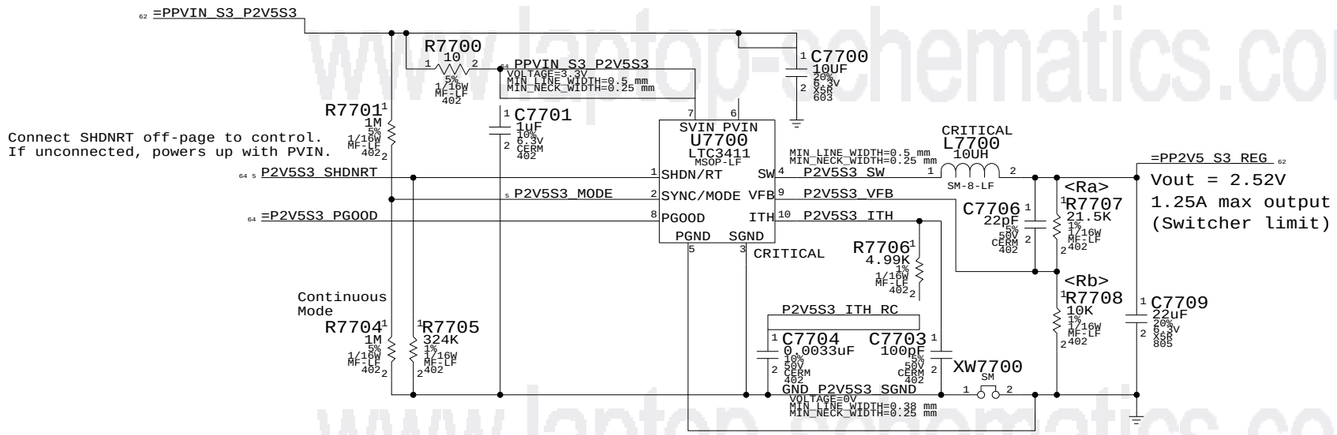
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

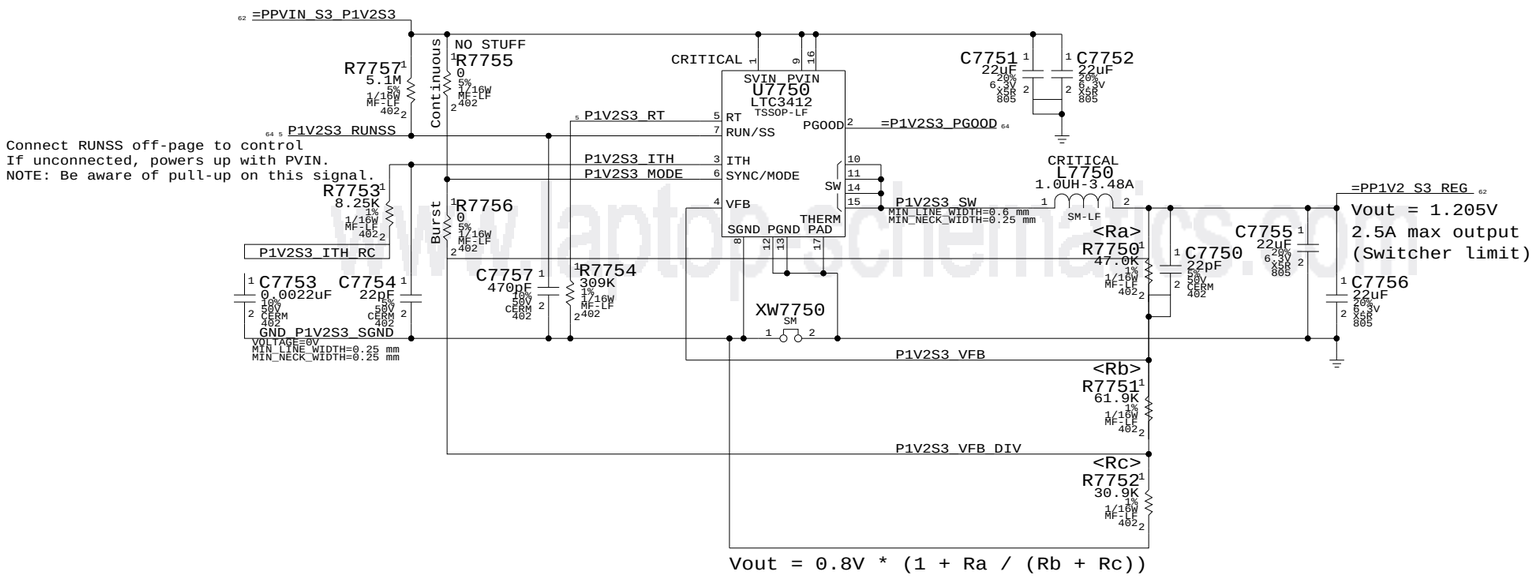
SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	57	81

2.5V S3 Regulator



1.2V S3 Regulator



2.5V & 1.2V Regulators

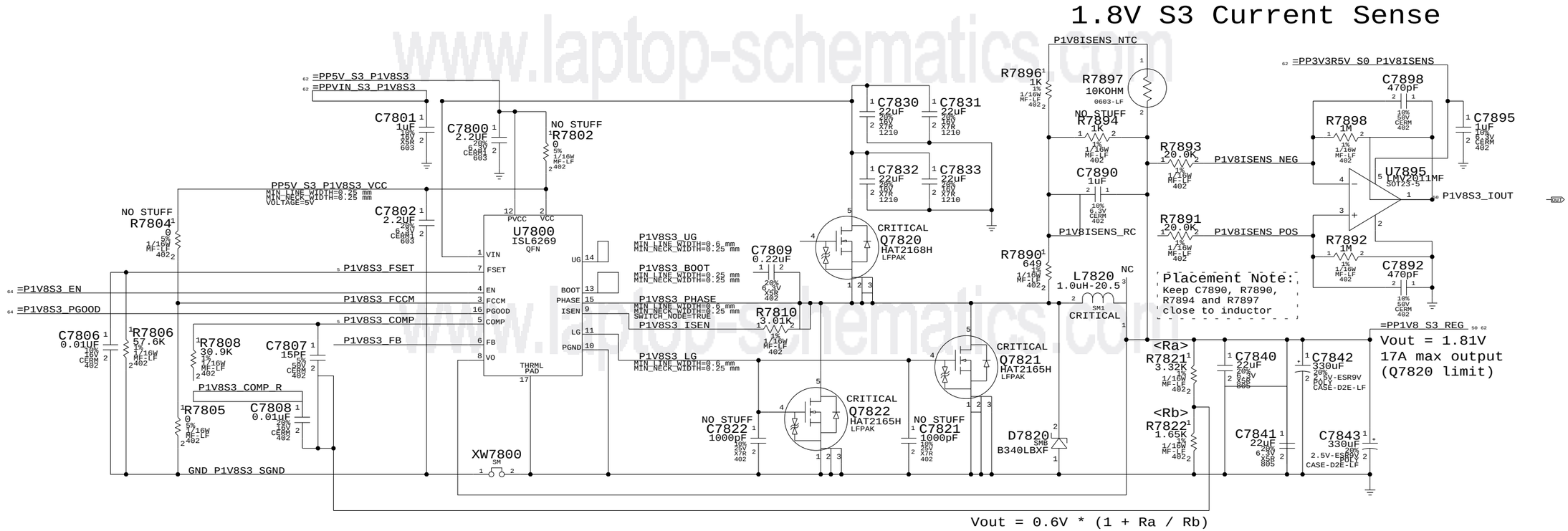
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	58	81

1.8V S3 Current Sense



1.8V Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	59	81

3.3V S5 Regulator

=PP5V_S5_P3V3S5
=PPVIN_S5_P3V3S5
C7901 1uF 10% 16V X5R 603
C7900 2.2UF 20% 6.3V CERM 603
NO STUFF R7902 0 5% 1/16W MF-LF 402
C7930 22uF 20% 16V X5R 1210
PP5V_S5_P3V3S5_VCC
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
NO STUFF R7904 0 5% 1/16W MF-LF 402
C7902 2.2UF 20% 6.3V CERM 603
U7900 ISL6269 QFN
PVCC VCC
VIN FSET EN FCCM PGOOD COMP VO THRML PAD UG BOOT PHASE ISEN LG PGND
CRITICAL Q7920 FDC796N SUPERSOT-6
P3V3S5_UG
P3V3S5_BOOT
P3V3S5_PHASE
P3V3S5_ISEN
C7909 0.22uF 20% 6.3V CERM 402
R7910 3.01K 1% 1/16W MF-LF 402
CRITICAL Q7921 FDC796N SUPERSOT-6
P3V3S5_LG
NO STUFF C7921 1000pF 10% 25V X7R 402
D7920 SMB MBRS140XXG
CRITICAL L7920 4.7uH IHLP
=P3V3S5_EN
=P3V3S5_PGOOD
R7949 0 5% 1/16W MF-LF 402
P3V3S5_FSET
P3V3S5_EN_RC
P3V3S5_FCCM
P3V3S5_COMP
P3V3S5_FB
C7906 0.01UF 10% 16V CERM 402
R7906 57.6K 1% 1/16W MF-LF 402
R7908 51.1K 1% 1/16W MF-LF 402
C7907 470PF 10% 50V CERM 402
P3V3S5_COMP_R
R7905 0 5% 1/16W MF-LF 402
C7908 0.022UF 10% 16V CERM-X5R 402
NO STUFF C7949 0.01UF 10% 16V CERM 402
XW7900 SM
GND_P3V3S5_SGND
<Ra> R7921 3.32K 1% 1/16W MF-LF 402
<Rb> R7922 732 1% 1/16W MF-LF 402
C7920 0.0047uF 10% 25V CERM 402
P3V3S5_FB_RC
R7920 0 5% 1/16W MF-LF 402
C7940 22uF 20% 6.3V X5R 805
C7941 22uF 20% 6.3V X5R 805
=PP3V3_S5_REG
Vout = 3.32V
4.5A max output
(L7920 limit)
C7942 150uF 20% 6.3V POLY SMC-LF

Vout = 0.6V * (1 + Ra / Rb)

1.05V Current Sense

1.05V S0 Regulator

=PP5V_S0_P1V05S0
=PPVIN_S0_P1V05S0
C7951 1uF 10% 16V X5R 603
C7950 2.2UF 20% 6.3V CERM 603
NO STUFF R7952 0 5% 1/16W MF-LF 402
C7980 22uF 20% 16V X7R 1210
C7981 22uF 20% 16V X7R 1210
C7982 22uF 20% 16V X7R 1210
PP5V_S0_P1V05S0_VCC
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
NO STUFF R7954 0 5% 1/16W MF-LF 402
C7952 2.2UF 20% 6.3V CERM 603
U7950 ISL6269 QFN
PVCC VCC
VIN FSET EN FCCM PGOOD COMP VO THRML PAD UG BOOT PHASE ISEN LG PGND
CRITICAL Q7970 FDC796N SUPERSOT-6
P1V05S0_UG
P1V05S0_BOOT
P1V05S0_PHASE
P1V05S0_ISEN
C7959 0.22uF 20% 6.3V CERM 402
R7960 2.8K 1% 1/16W MF-LF 402
CRITICAL Q7971 IRF7832PBF SO-8
P1V05S0_LG
NO STUFF C7971 1000pF 10% 25V X7R 402
CRITICAL L7970 1.53uH SM
NC
=P1V05S0_EN
=P1V05S0_PGOOD
P1V05S0_FSET
P1V05S0_FCCM
P1V05S0_COMP
P1V05S0_FB
C7956 0.01UF 10% 16V CERM 402
R7956 57.6K 1% 1/16W MF-LF 402
R7958 30.9K 1% 1/16W MF-LF 402
C7957 15PF 5% 50V CERM 402
P1V05S0_COMP_R
R7955 0 5% 1/16W MF-LF 402
C7958 0.01UF 20% 16V CERM 402
XW7950 SM
GND_P1V05S0_SGND
P1V05ISENS_NTC
R7996 1K 1% 1/16W MF-LF 402
R7997 10KOHM 0603-LF
NO STUFF R7994 1K 1% 1/16W MF-LF 402
C7990 1uF 10% 6.3V CERM 402
P1V05ISENS_RC
R7990 649 1% 1/16W MF-LF 402
R7993 20.0K 1% 1/16W MF-LF 402
P1V05ISENS_NEG
R7991 20.0K 1% 1/16W MF-LF 402
P1V05ISENS_POS
=PP3V3R5V_S0_P1V05ISENS
C7998 470PF 10% 50V CERM 402
R7998 1M 1% 1/16W MF-LF 402
C7995 1uF 10% 6.3V CERM 402
U7995 LMV2011MF SOT23-5
P1V05S0_IOUT
R7992 1M 1% 1/16W MF-LF 402
C7992 470PF 10% 50V CERM 402
Placement Note:
Keep C7990, R7990, R7994 and R7997 close to inductor
<Ra> R7971 3.32K 1% 1/16W MF-LF 402
<Rb> R7972 4.42K 1% 1/16W MF-LF 402
C7985 22uF 20% 6.3V X5R 805
C7986 22uF 20% 6.3V X5R 805
=PP1V05_S0_REG
Vout = 1.05V
10A max output
(Q7970 & L7970 limit)
C7989 330uF 20% 2V POLY CASE-D2E-LF

Vout = 0.6V * (1 + Ra / Rb)

3.3V / 1.05V Power Supplies

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

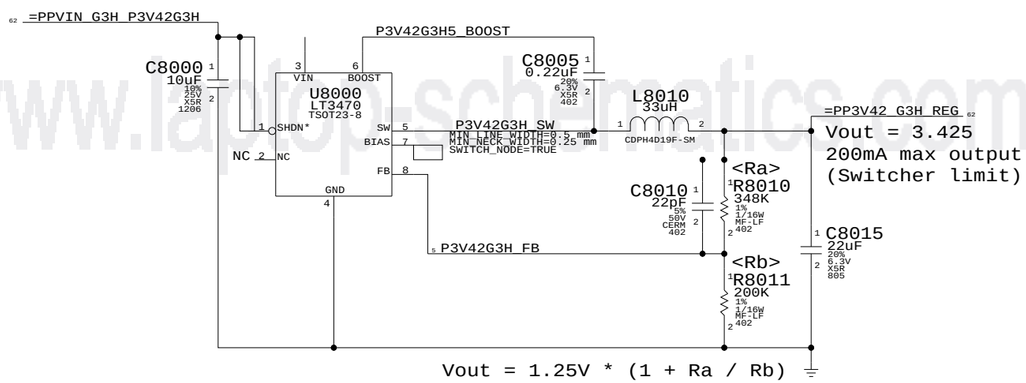
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	60	81

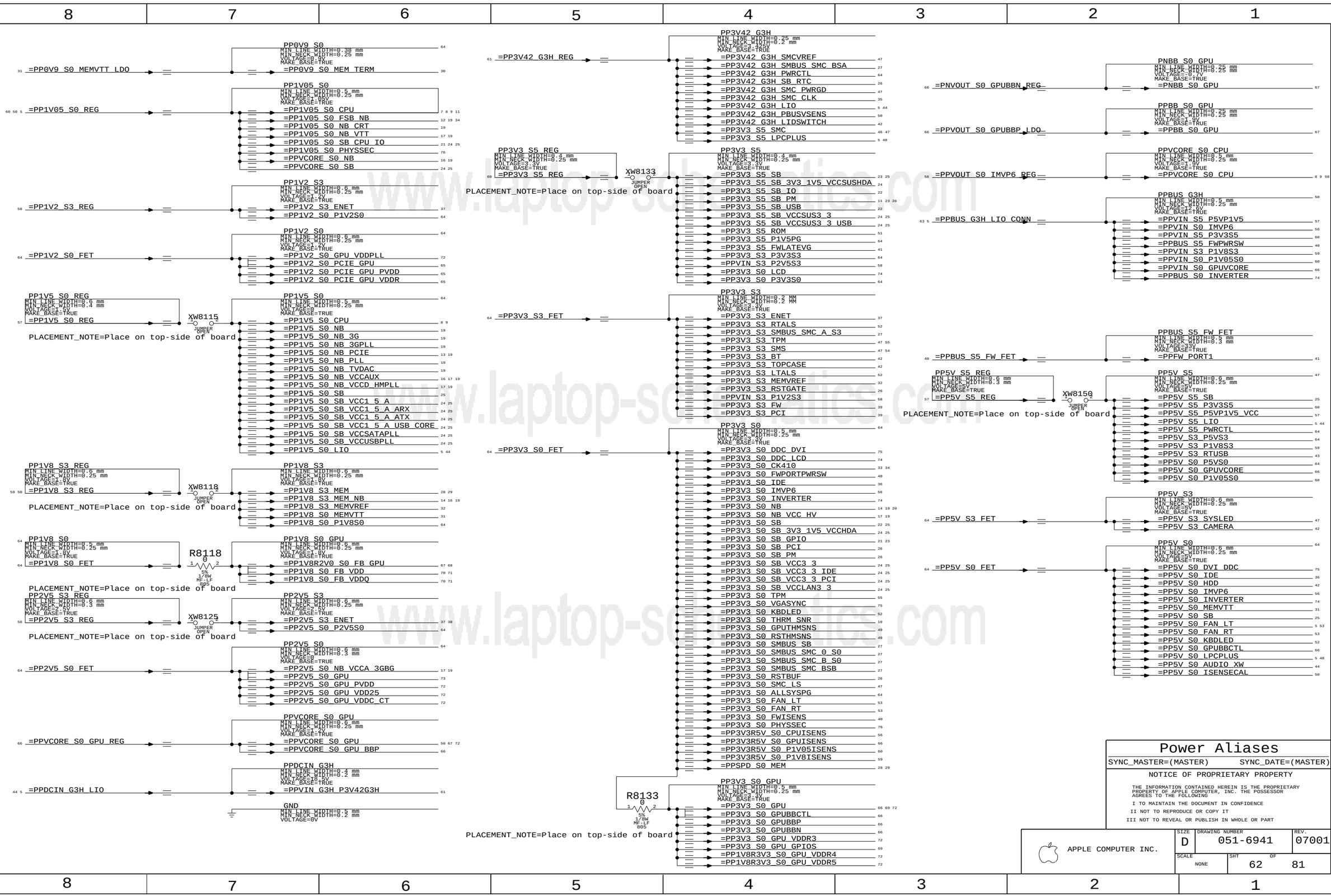
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

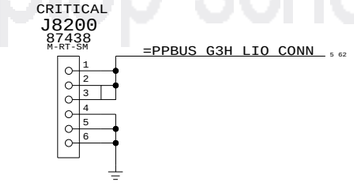


3.3V G3Hot Supply	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)

APPLE COMPUTER INC.	SIZE: D	DRAWING NUMBER: 051-6941	REV: 07001
	SCALE: NONE	SHT: 61	OF: 81

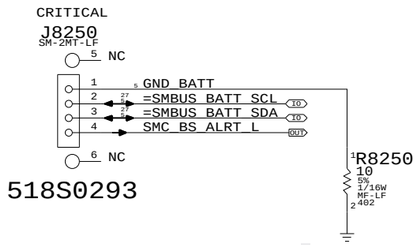


Left I/O Power Connector



518S0368

Battery Connector (Digital Signals)



518S0293

PBus-In & Battery Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	63	81

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

5V S3 FET

Q8300 FDC638P SM-LF
=PP5V_S3_P5VS3 → =PP5V_S3_FET
C8300 0.0022uF 10% 50V CERM 402
=P5VS3_EN_L → R8300 0 5% 1/16W MF-LF 402 → P5VS3_EN_L_RC

5V S0 FET

Q8305 FDC638P SM-LF
=PP5V_S0_P5VS0 → =PP5V_S0_FET
C8306 22uF 20% 6.3V X5R 805
C8305 0.0022uF 10% 50V CERM 402
C8307 22uF 20% 6.3V X5R 805
=P5VS0_EN_L → R8305 100K 5% 1/16W MF-LF 402 → P5VS0_EN_L_RC

2.5V S0 FET

=PP2V5_S0_P2V5S0 → Q8320 SI3446DV TSOP-LF → =PP2V5_S0_FET
C8320 0.0022uF 10% 50V CERM 402
=P2V5S0_EN → R8320 0 5% 1/16W MF-LF 402 → P2V5S0_EN_RC

Power Control Signals

=PP5V_S5_PWRCTL
R8350 10K 5% 1/16W MF-LF 402
R8351 10K 5% 1/16W MF-LF 402
GPU requires 1.2V, 1.8V, 2.5V and 3.3V rise after VCore is up. (How to guarantee 3.3V?)
=GPUVCORE_PGOOD
Need to ensure that ISL6269 PGOOD does not deassert while GPU PowerPlay is changing GPU core voltage.
PM_SLP_S3_LS5V_L (MAKE_BASE=TRUE) → =P2V5S0_EN, =P1V8S0_EN, =P1V2S0_EN
Q8350 2N7002DW-X-F SOT-363
=P5VS0_EN_L, =P3V3S0_EN_L, LIO_P3V3S0_EN_L
PM_SLP_S3_LS5V (MAKE_BASE=TRUE)
=PP3V42_G3H_PWRCTL
Q8350 2N7002DW-X-F SOT-363
R8354 100K 5% 1/16W MF-LF 402
P1V5S0_RUNSS
1.5V Enable has pull-up to PBUS
Q8357 2N7002DW-X-F SOT-363
PM_SLP_S3_L
R8356 100K 5% 1/16W MF-LF 402
Q8357 2N7002DW-X-F SOT-363
(PM_SLP_S3_L) (MAKE_BASE=TRUE) → =P1V05S0_EN, =GPUVCORE_EN, =MEMVREF_EN, =PBUSVSENS_EN
=PP5V_S5_PWRCTL
R8355 10K 5% 1/16W MF-LF 402
PM_SLP_S4_LS5V (MAKE_BASE=TRUE) → =P5VS3_EN_L, =P3V3S3_EN_L, P1V2S3_RUNSS
1.2V Enable has pull-up to 3.3V
Q8355 2N7002DW-X-F SOT-363
Q8355 2N7002DW-X-F SOT-363
PM_SLP_S4_L
R8357 100K 5% 1/16W MF-LF 402
(PM_SLP_S4_L) (MAKE_BASE=TRUE) → =P1V8S3_EN, =RTUSB_EN, LIO_P3V3S3_EN
Q8358 TP0610 SOT23-3
PPVIN_S3_P2V5S3
P2V5S3_SHDNRT
2.5V SHDN/RT pin has dual purpose and pull-down at regulator.
=PP3V42_G3H_PWRCTL
P5VS5_PGOOD
(P5VS5_PGOOD) (MAKE_BASE=TRUE) → =P3V3S5_EN
R8359 470K 5% 1/16W MF-LF 402
P5VS5_RUNSS
5V Enable has pull-up to PBUS
Q8359 2N7002DW-X-F SOT-363
SMC_PM_G2_EN_L
SMC_PM_G2_EN
R8358 100K 5% 1/16W MF-LF 402
Q8359 2N7002DW-X-F SOT-363

3.3V S3 FET

Q8310 FDC638P SM-LF
=PP3V3_S3_P3V3S3 → =PP3V3_S3_FET
C8310 0.0022uF 10% 50V CERM 402
=P3V3S3_EN_L → R8310 100K 5% 1/16W MF-LF 402 → P3V3S3_EN_L_RC

3.3V S0 FET

Q8315 FDC638P SM-LF
=PP3V3_S0_P3V3S0 → =PP3V3_S0_FET
C8315 0.0022uF 10% 50V CERM 402
=P3V3S0_EN_L → R8315 100K 5% 1/16W MF-LF 402 → P3V3S0_EN_L_RC

1.8V S0 FET

=PP1V8_S0_P1V8S0 → Q8325 FDC796N SUPERSOT-6 → =PP1V8_S0_FET
C8325 0.0022uF 10% 50V CERM 402
C8326 22uF 20% 6.3V X5R 805
C8327 22uF 20% 6.3V X5R 805
=P1V8S0_EN → R8325 0 5% 1/16W MF-LF 402 → P1V8S0_EN_RC

1.2V S0 FET

=PP1V2_S0_P1V2S0 → Q8330 SI3446DV TSOP-LF → =PP1V2_S0_FET
C8330 0.0022uF 10% 50V CERM 402
=P1V2S0_EN → R8330 0 5% 1/16W MF-LF 402 → P1V2S0_EN_RC

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

=PP3V3_S5_P1V5PG
PP1V5_S0
R8361 27.4K 1% 1/16W MF-LF 402
R8363 4.99K 1% 1/16W MF-LF 402
C8360 0.1uF 20% 10V CERM 402
U8360 LMC7211 SM-LF
0.89V Reference → P1V0_P1V5PG_REF
P1V5S0_COMP_POS
P1V5S0_PGOOD
R8362 10K 1% 1/16W MF-LF 402
R8364 10K 1% 1/16W MF-LF 402
R8365 10K 5% 1/16W MF-LF 402
1.5V Comp threshold set to 1.32V (88%)
IMVP_PWRGD_IN
=P1V05S0_PGOOD → P1V5P1V05S0_PGOOD (MAKE_BASE=TRUE)
ISL6269 undervoltage threshold 81-87% (0.85 - 0.91V)
NOTE: R8365 acts as 10K pull-up for PGOOD signal

Unused PGOOD Signals

=P5VP1V5_PGOOD → TP_P5V_P1V5_PGOOD (MAKE_BASE=TRUE)
=P2V5S3_PGOOD → TP_P2V5S3_PGOOD (MAKE_BASE=TRUE)
=P1V8S3_PGOOD → TP_P1V8S3_PGOOD (MAKE_BASE=TRUE)
=P1V2S3_PGOOD → TP_P1V2S3_PGOOD (MAKE_BASE=TRUE)
These rails are monitored by LTC2908

Other S0 Rails PWRGD Circuit

Reports when 5V S0, 3.3V S0, 2.5V S0, 1.8V S0, 1.2V S0 and 0.9V S0 are in regulation

PP5V_S0
PP3V3_S0
PP2V5_S0
PP1V8_S0
PP1V2_S0
PP0V9_S0
R8374 68.1K 1% 1/16W MF-LF 402
R8372 124K 1% 1/16W MF-LF 402
R8375 100K 1% 1/16W MF-LF 402
R8373 100K 1% 1/16W MF-LF 402
C8370 0.1uF 20% 10V CERM 402
C8371 0.1uF 20% 10V CERM 402
U8370 LTC2908 LLP
V1, V2, V3, V4 CRITICAL, VADJ1, VADJ2, RST*, GND, THRML PAD
S0PGOOD_1V2_DIV
S0PGOOD_0V9_DIV
S0PGOOD_PWROK
R8376 549K 1% 1/16W MF-LF 402
LTC2908 sources 6uA at 5.0V
R8375 serves as pull-down
and 3.3V level-shifter.
LTC2908 threshold is 95% (4.75V, 3.135V, 2.375V, 1.71V, 1.14V, 0.86V)

=PP3V3_S0_ALLSYSPG
U8380 MC74VHC1G08 SC70
ALL_SYS_PWRGD
C8380 0.1UF 20% 10V CERM 402

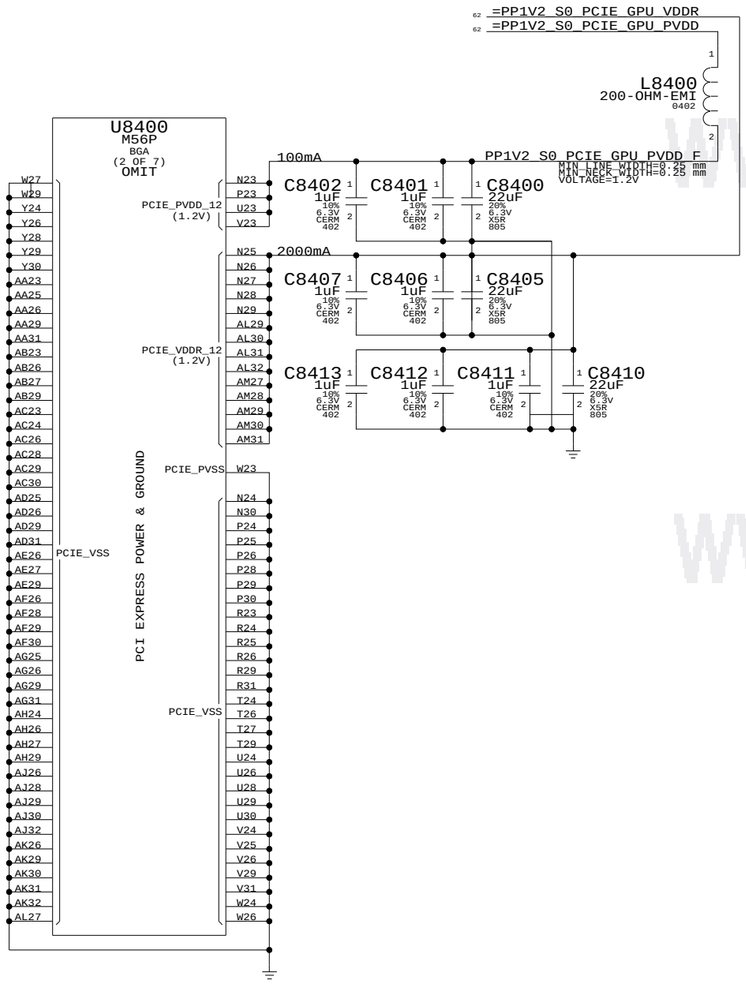
S3/S0 FETs & Power Control

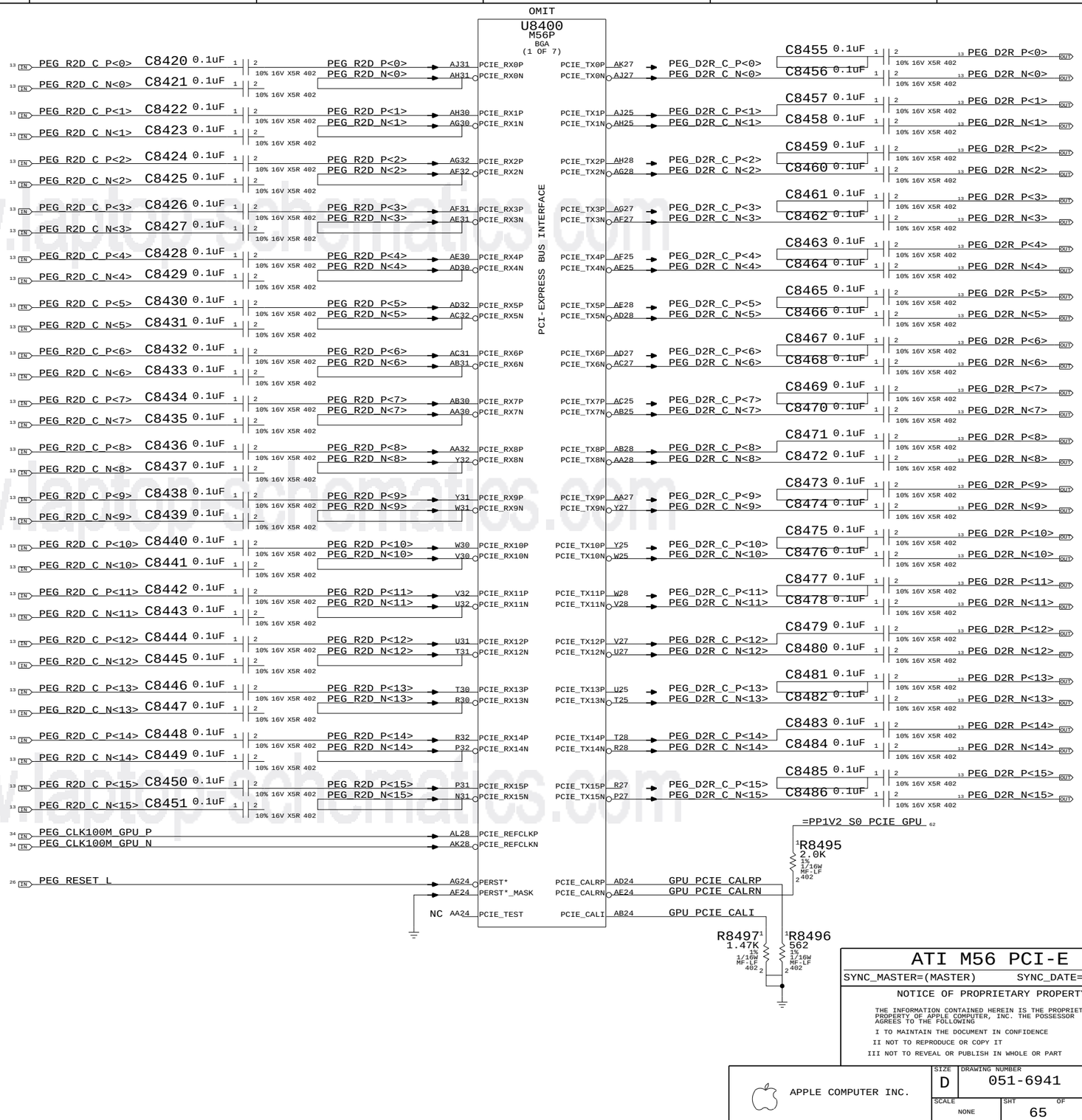
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6941 | REV. 07001

SCALE NONE | SHT 64 OF 81





ATI M56 PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001
SCALE: NONE	SHT 65 OF 81	

GPU VCore Supply

=PP5V_S0_GPUVCORE
=PPVIN_S0_GPUVCORE
C8501 1uF 10% 16V X5R 603
C8500 2.2UF 20% 6.3V CERM 603
NO STUFF R8502 0 5% 1/16W MF-LF 402
PP5V_S0_GPUVCORE_VCC
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
NO STUFF R8504 0 5% 1/16W MF-LF 402
C8502 2.2UF 20% 6.3V CERM 603
U8500 ISL6269 QFN
PVCC VCC
VIN FSET EN FCCM PGOOD COMP FB VO THRML PAD
UG BOOT PHASE ISEN LG PGND
=GPUVCORE_EN
=GPUVCORE_PGOOD
GPUVCORE_FSET
GPUVCORE_FCCM
GPUVCORE_COMP
GPUVCORE_FB
GPUVCORE_UG MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm
GPUVCORE_BOOT MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm
GPUVCORE_PHASE MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm SWITCH_NODE=TRUE
GPUVCORE_ISEN
GPUVCORE_LG MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm
C8509 0.22UF 20% 25V CERM 402
R8510 3.01K 1% 1/16W MF-LF 402
R8508 51.1K 1% 1/16W MF-LF 402
C8507 470pF 10% 50V CERM 402
C8506 0.01UF 10% 16V CERM 402
R8506 57.6K 1% 1/16W MF-LF 402
GPUVCORE_COMP_R
R8505 0 5% 1/16W MF-LF 402
C8508 0.022UF 10% 16V CERM-X5R 402
XW8500 SM
GND_GPUVCORE_SGND
C8530 22uF 20% 6.3V X7R 1210
C8531 22uF 20% 6.3V X7R 1210
C8532 22uF 20% 6.3V X7R 1210
CRITICAL Q8520 HAT2168H LFPAK
CRITICAL Q8521 HAT2165H LFPAK
CRITICAL Q8522 HAT2165H LFPAK
NO STUFF C8522 1000pF 10% 25V X7R 402
NO STUFF C8521 1000pF 10% 25V X7R 402
D8520 B340LBXF
CRITICAL L8520 1.0uH-20.5 SM1
NC

GPU VCore Current Sense

GPUISENS_NTC
R8596 1K 1% 1/10W MF-LF 402
R8597 10KOHM 0603-LF
NO STUFF R8594 1K 1% 1/10W MF-LF 402
C8590 1uF 10% 6.3V CERM 402
GPUISENS_RC
R8590 649 1% 1/10W MF-LF 402
=PP3V3R5V_S0_GPUISENS
R8593 20.0K 1% 1/10W MF-LF 402
GPUISENS_NEG
R8591 20.0K 1% 1/10W MF-LF 402
GPUISENS_POS
C8598 470pF 10% 50V CERM 402
R8598 1M 1% 1/16W MF-LF 402
C8595 1uF 10% 6.3V CERM 402
U8595 LMV2011MF SOT23-5
GPUVCORE_IOUT
R8592 1M 1% 1/16W MF-LF 402
C8592 470pF 10% 50V CERM 402

Placement Note:
Keep C8590, R8590, R8594 and R8597 close to inductor

=PPVCORE_S0_GPU_REG
Vout = 1.08V / 1.00V
17A max output
(Q8520 limit)

<Ra> R8521 10K 1% 1/10W MF-LF 402
C8520 0.0047uF 10% 25V CERM 402
C8540 22uF 20% 6.3V X5R 805
C8542 330uF 20% 2.5V-ESR9V CASE-D2E-LF
<Rb> R8522 15.0K 1% 1/10W MF-LF 402
<Rc> R8523 75K 1% 1/10W MF-LF 402
C8541 22uF 20% 6.3V X5R 805
C8543 330uF 20% 2.5V-ESR9V CASE-D2E-LF
GPUVCORE_FB_LOW

Vout(low) = 0.6V * (1 + Ra / Rb)
Vout(high) = 0.6V * (1 + Ra / Req)
Req = Rb || Rc

Back-Bias Positive Supply

Back-bias positive supply provides VDDC + 0.5V when active.
When inactive, provides VDDC to BBP pins.
NOTE: BBP tracks VDDC based on GPU voltage GPIO.

=PPVCORE_S0_GPU_BBP
Q8575 FDC796N SUPERSOT-6 CRITICAL
GPUBB_EN_L
=PPVOUT_S0_GPUBBP_LDO
Vout = 1.58V / 1.50V
180mA max output
(LDO limit)
CRITICAL U8550 FAN2558 SOT23-6-LF
VIN PG EN GND VOUT ADJ
=PP3V3_S0_GPUBBP
GPUBB_EN
C8551 2.2uF 20% 6.3V CERM 603
C8555 0.01UF 10% 16V CERM 402
<Ra> R8555 24.9K 1% 1/16W MF-LF 402
C8556 22uF 20% 6.3V X5R 805
GPUBBP_ADJ
<Rc> R8554 174K 1% 1/16W MF-LF 402
<Rb> R8556 16.2K 1% 1/16W MF-LF 402
C8557 22uF 20% 6.3V X5R 805
GPUBBP_ADJ_LOW
Q8554 2N7002 SOT23-LF
GPU_VCORE_HIGH

Vout(low) = 0.59V * (1 + Ra/Rb)
Vout(high) = 0.59V * (1 + Ra/Req)
Req = Rb || Rc

Pull-up voltage must be high enough to satisfy BBP FET Vgs (where Vs = 1.2V)
=PP5V_S0_GPUBBCTL
FDC796N max Vgs is 3.0V
Vin must be > 4.2V
R8570 100K 5% 1/10W MF-LF 402
GPUBB_EN_L
=PP3V3_S0_GPUBBCTL
GPU_BB_CTL
R8561 0 5% 1/10W MF-LF 402
GPU_GENERICD
GPU_BB_EN
U8560 MC74VHC1G08 SC70
GPUBB_EN
R8560 10K 5% 1/10W MF-LF 402
C8560 1UF 10% 6.3V CERM 402
Q8570 2N7002 SOT23-LF
C8570 0.01uF 10% 16V CERM 402

Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.5V when active.
When inactive, provides VSS to BBN pins.

=PP3V3_S0_GPUBBN
C8580 10uF 20% 6.3V X5R 603
CRITICAL L8585 15uH SDQ12150-SM
GPUBBN_SW MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm
GPUBBN_D
C8585 330pF 10% 50V CERM 402
GPUBBN_D_RC MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm
R8585 10 5% 1/10W MF-LF 603
U8580 LT3483 TSOT23-6
SW VIN SHDN* GND FB (GPUBBN_D)
CRITICAL
MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm
GPUBB_EN
GPUBBN_FB
C8589 22uF 20% 6.3V X5R 805
=PNVOUT_S0_GPUBBN_REG
Vout = -0.50V
150mA max output
(Inductor & IC current limit)
Q8576 FDC796N SUPERSOT-6 CRITICAL
GPUBB_EN_L
Watch FET Vgs, since Vs will be negative
FDC796N min Vgs is 1.0V
C8586 220pF 5% 25V CERM 402
<Ra> R8586 49.9K 1% 1/16W MF-LF 402

Vout = -10uA * Ra

GPU (M56) Core Supplies

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.

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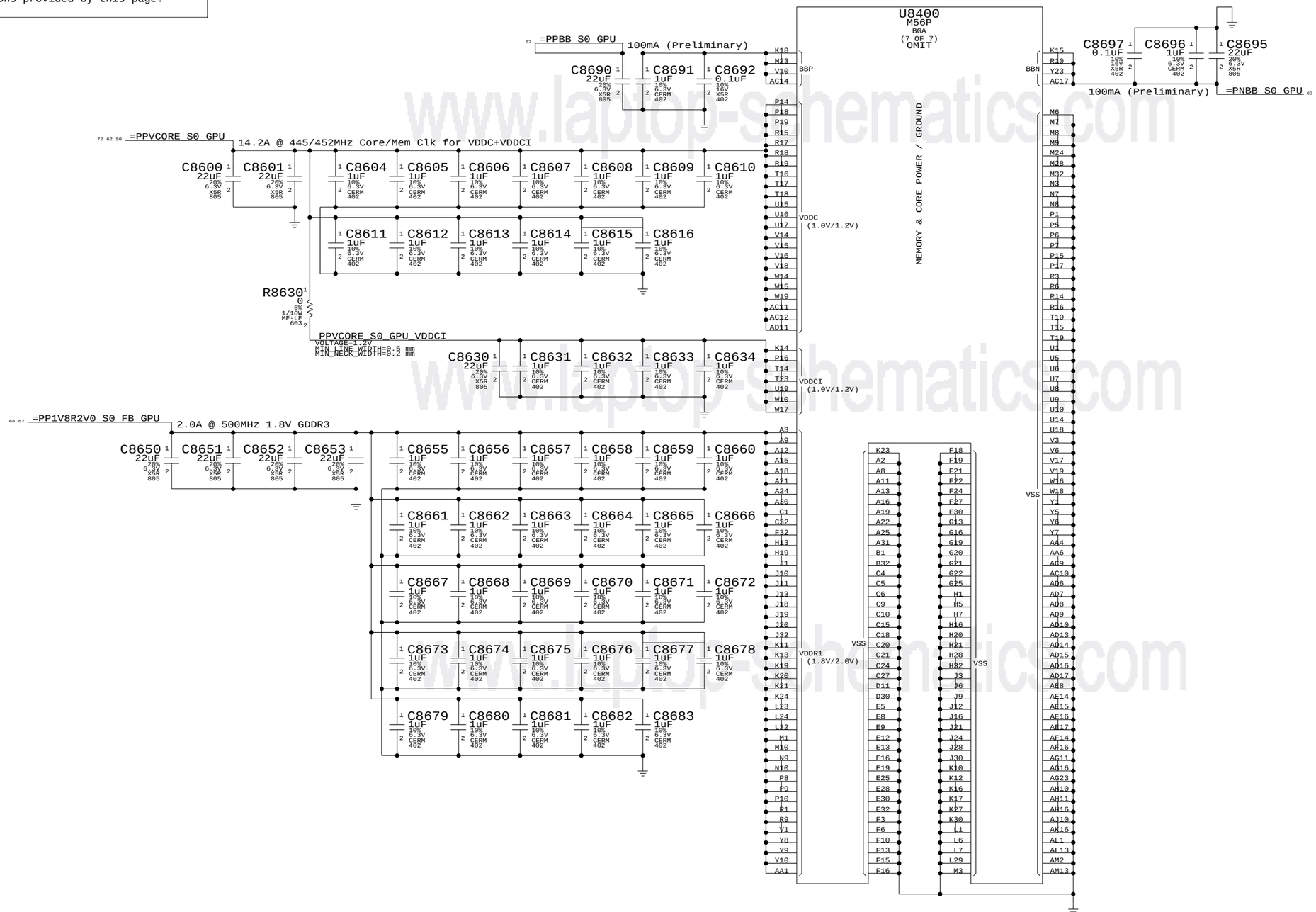
Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

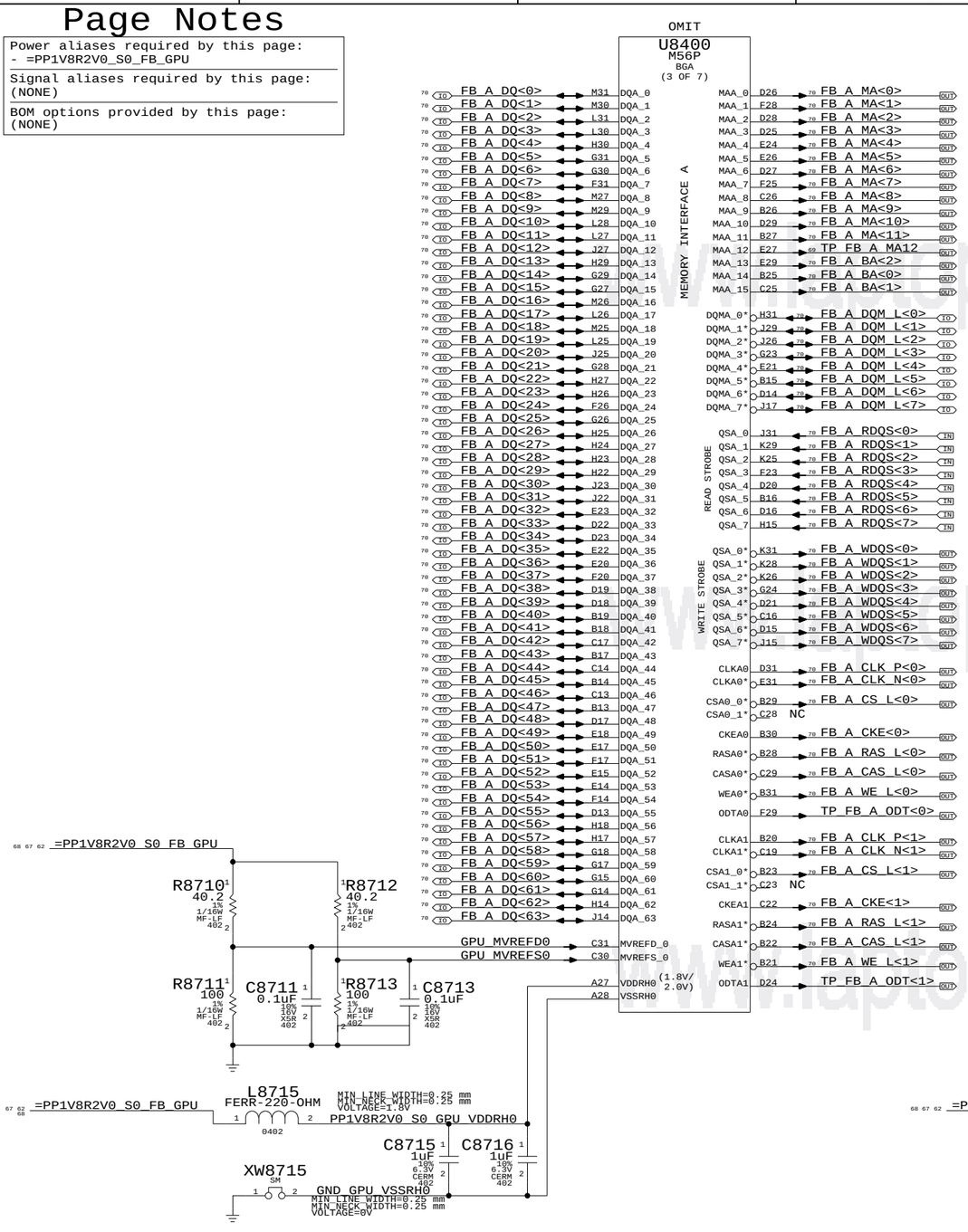
SCALE	SHT	OF
NONE	67	81

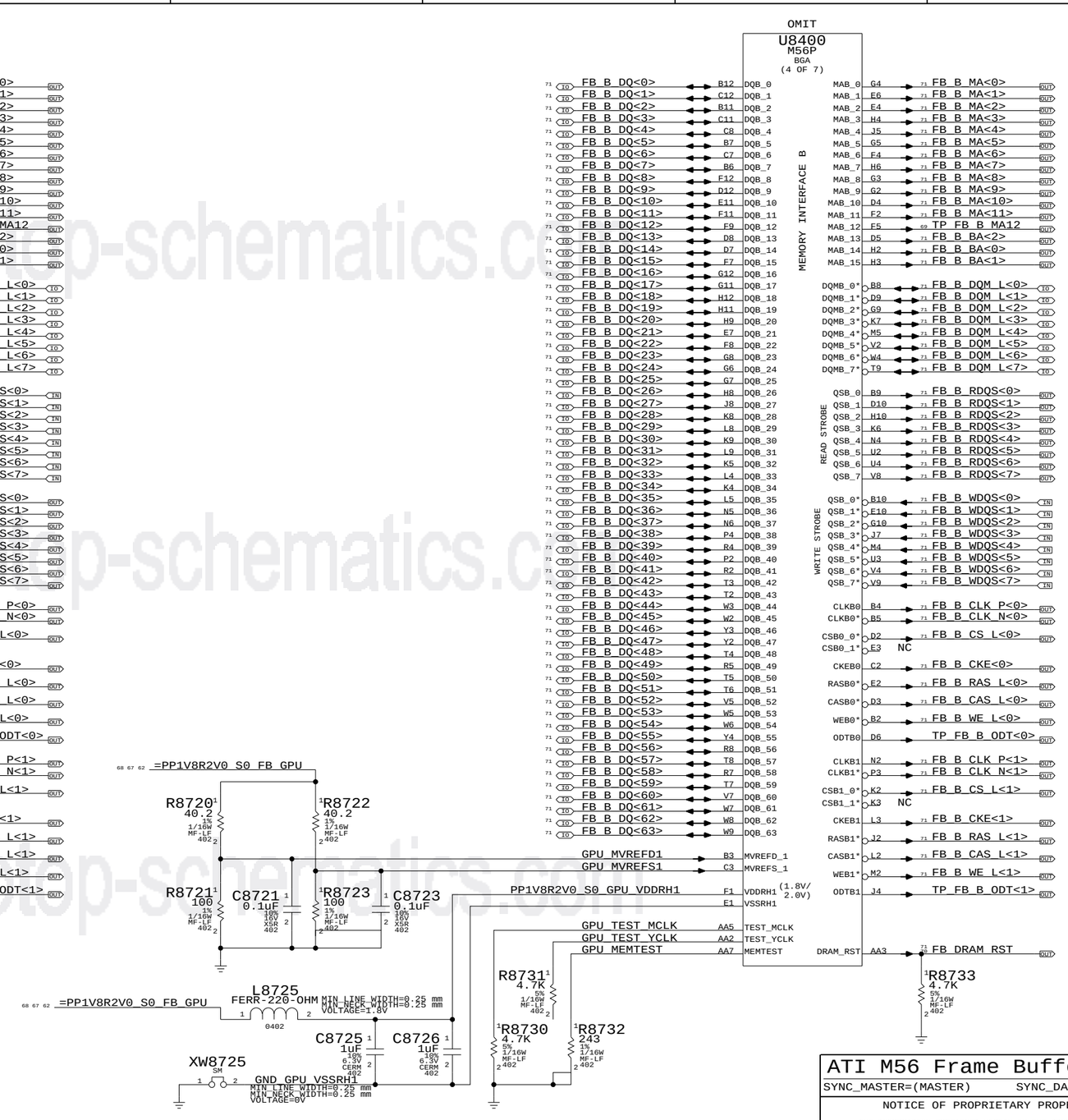
Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)





ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

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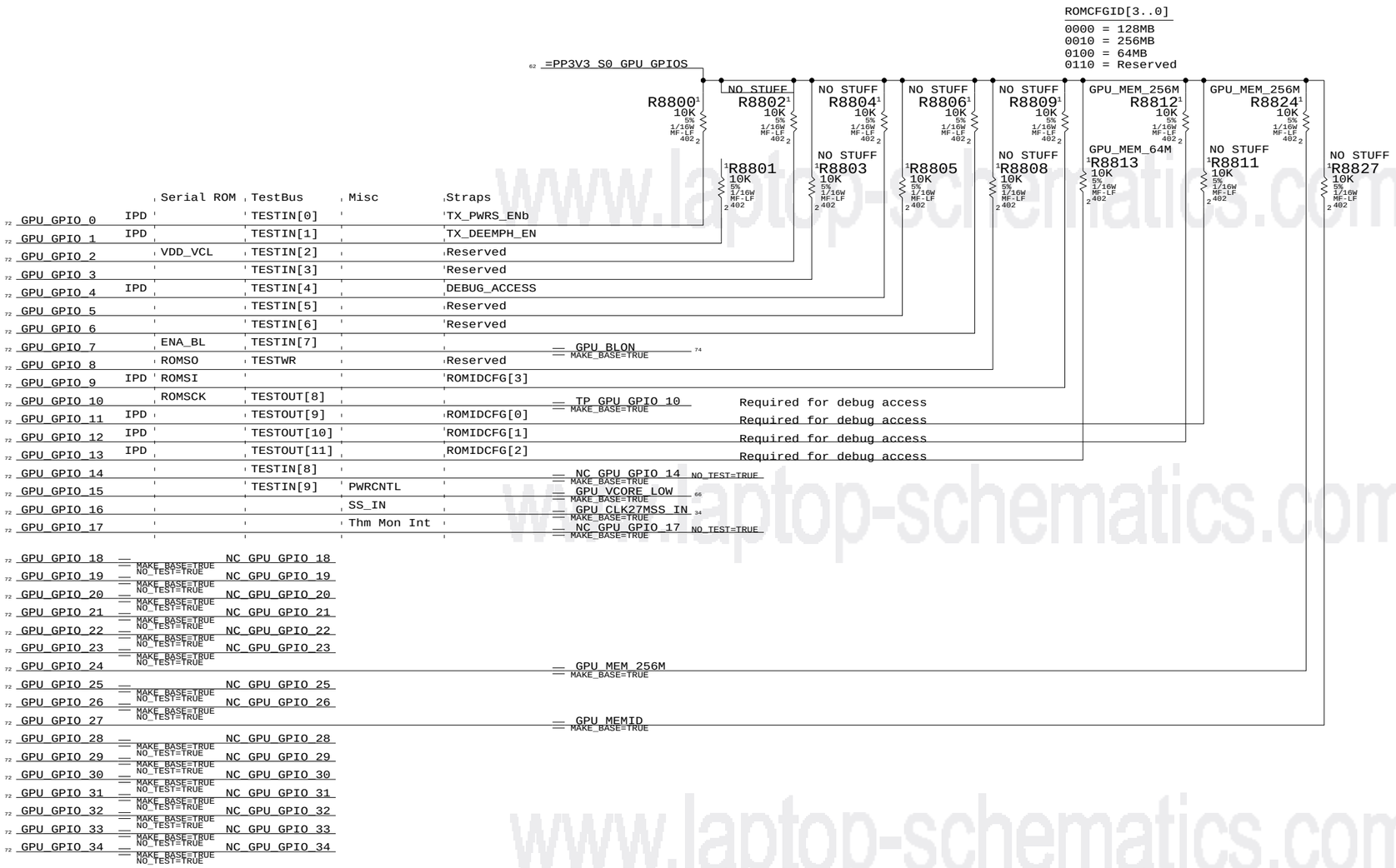


Renamed signals

GPU_CLK27M (MAKE_BASE=TRUE) = GPU_XTALIN

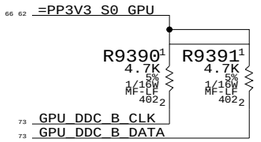
Unused signals

NC_GPU_XTALOUT (MAKE_BASE=TRUE, NO_TEST=TRUE) = GPU_XTALOUT
NC_ATI_ROMCS_L (MAKE_BASE=TRUE, NO_TEST=TRUE) = TP_ATI_ROMCS_L
NC_FB_A_MA12 (MAKE_BASE=TRUE, NO_TEST=TRUE) = TP_FB_A_MA12
NC_FB_B_MA12 (MAKE_BASE=TRUE, NO_TEST=TRUE) = TP_FB_B_MA12
NC_GPU_GENERICA (MAKE_BASE=TRUE, NO_TEST=TRUE) = GPU_GENERICA
NC_GPU_GENERICB (MAKE_BASE=TRUE, NO_TEST=TRUE) = GPU_GENERICB
NC_GPU_GENERICC (MAKE_BASE=TRUE, NO_TEST=TRUE) = GPU_GENERICC
NC_GPU_VGA_R (MAKE_BASE=TRUE, NO_TEST=TRUE) = GPU_VGA_R
NC_GPU_VGA_G (MAKE_BASE=TRUE, NO_TEST=TRUE) = GPU_VGA_G
NC_GPU_VGA_B (MAKE_BASE=TRUE, NO_TEST=TRUE) = GPU_VGA_B
TP_GPU_VGA_HSYNC (MAKE_BASE=TRUE) = GPU_VGA_HSYNC
TP_GPU_VGA_VSYNC (MAKE_BASE=TRUE) = GPU_VGA_VSYNC
NC_GPU_TV_Y (MAKE_BASE=TRUE, NO_TEST=TRUE) = GPU_TV_Y
NC_GPU_TV_C (MAKE_BASE=TRUE, NO_TEST=TRUE) = GPU_TV_C
NC_GPU_TV_COMP (MAKE_BASE=TRUE, NO_TEST=TRUE) = GPU_TV_COMP
NC_LVDS_U_DATAP<3> (MAKE_BASE=TRUE, NO_TEST=TRUE) = LVDS_U_DATA_P<3>
NC_LVDS_U_DATAN<3> (MAKE_BASE=TRUE, NO_TEST=TRUE) = LVDS_U_DATA_N<3>
NC_LVDS_L_DATAP<3> (MAKE_BASE=TRUE, NO_TEST=TRUE) = LVDS_L_DATA_P<3>
NC_LVDS_L_DATAN<3> (MAKE_BASE=TRUE, NO_TEST=TRUE) = LVDS_L_DATA_N<3>
NC_ATI_DVPCLK (MAKE_BASE=TRUE, NO_TEST=TRUE) = ATI_DVPCLK
NC_ATI_DVPCNTL<2..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) = ATI_DVPCNTL<2..0>
NC_ATI_DVPDATA<15..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) = ATI_DVPDATA<15..0>

Required for debug access

TP_ATI_DVPDATA<23..16> (MAKE_BASE=TRUE) = ATI_DVPDATA<23..16>

Also required: GPIO10 - GPIO13



GPU Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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SCALE: NONE SHT 69 OF 81

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

=PP1V8_S0_FB_VDD

=PP1V8_S0_FB_VDDQ

C8900 22uF 20% 6.3V X5R 805 2

C8901 C8902 C8903 C8904 0.1uF 10% 16V X5R 402 2

L8910 FERR-220-OHM 0402

L8915 FERR-220-OHM 0402

PP1V8_S0_FB_A0_VDDA0 MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.8V

PP1V8_S0_FB_A0_VDDA1 MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.8V

Connect to designated pin, then GND

C8910 C8915 0.1uF 10% 16V X5R 402 2

U8900.J1 U8900.J12

C8920 22uF 20% 6.3V X5R 805 2

C8921 C8922 C8923 C8924 C8925 C8926 0.1uF 10% 16V X5R 402 2

R8930 R8932 2.37K 1% 1/16W MF-LF 402 2

R8931 R8933 5.49K 1% 1/16W MF-LF 402 2

FB_A0_VREF0 MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

FB_A0_VREF1 MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

C8931 C8933 0.1uF 10% 16V X5R 402 2

R8940 R8942 121 1% 1/16W MF-LF 402 2

R8944 121 1% 1/16W MF-LF 402 2

R8946 60.4 1% 1/16W MF-LF 402 2

R8941 0 5% 1/16W MF-LF 402 2

R8943 121 1% 1/16W MF-LF 402 2

R8945 60.4 1% 1/16W MF-LF 402 2

R8947 121 1% 1/16W MF-LF 402 2

NOTE: U8900 DQ0-7 MUST connect to GPU DQA0-7 or DQA8-15. Bits can be swapped within byte-lane, but software must know how these bits are mapped for GPU to support GDDR3 vendor/device identification scheme.

CRITICAL OMIT

U8900 FBGA (2 OF 2) 16MX32-GDDR3-500MHZ K4J52324QC-BC20

MFHIGH

FB_A_MA<0> FB_A_MA<1> FB_A_MA<2> FB_A_MA<3> FB_A_MA<4> FB_A_MA<5> FB_A_MA<6> FB_A_MA<7> FB_A_MA<8> FB_A_MA<9> FB_A_MA<10> FB_A_MA<11>

FB_A_CKE<0> FB_A_CLK_P<0> FB_A_CLK_N<0> FB_A_CS_L<0> FB_A_WE_L<0> FB_A_CAS_L<0> FB_A_RAS_L<0>

FB_A0_ZQ FB_A0_MF FB_A0_SEN

FB_DRAM_RST

FB_A_RDQS<0> FB_A_RDQS<1> FB_A_RDQS<2> FB_A_RDQS<3>

FB_A_WDQS<0> FB_A_WDQS<1> FB_A_WDQS<2> FB_A_WDQS<3>

FB_A_BA<0> FB_A_BA<1> FB_A_BA<2>

NC NC

R8948 243 1% 1/16W MF-LF 402 2

R8949 0 5% 1/16W MF-LF 402 2

FB_A_DQM_L<0> FB_A_DQM_L<1> FB_A_DQM_L<2> FB_A_DQM_L<3>

FB_A_DQ<0> FB_A_DQ<1> FB_A_DQ<2> FB_A_DQ<3> FB_A_DQ<4> FB_A_DQ<5> FB_A_DQ<6> FB_A_DQ<7> FB_A_DQ<8> FB_A_DQ<9> FB_A_DQ<10> FB_A_DQ<11> FB_A_DQ<15> FB_A_DQ<14> FB_A_DQ<12> FB_A_DQ<13> FB_A_DQ<19> FB_A_DQ<16> FB_A_DQ<18> FB_A_DQ<17> FB_A_DQ<23> FB_A_DQ<21> FB_A_DQ<20> FB_A_DQ<22> FB_A_DQ<24> FB_A_DQ<25> FB_A_DQ<26> FB_A_DQ<27> FB_A_DQ<29> FB_A_DQ<30> FB_A_DQ<28> FB_A_DQ<31>

C8950 22uF 20% 6.3V X5R 805 2

C8951 C8952 C8953 C8954 0.1uF 10% 16V X5R 402 2

L8960 FERR-220-OHM 0402

L8965 FERR-220-OHM 0402

PP1V8_S0_FB_A1_VDDA0 MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.8V

PP1V8_S0_FB_A1_VDDA1 MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.8V

Connect to designated pin, then GND

C8960 C8965 0.1uF 10% 16V X5R 402 2

U8900.J1 U8900.J12

C8970 22uF 20% 6.3V X5R 805 2

C8971 C8972 C8973 C8974 C8975 C8976 0.1uF 10% 16V X5R 402 2

R8980 R8982 2.37K 1% 1/16W MF-LF 402 2

R8981 R8983 5.49K 1% 1/16W MF-LF 402 2

FB_A1_VREF0 MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

FB_A1_VREF1 MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

C8981 C8983 0.1uF 10% 16V X5R 402 2

R8990 R8992 121 1% 1/16W MF-LF 402 2

R8994 121 1% 1/16W MF-LF 402 2

R8996 60.4 1% 1/16W MF-LF 402 2

R8991 0 5% 1/16W MF-LF 402 2

R8993 121 1% 1/16W MF-LF 402 2

R8995 60.4 1% 1/16W MF-LF 402 2

R8997 121 1% 1/16W MF-LF 402 2

CRITICAL OMIT

U8950 FBGA (1 OF 2) 16MX32-GDDR3-500MHZ K4J52324QC-BC20

MFHIGH

FB_A_MA<0> FB_A_MA<1> FB_A_MA<2> FB_A_MA<3> FB_A_MA<4> FB_A_MA<5> FB_A_MA<6> FB_A_MA<7> FB_A_MA<8> FB_A_MA<9> FB_A_MA<10> FB_A_MA<11>

FB_A_CKE<1> FB_A_CLK_P<1> FB_A_CLK_N<1> FB_A_CS_L<1> FB_A_WE_L<1> FB_A_CAS_L<1> FB_A_RAS_L<1>

FB_A1_ZQ FB_A1_MF FB_A1_SEN

FB_DRAM_RST

FB_A_RDQS<4> FB_A_RDQS<5> FB_A_RDQS<6> FB_A_RDQS<7>

FB_A_WDQS<4> FB_A_WDQS<5> FB_A_WDQS<6> FB_A_WDQS<7>

FB_A_BA<0> FB_A_BA<1> FB_A_BA<2>

NC NC

R8998 243 1% 1/16W MF-LF 402 2

R8999 0 5% 1/16W MF-LF 402 2

FB_A_DQM_L<4> FB_A_DQM_L<5> FB_A_DQM_L<6> FB_A_DQM_L<7>

FB_A_DQ<32> FB_A_DQ<34> FB_A_DQ<33> FB_A_DQ<35> FB_A_DQ<36> FB_A_DQ<37> FB_A_DQ<38> FB_A_DQ<39> FB_A_DQ<40> FB_A_DQ<41> FB_A_DQ<42> FB_A_DQ<43> FB_A_DQ<46> FB_A_DQ<44> FB_A_DQ<47> FB_A_DQ<45> FB_A_DQ<48> FB_A_DQ<49> FB_A_DQ<50> FB_A_DQ<51> FB_A_DQ<52> FB_A_DQ<55> FB_A_DQ<54> FB_A_DQ<53> FB_A_DQ<60> FB_A_DQ<59> FB_A_DQ<61> FB_A_DQ<57> FB_A_DQ<62> FB_A_DQ<56> FB_A_DQ<63> FB_A_DQ<58>

GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

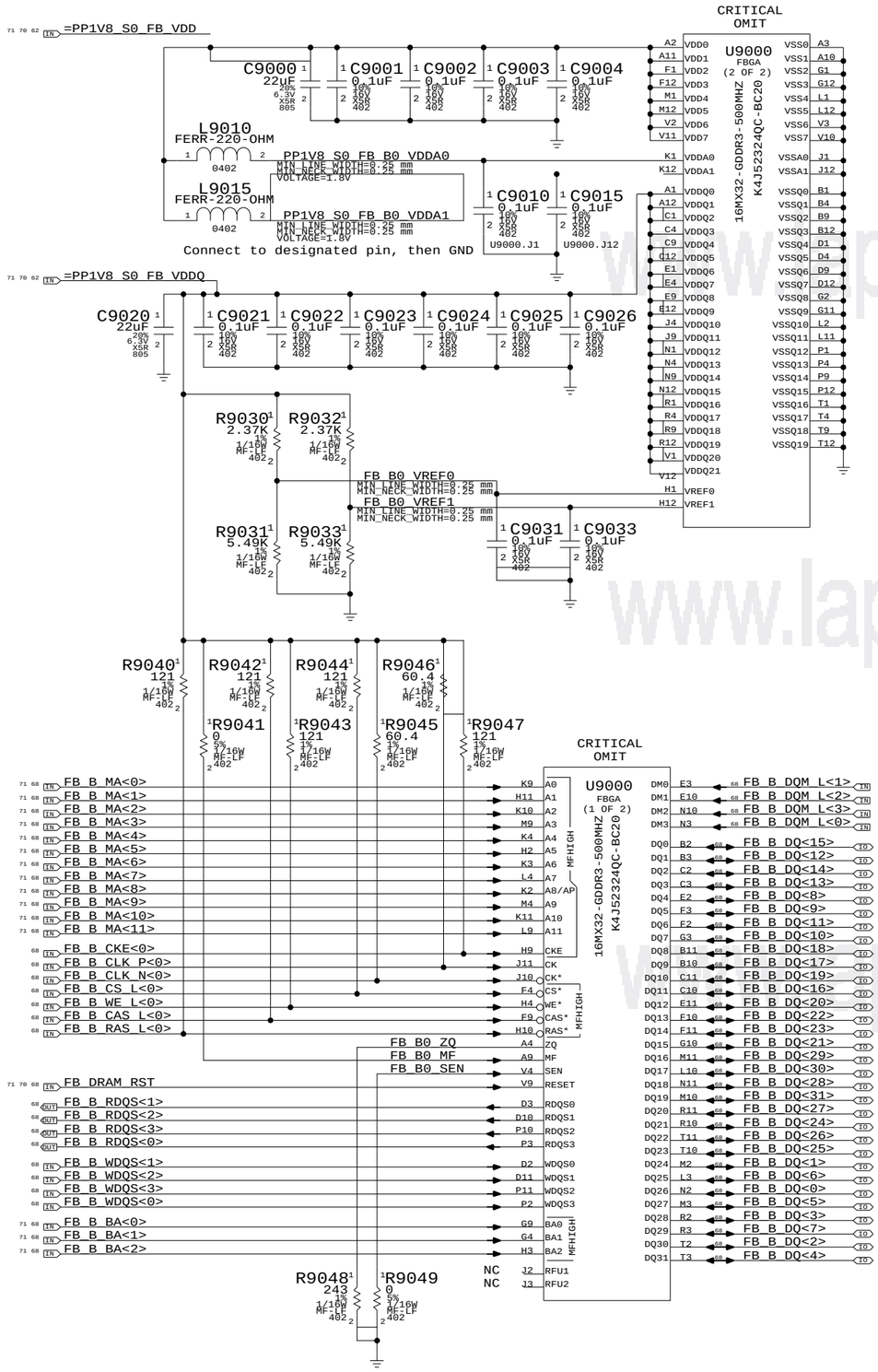
SIZE	DRAWING NUMBER	REV.
D	051-6941	07001
SCALE: NONE	SHT 70 OF 81	

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

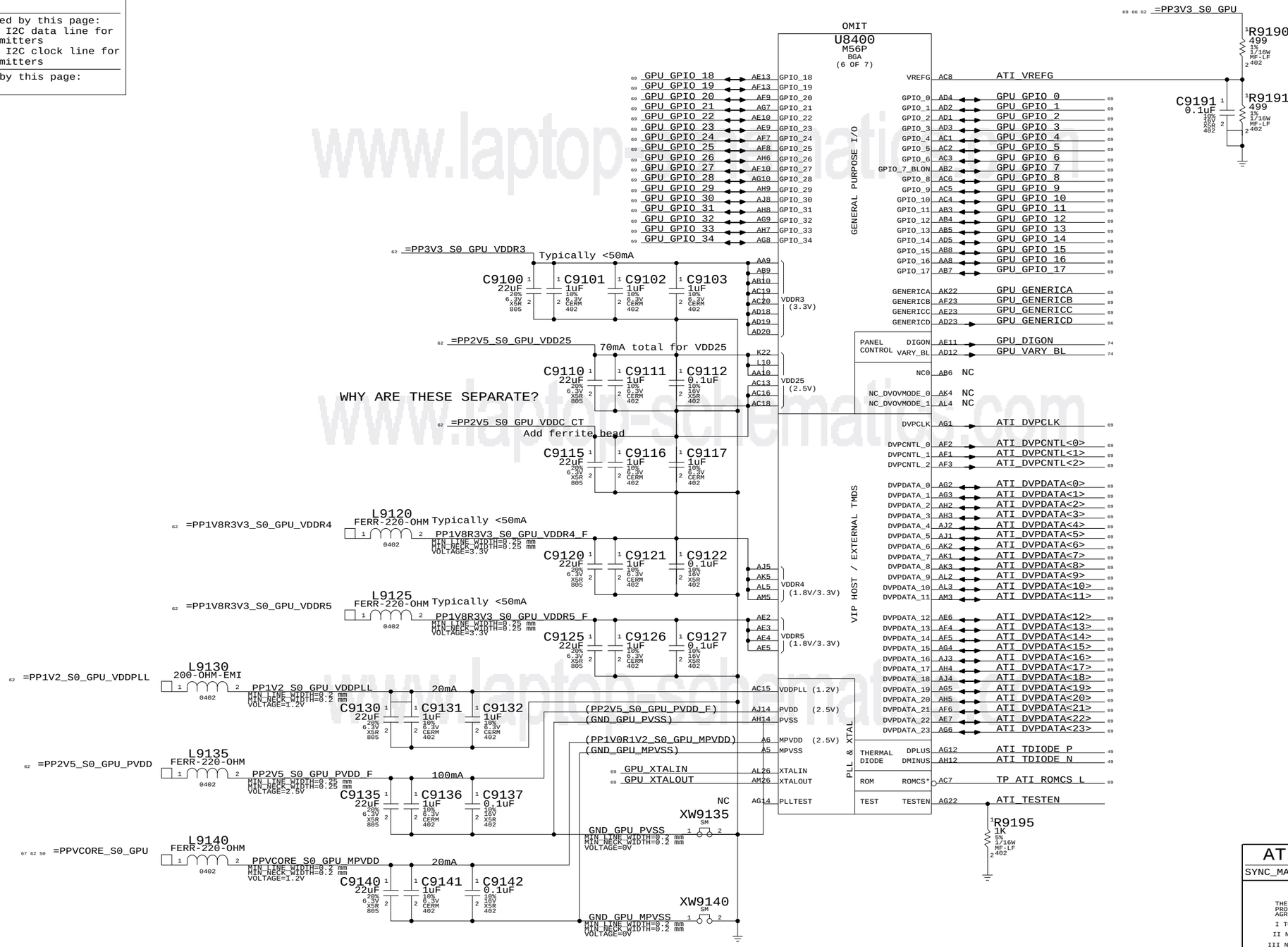
SIZE	DRAWING NUMBER	REV.
D	051-6941	07001
SCALE	SHT	OF
NONE	71	81

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



ATI M56 GPIO/DVO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

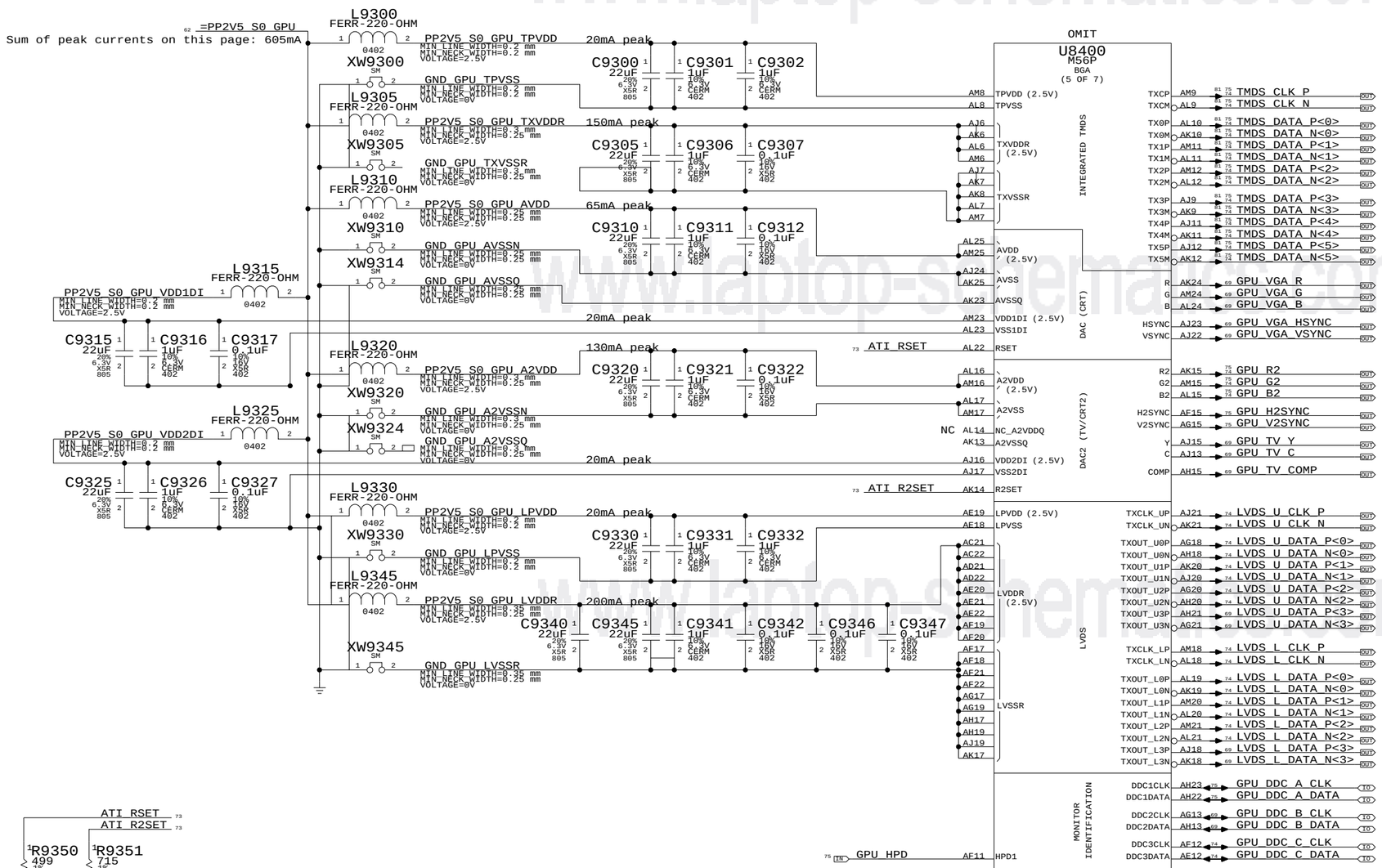
SIZE	DRAWING NUMBER	REV.
D	051-6941	07001
SCALE: NONE	SHT 72 OF 81	

Page Notes

Power aliases required by this page:
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

ATI M56 Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

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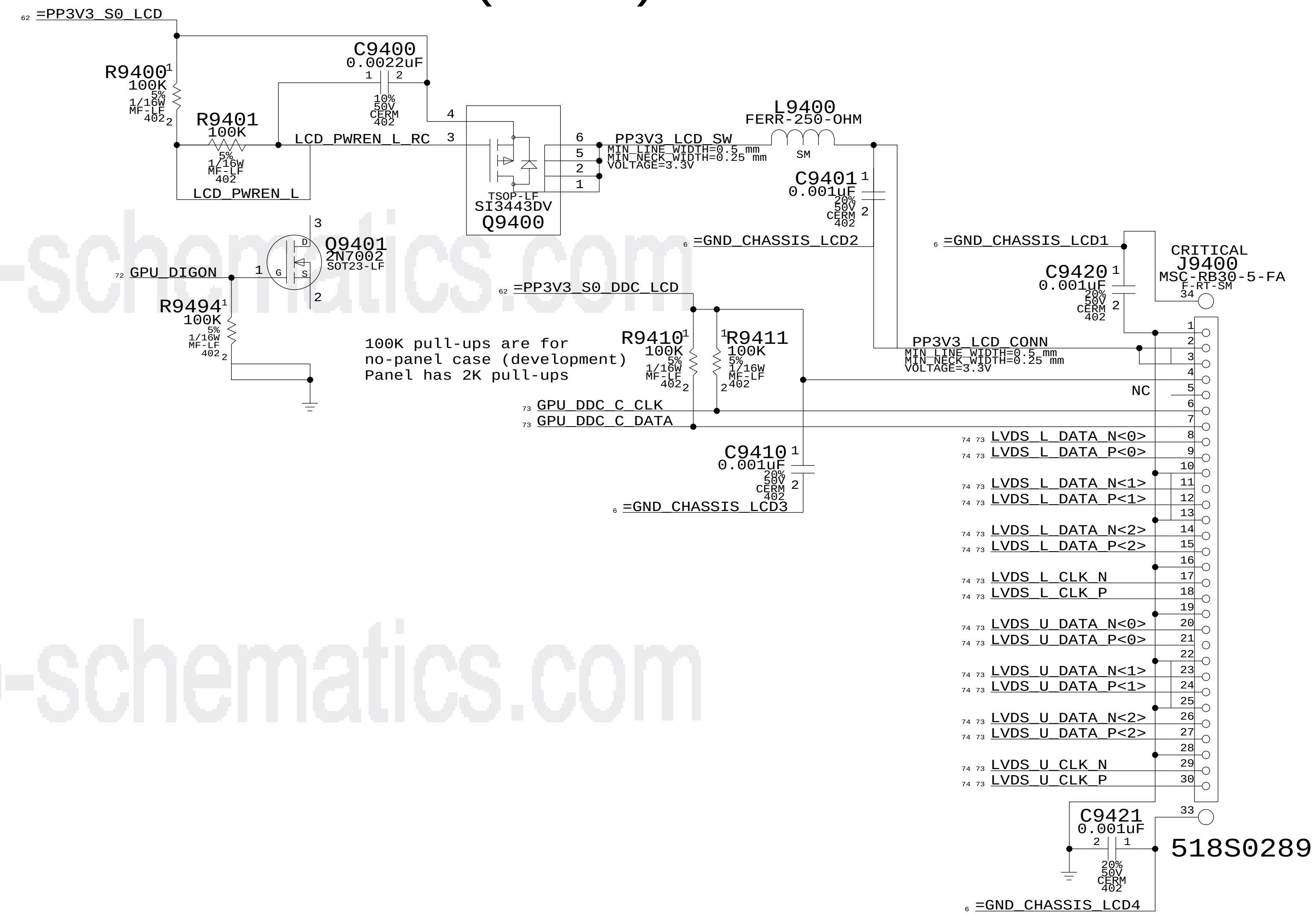
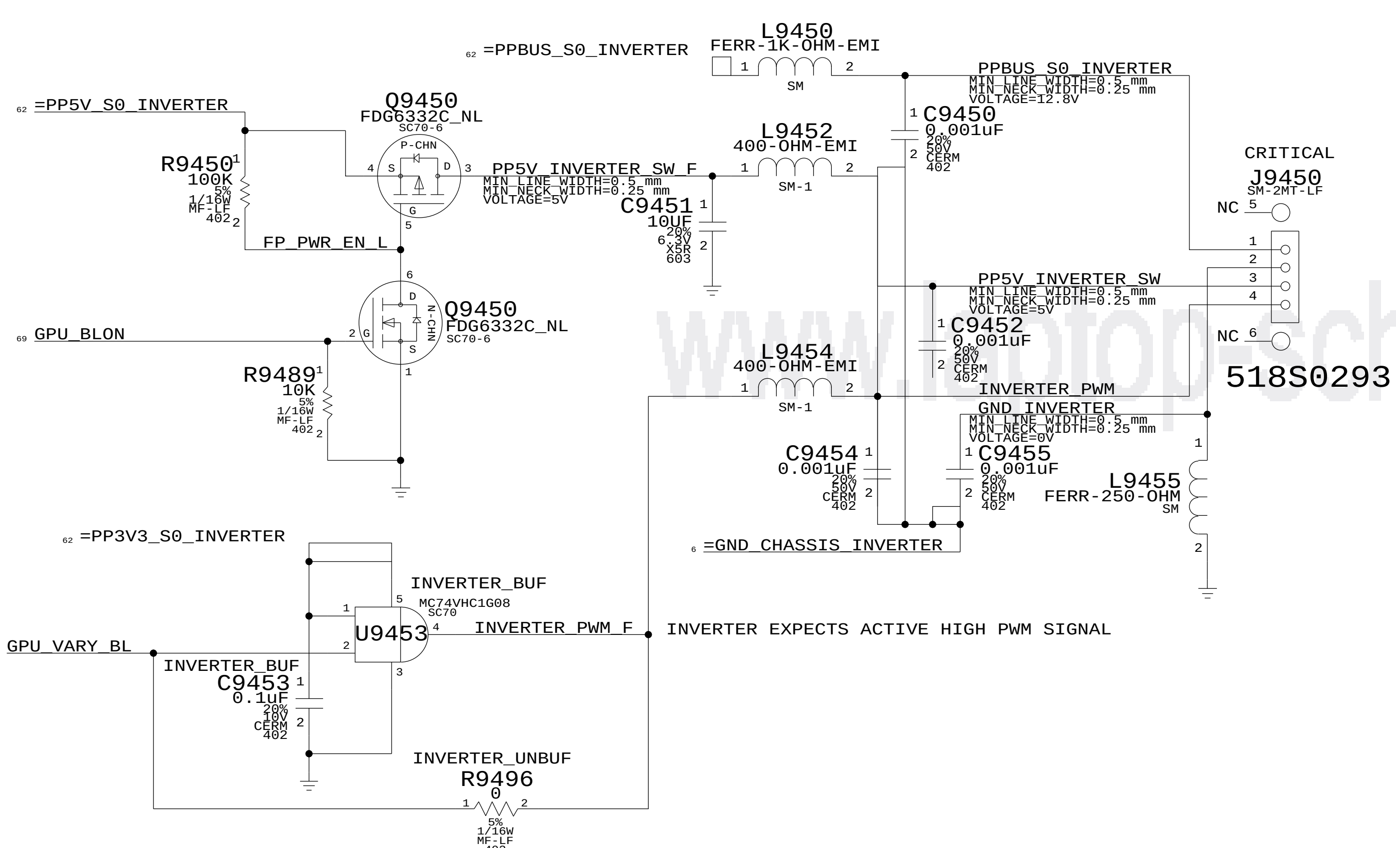
LCD (LVDS) INTERFACE

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	NET	
	VGA	VGA	GPU_R2	73 75
	VGA	VGA	GPU_G2	73 75
	VGA	VGA	GPU_B2	73 75
	LVDS	LVDS	LVDS_U_CLK_P	73 74
	LVDS	LVDS	LVDS_U_CLK_N	73 74
	LVDS	LVDS	LVDS_U_DATA_P<2..0>	73 74
	LVDS	LVDS	LVDS_U_DATA_N<2..0>	73 74
	LVDS	LVDS	LVDS_L_CLK_P	73 74
	LVDS	LVDS	LVDS_L_CLK_N	73 74
	LVDS	LVDS	LVDS_L_DATA_P<2..0>	73 74
	LVDS	LVDS	LVDS_L_DATA_N<2..0>	73 74
	TMDS	TMDS	TMDS_CLK_P	73 75 81
	TMDS	TMDS	TMDS_CLK_N	73 75 81
	TMDS	TMDS	TMDS_DATA_P<5..3>	73 75 81
	TMDS	TMDS	TMDS_DATA_N<5..3>	73 75 81
	TMDS	TMDS	TMDS_DATA_P<2..0>	73 75 81
	TMDS	TMDS	TMDS_DATA_N<2..0>	73 75 81



=PP3V3_S0_LCD
R9400 100K 5% 1/16W MF-LF 402
C9400 0.0022uF 10% 50V CERM 402
R9401 100K 5% 1/16W MF-LF 402
LCD_PWREN_L_RC
LCD_PWREN_L
Q9400 SI3443DV TSOP-LF
L9400 FERR-250-OHM SM
PP3V3_LCD_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
C9401 0.001uF 20% 50V CERM 402
Q9401 2N7002 SOT23-LF
GPU_DIGON
R9494 100K 5% 1/16W MF-LF 402
=GND_CHASSIS_LCD2
=GND_CHASSIS_LCD1
=PP3V3_S0_DDC_LCD
R9410 100K 5% 1/16W MF-LF 402
R9411 100K 5% 1/16W MF-LF 402
100K pull-ups are for
no-panel case (development)
Panel has 2K pull-ups
GPU_DDC_C_CLK
GPU_DDC_C_DATA
C9410 0.001uF 20% 50V CERM 402
=GND_CHASSIS_LCD3
C9420 0.001uF 20% 50V CERM 402
CRITICAL
J9400 MSC-RB30-5-FA F-RT-SM
PP3V3_LCD_CONN
NC
LVDS_L_DATA_N<0>
LVDS_L_DATA_P<0>
LVDS_L_DATA_N<1>
LVDS_L_DATA_P<1>
LVDS_L_DATA_N<2>
LVDS_L_DATA_P<2>
LVDS_L_CLK_N
LVDS_L_CLK_P
LVDS_U_DATA_N<0>
LVDS_U_DATA_P<0>
LVDS_U_DATA_N<1>
LVDS_U_DATA_P<1>
LVDS_U_DATA_N<2>
LVDS_U_DATA_P<2>
LVDS_U_CLK_N
LVDS_U_CLK_P
C9421 0.001uF 20% 50V CERM 402
518S0289
=GND_CHASSIS_LCD4

INVERTER INTERFACE



=PPBUS_S0_INVERTER
L9450 FERR-1K-OHM-EMI SM
PPBUS_S0_INVERTER
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.8V
=PP5V_S0_INVERTER
Q9450 FDG6332C_NL SC70-6
P-CHN
R9450 100K 5% 1/16W MF-LF 402
PP5V_INVERTER_SW_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
L9452 400-OHM-EMI SM-1
C9450 0.001uF 20% 50V CERM 402
C9451 10UF 20% 6.3V X5R 603
FP_PWR_EN_L
Q9450 FDG6332C_NL SC70-6
N-CHN
GPU_BLON
R9489 10K 5% 1/16W MF-LF 402
CRITICAL
J9450 SM-2MT-LF
NC
PP5V_INVERTER_SW
C9452 0.001uF 20% 50V CERM 402
518S0293
L9454 400-OHM-EMI SM-1
INVERTER_PWM
GND_INVERTER
VOLTAGE=0V
C9454 0.001uF 20% 50V CERM 402
C9455 0.001uF 20% 50V CERM 402
L9455 FERR-250-OHM SM
=GND_CHASSIS_INVERTER
=PP3V3_S0_INVERTER
INVERTER_BUF
MC74VHC1G08 SC70
U9453
INVERTER_PWM_F
INVERTER EXPECTS ACTIVE HIGH PWM SIGNAL
GPU_VARY_BL
INVERTER_BUF
C9453 0.1uF 20% 10V CERM 402
INVERTER_UNBUF
R9496 0 5% 1/16W MF-LF 402

Internal Display Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE NONE	SHT 74	OF 81

TMDS Filtering

Place series R's close to GPU, other parts near connector.

TMDS_DATA_N<0>	R9760 0	TMDS_DATA_R_N<0>	CRITICAL L9700 90-OHM-300mA 2012H	TMDS_DATA_F_N<0>
TMDS_DATA_P<0>	R9761 0	TMDS_DATA_R_P<0>		TMDS_DATA_F_P<0>
	R9762 49.9 1%	R9763 49.9 1%		
	C9762 0.001uF	TMDS_D0_CMF		
TMDS_DATA_N<1>	R9764 0	TMDS_DATA_R_N<1>	CRITICAL L9701 90-OHM-300mA 2012H	TMDS_DATA_F_N<1>
TMDS_DATA_P<1>	R9765 0	TMDS_DATA_R_P<1>		TMDS_DATA_F_P<1>
	R9766 49.9 1%	R9767 49.9 1%		
	C9766 0.001uF	TMDS_D1_CMF		
TMDS_DATA_N<2>	R9768 0	TMDS_DATA_R_N<2>	CRITICAL L9702 90-OHM-300mA 2012H	TMDS_DATA_F_N<2>
TMDS_DATA_P<2>	R9769 0	TMDS_DATA_R_P<2>		TMDS_DATA_F_P<2>
	R9770 49.9 1%	R9771 49.9 1%		
	C9770 0.001uF	TMDS_D2_CMF		
TMDS_CLK_N	R9772 0	TMDS_CLK_R_N	CRITICAL L9706 370-OHM SM	TMDS_CLK_F_P
TMDS_CLK_P	R9773 0	TMDS_CLK_R_P		TMDS_CLK_F_N
	R9774 49.9 1%	R9775 49.9 1%		
	C9774 0.001uF	TMDS_CLK_CMF		
TMDS_DATA_N<3>	R9776 0	TMDS_DATA_R_N<3>	CRITICAL L9703 90-OHM-300mA 2012H	TMDS_DATA_F_N<3>
TMDS_DATA_P<3>	R9777 0	TMDS_DATA_R_P<3>		TMDS_DATA_F_P<3>
	R9778 49.9 1%	R9779 49.9 1%		
	C9778 0.001uF	TMDS_D3_CMF		
TMDS_DATA_N<4>	R9780 0	TMDS_DATA_R_N<4>	CRITICAL L9704 90-OHM-300mA 2012H	TMDS_DATA_F_N<4>
TMDS_DATA_P<4>	R9781 0	TMDS_DATA_R_P<4>		TMDS_DATA_F_P<4>
	R9782 49.9 1%	R9783 49.9 1%		
	C9782 0.001uF	TMDS_D4_CMF		
TMDS_DATA_N<5>	R9784 0	TMDS_DATA_R_N<5>	CRITICAL L9705 90-OHM-300mA 2012H	TMDS_DATA_F_N<5>
TMDS_DATA_P<5>	R9785 0	TMDS_DATA_R_P<5>		TMDS_DATA_F_P<5>
	R9786 49.9 1%	R9787 49.9 1%		
	C9786 0.001uF	TMDS_D5_CMF		

VGA SYNC BUFFERS

=PP3V3_S0_VGASYNC → U9750 (MC74VHC1G08 SC70)
GPU_V2SYNC → U9750
U9750 → VGA_VSYNC_R → R9750 33 → VGA_VSYNC
C9750 0.1uF

PLACE R9750 & R9751 CLOSE TO DVI CONNECTOR

=PP3V3_S0_VGASYNC → U9751 (MC74VHC1G08 SC70)
GPU_H2SYNC → U9751
U9751 → VGA_HSYNC_R → R9751 33 → VGA_HSYNC
C9751 0.1uF

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

GPU_B2 (DAC2 Comp)	R9740 75 1%	CRITICAL FL9740 LCFILTER SM-220MHZ-LF	VGA_B
			C9740 3.3pF 0.25% 50V CERM 402
GPU_G2 (DAC2 Y)	R9741 75 1%	CRITICAL FL9741 LCFILTER SM-220MHZ-LF	VGA_G
			C9741 3.3pF 0.25% 50V CERM 402
GPU_R2 (DAC2 C)	R9742 75 1%	CRITICAL FL9742 LCFILTER SM-220MHZ-LF	VGA_R
			C9742 3.3pF 0.25% 50V CERM 402

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

=PP5V_S0_DVI_DDC → CRITICAL F9710 0.5AMP-13.2V SM-LF → PP5V_S0_DDC_F
L9710 400-OHM-EMI SM-1 → PP5V_S0_DDC
VOLTAGE=5V MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm

DVI INTERFACE

Isolation required for DVI power switch

D9710 SOD-123 B0530WXF
PP5V_S0_DDC_PULLUPS
R9710 4.7K 5%
R9712 4.7K 5%

CRITICAL J9700 QH11121-RIG02-4F F-RT-TH-DVI

=GND_CHASSIS_DVI1		
TMDS_DATA_F_N<0>	17	1 TMDS_DATA_F_N<2>
	9	TMDS_DATA_F_N<1>
TMDS_DATA_F_P<0>	18	2 TMDS_DATA_F_P<2>
	10	TMDS_DATA_F_P<1>
	19	3
		11
TMDS_DATA_F_N<5>	20	4 TMDS_DATA_F_N<4>
		12 TMDS_DATA_F_N<3>
TMDS_DATA_F_P<5>	21	5 TMDS_DATA_F_P<4>
		13 TMDS_DATA_F_P<3>
	22	6 DVI_DDC_CLK_R
		14 (PP5V_S0_DDC)
TMDS_CLK_F_P	23	7 DVI_DDC_DATA_R
		15
TMDS_CLK_F_N	24	8 VGA_VSYNC
		16 DVI_HPD_R
VGA_B	C3	C1 VGA_R
	C5B	C5A
VGA_HSYNC	C4	C2 VGA_G
	34	32
=GND_CHASSIS_DVI2		

514-0278

C9711 100pF 5% 50V CERM 402 (DVI_DDC_CLK)
C9713 100pF 5% 50V CERM 402 (DVI_DDC_DATA)
C9714 100pF 5% 50V CERM 402 (DVI_HPD)
C9710 0.01uF 20% 50V CERM 603

PLACE NEAR C5A & C5B
R9730 0 5% 1/10W MF-LF 402
R9731 0 5% 1/10W MF-LF 402 → =GND_CHASSIS_DVI4

PLACE NEAR 3, 11 & 19

=GND_CHASSIS_DVI3

3V LEVEL SHIFTERS

=PP3V3_S0_DDC_DVI

DVI_DDC_CLK	Q9711 2N7002DW-X-F SOT-363	GPU_DDC_A_CLK
DVI_DDC_DATA	Q9711 2N7002DW-X-F SOT-363	GPU_DDC_A_DATA
DVI_HPD	Q9714 2N7002DW-X-F SOT-363	GPU_HPD

R9720 10K 5% 1/16W MF-LF 402
R9721 10K 5% 1/16W MF-LF 402
R9722 100K 5% 1/16W MF-LF 402
R9715 20K 5% 1/16W MF-LF 402

NET_TYPE		
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL
	TMDS	TMDS_CLK_R_P
	TMDS	TMDS_CLK_R_N
	TMDS	TMDS_DATA_R_P<5..0>
	TMDS	TMDS_DATA_R_N<5..0>
	TMDSCONN	TMDS_CLK_F_P
	TMDSCONN	TMDS_CLK_F_N
	TMDSCONN	TMDS_DATA_F_P<5..0>
	TMDSCONN	TMDS_DATA_F_N<5..0>

External Display Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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Secure Signal List

Nets must be buried with no exposed vias between parts listed in SECURE_NET property. No test points allowed between the secure devices, test points are allowed past the secure devices except on nets marked as NO_TEST=TRUE, no test points are allowed on those nets.

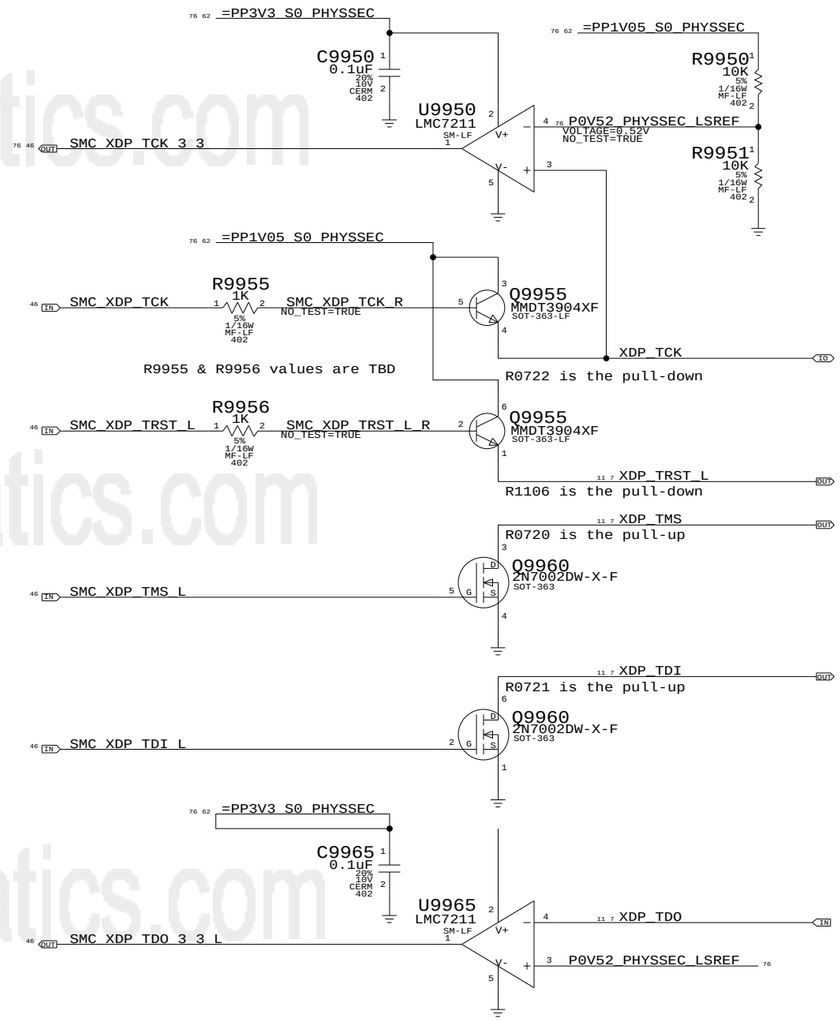
SECURE_NET=U2100:U5800		SPI_CE_L	22 46 51
SECURE_NET=U2100:U5800		SPI_SO	22 46 51
SECURE_NET=U2100:U5800		SPI_SI	22 46 51
SECURE_NET=U2100:U5800	NO_TEST=TRUE	SPI_ARB	22 46
SECURE_NET=U5800:U7530		BOOT_LPC_SPI_L	5 22 46 48
SECURE_NET=U5800:U7530		IMVP_VR_ON	46 56
SECURE_NET=U0700:U9950:Q9955		XDP_TCK	7 11 76
SECURE_NET=U9950:U5800		SMC_XDP_TCK_3_3	46 76
SECURE_NET=U5800:R9955		SMC_XDP_TCK_L	
SECURE_NET=R9955:Q9955		SMC_XDP_TCK_L_R	

NEED TO TURN PCI_GNT3_L INTO A NC NET!

SMC <-> CPU JTAG Level-Shifting

ALL OF THESE PARTS WILL BE COVERED IN EPOXY

Place these parts on one side and as close together as possible, and keep enough room from other parts to leave room for epoxy covering. Nets that are local to this circuit do not need test points as they will not be accessible.



Physical Security

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT	OF
NONE	76	81

Date - Radar # - Description

DMS Release #03000 (RFA #394758)

2005/08/11 - 4214109 - Changed J4931 to proper 518S0342 part.
2005/08/12 - 4231030 - Changed pinout of J4960, added placement notes.

Changes from Proto Branch (DMS Release #04000):

2005/08/27 - 4230219 - Changed Y3301 to non-obsoleted part.
2005/08/27 - 4235208 - Changed value of R7707 to fix 2.5V S3 supply.
2005/08/27 - 4235213 - Changed R8305, R8310, R8315 to slow down FET RCs.
2005/08/27 - 4235401 - Moved a few pins at LIO BTB connector.
2005/08/27 - 4227325 - Removed S0 option for camera, now S3-only.
2005/08/27 - 4227369 - Removed SMC options for display/backlight, now GPU-only.
2005/08/27 - 4225433 - Changed PBUS voltage sense circuit.
2005/08/28 - 4217535 - Added Left ALS FFC connector.
2005/08/28 - 4232563 - Changed analog video from Y/C/Comp to G2/R2/B2.
2005/08/28 - 4235203 - Changed BOM settings to stuff R2251.
2005/08/28 - 4217524 - Added LEFT ALS connector (J6430).
2005/08/28 - 4217535 - OMITs and tables to change 4-pin WTB connector parts.
2005/08/28 - 4221973 - Added pull-up for SB GPIO22 (REQ4#).
2005/08/28 - 4225369 - Changed ISL6269 PVCC aliases, added RC for 3.3V S5.
2005/08/28 - 4225433 - Changed PBUS Voltage Sense circuit.
2005/08/28 - 4227322 - Changed FW323 PCI_VIOS pin from 3.3V S0 to 3.3V S3.
2005/08/28 - 4235179 - OMIT and table to change 8-pin DC-In connector to 6-pin.
2005/08/28 - 4235179 - Changed PBUS net names to merge PBUS A & PBUS B.
2005/08/28 - 4232715 - Added FireWire ISense resistor, changed INA193 to INA194.
2005/08/28 - 4235217 - Added RC on Q3820 gate to slow down ODD FET turn-on.
2005/08/28 - 4225369 - OMITs and tables for staged LeMenu BOM approach.
2005/08/28 - 4227323 - Repinned Top-Case Flex connector.

DMS Checkin #04001

2005/08/29 - 4235179 - Changed J8200 to proper 6-pin part.
2005/08/29 - 4232826 - Changed MEM_ODT* from RPAKs to discrete Rs.
2005/08/29 - 4217524 - Changed R6430 from 4.5K to 3.5K.
2005/08/29 - 4237119 - Changed LIO 5V S3 to 5V S5.
2005/08/29 - 4225369 - Changed 3.3V S5 sequence to follow 5V S5 PGOOD.
2005/08/29 - 4227336 - Changed Y5920 to 197S0169.
2005/08/29 - 4227309 - Resolved sync issues with M38 (SB page 21).
2005/08/29 - 4227310 - Resolved sync issues with M38 (SB page 22).
2005/08/29 - 4227312 - Resolved sync issues with M38 (SB page 23).
2005/08/29 - 4227322 - Sync page 44 with M42 to fix FW power net S-states.
2005/08/29 - 4227332 - Resolved sync issues with M38 (SMC page 58).
2005/08/29 - 4227335 - Changed U5900 to resolve ROHS issue.

DMS Checkin #04002

2005/08/30 - 4225433 - Fixed voltage divider values in PBUS VSense circuit.
2005/08/30 - 4217535 - Removed BOM tables and OMITs for new 4-pin WTB connector.
2005/08/31 - 4214109 - Reversed pinout of J4931 to match updated PCB footprint.
2005/08/31 - 4227328 - Added ESD protection diode on right USB port.
2005/08/31 - 4223808 - Various power supply R/C updates, plus some R/C adds.
2005/08/31 - 4227315 - Changed BSA bus pull-ups from 2K to 10K.
2005/08/31 - 4237025 - Added R8824 and R8827 for GPU memory configuration straps.

DMS Checkin #04003

2005/08/31 - 4240157 - Corrected pinout at SATA/BT conn (J4960) to match flex.
2005/08/31 - 4240150 - Swapped PCIE Mini Card R2D/D2R connections at J5500.
2005/08/31 - 4232563 - Corrected net properties on R2/G2/B2 nets.
2005/08/31 - 4227306 - Swapped primary & alt part numbers for CPU VCore caps.
2005/08/31 - 4240300 - Changed C6455 to a smaller part for cost & MCO.
2005/08/31 - 4240486 - Power line width & neck reductions at PCB request.
2005/08/31 - 4240257 - Swapped some top & bottom EMC connections at DVI connector.

DMS Checkin #04004

2005/08/31 - 4227328 - Changed EMI caps from 50V to 16V to fid in ESD protection.

DMS Checkin #04005

2005/09/02 - 4241087 - Fixed pinout of USB D+/D- at camera connector to match FHB.
2005/09/02 - 4243269 - Inverted GPU VCore control, adjusted supply R values.
2005/09/02 - 4244019 - Moved GPU-related power alias from PP3V3_S0 to PP3V3_S0_GPU.
2005/09/02 - 4240486 - Adjusted line/neck widths, changed J4931 to 518S0371.

DMS Checkin #04006

2005/09/03 - 4232534 - Fixed documentation of battery address on I2C page.
2005/09/03 - 4244484 - Changed P1V5S0_RUNSS circuit to work properly in G3Hot.
2005/09/03 - 4244539 - Added GPUVCORE_PGOOD to 1.2V, 1.8V, & 2.5V S0 sequence.
2005/09/03 - 4227315 - Changed SMBus pull-ups to 4.7K.
2005/09/03 - 4232534 - Added notes for power supplies and connectors.

DMS Checkin #04007

2005/09/06 - 4240486 - Removed NO_TEST property from GPU HSYNC and VSYNC.
2005/09/06 - 4246683 - Removed NO_STUFF option from R8805 per ATI request.
2005/09/06 - 4232534 - Fixed label BOM tables to call out proper EEE #'s.

DMS Release #05000-07000 (Proto 2 releases)

2005/09/08 - 4247941 - Net property & name changes to support PCB/ICT requests.
2005/09/08 - 4248911 - Sync with M38 & M42
2005/09/08 - 4214493 - Combined RTC coin cell diodes into dual-diode package.
2005/09/08 - 4229560 - First implementation of Physical Security Guidelines.
2005/09/16 - 4256660 - Updated FUNC_TEST property for merged PBUS.
2005/09/16 - 4229560 - Changed FW PCI REQ/GNT pair for Physical Security.
2005/09/20 - 4214847 - Updated L1970 (old part no longer exists in library).
2005/09/26 - 4239505 - Updated J4200 (old part no longer exists in library).
2005/09/26 - 4274915 - Thermal sensor BOM updates from Proto 2 MLB branch.
2005/09/26 - 4274915 - U6301 part number updated to M1 development BootROM.

Revision History

SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE	SHT	OF
NONE	77	81

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
FSB_ADDR	*	=3:1_SPACING
FSB_ADDR2ADDR	*	=2:1_SPACING
FSB_ADSTB	*	=3:1_SPACING
FSB_ADDR2ADSTB	*	=3:1_SPACING

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
FSB_DATA	*	=3:1_SPACING
FSB_DATA2DATA	*	=2:1_SPACING
FSB_DSTB	*	=3:1_SPACING
FSB_DATA2DSTB	*	=3:1_SPACING

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
FSB_COMMON	*	=2:1_SPACING

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 3:1, even in constraint areas.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
CPU_2TO1	*	=2:1_SPACING
CPU_COMP	*	25 MIL
CPU_GTLREF	*	25 MIL
CPU_ITP	*	=2:1_SPACING
CPU_VCCSENSE	*	25 MIL

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.4, 4.6.2, & 5.8.2.4

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	Y	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	Y	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
MEM_CLK2MEM	*	=4:1_SPACING
MEM_CTRL2CTRL	*	=2:1_SPACING
MEM_CTRL2MEM	*	=3:1_SPACING
MEM_CMD2CMD	*	=1.5:1_SPACING
MEM_CMD2MEM	*	=3:1_SPACING
MEM_DATA2DATA	*	=1.5:1_SPACING
MEM_DATA2MEM	*	=3:1_SPACING
MEM_DQS2MEM	*	=3:1_SPACING
MEM_2OTHER	*	25 MIL

Need to support MEM_*-style wildcards!

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 6.2

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
PCIE	*	20 MIL
DMI	*	20 MIL

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 7.2, 9.2 & 10.5.2

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
IDE	*	=1.8:1_SPACING
SATA	*	20 MIL

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 10.6 & 10.7.2

Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIO_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
AUDIO	*	=1.8:1_SPACING

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB2_90D	*	Y	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
USB2	*	=4:1_SPACING
USB2_2CLK	*	25 MIL

DG says minimum spacing 50 mils to clocks

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.10.1.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
SMB	*	=3:1_SPACING
SPI	*	=1.8:1_SPACING

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.17.1.1

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
CLK_FSB	*	25 MIL
CLK_PCIE	*	20 MIL
CLK_MED	*	20 MIL
CLK_SLOW	*	10 MIL

Napa Platform Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	78	81

GDDR3 (Frame Buffer) Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FB_35S_TO_55S	*	Y	=35_OHM_SE	=55_OHM_SE	=35_55_OHM_SE	=STANDARD	=STANDARD
FB_40S	*	Y	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
FB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FB_75D	*	Y	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
FB_ADCTRL	*	=2.5:1_SPACING
FB_CLK	*	=2.5:1_SPACING
FB_DATA	*	=2.5:1_SPACING

ADDR/CTRL lines should route 35-ohms to T, then 55-ohms to each VRAM device.
CTRL lines are 55-ohm single-ended impedence.
DQ/DQM/DQS lines are 40-ohm single-ended impedence.

NOTE: CLK lines are specified in Layout Guide as 40-ohm single-ended. We treat as 75-ohm differential.
NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TMDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_75S	*	Y	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
LVDS	*	=3:1_SPACING
TMDS	*	=3:1_SPACING
VGA	*	15 MIL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
LVDS_PAIR2PAIR	*	25 MIL
TMDS_PAIR2PAIR	*	25 MIL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	LVDS	*	LVDS_PAIR2PAIR
TMDS	TMDS	*	TMDS_PAIR2PAIR

LVDS and TMDS signals are 100-ohm +/- 10% differential impedence.
LVDS and TMDS pairs should be kept at least 25 mils apart.
Ground shields can be used around each pair if spacing cannot be met.
VGA should be routed as close to 75-ohms single-ended impedence as possible.
VGA signals should be kept at least 15 mils from other traces.
Ground shields recommended around VGA signals.

NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

High-Speed I/O Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
FW_110D	*	Y	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
ENET	*	=3:1_SPACING
FW	*	=3:1_SPACING

note

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
PCI	*	=2:1_SPACING

More System Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	79	81

M1 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	12.7 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.124 MM	0.124 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.131 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.230 MM			
35_OHM_SE	*	Y	0.165 MM	0.165 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_55_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.100 MM			
35_55_OHM_SE	*	Y	0.165 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

Unsupported rule

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	0.149 MM	0.149 MM	=STANDARD	0.125 MM	0.125 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_DIFF	*	Y	0.131 MM	0.131 MM	=STANDARD	0.125 MM	0.125 MM
75_OHM_DIFF	TOP,BOTTOM	Y	0.161 MM	0.161 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.115 MM	0.111 MM	=STANDARD	0.125 MM	0.125 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.101 MM	0.101 MM	=STANDARD	0.125 MM	0.125 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.102 MM	0.102 MM	=STANDARD	0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.080 MM	0.080 MM	=STANDARD	0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	Y	0.076 MM	0.076 MM	=STANDARD	0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
DEFAULT	*	0.1 MM
STANDARD	*	=DEFAULT
BGA_P1MM	*	=DEFAULT
BGA_P2MM	*	=DEFAULT
BGA_P3MM	*	=DEFAULT

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FB_CLK	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
1.5:1_SPACING	*	0.15 MM
1.8:1_SPACING	*	0.18 MM
2:1_SPACING	*	0.2 MM
2.5:1_SPACING	*	0.25 MM
3:1_SPACING	*	0.3 MM
4:1_SPACING	*	0.4 MM

Allow 0.1 MM on blind-to-buried via dogbones (layers 2 & 11)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
1.5:1_SPACING	ISL2,ISL11	0.1 MM
1.8:1_SPACING	ISL2,ISL11	0.1 MM
2:1_SPACING	ISL2,ISL11	0.1 MM
2.5:1_SPACING	ISL2,ISL11	0.1 MM
3:1_SPACING	ISL2,ISL11	0.1 MM
4:1_SPACING	ISL2,ISL11	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
CLK_FSB	ISL2,ISL11	0.1 MM
CLK_PCIE	ISL2,ISL11	0.1 MM
CLK_MED	ISL2,ISL11	0.1 MM
CLK_SLOW	ISL2,ISL11	0.1 MM
CPU_COMP	ISL2,ISL11	0.1 MM
CPU_GTLREF	ISL2,ISL11	0.1 MM
CPU_VCCSENSE	ISL2,ISL11	0.1 MM
DMI	ISL2,ISL11	0.1 MM
LVDS_PAIR2PAIR	ISL2,ISL11	0.1 MM
MEM_2OTHER	ISL2,ISL11	0.1 MM
PCIE	ISL2,ISL11	0.1 MM
SATA	ISL2,ISL11	0.1 MM
TMDS_PAIR2PAIR	ISL2,ISL11	0.1 MM
VGA	ISL2,ISL11	0.1 MM

Rules for "Topology #3" for FSB signals, Napa DG tables 4-7 & 4-12.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
FSB_ADDR OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE
FSB_ADDR2ADDR OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE
FSB_ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE
FSB_ADDR2ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
FSB_DATA OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE
FSB_DATA2DATA OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE
FSB_DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE
FSB_DATA2DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS	*	LVDS_100D
TMDS	*	TMDS_100D
TMDSCONN	*	TMDS_100D
VGA	*	VGA_75S

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
MEM_2OTHER OVERRIDE	* OVERRIDE	0.5 MM OVERRIDE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENETCONN	*	*	ENET
TMDSCONN	*	*	TMDS

"Stale" physical / spacing types

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ANALOG	*	*	FSB_COMMON
FSB_P2MM	*	*	FSB_COMMON
I2C	*	*	SMB
GND	*	*	STANDARD
MEM_PP1V8_S3	*	*	STANDARD
FB_PP1V8	*	*	STANDARD

FSB_ANALOG
FSB_P2MM
I2C
GND
MEM_PP1V8_S3
FB_PP1V8
PCI PCI_55S

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

M1 Spacing & Physical Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	80	81

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	FSB_55S	FSB_COMMON	FSB_ADS_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_BNR_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_BPRI_L	7 12
	FSB_55S	FSB_COMMON	FSB_BREQ0_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DBSY_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DEFER_L	7 12
	FSB_55S	FSB_COMMON	FSB_DPWR_L	7 12
	FSB_55S	FSB_COMMON	FSB_DRDY_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_HIT_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_HITM_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_LOCK_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	7 12
	FSB_55S	FSB_COMMON	FSB_TRDY_L	7 12
	FSB_55S	FSB_COMMON	FSB_CPURST_L	7 11 12 47
	FSB_55S	FSB_DATA	FSB_D_L<63..0>	5 7 12
	FSB_55S	FSB_DATA	FSB_DINV_L<3..0>	5 7 12
	FSB_55S	FSB_DSTB	FSB_DSTBP_L<3..0>	5 7 12
	FSB_55S	FSB_DSTB	FSB_DSTBN_L<3..0>	5 7 12
	FSB_55S	FSB_ADDR	FSB_A_L<31..3>	5 7 12
	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	5 7 12
	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<3..0>	5 7 12
	CPU_55S		FSB_IERR_L	7
	CPU_55S		FSB_FERR_L	
	CPU_55S		CPU_PWRGD	7 21
	CPU_55S		CPU_INTR	7 21
	CPU_55S		CPU_NMI	7 21
	CPU_55S		CPU_A20M_L	7 21
	CPU_55S		CPU_DPSLP_L	7 21
	CPU_55S		CPU_IGNNE_L	7 21
	CPU_55S		CPU_INIT_L	7 21
	CPU_55S		CPU_SMI_L	7 21
	CPU_55S		CPU_STPCLK_L	7 21
	CPU_55S	CPU_2TO1	CPU_THERMTRIP_L	
	CPU_55S	CPU_2TO1	PM_DPRSLPVR	14 23 56
	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	56
	CPU_55S	CPU_GTLREF	CPU_GTLREF	7
	CPU_55S	CPU_COMP	CPU_COMP<3>	7
	CPU_27P4S	CPU_COMP	CPU_COMP<2>	7
	CPU_55S	CPU_COMP	CPU_COMP<1>	7
	CPU_27P4S	CPU_COMP	CPU_COMP<0>	7
	CPU_55S	CPU_ITP	XDP_BPM_L<5..0>	7 11
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_P	11 34
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_N	11 34
	CPU_55S	CPU_ITP	ITPRESET_L	11
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8 9 81
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8 9 81
	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 56
	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	8 56
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	56
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	56

	MEM_CLK	MEM_70D
	MEM_CTRL	MEM_45S
	MEM_CMD	MEM_55S
	MEM_DATA	MEM_55S
	MEM_DQS	MEM_85D
	FB_CLK	FB_75D
	FB_ADCTRL	FB_35S_TO_55S
	FB_ADCTRL	FB_55S
	FB_DATA	FB_40S
	LVDS	LVDS_100D
	TMDS	TMDS_100D
	VGA	VGA_75S
	PCIE	PCIE_100D
	DMI	DMI_100D
	SATA	SATA_100D
	IDE	IDE_55S
	USB2	USB2_90D
	ENET	ENET_100D
	FW	FW_110D
	SMB	SMB_55S
	SPI	SPI_55S
	CLK_FSB	CLK_FSB_100D
	CLK_PCIE	CLK_PCIE_100D
	CLK_MED	CLK_MED_55S
	CLK_SLOW	CLK_SLOW_55S

	AUDIO_55S	AUDIO	SB_ACZ_BITCLK	21
	AUDIO_55S	AUDIO	ACZ_BITCLK	5 21 44
	AUDIO_55S	AUDIO	SB_ACZ_SYNC	21
	AUDIO_55S	AUDIO	ACZ_SYNC	5 21 44
	AUDIO_55S	AUDIO	SB_ACZ_RST_L	21
	AUDIO_55S	AUDIO	ACZ_RST_L	5 21 44
	AUDIO_55S	AUDIO	ACZ_SDATAIN<0>	5 21 44
	AUDIO_55S	AUDIO	SB_ACZ_SDATAOUT	21
	AUDIO_55S	AUDIO	ACZ_SDATAOUT	5 21 44

	TMDS	TMDS	TMDS_CLK_P	73 74 75
	TMDS	TMDS	TMDS_CLK_N	73 74 75
	TMDS	TMDS	TMDS_DATA_P<5..3>	73 74 75
	TMDS	TMDS	TMDS_DATA_N<5..3>	73 74 75
	TMDS	TMDS	TMDS_DATA_P<2..0>	73 74 75
	TMDS	TMDS	TMDS_DATA_N<2..0>	73 74 75
	TMDSCONN	TMDSCONN	TMDS_CLK_F_P	75
	TMDSCONN	TMDSCONN	TMDS_CLK_F_N	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..3>	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..3>	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_P<2..0>	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_N<2..0>	75

M1 Net Properties

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	81	81