1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
?		?	?	?	?

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TITLE=M72
ABBREV=DRAWING
LAST_MODIFIED=Tue Jan 8 14:42:38 2008

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

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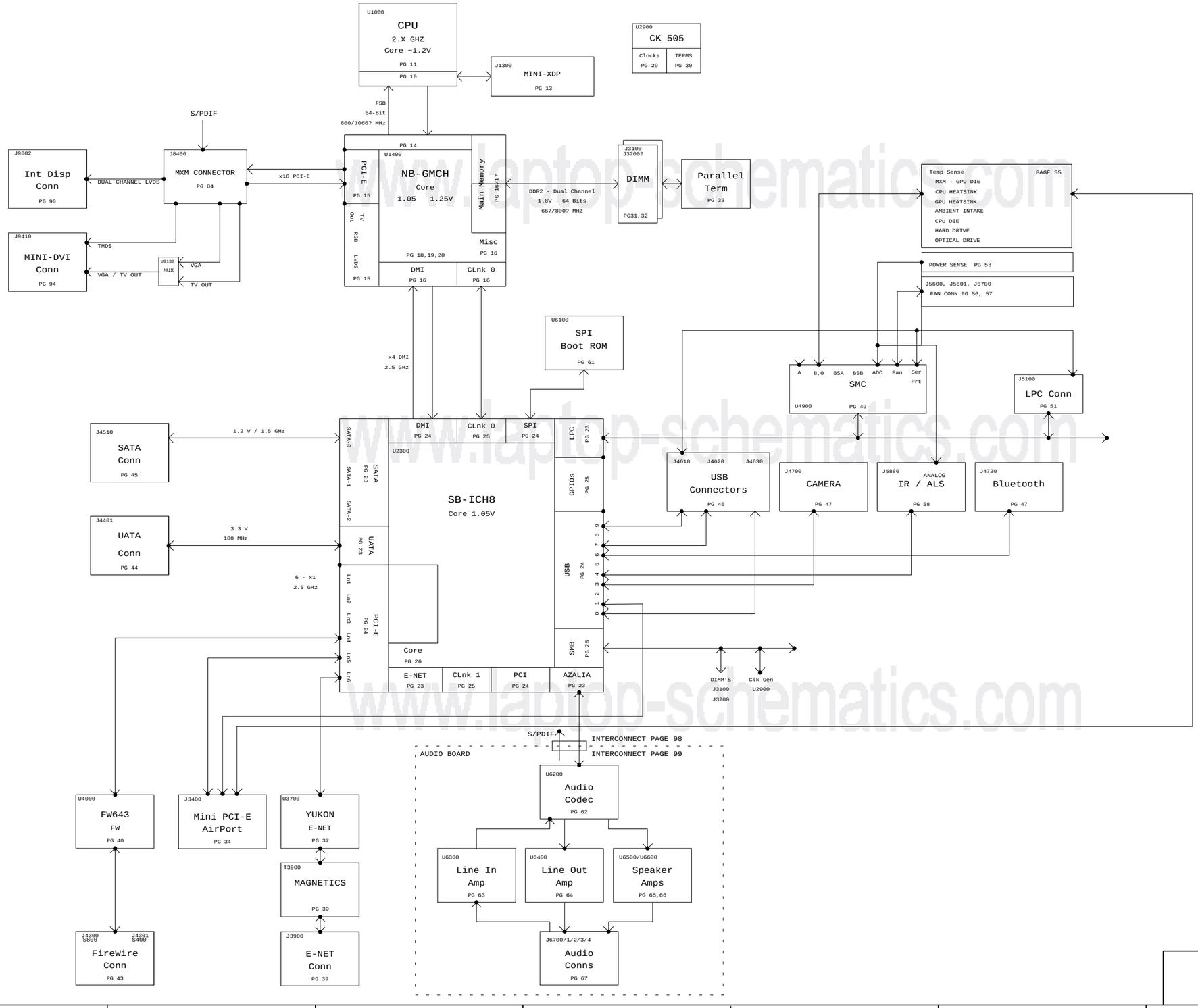

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System Block Diagram

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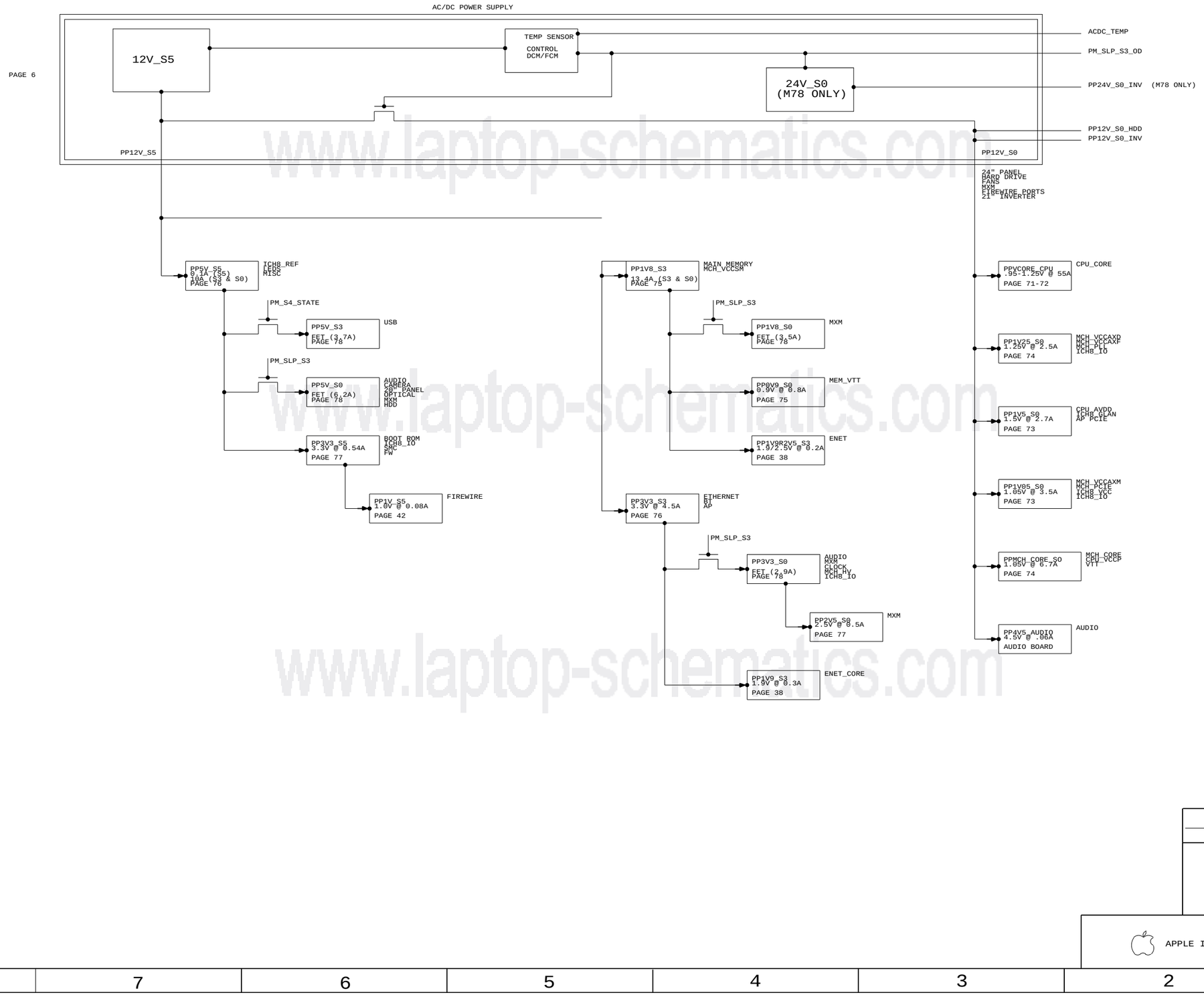

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Power Block Diagram

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Revision History

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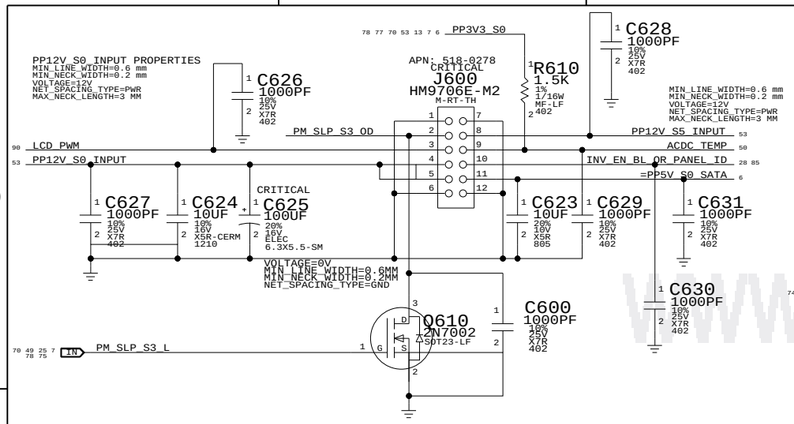


"S0" RAILS

ONLY ON IN RUN

- PP0V9_S0 → =PP0V9_S0M_MEM_TERM
- PPVCORE_CPU → =PPVCORE_S0_CPU
- PP1V8_S0 → =PP1V8_S0_MXM
- PP2V5_S0 → =PP2V5_S0_MXM
- PPMCH_CORE_S0 → =PPVCORE_S0_NB
- PP1V05_S0 → =PP1V05_S0_CPU, =PP1V25R1V05_S0_FSB_NB, =PP1V25R1V05_S0_NB_VTT, =PP1V05_S0_SB_CPU_IO
- PP1V05_S0 → =PP1V05_S0M_NB_VCCAXM, =PP1V05_S0_NB_PCIE, =PP1V05_S0_NB_FOLLOW, =PPVCORE_S0_SB
- PP1V5_S0 → =PP1V5_S0_CPU, =PP1V5_S0_NB_TVDAC, =PP1V5_S0_SB_VCC1_5_A_ARX, =PP1V5_S0_SB_VCC1_5_A_ATX, =PP1V5_S0_SB_VCCUSBPLL, =PP1V5_S0_SB_VCC1_5_A_USB_CORE, =PP1V5_S0_SB_VCC1_5_A, =PP1V5_S0_SB, =PP1V5_S0_MINI
- PP1V25_S0 → =PP1V25_S0_NB_VCCDMI, =PP1V25_S0M_NB_VCCA, =PP1V25_S0M_NB_VCC, =PP1V25_S0_NB_PLL, =PP1V25_S0_NB_VCC, =PP1V25_S0M_NB_PLL, =PP1V25_S0_SB_DMI
- PP3V3_S0 → =PP3V3_S0_NB_VCCHV, =PP3V3_S0_SB, =PP3V3_S0_SB_GPIO, =PP3V3_S0_SB_VCCGLAN3_3, =PP3V3_S0_SB_VCC3_3_PCI, =PP3V3_S0_SB_VCC3_3_IDE, =PP3V3_S0_SB_PCI, =PP3V3_S0_SB_PM, =PP3V3_S0_PATA, =PP3V3_S0_FAN, =PPSPD_S0_MEM, =PP3V3_S0_IMVP, =PP3V3_S0_AUDIO, =PP3V3_S0_LPCPLUS, =PP3V3_S0_SMBUS_SB, =PP3V3_S0_SMC_LS, =PP3V3_S0_SMBUS_SMC_0_S0, =PP3V3_S0_SMBUS_SMC_B_S0, =PP3V3_S0_SMBUS_SMC_MGMT, =PP3V3_S0_CK505, =PP3V3_S0_MXM, =PP3V3_S0_SATALED, =PP3V3_S0M_CK505, =PP3V3_S0MWOL_SB_CLINK0, =PP3V3_S0_SB_VCC3_3_DMI, =PP3V3_S0_SB_VCC3_3_SATA, =PP3V3_S0_SB_VCC3_3_VCCPCORE, =PP3V3R1V5_S0_SB_VCCHDA, =PP3V3_S0MWOL_SB_VCCLAN3_3, =PP3V3_S0MWOL_SB_VCCCL3_3, =PP3V3_S0_TSENS, =PP3V3_S0_SMC, =PP3V3_S0_NB_VCCA_PEG_BG, =PP3V3_S0_NB_FOLLOW, =PP3V3_S0_VIDEO, =PP3V3_S0_ENET
- PP5V_S0 → =PP5V_S0_SB, =PP5V_S0_PATA, =PP5V_S0_LPCPLUS, =PP5V_S0_AUDIO, =PP5V_S0_SATA, =PP5V_S0_MXM, =PPV_S0_LCD_20INCH
- PP12V_S0 → =PP12V_S0_FAN, =PP12V_S0_AUDIO_SPKRAMP, =PP12V_S0_CPU, =PPV_S0_LCD_24INCH, =PPV_S0_MXM_PWRSRC

"S3" RAILS

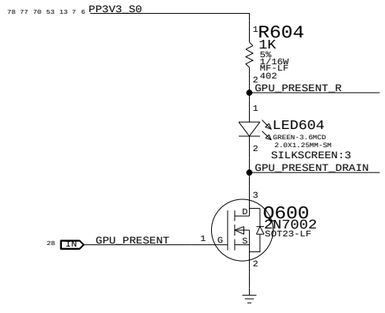
ON IN RUN AND SLEEP

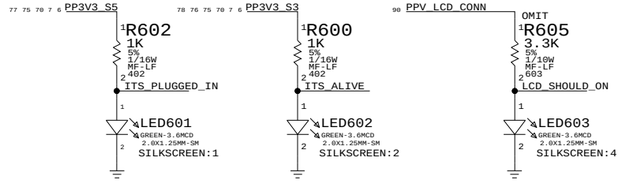
- PP1V8_S3 → =PP1V8_S3M_MEM_NB, =PP1V8_S3M_NB_VCC, =PP1V8_S3_MEM, =PP1V8_S3_MEMVTT, =PP1V8_S3_ENET
- PP3V3_S3 → =PP3V3_S3_MINI, =PP3V3_S3_ENET, =PP3V3_S3_BT
- PP5V_S3 → =PP5V_S3_BNDI, =PP5V_S3_MEMVTT

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

- PP3V3_S5 → =PP3V3_S5_SB, =PP3V3_S5_SB_USB, =PP3V3_S5_SB_PM, =PP3V3_S5_SB_VCCSUS3_3, =PP3V3_S5_SB_VCCSUS3_3_USB, =PP3V3_S5_SMBUS_SB_ME, =PP3V3_S5_FW, =PP3V3_S5_SMC, =PP3V3_S5_ROM, =PP3V3_S5_SB_GPIO, =PP3V3_S5_SB_CLINK1, =PP3V3_S5_SB_3V3_VCCSUSHDA, =PP3V3_S5_LPCPLUS, =PP3V3_S5_SMBUS_SMC_BSA, =PP3V3_S5_FAN, =PP3V3_S5_SMCUSBMUX, =PP3V3_S5_SMBUS_SMC_A_S5
- PP5V_S5 → =PP5V_S5_SB, =PPVIN_S5_SMCVREF, =PP5V_S5_USB
- PP12V_S5 → =PP12V_S5_FET, =PP12V_S5_FW





PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0082	1	RES,MF,1/10W,910OHM,5,0603,SMD,LF	R605		20_INCH_LCD
113S0095	1	RES,MF,1/10W,3.3KOHM,5,0603,SMD,LF	R605		24_INCH_LCD

Power Conn / Alias

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FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT

LAYOUT NOTE: PLACE NEAR J1000

100 14 10 7	FSB_A_L<6>	PP1000	OMIT	P4MM
100 14 10 7	FSB_ADSTB_L<0>	PP1001	OMIT	P4MM
100 14 10 7	FSB_A_L<27>	PP1002	OMIT	P4MM
100 14 10 7	FSB_ADSTB_L<1>	PP1003	OMIT	P4MM
100 14 10 7	FSB_D_L<0>	PP1004	OMIT	P4MM
100 14 10 7	FSB_DSTB_L_N<0>	PP1005	OMIT	P4MM
100 14 10 7	FSB_DSTB_L_P<0>	PP1006	OMIT	P4MM
100 14 10 7	FSB_DINV_L<0>	PP1007	OMIT	P4MM
100 14 10 7	FSB_D_L<16>	PP1008	OMIT	P4MM
100 14 10 7	FSB_DSTB_L_N<1>	PP1009	OMIT	P4MM
100 14 10 7	FSB_DSTB_L_P<1>	PP1010	OMIT	P4MM
100 14 10 7	FSB_DINV_L<1>	PP1011	OMIT	P4MM
100 14 10 7	FSB_D_L<41>	PP1012	OMIT	P4MM
100 14 10 7	FSB_DSTB_L_N<2>	PP1013	OMIT	P4MM
100 14 10 7	FSB_DSTB_L_P<2>	PP1014	OMIT	P4MM
100 14 10 7	FSB_DINV_L<2>	PP1015	OMIT	P4MM
100 14 10 7	FSB_D_L<59>	PP1016	OMIT	P4MM
100 14 10 7	FSB_DSTB_L_N<3>	PP1017	OMIT	P4MM
100 14 10 7	FSB_DSTB_L_P<3>	PP1018	OMIT	P4MM
100 14 10 7	FSB_DINV_L<3>	PP1019	OMIT	P4MM
100 14 10 7	FSB_LOCK_L	PP1020	OMIT	P4MM
100 14 13 10	FSB_CPURST_L	PP1021	OMIT	P4MM
100 51 23 10	CPU_INIT_L	PP1022	OMIT	P4MM
100 23 10	CPU_A20M_L	PP1023	OMIT	P4MM
100 23 10	CPU_IGNNE_L	PP1024	OMIT	P4MM
100 23 10	CPU_STPCLK_L	PP1025	OMIT	P4MM
100 23 10	CPU_INTR	PP1026	OMIT	P4MM
100 23 10	CPU_NMI	PP1027	OMIT	P4MM
100 23 10	CPU_SMI_L	PP1028	OMIT	P4MM
100 14 10 7	FSB_REQ_L<0>	PP1029	OMIT	P4MM
100 14 10 7	FSB_REQ_L<1>	PP1030	OMIT	P4MM
100 14 10 7	FSB_REQ_L<2>	PP1031	OMIT	P4MM
100 14 10 7	FSB_REQ_L<3>	PP1032	OMIT	P4MM
100 14 10 7	FSB_REQ_L<4>	PP1033	OMIT	P4MM
105 30 10	FSB_CLK_CPU_P	PP1034	OMIT	P4MM
105 30 10	FSB_CLK_CPU_N	PP1035	OMIT	P4MM

LAYOUT NOTE: PLACE NEAR U2100

105 30 23	SB_CLK100M_SATA_P	PP2100	OMIT	P4MM
105 30 23	SB_CLK100M_SATA_N	PP2101	OMIT	P4MM
103 44 23	IDE_PDIOR_L	PP2102	OMIT	P4MM
103 44 23	IDE_PDIORDY	PP2103	OMIT	P4MM
103 44 23	IDE_PDD<9>	PP2104	OMIT	P4MM
104 34 24	PCIE_MINI_D2R_P	PP2105	OMIT	P4MM
104 34 24	PCIE_MINI_D2R_N	PP2106	OMIT	P4MM
104 37 24	PCIE_ENET_D2R_P	PP2107	OMIT	P4MM
104 37 24	PCIE_ENET_D2R_N	PP2108	OMIT	P4MM
104 42 40	PCIE_FW_D2R_P	PP2132	OMIT	P4MM
104 42 40	PCIE_FW_D2R_N	PP2133	OMIT	P4MM
101 24 16	DMI_N2S_P<0>	PP2109	OMIT	P4MM
101 24 16	DMI_N2S_N<0>	PP2110	OMIT	P4MM
105 30 24	SB_CLK100M_DMI_P	PP2111	OMIT	P4MM
105 30 24 7	SB_CLK100M_DMI_N	PP2112	OMIT	P4MM
49 28 25	PM_SYSRST_L	PP2113	OMIT	P4MM
51 49 25 7	PM_CLKRUN_L	PP2114	OMIT	P4MM
105 30 25	SB_CLK14P3M_TIMER	PP2115	OMIT	P4MM
105 30 25	SB_CLK48M_USBCTLR	PP2116	OMIT	P4MM
105 30 24	PCI_CLK33M_SB	PP2117	OMIT	P4MM
28 23	SB_RTC_RST_L	PP2118	OMIT	P4MM
103 45 23	SATA_A_D2R_P	PP2119	OMIT	P4MM
103 45 23	SATA_A_D2R_N	PP2120	OMIT	P4MM
51 49 23 7	LPC_AD<1>	PP2121	OMIT	P4MM
103 47 24	USB_CAMERA_P	PP2122	OMIT	P4MM
103 47 24	USB_CAMERA_N	PP2123	OMIT	P4MM
103 47 24	USB_IR_P	PP2124	OMIT	P4MM
103 47 24	USB_IR_N	PP2125	OMIT	P4MM
103 47 24	USB_BT_P	PP2126	OMIT	P4MM
103 47 24	USB_BT_N	PP2127	OMIT	P4MM
103 61	SPI_SCLK	PP2128	OMIT	P4MM
103 61 24	SPI_SO	PP2129	OMIT	P4MM
104 25 16 7	CLINK_NB_CLK	PP2130	OMIT	P4MM
104 25 16 7	CLINK_NB_DATA	PP2131	OMIT	P4MM

LAYOUT NOTE: PLACE NEAR U1400

100 14 10 7	FSB_A_L<6>	PP1400	OMIT	P4MM
100 14 10 7	FSB_ADSTB_L<0>	PP1401	OMIT	P4MM
100 14 10 7	FSB_A_L<27>	PP1402	OMIT	P4MM
100 14 10 7	FSB_ADSTB_L<1>	PP1403	OMIT	P4MM
100 14 10 7	FSB_D_L<0>	PP1404	OMIT	P4MM
100 14 10 7	FSB_DSTB_L_N<0>	PP1405	OMIT	P4MM
100 14 10 7	FSB_DSTB_L_P<0>	PP1406	OMIT	P4MM
100 14 10 7	FSB_DINV_L<0>	PP1407	OMIT	P4MM
100 14 10 7	FSB_D_L<16>	PP1408	OMIT	P4MM
100 14 10 7	FSB_DSTB_L_N<1>	PP1409	OMIT	P4MM
100 14 10 7	FSB_DSTB_L_P<1>	PP1410	OMIT	P4MM
100 14 10 7	FSB_DINV_L<1>	PP1411	OMIT	P4MM
100 14 10 7	FSB_D_L<41>	PP1412	OMIT	P4MM
100 14 10 7	FSB_DSTB_L_N<2>	PP1413	OMIT	P4MM
100 14 10 7	FSB_DSTB_L_P<2>	PP1414	OMIT	P4MM
100 14 10 7	FSB_DINV_L<2>	PP1415	OMIT	P4MM
100 14 10 7	FSB_D_L<59>	PP1416	OMIT	P4MM
100 14 10 7	FSB_DSTB_L_N<3>	PP1417	OMIT	P4MM
100 14 10 7	FSB_DSTB_L_P<3>	PP1418	OMIT	P4MM
100 14 10 7	FSB_DINV_L<3>	PP1419	OMIT	P4MM
100 14 10 7	FSB_LOCK_L	PP1420	OMIT	P4MM
100 14 10	FSB_HIT_L	PP1421	OMIT	P4MM
100 14 10	FSB_HITM_L	PP1422	OMIT	P4MM
100 14 10	FSB_BNR_L	PP1423	OMIT	P4MM
100 14 10	FSB_BREQ0_L	PP1424	OMIT	P4MM
100 14 10	FSB_DBSY_L	PP1425	OMIT	P4MM
100 14 10	FSB_DPWR_L	PP1426	OMIT	P4MM
100 14 10 7	FSB_REQ_L<0>	PP1427	OMIT	P4MM
100 14 10 7	FSB_REQ_L<1>	PP1428	OMIT	P4MM
100 14 10 7	FSB_REQ_L<2>	PP1429	OMIT	P4MM
100 14 10 7	FSB_REQ_L<3>	PP1430	OMIT	P4MM
100 14 10 7	FSB_REQ_L<4>	PP1431	OMIT	P4MM
105 30 14	FSB_CLK_NB_P	PP1432	OMIT	P4MM
105 30 14 7	FSB_CLK_NB_N	PP1433	OMIT	P4MM
71 70 22 16 7	VR_PWRGOOD_DELAY	PP1434	OMIT	P4MM
28 16	NB_RESET_L	PP1435	OMIT	P4MM
105 30 16	NB_CLK100M_PCIE_P	PP1436	OMIT	P4MM
105 30 16 7	NB_CLK100M_PCIE_N	PP1437	OMIT	P4MM
101 24 16	DMI_S2N_N<0>	PP1438	OMIT	P4MM
101 24 16	DMI_S2N_P<0>	PP1439	OMIT	P4MM
22 16	=PP0V9_S3M_MEM_NBVREFA	PP1440	OMIT	P4MM
22 16	=PP0V9_S3M_MEM_NBVREFB	PP1441	OMIT	P4MM
102 31 17	MEM_A_DQ<7>	PP1442	OMIT	P4MM
102 31 17	MEM_A_DQ<14>	PP1443	OMIT	P4MM
102 31 17	MEM_A_DQ<16>	PP1444	OMIT	P4MM
102 31 17	MEM_A_DQ<25>	PP1445	OMIT	P4MM
102 31 17	MEM_A_DQ<39>	PP1446	OMIT	P4MM
102 31 17	MEM_A_DQ<47>	PP1447	OMIT	P4MM
102 31 17	MEM_A_DQ<54>	PP1448	OMIT	P4MM
102 31 17	MEM_A_DQ<59>	PP1449	OMIT	P4MM
102 31 17	MEM_A_DQS_P<0>	PP1450	OMIT	P4MM
102 31 17	MEM_A_DQS_N<0>	PP1451	OMIT	P4MM
102 31 17	MEM_A_DQS_P<1>	PP1452	OMIT	P4MM
102 31 17	MEM_A_DQS_N<1>	PP1453	OMIT	P4MM
102 31 17	MEM_A_DQS_P<2>	PP1454	OMIT	P4MM
102 31 17	MEM_A_DQS_N<2>	PP1455	OMIT	P4MM
102 31 17	MEM_A_DQS_P<3>	PP1456	OMIT	P4MM
102 31 17	MEM_A_DQS_N<3>	PP1457	OMIT	P4MM
102 31 17	MEM_A_DQS_P<4>	PP1458	OMIT	P4MM
102 31 17	MEM_A_DQS_N<4>	PP1459	OMIT	P4MM
102 31 17	MEM_A_DQS_P<5>	PP1460	OMIT	P4MM
102 31 17	MEM_A_DQS_N<5>	PP1461	OMIT	P4MM
102 31 17	MEM_A_DQS_P<6>	PP1462	OMIT	P4MM
102 31 17	MEM_A_DQS_N<6>	PP1463	OMIT	P4MM
102 31 17	MEM_A_DQS_P<7>	PP1464	OMIT	P4MM
102 31 17	MEM_A_DQS_N<7>	PP1465	OMIT	P4MM
102 32 17	MEM_B_DQ<6>	PP1466	OMIT	P4MM
102 32 17	MEM_B_DQ<8>	PP1467	OMIT	P4MM
102 32 17	MEM_B_DQ<23>	PP1468	OMIT	P4MM
102 32 17	MEM_B_DQ<25>	PP1469	OMIT	P4MM
102 32 17	MEM_B_DQ<38>	PP1470	OMIT	P4MM
102 32 17	MEM_B_DQ<44>	PP1471	OMIT	P4MM
102 32 17	MEM_B_DQ<48>	PP1472	OMIT	P4MM
102 32 17	MEM_B_DQ<62>	PP1473	OMIT	P4MM
102 32 17	MEM_B_DQS_P<0>	PP1474	OMIT	P4MM
102 32 17	MEM_B_DQS_N<0>	PP1475	OMIT	P4MM
102 32 17	MEM_B_DQS_P<1>	PP1476	OMIT	P4MM
102 32 17	MEM_B_DQS_N<1>	PP1477	OMIT	P4MM
102 32 17	MEM_B_DQS_P<2>	PP1478	OMIT	P4MM
102 32 17	MEM_B_DQS_N<2>	PP1479	OMIT	P4MM
102 32 17	MEM_B_DQS_P<3>	PP1480	OMIT	P4MM
102 32 17	MEM_B_DQS_N<3>	PP1481	OMIT	P4MM
102 32 17	MEM_B_DQS_P<4>	PP1482	OMIT	P4MM
102 32 17	MEM_B_DQS_N<4>	PP1483	OMIT	P4MM
102 32 17	MEM_B_DQS_P<5>	PP1484	OMIT	P4MM
102 32 17	MEM_B_DQS_N<5>	PP1485	OMIT	P4MM
102 32 17	MEM_B_DQS_P<6>	PP1486	OMIT	P4MM
102 32 17	MEM_B_DQS_N<6>	PP1487	OMIT	P4MM
102 32 17	MEM_B_DQS_P<7>	PP1488	OMIT	P4MM
102 32 17	MEM_B_DQS_N<7>	PP1489	OMIT	P4MM
101 84 15	PEG_D2R_P<7>	PP1490	OMIT	P4MM
101 84 15	PEG_D2R_N<7>	PP1491	OMIT	P4MM
104 25 16 7	CLINK_NB_CLK	PP1492	OMIT	P4MM
104 25 16 7	CLINK_NB_DATA	PP1493	OMIT	P4MM

LAYOUT NOTE: PLACE NEAR U3700

105 37 30	PCIE_CLK100M_ENET_P	PP3700	OMIT	P4MM
105 37 30	PCIE_CLK100M_ENET_N	PP3701	OMIT	P4MM
108 37	PCIE_ENET_R2D_P	PP3702	OMIT	P4MM
108 37	PCIE_ENET_R2D_N	PP3703	OMIT	P4MM
37 28	ENET_RESET_L	PP3704	OMIT	P4MM

LAYOUT NOTE: PLACE NEAR U4000

105 40 30	PCIE_CLK100M_FW_P	PP4000	OMIT	P4MM
105 40 30	PCIE_CLK100M_FW_N	PP4001	OMIT	P4MM
108 40	PCIE_FW_R2D_P	PP4002	OMIT	P4MM
108 40	PCIE_FW_R2D_N	PP4003	OMIT	P4MM
40 28	FW_RESET_L	PP4004	OMIT	P4MM

LAYOUT NOTE: PLACE NEAR U4900

105 49 30	PCI_CLK33M_SMC	PP4900	OMIT	P4MM
49 28	SMC_LRESET_L	PP4901	OMIT	P4MM
51 50 49 7	SMC_RESET_L	PP4902	OMIT	P4MM
51 49 23 7	LPC_AD<1>	PP4903	OMIT	P4MM

PP3V3_S3 — C701 0.01UF 10% 50V X7R 402 — C702 0.01UF 10% 50V X7R 402 — C703 0.01UF 10% 50V X7R 402 — C704 0.01UF 10% 50V X7R 402 — PP3V3_S0

LPC CONNECTOR

51 6	=PP3V3_S5_LPCPLUS	FUNC_TEST=TRUE	
51 6	=PP5V_S0_LPCPLUS	FUNC_TEST=TRUE	
51	FWH_INIT_L	FUNC_TEST=TRUE	
105 51 30	PCI_CLK33M_LPCPLUS	FUNC_TEST=TRUE	
51 49 23	LPC_AD<0>	FUNC_TEST=TRUE	
51 49 23 7	LPC_AD<1>	FUNC_TEST=TRUE	
51 49 23	LPC_AD<2>	FUNC_TEST=TRUE	
51 49 23	LPC_AD<3>	FUNC_TEST=TRUE	
51 49 23	LPC_FRAME_L	FUNC_TEST=TRUE	
51 49 25 7	PM_CLKRUN_L	FUNC_TEST=TRUE	
51 24	BOOT_LPC_SPI_L	FUNC_TEST=TRUE	
51 50 49	SMC_TMS	FUNC_TEST=TRUE	
51 28	DEBUG_RESET_L	FUNC_TEST=TRUE	
51 49	SMC_TRST_L	FUNC_TEST=TRUE	
51 50 49	SMC_TDO	FUNC_TEST=TRUE	
51 49	SMC_MD1	FUNC_TEST=TRUE	
51 50 49 46	SMC_TX_L	FUNC_TEST=TRUE	
51 49 25	INT_SERIRQ	FUNC_TEST=TRUE	
51 50 49 25 7	PM_SUS_STAT_L	FUNC_TEST=TRUE	
51 50 49	SMC_TDI	FUNC_TEST=TRUE	
51 50 49	SMC_TCK	FUNC_TEST=TRUE	
51 50 49 7	SMC_RESET_L	FUNC_TEST=TRUE	
51 49	SMC_NMI	FUNC_TEST=TRUE	
51 50 49 46	SMC_RX_L	FUNC_TEST=TRUE	
51 25	LINDACARD_GPIO	FUNC_TEST=TRUE	

16 TP'S

PWROK SEQUENCING

84 70 50 49 7	ALL_SYS_PWRGD	FUNC_TEST=TRUE	
70 28 25 7	PM_SB_PWROK	FUNC_TEST=TRUE	

STARTUP (BOOT/WAKE) TIMING

71 49	IMVP_VR_ON	FUNC_TEST=TRUE	
28 25	VR_PWRGD_CLKEN	FUNC_TEST=TRUE	
71 70 22 16 7	VR_PWRGOOD_DELAY	FUNC_TEST=TRUE	
70 28 25 7	PM_SB_PWROK	FUNC_TEST=TRUE	

SHUTDOWN/SLEEP TIMING

51 50 49 25 7	PM_SUS_STAT_L	FUNC_TEST=TRUE	
78 75 70 49 25 6	PM_SLP_S3_L	FUNC_TEST=TRUE	
78 75 49 46 25 7	PM_S4_STATE_L	FUNC_TEST=TRUE	
84 70 50 49 7	ALL_SYS_PWRGD	FUNC_TEST=TRUE	
100 23 13 10	CPU_PWRGD	FUNC_TEST=TRUE	

"S0" RAILS

75 70 6	PP0V9_S0	FUNC_TEST=TRUE	
72 71 6	PPVCORE_CPU	FUNC_TEST=TRUE	
78 70 6	PP1V8_S0	FUNC_TEST=TRUE	
77 6	PP2V5_S0	FUNC_TEST=TRUE	
74 73 55 6	PPMCH_CORE_S0	FUNC_TEST=TRUE	
73 34 6	PP1V05_S0	FUNC_TEST=TRUE	
74 6	PP1V25_S0	FUNC_TEST=TRUE	
78 77 70 53 13 7 6	PP3V3_S0	FUNC_TEST=TRUE	
94 78 74 73 72 71 70 6	PP5V_S0	FUNC_TEST=TRUE	
76 74 73 53 6	PP12V_S0	FUNC_TEST=TRUE	
73 6	PP1V5_S0	FUNC_TEST=TRUE	

3 TP'S

"S3" RAILS

3 TP'S

78 75 6	PP1V8_S3	FUNC_TEST=TRUE	
78 76 75 70 7 6	PP3V3_S3	FUNC_TEST=TRUE	
78 76 75 70 6	PP5V_S3	FUNC_TEST=TRUE	
78 75 49 46 25 7	PM_S4_STATE_L	FUNC_TEST=TRUE	

"S5" RAILS

3 TP'S

77 75 70 6	PP3V3_S5	FUNC_TEST=TRUE	
78 77 76 70 6	PP5V_S5	FUNC_TEST=TRUE	
76 75 70 53 6	PP12V_S5	FUNC_TEST=TRUE	

5 TP'S

FOR ICT

105 30 16 7	NB_CLK100M_PCIE_N	FUNC_TEST=TRUE	
105 30 14 7	FSB_CLK_NB_N	FUNC_TEST=TRUE	
16	TP_NB_CFG<13>	FUNC_TEST=TRUE	
16	TP_NB_CFG<12>	FUNC_TEST=TRUE	
16	TP_NB_CFG<18>	FUNC_TEST=TRUE	
16	NB_CFG<19>	FUNC_TEST=TRUE	
104 24	PCI_REQ1_L	FUNC_TEST=TRUE	
104 24	PCI_REQ2_L	FUNC_TEST=TRUE	
105 30 24 7	SB_CLK100M_DMI_N	FUNC_TEST=TRUE	
30	TP_CK505_REF1	FUNC_TEST=TRUE	
30	TP_CK505_PCI1_CLK	FUNC_TEST=TRUE	
40	TP_FW_TCK	FUNC_TEST=TRUE	
40	TP_FW_TMS	FUNC_TEST=TRUE	
40	TP_FW_TDI	FUNC_TEST=TRUE	
40	TP_FW_TDO	FUNC_TEST=TRUE	
40	FW_TRST_L	FUNC_TEST=TRUE	
40	TP_FW_SM	FUNC_TEST=TRUE	
40	TP_FW_SE	FUNC_TEST=TRUE	
40	TP_FW_NAND_TREE	FUNC_TEST=TRUE	
40	TP_FW_CE	FUNC_TEST=TRUE	
103 61	SPI_CE_L<0>	FUNC_TEST=TRUE	
103 61	SPI_A_SO_R	FUNC_TEST=TRUE	

MISC GROUND VIAS - NEEDED?

ZH500 ZH510 ZH520
ZH501 ZH511 ZH521
ZH502 ZH512 ZH522
ZH503 ZH513 ZH523
ZH504 ZH514 ZH524
ZH505 ZH515 ZH525
ZH506 ZH516 ZH526
ZH507 ZH517 ZH527
ZH508 ZH518 ZH528
ZH509 ZH519 ZH529
HOLE-VIA

CRITICAL SC0700 EMI-SPRING CLIP-SM1
CRITICAL SC0701 EMI-SPRING CLIP-SM1
CRITICAL SC0702 EMI-SPRING CLIP-SM-K2
BTW DIMMS

998-0845 FOR NB HEATSINK

ZH0722 3P9R3P15 — ZH0723 3P9R3P15 — ZH0724 3P9R3P15 — ZH0725 3P9R3P15

CRITICAL 452-0508 CRITICAL
SDF0726 HSK-NUT-6.5MM TH — SDF0727 HSK-NUT-6.5MM TH

998-0850 FOR CPU HEATSINK

ZH0700 4P75R4 — ZH0701 4P75R4 — ZH0702 4P75R4 — ZH0703 4P75R4

CRITICAL 860-0895
SDF0717 STDOFF-7P0OD15P0H-TH — SDF0721 STDOFF-7P0OD15P0H-TH — SDF0750 STDOFF-7P0OD15P0H-TH — SDF0751 STDOFF-7P0OD15P0H-TH

998-0847

ZH0711 4P25R3P5 — ZH0712 4P25R3P5 — ZH0714 4P25R3P5 — ZH0715 4P25R3P5 — ZH0718 4P25R3P5 — ZH0720 4P25R3P5 — ZH0750 4P25R3P5

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Functional / ICT Test

SYNC_DATE=N/A

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D		A

SCALE	SHT	OF
NONE	7	118

GND RAILS

98 GND_AUDIO_SPKRAMP
VOLTAGE=0V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
NET_SPACING_TYPE=GND

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CHASSIS GND

GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V
NET_SPACING_TYPE=GND
MAKE_BASE=TRUE
MAX_NECK_LENGTH=4.1 MM

46 GND_CHASSIS_USB

43 GND_CHASSIS_FIREWIRE
39 GND_CHASSIS_ENET
94 =GND_CHASSIS_DVI

NOTE:
PER EMC REQUIREMENTS, ALL CHASSIS GROUNDS ARE TIED DIRECTLY TO GND

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GROUNDING ALIASES

SYNC_DATE=01/08/2008

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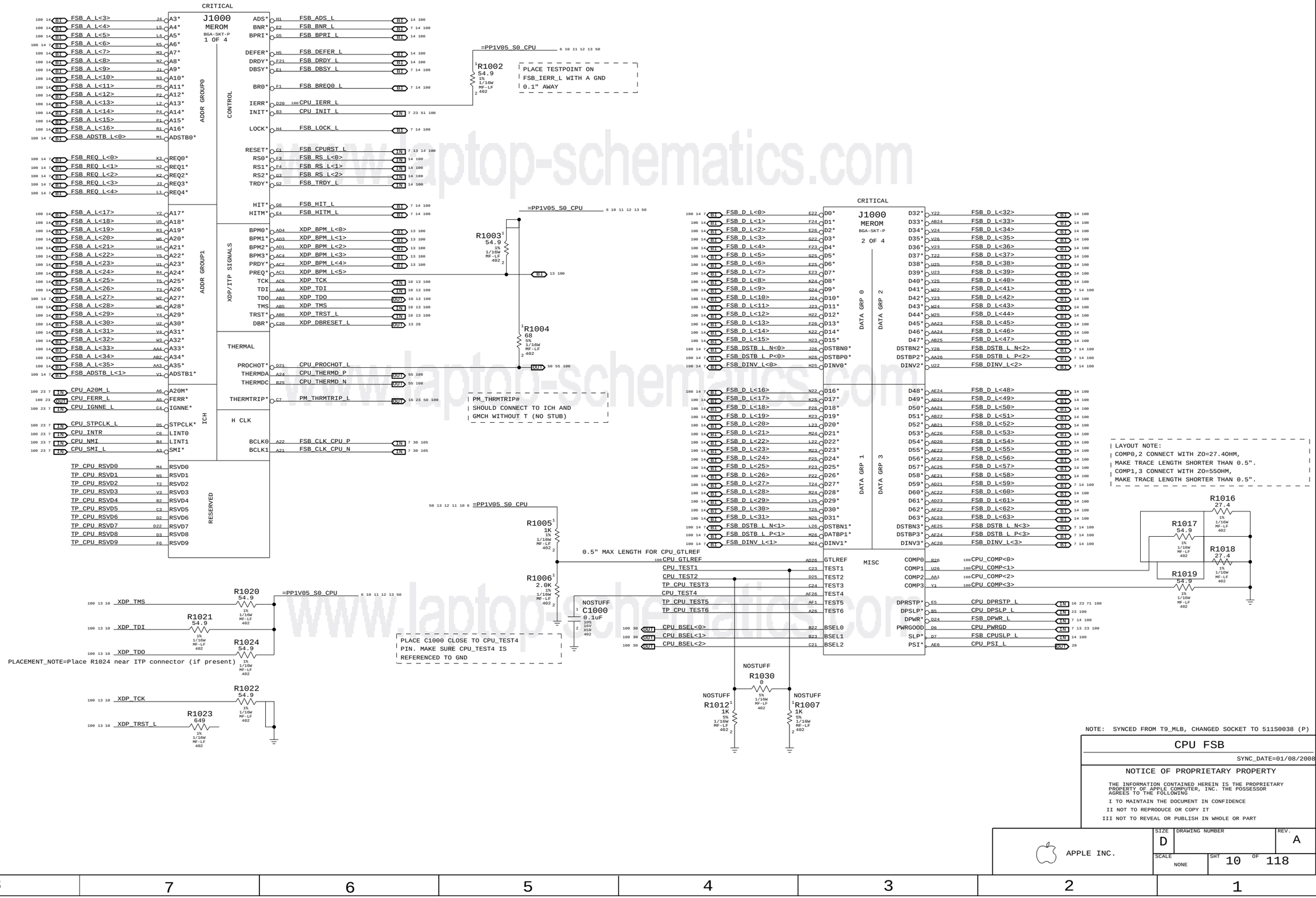
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D		A

SCALE NONE

SHT 9 OF 118


CRITICAL
J1000
MEROM
BGA-SKT-P
1 OF 4
ADDR GROUP0
ADDR GROUP1
CONTROL
XDP/ITP SIGNALS
THERMAL
H CLK
ICH
RESERVED
FSB_A_L<3>
FSB_A_L<4>
FSB_A_L<5>
FSB_A_L<6>
FSB_A_L<7>
FSB_A_L<8>
FSB_A_L<9>
FSB_A_L<10>
FSB_A_L<11>
FSB_A_L<12>
FSB_A_L<13>
FSB_A_L<14>
FSB_A_L<15>
FSB_A_L<16>
FSB_ADSTB_L<0>
FSB_REQ_L<0>
FSB_REQ_L<1>
FSB_REQ_L<2>
FSB_REQ_L<3>
FSB_REQ_L<4>
FSB_A_L<17>
FSB_A_L<18>
FSB_A_L<19>
FSB_A_L<20>
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FSB_A_L<23>
FSB_A_L<24>
FSB_A_L<25>
FSB_A_L<26>
FSB_A_L<27>
FSB_A_L<28>
FSB_A_L<29>
FSB_A_L<30>
FSB_A_L<31>
FSB_A_L<32>
FSB_A_L<33>
FSB_A_L<34>
FSB_A_L<35>
FSB_ADSTB_L<1>
CPU_A20M_L
CPU_FERR_L
CPU_IGNNE_L
CPU_STPCLK_L
CPU_INTR
CPU_NMI
CPU_SMI_L
TP_CPU_RSVD0
TP_CPU_RSVD1
TP_CPU_RSVD2
TP_CPU_RSVD3
TP_CPU_RSVD4
TP_CPU_RSVD5
TP_CPU_RSVD6
TP_CPU_RSVD7
TP_CPU_RSVD8
TP_CPU_RSVD9
ADS*
BNR*
BPRI*
DEFER*
DRDY*
DBSY*
BR0*
IERR*
INIT*
LOCK*
RESET*
RS0*
RS1*
RS2*
TRDY*
HIT*
HITM*
BPM0*
BPM1*
BPM2*
BPM3*
PRDY*
PREQ*
TCK
TDI
TDO
TMS
TRST*
DBR*
PROCHOT*
THERMDA
THERMDC
THERMTRIP*
BCLK0
BCLK1
FSB_ADS_L
FSB_BNR_L
FSB_BPRI_L
FSB_DEFER_L
FSB_DRDY_L
FSB_DBSY_L
FSB_BREQ0_L
CPU_IERR_L
CPU_INIT_L
FSB_LOCK_L
FSB_CPURST_L
FSB_RS_L<0>
FSB_RS_L<1>
FSB_RS_L<2>
FSB_TRDY_L
FSB_HIT_L
FSB_HITM_L
XDP_BPM_L<0>
XDP_BPM_L<1>
XDP_BPM_L<2>
XDP_BPM_L<3>
XDP_BPM_L<4>
XDP_BPM_L<5>
XDP_TCK
XDP_TDI
XDP_TDO
XDP_TMS
XDP_TRST_L
XDP_DBRESET_L
CPU_PROCHOT_L
CPU_THERMD_P
CPU_THERMD_N
PM_THRMTRIP_L
FSB_CLK_CPU_P
FSB_CLK_CPU_N
=PP1V05_S0_CPU
R1002 54.9 1% 1/16W MF-LF 402
PLACE TESTPOINT ON FSB_IERR_L WITH A GND 0.1" AWAY
R1003 54.9 1% 1/16W MF-LF 402
R1004 68 5% 1/16W MF-LF 402
PM_THRMTRIP# SHOULD CONNECT TO ICH AND GMCH WITHOUT T (NO STUB)
R1005 1K 1% 1/16W MF-LF 402
R1006 2.0K 1% 1/16W MF-LF 402
0.5" MAX LENGTH FOR CPU_GTLREF
NOSTUFF C1000 0.1uF 10% 16V X5R 402
PLACE C1000 CLOSE TO CPU_TEST4 PIN. MAKE SURE CPU_TEST4 IS REFERENCED TO GND
R1020 54.9 1% 1/16W MF-LF 402
R1021 54.9 1% 1/16W MF-LF 402
R1024 54.9 1% 1/16W MF-LF 402
PLACEMENT_NOTE=Place R1024 near ITP connector (if present)
R1022 54.9 1% 1/16W MF-LF 402
R1023 649 1% 1/16W MF-LF 402
CRITICAL
J1000
MEROM
BGA-SKT-P
2 OF 4
DATA GRP 0
DATA GRP 2
DATA GRP 1
DATA GRP 3
MISC
D0* D1* D2* D3* D4* D5* D6* D7* D8* D9* D10* D11* D12* D13* D14* D15*
DSTBN0* DSTBP0* DINV0*
D16* D17* D18* D19* D20* D21* D22* D23* D24* D25* D26* D27* D28* D29* D30* D31*
DSTBN1* DATBP1* DINV1*
D32* D33* D34* D35* D36* D37* D38* D39* D40* D41* D42* D43* D44* D45* D46* D47*
DSTBN2* DSTBP2* DINV2*
D48* D49* D50* D51* D52* D53* D54* D55* D56* D57* D58* D59* D60* D61* D62* D63*
DSTBN3* DSTBP3* DINV3*
FSB_D_L<0> FSB_D_L<1> FSB_D_L<2> FSB_D_L<3> FSB_D_L<4> FSB_D_L<5> FSB_D_L<6> FSB_D_L<7> FSB_D_L<8> FSB_D_L<9> FSB_D_L<10> FSB_D_L<11> FSB_D_L<12> FSB_D_L<13> FSB_D_L<14> FSB_D_L<15> FSB_DSTB_L_N<0> FSB_DSTB_L_P<0> FSB_DINV_L<0>
FSB_D_L<16> FSB_D_L<17> FSB_D_L<18> FSB_D_L<19> FSB_D_L<20> FSB_D_L<21> FSB_D_L<22> FSB_D_L<23> FSB_D_L<24> FSB_D_L<25> FSB_D_L<26> FSB_D_L<27> FSB_D_L<28> FSB_D_L<29> FSB_D_L<30> FSB_D_L<31> FSB_DSTB_L_N<1> FSB_DSTB_L_P<1> FSB_DINV_L<1>
FSB_D_L<32> FSB_D_L<33> FSB_D_L<34> FSB_D_L<35> FSB_D_L<36> FSB_D_L<37> FSB_D_L<38> FSB_D_L<39> FSB_D_L<40> FSB_D_L<41> FSB_D_L<42> FSB_D_L<43> FSB_D_L<44> FSB_D_L<45> FSB_D_L<46> FSB_D_L<47> FSB_DSTB_L_N<2> FSB_DSTB_L_P<2> FSB_DINV_L<2>
FSB_D_L<48> FSB_D_L<49> FSB_D_L<50> FSB_D_L<51> FSB_D_L<52> FSB_D_L<53> FSB_D_L<54> FSB_D_L<55> FSB_D_L<56> FSB_D_L<57> FSB_D_L<58> FSB_D_L<59> FSB_D_L<60> FSB_D_L<61> FSB_D_L<62> FSB_D_L<63> FSB_DSTB_L_N<3> FSB_DSTB_L_P<3> FSB_DINV_L<3>
GTLREF TEST1 TEST2 TEST3 TEST4 TEST5 TEST6 BSEL0 BSEL1 BSEL2
COMP0 COMP1 COMP2 COMP3
DPRSTP* DPSLP* DPWR* PWRGOOD SLP* PSI*
CPU_GTLREF CPU_TEST1 CPU_TEST2 TP_CPU_TEST3 CPU_TEST4 TP_CPU_TEST5 TP_CPU_TEST6 CPU_BSEL<0> CPU_BSEL<1> CPU_BSEL<2>
CPU_COMP<0> CPU_COMP<1> CPU_COMP<2> CPU_COMP<3>
CPU_DPRSTP_L CPU_DPSLP_L FSB_DPWR_L CPU_PWRGD FSB_CPUSLP_L CPU_PSI_L
R1016 27.4 1% 1/16W MF-LF 402
R1017 54.9 1% 1/16W MF-LF 402
R1018 27.4 1% 1/16W MF-LF 402
R1019 54.9 1% 1/16W MF-LF 402
NOSTUFF R1030 0 5% 1/16W MF-LF 402
NOSTUFF R1012 1K 5% 1/16W MF-LF 402
NOSTUFF R1007 1K 5% 1/16W MF-LF 402
LAYOUT NOTE:
COMP0,2 CONNECT WITH ZO=27.4OHM, MAKE TRACE LENGTH SHORTER THAN 0.5".
COMP1,3 CONNECT WITH ZO=55OHM, MAKE TRACE LENGTH SHORTER THAN 0.5".
NOTE: SYNCED FROM T9_MLB, CHANGED SOCKET TO 511S0038 (P)
CPU FSB
SYNC_DATE=01/08/2008
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(CPU CORE POWER)

=PPVCORE_S0_CPU 6 11 12 53

44 A (SV Design Target)
41 A (SV HFM)
30.4 A (SV LFM)
23 A (LV Design Target)

CRITICAL

J1000
MEROM
BGA-SKT-P
3 OF 4

VCC

VCCP

(CPU IO POWER 1.05V)

=PP1V05_S0_CPU 6 10 12 13 50

4500 mA (before VCC stable)
2500 mA (after VCC stable)

(CPU INTERNAL PLL POWER 1.5V)

=PP1V5_S0_CPU 6 12

130 mA

VCCA

VID0	AD6	CPU_VID<0>	OUT 12 100
VID1	AF5	CPU_VID<1>	OUT 12 100
VID2	AE5	CPU_VID<2>	OUT 12 100
VID3	AF4	CPU_VID<3>	OUT 12 100
VID4	AE3	CPU_VID<4>	OUT 12 100
VID5	AF3	CPU_VID<5>	OUT 12 100
VID6	AE2	CPU_VID<6>	OUT 12 100

=PPVCORE_S0_CPU 6 11 12 53

R1100
100
1%
1/16W
MF-LF
402

LAYOUT NOTE:
PLACE R1100 AND R1101 WITHIN
1 INCH OF CPU, NO STUBS

VCCSENSE AF7 CPU_VCCSENSE_P OUT 71 100

VSSSENSE AE7 CPU_VCCSENSE_N OUT 71 100

R1101
100
1%
1/16W
MF-LF
402

LAYOUT NOTE:
CPU_VCCSENSE_P/CPU_VCCSENSE_N USE
ZO=27.4 OHM DIFFERENTIAL TRACE ROUTING.

LAYOUT NOTE:
PROVIDE A TEST POINT (WITH NO STUB)
TO CONNECT A DIFFERENTIAL PROBE
BETWEEN VCCSENSE AND VSSSENSE

CRITICAL

J1000
MEROM
BGA-SKT-P
4 OF 4

VSS

VSS

Current numbers from Merom for Santa Rosa EMTS, doc #20905.

NOTE: SYNCED FROM T9_MLB, CHANGED SOCKET TO 511S0038 (P)

CPU Power & Ground

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CPU VCORE HF AND BULK DECOUPLING

6X 220UF. 32X 22UF 0805

53 11 6 =PPVCORE_S0_CPU

NOTE: CHANGED TO X5R CAPS TO MATCH PREVIOUS IMACS AND FOR C4

LAYOUT NOTE:
PLACE INSIDE SOCKET CAVITY (ON BOTTOMSIDE)

NOSTUFF C1200 22UF 20% 6.3V CERM-X5R 805
C1201 C1202 C1203 C1204 C1205 C1206 C1207 C1208 C1209 — 22UF 20% 6.3V CERM-X5R 805

LAYOUT NOTE:
PLACE INSIDE SOCKET CAVITY (ON BOTTOMSIDE)

C1210 C1211 C1212 C1213 C1214 C1215 C1216 C1217 C1218 C1219 — 22UF 20% 6.3V CERM-X5R 805

LAYOUT NOTE:
PLACE NEAR SOCKET NORTH SIDE (ON TOPSIDE)

C1220 C1221 NOSTUFF C1222 NOSTUFF C1223 NOSTUFF C1224 NOSTUFF C1225 — 22UF 20% 6.3V CERM-X5R 805

LAYOUT NOTE:
PLACE NEAR SOCKET SOUTH SIDE (ON TOPSIDE)

C1226 C1227 NOSTUFF C1228 NOSTUFF C1229 C1230 NOSTUFF C1231 — 22UF 20% 6.3V CERM-X5R 805

LAYOUT NOTE:
PLACE ON BOTTOMSIDE

CRITICAL NOSTUFF C1250 220UF 20% 2V POLY CASE-D2-SM1
CRITICAL C1251 220UF 20% 2V POLY CASE-D2-SM1
CRITICAL C1254 220UF 20% 2V POLY CASE-D2-SM1
CRITICAL C1255 220UF 20% 2V POLY CASE-D2-SM1
CRITICAL C1252 220UF 20% 2V POLY CASE-D2-SM1
CRITICAL C1253 220UF 20% 2V POLY CASE-D2-SM1

LAYOUT NOTE:
PLACE ON BOTTOMSIDE

CPU VCORE VID CONNECTIONS

Resistors to allow for override of CPU VID
Will probably be removed before production

R1290 0 5% 1/16W MF-LF 402	CPU_VID<0>	IMVP6_VID<0>	100 11 / 71 100
R1291 0 5% 1/16W MF-LF 402	CPU_VID<1>	IMVP6_VID<1>	100 11 / 71 100
R1292 0 5% 1/16W MF-LF 402	CPU_VID<2>	IMVP6_VID<2>	100 11 / 71 100
R1293 0 5% 1/16W MF-LF 402	CPU_VID<3>	IMVP6_VID<3>	100 11 / 71 100
R1294 0 5% 1/16W MF-LF 402	CPU_VID<4>	IMVP6_VID<4>	100 11 / 71 100
R1295 0 5% 1/16W MF-LF 402	CPU_VID<5>	IMVP6_VID<5>	100 11 / 71 100
R1296 0 5% 1/16W MF-LF 402	CPU_VID<6>	IMVP6_VID<6>	100 11 / 71 100

VCCA (CPU AVdd) DECOUPLING

11 6 =PP1V5_S0_CPU — 1x 10uF, 1x 0.01uF

C1280 10uF 20% 6.3V X5R 603
C1281 0.01UF 10% 16V CERM 402

LAYOUT NOTE:
PLACE C1281 NEAR PIN B26 OF U1000

VCCP (CPU I/O) DECOUPLING

50 13 11 10 6 =PP1V05_S0_CPU — 1X 330UF, 6X 0.1UF 0402

CRITICAL C1235 330UF 20% 6.3V ELEC 6.3X8-SM
C1236 C1237 C1238 C1239 C1240 C1241 — 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C1235 CLOSE TO CPU

CPU Decoupling & VID

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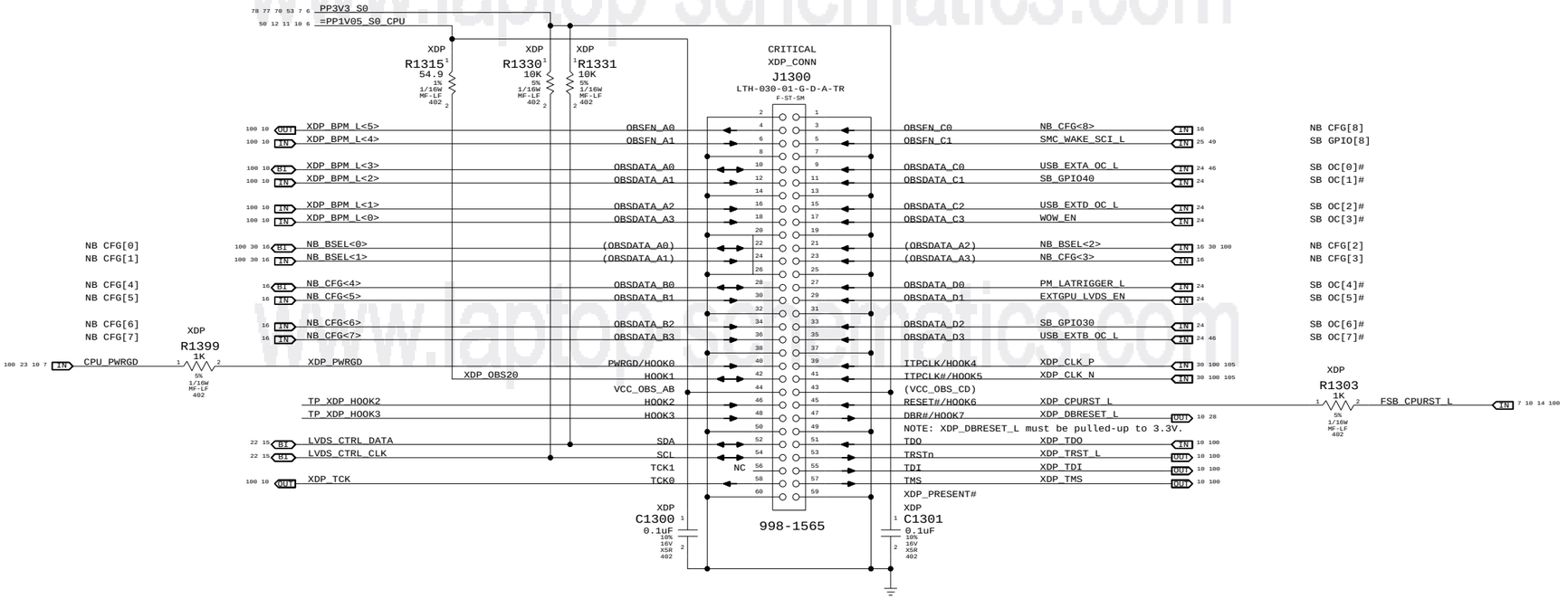
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0451 adapter board to support CPU, NB & SB debugging.



Direction of XDP module

Please avoid any obstructions
on even-numbered side of J1300

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eXtended Debug Port (XDP)

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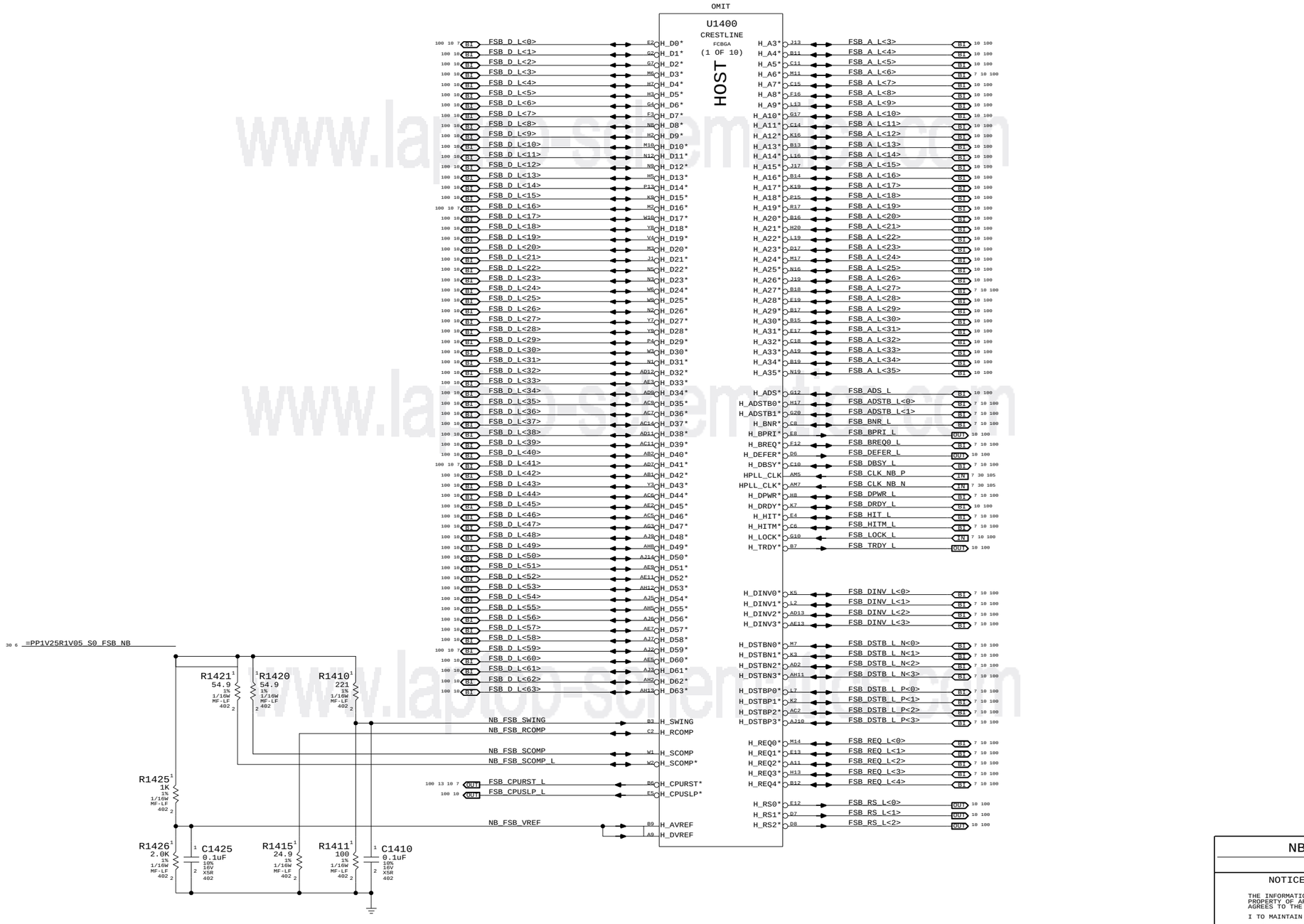

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NB CPU Interface

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LVDS Disable

Can leave all signals NC if LVDS is not implemented.
Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND.
All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

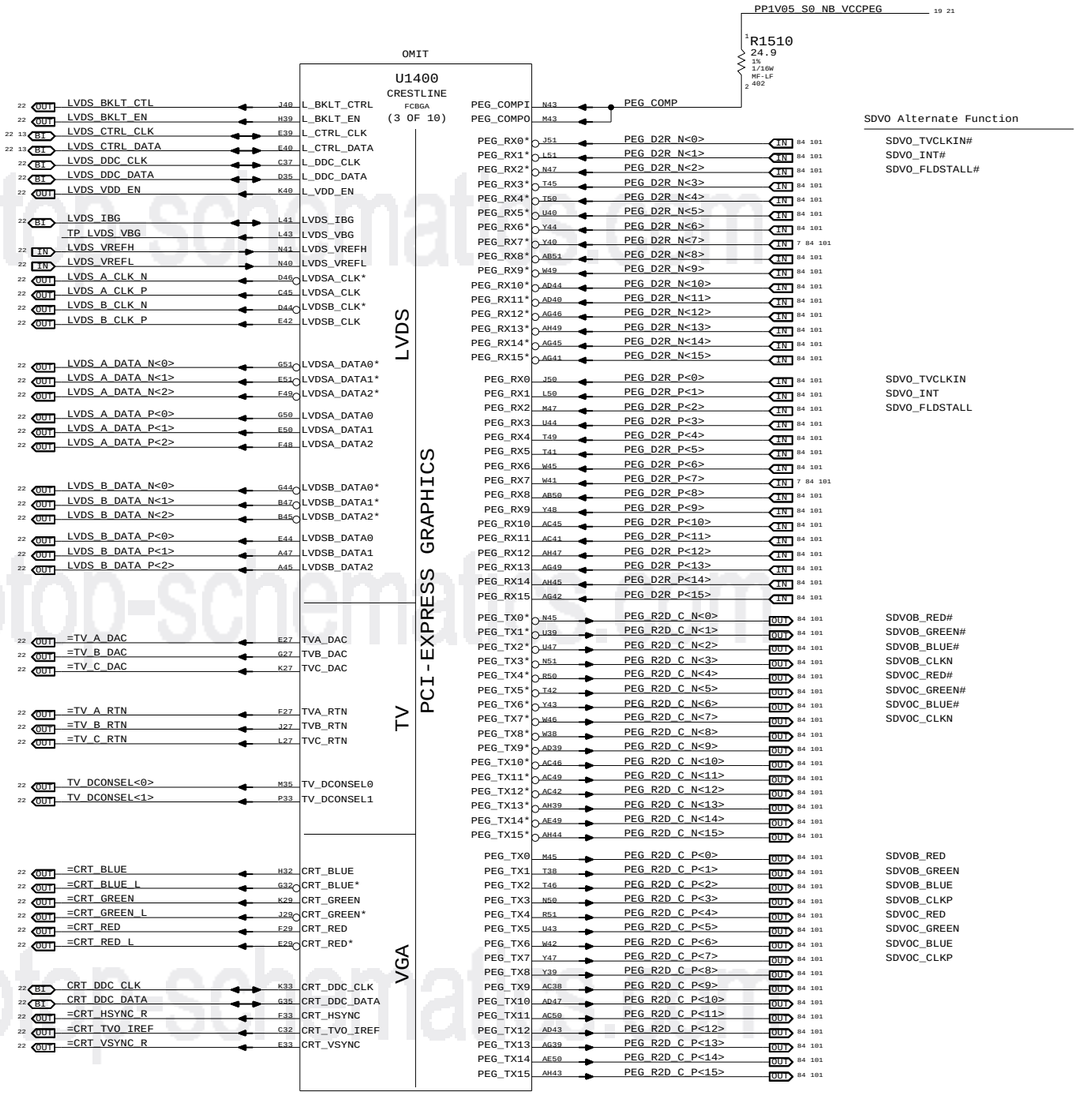
CRT & TV-Out Disable

Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TVO_IREF to GND.
Can tie the following rails to GND:
VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above.
Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and TV_DCONSELx to GND.
Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.



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NB PEG / Video Interfaces

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NB_CFG<3>	RESERVED
NB_CFG<4>	RESERVED
NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2
NB_CFG<6>	RESERVED
NB_CFG<7>	RESERVED
NB_CFG<8>	RESERVED
NB_CFG<9> PCIe Graphics Lane Reversal	High = Normal Low = Reversed
NB_CFG<10>	RESERVED
NB_CFG<11>	RESERVED
NB_CFG<12>	See Below
NB_CFG<13>	See Below
NB_CFG<14>	RESERVED
NB_CFG<15>	RESERVED
NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled
NB_CFG<17>	RESERVED
NB_CFG<18>	RESERVED
NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal
NB_CFG<20> Concurrent SDVO/PCIe x1	High = Both active Low = Only SDVO or PCIe x16

NB_CFG<13:12>

00 = RESERVED
01 = XOR Mode Enabled
10 = All-Z Mode Enabled
11 = Normal Operation

NB_CFG<5> — NBCFG_DMI_X2 — R1655 3.9K 5% 1/16W MF-LF 402

NB_CFG<9> — NBCFG_PEG_REVERSE — R1659 3.9K 5% 1/16W MF-LF 402

NB_CFG<16> — NBCFG_DYN_ODT_DISABLE — R1666 3.9K 5% 1/16W MF-LF 402

=PP3V3_S0_NB_VCCHV — NBCFG_DMI_REVERSE — R1669 3.9K 5% 1/16W MF-LF 402 — NB_CFG<19>

=PP3V3_S0_NB_VCCHV — NBCFG_SDVO_AND_PCIE — R1670 3.9K 5% 1/16W MF-LF 402 — NB_CFG<20>

NB CFG<8:0> used for debug access

NB CFG<13:12> require ICT access

=PP3V3_S0_NB_VCCHV — R1630 10K 5% 1/16W MF-LF 402 — R1631 10K 5% 1/16W MF-LF 402

PM_EXTTS_L<0>
PM_EXTTS_L<1>

OMIT

U1400
CRESTLINE
FCBGA
(2 OF 10)

TP_NB_RSVD<1>	P36	RSVD1	RSVD
TP_NB_RSVD<2>	P37	RSVD2	
TP_NB_RSVD<3>	R35	RSVD3	
TP_NB_RSVD<4>	N35	RSVD4	
TP_NB_RSVD<5>	AR12	RSVD5	
TP_NB_RSVD<6>	AR13	RSVD6	
TP_NB_RSVD<7>	AM12	RSVD7	
TP_NB_RSVD<8>	AN13	RSVD8	
TP_NB_RSVD<9>	J12	RSVD9	
TP_NB_RSVD<10>	AR37	RSVD10	
TP_NB_RSVD<11>	AM36	RSVD11	
TP_NB_RSVD<12>	AL36	RSVD12	
TP_NB_RSVD<13>	AM37	RSVD13	
TP_NB_RSVD<14>	D20	RSVD14	
TP_NB_RSVD<20>	H10	RSVD20	
TP_NB_RSVD<21>	B51	RSVD21	
TP_NB_RSVD<22>	BJ20	RSVD22	
TP_NB_RSVD<23>	BK22	RSVD23	
TP_NB_RSVD<24>	BF19	RSVD24	
TP_NB_RSVD<25>	BH20	RSVD25	
TP_NB_RSVD<26>	BK18	RSVD26	
TP_NB_RSVD<27>	BJ18	RSVD27	
TP_MEM_CLKP2	BF23	SM_CK2	DDR MUXING
TP_MEM_CLKN2	BG23	SM_CK2*	
TP_MEM_CLKP5	BC23	SM_CK5	
TP_MEM_CLKN5	BD24	SM_CK5*	
MEM_A_A<14>	BJ29	SA_MA14	
MEM_B_A<14>	BE24	SB_MA14	
TP_NB_RSVD<34>	BH39	RSVD34	
TP_NB_RSVD<35>	AW20	RSVD35	
TP_NB_RSVD<36>	BK20	RSVD36	
TP_LVDS_A_DATAN3	C48	RSVD37	
TP_LVDS_A_DATAP3	D47	RSVD38	
TP_LVDS_B_DATAN3	B44	RSVD39	
TP_LVDS_B_DATAP3	C44	RSVD40	
TP_NB_RSVD<41>	A35	RSVD41	
TP_NB_RSVD<42>	B37	RSVD42	
TP_NB_RSVD<43>	B36	RSVD43	
TP_NB_RSVD<44>	B34	RSVD44	
TP_NB_RSVD<45>	C34	RSVD45	
NB_BSEL<0>	P27	CFG0	CFG
NB_BSEL<1>	N27	CFG1	
NB_BSEL<2>	N24	CFG2	
NB_CFG<3>	C21	CFG3 IPU	
NB_CFG<4>	C23	CFG4 IPU	
NB_CFG<5>	F23	CFG5 IPU	
NB_CFG<6>	N23	CFG6 IPU	
NB_CFG<7>	G23	CFG7 IPU	
NB_CFG<8>	J20	CFG8 IPU	
NB_CFG<9>	C20	CFG9 IPU	
TP_NB_CFG<10>	R24	CFG10 IPU	
TP_NB_CFG<11>	L23	CFG11 IPU	
TP_NB_CFG<12>	J23	CFG12 IPU	
TP_NB_CFG<13>	E23	CFG13 IPU	
TP_NB_CFG<14>	E20	CFG14 IPU	
TP_NB_CFG<15>	K23	CFG15 IPU	
NB_CFG<16>	M20	CFG16 IPU	
TP_NB_CFG<17>	M24	CFG17 IPU	
TP_NB_CFG<18>	L32	CFG18 IPD	
NB_CFG<19>	N33	CFG19 IPD	
NB_CFG<20>	L35	CFG20 IPD	
PM_BMBUSY_L	G41	PM_BM_BUSY*	PM
CPU_DPRSTP_L	L39	PM_DPRSTP*	
	L36	PM_EXT_TS0*	
	J36	PM_EXT_TS1*	
VR_PWRGOOD_DELAY	AW49	PWROK	
NB_RESET_L	AV20	RSTIN*	
PM_THRMTRIP_L	N20	THERMTRIP*	
PM_DPRSLPVR	G36	DPRSLPVR	
TP_NB_NC<1>	BJ51	NC1	NC
TP_NB_NC<2>	BK51	NC2	
TP_NB_NC<3>	BK50	NC3	
TP_NB_NC<4>	BL50	NC4	
TP_NB_NC<5>	BL49	NC5	
TP_NB_NC<6>	BL3	NC6	
TP_NB_NC<7>	BL2	NC7	
TP_NB_NC<8>	BK1	NC8	
TP_NB_NC<9>	BJ1	NC9	
TP_NB_NC<10>	E1	NC10	
TP_NB_NC<11>	A5	NC11	
TP_NB_NC<12>	C51	NC12	
TP_NB_NC<13>	B50	NC13	
TP_NB_NC<14>	A50	NC14	
TP_NB_NC<15>	A49	NC15	
TP_NB_NC<16>	BK2	NC16	

SM_CK0	AV29	MEM_CLK_P<0>	DDR MUXING
SM_CK1	BB23	MEM_CLK_P<1>	
SM_CK3	BA25	MEM_CLK_P<3>	
SM_CK4	AV23	MEM_CLK_P<4>	
SM_CK0*	AW30	MEM_CLK_N<0>	
SM_CK1*	BA23	MEM_CLK_N<1>	
SM_CK3*	AW25	MEM_CLK_N<3>	
SM_CK4*	AW23	MEM_CLK_N<4>	
SM_CKE0	BE29	MEM_CKE<0>	
SM_CKE1	AY32	MEM_CKE<1>	
SM_CKE3	BD39	MEM_CKE<3>	
SM_CKE4	BG37	MEM_CKE<4>	
SM_CS0*	BG20	MEM_CS_L<0>	
SM_CS1*	BK16	MEM_CS_L<1>	
SM_CS2*	BG16	MEM_CS_L<2>	
SM_CS3*	BE13	MEM_CS_L<3>	
SM_ODT0	BH18	MEM_ODT<0>	
SM_ODT1	BJ15	MEM_ODT<1>	
SM_ODT2	BJ14	MEM_ODT<2>	
SM_ODT3	BE16	MEM_ODT<3>	
SM_RCOMP	BL15	MEM_RCOMP	
SM_RCOMP*	BK14	MEM_RCOMP_L	
SM_RCOMP_VOH	BK31	MEM_RCOMP_VOH	
SM_RCOMP_VOL	BL31	MEM_RCOMP_VOL	
SM_VREF0	AR49	=PP0V9_S3M_MEM_NBVREFA	
SM_VREF1	AW4	=PP0V9_S3M_MEM_NBVREFB	
DPLL_REF_CLK	B42	=NB_CLK96M_DOT_P	CLK
DPLL_REF_CLK*	C42	=NB_CLK96M_DOT_N	
DPLL_REF_SSCLK	H48	=NB_CLK100M_DPLLSS_P	
DPLL_REF_SSCLK*	H47	=NB_CLK100M_DPLLSS_N	
PEG_CLK	K44	NB_CLK100M_PCIE_P	
PEG_CLK*	K45	NB_CLK100M_PCIE_N	

Clk used for PEG and DMI

DMI_RXN0	AN47	DMI_S2N_N<0>	DMI
DMI_RXN1	AJ38	DMI_S2N_N<1>	
DMI_RXN2	AN42	DMI_S2N_N<2>	
DMI_RXN3	AN46	DMI_S2N_N<3>	
DMI_RXP0	AM47	DMI_S2N_P<0>	
DMI_RXP1	AJ39	DMI_S2N_P<1>	
DMI_RXP2	AN41	DMI_S2N_P<2>	
DMI_RXP3	AN45	DMI_S2N_P<3>	
DMI_TXN0	AJ46	DMI_N2S_N<0>	
DMI_TXN1	AJ41	DMI_N2S_N<1>	
DMI_TXN2	AM40	DMI_N2S_N<2>	
DMI_TXN3	AM44	DMI_N2S_N<3>	
DMI_TXP0	AJ47	DMI_N2S_P<0>	
DMI_TXP1	AJ42	DMI_N2S_P<1>	
DMI_TXP2	AM39	DMI_N2S_P<2>	
DMI_TXP3	AM43	DMI_N2S_P<3>	

		GFX_VID<0>	GRAPHICS VID
		GFX_VID<1>	
		GFX_VID<2>	
		GFX_VID<3>	
		GFX_VID<4>	
GFX_VID0	E35	=GFX_VR_EN	
GFX_VID1	A39		
GFX_VID2	C38		
GFX_VID3	B39		
GFX_VR_EN	E36		

CL_CLK	AM49	CLINK_NB_CLK	MISC
CL_DATA	AK50	CLINK_NB_DATA	
CL_PWROK	AT43	=NB_CLINK_MPWROK	
CL_RST*	AN49	CLINK_NB_RESET_L	
CL_VREF	AM50	NB_CLINK_VREF	
SDVO_CTRL_CLK	H35	SDVO_CTRLCLK	
SDVO_CTRL_DATA	K36	SDVO_CTRLDATA	
CLKREQ*	G39	NB_CLKREQ_L	
ICH_SYNC*	G40	NB_SB_SYNC_L	
TEST1	A37	NB_TEST1	
TEST2	R32	NB_TEST2	

=PP1V8_S3M_MEM_NB
R1610 20 1% 1/16W MF-LF 402
R1620 1K 1% 1/16W MF-LF 402
C1623 0.01UF 10% 16V CERM 402
C1622 2.2UF 20% 6.3V CERM1 603
R1622 3.01K 1% 1/16W MF-LF 402
R1611 20 1% 1/16W MF-LF 402
C1625 0.01UF 10% 16V CERM 402
C1624 2.2UF 20% 6.3V CERM1 603
R1624 1K 1% 1/16W MF-LF 402

C1615 0.1uF 20% 10V CERM 402
C1616 0.1uF 20% 10V CERM 402

PP1V25_S0M_NB_VCCAXD
R1640 1K 1% 1/16W MF-LF 402
C1640 0.1uF 20% 10V CERM 402
R1641 392 1% 1/16W MF-LF 402

R1691 20K 5% 1/16W MF-LF 402
R1690 0 5% 1/16W MF-LF 402

NOTE: GMCH CL_PWROK input must be PWRGD signal for PP3V3_S0M, PP3V3_S0MWOL, PP1V8_S3M, PP1V25_S0M, PP1V05_S0M, PP0V9_S3M and PP0V9_S0M.
If ME/AMT is used, short CL_PWROK to PWROK.

NB Misc Interfaces

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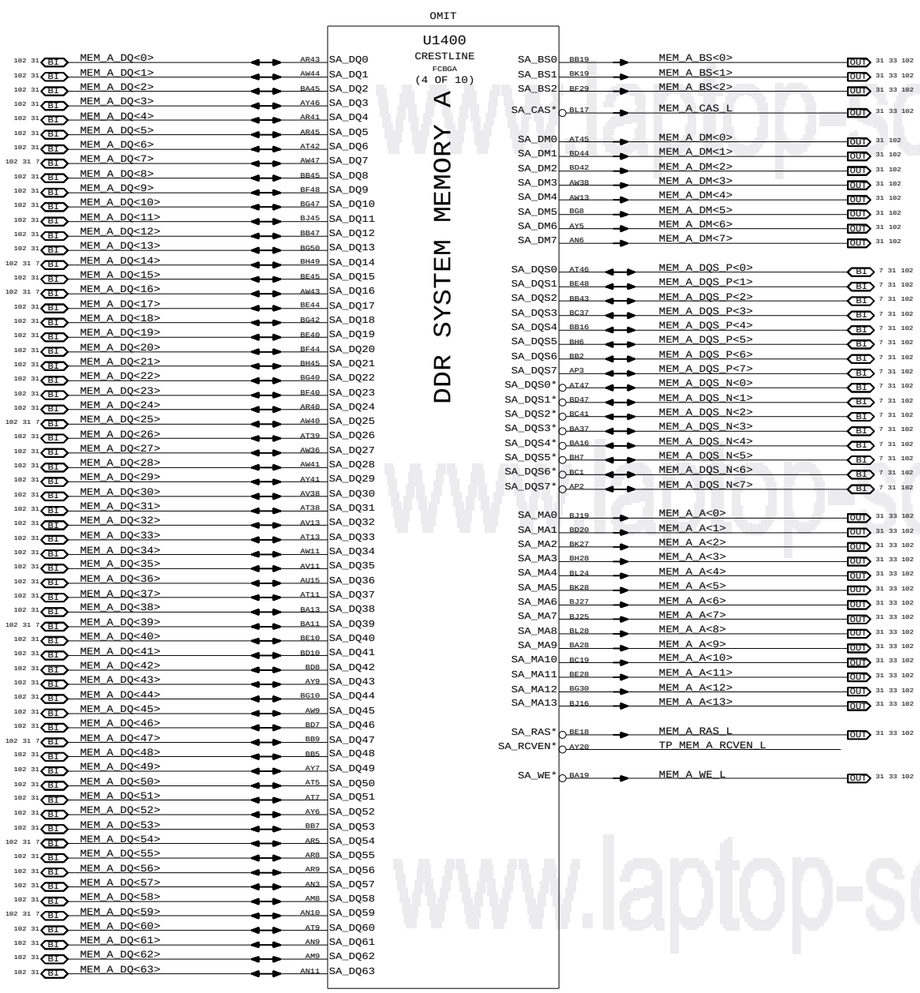

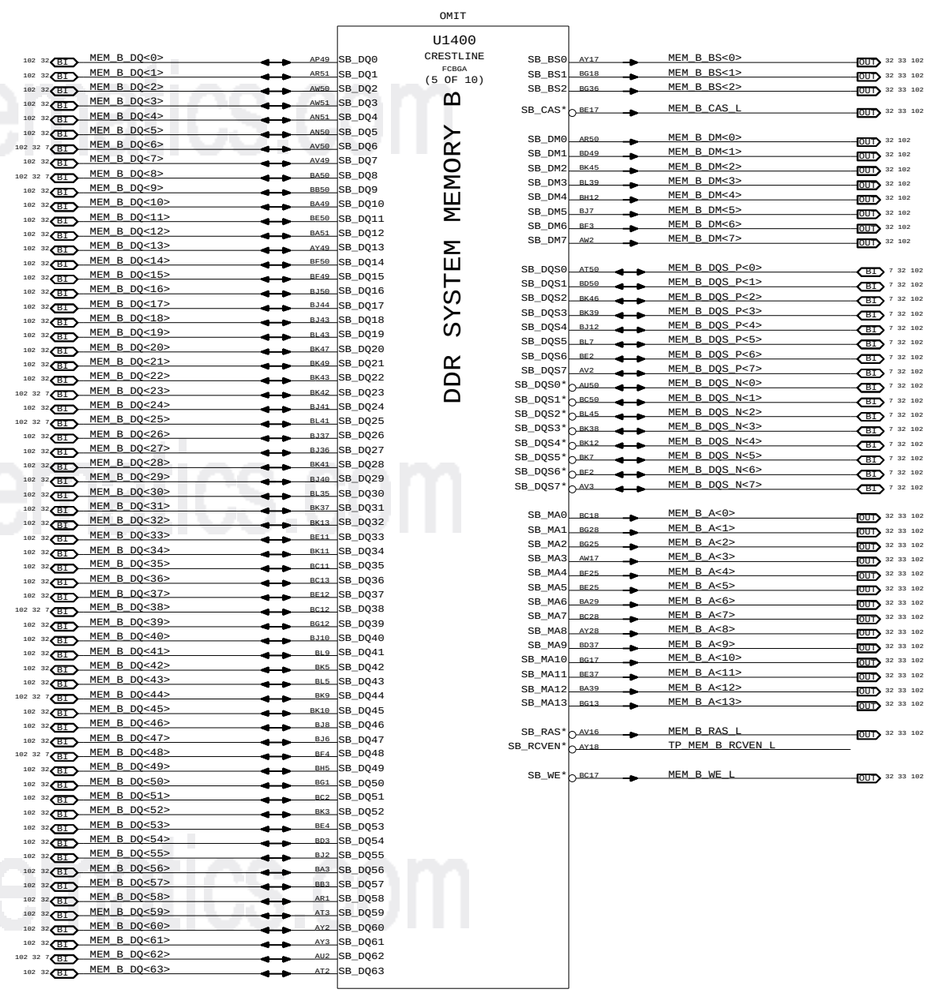

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NB DDR2 Interfaces

SYNC_DATE=01/08/2008

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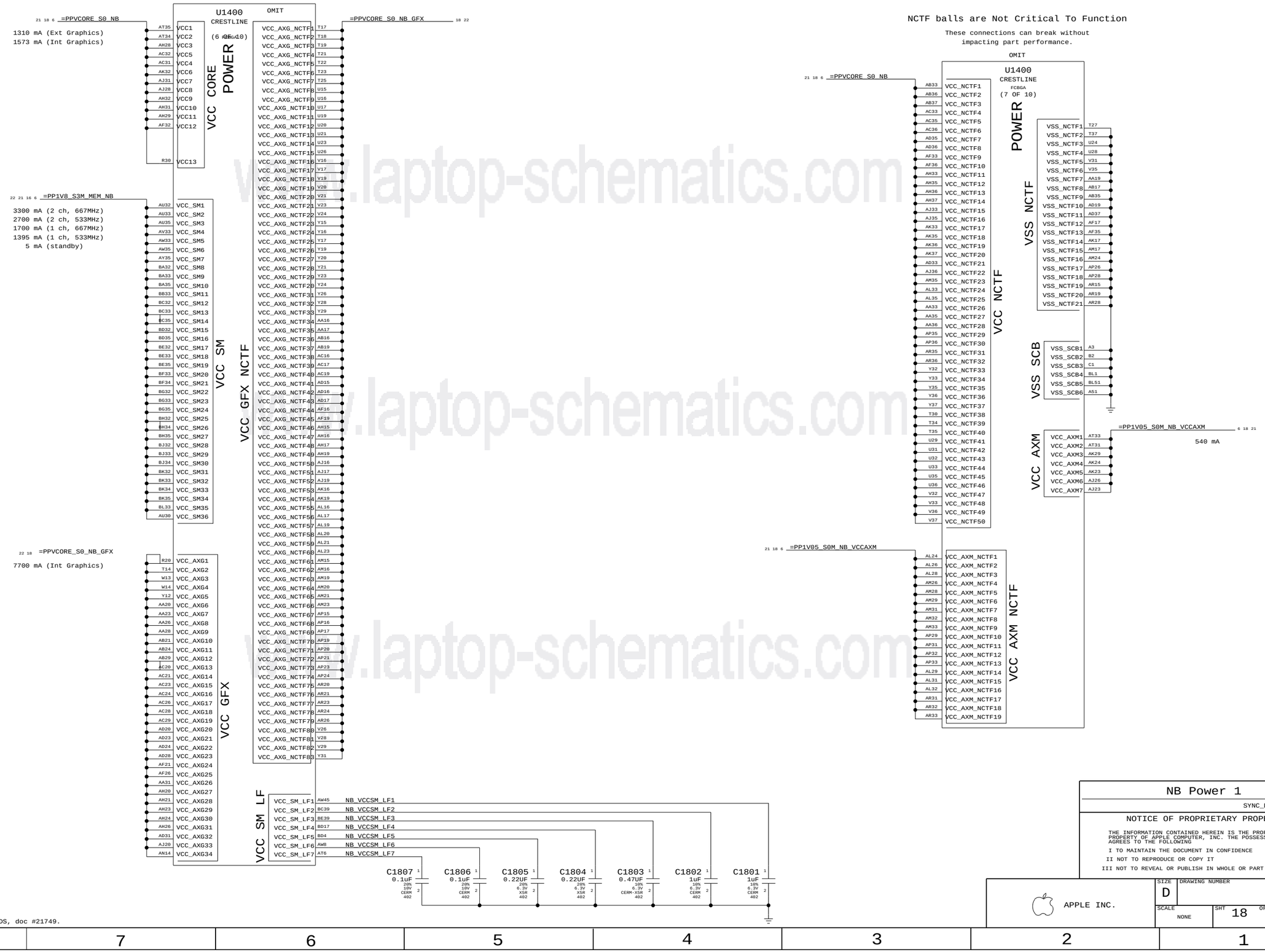
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D		A

SCALE: NONE

SHT 17 OF 118



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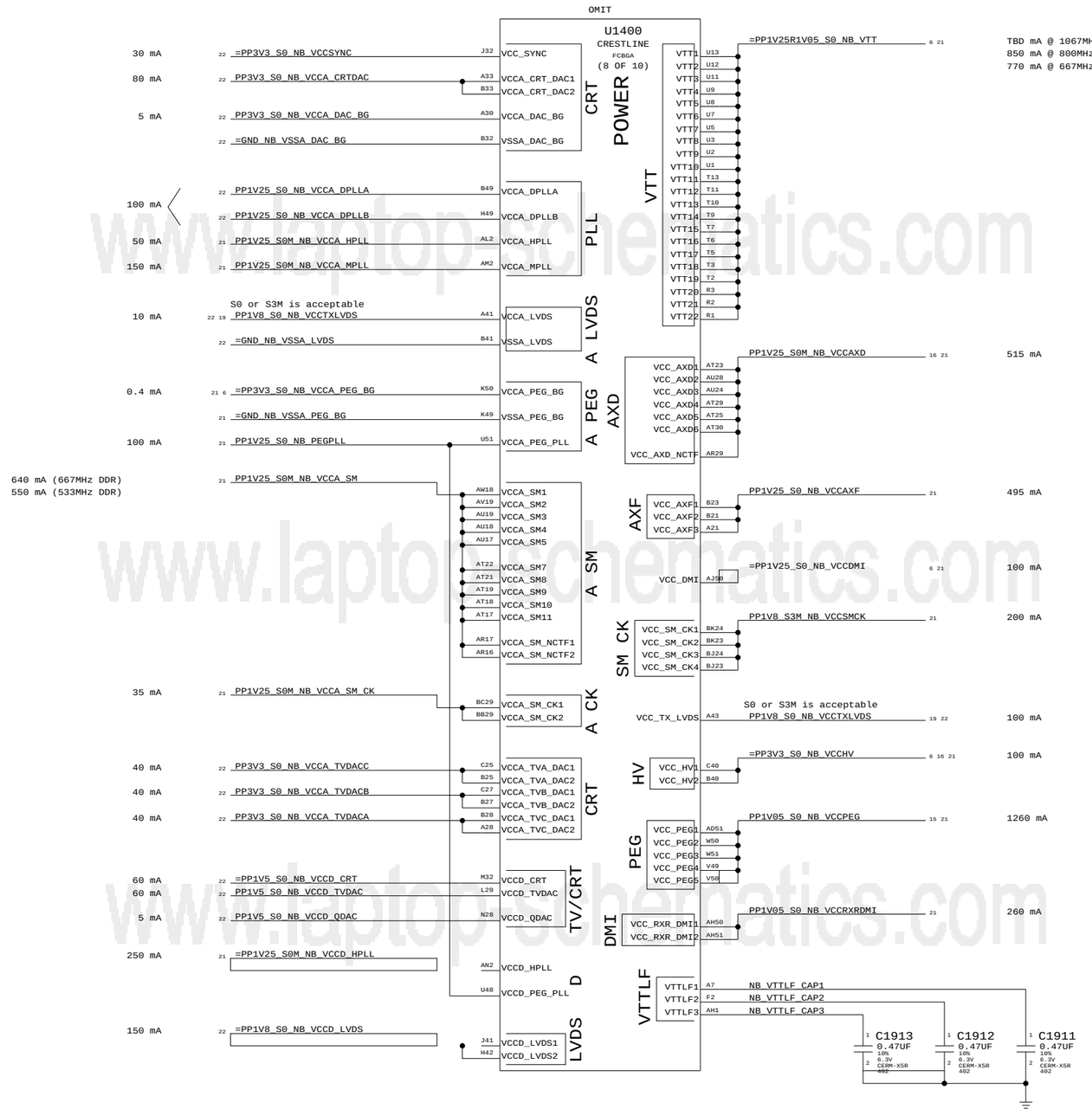

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Current numbers from Crestline EDS, doc #21749.

NB Power 2

SYNC_DATE=01/08/2008

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SIZE	DRAWING NUMBER	REV.
D		A
SCALE: NONE	SHT 19 OF 118	

OMIT

U1400
CRESTLINE
FCBGA
(9 OF 10)
VSS

A13	VSS1	VSS100	AW24
A15	VSS2	VSS101	AW29
A17	VSS3	VSS102	AW32
A24	VSS4	VSS103	AW5
AA21	VSS5	VSS104	AW7
AA24	VSS6	VSS105	AY10
AA29	VSS7	VSS106	AY24
AB20	VSS8	VSS107	AY37
AB23	VSS9	VSS108	AY42
AB26	VSS10	VSS109	AY43
AB28	VSS11	VSS110	AY45
AB31	VSS12	VSS111	AY47
AC10	VSS13	VSS112	AY50
AC13	VSS14	VSS113	B10
AC3	VSS15	VSS114	B20
AC39	VSS16	VSS115	B24
AC43	VSS17	VSS116	B29
AC47	VSS18	VSS117	B30
AD1	VSS19	VSS118	B35
AD21	VSS20	VSS119	B38
AD26	VSS21	VSS120	B43
AD29	VSS22	VSS121	B46
AD3	VSS23	VSS122	B5
AD41	VSS24	VSS123	B8
AD45	VSS25	VSS124	BA1
AD49	VSS26	VSS125	BA17
AD5	VSS27	VSS126	BA18
AD50	VSS28	VSS127	BA2
AD8	VSS29	VSS128	BA24
AE10	VSS30	VSS129	BB12
AE14	VSS31	VSS130	BB25
AE6	VSS32	VSS131	BB40
AF20	VSS33	VSS132	BB44
AF23	VSS34	VSS133	BB49
AF24	VSS35	VSS134	BB8
AF31	VSS36	VSS135	BC16
AG2	VSS37	VSS136	BC24
AG38	VSS38	VSS137	BC25
AG43	VSS39	VSS138	BC36
AG47	VSS40	VSS139	BC40
AG50	VSS41	VSS140	BC51
AH3	VSS42	VSS141	BD13
AH40	VSS43	VSS142	BD2
AH41	VSS44	VSS143	BD28
AH7	VSS45	VSS144	BD45
AH9	VSS46	VSS145	BD48
AJ11	VSS47	VSS146	BD5
AJ13	VSS48	VSS147	BE1
AJ21	VSS49	VSS148	BE19
AJ24	VSS50	VSS149	BE23
AJ29	VSS51	VSS150	BE30
AJ32	VSS52	VSS151	BE42
AJ43	VSS53	VSS152	BE51
AJ45	VSS54	VSS153	BE8
AJ49	VSS55	VSS154	BF12
AK20	VSS56	VSS155	BF16
AK21	VSS57	VSS156	BF36
AK26	VSS58	VSS157	BG19
AK28	VSS59	VSS158	BG2
AK31	VSS60	VSS159	BG24
AK51	VSS61	VSS160	BG29
AL1	VSS62	VSS161	BG39
AM11	VSS63	VSS162	BG48
AM13	VSS64	VSS163	BG5
AM3	VSS65	VSS164	BG51
AM4	VSS66	VSS165	BH17
AM41	VSS67	VSS166	BH30
AM45	VSS68	VSS167	BH44
AN1	VSS69	VSS168	BH46
AN38	VSS70	VSS169	BH8
AN39	VSS71	VSS170	BJ11
AN43	VSS72	VSS171	BJ13
AN5	VSS73	VSS172	BJ38
AN7	VSS74	VSS173	BJ4
AP4	VSS75	VSS174	BJ42
AP48	VSS76	VSS175	BJ46
AP50	VSS77	VSS176	BK15
AR11	VSS78	VSS177	BK17
AR2	VSS79	VSS178	BK25
AR39	VSS80	VSS179	BK29
AR44	VSS81	VSS180	BK36
AR47	VSS82	VSS181	BK40
AR7	VSS83	VSS182	BK44
AT10	VSS84	VSS183	BK6
AT14	VSS85	VSS184	BK8
AT41	VSS86	VSS185	BL11
AT49	VSS87	VSS186	BL13
AU1	VSS88	VSS187	BL19
AU23	VSS89	VSS188	BL22
AU29	VSS90	VSS189	BL37
AU3	VSS91	VSS190	BL47
AU36	VSS92	VSS191	C12
AU49	VSS93	VSS192	C16
AU51	VSS94	VSS193	C19
AV39	VSS95	VSS194	C28
AV48	VSS96	VSS195	C29
AW1	VSS97	VSS196	C33
AW12	VSS98	VSS197	C36
AW16	VSS99	VSS198	C41

OMIT

U1400
CRESTLINE
FCBGA
(10 OF 10)
VSS

C46	VSS199	VSS287	W11		
C50	VSS200	VSS288	W39		
C7	VSS201	VSS289	W43		
D13	VSS202	VSS290	W47		
D24	VSS203	VSS291	W5		
D3	VSS204	VSS292	W7		
D32	VSS205	VSS293	Y13		
D39	VSS206	VSS294	Y2		
D45	VSS207	VSS295	Y41		
D49	VSS208	VSS296	Y45		
E10	VSS209	VSS297	Y49		
E16	VSS210	VSS298	Y5		
E24	VSS211	VSS299	Y50		
E28	VSS212	VSS300	Y11		
E32	VSS213	VSS301	P29		
E47	VSS214				
F19	VSS215				
F36	VSS216	TDE_SENSE	VSS302	T29	=NB_TDE_SENSE 55
F4	VSS217				
F40	VSS218				
F50	VSS219	TDE_FORCE	VSS303	T31	=NB_TDE_FORCE 55
G1	VSS220				
G13	VSS221				
G16	VSS222	TDB_FORCE	VSS304	T33	=NB_TDB_FORCE 55
G19	VSS223				
G24	VSS224				
G28	VSS225	TDB_SENSE	VSS305	R28	=NB_TDB_SENSE 55
G29	VSS226				
G33	VSS227				
G42	VSS228				
G45	VSS229	VSS306	AA32		
G48	VSS230	VSS307	AB32		
G8	VSS231	VSS308	AD32		
H24	VSS232	VSS309	AF28		
H28	VSS233	VSS310	AF29		
H4	VSS234	VSS311	AT27		
H45	VSS235	VSS312	AV25		
J11	VSS236	VSS313	H50		
J16	VSS237				
J2	VSS238				
J24	VSS239				
J28	VSS240				
J33	VSS241				
J35	VSS242				
J39	VSS243				
K12	VSS245				
K47	VSS246				
K8	VSS247				
L1	VSS248				
L17	VSS249				
L20	VSS250				
L24	VSS251				
L28	VSS252				
L3	VSS253				
L33	VSS254				
L49	VSS255				
M28	VSS256				
M42	VSS257				
M46	VSS258				
M49	VSS259				
M5	VSS260				
M50	VSS261				
M9	VSS262				
N11	VSS263				
N14	VSS264				
N17	VSS265				
N29	VSS266				
N32	VSS267				
N36	VSS268				
N39	VSS269				
N44	VSS270				
N49	VSS271				
N7	VSS272				
P19	VSS273				
P2	VSS274				
P23	VSS275				
P3	VSS276				
P50	VSS277				
R49	VSS278				
T39	VSS279				
T43	VSS280				
T47	VSS281				
U41	VSS282				
U45	VSS283				
U50	VSS284				
V2	VSS285				
V3	VSS286				

Crestline Thermal Diode Pins

Mainly for investigation. If not used, alias these nets directly to GND.

NOTE: TDE = _P

NOTE: TDB = _N

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NB Grounds

SYNC_DATE=01/08/2008

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SIZE	DRAWING NUMBER	REV.
D		A

SCALE	SHT	OF
NONE	20	118

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GMCH Core Power

=PPVCORE_S0_NB

1573mA (Int Graphics)
1310mA (Ext Graphics)

C2100 330UF 20% 6.3V ELEC 6.3X8-SM
C2101 22uF 20% 6.3V CERM 805
C2102 0.22uF 20% 6.3V X5R 402
C2103 0.22uF 20% 6.3V X5R 402
C2104 0.1uF 20% 10V CERM 402

PLACEMENT_NOTE=Place in GMCH cavity

WF: Matanzas has 2-pin 270uF bulk cap

GMCH ME Core Power

=PP1V05_S0M_NB_VCCAXM

540 mA

C2110 22uF 20% 6.3V CERM 805
C2111 0.22uF 20% 6.3V X5R 402
C2112 0.22uF 20% 6.3V X5R 402
C2113 0.1uF 20% 10V CERM 402
C2114 0.1uF 20% 10V CERM 402
C2115 0.1uF 20% 10V CERM 402

PLACEMENT_NOTE=Place in GMCH cavity

GMCH FSB I/O Rail

=PP1V25R1V05_S0_NB_VTT

850 mA (800MHz FSB)
770 mA (667MHz FSB)

C2120 330UF 20% 6.3V ELEC 6.3X8-SM
C2121 4.7uF 20% 6.3V CERM 603
C2122 4.7uF 20% 6.3V CERM 603
C2123 2.2uF 20% 6.3V CERM1 603
C2124 0.47UF 10% 6.3V CERM-X5R 402

PLACEMENT_NOTE=Place close to U1400

WF: Matanzas has 270uF

GMCH Memory I/O Rail

=PP1V8_S3M_MEM_NB

3300 mA (2ch 667MHz)
2700 mA (2ch 533MHz)
1700 mA (1ch 667MHz)
1395 mA (1ch 533MHz)
5 mA (standby)

C2130 330UF 20% 6.3V ELEC 6.3X8-SM
C2135 0.1uF 20% 10V CERM 402
C2131 22uF 20% 6.3V CERM 805
C2132 22uF 20% 6.3V CERM 805

PLACEMENT_NOTE=Place close to U1400

WF: "Place where LVDS and DDR2 taps." (C2125)

Placeholder for 3.9nH, 1A, 32mOhm

=PP1V25_S0M_NB_VCCA

675 mA (667MHz DDR2)
585 mA (533MHz DDR2)

R2141 0 5% 1/10W MF-LF 603
NO STUFF C2141 22uF 20% 6.3V CERM 805
C2142 22uF 20% 6.3V CERM 805
C2143 4.7UF 20% 6.3V CERM 603
C2144 1UF 10% 10V X5R 402-1

PP1V25_S0M_NB_VCCA_SM
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

640 mA (667MHz DDR2)
550 mA (533MHz DDR2)

C2140 330UF 20% 6.3V ELEC 6.3X8-SM

Placeholder for 2.2nH, 1.4A, 17mOhm

R2145 0 5% 1/10W MF-LF 603
C2145 22uF 20% 6.3V CERM 805
NO STUFF C2146 2.2uF 20% 6.3V CERM1 603
C2148 0.1uF 20% 10V CERM 402

PP1V25_S0M_NB_VCCA_SM_CK
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

35 mA

Placeholder for 5.6nH, 0.9A, 45mOhm max

=PP1V25_S0M_NB_VCC

515 mA

NO STUFF L2150 FERR-120-OHM-0.2A 0603
R2150 0 5% 1/10W MF-LF 603

NO STUFF C2150 22uF 20% 6.3V CERM 805
C2151 1UF 10% 10V X5R 402-1

PP1V25_S0M_NB_VCCAXD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

515 mA

100 mA =PP3V3_S0_NB_VCCHV
100 mA =PP1V25_S0_NB_VCCDMI

C2160 0.1uF 20% 10V CERM 402
C2161 0.1uF 20% 10V CERM 402

=PP3V3_S0_NB_VCCA_PEG_BG

C2165 0.1uF 20% 10V CERM 402

0.4 mA

=GND_NB_VSSA_PEG_BG

Layout Note: Route to caps, then GND

=PP1V25_S0_NB_VCC

495 mA

R2170 0 5% 1/10W MF-LF 603

PP1V25_S0_NB_VCCAXF
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

495 mA

C2170 10uF 20% 6.3V X5R 603
C2171 1UF 10% 10V X5R 402-1

=PP1V25_S0_NB_PCIE

1520 mA

Layout Note: Place L and C close to MCH

L2173 91NH 1210 CRITICAL
C2173 220UF 20% 16V ELEC SM-CASE-C1

PP1V05_S0_NB_VCCPEG
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

1260 mA

C2174 10uF 20% 6.3V X5R 603

Layout Note: 10uF caps should be close to MCH on opposite side.

PP1V05_S0_NB_VCCRXRDMI
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

260 mA

C2177 10uF 20% 6.3V X5R 603

Layout Note: 10uF caps should be close to MCH on opposite side.

=PP1V05_S0_NB_FOLLOW

D2185 SOT23 BAT54E3

PP3V3_S0_NB1V05_FOLLOW_R
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

R2185 10 1% 1/16W MF-LF 402

=PP3V3_S0_NB_FOLLOW

BOMOPTION=CR_E

=PPVCORE_S0_NB_FOLLOW

D2186 SOT23 BAT54E3

PP3V3_S0_NBCORE_FOLLOW_R
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

R2186 10 1% 1/16W MF-LF 402

BOMOPTION=CR_E

NOTE: This follower is redundant if VCORE is always 1.05V.

=PP1V25_S0M_NB_PLL

450 mA

=PP1V25_S0M_NB_VCCD_HPLL

250 mA

C2180 0.1uF 20% 10V CERM 402

PLACEMENT_NOTE=Place C2180 by U1400.AN2

L2181 FERR-120-OHM-0.2A 0603

PP1V25_S0M_NB_VCCA_HPLL
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

50 mA

C2181 22UF 20% 6.3V CERM 805
C2182 0.1uF 20% 10V CERM 402

PLACEMENT_NOTE=Place C2182 by U1400.AL2

L2183 FERR-120-OHM-0.2A 0603

PP1V25_S0M_NB_VCCA_MPLL
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

150 mA

R2183 0.51 1% 1/10W MF-LF 402
C2184 0.1uF 20% 10V CERM 402

PLACEMENT_NOTE=Place C2184 by U1400.AM2

PP1V25_S0M_NB_MPLL_RC
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

C2183 22UF 20% 6.3V CERM 805

=PP1V25_S0_NB_PLL

100 mA

L2190 FERR-220-OHM 0805
R2190 1.1 1% 1/16W MF-LF 402
C2191 0.1uF 20% 10V CERM 402

PP1V25_S0_NB_PEGPLL
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

100 mA

C2192 0.1uF 20% 10V CERM 402

PP1V25_S0_NB_PEGPLL_RC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

C2190 10uF 20% 6.3V X5R 603

=PP1V8_S3M_NB_VCC

200 mA

L2195 1.0UH-220MA-0.12-OHM 0805
R2195 1.1 1% 1/16W MF-LF 402

PP1V8_S3M_NB_VCCSMCK
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V

200 mA

C2196 22uF 20% 6.3V CERM 805
C2197 0.1uF 20% 10V CERM 402

PP1V8_S3M_NB_VCCSMCK_RC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V

C2195 10UF 20% 6.3V X5R 603

NOTE:
SYNCED FROM T9_MLB_NOME ON 10/31/06
CHANGED C2100,20,30,40,73 TO ELEC

NB Standard Decoupling

SYNC_DATE=01/08/2008

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D		A
SCALE: NONE	SHT 21 OF 118	

Current numbers from Crestline EDS, doc #21749.

NOTE:
SANTA ROSA DESIGN GUIDE REV 1.5
P. 227-228 TABLE 95

15 LVDS_BKLT_CTL — TRUE — TP_LVDS_BKLT_CTL
15 LVDS_BKLT_EN — TRUE — TP_LVDS_BKLT_EN
15 13 LVDS_CTRL_CLK
15 13 LVDS_CTRL_DATA
15 LVDS_DDC_CLK
15 LVDS_DDC_DATA
15 LVDS_VDD_EN — TRUE — TP_LVDS_VDD_EN

15 LVDS_IBG — TRUE — TP_LVDS_IBG
15 LVDS_VREFH — TRUE — TP_LVDS_VREFH
15 LVDS_VREFL — TRUE — TP_LVDS_VREFL
15 LVDS_A_CLK_N — TRUE — TP_LVDS_A_CLK_N
15 LVDS_A_CLK_P — TRUE — TP_LVDS_A_CLK_P
15 LVDS_B_CLK_N — TRUE — TP_LVDS_B_CLK_N
15 LVDS_B_CLK_P — TRUE — TP_LVDS_B_CLK_P

15 LVDS_A_DATA_N<0> — TRUE — TP_LVDS_A_DATA_N<0>
15 LVDS_A_DATA_N<1> — TRUE — TP_LVDS_A_DATA_N<1>
15 LVDS_A_DATA_N<2> — TRUE — TP_LVDS_A_DATA_N<2>

15 LVDS_A_DATA_P<0> — TRUE — TP_LVDS_A_DATA_P<0>
15 LVDS_A_DATA_P<1> — TRUE — TP_LVDS_A_DATA_P<1>
15 LVDS_A_DATA_P<2> — TRUE — TP_LVDS_A_DATA_P<2>

15 LVDS_B_DATA_N<0> — TRUE — TP_LVDS_B_DATA_N<0>
15 LVDS_B_DATA_N<1> — TRUE — TP_LVDS_B_DATA_N<1>
15 LVDS_B_DATA_N<2> — TRUE — TP_LVDS_B_DATA_N<2>

15 LVDS_B_DATA_P<0> — TRUE — TP_LVDS_B_DATA_P<0>
15 LVDS_B_DATA_P<1> — TRUE — TP_LVDS_B_DATA_P<1>
15 LVDS_B_DATA_P<2> — TRUE — TP_LVDS_B_DATA_P<2>

15 =TV_A_DAC
15 =TV_B_DAC
15 =TV_C_DAC

15 =TV_A_RTN
15 =TV_B_RTN
15 =TV_C_RTN

15 TV_DCONSEL<0>
15 TV_DCONSEL<1>

15 =CRT_BLUE
15 =CRT_BLUE_L
15 =CRT_GREEN
15 =CRT_GREEN_L
15 =CRT_RED
15 =CRT_RED_L

15 CRT_DDC_CLK
15 CRT_DDC_DATA
15 =CRT_HSYNC_R
15 =CRT_TVO_IREF
15 =CRT_VSYNC_R

16 =NB_CLK96M_DOT_P
16 =NB_CLK96M_DOT_N

16 =NB_CLK100M_DPLLSS_P
16 =NB_CLK100M_DPLLSS_N

16 SDVO_CTRLCLK
16 SDVO_CTRLDATA

16 GFX_VID<1> — TRUE — TP_GFX_VID<1>
16 GFX_VID<2> — TRUE — TP_GFX_VID<2>
16 GFX_VID<3> — TRUE — TP_GFX_VID<3>
16 GFX_VID<4> — TRUE — TP_GFX_VID<4>
16 =GFX_VR_EN — TRUE — TP_GFX_VR_EN

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NOTE:
SANTA ROSA DESIGN GUIDE REV 1.5
P. 227-228 TABLE 95

19 PP1V25_S0_NB_VCCA_DPLLA
19 PP1V25_S0_NB_VCCA_DPLLB
19 =PP1V5_S0_NB_VCCD_CRT
19 PP1V5_S0_NB_VCCD_QDAC
18 =PPVCORE_S0_NB_GFX
19 PP3V3_S0_NB_VCCA_CRTDAC
19 PP3V3_S0_NB_VCCA_TVDACA
19 PP3V3_S0_NB_VCCA_TVDACB
19 PP3V3_S0_NB_VCCA_TVDACC
19 PP3V3_S0_NB_VCCA_DAC_BG
19 =GND_NB_VSSA_DAC_BG
19 PP1V8_S0_NB_VCCTXLVDS
19 =GND_NB_VSSA_LVDS
19 =PP1V8_S0_NB_VCCD_LVDS
19 =PP3V3_S0_NB_VCCSYNC

NOTE:
SANTA ROSA PLATFORM P180 FIG 119 - NC
ALSO CONFIRMED WITH INTEL

TP_NB_VSSA_LVDS — TRUE

16 =NB_CLINK_MPWROK — TRUE — VR_PWRGOOD_DELAY 7 16 70 71

VCCD_TVDAC ALSO POWERS INTERNAL THERMAL SENSORS.
CRITICAL
C2201
22000pF-1000mA
16V
NPM1B

6 =PP1V5_S0_NB_TVDAC
65 mA

PP1V5_S0_NB_VCCD_TVDAC 19
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
60 mA

C2213
10uF
20%
6.3V
X5R
603

C2200
0.1uF
20%
10V
CERM
402

Layout Note:
THESE CAPS SHOULD BE
within 6.35 mm of NB edge

21 18 16 6 =PP1V8_S3M_MEM_NB

R2200
1K
5%
1/16W
MF-LF
402

R2202
1K
5%
1/16W
MF-LF
402

PP0V9_S3M_MEM_NBVREFA — TRUE — =PP0V9_S3M_MEM_NBVREFA 7 16
VOLTAGE=0.9V
MIN_LINE_WIDTH=0.25MM
MIN_NECK_WIDTH=0.25MM

PP0V9_S3M_MEM_NBVREFB — TRUE — =PP0V9_S3M_MEM_NBVREFB 7 16
VOLTAGE=0.9V
MIN_LINE_WIDTH=0.25MM
MIN_NECK_WIDTH=0.25MM

R2201
1K
5%
1/16W
MF-LF
402

R2203
1K
5%
1/16W
MF-LF
402

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NB Graphics Decoupling

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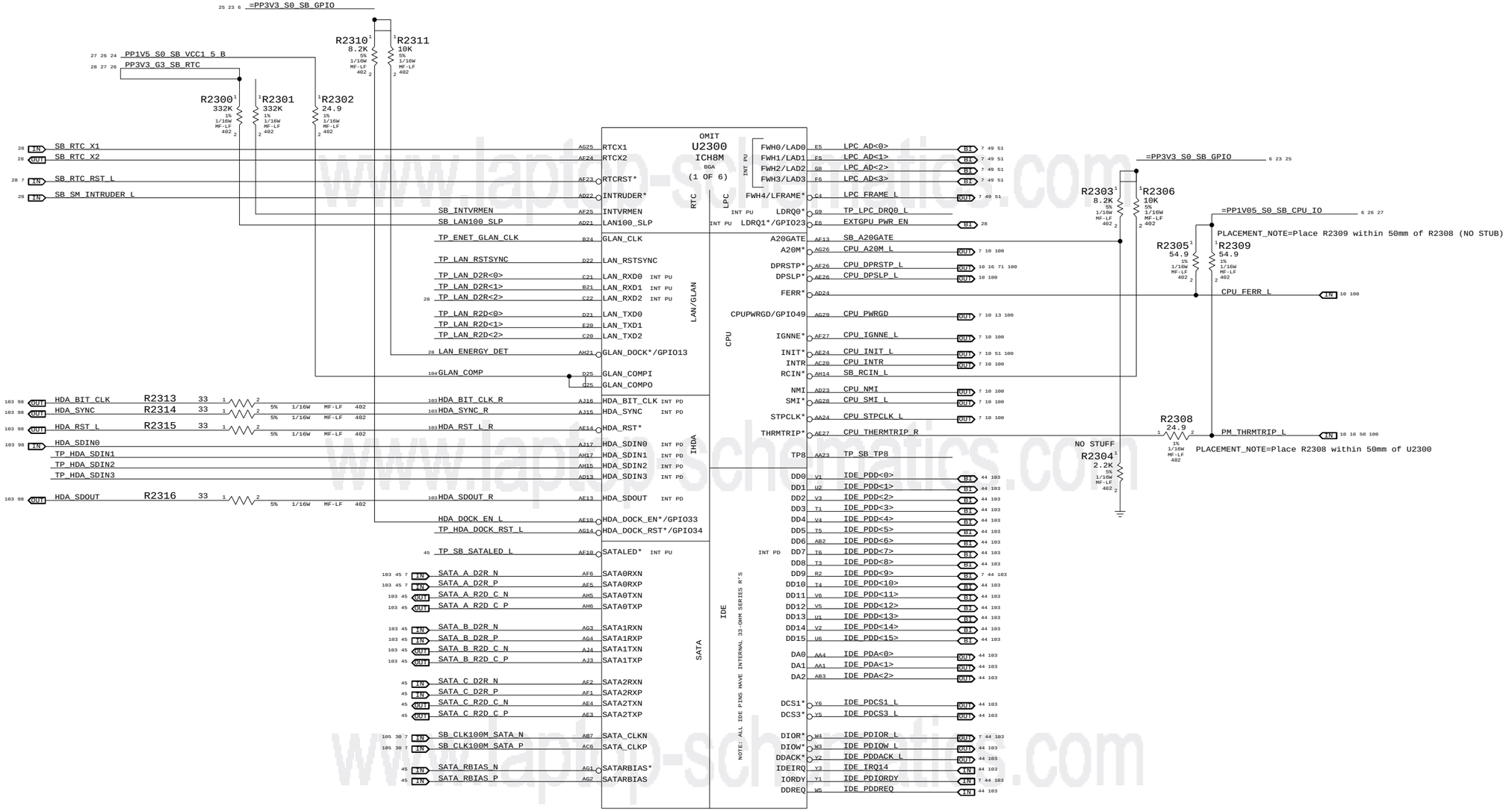

	HDA
HDA_BIT_CLK	24.000MHZ CLOCK W/INTERNAL WEAK PD
HDA_RST#	
HDA_SDIN[0-2]	INTEGRATED PDs
HDA_SDOUT	INTEGRATED PD
ACZ_SYNC	INTEGRATED PD

SB Enet, Disk, FSB, LPC

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PCI_EXPRESS

Spares
(x2-capable, pull HDA_SYNC high for x2)

TP_PCIE_A_D2R_N	P27	PERN1
TP_PCIE_A_D2R_P	P26	PERP1
TP_PCIE_A_R2D_C_N	N29	PETN1
TP_PCIE_A_R2D_C_P	N28	PETP1
TP_PCIE_B_D2R_N	M27	PERN2
TP_PCIE_B_D2R_P	M26	PERP2
TP_PCIE_B_R2D_C_N	L29	PETN2
TP_PCIE_B_R2D_C_P	L28	PETP2

ExpressCard

TP_PCIE_EXCARD_D2R_N	K27	PERN3
TP_PCIE_EXCARD_D2R_P	K26	PERP3
TP_PCIE_EXCARD_R2D_C_N	J29	PETN3
TP_PCIE_EXCARD_R2D_C_P	J28	PETP3

FireWire

42 TP_PCIE_FW_D2R_N	H27	PERN4
42 TP_PCIE_FW_D2R_P	H26	PERP4
42 TP_PCIE_FW_R2D_C_N	G29	PETN4
42 TP_PCIE_FW_R2D_C_P	G28	PETP4

PCIe Mini Card (AirPort)

104 34 7 IN PCIE_MINI_D2R_N	F27	PERN5
104 34 7 IN PCIE_MINI_D2R_P	F26	PERP5
104 34 OUT PCIE_MINI_R2D_C_N	E29	PETP5
104 34 OUT PCIE_MINI_R2D_C_P	E28	PETP5

Ethernet Yukon-PCIE Nineveh-GLCI

104 37 7 IN PCIE_ENET_D2R_N	D27	PERN6/GLAN_RXN
104 37 7 IN PCIE_ENET_D2R_P	D26	PERP6/GLAN_RXP
104 37 OUT PCIE_ENET_R2D_C_N	C29	PETN6/GLAN_TXN
104 37 OUT PCIE_ENET_R2D_C_P	C28	PETP6/GLAN_TXP

SPI

103 61 B1 SPI_SCLK_R	C23	SPI_CLK (INT PU)
103 61 B1 SPI_CE_R_L<0>	B23	SPI_CS0*
TP_SPI_CE_R_L<1>	E22	SPI_CS1* (INT PU)
103 61 B1 SPI_SI_R	D23	SPI_MOSI (INT PU)
103 61 7 B1 SPI_SO	F21	SPI_MISO (INT PU)

DIRECT MEDIA INTERFACE

DMI0RXN	V27	DMI_N2S_N<0> IN 7 16 101
DMI0RXP	V26	DMI_N2S_P<0> IN 7 16 101
DMI0TXN	U29	DMI_S2N_N<0> OUT 7 16 101
DMI0TXP	U28	DMI_S2N_P<0> OUT 7 16 101
DMI1RXN	Y27	DMI_N2S_N<1> IN 16 101
DMI1RXP	Y26	DMI_N2S_P<1> IN 16 101
DMI1TXN	W29	DMI_S2N_N<1> OUT 16 101
DMI1TXP	W28	DMI_S2N_P<1> OUT 16 101
DMI2RXN	AB26	DMI_N2S_N<2> IN 16 101
DMI2RXP	AB25	DMI_N2S_P<2> IN 16 101
DMI2TXN	AA29	DMI_S2N_N<2> OUT 16 101
DMI2TXP	AA28	DMI_S2N_P<2> OUT 16 101
DMI3RXN	AD27	DMI_N2S_N<3> IN 16 101
DMI3RXP	AD26	DMI_N2S_P<3> IN 16 101
DMI3TXN	AC29	DMI_S2N_N<3> OUT 16 101
DMI3TXP	AC28	DMI_S2N_P<3> OUT 16 101
DMI_CLKN	T26	SB_CLK100M_DMI_N IN 7 30 105
DMI_CLKP	T25	SB_CLK100M_DMI_P IN 7 30 105
DMI_ZCOMP	Y23	
DMI_IRCOMP	Y24	DMI_IRCOMP_R

R2413 24.9 1% 1/10W MF-LF 402
PP1V5_S0_SB_VCC1_5_B 23 26 27

USB

EHCI0

INT PD USBP0N	G3	USB_EXTA_N B1 46 103
INT PD USBP0P	G2	USB_EXTA_P B1 46 103
INT PD USBP1N	H5	USB_MINI_N B1 34 103
INT PD USBP1P	H4	USB_MINI_P B1 34 103
INT PD USBP2N	H2	USB_EXTD_N B1 46 103
INT PD USBP2P	H1	USB_EXTD_P B1 46 103
INT PD USBP3N	J3	USB_CAMERA_N B1 7 47 103
INT PD USBP3P	J2	USB_CAMERA_P B1 7 47 103
INT PD USBP4N	K5	USB_IR_N B1 7 47 103
INT PD USBP4P	K4	USB_IR_P B1 7 47 103
INT PD USBP5N	K2	USB_TPAD_N B1 47 103
INT PD USBP5P	K1	USB_TPAD_P B1 47 103

EHCI1

INT PD USBP6N	L3	USB_BT_N B1 7 47 103
INT PD USBP6P	L2	USB_BT_P B1 7 47 103
INT PD USBP7N	M5	USB_EXTB_N B1 46 103
INT PD USBP7P	M4	USB_EXTB_P B1 46 103
INT PD USBP8N	M2	USB_EXCARD_N B1 47 103
INT PD USBP8P	M1	USB_EXCARD_P B1 47 103
INT PD USBP9N	N3	USB_EXTC_N B1 46 103
INT PD USBP9P	N2	USB_EXTC_P B1 46 103

USBRBIAS*	F2	
USBRBIAS	F3	103 USB_RBIAS

R2414 22.6 1% 1/10W MF-LF 402

External A
AirPort (PCIe Mini-Card)
External D / WWAN
Camera
IR
Geyser Trackpad/Keyboard
Bluetooth
External B
ExpressCard
External C

NOTE: USBP[0-9]P/N have internal 15K pull-downs.

6 =PP3V3_S5_SB_USB

R2400 10K 5% 1/10W MF-LF 402
R2401 10K 5% 1/10W MF-LF 402
R2402 10K 5% 1/10W MF-LF 402
R2403 10K 5% 1/10W MF-LF 402
R2404 10K 5% 1/10W MF-LF 402
R2405 10K 5% 1/10W MF-LF 402
R2407 10K 5% 1/10W MF-LF 402
R2408 10K 5% 1/10W MF-LF 402
R2409 10K 5% 1/10W MF-LF 402

46 13 IN USB_EXTA_OC_L	AJ19	OC0*
13 OUT SB_GPIO40	AG16	OC1*/GPIO40
13 IN USB_EXTD_OC_L	AG15	OC2*/GPIO41
13 OUT WOW_EN	AE15	OC3*/GPIO42
13 OUT PM_LATRIGGER_L	AF15	OC4*/GPIO43
13 OUT EXTGPU_LVDS_EN	AG17	OC5*/GPIO29
13 OUT SB_GPIO30	AD12	OC6*/GPIO30
46 13 IN USB_EXTB_OC_L	AJ18	OC7*/GPIO31
IN EXCARD_OC_L	AD14	OC8*
46 IN USB_EXTC_OC_L	AH18	OC9*

R2406 10K 5% 1/10W MF-LF 402

NOTE: GNT[0-3]# have internal 20K pull-ups enabled only when PCIRST# = 0 and PWROK = 1

If used, ensure GNT2# is not low when PWROK rises, or PCIe ports 5 & 6 will be disabled.

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PCI

104 28 B1 PCI_AD<0>	D20	AD0
104 28 B1 PCI_AD<1>	E19	AD1
104 28 B1 PCI_AD<2>	D19	AD2
104 28 B1 PCI_AD<3>	A20	AD3
104 28 B1 PCI_AD<4>	D17	AD4
104 28 B1 PCI_AD<5>	A21	AD5
104 28 B1 PCI_AD<6>	A19	AD6
104 28 B1 PCI_AD<7>	C19	AD7
104 28 B1 PCI_AD<8>	A18	AD8
104 28 B1 PCI_AD<9>	B16	AD9
104 28 B1 PCI_AD<10>	A12	AD10
104 28 B1 PCI_AD<11>	E16	AD11
104 28 B1 PCI_AD<12>	A14	AD12
104 28 B1 PCI_AD<13>	G16	AD13
104 28 B1 PCI_AD<14>	A15	AD14
104 28 B1 PCI_AD<15>	B6	AD15
104 28 B1 PCI_AD<16>	C11	AD16
104 28 B1 PCI_AD<17>	A9	AD17
104 28 B1 PCI_AD<18>	D11	AD18
104 28 B1 PCI_AD<19>	B12	AD19
104 28 B1 PCI_AD<20>	C12	AD20
104 28 B1 PCI_AD<21>	D10	AD21
104 28 B1 PCI_AD<22>	C7	AD22
104 28 B1 PCI_AD<23>	F13	AD23
104 28 B1 PCI_AD<24>	E11	AD24
104 28 B1 PCI_AD<25>	E13	AD25
104 28 B1 PCI_AD<26>	E12	AD26
104 28 B1 PCI_AD<27>	D8	AD27
104 28 B1 PCI_AD<28>	A6	AD28
104 28 B1 PCI_AD<29>	E8	AD29
104 28 B1 PCI_AD<30>	D6	AD30
104 28 B1 PCI_AD<31>	A3	AD31

REQ0*	A4	PCI_FW_REQ_L IN 24 104
GNT0*	B7	PCI_FW_GNT_L OUT 104
REQ1*/GPIO50	E18	PCI_REQ1_L IN 7 24 104
GNT1*/GPIO51	C18	TP_SB_GPIO51
REQ2*/GPIO52	B19	PCI_REQ2_L IN 7 24 104
GNT2*/GPIO53	E18	TP_SB_GPIO53
REQ3*/GPIO54	A11	ODD_RST_5VTOL_L OUT 44 103
GNT3*/GPIO55	C10	TP_SB_GPIO55
C/BE0*	C17	PCI_C_BE_L<0> B1 28 104
C/BE1*	E15	PCI_C_BE_L<1> B1 28 104
C/BE2*	E16	PCI_C_BE_L<2> B1 28 104
C/BE3*	E17	PCI_C_BE_L<3> B1 28 104
IRDY*	C8	PCI_IRDY_L B1 24 104
PAR	D9	PCI_PAR B1 28 104
PCIRST*	G6	PCI_RST_L OUT 28
DEVSEL*	D16	PCI_DEVSEL_L B1 24 104
PERR*	A7	PCI_PERR_L B1 24 104
PLOCK*	B7	PCI_LOCK_L B1 24 104
SERR*	E10	PCI_SERR_L B1 24 28 104
STOP*	C16	PCI_STOP_L B1 24 104
TRDY*	C9	PCI_TRDY_L B1 24 104
FRAME*	A17	PCI_FRAME_L B1 24 104
PLTRST*	AG24	PLT_RST_L OUT 28
PCICLK	B10	PCI_CLK33M_SB IN 7 30 105
PME*	G7	TP_PCI_PME_L (INT PU)

INTERRUPT I/F

104 24 B1 INT_PIRQA_L	F9	PIRQA*
104 24 B1 INT_PIRQB_L	B5	PIRQB*
104 24 B1 INT_PIRQC_L	C5	PIRQC*
104 24 B1 INT_PIRQD_L	A10	PIRQD*

PIRQE*/GPIO2	F8	INT_PIRQE_L B1 24 98 104
PIRQF*/GPIO3	G11	INT_PIRQF_L B1 24 104
PIRQG*/GPIO4	F12	DVI_HOTPLUG_DET IN 28
PIRQH*/GPIO5	B3	ODD_PWR_EN_L OUT 24

FireWire INT*

Provide a pull-down on this GPIO if not used.

PCI_FW_GNT_L MAKE_BASE=TRUE
BOOT_LPC_SPI_L

R2415 1K 5% 1/16W MF-LF 402

R2415 pull-down on GNT0# selects SPI ROM by default.

SB BOOT BIOS SELECT

I/F	GNT0#
LPC	1
SPI	0

NOTE: GNT0# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
SPI_CS1# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

6 =PP3V3_S0_SB_PCI

104 24 PCI_FRAME_L	R2423	8.2K
104 24 PCI_IRDY_L	R2424	8.2K
104 24 PCI_TRDY_L	R2425	8.2K
104 24 PCI_STOP_L	R2426	8.2K
104 28 24 PCI_SERR_L	R2427	8.2K
104 24 PCI_DEVSEL_L	R2428	8.2K
104 24 PCI_PERR_L	R2430	8.2K
104 24 PCI_LOCK_L	R2429	8.2K
104 24 PCI_FW_REQ_L	R2432	8.2K
104 24 7 PCI_REQ1_L	R2431	8.2K
104 24 7 PCI_REQ2_L	R2433	8.2K
104 24 INT_PIRQA_L	R2437	8.2K
104 24 INT_PIRQB_L	R2436	8.2K
104 24 INT_PIRQC_L	R2438	8.2K
104 24 INT_PIRQD_L	R2439	8.2K
104 98 24 INT_PIRQE_L	R2440	8.2K
104 24 INT_PIRQF_L	R2441	8.2K
24 ODD_PWR_EN_L	R2442	8.2K

SB PCI, PCIe, DMI, USB

SYNC_DATE=01/08/2008

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=PP3V3_S0_SB_GPIO
=PP3V3_S5_SB_GPIO
NO_REBOOT_MODE

R2500 1K 5% 1/16W MF-LF 402
R2551 8.2K 5% 1/16W MF-LF 402
R2553 8.2K 5% 1/16W MF-LF 402
R2504 10K 5% 1/16W MF-LF 402
R2506 10K 5% 1/16W MF-LF 402
R2510 1K 5% 1/16W MF-LF 402
R2502 10K 5% 1/16W MF-LF 402
R2550 10K 5% 1/16W MF-LF 402
R2552 10K 5% 1/16W MF-LF 402
R2547 10K 5% 1/16W MF-LF 402
R2505 8.2K 5% 1/16W MF-LF 402
R2507 8.2K 5% 1/16W MF-LF 402

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SMB
SMB_CLK
SMB_DATA
TP_CLINK_WLAN_RESET_L
SMB_ME_CLK
SMB_ME_DATA

CLOCKS
PM_RI_L
PM_SUS_STAT_L
PM_SYSRST_L
PM_BMBUSY_L
LINDACARD_GPIO

SYS GPIO
PM_STPPCI_L
PM_STPCPU_L
PM_CLKRUN_L
PCIE_WAKE_L
INT_SERIRQ
PM_THRM_L
VR_PWRGD_CLKEN
TP_SB_TP7

GPIO
SMC_RUNTIME_SCI_L
SMC_WAKE_SCI_L
PCI_PME_FW_L
SB_GPIO6
LAN_PHYPC
EXTGPU_RST_L
SB_GPIO18
TP_SB_GPIO20
SB_SCLOCK
SATA_B_PWR_EN_L
FWH_MFG_MODE
SB_SATA_CLKREQ_L
SB_SLOAD
SB_SDATAOUT<0>
SB_SDATAOUT<1>

MISC
SB_SPKR
NB_SB_SYNC_L
TP_SB_TP3

Test access required
for XOR chain testing.

SATA GPIO
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA2GP/GPIO36
SATA3GP/GPIO37

R2532 10K 5% 1/16W MF-LF 402
R2535 10K 5% 1/16W MF-LF 402
R2533 10K 5% 1/16W MF-LF 402
R2534 10K 5% 1/16W MF-LF 402

RSVD_EXTGPU_LVDS_EN
SATA_B_DET_L
SB_GPIO36
SB_CRT_TVOUT_MUX_L

POWER MGT
CLK14
CLK48
SUSCLK
SLP_S3*
SLP_S4*
SLP_S5*
S4_STATE*/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW*
PWRBTN*
LAN_RST*
RSMRST*
CK_PWRGD
CLPWROK
SLP_M*

SB_CLK14P3M_TIMER
SB_CLK48M_USBCTLR
SUS_CLK_SB
PM_SLP_S3_L
TP_PM_SLP_S4_L
PM_SLP_S5_L
PM_S4_STATE_L
PM_SB_PWROK
PM_DPRSLPVR
PM_BATLOW_L
PM_PWRBTN_L
PM_LAN_ENABLE
PM_RSMRST_L
CLK_PWRGD
See note below
=SB_CLINK_MPWROK
TP_PM_SLP_M_L

NOTE: DPRSLPVR HAS INT 20K PD ENABLED
AT BOOT/RESET FOR STRAPPING FUNCTION

PM_LAN_ENABLE must remain deasseted
until VccCL3_3, VccLAN3_3 and VccLAN1_05
have been up for at least 1ms.

R2524 100K 5% 1/16W MF-LF 402
R2525 10K 5% 1/16W MF-LF 402

CONTROLLER LINK
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST*
MEM_LED/GPIO24
ME_EC_ALERT/GPIO10
EC_ME_ALERT/GPIO14
WOL_EN/GPIO9

CLINK_NB_CLK
TP_CLINK_WLAN_CLK
CLINK_NB_DATA
TP_CLINK_WLAN_DATA
SB_CLINK_VREF0
SB_CLINK_VREF1
CLINK_NB_RESET_L
CPU_SET_SPEED
SB_GPIO10_CL1
SB_GPIO14_CL2
WOL_EN

=PP3V3_S0MWOL_SB_CLINK0
R2526 3.24K 1% 1/16W MF-LF 402
C2500 0.1uF 10% 16V X5R 402
R2527 453 1% 1/16W MF-LF 402

=PP3V3_S5_SB_CLINK1
R2528 3.24K 1% 1/16W MF-LF 402
C2501 0.1uF 10% 16V X5R 402
R2529 453 1% 1/16W MF-LF 402

R2523 100K 5% 1/16W MF-LF 402

NOTE: ICH CLPWROK input must be PWRGD signal for
PP3V3_S0M, PP3V3_S0MWOL, PP1V8_S3M, PP1V25_S0M,
PP1V05_S0M, PP0V9_S3M and PP0V9_S0M.
If ME/AMT is not used, short CLPWROK to PWROK.

=PP3V3_S5_SB

R2511 10K 5% 1/16W MF-LF 402
R2515 10K 5% 1/16W MF-LF 402
R2514 100K 5% 1/16W MF-LF 402
R2512 0 5% 1/16W MF-LF 402 NOSTUFF
R2516 10K 5% 1/16W MF-LF 402 NOSTUFF

LINDACARD_GPIO
CPU_SET_SPEED
FWH_MFG_MODE

R2530 10K 1% 1/16W MF-LF 402 =PP3V3_S0_SB_GPIO
R2531 10K 1% 1/16W MF-LF 402
R2596 10K 1% 1/16W MF-LF 402
R2597 10K 1% 1/16W MF-LF 402
R2536 10K 1% 1/16W MF-LF 402 =PP3V3_S5_SB
R2544 8.2K 5% 1/16W MF-LF 402
R2545 10K 1% 1/16W MF-LF 402
R2598 10K 1% 1/16W MF-LF 402
R2546 10K 1% 1/16W MF-LF 402

SATA_B_PWR_EN_L
PCI_PME_FW_L
SB_GPIO6
EXTGPU_RST_L
PM_RI_L
PM_BATLOW_L
LAN_PHYPC
SB_GPIO10_CL1
SB_GPIO14_CL2

SB Pwr Mgt, GPIO, Clink

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VSS
VSS
VSS_NCTF

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6 uA S0-G3 — PP3V3_G3_SB_RTC — VCCRTC
1 mA — PP5V_S0_SB_V5REF — V5REF
1 mA S0-S5 — PP5V_S5_SB_V5REF_SUS — V5REF_SUS
657 mA — PP1V5_S0_SB_VCC1_5_B — VCC1_5_B — VCCA3GP
47 mA — PP1V5_S0_SB_VCCSATAPLL — VCCSATAPLL
=PP1V5_S0_SB_VCC1_5_A_ARX — VCC1_5_A — ARX
=PP1V5_S0_SB_VCC1_5_A_ATX — VCC1_5_A — ATX
1080 mA (VCC1_5_A total)
=PP1V5_S0_SB_VCC1_5_A — VCC1_5_A
=PP1V5_S0_SB_VCC1_5_A_USB_CORE — VCC1_5_A — USB CORE
10 mA — =PP1V5_S0_SB_VCCUSBPLL — VCCUSBPLL
VCC1_5_A24
TP_VCCLAN1_05_INTERNAL_REG1
TP_VCCLAN1_05_INTERNAL_REG2 — VCCLAN1_05
19 mA S0, 63 mA M1 & WOL — =PP3V3_S0MWOL_SB_VCCCL3_3 — VCCCL3_3
23 mA — PP1V5_S0_SB_VCCGLANPLL — VCCGLANPLL
80 mA — =PP1V5_S0_SB_VCCGLAN1_5 — VCCGLAN1_5 — GLAN POWER
1 mA — =PP3V3_S0_SB_VCCGLAN3_3 — VCCGLAN3_3

CORE
VCC1_05 — =PPVCORE_S0_SB — 1130 mA
VCCDMIPLL — PP1V5_S0_SB_VCCDMIPLL — 23 mA
VCC_DMI — =PP1V25_S0_SB_DMI — 50 mA
V_CPU_IO — =PP1V05_S0_SB_CPU_IO — 1 mA
VCC3_3 — =PP3V3_S0_SB_VCC3_3_DMI
VCC3_3 — =PP3V3_S0_SB_VCC3_3_SATA
VCCP CORE
VCC3_3 — =PP3V3_S0_SB_VCC3_3_VCCPCORE
IDE
VCC3_3 — =PP3V3_S0_SB_VCC3_3_IDE — 442 mA
PCI
VCC3_3 — =PP3V3_S0_SB_VCC3_3_PCI
(VCC3_3 total)
VCCHDA — =PP3V3R1V5_S0_SB_VCCHDA — 32 mA
VCCSUSHDA — =PP3V3_S5_SB_3V3_VCCSUSHDA — 11 mA S0, 1 mA S3-S5
VCCSUS1_05 — TP_VCCSUS1_05_INTERNAL_REG1
VCCSUS1_05 — TP_VCCSUS1_05_INTERNAL_REG2
VCCSUS1_5 — TP_VCCSUS1_5_INTERNAL_REG1
VCCSUS1_5 — TP_VCCSUS1_5_INTERNAL_REG2
VCCSUS3_3 — =PP3V3_S5_SB_VCCSUS3_3
VCCP SUS
VCCSUS3_3
VCCP USB
VCCSUS3_3 — =PP3V3_S5_SB_VCCSUS3_3_USB
(VCCSUS3_3 total) — 117 mA S0, 44 mA S3-S5
VCCCL1_05 — TP_VCCCL1_05_INTERNAL_REG
VCCCL1_5 — VCCCL1_5V
VCCLAN3_3 — =PP3V3_S0MWOL_SB_VCCLAN3_3 — 19 mA S0, 51 mA M1 & WOL

C2600 1uF 10% 6.3V CERM 402
C2601 0.1uF 20% 10V CERM 402

NOTE:
VccHDA and VccSusHDA can be 1.5V or 3.3V depending on VIO of HD Audio interface.
Current figures provided assume 1.5V.

Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.

SB Power & Ground

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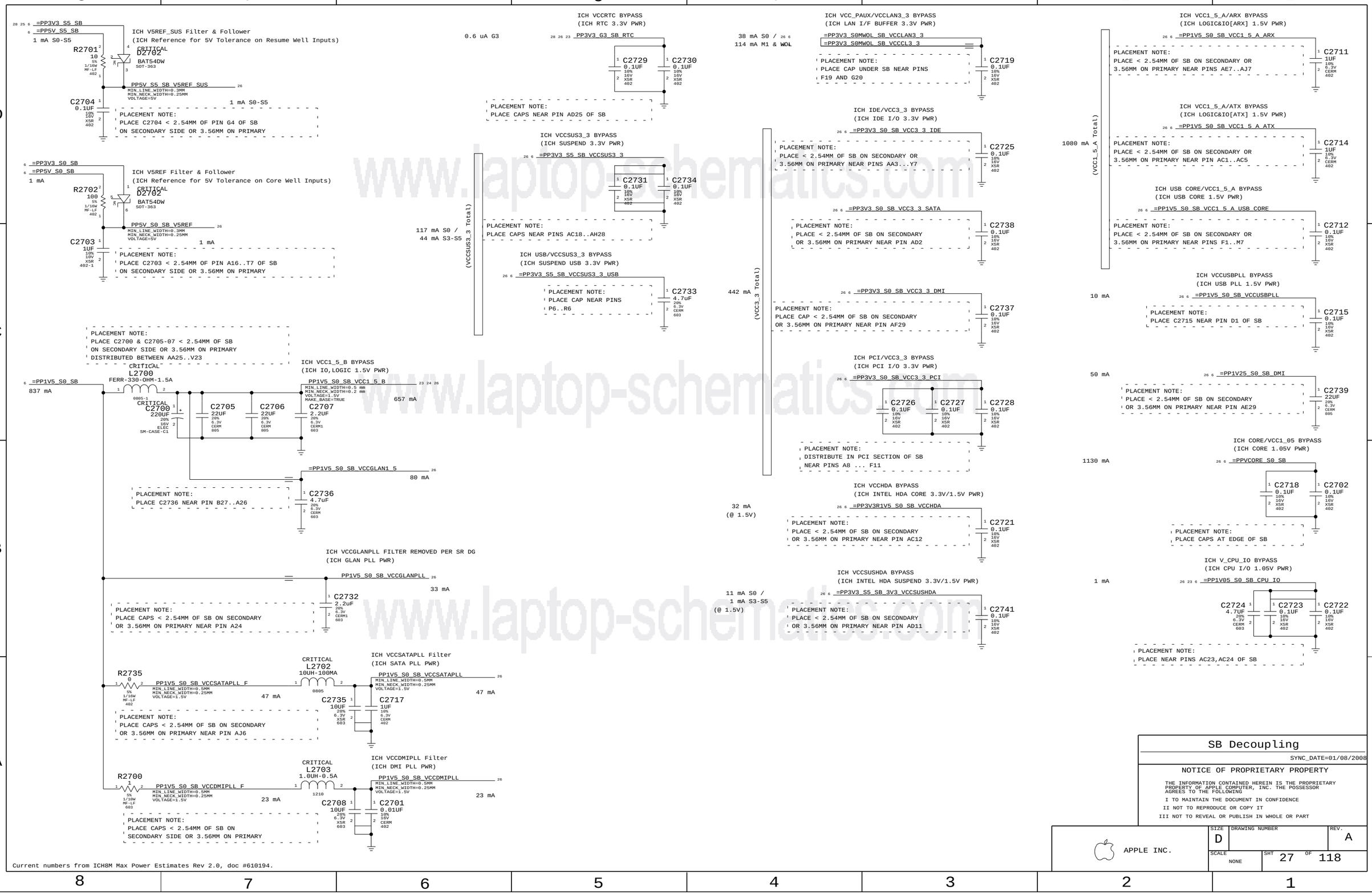

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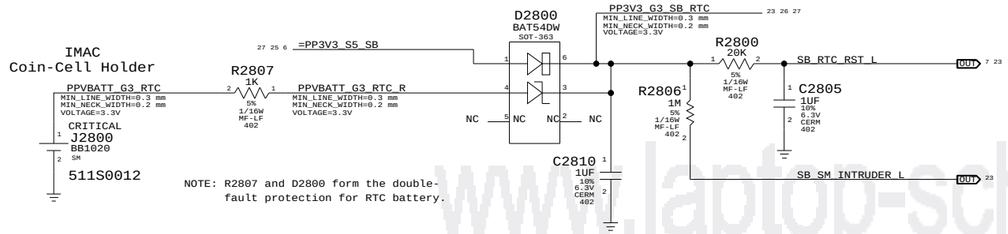
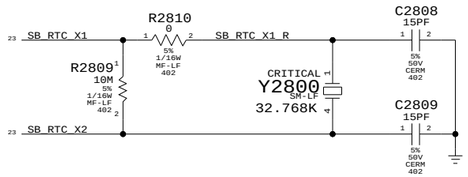
RTC Power Sources



SB RTC Crystal



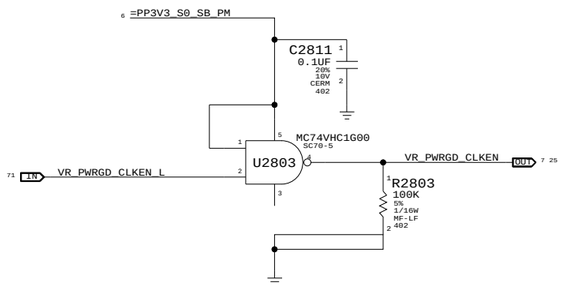
CPU VCORE FORCEPSI UNUSED

CPU_PSI_L → IMVP6_PSI_L (MAKE_BASE=TRUE)

PWROK = CLINK PWROK FOR NO ME

=SB_CLINK_MPWROK → PM_SB_PWROK (MAKE_BASE=TRUE)

VRMPWRGD INVERTER

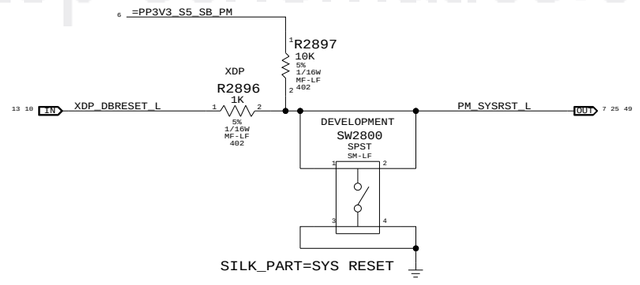


UNUSED PCI BUS

PCI_AD<0>	MAKE_BASE=TRUE	TP_PCI_AD_0
PCI_AD<1>	MAKE_BASE=TRUE	TP_PCI_AD_1
PCI_AD<2>	MAKE_BASE=TRUE	TP_PCI_AD_2
PCI_AD<3>	MAKE_BASE=TRUE	TP_PCI_AD_3
PCI_AD<4>	MAKE_BASE=TRUE	TP_PCI_AD_4 NO_TEST=TRUE
PCI_AD<5>	MAKE_BASE=TRUE	TP_PCI_AD_5
PCI_AD<6>	MAKE_BASE=TRUE	TP_PCI_AD_6
PCI_AD<7>	MAKE_BASE=TRUE	TP_PCI_AD_7
PCI_AD<8>	MAKE_BASE=TRUE	TP_PCI_AD_8
PCI_AD<9>	MAKE_BASE=TRUE	TP_PCI_AD_9
PCI_AD<10>	MAKE_BASE=TRUE	TP_PCI_AD_10
PCI_AD<11>	MAKE_BASE=TRUE	TP_PCI_AD_11
PCI_AD<12>	MAKE_BASE=TRUE	TP_PCI_AD_12
PCI_AD<13>	MAKE_BASE=TRUE	TP_PCI_AD_13
PCI_AD<14>	MAKE_BASE=TRUE	TP_PCI_AD_14
PCI_AD<15>	MAKE_BASE=TRUE	TP_PCI_AD_15
PCI_AD<16>	MAKE_BASE=TRUE	TP_PCI_AD_16
PCI_AD<17>	MAKE_BASE=TRUE	TP_PCI_AD_17
PCI_AD<18>	MAKE_BASE=TRUE	TP_PCI_AD_18
PCI_AD<19>	MAKE_BASE=TRUE	TP_PCI_AD_19
PCI_AD<20>	MAKE_BASE=TRUE	TP_PCI_AD_20
PCI_AD<21>	MAKE_BASE=TRUE	TP_PCI_AD_21
PCI_AD<22>	MAKE_BASE=TRUE	TP_PCI_AD_22
PCI_AD<23>	MAKE_BASE=TRUE	TP_PCI_AD_23
PCI_AD<24>	MAKE_BASE=TRUE	TP_PCI_AD_24
PCI_AD<25>	MAKE_BASE=TRUE	TP_PCI_AD_25
PCI_AD<26>	MAKE_BASE=TRUE	TP_PCI_AD_26
PCI_AD<27>	MAKE_BASE=TRUE	TP_PCI_AD_27
PCI_AD<28>	MAKE_BASE=TRUE	TP_PCI_AD_28
PCI_AD<29>	MAKE_BASE=TRUE	TP_PCI_AD_29
PCI_AD<30>	MAKE_BASE=TRUE	TP_PCI_AD_30
PCI_AD<31>	MAKE_BASE=TRUE	TP_PCI_AD_31
PCI_C_BE_L<0>	MAKE_BASE=TRUE	TP_PCI_C_BE_L_0
PCI_C_BE_L<1>	MAKE_BASE=TRUE	TP_PCI_C_BE_L_1
PCI_C_BE_L<2>	MAKE_BASE=TRUE	TP_PCI_C_BE_L_2
PCI_C_BE_L<3>	MAKE_BASE=TRUE	TP_PCI_C_BE_L_3
PCI_RST_L	MAKE_BASE=TRUE	TP_PCI_RST_L
PCI_PAR	MAKE_BASE=TRUE	TP_PCI_PAR

NO TEST DUE TO ROUTING

TP_LAN_D2R<2>		NO_TEST=TRUE
TP_CLINK_WLAN_DATA		NO_TEST=TRUE
PCI_SERR_L		NO_TEST=TRUE



Platform Reset Connections

Unbuffered

PLT_RST_L	R2885 47	NB_RESET_L
	R2881 100	DEBUG_RESET_L
	R2883 47	SMC_LRESET_L
	R2891 100	MINI_RESET_L
	R2892 47	ENET_RESET_L
	R2890 100	PEG_RESET_L
	R2893 47	FW_RESET_L

RE-PURPOSED GPIOS

SB_GPIO6 → GPU_PRESENT (MAKE_BASE=TRUE)

20_INCH_LCD

R2710 0

INV_EN_BL_OR_PANEL_ID → PANEL_ID (MAKE_BASE=TRUE) → TP_SB_GPIO20

TO ACDC ON M72 ONLY

UNUSED GPIOS

DVI_HOTPLUG_DET → SB_GPIO4 (MAKE_BASE=TRUE) R2850 10K

EXTGPU_RST_L		TP_EXTGPU_RST_L (MAKE_BASE=TRUE)
EXTGPU_PWR_EN		TP_EXTGPU_PWR_EN (MAKE_BASE=TRUE)
LAN_ENERGY_DET		TP_LAN_ENERGY_DET (MAKE_BASE=TRUE)

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SB Misc

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SCALE: NONE

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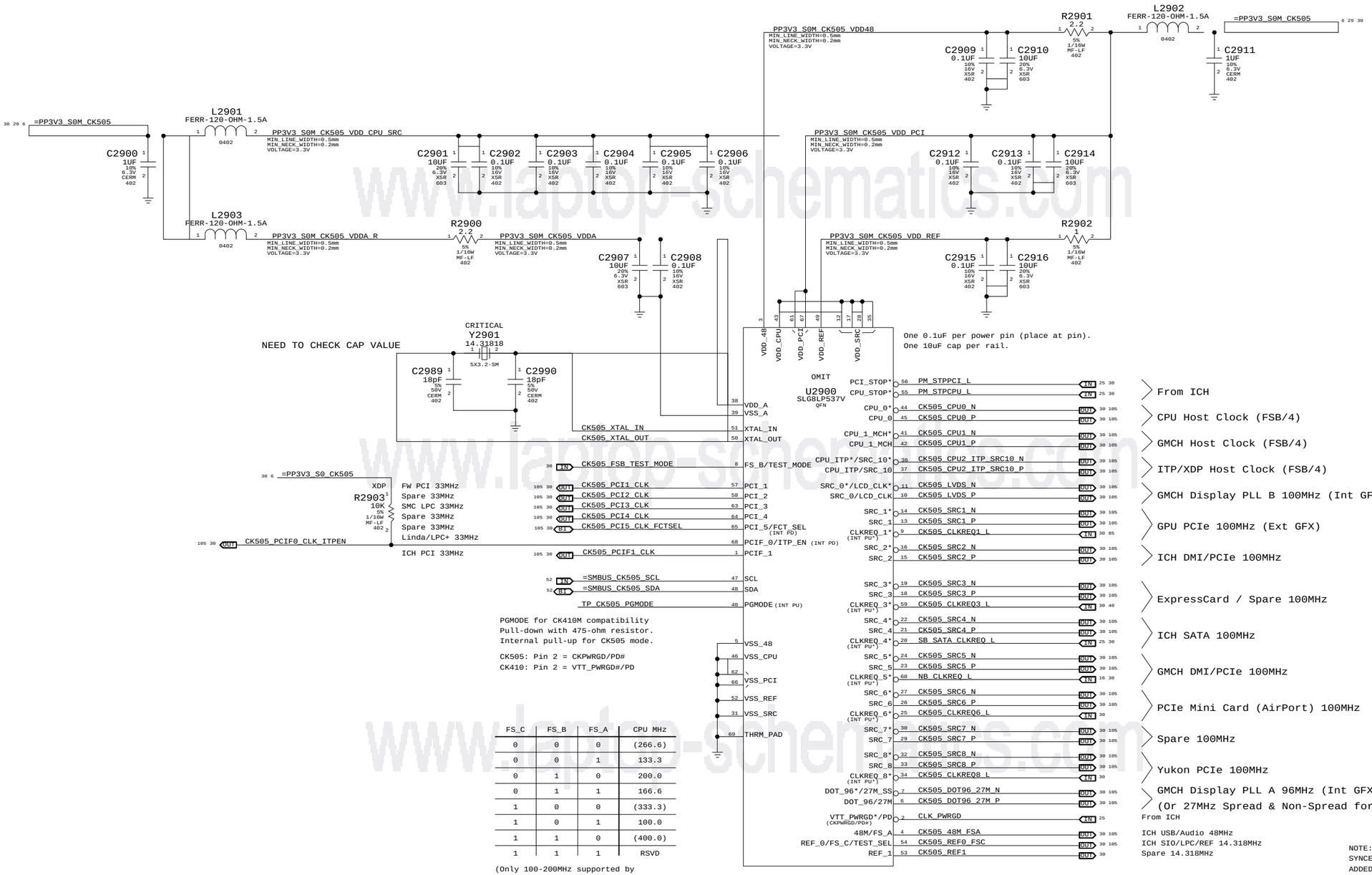

FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

(Only 100-200MHz supported by SLG8LP536 and CY28545-5)

FCT_SEL	PIN 6	PIN 7	PIN 10	PIN 11	
0	DOT_96+	DOT_96-	LCD_CLK+	LCD_CLK-	(For Internal Graphics)
1	27M	27M w/SS	SRC_0+	SRC_0-	(For External Graphics)

NOTE:
SYNCED FROM T9_MLB_NOME
ADDED 475-OHM RESISTOR TO NB_CLKREQ_L PER INTEL
DELETED RES AFTER INTEL SAID IT'S NOT NEEDED!

Clock (CK505)

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D		A
SCALE: NONE	SHT 29 OF 118	

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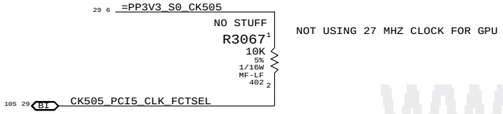
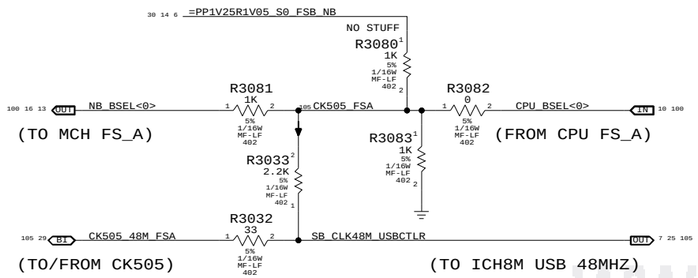
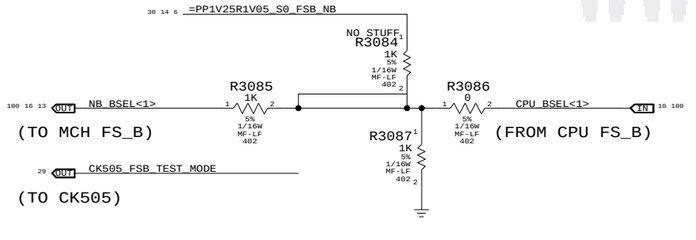
CK505 Configuration Straps

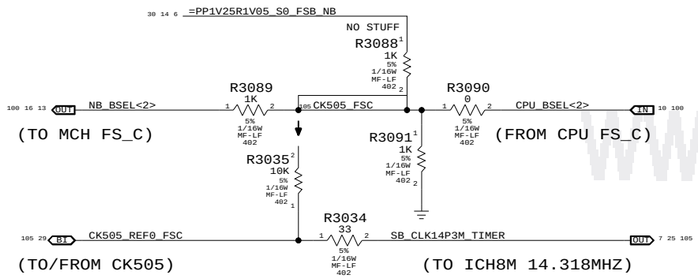
FCT_SEL (GFX clock select)



FS_A, FS_B, FS_C (Host clock freq select)





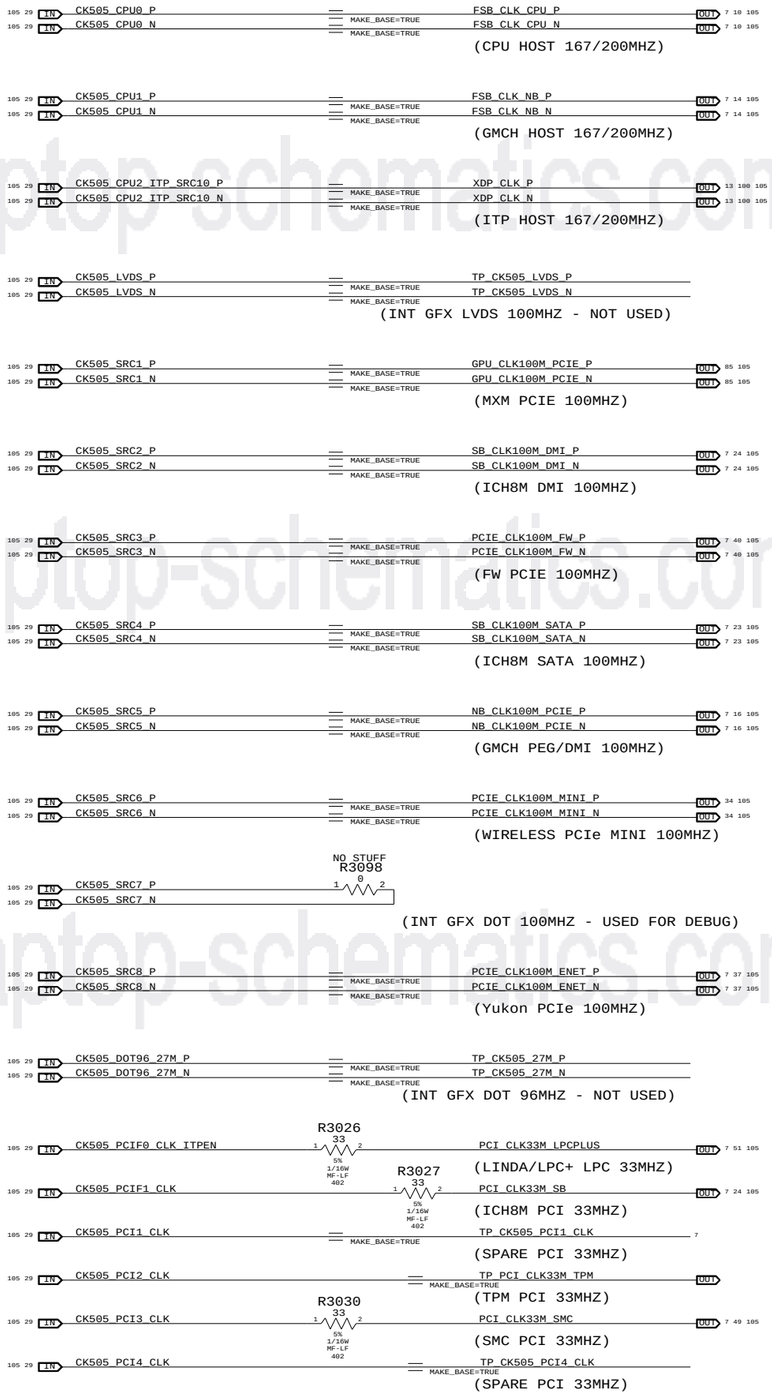


FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

NO STUFF R3082, R3086 & R3090
for manual CPU clk frequency.

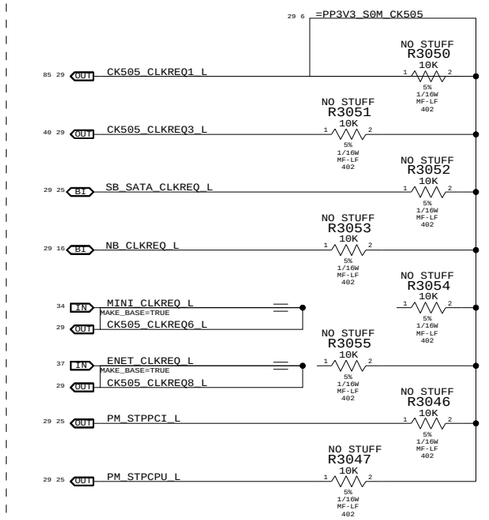
CLK Termination

(Note: HOST/SRC/GFX clock termination kept on T9 for Cypress CY28545-5 compatibility)



CLKREQ Controls

Silego SL8GLP537 has internal
PULL-UPS ON ALL CLKREQ# PINS?



Unused Clocks

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Clock Termination

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SCALE: NONE	SHT 30 OF 118	

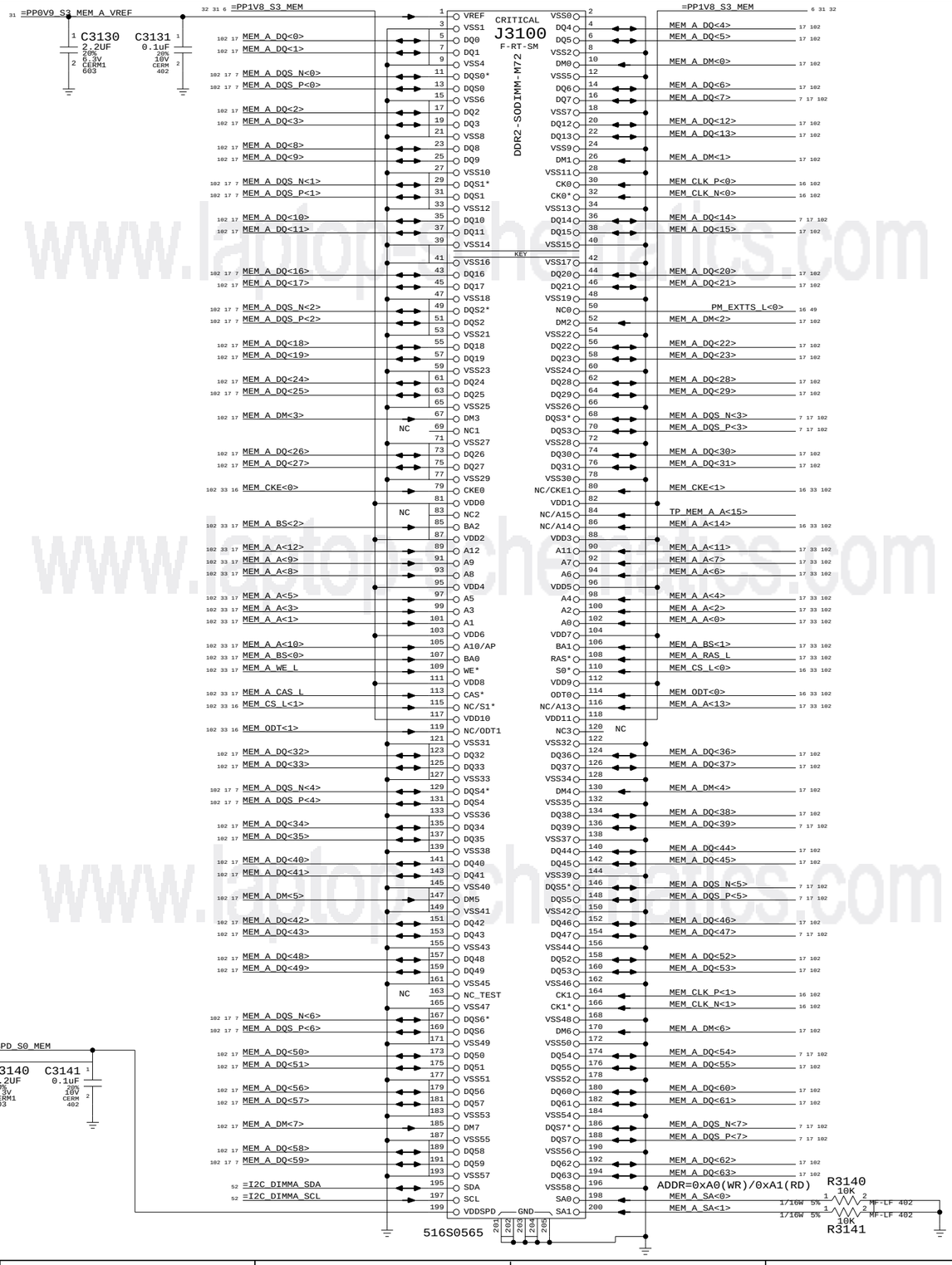
Page Notes

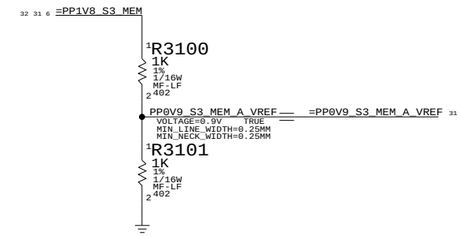
Power aliases required by this page:
- =PP1V8_S3_MEM
- =PP0V9_S3_MEM_VREF
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

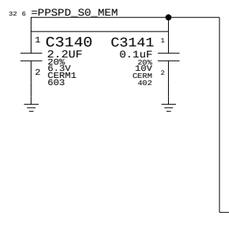
NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.





DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

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D		A

SCALE: NONE

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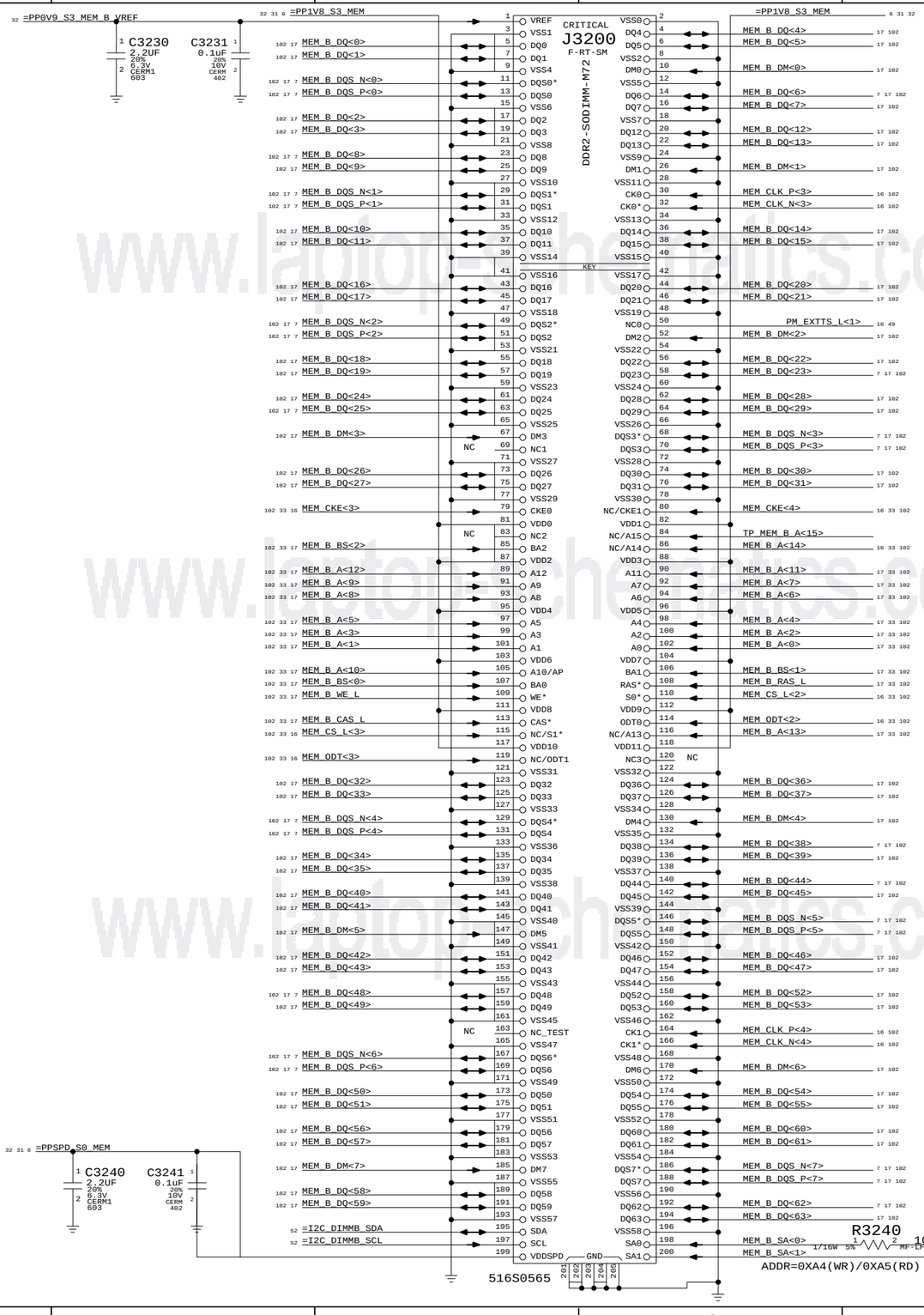
Page Notes

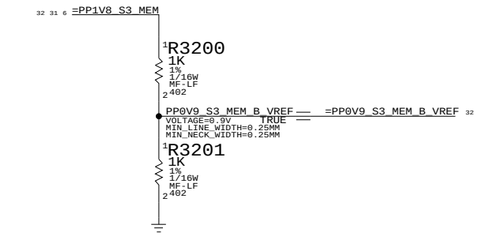
Power aliases required by this page:
- =PP1V8_S3_MEM
- =PP0V9_S3_MEM_VREF
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.





DDR2 Bypass Caps

(For return current)

DDR2 SO-DIMM Connector B

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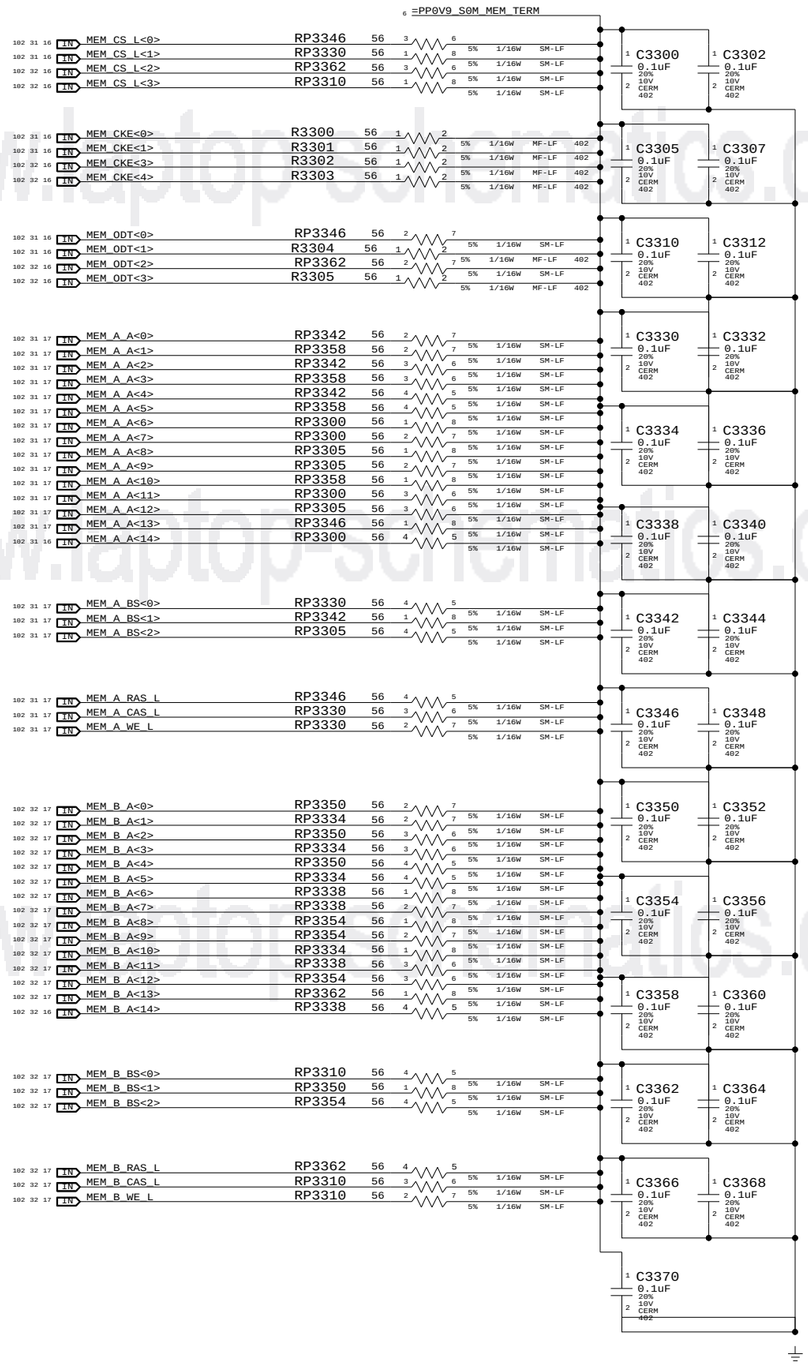
One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



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Memory Active Termination

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D		A

SCALE	SHT	OF
NONE	33	118

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3.3V_S3_CURRENT	D0-D2_D3HOT	D3COLD
MAX CONT:	1100MA	250MA
MAX PEAK	2750MA	2750MA
1.5V_CURRENT		
MAX CONT:	375MA	N/A
MAX PEAK	560MA	N/A

NOTE: CURRENT DATA PER 5/16/2005 PCIE MINI CEM ECN

NO STUFF
R3400
0
5%
1/16W
MF-LF
402

NO STUFF
R3401
0
5%
1/16W
MF-LF
402

CRITICAL
J3400
ASOB226-S80N-7F
F-RT-SM

37 25 OUT PCIE_WAKE_L
RSVD_MINI_WLAN_ACTIVE
RSVD_MINI_BT_ACTIVE
30 OUT MINI_CLKREQ_L
105 30 IN PCIE_CLK100M_MINI_N
105 30 IN PCIE_CLK100M_MINI_P
RESERVED
RESERVED
MINI_RESET_L IN 28
=SMBUS_MINI_SCL IN 52
=SMBUS_MINI_SDA BI 52
USB_MINI_N BI 24 103
USB_MINI_P BI 24 103
PP1V05_S0 6 7 73
=PP3V3_S3_MINI 6
=PP1V5_S0_MINI 6

NC
516S0391

C3410 0.1uF 20% 10V CERM 402
C3420 0.1uF 20% 10V CERM 402
C3421 10uF 20% 6.3V X5R 603
C3400 0.1uF 20% 10V CERM 402
C3401 10uF 20% 6.3V X5R 603

104 24 7 OUT PCIE_MINI_D2R_N
104 24 7 OUT PCIE_MINI_D2R_P

PLACEMENT_NOTE=Place close to U2300.
C3431
0.1uF
104 24 IN PCIE_MINI_R2D_C_N
10% 16V X5R 402

PLACEMENT_NOTE=Place close to U2300.
C3430
0.1uF
104 24 IN PCIE_MINI_R2D_C_P
10% 16V X5R 402

104 PCIE_MINI_R2D_N
104 PCIE_MINI_R2D_P

CLINK_WLAN_CLK = TP_CLINK_WLAN_CLK 25
MAKE_BASE=TRUE
CLINK_WLAN_DATA = TP_CLINK_WLAN_DATA 25 28
MAKE_BASE=TRUE
CLINK_WLAN_RESET_L = TP_CLINK_WLAN_RESET_L 25
MAKE_BASE=TRUE

STANDOFF FOR J3400
CRITICAL
SDF3400
STDOFF-4OD5.6H-1.35-TH
SDF3400_1
860-0691

R3410
0
5%
1/16W
MF-LF
402

PCI-E MiniCard Connector

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Page Notes

Power aliases required by this page:
- =PP3V3_ENET_PHY (EC / Ultra)
- =PP1V9R2V5_ENET_PHY (2.5V / 1.8V)

- =PP1V2_ENET_PHY

Signal aliases required by this page:
- =ENET_CLKREQ_L (NC/TP for Yukon EC)
- =ENET_VMAIN_AVLBL (See note by pin)

38 =PP1V2_ENET_PHY

Yukon Ultra

No link: 130 mA
10 Mbps: 130 mA
100 Mbps: 150 mA
1000 Mbps: 290 mA

NOSTUFF C3700 4.7UF 20% 6.3V CERM 603
C3701 C3702 C3703 C3704 C3705 C3706 C3707 C3708 1UF 10% 10V X5R 402

38 =PP3V3_ENET_PHY

Yukon Ultra

No link: 60 mA
10 Mbps: 70 mA
100 Mbps: 70 mA
1000 Mbps: 80 mA

NOSTUFF C3710 4.7UF 20% 6.3V CERM 603
C3711 C3712 C3713 C3714 C3715 1UF 10% 10V X5R 402

39 38 PP1V9_S3_ENET

R3720 0 5% 1/10W MF-LF 402

104 PP1V9_ENET_PHY_AVDD
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V

Yukon Ultra (1.8V)

No link: 0 mA
10 Mbps: 30 mA
100 Mbps: 40 mA
1000 Mbps: 150 mA

C3720 4.7UF 20% 6.3V CERM 603
C3721 C3722 C3723 C3724 1UF 10% 10V X5R 402

104 24 7 OUT PCIE_ENET_D2R_P
104 24 7 OUT PCIE_ENET_D2R_N
C3735 0.1uF 10% 16V X5R 402
C3736 0.1uF 10% 16V X5R 402
PLACEMENT_NOTE=Place C3730 close to southbridge.
104 24 IN PCIE_ENET_R2D_C_P
104 24 IN PCIE_ENET_R2D_C_N
C3730 0.1uF 10% 16V X5R 402
C3731 0.1uF 10% 16V X5R 402
PLACEMENT_NOTE=Place C3731 close to southbridge.
105 30 7 IN PCIE_CLK100M_ENET_P
105 30 7 IN PCIE_CLK100M_ENET_N
30 OUT ENET_CLKREQ_L
34 25 OUT PCIE_WAKE_L
28 7 IN ENET_RESET_L
104 39 BI ENET_MDI_P<0>
104 39 BI ENET_MDI_N<0>
104 39 BI ENET_MDI_P<1>
104 39 BI ENET_MDI_N<1>
104 39 BI ENET_MDI_P<2>
104 39 BI ENET_MDI_N<2>
104 39 BI ENET_MDI_P<3>
104 39 BI ENET_MDI_N<3>

R3740 R3741 R3742 R3743 R3744 R3745 R3746 R3747 49.9 1% 1/16W MF-LF 402
ENET_MDI0 ENET_MDI1 ENET_MDI2 ENET_MDI3
C3740 C3742 C3744 C3746 0.001UF 10% 50V CERM 402

C3750 27PF 5% 50V CERM 402
CRITICAL Y3750 25.0000M SM-3-LF 197S0167 CL = 20PF
C3751 27PF 5% 50V CERM 402
ENET_CLK25M_XTALI
ENET_CLK25M_XTALO

U3700 88E8058 QFN CRITICAL

108 PCIE_ENET_D2R_C_P	49	TX_P	PCI EXPRESS
108 PCIE_ENET_D2R_C_N	50	TX_N	
108 7 PCIE_ENET_R2D_P	54	RX_P	
108 7 PCIE_ENET_R2D_N	53	RX_N	
105 30 7 PCIE_CLK100M_ENET_P	55	REFCLKP	
105 30 7 PCIE_CLK100M_ENET_N	56	REFCLKN	
ENET_CLKREQ_L	42	CLKREQ*	
PCIE_WAKE_L	6	WAKE*	
ENET_RESET_L	5	PERST*	
ENET_MDI_P<0>	17	MDIP0	MEDIA
ENET_MDI_N<0>	18	MDIN0	
ENET_MDI_P<1>	20	MDIP1	
ENET_MDI_N<1>	21	MDIN1	
ENET_MDI_P<2>	26	MDIP2	
ENET_MDI_N<2>	27	MDIN2	
ENET_MDI_P<3>	30	MDIP3	
ENET_MDI_N<3>	31	MDIN3	
ENET_CLK25M_XTALI	15	XTALI	MAIN CLK
ENET_CLK25M_XTALO	14	XTALO	
	65	THRML_PAD	

NC_32 NC_51 NC_52 NC_57 NC_64 AVDD0 AVDD1 AVDD2 AVDD3 VDDO_TTL0 VDDO_TTL1 VDDO_TTL2 VDDO_TTL3 AVDDH VDD0 VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7

R3760 4.7K 5% 1/16W MF-LF 402

LOM_DISABLE* 10 — ENET_LOM_DIS_L
VAUX_AVLBL 12
SWITCH_VAUX 9 NC
VMAIN_AVLBL 47 — Must be high in S0 state (can use PP3V3_S0 as input) =ENET_VMAIN_AVLBL IN 38
SWITCH_VCC 11 NC
CTRL18 4 — TP_YUKON_CTRL18 OUT 38
CTRL12 3 — TP_YUKON_CTRL12 OUT 38
RSET 16 — YUKON_RSET

ANALOG

LED_ACT*	59	ENET_LED_ACT_L 39
LED_LINK10/100*	60	ENET_LED_LINK10_100_L 39
LED_LINK1000*	62	ENET_LED_LINK1000_L 39
LED_DUPLEX*	63	ENET_LED_LINK_L 39

R3765 4.99K 1% 1/16W MF-LF 402

LED

SPI
(IPU) SPI_DO 34 NC
(IPU) SPI_DI 35 NC
(IPU) SPI_CLK 37 NC
(IPU) SPI_CS 36 NC

TWSI
(IPU) VPD_CLK 38 — YUKON_VPD_CLK
(IPU) VPD_DATA 41 — YUKON_VPD_DATA

TEST/RSVD
(IPD) TESTMODE 46
RSVD_24 24 NC
RSVD_25 25 NC
RSVD_29 29 NC
RSVD_43 43 NC

VPD ROM

C3780 0.1UF 10% 16V X5R 402
R3780 4.7K 5% 1/16W MF-LF 402
R3781 4.7K 5% 1/16W MF-LF 402

E2	3		
NC1	2	NC	
NC0	1	NC	
WC*	7		
VCC	8		
SDA	5		
SCL	6		
VSS	4		

U3780 M24C08 SO8 OMIT CRITICAL

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S2060	1	IC,FLASH,88E8058 ETHERNET VPD,IIC,SO8	U3780	CRITICAL	

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Ethernet (Yukon)

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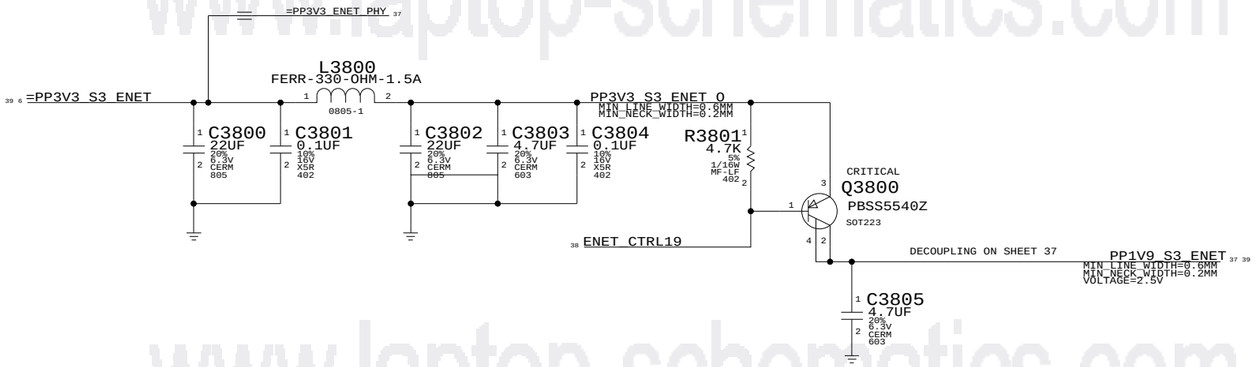
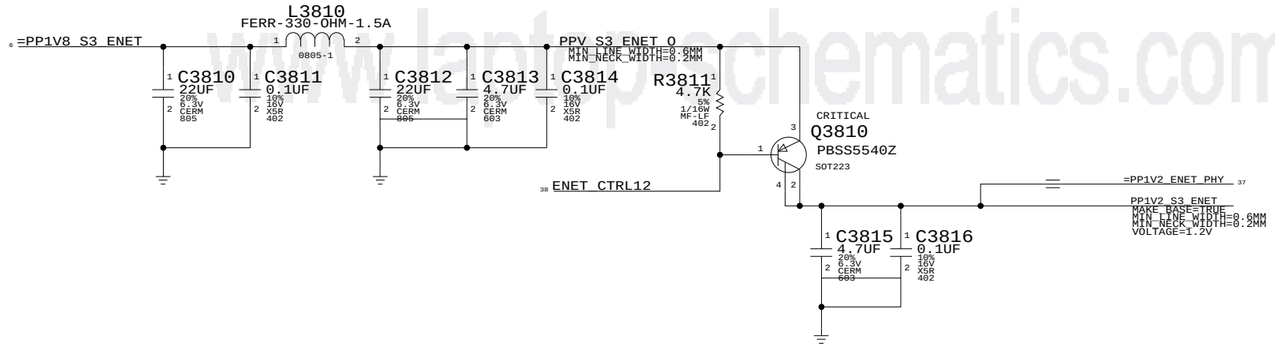
D		A
SCALE: NONE	SHT 37 OF 118	

YUKON 1.9V SUPPLY



YUKON 1.2 RAIL SUPPLY



YUKON T9 ALIASES

37 TP_YUKON_CTRL18 = ENET_CTRL19 38
MAKE_BASE=TRUE

37 TP_YUKON_CTRL12 = ENET_CTRL12 38
MAKE_BASE=TRUE

37 =ENET_VMAIN_AVLBL = =PP3V3_S0_ENET 6

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YUKON/ULTRA SUPPORT

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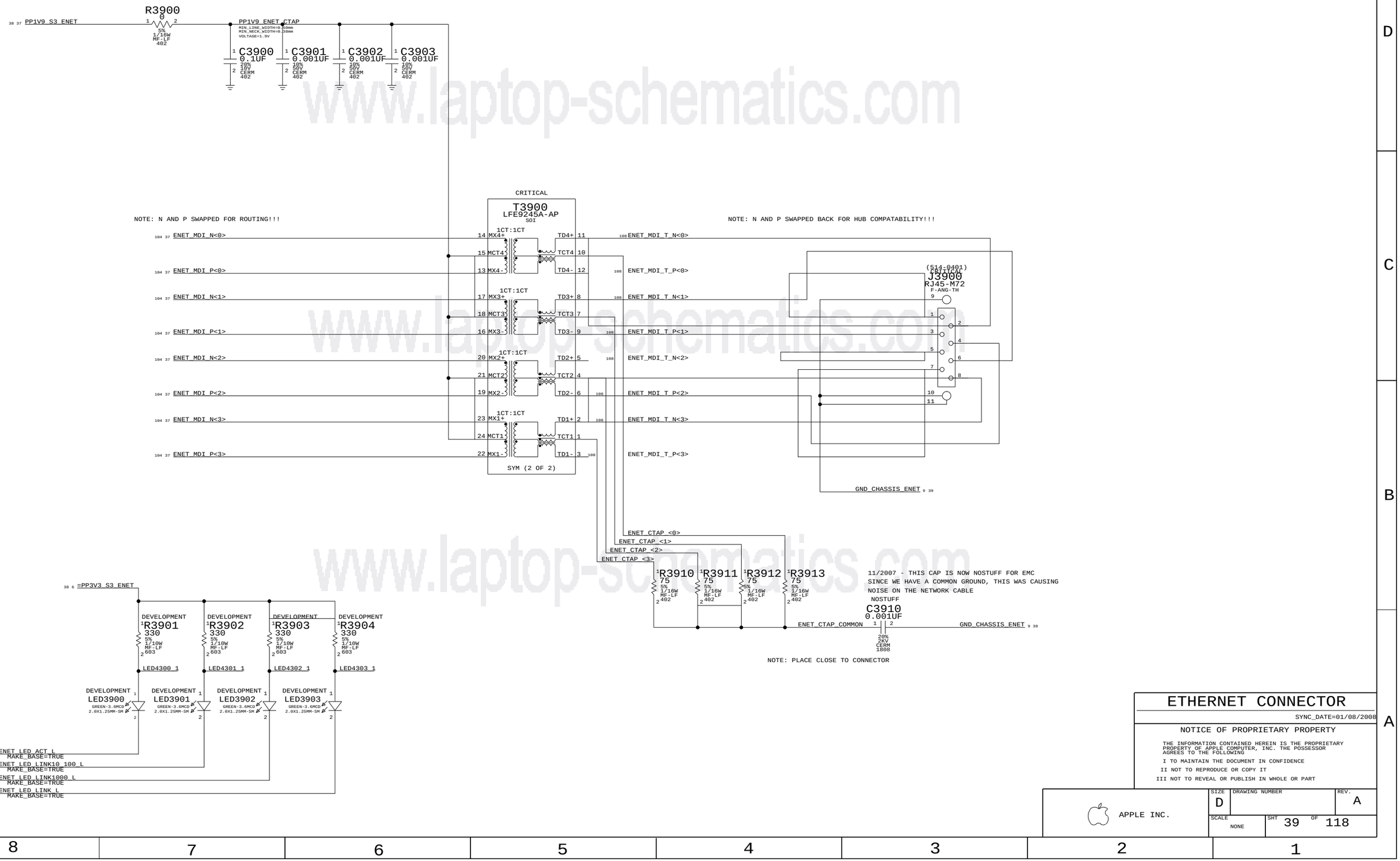
D		A

SCALE	SHT	OF
NONE	38	118



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ETHERNET CONNECTOR

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D		A

SCALE	SHT	OF
NONE	39	118

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=PP3V3_S5_FW 6 40 42 43
PP3V3_S5_FW_AVDD1 42
PP1V0_S5_FW_AVDD 42
PP3V3_S5_FW_AVDD2 42
=PP3V3_S5_FW 6 40 42 43
42 PP1V0_S5_FW_DVDD

A1 B1 B12 C13 E2 E10 H2 H12 K2 L1 M12 N3 N11 C1 C12 F1 G12 J1 L3 L11 M2 A12 D5 D6 D8 L5 L10 L6 L9 K12

VDD10 VDD33 VDDH VP VP25 VREG_PWR

LAYOUT NOTE: PLACE C4010,C4011 CLOSE TO SOUTHBRIDGE(U2300)

C4010 0.1UF 10% 16V X5R 402 — PCIE_FW_R2D_C_N 42 104
C4011 0.1UF 10% 16V X5R 402 — PCIE_FW_R2D_C_P 42 104

CRITICAL
U4000
FW643
BGA
OMIT PCI EXPRESS PHY

NC B13	ATBUSB	PCIE_RXD0N	N8 — PCIE_FW_R2D_N
NC A13	ATBUSH	PCIE_RXD0P	N7 — PCIE_FW_R2D_P
NC A11	ATBUSN	PCIE_TXD0N	N5 — PCIE_FW_D2R_C_N (C4020 0.1UF 10% 16V X5R 402) — PCIE_FW_D2R_N 7 42 104
		PCIE_TXD0P	N6 — PCIE_FW_D2R_C_P (C4021 0.1UF 10% 16V X5R 402) — PCIE_FW_D2R_P 7 42 104
42 FW_PHY_DS0	F12 DS0 NAND TREE PIN	REFCLKN	N9 — PCIE_CLK100M_FW_N 7 30 105
42 FW_PHY_DS1	E12 DS1 NAND TREE PIN	REFCLKP	N10 — PCIE_CLK100M_FW_P 7 30 105
42 FW_PHY_DS2	E13 DS2 NAND TREE PIN		

LAYOUT NOTE: PLACE C4020,C4021 CLOSE TO FW643(U4000)

1394 PHY

TEST CONTROLLER

43 FW_P0_TPA_N	B8 TPA0N	NAND TREE PIN TCK	M4 — TP_FW_TCK 7
43 FW_P0_TPA_P	A8 TPA0P	NAND TREE PIN TDI	N2 — TP_FW_TDI 7
43 FW_P1_TPA_N	B5 TPA1N	TDO	M1 — TP_FW_TDO 7
43 FW_P1_TPA_P	A5 TPA1P	NAND TREE PIN TMS	M3 — TP_FW_TMS 7
43 FW_P2_TPA_N	B3 TPA2N	NAND TREE PIN(-04) TRST*	N1 — FW_TRST_L
43 FW_P2_TPA_P	A3 TPA2P		
43 FW_P0_TPB_N	B9 TPB0N		
43 FW_P0_TPB_P	A9 TPB0P		
43 FW_P1_TPB_N	B6 TPB1N		
43 FW_P1_TPB_P	A6 TPB1P		
43 FW_P2_TPB_N	B4 TPB2N		
43 FW_P2_TPB_P	A4 TPB2P		
43 FW_P0_TPBIAS	B7 TPBIAS0	NAND TREE PIN WAKE*	C2 — PCI_PME_FW_L 25
43 FW_P1_TPBIAS	C3 TPBIAS1	FIXME!!! - TYPO IN SYMBOL REGCTL REGCLT	D13 — FW643_REGCTL
43 FW_P2_TPBIAS	A2 TPBIAS2	POWER MANAGEMENT NAND TREE PIN VAUX_DETECT	E1 — FW_VAUX_DETECT
FW_R0	B11 R0	NAND TREE PIN VAUX_DISABLE	D2 — TP_FW_VAUX_DISABLE
FW_TPCPS	B10 TPCPS	CLKREQN	L2 — CK505_CLKREQ3_L 29 30

SCIF

NAND TREE PIN SCIFCLK	G2	TP_FW_SCIFCLK
NAND TREE PIN SCIFDAIN	G1	TP_FW_SCIFDAIN
NAND TREE PIN SCIFDOUT	H1	TP_FW_SCIFDOUT
NAND TREE PIN SCIFMC	F2	TP_FW_SCIFMC

SERIAL EEPROM CONTROLLER

NAND TREE PIN SCL	N12	FW_SCL
NAND TREE PIN SDA	M11	TP_FW_SDA

CHIP RESET

NAND TREE PIN PERST*	N4	FW_RESET_L 7 28

7 TP_FW_NAND_TREE	K1	NAND_TREE	
FW_REXT	L8	REXT	
FW_XO	F13	XO	
FW_XI	G13	XI NAND TREE PIN	
7 TP_FW_SE	M13	SE NAND TREE PIN(NOT IN -04)	
7 TP_FW_SM	N13	SM NAND TREE PIN(NOT IN -04)	
PD INTERNAL TP_FW_MODE_A	J2	MODE_A NAND TREE PIN	
7 TP_FW_CE	L13	CE NAND TREE PIN(-02)	
PU INTERNAL TP_FW_FW620_L	D12	FW620* NAND TREE PIN(-02)	MISCELLANEOUS
TP_FW_JASI_EN	D1	JASI_EN NAND TREE PIN	
TP_FW_AVREG	A10	AVREG	
TP_FW_VBUF	H13	VBUF	
FW_PU_RST_L	K13	FW_RESET* NAND TREE PIN	
42 FW_OCR10_CTL	J12	OCR_CTL_V10	
NC	J13	OCR_CTL_V12	

VSS VREG_VSS

B2 D4 D7 D9 D10 E4 E5 E9 F4 F6 F7 F8 F10 G4 G6 G7 G8 G10 H4 H6 H7 H8 H10 J4 J5 J9 J10 K4 K5 K7 K8 K9 L7 K6 K10 L12

43 FW_PORTS_VP_R

R4001 390K 5% 1/16W MF-LF 402
R4002 2.94K 1% 1/16W MF-LF 402
R4080 191 1% 1/16W MF-LF 402
C4000 22PF 5% 50V CERM 402
C4001 22PF 5% 50V CERM 402
CRITICAL Y4000 24.576M HC49-USMD
R4000 412 1% 1/16W MF-LF 402
LAYOUT NOTE: PLACE Y4000 WITHIN 1.27CM OF XO/XI PINS
C4090 0.33UF 10% 6.3V CERM-X5R 402
R4090 470K 5% 1/16W MF-LF 402

NOSTUFF
R4010 10K 5% 1/16W MF-LF 402
=PP3V3_S5_FW 6 40 42 43
R4013 10K 5% 1/16W MF-LF 402
R4011 10K 5% 1/16W MF-LF 402
R4012 10K 5% 1/16W MF-LF 402

FW: 1394B CONTROLLER

SYNC_DATE=01/08/2008

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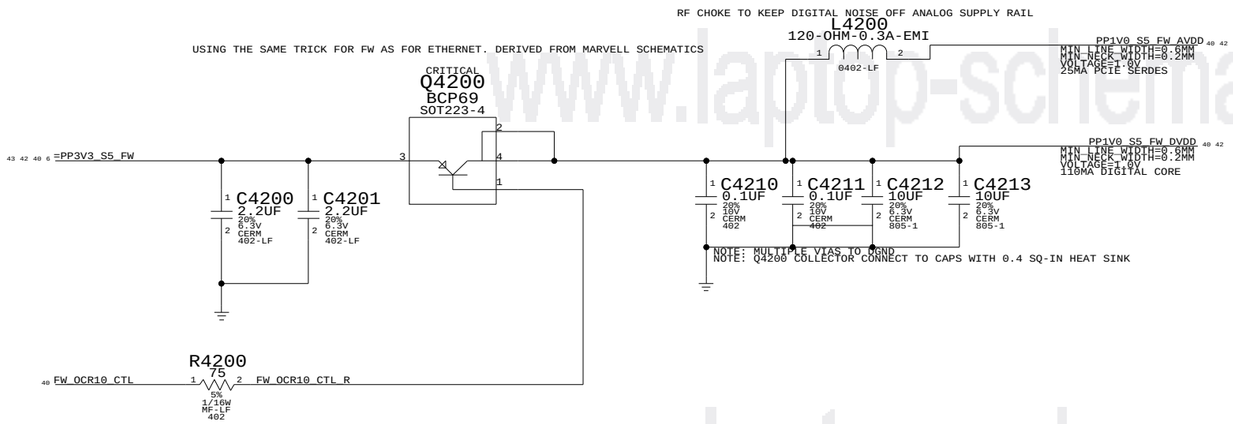
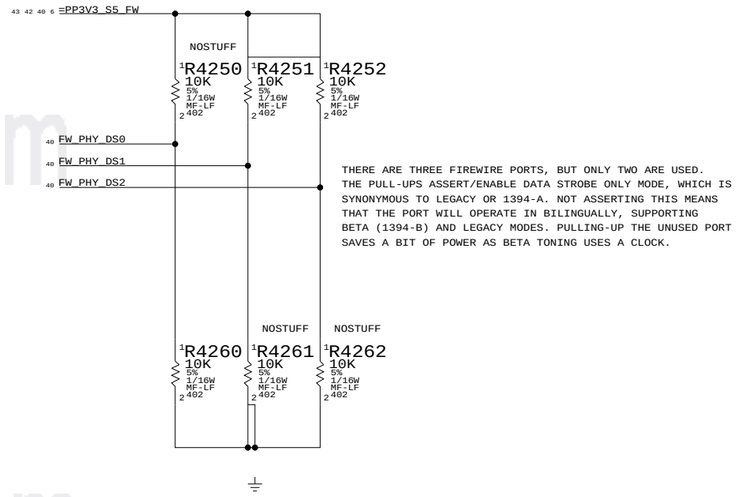
SCALE: NONE	SHT 40 OF 118	

FW643 1.0V GENERATION



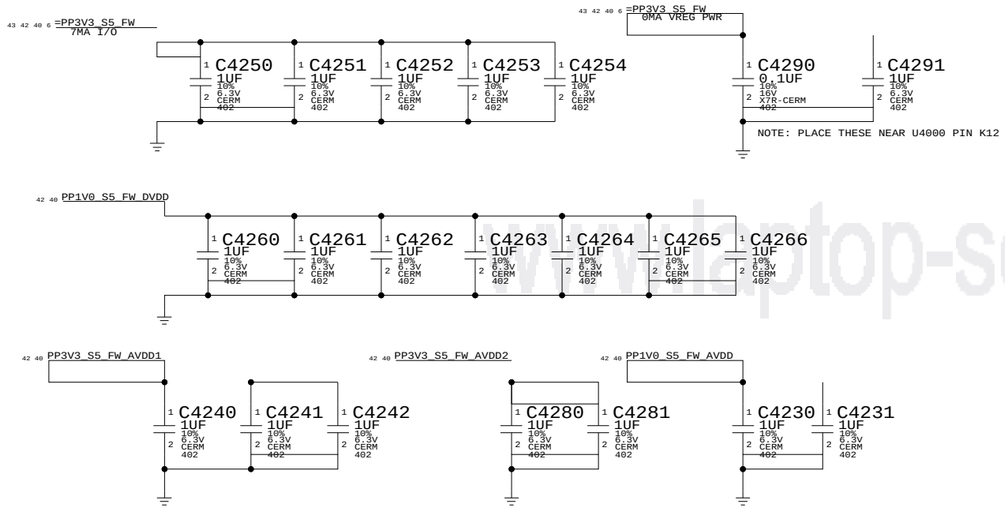
1394 PHY DATA/STROBE OPTIONS



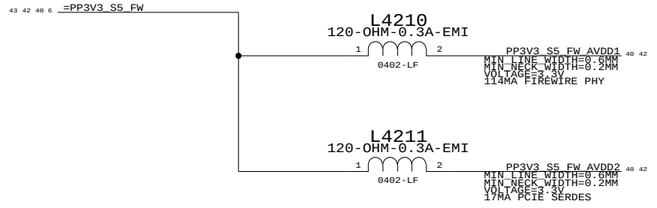
THERE ARE THREE FIREWIRE PORTS, BUT ONLY TWO ARE USED. THE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE, WHICH IS SYNONYMOUS TO LEGACY OR 1394-A. NOT ASSERTING THIS MEANS THAT THE PORT WILL OPERATE IN BILINGUALLY, SUPPORTING BETA (1394-B) AND LEGACY MODES. PULLING-UP THE UNUSED PORT SAVES A BIT OF POWER AS BETA TONING USES A CLOCK.

FW643 DECOUPLING

NOTE: PLACE 1 CAP CLOSE TO EACH POWER PIN ON U4000



FW 3.3V FILTERING



FW PCIE ALIASES

TP_PCIE_FW_R2D_C_N	=	PCIE_FW_R2D_C_N (MAKE_BASE=TRUE)
TP_PCIE_FW_R2D_C_P	=	PCIE_FW_R2D_C_P (MAKE_BASE=TRUE)
PCIE_FW_D2R_N (MAKE_BASE=TRUE)	=	TP_PCIE_FW_D2R_N
PCIE_FW_D2R_P (MAKE_BASE=TRUE)	=	TP_PCIE_FW_D2R_P

FW: 1394B MISC

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SCALE: NONE

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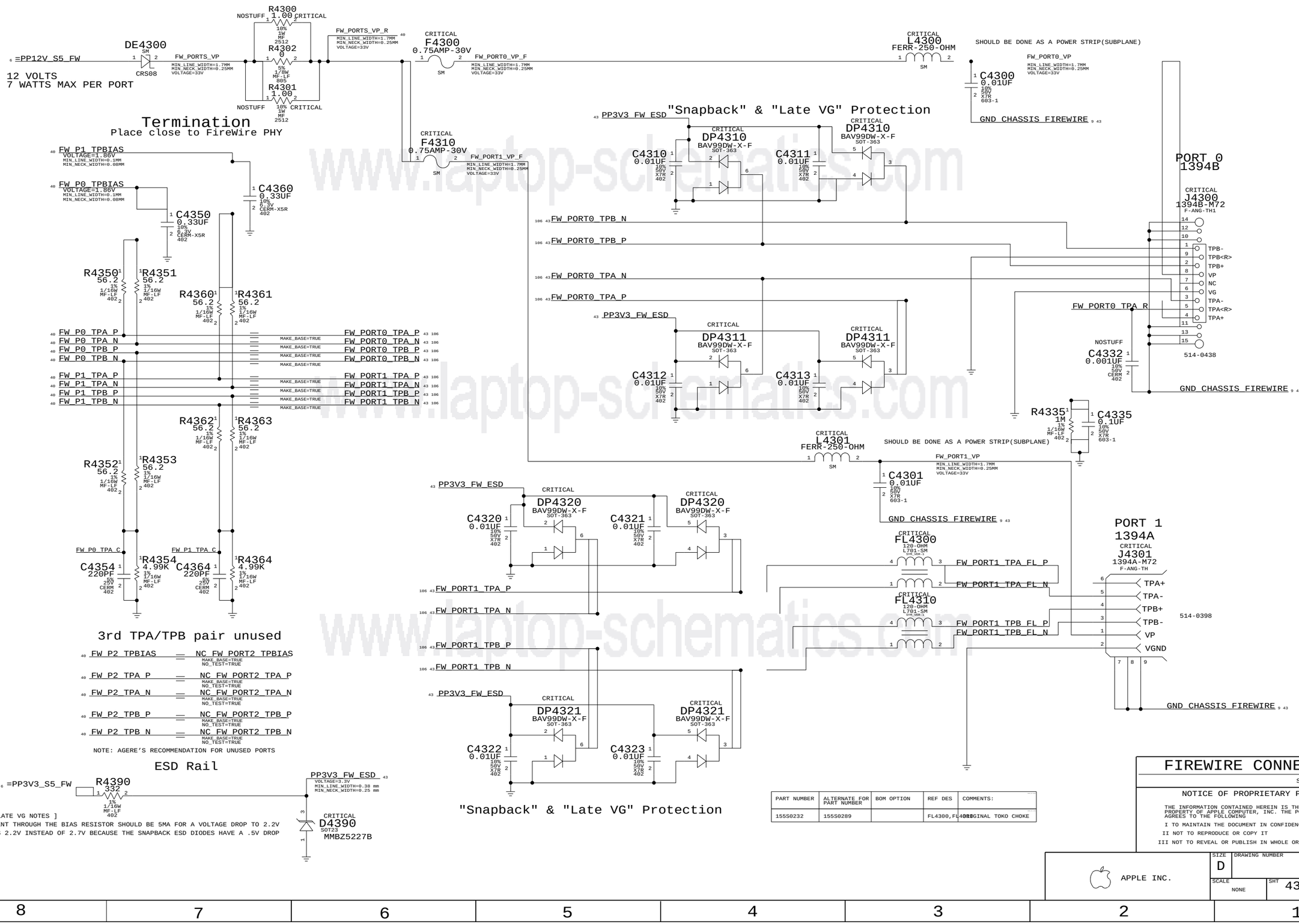

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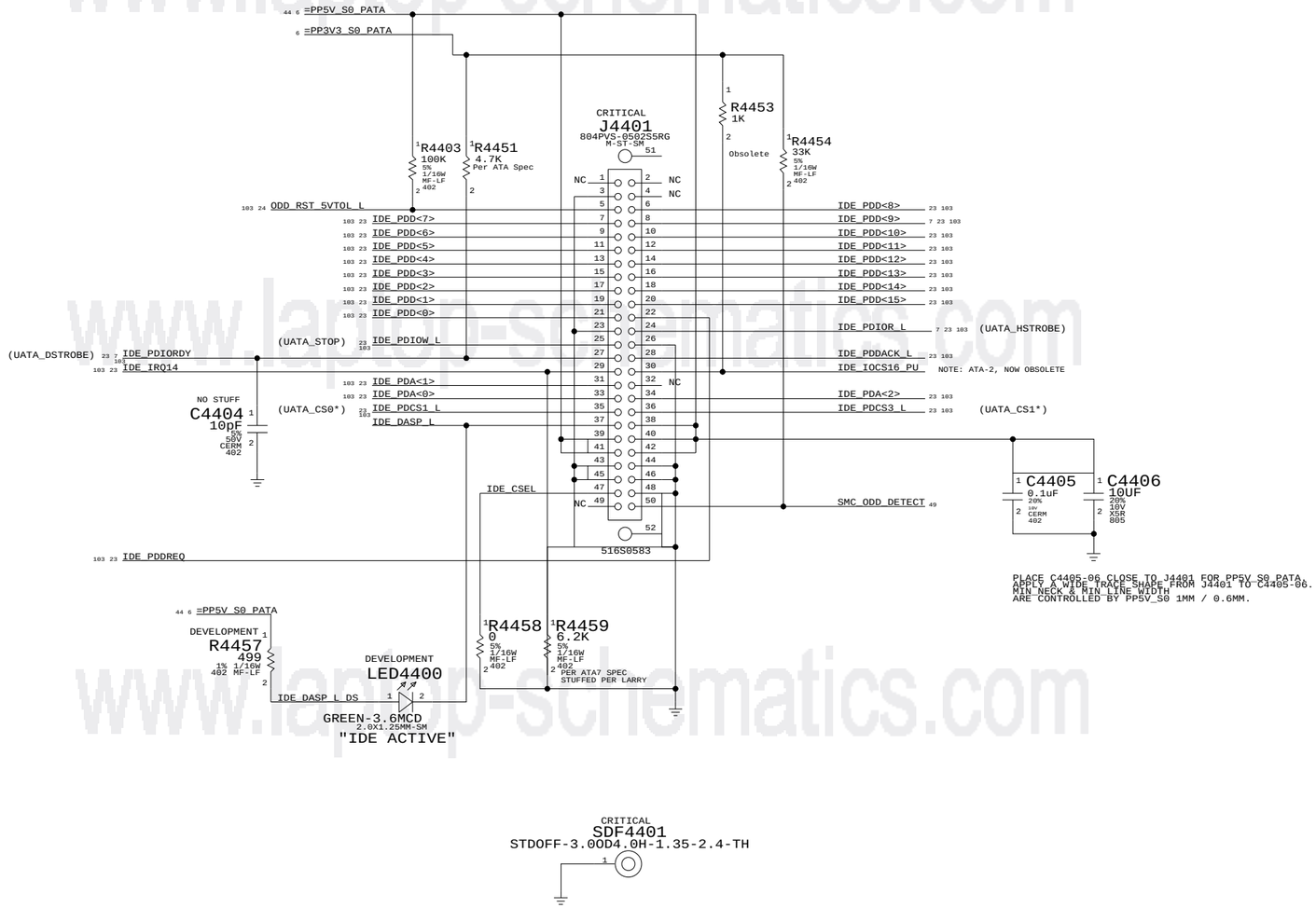
CRITICAL
SDF4400
STDOFF-3.0OD4.0H-1.35-2.4-TH

IDE (ODD) Connector



CRITICAL
SDF4401
STDOFF-3.0OD4.0H-1.35-2.4-TH

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PATA Connector

SYNC_DATE=N/A

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D		A
SCALE: NONE	SHT 44 OF 118	

SATA Port A

CRITICAL
J4510
EP00-081-91
M-ST-SM

518S0251

SATA_A_R2D_P 103
SATA_A_R2D_N 103
SATA_A_D2R_C_N 103
SATA_A_D2R_C_P 103

C4510 0.0047uF 10% 25V CERM 402
SATA_A_R2D_C_P → IN 23 103

C4511 0.0047uF 10% 25V CERM 402
SATA_A_R2D_C_N → IN 23 103

C4515 0.0047uF 10% 25V CERM 402
SATA_A_D2R_N → OUT 7 23 103

C4516 0.0047uF 10% 25V CERM 402
SATA_A_D2R_P → OUT 7 23 103

SATA Activity LED

6 =PP3V3_S0_SATALED

DEVELOPMENT
R4599 1
330
5%
1/10W
MF-LF
603
2

SB_SATALED_R_L

DEVELOPMENT
1
DS4599
GREEN-3.6MCD
2.0X1.25MM-SM
2

SILK_PART=SATA ACTIVE

23 TP_SB_SATALED_L — SB_SATALED_L MAKE_BASE=TRUE

50 49 SMC_EXCARD_OC_L

UNUSED SATA PORTS

TP_SATA_B_R2D_P MAKE_BASE=TRUE — SATA_B_R2D_C_P 23 103
TP_SATA_B_R2D_N MAKE_BASE=TRUE — SATA_B_R2D_C_N 23 103

103 23 SATA_B_D2R_P — TP_SATA_B_D2R_P MAKE_BASE=TRUE
103 23 SATA_B_D2R_N — TP_SATA_B_D2R_N MAKE_BASE=TRUE

TP_SATA_C_R2D_P MAKE_BASE=TRUE — SATA_C_R2D_C_P 23
TP_SATA_C_R2D_N MAKE_BASE=TRUE — SATA_C_R2D_C_N 23

23 SATA_C_D2R_P — TP_SATA_C_D2R_P MAKE_BASE=TRUE
23 SATA_C_D2R_N — TP_SATA_C_D2R_N MAKE_BASE=TRUE

ICH SATA Support

23 SATA_RBIAS_P
23 SATA_RBIAS_N
— 103 SATA_RBIAS MAKE_BASE=TRUE

PLACEMENT_NOTE=Place R4590 within 12.7mm of U2300 pins AG1 & AG2

1 R4590
24.9
1%
1/16W
MF-LF
2 402

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SATA Connectors

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D		A

SCALE NONE

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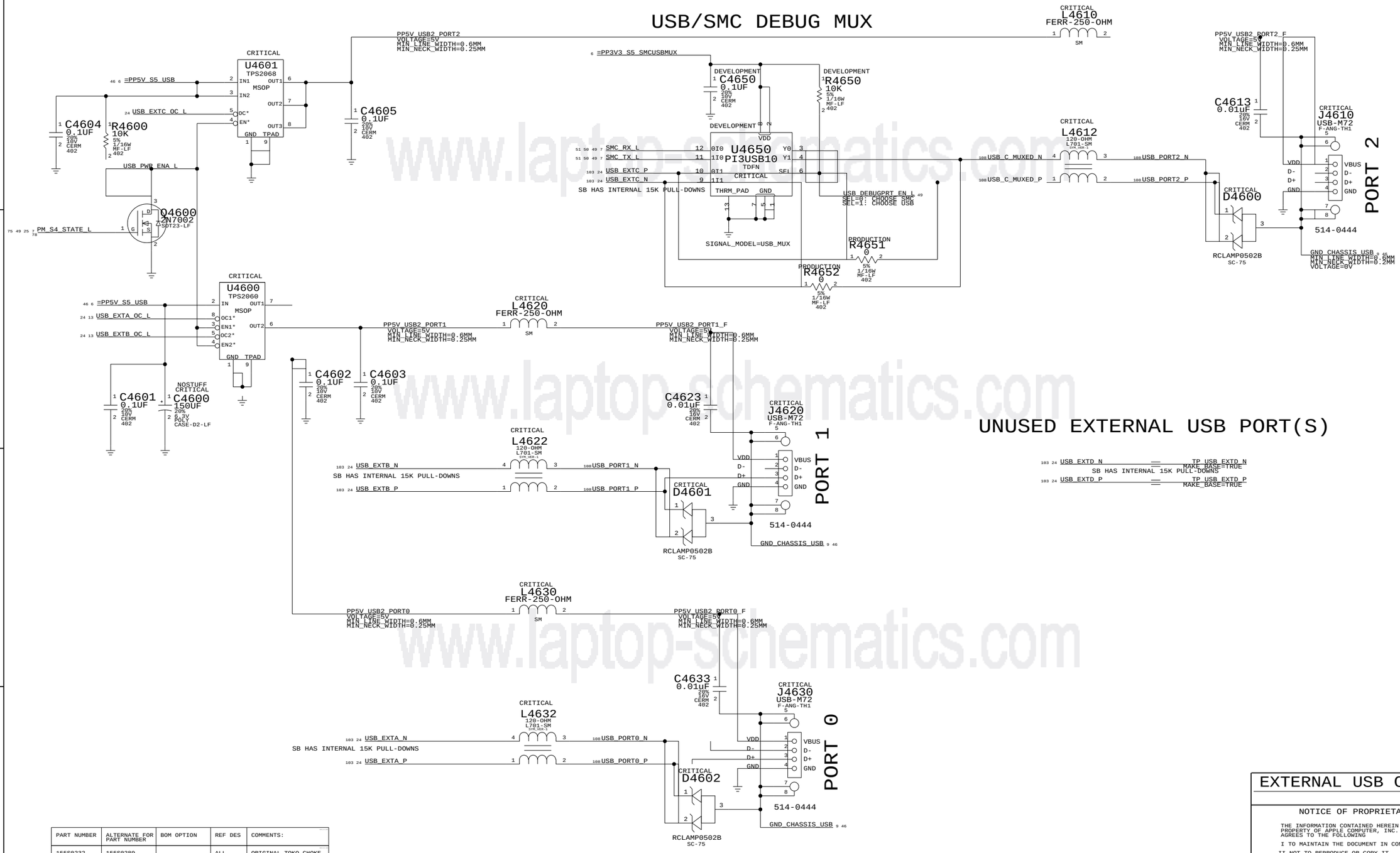
USB/SMC DEBUG MUX



UNUSED EXTERNAL USB PORT(S)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0232	155S0289		ALL	ORIGINAL TOKO CHOKE

EXTERNAL USB CONNECTORS

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D		A
SCALE: NONE	SHT 46 OF 118	

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CAMERA POWER FILTERING

47 6 =PP5V_S3_BNDI

C4700 10UF 20% 6.3V CERM 805-1

CRITICAL
L4700 FERR-250-OHM SM

PP5V_S3_BNDI
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
47

C4701 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C4700, C4701 & L4700
NEAR J4700 PINS 4 AND 5 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.

K37L (BLUETOOTH) CONNECTOR

CRITICAL
J4720 88262-0401 M-ST-SM

SB HAS INTERNAL 15K PULL-DOWNS

103 24 7 USB_BT_N
103 24 7 USB_BT_P
6 =PP3V3_S3_BT

C4720 10UF 20% 6.3V CERM 805-1

C4721 0.1UF 20% 10V CERM 402

CRITICAL
SDF4721 STDOFF-4.00D6.5H-1.35-2.4-TH

SDF4721_1

R4721 0 5% 1/16W MF-LF 402

CAMERA CONNECTOR

R4701 0 402
L4701 CRITICAL 120-OHM L701-SM
R4702 0 402

103 24 7 USB_CAMERA_P
SB HAS INTERNAL 15K PULL-DOWNS
NOSTUFF
103 24 7 USB_CAMERA_N

108 USB_CAMERA_L_P
108 USB_CAMERA_L_N
47 PP5V_S3_BNDI

FIXME!!! - THIS IS REISTECH CHOKE, T9 USES TOKO(155S0232)

R4710 0 402
L4710 CRITICAL 120-OHM L701-SM
R4711 0 402

103 24 7 USB_IR_N
SB HAS INTERNAL 15K PULL-DOWNS
NOSTUFF
103 24 7 USB_IR_P

USB_IR_L_N 47 108
USB_IR_L_P 47 108

CRITICAL
J4700 88262-0501 M-ST-SM

518S0553

47 CHASSIS_GND_BNDI

47 CHASSIS_GND_BNDI — MAKE_BASE=TRUE

UNUSED INTERNAL USB PORTS

103 24 USB_TPAD_N — TP_USB_TPAD_N MAKE_BASE=TRUE
103 24 USB_TPAD_P — TP_USB_TPAD_P MAKE_BASE=TRUE

SB HAS INTERNAL 15K PULL-DOWNS

103 24 USB_EXCARD_N — TP_USB_EXCARD_N MAKE_BASE=TRUE
103 24 USB_EXCARD_P — TP_USB_EXCARD_P MAKE_BASE=TRUE

SB HAS INTERNAL 15K PULL-DOWNS

IR RECEIVER

CRITICAL
J4780 88262-0401 M-ST-SM

108 47 USB_IR_L_N
108 47 USB_IR_L_P
47 6 =PP5V_S3_BNDI

C4781 1UF 10% 6.3V CERM 402

Internal USB Connections

SYNC_DATE=01/08/2008

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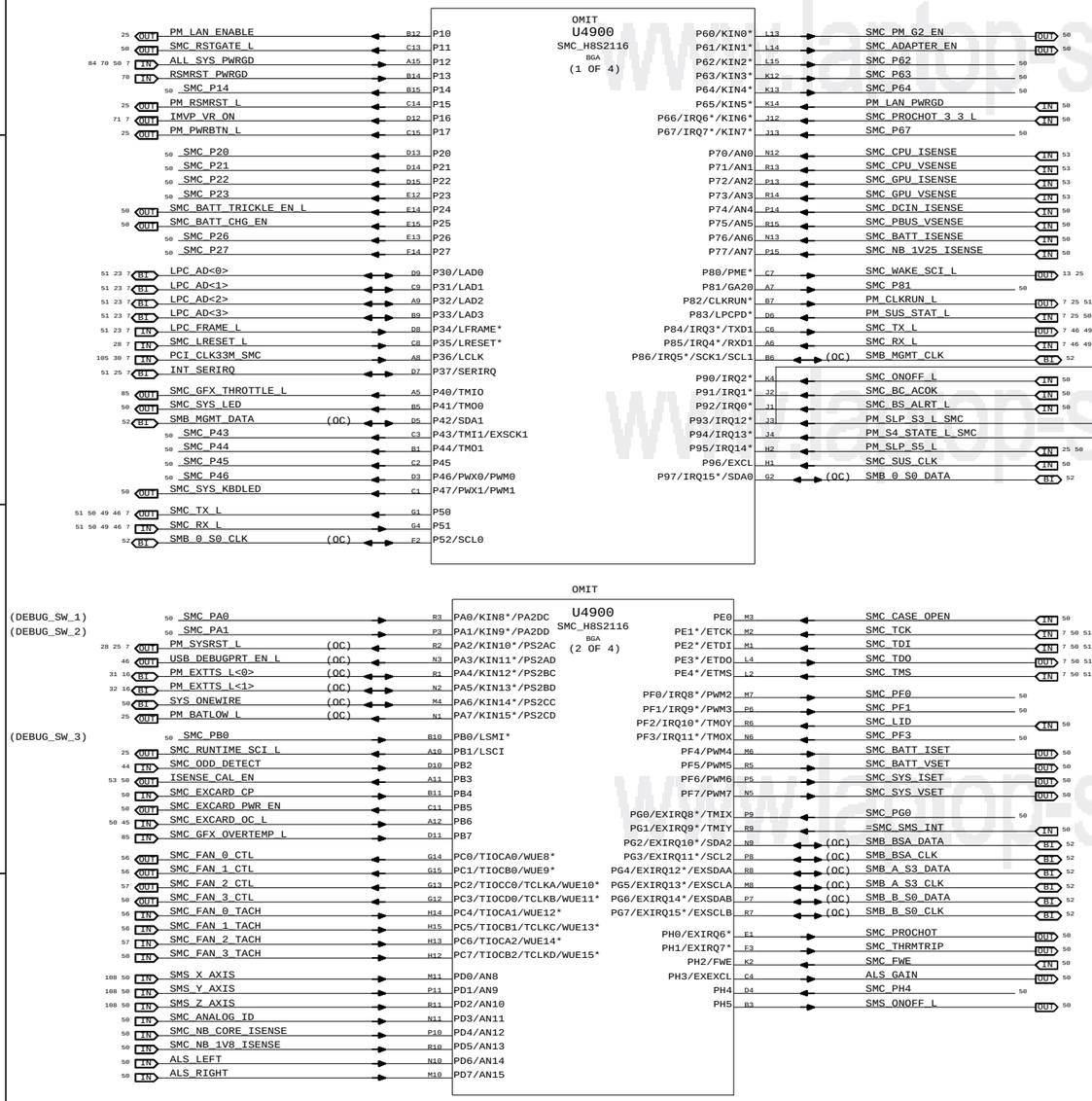
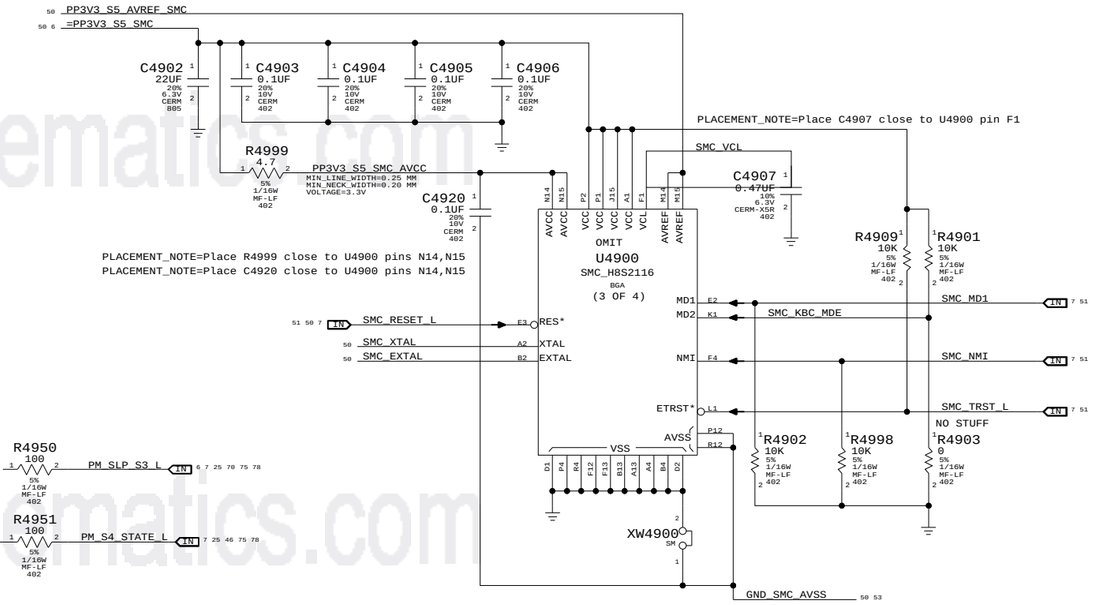
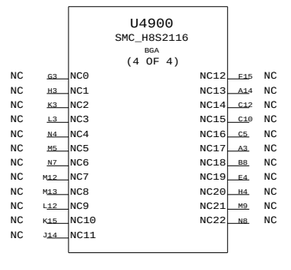
D		A
SCALE: NONE	SHT 47 OF 118	

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.





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SMC

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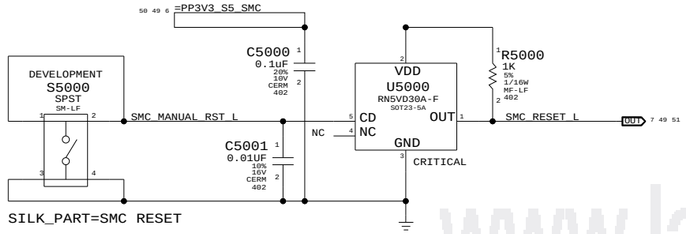
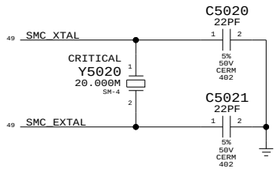
D		A
SCALE: NONE	SHT 49 OF 118	

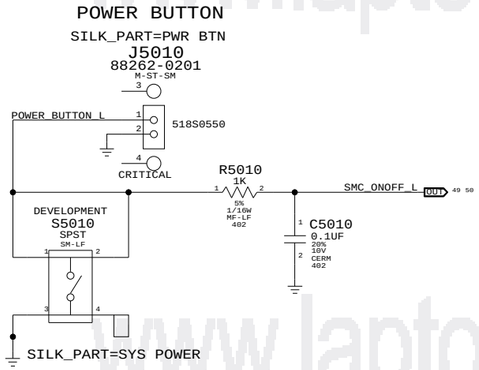
SMC Reset Button / Brownout Detect



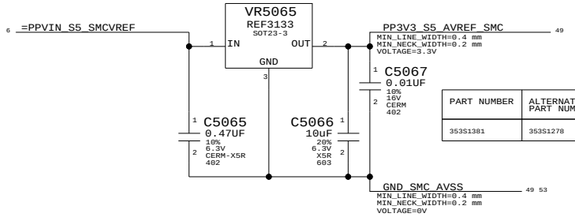
SMC Crystal Circuit



POWER BUTTON



SMC AVREF Supply



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		ALL	Intersil ISL60002-33

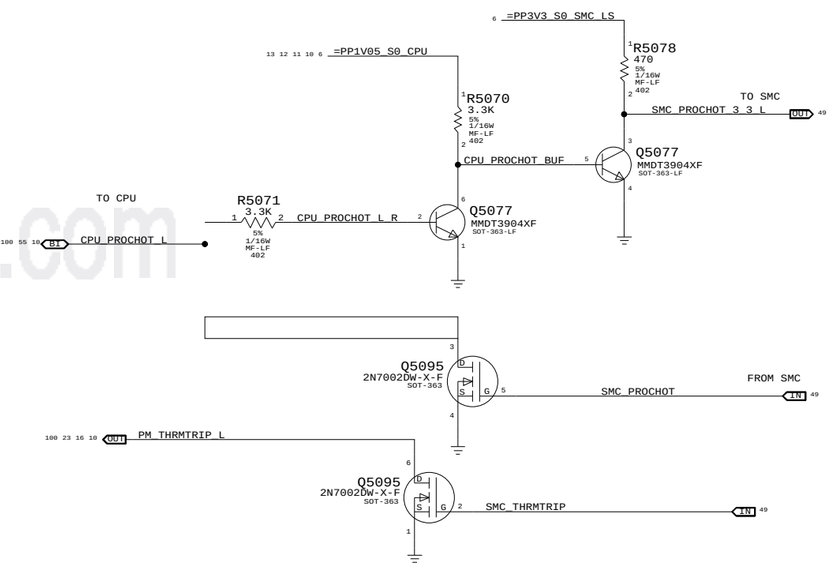
UNUSED TP/NC ALIASES

SMC_BATT_ISET	NC_SMC_BATT_ISET	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_SYS_ISET	NC_SMC_SYS_ISET	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_BATT_VSET	NC_SMC_BATT_VSET	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_SYS_VSET	NC_SMC_SYS_VSET	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_BATT_TRICKLE_EN_L	NC_SMC_BATT_TRICKLE_EN_L	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_BATT_CHG_EN	NC_SMC_BATT_CHG_EN	MAKE_BASE=TRUE	NO_TEST=TRUE
SMS_X_AXIS	NC_SMS_X_AXIS	MAKE_BASE=TRUE	NO_TEST=TRUE
SMS_Y_AXIS	NC_SMS_Y_AXIS	MAKE_BASE=TRUE	NO_TEST=TRUE
SMS_Z_AXIS	NC_SMS_Z_AXIS	MAKE_BASE=TRUE	NO_TEST=TRUE
ALS_GAIN	NC_ALS_GAIN	MAKE_BASE=TRUE	NO_TEST=TRUE
ALS_LEFT	TP_ALS_LEFT	MAKE_BASE=TRUE	
ALS_RIGHT	TP_ALS_RIGHT	MAKE_BASE=TRUE	
SMC_P14	TP_SMC_P14	MAKE_BASE=TRUE	
SMC_P20	TP_SMC_P20	MAKE_BASE=TRUE	
SMC_P21	TP_SMC_P21	MAKE_BASE=TRUE	
SMC_P22	TP_SMC_P22	MAKE_BASE=TRUE	
SMC_P23	TP_SMC_P23	MAKE_BASE=TRUE	
SMC_P26	TP_SMC_P26	MAKE_BASE=TRUE	
SMC_P27	TP_SMC_P27	MAKE_BASE=TRUE	
SMC_P43	TP_SMC_P43	MAKE_BASE=TRUE	
SMC_P44	TP_SMC_P44	MAKE_BASE=TRUE	
SMC_P45	TP_SMC_P45	MAKE_BASE=TRUE	
SMC_P62	TP_SMC_P62	MAKE_BASE=TRUE	
SMC_P63	TP_SMC_P63	MAKE_BASE=TRUE	
SMC_P64	TP_SMC_P64	MAKE_BASE=TRUE	
SMC_P81	TP_SMC_P81	MAKE_BASE=TRUE	
SMC_PF0	TP_SMC_PF0	MAKE_BASE=TRUE	
SMC_PF1	TP_SMC_PF1	MAKE_BASE=TRUE	
SMC_FAN_3_CTL	TP_SMC_FAN_3_CTL	MAKE_BASE=TRUE	
SMC_FAN_3_TACH	TP_SMC_FAN_3_TACH	MAKE_BASE=TRUE	
SMC_PM_G2_EN	TP_SMC_PM_G2_EN	MAKE_BASE=TRUE	
SMC_ADAPTER_EN	TP_SMC_ADAPTER_EN	MAKE_BASE=TRUE	
SMC_SYS_KBDLED	TP_SMC_SYS_KBDLED	MAKE_BASE=TRUE	
SMC_SYS_LED	TP_SMC_SYS_LED	MAKE_BASE=TRUE	
SMC_EXCARD_PWR_EN	TP_SMC_EXCARD_PWR_EN	MAKE_BASE=TRUE	
SMC_RSTGATE_L	TP_SMC_RSTGATE_L	MAKE_BASE=TRUE	
SMS_ONOFF_L	TP_SMS_ONOFF_L	MAKE_BASE=TRUE	
SMC_P46	TP_SMC_P46	MAKE_BASE=TRUE	

ANALOG SENSORS

SMC_NB_1V8_ISENSE	NC_SMC_NB_1V8_ISENSE	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_NB_CORE_ISENSE	NC_SMC_NB_CORE_ISENSE	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_DCIN_ISENSE	SMC_12V_S0_ISENSE	MAKE_BASE=TRUE	53
SMC_PBUS_VSENSE	SMC_12V_S0_VSENSE	MAKE_BASE=TRUE	53
SMC_BATT_ISENSE	SMC_12V_S5_ISENSE	MAKE_BASE=TRUE	53
SMC_NB_1V25_ISENSE	SMC_12V_S5_VSENSE	MAKE_BASE=TRUE	53

SMC FSB to 3.3V Level Shifting



MISC. SIGNAL ALIASES

SMC_ANALOG_ID	ACDC_TEMP	MAKE_BASE=TRUE
SMC_SUS_CLK	SUS_CLK_SB	MAKE_BASE=TRUE
PM_LAN_PWRGD	ALL_SYS_PWRGD	MAKE_BASE=TRUE

=PP3V3_S5_SMC

SMC_ONOFF_L	R5032	10K	5%	1/16W	MF-LF	402	
SMC_LID	R5033	100K	5%	1/16W	MF-LF	402	
SMC_FWE	R5034	10K	5%	1/16W	MF-LF	402	
SMC_TX_L	R5035	10K	5%	1/16W	MF-LF	402	
SMC_RX_L	R5036	100K	5%	1/16W	MF-LF	402	
SYS_ONEWIRE	R5037	2.0K	5%	1/16W	MF-LF	402	
SMC_BS_ALRT_L	R5038	100K	5%	1/16W	MF-LF	402	
SMC_TMS	R5039	10K	5%	1/16W	MF-LF	402	
SMC_TDO	R5040	10K	5%	1/16W	MF-LF	402	
SMC_TDI	R5041	10K	5%	1/16W	MF-LF	402	
SMC_TCK	R5042	10K	5%	1/16W	MF-LF	402	
SMC_EXCARD_OC_L (NO STUFF)	R5043	10K	5%	1/16W	MF-LF	402	
SMC_PF3	R5080	10K	5%	1/16W	MF-LF	402	
SMC_PH4	R5082	10K	5%	1/16W	MF-LF	402	
SMC_BC_ACOK	R5047	10K	5%	1/16W	MF-LF	402	
SMC_PA0	R5096	10K	5%	1/16W	MF-LF	402	
SMC_PA1	R5090	10K	5%	1/16W	MF-LF	402	
SMC_PB0	R5091	10K	5%	1/16W	MF-LF	402	
=SMC_SMS_INT — SMC_SMS_INT	R5092	10K	5%	1/16W	MF-LF	402	
SMC_P67	R5093	10K	5%	1/16W	MF-LF	402	
SMC_PG0	R5094	10K	5%	1/16W	MF-LF	402	
SMC_CASE_OPEN	R5046	10K	5%	1/16W	MF-LF	402	
SMC_EXCARD_CP	R5048	10K	5%	1/16W	MF-LF	402	
PM_SUS_STAT_L	R5083	100K	5%	1/16W	MF-LF	402	
PM_SLP_S5_L	R5084	100K	5%	1/16W	MF-LF	402	
ISENSE_CAL_EN (NO STUFF)	R5088	100K	5%	1/16W	MF-LF	402	

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SMC Support

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D		A
SCALE: NONE	SHT 50 OF 118	

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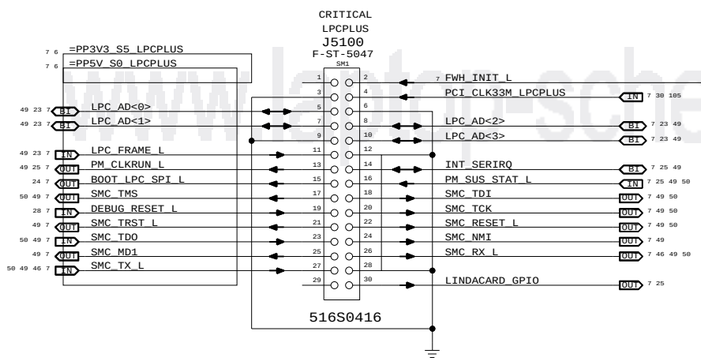
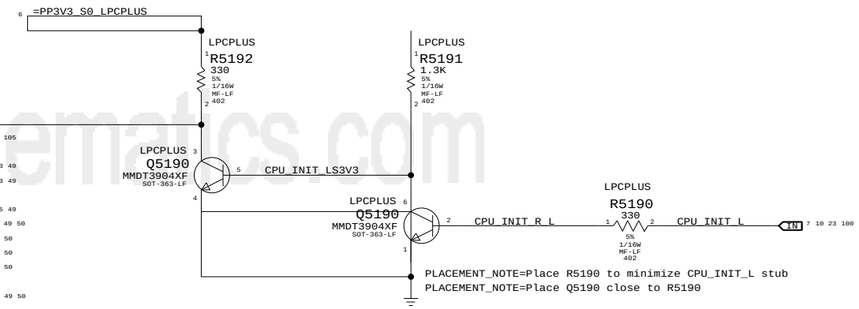
LPC+ Connector



FWH_INIT_L Generation



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LPC+ Debug Connector

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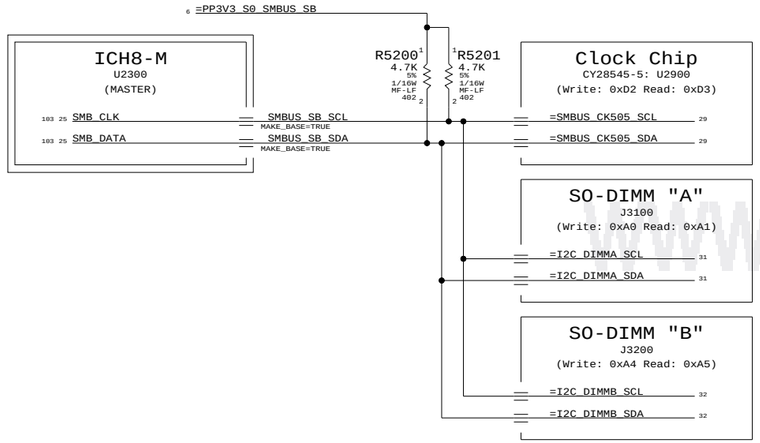
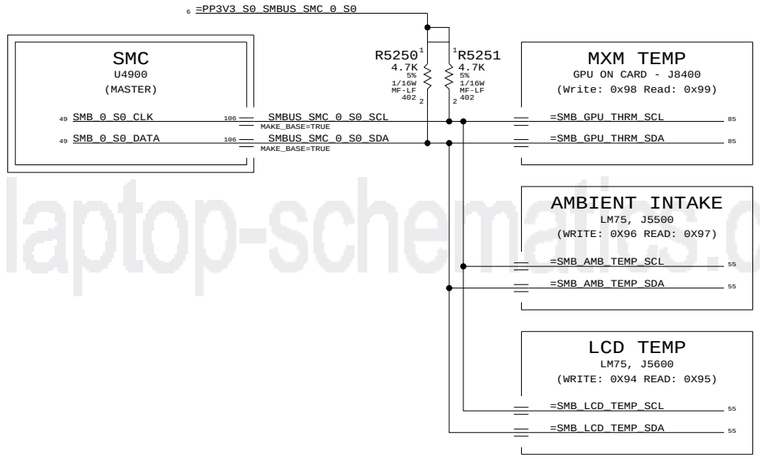
D		A

SCALE	SHT	OF
NONE	51	118

ICH8-M SMBus Connections

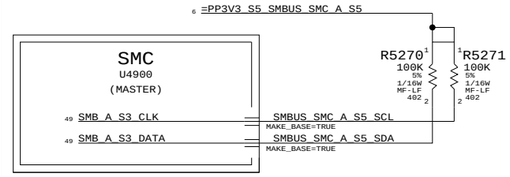


SMC "0" SMBus Connections

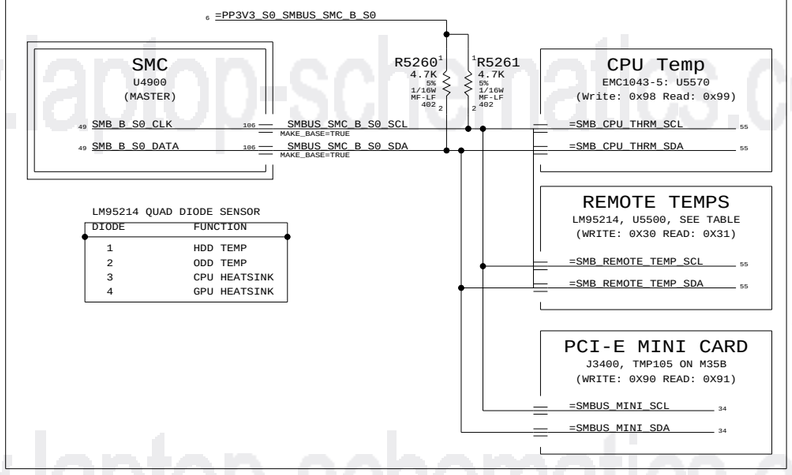


SMC "A" SMBus Connections

NOTE: SMC RMT BUS REMAINS POWERED AND MAY BE ACTIVE IN S5 STATE



SMC "B" SMBus Connections

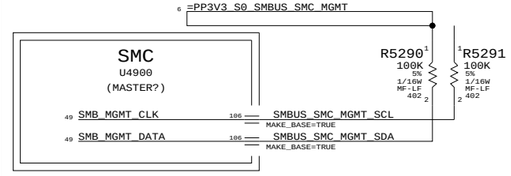


LM95214 QUAD DIODE SENSOR

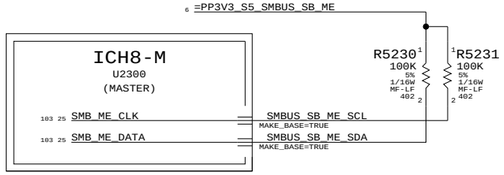
DIODE	FUNCTION
1	HDD TEMP
2	ODD TEMP
3	CPU HEATSINK
4	GPU HEATSINK

UNUSED SMC "BATTERY A" SMBUS CONNECTIONS

UNUSED SMC "MANAGEMENT" SMBUS CONNECTIONS



UNUSED ICH8-M ME SMBUS CONNECTIONS



SMBUS CONNECTIONS

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D		A

SCALE	SHT	OF
NONE	52	118

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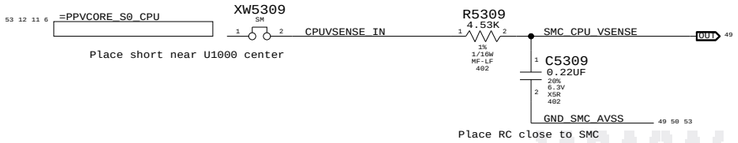
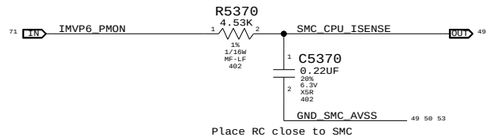
CPU POWER SENSE CALIBRATION CIRCUIT

Switches in fixed load on power supplies to calibrate current sense circuits

CPU Voltage Sense / Filter



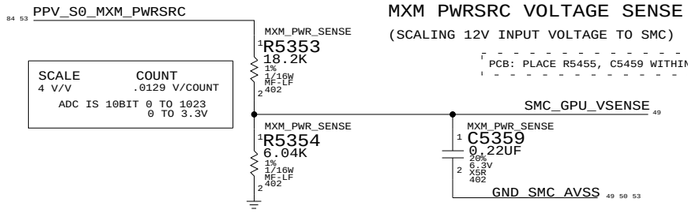
CPU SUPPLY POWER SENSE FILTER



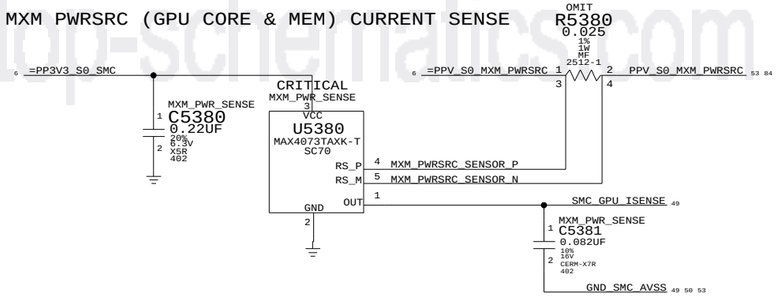
PCPU = VPMON / (17.5 * .0021)

MXM PWRSRC VOLTAGE SENSE

(SCALING 12V INPUT VOLTAGE TO SMC)



MXM PWRSRC (GPU CORE & MEM) CURRENT SENSE



K2 SET FOR APPROX 2V AT 4A ON PWRSRC

SCALE	COUNT
2 A/V	.0064453 A/COUNT

ADC IS 10BIT 0 TO 1023
0 TO 3.3V

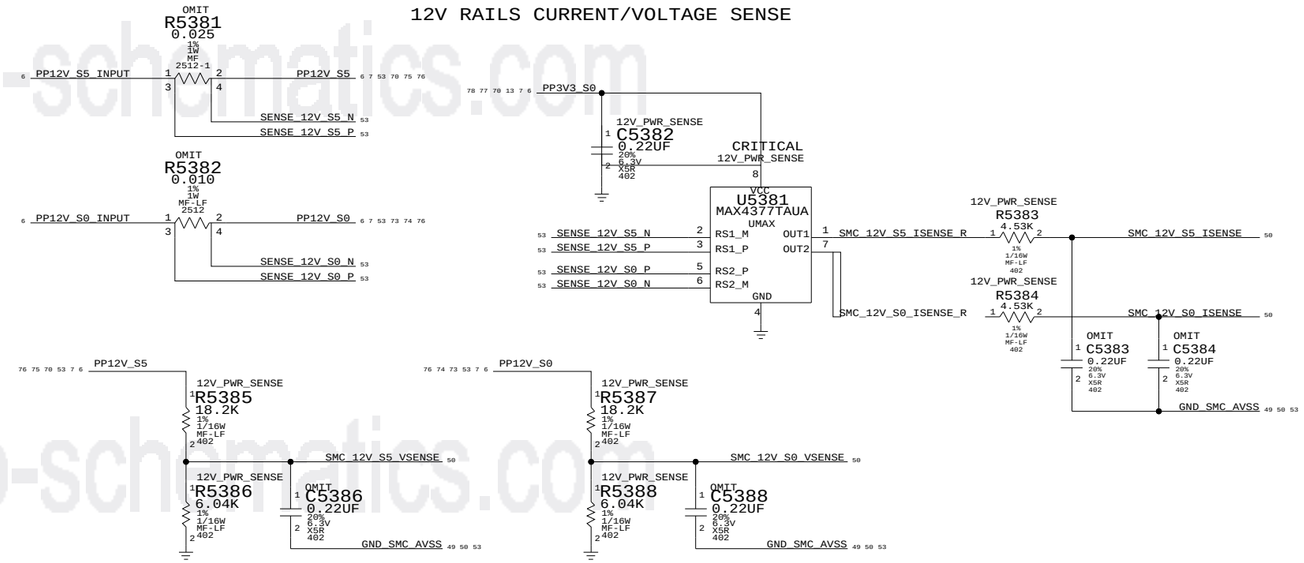
K3 SET FOR APPROX 1.98V AT 5.5A ON PWRSRC

SCALE	COUNT
2.778 A/V	.0087518 A/COUNT

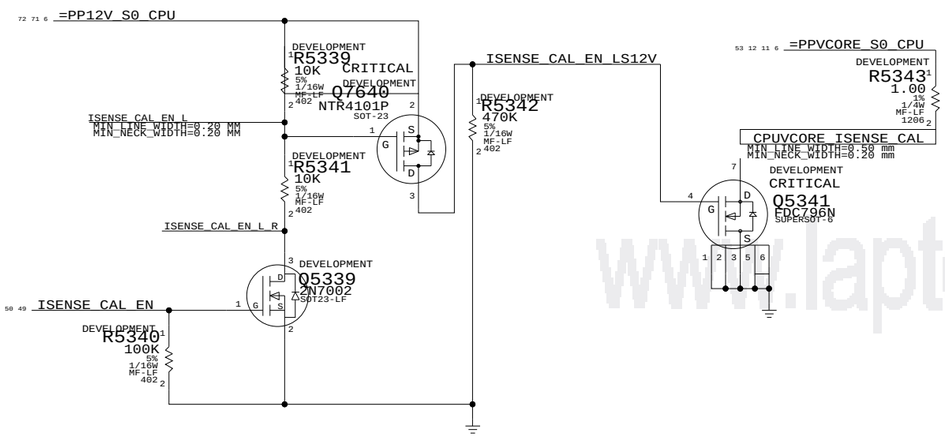
ADC IS 10BIT 0 TO 1023
0 TO 3.3V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
107S0063	1	25 MILLIOHM	R5380	CRITICAL	20_INCH_LCD
107S0111	1	18 MILLIOHM	R5380	CRITICAL	24_INCH_LCD

12V RAILS CURRENT/VOLTAGE SENSE



CPU Power Sense Calibration Circuit



12V_PWR_SENSE SHOULD BE STUFFED FOR K2 BETTER AND K3 (BEST/CTO)
K2 GOOD WILL NOT HAVE THE SENSORS, SO CAPS FROM THE RC FILTER BECOME RESISTORS TO GROUND (SO SMC READS 0)

K2 GOOD DOES NOT NEED 12V POWER SENSE BECAUSE THE CONFIGURATION DOES NOT DRAW CURRENT WHICH APPROACHES THE ACDC SPEC

Current & Voltage Sensing

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D		A
SCALE: NONE	SHT 53 OF 118	

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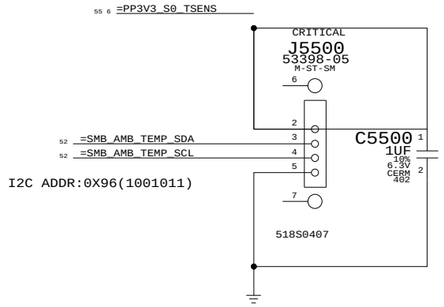
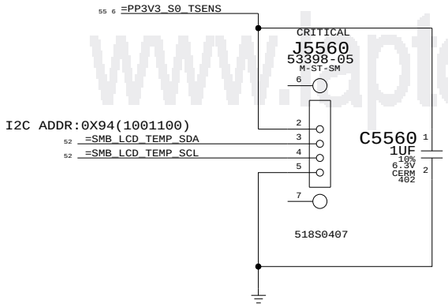
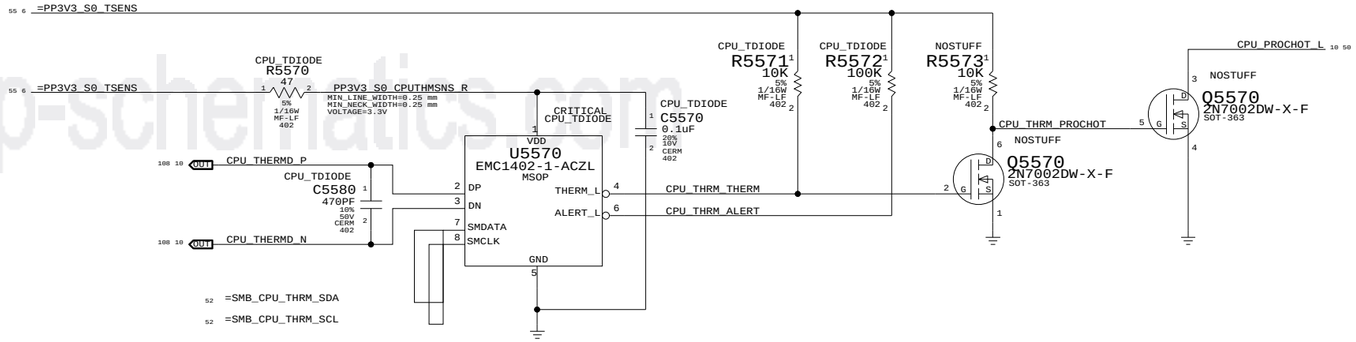
AMBIENT TEMP SENSOR



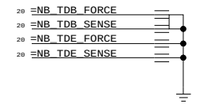
LCD TEMP SENSOR



CPU T-Diode Thermal Sensor



UNUSED NB THERMAL SENSORS

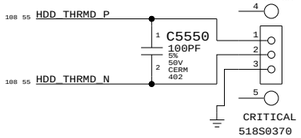


REMOTE THERMAL SENSORS (HEATSINKS AND DISKS)

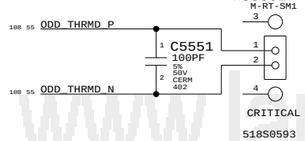
PLACE ALL CAPS NEAR U5500

PLACE DISK SENSOR CONNS BOTTOM SIDE

SILK_PART=HDD TEMP

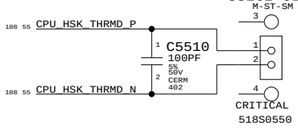


SILK_PART=ODD TEMP

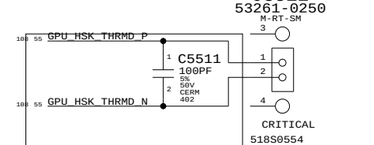


PLACE HSK SENSOR CONN. TOP SIDE NEAR GPU OR CPU

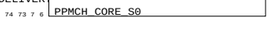
SILK_PART=CPU HSK

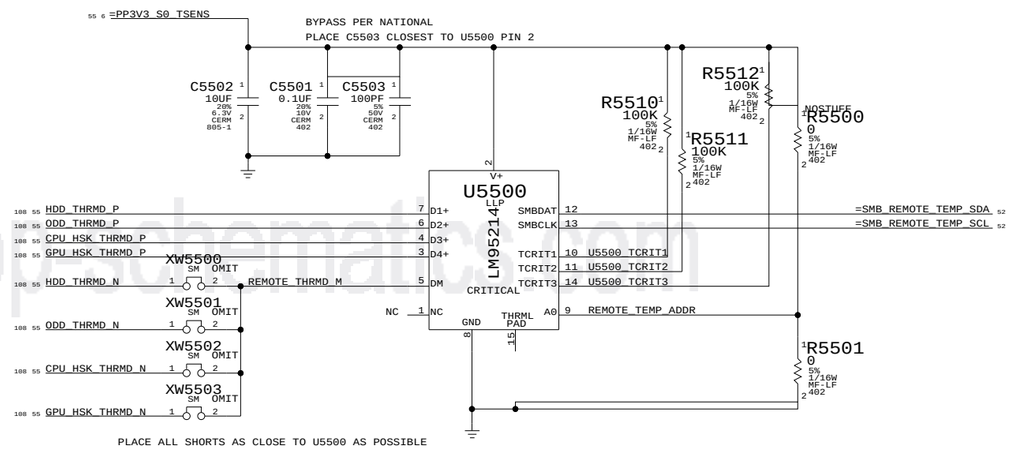


SILK_PART=GPU HSK



TO HELP POWER DELIVERY





PLACE ALL SHORTS AS CLOSE TO U5500 AS POSSIBLE
ROUTE DIODE SIGNALS AS DIFF PAIRS

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Thermal Sensors

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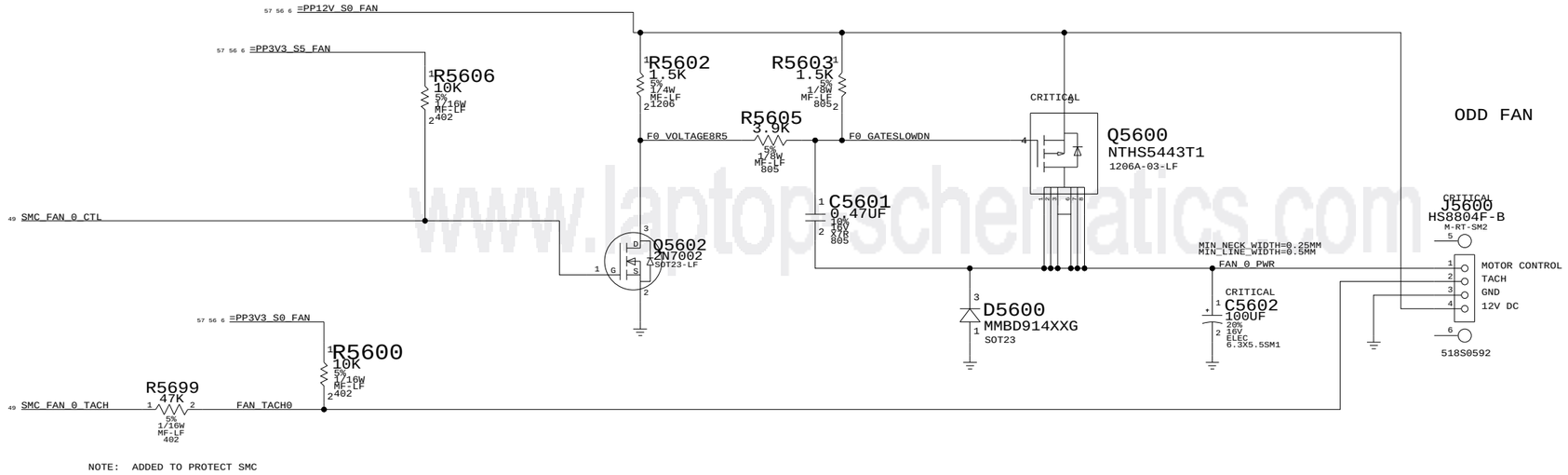
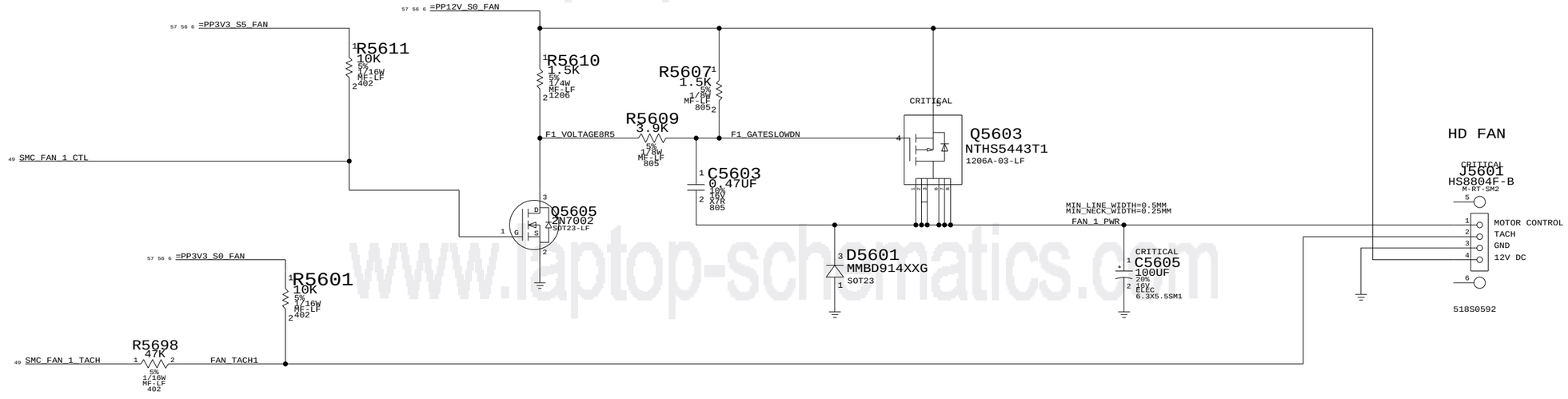
D		A
SCALE: NONE	SHT 55 OF 118	

FAN 0



NOTE: ADDED TO PROTECT SMC

FAN 1



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HD AND OD FAN

SYNC_DATE=N/A

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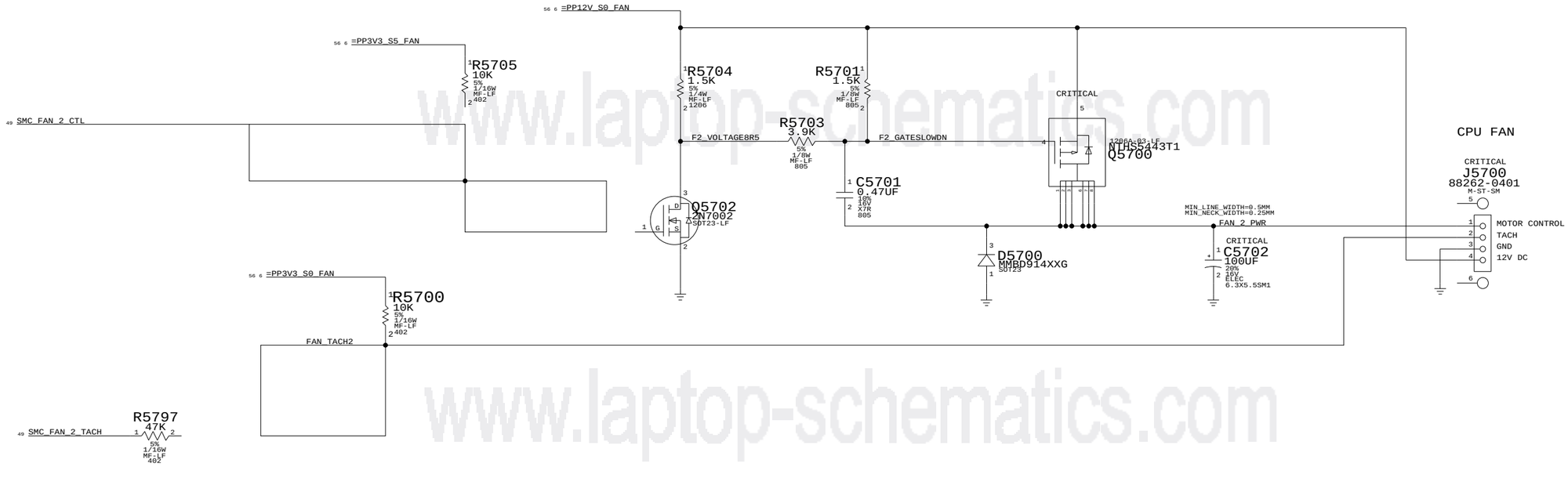
D		A

SCALE	SHT	OF
NONE	56	118

FAN 2



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CPU FAN

SYNC_DATE=01/08/2008

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D		A

SCALE	SHT	OF
NONE	57	118

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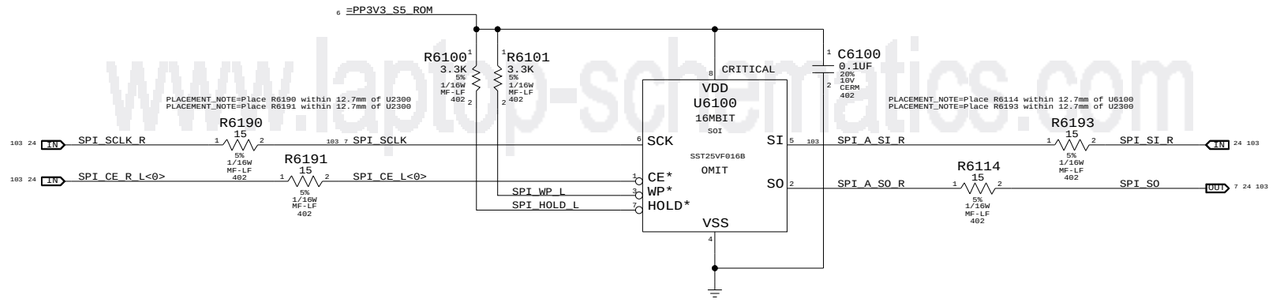

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SPI BootROM

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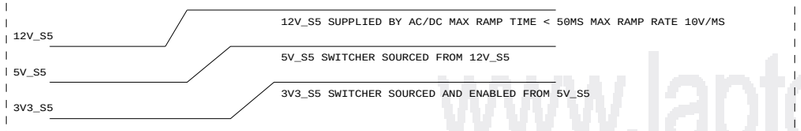
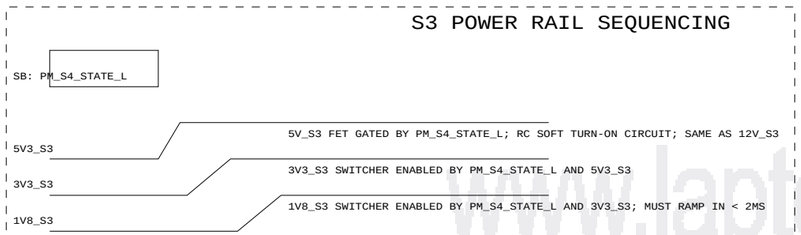
SCALE	SHT	OF
NONE	61	118

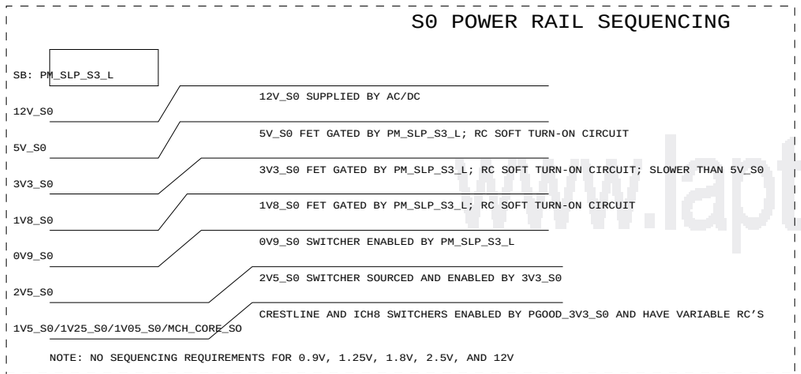
S5 POWER RAIL SEQUENCING



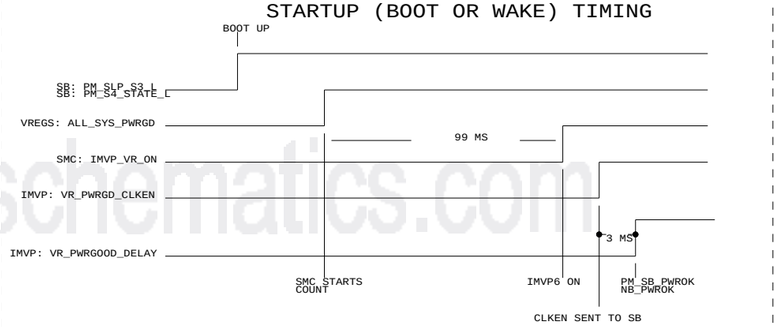
S3 POWER RAIL SEQUENCING



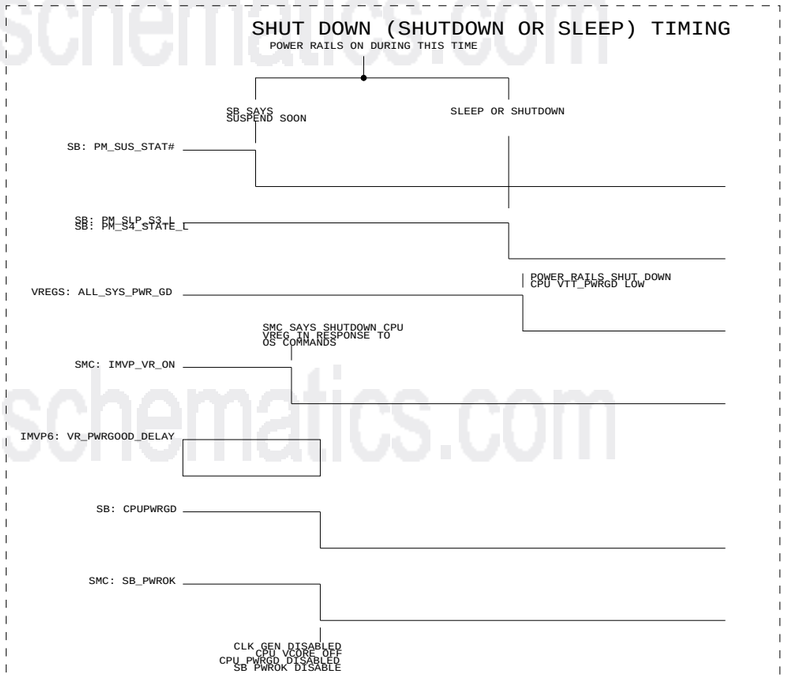
S0 POWER RAIL SEQUENCING



STARTUP (BOOT OR WAKE) TIMING



SHUT DOWN (SHUTDOWN OR SLEEP) TIMING



POWER SEQUENCING BLOCK DIAGRAM

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NONE	69	118

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PGOOD Comparators

PP12V_S5 (76 75 53 7 6)
PP5V_S5 (78 77 76 70 7 6)
PP3V3_S0 (78 77 70 53 13 7 6)
PP1V8_S0 (78 7 6)
PP5V_S0 (94 78 74 73 72 71 7 6)
PP0V9_S0 (75 7 6)

C7010 0.1UF 20% 16V CERM 603

R7010 2.21K 1% 1/16W MF-LF 402
R7013 7.5K 1% 1/16W MF-LF 402
R7018 5.62K 1% 1/16W MF-LF 402
R7020 1.62K 1% 1/16W MF-LF 402
R7000 2.74K 1% 1/16W MF-LF 402
R7001 1.43K 1% 1/16W MF-LF 402
R7002 3.92K 1% 1/16W MF-LF 402
R7003 715 1% 1/16W MF-LF 402
R7011 1K 1% 1/16W MF-LF 402
R7014 10K 1% 1/16W MF-LF 402
R7019 1K 1% 1/16W MF-LF 402
R7021 10K 1% 1/16W MF-LF 402

CRITICAL
U7010 LM339A SOI-LF
V+ GND

(2.94V/2.61V; 330MV HYSTERESIS)
(1.58V/1.41V; 172MV HYSTERESIS)
(4.47V/4.00V; 470MV HYSTERESIS)
(0.76V/0.67V; 85MV HYSTERESIS)

-1 +1 5VS5_2V80_REF
-2 +2 3V3S0_COMP_REF
-3 +3 5VS5_1V53_REF
-4 +4 1V8S0_COMP_REF
5VS5_4V24_REF1
5VS0_COMP_REF
5VS5_0V76_REF
0V9S0_COMP_REF

OUT1 PGOOD_3V3_S0 (OUT 70)
OUT2 PGOOD_1V8_S0 (OUT 70)
OUT3 PGOOD_5V_S0 (OUT 70)
OUT4 PGOOD_0V9_S0 (OUT 70)

R7005 100K 1% 1/16W MF-LF 402
R7006 100K 1% 1/16W MF-LF 402
R7007 100K 1% 1/16W MF-LF 402
R7008 100K 1% 1/16W MF-LF 402

NOSTUFF C7000 0.1UF 20% 10V CERM 402
NOSTUFF C7001 0.1UF 20% 10V CERM 402
NOSTUFF C7002 0.1UF 20% 10V CERM 402
NOSTUFF C7003 0.1UF 20% 10V CERM 402

(PULLUPS ARE NEAR LOADS)

(HYSTERESIS)
(R7000: 2.74K; R7001: 17.4K; R7002: 24.9K; R7003: 8.25K) (200MV; 150MV; 300MV; 100MV HYSTERESIS)
(R7010: 21.5K; R7013: 7.15K; R7018: 52.3K; R7020: 1.37K) (200MV; 150MV; 300MV; 100MV HYSTERESIS)

1.05V/MCH_CORE S0 RUN/SS CONTROL

PP3V3_S5 (77 75 70 7 6)
PGOOD_3V3_S0 (IN 78)
PGOOD_12V_S0 (IN 76)
PGOOD_CR_S0
RUNSS_GATE_D_L (70)

R7070 5.1K 5% 1/16W MF-LF 402
R7040 0 5% 1/16W MF-LF 402
R7041 0 5% 1/16W MF-LF 402
R7065 100K 5% 1/16W MF-LF 402
R7066 330 5% 1/16W MF-LF 402

1V05S0_RUNSS_BUF
1V05S0_RUNSS (OUT 73 74)

Q7007 SSM6N15FE SOT563
C7062 0.01UF 10% 16V CERM 402

1.25V S0 RUN/SS CONTROL

R7063 51K 5% 1/16W MF-LF 402
R7064 680 5% 1/16W MF-LF 402

1V25S0_RUNSS_BUF
1V25S0_RUNSS (OUT 74)

Q7006 SSM6N15FE SOT563
RUNSS_GATE_D_L (70)
C7061 0.01UF 10% 16V CERM 402

1.5V S0 RUN/SS CONTROL

R7061 10K 5% 1/16W MF-LF 402
R7062 1K 5% 1/16W MF-LF 402

1V5S0_RUNSS_BUF
1V5S0_RUNSS (OUT 73)

PP5V_S5 (78 77 76 70 7 6)
R7060 470K 5% 1/16W MF-LF 402
CRITICAL Q7007 SSM6N15FE SOT563
RUNSS_GATE_D_L (70)
C7060 0.01UF 10% 16V CERM 402

CRITICAL Q7006 SSM6N15FE SOT563
PM_SLP_S3_L (IN 78 75 49 25 7 6)

(SUPPLY CHANGED FOR ROUTING)

PP5V_S3 (78 76 75 7 6)
PP3V3_S3 (78 76 75 7 6)
(REMOVE AFTER DEVELOPMENT, MAKE INTO TP)

PGOOD_1V8_S3 (IN 75)
PGOOD_3V3_S3 (IN 76)

R7080 100K 5% 1/16W MF-LF 402
R7081 100K 5% 1/16W MF-LF 402

PWROK Sequencing

PP3V3_S0 (78 77 70 53 13 7 6)
PP3V3_S5 (77 75 70 7 6)

R7034 5.1K 5% 1/16W MF-LF 402

C7052 0.1UF 20% 10V CERM 402
C7056 0.1UF 20% 10V CERM 402

(MC74VHC1G08 HAS 100NS/V MAX SLEW RATE)
(10PF MAX CIN)

PGOOD_0V9_S0 (IN 70)
PGOOD_5V_S0 (IN 70)
PGOOD_1V8_S0 (IN 70)

R7030 100 5% 1/16W MF-LF 402
R7031 100 5% 1/16W MF-LF 402
R7032 100 5% 1/16W MF-LF 402

PGOOD_S0_OUT1

U7052 MC74VHC1G08 SOT23-5-LF
ALL_SYS_PWRGD (OUT 7 49 50 84)

U7056 MC74VHC1G08 SOT23-5-LF
VR_PWRGOOD_DELAY (IN 71 22 16 7)
PM_SB_PWROK (OUT 7 25 28)

(NOT ALL PGOODS ARE NEEDED HERE SINCE
(SOME REGULATORS ARE DAISY CHAIN ENABLED)

PP3V3_S0 (78 77 70 53 13 7 6)

R7039 5.1K 5% 1/16W MF-LF 402

PGOOD_MCH_CORE_S0 (IN 74)
PGOOD_1V05_S0 (IN 73)
PGOOD_1V25_S0 (IN 74)
PGOOD_1V5_S0 (IN 73)

R7035 100 5% 1/16W MF-LF 402
R7036 100 5% 1/16W MF-LF 402
R7037 100 5% 1/16W MF-LF 402
R7038 100 5% 1/16W MF-LF 402

CR_E
IMVP_PGD_IN

PP3V3_S5 (77 75 70 7 6)

R7092 10K 5% 1/16W MF-LF 402

(3.3V WILL NOT BE UP UNTIL 5V IS IN REGULATION)
(SMC CAN HANDLE SLOW RISE TIME OF RSMRST_PWRGD)

PGOOD_3V3_S5 (IN 77)
RSMRST_PWRGD MAKE_BASE=TRUE (OUT 49)

NOSTUFF C7090 220PF 5% 25V CERM 402

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PGOOD and Power Sequencing

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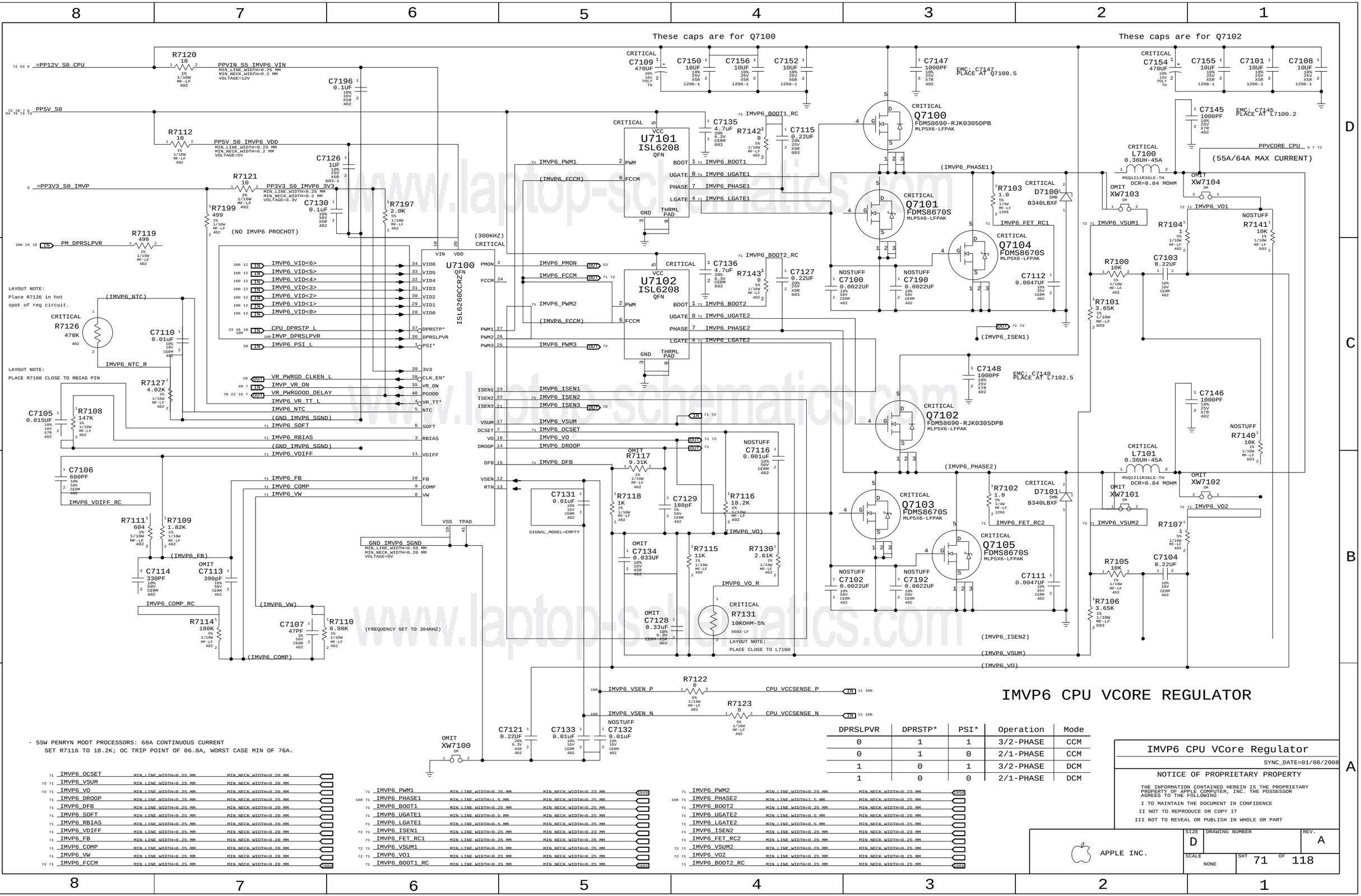
D		A
SCALE: NONE	SHT 70 OF 118	


These caps are for Q7100
These caps are for Q7102
U7100 ISL6260CCR2
U7101 ISL6208
U7102 ISL6208
Q7100 FDMS8690-RJK0305DPB
Q7101 FDMS8670S
Q7102 FDMS8690-RJK0305DPB
Q7103 FDMS8670S
Q7104 FDMS8670S
Q7105 FDMS8670S
D7100L B340LBXF
D7101L B340LBXF
L7100 0.36UH-45A
L7101 0.36UH-45A
=PP12V_S0_CPU
PP5V_S0
=PP3V3_S0_IMVP
PM_DPRSLPVR
PPVIN_S5_IMVP6_VIN
PP5V_S0_IMVP6_VDD
PP3V3_S0_IMVP6_3V3
(NO IMVP6 PROCHOT)
(300KHZ)
(FREQUENCY SET TO 304KHZ)
SIGNAL_MODEL=EMPTY
GND_IMVP6_SGND
PPVCORE_CPU
(55A/64A MAX CURRENT)
IMVP6_VID<6>
IMVP6_VID<5>
IMVP6_VID<4>
IMVP6_VID<3>
IMVP6_VID<2>
IMVP6_VID<1>
IMVP6_VID<0>
CPU_DPRSTP_L
IMVP_DPRSLPVR
IMVP6_PSI_L
VR_PWRGD_CLKEN_L
IMVP_VR_ON
VR_PWRGOOD_DELAY
IMVP6_VR_TT_L
IMVP6_PMON
IMVP6_FCCM
IMVP6_PWM1
IMVP6_PWM2
IMVP6_PWM3
IMVP6_ISEN1
IMVP6_ISEN2
IMVP6_ISEN3
IMVP6_VSUM
IMVP6_OCSET
IMVP6_VO
IMVP6_DROOP
IMVP6_DFB
IMVP6_FB
IMVP6_COMP
IMVP6_VW
IMVP6_VDIFF
IMVP6_SOFT
IMVP6_RBIAS
IMVP6_NTC
IMVP6_BOOT1_RC
IMVP6_BOOT2_RC
IMVP6_UGATE1
IMVP6_UGATE2
IMVP6_PHASE1
IMVP6_PHASE2
IMVP6_LGATE1
IMVP6_LGATE2
IMVP6_FET_RC1
IMVP6_FET_RC2
IMVP6_VO_R
IMVP6_VSEN_P
IMVP6_VSEN_N
CPU_VCCSENSE_P
CPU_VCCSENSE_N
IMVP6_VO1
IMVP6_VO2
IMVP6_VSUM1
IMVP6_VSUM2
(IMVP6_ISEN1)
(IMVP6_ISEN2)
(IMVP6_VSUM)
(IMVP6_VO)
(IMVP6_NTC)
(IMVP6_FB)
(IMVP6_VW)
(IMVP6_COMP)
(IMVP6_VDIFF)
(IMVP6_PHASE1)
(IMVP6_PHASE2)
IMVP6_NTC_R
IMVP6_VDIFF_RC
IMVP6_COMP_RC
IMVP6_VO_R
LAYOUT NOTE:
Place R7126 in hot spot of reg circuit.
LAYOUT NOTE:
PLACE R7108 CLOSE TO RBIAS PIN
LAYOUT NOTE:
PLACE CLOSE TO L7100
EMC: C7147 PLACE AT Q7100.5
EMC: C7145 PLACE AT L7100.2
EMC: C7148 PLACE AT L7102.5
NOSTUFF
OMIT
CRITICAL
IMVP6 CPU VCORE REGULATOR
- 55W PENRYN MODT PROCESSORS: 68A CONTINUOUS CURRENT
SET R7116 TO 18.2K; OC TRIP POINT OF 86.8A, WORST CASE MIN OF 76A.
DPRSLPVR | DPRSTP* | PSI* | Operation | Mode
0 | 1 | 1 | 3/2-PHASE | CCM
0 | 1 | 0 | 2/1-PHASE | CCM
1 | 0 | 1 | 3/2-PHASE | DCM
1 | 0 | 0 | 2/1-PHASE | DCM
IMVP6 CPU VCore Regulator
SYNC_DATE=01/08/2008
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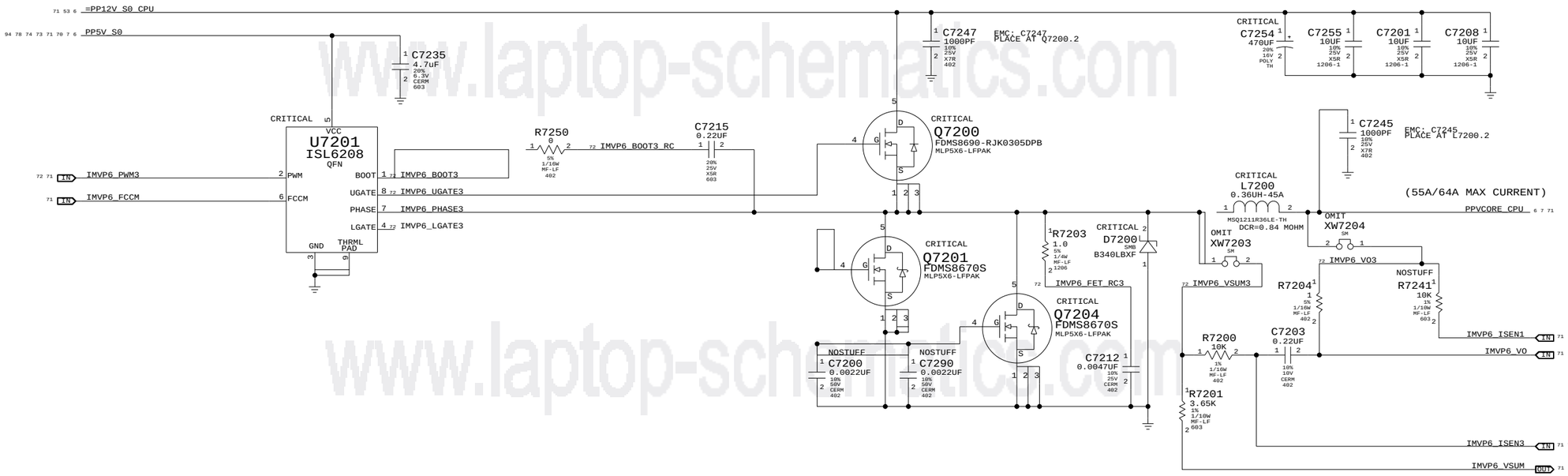
SCALE NONE
SHT 71 OF 118

IMVP6 CPU VCORE REGULATOR



NO TEST FOR CPU VREG, ADDED K2/K3

IMVP6_VO1	NO_TEST=TRUE	
IMVP6_VO2	NO_TEST=TRUE	
IMVP6_VO3	NO_TEST=TRUE	
IMVP6_VSUM1	NO_TEST=TRUE	
IMVP6_VSUM2	NO_TEST=TRUE	
IMVP6_VSUM3	NO_TEST=TRUE	

IMVP6_PWM3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.23 MM	T51
IMVP6_PHASE3	MIN_LINE_WIDTH=1.5 MM	MIN_NECK_WIDTH=0.25 MM	T43
IMVP6_BOOT3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	T44
IMVP6_UGATE3	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.25 MM	T45
IMVP6_LGATE3	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.25 MM	T46
IMVP6_ISEN3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.23 MM	T48
IMVP6_FET_RC3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	T47
IMVP6_VSUM3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	T49
IMVP6_VO3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	T50
IMVP6_BOOT3_RC	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	T52

IMVP6 3RD PHASE

SYNC_DATE=01/08/2008

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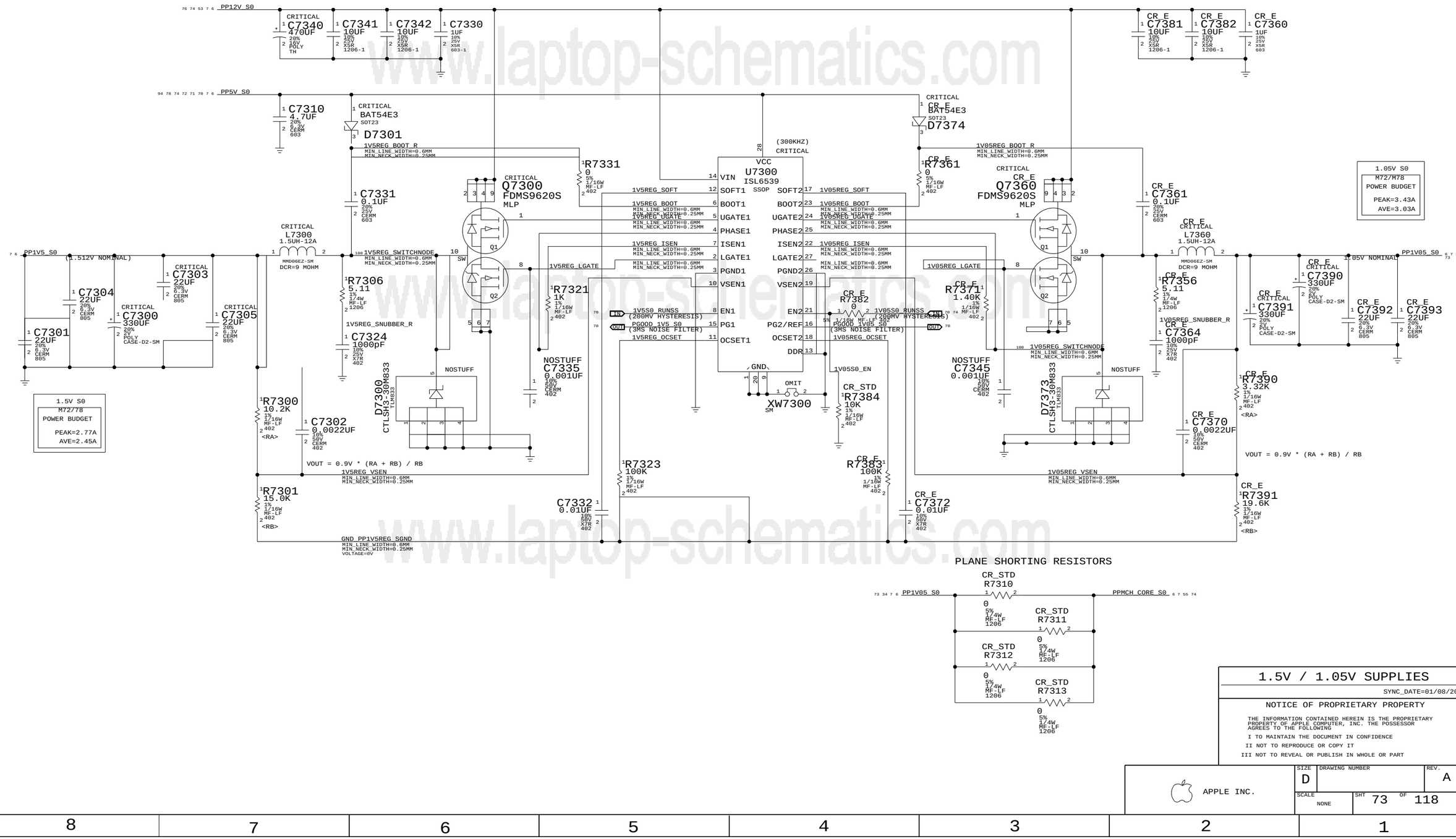
SIZE	DRAWING NUMBER	REV.
D		A

SCALE	SHT	OF
NONE	72	118

www.laptop-schematics.com

1.5V S0 & 1.05V SO RAILS



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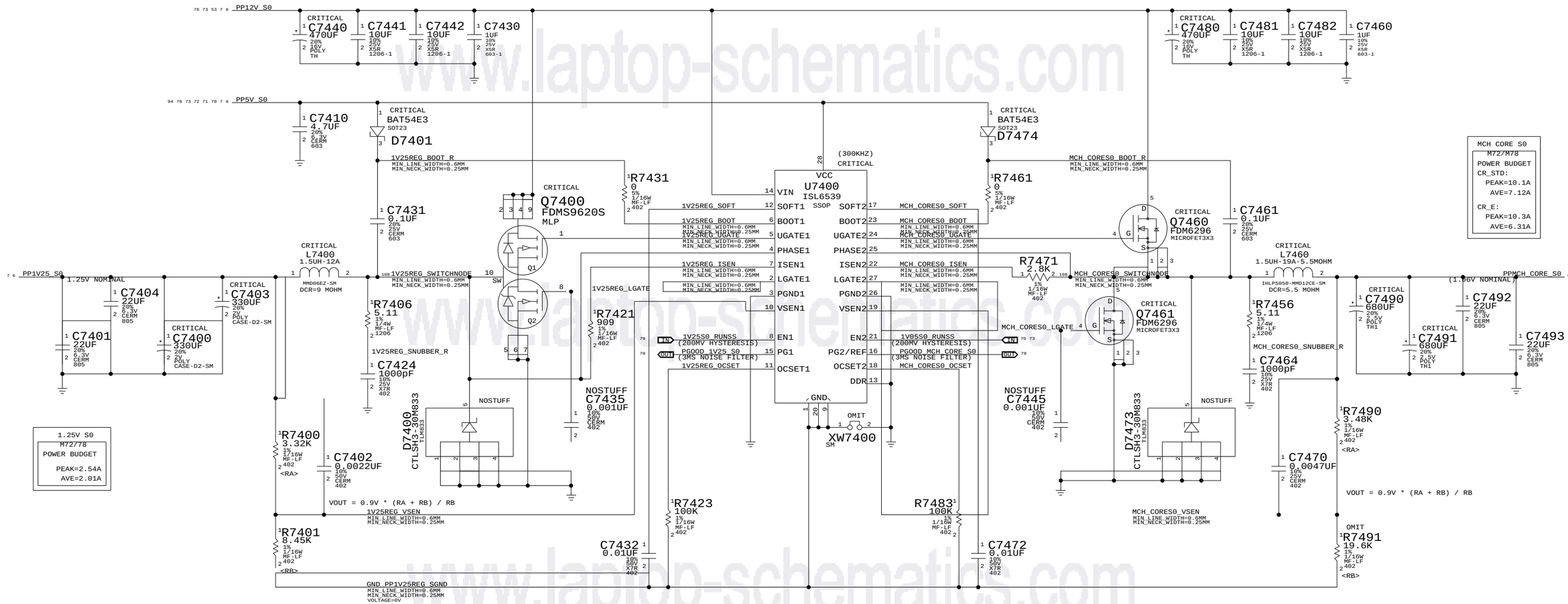
1.25V S0 & MCH CORE RAILS



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0342	1	RES,MTL FILM,1/16W,19.6K,1,0402,SMD,LF	R7491		CR_STD
114S0309	1	RES,MTL FILM,1/16W,8.66K,1,0402,SMD,LF	R7491		CR_E

1.25V / MCH CORE SUPPLIES

SYNC_DATE=01/08/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D		A

SCALE	SHT	OF
NONE	74	118

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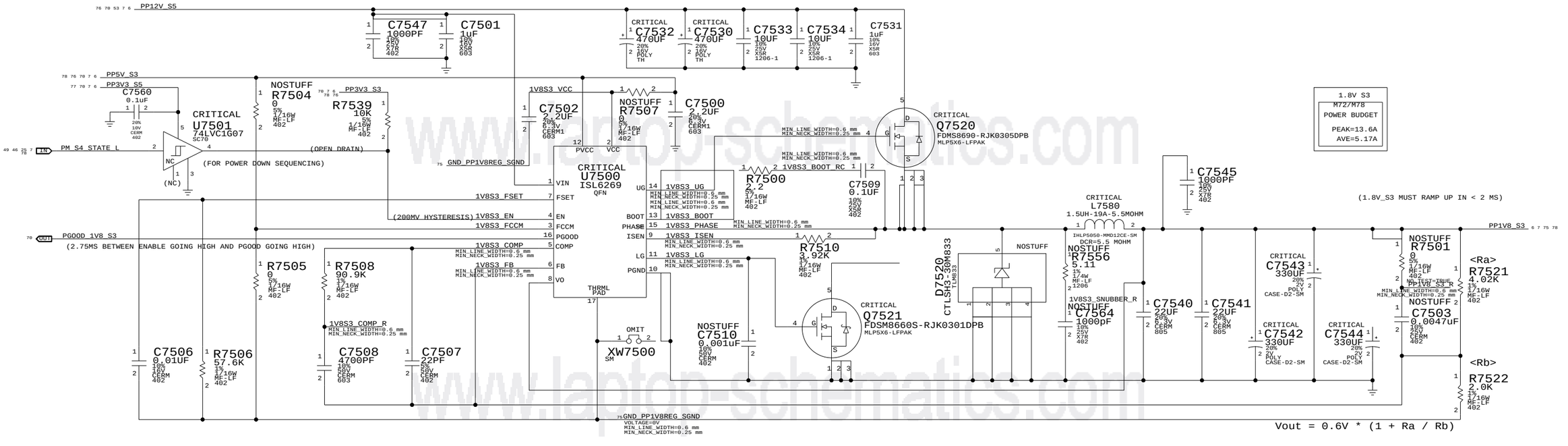
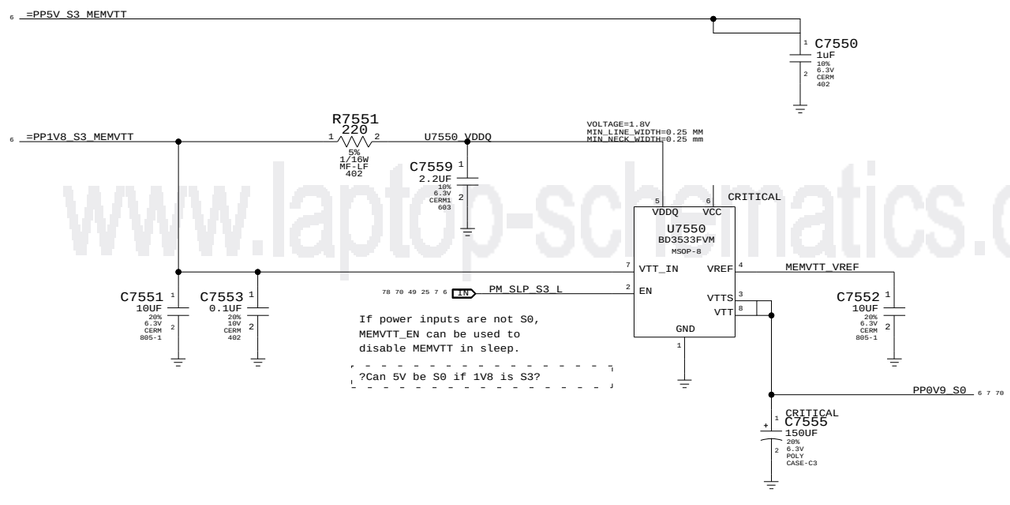
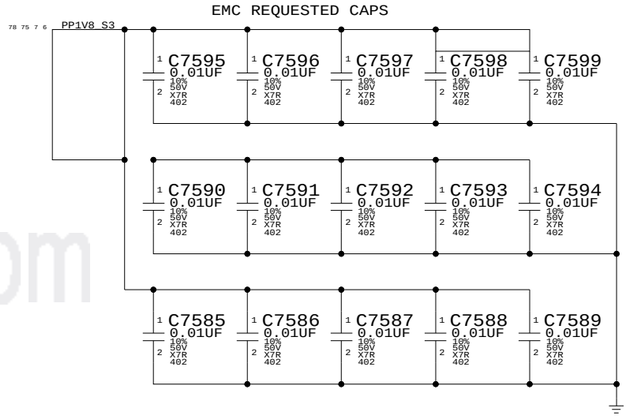
1.8V S3 / MEM VTT RAILS



DDR2 Vtt Regulator



EMC REQUESTED CAPS



1.8V S3 /0.9V S0 SUPPLIES

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SIZE	DRAWING NUMBER	REV.
D		A
SCALE: NONE	SHT 75 OF 118	

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5V S5 & 3.3V S3 RAILS

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PP12V_S0
PP5V_S5
R7615 1.65K 1% 1/16W MF-LF 402
R7616 10K 1% 1/16W MF-LF 402
R7613 10K 1% 1/16W MF-LF 402
R7614 10K 1% 1/16W MF-LF 402
5VS5_4V29_REF
12VS0_6V0_REF
R7617 4.99K 1% 1/16W MF-LF 402
12VS0_COMP_REF
R7618 100K 1% 1/16W MF-LF 402
CRITICAL
U7601 LM393A SOI-1-LF
PGOOD_12V_S0
(DUAL PACKAGE: SUPPLY PINS CONNECTED ON BOTTOM OF PAGE)

PP12V_S5

R7621 3.65K 1% 1/16W MF-LF 402
C7609 0.1UF 10% 16V X5R 402
R7629 47.5K 1% 1/16W MF-LF 402
C7631 0.1UF 10% 16V X5R 402
R7626 3.92K 1% 1/16W MF-LF 402

C7643 10UF 10% 25V X5R 1206-1
C7640 10UF 10% 25V X5R 1206-1
C7641 10UF 10% 25V X5R 1206-1
C7642 10UF 10% 25V X5R 1206-1

3V3S3_SNS_N
3V3S3_SNS_P
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

PP5VREG_INTVCC
CRITICAL D7624 CMDSH-3 SOD-323
3V3S3_BOOST_R
R7624 0 5% 1/16W MF-LF 402
C7622 22PF 5% 50V CERM 402
CRITICAL Q7620 FDMS9620S MLP
C7624 0.1UF 10% 16V X5R 402

CRITICAL C7653 22UF 20% 6.3V CERM 805
CRITICAL C7654 22UF 20% 6.3V CERM 805
PP3V3_S3 (3.34V NOMINAL)
C7652 22UF 20% 6.3V CERM 805
C7650 22UF 20% 6.3V CERM 805
CRITICAL C7651 330UF-0.009OHM 20% 6.3V POLY CASE-D3L

CRITICAL L7620 1.5UH-12A MMD06EZ-SM DCR=9 MOHM
NOSTUFF D7600 CTLSH13-30M833 TLM533
SW
NOSTUFF C7621 0.001UF 10% 50V CERM 402

<Rc> R7627 63.4K 1% 1/16W MF-LF 402
C7629 100PF 5% 50V CERM 402
Vout = 0.8V * (1 + Rc / Rd)
<Rd> R7628 20.0K 1% 1/16W MF-LF 402
NOSTUFF C7628 0.001UF 10% 50V CERM 402
GND_PP5VREG_SGND
VOLTAGE=0V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

3.3V S3
M72778
POWER BUDGET
PEAK=6.06A
AVE=3.06A

C7626 22PF 5% 50V CERM 402
C7625 0.001UF 10% 50V CERM 402
3V3S3_ITH_R
R7625 4.99K 1% 1/16W MF-LF 402
P5VREG_FCB
PP5V_S5
C7605 1UF 10% 6.3V CERM 402

R7600 10 1% 1/16W MF-LF 402
PPVIN_S5_5VS5_R
VOLTAGE=12V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
C7600 1UF 10% 16V X5R 603
R7670 1M 5% 1/16W MF-LF 402
CRITICAL C7682 150UF 20% 16V ELEC SM-1
C7681 10UF 10% 25V X5R 1206-1
C7680 10UF 10% 25V X5R 1206-1

U7600 LTC3728LXC QFN

3V3S3_TG	26	TG1	
3V3S3_BOOST	24	BOOST1	
3V3S3_SW	25	SW1	
3V3S3_BG	22	BG1	
TP_P5VREG_PLLIN (INTERNAL PULLDOWN)	3	PLLIN	
	30	SENSE1+	
	31	SENSE1-	
3V3S3_VOSNS	1	VOSENSE1	
3V3S3_ITH	5	ITH1	
3V3S3_RUNSS	28	RUN_SS1	
	4	FCB	
PP5V_S5	21	EXTVCC	
	6	SGND	
	33	THRML PAD	
	19	PGND	
5VS5_TG	14	TG2	
5VS5_BOOST	17	BOOST2	
5VS5_SW	15	SW2	
5VS5_BG	18	BG2	
P5VREG_FSEL	2	PLLFLTR	
	12	SENSE2+	
	11	SENSE2-	
5VS5_VOSNS	9	VOSENSE2	
5VS5_ITH	8	ITH2	
5VS5_RUNSS (VERIFY WHETHER OK TO PULL THIS UP TO 12V)	13	RUN_SS2	
NC	7	3_3VOUT	
PGOOD_3V3_S3	27	PGOOD	
	20	INTVCC	
NC	10	NC1	
NC	16	NC2	
NC	29	NC3	
NC	32	NC4	

C7689 220PF 5% 25V CERM 402
C7670 0.1UF 10% 16V X5R 402
C7665 0.001UF 10% 50V CERM 402
5VS5_ITH_R
R7665 20.0K 1% 1/16W MF-LF 402
C7666 100PF 5% 50V CERM 402

OMIT
XW7600 SM

5VS5_SNS_N
5VS5_SNS_P
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
PP5VREG_INTVCC
CRITICAL D7664 CMDSH-3 SOD-323
5VS5_BOOST_R
R7664 0 5% 1/16W MF-LF 402
C7664 0.1UF 10% 16V X5R 402
CRITICAL Q7660 FDMS8690-RJK0305DPB MLP5X6-LFPAK

C7608 0.1UF 10% 16V X5R 402
R7661 3.65K 1% 1/16W MF-LF 402
R7669 7.68K 1% 1/16W MF-LF 402
C7632 0.1UF 10% 16V X5R 402
R7666 6.98K 1% 1/16W MF-LF 402

CRITICAL L7680 3.0UH-14A-7.52MOHM MSQ121130R0LE-TH
PP5V_S5 (5.0V NOMINAL)
C7690 22UF 20% 6.3V CERM 805
CRITICAL C7691 330UF-0.009OHM 20% 6.3V POLY CASE-D3L
CRITICAL C7692 330UF-0.009OHM 20% 6.3V POLY CASE-D3L
CRITICAL C7693 330UF-0.009OHM 20% 6.3V POLY CASE-D3L

NOSTUFF C7661 0.0022UF 10% 50V CERM 402
CRITICAL Q7661 FDSM8660S-RJK0301DPB MLP5X6-LFPAK
CRITICAL D7601 CTLSH13-30M833 TLM533
C7669 180PF 5% 50V CERM 402
<Ra> R7667 105K 1% 1/16W MF-LF 402
<Rb> R7668 20.0K 1% 1/16W MF-LF 402
Vout = 0.8V * (1 + Rc / Rd)
NOSTUFF C7668 0.001UF 10% 50V CERM 402

5V S5
M72/M78
POWER BUDGET
M72 PEAK=12.0A
M72 AVE=6.83A
M78 PEAK=8.91A
M78 AVE=5.33A

PP12V_S5
PP5V_S5
R7631 11.8K 1% 1/16W MF-LF 402
R7601 100K 1% 1/16W MF-LF 402
R7602 0 5% 1/16W MF-LF 402
SPARE
(4.46V/3.99V; 471MV HYSTERESIS)
C7612 0.1UF 20% 16V CERM 603
R7612 47K 5% 1/16W MF-LF 402
5VS3_COMP_REF
5VS5_4V24_REF2
(REPEATED FOR EASE OF ROUTING)
NOSTUFF
R7630 86.6K 1% 1/16W MF-LF 402
C7613 0.1UF 20% 10V CERM 402
(HYSTERESIS)
(R7631: 71.5K; R7630: 40.2K; 300MV HYSTERESIS)
LM393A SOI-1-LF
U7601 GND
PGOOD_5V_S3_L
Q7603 2N7002 SOT23-LF
C7630 0.1UF 10% 16V X5R 402
R7692 100K 5% 1/16W MF-LF 402

(CHANGE FCB IF WE DON'T MEET E*)
C7602 1UF 10% 6.3V CERM 402
C7601 4.7UF 20% 6.3V CERM 603
5V1V8REG_SKIP
R7606 0 5% 1/16W MF-LF 402
5V1V8REG_CONT
R7607 0 5% 1/16W MF-LF 402
C7607 0.01UF 10% 16V CERM 402
R7603 30.1K 1% 1/16W MF-LF 402
R7604 5.62K 1% 1/16W MF-LF 402
C7604 0.01UF 10% 16V CERM 402

5V S5 / 3.3V S3 SUPPLIES

SYNC_DATE=01/08/2008

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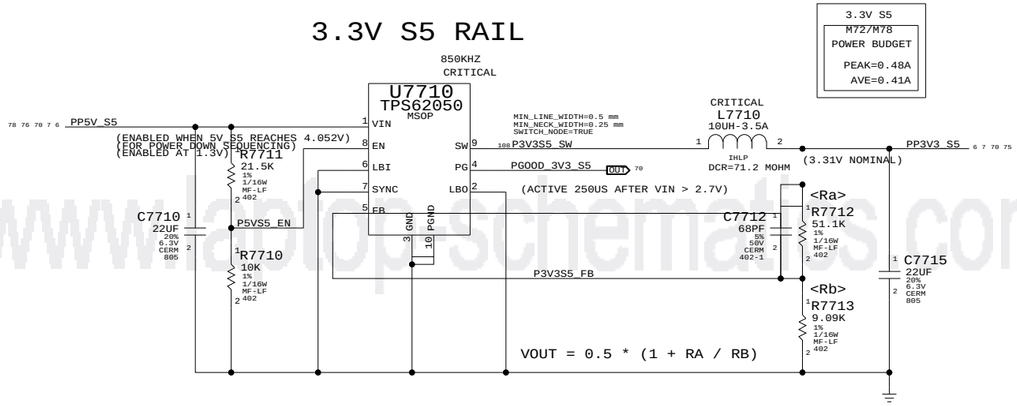
SIZE	DRAWING NUMBER	REV.
D		A
SCALE: NONE	SHT 76 OF 118	

3.3V S5 RAIL



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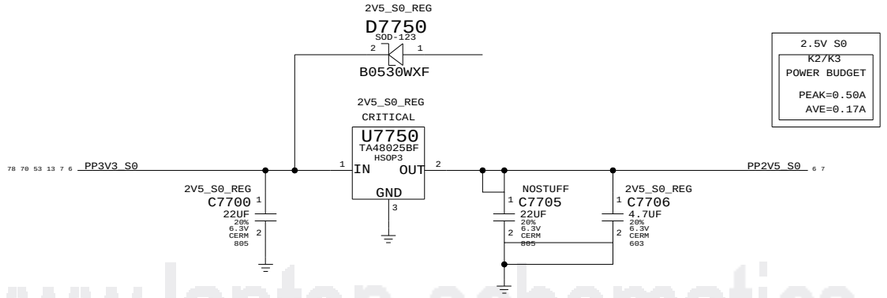
2.5V S0 RAIL (LDO)



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State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

3.3V / 2.5V POWER SUPPLIES

SYNC_DATE=01/08/2008

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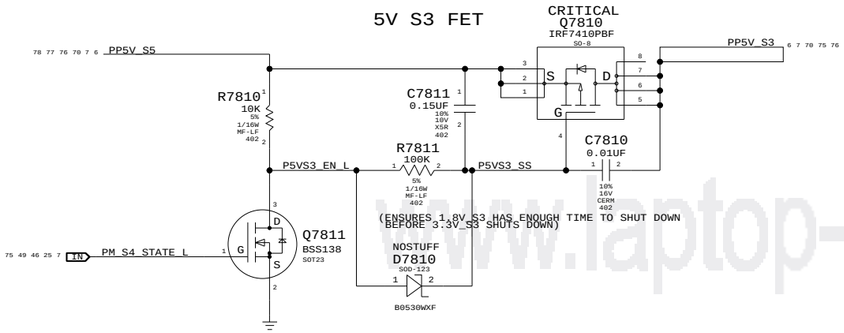
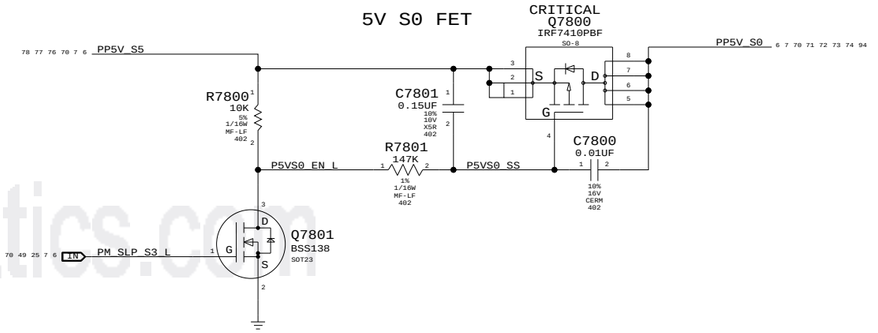
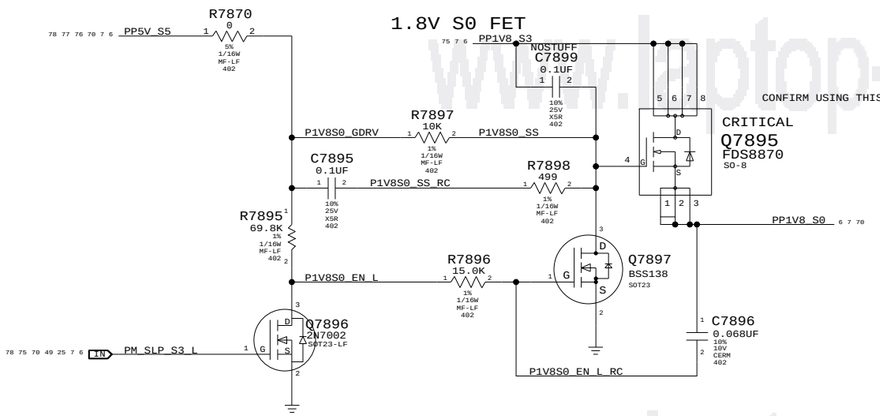
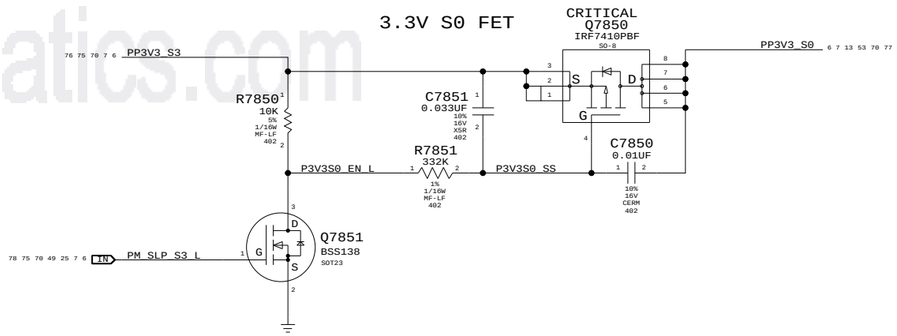
SIZE	DRAWING NUMBER	REV.
D		A
SCALE: NONE	SHT 77 OF 118	









	I	Rds(on)	Vgs +/-
IRF7410	13A	7mOHM	8V
IRF7413	9.6A	18mOHM	20V
FDS4435	8.8A	35mOHM	25V
IRF7406	5.8A	70mOHM	20V
IRF6402	3.7A	65mOHM	12V
SI2302	1.6A	115mOHM	8V

S3 & S0 FETs

SYNC_DATE=01/08/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D		A

SCALE	SHT	OF
NONE	78	118

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Page Notes

Power aliases required by this page:
- =PP12V_S0_MXM
- =PP5V_S0_MXM
- =PP1V8_S0_MXM

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Note: PCI-E Lanes are reversed to untangle routes
Need to stuff config strap using BOM option NBCFG_PEG_REVERSE
Polarity is also inverted (Tx+ goes to Rx-) to untangle routes

MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT

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APPLE P/N: 516S0562

J8400
AS0B52X-S43E-XF
F-RT-SM
(1 OF 2)
CRITICAL

=PP1V8_S0_MXM
C8410 1000PF 10% 25V X7R 402
C8401 22UF 20% 6.3V CERM 805

=PP5V_S0_MXM
C8411 1000PF 10% 25V X7R 402

(FOR ROUTING EASE ON M72/M78
(POLARITY REVERSED FOR LANES 4,7,14)

PLACE CAPS NEAR NB

ALL_SYS_PWRGD

PRSNT2_L: RESERVED FOR FUTURE USE

KEY

2	1V8RUN0	PWR_SRC0	1		
4	1V8RUN1	PWR_SRC1	3		
6	1V8RUN2	PWR_SRC2	5		
8	1V8RUN3	PWR_SRC3	7		
10	1V8RUN4	PWR_SRC4	9		
12	1V8RUN5	PWR_SRC5	11		
14	1V8RUN6	PWR_SRC6	13		
16	RUNPWROK	PWR_SRC7	15		
18	5VRUN	GND0	17		
20	GND20	GND1	19		
22	GND21	GND2	21		
24	GND22	GND3	23		
38	PRSNT2_L	PEX_RX15_L	37	PEG_D2R_N<0>	15 101
40	PEX_TX15_L	PEX_RX15	39	PEG_D2R_P<0>	15 101
42	PEX_TX15	GND4	41		
44	GND23	PEX_RX14_L	43	PEG_D2R_N<1>	15 101
46	PEX_TX14_L	PEX_RX14	45	PEG_D2R_P<1>	15 101
48	PEX_TX14	GND5	47		
50	GND24	PEX_RX13_L	49	PEG_D2R_N<2>	15 101
52	PEX_TX13_L	PEX_RX13	51	PEG_D2R_P<2>	15 101
54	PEX_TX13	GND6	53		
56	GND25	PEX_RX12_L	55	PEG_D2R_P<3>	15 101
58	PEX_TX12_L	PEX_RX12	57	PEG_D2R_N<3>	15 101
60	PEX_TX12	GND7	59		
62	GND26	PEX_RX11_L	61	PEG_D2R_P<4>	15 101
64	PEX_TX11_L	PEX_RX11	63	PEG_D2R_N<4>	15 101
66	PEX_TX11	GND8	65		
68	GND27	PEX_RX10_L	67	PEG_D2R_P<5>	15 101
70	PEX_TX10_L	PEX_RX10	69	PEG_D2R_N<5>	15 101
72	PEX_TX10	GND9	71		
74	GND28	PEX_RX9_L	73	PEG_D2R_P<6>	15 101
76	PEX_TX9_L	PEX_RX9	75	PEG_D2R_N<6>	15 101
78	PEX_TX9	GND10	77		
80	GND29	PEX_RX8_L	79	PEG_D2R_P<7>	7 15 101
82	PEX_TX8_L	PEX_RX8	81	PEG_D2R_N<7>	7 15 101
84	PEX_TX8	GND11	83		
86	GND30	PEX_RX7_L	85	PEG_D2R_P<8>	15 101
88	PEX_TX7_L	PEX_RX7	87	PEG_D2R_N<8>	15 101
90	PEX_TX7	GND12	89		
92	GND31	PEX_RX6_L	91	PEG_D2R_P<9>	15 101
94	PEX_TX6_L	PEX_RX6	93	PEG_D2R_N<9>	15 101
96	PEX_TX6	GND13	95		
98	GND32	PEX_RX5_L	97	PEG_D2R_P<10>	15 101
100	PEX_TX5_L	PEX_RX5	99	PEG_D2R_N<10>	15 101
102	PEX_TX5	GND14	101		
104	GND33	PEX_RX4_L	103	PEG_D2R_P<11>	15 101
106	PEX_TX4_L	PEX_RX4	105	PEG_D2R_N<11>	15 101
108	PEX_TX4	GND15	107		
110	GND34	PEX_RX3_L	109	PEG_D2R_P<12>	15 101
112	PEX_TX3_L	PEX_RX3	111	PEG_D2R_N<12>	15 101
114	PEX_TX3	GND16	113		
116	GND35	PEX_RX2_L	115	PEG_D2R_P<13>	15 101
118	PEX_TX2_L	PEX_RX2	117	PEG_D2R_N<13>	15 101
120	PEX_TX2	GND17	119		
122	GND36	PEX_RX1_L	121	PEG_D2R_P<14>	15 101
124	PEX_TX1_L	PEX_RX1	123	PEG_D2R_N<14>	15 101
126	PEX_TX1	GND18	125		
128	GND37	PEX_RX0_L	127	PEG_D2R_P<15>	15 101
130	PEX_TX0_L	PEX_RX0	129	PEG_D2R_N<15>	15 101
132	PEX_TX0	GND19	131		

(FOR ROUTING EASE ON M72/M78
(POLARITY REVERSED FOR LANES 0-2)

C8400 22UF 20% 35V ELEC SM-LF
C8412 1000PF 10% 25V X7R 402
C8413 1000PF 10% 25V X7R 402
C8414 1000PF 10% 25V X7R 402
C8415 1000PF 10% 25V X7R 402
C8416 1000PF 10% 25V X7R 402

PPV_S0_MXM_PWRSRC 53
VOLTAGE=12V
MIN_LINE_WIDTH=0.60MM
MIN_NECK_WIDTH=0.25MM

PEG_R2D_C_P<0>	C8420	0.1uF	16V 10% X5R 402	PEG_R2D_P<15>	
PEG_R2D_C_N<0>	C8421	0.1uF		PEG_R2D_N<15>	
PEG_R2D_C_P<1>	C8422	0.1uF		PEG_R2D_P<14>	
PEG_R2D_C_N<1>	C8423	0.1uF		PEG_R2D_N<14>	
PEG_R2D_C_P<2>	C8424	0.1uF		PEG_R2D_P<13>	
PEG_R2D_C_N<2>	C8425	0.1uF		PEG_R2D_N<13>	
PEG_R2D_C_P<3>	C8426	0.1uF		PEG_R2D_P<12>	
PEG_R2D_C_N<3>	C8427	0.1uF		PEG_R2D_N<12>	
PEG_R2D_C_N<4>	C8428	0.1uF		PEG_R2D_N<11>	
PEG_R2D_C_P<4>	C8429	0.1uF		PEG_R2D_P<11>	
PEG_R2D_C_P<5>	C8430	0.1uF		PEG_R2D_P<10>	
PEG_R2D_C_N<5>	C8431	0.1uF		PEG_R2D_N<10>	
PEG_R2D_C_P<6>	C8432	0.1uF		PEG_R2D_P<9>	
PEG_R2D_C_N<6>	C8433	0.1uF		PEG_R2D_N<9>	
PEG_R2D_C_N<7>	C8434	0.1uF		PEG_R2D_N<8>	
PEG_R2D_C_P<7>	C8435	0.1uF		PEG_R2D_P<8>	
PEG_R2D_C_P<8>	C8436	0.1uF		PEG_R2D_P<7>	
PEG_R2D_C_N<8>	C8437	0.1uF		PEG_R2D_N<7>	
PEG_R2D_C_P<9>	C8438	0.1uF		PEG_R2D_P<6>	
PEG_R2D_C_N<9>	C8439	0.1uF		PEG_R2D_N<6>	
PEG_R2D_C_P<10>	C8440	0.1uF		PEG_R2D_P<5>	
PEG_R2D_C_N<10>	C8441	0.1uF		PEG_R2D_N<5>	
PEG_R2D_C_P<11>	C8442	0.1uF		PEG_R2D_P<4>	
PEG_R2D_C_N<11>	C8443	0.1uF		PEG_R2D_N<4>	
PEG_R2D_C_P<12>	C8444	0.1uF		PEG_R2D_P<3>	
PEG_R2D_C_N<12>	C8445	0.1uF		PEG_R2D_N<3>	
PEG_R2D_C_P<13>	C8446	0.1uF		PEG_R2D_P<2>	
PEG_R2D_C_N<13>	C8447	0.1uF		PEG_R2D_N<2>	
PEG_R2D_C_N<14>	C8448	0.1uF		PEG_R2D_N<1>	
PEG_R2D_C_P<14>	C8449	0.1uF		PEG_R2D_P<1>	
PEG_R2D_C_P<15>	C8450	0.1uF		PEG_R2D_P<0>	
PEG_R2D_C_N<15>	C8451	0.1uF		PEG_R2D_N<0>	

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MXM PCI-E & PWR

SYNC_DATE=N/A

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SCALE: NONE	SHT 84 OF 118	

Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP2V5_S0_MXM

Signal aliases required by this page:
- =SMB_GPU_THRM_DATA
- =SMB_GPU_THRM_CLK

BOM options provided by this page:
24_INCH_LCD

MXM SPEC POWER REQUIREMENTS

(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT

MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J8400

=PP3V3_S0_MXM 6 85

MXM_ROM
C8570
0.1UF
20%
10V
CERM
402

STUFF FOR WRITE PROTECT
NOSTUFF
R8570
0
5%
1/16W
MF-LF
402

I2C ADDRESS: AC

U8570
M24C02-WMN6
SO8

VCC
E2/NC2
E1/NC1 CRITICAL
E0/NC0 OMIT
WC*
VSS
SDA
SCL

MXM_ROM_WP

GPU_DDC_C_DATA 85 90
GPU_DDC_C_CLK 85 90

J8400
AS0B52X-S43E-XF
F-RT-SM
(2 OF 2)

85 6 =PP3V3_S0_MXM
NOSTUFF
R8500
100K
5%
1/16W
MF-LF
402

30 29 CK505_CLKREQ1_L

28 PEG_RESET_L

85 6 =PP3V3_S0_MXM
R8502
100K
5%
1/16W

49 SMC_GFX_OVERTEMP_L

49 SMC_GFX_THROTTLE_L
10K PD ON MXM

=PP3V3_S0_MXM 6 85
R8501
100K
5%
1/16W
MF-LF
402
PULLED TO GROUND ON MXM

105 30 GPU_CLK100M_PCIE_N	133	PEX_REFCLK_L	PRSNT1_L	134	MXM_DETECT_L
105 30 GPU_CLK100M_PCIE_P	135	PEX_REFCLK	TV_C_HDTV_PR	136	GPU_TV_C 91 108
	137	CLK_REQ_L	GND46	138	
	139	PEX_RST_L	TV_Y_HDTV_Y_TV_CVBS	140	GPU_TV_Y 91 108
	141	RSVD0	GND47	142	
	143	RSVD1	TV_CVBS_HDTV_PB	144	GPU_TV_COMP 91 108
52 =SMB_GPU_THRM_SDA	145	SMB_DAT	GND48	146	
52 =SMB_GPU_THRM_SCL	147	SMB_CLK	VGA_RED	148	GPU_RED 91 108
	149	THERM_L	GND49	150	
108 91 GPU_H2SYNC	151	VGA_HSYNC	VGA_GRN	152	GPU_GRN 91 108
108 91 GPU_V2SYNC	153	VGA_VSYNC	GND50	154	
94 GPU_DDC_A_CLK	155	DDCA_CLK	VGA_BLU	156	GPU_BLU 91 108
EXT. DVI/VGA 94 GPU_DDC_A_DATA	157	DDCA_DAT	GND51	158	
	159	IGP0	LVDS_UCLK_L	160	LVDS_U_CLK_N 90 108
	161	IGP1	LVDS_UCLK	162	LVDS_U_CLK_P 90 108
	163	IGP2	GND52	164	
	165	RSVD2	LVDS_UTX3_L	166	LVDS_U_DATA_N<3> 90 108
	167	RSVD3	LVDS_UTX3	168	LVDS_U_DATA_P<3> 90 108
49 SMC_GFX_THROTTLE_L	169	AC_BATT_L	GND53	170	MXM_PIN170
	171	IGP3	LVDS_UTX2_L	172	LVDS_U_DATA_N<2> 90 108
	173	IGP4	LVDS_UTX2	174	LVDS_U_DATA_P<2> 90 108
	175	IGP5	GND54	176	
	177	IGP6	LVDS_UTX1_L	178	LVDS_U_DATA_N<1> 90 108
	179	IGP7	LVDS_UTX1	180	LVDS_U_DATA_P<1> 90 108
	181	IGP8	GND55	182	
	183	IGP9	LVDS_UTX0_L	184	LVDS_U_DATA_N<0> 90 108
	185	IGP10	LVDS_UTX0	186	LVDS_U_DATA_P<0> 90 108
	187	GND38	GND56	188	
	189	IGP_DVI_B_CLK_L	LVDS_LCLK_L	190	LVDS_L_CLK_N 90 108
	191	IGP_DVI_B_CLK	LVDS_LCLK	192	LVDS_L_CLK_P 90 108
	193	DVI_B_HPD_GND	GND57	194	
	195	RSVD4	LVDS_LTX3_L	196	LVDS_L_DATA_N<3> 90 108
	197	RSVD5	LVDS_LTX3	198	LVDS_L_DATA_P<3> 90 108
	199	GND39	GND58	200	
	201	IGP_DVI_B_TX2_L	LVDS_LTX2_L	202	LVDS_L_DATA_N<2> 90 108
	203	IGP_DVI_B_TX2	LVDS_LTX2	204	LVDS_L_DATA_P<2> 90 108
	205	GND40	GND59	206	
	207	IGP_DVI_B_TX1_L	LVDS_LTX1_L	208	LVDS_L_DATA_N<1> 90 108
	209	IGP_DVI_B_TX1	LVDS_LTX1	210	LVDS_L_DATA_P<1> 90 108
	211	GND41	GND60	212	
	213	IGP_DVI_B_TX0_L	LVDS_LTX0_L	214	LVDS_L_DATA_N<0> 90 108
	215	IGP_DVI_B_TX0	LVDS_LTX0	216	LVDS_L_DATA_P<0> 90 108
94 GPU_HPD	217	DVI_A_HPD	GND61	218	
108 94 TMDS_CLK_N	219	DVI_A_CLK_L	DDCC_DAT	220	GPU_DDC_C_DATA 85 90
108 94 TMDS_CLK_P	221	DVI_A_CLK	DDCC_CLK	222	GPU_DDC_C_CLK 85 90
	223	GND42	LVDS_PPEN	224	GPU_DIGON 90
108 94 TMDS_DATA_N<2>	225	DVI_A_TX2_L	LVDS_BL_BRGHT	226	GPU_VARY_BL 90 PWM
108 94 TMDS_DATA_P<2>	227	DVI_A_TX2	LVDS_BLEN	228	GPU_ENABLE_BL
	229	GND43	DDCB_DAT	230	TP_GPU_DDC_B_DATA
108 94 TMDS_DATA_N<1>	231	DVI_A_TX1_L	DDCB_CLK	232	TP_GPU_DDC_B_CLK UNCONNECTED. USE DDC_A FOR EXT. TMDS
108 94 TMDS_DATA_P<1>	233	DVI_A_TX1	2V5RUN	234	=PP2V5_S0_MXM 6
	235	GND44	GND62	236	
108 94 TMDS_DATA_N<0>	237	DVI_A_TX0_L	3V3RUN0	238	=PP3V3_S0_MXM 6 85
108 94 TMDS_DATA_P<0>	239	DVI_A_TX0	3V3RUN1	240	
	241	GND45	3V3RUN2	242	

TO INTERNAL PANEL

INPUT ENABLES HDMI FOR NVIDIA CARDS

REMOVE THESE RESISTORS IN PROTO 2
IF THIS PIN CONFIRMED TO BE USED
FOR MXM_SPDIF IN

R8505
0
5%
1/10W
MF-LF
402

24_INCH_LCD
R8503
0
5%
1/10W
MF-LF
402
INV_EN_BL_OR_PANEL_ID 6 28

C8500
22uF
20%
6.3V
X5R
805

C8511
1000PF
10%
25V
X7R
402
EMC: C8511

C8510
1000PF
10%
25V
X7R
402
EMC: C8510

MXM I/O

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Page Notes

Power aliases required by this page:
- =PPV_S0_LCD_24INCH
- =PPV_S0_LCD_20INCH
- =PP3V3_S0_VIDEO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
20_INCH_LCD, 24_INCH_LCD

94 91 6 =PP3V3_S0_VIDEO — I20 — =PP3V3_DDC_LCD 90

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LCD (LVDS) INTERFACE

6 =PPV_S0_LCD_24INCH — 24_INCH_LCD R9002 0 5% 1/8W MF-LF 805

6 =PPV_S0_LCD_20INCH — 20_INCH_LCD R9003 0 5% 1/8W MF-LF 805

PANEL POWER SEQUENCING

PPV_S0_LCD
VOLTAGE=12V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

R9000 100K 5% 1/10W MF-LF 402

C9000 0.1UF 10% 50V X7R 603-1

NOSTUFF R9090 0 5% 1/8W MF-LF 805

PLACE NEAR J9002

CRITICAL

R9001 29.4K 1% 1/10W MF-LF 402

LCD_PWREN_DIV

LCD_PWREN_L_RC

Q9000 SI3443DV TSOP-LF

PPV_LCD_SW
VOLTAGE=12V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

L9000 FERR-250-OHM SM

VOLTAGE=12V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

C9020 10UF 10% 16V X5R-CERM 1210

C9001 0.001uF 20% 50V CERM 402

PPV_LCD_CONN 6 90

5V FOR 20 INCH LCD
12V FOR 24 INCH LCD

OMIT R9099 100K 5% 1/10W MF-LF 402

LCD_PWREN_L

Q9001 2N7002 SOT23-LF

85 GPU_DIGON

R9070 100K 5% 1/16W MF-LF 402

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0114	1	RES,100K,5%,0402	R9099		24_INCH_LCD
116S0004	1	RES,0,5%,0402	R9099		20_INCH_LCD

CRITICAL
SDF9000
STDOFF-4.0OD4.6H-1.35-2.4-TH

516S0241
CRITICAL
J9002
53307-3052
F-ST-SM

108 85 LVDS_U_DATA_N<0>	1	2	LVDS_U_DATA_P<0> 85 108
108 85 LVDS_U_DATA_N<1>	3	4	LVDS_U_DATA_P<1> 85 108
108 85 LVDS_U_DATA_N<2>	5	6	LVDS_U_DATA_P<2> 85 108
	7	8	LVDS_U_CLK_N 85 108
108 85 LVDS_U_CLK_P	9	10	LVDS_U_DATA_N<3> 85 108
108 85 LVDS_U_DATA_P<3>	11	12	LVDS_L_DATA_N<0> 85 108
108 85 LVDS_L_DATA_P<0>	13	14	
108 85 LVDS_L_DATA_N<1>	15	16	LVDS_L_DATA_P<1> 85 108
	17	18	LVDS_L_DATA_N<2> 85 108
108 85 LVDS_L_DATA_P<2>	19	20	LVDS_L_CLK_N 85 108
108 85 LVDS_L_CLK_P	21	22	LVDS_L_DATA_N<3> 85 108
108 85 LVDS_L_DATA_P<3>	23	24	
90 =PP3V3_DDC_LCD	25	26	GPU_DDC_C_DATA 85
90 6 PPV_LCD_CONN	27	28	PPV_LCD_CONN 6 90
	29	30	

Panel has 4.7K DDC pull-ups
MXM also has 2.2K pull-ups

C9010 0.001uF 20% 50V CERM 402

CRITICAL
SDF9001
STDOFF-4.0OD4.6H-1.35-2.4-TH

INVERTER INTERFACE

INVERTER CONNECTOR INCORPORATED INTO AC/DC CONNECTOR

85 GPU_VARY_BL — R9075 47 5% 1/16W MF-LF 402 — LCD_PWM 6

NOSTUFF R9074 10K 5% 1/10W MF-LF 402

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INTERNAL DISPLAY CONNS

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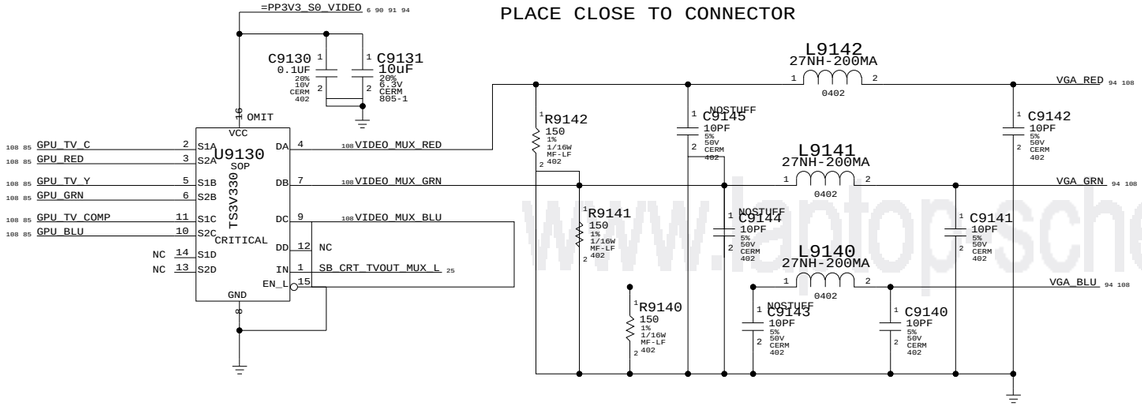
ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

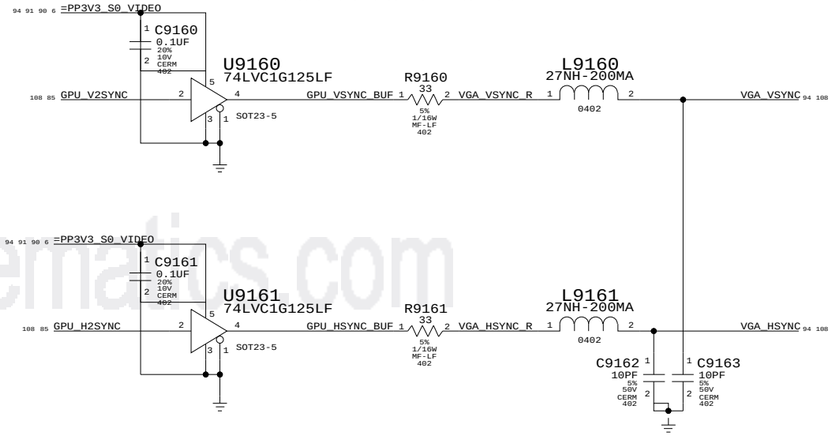


VIDEO_MUX_SEL	OUT
1	CRT
0	TV

PLACE U9120 NEAR GMCH

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1700	1	QUAD SPDT HIGH-BANDWITDH VIDEO SWITCH,LOW ON-RES	U9130	CRITICAL	

PLACE R9760 & R9761 CLOSE TO DVI CONNECTOR



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Analog Video Support

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D		A
SCALE: NONE	SHT 91 OF 118	

DVI INTERFACE

TMDS TERMINATION, IF ANY, IS ON MXM CARD

PLACE FILTER CLOSE TO MINI-DVI CONNECTOR

R9400 0 OMIT — L9400 CRITICAL 90-OHM-200MA — TMDS_DATA_N<0> — TMDS_CONN_DN<0>
R9402 0 OMIT — TMDS_DATA_P<0> — TMDS_CONN_DP<0>
R9403 0 OMIT — L9401 CRITICAL 90-OHM-200MA — TMDS_DATA_N<1> — TMDS_CONN_DN<1>
R9405 0 OMIT — TMDS_DATA_P<1> — TMDS_CONN_DP<1>
R9404 0 OMIT — L9402 CRITICAL 90-OHM-200MA — TMDS_DATA_N<2> — TMDS_CONN_DN<2>
R9409 0 OMIT — TMDS_DATA_P<2> — TMDS_CONN_DP<2>
R9408 0 OMIT — L9403 CRITICAL 90-OHM-200MA — TMDS_CLK_N — TMDS_CONN_CLKN
R9415 0 OMIT — TMDS_CLK_P — TMDS_CONN_CLKP

DVI DDC CURRENT LIMIT

(55mA requirement per DVI spec)

PP5V_S0 — D9410 SOD-123 B0530WXF — PP5V_S0_DDC_DIODE — F9410 CRITICAL 0.10A-15V 805 — PP5V_S0_DDC_FUSE — L9410 400-OHM-EMI SM-1 — PP5V_S0_DDC

DON'T USE M51 SPECIFIC: 514S0129
APPLE PN: 514S0204

J9410 OMIT CRITICAL MINI-DVI-M72 F-ST-SM1

DVI_HPD_UF	25	1	TMDS_CONN_DP<2>
	17	9	
DVI_DDC_CLK_UF	26	2	TMDS_CONN_DN<2> NO_TEST=TRUE
DVI_DDC_DATA_UF	18	10	
	27	3	TMDS_CONN_DP<1>
	19	11	
	28	4	TMDS_CONN_DN<1> NO_TEST=TRUE
VGA_BLU	20	12	
VGA_HSYNC	29	5	TMDS_CONN_DP<0>
		13	
	30	6	TMDS_CONN_DN<0> NO_TEST=TRUE
VGA_GRN	22	14	
VGA_VSYNC	31	7	TMDS_CONN_CLKP
		15	
	32	8	TMDS_CONN_CLKN NO_TEST=TRUE
VGA_RED	24	16	

DVI_CHASSIS_33 — DVI_CHASSIS_34 — =GND_CHASSIS_DVI

FOR IMAGE PLANE, THE SHELL PINS OF THE CONNECTOR ARE ALIASED DIRECTLY TO DIGITAL GROUND. IF CAPS ARE NECESSARY LATER, THEY SHOULD BE ADDED TO THE PAGE WHERE =SIGNAL =GND_CHASSIS_DVI IS CONNECTED

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S0204	1	CONN,RCPT,MINI_DVI,SMT,14 DGE,32P	J9410	CRITICAL	

PLACE CLOSE TO MINI-DVI CONNECTOR
3V LEVEL SHIFTERS

PP5V_S0_DDC

R9410 4.7K — R9412 4.7K — =PP3V3_S0_VIDEO — NO PULL UPS ON MXM CARD TO PREVENT LEAKAGE PATH

DVI_DDC_CLK_UF — R9411 100 — Q9411 2N7002DW-X-F SOT-363 — R9420 4.7K — DVI_DDC_CLK — GPU_DDC_A_CLK
C9411 100pF 5% 50V CERM 402

DVI_DDC_DATA_UF — R9413 100 — Q9411 2N7002DW-X-F SOT-363 — R9421 4.7K — DVI_DDC_DATA — GPU_DDC_A_DATA
C9413 100pF 5% 50V CERM 402

DVI_HPD_UF — R9414 0 — GPU_HPD

C9410 0.01uF 20% 50V CERM 603
C9414 0.0047UF 10% 25V CERM 402

NOSTUFF R9422 100K — NOSTUFF D9400 CASE425 MMSZ4681XXG

Note: this clamp is supposed to be on the MXM card

R9414 SHOULD BE GREATER THAN 0 IF MXM CARD DOES NOT HAVE A CURRENT LIMITING RESISTOR ON THIS LINE

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External Display Conns

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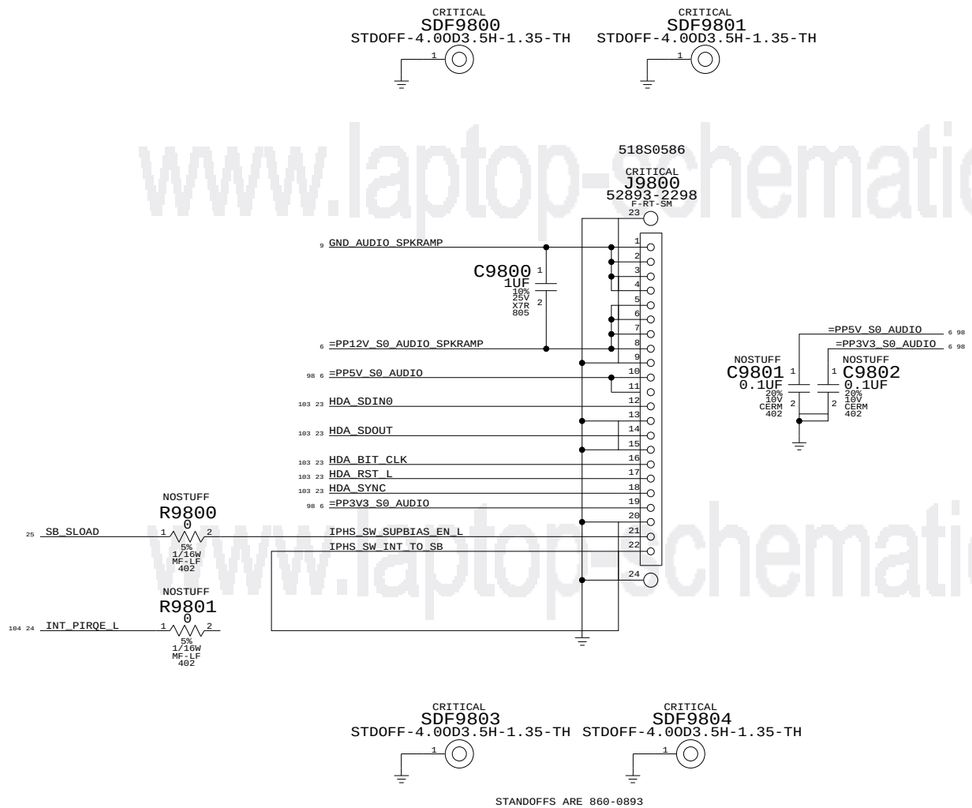
SCALE	SHT	OF
NONE	94	118



STANDOFFS ARE 860-0893

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MLB: AUDIO CONNECTOR

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D		A

SCALE	SHT	OF
NONE	98	118

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_DSTB_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
FSB_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	*	*	SPACING_0.2MM
FSB_ADSTB	*	*	SPACING_0.3MM
FSB_DATA	*	*	SPACING_0.2MM
FSB_DSTB	*	*	SPACING_0.3MM
FSB_COMMON	*	*	SPACING_0.2MM

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

CPU Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CPU_55S	*	55_OHM_SE
CPU_27P4S	*	27P4_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_2TO1	*	*	SPACING_0.2MM
CPU_COMP	*	*	SPACING_0.6MM
CPU_GTLREF	*	*	SPACING_0.6MM
CPU_ITP	*	*	SPACING_0.2MM
CPU_VCCSENSE	*	*	SPACING_0.6MM

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_ADS_L	10 14
FSB_COMMON_PP	FSB_55S	FSB_COMMON	FSB_BNR_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BPRI_L	10 14
FSB_COMMON_PP	FSB_55S	FSB_COMMON	FSB_BREQ0_L	7 10 14
FSB_COMMON_PP	FSB_55S	FSB_COMMON	FSB_DBSY_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DEFER_L	10 14
FSB_COMMON_PP	FSB_55S	FSB_COMMON	FSB_DPWR_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DRDY_L	10 14
FSB_COMMON_PP	FSB_55S	FSB_COMMON	FSB_HIT_L	7 10 14
FSB_COMMON_PP	FSB_55S	FSB_COMMON	FSB_HITM_L	7 10 14
FSB_COMMON_2PP	FSB_55S	FSB_COMMON	FSB_LOCK_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_TRDY_L	10 14
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB_CPURST_L	7 10 13 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_D_L<15..1>	10 14
FSB_DATA_GROUP0_PP	FSB_55S	FSB_DATA	FSB_D_L<0>	7 10 14
FSB_DATA_GROUP0_PP	FSB_55S	FSB_DATA	FSB_DINV_L<0>	7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<0>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<0>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_D_L<31..17>	10 14
FSB_DATA_GROUP1_PP	FSB_55S	FSB_DATA	FSB_D_L<16>	7 10 14
FSB_DATA_GROUP1_PP	FSB_55S	FSB_DATA	FSB_DINV_L<1>	7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<1>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<1>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_D_L<47..42>	10 14
FSB_DATA_GROUP2_PP	FSB_55S	FSB_DATA	FSB_D_L<41>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_D_L<40..32>	10 14
FSB_DATA_GROUP2_PP	FSB_55S	FSB_DATA	FSB_DINV_L<2>	7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<2>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<2>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_D_L<63..60>	10 14
FSB_DATA_GROUP3_PP	FSB_55S	FSB_DATA	FSB_D_L<59>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_D_L<58..48>	10 14
FSB_DATA_GROUP3_PP	FSB_55S	FSB_DATA	FSB_DINV_L<3>	7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<3>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_A_L<16..7>	10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_A_L<5..3>	10 14
FSB_ADDR_GROUP0_PP	FSB_55S	FSB_ADDR	FSB_A_L<6>	7 10 14
FSB_ADDR_GROUP0_PP	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	7 10 14
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<0>	7 10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB_A_L<35..28>	10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB_A_L<26..17>	10 14
FSB_ADDR_GROUP1_PP	FSB_55S	FSB_ADDR	FSB_A_L<27>	7 10 14
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<1>	7 10 14
CPU_IERR_L	CPU_55S		CPU_IERR_L	10
CPU_FERR_L	CPU_55S		CPU_FERR_L	10 23
CPU_PROCHOT_L	CPU_55S	CPU_2TO1	CPU_PROCHOT_L	10 50 55
CPU_PWRGD	CPU_55S		CPU_PWRGD	7 10 13 23
CPU_FROM_SB_PP	CPU_55S		CPU_INTR	7 10 23
CPU_FROM_SB_PP	CPU_55S		CPU_NMI	7 10 23
CPU_FROM_SB_PP	CPU_55S		CPU_A20M_L	7 10 23
CPU_FROM_SB	CPU_55S		CPU_DPSLP_L	10 23
CPU_FROM_SB_PP	CPU_55S		CPU_IGNNE_L	7 10 23
CPU_INIT_L	CPU_55S		CPU_INIT_L	7 10 23 51
CPU_FROM_SB_PP	CPU_55S		CPU_SMI_L	7 10 23
CPU_FROM_SB_PP	CPU_55S		CPU_STPCLK_L	7 10 23
PM_THRMTRIP_L	CPU_55S	CPU_2TO1	PM_THRMTRIP_L	10 16 23 50
FSB_CPUSLP_L	CPU_55S		FSB_CPUSLP_L	10 14
PM_DPRSLPVR	CPU_55S	CPU_2TO1	PM_DPRSLPVR	16 25 71
	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	71
CPU_BSEL0	CPU_55S	CPU_2TO1	CPU_BSEL<0>	10 30
	CPU_55S	CPU_2TO1	NB_BSEL<0>	13 16 30
CPU_BSEL1	CPU_55S	CPU_2TO1	CPU_BSEL<1>	10 30
	CPU_55S	CPU_2TO1	NB_BSEL<1>	13 16 30
CPU_BSEL2	CPU_55S	CPU_2TO1	CPU_BSEL<2>	10 30
	CPU_55S	CPU_2TO1	NB_BSEL<2>	13 16 30
CPU_DPRSTP_L	CPU_55S	CPU_2TO1	CPU_DPRSTP_L	10 16 23 71
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU_GTLREF	10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<3>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<1>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10
XDP_TDI	CPU_55S	CPU_ITP	XDP_TDI	10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP_TDO	10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP_TMS	10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP_TCK	10 13
XDP_TRST_L	CPU_55S	CPU_ITP	XDP_TRST_L	10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP_BPM_L<4..0>	10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP_BPM_L<5>	10 13
	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 30 105
	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 30 105
(FSB_CPURST_L)	CPU_55S	CPU_ITP	ITP_CPURST_L	
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	11 12
	CPU_55S	CPU_2TO1	IMVP6_VID<6..0>	12 71
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 71
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 71
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	71
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	71

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CPU/FSB Constraints

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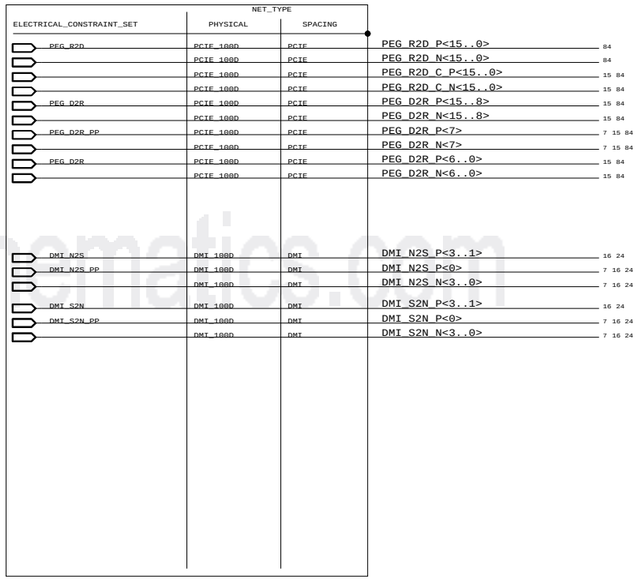
PCI-Express / DMI Bus Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE_100D	*	100_OHM_DIFF
DMI_100D	*	100_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE	*	*	SPACING_0.5MM
DMI	*	*	SPACING_0.5MM

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5



Video Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	*	100_OHM_DIFF
CRT_55S	*	55_OHM_SE
CRT_50S	*	50_OHM_SE
TMDS_100D	*	100_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	
LVDS	*	*	SPACING_0.5MM	
CRT	*	*	SPACING_0.6MM	DG Says 40 mil spacing minimum
CRT	CRT	*	SPACING_0.5MM	
TVDAC				DG Says 30 mil spacing minimum
CRT_SYNC	*	*	SPACING_0.6MM	
CRT_SYNC	CRT_SYNC	*	SPACING_0.5MM	DG Says 40 mil spacing minimum
TMDS	*	*	SPACING_0.5MM	

LVDS signals are 100-ohm +/- 20% differential impedence.
CRT & TVDAC signal single-ended impedence varies by location:
- 37.5-ohm +/- 15% from GMCH to first termination resistor.
- 50-ohm +/- 15% from first to second termination resistor.
- 55-ohm +/- 15% from second termination resistor to connector.

CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedence.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

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DDR2 Memory Bus Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_45S	*	45_OHM_SE
MEM_55S	*	55_OHM_SE
MEM_70D	*	70_OHM_DIFF
MEM_85D	*	85_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	SPACING_0.6MM
MEM_CMD	*	*	SPACING_0.15MM
MEM_CTRL	*	*	SPACING_0.6MM
MEM_DATA	*	*	SPACING_0.6MM
MEM_DQS	*	*	SPACING_0.6MM
MEM_CLK	MEM_CLK	*	SPACING_0.4MM
MEM_CLK	MEM_CTRL	*	SPACING_0.4MM
MEM_CLK	MEM_CMD	*	SPACING_0.4MM
MEM_CLK	MEM_DATA	*	SPACING_0.4MM
MEM_CLK	MEM_DQS	*	SPACING_0.4MM
MEM_CTRL	MEM_CTRL	*	SPACING_0.2MM
MEM_CTRL	MEM_CMD	*	SPACING_0.3MM
MEM_CTRL	MEM_DATA	*	SPACING_0.3MM
MEM_CTRL	MEM_DQS	*	SPACING_0.3MM
MEM_CMD	MEM_CMD	*	SPACING_0.15MM
MEM_CMD	MEM_DATA	*	SPACING_0.3MM
MEM_CMD	MEM_DQS	*	SPACING_0.3MM
MEM_DATA	MEM_DATA	*	SPACING_0.15MM
MEM_DATA	MEM_DQS	*	SPACING_0.3MM
MEM_DQS	MEM_DQS	*	SPACING_0.3MM

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_CLK_P<1..0>	16 31
	MEM_70D	MEM_CLK	MEM_CLK_N<1..0>	16 31
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<1..0>	16 31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CS_L<1..0>	16 31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_ODT<1..0>	16 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_A<14..0>	16 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_BS<2..0>	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_RAS_L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_CAS_L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_WE_L	17 31 33
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A_DQ<6..0>	17 31
MEM_A_DQ_BYTE0_PP	MEM_55S	MEM_DATA	MEM_A_DQ<7>	7 17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DQ<13..8>	17 31
MEM_A_DQ_BYTE1_PP	MEM_55S	MEM_DATA	MEM_A_DQ<14>	7 17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DQ<15>	17 31
MEM_A_DQ_BYTE2_PP	MEM_55S	MEM_DATA	MEM_A_DQ<16>	7 17 31
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A_DQ<23..17>	17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DQ<24>	17 31
MEM_A_DQ_BYTE3_PP	MEM_55S	MEM_DATA	MEM_A_DQ<25>	7 17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DQ<31..26>	17 31
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A_DQ<38..32>	17 31
MEM_A_DQ_BYTE4_PP	MEM_55S	MEM_DATA	MEM_A_DQ<39>	7 17 31
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A_DQ<46..40>	17 31
MEM_A_DQ_BYTE5_PP	MEM_55S	MEM_DATA	MEM_A_DQ<47>	7 17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DQ<53..48>	17 31
MEM_A_DQ_BYTE6_PP	MEM_55S	MEM_DATA	MEM_A_DQ<54>	7 17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DQ<55>	17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DQ<58..56>	17 31
MEM_A_DQ_BYTE7_PP	MEM_55S	MEM_DATA	MEM_A_DQ<59>	7 17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DQ<63..60>	17 31
MEM_A_DM0	MEM_55S	MEM_DATA	MEM_A_DM<0>	17 31
MEM_A_DM1	MEM_55S	MEM_DATA	MEM_A_DM<1>	17 31
MEM_A_DM2	MEM_55S	MEM_DATA	MEM_A_DM<2>	17 31
MEM_A_DM3	MEM_55S	MEM_DATA	MEM_A_DM<3>	17 31
MEM_A_DM4	MEM_55S	MEM_DATA	MEM_A_DM<4>	17 31
MEM_A_DM5	MEM_55S	MEM_DATA	MEM_A_DM<5>	17 31
MEM_A_DM6	MEM_55S	MEM_DATA	MEM_A_DM<6>	17 31
MEM_A_DM7	MEM_55S	MEM_DATA	MEM_A_DM<7>	17 31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	7 17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	7 17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	7 17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	7 17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	7 17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	7 17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	7 17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	7 17 31

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_CLK_P<4..3>	16 32
	MEM_70D	MEM_CLK	MEM_CLK_N<4..3>	16 32
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<4..3>	16 32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CS_L<3..2>	16 32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_ODT<3..2>	16 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_A<14..0>	16 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_BS<2..0>	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_RAS_L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_CAS_L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_WE_L	17 32 33
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DQ<5..0>	17 32
MEM_B_DQ_BYTE0_PP	MEM_55S	MEM_DATA	MEM_B_DQ<6>	7 17 32
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DQ<7>	17 32
MEM_B_DQ_BYTE1_PP	MEM_55S	MEM_DATA	MEM_B_DQ<8>	7 17 32
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B_DQ<15..9>	17 32
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B_DQ<22..16>	17 32
MEM_B_DQ_BYTE2_PP	MEM_55S	MEM_DATA	MEM_B_DQ<23>	7 17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DQ<24>	17 32
MEM_B_DQ_BYTE3_PP	MEM_55S	MEM_DATA	MEM_B_DQ<25>	7 17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DQ<31..26>	17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DQ<37..32>	17 32
MEM_B_DQ_BYTE4_PP	MEM_55S	MEM_DATA	MEM_B_DQ<38>	7 17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DQ<39>	17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DQ<43..40>	17 32
MEM_B_DQ_BYTE5_PP	MEM_55S	MEM_DATA	MEM_B_DQ<44>	7 17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DQ<47..45>	17 32
MEM_B_DQ_BYTE6_PP	MEM_55S	MEM_DATA	MEM_B_DQ<48>	7 17 32
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B_DQ<55..49>	17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DQ<61..56>	17 32
MEM_B_DQ_BYTE7_PP	MEM_55S	MEM_DATA	MEM_B_DQ<62>	7 17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DQ<63>	17 32
MEM_B_DM0	MEM_55S	MEM_DATA	MEM_B_DM<0>	17 32
MEM_B_DM1	MEM_55S	MEM_DATA	MEM_B_DM<1>	17 32
MEM_B_DM2	MEM_55S	MEM_DATA	MEM_B_DM<2>	17 32
MEM_B_DM3	MEM_55S	MEM_DATA	MEM_B_DM<3>	17 32
MEM_B_DM4	MEM_55S	MEM_DATA	MEM_B_DM<4>	17 32
MEM_B_DM5	MEM_55S	MEM_DATA	MEM_B_DM<5>	17 32
MEM_B_DM6	MEM_55S	MEM_DATA	MEM_B_DM<6>	17 32
MEM_B_DM7	MEM_55S	MEM_DATA	MEM_B_DM<7>	17 32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	7 17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	7 17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	7 17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	7 17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	7 17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	7 17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	7 17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	7 17 32

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Memory Constraints

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Disk Interface Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
IDE_55S	*	55_OHM_SE
SATA_55S	*	55_OHM_SE
SATA_100D	*	100_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
IDE	*	*	SPACING_0.18MM
SATA	*	*	SPACING_0.5MM

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
HDA_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HDA	*	*	SPACING_0.18MM

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB_60S	*	55_OHM_SE
USB_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	*	*	SPACING_0.5MM

DG SAYS MINIMUM SPACING 50 MILS FROM USB TO CLOCKS

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2

Internal Interface Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMB_55S	*	55_OHM_SE
SPI_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMB	*	*	SPACING_0.3MM
SPI	*	*	SPACING_0.18MM

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

NET_TYPE ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
IDE_PDD	IDE_55S	IDE	IDE_PDD<15..10>	23 44
IDE_PDD_PP	IDE_55S	IDE	IDE_PDD<9>	7 23 44
IDE_PDD	IDE_55S	IDE	IDE_PDD<8..0>	23 44
IDE_PDA	IDE_55S	IDE	IDE_PDA<2..0>	23 44
IDE_PDCS	IDE_55S	IDE	IDE_PDCS1_L	23 44
IDE_PDCS	IDE_55S	IDE	IDE_PDCS3_L	23 44
IDE_CNTL	IDE_55S	IDE	IDE_PDIOW_L	23 44
IDE_PDIOR_L	IDE_55S	IDE	IDE_PDIOR_L	7 23 44
IDE_CNTL	IDE_55S	IDE	IDE_PDDACK_L	23 44
IDE_CNTL	IDE_55S	IDE	IDE_PDDREQ	23 44
IDE_PDIORDY	IDE_55S	IDE	IDE_PDIORDY	7 23 44
IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14	23 44
IDE_RST_L	IDE_55S	IDE	ODD_RST_5VTOL_L	24 44
SATA_A_R2D	SATA_100D	SATA	SATA_A_R2D_C_P	23 45
	SATA_100D	SATA	SATA_A_R2D_C_N	23 45
	SATA_100D	SATA	SATA_A_R2D_P	45
	SATA_100D	SATA	SATA_A_R2D_N	45
SATA_A_D2R	SATA_100D	SATA	SATA_A_D2R_P	7 23 45
	SATA_100D	SATA	SATA_A_D2R_N	7 23 45
	SATA_100D	SATA	SATA_A_D2R_C_P	45
	SATA_100D	SATA	SATA_A_D2R_C_N	45
	SATA_100D	SATA	SATA_B_R2D_C_P	23 45
	SATA_100D	SATA	SATA_B_R2D_C_N	23 45
	SATA_100D	SATA	SATA_B_D2R_P	23 45
	SATA_100D	SATA	SATA_B_D2R_N	23 45
SATA_RBIAS	SATA_55S		SATA_RBIAS	45
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	23 98
	HDA_55S	HDA	HDA_BIT_CLK_R	23
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	23 98
	HDA_55S	HDA	HDA_SYNC_R	23
HDA_RST_L	HDA_55S	HDA	HDA_RST_L	23 98
	HDA_55S	HDA	HDA_RST_L_R	23
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	23 98
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	23 98
	HDA_55S	HDA	HDA_SDOUT_R	23
USB_EXTA	USB_90D	USB	USB_EXTA_P	24 46
	USB_90D	USB	USB_EXTA_N	24 46
	USB_90D	USB	USB_EXTA_MUXED_P	
	USB_90D	USB	USB_EXTA_MUXED_N	
USB_MINI	USB_90D	USB	USB_MINI_P	24 34
	USB_90D	USB	USB_MINI_N	24 34
	USB_90D	USB	USB_EXTD_P	24 46
	USB_90D	USB	USB_EXTD_N	24 46
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	7 24 47
	USB_90D	USB	USB_CAMERA_N	7 24 47
USB_BT	USB_90D	USB	USB_BT_P	7 24 47
	USB_90D	USB	USB_BT_N	7 24 47
	USB_90D	USB	USB_TPAD_P	24 47
	USB_90D	USB	USB_TPAD_N	24 47
USB_IR	USB_90D	USB	USB_IR_P	7 24 47
	USB_90D	USB	USB_IR_N	7 24 47
USB_EXTB	USB_90D	USB	USB_EXTB_P	24 46
	USB_90D	USB	USB_EXTB_N	24 46
	USB_90D	USB	USB_EXCARD_P	24 47
	USB_90D	USB	USB_EXCARD_N	24 47
USB_EXTC	USB_90D	USB	USB_EXTC_P	24 46
	USB_90D	USB	USB_EXTC_N	24 46
USB_RBIAS	USB_60S		USB_RBIAS	24
SMB_SB_SCL	SMB_55S	SMB	SMB_CLK	25 52
SMB_SB_SDA	SMB_55S	SMB	SMB_DATA	25 52
SMB_SB_ME_SCL	SMB_55S	SMB	SMB_ME_CLK	25 52
SMB_SB_ME_SDA	SMB_55S	SMB	SMB_ME_DATA	25 52
SPI_SCLK	SPI_55S	SPI	SPI_SCLK_R	24 61
	SPI_55S	SPI	SPI_SCLK	7 61
	SPI_55S	SPI	SPI_A_SCLK_R	
	SPI_55S	SPI	SPI_B_SCLK_R	
SPI_SI	SPI_55S	SPI	SPI_SI_R	24 61
	SPI_55S	SPI	SPI_SI	
	SPI_55S	SPI	SPI_A_SI_R	61
	SPI_55S	SPI	SPI_B_SI_R	
SPI_SO	SPI_55S	SPI	SPI_SO	7 24 61
	SPI_55S	SPI	SPI_A_SO_R	7 61
	SPI_55S	SPI	SPI_B_SO	
	SPI_55S	SPI	SPI_B_SO_R	
SPI_CE_L0	SPI_55S	SPI	SPI_CE_R_L<0>	24 61
	SPI_55S	SPI	SPI_CE_L<0>	7 61
SPI_CE_L1	SPI_55S	SPI	SPI_CE_R_L<1>	
	SPI_55S	SPI	SPI_CE_L<1>	

SB Constraints (1 of 2)

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PCI Bus Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCI_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCI	*	*	STANDARD

CHANGED TO 0.1MM SPACING AS THERE ARE NO PCI DEVICES

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Controller Link (AMT) Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLINK_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLINK	*	*	SPACING_0.18MM
CLINK_VREF	*	*	SPACING_0.3MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_12MIL	*	=STANDARD	0.3 MM	0.125 MM	7.5 MM	=STANDARD	=STANDARD

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Ethernet (Yukon) Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
ENET_100D	*	100_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	*	*	SPACING_0.5MM
ENET_MDI	ENET_MDI_TERM	*	SPACING_0.2MM

SOURCE: Based on Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
	PCI_55S	PCI	PCI_AD<18..0>	24 28
	PCI_55S	PCI	PCI_AD<19>	24 28
	PCI_55S	PCI	PCI_AD<20>	24 28
	PCI_55S	PCI	PCI_AD<31..21>	24 28
	PCI_55S	PCI	PCI_PAR	24 28
	PCI_55S	PCI	PCI_C_BE_L<3..0>	24 28
	PCI_55S	PCI	PCI_IRDY_L	24
	PCI_55S	PCI	PCI_DEVSEL_L	24
	PCI_55S	PCI	PCI_PERR_L	24
	PCI_55S	PCI	PCI_LOCK_L	24
	PCI_55S	PCI	PCI_SERR_L	24 28
	PCI_55S	PCI	PCI_STOP_L	24
	PCI_55S	PCI	PCI_TRDY_L	24
	PCI_55S	PCI	PCI_FRAME_L	24
	PCI_55S	PCI	PCI_FW_REQ_L	24
	PCI_55S	PCI	PCI_FW_GNT_L	24
	PCI_55S	PCI	PCI_REQ1_L	7 24
	PCI_55S	PCI	PCI_GNT1_L	
	PCI_55S	PCI	PCI_REQ2_L	7 24
	PCI_55S	PCI	PCI_GNT2_L	
INT_PIRQA_L	PCI_55S	PCI	INT_PIRQA_L	24
INT_PIRQB_L	PCI_55S	PCI	INT_PIRQB_L	24
INT_PIRQC_L	PCI_55S	PCI	INT_PIRQC_L	24
INT_PIRQD_L	PCI_55S	PCI	INT_PIRQD_L	24
INT_PIRQE_L	PCI_55S	PCI	INT_PIRQE_L	24 98
INT_PIRQF_L	PCI_55S	PCI	INT_PIRQF_L	24
PCIE_A_R2D	PCIE_100D	PCIE	PCIE_MINI_R2D_C_P	24 34
	PCIE_100D	PCIE	PCIE_MINI_R2D_C_N	24 34
PCIE_A_D2R	PCIE_100D	PCIE	PCIE_MINI_D2R_P	7 24 34
	PCIE_100D	PCIE	PCIE_MINI_D2R_N	7 24 34
PCIE_B_R2D	PCIE_100D	PCIE	PCIE_ENET_R2D_C_P	24 37
	PCIE_100D	PCIE	PCIE_ENET_R2D_C_N	24 37
PCIE_B_D2R	PCIE_100D	PCIE	PCIE_ENET_D2R_P	7 24 37
	PCIE_100D	PCIE	PCIE_ENET_D2R_N	7 24 37
PCIE_B_R2D	PCIE_100D	PCIE	PCIE_FW_R2D_C_P	40 42
	PCIE_100D	PCIE	PCIE_FW_R2D_C_N	40 42
PCIE_B_D2R	PCIE_100D	PCIE	PCIE_FW_D2R_P	7 40 42
	PCIE_100D	PCIE	PCIE_FW_D2R_N	7 40 42
GLAN_COMP			GLAN_COMP	23
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_CLK	7 16 25
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_DATA	7 16 25
CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK_NB_RESET_L	16 25
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB_CLINK_VREF	16
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF0	25
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF1	25
I149		PWR	PP1V9_ENET_PHY_AVDD	37
I147		ENET_MDI_TERM	ENET_MDI0	37
I148		ENET_MDI_TERM	ENET_MDI1	37
I149		ENET_MDI_TERM	ENET_MDI2	37
I148		ENET_MDI_TERM	ENET_MDI3	37
ENET_MDI0	ENET_100D	ENET_MDI	ENET_MDI_P<0>	37 39
	ENET_100D	ENET_MDI	ENET_MDI_N<0>	37 39
ENET_MDI1	ENET_100D	ENET_MDI	ENET_MDI_P<1>	37 39
	ENET_100D	ENET_MDI	ENET_MDI_N<1>	37 39
ENET_MDI2	ENET_100D	ENET_MDI	ENET_MDI_P<2>	37 39
	ENET_100D	ENET_MDI	ENET_MDI_N<2>	37 39
ENET_MDI3	ENET_100D	ENET_MDI	ENET_MDI_P<3>	37 39
	ENET_100D	ENET_MDI	ENET_MDI_N<3>	37 39

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Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_FSB_100D	*	100_OHM_DIFF
CLK_PCIE_100D	*	100_OHM_DIFF
CLK_MED_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	*	*	CLK_SPACING_0.6MM
CLK_PCIE	*	*	CLK_SPACING_0.5MM
CLK_MED	*	*	CLK_SPACING_0.5MM

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_P	29 30
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_N	29 30
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_P	29 30
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_N	29 30
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_P	29 30
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_N	29 30
CK505_PCIF0	CLK_MED_55S	CLK_MED	CK505_PCIF0_CLK_ITPEN	29 30
CK505_PCIF1	CLK_MED_55S	CLK_MED	CK505_PCIF1_CLK	29 30
	CLK_MED_55S	CLK_MED	CK505_PCI1_CLK	29 30
	CLK_MED_55S	CLK_MED	CK505_PCI2_CLK	29 30
CK505_PCI3	CLK_MED_55S	CLK_MED	CK505_PCI3_CLK	29 30
	CLK_MED_55S	CLK_MED	CK505_PCI4_CLK	29 30
CK505_PCI5	CLK_MED_55S	CLK_MED	CK505_PCI5_CLK_FCTSEL	29 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_48M_FSA	29 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_REF0_FSC	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_N	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_N	29 30
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_N	29 30
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_N	29 30
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_N	29 30
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_N	29 30
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_N	29 30
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_N	29 30
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_N	29 30
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_N	29 30
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	7 10 30
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	7 10 30
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	7 14 30
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	7 14 30
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 30 100
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 30 100
(CK505_PCIF0)	CLK_MED_55S	CLK_MED	PCI_CLK33M_LPCPLUS	7 30 51
(CK505_PCIF1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SB	7 24 30
(CK505_PCI2)	CLK_MED_55S	CLK_MED	PCI_CLK33M_TPM	
(CK505_PCI3)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SMC	7 30 49
			CK505 PCI4 is project-specific	
			CK505 PCI5 is project-specific	
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB_CLK48M_USBCTLR	7 25 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB_CLK14P3M_TIMER	7 25 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_FSA	30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_FSC	30
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_P	30 85
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_N	30 85
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	7 24 30
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	7 24 30
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	7 30 40
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	7 30 40
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_P	7 23 30
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_N	7 23 30
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	7 16 30
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	7 16 30
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	30 34
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	30 34
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	7 30 37
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	7 30 37

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Clock Constraints

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FireWire Interface Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
FW_110D	*	110_OHM_DIFF
FW_110D	BGA_P1MM	110_OHM_DIFF_ESCAPE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FW_TP	*	*	SPACING_0.3MM

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FW_0_TPA	FW_110D	FW_TP	FW_PORT0_TPA_P	43
	FW_110D	FW_TP	FW_PORT0_TPA_N	43
FW_0_TPB	FW_110D	FW_TP	FW_PORT0_TPB_P	43
	FW_110D	FW_TP	FW_PORT0_TPB_N	43
FW_1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_P	43
	FW_110D	FW_TP	FW_PORT1_TPA_N	43
FW_1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_P	43
	FW_110D	FW_TP	FW_PORT1_TPB_N	43
	FW_110D	FW_TP	FW_PORT1_TPA_FL_P	43
	FW_110D	FW_TP	FW_PORT1_TPA_FL_N	43
	FW_110D	FW_TP	FW_PORT1_TPB_FL_P	43
	FW_110D	FW_TP	FW_PORT1_TPB_FL_N	43

Port 2 Not Used

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_A_S3_SCL	SMB_5SS	SMB	SMBUS_SMC_A_S3_SCL	
SMBUS_SMC_A_S3_SDA	SMB_5SS	SMB	SMBUS_SMC_A_S3_SDA	
SMBUS_SMC_B_S0_SCL	SMB_5SS	SMB	SMBUS_SMC_B_S0_SCL	52
SMBUS_SMC_B_S0_SDA	SMB_5SS	SMB	SMBUS_SMC_B_S0_SDA	52
SMBUS_SMC_0_S0_SCL	SMB_5SS	SMB	SMBUS_SMC_0_S0_SCL	52
SMBUS_SMC_0_S0_SDA	SMB_5SS	SMB	SMBUS_SMC_0_S0_SDA	52
SMBUS_SMC_BSA_SCL	SMB_5SS	SMB	SMBUS_SMC_BSA_SCL	52
SMBUS_SMC_BSA_SDA	SMB_5SS	SMB	SMBUS_SMC_BSA_SDA	52
SMBUS_SMC_MGMT_SCL	SMB_5SS	SMB	SMBUS_SMC_MGMT_SCL	52
SMBUS_SMC_MGMT_SDA	SMB_5SS	SMB	SMBUS_SMC_MGMT_SDA	52

FireWire & SMC Constraints

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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	900
PWR	*	=STANDARD	900

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PWR	*	PWR_P2MM
MEM_CMD	PWR	*	PWR_P2MM
MEM_CTRL	PWR	*	PWR_P2MM
MEM_DATA	PWR	*	PWR_P2MM
MEM_DQS	PWR	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLINK_VREF	GND	*	GND_P2MM
CLK_MED	GND	*	GND_P2MM
CLK_PCIE	GND	*	GND_P2MM
DMI	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	PWR	*	PWR_P2MM
DMI	PWR	*	PWR_P2MM
SATA	PWR	*	PWR_P2MM
USB	PWR	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	PWR	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM
ENET_MDI	PWR	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_MED	PWR	*	GND_P2MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	SPACING_0.4MM
SWITCHNODE	*	*	SWITCHNODE
THERMAL	PWR	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM
SMS	*	*	SPACING_0.3MM

M72/M78 SPECIFIC NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
TMDS_DATA	TMDS_100D	TMDS	TMDS_DATA_P<3..0>	85 94
	TMDS_100D	TMDS	TMDS_DATA_N<3..0>	85 94
TMDS_CLK	TMDS_100D	TMDS	TMDS_CLK_P	85 94
	TMDS_100D	TMDS	TMDS_CLK_N	85 94
	TMDS_100D	TMDS	TMDS_CONN_DP<3..0>	94
	TMDS_100D	TMDS	TMDS_CONN_DN<3..0>	94
	TMDS_100D	TMDS	TMDS_CONN_CLKP	94
	TMDS_100D	TMDS	TMDS_CONN_CLKN	94
(USB_EXTA)	USB_90D	USB	USB_PORT0_P	46
(USB_EXTA)	USB_90D	USB	USB_PORT0_N	46
(USB_EXTB)	USB_90D	USB	USB_PORT1_P	46
(USB_EXTB)	USB_90D	USB	USB_PORT1_N	46
(USB_EXTC)	USB_90D	USB	USB_PORT2_P	46
(USB_EXTC)	USB_90D	USB	USB_PORT2_N	46
(USB_EXTD)	USB_90D	USB	USB_C_MUXED_P	46
(USB_EXTD)	USB_90D	USB	USB_C_MUXED_N	46
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_L_P	47
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_L_N	47
(USB_IR)	USB_90D	USB	USB_IR_L_P	47
(USB_IR)	USB_90D	USB	USB_IR_L_N	47
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_L_CLK_P	85 90
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_L_CLK_N	85 90
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_L_DATA_P<3..0>	85 90
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_L_DATA_N<3..0>	85 90
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_U_CLK_P	85 90
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_U_CLK_N	85 90
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_U_DATA_P<3..0>	85 90
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_U_DATA_N<3..0>	85 90
	PCIE_100D	PCIE	PCIE_FW_R2D_N	7 40
	PCIE_100D	PCIE	PCIE_FW_R2D_P	7 40
	PCIE_100D	PCIE	PCIE_FW_D2R_C_N	40
	PCIE_100D	PCIE	PCIE_FW_D2R_C_P	40
	PCIE_100D	PCIE	PCIE_ENET_R2D_P	7 37
	PCIE_100D	PCIE	PCIE_ENET_R2D_N	7 37
	PCIE_100D	PCIE	PCIE_ENET_D2R_C_P	37
	PCIE_100D	PCIE	PCIE_ENET_D2R_C_N	37
	PCIE_100D	PCIE	PCIE_MINI_R2D_N	34
	PCIE_100D	PCIE	PCIE_MINI_R2D_P	34
ENET_MDI_T	ENET_100D	ENET_MDI	ENET_MDI_T_P<0>	39
	ENET_100D	ENET_MDI	ENET_MDI_T_N<0>	39
ENET_MDI_T	ENET_100D	ENET_MDI	ENET_MDI_T_P<1>	39
	ENET_100D	ENET_MDI	ENET_MDI_T_N<1>	39
ENET_MDI_T	ENET_100D	ENET_MDI	ENET_MDI_T_P<2>	39
	ENET_100D	ENET_MDI	ENET_MDI_T_N<2>	39
ENET_MDI_T	ENET_100D	ENET_MDI	ENET_MDI_T_P<3>	39
	ENET_100D	ENET_MDI	ENET_MDI_T_N<3>	39
	ENET_100D	ENET_MDI	ENET_MDI_R_P<0>	
	ENET_100D	ENET_MDI	ENET_MDI_R_N<0>	
	ENET_100D	ENET_MDI	ENET_MDI_R_P<1>	
	ENET_100D	ENET_MDI	ENET_MDI_R_N<1>	
	ENET_100D	ENET_MDI	ENET_MDI_R_P<2>	
	ENET_100D	ENET_MDI	ENET_MDI_R_N<2>	
	ENET_100D	ENET_MDI	ENET_MDI_R_P<3>	
	ENET_100D	ENET_MDI	ENET_MDI_R_N<3>	
	CRT_50S	CRT	GPU_TV_COMP	85 91
	CRT_50S	CRT	GPU_TV_C	85 91
	CRT_50S	CRT	GPU_TV_Y	85 91
CRT_RED	CRT_50S	CRT	GPU_RED	85 91
CRT_GREEN	CRT_50S	CRT	GPU_GRN	85 91
CRT_BLUE	CRT_50S	CRT	GPU_BLU	85 91
(CRT_SYNC)	CRT_55S	CRT_SYNC	GPU_H2SYNC	85 91
(CRT_SYNC)	CRT_55S	CRT_SYNC	GPU_V2SYNC	85 91
CRT_SYNC	CRT_55S	CRT_SYNC	VGA_HSYNC	91 94
CRT_SYNC	CRT_55S	CRT_SYNC	VGA_VSYNC	91 94
(CRT_SYNC)	CRT_55S	CRT_SYNC	GPU_BUF_HSYNC	
(CRT_SYNC)	CRT_55S	CRT_SYNC	GPU_BUF_VSYNC	
	CRT_50S	CRT	VIDEO_MUX_RED	91
	CRT_50S	CRT	VIDEO_MUX_GRN	91
	CRT_50S	CRT	VIDEO_MUX_BLU	91
	CRT_55S	CRT	VGA_RED	91 94
	CRT_55S	CRT	VGA_GRN	91 94
	CRT_55S	CRT	VGA_BLU	91 94
THERM_DIFF	THERM_DIFF	THERMAL	HDD_THRMD_P	55
	THERM_DIFF	THERMAL	HDD_THRMD_N	55
THERM_DIFF	THERM_DIFF	THERMAL	ODD_THRMD_P	55
	THERM_DIFF	THERMAL	ODD_THRMD_N	55
THERM_DIFF	THERM_DIFF	THERMAL	CPU_THERMD_P	10 55
	THERM_DIFF	THERMAL	CPU_THERMD_N	10 55
THERM_DIFF	THERM_DIFF	THERMAL	GPU_HSK_THRMD_P	55
	THERM_DIFF	THERMAL	GPU_HSK_THRMD_N	55
THERM_DIFF	THERM_DIFF	THERMAL	CPU_HSK_THRMD_P	55
	THERM_DIFF	THERMAL	CPU_HSK_THRMD_N	55

M72/M78 SPECIFIC NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
		SWITCHNODE	IMVP6_PHASE1	71
		SWITCHNODE	IMVP6_PHASE2	71
		SWITCHNODE	IMVP6_PHASE3	72
		SWITCHNODE	1V05REG_SWITCHNODE	73
		SWITCHNODE	1V5REG_SWITCHNODE	73
		SWITCHNODE	MCH_CORES0_SWITCHNODE	74
		SWITCHNODE	1V25REG_SWITCHNODE	74
		SWITCHNODE	1V8S3_PHASE	75
		SWITCHNODE	5VS5_SW	76
		SWITCHNODE	3V3S3_SW	76
		SWITCHNODE	P3V3S5_SW	77
		SWITCHNODE	P2V5S0_SW	
		SMS	SMS_X_AXIS	49 50
		SMS	SMS_Y_AXIS	49 50
		SMS	SMS_Z_AXIS	49 50

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M72/M78 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	4 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT
DEFAULT	TOP,BOTTOM	Y	=55_OHM_SE	0.100 MM	3 MM	0 MM	0 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.125 MM	0.125 MM			
55_OHM_SE	*	Y	0.100 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.225 MM	0.225 MM			
40_OHM_SE	*	Y	0.185 MM	0.185 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.185 MM			
45_OHM_SE	*	Y	0.150 MM	0.150 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.340 MM	0.340 MM			
27P4_OHM_SE	*	Y	0.265 MM	0.265 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL6	Y	0.180 MM	0.180 MM		0.120 MM	0.120 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.215 MM	0.215 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL6	Y	0.120 MM	0.120 MM		0.130 MM	0.130 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.145 MM	0.145 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL6	Y	0.125 MM	0.125 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.145 MM	0.145 MM		0.175 MM	0.175 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL6	Y	0.095 MM	0.095 MM		0.205 MM	0.205 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL6	Y	0.085 MM	0.085 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.105 MM	0.100 MM		0.280 MM	0.280 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF_ESCAPE	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF_ESCAPE	TOP,BOTTOM	Y	0.105 MM	0.100 MM		0.250 MM	0.250 MM
110_OHM_DIFF_ESCAPE	ISL3,ISL6	Y	0.085 MM	0.085 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.15 MM	0.15 MM			
50_OHM_SE	*	Y	0.120 MM	0.120 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPACING_0.15MM	*	0.15 MM	?
SPACING_0.18MM	*	0.18 MM	?
SPACING_0.2MM	*	0.2 MM	?
SPACING_0.25MM	*	0.25 MM	?
SPACING_0.3MM	*	0.3 MM	?
SPACING_0.4MM	*	0.4 MM	?
SPACING_0.5MM	*	0.5 MM	?
SPACING_0.6MM	*	0.6 MM	?
SWITCHNODE	*	0.6 MM	1000
SWITCHNODE	TOP,BOTTOM	0.2 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P2MM
CLK_MED	*	BGA_P1MM	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P3MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SPACING_0.5MM	*	0.5 MM	?
CLK_SPACING_0.6MM	*	0.6 MM	?
CLK_SPACING_0.5MM	TOP,BOTTOM	0.2 MM	?
CLK_SPACING_0.6MM	TOP,BOTTOM	0.2 MM	?

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Title: Basenet Report
Design: mlb
Date: Jan 8 14:44:54 2008

Base nets and synonyms for mlb_lib.MLB(@mlb_lib.mlb(sch_1))

Base Signal	Synonyms	Location([Zone][dir])
0V9S0_COMP_REF	0V9S0_COMP_REF - @mlb_lib.MLB	70C6
1V05REG_BOOT	1V05REG_BOOT - @mlb_lib.MLB	73C4
1V05REG_BOOT_R	1V05REG_BOOT_R - @mlb_lib.MLB	73C3
1V05REG_ISEN	1V05REG_ISEN - @mlb_lib.MLB	73C4
1V05REG_LGATE	1V05REG_LGATE - @mlb_lib.MLB	73C3
1V05REG_OCSET	1V05REG_OCSET - @mlb_lib.MLB	73B4
1V05REG_SNUBBER_R	1V05REG_SNUBBER_R - @mlb_lib.MLB	73C2
1V05REG_SOFT	1V05REG_SOFT - @mlb_lib.MLB	73C4
1V05REG_SWITCHNODE	1V05REG_SWITCHNODE - @mlb_lib.MLB	73B3 108D1
1V05REG_UGATE	1V05REG_UGATE - @mlb_lib.MLB	73C4
1V05REG_VSEN	1V05REG_VSEN - @mlb_lib.MLB	73B3
1V05S0_EN	1V05S0_EN - @mlb_lib.MLB	73B4
1V05S0_RUNSS	1V05S0_RUNSS - @mlb_lib.MLB	70C5 73C3 74C3
1V05S0_RUNSS_BUF	1V05S0_RUNSS_BUF - @mlb_lib.MLB	70C6
1V5REG_BOOT	1V5REG_BOOT - @mlb_lib.MLB	73C5
1V5REG_BOOT_R	1V5REG_BOOT_R - @mlb_lib.MLB	73C6
1V5REG_ISEN	1V5REG_ISEN - @mlb_lib.MLB	73C5
1V5REG_LGATE	1V5REG_LGATE - @mlb_lib.MLB	73C5
1V5REG_OCSET	1V5REG_OCSET - @mlb_lib.MLB	73B5
1V5REG_SNUBBER_R	1V5REG_SNUBBER_R - @mlb_lib.MLB	73B7
1V5REG_SOFT	1V5REG_SOFT - @mlb_lib.MLB	73C5
1V5REG_SWITCHNODE	1V5REG_SWITCHNODE - @mlb_lib.MLB	73C6 108D1
1V5REG_UGATE	1V5REG_UGATE - @mlb_lib.MLB	73C5
1V5REG_VSEN	1V5REG_VSEN - @mlb_lib.MLB	73B7
1V5S0_RUNSS	1V5S0_RUNSS - @mlb_lib.MLB	70A5 73C5
1V5S0_RUNSS_BUF	1V5S0_RUNSS_BUF - @mlb_lib.MLB	70A6
1V8S0_COMP_REF	1V8S0_COMP_REF - @mlb_lib.MLB	70D6
1V8S3_BOOT	1V8S3_BOOT - @mlb_lib.MLB	75C5
1V8S3_BOOT_RC	1V8S3_BOOT_RC - @mlb_lib.MLB	75D5
1V8S3_COMP	1V8S3_COMP - @mlb_lib.MLB	75C6
1V8S3_COMP_R	1V8S3_COMP_R - @mlb_lib.MLB	75C6
1V8S3_EN	1V8S3_EN - @mlb_lib.MLB	75C6
1V8S3_FB	1V8S3_FB - @mlb_lib.MLB	75C6
1V8S3_FCCM	1V8S3_FCCM - @mlb_lib.MLB	75C6
1V8S3_FSET	1V8S3_FSET - @mlb_lib.MLB	75C6
1V8S3_ISEN	1V8S3_ISEN - @mlb_lib.MLB	75C5
1V8S3_LG	1V8S3_LG - @mlb_lib.MLB	75C5
1V8S3_PHASE	1V8S3_PHASE - @mlb_lib.MLB	75C5 108D1
1V8S3_SNUBBER_R	1V8S3_SNUBBER_R - @mlb_lib.MLB	75C3
1V8S3_UG	1V8S3_UG - @mlb_lib.MLB	75C5
1V8S3_VCC	1V8S3_VCC - @mlb_lib.MLB	75D6
1V25REG_BOOT	1V25REG_BOOT - @mlb_lib.MLB	74C5
1V25REG_BOOT_R	1V25REG_BOOT_R - @mlb_lib.MLB	74C6
1V25REG_ISEN	1V25REG_ISEN - @mlb_lib.MLB	74C5
1V25REG_LGATE	1V25REG_LGATE - @mlb_lib.MLB	74C5
1V25REG_OCSET	1V25REG_OCSET - @mlb_lib.MLB	74B5
1V25REG_SNUBBER_R	1V25REG_SNUBBER_R - @mlb_lib.MLB	74B7
1V25REG_SOFT	1V25REG_SOFT - @mlb_lib.MLB	74C5
1V25REG_SWITCHNODE	1V25REG_SWITCHNODE - @mlb_lib.MLB	74C6 108D1
1V25REG_UGATE	1V25REG_UGATE - @mlb_lib.MLB	74C5
1V25REG_VSEN	1V25REG_VSEN - @mlb_lib.MLB	74B7
1V25S0_RUNSS	1V25S0_RUNSS - @mlb_lib.MLB	70B5 74C5
1V25S0_RUNSS_BUF	1V25S0_RUNSS_BUF - @mlb_lib.MLB	70B6
3V3S0_COMP_REF	3V3S0_COMP_REF - @mlb_lib.MLB	70D6
3V3S3_BG	3V3S3_BG - @mlb_lib.MLB	76B5
3V3S3_BOOST	3V3S3_BOOST - @mlb_lib.MLB	76B5
3V3S3_BOOST_R	3V3S3_BOOST_R - @mlb_lib.MLB	76C6
3V3S3_ITH	3V3S3_ITH - @mlb_lib.MLB	76B5
3V3S3_ITH_R	3V3S3_ITH_R - @mlb_lib.MLB	76B6
3V3S3_RUNSS	3V3S3_RUNSS - @mlb_lib.MLB	76B5
3V3S3_SNS_N	3V3S3_SNS_N - @mlb_lib.MLB	76C6
3V3S3_SNS_P	3V3S3_SNS_P - @mlb_lib.MLB	76C6
3V3S3_SW	3V3S3_SW - @mlb_lib.MLB	76B5 108D1
3V3S3_TG	3V3S3_TG - @mlb_lib.MLB	76C5
3V3S3_VOSNS	3V3S3_VOSNS - @mlb_lib.MLB	76B5
5VS0_COMP_REF	5VS0_COMP_REF - @mlb_lib.MLB	70C6
5VS3_COMP_REF	5VS3_COMP_REF - @mlb_lib.MLB	76A7
5VS5_0V76_REF	5VS5_0V76_REF - @mlb_lib.MLB	70C6
5VS5_1V53_REF	5VS5_1V53_REF - @mlb_lib.MLB	70D6
5VS5_2V80_REF	5VS5_2V80_REF - @mlb_lib.MLB	70D6
5VS5_4V24_REF1	5VS5_4V24_REF1 - @mlb_lib.MLB	70D6
5VS5_4V24_REF2	5VS5_4V24_REF2 - @mlb_lib.MLB	76A7
5VS5_4V29_REF	5VS5_4V29_REF - @mlb_lib.MLB	76D7
5VS5_BG	5VS5_BG - @mlb_lib.MLB	76B4
5VS5_BOOST	5VS5_BOOST - @mlb_lib.MLB	76B4
5VS5_BOOST_R	5VS5_BOOST_R - @mlb_lib.MLB	76C3
5VS5_ITH	5VS5_ITH - @mlb_lib.MLB	76B4
5VS5_ITH_R	5VS5_ITH_R - @mlb_lib.MLB	76B3
5VS5_RUNSS	5VS5_RUNSS - @mlb_lib.MLB	76B4
5VS5_SNS_N	5VS5_SNS_N - @mlb_lib.MLB	76C3
5VS5_SNS_P	5VS5_SNS_P - @mlb_lib.MLB	76C3
5VS5_SW	5VS5_SW - @mlb_lib.MLB	76B4 108D1
5VS5_TG	5VS5_TG - @mlb_lib.MLB	76C4
5VS5_VOSNS	5VS5_VOSNS - @mlb_lib.MLB	76B4
12VS0_6V0_REF	12VS0_6V0_REF - @mlb_lib.MLB	76D7
12VS0_COMP_REF	12VS0_COMP_REF - @mlb_lib.MLB	76D7
=ENET_VMAIN_AVLBL	=ENET_VMAIN_AVLBL - @mlb_lib.MLB	37C2 38B3
	PP3V3_S0 - @mlb_lib.MLB	6B8 6C6 6D7 7C5 7D3 13D6 53C3 70C3 70D3 70D8 77B6 78C1
	=PP3V3_DDC_LCD - @mlb_lib.MLB	90A8 90D5
	=PP3V3_S0_VIDEO - @mlb_lib.MLB	6A4 90D7 91B4 91B4 91B7 94D2
	=PP3V3_S0_NB_VCCA_PEG_BG - @mlb_lib.MLB	6A4 19C6 21A6
	=PP3V3_S0_NB_FOLLOW - @mlb_lib.MLB	6A4 21C2
	=PP3V3_S0_TSENS - @mlb_lib.MLB	6A4 55B5 55D5 55D5 55D6 55D8
	=PP3V3_S0_SMC - @mlb_lib.MLB	6A4 53D5
	=PP3V3_S0MSWDL_SB_VCCCL3_3 - @mlb_lib.MLB	6A4 26A6 27D4
	=PP3V3_S0MSWDL_SB_VCCLAN3_3 - @mlb_lib.MLB	6A4 26A3 27D4
	=PP3V3_S0_SB_VCC3_3_VCCPCORE - @mlb_lib.MLB	6B4 26C3
	=PP3V3R1V5_S0_SB_VCCHDA - @mlb_lib.MLB	6B4 26B3 27B4
	=PP3V3_S0_SB_VCC3_3_DMI - @mlb_lib.MLB	6B4 26C3 27C4
	=PP3V3_S0_SB_VCC3_3_SATA - @mlb_lib.MLB	6B4 26C3 27C4
	=PP3V3_S0MWOL_SB_CLINK0 - @mlb_lib.MLB	6B4 25C1
	=PP3V3_S0M_CK505 - @mlb_lib.MLB	6B4 29D2 29D8 30D1
	=PP3V3_S0_SATALED - @mlb_lib.MLB	6B4 45C3
	=PP3V3_S0_MXM - @mlb_lib.MLB	6B4 85A3 85C4 85C8 85C8 85D2
	=PP3V3_S0_CK505 - @mlb_lib.MLB	6B4 29C7 30D7
	=PP3V3_S0_SMBUS_SMC_B_S0 - @mlb_lib.MLB	6B4 52C5
	=PP3V3_S0_SMBUS_SMC_MGMT - @mlb_lib.MLB	6B4 52B3
	=PP3V3_S0_SMBUS_SMC_0_S0 - @mlb_lib.MLB	6B4 52D5
	=PP3V3_S0_SMC_LS - @mlb_lib.MLB	6B4 50D2
	=PP3V3_S0_LPCPLUS - @mlb_lib.MLB	6B4 51C4
	=PP3V3_S0_SMBUS_SB - @mlb_lib.MLB	6B4 52D8
	=PP3V3_S0_IMVP - @mlb_lib.MLB	6B4 71D8
	=PP3V3_S0_AUDIO - @mlb_lib.MLB	6B4 98C4 98C6
	=PPSPD_S0_MEM - @mlb_lib.MLB	6B4 31A7 32A3 32A7
	=PP3V3_S0_FAN - @mlb_lib.MLB	6B4 56B7 56C7 57C7
	=PP3V3_S0_SB_PM - @mlb_lib.MLB	6B4 28A7
	=PP3V3_S0_PATA - @mlb_lib.MLB	6B4 44C6
	=PP3V3_S0_SB_PCI - @mlb_lib.MLB	6B4 24A3
	=PP3V3_S0_SB_VCC3_3_IDE - @mlb_lib.MLB	6B4 26C3 27D4
	=PP3V3_S0_SB_VCC3_3_PCI - @mlb_lib.MLB	6B4 26B3 27C4
	=PP3V3_S0_SB_GPIO - @mlb_lib.MLB	6B4 23D2 23D7 25B3 25D8
	=PP3V3_S0_SB_VCCGLAN3_3 - @mlb_lib.MLB	6B4 26A6
	=PP3V3_S0_SB - @mlb_lib.MLB	6C4 27D8
	=PP3V3_S0_NB_VCCHV - @mlb_lib.MLB	6C4 16B7 16C7 16C7 19B3 21A8
	PP3V3_S0 - @mlb_lib.MLB	6B8 6C6 6D7 7C5 7D3 13D6 53C3 70C3 70D3 70D8 77B6 78C1
	=PPSPD_S0_MEM - @mlb_lib.MLB	6B4 31A7 32A3 32A7
	=PP3V3_S0_VIDEO - @mlb_lib.MLB	6A4 90D7 91B4 91B4 91B7 94D2
	=PP3V3_S0_TSENS - @mlb_lib.MLB	6A4 55B5 55D5 55D5 55D6 55D8
	=PP3V3_S0_SMC_LS - @mlb_lib.MLB	6B4 50D2
	=PP3V3_S0_SMC - @mlb_lib.MLB	6A4 53D5
	=PP3V3_S0_SMBUS_SMC_MGMT - @mlb_lib.MLB	6B4 52B3
	=PP3V3_S0_SMBUS_SMC_B_S0 - @mlb_lib.MLB	6B4 52C5
	=PP3V3_S0_SMBUS_SMC_0_S0 - @mlb_lib.MLB	6B4 52D5
	=PP3V3_S0_SMBUS_SB - @mlb_lib.MLB	6B4 52D8
	=PP3V3_S0_SB_VCCGLAN3_3 - @mlb_lib.MLB	6B4 26A6
	=PP3V3_S0_SB_VCC3_3_VCCPCORE - @mlb_lib.MLB	6B4 26C3
	=PP3V3_S0_SB_VCC3_3_SATA - @mlb_lib.MLB	6B4 26C3 27C4
	=PP3V3_S0_SB_VCC3_3_PCI - @mlb_lib.MLB	6B4 26B3 27C4
	=PP3V3_S0_SB_VCC3_3_IDE - @mlb_lib.MLB	6B4 26C3 27D4
	=PP3V3_S0_SB_VCC3_3_DMI - @mlb_lib.MLB	6B4 26C3 27C4
	=PP3V3_S0_SB_PM - @mlb_lib.MLB	6B4 28A7
	=PP3V3_S0_SB_PCI - @mlb_lib.MLB	6B4 24A3
	=PP3V3_S0_SB_GPIO - @mlb_lib.MLB	6B4 23D2 23D7 25B3 25D8
	=PP3V3_S0_SB - @mlb_lib.MLB	6C4 27D8
	=PP3V3_S0_SATALED - @mlb_lib.MLB	6B4 45C3
	=PP3V3_S0_PATA - @mlb_lib.MLB	6B4 44C6
	=PP3V3_S0_NB_VCCHV - @mlb_lib.MLB	6C4 16B7 16C7 16C7 19B3 21A8
	=PP3V3_S0_NB_VCCA_PEG_BG - @mlb_lib.MLB	6A4 19C6 21A6
	=PP3V3_S0_NB_FOLLOW - @mlb_lib.MLB	6A4 21C2
	=PP3V3_S0_MXM - @mlb_lib.MLB	6B4 85A3 85C4 85C8 85C8 85D2
	=PP3V3_S0_LPCPLUS - @mlb_lib.MLB	6B4 51C4
	=PP3V3_S0_IMVP - @mlb_lib.MLB	6B4 71D8
	=PP3V3_S0_FAN - @mlb_lib.MLB	6B4 56B7 56C7 57C7
	=PP3V3_S0_ENET - @mlb_lib.MLB	6A4 38B1
	=PP3V3_S0_CK505 - @mlb_lib.MLB	6B4 29C7 30D7
	=PP3V3_S0_AUDIO - @mlb_lib.MLB	6B4 98C4 98C6
	=PP3V3_S0M_CK505 - @mlb_lib.MLB	6B4 29D2 29D8 30D1
	=PP3V3_S0MWOL_SB_VCCLAN3_3 - @mlb_lib.MLB	6A4 26A3 27D4
	=PP3V3_S0MWOL_SB_VCCCL3_3 - @mlb_lib.MLB	6A4 26A6 27D4
	=PP3V3_S0MWOL_SB_CLINK0 - @mlb_lib.MLB	6B4 25C1
	=PP3V3R1V5_S0_SB_VCCHDA - @mlb_lib.MLB	6B4 26B3 27B4
=GFX_VR_EN	=GFX_VR_EN - @mlb_lib.MLB	16B3 22A8
	TP_GFX_VR_EN - @mlb_lib.MLB	22A7
=GND_NB_VSSA_LVDS	=GND_NB_VSSA_LVDS - @mlb_lib.MLB	19C6 22C1
	TP_NB_VSSA_LVDS - @mlb_lib.MLB	22C2
=NB_CLINK_MPWROK	=NB_CLINK_MPWROK - @mlb_lib.MLB	16A3 22C2
	VR_PWRGOOD_DELAY - @mlb_lib.MLB	7C4 7C7 16B6 22C1 70C2 71C7
=PP0V9_S0M_MEM_TERM	=PP0V9_S0M_MEM_TERM - @mlb_lib.MLB	6D4 33D5
	PP0V9_S0 - @mlb_lib.MLB	6D6 7D3 70C8 75A3
=PP0V9_S3M_MEM_NBVRE FA	=PP0V9_S3M_MEM_NBVREFA - @mlb_lib.MLB	7C7 16C2 22B1
	PP0V9_S3M_MEM_NBVREFA - @mlb_lib.MLB	22B2
=PP0V9_S3M_MEM_NBVRE FB	=PP0V9_S3M_MEM_NBVREFB - @mlb_lib.MLB	7C7 16C2 22A1
	PP0V9_S3M_MEM_NBVREFB - @mlb_lib.MLB	22A2
=PP0V9_S3_MEM_A_VREF	=PP0V9_S3_MEM_A_VREF - @mlb_lib.MLB	31C1 31D6
	PP0V9_S3_MEM_A_VREF - @mlb_lib.MLB	31C2
=PP0V9_S3_MEM_B_VREF	=PP0V9_S3_MEM_B_VREF - @mlb_lib.MLB	32C1 32D7
	PP0V9_S3_MEM_B_VREF - @mlb_lib.MLB	32C2
=PP1V2_ENET_PHY	=PP1V2_ENET_PHY - @mlb_lib.MLB	37D6 38A3
	PP1V2_S3_ENET - @mlb_lib.MLB	38A3
=PP1V05_S0M_NB_VCCAX M	=PP1V05_S0M_NB_VCCAXM - @mlb_lib.MLB	6C4 18B3 18C1 21D8
	=PP1V05_S0_NB_FOLLOW - @mlb_lib.MLB	6C4 21C4
	=PPVCORE_S0_SB - @mlb_lib.MLB	6C4 26D3 27B1
	PP1V05_S0 - @mlb_lib.MLB	6C6 7D3 34C3 73A4 73C1
	=PP1V05_S0_NB_PCIE - @mlb_lib.MLB	6C4 21D5
	PP1V05_S0 - @mlb_lib.MLB	6C6 7D3 34C3 73A4 73C1
	=PPVCORE_S0_SB - @mlb_lib.MLB	6C4 26D3 27B1
	=PP1V05_S0_NB_PCIE - @mlb_lib.MLB	6C4 21D5
	=PP1V05_S0_NB_FOLLOW - @mlb_lib.MLB	6C4 21C4
=PP1V05_S0_CPU	=PP1V05_S0_CPU - @mlb_lib.MLB	6D4 10B5 10B6 10C5 10D5 11C6 12A3 13D6 50D2
	=PP1V05_S0_SB_CPU_IO - @mlb_lib.MLB	6C4 23D2 26C3 27B2
	=PPVCORE_S0_NB_FOLLOW - @mlb_lib.MLB	6D4 21B4
	PPMCH_CORE_S0 - @mlb_lib.MLB	6D6 7D3 55A6 73A2 74C1
	=PP1V25R1V05_S0_NB_VTT - @mlb_lib.MLB	6D4 19D3 21C8
	=PP1V25R1V05_S0_FSB_NB - @mlb_lib.MLB	6D4 14B7 30B8 30C8 30C8
	=PPVCORE_S0_NB - @mlb_lib.MLB	6D4 18D3 18D7 21D8
	=PP1V25R1V05_S0_NB_VTT - @mlb_lib.MLB	6D4 19D3 21C8
	=PP1V25R1V05_S0_FSB_NB - @mlb_lib.MLB	6D4 14B7 30B8 30C8 30C8
	=PP1V05_S0_SB_CPU_IO - @mlb_lib.MLB	6C4 23D2 26C3 27B2
=PP1V5_S0_CPU	=PP1V5_S0_CPU - @mlb_lib.MLB	6C4 11B6 12B3
	=PP1V5_S0_MINI - @mlb_lib.MLB	6C4 34C2
	PP1V5_S0 - @mlb_lib.MLB	6C6 7D3 73C8
	=PP1V5_S0_SB - @mlb_lib.MLB	6C4 27C8
	PP1V5_S0_SB_VCCGLANPLL - @mlb_lib.MLB	26A6 27B6
	=PP1V5_S0_SB_VCC1_5_A - @mlb_lib.MLB	6C4 26B6
	=PP1V5_S0_SB_VCCUSBPLL - @mlb_lib.MLB	6C4 26A6 27C2
	=PP1V5_S0_SB_VCC1_5_A_USB_CORE - @mlb_lib.MLB	6C4 26B6 27C2
	=PP1V5_S0_SB_VCC1_5_A_ATX - @mlb_lib.MLB	6C4 26B6 27D2
	=PP1V5_S0_SB_VCC1_5_A_ARX - @mlb_lib.MLB	6C4 26B6 27D2
	=PP1V5_S0_NB_TVDAC - @mlb_lib.MLB	6C4 22B3
	PP1V5_S0 - @mlb_lib.MLB	6C6 7D3 73C8
	=PP1V5_S0_SB_VCCUSBPLL - @mlb_lib.MLB	6C4 26A6 27C2
	=PP1V5_S0_SB_VCC1_5_A_USB_CORE - @mlb_lib.MLB	6C4 26B6 27C2
	=PP1V5_S0_SB_VCC1_5_A_ATX - @mlb_lib.MLB	6C4 26B6 27D2
	=PP1V5_S0_SB_VCC1_5_A_ARX - @mlb_lib.MLB	6C4 26B6 27D2
	=PP1V5_S0_SB_VCC1_5_A - @mlb_lib.MLB	6C4 26B6
	=PP1V5_S0_SB - @mlb_lib.MLB	6C4 27C8
	=PP1V5_S0_NB_TVDAC - @mlb_lib.MLB	6C4 22B3
	=PP1V5_S0_MINI - @mlb_lib.MLB	6C4 34C2
=PP1V5_S0_SB_VCCGLAN 1_5	=PP1V5_S0_SB_VCCGLAN1_5 - @mlb_lib.MLB	26A6 27B6
	PP1V5_S0_SB_VCC1_5_B - @mlb_lib.MLB	23D7 24C2 26D6 27C6
=PP1V8_S0_MXM	=PP1V8_S0_MXM - @mlb_lib.MLB	6D4 84C8
	PP1V8_S0 - @mlb_lib.MLB	6D6 7D3 70D8 78B5
=PP1V8_S3M_MEM_NB	=PP1V8_S3M_MEM_NB - @mlb_lib.MLB	6D3 16D2 18D7 21C8 22B3
	=PP1V8_S3M_NB_VCC - @mlb_lib.MLB	6D3 21A4
	=PP1V8_S3_ENET - @mlb_lib.MLB	6D3 38B7
	PP1V8_S3 - @mlb_lib.MLB	6D4 7D3 75B3 75C1 78C6
	=PP1V8_S3_MEMVTT - @mlb_lib.MLB	6D3 75B6
	=PP1V8_S3_MEM - @mlb_lib.MLB	6D3 31B2 31D2 31D3 31D6 32B2 32D2 32D3 32D6
	PP1V8_S3 - @mlb_lib.MLB	6D4 7D3 75B3 75C1 78C6
	=PP1V8_S3_MEMVTT - @mlb_lib.MLB	6D3 75B6
	=PP1V8_S3_MEM - @mlb_lib.MLB	6D3 31B2 31D2 31D3 31D6 32B2 32D2 32D3 32D6
	=PP1V8_S3_ENET - @mlb_lib.MLB	6D3 38B7
	=PP1V8_S3M_NB_VCC - @mlb_lib.MLB	6D3 21A4
=PP1V25_S0M_NB_PLL	=PP1V25_S0M_NB_PLL - @mlb_lib.MLB	6C4 21D3
	=PP1V25_S0M_NB_VCCD_HPLL - @mlb_lib.MLB	19A6 21D1
	=PP1V25_S0_SB_DMI - @mlb_lib.MLB	6C4 26C3 27C1
	PP1V25_S0 - @mlb_lib.MLB	6C6 7D3 74C8
	=PP1V25_S0_NB_VCC - @mlb_lib.MLB	6C4 21D5
	=PP1V25_S0_NB_PLL - @mlb_lib.MLB	6C4 21B4
	=PP1V25_S0M_NB_VCC - @mlb_lib.MLB	6C4 21A8
	=PP1V25_S0M_NB_VCCA - @mlb_lib.MLB	6C4 21B8
	=PP1V25_S0_NB_VCCDMI - @mlb_lib.MLB	6C4 19C3 21A8
=PP2V5_S0_MXM	=PP2V5_S0_MXM - @mlb_lib.MLB	6D4 85A3
	PP2V5_S0 - @mlb_lib.MLB	6D6 7D3 77B4
=PP3V3_ENET_PHY	=PP3V3_ENET_PHY - @mlb_lib.MLB	37D6 38D6
	=PP3V3_S3_ENET - @mlb_lib.MLB	6D3 38C7 39A8
	=PP3V3_S3_BT - @mlb_lib.MLB	6D3 47D3
	=PP3V3_S3_MINI - @mlb_lib.MLB	6D3 34D2
	PP3V3_S3 - @mlb_lib.MLB	6A7 6D4 7C6 7D3 70D2 75D7 76B8 78C4
	=PP3V3_S3_MINI - @mlb_lib.MLB	6D3 34D2
	=PP3V3_S3_ENET - @mlb_lib.MLB	6D3 38C7 39A8
	=PP3V3_S3_BT - @mlb_lib.MLB	6D3 47D3
=PP3V3_S5_FAN	=PP3V3_S5_FAN - @mlb_lib.MLB	6D1 56B7 56D7 57D7
	=PP3V3_S5_SMBUS_SMC_A_S5 - @mlb_lib.MLB	6D1 52D3
	PP3V3_S5 - @mlb_lib.MLB	6A8 6D2 7C3 70B3 70C7 70D3 75D8 77D3
	=PP3V3_S5_SMCUSBMUX - @mlb_lib.MLB	6D1 46D5
	=PP3V3_S5_SMBUS_SMC_BSA - @mlb_lib.MLB	6D1 52C3
	=PP3V3_S5_LPCPLUS - @mlb_lib.MLB	6D1 7D4 51C6
	=PP3V3_S5_SB_3V3_VCCSUSHDA - @mlb_lib.MLB	6D1 26B3 27B4
	=PP3V3_S5_SB_CLINK1 - @mlb_lib.MLB	6D1 25B1
	=PP3V3_S5_SB_GPIO - @mlb_lib.MLB	6D1 25D8
	=PP3V3_S5_ROM - @mlb_lib.MLB	6D1 61C6
	=PP3V3_S5_SMC - @mlb_lib.MLB	6D1 49D4 50B1 50D7
	=PP3V3_S5_FW - @mlb_lib.MLB	6D1 40C2 40D3 40D4 42B3 42B6 42B8 42C8 42D3 43A8
	=PP3V3_S5_SMBUS_SB_ME - @mlb_lib.MLB	6D1 52A8
	=PP3V3_S5_SB_VCCSUS3_3_USB - @mlb_lib.MLB	6D1 26A3 27C5
	=PP3V3_S5_SB_VCCSUS3_3 - @mlb_lib.MLB	6D1 26A3 27D5
	=PP3V3_S5_SB_USB - @mlb_lib.MLB	6D1 24C8
	=PP3V3_S5_SB_PM - @mlb_lib.MLB	6D1 28A5
	=PP3V3_S5_SB_GPIO - @mlb_lib.MLB	6D1 25D8
	=PP3V3_S5_SB_CLINK1 - @mlb_lib.MLB	6D1 25B1
	=PP3V3_S5_SB_3V3_VCCSUSHDA - @mlb_lib.MLB	6D1 26B3 27B4
	=PP3V3_S5_SB - @mlb_lib.MLB	6D1 25A3 25A8 27D8 28D7
	=PP3V3_S5_ROM - @mlb_lib.MLB	6D1 61C6
	=PP3V3_S5_LPCPLUS - @mlb_lib.MLB	6D1 7D4 51C6
	=PP3V3_S5_FW - @mlb_lib.MLB	6D1 40C2 40D3 40D4 42B3 42B6 42B8 42C8 42D3 43A8
=PP5V_S0_AUDIO	=PP5V_S0_AUDIO - @mlb_lib.MLB	6A4 98C4 98C6
	=PP5V_S0_MXM - @mlb_lib.MLB	6A4 84C8
	=PPV_S0_LCD_20INCH - @mlb_lib.MLB	6A4 90C8
	PP5V_S0 - @mlb_lib.MLB	6A6 7D3 70C8 71D8 72D7 73C7 74C7 78D1 94D6
	=PP5V_S0_SATA - @mlb_lib.MLB	6A4 6D6
	=PP5V_S0_LPCPLUS - @mlb_lib.MLB	6A4 7D4 51C6
	=PP5V_S0_PATA - @mlb_lib.MLB	6A4 44B6 44D6
	=PP5V_S0_SB - @mlb_lib.MLB	6A4 27D8
	PP5V_S0 - @mlb_lib.MLB	6A6 7D3 70C8 71D8 72D7 73C7 74C7 78D1 94D6
	=PPV_S0_LCD_20INCH - @mlb_lib.MLB	6A4 90C8
	=PP5V_S0_SB - @mlb_lib.MLB	6A4 27D8
	=PP5V_S0_PATA - @mlb_lib.MLB	6A4 44B6 44D6
	=PP5V_S0_MXM - @mlb_lib.MLB	6A4 84C8
	=PP5V_S0_LPCPLUS - @mlb_lib.MLB	6A4 7D4 51C6
=PP5V_S3_BNDI	=PP5V_S3_BNDI - @mlb_lib.MLB	6C3 47A3 47D7
	=PP5V_S3_MEMVTT - @mlb_lib.MLB	6C3 75B6
	PP5V_S3 - @mlb_lib.MLB	6C4 7D3 70D3 75D8 76A8 78D5
	=PP5V_S3_MEMVTT - @mlb_lib.MLB	6C3 75B6
=PP5V_S5_SB	=PP5V_S5_SB - @mlb_lib.MLB	6C1 27D8
	=PP5V_S5_USB - @mlb_lib.MLB	6C1 46C8 46D8
	PP5V_S5 - @mlb_lib.MLB	6C2 7C3 70A7 70D8 76A8 76B1 76B5 76D8 77D6 78C7 78D4 78D7
	=PPVIN_S5_SMCVREF - @mlb_lib.MLB	6C1 50B8
	PP5V_S5 - @mlb_lib.MLB	6C2 7C3 70A7 70D8 76A8 76B1 76B5 76D8 77D6 78C7 78D4 78D7
	=PPVIN_S5_SMCVREF - @mlb_lib.MLB	6C1 50B8
	=PP5V_S5_USB - @mlb_lib.MLB	6C1 46C8 46D8
=PP12V_S0_AUDIO_SPKR AMP	=PP12V_S0_AUDIO_SPKRAMP - @mlb_lib.MLB	6A4 98C6
	=PP12V_S0_CPU - @mlb_lib.MLB	6A4 53B8 71D8 72D7
	=PPV_S0_LCD_24INCH - @mlb_lib.MLB	6A4 90C8
	=PPV_S0_MXM_PWRSRC - @mlb_lib.MLB	6A4 53D4
	P12V_S0 - @mlb_lib.MLB	6A6 7D3 53B3 53B4 73D7 74D7 76D8
	=PP12V_S0_FAN - @mlb_lib.MLB	6A4 56B6 56D7 57D6
	P12V_S0 - @mlb_lib.MLB	6A6 7D3 53B3 53B4 73D7 74D7 76D8
	=PPV_S0_MXM_PWRSRC - @mlb_lib.MLB	6A4 53D4
	=PPV_S0_LCD_24INCH - @mlb_lib.MLB	6A4 90C8
	=PP12V_S0_FAN - @mlb_lib.MLB	6A4 56B6 56D7 57D6
	=PP12V_S0_CPU - @mlb_lib.MLB	6A4 53B8 71D8 72D7
=PP12V_S5_FET	=PP12V_S5_FET - @mlb_lib.MLB	6C1
	PP12V_S5 - @mlb_lib.MLB	6C2 7C3 53B5 53C4 70D8 75D8 76A8 76D5 76D8
	=PP12V_S5_FW - @mlb_lib.MLB	6C1 43D8
	PP12V_S5 - @mlb_lib.MLB	6C2 7C3 53B5 53C4 70D8 75D8 76A8 76D5 76D8
=PPVCORE_S0_CPU	=PPVCORE_S0_CPU - @mlb_lib.MLB	6D4 11B5 11D6 12D7 53B6 53D8
	PPVCORE_CPU - @mlb_lib.MLB	6D6 7D3 71D1 72C1
=SB_CLINK_MPWROK	=SB_CLINK_MPWROK - @mlb_lib.MLB	25C3 28B7
	PM_SB_PWROK - @mlb_lib.MLB	7C4 7C4 25C3 28B6 70C1
=SMC_SMS_INT	=SMC_SMS_INT - @mlb_lib.MLB	49B5 50B2
	SMC_SMS_INT - @mlb_lib.MLB	50B2
ACDC_TEMP	ACDC_TEMP - @mlb_lib.MLB	6D6 50C2
	SMC_ANALOG_ID - @mlb_lib.MLB	49A8 50C3
ALL_SYS_PWRGD	ALL_SYS_PWRGD - @mlb_lib.MLB	7C4 7C4 49D8 50C2 70C1 84C7
	PM_LAN_PWRGD - @mlb_lib.MLB	49C5 50C3
ALS_GAIN	ALS_GAIN - @mlb_lib.MLB	49A5 50D5
	NC_ALS_GAIN - @mlb_lib.MLB	50D3
ALS_LEFT	ALS_LEFT - @mlb_lib.MLB	49A8 50D5
	TP_ALS_LEFT - @mlb_lib.MLB	50D3
ALS_RIGHT	ALS_RIGHT - @mlb_lib.MLB	49A8

8		7		6		5		4		3		2		1
CK505_PCI3_CLK	CK505_PCI3_CLK - @mlb_lib.MLB	29B5 30A5 105D3	DMI_S2N_P<3..1>	DMI_S2N_P<3..1> - @mlb_lib.MLB	101D3	FSB_DINV_L<3>	FSB_DINV_L<3> - @mlb_lib.MLB	7D7 7D8 10B2 14B3 100C3	FW_PORT0_TPB_P	FW_PORT0_TPB_P - @mlb_lib.MLB	43C5 43C6 106D3		
CK505_PCI4_CLK	CK505_PCI4_CLK - @mlb_lib.MLB	29B5 30A5 105D3	DMI_S2N_P<2>	DMI_S2N_P<2> - @mlb_lib.MLB	16B3 24D2	FSB_DPWR_L	FSB_DPWR_L - @mlb_lib.MLB	7C7 10B2 14B3 100D3		FW_P0_TPB_P - @mlb_lib.MLB	40C6 43C8		
	TP_CK505_PCI4_CLK - @mlb_lib.MLB	30A3	DMI_S2N_P<3>	DMI_S2N_P<3> - @mlb_lib.MLB	16B3 24D2	FSB_DRDY_L	FSB_DRDY_L - @mlb_lib.MLB	10D6 14B3 100D3	FW_PORT0_VP	FW_PORT0_VP - @mlb_lib.MLB	43D3		
CK505_PCI5_CLK_FCTSE	CK505_PCI5_CLK_FCTSEL -	29B5 30D8 105D3	DVI_DDC_CLK	DVI_DDC_CLK - @mlb_lib.MLB	94D2	FSB_DSTB_L_N<0>	FSB_DSTB_L_N<0> - @mlb_lib.MLB	7D7 7D8 10C4 14B3 100C3	FW_PORT0_VP_F	FW_PORT0_VP_F - @mlb_lib.MLB	43D5		
L	@mlb_lib.MLB		DVI_DDC_CLK_UF	DVI_DDC_CLK_UF - @mlb_lib.MLB	94D3 94D5	FSB_DSTB_L_N<1>	FSB_DSTB_L_N<1> - @mlb_lib.MLB	7D7 7D8 10B4 14B3 100C3	FW_PORT1_TPA_FL_N	FW_PORT1_TPA_FL_N - @mlb_lib.MLB	43B2 106D3		
CK505_PCIF0_CLK_ITPE	CK505_PCIF0_CLK_ITPEN -	29B7 30A5 105D3	DVI_DDC_DATA	DVI_DDC_DATA - @mlb_lib.MLB	94C2	FSB_DSTB_L_N<2>	FSB_DSTB_L_N<2> - @mlb_lib.MLB	7D7 7D8 10C2 14B3 100C3	FW_PORT1_TPA_FL_P	FW_PORT1_TPA_FL_P - @mlb_lib.MLB	43B2 106D3		
N	@mlb_lib.MLB		DVI_DDC_DATA_UF	DVI_DDC_DATA_UF - @mlb_lib.MLB	94C3 94D5	FSB_DSTB_L_N<3>	FSB_DSTB_L_N<3> - @mlb_lib.MLB	7D7 7D8 10B2 14B3 100C3	FW_PORT1_TPA_N	FW_PORT1_TPA_N - @mlb_lib.MLB	43B6 43C6 106D3		
CK505_PCIF1_CLK	CK505_PCIF1_CLK - @mlb_lib.MLB	29B5 30A5 105D3	DVI_HOTPLUG_DET	DVI_HOTPLUG_DET - @mlb_lib.MLB	24A6 28B2	FSB_DSTB_L_P<0>	FSB_DSTB_L_P<0> - @mlb_lib.MLB	7D7 7D8 10C4 14B3 100D3		FW_P1_TPA_N - @mlb_lib.MLB	40C6 43C8		
CK505_REF0_FSC	CK505_REF0_FSC - @mlb_lib.MLB	29A3 30A8 105D3		SB_GPIO4 - @mlb_lib.MLB	28B2	FSB_DSTB_L_P<1>	FSB_DSTB_L_P<1> - @mlb_lib.MLB	7D7 7D8 10B4 14B3 100C3	FW_PORT1_TPA_P	FW_PORT1_TPA_P - @mlb_lib.MLB	43B6 43C6 106D3		
CK505_REF1	CK505_REF1 - @mlb_lib.MLB	29A3 30B2	DVI_HPD_UF	DVI_HPD_UF - @mlb_lib.MLB	94C3 94D5	FSB_DSTB_L_P<2>	FSB_DSTB_L_P<2> - @mlb_lib.MLB	7D7 7D8 10C2 14A3 100C3		FW_P1_TPA_P - @mlb_lib.MLB	40C6 43C8		
	TP_CK505_REF1 - @mlb_lib.MLB	7C3 30B1	ENET_CLK25M_XTALI	ENET_CLK25M_XTALI - @mlb_lib.MLB	37B4	FSB_DSTB_L_P<3>	FSB_DSTB_L_P<3> - @mlb_lib.MLB	7D7 7D8 10B2 14A3 100C3	FW_PORT1_TPB_FL_N	FW_PORT1_TPB_FL_N - @mlb_lib.MLB	43B2 106D3		
CK505_SRC1_N	CK505_SRC1_N - @mlb_lib.MLB	29B3 30C5 105C3	ENET_CLK25M_XTALO	ENET_CLK25M_XTALO - @mlb_lib.MLB	37B4	FSB_D_L<0>	FSB_D_L<0> - @mlb_lib.MLB	7D7 7D8 10C4 14D5 100D3	FW_PORT1_TPB_FL_P	FW_PORT1_TPB_FL_P - @mlb_lib.MLB	43B2 106D3		
	GPU_CLK100M_PCIE_N - @mlb_lib.MLB	30C3 85C7 105B3	ENET_CTAP_<0>	ENET_CTAP_<0> - @mlb_lib.MLB	39B5	FSB_D_L<1>	FSB_D_L<1> - @mlb_lib.MLB	10C4 14D5	FW_PORT1_TPB_N	FW_PORT1_TPB_N - @mlb_lib.MLB	43A6 43C6 106D3		
CK505_SRC1_P	CK505_SRC1_P - @mlb_lib.MLB	29B3 30C5 105C3	ENET_CTAP_<1>	ENET_CTAP_<1> - @mlb_lib.MLB	39B5	FSB_D_L<15..1>	FSB_D_L<15..1> - @mlb_lib.MLB	100D3		FW_P1_TPB_N - @mlb_lib.MLB	40C6 43C8		
	GPU_CLK100M_PCIE_P - @mlb_lib.MLB	30C3 85C7 105B3	ENET_CTAP_<2>	ENET_CTAP_<2> - @mlb_lib.MLB	39B5	FSB_D_L<2>	FSB_D_L<2> - @mlb_lib.MLB	10C4 14D5	FW_PORT1_TPB_P	FW_PORT1_TPB_P - @mlb_lib.MLB	43B6 43C6 106D3		
CK505_SRC2_N	CK505_SRC2_N - @mlb_lib.MLB	29B3 30C5 105C3	ENET_CTAP_<3>	ENET_CTAP_<3> - @mlb_lib.MLB	39B5	FSB_D_L<3>	FSB_D_L<3> - @mlb_lib.MLB	10C4 14D5		FW_P1_TPB_P - @mlb_lib.MLB	40C6 43C8		
	SB_CLK100M_DMI_N - @mlb_lib.MLB	7B8 7C3 24D2 30C3 105B3	ENET_CTAP_COMMON	ENET_CTAP_COMMON - @mlb_lib.MLB	39A4	FSB_D_L<4>	FSB_D_L<4> - @mlb_lib.MLB	10C4 14D5	FW_PORT1_VP	FW_PORT1_VP - @mlb_lib.MLB	43B3		
CK505_SRC2_P	CK505_SRC2_P - @mlb_lib.MLB	29B3 30C5 105C3	ENET_CTRL12	ENET_CTRL12 - @mlb_lib.MLB	38A5 38B1	FSB_D_L<5>	FSB_D_L<5> - @mlb_lib.MLB	10C4 14D5	FW_PORT1_VP_F	FW_PORT1_VP_F - @mlb_lib.MLB	43D5		
	SB_CLK100M_DMI_P - @mlb_lib.MLB	7B8 24C2 30C3 105B3		TP_YUKON_CTRL12 - @mlb_lib.MLB	37C2 38B3	FSB_D_L<6>	FSB_D_L<6> - @mlb_lib.MLB	10C4 14D5	FW_PORTS_VP	FW_PORTS_VP - @mlb_lib.MLB	43D7		
CK505_SRC3_N	CK505_SRC3_N - @mlb_lib.MLB	29B3 30C5 105C3	ENET_CTRL19	ENET_CTRL19 - @mlb_lib.MLB	38B1 38C5	FSB_D_L<7>	FSB_D_L<7> - @mlb_lib.MLB	10C4 14D5	FW_PORTS_VP_R	FW_PORTS_VP_R - @mlb_lib.MLB	40C7 43D6		
	PCIE_CLK100M_FW_N - @mlb_lib.MLB	7D6 30C3 40C3 105B3		TP_YUKON_CTRL18 - @mlb_lib.MLB	37C2 38B3	FSB_D_L<8>	FSB_D_L<8> - @mlb_lib.MLB	10C4 14D5	FW_PU_RST_L	FW_PU_RST_L - @mlb_lib.MLB	40B6		
CK505_SRC3_P	CK505_SRC3_P - @mlb_lib.MLB	29B3 30C5 105C3	ENET_LED_ACT_L	ENET_LED_ACT_L - @mlb_lib.MLB	37B2 39A8	FSB_D_L<9>	FSB_D_L<9> - @mlb_lib.MLB	10C4 14D5	FW_R0	FW_R0 - @mlb_lib.MLB	40B6		
	PCIE_CLK100M_FW_P - @mlb_lib.MLB	7D6 30C3 40C3 105B3	ENET_LED_LINK10_100_	ENET_LED_LINK10_100_L -	37B2 39A8	FSB_D_L<10>	FSB_D_L<10> - @mlb_lib.MLB	10C4 14D5	FW_RESET_L	FW_RESET_L - @mlb_lib.MLB	7D6 28C1 40B3		
CK505_SRC4_N	CK505_SRC4_N - @mlb_lib.MLB	29B3 30B5 105C3	L	@mlb_lib.MLB		FSB_D_L<11>	FSB_D_L<11> - @mlb_lib.MLB	10C4 14D5	FW_REXT	FW_REXT - @mlb_lib.MLB	40B6		
	SB_CLK100M_SATA_N - @mlb_lib.MLB	7C8 23B6 30B3 105B3	ENET_LED_LINK1000_L	ENET_LED_LINK1000_L - @mlb_lib.MLB	37B2 39A8	FSB_D_L<12>	FSB_D_L<12> - @mlb_lib.MLB	10C4 14D5	FW_SCL	FW_SCL - @mlb_lib.MLB	40B3		
CK505_SRC4_P	CK505_SRC4_P - @mlb_lib.MLB	29B3 30B5 105C3	ENET_LED_LINK_L	ENET_LED_LINK_L - @mlb_lib.MLB	37B2 39A8	FSB_D_L<13>	FSB_D_L<13> - @mlb_lib.MLB	10C4 14C5	FW_TPCPS	FW_TPCPS - @mlb_lib.MLB	40B6		
	SB_CLK100M_SATA_P - @mlb_lib.MLB	7C8 23B6 30B3 105B3	ENET_LOM_DIS_L	ENET_LOM_DIS_L - @mlb_lib.MLB	37C2	FSB_D_L<14>	FSB_D_L<14> - @mlb_lib.MLB	10C4 14C5	FW_TRST_L	FW_TRST_L - @mlb_lib.MLB	7C3 40C3		
CK505_SRC5_N	CK505_SRC5_N - @mlb_lib.MLB	29B3 30B5 105C3	ENET_MDI0	ENET_MDI0 - @mlb_lib.MLB	37B7 104B3	FSB_D_L<15>	FSB_D_L<15> - @mlb_lib.MLB	10C4 14C5	FW_VAUX_DETECT	FW_VAUX_DETECT - @mlb_lib.MLB	40C3		
	NB_CLK100M_PCIE_N - @mlb_lib.MLB	7C3 7C7 16C3 30B3 105B3	ENET_MDI1	ENET_MDI1 - @mlb_lib.MLB	37B6 104B3	FSB_D_L<16>	FSB_D_L<16> - @mlb_lib.MLB	7D7 7D8 10C4 14C5 100C3	FW_XI	FW_XI - @mlb_lib.MLB	40B6		
CK505_SRC5_P	CK505_SRC5_P - @mlb_lib.MLB	29B3 30B5 105C3	ENET_MDI2	ENET_MDI2 - @mlb_lib.MLB	37B6 104B3	FSB_D_L<17>	FSB_D_L<17> - @mlb_lib.MLB	10C4 14C5	FW_XO	FW_XO - @mlb_lib.MLB	40B6		
	NB_CLK100M_PCIE_P - @mlb_lib.MLB	7C7 16C3 30B3 105B3	ENET_MDI3	ENET_MDI3 - @mlb_lib.MLB	37B5 104B3	FSB_D_L<31..17>	FSB_D_L<31..17> - @mlb_lib.MLB	100C3	FW_XO_R	FW_XO_R - @mlb_lib.MLB	40B7		
CK505_SRC6_N	CK505_SRC6_N - @mlb_lib.MLB	29B3 30B5 105C3	ENET_MDI_N<0>	ENET_MDI_N<0> - @mlb_lib.MLB	37B8 39C7 104B3	FSB_D_L<18>	FSB_D_L<18> - @mlb_lib.MLB	10C4 14C5	GFX_VID<1>	GFX_VID<1> - @mlb_lib.MLB	16B3 22B8		
	PCIE_CLK100M_MINI_N - @mlb_lib.MLB	30B3 34C6 105B3	ENET_MDI_N<1>	ENET_MDI_N<1> - @mlb_lib.MLB	37B8 39C7 104B3	FSB_D_L<19>	FSB_D_L<19> - @mlb_lib.MLB	10B4 14C5	GFX_VID<2>	GFX_VID<2> - @mlb_lib.MLB	16B3 22A8		
CK505_SRC6_P	CK505_SRC6_P - @mlb_lib.MLB	29B3 30B5 105C3	ENET_MDI_N<2>	ENET_MDI_N<2> - @mlb_lib.MLB	37B8 39B7 104A3	FSB_D_L<20>	FSB_D_L<20> - @mlb_lib.MLB	10B4 14C5	GFX_VID<3>	GFX_VID<3> - @mlb_lib.MLB	16B3 22A8		
	PCIE_CLK100M_MINI_P - @mlb_lib.MLB	30B3 34C6 105B3	ENET_MDI_N<3>	ENET_MDI_N<3> - @mlb_lib.MLB	37B8 39B7 104A3	FSB_D_L<21>	FSB_D_L<21> - @mlb_lib.MLB	10B4 14C5	GFX_VID<4>	GFX_VID<4> - @mlb_lib.MLB	16B3 22A8		
CK505_SRC7_N	CK505_SRC7_N - @mlb_lib.MLB	29B3 30B5 105C3	ENET_MDI_P<0>	ENET_MDI_P<0> - @mlb_lib.MLB	37B8 39C7 104B3	FSB_D_L<22>	FSB_D_L<22> - @mlb_lib.MLB	10B4 14C5	GLAN_COMP	GLAN_COMP - @mlb_lib.MLB	23C6 104B3		
CK505_SRC7_P	CK505_SRC7_P - @mlb_lib.MLB	29B3 30B5 105C3	ENET_MDI_P<1>	ENET_MDI_P<1> - @mlb_lib.MLB	37B8 39C7 104B3	FSB_D_L<23>	FSB_D_L<23> - @mlb_lib.MLB	10B4 14C5	GND_IMVP6_SGND	GND_IMVP6_SGND - @mlb_lib.MLB	71B6		
CK505_SRC8_N	CK505_SRC8_N - @mlb_lib.MLB	29B3 30B5 105C3	ENET_MDI_P<2>	ENET_MDI_P<2> - @mlb_lib.MLB	37B8 39B7 104B3	FSB_D_L<24>	FSB_D_L<24> - @mlb_lib.MLB	10B4 14C5	GND_PP1V5REG_SGND	GND_PP1V5REG_SGND - @mlb_lib.MLB	73B7		
	PCIE_CLK100M_ENET_N - @mlb_lib.MLB	7D6 30B3 37C8 105B3	ENET_MDI_P<3>	ENET_MDI_P<3> - @mlb_lib.MLB	37B8 39B7 104A3	FSB_D_L<25>	FSB_D_L<25> - @mlb_lib.MLB	10B4 14C5	GND_PP1V8REG_SGND	GND_PP1V8REG_SGND - @mlb_lib.MLB	75C5 75D6		
CK505_SRC8_P	CK505_SRC8_P - @mlb_lib.MLB	29A3 30B5 105C3	ENET_MDI_R_N<0>	ENET_MDI_R_N<0> - @mlb_lib.MLB	108B3	FSB_D_L<26>	FSB_D_L<26> - @mlb_lib.MLB	10B4 14C5	GND_PP1V25REG_SGND	GND_PP1V25REG_SGND - @mlb_lib.MLB	74B7		
	PCIE_CLK100M_ENET_P - @mlb_lib.MLB	7D6 30B3 37C8 105B3	ENET_MDI_R_N<1>	ENET_MDI_R_N<1> - @mlb_lib.MLB	108B3	FSB_D_L<27>	FSB_D_L<27> - @mlb_lib.MLB	10B4 14C5	GND_PP5VREG_SGND	GND_PP5VREG_SGND - @mlb_lib.MLB	76A7		
CK505_XTAL_IN	CK505_XTAL_IN - @mlb_lib.MLB	29C5	ENET_MDI_R_N<2>	ENET_MDI_R_N<2> - @mlb_lib.MLB	108B3	FSB_D_L<28>	FSB_D_L<28> - @mlb_lib.MLB	10B4 14C5	GND_SMC_AVSS	GND_SMC_AVSS - @mlb_lib.MLB	49B2 50B7 53A2 53A3 53B1		
CK505_XTAL_OUT	CK505_XTAL_OUT - @mlb_lib.MLB	29C5	ENET_MDI_R_N<3>	ENET_MDI_R_N<3> - @mlb_lib.MLB	108B3	FSB_D_L<29>	FSB_D_L<29> - @mlb_lib.MLB	10B4 14C5			53C3 53C6 53D3 53D6		
CLINK_NB_CLK	CLINK_NB_CLK - @mlb_lib.MLB	7A7 7A8 16A3 25C3 104B3	ENET_MDI_R_P<0>	ENET_MDI_R_P<0> - @mlb_lib.MLB	108B3	FSB_D_L<30>	FSB_D_L<30> - @mlb_lib.MLB	10B4 14C5	GPU_BLU	GPU_BLU - @mlb_lib.MLB	85C4 91B8 108B3		
CLINK_NB_DATA	CLINK_NB_DATA - @mlb_lib.MLB	7A7 7A8 16A3 25C3 104B3	ENET_MDI_R_P<1>	ENET_MDI_R_P<1> - @mlb_lib.MLB	108B3	FSB_D_L<31>	FSB_D_L<31> - @mlb_lib.MLB	10B4 14C5	GPU_BUF_HSYNC	GPU_BUF_HSYNC - @mlb_lib.MLB	108A3		
CLINK_NB_RESET_L	CLINK_NB_RESET_L - @mlb_lib.MLB	16A3 25C3 104B3	ENET_MDI_R_P<2>	ENET_MDI_R_P<2> - @mlb_lib.MLB	108B3	FSB_D_L<32>	FSB_D_L<32> - @mlb_lib.MLB	10C2 14C5	GPU_BUF_VSYNC	GPU_BUF_VSYNC - @mlb_lib.MLB	108A3		
CLINK_WLAN_CLK	CLINK_WLAN_CLK - @mlb_lib.MLB	34A8	ENET_MDI_R_P<3>	ENET_MDI_R_P<3> - @mlb_lib.MLB	108B3	FSB_D_L<40..32>	FSB_D_L<40..32> - @mlb_lib.MLB	100C3	GPU_DDC_A_CLK	GPU_DDC_A_CLK - @mlb_lib.MLB	85C7 94D1		
	TP_CLINK_WLAN_CLK - @mlb_lib.MLB	25C3 34A6	ENET_MDI_T_N<0>	ENET_MDI_T_N<0> - @mlb_lib.MLB	39C5 108B3	FSB_D_L<33>	FSB_D_L<33> - @mlb_lib.MLB	10C2 14C5	GPU_DDC_A_DATA	GPU_DDC_A_DATA - @mlb_lib.MLB	85C7 94C1		
CLINK_WLAN_DATA	CLINK_WLAN_DATA - @mlb_lib.MLB	34A8	ENET_MDI_T_N<1>	ENET_MDI_T_N<1> - @mlb_lib.MLB	39C5 108B3	FSB_D_L<34>	FSB_D_L<34> - @mlb_lib.MLB	10C2 14C5	GPU_DDC_C_CLK	GPU_DDC_C_CLK - @mlb_lib.MLB	85A4 85D1 90A8		
	TP_CLINK_WLAN_DATA - @mlb_lib.MLB	25C3 28C4 34A6	ENET_MDI_T_N<2>	ENET_MDI_T_N<2> - @mlb_lib.MLB	39B5 108B3	FSB_D_L<35>	FSB_D_L<35> - @mlb_lib.MLB	10C2 14C5	GPU_DDC_C_DATA	GPU_DDC_C_DATA - @mlb_lib.MLB	85A4 85D1 90A6		
CLINK_WLAN_RESET_L	CLINK_WLAN_RESET_L - @mlb_lib.MLB	34A8	ENET_MDI_T_N<3>	ENET_MDI_T_N<3> - @mlb_lib.MLB	39B5 108B3	FSB_D_L<36>	FSB_D_L<36> - @mlb_lib.MLB	10C2 14C5	GPU_DIGON	GPU_DIGON - @mlb_lib.MLB	85A4 90B8		
	TP_CLINK_WLAN_RESET_L -	25D5 34A6	ENET_MDI_T_P<0>	ENET_MDI_T_P<0> - @mlb_lib.MLB	39C5 108B3	FSB_D_L<37>	FSB_D_L<37> - @mlb_lib.MLB	10C2 14C5	GPU_ENABLE_BL	GPU_ENABLE_BL - @mlb_lib.MLB	85A5		
	@mlb_lib.MLB		ENET_MDI_T_P<1>	ENET_MDI_T_P<1> - @mlb_lib.MLB	39C5 108B3	FSB_D_L<38>	FSB_D_L<38> - @mlb_lib.MLB	10C2 14C5	GPU_GRN	GPU_GRN - @mlb_lib.MLB	85C4 91B8 108B3		
CLK_PWRGD	CLK_PWRGD - @mlb_lib.MLB	25C3 29A3	ENET_MDI_T_P<2>	ENET_MDI_T_P<2> - @mlb_lib.MLB	39B5 108B3	FSB_D_L<39>	FSB_D_L<39> - @mlb_lib.MLB	10C2 14B5	GPU_H2SYNC	GPU_H2SYNC - @mlb_lib.MLB	85C7 91A4 108B3		
CPUVCORE_ISENSE_CAL	CPUVCORE_ISENSE_CAL - @mlb_lib.MLB	53B6	ENET_MDI_T_P<3>	ENET_MDI_T_P<3> - @mlb_lib.MLB	39B5 108B3	FSB_D_L<40>	FSB_D_L<40> - @mlb_lib.MLB	10C2 14B5	GPU_HPD	GPU_HPD - @mlb_lib.MLB	85A7 94C1		
CPUVSENSE_IN	CPUVSENSE_IN - @mlb_lib.MLB	53D7	ENET_RESET_L	ENET_RESET_L - @mlb_lib.MLB	7D6 28C1 37B8	FSB_D_L<41>	FSB_D_L<41> - @mlb_lib.MLB	7D7 7D8 10C2 14B5 100C3	GPU_HSK_THRMD_N	GPU_HSK_THRMD_N - @mlb_lib.MLB	55A5 55A6 108A3		
CPU_A20M_L	CPU_A20M_L - @mlb_lib.MLB	7C8 10C8 23C4 100B3	EXCARD_OC_L	EXCARD_OC_L - @mlb_lib.MLB	24C8	FSB_D_L<42>	FSB_D_L<42> - @mlb_lib.MLB	10C2 14B5	GPU_HSK_THRMD_P	GPU_HSK_THRMD_P - @mlb_lib.MLB	55A6 55B5 108A3		
CPU_BSEL<0>	CPU_BSEL<0> - @mlb_lib.MLB	10B4 30C6 100B3	EXTGPU_LVDS_EN	EXTGPU_LVDS_EN - @mlb_lib.MLB	13C3 24C8	FSB_D_L<47..42>	FSB_D_L<47..42> - @mlb_lib.MLB	100C3	GPU_HSYNC_BUF	GPU_HSYNC_BUF - @mlb_lib.MLB	91A3		
CPU_BSEL<1>	CPU_BSEL<1> - @mlb_lib.MLB	10A4 30B6 100B3	EXTGPU_PWR_EN	EXTGPU_PWR_EN - @mlb_lib.MLB	23C4 28A2	FSB_D_L<43>	FSB_D_L<43> - @mlb_lib.MLB	10C2 14B5	GPU_PRESENT	GPU_PRESENT - @mlb_lib.MLB	6A8 28C1		
CPU_BSEL<2>	CPU_BSEL<2> - @mlb_lib.MLB	10A4 30B6 100A3		TP_EXTGPU_PWR_EN - @mlb_lib.MLB	28A1	FSB_D_L<44>	FSB_D_L<44> - @mlb_lib.MLB	10C2 14B5		SB_GPIO6 - @mlb_lib.MLB	25A5 25C5 28C2		
CPU_COMP<0>	CPU_COMP<0> - @mlb_lib.MLB	10B3 100A3	EXTGPU_RST_L	EXTGPU_RST_L - @mlb_lib.MLB	25A5 25C5 28A2	FSB_D_L<45>	FSB_D_L<45> - @mlb_lib.MLB	10C2 14B5	GPU_PRESENT_DRAIN	GPU_PRESENT_DRAIN - @mlb_lib.MLB	6B7		
CPU_COMP<1>	CPU_COMP<1> - @mlb_lib.MLB	10B3 100A3		TP_EXTGPU_RST_L - @mlb_lib.MLB	28A1	FSB_D_L<46>	FSB_D_L<46> - @mlb_lib.MLB	10C2 14B5	GPU_PRESENT_R	GPU_PRESENT_R - @mlb_lib.MLB	6B7		
CPU_COMP<2>	CPU_COMP<2> - @mlb_lib.MLB	10B3 100A3	F0_GATESLOWDN	F0_GATESLOWDN - @mlb_lib.MLB	56D5	FSB_D_L<47>	FSB_D_L<47> - @mlb_lib.MLB	10C2 14B5	GPU_RED	GPU_RED - @mlb_lib.MLB	85C4 91B8 108B3		
CPU_COMP<3>	CPU_COMP<3> - @mlb_lib.MLB	10B3 100A3	F0_VOLTAGE8R5	F0_VOLTAGE8R5 - @mlb_lib.MLB	56D6	FSB_D_L<48>	FSB_D_L<48> - @mlb_lib.MLB	10C2 14B5	GPU_TV_C	GPU_TV_C - @mlb_lib.MLB	85C4 91B8 108B3		
CPU_DPRSTP_L	CPU_DPRSTP_L - @mlb_lib.MLB	10B2 16B6 23C4 71C7 100A3	F1_GATESLOWDN	F1_GATESLOWDN - @mlb_lib.MLB	56B5	FSB_D_L<58..48>	FSB_D_L<58..48> - @mlb_lib.MLB	100C3	GPU_TV_COMP	GPU_TV_COMP - @mlb_lib.MLB	85C4 91B8 108B3		
CPU_DPSLP_L	CPU_DPSLP_L - @mlb_lib.MLB	10B2 23C4 100B3	F1_VOLTAGE8R5	F1_VOLTAGE8R5 - @mlb_lib.MLB	56B6	FSB_D_L<49>	FSB_D_L<49> - @mlb_lib.MLB	10C2 14B5	GPU_TV_Y	GPU_TV_Y - @mlb_lib.MLB	85C4 91B8 108B3		
CPU_FERR_L	CPU_FERR_L - @mlb_lib.MLB	10C8 23C2 100B3	F2_GATESLOWDN	F2_GATESLOWDN - @mlb_lib.MLB	57D4	FSB_D_L<50>	FSB_D_L<50> - @mlb_lib.MLB	10C2 14B5	GPU_V2SYNC	GPU_V2SYNC - @mlb_lib.MLB	85C7 91B4 108A3		
CPU_GTLREF	CPU_GTLREF - @mlb_lib.MLB	10B4 100A3	F2_VOLTAGE8R5	F2_VOLTAGE8R5 - @mlb_lib.MLB	57D5	FSB_D_L<51>	FSB_D_L<51> - @mlb_lib.MLB	10B2 14B5	GPU_VARY_BL	GPU_VARY_BL - @mlb_lib.MLB	85A4 90B3		
CPU_HSK_THRMD_N	CPU_HSK_THRMD_N - @mlb_lib.MLB	55A5 55A7 108A3	FAN_0_PWR	FAN_0_PWR - @mlb_lib.MLB	56C4	FSB_D_L<52>	FSB_D_L<52> - @mlb_lib.MLB	10B2 14B5	GPU_VSYNC_BUF	GPU_VSYNC_BUF - @mlb_lib.MLB	91B3		
CPU_HSK_THRMD_P	CPU_HSK_THRMD_P - @mlb_lib.MLB	55A7 55B5 108A3	FAN_1_PWR	FAN_1_PWR - @mlb_lib.MLB	56B3	FSB_D_L<53>	FSB_D_L<53> - @mlb_lib.MLB	10B2 14B5	HDA_BIT_CLK	HDA_BIT_CLK - @mlb_lib.MLB	23C8 98C6 103C3		
CPU_IERR_L	CPU_IERR_L - @mlb_lib.MLB	10D6 100B3	FAN_2_PWR	FAN_2_PWR - @mlb_lib.MLB	57C3	FSB_D_L<54>	FSB_D_L<54> - @mlb_lib.MLB	10B2 14B5	HDA_BIT_CLK_R	HDA_BIT_CLK_R - @mlb_lib.MLB	23C6 103C3		
CPU_IGNNE_L	CPU_IGNNE_L - @mlb_lib.MLB	7C8 10C8 23C4 100B3	FAN_TACH0	FAN_TACH0 - @mlb_lib.MLB	56C7	FSB_D_L<55>	FSB_D_L<55> - @mlb_lib.MLB	10B2 14B5	HDA_DOCK_EN_L	HDA_DOCK_EN_L - @mlb_lib.MLB	23B6		
CPU_INIT_L	CPU_INIT_L - @mlb_lib.MLB	7C8 10D6 23C4 51B2 100B3	FAN_TACH1	FAN_TACH1 - @mlb_lib.MLB	56A7	FSB_D_L<56>	FSB_D_L<56> - @mlb_lib.MLB	10B2 14B5	HDA_RST_L	HDA_RST_L - @mlb_lib.MLB	23C8 98C6 103C3		
CPU_INIT_LS3V3	CPU_INIT_LS3V3 - @mlb_lib.MLB	51C4	FAN_TACH2	FAN_TACH2 - @mlb_lib.MLB	57C7	FSB_D_L<57>	FSB_D_L<57> - @mlb_lib.MLB	10B2 14B5	HDA_RST_L_R	HDA_RST_L_R - @mlb_lib.MLB	23C6 103C3		
CPU_INIT_R_L	CPU_INIT_R_L - @mlb_lib.MLB	51B3	FSB_ADSTB_L<0>	FSB_ADSTB_L<0> - @mlb_lib.MLB	7D7 7D8 10D8 14C3 100C3	FSB_D_L<58>	FSB_D_L<58> - @mlb_lib.MLB	10B2 14B5	HDA_SDIN0	HDA_SDIN0 - @mlb_lib.MLB	23C8 98C6 103B3		
CPU_INTR	CPU_INTR - @mlb_lib.MLB	7C8 10B8 23C4 100B3	FSB_ADSTB_L<1>	FSB_ADSTB_L<1> - @mlb_lib.MLB	7D7 7D8 10C8 14C3 100B3	FSB_D_L<59>	FSB_D_L<59> - @mlb_lib.MLB	7D7 7D8 10B2 14B5 100C3	HDA_SDIN_CODEC	HDA_SDIN_CODEC - @mlb_lib.MLB	103B3		
CPU_NMI	CPU_NMI - @mlb_lib.MLB	7C8 10B8 23C4 100B3	FSB_ADS_L	FSB_ADS_L - @mlb_lib.MLB	10D6 14C3 100D3	FSB_D_L<60>	FSB_D_L<60> - @mlb_lib.MLB	10B2 14B5	HDA_SDOUT	HDA_SDOUT - @mlb_lib.MLB	23B8 98C6 103B3		
CPU_PROCHOT_BUF	CPU_PROCHOT_BUF - @mlb_lib.MLB	50D2	FSB_A_L<3>	FSB_A_L<3> - @mlb_lib.MLB	10D8 14D3	FSB_D_L<63..60>	FSB_D_L<63..60> - @mlb_lib.MLB	100C3	HDA_SDOUT_R	HDA_SDOUT_R - @mlb_lib.MLB	23B6 103B3		
CPU_PROCHOT_L	CPU_PROCHOT_L - @mlb_lib.MLB	10C5 50D3 55D1 100B3	FSB_A_L<5..3>	FSB_A_L<5..3> - @mlb_lib.MLB	100C3	FSB_D_L<61>	FSB_D_L<61> - @mlb_lib.MLB	10B2 14B5	HDA_SYNC	HDA_SYNC - @mlb_lib.MLB	23C8 98C6 103C3		
CPU_PROCHOT_L_R	CPU_PROCHOT_L_R - @mlb_lib.MLB	50D2	FSB_A_L<4>	FSB_A_L<4> - @mlb_lib.MLB	10D8 14D3	FSB_D_L<62>	FSB_D_L<62> - @mlb_lib.MLB	10B2 14B5	HDA_SYNC_R	HDA_SYNC_R - @mlb_lib.MLB	23C6 103C3		
CPU_PSI_L	CPU_PSI_L - @mlb_lib.MLB	10A2 28B7	FSB_A_L<5>	FSB_A_L<5> - @mlb_lib.MLB	10D8 14D3	FSB_D_L<63>	FSB_D_L<63> - @mlb_lib.MLB	10B2 14B5	HDD_THRMD_N	HDD_THRMD_N - @mlb_lib.MLB	55A5 55B7 108A3		
	IMVP6_PSI_L - @mlb_lib.MLB	28B6 71C7	FSB_A_L<6>	FSB_A_L<6> - @mlb_lib.MLB	7D7 7D8 10D8 14D3 100C3	FSB_HITM_L	FSB_HITM_L - @mlb_lib.MLB	7C7 10C6 14B3 100D3	HDD_THRMD_P	HDD_THRMD_P - @mlb_lib.MLB	55B5 55B7 108A3		
CPU_PWRGD	CPU_PWRGD - @mlb_lib.MLB	7C4 10B2 13C7 23C4 100B3	FSB_A_L<7>	FSB_A_L<7> - @mlb_lib.MLB	10D8 14D3	FSB_HIT_L	FSB_HIT_L - @mlb_lib.MLB	7C7 10C6 14B3 100D3	IDE_CSEL	IDE_CSEL - @mlb_lib.MLB	44B5		
CPU_SET_SPEED	CPU_SET_SPEED - @mlb_lib.MLB	25A7 25B3	FSB_A_L<16..7>	FSB_A_L<16..7> - @mlb_lib.MLB	100C3	FSB_LOCK_L	FSB_LOCK_L - @mlb_lib.MLB	7D7 7D8 10D6 14B3 100D3	IDE_DASP_L	IDE_DASP_L - @mlb_lib.MLB	44B5		
CPU_SMI_L	CPU_SMI_L - @mlb_lib.MLB	7C8 10B8 23C4 100B3	FSB_A_L<8>	FSB_A_L<8> - @mlb_lib.MLB	10D8 14D3	FSB_REQ_L<0>	FSB_REQ_L<0> - @mlb_lib.MLB	7C

IMVP6_DFB	IMVP6_DFB - @mlb_lib.MLB	71A8 71B5
IMVP6_DROOP	IMVP6_DROOP - @mlb_lib.MLB	71A8 71B4
IMVP6_FB	IMVP6_FB - @mlb_lib.MLB	71A8 71B7
IMVP6_FCCM	IMVP6_FCCM - @mlb_lib.MLB	71A8 71C5 72C7
IMVP6_FET_RC1	IMVP6_FET_RC1 - @mlb_lib.MLB	71A6 71C3
IMVP6_FET_RC2	IMVP6_FET_RC2 - @mlb_lib.MLB	71A4 71B3
IMVP6_FET_RC3	IMVP6_FET_RC3 - @mlb_lib.MLB	72A7 72C3
IMVP6_ISEN1	IMVP6_ISEN1 - @mlb_lib.MLB	71A6 71C3 72C1
IMVP6_ISEN2	IMVP6_ISEN2 - @mlb_lib.MLB	71A4 71C5
IMVP6_ISEN3	IMVP6_ISEN3 - @mlb_lib.MLB	71C5 72A7 72B1
IMVP6_LGATE1	IMVP6_LGATE1 - @mlb_lib.MLB	71A6 71D4
IMVP6_LGATE2	IMVP6_LGATE2 - @mlb_lib.MLB	71A4 71C4
IMVP6_LGATE3	IMVP6_LGATE3 - @mlb_lib.MLB	72A7 72C6
IMVP6_NTC	IMVP6_NTC - @mlb_lib.MLB	71C7
IMVP6_NTC_R	IMVP6_NTC_R - @mlb_lib.MLB	71C8
IMVP6_OCSET	IMVP6_OCSET - @mlb_lib.MLB	71A8 71B5
IMVP6_PHASE1	IMVP6_PHASE1 - @mlb_lib.MLB	71A6 71D4 108D1
IMVP6_PHASE2	IMVP6_PHASE2 - @mlb_lib.MLB	71A4 71C4 108D1
IMVP6_PHASE3	IMVP6_PHASE3 - @mlb_lib.MLB	72A7 72C6 108D1
IMVP6_PMON	IMVP6_PMON - @mlb_lib.MLB	53C8 71C5
IMVP6_PWM1	IMVP6_PWM1 - @mlb_lib.MLB	71A6 71D5
IMVP6_PWM2	IMVP6_PWM2 - @mlb_lib.MLB	71A4 71C5
IMVP6_PWM3	IMVP6_PWM3 - @mlb_lib.MLB	71C5 72A7 72C7
IMVP6_RBIAS	IMVP6_RBIAS - @mlb_lib.MLB	71A8 71B7
IMVP6_SOFT	IMVP6_SOFT - @mlb_lib.MLB	71A8 71C7
IMVP6_UGATE1	IMVP6_UGATE1 - @mlb_lib.MLB	71A6 71D4
IMVP6_UGATE2	IMVP6_UGATE2 - @mlb_lib.MLB	71A4 71C4
IMVP6_UGATE3	IMVP6_UGATE3 - @mlb_lib.MLB	72A7 72C6
IMVP6_VDIFF	IMVP6_VDIFF - @mlb_lib.MLB	71A8 71B7
IMVP6_VDIFF_RC	IMVP6_VDIFF_RC - @mlb_lib.MLB	71B8
IMVP6_VID<0>	IMVP6_VID<0> - @mlb_lib.MLB	12C1 71C7
IMVP6_VID<6..0>	IMVP6_VID<6..0> - @mlb_lib.MLB	100A3
IMVP6_VID<1>	IMVP6_VID<1> - @mlb_lib.MLB	12C1 71C7
IMVP6_VID<2>	IMVP6_VID<2> - @mlb_lib.MLB	12C1 71C7
IMVP6_VID<3>	IMVP6_VID<3> - @mlb_lib.MLB	12C1 71C7
IMVP6_VID<4>	IMVP6_VID<4> - @mlb_lib.MLB	12C1 71C7
IMVP6_VID<5>	IMVP6_VID<5> - @mlb_lib.MLB	12C1 71C7
IMVP6_VID<6>	IMVP6_VID<6> - @mlb_lib.MLB	12C1 71C7
IMVP6_VO	IMVP6_VO - @mlb_lib.MLB	71A8 71B4 72C1
IMVP6_VO1	IMVP6_VO1 - @mlb_lib.MLB	71A6 71D1 72A7
IMVP6_VO2	IMVP6_VO2 - @mlb_lib.MLB	71A4 71B1 72A7
IMVP6_VO3	IMVP6_VO3 - @mlb_lib.MLB	72A7 72A7 72C2
IMVP6_VO_R	IMVP6_VO_R - @mlb_lib.MLB	71B4
IMVP6_VR_TT_L	IMVP6_VR_TT_L - @mlb_lib.MLB	71C7
IMVP6_VSEN_N	IMVP6_VSEN_N - @mlb_lib.MLB	71A5 100A3
IMVP6_VSEN_P	IMVP6_VSEN_P - @mlb_lib.MLB	71A5 100A3
IMVP6_VSUM	IMVP6_VSUM - @mlb_lib.MLB	71A8 71C4 72B1
IMVP6_VSUM1	IMVP6_VSUM1 - @mlb_lib.MLB	71A6 71C2 72A7
IMVP6_VSUM2	IMVP6_VSUM2 - @mlb_lib.MLB	71A4 71B2 72A7
IMVP6_VSUM3	IMVP6_VSUM3 - @mlb_lib.MLB	72A7 72A7 72C3
IMVP6_VW	IMVP6_VW - @mlb_lib.MLB	71A8 71B7
IMVP_DPRSLPVR	IMVP_DPRSLPVR - @mlb_lib.MLB	71C7 100B3
IMVP_PGD_IN	IMVP_PGD_IN - @mlb_lib.MLB	70B3
IMVP_VR_ON	IMVP_VR_ON - @mlb_lib.MLB	7C4 49C8 71C7
INT_PIRQA_L	INT_PIRQA_L - @mlb_lib.MLB	24A4 24A8 104C3
INT_PIRQB_L	INT_PIRQB_L - @mlb_lib.MLB	24A4 24A8 104C3
INT_PIRQC_L	INT_PIRQC_L - @mlb_lib.MLB	24A4 24A8 104C3
INT_PIRQD_L	INT_PIRQD_L - @mlb_lib.MLB	24A4 24A8 104C3
INT_PIRQE_L	INT_PIRQE_L - @mlb_lib.MLB	24A4 24A6 98B7 104C3
INT_PIRQF_L	INT_PIRQF_L - @mlb_lib.MLB	24A4 24A6 104C3
INT_SERIRQ	INT_SERIRQ - @mlb_lib.MLB	7D4 25C8 49C8 51B4
INV_EN_BL_OR_PANEL_I D	INV_EN_BL_OR_PANEL_ID - @mlb_lib.MLB	6D6 28B2 85A3
IPHS_SW_INT_TO_SB	IPHS_SW_INT_TO_SB - @mlb_lib.MLB	98C6
IPHS_SW_SUPBIAS_EN_L	IPHS_SW_SUPBIAS_EN_L - @mlb_lib.MLB	98C6
ISENSE_CAL_EN	ISENSE_CAL_EN - @mlb_lib.MLB	49B8 50A2 53A8
ISENSE_CAL_EN_L	ISENSE_CAL_EN_L - @mlb_lib.MLB	53B8
ISENSE_CAL_LS12V	ISENSE_CAL_LS12V - @mlb_lib.MLB	53B7
ISENSE_CAL_EN_L_R	ISENSE_CAL_EN_L_R - @mlb_lib.MLB	53B8
ITP_CPURST_L	ITP_CPURST_L - @mlb_lib.MLB	100A3
ITS_ALIVE	ITS_ALIVE - @mlb_lib.MLB	6A7
ITS_PLUGGED_IN	ITS_PLUGGED_IN - @mlb_lib.MLB	6A8
LAN_ENERGY_DET	LAN_ENERGY_DET - @mlb_lib.MLB	23C6 28A2
LAN_PHYPC	TP_LAN_ENERGY_DET - @mlb_lib.MLB LAN_PHYPC - @mlb_lib.MLB	28A1 25A5 25C5
LCD_PWM	LCD_PWM - @mlb_lib.MLB	6D8 90B1
LCD_PWREN_DIV	LCD_PWREN_DIV - @mlb_lib.MLB	90C8
LCD_PWREN_L	LCD_PWREN_L - @mlb_lib.MLB	90B7
LCD_PWREN_L_RC	LCD_PWREN_L_RC - @mlb_lib.MLB	90C7
LCD_SHOULD_ON	LCD_SHOULD_ON - @mlb_lib.MLB	6A6
LED4300_1	LED4300_1 - @mlb_lib.MLB	39A7
LED4301_1	LED4301_1 - @mlb_lib.MLB	39A7
LED4302_1	LED4302_1 - @mlb_lib.MLB	39A6
LED4303_1	LED4303_1 - @mlb_lib.MLB	39A6
LINDACARD_GPIO	LINDACARD_GPIO - @mlb_lib.MLB	7C4 25A7 25D5 51B4
LPC_AD<0>	LPC_AD<0> - @mlb_lib.MLB	7D4 23D4 49C8 51C6
LPC_AD<1>	LPC_AD<1> - @mlb_lib.MLB	7A8 7C6 7D4 23D4 49C8 51C6
LPC_AD<2>	LPC_AD<2> - @mlb_lib.MLB	7D4 23D4 49C8 51C4
LPC_AD<3>	LPC_AD<3> - @mlb_lib.MLB	7D4 23D4 49C8 51C4
LPC_FRAME_L	LPC_FRAME_L - @mlb_lib.MLB	7D4 23D4 49C8 51B6
LVDS_A_CLK_N	LVDS_A_CLK_N - @mlb_lib.MLB TP_LVDS_A_CLK_N - @mlb_lib.MLB	15C5 22D8 22D7
LVDS_A_CLK_P	LVDS_A_CLK_P - @mlb_lib.MLB TP_LVDS_A_CLK_P - @mlb_lib.MLB	15C5 22D8 22D7
LVDS_A_DATA_N<0>	LVDS_A_DATA_N<0> - @mlb_lib.MLB	15C5 22D8
LVDS_A_DATA_N<1>	LVDS_A_DATA_N<1> - @mlb_lib.MLB	15C5 22C8
LVDS_A_DATA_N<2>	LVDS_A_DATA_N<2> - @mlb_lib.MLB	15C5 22C8
LVDS_A_DATA_P<0>	LVDS_A_DATA_P<0> - @mlb_lib.MLB	15C5 22C8
LVDS_A_DATA_P<1>	LVDS_A_DATA_P<1> - @mlb_lib.MLB	15C5 22C8
LVDS_A_DATA_P<2>	LVDS_A_DATA_P<2> - @mlb_lib.MLB	15C5 22C8
LVDS_BKLT_CTL	LVDS_BKLT_CTL - @mlb_lib.MLB TP_LVDS_BKLT_CTL - @mlb_lib.MLB	15D5 22D8 22D7
LVDS_BKLT_EN	LVDS_BKLT_EN - @mlb_lib.MLB TP_LVDS_BKLT_EN - @mlb_lib.MLB	15D5 22D8 22D7
LVDS_B_CLK_N	LVDS_B_CLK_N - @mlb_lib.MLB TP_LVDS_B_CLK_N - @mlb_lib.MLB	15C5 22D8 22D7
LVDS_B_CLK_P	LVDS_B_CLK_P - @mlb_lib.MLB TP_LVDS_B_CLK_P - @mlb_lib.MLB	15C5 22D8 22D7
LVDS_B_DATA_N<0>	LVDS_B_DATA_N<0> - @mlb_lib.MLB	15C5 22C8
LVDS_B_DATA_N<1>	LVDS_B_DATA_N<1> - @mlb_lib.MLB	15C5 22C8
LVDS_B_DATA_N<2>	LVDS_B_DATA_N<2> - @mlb_lib.MLB	15C5 22C8
LVDS_B_DATA_P<0>	LVDS_B_DATA_P<0> - @mlb_lib.MLB	15C5 22C8
LVDS_B_DATA_P<1>	LVDS_B_DATA_P<1> - @mlb_lib.MLB	15C5 22C8
LVDS_B_DATA_P<2>	LVDS_B_DATA_P<2> - @mlb_lib.MLB	15C5 22C8
LVDS_IBG	LVDS_IBG - @mlb_lib.MLB TP_LVDS_IBG - @mlb_lib.MLB	15D5 22D8 22D7
LVDS_L_CLK_N	LVDS_L_CLK_N - @mlb_lib.MLB	85B4 90A6 108C3
LVDS_L_CLK_P	LVDS_L_CLK_P - @mlb_lib.MLB	85B4 90A8 108C3
LVDS_L_DATA_N<0>	LVDS_L_DATA_N<0> - @mlb_lib.MLB	85A4 90A6
LVDS_L_DATA_N<3..0>	LVDS_L_DATA_N<3..0> - @mlb_lib.MLB	108C3
LVDS_L_DATA_N<1>	LVDS_L_DATA_N<1> - @mlb_lib.MLB	85A4 90A6
LVDS_L_DATA_N<2>	LVDS_L_DATA_N<2> - @mlb_lib.MLB	85A4 90A8
LVDS_L_DATA_N<3>	LVDS_L_DATA_N<3> - @mlb_lib.MLB	85A4 90A8
LVDS_L_DATA_P<0>	LVDS_L_DATA_P<0> - @mlb_lib.MLB	85A4 90A8
LVDS_L_DATA_P<3..0>	LVDS_L_DATA_P<3..0> - @mlb_lib.MLB	108C3
LVDS_L_DATA_P<1>	LVDS_L_DATA_P<1> - @mlb_lib.MLB	85A4 90A6
LVDS_L_DATA_P<2>	LVDS_L_DATA_P<2> - @mlb_lib.MLB	85A4 90A6
LVDS_L_DATA_P<3>	LVDS_L_DATA_P<3> - @mlb_lib.MLB	85A4 90A8
LVDS_VDD_EN	LVDS_VDD_EN - @mlb_lib.MLB TP_LVDS_VDD_EN - @mlb_lib.MLB	15D5 22D8 22D7
LVDS_VREFH	LVDS_VREFH - @mlb_lib.MLB TP_LVDS_VREFH - @mlb_lib.MLB	15D5 22D8 22D7
LVDS_VREFL	LVDS_VREFL - @mlb_lib.MLB TP_LVDS_VREFL - @mlb_lib.MLB	15D5 22D8 22D7
MCH_CORES0_BOOT	MCH_CORES0_BOOT - @mlb_lib.MLB	74C4
MCH_CORES0_BOOT_R	MCH_CORES0_BOOT_R - @mlb_lib.MLB	74C3
MCH_CORES0_ISEN	MCH_CORES0_ISEN - @mlb_lib.MLB	74C4
MCH_CORES0_LGATE	MCH_CORES0_LGATE - @mlb_lib.MLB	74C3
MCH_CORES0_OCSET	MCH_CORES0_OCSET - @mlb_lib.MLB	74B4
MCH_CORES0_SNUBBER_R	MCH_CORES0_SNUBBER_R - @mlb_lib.MLB	74C2
MCH_CORES0_SOFT	MCH_CORES0_SOFT - @mlb_lib.MLB	74C4
MCH_CORES0_SWITCHNOD E	MCH_CORES0_SWITCHNODE - @mlb_lib.MLB	74C3 108D1
MCH_CORES0_UGATE	MCH_CORES0_UGATE - @mlb_lib.MLB	74C4
MCH_CORES0_VSEN	MCH_CORES0_VSEN - @mlb_lib.MLB	74B3
MEMVTT_VREF	MEMVTT_VREF - @mlb_lib.MLB	75A4
MEM_A_A<0>	MEM_A_A<0> - @mlb_lib.MLB	17C5 31B3 33C6
MEM_A_A<14..0>	MEM_A_A<14..0> - @mlb_lib.MLB	102D3
MEM_A_A<1>	MEM_A_A<1> - @mlb_lib.MLB	17C5 31B6 33C6
MEM_A_A<2>	MEM_A_A<2> - @mlb_lib.MLB	17B5 31B3 33C6
MEM_A_A<3>	MEM_A_A<3> - @mlb_lib.MLB	17B5 31B6 33C6
MEM_A_A<4>	MEM_A_A<4> - @mlb_lib.MLB	17B5 31C3 33C6
MEM_A_A<5>	MEM_A_A<5> - @mlb_lib.MLB	17B5 31C6 33C6
MEM_A_A<6>	MEM_A_A<6> - @mlb_lib.MLB	17B5 31C3 33C6
MEM_A_A<7>	MEM_A_A<7> - @mlb_lib.MLB	17B5 31C3 33C6
MEM_A_A<8>	MEM_A_A<8> - @mlb_lib.MLB	17B5 31C6 33C6
MEM_A_A<9>	MEM_A_A<9> - @mlb_lib.MLB	17B5 31C6 33C6
MEM_A_A<10>	MEM_A_A<10> - @mlb_lib.MLB	17B5 31B6 33C6
MEM_A_A<11>	MEM_A_A<11> - @mlb_lib.MLB	17B5 31C3 33C6
MEM_A_A<12>	MEM_A_A<12> - @mlb_lib.MLB	17B5 31C6 33C6
MEM_A_A<13>	MEM_A_A<13> - @mlb_lib.MLB	17B5 31B3 33C6
MEM_A_A<14>	MEM_A_A<14> - @mlb_lib.MLB	16C6 31C3 33C6
MEM_A_BS<0>	MEM_A_BS<0> - @mlb_lib.MLB	17D5 31B6 33B6
MEM_A_BS<2..0>	MEM_A_BS<2..0> - @mlb_lib.MLB	102D3
MEM_A_BS<1>	MEM_A_BS<1> - @mlb_lib.MLB	17D5 31B3 33B6
MEM_A_BS<2>	MEM_A_BS<2> - @mlb_lib.MLB	17D5 31C6 33B6
MEM_A_CAS_L	MEM_A_CAS_L - @mlb_lib.MLB	17D5 31B6 33B6 102D3
MEM_A_DM<0>	MEM_A_DM<0> - @mlb_lib.MLB	17D5 31D3 102C3
MEM_A_DM<1>	MEM_A_DM<1> - @mlb_lib.MLB	17D5 31D3 102C3
MEM_A_DM<2>	MEM_A_DM<2> - @mlb_lib.MLB	17C5 31C3 102C3
MEM_A_DM<3>	MEM_A_DM<3> - @mlb_lib.MLB	17C5 31C6 102C3
MEM_A_DM<4>	MEM_A_DM<4> - @mlb_lib.MLB	17C5 31B3 102C3
MEM_A_DM<5>	MEM_A_DM<5> - @mlb_lib.MLB	17C5 31B6 102C3
MEM_A_DM<6>	MEM_A_DM<6> - @mlb_lib.MLB	17C5 31A3 102C3
MEM_A_DM<7>	MEM_A_DM<7> - @mlb_lib.MLB	17C5 31A6 102C3
MEM_A_DQ<0>	MEM_A_DQ<0> - @mlb_lib.MLB	17D8 31D6
MEM_A_DQ<6..0>	MEM_A_DQ<6..0> - @mlb_lib.MLB	102D3
MEM_A_DQ<1>	MEM_A_DQ<1> - @mlb_lib.MLB	17D8 31D6
MEM_A_DQ<2>	MEM_A_DQ<2> - @mlb_lib.MLB	17D8 31D6
MEM_A_DQ<3>	MEM_A_DQ<3> - @mlb_lib.MLB	17D8 31D6
MEM_A_DQ<4>	MEM_A_DQ<4> - @mlb_lib.MLB	17D8 31D3
MEM_A_DQ<5>	MEM_A_DQ<5> - @mlb_lib.MLB	17D8 31D3
MEM_A_DQ<6>	MEM_A_DQ<6> - @mlb_lib.MLB	17D8 31D3
MEM_A_DQ<7>	MEM_A_DQ<7> - @mlb_lib.MLB	7C7 17D8 31D3 102D3
MEM_A_DQ<8>	MEM_A_DQ<8> - @mlb_lib.MLB	17C8 31D6
MEM_A_DQ<13..8>	MEM_A_DQ<13..8> - @mlb_lib.MLB	102D3
MEM_A_DQ<9>	MEM_A_DQ<9> - @mlb_lib.MLB	17C8 31D6
MEM_A_DQ<10>	MEM_A_DQ<10> - @mlb_lib.MLB	17C8 31D6
MEM_A_DQ<11>	MEM_A_DQ<11> - @mlb_lib.MLB	17C8 31D6
MEM_A_DQ<12>	MEM_A_DQ<12> - @mlb_lib.MLB	17C8 31D3
MEM_A_DQ<13>	MEM_A_DQ<13> - @mlb_lib.MLB	17C8 31D3
MEM_A_DQ<14>	MEM_A_DQ<14> - @mlb_lib.MLB	7C7 17C8 31D3 102D3
MEM_A_DQ<15>	MEM_A_DQ<15> - @mlb_lib.MLB	17C8 31D3 102C3
MEM_A_DQ<16>	MEM_A_DQ<16> - @mlb_lib.MLB	7B7 17C8 31D6 102C3
MEM_A_DQ<17>	MEM_A_DQ<17> - @mlb_lib.MLB	17C8 31D6
MEM_A_DQ<23..17>	MEM_A_DQ<23..17> - @mlb_lib.MLB	102C3
MEM_A_DQ<18>	MEM_A_DQ<18> - @mlb_lib.MLB	17C8 31C6
MEM_A_DQ<19>	MEM_A_DQ<19> - @mlb_lib.MLB	17C8 31C6
MEM_A_DQ<20>	MEM_A_DQ<20> - @mlb_lib.MLB	17C8 31D3
MEM_A_DQ<21>	MEM_A_DQ<21> - @mlb_lib.MLB	17C8 31D3
MEM_A_DQ<22>	MEM_A_DQ<22> - @mlb_lib.MLB	17C8 31C3
MEM_A_DQ<23>	MEM_A_DQ<23> - @mlb_lib.MLB	17C8 31C3
MEM_A_DQ<24>	MEM_A_DQ<24> - @mlb_lib.MLB	17C8 31C6 102C3
MEM_A_DQ<25>	MEM_A_DQ<25> - @mlb_lib.MLB	7B7 17C8 31C6 102C3
MEM_A_DQ<26>	MEM_A_DQ<26> - @mlb_lib.MLB	17C8 31C6
MEM_A_DQ<31..26>	MEM_A_DQ<31..26> - @mlb_lib.MLB	102C3
MEM_A_DQ<27>	MEM_A_DQ<27> - @mlb_lib.MLB	17C8 31C6
MEM_A_DQ<28>	MEM_A_DQ<28> - @mlb_lib.MLB	17C8 31C3
MEM_A_DQ<29>	MEM_A_DQ<29> - @mlb_lib.MLB	17C8 31C3
MEM_A_DQ<30>	MEM_A_DQ<30> - @mlb_lib.MLB	17C8 31C3
MEM_A_DQ<31>	MEM_A_DQ<31> - @mlb_lib.MLB	17C8 31C3
MEM_A_DQ<32>	MEM_A_DQ<32> - @mlb_lib.MLB	17C8 31B6
MEM_A_DQ<38..32>	MEM_A_DQ<38..32> - @mlb_lib.MLB	102C3
MEM_A_DQ<33>	MEM_A_DQ<33> - @mlb_lib.MLB	17C8 31B6
MEM_A_DQ<34>	MEM_A_DQ<34> - @mlb_lib.MLB	17B8 31B6
MEM_A_DQ<35>	MEM_A_DQ<35> - @mlb_lib.MLB	17B8 31B6
MEM_A_DQ<36>	MEM_A_DQ<36> - @mlb_lib.MLB	17B8 31B3
MEM_A_DQ<37>	MEM_A_DQ<37> - @mlb_lib.MLB	17B8 31B3
MEM_A_DQ<38>	MEM_A_DQ<38> - @mlb_lib.MLB	17B8 31B3
MEM_A_DQ<39>	MEM_A_DQ<39> - @mlb_lib.MLB	7B7 17B8 31B3 102C3
MEM_A_DQ<40>	MEM_A_DQ<40> - @mlb_lib.MLB	17B8 31B6
MEM_A_DQ<46..40>	MEM_A_DQ<46..40> - @mlb_lib.MLB	102C3
MEM_A_DQ<41>	MEM_A_DQ<41> - @mlb_lib.MLB	17B8 31B6
MEM_A_DQ<42>	MEM_A_DQ<42> - @mlb_lib.MLB	17B8 31A6
MEM_A_DQ<43>	MEM_A_DQ<43> - @mlb_lib.MLB	17B8 31A6
MEM_A_DQ<44>	MEM_A_DQ<44> - @mlb_lib.MLB	17B8 31B3
MEM_A_DQ<45>	MEM_A_DQ<45> - @mlb_lib.MLB	17B8 31B3
MEM_A_DQ<46>	MEM_A_DQ<46> - @mlb_lib.MLB	17B8 31A3
MEM_A_DQ<47>	MEM_A_DQ<47> - @mlb_lib.MLB	7B7 17B8 31A3 102C3
MEM_A_DQ<48>	MEM_A_DQ<48> - @mlb_lib.MLB	17B8 31A6
MEM_A_DQ<53..48>	MEM_A_DQ<53..48> - @mlb_lib.MLB	102C3
MEM_A_DQ<49>	MEM_A_DQ<49> - @mlb_lib.MLB	17B8 31A6
MEM_A_DQ<50>	MEM_A_DQ<50> - @mlb_lib.MLB	17B8 31A6
MEM_A_DQ<51>	MEM_A_DQ<51> - @mlb_lib.MLB	17B8 31A6
MEM_A_DQ<52>	MEM_A_DQ<52> - @mlb_lib.MLB	17B8 31A3
MEM_A_DQ<53>	MEM_A_DQ<53> - @mlb_lib.MLB	17B8 31A3
MEM_A_DQ<54>	MEM_A_DQ<54> - @mlb_lib.MLB	7B7 17B8 31A3 102C3
MEM_A_DQ<55>	MEM_A_DQ<55> - @mlb_lib.MLB	17B8 31A3 102C3
MEM_A_DQ<56>	MEM_A_DQ<56> - @mlb_lib.MLB	17B8 31A6
MEM_A_DQ<58..56>	MEM_A_DQ<58..56> - @mlb_lib.MLB	102C3
MEM_A_DQ<57>	MEM_A_DQ<57> - @mlb_lib.MLB	17B8 31A6
MEM_A_DQ<58>	MEM_A_DQ<58> - @mlb_lib.MLB	17B8 31A6
MEM_A_DQ<59>	MEM_A_DQ<59> - @mlb_lib.MLB	7B7 17B8 31A6 102C3
MEM_A_DQ<60>	MEM_A_DQ<60> - @mlb_lib.MLB	17A8 31A3
MEM_A_DQ<63..60>	MEM_A_DQ<63..60> - @mlb_lib.MLB	102C3
MEM_A_DQ<61>	MEM_A_DQ<61> - @mlb_lib.MLB	17A8 31A3
MEM_A_DQ<62>	MEM_A_DQ<62> - @mlb_lib.MLB	17A8 31A3
MEM_A_DQ<63>	MEM_A_DQ<63> - @mlb_lib.MLB	17A8 31A3
MEM_A_DQS_N<0>	MEM_A_DQS_N<0> - @mlb_lib.MLB	7B7 17C5 31D6 102B3
MEM_A_DQS_N<1>	MEM_A_DQS_N<1> - @mlb_lib.MLB	7B7 17C5 31D6 102B3
MEM_A_DQS_N<2>	MEM_A_DQS_N<2> - @mlb_lib.MLB	7B7 17C5 31C6 102B3
MEM_A_DQS_N<3>	MEM_A_DQS_N<3> - @mlb_lib.MLB	7B7 17C5 31C3 102B3
MEM_A_DQS_N<4>	MEM_A_DQS_N<4> - @mlb_lib.MLB	7B7 17C5 31B6 102B3
MEM_A_DQS_N<5>	MEM_A_DQS_N<5> - @mlb_lib.MLB	7B7 17C5 31B3 102B3
MEM_A_DQS_N<6>	MEM_A_DQS_N<6> - @mlb_lib.MLB	7B7 17C5 31A6 102B3
MEM_A_DQS_N<7>	MEM_A_DQS_N<7> - @mlb_lib.MLB	7B7 17C5 31A3 102B3
MEM_A_DQS_P<0>	MEM_A_DQS_P<0> - @mlb_lib.MLB	7B7 17C5 31D6 102B3
MEM_A_DQS_P<1>	MEM_A_DQS_P<1> - @mlb_lib.MLB	7B7 17C5 31D6 102B3
MEM_A_DQS_P<2>	MEM_A_DQS_P<2> - @mlb_lib.MLB	7B7 17C5 31C6 102B3
MEM_A_DQS_P<3>	MEM_A_DQS_P<3> - @mlb_lib.MLB	7B7 17C5 31C3 102B3
MEM_A_DQS_P<4>	MEM_A_DQS_P<4> - @mlb_lib.MLB	7B7 17C5 31B6 102B3
MEM_A_DQS_P<5>	MEM_A_DQS_P<5> - @mlb_lib.MLB	7B7 17C5 31B3 102B3
MEM_A_DQS_P<6>	MEM_A_DQS_P<6> - @mlb_lib.MLB	7B7 17C5 31A6 102B3
MEM_A_DQS_P<7>	MEM_A_DQS_P<7> - @mlb_lib.MLB	7B7 17C5 31A3 102B3
MEM_A_RAS_L	MEM_A_RAS_L - @mlb_lib.MLB	17B5 31B3 33B6 102D3
MEM_A_SA<0>	MEM_A_SA<0> - @mlb_lib.MLB	31A4
MEM_A_SA<1>	MEM_A_SA<1> - @mlb_lib.MLB	31A4
MEM_A_WE_L	MEM_A_WE_L - @mlb_lib.MLB	17B5 31B6 33B6 102D3
MEM_B_A<0>	MEM_B_A<0> - @mlb_lib.MLB	17C1 32B3 33B6
MEM_B_A<14..0>	MEM_B_A<14..0> - @mlb_lib.MLB	102D1
MEM_B_A<1>	MEM_B_A<1> - @mlb_lib.MLB	17C1 32B6 33B6
MEM_B_A<2>	MEM_B_A<2> - @mlb_lib.MLB	17B1 32B3 33B6
MEM_B_A<3>	MEM_B_A<3> - @mlb_lib.MLB	17B1 32B6 33B6
MEM_B_A<4>	MEM_B_A<4> - @mlb_lib.MLB	17B1 32C3 33B6
MEM_B_A<5>	MEM_B_A<5> - @mlb_lib.MLB	17B1 32C6 33B6
MEM_B_A<6>	MEM_B_A<6> - @mlb_lib.MLB	17B1 32C3 33B6
MEM_B_A<7>	MEM_B_A<7> - @mlb_lib.MLB	17B1 32C3 33B6
MEM_B_A<8>	MEM_B_A<8> - @mlb_lib.MLB	17B1 32C6 33B6
MEM_B_A<9>	MEM_B_A<9> - @mlb_lib.MLB	17B1 32C6 33B6
MEM_B_A<10>	MEM_B_A<10> - @mlb_lib.MLB	17B1 32B6 33B6
MEM_B_A<11>	MEM_B_A<11> - @mlb_lib.MLB	17B1 32C3 33A6
MEM_B_A<12>	MEM_B_A<12> - @mlb_lib.MLB	17B1 32C6 33A6
MEM_B_A<13>	MEM_B_A<13> - @mlb_lib.MLB	17B1 32B3 33A6
MEM_B_A<14>	MEM_B_A<14> - @mlb_lib.MLB	16C6 32C3 33A6
MEM_B_BS<0>	MEM_B_BS<0> - @mlb_lib.MLB	17D1 32B6 33A6
MEM_B_BS<2..0>	MEM_B_BS<2..0> - @mlb_lib.MLB	102D1
MEM_B_BS<1>	MEM_B_BS<1> - @mlb_lib.MLB	17D1 32B3 33A6
MEM_B_BS<2>	MEM_B_BS<2> - @mlb_lib.MLB	17D1 32C6 33A6
MEM_B_CAS_L	MEM_B_CAS_L - @mlb_lib.MLB	17D1 32B6 33A6 102D1
MEM_B_DM<0>	MEM_B_DM<0> - @mlb_lib.MLB	17D1 32D3 102C1
MEM_B_DM<1>	MEM_B_DM<1> - @mlb_lib.MLB	17D1 32D3 102C1
MEM_B_DM<2>	MEM_B_DM<2> - @mlb_lib.MLB	17C1 32C3 102C1
MEM_B_DM<3>	MEM_B_DM<3> - @mlb_lib.MLB	17C1 32C6 102C1
MEM_B_DM<4>	MEM_B_DM<4> - @mlb_lib.MLB	17C1 32B3 102C1
MEM_B_DM<5>	MEM_B_DM<5> - @mlb_lib.MLB	17C1 32B6 102C1
MEM_B_DM<6>	MEM_B_DM<6> - @mlb_lib.MLB	17C1 32A3 102C1
MEM_B_DM<7>	MEM_B_DM<7> - @mlb_lib.MLB	17C1 32A6 102C1
MEM_B_DQ<0>	MEM_B_DQ<0> - @mlb_lib.MLB	17D4 32D6
MEM_B_DQ<5..0>	MEM_B_DQ<5..0> - @mlb_lib.MLB	102D1
MEM_B_DQ<1>	MEM_B_DQ<1> - @mlb_lib.MLB	17D4 32D6
MEM_B_DQ<2>	MEM_B_DQ<2> - @mlb_lib.MLB	17D4 32D6
MEM_B_DQ<3>	MEM_B_DQ<3> - @mlb_lib.MLB	17D4 32D6
MEM_B_DQ<4>	MEM_B_DQ<4> - @mlb_lib.MLB	17D4 32D3
MEM_B_DQ<5>	MEM_B_DQ<5> - @mlb_lib.MLB	17D4 32D3
MEM_B_DQ<6>	MEM_B_DQ<6> - @mlb_lib.MLB	7B7 17D4 32D3 102D1
MEM_B_DQ<7>	MEM_B_DQ<7> - @mlb_lib.MLB	17D4 32D3 102D1
MEM_B_DQ<8>	MEM_B_DQ<8> - @mlb_lib.MLB	7B7 17C4 32D6 102D1
MEM_B_DQ<9>	MEM_B_DQ<9> - @mlb_lib.MLB	17C4 32D6
MEM_B_DQ<15..9>	MEM_B_DQ<15..9> - @mlb_lib.MLB	102D1
MEM_B_DQ<10>	MEM_B_DQ<10> - @mlb_lib.MLB	17C4 32D6
MEM_B_DQ<11>	MEM_B_DQ<11> - @mlb_lib.MLB	17C4 32D6
MEM_B_DQ<12>	MEM_B_DQ<12> - @mlb_lib.MLB	17C4 32D3
MEM_B_DQ<13>	MEM_B_DQ<13> - @mlb_lib.MLB	17C4 32D3
MEM_B_DQ<14>	MEM_B_DQ<14> - @mlb_lib.MLB	17C4 32D3
MEM_B_DQ<15>	MEM_B_DQ<15> - @mlb_lib.MLB	17C4 32D3
MEM_B_DQ<16>	MEM_B_DQ<16> - @mlb_lib.MLB	17C4 32D6
MEM_B_DQ<22..16>	MEM_B_DQ<22..16> - @mlb_lib.MLB	102D1
MEM_B_DQ<17>	MEM_B_DQ<17> - @mlb_lib.MLB	17C4 32D6

ODD_PWR_EN_L	ODD_PWR_EN_L - @mlb_lib.MLB	24A4 24A6
ODD_RST_5VTOL_L	ODD_RST_5VTOL_L - @mlb_lib.MLB	24B6 44C6 103D3
ODD_THRMD_N	ODD_THRMD_N - @mlb_lib.MLB	55A5 55B6 108A3
ODD_THRMD_P	ODD_THRMD_P - @mlb_lib.MLB	55B5 55B6 108A3
P1V8S0_EN_L	P1V8S0_EN_L - @mlb_lib.MLB	78B7
P1V8S0_EN_L_RC	P1V8S0_EN_L_RC - @mlb_lib.MLB	78B6
P1V8S0_GDRV	P1V8S0_GDRV - @mlb_lib.MLB	78B7
P1V8S0_SS	P1V8S0_SS - @mlb_lib.MLB	78B6
P1V8S0_SS_RC	P1V8S0_SS_RC - @mlb_lib.MLB	78B7
P2V5S0_SW	P2V5S0_SW - @mlb_lib.MLB	108D1
P3V3S0_EN_L	P3V3S0_EN_L - @mlb_lib.MLB	78B3
P3V3S0_SS	P3V3S0_SS - @mlb_lib.MLB	78B2
P3V3S5_FB	P3V3S5_FB - @mlb_lib.MLB	77D5
P3V3S5_SW	P3V3S5_SW - @mlb_lib.MLB	77D5 108D1
P5VREG_FCB	P5VREG_FCB - @mlb_lib.MLB	76A3 76B5
P5VREG_FSEL	P5VREG_FSEL - @mlb_lib.MLB	76A2 76B4
P5VS0_EN_L	P5VS0_EN_L - @mlb_lib.MLB	78D3
P5VS0_SS	P5VS0_SS - @mlb_lib.MLB	78D2
P5VS3_EN_L	P5VS3_EN_L - @mlb_lib.MLB	78D7
P5VS3_SS	P5VS3_SS - @mlb_lib.MLB	78D6
P5VS5_EN	P5VS5_EN - @mlb_lib.MLB	77D6
PANEL_ID	PANEL_ID - @mlb_lib.MLB	28B2
	TP_SB_GPIO20 - @mlb_lib.MLB	25C5 28B1
PCIE_ENET_D2R_C_N	PCIE_ENET_D2R_C_N - @mlb_lib.MLB	37C4 108C3
PCIE_ENET_D2R_C_P	PCIE_ENET_D2R_C_P - @mlb_lib.MLB	37C4 108C3
PCIE_ENET_D2R_N	PCIE_ENET_D2R_N - @mlb_lib.MLB	7B8 24C5 37C8 104C3
PCIE_ENET_D2R_P	PCIE_ENET_D2R_P - @mlb_lib.MLB	7B8 24C5 37C8 104C3
PCIE_ENET_R2D_C_N	PCIE_ENET_R2D_C_N - @mlb_lib.MLB	24C5 37C8 104C3
PCIE_ENET_R2D_C_P	PCIE_ENET_R2D_C_P - @mlb_lib.MLB	24C5 37C8 104C3
PCIE_ENET_R2D_N	PCIE_ENET_R2D_N - @mlb_lib.MLB	7D6 37C4 108C3
PCIE_ENET_R2D_P	PCIE_ENET_R2D_P - @mlb_lib.MLB	7D6 37C4 108C3
PCIE_FW_D2R_C_N	PCIE_FW_D2R_C_N - @mlb_lib.MLB	40C3 108C3
PCIE_FW_D2R_C_P	PCIE_FW_D2R_C_P - @mlb_lib.MLB	40C3 108C3
PCIE_FW_D2R_N	PCIE_FW_D2R_N - @mlb_lib.MLB	7B8 40C2 42A3 104C3
	TP_PCIE_FW_D2R_N - @mlb_lib.MLB	24D5 42A2
PCIE_FW_D2R_P	PCIE_FW_D2R_P - @mlb_lib.MLB	7B8 40C2 42A3 104C3
	TP_PCIE_FW_D2R_P - @mlb_lib.MLB	24D5 42A2
PCIE_FW_R2D_C_N	PCIE_FW_R2D_C_N - @mlb_lib.MLB	40C1 42A2 104C3
	TP_PCIE_FW_R2D_C_N - @mlb_lib.MLB	24D5 42A3
PCIE_FW_R2D_C_P	PCIE_FW_R2D_C_P - @mlb_lib.MLB	40C1 42A2 104C3
	TP_PCIE_FW_R2D_C_P - @mlb_lib.MLB	24D5 42A3
PCIE_FW_R2D_N	PCIE_FW_R2D_N - @mlb_lib.MLB	7D6 40C3 108C3
PCIE_FW_R2D_P	PCIE_FW_R2D_P - @mlb_lib.MLB	7D6 40C3 108C3
PCIE_MINI_D2R_N	PCIE_MINI_D2R_N - @mlb_lib.MLB	7B8 24D5 34C8 104C3
PCIE_MINI_D2R_P	PCIE_MINI_D2R_P - @mlb_lib.MLB	7B8 24C5 34C8 104C3
PCIE_MINI_R2D_C_N	PCIE_MINI_R2D_C_N - @mlb_lib.MLB	24C5 34B8 104C3
PCIE_MINI_R2D_C_P	PCIE_MINI_R2D_C_P - @mlb_lib.MLB	24C5 34B8 104C3
PCIE_MINI_R2D_N	PCIE_MINI_R2D_N - @mlb_lib.MLB	34B6 108C3
PCIE_MINI_R2D_P	PCIE_MINI_R2D_P - @mlb_lib.MLB	34B6 108B3
PCIE_WAKE_L	PCIE_WAKE_L - @mlb_lib.MLB	25C8 34C6 37B8
PCI_AD<0>	PCI_AD<0> - @mlb_lib.MLB	24B8 28C5
	TP_PCI_AD_0 - @mlb_lib.MLB	28C4
PCI_AD<18..0>	PCI_AD<18..0> - @mlb_lib.MLB	104D3
	TP_PCI_AD_18 - @mlb_lib.MLB	28B4
PCI_AD<1>	PCI_AD<1> - @mlb_lib.MLB	24B8 28C5
	TP_PCI_AD_1 - @mlb_lib.MLB	28C4
PCI_AD<2>	PCI_AD<2> - @mlb_lib.MLB	24B8 28C5
	TP_PCI_AD_2 - @mlb_lib.MLB	28C4
PCI_AD<3>	PCI_AD<3> - @mlb_lib.MLB	24B8 28C5
	TP_PCI_AD_3 - @mlb_lib.MLB	28C4
PCI_AD<4>	PCI_AD<4> - @mlb_lib.MLB	24B8 28C5
	TP_PCI_AD_4 - @mlb_lib.MLB	28C4
PCI_AD<5>	PCI_AD<5> - @mlb_lib.MLB	24B8 28C5
	TP_PCI_AD_5 - @mlb_lib.MLB	28C4
PCI_AD<6>	PCI_AD<6> - @mlb_lib.MLB	24B8 28C5
	TP_PCI_AD_6 - @mlb_lib.MLB	28C4
PCI_AD<7>	PCI_AD<7> - @mlb_lib.MLB	24B8 28C5
	TP_PCI_AD_7 - @mlb_lib.MLB	28C4
PCI_AD<8>	PCI_AD<8> - @mlb_lib.MLB	24B8 28C5
	TP_PCI_AD_8 - @mlb_lib.MLB	28C4
PCI_AD<9>	PCI_AD<9> - @mlb_lib.MLB	24B8 28C5
	TP_PCI_AD_9 - @mlb_lib.MLB	28C4
PCI_AD<10>	PCI_AD<10> - @mlb_lib.MLB	24A8 28C5
	TP_PCI_AD_10 - @mlb_lib.MLB	28C4
PCI_AD<11>	PCI_AD<11> - @mlb_lib.MLB	24A8 28C5
	TP_PCI_AD_11 - @mlb_lib.MLB	28C4
PCI_AD<12>	PCI_AD<12> - @mlb_lib.MLB	24A8 28C5
	TP_PCI_AD_12 - @mlb_lib.MLB	28C4
PCI_AD<13>	PCI_AD<13> - @mlb_lib.MLB	24A8 28C5
	TP_PCI_AD_13 - @mlb_lib.MLB	28C4
PCI_AD<14>	PCI_AD<14> - @mlb_lib.MLB	24A8 28C5
	TP_PCI_AD_14 - @mlb_lib.MLB	28C4
PCI_AD<15>	PCI_AD<15> - @mlb_lib.MLB	24A8 28C5
	TP_PCI_AD_15 - @mlb_lib.MLB	28C4
PCI_AD<16>	PCI_AD<16> - @mlb_lib.MLB	24A8 28C5
	PCI_AD<16 - @mlb_lib.MLB	28C4
PCI_AD<17>	PCI_AD<17> - @mlb_lib.MLB	24A8 28C5
	TP_PCI_AD_17 - @mlb_lib.MLB	28C4
PCI_AD<18>	PCI_AD<18> - @mlb_lib.MLB	24A8 28B5
	TP_PCI_AD_18 - @mlb_lib.MLB	28B4
PCI_AD<19>	PCI_AD<19> - @mlb_lib.MLB	24A8 28B5 104D3
	TP_PCI_AD_19 - @mlb_lib.MLB	28B4
PCI_AD<20>	PCI_AD<20> - @mlb_lib.MLB	24A8 28B5 104D3
	TP_PCI_AD_20 - @mlb_lib.MLB	28B4
PCI_AD<21>	PCI_AD<21> - @mlb_lib.MLB	24A8 28B5
	TP_PCI_AD_21 - @mlb_lib.MLB	28B4
PCI_AD<31..21>	PCI_AD<31..21> - @mlb_lib.MLB	104D3
	TP_PCI_AD_31 - @mlb_lib.MLB	28B4
PCI_AD<22>	PCI_AD<22> - @mlb_lib.MLB	24A8 28B5
	TP_PCI_AD_22 - @mlb_lib.MLB	28B4
PCI_AD<23>	PCI_AD<23> - @mlb_lib.MLB	24A8 28B5
	TP_PCI_AD_23 - @mlb_lib.MLB	28B4
PCI_AD<24>	PCI_AD<24> - @mlb_lib.MLB	24A8 28B5
	TP_PCI_AD_24 - @mlb_lib.MLB	28B4
PCI_AD<25>	PCI_AD<25> - @mlb_lib.MLB	24A8 28B5
	TP_PCI_AD_25 - @mlb_lib.MLB	28B4
PCI_AD<26>	PCI_AD<26> - @mlb_lib.MLB	24A8 28B5
	TP_PCI_AD_26 - @mlb_lib.MLB	28B4
PCI_AD<27>	PCI_AD<27> - @mlb_lib.MLB	24A8 28B5
	TP_PCI_AD_27 - @mlb_lib.MLB	28B4
PCI_AD<28>	PCI_AD<28> - @mlb_lib.MLB	24A8 28B5
	TP_PCI_AD_28 - @mlb_lib.MLB	28B4
PCI_AD<29>	PCI_AD<29> - @mlb_lib.MLB	24A8 28B5
	TP_PCI_AD_29 - @mlb_lib.MLB	28B4
PCI_AD<30>	PCI_AD<30> - @mlb_lib.MLB	24A8 28B5
	TP_PCI_AD_30 - @mlb_lib.MLB	28B4
PCI_AD<31>	PCI_AD<31> - @mlb_lib.MLB	24A8 28B5
	TP_PCI_AD_31 - @mlb_lib.MLB	28B4
PCI_CLK33M_LPCPLUS	PCI_CLK33M_LPCPLUS - @mlb_lib.MLB	7D4 30A3 51C4 105C3
PCI_CLK33M_SB	PCI_CLK33M_SB - @mlb_lib.MLB	7B8 24A6 30A3 105B3
PCI_CLK33M_SMC	PCI_CLK33M_SMC - @mlb_lib.MLB	7C6 30A3 49C8 105B3
PCI_CLK33M_TPM	PCI_CLK33M_TPM - @mlb_lib.MLB	105B3
PCI_C_BE_L<0>	PCI_C_BE_L<0> - @mlb_lib.MLB	24B6 28B5
	TP_PCI_C_BE_L_0 - @mlb_lib.MLB	28B4

PCI_C_BE_L<3..0>	PCI_C_BE_L<3..0> - @mlb_lib.MLB	104D3
	TP_PCI_C_BE_L_3 - @mlb_lib.MLB	28B4
PCI_C_BE_L<1>	PCI_C_BE_L<1> - @mlb_lib.MLB	24A6 28B5
	TP_PCI_C_BE_L_1 - @mlb_lib.MLB	28B4
PCI_C_BE_L<2>	PCI_C_BE_L<2> - @mlb_lib.MLB	24A6 28B5
	TP_PCI_C_BE_L_2 - @mlb_lib.MLB	28B4
PCI_C_BE_L<3>	PCI_C_BE_L<3> - @mlb_lib.MLB	24A6 28B5
	TP_PCI_C_BE_L_3 - @mlb_lib.MLB	28B4
PCI_DEVSEL_L	PCI_DEVSEL_L - @mlb_lib.MLB	24A4 24A6 104D3
PCI_FRAME_L	PCI_FRAME_L - @mlb_lib.MLB	24A4 24A6 104D3
PCI_FW_GNT_L	PCI_FW_GNT_L - @mlb_lib.MLB	24B5 104D3
	BOOT_LPC_SPI_L - @mlb_lib.MLB	7D4 24B5 51B6
PCI_FW_REQ_L	PCI_FW_REQ_L - @mlb_lib.MLB	24A4 24B6 104D3
PCI_GNT1_L	PCI_GNT1_L - @mlb_lib.MLB	104D3
PCI_GNT2_L	PCI_GNT2_L - @mlb_lib.MLB	104C3
PCI_IRDY_L	PCI_IRDY_L - @mlb_lib.MLB	24A4 24A6 104D3
PCI_LOCK_L	PCI_LOCK_L - @mlb_lib.MLB	24A4 24A6 104D3
PCI_PAR	PCI_PAR - @mlb_lib.MLB	24A6 28B5 104D3
	TP_PCI_PAR - @mlb_lib.MLB	28B4
PCI_PERR_L	PCI_PERR_L - @mlb_lib.MLB	24A4 24A6 104D3
PCI_PME_FW_L	PCI_PME_FW_L - @mlb_lib.MLB	25B5 25C5 40C3
PCI_REQ1_L	PCI_REQ1_L - @mlb_lib.MLB	7C3 24A4 24B6 104D3
PCI_REQ2_L	PCI_REQ2_L - @mlb_lib.MLB	7C3 24A4 24B6 104D3
PCI_RST_L	PCI_RST_L - @mlb_lib.MLB	24A6 28B5
	TP_PCI_RST_L - @mlb_lib.MLB	28B4
PCI_SERR_L	PCI_SERR_L - @mlb_lib.MLB	24A4 24A6 28C4 104D3
PCI_STOP_L	PCI_STOP_L - @mlb_lib.MLB	24A4 24A6 104D3
PCI_TRDY_L	PCI_TRDY_L - @mlb_lib.MLB	24A4 24A6 104D3
PEG_COMP	PEG_COMP - @mlb_lib.MLB	15D3
PEG_D2R_N<0>	PEG_D2R_N<0> - @mlb_lib.MLB	15D3 84C4
PEG_D2R_N<6..0>	PEG_D2R_N<6..0> - @mlb_lib.MLB	101D3
PEG_D2R_N<1>	PEG_D2R_N<1> - @mlb_lib.MLB	15D3 84C4
PEG_D2R_N<2>	PEG_D2R_N<2> - @mlb_lib.MLB	15D3 84B4
PEG_D2R_N<3>	PEG_D2R_N<3> - @mlb_lib.MLB	15D3 84B4
PEG_D2R_N<4>	PEG_D2R_N<4> - @mlb_lib.MLB	15D3 84B4
PEG_D2R_N<5>	PEG_D2R_N<5> - @mlb_lib.MLB	15D3 84B4
PEG_D2R_N<6>	PEG_D2R_N<6> - @mlb_lib.MLB	15D3 84B4
PEG_D2R_N<7>	PEG_D2R_N<7> - @mlb_lib.MLB	7A7 15D3 84B4 101D3
PEG_D2R_N<8>	PEG_D2R_N<8> - @mlb_lib.MLB	15D3 84B4
PEG_D2R_N<15..8>	PEG_D2R_N<15..8> - @mlb_lib.MLB	101D3
PEG_D2R_N<9>	PEG_D2R_N<9> - @mlb_lib.MLB	15D3 84B4
PEG_D2R_N<10>	PEG_D2R_N<10> - @mlb_lib.MLB	15C3 84B4
PEG_D2R_N<11>	PEG_D2R_N<11> - @mlb_lib.MLB	15C3 84A4
PEG_D2R_N<12>	PEG_D2R_N<12> - @mlb_lib.MLB	15C3 84A4
PEG_D2R_N<13>	PEG_D2R_N<13> - @mlb_lib.MLB	15C3 84A4
PEG_D2R_N<14>	PEG_D2R_N<14> - @mlb_lib.MLB	15C3 84A4
PEG_D2R_N<15>	PEG_D2R_N<15> - @mlb_lib.MLB	15C3 84A4
PEG_D2R_P<0>	PEG_D2R_P<0> - @mlb_lib.MLB	15C3 84C4
PEG_D2R_P<6..0>	PEG_D2R_P<6..0> - @mlb_lib.MLB	101D3
PEG_D2R_P<1>	PEG_D2R_P<1> - @mlb_lib.MLB	15C3 84C4
PEG_D2R_P<2>	PEG_D2R_P<2> - @mlb_lib.MLB	15C3 84B4
PEG_D2R_P<3>	PEG_D2R_P<3> - @mlb_lib.MLB	15C3 84B4
PEG_D2R_P<4>	PEG_D2R_P<4> - @mlb_lib.MLB	15C3 84A4
PEG_D2R_P<5>	PEG_D2R_P<5> - @mlb_lib.MLB	15C3 84B4
PEG_D2R_P<6>	PEG_D2R_P<6> - @mlb_lib.MLB	7A7 15C3 84B4 101D3
PEG_D2R_P<15..8>	PEG_D2R_P<15..8> - @mlb_lib.MLB	101D3
PEG_D2R_P<9>	PEG_D2R_P<9> - @mlb_lib.MLB	15C3 84B4
PEG_D2R_P<10>	PEG_D2R_P<10> - @mlb_lib.MLB	15C3 84B4
PEG_D2R_P<11>	PEG_D2R_P<11> - @mlb_lib.MLB	15C3 84A4
PEG_D2R_P<12>	PEG_D2R_P<12> - @mlb_lib.MLB	15C3 84A4
PEG_D2R_P<13>	PEG_D2R_P<13> - @mlb_lib.MLB	15C3 84A4
PEG_D2R_P<14>	PEG_D2R_P<14> - @mlb_lib.MLB	15C3 84A4
PEG_D2R_P<15>	PEG_D2R_P<15> - @mlb_lib.MLB	15C3 84A4
PEG_R2D_C_N<0>	PEG_R2D_C_N<0> - @mlb_lib.MLB	15C3 84C8
PEG_R2D_C_N<15..0>	PEG_R2D_C_N<15..0> - @mlb_lib.MLB	101D3
PEG_R2D_C_N<1>	PEG_R2D_C_N<1> - @mlb_lib.MLB	15C3 84C8
PEG_R2D_C_N<2>	PEG_R2D_C_N<2> - @mlb_lib.MLB	15C3 84B8
PEG_R2D_C_N<3>	PEG_R2D_C_N<3> - @mlb_lib.MLB	15B3 84B8
PEG_R2D_C_N<4>	PEG_R2D_C_N<4> - @mlb_lib.MLB	15B3 84B8
PEG_R2D_C_N<5>	PEG_R2D_C_N<5> - @mlb_lib.MLB	15B3 84B8
PEG_R2D_C_N<6>	PEG_R2D_C_N<6> - @mlb_lib.MLB	15B3 84B8
PEG_R2D_C_N<7>	PEG_R2D_C_N<7> - @mlb_lib.MLB	15B3 84B8
PEG_R2D_C_N<8>	PEG_R2D_C_N<8> - @mlb_lib.MLB	15B3 84B8
PEG_R2D_C_N<9>	PEG_R2D_C_N<9> - @mlb_lib.MLB	15B3 84B8
PEG_R2D_C_N<10>	PEG_R2D_C_N<10> - @mlb_lib.MLB	15B3 84A8
PEG_R2D_C_N<11>	PEG_R2D_C_N<11> - @mlb_lib.MLB	15B3 84A8
PEG_R2D_C_N<12>	PEG_R2D_C_N<12> - @mlb_lib.MLB	15B3 84A8
PEG_R2D_C_N<13>	PEG_R2D_C_N<13> - @mlb_lib.MLB	15B3 84A8
PEG_R2D_C_N<14>	PEG_R2D_C_N<14> - @mlb_lib.MLB	15B3 84A8
PEG_R2D_C_N<15>	PEG_R2D_C_N<15> - @mlb_lib.MLB	15B3 84A8
PEG_R2D_C_P<0>	PEG_R2D_C_P<0> - @mlb_lib.MLB	15B3 84C8
PEG_R2D_C_P<15..0>	PEG_R2D_C_P<15..0> - @mlb_lib.MLB	101D3
PEG_R2D_C_P<1>	PEG_R2D_C_P<1> - @mlb_lib.MLB	15B3 84C8
PEG_R2D_C_P<2>	PEG_R2D_C_P<2> - @mlb_lib.MLB	15B3 84B8
PEG_R2D_C_P<3>	PEG_R2D_C_P<3> - @mlb_lib.MLB	15B3 84B8
PEG_R2D_C_P<4>	PEG_R2D_C_P<4> - @mlb_lib.MLB	15B3 84B8
PEG_R2D_C_P<5>	PEG_R2D_C_P<5> - @mlb_lib.MLB	15B3 84B8
PEG_R2D_C_P<6>	PEG_R2D_C_P<6> - @mlb_lib.MLB	15B3 84B8
PEG_R2D_C_P<7>	PEG_R2D_C_P<7> - @mlb_lib.MLB	15B3 84B8
PEG_R2D_C_P<8>	PEG_R2D_C_P<8> - @mlb_lib.MLB	15B3 84B8
PEG_R2D_C_P<9>	PEG_R2D_C_P<9> - @mlb_lib.MLB	15B3 84B8
PEG_R2D_C_P<10>	PEG_R2D_C_P<10> - @mlb_lib.MLB	15B3 84B8
PEG_R2D_C_P<11>	PEG_R2D_C_P<11> - @mlb_lib.MLB	15B3 84A8
PEG_R2D_C_P<12>	PEG_R2D_C_P<12> - @mlb_lib.MLB	15A3 84A8
PEG_R2D_C_P<13>	PEG_R2D_C_P<13> - @mlb_lib.MLB	15A3 84A8
PEG_R2D_C_P<14>	PEG_R2D_C_P<14> - @mlb_lib.MLB	15A3 84A8
PEG_R2D_C_P<15>	PEG_R2D_C_P<15> - @mlb_lib.MLB	15A3 84A8
PEG_R2D_N<0>	PEG_R2D_N<0> - @mlb_lib.MLB	84A7
PEG_R2D_N<15..0>	PEG_R2D_N<15..0> - @mlb_lib.MLB	101D3
PEG_R2D_N<1>	PEG_R2D_N<1> - @mlb_lib.MLB	84A7
PEG_R2D_N<2>	PEG_R2D_N<2> - @mlb_lib.MLB	84A7
PEG_R2D_N<3>	PEG_R2D_N<3> - @mlb_lib.MLB	84A7
PEG_R2D_N<4>	PEG_R2D_N<4> - @mlb_lib.MLB	84A7
PEG_R2D_N<5>	PEG_R2D_N<5> - @mlb_lib.MLB	84A7
PEG_R2D_N<6>	PEG_R2D_N<6> - @mlb_lib.MLB	84B7
PEG_R2D_N<7>	PEG_R2D_N<7> - @mlb_lib.MLB	84B7
PEG_R2D_N<8>	PEG_R2D_N<8> - @mlb_lib.MLB	84B7
PEG_R2D_N<9>	PEG_R2D_N<9> - @mlb_lib.MLB	84B7
PEG_R2D_N<10>	PEG_R2D_N<10> - @mlb_lib.MLB	84B7
PEG_R2D_N<11>	PEG_R2D_N<11> - @mlb_lib.MLB	84B7
PEG_R2D_N<12>	PEG_R2D_N<12> - @mlb_lib.MLB	84B7
PEG_R2D_N<13>	PEG_R2D_N<13> - @mlb_lib.MLB	84B7
PEG_R2D_N<14>	PEG_R2D_N<14> - @mlb_lib.MLB	84C7
PEG_R2D_N<15>	PEG_R2D_N<15> - @mlb_lib.MLB	84C7
PEG_R2D_P<0>	PEG_R2D_P<0> - @mlb_lib.MLB	84A7
PEG_R2D_P<15..0>	PEG_R2D_P<15..0> - @mlb_lib.MLB	101D3
PEG_R2D_P<1>	PEG_R2D_P<1> - @mlb_lib.MLB	84A7
PEG_R2D_P<2>	PEG_R2D_P<2> - @mlb_lib.MLB	84A7
PEG_R2D_P<3>	PEG_R2D_P<3> - @mlb_lib.MLB	84A7
PEG_R2D_P<4>	PEG_R2D_P<4> - @mlb_lib.MLB	84A7
PEG_R2D_P<5>	PEG_R2D_P<5> - @mlb_lib.MLB	84B7
PEG_R2D_P<6>	PEG_R2D_P<6> - @mlb_lib.MLB	84B7

PEG_R2D_P<7>	PEG_R2D_P<7> - @mlb_lib.MLB	84B7
PEG_R2D_P<8>	PEG_R2D_P<8> - @mlb_lib.MLB	84B7
PEG_R2D_P<9>	PEG_R2D_P<9> - @mlb_lib.MLB	84B7
PEG_R2D_P<10>	PEG_R2D_P<10> - @mlb_lib.MLB	84B7
PEG_R2D_P<11>	PEG_R2D_P<11> - @mlb_lib.MLB	84B7
PEG_R2D_P<12>	PEG_R2D_P<12> - @mlb_lib.MLB	84B7
PEG_R2D_P<13>	PEG_R2D_P<13> - @mlb_lib.MLB	84B7
PEG_R2D_P<14>	PEG_R2D_P<14> - @mlb_lib.MLB	84C7
PEG_R2D_P<15>	PEG_R2D_P<15> - @mlb_lib.MLB	84C7
PEG_RESET_L	PEG_RESET_L - @mlb_lib.MLB	28C1 85C7
PGOOD_0V9_S0	PGOOD_0V9_S0 - @mlb_lib.MLB	70C4 70C4
PGOOD_1V05_S0	PGOOD_1V05_S0 - @mlb_lib.MLB	70B4 73B3
PGOOD_1V5_S0	PGOOD_1V5_S0 - @mlb_lib.MLB	70B4 73B5
PGOOD_1V8_S0	PGOOD_1V8_S0 - @mlb_lib.MLB	70C4 70D4
PGOOD_1V8_S3	PGOOD_1V8_S3 - @mlb_lib.MLB	70D4 75C8
PGOOD_1V25_S0	PGOOD_1V25_S0 - @mlb_lib.MLB	70B4 74B5
PGOOD_3V3_S0	PGOOD_3V3_S0 - @mlb_lib.MLB	70C8 70D4
PGOOD_3V3_S3	PGOOD_3V3_S3 - @mlb_lib.MLB	70D4 76B4
PGOOD_3V3_S5	PGOOD_3V3_S5 - @mlb_lib.MLB	70B4 77D4
	RSMRST_PWRGD - @mlb_lib.MLB	49D8 70B2
PGOOD_5V_S0	PGOOD_5V_S0 - @mlb_lib.MLB	70C4 70C4
PGOOD_5V_S3_L	PGOOD_5V_S3_L - @mlb_lib.MLB	76A6
PGOOD_12V_S0	PGOOD_12V_S0 - @mlb_lib.MLB	70B8 76D5
PGOOD_CR_S0	PGOOD_CR_S0 - @mlb_lib.MLB	70C7
PGOOD_MCH_CORE_S0	PGOOD_MCH_CORE_S0 - @mlb_lib.MLB	70B4 74B3
PGOOD_S0_OUT1	PGOOD_S0_OUT1 - @mlb_lib.MLB	70C3
PLT_RST_L	PLT_RST_L - @mlb_lib.MLB	24A6 28D4
PM_BATLOW_L	PM_BATLOW_L - @mlb_lib.MLB	25A5 25C3 49B8
PM_BMBUSY_L	PM_BMBUSY_L - @mlb_lib.MLB	16B6 25D5
PM_CLKRUN_L	PM_CLKRUN_L - @mlb_lib.MLB	7B8 7D4 25C8 49C5 51B6
PM_DPRSLPVR	PM_DPRSLPVR - @mlb_lib.MLB	16A6 25C3 71C8 100B3
PM_EXTTS_L<0>	PM_EXTTS_L<0> - @mlb_lib.MLB	16B7 31C3 49B8
PM_EXTTS_L<1>	PM_EXTTS_L<1> - @mlb_lib.MLB	16B7 32C3 49B8
PM_LAN_ENABLE	PM_LAN_ENABLE - @mlb_lib.MLB	25C2 49D8
PM_LATRIGGER_L	PM_LATRIGGER_L - @mlb_lib.MLB	13C3 24C8
PM_PWRBTN_L	PM_PWRBTN_L - @mlb_lib.MLB	25C3 49C8
PM_RI_L	PM_RI_L - @mlb_lib.MLB	25A5 25D5
PM_RSMRST_L	PM_RSMRST_L - @mlb_lib.MLB	25C2 49C8
PM_S4_STATE_L	PM_S4_STATE_L - @mlb_lib.MLB	7C4 7D3 25D3 46C8 49C4
		75D8 78D7
PM_S4_STATE_L_SMC	PM_S4_STATE_L_SMC - @mlb_lib.MLB	49C6
PM_SLP_S3_L	PM_SLP_S3_L - @mlb_lib.MLB	6D8 7C4 25D3 49C4 70A8
		75A5 78B4 78B7 78D4
PM_SLP_S3_L_SMC	PM_SLP_S3_L_SMC - @mlb_lib.MLB	49C6
PM_SLP_S3_OD	PM_SLP_S3_OD - @mlb_lib.MLB	6D7
PM_SLP_S5_L	PM_SLP_S5_L - @mlb_lib.MLB	25D3 49C5 50A2
PM_STPCPU_L	PM_STPCPU_L - @mlb_lib.MLB	25C8 29C3 30C2
PM_STPPCI_L	PM_STPPCI_L - @mlb_lib.MLB	25C8 29C3 30C2
PM_SUS_STAT_L	PM_SUS_STAT_L - @mlb_lib.MLB	7C4 7D4 25D5 49C5 50A2
		51B4
PM_SYSRST_L	PM_SYSRST_L - @mlb_lib.MLB	7B8 25D5 28A3 49B8
PM_THRMTRIP_L	PM_THRMTRIP_L - @mlb_lib.MLB	10C6 16A6 23C2 50C3 100B3
PM_THRM_L	PM_THRM_L - @mlb_lib.MLB	25C5
POWER_BUTTON_L	POWER_BUTTON_L - @mlb_lib.MLB	50C7
PP1V0_S5_FW_AVDD	PP1V0_S5_FW_AVDD - @mlb_lib.MLB	40D3 42A6 42D4
PP1V0_S5_FW_DVDD	PP1V0_S5_FW_DVDD - @mlb_lib.MLB	40D6 42B8 42C4
PP1V05_S0_NB_VCCPEG	PP1V05_S0_NB_VCCPEG - @mlb_lib.MLB	15D2 19B3 21D3
	PP1V05_S0_NB_VCCRXRDMI -	19B3 21C3
	@mlb_lib.MLB	
PP1V5_S0_NB_VCCD_TVD	PP1V5_S0_NB_VCCD_TVDAC -	19B6 22B1
AC	@mlb_lib.MLB	
PP1V5_S0_SB_VCCDMIPL	PP1V5_S0_SB_VCCDMIPLL -	26C3 27A6
L	@mlb_lib.MLB	
PP1V5_S0_SB_VCCDMIPL	PP1V5_S0_SB_VCCDMIPLL_F -	27A8
L_F	@mlb_lib.MLB	
PP1V5_S0_SB_VCCSATAP	PP1V5_S0_SB_VCCSATAPLL -	26B6 27A6
LL	@mlb_lib.MLB	
PP1V5_S0_SB_VCCSATAP	PP1V5_S0_SB_VCCSATAPLL_F -	27A8
LL_F	@mlb_lib.MLB	
PP1V8_S3M_NB_VCCSMCK	PP1V8_S3M_NB_VCCSMCK - @mlb_lib.MLB	19B3 21A2
PP1V8_S3M_NB_VCCSMCK	PP1V8_S3M_NB_VCCSMCK_RC -	21A4
_RC	@mlb_lib.MLB	
PP1V8_S3_R	PP1V8_S3_R - @mlb_lib.MLB	75C1
PP1V9_ENET_CTAP	PP1V9_ENET_CTAP - @mlb_lib.MLB	39D7
PP1V9_ENET_PHY_AVDD	PP1V9_ENET_PHY_AVDD - @mlb_lib.MLB	37C6 104B3
PP1V9_S3_ENET	PP1V9_S3_ENET - @mlb_lib.MLB	37C7 38C3 39D8
PP1V25_S0M_NB_MPLL_R	PP1V25_S0M_NB_MPLL_RC -	21C3
C	@mlb_lib.MLB	
PP1V25_S0M_NB_VCCAXD	PP1V25_S0M_NB_VCCAXD - @mlb_lib.MLB	16A2 19C3 21A6
PP1V25_S0M_NB_VCCA_H	PP1V25_S0M_NB_VCCA_HPLL -	19D6 21D1
PLL	@mlb_lib.MLB	
PP1V25_S0M_NB_VCCA_M	PP1V25_S0M_NB_VCCA_MPLL -	19D6 21C1
PLL	@mlb_lib.MLB	
PP1V25_S0M_NB_VCCA_S	PP1V25_S0M_NB_VCCA_SM -	19C6 21B5
M	@mlb_lib.MLB	
PP1V25_S0M_NB_VCCA_S	PP1V25_S0M_NB_VCCA_SM_CK -	19B6 21B5
M_CK	@mlb_lib.MLB	
PP1V25_S0_NB_PEGPLL	PP1V25_S0_NB_PEGPLL - @mlb_lib.MLB	19C6 21B2
PP1V25_S0_NB_PEGPLL_	PP1V25_S0_NB_PEGPLL_RC -	21B4
RC	@mlb_lib.MLB	
PP1V25_S0_NB_VCCAXF	PP1V25_S0_NB_VCCAXF - @mlb_lib.MLB	19C3 21D3
PP3V3_FW_ESD	PP3V3_FW_ESD - @mlb_lib.MLB	43A6 43A6 43B6 43C5 43D5
PP3V3_G3_SB_RTC	PP3V3_G3_SB_RTC - @mlb_lib.MLB	23D7 26D6 27D5 28D5
PP3V3_S0M_CK505_VDD4	PP3V3_S0M_CK505_VDD48 -	29D4
8	@mlb_lib.MLB	
PP3V3_S0M_CK505_VDDA	PP3V3_S0M

SMBUS_SMC_B_S0_SDA	SMBUS_SMC_B_S0_SDA - @mlb_lib.MLB	52B5 106B3
	=SMBUS_MINI_SDA - @mlb_lib.MLB	34B3 52B3
	=SMB_REMOTE_TEMP_SDA - @mlb_lib.MLB	52B3 55B2
	=SMB_CPU_THRM_SDA - @mlb_lib.MLB	52B3 55C4
	SMB_B_S0_DATA - @mlb_lib.MLB	49A5 52B5
	=SMB_REMOTE_TEMP_SDA - @mlb_lib.MLB	52B3 55B2
	=SMB_CPU_THRM_SDA - @mlb_lib.MLB	52B3 55C4
	=SMBUS_MINI_SDA - @mlb_lib.MLB	34B3 52B3
SMBUS_SMC_MGMT_SCL	SMBUS_SMC_MGMT_SCL - @mlb_lib.MLB	52B2 106B3
	SMB_MGMT_CLK - @mlb_lib.MLB	49C5 52B3
SMBUS_SMC_MGMT_SDA	SMBUS_SMC_MGMT_SDA - @mlb_lib.MLB	52B2 106B3
	SMB_MGMT_DATA - @mlb_lib.MLB	49C8 52B3
SMB_CLK	SMB_CLK - @mlb_lib.MLB	25D5 52D8 103A3
	=SMBUS_CK505_SCL - @mlb_lib.MLB	29B5 52D6
	SMBUS_SB_SCL - @mlb_lib.MLB	52D7
	=I2C_DIMMA_SCL - @mlb_lib.MLB	31A6 52D6
	=I2C_DIMMB_SCL - @mlb_lib.MLB	32A6 52C6
	SMBUS_SB_SCL - @mlb_lib.MLB	52D7
	=SMBUS_CK505_SCL - @mlb_lib.MLB	29B5 52D6
	=I2C_DIMMB_SCL - @mlb_lib.MLB	32A6 52C6
	=I2C_DIMMA_SCL - @mlb_lib.MLB	31A6 52D6
SMB_DATA	SMB_DATA - @mlb_lib.MLB	25D5 52D8 103A3
	=SMBUS_CK505_SDA - @mlb_lib.MLB	29B5 52D6
	SMBUS_SB_SDA - @mlb_lib.MLB	52D7
	=I2C_DIMMA_SDA - @mlb_lib.MLB	31A6 52D6
	=I2C_DIMMB_SDA - @mlb_lib.MLB	32A6 52C6
	SMBUS_SB_SDA - @mlb_lib.MLB	52D7
	=SMBUS_CK505_SDA - @mlb_lib.MLB	29B5 52D6
	=I2C_DIMMB_SDA - @mlb_lib.MLB	32A6 52C6
	=I2C_DIMMA_SDA - @mlb_lib.MLB	31A6 52D6
SMB_ME_CLK	SMB_ME_CLK - @mlb_lib.MLB	25D5 52A8 103A3
	SMBUS_SB_ME_SCL - @mlb_lib.MLB	52A7
SMB_ME_DATA	SMB_ME_DATA - @mlb_lib.MLB	25D5 52A8 103A3
	SMBUS_SB_ME_SDA - @mlb_lib.MLB	52A7
SMC_12V_S0_ISENSE	SMC_12V_S0_ISENSE - @mlb_lib.MLB	50B3 53B1
	SMC_DCIN_ISENSE - @mlb_lib.MLB	49C5 50B5
SMC_12V_S0_ISENSE_R	SMC_12V_S0_ISENSE_R - @mlb_lib.MLB	53B2
SMC_12V_S0_VSENSE	SMC_12V_S0_VSENSE - @mlb_lib.MLB	50B3 53B2
	SMC_PBUS_VSENSE - @mlb_lib.MLB	49C5 50B5
SMC_12V_S5_ISENSE	SMC_12V_S5_ISENSE - @mlb_lib.MLB	50B3 53B1
	SMC_BATT_ISENSE - @mlb_lib.MLB	49C5 50B5
SMC_12V_S5_ISENSE_R	SMC_12V_S5_ISENSE_R - @mlb_lib.MLB	53B2
SMC_12V_S5_VSENSE	SMC_12V_S5_VSENSE - @mlb_lib.MLB	50A3 53B3
	SMC_NB_VX25_ISENSE - @mlb_lib.MLB	49C5 50A5
SMC_ADAPTER_EN	SMC_ADAPTER_EN - @mlb_lib.MLB	49D5 50B5
	TP_SMC_ADAPTER_EN - @mlb_lib.MLB	50B3
SMC_BC_ACOK	SMC_BC_ACOK - @mlb_lib.MLB	49C5 50B2
SMC_BS_ALRT_L	SMC_BS_ALRT_L - @mlb_lib.MLB	49C5 50B2
SMC_CASE_OPEN	SMC_CASE_OPEN - @mlb_lib.MLB	49B5 50A2
SMC_CPU_ISENSE	SMC_CPU_ISENSE - @mlb_lib.MLB	49C5 53C6
SMC_CPU_VSENSE	SMC_CPU_VSENSE - @mlb_lib.MLB	49C5 53D6
SMC_EXCARD_CP	SMC_EXCARD_CP - @mlb_lib.MLB	49B8 50A2
SMC_EXCARD_PWR_EN	SMC_EXCARD_PWR_EN - @mlb_lib.MLB	49B8 50B5
	TP_SMC_EXCARD_PWR_EN - @mlb_lib.MLB	50B3
SMC_EXTAL	SMC_EXTAL - @mlb_lib.MLB	49C3 50C8
SMC_FAN_0_CTL	SMC_FAN_0_CTL - @mlb_lib.MLB	49A8 56D8
SMC_FAN_0_TACH	SMC_FAN_0_TACH - @mlb_lib.MLB	49A8 56C8
SMC_FAN_1_CTL	SMC_FAN_1_CTL - @mlb_lib.MLB	49A8 56B8
SMC_FAN_1_TACH	SMC_FAN_1_TACH - @mlb_lib.MLB	49A8 56A8
SMC_FAN_2_CTL	SMC_FAN_2_CTL - @mlb_lib.MLB	49A8 57D8
SMC_FAN_2_TACH	SMC_FAN_2_TACH - @mlb_lib.MLB	49A8 57C8
SMC_FAN_3_CTL	SMC_FAN_3_CTL - @mlb_lib.MLB	49A8 50C5
	TP_SMC_FAN_3_CTL - @mlb_lib.MLB	50C3
SMC_FAN_3_TACH	SMC_FAN_3_TACH - @mlb_lib.MLB	49A8 50C5
	TP_SMC_FAN_3_TACH - @mlb_lib.MLB	50C3
SMC_FWE	SMC_FWE - @mlb_lib.MLB	49A5 50B2
SMC_GFX_OVERTEMP_L	SMC_GFX_OVERTEMP_L - @mlb_lib.MLB	49A8 85C8
SMC_GFX_THROTTLE_L	SMC_GFX_THROTTLE_L - @mlb_lib.MLB	49C8 85B7
SMC_GPU_ISENSE	SMC_GPU_ISENSE - @mlb_lib.MLB	49C5 53C3
SMC_GPU_VSENSE	SMC_GPU_VSENSE - @mlb_lib.MLB	49C5 53D3
SMC_KBC_MDE	SMC_KBC_MDE - @mlb_lib.MLB	49C2
SMC_LID	SMC_LID - @mlb_lib.MLB	49B5 50B2
SMC_LRESET_L	SMC_LRESET_L - @mlb_lib.MLB	7C6 28D1 49C8
SMC_MANUAL_RST_L	SMC_MANUAL_RST_L - @mlb_lib.MLB	50D7
SMC_MD1	SMC_MD1 - @mlb_lib.MLB	7D4 49C1 51B6
SMC_NMI	SMC_NMI - @mlb_lib.MLB	7C4 49C1 51B4
SMC_ODD_DETECT	SMC_ODD_DETECT - @mlb_lib.MLB	44B3 49B8
SMC_ONOFF_L	SMC_ONOFF_L - @mlb_lib.MLB	49C5 50B2 50C5
SMC_P14	SMC_P14 - @mlb_lib.MLB	49D8 50D5
	TP_SMC_P14 - @mlb_lib.MLB	50D3
SMC_P20	SMC_P20 - @mlb_lib.MLB	49C8 50D5
	TP_SMC_P20 - @mlb_lib.MLB	50D3
SMC_P21	SMC_P21 - @mlb_lib.MLB	49C8 50C5
	TP_SMC_P21 - @mlb_lib.MLB	50C3
SMC_P22	SMC_P22 - @mlb_lib.MLB	49C8 50C5
	TP_SMC_P22 - @mlb_lib.MLB	50C3
SMC_P23	SMC_P23 - @mlb_lib.MLB	49C8 50C5
	TP_SMC_P23 - @mlb_lib.MLB	50C3
SMC_P26	SMC_P26 - @mlb_lib.MLB	49C8 50C5
	TP_SMC_P26 - @mlb_lib.MLB	50C3
SMC_P27	SMC_P27 - @mlb_lib.MLB	49C8 50C5
	TP_SMC_P27 - @mlb_lib.MLB	50C3
SMC_P43	SMC_P43 - @mlb_lib.MLB	49C8 50C5
	TP_SMC_P43 - @mlb_lib.MLB	50C3
SMC_P44	SMC_P44 - @mlb_lib.MLB	49C8 50C5
	TP_SMC_P44 - @mlb_lib.MLB	50C3
SMC_P45	SMC_P45 - @mlb_lib.MLB	49C8 50C5
	TP_SMC_P45 - @mlb_lib.MLB	50C3
SMC_P46	SMC_P46 - @mlb_lib.MLB	49B8 50B5
	TP_SMC_P46 - @mlb_lib.MLB	50B3
SMC_P62	SMC_P62 - @mlb_lib.MLB	49D5 50C5
	TP_SMC_P62 - @mlb_lib.MLB	50C3
SMC_P63	SMC_P63 - @mlb_lib.MLB	49D5 50C5
	TP_SMC_P63 - @mlb_lib.MLB	50C3
SMC_P64	SMC_P64 - @mlb_lib.MLB	49D5 50C5
	TP_SMC_P64 - @mlb_lib.MLB	50C3
SMC_P67	SMC_P67 - @mlb_lib.MLB	49C5 50B2
SMC_P81	SMC_P81 - @mlb_lib.MLB	49C5 50C5
	TP_SMC_P81 - @mlb_lib.MLB	50C3
SMC_PA0	SMC_PA0 - @mlb_lib.MLB	49B8 50B2
SMC_PA1	SMC_PA1 - @mlb_lib.MLB	49B8 50B2
SMC_PB0	SMC_PB0 - @mlb_lib.MLB	49B8 50B2
SMC_PF0	SMC_PF0 - @mlb_lib.MLB	49B5 50C5
	TP_SMC_PF0 - @mlb_lib.MLB	50C3
SMC_PF1	SMC_PF1 - @mlb_lib.MLB	49B5 50C5
	TP_SMC_PF1 - @mlb_lib.MLB	50C3
SMC_PF3	SMC_PF3 - @mlb_lib.MLB	49B5 50B2
SMC_PG0	SMC_PG0 - @mlb_lib.MLB	49B5 50B2
SMC_PH4	SMC_PH4 - @mlb_lib.MLB	49A5 50B2
SMC_PM_G2_EN	SMC_PM_G2_EN - @mlb_lib.MLB	49D5 50C5
	TP_SMC_PM_G2_EN - @mlb_lib.MLB	50C3
SMC_PROCHOT	SMC_PROCHOT - @mlb_lib.MLB	49A5 50C1
SMC_PROCHOT_3_3_L	SMC_PROCHOT_3_3_L - @mlb_lib.MLB	49C5 50D1
SMC_RESET_L	SMC_RESET_L - @mlb_lib.MLB	7C4 7C6 49C3 50D6 51B4

SMC_RSTGATE_L	SMC_RSTGATE_L - @mlb_lib.MLB	49D8 50B5
	TP_SMC_RSTGATE_L - @mlb_lib.MLB	50B3
SMC_RUNTIME_SCI_L	SMC_RUNTIME_SCI_L - @mlb_lib.MLB	25C8 49B8
SMC_RX_L	SMC_RX_L - @mlb_lib.MLB	7C4 46D5 49B8 49C5 50B2
		51B4
SMC_SUS_CLK	SMC_SUS_CLK - @mlb_lib.MLB	49C5 50C3
	SUS_CLK_SB - @mlb_lib.MLB	25D3 50C2
SMC_SYS_KBDLED	SMC_SYS_KBDLED - @mlb_lib.MLB	49B8 50B5
	TP_SMC_SYS_KBDLED - @mlb_lib.MLB	50B3
SMC_SYS_LED	SMC_SYS_LED - @mlb_lib.MLB	49C8 50B5
	TP_SMC_SYS_LED - @mlb_lib.MLB	50B3
SMC_TCK	SMC_TCK - @mlb_lib.MLB	7D4 49B5 50B2 51B4
SMC_TDI	SMC_TDI - @mlb_lib.MLB	7D4 49B5 50B2 51B4
SMC_TDO	SMC_TDO - @mlb_lib.MLB	7D4 49B5 50B2 51B6
SMC_THRMTRIP	SMC_THRMTRIP - @mlb_lib.MLB	49A5 50C1
SMC_TMS	SMC_TMS - @mlb_lib.MLB	7D4 49B5 50B2 51B6
SMC_TRST_L	SMC_TRST_L - @mlb_lib.MLB	7D4 49C1 51B6
SMC_TX_L	SMC_TX_L - @mlb_lib.MLB	7D4 46D5 49B8 49C5 50B2
		51B6
SMC_VCL	SMC_VCL - @mlb_lib.MLB	49D2
SMC_WAKE_SCI_L	SMC_WAKE_SCI_L - @mlb_lib.MLB	13C3 25C8 49C5
SMC_XTAL	SMC_XTAL - @mlb_lib.MLB	49C3 50C8
SMS_ONOFF_L	SMS_ONOFF_L - @mlb_lib.MLB	49A5 50B5
	TP_SMS_ONOFF_L - @mlb_lib.MLB	50B3
SMS_X_AXIS	SMS_X_AXIS - @mlb_lib.MLB	49A8 50D5 108D1
	NC_SMS_X_AXIS - @mlb_lib.MLB	50D3
SMS_Y_AXIS	SMS_Y_AXIS - @mlb_lib.MLB	49A8 50D5 108D1
	NC_SMS_Y_AXIS - @mlb_lib.MLB	50D3
SMS_Z_AXIS	SMS_Z_AXIS - @mlb_lib.MLB	49A8 50D5 108D1
	NC_SMS_Z_AXIS - @mlb_lib.MLB	50D3
SPI_A_SCLK_R	SPI_A_SCLK_R - @mlb_lib.MLB	103A3
SPI_A_SI_R	SPI_A_SI_R - @mlb_lib.MLB	61B4 103A3
SPI_A_SO_R	SPI_A_SO_R - @mlb_lib.MLB	7B3 61B4 103A3
SPI_B_SCLK_R	SPI_B_SCLK_R - @mlb_lib.MLB	103A3
SPI_B_SI_R	SPI_B_SI_R - @mlb_lib.MLB	103A3
SPI_B_SO	SPI_B_SO - @mlb_lib.MLB	103A3
SPI_B_SO_R	SPI_B_SO_R - @mlb_lib.MLB	103A3
SPI_CE_L<0>	SPI_CE_L<0> - @mlb_lib.MLB	7B3 61B6 103A3
SPI_CE_L<1>	SPI_CE_L<1> - @mlb_lib.MLB	103A3
SPI_CE_R_L<0>	SPI_CE_R_L<0> - @mlb_lib.MLB	24C5 61B7 103A3
SPI_CE_R_L<1>	SPI_CE_R_L<1> - @mlb_lib.MLB	103A3
SPI_HOLD_L	SPI_HOLD_L - @mlb_lib.MLB	61B5
SPI_SCLK	SPI_SCLK - @mlb_lib.MLB	7A8 61B6 103A3
SPI_SCLK_R	SPI_SCLK_R - @mlb_lib.MLB	24C5 61B7 103A3
SPI_SI	SPI_SI - @mlb_lib.MLB	103A3
SPI_SI_R	SPI_SI_R - @mlb_lib.MLB	24C5 61B3 103A3
SPI_SO	SPI_SO - @mlb_lib.MLB	7A8 24C5 61B3 103A3
SPI_WP_L	SPI_WP_L - @mlb_lib.MLB	61B5
SYS_ONEWIRE	SYS_ONEWIRE - @mlb_lib.MLB	49B8 50B2
TMDS_CLK_N	TMDS_CLK_N - @mlb_lib.MLB	85A7 94D8 108D3
TMDS_CLK_P	TMDS_CLK_P - @mlb_lib.MLB	85A7 94B8 108D3
TMDS_CONN_CLKN	TMDS_CONN_CLKN - @mlb_lib.MLB	94C4 94C7 108D3
TMDS_CONN_CLKP	TMDS_CONN_CLKP - @mlb_lib.MLB	94B7 94C4 108D3
TMDS_CONN_DN<0>	TMDS_CONN_DN<0> - @mlb_lib.MLB	94C4 94D6
TMDS_CONN_DN<3..0>	TMDS_CONN_DN<3..0> - @mlb_lib.MLB	108D3
TMDS_CONN_DN<1>	TMDS_CONN_DN<1> - @mlb_lib.MLB	94C4 94D6
TMDS_CONN_DN<2>	TMDS_CONN_DN<2> - @mlb_lib.MLB	94C6 94D4
TMDS_CONN_DP<0>	TMDS_CONN_DP<0> - @mlb_lib.MLB	94C4 94D6
TMDS_CONN_DP<3..0>	TMDS_CONN_DP<3..0> - @mlb_lib.MLB	108D3
TMDS_CONN_DP<1>	TMDS_CONN_DP<1> - @mlb_lib.MLB	94C4 94D6
TMDS_CONN_DP<2>	TMDS_CONN_DP<2> - @mlb_lib.MLB	94C6 94D4
TMDS_DATA_N<0>	TMDS_DATA_N<0> - @mlb_lib.MLB	85A7 94D8
TMDS_DATA_N<3..0>	TMDS_DATA_N<3..0> - @mlb_lib.MLB	108D3
TMDS_DATA_N<1>	TMDS_DATA_N<1> - @mlb_lib.MLB	85A7 94D8
TMDS_DATA_N<2>	TMDS_DATA_N<2> - @mlb_lib.MLB	85A7 94C8
TMDS_DATA_P<0>	TMDS_DATA_P<0> - @mlb_lib.MLB	85A7 94D8
TMDS_DATA_P<3..0>	TMDS_DATA_P<3..0> - @mlb_lib.MLB	108D3
TMDS_DATA_P<1>	TMDS_DATA_P<1> - @mlb_lib.MLB	85A7 94C8
TMDS_DATA_P<2>	TMDS_DATA_P<2> - @mlb_lib.MLB	85A7 94C8
TP_CK505_PGMODE	TP_CK505_PGMODE - @mlb_lib.MLB	29B5
TP_CPU_RSVD0	TP_CPU_RSVD0 - @mlb_lib.MLB	10B8
TP_CPU_RSVD1	TP_CPU_RSVD1 - @mlb_lib.MLB	10B8
TP_CPU_RSVD2	TP_CPU_RSVD2 - @mlb_lib.MLB	10B8
TP_CPU_RSVD3	TP_CPU_RSVD3 - @mlb_lib.MLB	10B8
TP_CPU_RSVD4	TP_CPU_RSVD4 - @mlb_lib.MLB	10B8
TP_CPU_RSVD5	TP_CPU_RSVD5 - @mlb_lib.MLB	10B8
TP_CPU_RSVD6	TP_CPU_RSVD6 - @mlb_lib.MLB	10B8
TP_CPU_RSVD7	TP_CPU_RSVD7 - @mlb_lib.MLB	10B8
TP_CPU_RSVD8	TP_CPU_RSVD8 - @mlb_lib.MLB	10B8
TP_CPU_RSVD9	TP_CPU_RSVD9 - @mlb_lib.MLB	10B8
TP_CPU_TEST3	TP_CPU_TEST3 - @mlb_lib.MLB	10B4
TP_CPU_TEST5	TP_CPU_TEST5 - @mlb_lib.MLB	10B4
TP_CPU_TEST6	TP_CPU_TEST6 - @mlb_lib.MLB	10B4
TP_ENET_GLAN_CLK	TP_ENET_GLAN_CLK - @mlb_lib.MLB	23C6
TP_FW_AVREG	TP_FW_AVREG - @mlb_lib.MLB	40B6
TP_FW_CE	TP_FW_CE - @mlb_lib.MLB	7B3 40B6
TP_FW_FW620_L	TP_FW_FW620_L - @mlb_lib.MLB	40B6
TP_FW_JASI_EN	TP_FW_JASI_EN - @mlb_lib.MLB	40B6
TP_FW_MODE_A	TP_FW_MODE_A - @mlb_lib.MLB	40B6
TP_FW_NAND_TREE	TP_FW_NAND_TREE - @mlb_lib.MLB	7C3 40B6
TP_FW_SCIFCLK	TP_FW_SCIFCLK - @mlb_lib.MLB	40B3
TP_FW_SCIFDAIN	TP_FW_SCIFDAIN - @mlb_lib.MLB	40B3
TP_FW_SCIFDOUT	TP_FW_SCIFDOUT - @mlb_lib.MLB	40B3
TP_FW_SCIFMC	TP_FW_SCIFMC - @mlb_lib.MLB	40B3
TP_FW_SDA	TP_FW_SDA - @mlb_lib.MLB	40B3
TP_FW_SE	TP_FW_SE - @mlb_lib.MLB	7C3 40B6
TP_FW_SM	TP_FW_SM - @mlb_lib.MLB	7C3 40B6
TP_FW_TCK	TP_FW_TCK - @mlb_lib.MLB	7C3 40C3
TP_FW_TDI	TP_FW_TDI - @mlb_lib.MLB	7C3 40C3
TP_FW_TDO	TP_FW_TDO - @mlb_lib.MLB	7C3 40C3
TP_FW_TMS	TP_FW_TMS - @mlb_lib.MLB	7C3 40C3
TP_FW_VAUX_DISABLE	TP_FW_VAUX_DISABLE - @mlb_lib.MLB	40C3
TP_FW_VBUF	TP_FW_VBUF - @mlb_lib.MLB	40B6
TP_GPU_DDC_B_CLK	TP_GPU_DDC_B_CLK - @mlb_lib.MLB	85A4
TP_GPU_DDC_B_DATA	TP_GPU_DDC_B_DATA - @mlb_lib.MLB	85A4
TP_HDA_DOCK_RST_L	TP_HDA_DOCK_RST_L - @mlb_lib.MLB	23B6
TP_HDA_SDIN1	TP_HDA_SDIN1 - @mlb_lib.MLB	23C8
TP_HDA_SDIN2	TP_HDA_SDIN2 - @mlb_lib.MLB	23C8
TP_HDA_SDIN3	TP_HDA_SDIN3 - @mlb_lib.MLB	23C8
TP_LAN_D2R<0>	TP_LAN_D2R<0> - @mlb_lib.MLB	23C6
TP_LAN_D2R<1>	TP_LAN_D2R<1> - @mlb_lib.MLB	23C6
TP_LAN_D2R<2>	TP_LAN_D2R<2> - @mlb_lib.MLB	23C6 28C4
TP_LAN_R2D<0>	TP_LAN_R2D<0> - @mlb_lib.MLB	23C6
TP_LAN_R2D<1>	TP_LAN_R2D<1> - @mlb_lib.MLB	23C6
TP_LAN_R2D<2>	TP_LAN_R2D<2> - @mlb_lib.MLB	23C6
TP_LAN_RSTSYNC	TP_LAN_RSTSYNC - @mlb_lib.MLB	23C6
TP_LPC_DRQ0_L	TP_LPC_DRQ0_L - @mlb_lib.MLB	23D4
TP_LVDS_A_DATAN3	TP_LVDS_A_DATAN3 - @mlb_lib.MLB	16C6
TP_LVDS_A_DATAP3	TP_LVDS_A_DATAP3 - @mlb_lib.MLB	16C6
TP_LVDS_B_DATAN3	TP_LVDS_B_DATAN3 - @mlb_lib.MLB	16C6
TP_LVDS_B_DATAP3	TP_LVDS_B_DATAP3 - @mlb_lib.MLB	16C6
TP_LVDS_VBG	TP_LVDS_VBG - @mlb_lib.MLB	15D5
TP_MEM_A_A<15>	TP_MEM_A_A<15> - @mlb_lib.MLB	31C3
TP_MEM_A_RCVEN_L	TP_MEM_A_RCVEN_L - @mlb_lib.MLB	17B5

TP_MEM_B_A<15>	TP_MEM_B_A<15> - @mlb_lib.MLB	32C3
TP_MEM_B_RCVEN_L	TP_MEM_B_RCVEN_L - @mlb_lib.MLB	17B2
TP_MEM_CLKN2	TP_MEM_CLKN2 - @mlb_lib.MLB	16C6
TP_MEM_CLKN5	TP_MEM_CLKN5 - @mlb_lib.MLB	16C6
TP_MEM_CLKP2	TP_MEM_CLKP2 - @mlb_lib.MLB	16C6
TP_MEM_CLKP5	TP_MEM_CLKP5 - @mlb_lib.MLB	16C6
TP_NB_CFG<10>	TP_NB_CFG<10> - @mlb_lib.MLB	16B6
TP_NB_CFG<11>	TP_NB_CFG<11> - @mlb_lib.MLB	16B6
TP_NB_CFG<12>	TP_NB_CFG<12> - @mlb_lib.MLB	7C3 16B6
TP_NB_CFG<13>	TP_NB_CFG<13> - @mlb_lib.MLB	7C3 16B6
TP_NB_CFG<14>	TP_NB_CFG<14> - @mlb_lib.MLB	16B6
TP_NB_CFG<15>	TP_NB_CFG<15> - @mlb_lib.MLB	16B6
TP_NB_CFG<17>	TP_NB_CFG<17> - @mlb_lib.MLB	16B6
TP_NB_CFG<18>	TP_NB_CFG<18> - @mlb_lib.MLB	7C3 16B6
TP_NB_NC<1>	TP_NB_NC<1> - @mlb_lib.MLB	16A6
TP_NB_NC<2>	TP_NB_NC<2> - @mlb_lib.MLB	16A6
TP_NB_NC<3>	TP_NB_NC<3> - @mlb_lib.MLB	16A6
TP_NB_NC<4>	TP_NB_NC<4> - @mlb_lib.MLB	16A6
TP_NB_NC<5>	TP_NB_NC<5> - @mlb_lib.MLB	16A6
TP_NB_NC<6>	TP_NB_NC<6> - @mlb_lib.MLB	16A6
TP_NB_NC<7>	TP_NB_NC<7> - @mlb_lib.MLB	16A6
TP_NB_NC<8>	TP_NB_NC<8> - @mlb_lib.MLB	16A6
TP_NB_NC<9>	TP_NB_NC<9> - @mlb_lib.MLB	16A6
TP_NB_NC<10>	TP_NB_NC<10> - @mlb_lib.MLB	16A6
TP_NB_NC<11>	TP_NB_NC<11> - @mlb_lib.MLB	16A6
TP_NB_NC<12>	TP_NB_NC<12> - @mlb_lib.MLB	16A6
TP_NB_NC<13>	TP_NB_NC<13> - @mlb_lib.MLB	16A6
TP_NB_NC<14>	TP_NB_NC<14> - @mlb_lib.MLB	16A6
TP_NB_NC<15>	TP_NB_NC<15> - @mlb_lib.MLB	16A6
TP_NB_NC<16>	TP_NB_NC<16> - @mlb_lib.MLB	16A6
TP_NB_RSVD<1>	TP_NB_RSVD<1> - @mlb_lib.MLB	16D6
TP_NB_RSVD<2>	TP_NB_RSVD<2> - @mlb_lib.MLB	16D6
TP_NB_RSVD<3>	TP_NB_RSVD<3> - @mlb_lib.MLB	16D6
TP_NB_RSVD<4>	TP_NB_RSVD<4> - @mlb_lib.MLB	16D6
TP_NB_RSVD<5>	TP_NB_RSVD<5> - @mlb_lib.MLB	16D6
TP_NB_RSVD<6>	TP_NB_RSVD<6> - @mlb_lib.MLB	16D6
TP_NB_RSVD<7>	TP_NB_RSVD<7> - @mlb_lib.MLB	16D6
TP_NB_RSVD<8>	TP_NB_RSVD<8> - @mlb_lib.MLB	16D6
TP_NB_RSVD<9>	TP_NB_RSVD<9> - @mlb_lib.MLB	16D6
TP_NB_RSVD<10>	TP_NB_RSVD<10> - @mlb_lib.MLB	16D6
TP_NB_RSVD<11>	TP_NB_RSVD<11> - @mlb_lib.MLB	16D6
TP_NB_RSVD<12>	TP_NB_RSVD<12> - @mlb_lib.MLB	16D6
TP_NB_RSVD<13>	TP_NB_RSVD<13> - @mlb_lib.MLB	16D6
TP_NB_RSVD<14>	TP_NB_RSVD<14> - @mlb_lib.MLB	16D6
TP_NB_RSVD<20>	TP_NB_RSVD<20> - @mlb_lib.MLB	16D6
TP_NB_RSVD<21>	TP_NB_RSVD<21> - @mlb_lib.MLB	16D6
TP_NB_RSVD<22>	TP_NB_RSVD<22> - @mlb_lib.MLB	16C6
TP_NB_RSVD<23>	TP_NB_RSVD<23> - @mlb_lib.MLB	16C6
TP_NB_RSVD<24>	TP_NB_RSVD<24> - @mlb_lib.MLB	16C6
TP_NB_RSVD<25>	TP_NB_RSVD<25> - @mlb_lib.MLB	16C6
TP_NB_RSVD<26>	TP_NB_RSVD<26> - @mlb_lib.MLB	16C6
TP_NB_RSVD<27>	TP_NB_RSVD<27> - @mlb_lib.MLB	16C6
TP_NB_RSVD<34>	TP_NB_RSVD<34> - @mlb_lib.MLB	16C6
TP_NB_RSVD<35>	TP_NB_RSVD<35> - @mlb_lib.MLB	16C6
TP_NB_RSVD<36>	TP_NB_RSVD<36> - @mlb_lib.MLB	16C6
TP_NB_RSVD<41>	TP_NB_RSVD<41> - @mlb_lib.MLB	16C6
TP_NB_RSVD<42>	TP_NB_RSVD<42> - @mlb_lib.MLB	16C6
TP_NB_RSVD<43>	TP_NB_RSVD<43> - @mlb_lib.MLB	16C6
TP_NB_RSVD<44>	TP_NB_RSVD<44> - @mlb_lib.MLB	16C6
TP_NB_RSVD<45>	TP_NB_RSVD<45> - @mlb_lib.MLB	16C6
TP_PCIE_A_D2R_N	TP_PCIE_A_D2R_N - @mlb_lib.MLB	24D5
TP_PCIE_A_D2R_P	TP_PCIE_A_D2R_P - @mlb_lib.MLB	24D5
TP_PCIE_A_R2D_C_N	TP_PCIE_A_R2D_C_N - @mlb_lib.MLB	24D5
TP_PCIE_A_R2D_C_P	TP_PCIE_A_R2D_C_P - @mlb_lib.MLB	24D5
TP_PCIE_B_D2R_N	TP_PCIE_B_D2R_N - @mlb_lib.MLB	24D5
TP_PCIE_B_D2R_P	TP_PCIE_B_D2R_P - @mlb_lib.MLB	24D5
TP_PCIE_B_R2D_C_N	TP_PCIE_B_R2D_C_N - @mlb_lib.MLB	24D5
TP_PCIE_B_R2D_C_P	TP_PCIE_B_R2D_C_P - @mlb_lib.MLB	24D5
TP_PCIE_EXCARD_D2R_N	TP_PCIE_EXCARD_D2R_N - @mlb_lib.MLB	24D5
TP_PCIE_EXCARD_D2R_P	TP_PCIE_EXCARD_D2R_P - @mlb_lib.MLB	24D5
TP_PCIE_EXCARD_R2D_C_N	TP_PCIE_EXCARD_R2D_C_N - @mlb_lib.MLB	24D5
TP_PCIE_EXCARD_R2D_C_P	TP_PCIE_EXCARD_R2D_C_P - @mlb_lib.MLB	24D5
TP_PCI_PME_L	TP_PCI_PME_L - @mlb_lib.MLB	24A6
TP_PM_SLP_M_L	TP_PM_SLP_M_L - @mlb_lib.MLB	25C3
TP_PM_SLP_S4_L	TP_PM_SLP_S4_L - @mlb_lib.MLB	25D3
TP_PP5VREG_PLLIN	TP_PP5VREG_PLLIN - @mlb_lib.MLB	76B5
TP_SB_GPIO51	TP_SB_GPIO51 - @mlb_lib.MLB	24B6
TP_SB_GPIO53	TP_SB_GPIO53 - @mlb_lib.MLB	24B6
TP_SB_GPIO55	TP_SB_GPIO55 - @mlb_lib.MLB	24B6
TP_SB_TP3	TP_SB_TP3 - @mlb_lib.MLB	25B5
TP_SB_TP7	TP_SB_TP7 - @mlb_lib.MLB	25C5
TP_SB_TP8	TP_SB_TP8 - @mlb_lib.MLB	23C4
TP_SPI_CE_R_L<1>	TP_SPI_CE_R_L<1> - @mlb_lib.MLB	24C5
TP_VCCCL1_05_INTERNA L_REG	TP_VCCCL1_05_INTERNAL_REG - @mlb_lib.MLB	26A3
TP_VCCLAN1_05_INTERN AL_REG1	TP_VCCLAN1_05_INTERNAL_REG1 - @mlb_lib.MLB	26A6
TP_VCCLAN1_05_INTERN AL_REG2	TP_VCCLAN1_05_INTERNAL_REG2 - @mlb_lib.MLB	26A6
TP_VCCSUS1_05_INTERN AL_REG1	TP_VCCSUS1_05_INTERNAL_REG1 - @mlb_lib.MLB	26B3
TP_VCCSUS1_05_INTERN AL_REG2	TP_VCCSUS1_05_INTERNAL_REG2 - @mlb_lib.MLB	26B3
TP_VCCSUS1_5_INTERNA L_REG1	TP_VCCSUS1_5_INTERNAL_REG1 - @mlb_lib.MLB	26B3
TP_VCCSUS1_5_INTERNA L_REG2	TP_VCCSUS1_5_INTERNAL_REG2 - @mlb_lib.MLB	26B3
TP_XDP_HOOK2	TP_XDP_HOOK2 - @mlb_lib.MLB	13B6
TP_XDP_HOOK3	TP_XDP_HOOK3 - @mlb_lib.MLB	13B6
U5500_TCRIT1	U5500_TCRIT1 - @mlb_lib.MLB	55B3
U5500_TCRIT2	U5500_TCRIT2 - @mlb_lib.MLB	55B3
U5500_TCRIT3	U5500_TCRIT3 - @mlb_lib.MLB	55A3
U7550_VDDQ	U7550_VDDQ - @m

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C600	CAP_402	mlb[6D7]
C623	CAP_805	mlb[6D7]
C624	CAP_1210	mlb[6D8]
C625	CAP_P_6.3X5.5-SM	mlb[6D8]
C626	CAP_402	mlb[6D8]
C627	CAP_402	mlb[6D8]
C628	CAP_402	mlb[6D6]
C629	CAP_402	mlb[6D7]
C630	CAP_402	mlb[6D6]
C631	CAP_402	mlb[6D6]
C701	CAP_402	mlb[7C6]
C702	CAP_402	mlb[7C5]
C703	CAP_402	mlb[7C6]
C704	CAP_402	mlb[7C5]
C1000	CAP_402	mlb[10B5]
C1200	CAP_805	mlb[12D7]
C1201	CAP_805	mlb[12D6]
C1202	CAP_805	mlb[12D6]
C1203	CAP_805	mlb[12D6]
C1204	CAP_805	mlb[12D6]
C1205	CAP_805	mlb[12D5]
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C1208	CAP_805	mlb[12D4]
C1209	CAP_805	mlb[12D4]
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C1211	CAP_805	mlb[12C6]
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C1213	CAP_805	mlb[12C6]
C1214	CAP_805	mlb[12C6]
C1215	CAP_805	mlb[12C5]
C1216	CAP_805	mlb[12C5]
C1217	CAP_805	mlb[12C5]
C1218	CAP_805	mlb[12C4]
C1219	CAP_805	mlb[12C4]
C1220	CAP_805	mlb[12C7]
C1221	CAP_805	mlb[12C6]
C1222	CAP_805	mlb[12C6]
C1223	CAP_805	mlb[12C6]
C1224	CAP_805	mlb[12C6]
C1225	CAP_805	mlb[12C5]
C1226	CAP_805	mlb[12B7]
C1227	CAP_805	mlb[12B6]
C1228	CAP_805	mlb[12B6]
C1229	CAP_805	mlb[12B6]
C1230	CAP_805	mlb[12B6]
C1231	CAP_805	mlb[12B5]
C1235	CAP_P_6.3X8-SM	mlb[12A3]
C1236	CAP_402	mlb[12A2]
C1237	CAP_402	mlb[12A2]
C1238	CAP_402	mlb[12A2]
C1239	CAP_402	mlb[12A2]
C1240	CAP_402	mlb[12A1]
C1241	CAP_402	mlb[12A1]
C1250	CAP_P_CASE-D2-SM1	mlb[12B7]
C1251	CAP_P_CASE-D2-SM1	mlb[12B6]
C1252	CAP_P_CASE-D2-SM1	mlb[12B5]
C1253	CAP_P_CASE-D2-SM1	mlb[12B5]
C1254	CAP_P_CASE-D2-SM1	mlb[12B6]
C1255	CAP_P_CASE-D2-SM1	mlb[12B5]
C1280	CAP_603	mlb[12B3]
C1281	CAP_402	mlb[12B2]
C1300	CAP_402	mlb[13B5]
C1301	CAP_402	mlb[13B4]
C1410	CAP_402	mlb[14A6]
C1425	CAP_402	mlb[14A7]
C1615	CAP_402	mlb[16C3]
C1616	CAP_402	mlb[16C3]
C1622	CAP_603	mlb[16C1]
C1623	CAP_402	mlb[16C1]
C1624	CAP_603	mlb[16C1]
C1625	CAP_402	mlb[16C1]
C1640	CAP_402	mlb[16A3]
C1801	CAP_402	mlb[18A4]
C1802	CAP_402	mlb[18A4]
C1803	CAP_402	mlb[18A4]
C1804	CAP_402	mlb[18A4]
C1805	CAP_402	mlb[18A5]
C1806	CAP_402	mlb[18A5]
C1807	CAP_402	mlb[18A5]
C1911	CAP_402	mlb[19A3]
C1912	CAP_402	mlb[19A3]
C1913	CAP_402	mlb[19A3]
C2100	CAP_P_6.3X8-SM	mlb[21D7]
C2101	CAP_805	mlb[21D7]
C2102	CAP_402	mlb[21D7]
C2103	CAP_402	mlb[21D6]
C2104	CAP_402	mlb[21D6]
C2110	CAP_805	mlb[21C7]
C2111	CAP_402	mlb[21C7]
C2112	CAP_402	mlb[21C7]
C2113	CAP_402	mlb[21C6]
C2114	CAP_402	mlb[21C6]
C2115	CAP_402	mlb[21C6]
C2120	CAP_P_6.3X8-SM	mlb[21C7]
C2121	CAP_603	mlb[21C7]
C2122	CAP_603	mlb[21C7]
C2123	CAP_603	mlb[21C6]
C2124	CAP_402	mlb[21C6]
C2130	CAP_P_6.3X8-SM	mlb[21C7]
C2131	CAP_805	mlb[21C7]
C2132	CAP_805	mlb[21C7]
C2135	CAP_402	mlb[21C7]
C2140	CAP_P_6.3X8-SM	mlb[21B7]
C2141	CAP_805	mlb[21B7]
C2142	CAP_805	mlb[21B6]
C2143	CAP_603	mlb[21B6]
C2144	CAP_402-1	mlb[21B6]
C2145	CAP_805	mlb[21B6]
C2146	CAP_603	mlb[21B6]
C2148	CAP_402	mlb[21B6]
C2150	CAP_805	mlb[21A7]
C2151	CAP_402-1	mlb[21A6]
C2160	CAP_402	mlb[21A7]
C2161	CAP_402	mlb[21A7]
C2165	CAP_402	mlb[21A7]
C2170	CAP_603	mlb[21D4]
C2171	CAP_402-1	mlb[21D4]
C2173	CAP_P_SM-CASE-C1	mlb[21C4]
C2174	CAP_603	mlb[21C4]
C2177	CAP_603	mlb[21C4]
C2180	CAP_402	mlb[21D2]
C2181	CAP_805	mlb[21D2]
C2182	CAP_402	mlb[21D2]
C2183	CAP_805	mlb[21C3]
C2184	CAP_402	mlb[21C2]
C2190	CAP_603	mlb[21B4]
C2191	CAP_402	mlb[21B3]
C2192	CAP_402	mlb[21B3]
C2195	CAP_603	mlb[21A4]
C2196	CAP_805	mlb[21A3]
C2197	CAP_402	mlb[21A3]
C2200	CAP_402	mlb[22B2]
C2201	FILTER_3P_A_NFM18	mlb[22B2]
C2213	CAP_603	mlb[22B2]
C2500	CAP_402	mlb[25C2]
C2501	CAP_402	mlb[25B2]
C2600	CAP_402	mlb[26A3]
C2601	CAP_402	mlb[26A3]
C2700	CAP_P_SM-CASE-C1	mlb[27C7]
C2701	CAP_402	mlb[27A6]
C2702	CAP_402	mlb[27B1]
C2703	CAP_402-1	mlb[27C8]
C2704	CAP_402	mlb[27D8]
C2705	CAP_805	mlb[27C7]
C2706	CAP_805	mlb[27C7]
C2707	CAP_603	mlb[27C7]
C2708	CAP_603	mlb[27A6]
C2711	CAP_402	mlb[27D1]
C2712	CAP_402	mlb[27C1]
C2714	CAP_402	mlb[27D1]
C2715	CAP_402	mlb[27C1]
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C2719	CAP_402	mlb[27D3]
C2721	CAP_402	mlb[27B3]
C2722	CAP_402	mlb[27B1]
C2723	CAP_402	mlb[27B1]
C2724	CAP_603	mlb[27B1]
C2725	CAP_402	mlb[27D3]
C2726	CAP_402	mlb[27C3]
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C2728	CAP_402	mlb[27C3]
C2729	CAP_402	mlb[27D5]
C2730	CAP_402	mlb[27D5]
C2731	CAP_402	mlb[27D5]
C2732	CAP_603	mlb[27B7]
C2733	CAP_603	mlb[27C5]
C2734	CAP_402	mlb[27D5]
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C2736	CAP_603	mlb[27B7]
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C2738	CAP_402	mlb[27C3]
C2739	CAP_805	mlb[27C1]
C2741	CAP_402	mlb[27B3]
C2805	CAP_402	mlb[28D5]
C2808	CAP_402	mlb[28C6]
C2809	CAP_402	mlb[28C6]
C2810	CAP_402	mlb[28D6]
C2811	CAP_402	mlb[28A7]
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C2903	CAP_402	mlb[29D6]
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C2905	CAP_402	mlb[29D5]
C2906	CAP_402	mlb[29D5]
C2907	CAP_603	mlb[29C5]
C2908	CAP_402	mlb[29C5]
C2909	CAP_402	mlb[29D4]
C2910	CAP_603	mlb[29D3]
C2911	CAP_402	mlb[29D2]
C2912	CAP_402	mlb[29D4]
C2913	CAP_402	mlb[29D3]
C2914	CAP_603	mlb[29D3]
C2915	CAP_402	mlb[29C4]
C2916	CAP_603	mlb[29C3]
C2989	CAP_402	mlb[29C6]
C2990	CAP_402	mlb[29C6]
C3100	CAP_603	mlb[31B2]
C3101	CAP_603	mlb[31B2]
C3110	CAP_402	mlb[31B2]
C3111	CAP_402	mlb[31B2]
C3112	CAP_402	mlb[31B1]
C3113	CAP_402	mlb[31B1]
C3114	CAP_402	mlb[31B2]
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C3118	CAP_402	mlb[31B2]
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C3120	CAP_402	mlb[31B1]
C3121	CAP_402	mlb[31B1]
C3122	CAP_402	mlb[31A1]
C3123	CAP_402	mlb[31A1]
C3130	CAP_603	mlb[31D6]
C3131	CAP_402	mlb[31D6]
C3140	CAP_603	mlb[31A7]
C3141	CAP_402	mlb[31A6]
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C3210	CAP_402	mlb[32B2]
C3211	CAP_402	mlb[32B2]
C3212	CAP_402	mlb[32B1]
C3213	CAP_402	mlb[32B1]
C3214	CAP_402	mlb[32B2]
C3215	CAP_402	mlb[32B2]
C3216	CAP_402	mlb[32B1]
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C3219	CAP_402	mlb[32B2]
C3220	CAP_402	mlb[32B1]
C3221	CAP_402	mlb[32B1]
C3222	CAP_402	mlb[32A1]
C3223	CAP_402	mlb[32A1]
C3230	CAP_603	mlb[32D6]
C3231	CAP_402	mlb[32D6]
C3240	CAP_603	mlb[32A6]
C3241	CAP_402	mlb[32A6]
C3300	CAP_402	mlb[33D4]
C3302	CAP_402	mlb[33D4]
C3305	CAP_402	mlb[33D4]
C3307	CAP_402	mlb[33D4]
C3310	CAP_402	mlb[33C4]
C3312	CAP_402	mlb[33C4]
C3330	CAP_402	mlb[33C4]
C3332	CAP_402	mlb[33C4]
C3334	CAP_402	mlb[33C4]
C3336	CAP_402	mlb[33C4]
C3338	CAP_402	mlb[33C4]
C3340	CAP_402	mlb[33C4]
C3342	CAP_402	mlb[33B4]
C3344	CAP_402	mlb[33B4]
C3346	CAP_402	mlb[33B4]
C3348	CAP_402	mlb[33B4]
C3350	CAP_402	mlb[33B4]
C3352	CAP_402	mlb[33B4]
C3354	CAP_402	mlb[33B4]
C3356	CAP_402	mlb[33B4]
C3358	CAP_402	mlb[33A4]
C3360	CAP_402	mlb[33A4]
C3362	CAP_402	mlb[33A4]
C3364	CAP_402	mlb[33A4]
C3366	CAP_402	mlb[33A4]
C3368	CAP_402	mlb[33A4]
C3370	CAP_402	mlb[33A4]
C3400	CAP_402	mlb[34C3]
C3401	CAP_603	mlb[34C3]
C3410	CAP_402	mlb[34C3]
C3420	CAP_402	mlb[34C3]
C3421	CAP_603	mlb[34C3]
C3430	CAP_402	mlb[34B7]
C3431	CAP_402	mlb[34B7]
C3700	CAP_603	mlb[37D6]
C3701	CAP_402	mlb[37D6]
C3702	CAP_402	mlb[37D5]
C3703	CAP_402	mlb[37D5]
C3704	CAP_402	mlb[37D5]
C3705	CAP_402	mlb[37D4]
C3706	CAP_402	mlb[37D4]
C3707	CAP_402	mlb[37D4]
C3708	CAP_402	mlb[37D3]
C3710	CAP_603	mlb[37D6]
C3711	CAP_402	mlb[37D6]
C3712	CAP_402	mlb[37D5]
C3713	CAP_402	mlb[37D5]
C3714	CAP_402	mlb[37D5]
C3715	CAP_402	mlb[37D4]
C3720	CAP_603	mlb[37C5]
C3721	CAP_402	mlb[37C5]
C3722	CAP_402	mlb[37C5]
C3723	CAP_402	mlb[37C4]
C3724	CAP_402	mlb[37C4]
C3730	CAP_402	mlb[37C7]
C3731	CAP_402	mlb[37C7]
C3735	CAP_402	mlb[37C5]
C3736	CAP_402	mlb[37C5]
C3740	CAP_402	mlb[37B7]
C3742	CAP_402	mlb[37B6]
C3744	CAP_402	mlb[37B6]
C3746	CAP_402	mlb[37B5]
C3750	CAP_402	mlb[37B5]
C3751	CAP_402	mlb[37B5]
C3780	CAP_402	mlb[37B2]
C3800	CAP_805	mlb[38C6]
C3801	CAP_402	mlb[38C6]
C3802	CAP_805	mlb[38C6]
C3803	CAP_603	mlb[38C5]
C3804	CAP_402	mlb[38C5]
C3805	CAP_603	mlb[38C4]
C3810	CAP_805	mlb[38B6]
C3811	CAP_402	mlb[38B6]
C3812	CAP_805	mlb[38B6]
C3813	CAP_603	mlb[38B5]
C3814	CAP_402	mlb[38B5]
C3815	CAP_603	mlb[38A4]
C3816	CAP_402	mlb[38A4]
C3900	CAP_402	mlb[39D7]
C3901	CAP_402	mlb[39D7]
C3902	CAP_402	mlb[39D6]
C3903	CAP_402	mlb[39D6]
C3910	CAP_1808	mlb[39A3]
C4000	CAP_402	mlb[40B7]
C4001	CAP_402	mlb[40B7]
C4010	CAP_402	mlb[40C2]
C4011	CAP_402	mlb[40C2]
C4020	CAP_402	mlb[40C3]
C4021	CAP_402	mlb[40C3]
C4090	CAP_402	mlb[40B6]
C4200	CAP_402-LF	mlb[42C7]
C4201	CAP_402-LF	mlb[42C7]
C4210	CAP_402	mlb[42C6]
C4211	CAP_402	mlb[42C5]
C4212	CAP_805-1	mlb[42C5]
C4213	CAP_805-1	mlb[42C5]
C4230	CAP_402	mlb[42A5]
C4231	CAP_402	mlb[42A5]
C4240	CAP_402	mlb[42A7]
C4241	CAP_402	mlb[42A7]
C4242	CAP_402	mlb[42A7]
C4250	CAP_402	mlb[42B7]
C4251	CAP_402	mlb[42B7]
C4252	CAP_402	mlb[42B7]
C4253	CAP_402	mlb[42B6]
C4254	CAP_402	mlb[42B6]
C4260	CAP_402	mlb[42B7]
C4261	CAP_402	mlb[42B7]
C4262	CAP_402	mlb[42B7]
C4263	CAP_402	mlb[42B6]
C4264	CAP_402	mlb[42B6]
C4265	CAP_402	mlb[42B6]
C4266	CAP_402	mlb[42B6]
C4280	CAP_402	mlb[42A6]
C4281	CAP_402	mlb[42A6]
C4290	CAP_402	mlb[42B5]
C4291	CAP_402	mlb[42B5]
C4300	CAP_603-1	mlb[43D3]
C4301	CAP_603-1	mlb[43B3]
C4310	CAP_402	mlb[43D4]
C4311	CAP_402	mlb[43D4]
C4312	CAP_402	mlb[43C4]
C4313	CAP_402	mlb[43C4]
C4320	CAP_402	mlb[43B5]
C4321	CAP_402	mlb[43B5]
C4322	CAP_402	mlb[43A5]
C4323	CAP_402	mlb[43A5]
C4332	CAP_402	mlb[43C2]
C4335	CAP_603-1	mlb[43C2]
C4350	CAP_402	mlb[43C7]
C4354	CAP_402	mlb[43B7]
C4360	CAP_402	mlb[43D7]
C4364	CAP_402	mlb[43B7]
C4404	CAP_402	mlb[44B6]
C4405	CAP_402	mlb[44B3]
C4406	CAP_805	mlb[44B3]
C4510	CAP_402	mlb[45D6]
C4511	CAP_402	mlb[45D6]
C4515	CAP_402	mlb[45C6]
C4516	CAP_402	mlb[45C6]
C4600	CAP_P_CASE-D2-LF	mlb[46C8]
C4601	CAP_402	mlb[46C8]
C4602	CAP_402	mlb[46C7]
C4603	CAP_402	mlb[46C7]
C4604	CAP_402	mlb[46D8]
C4605	CAP_402	mlb[46D7]
C4613	CAP_402	mlb[46D2]
C4623	CAP_402	mlb[46C5]
C4633	CAP_402	mlb[46A5]
C4650	CAP_402	mlb[46D5]
C4700	CAP_805-1	mlb[47D7]
C4701	CAP_402	mlb[47D6]
C4720	CAP_805-1	mlb[47D3]
C4721	CAP_402	mlb[47D3]
C4781	CAP_402	mlb[47A2]
C4902	CAP_805	mlb[49D4]
C4903	CAP_402	mlb[49D4]
C4904	CAP_402	mlb[49D3]
C4905	CAP_402	mlb[49D3]
C4906	CAP_402	mlb[49D3]
C4907	CAP_402	mlb[49D2]
C4920	CAP_402	mlb[49C3]
C5000	CAP_402	mlb[50D7]
C5001	CAP_402	mlb[50D7]
C5010	CAP_402	mlb[50C6]
C5020	CAP_402	mlb[50C7]
C5021	CAP_402	mlb[50C7]
C5065	CAP_402	mlb[50B8]
C5066	CAP_603	mlb[50B7]
C5067	CAP_402	mlb[50B7]
C5309	CAP_402	mlb[53D6]
C5359	CAP_402	mlb[53D3]
C5370	CAP_402	mlb[53C7]
C5380	CAP_402	mlb[53C5]
C5381	CAP_402	mlb[53C4]
C5382	CAP_402	mlb[53B3]
C5383	CAP_402	mlb[53B1]
C5384	CAP_402	mlb[53B1]
C5386	CAP_402	mlb[53A4]
C5388	CAP_402	mlb[53A3]
C5500	CAP_402	mlb[55C7]
C5501	CAP_402	mlb[55B4]
C5502	CAP_805-1	mlb[55B4]
C5503	CAP_402	mlb[55B4]
C5510	CAP_402	mlb[55A7]
C5511	CAP_402	mlb[55A6]
C5550	CAP_402	mlb[55B7]
C5551	CAP_402	mlb[55B6]
C5560	CAP_402	mlb[55C5]
C5570	CAP_402	mlb[55D3]
C5580	CAP_402	mlb[55C4]
C5601	CAP_805	mlb[56D5]
C5602	CAP_P_6.3X5.5SM1	mlb[56C4]
C5603	CAP_805	mlb[56B5]
C5605	CAP_P_6.3X5.5SM1	mlb[56B3]
C5701	CAP_805	mlb[57C5]
C5702	CAP_P_6.3X5.5SM1	mlb[57C3]
C6100	CAP_402	mlb[61C4]
C7000	CAP_402	mlb[70C6]
C7001	CAP_402	mlb[70C6]
C7002	CAP_402	mlb[70C6]
C7003	CAP_402	mlb[70C6]
C7010	CAP_603	mlb[70D6]
C7052	CAP_402	mlb[70D2]
C7056	CAP_402	mlb[70D1]
C7060	CAP_402	mlb[70A5]
C7061	CAP_402	mlb[70B5]
C7062	CAP_402	mlb[70B5]
C7090	CAP_402	mlb[70A3]
C7100	CAP_402	mlb[71C4]
C7101	CAP_1206-1	mlb[71D1]
C7102	CAP_402	mlb[71B4]
C7103	CAP_402	mlb[71C2]
C7104	CAP_402	mlb[71B2]
C7105	CAP_402	mlb[71C8]
C7106	CAP_402	mlb[71B8]
C7107	CAP_402	mlb[71B7]
C7108	CAP_1206-1	mlb[71D1]
C7109	CAP_P_TH	mlb[71D5]
C7110	CAP_402	mlb[71C7]
C7111	CAP_402	mlb[71B2]
C7112	CAP_402	mlb[71C2]
C7113	CAP_402	mlb[71B7]
C7114	CAP_402	mlb[71B8]
C7115	CAP_603	mlb[71D4]
C7116	CAP_402	mlb[71B4]
C7121	CAP_402	mlb[71A5]
C7126	CAP_603-1	mlb[71D6]
C7127	CAP_603	mlb[71C4]
C7128	CAP_402	mlb[71B4]
C7129	CAP_402	mlb[71B5]
C7130	CAP_402	mlb[71D6]
C7131	CAP_402	mlb[71B5]
C7132	CAP_402	mlb[71A5]
C7133	CAP_402	mlb[71A5]
C7134	CAP_402	mlb[71B5]
C7135	CAP_603	mlb[71D4]
C7136	CAP_603	mlb[71C4]
C7145	CAP_402	mlb[71D1]
C7146	CAP_402	mlb[71C1]
C7147	CAP_402	mlb[71D3]
C7148	CAP_402	mlb[71C3]
C7150	CAP_1206-1	mlb[71D4]
C7152	CAP_1206-1	mlb[71D4]
C7154	CAP_P_TH	mlb[71D2]
C7155	CAP_1206-1	mlb[71D1]
C7156	CAP_1206-1	mlb[71D4]
C7190	CAP_402	mlb[71C3]
C7192	CAP_402	mlb[71B3]
C7196	CAP_402	mlb[71D6]
C7200	CAP_402	mlb[72C4]
C7201	CAP_1206-1	mlb[72D2]

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C7203	CAP_402	mlb[72C2]
C7208	CAP_1206-1	mlb[72D2]
C7212	CAP_402	mlb[72C3]
C7215	CAP_603	mlb[72C5]
C7235	CAP_603	mlb[72D6]
C7245	CAP_402	mlb[72C2]
C7247	CAP_402	mlb[72D4]
C7254	CAP_P_TH	mlb[72D2]
C7255	CAP_1206-1	mlb[72D2]
C7290	CAP_402	mlb[72C4]
C7300	CAP_P_CASE-D2-SM	mlb[73C8]
C7301	CAP_805	mlb[73B8]
C7302	CAP_402	mlb[73B7]
C7303	CAP_805	mlb[73C7]
C7304	CAP_805	mlb[73C8]
C7305	CAP_805	mlb[73C7]
C7310	CAP_603	mlb[73C7]
C7324	CAP_402	mlb[73B7]
C7330	CAP_603-1	mlb[73D6]
C7331	CAP_603	mlb[73C6]
C7332	CAP_402	mlb[73B5]
C7335	CAP_402	mlb[73B6]
C7340	CAP_P_TH	mlb[73D7]
C7341	CAP_1206-1	mlb[73D7]
C7342	CAP_1206-1	mlb[73D6]
C7345	CAP_402	mlb[73B3]
C7360	CAP_603	mlb[73D2]
C7361	CAP_603	mlb[73C2]
C7364	CAP_402	mlb[73B2]
C7370	CAP_402	mlb[73B2]
C7372	CAP_402	mlb[73B4]
C7381	CAP_1206-1	mlb[73D2]
C7382	CAP_1206-1	mlb[73D2]
C7390	CAP_P_CASE-D2-SM	mlb[73C1]
C7391	CAP_P_CASE-D2-SM	mlb[73C2]
C7392	CAP_805	mlb[73C1]
C7393	CAP_805	mlb[73C1]
C7400	CAP_P_CASE-D2-SM	mlb[74C8]
C7401	CAP_805	mlb[74C8]
C7402	CAP_402	mlb[74B7]
C7403	CAP_P_CASE-D2-SM	mlb[74C7]
C7404	CAP_805	mlb[74C8]
C7410	CAP_603	mlb[74C7]
C7424	CAP_402	mlb[74B7]
C7430	CAP_603-1	mlb[74D6]
C7431	CAP_603	mlb[74C6]
C7432	CAP_402	mlb[74B5]
C7435	CAP_402	mlb[74B6]
C7440	CAP_P_TH	mlb[74D7]
C7441	CAP_1206-1	mlb[74D7]
C7442	CAP_1206-1	mlb[74D6]
C7445	CAP_402	mlb[74B3]
C7460	CAP_603-1	mlb[74D2]
C7461	CAP_603	mlb[74C2]
C7464	CAP_402	mlb[74B2]
C7470	CAP_402	mlb[74B2]
C7472	CAP_402	mlb[74B4]
C7480	CAP_P_TH	mlb[74D3]
C7481	CAP_1206-1	mlb[74D2]
C7482	CAP_1206-1	mlb[74D2]
C7490	CAP_P_TH1	mlb[74C2]
C7491	CAP_P_TH1	mlb[74C1]
C7492	CAP_805	mlb[74C1]
C7493	CAP_805	mlb[74C1]
C7500	CAP_603	mlb[75D5]
C7501	CAP_603	mlb[75D6]
C7502	CAP_603	mlb[75D6]
C7503	CAP_402	mlb[75C2]
C7506	CAP_402	mlb[75C8]
C7507	CAP_402	mlb[75C6]
C7508	CAP_603	mlb[75C7]
C7509	CAP_402	mlb[75D4]
C7510	CAP_402	mlb[75C5]
C7530	CAP_P_TH	mlb[75D5]
C7531	CAP_603	mlb[75D4]
C7532	CAP_P_TH	mlb[75D5]
C7533	CAP_1206-1	mlb[75D5]
C7534	CAP_1206-1	mlb[75D4]
C7540	CAP_805	mlb[75C3]
C7541	CAP_805	mlb[75C3]
C7542	CAP_P_CASE-D2-SM	mlb[75C2]
C7543	CAP_P_CASE-D2-SM	mlb[75C2]
C7544	CAP_P_CASE-D2-SM	mlb[75C2]
C7545	CAP_402	mlb[75C3]
C7547	CAP_402	mlb[75D7]
C7550	CAP_402	mlb[75B4]
C7551	CAP_805-1	mlb[75A6]
C7552	CAP_805-1	mlb[75A4]
C7553	CAP_402	mlb[75A6]
C7555	CAP_P_CASE-C3	mlb[75A4]
C7559	CAP_603	mlb[75B5]
C7560	CAP_402	mlb[75D8]
C7564	CAP_402	mlb[75C3]
C7585	CAP_402	mlb[75A3]
C7586	CAP_402	mlb[75A2]
C7587	CAP_402	mlb[75A2]
C7588	CAP_402	mlb[75A2]
C7589	CAP_402	mlb[75A1]
C7590	CAP_402	mlb[75B3]
C7591	CAP_402	mlb[75B2]
C7592	CAP_402	mlb[75B2]
C7593	CAP_402	mlb[75B2]
C7594	CAP_402	mlb[75B1]
C7595	CAP_402	mlb[75B3]
C7596	CAP_402	mlb[75B2]
C7597	CAP_402	mlb[75B2]
C7598	CAP_402	mlb[75B2]
C7599	CAP_402	mlb[75B1]
C7600	CAP_603	mlb[76C4]
C7601	CAP_603	mlb[76A4]
C7602	CAP_402	mlb[76A4]
C7604	CAP_402	mlb[76A3]
C7605	CAP_402	mlb[76B5]
C7607	CAP_402	mlb[76A3]
C7608	CAP_402	mlb[76D2]
C7609	CAP_402	mlb[76D7]
C7612	CAP_603	mlb[76A7]
C7613	CAP_402	mlb[76A7]
C7621	CAP_402	mlb[76B6]
C7622	CAP_402	mlb[76C5]
C7624	CAP_402	mlb[76C6]
C7625	CAP_402	mlb[76B6]
C7626	CAP_402	mlb[76B6]
C7628	CAP_402	mlb[76B7]
C7629	CAP_402	mlb[76B7]
C7630	CAP_402	mlb[76A5]
C7631	CAP_402	mlb[76C7]
C7632	CAP_402	mlb[76C2]
C7640	CAP_1206-1	mlb[76D6]
C7641	CAP_1206-1	mlb[76D6]
C7642	CAP_1206-1	mlb[76D6]
C7643	CAP_1206-1	mlb[76D6]
C7650	CAP_805	mlb[76B7]
C7651	CAP_P_CASE-D3L	mlb[76B8]
C7652	CAP_805	mlb[76B8]
C7653	CAP_805	mlb[76C8]
C7654	CAP_805	mlb[76C8]
C7661	CAP_402	mlb[76B3]
C7662	CAP_402	mlb[76C4]
C7664	CAP_402	mlb[76C3]
C7665	CAP_402	mlb[76B4]
C7666	CAP_402	mlb[76B3]
C7668	CAP_402	mlb[76B2]
C7669	CAP_402	mlb[76B2]
C7670	CAP_402	mlb[76B4]
C7680	CAP_1206-1	mlb[76D3]
C7681	CAP_1206-1	mlb[76D4]
C7682	CAP_P_SM-1	mlb[76D4]
C7689	CAP_402	mlb[76B4]
C7690	CAP_805	mlb[76B2]
C7691	CAP_P_CASE-D3L	mlb[76B1]
C7692	CAP_P_CASE-D3L	mlb[76B1]
C7693	CAP_P_CASE-D3L	mlb[76B1]
C7700	CAP_805	mlb[77B5]
C7705	CAP_805	mlb[77B5]
C7706	CAP_603	mlb[77B4]
C7710	CAP_805	mlb[77D6]
C7712	CAP_402-1	mlb[77D4]
C7715	CAP_805	mlb[77D3]
C7800	CAP_402	mlb[78D2]
C7801	CAP_402	mlb[78D2]
C7810	CAP_402	mlb[78D6]
C7811	CAP_402	mlb[78D6]
C7850	CAP_402	mlb[78B2]
C7851	CAP_402	mlb[78C2]
C7895	CAP_402	mlb[78B7]
C7896	CAP_402	mlb[78B5]
C7899	CAP_402	mlb[78C6]
C8400	CAP_P_SM-LF	mlb[84C5]
C8401	CAP_805	mlb[84C7]
C8410	CAP_402	mlb[84C7]
C8411	CAP_402	mlb[84C7]
C8412	CAP_402	mlb[84C4]
C8413	CAP_402	mlb[84C4]
C8414	CAP_402	mlb[84C4]
C8415	CAP_402	mlb[84C4]
C8416	CAP_402	mlb[84C3]
C8420	CAP_402	mlb[84C7]
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C8422	CAP_402	mlb[84C7]
C8423	CAP_402	mlb[84C7]
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C8429	CAP_402	mlb[84B7]
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C8431	CAP_402	mlb[84B7]
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C8434	CAP_402	mlb[84B7]
C8435	CAP_402	mlb[84B7]
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C8437	CAP_402	mlb[84B7]
C8438	CAP_402	mlb[84B7]
C8439	CAP_402	mlb[84B7]
C8440	CAP_402	mlb[84B7]
C8441	CAP_402	mlb[84A7]
C8442	CAP_402	mlb[84A7]
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C8444	CAP_402	mlb[84A7]
C8445	CAP_402	mlb[84A7]
C8446	CAP_402	mlb[84A7]
C8447	CAP_402	mlb[84A7]
C8448	CAP_402	mlb[84A7]
C8449	CAP_402	mlb[84A7]
C8450	CAP_402	mlb[84A7]
C8451	CAP_402	mlb[84A7]
C8500	CAP_805	mlb[85A5]
C8510	CAP_402	mlb[85A4]
C8511	CAP_402	mlb[85A4]
C8570	CAP_402	mlb[85D2]
C9000	CAP_603-1	mlb[90C7]
C9001	CAP_402	mlb[90C5]
C9010	CAP_402	mlb[90A8]
C9020	CAP_1210	mlb[90C5]
C9130	CAP_402	mlb[91B7]
C9131	CAP_805-1	mlb[91B7]
C9140	CAP_402	mlb[91A5]
C9141	CAP_402	mlb[91B5]
C9142	CAP_402	mlb[91B5]
C9143	CAP_402	mlb[91A6]
C9144	CAP_402	mlb[91B6]
C9145	CAP_402	mlb[91B6]
C9160	CAP_402	mlb[91B4]
C9161	CAP_402	mlb[91B4]
C9162	CAP_402	mlb[91A2]
C9163	CAP_402	mlb[91A2]
C9410	CAP_603	mlb[94C3]
C9411	CAP_402	mlb[94D3]
C9413	CAP_402	mlb[94C2]
C9414	CAP_402	mlb[94C2]
C9800	CAP_805	mlb[98C5]
C9801	CAP_402	mlb[98C4]
C9802	CAP_402	mlb[98C4]
D2185	DIODE_SCHOT_SOT23	mlb[21C4]
D2186	DIODE_SCHOT_SOT23	mlb[21B4]
D2702	DIODE_SCHOT_6PB_SOT-363	mlb[27D8 27D8]
D2800	DIODE_SCHOT_6PB_SOT-363	mlb[28D6]
D4390	ZENER_SOT23	mlb[43A6]
D4600	DIODE_SCHOT_3P_A_SC-75	mlb[46C2]
D4601	DIODE_SCHOT_3P_A_SC-75	mlb[46B5]
D4602	DIODE_SCHOT_3P_A_SC-	mlb[46A5]
D5600	DIODE_SOT23	mlb[56C4]
D5601	DIODE_SOT23	mlb[56B4]
D5700	DIODE_SOT23	mlb[57C4]
D7100	DIODE_SCHOT_SMB	mlb[71D2]
D7101	DIODE_SCHOT_SMB	mlb[71B2]
D7200	DIODE_SCHOT_SMB	mlb[72C3]
D7300	DIODE_SCHOT_5P_TLM83-3	mlb[73B6]
D7301	DIODE_SCHOT_SOT23	mlb[73C6]
D7373	DIODE_SCHOT_5P_TLM83-3	mlb[73B3]
D7374	DIODE_SCHOT_SOT23	mlb[73C3]
D7400	DIODE_SCHOT_5P_TLM83-3	mlb[74B6]
D7401	DIODE_SCHOT_SOT23	mlb[74C6]
D7473	DIODE_SCHOT_5P_TLM83-3	mlb[74B3]
D7474	DIODE_SCHOT_SOT23	mlb[74C4]
D7520	DIODE_SCHOT_5P_TLM83-3	mlb[75C4]
D7600	DIODE_SCHOT_5P_TLM83-3	mlb[76B7]
D7601	DIODE_SCHOT_5P_TLM83-3	mlb[76B2]
D7624	DIODE_SCHOT_SOD-323	mlb[76C6]
D7664	DIODE_SCHOT_SOD-323	mlb[76C3]
D7750	DIODE_SCHOT_SOD-123	mlb[77B5]
D7810	DIODE_SCHOT_SOD-123	mlb[78C6]
D9400	ZENER_CASE4Z5	mlb[94C1]
D9410	DIODE_SCHOT_SOD-123	mlb[94D6]
DE4300	DIODE_SCHOT_SM	mlb[43D7]
DP4310	DIODE_DUAL_6P_SOT-363	mlb[43D4 43D3]
DP4311	DIODE_DUAL_6P_SOT-363	mlb[43C4 43C3]
DP4320	DIODE_DUAL_6P_SOT-363	mlb[43B5 43B4]
DP4321	DIODE_DUAL_6P_SOT-363	mlb[43A5 43A4]
DS4599	LED_2.0X1.25MM-SM	mlb[45C2]
F4300	FUSE_SM	mlb[43D6]
F4310	FUSE_SM	mlb[43D6]
F9410	FUSE_805	mlb[94D5]
FL4300	FILTER_4P_L701-SM	mlb[43B3]
FL4310	FILTER_4P_L701-SM	mlb[43B3]
J600	CON_M12RT_D_THB_M-RT-TH	mlb[6D7]
J1000	MEROM_BGA-SKT-P	mlb[10C3 10D7]
J1000	MEROM_BGA-SKT-P	mlb[11D3 11D7]
J1300	CON_F60ST_D_SM1_F-ST-SM	mlb[13C4]
J2800	BATTERY_2P_SM	mlb[28D8]
J3100	CON_F200RT_DDR2DIMM_5MT_SM_F-RT-SM	mlb[31D5]
J3200	CON_F200RT_DDR2DIMM_5MT_SM_F-RT-SM	mlb[32D5]
J3400	CON_F52RT_D2MT_SM_F-RT-SM	mlb[34C5]
J3900	CON_RJ45_8ANG_D3MT_TH_F-ANG-TH	mlb[39C3]
J4300	CON_F9ANG_1394B_D6MT_TH_F-ANG-TH1	mlb[43C2]
J4301	CON_F6ANG_S3MT_1394A_TH_F-ANG-TH	mlb[43B2]
J4401	CON_M50ST_D2MT_SM1_M-ST-SM	mlb[44C4]
J4510	CON_M7ST_SATA_SM_M-S-T-SM	mlb[45D7]
J4610	CON_F4ANG_S4MT_USB_T-H_F-ANG-TH1	mlb[46D1]
J4620	CON_F4ANG_S4MT_USB_T-H_F-ANG-TH1	mlb[46B4]
J4630	CON_F4ANG_S4MT_USB_T-H_F-ANG-TH1	mlb[46A4]
J4700	CON_M5ST_S2MT_SM_M-S-T-SM	mlb[47B5]
J4720	CON_M4ST_S2MT_SM_M-S-T-SM	mlb[47D2]
J4780	CON_M4ST_S2MT_SM_M-S-T-SM	mlb[47B2]
J5010	CON_M2ST_S2MT_SM_M-S-T-SM	mlb[50C6]
J5100	CON_F30STSM_5047_SM1	mlb[51B5]
J5500	CON_M5ST_S2MT_SM_PN1-VD_M-ST-SM	mlb[55D7]
J5510	CON_M2ST_S2MT_SM_M-S-T-SM	mlb[55A7]
J5511	CON_M2RT_S2MT_SM_M-R-T-SM	mlb[55A5]
J5550	CON_M3RT_S2MT_SM_M-R-T-SM	mlb[55B7]
J5551	CON_M2RT_S2MT_SM_M-R-T-SM1	mlb[55B5]
J5560	CON_M5ST_S2MT_SM_PN1-VD_M-ST-SM	mlb[55D6]
J5600	CON_M4RT_S2MT_SM_M-R-T-SM2	mlb[56D3]
J5601	CON_M4RT_S2MT_SM_M-R-T-SM2	mlb[56B2]
J5700	CON_M4ST_S2MT_SM_M-S-T-SM	mlb[57C2]
J8400	CON_F232RT_MXM_SM1_F-RT-SM	mlb[84C5]
J8400	CON_F232RT_MXM_SM1_F-RT-SM	mlb[85C6]
J9002	CON_F30ST_D_SM_F-ST-SM	mlb[90B7]
J9410	CON_DVI_F32ST_Q2MT_SM_F-ST-SM1	mlb[94D5]
J9800	CON_F22RT_S2MT_SM_F-RT-SM	mlb[98C5]
L2150	IND_0603	mlb[21A7]
L2173	IND_1210	mlb[21D4]
L2181	IND_0603	mlb[21D2]
L2183	IND_0603	mlb[21C2]
L2190	IND_0805	mlb[21B3]
L2195	IND_0805	mlb[21A3]
L2700	IND_0805-1	mlb[27C8]
L2702	IND_0805	mlb[27A7]
L2703	IND_1210	mlb[27A7]
L2901	IND_0402	mlb[29D7]
L2902	IND_0402	mlb[29D3]
L2903	IND_0402	mlb[29C7]
L3800	IND_0805-1	mlb[38C6]
L3810	IND_0805-1	mlb[38B6]
L4200	IND_0402-LF	mlb[42D5]
L4210	IND_0402-LF	mlb[42B2]
L4211	IND_0402-LF	mlb[42B2]
L4300	IND_SM	mlb[43D3]
L4301	IND_SM	mlb[43B4]
L4610	IND_SM	mlb[46D3]
L4612	FILTER_4P_L701-SM	mlb[46D3]
L4620	IND_SM	mlb[46C6]
L4622	FILTER_4P_L701-SM	mlb[46B6]
L4630	IND_SM	mlb[46B6]
L4632	FILTER_4P_L701-SM	mlb[46A6]
L4700	IND_SM	mlb[47D6]
L4701	FILTER_4P_L701-SM	mlb[47B6]
L4710	FILTER_4P_L701-SM	mlb[47A6]
L7100	IND_MSQ1211R36LE-TH	mlb[71D2]
L7101	IND_MSQ1211R36LE-TH	mlb[71B2]
L7200	IND_MSQ1211R36LE-TH	mlb[72C3]
L7300	IND_MMD06EZ-SM	mlb[73C7]
L7360	IND_MMD06EZ-SM	mlb[73C2]
L7400	IND_MMD06EZ-SM	mlb[74C7]
L7460	IND_IHLP5050-MMD12CE-SM	mlb[74C2]
L7580	IND_IHLP5050-MMD12CE-SM	mlb[75C3]
L7620	IND_MMD06EZ-SM	mlb[76B7]
L7680	IND_MSQ12113R0LE-TH	mlb[76B2]
L7710	IND_IHLP	mlb[77D4]
L9000	IND_SM	mlb[90C6]
L9140	IND_0402	mlb[91A5]
L9141	IND_0402	mlb[91B5]
L9142	IND_0402	mlb[91B5]
L9160	IND_0402	mlb[91B2]
L9161	IND_0402	mlb[91A2]
L9400	FILTER_4P_SM	mlb[94D7]
L9401	FILTER_4P_SM	mlb[94D7]
L9402	FILTER_4P_SM	mlb[94C7]
L9403	FILTER_4P_SM	mlb[94B7]
L9410	IND_SM-1	mlb[94D4]
LED601	LED_2.0X1.25MM-SM	mlb[6A8]
LED602	LED_2.0X1.25MM-SM	mlb[6A7]
LED603	LED_2.0X1.25MM-SM	mlb[6A6]
LED604	LED_2.0X1.25MM-SM	mlb[6B7]
LED3900	LED_2.0X1.25MM-SM	mlb[39A7]
LED3901	LED_2.0X1.25MM-SM	mlb[39A7]
LED3902	LED_2.0X1.25MM-SM	mlb[39A7]
LED3903	LED_2.0X1.25MM-SM	mlb[39A6]
LED4400	LED_2.0X1.25MM-SM	mlb[44B5]
PP1000	PROBEPOINT_SM	mlb[7D7]
PP1001	PROBEPOINT_SM	mlb[7D7]
PP1002	PROBEPOINT_SM	mlb[7D7]
PP1003	PROBEPOINT_SM	mlb[7D7]
PP1004	PROBEPOINT_SM	mlb[7D7]
PP1005	PROBEPOINT_SM	mlb[7D7]
PP1006	PROBEPOINT_SM	mlb[7D7]
PP1007	PROBEPOINT_SM	mlb[7D7]
PP1008	PROBEPOINT_SM	mlb[7D7]
PP1009	PROBEPOINT_SM	mlb[7D7]
PP1010	PROBEPOINT_SM	mlb[7D7]
PP1011	PROBEPOINT_SM	mlb[7D7]
PP1012	PROBEPOINT_SM	mlb[7D7]
PP1013	PROBEPOINT_SM	mlb[7D7]
PP1014	PROBEPOINT_SM	mlb[7D7]
PP1015	PROBEPOINT_SM	mlb[7D7]
PP1016	PROBEPOINT_SM	mlb[7D7]
PP1017	PROBEPOINT_SM	mlb[7D7]
PP1018	PROBEPOINT_SM	mlb[7D7]
PP1019	PROBEPOINT_SM	mlb[7D7]
PP1020	PROBEPOINT_SM	mlb[7D7]
PP1021	PROBEPOINT_SM	mlb[7C7]
PP1022	PROBEPOINT_SM	mlb[7C7]
PP1023	PROBEPOINT_SM	mlb[7C7]
PP1024	PROBEPOINT_SM	mlb[7C7]
PP1025	PROBEPOINT_SM	mlb[7C7]
PP1026	PROBEPOINT_SM	mlb[7C7]
PP1027	PROBEPOINT_SM	mlb[7C7]
PP1028	PROBEPOINT_SM	mlb[7C7]
PP1029	PROBEPOINT_SM	mlb[7C7]
PP1030	PROBEPOINT_SM	mlb[7C7]
PP1031	PROBEPOINT_SM	mlb[7C7]
PP1032	PROBEPOINT_SM	mlb[7C7]
PP1033	PROBEPOINT_SM	mlb[7C7]
PP1034	PROBEPOINT_SM	mlb[7C7]
PP1035	PROBEPOINT_SM	mlb[7C7]
PP1400	PROBEPOINT_SM	mlb[7D6]
PP1401	PROBEPOINT_SM	mlb[7D6]
PP1402	PROBEPOINT_SM	mlb[7D6]
PP1403	PROBEPOINT_SM	mlb[7D6]
PP1404	PROBEPOINT_SM	mlb[7D6]
PP1405	PROBEPOINT_SM	mlb[7D6]
PP1406	PROBEPOINT_SM	mlb[7D6]
PP1407	PROBEPOINT_SM	mlb[7D6]
PP1408	PROBEPOINT_SM	mlb[7D6]
PP1409	PROBEPOINT_SM	mlb[7D6]
PP1410	PROBEPOINT_SM	mlb[7D6]
PP1411	PROBEPOINT_SM	mlb[7D6]
PP1412	PROBEPOINT_SM	mlb[7D6]
PP1413	PROBEPOINT_SM	mlb[7D6]
PP1414	PROBEPOINT_SM	mlb[7D6]
PP1415	PROBEPOINT_SM	mlb[7D6]
PP1416	PROBEPOINT_SM	mlb[7D6]
PP1417	PROBEPOINT_SM	mlb[7D6]
PP1418	PROBEPOINT_SM	mlb[7D6]
PP1419	PROBEPOINT_SM	mlb[7D6]
PP1420	PROBEPOINT_SM	mlb[7D6]
PP1421	PROBEPOINT_SM	mlb[7C6]
PP1422	PROBEPOINT_SM	mlb[7C6]
PP1423	PROBEPOINT_SM	mlb[7C6]
PP1424	PROBEPOINT_SM	mlb[7C6]
PP1425	PROBEPOINT_SM	mlb[7C6]
PP1426	PROBEPOINT_SM	mlb[7C6]
PP1427	PROBEPOINT_SM	mlb[7C6]
PP1428	PROBEPOINT_SM	mlb[7C6]
PP1429	PROBEPOINT_SM	mlb[7C6]
PP1430	PROBEPOINT_SM	mlb[7C6]
PP1431	PROBEPOINT_SM	mlb[7C6]
PP1432	PROBEPOINT_SM	mlb[7C6]
PP1433	PROBEPOINT_SM	mlb[7C6]
PP1434	PROBEPOINT_SM	mlb[7C6]
PP1435	PROBEPOINT_SM	mlb[7C6]
PP1436	PROBEPOINT_SM	mlb[7C6]
PP1437	PROBEPOINT_SM	mlb[7C6]
PP1438	PROBEPOINT_SM	mlb[7C6]

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PP1439	PROBEPOINT_SM	mlb[7C6]
PP1440	PROBEPOINT_SM	mlb[7C6]
PP1441	PROBEPOINT_SM	mlb[7C6]
PP1442	PROBEPOINT_SM	mlb[7C6]
PP1443	PROBEPOINT_SM	mlb[7C6]
PP1444	PROBEPOINT_SM	mlb[7B6]
PP1445	PROBEPOINT_SM	mlb[7B6]
PP1446	PROBEPOINT_SM	mlb[7B6]
PP1447	PROBEPOINT_SM	mlb[7B6]
PP1448	PROBEPOINT_SM	mlb[7B6]
PP1449	PROBEPOINT_SM	mlb[7B6]
PP1450	PROBEPOINT_SM	mlb[7B6]
PP1451	PROBEPOINT_SM	mlb[7B6]
PP1452	PROBEPOINT_SM	mlb[7B6]
PP1453	PROBEPOINT_SM	mlb[7B6]
PP1454	PROBEPOINT_SM	mlb[7B6]
PP1455	PROBEPOINT_SM	mlb[7B6]
PP1456	PROBEPOINT_SM	mlb[7B6]
PP1457	PROBEPOINT_SM	mlb[7B6]
PP1458	PROBEPOINT_SM	mlb[7B6]
PP1459	PROBEPOINT_SM	mlb[7B6]
PP1460	PROBEPOINT_SM	mlb[7B6]
PP1461	PROBEPOINT_SM	mlb[7B6]
PP1462	PROBEPOINT_SM	mlb[7B6]
PP1463	PROBEPOINT_SM	mlb[7B6]
PP1464	PROBEPOINT_SM	mlb[7B6]
PP1465	PROBEPOINT_SM	mlb[7B6]
PP1466	PROBEPOINT_SM	mlb[7B6]
PP1467	PROBEPOINT_SM	mlb[7B6]
PP1468	PROBEPOINT_SM	mlb[7B6]
PP1469	PROBEPOINT_SM	mlb[7B6]
PP1470	PROBEPOINT_SM	mlb[7A6]
PP1471	PROBEPOINT_SM	mlb[7A6]
PP1472	PROBEPOINT_SM	mlb[7A6]
PP1473	PROBEPOINT_SM	mlb[7A6]
PP1474	PROBEPOINT_SM	mlb[7A6]
PP1475	PROBEPOINT_SM	mlb[7A6]
PP1476	PROBEPOINT_SM	mlb[7A6]
PP1477	PROBEPOINT_SM	mlb[7A6]
PP1478	PROBEPOINT_SM	mlb[7A6]
PP1479	PROBEPOINT_SM	mlb[7A6]
PP1480	PROBEPOINT_SM	mlb[7A6]
PP1481	PROBEPOINT_SM	mlb[7A6]
PP1482	PROBEPOINT_SM	mlb[7A6]
PP1483	PROBEPOINT_SM	mlb[7A6]
PP1484	PROBEPOINT_SM	mlb[7A6]
PP1485	PROBEPOINT_SM	mlb[7A6]
PP1486	PROBEPOINT_SM	mlb[7A6]
PP1487	PROBEPOINT_SM	mlb[7A6]
PP1488	PROBEPOINT_SM	mlb[7A6]
PP1489	PROBEPOINT_SM	mlb[7A6]
PP1490	PROBEPOINT_SM	mlb[7A6]
PP1491	PROBEPOINT_SM	mlb[7A6]
PP1492	PROBEPOINT_SM	mlb[7A6]
PP1493	PROBEPOINT_SM	mlb[7A6]
PP2100	PROBEPOINT_SM	mlb[7C7]
PP2101	PROBEPOINT_SM	mlb[7C7]
PP2102	PROBEPOINT_SM	mlb[7C7]
PP2103	PROBEPOINT_SM	mlb[7B7]
PP2104	PROBEPOINT_SM	mlb[7B7]
PP2105	PROBEPOINT_SM	mlb[7B7]
PP2106	PROBEPOINT_SM	mlb[7B7]
PP2107	PROBEPOINT_SM	mlb[7B7]
PP2108	PROBEPOINT_SM	mlb[7B7]
PP2109	PROBEPOINT_SM	mlb[7B7]
PP2110	PROBEPOINT_SM	mlb[7B7]
PP2111	PROBEPOINT_SM	mlb[7B7]
PP2112	PROBEPOINT_SM	mlb[7B7]
PP2113	PROBEPOINT_SM	mlb[7B7]
PP2114	PROBEPOINT_SM	mlb[7B7]
PP2115	PROBEPOINT_SM	mlb[7B7]
PP2116	PROBEPOINT_SM	mlb[7B7]
PP2117	PROBEPOINT_SM	mlb[7B7]
PP2118	PROBEPOINT_SM	mlb[7B7]
PP2119	PROBEPOINT_SM	mlb[7B7]
PP2120	PROBEPOINT_SM	mlb[7B7]
PP2121	PROBEPOINT_SM	mlb[7A7]
PP2122	PROBEPOINT_SM	mlb[7A7]
PP2123	PROBEPOINT_SM	mlb[7A7]
PP2124	PROBEPOINT_SM	mlb[7A7]
PP2125	PROBEPOINT_SM	mlb[7A7]
PP2126	PROBEPOINT_SM	mlb[7A7]
PP2127	PROBEPOINT_SM	mlb[7A7]
PP2128	PROBEPOINT_SM	mlb[7A7]
PP2129	PROBEPOINT_SM	mlb[7A7]
PP2130	PROBEPOINT_SM	mlb[7A7]
PP2131	PROBEPOINT_SM	mlb[7A7]
PP2132	PROBEPOINT_SM	mlb[7B7]
PP2133	PROBEPOINT_SM	mlb[7B7]
PP3700	PROBEPOINT_SM	mlb[7D5]
PP3701	PROBEPOINT_SM	mlb[7D5]
PP3702	PROBEPOINT_SM	mlb[7D5]
PP3703	PROBEPOINT_SM	mlb[7D5]
PP3704	PROBEPOINT_SM	mlb[7D5]
PP4000	PROBEPOINT_SM	mlb[7D5]
PP4001	PROBEPOINT_SM	mlb[7D5]
PP4002	PROBEPOINT_SM	mlb[7D5]
PP4003	PROBEPOINT_SM	mlb[7D5]
PP4004	PROBEPOINT_SM	mlb[7D5]
PP4900	PROBEPOINT_SM	mlb[7C5]
PP4901	PROBEPOINT_SM	mlb[7C5]
PP4902	PROBEPOINT_SM	mlb[7C5]
PP4903	PROBEPOINT_SM	mlb[7C5]
Q600	TRA_2N7002_SOT23-LF	mlb[6A8]
Q610	TRA_2N7002_SOT23-LF	mlb[6D7]
Q3800	TRA_PBSS5540Z_SOT223	mlb[38C4]
Q3810	TRA_PBSS5540Z_SOT223	mlb[38A4]
Q4200	TRA_BCP69_SOT223-4	mlb[42D6]
Q4600	TRA_2N7002_SOT23-LF	mlb[46C8]
Q5077	TRA_DUAL_MMDT3904_SOT-363-LF	mlb[50D1 50D2]
Q5095	TRA_2N7002DW_SOT-363-LF	mlb[50C2 50C2]
Q5190	TRA_DUAL_MMDT3904_SOT-363-LF	mlb[51B3 51C4]
Q5339	TRA_2N7002_SOT23-LF	mlb[53B7]
Q5341	TRA_FDC796N_SUPERSOT-6	mlb[53B6]
Q5570	TRA_2N7002DW_SOT-363	mlb[55D1 55C2]
Q5600	TRA_NTHS5443T1_1206A-03-LF	mlb[56D4]
Q5602	TRA_2N7002_SOT23-LF	mlb[56D6]
Q5603	TRA_NTHS5443T1_1206A-03-LF	mlb[56B4]
Q5605	TRA_2N7002_SOT23-LF	mlb[56B6]
Q5700	TRA_NTHS5443T1_1206A-03-LF	mlb[57D4]
Q5702	TRA_2N7002_SOT23-LF	mlb[57C5]
Q7006	TRA_DUAL_SSM6N15FE_SOT563	mlb[70A7 70B6]
Q7007	TRA_DUAL_SSM6N15FE_SOT563	mlb[70A6 70B6]
Q7100	TRA_MOSFET_NCHN_5P1_MLP5X6-LFPAK	mlb[71D3]
Q7101	TRA_MOSFET_NCHN_5P2_MLP5X6-LFPAK	mlb[71D3]
Q7102	TRA_MOSFET_NCHN_5P1_MLP5X6-LFPAK	mlb[71C3]
Q7103	TRA_MOSFET_NCHN_5P2_MLP5X6-LFPAK	mlb[71B3]
Q7104	TRA_MOSFET_NCHN_5P2_MLP5X6-LFPAK	mlb[71C3]
Q7105	TRA_MOSFET_NCHN_5P2_MLP5X6-LFPAK	mlb[71B3]
Q7200	TRA_MOSFET_NCHN_5P1_MLP5X6-LFPAK	mlb[72C4]
Q7201	TRA_MOSFET_NCHN_5P2_MLP5X6-LFPAK	mlb[72C4]
Q7204	TRA_MOSFET_NCHN_5P2_MLP5X6-LFPAK	mlb[72C3]
Q7300	TRA_FDMS9620S_MLP	mlb[73C6]
Q7360	TRA_FDMS9620S_MLP	mlb[73C3]
Q7400	TRA_FDMS9620S_MLP	mlb[74C6]
Q7460	TRA_FDM6296_MICROFET 3X3	mlb[74C3]
Q7461	TRA_FDM6296_MICROFET 3X3	mlb[74C3]
Q7520	TRA_MOSFET_NCHN_5P1_MLP5X6-LFPAK	mlb[75D4]
Q7521	TRA_MOSFET_NCHN_5P2_MLP5X6-LFPAK	mlb[75C4]
Q7603	TRA_2N7002_SOT23-LF	mlb[76A6]
Q7620	TRA_FDMS9620S_MLP	mlb[76C7]
Q7640	TRA_SINGLE_MOSFET_PC HN_SOT-23	mlb[53B7]
Q7660	TRA_MOSFET_NCHN_5P1_MLP5X6-LFPAK	mlb[76C3]
Q7661	TRA_MOSFET_NCHN_5P2_MLP5X6-LFPAK	mlb[76B3]
Q7800	TRA_IRF7410_SO-8	mlb[78D2]
Q7801	TRA_SINGLE_MOSFET_NC HN_SOT23	mlb[78D3]
Q7810	TRA_IRF7410_SO-8	mlb[78D6]
Q7811	TRA_SINGLE_MOSFET_NC HN_SOT23	mlb[78D7]
Q7850	TRA_IRF7410_SO-8	mlb[78C2]
Q7851	TRA_SINGLE_MOSFET_NC HN_SOT23	mlb[78B3]
Q7895	TRA_MOSFET_NCHN_8P_S O-8	mlb[78B6]
Q7896	TRA_2N7002_SOT23-LF	mlb[78B7]
Q7897	TRA_SINGLE_MOSFET_NC HN_SOT23	mlb[78B6]
Q9000	TRA_SI3443DV_TSOP-LF	mlb[90C7]
Q9001	TRA_2N7002_SOT23-LF	mlb[90B7]
Q9411	TRA_2N7002DW_SOT-363	mlb[94D2 94C2]
R600	RES_402	mlb[6A7]
R602	RES_402	mlb[6A8]
R604	RES_402	mlb[6B7]
R605	RES_603	mlb[6A6]
R610	RES_402	mlb[6D7]
R1002	RES_402	mlb[10D5]
R1003	RES_402	mlb[10C5]
R1004	RES_402	mlb[10C5]
R1005	RES_402	mlb[10B5]
R1006	RES_402	mlb[10B5]
R1007	RES_402	mlb[10A4]
R1012	RES_402	mlb[10A4]
R1016	RES_402	mlb[10B1]
R1017	RES_402	mlb[10B1]
R1018	RES_402	mlb[10B1]
R1019	RES_402	mlb[10B1]
R1020	RES_402	mlb[10B7]
R1021	RES_402	mlb[10B7]
R1022	RES_402	mlb[10A7]
R1023	RES_402	mlb[10A7]
R1024	RES_402	mlb[10A7]
R1030	RES_402	mlb[10A4]
R1100	RES_402	mlb[11B5]
R1101	RES_402	mlb[11A5]
R1290	RES_402	mlb[12C2]
R1291	RES_402	mlb[12C2]
R1292	RES_402	mlb[12C2]
R1293	RES_402	mlb[12C2]
R1294	RES_402	mlb[12C2]
R1295	RES_402	mlb[12C2]
R1296	RES_402	mlb[12C2]
R1303	RES_402	mlb[13B2]
R1315	RES_402	mlb[13C6]
R1330	RES_402	mlb[13C5]
R1331	RES_402	mlb[13C5]
R1399	RES_402	mlb[13C7]
R1410	RES_402	mlb[14B6]
R1411	RES_402	mlb[14A6]
R1415	RES_402	mlb[14A6]
R1420	RES_402	mlb[14B6]
R1421	RES_402	mlb[14B6]
R1425	RES_402	mlb[14A7]
R1426	RES_402	mlb[14A7]
R1510	RES_402	mlb[15D3]
R1610	RES_402	mlb[16C2]
R1611	RES_402	mlb[16C2]
R1620	RES_402	mlb[16C1]
R1622	RES_402	mlb[16C1]
R1624	RES_402	mlb[16C1]
R1630	RES_402	mlb[16B7]
R1631	RES_402	mlb[16B7]
R1640	RES_402	mlb[16A3]
R1641	RES_402	mlb[16A3]
R1655	RES_402	mlb[16D7]
R1659	RES_402	mlb[16D7]
R1666	RES_402	mlb[16C7]
R1669	RES_402	mlb[16C7]
R1670	RES_402	mlb[16C7]
R1690	RES_402	mlb[16A3]
R1691	RES_402	mlb[16A3]
R2141	RES_603	mlb[21B7]
R2145	RES_603	mlb[21B7]
R2150	RES_603	mlb[21A7]
R2170	RES_603	mlb[21D4]
R2183	RES_402	mlb[21C2]
R2185	RES_402	mlb[21C3]
R2186	RES_402	mlb[21B3]
R2190	RES_402	mlb[21B3]
R2195	RES_402	mlb[21A3]
R2200	RES_402	mlb[22B2]
R2201	RES_402	mlb[22A2]
R2202	RES_402	mlb[22B2]
R2203	RES_402	mlb[22A2]
R2300	RES_402	mlb[23D7]
R2301	RES_402	mlb[23D7]
R2302	RES_402	mlb[23D6]
R2303	RES_402	mlb[23D3]
R2304	RES_402	mlb[23C3]
R2305	RES_402	mlb[23C3]
R2306	RES_402	mlb[23D3]
R2308	RES_402	mlb[23C3]
R2309	RES_402	mlb[23C3]
R2310	RES_402	mlb[23D6]
R2311	RES_402	mlb[23D6]
R2313	RES_402	mlb[23C7]
R2314	RES_402	mlb[23C7]
R2315	RES_402	mlb[23C7]
R2316	RES_402	mlb[23B7]
R2400	RES_402	mlb[24C7]
R2401	RES_402	mlb[24C7]
R2402	RES_402	mlb[24C7]
R2403	RES_402	mlb[24C7]
R2404	RES_402	mlb[24C7]
R2405	RES_402	mlb[24C6]
R2406	RES_402	mlb[24B6]
R2407	RES_402	mlb[24C6]
R2408	RES_402	mlb[24C6]
R2409	RES_402	mlb[24C6]
R2413	RES_402	mlb[24C3]
R2414	RES_402	mlb[24B3]
R2415	RES_402	mlb[24B5]
R2423	RES_402	mlb[24A3]
R2424	RES_402	mlb[24A3]
R2425	RES_402	mlb[24A3]
R2426	RES_402	mlb[24A3]
R2427	RES_402	mlb[24A3]
R2428	RES_402	mlb[24A3]
R2429	RES_402	mlb[24A3]
R2430	RES_402	mlb[24A3]
R2431	RES_402	mlb[24A3]
R2432	RES_402	mlb[24A3]
R2433	RES_402	mlb[24A3]
R2436	RES_402	mlb[24A3]
R2437	RES_402	mlb[24A3]
R2438	RES_402	mlb[24A3]
R2439	RES_402	mlb[24A3]
R2440	RES_402	mlb[24A3]
R2441	RES_402	mlb[24A3]
R2442	RES_402	mlb[24A3]
R2500	RES_402	mlb[25D7]
R2502	RES_402	mlb[25D7]
R2504	RES_402	mlb[25D6]
R2505	RES_402	mlb[25D6]
R2506	RES_402	mlb[25D6]
R2507	RES_402	mlb[25D6]
R2510	RES_402	mlb[25D6]
R2511	RES_402	mlb[25A8]
R2512	RES_402	mlb[25A8]
R2514	RES_402	mlb[25A7]
R2515	RES_402	mlb[25A7]
R2516	RES_402	mlb[25A7]
R2523	RES_402	mlb[25B3]
R2524	RES_402	mlb[25C2]
R2525	RES_402	mlb[25C2]
R2526	RES_402	mlb[25C2]
R2527	RES_402	mlb[25B2]
R2528	RES_402	mlb[25B2]
R2529	RES_402	mlb[25B2]
R2530	RES_402	mlb[25B4]
R2531	RES_402	mlb[25B4]
R2532	RES_402	mlb[25D3]
R2533	RES_402	mlb[25D2]
R2534	RES_402	mlb[25D2]
R2535	RES_402	mlb[25D3]
R2536	RES_402	mlb[25A4]
R2544	RES_402	mlb[25A4]
R2545	RES_402	mlb[25A4]
R2546	RES_402	mlb[25A4]
R2547	RES_402	mlb[25D6]
R2550	RES_402	mlb[25D7]
R2551	RES_402	mlb[25D7]
R2552	RES_402	mlb[25D7]
R2553	RES_402	mlb[25D7]
R2596	RES_402	mlb[25A4]
R2597	RES_402	mlb[25A4]
R2598	RES_402	mlb[25A4]
R2700	RES_603	mlb[27A8]
R2701	RES_402	mlb[27D8]
R2702	RES_402	mlb[27D8]
R2710	RES_402	mlb[28B2]
R2735	RES_402	mlb[27A8]
R2800	RES_402	mlb[28D5]
R2803	RES_402	mlb[28A6]
R2806	RES_402	mlb[28D6]
R2807	RES_402	mlb[28D7]
R2809	RES_402	mlb[28C7]
R2810	RES_402	mlb[28C7]
R2850	RES_402	mlb[28B1]
R2881	RES_402	mlb[28D2]
R2883	RES_402	mlb[28D2]
R2885	RES_402	mlb[28D2]
R2890	RES_402	mlb[28C2]
R2891	RES_402	mlb[28D2]
R2892	RES_402	mlb[28C2]
R2893	RES_402	mlb[28C2]
R2896	RES_402	mlb[28A4]
R2897	RES_402	mlb[28A4]
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R2901	RES_402	mlb[29D3]
R2902	RES_402	mlb[29C3]
R2903	RES_402	mlb[29B6]
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R3027	RES_402	mlb[30A4]
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R3032	RES_402	mlb[30C7]
R3033	RES_402	mlb[30C7]
R3034	RES_402	mlb[30A7]
R3035	RES_402	mlb[30A7]
R3046	RES_402	mlb[30C1]
R3047	RES_402	mlb[30C1]
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R3081	RES_402	mlb[30C7]
R3082	RES_402	mlb[30C7]
R3083	RES_402	mlb[30C7]
R3084	RES_402	mlb[30B7]
R3085	RES_402	mlb[30B7]
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R3090	RES_402	mlb[30B7]
R3091	RES_402	mlb[30B7]
R3098	RES_402	mlb[30B4]
R3100	RES_402	mlb[31D2]
R3101	RES_402	mlb[31C2]
R3140	RES_402	mlb[31A3]
R3141	RES_402	mlb[31A3]
R3200	RES_402	mlb[32C2]
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R3240	RES_402	mlb[32A3]
R3241	RES_402	mlb[32A3]
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R3301	RES_402	mlb[33D5]
R3302	RES_402	mlb[33D5]
R3303	RES_402	mlb[33D5]
R3304	RES_402	mlb[33C5]
R3305	RES_402	mlb[33C5]
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R4011	RES_402	mlb[40B2]
R4012	RES_402	mlb[40B2]
R4013	RES_402	mlb[40C2]
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R4090	RES_402	mlb[40B6]
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R4262	RES_402	mlb[42C2]
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R4301	RES_2512	mlb[43D7]
R4302	RES_805	mlb[43D7]
R4335	RES_402	mlb[43B2]
R4350	RES_402	mlb[43C7]
R4351	RES_402	mlb[43C7]
R4352	RES_402	mlb[43B7]
R4353	RES_402	mlb[43B7]
R4354	RES_402	mlb[43B7]
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R4453	RES_402	mlb[44C4]
R4454	RES_402	mlb[44C4]
R4457	RES_402	mlb[44B6]
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R4599	RES_603	mlb[45C2]
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R4702	RES_402	mlb[47B6]
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R4909	RES_402	mlb[49C1]
R4950	RES_402	mlb[49C4]
R4951	RES_402	mlb[49C4]
R4998	RES_402	mlb[49C2]
R4999	RES_402	mlb[49D4]
R5000	RES_402	mlb[50D6]
R5010	RES_402	mlb[50C6]
R5032	RES_402	mlb[50B1]

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R5033	RES_402	mlb[50B1]
R5034	RES_402	mlb[50B1]
R5035	RES_402	mlb[50B1]
R5036	RES_402	mlb[50B1]
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R5370	RES_402	mlb[53C7]
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R5381	RES_SENSE_2512-1	mlb[53C4]
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R5602	RES_1206	mlb[56D6]
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R5605	RES_805	mlb[56D5]
R5606	RES_402	mlb[56D6]
R5607	RES_805	mlb[56B5]
R5609	RES_805	mlb[56B5]
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R5611	RES_402	mlb[56B6]
R5698	RES_402	mlb[56A7]
R5699	RES_402	mlb[56C7]
R5700	RES_402	mlb[57C7]
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R5703	RES_805	mlb[57D5]
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R6191	RES_402	mlb[61B6]
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R7103	RES_1206	mlb[71D3]
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R7105	RES_402	mlb[71B2]
R7106	RES_603	mlb[71B2]
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R7119	RES_402	mlb[71C8]
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R7123	RES_402	mlb[71A4]
R7126	THERMISTER_402	mlb[71C8]
R7127	RES_402	mlb[71C7]
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R7131	THERMISTER_0603-LF	mlb[71B4]
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R7141	RES_603	mlb[71C1]
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R7143	RES_402	mlb[71C4]
R7197	RES_402	mlb[71D6]
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R7200	RES_402	mlb[72C3]
R7201	RES_603	mlb[72B3]
R7203	RES_1206	mlb[72C3]
R7204	RES_402	mlb[72C2]
R7241	RES_603	mlb[72C2]
R7250	RES_402	mlb[72C5]
R7300	RES_402	mlb[73B7]
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R7311	RES_1206	mlb[73A3]
R7312	RES_1206	mlb[73A3]
R7313	RES_1206	mlb[73A3]
R7321	RES_402	mlb[73C5]
R7323	RES_402	mlb[73B5]
R7331	RES_402	mlb[73C5]
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R7382	RES_402	mlb[73C4]
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R9075	RES_402	mlb[90B2]
R9090	RES_805	mlb[90C6]
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R9161	RES_402	mlb[91A3]
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R9414	RES_402	mlb[94C2]
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R9420	RES_402	mlb[94D1]
R9421	RES_402	mlb[94D1]
R9422	RES_402	mlb[94C2]
R9800	RES_402	mlb[98C6]
R9801	RES_402	mlb[98B6]
RP3300	RPAK4P_SM-LF	mlb[33C4 33C4 33C4 33C4]
RP3305	RPAK4P_SM-LF	mlb[33B4 33C4 33C4 33C4]
RP3310	RPAK4P_SM-LF	mlb[33D4 33A4 33A4 33A4]
RP3330	RPAK4P_SM-LF	mlb[33D4 33B4 33B4 33B4]
RP3334	RPAK4P_SM-LF	mlb[33B4 33B4 33B4 33B4]
RP3338	RPAK4P_SM-LF	mlb[33A4 33B4 33B4 33A4]
RP3342	RPAK4P_SM-LF	mlb[33B4 33C4 33C4 33C4]
RP3346	RPAK4P_SM-LF	mlb[33D4 33C4 33B4 33C4]
RP3350	RPAK4P_SM-LF	mlb[33B4 33A4 33B4 33B4]
RP3354	RPAK4P_SM-LF	mlb[33B4 33A4 33A4 33B4]
RP3358	RPAK4P_SM-LF	mlb[33C4 33C4 33C4 33C4]
RP3362	RPAK4P_SM-LF	mlb[33A4 33C4 33D4 33A4]
S5000	SWI_TACT_4SM_EVQPH_S M-LF	mlb[50D8]
S5010	SWI_TACT_4SM_EVQPH_S M-LF	mlb[50C7]
SC0700	SPRING_CLIP_1P_EMI_C LIP-SM1	mlb[7B6]
SC0701	SPRING_CLIP_1P_EMI_C LIP-SM1	mlb[7B5]
SC0702	SPRING_CLIP_1P_EMI_C LIP-SM-K2	mlb[7B5]
SDF0717	PCB_STANDOFF	mlb[7A3]
SDF0721	PCB_STANDOFF	mlb[7A3]
SDF0726	HSK_NUT_TH	mlb[7A6]
SDF0727	HSK_NUT_TH	mlb[7A5]
SDF0750	PCB_STANDOFF	mlb[7A3]
SDF0751	PCB_STANDOFF	mlb[7A2]
SDF3400	PCB_STANDOFF	mlb[34A5]
SDF4400	PCB_STANDOFF	mlb[44D4]
SDF4401	PCB_STANDOFF	mlb[44A4]
SDF4721	PCB_STANDOFF	mlb[47D1]
SDF9000	PCB_STANDOFF	mlb[90B7]
SDF9001	PCB_STANDOFF	mlb[90A7]
SDF9800	PCB_STANDOFF	mlb[98D5]
SDF9801	PCB_STANDOFF	mlb[98D5]
SDF9803	PCB_STANDOFF	mlb[98B5]
SDF9804	PCB_STANDOFF	mlb[98B5]
SW2800	SWI_TACT_4SM_EVQPH_S M-LF	mlb[28A4]
T3900	XFR_LFE9245A_SOI	mlb[39C5]
U1400	CRESTLINE_FCBGA	mlb[14D4]
U1400	CRESTLINE_FCBGA	mlb[15D4]
U1400	CRESTLINE_FCBGA	mlb[16D5]
U1400	CRESTLINE_FCBGA	mlb[17D3 17D7]
U1400	CRESTLINE_FCBGA	mlb[18D3 18D7]
U1400	CRESTLINE_FCBGA	mlb[19D5]
U1400	CRESTLINE_FCBGA	mlb[20D4 20D7]
U2300	SB_ICH8M_BGA	mlb[23D5]
U2300	SB_ICH8M_BGA	mlb[24B7 24D4]
U2300	SB_ICH8M_BGA	mlb[25D4]
U2300	SB_ICH8M_BGA	mlb[26D5 26D8]
U2803	MC74VHC1G00_SC70-5	mlb[28A7]
U2900	CLK_SYN_SLG8LP537_QF N	mlb[29C5]
U3700	88E8058_QFN	mlb[37C4]
U3780	EEPROM_M24C08_SO8	mlb[37B2]
U4000	FW643_BGA	mlb[40C5]
U4600	SWI_TPS2060_MSOP	mlb[46C7]
U4601	SWI_TPS2068_MSOP	mlb[46D7]
U4650	PI3USB10_TDFN	mlb[46D4]
U4900	SMC_H8S2116_BGA	mlb[49A3 49C3 49B7 49D7]
U5000	VDET_RN5VD_SOT23-5A	mlb[50D7]
U5380	MAX4073_SC70	mlb[53C4]
U5381	MAX4377_UMAX	mlb[53B3]
U5500	LM95214_LLP	mlb[55B4]
U5570	EMC1402_MSOP	mlb[55D4]
U6100	FLASH_SST25VF016B_SO I_SOI	mlb[61C5]
U7010	COMPARATOR_LM339A_SO I-LF	mlb[70D6]

U7052	MC74VHC1G08_SOT23-5- LF	mlb[70C2]
U7056	MC74VHC1G08_SOT23-5- LF	mlb[70C2]
U7100	ISL6260C_QFN	mlb[71C6]
U7101	ISL6208_QFN	mlb[71D5]
U7102	ISL6208_QFN	mlb[71C5]
U7201	ISL6208_QFN	mlb[72C7]
U7300	ISL6539_SSOP	mlb[73C5]
U7400	ISL6539_SSOP	mlb[74C5]
U7500	ISL6269_QFN	mlb[75D6]
U7501	SN74LVC1G07_SC70	mlb[75D8]
U7550	LREG_BD3533FVM_MSOP-8	mlb[75B4]
U7600	LTC3728L_QFN	mlb[76C5]
U7601	COMPARATOR_LM393_SOI -1-LF	mlb[76D6 76A7]
U7710	TPS62050_MSOP	mlb[77D5]
U7750	VREG_TA48025BF_HSOP3	mlb[77B5]
U8570	EEPROM_M24C02_SO8	mlb[85D2]
U9130	VIDEO_TS3V330_SOP	mlb[91B7]
U9160	74LVC1G125LF_SOT23-5	mlb[91B4]
U9161	74LVC1G125LF_SOT23-5	mlb[91A4]
VR5065	VREF_REF3133_SOT23-3	mlb[50B8]
XW4900	SHORT_SM	mlb[49C2]
XW5309	SHORT_SM	mlb[53D7]
XW5500	SHORT_SM	mlb[55A4]
XW5501	SHORT_SM	mlb[55A4]
XW5502	SHORT_SM	mlb[55A4]
XW5503	SHORT_SM	mlb[55A4]
XW7100	SHORT_SM	mlb[71A6]
XW7101	SHORT_SM	mlb[71B2]
XW7102	SHORT_SM	mlb[71B1]
XW7103	SHORT_SM	mlb[71D2]
XW7104	SHORT_SM	mlb[71D1]
XW7203	SHORT_SM	mlb[72C3]
XW7204	SHORT_SM	mlb[72C2]
XW7300	SHORT_SM	mlb[73B4]
XW7400	SHORT_SM	mlb[74B4]
XW7500	SHORT_SM	mlb[75C5]
XW7600	SHORT_SM	mlb[76A5]
Y2800	CRYSTAL_4PIN_SM-LF	mlb[28C7]
Y2901	CRYSTAL_5X3.2-SM	mlb[29C6]
Y3750	CRYSTAL_SM-3-LF	mlb[37B5]
Y4000	CRYSTAL_HC49-USMD	mlb[40B7]
Y5020	CRYSTAL_SM-4	mlb[50C8]
ZH500	HOLE_VIA	mlb[7C1]
ZH501	HOLE_VIA	mlb[7C1]
ZH502	HOLE_VIA	mlb[7C1]
ZH503	HOLE_VIA	mlb[7C1]
ZH504	HOLE_VIA	mlb[7B1]
ZH505	HOLE_VIA	mlb[7B1]
ZH506	HOLE_VIA	mlb[7B1]
ZH507	HOLE_VIA	mlb[7B1]
ZH508	HOLE_VIA	mlb[7B1]
ZH509	HOLE_VIA	mlb[7B1]
ZH510	HOLE_VIA	mlb[7C1]
ZH511	HOLE_VIA	mlb[7C1]
ZH512	HOLE_VIA	mlb[7C1]
ZH513	HOLE_VIA	mlb[7C1]
ZH514	HOLE_VIA	mlb[7B1]
ZH515	HOLE_VIA	mlb[7B1]
ZH516	HOLE_VIA	mlb[7B1]
ZH517	HOLE_VIA	mlb[7B1]
ZH518	HOLE_VIA	mlb[7B1]
ZH519	HOLE_VIA	mlb[7B1]
ZH520	HOLE_VIA	mlb[7C1]
ZH521	HOLE_VIA	mlb[7C1]
ZH522	HOLE_VIA	mlb[7C1]
ZH523	HOLE_VIA	mlb[7C1]
ZH524	HOLE_VIA	mlb[7B1]
ZH525	HOLE_VIA	mlb[7B1]
ZH526	HOLE_VIA	mlb[7B1]
ZH527	HOLE_VIA	mlb[7B1]
ZH528	HOLE_VIA	mlb[7B1]
ZH529	HOLE_VIA	mlb[7B1]
ZH0700	MTGHOLE	mlb[7A5]
ZH0701	MTGHOLE	mlb[7A5]
ZH0702	MTGHOLE	mlb[7A4]
ZH0703	MTGHOLE	mlb[7A4]
ZH0711	MTGHOLE	mlb[7A6]
ZH0712	MTGHOLE	mlb[7A5]
ZH0714	MTGHOLE	mlb[7A5]
ZH0715	MTGHOLE	mlb[7A5]
ZH0718	MTGHOLE	mlb[7A5]
ZH0720	MTGHOLE	mlb[7A4]
ZH0722	MTGHOLE	mlb[7B4]
ZH0723	MTGHOLE	mlb[7B4]
ZH0724	MTGHOLE	mlb[7B3]
ZH0725	MTGHOLE	mlb[7B3]
ZH0750	MTGHOLE	mlb[7A4]

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