

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
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Revision History

*****2008/08/21*****
PAGE 61:
- U7500 PIN V5DRV1 LINK TO PP5V_S0_MCPREG_VCC.
- U7500 PIN TONSEL LINK TO GND DIRECTLY.
PAGE 64:
- R7859 CHANGE TO 100 OHM.
- R7879 CHANGE TO 100K OHM.
PAGE 65:
- DELETE 1.05V S0 FET CIRCUIT.
PAGE 57:
- R7011 CHANGE TO 9.31K OHM, 1k
*****2008/08/22*****
PAGE 7:
- ADD SMC_EXCARD_PWR_EN TEST_POINT
PAGE 8:
- ADD =PP3V42_G3H_RTC_D LINK TO =PP3V42_G3H_REG
PAGE 14:
- R1410 CHANGE TO 49.9 OHM
- CHANGE R1440 TO 150_5% AND NO STUFF
PAGE 26:
- R2872 CHANGE TO 0OHM
- RTC FOLLOW M97 DESIGN AND USE SUPERCAP SOLUTION
- MCP S0 PWRGD FOLLOW M97 DESIGN
PAGE 29:
- PULL R3240 DOWN TO GND. PULL R3241 HIGH
PAGE 32,33,34
- FOLLOW M97 DESIGN
PAGE 39:
- D4600/D4601/PIN-6 CONNECT TO USB VBUS (FOLLOW M97D)
PAGE 44:
- R5270/R5271 = 1K (FOLLOW M97D)
- R5280/R5281 = 1K (FOLLOW M97D)
PAGE 68:
- CHANGE C9411, C9412 TO 220PF
- CHANGE R9462, R9463 TO 2.7KOHM
- ADD C9480 0.1UF_16V_0402 FROM GND_CHASSIS_TMDS_DOWN TO GND
- CHANGE R9460,R9461 TO 0OHM,
- CHANG C9442 AND C9443 TO 47PF
*****2008/08/23*****
MODIFY ALL NOSTUFF TO NO STUFF.
PAGE 6:
- REMOVE ETHERNET CIRCUIT.
PAGE 8:
- ADD =PP3V3_S5_P3V3ENETPHY LINK TO PP3V3_S5
- ADD =P1V05_ENET_PHY LINK TO P1V2R1V05_ENET.
PAGE 9:
- ADD =RTL8211_ENSWRE LINK TO GND.
- ADD =PP3V3_ENET_PHY_VDDREG LINK TO TP_PP3V3_ENET_PHY_VDDREG.
- ADD =RTL8211_REGOUT LINK TO NC_RTL8211_REGOUT.
- =P3V3ENET_EN_L LINK TO PM_SLP_RMG_T_L
- =P1V05ENET_EN LINK TO PM_SLP_RMG_T_L
PAGE 10:
- CHANGE XDP_TDO_CONN TO XDP_TDO
PAGE 13:
- XDP FOLLOW M98 DESIGN. CONNECTOR FROM 516S0625 CHANGE TO 998-1571.
PAGE 23:
- DELETE R2400-R2413 FOR MCP A01 VERSION.
PAGE 31:
- REMOVE R3400, R3401
- L3401 FROM NO STUFF CHANGE TO STUFF.
PAGE 39:
- DELETE R4699.
- R4690 FROM NO STUFF CHANGE TO STUFF.
PAGE 41:
- SMC_NB_DDR_ISENSE CHANGE TO SMC_MCP_DDR_ISENSE
- SMC_NB_CORE_ISENSE CHANGE TO SMC_MCP_CORE_ISENSE
PAGE 46:
- SMC_NB_DDR_ISENSE CHANGE TO SMC_MCP_DDR_ISENSE
- SMC_NB_CORE_ISENSE CHANGE TO SMC_MCP_CORE_ISENSE
- R5417 ADD BOM OPTION FOR NO STUFF
- R5416 ADD BOM OPTION FOR NO STUFF
PAGE 50:
- ADD C5926 (10UF,20%,0603) TO =PP3V3_S3_SMS
PAGE 63:
- REMOVE USB_PWR_EN_S3
PAGE 66:
- REMOVE R9010, R9011
*****2008/08/24*****
PAGE 6:
- R0602 BOMOPTION FROM JTAG_LDEV CHANGE TO NO STUFF.
PAGE 13:
- XDP FOLLOW M97 DESIGN. CONNECTOR FROM 998-1571 CHANGE TO 516S0625.
PAGE 18:
- R1860 AND R1861 CHANGE TO PAGE 68.
PAGE 25:
- C2504-C2507 FROM 138S0578(402) CHANGE TO 138S0614(402-1)
- C2516-C2517 FROM 138S0578(402) CHANGE TO 138S0614(402-1)
PAGE 35:
- R4150 FROM 118S0343 (0201) CHANGE TO 116S0056(0402)
PAGE 58:
- C7281, C7241, C7272 FROM 138S0555(603) CHANGE TO 138S0615(603-1)
- C7280, C7240 FROM 128S0092(POLY) CHANGE TO 128S0128(POLY-TANT)
- C7291, C7292, C7252, C7251 FROM 128S0115(POLY,CASE-B2) CHANGE TO 128S0222(POLY,CASE-B2-SM)
- Q7260, Q7261 FROM 376S0512 CHANGE TO 376S0652 (H-F)
PAGE 59:
- Q7320 FROM 376S0512 CHANGE TO 376S0652 (H-F)
- Q7321 FROM 376S0511 CHANGE TO 376S0651 (H-F)
- C7321 FROM 128S0111(POLY) CHANGE TO 128S0218 (POLY,CASE-D2E-SM)
- C7343 FROM 128S0073 CHANGE TO 128S0233.
PAGE 60:
- XW7400 ADD BOMOPTION OMIT.
- Q7400, Q7402 FROM 376S0472 CHANGE TO 376S0617.
PAGE 61:
- L7500 FROM 152S0869 CHANGE TO 152S0685.
- Q7500 FROM 376S0512 CHANGE TO 376S0652.
- C7560 FROM 128S0092 CHANGE TO 128S0218.
PAGE 62:
- Q7620 FROM 376S0512 CHANGE TO 376S0652.
- C7601 FROM 138S0578 CHANGE TO 138S0614.

*****2008/08/25*****
CHANGE CSA BASE ON WILL'S SUGGESTION.
PAGE 9:
- ADD GMUX_UTAG_TMS AND GMUX_UTAG_TDI IN MISC NC MCP79 ALIASES.
PAGE 18:
- NETNAME ENET_INTR_L CHANGE TO TP_ENET_INTR_L.
- ENET_PWRDWN_L CHANGE TO TP_ENET_PWRDWN_L
PAGE 19:
- DELETE R1987,R1988,R1995,R1970,R1971,R1972,R1973,R1996,R1997,R1998,R1999,R1978,R1979
(FOLLOW M97 DESIGN).
- NET DPMUX_LOWVWR_L SYNC M97 NETNAME AUD_IPHS_SWITCH_EN
- NET LVDSMUX_SEL_IG_L SYNC M97 NETNAME
- NET DPMUX_SEL_IG_L SYNC M97 NETNAME
PAGE 28:
- REMOVE NET DIMM_OVERTEMPA_L
PAGE 29:
- REMOVE NET DIMM_OVERTEMPA_L
PAGE 42:
- ADD SMC_EXCARD_PWR_EN TO TP_SMC_EXCARD_PWR_EN
- ADD SMC_RSTGATE_L TO TP_SMC_RSTGATE_L
- ADD ALS_GAIN TO NC_ALS_GAIN
- ADD ESTARLDO_EN TO NC_ESTARLDO_EN
- ADD SMC_ANALOG_ID TO NC_SMC_ANALOG_ID
- ADD SMC_SYS_KBDLED TO NC_SMC_SYS_KBDLED
- ADD R5054 10KOHM LINK SMC_GPU_ISENSE PULL DOWN TO GND.
- ADD R5055 10KOHM LINK SMC_NR_MISC_ISENSE PULL DOWN TO GND.
PAGE 43:
- R5142 CHANGE TO NO STUFF.
PAGE 46:
- R5416 CHANGE TO 4.53K AND DELETE BOM OPTION.
- R5417 CHANGE TO 4.53K AND DELETE BOM OPTION.
- R5418 CHANGE TO 4.53K AND DELETE BOM OPTION.
PAGE 57:
- NETNAME FROM CHGR_LOWCURRENT_REF CHANGE TO CHGR_LOWCURRENT_REF
- NETNAME FROM CHGR_LOWCURRENT_GATE CHANGE TO CHGR_LOWCURRENT_GATE
PAGE 5:
- REMOVE R7884 AND C7884
PAGE 66:
- REMOVE J9001 PIN 20 AND PIN21 NET.
*****2008/09/02*****
PAGE 45:
- CHANGE ODD CONNECTOR FROM 516S0720 TO 516S0719
*****2008/09/27*****
PAGE 9:
- ADD STANDOFF 860-0964 X 4
- ADD STANDOFF 860-0723 X 1
- ADD STANDOFF 860-0749 X 1
PAGE 29:
- REMOVE BOMOPTION TABLE OF R2903/R2905/R2909/R2911
PAGE 66:
- C6601/C6603 CHANGE TO APN 128S0135, and REMOVE BOMOPTION OMIT
- C6605 CHANGE TO APN 128s0148, HF APN 128s0221, and REMOVE BOMOPTION OMIT
PAGE 68:
- C6830/C6831 CHANGE TO APN 128S0220, and REMOVE BOMOPTION OMIT
PAGE 72:
- R7272 CHANGE FROM 57.6K 1%(114s0389) TO 75K 1%(114s0399)
*****2008/10/20*****
PAGE 29:
- ADD R2903/R2905 BOMOTION AND CHANGE VALUE TO 200 OHM
PAGE 50:
- REMOVE ALT TABLE
PAGE 74:
- REMOVE ALT TABLE
PAGE 94:
- REMOVE K36 BOM OPTION TABLE AND ALT TABLE
*****2008/10/22*****
PAGE 12:
- C1200 ~ C1219 CHANGE TO 138S0580
PAGE 28:
- C2870 CHANGE TO 138S0614
PAGE 37:
- ADD R3731 (116s0026 22 ohm 5%,0402) FOR EMI 125MHZ NOISE
- TP_RTL8211_CLK125 CHANGE TO RTL8211_CLK125
PAGE 48:
- C4803 CHANGE TO 138S0614
PAGE 66:
- C6605 CHANGE TO HF APN 128S0221
PAGE 70:
- C7040/C7041/C7047 CHANGE TO 138S0614
PAGE 90:
- L9002 CHANGE TO 116S0004(0ohm,5%,0402)
- C9003 CHANGE TO 116S0004(0ohm,5%,0402)
*****2008/10/24*****
PAGE 19:
- R1950/R1951/R1952/1953 CHANGE TO 116s0004 (0 OHM,5%,0402)
PAGE 28:
- R2825/R2826 CHANGE TO 116s0004 (0 OHM,5%,0402)
PAGE 34:
- J3400 516S0635 CHANGE TO HF APN 516S0729
PAGE 52:
- ADD C5250/C5251/C5270/C5260/C5261/C5280/C5281 131S1104 (22PF,5%,0402) NO STUFF
- TEXT "ALS" CHANGE TO "MINI-PCIE"
- I2C_ALS_SCL CHANGE TO I2C_MINI_PCIE_SCL
- I2C_ALS_SDA CHANGE TO I2C_MINI_PCIE_SDA
PAGE 67:
- J6700 514-0604 CHANGE TO HF APN 514-0521
- J6750 514-0603 CHANGE TO HF APN 514-0519
PAGE 69:
- J6950 516S0620 CHANGE TO HF APN 516S0735
*****2008/10/25*****
PAGE 52:
- STUFF C5250/C5251/C5270/C5260/C5261/C5280/C5281
*****2008/10/28*****
PAGE 34:
- J3400 516S0729 CHANGE TO 516S0635
*****2008/10/30*****
PAGE 69:
- J6950 516S0735 CHANGE TO 516S0620

*****2008/10/31*****
PAGE 41:
- U4100 CHANGE FROM 338S0523 TO 338S0654
*****2008/11/01*****
PAGE 4:
- BOM change U1400 CHANGE FROM 338S0678 TO 338S0702
*****2008/11/05*****
PAGE 62:
- C6210 CHANGE FROM 127S0062 TO 127S0108
PAGE 68:
- C6832, C6833 CHANGE FROM 127S0062 TO 127S0108
PAGE 45:
- DELETE L4502, NET SATA_HDD_D2R_UF_P / SATA_HDD_D2R_UF_N
- L4501 / F14520 / FL4525 CHANGE FROM 155S0303 TO 155S0371
PAGE 102:
- DELETE PHYSICAL/SPACING SETTING OF SATA_HDD_D2R_UF_P / SATA_HDD_D2R_UF_N
*****2008/11/06*****
- U5413 CHANGE FROM 353S1432 TO 353S2220
- R7417 CHANGE FROM 5.36K(114S0289) TO 4.42K(114S0280)
*****2008/11/12*****
- U1000 CHANGE FROM 373S3646 TO 373S3702
*****2008/11/19*****
- J6950 CHANGE FROM 516S0620 TO 516S0735
- J9401 CHANGE FROM 514-0517 TO 514-0665
- J6750 CHANGE FROM 514-0519 TO 514-0666
- J6700 CHANGE FROM 514-0521 TO 514-0667
- J3900 CHANGE FROM 514-0523 TO 514-0668
- J4600, J4601 CHANGE FROM 514-0527 TO 514-0669
- U3700 CHANGE FROM 338S0570 TO 338S0694
*****2008/11/26*****
- PAGE 61 NOTE : CORRECT REFERENCE TO R5164 AND R5144
- J3400 CHANGE TO 516S0729
*****2008/12/12*****
- R5144 and R5164 changed to 10K 5% 0402 (116S0090)
*****2008/12/17*****
- U4900 symbol update
*****2008/12/20*****
- R5156, R5157, R5158 change from 0 to 33 ohm, 5%, 0402(116s0030)

D

D

C

C

B

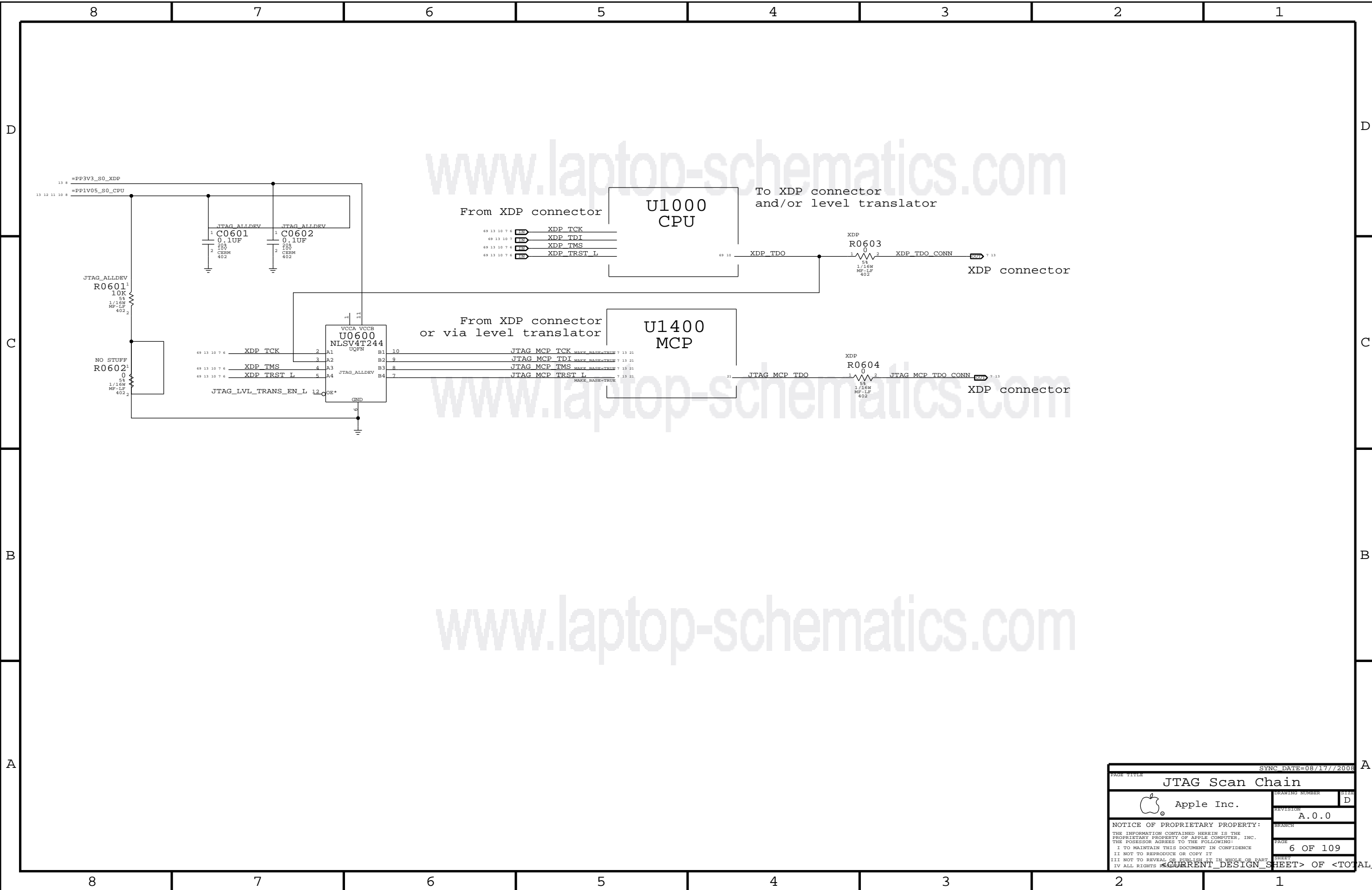
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JTAG Scan Chain			
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		BRANCH	
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Functional Test Points

#J5601 Fan Connectors

```

8800 TRUE PP5VRT_S0 7 8
8801 TRUE FAN_RT_PWM 48
8802 TRUE FAN_RT_TACH 48
8803 TRUE GND
    
```

#J6950 Battery/Lid Connector

```

8970 TRUE SMC_BS_ALERT_L_F 56
8971 TRUE SMBUS_BATT_SCL_F 56
8972 TRUE SMBUS_BATT_SDA_F 56
8973 TRUE PVBAT_G3H_CONN_F 56
8974 TRUE SMC_LID_F 56
8975 TRUE GND_SMC_LID_F 56
8976 TRUE PP3V42_G3H_LIDSWITCH_F 56
8977 TRUE GND Need 6 TP
    
```

#J6900 MagSafe DC Power Jack

```

8920 TRUE PP18V5_DCN_FUSE Need 2 TP 56
8921 TRUE ADAPTER_SENSE 56
8922 TRUE GND Need 2 TP
    
```

#J9000 INVERTER Connector

```

8860 TRUE PPBUS_ALL_INV_CONN Need 2 TP 66
8861 TRUE INV_GND 66
8862 TRUE PP5V_INV_F 66
8863 TRUE INV_BKLIGHT_PWM_L Need 4 TP 66
    
```

#J9001 LCD + CAMERA CONNECTOR

```

8800 TRUE PP3V3_LCDVDD_SW_F 66
8801 TRUE PP3V3_S0_LCD_F 66
8802 TRUE LVDS_IG_DDC_CLK 18 66
8803 TRUE LVDS_IG_DDC_DATA 18 66
8804 TRUE LVDS_IG_A_DATA_N<0> 18 66 71
8805 TRUE LVDS_IG_A_DATA_P<0> 18 66 71
8806 TRUE LVDS_IG_A_DATA_N<1> 18 66 71
8807 TRUE LVDS_IG_A_DATA_P<1> 18 66 71
8808 TRUE LVDS_IG_A_DATA_N<2> 18 66 71
8809 TRUE LVDS_IG_A_DATA_P<2> 18 66 71
8810 TRUE LVDS_IG_A_CLK_F_N 66
8811 TRUE LVDS_IG_A_CLK_F_P 66
8812 TRUE USB2_CAMERA_CONN_P 66 72
8813 TRUE USB2_CAMERA_CONN_N 66 72
8814 TRUE PP5V_S3_CAMERA_F 66
8815 TRUE GND
    
```

J6701 MIC CONNECTOR

```

8816 TRUE MIC_LO_CONN 54
8817 TRUE MIC_HI_CONN 54
8818 TRUE MIC_SHLD_CONN 54 55
    
```

#J6702 Left SPEAKER CONNECTOR

```

8819 TRUE SPKRCONN_L_P_OUT 53 54
8820 TRUE SPKRCONN_L_N_OUT 53 54
    
```

#J6703 Right SUB SPEAKER CONNECTOR

```

8821 TRUE SPKRCONN_SUB_P_OUT 53 54
8822 TRUE SPKRCONN_SUB_N_OUT 53 54
8823 TRUE SPKRCONN_R_P_OUT 53 54
8824 TRUE SPKRCONN_R_N_OUT 53 54
    
```

J5800 GEYSER AND DIMMO REMOTE TEMP SENSORS

```

8825 TRUE TPAD_GND_F 49
8826 TRUE CONN_TPAD_ONOFF_FLTR_L 49
8827 TRUE CONN_TPAD_USB_P 49 72
8828 TRUE CONN_TPAD_USB_N 49 72
8829 TRUE SMC_LID_LC 49
8830 TRUE PP5V_S3_TPAD_F 49
    
```

#J5520 CPU/MCP Thermal Sensor

```

8831 TRUE CPUTHSNS_D2_P 47
8832 TRUE CPUTHSNS_D2_N 47
8833 TRUE MCPTHSNS_D2_P 47
8834 TRUE MCPTHSNS_D2_N 47
    
```

#J4810 BLUETOOTH

```

8835 TRUE PP3V3_S3_BT_F_CONN 40
8836 TRUE USB2_BT_F_N_CONN 40 72
8837 TRUE USB2_BT_F_P_CONN 40 72
8838 TRUE GND_BT_F_CONN 40
    
```

#J4500 SATA ODD

```

8839 TRUE SATA_ODD_R2D_UF_P 38 71
8840 TRUE SATA_ODD_R2D_UF_N 38 71
8841 TRUE SATA_ODD_D2R_C_N 38 71
8842 TRUE SATA_ODD_D2R_C_P 38 71
8843 TRUE PP3V3_S0 Need 4 TP 7 8
8844 TRUE SMC_ODD_DETECT 38 41
8845 TRUE GND Need 6 TP
    
```

J4501 SATA HD System LED and IR

```

8846 TRUE SATA_HDD_R2D_P 38 71
8847 TRUE SATA_HDD_R2D_N 38 71
8848 TRUE SATA_HDD_D2R_C_N 38 71
8849 TRUE SATA_HDD_D2R_C_P 38 71
8850 TRUE PP5V_S0_HDD_FLT Need 4 TP 38
8851 TRUE SYS_LED_ANODE_L 38
8852 TRUE IR_EX_OUT 38 40
8853 TRUE PP5V_S3_IR_CONN 38
8854 TRUE GND Need 4 TP
    
```

#J3400 Airport

```

8855 TRUE PCIE_WAKE_L 17 31
8856 TRUE MINI_CLKREQ_L 17 31
8857 TRUE PCIE_CLK100M_MINI_N 17 31 71
8858 TRUE PCIE_CLK100M_MINI_P 17 31 71
8859 TRUE PCIE_MINI_D2R_N 17 31 71
8860 TRUE PCIE_MINI_D2R_P 17 31 71
8861 TRUE PCIE_MINI_R2D_N 31 71
8862 TRUE PCIE_MINI_R2D_P 31 71
8863 TRUE PP3V3_WLAN Need 4 TP 31
8864 TRUE PP1V5_S0_R Need 3 TP 7 8
8865 TRUE MINI_RESET 31
8866 TRUE PP3V3_S3_AIRPORT_CONN 31
8867 TRUE I2C_MINI_PCIE_SCL 31 44
8868 TRUE I2C_MINI_PCIE_SDA 31 44
8869 TRUE USB2_AIRPORT_N 31 72
8870 TRUE USB2_AIRPORT_P 31 72
8871 TRUE GND Need 6 TP
    
```

Other Func Test Points

```

8872 TRUE ALL_SYS_PWRGD 26 41 64
8873 TRUE PPVCORE_S0_CPU 8
8874 TRUE PPCPUVTT_S0 8
8875 TRUE PPVCORE_S0_MCP_R 8
8876 TRUE PPVCORE_S0_MCP 8
8877 TRUE PP0V9_S0 8
8878 TRUE PP1V05_S0 8
8879 TRUE PP1V5_S0_R 7 8
8880 TRUE PP1V8_S0 8
8881 TRUE PP1V8_S0_R 8
8882 TRUE PP1V05_S0_MCP_PEX_AVDD 8 24
8883 TRUE PP1V05_S0 8
8884 TRUE PP1V05_S0_MCP_SATA_AVDD 8 24
8885 TRUE PP1V05_S0 7 8
8886 TRUE PP5VRT_S0 7 8
8887 TRUE PP3V3_S0 7 8
8888 TRUE PP1V0_PWM 8
8889 TRUE PP1V8_S3 8
8890 TRUE PP3V3_S3 8
8891 TRUE PP5VLT_S3 8
8892 TRUE PPVTT_S3_DDR_BUF 8
8893 TRUE PP1V05_S5_REG 8
8894 TRUE PP3V3_S5 8
8895 TRUE PP3V42_G3H 7 8
8896 TRUE PP18V5_G3H 8
8897 TRUE PPBUS_G3H 8
8898 TRUE PPBUS_G3H_CPU_ISNS 8
8899 TRUE PP3V3_ENET_PHY 8
8900 TRUE PP1V2R1V05_ENET 8
8901 TRUE PPVP_FW 8
    
```

#J1300 XDP

```

8892 TRUE XDP_BPM_L<5> 10 13 69
8893 TRUE XDP_BPM_L<4> 10 13 69
8894 TRUE XDP_BPM_L<3> 10 13 69
8895 TRUE XDP_BPM_L<2> 10 13 69
8896 TRUE XDP_BPM_L<1> 10 13 69
8897 TRUE XDP_BPM_L<0> 10 13 69
8898 TRUE TP_XDP_OBSFN_B0 13
8899 TRUE TP_XDP_OBSFN_B1 13
8900 TRUE TP_XDP_OBSDATA_B0 13
8901 TRUE TP_XDP_OBSDATA_B1 13
8902 TRUE TP_XDP_OBSDATA_B2 13
8903 TRUE TP_XDP_OBSDATA_B3 13
8904 TRUE XDP_PWRGD 13
8905 TRUE XDP_OBS20 13
8906 TRUE PM_LATIGGER_L 13 19
8907 TRUE JTAG_MCP_TCK 6 13 21
8908 TRUE SMBUS_MCP_0_DATA 13 21 44 72
8909 TRUE SMBUS_MCP_0_CLK 13 21 44 72
8910 TRUE XDP_TCK 6 10 13 69
8911 TRUE PPCPUVTT_S0 7 8
8912 TRUE PP3V3_S0 7 8
8913 TRUE JTAG_MCP_TDO_CONN 6 13
8914 TRUE JTAG_MCP_TRST_L 6 13 21
8915 TRUE MCP_DEBUG<0> 13 19 72
8916 TRUE MCP_DEBUG<1> 13 19 72
8917 TRUE MCP_DEBUG<2> 13 19 72
8918 TRUE MCP_DEBUG<3> 13 19 72
8919 TRUE JTAG_MCP_TDI 6 13 21
8920 TRUE JTAG_MCP_TMS 6 13 21
8921 TRUE MCP_DEBUG<4> 13 19 72
8922 TRUE MCP_DEBUG<5> 13 19 72
8923 TRUE MCP_DEBUG<6> 13 19 72
8924 TRUE MCP_DEBUG<7> 13 19 72
8925 TRUE FSB_CLK_ITP_P 13 14 69
8926 TRUE FSB_CLK_ITP_N 13 14 69
8927 TRUE XDP_CPURST_L 13 69
8928 TRUE XDP_DBRESET_L 10 13 26
8929 TRUE XDP_TDO_CONN 6 13
8930 TRUE XDP_TRST_L 6 10 13 69
8931 TRUE XDP_TDI 6 10 13 69
8932 TRUE XDP_TMS 6 10 13 69
8933 TRUE GND Need 8 TP
    
```

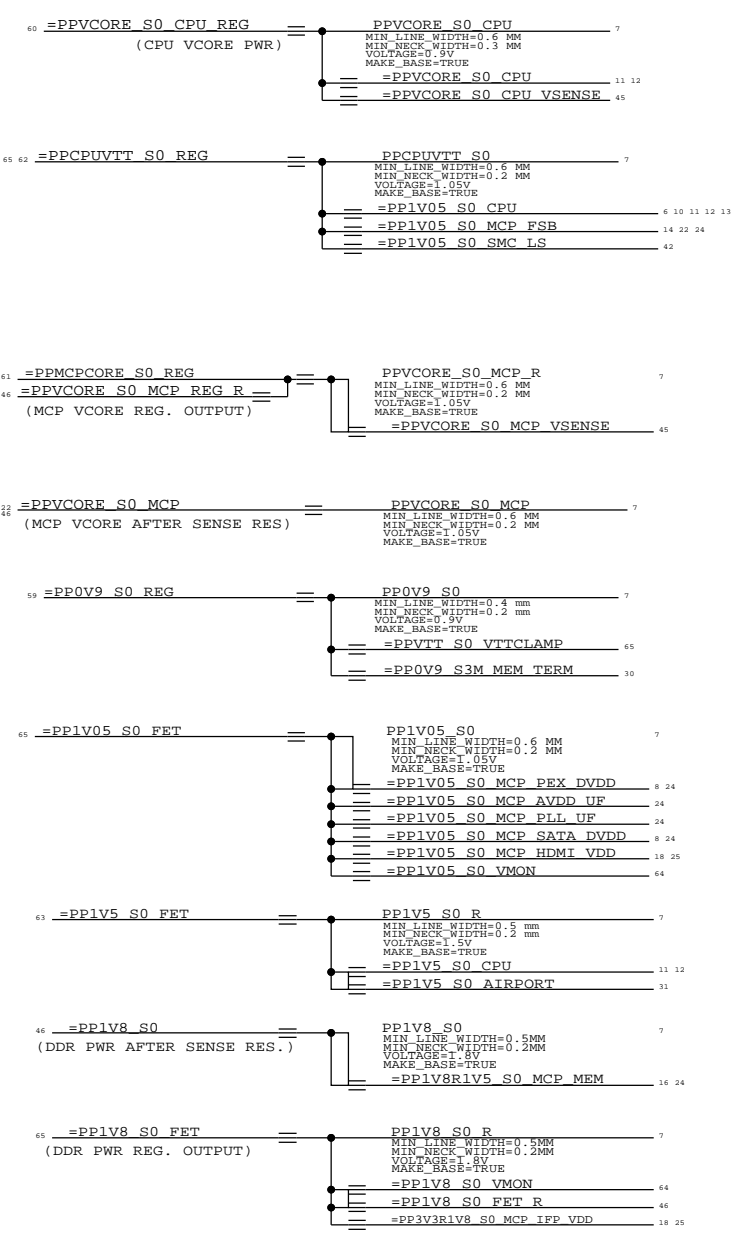
J5100 LPC+SPI Connector

```

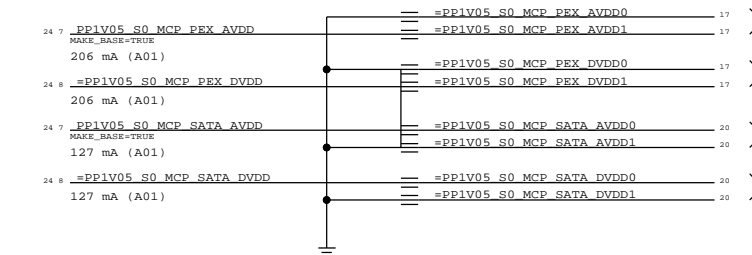
8934 TRUE PP3V42_G3H 7 8
8935 TRUE PP5VRT_S0 7 8
8936 TRUE LPC_AD<0> 19 41 43 72
8937 TRUE LPC_AD<1> 19 41 43 72
8938 TRUE SPI_ALT_MOSI 43
8939 TRUE SPI_ALT_MISO 43
8940 TRUE LPC_FRAME_L 19 41 43 72
8941 TRUE PM_CLKRUN_L 19 41 43
8942 TRUE SMC_TMS 41 42 43
8943 TRUE DEBUG_RESET_L 26 43
8944 TRUE SMC_TDO 41 42 43
8945 TRUE SMC_TRST_L 41 43
8946 TRUE SMC_MDI 41 43
8947 TRUE SMC_TX_L 39 41 42 43
8948 TRUE LPC_CLK33M_LPCPLUS 26 43 72
8949 TRUE LPC_AD<2> 19 41 43 72
8950 TRUE LPC_AD<3> 19 41 43 72
8951 TRUE SPIROM_USE_MLB 43
8952 TRUE SPI_ALT_CLK 43
8953 TRUE SPI_ALT_CS_L 43
8954 TRUE LPC_SERIRQ 19 41 43
8955 TRUE LPC_PWRDWN_L 19 41 43
8956 TRUE SMC_TDI 41 42 43
8957 TRUE SMC_TCK 41 42 43
8958 TRUE SMC_RESET_L 41 42 43
8959 TRUE SMC_NMI 41 43
8960 TRUE SMC_RX_L 39 41 42 43
8961 TRUE LPCPLUS_GPIO 18 43
8962 TRUE GND Need 2 TP
    
```

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FUNC TEST		D	
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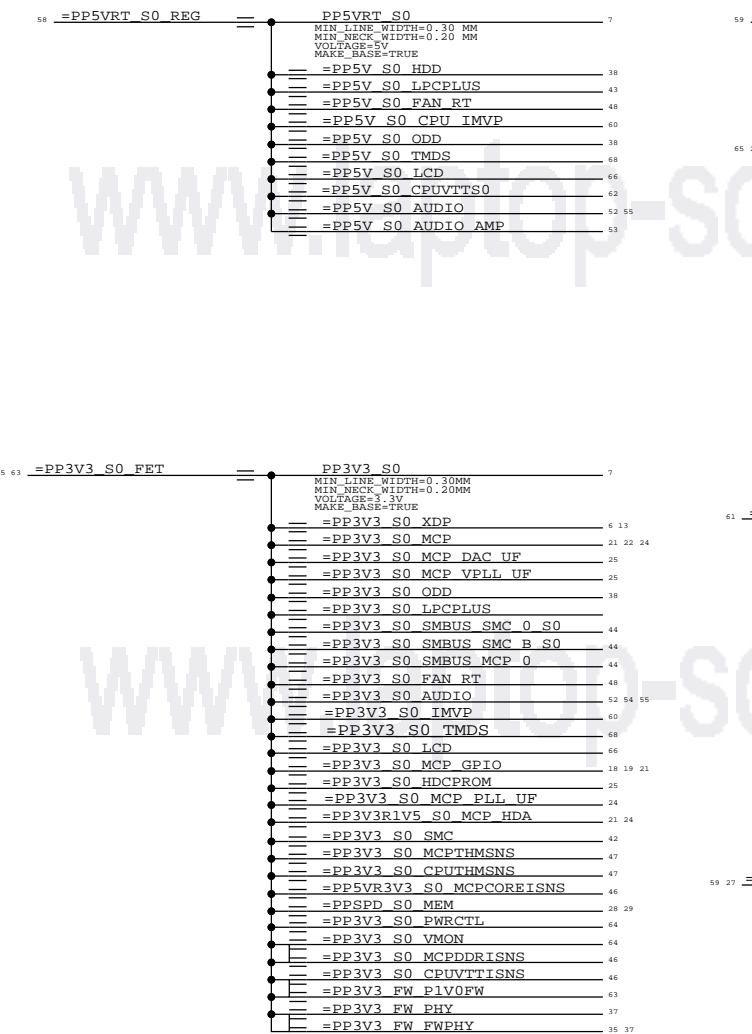
"S0,S0M" RAILS



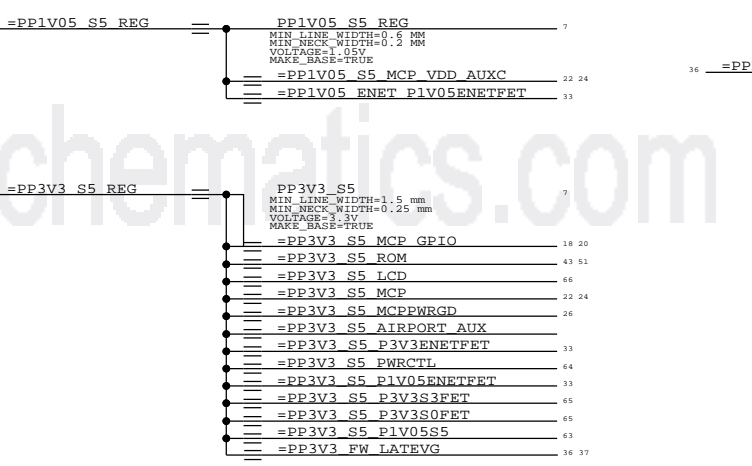
PEX & SATA AVDD/DVDD aliases



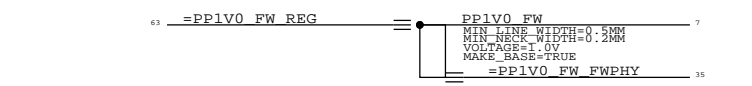
"S3" RAILS



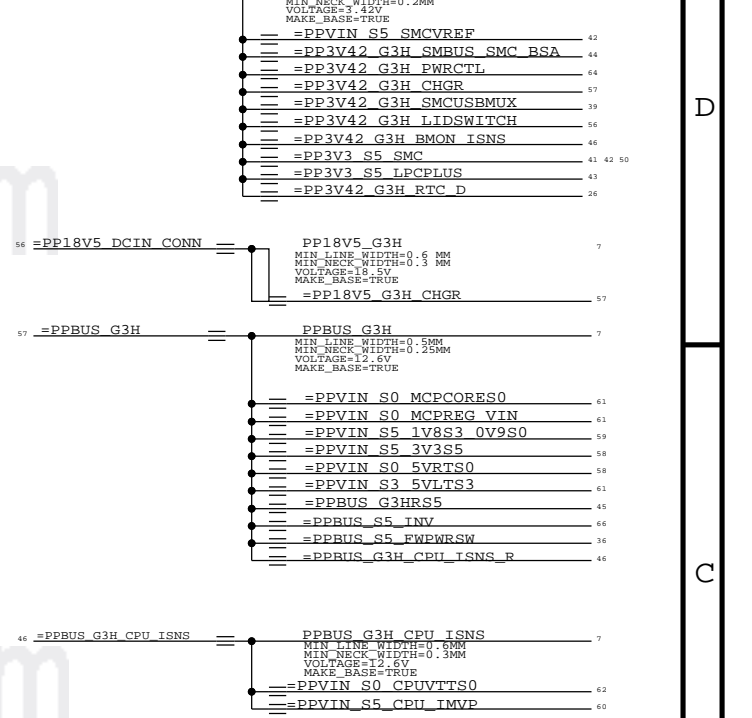
"S5" RAILS



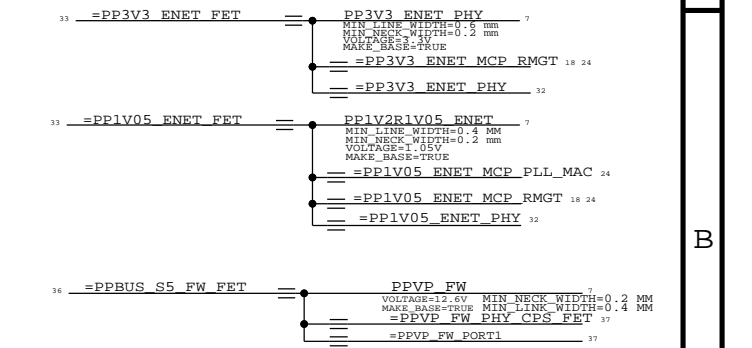
"FW" RAILS



"G3H" RAILS

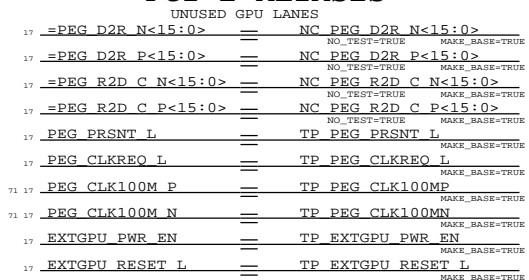


"ENET" RAILS

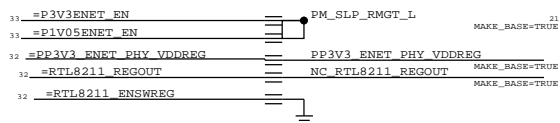


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Power Aliases		D	
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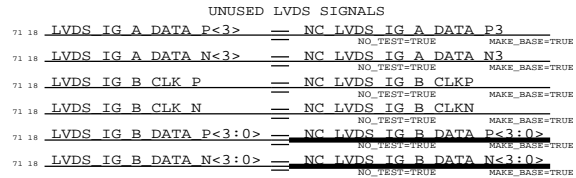
PCI-E ALIASES



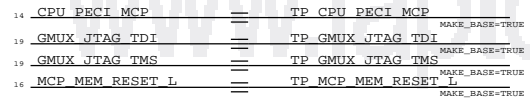
ETHERNET ALIASES



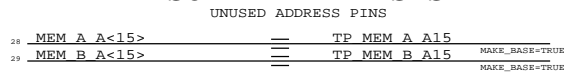
LVDS ALIASES



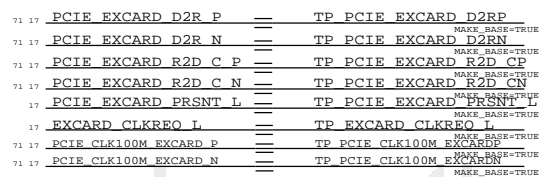
MISC NC MCP79 ALIASES



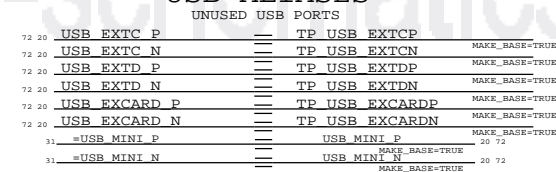
SO-DIMM ALIASES



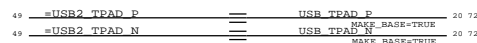
UNUSED EXPRESS CARD LANE



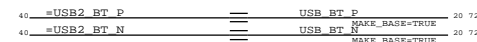
USB ALIASES



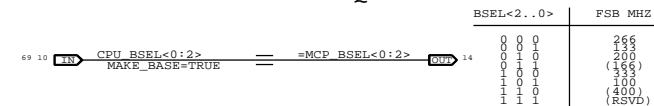
TRACKPAD (WELLSPRING)



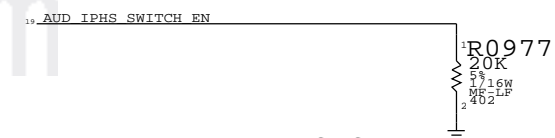
BLUETOOTH



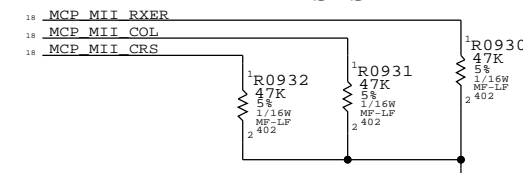
CPU FSB FREQUENCY STRAPS



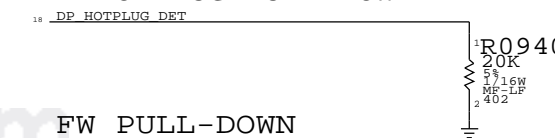
HDA PULL-DOWN



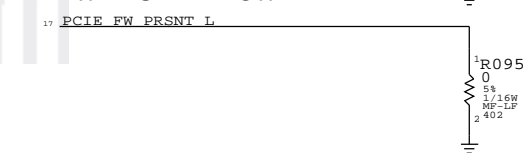
LAN ALIASES



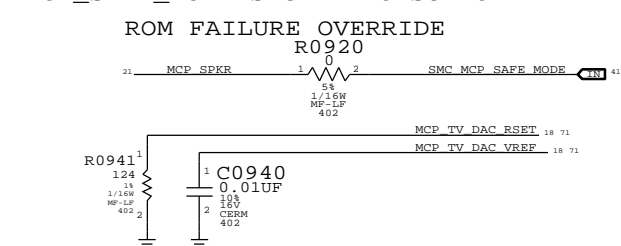
DP HOTPLUG PULL-DOWN



FW PULL-DOWN

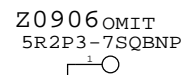


MCP_SAFE_MODE SIGNAL TO SUPPORT

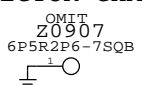


Screw Holes

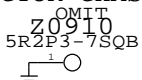
BATTERY,AUDIO,DIP DIMM CONNECTOR CHASSIS GND



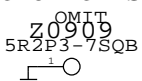
SATA,LVDS CONNECTOR CHASSIS GND



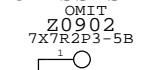
DIP DIMM CONNECTOR CHASSIS GND



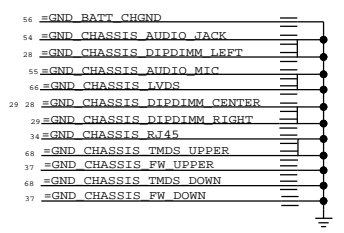
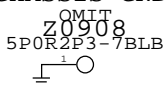
DIP DIMM CONNECTOR CHASSIS GND



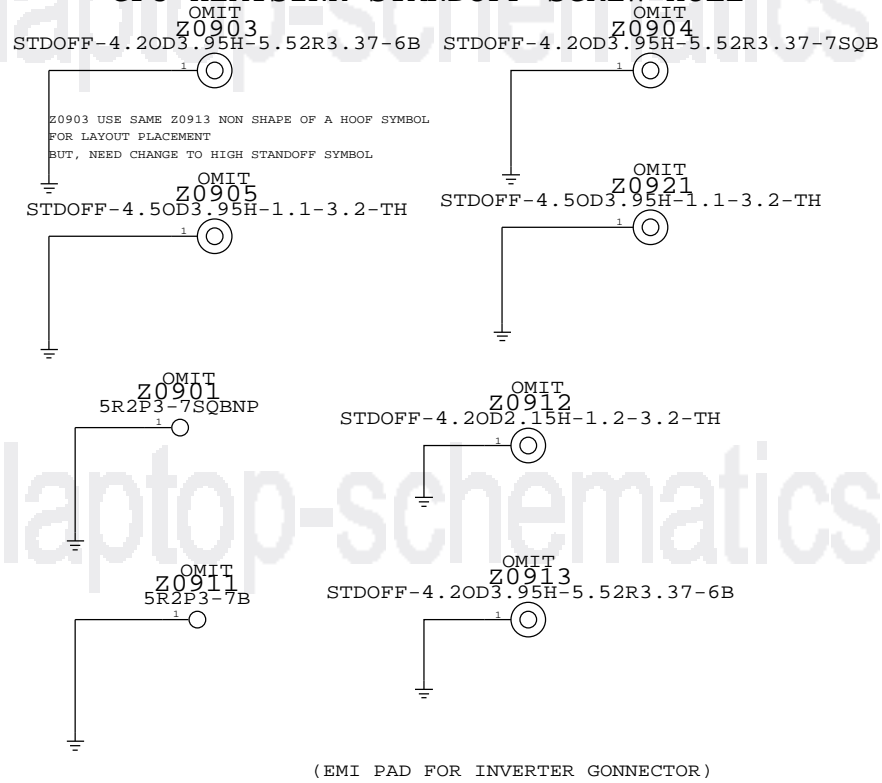
DCIN CONNECTOR CHASSIS GND



I/O CONNECTOR CHASSIS GND



CPU HEATSINK STANDOFF SCREW HOLE



(EMI PAD FOR INVERTER GONNECTOR)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
860-0964	4	THERMAL STANDOFF	Z0903,Z0904,Z0905,Z0921	?	STANDOFF
860-0723	1	STANDOFF WIRELESS	Z0912	?	STANDOFF
860-0749	1	STANDOFF W/THRU HOLES,WIRELESS	Z0913	?	STANDOFF

PAGE TITLE

SIGNAL ALIAS

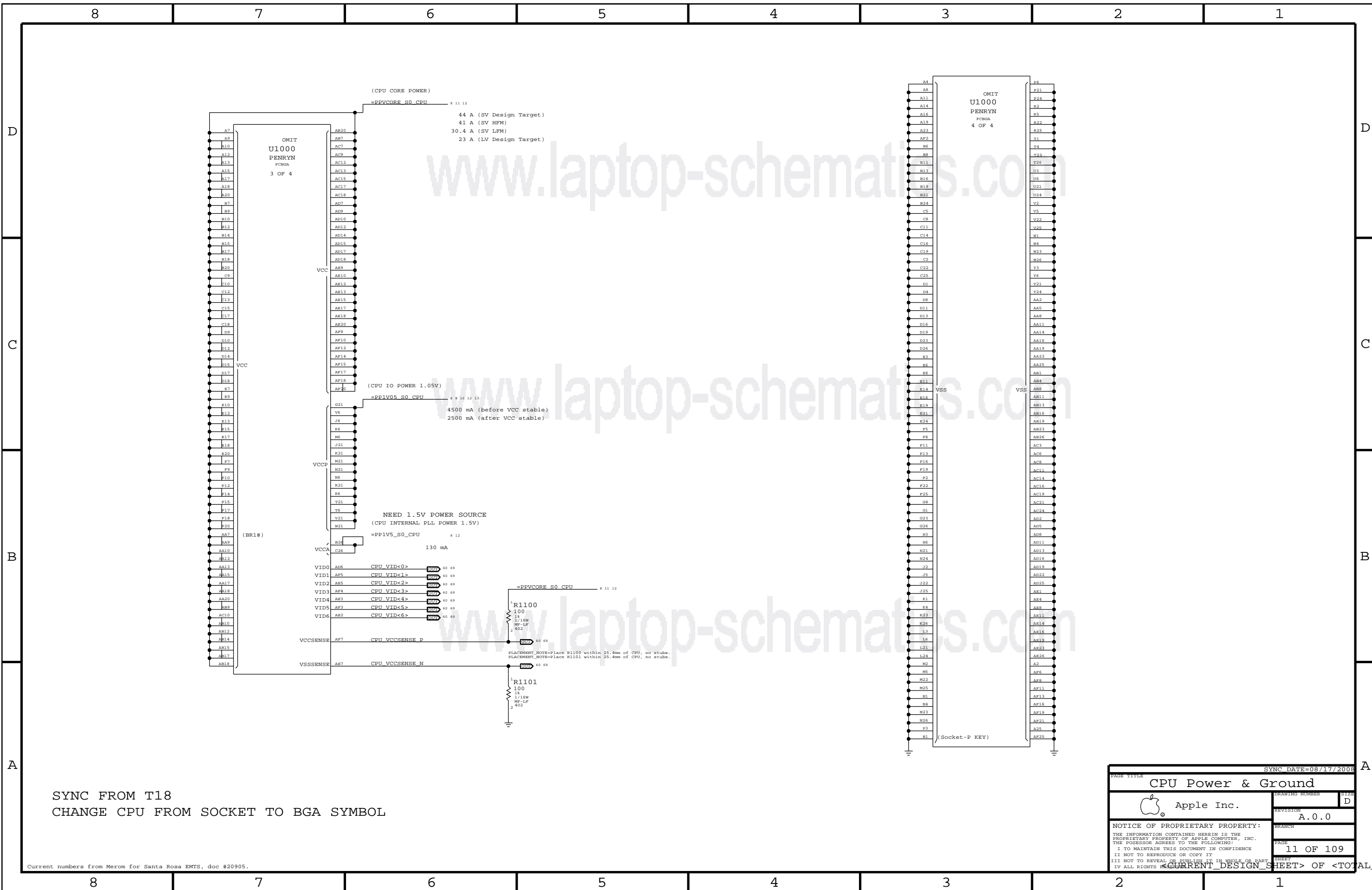
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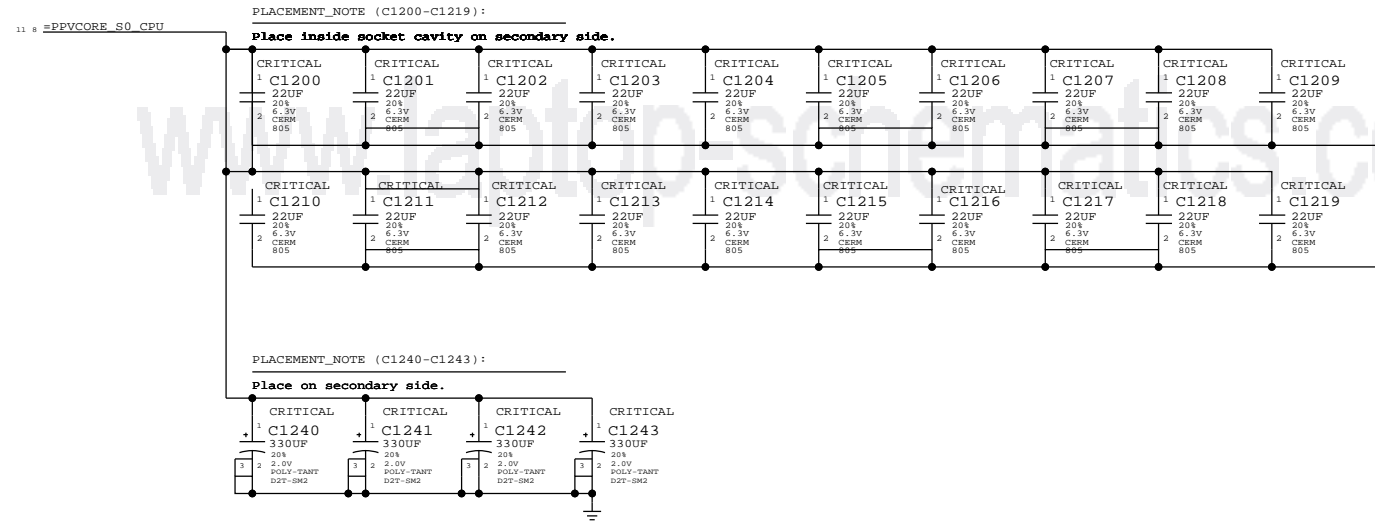


SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

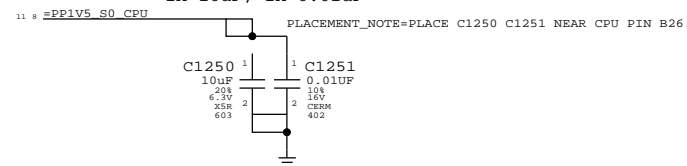
PAGE TITLE		SYNC DATE=08/17/2008	
CPU Power & Ground		DESIGN NUMBER	N122
Apple Inc.		REVISION	D
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CPU VCore HF and Bulk Decoupling

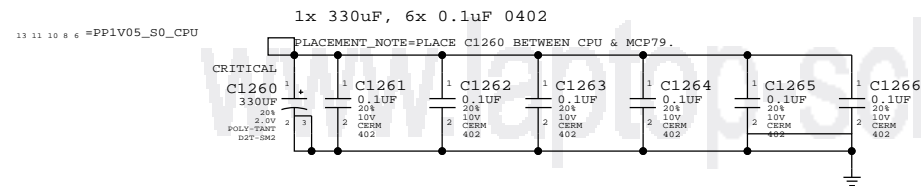
6x 330uF, 32x 22uF 0805 (20 stuffed)



VCCA (CPU AVdd) DECOUPLING



VCCP (CPU I/O) DECOUPLING



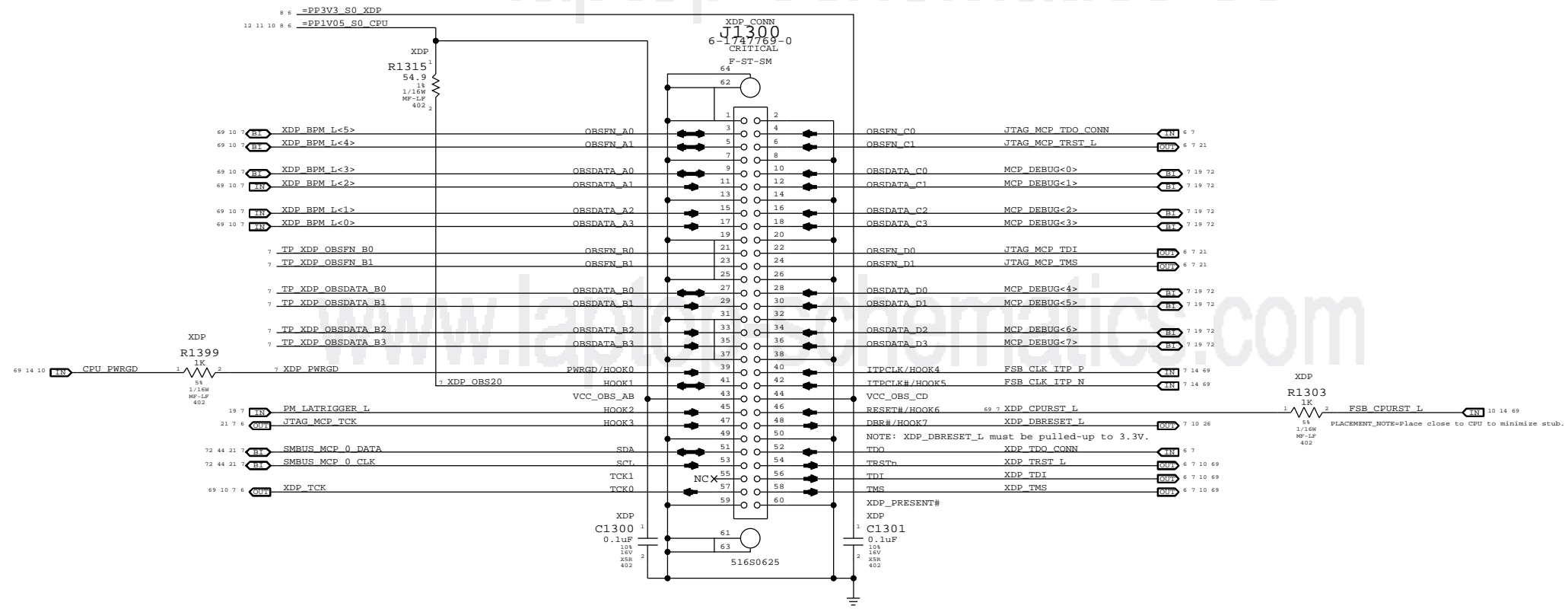
SYNC FROM T18

PAGE TITLE		CPU Decoupling	
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Mini-XDP Connector

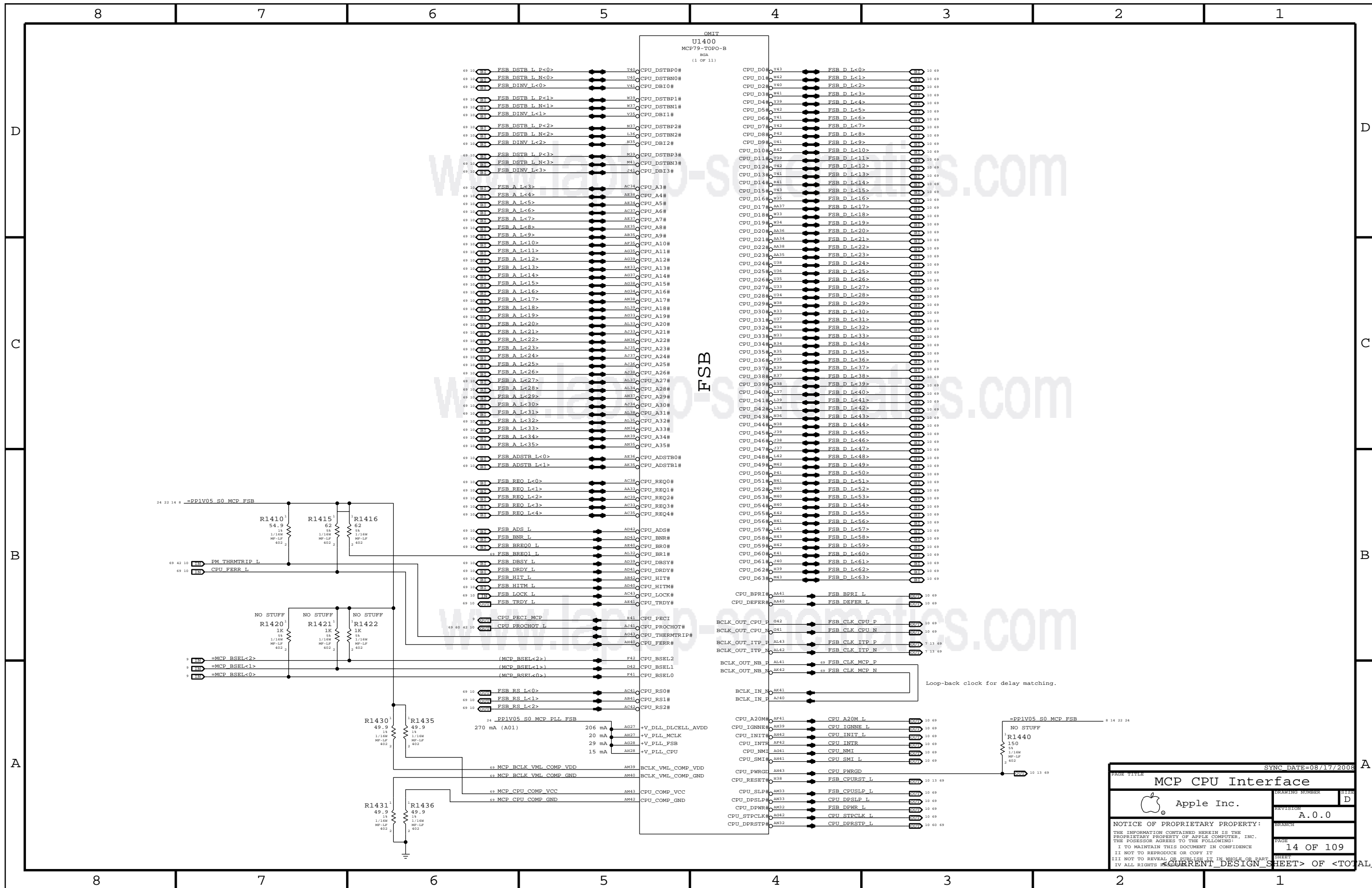
NOTE: This is not the standard XDP pinout.
Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout



← Direction of XDP module
Please avoid any obstructions on even-numbered side of J1300

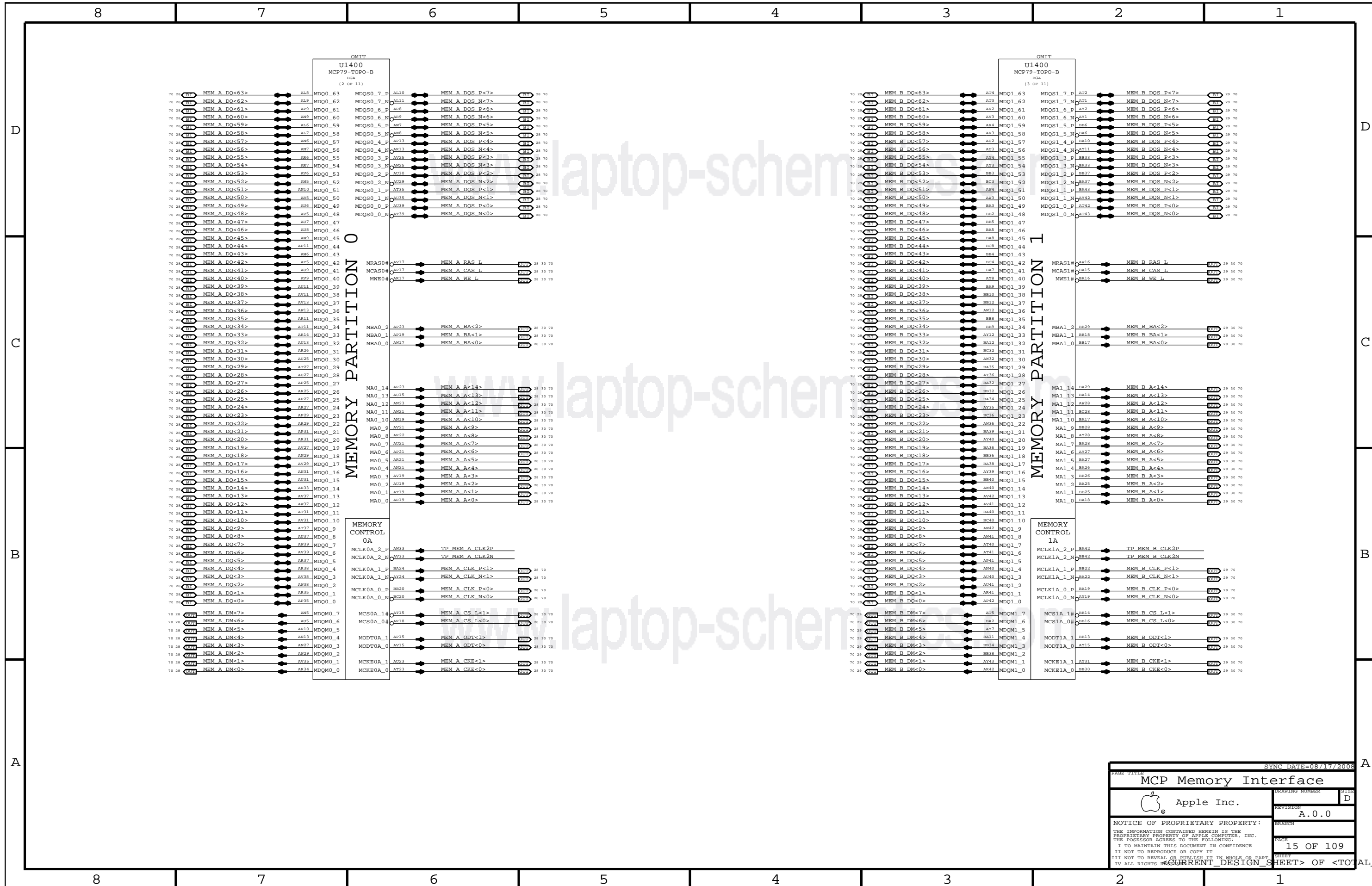
PAGE TITLE		SYNC DATE=01/08/2008	
eXtended Debug Port (MiniXDP)		DESIGN NUMBER	1122
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MCP CPU Interface		DRAWING NUMBER D
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MCP Memory Interface

Apple Inc.

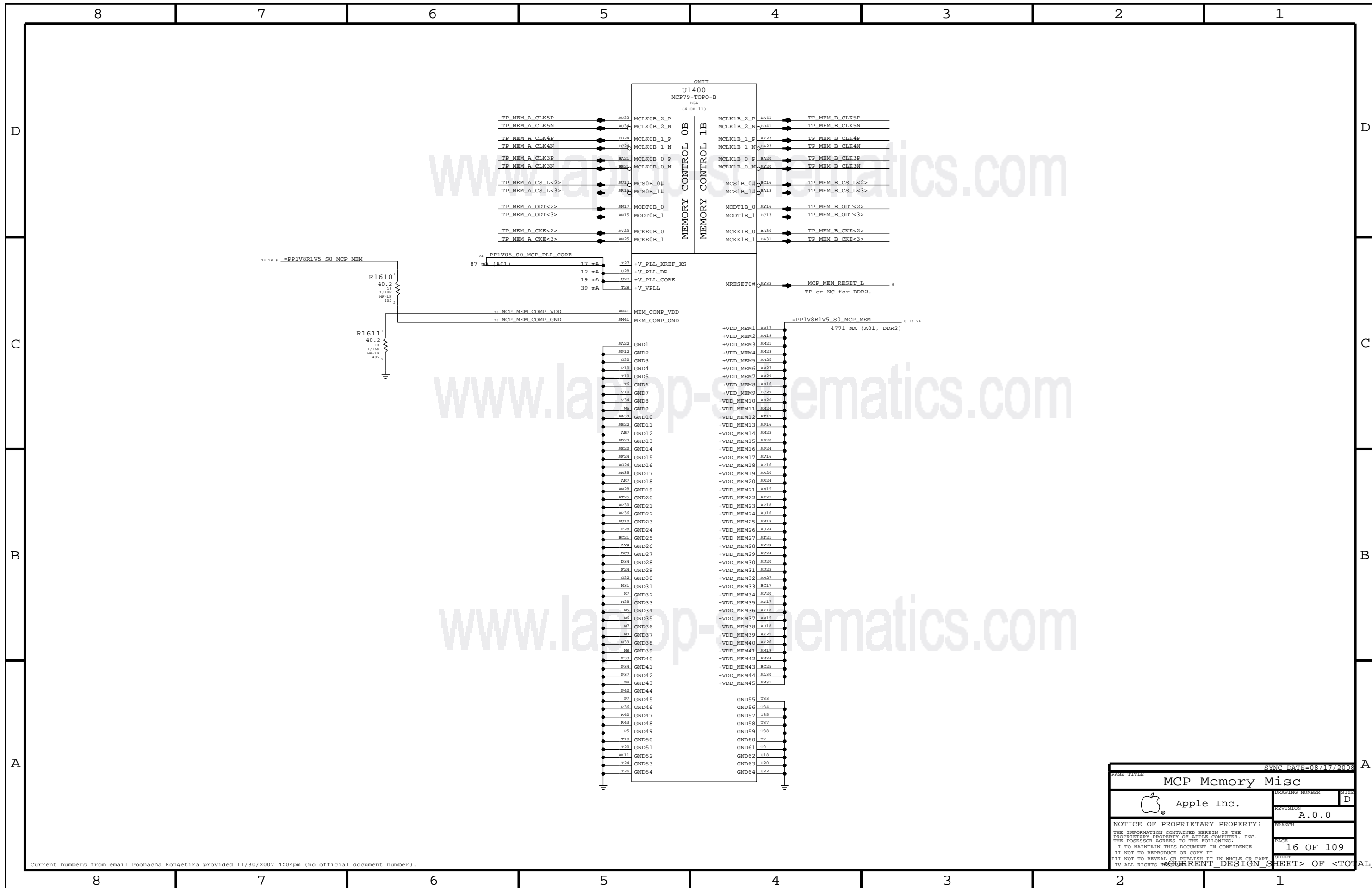
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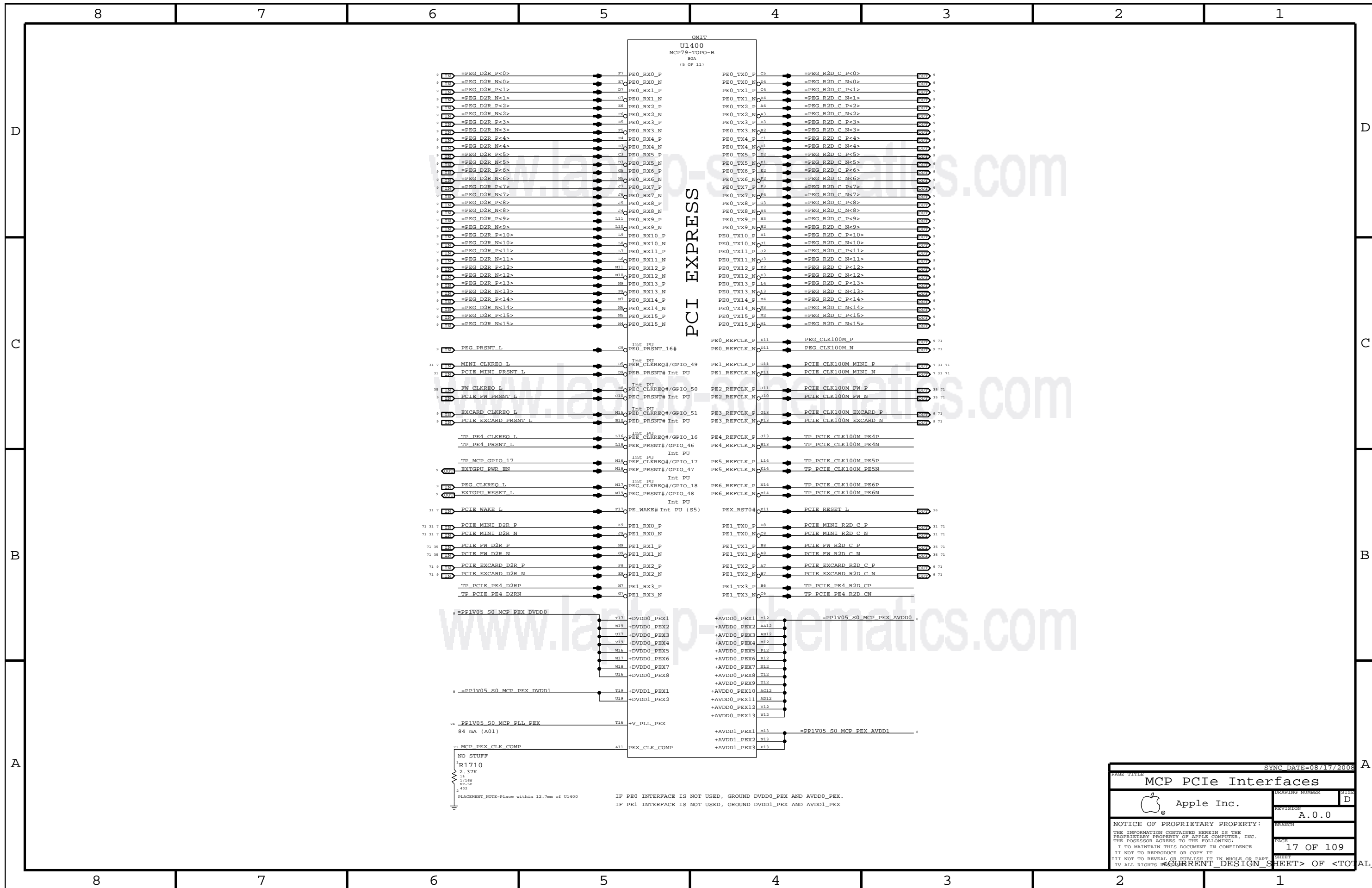
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PAGE TITLE		SYNC DATE=08/17/2008	
MCP Memory Misc		DESIGN NUMBER	M122
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SYNC DATE=08/17/2008

MCP PCIe Interfaces

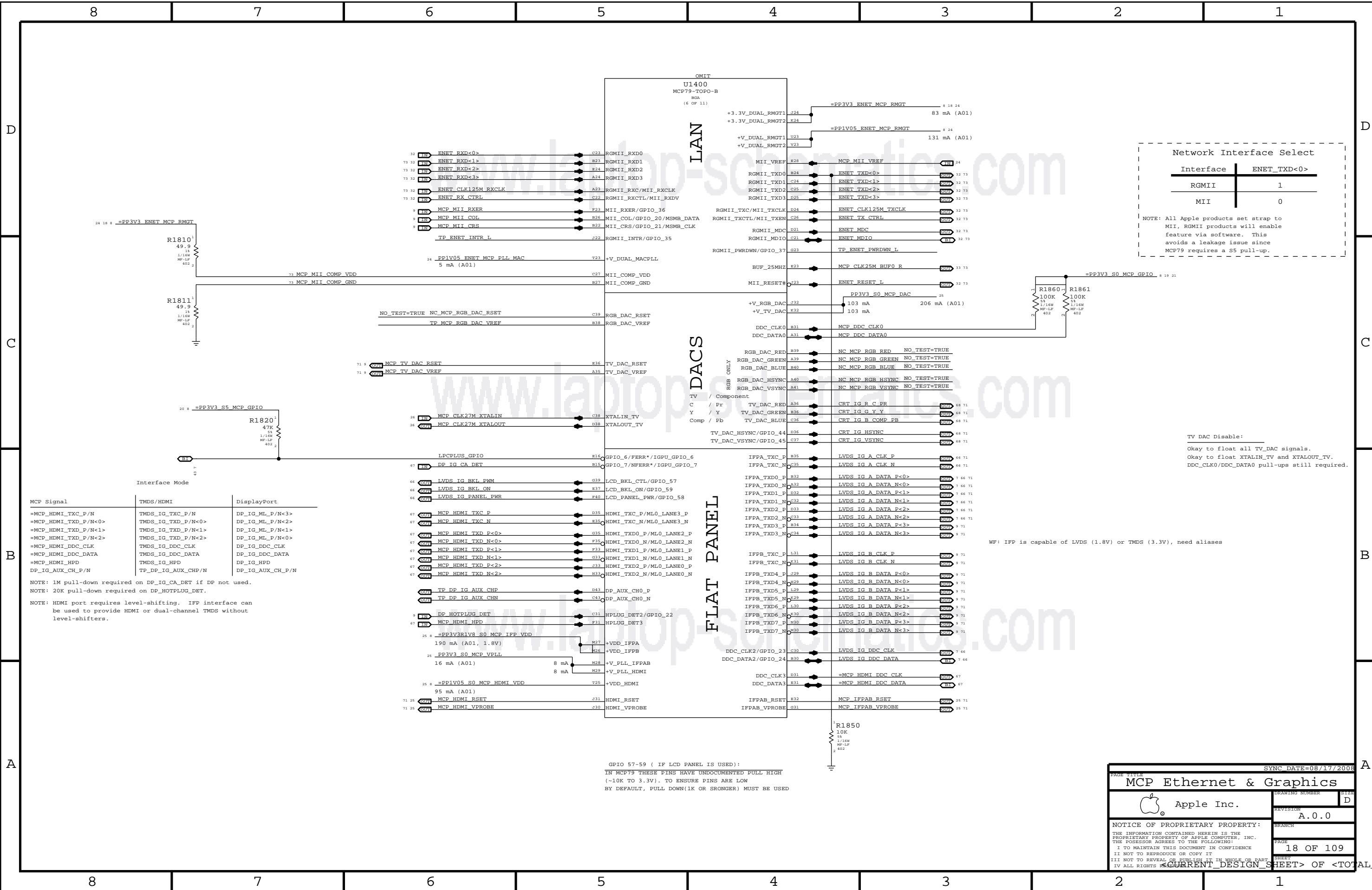
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DESIGN NUMBER: 1122
 SHEET: D



Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

TV DAC Disable:
 Okay to float all TV_DAC signals.
 Okay to float XTALIN_TV and XTALOUT_TV.
 DDC_CLK0/DDC_DATA0 pull-ups still required.

Interface Mode

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CH_P/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
 NOTE: 20K pull-down required on DP_HOTPLUG_DET.
 NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

GPIO 57-59 (IF LCD PANEL IS USED):
 IN MCP79 THESE PINS HAVE UNDOCUMENTED PULL HIGH (~10K to 3.3V). TO ENSURE PINS ARE LOW BY DEFAULT, PULL DOWN(1K OR STRONGER) MUST BE USED

SYNC DATE=08/17/2008

MCP Ethernet & Graphics

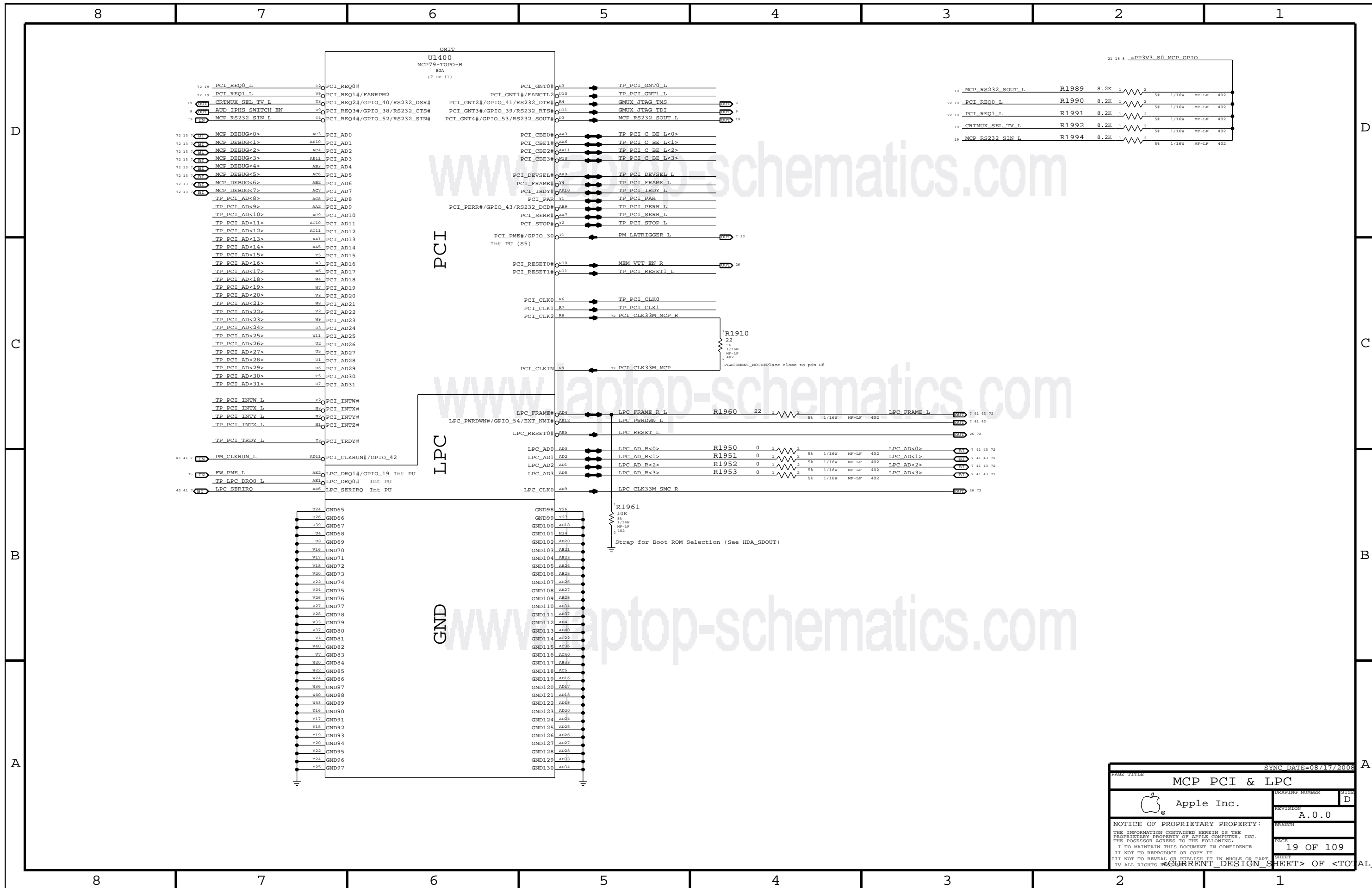
Apple Inc.

REVISION: A.0.0

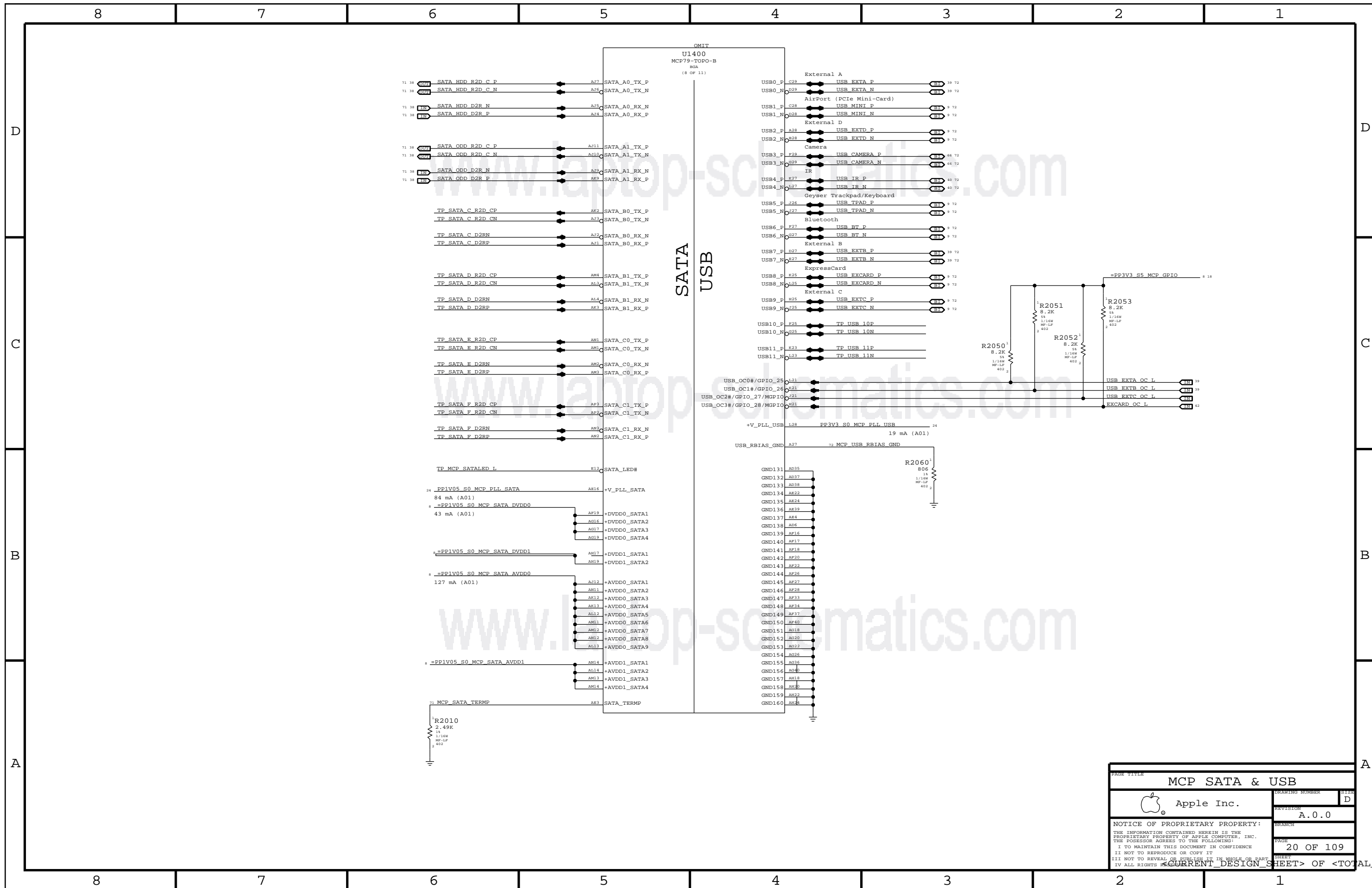
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PAGE TITLE		SYNC DATE=08/17/2008	
MCP PCI & LPC			
Apple Inc.		DRAWING NUMBER	M122
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PAGE TITLE		MCP SATA & USB	
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D

C

B

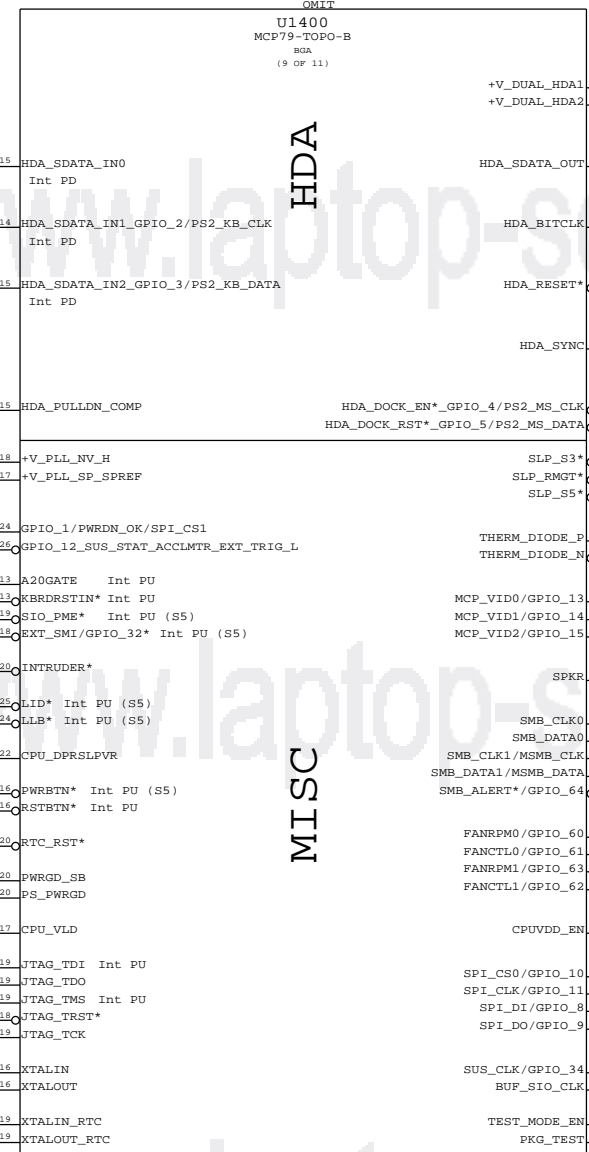
A

D

C

B

A



BIOS Boot Select

I/F	HDA_SDOUR	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L
 R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.
 NOTE: MCP79 does not support FW, only LPC ROMs. So Apple designs will not use LPC for BootROM override.
 NOTE: MCP79 rev A01 does not support SPI1 option.

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

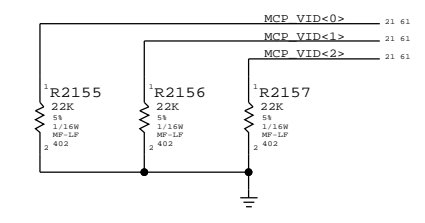
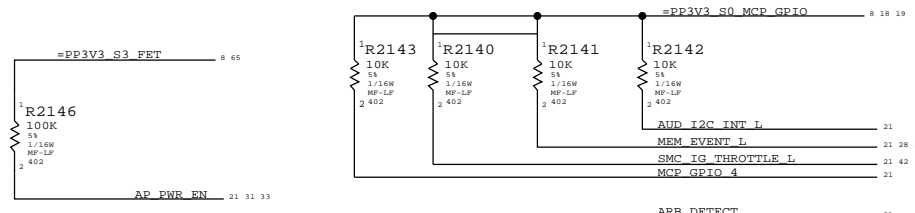
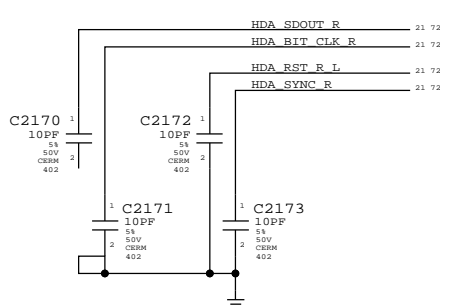
SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

HDA Output Caps

For EMI Reduction on HDA interface



SYNC DATE=08/17/2008

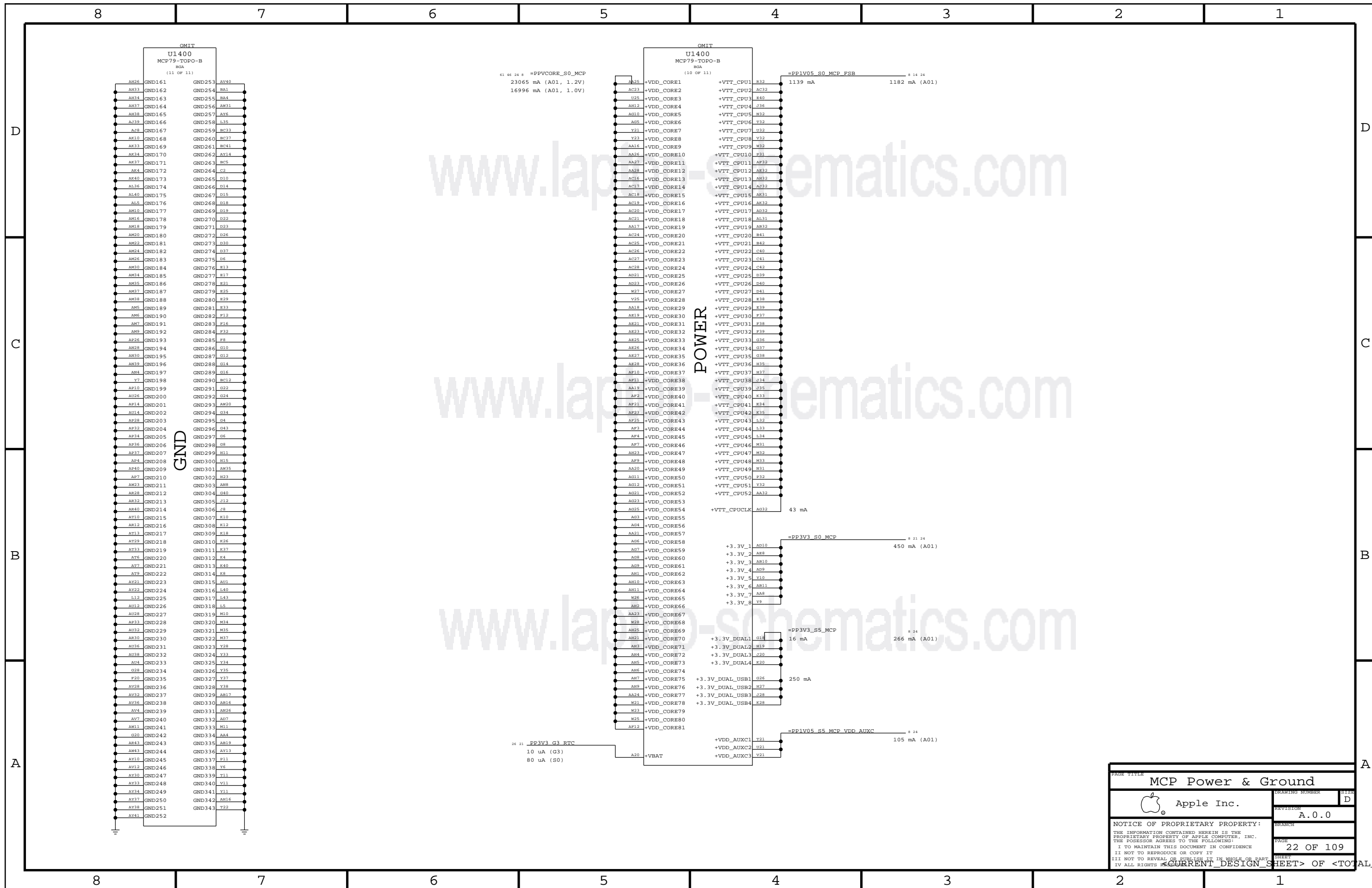
MCP HDA & MISC

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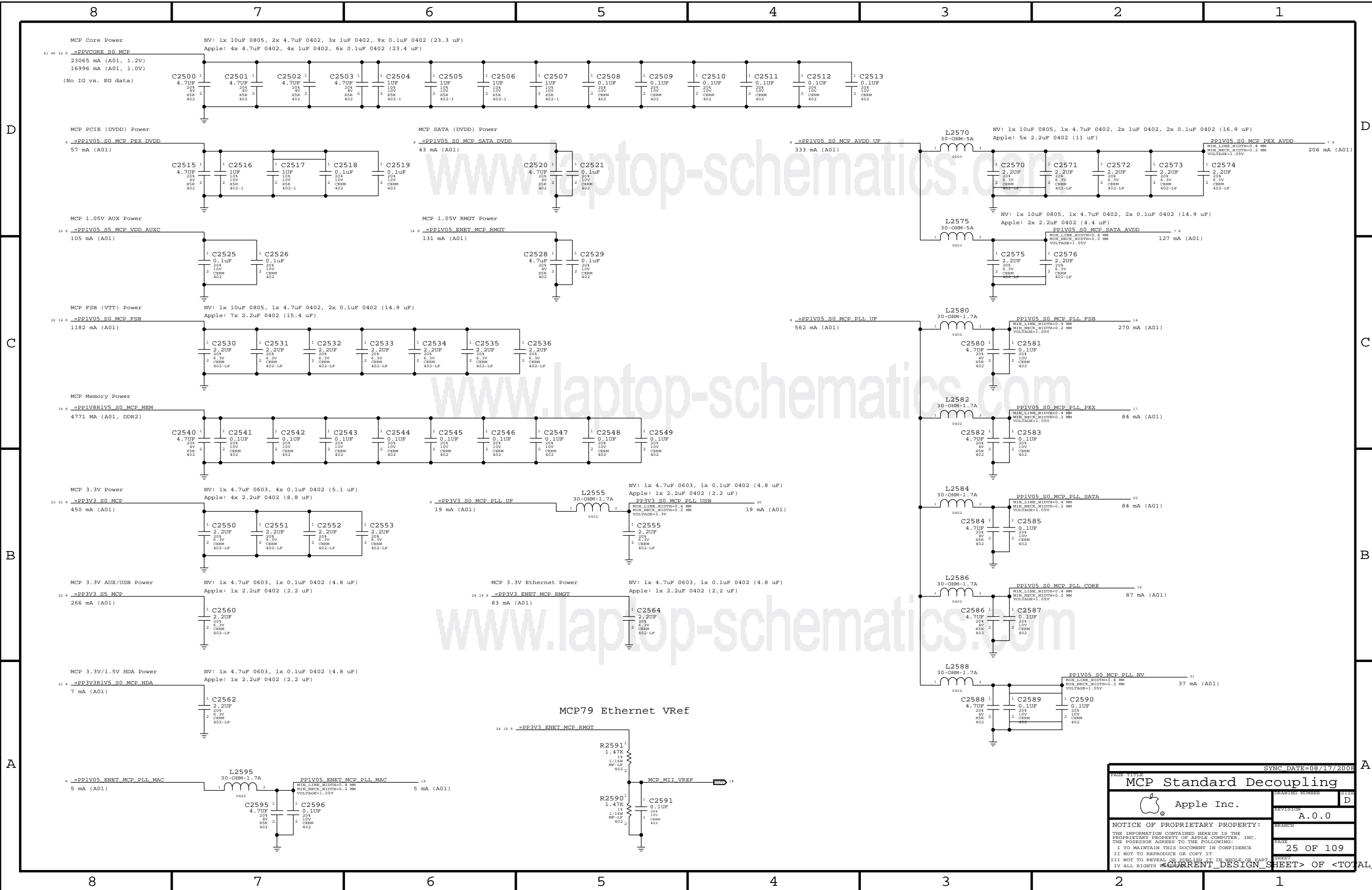
www.laptop-schematics.com

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PAGE TITLE MCP79 A01 Silicon Support	
 Apple Inc.	DRAWING NUMBER D
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SYNC DATE=08/17/2008

MCP Standard Decoupling

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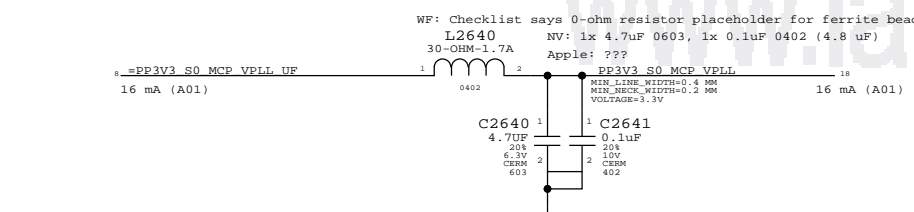
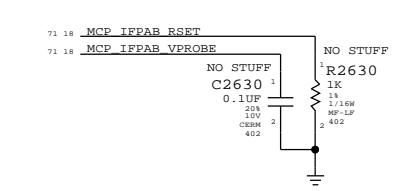
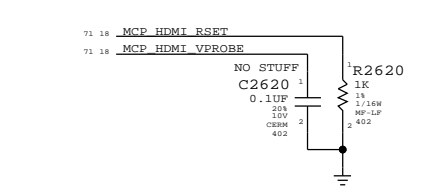
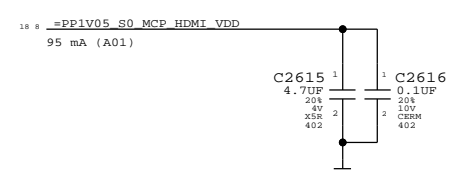
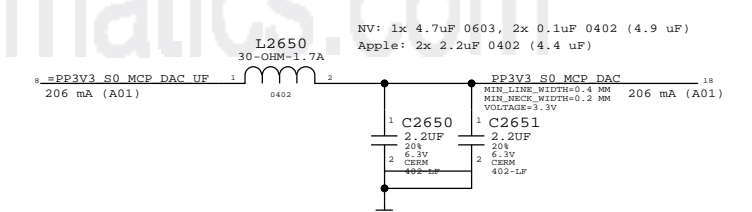
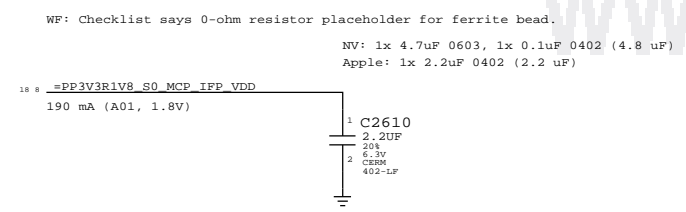
SHEET: 25 OF 109

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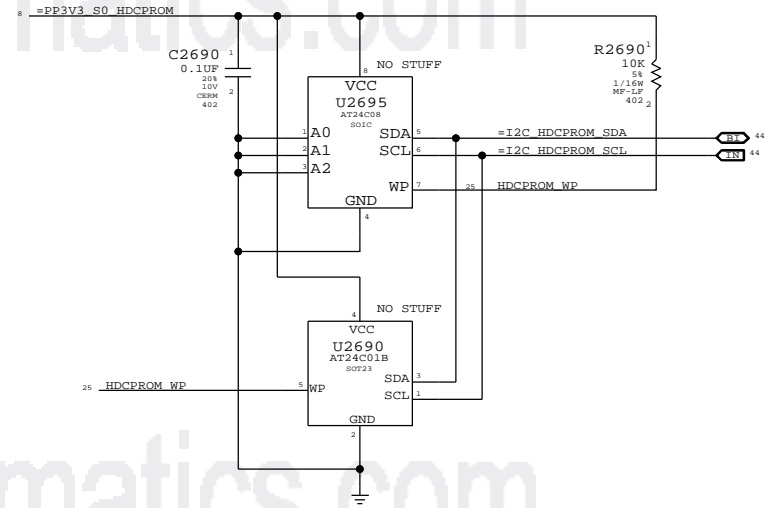
www.laptop-schematics.com

www.laptop-schematics.com



HDCP ROM

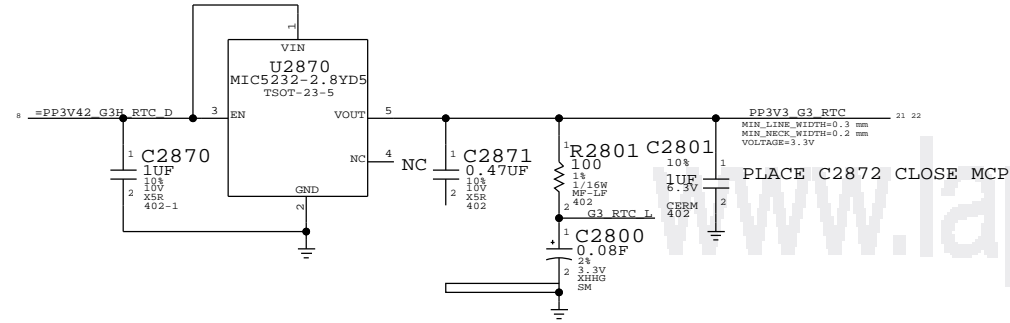
WF: Open question on which package option(s) nVidia can support.



SYNC FROM T18
 REMOVE MCP 27MHZ CRYSTAL CRICUIT SINCE NOT SUPPORTING TV-OUT
 REMOVE DAC TERMINATIONS R2665,C2665 AND R2670 TO R2672

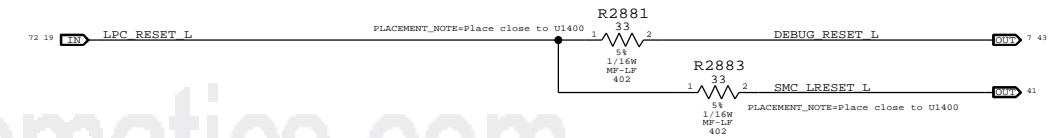
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MCP Graphics Support		REVISION NUMBER	SIZE
Apple Inc.		A.0.0	D
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RTC Power Sources

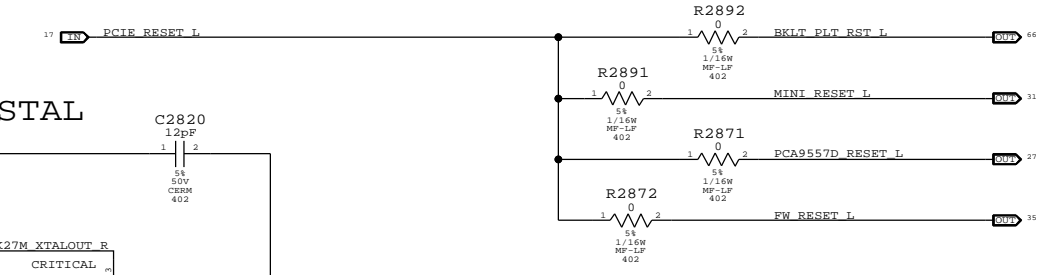


Platform Reset Connections

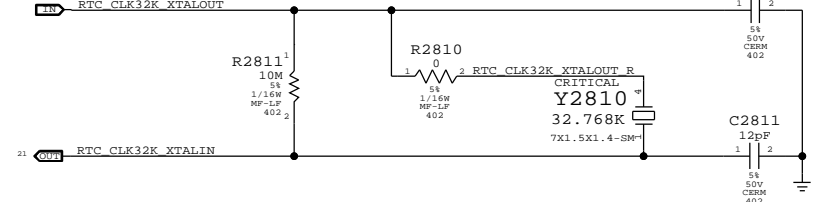
LPC Reset (Unbuffered)



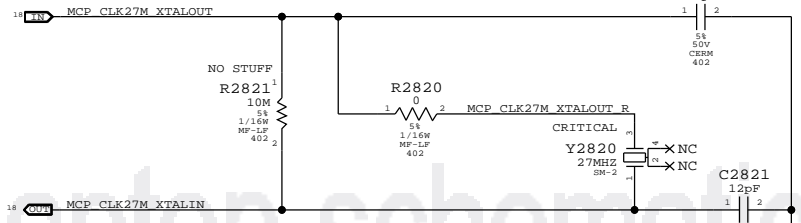
PCIE Reset (Unbuffered)



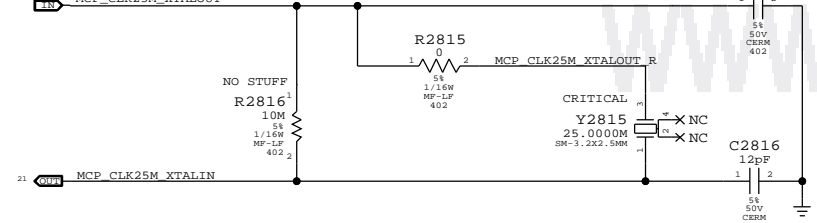
RTC Crystal



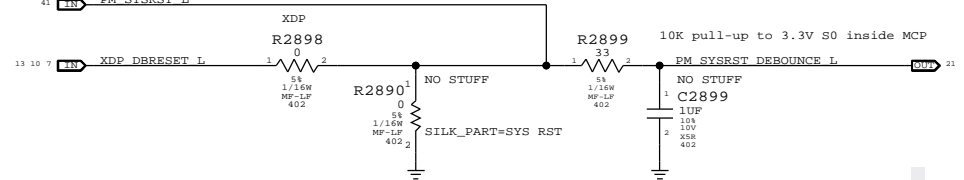
MCP 27MHZ CRYSTAL



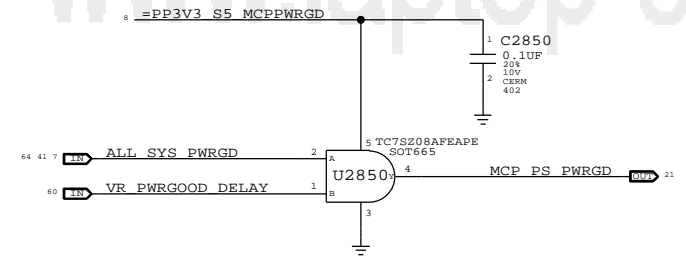
MCP 25MHz Crystal



Reset Button



MCP S0 PWRGD



SYNC FROM T18
 CHANGE RESET BUTTON TO RESET PADS
 REMOVE UNUSED PCIE RESET SIGNALS
 REMOVE R2824 AND NET PCI_CLK33M_SLOT_A
 CHANGE RTC POWER SOURCE FROM COIN CELL TO SUPER CAPS
 ALIAS MEM_VTT_EN TO =DDRVTT_EN
 CHANGE Y2810 AND U2850 TO SMALLER PARTS

PAGE TITLE		SB Misc	
DRAWING NUMBER		M122 D	
REVISION		A.0.0	
BRANCH			
PAGE		28 OF 109	
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SHEET			
SHEET			
SHEET			

Page Notes

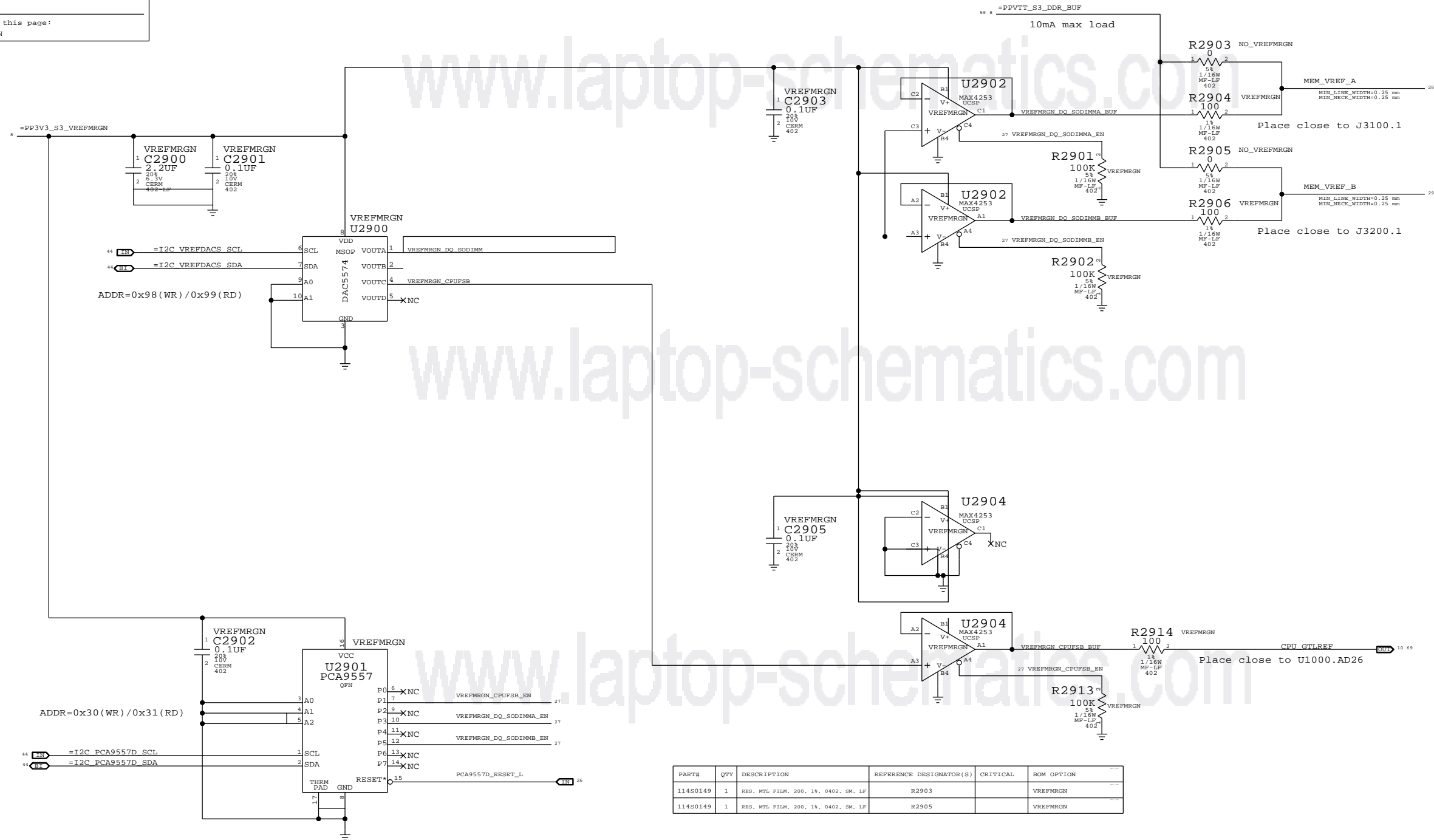
Power aliases required by this page:
 - =PP3V3_S3_VREFMRGN
 - =PP3V3_S5_VREFMRGN
 - =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
 - =I2C_VREFDACS_SCL
 - =I2C_VREFDACS_SDA
 - =I2C_PCA9557D_SCL
 - =I2C_PCA9557D_SDA

BOM options provided by this page:
 VREFMRGN AND NO_VREFMRGN

Voltage divider resistor values at op-amp outputs not yet finalized.

BOM OPTION TO SELECT VREF SOURCE



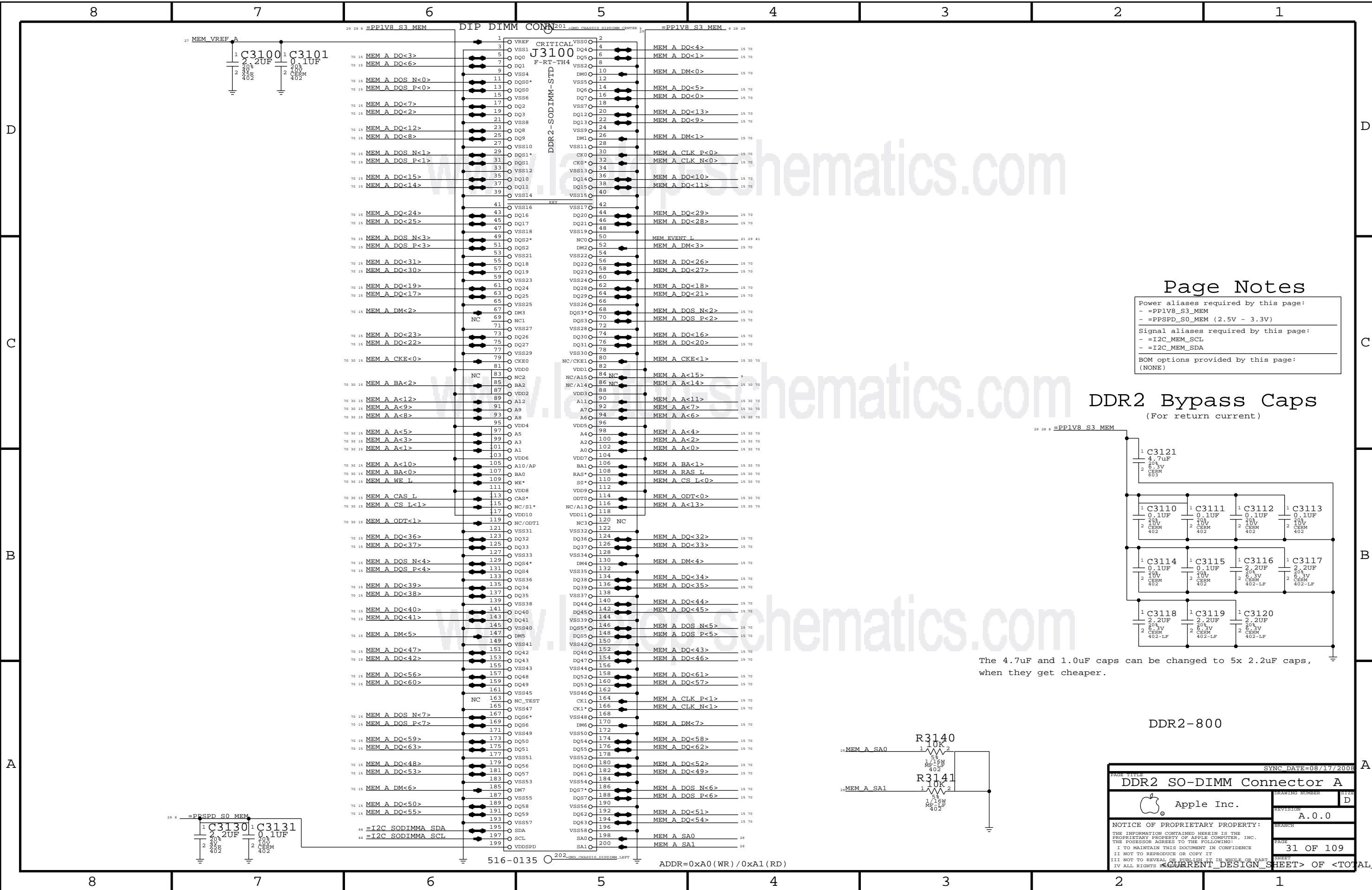
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0149	1	RES. MTL FILM, 200, 1%, 0402, SM, LF	R2903		VREFMRGN
114S0149	1	RES. MTL FILM, 200, 1%, 0402, SM, LF	R2905		VREFMRGN

PAGE TITLE
FSB/DDR2 VREF MARGINING

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DRAWING NUMBER: 1144
 REVISION: A.0.0
 BRANCH:
 PAGE: 29 OF 109
 SHEET: 1



Page Notes

Power aliases required by this page:
 - =PPIV8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

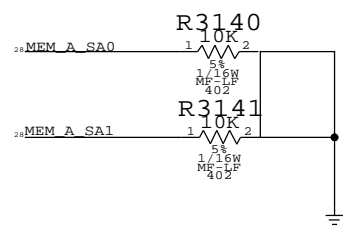
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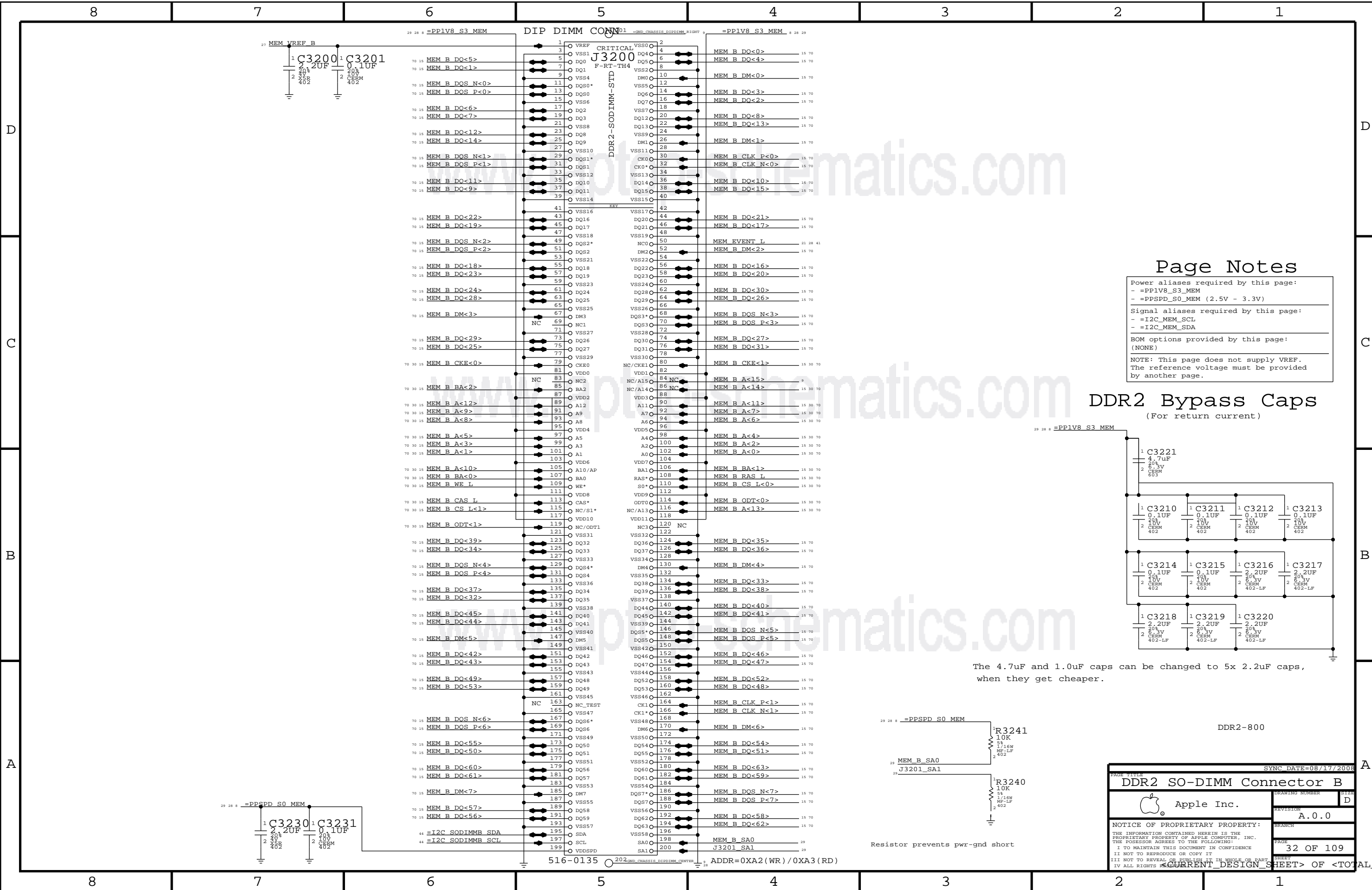
DDR2 Bypass Caps (For return current)

The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps, when they get cheaper.

DDR2-800

PAGE TITLE		SYNC DATE=08/17/2008	
DDR2 SO-DIMM Connector A		CREATING NUMBER	1122
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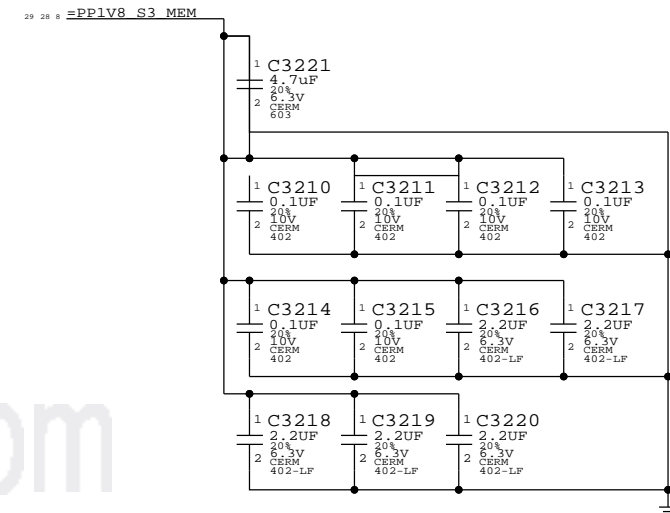
Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

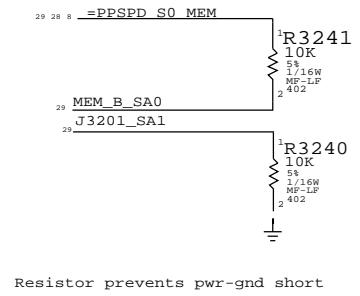
BOM options provided by this page:
 (NONE)

NOTE: This page does not supply VREF.
 The reference voltage must be provided
 by another page.

DDR2 Bypass Caps (For return current)



The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps, when they get cheaper.



Resistor prevents pwr-gnd short

DDR2-800

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SYNC DATE=08/17/2008

REVISION: A.0.0

CURRENT DESIGN SHEET OF TOTAL DESIGN SHEETS

516-0135 ADDR=0XA2(WR)/0XA3(RD)

8

7

6

5

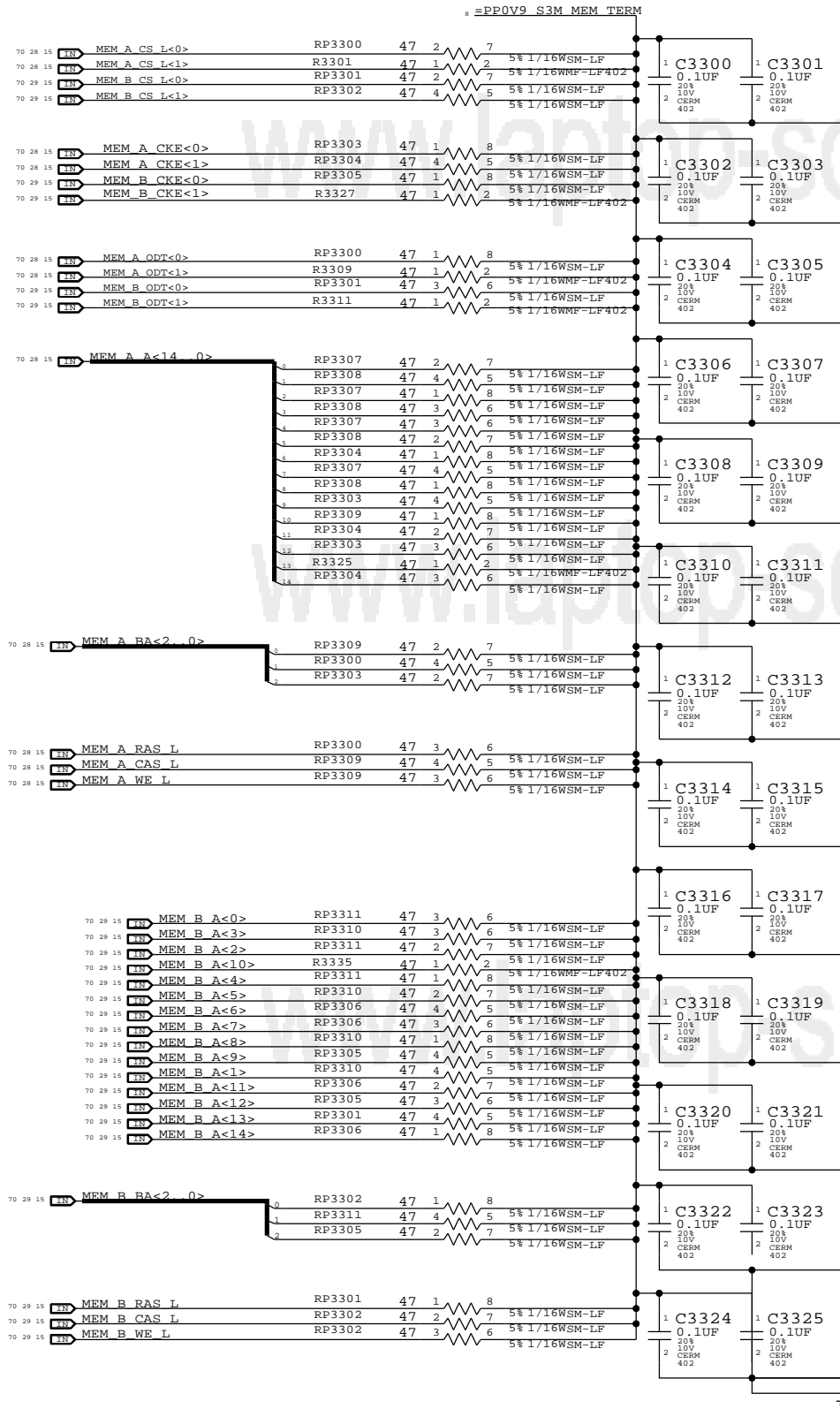
4

3

2

1

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



LAYOUT NOTE: PLACE ONE CAP CLOSE TO EVERY TWO PULLUP RESISTORS TERMINATED TO PP0V9_S0_MEM_TERM

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Memory Active Termination		D	
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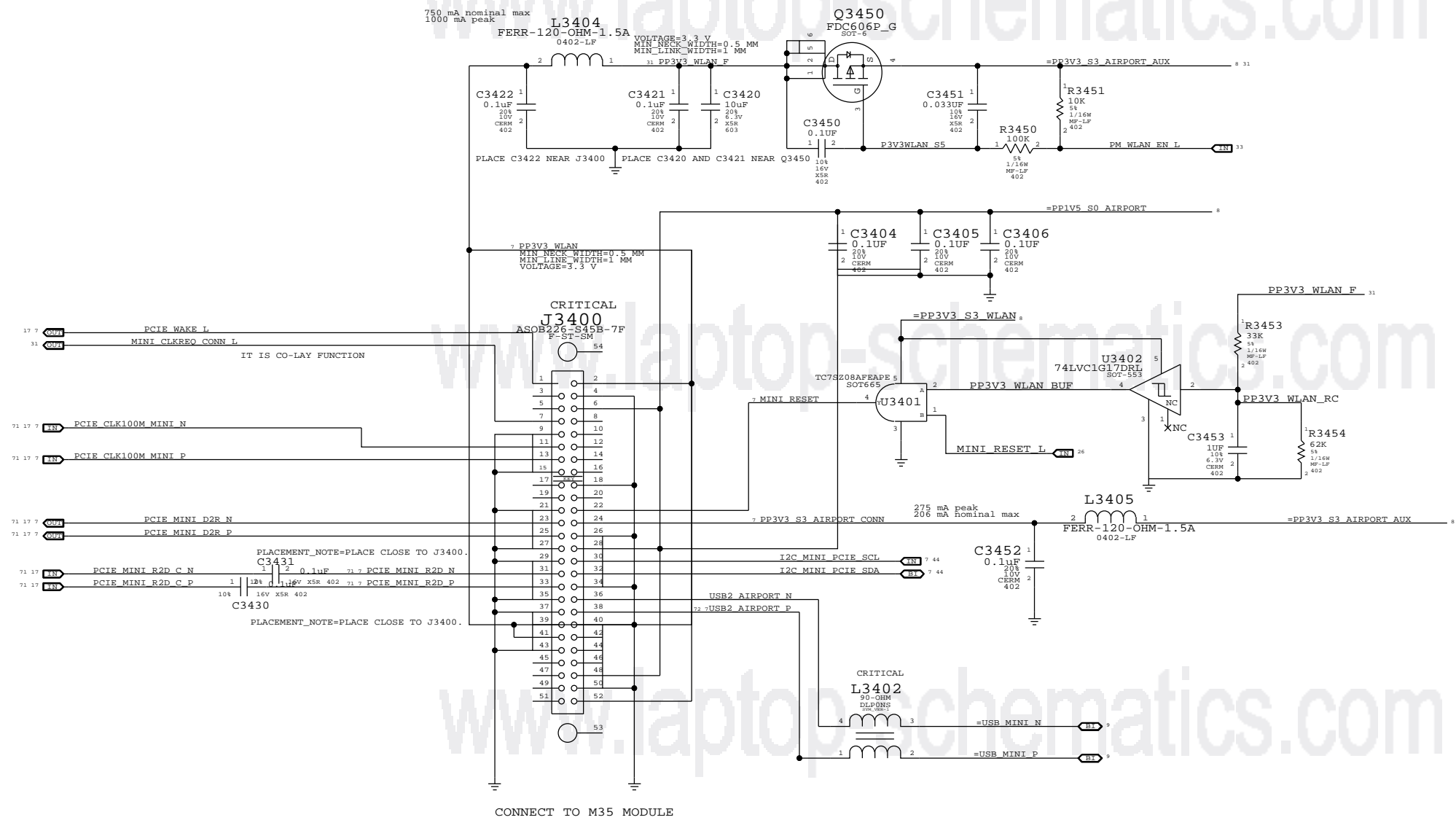
3

2

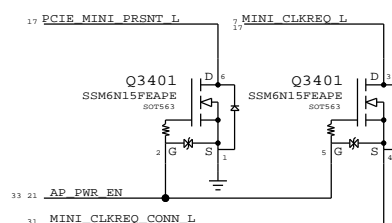
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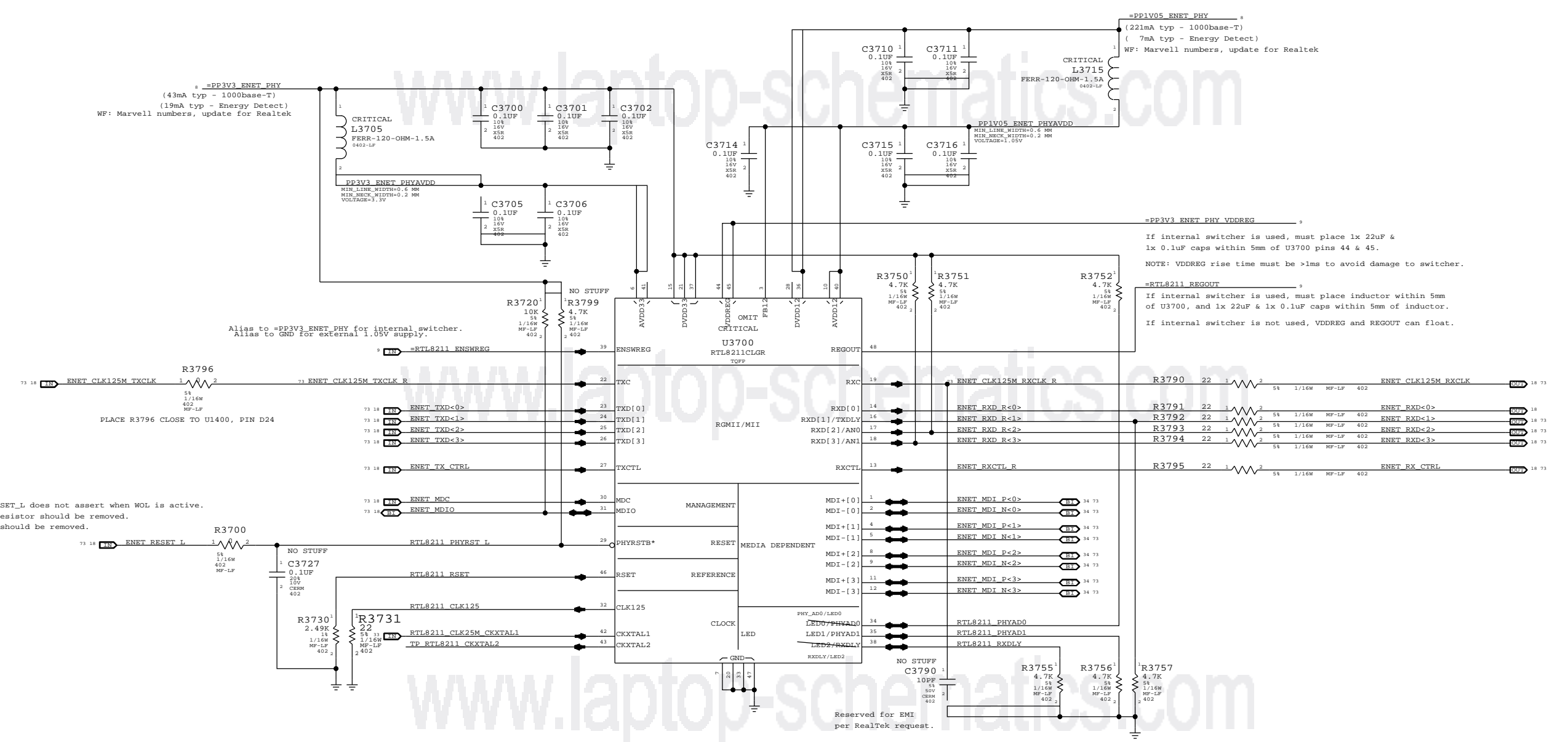
AIRPORT



OLD:516S0406 (FOXCONN ONLY)
NEW:516S0635 (FOXCONN & ACON)



PAGE TITLE		DRAWING NUMBER	
Right Clutch Connector		D	
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WF: Verify that ENET_RESET_L does not assert when WOL is active. If true, RC and 0-ohm resistor should be removed. If false, ENET_RESET_L should be removed.

If internal switcher is used, must place 1x 22uF & 1x 0.1uF caps within 5mm of U3700 pins 44 & 45. NOTE: VDDREG rise time must be >1ms to avoid damage to switcher.

If internal switcher is used, must place inductor within 5mm of U3700, and 1x 22uF & 1x 0.1uF caps within 5mm of inductor. If internal switcher is not used, VDDREG and REGOUT can float.

Configuration Settings:
 PHYAD = 01 (PHY Address 00001)
 AN[1:0] = 11 (Full auto-negotiation)
 RXDLY = 0 (RXCLK transitions with data)
 TXDLY = 0 (No TXCLK Delay)

SYNC DATE=03/20/2008

Ethernet PHY (RTL8211CL)

Apple Inc.

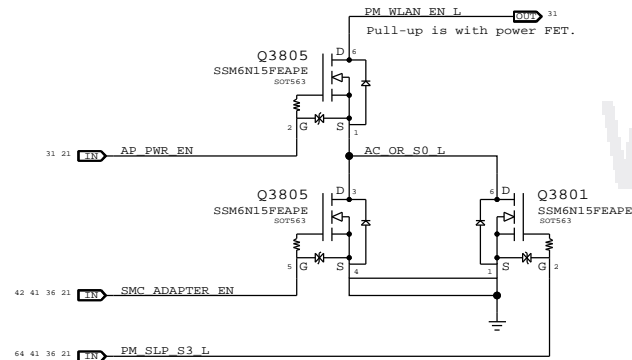
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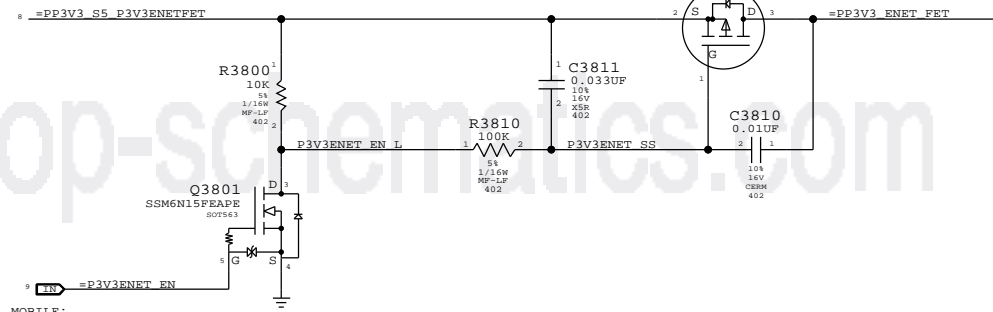
WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
 NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



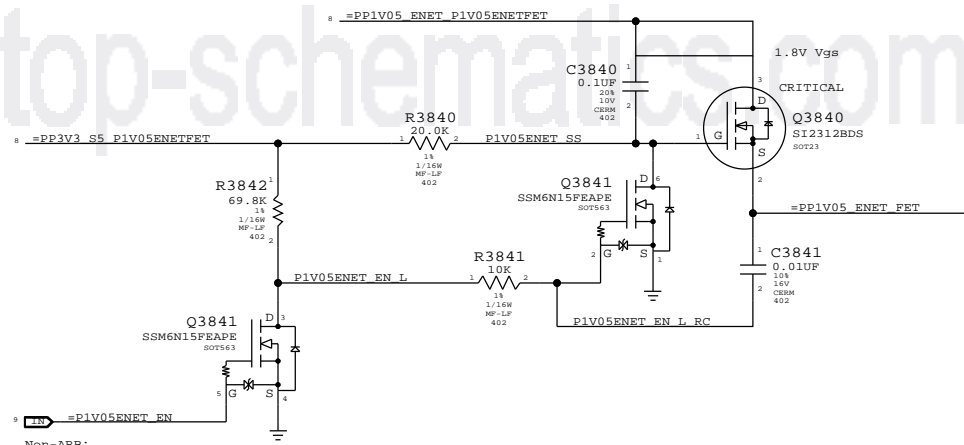
3.3V ENET FET

CRITICAL
 @ 2.5V Vgs:
 Rds(on) = 90mOhm max
 I(max) = 1.7A (85C)



MOBILE:
 Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

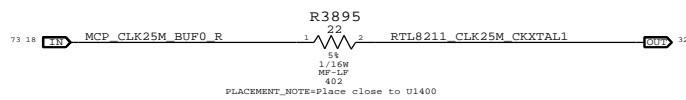
1.05V ENET FET



Non-ARB:
 Recommend aliasing PM_SLP_RMGT_L and =P1V05ENET_EN. Nets separated on ARB for alternate power options.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered. Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



SYNC DATE=04/04/2008

Ethernet & AirPort Support

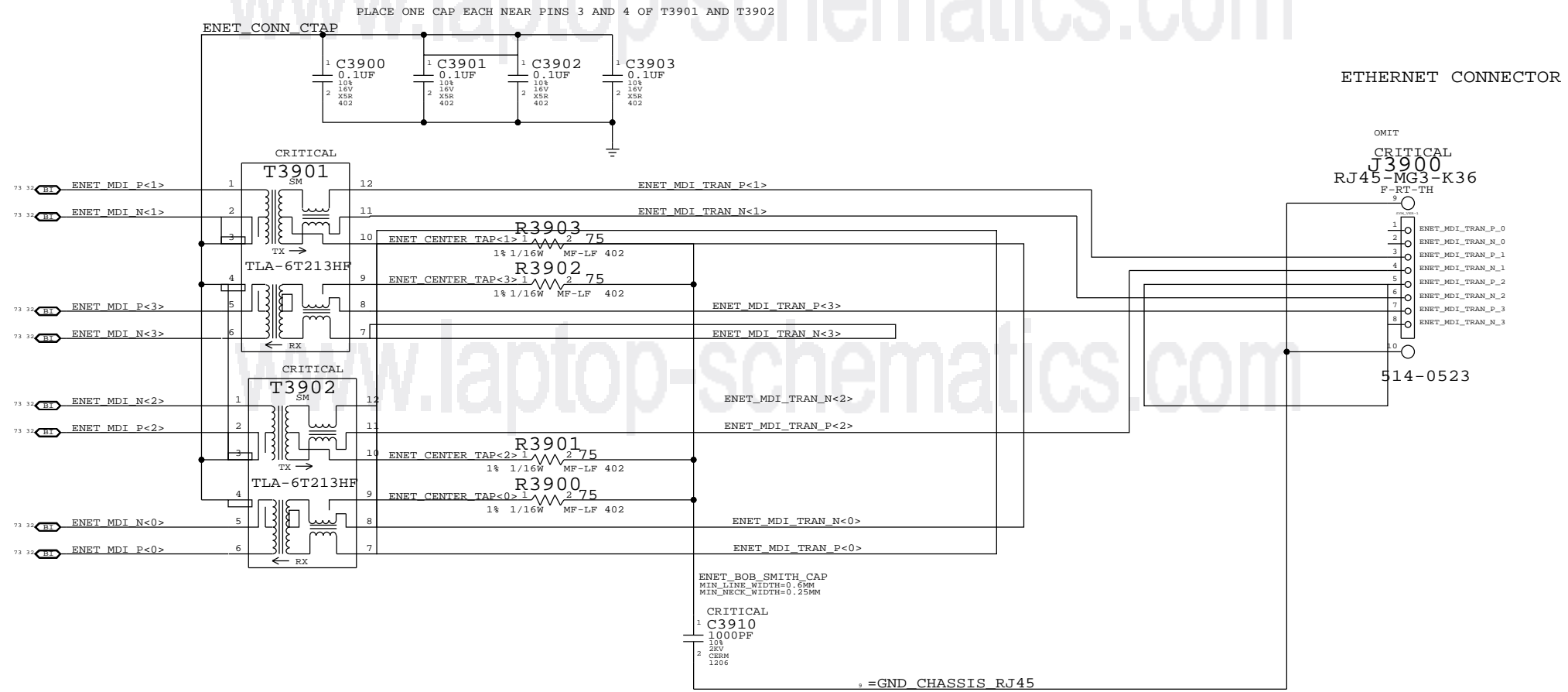
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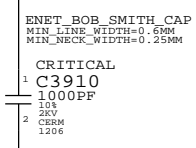
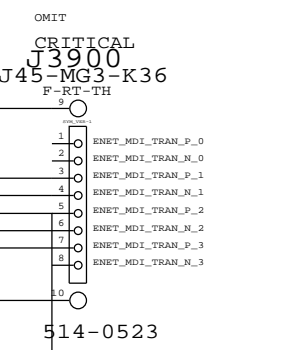
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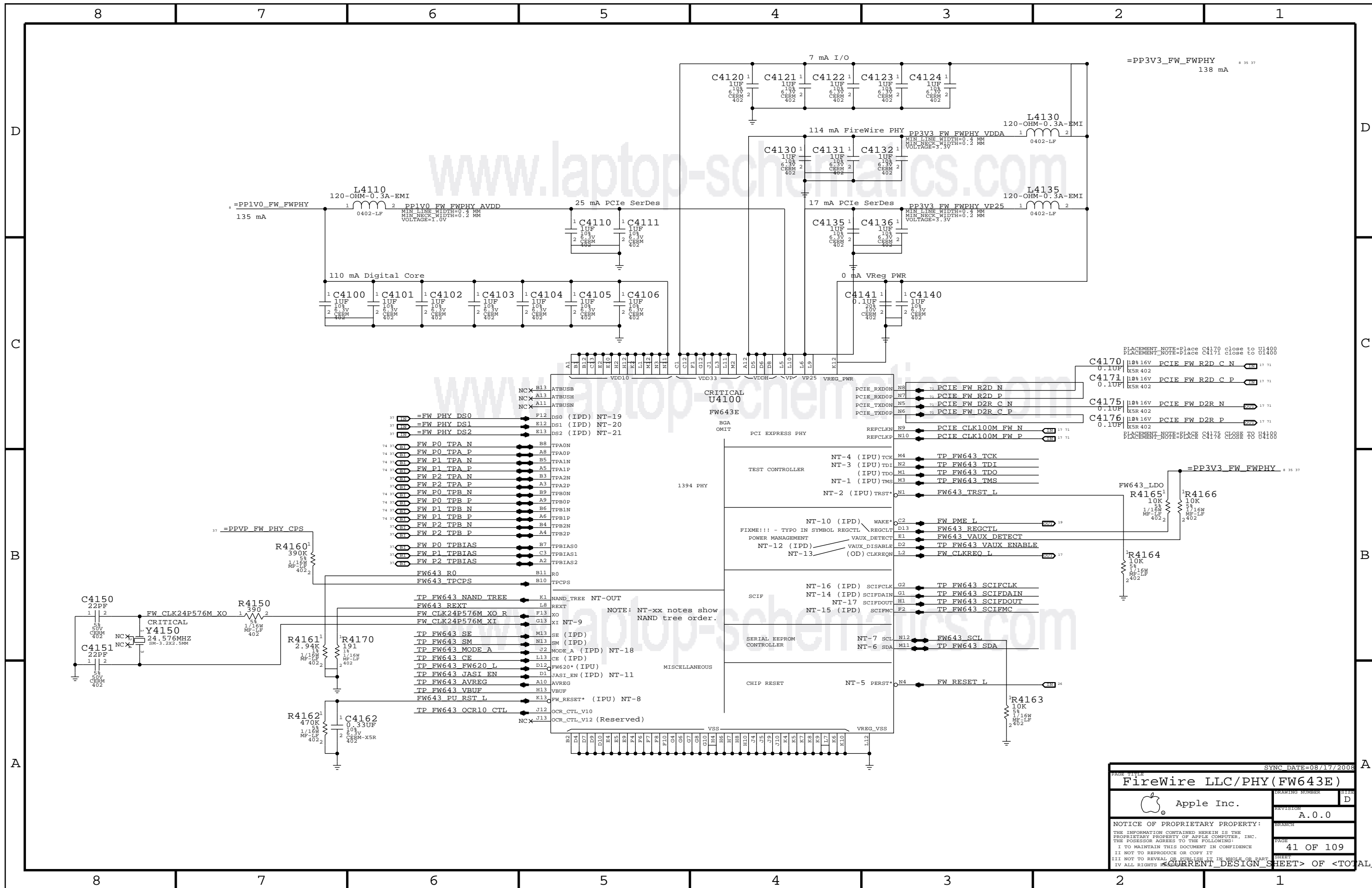
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ETHERNET CONNECTOR



PAGE TITLE		SYNC DATE=04/04/2008	
ETHERNET CONNECTOR		DESIGN NUMBER	REV D
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PAGE TITLE		SYNC DATE=08/17/2008	
FireWire LLC/PHY (FW643E)		CREATING NUMBER	1122
Apple Inc.		REVISION	A.0.0
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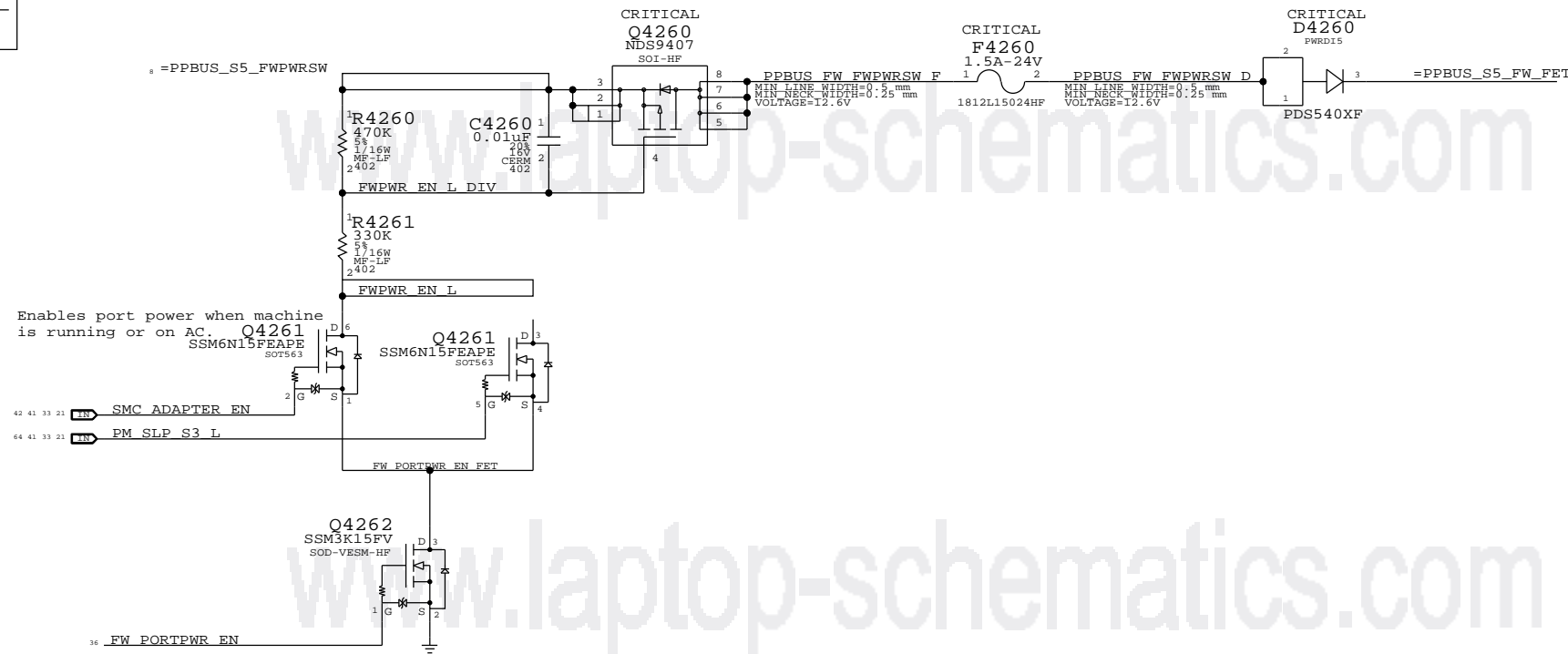
Page Notes

Power aliases required by this page:
 - =PPBUS_S5_FWPWSW (system supply for bus power)
 - =PP3V3_FW_LATEVG_ACTIVE
 - =PPVP_FW_SUMNODE (power passthru summation node)

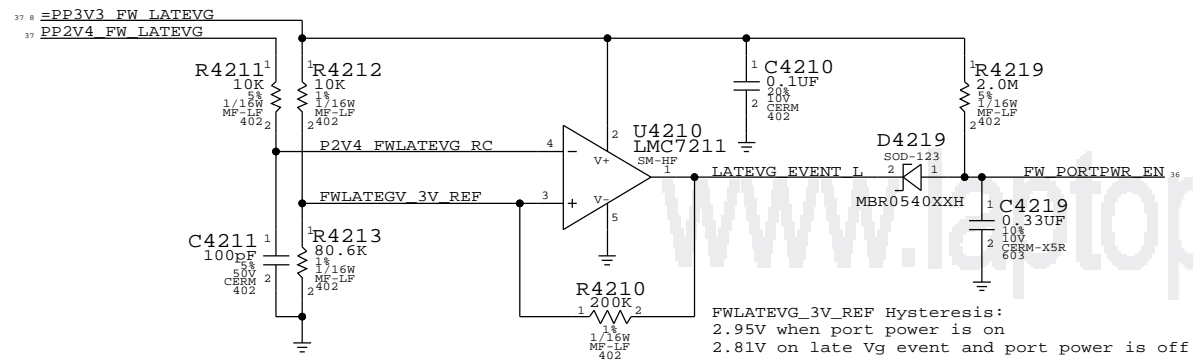
Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - FW_PORT_FAULT_PU

FireWire Port Power Switch



Late-VG Event Detection



PAGE TITLE		FireWire Port Power	
DRAWING NUMBER		D	
REVISION		A.0.0	
BRANCH			
PAGE		42 OF 109	
SHEET			
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Page Notes

Power aliases required by this page:
 - =PPVP_FW_PORT1
 - =PP3V3_FW_LATEVG

Signal aliases required by this page:
 (NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

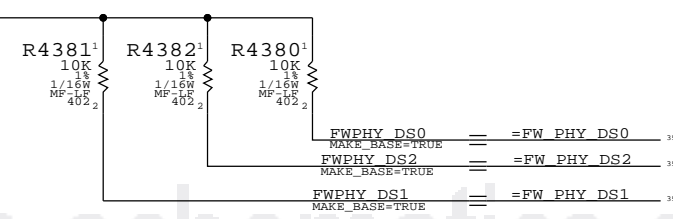
BOM options provided by this page:
 (NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

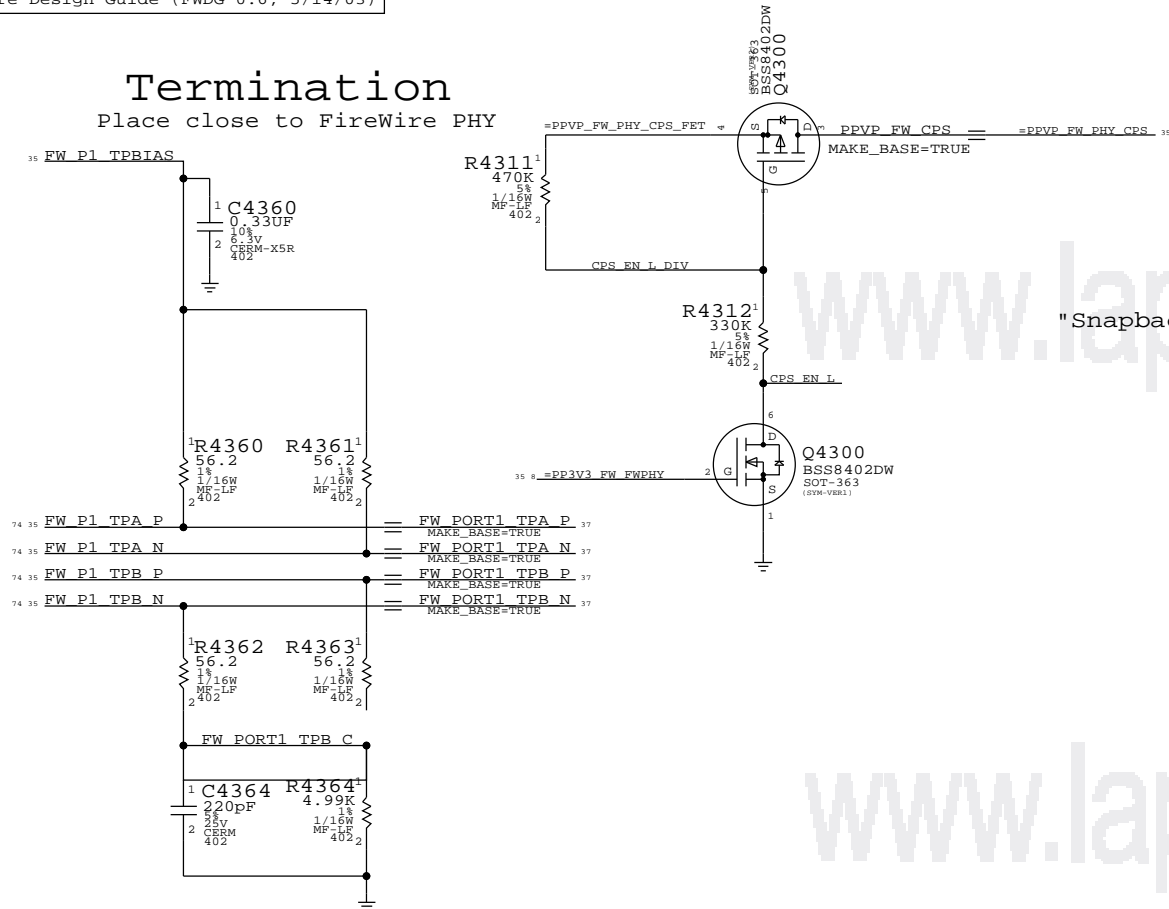
Configures PHY for:
 - 1-port Portable Power Class (0)



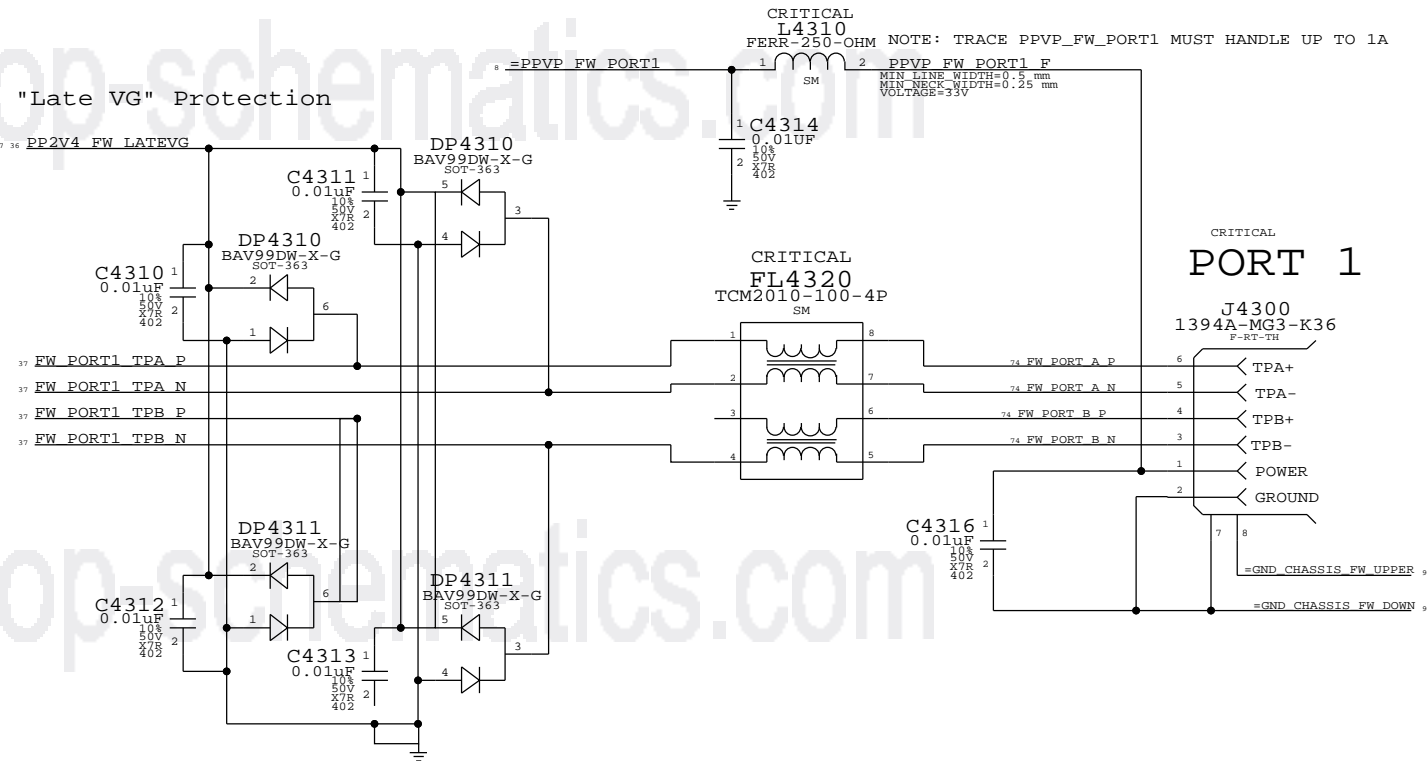
35	FW_P0_TPB_IAS	==	NC_FW0_TPB_IAS	MAKE_BASE=TRUE
35	FW_P2_TPB_IAS	==	NC_FW2_TPB_IAS	MAKE_BASE=TRUE
74	FW_P0_TPA_N	==	NC_FW0_TPA_N	MAKE_BASE=TRUE
74	FW_P0_TPA_P	==	NC_FW0_TPA_P	MAKE_BASE=TRUE
35	FW_P2_TPA_N	==	NC_FW2_TPA_N	MAKE_BASE=TRUE
35	FW_P2_TPA_P	==	NC_FW2_TPA_P	MAKE_BASE=TRUE
74	FW_P0_TPB_N	==	NC_FW0_TPB_N	MAKE_BASE=TRUE
74	FW_P0_TPB_P	==	NC_FW0_TPB_P	MAKE_BASE=TRUE
35	FW_P2_TPB_N	==	NC_FW2_TPB_N	MAKE_BASE=TRUE
35	FW_P2_TPB_P	==	NC_FW2_TPB_P	MAKE_BASE=TRUE

Termination

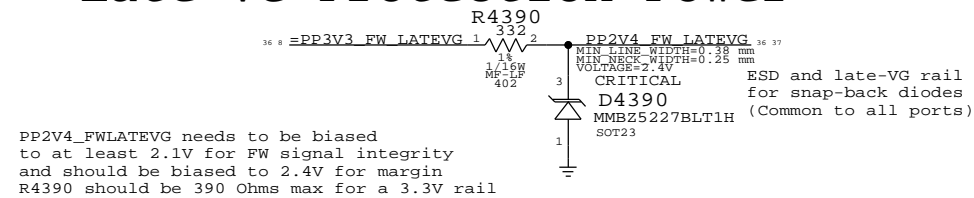
Place close to FireWire PHY



"Snapback" & "Late VG" Protection



Late-VG Protection Power



PAGE TITLE		SYNC DATE=(MASTER)	
FireWire Ports		CREATING NUMBER	1122
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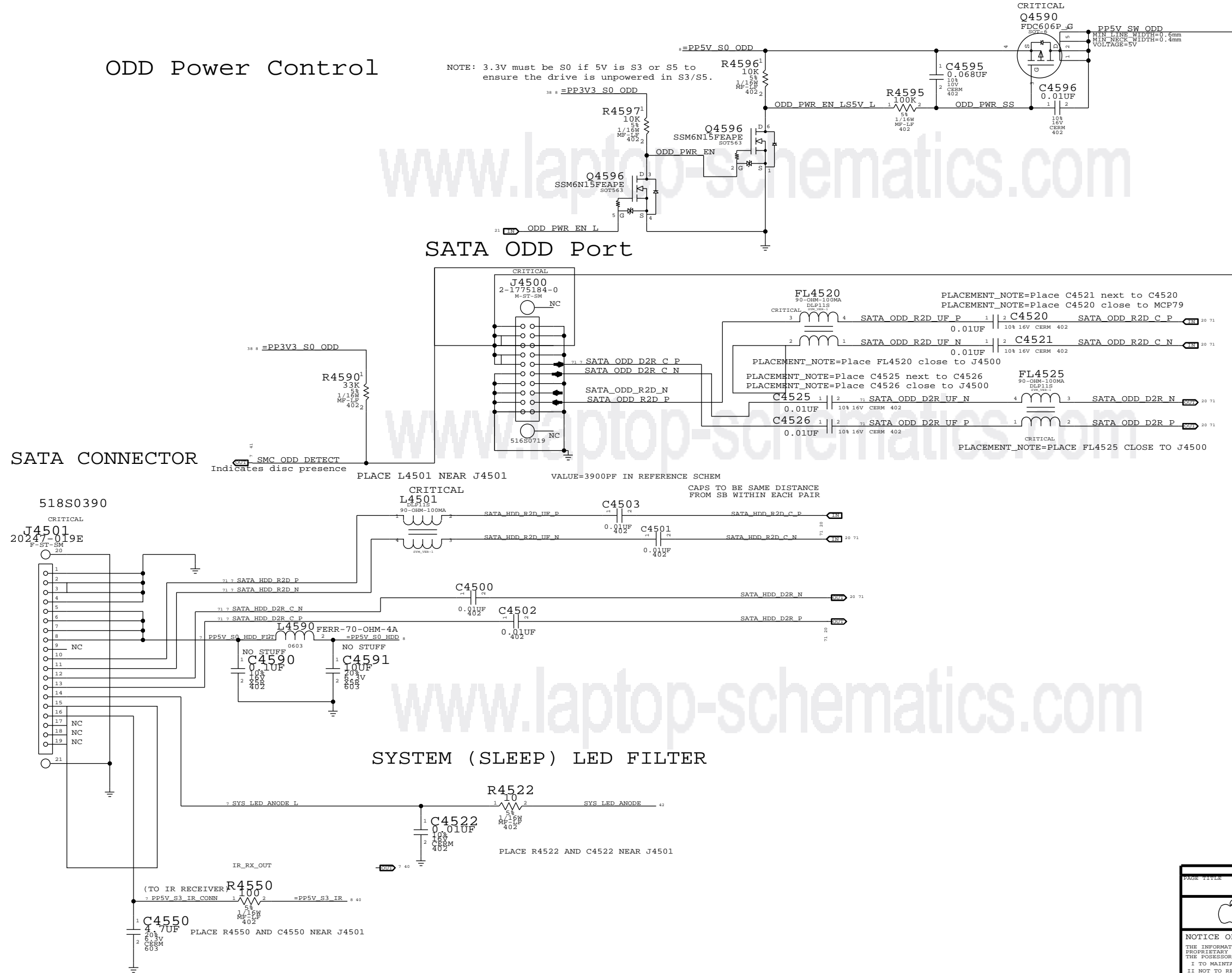
ODD Power Control

NOTE: 3.3V must be S0 if 5V is S3 or S5 to ensure the drive is unpowered in S3/S5.

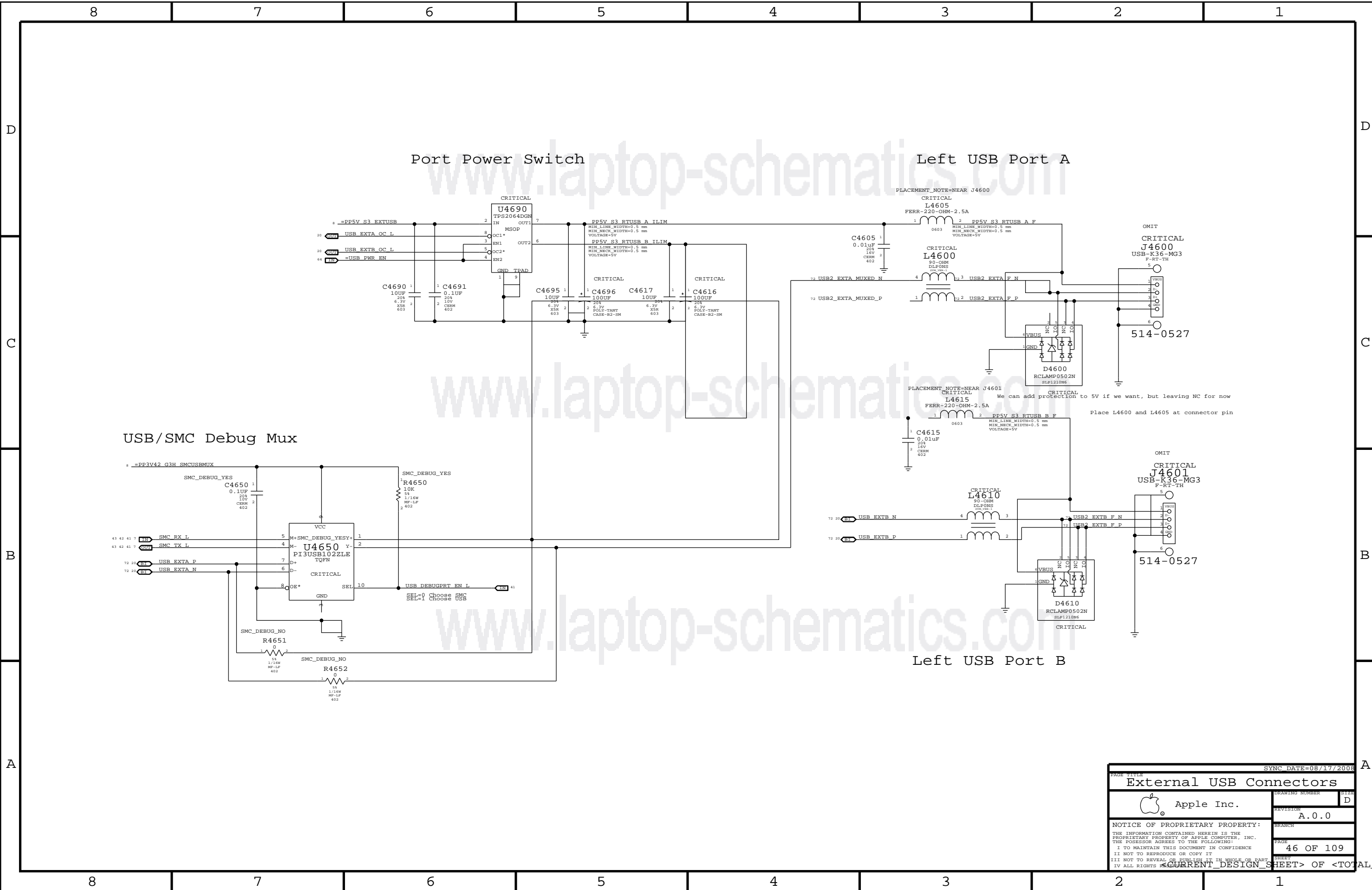
SATA ODD Port

SATA CONNECTOR

SYSTEM (SLEEP) LED FILTER



PAGE TITLE		SYNC DATE=08/17/2008	
SATA Connectors		DESIGN NUMBER	M122
Apple Inc.		REVISION	A.0.0
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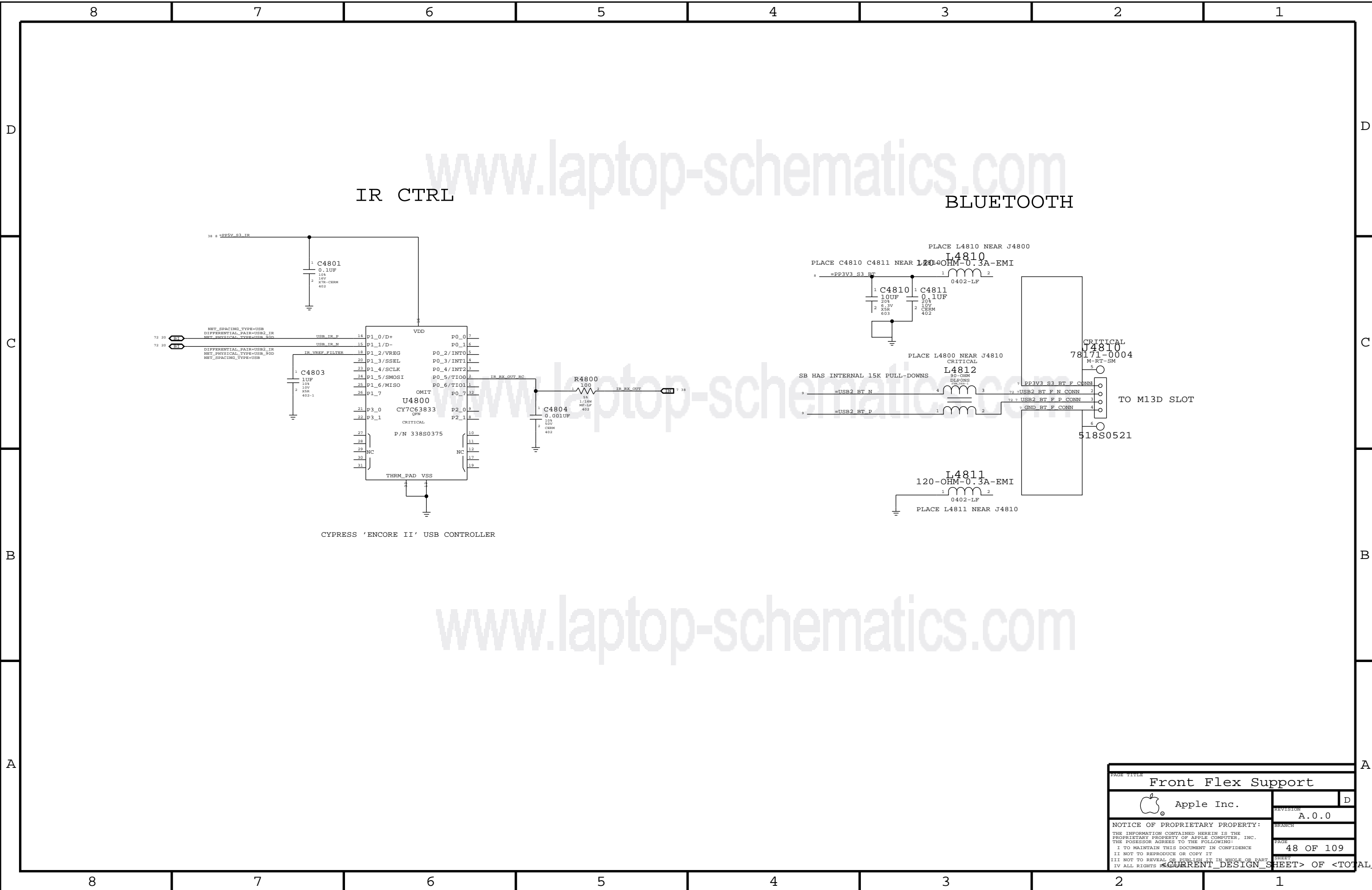
Port Power Switch

Left USB Port A

USB/SMC Debug Mux

Left USB Port B

PAGE TITLE		SYNC DATE=08/17/2008	
External USB Connectors			
 Apple Inc.		DESIGN NUMBER	1122
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IR CTRL

BLUETOOTH

CYPRESS 'ENCORE II' USB CONTROLLER

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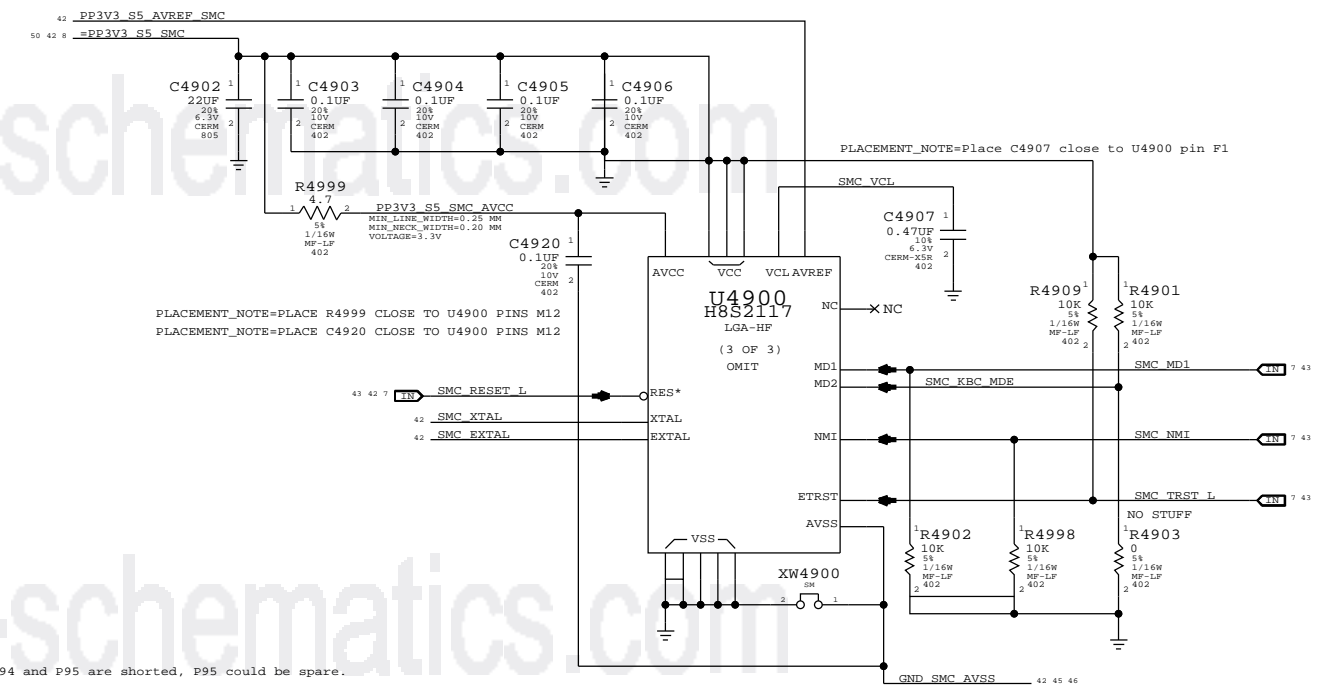
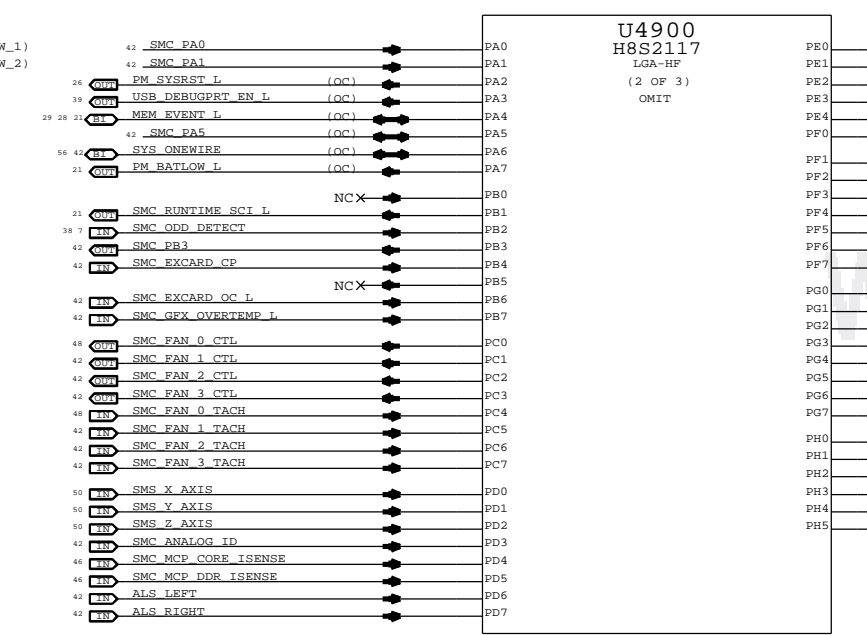
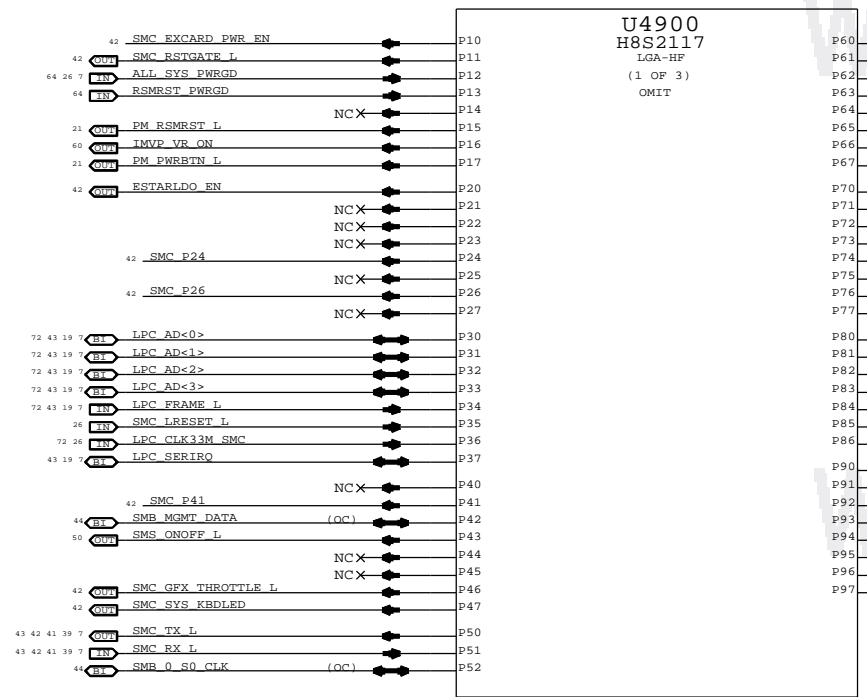
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NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



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PAGE TITLE	
SMC	
Apple Inc.	
DRAWING NUMBER	M122 D
REVISION	A.0.0
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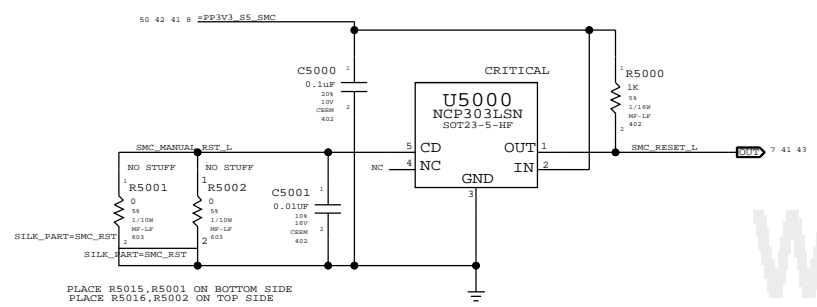
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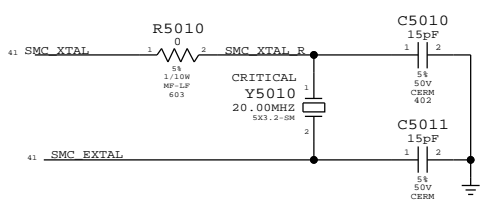
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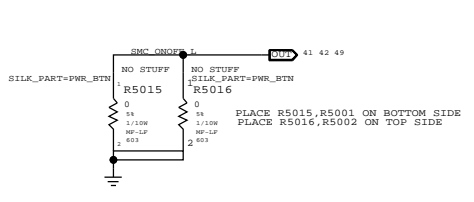
SMC Reset "Button" / Brownout Detect



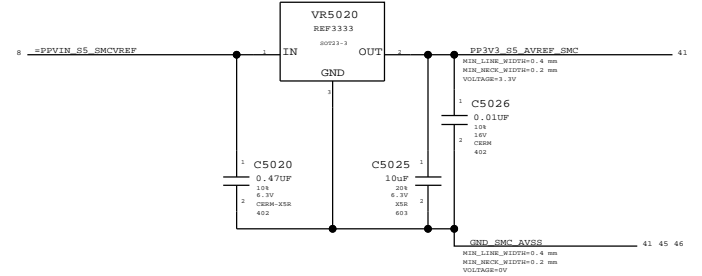
SMC Crystal Circuit



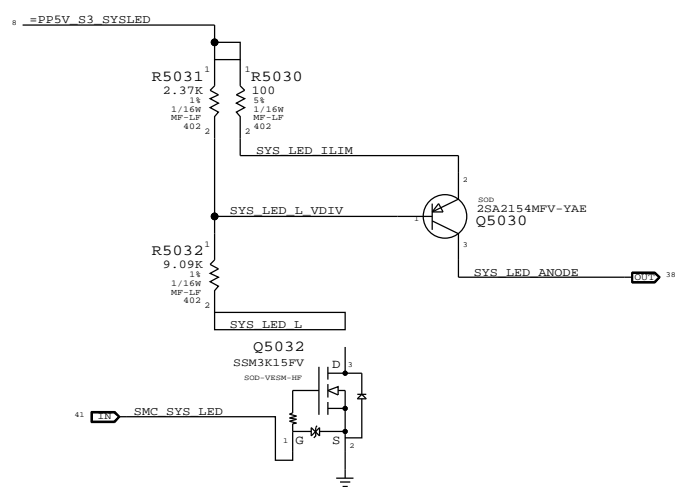
Debug Power "Button"



SMC AVREF Supply

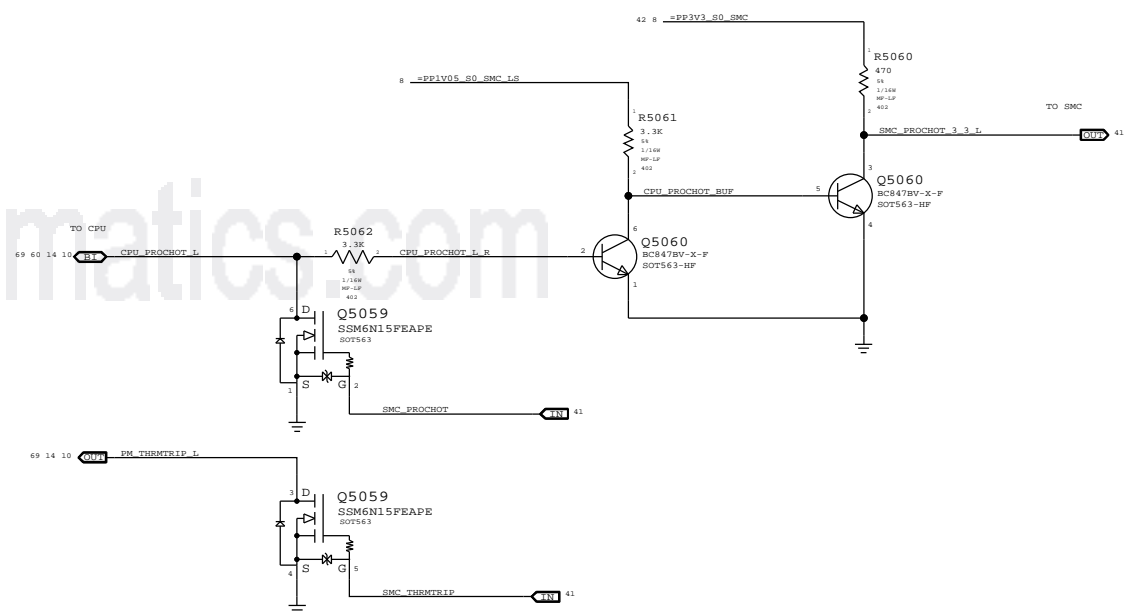


System (Sleep) LED Circuit



41	SMC_FAN_1_CTL	==	NC_SMC_FAN_1_CTL	
41	SMC_FAN_1_TACH	==	MAKE_BASE+TRUE	NO_TEST+TRUE
41	SMC_FAN_2_CTL	==	NC_SMC_FAN_2_CTL	
41	SMC_FAN_2_TACH	==	MAKE_BASE+TRUE	NO_TEST+TRUE
41	SMC_FAN_3_CTL	==	NC_SMC_FAN_3_CTL	
41	SMC_FAN_3_TACH	==	MAKE_BASE+TRUE	NO_TEST+TRUE
41	SMC_GFX_OVERTEMP_I	==	TP_SMC_GFX_OVERTEMP_I	
41	SMC_GFX_THROTTLE_L	==	SMC_IQ_THROTTLE_L	21
57	SMC_BC_ACOK	==	NC_SMC_BC_ACOK	
41	ALS_GAIN	==	NC_ALS_GAIN	
41	SMC_PB3	==	NC_SMC_PB3	
41	SMC_P24	==	MAKE_BASE+TRUE	
41	SMC_P26	==	TP_SMC_P24	46
41	SMC_P41	==	MAKE_BASE+TRUE	
41	SMC_RSTGATE_I	==	TP_SMC_RSTGATE_I	
41	SMC_EXCARD_PWR_EN	==	TP_SMC_EXCARD_PWR_EN	
41	ALS_RIGHT	==	NC_ALS_RIGHT	
41	ESTABLDO_EN	==	MAKE_BASE+TRUE	NO_TEST+TRUE
41	SMC_ANALOG_ID	==	NC_SMC_ANALOG_ID	
41	SMC_SYS_KBLED	==	NC_SMC_SYS_KBLED	
41	SMC_SNS_INT	==	MAKE_BASE+TRUE	NO_TEST+TRUE
45	SMC_MCP_VSENSE	==	SMC_GPD_VSENSE	41
46	SMC_CPU_FSB_ISENSE	==	ALS_LEFT	41

SMC FSB to 3.3V Level Shifting



41	SMC_PA0	==	R5091	100K	5%	1/16W	MP-LP	402
41	SMC_PA1	==	R5092	100K	5%	1/16W	MP-LP	402
49	SMC_ONOFF_I	==	R5070	10K	5%	1/16W	MP-LP	402
56	SMC_FSD	==	R5071	100K	5%	1/16W	MP-LP	402
41	SMC_FME	==	R5072	10K	5%	1/16W	MP-LP	402
43	SMC_TX_L	==	R5073	10K	5%	1/16W	MP-LP	402
43	SMC_RX_L	==	R5074	100K	5%	1/16W	MP-LP	402
56	SMC_ONWIRE	==	R5075	2.0K	5%	1/16W	MP-LP	402
56	SMC_BS_ALERT_L	==	R5076	100K	5%	1/16W	MP-LP	402
43	SMC_TMS	==	R5077	10K	5%	1/16W	MP-LP	402
43	SMC_TDO	==	R5078	10K	5%	1/16W	MP-LP	402
43	SMC_TDI	==	R5079	10K	5%	1/16W	MP-LP	402
43	SMC_TCK	==	R5080	10K	5%	1/16W	MP-LP	402
41	SMC_BIL_BUTTON_L	==	R5081	10K	5%	1/16W	MP-LP	402
57	SMC_BC_ACOK	==	R5087	470K	5%	1/16W	MP-LP	402

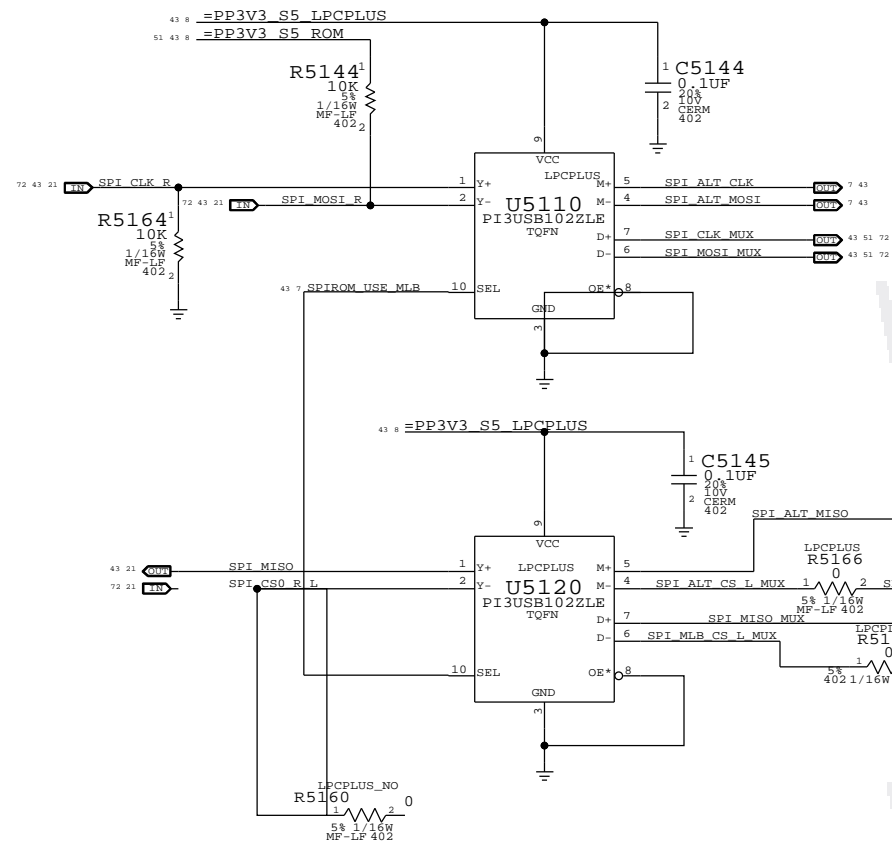
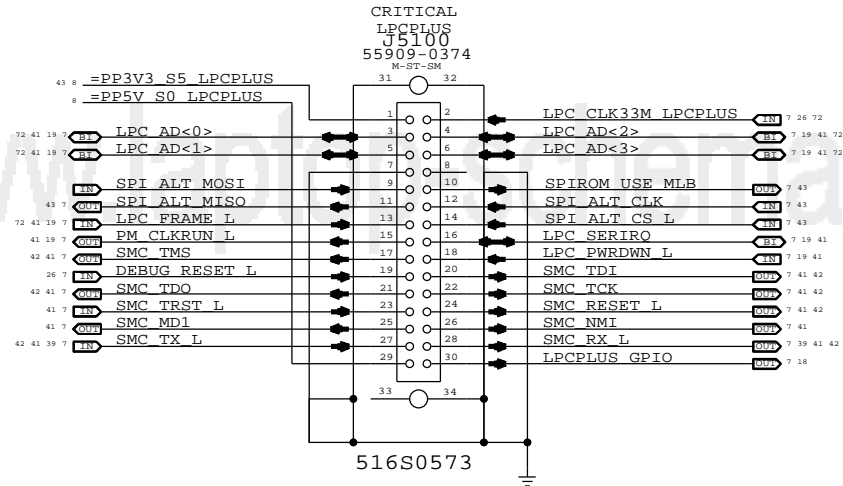
41	SMC_NB_MISC_ISENSE	==	R5055	10K	5%	1/16W	MP-LP	402
41	SMC_GPU_ISENSE	==	R5054	10K	5%	1/16W	MP-LP	402
41	SMC_ADAPTER_EN	==	R5085	10K	5%	1/16W	MP-LP	402
41	SMC_CASE_OPEN	==	R5086	10K	5%	1/16W	MP-LP	402
41	SMC_EXCARD_CP	==	R5088	10K	5%	1/16W	MP-LP	402
41	PM_BLD_R4_L	==	R5090	22K	5%	1/16W	MP-LP	402
44	PM_BLD_R4_L	==	R5090	22K	5%	1/16W	MP-LP	402
41	SMC_PA5	==	R5089	10K	5%	1/16W	MP-LP	402

ADD NC ALIASES FOR FAN1 SIGNALS

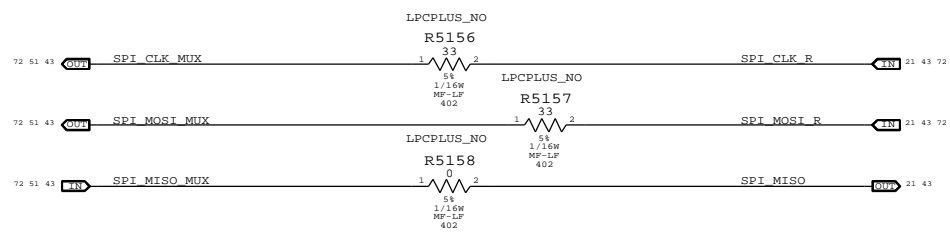
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SMC Support	
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PAGE	50 OF 109
SHEET	

LPC+SPI Connector

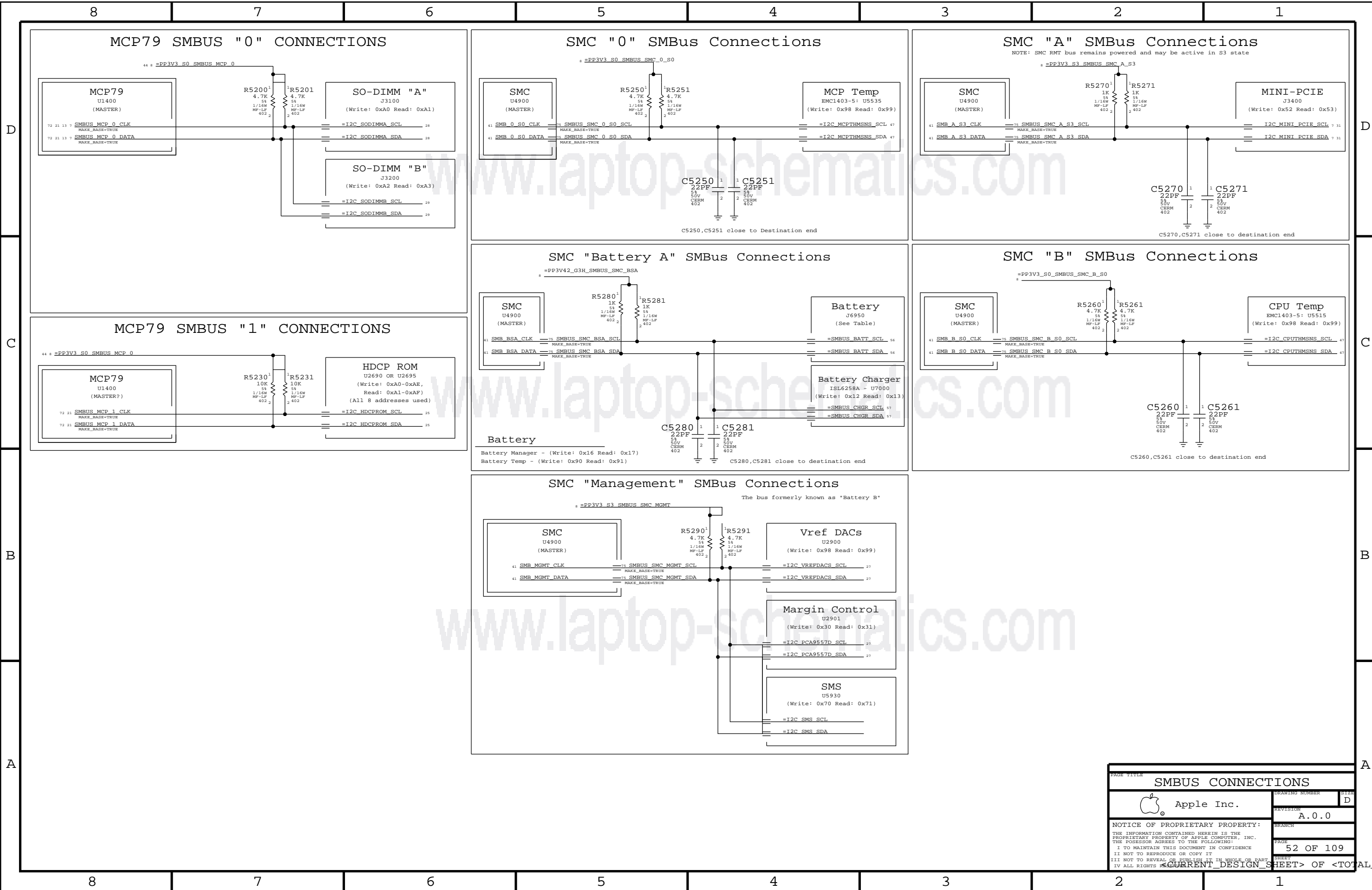
Alternate SPI ROM Support



SPI Bus Series Resistance Option

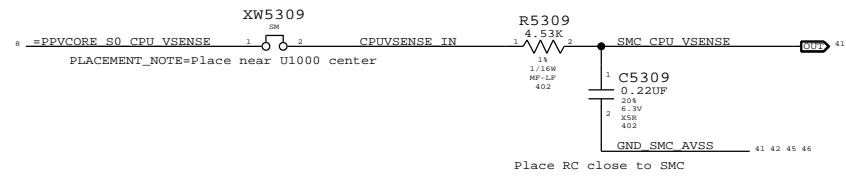


PAGE TITLE LPC+SPI Debug Connector		DRAWING NUMBER M122
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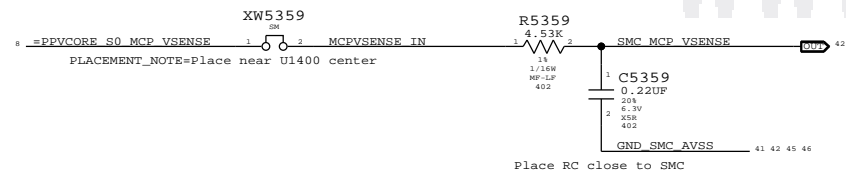


PAGE TITLE		SMBUS CONNECTIONS	
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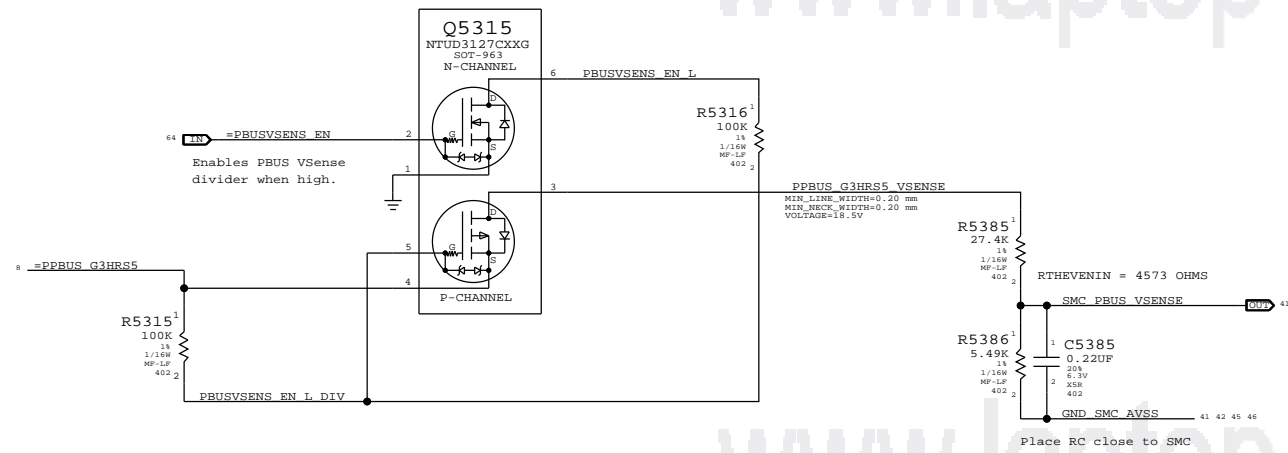
CPU Voltage Sense / Filter



MCP Voltage Sense / Filter



PBUS VOLTAGE SENSE ENABLE & FILTER



PAGE TITLE		SYNC DATE=08/17/2008	
VOLTAGE SENSING		DRAWING NUMBER	SIZE
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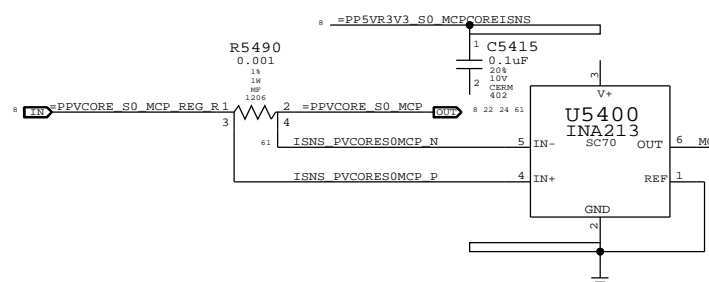
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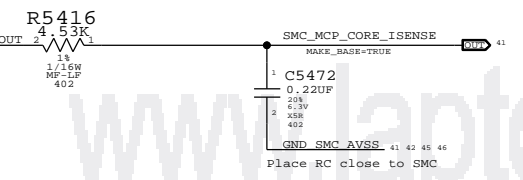
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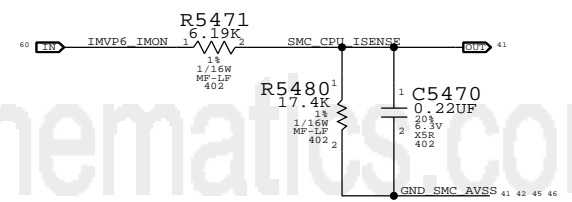
MCP VCore Current Sense



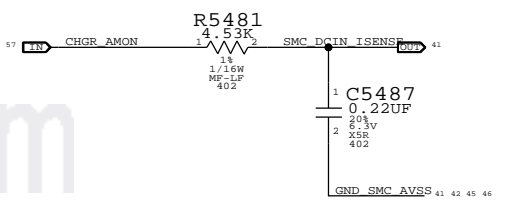
MCP VCore Current Sense Filter



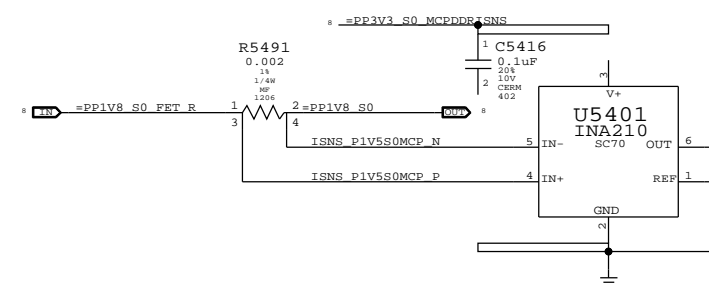
CPU VCore Load Side Current Sensor / Filter



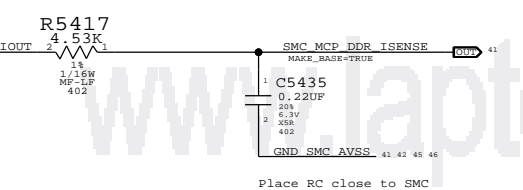
DC-IN (AMON) CURRENT SENSE



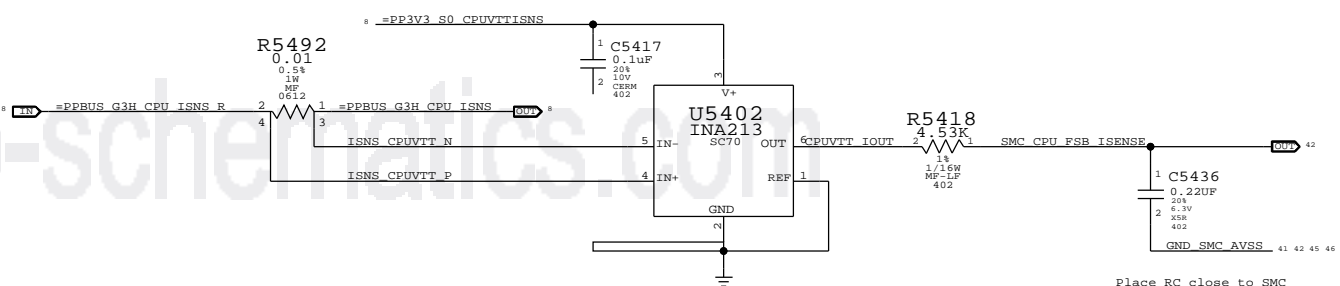
MCP MEM VDD Current Sense



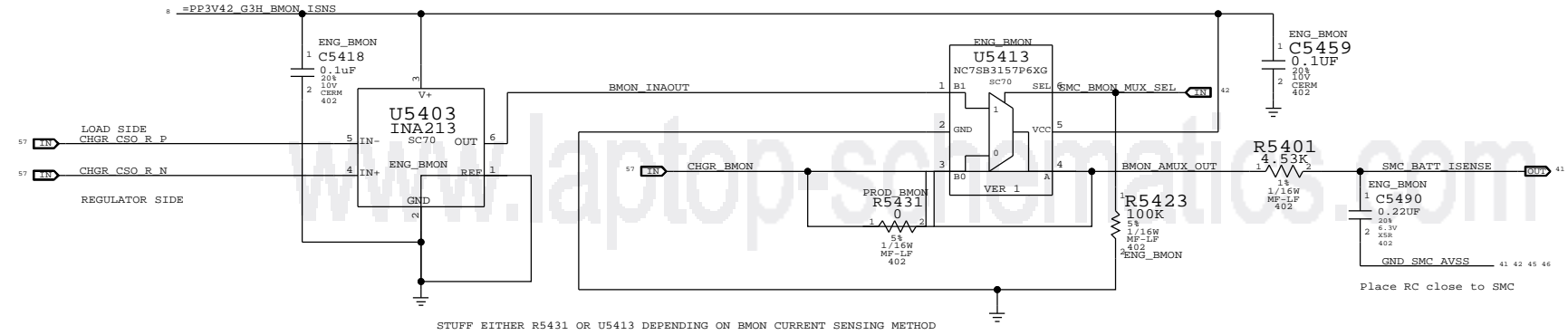
MCP MEM VDD Current Sense Filter



CPU 1.05V CURRENT SENSE



CHARGER BMON CURRENT SENSE



STUFF EITHER R5431 OR U5413 DEPENDING ON BMON CURRENT SENSING METHOD

PAGE TITLE		Current Sensing	
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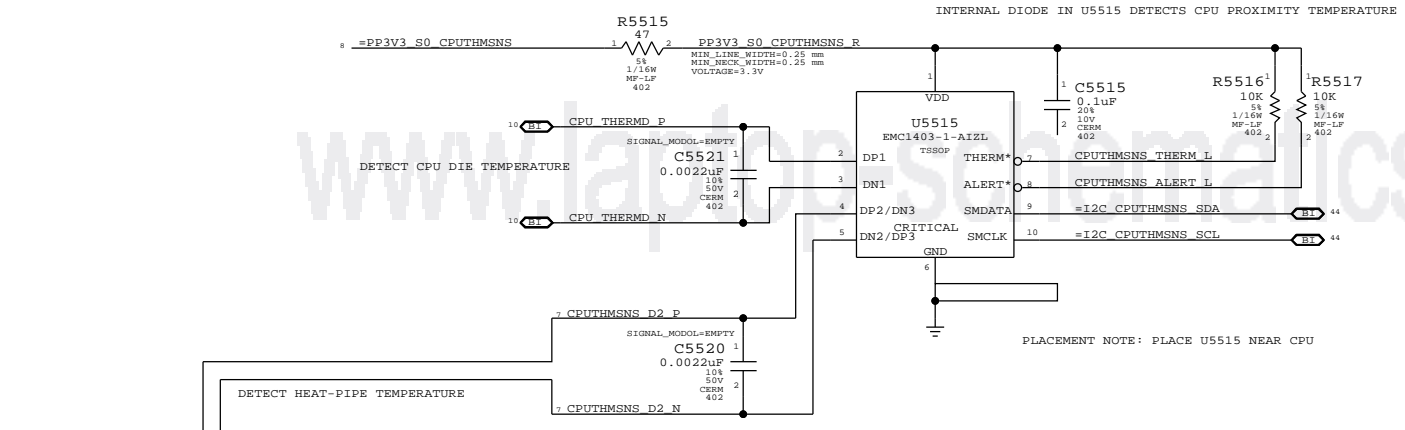
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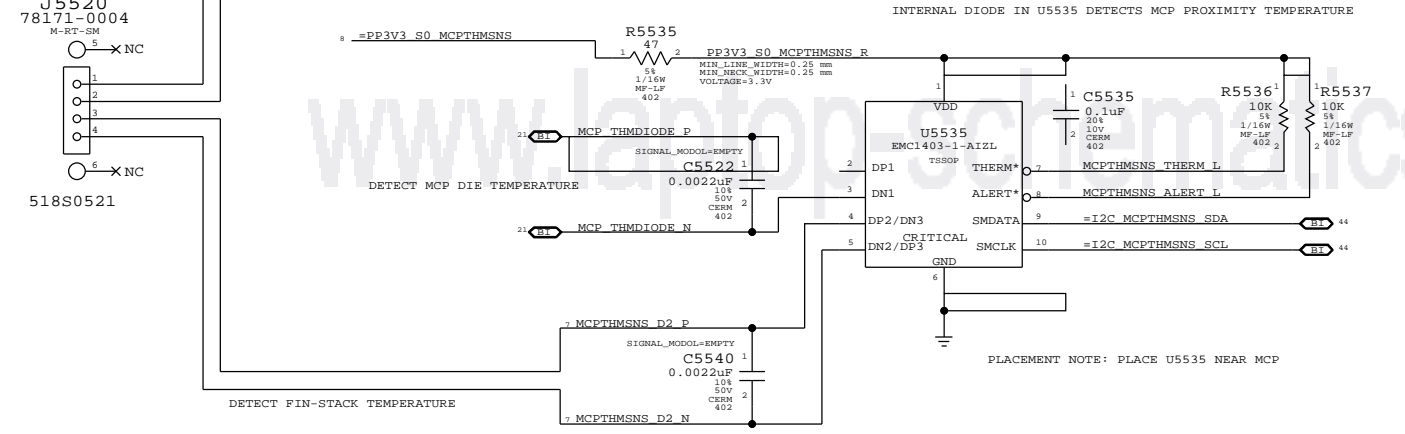
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CPU T-Diode Thermal Sensor



MCP T-Diode Thermal Sensor

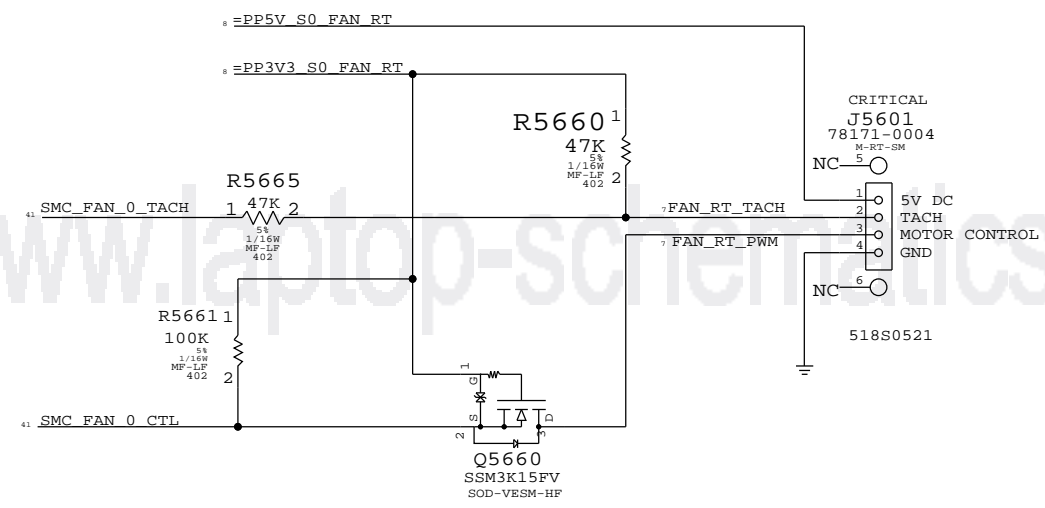


PAGE TITLE		Thermal Sensors	
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		PAGE	55 OF 109
		SHEET	<CURRENT DESIGN SHEET> OF <TOTAL DESIGN SHEETS>

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PAGE TITLE		Fan	
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PAGE		56 OF 109	
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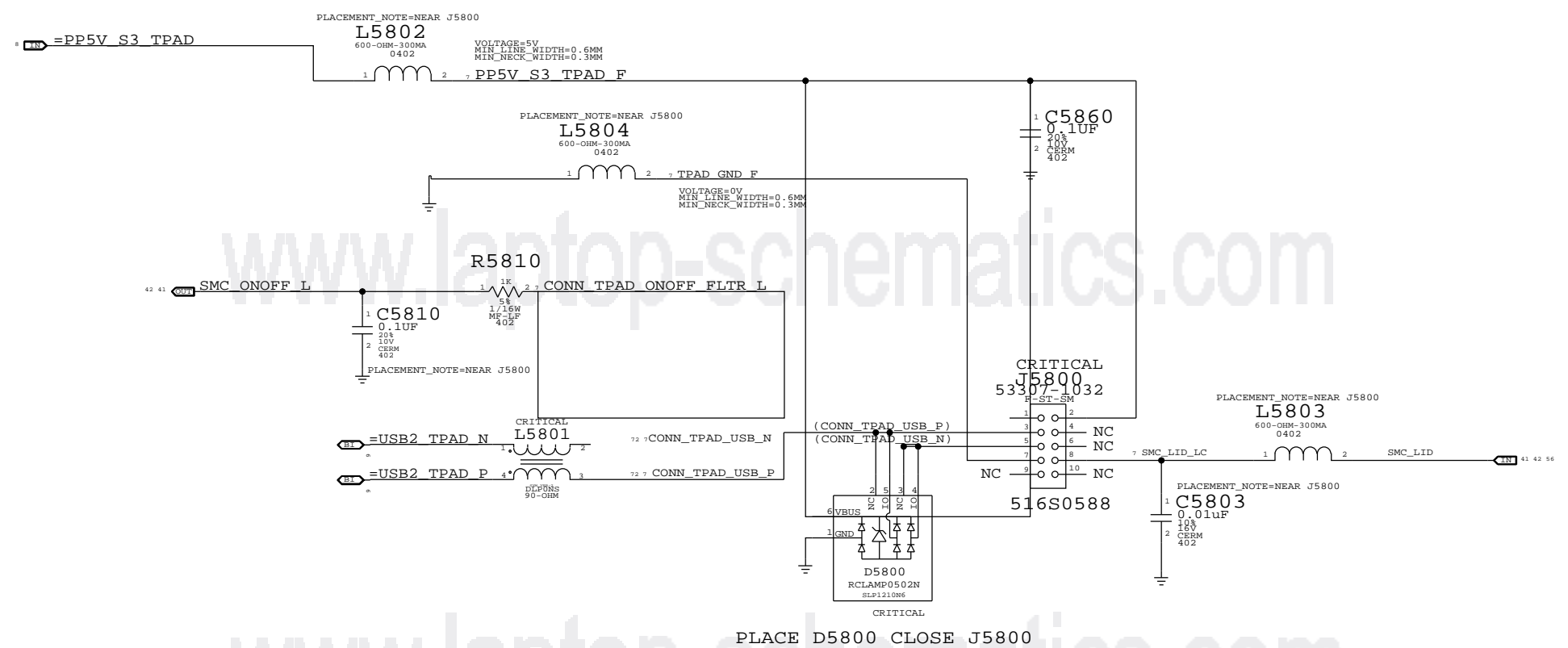
<CURRENT DESIGN SHEET> OF <TOTAL DESIGN SHEETS>

- SYNC WITH T18
 - COPY THIS PAGE FROM T18 CSA.58

PLACEMENT NOTE

PLACE L5800,L5801,L5803 NEAR J5800
 PLACE C5800,C5810,C5803 NEAR J5800
 PLACE D5800 NEAR J5800

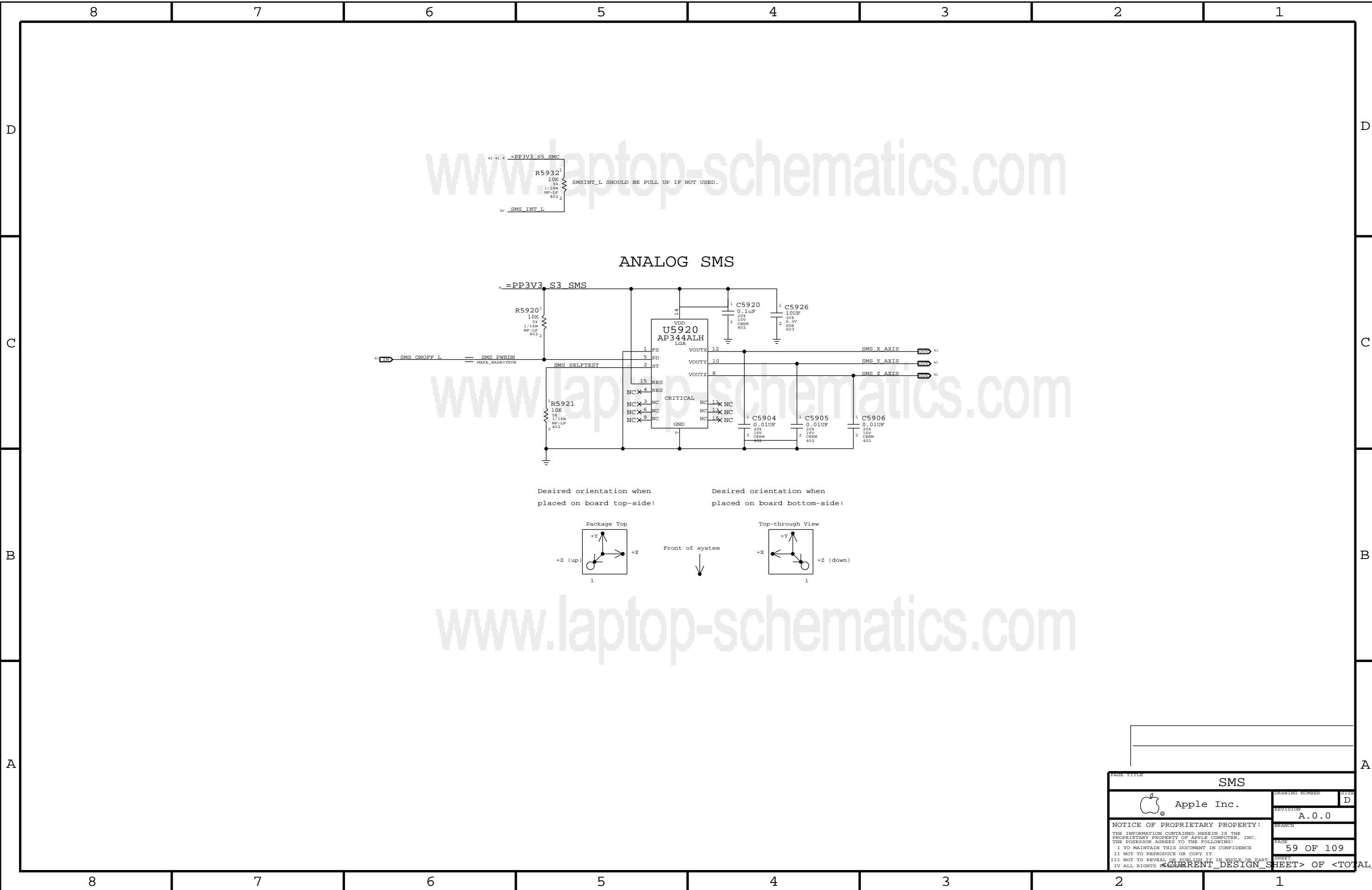
www.laptop-schematics.com
GEYSER



PLACE D5800 CLOSE J5800

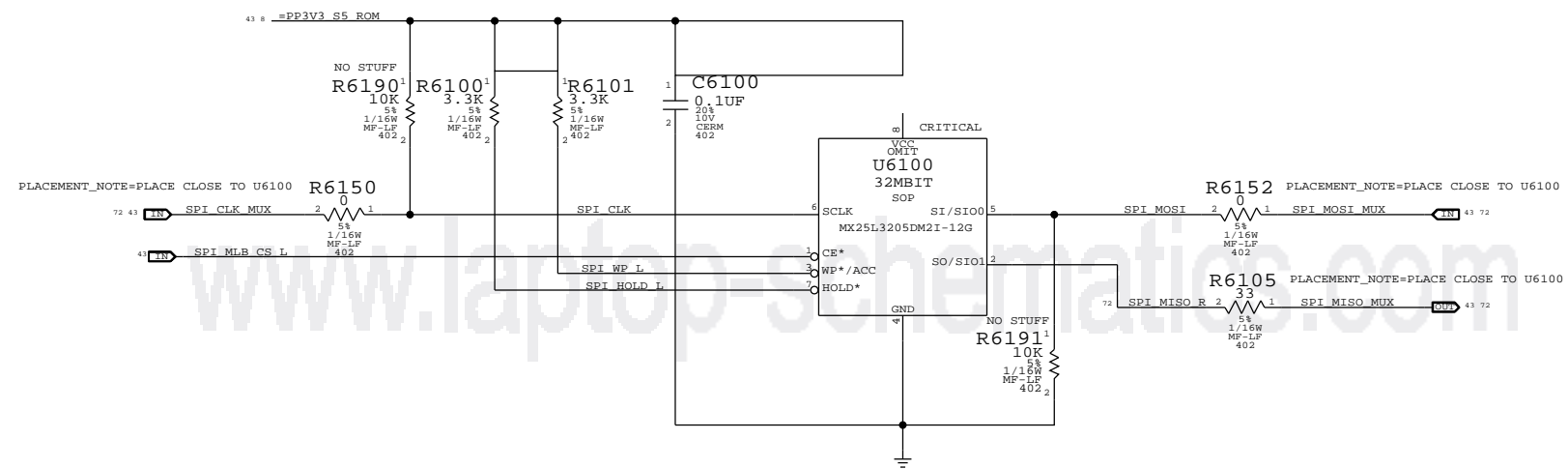
PAGE TITLE		SYNC DATE=08/17/2008	
GEYSER		DRAWING NUMBER	M128
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Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHZ IS SELECTED WITH R5164 AND R5144
 ANY FO THE 4 FREQUENCIES CAN BE SELECTED
 WITH R6190, R6191, R5164 AND R5144

SYNC DATE=081/17/2008

SPI ROM

Apple Inc.

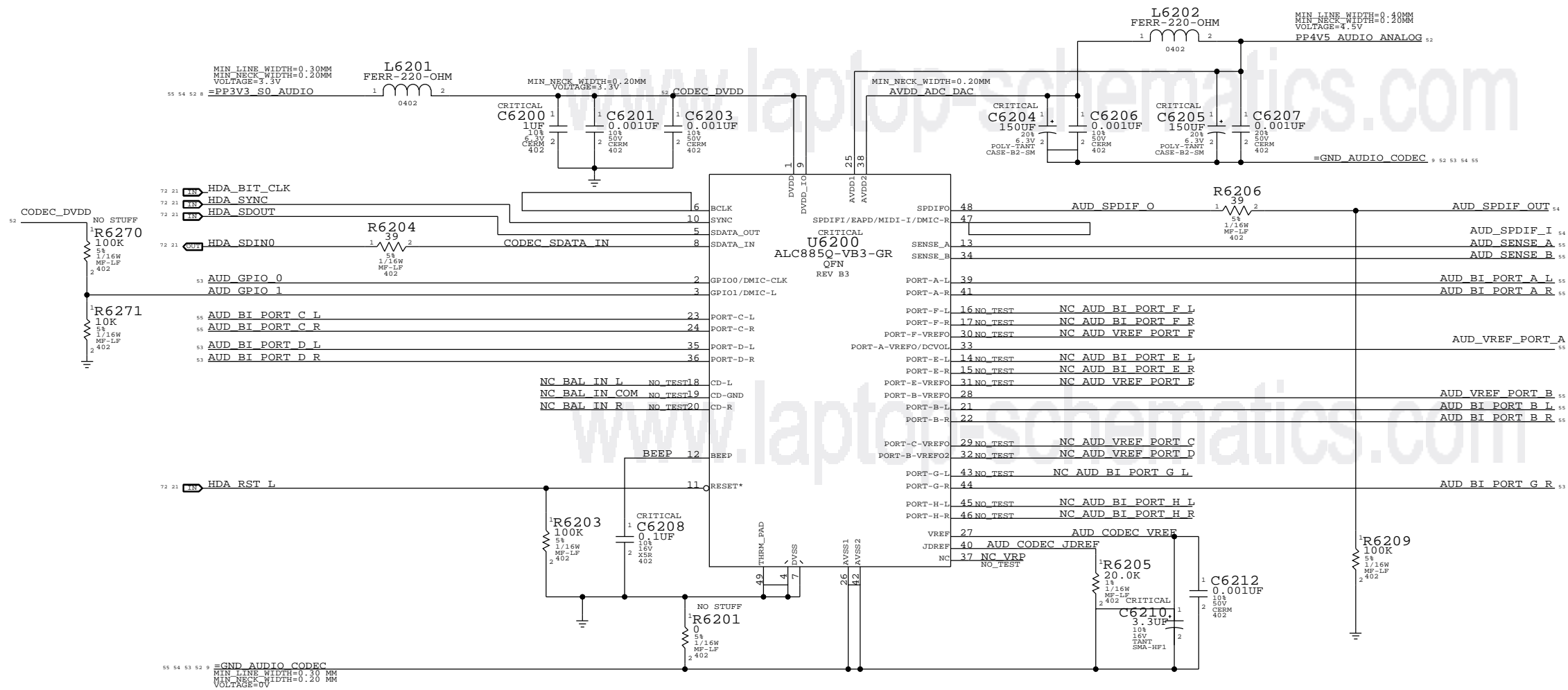
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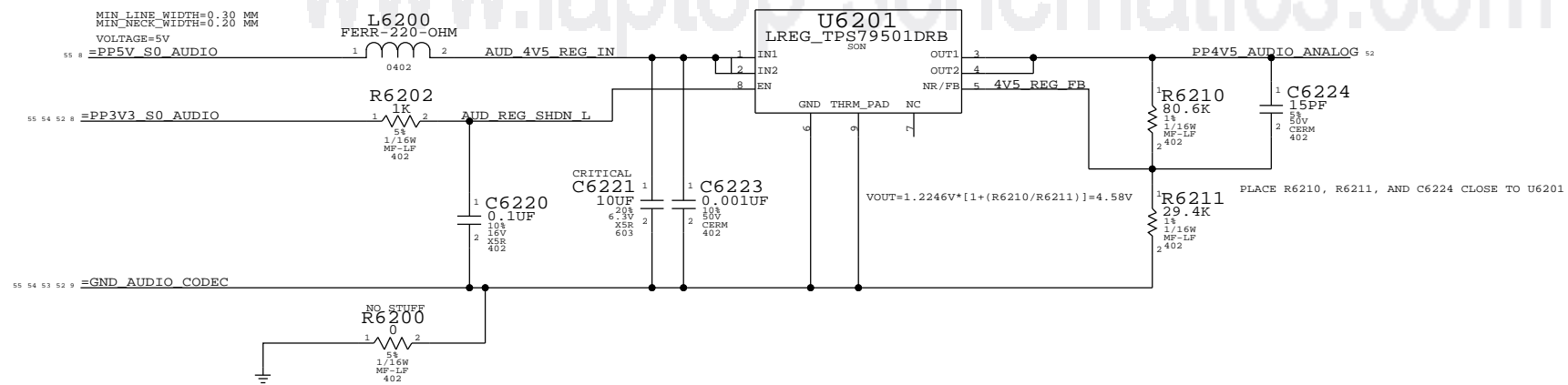
61 OF 109 SHEETS

<CURRENT DESIGN SHEET> OF <TOTAL DESIGN SHEETS>

AUDIO CODEC
APPLE P/N 353S1538



AUDIO 4.5V REGULATOR
APPLE P/N 353S1576



SYNC DATE=08/29/2008

AUDIO: CODEC

Apple Inc.

REVISION: A.0.0

PAGE: 62 OF 109

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CREATING NUMBER: D
SHEET: 62 OF 109
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SATELLITE & SUB TWEETER AMPLIFIER APN:353S1595

SATELLITE 169 HZ < FC < 282 HZ
 SUB 80 HZ < FC < 132 HZ
 GAIN 12DB

VOLTAGE=5V
 MIN_LINE_WIDTH=0.60 MM
 MIN_NECK_WIDTH=0.20 MM
 PP5V_S0_AUDIO_AMP

VOLTAGE=5V
 MIN_LINE_WIDTH=0.30 MM
 MIN_NECK_WIDTH=0.20 MM

MIN_LINE_WIDTH=0.30 mm
 MIN_NECK_WIDTH=0.20 mm
 SPKRAMP R P OUT

MIN_LINE_WIDTH=0.30 mm
 MIN_NECK_WIDTH=0.20 mm
 SPKRAMP R N OUT

RIGHT SATELLITE

MIN_LINE_WIDTH=0.30 mm
 MIN_NECK_WIDTH=0.20 mm
 SPKRAMP L P OUT

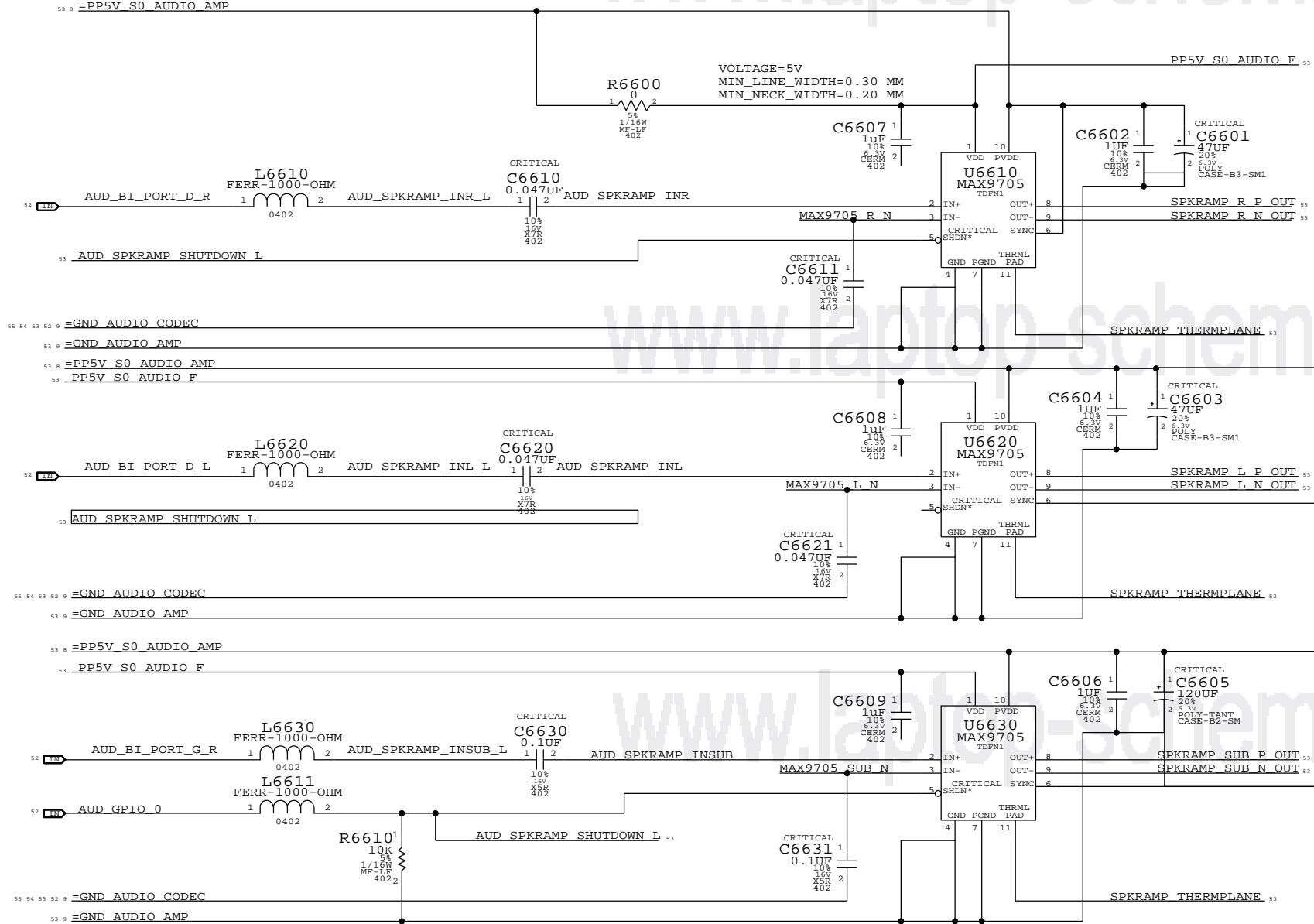
MIN_LINE_WIDTH=0.30 mm
 MIN_NECK_WIDTH=0.20 mm
 SPKRAMP L N OUT

LEFT SATELLITE

MIN_LINE_WIDTH=0.30 mm
 MIN_NECK_WIDTH=0.20 mm
 SPKRAMP SUB P OUT

MIN_LINE_WIDTH=0.30 mm
 MIN_NECK_WIDTH=0.20 mm
 SPKRAMP SUB N OUT

SUB-TWEETER



MIN_LINE_WIDTH=0.60 MM
 MIN_NECK_WIDTH=0.20 MM
 PP5V_S0_AUDIO_AMP
 SPKRAMP_THERMPLANE

SYNC DATE=08/29/2008

PAGE TITLE		AUDIO: SPEAKER AMP	
Apple Inc.		CREATING NUMBER	1122
		REVISION	A.0.0
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AUDIO JACK 1: LO/HP CONNECTOR, SPDIF TX

MIC CONNECTOR
APN:518S0392

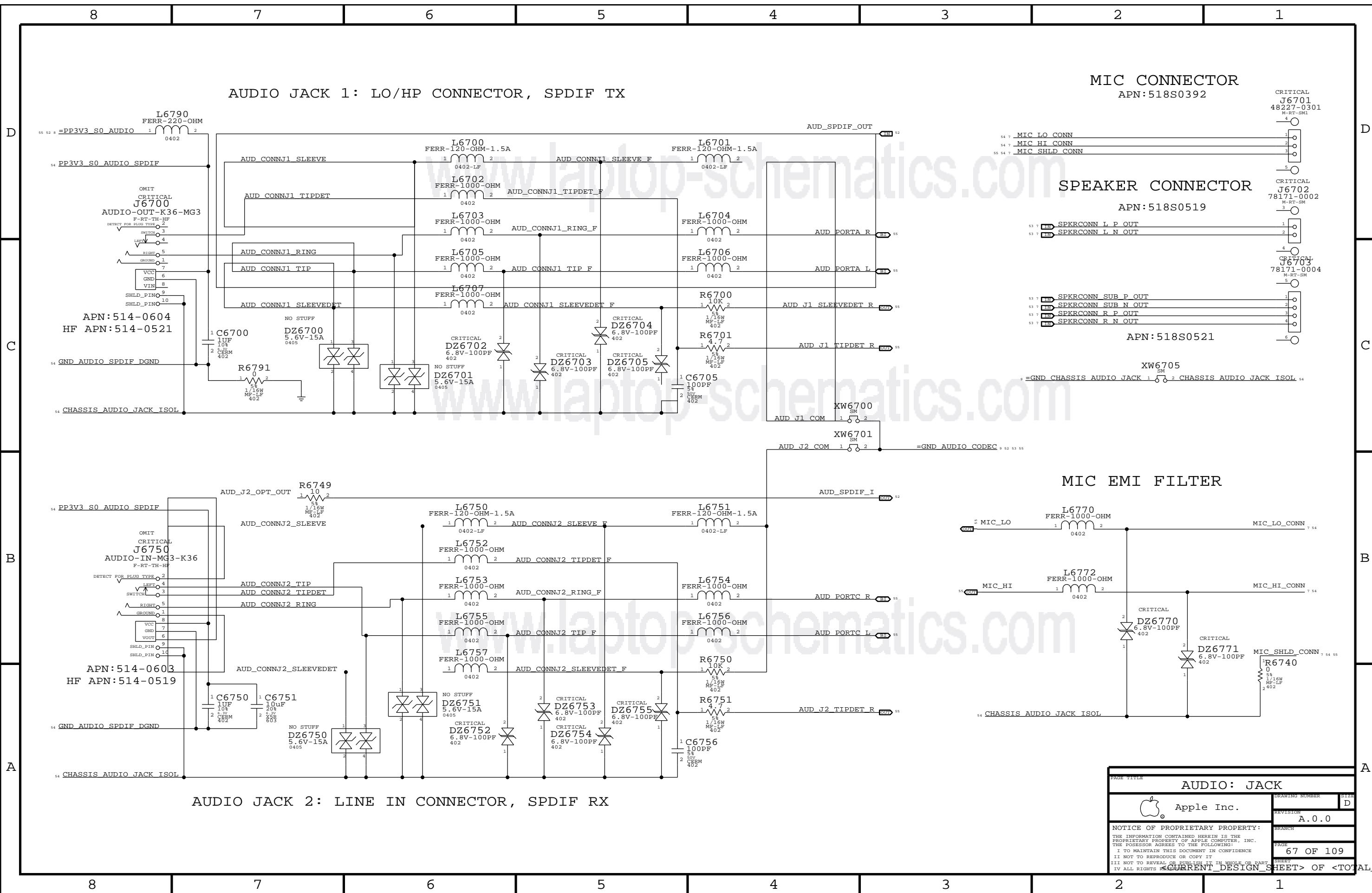
SPEAKER CONNECTOR
APN:518S0519

APN:518S0521

MIC EMI FILTER

AUDIO JACK 2: LINE IN CONNECTOR, SPDIF RX

PAGE TITLE		AUDIO: JACK	
DRAWING NUMBER		D	
REVISION		A.0.0	
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PAGE		67 OF 109	
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8

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1

CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP OUT	0X0F (15)	0X05 (5)	0X15 (21,PORTA)	VREF_A(100%)	0X15 (21,PORTA)
SAT SPKR	0X26 (38)	0X25 (37)	0X14 (20,PORTD)	GPIO 0	N/A
SUB SPKR	0X0E (14)	0X04 (4)	0X16 (22,PORTG)	GPIO 0	N/A
SPDIF OUT	N/A	0X06 (6)	0X1E (30,SPDIF OUT)	N/A	0X1B (27,PORTE)

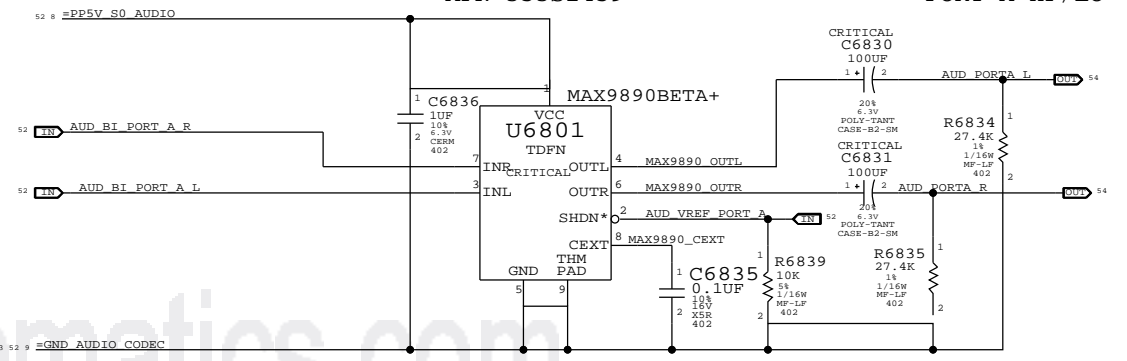
CODEC INPUT SIGNAL PATHS

FUNCTION	MIXER	VOLUME	MUTE CONTROL	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X23 (35)	0X08 (8)	0X08 (8)	0X08 (8)	0X1A (26,PORTC)	N/A	0X1A (26,PORTC)
MIC IN	0X24 (36)	0X07 (7)	0X07 (7)	0X07 (7)	0X18 (24,PORTB)	VREF_B (80%)	N/A
SPDIF IN	N/A	N/A	N/A	0X0A (10)	0X1F (31,SPDIF IN)	N/A	N/A

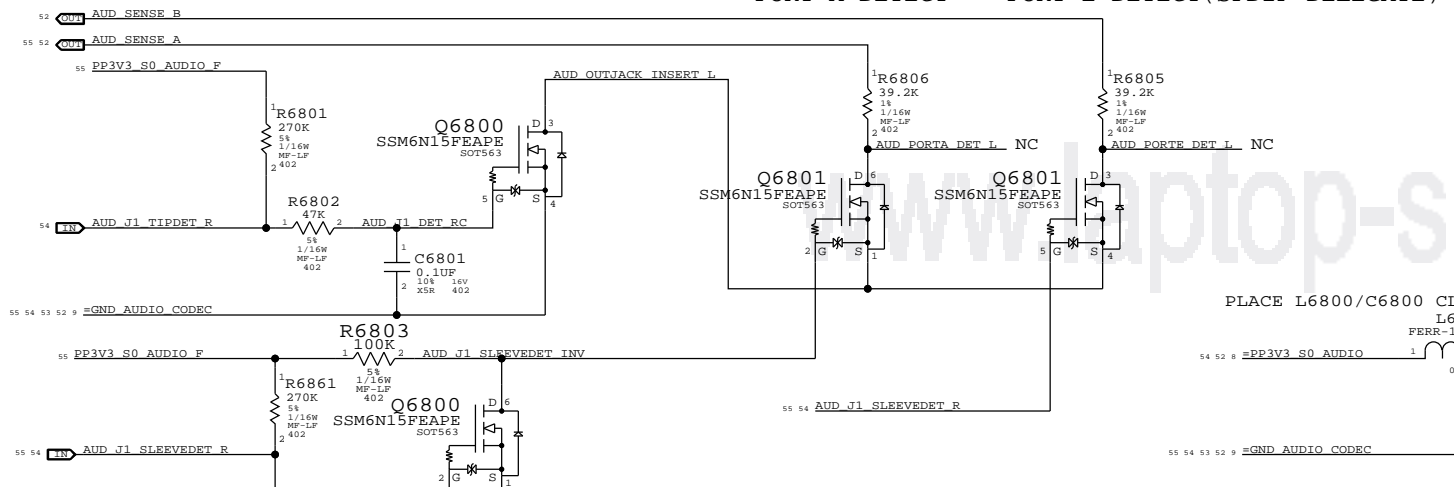
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HP/LO DE-POP SWITCH APN: 353S1459

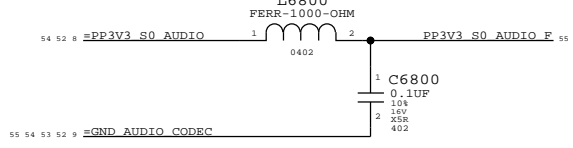
PORT A HP/LO



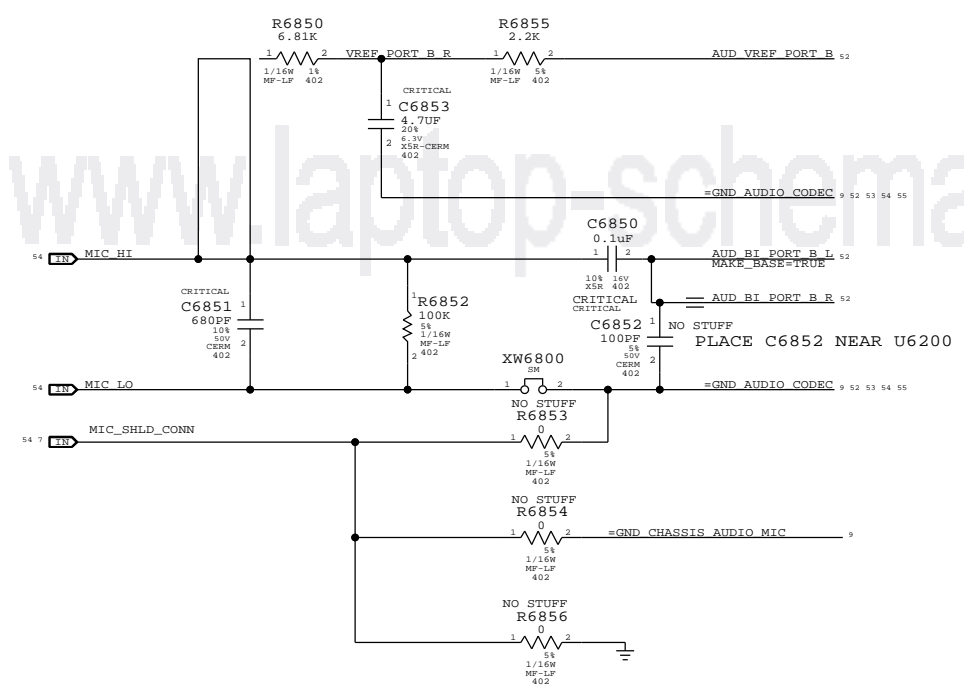
PORT A DETECT PORT E DETECT (SPDIF DELEGATE)



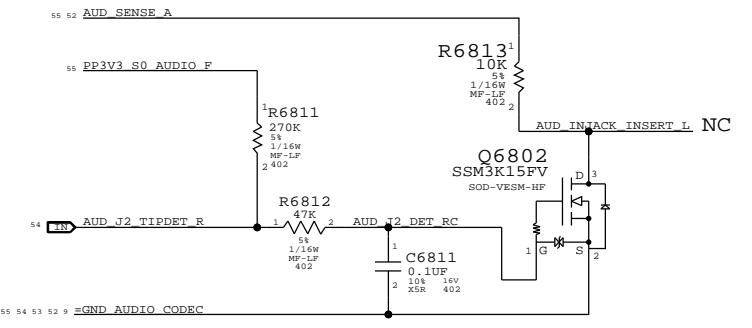
PLACE L6800/C6800 CLOSE TO Q6800



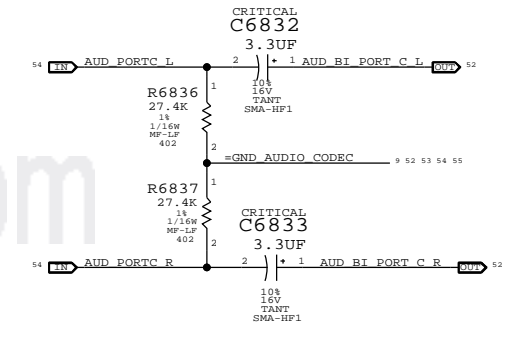
MIC INPUT CIRCUITRY



Line-in (PORT C) DETECT



PORT C LI



SYNC DATE=08/29/2008

AUDIO: JACK TRANSLATORS

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1

- COPY THIS PAGE FROM T18 CSA.69
- DO WE NEED TO CHANGE BATTERY CONNECTOR?

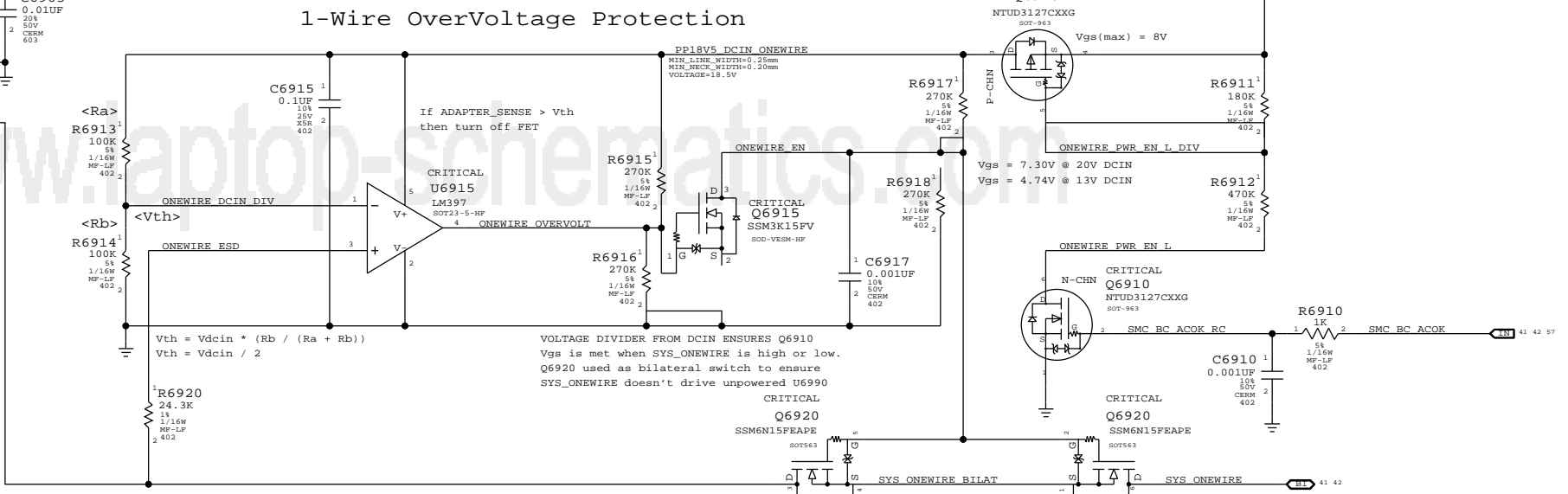
MagSafe DC Power Jack

CRITICAL
J6900
78048-0573
M-RT-SM

518S0656

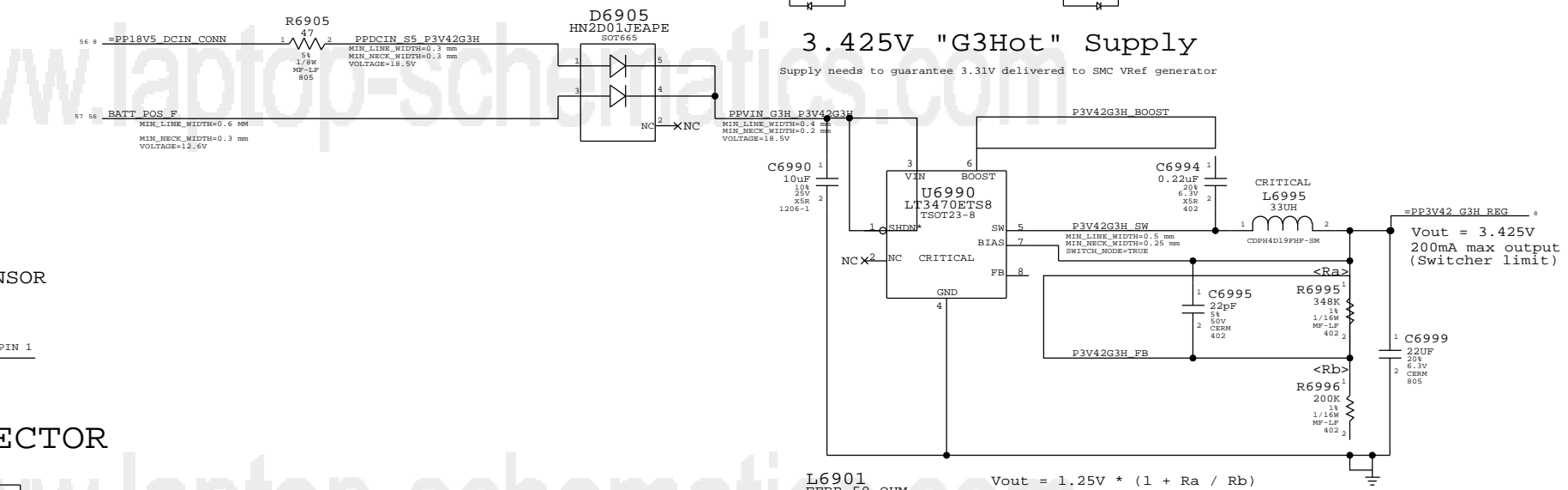
PP18V5 DCIN FUSE
MIN_LINE_WIDTH=1mm
MIN_NECK_WIDTH=0.20mm
VOLTAGE=18.5V

CRITICAL
F6905
6AMP-24V
1206

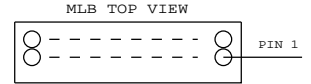


3.425V "G3Hot" Supply

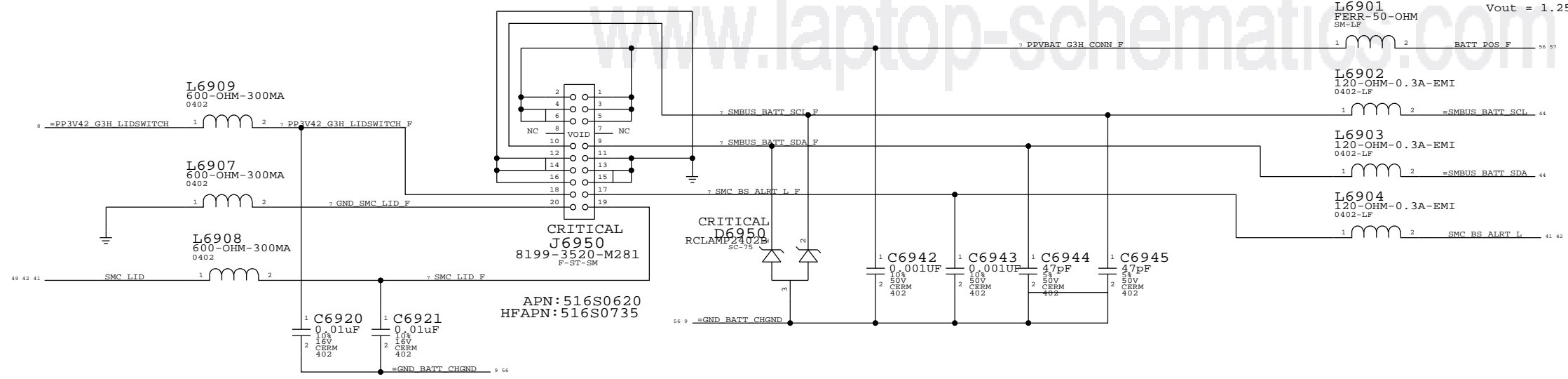
Supply needs to guarantee 3.31V delivered to SMC VRef generator



LID HALL EFFECT SENSOR

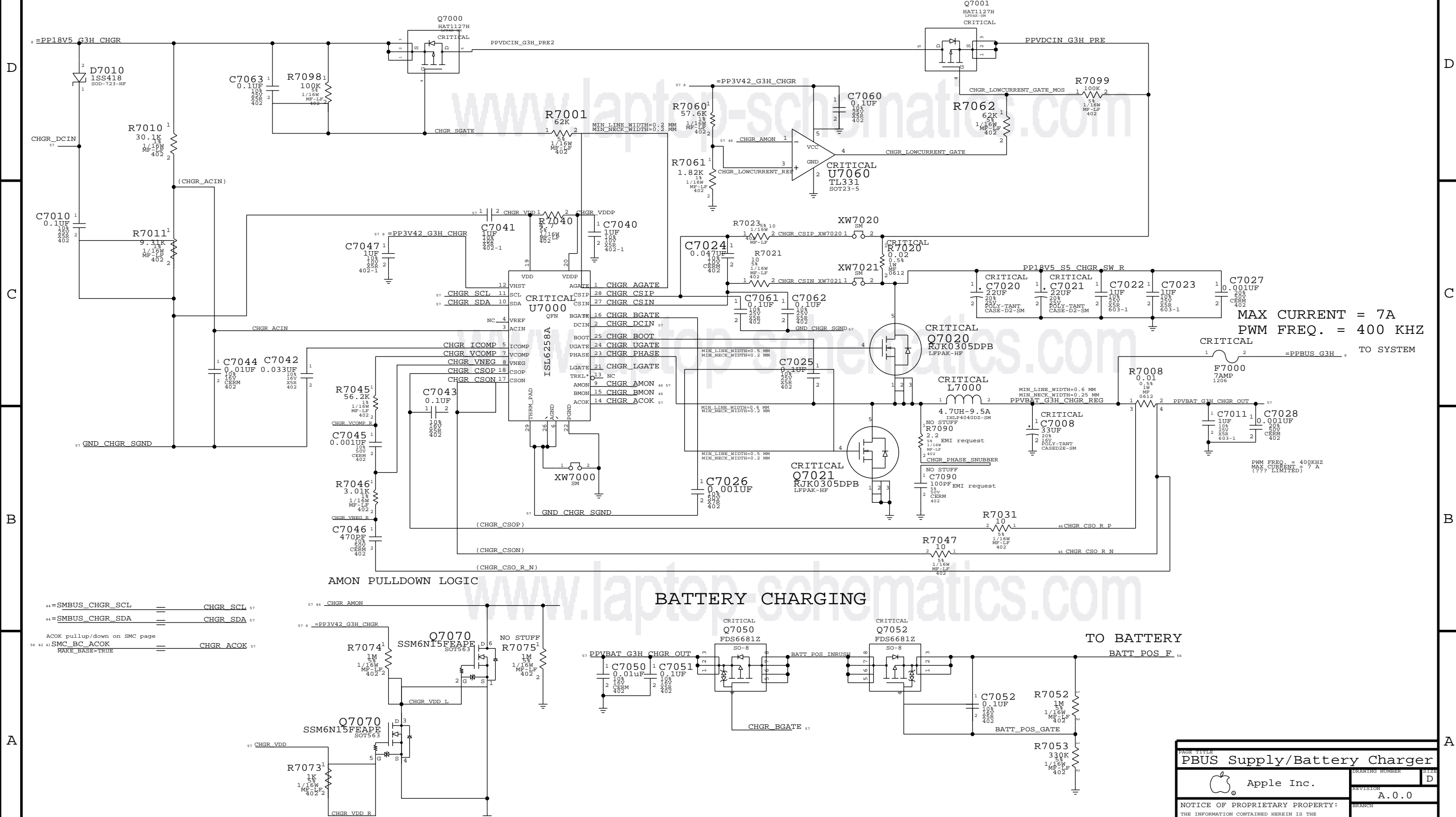


BATTERY/LID CONNECTOR



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DC-In & Battery Connectors		DRAWING NUMBER	M122
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OF TOTAL DESIGN SHEETS		SHEET	

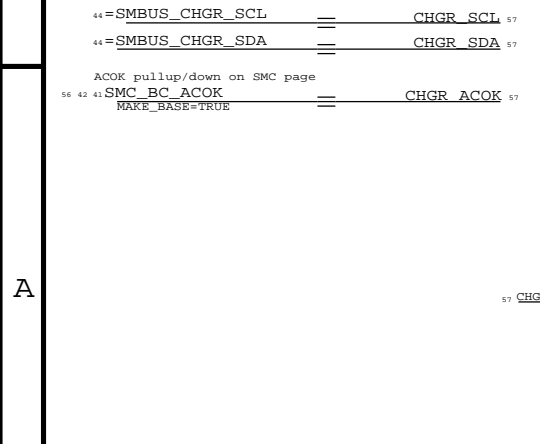
PBUS SUPPLY / BATTERY CHARGER



MAX CURRENT = 7A
PWM FREQ. = 400 KHZ

PWM FREQ. = 400KHZ
MAX CURRENT = 7 A
(???) LIMITED

BATTERY CHARGING

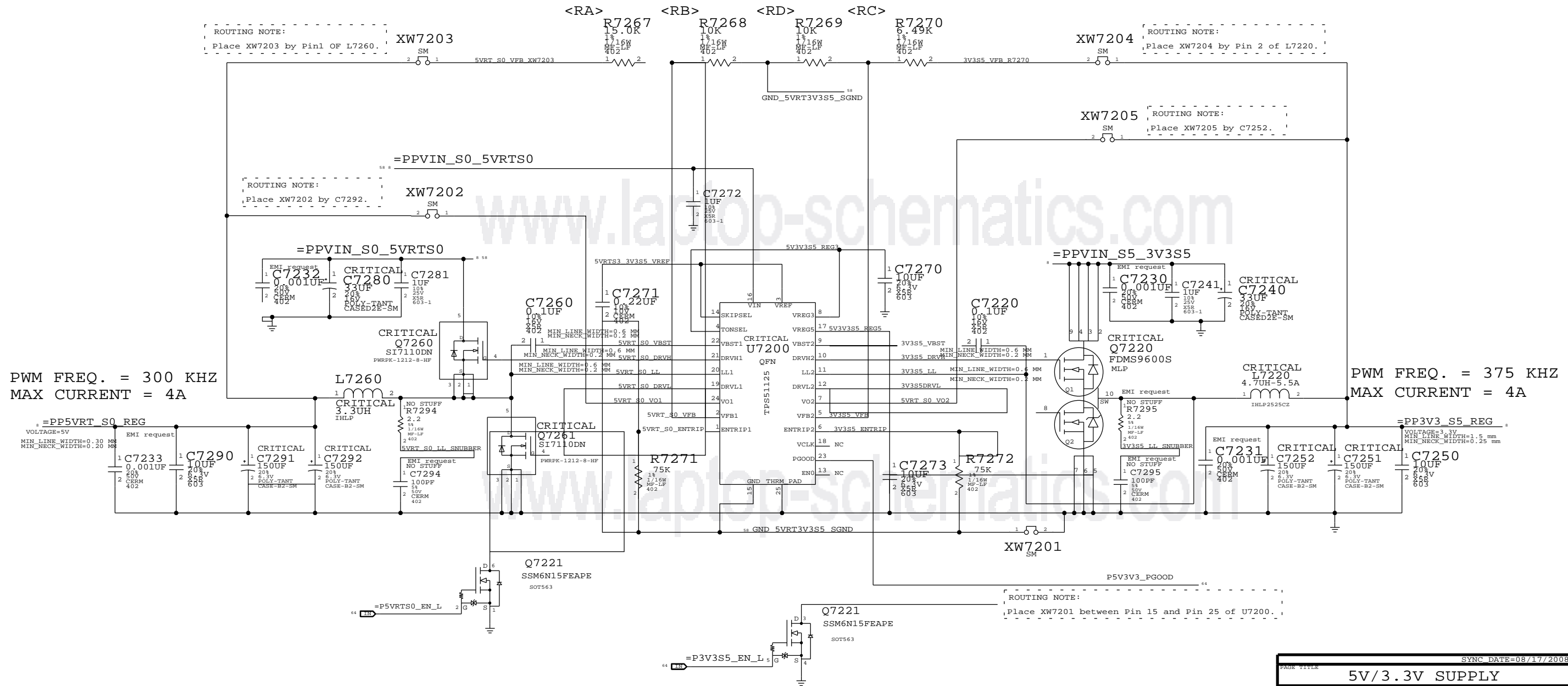


PAGE TITLE	
PBUS Supply/Battery Charger	
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70 OF 109	SHEET
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5V_RT/3.3V POWER SUPPLY

$$V_{OUT} = (2 * R_A / R_B) + 2$$

$$V_{OUT} = (2 * R_C / R_D) + 2$$



PWM FREQ. = 300 KHZ
MAX CURRENT = 4A

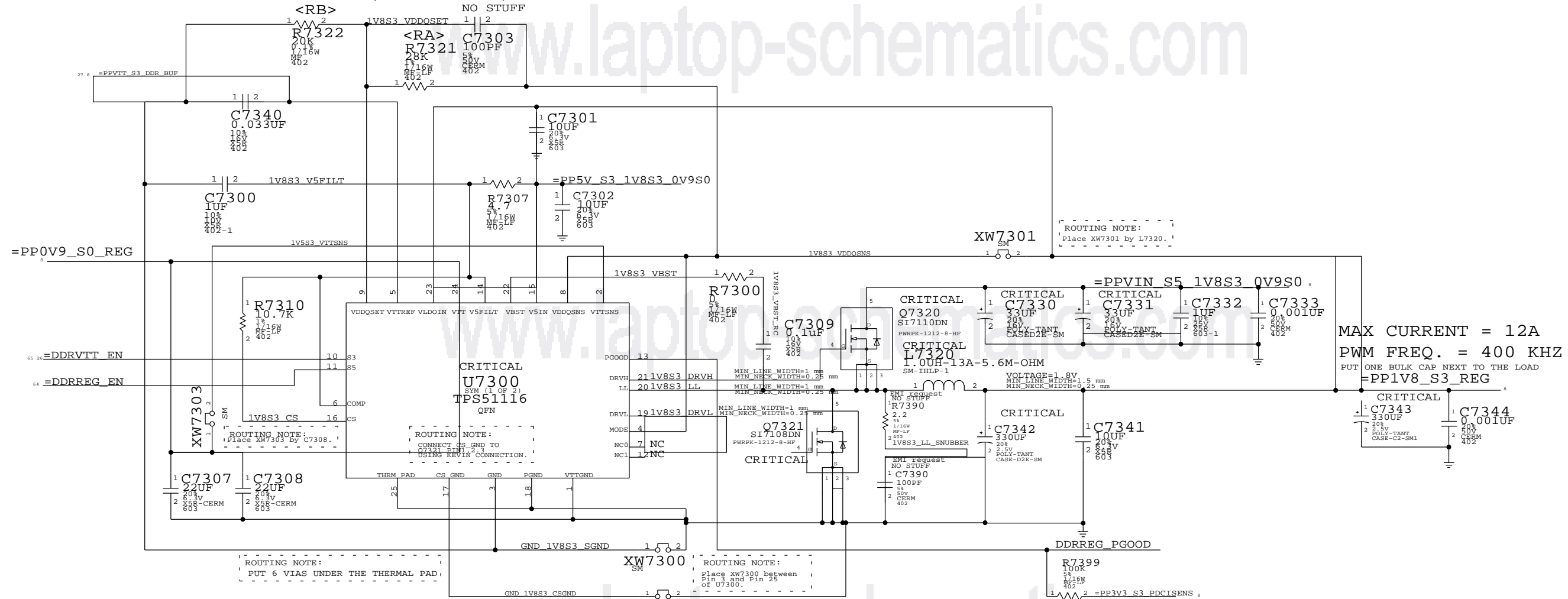
PWM FREQ. = 375 KHZ
MAX CURRENT = 4A

SEPARATED MASTER PGOOD FOR BOTH 5V AND 3V3.

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5V/3.3V SUPPLY		DRAWING NUMBER	M122 D
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			72 OF 109
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1.8V/0.9V (DDR2) POWER SUPPLY

$$V_{OUT} = 0.75V * (1 + R_A / R_B)$$



MAX CURRENT = 12A
 PWM FREQ. = 400 KHZ
 PUT ONE BULK CAP NEXT TO THE LOAD
 =PP1V8_S3_REG

STATE	PM_SLP_S4_L	PM_SLP_S3_L	PP1V8_S3	PP0V9_S0
S0	HIGH	HIGH	1.8V	0.9V
S3	HIGH	LOW	1.8V	0.0V
S5/G3HOT	LOW	LOW	0.0V	0.0V

SYNC DATE=08/17/2008

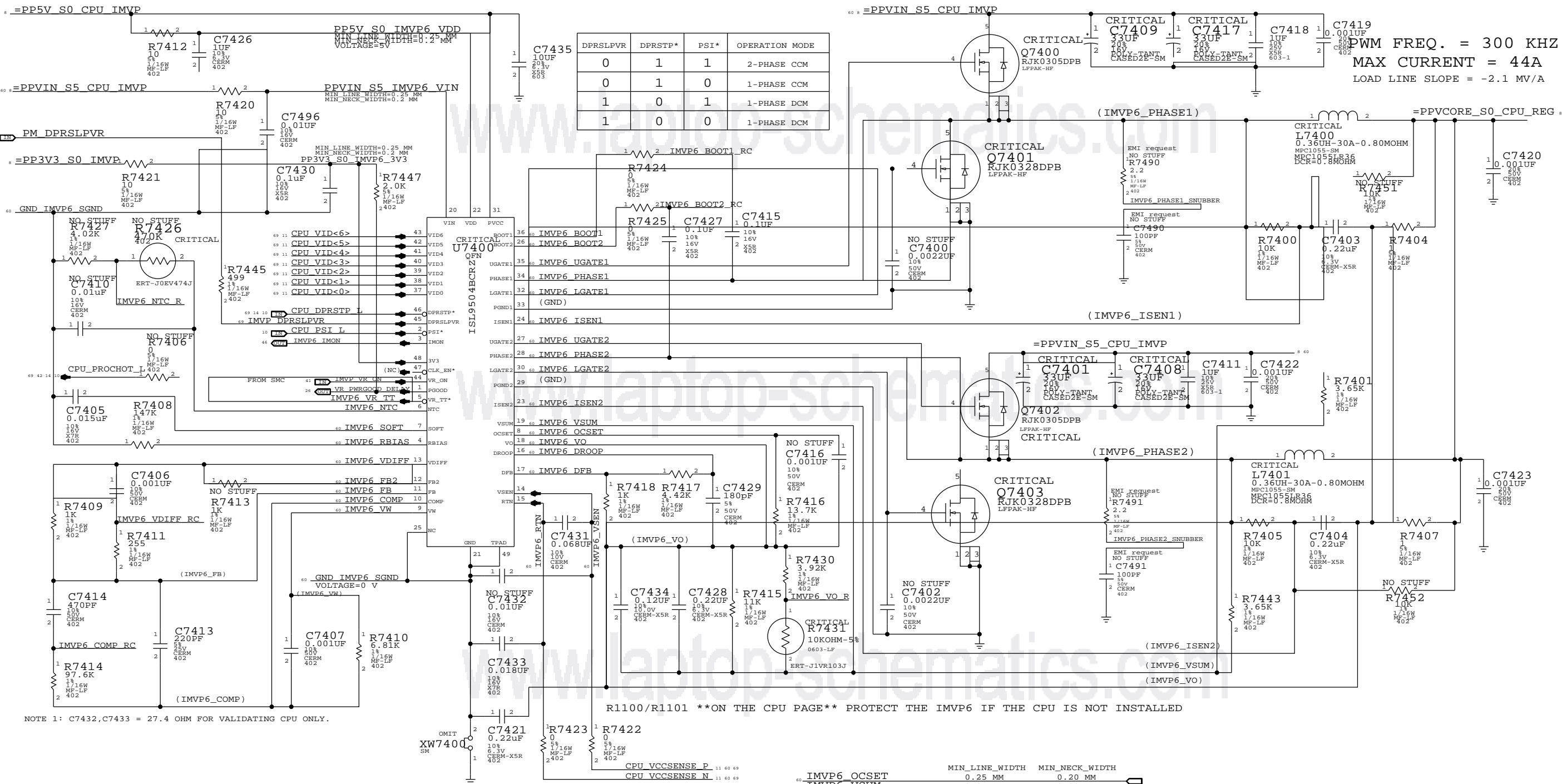
1.8V/0.9V DDR2 SUPPLY

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IMVP6 CPU VCore Regulator

Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM

Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM

Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIA5	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
CPU_VCCSENSE_P	0.25 MM	0.25 MM
CPU_VCCSENSE_N	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

LATEST ISSUE: 2007/01/23

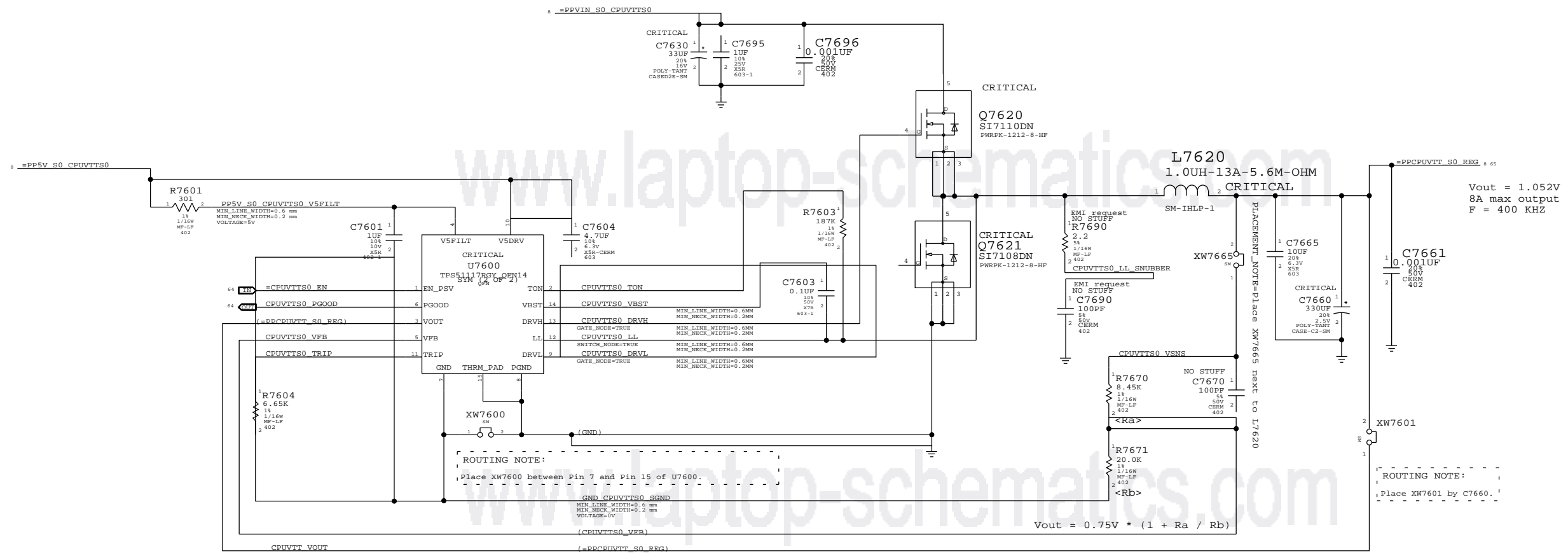
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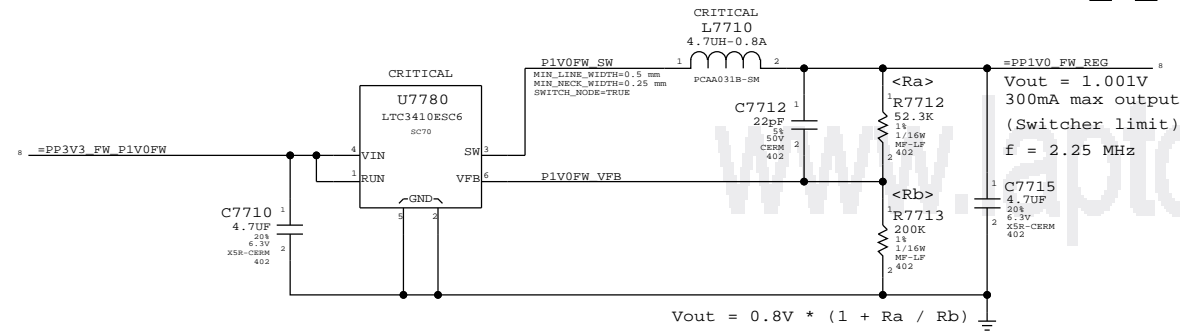
CPUVTT POWER SUPPLY

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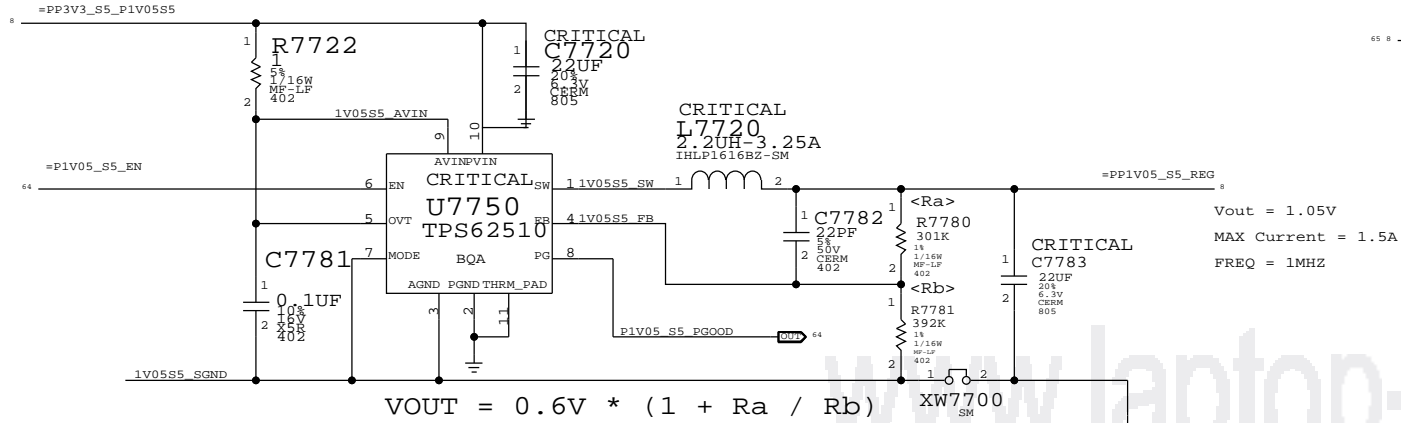


PAGE TITLE		SYNC DATE=08/17/2008	
CPU VTT(1.05V) SUPPLY		CREATING NUMBER	1122
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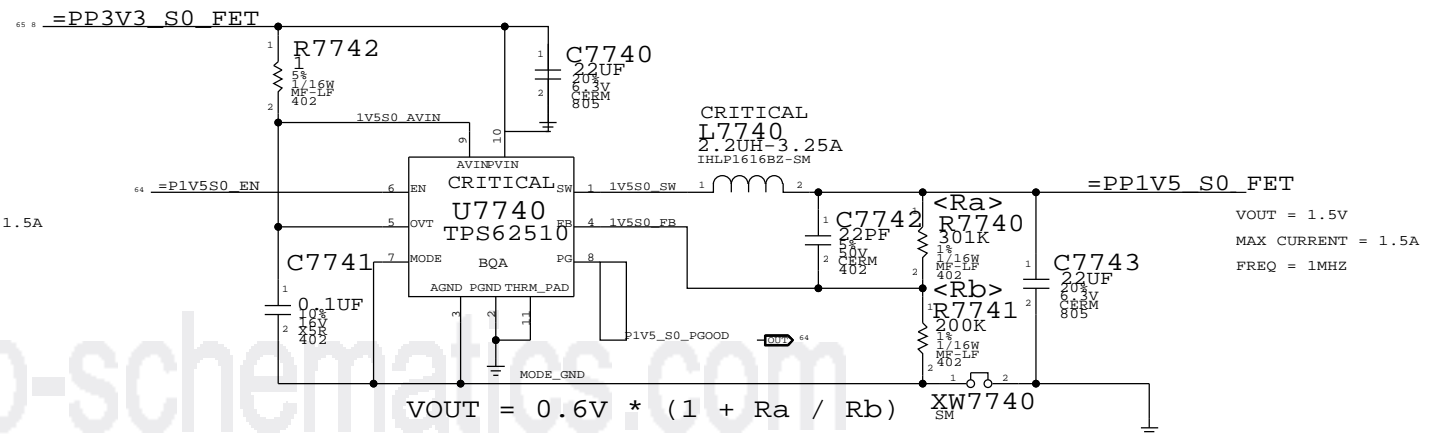
FireWire 1.0V (Core) Supply



MCP 1.05V_S5 AUXC SUPPLY



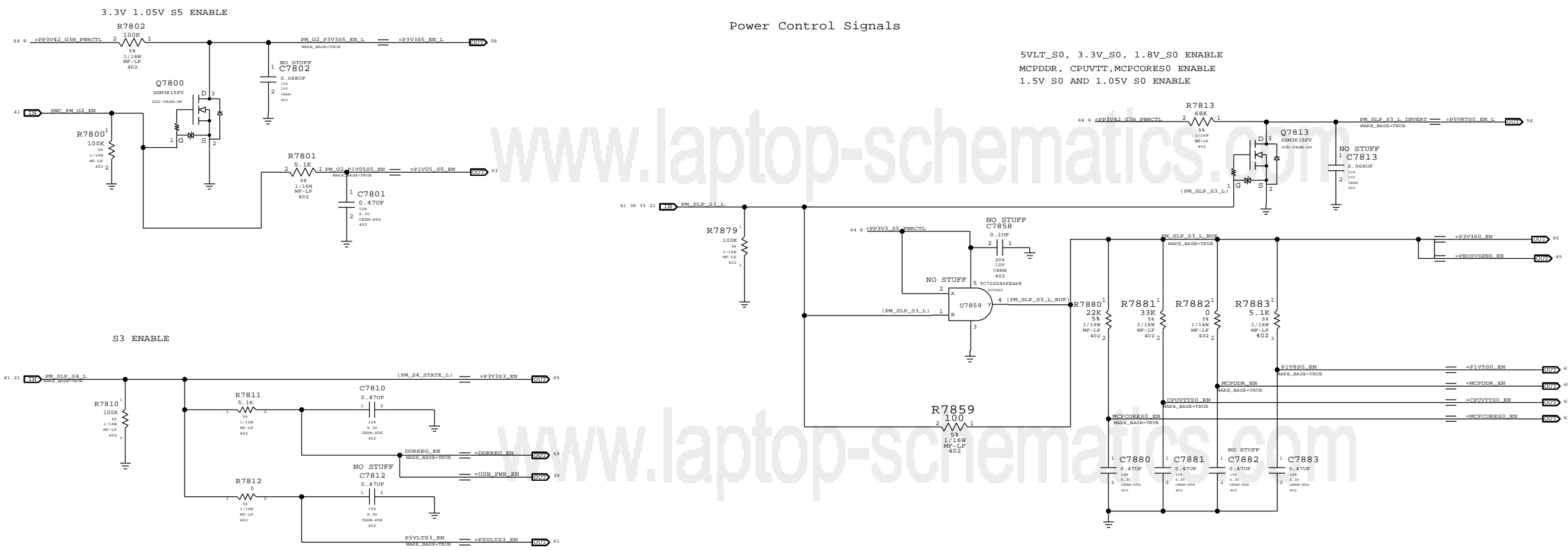
1.5V S0 SWITCH



PAGE TITLE		MISC POWER SUPPLIES	
Apple Inc.		DESIGN NUMBER	M122 D
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Power Control Signals

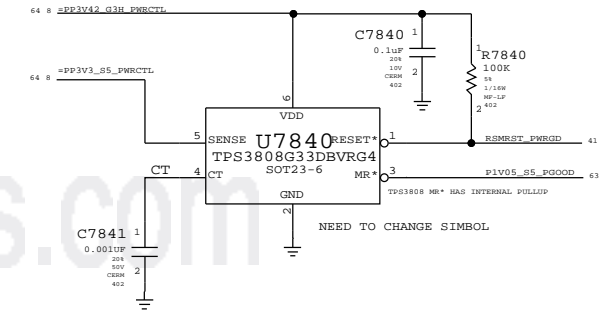
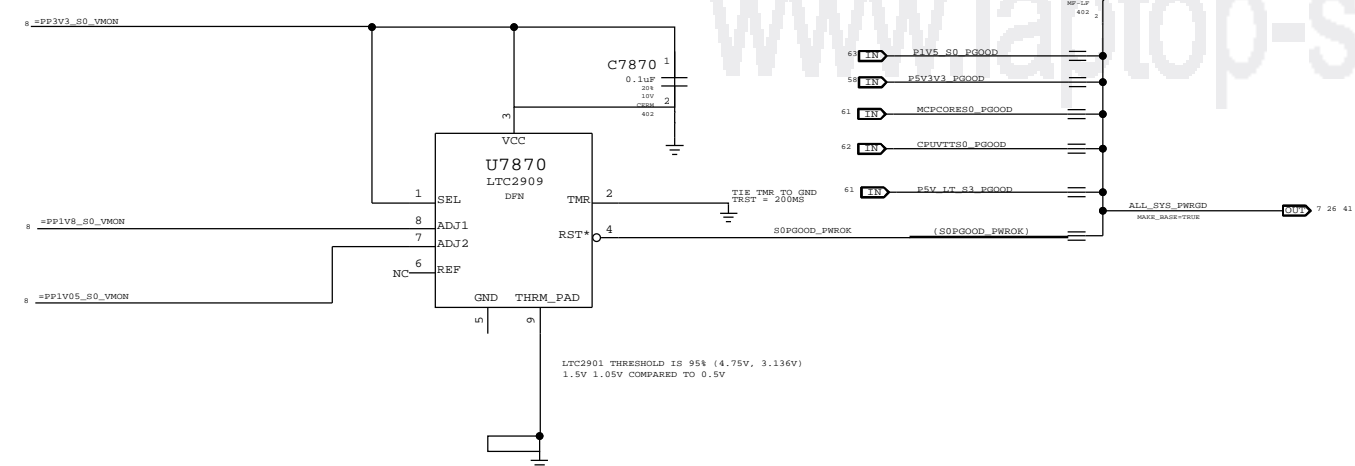
SVLT_S0, 3.3V_S0, 1.8V_S0 ENABLE
MCPDDR, CPUVTT, MCPCORES0 ENABLE
1.5V_S0 AND 1.05V_S0 ENABLE



OTHER S0 RAILS PGOOD

5.0V (RIGHT AND LEFT), 3.3V AND 1.5V S0 RAILS MONITOR CIRCUIT

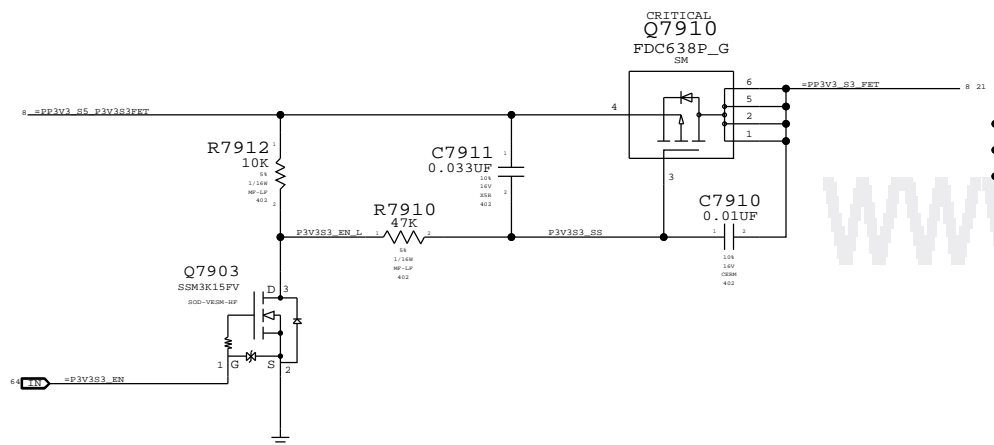
LAYOUT_NOTE: ADD XW IF NEEDS TO SAVE SPACE FOR PIN2,10,1,9



Unused PGOOD signal

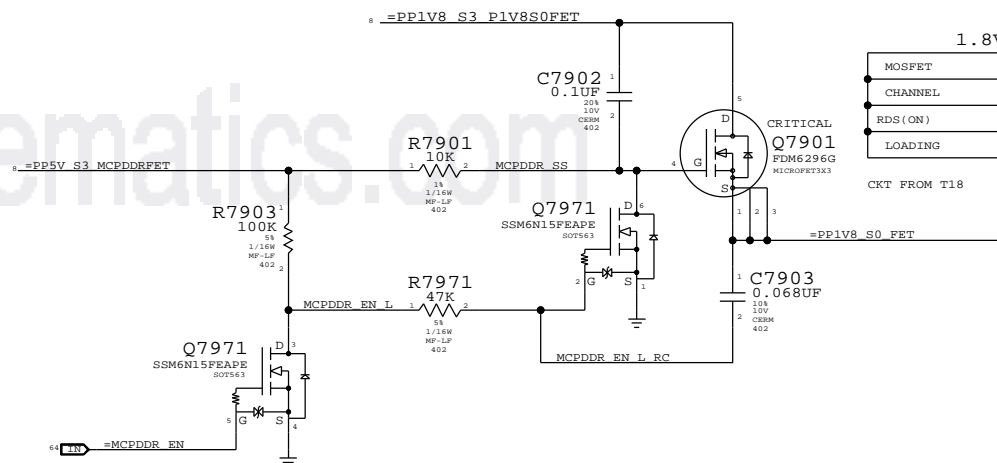
PAGE TITLE		SYNC DATE=08/17/2008	
POWER SEQUENCING		DESIGN NUMBER	1122
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3.3V S3 FET



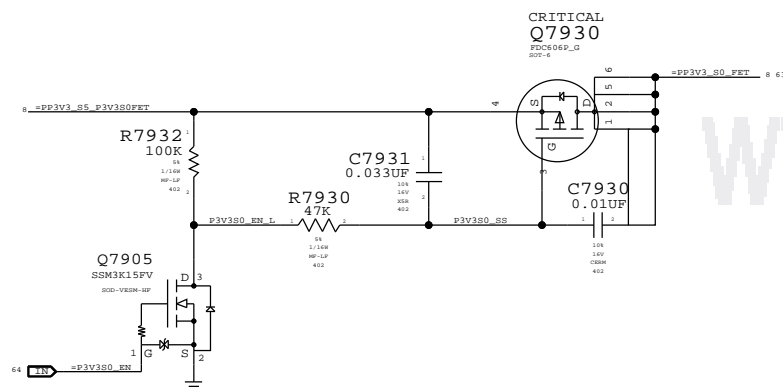
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.182 A (EDP)

1.8V S0 FET
(1.8V S0 FET FOR DDR2 MEM)



MOSFET	FDM6296G
CHANNEL	N-TYPE
RDS(ON)	15 MOHM @4.5V VGS
LOADING	5A (EDP)

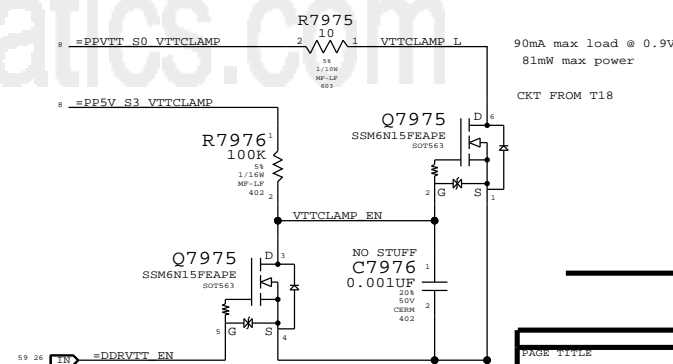
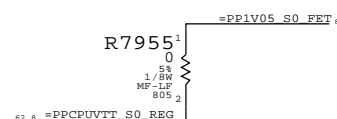
3.3V S0 FET



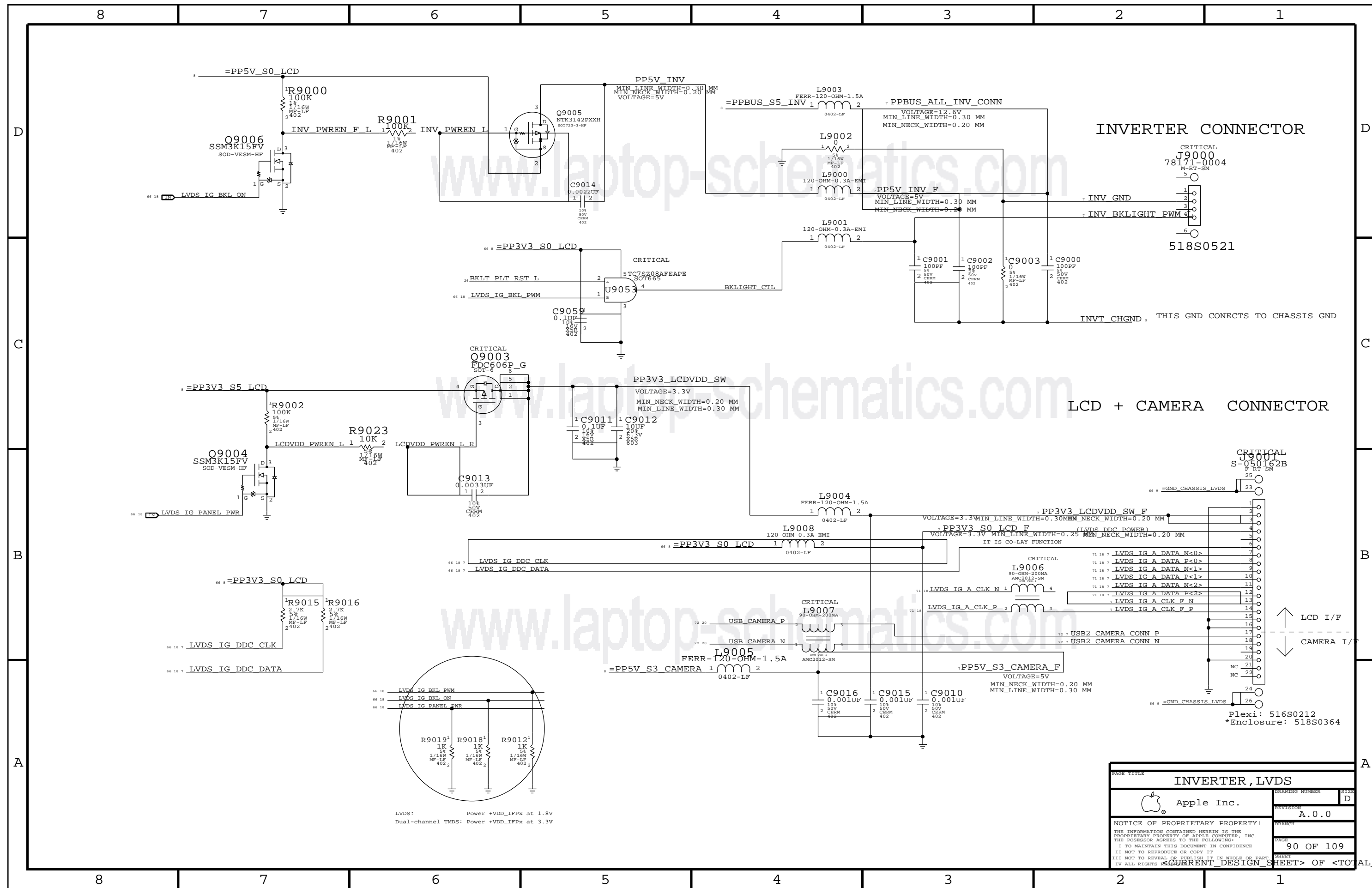
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.431 A (EDP)

MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT NVIDIA RECOMMENDS UNPOWERING DURING SLEEP. IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE MUST GUARANTEE MEM_CKE SIGNALS ARE LOW BEFORE RAIL IS TURNED OFF, AND REMAINS LOW UNTIL AFTER RAIL TURNS BACK ON OR DIMMS WILL EXIT SELF-REFRESH PREMATURELY. MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS LOW THROUGH VTT TERMINATION RESISTORS.



PAGE TITLE		POWER FETS	
Apple Inc.		DESIGN NUMBER	1122 D
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		PAGE	79 OF 109
		SHEET	
		CURRENT DESIGN SHEET OF TOTAL DESIGN SHEETS	



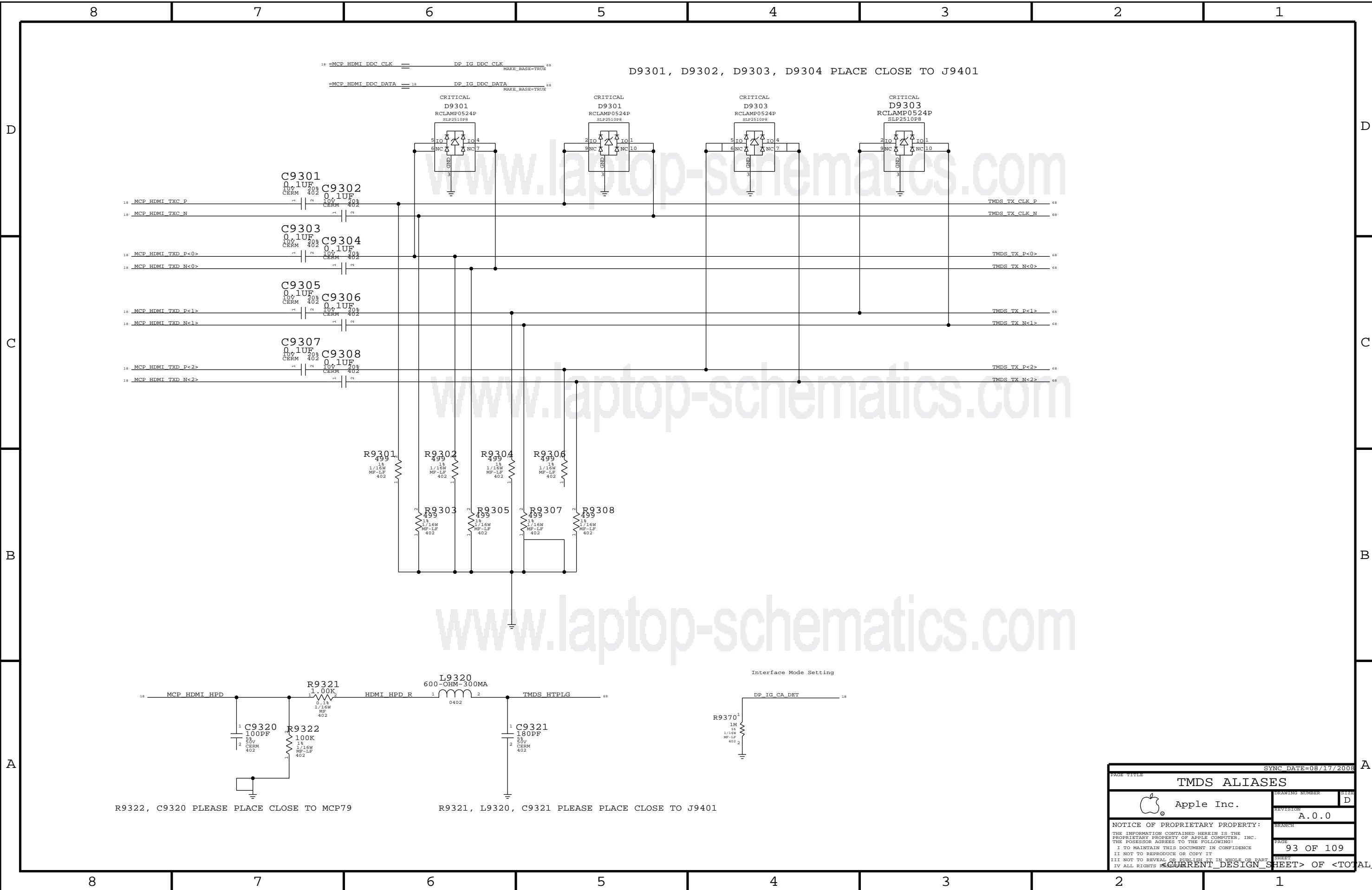
INVERTER CONNECTOR

LCD + CAMERA CONNECTOR

PAGE TITLE		INVERTER, LVDS	
DRAWING NUMBER		D	
REVISION		A.0.0	
BRANCH			
PAGE		90 OF 109	
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LVDS: Power +VDD_IPFx at 1.8V
Dual-channel TMDS: Power +VDD_IPFx at 3.3V

Plexi: 516S0212
*Enclosure: 518S0364



D9301, D9302, D9303, D9304 PLACE CLOSE TO J9401

MCP HDMI DDC CLK == DP IG DDC CLK MAKE_BASE=TRUE
 MCP HDMI DDC DATA == DP IG DDC DATA MAKE_BASE=TRUE

CRITICAL
 D9301
 RCLAMP0524P
 SLP2510P8

CRITICAL
 D9302
 RCLAMP0524P
 SLP2510P8

CRITICAL
 D9303
 RCLAMP0524P
 SLP2510P8

CRITICAL
 D9304
 RCLAMP0524P
 SLP2510P8

C9301
 0.1uF
 50V
 CERM
 402

C9302
 0.1uF
 50V
 CERM
 402

C9303
 0.1uF
 50V
 CERM
 402

C9304
 0.1uF
 50V
 CERM
 402

C9305
 0.1uF
 50V
 CERM
 402

C9306
 0.1uF
 50V
 CERM
 402

C9307
 0.1uF
 50V
 CERM
 402

C9308
 0.1uF
 50V
 CERM
 402

R9301
 18
 1/16W
 MF-LP
 402

R9302
 18
 1/16W
 MF-LP
 402

R9304
 18
 1/16W
 MF-LP
 402

R9306
 18
 1/16W
 MF-LP
 402

R9303
 18
 1/16W
 MF-LP
 402

R9305
 18
 1/16W
 MF-LP
 402

R9307
 18
 1/16W
 MF-LP
 402

R9308
 18
 1/16W
 MF-LP
 402

R9321
 1.00K
 18
 1/16W
 MF-LP
 402

L9320
 600-OHM-300MA
 0402

C9321
 180PF
 50V
 CERM
 402

Interface Mode Setting

R9370
 18
 18
 1/16W
 MF-LP
 402

R9322, C9320 PLEASE PLACE CLOSE TO MCP79

R9321, L9320, C9321 PLEASE PLACE CLOSE TO J9401

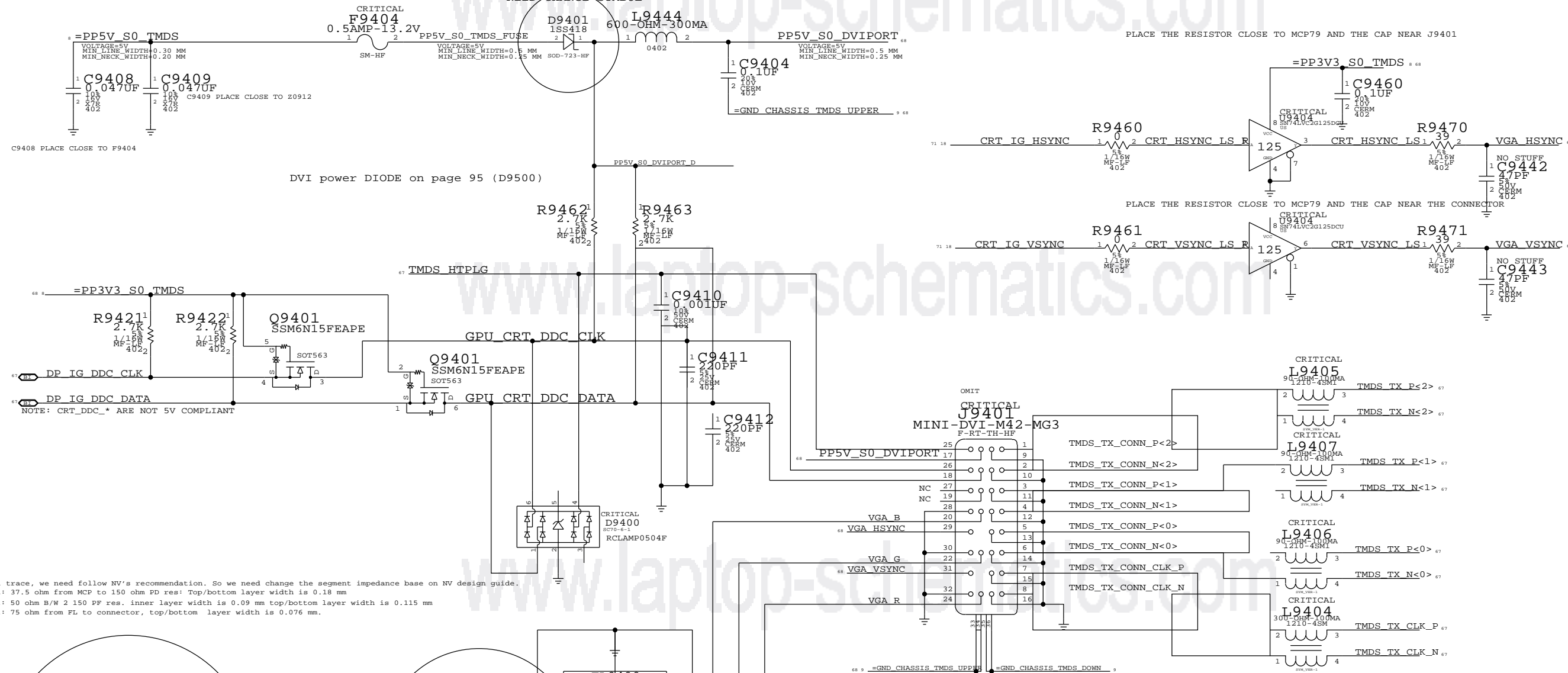
PAGE TITLE		SYNC DATE=08/17/2008	
TMDS ALIASES		DRAWING NUMBER	REV D
Apple Inc.		REVISION	A.0.0
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Video Connectors

EXTERNAL VIDEO (VGA) INTERFACE

Isolation required for DVI power switch

TMDS (MINI DVI) INTERFACE



for VG signal trace, we need follow NV's recommendation. So we need change the segment impedance base on NV design guide.
 for A segment: 37.5 ohm from MCP to 150 ohm PD res; Top/bottom layer width is 0.18 mm
 for B segment: 50 ohm B/W 2 150 PF res; inner layer width is 0.09 mm top/bottom layer width is 0.115 mm
 for C segment: 75 ohm from FL to connector; top/bottom layer width is 0.076 mm.

PAGE TITLE		MINI-DVI CONNECTOR	
Apple Inc.		CREATING NUMBER	1122
		REVISION	A.0.0
		BRANCH	
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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFPPAIR	=1:1_DIFPPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?	FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?	FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?	FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	*	=2x_DIELECTRIC	?	FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?	FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4x signals / groups shown in signal table on right. Signals within each 4x group should be matched within 5 ps of strobe. DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps. Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s. DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2x signals / groups shown in signal table on right. Signals within each 2x group should be matched within 20 ps. ADSTB#s should be matched +/- 300 ps. Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1x signals shown in signal table on right. Signals within each 1x group should be matched to CPU clock, +/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer. Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?	CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_BMIL	*	8 MIL	?				
CPU_COMP	*	25 MIL	?				
CPU_GTLREF	*	25 MIL	?				
CPU_ITP	*	=2:1_SPACING	?				
CPU_VCCSENSE	*	25 MIL	?				

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?	CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB D L<15..0>	10 14
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB DINV L<0>	10 14
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<0>	10 14
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<0>	10 14
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB D L<31..16>	10 14
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB DINV L<1>	10 14
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<1>	10 14
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<1>	10 14
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB D L<47..32>	10 14
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB DINV L<2>	10 14
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<2>	10 14
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<2>	10 14
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB D L<63..48>	10 14
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB DINV L<3>	10 14
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<3>	10 14
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<3>	10 14
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB A L<16..3>	10 14
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB REQ L<4..0>	10 14
FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB ADSTB L<0>	10 14
FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB A L<35..17>	10 14
FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB ADSTB L<1>	10 14
FSB_1X	FSB_50S	FSB_1X	FSB ADS L	10 14
FSB_BREQ0	FSB_50S	FSB_1X	FSB BREQ0 L	10 14
FSB_BREQ1	FSB_50S	FSB_1X	FSB BREQ1 L	14
FSB_1X	FSB_50S	FSB_1X	FSB BNR L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB BPRI L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB DBSY L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB DEFER L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB DRDY L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB HIT L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB HITM L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB LOCK L	10 14
FSB_CPURST	FSB_50S	FSB_1X	FSB CPURST L	10 13 14
FSB_1X	FSB_50S	FSB_1X	FSB RS L<2..0>	10 14
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L	10 14
CPU_ASYM*	CPU_50S	CPU_ASYM	CPU A20M L	10 14
CPU_BSEL	CPU_50S	CPU_ASYM	CPU BSEL<2..0>	9 10
CPU_FERR	CPU_50S	CPU_BMIL	CPU FERR L	10 14
CPU_IGNNE	CPU_50S	CPU_ASYM	CPU IGNNE L	10 14
CPU_INIT	CPU_50S	CPU_ASYM	CPU INIT L	10 14
CPU_INTR	CPU_50S	CPU_ASYM	CPU INTR	10 14
CPU_NMI	CPU_50S	CPU_ASYM	CPU NMI	10 14
CPU_PROCHOT	CPU_50S	CPU_ASYM	CPU PROCHOT L	10 14 42 60
CPU_PWRGD	CPU_50S	CPU_ASYM	CPU PWRGD	10 13 14
CPU_SMI	CPU_50S	CPU_ASYM	CPU SMI L	10 14
CPU_STPCLK	CPU_50S	CPU_ASYM	CPU STPCLK L	10 14
PM_THRMTRIP	CPU_50S	CPU_BMIL	PM THRMTRIP L	10 14 42
FSB_CPUSLP	CPU_50S	CPU_ASYM	FSB CPUSLP L	10 14
CPU_DESLP	CPU_50S	CPU_ASYM	CPU DESLP L	10 14
CPU_DPRSTP	CPU_50S	CPU_ASYM	CPU DPRSTP L	10 14 60
FSB_DPWR	CPU_50S	CPU_ASYM	FSB DPWR L	10 14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP VDD	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP GND	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP VCC	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP GND	14
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P	10 14
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N	10 14
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP P	7 13 14
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP N	7 13 14
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP P	14
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP N	14
CPU_IERR	CPU_50S		CPU IERR L	10
PM DPRSLPVR	CPU_50S	CPU_ASYM	PM DPRSLPVR	21 60
(See above)	CPU_50S	CPU_ASYM	IMVP DPRSLPVR	60
CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU GTLREF	10 27
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<3>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	10
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<1>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	10
XDP_TDI	CPU_50S	CPU_TTP	XDP TDI	6 7 10 13
XDP_TDO	CPU_50S	CPU_TTP	XDP TDO	6 10
XDP_TMS	CPU_50S	CPU_TTP	XDP TMS	6 7 10 13
XDP_TCK	CPU_50S	CPU_TTP	XDP TCK	6 7 10 13
XDP_TRST	CPU_50S	CPU_TTP	XDP TRST L	6 7 10 13
XDP_BPM	CPU_50S	CPU_TTP	XDP BPM L<4..0>	7 10 13
XDP_BPM	CPU_50S	CPU_TTP	XDP BPM L<5>	7 10 13
(FSB_CPURST L)	CPU_50S	CPU_TTP	XDP CPURST L	7 13
CPU_VID<6..0>	CPU_50S	CPU_BMIL	CPU VID<6..0>	11 60
IMVP6_VID<6..0>	CPU_50S	CPU_BMIL	IMVP6 VID<6..0>	11 60
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P	11 60
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N	11 60
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN P	
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN N	

Apple Inc. CPU/FSB Constraints

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DATE: 08/17/2008

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PAGE: 100 OF 109

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SR	=40_OHM_SE	=40_OHM_SR	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SR	=40_OHM_SE	=40_OHM_SR	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_20THER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_20THER
MEM_CTRL	*	*	MEM_20THER
MEM_CMD	*	*	MEM_20THER
MEM_DATA	*	*	MEM_20THER
MEM_DQS	*	*	MEM_20THER

Need to support MEM*-style wildcards!

DDR2:
 DQ signals should be matched within 20 ps of associated DQS pair.
 DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
 All DQS pairs should be matched within 100 ps of clocks.
 CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
 A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
 All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
 DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:
 DQ signals should be matched within 5 ps of associated DQS pair.
 DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 180 ps.
 No DQS to clock matching requirement.
 CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
 A/BA/cmd signals should be matched within 5 ps of CLK pairs.
 All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
 DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
 SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		NET_TYPE	VALUE
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK P<5..0>	15 28
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK N<5..0>	15 28
MEM_A_CKE	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>	15 28 30
MEM_A_CKE	MEM_40S_VDD	MEM_CTRL	MEM_A_CS I<3..0>	15 28 30
MEM_A_CKE	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>	15 28 30
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A A<14..0>	15 28 30
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A BA<2..0>	15 28 30
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A RAS L	15 28 30
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A CAS L	15 28 30
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A WE L	15 28 30
MEM_A_DQ	MEM_40S	MEM_DATA	MEM_A DQ<7..0>	15 28
MEM_A_DQ	MEM_40S	MEM_DATA	MEM_A DQ<15..8>	15 28
MEM_A_DQ	MEM_40S	MEM_DATA	MEM_A DQ<23..16>	15 28
MEM_A_DQ	MEM_40S	MEM_DATA	MEM_A DQ<31..24>	15 28
MEM_A_DQ	MEM_40S	MEM_DATA	MEM_A DQ<39..32>	15 28
MEM_A_DQ	MEM_40S	MEM_DATA	MEM_A DQ<47..40>	15 28
MEM_A_DQ	MEM_40S	MEM_DATA	MEM_A DQ<55..48>	15 28
MEM_A_DQ	MEM_40S	MEM_DATA	MEM_A DQ<63..56>	15 28
MEM_A_DM	MEM_40S	MEM_DATA	MEM_A DM<0>	15 28
MEM_A_DM	MEM_40S	MEM_DATA	MEM_A DM<1>	15 28
MEM_A_DM	MEM_40S	MEM_DATA	MEM_A DM<2>	15 28
MEM_A_DM	MEM_40S	MEM_DATA	MEM_A DM<3>	15 28
MEM_A_DM	MEM_40S	MEM_DATA	MEM_A DM<4>	15 28
MEM_A_DM	MEM_40S	MEM_DATA	MEM_A DM<5>	15 28
MEM_A_DM	MEM_40S	MEM_DATA	MEM_A DM<6>	15 28
MEM_A_DM	MEM_40S	MEM_DATA	MEM_A DM<7>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS P<0>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS N<0>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS P<1>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS N<1>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS P<2>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS N<2>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS P<3>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS N<3>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS P<4>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS N<4>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS P<5>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS N<5>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS P<6>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS N<6>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS P<7>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS N<7>	15 28
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK P<5..0>	15 29
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK N<5..0>	15 29
MEM_B_CKE	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>	15 29 30
MEM_B_CKE	MEM_40S_VDD	MEM_CTRL	MEM_B_CS I<3..0>	15 29 30
MEM_B_CKE	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>	15 29 30
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B A<14..0>	15 29 30
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B BA<2..0>	15 29 30
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B RAS L	15 29 30
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B CAS L	15 29 30
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B WE L	15 29 30
MEM_B_DQ	MEM_40S	MEM_DATA	MEM_B DQ<7..0>	15 29
MEM_B_DQ	MEM_40S	MEM_DATA	MEM_B DQ<15..8>	15 29
MEM_B_DQ	MEM_40S	MEM_DATA	MEM_B DQ<23..16>	15 29
MEM_B_DQ	MEM_40S	MEM_DATA	MEM_B DQ<31..24>	15 29
MEM_B_DQ	MEM_40S	MEM_DATA	MEM_B DQ<39..32>	15 29
MEM_B_DQ	MEM_40S	MEM_DATA	MEM_B DQ<47..40>	15 29
MEM_B_DQ	MEM_40S	MEM_DATA	MEM_B DQ<55..48>	15 29
MEM_B_DQ	MEM_40S	MEM_DATA	MEM_B DQ<63..56>	15 29
MEM_B_DM	MEM_40S	MEM_DATA	MEM_B DM<0>	15 29
MEM_B_DM	MEM_40S	MEM_DATA	MEM_B DM<1>	15 29
MEM_B_DM	MEM_40S	MEM_DATA	MEM_B DM<2>	15 29
MEM_B_DM	MEM_40S	MEM_DATA	MEM_B DM<3>	15 29
MEM_B_DM	MEM_40S	MEM_DATA	MEM_B DM<4>	15 29
MEM_B_DM	MEM_40S	MEM_DATA	MEM_B DM<5>	15 29
MEM_B_DM	MEM_40S	MEM_DATA	MEM_B DM<6>	15 29
MEM_B_DM	MEM_40S	MEM_DATA	MEM_B DM<7>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS P<0>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS N<0>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS P<1>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS N<1>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS P<2>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS N<2>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS P<3>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS N<3>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS P<4>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS N<4>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS P<5>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS N<5>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS P<6>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS N<6>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS P<7>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS N<7>	15 29
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP_VDD	16
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP_GND	16

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	=4:1_SPACING	?
CRT_2CRT	*	=STANDARD	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	16 MIL	?
MCP_DAC_COMP	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT

CRT signal single-ended impedance varies by location:
 - 37.5-ohm from MCP to first termination resistor.
 - 50-ohm from first to second termination resistor.
 - 75-ohm from output of three-pole filter to connector (if possible).
 R/G/B signals should be matched as close as possible and < 10 inches.
 SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.1 & 2.5.2.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	?	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3X_DIELECTRIC	?
LVDS	*	=3X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4X_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4X_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
 DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
 DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
 Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
 SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SATA_100D_HDD	*	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4X_DIELECTRIC	?
SATA_TERM	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
PEG R2D	ECIE 90D	ECIE	PEG R2D P<15.0>
PEG R2D	ECIE 90D	ECIE	PEG R2D N<15.0>
PEG R2D	ECIE 90D	ECIE	PEG R2D C P<15.0>
PEG R2D	ECIE 90D	ECIE	PEG R2D C N<15.0>
PEG D2R	ECIE 90D	ECIE	PEG D2R P<15.0>
PEG D2R	ECIE 90D	ECIE	PEG D2R N<15.0>
PEG D2R	ECIE 90D	ECIE	PEG D2R C P<15.0>
PEG D2R	ECIE 90D	ECIE	PEG D2R C N<15.0>
PCI MINI R2D P	ECIE 90D	ECIE	PCI MINI R2D P
PCI MINI R2D N	ECIE 90D	ECIE	PCI MINI R2D N
PCI MINI R2D C P	ECIE 90D	ECIE	PCI MINI R2D C P
PCI MINI R2D C N	ECIE 90D	ECIE	PCI MINI R2D C N
PCI MINI D2R P	ECIE 90D	ECIE	PCI MINI D2R P
PCI MINI D2R N	ECIE 90D	ECIE	PCI MINI D2R N
PCI FW R2D P	ECIE 90D	ECIE	PCI FW R2D P
PCI FW R2D N	ECIE 90D	ECIE	PCI FW R2D N
PCI FW R2D C P	ECIE 90D	ECIE	PCI FW R2D C P
PCI FW R2D C N	ECIE 90D	ECIE	PCI FW R2D C N
PCI FW D2R P	ECIE 90D	ECIE	PCI FW D2R P
PCI FW D2R N	ECIE 90D	ECIE	PCI FW D2R N
PCI FW D2R C P	ECIE 90D	ECIE	PCI FW D2R C P
PCI FW D2R C N	ECIE 90D	ECIE	PCI FW D2R C N
PCI EXCARD R2D P	ECIE 90D	ECIE	PCI EXCARD R2D P
PCI EXCARD R2D N	ECIE 90D	ECIE	PCI EXCARD R2D N
PCI EXCARD R2D C P	ECIE 90D	ECIE	PCI EXCARD R2D C P
PCI EXCARD R2D C N	ECIE 90D	ECIE	PCI EXCARD R2D C N
PCI EXCARD D2R P	ECIE 90D	ECIE	PCI EXCARD D2R P
PCI EXCARD D2R N	ECIE 90D	ECIE	PCI EXCARD D2R N
CLK_PCIE_100D	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M P
CLK_PCIE_100D	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M N
CLK_PCIE_100D	CLK_PCIE_100D	CLK_PCIE	PCI CLK100M MINI P
CLK_PCIE_100D	CLK_PCIE_100D	CLK_PCIE	PCI CLK100M MINI N
CLK_PCIE_100D	CLK_PCIE_100D	CLK_PCIE	PCI CLK100M FW P
CLK_PCIE_100D	CLK_PCIE_100D	CLK_PCIE	PCI CLK100M FW N
CLK_PCIE_100D	CLK_PCIE_100D	CLK_PCIE	PCI CLK100M EXCARD P
CLK_PCIE_100D	CLK_PCIE_100D	CLK_PCIE	PCI CLK100M EXCARD N
MCP_PEX_CLK_COMP	MCP_PEX_CLK_COMP	MCP_PEX_COMP	MCP PEX CLK COMP
CRT_RED	CRT_MCP_E	CRT	CRT IG R C PR
CRT_GREEN	CRT_MCP_E	CRT	CRT IG G Y Y
CRT_BLUE	CRT_MCP_E	CRT	CRT IG B COMP EB
CRT_SYNC	CRT_50S	CRT_SYNC	CRT IG HSYNC
CRT_SYNC	CRT_50S	CRT_SYNC	CRT IG VSYNC
MCP_DAC_RSET	MCP_DAC_COMP	MCP_DAC_COMP	MCP TV DAC RSET
MCP_DAC_VREF	MCP_DAC_COMP	MCP_DAC_COMP	MCP TV DAC VREF
TMDS IG TXC P	DE_100D	DISPLAYPORT	TMDS IG TXC P
TMDS IG TXC N	DE_100D	DISPLAYPORT	TMDS IG TXC N
TMDS IG TXD P<2.0>	DE_100D	DISPLAYPORT	TMDS IG TXD P<2.0>
TMDS IG TXD N<2.0>	DE_100D	DISPLAYPORT	TMDS IG TXD N<2.0>
DP MI	DE_100D	DISPLAYPORT	DP IG MI P<3.0>
DP MI	DE_100D	DISPLAYPORT	DP IG MI N<3.0>
DP AUX CH	DE_100D	DISPLAYPORT	TP DP IG AUX CH P
DP AUX CH	DE_100D	DISPLAYPORT	TP DP IG AUX CH N
MCP_HDMI_RSET	MCP_DV_COMP	MCP_DV_COMP	MCP HDMI RSET
MCP_HDMI_VPROBE	MCP_DV_COMP	MCP_DV_COMP	MCP HDMI VPROBE
LVDS IG A CLK P	LVDS_100D	LVDS	LVDS IG A CLK P
LVDS IG A CLK N	LVDS_100D	LVDS	LVDS IG A CLK N
LVDS IG A DATA P<2.0>	LVDS_100D	LVDS	LVDS IG A DATA P<2.0>
LVDS IG A DATA N<2.0>	LVDS_100D	LVDS	LVDS IG A DATA N<2.0>
LVDS IG A DATA P<3>	LVDS_100D	LVDS	LVDS IG A DATA P<3>
LVDS IG A DATA N<3>	LVDS_100D	LVDS	LVDS IG A DATA N<3>
LVDS IG B CLK P	LVDS_100D	LVDS	LVDS IG B CLK P
LVDS IG B CLK N	LVDS_100D	LVDS	LVDS IG B CLK N
LVDS IG B DATA P<2.0>	LVDS_100D	LVDS	LVDS IG B DATA P<2.0>
LVDS IG B DATA N<2.0>	LVDS_100D	LVDS	LVDS IG B DATA N<2.0>
LVDS IG B DATA P<3>	LVDS_100D	LVDS	LVDS IG B DATA P<3>
LVDS IG B DATA N<3>	LVDS_100D	LVDS	LVDS IG B DATA N<3>
MCP_I2PAR_RSET	MCP_DV_COMP	MCP_DV_COMP	MCP I2PAR RSET
MCP_I2PAR_VPROBE	MCP_DV_COMP	MCP_DV_COMP	MCP I2PAR VPROBE
SATA HDD R2D	SATA_100D_HDD	SATA	SATA HDD R2D C P
SATA HDD R2D	SATA_100D_HDD	SATA	SATA HDD R2D C N
SATA HDD R2D	SATA_100D_HDD	SATA	SATA HDD R2D P
SATA HDD R2D	SATA_100D_HDD	SATA	SATA HDD R2D N
SATA HDD R2D	SATA_100D_HDD	SATA	SATA HDD R2D UF P
SATA HDD R2D	SATA_100D_HDD	SATA	SATA HDD R2D UF N
SATA HDD D2R	SATA_100D_HDD	SATA	SATA HDD D2R P
SATA HDD D2R	SATA_100D_HDD	SATA	SATA HDD D2R N
SATA HDD D2R	SATA_100D_HDD	SATA	SATA HDD D2R C P
SATA HDD D2R	SATA_100D_HDD	SATA	SATA HDD D2R C N
SATA ODD R2D	SATA_100D	SATA	SATA ODD R2D C P
SATA ODD R2D	SATA_100D	SATA	SATA ODD R2D C N
SATA ODD R2D	SATA_100D	SATA	SATA ODD R2D P
SATA ODD R2D	SATA_100D	SATA	SATA ODD R2D N
SATA ODD R2D	SATA_100D	SATA	SATA ODD R2D UF P
SATA ODD R2D	SATA_100D	SATA	SATA ODD R2D UF N
SATA ODD D2R	SATA_100D	SATA	SATA ODD D2R P
SATA ODD D2R	SATA_100D	SATA	SATA ODD D2R N
SATA ODD D2R	SATA_100D	SATA	SATA ODD D2R C P
SATA ODD D2R	SATA_100D	SATA	SATA ODD D2R C N
SATA ODD D2R	SATA_100D	SATA	SATA ODD D2R UF P
SATA ODD D2R	SATA_100D	SATA	SATA ODD D2R UF N
MCP_SATA_TERM	SATA_TERM	MCP_SATA_TERM	MCP SATA TERM

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_BIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7..0>	7 13 19
PCI_AD	PCI_55S	PCI	PCI AD<23..8>	
PCI_AD24	PCI_55S	PCI	PCI AD<24>	
PCI_AD	PCI_55S	PCI	PCI AD<31..25>	
PCI_AD	PCI_55S	PCI	PCI PAR	
PCI_C_BE_L	PCI_55S	PCI	PCI C BE L<3..0>	
PCI_CNTL	PCI_55S	PCI	PCI IRDY L	
PCI_CNTL	PCI_55S	PCI	PCI DEVSEL L	
PCI_CNTL	PCI_55S	PCI	PCI PERR L	
PCI_CNTL	PCI_55S	PCI	PCI SERR L	
PCI_CNTL	PCI_55S	PCI	PCI STOP L	
PCI_CNTL	PCI_55S	PCI	PCI TRDY L	
PCI_CNTL	PCI_55S	PCI	PCI FRAME L	
PCI_REQD_L	PCI_55S	PCI	PCI REQ0 L	19
PCI_REQD_L	PCI_55S	PCI	PCI GNT0 L	
PCI_REQD_L	PCI_55S	PCI	PCI REQ1 L	19
PCI_GNT1_L	PCI_55S	PCI	PCI GNT1 L	
PCI_INTX_L	PCI_55S	PCI	PCI INTX L	
PCI_INTX_L	PCI_55S	PCI	PCI INTY L	
PCI_INTX_L	PCI_55S	PCI	PCI INTZ L	
MCP_PCI_CLK2	CLK PCI_55S	CLK PCI	PCI CLK33M MCP R	19
MCP_PCI_CLK	CLK PCI_55S	CLK PCI	PCI CLK33M MCP	19
LPC_AD	LPC_55S	LPC	LPC AD<3..0>	7 19 41 43
LPC_FRAME_L0	LPC_55S	LPC	LPC FRAME L	7 19 41 43
LPC_RESET_L	LPC_55S	LPC	LPC RESET L	19 26
MCP_LPC_CLK	CLK LPC_55S	CLK LPC	LPC CLK33M SMC R	19 26
MCP_LPC_CLK	CLK LPC_55S	CLK LPC	LPC CLK33M SMC	26 41
MCP_LPC_CLK	CLK LPC_55S	CLK LPC	LPC CLK33M LCPPLUS	7 26 43
USB_EXTA	USB_90D	USB	USB EXTA P	20 39
USB_EXTA	USB_90D	USB	USB EXTA N	20 39
USB_EXTA	USB_90D	USB	USB2 EXTA MUXED P	39
USB_EXTA	USB_90D	USB	USB2 EXTA MUXED N	39
USB_EXTA	USB_90D	USB	USB2 EXTA F P	39
USB_EXTA	USB_90D	USB	USB2 EXTA F N	39
USB_MINI	USB_90D	USB	USB MINI P	9 20
USB_MINI	USB_90D	USB	USB MINI N	9 20
USB_MINI	USB_90D	USB	USB2 AIRPORT P	7 31
USB_MINI	USB_90D	USB	USB2 AIRPORT N	7 31
USB_EXTB	USB_90D	USB	USB EXTB P	9 20
USB_EXTB	USB_90D	USB	USB EXTB N	9 20
USB_CAMERA	USB_90D	USB	USB CAMERA P	20 66
USB_CAMERA	USB_90D	USB	USB CAMERA N	20 66
USB_CAMERA	USB_90D	USB	USB2 CAMERA CONN P	7 66
USB_CAMERA	USB_90D	USB	USB2 CAMERA CONN N	7 66
USB_IR	USB_90D	USB	USB IR P	20 60
USB_IR	USB_90D	USB	USB IR N	20 60
USB_TPAD	USB_90D	USB	USB TPAD P	9 20
USB_TPAD	USB_90D	USB	USB TPAD N	9 20
USB_TPAD	USB_90D	USB	CONN TPAD USB P	7 49
USB_TPAD	USB_90D	USB	CONN TPAD USB N	7 49
USB_BT	USB_90D	USB	USB BT P	9 20
USB_BT	USB_90D	USB	USB BT N	9 20
USB_BT	USB_90D	USB	USB2 BT F P CONN	7 40
USB_BT	USB_90D	USB	USB2 BT F N CONN	7 40
USB_EXTB	USB_90D	USB	USB EXTB P	20 39
USB_EXTB	USB_90D	USB	USB EXTB N	20 39
USB_EXTB	USB_90D	USB	USB2 EXTB F P	39
USB_EXTB	USB_90D	USB	USB2 EXTB F N	39
USB_EXCARD	USB_90D	USB	USB EXCARD P	9 20
USB_EXCARD	USB_90D	USB	USB EXCARD N	9 20
USB_EXTC	USB_90D	USB	USB EXTC P	9 20
USB_EXTC	USB_90D	USB	USB EXTC N	9 20
MCP_USB_BIAS	MCP_USB_BIAS		MCP USB BIAS GND	20
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS MCP 0 CLK	7 13 21 44
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS MCP 0 DATA	7 13 21 44
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS MCP 1 CLK	21 44
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS MCP 1 DATA	21 44
HDA_BIT_CLK	HDA_55S	HDA	HDA BIT CLK	21 52
HDA_BIT_CLK	HDA_55S	HDA	HDA BIT CLK R	21
HDA_SYNC	HDA_55S	HDA	HDA SYNC	21 52
HDA_SYNC	HDA_55S	HDA	HDA SYNC R	21
HDA_RST_L	HDA_55S	HDA	HDA RST R L	21
HDA_RST_L	HDA_55S	HDA	HDA RST L	21 52
HDA_SDIN0	HDA_55S	HDA	HDA SDIN0	21 52
HDA_SDIN0	HDA_55S	HDA	HDA SDIN CODEC	21 52
HDA_SDOIT	HDA_55S	HDA	HDA SDOIT	21
HDA_SDOIT	HDA_55S	HDA	HDA SDOIT R	21 52
MCP_HDA_PULLDN_COMP	MCP_HDA_COMP		MCP_HDA_PULLDN_COMP	21
MCP_SIO_CLK	CLK_SLOW_55S	CLK_SLOW	PM CLK32K SUSCLK R	21 26
MCP_SIO_CLK	CLK_SLOW_55S	CLK_SLOW	PM CLK32K SUSCLK	26 41
SPI_CLK	SPI_55S	SPI	SPI CLK R	21 43
SPI_CLK	SPI_55S	SPI	SPI CLK MUX	43 51
SPI_MOSI	SPI_55S	SPI	SPI MOSI R	21 43
SPI_MOSI	SPI_55S	SPI	SPI MOSI MUX	43 51
SPI_MISO	SPI_55S	SPI	SPI MISO MUX	43 51
SPI_MISO	SPI_55S	SPI	SPI MISO R	51
SPI_CS0	SPI_55S	SPI	SPI CS0 R L	21 43
SPI_CS0	SPI_55S	SPI	SPI CS0 L	

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MCP Constraints 2

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SR	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP VDD	18
MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP GND	18
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP CLK25M_BUF0_R	18 33
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP CLK25M_BUF0	18 33
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	18 32
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET MDIO	18 32
ENET_MDC	ENET_MII_55S	ENET_MII	ENET MDC	18 32
ENET_PWDWN_L	ENET_MII_55S	ENET_MII	ENET_PWDWN_L	18 32
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET CLK125M_RXCLK	18 32
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET CLK125M_RXCLK_R	18 32
ENET_RX_CTRL	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	18 32
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET CLK125M_TXCLK	18 32
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET CLK125M_TXCLK_R	18 32
ENET_TXD<0>	ENET_MII_55S	ENET_MII	ENET_TXD<0>	18 32
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	18 32
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	18 32
ENET_RESET_L	ENET_MII_55S	ENET_MII	ENET_RESET_L	18 32
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET MDI P<3..0>	12 34
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET MDI N<3..0>	12 34

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	7

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FW_P0_TPA_P	FW_110D	FW_TP	FW_P0_TPA_P	35 37
FW_P0_TPA_N	FW_110D	FW_TP	FW_P0_TPA_N	35 37
FW_P0_TPB_P	FW_110D	FW_TP	FW_P0_TPB_P	35 37
FW_P0_TPB_N	FW_110D	FW_TP	FW_P0_TPB_N	35 37
FW_P1_TPA_P	FW_110D	FW_TP	FW_P1_TPA_P	35 37
FW_P1_TPA_N	FW_110D	FW_TP	FW_P1_TPA_N	35 37
FW_P1_TPB_P	FW_110D	FW_TP	FW_P1_TPB_P	35 37
FW_P1_TPB_N	FW_110D	FW_TP	FW_P1_TPB_N	35 37
FW_PORT_A_P	FW_110D	FW_TP	FW_PORT_A_P	37
FW_PORT_A_N	FW_110D	FW_TP	FW_PORT_A_N	37
FW_PORT_B_P	FW_110D	FW_TP	FW_PORT_B_P	37
FW_PORT_B_N	FW_110D	FW_TP	FW_PORT_B_N	37

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1T01_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
SMBUS SMC A S3 SCL	SMB 550	5MM	SMBUS SMC A S3 SCL
SMBUS SMC A S3 SDA	SMB 550	5MM	SMBUS SMC A S3 SDA
SMBUS SMC B S0 SCL	SMB 550	5MM	SMBUS SMC B S0 SCL
SMBUS SMC B S0 SDA	SMB 550	5MM	SMBUS SMC B S0 SDA
SMBUS SMC O S0 SCL	SMB 550	5MM	SMBUS SMC O S0 SCL
SMBUS SMC O S0 SDA	SMB 550	5MM	SMBUS SMC O S0 SDA
SMBUS SMC BSA SCL	SMB 550	5MM	SMBUS SMC BSA SCL
SMBUS SMC BSA SDA	SMB 550	5MM	SMBUS SMC BSA SDA
SMBUS SMC MGMT SCL	SMB 550	5MM	SMBUS SMC MGMT SCL
SMBUS SMC MGMT SDA	SMB 550	5MM	SMBUS SMC MGMT SDA

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
CHGR CSI	1T01_DIFFPAIR		CHGR CSI P
CHGR CSI	1T01_DIFFPAIR		CHGR CSI N
CHGR CSO	1T01_DIFFPAIR		CHGR CSO P
CHGR CSO	1T01_DIFFPAIR		CHGR CSO N

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SMC Constraints

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K36B BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS				BOARD AREAS				BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA_P1MM				MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.115 MM	0.115 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.165 MM			
40_OHM_SE	*	Y	0.145 MM	0.145 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
27F4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.310 MM			
27F4_OHM_SE	*	Y	0.275 MM	0.275 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.175 MM	0.175 MM	0.200 MM	0.200 MM	0.200 MM
70_OHM_DIFF	TOP, BOTTOM	Y	0.185 MM	0.185 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.109 MM	0.109 MM	0.220 MM	0.220 MM	0.220 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.089 MM	0.089 MM	0.230 MM	0.230 MM	0.230 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
100_OHM_DIFF_HDD	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF_HDD	ISL3, ISL4, ISL9, ISL10	Y	0.095 MM	0.095 MM	0.400 MM	0.400 MM	0.400 MM
100_OHM_DIFF_HDD	TOP, BOTTOM	Y	0.095 MM	0.095 MM		0.400 MM	0.400 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.075 MM	0.075 MM	0.330 MM	0.330 MM	0.330 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
1:1_DIFPPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	TOP, BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP, BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP, BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP, BOTTOM	0.350 MM	?
2X_DIELECTRIC	*	0.152 MM	?
3X_DIELECTRIC	*	0.228 MM	?
4X_DIELECTRIC	*	0.304 MM	?
5X_DIELECTRIC	*	0.380 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_LPC	*	BGA_P1MM	BGA_P2MM
CLK_PCI	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P2MM
CLK_SLOW	*	BGA_P1MM	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P3MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA_P1MM	STANDARD
MEM_40S_VDD	BGA_P1MM	STANDARD

SYNC DATE=08/17/2008

Apple Inc.

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