1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

SCHEM,MLB,D1

8/8/12

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9216	1	SCHEM,MLB,D1	SCH	CRITICAL	
820-3462	1	PCBF,MLB(NEW),D1	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=ABBREV
LAST_MODIFIED=Thu Aug 9 12:34:09 2012

DRAWING TITLE: SCHEM,MLB,D1

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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U1000
INTEL CPU
2.X GHz
IVY BRIDGE 2C-35W
PG 9-15

J2500 XDP CONN PG 23

DDR3-1333/1600MHZ

U3100-U3170 Mem PG 28

U2900-U2970 Mem PG 27

INTEL
PANTHER POINT-MPCH
U1800
PG 16-21

GPIO PG 19 | FDI PG 17 | DMI PG 17 | RTC PG 16

CLK BUFFER PG 16 | MISC PG 19 | SPI PG 16 | SATA PG 16 | LPC PG 16 | PWR CTRL PG 17 | LVDS OUT | RGB OUT | DP OUT | DVI OUT | TMDS OUT PG 17 | eDP OUT PG 17 | PCI PG 18 | HDMI PG 17 | JTAG PG 16 | SMBUS PG 16 | PEG PG 16 | PCI-E (UP TO 8 LINES) PG 16 | HDA PG 16

USB (UP TO 14 DEVICES) PG 18 — 0 1 2 3 4 5 6 7 8 9 10 11 12 13

USB 3 PG 18 — 1 2 3 4

U2600 SYSTEM CLOCK PG 24

U4510 SATA REDRIVER PG 36 — 1.05V/6GHZ.

J4500 SATA CONN HDD PG 36

U6100 SPI Boot ROM PG 49

J6900, J6950 DC/BATT PG 55

POWER SUPPLY PG 56-65

U5550,U5570 TEMP SENSOR PG 47

U5920,U5940 Motion Sensor/GYRO PG 48

U5340,U5350,U5360,U5370,U5400,U5410,Q5480 Q5490 POWER SENSE PG 42, 43

J5650,J5660 FAN CONN AND CONTROL PG 45

U4900 SMC PG 38 — I2C SMS ADC Fan Ser Prt

SPI

J5100 LPC+SPI Conn Port80,serial PG 40

J9400 DP/TBT PORT CONN PG 68,69 — PortA PortB

U9420 MUX PG 68

U9620 MUX PG 69

U3600 TBT Host — CIO PCIe x4 CIO PG 32,33

DP

J9000 eDP CONN PG 66

J4410 RIO CONN HDMI PG 35

J4410 RIO CONN Bluetooth PG 35

U5701 TP/KB PSOC PG 46

J5700, J5713 TRACKPAD/ KEYBOARD PG 46

J3502 CAMERA PG 31

U4900 SMC PG 38

U2700 USB HUB PG 25 — 1 2 3

U2760 USB MUX PG 25 — EHCI XHCI

J4410 RIO CONN USB 3 PG 35

J4600 EXTERNAL A USB 3 PG37

J4410 RIO CONN Airport/SD Card PG 35

From PCH

J2550 PCH XDP CONN PG 23

U6201 AUDIO Codec PG 50 — EXTMIC LINEIN HPOUT SPDIF MICIN LINEOUT

U6750 MIC BIAS PG53

U6610,U6620 U6630,U6640 SPEAKER AMPs PG 52

J6701 PG 53 | J5815 PG 47 | J6802 J6803 PG 54

AUDIO CONNs

SYNC_MASTER=MASTER SYNC_DATE=02/15/2013

PAGE TITLE: System Block Diagram

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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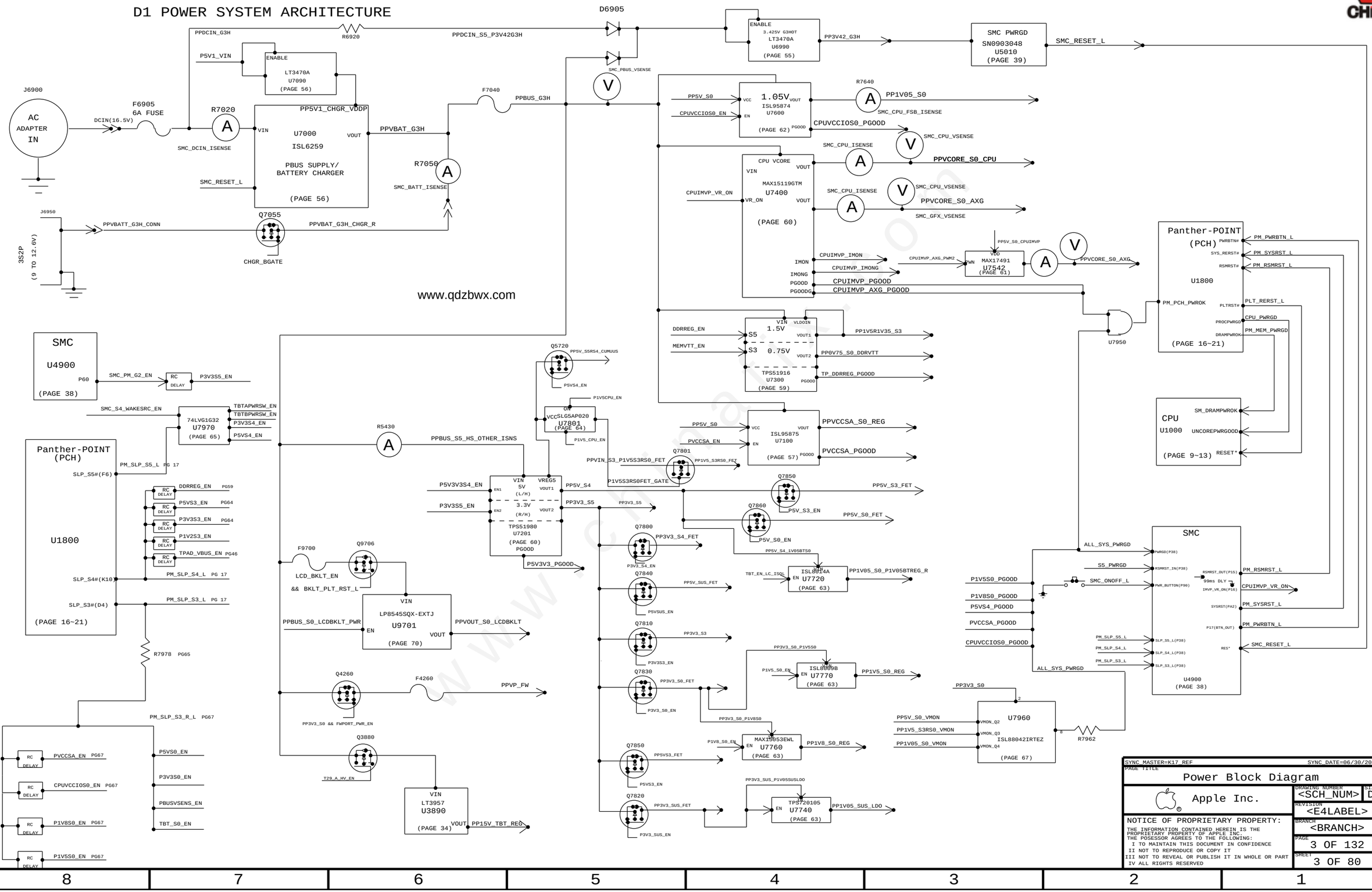
D1 POWER SYSTEM ARCHITECTURE



SYNC_MASTER=K17_REF SYNC_DATE=06/30/2009

PAGE TITLE

Power Block Diagram

Apple Inc.

DRAWING NUMBER	<SCH_NUM>
SIZE	D
REVISION	<E4LABEL>
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PAGE	3 OF 132
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SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

Revision History

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
085-4094	DEV BOM,MLB,D1	D1_DEVEL:PVB
607-9189	CMN PTS,PCBA,MLB,D1	D1_COMMON
639-3288	PCBA,2.5G,SS 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:DWP2,RAM_6G_SAMSUNG_35NM_CH0_1600_S
639-3289	PCBA,2.9G,SS 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:DWNY,RAM_6G_SAMSUNG_35NM_CH0_1600_S
639-3290	PCBA,2.5G,HYNIX 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:DWP0,RAM_6G_HYNIX_CH0_1600_S
639-3291	PCBA,2.9G,HYNIX 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:DWNW,RAM_6G_HYNIX_CH0_1600_S
639-3694	PCBA,2.5G,SS 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:F16P,RAM_4G_SAMSUNG_35NM_1600_S
639-3695	PCBA,2.9G,SS 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:F16M,RAM_4G_SAMSUNG_35NM_1600_S
639-3696	PCBA,2.9G,HYNIX 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:F16N,RAM_4G_HYNIX_1600_S
639-3697	PCBA,2.5G,HYNIX 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:F16V,RAM_4G_HYNIX_1600_S
639-3773	PCBA,2.5G,ELPIDA 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:F26M,RAM_6G_ELPIDA_CH0_1600_S
639-3772	PCBA,2.9G,ELPIDA 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:F26J,RAM_6G_ELPIDA_CH0_1600_S
639-3770	PCBA,2.5G,ELPIDA 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:F26L,RAM_4G_ELPIDA_1600_S
639-3771	PCBA,2.9G,ELPIDA 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:F26H,RAM_4G_ELPIDA_1600_S
639-3849	PCBA,2.5G,MICRON 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:F2WT,RAM_6G_MICRON_CH0_1600_S
639-3848	PCBA,2.9G,MICRON 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:F2WR,RAM_6G_MICRON_CH0_1600_S
639-3873	PCBA,2.6G,SS 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33H,RAM_6G_SAMSUNG_35NM_CH0_1600_S
639-3874	PCBA,2.8G,SS 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F33P,RAM_6G_SAMSUNG_35NM_CH0_1600_S
639-3875	PCBA,2.6G,HYNIX 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33L,RAM_6G_HYNIX_CH0_1600_S
639-3876	PCBA,2.8G,HYNIX 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F339,RAM_6G_HYNIX_CH0_1600_S
639-3881	PCBA,2.6G,SS 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33G,RAM_4G_SAMSUNG_35NM_1600_S
639-3882	PCBA,2.8G,SS 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F33C,RAM_4G_SAMSUNG_35NM_1600_S
639-3884	PCBA,2.8G,HYNIX 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F337,RAM_4G_HYNIX_1600_S
639-3883	PCBA,2.6G,HYNIX 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33D,RAM_4G_HYNIX_1600_S
639-3877	PCBA,2.6G,ELPIDA 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33Q,RAM_6G_ELPIDA_CH0_1600_S
639-3878	PCBA,2.8G,ELPIDA 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F338,RAM_6G_ELPIDA_CH0_1600_S
639-3885	PCBA,2.6G,ELPIDA 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33J,RAM_4G_ELPIDA_1600_S
639-3886	PCBA,2.8G,ELPIDA 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F33N,RAM_4G_ELPIDA_1600_S
639-3879	PCBA,2.6G,MICRON 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33M,RAM_6G_MICRON_CH0_1600_S
639-3880	PCBA,2.8G,MICRON 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F336,RAM_6G_MICRON_CH0_1600_S
639-3846	PCBA,2.5G,MICRON 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:F2WV,RAM_4G_MICRON_1600_S
639-3847	PCBA,2.9G,MICRON 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:F2WQ,RAM_4G_MICRON_1600_S
639-3887	PCBA,2.6G,MICRON 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33K,RAM_4G_MICRON_1600_S
639-3888	PCBA,2.8G,MICRON 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F33F,RAM_4G_MICRON_1600_S

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DV7Q]	CRITICAL	EEEE:DV7Q
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DWNY]	CRITICAL	EEEE:DWNY
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DWNW]	CRITICAL	EEEE:DWNW
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DWP0]	CRITICAL	EEEE:DWP0
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DWP2]	CRITICAL	EEEE:DWP2
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F16M]	CRITICAL	EEEE:F16M
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F16N]	CRITICAL	EEEE:F16N
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F16P]	CRITICAL	EEEE:F16P
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F16V]	CRITICAL	EEEE:F16V
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F26H]	CRITICAL	EEEE:F26H
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F26J]	CRITICAL	EEEE:F26J
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F26L]	CRITICAL	EEEE:F26L
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F26M]	CRITICAL	EEEE:F26M
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F2WQ]	CRITICAL	EEEE:F2WQ
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F2WR]	CRITICAL	EEEE:F2WR
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F2WT]	CRITICAL	EEEE:F2WT
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F2WV]	CRITICAL	EEEE:F2WV
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F336]	CRITICAL	EEEE:F336
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F337]	CRITICAL	EEEE:F337
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826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F339]	CRITICAL	EEEE:F339
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33C]	CRITICAL	EEEE:F33C
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33D]	CRITICAL	EEEE:F33D
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33F]	CRITICAL	EEEE:F33F
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33G]	CRITICAL	EEEE:F33G
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33H]	CRITICAL	EEEE:F33H
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33J]	CRITICAL	EEEE:F33J
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33K]	CRITICAL	EEEE:F33K
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33L]	CRITICAL	EEEE:F33L
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33M]	CRITICAL	EEEE:F33M
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33N]	CRITICAL	EEEE:F33N
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33P]	CRITICAL	EEEE:F33P
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33Q]	CRITICAL	EEEE:F33Q

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0364	128S0264		ALL	Kemet alt to Sanyo
128S0303	128S0353		ALL	Panasonic alt to Sanyo
376S0953	376S0958		ALL	RENESAS ALT TO FAIRCHILD
128S0311	128S0329		ALL	NEC ALT TO SANYO
353S3237	353S2192		ALL	TI ALT TO INTERSIL
376S0977	376S0859		ALL	Diodes alt to Toshiba
138S0722	138S0691		ALL	Multi alt to Samsung
197S0487	197S0485		ALL	Epson alt to TXC
197S0484	197S0485		ALL	NDK alt to TXC
197S0479	197S0486		ALL	Epson alt to TXC
197S0478	197S0486		ALL	NDK alt to TXC
197S0481	197S0480		ALL	Epson alt to NDK
376S0972	376S0612		ALL	ROHM alt to Toshiba
376S1053	376S0604		ALL	Diodes alt to Fairchild
376S1017	376S0612		ALL	ROHM alt to Toshiba
138S0624	138S0677		ALL	Murata alt to Taiyo Yuden
138S0681	138S0638		ALL	Taiyo Yuden alt to Samsung
152S1703	152S1701		ALL	Sumida alt to Cyntec
371S0730	371S0490		ALL	Diodes alt to NXP
138S0725	138S0724		ALL	Samsung alt to Murata
138S0727	138S0709		ALL	Samsung alt to Murata
376S1080	376S0820		ALL	Diodes alt to ON Semi
372S0186	372S0185		ALL	NXP alt to Diodes
128S0363	128S0296		ALL	NEC alt to Sanyo
376S0903	376S0796		ALL	Fairchild alt to Siliconix
740S0144	740S0118		ALL	Littlefuse alt to Polytronic
152S1539	152S1598		ALL	Cyntec alt to Toko
152S1645	152S0461		ALL	Cyntec alt to Vishay
155S0667	155S0583		ALL	MAG LAYERS ALT TO MURATA
103S0305	103S0266		ALL	Yageo alt to Cyntec
112S0274	112S0254		ALL	Yageo alt to Cyntec
376S1113	376S1110		ALL	Diodes to AOS
155S0588	155S0367		ALL	murata ALT TO MURATA

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4181	1	IVB,QBP0,ES2,KB,2.3,35W,2+2,1.0,3M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.3G_ES2
337S4182	1	IVB,QBP0,ES2,KB,2.6,35W,2+2,1.05,4M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.6G_ES2
337S4292	1	IVB,Q4CT,Q5,L1,2.5,35W,2+2,1.1,3M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.5G_Q5
337S4300	1	IVB,QC36,Q5,L1,2.6,35W,2+2,1.2,3M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.6G_Q5
337S4302	1	IVB,QC34,Q5,L1,2.8,35W,2+2,1.2,3M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.8G_Q5
337S4294	1	IVB,QC4M,Q5,L1,2.9,35W,2+2,1.25,4M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.9G_Q5
337S4264	1	IVB,S R0N0,PRQ,L1,2.5,35W,2+2,1.1,3M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.5G
337S4338	1	IVB,S R0MY,PRQ,L1,2.6,35W,2+2,1.2,3M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.6G
337S4339	1	IVB,S R0MU,PRQ,L1,2.8,35W,2+2,1.2,3M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.8G
337S4265	1	IVB,S R0MU,PRQ,L1,2.9,35W,2+2,1.25,4M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.9G
337S4180	1	IC,PCH,PPT-MB SFF,ES2,B0	U1800	CRITICAL	PCH_ES2
337S4235	1	IC,PCH,PPT-MB SFF,P-Q5,C0	U1800	CRITICAL	PCH_C0
337S4283	1	IC,PCH,PPT-MB SFF,PRQ,C1	U1800	CRITICAL	PCH_C1
338S1113	1	IC,TBT,CR-4C,B1,FRQ,288FCBGA,12X12MM	U3600	CRITICAL	TBTRTR:B1
333S0623	16	IC,SDRAM,2GBIT,256MX8,DDR3-1600,78FBGA	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070,U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	2G_SAMSUNG_35NM_1600_S
333S0622	16	IC,SDRAM,2GBIT,256MX8,DDR3-1600,78FBGA	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070,U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	2G_HYNIX_1600_S
333S0628	16	IC,SDRAM,DDR3-1600,256MX8,78FBGA,D-DIE,ELPIDA	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070,U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	2G_ELPIDA_1600_S
333S0649	16	IC,SDRAM,DDR3-1600,256MX8,78FBGA,MICRON	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070,U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	2G_MICRON_1600_S
333S0625	16	IC,SDRAM,DDR3-1600,512MX8,78FBGA,HYNIX	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070,U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	4G_HYNIX_1600_S
333S0629	16	IC,SDRAM,DDR3-1600,512MX8,78FBGA,B-DIE,ELPIDA	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070,U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	4G_ELPIDA_1600_S
333S0624	16	IC,SDRAM,DDR3-1600,512MX8,78FBGA,D35,SAMSUNG	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070,U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	4G_SAMSUNG_35NM_1600_S
333S0623	8	IC,SDRAM,2GBIT,256MX8,DDR3-1600,78FBGA	U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	6G_SAMSUNG_35NM_CH0_1600_S
333S0624	8	IC,SDRAM,DDR3-1600,512MX8,78FBGA,D35,SAMSUNG	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070	CRITICAL	6G_SAMSUNG_35NM_CH0_1600_S
333S0622	8	IC,SDRAM,2GBIT,256MX8,DDR3-1600,78FBGA	U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	6G_HYNIX_CH0_1600_S
333S0625	8	IC,SDRAM,DDR3-1600,512MX8,78FBGA,HYNIX	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070	CRITICAL	6G_HYNIX_CH0_1600_S
333S0628	8	IC,SDRAM,DDR3-1600,256MX8,78FBGA,D-DIE,ELPIDA	U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	6G_ELPIDA_CH0_1600_S
333S0629	8	IC,SDRAM,DDR3-1600,512MX8,78FBGA,B-DIE,ELPIDA	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070	CRITICAL	6G_ELPIDA_CH0_1600_S
333S0660	16	IC,SDRAM,DDR3-1600,512MX8,78FBGA,MICRON	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070,U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	4G_MICRON_1600_S
333S0649	8	IC,SDRAM,DDR3-1600,256MX8,78FBGA,MICRON	U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	6G_MICRON_CH0_1600_S
333S0660	8	IC,SDRAM,DDR3-1600,512MX8,78FBGA,MICRON	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070	CRITICAL	6G_MICRON_CH0_1600_S

D1 BOM GROUPS

BOM GROUP	BOM OPTIONS
D1_COMMON	ALTERNATE,COMMON,D1_COMMON1,D1_COMMON2,D1_PROGPARTS,D1_PVB
D1_COMMON1	CPUMEM:S0,SMC_DEBUG_YES,TBTBST:Y,TBTRTR:B1,TBTHV:P15V,HUB_2NONREM,USBHUB:2512B,AXG_PHASE2,TBTISNS:YES
D1_COMMON2	EDP:YES,PPDDR:1V35,LPCPLUS_CONN:YES,LPCPLUS_R:YES,CAPS:INT,BTPWR:S4,SKIP_5V3V3:AUDIBLE,TPAD_5V_LDO:S5,SMS
D1_PVB	LOADISNS:NO,LCDBKLT:PROD,KBDBKLT:PROD
D1_PROGPARTS	SMC_PROG:PVB,TBTROM:PROG,BOOTROM_PROG:PVB,TPAD_PSOC:PROG
D1_BLANK	
D1_DEVEL:ENG	ALTERNATE,IVB_PPT_XDP,LOADISNS:YES,S0PGOOD_ISL,DDRVREF_DAC,VREFDQ:M1_M3,VREFCA:LDO_DAC
D1_DEVEL:PVB	ALTERNATE,IVB_PPT_XDP,VREFDQ:M1_M3,VREFCA:LDO
IVB_PPT_XDP	XDP,XDP_CONN,XDP_CPU:BPM,XDP_PCH

DDR3 SPD STRAPPINGS

BOM GROUP	BOM OPTIONS
RAM_4G_HYNIX_1600_S	4G_HYNIX_1600_S,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM_2G_ELPIDA_1600_S	2G_ELPIDA_1600_S,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H
RAM_4G_SAMSUNG_28NM_1600_S	4G_SAMSUNG_28NM_1600_S,RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM_2G_MICRON_1600_S	2G_MICRON_1600_S,RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H
RAM_4G_ELPIDA_1600_S	4G_ELPIDA_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM_4G_SAMSUNG_35NM_1600_S	4G_SAMSUNG_35NM_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H
RAM_6G_SAMSUNG_35NM_CH0_1600_S	6G_SAMSUNG_35NM_CH0_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L
RAM_4G_MICRON_1600_S	4G_MICRON_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H
RAM_6G_MICRON_CH0_1600_S	6G_MICRON_CH0_1600_S,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM_6G_ELPIDA_CH0_1600_S	6G_ELPIDA_CH0_1600_S,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM_6G_SAMSUNG_28NM_CH0_1600_S	6G_SAMSUNG_28NM_CH0_1600_S,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H
RAM_6G_HYNIX_CH0_1600_S	6G_HYNIX_CH0_1600_S,RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM_2G_SAMSUNG_1600_S	2G_SAMSUNG_35NM_1600_S,RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H
RAM_2G_HYNIX_1600_S	2G_HYNIX_1600_S,RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0642	16	IC,SDRAM,DDR3-1600,512MX8,78FBGA,C-DIE,SAMSUNG	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070,U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	4G_SAMSUNG_28NM_1600_S
333S0623	8	IC,SDRAM,2GBIT,256MX8,DDR3-1600,78FBGA	U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	6G_SAMSUNG_28NM_CH0_1600_S
333S0642	8	IC,SDRAM,DDR3-1600,512MX8,78FBGA,C-DIE,SAMSUNG	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070	CRITICAL	6G_SAMSUNG_28NM_CH0_1600_S

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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PD Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
860-1533	1	STDOFF,BMU,TOPSIDE,D1,SM	J6950_63	CRITICAL	
860-1530	1	STDOFF-1.9D2.93H-TH-0.85-1.2	J6950_64	CRITICAL	
860-1529	1	STDOFF-1.80D1.53H-SM	J6950_65	CRITICAL	
825-7841	1	LBL,PART CONFIG,BOARDS,D2	CONFIG_LABEL	CRITICAL	
946-4350	1	D1 MLB LOCTITE UV GLUE 190024/S 0.24G	EDGE_BOND	CRITICAL	

DEVELOPMENT/BASE BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-4094	1	D1 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
607-9189	1	D1 MLB BASE BOM	BASE	CRITICAL	BASE_BOM

SMC

341S3528	1	IC,SMC12,PROTO1,D1	U4900	CRITICAL	SMC_PROG:PROTO
341S3404	1	IC,SMC,DEVELOPMENT-PIB,D1	U4900	CRITICAL	SMC_PROG:PIB
341S3405	1	IC,SMC,DEVELOPMENT-FSB,D1	U4900	CRITICAL	SMC_PROG:FSB
341S3406	1	IC,SMC,DEVELOPMENT-PVB,D1	U4900	CRITICAL	SMC_PROG:PVB

EFI ROM

341S3571	1	IC,EF,ROM,PROTO1,D1	U6100	CRITICAL	BOOTROM_PROG:PROTO
341S3603	1	IC,EFI,ROM,PIB, D1	U6100	CRITICAL	BOOTROM_PROG:PIB
341S3636	1	IC,EFI,ROM,PIB2, D1	U6100	CRITICAL	BOOTROM_PROG:PIB2
341S3650	1	IC,EFI,ROM,FSB, D1	U6100	CRITICAL	BOOTROM_PROG:FSB
341SXXXX	1	IC,EFI,ROM,FSB2, D1	U6100	CRITICAL	BOOTROM_PROG:FSB2
341S3667	1	IC,EFI,ROM,PVB, D1	U6100	CRITICAL	BOOTROM_PROG:PVB

Programmables - All builds

335S0809	1	64 MBIT SPI SERIAL DUAL I/O FLASH,Macronix	U6100	CRITICAL	BOOTROM_BLANK
335S0803	1	64 MBIT SPI SERIAL DUAL I/O FLASH,Numonyx	U6100	CRITICAL	BOOTROM_BLANK
341S3670	1	IC,TP PSOC,V224,PVB,D1	U5701	CRITICAL	TPAD_PSOC:PROG
337S2983	1	IC,TP PSOC,QFN,BLANK	U5701	CRITICAL	TPAD_PSOC:BLANK
341S3668	1	IC,EEPROM,CR,V14.1,D1 PVB	U3690	CRITICAL	TBTROM:PROG
335S0865	1	IC,EEPROM,SERIAL,8KB,S3C	U3690	CRITICAL	TBTROM:BLANK
338S1098	1	IC,SMC12-A3,LX4FS1AH58BC1GA3	U4900	CRITICAL	SMC_BLANK
998-3919	1	SOCKET, SMC12	J4900	CRITICAL	SMC_SOCKET

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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Functional Test Points

J3650 (LEFT FAN CONN)

FUNC_TEST
- PP5V_S0 — 7 8 — 3 TPs per Fan
- FAN_LT_PWM — 46
- FAN_LT_TACH — 46

J3660 (RIGHT FAN CONN)
- FAN_RT_PWM — 46 — 75 33 9
- FAN_RT_TACH — 46 — 75 33 9
- GND — 5 TPs per Fan

J3502 (ALS/CAMERA CONN)
- SMBUS_SMC_2_S3_SDA — 7 39 42 77
- SMBUS_SMC_2_S3_SCL — 7 39 42 77
- PP5V_S3_ALSCAMERA_F — 7 32

J4400 (RIO CABLE CONN)
- PP3V3_S4 — 7 8
- PP3V3_S3 — 7 8
- PP3V3_WLAN_F — 7 36 40 80
- PP5V_S4 — 8
- PP1V5_S0 — 8 — 75 36 17 7 / 75 36 17 7 / 75 36 17 / 75 36 17

J4410 (RIO FLEX CONN)
- USB_EXTB_OC_L — 24 36
- HDMI_IG_DDC_CLK — 9 36
- HDMI_IG_DDC_DATA — 9 36
- HDMI_HPD_L — 36 40
- PM_SLP_S3_L — 7 18 27 36 39 66
- PM_SLP_S4_L — 18 27 36 38 39 66
- AP_CLKREQ_Q_L — 7 36
- ENET_RESET_L — 25
- ENET_CLKREQ_L — 17 36
- SD_PWR_EN — 9 36
- SCONN_STATE_CHANGE_SMC — 25 40
- PCIE_WAKE_L — 7 18 36
- AP_CLKREQ_Q_L — 7 36
- AP_RESET_CONN_L — 7 36
- WIFI_EVENT_L — 36 39 40
- USB_EXTB_P — 26 36 74
- USB_EXTB_N — 26 36 74
- USB_BT_CONN_P — 9 36 74
- USB_BT_CONN_N — 9 36 74

- AP_RESET_CONN_L — 7 36
- SMBUS_PCH_CLK — 17 42 75
- SMBUS_PCH_DATA — 17 42 75

- SMBUS_SMC_1_S0_SCL — 39 42 77
- SMBUS_SMC_1_S0_SDA — 39 42 77

J5815 (KBD BACKLIGHT CONN)
- PP_KBD_BOOST_VOUT — 48
- KBDLED_CATHODE1 — 48
- KBDLED_CATHODE2 — 48
- SMC_KBDLED_PRESENT_L — 48

J6950 (MAIN BATT CONN)
- PPVBAT_G3H_CONN — 66 67
- SMBUS_SMC_5_G3_SCL — 39 42
- SMBUS_SMC_5_G3_SDA — 39 42
- SYS_DETECT_L_R

- SYSDET1
- SYSDET_3_4 — 56

J6801 (2 MIC CONN)
- CON_DMIC_PWR — 55
- CON_DMIC_SDA1 — 55
- CON_DMIC_CLK — 55

- PCH_VSS_NCTF<19> — 7
- PCH_VSS_NCTF<19> — 7

J4600 (LEFT USB CONN)
- PP5V_S3_LTUSB_A_F — 38
- USB_LT1_N — 38 74
- USB_LT1_P — 38 74

FUNC_TEST
- GND
- GND
- GND — 6 TPs

U1000 CHARZ TPS

PCIE_TBT_D2R_P<0>	1	P2MM SM	PP0700
PCIE_TBT_D2R_N<0>	1	P2MM SM	PP0701
DMI_S2N_P<0>	1	P2MM SM	PP0702
DMI_S2N_N<0>	1	P2MM SM	PP0703
DMI_CLK100M_CPU_P	1	P2MM SM	PP0721
DMI_CLK100M_CPU_N	1	PT	PP0722

U1800 CHARZ TPS

DMI_N2S_P<0>	1	P2MM SM	PP0704
DMI_N2S_N<0>	1	P2MM SM	PP0705
FDI_DATA_P<0>	1	P2MM SM	PP0706
FDI_DATA_N<0>	1	P2MM SM	PP0707
FDI_DATA_P<4>	1	P2MM SM	PP0708
FDI_DATA_N<4>	1	P2MM SM	PP0709
PCIE_AP_D2R_P	1	PT	PP0710
PCIE_AP_D2R_N	1	PT	PP0711
PCIE_ENET_D2R_P	1	PT	PP0712
PCIE_ENET_D2R_N	1	PT	PP0713
PCIE_CLK100M_TBT_P	1	PT	PP0723
PCIE_CLK100M_TBT_N	1	PT	PP0724

U4900 CHARZ TPS

LPC_AD<0>	1	P2MM SM	PP0714
LPC_AD<1>	1	P2MM SM	PP0715
LPC_AD<2>	1	P2MM SM	PP0716
LPC_AD<3>	1	P2MM SM	PP0717
LPC_FRAME_L	1	P2MM SM	PP0718
LPC_CLK33M_SMC	1	PT	PP0719
AUD_DMIC_SDA1	1	P2MM SM	PP0720

J6701 (AUDIO JACK CONN)
- AUD_CONN_SLEEVE — 54
- AUD_CONN_MIC_XW — 54
- AUD_CONN_SLEEVE_XW — 54
- AUD_CONN_HP_LEFT — 54
- AUD_CONN_TIPDET_INV — 54
- PP3V3_S0 — 7 8 78
- AUD_SPDIF_OUT_JACK — 51 54
- AUD_CONN_HP_RIGHT — 54
- AUD_CONN_TYPEDET — 54
- AUD_CONN_MIC — 54

J6802 (AUDIO LEFT SPEAKER CONN)
- SPKRCONN_L_OUT_P — 53 55 78
- SPKRCONN_L_OUT_N — 53 55 78
- SPKRCONN_L_ID — 51 55
- SPKRCONN_SL_OUT_P — 53 55 78
- SPKRCONN_SL_OUT_N — 53 55 78

J6803 (AUDIO RIGHT SPEAKER CONN)
- SPKRCONN_R_OUT_P — 53 55 78
- SPKRCONN_R_OUT_N — 53 55 78
- SPKRCONN_R_ID — 51 55
- SPKRCONN_SR_OUT_P — 53 55 78
- SPKRCONN_SR_OUT_N — 53 55 78
- GND — 53 55 78

J9000 (EDP CONN)
- PP5VR3V3_SW_LCD — 67
- PPVOUT_S0_LCDBKLT — 67 71 80 — 2 TP needed
- LED_RETURN_6 — 7 67 71
- LED_RETURN_5 — 7 67 71
- LED_RETURN_4 — 7 67 71
- LED_RETURN_3 — 7 67 71
- LED_RETURN_2 — 7 67 71
- LED_RETURN_1 — 67 71
- LCD_HPD_CONN — 67
- DP_INT_AUX_P — 67 79
- DP_INT_AUX_N — 67 79

J3401 & J3402 (AIRPORT/BT/CAMERA CONN)
- PCIE_CLK100M_AP_CONN_P — 36 78
- PCIE_CLK100M_AP_CONN_N — 36 78
- AP_CLKREQ_Q_L — 7 36
- PCIE_WAKE_L — 7 18 36
- AP_RESET_CONN_L — 7 36
- PP3V3_WLAN_F — 7 36 40 80
- PP5V_S3_ALSCAMERA_F — 7 32
- SMBUS_SMC_2_S3_SDA — 7 39 42 77
- SMBUS_SMC_2_S3_SCL — 7 39 42 77
- USB_CAMERA_CONN_P — 32 74
- USB_CAMERA_CONN_N — 32 74

J5713 (KEY BOARD CONN)
- PP3V3_S4 — 7 8
- PP3V42_G3H — 7 8
- WS_KBD1 — 47
- WS_KBD2 — 47
- WS_KBD3 — 47
- WS_KBD4 — 47
- WS_KBD5 — 47
- WS_KBD6 — 47
- WS_KBD7 — 47
- WS_KBD8 — 47
- WS_KBD9 — 47
- WS_KBD10 — 47
- WS_KBD11 — 47
- WS_KBD12 — 47
- WS_KBD13 — 47
- WS_KBD14 — 47
- WS_KBD15_CAP — 47
- WS_KBD16_NUM — 47
- WS_KBD17 — 47
- WS_KBD18 — 47
- WS_KBD19 — 47
- WS_KBD20 — 47
- WS_KBD21 — 47
- WS_KBD22 — 47
- WS_KBD23 — 47
- WS_KBD_ONOFF_L — 47
- WS_LEFT_SHIFT_KBD — 47
- WS_LEFT_OPTION_KBD — 47
- WS_CONTROL_KBD — 47

J5700 (IPD FLEX CONN)
- PP3V3_S4 — 7 8
- Z2_CS_L — 47
- Z2_MOSI — 47
- Z2_MISO — 47
- Z2_SCLK — 47
- Z2_HOST_INTN — 47
- PP5V_S4_CUMULUS — 47
- Z2_CLKIN — 47
- SMBUS_SMC_2_S3_SCL — 7 39 42 77
- SMBUS_SMC_2_S3_SDA — 7 39 42 77
- PSOC_SCLK — 47
- PSOC_MOSI — 47
- PSOC_MISO — 47
- PICKB_L — 47
- PSOC_F_CS_L — 47
- Z2_KEY_ACT_L — 47

J6900 (DC POWER CONN)
- TDM_ONEWIRE_MPM
- ADAPTER_SENSE — 56
- PP18V5_DCIN_FUSE — 56
- GND

J4500 (SSD/HDD FLEX CONN)
- PP3V3_S0_SSD_FLT — 37
- SMC_OOB1_TX_L — 37 39 40
- SMC_OOB1_RX_L — 37 39 40
- PP5V_S0_HDD_FLT — 37
- GND

FUNC_TEST
- BKLT_EN — 71
- LCD_BKLT_PWM — 9 71
- PM_CLKRUN_L — 7 18 39 41
- PM_SYSRST_L — 18 25 39
- SMC_ONOFF_L — 39 40 47

J5100 (LPC + SPI CONN)
- PP3V42_G3H — 7 8
- PP5V_S0 — 7 8
- LPC_CLK33M_LPCPLUS — 25 41 75
- LPC_AD<0> — 7 17 39 41 75
- LPC_AD<2> — 7 17 39 41 75
- LPC_AD<1> — 7 17 39 41 75
- LPC_AD<3> — 7 17 39 41 75
- SPI_ALT_MOSI — 41
- LPCPLUS_GPIO — 20 41
- LPCPLUS_RESET_L — 25 41
- SMC_TDO — 39 40 41
- TP_SMC_TRST_L — 41
- TP_SMC_MD1 — 41
- SMC_TX_L — 39 40 41
- SPI_ALT_MISO — 41
- LPC_FRAME_L — 7 17 39 41 75
- SPIROM_USE_MLB — 20 41 50
- PM_CLKRUN_L — 7 18 39 41
- SPI_ALT_CLK — 41
- SPI_ALT_CS_L — 41
- LPC_SERIRQ — 17 39 41
- LPC_PWRDWN_L — 18 25 39 41
- SMC_TDI — 39 40 41
- SMC_TCK — 39 40 41
- SMC_RESET_L — 39 40 41 57
- SMC_ROMBOOT — 40 41
- SMC_RX_L — 39 40 41
- SMC_TMS — 39 40 41

POWER RAILS

FUNC_TEST
- PM_SLP_S3_L — 7 18 27 36 39 66
- PP0V75_S0_DDRVTT — 8
- PP1V05_S0 — 8
- LED_RETURN_2 — 7 67 71
- LED_RETURN_3 — 7 67 71
- LED_RETURN_4 — 7 67 71
- LED_RETURN_5 — 7 67 71
- LED_RETURN_6 — 7 67 71
- GND — 4 TPs
- PP3V3_S0 — 7 8 78
- PP3V3_S3 — 7 8
- PP3V3_S5 — 8 78
- PP3V3_S5_AVREF_SMC — 39 40
- PP3V42_G3H — 7 8
- PP5V_S0 — 7 8
- PP5V_S3 — 8
- PP5V_S5 — 8
- PPBUS_G3H — 8
- PPDCIN_G3H — 8
- PPVCORE_S0_CPU — 8
- PPVTTDDR_S3 — 8

- DMI_S2N_P<3..1> — 10 18 72 — TBT
- DMI_S2N_N<3..1> — 10 18 72 — TBT — TRUE
- DMI_N2S_P<3..1> — 10 18 72 — TBT — TRUE
- DMI_N2S_N<3..1> — 10 18 72 — TBT — TRUE

- TBTBPWRSW_ISET_V3P3 — 70 — TBT — TRUE
- TBTBPWRSW_ISET_S0_R — 70 — TBT
- TBTBPWRSW_ISET_S3 — 70 — TBT — TRUE
- TBTAPWRSW_ISET_V3P3 — 69 — TBT — TRUE
- TBTAPWRSW_ISET_S0 — 69 — TBT — TRUE
- TBTAPWRSW_ISET_S3 — 69 — TBT — TRUE
- TBTAPWRSW_ISET_S3_R — 69 — TBT — TRUE

- TBT_A_R2D_C_P<1..0> — 33 69 76 — TBUS — TRUE
- TBT_A_R2D_C_N<1..0> — 33 69 76 — TBUS — TRUE
- TBT_A_R2D_P<1..0> — 69 76 — TBUS — TRUE
- TBT_A_R2D_N<1..0> — 69 76 — TBUS — TRUE
- TBT_A_D2R_C_P<1> — 69 76 — TBUS — TRUE
- TBT_A_D2R_C_N<1> — 69 76 — TBUS — TRUE
- TBT_A_D2R_C_P<0> — 69 76 — TBUS — TRUE
- TBT_A_D2R_C_N<0> — 69 76 — TBUS — TRUE

- TBT_A_D2R_P<1> — 33 69 76 — TBT — TRUE
- TBT_A_D2R_N<1> — 33 69 76 — TBT — TRUE
- TBT_A_D2R_P<0> — 33 69 76 — TBT — TRUE
- TBT_A_D2R_N<0> — 33 69 76 — TBT — TRUE

- TBT_B_R2D_C_P<1..0> — 33 70 76 — TBUS — TRUE
- TBT_B_R2D_C_N<1..0> — 33 70 76 — TBUS — TRUE
- TBT_B_R2D_P<1..0> — 70 76 — TBUS — TRUE
- TBT_B_R2D_N<1..0> — 70 76 — TBUS — TRUE
- TBT_B_D2R_C_P<0> — 70 76 — TBUS — TRUE
- TBT_B_D2R_C_N<0> — 70 76 — TBUS — TRUE
- TBT_B_D2R_C_P<1> — 70 76 — TBUS — TRUE
- TBT_B_D2R_C_N<1> — 70 76 — TBUS — TRUE

- TBT_B_D2R_P<0> — 33 70 76 — TBT — TRUE
- TBT_B_D2R_N<0> — 33 70 76 — TBT — TRUE
- TBT_B_D2R_P<1> — 33 70 76 — TBT — TRUE
- TBT_B_D2R_N<1> — 33 70 76 — TBT — TRUE

- PCIE_AP_D2R_P — 7 17 36 75
- PCIE_AP_D2R_N — 7 17 36 75
- PCIE_AP_R2D_P — 36 75
- PCIE_AP_R2D_N — 36 75

ICT Test Points

CPU NO_TESTs
- TP_TBT_MONDC0 — NC_TBT_MONDC0 — 33 — TRUE — MAKE_BASE=TRUE
- TP_TBT_MONDC1 — NC_TBT_MONDC1 — 33 — TRUE — MAKE_BASE=TRUE
- TP_TBT_PCIE_RESET0_L — NC_TBT_PCIE_RESET0_L — 33 — TRUE — MAKE_BASE=TRUE
- TP_TBT_PCIE_RESET1_L — NC_TBT_PCIE_RESET1_L — 33 — TRUE — MAKE_BASE=TRUE
- TP_TBT_PCIE_RESET2_L — NC_TBT_PCIE_RESET2_L — 33 — TRUE — MAKE_BASE=TRUE
- TP_TBT_PCIE_RESET3_L — NC_TBT_PCIE_RESET3_L — 33 — TRUE — MAKE_BASE=TRUE
- TP_TBT_XTAL25OUT — NC_TBT_XTAL25OUT — 33 — TRUE — MAKE_BASE=TRUE

- TP_DP_TBTSRC_ML_CP<3> — NC_DP_TBTSRC_ML_CP<3> — 33 — TRUE — MAKE_BASE=TRUE
- TP_DP_TBTSRC_ML_CN<3> — NC_DP_TBTSRC_ML_CN<3> — 33 — TRUE — MAKE_BASE=TRUE
- TP_DP_TBTSRC_ML_CP<2> — NC_DP_TBTSRC_ML_CP<2> — 33 — TRUE — MAKE_BASE=TRUE
- TP_DP_TBTSRC_ML_CN<2> — NC_DP_TBTSRC_ML_CN<2> — 33 — TRUE — MAKE_BASE=TRUE
- TP_DP_TBTSRC_ML_CP<1> — NC_DP_TBTSRC_ML_CP<1> — 33 — TRUE — MAKE_BASE=TRUE
- TP_DP_TBTSRC_ML_CN<1> — NC_DP_TBTSRC_ML_CN<1> — 33 — TRUE — MAKE_BASE=TRUE
- TP_DP_TBTSRC_ML_CP<0> — NC_DP_TBTSRC_ML_CP<0> — 33 — TRUE — MAKE_BASE=TRUE
- TP_DP_TBTSRC_ML_CN<0> — NC_DP_TBTSRC_ML_CN<0> — 33 — TRUE — MAKE_BASE=TRUE
- TP_DP_TBTSRC_AUXCH_CP — NC_DP_TBTSRC_AUXCH_CP — 33 — TRUE — MAKE_BASE=TRUE
- TP_DP_TBTSRC_AUXCH_CN — NC_DP_TBTSRC_AUXCH_CN — 33 — TRUE — MAKE_BASE=TRUE

- TP_SPI_CS1_L — NC_SPI_CS1_L — 17 — TRUE — MAKE_BASE=TRUE
- TP_PCH_GPIO8 — NC_PCH_GPIO8 — 20 — TRUE — MAKE_BASE=TRUE
- TP_PCH_STRP_BBS1 — NC_PCH_STRP_BBS1 — 19 — TRUE — MAKE_BASE=TRUE
- TP_PCH_STRP_ESI_L — NC_PCH_STRP_ESI_L — 19 — TRUE — MAKE_BASE=TRUE
- TP_PCH_TP23 — NC_PCH_TP23 — 19 — TRUE — MAKE_BASE=TRUE
- TP_PCI_CLK33M_OUT2 — NC_PCI_CLK33M_OUT2 — 19 — TRUE — MAKE_BASE=TRUE
- TP_PCIE_CLK100M_PEGAN — NC_PCIE_CLK100M_PEGAN — 17 — TRUE — MAKE_BASE=TRUE
- TP_PCIE_CLK100M_PEGAP — NC_PCIE_CLK100M_PEGAP — 17 — TRUE — MAKE_BASE=TRUE
- TP_PM_SLP_A_L — NC_PM_SLP_A_L — 18 — TRUE — MAKE_BASE=TRUE
- TP_PPVOUT_PCH_DCPSUSBYP — NC_PPVOUT_PCH_DCPSUSBYP — 21 — TRUE — MAKE_BASE=TRUE
- TP_SMC_MPM5_LED_PWR — NC_SMC_MPM5_LED_PWR — 17 — TRUE — MAKE_BASE=TRUE
- TP_SMC_MPM5_LED_CHG — NC_SMC_MPM5_LED_CHG — 17 — TRUE — MAKE_BASE=TRUE
- TP_SMS_INT2 — NC_SMS_INT2 — 49 — TRUE — MAKE_BASE=TRUE

- TP_XDP_PCH_HOOK4 — NC_XDP_PCH_HOOK4 — 24 — TRUE — MAKE_BASE=TRUE
- TP_XDP_PCH_HOOK5 — NC_XDP_PCH_HOOK5 — 24 — TRUE — MAKE_BASE=TRUE
- TP_XDP_PCH_OBSFN_B<0> — NC_XDP_PCH_OBSFN_B<0> — 24 — TRUE — MAKE_BASE=TRUE
- TP_XDP_PCH_OBSFN_B<1> — NC_XDP_PCH_OBSFN_B<1> — 24 — TRUE — MAKE_BASE=TRUE
- TP_XDP_PCH_OBSFN_A<0> — NC_XDP_PCH_OBSFN_A<0> — 24 — TRUE — MAKE_BASE=TRUE
- TP_XDP_PCH_OBSFN_A<1> — NC_XDP_PCH_OBSFN_A<1> — 24 — TRUE — MAKE_BASE=TRUE
- TP_XDP_PCH_OBSFN_D<0> — NC_XDP_PCH_OBSFN_D<0> — 24 — TRUE — MAKE_BASE=TRUE
- TP_XDP_PCH_OBSFN_D<1> — NC_XDP_PCH_OBSFN_D<1> — 24 — TRUE — MAKE_BASE=TRUE
- TP_XDP_PCH_TRST_L — NC_XDP_PCH_TRST_L — 24 — TRUE — MAKE_BASE=TRUE

- TP_1V05_S0_PCH_VCCAPLLEXP — NC_1V05_S0_PCH_VCCAPLLEXP — 21 — TRUE — MAKE_BASE=TRUE
- TP_AUD_CODEC_MICBIAS — NC_AUD_CODEC_MICBIAS — 51 — TRUE — MAKE_BASE=TRUE
- TP_AUD_MIC_INRP — NC_AUD_MIC_INRP — 51 — TRUE — MAKE_BASE=TRUE
- TP_AUD_MIC_INRN — NC_AUD_MIC_INRN — 51 — TRUE — MAKE_BASE=TRUE
- AUD_SPDIF_IN — AUD_SPDIF_IN — 51 7 — TRUE — MAKE_BASE=TRUE
- TP_BKL_FAULT — NC_BKL_FAULT — 71 — TRUE — MAKE_BASE=TRUE
- TP_LPC_DREQ0_L — NC_LPC_DREQ0_L — 17 7 — TRUE — MAKE_BASE=TRUE

- TP_PCIE_TBT_R2D_C_P<3..0> — 9 33 75 — TBUS — TRUE
- TP_PCIE_TBT_R2D_C_N<3..0> — TRUE — 9 33 75
- TP_PCIE_TBT_R2D_P<3..0> — TRUE — 33 75 — TBUS
- TP_PCIE_TBT_R2D_N<3..0> — TRUE — 33 75 — TBUS
- TP_PCIE_TBT_D2R_P<3..1> — TRUE — 9 33 75 — TBUS
- TP_PCIE_TBT_D2R_N<3..1> — TRUE — 9 33 75 — TBUS
- TP_PCIE_TBT_D2R_C_P<3..1> — TRUE — 33 75 — TBUS
- TP_PCIE_TBT_D2R_C_N<3..1> — TRUE — 33 75 — TBUS

- MEM_A_DQ<0> — 12 28 73 — MAA — TRUE
- MEM_A_DQ<12..2> — 12 28 73 — MAA — TRUE
- MEM_A_DQ<19..14> — 12 28 73 — MAA — TRUE
- MEM_A_DQ<24..21> — 12 28 73 — MAA — TRUE
- MEM_A_DQ<32..26> — 12 28 73 — MAA — TRUE
- MEM_A_DQ<42..34> — 12 28 73 — MAA — TRUE
- MEM_A_DQ<54..44> — 12 28 73 — MAA — TRUE
- MEM_A_DQ<56> — 12 28 73 — MAA — TRUE
- MEM_A_DQ<63..58> — 12 28 73 — MAA — TRUE

- MEM_B_DQ<2..0> — 12 29 73 — MAB — TRUE
- MEM_B_DQ<13..4> — 12 29 73 — MAB — TRUE
- MEM_B_DQ<19..15> — 12 29 73 — MAB — TRUE
- MEM_B_DQ<25..21> — 12 29 73 — MAB — TRUE
- MEM_B_DQ<35..27> — 12 29 73 — MAB — TRUE
- MEM_B_DQ<40..37> — 12 29 73 — MAB — TRUE
- MEM_B_DQ<47..42> — 12 29 73 — MAB — TRUE
- MEM_B_DQ<57..49> — 12 29 73 — MAB — TRUE
- MEM_B_DQ<63..59> — 12 29 73 — MAB — TRUE

- NC_MEM_EVENT_L — 40 — MAA — TRUE

- HDMI_IG_CLK_C_P — 9 36 78 — HDMI — TRUE
- HDMI_IG_CLK_C_N — 9 36 78 — HDMI — TRUE
- HDMI_IG_DATA_C_P<2..0> — 9 36 78 — HDMI — TRUE
- HDMI_IG_DATA_C_N<2..0> — 9 36 78 — HDMI — TRUE

- PCIE_CLK100M_ENET_P — 7 17 36 75 — TBUS — TRUE
- PCIE_CLK100M_ENET_N — 7 17 36 75 — TBUS — TRUE
- USB3_EXTB_TX_C_P — 36 79 — TBUS — TRUE
- USB3_EXTB_TX_C_N — 36 79 — TBUS — TRUE

S2 CAMERA PCIE SIGNALS
- NC_PCIE_CAMERA_D2RP — PCIE_EXCARD_D2R_N — 17 — MAKE_BASE=TRUE — TRUE
- NC_PCIE_CAMERA_D2RN — PCIE_EXCARD_D2R_P — 17 — MAKE_BASE=TRUE — TRUE
- NC_PCIE_CAMERA_R2D_CN — PCIE_EXCARD_R2D_C_N — 17 — MAKE_BASE=TRUE — TRUE
- NC_PCIE_CAMERA_R2D_CP — PCIE_EXCARD_R2D_C_P — 17 — MAKE_BASE=TRUE — TRUE
- NC_PCIE_CLK100M_CAMERAN — PCIE_CLK100M_EXCARD_N — 7 17 75 — MAKE_BASE=TRUE — TRUE
- NC_PCIE_CLK100M_CAMERAP — PCIE_CLK100M_EXCARD_P — 7 17 75 — MAKE_BASE=TRUE — TRUE

NO_TEST NC NO_TESTs
- NC_PCIE_5_D2RN — 17 — TRUE — MAKE_BASE=TRUE
- NC_PCIE_5_D2RP — 17 — TRUE — MAKE_BASE=TRUE
- NC_PCIE_5_R2D_CN — 17 — TRUE — MAKE_BASE=TRUE
- NC_PCIE_5_R2D_CP — 17 — TRUE — MAKE_BASE=TRUE
- NC_PCIE_6_D2RN — 17 — TRUE — MAKE_BASE=TRUE
- NC_PCIE_6_D2RP — 17 — TRUE — MAKE_BASE=TRUE
- NC_PCIE_6_R2D_CN — 17 — TRUE — MAKE_BASE=TRUE
- NC_PCIE_6_R2D_CP — 17 — TRUE — MAKE_BASE=TRUE
- NC_PCIE_7_D2RN — 17 — TRUE — MAKE_BASE=TRUE
- NC_PCIE_7_D2RP — 17 — TRUE — MAKE_BASE=TRUE
- NC_PCIE_7_R2D_CN — 17 — TRUE — MAKE_BASE=TRUE
- NC_PCIE_7_R2D_CP — 17 — TRUE — MAKE_BASE=TRUE
- NC_PCIE_8_D2RN — 17 — TRUE — MAKE_BASE=TRUE
- NC_PCIE_8_D2RP — 17 — TRUE — MAKE_BASE=TRUE
- NC_PCIE_8_R2D_CN — 17 — TRUE — MAKE_BASE=TRUE
- NC_PCIE_8_R2D_CP — 17 — TRUE — MAKE_BASE=TRUE

- TP_PCIE_CLK100M_PE4N — NC_PCIE_CLK100M_PE4N — 17 — TRUE — MAKE_BASE=TRUE
- TP_PCIE_CLK100M_PE4P — NC_PCIE_CLK100M_PE4P — 17 — TRUE — MAKE_BASE=TRUE
- TP_PCIE_CLK100M_PEBN — NC_PCIE_CLK100M_PEBN — 17 — TRUE — MAKE_BASE=TRUE
- TP_PCIE_CLK100M_PEBP — NC_PCIE_CLK100M_PEBP — 17 — TRUE — MAKE_BASE=TRUE

- TP_SATA_C_D2RN — NC_SATA_C_D2RN — 17 — TRUE — MAKE_BASE=TRUE
- TP_SATA_C_D2RP — NC_SATA_C_D2RP — 17 — TRUE — MAKE_BASE=TRUE
- TP_SATA_C_R2D_CN — NC_SATA_C_R2D_CN — 17 — TRUE — MAKE_BASE=TRUE
- TP_SATA_C_R2D_CP — NC_SATA_C_R2D_CP — 17 — TRUE — MAKE_BASE=TRUE
- TP_SATA_D_D2RN — NC_SATA_D_D2RN — 17 — TRUE — MAKE_BASE=TRUE
- TP_SATA_D_D2RP — NC_SATA_D_D2RP — 17 — TRUE — MAKE_BASE=TRUE
- TP_SATA_D_R2D_CN — NC_SATA_D_R2D_CN — 17 — TRUE — MAKE_BASE=TRUE
- TP_SATA_D_R2D_CP — NC_SATA_D_R2D_CP — 17 — TRUE — MAKE_BASE=TRUE
- TP_SATA_E_D2RN — NC_SATA_E_D2RN — 17 — TRUE — MAKE_BASE=TRUE
- TP_SATA_E_D2RP — NC_SATA_E_D2RP — 17 — TRUE — MAKE_BASE=TRUE
- TP_SATA_E_R2D_CN — NC_SATA_E_R2D_CN — 17 — TRUE — MAKE_BASE=TRUE
- TP_SATA_E_R2D_CP — NC_SATA_E_R2D_CP — 17 — TRUE — MAKE_BASE=TRUE
- TP_SATA_F_D2RN — NC_SATA_F_D2RN — 17 — TRUE — MAKE_BASE=TRUE
- TP_SATA_F_D2RP — NC_SATA_F_D2RP — 17 — TRUE — MAKE_BASE=TRUE
- TP_SATA_F_R2D_CN — NC_SATA_F_R2D_CN — 17 — TRUE — MAKE_BASE=TRUE
- TP_SATA_F_R2D_CP — NC_SATA_F_R2D_CP — 17 — TRUE — MAKE_BASE=TRUE

- TP_CRT_IG_BLUE — NC_CRT_IG_BLUE — 18 — TRUE — MAKE_BASE=TRUE
- TP_CRT_IG_GREEN — NC_CRT_IG_GREEN — 18 — TRUE — MAKE_BASE=TRUE
- TP_CRT_IG_RED — NC_CRT_IG_RED — 18 — TRUE — MAKE_BASE=TRUE
- TP_CRT_IG_DDC_CLK — NC_CRT_IG_DDC_CLK — 18 — TRUE — MAKE_BASE=TRUE
- TP_CRT_IG_DDC_DATA — NC_CRT_IG_DDC_DATA — 18 — TRUE — MAKE_BASE=TRUE
- TP_CRT_IG_HSYNC — NC_CRT_IG_HSYNC — 18 — TRUE — MAKE_BASE=TRUE
- TP_CRT_IG_VSYNC — NC_CRT_IG_VSYNC — 18 — TRUE — MAKE_BASE=TRUE
- TP_HDA_SDIN1 — NC_HDA_SDIN1 — 17 — TRUE — MAKE_BASE=TRUE
- TP_HDA_SDIN2 — NC_HDA_SDIN2 — 17 — TRUE — MAKE_BASE=TRUE
- TP_HDA_SDIN3 — NC_HDA_SDIN3 — 17 — TRUE — MAKE_BASE=TRUE

- TP_SDVO_TVCLKINN — NC_SDVO_TVCLKINN — 18 — TRUE — MAKE_BASE=TRUE
- TP_SDVO_TVCLKINP — NC_SDVO_TVCLKINP — 18 — TRUE — MAKE_BASE=TRUE
- TP_SDVO_STALLN — NC_SDVO_STALLN — 18 — TRUE — MAKE_BASE=TRUE
- TP_SDVO_STALLP — NC_SDVO_STALLP — 18 — TRUE — MAKE_BASE=TRUE
- TP_SDVO_INTN — NC_SDVO_INTN — 18 — TRUE — MAKE_BASE=TRUE
- TP_SDVO_INTP — NC_SDVO_INTP — 18 — TRUE — MAKE_BASE=TRUE

- TP_PCI_PME_L — NC_PCI_PME_L — 19 — TRUE — MAKE_BASE=TRUE
- TP_PCI_CLK33M_OUT3 — NC_PCI_CLK33M_OUT3 — 19 — TRUE — MAKE_BASE=TRUE

- NC_ISNS_LCDBKLTN — 80 — TRUE — MAKE_BASE=TRUE
- NC_ISNS_LCDBKLTP — 80 — TRUE — MAKE_BASE=TRUE
- NC_ISNS_WLANN — 80 — TRUE — MAKE_BASE=TRUE
- NC_ISNS_WLANP — 80 — TRUE — MAKE_BASE=TRUE
- NC_ISNS_LCD_PANELN — 67 80 — TRUE — MAKE_BASE=TRUE
- NC_ISNS_LCD_PANELP — 67 80 — TRUE — MAKE_BASE=TRUE

PCH ALIASES
- NC_LPC_DREQ0_L — TP_LPC_DREQ0_L — 7 17 — MAKE_BASE=TRUE — TRUE
- NC_LPC_DREQ1_L — TP_LPC_DREQ1_L — MAKE_BASE=TRUE — TRUE
- TP_CLINK_CLK — NC_CLINK_CLK — 17 — TRUE — MAKE_BASE=TRUE
- TP_CLINK_DATA — NC_CLINK_DATA — 17 — TRUE — MAKE_BASE=TRUE
- TP_CLINK_RESET_L — NC_CLINK_RESET_L — 17 — TRUE — MAKE_BASE=TRUE

SYNC_MASTER=MASTER SYNC_DATE=MASTER
PAGE TITLE: Functional / ICT Test

Apple Inc.

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REVISION: <E4LABEL>
BRANCH: <BRANCH>
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- PCIE_ENET_R2D_C_P — TRUE
- PCIE_ENET_R2D_C_N — TRUE

- PCIE_AP_R2D_C_P — TRUE
- PCIE_AP_R2D_C_N — TRUE
- PCIE_AP_D2R_P — TRUE
- PCIE_AP_D2R_N — TRUE

- PCIE_AP_D2R_PI_P — TRUE
- PCIE_AP_D2R_PI_N — TRUE
- PCIE_AP_R2D_PI_P — TRUE
- PCIE_AP_R2D_PI_N — TRUE

- PCIE_CLK100M_PCH_P — TRUE
- PCIE_CLK100M_PCH_N — TRUE
- PCIE_CLK100M_TBT_P — TRUE
- PCIE_CLK100M_TBT_N — TRUE

- PCH_CLK100M_SATA_P — TRUE
- PCH_CLK33M_PCIIN — TRUE

- PCIE_CLK100M_SSD_P — TRUE
- PCIE_CLK100M_SSD_N — TRUE
- PEG_CLK100M_P — TRUE
- PEG_CLK100M_N — TRUE
- PCIE_CLK100M_ENET_P — TRUE
- PCIE_CLK100M_ENET_N — TRUE
- PCIE_CLK100M_AP_P — TRUE
- PCIE_CLK100M_AP_N — TRUE
- PCIE_CLK100M_FW_P — TRUE
- PCIE_CLK100M_FW_N — TRUE
- PCIE_CLK100M_EXCARD_P — TRUE
- PCIE_CLK100M_EXCARD_N — TRUE

- SATA_HDD_R2D_RDRIN_P — TRUE
- SATA_HDD_R2D_RDRIN_N — TRUE
- SATA_HDD_D2R_RDROUT_P — TRUE
- SATA_HDD_D2R_RDROUT_N — TRUE
- SATA_HDD_D2R_RDRIN_P — TRUE
- SATA_HDD_D2R_RDRIN_N — TRUE
- SATA_HDD_R2D_RDROUT_P — TRUE
- SATA_HDD_R2D_RDROUT_N — TRUE
- SATA_HDD_D2R_RC_P — TRUE
- SATA_HDD_D2R_RC_N — TRUE
- SATA_HDD_R2D_RC_P — TRUE
- SATA_HDD_R2D_RC_N — TRUE

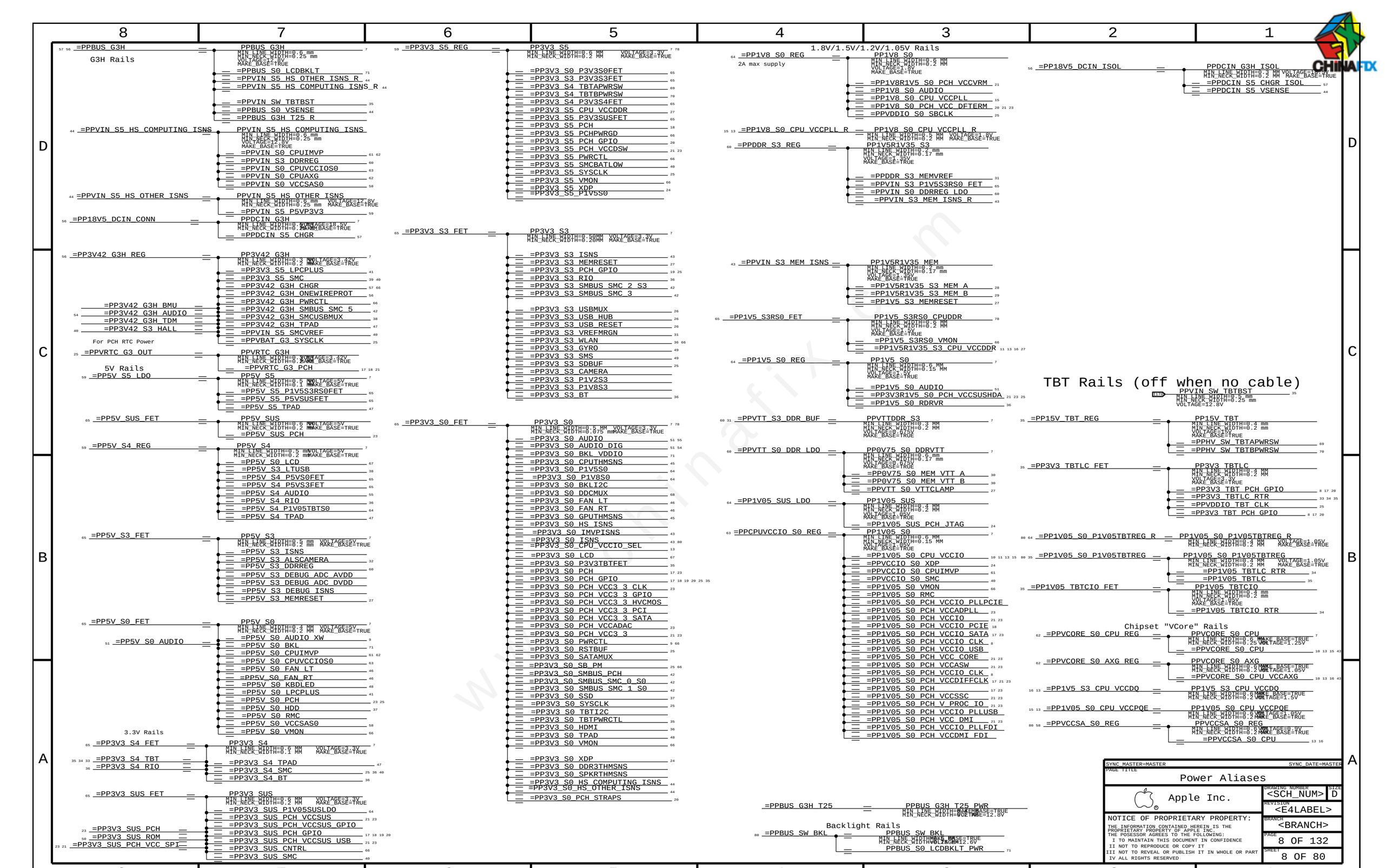
- SATA_HDD_R2D_C_P — TRUE
- SATA_HDD_R2D_C_N — TRUE
- SATA_HDD_D2R_P — TRUE
- SATA_HDD_D2R_N — TRUE

- SATA_SSDRHDD_D2R_P — TRUE
- SATA_SSDRHDD_D2R_N — TRUE
- SATA_SSDRHDD_R2D_P — TRUE
- SATA_SSDRHDD_R2D_N — TRUE

- USB3_EXTA_RX_F_P — TRUE
- USB3_EXTA_RX_F_N — TRUE
- USB3_EXTA_RX_P — TRUE
- USB3_EXTA_RX_N — TRUE

- USB3_EXTA_TX_C_P — TRUE
- USB3_EXTA_TX_C_N — TRUE
- USB3_EXTA_TX_N — TRUE
- USB3_EXTA_RX_N — TRUE

- USB3_EXTB_RX_RC_P — TRUE
- USB3_EXTB_RX_RC_N — TRUE
- USB3_EXTB_RX_P — TRUE
- USB3_EXTB_RX_N — TRUE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=PPVIN_S5_HS_OTHER_ISNS_R
=PPVIN_S5_HS_COMPUTING_ISNS_R
=PPVIN_SW_TBTBST
=PPBUS_S0_VSENSE
=PPBUS_G3H_T25_R
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=PPVIN_S0_CPUIMVP
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=PPVIN_S0_VCCSAS0
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=PPVIN_S5_P5VP3V3
=PP18V5_DCIN_CONN
PPDCIN_G3H
=PPDCIN_S5_CHGR
=PP3V42_G3H_REG
PP3V42_G3H
=PP3V3_S5_LPCPLUS
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=PP3V42_G3H_CHGR
=PP3V42_G3H_ONEWIREPROT
=PP3V42_G3H_PWRCTL
=PP3V42_G3H_SMBUS_SMC_5
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=PP3V42_G3H_TPAD
=PPVIN_S5_SMCVREF
=PPVBAT_G3_SYSCLK
=PP3V42_G3H_BMU
=PP3V42_G3H_AUDIO
=PP3V42_G3H_TDM
=PP3V42_S3_HALL
For PCH RTC Power
=PPVRTC_G3_OUT
PPVRTC_G3H
=PPVRTC_G3_PCH
5V Rails
=PP5V_S5_LDO
PP5V_S5
=PP5V_S5_P1V5S3RS0FET
=PP5V_S5_P5VSUSFET
=PP5V_S5_TPAD
=PP5V_SUS_FET
PP5V_SUS
=PP5V_SUS_PCH
=PP5V_S4_REG
PP5V_S4
=PP5V_S0_LCD
=PP5V_S3_LTUSB
=PP5V_S4_P5VS0FET
=PP5V_S4_P5VS3FET
=PP5V_S4_AUDIO
=PP5V_S4_RIO
=PP5V_S4_P1V05TBTS0
=PP5V_S4_TPAD
=PP5V_S3_FET
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=PP5V_S3_ALSCAMERA
=PP5V_S3_DDRREG
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=PP5V_S3_DEBUG_ADC_DVDD
=PP5V_S3_DEBUG_ISNS
=PP5V_S3_MEMRESET
=PP5V_S0_FET
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=PP5V_S0_FAN_LT
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=PP5V_S0_KBDLED
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=PP5V_S0_PCH
=PP5V_S0_HDD
=PP5V_S0_RMC
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3.3V Rails
=PP3V3_S4_FET
PP3V3_S4
=PP3V3_S4_TBT
=PP3V3_S4_RIO
=PP3V3_S4_TPAD
=PP3V3_S4_SMC
=PP3V3_S4_BT
=PP3V3_SUS_FET
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=PP3V3_SUS_P1V05SUSLDO
=PP3V3_SUS_PCH
=PP3V3_SUS_PCH_VCCSUS
=PP3V3_SUS_PCH_VCCSUS_GPIO
=PP3V3_SUS_ROM
=PP3V3_SUS_PCH_GPIO
=PP3V3_SUS_PCH_VCCSUS_USB
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=PP3V3_SUS_CNTRL
=PP3V3_SUS_SMC
=PP3V3_S5_REG
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=PP3V3_S3_P3V3S3FET
=PP3V3_S4_TBTAPWRSW
=PP3V3_S4_TBTBPWRSW
=PP3V3_S4_P3V3S4FET
=PP3V3_S5_CPU_VCCDDR
=PP3V3_S5_P3V3SUSFET
=PP3V3_S5_PCH
=PP3V3_S5_PCHPWRGD
=PP3V3_S5_PCH_GPIO
=PP3V3_S5_PCH_VCCDSW
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=PP3V3_S5_SYSCLK
=PP3V3_S5_VMON
=PP3V3_S5_XDP
=PP3V3_S5_P1V5S0
=PP3V3_S3_FET
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=PP3V3_S3_ISNS
=PP3V3_S3_MEMRESET
=PP3V3_S3_PCH_GPIO
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=PP3V3_S3_SMBUS_SMC_2_S3
=PP3V3_S3_SMBUS_SMC_3
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=PP3V3_S3_USB_HUB
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=PP3V3_S3_SDBUF
=PP3V3_S3_CAMERA
=PP3V3_S3_P1V2S3
=PP3V3_S3_P1V8S3
=PP3V3_S3_BT
=PP3V3_S0_FET
PP3V3_S0
=PP3V3_S0_AUDIO
=PP3V3_S0_AUDIO_DIG
=PP3V3_S0_BKL_VDDIO
=PP3V3_S0_CPUTHMSNS
=PP3V3_S0_P1V5S0
=PP3V3_S0_P1V8S0
=PP3V3_S0_BKLI2C
=PP3V3_S0_DDCMUX
=PP3V3_S0_FAN_LT
=PP3V3_S0_FAN_RT
=PP3V3_S0_GPUTHMSNS
=PP3V3_S0_HS_ISNS
=PP3V3_S0_IMVPISNS
=PP3V3_S0_ISNS
=PP3V3_S0_CPU_VCCIO_SEL
=PP3V3_S0_LCD
=PP3V3_S0_P3V3TBTFET
=PP3V3_S0_PCH
=PP3V3_S0_PCH_GPIO
=PP3V3_S0_PCH_VCC3_3_CLK
=PP3V3_S0_PCH_VCC3_3_GPIO
=PP3V3_S0_PCH_VCC3_3_HVCMOS
=PP3V3_S0_PCH_VCC3_3_PCI
=PP3V3_S0_PCH_VCC3_3_SATA
=PP3V3_S0_PCH_VCCADAC
=PP3V3_S0_PCH_VCC3_3
=PP3V3_S0_PWRCTL
=PP3V3_S0_RSTBUF
=PP3V3_S0_SATAMUX
=PP3V3_S0_SB_PM
=PP3V3_S0_SMBUS_PCH
=PP3V3_S0_SMBUS_SMC_0_S0
=PP3V3_S0_SMBUS_SMC_1_S0
=PP3V3_S0_SSD
=PP3V3_S0_SYSCLK
=PP3V3_S0_TBTI2C
=PP3V3_S0_TBTPWRCTL
=PP3V3_S0_HDMI
=PP3V3_S0_TPAD
=PP3V3_S0_VMON
=PP3V3_S0_XDP
=PP3V3_S0_DDR3THMSNS
=PP3V3_S0_SPKRTHMSNS
=PP3V3_S0_HS_COMPUTING_ISNS
=PP3V3_S0_HS_OTHER_ISNS
=PP3V3_S0_PCH_STRAPS
1.8V/1.5V/1.2V/1.05V Rails
=PP1V8_S0_REG
2A max supply
PP1V8_S0
=PP1V8R1V5_S0_PCH_VCCVRM
=PP1V8_S0_AUDIO
=PP1V8_S0_CPU_VCCPLL
=PP1V8_S0_PCH_VCC_DFTERM
=PPVDDIO_S0_SBCLK
=PP1V8_S0_CPU_VCCPLL_R
PP1V8_S0_CPU_VCCPLL_R
=PPDDR_S3_REG
PP1V5R1V35_S3
=PPDDR_S3_MEMVREF
=PPVIN_S3_P1V5S3RS0_FET
=PPVIN_S0_DDRREG_LDO
=PPVIN_S3_MEM_ISNS_R
=PPVIN_S3_MEM_ISNS
PP1V5R1V35_MEM
=PP1V5R1V35_S3_MEM_A
=PP1V5R1V35_S3_MEM_B
=PP1V5_S3_MEMRESET
=PP1V5_S3RS0_FET
PP1V5_S3RS0_CPUDDR
=PP1V5_S3RS0_VMON
=PP1V5R1V35_S3_CPU_VCCDDR
=PP1V5_S0_REG
PP1V5_S0
=PP1V5_S0_AUDIO
=PP3V3R1V5_S0_PCH_VCCSUSHDA
=PP1V5_S0_RDRVR
=PPVTT_S3_DDR_BUF
PPVTTDDR_S3
=PPVTT_S0_DDR_LDO
PP0V75_S0_DDRVTT
=PP0V75_S0_MEM_VTT_A
=PP0V75_S0_MEM_VTT_B
=PPVTT_S0_VTTCLAMP
=PP1V05_SUS_LDO
PP1V05_SUS
=PP1V05_SUS_PCH_JTAG
=PPCPUVCCIO_S0_REG
PP1V05_S0
=PP1V05_S0_CPU_VCCIO
=PPVCCIO_S0_XDP
=PPVCCIO_S0_CPUIMVP
=PPVCCIO_S0_SMC
=PP1V05_S0_VMON
=PP1V05_S0_RMC
=PP1V05_S0_PCH_VCCIO_PLLPCIE
=PP1V05_S0_PCH_VCCADPLL
=PP1V05_S0_PCH_VCCIO
=PP1V05_S0_PCH_VCCIO_PCIE
=PP1V05_S0_PCH_VCCIO_SATA
=PP1V05_S0_PCH_VCCIO_CLK
=PP1V05_S0_PCH_VCCIO_USB
=PP1V05_S0_PCH_VCC_CORE
=PP1V05_S0_PCH_VCCASW
=PP1V05_S0_PCH_VCCIO_CLK
=PP1V05_S0_PCH_VCCDIFFCLK
=PP1V05_S0_PCH
=PP1V05_S0_PCH_VCCSSC
=PP1V05_S0_PCH_V_PROC_IO
=PP1V05_S0_PCH_VCCIO_PLLUSB
=PP1V05_S0_PCH_VCC_DMI
=PP1V05_S0_PCH_VCCIO_PLLFDI
=PP1V05_S0_PCH_VCCDMI_FDI
=PPBUS_G3H_T25
PPBUS_G3H_T25_PWR
Backlight Rails
=PPBUS_SW_BKL
PPBUS_SW_BKL
PPBUS_S0_LCDBKLT_PWR
=PP18V5_DCIN_ISOL
PPDCIN_G3H_ISOL
=PPDCIN_S5_CHGR_ISOL
=PPDCIN_S5_VSENSE
TBT Rails (off when no cable)
PPVIN_SW_TBTBST
=PP15V_TBT_REG
PP15V_TBT
=PPHV_SW_TBTAPWRSW
=PPHV_SW_TBTBPWRSW
=PP3V3_TBTLC_FET
PP3V3_TBTLC
=PP3V3_TBT_PCH_GPIO
=PP3V3_TBTLC_RTR
=PPVDDIO_TBT_CLK
=PP3V3_TBT_PCH_GPIO
=PP1V05_S0_P1V05TBTREG_R
PP1V05_S0_P1V05TBTREG_R
=PP1V05_S0_P1V05TBTREG
PP1V05_S0_P1V05TBTREG
=PP1V05_TBTLC_RTR
=PP1V05_TBTLC
=PP1V05_TBTCIO_FET
PP1V05_TBTCIO
=PP1V05_TBTCIO_RTR
Chipset "VCore" Rails
=PPVCORE_S0_CPU_REG
PPVCORE_S0_CPU
=PPVCORE_S0_CPU
=PPVCORE_S0_AXG_REG
PPVCORE_S0_AXG
=PPVCORE_S0_CPU_VCCAXG
=PP1V5_S3_CPU_VCCDQ
PP1V5_S3_CPU_VCCDQ
=PP1V05_S0_CPU_VCCPQE
PP1V05_S0_CPU_VCCPQE
=PPVCCSA_S0_REG
PPVCCSA_S0_REG
=PPVCCSA_S0_CPU
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Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
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REVISION
<E4LABEL>
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Frame Holes

ZT0940
4P5R2P3-3P5B

ZT0960
4P5R2P3-3P5B

Bosses for limiting deflection

SH0910
2.8OD1.2ID-2.25H-SM-D1 APN:860-1557

SH0911
2.8OD1.2ID-2.25H-SM-D1

SH0912
2.8OD1.2ID-2.25H-SM-D1

SH0913
2.8OD1.2ID-2.25H-SM-D1

SH0950
SM
SHLD-D1-USB

SH0951
SM
SHLD-D1-MLB-T29

D1 THERMAL MODULE STANDOFF (860-1439)

SH0920
STDOFF-4.50D2.15H-SM

SH0921
STDOFF-4.50D2.15H-SM

SH0926
STDOFF-4.50D2.15H-SM

SH0927
STDOFF-4.50D2.15H-SM

D1 BMU MODULE STANDOFFS

SH0928
STDOFF-4.50D1.73H-SM
APN: 860-1490

SH0963
STDOFF-4.50D2.33H-SM

SH0963 is BMU standoff with flange. 860-1534

TH0900 for upper TBT can gnd slot

TH0903 for lower TBT can gnd slot

TH0904,5 for USB can gnd slot

FAN BOSSES (4X 860-1327)

SH0922
STDOFF-4.50D1.8H-SM

SH0923
STDOFF-4.50D1.8H-SM

SH0924
STDOFF-4.50D1.8H-SM

SH0925
STDOFF-4.50D1.8H-SM

D1 POGO PINS (870-2451)

SH0932
POGO-2.30D-5.5H-SM-LOW-FORCE

SH0933
POGO-2.30D-4.1H-SM-LOW-FORCE

SH0934
POGO-2.30D-5.5H-SM-LOW-FORCE

SH0935
POGO-2.30D-5.5H-SM-LOW-FORCE

SH0936
POGO-2.30D-5.5H-SM-LOW-FORCE

SH0937
POGO-2.30D-5.5H-SM-LOW-FORCE

D1 ELIPTICAL SLOT HOLES

ZT0930
TH-NSP
SL-3.9X2.3-4.2x2.6

ZT0920
TH-NSP
SL-2.8X1.8-3.1x2.1

ZT0931
TH-NSP
SL-3.9X2.3-4.2x2.6

TH0900
TH-NSP
SL-1.1X0.5-1.4x0.8

TH0903
TH-NSP
SL-1.1X0.5-1.4x0.8

TH0904
TH-NSP
SL-1.1X0.45-1.4x0.75

TH0905
TH-NSP
SL-1.1X0.45-1.4x0.75

APN:862-0118

APN:998-3975

MLB_RAMCFG3
MLB_RAMCFG2
MLB_RAMCFG1
MLB_RAMCFG0
RAMCFG0:L R0910 1K 5% 1/20W MF 201
RAMCFG1:L R0911 1K 5% 1/20W MF 201
RAMCFG2:L R0912 1K 5% 1/20W MF 201
RAMCFG3:L R0913 1K 5% 1/20W MF 201

GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

Digital Ground

=PP5V_S0_AUDIO_XW

XW0902 SM
PP5V_S0_AUDIO_AMP_L
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

XW0903 SM
PP5V_S0_AUDIO_AMP_R
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

eDP signals

DP_INT_AUX_C_P		TP_EDP_AUX_P
DP_INT_AUX_C_N		TP_EDP_AUX_N
DP_INT_ML_C_P<3..0>		TP_EDP_TX_P<3..0>
DP_INT_ML_C_N<3..0>		TP_EDP_TX_N<3..0>

LCD_BKLT_PWM		LVDS_IG_BKL_PWM
LCD_BKLT_EN		LVDS_IG_BKL_ON
LCD_PWR_EN		LVDS_IG_PANEL_PWR

CR SFF DG v1p0 Table 3-56 mapping for HDMI

HDMI_IG_CLK_C_P		TP_DP_IG_B_MLP<3>
HDMI_IG_CLK_C_N		TP_DP_IG_B_MLN<3>
HDMI_IG_DATA_C_P<2..0>		TP_DP_IG_B_MLP<0..2>
HDMI_IG_DATA_C_N<2..0>		TP_DP_IG_B_MLN<0..2>
HDMI_IG_DDC_CLK		DPA_IG_DDC_CLK
HDMI_IG_DDC_DATA		DPA_IG_DDC_DATA
HDMI_HPD		DPA_IG_HPD

DP_TBTSNK0_AUXCH_C_P		DPB_IG_AUX_CH_P
DP_TBTSNK0_AUXCH_C_N		DPB_IG_AUX_CH_N
DP_TBTSNK0_ML_C_P<3..0>		TP_DP_IG_C_MLP<3..0>
DP_TBTSNK0_ML_C_N<3..0>		TP_DP_IG_C_MLN<3..0>
DP_TBTSNK0_DDC_CLK		DPB_IG_DDC_CLK
DP_TBTSNK0_DDC_DATA		DPB_IG_DDC_DATA
DP_TBTSNK0_HPD		DPB_IG_HPD
DP_TBTSNK1_AUXCH_C_P		TP_DP_IG_D_AUXP
DP_TBTSNK1_AUXCH_C_N		TP_DP_IG_D_AUXN
DP_TBTSNK1_ML_C_P<3..0>		TP_DP_IG_D_MLP<3..0>
DP_TBTSNK1_ML_C_N<3..0>		TP_DP_IG_D_MLN<3..0>
DP_TBTSNK1_DDC_CLK		TP_DP_IG_D_CTRL_CLK
DP_TBTSNK1_DDC_DATA		TP_DP_IG_D_CTRL_DATA
DP_TBTSNK1_HPD		TP_DP_IG_D_HPD

NC_PCH_GPIO64_CLKOUTFLEX0		TP_PCH_GPIO64_CLKOUTFLEX0
NC_PCH_GPIO65_CLKOUTFLEX1		TP_PCH_GPIO65_CLKOUTFLEX1
NC_PCH_GPIO66_CLKOUTFLEX2		TP_PCH_GPIO66_CLKOUTFLEX2
NC_PCH_GPIO67_CLKOUTFLEX3		TP_PCH_GPIO67_CLKOUTFLEX3

CPU signals

MEMVTT_EN		=DDRVTT_EN

T29 Signals Through PEG

PCIE_TBT_D2R_P<3..0>		=PEG_D2R_P<11..8>
PCIE_TBT_D2R_N<3..0>		=PEG_D2R_N<11..8>
PCIE_TBT_R2D_C_P<3..0>		=PEG_R2D_C_P<11..8>
PCIE_TBT_R2D_C_N<3..0>		=PEG_R2D_C_N<11..8>

SD_PWR_EN_PCH		ENET_LOW_PWR_PCH
SD_PWR_EN		ENET_LOW_PWR
TP_FW_PWR_EN		FW_PWR_EN

Unused PEG signals

NC_PEG_D2RP<15..12>		=PEG_D2R_P<15..12>
NC_PEG_D2RN<15..12>		=PEG_D2R_N<15..12>
NC_PEG_R2D_CP<15..12>		=PEG_R2D_C_P<15..12>
NC_PEG_R2D_CN<15..12>		=PEG_R2D_C_N<15..12>

Unused GPU signals

NC_PEG_D2RP<7..0>		=PEG_D2R_P<7..0>
NC_PEG_D2RN<7..0>		=PEG_D2R_N<7..0>
NC_PEG_R2D_CP<7..0>		=PEG_R2D_C_P<7..0>
NC_PEG_R2D_CN<7..0>		=PEG_R2D_C_N<7..0>

NC_DPA_IG_AUX_CHP		DPA_IG_AUX_CH_P
NC_DPA_IG_AUX_CHN		DPA_IG_AUX_CH_N

NC_PEG_CLK100MN		PEG_CLK100M_N
NC_PEG_CLK100MP		PEG_CLK100M_P

UNUSED USB SIGNALS

NC_USB3_EXTC_TXP		USB3_EXTC_TX_P
NC_USB3_EXTC_TXN		USB3_EXTC_TX_N
NC_USB3_EXTC_RXP		USB3_EXTC_RX_P
NC_USB3_EXTC_RXN		USB3_EXTC_RX_N
NC_USB_EXTCP		USB_EXTC_P
NC_USB_EXTCN		USB_EXTC_N
NC_USB3_EXTD_TXP		USB3_EXTD_TX_P
NC_USB3_EXTD_TXN		USB3_EXTD_TX_N
NC_USB3_EXTD_RXP		USB3_EXTD_RX_P
NC_USB3_EXTD_RXN		USB3_EXTD_RX_N
NC_USB_EXTD_EHCIP		USB_EXTD_EHCI_P
NC_USB_EXTD_EHCIN		USB_EXTD_EHCI_N
NC_USB_4N		TP_USB_4N
NC_USB_4P		TP_USB_4P
NC_USB_SDN		TP_USB_SDN
NC_USB_SDP		TP_USB_SDP
NC_USB_WLANN		TP_USB_WLANN
NC_USB_WLANP		TP_USB_WLANP
NC_USB_BT_HSN		TP_USB_BT_HSN
NC_USB_BT_HSP		TP_USB_BT_HSP
NC_USB_12N		TP_USB_12N
NC_USB_12P		TP_USB_12P
NC_USB_13N		TP_USB_13N
NC_USB_13P		TP_USB_13P

USB SIGNALS

USB_BT_P		USBHUB_DN1_P
USB_BT_N		USBHUB_DN1_N
USB_TPAD_P		USBHUB_DN2_P
USB_TPAD_N		USBHUB_DN2_N
USB_SMC_P		USBHUB_DN3_P
USB_SMC_N		USBHUB_DN3_N
PU_USBHUB_DN4_P		USBHUB_DN4_P
PU_USBHUB_DN4_N		USBHUB_DN4_N

NC_CPU_THERMDN		CPU_THERMD_N
NC_CPU_THERMDP		CPU_THERMD_P
NC_LCD_FSS		LCD_FSS

NC_PCIE_CLK100M_SSDN		PCIE_CLK100M_SSD_N
NC_PCIE_CLK100M_SSDP		PCIE_CLK100M_SSD_P
NC_PCIE_CLK100M_FWN		PCIE_CLK100M_FW_N
NC_PCIE_CLK100M_FWP		PCIE_CLK100M_FW_P

NC_PCIE_FW_D2RN		PCIE_FW_D2R_N
NC_PCIE_FW_D2RP		PCIE_FW_D2R_P
NC_PCIE_FW_R2D_CN		PCIE_FW_R2D_C_N
NC_PCIE_FW_R2D_CP		PCIE_FW_R2D_C_P

Unused SATA ODD Signals

NC_SATA_ODD_D2RN		SATA_ODD_D2R_N
NC_SATA_ODD_D2RP		SATA_ODD_D2R_P
NC_SATA_ODD_R2D_CN		SATA_ODD_R2D_C_N
NC_SATA_ODD_R2D_CP		SATA_ODD_R2D_C_P

Unused Memory Signals

NC_MEM_A_CLKP<1>		MEM_A_CLK_P<1>
NC_MEM_A_CLKN<1>		MEM_A_CLK_N<1>
NC_MEM_B_CLKP<1>		MEM_B_CLK_P<1>
NC_MEM_B_CLKN<1>		MEM_B_CLK_N<1>

=PP3V3_S0_PWRCTL

R0991 10K 5% 1/20W MF 201

Unused PGOOD signal

CPUIMVP_AXG_PGOOD

TP_P1V5S3RS0_RAMP_DONE		P1V5S3RS0_RAMP_DONE
TP_DDRREG_PGOOD		DDRREG_PGOOD

SYNC_MASTER=D1_MLB_TEST	SYNC_DATE=01/27/2012
PAGE TITLE	Signal Aliases
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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	SHEET 9 OF 80

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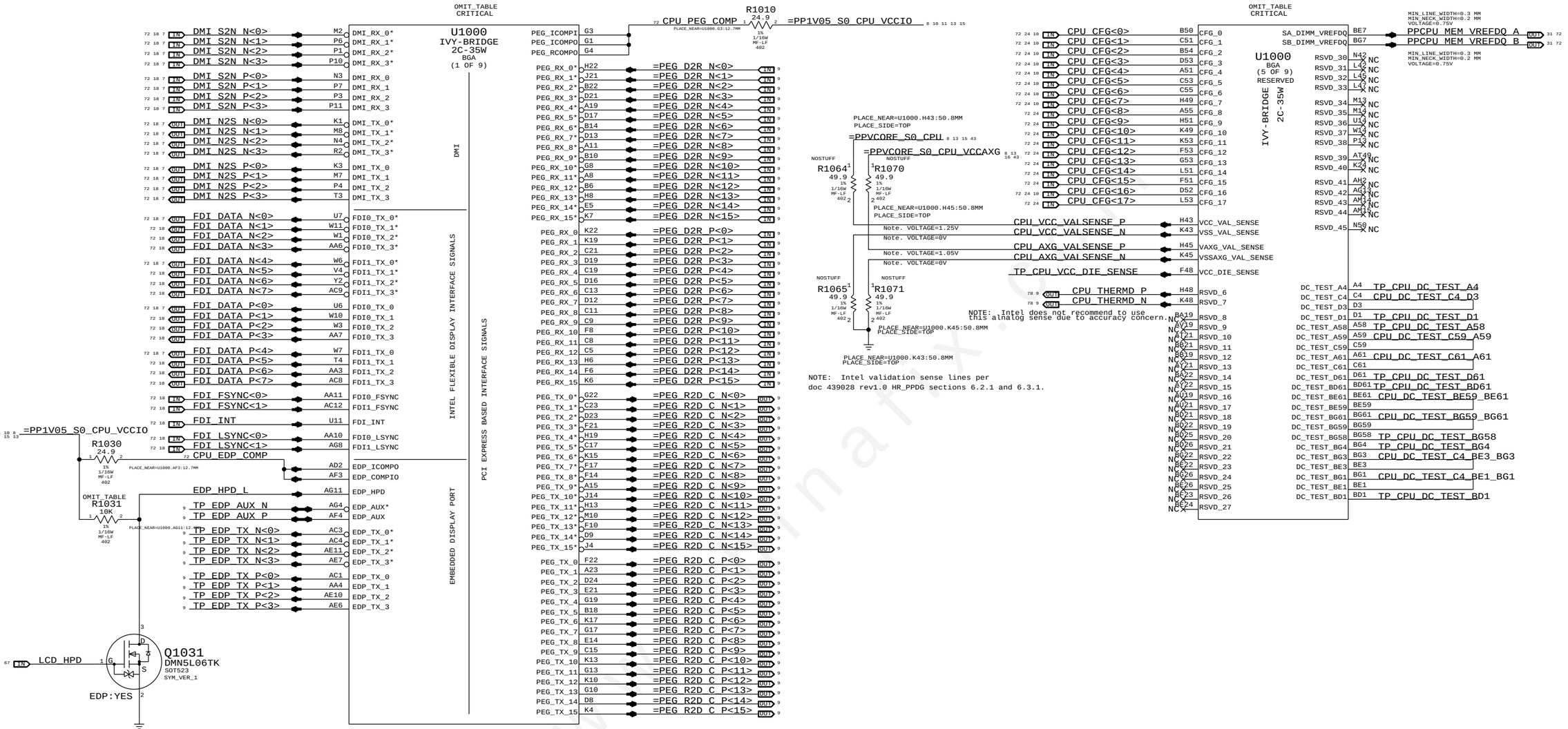
NOTE: Intel provides an internal pull-up OF 5-15k to VCCIO on all CFG signals.



FOR IVYBRIDGE PROCESSOR

CFG [7] :PEG DEFER TRAINING	1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB	0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION	11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD	00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0066	1	RES,MTL FILM,1/16W,1K,0402,SMD,LF	R1031		EDP:YES
116S0090	1	RES,MTL FILM,1/16W,10K,0402,SMD,LF	R1031		EDP:NO

Intel Doc 460452 ChiefRiver Platform design guild rev1.0 section 2.2.12 recommendation.

NOTE: eDP_COMPIO and eDP_ICOMPO can not be left floating
even if Internal Graphics is disabled since they are
shared with other interfaces.

NOTE: The EDP_HPD processor input is a low voltage active low signal.
Therefore, an inverting level shifter is required on the motherboard
to convert the active High signal from Embedded DisplayPort sink device
to low voltage signals for the processor
(refer to latest Processor EDS for DC Specifications).

If HPD is disabled while eDP interface is still enabled,
connect it to CPU VCCIO via a 10-kohm pull-up resistor on the motherboard.
This signal can be left as no-connect if entire eDP interface is disabled.

SYNC_MASTER=J30_MLB SYNC_DATE=07/14/2011

PAGE TITLE
CPU DMI/PEG/FDI/RSVD

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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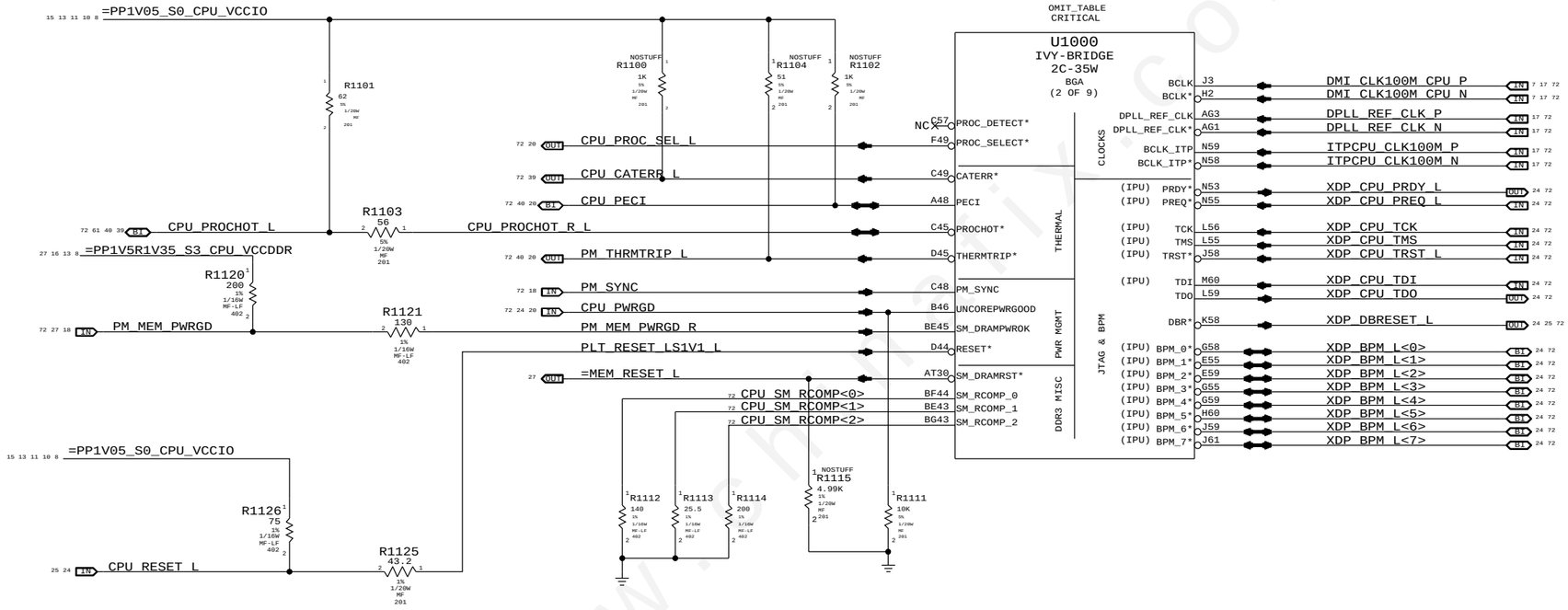

SYNC_MASTER=J30_MLB SYNC_DATE=07/14/2013

PAGE TITLE

CPU CLOCK/MISC/JTAG

Apple Inc.

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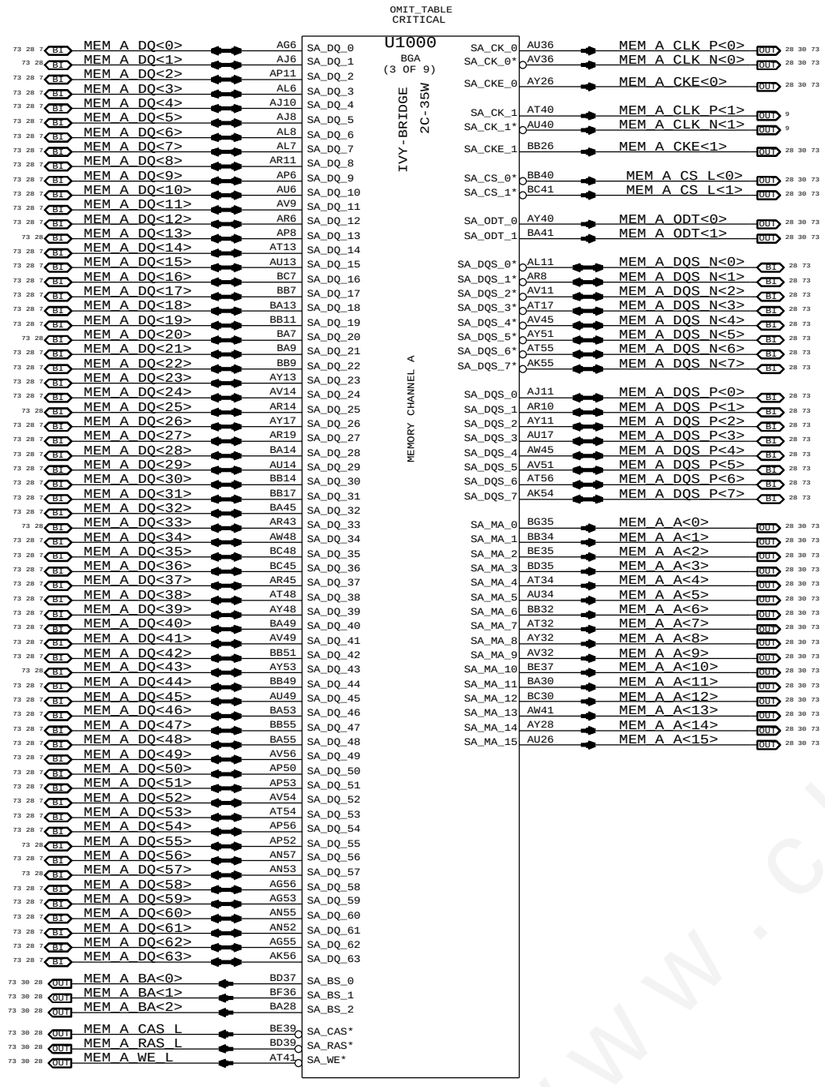

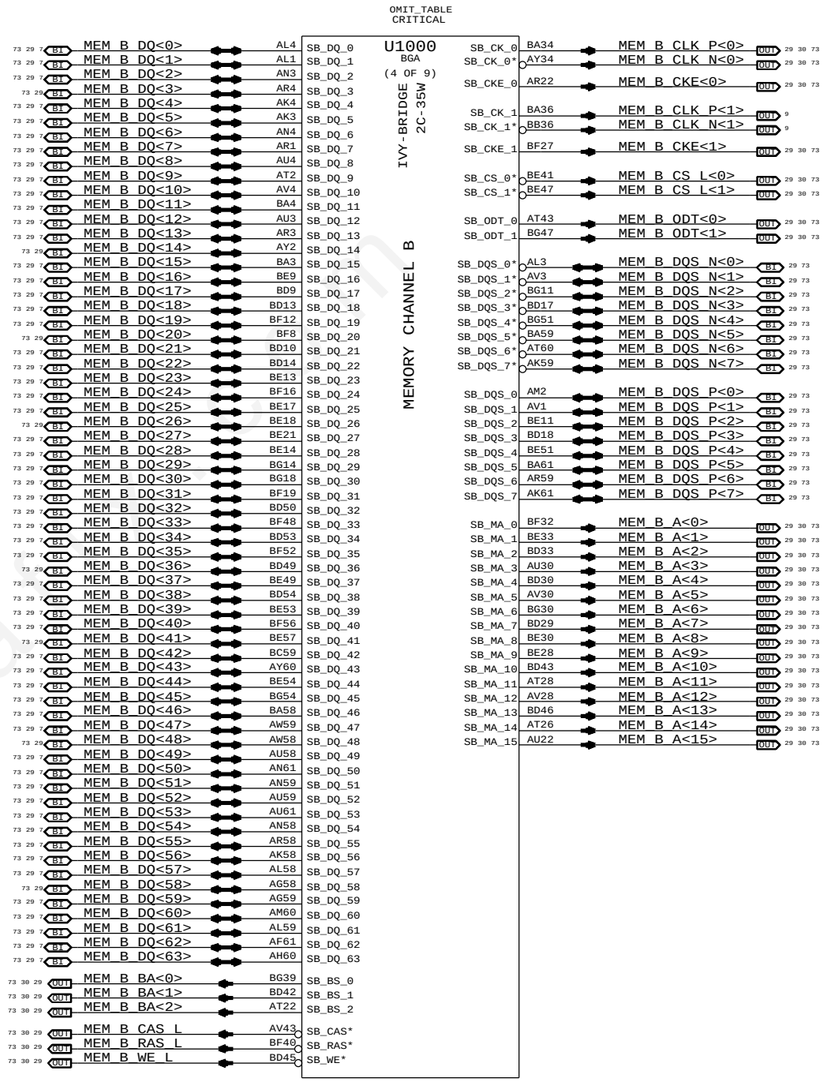

SYNC_MASTER=J30_MLB SYNC_DATE=07/14/2011

PAGE TITLE

CPU DDR3 INTERFACES

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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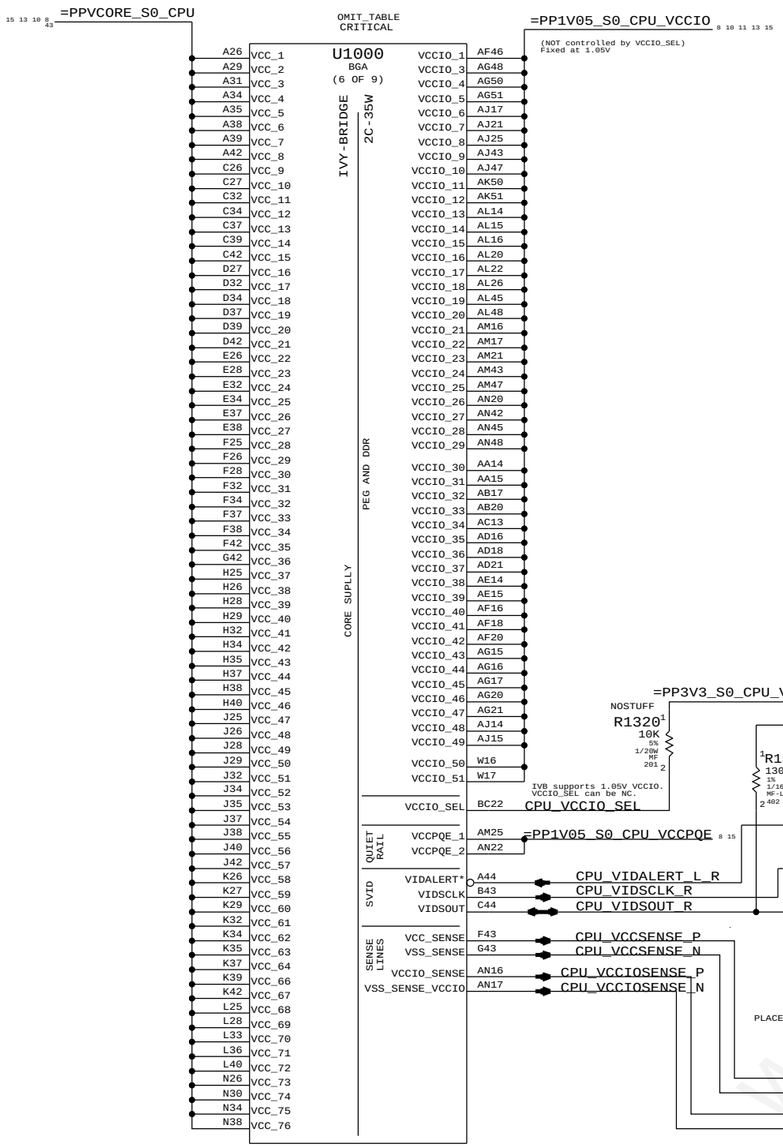

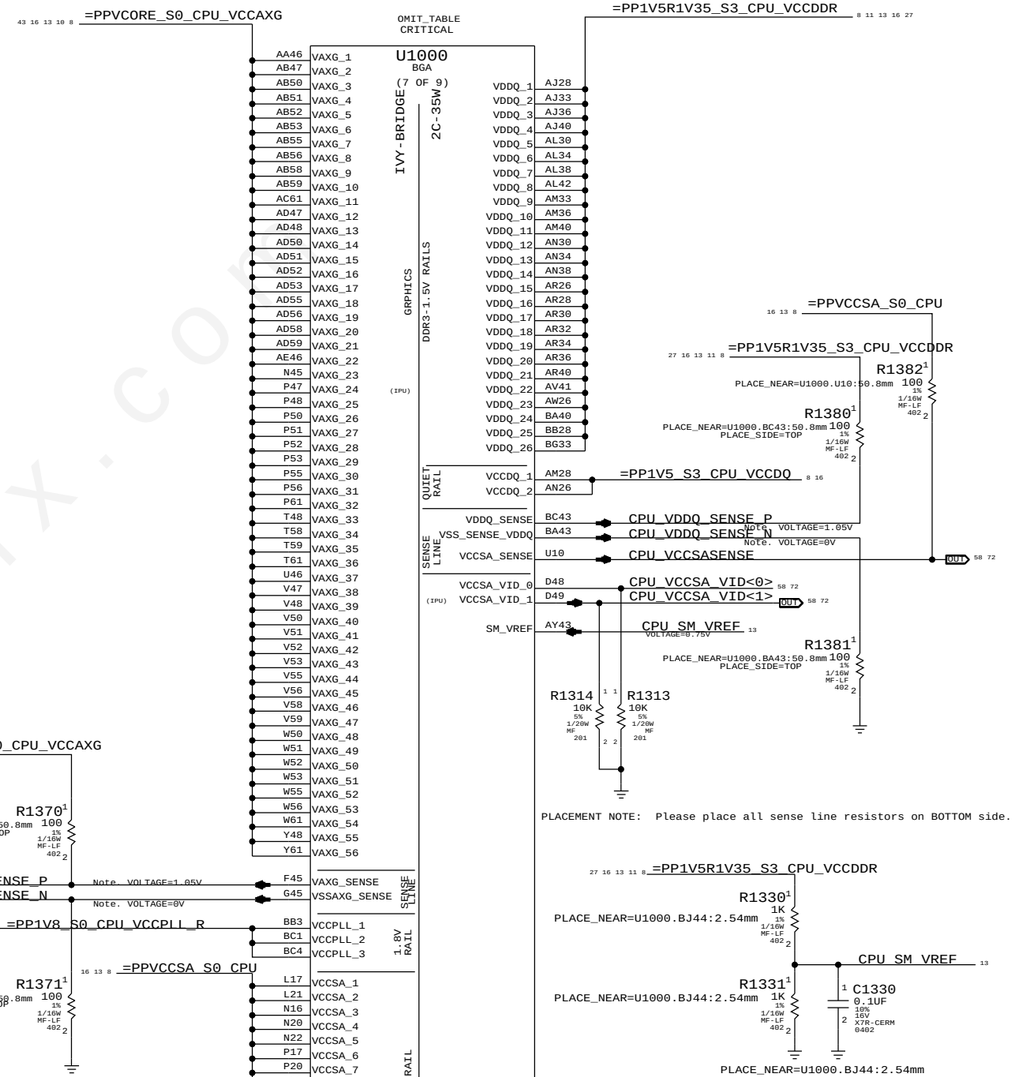

SYNC_MASTER=J30_MLB	SYNC_DATE=07/14/2013
PAGE TITLE	CPU POWER
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
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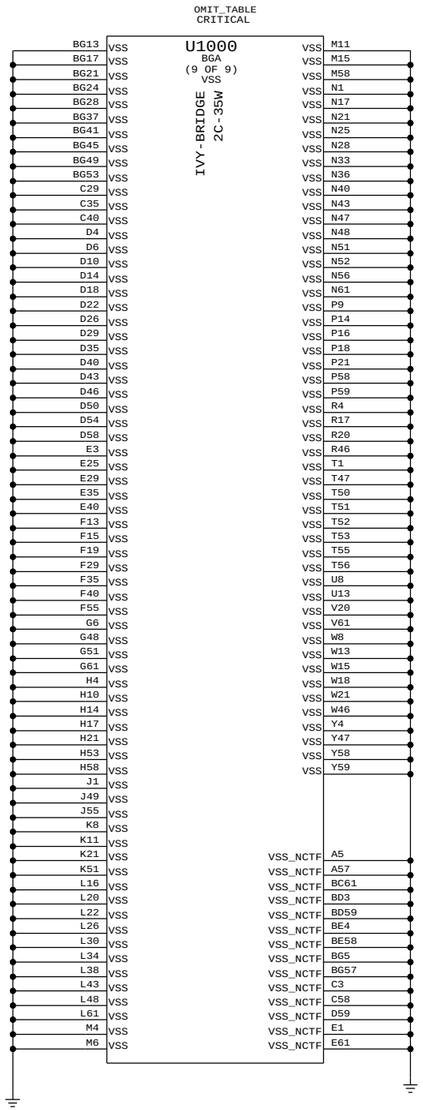

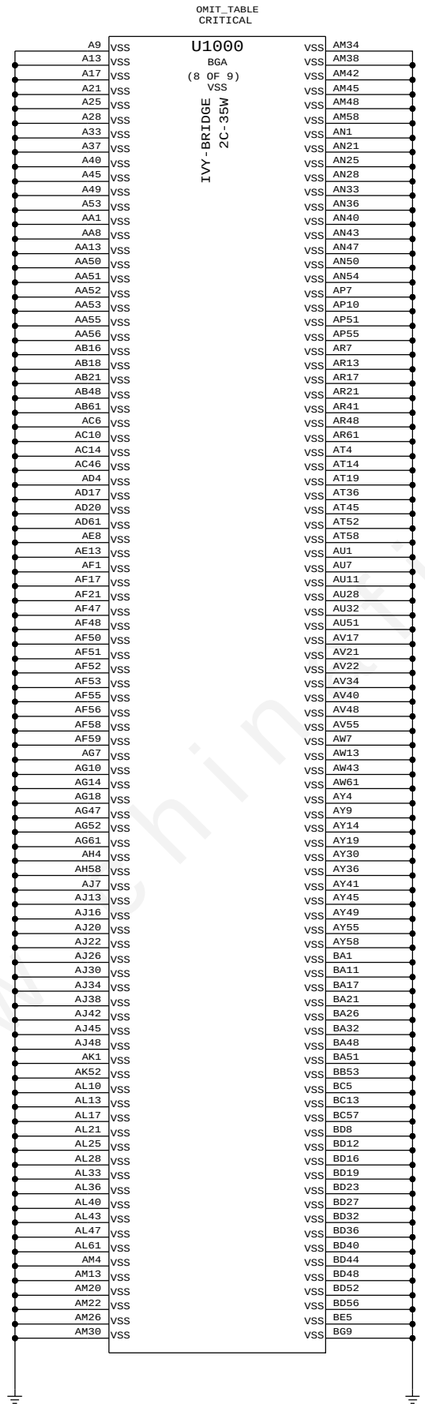

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PAGE TITLE

CPU GROUNDS

Apple Inc.

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All INTEL recommendations from Intel doc #458544 Chief River Platform Power Design Guide v0p9

CPU VCORE DECOUPLING

Intel recommendation (Table 7-2): Option 2: 35x 2.2uF, 12x 22uF, 4x 470uF, or Option 3: 35x 2.2uF, 6x 22uF, 6x 330 uF

43 13 10 8 =PPVCORE_S0_CPU

CRITICAL: C1600 C1604 C1606 C1607 C1608 C1609 C1610 C1612 C1613 C1615 C1617 C1623 C1624
CRITICAL: C1625 C1627 C1628 C1631 C1632 C1635 C1637 C1638 C1639 C1640 C1641 C1642 C1643 C1644 C1645 C1647 C1648
CRITICAL: C1650 C1651 C1652 C1653 C1654

PLACEMENT_NOTE (C1655-C1666):
Place close to U1000 on top side.

CRITICAL: C1646 C168F NO STUFF C16A0
CRITICAL: C1655 C1656 NO STUFF C1657 C1658 NO STUFF C1659 C1660 C1661 NO STUFF C1662 C1663 NO STUFF C1664 C1665 NO STUFF C1666 C166A C166B C166C NO STUFF C166D C166E C166F C165A C165B NO STUFF C1667 C1674

PLACEMENT_NOTE (C1667-C1679):
Place close to U1000 on bottom side.

CRITICAL: C16A1 C16A2 NO STUFF C16A3
CRITICAL: NO STUFF C1675 C1668 NO STUFF C1669 C1670 NO STUFF C1671 C1672 NO STUFF C1673 C1649 C164A C1676 NO STUFF C1677 C1678 NO STUFF C1679 C165C NO STUFF C165D C165E C165F NO STUFF C164E NO STUFF C164B C164C NO STUFF C164D C164F

PLACEMENT_NOTE (C1640-C1645):
Place near inductors on bottom side.

C1680 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM1
C1681 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM1
C1682 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM1
C1683 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM1
C168D 270UF 20% 2V TANT CASE-B2-SM
C168E 270UF 20% 2V TANT CASE-B2-SM

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Table 7-7): 26x 1uF, 10x 10uF, 2x 330uF

PLACEMENT_NOTE (C1684-C167F):
Place on bottom side of U1000

13 11 10 8 =PP1V05_S0_CPU_VCCIO

C1684 C1685 C1686 C1687 C1688 C1689 C1690 C1691 C1692 C1693 C1694 C1695 C1696
C1697 C1698 C1699 C169A C169B C169C C169D C169E C169F C161A C161B C161C C161D
1UF 10% 10V X5R-CERM 0402

PLACEMENT_NOTE (C1672-C1681):
Place near U1000 on bottom side

C161E C161F C162A C162B C162C C162D C162E C167A C167B C167C
10UF 20% 6.3V CERM-X5R 0402-1

C167D 270UF 20% 2V TANT CASE-B2-SM
C167E 270UF 20% 2V TANT CASE-B2-SM
C168A 270UF 20% 2V TANT CASE-B2-SM
C168B 270UF 20% 2V TANT CASE-B2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1601 0.010 1% 1/4W MF 0603
=PP1V05_S0_CPU_VCCPQE 8 13
C167F 1UF 10% 10V X5R 402

Note:The smallest 10mOhm available in the library are 0805s

CPU VCCPLL DECOUPLING

Intel recommendation (table 7-5): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):

8 =PP1V8_S0_CPU_VCCPLL
R1600 0 5% 1/16W MF-LF 402
=PP1V8_S0_CPU_VCCPLL_R 8 13
PLACE_NEAR=U1000.AK61:5mm PLACE_NEAR=U1000.AK61:5mm
PLACE_NEAR=U1000.AK63:2.54 mm:NO_VIA
PLACE_NEAR=U1000.AK65:2.54 mm:NO_VIA
C160X 1UF 10% 10V X5R 402
C160Y 1UF 10% 10V X5R 402
C160Z 270UF 20% 2V TANT CASE-B2-SM
C168C 270UF 20% 2V TANT CASE-B2-SM

CPU VCCPLL Low pass filter

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VAXG DECOUPLING

Intel recommendation (Table 7-4) for GT2 3.9mOhm LL: 11x 1uF, 6x 10uF, 6x 22uF, 2x 470uF

43 13 10 8 =PPVCORE_S0_CPU_VCCAXG

PLACEMENT_NOTE (C1700-C1710):

Place on bottom side of U1000

CRITICAL C1700 1UF 10% 10V X5R-CERM 0402
CRITICAL C1701 1UF 10% 10V X5R-CERM 0402
CRITICAL C1702 1UF 10% 10V X5R-CERM 0402
CRITICAL C1703 1UF 10% 10V X5R-CERM 0402
CRITICAL C1704 1UF 10% 10V X5R-CERM 0402
CRITICAL C1705 1UF 10% 10V X5R-CERM 0402
CRITICAL C1706 1UF 10% 10V X5R-CERM 0402
CRITICAL C1707 1UF 10% 10V X5R-CERM 0402
CRITICAL C1708 1UF 10% 10V X5R-CERM 0402
CRITICAL C1709 1UF 10% 10V X5R-CERM 0402
CRITICAL C1710 1UF 10% 10V X5R-CERM 0402

PLACEMENT_NOTE (C1711-C1716):

CRITICAL C1711 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1712 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1713 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1714 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1715 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1716 10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1717-C1722):

CRITICAL C1717 20UF 20% 2V X6T-CERM 0402
CRITICAL C1718 20UF 20% 2V X6T-CERM 0402
CRITICAL C1719 20UF 20% 2V X6T-CERM 0402
CRITICAL C1720 20UF 20% 2V X6T-CERM 0402
CRITICAL C1721 20UF 20% 2V X6T-CERM 0402
CRITICAL C1722 20UF 20% 2V X6T-CERM 0402
CRITICAL NO STUFF C1725 20UF 20% 2V X6T-CERM 0402
CRITICAL NO STUFF C1726 20UF 20% 2V X6T-CERM 0402
CRITICAL NO STUFF C1727 20UF 20% 2V X6T-CERM 0402
CRITICAL NO STUFF C1728 20UF 20% 2V X6T-CERM 0402
CRITICAL NO STUFF C1729 20UF 20% 2V X6T-CERM 0402
CRITICAL NO STUFF C172A 20UF 20% 2V X6T-CERM 0402

PLACEMENT_NOTE (C1723-C1724):

Place near inductors on bottom side.

C1723 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM1
C1724 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM1

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation (Table 7-11): 10x 1uF, 8x 10uF, 1x 330uF

27 13 11 8 =PP1V5R1V35_S3_CPU_VCCDDR

PLACEMENT_NOTE (C1738-C1747):

Place on bottom side of U1000

C1738 1UF 10% 10V X5R-CERM 0402
C1739 1UF 10% 10V X5R-CERM 0402
C1740 1UF 10% 10V X5R-CERM 0402
C1741 1UF 10% 10V X5R-CERM 0402
C1742 1UF 10% 10V X5R-CERM 0402
C1743 1UF 10% 10V X5R-CERM 0402
C1744 1UF 10% 10V X5R-CERM 0402
C1745 1UF 10% 10V X5R-CERM 0402
C1746 1UF 10% 10V X5R-CERM 0402
C1747 1UF 10% 10V X5R-CERM 0402

Place close to U1000 on bottom side

C1748 10UF 20% 6.3V CERM-X5R 0402-1
C1749 10UF 20% 6.3V CERM-X5R 0402-1
C1750 10UF 20% 6.3V CERM-X5R 0402-1
C1751 10UF 20% 6.3V CERM-X5R 0402-1
C1752 10UF 20% 6.3V CERM-X5R 0402-1
C1753 10UF 20% 6.3V CERM-X5R 0402-1
C1754 10UF 20% 6.3V CERM-X5R 0402-1
C1755 10UF 20% 6.3V CERM-X5R 0402-1

C1756 270UF 20% 2V TANT CASE-B2-SM
C1770 270UF 20% 2V TANT CASE-B2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1702 0.010 1% 1/4W MF 0603

=PP1V5_S3_CPU_VCCDQ 8 13

C1757 1UF 10% 10V X5R 402

CPU VCCSA DECOUPLING

Intel recommendation (Table 7-9): 5x 1uf, 5x 10uf, 1x 330uf

13 8 =PPVCCSA_S0_CPU

PLACEMENT_NOTE (C1758-C1762):

Place on bottom side of U1000

C1758 1UF 10% 10V X5R-CERM 0402
C1759 1UF 10% 10V X5R-CERM 0402
C1760 1UF 10% 10V X5R-CERM 0402
C1761 1UF 10% 10V X5R-CERM 0402
C1762 1UF 10% 10V X5R-CERM 0402

C1763 10UF 20% 6.3V CERM-X5R 0402-1
C1764 10UF 20% 6.3V CERM-X5R 0402-1
C1765 10UF 20% 6.3V CERM-X5R 0402-1
C1766 10UF 20% 6.3V CERM-X5R 0402-1
C1767 10UF 20% 6.3V CERM-X5R 0402-1

C1768 270UF 20% 2V TANT CASE-B2-SM
C1769 270UF 20% 2V TANT CASE-B2-SM

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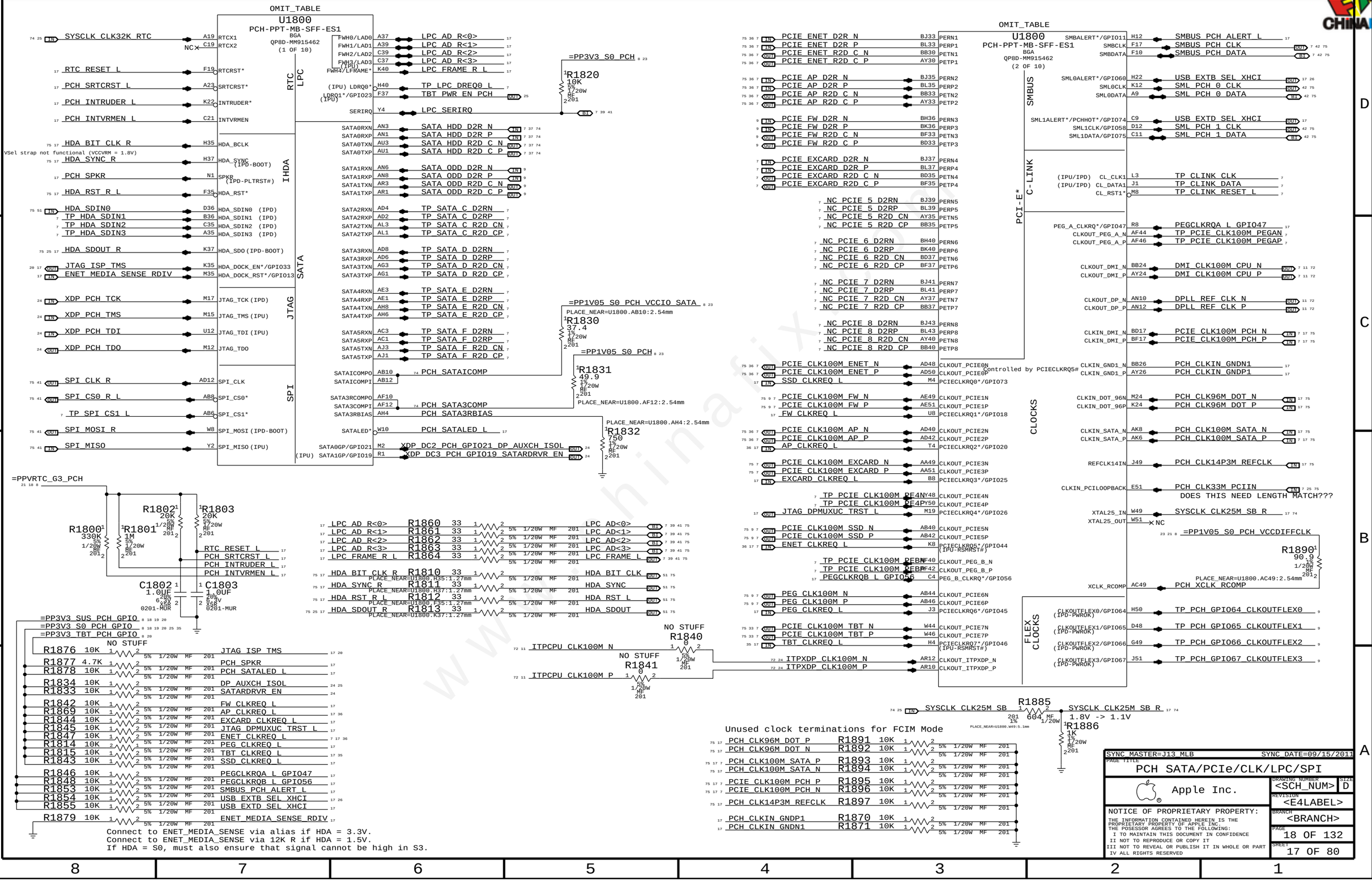
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U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(1 OF 10)
RTC
LPC
IHDA
SATA
JTAG
SPI
SYSCLK CLK32K RTC
RTC RESET L
PCH SRTCRST L
PCH INTRUDER L
PCH INTVRMEN L
HDA BIT CLK R
HDA SYNC R
PCH SPKR
HDA RST R L
HDA SDIN0
TP HDA SDIN1
TP HDA SDIN2
TP HDA SDIN3
HDA SDOUT R
JTAG ISP TMS
ENET MEDIA SENSE RDIV
XDP PCH TCK
XDP PCH TMS
XDP PCH TDI
XDP PCH TDO
SPI CLK R
SPI CS0 R L
TP SPI CS1 L
SPI MOSI R
SPI MISO
LPC AD R<0>
LPC AD R<1>
LPC AD R<2>
LPC AD R<3>
LPC FRAME R L
LPC SERIRQ
TP LPC DREQ0 L
TBT PWR EN PCH
SATA HDD D2R N
SATA HDD D2R P
SATA HDD R2D C N
SATA HDD R2D C P
SATA ODD D2R N
SATA ODD D2R P
SATA ODD R2D C N
SATA ODD R2D C P
TP SATA C D2RN
TP SATA C D2RP
TP SATA C R2D CN
TP SATA C R2D CP
TP SATA D D2RN
TP SATA D D2RP
TP SATA D R2D CN
TP SATA D R2D CP
TP SATA E D2RN
TP SATA E D2RP
TP SATA E R2D CN
TP SATA E R2D CP
TP SATA F D2RN
TP SATA F D2RP
TP SATA F R2D CN
TP SATA F R2D CP
PCH SATAICOMP
PCH SATA3COMP
PCH SATA3RBIAS
PCH SATALED L
XDP DC2 PCH GPIO21 DP AUXCH ISOL
XDP DC3 PCH GPIO19 SATARDRVR EN
=PP3V3 S0 PCH
=PP1V05 S0 PCH VCCIO SATA
=PP1V05 S0 PCH
PLACE_NEAR=U1800.AB10:2.54mm
PLACE_NEAR=U1800.AF12:2.54mm
PLACE_NEAR=U1800.AH4:2.54mm
R1820 10K
R1830 37.4
R1831 49.9
R1832 750
=PPVRTC_G3_PCH
R1800 330K
R1801 1M
R1802 20K
R1803 20K
C1802 1.0UF
C1803 1.0UF
RTC RESET L
PCH SRTCRST L
PCH INTRUDER L
PCH INTVRMEN L
LPC AD<0>
LPC AD<1>
LPC AD<2>
LPC AD<3>
LPC FRAME L
HDA BIT CLK
HDA SYNC
HDA RST L
HDA SDOUT
R1860 33
R1861 33
R1862 33
R1863 33
R1864 33
R1810 33
R1811 33
R1812 33
R1813 33
=PP3V3 SUS PCH GPIO
=PP3V3 S0 PCH GPIO
=PP3V3 TBT PCH GPIO
NO STUFF
R1876 10K JTAG ISP TMS
R1877 4.7K PCH SPKR
R1878 10K PCH SATALED L
R1834 10K DP AUXCH ISOL
R1833 10K SATARDRVR EN
R1842 10K FW CLKREQ L
R1869 10K AP CLKREQ L
R1844 10K EXCARD CLKREQ L
R1845 10K JTAG DPMUXUC TRST L
R1847 10K ENET CLKREQ L
R1814 10K PEG CLKREQ L
R1815 10K TBT CLKREQ L
R1843 10K SSD CLKREQ L
R1846 10K PEGCLKRQA L GPIO47
R1848 10K PEGCLKRQB L GPIO56
R1853 10K SMBUS PCH ALERT L
R1854 10K USB EXTB SEL XHCI
R1855 10K USB EXTD SEL XHCI
R1879 10K ENET MEDIA SENSE RDIV
Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.
ITPCPU CLK100M N
ITPCPU CLK100M P
NO STUFF
R1840 0
R1841 0
OMIT_TABLE
U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(2 OF 10)
PCI-E* C-LINK
SMBUS
CLOCKS
FLEX CLOCKS
PCIE ENET D2R N
PCIE ENET D2R P
PCIE ENET R2D C N
PCIE ENET R2D C P
PCIE AP D2R N
PCIE AP D2R P
PCIE AP R2D C N
PCIE AP R2D C P
PCIE FW D2R N
PCIE FW D2R P
PCIE FW R2D C N
PCIE FW R2D C P
PCIE EXCARD D2R N
PCIE EXCARD D2R P
PCIE EXCARD R2D C N
PCIE EXCARD R2D C P
NC PCIE 5 D2RN
NC PCIE 5 D2RP
NC PCIE 5 R2D CN
NC PCIE 5 R2D CP
NC PCIE 6 D2RN
NC PCIE 6 D2RP
NC PCIE 6 R2D CN
NC PCIE 6 R2D CP
NC PCIE 7 D2RN
NC PCIE 7 D2RP
NC PCIE 7 R2D CN
NC PCIE 7 R2D CP
NC PCIE 8 D2RN
NC PCIE 8 D2RP
NC PCIE 8 R2D CN
NC PCIE 8 R2D CP
PCIE CLK100M ENET N
PCIE CLK100M ENET P
SSD CLKREQ L
PCIE CLK100M FW N
PCIE CLK100M FW P
FW CLKREQ L
PCIE CLK100M AP N
PCIE CLK100M AP P
AP CLKREQ L
PCIE CLK100M EXCARD N
PCIE CLK100M EXCARD P
EXCARD CLKREQ L
TP PCIE CLK100M PE4N
TP PCIE CLK100M PE4P
JTAG DPMUXUC TRST L
PCIE CLK100M SSD N
PCIE CLK100M SSD P
ENET CLKREQ L
TP PCIE CLK100M PEBN
TP PCIE CLK100M PEBP
PEGCLKRQB L GPIO56
PEG CLK100M N
PEG CLK100M P
PEG CLKREQ L
PCIE CLK100M TBT N
PCIE CLK100M TBT P
TBT CLKREQ L
ITPXDP CLK100M N
ITPXDP CLK100M P
SMBALERT*/GPIO11
SMBCLK
SMBDATA
SML0ALERT*/GPIO60
SML0CLK
SML0DATA
SML1ALERT*/PCHHOT*/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
SMBUS PCH ALERT L
SMBUS PCH CLK
SMBUS PCH DATA
USB EXTB SEL XHCI
SML PCH 0 CLK
SML PCH 0 DATA
USB EXTD SEL XHCI
SML PCH 1 CLK
SML PCH 1 DATA
CL_CLK1
CL_DATA1
CL_RST1*
TP CLINK CLK
TP CLINK DATA
TP CLINK RESET L
PEG_A_CLKRQ*/GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
PEGCLKRQA L GPIO47
TP PCIE CLK100M PEGAN
TP PCIE CLK100M PEGAP
CLKOUT_DMI_N
CLKOUT_DMI_P
DMI CLK100M CPU N
DMI CLK100M CPU P
CLKOUT_DP_N
CLKOUT_DP_P
DPLL REF CLK N
DPLL REF CLK P
CLKIN_DMI_N
CLKIN_DMI_P
PCIE CLK100M PCH N
PCIE CLK100M PCH P
CLKIN_GND1_N
CLKIN_GND1_P
PCH CLKIN GNDN1
PCH CLKIN GNDP1
CLKIN_DOT_96N
CLKIN_DOT_96P
PCH CLK96M DOT N
PCH CLK96M DOT P
CLKIN_SATA_N
CLKIN_SATA_P
PCH CLK100M SATA N
PCH CLK100M SATA P
REFCLK14IN
PCH CLK14P3M REFCLK
CLKIN_PCILOOPBACK
PCH CLK33M PCIIN
DOES THIS NEED LENGTH MATCH???
XTAL25_IN
XTAL25_OUT
SYSCLK CLK25M SB R
=PP1V05 S0 PCH VCCDIFFCLK
R1890 90.9
PLACE_NEAR=U1800.AC49:2.54mm
XCLK_RCOMP
PCH XCLK RCOMP
CLKOUTFLEX0/GPIO64
CLKOUTFLEX1/GPIO65
CLKOUTFLEX2/GPIO66
CLKOUTFLEX3/GPIO67
TP PCH GPIO64 CLKOUTFLEX0
TP PCH GPIO65 CLKOUTFLEX1
TP PCH GPIO66 CLKOUTFLEX2
TP PCH GPIO67 CLKOUTFLEX3
Controlled by PCIECLKRQ5#
SYSCLK CLK25M SB
SYSCLK CLK25M SB R
R1885 604
1.8V -> 1.1V
R1886 1K
Unused clock terminations for FCIM Mode
PCH CLK96M DOT P R1891 10K
PCH CLK96M DOT N R1892 10K
PCH CLK100M SATA P R1893 10K
PCH CLK100M SATA N R1894 10K
PCIE CLK100M PCH P R1895 10K
PCIE CLK100M PCH N R1896 10K
PCH CLK14P3M REFCLK R1897 10K
PCH CLKIN GNDP1 R1870 10K
PCH CLKIN GNDN1 R1871 10K
SYNC_MASTER=J13_MLB
SYNC_DATE=09/15/2011
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Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
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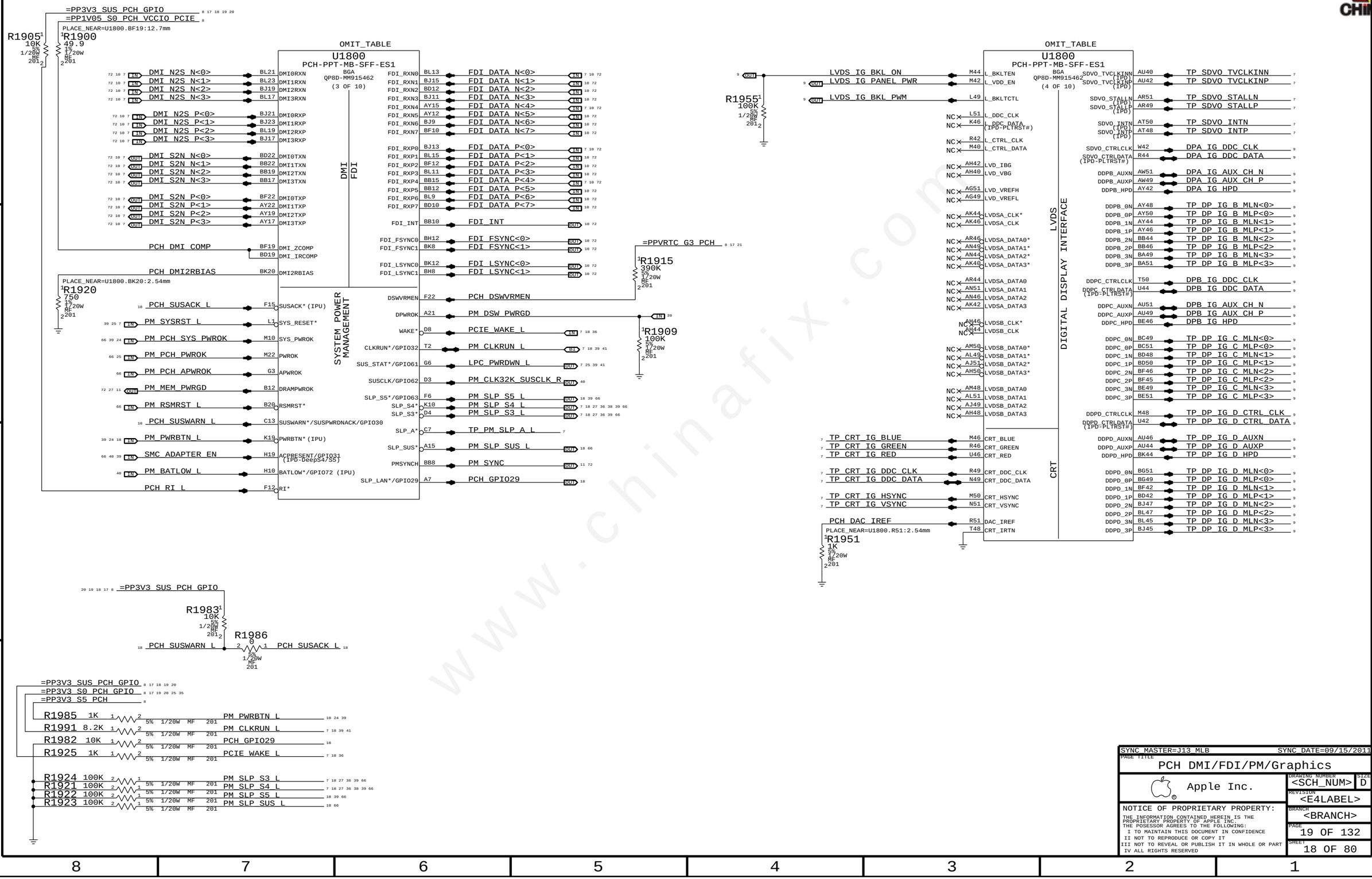
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R1905 10K 5% 1/20W MF 201
R1900 49.9 1% 1/20W MF 201
OMIT_TABLE
U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(3 OF 10)
DMI_N2S_N<0> BL21 DMI0RXN
DMI_N2S_N<1> BL23 DMI1RXN
DMI_N2S_N<2> BJ19 DMI2RXN
DMI_N2S_N<3> BL17 DMI3RXN
DMI_N2S_P<0> BJ21 DMI0RXP
DMI_N2S_P<1> BJ23 DMI1RXP
DMI_N2S_P<2> BL19 DMI2RXP
DMI_N2S_P<3> BJ17 DMI3RXP
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DMI_S2N_P<0> BF22 DMI0TXP
DMI_S2N_P<1> AY22 DMI1TXP
DMI_S2N_P<2> AY19 DMI2TXP
DMI_S2N_P<3> AY17 DMI3TXP
PCH_DMI_COMP BF19 DMI_ZCOMP
BD19 DMI_IRCOMP
PCH_DMI2RBIAS BK20 DMI2RBIAS
DMI
FDI
FDI_RXN0 BL13 FDI_DATA_N<0>
FDI_RXN1 BJ15 FDI_DATA_N<1>
FDI_RXN2 BD12 FDI_DATA_N<2>
FDI_RXN3 BJ11 FDI_DATA_N<3>
FDI_RXN4 AY15 FDI_DATA_N<4>
FDI_RXN5 AY12 FDI_DATA_N<5>
FDI_RXN6 BJ9 FDI_DATA_N<6>
FDI_RXN7 BF10 FDI_DATA_N<7>
FDI_RXP0 BJ13 FDI_DATA_P<0>
FDI_RXP1 BL15 FDI_DATA_P<1>
FDI_RXP2 BF12 FDI_DATA_P<2>
FDI_RXP3 BL11 FDI_DATA_P<3>
FDI_RXP4 BB15 FDI_DATA_P<4>
FDI_RXP5 BB12 FDI_DATA_P<5>
FDI_RXP6 BL9 FDI_DATA_P<6>
FDI_RXP7 BD10 FDI_DATA_P<7>
FDI_INT BB10 FDI_INT
FDI_FSYNC0 BH12 FDI_FSYNC<0>
FDI_FSYNC1 BK8 FDI_FSYNC<1>
FDI_LSYNC0 BK12 FDI_LSYNC<0>
FDI_LSYNC1 BH8 FDI_LSYNC<1>
SYSTEM POWER MANAGEMENT
DSWVRMEN F22 PCH_DSWVRMEN
DPWROK A21 PM_DSW_PWRGD
WAKE* D8 PCIE_WAKE_L
CLKRUN*/GPIO32 T2 PM_CLKRUN_L
SUS_STAT*/GPIO61 G6 LPC_PWRDWN_L
SUSCLK/GPIO62 D3 PM_CLK32K_SUSCLK_R
SLP_S5*/GPIO63 F6 PM_SLP_S5_L
SLP_S4* K10 PM_SLP_S4_L
SLP_S3* D4 PM_SLP_S3_L
SLP_A* C7 TP_PM_SLP_A_L
SLP_SUS* A15 PM_SLP_SUS_L
PMSYNCH BB8 PM_SYNC
SLP_LAN*/GPIO29 A7 PCH_GPIO29
=PPVRTC_G3_PCH
R1915 390K 5% 1/20W MF 201
R1909 100K 5% 1/20W MF 201
PLACE_NEAR=U1800.BK20:2.54mm
R1920 750 1% 1/20W MF 201
PCH_SUSACK_L F15 SUSACK*(IPU)
PM_SYSRST_L L1 SYS_RESET*
PM_PCH_SYS_PWROK M10 SYS_PWROK
PM_PCH_PWROK M22 PWROK
PM_PCH_APWROK G3 APWROK
PM_MEM_PWRGD B12 DRAMPWROK
PM_RSMRST_L B20 RSMRST*
PCH_SUSWARN_L C13 SUSWARN*/SUSPWRDNACK/GPIO30
PM_PWRBTN_L K19 PWRBTN*(IPU)
SMC_ADAPTER_EN H19 ACPRESENT/GPIO31 (IPD-DeepS4/S5)
PM_BATLOW_L H10 BATLOW*/GPIO72 (IPU)
PCH_RI_L F12 RI*
OMIT_TABLE
U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(4 OF 10)
LVDS_IG_BKL_ON M44 L_BKLTEN
LVDS_IG_PANEL_PWR M42 L_VDD_EN
LVDS_IG_BKL_PWM L49 L_BKLTCTL
R1955 100K 5% 1/20W MF 201
L51 L_DDC_CLK
K46 L_DDC_DATA (IPD-PLTRST#)
R42 L_CTRL_CLK
M40 L_CTRL_DATA
AH42 LVD_IBG
AH40 LVD_VBG
AG51 LVD_VREFH
AG49 LVD_VREFL
AK44 LVDSA_CLK*
AK46 LVDSA_CLK
AR46 LVDSA_DATA0*
AN49 LVDSA_DATA1*
AN44 LVDSA_DATA2*
AK40 LVDSA_DATA3*
AR44 LVDSA_DATA0
AN51 LVDSA_DATA1
AN46 LVDSA_DATA2
AK42 LVDSA_DATA3
AH46 LVDSB_CLK*
AH44 LVDSB_CLK
AM50 LVDSB_DATA0*
AL49 LVDSB_DATA1*
AJ51 LVDSB_DATA2*
AH50 LVDSB_DATA3*
AM48 LVDSB_DATA0
AL51 LVDSB_DATA1
AJ49 LVDSB_DATA2
AH48 LVDSB_DATA3
LVDS
DIGITAL DISPLAY INTERFACE
TP_CRT_IG_BLUE M46 CRT_BLUE
TP_CRT_IG_GREEN R46 CRT_GREEN
TP_CRT_IG_RED U46 CRT_RED
TP_CRT_IG_DDC_CLK R49 CRT_DDC_CLK
TP_CRT_IG_DDC_DATA N49 CRT_DDC_DATA
TP_CRT_IG_HSYNC M50 CRT_HSYNC
TP_CRT_IG_VSYNC N51 CRT_VSYNC
PCH_DAC_IREF R51 DAC_IREF
T48 CRT_IRTN
PLACE_NEAR=U1800.R51:2.54mm
R1951 1K 5% 1/20W MF 201
CRT
SDVO_TVCLKINN (IPD) AU40 TP_SDVO_TVCLKINN
SDVO_TVCLKINP (IPD) AU42 TP_SDVO_TVCLKINP
SDVO_STALLN (IPD) AR51 TP_SDVO_STALLN
SDVO_STALLP (IPD) AR49 TP_SDVO_STALLP
SDVO_INTN (IPD) AT50 TP_SDVO_INTN
SDVO_INTP (IPD) AT48 TP_SDVO_INTP
SDVO_CTRLCLK W42 DPA_IG_DDC_CLK
SDVO_CTRLDATA (IPD-PLTRST#) R44 DPA_IG_DDC_DATA
DDPB_AUXN AW51 DPA_IG_AUX_CH_N
DDPB_AUXP AW49 DPA_IG_AUX_CH_P
DDPB_HPD AY42 DPA_IG_HPD
DDPB_0N AY48 TP_DP_IG_B_MLN<0>
DDPB_0P AY50 TP_DP_IG_B_MLP<0>
DDPB_1N AY44 TP_DP_IG_B_MLN<1>
DDPB_1P AY46 TP_DP_IG_B_MLP<1>
DDPB_2N BB44 TP_DP_IG_B_MLN<2>
DDPB_2P BB46 TP_DP_IG_B_MLP<2>
DDPB_3N BA49 TP_DP_IG_B_MLN<3>
DDPB_3P BA51 TP_DP_IG_B_MLP<3>
DDPC_CTRLCLK T50 DPB_IG_DDC_CLK
DDPC_CTRLDATA (IPD-PLTRST#) U44 DPB_IG_DDC_DATA
DDPC_AUXN AU51 DPB_IG_AUX_CH_N
DDPC_AUXP AU49 DPB_IG_AUX_CH_P
DDPC_HPD BE46 DPB_IG_HPD
DDPC_0N BC49 TP_DP_IG_C_MLN<0>
DDPC_0P BC51 TP_DP_IG_C_MLP<0>
DDPC_1N BD48 TP_DP_IG_C_MLN<1>
DDPC_1P BD50 TP_DP_IG_C_MLP<1>
DDPC_2N BF46 TP_DP_IG_C_MLN<2>
DDPC_2P BF45 TP_DP_IG_C_MLP<2>
DDPC_3N BE49 TP_DP_IG_C_MLN<3>
DDPC_3P BE51 TP_DP_IG_C_MLP<3>
DDPD_CTRLCLK M48 TP_DP_IG_D_CTRL_CLK
DDPD_CTRLDATA (IPD-PLTRST#) U42 TP_DP_IG_D_CTRL_DATA
DDPD_AUXN AU46 TP_DP_IG_D_AUXN
DDPD_AUXP AU44 TP_DP_IG_D_AUXP
DDPD_HPD BK44 TP_DP_IG_D_HPD
DDPD_0N BG51 TP_DP_IG_D_MLN<0>
DDPD_0P BG49 TP_DP_IG_D_MLP<0>
DDPD_1N BF42 TP_DP_IG_D_MLN<1>
DDPD_1P BD42 TP_DP_IG_D_MLP<1>
DDPD_2N BJ47 TP_DP_IG_D_MLN<2>
DDPD_2P BL47 TP_DP_IG_D_MLP<2>
DDPD_3N BL45 TP_DP_IG_D_MLN<3>
DDPD_3P BJ45 TP_DP_IG_D_MLP<3>
=PP3V3_SUS_PCH_GPIO
R1983 10K 5% 1/20W MF 201
R1986 0 5% 1/20W MF 201
PCH_SUSWARN_L
PCH_SUSACK_L
=PP3V3_SUS_PCH_GPIO
=PP3V3_S0_PCH_GPIO
=PP3V3_S5_PCH
R1985 1K 5% 1/20W MF 201 PM_PWRBTN_L
R1991 8.2K 5% 1/20W MF 201 PM_CLKRUN_L
R1982 10K 5% 1/20W MF 201 PCH_GPIO29
R1925 1K 5% 1/20W MF 201 PCIE_WAKE_L
R1924 100K 5% 1/20W MF 201 PM_SLP_S3_L
R1921 100K 5% 1/20W MF 201 PM_SLP_S4_L
R1922 100K 5% 1/20W MF 201 PM_SLP_S5_L
R1923 100K 5% 1/20W MF 201 PM_SLP_SUS_L
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PAGE TITLE
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OMIT_TABLE

U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
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NC BH24 TP1
NC BK24 TP2
NC BH20 TP3
NC BK16 TP4
NC BH16 TP5
NC AN42 TP6
NC AN40 TP7
NC AR40 TP8
NC AR42 TP9
NC D20 TP10
NC M30 TP11
NC E3 TP12
NC AM4 TP13
NC AT4 TP14
NC AT2 TP15
NC AD10 TP16
NC B24 TP17
NC D24 TP18
NC AD44 TP19
NC AD46 TP20
NC BJ48 TP21
NC BL7 TP22
7 TP_PCH_TP23 W40 TP23
NC K30 TP24
NC BH49 TP41
NC BB42 TP42

AU6 NC
AU8 NC
AW1 NC
AW3 NC
AY2 NC
AY4 NC
AY6 NC
AY8 NC
BA1 NC
BA3 NC
BB6 NC
BC1 NC
RSVD BC3 NC
BD2 NC
BD4 NC
BE1 NC
BE3 NC
BE6 NC
BF6 NC
BF7 NC
BG1 NC
BG3 NC
BH3 NC
BH4 NC
BJ4 NC
BJ5 NC
BJ7 NC
BK6 NC
BL5 NC

USB

74 38 7 IN USB3_EXTA_RX_N BJ25 USB3RN1
9 IN USB3_EXTC_RX_N BJ27 USB3RN2
74 36 7 IN USB3_EXTB_RX_N BJ31 USB3RN3
9 IN USB3_EXTD_RX_N BJ29 USB3RN4

74 38 7 IN USB3_EXTA_RX_P BL25 USB3RP1
9 IN USB3_EXTC_RX_P BL27 USB3RP2
74 36 7 IN USB3_EXTB_RX_P BL31 USB3RP3
9 IN USB3_EXTD_RX_P BL29 USB3RP4

74 38 7 OUT USB3_EXTA_TX_N BF26 USB3TN1
9 OUT USB3_EXTC_TX_N BB28 USB3TN2
74 36 OUT USB3_EXTB_TX_N BF28 USB3TN3
9 OUT USB3_EXTD_TX_N BF30 USB3TN4

74 38 OUT USB3_EXTA_TX_P BD26 USB3TP1
9 OUT USB3_EXTC_TX_P AY28 USB3TP2
74 36 OUT USB3_EXTB_TX_P BD28 USB3TP3
9 OUT USB3_EXTD_TX_P BD30 USB3TP4

USBP0N F24 USB_EXTA_N B1 38 74
USBP0P H24 USB_EXTA_P B1 38 74
Ext A (XHCI/EHCI)

USBP1N C25 USB_EXTC_N B1 9
USBP1P A25 USB_EXTC_P B1 9
Ext C (XHCI/EHCI)

USBP2N C27 USB_EXTB_XHCI_N B1 26 74
USBP2P A27 USB_EXTB_XHCI_P B1 26 74
Ext B (XHCI)

USBP3N H28 USB_EXTD_XHCI_N B1 26 74
USBP3P F28 USB_EXTD_XHCI_P B1 26 74
Ext D (XHCI) (Mobiles: Trackpad)

USBP4N M26 TP_USB_4N 9
USBP4P K26 TP_USB_4P 9
Unused

USBP5N D28 TP_USB_SDN 9
USBP5P B28 TP_USB_SDP 9
RSVD: SD

USBP6N H26 TP_USB_WLANN 9
USBP6P F26 TP_USB_WLANP 9
RSVD: WiFi

USBP7N D32 USB_HUB_UP_N B1 26 74
USBP7P B32 USB_HUB_UP_P B1 26 74
USB Hub (All LS/FS Devices)

USBP8N M28 USB_CAMERA_N B1 32 74
USBP8P K28 USB_CAMERA_P B1 32 74
Camera

USBP9N C29 USB_EXTB_EHCI_N B1 26 74
USBP9P A29 USB_EXTB_EHCI_P B1 26 74
Ext B (EHCI)

USBP10N C31 USB_EXTD_EHCI_N B1 9
USBP10P A31 USB_EXTD_EHCI_P B1 9
Ext D (EHCI)

USBP11N H33 TP_USB_BT_HSN 9
USBP11P F33 TP_USB_BT_HSP 9
RSVD: BT (HS)

USBP12N H30 TP_USB_12N 9
USBP12P F30 TP_USB_12P 9
Unused

USBP13N M33 TP_USB_13N 9
USBP13P K33 TP_USB_13P 9
Unused

(IPD)

USBRBIAS* C33 74 PCH_USB_RBIAS
USBRBIAS A33

PLACE_NEAR=U1800.A33:2.54mm
1 R2070 22.6 1% 1/20W MF 201 2

OC0*/GPIO59 C17 XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L IN 19 24
OC1*/GPIO40 A17 XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L IN 19 24
OC2*/GPIO41 A13 XDP_DA2_PCH_GPIO41_USB_EXTC_OC_L IN 19 24
OC3*/GPIO42 D16 XDP_DA3_PCH_GPIO42_USB_EXTD_OC_L IN 19 24
OC4*/GPIO43 A11 XDP_DB0_PCH_GPIO43_USB_EXTB_OC_EHCI_L IN 24
OC5*/GPIO9 B16 XDP_DB1_PCH_GPIO9_USB_EXTD_OC_EHCI_L IN 24
OC6*/GPIO10 C23 XDP_DB2_PCH_GPIO10_AP_PWR_EN OUT 24
OC7*/GPIO14 H15 XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE IN 19 24

PCI

19 OUT JTAG_GMUX_TMS G46 REQ1*/GPIO50
19 OUT BLC_I2C_MUX_SEL K44 REQ2*/GPIO52
19 OUT USE_HDD_OOB_L F46 REQ3*/GPIO54

7 TP_PCH_STRP_BBS1 F42 GNT1*/GPIO51
7 TP_PCH_STRP_ESI_L H42 GNT2*/GPIO53
PCH_STRP_TOPBLK_SWP_L D44 GNT3*/GPIO55
(IPU-PCIERST#)

19 IN BLC_GPIO A47 PIRQE*/GPIO2
55 19 IN AUD_IP_PERIPHERAL_DET C41 PIRQF*/GPIO3
33 19 IN TBT_PWR_REQ_L F45 PIRQG*/GPIO4
54 19 IN AUD_I2C_INT_L F40 PIRQH*/GPIO5

7 TP_PCI_PME_L H2 PME* (IPU)
27 25 OUT PLT_RESET_L F7 PLTRSTB*

75 25 OUT LPC_CLK33M_SMC_R G51 CLKOUT_PCI0
25 OUT LPC_CLK33M_LPCPLUS_R E49 CLKOUT_PCI1
7 TP_PCI_CLK33M_OUT2 H48 CLKOUT_PCI2
7 TP_PCI_CLK33M_OUT3 J43 CLKOUT_PCI3
25 OUT PCH_CLK33M_PCIOUT G45 CLKOUT_PCI4
(IPD)

35 25 20 19 18 17 8 =PP3V3_S0_PCH_GPIO

R2010 10K 1 2 5% 1/20W MF 201 PCI_INTA_L D49 PIRQA*
R2011 10K 1 2 5% 1/20W MF 201 PCI_INTB_L C48 PIRQB*
R2012 10K 1 2 5% 1/20W MF 201 PCI_INTC_L C47 PIRQC*
R2013 10K 1 2 5% 1/20W MF 201 PCI_INTD_L C45 PIRQD*

NO STUFF
R2054 10K 2 1 5% 1/20W MF 201

=PP3V3_SUS_PCH_GPIO 8 17 18 20
=PP3V3_S3_PCH_GPIO 8 25
=PP3V3_S0_PCH_GPIO 8 17 18 19 20 25 35

R2016 10K 1 2 5% 1/20W MF 201 JTAG_GMUX_TMS 19
R2017 10K 1 2 5% 1/20W MF 201 BLC_I2C_MUX_SEL 19
R2018 10K 1 2 5% 1/20W MF 201 USE_HDD_OOB_L 19
R2030 10K 1 2 5% 1/20W MF 201 BLC_GPIO 19

NO STUFF Redundant to pull-up on audio page
R2014 10K 1 2 5% 1/20W MF 201 AUD_IP_PERIPHERAL_DET 19 55
R2031 10K 1 2 5% 1/20W MF 201 TBT_PWR_REQ_L 19 33

NO STUFF Redundant to pull-up on audio page
R2033 10K 1 2 5% 1/20W MF 201 AUD_I2C_INT_L 19 54

R2069 10K 1 2 5% 1/20W MF 201 XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE 19 24
R2060 10K 1 2 5% 1/20W MF 201 XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L 19 24
R2061 10K 1 2 5% 1/20W MF 201 XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L 19 24
R2062 10K 1 2 5% 1/20W MF 201 XDP_DA2_PCH_GPIO41_USB_EXTC_OC_L 19 24
R2068 10K 1 2 5% 1/20W MF 201 XDP_DA3_PCH_GPIO42_USB_EXTD_OC_L 19 24
R2067 10K 2 1 5% 1/20W MF 201 AP_PWR_EN 24 36 66

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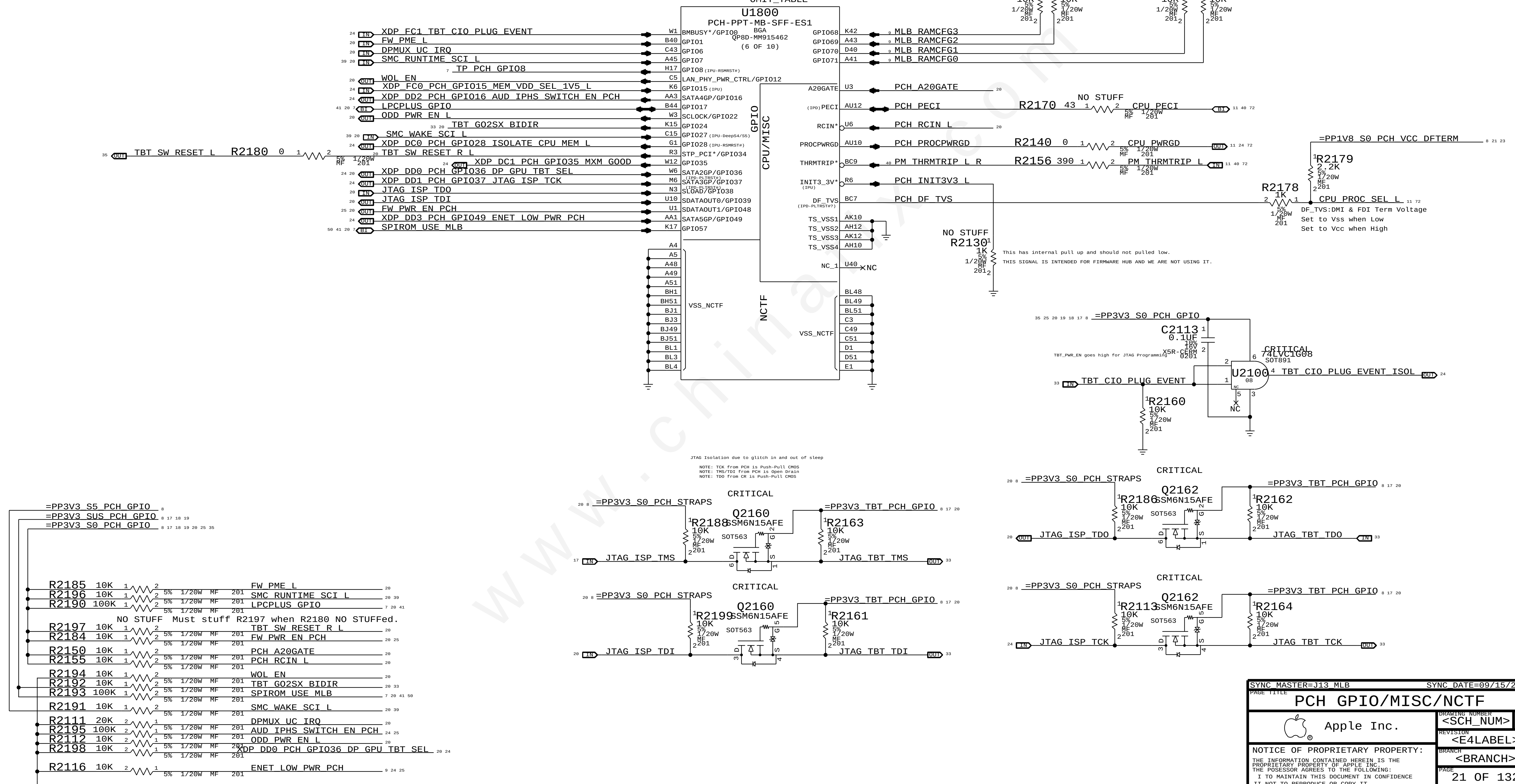
BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.

R2574 is 1K series resistor between U2100 output and PCH input to reduce the current between the two drivers..



OMIT_TABLE
U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
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GPIO
CPU/MISC
NCTF
VSS_NCTF
XDP_FC1_TBT_CIO_PLUG_EVENT
FW_PME_L
DPMUX_UC_IRQ
SMC_RUNTIME_SCI_L
TP_PCH_GPIO8
WOL_EN
XDP_FC0_PCH_GPIO15_MEM_VDD_SEL_1V5_L
XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH
LPCPLUS_GPIO
ODD_PWR_EN_L
TBT_GO2SX_BIDIR
SMC_WAKE_SCI_L
XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L
TBT_SW_RESET_R_L
XDP_DC1_PCH_GPIO35_MXM_GOOD
XDP_DD0_PCH_GPIO36_DP_GPU_TBT_SEL
XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK
JTAG_ISP_TDO
JTAG_ISP_TDI
FW_PWR_EN_PCH
XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH
SPIROM_USE_MLB
TBT_SW_RESET_L
R2180
=PP3V3_S0_PCH_GPIO
RAMCFG3:H
RAMCFG2:H
RAMCFG1:H
RAMCFG0:H
R2172
R2173
R2174
R2175
MLB_RAMCFG3
MLB_RAMCFG2
MLB_RAMCFG1
MLB_RAMCFG0
PCH_A20GATE
PCH_PECI
NO STUFF
R2170
CPU_PECI
PCH_RCIN_L
PCH_PROCPWRGD
R2140
CPU_PWRGD
PM_THRMTRIP_L_R
R2156
PM_THRMTRIP_L
PCH_INIT3V3_L
PCH_DF_TVS
=PP1V8_S0_PCH_VCC_DFTERM
R2179
R2178
CPU_PROC_SEL_L
DF_TVS:DMI & FDI Term Voltage
Set to Vss when Low
Set to Vcc when High
NO STUFF
R2130
This has internal pull up and should not pulled low.
THIS SIGNAL IS INTENDED FOR FIRMWARE HUB AND WE ARE NOT USING IT.
NC
C2113
0.1UF
CRITICAL
74LVC1G08
SOT891
U2100
TBT_PWR_EN goes high for JTAG Programming
TBT_CIO_PLUG_EVENT
TBT_CIO_PLUG_EVENT_ISOL
R2160
JTAG Isolation due to glitch in and out of sleep
NOTE: TCK from PCH is Push-Pull CMOS
NOTE: TMS/TDI from PCH is Open Drain
NOTE: TDO from CR is Push-Pull CMOS
=PP3V3_S0_PCH_STRAPS
=PP3V3_TBT_PCH_GPIO
CRITICAL
Q2160
SSM6N15AFE
SOT563
R2188
R2163
JTAG_ISP_TMS
JTAG_TBT_TMS
R2199
R2161
JTAG_ISP_TDI
JTAG_TBT_TDI
Q2162
R2186
R2162
JTAG_ISP_TDO
JTAG_TBT_TDO
R2113
R2164
JTAG_ISP_TCK
JTAG_TBT_TCK
=PP3V3_S5_PCH_GPIO
=PP3V3_SUS_PCH_GPIO
=PP3V3_S0_PCH_GPIO
R2185 10K
R2196 10K
R2190 100K
NO STUFF Must stuff R2197 when R2180 NO STUFFed.
R2197 10K
R2184 10K
R2150 10K
R2155 10K
R2194 10K
R2192 10K
R2193 100K
R2191 10K
R2111 20K
R2195 100K
R2112 10K
R2198 10K
R2116 10K
FW_PME_L
SMC_RUNTIME_SCI_L
LPCPLUS_GPIO
TBT_SW_RESET_R_L
FW_PWR_EN_PCH
PCH_A20GATE
PCH_RCIN_L
WOL_EN
TBT_GO2SX_BIDIR
SPIROM_USE_MLB
SMC_WAKE_SCI_L
DPMUX_UC_IRQ
AUD_IPHS_SWITCH_EN_PCH
ODD_PWR_EN_L
XDP_DD0_PCH_GPIO36_DP_GPU_TBT_SEL
ENET_LOW_PWR_PCH

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PCH GPIO/MISC/NCTF

Apple Inc.

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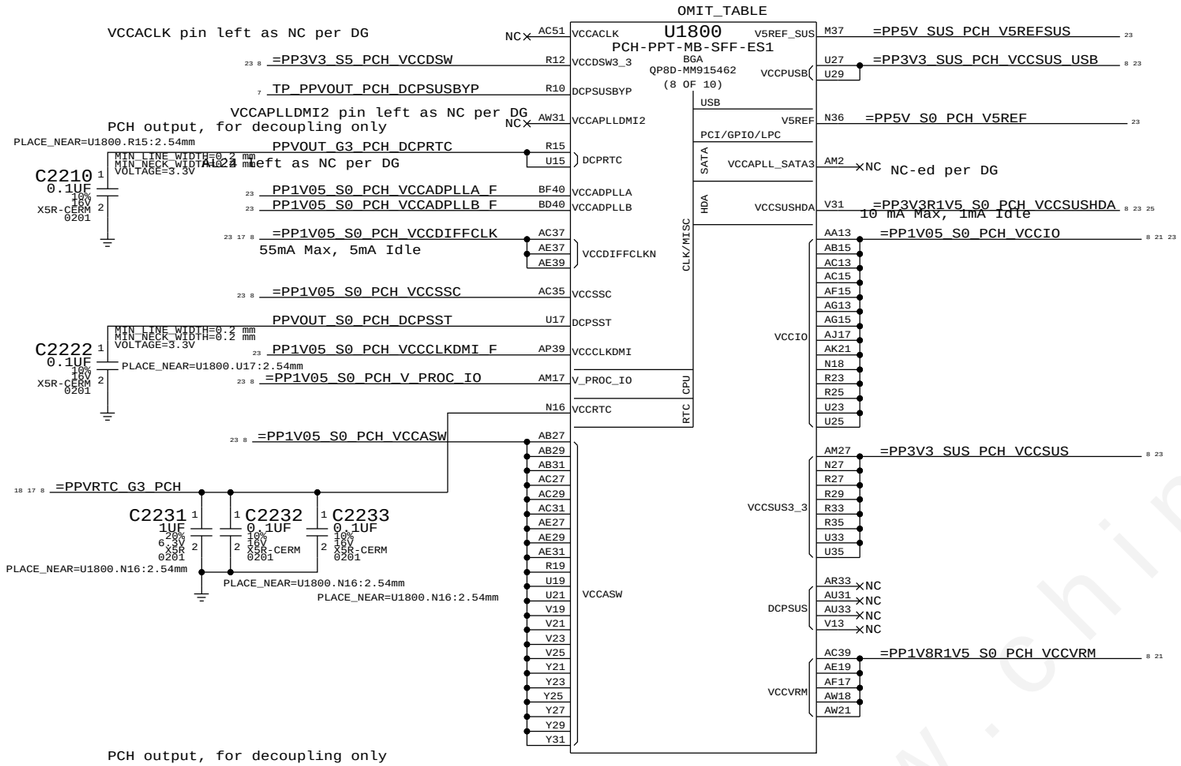

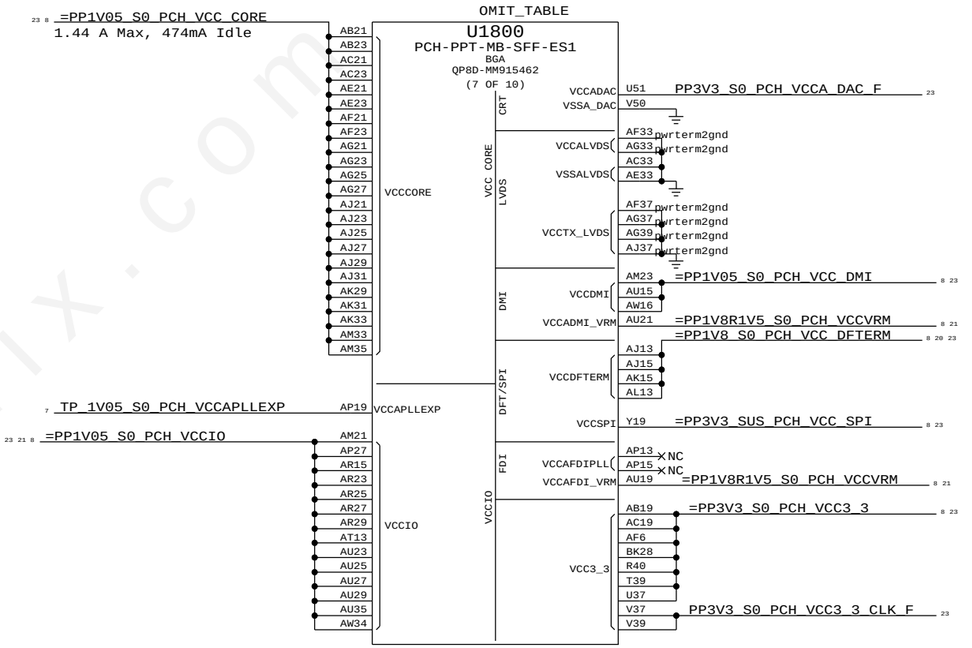

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U1800
PCH-PPT-MB-SFF-ES1
BGA
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AA7			AP2
AA9			AP4
AA11			AP7
AA39			AP9
AA41			AP11
AA43			AP17
AA45			AP21
AB2			AP23
AB4			AP25
AB17			AP29
AB25			AP31
AB33			AP33
AB35			AP35
AB37			AP37
AB48			AP41
AB50			AP43
AC7			AP45
AC9			AP48
AC11			AP50
AC17			AR6
AC25			AR8
AC41			AR17
AC43			AR19
AC45			AR21
AE7			AR31
AE9			AR35
AE11			AR37
AE13			AT7
AE15			AT9
AE17			AT11
AE25			AT39
AE35			AT41
AE41			AT43
AE43			AT45
AE45			AU17
AF2			AU37
AF4			AV2
AF8			AV4
AF19			AV48
AF25			AV50
AF27			AW7
AF29	VSS	VSS	AW9
AF31			AW11
AF35			AW13
AF48			AW23
AF50			AW25
AG7			AW27
AG9			AW29
AG11			AW36
AG17			AW39
AG19			AW41
AG29			AW43
AG31			AW45
AG35			AY10
AG41			B6
AG43			B10
AG45			B14
AH2			B18
AJ7			B22
AJ9			B26
AJ11			B30
AJ19			B34
AJ33			B38
AJ35			B42
AJ39			B46
AJ41			BA7
AJ43			BA9
AJ45			BA11
AK2			BA13
AK4			BA16
AK17			BA18
AK19			BA21
AK23			BA23
AK25			BA25
AK27			BA27
AK35			BA29
AK37			BA31
AK48			BA34
AK50			BA36
AL7			BA39
AL9			BA41
AL11			BA43
AL39			BA45
AL41			BB2
AL43			BB4
AL45			BB48
AM15			BB50
AM19			BC11
AM25			BC13
AM29			BC16
AM31			BC18
AM37			BC21

OMIT_TABLE

U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(10 OF 10)

BC23			G39
BC25			G41
BC27			G43
BC29			J7
BC31			J9
BC34			J11
BC36			J13
BC39			J16
BC41			J18
BC43			J21
BC45			J23
BD15			J25
BD24			J27
BE7			J29
BE9			J31
BE11			J34
BE13			J36
BE16			J39
BE18			J41
BE21			J45
BE23			K2
BE25			K4
BE27			K48
BE29			K50
BE31			L7
BE34			L9
BE36			L11
BE39			L13
BE41			L16
BE43			L18
BE45			L21
BF2			L23
BF4			L25
BF15			L27
BF24			L29
BF48			L31
BF50			L34
BH6			L36
BH10			L39
BH14	VSS	VSS	L41
BH18			L43
BH22			L45
BH26			N7
BH28			N9
BH30			N11
BH32			N13
BH34			N21
BH38			N23
BH42			N25
BH44			N29
BH46			N31
BH48			N34
BK10			N39
BK14			N41
BK18			N43
BK22			N45
BK26			P2
BK30			P4
BK32			P48
BK34			P50
BK38			R17
BK42			R21
BK46			R31
D6			R37
D10			T7
D14			T9
D18			T11
D22			T13
D26			T41
D30			T43
D34			T45
D38			U31
D42			U49
D46			V2
F2			V4
F4			V7
F48			V9
F50			V11
G7			V15
G9			V17
G11			V27
G13			V29
G16			V33
G18			V35
G21			V41
G23			V43
G25			V45
G27			V48
G29			Y15
G31			Y17
G34			Y33
G36			Y35
			Y37

SYNC_MASTER=J13_MLB SYNC_DATE=09/15/2011

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PCH GROUNDS

Apple Inc.

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REVISION <E4LABEL>
BRANCH <BRANCH>
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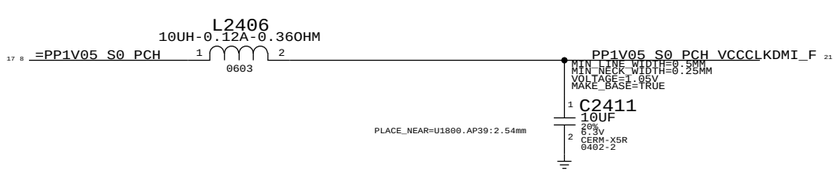

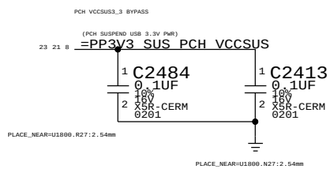

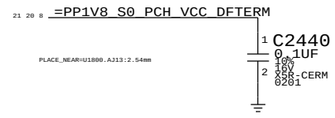

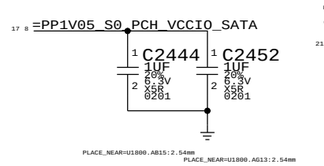

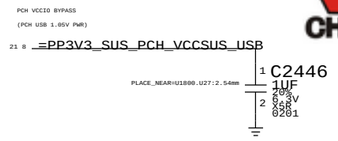

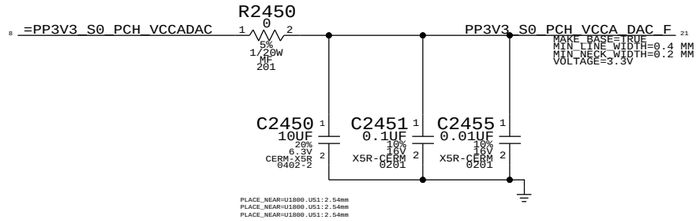

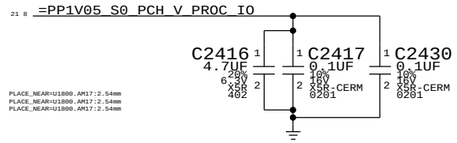

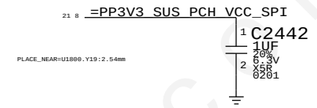

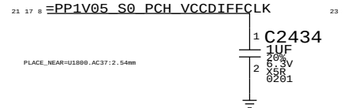

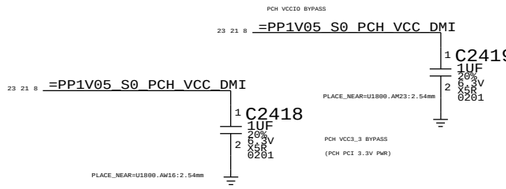

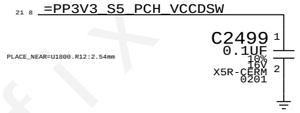

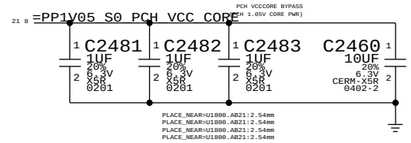

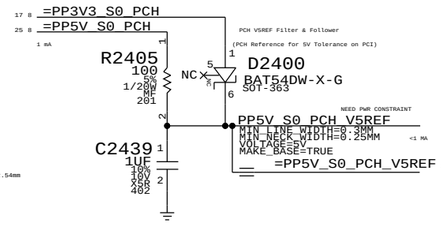

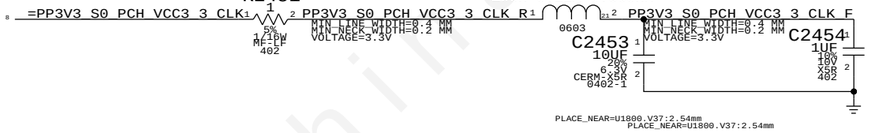

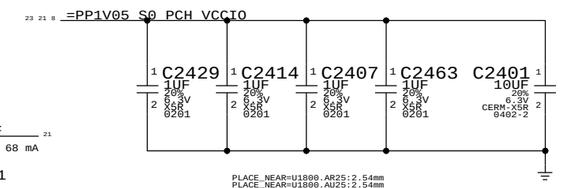

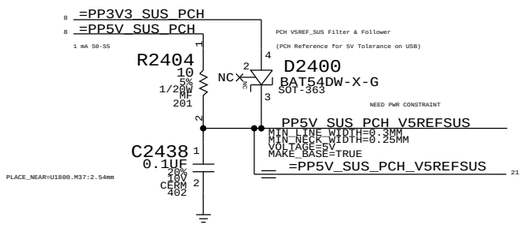

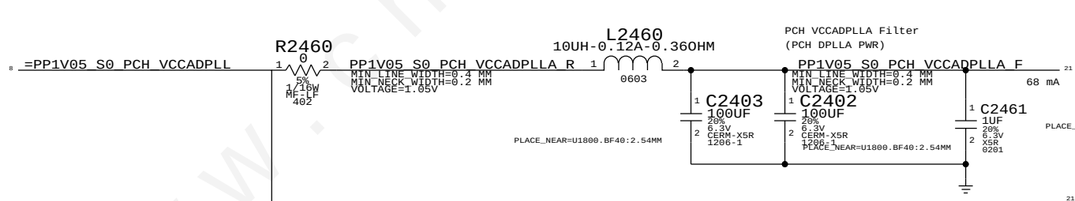

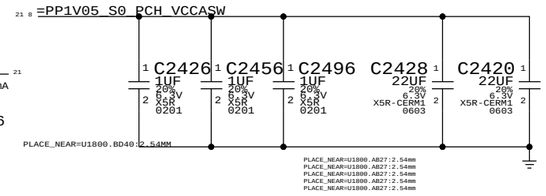

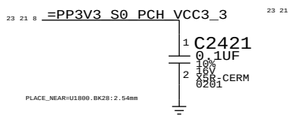

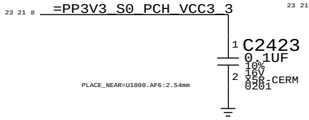

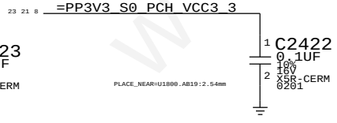

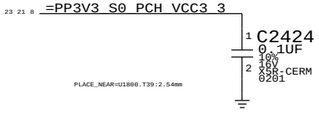

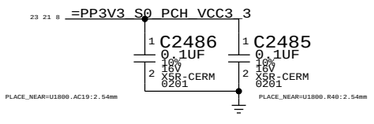

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PCH DECOUPLING

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REVISION	<E4LABEL>
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CPU Micro2-XDP

=PPVCCIO_S0_XDP

=PP3V3_S0_XDP
NO STUFF
R2540 1K 5% 1/16W MF-LF 402

CRITICAL
XDP_CONN
J2500
DF40RC-60DP-0.4V
M-ST-SM1

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

XDP_CPU_PREQ_L	OBSEN_A0	OBSEN_C0	CPU_CFG<16>
XDP_CPU_PRDY_L	OBSEN_A1	OBSEN_C1	CPU_CFG<17>
XDP_BPM_L<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<0>
XDP_BPM_L<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<1>
XDP_BPM_L<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<2>
XDP_BPM_L<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<3>
CPU_CFG<10>	OBSEN_B0	OBSEN_D0	CPU_CFG<8>
CPU_CFG<11>	OBSEN_B1	OBSEN_D1	CPU_CFG<9>
XDP_OBSDATA_B<0>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<4>
XDP_OBSDATA_B<1>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<5>
XDP_OBSDATA_B<2>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<6>
XDP_OBSDATA_B<3>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<7>
XDP_CPU_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	XDP_CPU_CLK100M_P
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	XDP_CPU_CLK100M_N
	VCC_OBS_AB	VCC_OBS_CD	
XDP_CPU_CFG<0>	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_VR_READY	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
=SMBUS_XDP_SDA	SDA	TDO	XDP_CPU_TDO
=SMBUS_XDP_SCL	SCL	TRSTn	XDP_CPU_TRST_L
	TCK1	TDI	XDP_CPU_TDI
XDP_CPU_TCK	TCK0	TMS	XDP_CPU_TMS
	NCX	XDP_PRESENT#	

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP_CPU_TDO R2510 51 — PLACE_NEAR=J2500.52:2.54mm
XDP_CPU_TDI R2511 51 — PLACE_NEAR=U1000.K61:2.54mm
XDP_CPU_TMS R2512 51 — PLACE_NEAR=U1000.H59:2.54mm
XDP_CPU_TCK R2513 51 — PLACE_NEAR=U1000.J58:2.54mm
XDP_CPU_TRST_L R2514 51 — PLACE_NEAR=U1000.H63:2.54mm

R2515 0 — XDP PLACE_NEAR=R1841.1:2.54mm — ITPXDP_CLK100M_P
R2516 0 — XDP PLACE_NEAR=R1840.1:2.54mm — ITPXDP_CLK100M_N
R2505 1K — XDP PLACE_NEAR=U1000.G3:2.54mm — CPU_RESET_L

(R2560-R2563)
XDP_CPU:BPM

XDP_BPM_L<4>	R2560	0
XDP_BPM_L<5>	R2561	0
XDP_BPM_L<6>	R2562	0
XDP_BPM_L<7>	R2563	0

(R2564-R2567)
XDP_CPU:CFG

CPU_CFG<12>	R2564	0
CPU_CFG<13>	R2565	0
CPU_CFG<14>	R2566	0
CPU_CFG<15>	R2567	0

CPU_PWRGD	R2500	1K	XDP, PLACE_NEAR=U1000.C60:2.54mm
PM_PWRBTN_L	R2502	0	XDP, PLACE_NEAR=U4900.P17:2.54mm
CPU_CFG<0>	R2501	1K	XDP, PLACE_NEAR=U1000.B57:2.54mm
PM_PCH_SYS_PWROK	R2504	330	XDP

R2581 1K 1/20W 5% MF 201
R2580 1K 1/20W 5% MF 201

C2500 0.1UF 10% 10V X7R-CERM 0402
C2501 0.1UF 10% 10V X7R-CERM 0402

518S0847

XDP SIGNALS

(R2520-R2537)
XDP PCH SIGNALS

XDP_DA0_USB_EXTA_OC_L	R2520	33	XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L
XDP_DA1_USB_EXTB_OC_L	R2521	33	XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L
XDP_DA2_USB_EXTC_OC_L	R2522	33	XDP_DA2_PCH_GPIO41_USB_EXTC_OC_L
XDP_DA3_USB_EXTD_OC_L	R2523	33	XDP_DA3_PCH_GPIO42_USB_EXTD_OC_L
XDP_DB0_USB_EXTB_OC_EHCI_L	R2524	33	XDP_DB0_PCH_GPIO43_USB_EXTB_OC_EHCI
XDP_DB1_USB_EXTD_OC_EHCI_L	R2525	33	XDP_DB1_PCH_GPIO9_USB_EXTD_OC_EHCI_L
XDP_DB2_AP_PWR_EN	R2526	33	XDP_DB2_PCH_GPIO10_AP_PWR_EN
XDP_DB3_SDCONN_STATE_CHANGE	R2527	33	XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE
XDP_FC0_MEM_VDD_SEL_1V5_L	R2528	33	XDP_FC0_PCH_GPIO15_MEM_VDD_SEL_1V5_L
XDP_FC1	R2529	33	XDP_FC1_TBT_CIO_PLUG_EVENT
XDP_DC0_ISOLATE_CPU_MEM_L	R2530	33	XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L
XDP_DC1_MXM_GOOD	R2531	33	XDP_DC1_PCH_GPIO35_MXM_GOOD
XDP_DC2_DP_AUXCH_ISOL	R2532	33	XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL
XDP_DC3_SATARDRVR_EN	R2533	33	XDP_DC3_PCH_GPIO19_SATARDRVR_EN
XDP_DD0_DP_GPU_TBT_SEL	R2534	33	XDP_DD0_PCH_GPIO36_DP_GPU_TBT_SEL
XDP_DD1_JTAG_ISP_TCK	R2535	33	XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK
XDP_DD2_AUD_IPHS_SWITCH_EN	R2536	33	XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH
XDP_DD3_ENET_LOW_PWR	R2537	33	XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH

PCH SIGNALS

XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L	R2590	0	USB_EXTA_OC_L
XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L	R2591	0	USB_EXTB_OC_L
XDP_DB2_PCH_GPIO10_AP_PWR_EN	R2596	0	AP_PWR_EN
XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE	R2597	0	SDCONN_STATE_CHANGE
XDP_DC3_PCH_GPIO19_SATARDRVR_EN	R2573	0	SATARDRVR_EN
XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L	R2570	0	ISOLATE_CPU_MEM_L
XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL	R2572	0	DP_AUXCH_ISOL
XDP_FC1_TBT_CIO_PLUG_EVENT	R2574	1K	TBT_CIO_PLUG_EVENT_ISOL

Non-XDP Signals

PPDDR:1V5

XDP_FC0_PCH_GPIO15_MEM_VDD_SEL_1V5_L	R2595	0	MEM_VDD_SEL_1V5_L
XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK	R2575	0	JTAG_ISP_TCK
XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH	R2576	0	AUD_IPHS_SWITCH_EN_PCH
XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH	R2577	0	ENET_LOW_PWR_PCH

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

PCH Micro2-XDP

=PP3V3_S5_XDP

CRITICAL
XDP_CONN
J2550
DF40RC-60DP-0.4V
M-ST-SM1

TP_XDP_PCH_OBSFN_A<0>	OBSEN_A0	OBSEN_C0	XDP_FC0_MEM_VDD_SEL_1V5_L
TP_XDP_PCH_OBSFN_A<1>	OBSEN_A1	OBSEN_C1	XDP_FC1
XDP_DA0_USB_EXTA_OC_L	OBSDATA_A0	OBSDATA_C0	XDP_DC0_ISOLATE_CPU_MEM_L
XDP_DA1_USB_EXTB_OC_L	OBSDATA_A1	OBSDATA_C1	XDP_DC1_MXM_GOOD
XDP_DA2_USB_EXTC_OC_L	OBSDATA_A2	OBSDATA_C2	XDP_DC2_DP_AUXCH_ISOL
XDP_DA3_USB_EXTD_OC_L	OBSDATA_A3	OBSDATA_C3	XDP_DC3_SATARDRVR_EN
TP_XDP_PCH_OBSFN_B<0>	OBSEN_B0	OBSEN_D0	TP_XDP_PCH_OBSFN_D<0>
TP_XDP_PCH_OBSFN_B<1>	OBSEN_B1	OBSEN_D1	TP_XDP_PCH_OBSFN_D<1>
XDP_DB0_USB_EXTB_OC_EHCI_L	OBSDATA_B0	OBSDATA_D0	XDP_DD0_DP_GPU_TBT_SEL
XDP_DB1_USB_EXTD_OC_EHCI_L	OBSDATA_B1	OBSDATA_D1	XDP_DD1_JTAG_ISP_TCK
XDP_DB2_AP_PWR_EN	OBSDATA_B2	OBSDATA_D2	XDP_DD2_AUD_IPHS_SWITCH_EN
XDP_DB3_SDCONN_STATE_CHANGE	OBSDATA_B3	OBSDATA_D3	XDP_DD3_ENET_LOW_PWR
XDP_PCH_S5_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	TP_XDP_PCH_HOOK4
XDP_PCH_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	TP_XDP_PCH_HOOK5
	VCC_OBS_AB	VCC_OBS_CD	
TP_XDPPCH_HOOK2	HOOK2	RESET#/HOOK6	XDPPCH_PLTRST_L
TP_XDPPCH_HOOK3	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
=SMBUS_XDP_SDA	SDA	TDO	XDP_PCH_TDO
=SMBUS_XDP_SCL	SCL	TRSTn	TP_XDP_PCH_TRST_L
	TCK1	TDI	XDP_PCH_TDI
XDP_PCH_TCK	TCK0	TMS	XDP_PCH_TMS
	NCX	XDP_PRESENT#	

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

C2580 0.1UF 10% 10V X7R-CERM 0402
C2581 0.1UF 10% 10V X7R-CERM 0402

518S0847

PCH/XDP Signal Isolation Notes:

- Following Intel's Debug Prot Design Guid for HR and CR v1.3 doc id 404081.
Initially, stuffing both 33 and 0 ohms and validate whether it is functional in that state, else add BOM options.
- For isolated GPIOs:
  - 'Output' non-XDP signals require pulls.
  - 'Output' PCH/XDP signals require pulls.

R252x, R253x, R257x and R259x should be placed where signal path needes to split between route from PCH to J2550 and path to non-XDP signal destination.

ALL_SYS_PWRGD R2584 1K — XDP PLACE_NEAR=J2550.39:2.54mm
PM_PWRBTN_L R2585 0 — XDP PLACE_NEAR=U4900.P17:2.54mm

=PP1V05_SUS_PCH_JTAG

XDP_PCH_TDO R2550 51 — PLACE_NEAR=J2550.52:2.54mm
XDP_PCH_TDI R2551 51 — PLACE_NEAR=U1800.K5:2.54mm
XDP_PCH_TMS R2552 51 — PLACE_NEAR=U1800.H7:2.54mm
XDP_PCH_TCK R2556 51 — PLACE_NEAR=U1800.J3:2.54mm

1K series R on PCH Support Page

SYNC_MASTER=J30_MLB SYNC_DATE=07/14/2011

PAGE TITLE: CPU & PCH XDP

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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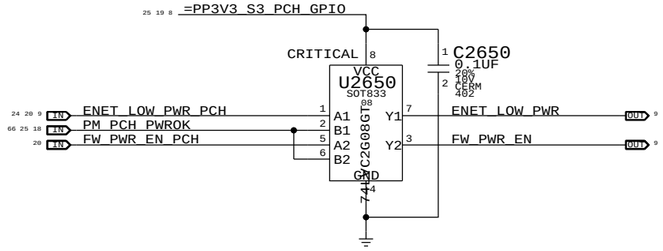
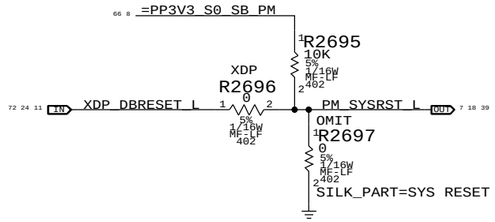
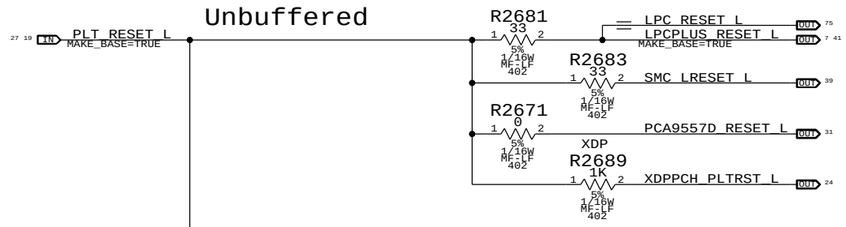
GPIO Glitch Prevention



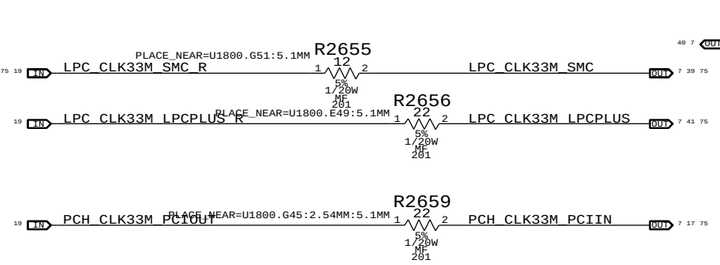
PCH Reset Button



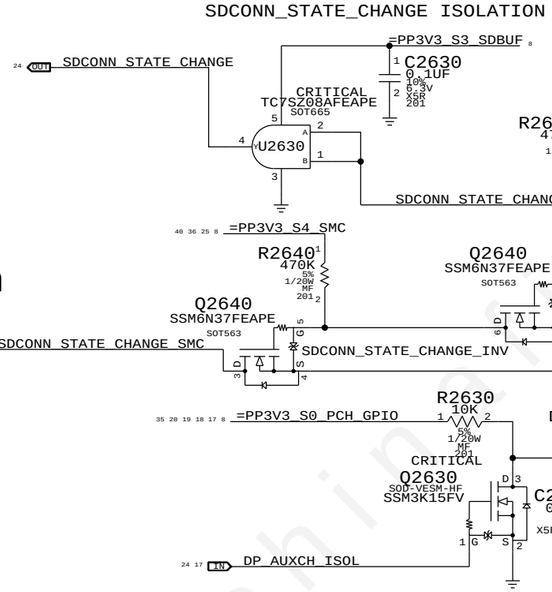
Platform Reset Connections



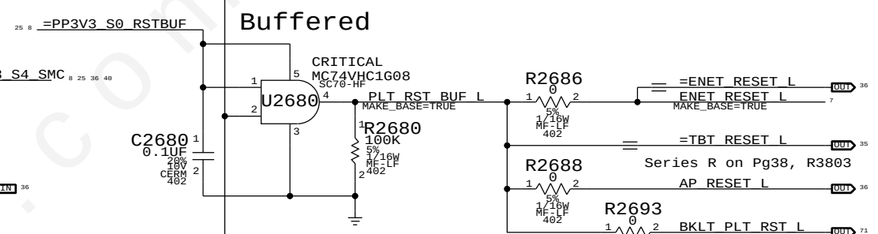
33 MHz Clock Series Termination



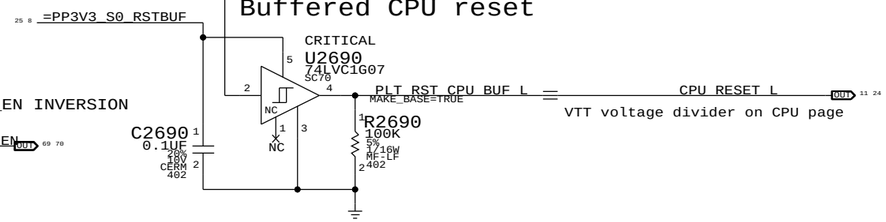
SDCONN_STATE_CHANGE ISOLATION



Buffered



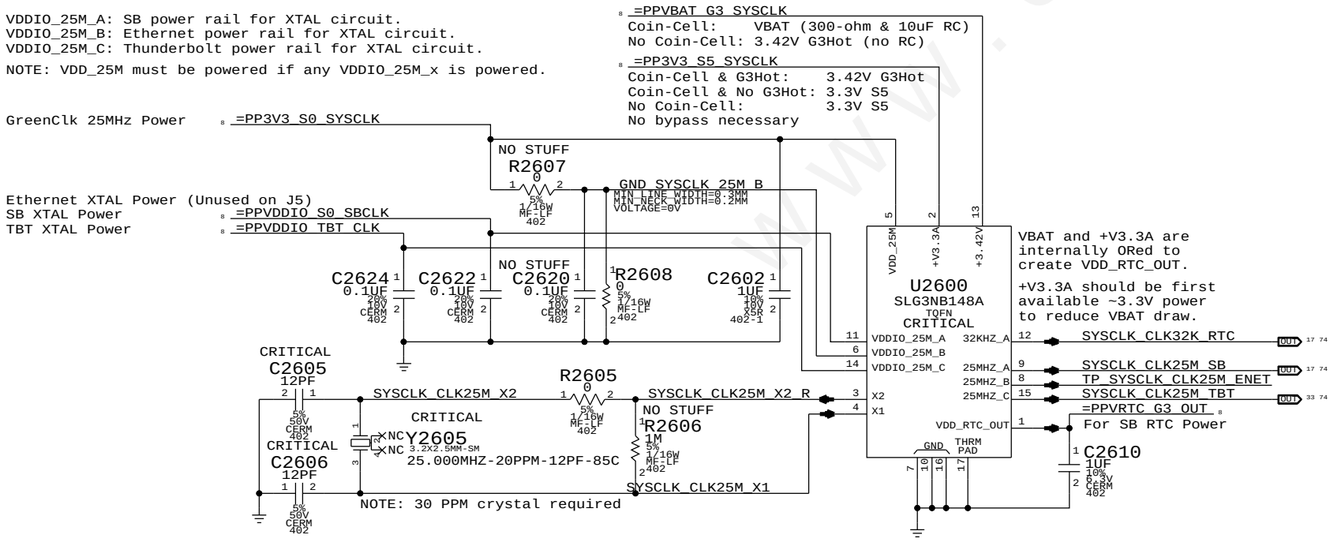
Buffered CPU reset



System RTC Power Source & 32kHz / 25MHz Clock Generator

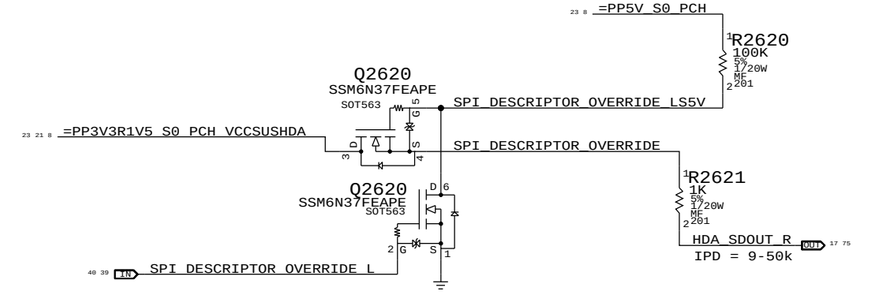
VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: Thunderbolt power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.



PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q2620 & 5V pull-up allows circuit to work regardless of HDA voltage.



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: Chipset Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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USB MUX FOR LS/FS INTERNAL DEVICES

BOM GROUP	BOM OPTIONS
HUB_ALLREM	HUB_NONREM1_0,HUB_NONREM0_0
HUB_1NONREM	HUB_NONREM1_0,HUB_NONREM0_1
HUB_2NONREM	HUB_NONREM1_1,HUB_NONREM0_0
HUB_3NONREM	HUB_NONREM1_1,HUB_NONREM0_1

NON_REM 1	NON_REM 0	STRAP PIN CFG
0	0	ALL PORTS ARE REMOVABLE
0	1	PORT 1 IS NON REMOVABLE
1	0	PORT 1&2 ARE NON REMOVABLE
1	1	PORT 1&2&3 ARE NON REMOVABLE

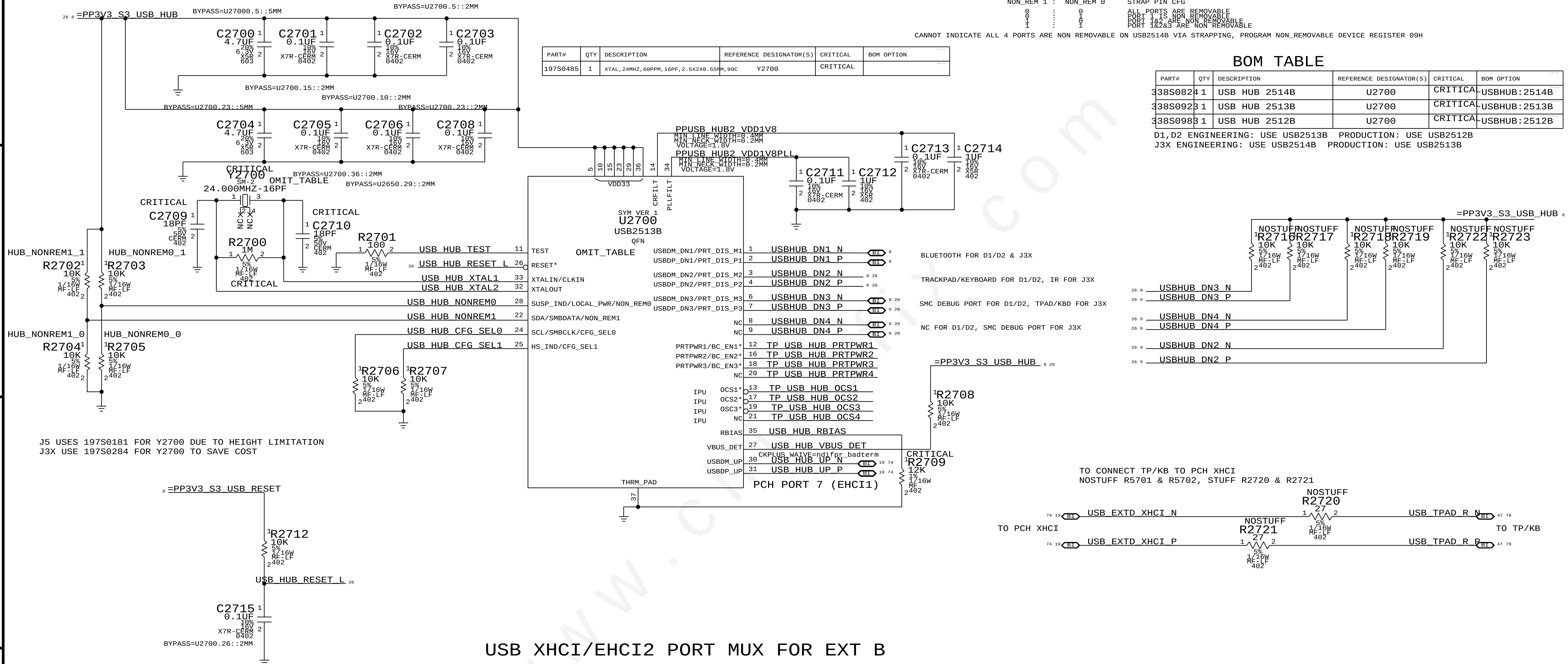
CANNOT INDICATE ALL 4 PORTS ARE NON REMOVABLE ON USB2514B VIA STRAPPING, PROGRAM NON_REMOVABLE DEVICE REGISTER 09H

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0485	1	XTAL,24MHZ,60PPM,16PF,2.5X2X0.55MM,90C	Y2700	CRITICAL	

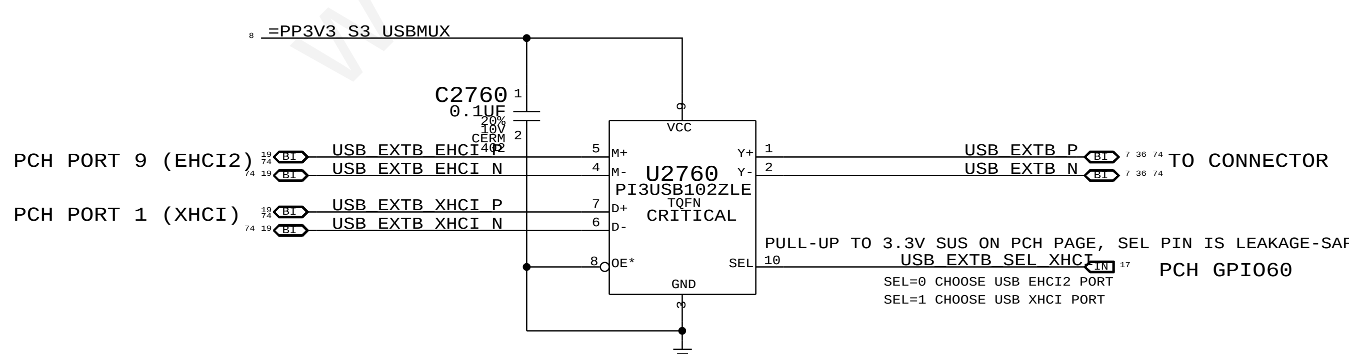
BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0824	1	USB HUB 2514B	U2700	CRITICAL	USBHUB:2514B
338S0923	1	USB HUB 2513B	U2700	CRITICAL	USBHUB:2513B
338S0988	1	USB HUB 2512B	U2700	CRITICAL	USBHUB:2512B

D1,D2 ENGINEERING: USE USB2513B PRODUCTION: USE USB2512B
J3X ENGINEERING: USE USB2514B PRODUCTION: USE USB2513B



USB XHCI/EHCI2 PORT MUX FOR EXT B



SYNC_MASTER=J5_AMD SYNC_DATE=08/17/2011

PAGE TITLE: USB HUB & MUX

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

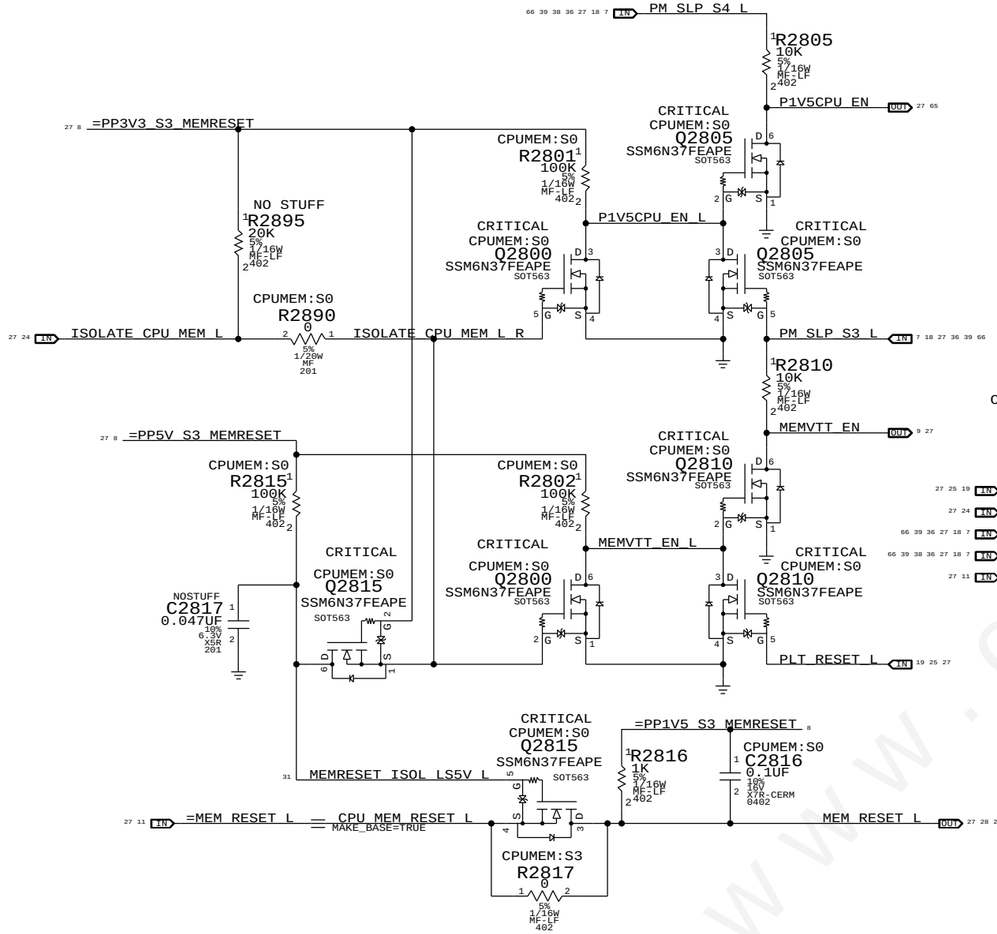
REVISION <E4LABEL>

BRANCH <BRANCH>

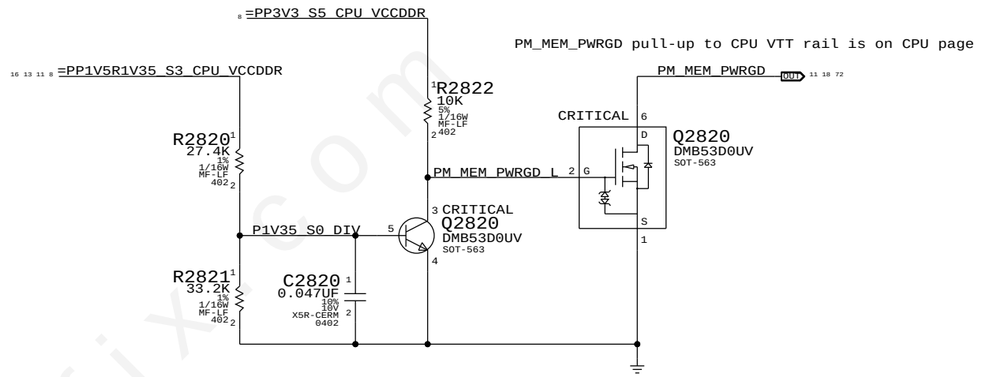
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

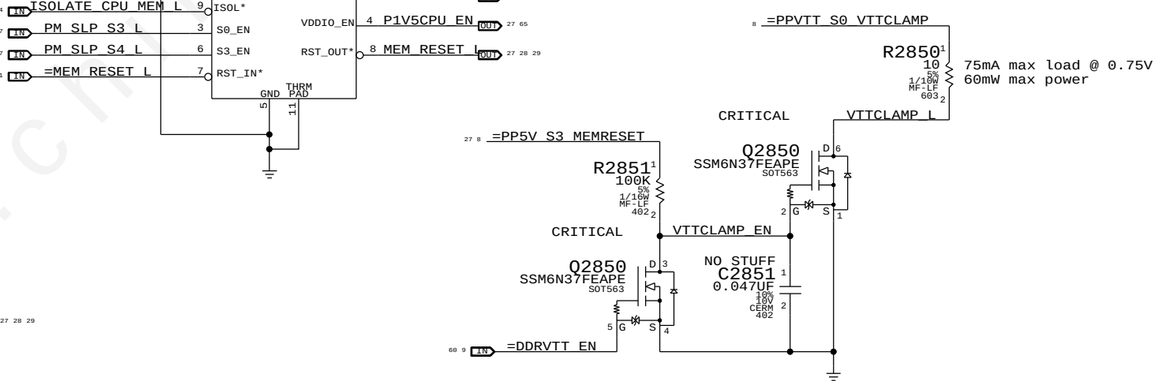


1V35 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
	4	0	0	1	1	X	1	0	1
S3	5	0	1	1	1	0 (*)	1	1	1
to	6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC_MASTER=J5_MLB SYNC_DATE=07/29/2011

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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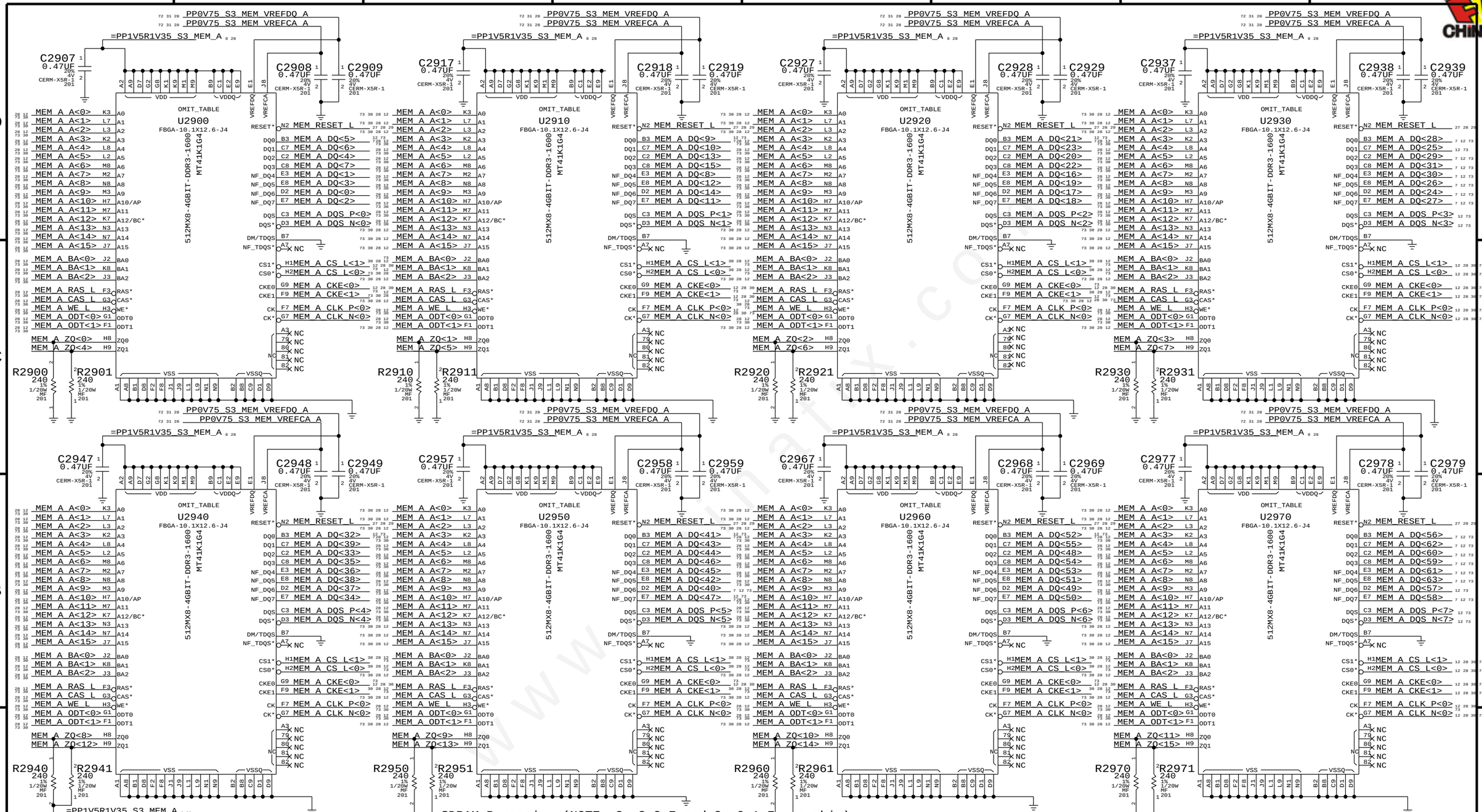

SYNC_MASTER=J5_MLB SYNC_DATE=07/14/2011

PAGE TITLE
DDR3 SDRAM Bank A (Rank 0)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
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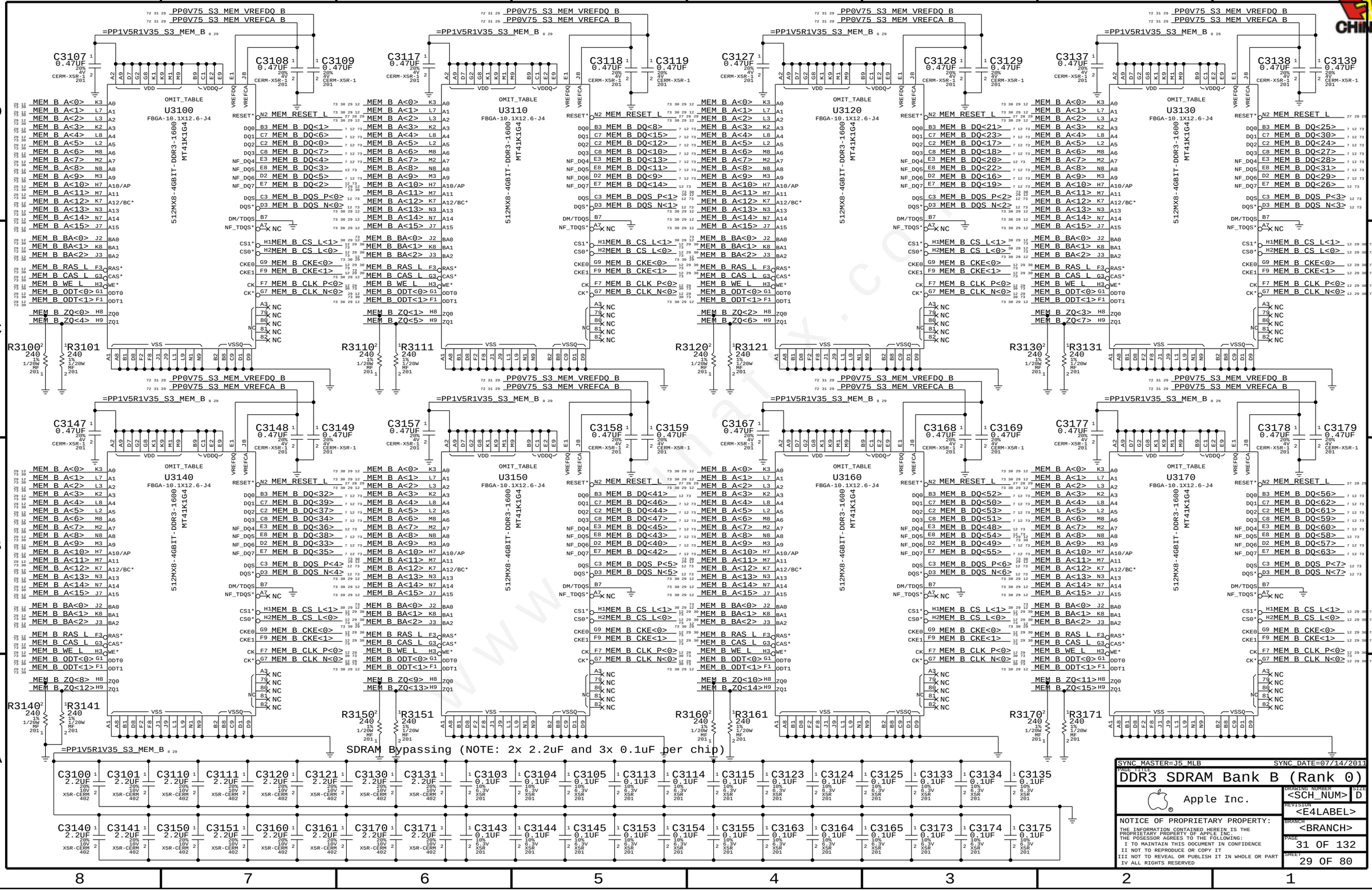

SYNC_MASTER=J5_MLB SYNC_DATE=07/14/2011

PAGE TITLE
DDR3 SDRAM Bank B (Rank 0)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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JEDEC 4.20.18 Unbuffered SODIMM Raw Card F spec recommends 36 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE

=PP0V75_S0_MEM_VTT_A

MEM_A_A<3>	RP3305	36	1	8	5% 1/32W	4X0201
MEM_A_CKE<1>	RP3301	36	4	5	5% 1/32W	4X0201
MEM_A_BA<2>	RP3302	36	2	7	5% 1/32W	4X0201
MEM_A_A<14>	RP3306	36	2	7	5% 1/32W	4X0201
MEM_A_A<2>	RP3303	36	1	8	5% 1/32W	4X0201
MEM_A_A<12>	RP3302	36	1	8	5% 1/32W	4X0201
MEM_A_ODT<0>	RP3301	36	2	7	5% 1/32W	4X0201
MEM_A_BA<0>	RP3305	36	2	7	5% 1/32W	4X0201
MEM_A_A<1>	RP3303	36	2	7	5% 1/32W	4X0201
MEM_A_A<7>	RP3307	36	3	6	5% 1/32W	4X0201
MEM_A_A<8>	RP3306	36	1	8	5% 1/32W	4X0201
MEM_A_CS_L<1>	RP3305	36	3	6	5% 1/32W	4X0201
MEM_A_A<11>	RP3306	36	4	5	5% 1/32W	4X0201
MEM_A_BA<1>	RP3302	36	3	6	5% 1/32W	4X0201
MEM_A_CKE<0>	RP3304	36	3	6	5% 1/32W	4X0201
MEM_A_A<0>	RP3303	36	4	5	5% 1/32W	4X0201
MEM_A_A<10>	RP3304	36	1	8	5% 1/32W	4X0201
MEM_A_A<9>	RP3307	36	2	7	5% 1/32W	4X0201
MEM_A_WE_L	RP3302	36	4	5	5% 1/32W	4X0201
MEM_A_A<4>	RP3303	36	3	6	5% 1/32W	4X0201
MEM_A_A<5>	RP3307	36	1	8	5% 1/32W	4X0201
MEM_A_A<15>	RP3305	36	4	5	5% 1/32W	4X0201
MEM_A_A<13>	RP3307	36	4	5	5% 1/32W	4X0201
MEM_A_CAS_L	RP3304	36	2	7	5% 1/32W	4X0201
MEM_A_CS_L<0>	RP3304	36	4	5	5% 1/32W	4X0201
MEM_A_RAS_L	RP3301	36	3	6	5% 1/32W	4X0201
MEM_A_ODT<1>	RP3301	36	1	8	5% 1/32W	4X0201
MEM_A_A<6>	RP3306	36	3	6	5% 1/32W	4X0201

C3300 0.47UF 20% 4V CERM-X5R-1 201
C3302 0.47UF 20% 4V CERM-X5R-1 201
C3303 0.47UF 20% 4V CERM-X5R-1 201
C3304 0.47UF 20% 4V CERM-X5R-1 201
C3305 0.47UF 20% 4V CERM-X5R-1 201
C3306 0.47UF 20% 4V CERM-X5R-1 201
C3307 0.47UF 20% 4V CERM-X5R-1 201
C3308 0.47UF 20% 4V CERM-X5R-1 201
C3310 0.47UF 20% 4V CERM-X5R-1 201

=PP0V75_S0_MEM_VTT_B

MEM_B_WE_L	RP3322	36	2	7	5% 1/32W	4X0201
MEM_B_A<13>	RP3325	36	1	8	5% 1/32W	4X0201
MEM_B_CKE<1>	RP3328	36	1	8	5% 1/32W	4X0201
MEM_B_A<12>	RP3325	36	2	7	5% 1/32W	4X0201
MEM_B_ODT<1>	RP3328	36	2	7	5% 1/32W	4X0201
MEM_B_A<0>	RP3325	36	3	6	5% 1/32W	4X0201
MEM_B_CS_L<1>	RP3320	36	2	7	5% 1/32W	4X0201
MEM_B_BA<0>	RP3326	36	4	5	5% 1/32W	4X0201
MEM_B_A<6>	RP3330	36	2	7	5% 1/32W	4X0201
MEM_B_ODT<0>	RP3320	36	3	6	5% 1/32W	4X0201
MEM_B_A<4>	RP3330	36	1	8	5% 1/32W	4X0201
MEM_B_A<5>	RP3330	36	3	6	5% 1/32W	4X0201
MEM_B_BA<1>	RP3324	36	4	5	5% 1/32W	4X0201
MEM_B_A<9>	RP3326	36	2	7	5% 1/32W	4X0201
MEM_B_A<8>	RP3324	36	1	8	5% 1/32W	4X0201
MEM_B_A<3>	RP3326	36	3	6	5% 1/32W	4X0201
MEM_B_A<10>	RP3322	36	3	6	5% 1/32W	4X0201
MEM_B_A<7>	RP3326	36	1	8	5% 1/32W	4X0201
MEM_B_A<1>	RP3330	36	4	5	5% 1/32W	4X0201
MEM_B_A<14>	RP3324	36	3	6	5% 1/32W	4X0201
MEM_B_A<11>	RP3324	36	2	7	5% 1/32W	4X0201
MEM_B_A<2>	RP3325	36	4	5	5% 1/32W	4X0201
MEM_B_BA<2>	RP3320	36	4	5	5% 1/32W	4X0201
MEM_B_CS_L<0>	RP3320	36	1	8	5% 1/32W	4X0201
MEM_B_RAS_L	RP3322	36	1	8	5% 1/32W	4X0201
MEM_B_CAS_L	RP3328	36	4	5	5% 1/32W	4X0201
MEM_B_CKE<0>	RP3328	36	3	6	5% 1/32W	4X0201
MEM_B_A<15>	RP3322	36	4	5	5% 1/32W	4X0201

C3320 0.47UF 20% 4V CERM-X5R-1 201
C3322 0.47UF 20% 4V CERM-X5R-1 201
C3323 0.47UF 20% 4V CERM-X5R-1 201
C3324 0.47UF 20% 4V CERM-X5R-1 201
C3325 0.47UF 20% 4V CERM-X5R-1 201
C3326 0.47UF 20% 4V CERM-X5R-1 201
C3327 0.47UF 20% 4V CERM-X5R-1 201
C3328 0.47UF 20% 4V CERM-X5R-1 201
C3330 0.47UF 20% 4V CERM-X5R-1 201

MEM Clock Termination

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM

MEM_A_CLK_N<0> — R3350 30 5% 1/20W MF 201 — MEM_A_CLK0_TERM_R — C3351 0.1UF 10% 6.3V X5R 201
C3350 3.3PF 5% 25V CERM 201 PLACE_NEAR=U2900.F7:3.2mm
MEM_A_CLK_P<0> — R3351 30 5% 1/20W MF 201

MEM_B_CLK_N<0> — R3360 30 5% 1/20W MF 201 — MEM_B_CLK0_TERM_R — C3361 0.1UF 10% 6.3V X5R 201
C3360 3.3PF 5% 25V CERM 201 PLACE_NEAR=U3170.F7:3.2mm
MEM_B_CLK_P<0> — R3361 30 5% 1/20W MF 201

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: DDR3 Termination

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
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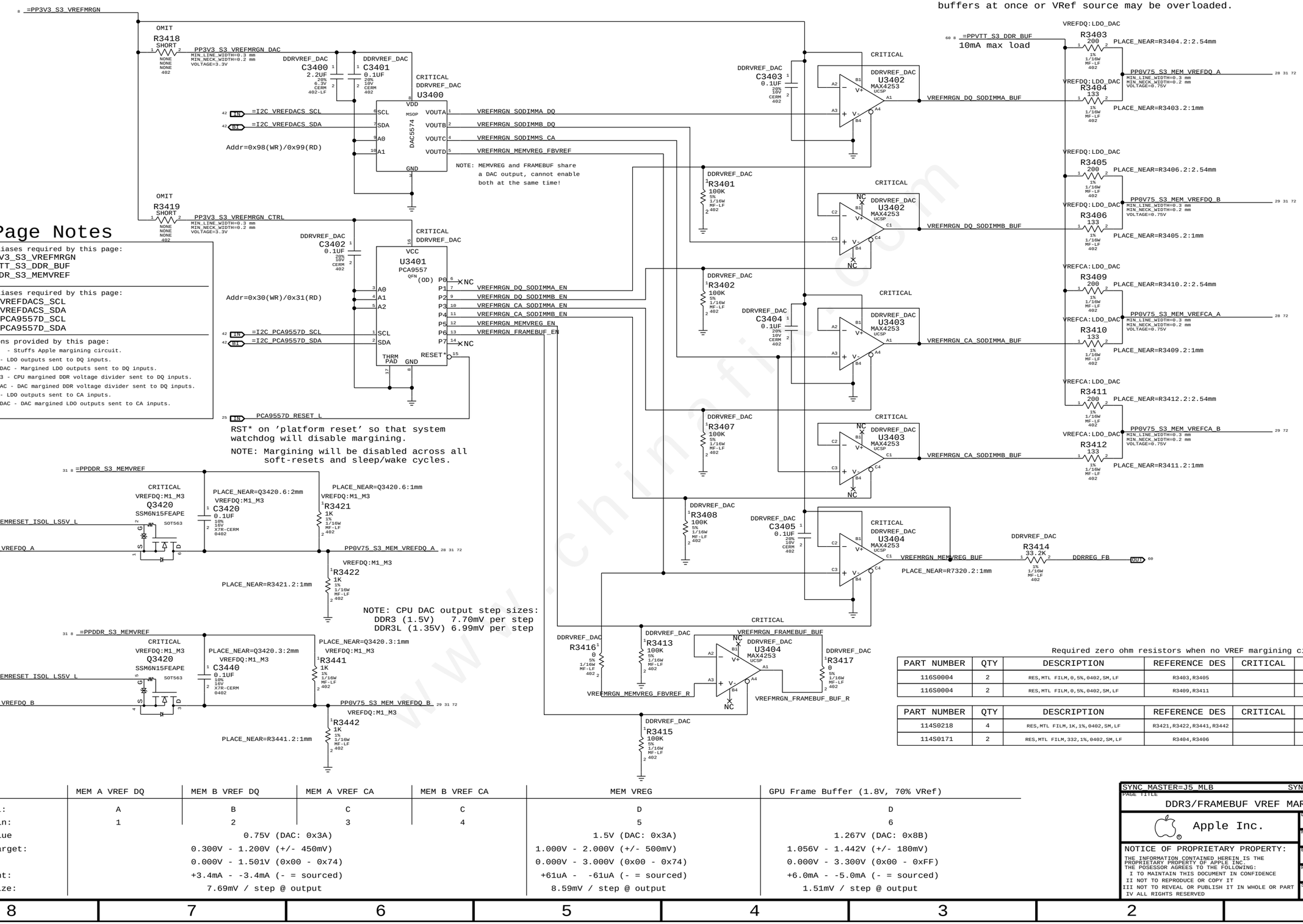

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:

DDRVREF_DAC - Stuffs Apple margining circuit.
VREFDQ:LDO - LDO outputs sent to DQ inputs.
VREFDQ:LDO_DAC - Margined LDO outputs sent to DQ inputs.
VREFDQ:M1_M3 - CPU margined DDR voltage divider sent to DQ inputs.
VREFDQ:M1_DAC - DAC margined DDR voltage divider sent to DQ inputs.
VREFCA:LDO - LDO outputs sent to CA inputs.
VREFCA:LDO_DAC - DAC margined LDO outputs sent to CA inputs.

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3403,R3405		VREFDQ:LDO
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3409,R3411		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0218	4	RES,MTL FILM,1K,1%,0402,SM,LF	R3421,R3422,R3441,R3442		VREFDQ:M1_DAC
114S0171	2	RES,MTL FILM,332,1%,0402,SM,LF	R3404,R3406		VREFDQ:M1_DAC

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=J5_MLB SYNC_DATE=07/29/2011

PAGE TITLE: DDR3/FRAMEBUF VREF MARGINING

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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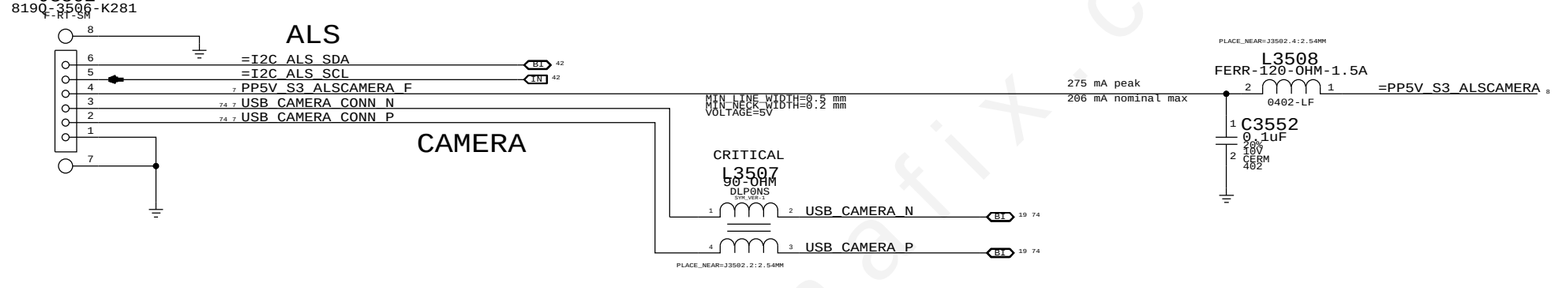
518S0767

CRITICAL
J3502
819Q-3506-K281
F-RT-SM



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PAGE TITLE
ALS/CAMERA CONNECTOR

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
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BRANCH <BRANCH>
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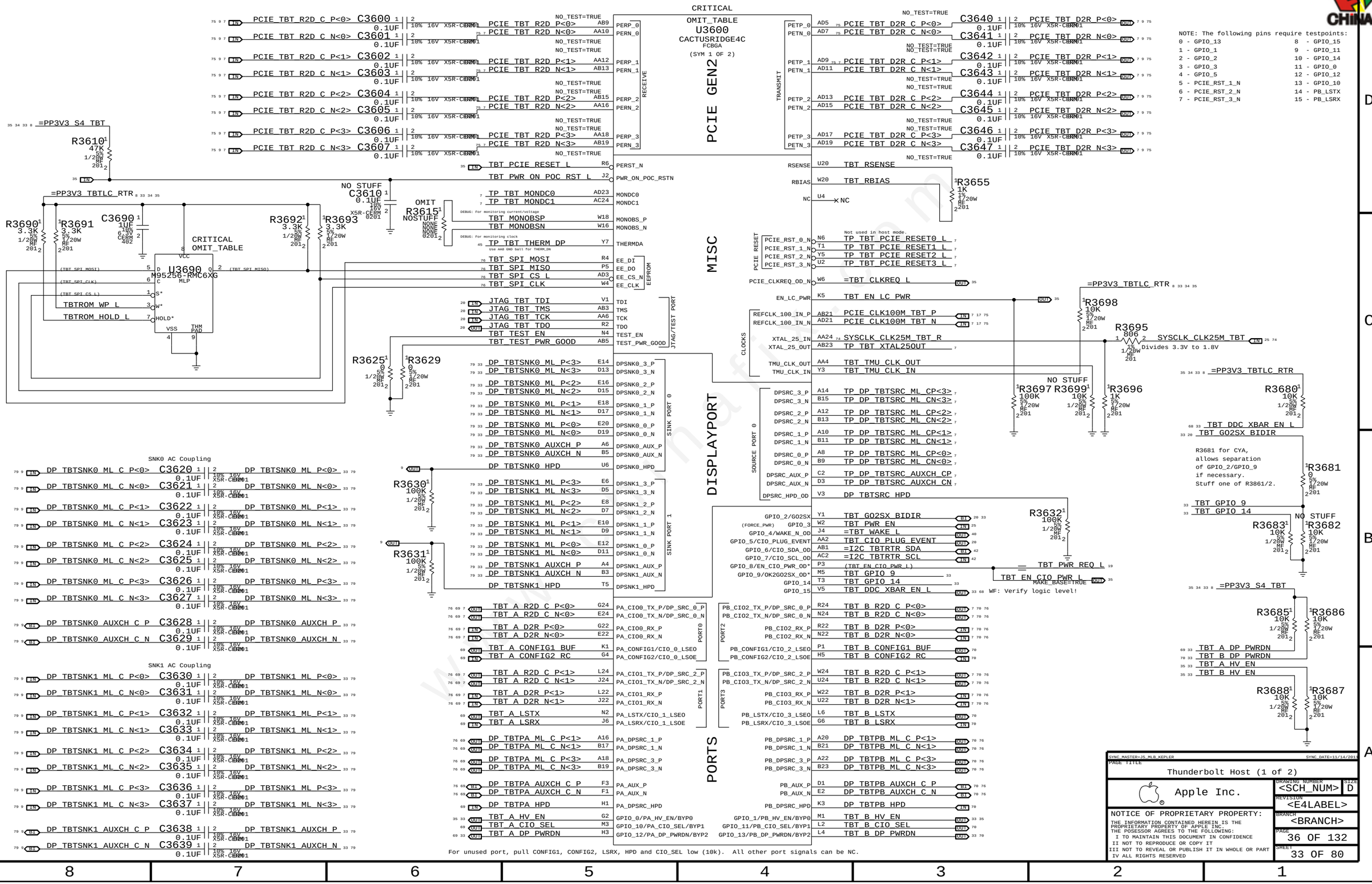
CRITICAL
OMIT_TABLE
U3600
CACTUSRIDGE4C
FCBGA
(SYM 1 OF 2)
PCIE GEN2
MISC
DISPLAYPORT
PORTS
RECEIVE
TRANSMIT
JTAG/TEST PORT
EEPROM
SINK PORT 0
SINK PORT 1
SOURCE PORT 0
PORT0
PORT1
PORT2
PORT3
CLOCKS
PCIE RESET
NOTE: The following pins require testpoints:
0 - GPIO_13
1 - GPIO_1
2 - GPIO_2
3 - GPIO_3
4 - GPIO_5
5 - PCIE_RST_1_N
6 - PCIE_RST_2_N
7 - PCIE_RST_3_N
8 - GPIO_15
9 - GPIO_11
10 - GPIO_14
11 - GPIO_0
12 - GPIO_12
13 - GPIO_10
14 - PB_LSTX
15 - PB_LSRX
SNK0 AC Coupling
SNK1 AC Coupling
For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.
SYNC_MASTER=J5_MLB_KEPLER
SYNC_DATE=11/14/2011
PAGE TITLE
Thunderbolt Host (1 of 2)
Apple Inc.
DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 36 OF 132
SHEET 33 OF 80
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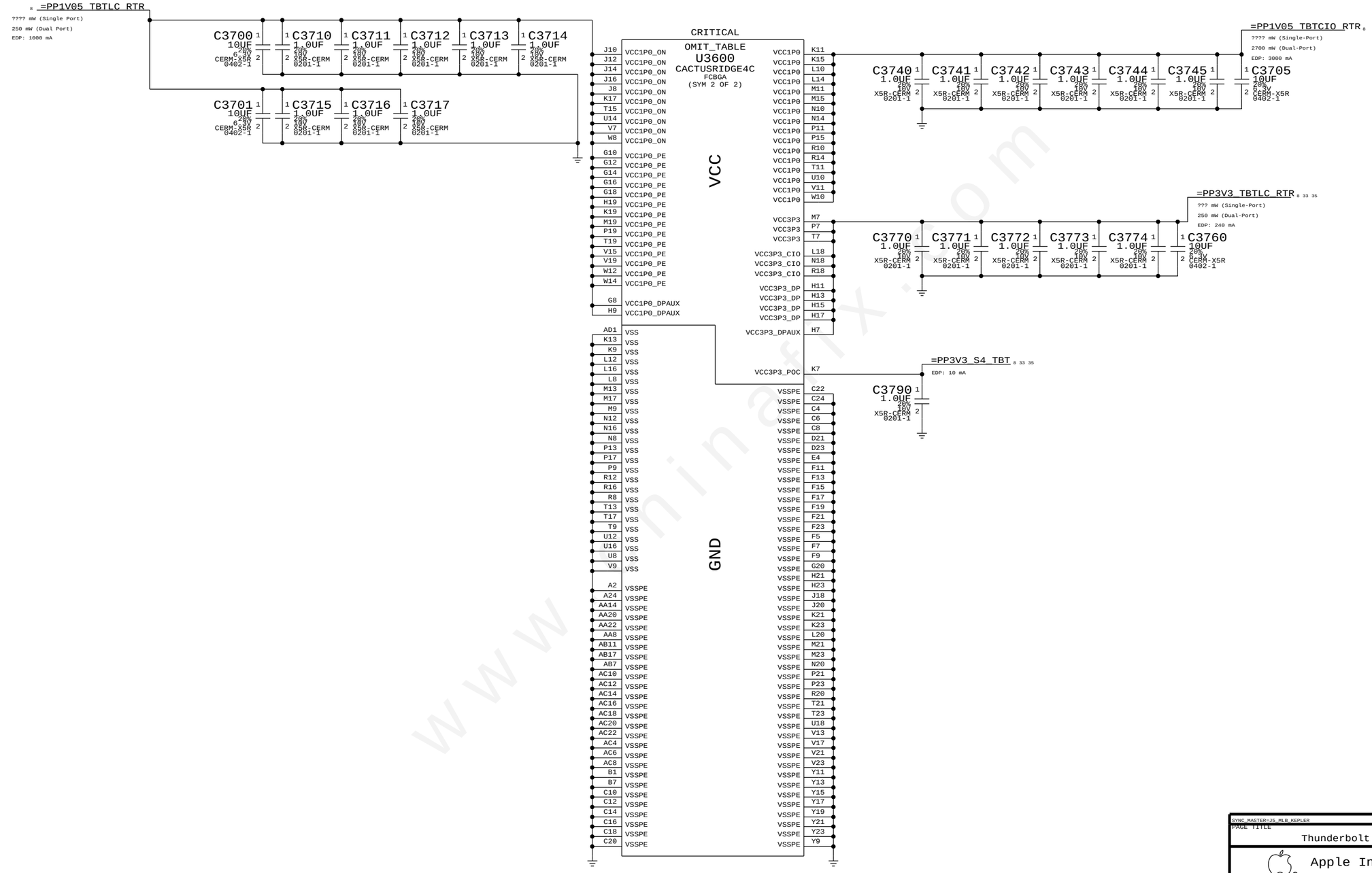

SYNC_MASTER=J5_MLB_KEPLER SYNC_DATE=11/14/2011

PAGE TITLE: Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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SHEET: 34 OF 80

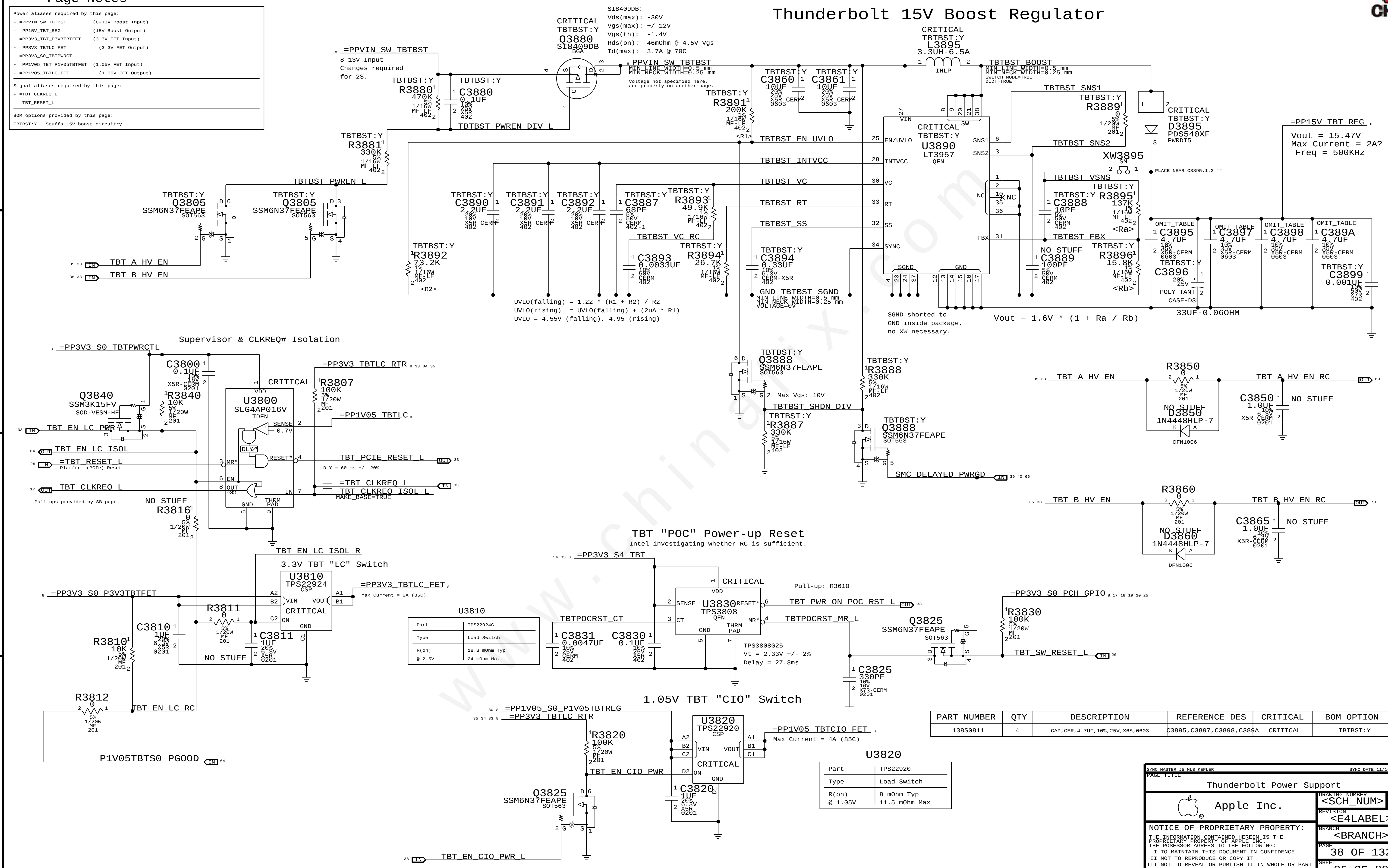
Thunderbolt 15V Boost Regulator

Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBTLC_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBTLC_FET (1.05V FET Output)

Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
TBTBST:Y - Stuffs 15V boost circuitry.



U3810

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.3 mOhm Typ 24 mOhm Max

U3820

Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	8 mOhm Typ 11.5 mOhm Max

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	4	CAP,CER,4.7UF,10%,25V,X6S,0603	C3895,C3897,C3898,C389A	CRITICAL	TBTBST:Y

SYNC_MASTER=J5_MLB_KEPLER SYNC_DATE=11/14/2011

PAGE TITLE: Thunderbolt Power Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 38 OF 132

SHEET: 35 OF 80

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	4	RES, 0OHM, 0201	L4470,L4471,L4473,L4474		

3V S3 WLAN FET

AIRPORT

DEBUG CURRENT SENSE RD135 connects to PP3V3_WLAN_F

U4450 TPS22924 CSP — CRITICAL

Max Current = 2A (85C)

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.3 mOhm Typ 24 mOhm Max

RIO FLEX CONNECTOR

CRITICAL

J4410 DF40CG3.0-70DS-0.4V F-ST-SM

516S1058

*NOTE: This connector is shielded 70P Hirose Receptacle.

Note: This receptacle mates with the plug with APN 998-4708.

RIO POWER CONNECTOR

CRITICAL

J4400 504050-0691 M-RT-SM

518S0862

Supervisor & CLKFREG # Isolation

Delay = 130 ms +/- 20%

SYNC_MASTER=MASTER SYNC_DATE=MASTER

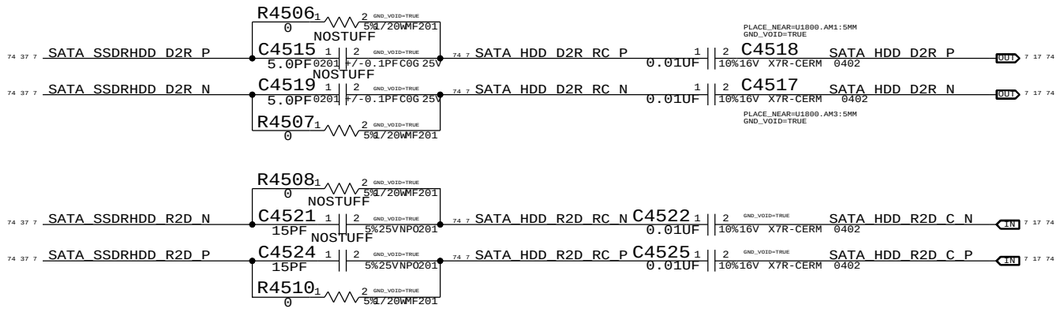
PAGE TITLE: RIO CONNECTORS

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 44 OF 132
SHEET: 36 OF 80

' C4518 & C4517 Placement Note:
' It is critical that these two should be near
' to U1800 pin AM1 and AM3.

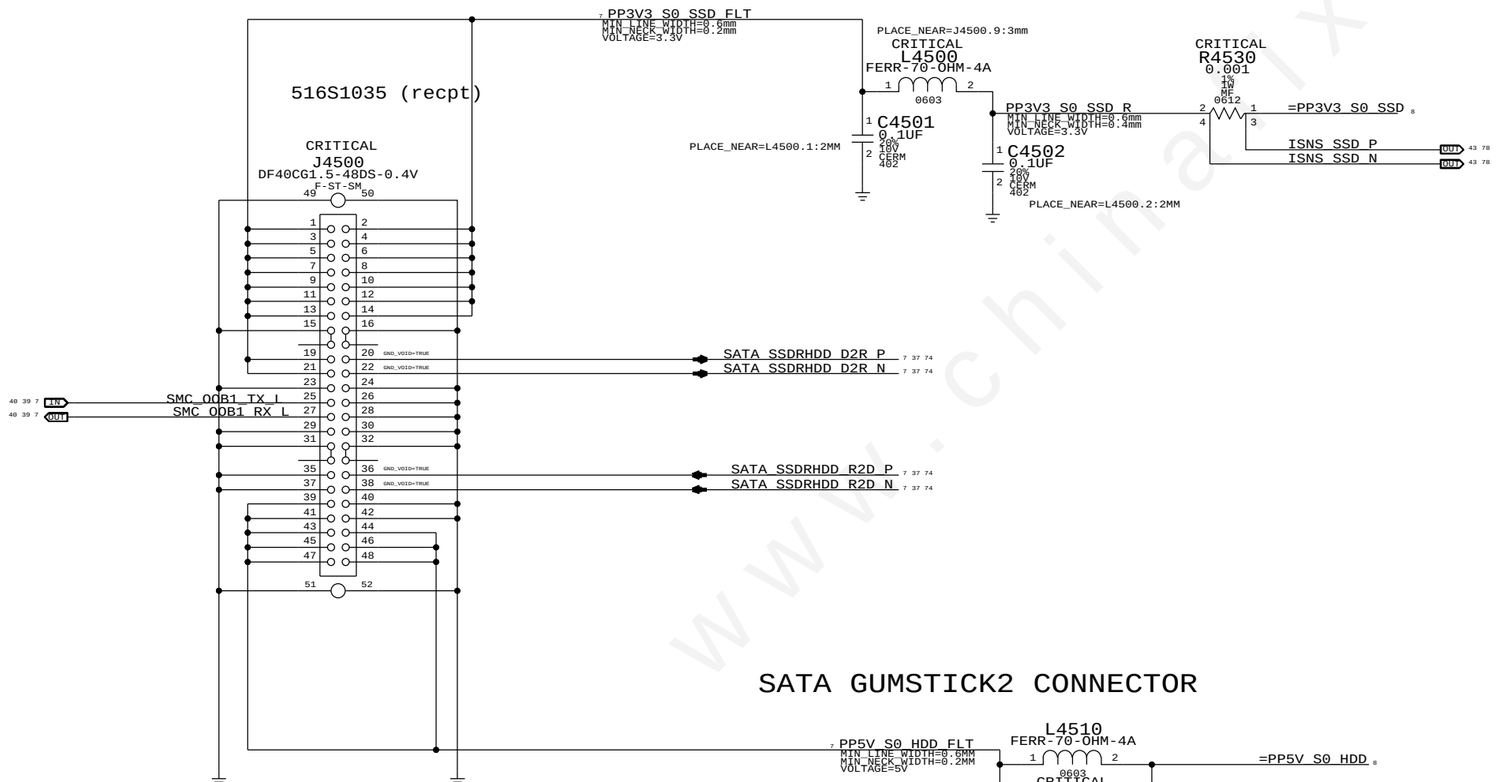
D2R Passive DeEmphasis

VALUE: 0.0 DB

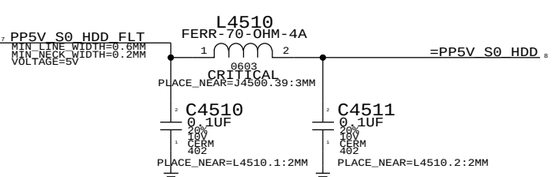


R2D Passive DeEmphasis

VALUE: 0.0 DB



SATA GUMSTICK2 CONNECTOR



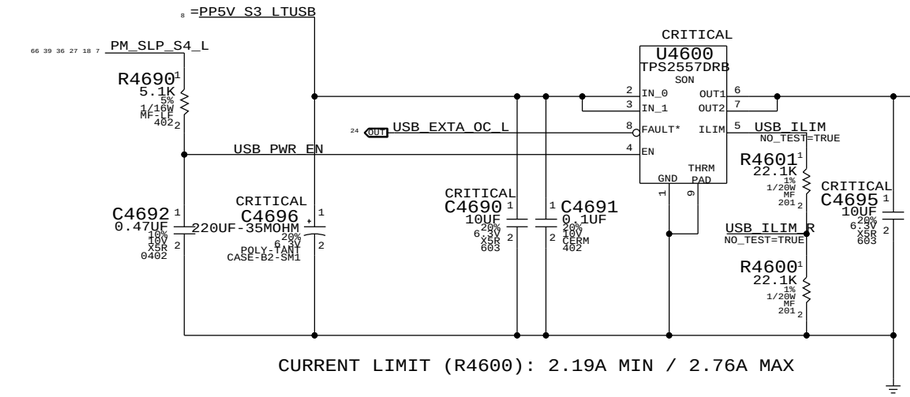
SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: SSD/HDD Connectors

Apple Inc.

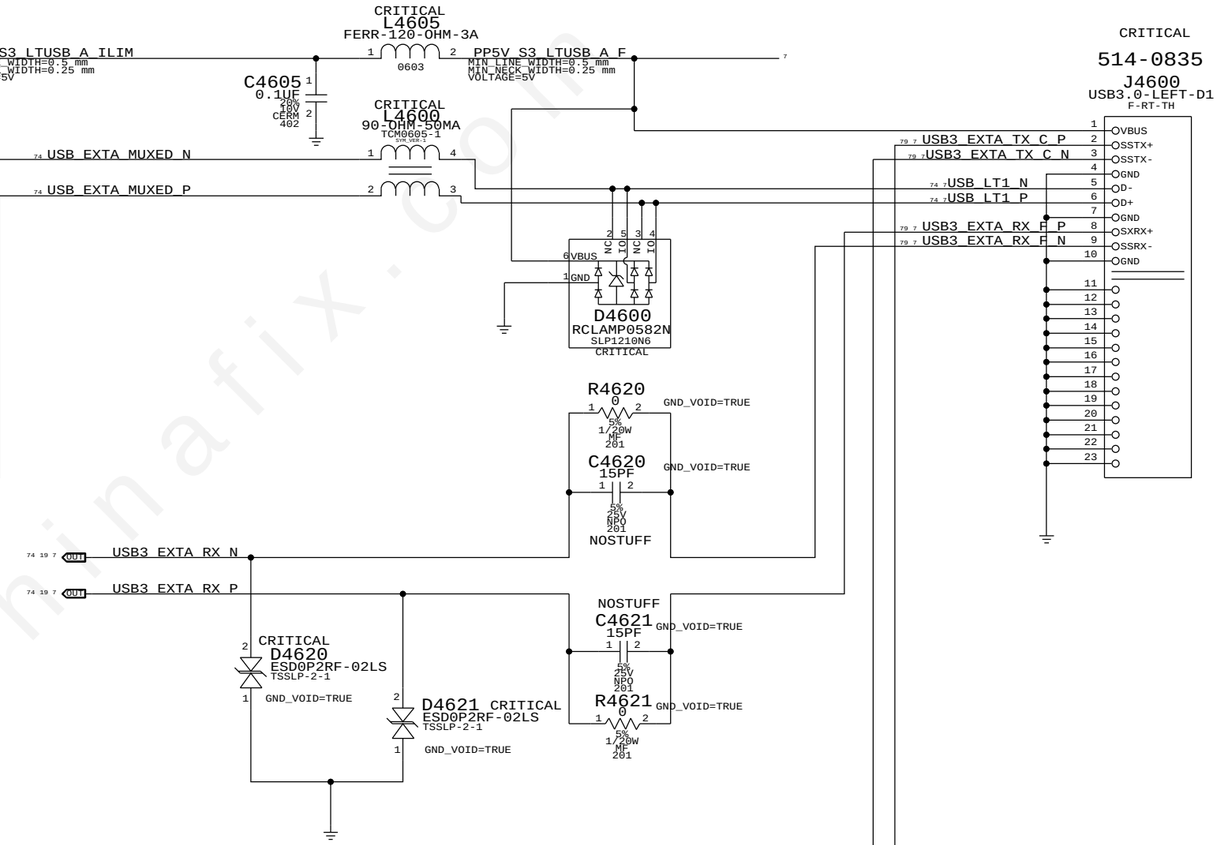
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 45 OF 132
SHEET: 37 OF 80

USB Port Power Switch

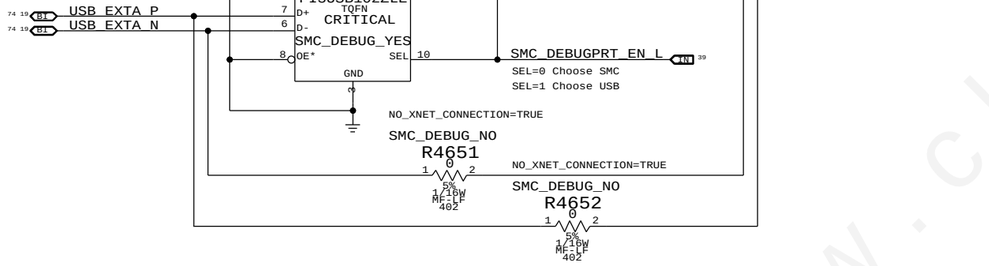


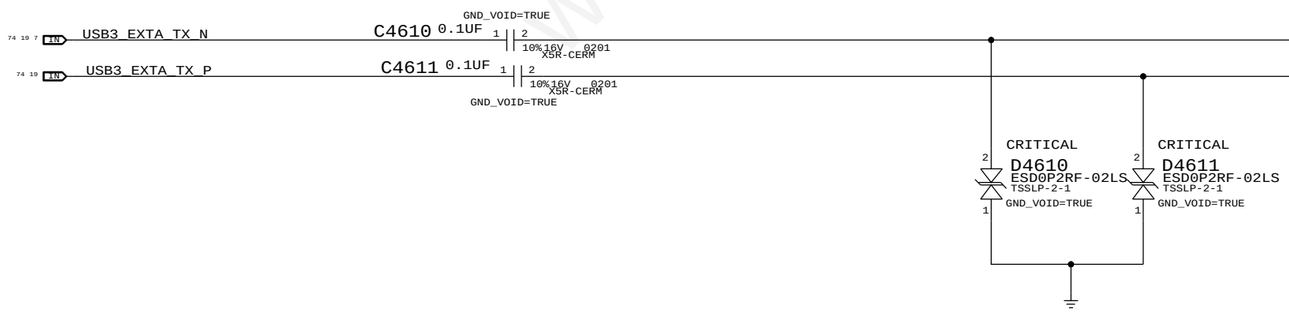
CURRENT LIMIT (R4600): 2.19A MIN / 2.76A MAX

Left USB Port A



USB/SMC Debug Mux





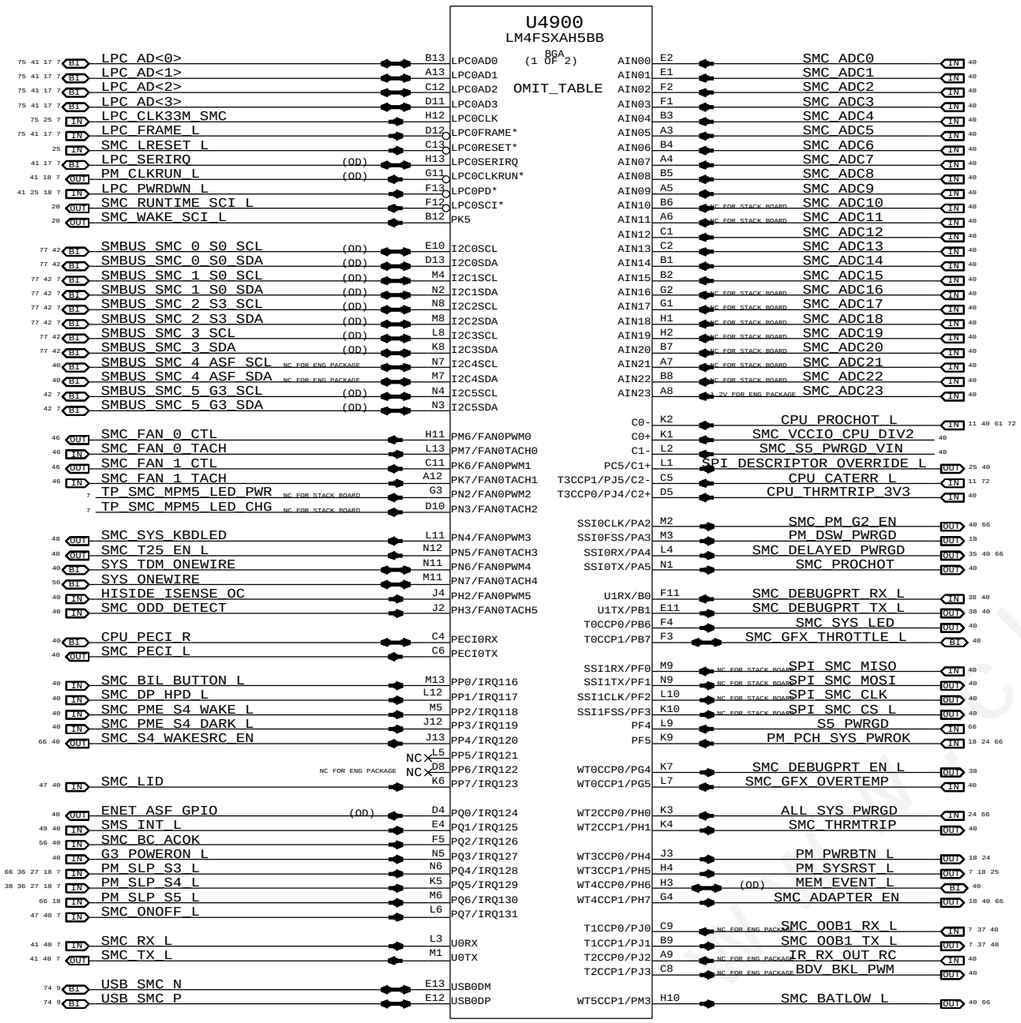
SYNC_MASTER=J5_AMD SYNC_DATE=08/24/2011

PAGE TITLE: USB 3.0 CONNECTORS

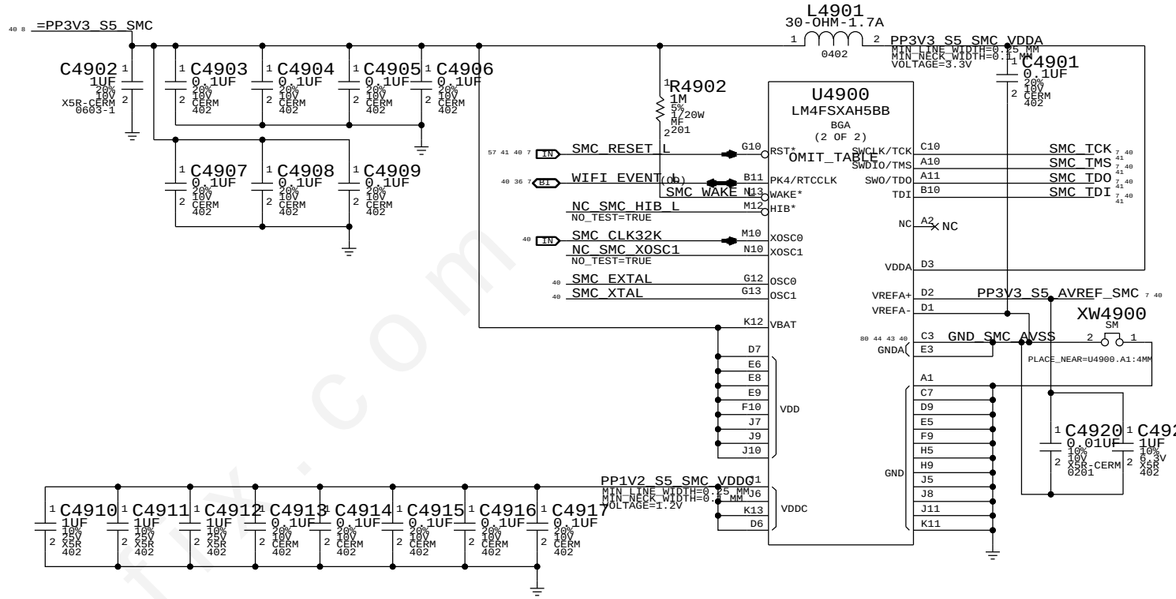
Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 46 OF 132
SHEET: 38 OF 80

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.



SYNC_MASTER=D1_SENSORS	SYNC_DATE=02/20/2012
PAGE TITLE	SMC
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 49 OF 132
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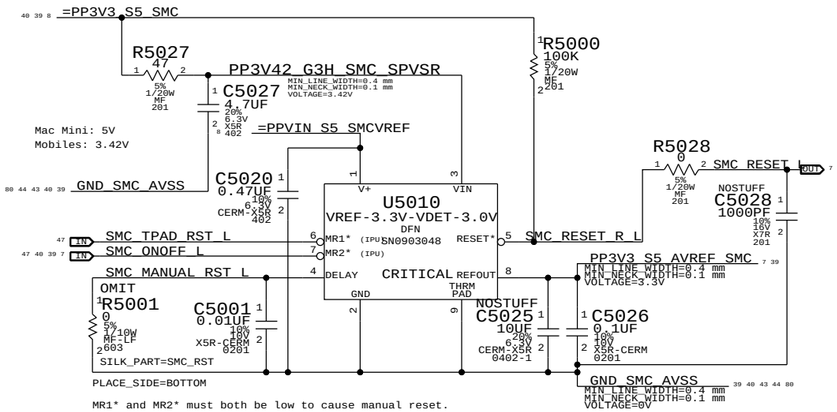
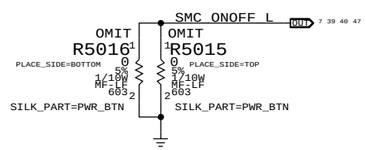
SMC Reset "Button", Supervisor & AVREF Supply



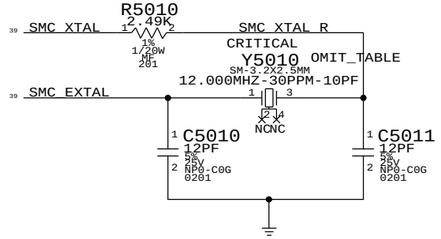
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

Debug Power "Buttons"



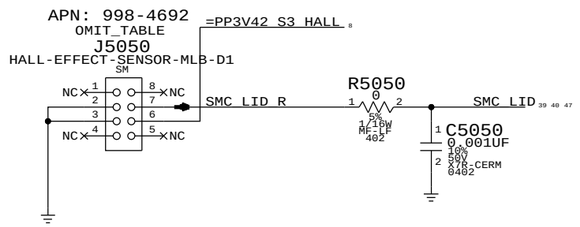
SMC Crystal Circuit



SMC USB CLOCK REQUIRE THESE CRYSTAL VALUES:5,6,8,10,12,16,18,20,24,25 MHZ

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
197S0486	1	XTAL,12MHZ,30PPM,10PF,3.2X2.5X0.7MM,90C	Y5010	CRITICAL	

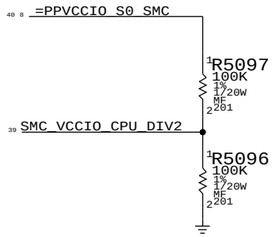
Hall Effect pads



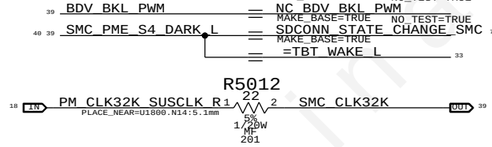
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-9320	1	SUBASSY,PCBA HALL EFFECT,J4	J5050	CRITICAL	

639-3261 (J4 Hall effect board) reports to 607-9320

Debug Power "Buttons"

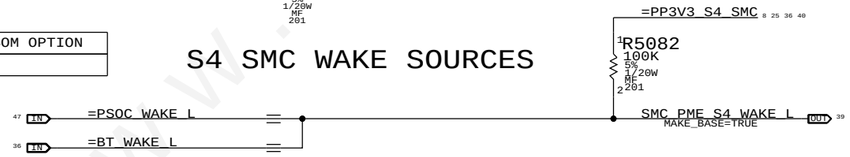


SMC Crystal Circuit

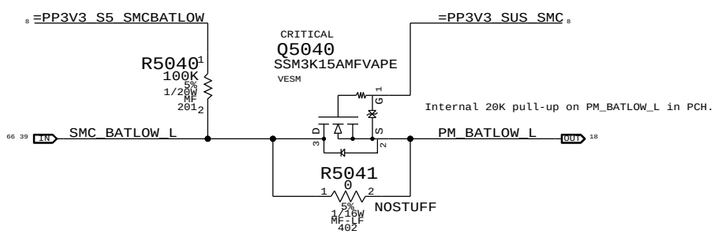


HDMI HPD ESD PROTECTION

S4 SMC WAKE SOURCES



BATLOW# ISOLATION

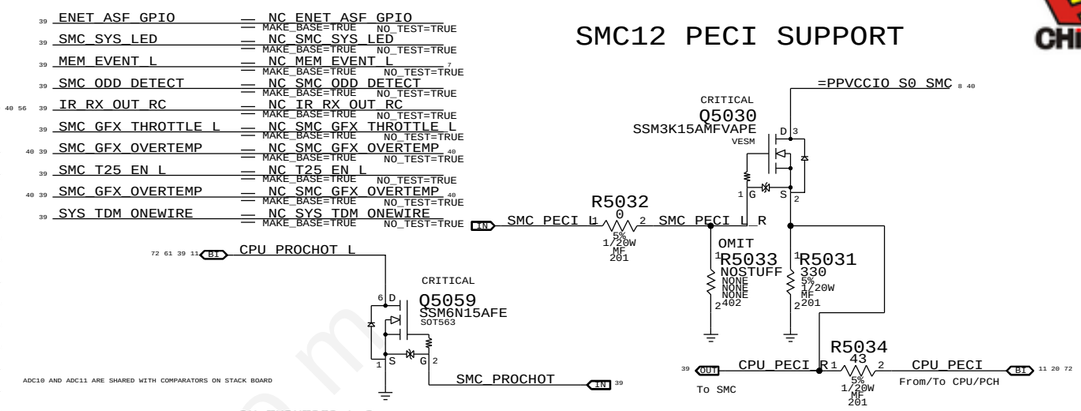


SMC_BC_ACOK	=CHGR_ACOK
NC_HISIDE_ISENSE_OC	HISIDE_ISENSE_OC
SMC_CPU_VSENSE	SMC_ADC0
SMC_CPU_ISENSE	SMC_ADC1
NC_SMC_GPU_HI_ISENSE	SMC_ADC2
SMC_DCIN_VSENSE	SMC_ADC3
SMC_DCIN_ISENSE	SMC_ADC4
SMC_PBUS_VSENSE	SMC_ADC5
SMC_SSD_ISENSE	SMC_ADC6
SMC_BMON_ISENSE	SMC_ADC7
SMC_CPU_HI_ISENSE	SMC_ADC8
SMC_OTHER_HI_ISENSE	SMC_ADC9
SMC_MEM_ISENSE	SMC_ADC10
SMC_VCCIO_ISENSE	SMC_ADC11
SMC_AXG_VSENSE	SMC_ADC12
SMC_CPU_SA_ISENSE	SMC_ADC13
SMC_CPU_SA_VSENSE	SMC_ADC14
SMC_LCD_PANEL_ISENSE	SMC_ADC15
SMC_LCDBKLT_VSENSE	SMC_ADC16
SMC_LCDBKLT_ISENSE	SMC_ADC17
SMC_AXG_ISENSE	SMC_ADC18
NC_SMC_GPU_P1V35_ISENSE	SMC_ADC19
NC_SMC_T25_ISENSE	SMC_ADC20
NC_SMC_PCH_CORE_ISENSE	SMC_ADC21
SMC_X29_ISENSE	SMC_ADC22
SMC_TBT_ISENSE	SMC_ADC23
NC_SMBUS_SMC_4_ASF_SCL	SMBUS_SMC_4_ASF_SCL
NC_SMBUS_SMC_4_ASF_SDA	SMBUS_SMC_4_ASF_SDA
NC_BDV_BKL_PWM	BDV_BKL_PWM
SDCONN_STATE_CHANGE_SMC	SMC_PME_S4_DARK_L
=TBT_WAKE_L	

NC_ENET_ASF_GPIO	ENET_ASF_GPIO
NC_SMC_SYS_LED	SMC_SYS_LED
NC_SMC_MEM_EVENT_L	MEM_EVENT_L
NC_SMC_ODD_DETECT	SMC_ODD_DETECT
NC_IR_RX_OUT_RC	IR_RX_OUT_RC
NC_SMC_GFX_THROTTLE_L	SMC_GFX_THROTTLE_L
NC_SMC_GFX_OVERTEMP	SMC_GFX_OVERTEMP
NC_T25_EN_L	SMC_T25_EN_L
NC_SMC_GFX_OVERTEMP	SMC_GFX_OVERTEMP
NC_SYS_TDM_ONEWIRE	SYS_TDM_ONEWIRE

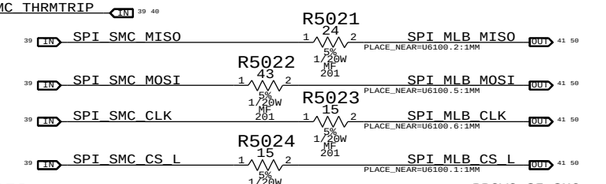
ADC10 AND ADC11 ARE SHARED WITH COMPARATORS ON STACK BOARD

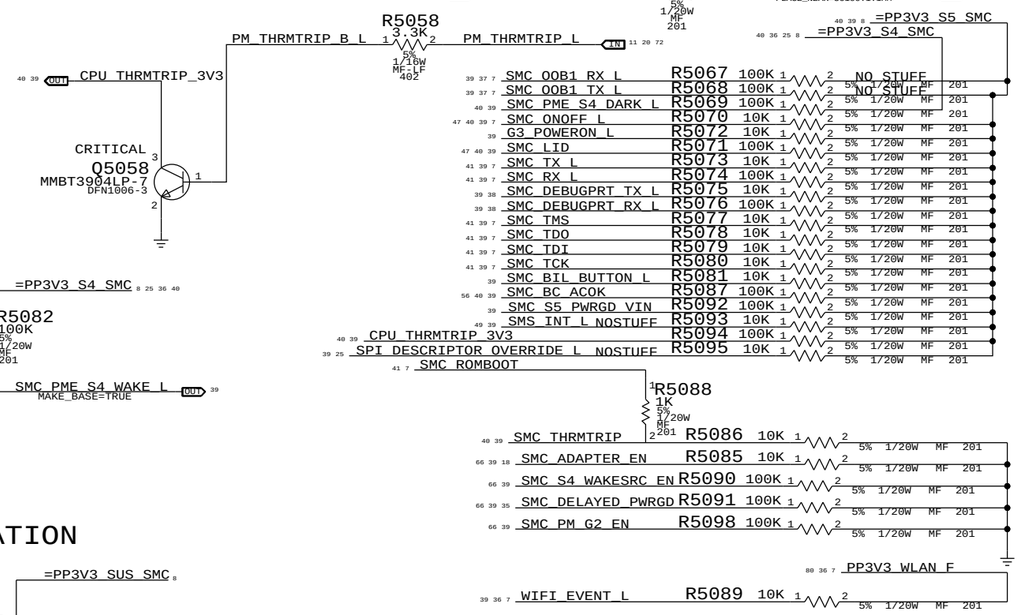
SMC12 PECI SUPPORT



SMC12 SPI SUPPORT

SERIES RESISTORS ARE NO STUFFED UNTIL THE TOPOLOGY OF 2 SPI MASTERS IS VERIFIED





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PAGE TITLE: SMC Support	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
	BRANCH: <BRANCH>
	PAGE: 50 OF 132
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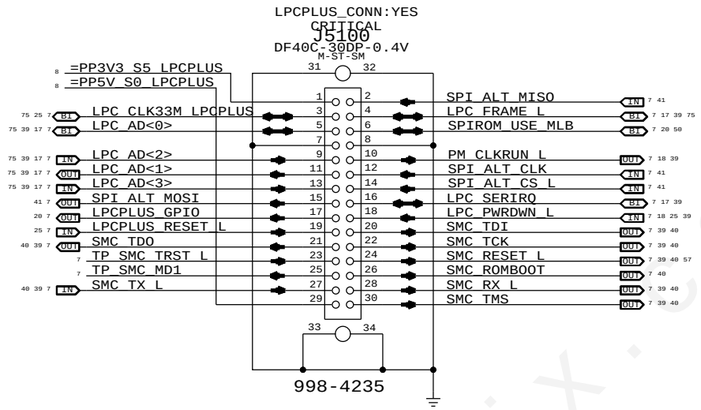
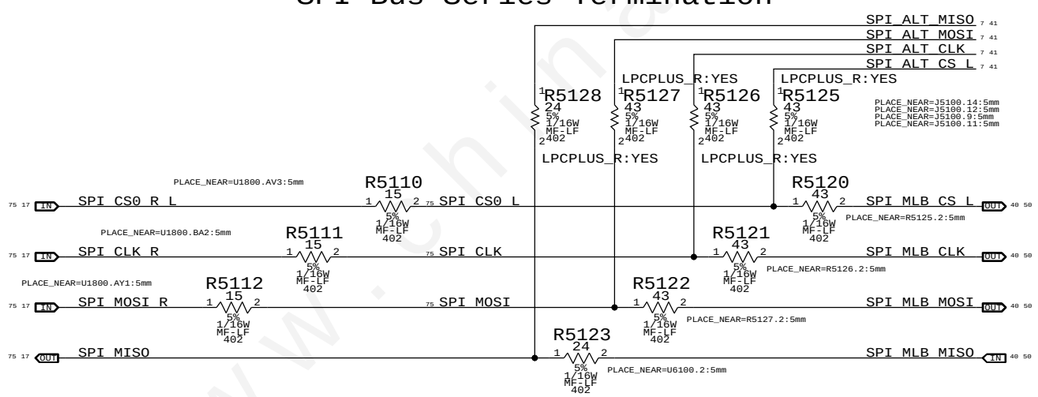
LPC+SPI Connector



SPI Bus Series Termination



SYNC_MASTER=D1_SENSORS SYNC_DATE=02/20/2012

PAGE TITLE
LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 51 OF 132
SHEET 41 OF 80

PCH SMBus "0" Connections

=PP3V3_S0_SMBUS_PCH

Panther Point
U1800
(MASTER)
SMBUS_PCH_CLK — MAKE_BASE=TRUE
SMBUS_PCH_DATA — MAKE_BASE=TRUE

R5200 1K 5% 1/20W MF 201
R5201 1K 5% 1/20W MF 201

TBT
U3600
(WRITE: 0XX READ: 0XX)
=I2C_TBTRTR_SCL
=I2C_TBTRTR_SDA

VRef DACs
U3300
(Write: 0x98 Read: 0x99)
=I2C_VREFDACS_SCL
=I2C_VREFDACS_SDA

AUDIO
U6411
(WRITE: 0X34 READ: 0X35)

Margin Control
U3301
(Write: 0x30 Read: 0x31)
=I2C_PCA9557D_SCL
=I2C_PCA9557D_SDA

AUDIO
U6410
(WRITE: 0X32 READ: 0X33)

MIKEY
U6751
(WRITE: 0X72 READ: 0X73)
=I2C_MIKEY_SCL
=I2C_MIKEY_SDA

AUDIO
U6400
(WRITE: 0XE0 READ: 0XE1)

XDP Connectors
J2500 & J2550
(MASTER)
=SMBUS_XDP_SCL
=SMBUS_XDP_SDA

AUDIO
U6750
(WRITE: 0X76 READ: 0X77)

HDMI Redriver (on RIO)
J4410
(WRITE: 0xCC READ: 0xCD)
=I2C_HDMIRDRV_SCL
=I2C_HDMIRDRV_SDA

LED BACKLIGHT
U9700
(WRITE: 0X58 READ: 0X59)
=I2C_BKL_1_SCL
=I2C_BKL_1_SDA

SMC "0" SMBus Connections

=PP3V3_S0_SMBUS_SMC_0_S0

SMC
U4900
(MASTER)
SMB_0_S0_CLK — SMBUS_SMC_0_S0_SCL — MAKE_BASE=TRUE
SMB_0_S0_DATA — SMBUS_SMC_0_S0_SDA — MAKE_BASE=TRUE

R5250 4.7K 5% 1/20W MF 201
R5251 4.7K 5% 1/20W MF 201

GPU Temp (Ext)
EMC1414-A: U5550
(Write: 0x98 Read: 0x99)
=SMBUS_GPUTHMSNS_SCL
=SMBUS_GPUTHMSNS_SDA

SMC "2" SMBUS CONNECTIONS

NOTE: SMC RMT bus remains powered and may be active in S3 state

=PP3V3_S3_SMBUS_SMC_2_S3

SMC
U4900
(MASTER)
SMB_2_S3_CLK — SMBUS_SMC_2_S3_SCL — MAKE_BASE=TRUE
SMB_2_S3_DATA — SMBUS_SMC_2_S3_SDA — MAKE_BASE=TRUE

R5270 1K 5% 1/20W MF 201
R5271 1K 5% 1/20W MF 201

Trackpad
J5800
(Write: 0x90 Read: 0x91)
=I2C_TPAD_SCL
=I2C_TPAD_SDA

ALS
J3502
(Write: 0x72 Read: 0x73)
=I2C_ALS_SCL
=I2C_ALS_SDA

SMS
U5920
(WRITE: 0X30/31 READ: 0X32/33)
=I2C_SMC_SMS_SCL
=I2C_SMC_SMS_SDA

GYRO
U5940
(WRITE: 0XD0 READ: 0XD1)
=I2C_SMC_GYRO_SCL
=I2C_SMC_GYRO_SDA

SMC "5" SMBUS CONNECTIONS

=PP3V42_G3H_SMBUS_SMC_5

SMC
U4900
(MASTER)
SMB_5_CLK — SMBUS_SMC_5_G3_SCL — MAKE_BASE=TRUE
SMB_5_DATA — SMBUS_SMC_5_G3_SDA — MAKE_BASE=TRUE

R5280 2.0K 5% 1/20W MF 201
R5281 2.0K 5% 1/20W MF 201

Battery Charger
ISL6258 - U7000
(Write: 0x12 Read: 0x13)
=SMBUS_CHGR_SCL
=SMBUS_CHGR_SDA

Battery
J6955
(See Table)
=SMBUS_BATT_SCL
=SMBUS_BATT_SDA

Battery
Battery Manager - (Write: 0x16 Read: 0x17)

SMC "3" SMBUS CONNECTIONS

=PP3V3_S3_SMBUS_SMC_3

SMC
U4900
(MASTER)
SMB_3_CLK — SMBUS_SMC_3_SCL — MAKE_BASE=TRUE
SMB_3_DATA — SMBUS_SMC_3_SDA — MAKE_BASE=TRUE

R5290 4.7K 5% 1/20W MF 201 (DEBUG_ADC)
R5291 4.7K 5% 1/20W MF 201 (DEBUG_ADC)

DEBUG SENSOR ADC A
UD000
(Write: 0x10 Read: 0x11)
=I2C_SMC_ADCS_SCL
=I2C_SMC_ADCS_SDA

PCH "SMLink 0" Connections

=PP3V3_S0_SMBUS_PCH

Panther Point
U1800
(MASTER)
SML_PCH_0_CLK — MAKE_BASE=TRUE
SML_PCH_0_DATA — MAKE_BASE=TRUE

R5210 8.2K 5% 1/20W MF 201
R5211 8.2K 5% 1/20W MF 201

SMC "1" SMBUS CONNECTIONS

=PP3V3_S0_SMBUS_SMC_1_S0

SMC
U4900
(MASTER)
SMB_1_S0_CLK — SMBUS_SMC_1_S0_SCL — MAKE_BASE=TRUE
SMB_1_S0_DATA — SMBUS_SMC_1_S0_SDA — MAKE_BASE=TRUE

R5260 1K 5% 1/20W MF 201
R5261 1K 5% 1/20W MF 201

CPU/DDR3/PCH/AIRFLOW TEMP
EMC1414-A: U5570
(Write: 0x98 Read: 0x99)
=I2C_CPUTHMSNS_SCL
=I2C_CPUTHMSNS_SDA

PCH "SMLink 1" Connections

Panther Point
U1800
(Write: 0x88 Read: 0x89)
SML_PCH_1_CLK
SML_PCH_1_DATA

SMLink 1 is slave port to access PCH & CPU via PECI.

X29 TEMP
TMP105: U5523
(WRITE: 0X92 READ: 0X93)
=I2C_X29THMSNS_SCL
=I2C_X29THMSNS_SDA

SPKR TEMP
U6420
(WRITE: 0XD8 READ: 0XD9)
U6421
(WRITE: 0X38 READ: 0X39)
=I2C_SPKRTHMSNS_SCL
=I2C_SPKRTHMSNS_SDA

SYNC_MASTER=MASTER — SYNC_DATE=MASTER

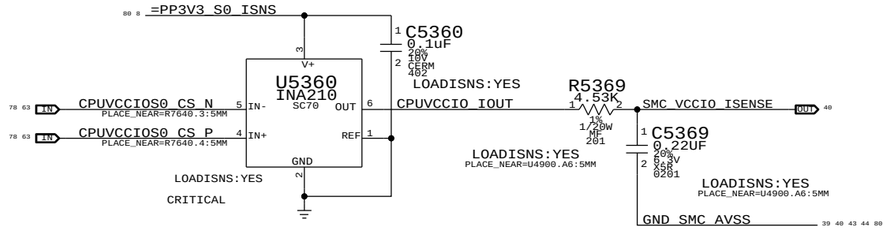
PAGE TITLE: SMBus Connections

Apple Inc.

DRAWING NUMBER: <SCH_NUM> — SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 52 OF 132
SHEET: 42 OF 80

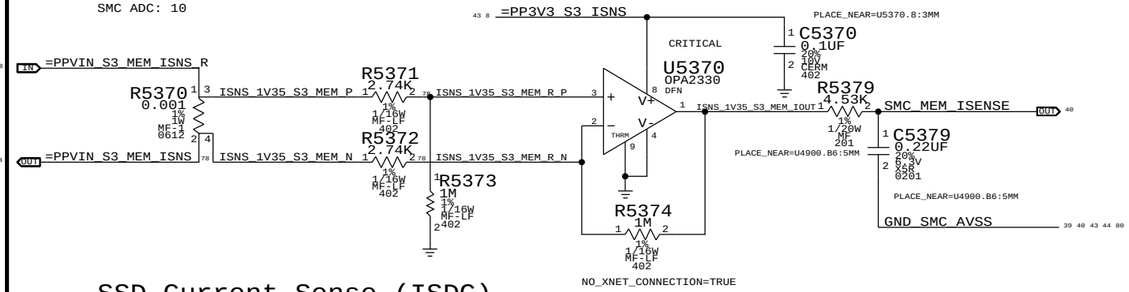
CPU/PCH VCCIO & TBT 1.05V Load Side Current Sense (IC1C)

Gain: 200x, EDP: 20 A
Rsense: 0.001 (R7640)
V across Rsense: 15 mV
SMC ADC: 11



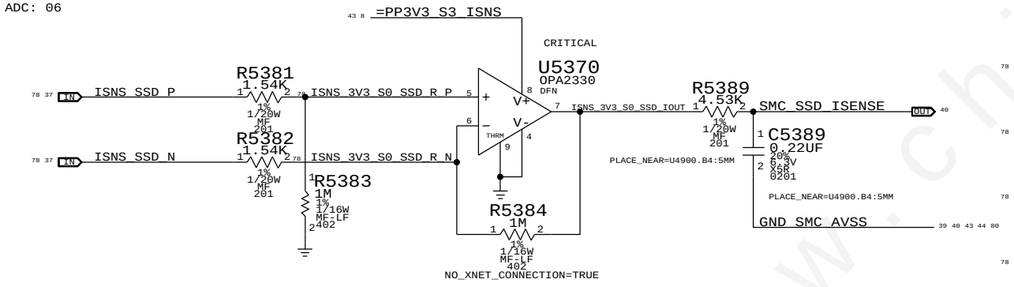
DDR 1.35V S3 (Memory) Current Sense (IM0C)

Gain: 364.9x, EDP: 9 A
Rsense: 0.001 (R5370)
V across Rsense: 9 mV
SMC ADC: 10



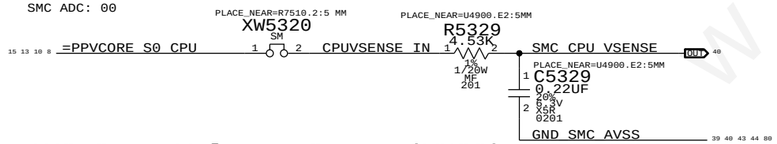
SSD Current Sense (ISDC)

Gain: 649.35x, EDP: 5 A (16.5 W)
Rsense: 0.001 (R5370)
V across Rsense: 5 mV
SMC ADC: 06



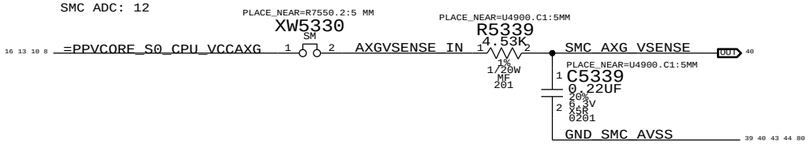
CPU Core Voltage Sense (VC0C)

Gain: 1x
SMC ADC: 00



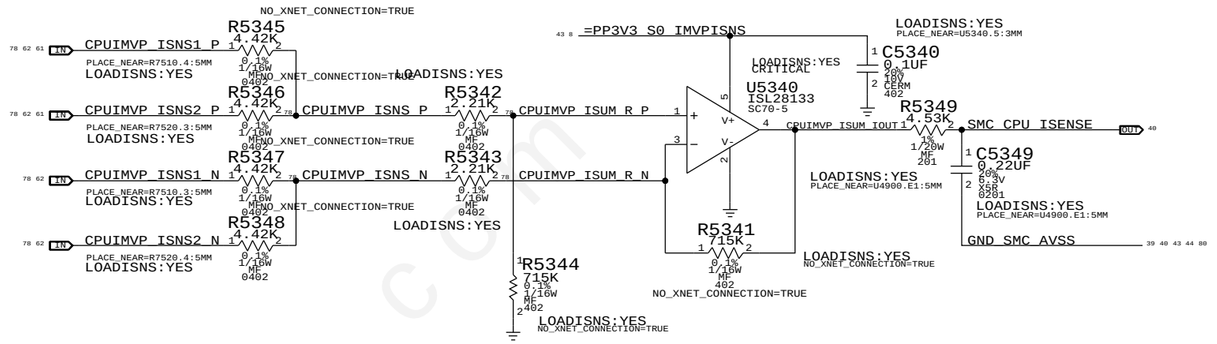
AXG Core Voltage Sense (VN0C)

Gain: 1x
SMC ADC: 12



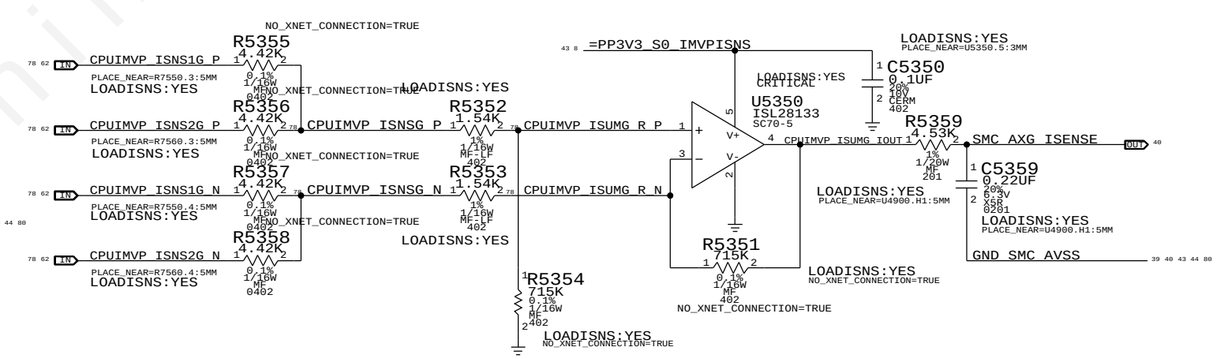
CPU Core Load Side Current Sense (IC0C)

Gain: 161.7x, EDP: 53 A
Rsense: 2x of 0.00075 (R7510, R7520), Rsum: 0.000375
V across Rsense: 19.8 mV
SMC ADC: 01



AXG Core Load Side Current Sense (IN0C)

Gain: 190.6x, EDP: 46 A
Rsense: 2x of 0.00075 (R7550, R7560), Rsum: 0.000375
V across Rsense: 17.25 mV
SMC ADC: 18



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	3	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5349,C5359,C5369		LOADISNS:NO

SYNC_MASTER=D1_SENSORS SYNC_DATE=02/20/2012

PAGE TITLE
Power Sensor: Load Side

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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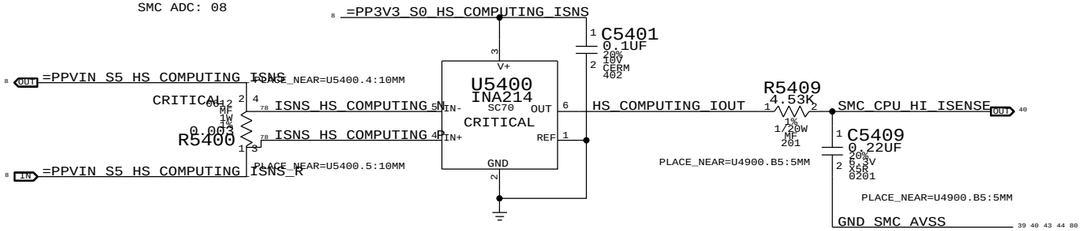
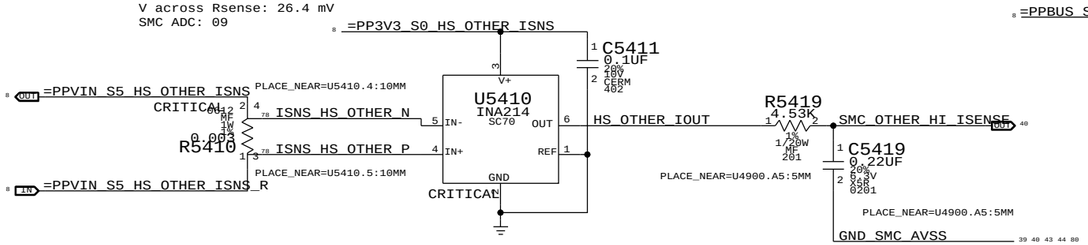
CPU High Side Current Sense (IC0R)

Gain: 50x, EDP: 17.4 A
Rsense: 0.003 (R5400)
V across Rsense: 52.2 mV
SMC ADC: 08



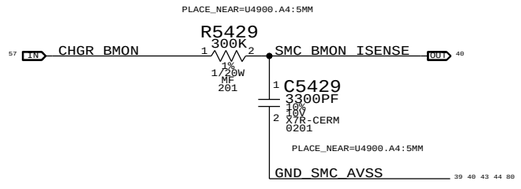
OTHER High Side Current Sense (IO0R)

Gain: 100x, EDP: 8.8 A
Rsense: 0.003 (R5410)
V across Rsense: 26.4 mV
SMC ADC: 09



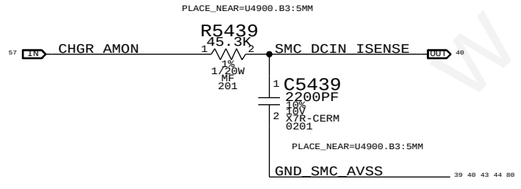
Charger (BMON Production) Current Sense (IPBR)

Charger Gain: 36x, EDP: 6.6 A
Rsense: 0.010 (R7050)
SMC ADC: 07



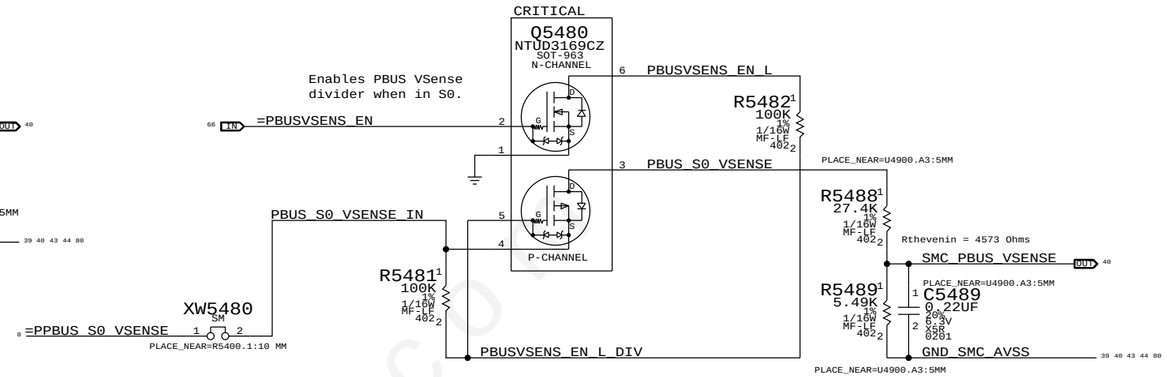
DC-In (AMON) Current Sense (ID0R)

Charger Gain: 20x, EDP: 4.6 A
Rsense: 0.020 (R7020)
SMC ADC: 04



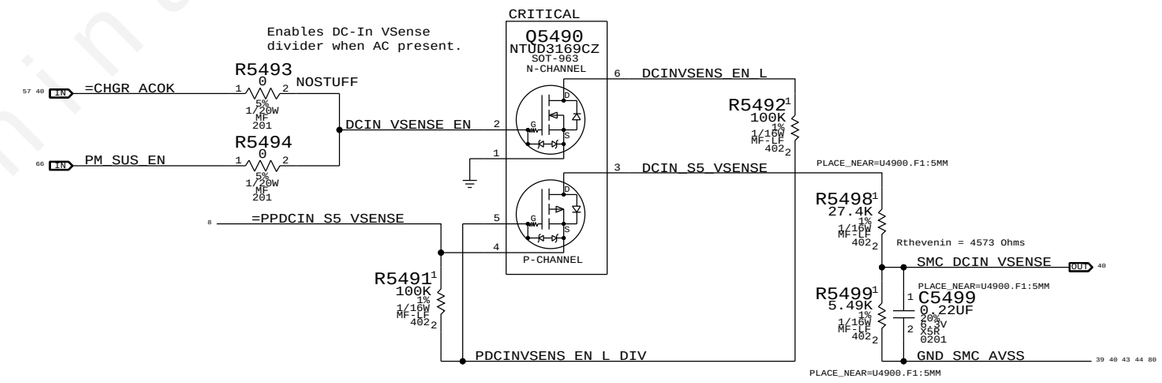
PBUS Voltage Sense & Enable (VP0R)

Gain: 0.167x
SMC ADC: 05



DC In Voltage Sense & Enable (VD0R)

Gain: 0.167x
SMC ADC: 03



SYNC_MASTER=D1_SENSORS SYNC_DATE=02/20/2012

PAGE TITLE
Power Sensor: High Side

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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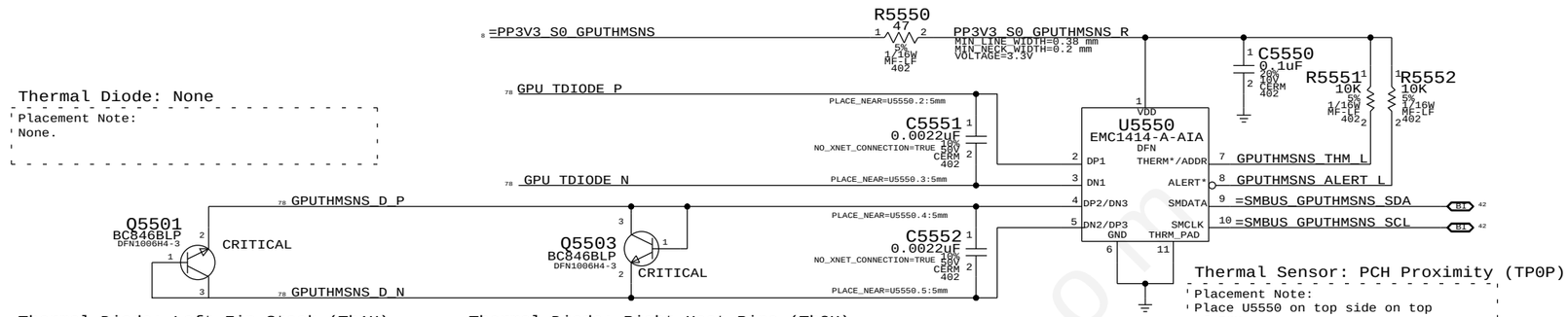
Thermal Sensor A:
PCH Proximity, Left Fin Pipe, Right Fin Stack

I2C Write: 0x98, I2C Read: 0x99



Thermal Diode: None

Placement Note:
None.

Thermal Diode: Left Fin Stack (Th1H)

Placement Note:
Place Q5501 on the top side on the corner close to the Left Fin Stack.

Thermal Diode: Right Heat Pipe (Th2H)

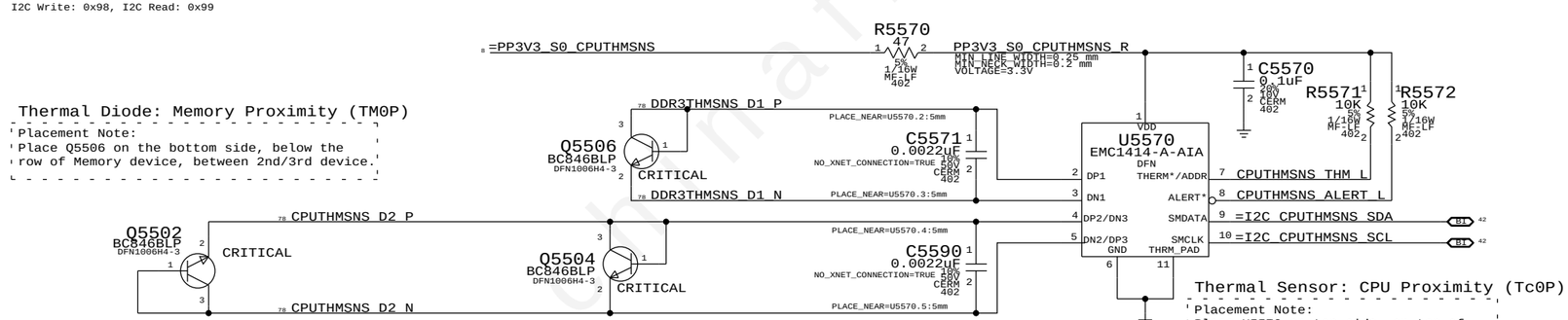
Placement Note:
Place Q5503 under the top side on the corner close to the Right Fin Stack.

Thermal Sensor: PCH Proximity (TP0P)

Placement Note:
Place U5550 on top side on top of PCH.

Thermal Sensor B:
CPU Proximity, Memory Proximity, Airflow

I2C Write: 0x98, I2C Read: 0x99



Thermal Diode: Memory Proximity (TM0P)

Placement Note:
Place Q5506 on the bottom side, below the row of Memory device, between 2nd/3rd device.

Thermal Diode: Airflow (TA0P)

Placement Note:
Place Q5502 on the bottom side, below left underneath the left fan well in the neck.

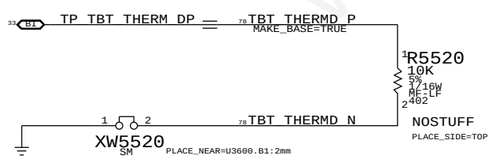
Thermal Diode: Airflow (TA1P)

Placement Note:
Place Q5504 on the either side, near LCD connector and DCIN connector.

Thermal Sensor: CPU Proximity (Tc0P)

Placement Note:
Place U5570 on top side, on top of the CPU.

Thermal Sensor: T29 Die



Note: Use GND pin B1 on U3600 for N leg.

SYNC_MASTER=D1_SENSORS SYNC_DATE=02/20/2012

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
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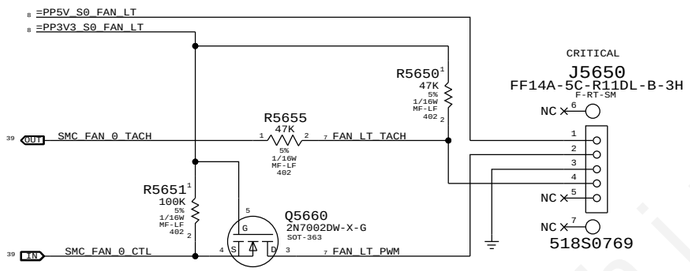
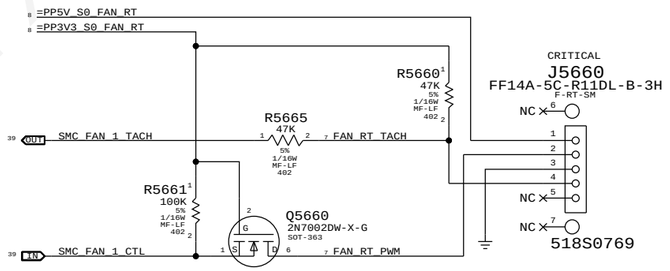
Left Fan



Right Fan



SYNC_MASTER=J5_MLB SYNC_DATE=07/29/2013

PAGE TITLE

Fan Connectors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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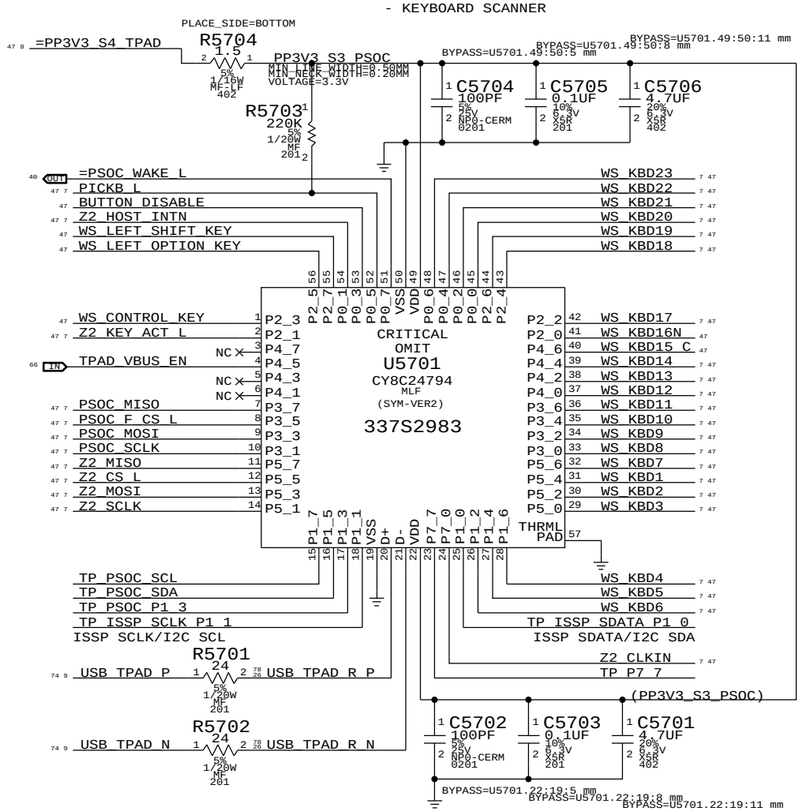
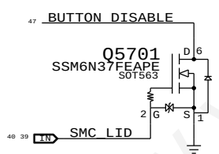
PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

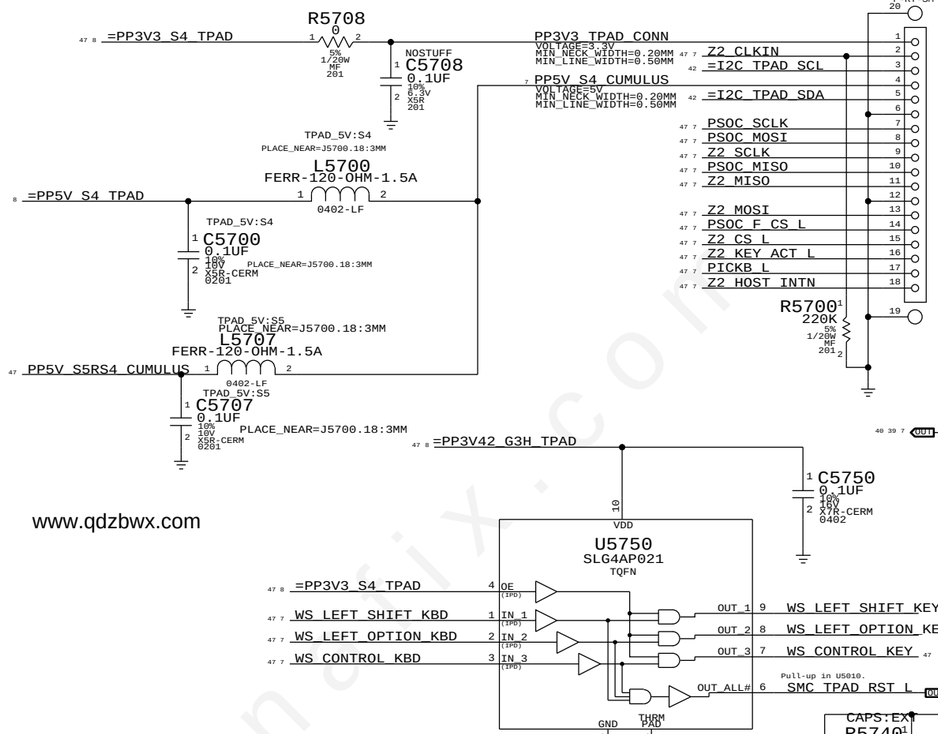
TPAD Buttons Disable



PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

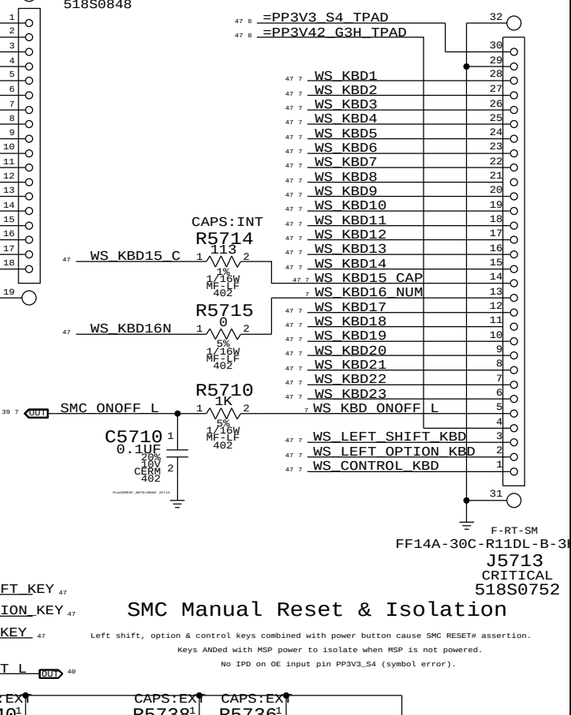
THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

IPD Flex Connector



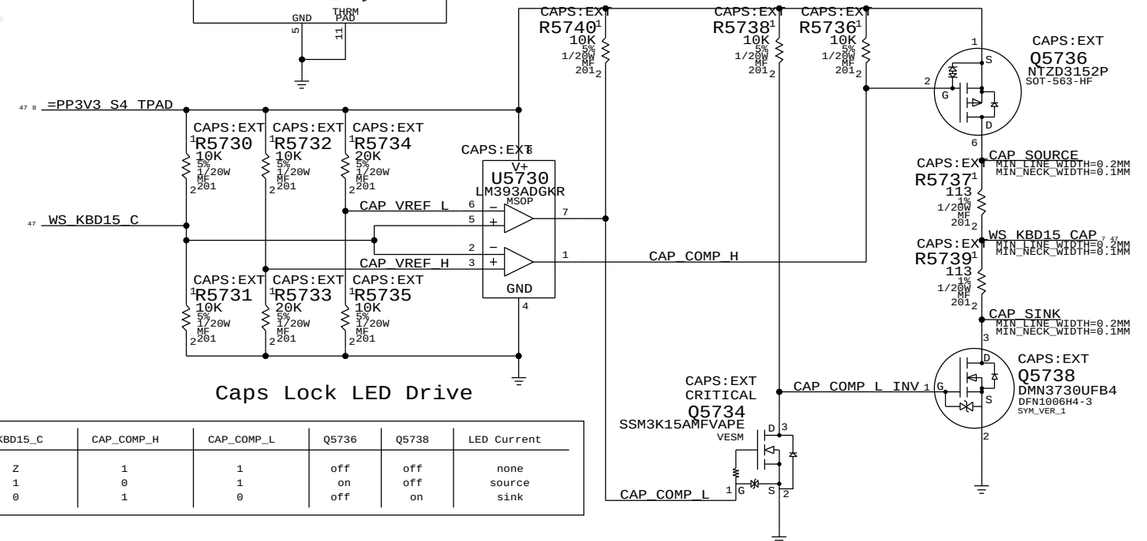
www.qdzbwx.com

Keyboard Connector



SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with MSP power to isolate when MSP is not powered.
No IPD on OE input pin PP3V3_S4 (symbol error).



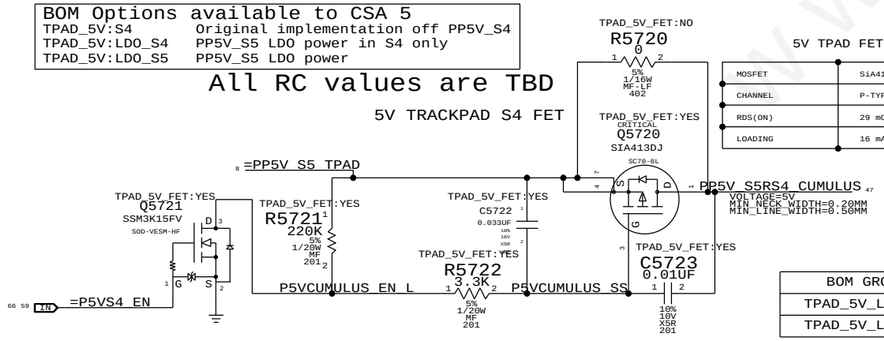
Caps Lock LED Drive

WS_KBD15_C	CAP_COMP_H	CAP_COMP_L	Q5736	Q5738	LED Current
Z	1	1	off	off	none
1	0	1	on	off	source
0	1	0	off	on	sink

BOM Options available to CSA 5	
TPAD_5V:S4	Original implementation off PP5V_S4
TPAD_5V:LDO_S4	PP5V_S5 LDO power in S4 only
TPAD_5V:LDO_S5	PP5V_S5 LDO power

All RC values are TBD

5V TRACKPAD S4 FET



5V TPAD FET	
MOSFET	SiA413
CHANNEL	P-TYPE 12V
RDS(ON)	29 mOhm @4.5V
LOADING	16 mA (EDP)

BOM GROUP	BOM OPTIONS
TPAD_5V_LDO:S4	TPAD_5V_FET:YES,TPAD_5V:S5
TPAD_5V_LDO:S5	TPAD_5V_FET:NO,TPAD_5V:S5

SYNC_MASTER=D2_MLB_KEPLER
SYNC_DATE=12/08/2011

PAGE TITLE

KEYBOARD/TRACKPAD (1 OF 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM>
SIZE D
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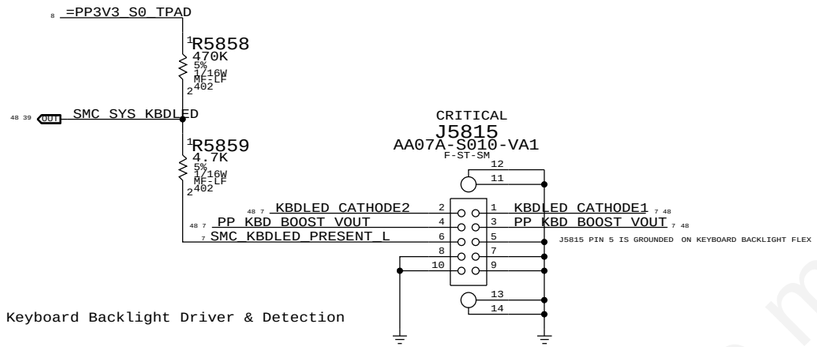


Keyboard Backlight Driver & Detection

To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:

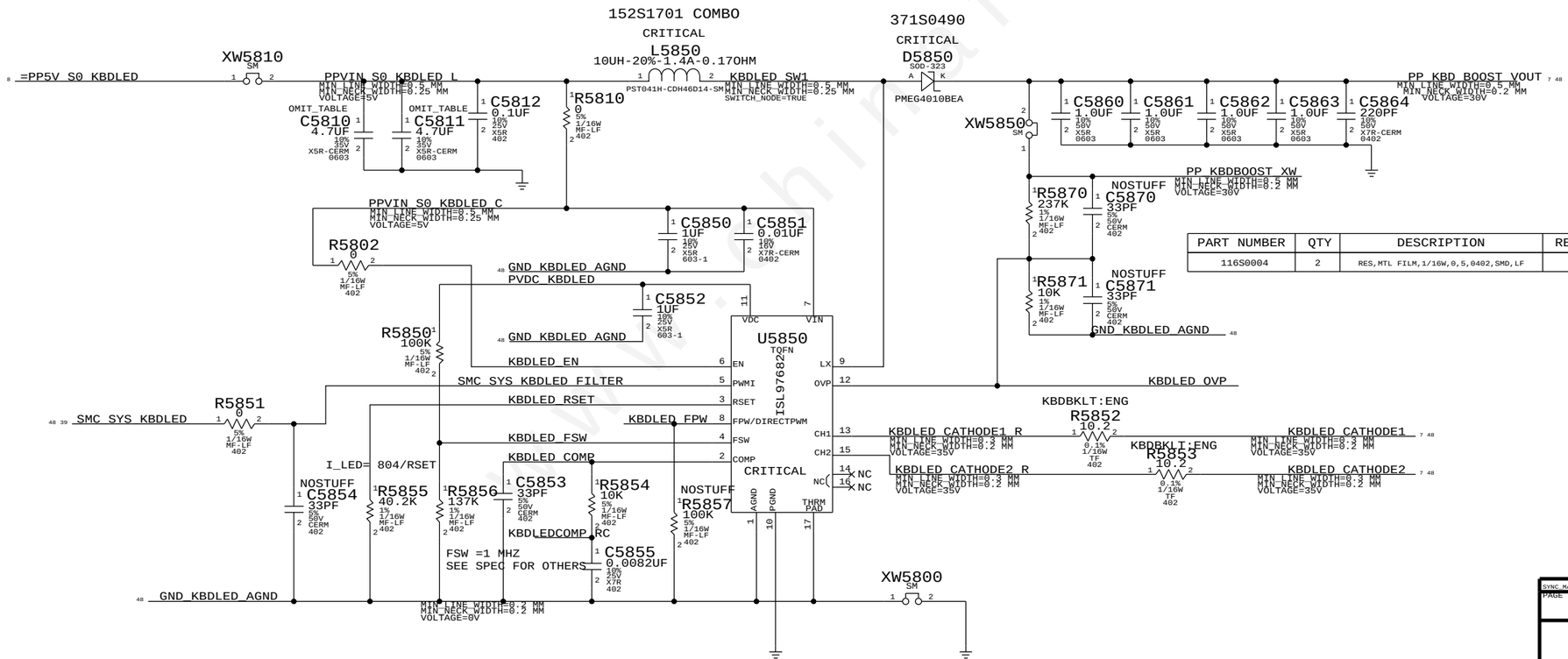
If LOW, keyboard backlight present

If HIGH, keyboard backlight not present

516S0899

Keyboard Backlight Connector

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	2	CAP,CER,4.7UF,10%,25V,X6S,0603	C5810,C5811	CRITICAL	



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,1/16W,0,5,0402,SMD,LF	R5852,R5853	CRITICAL	KBDBKLT:PROD

SYNC_MASTER=D2_MLB_KEPLER SYNC_DATE=12/08/2011

PAGE TITLE

KEYBOARD/TRACKPAD (2 OF 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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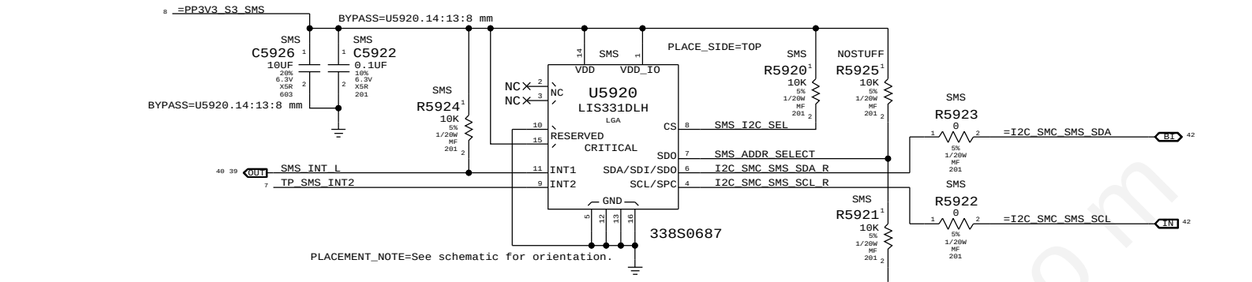
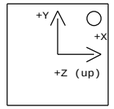
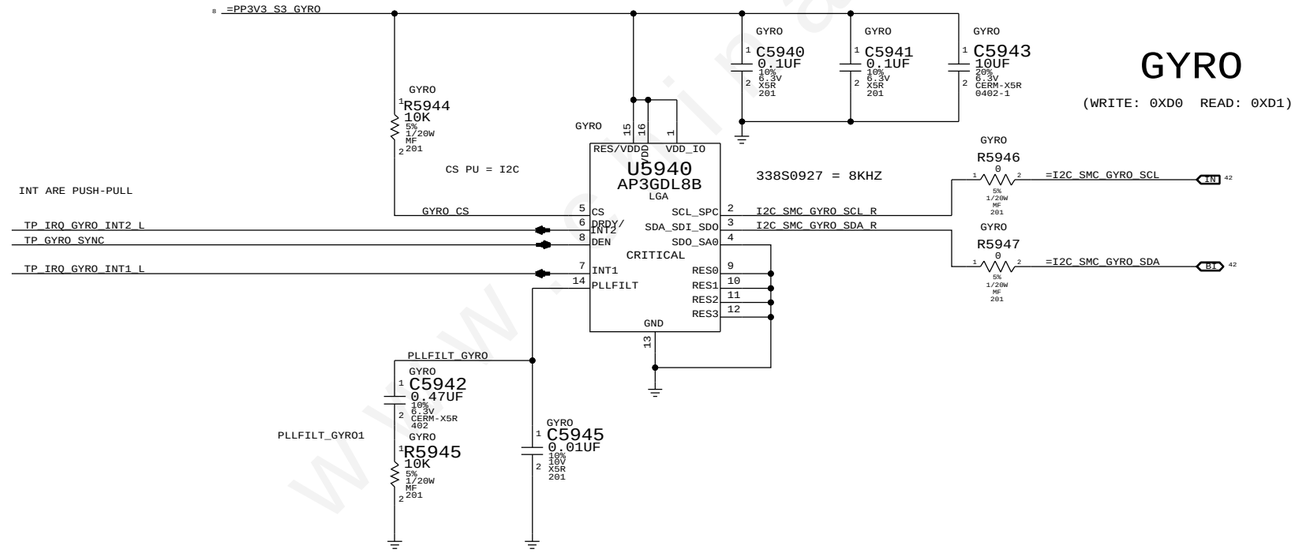


Desired orientation when placed on top-side (view top):



Front of system

Circle indicates pin 1 location when placed in correct orientation



GYRO

(WRITE: 0XD0 READ: 0XD1)

SYNC_MASTER=J5_MLB SYNC_DATE=07/29/2011

PAGE TITLE: DIGITAL ACCELEROMETER & GYRO

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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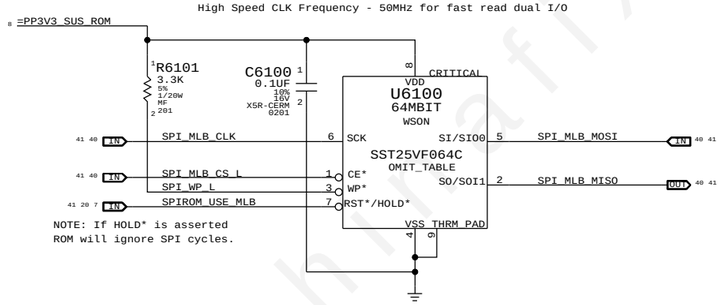
DUAL I/O MODE (MODE 0 & 3) SUPPORTED
High Speed CLK Frequency - 50MHz for fast read dual I/O



NOTE: If HOLD* is asserted
ROM will ignore SPI cycles.

SYNC_MASTER=J13_MLB SYNC_DATE=01/20/2012

PAGE TITLE
SPI ROM

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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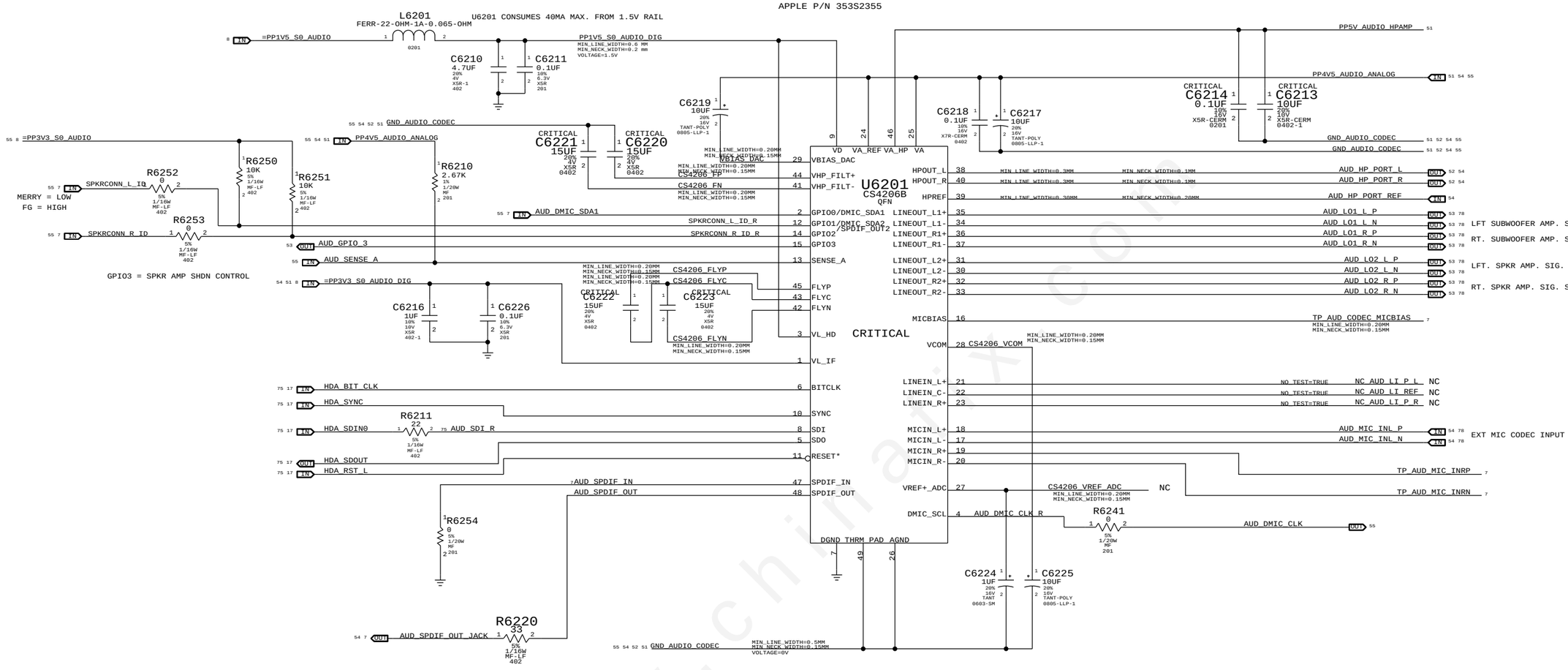
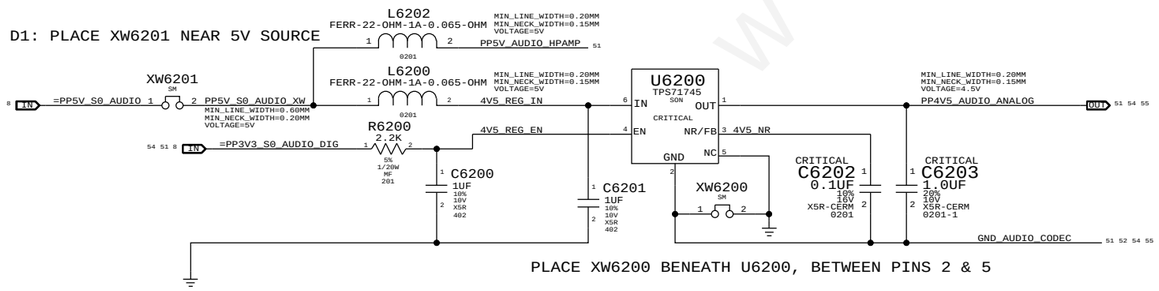
AUDIO CODEC

APPLE P/N 353S2355



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456



NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC_MASTER=D1_AUDIO SYNC_DATE=06/06/2012

PAGE TITLE

AUDIO: CODEC/REGULATOR

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
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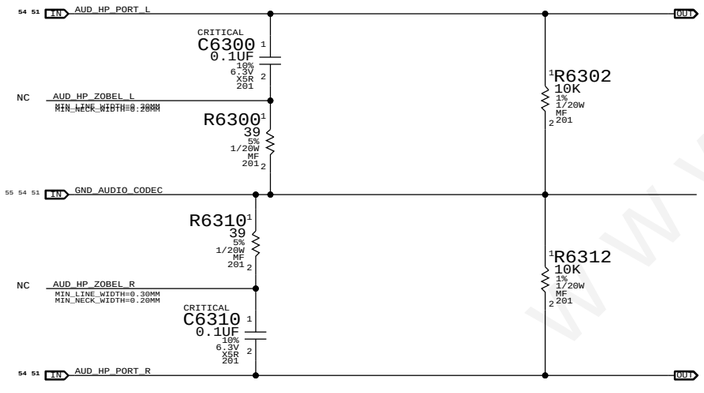
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



SYNC_MASTER=D1_AUDIO SYNC_DATE=06/06/2012

PAGE TITLE

AUDIO: HEADPHONE FILTER

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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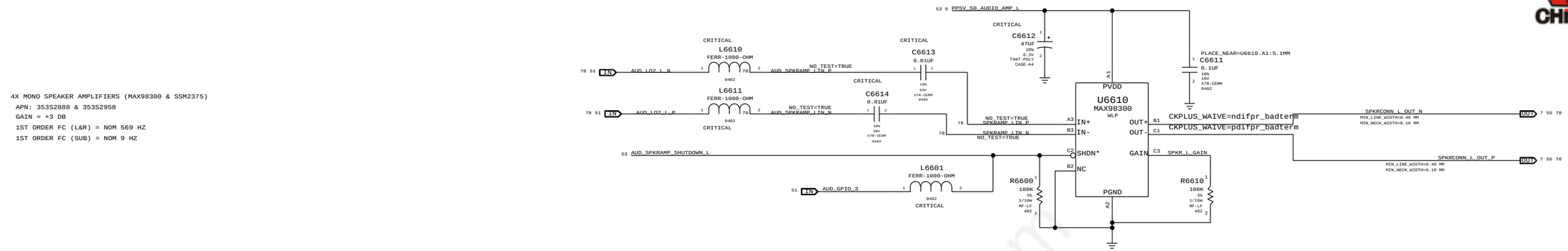
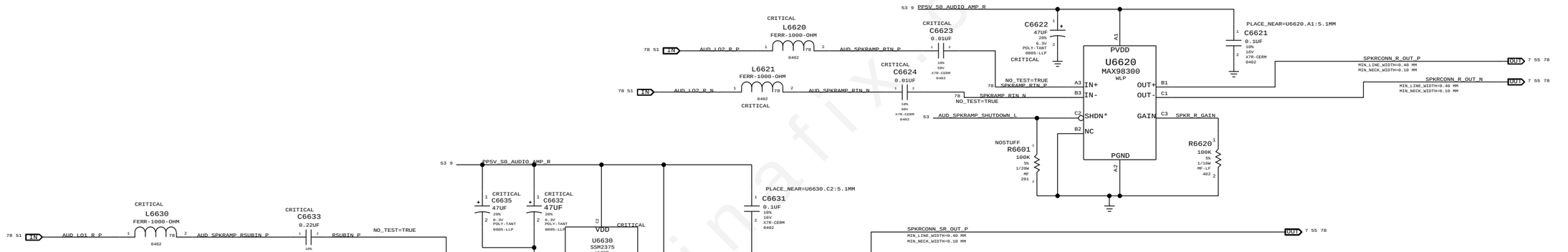
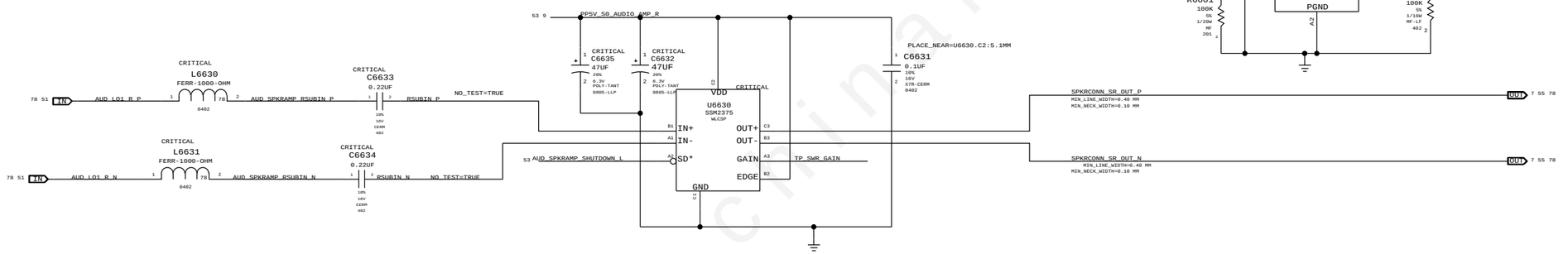
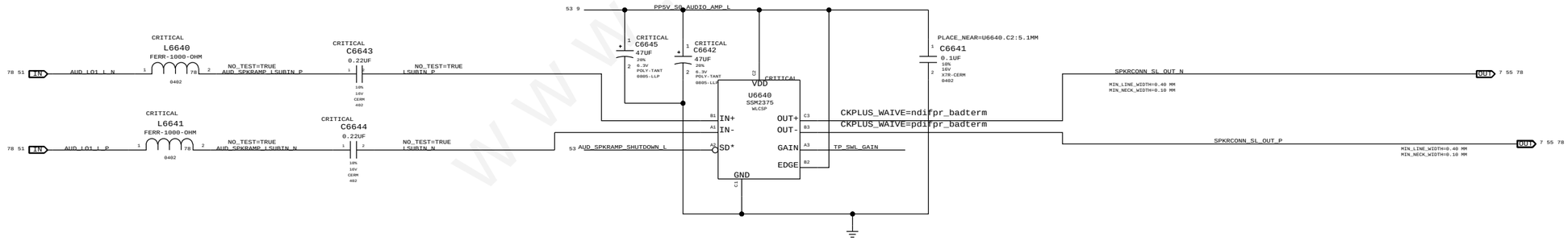
SHEET 52 OF 80

4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ









SYNC_MASTER=D1_AUDIO SYNC_DATE=06/06/2013

PAGE TITLE
AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 66 OF 132
SHEET 53 OF 80

AUDIO JACK: HP CONNECTOR WITH MIKEY & CHS

PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=10.63KHZ

MIKEY 1A
APN:353S2640
MIKEY ADDRESS: WRITE=72H, READ=73H

I2C PULLUPS ON SOUTHBRIDGE PAGE

PP4V5_AUDIO_ANALOG
=PP3V3_S0_AUDIO_DIG
=I2C_MIKEY_SCL
=I2C_MIKEY_SDA
AUD_I2C_INT_L
AUD_IPHS_SWITCH_EN
AUD_PORTA_DET_L
HS_HDET
AUDIO_SCL
AUDIO_SDA
GND_AUDIO_CODEC

R6762 10K 5% 1/20W MF 201
R6757 33 5% 1/20W MF 201
R6758 33 5% 1/20W MF 201
R6761 NOSTUFF 47K 5% 1/20W MF 201
R6755 100K 5% 1/20W MF 201
C6755 CRITICAL 4.7UF 20% 6.3V X5R-CERM1 402

U6751 CD3282A1 WCSP
AVDD A2
SCL C3
SDA B3
INT* D3
ENABLE A3
HDET A1
CS B2
MICBIAS C1
DETECT B1
BYPASS D1
DGND C2
AGND D2

HS_MIC_BIAS
HS_SW_DET
HS_RX_BP
NO_XNET_CONNECTION=TRUE
R6754 1K 5% 1/20W MF 201
C6756 0.01UF 10% 16V X5R-CERM 0201

L6754 FERR-22-OHM-1A-0.065-OHM 0201
=PP3V42_G3H_AUDIO
PP3V42_G3H_AUDIO_LC
MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM VOLTAGE=3.42V
C6790 1UF 10% 16V X5R 402
C6754 0.1UF 10% 16V X5R-CERM 0201
GND_AUDIO_CODEC

U6750 TS3A8235YFP WCSP CRITICAL
VDD A1
RAMPI D4
RAMPO D3
CLAMPI C4
CLAMPO B4
MIC D2
REF D1
SCL B3
SDA A4
ADDR A2
GND1 C2
GND2 B2
GND C3
MIC1 B1
MIC2 C1

CHS_CLAMPI
CHS_CLAMPO
HS_MIC_HI
HS_MIC_LO
AUDIO_SCL
AUDIO_SDA
US_HS_GND
CH_HS_GND

R6751 1K 5% 1/20W MF 201
R6752 2.2K 1% 1/20W MF 201
R6753 2.2K 1% 1/20W MF 201
C6751 10UF 20% 10V X5R-CERM 0402-1
C6791 10UF 20% 10V X5R-CERM 0402-1

C6752 CRITICAL 0.1UF 10% 6.3V X5R 201
C6753 CRITICAL 0.1UF 10% 6.3V X5R 201
R6750 2.2K 5% 1/20W MF 201
R6756 100K 5% 1/20W MF 201
C6750 CRITICAL 6800PF 10% 10V X5R-X7R-CERM 201
C6758 CRITICAL 27PF 5% 25V NP0-C0G 0201
R6759 0 5% 1/20W MF 201
R6760 47K 5% 1/20W MF 201 NOSTUFF
XW6751 3M
AUD_HP_PORT_REF
PLACE_NEAR=U6750.D1:5.1MM
NO_XNET_CONNECTION=TRUE

R/C6750 FILTER TO ADDRESS OUT-OF-BAND NOISE ISSUE SEEN ON EARLY HEADSETS (SEE RADAR # 6210118)

L6701 CRITICAL FERR-33-OHM-0.8A-0.09-OHM 0201
US_HS_MIC
AUD_CONN_MIC

L6700 CRITICAL 120-OHM-25%-1.3A 0402
US_HS_GND
AUD_CONN_SLEEVE_XW
MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.06MM
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM

L6702 CRITICAL 120-OHM-25%-1.3A 0402
CH_HS_GND
AUD_CONN_MIC_XW
MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.06MM
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM

=PP3V3_S0_AUDIO_DIG
AUD_SPDIF_OUT_JACK
AUD_TIPDET_INV

APN:510S0009
J6701 CRITICAL 51138-0274 F-ST-SM

L6704 CRITICAL 120-OHM-25%-1.3A 0402
AUD_HP_PORT_R
AUD_CONN_HP_LEFT
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.1MM
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.1MM

L6703 CRITICAL FERR-33-OHM-0.8A-0.09-OHM 0201
CH_HS_MIC
AUD_CONN_SLEEVE

L6705 CRITICAL 120-OHM-25%-1.3A 0402
AUD_HP_PORT_R
AUD_CONN_HP_RIGHT
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.1MM
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.1MM

L6706 CRITICAL FERR-470-OHM 0201
AUD_TYPEDET
AUD_CONN_TYPEDET

I2C ADDRESSES

MIKEY	U6751	READ	0111 0011	0X73
MIKEY	U6751	WRITE	0111 0010	0X72
CHS	U6750	READ	0111 0111	0X77
CHS	U6750	WRITE	0111 0110	0X76

SYNC_MASTER=D1_AUDIO SYNC_DATE=06/06/2012

PAGE TITLE: AUDIO: JACK

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 67 OF 132
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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	0X09 (B)
TWEETERS	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0C (A)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
DMIC 1	0X06 (6)	0X0E (0,E)	3V3	N/A
DMIC2	0X05 (5)	0X12 (12,C)	3V3	0X0C (12,C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

SYSTEM INT AND GPIO LINES

FUNCTION	INT	GPIO
MIKEY ENABLE		SATA4GP/GPIO 16
MIKEY INTERRUPT	PIRQ H	GPIO 5
PERIPHERAL DETECT	PIRQ F	GPIO 3

2-MIC CONNECTOR

MIN_LINE_WIDTH=0.40MM
MIN_NECK_WIDTH=0.15MM
VOLTAGE=3.3V

55 51 8 =PP3V3_S0_AUDIO
R6885 0 5% 1/16W MF-LF 402
CON_DMIC_PWR
51 7 OUT AUD_DMIC_SDA1
R6884 0 5% 1/16W MF-LF 402
CON_DMIC_SDA1
51 OUT AUD_DMIC_CLK
R6883 0 5% 1/16W MF-LF 402
CON_DMIC_CLK

CRITICAL
J6801
FF14A-6C-R11DL-B-3H
F-RT-SM
NC 7
NC 8
1 2 3 4 5 6

SPEAKER CONNECTOR

HP=80HZ

APN: 518S0627

CRITICAL
J6802
78171-6006
M-RT-SM

78 53 7 IN SPKRCONN_L_OUT_P
78 53 7 IN SPKRCONN_L_OUT_N
55 51 7 OUT SPKRCONN_L_ID
78 53 7 IN SPKRCONN_SL_OUT_P
78 53 7 IN SPKRCONN_SL_OUT_N

CRITICAL
J6803
78171-6006
M-RT-SM

78 53 7 IN SPKRCONN_R_OUT_P
78 53 7 IN SPKRCONN_R_OUT_N
55 51 7 OUT SPKRCONN_R_ID
78 53 7 IN SPKRCONN_SR_OUT_P
78 53 7 IN SPKRCONN_SR_OUT_N

PORT B DETECT(SPDIF DELEGATE)

PORT A DETECT (HEADPHONES)

55 51 OUT AUD_SENSE_A
R6896 20.0K 1% 1/16W MF-LF 2402
AUD_PORTA_DET_L 54
R6895 39.2K 1% 1/16W MF-LF 2402
AUD_PORTB_DET_L NC

Q6897 SSM6N15AFE SOT563
AUD_OUTJACK_INSERT_L
55 IN

AUD_TYPEDET_OD OUT 55
55 54 52 51 GND_AUDIO_CODEC
R6802 100K 5% 1/20W MF 201

PP4V5_AUDIO_ANALOG
R6801 150K 1% 1/20W MF 201
Q6800 DMC2400UV SOT563 P-CHN
AUD_TYPEDET IN 54

55 54 51 PP4V5_AUDIO_ANALOG
R6803 100K 5% 1/20W MF 201
AUD_TYPEDET_OD_INV
C6800 0.1UF 10% 6.3V X5R 201
PLACE_NEAR=Q6800.4:5.1MM
Q6800 DMC2400UV SOT563 N-CHN
AUD_TYPEDET_OD IN 55
PP4V5_AUDIO_ANALOG 51 54 55
GND_AUDIO_CODEC 51 52 54 55

55 8 =PP5V_S4_AUDIO
SPEAKERID R6810 100K 1% 1/16W MF-LF 402
SPEAKERID R6811 100K 1% 1/16W MF-LF 402
55 51 7 IN SPKRCONN_L_ID
SPKRCONN_R_ID IN 7 51 55
R6812 100K 1% 1/16W MF-LF 402
R6813 100K 1% 1/16W MF-LF 402

SPEAKERID R6816 100K 1% 1/16W MF-LF 402
55 8 =PP5V_S4_AUDIO
SPEAKERID C6810 0.1UF 10% 6.3V X5R 201
SPEAKERID CRITICAL U6800 MCP6541T SC70-5
MCP6514_POS 3
MCP6514_NEG 4
MCP6514_OUT 1
SPEAKERID L6802 FERR-1000-OHM 0402
SPKR_MATCH_DRV_R 1
SPEAKERID R6820 33 5% 1/16W MF-LF 402
SPKR_MATCH_DRV 2

55 8 =PP5V_S4_AUDIO
SPEAKERID R6814 274K 1% 1/16W MF-LF 402
SPEAKERID R6815 90.9K 1% 1/16W MF-LF 402
SPEAKERID C6811 4.7UF 20% 10V X5R-CERM 0402
SPEAKERID R6817 45.3K 1% 1/16W MF-LF 402

PORT C DETECT(SPEAKER MISMATCH)

55 51 OUT AUD_SENSE_A
SPEAKERID R6894 10K 1% 1/16W MF-LF 402
NC AUD_PORTC_DET_L
SPEAKERID Q6896 SSM6N15AFE SOT563
55 54 52 51 GND_AUDIO_CODEC

55 51 8 =PP3V3_S0_AUDIO
R6867 0 5% 1/16W MF-LF 402
AUD_IP_PERIPHERAL_DET OUT 19
EXTRACTION NOTIFICATION

R6865 47K 5% 1/20W MF 201
R6866 475K 1% 1/20W MF 201
APN:376S0613
AUD_TIPDET_FET1
AUD_OUTJACK_INSERT_L OUT 55

Q6803 SSM6N15AFE SOT563
54 IN AUD_TIPDET_INV
R6892 1.5K 1% 1/10W MF-LF 402
AUD_TIPDET_INV_R
C6860 1UF 10% 25V X5R 402
CRITICAL
L6801 FERR-33-OHM-0.8A-0.09-OHM 0201
AUD_TIPDET_FET2
C6891 1UF 10% 25V X5R 402
55 54 52 51 GND_AUDIO_CODEC

NOM R6892-C6860 FC = 106Hz
SSM6N15FE Vth = 0.8V to 1.5V
SSM6N15FE IGSS = +/-1uA
FLEX-SIDE RPULLDOWN = 100k (TB 49.9k in REV 3)

AUDIO CONNECTOR DETECT STATES

	NOTHING	SPDIF	HEADPHONE
AUD_J1_TYPEDET_R	1	1	0
AUD_J1_TIPDET_R	0	1	1
AUD_OUTJACK_INSERT_L	1	0	0
AUD_SENSE_A	1	20K/2.67K RDIV	39.2K/2.67K RDIV

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S3452	353S1286		U6800	MAXIM ALT TO MICROCHIP
376S0975	376S1081		Q6800	TOSHIBA ALT TO DIODES

SYNC_MASTER=D1_AUDIO SYNC_DATE=06/06/2012

PAGE TITLE
AUDIO: JACK TRANSLATORS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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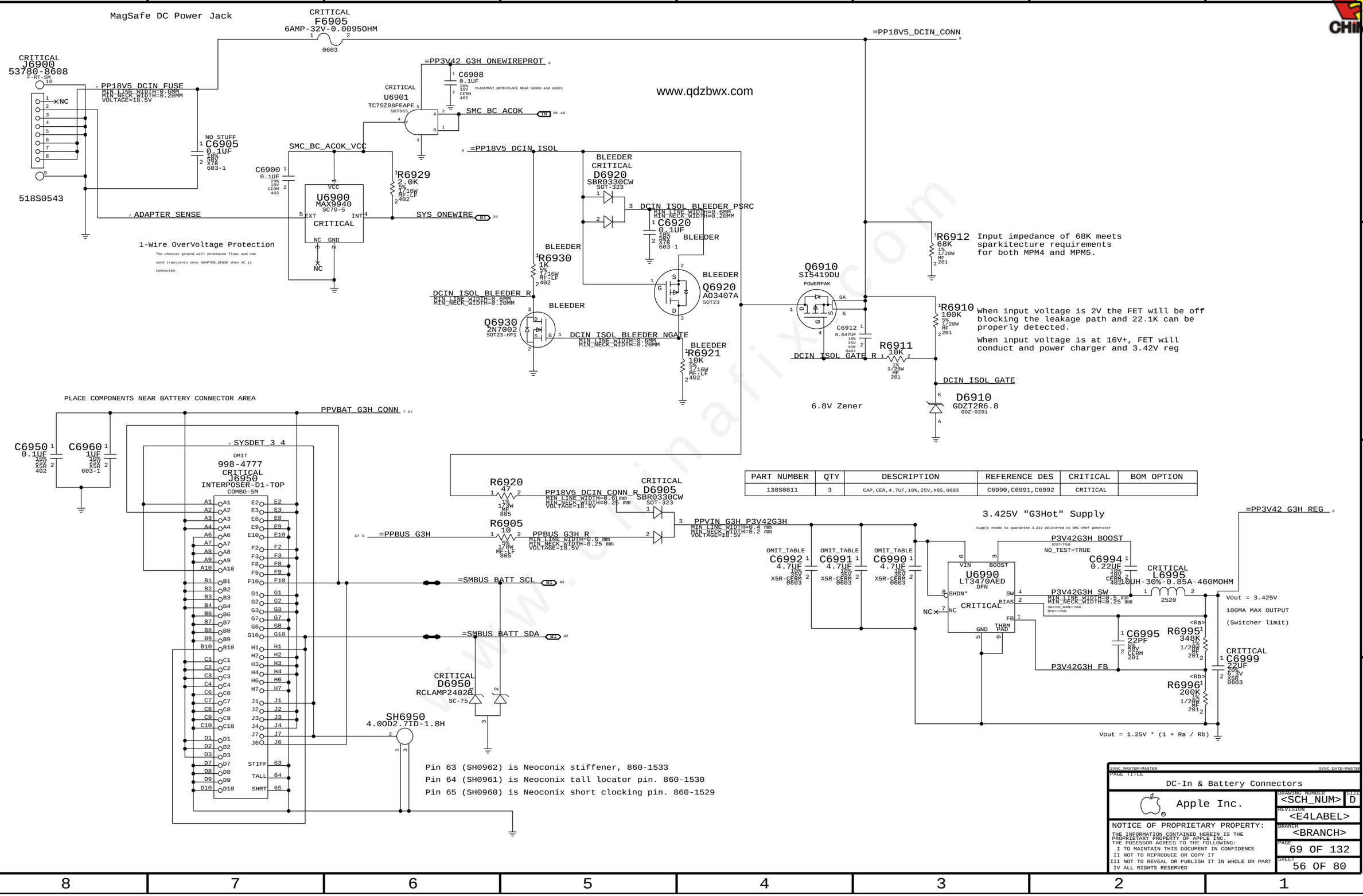

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	3	CAP,CER,4.7UF,10%,25V,X6S,0603	C6990,C6991,C6992	CRITICAL	

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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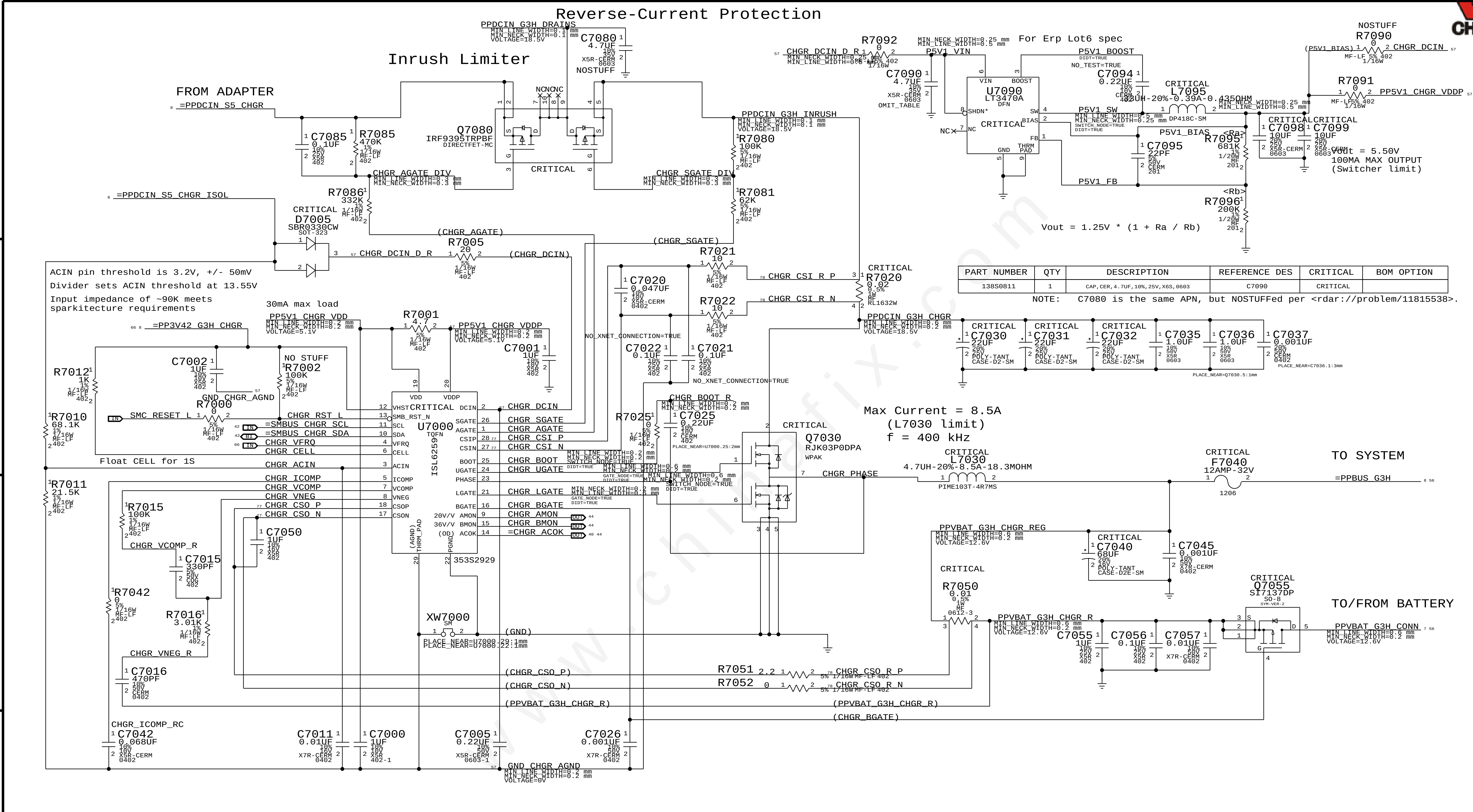


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	1	CAP,CER,4.7UF,10%,25V,X6S,0603	C7090	CRITICAL	

NOTE: C7080 is the same APN, but NOSTUFFed per <rdar://problem/11815538>.

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: PBus Supply & Battery Charger

Apple Inc.

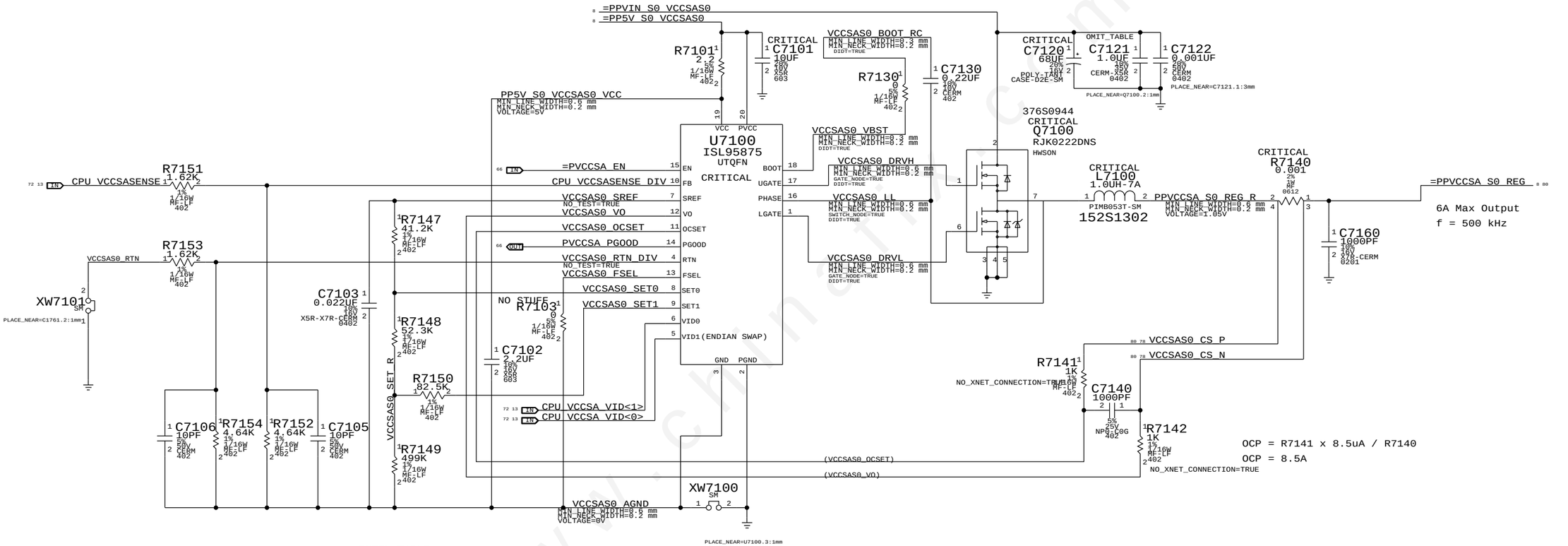
DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

System Agent Power Supply

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	1	CAP,CER,1UF,10%,35V,X6S,0402,MURATA	C7121	CRITICAL	



INTEL TABLE:

VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V
0	1	0.725V
1	1	0.675V

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: System Agent Supply

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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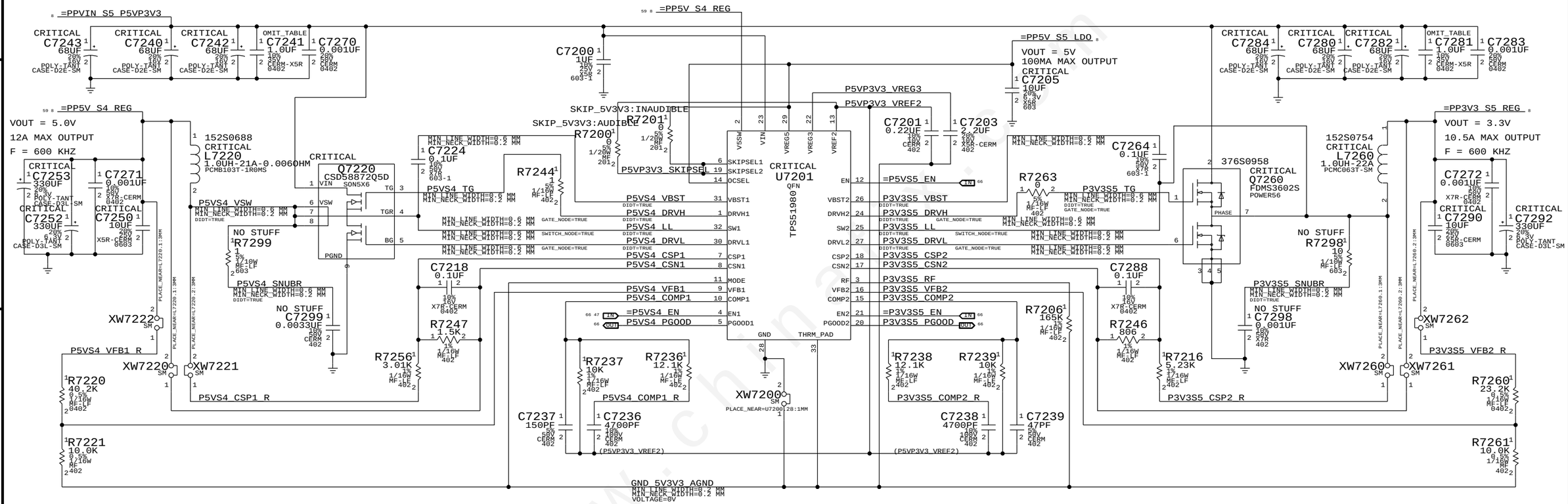
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	2	CAP,CER,1UF,10%,35V,X6S,0402,MURATA	C7241,C7281	CRITICAL	



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

5V / 3.3V Power Supply

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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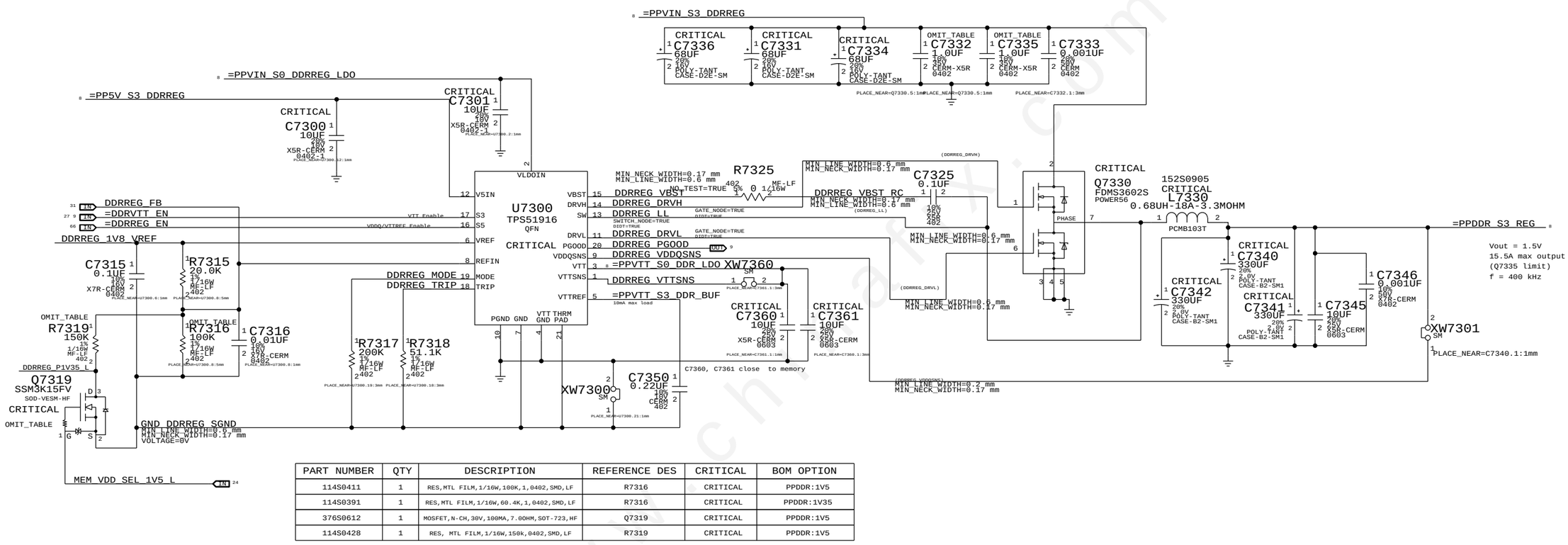
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	2	CAP,CER,1UF,10%,35V,X6S,0402,MURATA	C7332,C7335	CRITICAL	

DDR3 (1V5R1V35 S3) REGULATOR



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0411	1	RES,MTL FILM,1/16W,100K,1,0402,SMD,LF	R7316	CRITICAL	PPDDR:1V5
114S0391	1	RES,MTL FILM,1/16W,60.4K,1,0402,SMD,LF	R7316	CRITICAL	PPDDR:1V35
376S0612	1	MOSFET,N-CH,30V,100MA,7.0OHM,SOT-723,HF	Q7319	CRITICAL	PPDDR:1V5
114S0428	1	RES, MTL FILM,1/16W,150k,0402,SMD,LF	R7319	CRITICAL	PPDDR:1V5

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: 1.5V DDR3 Supply

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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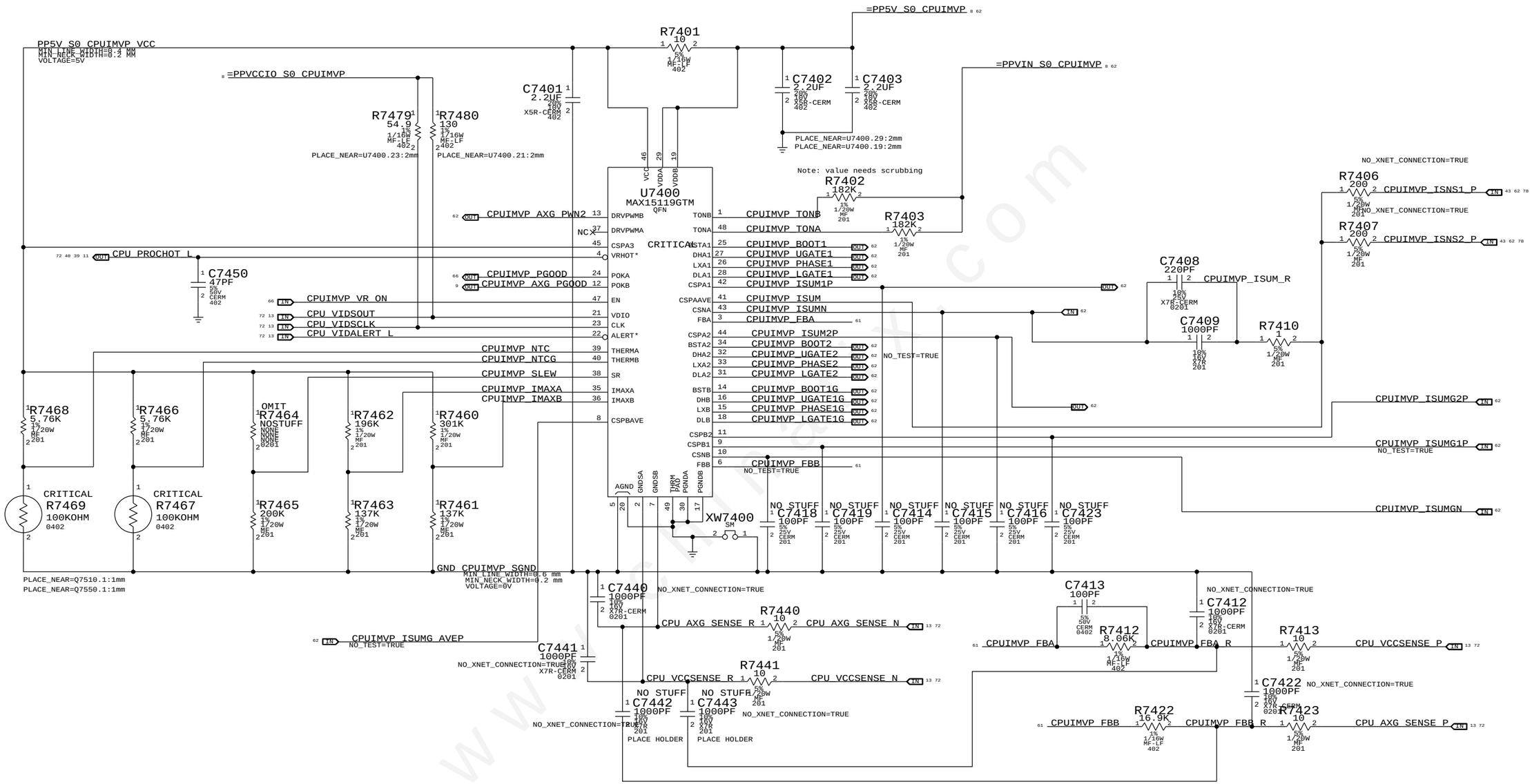

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: CPU IMVP7 & AXG VCore Regulator

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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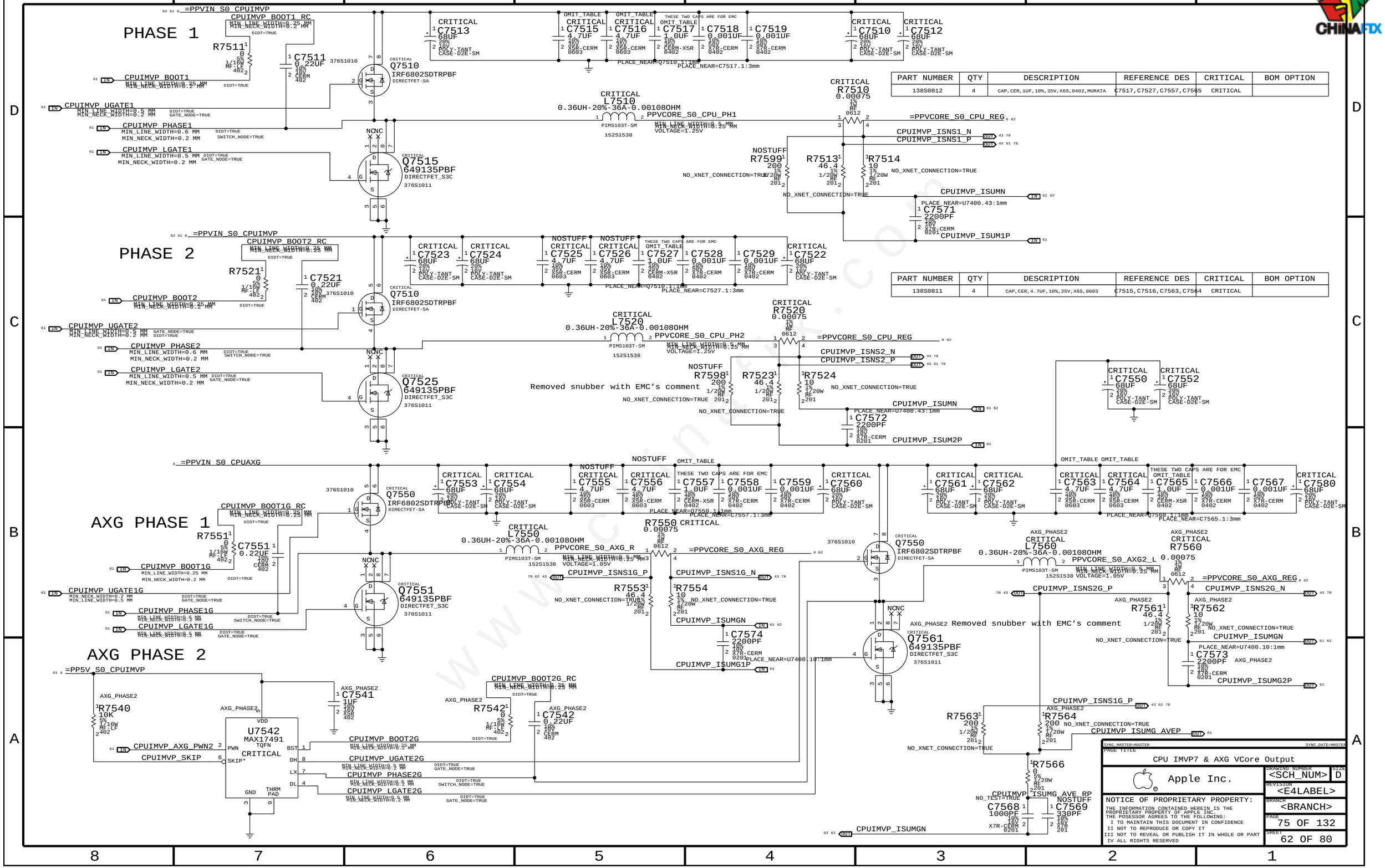
PHASE 1
CPUIMVP_BOOT1_RC
R7511 0 5% 1/10W MF-LF 402
C7511 0.22UF 10% 10V X5R CERM 402
376S1010
Q7510 IRF6802SDTRPBF DIRECTFET-SA
CPUIMVP_BOOT1
CPUIMVP_UGATE1
CPUIMVP_PHASE1
CPUIMVP_LGATE1
Q7515 649135PBF DIRECTFET_S3C 376S1011
=PPVIN_S0_CPUIMVP
C7513 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7515 4.7UF 10% 35V X5R-CERM 0603
C7516 4.7UF 10% 35V X5R-CERM 0603
C7517 1.0UF 10% 50V CERM-X5R 0402
C7518 0.001UF 10% 50V X7R-CERM 0402
C7519 0.001UF 10% 50V X7R-CERM 0402
C7510 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7512 68UF 20% 16V POLY-TANT CASE-D2E-SM
THESE TWO CAPS ARE FOR EMC
PLACE_NEAR=Q7510.1:1mm
PLACE_NEAR=C7517.1:3mm
L7510 0.36UH-20%-36A-0.001080HM PIMS103T-SM 152S1538
PPVCORE_S0_CPU_PH1
VOLTAGE=1.25V
R7510 0.00075 1% 1W MF 0612
=PPVCORE_S0_CPU_REG
CPUIMVP_ISNS1_N
CPUIMVP_ISNS1_P
R7599 200 1% 1/20W MF 201
R7513 46.4 1% 1/20W MF 201
R7514 10 1% 1/20W MF 201
NO_XNET_CONNECTION=TRUE
CPUIMVP_ISUMN
C7571 2200PF 10% 16V X7R-CERM 0201
CPUIMVP_ISUM1P
PHASE 2
CPUIMVP_BOOT2_RC
R7521 0 5% 1/10W MF-LF 402
C7521 0.22UF 10% 10V X5R CERM 402
376S1010
Q7510 IRF6802SDTRPBF DIRECTFET-SA
CPUIMVP_BOOT2
CPUIMVP_UGATE2
CPUIMVP_PHASE2
CPUIMVP_LGATE2
Q7525 649135PBF DIRECTFET_S3C 376S1011
C7523 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7524 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7525 4.7UF 10% 35V X5R-CERM 0603
C7526 4.7UF 10% 35V X5R-CERM 0603
C7527 1.0UF 10% 50V CERM-X5R 0402
C7528 0.001UF 10% 50V X7R-CERM 0402
C7529 0.001UF 10% 50V X7R-CERM 0402
C7522 68UF 20% 16V POLY-TANT CASE-D2E-SM
PLACE_NEAR=Q7510.1:1mm
PLACE_NEAR=C7527.1:3mm
L7520 0.36UH-20%-36A-0.001080HM PIMS103T-SM 152S1538
PPVCORE_S0_CPU_PH2
VOLTAGE=1.25V
R7520 0.00075 1% 1W MF 0612
=PPVCORE_S0_CPU_REG
CPUIMVP_ISNS2_N
CPUIMVP_ISNS2_P
R7598 200 1% 1/20W MF 201
R7523 46.4 1% 1/20W MF 201
R7524 10 1% 1/20W MF 201
NO_XNET_CONNECTION=TRUE
CPUIMVP_ISUMN
C7572 2200PF 10% 16V X7R-CERM 0201
CPUIMVP_ISUM2P
Removed snubber with EMC's comment
C7550 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7552 68UF 20% 16V POLY-TANT CASE-D2E-SM
AXG PHASE 1
CPUIMVP_BOOT1G_RC
R7551 0 5% 1/10W MF-LF 402
C7551 0.22UF 10% 10V CERM 402
376S1010
Q7550 IRF6802SDTRPBF DIRECTFET-SA
CPUIMVP_BOOT1G
CPUIMVP_UGATE1G
CPUIMVP_PHASE1G
CPUIMVP_LGATE1G
Q7551 649135PBF DIRECTFET_S3C 376S1011
=PPVIN_S0_CPUAXG
C7553 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7554 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7555 4.7UF 10% 35V X5R-CERM 0603
C7556 4.7UF 10% 35V X5R-CERM 0603
C7557 1.0UF 10% 50V CERM-X5R 0402
C7558 0.001UF 10% 50V X7R-CERM 0402
C7559 0.001UF 10% 50V X7R-CERM 0402
C7560 68UF 20% 16V POLY-TANT CASE-D2E-SM
PLACE_NEAR=Q7550.1:1mm
PLACE_NEAR=C7557.1:3mm
L7550 0.36UH-20%-36A-0.001080HM PIMS103T-SM 152S1538
PPVCORE_S0_AXG_R
VOLTAGE=1.05V
R7550 0.00075 1% 1W MF 0612
=PPVCORE_S0_AXG_REG
CPUIMVP_ISNS1G_P
CPUIMVP_ISNS1G_N
R7553 46.4 1% 1/20W MF 201
R7554 10 1% 1/20W MF 201
NO_XNET_CONNECTION=TRUE
CPUIMVP_ISUMGN
C7574 2200PF 10% 16V X7R-CERM 0201
CPUIMVP_ISUM1P
AXG PHASE 2
=PP5V_S0_CPUIMVP
R7540 10K 5% 1/16W MF-LF 402
C7541 1UF 10% 16V X5R 402
U7542 MAX17491 TQFN CRITICAL
CPUIMVP_AXG_PWN2
CPUIMVP_SKIP
CPUIMVP_BOOT2G_RC
R7542 0 5% 1/10W MF-LF 402
C7542 0.22UF 10% 10V CERM 402
CPUIMVP_BOOT2G
CPUIMVP_UGATE2G
CPUIMVP_PHASE2G
CPUIMVP_LGATE2G
Q7561 649135PBF DIRECTFET_S3C 376S1011
C7561 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7562 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7563 4.7UF 10% 35V X5R-CERM 0603
C7564 4.7UF 10% 35V X5R-CERM 0603
C7565 1.0UF 10% 50V CERM-X5R 0402
C7566 0.001UF 10% 50V X7R-CERM 0402
C7567 0.001UF 10% 50V X7R-CERM 0402
C7580 68UF 20% 16V POLY-TANT CASE-D2E-SM
PLACE_NEAR=Q7560.1:1mm
PLACE_NEAR=C7565.1:3mm
L7560 0.36UH-20%-36A-0.001080HM PIMS103T-SM 152S1538
PPVCORE_S0_AXG2_L
VOLTAGE=1.05V
R7560 0.00075 1% 1W MF 0612
=PPVCORE_S0_AXG_REG
CPUIMVP_ISNS2G_P
CPUIMVP_ISNS2G_N
R7561 46.4 1% 1/20W MF 201
R7562 10 1% 1/20W MF 201
NO_XNET_CONNECTION=TRUE
CPUIMVP_ISUMGN
C7573 2200PF 10% 16V X7R-CERM 0201
CPUIMVP_ISUM2P
Removed snubber with EMC's comment
CPUIMVP_ISNS1G_P
R7563 200 1% 1/20W MF 201
R7564 200 1% 1/20W MF 201
NO_XNET_CONNECTION=TRUE
CPUIMVP_ISUMG_AVEP
R7566 0 5% 1/20W MF 201
CPUIMVP_ISUMG_AVE_RP
C7568 1000PF 10% 16V X7R-CERM 0201
C7569 330PF 10% 16V X7R 201
NO_TEST=TRUE
CPUIMVP_ISUMGN
PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION
138S0812 | 4 | CAP,CER,1UF,10%,35V,X6S,0402,MURATA | C7517,C7527,C7557,C7565 | CRITICAL
PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION
138S0811 | 4 | CAP,CER,4.7UF,10%,25V,X6S,0603 | C7515,C7516,C7563,C7564 | CRITICAL
SYNC_MASTER=MASTER
SYNC_DATE=MASTER
PAGE TITLE
CPU IMVP7 & AXG VCore Output
Apple Inc.
DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 75 OF 132
SHEET 62 OF 80
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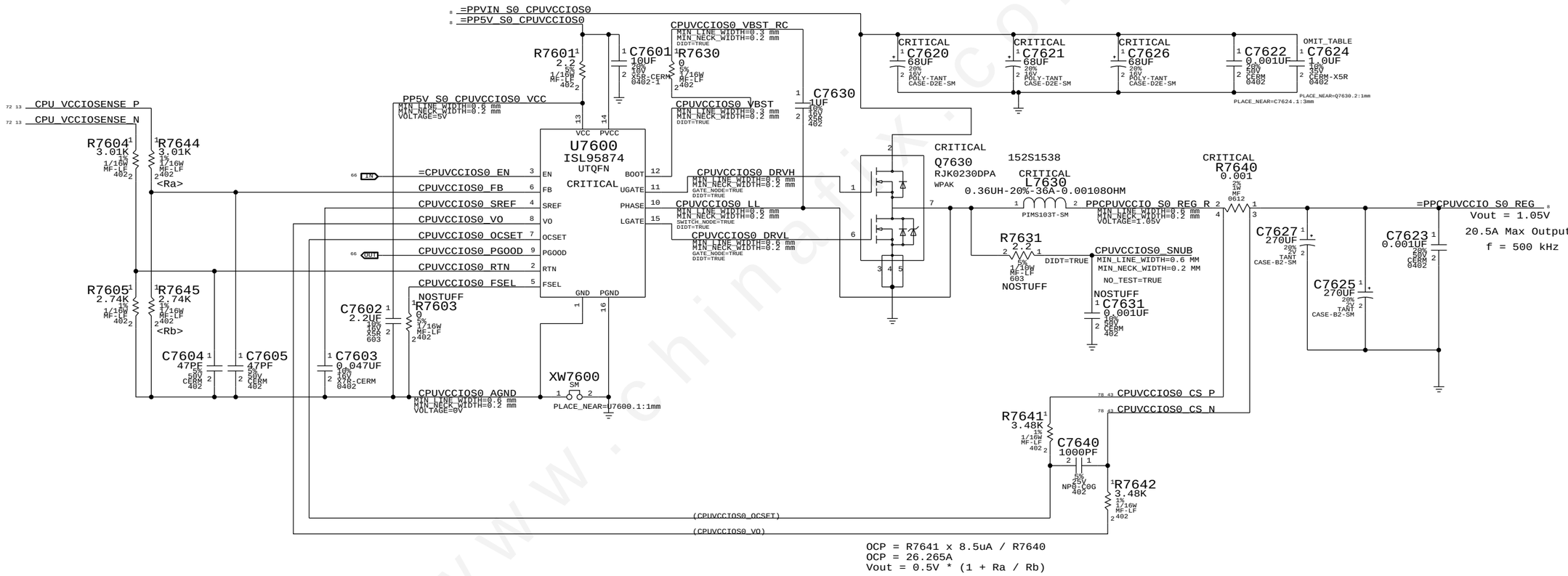
CPU VCCIO (1.05V S0) Regulator

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	1	CAP,CER,1UF,10%,35V,X6S,0402,MURATA	C7624	CRITICAL	



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: CPUVCCIO (1.05V) Power Supply

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

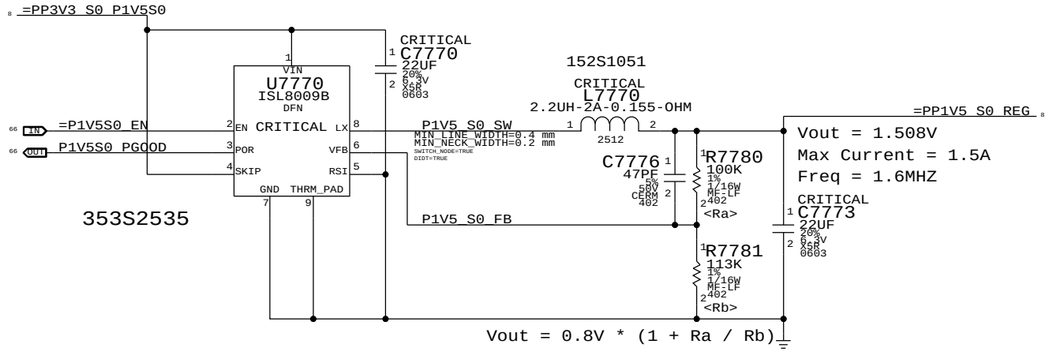
REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 76 OF 132

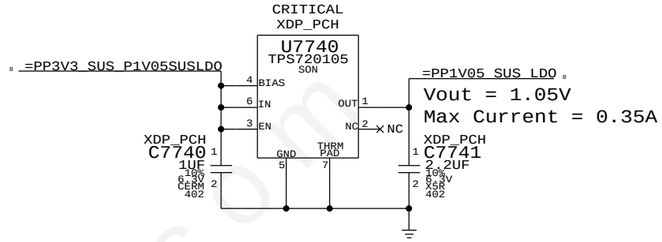
SHEET: 63 OF 80

1.5V S0 Switcher



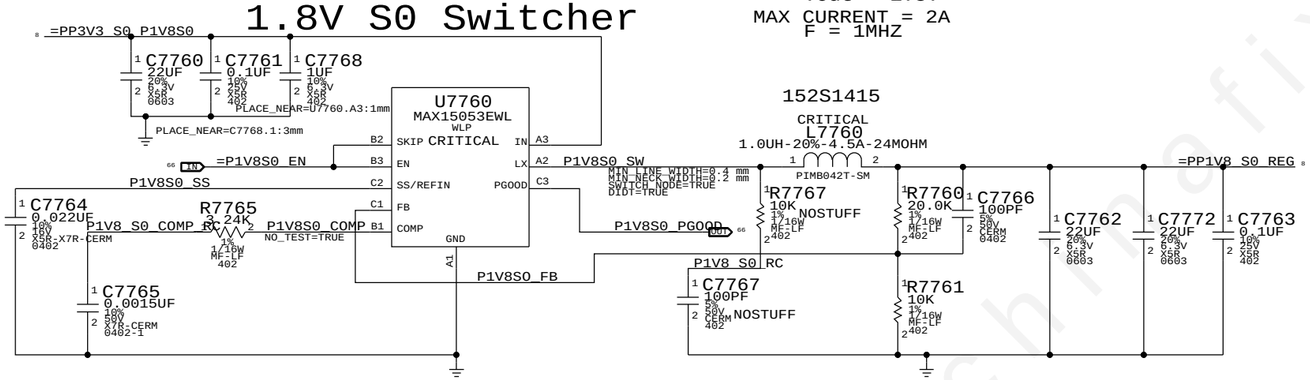
1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V in SUS.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.

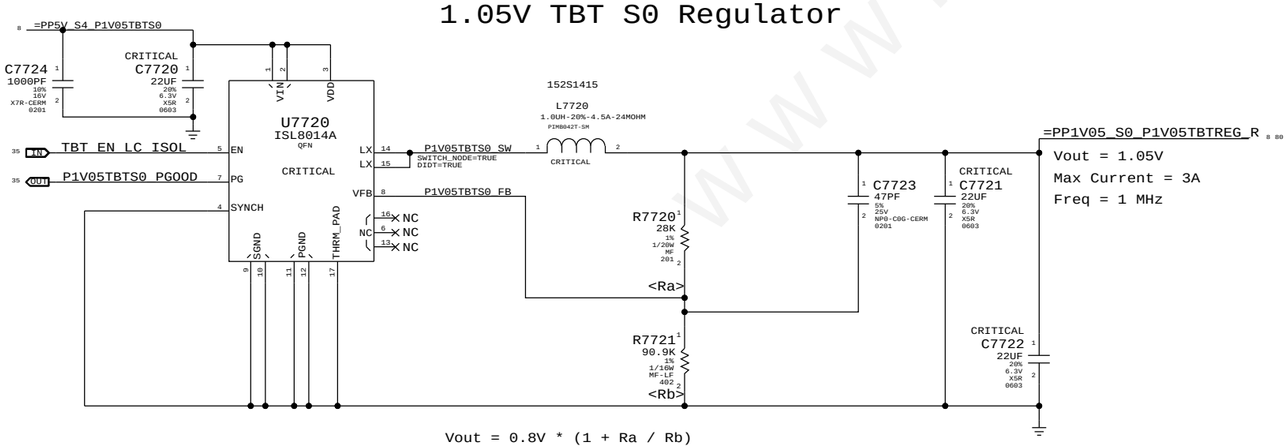


1.8V S0 Switcher

Vout = 1.8V
MAX CURRENT = 2A
F = 1MHZ



1.05V TBT S0 Regulator



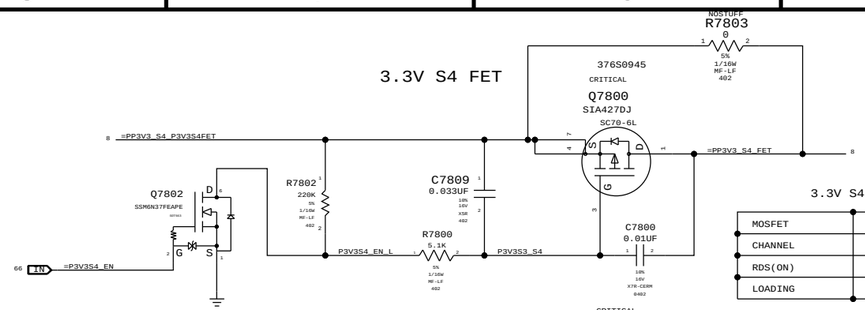
SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
Misc Power Supplies

Apple Inc.

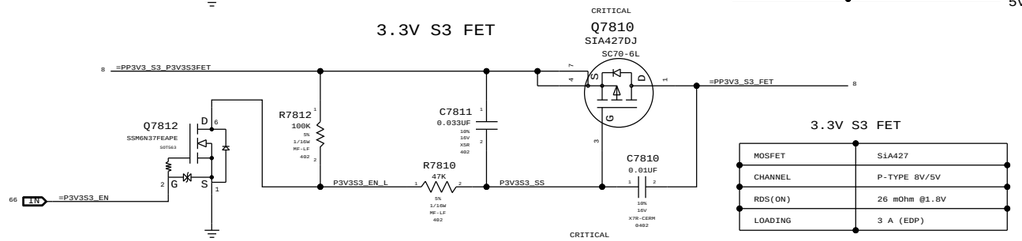
DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 77 OF 132
SHEET 64 OF 80

3.3V S4 FET



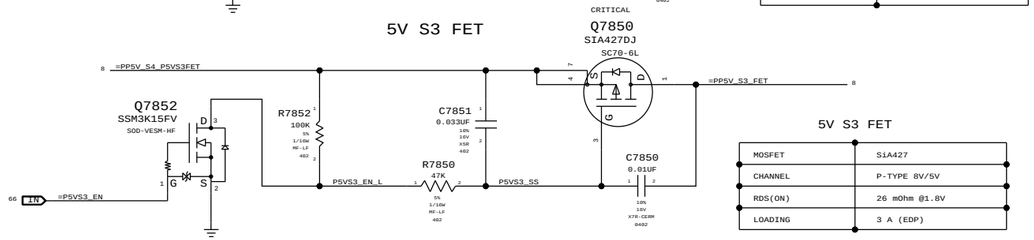
3.3V S4 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.7? A (EDP)

3.3V S3 FET



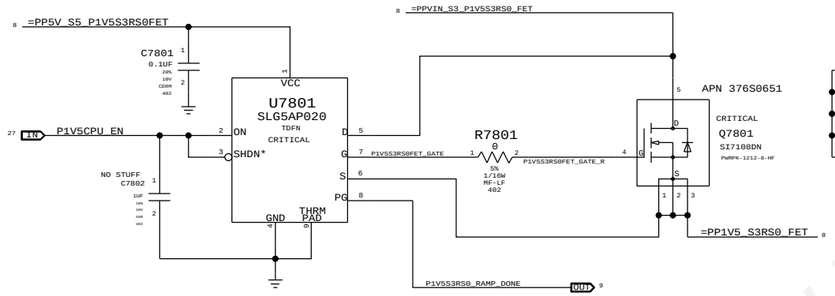
3.3V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3 A (EDP)

5V S3 FET



5V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3 A (EDP)

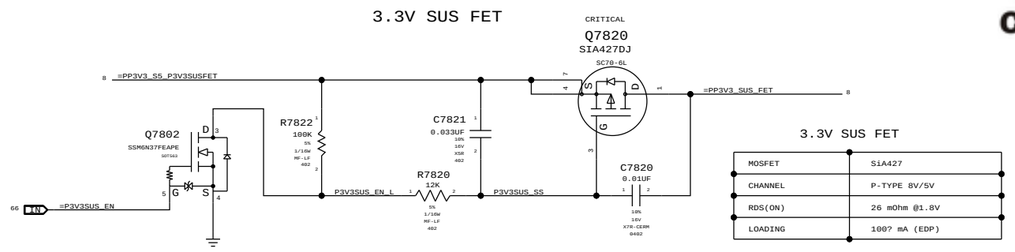
1.5V S3/S0 FET



1.5V S3/S0 FET	
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	5 A (EDP)

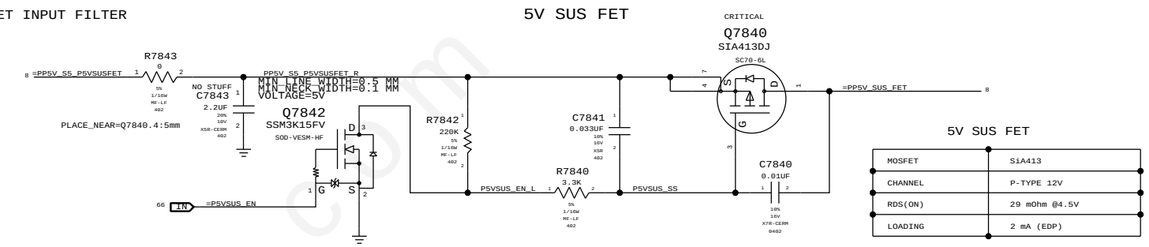
5V_SUS FET INPUT FILTER

3.3V SUS FET



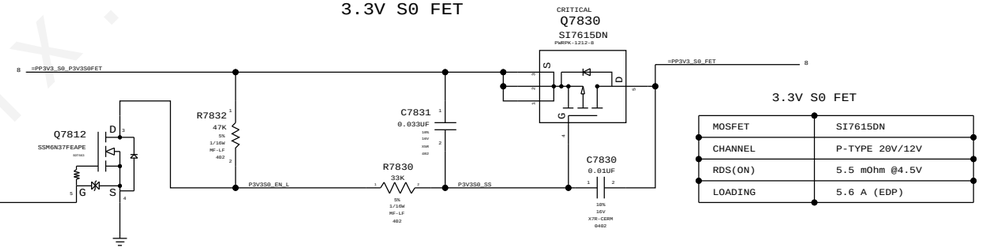
3.3V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

5V SUS FET



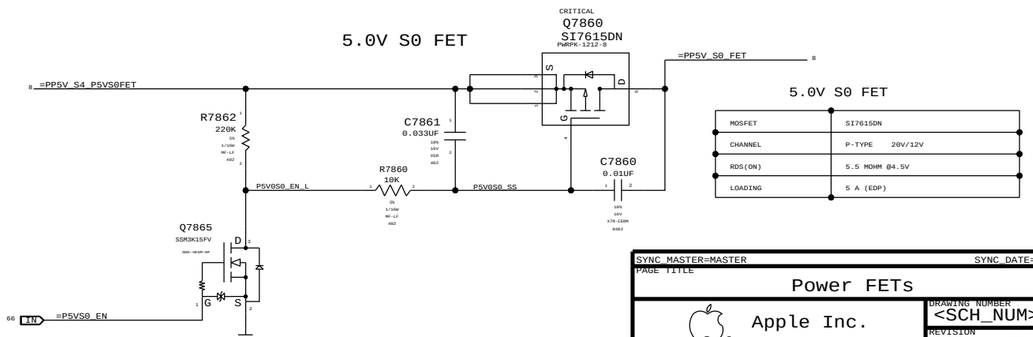
5V SUS FET	
MOSFET	SiA413
CHANNEL	P-TYPE 12V
RDS(ON)	29 mOhm @4.5V
LOADING	2 mA (EDP)

3.3V S0 FET



3.3V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5.6 A (EDP)

5.0V S0 FET



5.0V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	5 A (EDP)

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

Power FETs

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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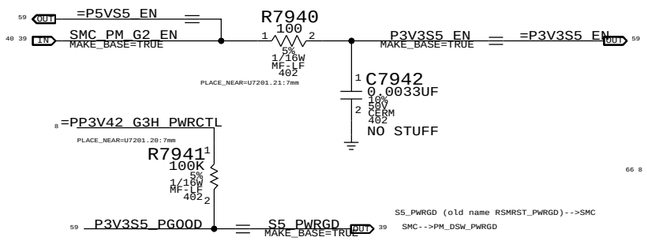
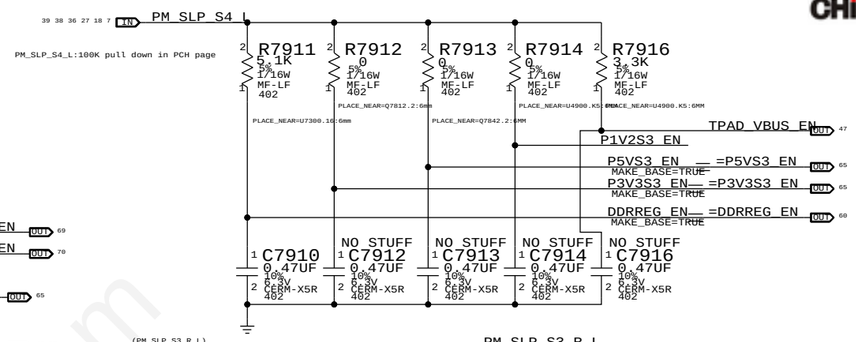
S5 Rail Enables & PGOOD



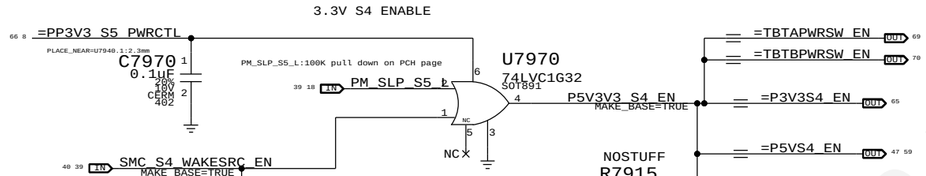
Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SUS_EN	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (S4AC)	1	1	1	0	0	0	0
Deep Sleep (S4)	0	1	1	0	0	0	0
Deep Sleep (S5AC)	1	1	0	0	0	0	0
Deep Sleep (S5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

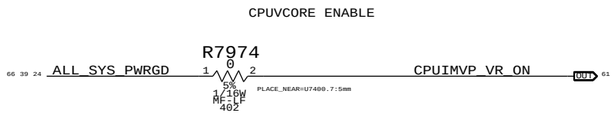
1.2V, 5V, 3.3V, DDR S3 ENABLE



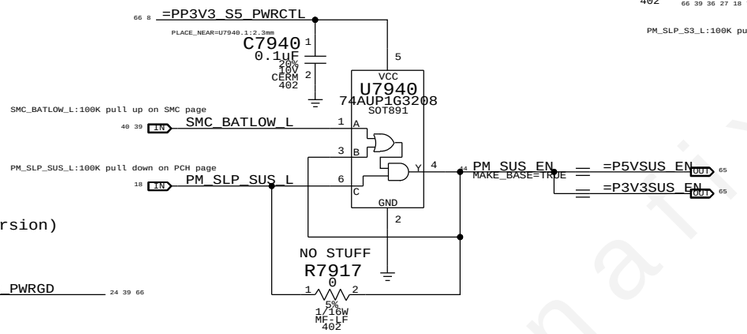
3.3V S4 ENABLE



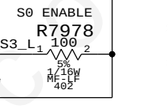
CPUVCORE ENABLE



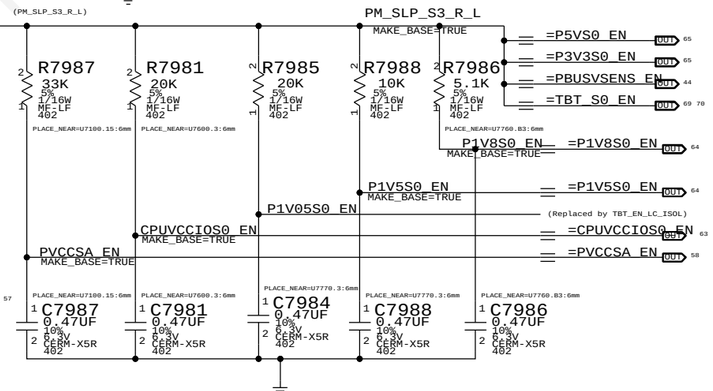
3.3V/5.0V Sus ENABLE



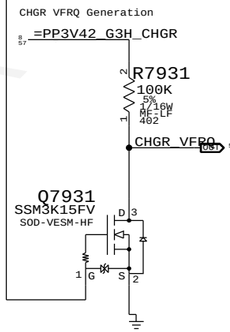
S0 ENABLE



PM_SLP_S3_R_L

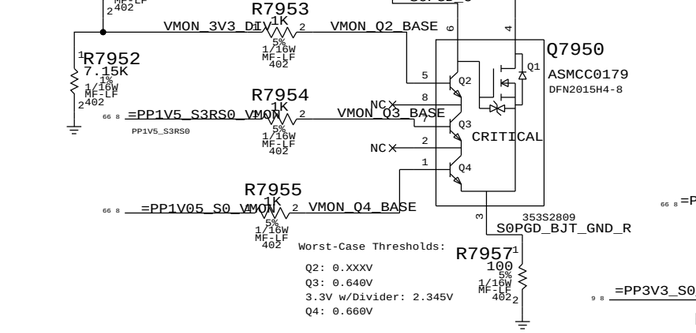


CHGR VFRQ Generation

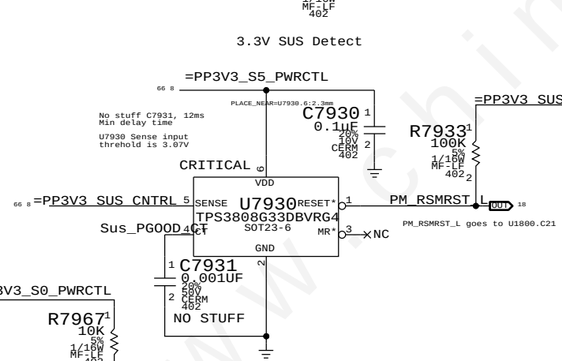


VFRQ Low: Fix Frequency
VFRQ High: Variable Frequency

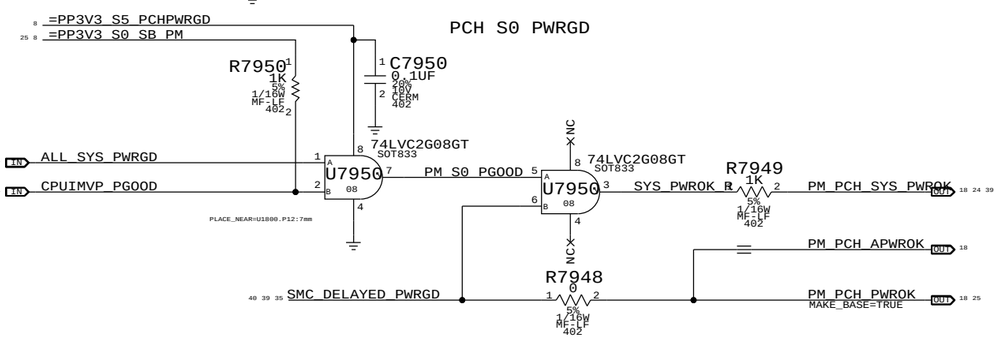
S0 Rail PGOOD (BJT Version)



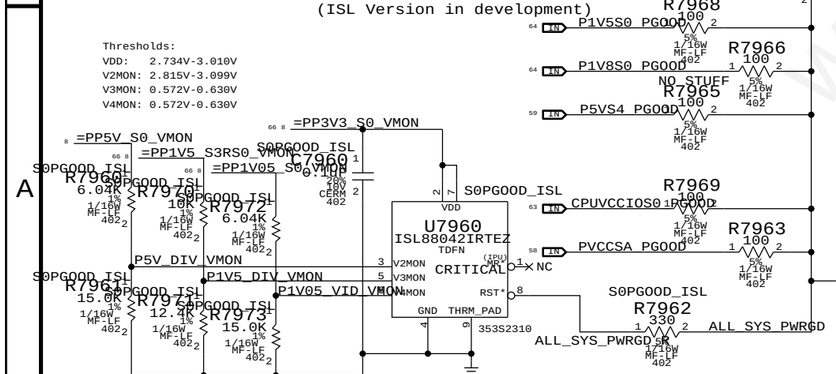
3.3V SUS Detect



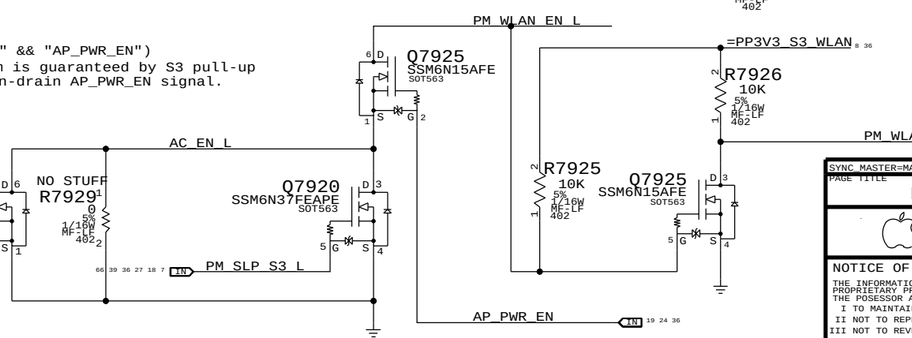
PCH S0 PWRGD



S0 Rail PGOOD Circuitry
(ISL Version in development)



"WLAN" = ("S3" && "AP_PWR_EN")
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



SYNC_MASTER=MASTER SYNC_DATE=MASTER
PAGE TITLE
Power Control 1/ENABLE

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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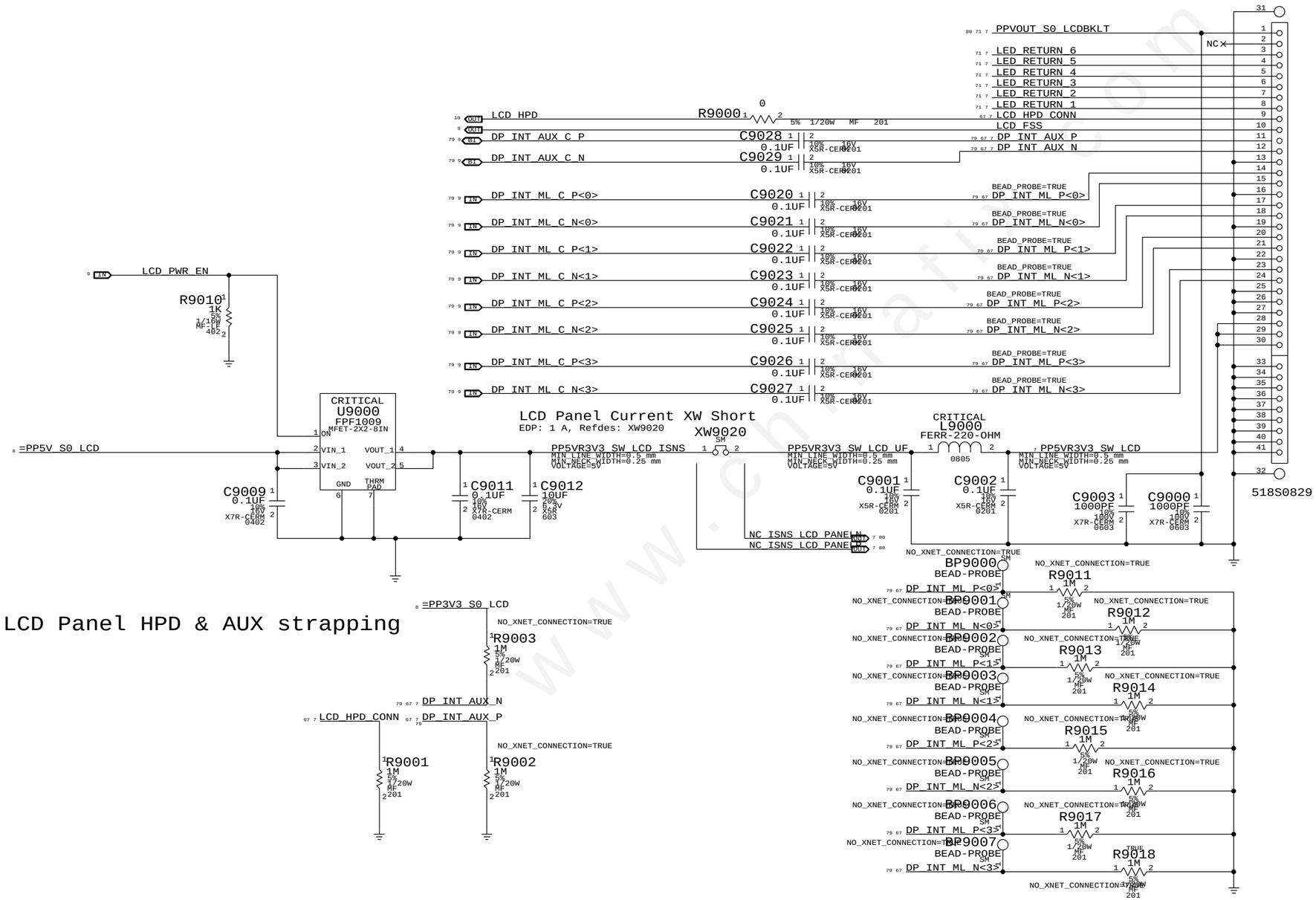
LCD PANEL INTERFACE (eDP)



LCD Panel HPD & AUX strapping

SYNC_MASTER=D1_SENSORS SYNC_DATE=07/11/2012

PAGE TITLE: eDP Display Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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8 =PP3V3_S0_DDCMUX

DDC Crossbar

Only necessary on dual-port hosts.
On single-port hosts alias TBTPA_DDC to TBTSNK0_DDC.
NEVER SEND AUXCH THROUGH CROSSBAR!

R9251 2.2K 1% 1/20W MF 201
R9252 2.2K 1% 1/20W MF 201
R9253 2.2K 1% 1/20W MF 201
R9254 2.2K 1% 1/20W MF 201

C9280 0.1UF 20% 10V CERM 402

U9200
TS3DS10224
QFN
CRITICAL

		13	VCC		
69 OUT / 69 BI	DP_TBTPA_DDC_CLK / DP_TBTPA_DDC_DATA	1	INA+	OUTA1+	20
		2	INA-	OUTA1-	19
				OUTA0+	18
				OUTA0-	17
		14	SAI	SAO	15
		10	ENB		
70 OUT / 70 BI	DP_TBTPB_DDC_CLK / DP_TBTPB_DDC_DATA	3	INB+	OUTB1+	6
		4	INB-	OUTB1-	7
				OUTB0+	8
				OUTB0-	9
33 IN	TBT_DDC_XBAR_EN_L	12	SBI	SBO	11
		5	GND	THRM PAD	21

DP_TBTSNK0_DDC_CLK (IN 9) / DP_TBTSNK0_DDC_DATA (BI 9)
DP_TBTSNK1_DDC_CLK (IN 9) / DP_TBTSNK1_DDC_DATA (BI 9)

SAI/SBI = 1: INA == OUTA0, INB == OUTB0
SAI/SBI = 0: INA == OUTB0, INB == OUTA0

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: DDC Crossbar

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 92 OF 132
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	1	CAP,CER,4.7UF,10%,25V,X5R,0603,MURATA	C9415	CRITICAL	

3.3V/HV Power MUX

V3P3 must be S4 to support wake from Thunderbolt devices.

=PP3V3_S4_TBTAPWRSW

CRITICAL C9487 100UF 20% 6.3V POLY-TANT CASE-B2-SM; CRITICAL C9480 22UF 20% 6.3V X5R-CERM 603; C9481 0.1UF 10% 16V X5R-CERM 0201

=PPHV_SW_TBTAPWRSW (18.9V Max)

OMIT_TABLE; C9415 4.7UF 10% 25V X5R-CERM 0603; C9410 0.1UF 10% 25V X5R 402

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 35, 9-12.6V, 7.5-11.7W)

CRITICAL U9410 CD3210A0RGP QFN

V3P3 ← V3P3OUT; VHV ← OUT; RSVD; EN ← =TBTAPWRSW_EN; HV_EN ← TBT_A_HV_EN_RC; S0 ← =TBT_S0_EN; ISET_V3P3 → TBTAPWRSW_ISET_V3P3; ISET_S0 → TBTAPWRSW_ISET_S0; ISET_S3 → TBTAPWRSW_ISET_S3; GND; THRM PAD

C9485 0.1UF 10% 16V X5R-CERM 0201; C9486 10UF 20% 6.3V CERM-X5R 0402; C9411 0.1UF 10% 25V X5R 402

PP3V3_SW_TBTAPWR — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=3.3V

PPHV_SW_TBTAPWR — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=15V

TBTHV:P15V
R9410 22.6K 1% 1/20W MF 201 (12V: See below)
R9411 22.6K 1% 1/20W MF 201
R9412 36.5K 1% 1/20W MF 201 <RV3P3>
R9413 22.6K 1% 1/20W MF 201 <RHVS3>
R9414 22.6K 1% 1/20W MF 201 <RHVS0>

Single-fault protection requires two R's per HV ISET_Sx with CD3210. Single R on ISET_V3P3 OK.

ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/16W,17.8K,1,0201,SMD,LF	R9410,R9413		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/16W,17.8K,1,0201,SMD,LF	R9411,R9414		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

TBT_A_D2R_P<0> / TBT_A_D2R_N<0> — C9474 0.47UF, C9475 0.47UF 20% 4V CERM-X5R 201 — TBT_A_D2R_C_P<0> / TBT_A_D2R_C_N<0>

R9494 1K 5% 1/20W MF 201; R9495 1K 5% 1/20W MF 201 (NO_XNET_CONNECTION=TRUE)

DP_TBTPA_ML_C_P<3> / DP_TBTPA_ML_C_N<3> — C9478 0.22UF, C9479 0.22UF 20% 6.3V X5R 0201 — DP_TBTPA_ML_P<3> / DP_TBTPA_ML_N<3>

R9478 470K 5% 1/20W MF 201; R9479 470K 5% 1/20W MF 201 (TBT: Unused)

TBT_A_BIAS

R9498 2.2K 5% 1/20W MF 201; R9499 2.2K 5% 1/20W MF 201

TBT_A_D2R_P<1> / TBT_A_D2R_N<1> — C9476 0.47UF, C9477 0.47UF (Both C's) 20% 4V CERM-X5R 201 — TBT_A_D2R_C_P<1> / TBT_A_D2R_C_N<1>

CRITICAL D9498 / D9499 BAR90-02LRH TSLP-2-7 (Both D's) — TBT_A_D2R1_AUXDDC_P / TBT_A_D2R1_AUXDDC_N

CRITICAL L9498 650NH-5%-0.430MA-0.52OHM 0603; CRITICAL L9499 650NH-5%-0.430MA-0.52OHM 0603

DP_A_AUXCH_DDC_P / DP_A_AUXCH_DDC_N

C9498 30PF 5% 25V C0G-CERM 0201; C9499 30PF 5% 25V C0G-CERM 0201

TBT_A_HPD

TBT_A_CONFIG1_RC

TBT_A_CONFIG2_RC

R9452 1M 5% 1/20W MF 201; R9451 1M 5% 1/20W MF 201; C9494 330PF 10% 16V X7R-CERM 0201; C9495 330PF 10% 16V X7R-CERM 0201; R9441 100K 5% 1/20W MF 201

C9402 0.01UF 10% 16V X5R-CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

PP3V3_SW_TBTAPWR

C9420 0.1UF 10% 16V X5R-CERM 0201; C9421 0.1UF 10% 16V X5R-CERM 0201

R9427 10K 5% 1/20W MF 201; R9429 100K 5% 1/20W MF 201

CRITICAL U9420 CBTL05023 HVQFN

SIGNAL_MODEL=TBT_MUX

TBT_A_CIO_SEL	1	BIASIN	BIASOUT	24	TBT_A_BIAS (VOLTAGE=3.3V)
DP_AUXIO_EN	2	AUXIO_EN			C9425 0.1UF 10% 16V X5R-CERM 0201
DP_TBTPA_AUXCH_C_N	7	AUX-	AUXIO-	23	DP_A_AUXCH_DDC_N
DP_TBTPA_AUXCH_P	8	AUX+	AUXIO+	22	DP_A_AUXCH_DDC_P
DP_TBTPA_DDC_DATA	4	DDC_DAT			TBT: RX_1 Bias Sink
DP_TBTPA_DDC_CLK	5	DDC_CLK			
TBT_A_CONFIG1_BUF	16	CA_DETOUT	CA_DET	18	TBT_A_CONFIG1_RC
DP_TBTPA_ML_P<1>	11	DP+	DPML0+	19	DP_A_LSX_ML_P<1>
DP_TBTPA_ML_N<1>	10	DP-	DPML0-	20	DP_A_LSX_ML_N<1>
TBT_A_LSTX	14	LSTX			TBT: LSX_A_R2P/P2R (P/N)
TBT_A_LSRX_UNBUF	13	LSRX			
TBT_A_DP_PWRDN	6	DP_PD			
DP_TBTPA_HPD	12	HPDOUT	HPD	17	TBT_A_HPD
	9	GND_THMPAD		21, 25	

DP_TBTPA_AUXCH_C_N / DP_TBTPA_AUXCH_C_P — C9430 0.1UF, C9431 0.1UF 10% 16V X5R-CERM 0201

DP_TBTPA_ML_C_P<1> / DP_TBTPA_ML_C_N<1> — C9432 0.22UF, C9433 0.22UF 20% 6.3V X5R 0201

R9426 1M 5% 1/20W MF 201; R9428 100K 5% 1/20W MF 201

PP3V3_SW_TBTAPWR

CRITICAL U9460 74AUP1T97 SOT891 — TBT_A_LSRX (OUT) → Y; C9460 0.1UF 10% 16V X5R-CERM 0201

Thunderbolt Connector A

L9400 FERR-120-OHM-3A 0603 — PP3V3RHV_SW_TBTAPWR — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=15V

C9400 0.01UF 10% 16V X7R-CERM 0402; C9401 0.01UF 10% 16V X7R-CERM 0402

TBTACONN_20_RC — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18V

R9401 12 5% 1/20W MF 201

For J9400 TBT SMT pads (3, 5, 17 & 19):

CRITICAL J9400 MDP-D1 F-RT-TH SHIELD PINS

B2	HPD	GND0	B1
B4	CONFIG1	ML_LANE0P	B3
B6	CONFIG2	ML_LANE0N	B5
B8	GND2	GND1	B7
B10	ML_LANE3P	ML_LANE1P	B9
B12	ML_LANE3N	ML_LANE1N	B11
B14	GND4	GND3	B13
B16	AUX_CHP	ML_LANE2P	B15
B18	AUX_CHN	ML_LANE2N	B17
B20	DP_PWR	RETURN	B19

PORT B SHIELD PINS: S24, S22, S21, S20, S19, S18, S17

514-0836

TBTACONN_1_C — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18.9V

C9405 0.01UF 10% 16V X5R-CERM 0201 (GND_VOID=TRUE)

TBT_A_R2D_P<0> / TBT_A_R2D_N<0> (0-18.9V, TBT: TX_0) — C9470 0.22UF, C9471 0.22UF (Both C's) 20% 6.3V X5R 0201 — TBT_A_R2D_C_P<0> / TBT_A_R2D_C_N<0>

TBTACONN_7_C — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.28 MM, VOLTAGE=18.9V

C9406 0.01UF 10% 16V X5R-CERM 0201

R9470 470K 5% 1/20W MF 201; R9471 470K 5% 1/20W MF 201

DP_A_LSX_ML_P<1> / DP_A_LSX_ML_N<1> (0-18.9V, TBT: LSX_R2P/P2R (P/N))

TBT_A_R2D_P<1> / TBT_A_R2D_N<1> (TBT: TX_1) — C9472 0.22UF, C9473 0.22UF (Both C's) 20% 6.3V X5R 0201 — TBT_A_R2D_C_P<1> / TBT_A_R2D_C_N<1>

R9472 470K 5% 1/20W MF 201; R9473 470K 5% 1/20W MF 201

470k R's for ESD protection on AC-coupled signals.

SYNC_MASTER=J5_MLB_KEPLER SYNC_DATE=11/14/2011

PAGE TITLE: Thunderbolt Connector A

Apple Inc.

DRAWING NUMBER	<SCH_NUM>
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REVISION	<E4LABEL>
BRANCH	<BRANCH>
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	1	CAP,CER,4.7UF,10%,25V,X5R,0603,MURATA	C9615	CRITICAL	

3.3V/HV Power MUX

V3P3 must be S4 to support wake from Thunderbolt devices.

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)

For 12V systems:

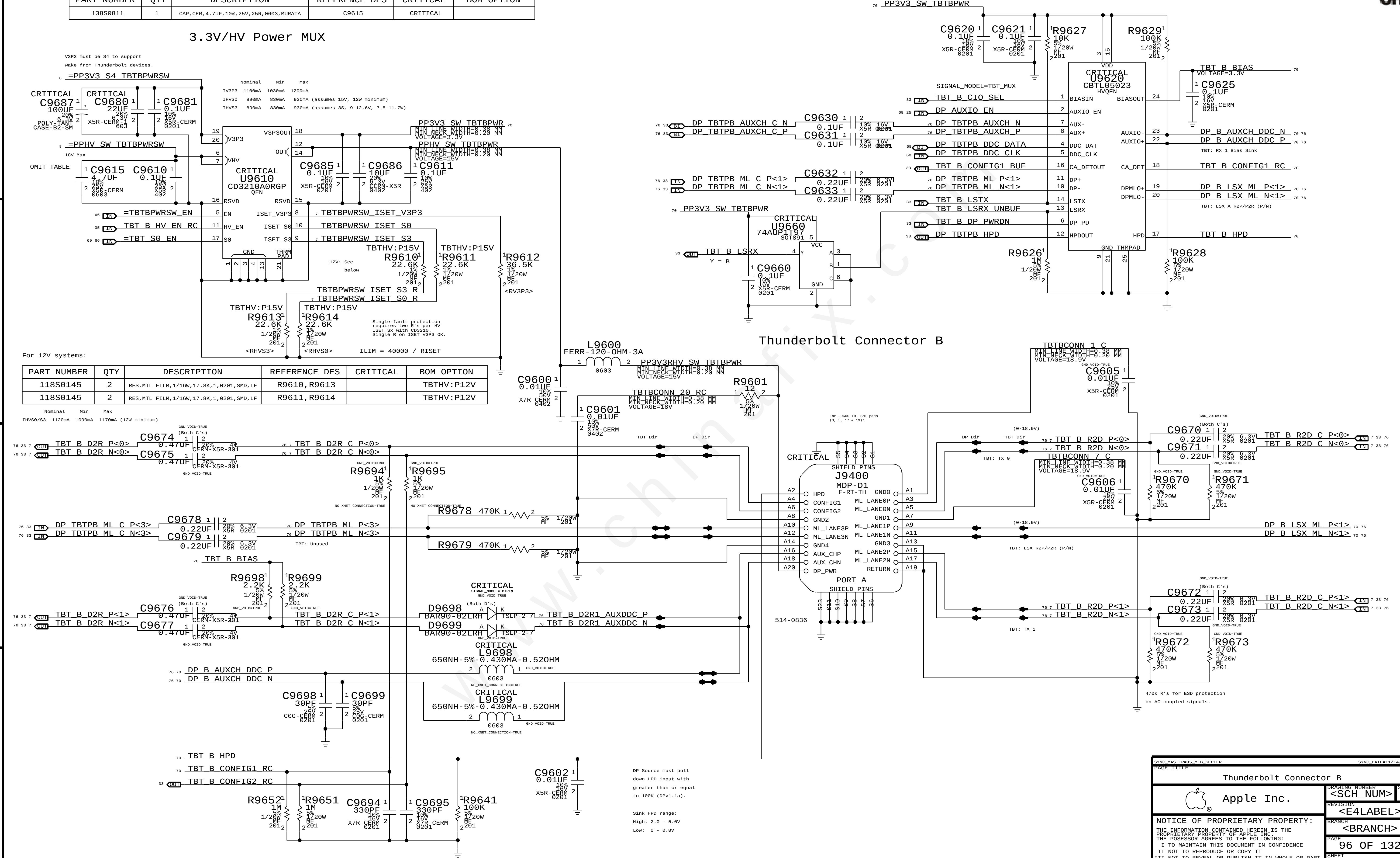
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/16W,17.8K,1,0201,SMD,LF	R9610,R9613		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/16W,17.8K,1,0201,SMD,LF	R9611,R9614		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

Single-fault protection requires two R's per HV ISET_Sx with CD3210. Single R on ISET_V3P3 OK.

ILIM = 40000 / RISET

Thunderbolt Connector B



SYNC_MASTER=J5_MLB_KEPLER SYNC_DATE=11/14/2011

PAGE TITLE: Thunderbolt Connector B

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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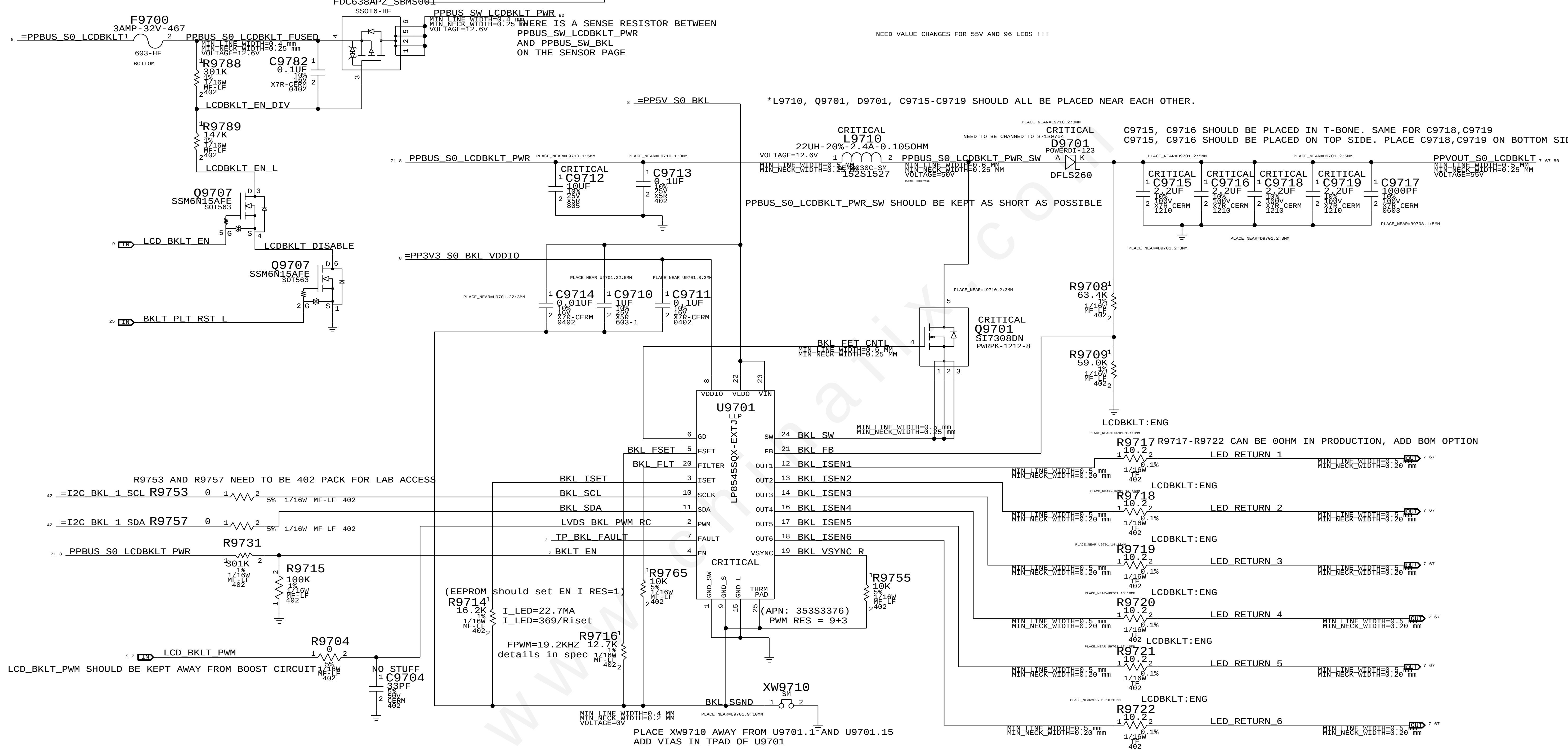
PPBUS S0 LCDBKLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.715 A (EDP)



=PPBUS_S0_LCDBKLT
F9700
3AMP-32V-467
603-HF
BOTTOM
PPBUS_S0_LCDBKLT_FUSED
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
CRITICAL
Q9706
FDC638APZ_SBMS001
SSOT6-HF
PPBUS_SW_LCDBKLT_PWR
THERE IS A SENSE RESISTOR BETWEEN
PPBUS_SW_LCDBKLT_PWR
AND PPBUS_SW_BKL
ON THE SENSOR PAGE
NEED VALUE CHANGES FOR 55V AND 96 LEDS !!!
R9788
301K
C9782
0.1UF
LCDBKLT_EN_DIV
R9789
147K
LCDBKLT_EN_L
Q9707
SSM6N15AFE
SOT563
LCD_BKLT_EN
LCDBKLT_DISABLE
BKLT_PLT_RST_L
=PP5V_S0_BKL
*L9710, Q9701, D9701, C9715-C9719 SHOULD ALL BE PLACED NEAR EACH OTHER.
CRITICAL
L9710
22UH-20%-2.4A-0.105OHM
152S1527
CRITICAL
D9701
POWERDI-123
DFLS260
PPBUS_S0_LCDBKLT_PWR_SW
C9715, C9716 SHOULD BE PLACED IN T-BONE. SAME FOR C9718,C9719
C9715, C9716 SHOULD BE PLACED ON TOP SIDE. PLACE C9718,C9719 ON BOTTOM SIDE
PPVOUT_S0_LCDBKLT
VOLTAGE=55V
PPBUS_S0_LCDBKLT_PWR
CRITICAL
C9712
10UF
C9713
0.1UF
C9715
C9716
C9718
C9719
2.2UF
C9717
1000PF
PPBUS_S0_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE
=PP3V3_S0_BKL_VDDIO
C9714
0.01UF
C9710
1UF
C9711
0.1UF
R9708
63.4K
CRITICAL
Q9701
SI7308DN
PWRPK-1212-8
BKL_FET_CNTL
R9709
59.0K
LCDBKLT:ENG
U9701
LP8545SQX-EXTJ
CRITICAL
VDDIO
VLDO
VIN
GD
FSET
FILTER
ISET
SCLK
SDA
PWM
FAULT
EN
SW
FB
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
VSYNC
THRM PAD
BKL_SW
BKL_FB
BKL_ISEN1
BKL_ISEN2
BKL_ISEN3
BKL_ISEN4
BKL_ISEN5
BKL_ISEN6
BKL_VSYNC_R
BKL_FSET
BKL_FLT
BKL_ISET
BKL_SCL
BKL_SDA
LVDS_BKL_PWM_RC
TP_BKL_FAULT
BKL_EN
R9717-R9722 CAN BE 0OHM IN PRODUCTION, ADD BOM OPTION
R9717
R9718
R9719
R9720
R9721
R9722
10.2
LED_RETURN_1
LED_RETURN_2
LED_RETURN_3
LED_RETURN_4
LED_RETURN_5
LED_RETURN_6
R9753 AND R9757 NEED TO BE 402 PACK FOR LAB ACCESS
=I2C_BKL_1_SCL
R9753
=I2C_BKL_1_SDA
R9757
PPBUS_S0_LCDBKLT_PWR
R9731
301K
R9715
100K
R9765
10K
R9755
10K
(APN: 353S3376)
PWM RES = 9+3
(EEPROM should set EN_I_RES=1)
R9714
16.2K
I_LED=22.7MA
I_LED=369/Riset
R9716
12.7K
FPWM=19.2KHZ
details in spec
LCD_BKLT_PWM
R9704
0
LCD_BKLT_PWM SHOULD BE KEPT AWAY FROM BOOST CIRCUIT
NO STUFF
C9704
33PF
XW9710
BKL_SGND
PLACE XW9710 AWAY FROM U9701.1 AND U9701.15
ADD VIAS IN TPAD OF U9701

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	6	RES,MTL FILM,1/16W,0,5,0402,SMD,LF	R9717,R9718,R9719,R9720,R9721,R9722	CRITICAL	LCDBKLT:PROD

SYNC_MASTER=J5_MLB_KEPLER SYNC_DATE=09/21/2011

PAGE TITLE

LCD Backlight Driver (LP8545)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.1MM	0.1MM

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	=4X_DIELECTRIC	?
CPU_ITP	*	=4x_DIELECTRIC	?
CPU_VCCSENSE	*	=6X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?
CPU_VREF	*	12 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=6X_DIELECTRIC	?
CLK_PCIE	*	=5X_DIELECTRIC	?

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	7 10 18
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	7 10 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	7 10 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	7 10 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	7 10 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	7 10 18
FDI_FSYNC	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	10 18
FDI_LSYNC	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	10 18
FDI_INT	CPU_50S	CPU_AGTL	FDI_INT	10 18
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	7 11 17
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	7 11 17
CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU_EDP_COMP	10
CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	10
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..0>	10 24
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	11 17
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	11 17
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	17 24
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	17 24
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLK_P	11 17
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLK_N	11 17
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	11 24
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	11 24
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	11 24
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	11 24
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	11 24
XDP_BPM	CPU_50S	CPU_ITP	XDP_BPM_L<3..0>	11 24
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7..4>	11 24
XDP_BDRESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L	11 24 25
XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	11 24
XDP_PREQ_L	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	11 24
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	11 39
CPU_PROC_SEL_L	CPU_50S	CPU_AGTL	CPU_PROC_SEL_L	11 20
CPU_PECI	CPU_50S	CPU_VID	CPU_PECI	11 20 40
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	11 39 40 61
XDP_CPU_PWRGD	CPU_50S	CPU_ITP	XDP_CPU_PWRGD	24
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	11 20 40
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	11 18
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	11 18 27
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	11 20 24
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2..0>	11
	CPU_50S	CPU_VID	CPU_VIDSOUT	13 61
	CPU_50S	CPU_VID	CPU_VIDSCLK	13 61
	CPU_50S	CPU_VID	CPU_VIDALERT_L	13 61
	CPU_55S	CPU_VID	CPU_VCCSA_VID<1..0>	13 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	13 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	13 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	13 63
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	13 63
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	13 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	13 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	10
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	10
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	10
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	10
CPU_VCCSASENSE	CPU_50S	CPU_AGTL	CPU_VCCSASENSE	13 58
CPU_MEM_VREF		CPU_VREF	PPCPU_MEM_VREFDQ_A	10 31
CPU_MEM_VREF		CPU_VREF	PPCPU_MEM_VREFDQ_B	10 31
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_A	28 31
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_B	29 31
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFCA_A	28 31
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFCA_B	29 31
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	24
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	24

SYNC_MASTER=JS_MLB SYNC_DATE=09/13/2012

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CPU Constraints

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4X_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3X_DIELECTRIC	?
MEM_CTRL2MEM	*	=3X_DIELECTRIC	?
MEM_CMD2CMD	*	=2X_DIELECTRIC	?
MEM_CMD2MEM	*	=3X_DIELECTRIC	?
MEM_DATA2DATA	*	=2X_DIELECTRIC	?
MEM_DATA2MEM	*	=3X_DIELECTRIC	?
MEM_DQS2MEM	*	=4X_DIELECTRIC	?
MEM_2OTHER	*	=6X_DIELECTRIC	?
MEM_DQBL2BL	*	=4X_DIELECTRIC	?
MEM_DQCH2CH	*	=6X_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_*	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_*	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_*	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQ_BYTE*	MEM_*	*	MEM_DATA2MEM
MEM_*_DQ_BYTE*	=SAME	*	MEM_DATA2DATA
MEM_A_DQ_BYTE*	MEM_A_DQ_BYTE*	*	MEM_DQBL2BL
MEM_B_DQ_BYTE*	MEM_B_DQ_BYTE*	*	MEM_DQBL2BL
MEM_A_DQ_BYTE*	MEM_B_DQ_BYTE*	*	MEM_DQCH2CH

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_*	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	*	*	MEM_2OTHER

DDR3 (Memory Down):

DQ signals should be matched within 0.508mm of associated DQS pair
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Chief River SFF Platform DG, Rev 0.7 (#460452), Section 2.6.3

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<0>	12 28 30
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<0>	12 28 30
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<1..0>	12 28 30
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<1>	12 28 30
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<0>	12 28 30
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<1>	12 28 30
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<0>	12 28 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	12 28 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	12 28 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L	12 28 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L	12 28 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L	12 28 30
MEM_A_DQ_BYTE0	MEM_50S	MEM_A_DQ_BYTE0	MEM_A_DQ<7..0>	7 12 28
MEM_A_DQ_BYTE1	MEM_50S	MEM_A_DQ_BYTE1	MEM_A_DQ<15..8>	7 12 28
MEM_A_DQ_BYTE2	MEM_50S	MEM_A_DQ_BYTE2	MEM_A_DQ<23..16>	7 12 28
MEM_A_DQ_BYTE3	MEM_50S	MEM_A_DQ_BYTE3	MEM_A_DQ<31..24>	7 12 28
MEM_A_DQ_BYTE4	MEM_50S	MEM_A_DQ_BYTE4	MEM_A_DQ<39..32>	7 12 28
MEM_A_DQ_BYTE5	MEM_50S	MEM_A_DQ_BYTE5	MEM_A_DQ<47..40>	7 12 28
MEM_A_DQ_BYTE6	MEM_50S	MEM_A_DQ_BYTE6	MEM_A_DQ<55..48>	7 12 28
MEM_A_DQ_BYTE7	MEM_50S	MEM_A_DQ_BYTE7	MEM_A_DQ<63..56>	7 12 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	12 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	12 28
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	12 28
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	12 28
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	12 28
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	12 28
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	12 28
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	12 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	12 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	12 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	12 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	12 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	12 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	12 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	12 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	12 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<0>	12 29 30
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<0>	12 29 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<1>	12 29 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<0>	12 29 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0>	12 29 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<1..0>	12 29 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0>	12 29 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	12 29 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L	12 29 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L	12 29 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L	12 29 30
MEM_B_DQ_BYTE0	MEM_50S	MEM_B_DQ_BYTE0	MEM_B_DQ<7..0>	7 12 29
MEM_B_DQ_BYTE1	MEM_50S	MEM_B_DQ_BYTE1	MEM_B_DQ<15..8>	7 12 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_B_DQ_BYTE2	MEM_B_DQ<23..16>	7 12 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_B_DQ_BYTE3	MEM_B_DQ<31..24>	7 12 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_B_DQ_BYTE4	MEM_B_DQ<39..32>	7 12 29
MEM_B_DQ_BYTE5	MEM_50S	MEM_B_DQ_BYTE5	MEM_B_DQ<47..40>	7 12 29
MEM_B_DQ_BYTE6	MEM_50S	MEM_B_DQ_BYTE6	MEM_B_DQ<55..48>	7 12 29
MEM_B_DQ_BYTE7	MEM_50S	MEM_B_DQ_BYTE7	MEM_B_DQ<63..56>	7 12 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	12 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	12 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	12 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	12 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	12 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	12 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	12 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	12 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	12 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	12 29
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	12 29
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	12 29
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	12 29
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	12 29
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	12 29
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	12 29

SYNC_MASTER=J5_MLB SYNC_DATE=09/13/2013

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Digital Video Signal Constraints

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=5:1_SPACING	?
SATA_ICOMP	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=5:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4:1_SPACING	?
USB_RBIAS	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 3.0 INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3	*	=5:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3	TOP,BOTTOM	=5:1_SPACING	?

SOURCE: CR SFF PLATFORM DESIGN GUIDE V0.7, TABLE 4-211, 1X1+

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
T25 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDRIN_P	7
T26 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDRIN_N	7
T25 SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDROUT_P	7
T26 SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDROUT_N	7
T25 SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDRIN_P	7
T26 SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDRIN_N	7
T26 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDROUT_N	7
T26 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDROUT_P	7
T26 SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RC_P	7 37
T26 SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RC_N	7 37
T26 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RC_N	7 37
T26 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RC_P	7 37
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P	7 17 37
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_N	7 17 37
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P	7 17 37
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_N	7 17 37
T232 SATA_HDD_D2R	SATA_90D	SATA	SATA_SSDRHDD_D2R_P	7 37
T233 SATA_HDD_D2R	SATA_90D	SATA	SATA_SSDRHDD_D2R_N	7 37
T234 SATA_HDD_R2D	SATA_90D	SATA	SATA_SSDRHDD_R2D_P	7 37
T235 SATA_HDD_R2D	SATA_90D	SATA	SATA_SSDRHDD_R2D_N	7 37
T33 PCH_SATA3_ICOMP	SATA_50SE	SATA_ICOMP	PCH_SATA3COMP	17
PCH_SATA_ICOMP	SATA_37SE	SATA_ICOMP	PCH_SATAICOMP	17
T236 USB_EXTB	USB_85D	USB	USB_EXTB_XHCI_P	19 26
T237 USB_EXTB	USB_85D	USB	USB_EXTB_XHCI_N	19 26
USB_EXTB	USB_85D	USB	USB_EXTB_EHCI_P	19 26
USB_EXTB	USB_85D	USB	USB_EXTB_EHCI_N	19 26
USB_HUB2_UP	USB_85D	USB	USB_HUB_UP_P	19 26
USB_HUB2_UP	USB_85D	USB	USB_HUB_UP_N	19 26
USB_EXTA	USB_85D	USB	USB_EXTA_P	19 38
USB_EXTA	USB_85D	USB	USB_EXTA_N	19 38
USB_EXTB	USB_85D	USB	USB_EXTB_P	7 26 36
USB_EXTB	USB_85D	USB	USB_EXTB_N	7 26 36
USB_EXTC	USB_85D	USB	USB_EXTD_P	
USB_EXTC	USB_85D	USB	USB_EXTD_N	
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P	7 32
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_N	7 32
USB_BT	USB_85D	USB	USB_BT_P	7 9 36
USB_BT	USB_85D	USB	USB_BT_N	7 9 36
USB_TPAD	USB_85D	USB	USB_TPAD_P	9 47
USB_TPAD	USB_85D	USB	USB_TPAD_N	9 47
USB_SMC	USB_85D	USB	USB_SMC_P	9 39
USB_SMC	USB_85D	USB	USB_SMC_N	9 39
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	19
T238 USB_EXTD	USB_85D	USB	USB_EXTD_XHCI_P	19 26
T239 USB_EXTD	USB_85D	USB	USB_EXTD_XHCI_N	19 26
T245 USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_P	38
T244 USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_N	38
T247 USB_CAMERA	USB_85D	USB	USB_CAMERA_P	19 32
T246 USB_CAMERA	USB_85D	USB	USB_CAMERA_N	19 32
T245 USB_EXTA	USB_85D	USB	USB_LT1_P	7 38
T243 USB_EXTA	USB_85D	USB	USB_LT1_N	7 38
T222 USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_P	19 36
T221 USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_N	19 36
T222 USB3_EXTB_RX	USB3_85D	USB3	USB3_EXTB_RX_P	7 19 36
T223 USB3_EXTB_RX	USB3_85D	USB3	USB3_EXTB_RX_N	7 19 36
T230 USB3_EXTA_TX	USB3_85D	USB3	USB3_EXTA_TX_P	19 38
T229 USB3_EXTA_TX	USB3_85D	USB3	USB3_EXTA_TX_N	7 19 38
T228 USB3_EXTA_RX	USB3_85D	USB3	USB3_EXTA_RX_P	7 19 38
T231 USB3_EXTA_RX	USB3_85D	USB3	USB3_EXTA_RX_N	7 19 38

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
T256 SYSCLK_CLK32K_RTC	CLK_SLOW_55S	CLK_SLOW	SYSCLK_CLK32K_RTC	17 25
T255 SYSCLK_CLK25M_SB	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB	17 25
T254	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB_R	17
T253 SYSCLK_CLK25M_ENET	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET	
T252	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET_R	
T251 SYSCLK_CLK25M_TBT	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_TBT	25 33
T250	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_TBT_R	33

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
LPC_AD	LPC_50S	LPC	LPC_AD<3..0>	7 17 39 41
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	7 17 39 41
LPC_RESET_L	LPC_50S	LPC	LPC_RESET_L	25
PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	19 25
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	7 25 39
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	7 25 41
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	7 17 42
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	7 17 42
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	17 42
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	17 42
SMBUS_SMC_1_S0_SCL	SMB_50S	SMB	SML_PCH_1_CLK	17 42
SMBUS_SMC_1_S0_SDA	SMB_50S	SMB	SML_PCH_1_DATA	17 42
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	17 51
	HDA_50S	HDA	HDA_BIT_CLK_R	17
HDA_SYNC	HDA_50S	HDA	HDA_SYNC	17 51
	HDA_50S	HDA	HDA_SYNC_R	17
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	17
	HDA_50S	HDA	HDA_RST_L	17 51
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	17 51
	HDA_50S	HDA	AUD_SDI_R	51
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	17 51
	HDA_50S	HDA	HDA_SDOUT_R	17 25
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	17 41
	SPI_55S	SPI	SPI_CLK	41
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	17 41
	SPI_55S	SPI	SPI_MOSI	41
SPI_MISO	SPI_55S	SPI	SPI_MISO	17 41
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	17 41
	SPI_55S	SPI	SPI_CS0_L	41
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	7 17 36
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	7 17 36
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	7 17 36
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_N	7 17 36
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_P	7 36
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_N	7 36
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	7 17 36
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	7 17 36
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	7 17 36
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_N	7 17 36
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_PI_P	7 36
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_PI_N	7 36
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_R2D_PI_P	7 36
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_R2D_PI_N	7 36
PCIE_CLK100M_PCH	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	7 17
PCIE_CLK100M_PCH	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	7 17
PCIE_CLK100M_TBT	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_TBT_P	7 17 33
PCIE_CLK100M_TBT	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_TBT_N	7 17 33
PCH_CLK96M	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	17
PCH_CLK96M	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	17
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	7 17
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	17
	CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	17
	CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN	7 17 25
PCIE_CLK100M_SSD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_SSD_P	7 9 17
PCIE_CLK100M_SSD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_SSD_N	7 9 17
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	7 9 17
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	7 9 17
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	7 17 36
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	7 17 36
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	7 17 36
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	7 17 36
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	7 9 17
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	7 9 17
PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	7 17
PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	7 17
PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_C_P<3..0>	7 9 33
PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_C_N<3..0>	7 9 33
PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_P<3..0>	7 33
PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_N<3..0>	7 33
PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_P<3..0>	7 9 33
PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_N<3..0>	7 9 33
PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_C_P<3..0>	7 33
PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_C_N<3..0>	7 33

SYNC_MASTER=J5_MLB SYNC_DATE=07/29/2013

PAGE TITLE: PCH Constraints 2

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP	TOP,BOTTOM	=7x_DIELECTRIC	?

NOTE: Thunderbolt high-speed nets are NOT directly assigned to TBTDP_*D physical rules.
TABLE_PHYSICAL_ASSIGNMENT symbols must be used to create the assignments.
Proper differential impedance depends on mDP connector used.
For 514-0637: R2D nets (SMT pins) = 80D, D2R nets (TH pins) = 100D

SOURCE: Bill Cornelius's Thunderbolt Routing Notes

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
HDMI_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
HDMI	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
HDMI	TOP,BOTTOM	=4x_DIELECTRIC	?

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_A_R2D_C_P<1..0>	7 33 69
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_A_R2D_C_N<1..0>	7 33 69
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_A_R2D_P<1..0>	7 69
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_A_R2D_N<1..0>	7 69
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3..1:2>	33 69
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3..1:2>	33 69
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3..1:2>	69
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3..1:2>	69
DP_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1>	69
DP_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1>	69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_A_D2R_C_P<1>	7 69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_A_D2R_C_N<1>	7 69
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_A_D2R_C_P<0>	7 69
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_A_D2R_C_N<0>	7 69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_A_D2R_P<1>	7 33 69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_A_D2R_N<1>	7 33 69
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_A_D2R_P<0>	7 33 69
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_A_D2R_N<0>	7 33 69
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_P	33 69
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_N	33 69
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_P	69
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_N	69
	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_P	69
	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_N	69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_A_D2R1_AUXDDC_P	69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_A_D2R1_AUXDDC_N	69
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_B_R2D_C_P<1..0>	7 33 70
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_B_R2D_C_N<1..0>	7 33 70
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_B_R2D_P<1..0>	7 70
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_B_R2D_N<1..0>	7 70
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3..1:2>	33 70
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3..1:2>	33 70
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3..1:2>	70
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3..1:2>	70
DP_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>	70
DP_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>	70
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_B_D2R_C_P<0>	7 70
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_B_D2R_C_N<0>	7 70
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_B_D2R_C_P<1>	7 70
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_B_D2R_C_N<1>	7 70
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_B_D2R_P<0>	7 33 70
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_B_D2R_N<0>	7 33 70
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_B_D2R_P<1>	7 33 70
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_B_D2R_N<1>	7 33 70
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_P	33 70
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_N	33 70
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_P	70
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_N	70
	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_P	70
	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_N	70
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_B_D2R1_AUXDDC_P	70
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_B_D2R1_AUXDDC_N	70

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_P	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_N	
TBT_SPI_CLK	TBT_SPI_55S	TBT_SPI	TBT_SPI_CLK	33
TBT_SPI_MOSI	TBT_SPI_55S	TBT_SPI	TBT_SPI_MOSI	33
TBT_SPI_MISO	TBT_SPI_55S	TBT_SPI	TBT_SPI_MISO	33
TBT_SPI_CS_L	TBT_SPI_55S	TBT_SPI	TBT_SPI_CS_L	33

Only used on hosts supporting Thunderbolt video-in

SYNC_MASTER=T29_CR SYNC_DATE=08/31/2011

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Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL (NET_TYPE)	SPACING (NET_TYPE)		
SMBUS_SMC_2_S3_SCL	SMB_50S	SMB	SMBUS_SMC_2_S3_SCL	7 39 42
SMBUS_SMC_2_S3_SDA	SMB_50S	SMB	SMBUS_SMC_2_S3_SDA	7 39 42
SMBUS_SMC_1_S0_SCL	SMB_50S	SMB	SMBUS_SMC_1_S0_SCL	7 39 42
SMBUS_SMC_1_S0_SDA	SMB_50S	SMB	SMBUS_SMC_1_S0_SDA	7 39 42
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	39 42
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	39 42
SMBUS_SMC_5_SCL	SMB_50S	SMB	SMBUS_SMC_5_SCL	
SMBUS_SMC_5_SDA	SMB_50S	SMB	SMBUS_SMC_5_SDA	
SMBUS_SMC_3_SCL	SMB_50S	SMB	SMBUS_SMC_3_SCL	39 42
SMBUS_SMC_3_SDA	SMB_50S	SMB	SMBUS_SMC_3_SDA	39 42

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL (NET_TYPE)	SPACING (NET_TYPE)		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	57
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_N	57
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	57
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_N	57

SYNC_MASTER=J5_MLB SYNC_DATE=07/29/2011

PAGE TITLE: SMC Constraints

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_CLK	*	GND_P2MM
GND	MEM_CMD	*	GND_P2MM
GND	MEM_CTRL	*	GND_P2MM
GND	MEM_*_DQ_BYTE*	*	GND_P2MM
GND	MEM_DQS	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB3	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB3	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 MM OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.1 MM	500 MIL		
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
USB3_85D	TOP			0.1 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

DDR3 Loaded Segment Constraint Relaxations

Alternate single ended and differential impedances between devices.

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_37S	BGA_MEM	MEM_50S
MEM_40S	BGA_MEM	MEM_50S
MEM_72D	BGA_MEM	MEM_85D

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
1TO1_DIFFPAIR	*	1:1_DIFFPAIR
SENSE_1TO1_55S	*	SENSE_1TO1_55S
THERM_1TO1_55S	*	THERM_1TO1_55S
DIFFPAIR	*	DIFFPAIR

Graphics, SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

D1 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P	9 10
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_N	9 10
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_N	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	TBT_THERMD_P	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	TBT_THERMD_N	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	DDR3THMSNS_D1_P	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	DDR3THMSNS_D1_N	45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_P	43 63
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_N	43 63
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_VDDQ_SENSE_P	13
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_VDDQ_SENSE_N	13
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCD_PANEL_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCD_PANEL_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V35_S3_MEM_P	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V35_S3_MEM_N	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_SSD_P	37 43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_SSD_N	37 43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_3V3_S0_SSD_R_P	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_3V3_S0_SSD_R_N	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_WLAN_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_WLAN_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_TBT_P	80
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_TBT_N	80
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V35_S3_MEM_R_P	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V35_S3_MEM_R_N	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_P	58 80
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_N	58 80
HDMI_CLK	HDMI_90D	HDMI	HDMI_IG_CLK_C_P	7 9 36
HDMI_CLK	HDMI_90D	HDMI	HDMI_IG_CLK_C_N	7 9 36
HDMI_DATA	HDMI_90D	HDMI	HDMI_IG_DATA_C_P<2..0>	7 9 36
HDMI_DATA	HDMI_90D	HDMI	HDMI_IG_DATA_C_N<2..0>	7 9 36

D1 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	7 36
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	7 36
	1TO1_DIFFPAIR		CHGR_CSI_R_P	57
	1TO1_DIFFPAIR		CHGR_CSI_R_N	57
	1TO1_DIFFPAIR		CHGR_CSO_R_P	57
	1TO1_DIFFPAIR		CHGR_CSO_R_N	57
USB_BT	USB_85D	USB	USB_BT_CONN_P	36
USB_BT	USB_85D	USB	USB_BT_CONN_N	36
USB_BT	USB_85D	USB	USB_BT_WAKE_P	36
USB_BT	USB_85D	USB	USB_BT_WAKE_N	36
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_P	7 53 55
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_N	7 53 55
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_P	7 53 55
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_N	7 53 55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_L_OUT_P	7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_L_OUT_N	7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_R_OUT_P	7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_R_OUT_N	7 53 55 78
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNSG_P	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNSG_N	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_P	43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_N	43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2G_P	43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2G_N	43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_P	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_N	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_P	44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_N	44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_P	44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_N	44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_P	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_N	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_P	43 61 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_N	43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_P	43 61 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_N	43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_P	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_N	43
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_P	51 54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_N	51 54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSUBIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSUBIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSUBIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSUBIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_LIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_LIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_RIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_RIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	HS_MIC_HI_RC	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	HS_MIC_LO_RC	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	HS_MIC_HI	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	HS_MIC_LO	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_L_OUT_P	7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_L_OUT_N	7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_R_OUT_P	7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_R_OUT_N	7 53 55 78
USB_TPAD	USB_85D	USB	USB_TPAD_R_P	26 47
USB_TPAD	USB_85D	USB	USB_TPAD_R_N	26 47
USB_HUB	USB_85D	USB	PU_USBHUB_DN4_P	9
USB_HUB	USB_85D	USB	PU_USBHUB_DN4_N	9
		SB_POWER	PP3V3_S5	7 8
		SB_POWER	PP3V3_S0	7 8
		SB_POWER	PP1V5_S3RS0_CPUDDR	8
		GND	GND	

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D1 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,BGA_MEM	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
50_OHM_SE	*	Y	0.070 MM	0.070 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.105 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.120 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.190 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.124 MM	0.124 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.124 MM	0.124 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.089 MM	0.089 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.089 MM	0.089 MM		0.180 MM	0.180 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.110 MM	0.110 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.081 MM	0.081 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.081 MM	0.081 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.090 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.079 MM	0.079 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE

Stackup-Defined Spacing Rules

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	TOP,BOTTOM	0.1 MM	?
1:1_SPACING	ISL3,ISL4,ISL9,ISL10	0.1 MM	?
1:1_SPACING	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.101 MM	?

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.053 MM	?
1X_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.101 MM	?

J4 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
J4P1 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P	9 33
J4P2 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N	9 33
J4P3 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P	9 33
J4P4 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N	9 33
J4P5 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	9 33
J4P6 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	9 33
J4P7 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	9 33
J4P8 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	9 33
J4P72 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P	33
J4P73 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N	33
J4P74 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P	33
J4P75 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N	33
J4P76 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	33
J4P77 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	33
J4P78 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	33
J4P79 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	33
J4P62 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	9 67
J4P63 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	9 67
J4P59 DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_C_P	9 67
J4P60 DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_C_N	9 67
J4P57 DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_P	7 67
J4P58 DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_N	7 67
J4P56 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	67
J4P55 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	67
J4P54 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0>	
J4P53 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0>	
J4P41 USB3_EXTB_RX	USB3_85D	USB3	USB3_EXTB_RX_RC_P	7 36
J4P42 USB3_EXTB_RX	USB3_85D	USB3	USB3_EXTB_RX_RC_N	7 36
J4P43 USB3_EXTA_RX	USB3_85D	USB3	USB3_EXTA_RX_F_P	7 38
J4P44 USB3_EXTA_RX	USB3_85D	USB3	USB3_EXTA_RX_F_N	7 38
J4P45 USB3_EXTA_TX	USB3_85D	USB3	USB3_EXTA_TX_C_P	7 38
J4P46 USB3_EXTA_TX	USB3_85D	USB3	USB3_EXTA_TX_C_N	7 38
J4P47 USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_C_P	7 36
J4P48 USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_C_N	7 36

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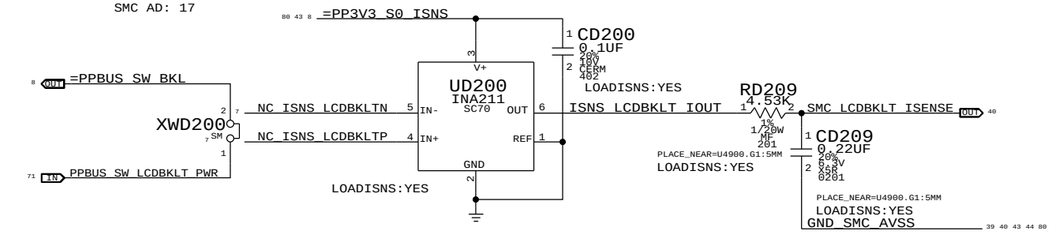
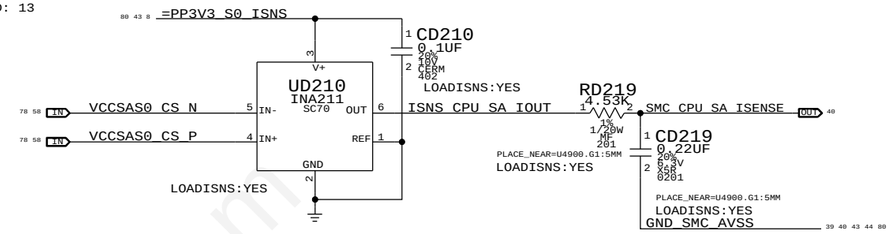
LCD Backlight Current Sense (IBLC)

Gain: 500x. EDP: 0.9 A
Rsense: 0.005 (RD200 / XWD200)
V across Rsense: 4.5 mV
SMC AD: 17



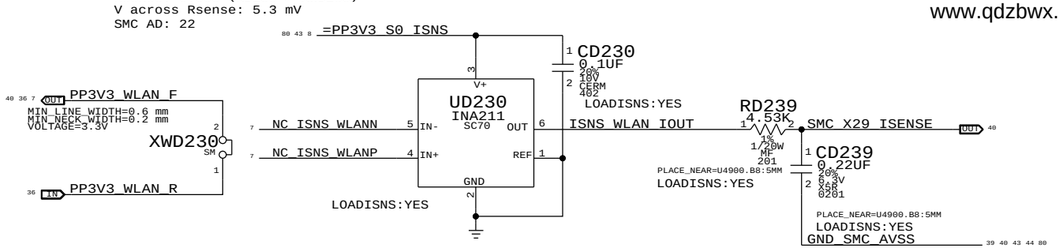
CPU SA Current Sense (IC2C)

Gain: 500x. EDP: 6 A
Rsense: 0.001 (R7140)
V across Rsense: 6 mV
SMC AD: 13



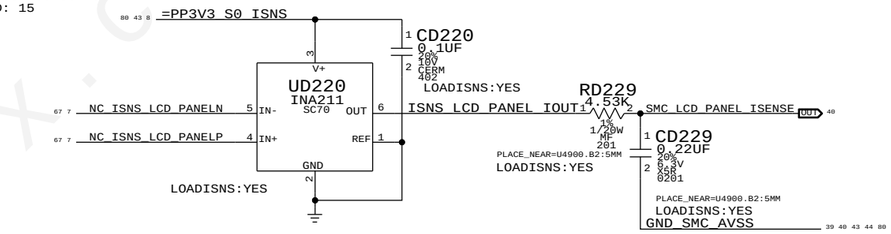
Airport X29 Current Sense (IAPC)

Gain: 500x. EDP: 1.06 A
Rsense: 0.005 (RD230 / XWD230)
V across Rsense: 5.3 mV
SMC AD: 22



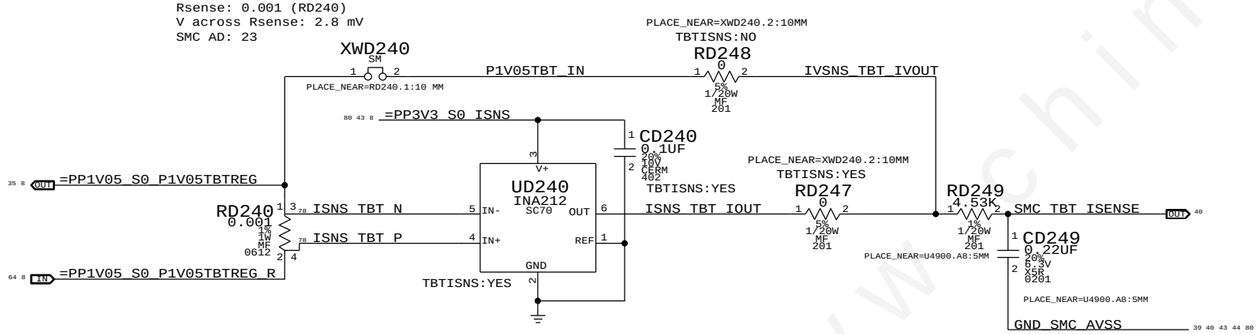
LCD Panel Current Sense (ILDC)

Gain: 500x. EDP: 1 A
Rsense: 0.005 (R9020, XW9020)
V across Rsense: 5 mV
SMC AD: 15



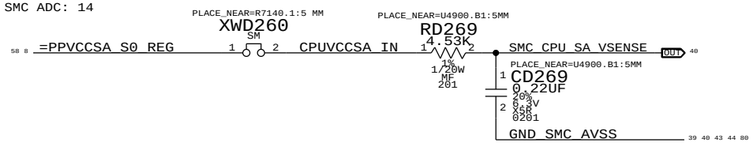
Thunderbolt TBT Current/Voltage Sense (IHSP/VHSP)

Gain: 1000x. EDP: 2.8 A
Rsense: 0.001 (RD240)
V across Rsense: 2.8 mV
SMC AD: 23



CPU SA Voltage Sense (VC2C)

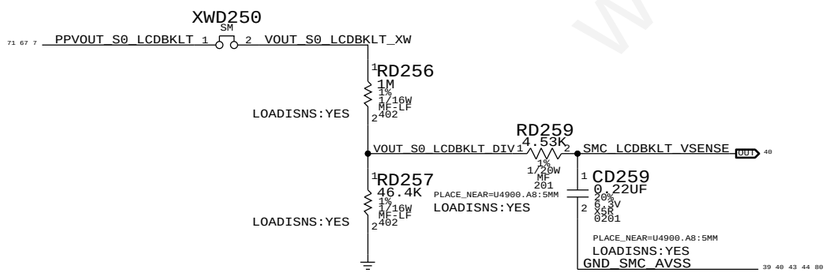
Gain: 1x
SMC ADC: 14



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	3	RES,MTL FILM,100K,1/16W,0201,SMD,LF	CD209,CD219,CD229		LOADISNS:NO
117S0008	3	RES,MTL FILM,100K,1/16W,0201,SMD,LF	CD239,CD259		LOADISNS:NO

LCD Backlight Voltage Sense (VBLC)

Gain: 0.04434



SYNC_MASTER=D1_SENSORS SYNC_DATE=07/11/2017

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Power Sensors: Extended

Apple Inc.

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