

SYNC MASTER=113 MLB

SYNC DATE=11/18/2011

System Block Diagram

Apple Inc.

051-9276

2.7.0

2 OF 109

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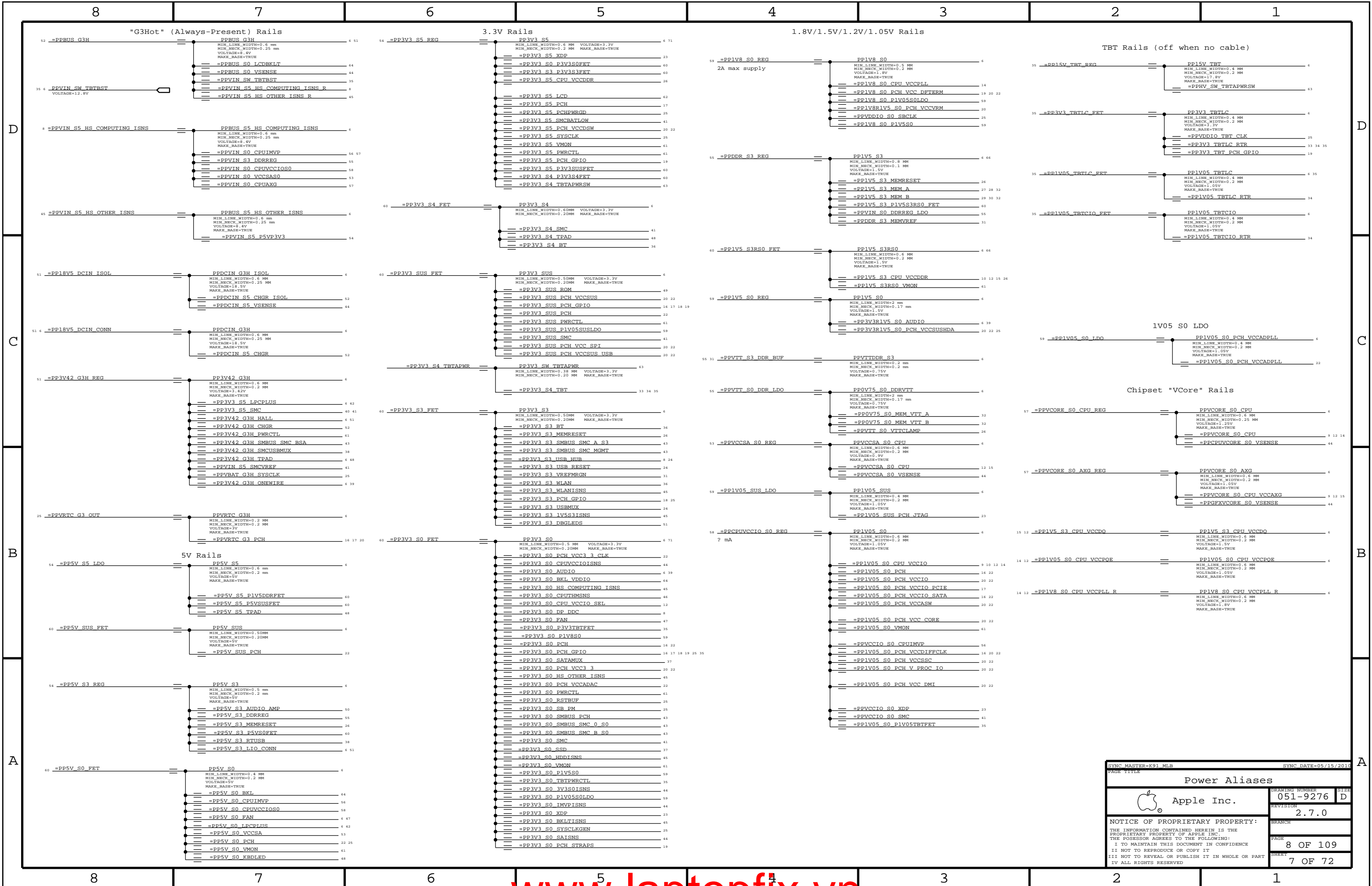


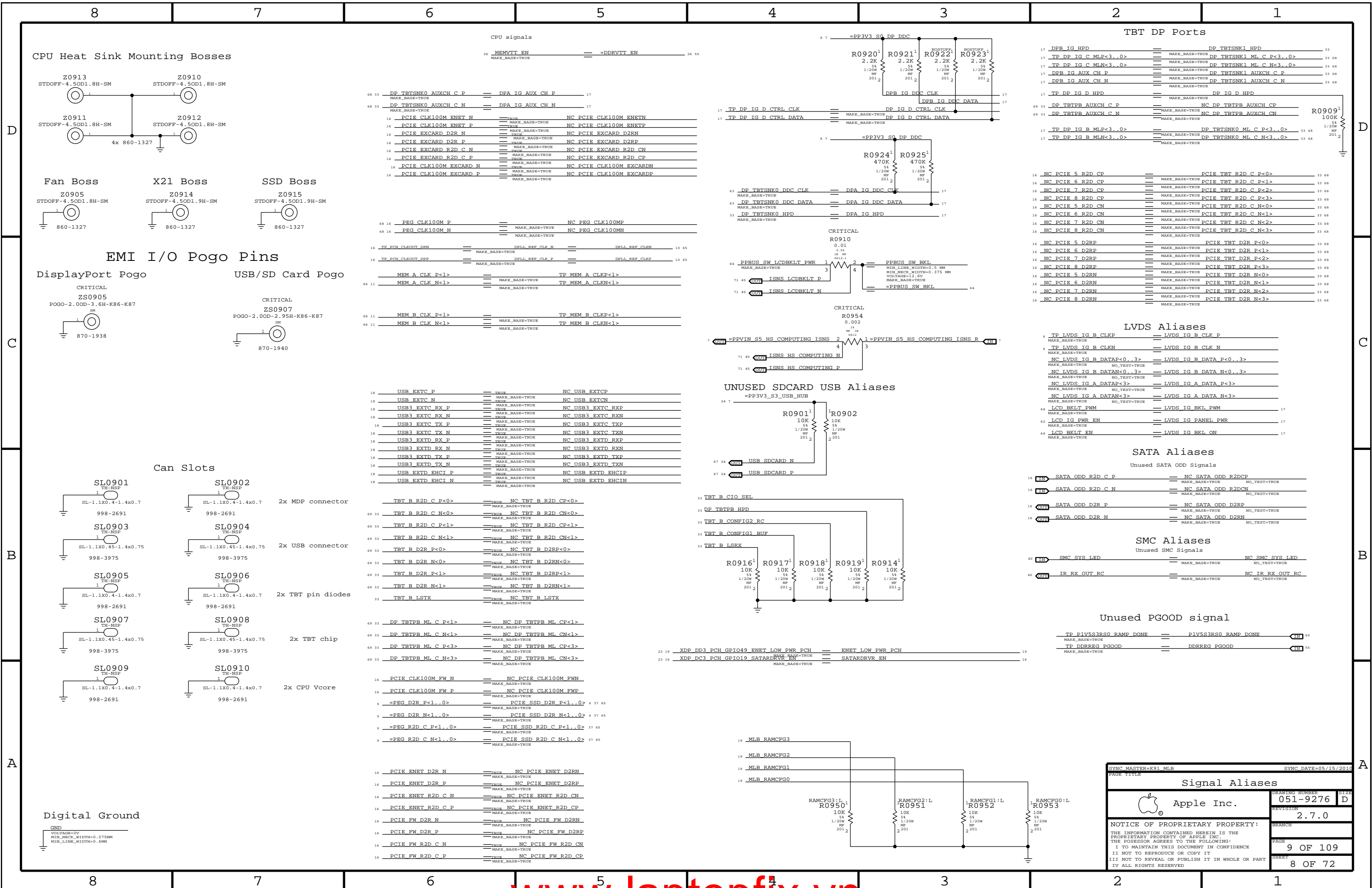
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-3937	1	J11 MIB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
607-9089	1	OMN PTS,PCBA,MIB,J11	OMNPTS	CRITICAL	J11_OMNPTS

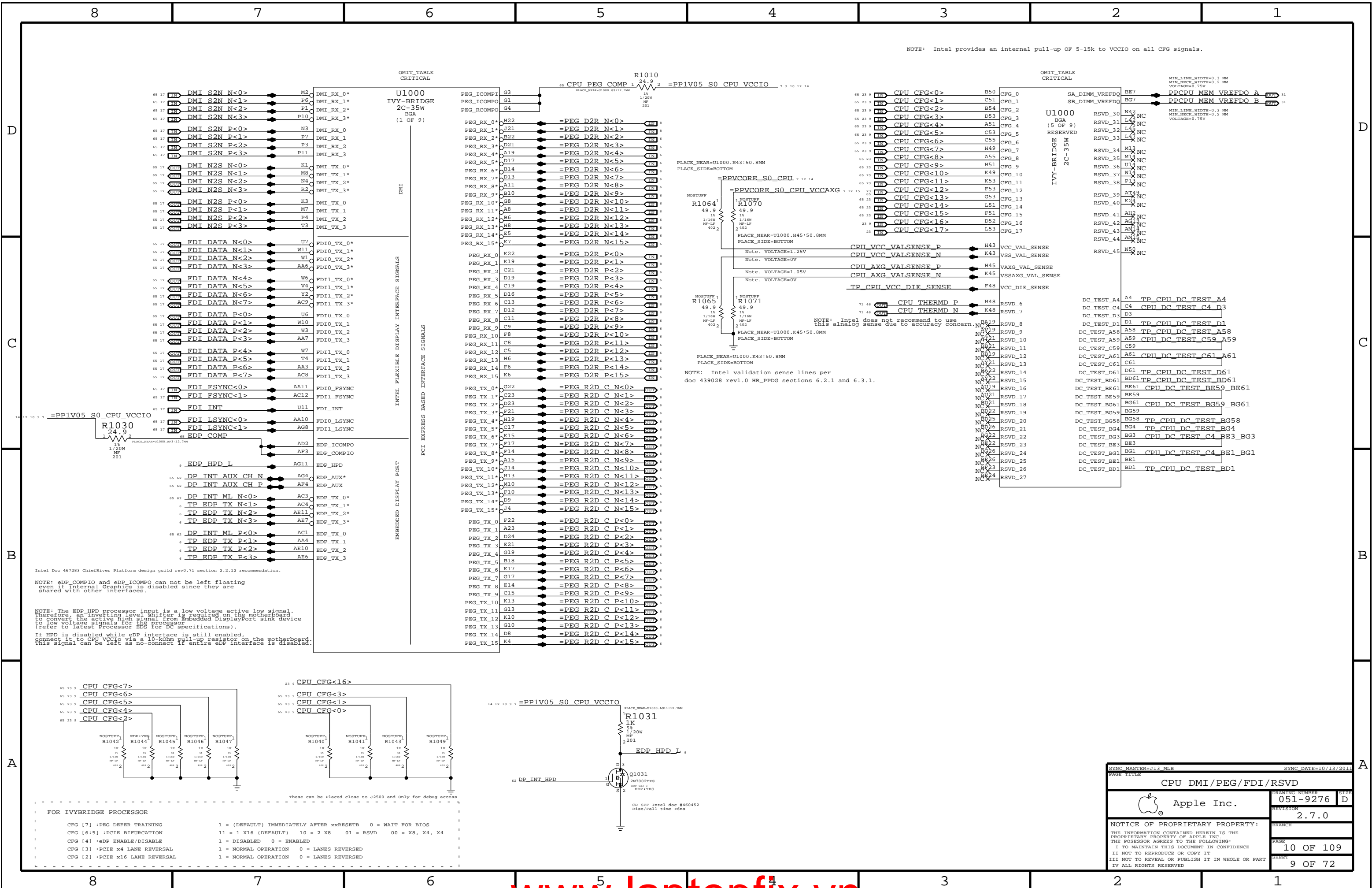
SYNC MASTER=K21 MLB		SYNC DATE=11/16/2010	
PAGE TITLE			
K78 BOM Variants			
	Apple Inc.		DRAWING NUMBER 051-9276
			REVISION 2.7.0
			BRANCH 
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			SHEET 4 OF 72



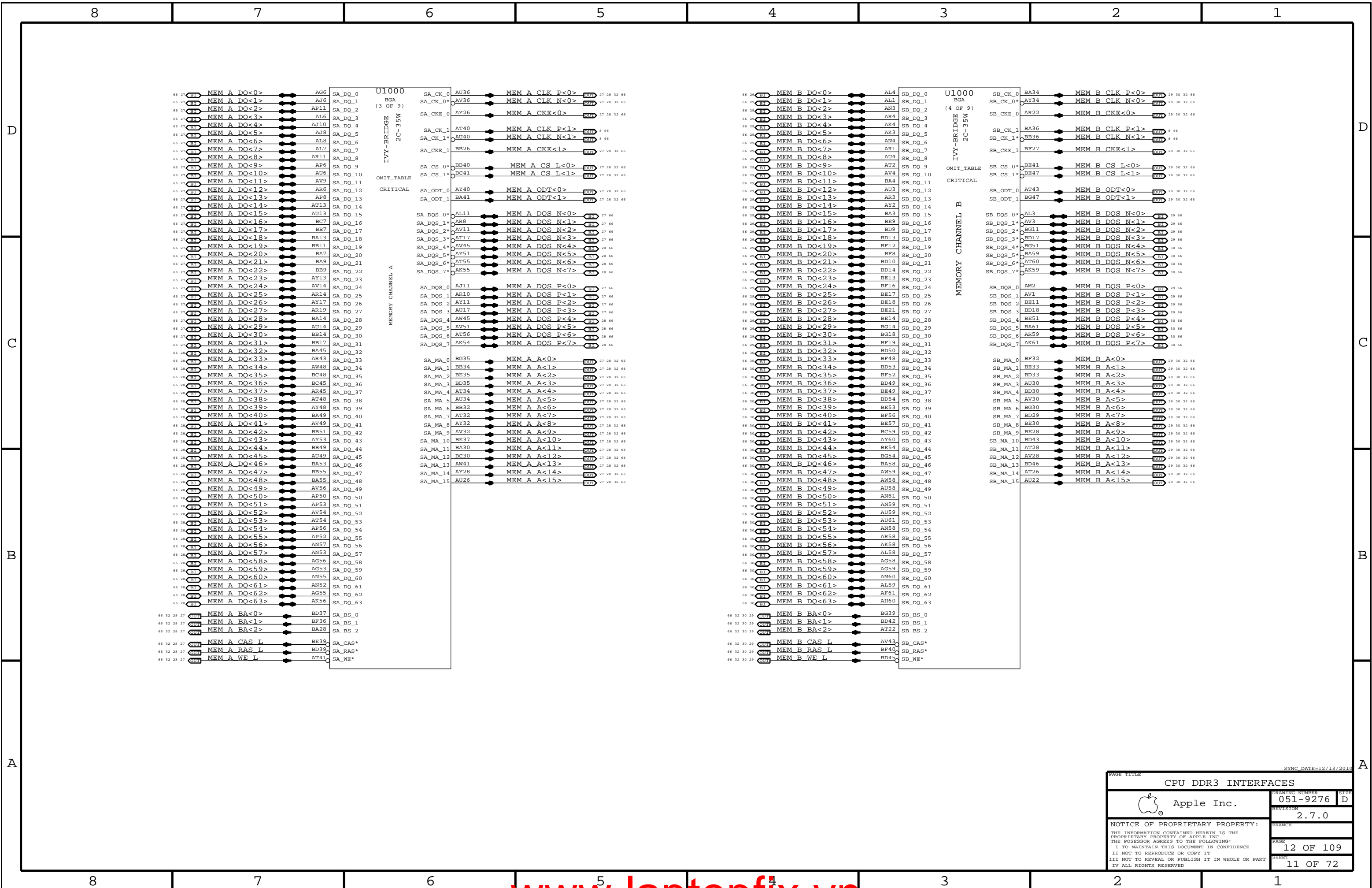
8	7	6	5	4	3	2	1
Functional Test Points				Misc Voltages & Control Signals			
J4001: AirPort / BT Connector				J5600: Fan Connector		NC EDP TXP<0..3>	
FUNC_TEST				FUNC_TEST		MAKE_BASE=TRUE	
PP3V3 WLAN F (Need 6 TPas)				=PP5V S0 FAN		TP EDP TX P<0..3>	
WIFI EVENT L				FAN_RT TACH		NC EDP TXN<0..3>	
PCIE AP R2D N				FAN_RT PWM		MAKE_BASE=TRUE	
PCIE AP R2D P				(Need to add 1 GND TP)		TP EDP AUX P	
PCIE CLK100M AP N				J5700: IPD Flex Connector		NC EDP AUXN	
PCIE CLK100M AP P				FUNC_TEST		MAKE_BASE=TRUE	
USB BT CONN P				SMC PME S4 WAKE L		TP CPU THERMDA	
USB BT CONN N				PP5V TPAD FILT		NC CPU THERMDC	
PCIE AP D2R P				=PP3V42 G3H TPAD		MAKE_BASE=TRUE	
PCIE AP D2R N				PP3V3 TPAD CONN		NC CPU RSVD<30..45>	
PCIE WAKE L				USB TPAD P		MAKE_BASE=TRUE	
AP RESET CONN L				USB TPAD N		TP CPU RSVD<8..27>	
AP CLKREQ O L				=I2C TPAD SDA			
PP3V3 S3RS4 BT F				=I2C TPAD SCL			
(Need to add 8 GND TPas)				SMC ONOFF L			
				SMC LID			
				SMC TPAD RST L			
				(Need to add 5 GND TPas)			
J4501: SATA SSD Connector				J6900: DC-In Connector			
FUNC_TEST				FUNC_TEST			
PP3V3 S0 SSD FLT (Need 5 TPas)				=PP18V5 DCIN CONN			
SATA SSD D2R P				=PP5V S3 LIO CONN			
SATA SSD D2R N				(Need to add 5 GND TPas)			
SATA SSD R2D N				J6903: Speaker Connector			
SATA SSD R2D P				FUNC_TEST			
SMC OOB1 RX L				SPKRAMP ROUT P			
SMC OOB1 TX L				SPKRAMP ROUT N			
PCIE SSD D2R N<1>				(Need to add 3 GND TPas)			
PCIE SSD D2R P<1>							
PCIE SSD R2D N<1>							
PCIE SSD R2D P<1>							
PCIE CLK100M SSD N							
PCIE CLK100M SSD P							
SSD CLKREQ L							
SSD RESET L							
SATA PCIE SEL							
SSD P3V3S0 EN							
(Need to add 6 GND TPas)							
J4700: LIO Connector				J6950: Battery Connector			
FUNC_TEST				FUNC_TEST			
=PP3V42 G3H ONEWIRE				PPVBAT G3H CONN			
=PP3V3 S0 AUDIO				=SMBUS BATT SCL			
=PP3V3R1V5 S0 AUDIO				=SMBUS BATT SDA			
SYS ONEWIRE				SYS DETECT L			
SMC BC ACOK				(Need to add 4 GND TPas near J6950 and 1 for shield)			
=USB PWR EN				J9000: Internal DP Connector			
=I2C LIO SDA				FUNC_TEST			
=I2C LIO SCL				PPVOUT SW LCDBKLT			
=I2C MIKEY SCL				PP3V3 SW LCD			
=I2C MIKEY SDA				I2C TCON SDA R			
AUD IPHS SWITCH EN				LED RETURN 6			
AUD IP PERIPHERAL DET				LED RETURN 5			
AUD I2C INT L				LED RETURN 4			
AUD GPIO 3				LED RETURN 3			
SPKRAMP INR N				LED RETURN 2			
SPKRAMP INR P				LED RETURN 1			
USB EXTB N				DP INT HPD CONN			
USB EXTB P				DP INT AUX CH C N			
USB CAMERA N				DP INT AUX CH C P			
USB CAMERA P				DP INT ML F P<0>			
HDA SDOUT				DP INT ML F N<0>			
HDA BIT CLK				I2C TCON SCL R			
HDA SDIN0				(Need to add 5 GND TPas)			
USB EXTB OC L				J5715: KB BKLT Connector			
HDA RST L				FUNC_TEST			
HDA SYNC				KBDLED FB			
USB3 EXTB RX RC N				KBDLED ANODE			
USB3 EXTB RX RC P				(Need to add 2 GND TPas)			
USB3 EXTB TX C P				J6955: HALL EFFECT Connector			
USB3 EXTB TX C N				FUNC_TEST			
(Need to add 5 GND TPas)				SMC LID R			
				=PP3V42 G3H HALL			
J5100: LPC+SPI Connector							
FUNC_TEST							
=PP3V3 S5 LPCPLUS							
=PP5V S0 LPCPLUS							
LPC AD<3..0>							
SPI ALT MOSI							
SPI ALT MISO							
LPC FRAME L							
PM CLKRUN L							
SMC TMS							
LPCPLUS RESET L							
SMC TDO							
TP SMC TRST L							
TP SMC MD1							
SMC TX L							
LPC CLK33M LPCPLUS							
SPIROM USE MLB							
SPI ALT CLK							
SPI ALT CS L							
LPC SERIRO							
LPC PMRDWN L							
SMC TDI							
SMC TCK							
SMC RESET L							
SMC ROMBOOT							
SMC RX L							
LPCPLUS GPIO							
(Need to add 6 GND TPas)							

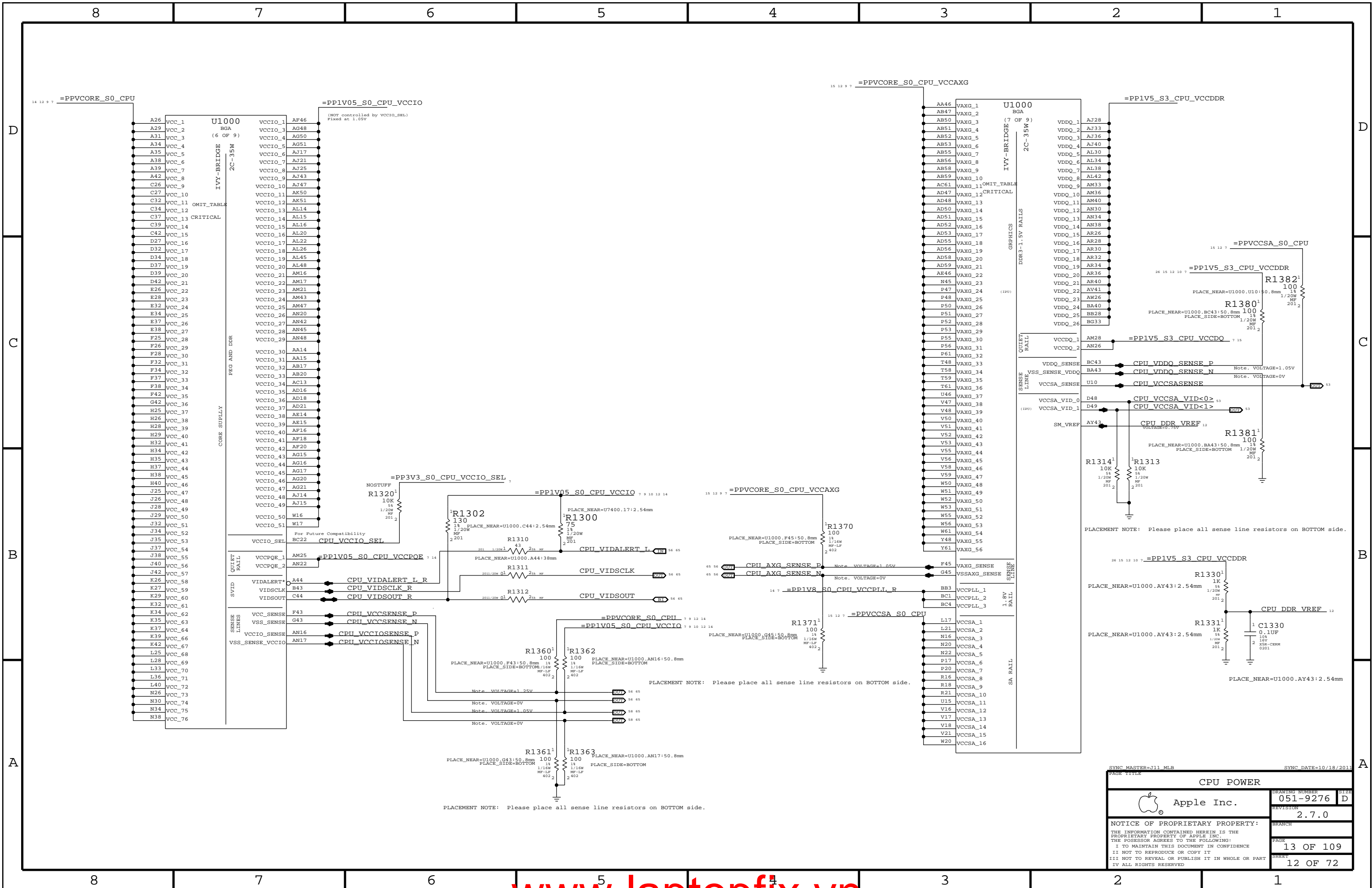





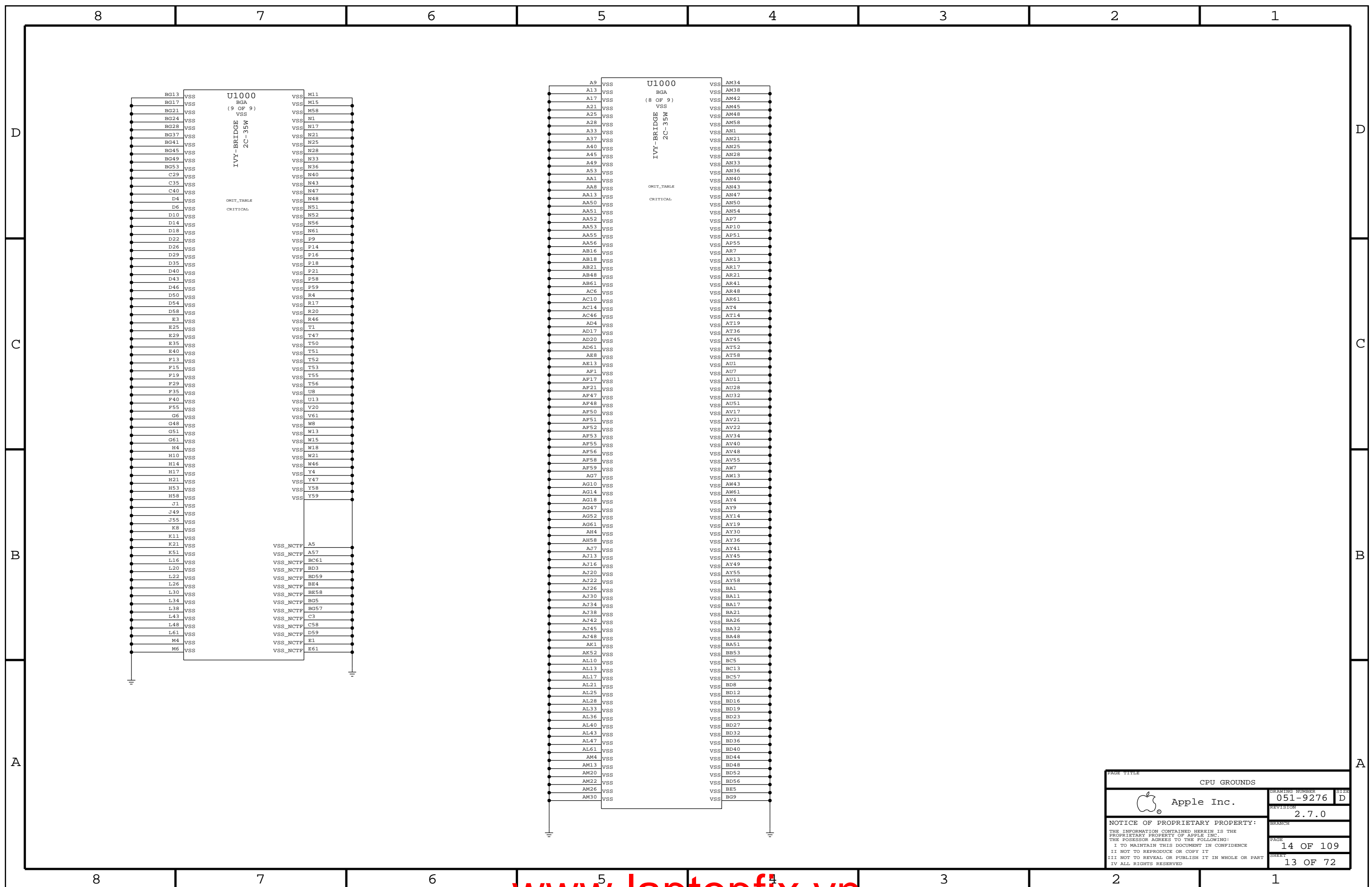


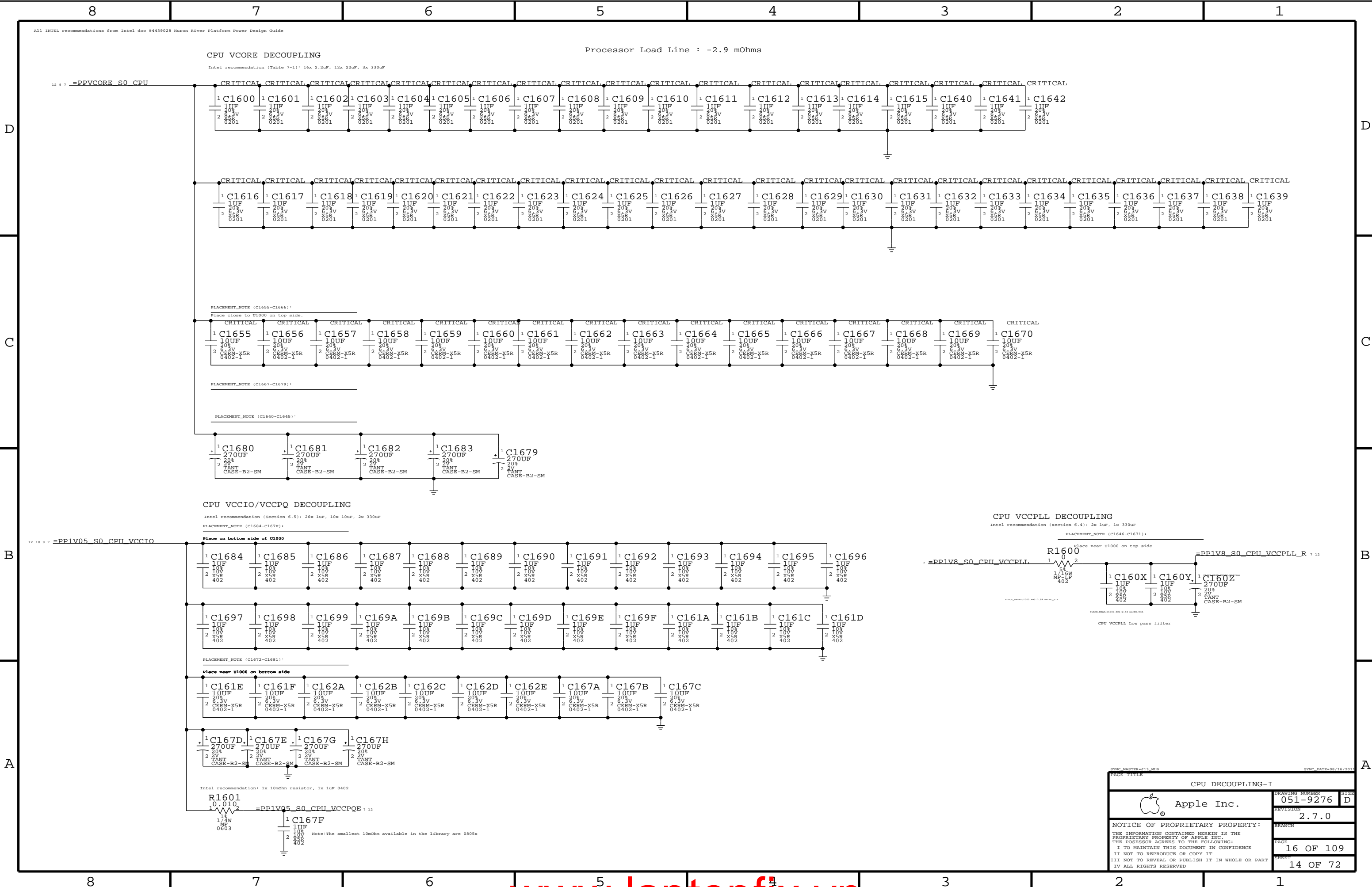







SYNC MASTER=J11 MLB		SYNC DATE=10/18/2011	
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CPU POWER			
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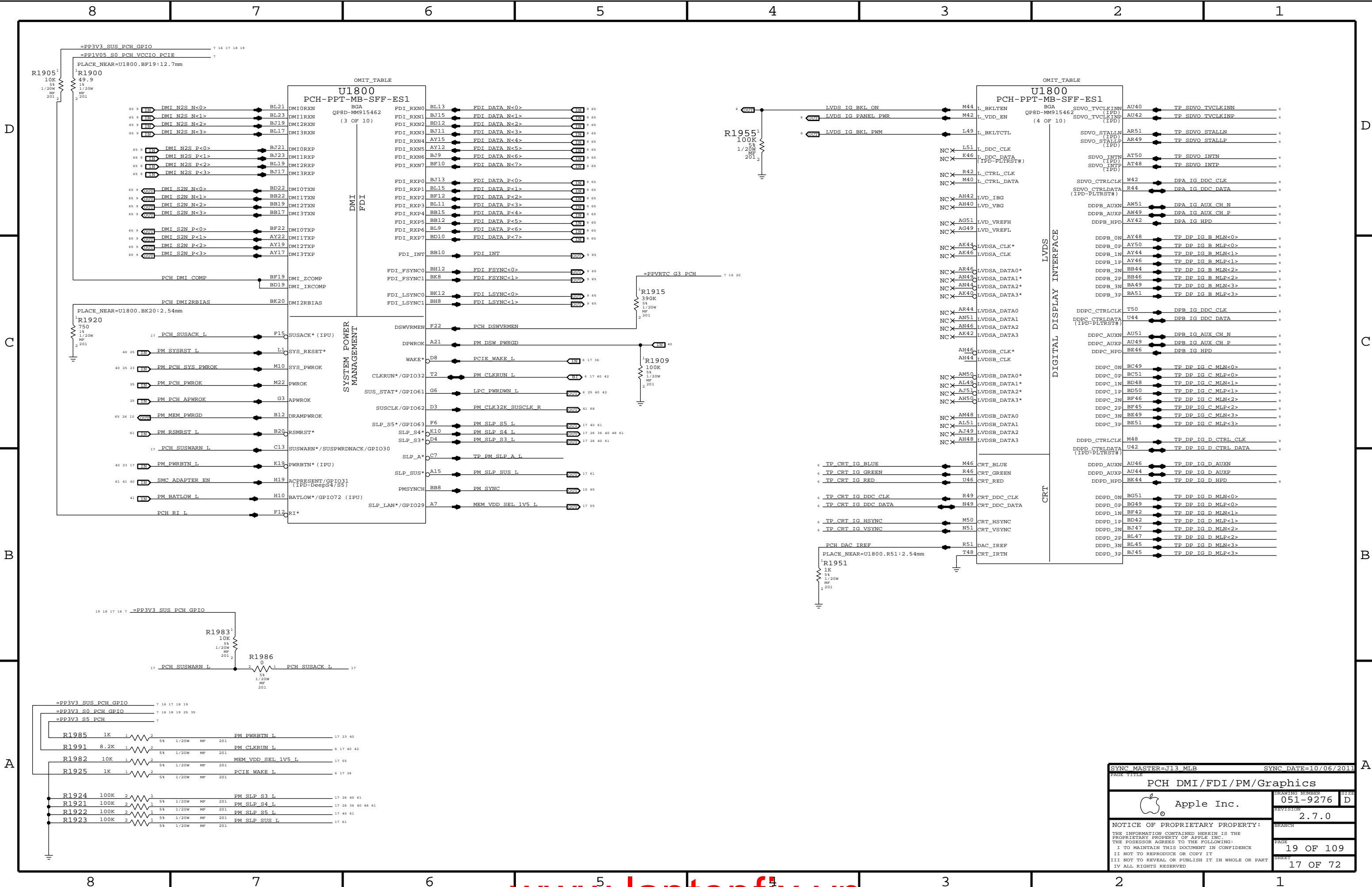


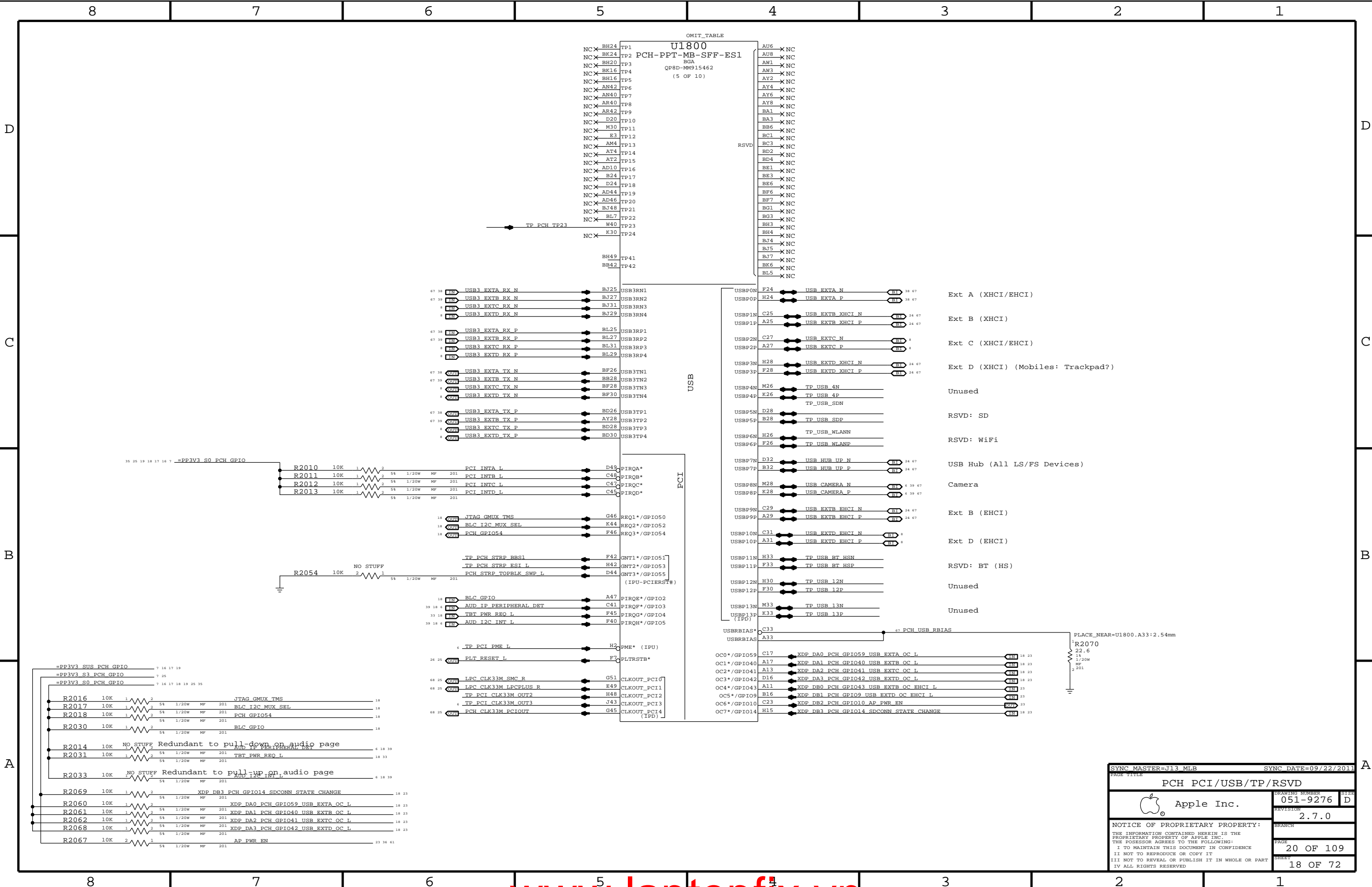


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SYNC MASTER=J13 MLB

SYNC DATE=09/22/2011

PCH PCI/USB/TP/RSVD

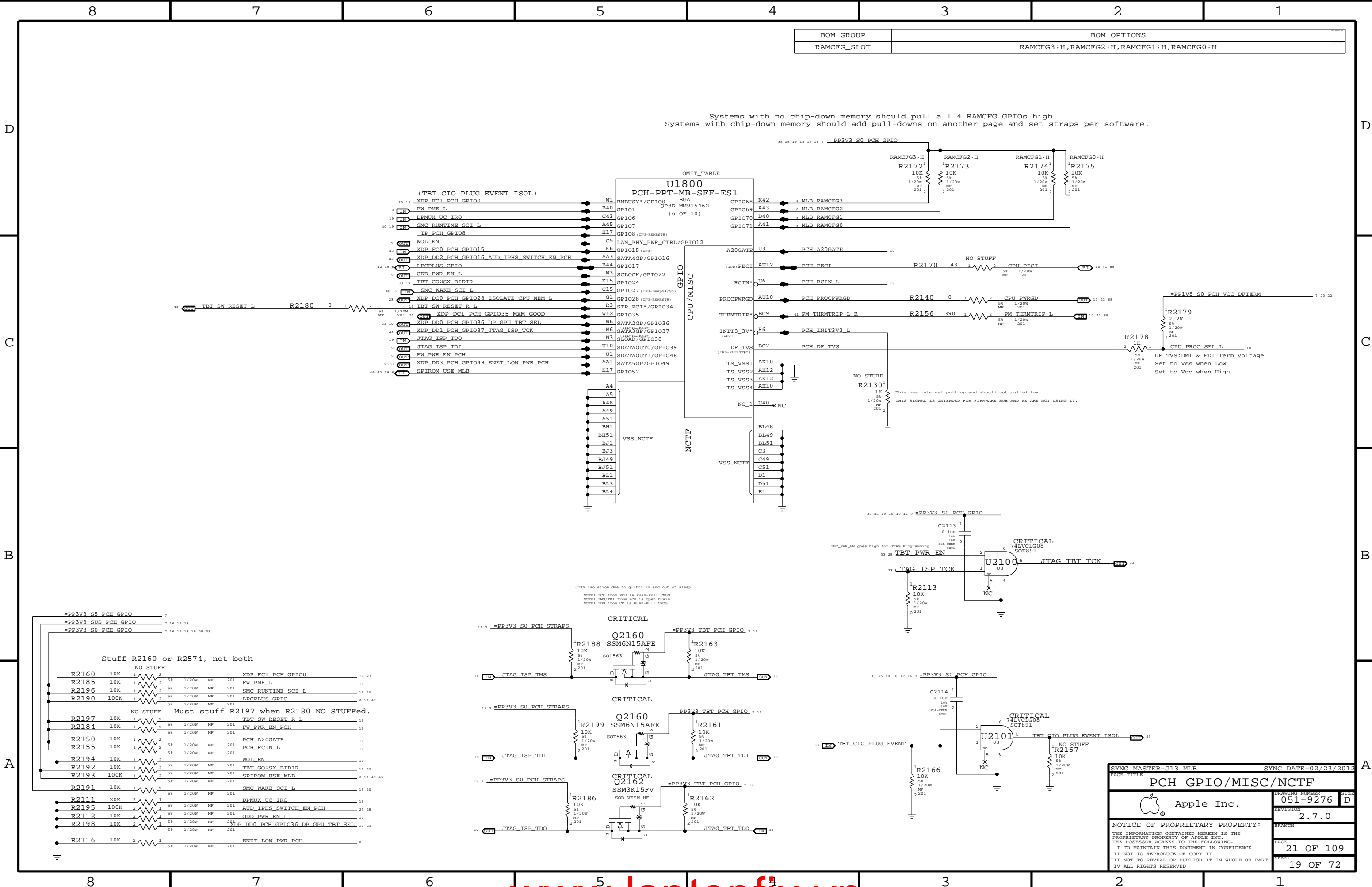
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BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H, RAMCFG2:H, RAMCFG1:H, RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.  
Systems with chip-down memory should add pull-downs on another page and set straps per software.

SYNC MASTER=J13 MLB

SYNC DATE=02/23/2012

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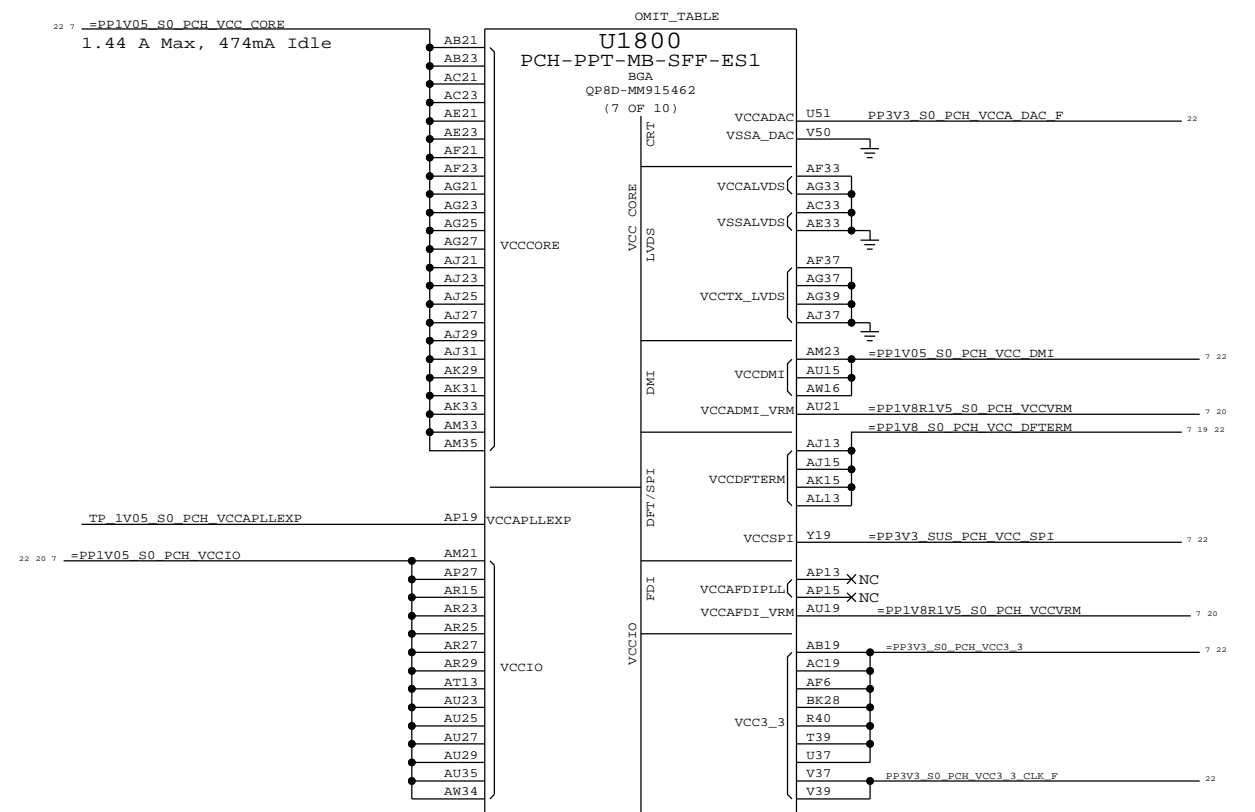
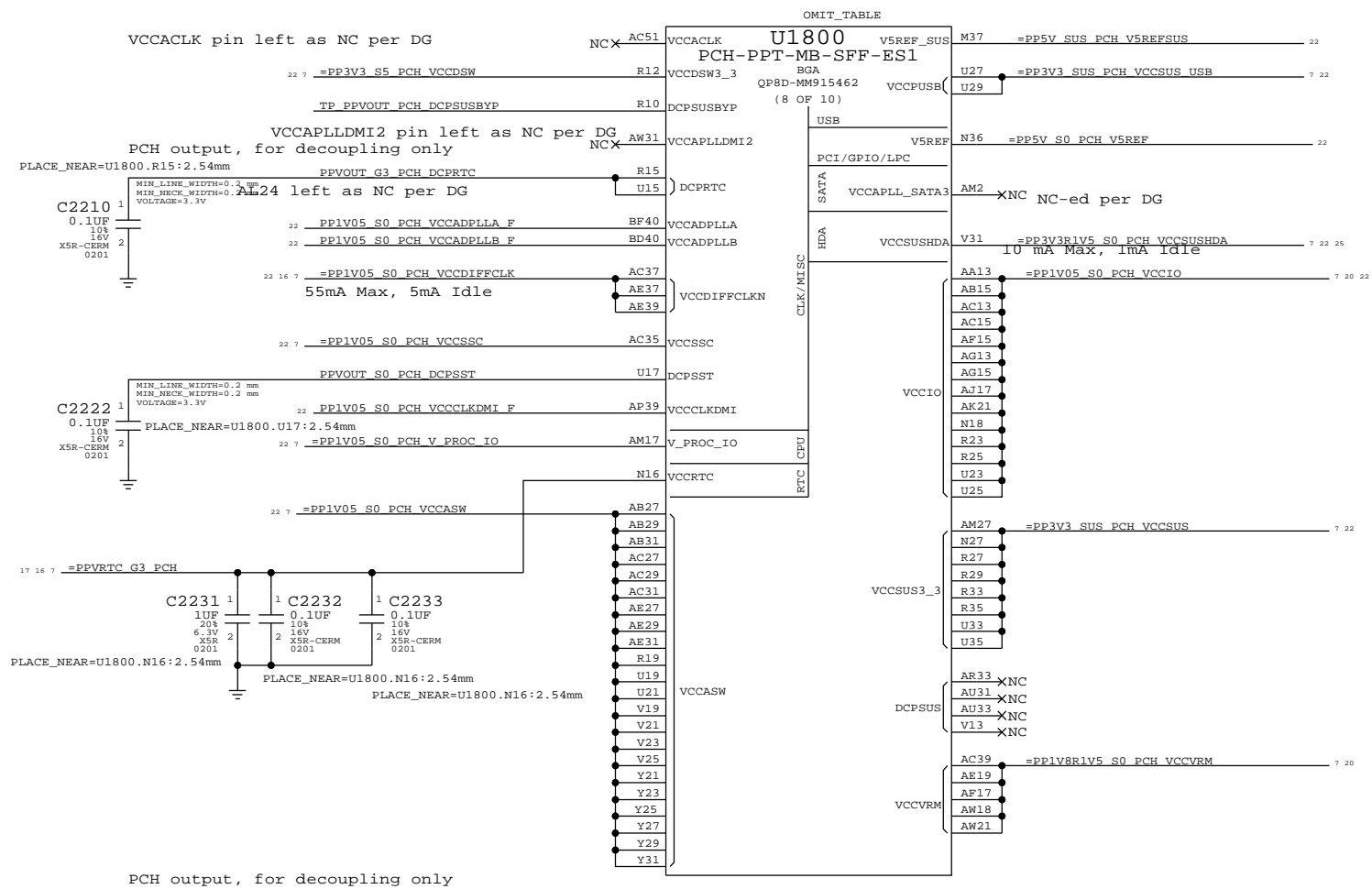
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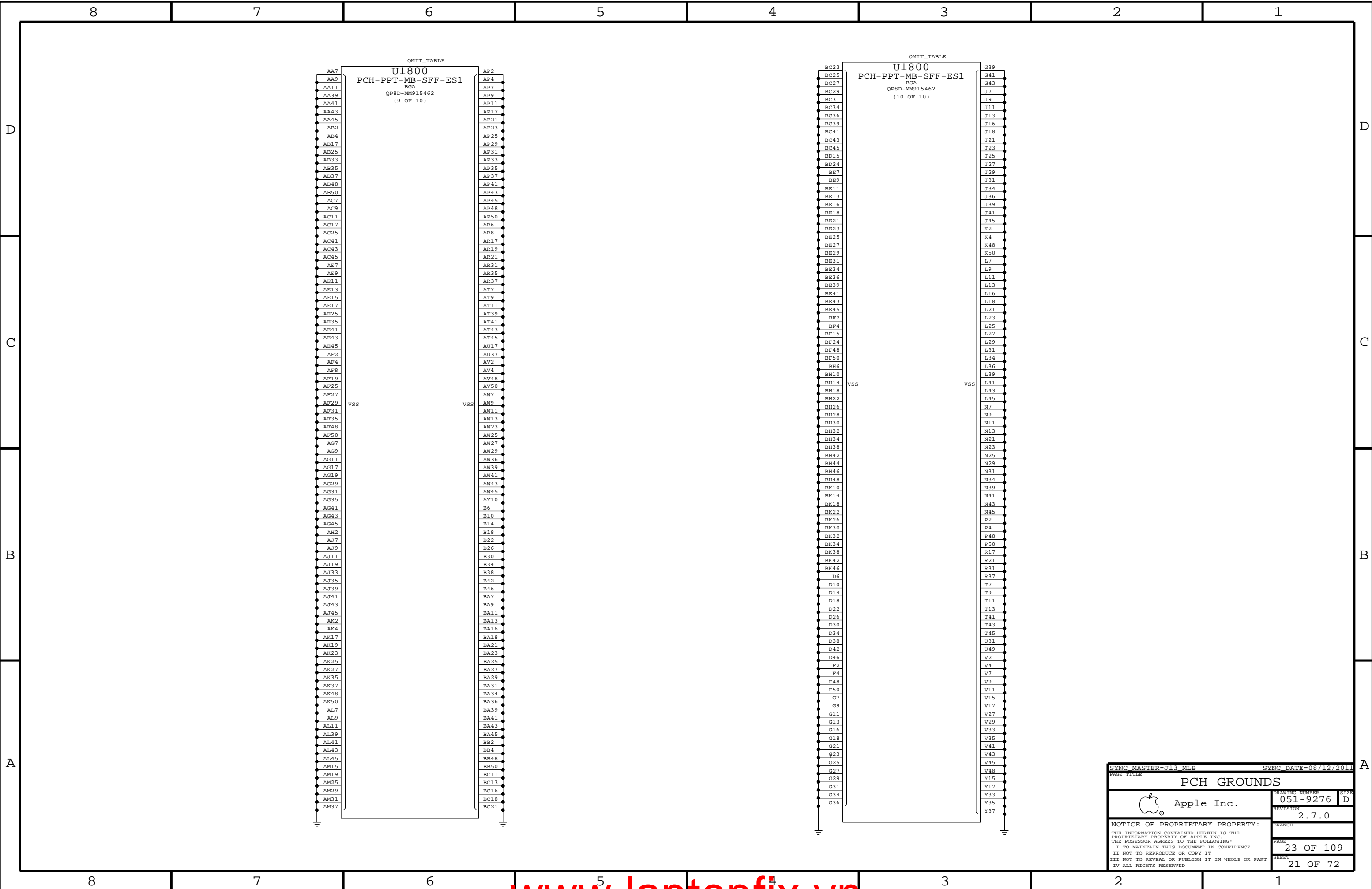
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SYNC MASTER=J13 MLB

SYNC DATE=08/12/2011

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PCH GROUNDS

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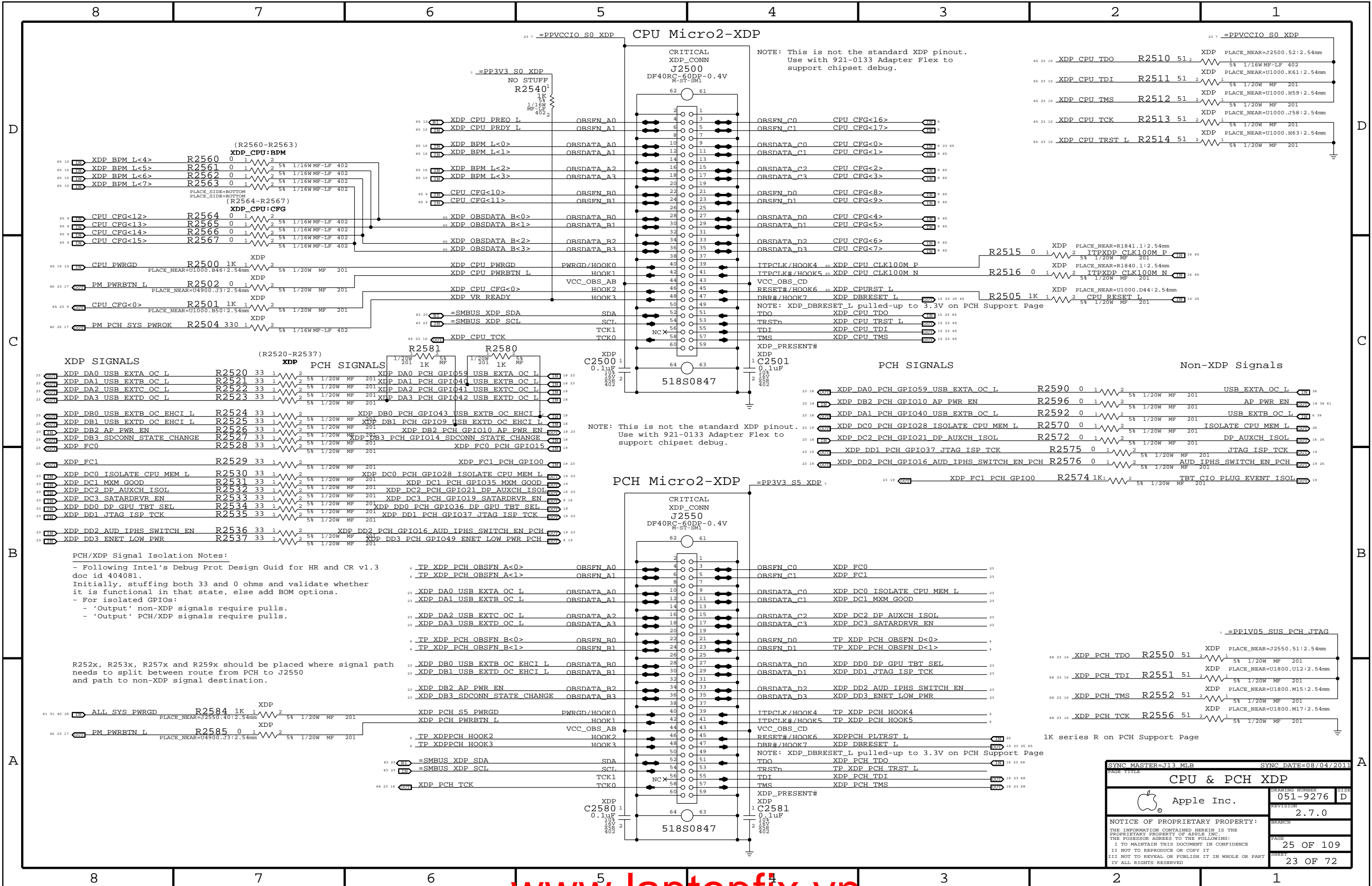
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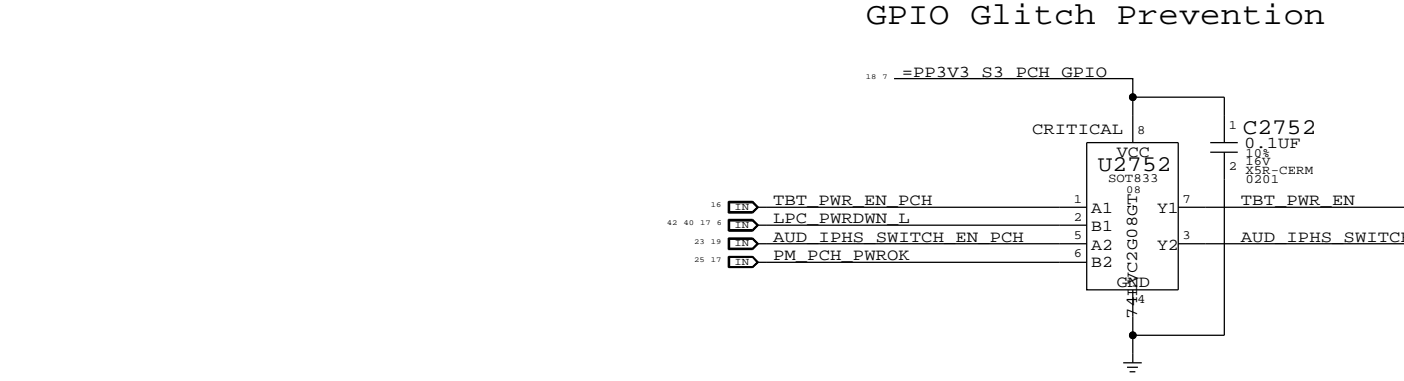
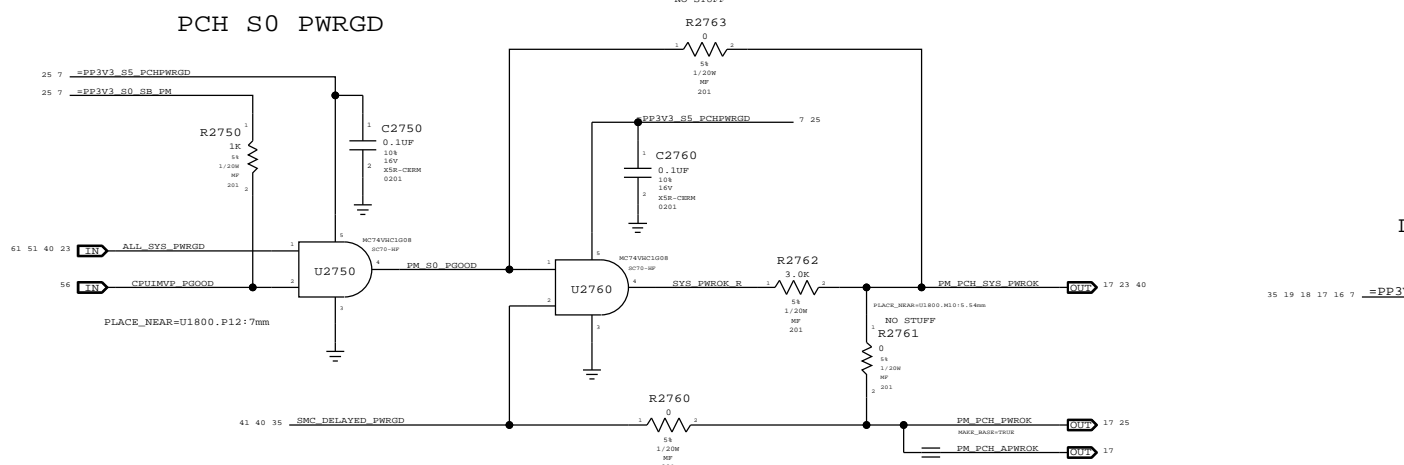
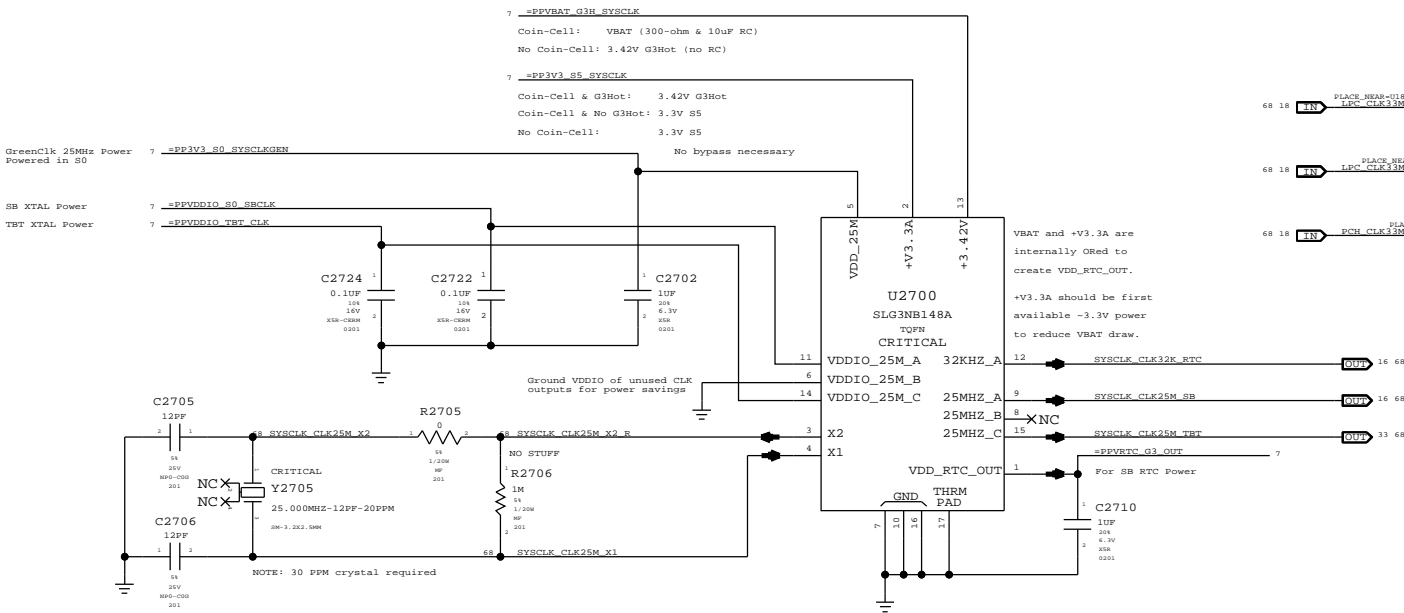




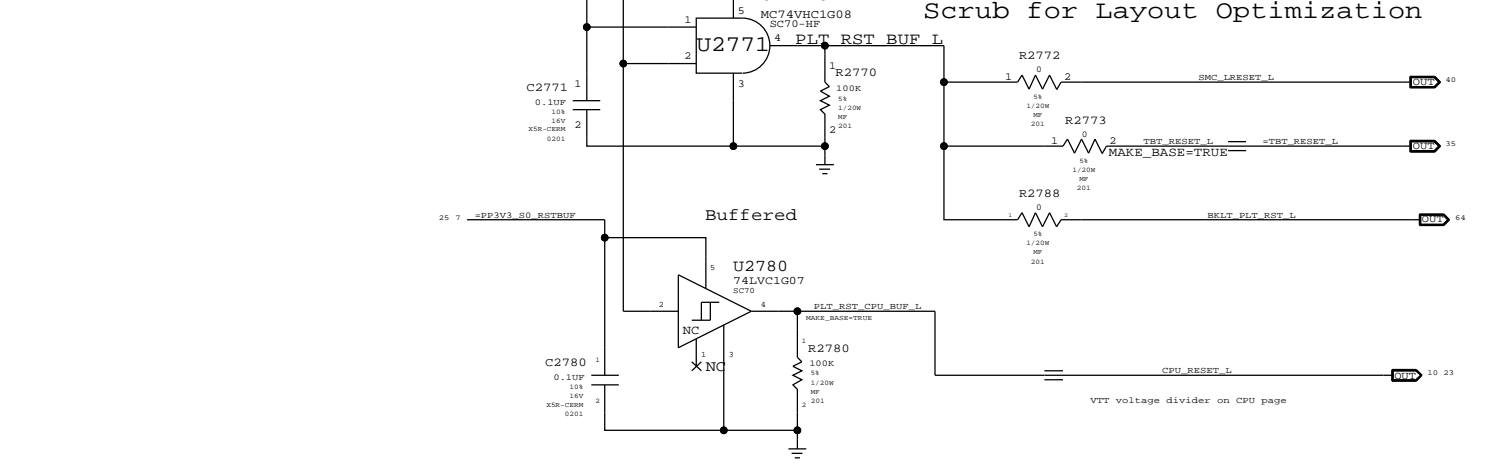
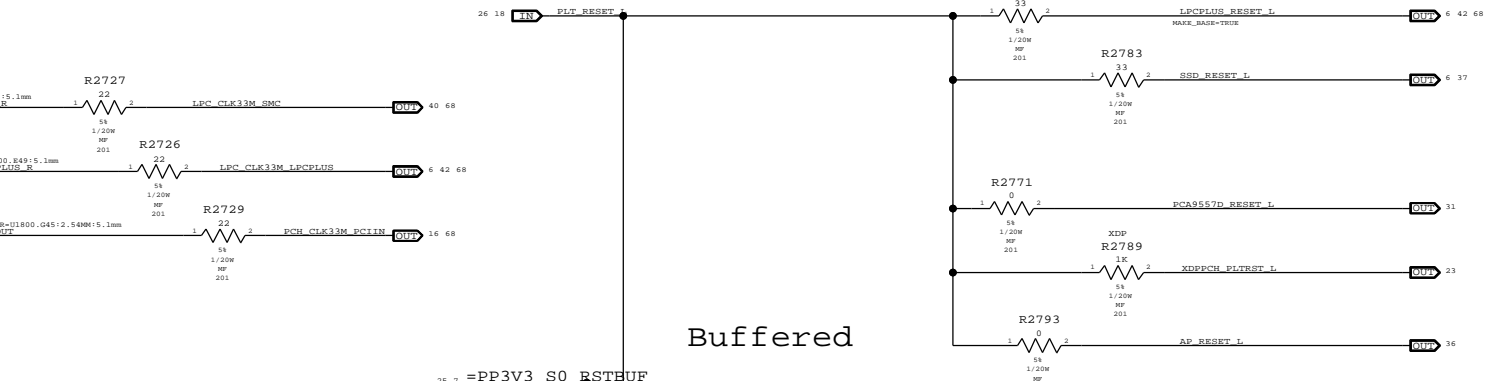
SYNC MASTER=J13 MLB		SYNC DATE=08/04/2011	
PAGE TITLE		CPU & PCH XDP	
Apple Inc.		DRAWING NUMBER	051-9276
		REVISION	2.7.0
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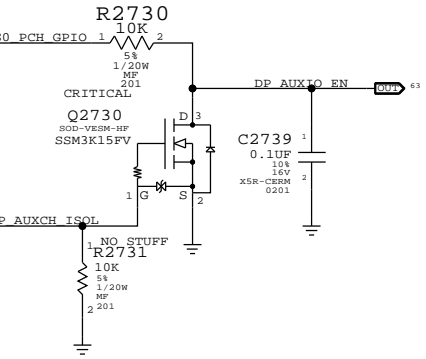
System RTC Power Source & 32kHz / 25MHz Clock Generator



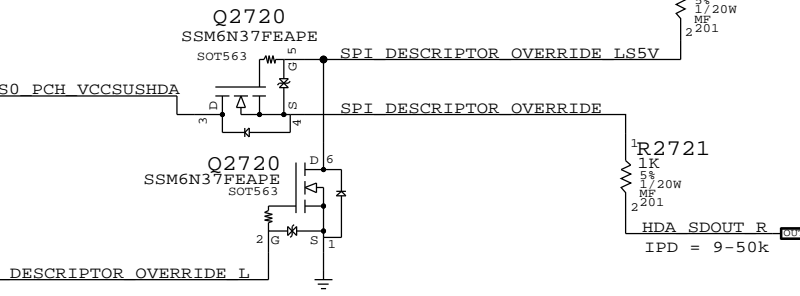
Platform Reset Connections  
Unbuffered



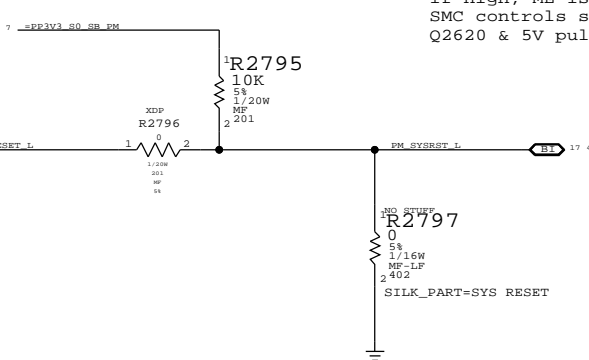
DP\_AUXIO\_EN Inversion




PCH ME Disable Strap



PCH Reset Button



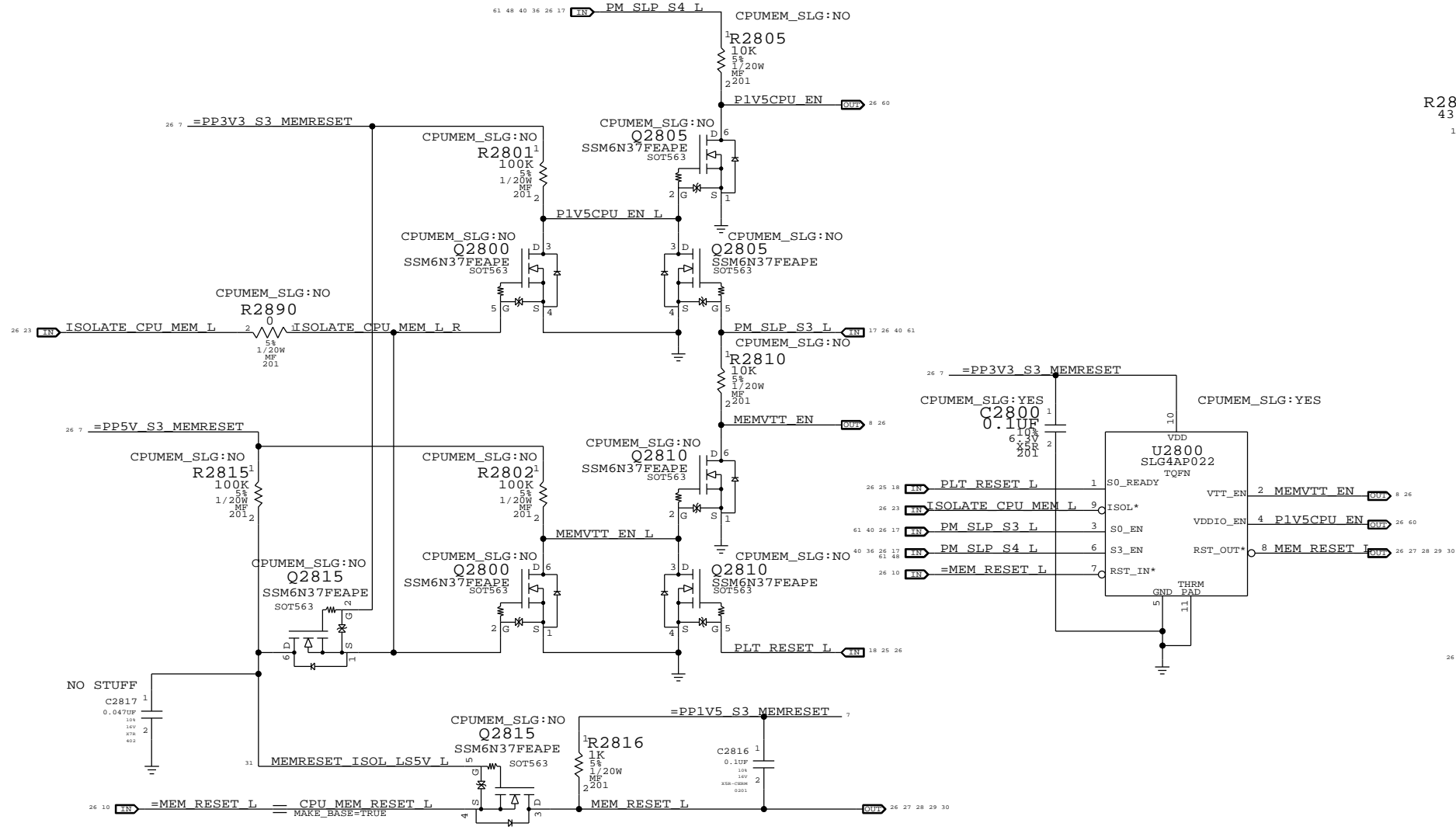
PCH uses HDA\_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q2620 & 5V pull-up allows circuit to work regardless of HDA voltage.

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PAGE TITLE		DRAWING NUMBER	
Clock (CK505) and Chipset Support		051-9276	
Apple Inc.		SIZE	
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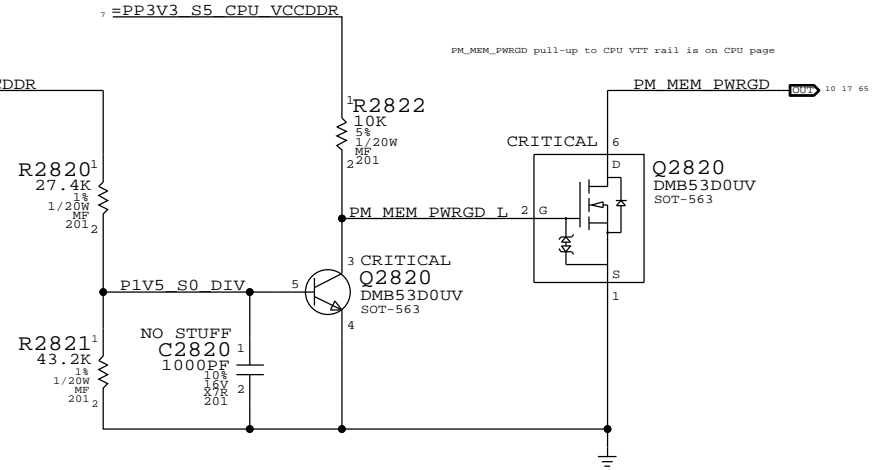
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM\_DRAMRST# output from the S0-DIMMs when necessary.

ISOLATE\_CPU\_MEM\_L GPIO state during S3->S0 transitions determines behavior of signals.  
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM\_RESET\_L not isolated.  
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM\_RESET\_L isolated.

P1V5CPU\_EN = (ISOLATE\_CPU\_MEM\_L + PM\_SLP\_S3\_L) \* PM\_SLP\_S4\_L  
MEMVTT\_EN = (ISOLATE\_CPU\_MEM\_L + PLT\_RST\_L) \* PM\_SLP\_S3\_L  
MEM\_RESET\_L = !ISOLATE\_CPU\_MEM\_L + CPU\_MEM\_RESET\_L

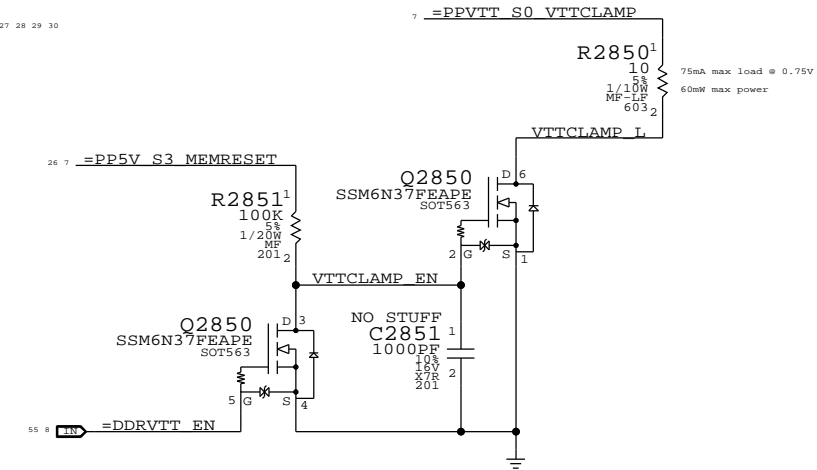


### 1V5 S0 "PGOOD" for CPU



### MEMVTT Clamp


Ensures CKE signals are held low in S3

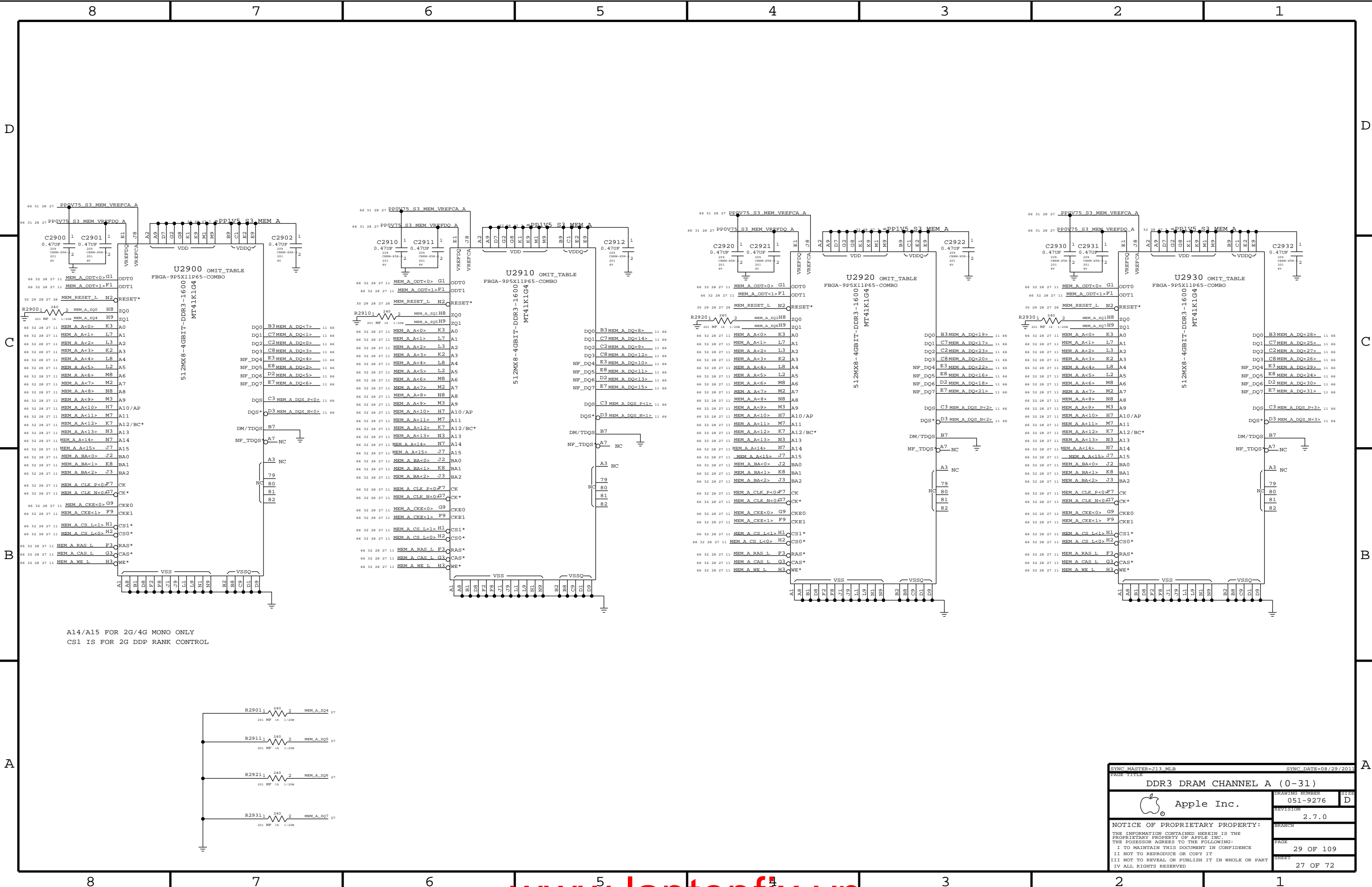


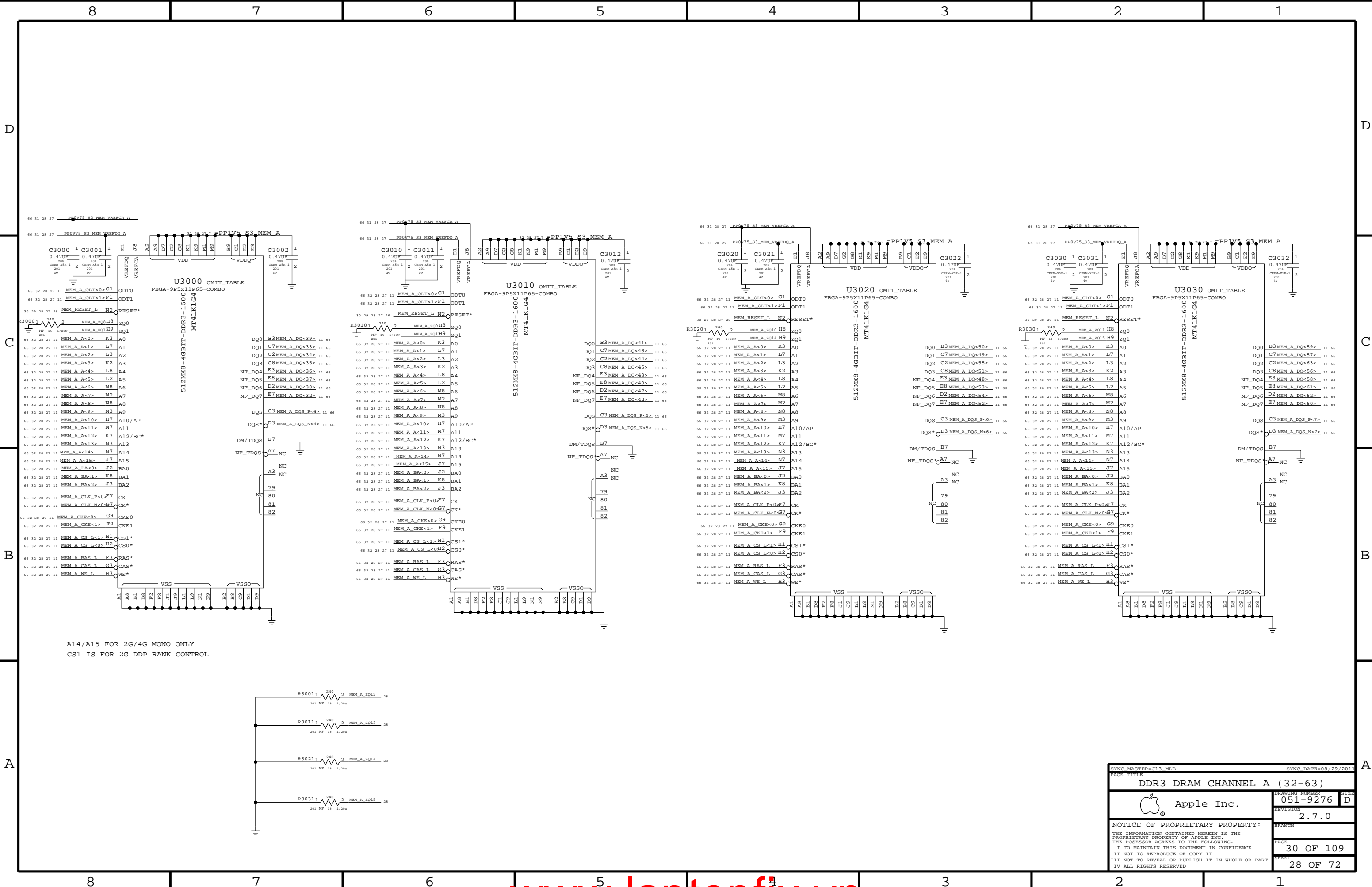
Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
1	0	1	1	1	1	1	1	1
2	0	0	0	1	1	0	0	1
3	0	0	0	1	X	0	0	0
S3	4	0	0	1	X	0	0	1
5	0	1	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	CPU_MEM_RESET_L	1	1

(\*) CPU\_MEM\_RESET\_L asserts due to loss of PM\_MEM\_PWRGD, must wait for software to clear before deasserting ISOLATE\_CPU\_MEM\_L GPIO.

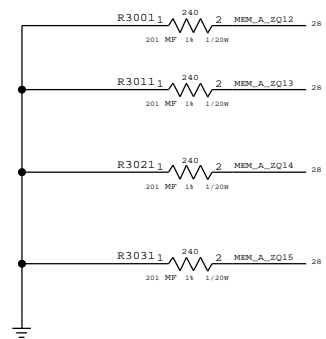
NOTE: In the event of a S3->S5 transition ISOLATE\_CPU\_MEM\_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM\_RESET\_L will not properly assert. Software must deassert ISOLATE\_CPU\_MEM\_L and then generate a valid reset cycle on CPU\_MEM\_RESET\_L.


BPMC MASTER-113 MLE		BPMC DATE-11/18/2013	
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CPU Memory S3 Support			
 Apple Inc.		DRAWING NUMBER	051-9276
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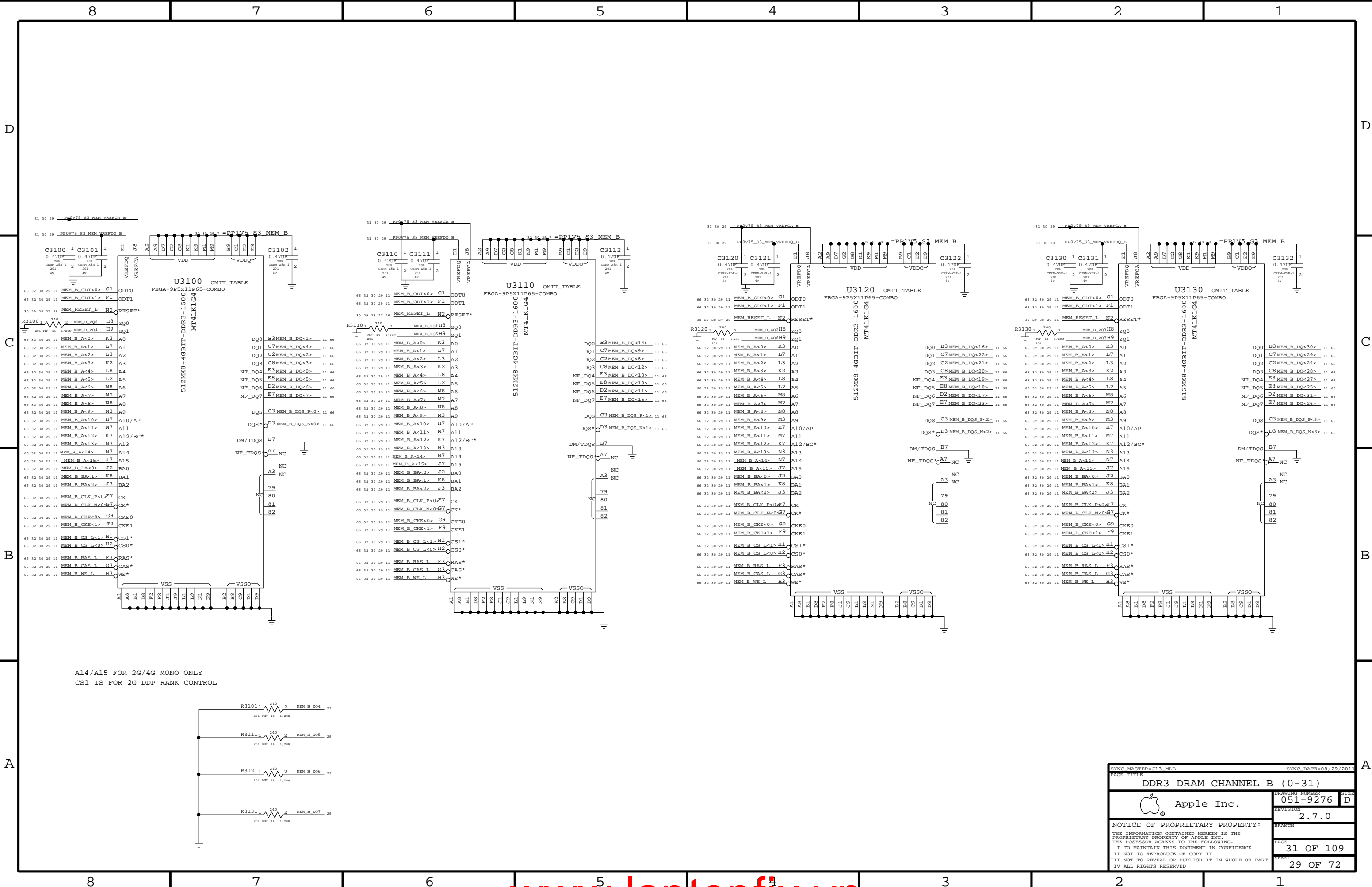




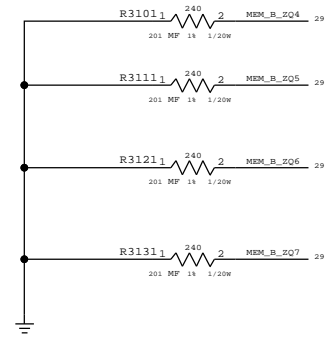
A14/A15 FOR 2G/4G MONO ONLY  
CS1 IS FOR 2G DDP RANK CONTROL




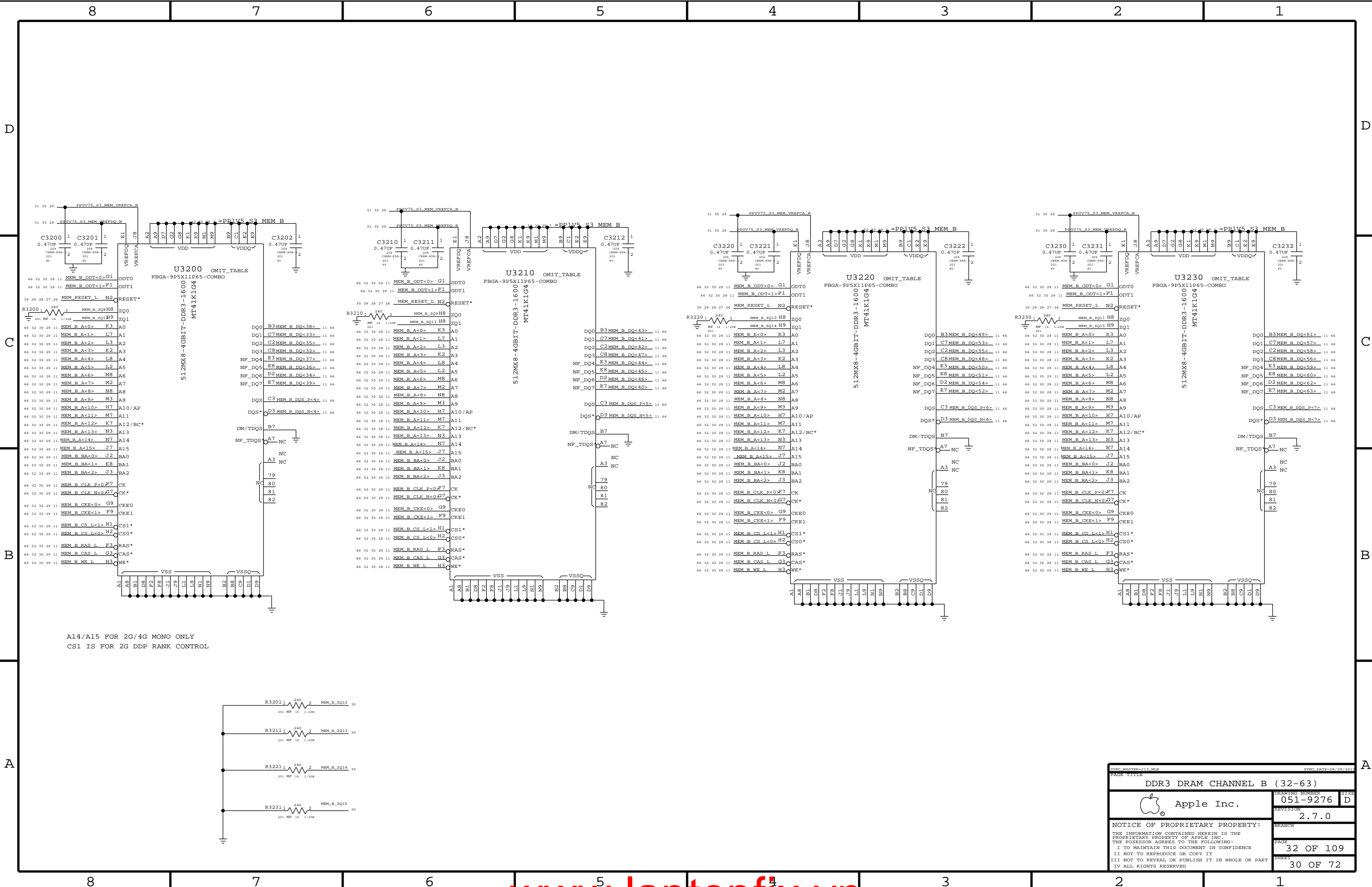
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DDR3 DRAM CHANNEL A (32-63)			
 Apple Inc.	DRAWING NUMBER	051-9276	SIZE D
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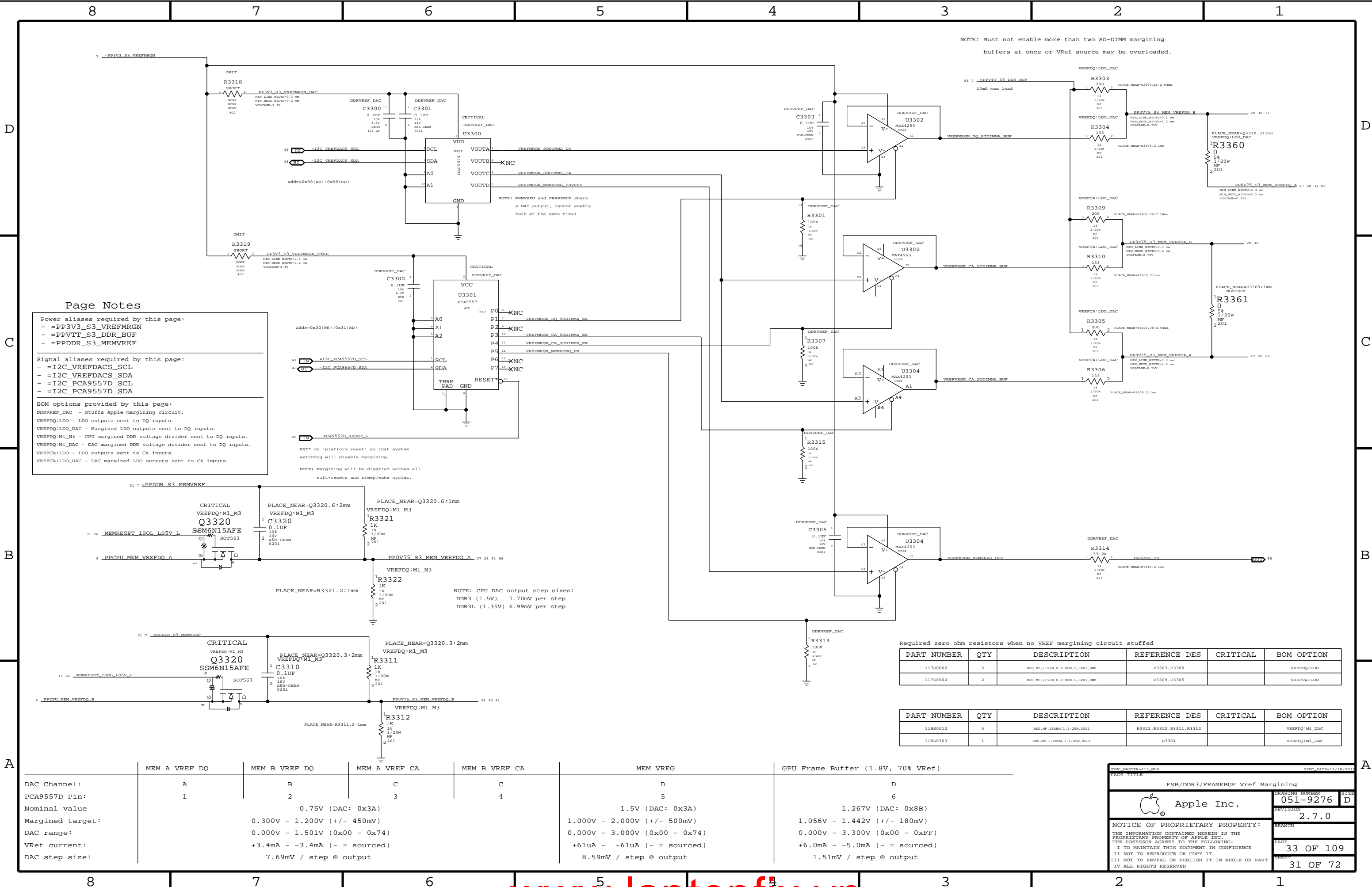


A14/A15 FOR 2G/4G MONO ONLY  
CS1 IS FOR 2G DDP RANK CONTROL



SYNC MASTER=J13 MLB		SYNC DATE=08/29/2011	
PAGE TITLE			
DDR3 DRAM CHANNEL B (0-31)			
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Page Notes

Power aliases required by this page:

- =PP3V3\_S3\_VREFMRGN
- =PPVTT\_S3\_DDR\_BUF
- =PPDDR\_S3\_MEMVREF

Signal aliases required by this page:

- =I2C\_VREFDACS\_SCL
- =I2C\_VREFDACS\_SDA
- =I2C\_PCA9557D\_SCL
- =I2C\_PCA9557D\_SDA

BOM options provided by this page:

- DDRREF\_DAC - Stuffs Apple margining circuit.
- VREFDQ:LDO - LDO outputs sent to DQ inputs.
- VREFDQ:LDO\_DAC - Margined LDO outputs sent to DQ inputs.
- VREFDQ:M1\_M3 - CPU margined DDR voltage divider sent to DQ inputs.
- VREFDQ:M1\_DAC - DAC margined DDR voltage divider sent to DQ inputs.
- VREFCA:LDO - LDO outputs sent to CA inputs.
- VREFCA:LDO\_DAC - DAC margined LDO outputs sent to CA inputs.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

NOTE: CPU DAC output step sizes:  
DDR3 (1.5V) 7.70mV per step  
DDR3L (1.35V) 6.99mV per step

Required zero ohm resistors when no Vref margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11780002	2	RES,MP,1/20W,0.0 OHM,5,0201,SMD	R3303,R3360		VREFDQ:LDO
11780002	2	RES,MP,1/20W,0.0 OHM,5,0201,SMD	R3309,R3305		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11880012	4	RES,MP,1KOHM,1,1/20W,0201	R3321,R3322,R3311,R3312		VREFDQ:M1_DAC
11880303	1	RES,MP,3320OHM,1,1/20W,0201	R3304		VREFDQ:M1_DAC

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% Vref)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0xFF)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYMC PARTSHEET:113 WEB SYMC DATE:11/18/2011

PAGE TITLE

FSB/DDR3/FRAMEBUF Vref Margining

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D

REVISION 2.7.0

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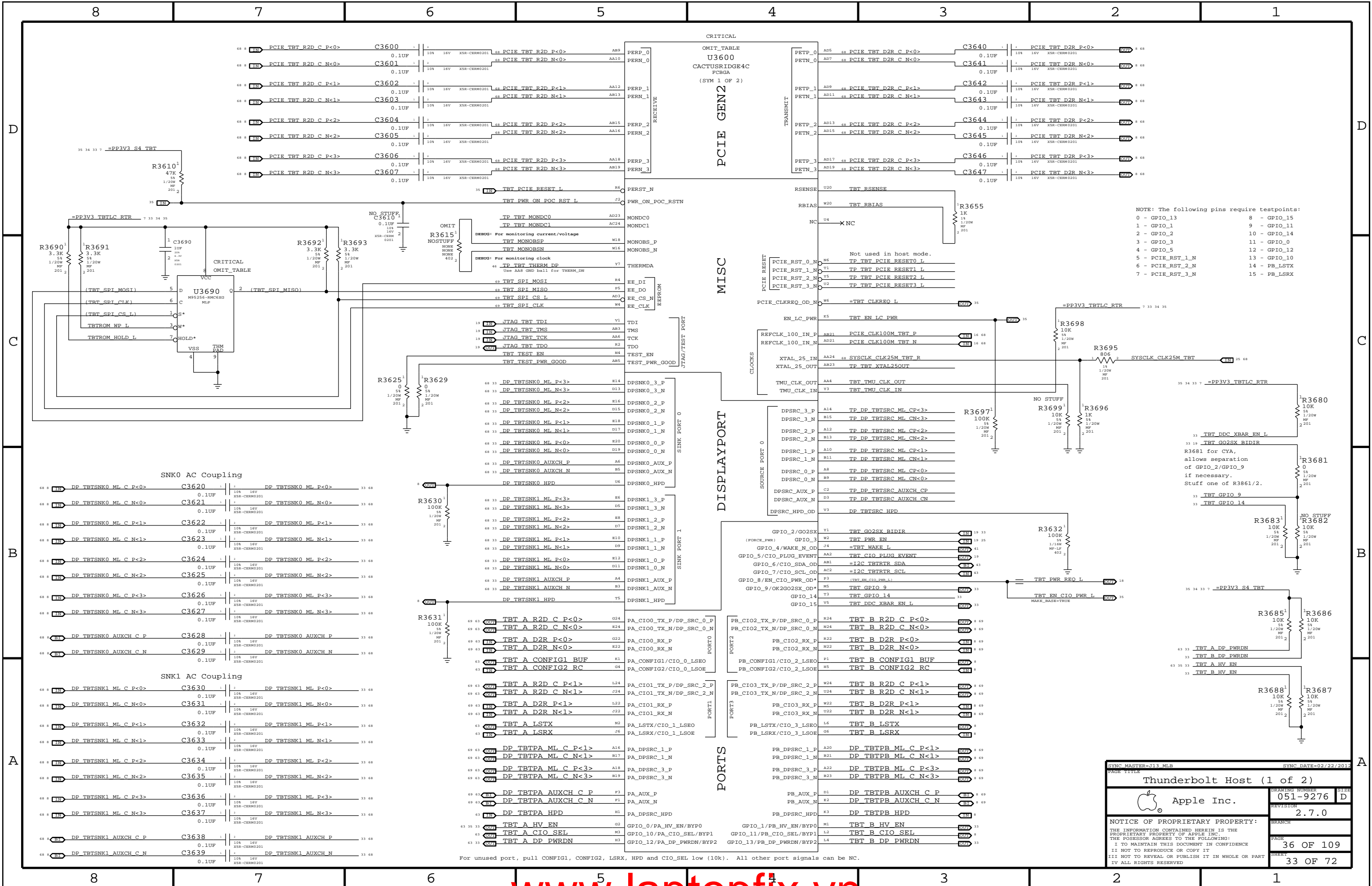
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SYNC MASTER=J13 MLB

SYNC DATE=03/22/2012

Thunderbolt Host (1 of 2)

 Apple Inc.

DRAWING NUMBER  
051-9276

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33 OF 72

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For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO\_SEL low (10k). All other port signals can be NC.



Power aliases required by this page:

- =PVPIN\_SW\_TBTBST (8-13V Boost Input)
- =PP18V\_TBT\_REG (18V Boost Output)
- =PP3V3\_TBT\_P3V3TBTFT (3.3V FET Input)
- =PP3V3\_TBT\_FET (3.3V FET Output)
- =PP3V3\_S0\_TBT\_PWRCTL
- =PPIV05\_TBT\_P1V05TBTFT (1.05V FET Input)
- =PPIV05\_TBT\_FET (1.05V FET Output)

---

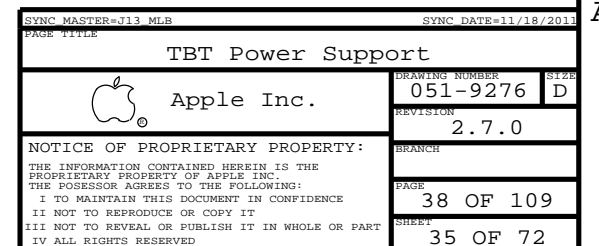
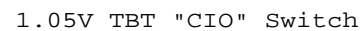
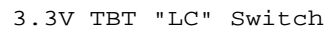
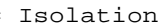
Signal aliases required by this page:

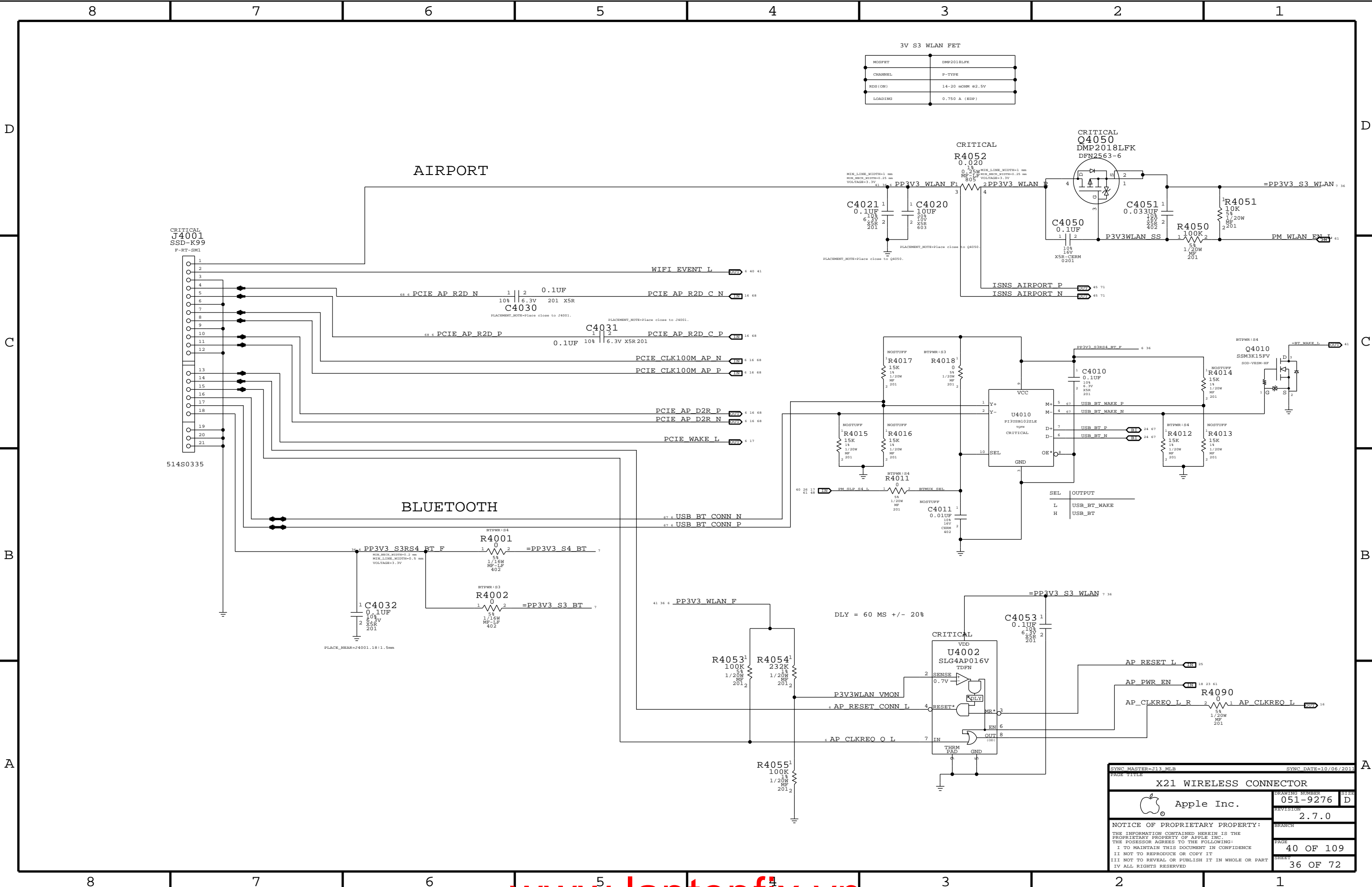
- =TBT\_CLKREQ\_L
- =TBT\_RESET\_L

---

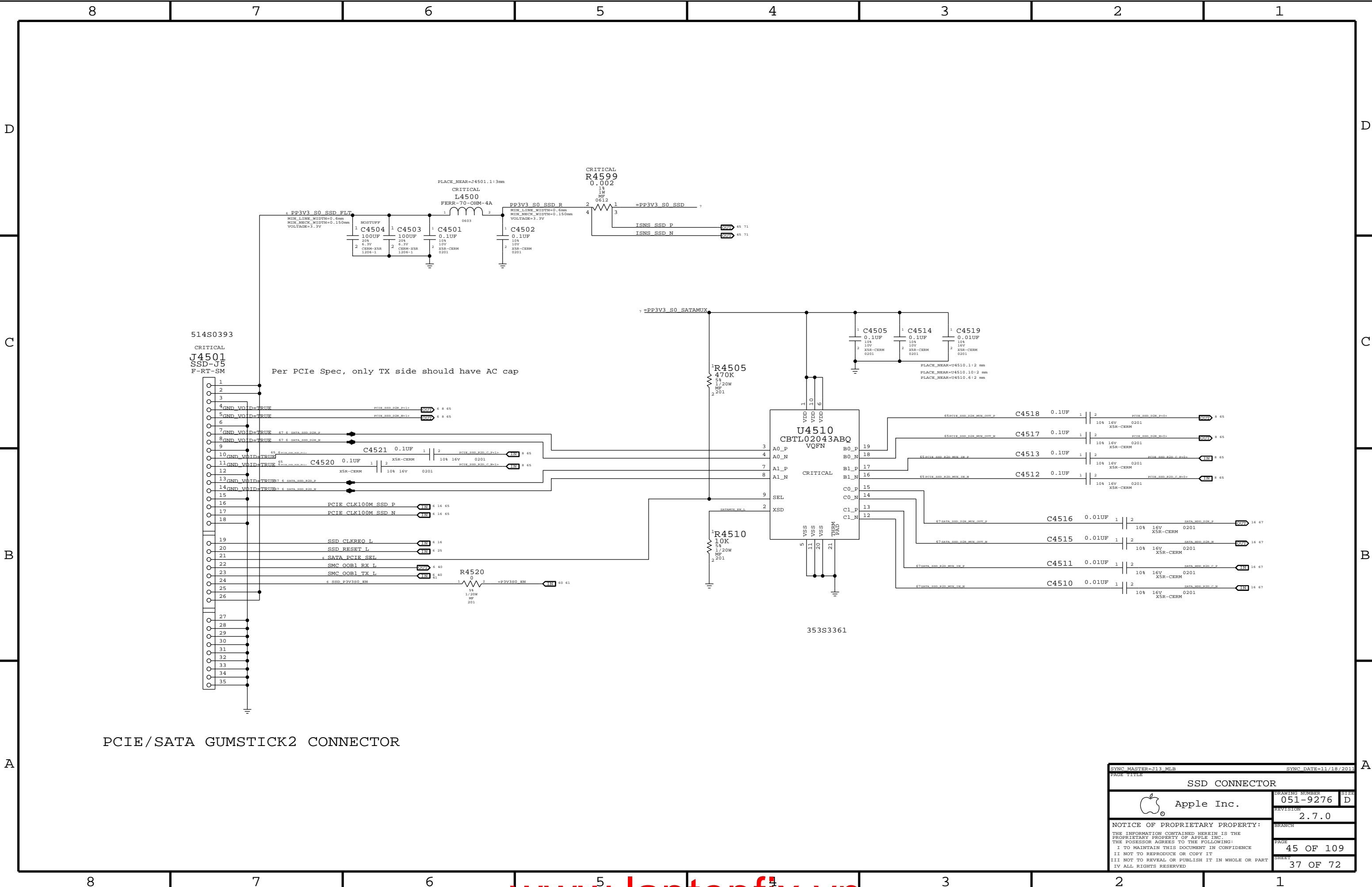
BOM options provided by this page:

TBTBST:Y - Stuffs 18V boost circuitry.






SYNC MASTER=J13 MLB		SYNC DATE=10/06/2011	
PAGE TITLE		X21 WIRELESS CONNECTOR	
Apple Inc.		DRAWING NUMBER	051-9276
		REVISION	2.7.0
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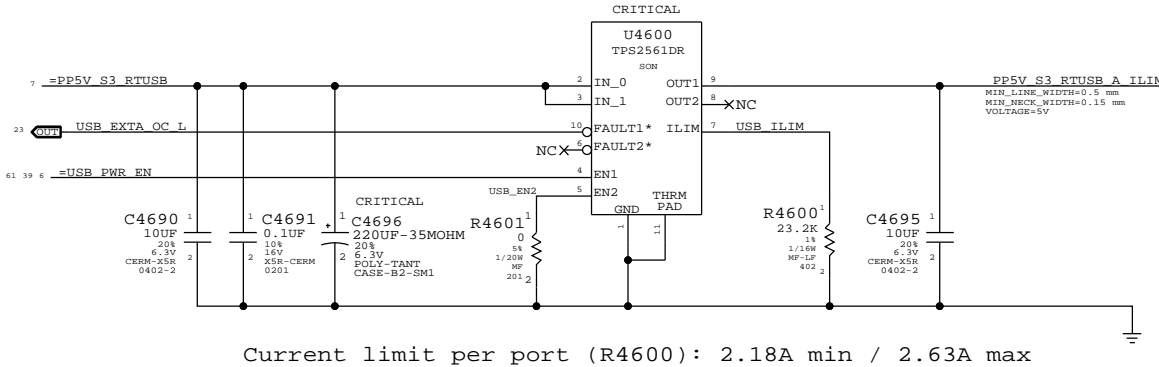


PCIE/SATA GUMSTICK2 CONNECTOR

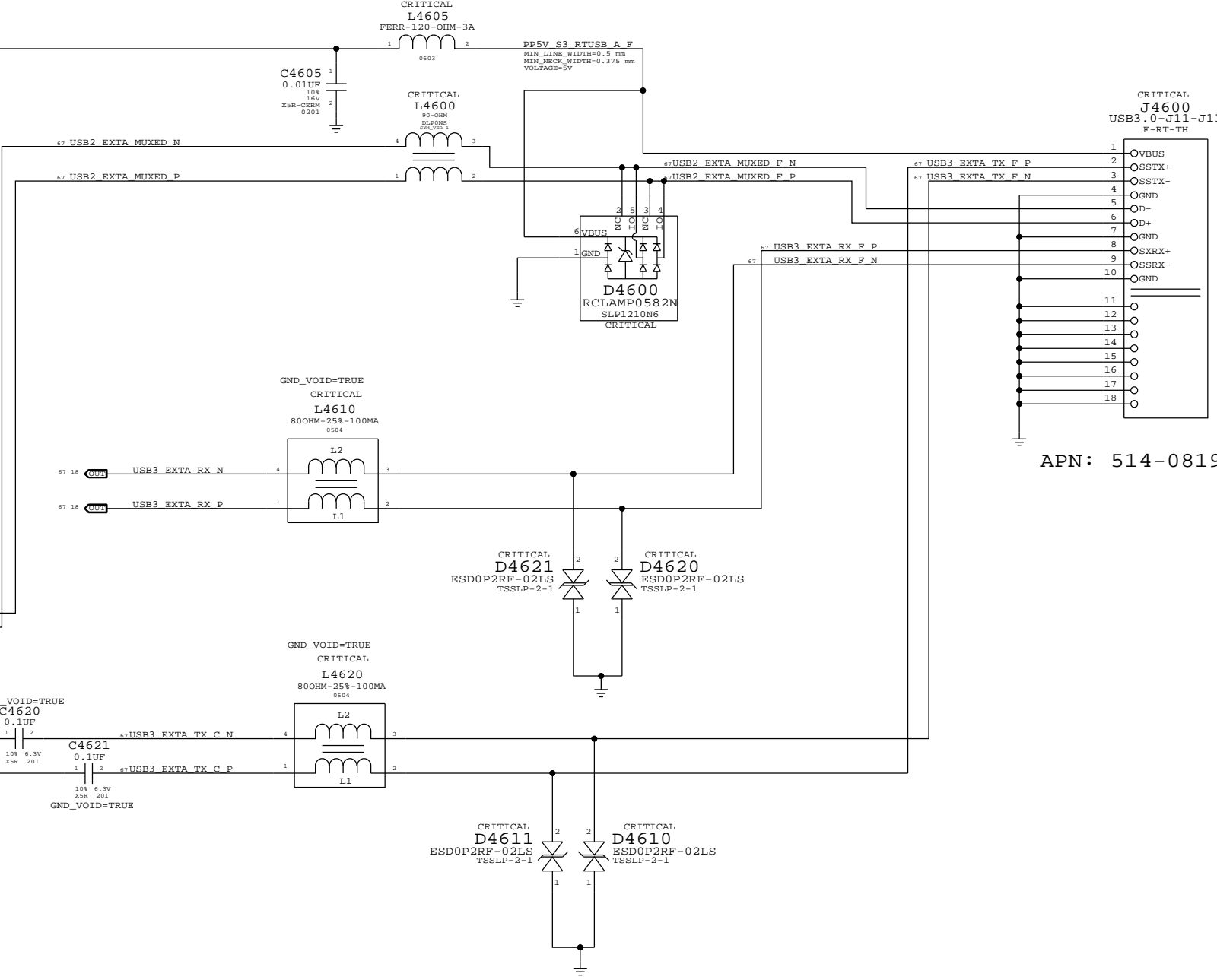
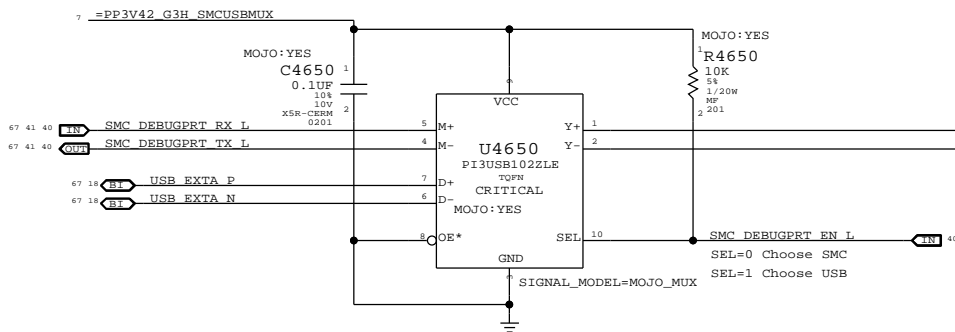
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SSD CONNECTOR			
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Right USB Port A


USB Port Power Switch

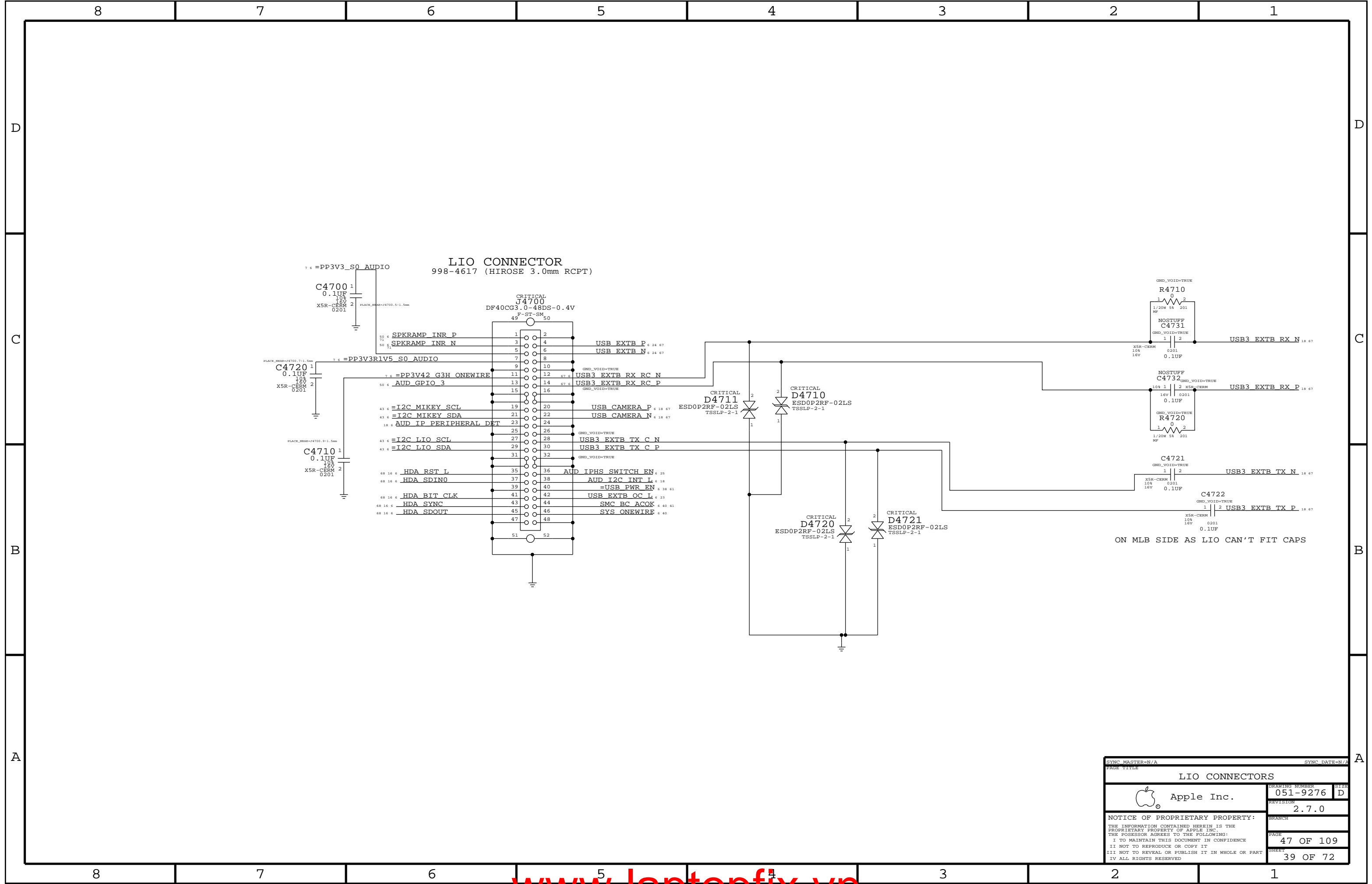



Mojo SMC Debug Mux

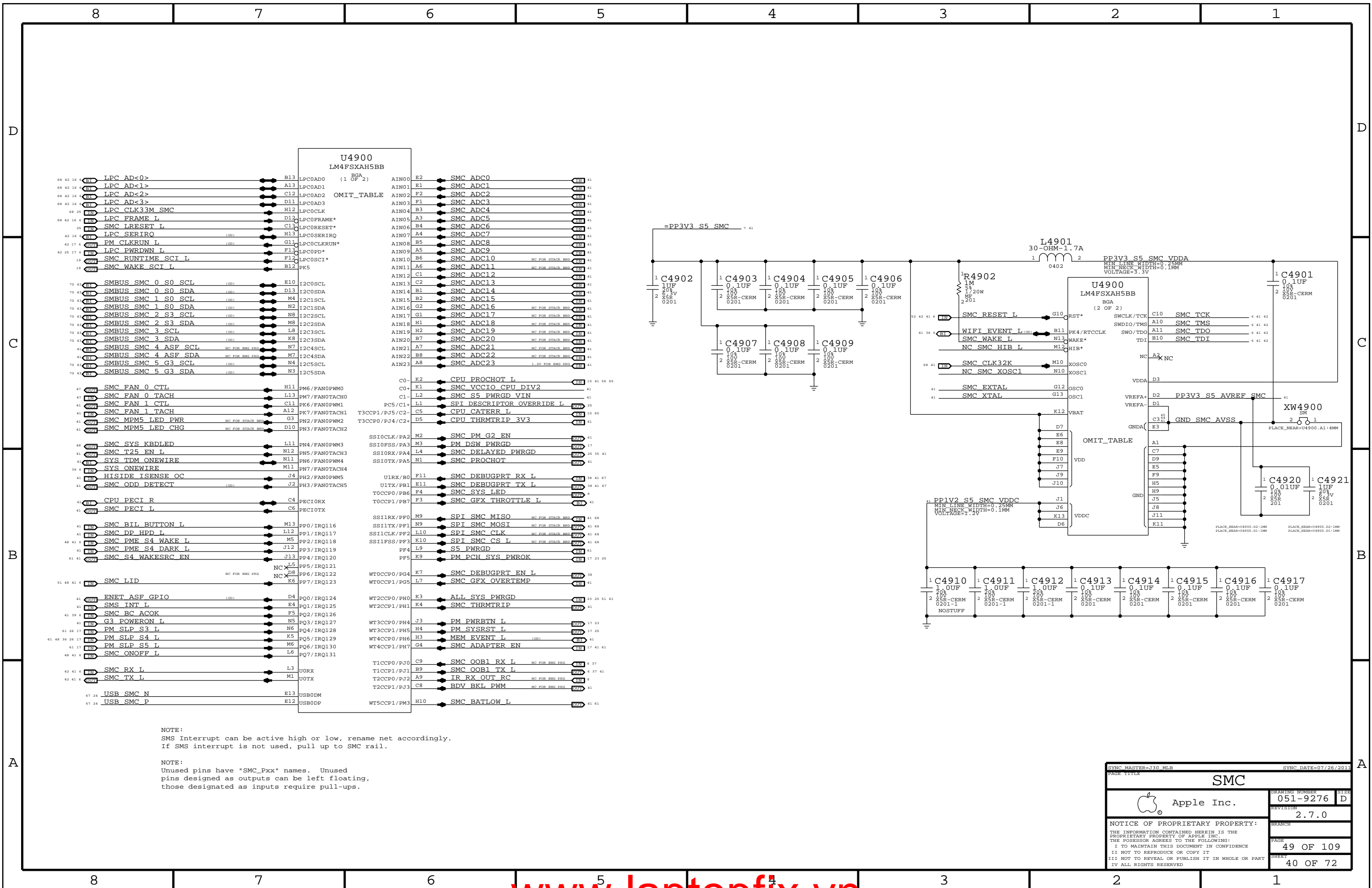


APN: 514-0819

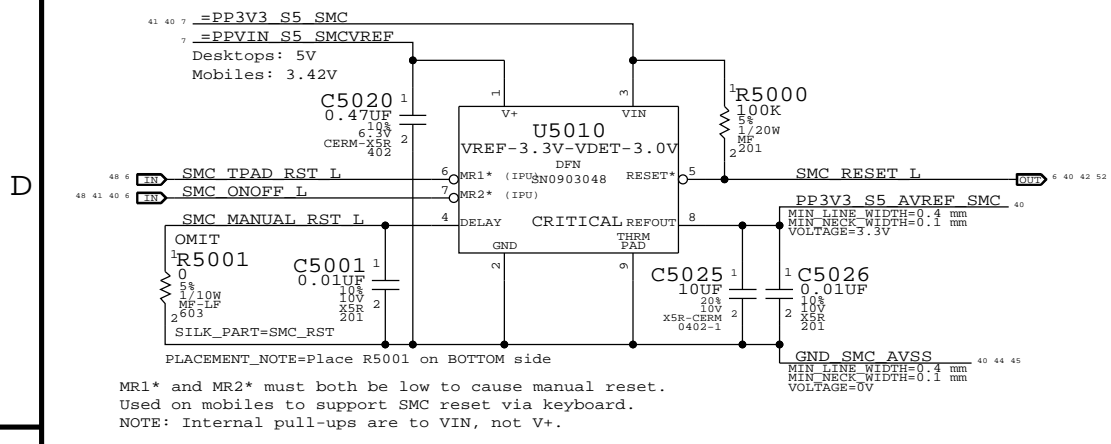
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PAGE TITLE			
External A USB3 Connector			
 Apple Inc.		DRAWING NUMBER	051-9276
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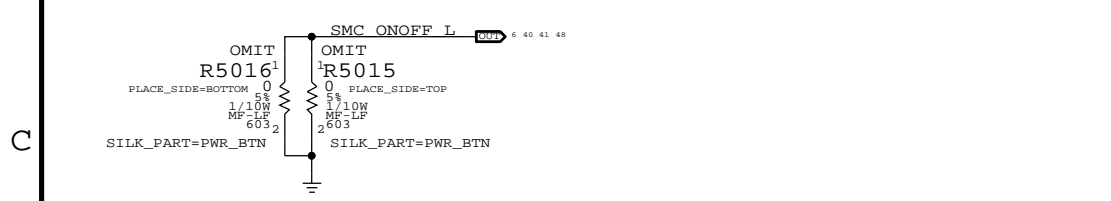
SYNC MASTER=N/A		SYNC DATE=N/A	
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LIO CONNECTORS			
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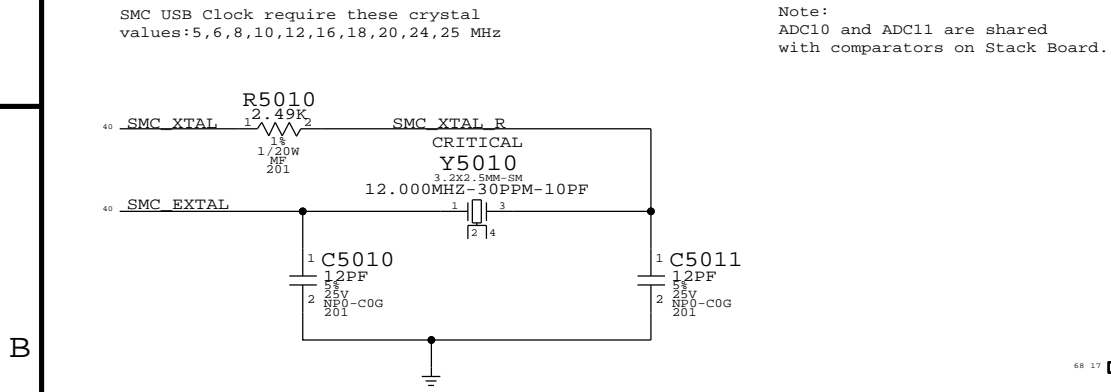
SMC Reset "Button", Supervisor & AVREF Supply



Debug Power "Buttons"

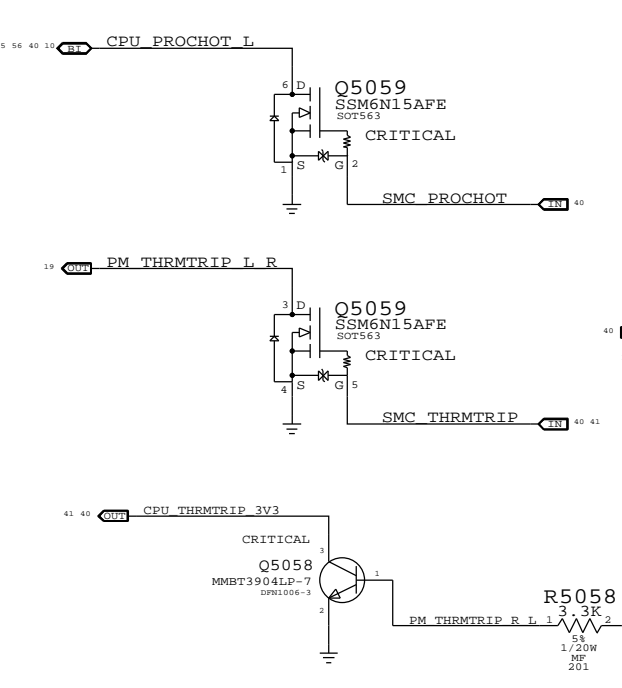


SMC Crystal Circuit

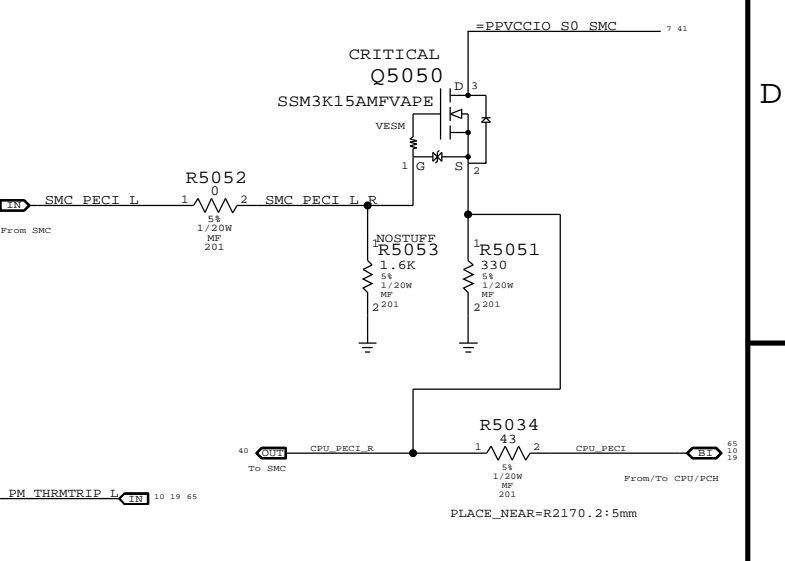


Note:  
ADC10 and ADC11 are shared  
with comparators on Stack Board.

SMC ADC0	= SMC CPU VSENSE
SMC ADC1	= SMC CPU ISENSE
SMC ADC2	= SMC VCCSA VSENSE
SMC ADC3	= SMC DCIN VSENSE
SMC ADC4	= SMC DCIN ISENSE
SMC ADC5	= SMC PBUS VSENSE
SMC ADC6	= SMC HDD ISENSE
SMC ADC7	= SMC BMON ISENSE
SMC ADC8	= SMC HS COMPUTING ISENSE
SMC ADC9	= SMC OTHER HI ISENSE
SMC ADC10	= SMC 1V5S3 ISENSE
SMC ADC11	= SMC CPUVCCIO ISENSE
SMC ADC12	= SMC GFX VSENSE
SMC ADC13	= SMC CPU SA ISENSE
SMC ADC14	= SMC 3V3S0 ISENSE
SMC ADC15	= SMC WLAN ISENSE
SMC ADC16	= SMC LCDBKLT ISENSE
SMC ADC17	= NC SMC ADC17
SMC ADC18	= SMC GFX ISENSE
SMC ADC19	= NC SMC ADC19
SMC ADC20	= NC SMC ADC20
SMC ADC21	= NC SMC ADC21
SMC ADC22	= NC SMC ADC22
SMC ADC23	= SMC ADC23
SMC GFX OVERTEMP	= NC SMC GFX OVERTEMP
SMC GFX THROTTLE L	= NC SMC GFX THROTTLE L
SMC FAN 1 CTL	= NC SMC FAN 1 CTL
SMC FAN 1 TACH	= NC SMC FAN 1 TACH
ENET ASF GPIO	= NC ENET ASF GPIO
SMC MPM5 LED PWR	= NC SMC MPM5 LED PWR
SMC MPM5 LED CHG	= NC SMC MPM5 LED CHG
SYS TDM ONEWIRE	= NC SYS TDM ONEWIRE



SMC12 PECI Support

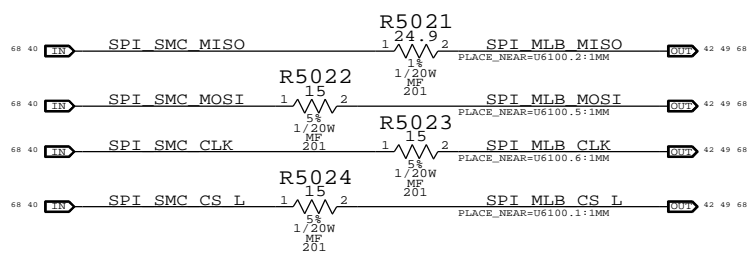


SMC12 Eng Pkg Support

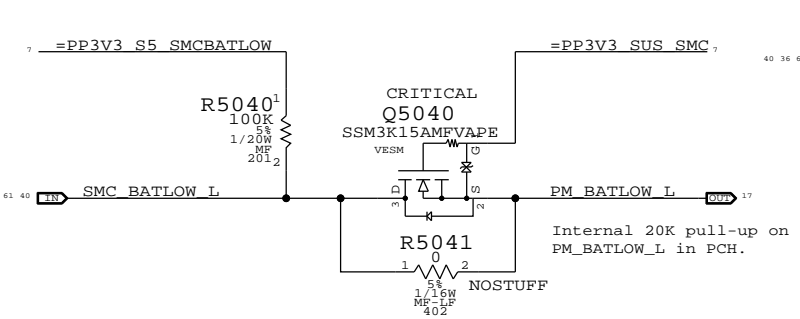
Eng Package requires 1.2V ON SMC\_ADC23 pin.

SMC12 SPI Support

Series resistors are no stuffed until the topology of 2 SPI Masters are verified.



BATLOW# Isolation



SMC ODD DETECT	R5066 33K	NO STUFF
SMC PME S4 DARK L	R5067 100K	5% 1/20W MF 201
SMC OOB1 TX L	R5068 100K	NO STUFF
SMC ONOFF L	R5070 10K	5% 1/20W MF 201
G3 POWERON L	R5072 10K	5% 1/20W MF 201
SMC LID	R5071 100K	5% 1/20W MF 201
SMC TX L	R5073 10K	5% 1/20W MF 201
SMC RX L	R5074 100K	5% 1/20W MF 201
SMC DEBUGPT TX L	R5075 10K	5% 1/20W MF 201
SMC DEBUGPT RX L	R5076 100K	5% 1/20W MF 201
SMC TMS	R5077 10K	5% 1/20W MF 201
SMC TDO	R5078 10K	5% 1/20W MF 201
SMC TDI	R5079 10K	5% 1/20W MF 201
SMC TCK	R5080 10K	5% 1/20W MF 201
SMC BIL BUTTON L	R5081 10K	5% 1/20W MF 201
SMC BC ACOK	R5087 100K	5% 1/20W MF 201
SMC S5 PWGRD VIN	R5092 100K	5% 1/20W MF 201
SMC INT L	R5093 10K	5% 1/20W MF 201
MEM EVENT L	R5014 10K	NO STUFF
CPU THRMTRIP 3V3	R5017 100K	5% 1/20W MF 201
SMC ROMBOOT	R5088	5% 1/20W MF 201
SMC ADAPTER EN	R5085 10K	5% 1/20W MF 201
SMC THRMTRIP	R5086 10K	5% 1/20W MF 201
SMC DELAYED PWGRD	R5091 100K	5% 1/20W MF 201
SMC S4 WAKESRC EN	R5090 100K	5% 1/20W MF 201
WIFI EVENT L	R5089 10K	5% 1/20W MF 201

SYNC MASTER=J13 MLB

SYNC DATE=10/06/2011

Apple Inc.

051-9276

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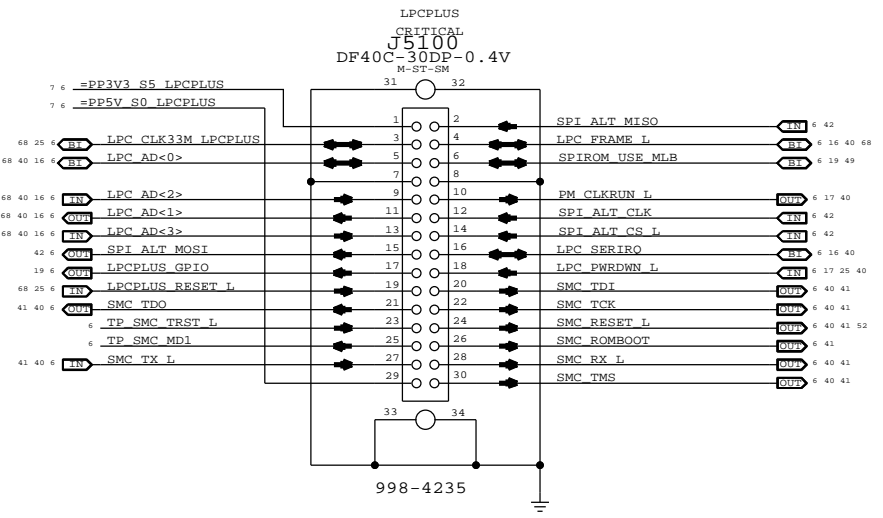
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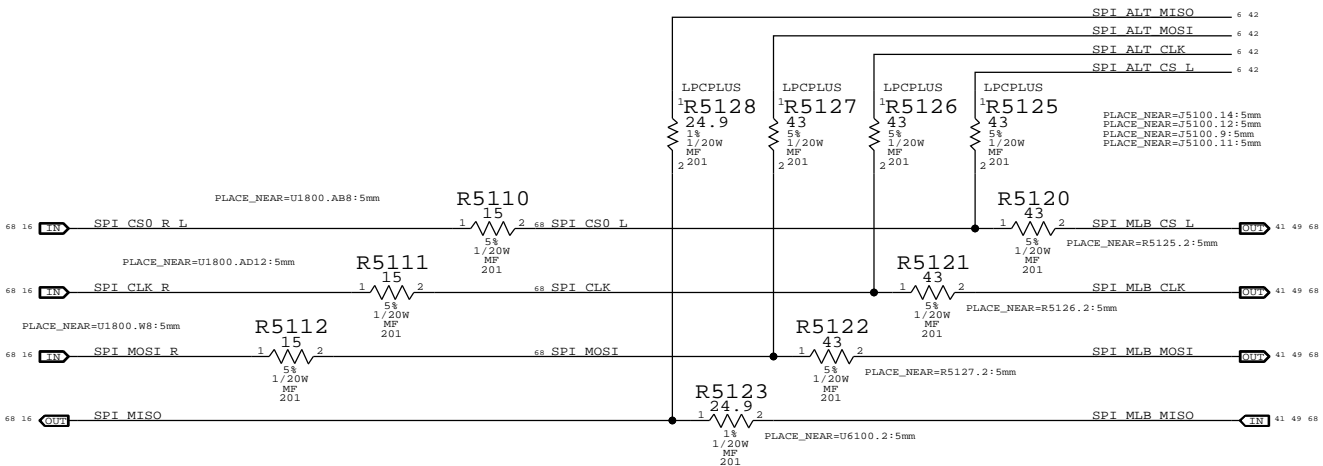
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LPC+SPI Connector




SPI Bus Series Termination



SYNC MASTER=K21 MLB

SYNC DATE=12/13/2010

LPC+SPI Debug Connector

 Apple Inc.

DRAWING NUMBER  
051-9276

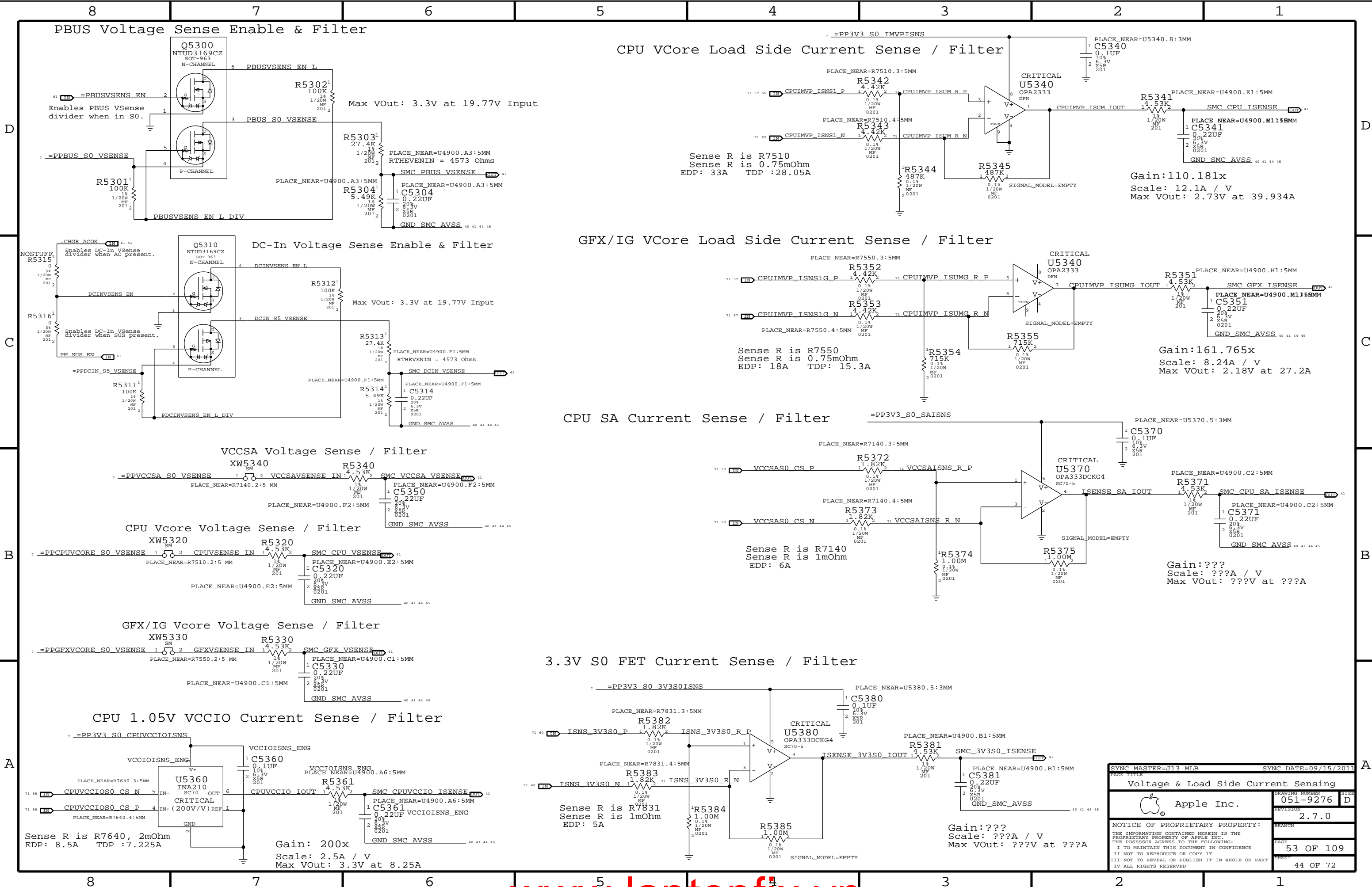
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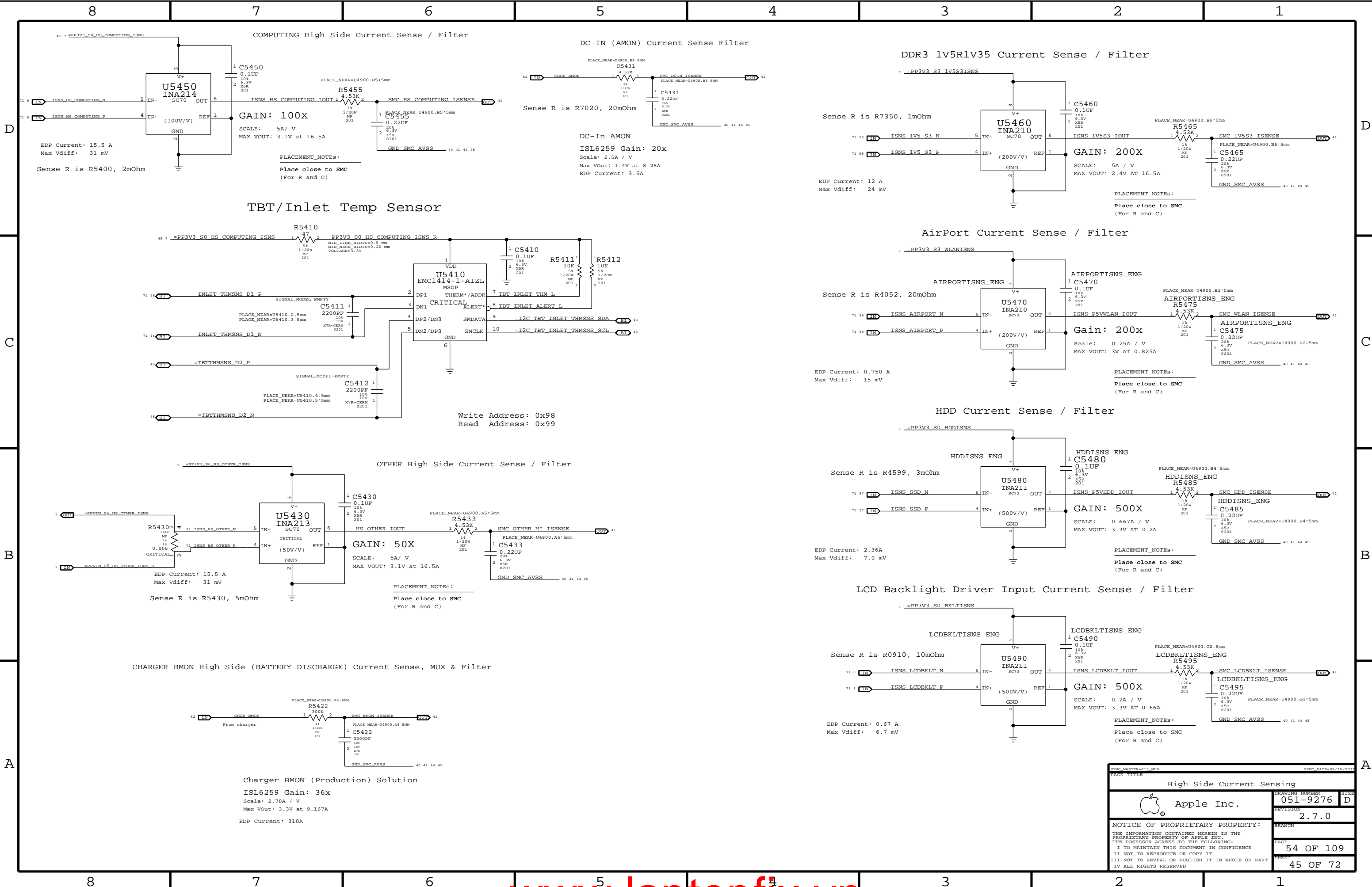
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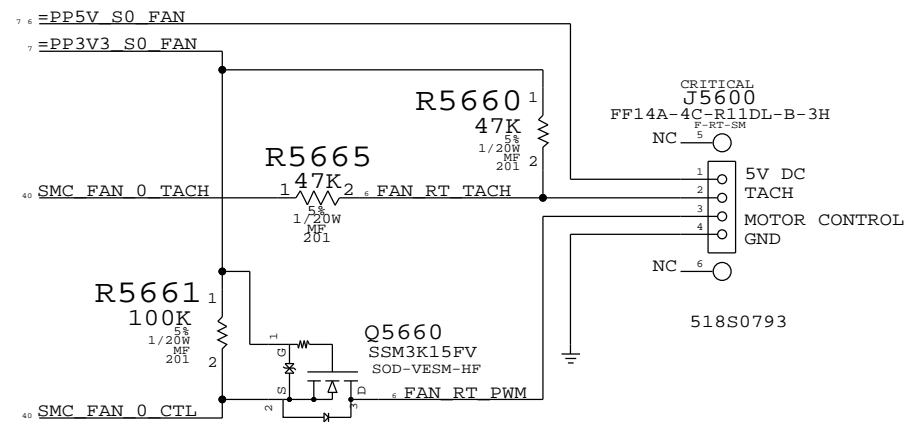





SYMC PARTS=113 MCB		SYMC DATE=09/16/2011	
PAGE TITLE			
High Side Current Sensing			
	Apple Inc.	DRAWING NUMBER	051-9276
		D	D
		REVISION	2.7.0
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FAN CONNECTOR



SYNC MASTER=K21_MLB		SYNC DATE=12/13/2010	
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Fan			
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		56 OF 109	
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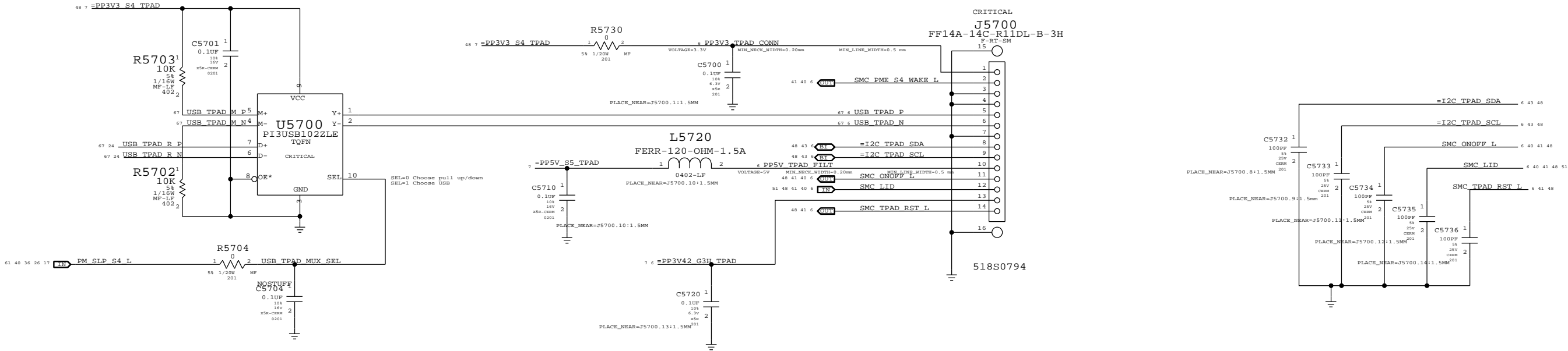
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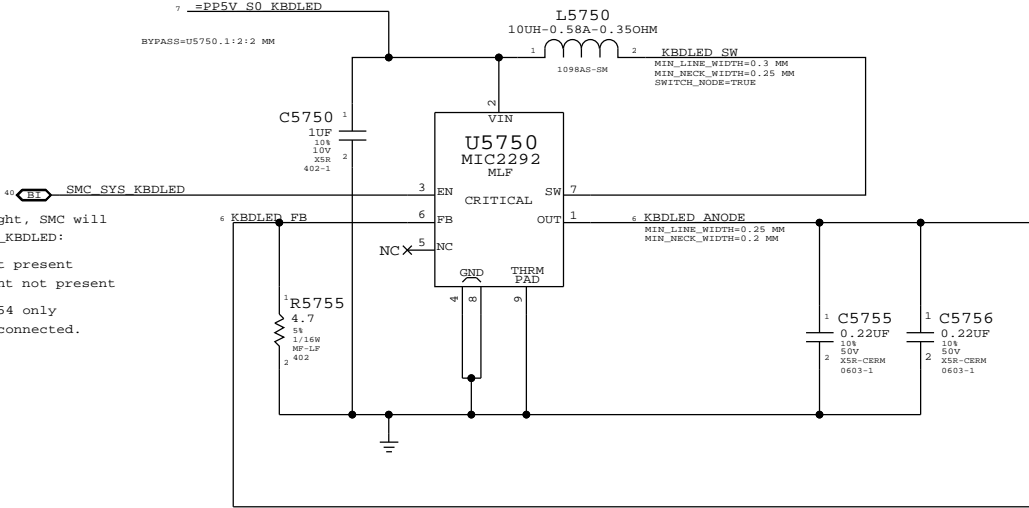
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IPD Flex Connector

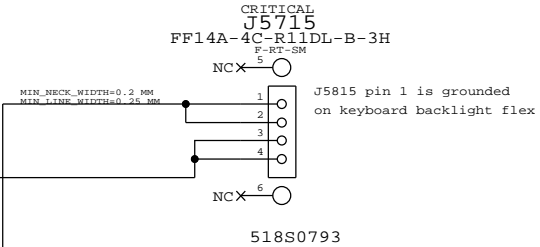



Keyboard Backlight Driver & Detection

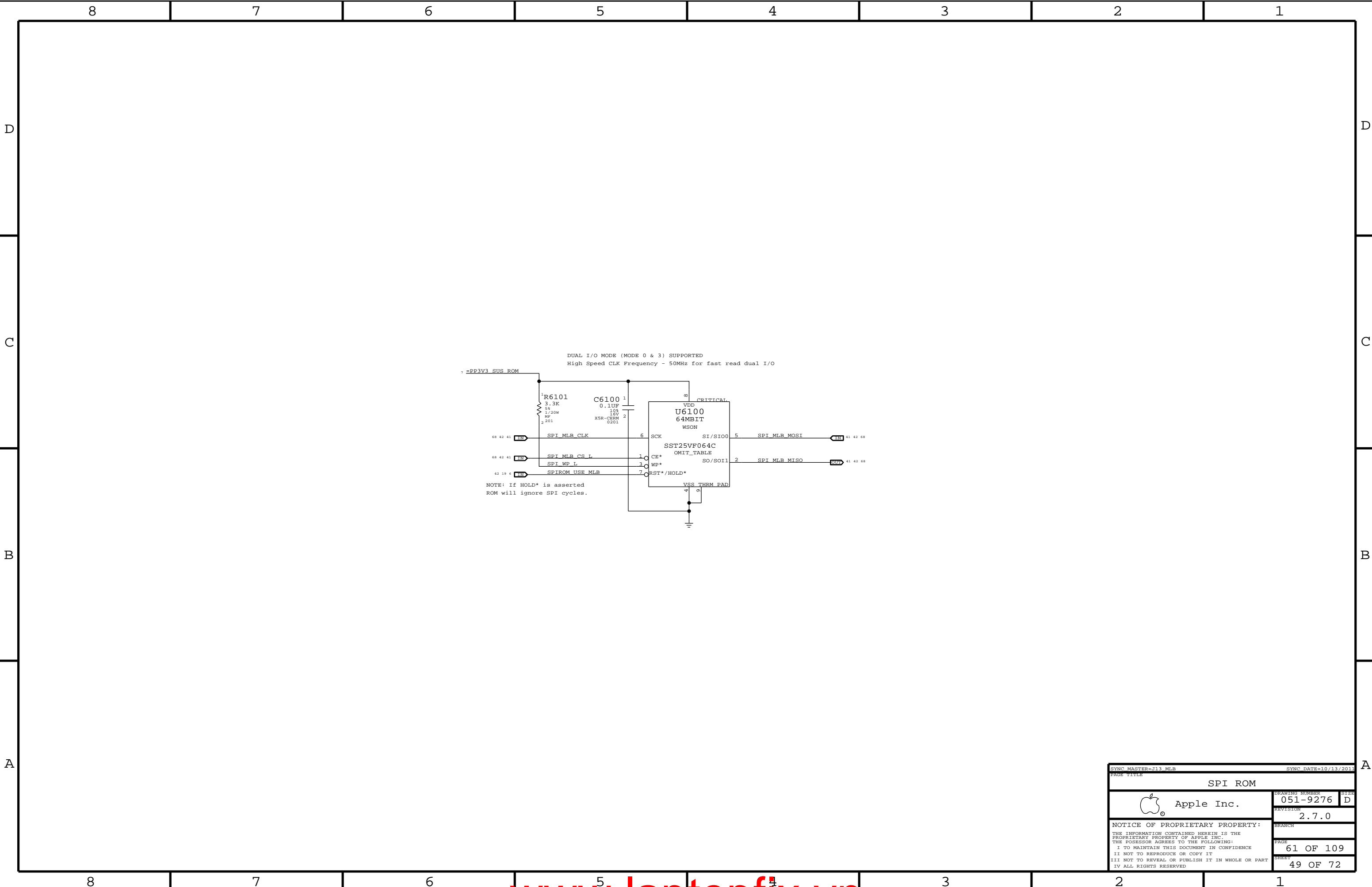
To detect Keyboard backlight, SMC will tristate and read SMC\_SYS\_KBDLED:  
If LOW, keyboard backlight present  
If HIGH, keyboard backlight not present  
R5853 always stuffed, R5854 only grounded when KB BL flex connected.




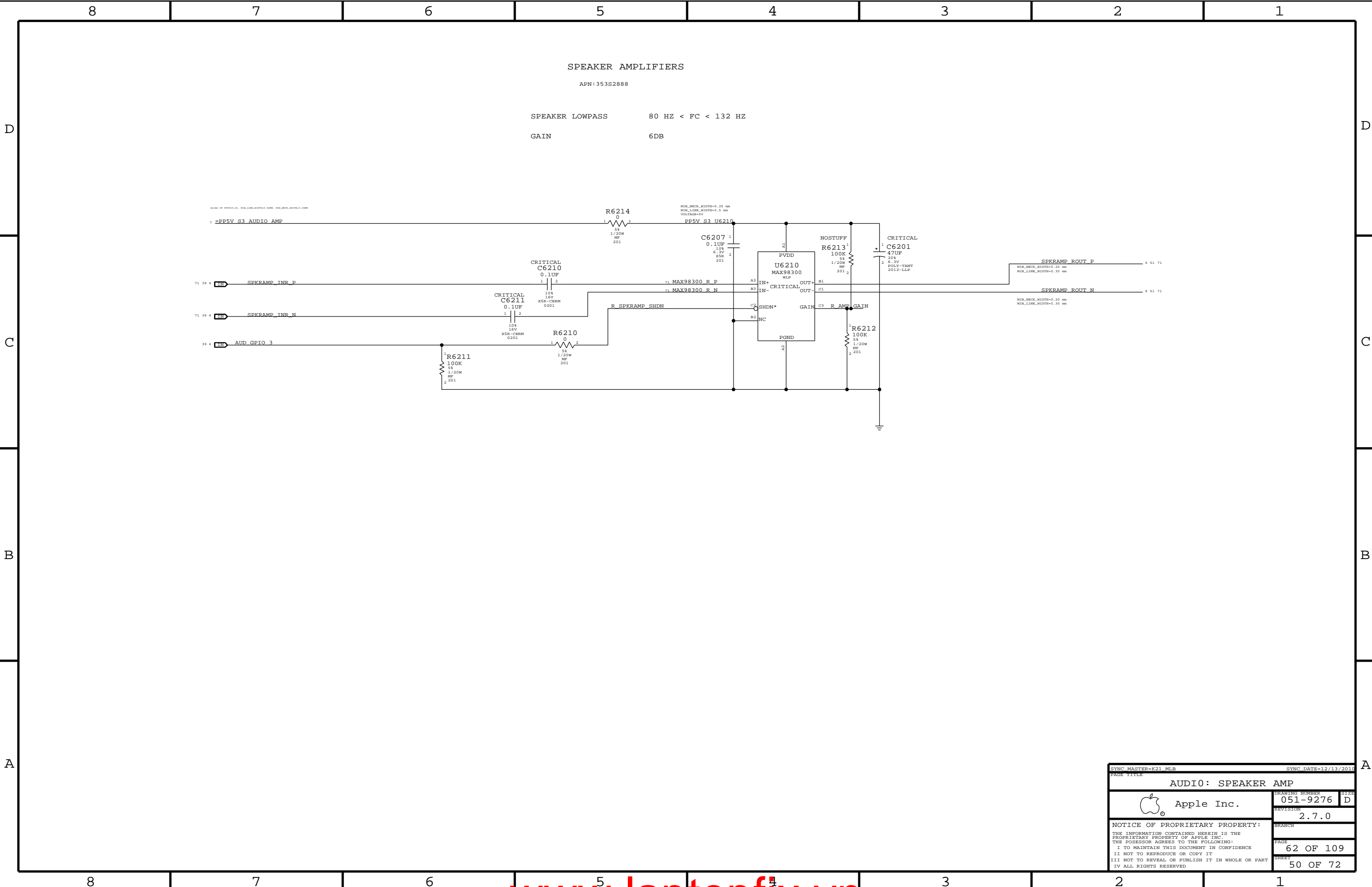
Keyboard Backlight Connector

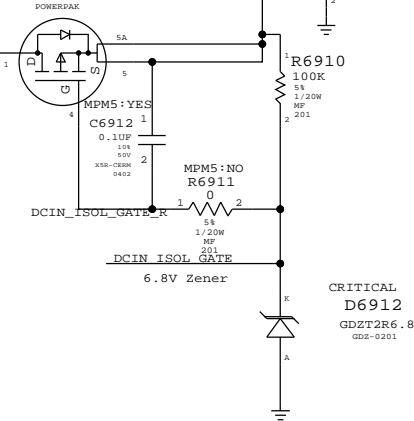
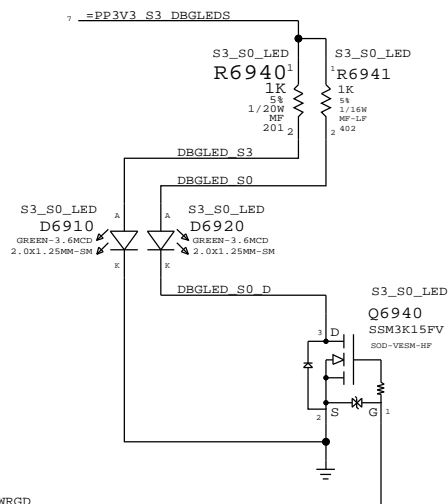
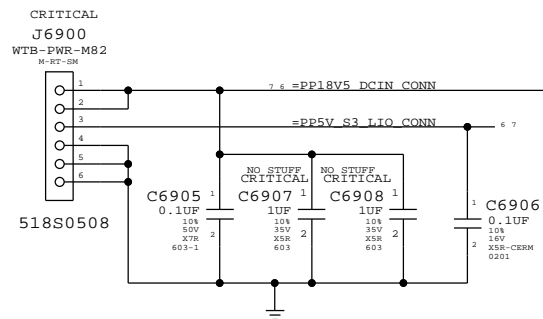
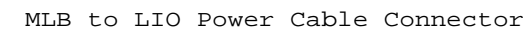


SYNC MASTER=K21 MLB		SYNC DATE=12/13/2010	
PAGE TITLE			
IPD / KBD Backlight			
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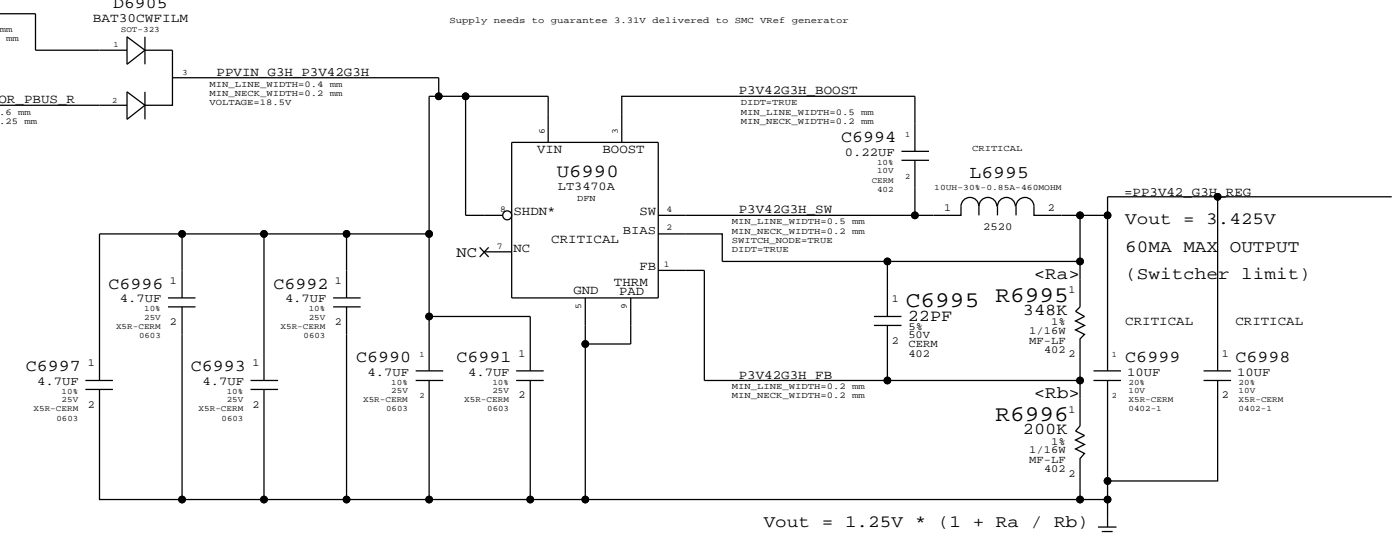
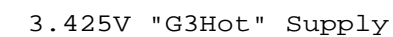
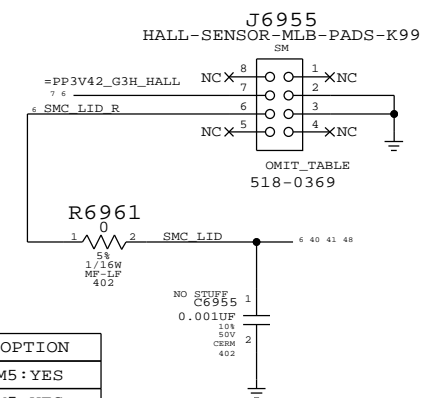


SYNC MASTER=J13_MLB		SYNC DATE=10/13/2011	
PAGE TITLE			
SPI ROM			
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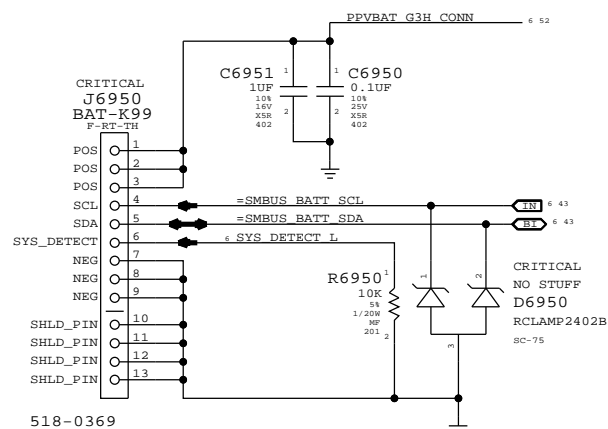




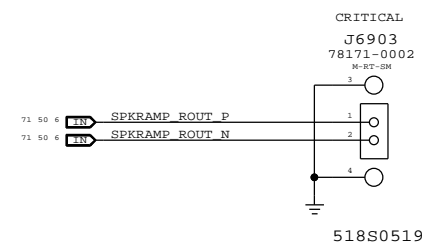
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0560	1	RES,MF,90.9KOHM,1,1/20W,0201	R6912	CRITICAL	MPM5: YES
117S0008	1	RES,MF,100KOHM,1,1/20W,0201	R6911	CRITICAL	MPM5: YES

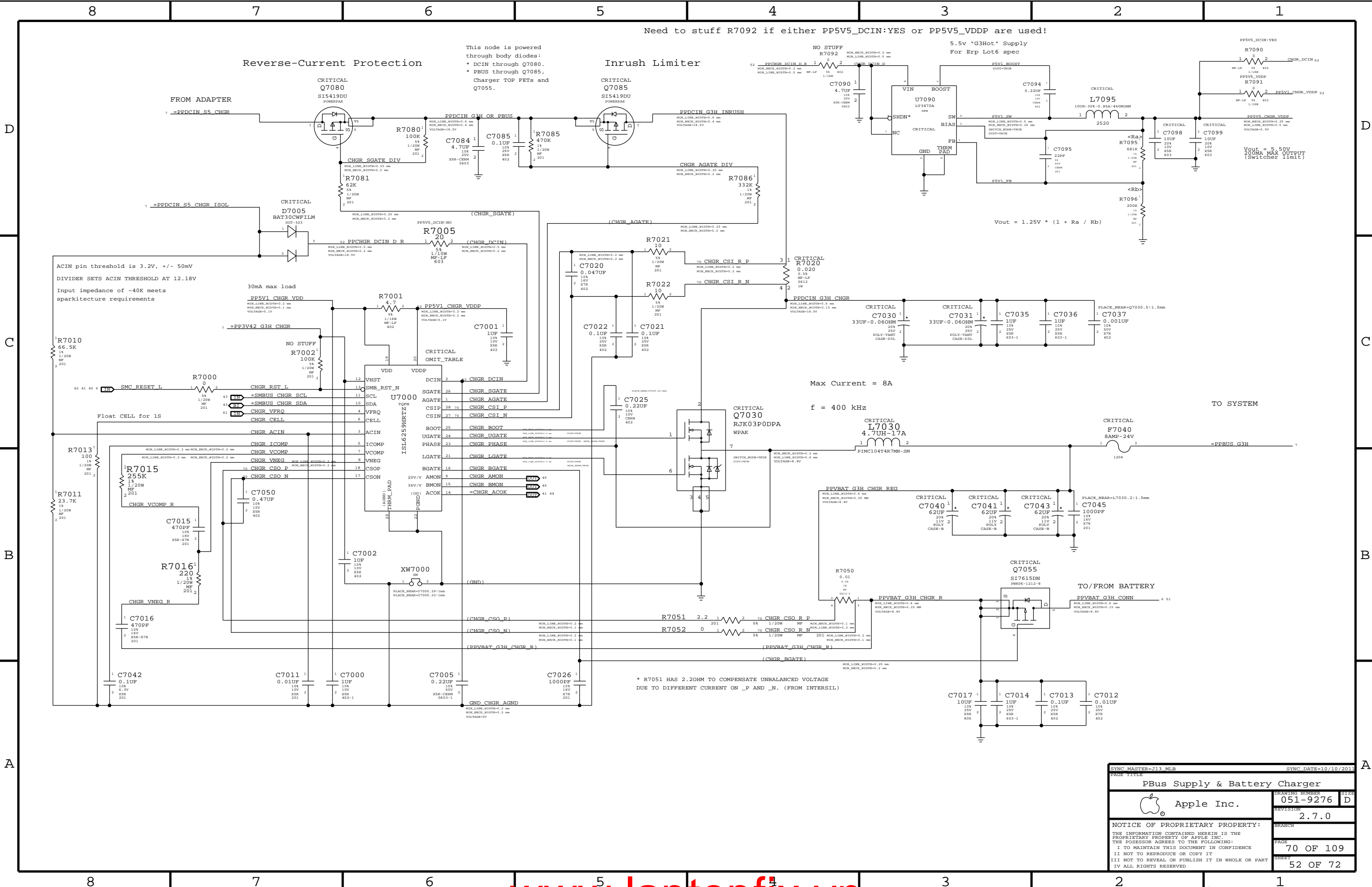



# K99-Specific Battery Connector



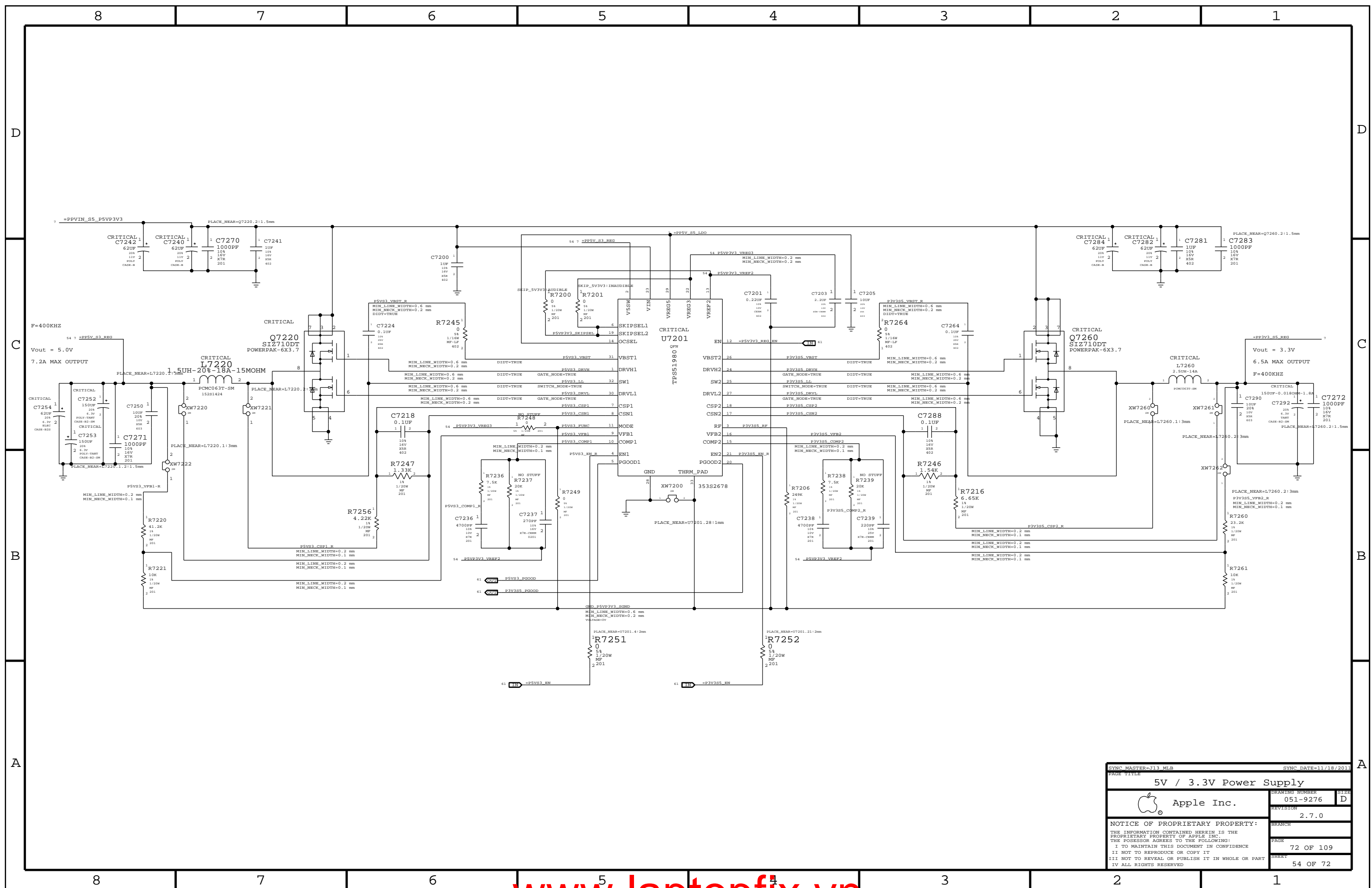
## Right Speaker Connector





SYNC MASTER=J13 MLB		SYNC DATE=10/10/2013	
PAGE TITLE			
PBus Supply & Battery Charger			
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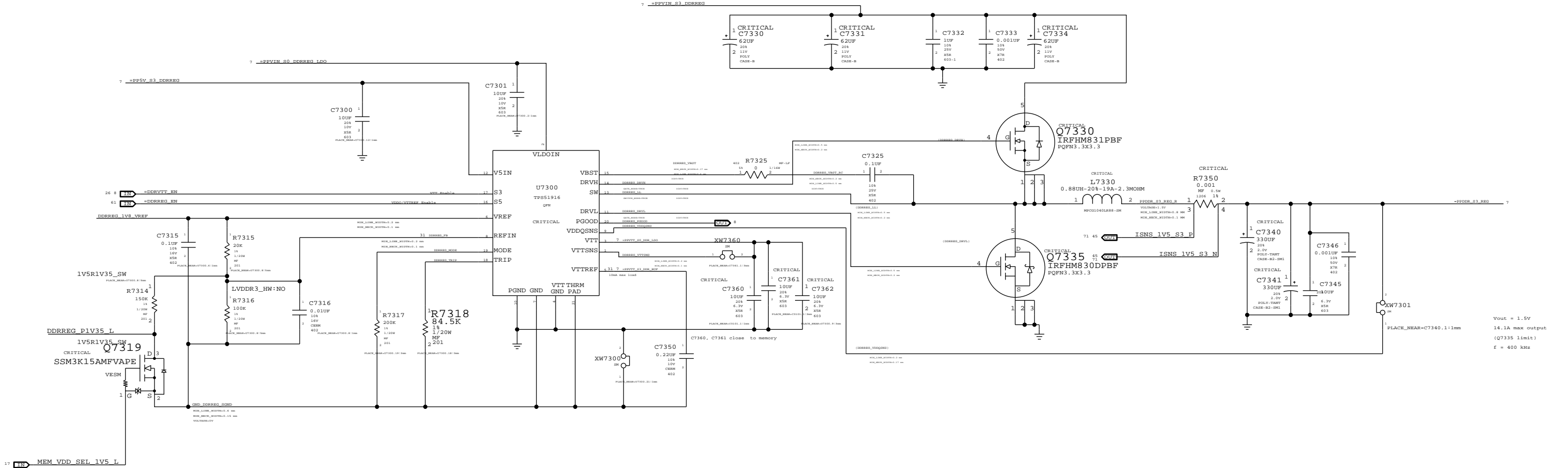
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A



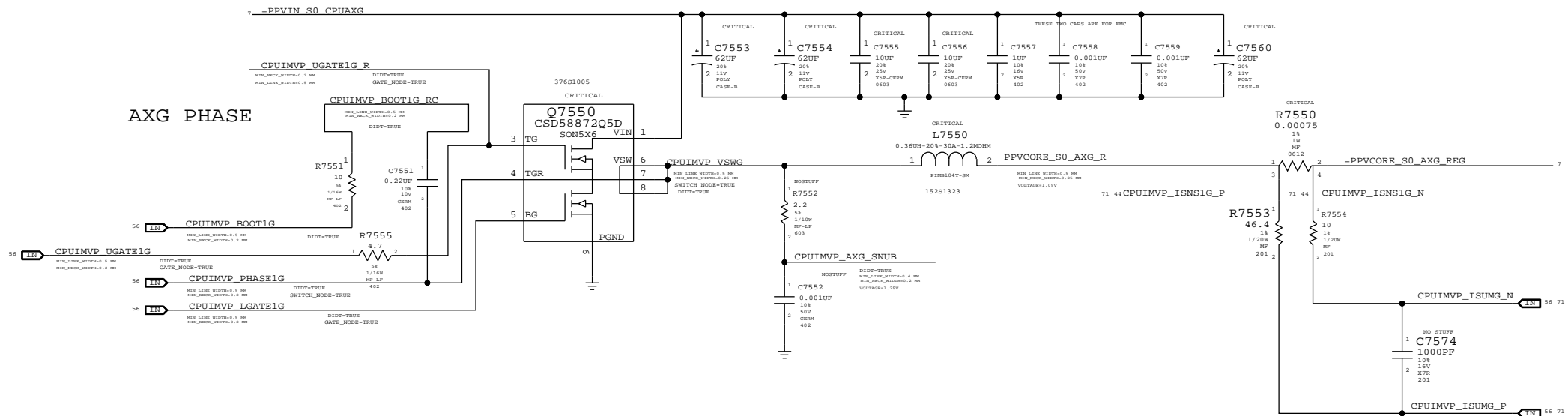
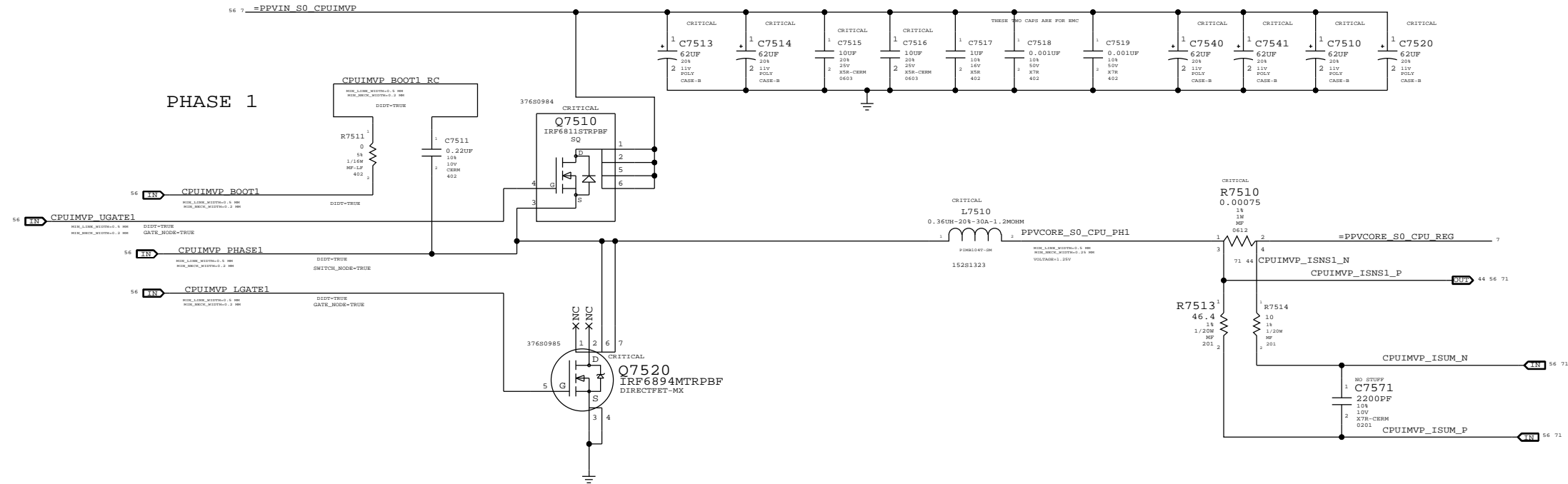
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0460	1	RES, MF, 60.4KOHM, 1/1/20W, 0201	R7316		LVDDR3_HW:YES

If LVDDR3\_HW:NO is turned ON, switch R2821 & R7971 back to the original value for 1.5V DDR unless 1V5R1V35\_SW is turned ON

1.5V DDR3 Supply			
Apple Inc.		DRAWING NUMBER	051-9276
		REVISION	2.7.0
		BRANCH	
		PAGE	73 OF 109
		SHEET	55 OF 72
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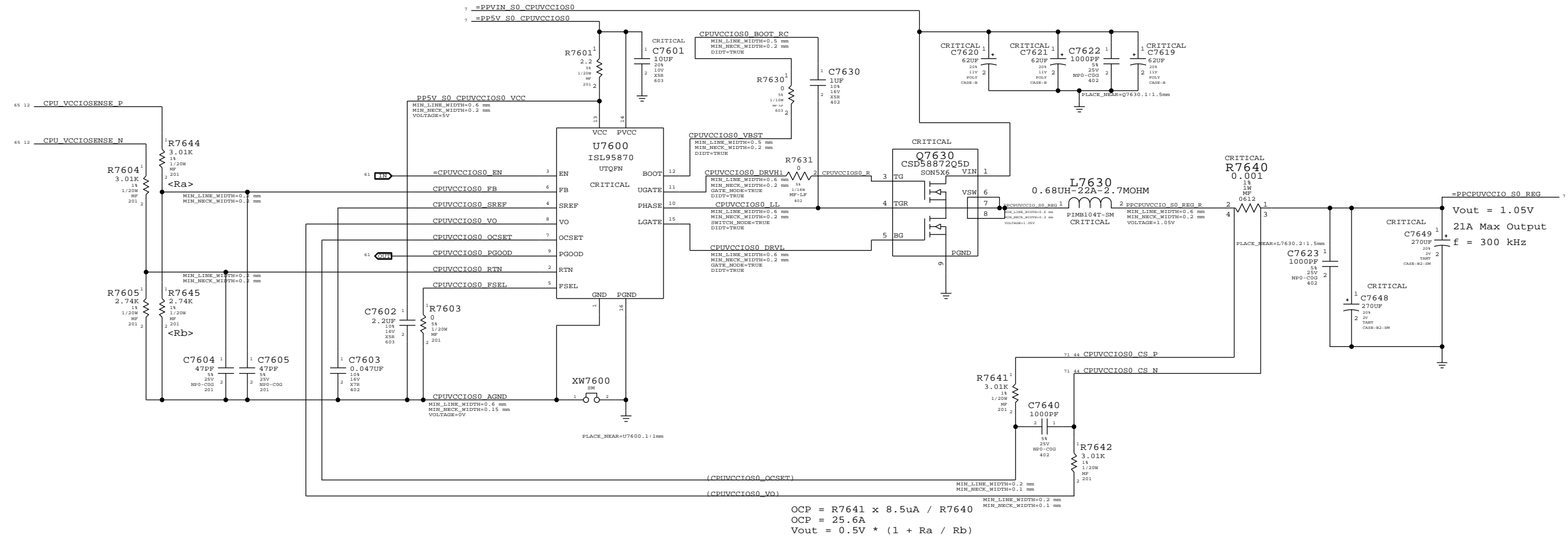


CPU=IV Bridge ULV, AXG=GT2



CPU IMVP7 & AXG VCore Output		
Apple Inc.		
DRAWING NUMBER	051-9276	SIZE D
REVISION	2.7.0	
BRANCH		
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CPU VCCIO (1.05V S0) Regulator



$$OCP = R7641 \times 8.5\mu A / R7640$$
$$OCP = 25.6A$$
$$V_{out} = 0.5V \times (1 + R_a / R_b)$$

SYNOPSIS: CPU VCCIO (1.05V) Power Supply		SYNOPSIS: CPU VCCIO (1.05V) Power Supply
DRAWING NUMBER		051-9276
REVISION		2.7.0
BRANCH		
PAGE		76 OF 109
SHEET		58 OF 72

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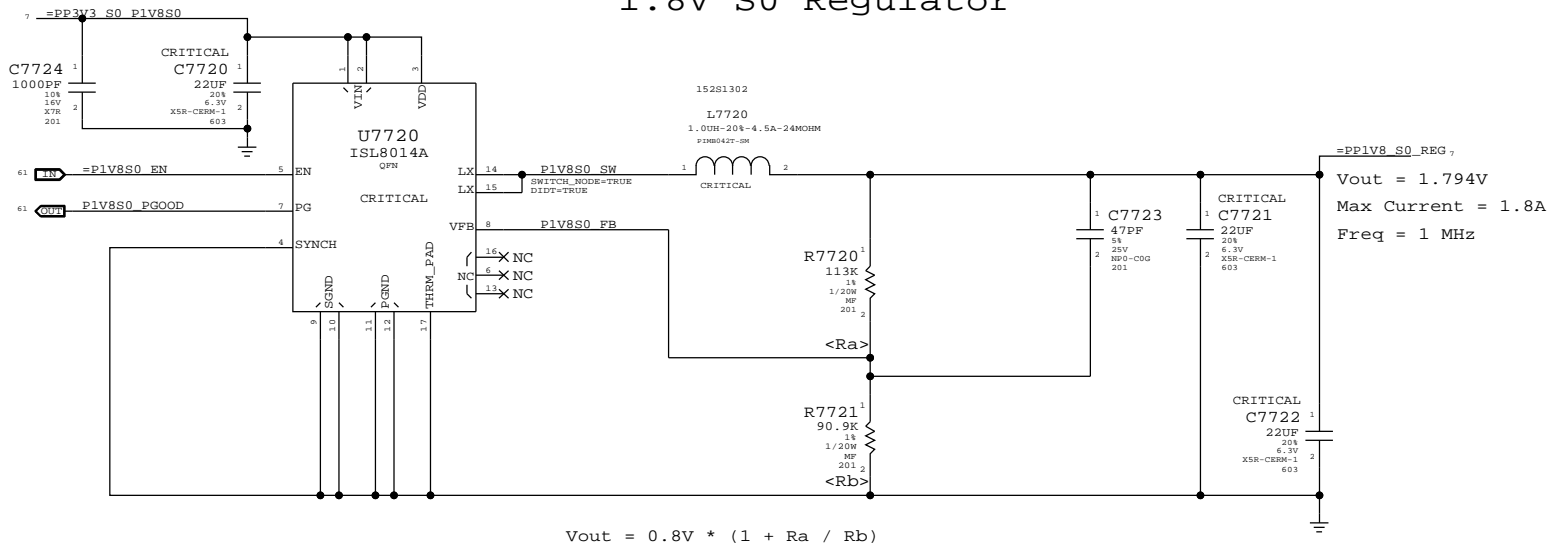
C

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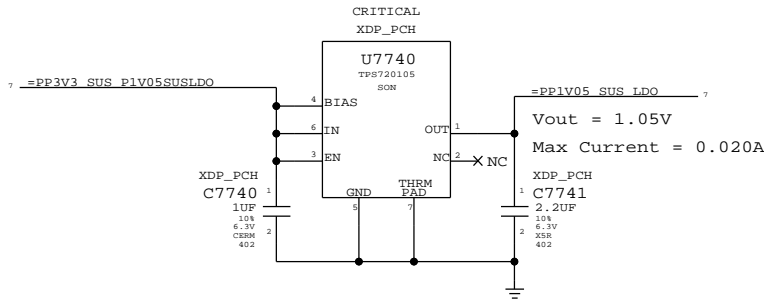
8 7 6 5 4 3 2 1

### 1.8V S0 Regulator

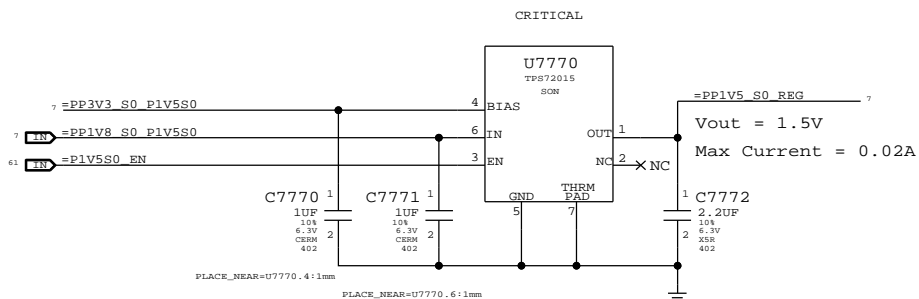


### 1.05V SUS LDO

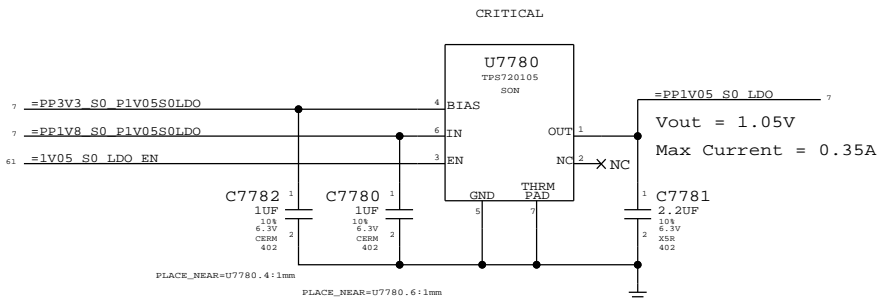
Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.




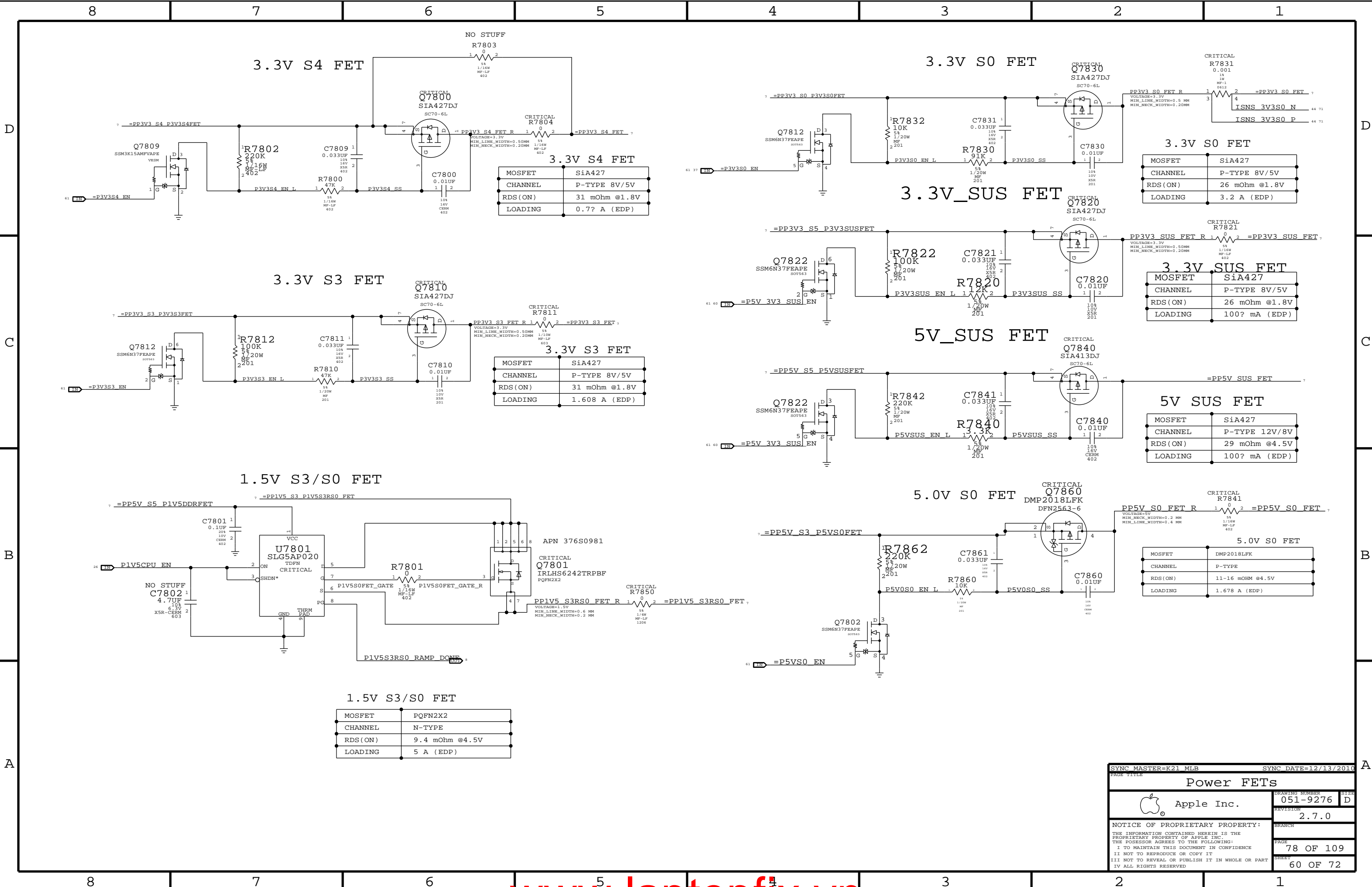
### 1.5V S0 LDO



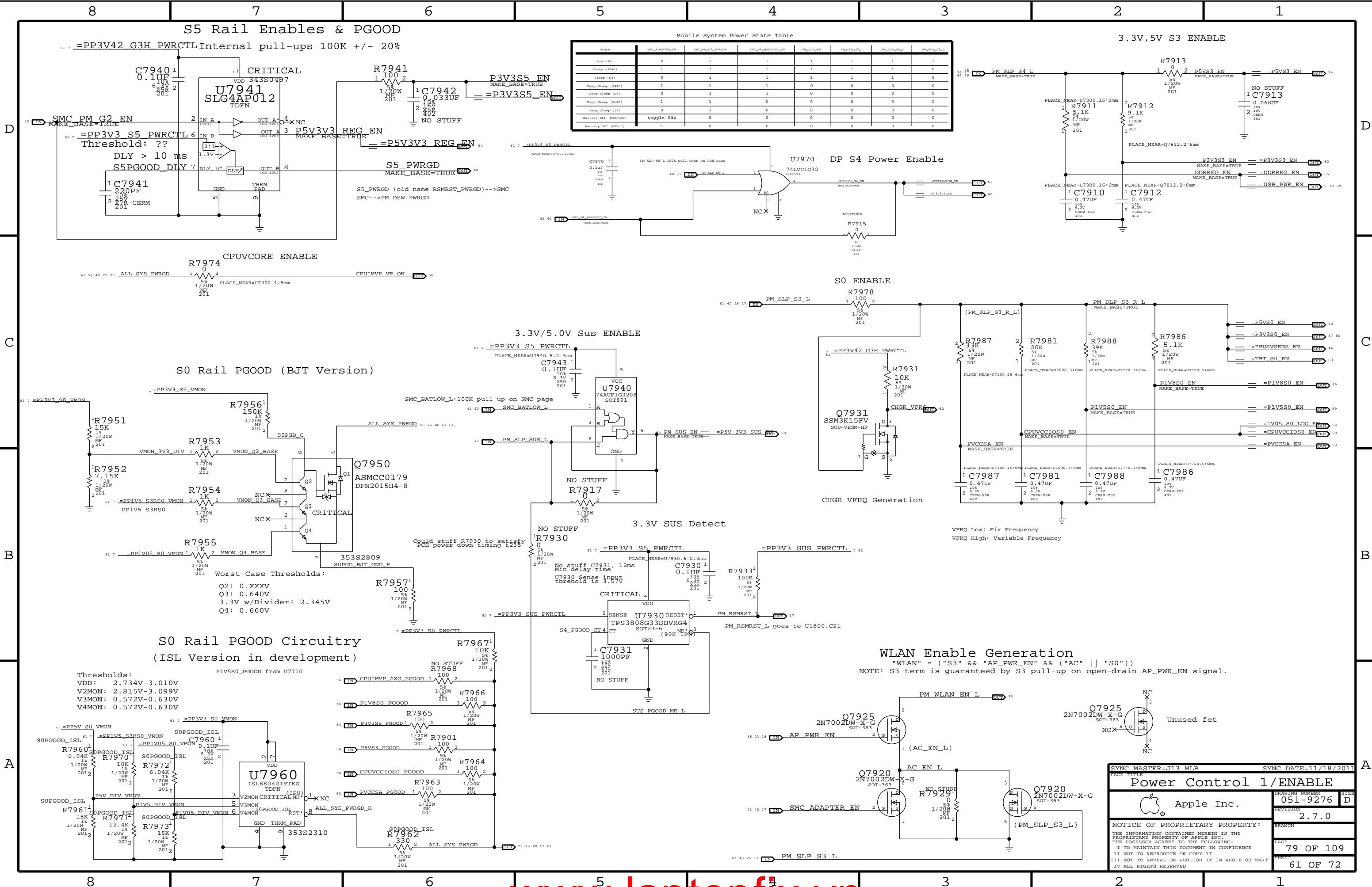
### 1.05V S0 LDO

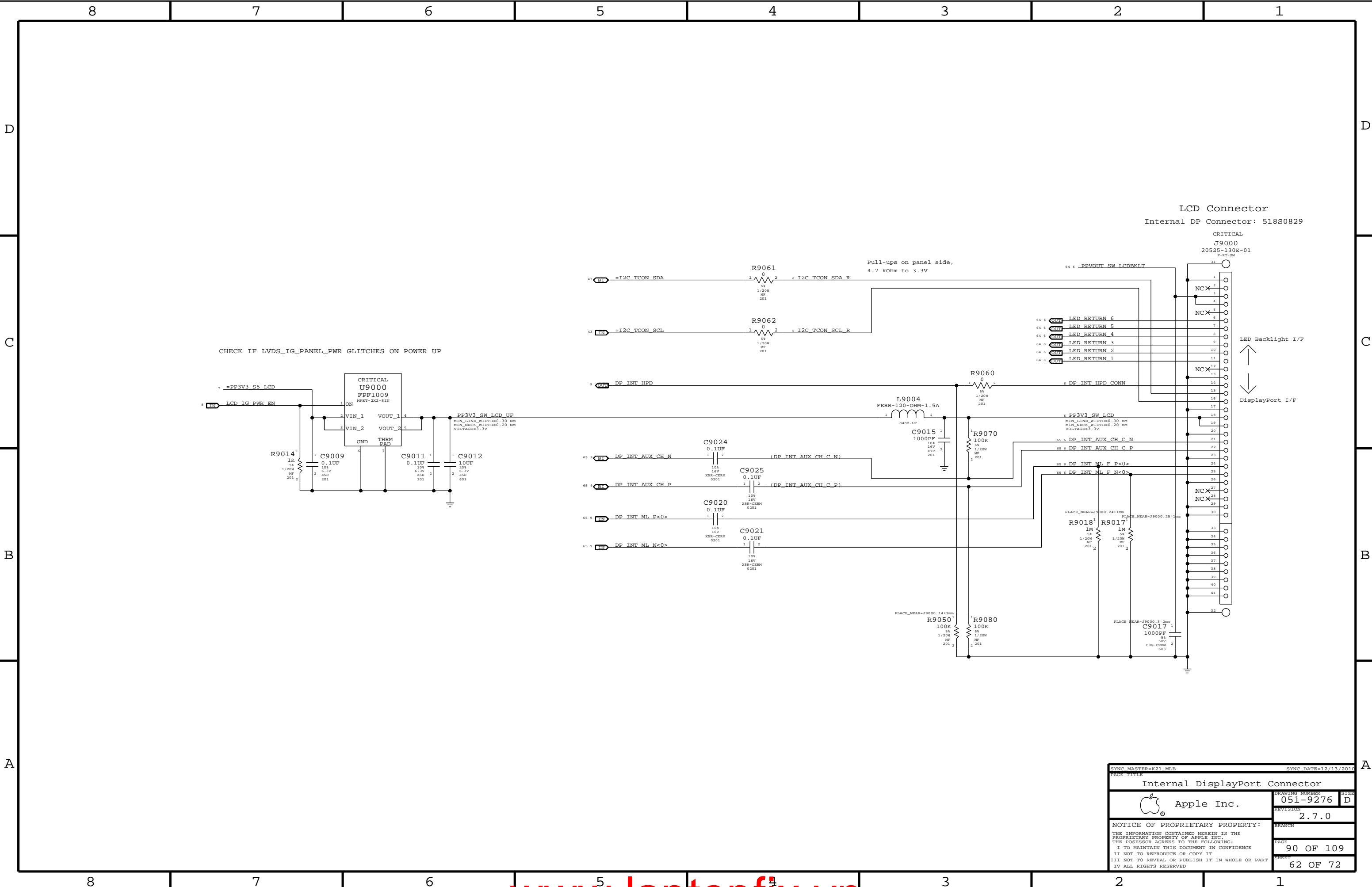



SYNC MASTER=K21 MLB		SYNC DATE=12/13/2010	
PAGE TITLE			
Misc Power Supplies			
	Apple Inc.	DRAWING NUMBER	051-9276
		SIZE	D
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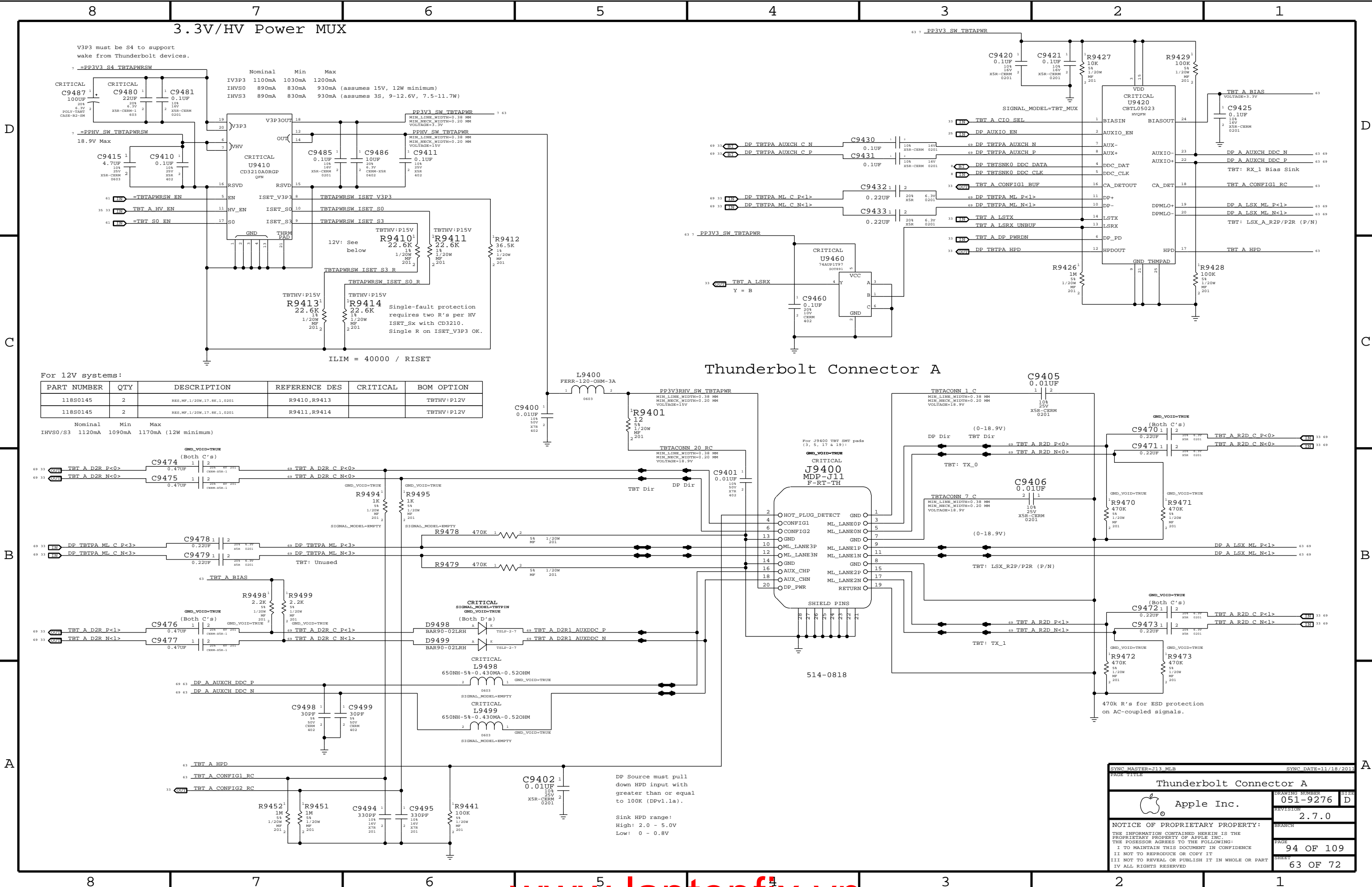


SYNC MASTER=K21 MLB		SYNC DATE=12/13/2010	
PAGE TITLE		Power FETs	
Apple Inc.		DRAWING NUMBER	051-9276
		REVISION	2.7.0
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SYNC MASTER=K21 MLB		SYNC DATE=12/13/2010	
PAGE TITLE			
Internal DisplayPort Connector			
 Apple Inc.	DRAWING NUMBER		SHEET
	051-9276		D
REVISION		2.7.0	
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MP,1/20W,17.8K,1,0201	R9410,R9413		TBTHV:P12V
118S0145	2	RES,MP,1/20W,17.8K,1,0201	R9411,R9414		TBTHV:P12V

	Nominal	Min	Max
IHVSO/S3	1120mA	1090mA	1170mA (12W minimum)

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:  
High: 2.0 - 5.0V  
Low: 0 - 0.8V

SYNC MASTER=J13 MLB		SYNC DATE=11/18/2013	
PAGE TITLE			
Thunderbolt Connector A		DRAWING NUMBER	051-9276
Apple Inc.		REVISION	2.7.0
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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.100 MM	0.100 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_AGTL	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SEQUENCE
CPU_8MIL	*	*	CPU_8MIL_2ANY

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SEQUENCE
CPU_ITP	*	*	CPU_ITP_2ANY

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SEQUENCE
CPU_COMP	CPU_COMP	*	CPU_COMP_2SEL
CPU_COMP	*	*	CPU_COMP_20TH

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SEQUENCE
CPU_VCCSENSE	CPU_VCCSENSE	*	CPU_VCCSENSE_25E
CPU_VCCSENSE	*	*	CPU_VCCSENSE_20TH

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_8MIL_2ANY	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ITP_2ANY	*	=4x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_COMP_20THER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	*	=4x_DIELECTRIC	?
CPU_COMP_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	TOP, BOTTOM	=6x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	TOP, BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	*	=4x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	*	=6x_DIELECTRIC	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
CLK_PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE	CLK_PCIE	*	CLK_PCIE_2SELF	CLK_PCIE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CLK_PCIE	*	*	CLK_PCIE_2OTHER	CLK_PCIE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	*	=4x_DIELECTRIC	?
CLK_PCIE_2OTHER	*	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_CPU_TX	PCIE_CPU_TX	*	PCIE_TX2TX	PCIE_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_CPU_RX	PCIE_CPU_RX	*	PCIE_RX2RX	PCIE_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2OTHERTX	PCIE_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_CPU_RX	*_CPU_RX	*	PCIE_RX2OTHERRX	PCIE_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_CPU_TX	*_CPU_RX	*	PCIE_TX2RX	PCIE_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_CPU_RX	*_CPU_TX	*	PCIE_RX2TX	PCIE_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_CPU_TX	*_TX	*	PCIE_20THERHS	PCIE_20THERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
PCIE_CPU_RX	*_TX	*	PCIE_20THERHS	PCIE_20THER	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_CPU_TX	*_RX	*	PCIE_20THERHS				
PCIE_CPU_RX	*_RX	*	PCIE_20THERHS				
PCIE_CPU_TX	*	*	PCIE_20THER				
PCIE_CPU_RX	*	*	PCIE_20THER				

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_PCH_TX	PCIE_PCH_TX	*	PCIE_TX2TX
PCIE_PCH_RX	PCIE_PCH_RX	*	PCIE_RX2RX
PCIE_PCH_TX	*_PCH_TX	*	PCIE_TX2OTHERTX
PCIE_PCH_RX	*_PCH_RX	*	PCIE_RX2OTHERRX
PCIE_PCH_TX	*_PCH_RX	*	PCIE_TX2RX
PCIE_PCH_RX	*_PCH_TX	*	PCIE_RX2TX
PCIE_PCH_TX	*_TX	*	PCIE_20THERHS
PCIE_PCH_RX	*_TX	*	PCIE_20THERHS
PCIE_PCH_TX	*_RX	*	PCIE_20THERHS
PCIE_PCH_RX	*_RX	*	PCIE_20THERHS
PCIE_PCH_TX	*	*	PCIE_20THER
PCIE_PCH_RX	*	*	PCIE_20THER

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
<input type="checkbox"/>	DMT_S2N	PCIE_80D	PCIE_PCH_TX	DMI S2N P<3:0>	9 17
<input type="checkbox"/>	DMT_S2N	PCIE_80D	PCIE_PCH_TX	DMI S2N N<3:0>	9 17
<input type="checkbox"/>	DMT_N2S	PCIE_80D	PCIE_PCH_RX	DMI N2S P<3:0>	9 17
<input type="checkbox"/>	DMT_N2S	PCIE_80D	PCIE_PCH_RX	DMI N2S N<3:0>	9 17
<input type="checkbox"/>	FDI_DATA	PCIE_80D	PCIE_PCH_RX	FDI DATA P<7:0>	9 17
<input type="checkbox"/>	FDI_DATA	PCIE_80D	PCIE_PCH_RX	FDI DATA N<7:0>	9 17
<input type="checkbox"/>		CPU_45S	CPU_AGTL	FDI FSYNC<1..0>	9 17
<input type="checkbox"/>		CPU_45S	CPU_AGTL	FDI LSYNC<1..0>	9 17
<input type="checkbox"/>		CPU_45S	CPU_AGTL	FDI INT	9 17

CPU_PECT	CPU_45S	CPU_COMP	CPU_PECT	10 19 41
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	10 17
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	10 17 26





	CPU_45S	CPU_I7P	XDP DBRESET L	10 23 25
	CPU_45S	CPU_I7P	XDP CPU PRDY L	10 23
	CPU_45S	CPU_I7P	XDP CPU PREQ L	10 23

	CPU1_27B4S	CPU1_COMP	EDP_COMP	9
	CPU1_27B4S	CPU1_COMP	CPU_PEG_COMP	9
CPU1_SM_RCOMP	CPU1_27B4S	CPU1_COMP	CPU1_SM_RCOMP<0>	10
CPU1_SM_RCOMP	CPU1_27B4S	CPU1_COMP	CPU1_SM_RCOMP<1>	10
CPU1_SM_RCOMP	CPU1_27B4S	CPU1_COMP	CPU1_SM_RCOMP<2>	..

	CPU_45S	CPU_TDR	CPU_CAGSTL_102	9.23
	CPU_CATERR_L	CPU_45S	CPU_CATERR_L	10.40
	CPU_45S	CPU_AGTL	CPU_VCCIO_SEL	12
	CPU_BROCHOT_L	CPU_45S	CPU_PROCHOT_L	10.40 41
	CPU_PWRGD	CPU_45S	CPU_AGTL	10.19 23

DMT_CLK100M	CLK_PCFE_80D	CLK_PCFE	DMI_CLK100M_CPU_P	10 16
DMI_CLK100M	CLK_PCFE_80D	CLK_PCFE	DMI_CLK100M_CPU_N	10 16
DPLL_REF_CLK120M	CLK_PCFE_80D	CLK_PCFE	DPLL_REF_CLKP	8 10
DPLL_REF_CLK120M	CLK_PCFE_80D	CLK_PCFE	DPLL_REF_CLKN	8 10
ITPCPU_CLK100M	CLK_PCFE_80D	CLK_PCFE	ITPCPU_CLK100M_P	10 16

ITPCPU_CLK100M	CLK_PCTE_80D	CLK_PCTE	ITPXPDP_CLK100M_P	16	23
ITPCPU_CLK100M	CLK_PCTE_80D	CLK_PCTE	ITPXPDP_CLK100M_N	16	23
ITPCPU_CLK100M	CLK_PCTE_80D	CLK_PCTE	XDP_CPU_CLK100M_P	16	23
ITPCPU_CLK100M	CLK_PCTE_80D	CLK_PCTE	XDP_CPU_CLK100M_N	16	23

	XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO	10_23
	XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS	10_23
	XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK	10_23
	XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPU_TRST_L	10_23
	YDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<3..0>	10_23

(XDP_BPM_L_R_CFG)	CPU_45S	CPU_ITP	XDP_OBSDATA B<3..0>	10 23
(XDP_BPM_L_R_CFG)	CPU_45S	CPU_ITP	XDP_OBSDATA B<3..0>	9
(XDP_BPM_L_R_CFG)	CPU_45S	CPU_ITP	CPU_CFG<15..12>	9 23
(FSB_CPURST_L)	CPU_45S	CPU_ITP	XDP_CPURST L	23

0000	CPU_VCCSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_P	12_56
0000	CPU_VCCSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_N	12_56
0000	CPU_VCCIOSENSE	SENSE_1T01_P2MM	CPU_VCCIOSENSE	CPU_VCCIOSENSE_P	12_58
0000	CPU_VCCIOSENSE	SENSE_1T01_P2MM	CPU_VCCIOSENSE	CPU_VCCIOSENSE_N	12_58
0000	CPU_AYX_SENSE	SENSE_1T01_P2MM	CPU_AYX_SENSE	CPU_AYX_SENSE_P	12_58

CPU_AIX_VSENSE	SENSE[111] 2764s	CPU_VCCSENSE	CPU_HVS_VSENSE_P	12	56
CPU_VALSENSE	CPU 27P4s	CPU_VCCSENSE	CPU_VDDO SENSE P	12	
CPU_VALSENSE	CPU 27P4s	CPU_VCCSENSE	CPU_VDDO SENSE N	12	
CPU_VALSENSE	CPU 27P4s	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	9	
CPU_VALSENSE	CPU 27P4s	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	9	
CPU_VALSENSE	CPU 27P4s	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	9	
CPU_VALSENSE	CPU 27P4s	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	9	


CPU_SVIDALERT_L	CPU_45S	CPU_COMP	CPU VIDALERT L	12 56
CPU_SVIDSCLK	CPU_45S	CPU_COMP	CPU VIDSCLK	12 56
CPU_SVIDSOUT	CPU_45S	CPU_COMP	CPU VIDSOUT	12 56

PCIE_CPU_MUX_R2D	PCIE_R0D	PCIE_CPU_TX	PCIE_SSD_R2D_C_P<0>	6 37
PCIE_CPU_MUX_R2D	PCIE_R0D	PCIE_CPU_TX	PCIE_SSD_R2D_C_N<0>	6 37
PCIE_R0D	PCIE_R0D	PCIE_CPU_TX	PCIE_SSD_R2D_MUX_IN_P	37
PCIE_R0D	PCIE_R0D	PCIE_CPU_TX	PCIE_SSD_R2D_MUX_IN_N	37
PCIE_CPU_MUX_R2D	PCIE_R0D	PCIE_CPU_TX	PCIE_SSD_R2D_P<0>	

PCIE_CPU_MUX_D2R	PCIE_80D	PCIE_CPU_RX	PCIE SSD D2R N<0>	8 37
	PCIE_80D	PCIE_CPU_RX	PCIE SSD D2R MUX OUT P	37
	PCIE_80D	PCIE_CPU_RX	PCIE SSD D2R MUX OUT N	37


PCIe_CPU_SSD_R2D	PCIe_R0D	PCIe_CPU_RX	PCIe_SSD_R2D_C_P<1>	6.37
PCIe_CPU_SSD_R2D	PCIe_R0D	PCIe_CPU_RX	PCIe_SSD_R2D_C_N<1>	6.37
	PCIe_R0D	PCIe_CPU_TX	PCIe_SSD_R2D_P<1>	6.37
	PCIe_R0D	PCIe_CPU_TX	PCIe_SSD_R2D_N<1>	6.37
PCIe_CPU_SSD_R2D	PCIe_R0D	PCIe_CPU_RX	PCIe_SSD_R2D_P<1>	

PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R C N<1>	6 8 37
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R C P<1>	
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R C N<1>	

	PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD P	6 16 37
	PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD N	6 16 37

DP_INT_ML	DP_80D	DP_TX	DP_INT_ML F P<3..0>	6 62
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML N<3..0>	6 62
	DP_80D	DP_TX	DP_INT_ML F P<3..0>	6 62
	DP_80D	DP_TX	DP_INT_ML F N<3..0>	6 62

DP_INT_AUXCH	DP_RD0	DP_AUX	DP_INT_AUX_CH_C_P	6 62
DP_INT_AUXCH	DP_RD0	DP_AUX	DP_INT_AUX_CH_C_N	6 62
	DP_RD0	DP_AUX	DP_INT_AUX_CH_P	9 62
	DP_RD0	DP_AUX	DP_INT_AUX_CH_N	9 62

SYNCH MASTER=CONSTRAINTS		SYNCH DATE=01/11/2012	
PAGE TITLE			
CPU Constraints			
	Apple Inc.	DRAWING NUMBER	SIZE
		051-9276	D
		REVISION	
		2.7.0	
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1

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM_CMD2CTRL	*	=3x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=PWR_P2MM	?
MEM_2GND	*	=GND_P2MM	?
MEM_2OTHER	*	=6x_DIELECTRIC	?

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	MEM_*	*	MEM_2OTHERMEM

PalPilot Spacing

=2x\_DIELECTRIC

=5.7x\_DIELECTRIC

=4x\_DIELECTRIC

=4x\_DIELECTRIC

=8.6x\_DIELECTRIC

=5.7x\_DIELECTRIC

=PWR\_P2MM

=GND\_P2MM

=8.6x\_DIELECTRIC

"Real" Spacing

=2x\_DIELECTRIC

=3x\_DIELECTRIC

=3x\_DIELECTRIC

=3x\_DIELECTRIC

=6x\_DIELECTRIC

=4x\_DIELECTRIC

=PWR\_P2MM

=GND\_P2MM

=6x\_DIELECTRIC

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK P<5..0>	8 11 27 28 32
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK N<5..0>	8 11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM A CKE<3..0>	11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM A CS L<3..0>	11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM A ODT<3..0>	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A A<15..0>	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A BA<2..0>	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A RAS L	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A CAS L	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A WE L	11 27 28 32
MEM_A_DQ_BYTE0	MEM_45S	MEM_A_DATA_0	MEM A DQ<7..0>	11 27
MEM_A_DQ_BYTE1	MEM_45S	MEM_A_DATA_1	MEM A DQ<15..8>	11 27
MEM_A_DQ_BYTE2	MEM_45S	MEM_A_DATA_2	MEM A DQ<23..16>	11 27
MEM_A_DQ_BYTE3	MEM_45S	MEM_A_DATA_3	MEM A DQ<31..24>	11 27
MEM_A_DQ_BYTE4	MEM_45S	MEM_A_DATA_4	MEM A DQ<39..32>	11 28
MEM_A_DQ_BYTE5	MEM_45S	MEM_A_DATA_5	MEM A DQ<47..40>	11 28
MEM_A_DQ_BYTE6	MEM_45S	MEM_A_DATA_6	MEM A DQ<55..48>	11 28
MEM_A_DQ_BYTE7	MEM_45S	MEM_A_DATA_7	MEM A DQ<63..56>	11 28
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM A DQS P<0>	11 27
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM A DQS N<0>	11 27
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM A DQS P<1>	11 27
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM A DQS N<1>	11 27
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM A DQS P<2>	11 27
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM A DQS N<2>	11 27
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM A DQS P<3>	11 27
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM A DQS N<3>	11 27
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM A DQS P<4>	11 28
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM A DQS N<4>	11 28
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM A DQS P<5>	11 28
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM A DQS N<5>	11 28
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM A DQS P<6>	11 28
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM A DQS N<6>	11 28
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM A DQS P<7>	11 28
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM A DQS N<7>	11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK P<5..0>	8 11 29 30 32
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK N<5..0>	8 11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM B CKE<3..0>	11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM B CS L<3..0>	11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM B ODT<3..0>	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B A<15..0>	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B BA<2..0>	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B RAS L	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B CAS L	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B WE L	11 29 30 32
MEM_B_DQ_BYTE0	MEM_45S	MEM_B_DATA_0	MEM B DQ<7..0>	11 29
MEM_B_DQ_BYTE1	MEM_45S	MEM_B_DATA_1	MEM B DQ<15..8>	11 29
MEM_B_DQ_BYTE2	MEM_45S	MEM_B_DATA_2	MEM B DQ<23..16>	11 29
MEM_B_DQ_BYTE3	MEM_45S	MEM_B_DATA_3	MEM B DQ<31..24>	11 29
MEM_B_DQ_BYTE4	MEM_45S	MEM_B_DATA_4	MEM B DQ<39..32>	11 30
MEM_B_DQ_BYTE5	MEM_45S	MEM_B_DATA_5	MEM B DQ<47..40>	11 30
MEM_B_DQ_BYTE6	MEM_45S	MEM_B_DATA_6	MEM B DQ<55..48>	11 30
MEM_B_DQ_BYTE7	MEM_45S	MEM_B_DATA_7	MEM B DQ<63..56>	11 30
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM B DQS P<0>	11 29
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM B DQS N<0>	11 29
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM B DQS P<1>	11 29
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM B DQS N<1>	11 29
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM B DQS P<2>	11 29
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM B DQS N<2>	11 29
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM B DQS P<3>	11 29
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM B DQS N<3>	11 29
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM B DQS P<4>	11 30
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM B DQS N<4>	11 30
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM B DQS P<5>	11 30
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM B DQS N<5>	11 30
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM B DQS P<6>	11 30
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM B DQS N<6>	11 30
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM B DQS P<7>	11 30
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM B DQS N<7>	11 30
		MEM_PWR	PP1V5 S3RS0	6 7
		MEM_PWR	PP1V5 S3	6 7
		MEM_PWR	PP0V75 S3 MEM VREFCA A	27 28 31
		MEM_PWR	PP0V75 S3 MEM VREFDO A	27 28 31

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Memory Constraints

Apple Inc.

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## SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ICOMP	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA3_PCH_TX	SATA3_PCH_TX	*	SATA3_TX2TX
SATA3_PCH_RX	SATA3_PCH_RX	*	SATA3_RX2RX
SATA3_PCH_TX	*_PCH_TX	*	SATA3_TX2OTHERS
SATA3_PCH_RX	*_PCH_RX	*	SATA3_RX2OTHERS
SATA3_PCH_TX	*_PCH_RX	*	SATA3_TX2RX
SATA3_PCH_RX	*_PCH_TX	*	SATA3_RX2TX
SATA3_PCH_TX	*_TX	*	SATA3_2OTHERS
SATA3_PCH_RX	*_RX	*	SATA3_2OTHERS
SATA3_PCH_TX	*_RX	*	SATA3_2OTHERS
SATA3_PCH_RX	*	*	SATA3_2OTHER
SATA3_PCH_RX	*	*	SATA3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_TX20THERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_RX20THERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
SATA3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
SATA3_20THERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
SATA3_20THER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA3_TX2TX	*	= 2.5x_DIELECTRIC	?
SATA3_RX2RX	*	= 2.5x_DIELECTRIC	?
SATA3_TX20THERTX	*	= 4x_DIELECTRIC	?
SATA3_RX20THERRX	*	= 4x_DIELECTRIC	?
SATA3_TX2RX	*	= 6x_DIELECTRIC	?
SATA3_RX2TX	*	= 6x_DIELECTRIC	?
SATA3_20THERHS	*	= 4x_DIELECTRIC	?
SATA3_20THER	*	= 3x_DIELECTRIC	?

SOURCE: 471984\_Chief\_River\_MS\_PDG\_1.0 and the spacing rule is adjusted per SI team feedback.

## UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x_DIELECTRIC	?

## USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP , BOTTOM	= 4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905\_v1.5), Section 3.8

## USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_PCH_TX	USB3_PCH_TX	*	USB3_TX2TX
USB3_PCH_RX	USB3_PCH_RX	*	USB3_RX2RX
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2OTHERTX
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2OTHERRX
USB3_PCH_TX	*_PCH_RX	*	USB3_TX2RX
USB3_PCH_RX	*_PCH_TX	*	USB3_RX2TX
USB3_PCH_TX	*_TX	*	USB3_2OTHERHS
USB3_PCH_RX	*_TX	*	USB3_2OTHERHS
USB3_PCH_TX	*_RX	*	USB3_2OTHERHS
USB3_PCH_RX	*_RX	*	USB3_2OTHERHS
USB3_PCH_TX	*	*	USB3_2OTHER
USB3_PCH_RX	*	*	USB3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX20THERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX20THERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_20THERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_20THER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	*	=2.5x_DIELECTRIC	?
USB3_RX2RX	*	=2.5x_DIELECTRIC	?
USB3_TX20THERTX	*	=4x_DIELECTRIC	?
USB3_RX20THERRX	*	=4x_DIELECTRIC	?
USB3_TX2RX	*	=6x_DIELECTRIC	?
USB3_RX2TX	*	=6x_DIELECTRIC	?
USB3_20THERHS	*	=4x_DIELECTRIC	?
USB3_20THER	*	=3x_DIELECTRIC	?

SOURCE: 471984\_Cheif\_River\_MS\_PDG\_1.0 and the spacing rule is adjusted per SI team feedback.

## PCH Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	SATA_PCH_MUX_R2D	SATA_80D	SATA3_PCH_TX	SATA HDD R2D C P16 37
	SATA_PCH_MUX_R2D	SATA_80D	SATA3_PCH_TX	SATA HDD R2D C N16 37
		SATA_80D	SATA3_PCH_TX	SATA SSD R2D MUX IN P37
		SATA_80D	SATA3_PCH_TX	SATA SSD R2D MUX IN N37
	SATA_MUX_SSD_R2D	SATA_80D	SATA3_PCH_TX	SATA SSD R2D P6 37
	SATA_MUX_SSD_R2D	SATA_80D	SATA3_PCH_TX	SATA SSD R2D N6 37
	SATA_PCH_MUX_D2R	SATA_80D	SATA3_PCH_RX	SATA HDD D2R P16 37
	SATA_PCH_MUX_D2R	SATA_80D	SATA3_PCH_RX	SATA HDD D2R N16 37
		SATA_80D	SATA3_PCH_RX	SATA SSD D2R MUX OUT P37
		SATA_80D	SATA3_PCH_RX	SATA SSD D2R MUX OUT N37
	SATA_MUX_SSD_D2R	SATA_80D	SATA3_PCH_RX	SATA SSD D2R P6 37
	SATA_MUX_SSD_D2R	SATA_80D	SATA3_PCH_RX	SATA SSD D2R N6 37
	PCH_SATA_ICOMP		SATA_ICOMP	PCH SATAICOMP16
		USB_80D	USB	USB HUB UP P18 24
		USB_80D	USB	USB HUB UP N18 24
	USB_BT	USB_80D	USB	USB BT P24 36
	USB_BT	USB_80D	USB	USB BT N24 36
		USB_80D	USB	USB BT CONN P6 36
		USB_80D	USB	USB BT CONN N6 36
		USB_80D	USB	USB BT WAKE P36
		USB_80D	USB	USB BT WAKE N36
	USB_TPAD	USB_80D	USB	USB TPAD P6 48
	USB_TPAD	USB_80D	USB	USB TPAD N6 48
		USB_80D	USB	USB TPAD CONN P
		USB_80D	USB	USB TPAD CONN N
	USB_TPAD_HUB	USB_80D	USB	USB TPAD HUB P24
	USB_TPAD_HUB	USB_80D	USB	USB TPAD HUB N24
		USB_80D	USB	USB TPAD R P24 48
		USB_80D	USB	USB TPAD R N24 48
	USB_TPAD_M	USB_80D	USB	USB TPAD M P48
	USB_TPAD_M	USB_80D	USB	USB TPAD M N48
	USB_SDCARD	USB_80D	USB	USB SDCARD P8 24
	USB_SDCARD	USB_80D	USB	USB SDCARD N8 24
	USB_SMC	USB_80D	USB	USB SMC P24 40
	USB_SMC	USB_80D	USB	USB SMC N24 40
	USB_CAMERA	USB_80D	USB	USB CAMERA P6 18 39
	USB_CAMERA	USB_80D	USB	USB CAMERA N6 18 39
	USB_EXTA	USB_80D	USB	USB EXTA P18 38
	USB_EXTA	USB_80D	USB	USB EXTA N18 38
	UART_45S	UART		SMC DEBUGPRT TX L30 40 41
	UART_45S	UART		SMC DEBUGPRT RX L30 40 41
		USB_80D	USB	USB2 EXTA MUXED P38
		USB_80D	USB	USB2 EXTA MUXED N38
		USB_80D	USB	USB2 EXTA MUXED F P38
		USB_80D	USB	USB2 EXTA MUXED F N38
	USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3 EXTA RX P18 38
	USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3 EXTA RX N18 38
	USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3 EXTA TX P18 38
	USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3 EXTA TX N18 38
		USB_80D	USB3_PCH_RX	USB3 EXTA RX F P38
		USB_80D	USB3_PCH_RX	USB3 EXTA RX F N38
		USB_80D	USB3_PCH_TX	USB3 EXTA TX F P38
		USB_80D	USB3_PCH_TX	USB3 EXTA TX F N38
		USB_80D	USB3_PCH_TX	USB3 EXTA TX C P38
		USB_80D	USB3_PCH_TX	USB3 EXTA TX C N38
	USB_EXTB	USB_80D	USB	USB EXTB P6 24 39
	USB_EXTB	USB_80D	USB	USB EXTB N6 24 39
		USB_80D	USB	USB EXTB EHCI P18 24
		USB_80D	USB	USB EXTB EHCI N18 24
		USB_80D	USB	USB EXTB XHCI P18 24
		USB_80D	USB	USB EXTB XHCI N18 24
	USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3 EXTB RX P18 39
	USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3 EXTB RX N18 39
		USB_80D	USB3_PCH_RX	USB3 EXTB RX RC P6 39
		USB_80D	USB3_PCH_RX	USB3 EXTB RX RC N6 39
		USB_80D	USB3_PCH_RX	USB3 EXTB RX CONN P
		USB_80D	USB3_PCH_RX	USB3 EXTB RX CONN N
	USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3 EXTB TX P18 39
	USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3 EXTB TX N18 39
		USB_80D	USB3_PCH_TX	USB3 EXTB TX C P6 39
		USB_80D	USB3_PCH_TX	USB3 EXTB TX C N6 39
	(USB_TPAD_HUB)	USB_80D	USB	USB EXTD XHCI P18 24
	(USB_TPAD_HUB)	USB_80D	USB	USB EXTD XHCI N18 24
	PCH_USB_RBIAS			PCH USB RBIAS18
	CLK_PCIE_80D	CLK_PCIE		PCIE CLK100M PCH P16
	CLK_PCIE_80D	CLK_PCIE		PCIE CLK100M PCH N16
	CLK_PCIE_80D	CLK_PCIE		PCH CLK96M DOT P16
	CLK_PCIE_80D	CLK_PCIE		PCH CLK96M DOT N16
	CLK_PCIE_80D	CLK_PCIE		PCH CLK100M SATA P16
	CLK_PCIE_80D	CLK_PCIE		PCH CLK100M SATA N16
	CPU_45S	CLK_PCIE		PCH CLK14P3M REFCLK16

SATA SSD


## USB Hub nets

USB Camera nets

USB EXTA nets (Right USB port)

USB EXTB nets (Left USB port)

Unused USB nets

SYNC MASTER=CONSTRAINTS		SYNC DATE=01/11/2012	
PAGE TITLE			
PCH Constraints 1			
	Apple Inc.	DRAWING NUMBER	051-9276
		SIZE	D
	REVISION	2.7.0	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
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		SHEET 67 OF 72	

## LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x_DIELECTRIC	?
CLK_LPC	*	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ixex Peak M (DG-398905-398905\_v1.5), Section 3.15

## SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S_R_50S	TOP,BOTTOM	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE		
SMB_45S_R_50S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

## HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for IbeX Peak M (DG-398905-398905\_v1.5), Section 3.15

## SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?

## SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x <sub>DIELECTRIC</sub>	?

## XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_ITP	*	=2:1_SPACING	?

## DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	*	=3x_DIELECTRIC	?
DP_2OTHERHS	*	=4x_DIELECTRIC	?
DP_2OTHER	*	=3x_DIELECTRIC	?
DP_AUX	*	=3x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_TX	DP_TX	*	DP_2DP
DP_TX	*_TX	*	DP_2OTHERHS
DP_TX	*_RX	*	DP_2OTHERHS
DP_TX	*	*	DP_2OTHER

## System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

















SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.









## PCH Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	LPC_AD	LPC_45S	LPC	LPC AD<3..0>	6 16 40
	LPC_FRAME_L	LPC_45S	LPC	LPC FRAME_L	6 16 40 42
		LPC_45S	LPC	LPCPLUS RESET_L	6 25 42
	LPC_CLK33M	CLK LPC_45S	CLK LPC	LPC CLK33M_SMC	25 40
		CLK LPC_45S	CLK LPC	LPC CLK33M_SMC_R	18 25
	LPC_CLK33M	CLK LPC_45S	CLK LPC	LPC CLK33M LPCPLUS	6 25 42
		CLK LPC_45S	CLK LPC	LPC CLK33M LPCPLUS_R	18 25
	LPC_CLK33M	CLK LPC_45S	CLK LPC	PCH CLK33M PCIIN	16 25
		CLK LPC_45S	CLK LPC	PCH CLK33M PCIOUT	18 25
	SMBUS_PCH_CLK	SMR_45S_R_50S	SMR	SMBUS_PCH_CLK	16 43
	SMBUS_PCH_DATA	SMR_45S_R_50S	SMR	SMBUS_PCH_DATA	16 43
	SMBUS_PCH_0_CLK	SMR_45S_R_50S	SMR	SML_PCH_0_CLK	16 43
	SMBUS_PCH_0_DATA	SMR_45S_R_50S	SMR	SML_PCH_0_DATA	16 43
	SMBUS_SMC_1_50_SCI	SMR_45S_R_50S	SMR	SML_PCH_1_CLK	16 43
	SMBUS_SMC_1_50_SDA	SMR_45S_R_50S	SMR	SML_PCH_1_DATA	16 43
	HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	6 16 39
		HDA_45S	HDA	HDA_BIT_CLK_R	16
	HDA_SYNC	HDA_45S	HDA	HDA_SYNC	6 16 39
		HDA_45S	HDA	HDA_SYNC_R	16
	HDA_RST_L	HDA_45S	HDA	HDA_RST_R_L	16
		HDA_45S	HDA	HDA_RST_L	6 16 39
	HDA_SDINO	HDA_45S	HDA	HDA_SDINO	6 16 39
	HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	6 16 39
		HDA_45S	HDA	HDA_SDOUT_R	16 25
	PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM_CLK32K_SUSCLK_R	17 41
		CLK_SLOW_45S	CLK_SLOW	SMC_CLK32K	40 41
	SPI_CLK	SPT_45S	SPT	SPI_CLK_R	16 42
		SPT_45S	SPT	SPT_CLK	42
	SPI_MOSI	SPT_45S	SPT	SPI_MOSI_R	16 42
		SPT_45S	SPT	SPI_MOSI	42
	SPI_MISO	SPT_45S	SPT	SPI_MISO	16 42
	SPI_CS0	SPT_45S	SPT	SPI_CS0_R_L	16 42
		SPT_45S	SPT	SPT_CS0_L	42
		SPT_45S	SPT	SPI_SMC_CLK	40 41
		SPT_45S	SPT	SPI_SMC_MOSI	40 41
		SPT_45S	SPT	SPI_SMC_MISO	40 41
		SPT_45S	SPT	SPI_SMC_CS_L	40 41
		SPT_45S	SPT	SPI_MLB_CLK	41 42 49
		SPT_45S	SPT	SPI_MLB_MOSI	41 42 49
		SPT_45S	SPT	SPI_MLB_MISO	41 42 49
		SPT_45S	SPT	SPI_MLB_CS_L	41 42 49
	PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_P	6 36
	PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_N	6 36
		PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_P	16 36
		PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_N	16 36
	PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_P	6 16 36
	PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_N	6 16 36
	PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_P	6 16 36
	PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_N	6 16 36
	PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_P<3..0>	33
	PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_N<3..0>	33
		PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_P<3..0>	8 33
		PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_N<3..0>	8 33
	PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_P<3..0>	8 33
	PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_N<3..0>	8 33
		PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_P<3..0>	33
		PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_N<3..0>	33
	PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_P	16 33
	PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_N	16 33
		CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_P	8 16
		CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_N	8 16
	XDP_TDI	PCH_45S	PCH_ITP	XDP_PCH_TDI	16 23
	XDP_TDO	PCH_45S	PCH_ITP	XDP_PCH_TDO	16 23
	XDP_TMS	PCH_45S	PCH_ITP	XDP_PCH_TMS	16 23
	XDP_TCK	PCH_45S	PCH_ITP	XDP_PCH_TCK	16 23

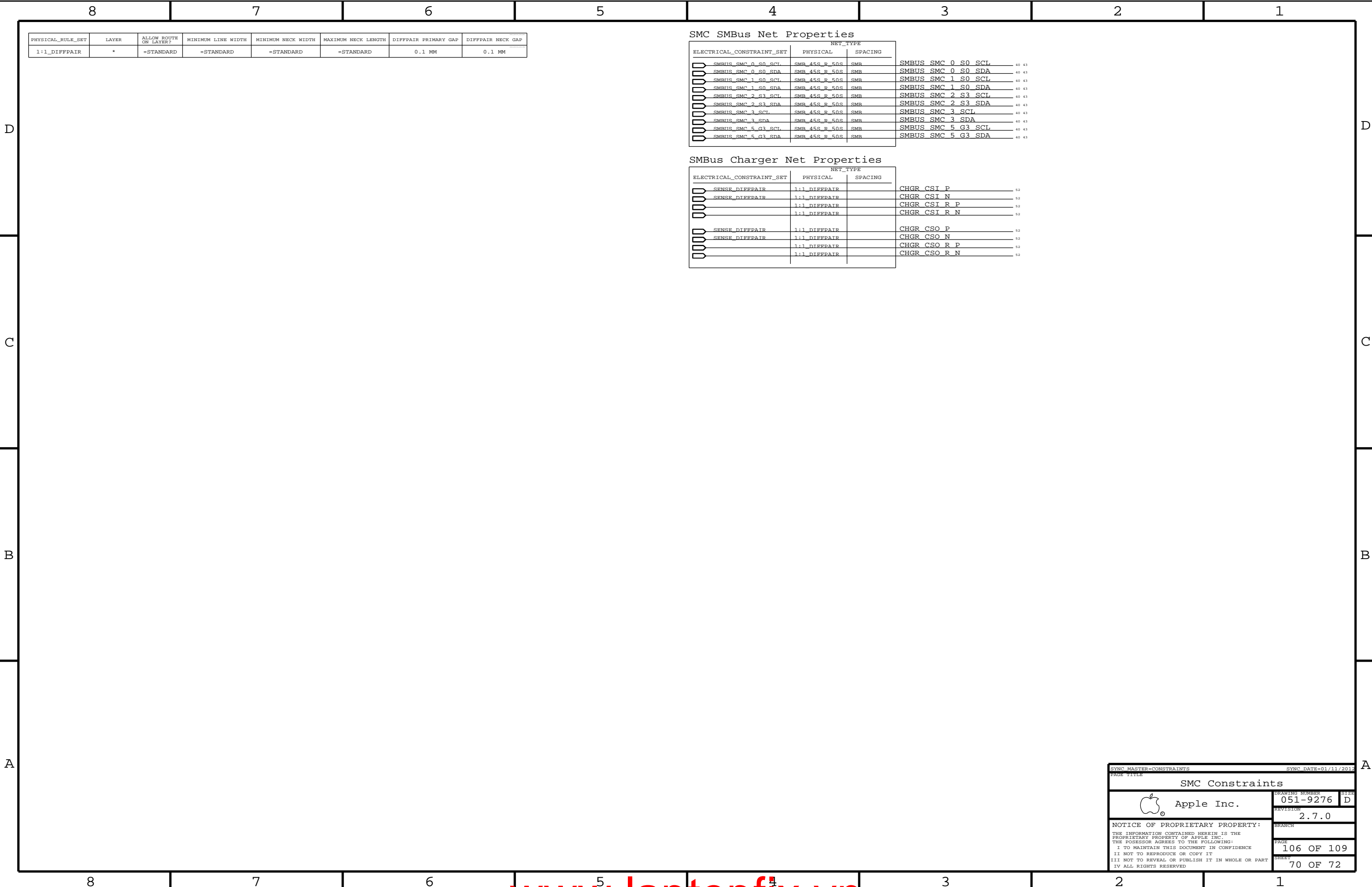
## Chipset Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	DP_TBT_ML	DP_80D	DP_TX	DP TBTSNK0 ML P<3..0>	33
	DP_TBT_ML	DP_80D	DP_TX	DP TBTSNK0 ML N<3..0>	33
	DP_TBT_ML	DP_80D	DP_TX	DP TBTSNK0 ML C P<3..0>	4 33
	DP_TBT_ML	DP_80D	DP_TX	DP TBTSNK0 ML C N<3..0>	4 33
	DP_TBT_AUXCH	DP_80D	DP_AUX	DP TBTSNK0 AUXCH P	33
	DP_TBT_AUXCH	DP_80D	DP_AUX	DP TBTSNK0 AUXCH N	33
	DP_TBT_AUXCH	DP_80D	DP_AUX	DP TBTSNK0 AUXCH C P	4 33
		DP_80D	DP_AUX	DP TBTSNK0 AUXCH C N	4 33
	DP_TBT_ML	DP_80D	DP_TX	DP TBTSNK1 ML P<3..0>	33
	DP_TBT_ML	DP_80D	DP_TX	DP TBTSNK1 ML N<3..0>	33
	DP_TBT_ML	DP_80D	DP_TX	DP TBTSNK1 ML C P<3..0>	4 33
	DP_TBT_ML	DP_80D	DP_TX	DP TBTSNK1 ML C N<3..0>	4 33
	DP_TBT_AUXCH	DP_80D	DP_AUX	DP TBTSNK1 AUXCH P	33
	DP_TBT_AUXCH	DP_80D	DP_AUX	DP TBTSNK1 AUXCH N	33
	DP_TBT_AUXCH	DP_80D	DP_AUX	DP TBTSNK1 AUXCH C P	4 33
		DP_80D	DP_AUX	DP TBTSNK1 AUXCH C N	4 33

## Clock Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTC	16 25
	SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB	16 25
		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB_R	16
	SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	25 33
		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	33
	SYSCLK_CLK25M_XTAL	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1	25
		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2	
		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R	25





A

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCIE	*	GND_P2MM
GND	PCIE*	*	GND_P2MM
GND	SATA*	*	GND_P2MM
GND	USB*	*	GND_P2MM
GND	LVDS*	*	GND_P2MM
SB_POWER	CLK_PCIE	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM

## A

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