1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

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REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2012-02-23

SCHEM,MLB,J13

2/23/12

Page (.csa)	Contents	Sync Date
1	Table of Contents	J30_MLB 07/27/2011
2	System Block Diagram	J13_MLB_NON_POR 11/10/2011
3	Revision History	J13_MLB_NON_POR 11/10/2011
4	Revision History	J30_MLB 07/27/2011
5	BOM Configuration	J30_MLB 07/27/2011
6	Functional Test / No Test	K21_MLB 07/29/2011
7	Power Aliases	K21_MLB 07/29/2011
8	Signal Aliases	J13_MLB_NON_POR 11/10/2011
9	CPU DMI/PEG/FDI/RSVD	J13_MLB_NON_POR 10/17/2011
10	CPU CLOCK/MISC/JTAG	J30_MLB 07/27/2011
11	CPU DDR3 INTERFACES	J30_MLB 07/27/2011
12	CPU POWER	J13_MLB_NON_POR 11/10/2011
13	CPU GROUNDS	J30_MLB 07/27/2011
14	CPU DECOUPLING-I	J11_MLB 10/03/2011
15	CPU DECOUPLING-II	K21_MLB 07/29/2011
16	PCH SATA/PCIe/CLK/LPC/SPI	J30_MLB 07/27/2011
17	PCH DMI/FDI/PM/Graphics	J30_MLB 07/27/2011
18	PCH PCI/USB/TP/RSVD	J13_MLB_NON_POR 11/10/2011
19	PCH GPIO/MISC/NCTF	J11_MLB 09/16/2011
20	PCH POWER	J11_MLB 09/30/2011
21	PCH GROUNDS	J30_MLB 07/27/2011
22	PCH DECOUPLING	J11_MLB 10/03/2011
23	CPU & PCH XDP	J13_MLB_NON_POR 10/17/2011
24	USB HUB & MUX	J13_MLB_NON_POR 11/10/2011
25	Clock (CK505) and Chipset Support	K21_MLB 07/29/2011
26	CPU Memory S3 Support	J13_MLB_NON_POR 11/10/2011
27	DDR3 DRAM CHANNEL A (0-31)	K21_MLB 07/28/2011
28	DDR3 DRAM CHANNEL A (32-63)	K21_MLB 07/28/2011
29	DDR3 DRAM CHANNEL B (0-31)	K21_MLB 07/28/2011
30	DDR3 DRAM CHANNEL B (32-63)	K21_MLB 07/28/2011
31	FSB/DDR3/FRAMEBUF Vref Margining	J11_MLB 08/04/2011
32	DDR3 Bypassing/Termination	K21_MLB 07/28/2011
33	SecureDigital Card Reader	J13_MLB_NON_POR 11/10/2011
34	Thunderbolt Host (1 of 2)	J11_MLB 09/30/2011
35	Thunderbolt Host (2 of 2)	J11_MLB 10/04/2011
36	TBT Power Support	J13_MLB_NON_POR 11/10/2011
37	X21 WIRELESS CONNECTOR	J11_MLB 10/11/2011
38	SSD CONNECTOR	J13_MLB_NON_POR 10/17/2011
39	External A USB3 Connector	J11_MLB 09/30/2011
40	Left I/O (LIO) Connector	J13_MLB_NON_POR 11/10/2011
41	SMC	J13_MLB_NON_POR 10/17/2011
42	SMC Support	J13_MLB_NON_POR 11/10/2011
43	LPC+SPI Debug Connector	J11_MLB 09/08/2011
44	SMBus Connections	J11_MLB 10/04/2011
45	Voltage & Load Side Current Sensing	J11_MLB 12/02/2011
46	High Side Current Sensing	J13_MLB_NON_POR 10/17/2011
47	Thermal Sensors	J11_MLB 08/03/2011
48	Fan	K21_MLB 07/28/2011
49	IPD / KBD Backlight	J13_MLB_NON_POR 11/10/2011
50	SPI ROM	K21_MLB 07/28/2011
51	AUDIO: SPEAKER AMP	J11_MLB 09/30/2011
52	DC-In & Battery Connectors	J13_MLB_NON_POR 11/10/2011
53	PBus Supply & Battery Charger	J13_MLB_NON_POR 11/10/2011
54	System Agent Supply	J13_MLB_NON_POR 10/17/2011
55	5V / 3.3V Power Supply	J13_MLB_NON_POR 10/17/2011
56	1.5V DDR3 Supply	J11_MLB 12/02/2011
57	CPU IMVP7 & AXG VCore Regulator	J11_MLB 10/14/2011
58	CPU IMVP7 & AXG VCore Output	J13_MLB_NON_POR 10/17/2011
59	CPU VCCIO (1.05V) Power Supply	J13_MLB_NON_POR 10/17/2011
60	Misc Power Supplies	K21_MLB 07/28/2011
61	Power FETs	K21_MLB 07/28/2011
62	Power Control 1/ENABLE	J13_MLB_NON_POR 11/10/2011
63	Internal DisplayPort Connector	K21_MLB 07/28/2011
64	Thunderbolt Connector A	J11_MLB 10/03/2011
65	LCD Backlight Driver	K21_MLB 07/28/2011
66	CPU Constraints	J13_CONSTRAINTS 01/11/2012
67	Memory Constraints	J13_CONSTRAINTS 01/11/2012
68	PCH Constraints 1	J13_CONSTRAINTS 01/11/2012
69	PCH Constraints 2	J13_CONSTRAINTS 01/11/2012
70	Thunderbolt Constraints	J13_CONSTRAINTS 01/11/2012
71	SMC Constraints	J13_CONSTRAINTS 01/11/2012
72	Project Specific Constraints	J13_CONSTRAINTS 01/11/2012
73	PCB Rule Definitions	J13_CONSTRAINTS 01/11/2012

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9277	1	SCHEM,MLB,J13	SCH	CRITICAL	
820-3209	1	PCBF,MLB,J13	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Thu Feb 23 17:52:06 2012

DRAWING TITLE: SCHEM,MLB,J13

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REVISION: 2.8.0
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PAGE: 1 OF 109
SHEET: 1 OF 73

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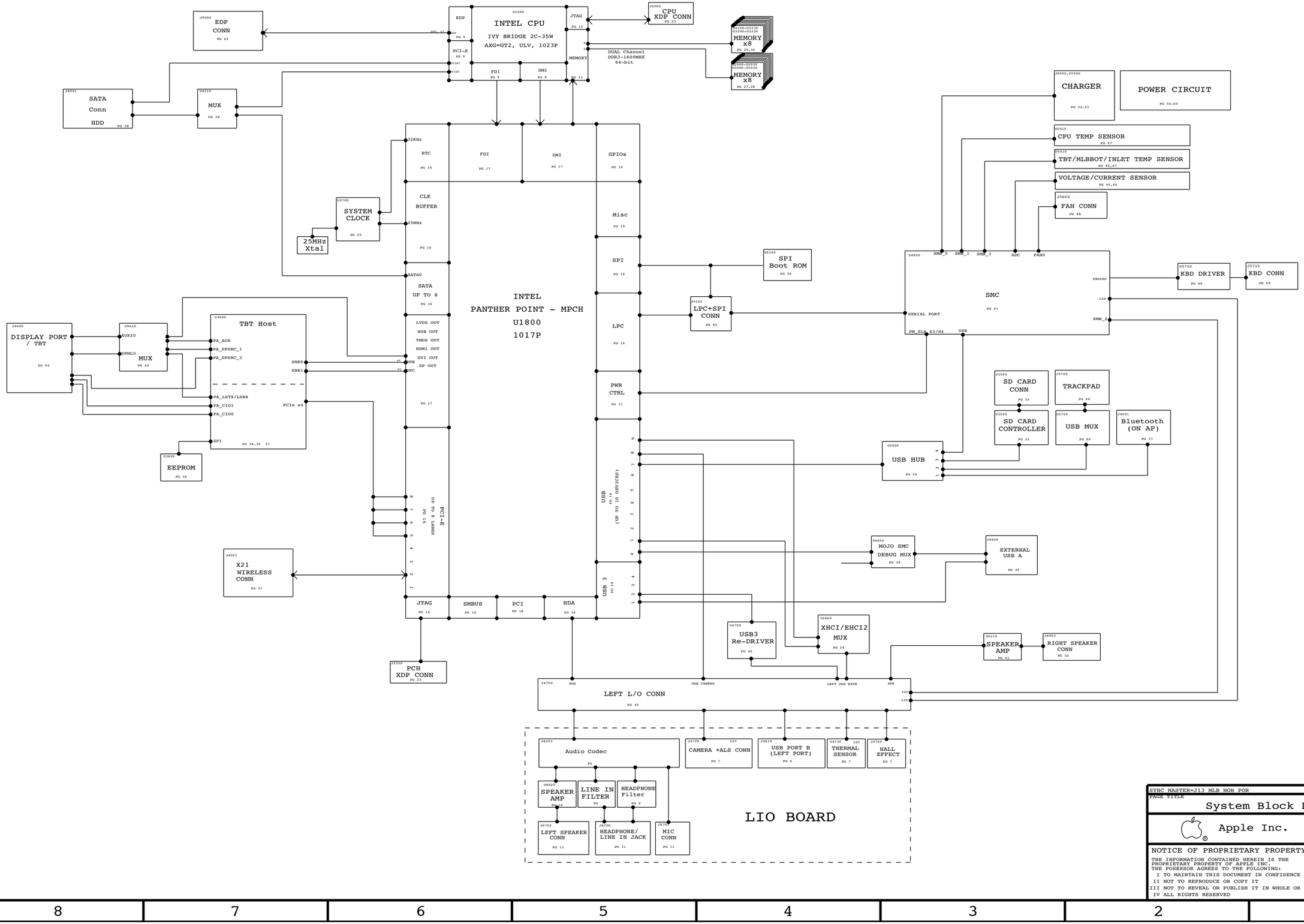

SYNC MASTER=J13 MLB NON POR | SYNC DATE=11/10/2011

PAGE TITLE

System Block Diagram

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DRAWING NUMBER 051-9277 | SIZE D

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PAGE 2 OF 109

SHEET 2 OF 73

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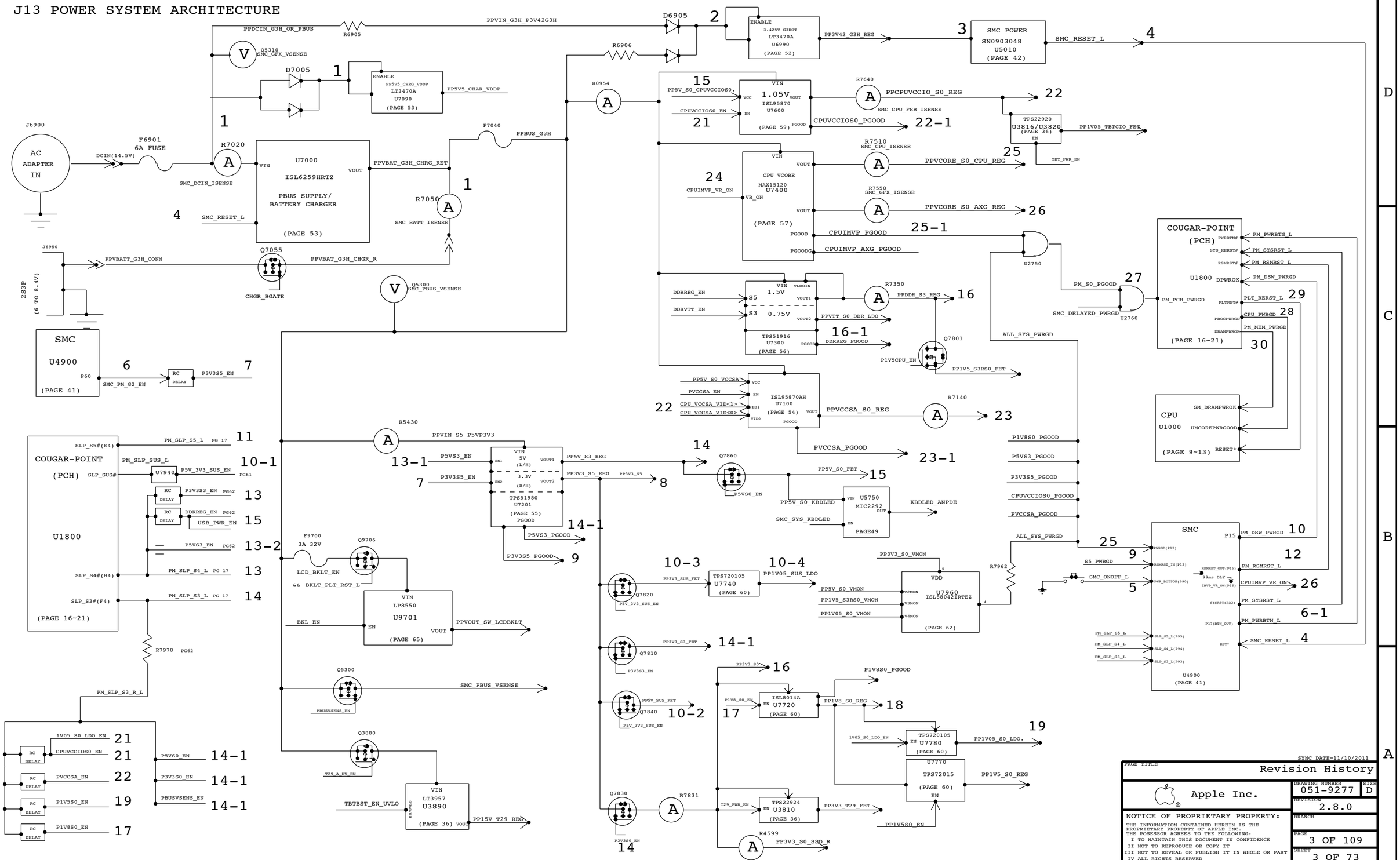
J13 POWER SYSTEM ARCHITECTURE



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PAGE TITLE: Revision History

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DRAWING NUMBER: 051-9277
SIZE: D
REVISION: 2.8.0
BRANCH:
PAGE: 3 OF 109
SHEET: 3 OF 73

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
085-3939	J13 MLB DEVELOPMENT BOM	J13_DEVEL:ENG
607-9090	CMN PTS,PCBA,MLB,J13	J13_COMMON
639-3552	PCBA,MLB,1.7GHZ,SA 4GB,J13	J13_CMNPTS,EEEE:DYRQ,CPU:1.7GHZ,DDR3:SAMSUNG_4GB
639-3553	PCBA,MLB,1.5GHZ,SA 4GB,J13	J13_CMNPTS,EEEE:DYRM,CPU:1.5GHZ,DDR3:SAMSUNG_4GB
639-3554	PCBA,MLB,1.5GHZ,HY 4GB,J13	J13_CMNPTS,EEEE:DYRN,CPU:1.5GHZ,DDR3:HYNIX_4GB
639-3555	PCBA,MLB,1.5GHZ,HY 8GB,J13	J13_CMNPTS,EEEE:DYRL,CPU:1.5GHZ,DDR3:HYNIX_8GB
639-3556	PCBA,MLB,1.7GHZ,HY 8GB,J13	J13_CMNPTS,EEEE:DYRK,CPU:1.7GHZ,DDR3:HYNIX_8GB
639-3557	PCBA,MLB,1.7GHZ,HY 4GB,J13	J13_CMNPTS,EEEE:DYRP,CPU:1.7GHZ,DDR3:HYNIX_4GB
639-3645	PCBA,MLB,1.5GHZ,EL 8GB,J13	J13_CMNPTS,EEEE:F0TC,CPU:1.5GHZ,DDR3:ELPIDA_8GB
639-3644	PCBA,MLB,1.7GHZ,EL 8GB,J13	J13_CMNPTS,EEEE:F0TD,CPU:1.7GHZ,DDR3:ELPIDA_8GB
639-3760	PCBA,MLB,1.8GHZ,SA 4GB,J13	J13_CMNPTS,EEEE:F25Q,CPU:1.8GHZ,DDR3:SAMSUNG_4GB
639-3761	PCBA,MLB,1.8GHZ,HY 8GB,J13	J13_CMNPTS,EEEE:F25T,CPU:1.8GHZ,DDR3:HYNIX_8GB
639-3762	PCBA,MLB,1.8GHZ,HY 4GB,J13	J13_CMNPTS,EEEE:F25V,CPU:1.8GHZ,DDR3:HYNIX_4GB
639-3763	PCBA,MLB,1.8GHZ,EL 8GB,J13	J13_CMNPTS,EEEE:F25P,CPU:1.8GHZ,DDR3:ELPIDA_8GB
639-3764	PCBA,MLB,2.0GHZ,SA 4GB,J13	J13_CMNPTS,EEEE:F25N,CPU:2.0GHZ,DDR3:SAMSUNG_4GB
639-3765	PCBA,MLB,2.0GHZ,HY 8GB,J13	J13_CMNPTS,EEEE:F25W,CPU:2.0GHZ,DDR3:HYNIX_8GB
639-3766	PCBA,MLB,2.0GHZ,HY 4GB,J13	J13_CMNPTS,EEEE:F25R,CPU:2.0GHZ,DDR3:HYNIX_4GB
639-3767	PCBA,MLB,2.0GHZ,EL 8GB,J13	J13_CMNPTS,EEEE:F25V,CPU:2.0GHZ,DDR3:ELPIDA_8GB
639-3790	PCBA,MLB,1.7GHZ,SA 8GB,J13	J13_CMNPTS,EEEE:F27V,CPU:1.7GHZ,DDR3:SAMSUNG_8GB
639-3791	PCBA,MLB,1.8GHZ,SA 8GB,J13	J13_CMNPTS,EEEE:F27Q,CPU:1.8GHZ,DDR3:SAMSUNG_8GB
639-3792	PCBA,MLB,2.0GHZ,SA 8GB,J13	J13_CMNPTS,EEEE:F27R,CPU:2.0GHZ,DDR3:SAMSUNG_8GB
639-3793	PCBA,MLB,1.7GHZ,EL 4GB,J13	J13_CMNPTS,EEEE:F27W,CPU:1.7GHZ,DDR3:ELPIDA_4GB
639-3794	PCBA,MLB,1.8GHZ,EL 4GB,J13	J13_CMNPTS,EEEE:F27Y,CPU:1.8GHZ,DDR3:ELPIDA_4GB
639-3795	PCBA,MLB,2.0GHZ,EL 4GB,J13	J13_CMNPTS,EEEE:F27T,CPU:2.0GHZ,DDR3:ELPIDA_4GB

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DYRK]	CRITICAL	EEEE:DYRK
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DYRL]	CRITICAL	EEEE:DYRL
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DYRM]	CRITICAL	EEEE:DYRM
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DYRN]	CRITICAL	EEEE:DYRN
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DYRP]	CRITICAL	EEEE:DYRP
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DYRQ]	CRITICAL	EEEE:DYRQ
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F0TC]	CRITICAL	EEEE:F0TC
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F0TD]	CRITICAL	EEEE:F0TD
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25N]	CRITICAL	EEEE:F25N
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25P]	CRITICAL	EEEE:F25P
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25Q]	CRITICAL	EEEE:F25Q
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25R]	CRITICAL	EEEE:F25R
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25T]	CRITICAL	EEEE:F25T
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25V]	CRITICAL	EEEE:F25V
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25W]	CRITICAL	EEEE:F25W
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25Y]	CRITICAL	EEEE:F25Y
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F27Q]	CRITICAL	EEEE:F27Q
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F27R]	CRITICAL	EEEE:F27R
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F27T]	CRITICAL	EEEE:F27T
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F27V]	CRITICAL	EEEE:F27V
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F27W]	CRITICAL	EEEE:F27W
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F27Y]	CRITICAL	EEEE:F27Y

Sub BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-3939	1	J13 MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM
607-9090	1	CMN PTS,PCBA,MLB,J13	CMNPTS	CRITICAL	J13_CMNPTS

SYNC MASTER=J30 MLB SYNC DATE=07/27/2011

PAGE TITLE

Revision History

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DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

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PAGE 4 OF 109

SHEET 4 OF 73

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J13 BOM GROUPS

BOM GROUP	BOM OPTIONS
J13_COMMON	ALTERNATE,COMMON,J13_MISC,J13_DEBUG:ENG,J13_PROGPARTS,USBHUB2514B,EDP:YES,PCH_C1
J13_MISC	CPUMEM_8LG:NO,HUB_3NONREM,TBT,MPM5:YES,PP5V5_DCIN:NO,TPAD_PCH:NO,SKIP_5V3V3:INAUDIBLE,BTPWR:84,TWTHV:P15V,LVDDR3_HW:YES,AXG_ACOUSTIC:NO
J13_PROGPARTS	BOOTROM_PROG,SMC_PROG,TBTROM:PROG
J13_DEVEL:ENG	ALTERNATE,BKLT:ENG,KDP_CONN,KDP_CPU:BPM,KDP_PCH,LPCPLUS,DDRVREF_DAC,VREFDQ:M1_M3,VREFCA:LDO_DAC,S0PGOOD_1SL,S3_S0_LED,VCCIOISNS_ENG,AIRPORTISNS_ENG,HDDISNS_ENG,LCDBKLTISNS_ENG
J13_DEVEL:PVT	LPCPLUS,KDP_CONN
J13_DEBUG:ENG	DEVEL_BOM,MOJO:YES,KDP
J13_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,MOJO:YES,KDP,KDP_CPU:BPM,VREFDQ:LDO,VREFCA:LDO,VCCIOISNS_PROD,AIRPORTISNS_PROD,HDDISNS_PROD,LCDBKLTISNS_PROD
J13_DEBUG:PROD	BKLT:PROD,MOJO:YES,KDP,KDP_CPU:BPM,VREFDQ:LDO,VREFCA:LDO,LPCPLUS,VCCIOISNS_PROD,AIRPORTISNS_PROD,HDDISNS_PROD,LCDBKLTISNS_PROD
DDR3:HYNIX_4GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:HYNIX_8GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:HYNIX_8GB
DDR3:SAMSUNG_4GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:SAMSUNG_8GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:SAMSUNG_8GB
DDR3:ELPIDA_8GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:ELPIDA_8GB
DDR3:ELPIDA_4GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:ELPIDA_4GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0865	1	IC,SERIAL SPI EEPROM,256KBIT,20MHZ,MLP8	U3690	CRITICAL	TBTROM:BLANK
34183475	1	IC,EEPROM,CR,V24.1,J11/J13	U3690	CRITICAL	TBTROM:PROG
338S1098	1	IC,SMC12-A3,40MHZ/50MIPS MCU,9X9,157BGA	U4900	CRITICAL	SMC_BLANK
338S1065	1	IC,SMC12,40MHZ/50MIPS MCU, 9X9,157BGA	U4900	CRITICAL	SMC_BLANK
34183433	1	IC,SMC,V2.1A43,Proto1B,J13	U4900	CRITICAL	SMC_PROG
335S0809	1	64 MBIT SPI SERIAL DUAL I/O FLASH,Macronix	U6100	CRITICAL	BOOTROM_BLANK
335S0803	1	64 MBIT SPI SERIAL DUAL I/O FLASH,Numonyx	U6100	CRITICAL	BOOTROM_BLANK
34183482	1	IC,EFI ROM,PROTO1B,J13 J11	U6100	CRITICAL	BOOTROM_PROG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
37680855	37680613		ALL	Diodes alt to Toshiba
37680977	37680859		ALL	Diodes alt to Toshiba
37680972	37680612		ALL	Rohm alt to Toshiba
13880676	13880691		ALL	Murata alt to Samsung
37180709	37180652		ALL	NXP alt to NXP
13880671	13880673		ALL	Taiyo alt to Murata
37680790	37680928		ALL	TI alt to Fairchild
15281462	15281295		ALL	Toko alt for NEC inductor
15281085	15281307		ALL	Toko alt for Cystec
13880703	13880648		ALL	Murata alt to Taiyo Yuden
13880684	13880660		ALL	Murata alt to Taiyo Yuden
15281493	15281300		ALL	Coilcraft alt to Murata
353S3238	353S1428		ALL	Intersil alt to OPA2333
37280186	37280185		ALL	NXP alt to Diodes
37681053	37680604		ALL	Diodes alt to Fairchild
37680855	37680613		ALL	Diodes alt to Toshiba
37680903	37680796		ALL	Fairchild alt to Siliconix
19780431	19780432		ALL	Epson alt to NDK
33784198	33784197		ALL	TDP 1.5GHZ alt to Nominal
33784236	33784196		ALL	TDP 1.7GHZ alt to Nominal
37180713	37180558		ALL	Diodes alt to ST Micro
12880333	998-4435		ALL	Sanyo alt to Kemet
12880357	998-4435		ALL	Sanyo alt to POS caps
998-4715	998-4435		ALL	Kemet_8sct alt to POS caps
998-4716	998-4435		ALL	Kemet_.0045 Flute alt to POS caps

DRAM CFG CHART

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 2
4GB	0
8GB	1

DIE REV	CFG 3
A	0
B	1

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4197	1	IVB,QBP8,ES2,K0,1.5,17W,2+2,0.95,4M,ULVB	U1000	CRITICAL	CPU:1.5GHZ
337S4299	1	IVB,QC55,Q8,L0,1.7,17W,2+2,1.0,3M,ULVBGA	U1000	CRITICAL	CPU:1.7GHZ
337S4298	1	IVB,QC54,Q8,L0,1.8,17W,2+2,1.1,3M,ULVBGA	U1000	CRITICAL	CPU:1.8GHZ
337S4296	1	IVB,QC52.Q8,L0,2.0,17W,2+2,1.1,4M,ULVBGA	U1000	CRITICAL	CPU:2.0GHZ
337S4198	1	IVB,QBP8,ES2,K0,1.5,17W,2+2,0.95,4M,ULVB	U1000	CRITICAL	CPU:1.5GHZTDP
337S4236	1	IVB,QMQF,ES2,K0,1.7,17W,2+2,1.0,4M,ULV,TDP	U1000	CRITICAL	CPU:1.7GHZTDP
337S4165	1	IC,PCH,PPT-MB,SFF,ES1	U1800	CRITICAL	PCH_ES1
337S4180	1	IC,PCH,PPT-MB,SFF,ES2,B0	U1800	CRITICAL	PCH_ES2
337S4235	1	IC,PCH,PPT-MB,SFF,P-QS,C0	U1800	CRITICAL	PCH_C0
337S4275	1	IC,PCH,PPT-MB,QS77,C1,QS	U1800	CRITICAL	PCH_C1
338S1047	1	IC,TBT,CR-4C,ES1,288 FCBGA,12X12MM	U3600	CRITICAL	TBT
333S0622	4	IC,SDRAM,2GBIT,256MX8,DDR3-1600,78P FPGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0622	4	IC,SDRAM,2GBIT,256MX8,DDR3-1600,78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0622	4	IC,SDRAM,2GBIT,256MX8,DDR3-1600,78P FGBA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0622	4	IC,SDRAM,2GBIT,256MX8,DDR3-1600,78P FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0625	4	IC,SDRAM,4GBIT,512MX8,DDR3-1600,82 FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0625	4	IC,SDRAM,4GBIT,512MX8,DDR3-1600,82 FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0625	4	IC,SDRAM,4GBIT,512MX8,DDR3-1600,82 FGBA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0625	4	IC,SDRAM,4GBIT,512MX8,DDR3-1600,82 FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0623	4	IC,SDRAM,2GBIT,DDR3-1600,78P FBGA,D-DIE	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0623	4	IC,SDRAM,2GBIT,DDR3-1600,78P FBGA,D-DIE	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0623	4	IC,SDRAM,2GBIT,DDR3-1600,78P FGBA,D-DIE	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0623	4	IC,SDRAM,2GBIT,DDR3-1600,78P FBGA,D-DIE	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0642	4	IC,SDRAM,4GBIT,DDR3-1600,78P FBGA,C-DIE	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0642	4	IC,SDRAM,4GBIT,DDR3-1600,78P FBGA,C-DIE	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0642	4	IC,SDRAM,4GBIT,DDR3-1600,78P FGBA,C-DIE	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0642	4	IC,SDRAM,4GBIT,DDR3-1600,78P FBGA,C-DIE	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0629	4	IC,SDRAM,4GBIT,DDR3L-1600,REV B,78P FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0629	4	IC,SDRAM,4GBIT,DDR3L-1600,REV B.78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0629	4	IC,SDRAM,4GBIT,DDR3L-1600,REV B,78P FGBA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0629	4	IC,SDRAM,4GBIT,DDR3L-1600,REV B,78P FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D,78P FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D.78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D,78P FGBA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D,78P FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_4GB
353S2929	1	IC,ISL6259,BATCHARGER,3%,4X4MM,QFN28	U7000	CRITICAL	
946-3115	1	MLB,DYMAX UV EB 0.22GRAM,K21	GLUE	CRITICAL	

PD Module Parts

806-3142	1	CAN,T29,J11/J13	TBTFENCE	CRITICAL	
806-3215	1	CAN,COVER,T29,J11/J13	TBTCOVER	CRITICAL	
806-3214	1	CAN,TOPSIDE,J11/J13	TBTTOPSIDE_1P	CRITICAL	
806-3706	1	CAN,TOPSIDE_2Piece_Cover,J11/J13	TBTTOPSIDE_2P_COVER	CRITICAL	
806-3705	1	CAN,TOPSIDE_2Piece_Fence,J11/J13	TBTTOPSIDE_2P_FENCE	CRITICAL	
806-3216	1	CAN,MDP,J11/J13	MDPCAN	CRITICAL	
806-3083	1	SHLD,USB,MLB,J11/J13	USBCAN	CRITICAL	
806-2377	1	K78, mDP Spring	MDPSPRING	CRITICAL	NOSTUFF

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PAGE TITLE
BOM Configuration

Apple Inc.

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SIZE D
REVISION 2.8.0
BRANCH
PAGE 5 OF 109
SHEET 5 OF 73

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Functional Test Points

J4001: AirPort / BT Connector

FUNC_TEST

TRUE	PP3V3_WLAN_F	37 42	(Need 5 TPs)
TRUE	WIFI_EVENT_L	37 41 42	
TRUE	PCIE_AP_R2D_N	37 69	
TRUE	PCIE_AP_R2D_P	37 69	
TRUE	PCIE_CLK100M_AP_N	16 37 69	
TRUE	PCIE_CLK100M_AP_P	16 37 69	
TRUE	USB_BT_CONN_P	37 68	
TRUE	USB_BT_CONN_N	37 68	
TRUE	PCIE_AP_D2R_P	16 37 69	
TRUE	PCIE_AP_D2R_N	16 37 69	
TRUE	PCIE_WAKE_L	17 37	
TRUE	AP_RESET_CONN_L	37	
TRUE	AP_CLKREQ_O_L	37	
TRUE	PP3V3_S3RS4_BT_F	37	

(Need to add 8 GND TPs)

J5715: KB BKLT CONNECTOR

FUNC_TEST

TRUE	KBDLED_FB	49	
TRUE	KBDLED_ANODE	49	

(Need to add 2 GND TP)

J4700: LIO Connector

FUNC_TEST

TRUE	=PP3V42_G3H_ONEWIRE	7 40	
TRUE	=PP3V3_S0_AUDIO	7 40	(Need 2 TPs)
TRUE	=PP3V3R1V5_S0_AUDIO	7 40	
TRUE	SYS_ONEWIRE	40 41	
TRUE	SMC_BC_ACOK	40 41 42	
TRUE	=USB_PWR_EN	39 40 62	
TRUE	SMC_LID	6 40 41 42 49	
TRUE	=I2C_LIO_SDA	40 44	
TRUE	=I2C_LIO_SCL	40 44	
TRUE	=I2C_MIKEY_SCL	40 44	
TRUE	=I2C_MIKEY_SDA	40 44	
TRUE	AUD_IPHS_SWITCH_EN	25 40	
TRUE	AUD_IP_PERIPHERAL_DET	18 40	
TRUE	AUD_I2C_INT_L	18 40	
TRUE	AUD_GPIO_3	40 51	
TRUE	SPKRAMP_INR_N	40 51 72	
TRUE	SPKRAMP_INR_P	40 51 72	
TRUE	USB_EXTB_N	24 40 68	
TRUE	USB_EXTB_P	24 40 68	
TRUE	USB3_EXTB_TX_C_N	40 68	
TRUE	USB3_EXTB_TX_C_P	40 68	
TRUE	USB3_EXTB_RX_RC_N	40 68	
TRUE	USB3_EXTB_RX_RC_P	40 68	
TRUE	USB_CAMERA_N	18 40 68	
TRUE	USB_CAMERA_P	18 40 68	
TRUE	HDA_SDOUT	16 40 69	
TRUE	HDA_BIT_CLK	16 40 69	
TRUE	HDA_SDIN0	16 40 69	
TRUE	USB_EXTB_OC_L		
TRUE	HDA_RST_L	16 40 69	
TRUE	HDA_SYNC	16 40 69	

(Need to add 5 GND TPs)

J4800: SD Card Connector

FUNC_TEST

TRUE	PP3V3_SW_SD_PWR	33
TRUE	SD_CLK	33
TRUE	SD_CMD	33
TRUE	SD_D<7..0>	33
TRUE	SD_CD_L	33
TRUE	SD_WP	33

(Need to add 2 GND TPs)

J5100: LPC+SPI Connector

FUNC_TEST

TRUE	=PP3V3_S5_LPCPLUS	7 43
TRUE	=PP5V_S0_LPCPLUS	7 43
TRUE	LPC_AD<3..0>	16 41 43 69
TRUE	SPI_ALT_MOSI	43
TRUE	SPI_ALT_MISO	43
TRUE	LPC_FRAME_L	16 41 43 69
TRUE	PM_CLKRUN_L	17 41 43
TRUE	SMC_TMS	41 42 43
TRUE	LPCPLUS_RESET_L	25 43 69
TRUE	SMC_TDO	41 42 43
TRUE	TP_SMC_TRST_L	43
TRUE	TP_SMC_MD1	43
TRUE	SMC_TX_L	41 42 43
TRUE	LPC_CLK33M_LPCPLUS	25 43 69
TRUE	SPIROM_USE_MLB	19 43 50
TRUE	SPI_ALT_CLK	43
TRUE	SPI_ALT_CS_L	43
TRUE	LPC_SERIRQ	16 41 43
TRUE	LPC_PWRDWN_L	17 25 41 43
TRUE	SMC_TDI	41 42 43
TRUE	SMC_TCK	41 42 43
TRUE	SMC_RESET_L	41 42 43 53
TRUE	SMC_ROMBOOT	42 43
TRUE	SMC_RX_L	41 42 43
TRUE	LPCPLUS_GPIO	19 43

(Need to add 6 GND TPs)

J5600: Fan Connector

FUNC_TEST

TRUE	=PP5V_S0_FAN	7 48	
TRUE	FAN_RT_TACH	48	
TRUE	FAN_RT_PWM	48	

(Need to add 1 GND TP)

J5700: IPD Flex Connector

FUNC_TEST

TRUE	PP3V3_TPAD_CONN	49	
TRUE	PP5V_TPAD_FILT	49	
TRUE	=PP3V42_G3H_TPAD	7 49	
TRUE	USB_TPAD_CONN_P	68	
TRUE	USB_TPAD_CONN_N	68	
TRUE	=I2C_TPAD_SDA	44 49	
TRUE	=I2C_TPAD_SCL	44 49	
TRUE	SMC_ONOFF_L	41 42 49	
TRUE	SMC_LID	6 40 41 42 49	
TRUE	SMC_TPAD_RST_L	42 49	
TRUE	SMC_PME_S4_WAKE_L	41 42 49	

(Need to add 5 GND TPs)

J6903: Speaker Connector

FUNC_TEST

TRUE	SPKRAMP_ROUT_P	51 52 72	
TRUE	SPKRAMP_ROUT_N	51 52 72	

(Need to add 3 GND TPs)

J6950: Battery Connector

FUNC_TEST

TRUE	PPVBAT_G3H_CONN	52 53	(Need 4 TPs)
TRUE	=SMBUS_BATT_SCL	44 52	
TRUE	=SMBUS_BATT_SDA	44 52	
TRUE	SYS_DETECT_L	52	

(Need to add 4 GND TPs near J6950 and 1 for shield)

J9000: Internal DP Connector

FUNC_TEST

TRUE	PPVOUT_SW_LCDBKLT	63 65	(Need 2 TPs)
TRUE	PP3V3_SW_LCD	63	(Need 2 TPs)
TRUE	I2C_TCON_SDA_R	63	
TRUE	I2C_TCON_SCL_R	63	
TRUE	LED_RETURN_6	63 65	
TRUE	LED_RETURN_5	63 65	
TRUE	LED_RETURN_4	63 65	
TRUE	LED_RETURN_3	63 65	
TRUE	LED_RETURN_2	63 65	
TRUE	LED_RETURN_1	63 65	
TRUE	DP_INT_HPD_CONN	63	
TRUE	DP_INT_AUX_CH_C_N	63 66	
TRUE	DP_INT_AUX_CH_C_P	63 66	
TRUE	DP_INT_ML_F_P<0>	63 66	
TRUE	DP_INT_ML_F_N<0>	63 66	
TRUE	DP_INT_ML_F_P<1>	66	
TRUE	DP_INT_ML_F_N<1>	66	

(Need to add 5 GND TPs)

Misc Voltages & Control Signals

FUNC_TEST

TRUE	PPBUS_G3H	7 52	
TRUE	PPVIN_SW_TBTBST	7 36	
TRUE	PPBUS_S5_HS_COMPUTING_ISNS	7	
TRUE	PPDCIN_G3H	7	
TRUE	PP3V42_G3H	7	
TRUE	PPVRTC_G3H	7	
TRUE	PP5V_S5	7	
TRUE	PP5V_SUS	7	
TRUE	PP3V3_S5	7 72	
TRUE	PP3V3_SUS	7	
TRUE	PP3V3_S3	7	
TRUE	PP1V8_S0	7	
TRUE	PP3V3_S0	7 72	
TRUE	PP1V5_S3	7 67	
TRUE	PP1V5_S3RS0	7 67	
TRUE	PP1V5_S0	7	
TRUE	PP1V05_S0	7	
TRUE	PPVTTDDR_S3	7	
TRUE	PP0V75_S0_DDRVTT	7	
TRUE	PPVCCSA_S0_CPU	7	
TRUE	PP1V05_SUS	7	
TRUE	PP15V_TBT	7	
TRUE	PP3V3_TBTLC	7	
TRUE	PP1V05_TBTLC	7 36	
TRUE	PP1V05_S0_PCH_VCCADPLL	7	
TRUE	PPVCORE_S0_CPU	7	
TRUE	PPVCORE_S0_AXG	7	
TRUE	PP1V5_S3_CPU_VCCDQ	7	
TRUE	PP1V05_S0_CPU_VCCPQE	7	
TRUE	PP1V8_S0_CPU_VCCPLL_R	7	
TRUE	PP1V05_TBTCIO	7	
TRUE	PPBUS_S5_HS_OTHER_ISNS	7	
TRUE	PPDCIN_G3H_ISOL	7	
TRUE	PP5V_S3	7	
TRUE	PP5V_S0	7	
TRUE	PP3V3_S4	7	

(Need to add 27 GND TPs)

J4501: SATA SSD Connector

FUNC_TEST

TRUE	PP3V3_S0_SSD_FLT	38	(Need 5 TPs)
TRUE	SATA_SSD_D2R_P	38 68	
TRUE	SATA_SSD_D2R_N	38 68	
TRUE	SMC_OOB1_RX_L	38 41	
TRUE	SMC_OOB1_TX_L	38 41 42	
TRUE	PCIE_CLK100M_SSD_P	16 38 66	
TRUE	PCIE_CLK100M_SSD_N	16 38 66	
TRUE	PCIE_SSD_R2D_P<1>	38 66	
TRUE	PCIE_SSD_R2D_N<1>	38 66	
TRUE	PCIE_SSD_D2R_P<1>	8 38 66	
TRUE	PCIE_SSD_D2R_N<1>	8 38 66	
TRUE	SATA_SSD_R2D_N	38 68	
TRUE	SATA_SSD_R2D_P	38 68	
TRUE	SSD_CLKREQ_L	16 38	
TRUE	SATA_PCIE_SEL	38	
TRUE	SSD_P3V3S0_EN	38	
TRUE	SSD_RESET_L	25 38	

(Need to add 6 GND TPs)

J6900: DC-In Connector

FUNC_TEST

TRUE	=PP18V5_DCIN_CONN	7 52	(Need 6 TPs)
TRUE	=PP5V_S3_LIO_CONN	7 52	

(Need to add 5 GND TPs)

NO_TEST Nets

POWER SIGNALS	TRUE	VCCSAS0_SREF	54
	TRUE	VCCSAS0_SET1_R	54
	TRUE	VCCSAS0_SET0	54
	TRUE	VCCSAS0_SET1	54

NO_TEST

17	TP_CRT_IG_BLUE	TRUE / MAKE_BASE=TRUE	NC_CRT_IG_BLUE	
17	TP_CRT_IG_GREEN	TRUE / MAKE_BASE=TRUE	NC_CRT_IG_GREEN	
17	TP_CRT_IG_RED	TRUE / MAKE_BASE=TRUE	NC_CRT_IG_RED	
17	TP_CRT_IG_DDC_CLK	TRUE / MAKE_BASE=TRUE	NC_CRT_IG_DDC_CLK	
17	TP_CRT_IG_DDC_DATA	TRUE / MAKE_BASE=TRUE	NC_CRT_IG_DDC_DATA	
17	TP_CRT_IG_HSYNC	TRUE / MAKE_BASE=TRUE	NC_CRT_IG_HSYNC	
17	TP_CRT_IG_VSYNC	TRUE / MAKE_BASE=TRUE	NC_CRT_IG_VSYNC	
	TP_LVDS_IG_CTRL_CLK	TRUE / MAKE_BASE=TRUE	NC_LVDS_IG_CTRL_CLK	
	TP_LVDS_IG_CTRL_DATA	TRUE / MAKE_BASE=TRUE	NC_LVDS_IG_CTRL_DATA	
	TP_PCH_LVDS_VBG	TRUE / MAKE_BASE=TRUE	NC_PCH_LVDS_VBG	
16	TP_HDA_SDIN1	TRUE / MAKE_BASE=TRUE	NC_HDA_SDIN1	
16	TP_HDA_SDIN2	TRUE / MAKE_BASE=TRUE	NC_HDA_SDIN2	
16	TP_HDA_SDIN3	TRUE / MAKE_BASE=TRUE	NC_HDA_SDIN3	
18	TP_PCI_PME_L	TRUE / MAKE_BASE=TRUE	NC_PCI_PME_L	
18	TP_PCI_CLK33M_OUT3	TRUE / MAKE_BASE=TRUE	NC_PCI_CLK33M_OUT3	
16	TP_CLINK_CLK	TRUE / MAKE_BASE=TRUE	NC_CLINK_CLK	
16	TP_CLINK_DATA	TRUE / MAKE_BASE=TRUE	NC_CLINK_DATA	
16	TP_CLINK_RESET_L	TRUE / MAKE_BASE=TRUE	NC_CLINK_RESET_L	
16	TP_PCIE_CLK100M_PEBN	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEBN	
16	TP_PCIE_CLK100M_PEBP	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEBP	

E53	TRUE	XDP_PCH_AP_PWR_EN	
E52	TRUE	XDP_PCH_USB_HUB_SOFT_RST_L	
E49	TRUE	XDP_PCH_SDCONN_STATE_RST_L	
E48	TRUE	XDP_PCH_ENET_PWR_EN	
E46	TRUE	XDP_PCH_SDCONN_DET_L	
E45	TRUE	XDP_PCH_S5_PWRGD	23
E43	TRUE	XDP_PCH_PWRBTN_L	23
E42	TRUE	XDP_PCH_ISOLATE_CPU_MEM_L	
E40	TRUE	XDP_FW_CLKREQ_L	
E39	TRUE	XDP_AP_CLKREQ_L	
E38	TRUE	XDP_PCH_AUD_IPHS_SWITCH_EN	

17	TP_SDVO_TVCLKINN	TRUE / MAKE_BASE=TRUE	NC_SDVO_TVCLKINN
17	TP_SDVO_TVCLKINP	TRUE / MAKE_BASE=TRUE	NC_SDVO_TVCLKINP
17	TP_SDVO_STALLN	TRUE / MAKE_BASE=TRUE	NC_SDVO_STALLN
17	TP_SDVO_STALLP	TRUE / MAKE_BASE=TRUE	NC_SDVO_STALLP
17	TP_SDVO_INTN	TRUE / MAKE_BASE=TRUE	NC_SDVO_INTN
17	TP_SDVO_INTP	TRUE / MAKE_BASE=TRUE	NC_SDVO_INTP

23	TP_XDP_PCH_OBSFN_A<0..1>	TRUE / MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_A<0..1>
23	TP_XDP_PCH_OBSFN_B<0..1>	TRUE / MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_B<0..1>
23	TP_XDPPCH_HOOK2	TRUE / MAKE_BASE=TRUE	NC_TP_XDPPCH_HOOK2
23	TP_XDPPCH_HOOK3	TRUE / MAKE_BASE=TRUE	NC_TP_XDPPCH_HOOK3
23	TP_XDP_PCH_OBSFN_D<0..1>	TRUE / MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_D<0..1>
23	TP_XDP_PCH_HOOK4	TRUE / MAKE_BASE=TRUE	NC_TP_XDP_PCH_HOOK4
23	TP_XDP_PCH_HOOK5	TRUE / MAKE_BASE=TRUE	NC_TP_XDP_PCH_HOOK5
16	TP_PCH_GPIO64_CLKOUTFLEX0	TRUE / MAKE_BASE=TRUE	NC_PCH_GPIO64_CLKOUTFLEX0
16	TP_PCH_GPIO65_CLKOUTFLEX1	TRUE / MAKE_BASE=TRUE	NC_PCH_GPIO65_CLKOUTFLEX1
16	TP_PCH_GPIO66_CLKOUTFLEX2	TRUE / MAKE_BASE=TRUE	NC_PCH_GPIO66_CLKOUTFLEX2
16	TP_PCH_GPIO67_CLKOUTFLEX3	TRUE / MAKE_BASE=TRUE	NC_PCH_GPIO67_CLKOUTFLEX3

	NC_EDP_TXP<0..3>	TRUE / MAKE_BASE=TRUE	TP_EDP_TX_P<0..3> 9
	NC_EDP_TXN<0..3>	TRUE / MAKE_BASE=TRUE	TP_EDP_TX_N<0..3> 9
	NC_EDP_AUXP	TRUE / MAKE_BASE=TRUE	TP_EDP_AUX_P
	NC_EDP_AUXN	TRUE / MAKE_BASE=TRUE	TP_EDP_AUX_N
	NC_CPU_THERMDA	TRUE / MAKE_BASE=TRUE	TP_CPU_THERMDA
	NC_CPU_THERMDC	TRUE / MAKE_BASE=TRUE	TP_CPU_THERMDC
	NC_CPU_RSVD<30..45>	TRUE / MAKE_BASE=TRUE	TP_CPU_RSVD<30..45>
	NC_CPU_RSVD<8..27>	TRUE / MAKE_BASE=TRUE	TP_CPU_RSVD<8..27>
	NC_PEG_R2D_CP<15..2>	TRUE / MAKE_BASE=TRUE	=PEG_R2D_C_P<15..2> 9
	NC_PEG_R2D_CN<15..2>	TRUE / MAKE_BASE=TRUE	=PEG_R2D_C_N<15..2> 9
	NC_PEG_D2RP<15..2>	TRUE / MAKE_BASE=TRUE	=PEG_D2R_P<15..2> 9
	NC_PEG_D2RN<15..2>	TRUE / MAKE_BASE=TRUE	=PEG_D2R_N<15..2> 9

16	TP_PCIE_CLK100M_PE4N	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE4N
16	TP_PCIE_CLK100M_PE4P	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE4P
	TP_PCIE_CLK100M_PE5N	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE5N
	TP_PCIE_CLK100M_PE5P	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE5P
	TP_PCIE_CLK100M_PE6N	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE6N
	TP_PCIE_CLK100M_PE6P	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE6P
	TP_PCIE_CLK100M_PE7N	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE7N
	TP_PCIE_CLK100M_PE7P	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE7P
	TP_PROC_P1_3	TRUE / MAKE_BASE=TRUE	NC_PROC_P1_3
	TP_SATA_B_D2RN	TRUE / MAKE_BASE=TRUE	NC_SATA_B_D2RN
	TP_SATA_B_D2RP	TRUE / MAKE_BASE=TRUE	NC_SATA_B_D2RP
	TP_SATA_B_R2D_CN	TRUE / MAKE_BASE=TRUE	NC_SATA_B_R2D_CN
	TP_SATA_B_R2D_CP	TRUE / MAKE_BASE=TRUE	NC_SATA_B_R2D_CP
16	TP_SATA_D_D2RN	TRUE / MAKE_BASE=TRUE	NC_SATA_D_D2RN
16	TP_SATA_D_D2RP	TRUE / MAKE_BASE=TRUE	NC_SATA_D_D2RP
16	TP_SATA_D_R2D_CN	TRUE / MAKE_BASE=TRUE	NC_SATA_D_R2D_CN
16	TP_SATA_D_R2D_CP	TRUE / MAKE_BASE=TRUE	NC_SATA_D_R2D_CP
16	TP_SATA_E_D2RN	TRUE / MAKE_BASE=TRUE	NC_SATA_E_D2RN
16	TP_SATA_E_D2RP	TRUE / MAKE_BASE=TRUE	NC_SATA_E_D2RP
16	TP_SATA_E_R2D_CN	TRUE / MAKE_BASE=TRUE	NC_SATA_E_R2D_CN
16	TP_SATA_E_R2D_CP	TRUE / MAKE_BASE=TRUE	NC_SATA_E_R2D_CP
16	TP_SATA_F_D2RN	TRUE / MAKE_BASE=TRUE	NC_SATA_F_D2RN
16	TP_SATA_F_D2RP	TRUE / MAKE_BASE=TRUE	NC_SATA_F_D2RP
16	TP_SATA_F_R2D_CN	TRUE / MAKE_BASE=TRUE	NC_SATA_F_R2D_CN
16	TP_SATA_F_R2D_CP	TRUE / MAKE_BASE=TRUE	NC_SATA_F_R2D_CP

	TP_PCH_TP18	TRUE / MAKE_BASE=TRUE	NC_PCH_TP18
	TP_PCH_TP17	TRUE / MAKE_BASE=TRUE	NC_PCH_TP17
	TP_PCH_TP16	TRUE / MAKE_BASE=TRUE	NC_PCH_TP16
	TP_PCH_TP15	TRUE / MAKE_BASE=TRUE	NC_PCH_TP15
	TP_PCH_TP14	TRUE / MAKE_BASE=TRUE	NC_PCH_TP14
	TP_PCH_TP13	TRUE / MAKE_BASE=TRUE	NC_PCH_TP13
	TP_PCH_TP12	TRUE / MAKE_BASE=TRUE	NC_PCH_TP12
	TP_PCH_TP10	TRUE / MAKE_BASE=TRUE	NC_PCH_TP10
	TP_PCH_TP9	TRUE / MAKE_BASE=TRUE	NC_PCH_TP9
	TP_PCH_TP8	TRUE / MAKE_BASE=TRUE	NC_PCH_TP8
	TP_PCH_TP7	TRUE / MAKE_BASE=TRUE	NC_PCH_TP7
	TP_PCH_TP6	TRUE / MAKE_BASE=TRUE	NC_PCH_TP6
	TP_PCH_TP5	TRUE / MAKE_BASE=TRUE	NC_PCH_TP5
	TP_PCH_TP4	TRUE / MAKE_BASE=TRUE	NC_PCH_TP4
	TP_PCH_TP3	TRUE / MAKE_BASE=TRUE	NC_PCH_TP3
	TP_PCH_TP2	TRUE / MAKE_BASE=TRUE	NC_PCH_TP2
	TP_PCH_TP1	TRUE / MAKE_BASE=TRUE	NC_PCH_TP1

E56	PCH_VSS_NCTF<1>	TRUE	PCH_VSS_NCTF<15>
E57	PCH_VSS_NCTF<2>	TRUE	PCH_VSS_NCTF<17>
E54	PCH_VSS_NCTF<5>	TRUE	PCH_VSS_NCTF<19> 6
		TRUE	PCH_VSS_NCTF<19> 6
E57	PCH_VSS_NCTF<9>	TRUE	PCH_VSS_NCTF<21>
E57	PCH_VSS_NCTF<11>	TRUE	PCH_VSS_NCTF<25>
E56	PCH_VSS_NCTF<12>	TRUE	PCH_VSS_NCTF<27>
		TRUE	PCH_VSS_NCTF<29>

8	TP_LVDS_IG_B_CLKN	TRUE / MAKE_BASE=TRUE	NC_LVDS_IG_B_CLKN
8	TP_LVDS_IG_B_CLKP	TRUE / MAKE_BASE=TRUE	NC_LVDS_IG_B_CLKP
	TP_LVDS_IG_BKL_PWM	TRUE / MAKE_BASE=TRUE	NC_LVDS_IG_BKL_PWM
	SMC_BS_ALRT_L	TRUE / MAKE_BASE=TRUE	NC_SMC_BS_ALRT_L

SYNC MASTER=K21_MLB SYNC DATE=07/29/2013

PAGE TITLE

Functional Test / No Test

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

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PAGE 7 OF 109

SHEET 6 OF 73

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"G3Hot" (Always-Present) Rails

=PPBUS_G3H → PPBUS_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.4V
MAKE_BASE=TRUE
- =PPBUS_S0_LCDBKLT
- =PPBUS_S0_VSENSE
- =PPVIN_SW_TBTBST
- =PPVIN_S5_HS_COMPUTING_ISNS_R
- =PPVIN_S5_HS_OTHER_ISNS_R

PPVIN_SW_TBTBST (VOLTAGE=12.8V)

=PPVIN_S5_HS_OTHER_ISNS → PPBUS_S5_HS_OTHER_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.4V
MAKE_BASE=TRUE
- =PPVIN_S5_P5VP3V3

=PPVIN_S5_HS_COMPUTING_ISNS → PPBUS_S5_HS_COMPUTING_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.4V
MAKE_BASE=TRUE
- =PPVIN_S0_CPUIMVP
- =PPVIN_S3_DDRREG
- =PPVIN_S0_CPUVCCIOS0
- =PPVIN_S0_VCCSAS0
- =PPVIN_S0_CPUAXG

=PP18V5_DCIN_CONN → PPDCIN_G3H
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE
- =PPDCIN_S5_CHGR

=PP18V5_DCIN_ISOL → PPDCIN_G3H_ISOL
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE
- =PPDCIN_S5_CHGR_ISOL
- =PPDCIN_S5_VSENSE

=PP3V42_G3H_REG → PP3V42_G3H
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.42V
MAKE_BASE=TRUE
- =PP3V3_S5_LPCPLUS
- =PP3V3_S5_SMC
- =PP3V42_G3H_CHGR
- =PP3V42_G3H_PWRCTL
- =PP3V42_G3H_SMBUS_SMC_BSA
- =PP3V42_G3H_SMCUSBMUX
- =PP3V42_G3H_TPAD
- =PPVIN_S5_SMCVREF
- =PPVBAT_G3H_SYSCLK
- =PP3V42_G3H_ONEWIRE

=PPVRTC_G3_OUT → PPVRTC_G3H
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3V
MAKE_BASE=TRUE
- =PPVRTC_G3_PCH

5V Rails

=PP5V_S5_LDO → PP5V_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S5_P1V5DDRFET
- =PP5V_S5_P5VSUSFET
- =PP5V_S5_TPAD

=PP5V_SUS_FET → PP5V_SUS
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_SUS_PCH

=PP5V_S3_REG → PP5V_S3
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S3_AUDIO_AMP
- =PP5V_S3_DDRREG
- =PP5V_S3_MEMRESET
- =PP5V_S3_P5VS0FET
- =PP5V_S3_RTUSB
- =PP5V_S3_LIO_CONN

=PP5V_S0_FET → PP5V_S0
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S0_BKL
- =PP5V_S0_CPUIMVP
- =PP5V_S0_CPUVCCIOS0
- =PP5V_S0_FAN
- =PP5V_S0_LPCPLUS
- =PP5V_S0_VCCSA
- =PP5V_S0_PCH
- =PP5V_S0_VMON
- =PP5V_S0_KBDLED

3.3V Rails

=PP3V3_S5_REG → PP3V3_S5
MIN_LINE_WIDTH=0.6 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
- =PP3V3_S5_XDP
- =PP3V3_S0_P3V3S0FET
- =PP3V3_S3_P3V3S3FET
- =PP3V3_S5_CPU_VCCDDR
- =PP3V3_S5_PCH
- =PP3V3_S5_PCHPWRGD
- =PP3V3_S5_SMCBATLOW
- =PP3V3_S5_PCH_VCCDSW
- =PP3V3_S5_SYSCLK
- =PP3V3_S5_VMON
- =PP3V3_S5_PWRCTL
- =PP3V3_S4_TBTAPWRSW
- =PP3V3_S5_P3V3SUSFET
- =PP3V3_S4_P3V3S4FET
- =PP3V3_S5_PCH_GPIO

=PP3V3_S4_FET → PP3V3_S4
MIN_LINE_WIDTH=0.6 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
- =PP3V3_S4_SD_HPD
- =PP3V3_S4_SMC
- =PP3V3_S4_TPAD
- =PP3V3_S4_BT

=PP3V3_SUS_FET → PP3V3_SUS
MIN_LINE_WIDTH=0.50MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_SUS_PCH_VCCSUS
- =PP3V3_SUS_GPIO
- =PP3V3_SUS_PCH
- =PP3V3_SUS_PWRCTL
- =PP3V3_SUS_P1V05SUSLDO
- =PP3V3_SUS_SMC
- =PP3V3_SUS_PCH_VCC_SPI
- =PP3V3_SUS_PCH_GPIO
- =PP3V3_SUS_ROM
- =PP3V3_SUS_PCH_VCCSUS_USB

=PP3V3_S4_TBTAPWR → PP3V3_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20 MM MAKE_BASE=TRUE
- =PP3V3_S4_TBT

=PP3V3_S3_FET → PP3V3_S3
MIN_LINE_WIDTH=0.50MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_S3_BT
- =PP3V3_S3_CARDREADER
- =PP3V3_S3_MEMRESET
- =PP3V3_S3_SMBUS_SMC_A_S3
- =PP3V3_S3_SMBUS_SMC_MGMT
- =PP3V3_S3_USB_HUB
- =PP3V3_S3_USB_RESET
- =PP3V3_S3_VREFMRGN
- =PP3V3_S3_WLAN
- =PP3V3_S3_WLANISNS
- =PP3V3_S3_BMON_ISNS
- =PP3V3_S3_PCH_GPIO
- =PP3V3_S3_1V5S3ISNS
- =PP3V3_S3_DBGLEDS
- =PP3V3_S3_USBMUX
- =PP3V3_S3_LCD

=PP3V3_S0_FET → PP3V3_S0
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_S0_CPUVCCIOISNS
- =PP3V3_S0_AUDIO
- =PP3V3_S0_BKL_VDDIO
- =PP3V3_S0_HS_COMPUTING_ISNS
- =PP3V3_S0_CPUTHMSNS
- =PP3V3_S0_DP_DDC
- =PP3V3_S0_FAN
- =PP3V3_S0_P3V3TBTFET
- =PP3V3_S0_P1V8S0
- =PP3V3_S0_PCH
- =PP3V3_S0_PCH_GPIO
- =PP3V3_S0_HS_OTHER_ISNS
- =PP3V3_S0_PCH_VCC3_3
- =PP3V3_S0_PCH_VCCADAC
- =PP3V3_S0_PWRCTL
- =PP3V3_S0_RSTBUF
- =PP3V3_S0_SB_PM
- =PP3V3_S0_SMBUS_PCH
- =PP3V3_S0_SMBUS_SMC_0_S0
- =PP3V3_S0_SMBUS_SMC_B_S0
- =PP3V3_S0_SMC
- =PP3V3_S0_SSD
- =PP3V3_S0_HDDISNS
- =PP3V3_S0_VMON
- =PP3V3_S0_P1V5S0
- =PP3V3_S0_TBTPWRCTL
- =PP3V3_S0_P1V05S0LDO
- =PP3V3_S0_IMVPISNS
- =PP3V3_S0_XDP
- =PP3V3_S0_BKLTISNS
- =PP3V3_S0_SYSCLKGEN
- =PP3V3_S0_SATAMUX
- =PP3V3_S0_SAISNS
- =PP3V3_S0_3V3S0ISNS
- =PP3V3_S0_CPU_VCCIO_SEL
- =PP3V3_S0_PCH_VCC3_3_CLK
- =PP3V3_S0_PCH_STRAPS

1.8V/1.5V/1.2V/1.05V Rails

=PP1V8_S0_REG → PP1V8_S0
2A max supply
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
- =PP1V8_S0_CPU_VCCPLL
- =PP1V8_S0_PCH_VCC_DFTERM
- =PP1V8_S0_P1V05S0LDO
- =PP1V8R1V5_S0_PCH_VCCVRM
- =PPVDDIO_S0_SBCLK
- =PP1V8_S0_P1V5S0

=PPDDR_S3_REG → PP1V5_S3
MIN_LINE_WIDTH=0.8 MM
MIN_NECK_WIDTH=0.1 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
- =PP1V5_S3_MEMRESET
- =PP1V5_S3_MEM_A
- =PP1V5_S3_MEM_B
- =PP1V5_S3_P1V5S3RS0_FET
- =PPVIN_S0_DDRREG_LDO
- =PPDDR_S3_MEMVREF

=PP1V5_S3RS0_FET → PP1V5_S3RS0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
- =PP1V5_S3_CPU_VCCDDR
- =PP1V5_S3RS0_VMON

=PP1V5_S0_REG → PP1V5_S0
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
- =PP3V3R1V5_S0_AUDIO
- =PP3V3R1V5_S0_PCH_VCCSUSHDA

=PPVTT_S3_DDR_BUF → PPVTTDDR_S3
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE

=PPVTT_S0_DDR_LDO → PP0V75_S0_DDRVTT
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE
- =PP0V75_S0_MEM_VTT_A
- =PP0V75_S0_MEM_VTT_B
- =PPVTT_S0_VTTCLAMP

=PPVCCSA_S0_REG → PPVCCSA_S0_CPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.9V
MAKE_BASE=TRUE
- =PPVCCSA_S0_CPU
- =PPVCCSA_S0_VSENSE

=PP1V05_SUS_LDO → PP1V05_SUS
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_SUS_PCH_JTAG

=PPCPUVCCIO_S0_REG → PP1V05_S0
? mA
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_S0_CPU_VCCIO
- =PP1V05_S0_PCH
- =PP1V05_S0_PCH_VCCIO
- =PP1V05_S0_PCH_VCCIO_PCIE
- =PP1V05_S0_PCH_VCCIO_SATA
- =PP1V05_S0_PCH_VCCASW
- =PP1V05_S0_PCH_VCC_CORE
- =PP1V05_S0_VMON
- =PPVCCIO_S0_CPUIMVP
- =PP1V05_S0_PCH_VCCDIFFCLK
- =PP1V05_S0_PCH_VCCSSC
- =PP1V05_S0_PCH_V_PROC_IO
- =PP1V05_S0_PCH_VCC_DMI
- =PPVCCIO_S0_XDP
- =PPVCCIO_S0_SMC
- =PP1V05_S0_P1V05TBTFET

TBT Rails (off when no cable)

=PP15V_TBT_REG → PP15V_TBT
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=17.6V
MAKE_BASE=TRUE
- =PPHV_SW_DPAPWRSW
- =PPHV_SW_TBTAPWRSW

=PP3V3_TBTLC_FET → PP3V3_TBTLC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PPVDDIO_TBT_CLK
- =PP3V3_TBTLC_RTR
- =PP3V3_TBT_PCH_GPIO

=PP1V05_TBTLC_FET → PP1V05_TBTLC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_TBTLC_RTR

=PP1V05_TBTCIO_FET → PP1V05_TBTCIO
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_TBTCIO_RTR

1V05 S0 LDO

=PP1V05_S0_LDO → PP1V05_S0_PCH_VCCADPLL
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_S0_PCH_VCCADPLL

Chipset "VCore" Rails

=PPVCORE_S0_CPU_REG → PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE
- =PPVCORE_S0_CPU
- =PPCPUVCORE_S0_VSENSE

=PPVCORE_S0_AXG_REG → PPVCORE_S0_AXG
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PPVCORE_S0_CPU_VCCAXG
- =PPGFXVCORE_S0_VSENSE

=PP1V5_S3_CPU_VCCDQ → PP1V5_S3_CPU_VCCDQ
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE

=PP1V05_S0_CPU_VCCPQE → PP1V05_S0_CPU_VCCPQE
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

=PP1V8_S0_CPU_VCCPLL_R → PP1V8_S0_CPU_VCCPLL_R
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE

SYNC MASTER=K21 MLB SYNC DATE=07/29/2011

PAGE TITLE: Power Aliases

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DRAWING NUMBER 051-9277 SIZE D
REVISION 2.8.0
BRANCH
PAGE 8 OF 109
SHEET 7 OF 73

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Plated Board Slot

SL0900
TH-NSP
SL-2.3X3.9-2.9X4.5

CPU Heat Sink Mounting Bosses

Z0913 STDOFF-4.5OD1.8H-SM
Z0910 STDOFF-4.5OD1.8H-SM
Z0911 STDOFF-4.5OD1.8H-SM
Z0912 STDOFF-4.5OD1.8H-SM
4x 860-1327

Fan Boss

Z0905 STDOFF-4.5OD1.8H-SM
860-1327

X21 Boss

Z0914 STDOFF-4.5OD1.9H-SM
860-1327

SSD Boss

Z0915 STDOFF-4.5OD1.9H-SM
860-1327

EMI I/O Pogo Pins

DisplayPort Pogo

CRITICAL
ZS0905
POGO-2.0OD-3.6H-K86-K87
870-1938

USB/SD Card Pogo

CRITICAL
ZS0906
POGO-2.0OD-3.6H-K86-K87
870-1938

Digital Ground

GND
VOLTAGE=0V
MIN_NECK_WIDTH=0.075MM
MIN_LINE_WIDTH=0.6MM

Can Slots

SL0901 TH-NSP SL-1.1X0.4-1.4X0.7
SL0902 TH-NSP SL-1.1X0.4-1.4X0.7
2x TBT pin diodes
SL0903 TH-NSP SL-1.1X0.4-1.4X0.7
SL0906 TH-NSP SL-1.1X0.4-1.4X0.7
2x MDP Connector
SL0905 TH-NSP SL-1.1X0.45-1.4X0.75
SL0907 TH-NSP SL-1.1X0.45-1.4X0.75
2x TBT chip
SL0904 TH-NSP SL-1.1X0.4-1.4X0.7
SL0908 TH-NSP SL-1.1X0.4-1.4X0.7
2x USB Connector

Unused PPT

PCIE_CLK100M_ENET_N	NC_PCIE_CLK100M_ENET_N	MAKE_BASE=TRUE	NO_TEST=TRUE
PCIE_CLK100M_ENET_P	NC_PCIE_CLK100M_ENET_P	MAKE_BASE=TRUE	NO_TEST=TRUE
PCIE_CLK100M_FW_N	NC_PCIE_CLK100M_FW_N	MAKE_BASE=TRUE	NO_TEST=TRUE
PCIE_CLK100M_FW_P	NC_PCIE_CLK100M_FW_P	MAKE_BASE=TRUE	NO_TEST=TRUE
PCIE_CLK100M_EXCARD_N	NC_PCIE_CLK100M_EXCARD_N	MAKE_BASE=TRUE	NO_TEST=TRUE
PCIE_CLK100M_EXCARD_P	NC_PCIE_CLK100M_EXCARD_P	MAKE_BASE=TRUE	NO_TEST=TRUE
PEG_CLK100M_N	NC_PEG_CLK100M_N	MAKE_BASE=TRUE	NO_TEST=TRUE
PEG_CLK100M_P	NC_PEG_CLK100M_P	MAKE_BASE=TRUE	NO_TEST=TRUE
PCIE_ENET_D2R_N	NC_PCIE_ENET_D2R_N	MAKE_BASE=TRUE	NO_TEST=TRUE
PCIE_ENET_D2R_P	NC_PCIE_ENET_D2R_P	MAKE_BASE=TRUE	NO_TEST=TRUE
PCIE_ENET_R2D_C_N	NC_PCIE_ENET_R2D_C_N	MAKE_BASE=TRUE	NO_TEST=TRUE
PCIE_ENET_R2D_C_P	NC_PCIE_ENET_R2D_C_P	MAKE_BASE=TRUE	NO_TEST=TRUE
PCIE_FW_D2R_N	NC_PCIE_FW_D2R_N	MAKE_BASE=TRUE	NO_TEST=TRUE
PCIE_FW_D2R_P	NC_PCIE_FW_D2R_P	MAKE_BASE=TRUE	NO_TEST=TRUE
PCIE_FW_R2D_C_N	NC_PCIE_FW_R2D_C_N	MAKE_BASE=TRUE	NO_TEST=TRUE
PCIE_FW_R2D_C_P	NC_PCIE_FW_R2D_C_P	MAKE_BASE=TRUE	NO_TEST=TRUE
PCIE_EXCARD_D2R_N	NC_PCIE_EXCARD_D2R_N	MAKE_BASE=TRUE	NO_TEST=TRUE
PCIE_EXCARD_D2R_P	NC_PCIE_EXCARD_D2R_P	MAKE_BASE=TRUE	NO_TEST=TRUE
PCIE_EXCARD_R2D_C_N	NC_PCIE_EXCARD_R2D_C_N	MAKE_BASE=TRUE	NO_TEST=TRUE
PCIE_EXCARD_R2D_C_P	NC_PCIE_EXCARD_R2D_C_P	MAKE_BASE=TRUE	NO_TEST=TRUE

MEM_A_CLK_P<1>	TP_MEM_A_CLKP<1>	MAKE_BASE=TRUE
MEM_A_CLK_N<1>	TP_MEM_A_CLKN<1>	MAKE_BASE=TRUE
MEM_B_CLK_P<1>	TP_MEM_B_CLKP<1>	MAKE_BASE=TRUE
MEM_B_CLK_N<1>	TP_MEM_B_CLKN<1>	MAKE_BASE=TRUE

ENET_LOW_PWR_PCH	XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH	MAKE_BASE=TRUE
SATARDRVR_EN	XDP_DC3_PCH_GPIO19_SATARDRVR_EN	MAKE_BASE=TRUE
TP_PCH_CLKOUT_DPN	DPLL_REF_CLK_N	MAKE_BASE=TRUE
TP_PCH_CLKOUT_DPP	DPLL_REF_CLK_P	MAKE_BASE=TRUE

DPLL_REF_CLKN
DPLL_REF_CLKP

Unused USB

USB_EXTC_P	NC_USB_EXTC_P	MAKE_BASE=TRUE	NO_TEST=TRUE
USB_EXTC_N	NC_USB_EXTC_N	MAKE_BASE=TRUE	NO_TEST=TRUE
USB3_EXTC_RX_P	NC_USB3_EXTC_RX_P	MAKE_BASE=TRUE	NO_TEST=TRUE
USB3_EXTC_RX_N	NC_USB3_EXTC_RX_N	MAKE_BASE=TRUE	NO_TEST=TRUE
USB3_EXTC_TX_P	NC_USB3_EXTC_TX_P	MAKE_BASE=TRUE	NO_TEST=TRUE
USB3_EXTC_TX_N	NC_USB3_EXTC_TX_N	MAKE_BASE=TRUE	NO_TEST=TRUE
USB3_EXTD_RX_P	NC_USB3_EXTD_RX_P	MAKE_BASE=TRUE	NO_TEST=TRUE
USB3_EXTD_RX_N	NC_USB3_EXTD_RX_N	MAKE_BASE=TRUE	NO_TEST=TRUE
USB3_EXTD_TX_P	NC_USB3_EXTD_TX_P	MAKE_BASE=TRUE	NO_TEST=TRUE
USB3_EXTD_TX_N	NC_USB3_EXTD_TX_N	MAKE_BASE=TRUE	NO_TEST=TRUE
USB_EXTD_EHCI_N	NC_USB_EXTD_EHCI_N	MAKE_BASE=TRUE	NO_TEST=TRUE
USB_EXTD_EHCI_P	NC_USB_EXTD_EHCI_P	MAKE_BASE=TRUE	NO_TEST=TRUE

Unused PGOOD signal

TP_P1V5S3RS0_RAMP_DONE	P1V5S3RS0_RAMP_DONE	MAKE_BASE=TRUE
TP_DDRREG_PGOOD	DDRREG_PGOOD	MAKE_BASE=TRUE

SATA Aliases

Unused SATA ODD Signals

SATA_ODD_R2D_C_P	NC_SATA_ODD_R2DCP	MAKE_BASE=TRUE	NO_TEST=TRUE
SATA_ODD_R2D_C_N	NC_SATA_ODD_R2DCN	MAKE_BASE=TRUE	NO_TEST=TRUE
SATA_ODD_D2R_P	NC_SATA_ODD_D2RP	MAKE_BASE=TRUE	NO_TEST=TRUE
SATA_ODD_D2R_N	NC_SATA_ODD_D2RN	MAKE_BASE=TRUE	NO_TEST=TRUE

SSD PCIE Signals

=PEG_D2R_P<1..0>	PCIE_SSD_D2R_P<1..0>	MAKE_BASE=TRUE	6 38 66
=PEG_D2R_N<1..0>	PCIE_SSD_D2R_N<1..0>	MAKE_BASE=TRUE	6 38 66
=PEG_R2D_C_P<1..0>	PCIE_SSD_R2D_C_P<1..0>	MAKE_BASE=TRUE	38 66
=PEG_R2D_C_N<1..0>	PCIE_SSD_R2D_C_N<1..0>	MAKE_BASE=TRUE	38 66

CPU signals

MEMVTT_EN — =DDRVTT_EN (MAKE_BASE=TRUE)

=PP3V3_S0_DP_DDC

R0920 2.2K 5% 1/20W MF 201
R0921 2.2K 5% 1/20W MF 201
NO STUFF
R0922 2.2K 5% 1/20W MF 201
NO STUFF
R0923 2.2K 5% 1/20W MF 201

TP_DP_IG_C_CTRL_CLK	DPB_IG_DDC_CLK	MAKE_BASE=TRUE
TP_DP_IG_C_CTRL_DATA	DPB_IG_DDC_DATA	MAKE_BASE=TRUE
TP_DP_IG_D_CTRL_CLK	DP_IG_D_CTRL_CLK	MAKE_BASE=TRUE
TP_DP_IG_D_CTRL_DATA	DP_IG_D_CTRL_DATA	MAKE_BASE=TRUE

=PP3V3_S0_DP_DDC

R0924 470K 1% 1/20W MF 201
R0925 470K 1% 1/20W MF 201

DP_TBTSNK0_DDC_CLK	DPA_IG_DDC_CLK	MAKE_BASE=TRUE
DP_TBTSNK0_DDC_DATA	DPA_IG_DDC_DATA	MAKE_BASE=TRUE

CRITICAL
R0910 0.01 0.5% 1W MF 0612-1

PPBUS_SW_LCDBKLT_PWR — PPBUS_SW_BKL (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.375 MM, VOLTAGE=12.6V, MAKE_BASE=TRUE)
ISNS_LCDBKLT_P
ISNS_LCDBKLT_N
=PPBUS_SW_BKL

CRITICAL
R0954 0.002 1% 1W MF 0612

=PPVIN_S5_HS_COMPUTING_ISNS — =PPVIN_S5_HS_COMPUTING_ISNS_R
ISNS_HS_COMPUTING_N
ISNS_HS_COMPUTING_P

MLB_RAMCFG3
MLB_RAMCFG2
MLB_RAMCFG1
MLB_RAMCFG0

RAMCFG3:L R0950 10K 5% 1/20W MF 201
RAMCFG2:L R0951 10K 5% 1/20W MF 201
RAMCFG1:L R0952 10K 5% 1/20W MF 201
RAMCFG0:L R0953 10K 5% 1/20W MF 201

LVDS Aliases

TP_LVDS_IG_B_CLKP	LVDS_IG_B_CLK_P	MAKE_BASE=TRUE
TP_LVDS_IG_B_CLKN	LVDS_IG_B_CLK_N	MAKE_BASE=TRUE
NC_LVDS_IG_B_DATAP<0..3>	LVDS_IG_B_DATA_P<0..3>	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_LVDS_IG_B_DATAN<0..3>	LVDS_IG_B_DATA_N<0..3>	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_LVDS_IG_A_DATAP<3>	LVDS_IG_A_DATA_P<3>	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_LVDS_IG_A_DATAN<3>	LVDS_IG_A_DATA_N<3>	MAKE_BASE=TRUE, NO_TEST=TRUE
LCD_BKLT_PWM	LVDS_IG_BKL_PWM	MAKE_BASE=TRUE
LCD_IG_PWR_EN	LVDS_IG_PANEL_PWR	MAKE_BASE=TRUE
LCD_BKLT_EN	LVDS_IG_BKL_ON	MAKE_BASE=TRUE

SMC Aliases

Unused SMC Signals

SMC_SYS_LED	NC_SMC_SYS_LED	MAKE_BASE=TRUE, NO_TEST=TRUE
IR_RX_OUT_RC	NC_IR_RX_OUT_RC	MAKE_BASE=TRUE, NO_TEST=TRUE

TP_DP_IG_D_HPD — DP_IG_D_HPD (MAKE_BASE=TRUE)

R0909 100K 5% 1/20W MF 201

NC_PCIE_5_R2D_CP	PCIE_TBT_R2D_C_P<0>	MAKE_BASE=TRUE
NC_PCIE_6_R2D_CP	PCIE_TBT_R2D_C_P<1>	MAKE_BASE=TRUE
NC_PCIE_7_R2D_CP	PCIE_TBT_R2D_C_P<2>	MAKE_BASE=TRUE
NC_PCIE_8_R2D_CP	PCIE_TBT_R2D_C_P<3>	MAKE_BASE=TRUE
NC_PCIE_5_R2D_CN	PCIE_TBT_R2D_C_N<0>	MAKE_BASE=TRUE
NC_PCIE_6_R2D_CN	PCIE_TBT_R2D_C_N<1>	MAKE_BASE=TRUE
NC_PCIE_7_R2D_CN	PCIE_TBT_R2D_C_N<2>	MAKE_BASE=TRUE
NC_PCIE_8_R2D_CN	PCIE_TBT_R2D_C_N<3>	MAKE_BASE=TRUE
NC_PCIE_5_D2RP	PCIE_TBT_D2R_P<0>	MAKE_BASE=TRUE
NC_PCIE_6_D2RP	PCIE_TBT_D2R_P<1>	MAKE_BASE=TRUE
NC_PCIE_7_D2RP	PCIE_TBT_D2R_P<2>	MAKE_BASE=TRUE
NC_PCIE_8_D2RP	PCIE_TBT_D2R_P<3>	MAKE_BASE=TRUE
NC_PCIE_5_D2RN	PCIE_TBT_D2R_N<0>	MAKE_BASE=TRUE
NC_PCIE_6_D2RN	PCIE_TBT_D2R_N<1>	MAKE_BASE=TRUE
NC_PCIE_7_D2RN	PCIE_TBT_D2R_N<2>	MAKE_BASE=TRUE
NC_PCIE_8_D2RN	PCIE_TBT_D2R_N<3>	MAKE_BASE=TRUE

TBT DP Ports

DPB_IG_HPD	DP_TBTSNK1_HPD	MAKE_BASE=TRUE
DPA_IG_HPD	DP_TBTSNK0_HPD	MAKE_BASE=TRUE
DP_TBTSNK0_AUXCH_C_P	DPA_IG_AUX_CH_P	MAKE_BASE=TRUE
DP_TBTSNK0_AUXCH_C_N	DPA_IG_AUX_CH_N	MAKE_BASE=TRUE
DP_TBTSNK1_AUXCH_C_P	DPB_IG_AUX_CH_P	MAKE_BASE=TRUE
DP_TBTSNK1_AUXCH_C_N	DPB_IG_AUX_CH_N	MAKE_BASE=TRUE
DP_TBTSNK1_ML_C_P<3..0>	TP_DP_IG_C_MLP<3..0>	MAKE_BASE=TRUE
DP_TBTSNK1_ML_C_N<3..0>	TP_DP_IG_C_MLN<3..0>	MAKE_BASE=TRUE
DP_TBTSNK0_ML_C_P<3..0>	TP_DP_IG_B_MLP<3..0>	MAKE_BASE=TRUE
DP_TBTSNK0_ML_C_N<3..0>	TP_DP_IG_B_MLN<3..0>	MAKE_BASE=TRUE
DP_TBTPB_ML_C_P<1>	NC_DP_TBTPB_ML_C_P<1>	MAKE_BASE=TRUE
DP_TBTPB_ML_C_N<1>	NC_DP_TBTPB_ML_C_N<1>	MAKE_BASE=TRUE
DP_TBTPB_ML_C_P<3>	NC_DP_TBTPB_ML_C_P<3>	MAKE_BASE=TRUE
DP_TBTPB_ML_C_N<3>	NC_DP_TBTPB_ML_C_N<3>	MAKE_BASE=TRUE
DP_TBTPB_AUXCH_C_P	NC_DP_TBTPB_AUXCH_C_P	MAKE_BASE=TRUE
DP_TBTPB_AUXCH_C_N	NC_DP_TBTPB_AUXCH_C_N	MAKE_BASE=TRUE

TBT_B_R2D_C_N<0>	NC_TBT_B_R2D_C_N<0>	MAKE_BASE=TRUE	NO_TEST=TRUE
TBT_B_R2D_C_P<0>	NC_TBT_B_R2D_C_P<0>	MAKE_BASE=TRUE	NO_TEST=TRUE
TBT_B_R2D_C_N<1>	NC_TBT_B_R2D_C_N<1>	MAKE_BASE=TRUE	NO_TEST=TRUE
TBT_B_R2D_C_P<1>	NC_TBT_B_R2D_C_P<1>	MAKE_BASE=TRUE	NO_TEST=TRUE
TBT_B_D2R_P<0>	NC_TBT_B_D2R_P<0>	MAKE_BASE=TRUE	NO_TEST=TRUE
TBT_B_D2R_N<0>	NC_TBT_B_D2R_N<0>	MAKE_BASE=TRUE	NO_TEST=TRUE
TBT_B_D2R_P<1>	NC_TBT_B_D2R_P<1>	MAKE_BASE=TRUE	NO_TEST=TRUE
TBT_B_D2R_N<1>	NC_TBT_B_D2R_N<1>	MAKE_BASE=TRUE	NO_TEST=TRUE

TBT_B_CIO_SEL
DP_TBTPB_HPD
TBT_B_CONFIG2_RC
TBT_B_CONFIG1_BUF
TBT_B_LSRX

R0916 10K 5% 1/20W MF 201
R0917 10K 5% 1/20W MF 201
R0918 10K 5% 1/20W MF 201
R0919 10K 5% 1/20W MF 201
R0914 10K 5% 1/20W MF 201

TBT_B_LSTX — NC_TBT_B_LSTX (MAKE_BASE=TRUE, NO_TEST=TRUE)

SYNC MASTER=J13 MLB NON POR
SYNC DATE=11/10/2011
PAGE TITLE: Signal Aliases

Apple Inc.

DRAWING NUMBER: 051-9277
SIZE: D
REVISION: 2.8.0
BRANCH:
PAGE: 9 OF 109
SHEET: 8 OF 73

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NOTE: Intel provides an internal pull-up OF 5-15k to VCCIO on all CFG signals.

OMIT_TABLE
CRITICAL

U1000
IVY-BRIDGE
2C-35W
BGA
(1 OF 9)

DMI
PCI EXPRESS BASED INTERFACE SIGNALS
INTEL FLEXIBLE DISPLAY INTERFACE SIGNALS
EMBEDDED DISPLAY PORT

DMI_S2N_N<0>	M2	DMI_RX_0*	DMI
DMI_S2N_N<1>	P6	DMI_RX_1*	
DMI_S2N_N<2>	P1	DMI_RX_2*	
DMI_S2N_N<3>	P10	DMI_RX_3*	
DMI_S2N_P<0>	N3	DMI_RX_0	
DMI_S2N_P<1>	P7	DMI_RX_1	
DMI_S2N_P<2>	P3	DMI_RX_2	
DMI_S2N_P<3>	P11	DMI_RX_3	
DMI_N2S_N<0>	K1	DMI_TX_0*	
DMI_N2S_N<1>	M8	DMI_TX_1*	
DMI_N2S_N<2>	N4	DMI_TX_2*	
DMI_N2S_N<3>	R2	DMI_TX_3*	
DMI_N2S_P<0>	K3	DMI_TX_0	
DMI_N2S_P<1>	M7	DMI_TX_1	
DMI_N2S_P<2>	P4	DMI_TX_2	
DMI_N2S_P<3>	T3	DMI_TX_3	
FDI_DATA_N<0>	U7	FDI0_TX_0*	INTEL FLEXIBLE DISPLAY INTERFACE SIGNALS
FDI_DATA_N<1>	W11	FDI0_TX_1*	
FDI_DATA_N<2>	W1	FDI0_TX_2*	
FDI_DATA_N<3>	AA6	FDI0_TX_3*	
FDI_DATA_N<4>	W6	FDI1_TX_0*	
FDI_DATA_N<5>	V4	FDI1_TX_1*	
FDI_DATA_N<6>	Y2	FDI1_TX_2*	
FDI_DATA_N<7>	AC9	FDI1_TX_3*	
FDI_DATA_P<0>	U6	FDI0_TX_0	
FDI_DATA_P<1>	W10	FDI0_TX_1	
FDI_DATA_P<2>	W3	FDI0_TX_2	
FDI_DATA_P<3>	AA7	FDI0_TX_3	
FDI_DATA_P<4>	W7	FDI1_TX_0	
FDI_DATA_P<5>	T4	FDI1_TX_1	
FDI_DATA_P<6>	AA3	FDI1_TX_2	
FDI_DATA_P<7>	AC8	FDI1_TX_3	
FDI_FSYNC<0>	AA11	FDI0_FSYNC	
FDI_FSYNC<1>	AC12	FDI1_FSYNC	
FDI_INT	U11	FDI_INT	
FDI_LSYNC<0>	AA10	FDI0_LSYNC	
FDI_LSYNC<1>	AG8	FDI1_LSYNC	
EDP_COMP	AD2	EDP_ICOMPO	EMBEDDED DISPLAY PORT
	AF3	EDP_COMPIO	
EDP_HPD_L	AG11	EDP_HPD	
DP_INT_AUX_CH_N	AG4	EDP_AUX*	
DP_INT_AUX_CH_P	AF4	EDP_AUX	
DP_INT_ML_N<0>	AC3	EDP_TX_0*	
TP_EDP_TX_N<1>	AC4	EDP_TX_1*	
TP_EDP_TX_N<2>	AE11	EDP_TX_2*	
TP_EDP_TX_N<3>	AE7	EDP_TX_3*	
DP_INT_ML_P<0>	AC1	EDP_TX_0	
TP_EDP_TX_P<1>	AA4	EDP_TX_1	
TP_EDP_TX_P<2>	AE10	EDP_TX_2	
TP_EDP_TX_P<3>	AE6	EDP_TX_3	

=PP1V05_S0_CPU_VCCIO

R1030 24.9 1% 1/20W MF 201 — PLACE_NEAR=U1000.AF3:12.7MM

R1010 24.9 1% 1/20W MF 201 — CPU_PEG_COMP — PLACE_NEAR=U1000.G3:12.7MM

PEG_ICOMPI	G3		
PEG_ICOMPO	G1		
PEG_RCOMPO	G4		
PEG_RX_0*	H22	=PEG_D2R_N<0>	
PEG_RX_1*	J21	=PEG_D2R_N<1>	
PEG_RX_2*	B22	=PEG_D2R_N<2>	
PEG_RX_3*	D21	=PEG_D2R_N<3>	
PEG_RX_4*	A19	=PEG_D2R_N<4>	
PEG_RX_5*	D17	=PEG_D2R_N<5>	
PEG_RX_6*	B14	=PEG_D2R_N<6>	
PEG_RX_7*	D13	=PEG_D2R_N<7>	
PEG_RX_8*	A11	=PEG_D2R_N<8>	
PEG_RX_9*	B10	=PEG_D2R_N<9>	
PEG_RX_10*	G8	=PEG_D2R_N<10>	
PEG_RX_11*	A8	=PEG_D2R_N<11>	
PEG_RX_12*	B6	=PEG_D2R_N<12>	
PEG_RX_13*	H8	=PEG_D2R_N<13>	
PEG_RX_14*	E5	=PEG_D2R_N<14>	
PEG_RX_15*	K7	=PEG_D2R_N<15>	
PEG_RX_0	K22	=PEG_D2R_P<0>	
PEG_RX_1	K19	=PEG_D2R_P<1>	
PEG_RX_2	C21	=PEG_D2R_P<2>	
PEG_RX_3	D19	=PEG_D2R_P<3>	
PEG_RX_4	C19	=PEG_D2R_P<4>	
PEG_RX_5	D16	=PEG_D2R_P<5>	
PEG_RX_6	C13	=PEG_D2R_P<6>	
PEG_RX_7	D12	=PEG_D2R_P<7>	
PEG_RX_8	C11	=PEG_D2R_P<8>	
PEG_RX_9	C9	=PEG_D2R_P<9>	
PEG_RX_10	F8	=PEG_D2R_P<10>	
PEG_RX_11	C8	=PEG_D2R_P<11>	
PEG_RX_12	C5	=PEG_D2R_P<12>	
PEG_RX_13	H6	=PEG_D2R_P<13>	
PEG_RX_14	F6	=PEG_D2R_P<14>	
PEG_RX_15	K6	=PEG_D2R_P<15>	
PEG_TX_0*	G22	=PEG_R2D_C_N<0>	
PEG_TX_1*	C23	=PEG_R2D_C_N<1>	
PEG_TX_2*	D23	=PEG_R2D_C_N<2>	
PEG_TX_3*	F21	=PEG_R2D_C_N<3>	
PEG_TX_4*	H19	=PEG_R2D_C_N<4>	
PEG_TX_5*	C17	=PEG_R2D_C_N<5>	
PEG_TX_6*	K15	=PEG_R2D_C_N<6>	
PEG_TX_7*	F17	=PEG_R2D_C_N<7>	
PEG_TX_8*	F14	=PEG_R2D_C_N<8>	
PEG_TX_9*	A15	=PEG_R2D_C_N<9>	
PEG_TX_10*	J14	=PEG_R2D_C_N<10>	
PEG_TX_11*	H13	=PEG_R2D_C_N<11>	
PEG_TX_12*	M10	=PEG_R2D_C_N<12>	
PEG_TX_13*	F10	=PEG_R2D_C_N<13>	
PEG_TX_14*	D9	=PEG_R2D_C_N<14>	
PEG_TX_15*	J4	=PEG_R2D_C_N<15>	
PEG_TX_0	F22	=PEG_R2D_C_P<0>	
PEG_TX_1	A23	=PEG_R2D_C_P<1>	
PEG_TX_2	D24	=PEG_R2D_C_P<2>	
PEG_TX_3	E21	=PEG_R2D_C_P<3>	
PEG_TX_4	G19	=PEG_R2D_C_P<4>	
PEG_TX_5	B18	=PEG_R2D_C_P<5>	
PEG_TX_6	K17	=PEG_R2D_C_P<6>	
PEG_TX_7	G17	=PEG_R2D_C_P<7>	
PEG_TX_8	E14	=PEG_R2D_C_P<8>	
PEG_TX_9	C15	=PEG_R2D_C_P<9>	
PEG_TX_10	K13	=PEG_R2D_C_P<10>	
PEG_TX_11	G13	=PEG_R2D_C_P<11>	
PEG_TX_12	K10	=PEG_R2D_C_P<12>	
PEG_TX_13	G10	=PEG_R2D_C_P<13>	
PEG_TX_14	D8	=PEG_R2D_C_P<14>	
PEG_TX_15	K4	=PEG_R2D_C_P<15>	

Intel Doc 467283 ChiefRiver Platform design guild rev0.71 section 2.2.12 recommendation.

NOTE: eDP_COMPIO and eDP_ICOMPO can not be left floating even if Internal Graphics is disabled since they are shared with other interfaces.

NOTE: The EDP_HPD processor input is a low voltage active low signal. Therefore, an inverting level shifter is required on the motherboard to convert the active High signal from Embedded DisplayPort sink device to low voltage signals for the processor (refer to latest Processor EDS for DC specifications).

If HPD is disabled while eDP interface is still enabled, connect it to CPU_VCCIO via a 10-KOhm pull-up resistor on the motherboard. This signal can be left as no-connect if entire eDP interface is disabled.

PLACE_NEAR=U1000.H43:50.8MM
PLACE_SIDE=BOTTOM

=PPVCORE_S0_CPU

=PPVCORE_S0_CPU_VCCAXG

R1064 49.9 1% 1/16W MF-LF 402 — NOSTUFF
R1070 49.9 1% 1/16W MF-LF 402 — NOSTUFF — PLACE_NEAR=U1000.H45:50.8MM, PLACE_SIDE=BOTTOM
R1065 49.9 1% 1/16W MF-LF 402 — NOSTUFF — PLACE_NEAR=U1000.K45:50.8MM, PLACE_SIDE=BOTTOM
R1071 49.9 1% 1/16W MF-LF 402 — NOSTUFF
PLACE_NEAR=U1000.K43:50.8MM, PLACE_SIDE=BOTTOM

CPU_CFG<0>	B50	CFG_0	
CPU_CFG<1>	C51	CFG_1	
CPU_CFG<2>	B54	CFG_2	
CPU_CFG<3>	D53	CFG_3	
CPU_CFG<4>	A51	CFG_4	
CPU_CFG<5>	C53	CFG_5	
CPU_CFG<6>	C55	CFG_6	
CPU_CFG<7>	H49	CFG_7	
CPU_CFG<8>	A55	CFG_8	
CPU_CFG<9>	H51	CFG_9	
CPU_CFG<10>	K49	CFG_10	
CPU_CFG<11>	K53	CFG_11	
CPU_CFG<12>	F53	CFG_12	
CPU_CFG<13>	G53	CFG_13	
CPU_CFG<14>	L51	CFG_14	
CPU_CFG<15>	F51	CFG_15	
CPU_CFG<16>	D52	CFG_16	
CPU_CFG<17>	L53	CFG_17	
CPU_VCC_VALSENSE_P	H43	VCC_VAL_SENSE	Note. VOLTAGE=1.25V
CPU_VCC_VALSENSE_N	K43	VSS_VAL_SENSE	Note. VOLTAGE=0V
CPU_AXG_VALSENSE_P	H45	VAXG_VAL_SENSE	Note. VOLTAGE=1.05V
CPU_AXG_VALSENSE_N	K45	VSSAXG_VAL_SENSE	Note. VOLTAGE=0V
TP_CPU_VCC_DIE_SENSE	F48	VCC_DIE_SENSE	
CPU_THERMD_P	H48	RSVD_6	
CPU_THERMD_N	K48	RSVD_7	
	BA19	RSVD_8	
	AY19	RSVD_9	
	BA21	RSVD_10	
	AY21	RSVD_11	
	BA19	RSVD_12	
	AY21	RSVD_13	
	BA22	RSVD_14	
	AY22	RSVD_15	
	AU19	RSVD_16	
	AU21	RSVD_17	
	BA21	RSVD_18	
	BA22	RSVD_19	
	BA25	RSVD_20	
	BA26	RSVD_21	
	BA22	RSVD_22	
	BE22	RSVD_23	
	BE26	RSVD_24	
	BE23	RSVD_25	
	BE26	RSVD_26	
	BE24	RSVD_27	

NOTE: Intel does not recommend to use this alnalog sense due to accuracy concern.

NOTE: Intel validation sense lines per doc 439028 rev1.0 HR_PPDG sections 6.2.1 and 6.3.1.

OMIT_TABLE
CRITICAL

U1000
BGA
(5 OF 9)
RESERVED
IVY-BRIDGE
2C-35W

MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.75V

SA_DIMM_VREFDQ	BE7	PPCPU_MEM_VREFDQ_A	OUT 31
SB_DIMM_VREFDQ	BG7	PPCPU_MEM_VREFDQ_B	OUT 31
RSVD_30	N42	NC	
RSVD_31	L42	NC	
RSVD_32	L43	NC	
RSVD_33	L45	NC	
RSVD_34	M13	NC	
RSVD_35	M14	NC	
RSVD_36	U14	NC	
RSVD_37	W14	NC	
RSVD_38	P13	NC	
RSVD_39	AT49	NC	
RSVD_40	K23	NC	
RSVD_41	AH2	NC	
RSVD_42	AG1	NC	
RSVD_43	AH3	NC	
RSVD_44	AH1	NC	
RSVD_45	N50	NC	
DC_TEST_A4	A4	TP_CPU_DC_TEST_A4	
DC_TEST_C4	C4	CPU_DC_TEST_C4_D3	
DC_TEST_D3	D3		
DC_TEST_D1	D1	TP_CPU_DC_TEST_D1	
DC_TEST_A58	A58	TP_CPU_DC_TEST_A58	
DC_TEST_A59	A59	CPU_DC_TEST_C59_A59	
DC_TEST_C59	C59		
DC_TEST_A61	A61	CPU_DC_TEST_C61_A61	
DC_TEST_C61	C61		
DC_TEST_D61	D61	TP_CPU_DC_TEST_D61	
DC_TEST_BD61	BD61	TP_CPU_DC_TEST_BD61	
DC_TEST_BE61	BE61	CPU_DC_TEST_BE59_BE61	
DC_TEST_BE59	BE59		
DC_TEST_BG61	BG61	CPU_DC_TEST_BG59_BG61	
DC_TEST_BG59	BG59		
DC_TEST_BG58	BG58	TP_CPU_DC_TEST_BG58	
DC_TEST_BG4	BG4	TP_CPU_DC_TEST_BG4	
DC_TEST_BG3	BG3	CPU_DC_TEST_C4_BE3_BG3	
DC_TEST_BE3	BE3		
DC_TEST_BG1	BG1	CPU_DC_TEST_C4_BE1_BG1	
DC_TEST_BE1	BE1		
DC_TEST_BD1	BD1	TP_CPU_DC_TEST_BD1	

CPU_CFG<7>
CPU_CFG<6>
CPU_CFG<5>
CPU_CFG<4>
CPU_CFG<2>
R1042 R1044 R1045 R1046 R1047 — 1K 1% 1/16W MF-LF 402 — NOSTUFF / EDP:YES

CPU_CFG<16>
CPU_CFG<3>
CPU_CFG<1>
CPU_CFG<0>
R1040 R1041 R1043 R1049 — 1K 1% 1/16W MF-LF 402 — NOSTUFF

These can be Placed close to J2500 and Only for debug access

=PP1V05_S0_CPU_VCCIO

R1031 1K 5% 1/20W MF 201 — PLACE_NEAR=U1000.AG11:12.7MM

EDP_HPD_L

DP_INT_HPD

Q1031 2N7002TXG SOT-523-3 — EDP:YES

CR SFF Intel doc #460452
Rise/Fall time <6ns

FOR IVYBRIDGE PROCESSOR

CFG [7] :PEG DEFER TRAINING	1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB	0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION	11 = 1 X16 (DEFAULT) 10 = 2 X8	01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED

SYNC MASTER=J13 MLB NON POR — SYNC DATE=10/17/2013

PAGE TITLE: CPU DMI/PEG/FDI/RSVD

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DRAWING NUMBER: 051-9277 — SIZE: D
REVISION: 2.8.0
BRANCH:
PAGE: 10 OF 109
SHEET: 9 OF 73

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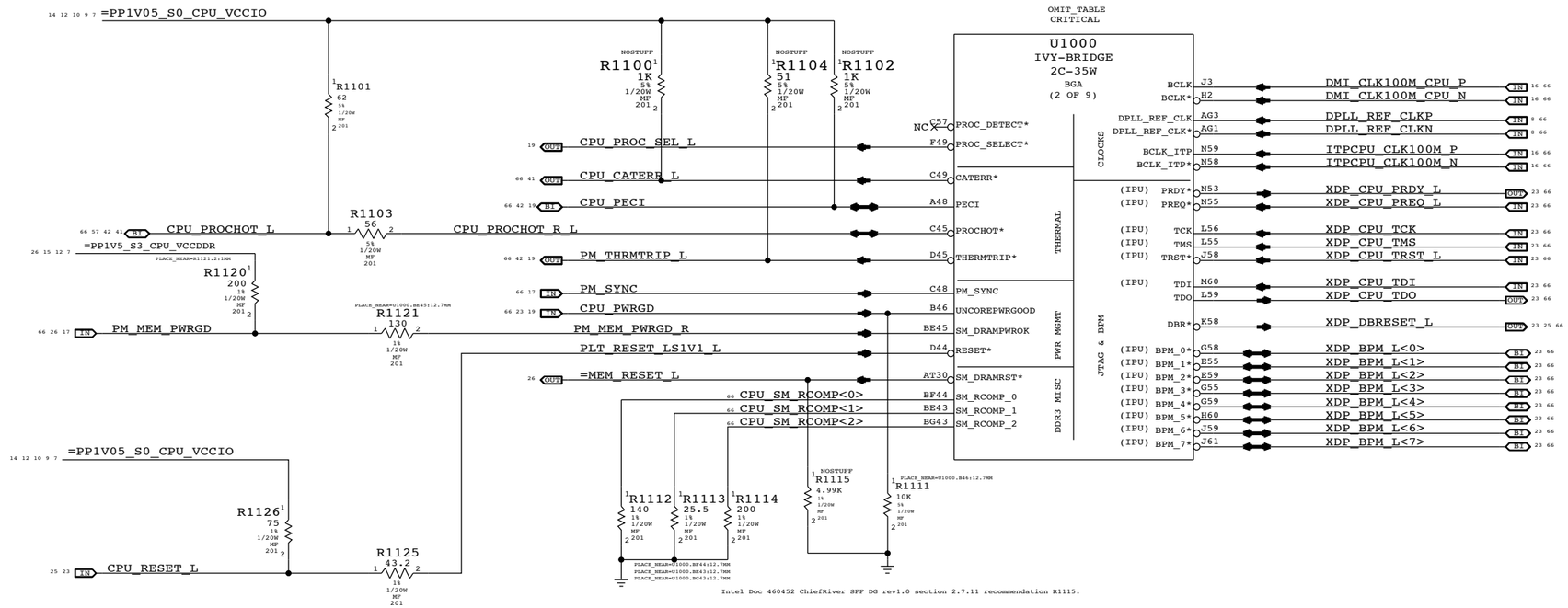

Intel Doc 460452 ChiefRiver SFF DG rev1.0 section 2.7.11 recommendation R1115.

SYNC MASTER=J30 MLB	SYNC DATE=07/27/2011
PAGE TITLE: CPU CLOCK/MISC/JTAG	
Apple Inc.	DRAWING NUMBER: 051-9277 SIZE: D
	REVISION: 2.8.0
	BRANCH:
	PAGE: 11 OF 109
	SHEET: 10 OF 73

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OMIT_TABLE
CRITICAL

U1000
BGA
(3 OF 9)
IVY-BRIDGE
2C-35W
MEMORY CHANNEL A

MEM_A_DQ<0>	AG6	SA_DQ_0	SA_CK_0	AU36	MEM_A_CLK_P<0>	OUT	27 28 32 67
MEM_A_DQ<1>	AJ6	SA_DQ_1	SA_CK_0*	AV36	MEM_A_CLK_N<0>	OUT	27 28 32 67
MEM_A_DQ<2>	AP11	SA_DQ_2	SA_CKE_0	AY26	MEM_A_CKE<0>	OUT	27 28 32 67
MEM_A_DQ<3>	AL6	SA_DQ_3					
MEM_A_DQ<4>	AJ10	SA_DQ_4	SA_CK_1	AT40	MEM_A_CLK_P<1>	OUT	8 67
MEM_A_DQ<5>	AJ8	SA_DQ_5	SA_CK_1*	AU40	MEM_A_CLK_N<1>	OUT	8 67
MEM_A_DQ<6>	AL8	SA_DQ_6					
MEM_A_DQ<7>	AL7	SA_DQ_7	SA_CKE_1	BB26	MEM_A_CKE<1>	OUT	27 28 32 67
MEM_A_DQ<8>	AR11	SA_DQ_8					
MEM_A_DQ<9>	AP6	SA_DQ_9	SA_CS_0*	BB40	MEM_A_CS_L<0>	OUT	27 28 32 67
MEM_A_DQ<10>	AU6	SA_DQ_10	SA_CS_1*	BC41	MEM_A_CS_L<1>	OUT	27 28 32 67
MEM_A_DQ<11>	AV9	SA_DQ_11					
MEM_A_DQ<12>	AR6	SA_DQ_12	SA_ODT_0	AY40	MEM_A_ODT<0>	OUT	27 28 32 67
MEM_A_DQ<13>	AP8	SA_DQ_13	SA_ODT_1	BA41	MEM_A_ODT<1>	OUT	27 28 32 67
MEM_A_DQ<14>	AT13	SA_DQ_14					
MEM_A_DQ<15>	AU13	SA_DQ_15	SA_DQS_0*	AL11	MEM_A_DQS_N<0>	BI	27 67
MEM_A_DQ<16>	BC7	SA_DQ_16	SA_DQS_1*	AR8	MEM_A_DQS_N<1>	BI	27 67
MEM_A_DQ<17>	BB7	SA_DQ_17	SA_DQS_2*	AV11	MEM_A_DQS_N<2>	BI	27 67
MEM_A_DQ<18>	BA13	SA_DQ_18	SA_DQS_3*	AT17	MEM_A_DQS_N<3>	BI	27 67
MEM_A_DQ<19>	BB11	SA_DQ_19	SA_DQS_4*	AV45	MEM_A_DQS_N<4>	BI	28 67
MEM_A_DQ<20>	BA7	SA_DQ_20	SA_DQS_5*	AY51	MEM_A_DQS_N<5>	BI	28 67
MEM_A_DQ<21>	BA9	SA_DQ_21	SA_DQS_6*	AT55	MEM_A_DQS_N<6>	BI	28 67
MEM_A_DQ<22>	BB9	SA_DQ_22	SA_DQS_7*	AK55	MEM_A_DQS_N<7>	BI	28 67
MEM_A_DQ<23>	AY13	SA_DQ_23					
MEM_A_DQ<24>	AV14	SA_DQ_24	SA_DQS_0	AJ11	MEM_A_DQS_P<0>	BI	27 67
MEM_A_DQ<25>	AR14	SA_DQ_25	SA_DQS_1	AR10	MEM_A_DQS_P<1>	BI	27 67
MEM_A_DQ<26>	AY17	SA_DQ_26	SA_DQS_2	AY11	MEM_A_DQS_P<2>	BI	27 67
MEM_A_DQ<27>	AR19	SA_DQ_27	SA_DQS_3	AU17	MEM_A_DQS_P<3>	BI	27 67
MEM_A_DQ<28>	BA14	SA_DQ_28	SA_DQS_4	AW45	MEM_A_DQS_P<4>	BI	28 67
MEM_A_DQ<29>	AU14	SA_DQ_29	SA_DQS_5	AV51	MEM_A_DQS_P<5>	BI	28 67
MEM_A_DQ<30>	BB14	SA_DQ_30	SA_DQS_6	AT56	MEM_A_DQS_P<6>	BI	28 67
MEM_A_DQ<31>	BB17	SA_DQ_31	SA_DQS_7	AK54	MEM_A_DQS_P<7>	BI	28 67
MEM_A_DQ<32>	BA45	SA_DQ_32					
MEM_A_DQ<33>	AR43	SA_DQ_33	SA_MA_0	BG35	MEM_A_A<0>	OUT	27 28 32 67
MEM_A_DQ<34>	AW48	SA_DQ_34	SA_MA_1	BB34	MEM_A_A<1>	OUT	27 28 32 67
MEM_A_DQ<35>	BC48	SA_DQ_35	SA_MA_2	BE35	MEM_A_A<2>	OUT	27 28 32 67
MEM_A_DQ<36>	BC45	SA_DQ_36	SA_MA_3	BD35	MEM_A_A<3>	OUT	27 28 32 67
MEM_A_DQ<37>	AR45	SA_DQ_37	SA_MA_4	AT34	MEM_A_A<4>	OUT	27 28 32 67
MEM_A_DQ<38>	AT48	SA_DQ_38	SA_MA_5	AU34	MEM_A_A<5>	OUT	27 28 32 67
MEM_A_DQ<39>	AY48	SA_DQ_39	SA_MA_6	BB32	MEM_A_A<6>	OUT	27 28 32 67
MEM_A_DQ<40>	BA49	SA_DQ_40	SA_MA_7	AT32	MEM_A_A<7>	OUT	27 28 32 67
MEM_A_DQ<41>	AV49	SA_DQ_41	SA_MA_8	AY32	MEM_A_A<8>	OUT	27 28 32 67
MEM_A_DQ<42>	BB51	SA_DQ_42	SA_MA_9	AV32	MEM_A_A<9>	OUT	27 28 32 67
MEM_A_DQ<43>	AY53	SA_DQ_43	SA_MA_10	BE37	MEM_A_A<10>	OUT	27 28 32 67
MEM_A_DQ<44>	BB49	SA_DQ_44	SA_MA_11	BA30	MEM_A_A<11>	OUT	27 28 32 67
MEM_A_DQ<45>	AU49	SA_DQ_45	SA_MA_12	BC30	MEM_A_A<12>	OUT	27 28 32 67
MEM_A_DQ<46>	BA53	SA_DQ_46	SA_MA_13	AW41	MEM_A_A<13>	OUT	27 28 32 67
MEM_A_DQ<47>	BB55	SA_DQ_47	SA_MA_14	AY28	MEM_A_A<14>	OUT	27 28 32 67
MEM_A_DQ<48>	BA55	SA_DQ_48	SA_MA_15	AU26	MEM_A_A<15>	OUT	27 28 32 67
MEM_A_DQ<49>	AV56	SA_DQ_49					
MEM_A_DQ<50>	AP50	SA_DQ_50					
MEM_A_DQ<51>	AP53	SA_DQ_51					
MEM_A_DQ<52>	AV54	SA_DQ_52					
MEM_A_DQ<53>	AT54	SA_DQ_53					
MEM_A_DQ<54>	AP56	SA_DQ_54					
MEM_A_DQ<55>	AP52	SA_DQ_55					
MEM_A_DQ<56>	AN57	SA_DQ_56					
MEM_A_DQ<57>	AN53	SA_DQ_57					
MEM_A_DQ<58>	AG56	SA_DQ_58					
MEM_A_DQ<59>	AG53	SA_DQ_59					
MEM_A_DQ<60>	AN55	SA_DQ_60					
MEM_A_DQ<61>	AN52	SA_DQ_61					
MEM_A_DQ<62>	AG55	SA_DQ_62					
MEM_A_DQ<63>	AK56	SA_DQ_63					
MEM_A_BA<0>	BD37	SA_BS_0					
MEM_A_BA<1>	BF36	SA_BS_1					
MEM_A_BA<2>	BA28	SA_BS_2					
MEM_A_CAS_L	BE39	SA_CAS*					
MEM_A_RAS_L	BD39	SA_RAS*					
MEM_A_WE_L	AT41	SA_WE*					

OMIT_TABLE
CRITICAL

U1000
BGA
(4 OF 9)
IVY-BRIDGE
2C-35W
MEMORY CHANNEL B

MEM_B_DQ<0>	AL4	SB_DQ_0	SB_CK_0	BA34	MEM_B_CLK_P<0>	OUT	29 30 32 67
MEM_B_DQ<1>	AL1	SB_DQ_1	SB_CK_0*	AY34	MEM_B_CLK_N<0>	OUT	29 30 32 67
MEM_B_DQ<2>	AN3	SB_DQ_2	SB_CKE_0	AR22	MEM_B_CKE<0>	OUT	29 30 32 67
MEM_B_DQ<3>	AR4	SB_DQ_3					
MEM_B_DQ<4>	AK4	SB_DQ_4	SB_CK_1	BA36	MEM_B_CLK_P<1>	OUT	8 67
MEM_B_DQ<5>	AK3	SB_DQ_5	SB_CK_1*	BB36	MEM_B_CLK_N<1>	OUT	8 67
MEM_B_DQ<6>	AN4	SB_DQ_6					
MEM_B_DQ<7>	AR1	SB_DQ_7	SB_CKE_1	BF27	MEM_B_CKE<1>	OUT	29 30 32 67
MEM_B_DQ<8>	AU4	SB_DQ_8					
MEM_B_DQ<9>	AT2	SB_DQ_9	SB_CS_0*	BE41	MEM_B_CS_L<0>	OUT	29 30 32 67
MEM_B_DQ<10>	AV4	SB_DQ_10	SB_CS_1*	BE47	MEM_B_CS_L<1>	OUT	29 30 32 67
MEM_B_DQ<11>	BA4	SB_DQ_11					
MEM_B_DQ<12>	AU3	SB_DQ_12	SB_ODT_0	AT43	MEM_B_ODT<0>	OUT	29 30 32 67
MEM_B_DQ<13>	AR3	SB_DQ_13	SB_ODT_1	BG47	MEM_B_ODT<1>	OUT	29 30 32 67
MEM_B_DQ<14>	AY2	SB_DQ_14					
MEM_B_DQ<15>	BA3	SB_DQ_15	SB_DQS_0*	AL3	MEM_B_DQS_N<0>	BI	29 67
MEM_B_DQ<16>	BE9	SB_DQ_16	SB_DQS_1*	AV3	MEM_B_DQS_N<1>	BI	29 67
MEM_B_DQ<17>	BD9	SB_DQ_17	SB_DQS_2*	BG11	MEM_B_DQS_N<2>	BI	29 67
MEM_B_DQ<18>	BD13	SB_DQ_18	SB_DQS_3*	BD17	MEM_B_DQS_N<3>	BI	29 67
MEM_B_DQ<19>	BF12	SB_DQ_19	SB_DQS_4*	BG51	MEM_B_DQS_N<4>	BI	30 67
MEM_B_DQ<20>	BF8	SB_DQ_20	SB_DQS_5*	BA59	MEM_B_DQS_N<5>	BI	30 67
MEM_B_DQ<21>	BD10	SB_DQ_21	SB_DQS_6*	AT60	MEM_B_DQS_N<6>	BI	30 67
MEM_B_DQ<22>	BD14	SB_DQ_22	SB_DQS_7*	AK59	MEM_B_DQS_N<7>	BI	30 67
MEM_B_DQ<23>	BE13	SB_DQ_23					
MEM_B_DQ<24>	BF16	SB_DQ_24	SB_DQS_0	AM2	MEM_B_DQS_P<0>	BI	29 67
MEM_B_DQ<25>	BE17	SB_DQ_25	SB_DQS_1	AV1	MEM_B_DQS_P<1>	BI	29 67
MEM_B_DQ<26>	BE18	SB_DQ_26	SB_DQS_2	BE11	MEM_B_DQS_P<2>	BI	29 67
MEM_B_DQ<27>	BE21	SB_DQ_27	SB_DQS_3	BD18	MEM_B_DQS_P<3>	BI	29 67
MEM_B_DQ<28>	BE14	SB_DQ_28	SB_DQS_4	BE51	MEM_B_DQS_P<4>	BI	30 67
MEM_B_DQ<29>	BG14	SB_DQ_29	SB_DQS_5	BA61	MEM_B_DQS_P<5>	BI	30 67
MEM_B_DQ<30>	BG18	SB_DQ_30	SB_DQS_6	AR59	MEM_B_DQS_P<6>	BI	30 67
MEM_B_DQ<31>	BF19	SB_DQ_31	SB_DQS_7	AK61	MEM_B_DQS_P<7>	BI	30 67
MEM_B_DQ<32>	BD50	SB_DQ_32					
MEM_B_DQ<33>	BF48	SB_DQ_33	SB_MA_0	BF32	MEM_B_A<0>	OUT	29 30 32 67
MEM_B_DQ<34>	BD53	SB_DQ_34	SB_MA_1	BE33	MEM_B_A<1>	OUT	29 30 32 67
MEM_B_DQ<35>	BF52	SB_DQ_35	SB_MA_2	BD33	MEM_B_A<2>	OUT	29 30 32 67
MEM_B_DQ<36>	BD49	SB_DQ_36	SB_MA_3	AU30	MEM_B_A<3>	OUT	29 30 32 67
MEM_B_DQ<37>	BE49	SB_DQ_37	SB_MA_4	BD30	MEM_B_A<4>	OUT	29 30 32 67
MEM_B_DQ<38>	BD54	SB_DQ_38	SB_MA_5	AV30	MEM_B_A<5>	OUT	29 30 32 67
MEM_B_DQ<39>	BE53	SB_DQ_39	SB_MA_6	BG30	MEM_B_A<6>	OUT	29 30 32 67
MEM_B_DQ<40>	BF56	SB_DQ_40	SB_MA_7	BD29	MEM_B_A<7>	OUT	29 30 32 67
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MEM_B_DQ<45>	BG54	SB_DQ_45	SB_MA_12	AV28	MEM_B_A<12>	OUT	29 30 32 67
MEM_B_DQ<46>	BA58	SB_DQ_46	SB_MA_13	BD46	MEM_B_A<13>	OUT	29 30 32 67
MEM_B_DQ<47>	AW59	SB_DQ_47	SB_MA_14	AT26	MEM_B_A<14>	OUT	29 30 32 67
MEM_B_DQ<48>	AW58	SB_DQ_48	SB_MA_15	AU22	MEM_B_A<15>	OUT	29 30 32 67
MEM_B_DQ<49>	AU58	SB_DQ_49					
MEM_B_DQ<50>	AN61	SB_DQ_50					
MEM_B_DQ<51>	AN59	SB_DQ_51					
MEM_B_DQ<52>	AU59	SB_DQ_52					
MEM_B_DQ<53>	AU61	SB_DQ_53					
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MEM_B_BA<0>	BG39	SB_BS_0					
MEM_B_BA<1>	BD42	SB_BS_1					
MEM_B_BA<2>	AT22	SB_BS_2					
MEM_B_CAS_L	AV43	SB_CAS*					
MEM_B_RAS_L	BF40	SB_RAS*					
MEM_B_WE_L	BD45	SB_WE*					

SYNC MASTER=J30 MLB SYNC DATE=07/27/2011

PAGE TITLE
CPU DDR3 INTERFACES

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DRAWING NUMBER 051-9277 SIZE D
REVISION 2.8.0
BRANCH
PAGE 12 OF 109
SHEET 11 OF 73

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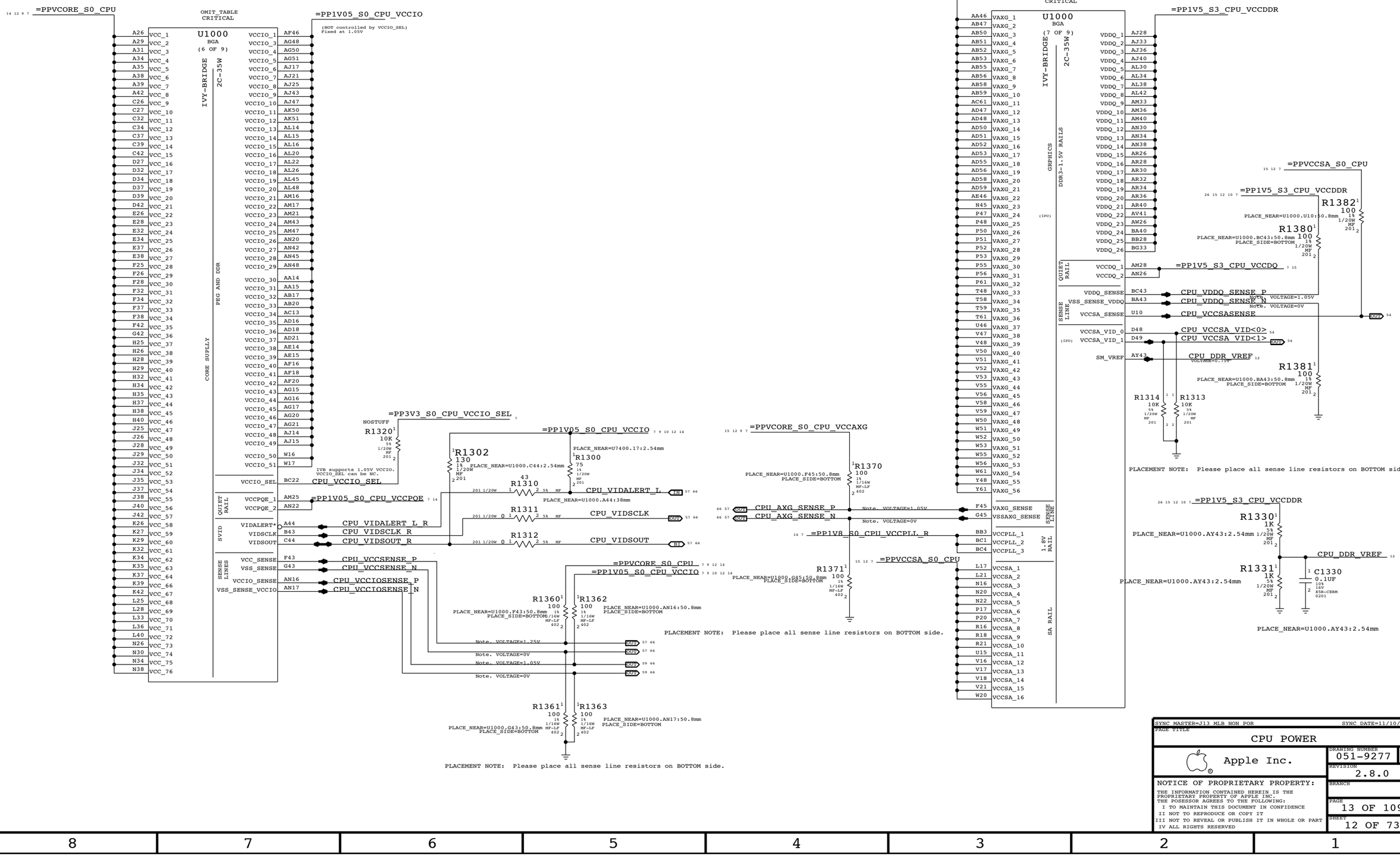

SYNC MASTER=J13 MLB NON POR
SYNC DATE=11/10/2011

PAGE TITLE

CPU POWER

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DRAWING NUMBER 051-9277
SIZE D
REVISION 2.8.0
BRANCH
PAGE 13 OF 109
SHEET 12 OF 73

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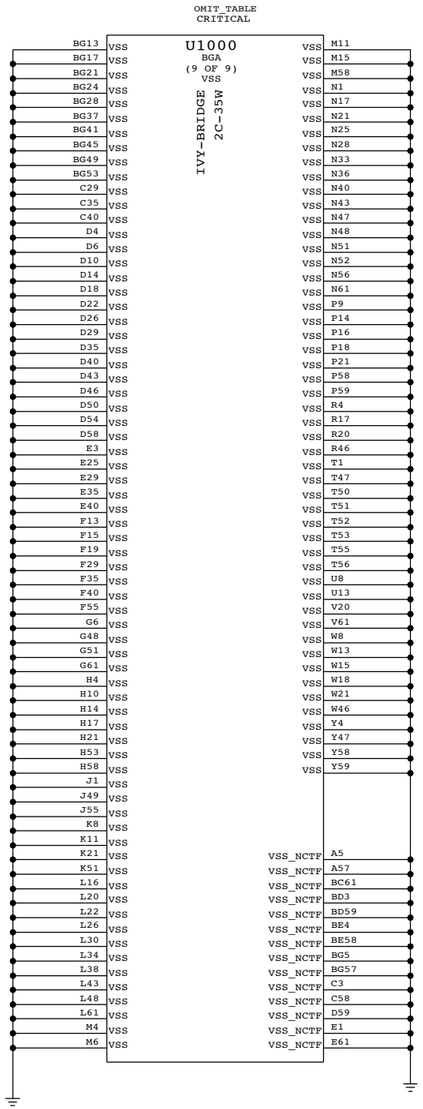

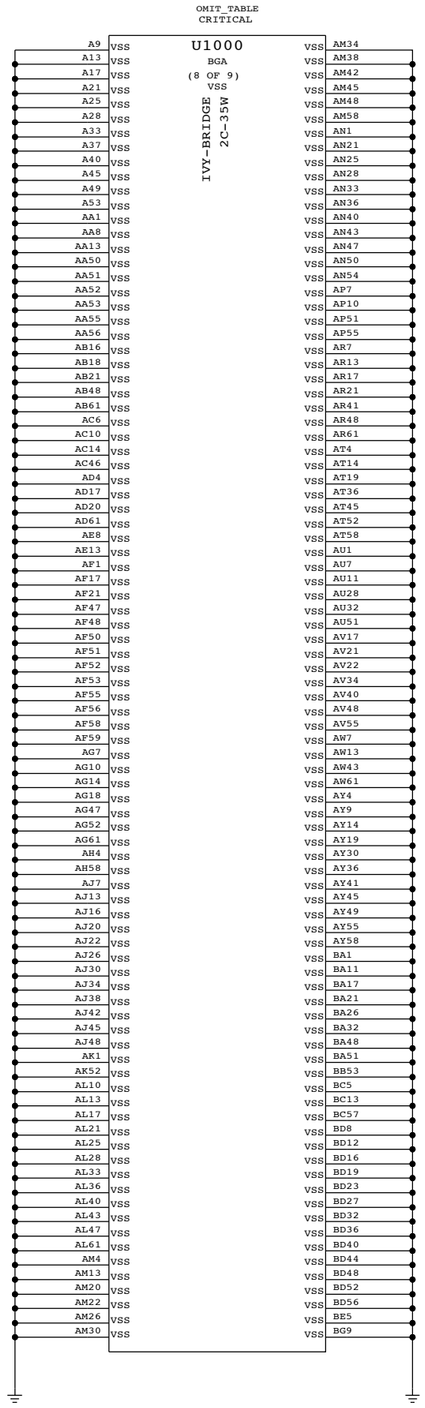

SYNC MASTER=J30 MLB	SYNC DATE=07/27/2011
PAGE TITLE	CPU GROUNDS
Apple Inc.	DRAWING NUMBER 051-9277 SIZE D
	REVISION 2.8.0
	BRANCH
	PAGE 14 OF 109
	SHEET 13 OF 73

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All INTEL recommendations from Intel doc #4439028 Huron River Platform Power Design Guide

CPU VCORE DECOUPLING

Processor Load Line : -2.9 mOhms

Intel recommendation (Table 7-1): 16x 2.2uF, 12x 22uF, 3x 330uF

12 9 7 =PPVCORE_S0_CPU

CRITICAL C1600 1UF 20% 6.3V X5R 0201 | C1601 1UF 20% 6.3V X5R 0201 | C1602 1UF 20% 6.3V X5R 0201 | C1603 1UF 20% 6.3V X5R 0201 | C1604 1UF 20% 6.3V X5R 0201 | C1605 1UF 20% 6.3V X5R 0201 | C1606 1UF 20% 6.3V X5R 0201 | C1607 1UF 20% 6.3V X5R 0201 | C1608 1UF 20% 6.3V X5R 0201 | C1609 1UF 20% 6.3V X5R 0201 | C1610 1UF 20% 6.3V X5R 0201 | C1611 1UF 20% 6.3V X5R 0201 | C1612 1UF 20% 6.3V X5R 0201 | C1613 1UF 20% 6.3V X5R 0201 | C1614 1UF 20% 6.3V X5R 0201 | C1615 1UF 20% 6.3V X5R 0201 | C1640 1UF 20% 6.3V X5R 0201 | C1641 1UF 20% 6.3V X5R 0201 | C1642 1UF 20% 6.3V X5R 0201

CRITICAL C1616 1UF 20% 6.3V X5R 0201 | C1617 1UF 20% 6.3V X5R 0201 | C1618 1UF 20% 6.3V X5R 0201 | C1619 1UF 20% 6.3V X5R 0201 | C1620 1UF 20% 6.3V X5R 0201 | C1621 1UF 20% 6.3V X5R 0201 | C1622 1UF 20% 6.3V X5R 0201 | C1623 1UF 20% 6.3V X5R 0201 | C1624 1UF 20% 6.3V X5R 0201 | C1625 1UF 20% 6.3V X5R 0201 | C1626 1UF 20% 6.3V X5R 0201 | C1627 1UF 20% 6.3V X5R 0201 | C1628 1UF 20% 6.3V X5R 0201 | C1629 1UF 20% 6.3V X5R 0201 | C1630 1UF 20% 6.3V X5R 0201 | C1631 1UF 20% 6.3V X5R 0201 | C1632 1UF 20% 6.3V X5R 0201 | C1633 1UF 20% 6.3V X5R 0201 | C1634 1UF 20% 6.3V X5R 0201 | C1635 1UF 20% 6.3V X5R 0201 | C1636 1UF 20% 6.3V X5R 0201 | C1637 1UF 20% 6.3V X5R 0201 | C1638 1UF 20% 6.3V X5R 0201 | C1639 1UF 20% 6.3V X5R 0201

PLACEMENT_NOTE (C1655-C1666):
Place close to U1000 on top side.

CRITICAL C1655 10UF 20% 6.3V CERM-X5R 0402-1 | C1656 10UF 20% 6.3V CERM-X5R 0402-1 | C1657 10UF 20% 6.3V CERM-X5R 0402-1 | C1658 10UF 20% 6.3V CERM-X5R 0402-1 | C1659 10UF 20% 6.3V CERM-X5R 0402-1 | C1660 10UF 20% 6.3V CERM-X5R 0402-1 | C1661 10UF 20% 6.3V CERM-X5R 0402-1 | C1662 10UF 20% 6.3V CERM-X5R 0402-1 | C1663 10UF 20% 6.3V CERM-X5R 0402-1 | C1664 10UF 20% 6.3V CERM-X5R 0402-1 | C1665 10UF 20% 6.3V CERM-X5R 0402-1 | C1666 10UF 20% 6.3V CERM-X5R 0402-1 | C1667 10UF 20% 6.3V CERM-X5R 0402-1 | C1668 10UF 20% 6.3V CERM-X5R 0402-1 | C1669 10UF 20% 6.3V CERM-X5R 0402-1 | C1670 10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1667-C1679):

PLACEMENT_NOTE (C1640-C1645):

C1680 270UF 20% 2V TANT CASE-B2-SM | C1681 270UF 20% 2V TANT CASE-B2-SM | C1682 270UF 20% 2V TANT CASE-B2-SM | C1683 270UF 20% 2V TANT CASE-B2-SM | C1679 270UF 20% 2V TANT CASE-B2-SM

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Section 6.5): 26x 1uF, 10x 10uF, 2x 330uF

PLACEMENT_NOTE (C1684-C167F):

Place on bottom side of U1000

12 10 9 7 =PP1V05_S0_CPU_VCCIO

C1684 1UF 10% 10V X5R 402 | C1685 1UF 10% 10V X5R 402 | C1686 1UF 10% 10V X5R 402 | C1687 1UF 10% 10V X5R 402 | C1688 1UF 10% 10V X5R 402 | C1689 1UF 10% 10V X5R 402 | C1690 1UF 10% 10V X5R 402 | C1691 1UF 10% 10V X5R 402 | C1692 1UF 10% 10V X5R 402 | C1693 1UF 10% 10V X5R 402 | C1694 1UF 10% 10V X5R 402 | C1695 1UF 10% 10V X5R 402 | C1696 1UF 10% 10V X5R 402

C1697 1UF 10% 10V X5R 402 | C1698 1UF 10% 10V X5R 402 | C1699 1UF 10% 10V X5R 402 | C169A 1UF 10% 10V X5R 402 | C169B 1UF 10% 10V X5R 402 | C169C 1UF 10% 10V X5R 402 | C169D 1UF 10% 10V X5R 402 | C169E 1UF 10% 10V X5R 402 | C169F 1UF 10% 10V X5R 402 | C161A 1UF 10% 10V X5R 402 | C161B 1UF 10% 10V X5R 402 | C161C 1UF 10% 10V X5R 402 | C161D 1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1672-C1681):

Place near U1000 on bottom side

C161E 10UF 20% 6.3V CERM-X5R 0402-1 | C161F 10UF 20% 6.3V CERM-X5R 0402-1 | C162A 10UF 20% 6.3V CERM-X5R 0402-1 | C162B 10UF 20% 6.3V CERM-X5R 0402-1 | C162C 10UF 20% 6.3V CERM-X5R 0402-1 | C162D 10UF 20% 6.3V CERM-X5R 0402-1 | C162E 10UF 20% 6.3V CERM-X5R 0402-1 | C167A 10UF 20% 6.3V CERM-X5R 0402-1 | C167B 10UF 20% 6.3V CERM-X5R 0402-1 | C167C 10UF 20% 6.3V CERM-X5R 0402-1

C167D 270UF 20% 2V TANT CASE-B2-SM | C167E 270UF 20% 2V TANT CASE-B2-SM | C167G 270UF 20% 2V TANT CASE-B2-SM | C167H 270UF 20% 2V TANT CASE-B2-SM

Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402

R1601 0.010 1% 1/4W MF 0603 =PP1V05_S0_CPU_VCCPQE 7 12

C167F 1UF 10% 10V X5R 402 Note:The smallest 10mOhm available in the library are 0805s

CPU VCCPLL DECOUPLING

Intel recommendation (section 6.4): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):

Place near U1000 on top side

7 =PP1V8_S0_CPU_VCCPLL

R1600 0 5% 1/16W MF-LF 402

C160X 1UF 10% 10V X5R 402 | C160Y 1UF 10% 10V X5R 402 | C160Z 270UF 20% 2V TANT CASE-B2-SM

=PP1V8_S0_CPU_VCCPLL_R 7 12

CPU VCCPLL Low pass filter

SYNC_MASTER=J11_MLB SYNC_DATE=10/03/2011

PAGE TITLE: CPU DECOUPLING-I

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DRAWING NUMBER 051-9277 | SIZE D
REVISION 2.8.0
BRANCH
PAGE 16 OF 109
SHEET 14 OF 73

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VAXG DECOUPLING

Graphics Load Line : -3.9 mOhms

Intel recommendation (section 6.3): 18x 1uF(9 no-stuff), 10x 104F(2 no-stuff), 8x 22uF(2 no stuff), 4x 470uF(2 no-stuff)

12 9 7 =PPVCORE_S0_CPU_VCCAXG

PLACEMENT_NOTE (C1700-C1710):

Place on bottom side of U1000

CRITICAL C1700 1UF 10% 10V X5R 402
CRITICAL C1701 1UF 10% 10V X5R 402
CRITICAL C1702 1UF 10% 10V X5R 402
CRITICAL C1703 1UF 10% 10V X5R 402
CRITICAL C1704 1UF 10% 10V X5R 402
CRITICAL C1705 1UF 10% 10V X5R 402
CRITICAL C1706 1UF 10% 10V X5R 402
CRITICAL C1707 1UF 10% 10V X5R 402
CRITICAL C1708 1UF 10% 10V X5R 402
CRITICAL C1709 1UF 10% 10V X5R 402
CRITICAL C1710 1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1711-C1716):

CRITICAL C1711 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1712 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1713 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1714 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1715 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1716 10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1717-C1722):

AXG_ACOUSTIC:NO C1717 22UF 20% 6.3V X5R-CERM1 0603
AXG_ACOUSTIC:NO C1718 22UF 20% 6.3V X5R-CERM1 0603
AXG_ACOUSTIC:NO C1719 22UF 20% 6.3V X5R-CERM1 0603
AXG_ACOUSTIC:NO C1720 22UF 20% 6.3V X5R-CERM1 0603
AXG_ACOUSTIC:NO C1721 22UF 20% 6.3V X5R-CERM1 0603
AXG_ACOUSTIC:NO C1722 22UF 20% 6.3V X5R-CERM1 0603
AXG_ACOUSTIC:YES C1727 22UF 20% 4V X5R 402
AXG_ACOUSTIC:YES C1728 22UF 20% 4V X5R 402
AXG_ACOUSTIC:YES C1729 22UF 20% 4V X5R 402
AXG_ACOUSTIC:YES C1730 22UF 20% 4V X5R 402
AXG_ACOUSTIC:YES C1731 22UF 20% 4V X5R 402
AXG_ACOUSTIC:YES C1732 22UF 20% 4V X5R 402

PLACEMENT_NOTE (C1723-C1724):

C1723 270UF 20% 2V TANT CASE-B2-SM
C1724 270UF 20% 2V TANT CASE-B2-SM
C1725 270UF 20% 2V TANT CASE-B2-SM

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation (Section 6.13): 10x 1uF, 8x 10uF, 1x 330uF

26 12 10 7 =PP1V5_S3_CPU_VCCDDR

PLACEMENT_NOTE (C1738-C1747):

Place on bottom side of U1000

C1738 1UF 10% 10V X5R 402
C1739 1UF 10% 10V X5R 402
C1740 1UF 10% 10V X5R 402
C1741 1UF 10% 10V X5R 402
C1742 1UF 10% 10V X5R 402
C1743 1UF 10% 10V X5R 402
C1744 1UF 10% 10V X5R 402
C1745 1UF 10% 10V X5R 402
C1746 1UF 10% 10V X5R 402
C1747 1UF 10% 10V X5R 402

Place close to U1000 on bottom side

C1748 10UF 20% 6.3V CERM-X5R 0402-1
C1749 10UF 20% 6.3V CERM-X5R 0402-1
C1750 10UF 20% 6.3V CERM-X5R 0402-1
C1751 10UF 20% 6.3V CERM-X5R 0402-1
C1752 10UF 20% 6.3V CERM-X5R 0402-1
C1753 10UF 20% 6.3V CERM-X5R 0402-1
C1754 10UF 20% 6.3V CERM-X5R 0402-1
C1755 10UF 20% 6.3V CERM-X5R 0402-1

C1756 270UF 20% 2V TANT CASE-B2-SM

Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402

R1702 0.010 1% 1/4W MF 0603

=PP1V5_S3_CPU_VCCDQ 7 12

C1757 1UF 10% 10V X5R 402

CPU VCCSA DECOUPLING

Intel recommendation (Section 6.6): 3x 1uf, 3x 10uf, 1x 330uf

12 7 =PPVCCSA_S0_CPU

PLACEMENT_NOTE (C1758-C1762):

Place on bottom side of U1000

C1758 1UF 10% 10V X5R 402
C1759 1UF 10% 10V X5R 402
C1760 1UF 10% 10V X5R 402
C1761 1UF 10% 10V X5R 402
C1762 1UF 10% 10V X5R 402

C1763 10UF 20% 6.3V CERM-X5R 0402-1
C1764 10UF 20% 6.3V CERM-X5R 0402-1
C1765 10UF 20% 6.3V CERM-X5R 0402-1
C1766 10UF 20% 6.3V CERM-X5R 0402-1
C1767 10UF 20% 6.3V CERM-X5R 0402-1

C1768 270UF 20% 2V TANT CASE-B2-SM

SYNC_MASTER=K21_MLB SYNC_DATE=07/29/2011

PAGE TITLE: CPU DECOUPLING-II

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DRAWING NUMBER 051-9277 SIZE D
REVISION 2.8.0
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PAGE 17 OF 109
SHEET 15 OF 73

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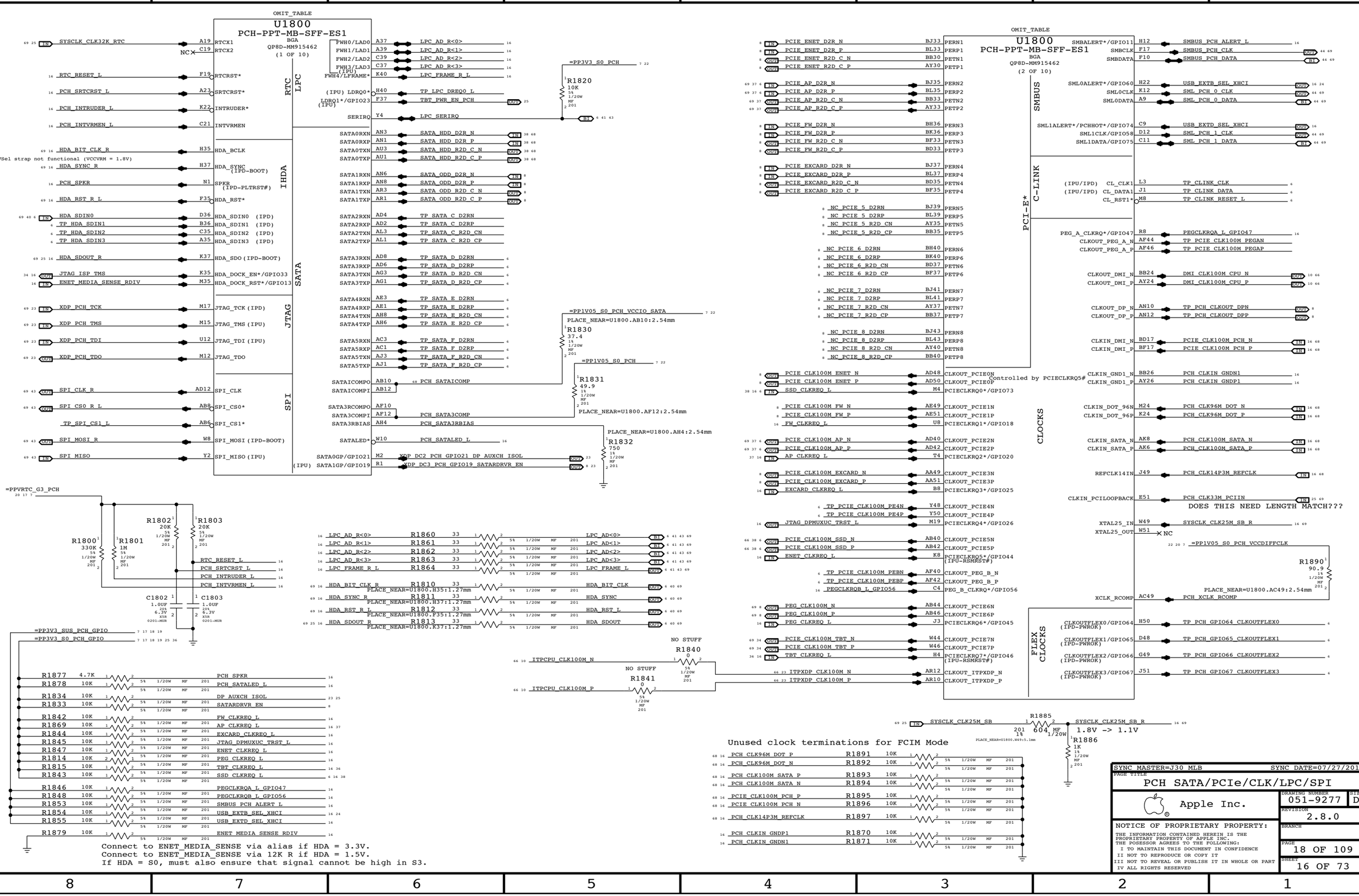
OMIT_TABLE
U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(1 OF 10)
RTC
LPC
HDA
SATA
JTAG
SPI
SYSCLK_CLK32K_RTC
RTCX1
RTCX2
NC
RTC_RESET_L
RTCRST*
PCH_SRTCRST_L
SRTCRST*
PCH_INTRUDER_L
INTRUDER*
PCH_INTVRMEN_L
INTVRMEN
HDA_BIT_CLK_R
HDA_BCLK
VSel strap not functional (VCCVRM = 1.8V)
HDA_SYNC_R
HDA_SYNC (IPD-BOOT)
PCH_SPKR
SPKR (IPD-PLTRST#)
HDA_RST_R_L
HDA_RST*
HDA_SDIN0
TP_HDA_SDIN1
TP_HDA_SDIN2
TP_HDA_SDIN3
HDA_SDOUT_R
JTAG_ISP_TMS
ENET_MEDIA_SENSE_RDIV
XDP_PCH_TCK
XDP_PCH_TMS
XDP_PCH_TDI
XDP_PCH_TDO
SPI_CLK_R
SPI_CS0_R_L
TP_SPI_CS1_L
SPI_MOSI_R
SPI_MISO
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME*
LPC_AD_R<0>
LPC_AD_R<1>
LPC_AD_R<2>
LPC_AD_R<3>
LPC_FRAME_R_L
(IPU) LDRQ0*
LDRQ1*/GPIO23
TP_LPC_DREQ0_L
TBT_PWR_EN_PCH
SERIRQ
LPC_SERIRQ
=PP3V3_S0_PCH
R1820 10K
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA_HDD_D2R_N
SATA_HDD_D2R_P
SATA_HDD_R2D_C_N
SATA_HDD_R2D_C_P
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA_ODD_D2R_N
SATA_ODD_D2R_P
SATA_ODD_R2D_C_N
SATA_ODD_R2D_C_P
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
TP_SATA_C_D2RN
TP_SATA_C_D2RP
TP_SATA_C_R2D_CN
TP_SATA_C_R2D_CP
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
TP_SATA_D_D2RN
TP_SATA_D_D2RP
TP_SATA_D_R2D_CN
TP_SATA_D_R2D_CP
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
TP_SATA_E_D2RN
TP_SATA_E_D2RP
TP_SATA_E_R2D_CN
TP_SATA_E_R2D_CP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
TP_SATA_F_D2RN
TP_SATA_F_D2RP
TP_SATA_F_R2D_CN
TP_SATA_F_R2D_CP
=PP1V05_S0_PCH_VCCIO_SATA
PLACE_NEAR=U1800.AB10:2.54mm
R1830 37.4
=PP1V05_S0_PCH
R1831 49.9
SATA3RCOMPO
SATA3CCOMPI
SATA3RBIAS
PCH_SATA3COMP
PCH_SATA3RBIAS
PLACE_NEAR=U1800.AF12:2.54mm
PLACE_NEAR=U1800.AH4:2.54mm
R1832 750
SATALED*
PCH_SATALED_L
SATA0GP/GPIO21
SATA1GP/GPIO19
XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL
XDP_DC3_PCH_GPIO19_SATARDRVR_EN
R1800 330K
R1801 1M
R1802 20K
R1803 20K
C1802 1.0UF
C1803 1.0UF
=PPVRTC_G3_PCH
=PP3V3_SUS_PCH_GPIO
=PP3V3_S0_PCH_GPIO
R1860 33
R1861 33
R1862 33
R1863 33
R1864 33
R1810 33
R1811 33
R1812 33
R1813 33
PLACE_NEAR=U1800.H35:1.27mm
PLACE_NEAR=U1800.H37:1.27mm
PLACE_NEAR=U1800.F35:1.27mm
PLACE_NEAR=U1800.K37:1.27mm
NO STUFF
R1840 0
R1841 0
ITPCPU_CLK100M_N
ITPCPU_CLK100M_P
R1877 4.7K
R1878 10K
R1834 10K
R1833 10K
R1842 10K
R1869 10K
R1844 10K
R1845 10K
R1847 10K
R1814 10K
R1815 10K
R1843 10K
R1846 10K
R1848 10K
R1853 10K
R1854 10K
R1855 10K
R1879 10K
Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.
OMIT_TABLE
U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(2 OF 10)
SMBUS
C-LINK
PCI-E*
CLOCKS
FLEX CLOCKS
PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_N
PCIE_ENET_R2D_C_P
PCIE_AP_D2R_N
PCIE_AP_D2R_P
PCIE_AP_R2D_C_N
PCIE_AP_R2D_C_P
PCIE_FW_D2R_N
PCIE_FW_D2R_P
PCIE_FW_R2D_C_N
PCIE_FW_R2D_C_P
PCIE_EXCARD_D2R_N
PCIE_EXCARD_D2R_P
PCIE_EXCARD_R2D_C_N
PCIE_EXCARD_R2D_C_P
NC_PCIE_5_D2RN
NC_PCIE_5_D2RP
NC_PCIE_5_R2D_CN
NC_PCIE_5_R2D_CP
NC_PCIE_6_D2RN
NC_PCIE_6_D2RP
NC_PCIE_6_R2D_CN
NC_PCIE_6_R2D_CP
NC_PCIE_7_D2RN
NC_PCIE_7_D2RP
NC_PCIE_7_R2D_CN
NC_PCIE_7_R2D_CP
NC_PCIE_8_D2RN
NC_PCIE_8_D2RP
NC_PCIE_8_R2D_CN
NC_PCIE_8_R2D_CP
PCIE_CLK100M_ENET_N
PCIE_CLK100M_ENET_P
SSD_CLKREQ_L
PCIE_CLK100M_FW_N
PCIE_CLK100M_FW_P
FW_CLKREQ_L
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
AP_CLKREQ_L
PCIE_CLK100M_EXCARD_N
PCIE_CLK100M_EXCARD_P
EXCARD_CLKREQ_L
TP_PCIE_CLK100M_PE4N
TP_PCIE_CLK100M_PE4P
JTAG_DPMUXUC_TRST_L
PCIE_CLK100M_SSD_N
PCIE_CLK100M_SSD_P
ENET_CLKREQ_L
TP_PCIE_CLK100M_PEBN
TP_PCIE_CLK100M_PEBP
PEGCLKRQB_L_GPIO56
PEG_CLK100M_N
PEG_CLK100M_P
PEG_CLKREQ_L
PCIE_CLK100M_TBT_N
PCIE_CLK100M_TBT_P
TBT_CLKREQ_L
ITPXDP_CLK100M_N
ITPXDP_CLK100M_P
SMBALERT*/GPIO11
SMBCLK
SMBDATA
SML0ALERT*/GPIO60
SML0CLK
SML0DATA
SML1ALERT*/PCHHOT*/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
(IPU/IPD) CL_CLK1
(IPU/IPD) CL_DATA1
CL_RST1*
PEG_A_CLKRQ*/GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N
CLKOUT_DP_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_GND1_N
CLKIN_GND1_P
CLKOUT_PCIE0N
CLKOUT_PCIE0P
PCIECLKRQ0*/GPIO73
Controlled by PCIECLKRQ5#
CLKOUT_PCIE1N
CLKOUT_PCIE1P
PCIECLKRQ1*/GPIO18
CLKOUT_PCIE2N
CLKOUT_PCIE2P
PCIECLKRQ2*/GPIO20
CLKOUT_PCIE3N
CLKOUT_PCIE3P
PCIECLKRQ3*/GPIO25
CLKOUT_PCIE4N
CLKOUT_PCIE4P
PCIECLKRQ4*/GPIO26
CLKOUT_PCIE5N
CLKOUT_PCIE5P
PCIECLKRQ5*/GPIO44 (IPU-RSMRST#)
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
PEG_B_CLKRQ*/GPIO56
CLKOUT_PCIE6N
CLKOUT_PCIE6P
PCIECLKRQ6*/GPIO45
CLKOUT_PCIE7N
CLKOUT_PCIE7P
PCIECLKRQ7*/GPIO46 (IPU-RSMRST#)
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
SMBUS_PCH_ALERT_L
SMBUS_PCH_CLK
SMBUS_PCH_DATA
USB_EXTB_SEL_XHCI
SML_PCH_0_CLK
SML_PCH_0_DATA
USB_EXTD_SEL_XHCI
SML_PCH_1_CLK
SML_PCH_1_DATA
TP_CLINK_CLK
TP_CLINK_DATA
TP_CLINK_RESET_L
PEGCLKRQA_L_GPIO47
TP_PCIE_CLK100M_PEGAN
TP_PCIE_CLK100M_PEGAP
DMI_CLK100M_CPU_N
DMI_CLK100M_CPU_P
TP_PCH_CLKOUT_DPN
TP_PCH_CLKOUT_DPP
PCIE_CLK100M_PCH_N
PCIE_CLK100M_PCH_P
PCH_CLKIN_GNDN1
PCH_CLKIN_GNDP1
PCH_CLK96M_DOT_N
PCH_CLK96M_DOT_P
PCH_CLK100M_SATA_N
PCH_CLK100M_SATA_P
PCH_CLK14P3M_REFCLK
PCH_CLK33M_PCIIN
DOES THIS NEED LENGTH MATCH???
SYSCLK_CLK25M_SB_R
=PP1V05_S0_PCH_VCCDIFFCLK
R1890 90.9
PCH_XCLK_RCOMP
TP_PCH_GPIO64_CLKOUTFLEX0
TP_PCH_GPIO65_CLKOUTFLEX1
TP_PCH_GPIO66_CLKOUTFLEX2
TP_PCH_GPIO67_CLKOUTFLEX3
SYSCLK_CLK25M_SB
R1885 604
SYSCLK_CLK25M_SB_R
1.8V -> 1.1V
R1886 1K
Unused clock terminations for FCIM Mode
R1891 10K
R1892 10K
R1893 10K
R1894 10K
R1895 10K
R1896 10K
R1897 10K
R1870 10K
R1871 10K
SYNC_MASTER=J30_MLB
SYNC_DATE=07/27/2011
PAGE TITLE
PCH SATA/PCIe/CLK/LPC/SPI
Apple Inc.
DRAWING NUMBER 051-9277
SIZE D
REVISION 2.8.0
BRANCH
PAGE 18 OF 109
SHEET 16 OF 73
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=PP3V3_SUS_PCH_GPIO 7 16 17 18 19
=PP1V05_S0_PCH_VCCIO_PCIE 7
PLACE_NEAR=U1800.BF19:12.7mm
R1905 10K 5% 1/20W MF 201
R1900 49.9 1% 1/20W MF 201

OMIT_TABLE
U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(3 OF 10)

DMI
FDI

DMI_N2S_N<0> BL21 DMI0RXN
DMI_N2S_N<1> BL23 DMI1RXN
DMI_N2S_N<2> BJ19 DMI2RXN
DMI_N2S_N<3> BL17 DMI3RXN
DMI_N2S_P<0> BJ21 DMI0RXP
DMI_N2S_P<1> BJ23 DMI1RXP
DMI_N2S_P<2> BL19 DMI2RXP
DMI_N2S_P<3> BJ17 DMI3RXP
DMI_S2N_N<0> BD22 DMI0TXN
DMI_S2N_N<1> BB22 DMI1TXN
DMI_S2N_N<2> BB19 DMI2TXN
DMI_S2N_N<3> BB17 DMI3TXN
DMI_S2N_P<0> BF22 DMI0TXP
DMI_S2N_P<1> AY22 DMI1TXP
DMI_S2N_P<2> AY19 DMI2TXP
DMI_S2N_P<3> AY17 DMI3TXP
PCH_DMI_COMP BF19 DMI_ZCOMP
BD19 DMI_IRCOMP
PCH_DMI2RBIAS BK20 DMI2RBIAS
PLACE_NEAR=U1800.BK20:2.54mm
R1920 750 1% 1/20W MF 201

FDI_RXN0 BL13 FDI_DATA_N<0>
FDI_RXN1 BJ15 FDI_DATA_N<1>
FDI_RXN2 BD12 FDI_DATA_N<2>
FDI_RXN3 BJ11 FDI_DATA_N<3>
FDI_RXN4 AY15 FDI_DATA_N<4>
FDI_RXN5 AY12 FDI_DATA_N<5>
FDI_RXN6 BJ9 FDI_DATA_N<6>
FDI_RXN7 BF10 FDI_DATA_N<7>
FDI_RXP0 BJ13 FDI_DATA_P<0>
FDI_RXP1 BL15 FDI_DATA_P<1>
FDI_RXP2 BF12 FDI_DATA_P<2>
FDI_RXP3 BL11 FDI_DATA_P<3>
FDI_RXP4 BB15 FDI_DATA_P<4>
FDI_RXP5 BB12 FDI_DATA_P<5>
FDI_RXP6 BL9 FDI_DATA_P<6>
FDI_RXP7 BD10 FDI_DATA_P<7>
FDI_INT BB10 FDI_INT
FDI_FSYNC0 BH12 FDI_FSYNC<0>
FDI_FSYNC1 BK8 FDI_FSYNC<1>
FDI_LSYNC0 BK12 FDI_LSYNC<0>
FDI_LSYNC1 BH8 FDI_LSYNC<1>

SYSTEM POWER MANAGEMENT

PCH_SUSACK_L 17 F15 SUSACK*(IPU)
PM_SYSRST_L 41 25 L1 SYS_RESET*
PM_PCH_SYS_PWROK 41 25 23 M10 SYS_PWROK
PM_PCH_PWROK 25 M22 PWROK
PM_PCH_APWROK 25 G3 APWROK
PM_MEM_PWRGD 66 26 10 B12 DRAMPWROK
PM_RSMRST_L 62 B20 RSMRST*
PCH_SUSWARN_L 17 C13 SUSWARN*/SUSPWRDNACK/GPIO30
PM_PWRBTN_L 41 23 17 K19 PWRBTN*(IPU)
SMC_ADAPTER_EN 62 42 41 H19 ACPRESENT/GPIO31 (IPD-DeepS4/S5)
PM_BATLOW_L 42 H10 BATLOW*/GPIO72 (IPU)
PCH_RI_L F12 RI*

DSWVRMEN F22 PCH_DSWVRMEN
DPWROK A21 PM_DSW_PWRGD
WAKE* D8 PCIE_WAKE_L
CLKRUN*/GPIO32 T2 PM_CLKRUN_L
SUS_STAT*/GPIO61 G6 LPC_PWRDWN_L
SUSCLK/GPIO62 D3 PM_CLK32K_SUSCLK_R
SLP_S5*/GPIO63 F6 PM_SLP_S5_L
SLP_S4* K10 PM_SLP_S4_L
SLP_S3* D4 PM_SLP_S3_L
SLP_A* C7 TP_PM_SLP_A_L
SLP_SUS* A15 PM_SLP_SUS_L
PMSYNCH BB8 PM_SYNC
SLP_LAN*/GPIO29 A7 MEM_VDD_SEL_1V5_L

=PPVRTC_G3_PCH 7 16 20
R1915 390K 5% 1/20W MF 201
R1909 100K 5% 1/20W MF 201

R1955 100K 5% 1/20W MF 201
LVDS_IG_BKL_ON 8 L_BKLTEN M44
LVDS_IG_PANEL_PWR 8 L_VDD_EN M42
LVDS_IG_BKL_PWM 8 L_BKLTCTL L49
L_DDC_CLK L51
L_DDC_DATA K46 (IPD-PLTRST#)
L_CTRL_CLK R42
L_CTRL_DATA M40
LVD_IBG AH42
LVD_VBG AH40
LVD_VREFH AG51
LVD_VREFL AG49
LVDSA_CLK* AK44
LVDSA_CLK AK46
LVDSA_DATA0* AR46
LVDSA_DATA1* AN49
LVDSA_DATA2* AN44
LVDSA_DATA3* AK40
LVDSA_DATA0 AR44
LVDSA_DATA1 AN51
LVDSA_DATA2 AN46
LVDSA_DATA3 AK42
LVDSB_CLK* AH46
LVDSB_CLK AH44
LVDSB_DATA0* AM50
LVDSB_DATA1* AL49
LVDSB_DATA2* AJ51
LVDSB_DATA3* AH50
LVDSB_DATA0 AM48
LVDSB_DATA1 AL51
LVDSB_DATA2 AJ49
LVDSB_DATA3 AH48

OMIT_TABLE
U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(4 OF 10)

LVDS
DIGITAL DISPLAY INTERFACE

SDVO_TVCLKINN (IPD) AU40 TP_SDVO_TVCLKINN
SDVO_TVCLKINP (IPD) AU42 TP_SDVO_TVCLKINP
SDVO_STALLN (IPD) AR51 TP_SDVO_STALLN
SDVO_STALLP (IPD) AR49 TP_SDVO_STALLP
SDVO_INTN (IPD) AT50 TP_SDVO_INTN
SDVO_INTP (IPD) AT48 TP_SDVO_INTP
SDVO_CTRLCLK W42 DPA_IG_DDC_CLK
SDVO_CTRLDATA (IPD-PLTRST#) R44 DPA_IG_DDC_DATA
DDPB_AUXN AW51 DPA_IG_AUX_CH_N
DDPB_AUXP AW49 DPA_IG_AUX_CH_P
DDPB_HPD AY42 DPA_IG_HPD
DDPB_0N AY48 TP_DP_IG_B_MLN<0>
DDPB_0P AY50 TP_DP_IG_B_MLP<0>
DDPB_1N AY44 TP_DP_IG_B_MLN<1>
DDPB_1P AY46 TP_DP_IG_B_MLP<1>
DDPB_2N BB44 TP_DP_IG_B_MLN<2>
DDPB_2P BB46 TP_DP_IG_B_MLP<2>
DDPB_3N BA49 TP_DP_IG_B_MLN<3>
DDPB_3P BA51 TP_DP_IG_B_MLP<3>
DDPC_CTRLCLK T50 DPB_IG_DDC_CLK
DDPC_CTRLDATA (IPD-PLTRST#) U44 DPB_IG_DDC_DATA
DDPC_AUXN AU51 DPB_IG_AUX_CH_N
DDPC_AUXP AU49 DPB_IG_AUX_CH_P
DDPC_HPD BE46 DPB_IG_HPD
DDPC_0N BC49 TP_DP_IG_C_MLN<0>
DDPC_0P BC51 TP_DP_IG_C_MLP<0>
DDPC_1N BD48 TP_DP_IG_C_MLN<1>
DDPC_1P BD50 TP_DP_IG_C_MLP<1>
DDPC_2N BF46 TP_DP_IG_C_MLN<2>
DDPC_2P BF45 TP_DP_IG_C_MLP<2>
DDPC_3N BE49 TP_DP_IG_C_MLN<3>
DDPC_3P BE51 TP_DP_IG_C_MLP<3>
DDPD_CTRLCLK M48 TP_DP_IG_D_CTRL_CLK
DDPD_CTRLDATA (IPD-PLTRST#) U42 TP_DP_IG_D_CTRL_DATA
DDPD_AUXN AU46 TP_DP_IG_D_AUXN
DDPD_AUXP AU44 TP_DP_IG_D_AUXP
DDPD_HPD BK44 TP_DP_IG_D_HPD
DDPD_0N BG51 TP_DP_IG_D_MLN<0>
DDPD_0P BG49 TP_DP_IG_D_MLP<0>
DDPD_1N BF42 TP_DP_IG_D_MLN<1>
DDPD_1P BD42 TP_DP_IG_D_MLP<1>
DDPD_2N BJ47 TP_DP_IG_D_MLN<2>
DDPD_2P BL47 TP_DP_IG_D_MLP<2>
DDPD_3N BL45 TP_DP_IG_D_MLN<3>
DDPD_3P BJ45 TP_DP_IG_D_MLP<3>

CRT

TP_CRT_IG_BLUE 6 M46 CRT_BLUE
TP_CRT_IG_GREEN 6 R46 CRT_GREEN
TP_CRT_IG_RED 6 U46 CRT_RED
TP_CRT_IG_DDC_CLK 6 R49 CRT_DDC_CLK
TP_CRT_IG_DDC_DATA 6 N49 CRT_DDC_DATA
TP_CRT_IG_HSYNC 6 M50 CRT_HSYNC
TP_CRT_IG_VSYNC 6 N51 CRT_VSYNC
PCH_DAC_IREF R51 DAC_IREF
PLACE_NEAR=U1800.R51:2.54mm
T48 CRT_IRTN
R1951 1K 2% 1/20W MF 201

19 18 17 16 7 =PP3V3_SUS_PCH_GPIO
R1983 10K 5% 1/20W MF 201
R1986 0 5% 1/20W MF 201
17 PCH_SUSWARN_L
PCH_SUSACK_L 17

=PP3V3_SUS_PCH_GPIO 7 16 17 18 19
=PP3V3_S0_PCH_GPIO 7 16 18 19 25 36
=PP3V3_S5_PCH 7

R1985 1K 5% 1/20W MF 201 PM_PWRBTN_L 17 23 41
R1991 8.2K 5% 1/20W MF 201 PM_CLKRUN_L 6 17 41 43
R1982 10K 5% 1/20W MF 201 MEM_VDD_SEL_1V5_L 17 56
R1925 1K 5% 1/20W MF 201 PCIE_WAKE_L 6 17 37
R1924 100K 5% 1/20W MF 201 PM_SLP_S3_L 17 26 41 62
R1921 100K 5% 1/20W MF 201 PM_SLP_S4_L 17 26 37 41 49 62
R1922 100K 5% 1/20W MF 201 PM_SLP_S5_L 17 41 62
R1923 100K 5% 1/20W MF 201 PM_SLP_SUS_L 17 62

SYNC_MASTER=J30_MLB SYNC_DATE=07/27/2011
PAGE TITLE
PCH DMI/FDI/PM/Graphics
Apple Inc.
DRAWING NUMBER 051-9277
SIZE D
REVISION 2.8.0
BRANCH
PAGE 19 OF 109
SHEET 17 OF 73

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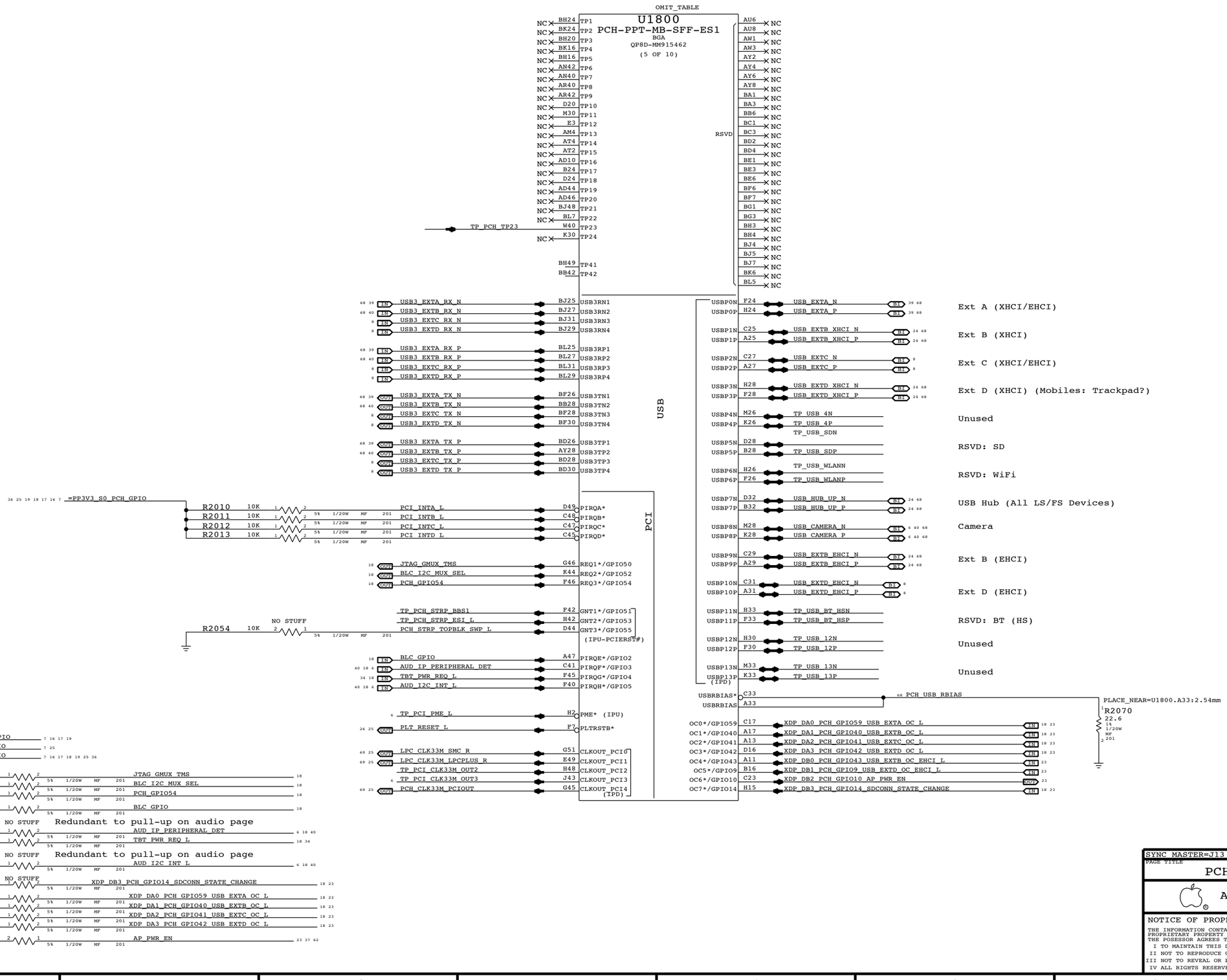

SYNC_MASTER=J13_MLB_NON_POR SYNC_DATE=11/10/2011

PAGE TITLE

PCH PCI/USB/TP/RSVD

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DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

BRANCH

PAGE 20 OF 109

SHEET 18 OF 73

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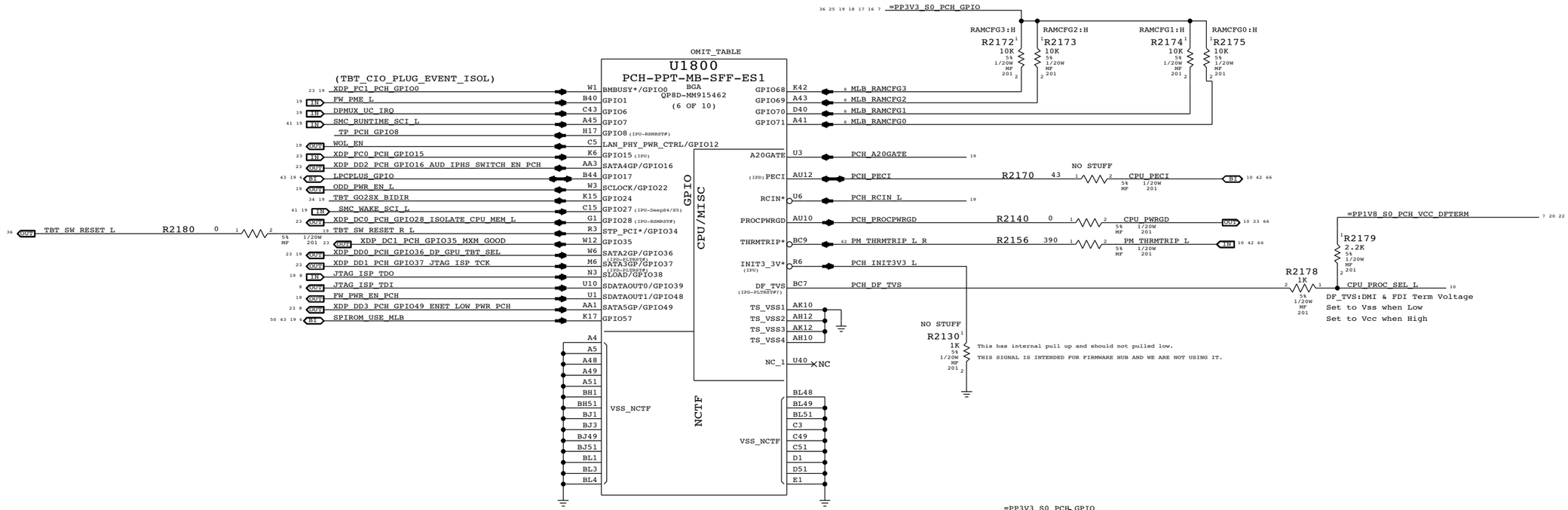
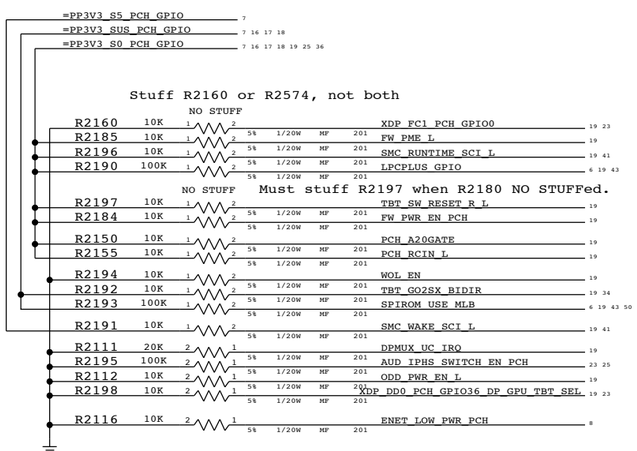
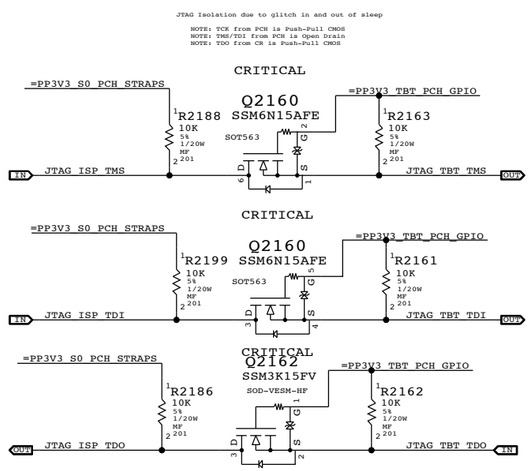
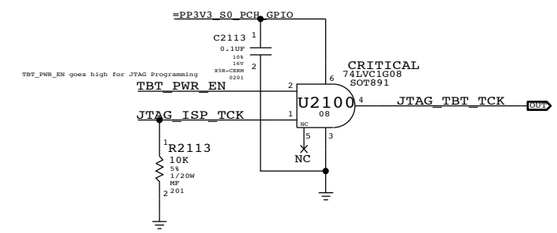
BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

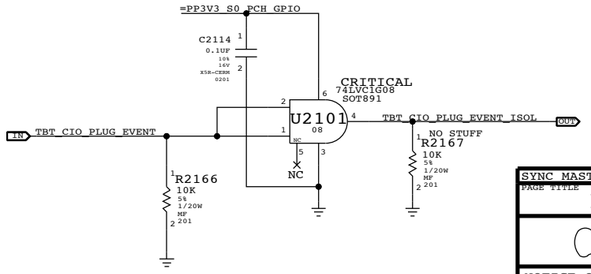
Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.











SYNC_MASTER=J11_MLB	SYNC_DATE=09/16/2011
PAGE TITLE	PCH GPIO/MISC/NCTF
Apple Inc.	DRAWING NUMBER 051-9277 / SIZE D
	REVISION 2.8.0
	BRANCH
	PAGE 21 OF 109
	SHEET 19 OF 73

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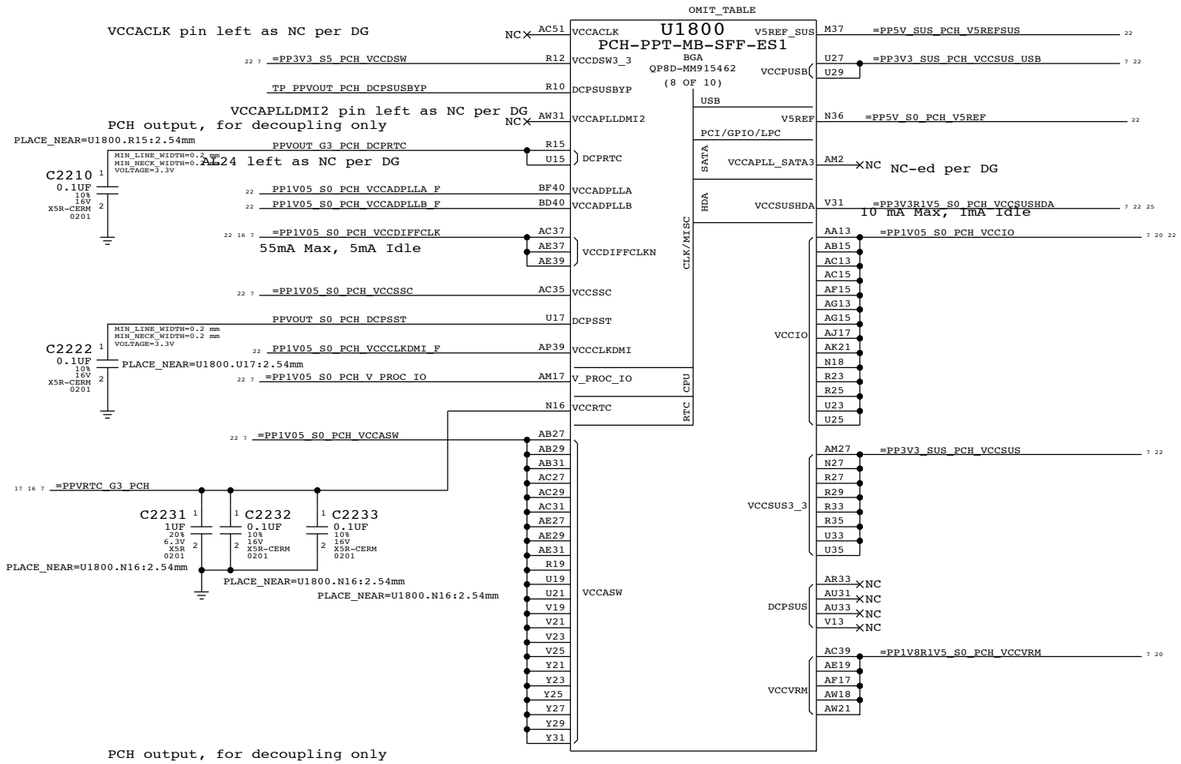

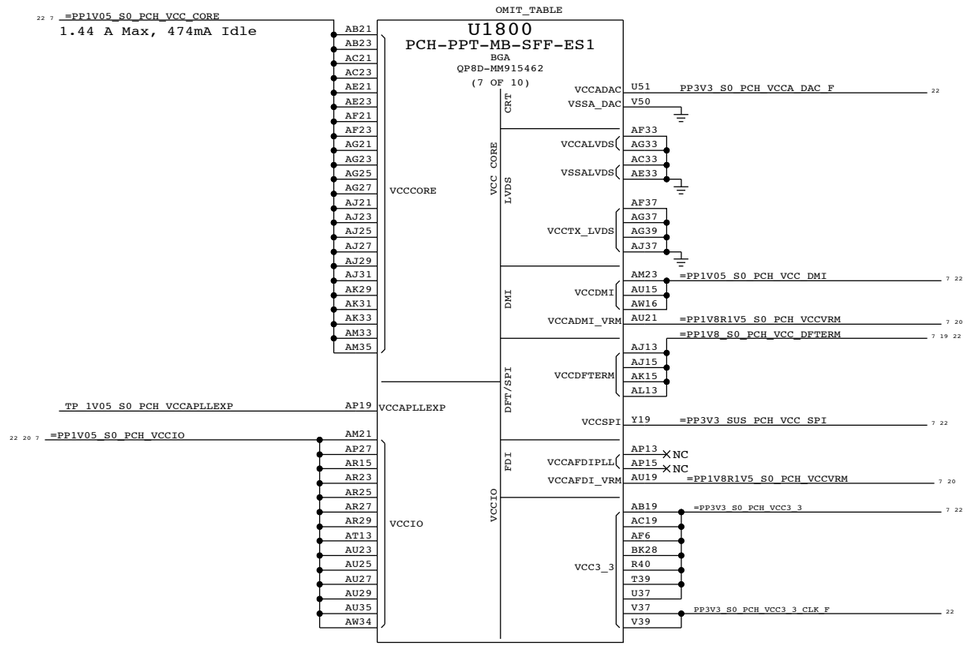

SYNC_MASTER=J11_MLB	SYNC_DATE=09/30/2011
PAGE TITLE	PCH POWER
Apple Inc.	DRAWING NUMBER 051-9277 · SIZE D
	REVISION 2.8.0
	BRANCH
	PAGE 22 OF 109
	SHEET 20 OF 73

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OMIT_TABLE

U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(9 OF 10)

AA7		AP2
AA9		AP4
AA11		AP7
AA39		AP9
AA41		AP11
AA43		AP17
AA45		AP21
AB2		AP23
AB4		AP25
AB17		AP29
AB25		AP31
AB33		AP33
AB35		AP35
AB37		AP37
AB48		AP41
AB50		AP43
AC7		AP45
AC9		AP48
AC11		AP50
AC17		AR6
AC25		AR8
AC41		AR17
AC43		AR19
AC45		AR21
AE7		AR31
AE9		AR35
AE11		AR37
AE13		AT7
AE15		AT9
AE17		AT11
AE25		AT39
AE35		AT41
AE41		AT43
AE43		AT45
AE45		AU17
AF2		AU37
AF4		AV2
AF8		AV4
AF19		AV48
AF25		AV50
AF27		AW7
AF29	VSS	AW9
AF31		AW11
AF35		AW13
AF48		AW23
AF50		AW25
AG7		AW27
AG9		AW29
AG11		AW36
AG17		AW39
AG19		AW41
AG29		AW43
AG31		AW45
AG35		AY10
AG41		B6
AG43		B10
AG45		B14
AH2		B18
AJ7		B22
AJ9		B26
AJ11		B30
AJ19		B34
AJ33		B38
AJ35		B42
AJ39		B46
AJ41		BA7
AJ43		BA9
AJ45		BA11
AK2		BA13
AK4		BA16
AK17		BA18
AK19		BA21
AK23		BA23
AK25		BA25
AK27		BA27
AK35		BA29
AK37		BA31
AK48		BA34
AK50		BA36
AL7		BA39
AL9		BA41
AL11		BA43
AL39		BA45
AL41		BB2
AL43		BB4
AL45		BB48
AM15		BB50
AM19		BC11
AM25		BC13
AM29		BC16
AM31		BC18
AM37		BC21

OMIT_TABLE

U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(10 OF 10)

BC23		G39
BC25		G41
BC27		G43
BC29		J7
BC31		J9
BC34		J11
BC36		J13
BC39		J16
BC41		J18
BC43		J21
BC45		J23
BD15		J25
BD24		J27
BE7		J29
BE9		J31
BE11		J34
BE13		J36
BE16		J39
BE18		J41
BE21		J45
BE23		K2
BE25		K4
BE27		K48
BE29		K50
BE31		L7
BE34		L9
BE36		L11
BE39		L13
BE41		L16
BE43		L18
BE45		L21
BF2		L23
BF4		L25
BF15		L27
BF24		L29
BF48		L31
BF50		L34
BH6		L36
BH10		L39
BH14	VSS	L41
BH18		L43
BH22		L45
BH26		N7
BH28		N9
BH30		N11
BH32		N13
BH34		N21
BH38		N23
BH42		N25
BH44		N29
BH46		N31
BH48		N34
BK10		N39
BK14		N41
BK18		N43
BK22		N45
BK26		P2
BK30		P4
BK32		P48
BK34		P50
BK38		R17
BK42		R21
BK46		R31
D6		R37
D10		T7
D14		T9
D18		T11
D22		T13
D26		T41
D30		T43
D34		T45
D38		U31
D42		U49
D46		V2
F2		V4
F4		V7
F48		V9
F50		V11
G7		V15
G9		V17
G11		V27
G13		V29
G16		V33
G18		V35
G21		V41
G23		V43
G25		V45
G27		V48
G29		Y15
G31		Y17
G34		Y33
G36		Y35
		Y37

SYNC MASTER=J30 MLB SYNC DATE=07/27/2011

PAGE TITLE
PCH GROUNDS

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DRAWING NUMBER 051-9277 SIZE D
REVISION 2.8.0
BRANCH
PAGE 23 OF 109
SHEET 21 OF 73

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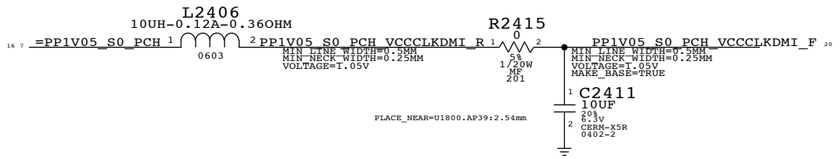

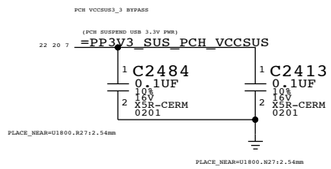

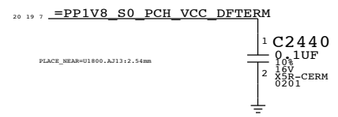

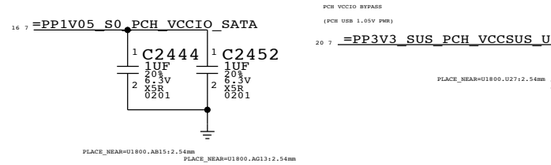

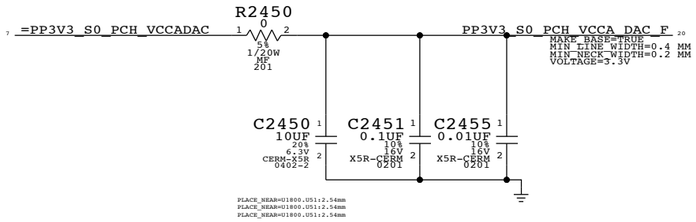

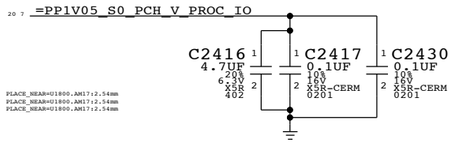

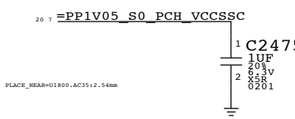

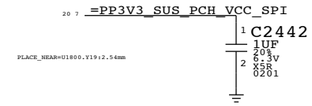

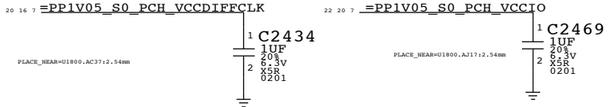

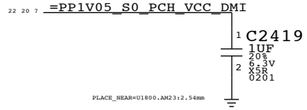

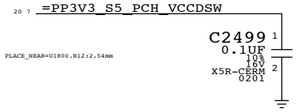

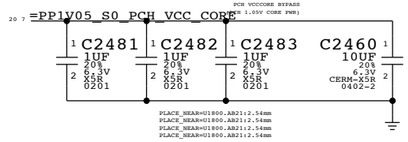

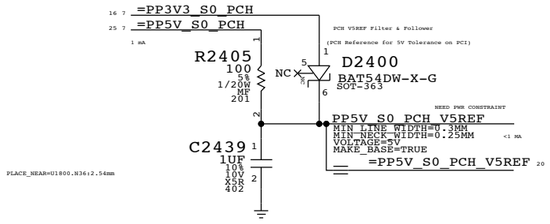

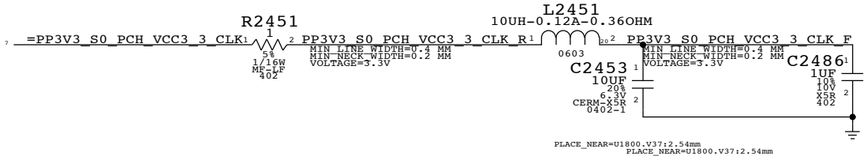

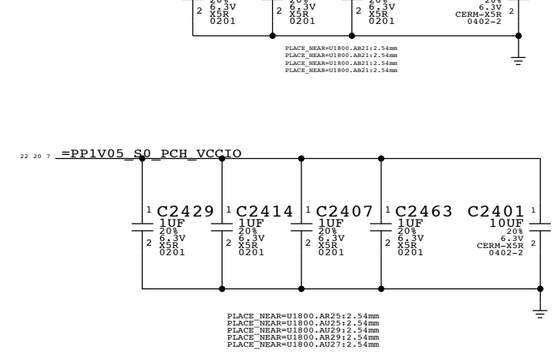

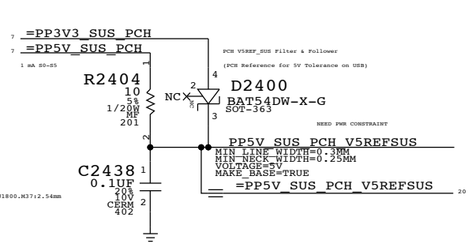

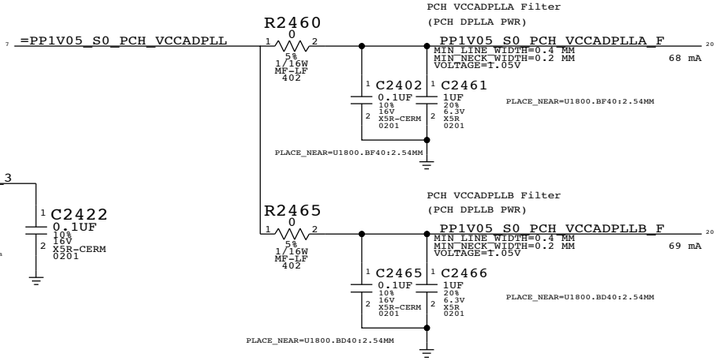

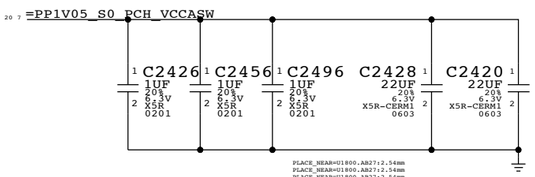

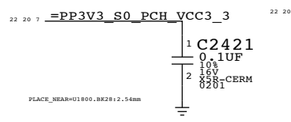

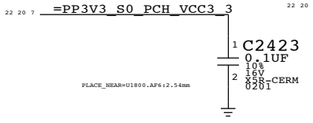

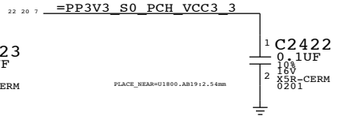

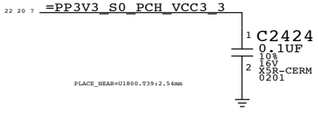

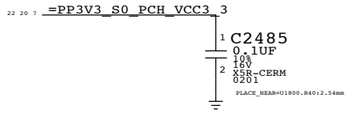

SYNC MASTER=J11 MLB
SYNC DATE=10/03/2011

PAGE TITLE

PCH DECOUPLING

Apple Inc.

DRAWING NUMBER 051-9277
SIZE D
REVISION 2.8.0
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PAGE 24 OF 109
SHEET 22 OF 73

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CPU Micro2-XDP

=PPVCCIO_S0_XDP

=PP3V3_S0_XDP
NO STUFF
R2540 1K 5% 1/16W MF-LF 402

CRITICAL
XDP_CONN
J2500
DF40RC-60DP-0.4V
M-ST-SM1
518S0047

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

(R2560–R2563)
XDP_CPU:BPM

XDP_BPM_L<4>	R2560	0	PLACE_SIDE=BOTTOM
XDP_BPM_L<5>	R2561	0	PLACE_SIDE=BOTTOM
XDP_BPM_L<6>	R2562	0	
XDP_BPM_L<7>	R2563	0	

(R2564–R2567)
XDP_CPU:CFG

CPU_CFG<12>	R2564	0
CPU_CFG<13>	R2565	0
CPU_CFG<14>	R2566	0
CPU_CFG<15>	R2567	0

CPU_PWRGD	R2500	1K	PLACE_NEAR=U1000.B46:2.54mm
PM_PWRBTN_L	R2502	0	PLACE_NEAR=U4900.J3:2.54mm
CPU_CFG<0>	R2501	1K	PLACE_NEAR=U1000.B50:2.54mm
PM_PCH_SYS_PWROK	R2504	330	

J2500 pin			
OBSFN_A0	XDP_CPU_PREQ_L	OBSFN_C0	CPU_CFG<16>
OBSFN_A1	XDP_CPU_PRDY_L	OBSFN_C1	CPU_CFG<17>
OBSDATA_A0	XDP_BPM_L<0>	OBSDATA_C0	CPU_CFG<0>
OBSDATA_A1	XDP_BPM_L<1>	OBSDATA_C1	CPU_CFG<1>
OBSDATA_A2	XDP_BPM_L<2>	OBSDATA_C2	CPU_CFG<2>
OBSDATA_A3	XDP_BPM_L<3>	OBSDATA_C3	CPU_CFG<3>
OBSFN_B0	CPU_CFG<10>	OBSFN_D0	CPU_CFG<8>
OBSFN_B1	CPU_CFG<11>	OBSFN_D1	CPU_CFG<9>
OBSDATA_B0	XDP_OBSDATA_B<0>	OBSDATA_D0	CPU_CFG<4>
OBSDATA_B1	XDP_OBSDATA_B<1>	OBSDATA_D1	CPU_CFG<5>
OBSDATA_B2	XDP_OBSDATA_B<2>	OBSDATA_D2	CPU_CFG<6>
OBSDATA_B3	XDP_OBSDATA_B<3>	OBSDATA_D3	CPU_CFG<7>
PWRGD/HOOK0	XDP_CPU_PWRGD	ITPCLK/HOOK4	XDP_CPU_CLK100M_P
HOOK1	XDP_CPU_PWRBTN_L	ITPCLK#/HOOK5	XDP_CPU_CLK100M_N
VCC_OBS_AB		VCC_OBS_CD	
HOOK2	XDP_CPU_CFG<0>	RESET#/HOOK6	XDP_CPURST_L
HOOK3	XDP_VR_READY	DBR#/HOOK7	XDP_DBRESET_L
SDA	=SMBUS_XDP_SDA	TDO	XDP_CPU_TDO
SCL	=SMBUS_XDP_SCL	TRSTn	XDP_CPU_TRST_L
TCK1		TDI	XDP_CPU_TDI
TCK0	XDP_CPU_TCK	TMS	XDP_CPU_TMS
NC		XDP_PRESENT#	

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP_CPU_TDO	R2510	51	PLACE_NEAR=J2500.52:2.54mm
XDP_CPU_TDI	R2511	51	PLACE_NEAR=U1000.M60:2.54mm
XDP_CPU_TMS	R2512	51	PLACE_NEAR=U1000.L55:2.54mm
XDP_CPU_TCK	R2513	51	PLACE_NEAR=U1000.L56:2.54mm
XDP_CPU_TRST_L	R2514	51	PLACE_NEAR=U1000.J58:2.54mm

R2515	0	XDP_CPU_CLK100M_P	PLACE_NEAR=R1841.1:2.54mm
R2516	0	XDP_CPU_CLK100M_N	PLACE_NEAR=R1840.1:2.54mm
R2505	1K	XDP_DBRESET_L	PLACE_NEAR=U1000.D44:2.54mm

C2500 0.1UF 10% 16V X7R-CERM 0402
C2501 0.1UF 10% 16V X7R-CERM 0402

XDP SIGNALS

(R2520–R2537)

XDP_DA0_USB_EXTA_OC_L	R2520	33	XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L
XDP_DA1_USB_EXTB_OC_L	R2521	33	XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L
XDP_DA2_USB_EXTC_OC_L	R2522	33	XDP_DA2_PCH_GPIO41_USB_EXTC_OC_L
XDP_DA3_USB_EXTD_OC_L	R2523	33	XDP_DA3_PCH_GPIO42_USB_EXTD_OC_L
XDP_DB0_USB_EXTB_OC_EHCI_L	R2524	33	XDP_DB0_PCH_GPIO43_USB_EXTB_OC_EHCI_L
XDP_DB1_USB_EXTD_OC_EHCI_L	R2525	33	XDP_DB1_PCH_GPIO9_USB_EXTD_OC_EHCI_L
XDP_DB2_AP_PWR_EN	R2526	33	XDP_DB2_PCH_GPIO10_AP_PWR_EN
XDP_DB3_SDCONN_STATE_CHANGE	R2527	33	XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE
XDP_FC0	R2528	33	XDP_FC0_PCH_GPIO15
XDP_FC1	R2529	33	XDP_FC1_PCH_GPIO0
XDP_DC0_ISOLATE_CPU_MEM_L	R2530	33	XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L
XDP_DC1_MXM_GOOD	R2531	33	XDP_DC1_PCH_GPIO35_MXM_GOOD
XDP_DC2_DP_AUXCH_ISOL	R2532	33	XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL
XDP_DC3_SATARDRVR_EN	R2533	33	XDP_DC3_PCH_GPIO19_SATARDRVR_EN
XDP_DD0_DP_GPU_TBT_SEL	R2534	33	XDP_DD0_PCH_GPIO36_DP_GPU_TBT_SEL
XDP_DD1_JTAG_ISP_TCK	R2535	33	XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK
XDP_DD2_AUD_IPHS_SWITCH_EN	R2536	33	XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH
XDP_DD3_ENET_LOW_PWR	R2537	33	XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH

R2581 1K 1/20W 5% MF 201
R2580 1K 1/20W 5% MF 201

PCH SIGNALS

XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L	R2590	0	USB_EXTA_OC_L
XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L	R2592	0	USB_EXTB_OC_L
XDP_DB2_PCH_GPIO10_AP_PWR_EN	R2596	0	AP_PWR_EN
XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE	R2597	0	SDCONN_STATE_RST_L
XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L	R2570	0	ISOLATE_CPU_MEM_L
XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL	R2572	0	DP_AUXCH_ISOL
XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK	R2575	0	JTAG_ISP_TCK
XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH	R2576	0	AUD_IPHS_SWITCH_EN_PCH
XDP_FC1_PCH_GPIO0	R2574	1K	TBT_CIO_PLUG_EVENT_ISOL

Non-XDP Signals

PCH/XDP Signal Isolation Notes:

- Following Intel's Debug Prot Design Guid for HR and CR v1.3 doc id 404081.
Initially, stuffing both 33 and 0 ohms and validate whether it is functional in that state, else add BOM options.
- For isolated GPIOs:
  - 'Output' non-XDP signals require pulls.
  - 'Output' PCH/XDP signals require pulls.

R252x, R253x, R257x and R259x should be placed where signal path needs to split between route from PCH to J2550 and path to non-XDP signal destination.

PCH Micro2-XDP

=PP3V3_S5_XDP

CRITICAL
XDP_CONN
J2550
DF40RC-60DP-0.4V
M-ST-SM1
518S0847

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

J2550 pin			
OBSFN_A0	TP_XDP_PCH_OBSFN_A<0>	OBSFN_C0	XDP_FC0
OBSFN_A1	TP_XDP_PCH_OBSFN_A<1>	OBSFN_C1	XDP_FC1
OBSDATA_A0	XDP_DA0_USB_EXTA_OC_L	OBSDATA_C0	XDP_DC0_ISOLATE_CPU_MEM_L
OBSDATA_A1	XDP_DA1_USB_EXTB_OC_L	OBSDATA_C1	XDP_DC1_MXM_GOOD
OBSDATA_A2	XDP_DA2_USB_EXTC_OC_L	OBSDATA_C2	XDP_DC2_DP_AUXCH_ISOL
OBSDATA_A3	XDP_DA3_USB_EXTD_OC_L	OBSDATA_C3	XDP_DC3_SATARDRVR_EN
OBSFN_B0	TP_XDP_PCH_OBSFN_B<0>	OBSFN_D0	TP_XDP_PCH_OBSFN_D<0>
OBSFN_B1	TP_XDP_PCH_OBSFN_B<1>	OBSFN_D1	TP_XDP_PCH_OBSFN_D<1>
OBSDATA_B0	XDP_DB0_USB_EXTB_OC_EHCI_L	OBSDATA_D0	XDP_DD0_DP_GPU_TBT_SEL
OBSDATA_B1	XDP_DB1_USB_EXTD_OC_EHCI_L	OBSDATA_D1	XDP_DD1_JTAG_ISP_TCK
OBSDATA_B2	XDP_DB2_AP_PWR_EN	OBSDATA_D2	XDP_DD2_AUD_IPHS_SWITCH_EN
OBSDATA_B3	XDP_DB3_SDCONN_STATE_CHANGE	OBSDATA_D3	XDP_DD3_ENET_LOW_PWR
PWRGD/HOOK0	XDP_PCH_S5_PWRGD	ITPCLK/HOOK4	TP_XDP_PCH_HOOK4
HOOK1	XDP_PCH_PWRBTN_L	ITPCLK#/HOOK5	TP_XDP_PCH_HOOK5
VCC_OBS_AB		VCC_OBS_CD	
HOOK2	TP_XDPPCH_HOOK2	RESET#/HOOK6	XDPPCH_PLTRST_L
HOOK3	TP_XDPPCH_HOOK3	DBR#/HOOK7	XDP_DBRESET_L
SDA	=SMBUS_XDP_SDA	TDO	XDP_PCH_TDO
SCL	=SMBUS_XDP_SCL	TRSTn	TP_XDP_PCH_TRST_L
TCK1		TDI	XDP_PCH_TDI
TCK0	XDP_PCH_TCK	TMS	XDP_PCH_TMS
NC		XDP_PRESENT#	

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

ALL_SYS_PWRGD	R2584	1K	PLACE_NEAR=J2550.50:2.54mm
PM_PWRBTN_L	R2585	0	PLACE_NEAR=U4900.J3:2.54mm

C2580 0.1UF 10% 16V X7R-CERM 0402
C2581 0.1UF 10% 16V X7R-CERM 0402

=PP1V05_SUS_PCH_JTAG

XDP_PCH_TDO	R2550	51	PLACE_NEAR=J2550.51:2.54mm
XDP_PCH_TDI	R2551	51	PLACE_NEAR=U1800.U12:2.54mm
XDP_PCH_TMS	R2552	51	PLACE_NEAR=U1800.M15:2.54mm
XDP_PCH_TCK	R2556	51	PLACE_NEAR=U1800.M17:2.54mm

1K series R on PCH Support Page

SYNC MASTER=J13 MLB NON POR SYNC DATE=10/17/2011

PAGE TITLE: CPU & PCH XDP

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DRAWING NUMBER: 051-9277 SIZE: D
REVISION: 2.8.0
BRANCH:
PAGE: 25 OF 109
SHEET: 23 OF 73

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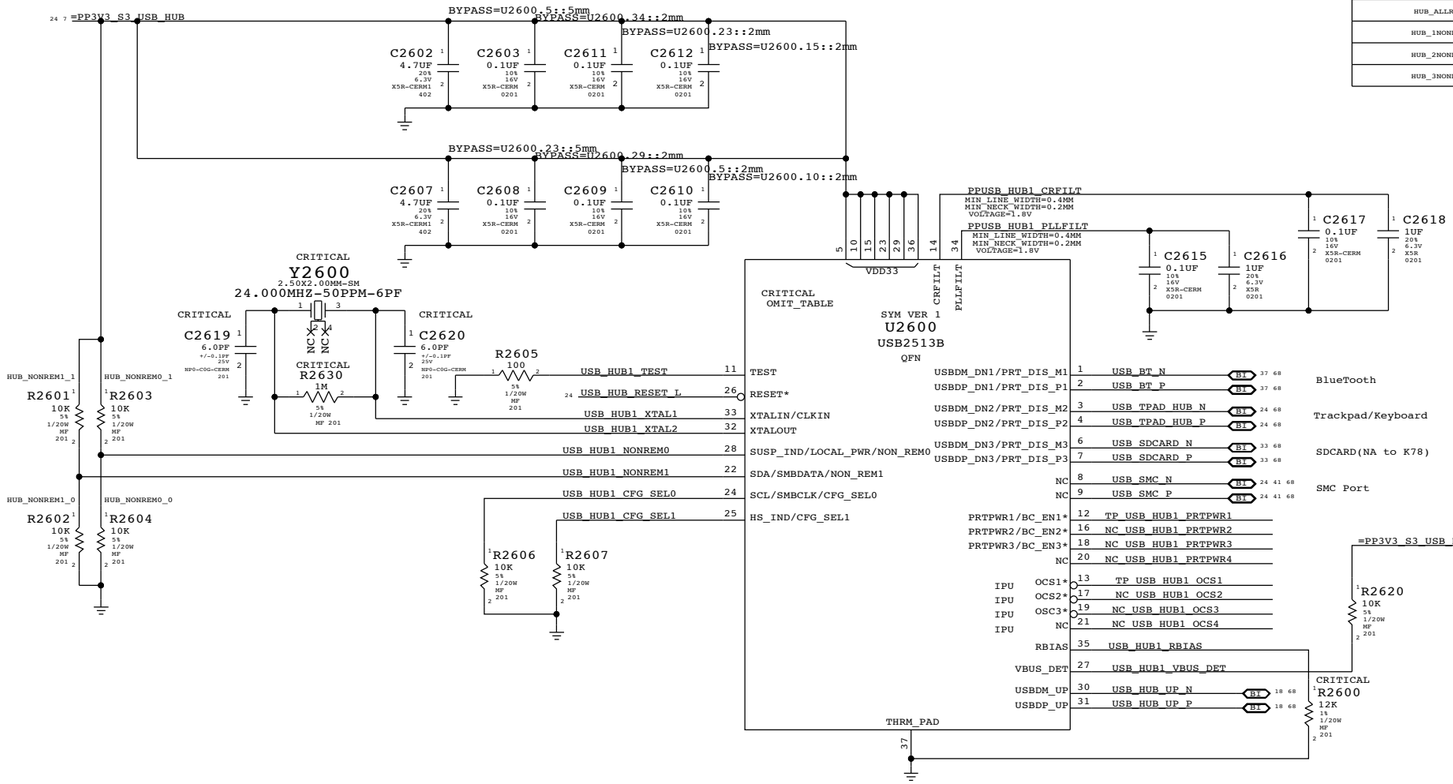
BOM GROUP	BOM OPTIONS
HUB_ALLREM	HUB_NONREM1_0,HUB_NONREM0_0
HUB_1NONREM	HUB_NONREM1_0,HUB_NONREM0_1
HUB_2NONREM	HUB_NONREM1_1,HUB_NONREM0_0
HUB_3NONREM	HUB_NONREM1_1,HUB_NONREM0_1

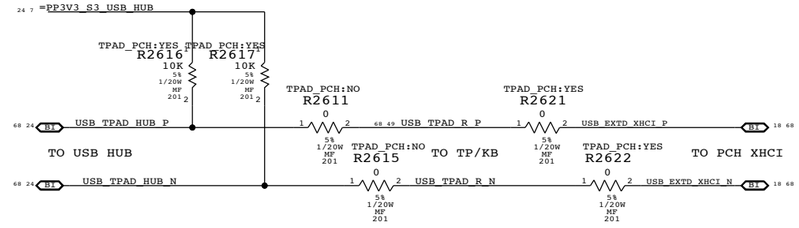
NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

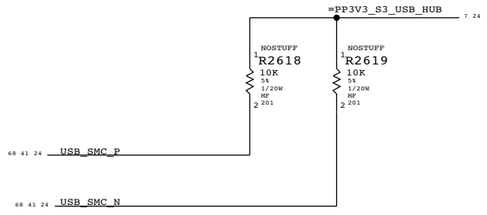
BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0983	1	IC,USB2512B,USB 2.0 HUB CNTRL,36-QFN	U2600	CRITICAL	USBHUB2512B
338S0923	1	IC,USB2513B,USB 2.0,HUB CNTRL,3PRT,36QFN	U2600	CRITICAL	USBHUB2513B
338S0824	1	IC,USB2514B,USB 2.0,HUB CNTRL,4PRT	U2600	CRITICAL	USBHUB2514B

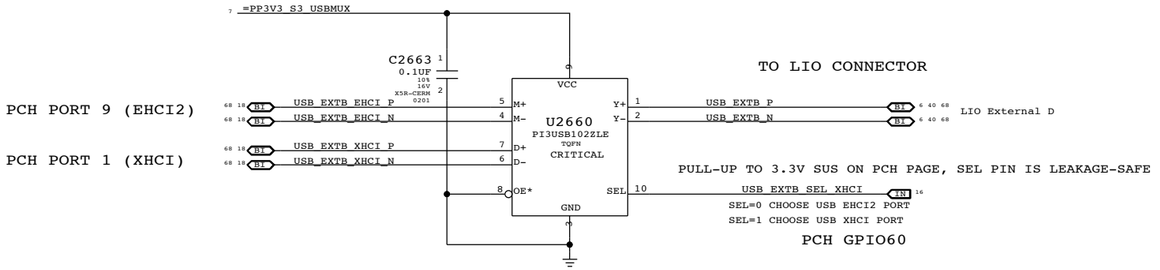


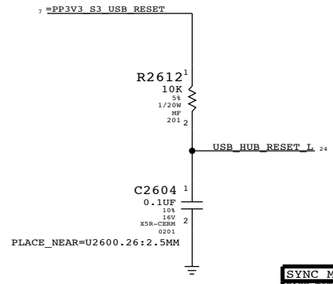
TO CONNECT TP/KB TO PCH XHCI
NOSTUFF R2611 & R2615, STUFF R2621 & R2622,R2616 & R2617





USB XHCI/EHCI2 PORT MUX FOR EXT B





SYNC_MASTER=J13_MLB_NON_POR SYNC_DATE=11/10/2011

PAGE TITLE
USB HUB & MUX

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D
REVISION 2.8.0
BRANCH
PAGE 26 OF 109
SHEET 24 OF 73

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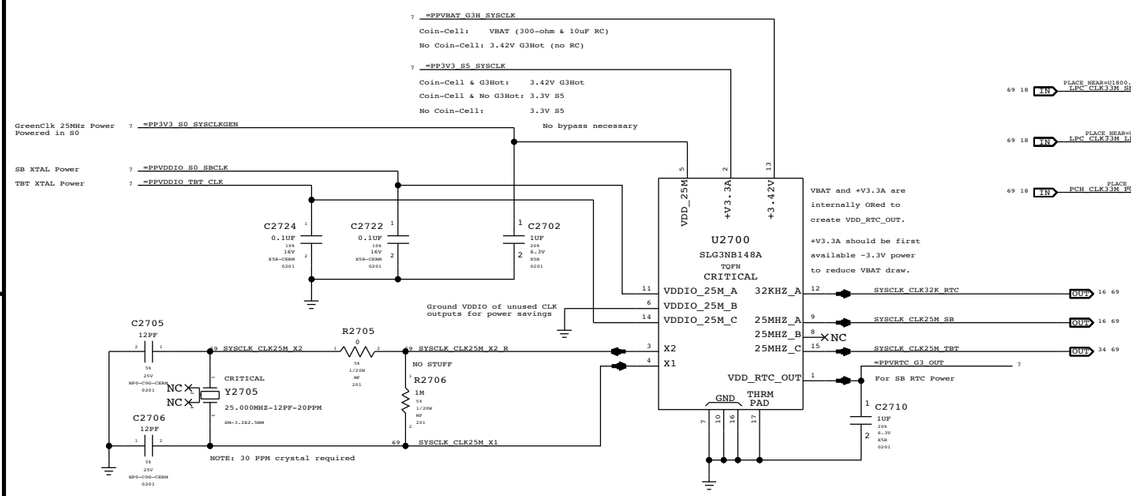
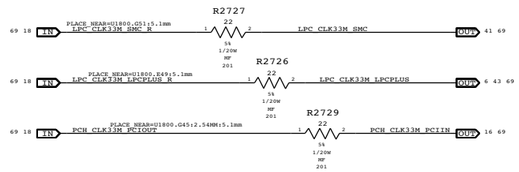
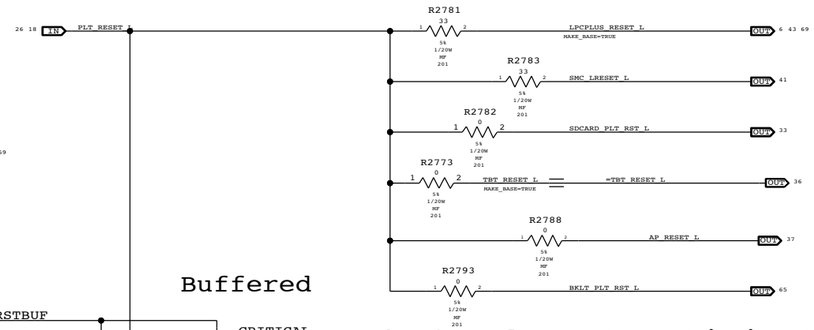
System RTC Power Source & 32kHz / 25MHz Clock Generator





Platform Reset Connections

Unbuffered



Buffered

=PP3V3_S0_RSTBUF

CRITICAL
MC74VHC1G08
SC70-HF
U2771
C2771 0.1UF
R2770 100K
PLT_RST_BUF_L
R2772 0
SSD_RESET_L
XDP
R2789 1K
XDPPCH_PLTRST_L
R2771 0
PCA9557D_RESET_L

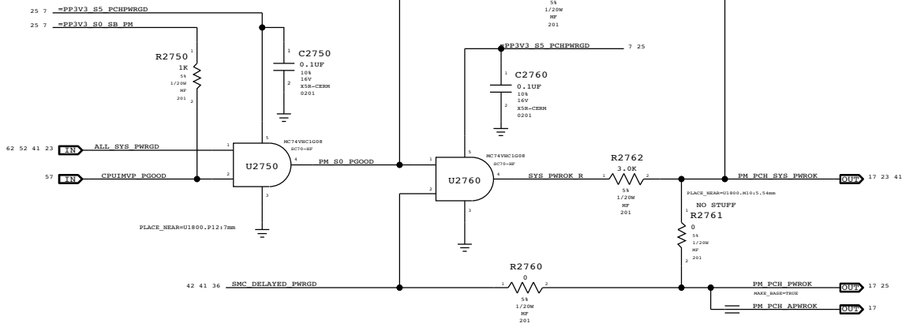
Buffered

=PP3V3_S0_RSTBUF

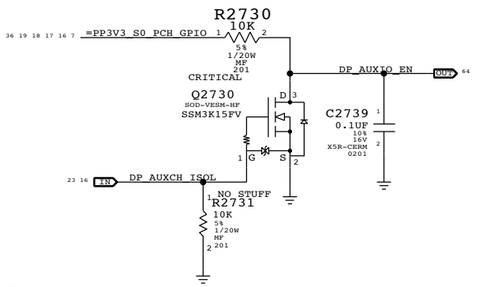
U2780
74LVC1G07
SC70
NC
C2780 0.1UF
R2780 100K
PLT_RST_CPU_BUF_L
MAKE_BASE=TRUE
CPU_RESET_L
VTT voltage divider on CPU page

Scrub for layout optimization

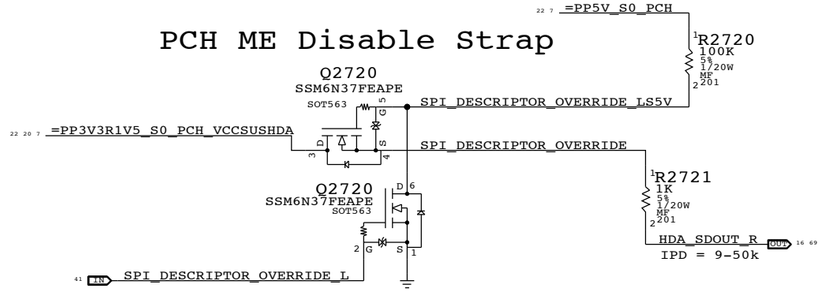
PCH S0 PWRGD



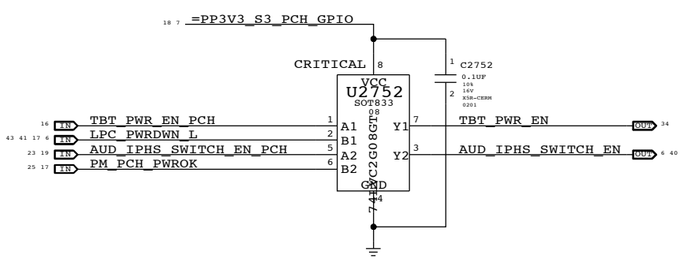
DP_AUXIO_EN Inversion



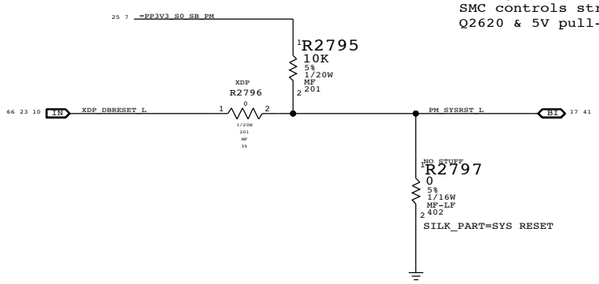
PCH ME Disable Strap



GPIO Glitch Prevention



PCH Reset Button



PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q2620 & 5V pull-up allows circuit to work regardless of HDA voltage.

SYNC_MASTER=K21_MLB SYNC_DATE=07/29/2011

PAGE TITLE

Clock (CK505) and Chipset Support

Apple Inc.

DRAWING NUMBER	051-9277
SIZE	D
REVISION	2.8.0
BRANCH	
PAGE	27 OF 109
SHEET	25 OF 73

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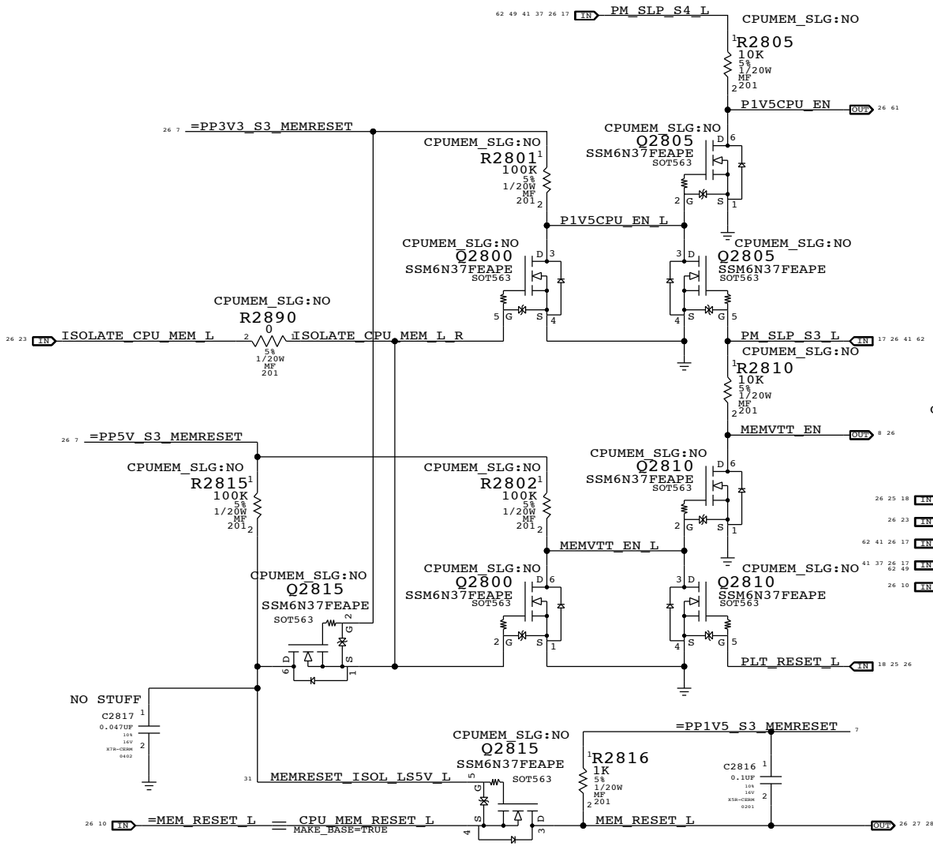
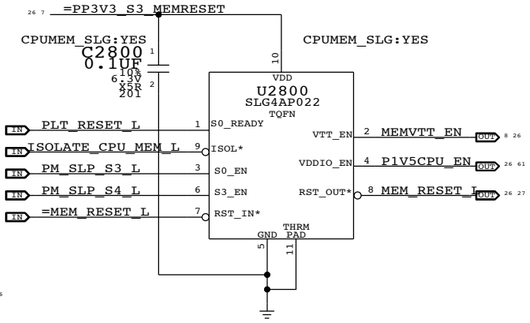
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well
as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L



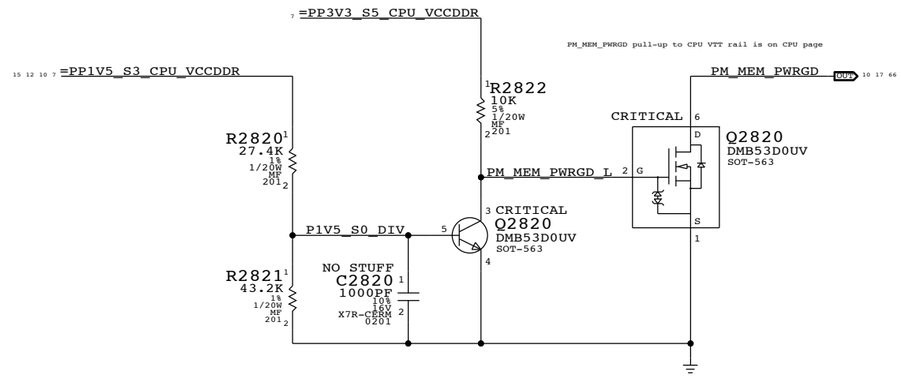


Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
1	0	1	1	1	1	1	1	1
to 2	0	0	1	1	1	1	0	1
3	0	0	0	1	X	1	0	0
S3 4	0	0	1	1	X	1	0	1
to 5	0	1	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
S0 7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

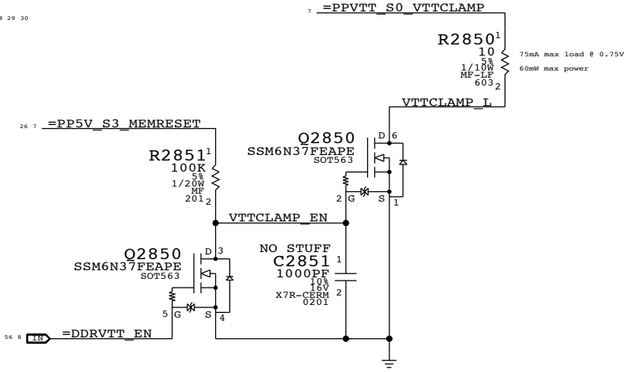
NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



SYNC_MASTER=J13_MLB_NON_POR SYNC_DATE=11/10/2011

PAGE TITLE
CPU Memory S3 Support

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D
REVISION 2.8.0
BRANCH
PAGE 28 OF 109
SHEET 26 OF 73

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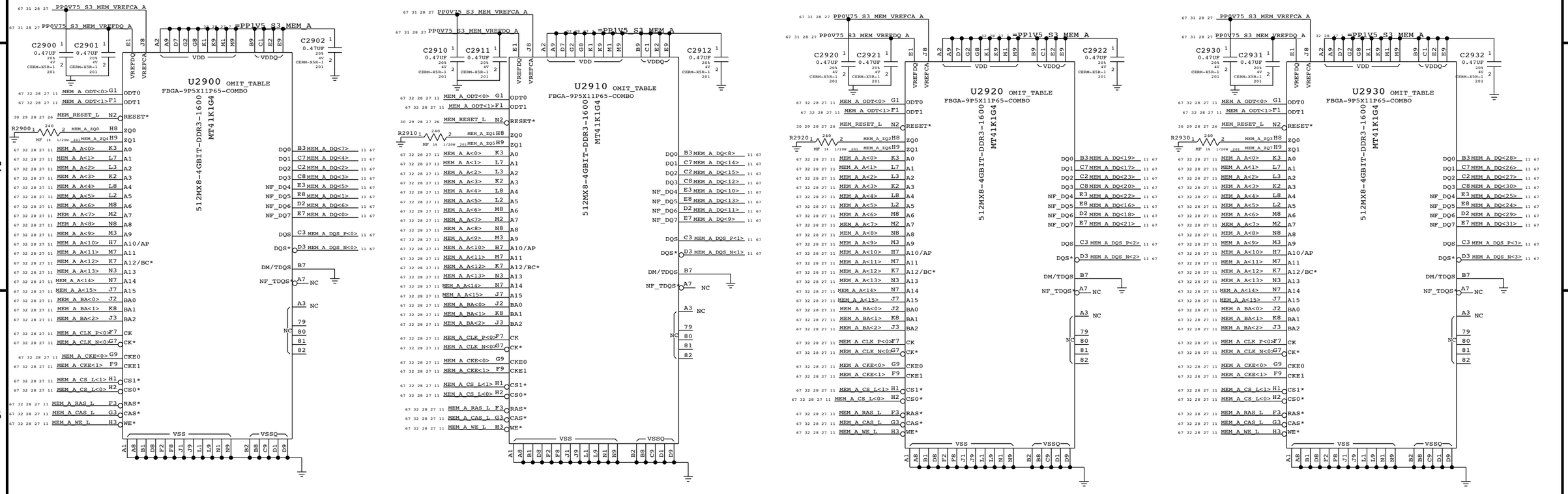
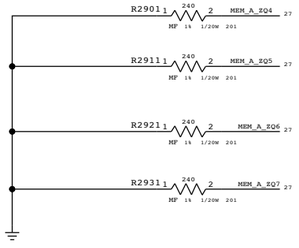


A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL



SYNC MASTER=K21 MLB
SYNC DATE=07/28/2011

PAGE TITLE
DDR3 DRAM CHANNEL A (0-31)

Apple Inc.

DRAWING NUMBER 051-9277
SIZE D
REVISION 2.8.0
BRANCH
PAGE 29 OF 109
SHEET 27 OF 73

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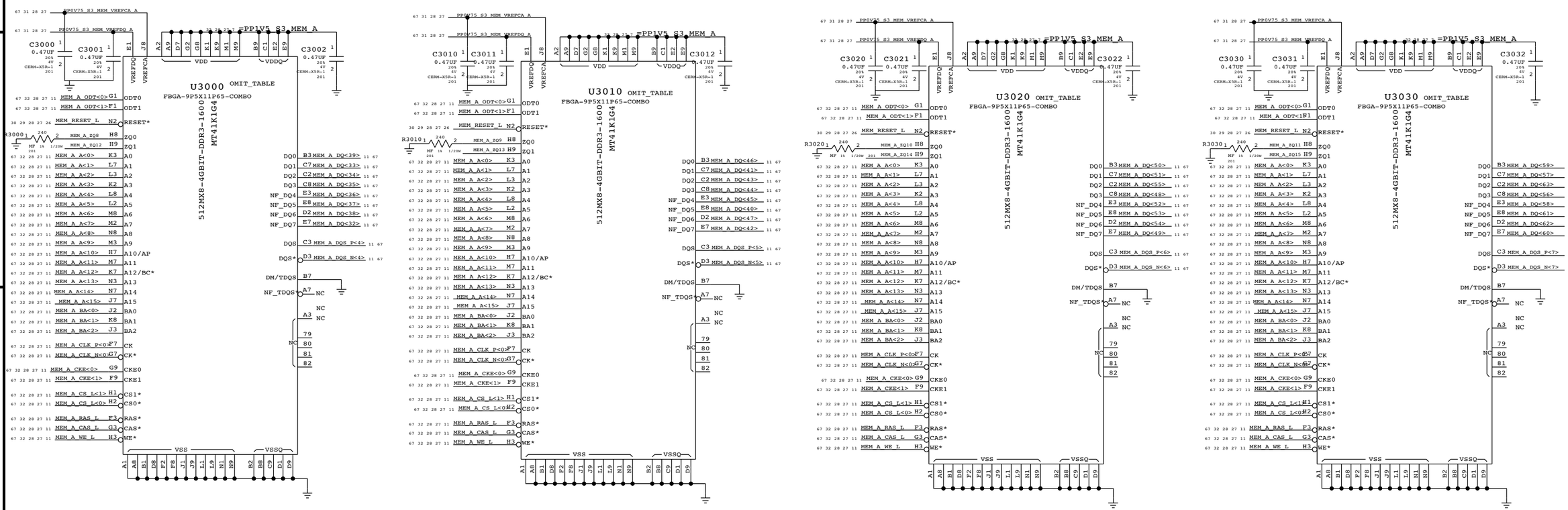

SYNC MASTER=K21 MLB — SYNC DATE=07/28/2011

PAGE TITLE

DDR3 DRAM CHANNEL A (32-63)

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REVISION 2.8.0

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PAGE 30 OF 109

SHEET 28 OF 73

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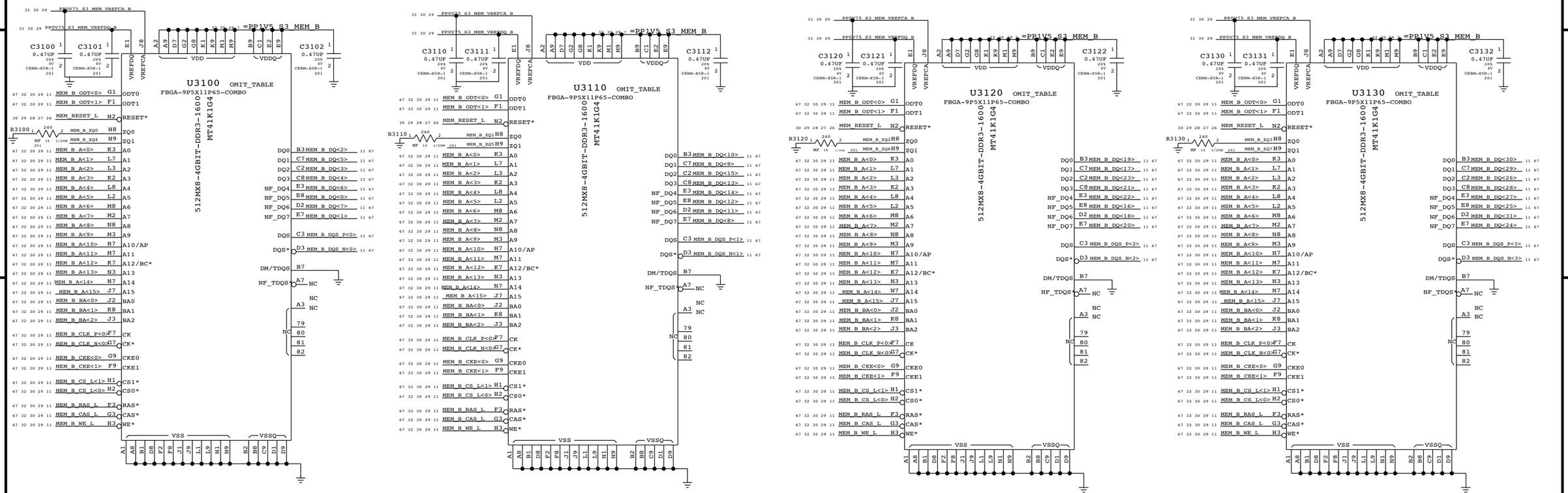
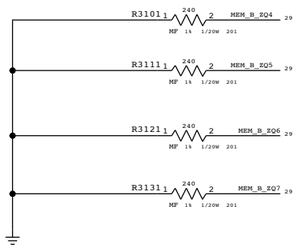


A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL



SYNC MASTER=K21 MLB
SYNC DATE=07/28/2011

PAGE TITLE
DDR3 DRAM CHANNEL B (0-31)

Apple Inc.

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SIZE D
REVISION 2.8.0
BRANCH
PAGE 31 OF 109
SHEET 29 OF 73

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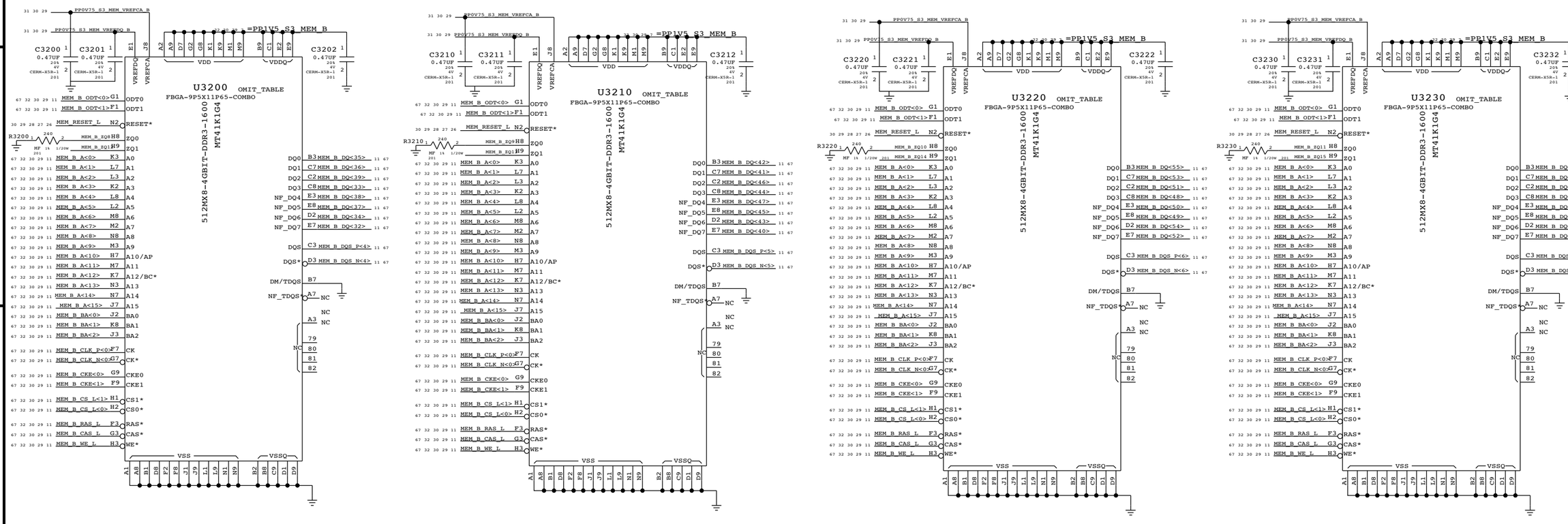
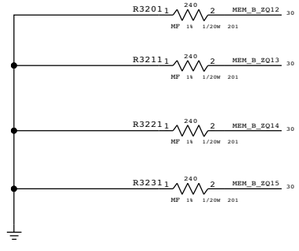


A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL



SYNC_MASTER=K21_MLB SYNC_DATE=07/28/2011

PAGE TITLE
DDR3 DRAM CHANNEL B (32-63)

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DRAWING NUMBER 051-9277
SIZE D
REVISION 2.8.0
BRANCH
PAGE 32 OF 109
SHEET 30 OF 73

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Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
DDRVREF_DAC - Stuffs Apple margining circuit.
VREFDQ:LDO - LDO outputs sent to DQ inputs.
VREFDQ:LDO_DAC - Margined LDO outputs sent to DQ inputs.
VREFDQ:M1_M3 - CPU margined DDR voltage divider sent to DQ inputs.
VREFDQ:M1_DAC - DAC margined DDR voltage divider sent to DQ inputs.
VREFCA:LDO - LDO outputs sent to CA inputs.
VREFCA:LDO_DAC - DAC margined LDO outputs sent to CA inputs.

NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.

NOTE: MEMVREG and FRAMEBUF share a DAC output, cannot enable both at the same time!

RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11780002	1	RES,MF,1/20W,0.0 OHM,5,0201,SMD	R3303,R3360		VREFDQ:LDO
11780002	2	RES,MF,1/20W,0.0 OHM,5,0201,SMD	R3309,R3305		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11880012	4	RES,MF,1KOHM,1,1/20W,0201	R3321,R3322,R3311,R3312		VREFDQ:M1_DAC
11880303	1	RES,MF,332OHM,1,1/20W,0201	R3304		VREFDQ:M1_DAC

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=J11_MLB SYNC_DATE=08/04/2011

PAGE TITLE
FSB/DDR3/FRAMEBUF Vref Margining

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D
REVISION 2.8.0
BRANCH
PAGE 33 OF 109
SHEET 31 OF 73

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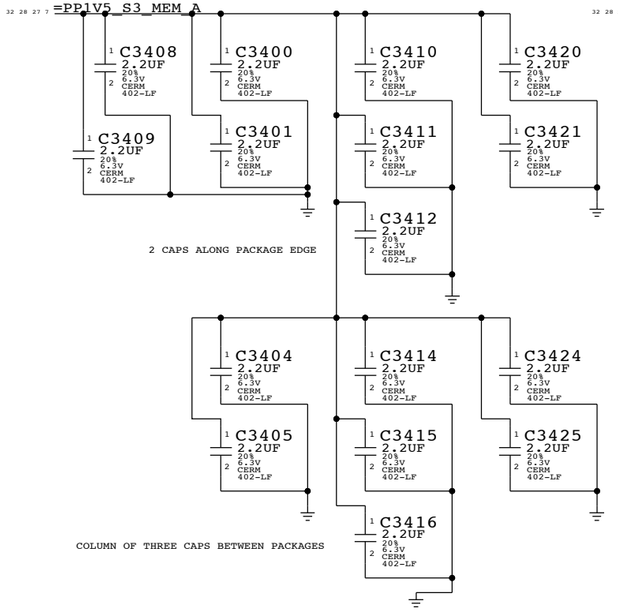
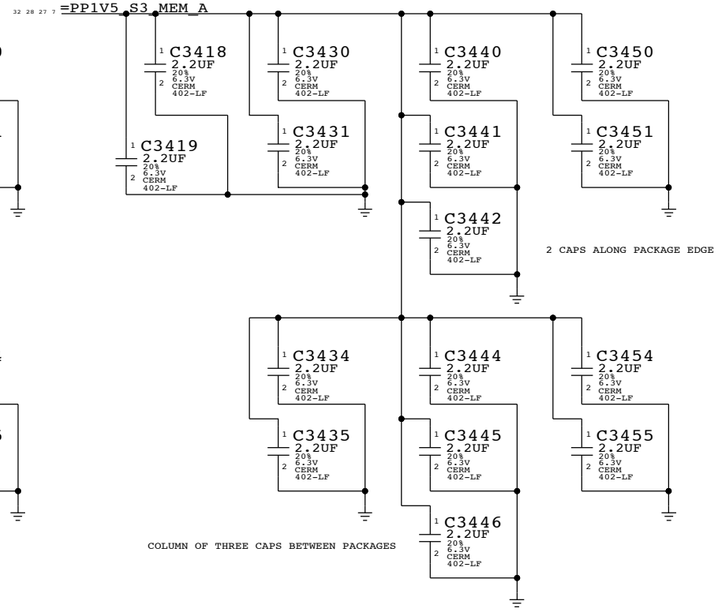
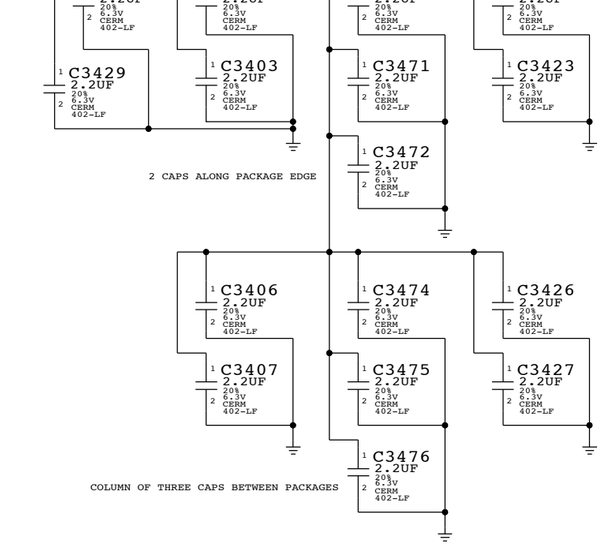
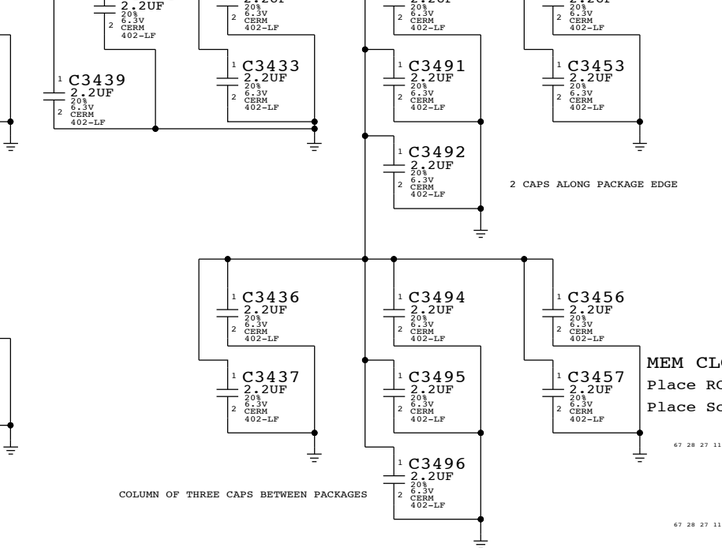
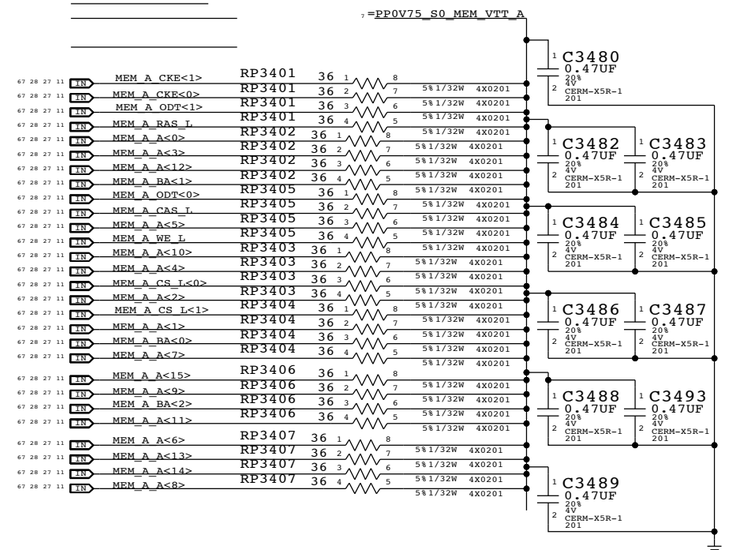


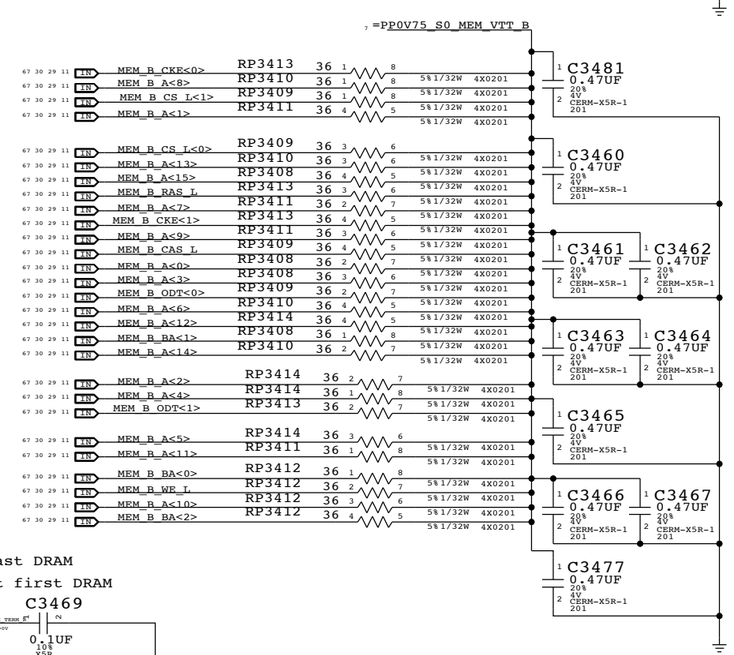






JEDEC recommends 30 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE

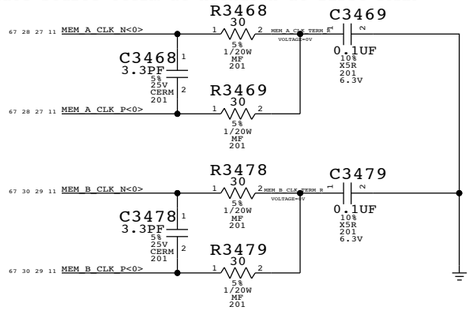




MEM CLOCK TERMINATION

Place RC end termination after last DRAM

Place Source Cterm at neckdown at first DRAM



SYNC MASTER=K21 MLB | SYNC DATE=07/28/2011

PAGE TITLE

DDR3 Bypassing/Termination

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REVISION 2.8.0

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PAGE 34 OF 109

SHEET 32 OF 73

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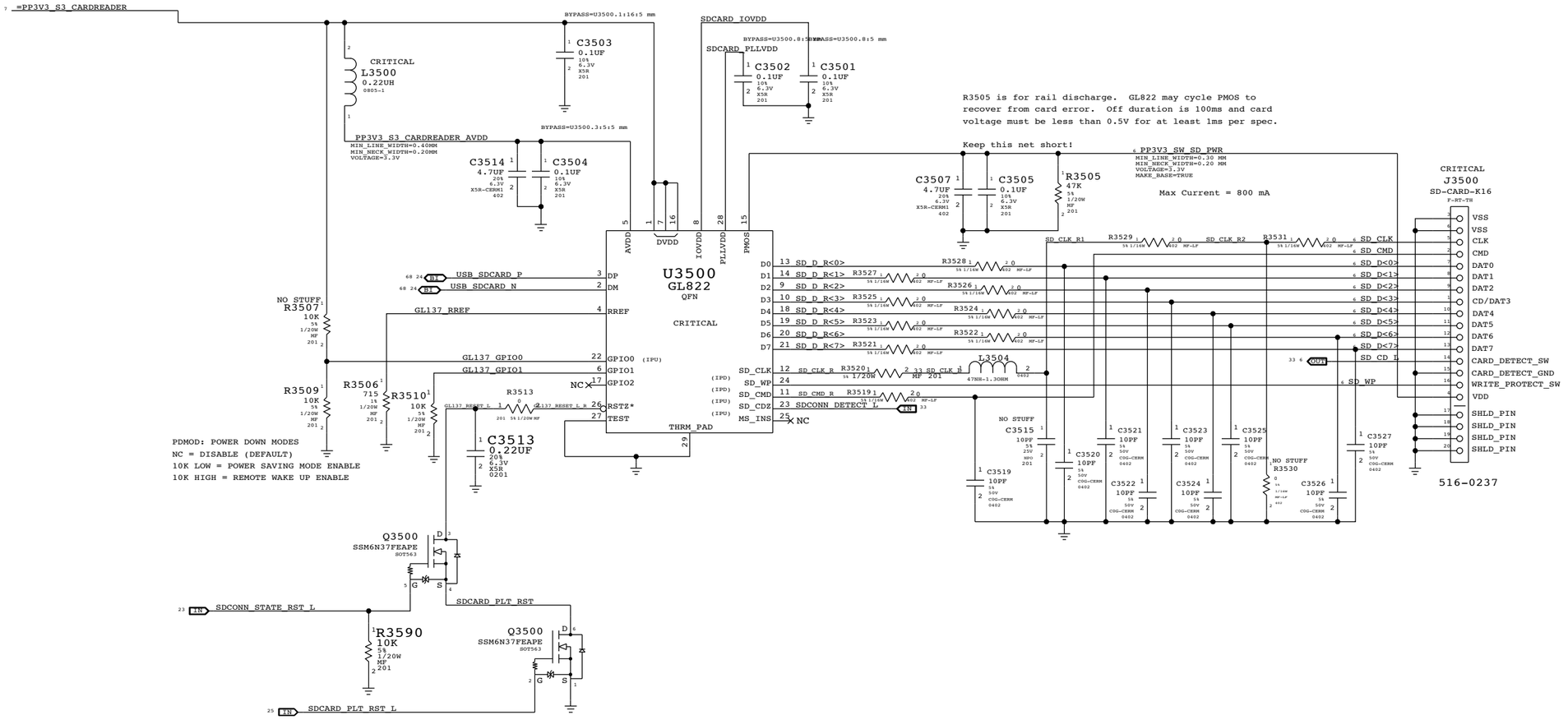
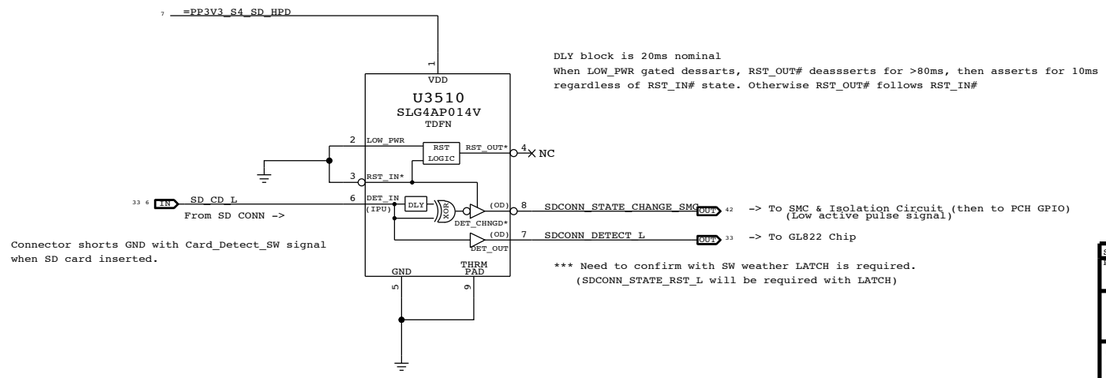


SD Detect & Reset Logic

SDCONN_DETECT Debounce, Inversion, Detect-Changed PCH GPIO Latch Circuit
Converts SDCONN from active-low level signal to active-high pulses
RESET_IN* musts be pulled to GND if not used. SD detect logic will only function if Reset logic is low.



SYNC MASTER=J13 MLB NON POR | SYNC DATE=11/10/2011

PAGE TITLE: SecureDigital Card Reader

Apple Inc.

DRAWING NUMBER: 051-9277 | SIZE: D

REVISION: 2.8.0

BRANCH:

PAGE: 35 OF 109

SHEET: 33 OF 73

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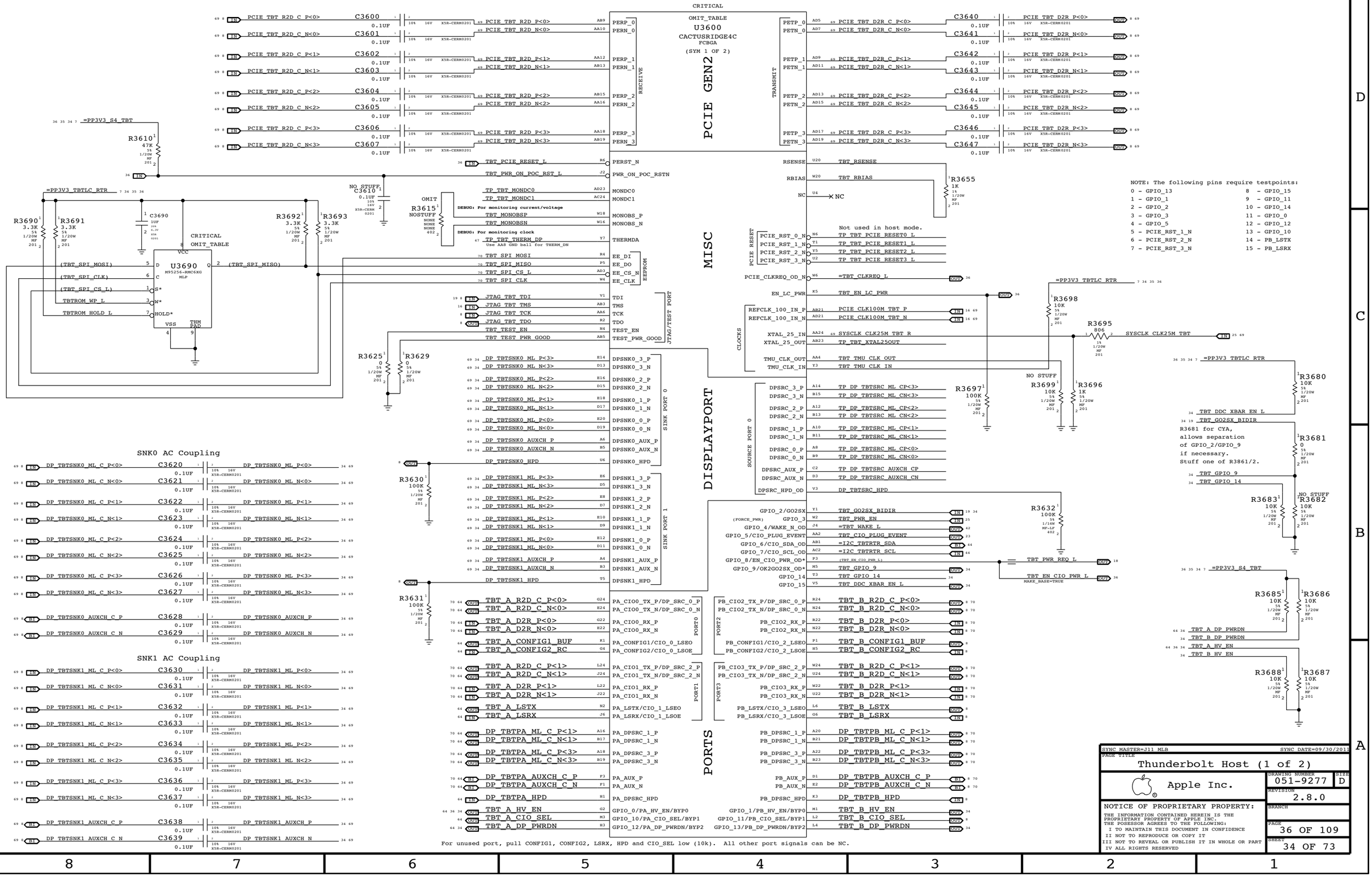

SYNC MASTER=J11 MLB | SYNC DATE=09/30/2011

PAGE TITLE: Thunderbolt Host (1 of 2)

Apple Inc.

DRAWING NUMBER: 051-9277 | SIZE: D

REVISION: 2.8.0

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PAGE: 36 OF 109

SHEET: 34 OF 73

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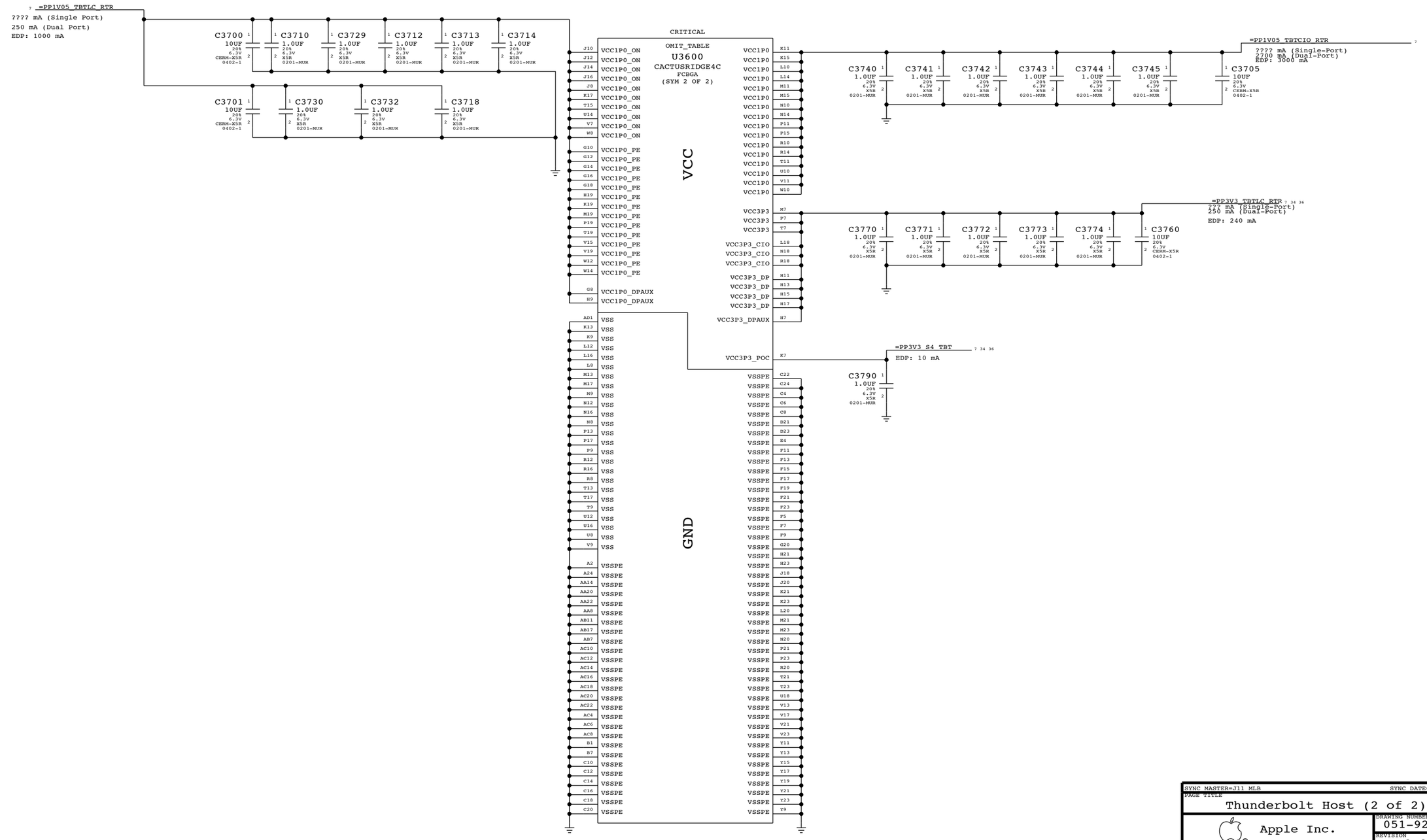

SYNC MASTER=J11 MLB SYNC DATE=10/04/2011

PAGE TITLE

Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

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PAGE 37 OF 109

SHEET 35 OF 73

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Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP18V_TBT_REG (18V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBT_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBT_FET (1.05V FET Output)

Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
TBTBST:Y - Stuffs 18V boost circuitry.

TBT 15V Boost Regulator

CRITICAL

Q3880
SI8409DB
BGA

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

=PPVIN_SW_TBTBST
8-13V Input
Changes required
for 2S.

R3880 470K 5% 1/20W MF 201
C3880 0.1UF 10% 25V X5R 402
TBTBST_PWREN_DIV_L
R3881 150K 5% 1/20W MF 201
TBTBST_PWREN_L
Q3805 SSM3K15FV SOD-VESM-HF
TBT_A_HV_EN

PPVIN_SW_TBTBST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here, add property on another page.

C3890 10UF 20% 25V X5R-CERM 0603
C3891 10UF 20% 25V X5R-CERM 0603
R3891 200K 1% 1/20W MF 201 <R1>
TBTBST_EN_UVLO

L3895 6.8UH-4.0A PIMB062D-SM
TBTBST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

U3890 LT3957 QFN
VIN
SW
SNS1
SNS2
EN/UVLO
INTVCC
VC
RT
SS
SYNC
FBX
NC
SGND
GND

TBTBST_SNS1
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
R3889 0 5% 1/20W MF 201
CRITICAL
D3895 POWERDI-123 DFLS230L
TBTBST_SNS2
R3890 49.9K 1% 1/16W MF-LF 402
TBTBST_VSNS
XW3895 SH
=PLACE_NEAR=C3895.1:2 mm

TBTBST_INTVCC
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
C3892 4.7UF 10% 10V X5R 805

TBTBST_VC
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
C3887 47PF 5% 25V CERM-COG-CERM 0201
R3893 10K 1% 1/20W MF 201
TBTBST_VC_RC
C3893 3300PF 10% 10V X7R-CERM 0201

TBTBST_RT
R3894 41.2K 1% 1/20W MF 201

TBTBST_SS
C3894 0.33UF 10% 6.3V CERM-X5R 402

GND_TBTBST_SGND
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

R3892 73.2K 1% 1/20W MF 201 <R2>

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

C3888 22PF 5% 50V CERM 402
NO STUFF
C3889 100PF 5% 50V CERM 402
R3895 133K 1% 1/16W MF-LF 402 <Ra>
R3896 15.8K 1% 1/16W MF-LF 402 <Rb>

Vout = 1.6V * (1 + Ra / Rb)

Vout = 15.1V
Max Current = 1.0A
Freq = 300KHz

=PP15V_TBT_REG

C3895 10UF 20% 25V X5R-CERM 0603
C3897 10UF 20% 25V X5R-CERM 0603
C3884 10UF 20% 25V X5R-CERM 0603
C3882 10UF 20% 25V X5R-CERM 0603
C3896 10UF 20% 25V X5R-CERM 0603
C3898 10UF 20% 25V X5R-CERM 0603
C3883 10UF 20% 25V X5R-CERM 0603
C3881 10UF 20% 25V X5R-CERM 0603
C3899 0.001UF 10% 50V X7R-CERM 0402

SGND shorted to GND inside package, no XW necessary.

Supervisor & CLKREQ# Isolation

=PP3V3_S0_TBTPWRCTL

Q3840 SSM3K15AMFVAPE VESM
R3840 10K 5% 1/20W MF 201
C3800 0.1UF 10% 16V X5R-CERM 0201

TBT_EN_LC_PWR

U3800 SLG4AP016V TDFN
VDD
SENSE 0.7V
DLY
RESET*
MR*
EN
OUT (OD)
IN
GND
THRM PAD

=PP3V3_TBTLC_RTR
R3807 100K 5% 1/20W MF 201
PP1V05_TBTLC
TBT_PCIE_RESET_L
DLY = 60 ms +/- 20%
=TBT_CLKREQ_L
TBT_CLKREQ_ISOL_L
MAKE_BASE=TRUE

=TBT_RESET_L
Platform (PCIe) Reset

TBT_CLKREQ_L
Pull-up provided by SB page.

Q3888 SSM6N37FEAPE SOT563
Max Vgs: 10V
R3888 330K 5% 1/20W MF 201
TBTBST_SHDN_DIV
R3887 330K 5% 1/20W MF 201
Q3888 SSM6N37FEAPE SOT563
SMC_DELAYED_PWRGD

TBT "POC" Power-up Reset

Intel investigating whether RC is sufficient.

=PP3V3_S4_TBT
U3830 TPS3808 GFN
CRITICAL
VDD
SENSE
CT
RESET*
MR*
GND
THRM PAD
Pull-up: R3610
TBT_PWR_ON_POC_RST_L
TBTPOCRST_MR_L
TBTPOCRST_CT
C3831 0.0047UF 10% 25V CERM 0402
C3830 0.1UF 10% 16V X5R-CERM 0201
TPS3808G25
Vt = 2.33V +/- 2%
Delay = 27.3ms

=PP3V3_S0_PCH_GPIO
R3830 100K 5% 1/20W MF 201
Q3825 SSM6N37FEAPE SOT563
TBT_SW_RESET_L
C3825 330PF 10% 16V X7R-CERM 0201
WF: C value may need tuning.

3.3V TBT "LC" Switch

=PP3V3_S0_P3V3TBTFET
U3810 TPS22924 CSP
VIN VOUT
CRITICAL
ON
GND
=PP3V3_TBTLC_FET
Max Current = 2A (85C)
R3811 0 5% 1/20W MF 201
TBT_EN_LC_3V3
C3810 1.0UF 10% 6.3V X5R-CERM 0201
C3811 1.0UF 10% 6.3V X5R-CERM 0201
NO STUFF

U3810	
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

TBT_EN_LC_ISOL
R3816 36.5K 1% 1/20W MF 201

1.05V TBT "LC" Switch

TBT_EN_LC_1V05
=PP1V05_S0_P1V05TBTFET
U3815 TPS22924 CSP
VIN VOUT
CRITICAL
ON
GND
=PP1V05_TBTLC_FET
Max Current = 2A (85C)
C3815 1.0UF 10% 6.3V X5R-CERM 0201
C3816 1.0UF 10% 6.3V X5R-CERM 0201
C3816 must be 10%
RC guarantees minimum 5ms to reach 0.5V

U3815	
Part	TPS22924C
Type	Load Switch
R(on) @ 1.0V	20.3 mOhm Typ 28.6 mOhm Max

1.05V TBT "CIO" Switch

=PP1V05_S0_P1V05TBTFET
=PP3V3_TBTLC_RTR
R3820 100K 5% 1/20W MF 201
TBT_EN_CIO_PWR
U3820 TPS22920 CSP
VIN VOUT
CRITICAL
ON
GND
=PP1V05_TBTCIO_FET
Max Current = 4A (85C)
C3820 1.0UF 10% 6.3V X5R-CERM 0201
Q3825 SSM6N37FEAPE SOT563
TBT_EN_CIO_PWR_L

U3820	
Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	8 mOhm Typ 11.5 mOhm Max

SYNC_MASTER=J13_MLB_NON_POR
SYNC_DATE=11/10/2011
PAGE TITLE
TBT Power Support

Apple Inc.

DRAWING NUMBER 051-9277
SIZE D
REVISION 2.8.0
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PAGE 38 OF 109
SHEET 36 OF 73

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AIRPORT

CRITICAL
J4001
SSD-K99
F-RT-SM1

514S0335

WIFI_EVENT_L
PCIE_AP_R2D_N
PCIE_AP_R2D_C_N
C4030 0.1UF 10% 6.3V X5R 201
PCIE_AP_R2D_P
PCIE_AP_R2D_C_P
C4031 0.1UF 10% 6.3V X5R 201
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
PCIE_AP_D2R_P
PCIE_AP_D2R_N
PCIE_WAKE_L

3V S3 WLAN FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	0.750 A (EDP)

CRITICAL
R4052 0.020 1% 0.25W MF-LF 805
CRITICAL
Q4050 DMP2018LFK DFN2563-6

PP3V3_WLAN_F1 → PP3V3_WLAN_F
C4021 0.1UF 10% 6.3V X5R 201
C4020 10UF 20% 10V X5R 603
PP3V3_WLAN_B
C4050 0.1UF 10% 16V X5R-CERM 0201
P3V3WLAN_SS
C4051 0.033UF 10% 16V X5R 402
R4050 100K 5% 1/20W MF 201
R4051 10K 5% 1/20W MF 201
=PP3V3_S3_WLAN
PM_WLAN_EN_L

ISNS_AIRPORT_P
ISNS_AIRPORT_N

BLUETOOTH

USB_BT_CONN_N
USB_BT_CONN_P

PP3V3_S3RS4_BT_F
R4001 0 5% 1/16W MF-LF 402
=PP3V3_S4_BT
C4032 0.1UF 10% 6.3V X5R 201
PLACE_NEAR=J4001.18:1.5mm
R4002 0 5% 1/16W MF-LF 402
=PP3V3_S3_BT

NOSTUFF R4017 15K 1% 1/20W MF 201
BTPWR:S3 R4018 0 5% 1/20W MF 201
NOSTUFF R4015 15K 1% 1/20W MF 201
NOSTUFF R4016 15K 1% 1/20W MF 201
BTPWR:S4 R4011 0 5% 1/20W MF 201
PM_SLP_S4_L
BTMUX_SEL
NOSTUFF C4011 0.01UF 10% 16V X7R-CERM 0402

U4010 PI3USB102ZLE TQFN CRITICAL
VCC
GND
SEL
OE*
Y+
Y-
M+
M-
D+
D-
USB_BT_WAKE_P
USB_BT_WAKE_N
USB_BT_P
USB_BT_N

SEL	OUTPUT
L	USB_BT_WAKE
H	USB_BT

PP3V3_S3RS4_BT_F
C4010 0.1UF 10% 6.3V X5R 201
NOSTUFF R4014 15K 1% 1/20W MF 201
BTPWR:S4 R4012 15K 1% 1/20W MF 201
NOSTUFF R4013 15K 1% 1/20W MF 201
BTPWR:S4 Q4010 SSM3K15FV SOD-VESM-HF
=BT_WAKE_L

DLY = 60 MS +/- 20%

PP3V3_WLAN_F
R4053 100K 5% 1/20W MF 201
R4054 232K 1% 1/20W MF 201
R4055 100K 1% 1/20W MF 201
P3V3WLAN_VMON
AP_RESET_CONN_L
AP_CLKREQ_O_L

CRITICAL
U4002 SLG4AP016V TDFN
VDD
SENSE 0.7V
RESET*
DLY
MR*
EN
IN
OUT (OD)
THRM PAD
GND

=PP3V3_S3_WLAN
C4053 0.1UF 10% 6.3V X5R 201

AP_RESET_L
AP_PWR_EN
AP_CLKREQ_L_R
R4090 0 5% 1/20W MF 201
AP_CLKREQ_L

SYNC MASTER=J11 MLB	SYNC DATE=10/11/2013
PAGE TITLE	X21 WIRELESS CONNECTOR
Apple Inc.	DRAWING NUMBER 051-9277
	SIZE D
	REVISION 2.8.0
	BRANCH
	PAGE 40 OF 109
	SHEET 37 OF 73

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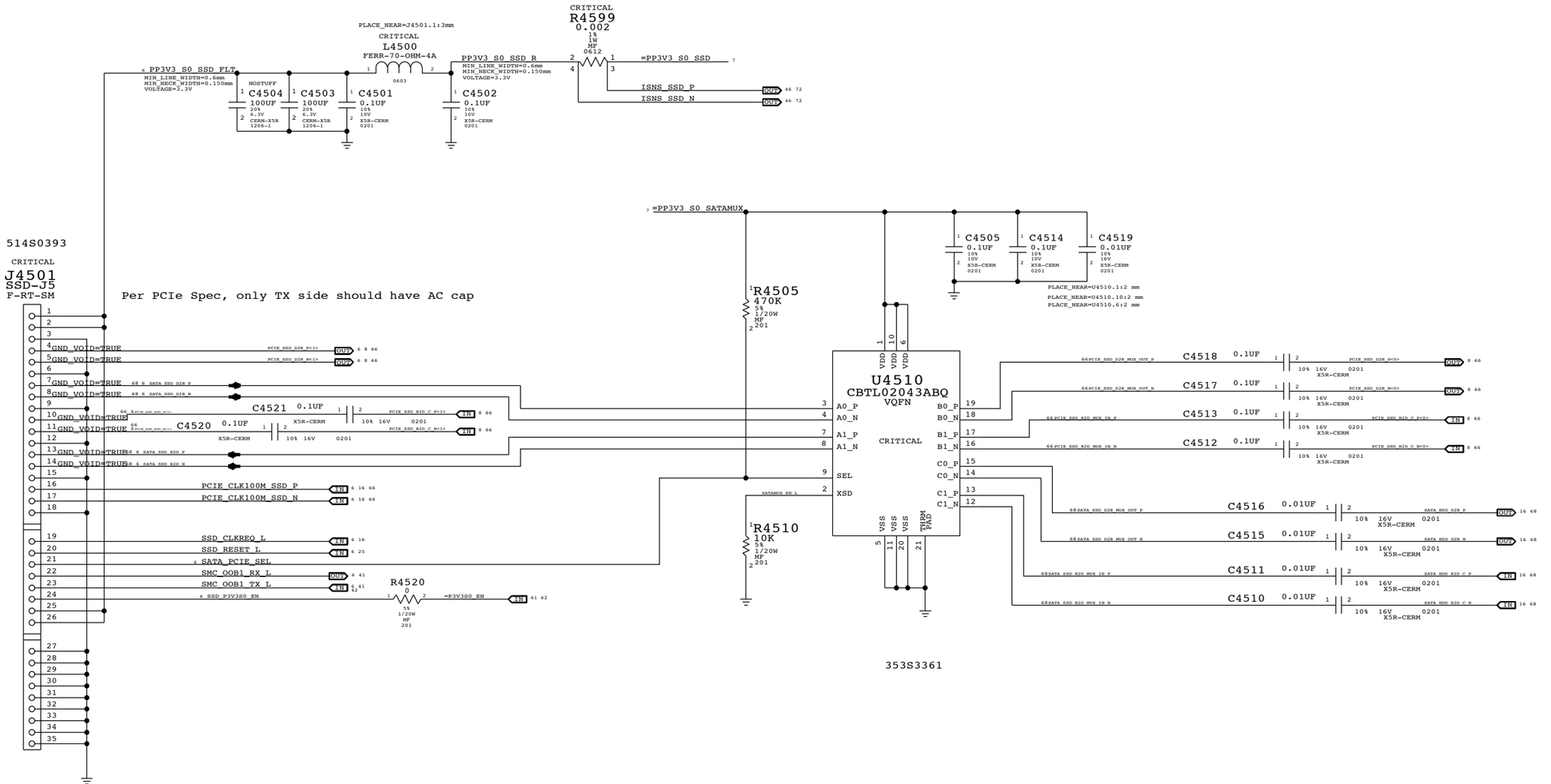

353S3361

PCIE/SATA GUMSTICK2 CONNECTOR

SYNC MASTER=J13 MLB NON POR	SYNC DATE=10/17/2011
PAGE TITLE	SSD CONNECTOR
Apple Inc.	DRAWING NUMBER 051-9277 SIZE D
	REVISION 2.8.0
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	SHEET 38 OF 73

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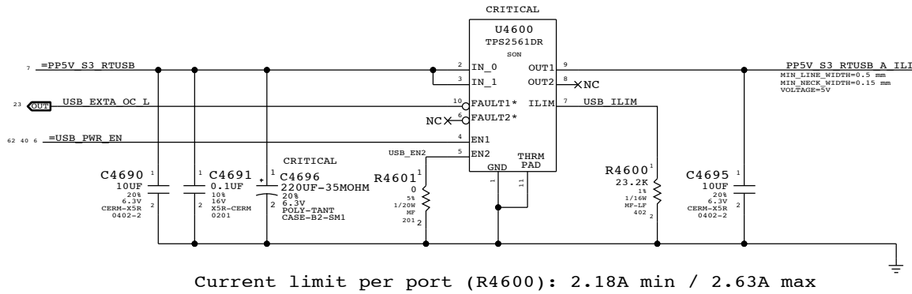
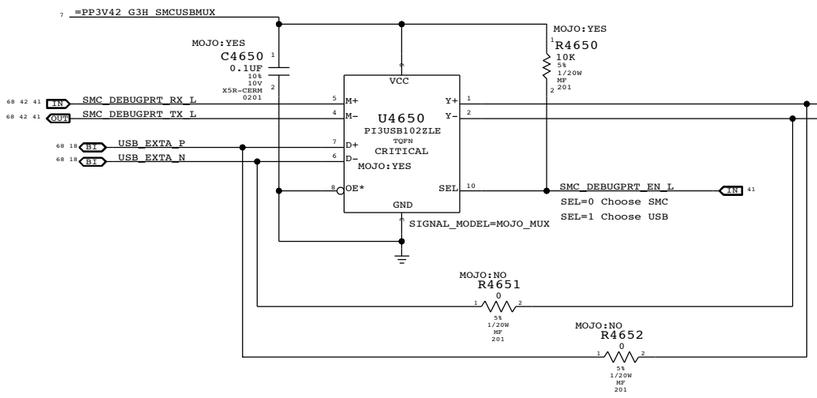
Right USB Port A

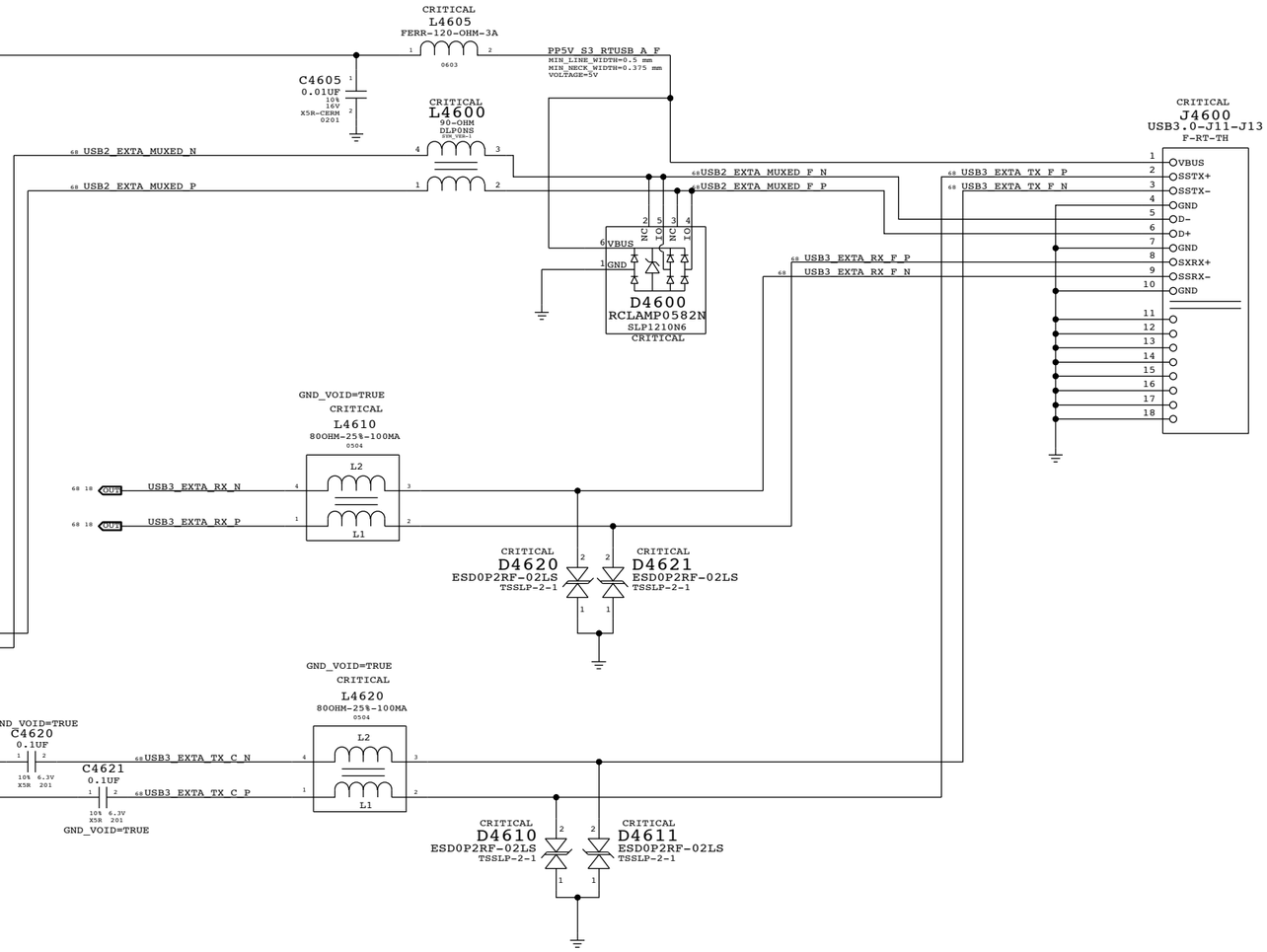
USB Port Power Switch



Current limit per port (R4600): 2.18A min / 2.63A max

Mojo SMC Debug Mux





SYNC MASTER=J11 MLB | SYNC DATE=09/30/2011

PAGE TITLE: External A USB3 Connector

Apple Inc.

DRAWING NUMBER: 051-9277 | SIZE: D

REVISION: 2.8.0

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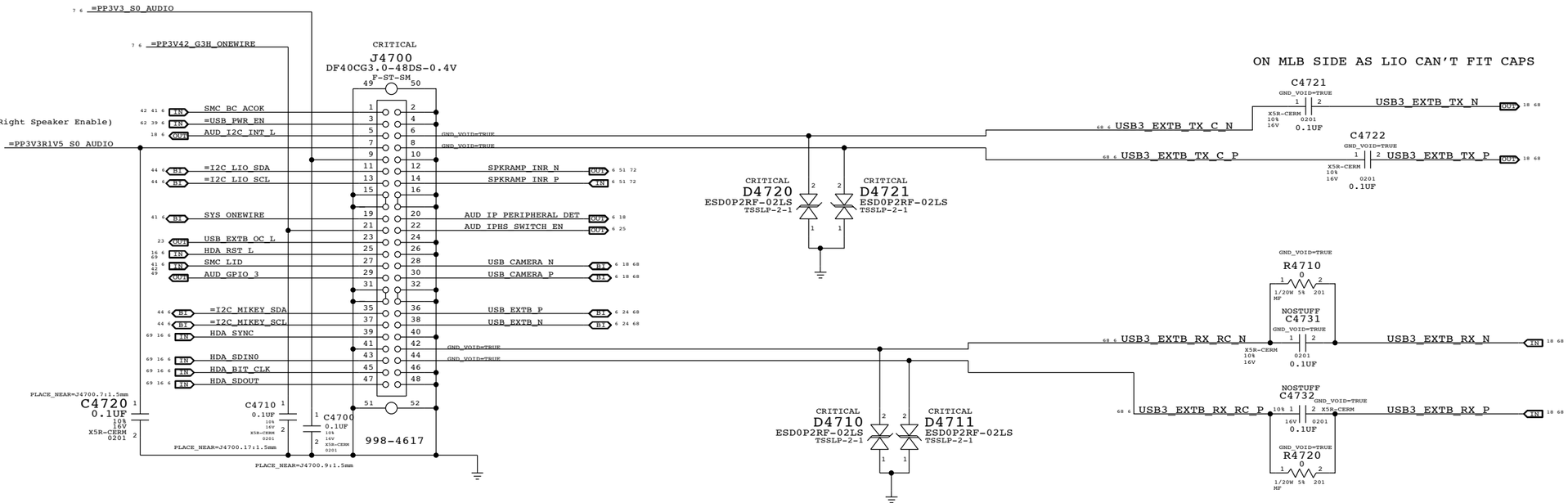

SYNC MASTER=J13 MLB NON POR SYNC DATE=11/10/2011

PAGE TITLE

Left I/O (LIO) Connector

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

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PAGE 47 OF 109

SHEET 40 OF 73

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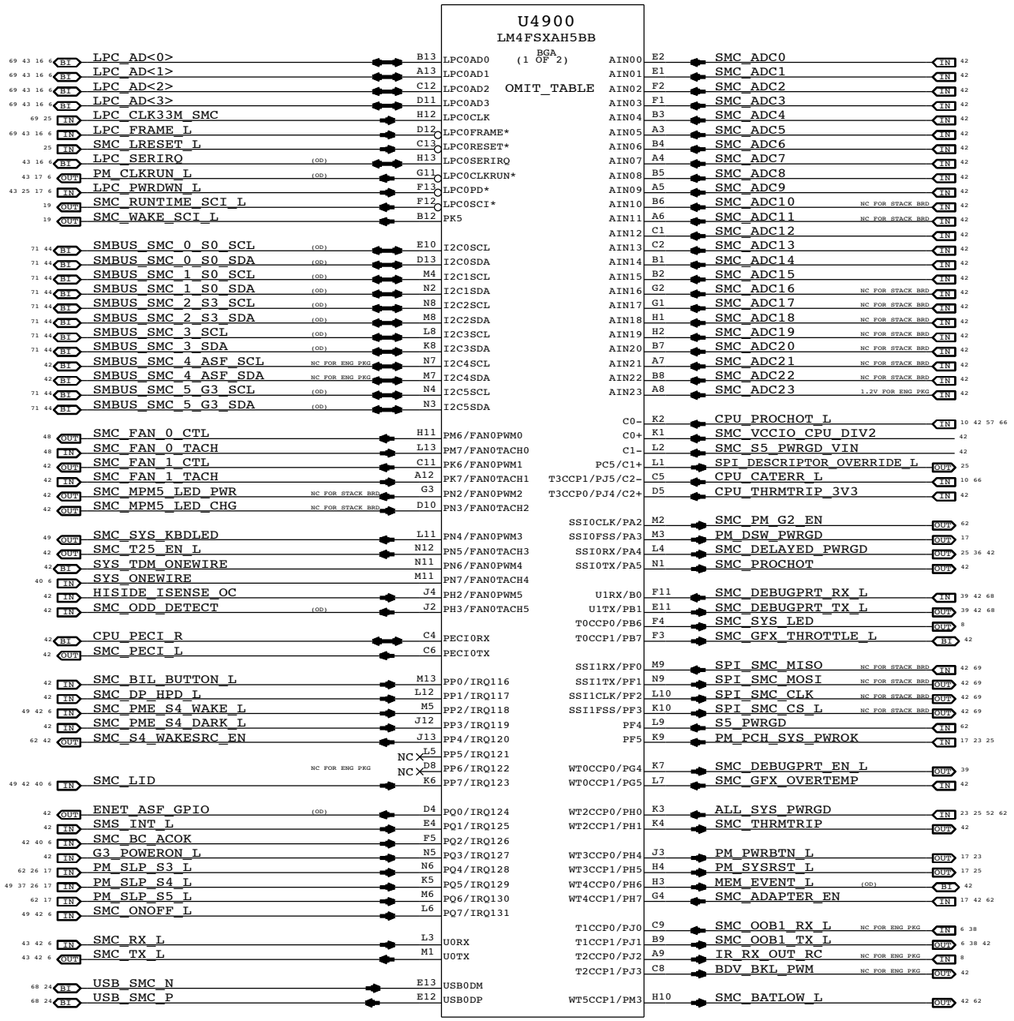
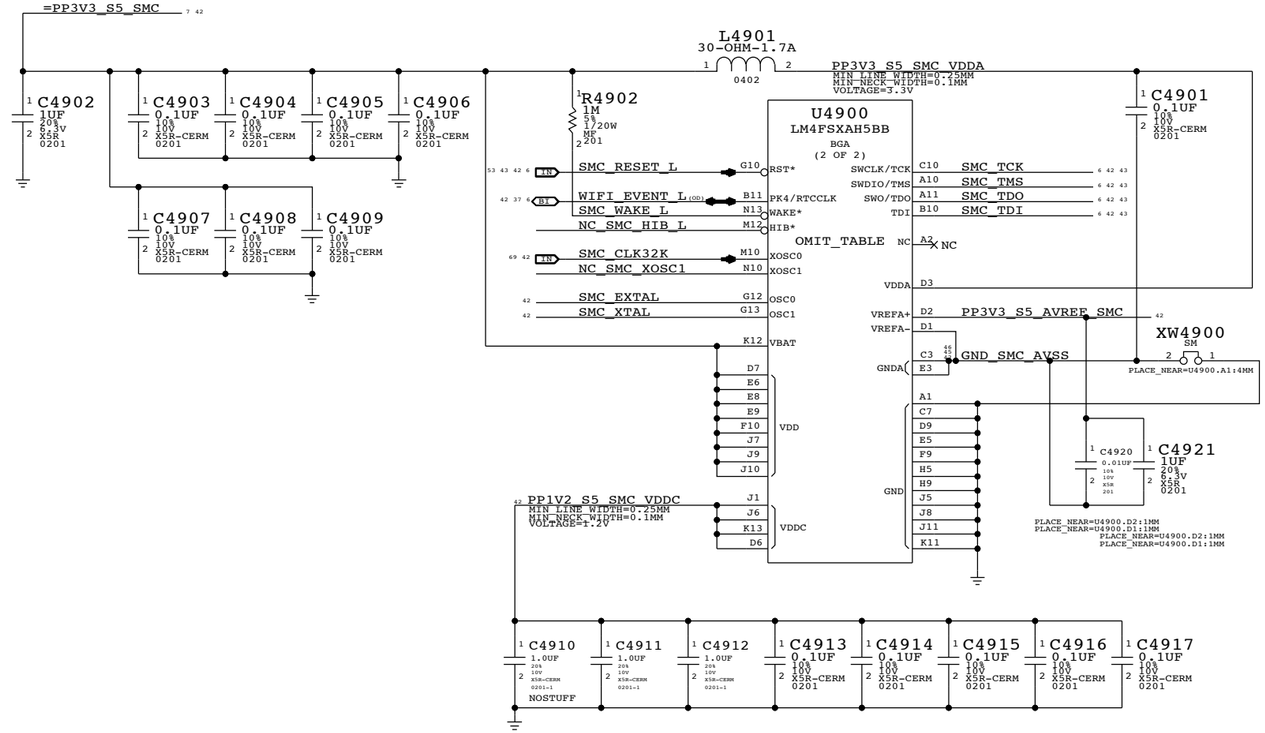


NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.



SYNC MASTER=J13 MLB NON POR
SYNC DATE=10/17/2011

PAGE TITLE
SMC

Apple Inc.

DRAWING NUMBER 051-9277
SIZE D
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PAGE 49 OF 109
SHEET 41 OF 73

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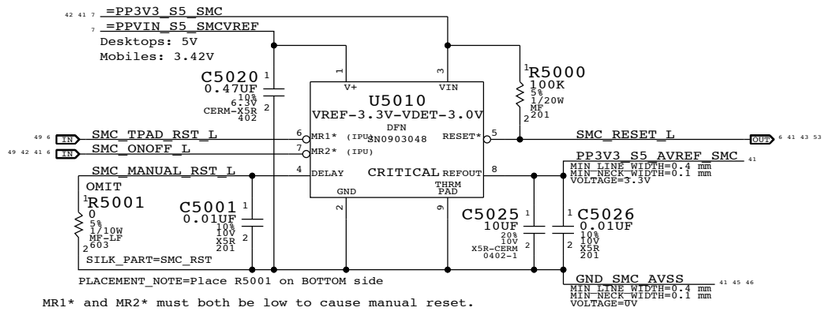
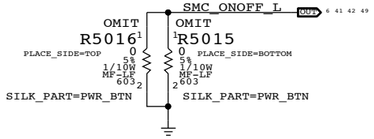
SMC Reset "Button", Supervisor & AVREF Supply



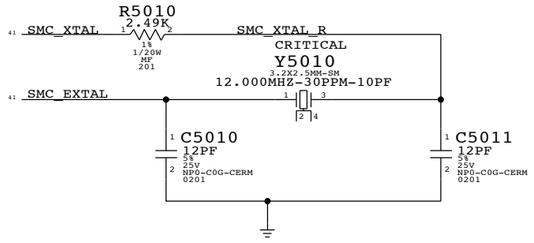
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.
NOTE: Internal pull-ups are to VIN, not V+.

Debug Power "Buttons"



SMC Crystal Circuit

SMC USB Clock require these crystal
values:5,6,8,10,12,16,18,20,24,25 MHz



Note:
ADC10 and ADC11 are shared
with comparators on Stack Board.

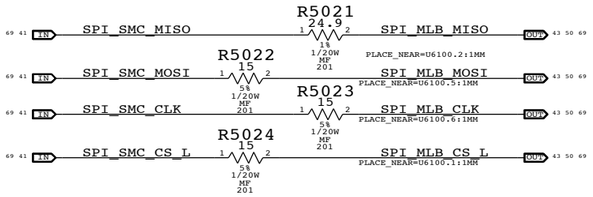
SMC_ADC0	SMC_CPU_VSENSE	
SMC_ADC1	SMC_CPU_ISENSE	
SMC_ADC2	SMC_VCCSA_VSENSE	
SMC_ADC3	SMC_DCIN_VSENSE	
SMC_ADC4	SMC_DCIN_ISENSE	
SMC_ADC5	SMC_PBUS_VSENSE	
SMC_ADC6	SMC_HDD_ISENSE	
SMC_ADC7	SMC_BMON_ISENSE	
SMC_ADC8	SMC_HS_COMPUTING_ISENSE	
SMC_ADC9	SMC_OTHER_HI_ISENSE	
SMC_ADC10	SMC_1V5S3_ISENSE	
SMC_ADC11	SMC_CPUVCCIO_ISENSE	
SMC_ADC12	SMC_GFX_VSENSE	
SMC_ADC13	SMC_CPU_SA_ISENSE	
SMC_ADC14	SMC_3V3S0_ISENSE	
SMC_ADC15	SMC_WLAN_ISENSE	
SMC_ADC16	SMC_LCDBKLT_ISENSE	
SMC_ADC17	NC_SCM_ADC17	
SMC_ADC18	SMC_GFX_ISENSE	
SMC_ADC19	NC_SMC_ADC19	
SMC_ADC20	NC_SMC_ADC20	
SMC_ADC21	NC_SMC_ADC21	
SMC_ADC22	NC_SMC_ADC22	
SMC_ADC23	SMC_ADC23	
SMC_GFX_OVERTEMP	NC_SMC_GFX_OVERTEMP	
SMC_GFX_THROTTLE_L	NC_SMC_GFX_THROTTLE_L	
SMC_FAN_1_CTL	NC_SMC_FAN_1_CTL	
SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH	
ENET_ASF_GPIO	NC_ENET_ASF_GPIO	
SMC_MPM5_LED_PWR	NC_SMC_MPM5_LED_PWR	
SMC_MPM5_LED_CHG	NC_SMC_MPM5_LED_CHG	
SYS_TDM_ONEWIRE	NC_SYS_TDM_ONEWIRE	
SMC_DP_HPD_L	NC_SMC_DP_HPD_L	
=CHGR_ACOK	SMC_BC_ACOK	
HISIDE_ISENSE_OC	NC_HISIDE_ISENSE_OC	
SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL	
SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA	
BDV_BKL_PWM	NC_BDV_BKL_PWM	
SMC_PME_S4_DARK_L	SDCONN_STATE_CHANGE_SMC	
	=TBT_WAKE_L	
SMC_T25_EN_L	NC_SMC_T25_EN_L	

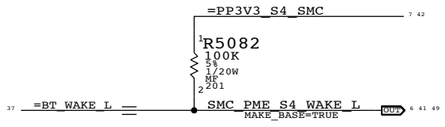
All: MAKE_BASE=TRUE

R5012 22 5% 1/20W MF 201
PM_CLK32K_SUSCLK_R — SMC_CLK32K
PLACE_NEAR=U1800.D3:5.1mm

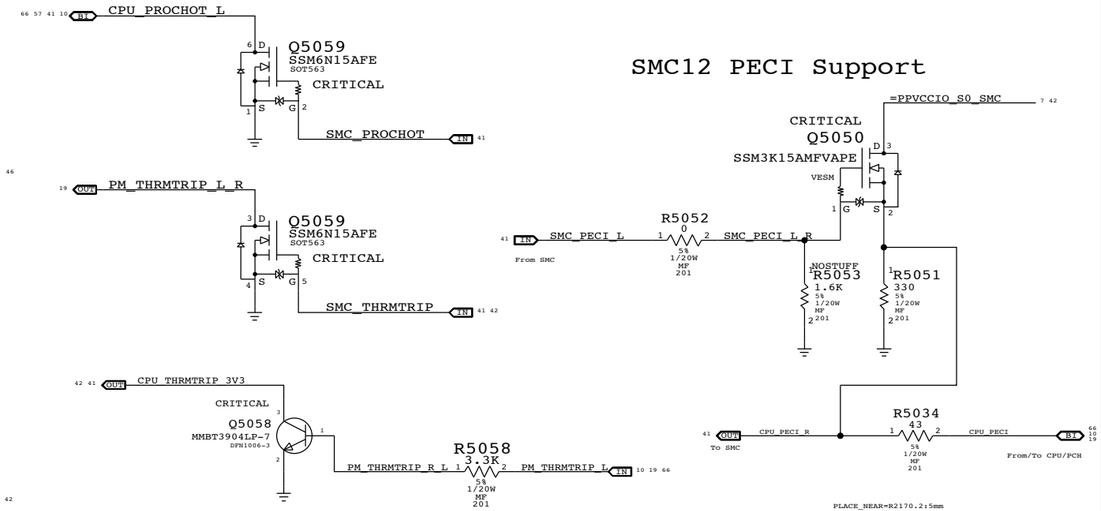
SMC12 SPI Support

Series resistors are no stuffed until the
topology of 2 SPI Masters are verified.



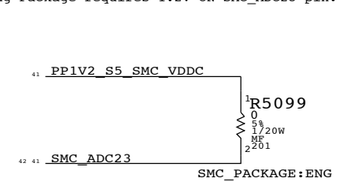


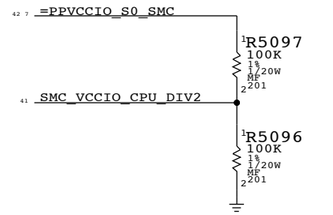
SMC12 PECI Support

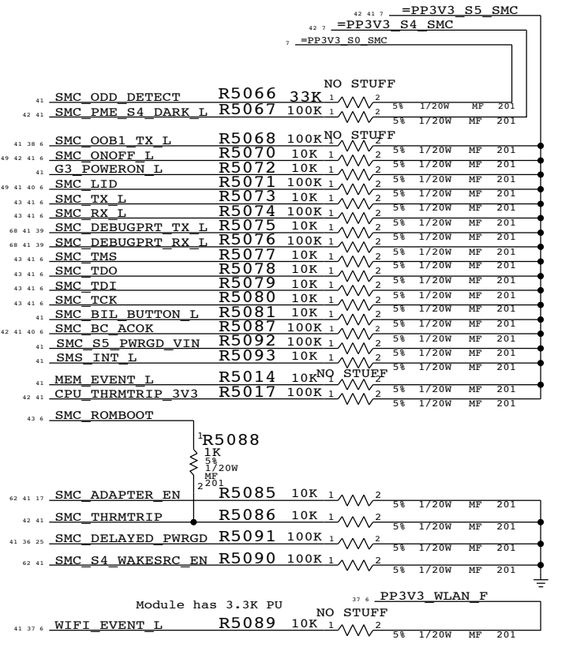


SMC12 Eng Pkg Support

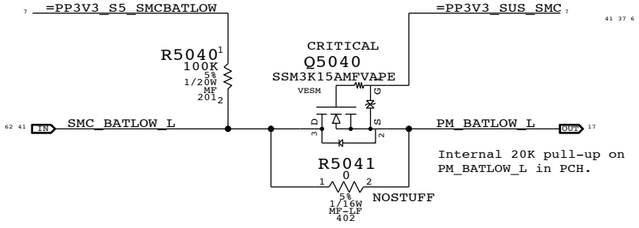
Eng Package requires 1.2V ON SMC_ADC23 pin.







BATLOW# Isolation



SYNC MASTER=J13 MLB NON POR — SYNC DATE=11/10/2011

PAGE TITLE: SMC Support

Apple Inc.

DRAWING NUMBER: 051-9277 — SIZE: D
REVISION: 2.8.0
BRANCH:
PAGE: 50 OF 109
SHEET: 42 OF 73

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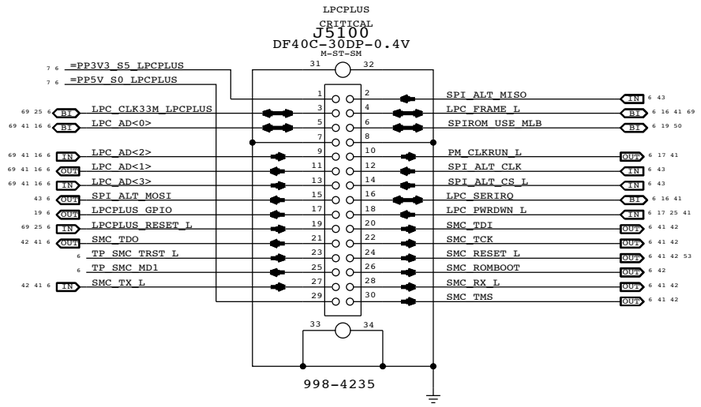
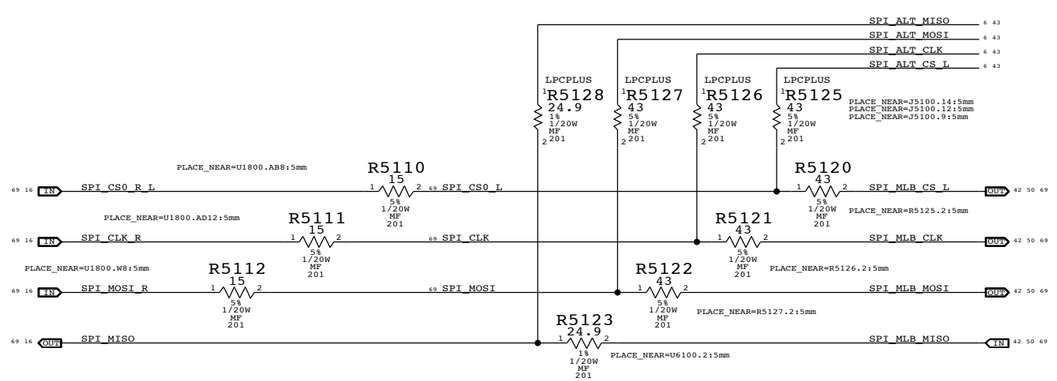
LPC+SPI Connector



SPI Bus Series Termination



SYNC MASTER=J11 MLB | SYNC DATE=09/08/2011

PAGE TITLE: LPC+SPI Debug Connector

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DRAWING NUMBER: 051-9277 | SIZE: D

REVISION: 2.8.0

BRANCH:

PAGE: 51 OF 109

SHEET: 43 OF 73

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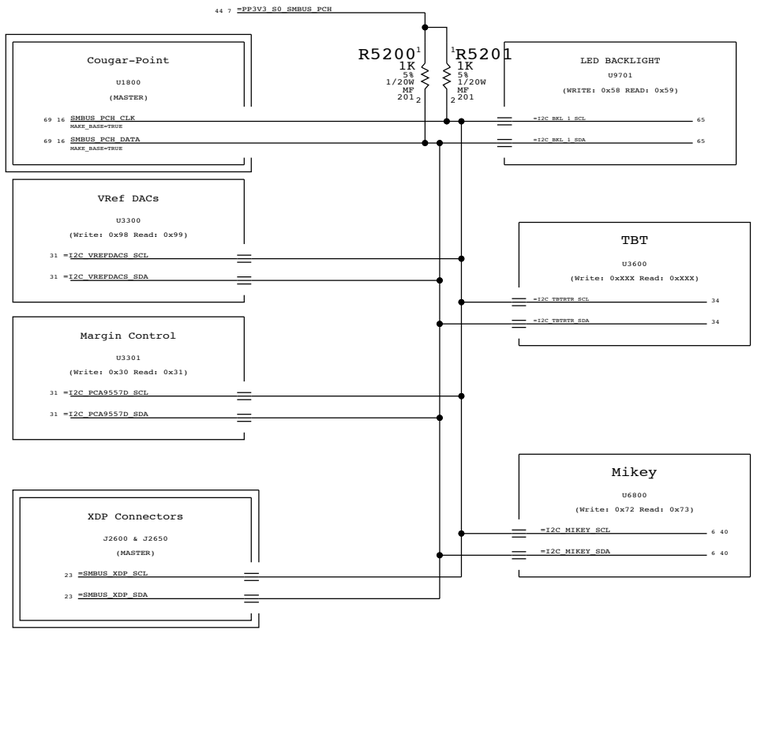
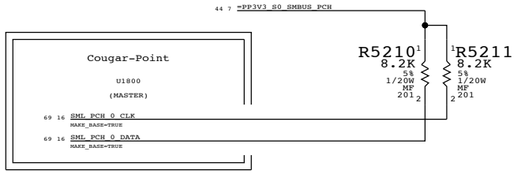
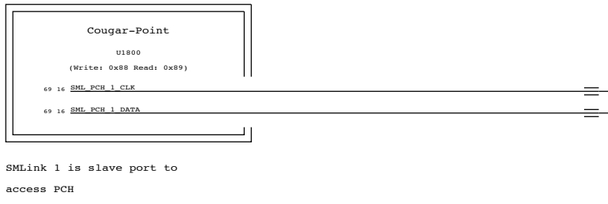
PCH S0 SMBus "0" Connections



PCH S0 "SMLink 0" Connections

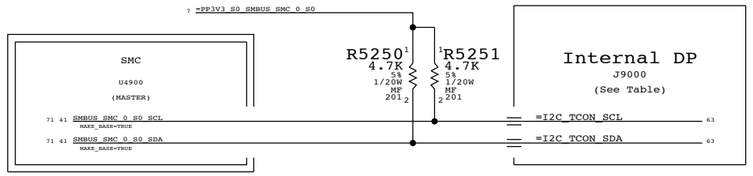


PCH S0 "SMLink 1" Connections



SMLink 1 is slave port to
access PCH

SMC "0" SMBus S0 Connections



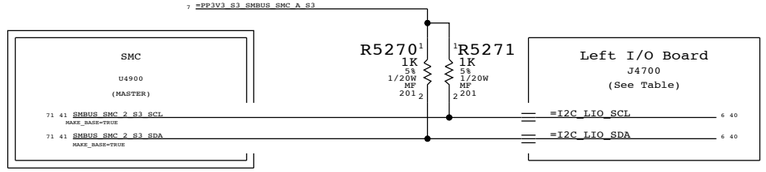
(* = Multiple options)

Internal DP

	K21		K78		
	Samsung	LGD	Samsung	LGD	AUO
Analogix T-con – (Write: 0x7B/0x87 Read: 0x7C/0x88)	N	Y	*	Y	*
Parade T-con – (0x10-0x1F or 0x30-0x3F)	Y	N	*	N	*
DVR – (Write: 0x4E Read: 0x4F)	Y	Y	Y	Y	N

SMC "2" SMBus S3 Connections

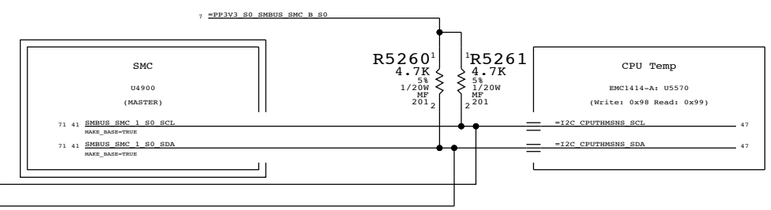
NOTE: SMC RMT bus remains powered and may be active in S3 state



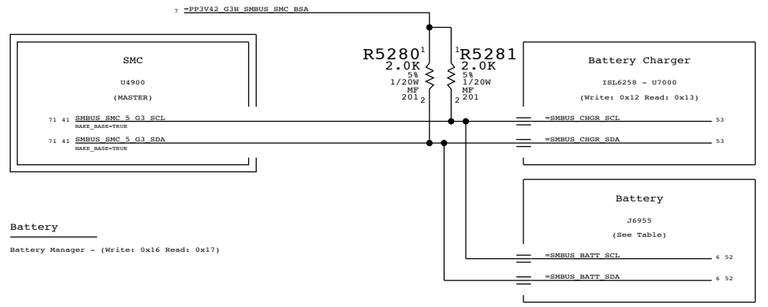
Left I/O Board

ALS – (write: 0x72 Read: 0x73)
Finstack Temp – (Write: 0x92 Read: 0x93)

SMC S0 "1" SMBus Connections



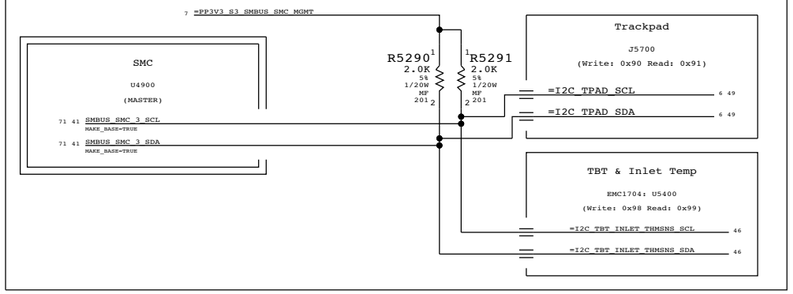
SMC "5" SMBus G3H Connections



Battery

Battery Manager – (Write: 0x16 Read: 0x17)

SMC "3" SMBus S3 Connections



SYNC_MASTER=J11_MLB SYNC_DATE=10/04/2011

PAGE TITLE
SMBus Connections

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D
REVISION 2.8.0
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PAGE 52 OF 109
SHEET 44 OF 73

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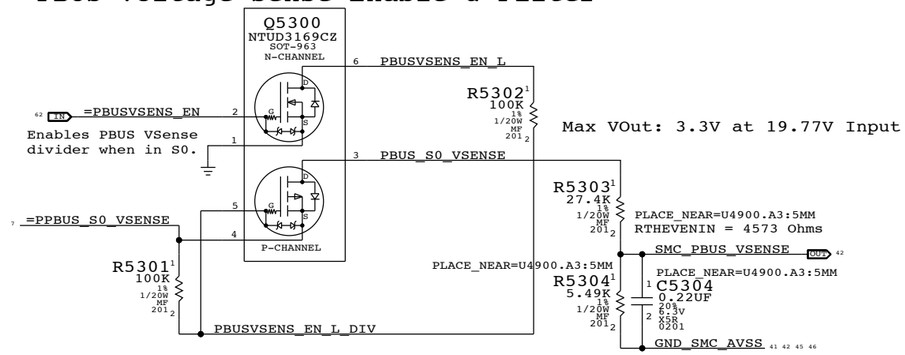
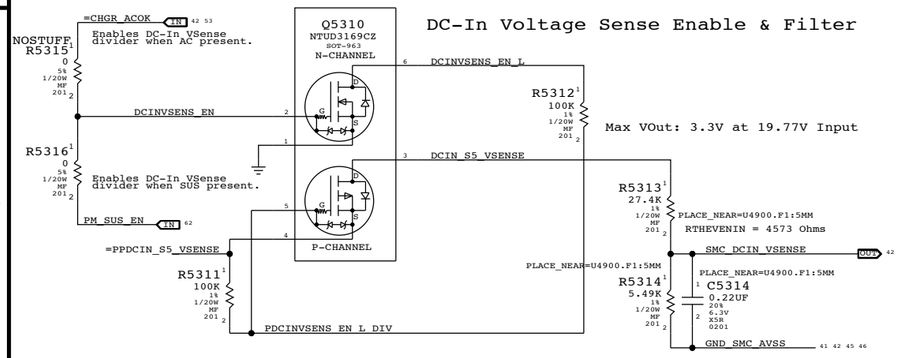
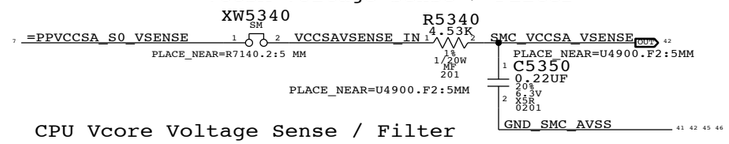
PBUS Voltage Sense Enable & Filter



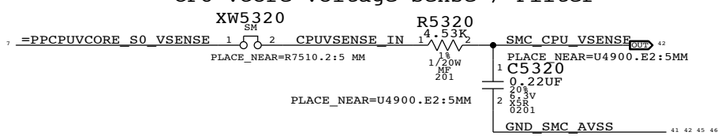
DC-In Voltage Sense Enable & Filter



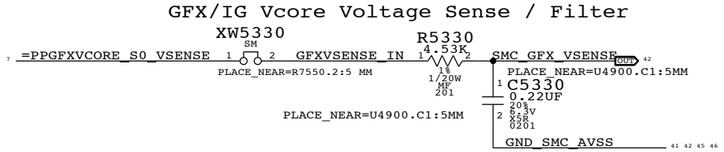
VCCSA Voltage Sense / Filter



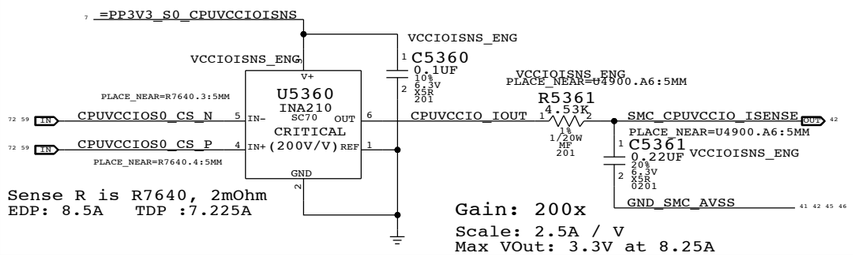
CPU Vcore Voltage Sense / Filter



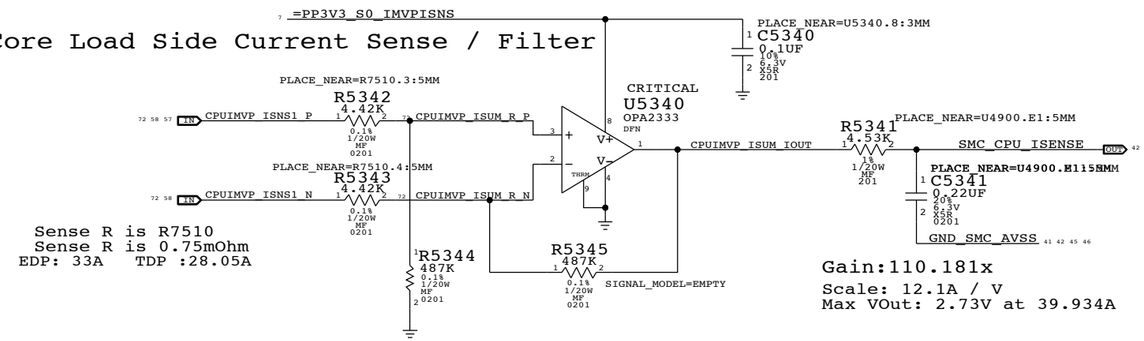
GFX/IG Vcore Voltage Sense / Filter



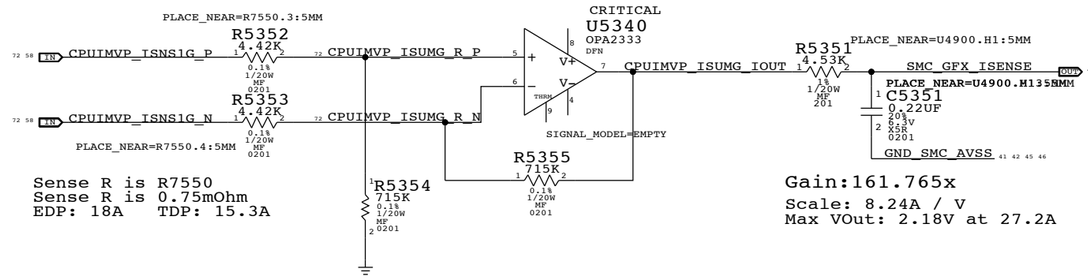
CPU 1.05V VCCIO Current Sense / Filter



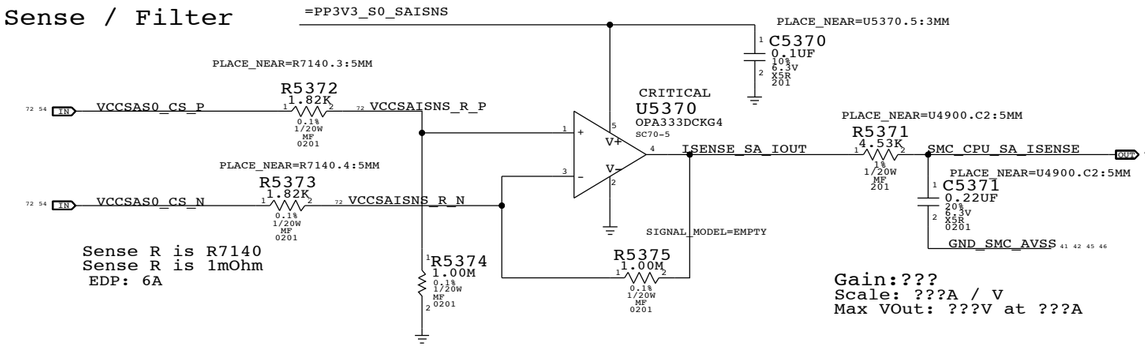
CPU VCore Load Side Current Sense / Filter



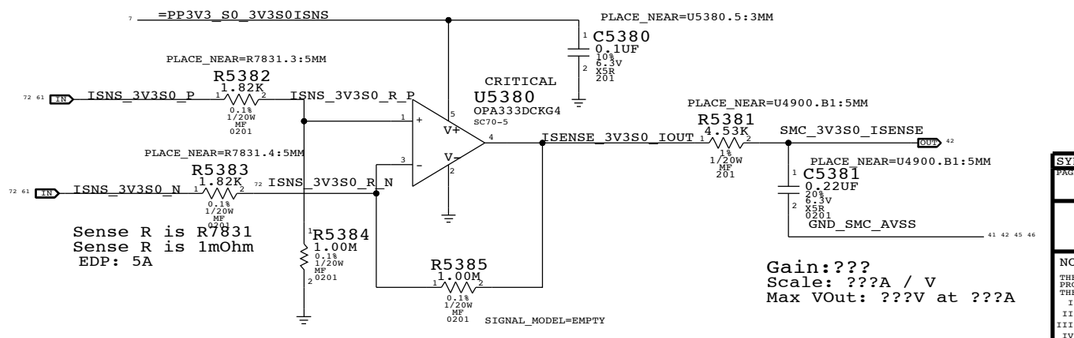
GFX/IG VCore Load Side Current Sense / Filter



CPU SA Current Sense / Filter



3.3V S0 FET Current Sense / Filter



SYNC_MASTER=J11_MLB SYNC_DATE=12/02/2011

PAGE TITLE: Voltage & Load Side Current Sensing

Apple Inc.

DRAWING NUMBER: 051-9277 SIZE: D

REVISION: 2.8.0

BRANCH:

PAGE: 53 OF 109

SHEET: 45 OF 73

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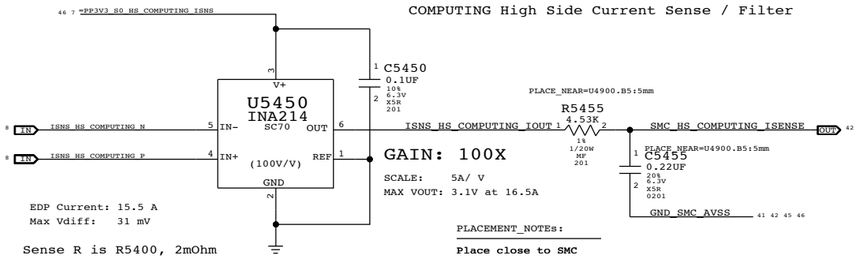
COMPUTING High Side Current Sense / Filter



GAIN: 100X

SCALE: 5A/ V

MAX VOUT: 3.1V at 16.5A

EDP Current: 15.5 A

Max Vdiff: 31 mV

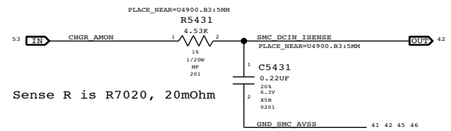
Sense R is R5400, 2mOhm

PLACEMENT_NOTES:

Place close to SMC

(For R and C)

DC-IN (AMON) Current Sense Filter



Sense R is R7020, 20mOhm

DC-In AMON

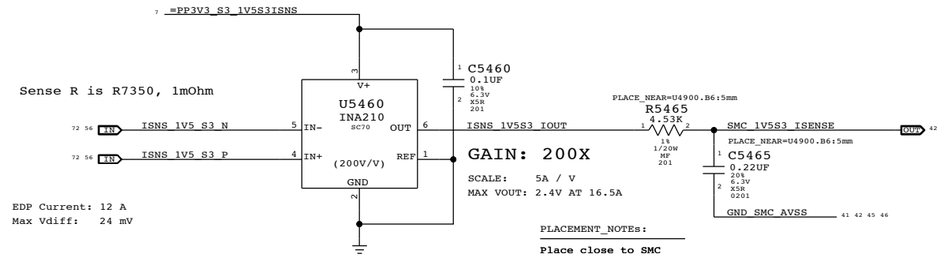
ISL6259 Gain: 20x

Scale: 2.5A / V

Max VOut: 1.4V at 8.25A

EDP Current: 3.5A

DDR3 1V5R1V35 Current Sense / Filter



Sense R is R7350, 1mOhm

GAIN: 200X

SCALE: 5A / V

MAX VOUT: 2.4V AT 16.5A

EDP Current: 12 A

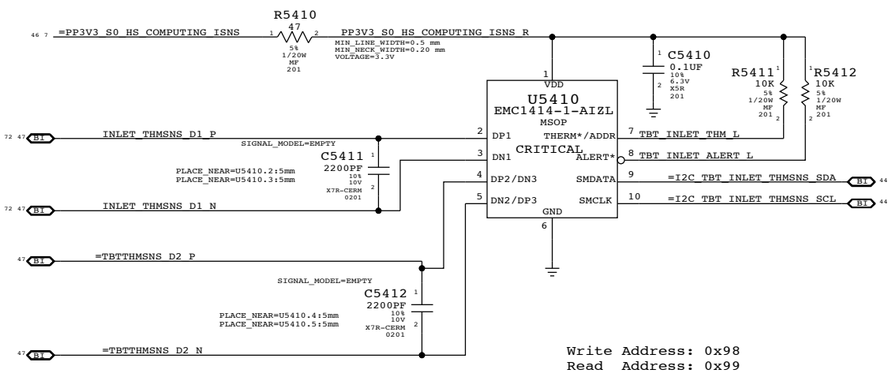
Max Vdiff: 24 mV

PLACEMENT_NOTES:

Place close to SMC

(For R and C)

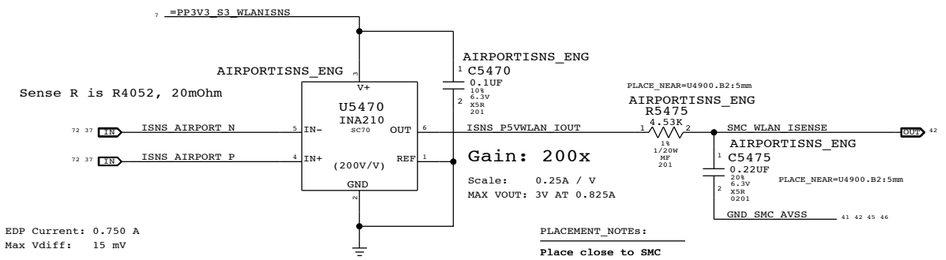
TBT/Inlet Temp Sensor



Write Address: 0x98

Read Address: 0x99

AirPort Current Sense / Filter



Sense R is R4052, 20mOhm

Gain: 200x

Scale: 0.25A / V

MAX VOUT: 3V AT 0.825A

EDP Current: 0.750 A

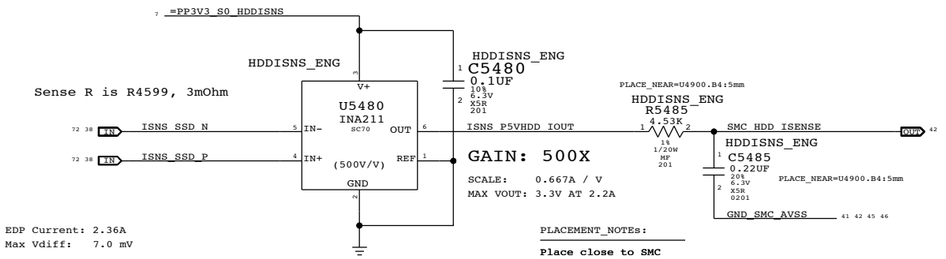
Max Vdiff: 15 mV

PLACEMENT_NOTES:

Place close to SMC

(For R and C)

HDD Current Sense / Filter



Sense R is R4599, 3mOhm

GAIN: 500X

SCALE: 0.667A / V

MAX VOUT: 3.3V AT 2.2A

EDP Current: 2.36A

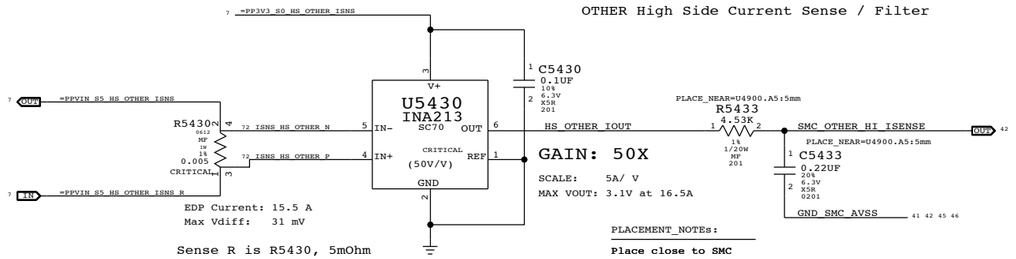
Max Vdiff: 7.0 mV

PLACEMENT_NOTES:

Place close to SMC

(For R and C)

OTHER High Side Current Sense / Filter



EDP Current: 15.5 A

Max Vdiff: 31 mV

Sense R is R5430, 5mOhm

GAIN: 50X

SCALE: 5A/ V

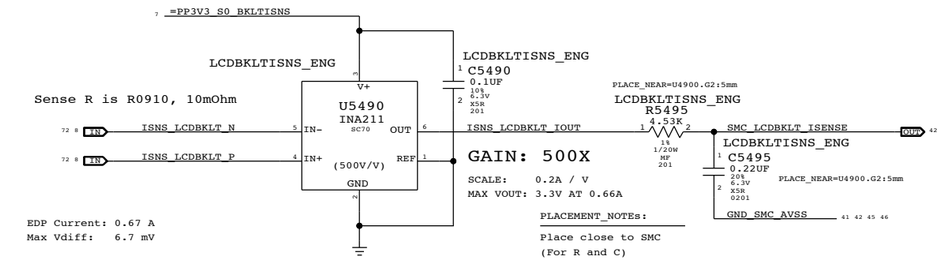
MAX VOUT: 3.1V at 16.5A

PLACEMENT_NOTES:

Place close to SMC

(For R and C)

LCD Backlight Driver Input Current Sense / Filter



Sense R is R0910, 10mOhm

GAIN: 500X

SCALE: 0.2A / V

MAX VOUT: 3.3V AT 0.66A

EDP Current: 0.67 A

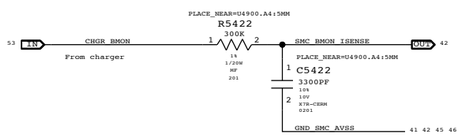
Max Vdiff: 6.7 mV

PLACEMENT_NOTES:

Place close to SMC

(For R and C)

CHARGER BMON High Side (BATTERY DISCHAEGE) Current Sense, MUX & Filter



Charger BMON (Production) Solution

ISL6259 Gain: 36x

Scale: 2.78A / V

Max VOut: 3.3V at 9.167A

EDP Current: 310A

SYNC_MASTER=J13_MLB_NON_POR SYNC_DATE=10/17/2011

PAGE TITLE

High Side Current Sensing

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

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PAGE 54 OF 109

SHEET 46 OF 73

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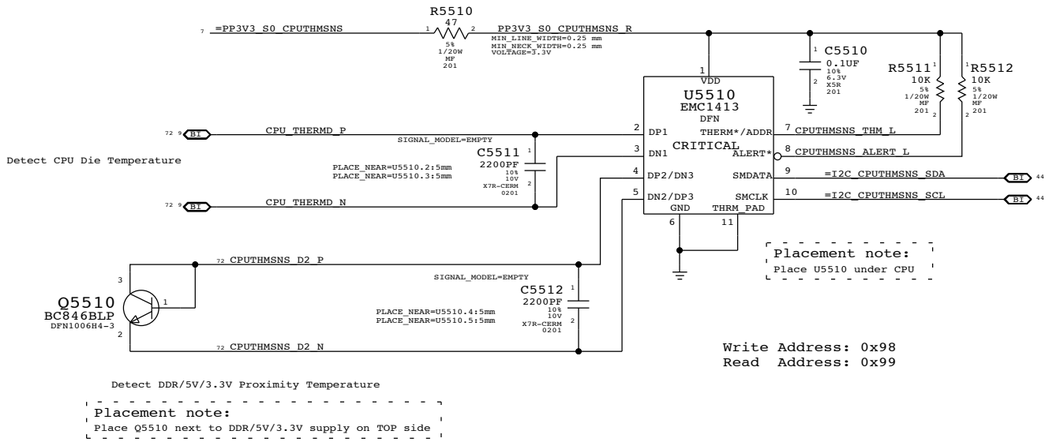
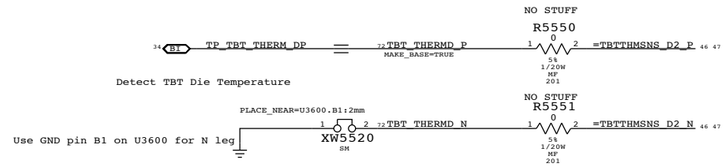
CPU Proximity Sensor



TBT Die

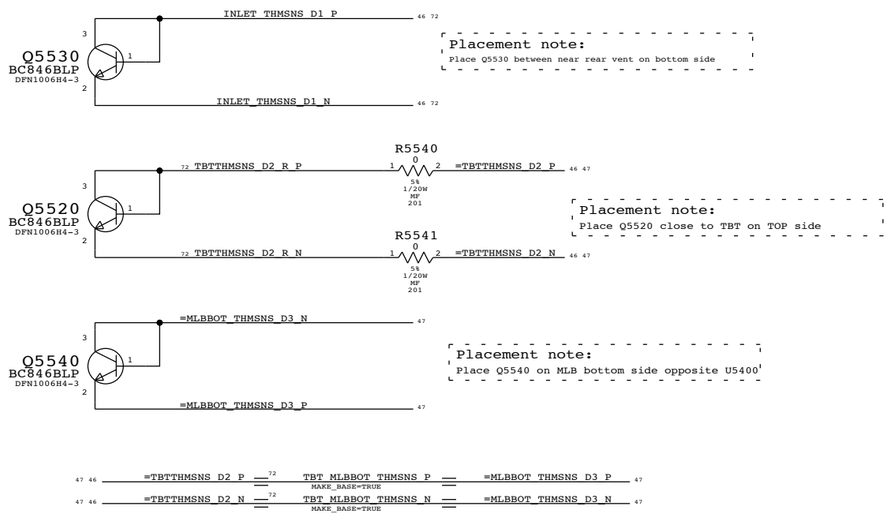


To connect Die Sensor, Stuff R5550 & R5551, No stuff R5540 & R5541
To connect Proximity Sensor, Stuff R5540 & R5541, No Stuff R5550,R5551

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5361		VCCIOISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5475		AIRPORTISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5485		HDDISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5495		LCDBKLTISNS_PROD

Replacing caps with 100K PD on ISENSE SMC inputs

TBT,MLB Bottom & Inlet Proximity Sensors



SYNC MASTER=J11 MLB
SYNC DATE=08/03/2011

PAGE TITLE
Thermal Sensors

Apple Inc.

DRAWING NUMBER 051-9277
SIZE D
REVISION 2.8.0
BRANCH
PAGE 55 OF 109
SHEET 47 OF 73

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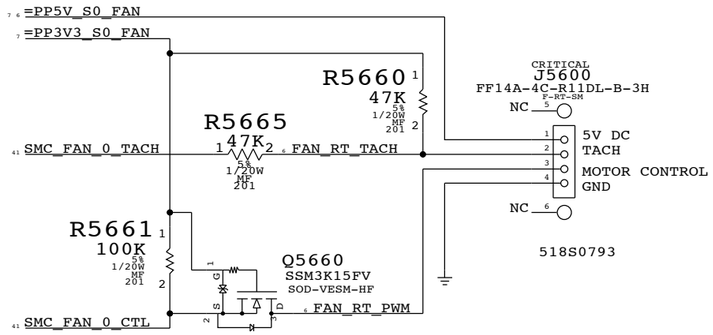
FAN CONNECTOR



SYNC MASTER=K21 MLB	SYNC DATE=07/28/2011
PAGE TITLE: Fan	
Apple Inc.	DRAWING NUMBER: 051-9277 SIZE: D
	REVISION: 2.8.0
	BRANCH:
	PAGE: 56 OF 109
	SHEET: 48 OF 73

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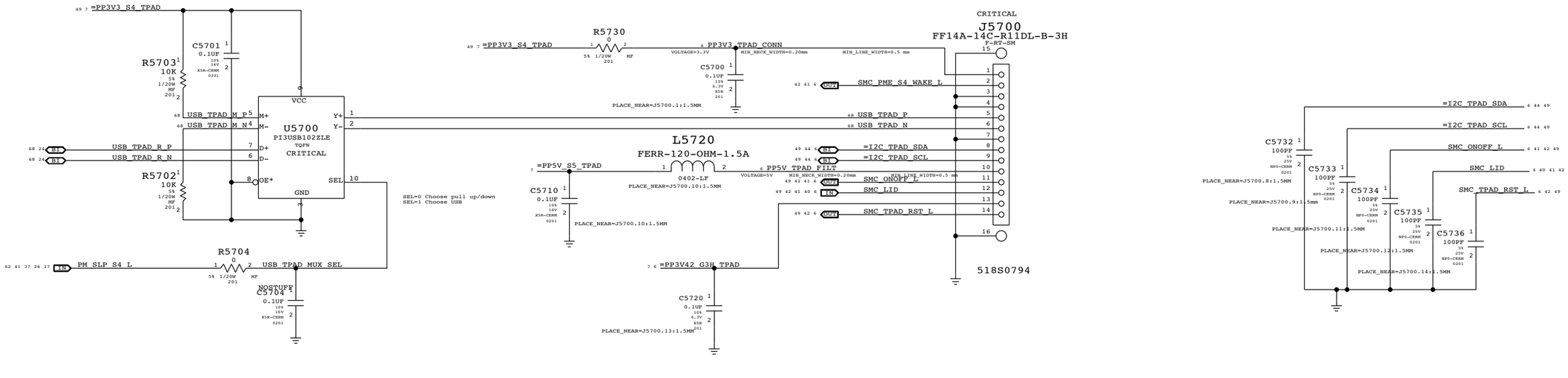
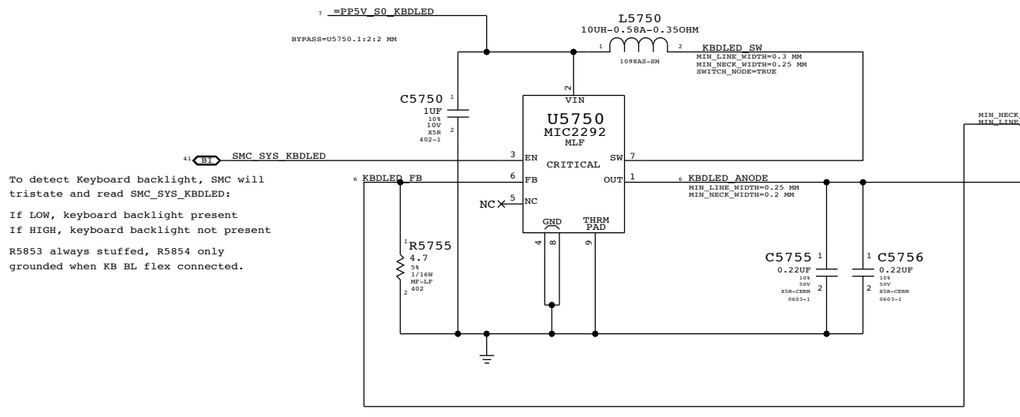
IPD Flex Connector



Keyboard Backlight Driver & Detection

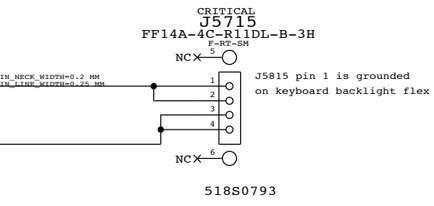


To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:

If LOW, keyboard backlight present
If HIGH, keyboard backlight not present

R5853 always stuffed, R5854 only grounded when KB BL flex connected.

Keyboard Backlight Connector



SYNC MASTER=J13 MLB NON POR	SYNC DATE=11/10/2011
PAGE TITLE: IPD / KBD Backlight	
Apple Inc.	DRAWING NUMBER 051-9277 SIZE D
	REVISION 2.8.0
	BRANCH
	PAGE 57 OF 109
	SHEET 49 OF 73

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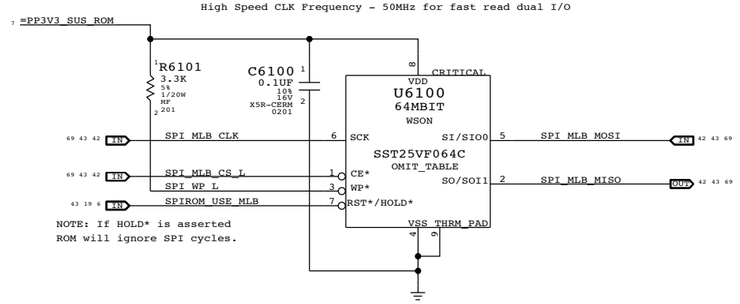
DUAL I/O MODE (MODE 0 & 3) SUPPORTED
High Speed CLK Frequency - 50MHz for fast read dual I/O



NOTE: If HOLD* is asserted
ROM will ignore SPI cycles.

SYNC MASTER=K21 MLB	SYNC DATE=07/28/2011
PAGE TITLE: SPI ROM	
Apple Inc.	DRAWING NUMBER: 051-9277 SIZE: D
	REVISION: 2.8.0
	BRANCH:
	PAGE: 61 OF 109
	SHEET: 50 OF 73

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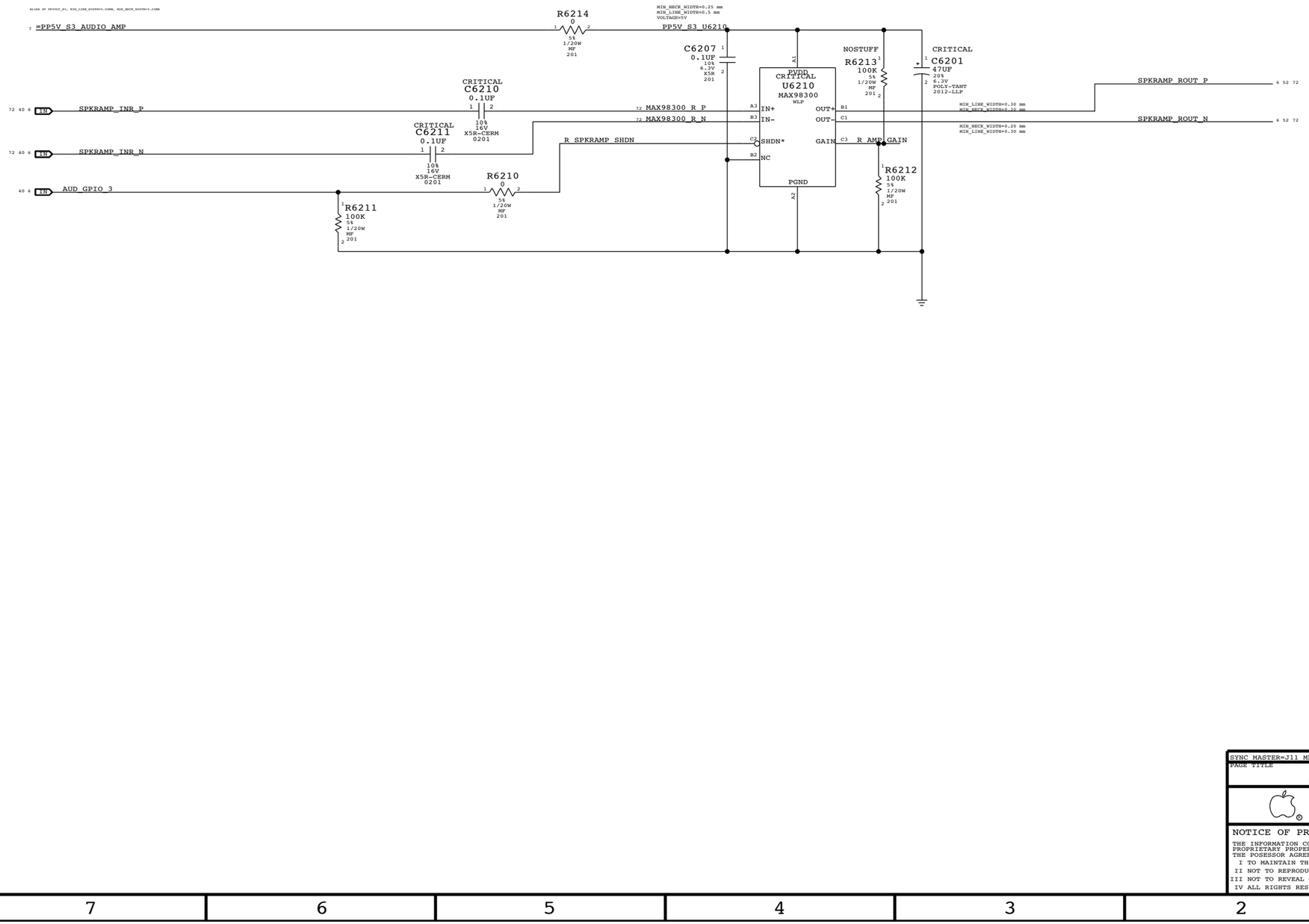
SPEAKER AMPLIFIERS

APN:353S2888

SPEAKER LOWPASS	80 HZ < FC < 132 HZ
GAIN	6DB



SYNC MASTER=J11 MLB SYNC DATE=09/30/2011

PAGE TITLE

AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

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PAGE 62 OF 109

SHEET 51 OF 73

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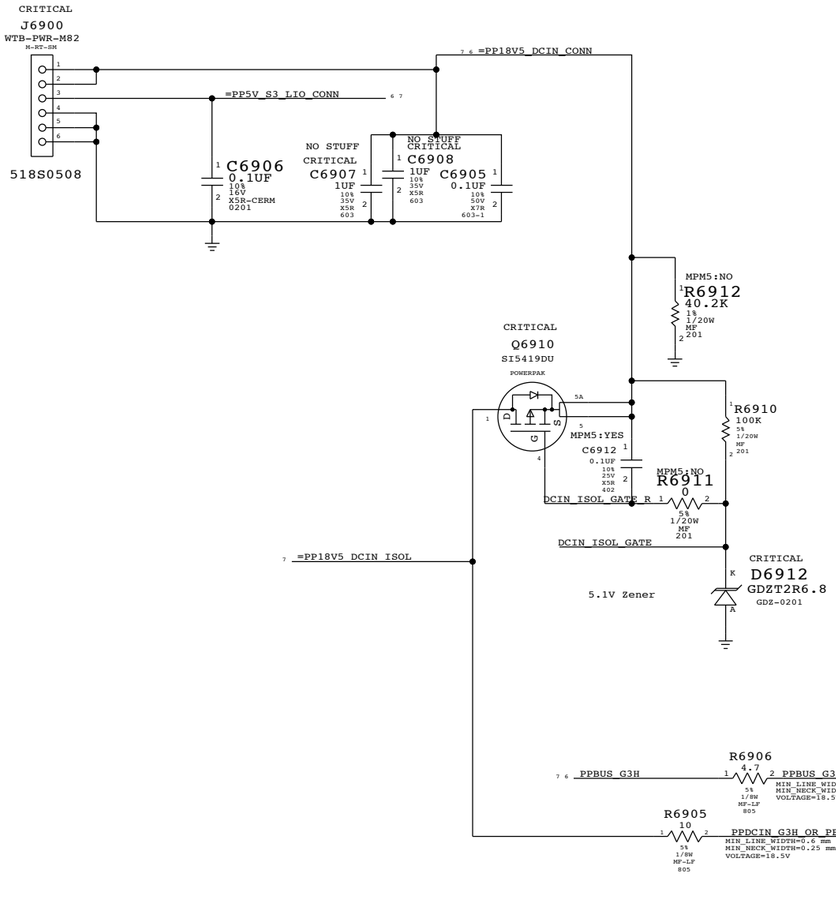
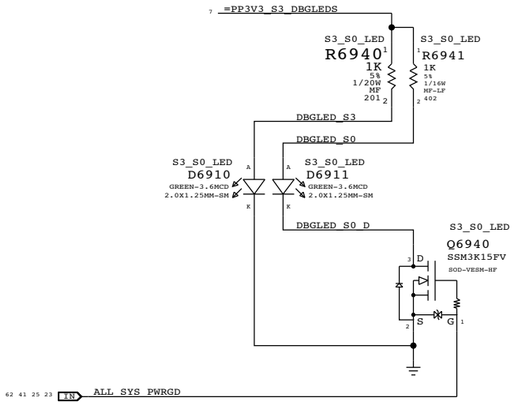
MLB to LIO Power Cable Connector

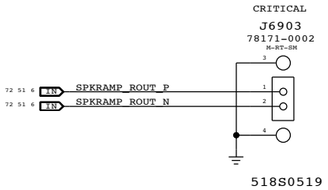


Debug LEDs

(For development only)

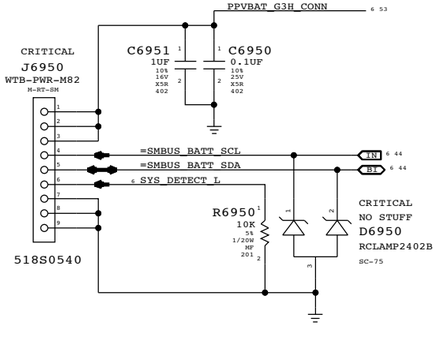


Right Speaker Connector



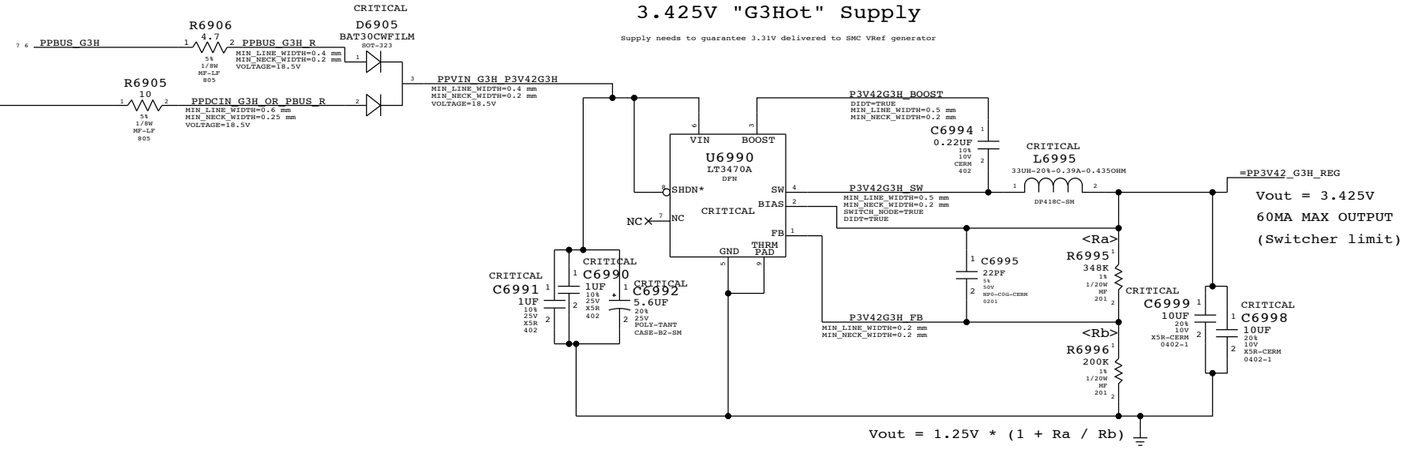
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0560	1	RES,MF,1/20W,90.9KOHM,1,0201,SMD	R6912		MPM5:YES
117S0008	1	RES,MF,1/20W,100KOHM,1,0201,SMD	R6911		MPM5:YES

K16-Specific Battery Connector



3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



SYNC_MASTER=J13_MLB_NON_POR SYNC_DATE=11/10/2011

PAGE TITLE

DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

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PAGE 69 OF 109

SHEET 52 OF 73

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Reverse-Current Protection

Inrush Limiter

This node is powered through body diodes:
* DCIN through Q7080.
* PBUS through Q7085, Charger TOP FETs and Q7055.

Need to stuff R7092 if either PP5V5_DCIN:Yes or PP5V5_VDDP are used

5.5v "G3Hot" Supply

For Erp Lot6 spec

FROM ADAPTER

=PPDCIN_S5_CHGR

CRITICAL Q7080 SI5419DU POWERPAK

PPDCIN_G3H_OR_PBUS

R7080 100K 5% 1/20W MF 201

NO STUFF C7084 4.7UF 10% 25V X5R-CERM 0603

C7085 0.1UF 10% 25V X5R 402

R7085 470K 1% 1/20W MF 201

CRITICAL Q7085 SI5419DU POWERPAK

PPDCIN_G3H_INRUSH

CHGR_SGATE_DIV

R7081 62K 1% 1/20W MF 201

CHGR_AGATE_DIV

R7086 332K 1% 1/20W MF 201

=PPDCIN_S5_CHGR_ISOL

CRITICAL D7005 BAT30CWFILM SOT-323

PP5V5_DCIN:NO R7005 20 5% 1/10W MF-LF 603

PPCHGR_DCIN_D_R

(CHGR_SGATE)

(CHGR_AGATE)

(CHGR_DCIN)

NO STUFF R7092 0 5% 1/16W MF-LF 402

PPCHGR_DCIN_D_R

CHGR_DCIN_D

C7090 4.7UF 10% 25V X5R-CERM 0603

U7090 LT3470A DFN

VIN BOOST SHDN* SW BIAS NC FB THRM GND PAD

P5V1_BOOST DIODE=TRUE

C7094 0.22UF 10% 16V CERM 402

CRITICAL L7095 10UH-30%-0.85A-460MOHM 2520

P5V1_SW

P5V1_FB

C7095 22PF 5% 50V NPO-COG-CERM 0201

<Ra> R7095 681K 1% 1/20W MF 201

<Rb> R7096 200K 1% 1/20W MF 201

CRITICAL C7098 10UF 20% 10V X5R 603

CRITICAL C7099 10UF 20% 10V X5R 603

PP5V5_DCIN:YES R7090 0 5% 1/16W MF-LF 402 CHGR_DCIN 53

PP5V5_VDDP R7091 0 5% 1/16W MF-LF 402 PP5V1_CHGR_VDDP 53

PP5V5_CHGR_VDDP

Vout = 5.50V 200MA MAX OUTPUT (Switcher limit)

Vout = 1.25V * (1 + Ra / Rb)

ACIN pin threshold is 3.2V, +/- 50mV

DIVIDER SETS ACIN THRESHOLD AT 12.18V

Input impedance of ~40K meets sparkitecture requirements

30mA max load

PP5V1_CHGR_VDD

R7001 4.7 5% 1/16W MF-LF 402

PP5V1_CHGR_VDDP

C7001 1UF 10% 10V X5R 402

=PP3V42_G3H_CHGR

R7010 66.5K 1% 1/20W MF 201

NO STUFF R7002 100K 5% 1/20W MF 201

CRITICAL OMIT_TABLE

R7000 0 5% 1/20W MF 201

SMC_RESET_L

CHGR_RST_L

=SMBUS_CHGR_SCL

=SMBUS_CHGR_SDA

CHGR_VFRQ

CHGR_CELL

Float CELL for 1S

CHGR_ACIN

CHGR_ICOMP

CHGR_VCOMP

CHGR_VNEG

CHGR_CSO_P

CHGR_CSO_N

U7000 ISL6259HRTZ TQFN

VDD	19		
VDDP	20		
VHST	12		
SMB_RST_N	13		
SCL	11		
SDA	10		
VFRQ	4		
CELL	6		
ACIN	3		
ICOMP	5		
VCOMP	7		
VNEG	8		
CSOP	18		
CSON	17		
DCIN	2		CHGR_DCIN
SGATE	26		CHGR_SGATE
AGATE	1		CHGR_AGATE
CSIP	28		CHGR_CSI_P
CSIN	27		CHGR_CSI_N
BOOT	25		CHGR_BOOT
UGATE	24		CHGR_UGATE
PHASE	23		CHGR_PHASE
LGATE	21		CHGR_LGATE
BGATE	16		CHGR_BGATE
20V/V AMON	9		CHGR_AMON
36V/V BMON	15		CHGR_BMON
(OD) ACOK	14		=CHGR_ACOK
(AGND) THRM_PAD	29		
PGND	22		

R7013 100 1% 1/20W MF 201

R7015 255K 1% 1/20W MF 201

R7011 23.7K 1% 1/20W MF 201

CHGR_VCOMP_R

C7015 470PF 10% 16V X5R-X7R-CERM 0201

R7016 220 1% 1/20W MF 201

CHGR_VNEG_R

C7016 470PF 10% 16V X5R-X7R-CERM 0201

C7050 0.47UF 10% 10V X5R 0402

C7002 1UF 10% 10V X5R 402

XW7000 SM

PLACE_NEAR=U7000.29:1mm

PLACE_NEAR=U7000.22:1mm

(GND)

C7042 0.1UF 10% 6.3V X5R 201

C7011 0.01UF 10% 10V X5R 201

C7000 1UF 10% 10V X5R 402-1

C7005 0.22UF 10% 50V X5R-CERM 0603-1

C7026 1000PF 10% 16V X7R-CERM 0201

GND_CHGR_AGND

R7021 10 5% 1/20W MF 201

R7022 10 5% 1/20W MF 201

CHGR_CSI_R_P

CHGR_CSI_R_N

C7020 0.047UF 10% 16V X7R-CERM 0402

C7022 0.1UF 10% 25V X5R 402

C7021 0.1UF 10% 25V X5R 402

CRITICAL R7020 0.020 0.5% MF-LF 0612 1W

PPDCIN_G3H_CHGR

CRITICAL C7030 33UF-0.06OHM 20% 25V POLY-TANT CASE-D3L

CRITICAL C7031 33UF-0.06OHM 20% 25V POLY-TANT CASE-D3L

C7035 1UF 10% 25V X5R 603-1

C7036 1UF 10% 25V X5R 603-1

PLACE_NEAR=Q7030.5:1.5mm

C7037 0.001UF 10% 50V X7R-CERM 0402

Max Current = 8A

f = 400 kHz

TO SYSTEM

C7025 0.22UF 10% 10V CERM 402

CRITICAL Q7030 RJK03P0DPA WPAK

CRITICAL L7030 4.7UH-17A PIMC104T4R7MN-SM

CRITICAL F7040 8AMP-24V 1206

=PPBUS_G3H

PPVBAT_G3H_CHGR_REG

CRITICAL C7040 62UF 20% 11V POLY CASE-B

CRITICAL C7041 62UF 20% 11V POLY CASE-B

CRITICAL C7043 62UF 20% 11V POLY CASE-B

C7045 1000PF 10% 16V X7R-CERM 0201

PLACE_NEAR=L7030.2:1.5mm

R7050 0.01 0.5% 1W MF 0612-1

CRITICAL Q7055 SI7615DN PWRPK-1212-8

TO/FROM BATTERY

PPVBAT_G3H_CONN

PPVBAT_G3H_CHGR_R

R7051 2.2 5% 1/20W MF 201

R7052 0 5% 1/20W MF 201

(CHGR_CSO_P)

(CHGR_CSO_N)

(PPVBAT_G3H_CHGR_R)

(CHGR_BGATE)

* R7051 HAS 2.2OHM TO COMPENSATE UNBALANCED VOLTAGE DUE TO DIFFERENT CURRENT ON _P AND _N. (FROM INTERSIL)

C7017 10UF 10% 25V X5R 805

C7014 1UF 10% 25V X5R 603-1

C7013 0.1UF 10% 25V X5R 402

C7012 0.01UF 10% 25V X7R 402

SYNC MASTER=J13 MLB NON POR SYNC DATE=11/10/2011

PAGE TITLE: PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

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PAGE 70 OF 109

SHEET 53 OF 73

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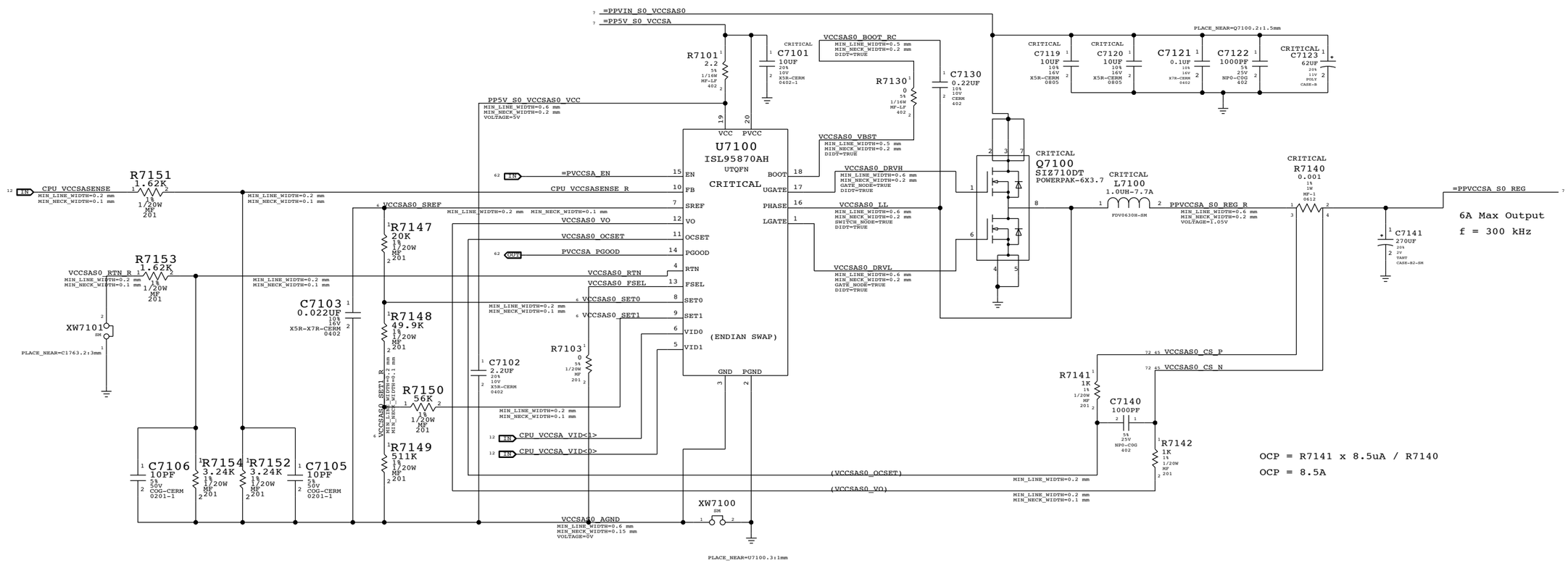

INTEL TABLE:

VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V
0	1	0.725V
1	1	0.675V

SYNC MASTER=J13 MLB NON POR — SYNC DATE=10/17/2011

PAGE TITLE: System Agent Supply

Apple Inc.

DRAWING NUMBER: 051-9277 — SIZE: D

REVISION: 2.8.0

BRANCH:

PAGE: 71 OF 109

SHEET: 54 OF 73

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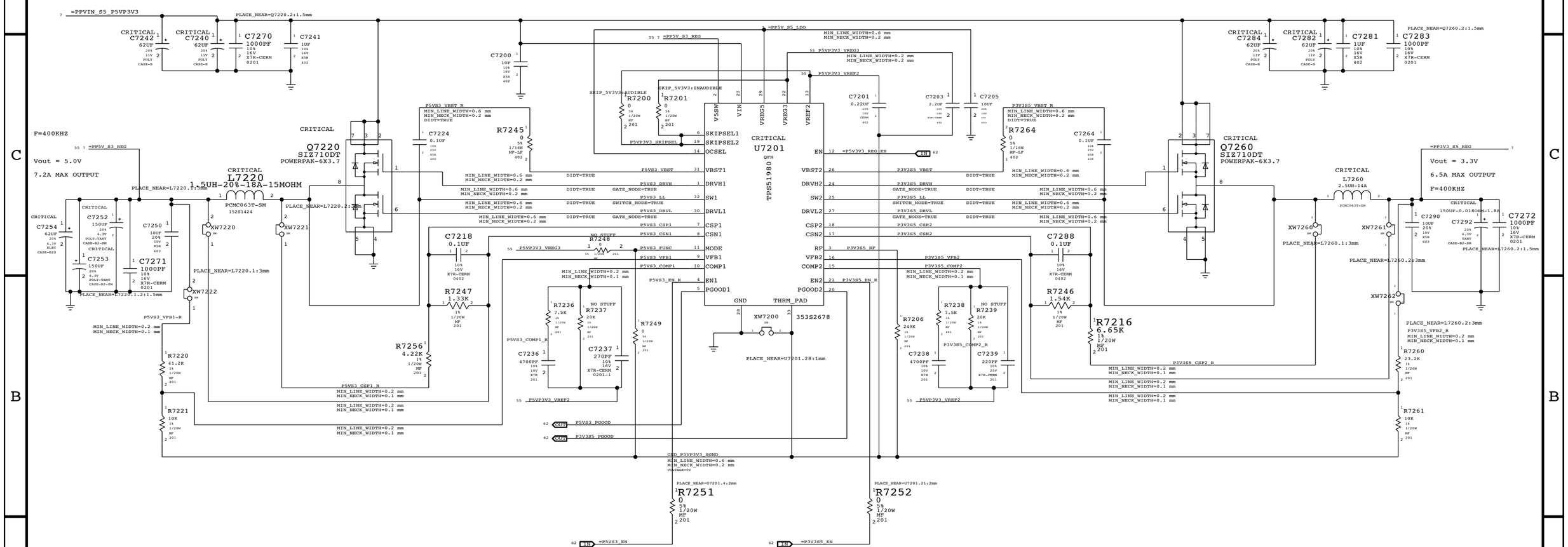

SYNC MASTER=J13 MLB NON POR	SYNC DATE=10/17/2011
PAGE TITLE	5V / 3.3V Power Supply
Apple Inc.	DRAWING NUMBER 051-9277 · SIZE D
	REVISION 2.8.0
	BRANCH
	PAGE 72 OF 109
	SHEET 55 OF 73

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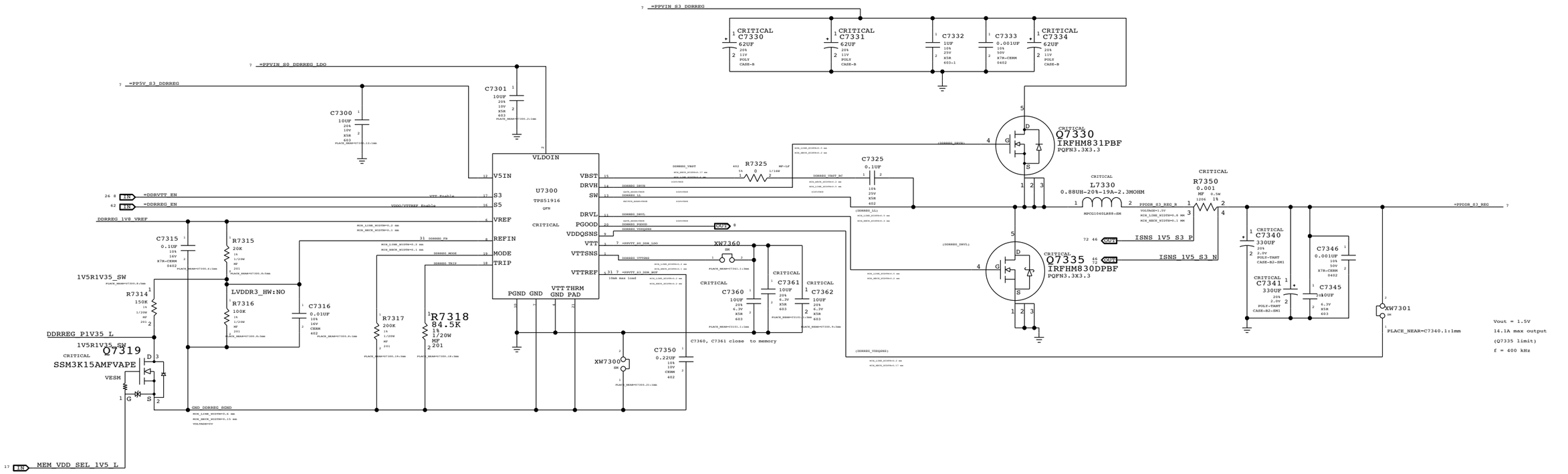

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0460	1	RES,MF,60.4KOHM,1,1/20W,0201	R7316		LVDDR3_HW:YES

If LVDDR3_HW:NO is turned ON, switch R2821 & R7971 back to the original value for 1.5V DDR unless 1V5R1V35_SW is turned ON

SYNC MASTER=J11 MLB SYNC DATE=12/02/201

PAGE TITLE

1.5V DDR3 Supply

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

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PAGE 73 OF 109

SHEET 56 OF 73

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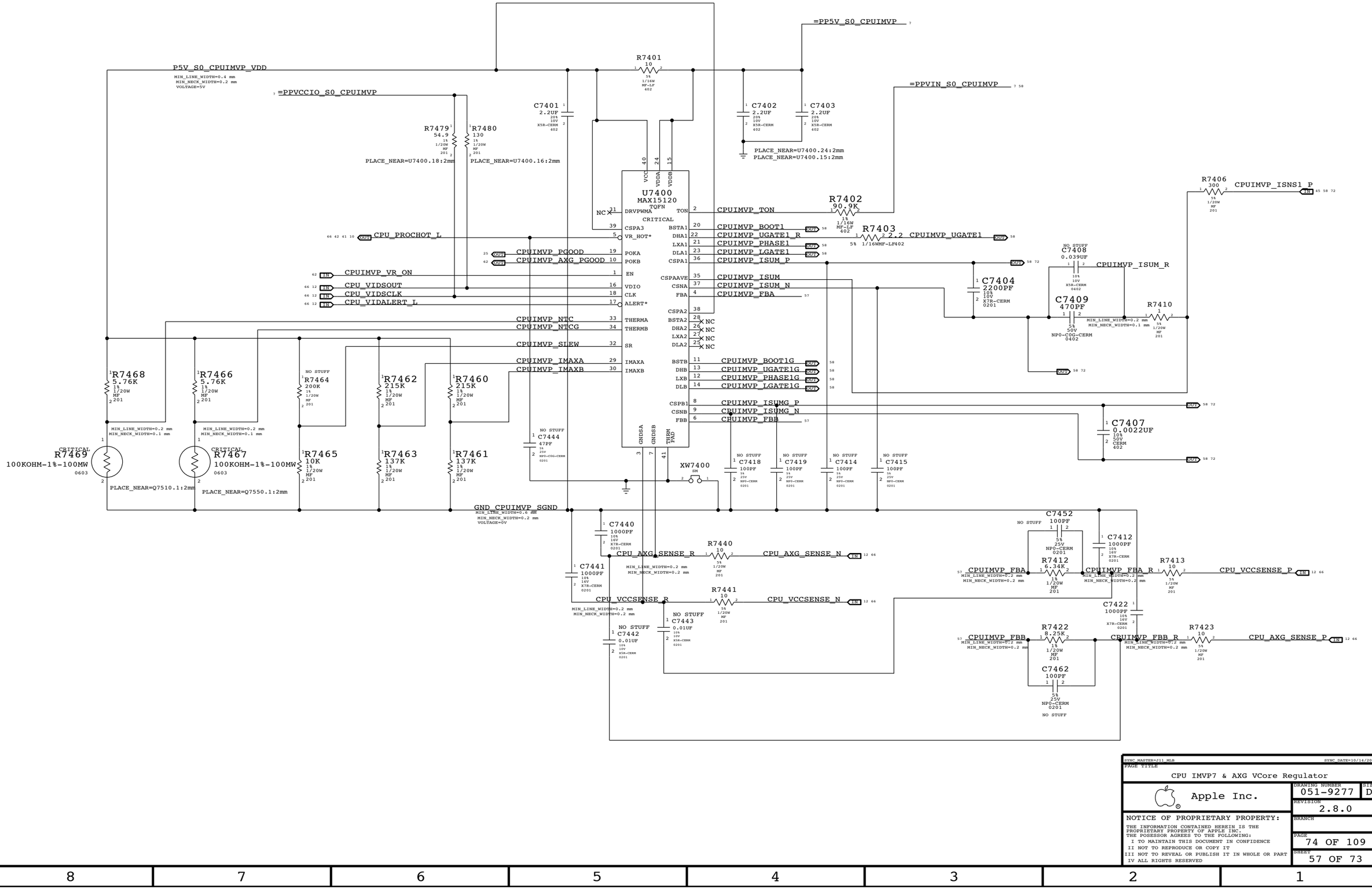

SYNC_MASTER=J11 MLB SYNC_DATE=10/14/201

PAGE TITLE

CPU IMVP7 & AXG VCore Regulator

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

BRANCH

PAGE 74 OF 109

SHEET 57 OF 73

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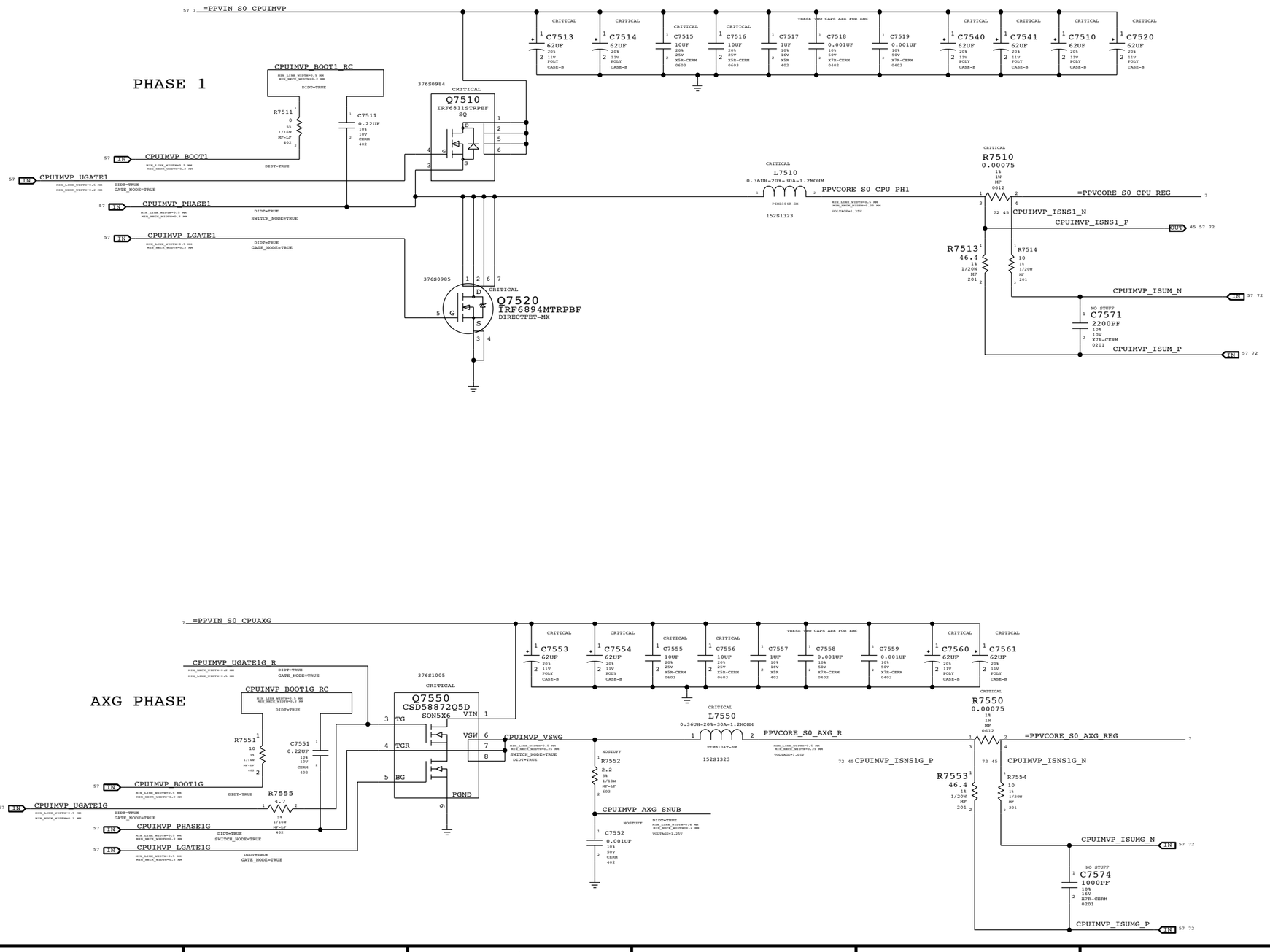
CPU=IV Bridge ULV, AXG=GT2



SYNC_MASTER=J13_MLB_MON_FOS	SYNC_DATE=10/17/2012
PAGE TITLE	CPU IMVP7 & AXG VCore Output
Apple Inc.	DRAWING NUMBER 051-9277 · SIZE D
	REVISION 2.8.0
	BRANCH
	PAGE 75 OF 109
	SHEET 58 OF 73

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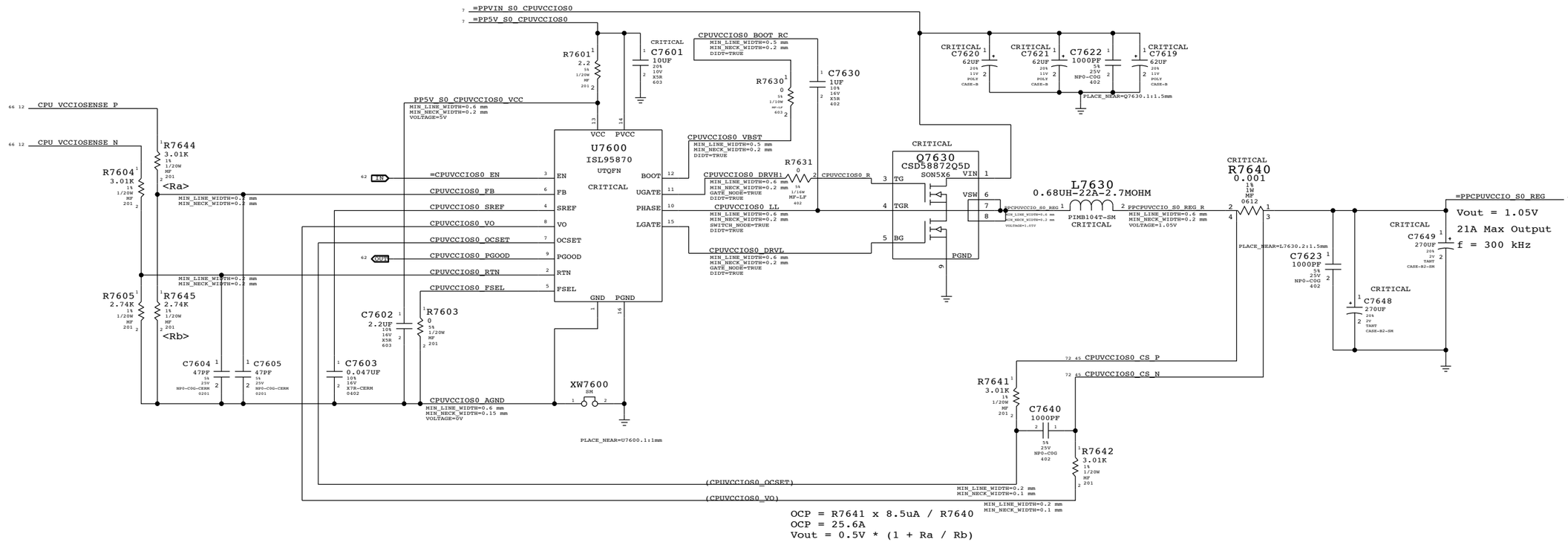
CPU VCCIO (1.05V S0) Regulator



SYNC_MASTER=J13_MLB_NON_POR SYNC_DATE=10/17/2011

PAGE TITLE

CPU VCCIO (1.05V) Power Supply

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

BRANCH

PAGE 76 OF 109

SHEET 59 OF 73

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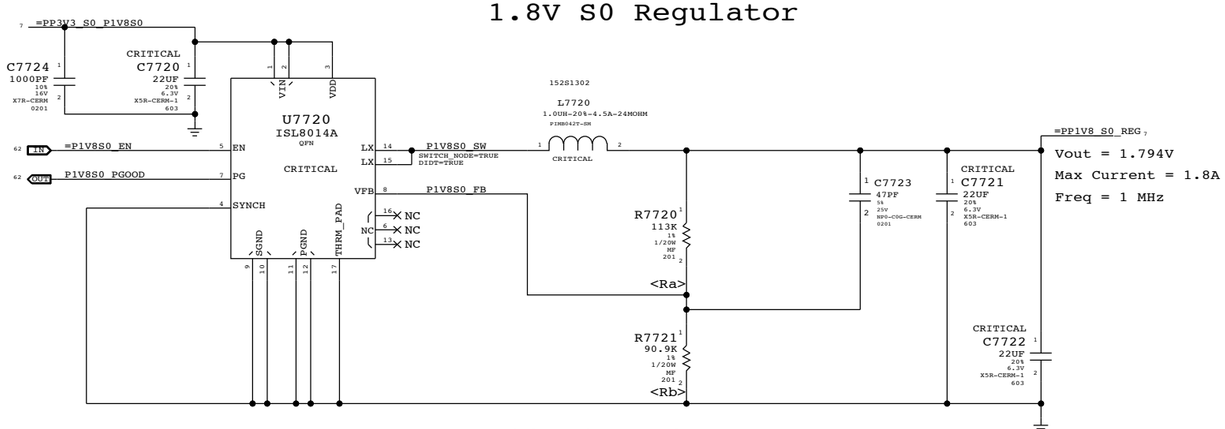
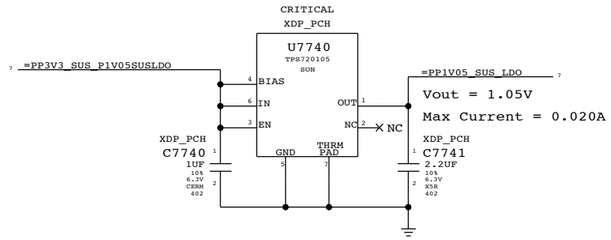
1.8V S0 Regulator



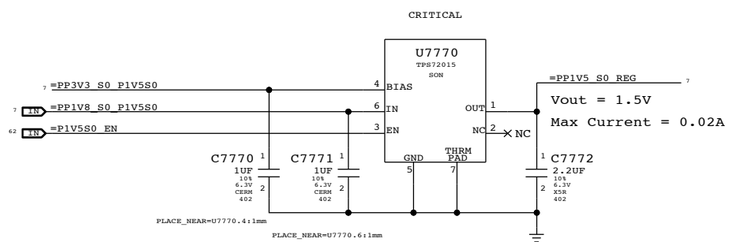
Vout = 0.8V * (1 + Ra / Rb)

1.05V SUS LDO

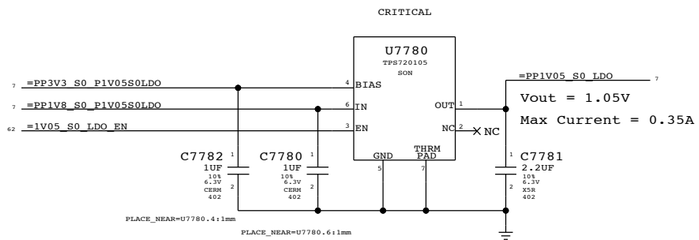
Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



1.5V S0 LDO



1.05V S0 LDO



SYNC MASTER=K21 MLB
SYNC DATE=07/28/2011

PAGE TITLE
Misc Power Supplies

Apple Inc.

DRAWING NUMBER 051-9277
SIZE D
REVISION 2.8.0
BRANCH
PAGE 77 OF 109
SHEET 60 OF 73

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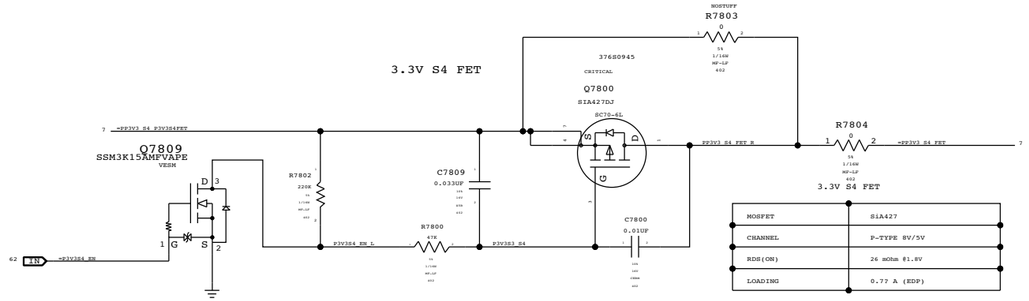

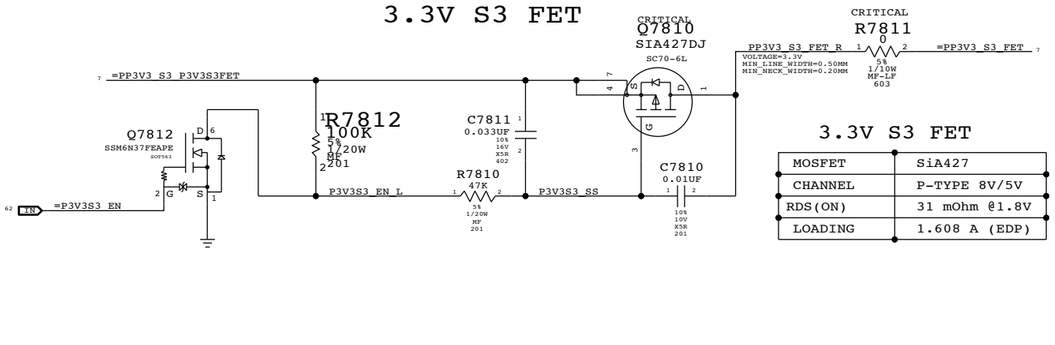

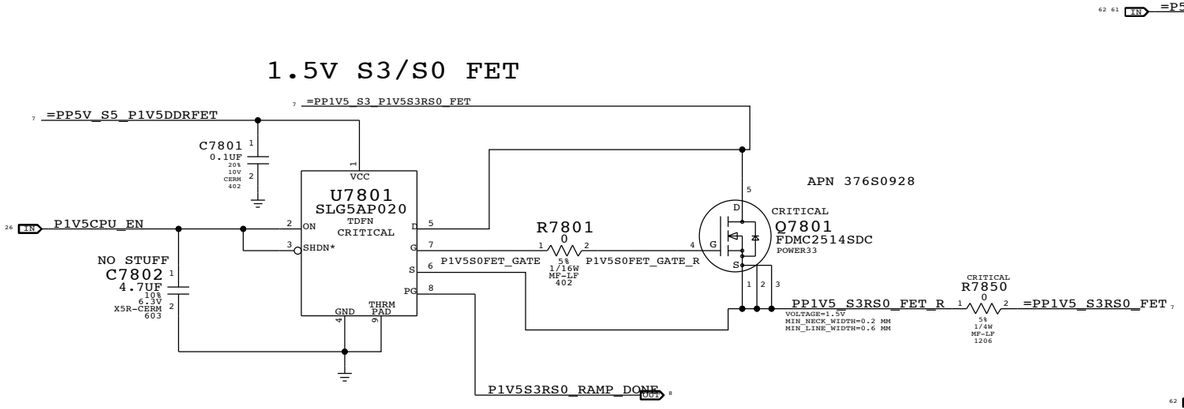

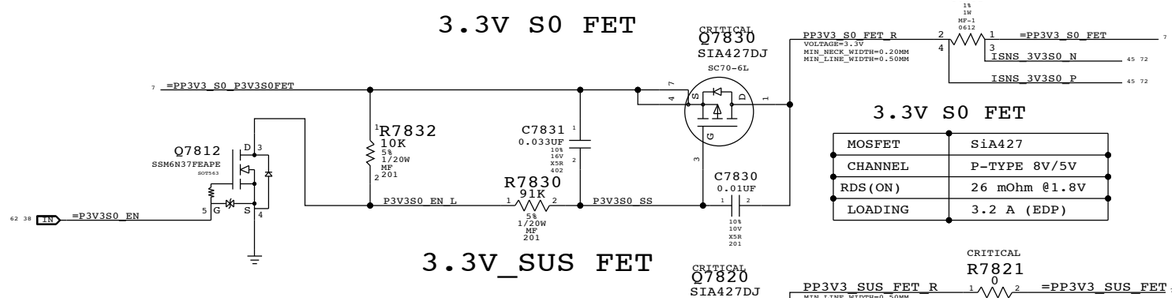

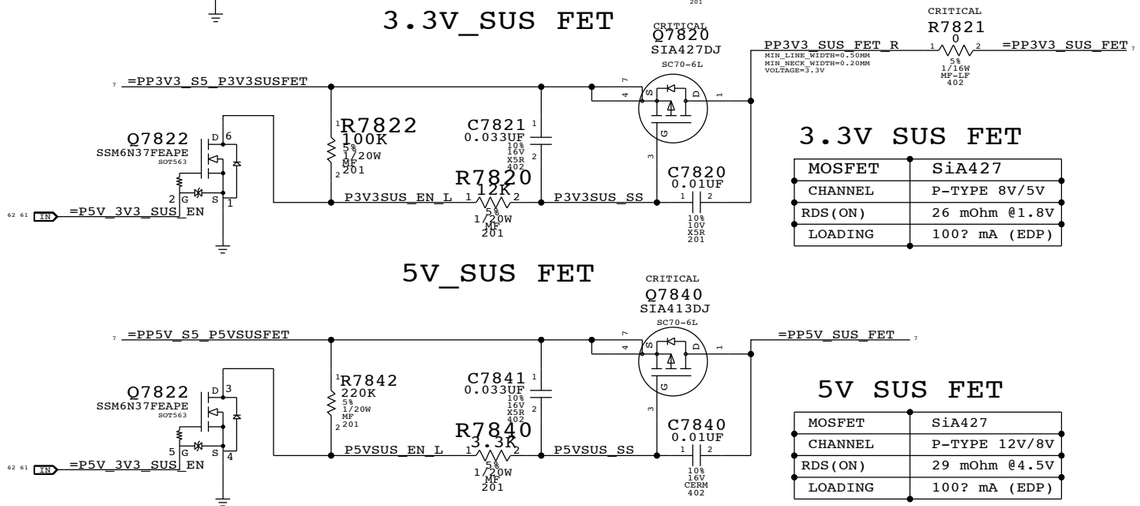

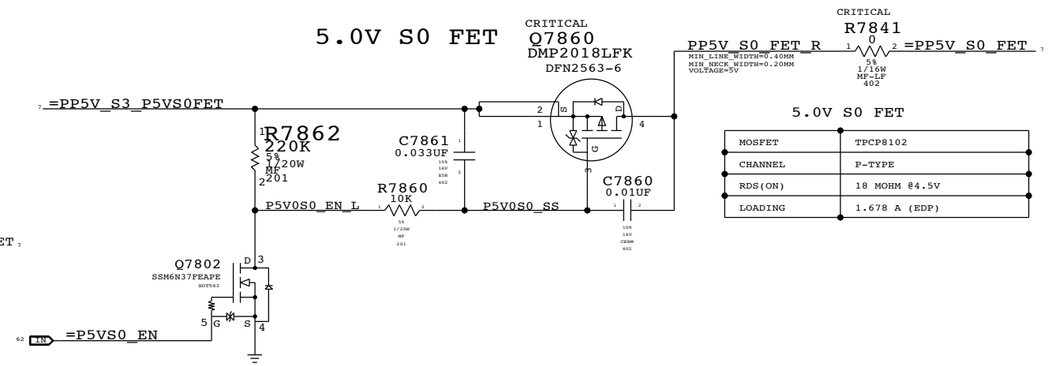

SYNC MASTER=K21 MLB SYNC DATE=07/28/2011

PAGE TITLE: Power FETs

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D
REVISION 2.8.0
BRANCH
PAGE 78 OF 109
SHEET 61 OF 73

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S5 Rail Enables & PGOOD

Internal pull-ups 100K +/- 20%

=PP3V42_G3H_PWRCTL

C7940 0.1UF 10% 6.3V X5R 201

U7941 SLG4AP012 TDFN — CRITICAL — 343S0497

SMC_PM_G2_EN — MAKE_BASE=TRUE

=PP3V3_S5_PWRCTL

Threshold: ??

DLY > 10 ms

S5PGOOD_DLY

C7941 220PF 10% 25V X7R-CERM 201

R7941 100 5% 1/20W MF 201

C7942 0.033UF 10% 16V X5R 402 — NO STUFF

P3V3S5_EN — MAKE_BASE=TRUE — =P3V3S5_EN

P5V3V3_REG_EN — MAKE_BASE=TRUE — =P5V3V3_REG_EN

S5_PWRGD — MAKE_BASE=TRUE

S5_PWRGD (old name RSMRST_PWRGD)-->SMC

SMC-->PM_DSW_PWRGD

Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SUS_EN	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (S4AC)	1	1	1	0	0	0	0
Deep Sleep (S4)	0	1	1	0	0	0	0
Deep Sleep (S5AC)	1	1	0	0	0	0	0
Deep Sleep (S5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

3.3V,5V S3 ENABLE

PM_SLP_S4_L — MAKE_BASE=TRUE

R7913 0 5% 1/20W MF 201 — P5VS3_EN — MAKE_BASE=TRUE — =P5VS3_EN

NO STUFF C7913 0.068UF 10% 10V CERM 402

PLACE_NEAR=U7300.16:6mm

R7911 5.1K 5% 1/20W MF 201

R7912 9.1K 5% 1/20W MF 201

PLACE_NEAR=Q7812.2:6mm

P3V3S3_EN — MAKE_BASE=TRUE — =P3V3S3_EN

DDRREG_EN — MAKE_BASE=TRUE — =DDRREG_EN

=USB_PWR_EN

C7910 0.47UF 10% 6.3V CERM-X5R 402

C7912 0.47UF 10% 6.3V CERM-X5R 402

U7970 DP S4 Power Enable

=PP3V3_S5_PWRCTL

C7970 0.1uF 20% 10V CERM 402

PM_SLP_S5_L:100K pull down on PCH page

PM_SLP_S5_L

U7970 74LVC1G32 SOT891

NC

P5V3V3_S4_EN — MAKE_WAIVE=TRUE — =TBTAPWRSW_EN — =P3V3S4_EN

SMC_S4_WAKESRC_EN — MAKE_BASE=TRUE

NOSTUFF R7915 0 5% 1/16W MF-LF 402

CPUVCORE ENABLE

ALL_SYS_PWRGD — R7974 0 5% 1/20W MF 201 — PLACE_NEAR=U7400.1:5mm — CPUIMVP_VR_ON

S0 ENABLE

PM_SLP_S3_L — R7978 100 5% 1/20W MF 201

PM_SLP_S3_R_L — MAKE_BASE=TRUE

(PM_SLP_S3_R_L)

R7987 33K 5% 1/20W MF 201 — PLACE_NEAR=U7100.15:6mm

R7981 20K 5% 1/20W MF 201 — PLACE_NEAR=U7600.3:6mm

R7988 39K 5% 1/20W MF 201 — PLACE_NEAR=U7770.3:6mm

R7986 5.1K 5% 1/20W MF 201 — PLACE_NEAR=U7720.5:6mm

=PP3V42_G3H_PWRCTL

R7931 10K 5% 1/20W MF 201

CHGR_VFRQ

Q7931 SSM3K15FV SOD-VESM-HF

=P5VS0_EN

=P3V3S0_EN

=PBUSVSENS_EN

=TBT_S0_EN

P1V8S0_EN — MAKE_BASE=TRUE — =P1V8S0_EN

P1V5S0_EN — MAKE_BASE=TRUE — =P1V5S0_EN

=1V05_S0_LDO_EN

CPUVCCIOS0_EN — MAKE_BASE=TRUE — =CPUVCCIOS0_EN

PVCCSA_EN — MAKE_BASE=TRUE — =PVCCSA_EN

C7987 0.47UF 10% 6.3V CERM-X5R 402

C7981 0.47UF 10% 6.3V CERM-X5R 402

C7988 0.47UF 10% 6.3V CERM-X5R 402

C7986 0.47UF 10% 6.3V CERM-X5R 402

CHGR VFRQ Generation

VFRQ Low: Fix Frequency

VFRQ High: Variable Frequency

S0 Rail PGOOD (BJT Version)

=PP3V3_S0_VMON — R7951 15K 1% 1/20W MF 201

R7952 7.15K 1% 1/20W MF 201

=PP3V3_S5_VMON — R7956 150K 1% 1/20W MF 201

S0PGD_C

R7953 1K 5% 1/20W MF 201 — VMON_3V3_DIV — VMON_Q2_BASE

R7954 1K 5% 1/20W MF 201 — =PP1V5_S3RS0_VMON — PP1V5_S3RS0 — VMON_Q3_BASE

R7955 1K 5% 1/20W MF 201 — =PP1V05_S0_VMON — VMON_Q4_BASE

Q7950 ASMCC0179 DFN2015H4-8 — Q1 Q2 Q3 Q4 — NC — CRITICAL

353S2809 S0PGD_BJT_GND_R

R7957 100 5% 1/20W MF 201

Worst-Case Thresholds:

Q2: 0.XXXV

Q3: 0.640V

3.3V w/Divider: 2.345V

Q4: 0.660V

3.3V/5.0V Sus ENABLE

=PP3V3_S5_PWRCTL — PLACE_NEAR=U7940.5:2.3mm — C7943 0.1UF 10% 6.3V X5R 201

SMC_BATLOW_L:100K pull up on SMC page

SMC_BATLOW_L

U7940 74AUP1G3208 SOT891

ALL_SYS_PWRGD

PM_SLP_SUS_L

PM_SUS_EN — MAKE_BASE=TRUE — =P5V_3V3_SUS_EN

NO STUFF R7917 0 5% 1/20W MF 201

3.3V SUS Detect

NO STUFF R7930 0 5% 1/20W MF 201

Could stuff R7930 to satisfy PCH power down timing tz35

=PP3V3_S5_PWRCTL — PLACE_NEAR=U7930.6:2.3mm

No stuff C7931, 12ms Min delay time

U7930 Sense input threhold is 3.07V

C7930 0.1UF 10% 6.3V X5R 201

=PP3V3_SUS_PWRCTL

R7933 100K 5% 1/20W MF 201

CRITICAL

U7930 TPS3808G33DBVRG4 SOT23-6 (90K IP9)

SENSE — RESET* — MR* — CT — GND

PM_RSMRST_L

PM_RSMRST_L goes to U1800.C21

C7931 1000PF 10% 16V X7R-CERM 0201

NO STUFF

SUS_PGOOD_MR_L

S0 Rail PGOOD Circuitry

(ISL Version in development)

Thresholds:

VDD: 2.734V-3.010V

V2MON: 2.815V-3.099V

V3MON: 0.572V-0.630V

V4MON: 0.572V-0.630V

=PP5V_S0_VMON — =PP1V5_S3RS0_VMON — =PP1V05_S0_VMON — =PP3V3_S0_VMON

S0PGOOD_ISL

C7960 0.1UF 10% 6.3V X5R 201

R7960 6.04K 1% 1/20W MF 201

R7970 10K 1% 1/20W MF 201

R7972 6.04K 1% 1/20W MF 201

R7961 15K 1% 1/20W MF 201

R7971 12.4K 1% 1/20W MF 201

R7973 15K 1% 1/20W MF 201

U7960 ISL88042IRTEZ TDFN (IPU) — CRITICAL — MR* — RST* — V2MON — V3MON — V4MON — VDD — GND — THRM_PAD

P5V_DIV_VMON — P1V5_DIV_VMON — P1V05_DIV_VMON

353S2310

ALL_SYS_PWRGD_R

P1V5S0_PGOOD from U7710

R7967 10K 5% 1/20W MF 201

NO STUFF R7968 100 5% 1/20W MF 201

CPUIMVP_AXG_PGOOD — R7966 100 5% 1/20W MF 201

P1V8S0_PGOOD — R7965 100 5% 1/20W MF 201

P3V3S5_PGOOD — R7901 100 5% 1/20W MF 201

P5V3V3_PGOOD — R7964 100 5% 1/20W MF 201

CPUVCCIOS0_PGOOD — R7963 100 5% 1/20W MF 201

PVCCSA_PGOOD — R7962 330 5% 1/20W MF 201

ALL_SYS_PWRGD

WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

PM_WLAN_EN_L

Q7925 2N7002DW-X-G SOT-363

AP_PWR_EN

(AC_EN_L)

AC_EN_L

Q7920 2N7002DW-X-G SOT-363

NO STUFF R7929 0 5% 1/20W MF 201

SMC_ADAPTER_EN

(PM_SLP_S3_L)

PM_SLP_S3_L

Q7925 2N7002DW-X-G SOT-363 — NC — Unused fet

SYNC MASTER=J13 MLB NON POR	SYNC DATE=11/10/2011
PAGE TITLE: Power Control 1/ENABLE	
Apple Inc.	DRAWING NUMBER: 051-9277
	SIZE: D
	REVISION: 2.8.0
	BRANCH:
	PAGE: 79 OF 109
	SHEET: 62 OF 73

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
518S0829	1	CONNWIN-AX,P=0.4,30P,W-BOSS,HF	J9000		

LCD Connector

Internal DP Connector: 518S0787

OMIT_TABLE
CRITICAL

J9000
CABLINE-CA
F-RT-SM

CHECK IF LVDS_IG_PANEL_PWR GLITCHES ON POWER UP

CRITICAL
U9000
FPF1009
MFET-2X2-8IN

=PP3V3_S3_LCD
LCD_IG_PWR_EN
ON
VIN_1
VIN_2
VOUT_1
VOUT_2
GND
THRM PAD

PP3V3_SW_LCD_UF
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

R9014 1K 5% 1/20W MF 201
C9009 0.1UF 10% 6.3V X5R 201
C9011 0.1UF 10% 6.3V X5R 201
C9012 10UF 20% 6.3V X5R 603

Pull-ups on panel side,
4.7 kOhm to 3.3V

=I2C_TCON_SDA
R9061 0 5% 1/20W MF 201
I2C_TCON_SDA_R

=I2C_TCON_SCL
R9062 0 5% 1/20W MF 201
I2C_TCON_SCL_R

DP_INT_HPD
R9060 0 5% 1/20W MF 201
DP_INT_HPD_CONN

L9004
FERR-120-OHM-1.5A
0402-LF

C9015 1000PF 10% 16V X7R-CERM 0201

PP3V3_SW_LCD
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

R9070 100K 5% 1/20W MF 201

DP_INT_AUX_CH_N
C9024 0.1UF 10% 16V X5R-CERM 0201
(DP_INT_AUX_CH_C_N)
DP_INT_AUX_CH_C_N

DP_INT_AUX_CH_P
C9025 0.1UF 10% 16V X5R-CERM 0201
(DP_INT_AUX_CH_C_P)
DP_INT_AUX_CH_C_P

DP_INT_ML_P<0>
C9020 0.1UF 10% 16V X5R-CERM 0201
DP_INT_ML_F_P<0>

DP_INT_ML_N<0>
C9021 0.1UF 10% 16V X5R-CERM 0201
DP_INT_ML_F_N<0>

PPVOUT_SW_LCDBKLT

LED_RETURN_6
LED_RETURN_5
LED_RETURN_4
LED_RETURN_3
LED_RETURN_2
LED_RETURN_1

LED Backlight I/F

DisplayPort I/F

PLACE_NEAR=J9000.25:1mm
R9017 1M 5% 1/20W MF 201
PLACE_NEAR=J9000.24:1mm
R9018 1M 5% 1/20W MF 201

PLACE_NEAR=J9000.14:2mm
R9050 100K 5% 1/20W MF 201
R9080 100K 5% 1/20W MF 201

PLACE_NEAR=J9000.3:2mm
C9017 1000PF 5% 50V COG-CERM 603

SYNC MASTER=K21 MLB
SYNC DATE=07/28/2011

PAGE TITLE
Internal DisplayPort Connector

Apple Inc.

DRAWING NUMBER 051-9277
SIZE D
REVISION 2.8.0
BRANCH
PAGE 90 OF 109
SHEET 63 OF 73

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3.3V/HV Power MUX

V3P3 must be S4 to support wake from Thunderbolt devices.

=PP3V3_S4_TBTAPWRSW

=PPHV_SW_TBTAPWRSW
18.9V Max

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)

C9487 100UF 20% 6.3V POLY-TANT CASE-B2-SM (CRITICAL)
C9480 22UF 20% 6.3V X5R-CERM-1 603 (CRITICAL)
C9481 0.1UF 10% 16V X5R-CERM 0201
C9415 4.7UF 10% 25V X5R-CERM 0603
C9410 0.1UF 10% 25V X5R 402

CRITICAL
U9410
CD3210A0RGP
QFN

Pin	Name
19, 20	V3P3
6, 7	VHV
16	RSVD
5	EN
11	HV_EN
17	S0
18	V3P3OUT
12, 14	OUT
15	RSVD
8	ISET_V3P3
10	ISET_S0
9	ISET_S3
GND, THRM PAD	1, 2, 3, 4, 13, 21

=TBTAPWRSW_EN
TBT_A_HV_EN
=TBT_S0_EN

C9485 0.1UF 10% 16V X5R-CERM 0201
C9486 10UF 20% 6.3V CERM-X5R 0402
C9411 0.1UF 10% 25V X5R 402

PP3V3_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

PPHV_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V

TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3
TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R

TBTHV:P15V
R9410 22.6K 1% 1/20W MF 201 (12V: See below)
R9411 22.6K 1% 1/20W MF 201
R9412 36.5K 1% 1/20W MF 201
R9413 22.6K 1% 1/20W MF 201
R9414 22.6K 1% 1/20W MF 201

Single-fault protection requires two R's per HV ISET_Sx with CD3210. Single R on ISET_V3P3 OK.

ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MF,1/20W,17.8K,1,0201	R9410,R9413		TBTHV:P12V
118S0145	2	RES,MF,1/20W,17.8K,1,0201	R9411,R9414		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

PP3V3_SW_TBTAPWR
C9420 0.1UF 10% 16V X5R-CERM 0201
C9421 0.1UF 10% 16V X5R-CERM 0201
R9427 10K 5% 1/20W MF 201
R9429 100K 5% 1/20W MF 201

SIGNAL_MODEL=TBT_MUX

TBT_A_CIO_SEL	1	BIASIN	
DP_AUXIO_EN	2	AUXIO_EN	
DP_TBTPA_AUXCH_N	7	AUX-	
DP_TBTPA_AUXCH_P	8	AUX+	
DP_TBTSNK0_DDC_DATA	4	DDC_DAT	
DP_TBTSNK0_DDC_CLK	5	DDC_CLK	
TBT_A_CONFIG1_BUF	16	CA_DETOUT	
DP_TBTPA_ML_P<1>	11	DP+	
DP_TBTPA_ML_N<1>	10	DP-	
TBT_A_LSTX	14	LSTX	
TBT_A_LSRX_UNBUF	13	LSRX	
TBT_A_DP_PWRDN	6	DP_PD	
DP_TBTPA_HPD	12	HPDOUT	
BIASOUT	24		
AUXIO-	23		
AUXIO+	22		
CA_DET	18		
DPMLO+	19		
DPMLO-	20		
HPD	17		

VDD
CRITICAL
U9420
CBTL05023
HVQFN

TBT_A_BIAS (VOLTAGE=3.3V)
C9425 0.1UF 10% 16V X5R-CERM 0201

DP_A_AUXCH_DDC_N
DP_A_AUXCH_DDC_P
TBT: RX_1 Bias Sink

TBT_A_CONFIG1_RC
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)
TBT_A_HPD

C9430 0.1UF 10% 16V X5R-CERM 0201
C9431 0.1UF 10% 16V X5R-CERM 0201
C9432 0.22UF 20% 6.3V X5R 0201
C9433 0.22UF 20% 6.3V X5R 0201

DP_TBTPA_AUXCH_C_N
DP_TBTPA_AUXCH_C_P
DP_TBTPA_ML_C_P<1>
DP_TBTPA_ML_C_N<1>

R9426 1M 5% 1/20W MF 201
R9428 100K 5% 1/20W MF 201

PP3V3_SW_TBTAPWR
CRITICAL
U9460
74AUP1T97
SOT891
VCC
GND
C9460 0.1UF 20% 10V CERM 402
TBT_A_LSRX
Y = B

Thunderbolt Connector A

L9400 FERR-120-OHM-3A 0603
C9400 0.01UF 10% 50V X7R-CERM 0402
PP3V3RHV_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V
R9401 12 5% 1/20W MF 201
TBTACONN_20_RC
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
C9401 0.01UF 10% 50V X7R-CERM 0402

For J9400 TBT SMT pads (3, 5, 17 & 19):
GND_VOID=TRUE
CRITICAL
J9400
MDP-J11
F-RT-TH

2	HOT_PLUG_DETECT	GND	1
4	CONFIG1	ML_LANE0P	3
6	CONFIG2	ML_LANE0N	5
13	GND	GND	7
10	ML_LANE3P	ML_LANE1P	9
12	ML_LANE3N	ML_LANE1N	11
14	GND	GND	8
16	AUX_CHP	ML_LANE2P	15
18	AUX_CHN	ML_LANE2N	17
20	DP_PWR	RETURN	19
SHIELD PINS	26, 27, 28, 29, 30, 31, 32, 33		

514-0818

TBTACONN_1_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
C9405 0.01UF 10% 25V X5R-CERM 0201

(0-18.9V)
DP Dir
TBT Dir
TBT: TX_0

TBTACONN_7_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
C9406 0.01UF 10% 25V X5R-CERM 0201

(0-18.9V)
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_R2P/P2R (P/N)

TBT_A_R2D_P<1>
TBT_A_R2D_N<1>
TBT: TX_1

GND_VOID=TRUE (Both C's)
C9470 0.22UF
C9471 0.22UF
TBT_A_R2D_C_P<0>
TBT_A_R2D_C_N<0>
R9470 470K 5% 1/20W MF 201
R9471 470K 5% 1/20W MF 201

C9472 0.22UF
C9473 0.22UF
TBT_A_R2D_C_P<1>
TBT_A_R2D_C_N<1>
R9472 470K 5% 1/20W MF 201
R9473 470K 5% 1/20W MF 201

470k R's for ESD protection on AC-coupled signals.

C9474 0.47UF
C9475 0.47UF
TBT_A_D2R_P<0>
TBT_A_D2R_N<0>
TBT_A_D2R_C_P<0>
TBT_A_D2R_C_N<0>
R9494 1K 5% 1/20W MF 201 (SIGNAL_MODEL=EMPTY)
R9495 1K 5% 1/20W MF 201 (SIGNAL_MODEL=EMPTY)

C9478 0.22UF
C9479 0.22UF
DP_TBTPA_ML_C_P<3>
DP_TBTPA_ML_C_N<3>
DP_TBTPA_ML_P<3>
DP_TBTPA_ML_N<3>
TBT: Unused
R9478 470K 5% 1/20W MF 201
R9479 470K 5% 1/20W MF 201

TBT_A_BIAS
R9498 2.2K 5% 1/20W MF 201
R9499 2.2K 5% 1/20W MF 201

C9476 0.47UF
C9477 0.47UF
TBT_A_D2R_P<1>
TBT_A_D2R_N<1>
TBT_A_D2R_C_P<1>
TBT_A_D2R_C_N<1>

CRITICAL
SIGNAL_MODEL=TBTPIN
GND_VOID=TRUE
D9498 BAR90-02LRH TSLP-2-7
D9499 BAR90-02LRH TSLP-2-7
TBT_A_D2R1_AUXDDC_P
TBT_A_D2R1_AUXDDC_N

CRITICAL
L9498 650NH-5%-0.430MA-0.52OHM 0603
L9499 650NH-5%-0.430MA-0.52OHM 0603
SIGNAL_MODEL=EMPTY

DP_A_AUXCH_DDC_P
DP_A_AUXCH_DDC_N
C9498 30PF 5% 50V C0G-NP0 0402
C9499 30PF 5% 50V C0G-NP0 0402

TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC
R9452 1M 5% 1/20W MF 201
R9451 1M 5% 1/20W MF 201
C9494 330PF 10% 16V X7R-CERM 0201
C9495 330PF 10% 16V X7R-CERM 0201
R9441 100K 5% 1/20W MF 201

C9402 0.01UF 10% 25V X5R-CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

SYNC MASTER=J11 MLB	SYNC DATE=10/03/2011
PAGE TITLE	Thunderbolt Connector A
Apple Inc.	DRAWING NUMBER 051-9277
	SIZE D
	REVISION 2.8.0
	BRANCH
	PAGE 94 OF 109
	SHEET 64 OF 73

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PPBUS S0 LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.65 A (EDP)

CRITICAL
Q9706
FDC638APZ_SSM6001
SSOT6-MF

F9700
3AMP-32V-467
603-MF
BOTTOM

=PPBUS_S0_LCDBKLT
PPBUS_S0_LCDBKLT_FUSED
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V

PPBUS_SW_LCDBKLT_PWR
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
8 65

THERE IS A SENSE RESISTOR BETWEEN
PPBUS_SW_LCDBKLT_PWR
AND PPBUS_SW_BKL
ON THE SENSOR PAGE

*C9797 AND C9799 SHOULD BE PLACED IN T-BONE FOR ACOUSTICS
*PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
*LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

R9788 301K 1% 1/20W MF 201
C9782 0.1UF 10% 16V X7R-CERM 0402
LCDBKLT_EN_DIV
R9789 147K 1% 1/20W MF 201
LCDBKLT_EN_L

Q9707 SSM6N15FEAPE SOT563
LCD_BKLT_EN
LCDBKLT_DISABLE
Q9707 SSM6N15FEAPE SOT563
BKLT_PLT_RST_L

=PP5V_S0_BKL
=PPBUS_SW_BKL
CRITICAL
L9701
15UH-2.8A
PIMB053T-SM
PPBUS_SW_LCDBKLT_PWR_SW
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.150 MM
VOLTAGE=50V
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL
C9712 10UF 10% 25V X5R 805
C9713 0.1UF 10% 25V X5R 402
PLACE_NEAR=L9701.1:3mm
PLACE_NEAR=L9701.1:3mm

PLACE_NEAR=L9701.2:3mm
CRITICAL
D9701
SOD-123
RB160M-60G
PLACE_NEAR=U9701.A5:3mm
C9796 220PF 10% 50V X7R-CERM 0402
CRITICAL
C9797 10UF 10% 50V X5R 1210-1
CRITICAL
C9799 10UF 10% 50V X5R 1210-1
PLACE_NEAR=D9701.2:5mm
PLACE_NEAR=D9701.2:3mm
PPVOUT_SW_LCDBKLT
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.375 MM
VOLTAGE=50V
6 63

PLACE_NEAR=U9701.D1:5mm
C9710 1UF 10% 25V X5R 603-1
PLACE_NEAR=U9701.D1:3mm
C9714 0.01UF 10% 10V X5R 201

=PP3V3_S0_BKL_VDDIO
PLACE_NEAR=U9701.C4:4mm
C9711 0.1UF 10% 6.3V X5R 201

XW9720
SM
PLACE_NEAR=C9797.1:5mm
PPVOUT_SW_LCDBKLT_FB
VOLTAGE=50V
MIN_LINE_WIDTH=0.1 MM
MIN_NECK_WIDTH=0.1 MM

U9701
25-BUMP-MICRO
LP8550

	VDDIO	VLDO	VIN
BKL_VSYNC_R	D2	VSYNC	CRITICAL SW_0 B1
			SW_1 B2
BKL_FLTR	C2	FILTER	
BKL_ISET	B3	ISET	
BKL_FSET	B4	FSET	
BKL_SCL	D3	SCLK	
BKL_SDA	D4	SDA	
BKL_PWM	A4	PWM	
BKL_EN	A3	EN	
TP_BKL_FAULT	C3	FAULT	
		FB	A5
		OUT1	E5 BKL_ISEN1
		OUT2	D5 BKL_ISEN2
		OUT3	C5 BKL_ISEN3
		OUT4	E3 BKL_ISEN4
		OUT5	E2 BKL_ISEN5
		OUT6	E1 BKL_ISEN6
	B5	GND_S	
	E4	GND_L	
	A1	GND_SW	
	A2	GND_SW	

R9741 10K 5% 1/20W MF 201
R9753 0 5% 1/20W MF 201
R9757 0 5% 1/20W MF 201
=I2C_BKL_1_SCL
=I2C_BKL_1_SDA
Addr: 0x58(Wr)/0x59(Rd)
PPBUS_SW_LCDBKLT_PWR
R9731 200K 1% 1/20W MF 201
R9715 100K 1% 1/20W MF 201
PLACE_SIDE=BOTTOM
R9704 33 5% 1/20W MF 201
LCD_BKLT_PWM
C9704 33PF 5% 25V NPO-COG 0201

Fpwm=9.62kHz
see spec for others
R9755 10K 1% 1/20W MF 201
R9716 90.9K 1% 1/20W MF 201
I_LED=20.3mA
R9714 18.2K 1% 1/20W MF 201
GND_BKL_SGND
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0V
XW9710
SM
PLACEMENT_NOTE=Keep away from noise nodes(E4, A1, A2, B1, B2 pins)

I_LED=369/Riset
(EEPROM should set EN_I_RES=1)

BKLT:PROD
R9717 0 5% 1/16W MF-LF 402
PLACE_NEAR=U9701.E5:10mm
LED_RETURN_1
BKLT:PROD
R9718 0 5% 1/16W MF-LF 402
PLACE_NEAR=U9701.D5:10mm
LED_RETURN_2
BKLT:PROD
R9719 0 5% 1/16W MF-LF 402
PLACE_NEAR=U9701.C5:10mm
LED_RETURN_3
BKLT:PROD
R9720 0 5% 1/16W MF-LF 402
PLACE_NEAR=U9701.E3:10mm
LED_RETURN_4
BKLT:PROD
R9721 0 5% 1/16W MF-LF 402
PLACE_NEAR=U9701.E2:10mm
LED_RETURN_5
BKLT:PROD
R9722 0 5% 1/16W MF-LF 402
PLACE_NEAR=U9701.E1:10mm
LED_RETURN_6
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.20 mm
BOTTOM
OUT 6 63

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC MASTER=K21 MLB
SYNC DATE=07/28/2011
PAGE TITLE
LCD Backlight Driver
Apple Inc.
DRAWING NUMBER 051-9277
SIZE D
REVISION 2.8.0
BRANCH
PAGE 97 OF 109
SHEET 65 OF 73

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.100 MM	0.100 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_AGTL	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_8MIL	*	*	CPU_8MIL_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_8MIL_2ANY	*	8 MIL	?

Note: CPU_8MIL and CPU_ITP can be converted back to TABLE_SPACING_RULE once rdar://10308147 is resolved

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_ITP	*	*	CPU_ITP_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ITP_2ANY	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	CPU_COMP	*	CPU_COMP_2SELF
CPU_COMP	*	*	CPU_COMP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_COMP_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	*	=4x_DIELECTRIC	?
CPU_COMP_2OTHER	*	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	CPU_VCCSENSE	*	CPU_VCCSENSE_2SELF
CPU_VCCSENSE	*	*	CPU_VCCSENSE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	*	=4x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	*	=6x_DIELECTRIC	?

PCI-Express Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
CLK_PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

PCIE Clock Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	CLK_PCIE	*	CLK_PCIE_2SELF
CLK_PCIE	*	*	CLK_PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CLK_PCIE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	*	=4x_DIELECTRIC	?
CLK_PCIE_2OTHER	*	=6x_DIELECTRIC	?

CPU PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_CPU_TX	PCIE_CPU_TX	*	PCIE_TX2TX
PCIE_CPU_RX	PCIE_CPU_RX	*	PCIE_RX2RX
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2OTHERTX
PCIE_CPU_RX	*_CPU_RX	*	PCIE_RX2OTHERRX
PCIE_CPU_TX	*_CPU_RX	*	PCIE_TX2RX
PCIE_CPU_RX	*_CPU_TX	*	PCIE_RX2TX
PCIE_CPU_TX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*	*	PCIE_2OTHER
PCIE_CPU_RX	*	*	PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	*	=2.5x_DIELECTRIC	?
PCIE_RX2RX	*	=2.5x_DIELECTRIC	?
PCIE_TX2OTHERTX	*	=4x_DIELECTRIC	?
PCIE_RX2OTHERRX	*	=4x_DIELECTRIC	?
PCIE_TX2RX	*	=6x_DIELECTRIC	?
PCIE_RX2TX	*	=6x_DIELECTRIC	?
PCIE_2OTHERHS	*	=4x_DIELECTRIC	?
PCIE_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

CPU Net Properties

NET_TYPE ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
DMI_S2N	PCIE_80D	PCIE_PCH_TX	DMI_S2N_P<3:0>	9 17
DMI_S2N	PCIE_80D	PCIE_PCH_TX	DMI_S2N_N<3:0>	9 17
DMI_N2S	PCIE_80D	PCIE_PCH_RX	DMI_N2S_P<3:0>	9 17
DMI_N2S	PCIE_80D	PCIE_PCH_RX	DMI_N2S_N<3:0>	9 17
FDI_DATA	PCIE_80D	PCIE_PCH_RX	FDI_DATA_P<7:0>	9 17
FDI_DATA	PCIE_80D	PCIE_PCH_RX	FDI_DATA_N<7:0>	9 17
	CPU_45S	CPU_AGTL	FDI_FSYNC<1..0>	9 17
	CPU_45S	CPU_AGTL	FDI_LSYNC<1..0>	9 17
	CPU_45S	CPU_AGTL	FDI_INT	9 17
CPU_PECI	CPU_45S	CPU_COMP	CPU_PECI	10 19 42
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	10 17
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	10 17 26
	CPU_45S	CPU_ITP	XDP_DBRESET_L	10 23 25
	CPU_45S	CPU_ITP	XDP_CPU_PRDY_L	10 23
	CPU_45S	CPU_ITP	XDP_CPU_PREQ_L	10 23
	CPU_27P4S	CPU_COMP	EDP_COMP	9
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>	10
	CPU_45S	CPU_ITP	CPU_CFG<11..0>	9 23
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L	10 41
	CPU_45S	CPU_AGTL	CPU_VCCIO_SEL	12
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	10 41 42 57
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD	10 19 23
PM_THRMTRIP_L	CPU_45S	CPU_8MIL	PM_THRMTRIP_L	10 19 42
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_P	10 16
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_N	10 16
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKP	8 10
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKN	8 10
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_P	10 16
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_N	10 16
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_P	16 23
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_N	16 23
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_P	23
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_N	23
XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI	10 23
XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO	10 23
XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS	10 23
XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK	10 23
XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPU_TRST_L	10 23
XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<3..0>	10 23
XDP_BPM_L_R_CFG	CPU_45S	CPU_ITP	XDP_BPM_L<7..4>	10 23
(XDP_BPM_L_R_CFG)	CPU_45S	CPU_ITP	XDP_OBSDATA_B<3..0>	23
(XDP_BPM_L_R_CFG)	CPU_45S	CPU_ITP	CPU_CFG<15..12>	9 23
(FSB_CPURST_L)	CPU_45S	CPU_ITP	XDP_CPURST_L	23
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_P	12 57
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_N	12 57
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_P	12 59
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_N	12 59
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_P	12 57
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_N	12 57
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_P	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_N	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	9
CPU_SVIDALERT_L	CPU_45S	CPU_COMP	CPU_VIDALERT_L	12 57
CPU_SVIDSCLK	CPU_45S	CPU_COMP	CPU_VIDSCLK	12 57
CPU_SVIDSOUT	CPU_45S	CPU_COMP	CPU_VIDSOUT	12 57
PCIE_CPU_MUX_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_P<0>	8 38
PCIE_CPU_MUX_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_N<0>	8 38
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_MUX_IN_P	38
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_MUX_IN_N	38
PCIE_CPU_MUX_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<0>	8 38
PCIE_CPU_MUX_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<0>	8 38
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_MUX_OUT_P	38
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_MUX_OUT_N	38
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_R2D_C_P<1>	8 38
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_R2D_C_N<1>	8 38
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_P<1>	6 38
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_N<1>	6 38
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<1>	6 8 38
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<1>	6 8 38
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_P<1>	
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_N<1>	
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_P	6 16 38
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_N	6 16 38
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_P<3..0>	9 63
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_N<3..0>	9 63
	DP_80D	DP_TX	DP_INT_ML_F_P<3..0>	6 63
	DP_80D	DP_TX	DP_INT_ML_F_N<3..0>	6 63
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_P	6 63
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_N	6 63
	DP_80D	DP_AUX	DP_INT_AUX_CH_P	9 63
	DP_80D	DP_AUX	DP_INT_AUX_CH_N	9 63

DMI/FDI

PCIe SSD

DP

Note: DisplayPort tables are on Page 103

SYNC MASTER=J13 CONSTRAINTS SYNC DATE=01/11/2012

PAGE TITLE

CPU Constraints

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

BRANCH

PAGE 100 OF 109

SHEET 66 OF 73

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM_CMD2CTRL	*	=3x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=PWR_P2MM	?
MEM_2GND	*	=GND_P2MM	?
MEM_2OTHER	*	=6x_DIELECTRIC	?

PalPilot Spacing	"Real" Spacing
=2x_DIELECTRIC	=2x_DIELECTRIC
=5.7x_DIELECTRIC	=3x_DIELECTRIC
=4x_DIELECTRIC	=3x_DIELECTRIC
=4x_DIELECTRIC	=3x_DIELECTRIC
=4x_DIELECTRIC	=3x_DIELECTRIC
=8.6x_DIELECTRIC	=6x_DIELECTRIC
=5.7x_DIELECTRIC	=4x_DIELECTRIC
=PWR_P2MM	=PWR_P2MM
=GND_P2MM	=GND_P2MM
=8.6x_DIELECTRIC	=6x_DIELECTRIC

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	*	*	MEM_2OTHER
MEM_A_DQS_1	*	*	MEM_2OTHER
MEM_A_DQS_2	*	*	MEM_2OTHER
MEM_A_DQS_3	*	*	MEM_2OTHER
MEM_A_DQS_4	*	*	MEM_2OTHER
MEM_A_DQS_5	*	*	MEM_2OTHER
MEM_A_DQS_6	*	*	MEM_2OTHER
MEM_A_DQS_7	*	*	MEM_2OTHER
MEM_B_DQS_0	*	*	MEM_2OTHER
MEM_B_DQS_1	*	*	MEM_2OTHER
MEM_B_DQS_2	*	*	MEM_2OTHER
MEM_B_DQS_3	*	*	MEM_2OTHER
MEM_B_DQS_4	*	*	MEM_2OTHER
MEM_B_DQS_5	*	*	MEM_2OTHER
MEM_B_DQS_6	*	*	MEM_2OTHER
MEM_B_DQS_7	*	*	MEM_2OTHER
MEM_A_DATA_0	*	*	MEM_2OTHER
MEM_A_DATA_1	*	*	MEM_2OTHER
MEM_A_DATA_2	*	*	MEM_2OTHER
MEM_A_DATA_3	*	*	MEM_2OTHER
MEM_A_DATA_4	*	*	MEM_2OTHER
MEM_A_DATA_5	*	*	MEM_2OTHER
MEM_A_DATA_6	*	*	MEM_2OTHER
MEM_A_DATA_7	*	*	MEM_2OTHER
MEM_B_DATA_0	*	*	MEM_2OTHER
MEM_B_DATA_1	*	*	MEM_2OTHER
MEM_B_DATA_2	*	*	MEM_2OTHER
MEM_B_DATA_3	*	*	MEM_2OTHER
MEM_B_DATA_4	*	*	MEM_2OTHER
MEM_B_DATA_5	*	*	MEM_2OTHER
MEM_B_DATA_6	*	*	MEM_2OTHER
MEM_B_DATA_7	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0>	8 11 27 28 32
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0>	8 11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM_A_CKE<3..0>	11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM_A_CS_L<3..0>	11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM_A_ODT<3..0>	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM_A_A<15..0>	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM_A_BA<2..0>	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM_A_RAS_L	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM_A_CAS_L	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM_A_WE_L	11 27 28 32
MEM_A_DQ_BYTE0	MEM_45S	MEM_A_DATA_0	MEM_A_DQ<7..0>	11 27
MEM_A_DQ_BYTE1	MEM_45S	MEM_A_DATA_1	MEM_A_DQ<15..8>	11 27
MEM_A_DQ_BYTE2	MEM_45S	MEM_A_DATA_2	MEM_A_DQ<23..16>	11 27
MEM_A_DQ_BYTE3	MEM_45S	MEM_A_DATA_3	MEM_A_DQ<31..24>	11 27
MEM_A_DQ_BYTE4	MEM_45S	MEM_A_DATA_4	MEM_A_DQ<39..32>	11 28
MEM_A_DQ_BYTE5	MEM_45S	MEM_A_DATA_5	MEM_A_DQ<47..40>	11 28
MEM_A_DQ_BYTE6	MEM_45S	MEM_A_DATA_6	MEM_A_DQ<55..48>	11 28
MEM_A_DQ_BYTE7	MEM_45S	MEM_A_DATA_7	MEM_A_DQ<63..56>	11 28
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM_A_DQS_P<0>	11 27
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM_A_DQS_N<0>	11 27
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM_A_DQS_P<1>	11 27
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM_A_DQS_N<1>	11 27
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM_A_DQS_P<2>	11 27
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM_A_DQS_N<2>	11 27
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM_A_DQS_P<3>	11 27
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM_A_DQS_N<3>	11 27
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM_A_DQS_P<4>	11 28
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM_A_DQS_N<4>	11 28
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM_A_DQS_P<5>	11 28
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM_A_DQS_N<5>	11 28
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM_A_DQS_P<6>	11 28
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM_A_DQS_N<6>	11 28
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM_A_DQS_P<7>	11 28
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM_A_DQS_N<7>	11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0>	8 11 29 30 32
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0>	8 11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM_B_CKE<3..0>	11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM_B_CS_L<3..0>	11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM_B_ODT<3..0>	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM_B_A<15..0>	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM_B_BA<2..0>	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM_B_RAS_L	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM_B_CAS_L	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM_B_WE_L	11 29 30 32
MEM_B_DQ_BYTE0	MEM_45S	MEM_B_DATA_0	MEM_B_DQ<7..0>	11 29
MEM_B_DQ_BYTE1	MEM_45S	MEM_B_DATA_1	MEM_B_DQ<15..8>	11 29
MEM_B_DQ_BYTE2	MEM_45S	MEM_B_DATA_2	MEM_B_DQ<23..16>	11 29
MEM_B_DQ_BYTE3	MEM_45S	MEM_B_DATA_3	MEM_B_DQ<31..24>	11 29
MEM_B_DQ_BYTE4	MEM_45S	MEM_B_DATA_4	MEM_B_DQ<39..32>	11 30
MEM_B_DQ_BYTE5	MEM_45S	MEM_B_DATA_5	MEM_B_DQ<47..40>	11 30
MEM_B_DQ_BYTE6	MEM_45S	MEM_B_DATA_6	MEM_B_DQ<55..48>	11 30
MEM_B_DQ_BYTE7	MEM_45S	MEM_B_DATA_7	MEM_B_DQ<63..56>	11 30
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM_B_DQS_P<0>	11 29
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM_B_DQS_N<0>	11 29
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM_B_DQS_P<1>	11 29
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM_B_DQS_N<1>	11 29
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM_B_DQS_P<2>	11 29
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM_B_DQS_N<2>	11 29
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM_B_DQS_P<3>	11 29
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM_B_DQS_N<3>	11 29
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM_B_DQS_P<4>	11 30
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM_B_DQS_N<4>	11 30
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM_B_DQS_P<5>	11 30
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM_B_DQS_N<5>	11 30
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM_B_DQS_P<6>	11 30
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM_B_DQS_N<6>	11 30
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM_B_DQS_P<7>	11 30
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM_B_DQS_N<7>	11 30
		MEM_PWR	PP1V5_S3RS0	6 7
		MEM_PWR	PP1V5_S3	6 7
		MEM_PWR	PP0V75_S3_MEM_VREFCA_A	27 28 31
		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A	27 28 31

SYNC MASTER=J13 CONSTRAINTS SYNC DATE=01/11/2012

PAGE TITLE

Memory Constraints

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

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PAGE 101 OF 109

SHEET 67 OF 73

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ICOMP	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA3_PCH_TX	SATA3_PCH_TX	*	SATA3_TX2TX
SATA3_PCH_RX	SATA3_PCH_RX	*	SATA3_RX2RX
SATA3_PCH_TX	*_PCH_TX	*	SATA3_TX2OTHERTX
SATA3_PCH_RX	*_PCH_RX	*	SATA3_RX2OTHERRX
SATA3_PCH_TX	*_PCH_RX	*	SATA3_TX2RX
SATA3_PCH_RX	*_PCH_TX	*	SATA3_RX2TX
SATA3_PCH_TX	*_TX	*	SATA3_2OTHERHS
SATA3_PCH_RX	*_TX	*	SATA3_2OTHERHS
SATA3_PCH_TX	*_RX	*	SATA3_2OTHERHS
SATA3_PCH_RX	*_RX	*	SATA3_2OTHERHS
SATA3_PCH_TX	*	*	SATA3_2OTHER
SATA3_PCH_RX	*	*	SATA3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
SATA3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
SATA3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
SATA3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA3_TX2TX	*	=2.5x_DIELECTRIC	?
SATA3_RX2RX	*	=2.5x_DIELECTRIC	?
SATA3_TX2OTHERTX	*	=4x_DIELECTRIC	?
SATA3_RX2OTHERRX	*	=4x_DIELECTRIC	?
SATA3_TX2RX	*	=6x_DIELECTRIC	?
SATA3_RX2TX	*	=6x_DIELECTRIC	?
SATA3_2OTHERHS	*	=4x_DIELECTRIC	?
SATA3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x_DIELECTRIC	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_PCH_TX	USB3_PCH_TX	*	USB3_TX2TX
USB3_PCH_RX	USB3_PCH_RX	*	USB3_RX2RX
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2OTHERTX
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2OTHERRX
USB3_PCH_TX	*_PCH_RX	*	USB3_TX2RX
USB3_PCH_RX	*_PCH_TX	*	USB3_RX2TX
USB3_PCH_TX	*_TX	*	USB3_2OTHERHS
USB3_PCH_RX	*_TX	*	USB3_2OTHERHS
USB3_PCH_TX	*_RX	*	USB3_2OTHERHS
USB3_PCH_RX	*_RX	*	USB3_2OTHERHS
USB3_PCH_TX	*	*	USB3_2OTHER
USB3_PCH_RX	*	*	USB3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	*	=2.5x_DIELECTRIC	?
USB3_RX2RX	*	=2.5x_DIELECTRIC	?
USB3_TX2OTHERTX	*	=4x_DIELECTRIC	?
USB3_RX2OTHERRX	*	=4x_DIELECTRIC	?
USB3_TX2RX	*	=6x_DIELECTRIC	?
USB3_RX2TX	*	=6x_DIELECTRIC	?
USB3_2OTHERHS	*	=4x_DIELECTRIC	?
USB3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SATA_PCH_MUX_R2D	SATA_80D	SATA3_PCH_TX	SATA_HDD_R2D_C_P	16 38
SATA_PCH_MUX_R2D	SATA_80D	SATA3_PCH_TX	SATA_HDD_R2D_C_N	16 38
	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_MUX_IN_P	38
	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_MUX_IN_N	38
SATA_MUX_SSD_R2D	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_P	6 38
SATA_MUX_SSD_R2D	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_N	6 38
SATA_PCH_MUX_D2R	SATA_80D	SATA3_PCH_RX	SATA_HDD_D2R_P	16 38
SATA_PCH_MUX_D2R	SATA_80D	SATA3_PCH_RX	SATA_HDD_D2R_N	16 38
	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_MUX_OUT_P	38
	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_MUX_OUT_N	38
SATA_MUX_SSD_D2R	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_P	6 38
SATA_MUX_SSD_D2R	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_N	6 38
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP	16
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_P	18 24
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_N	18 24
USB_BT	USB_80D	USB	USB_BT_P	24 37
USB_BT	USB_80D	USB	USB_BT_N	24 37
	USB_80D	USB	USB_BT_CONN_P	6 37
	USB_80D	USB	USB_BT_CONN_N	6 37
	USB_80D	USB	USB_BT_WAKE_P	37
	USB_80D	USB	USB_BT_WAKE_N	37
USB_TPAD	USB_80D	USB	USB_TPAD_P	49
USB_TPAD	USB_80D	USB	USB_TPAD_N	49
	USB_80D	USB	USB_TPAD_CONN_P	6
	USB_80D	USB	USB_TPAD_CONN_N	6
USB_TPAD_HUB	USB_80D	USB	USB_TPAD_HUB_P	24
USB_TPAD_HUB	USB_80D	USB	USB_TPAD_HUB_N	24
	USB_80D	USB	USB_TPAD_R_P	24 49
	USB_80D	USB	USB_TPAD_R_N	24 49
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_P	49
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_N	49
USB_SDCARD	USB_80D	USB	USB_SDCARD_P	24 33
USB_SDCARD	USB_80D	USB	USB_SDCARD_N	24 33
USB_SMC	USB_80D	USB	USB_SMC_P	24 41
USB_SMC	USB_80D	USB	USB_SMC_N	24 41
USB_CAMERA	USB_80D	USB	USB_CAMERA_P	6 18 40
USB_CAMERA	USB_80D	USB	USB_CAMERA_N	6 18 40
USB_EXTA	USB_80D	USB	USB_EXTA_P	18 39
USB_EXTA	USB_80D	USB	USB_EXTA_N	18 39
	UART_45S	UART	SMC_DEBUGPRT_TX_L	39 41 42
	UART_45S	UART	SMC_DEBUGPRT_RX_L	39 41 42
	USB_80D	USB	USB2_EXTA_MUXED_P	39
	USB_80D	USB	USB2_EXTA_MUXED_N	39
	USB_80D	USB	USB2_EXTA_MUXED_F_P	39
	USB_80D	USB	USB2_EXTA_MUXED_F_N	39
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_RX_P	18 39
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_RX_N	18 39
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_P	18 39
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_N	18 39
	USB_80D	USB3_PCH_RX	USB3_EXTA_RX_F_P	39
	USB_80D	USB3_PCH_RX	USB3_EXTA_RX_F_N	39
	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_F_P	39
	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_F_N	39
	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_C_P	39
	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_C_N	39
USB_EXTB	USB_80D	USB	USB_EXTB_P	6 24 40
USB_EXTB	USB_80D	USB	USB_EXTB_N	6 24 40
	USB_80D	USB	USB_EXTB_EHCI_P	18 24
	USB_80D	USB	USB_EXTB_EHCI_N	18 24
	USB_80D	USB	USB_EXTB_XHCI_P	18 24
	USB_80D	USB	USB_EXTB_XHCI_N	18 24
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_P	18 40
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_N	18 40
	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_RC_P	6 40
	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_RC_N	6 40
	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_CONN_P	
	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_CONN_N	
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_P	18 40
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_N	18 40
	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_C_P	6 40
	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_C_N	6 40
(USB_TPAD_HUB)	USB_80D	USB	USB_EXTD_XHCI_P	18 24
(USB_TPAD_HUB)	USB_80D	USB	USB_EXTD_XHCI_N	18 24
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	18
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_P	16
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_N	16
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_P	16
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_N	16
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_P	16
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_N	16
	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK	16

SATA SSD

USB Hub nets

USB Camera nets

USB EXTA nets (Right USB port)

USB EXTB nets (Left USB port)

Unused USB nets

SYNC MASTER=J13_CONSTRAINTS SYNC DATE=01/11/2012

PAGE TITLE

PCH Constraints 1

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

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BRANCH

PAGE 102 OF 109

SHEET 68 OF 73

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x_DIELECTRIC	?
CLK_LPC	*	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S_R_50S	TOP,BOTTOM	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE		
SMB_45S_R_50S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x_DIELECTRIC	?

XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_ITP	*	=2:1_SPACING	?

DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	*	=3x_DIELECTRIC	?
DP_2OTHERHS	*	=4x_DIELECTRIC	?
DP_2OTHER	*	=3x_DIELECTRIC	?
DP_AUX	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_AUX	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_TX	DP_TX	*	DP_2DP
DP_TX	*_TX	*	DP_2OTHERHS
DP_TX	*_RX	*	DP_2OTHERHS
DP_TX	*	*	DP_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	6 16 41 43
LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L	6 16 41 43
	LPC_45S	LPC	LPCPLUS_RESET_L	6 25 43
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC	25 41
	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC_R	18 25
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 25 43
	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	18 25
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	PCH_CLK33M_PCIIN	16 25
	CLK_LPC_45S	CLK_LPC	PCH_CLK33M_PCIOUT	18 25
SMBUS_PCH_CLK	SMB_45S_R_50S	SMB	SMBUS_PCH_CLK	16 44
SMBUS_PCH_DATA	SMB_45S_R_50S	SMB	SMBUS_PCH_DATA	16 44
SMBUS_PCH_0_CLK	SMB_45S_R_50S	SMB	SML_PCH_0_CLK	16 44
SMBUS_PCH_0_DATA	SMB_45S_R_50S	SMB	SML_PCH_0_DATA	16 44
SMBUS_SMC_1_SO_SCL	SMB_45S_R_50S	SMB	SML_PCH_1_CLK	16 44
SMBUS_SMC_1_SO_SDA	SMB_45S_R_50S	SMB	SML_PCH_1_DATA	16 44
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	6 16 40
	HDA_45S	HDA	HDA_BIT_CLK_R	16
HDA_SYNC	HDA_45S	HDA	HDA_SYNC	6 16 40
	HDA_45S	HDA	HDA_SYNC_R	16
HDA_RST_L	HDA_45S	HDA	HDA_RST_R_L	16
	HDA_45S	HDA	HDA_RST_L	6 16 40
HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0	6 16 40
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	6 16 40
	HDA_45S	HDA	HDA_SDOUT_R	16 25
PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM_CLK32K_SUSCLK_R	17 42
	CLK_SLOW_45S	CLK_SLOW	SMC_CLK32K	41 42
SPI_CLK	SPI_45S	SPI	SPI_CLK_R	16 43
	SPI_45S	SPI	SPI_CLK	43
SPI_MOSI	SPI_45S	SPI	SPI_MOSI_R	16 43
	SPI_45S	SPI	SPI_MOSI	43
SPI_MISO	SPI_45S	SPI	SPI_MISO	16 43
SPI_CS0	SPI_45S	SPI	SPI_CS0_R_L	16 43
	SPI_45S	SPI	SPI_CS0_L	43
	SPI_45S	SPI	SPI_SMC_CLK	41 42
	SPI_45S	SPI	SPI_SMC_MOSI	41 42
	SPI_45S	SPI	SPI_SMC_MISO	41 42
	SPI_45S	SPI	SPI_SMC_CS_L	41 42
	SPI_45S	SPI	SPI_MLB_CLK	42 43 50
	SPI_45S	SPI	SPI_MLB_MOSI	42 43 50
	SPI_45S	SPI	SPI_MLB_MISO	42 43 50
	SPI_45S	SPI	SPI_MLB_CS_L	42 43 50
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_P	6 37
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_N	6 37
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_P	16 37
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_N	16 37
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_P	6 16 37
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_N	6 16 37
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_P	6 16 37
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_N	6 16 37
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_P<3..0>	34
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_N<3..0>	34
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_P<3..0>	8 34
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_N<3..0>	8 34
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_P<3..0>	8 34
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_N<3..0>	8 34
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_P<3..0>	34
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_N<3..0>	34
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_P	16 34
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_N	16 34
	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_P	8 16
	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_N	8 16
XDP_TDI	PCH_45S	PCH_ITP	XDP_PCH_TDI	16 23
XDP_TDO	PCH_45S	PCH_ITP	XDP_PCH_TDO	16 23
XDP_TMS	PCH_45S	PCH_ITP	XDP_PCH_TMS	16 23
XDP_TCK	PCH_45S	PCH_ITP	XDP_PCH_TCK	16 23

Chipset Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_P<3..0>	34
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_N<3..0>	34
	DP_80D	DP_TX	DP_TBTSNK0_ML_C_P<3..0>	8 34
	DP_80D	DP_TX	DP_TBTSNK0_ML_C_N<3..0>	8 34
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_P	34
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_N	34
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_P	8 34
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_N	8 34
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_P<3..0>	34
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_N<3..0>	34
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_P<3..0>	8 34
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_N<3..0>	8 34
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_P	34
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_N	34
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_P	8 34
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_N	8 34

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTC	16 25
SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB	16 25
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB_R	16
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	25 34
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	34
SYSCLK_CLK25M_XTAL	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1	25
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2	25
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R	25

SYNC MASTER=J13 CONSTRAINTS SYNC DATE=01/11/2012

PAGE TITLE: PCH Constraints 2

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DRAWING NUMBER: 051-9277 SIZE: D

REVISION: 2.8.0

BRANCH:

PAGE: 103 OF 109

SHEET: 69 OF 73

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_TX	TBTDP_TX	*	TBTDP_TX2TX
TBTDP_RX	TBTDP_RX	*	TBTDP_RX2RX
TBTDP_TX	TBTDP_RX	*	TBTDP_TX2RX
TBTDP_RX	TBTDP_TX	*	TBTDP_TX2RX
TBTDP_TX	*_TX	*	TBTDP_2OTHERHS
TBTDP_RX	*_TX	*	TBTDP_2OTHERHS
TBTDP_TX	*_RX	*	TBTDP_2OTHERHS
TBTDP_RX	*_RX	*	TBTDP_2OTHERHS
TBTDP_TX	*	*	TBTDP_2OTHER
TBTDP_RX	*	*	TBTDP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_TX2TX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_RX2RX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_TX2RX	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHERHS	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_TX2TX	*	=4x_DIELECTRIC	?
TBTDP_RX2RX	*	=4x_DIELECTRIC	?
TBTDP_TX2RX	*	=6x_DIELECTRIC	?
TBTDP_2OTHERHS	*	=6x_DIELECTRIC	?
TBTDP_2OTHER	*	=4x_DIELECTRIC	?

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_P<1..0>	34 64
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_N<1..0>	34 64
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_P<1..0>	64
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_N<1..0>	64
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_P<1>	34 64
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_N<1>	34 64
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_P<3>	34 64
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_N<3>	34 64
	DP_80D	DP_TX	DP_TBTPA_ML_P<3..1:2>	64
	DP_80D	DP_TX	DP_TBTPA_ML_N<3..1:2>	64
	DP_80D	DP_TX	DP_A_LSX_ML_P<1>	64
	DP_80D	DP_TX	DP_A_LSX_ML_N<1>	64
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_P<1..0>	64
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_N<1..0>	64
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<1>	34 64
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<1>	34 64
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<0>	34 64
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<0>	34 64
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_P	34 64
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_N	34 64
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_P	64
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_N	64
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_P	64
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_N	64
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_P	64
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_N	64
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_P<1..0>	8 34
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_N<1..0>	8 34
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_P<1..0>	
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_N<1..0>	
DP_TBTPB_ML	DP_80D	DP_TX	DP_TBTPB_ML_C_P<3..1:2>	8 34
DP_TBTPB_ML	DP_80D	DP_TX	DP_TBTPB_ML_C_N<3..1:2>	8 34
	DP_80D	DP_TX	DP_TBTPB_ML_P<3..1:2>	
	DP_80D	DP_TX	DP_TBTPB_ML_N<3..1:2>	
	DP_80D	DP_TX	DP_B_LSX_ML_P<1>	
	DP_80D	DP_TX	DP_B_LSX_ML_N<1>	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_P<1..0>	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_N<1..0>	
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_P<1..0>	8 34
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_N<1..0>	8 34
TBT_B_AUXCH	DP_80D	DP_AUX	DP_TBTPB_AUXCH_C_P	8 34
TBT_B_AUXCH	DP_80D	DP_AUX	DP_TBTPB_AUXCH_C_N	8 34
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_P	
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_N	
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_P	
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_N	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_P	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_N	

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DP_80D	DP_TX	DP_TBTSRC_ML_C_P<3..0>	
	DP_80D	DP_TX	DP_TBTSRC_ML_C_N<3..0>	
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_P	
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_N	
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK	34
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI	34
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO	34
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L	34

Only used on hosts supporting Thunderbolt video-in

SYNC MASTER=J13 CONSTRAINTS | SYNC DATE=01/11/2012

PAGE TITLE: Thunderbolt Constraints

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DRAWING NUMBER: 051-9277 | SIZE: D

REVISION: 2.8.0

BRANCH:

PAGE: 105 OF 109

SHEET: 70 OF 73

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_0_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SCL	41 44
SMBUS_SMC_0_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SDA	41 44
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL	41 44
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA	41 44
SMBUS_SMC_2_S3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SCL	41 44
SMBUS_SMC_2_S3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SDA	41 44
SMBUS_SMC_3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SCL	41 44
SMBUS_SMC_3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SDA	41 44
SMBUS_SMC_5_G3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SCL	41 44
SMBUS_SMC_5_G3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SDA	41 44

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSI_P	53
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSI_N	53
	1:1_DIFFPAIR		CHGR_CSI_R_P	53
	1:1_DIFFPAIR		CHGR_CSI_R_N	53
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSO_P	53
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSO_N	53
	1:1_DIFFPAIR		CHGR_CSO_R_P	53
	1:1_DIFFPAIR		CHGR_CSO_R_N	53

SYNC MASTER=J13 CONSTRAINTS SYNC DATE=01/11/2012

PAGE TITLE

SMC Constraints

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DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

BRANCH

PAGE 106 OF 109

SHEET 71 OF 73

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SENSE_1TO1_P2MM	*	=1:1_DIFFPAIR	0.200 MM	0.100 MM	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SPKR_DIFFPAIR	*	=1:1_DIFFPAIR	0.300 MM	0.100 MM	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCIE	*	GND_P2MM
GND	PCIE*	*	GND_P2MM
GND	SATA*	*	GND_P2MM
GND	USB*	*	GND_P2MM
GND	LVDS*	*	GND_P2MM
SB_POWER	CLK_PCIE	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM

J11/J13 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM		INLET_THMSNS_D1_P 46 47
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM		INLET_THMSNS_D1_N 46 47
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM		TBT_THERMD_P 47
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM		TBT_THERMD_N 47
	THERM_1TO1_45S	THERM		TBT_MLBBOT_THMSNS_P 47
	THERM_1TO1_45S	THERM		TBT_MLBBOT_THMSNS_N 47
	THERM_1TO1_45S	THERM		TBTTHMSNS_D2_R_P 47
	THERM_1TO1_45S	THERM		TBTTHMSNS_D2_R_N 47
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE		CPU_THERMD_P 9 47
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE		CPU_THERMD_N 9 47
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE		CPUTHMSNS_D2_P 47
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE		CPUTHMSNS_D2_N 47
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE		CPUVCCIOS0_CS_N 45 59
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE		CPUVCCIOS0_CS_P 45 59
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE		CPUIMVP_ISNS1_P 45 57 58
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE		CPUIMVP_ISNS1_N 45 58
	SENSE_1TO1_45S	SENSE		CPUIMVP_ISUM_R_P 45
	SENSE_1TO1_45S	SENSE		CPUIMVP_ISUM_R_N 45
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE		CPUIMVP_ISNS1G_P 45 58
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE		CPUIMVP_ISNS1G_N 45 58
	SENSE_1TO1_45S	SENSE		CPUIMVP_ISUMG_R_P 45
	SENSE_1TO1_45S	SENSE		CPUIMVP_ISUMG_R_N 45
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE		VCCSAS0_CS_P 45 54
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE		VCCSAS0_CS_N 45 54
	SENSE_1TO1_45S	SENSE		VCCSAISNS_R_P 45
	SENSE_1TO1_45S	SENSE		VCCSAISNS_R_N 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE		ISNS_3V3S0_P 45 61
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE		ISNS_3V3S0_N 45 61
	SENSE_1TO1_45S	SENSE		ISNS_3V3S0_R_P 45
	SENSE_1TO1_45S	SENSE		ISNS_3V3S0_R_N 45
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE		CPUIMVP_ISUMG_P 57 58
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE		CPUIMVP_ISUMG_N 57 58
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE		CPUIMVP_ISUM_P 57 58
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE		CPUIMVP_ISUM_N 57 58
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE		ISNS_HS_COMPUTING_N 8 46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE		ISNS_HS_COMPUTING_P 8 46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE		ISNS_HS_OTHER_N 46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE		ISNS_HS_OTHER_P 46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE		ISNS_1V5_S3_N 46 56
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE		ISNS_1V5_S3_P 46 56
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE		ISNS_AIRPORT_N 37 46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE		ISNS_AIRPORT_P 37 46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE		ISNS_SSD_N 38 46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE		ISNS_SSD_P 38 46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE		ISNS_LCDBKLT_N 8 46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE		ISNS_LCDBKLT_P 8 46
AUD_DIFF	1:1_DIFFPAIR	AUDIO		SPKRAMP_INR_P 6 40 51
AUD_DIFF	1:1_DIFFPAIR	AUDIO		SPKRAMP_INR_N 6 40 51
	1:1_DIFFPAIR	AUDIO		MAX98300_R_P 51
	1:1_DIFFPAIR	AUDIO		MAX98300_R_N 51
SPKR_OUT	SPKR_DIFFPAIR	AUDIO		SPKRAMP_ROUT_P 6 51 52
SPKR_OUT	SPKR_DIFFPAIR	AUDIO		SPKRAMP_ROUT_N 6 51 52
		SB_POWER		PP3V3_S5 6 7
		SB_POWER		PP3V3_S0 6 7
		GND		GND

SYNC MASTER=J13 CONSTRAINTS SYNC DATE=01/11/2012

PAGE TITLE

Project Specific Constraints

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DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

BRANCH

PAGE 108 OF 109

SHEET 72 OF 73

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J11/J13 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	TOP,BOTTOM	Y	=50_OHM_SE	=50_OHM_SE			
DEFAULT	ISL2,ISL11	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL3,ISL10	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL4,ISL9	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	*	N	100 MM	100 MM	10 MM	0 MM	0 MM
STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

Single-ended Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	ISL2,ISL11	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL3,ISL10	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL4,ISL9	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.195 MM	0.195 MM			
35_OHM_SE	ISL2,ISL11	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL3,ISL10	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL4,ISL9	Y	0.125 MM	0.125 MM			
35_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL2,ISL11	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL3,ISL10	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL4,ISL9	Y	0.099 MM	0.099 MM			
40_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.135 MM			
45_OHM_SE	ISL2,ISL11	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL3,ISL10	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL4,ISL9	Y	0.080 MM	0.080 MM			
45_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Differential Pair Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.165 MM		0.130 MM	0.130 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.109 MM	0.109 MM		0.150 MM	0.150 MM
72_OHM_DIFF	ISL3,ISL10	Y	0.109 MM	0.109 MM		0.150 MM	0.150 MM
72_OHM_DIFF	ISL4,ISL9	Y	0.114 MM	0.114 MM		0.150 MM	0.150 MM
72_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	TOP,BOTTOM	Y	0.132 MM	0.132 MM		0.130 MM	0.130 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL3,ISL10	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL4,ISL9	Y	0.088 MM	0.088 MM		0.110 MM	0.110 MM
80_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Spacing Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.100 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.071 MM	?
1x_DIELECTRIC	ISL3,ISL10	0.053 MM	?
1x_DIELECTRIC	ISL4,ISL9	0.050 MM	?
1x_DIELECTRIC	*	0.090 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

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PAGE TITLE

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REVISION 2.8.0

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PAGE 109 OF 109

SHEET 73 OF 73

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