

8

7

6

5

4

3

2

1

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV

ECN

DESCRIPTION OF REVISION

CK APPD  
DATE

6

0001395489

ENGINEERING RELEASED

2012-03-13

SCHEM,MLB,J30

03/12/12

Page

(.cna)

Contents

Sync

1

1

Table of Contents

K901\_MLB

02/15/2011

2

2

System Block Diagram

MASTER

02/15/2011

3

3

Revision History

K20A\_MLB

03/26/2009

4

4

Revision History

K901\_MLB

02/15/2011

5

5

BOM Configuration

K901\_MLB

02/15/2011

6

7

FUNC TEST

K901\_MLB

02/15/2011

7

8

Power Aliases

K901\_MLB

02/15/2011

8

9

Signal Aliases

K901\_MLB

02/15/2011

9

10

CPU DMI/PEG/FDI/RSVD

MASTER

02/15/2011

10

11

CPU CLOCK/MISC/JTAG

MASTER

02/15/2011

11

12

CPU DDR3 INTERFACES

MASTER

02/15/2011

12

13

CPU POWER

MASTER

02/15/2011

13

14

CPU GROUNDS

MASTER

02/15/2011

14

16

CPU DECOUPLING-I

JACK\_J30

09/27/2011

15

17

CPU DECOUPLING-II

MASTER

02/15/2011

16

18

PCH SATA/PCIe/CLK/LPC/SPI

J31\_MLB

06/13/2011

17

19

PCH DMI/FDI/PM/Graphics

J31\_MLB

06/13/2011

18

20

PCH PCI/USB/TP/RSVD

J31\_MLB

06/13/2011

19

21

PCH GPIO/MISC/NCTF

J31\_MLB

06/13/2011

20

22

PCH POWER

J31\_MLB

06/13/2011

21

23

PCH GROUNDS

J31\_MLB

06/13/2011

22

24

PCH DECOUPLING

K901\_MLB

02/15/2011

23

25

CPU & PCH XDP

J31\_MLB

06/13/2011

24

26

Chipset Support

K901\_MLB

02/15/2011

25

27

USB HUB & MUX

LINDA\_J30

09/19/2011

26

28

CPU Memory S3 Support

K901\_MLB

02/15/2011

27

29

DDR3 SO-DIMM Connector A

K901\_MLB

02/15/2011

28

30

DDR3 Byte/Bit Swaps

K901\_MLB

02/15/2011

29

31

DDR3 SO-DIMM Connector B

K901\_MLB

02/15/2011

30

33

SD Card Connector

YONAS\_J30

11/03/2011

31

34

DDR3/FRAMEBUF VREF MARGINING

J31\_MLB

06/13/2011

32

35

X19/ALS/CAMERA CONNECTOR

K901\_MLB

02/15/2011

33

36

T29 Host (1 of 2)

K901\_MLB

02/15/2011

34

37

T29 Host (2 of 2)

K901\_MLB

02/15/2011

35

38

T29 Power Support

K901\_MLB

02/15/2011

36

39

ETHERNET PHY (CAESAR IV)

J31\_MLB

06/15/2011

37

40

Ethernet Connector

K901\_MLB

02/15/2011

38

41

FireWire LLC/PHY (FW643E)

K901\_MLB

02/15/2011

39

42

FireWire Port & PHY Power

K901\_MLB

06/23/2011

40

43

FireWire Connector

K901\_MLB

02/15/2011

41

45

SATA/IR/SIL Connectors

YONAS\_J30

11/08/2011

42

46

External A USB3 Connector

J31\_MLB

07/08/2011

43

47

External B USB3 Connector

J31\_MLB

07/08/2011

44

48

Front Flex Support

K901\_MLB

02/15/2011

45

49

SMC

YONAS\_J30

12/21/2011

Page

(.cna)

Contents

Sync

46

50

SMC Support

YONAS\_J30

01/02/2012

47

51

LPC+SPI Debug Connector

J31\_MLB

06/15/2011

48

52

SMBus Connections

K901\_MLB

02/15/2011

49

53

Power Sensors: Load Side

LINDA\_J30

09/28/2011

50

54

Power Sensors: High Side

YONAS\_J30

11/03/2011

51

55

Thermal Sensors

YONAS\_J30

08/01/2011

52

56

Fan

K901\_MLB

02/15/2011

53

57

WELLSPRING 1

J31\_MLB

07/01/2011

54

58

WELLSPRING 2

JACK\_J30

09/28/2011

55

59

Digital Accelerometer

K901\_MLB

02/15/2011

56

61

SPI ROM

K901\_MLB

02/15/2011

57

62

AUDIO: CODEC/REGULATOR

KAVITHA\_J30

07/25/2011

58

64

AUDIO: DETECT/MIC BIAS

DIRK\_J30

02/16/2012

59

65

AUDIO: HEADPHONE FILTER

KAVITHA\_J30

07/25/2011

60

66

AUDIO: SPEAKER AMP

KAVITHA\_J30

07/25/2011

61

67

AUDIO: JACK

DIRK\_J30

11/10/2011

62

68

AUDIO:Jack Translators

DIRK\_J30

02/20/2012

63

69

DC-In & Battery Connectors

JACK\_J30

07/29/2011

64

70

PBus Supply & Battery Charger

JACK\_J30

09/27/2011

65

71

System Agent Supply

JACK\_J30

09/28/2011

66

72

5V/3.3V SUPPLY

JACK\_J30

08/22/2011

67

73

1.5V DDR3 Supply

JACK\_J30

07/28/2011

68

74

CPU IMVP7 & AXG VCore Regulator

JACK\_J30

08/03/2011

69

75

CPU IMVP7 & AXG VCore Output

JACK\_J30

07/28/2011

70

76

CPUVCCIO (1.05V) Power Supply

JACK\_J30

09/28/2011

71

77

Misc Power Supplies

JACK\_J30

07/28/2011

72

78

Power FETs

K901\_MLB

02/15/2011

73

79

Power Control 1/ENABLE

K901\_MLB

02/15/2011

74

90

LVDS CONNECTOR

K901\_MLB

02/15/2011

75

93

DisplayPort/T29 A MUXing

K901\_MLB

02/15/2011

76

94

Thunderbolt Connector A

K901\_MLB

02/15/2011

77

97

LCD Backlight Driver

J31\_MLB

07/08/2011

78

100

CPU Constraints

K901\_MLB

02/15/2011

79

101

Memory Constraints

K901\_MLB

02/15/2011

80

102

PCH Constraints 1

K901\_MLB

02/15/2011

81

103

PCH Constraints 2

K901\_MLB

02/15/2011

82

104

Ethernet/FW Constraints

K901\_MLB

02/15/2011

83

105

T29 Constraints

K901\_MLB

02/15/2011

84

106

SMC Constraints

K901\_MLB

02/15/2011

85

108

Project Specific Constraints

K901\_MLB

02/15/2011

86

109

PCB Rule Definitions

K901\_MLB

02/15/2011

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9058	1	SCHEM,MLB,J30	SCH	CRITICAL	
820-3115	1	PCBF,MLB,J30	PCB	CRITICAL	

DRAWING

TITLE=MLB

ABBREV=DRAWING

LAST\_MODIFIED=Thu Mar 13 14:00:17 2012

SCHEM,MLB,J30

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:  
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.  
THE POSSESSOR AGREES TO THE FOLLOWING:  
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE  
II NOT TO REPRODUCE OR COPY IT  
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART  
IV ALL RIGHTS RESERVED

DRAWING NUMBER

051-9058

REVISION

6.0.0

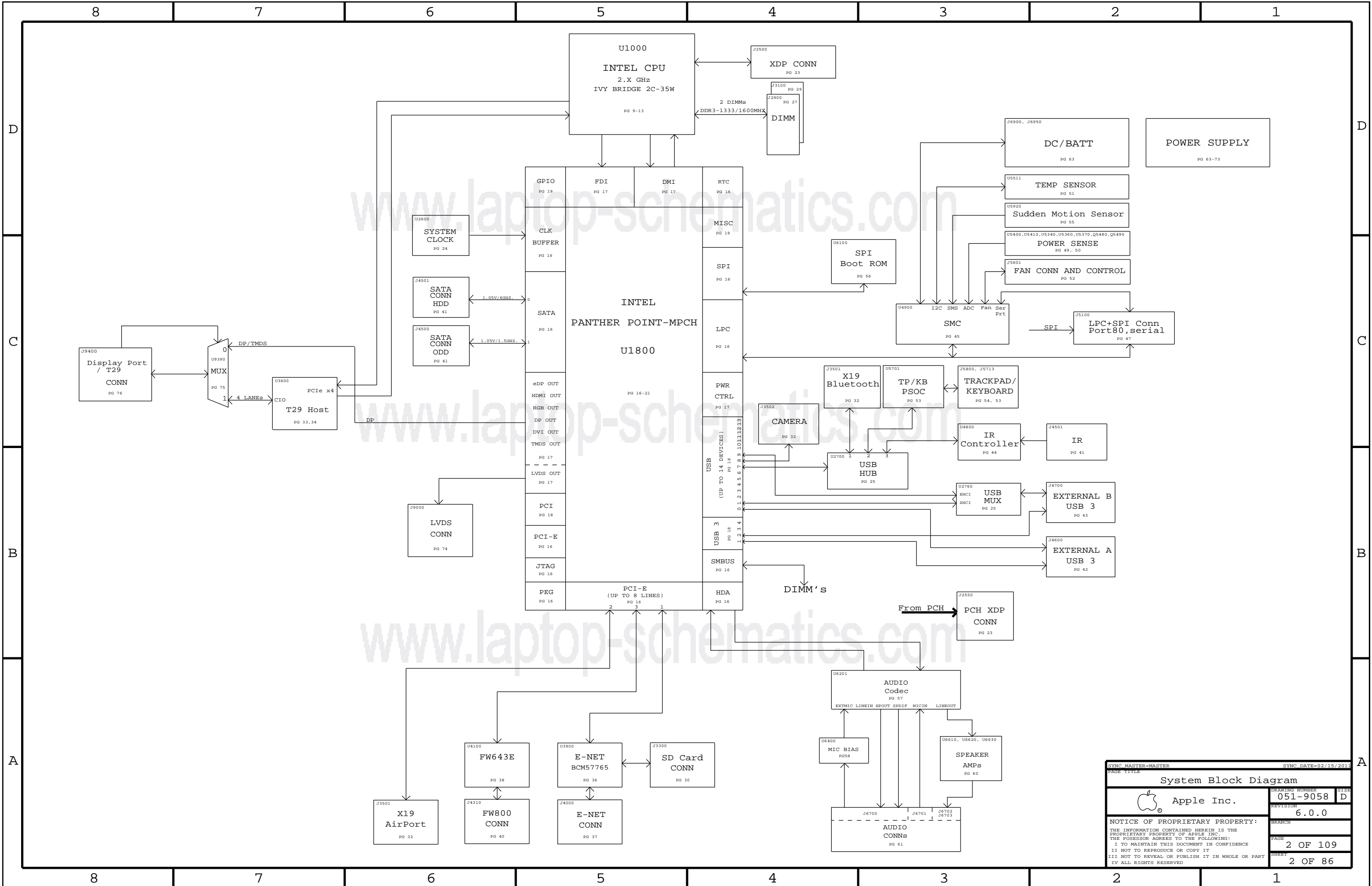
BRANCH

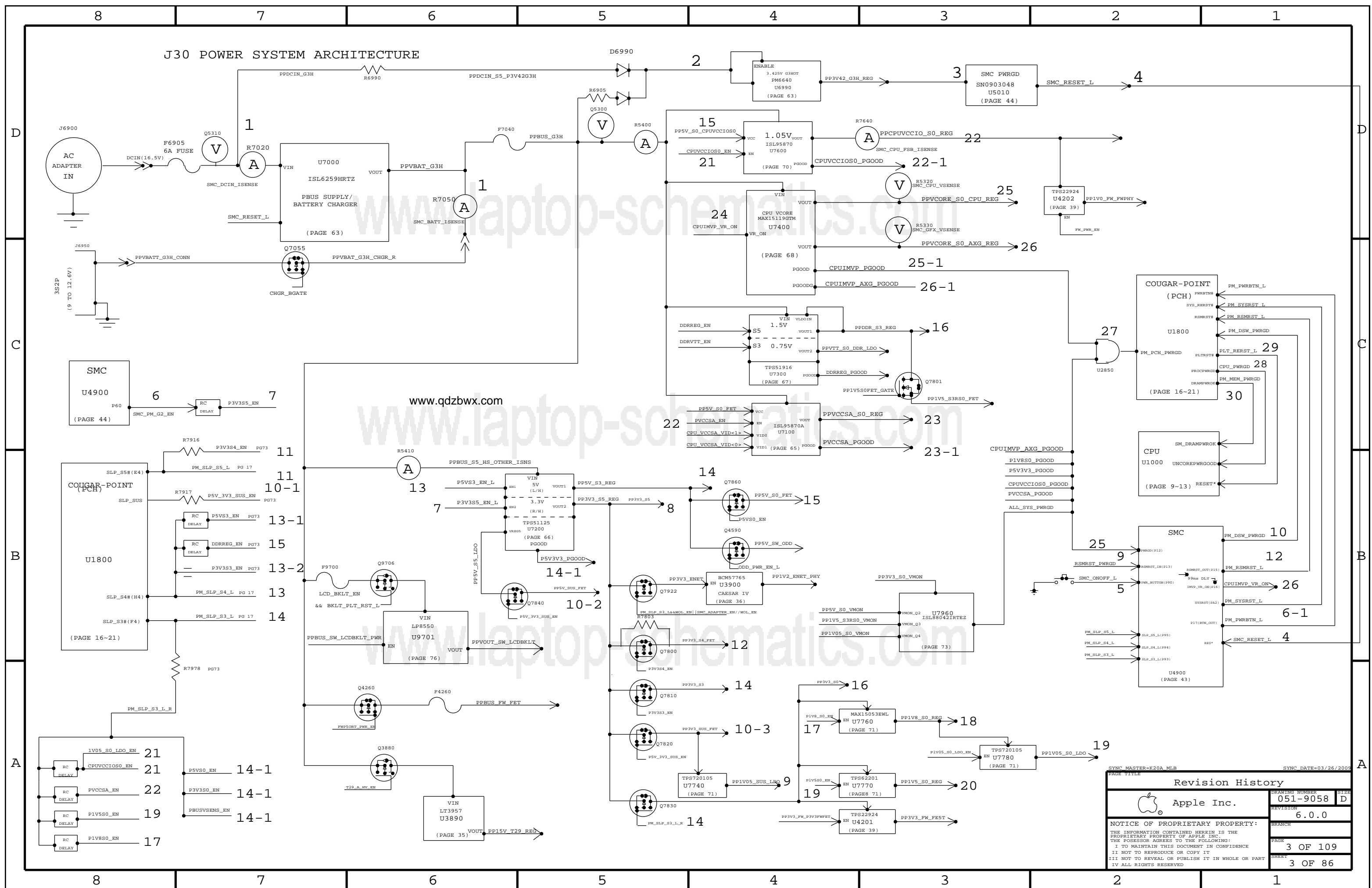
PAGE

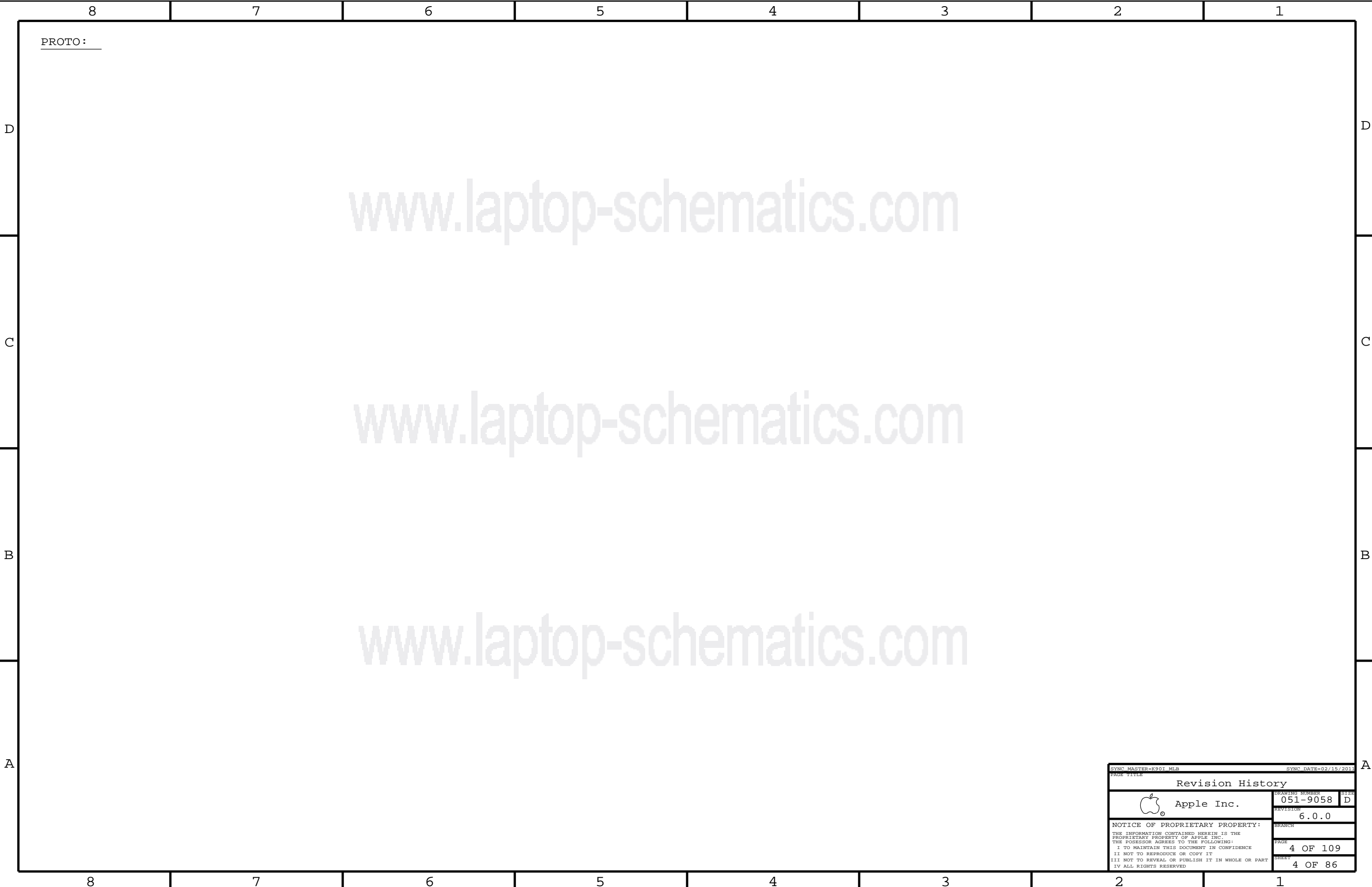
1 OF 109

SHEET


1 OF 86







PROTO:

SYNC MASTER=K901 MLB		SYNC DATE=02/15/2011	
PAGE TITLE			
Revision History			
 Apple Inc.	DRAWING NUMBER	051-9058	SIZE D
	REVISION	6.0.0	
	BRANCH		
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED			
		PAGE	4 OF 109
		SHEET	4 OF 86

## BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
607-8895	CMN PTS,PCBA,MLB,J30	J30_COMMON,FET_PAIR
085-3092	J30 MLB DEVELOPMENT BOM	J30_LEVEL:KNG
607-8721	POWER FETS PAIR,FAIRCHILD,DDR,J30	DDR_POWER_FET:PAIR
607-8722	POWER FETS PAIR,FAIRCHILD,5V_S3,J30	5V_S3_POWER_FET:PAIR
607-8723	POWER FETS PAIR,FAIRCHILD,PBUS_CHARGER,J30	CHARGER_POWER_FET:PAIR
607-9309	POWER FETS PAIR,RENESAS,DDR,J30	DDR_POWER_FET:REN
607-9310	POWER FETS PAIR,RENESAS,5V_S3,J30	5V_S3_POWER_FET:REN
607-9311	POWER FETS PAIR,RENESAS,PBUS_CHARGER,J30	CHARGER_POWER_FET:REN
639-3752	PCBA,MLB,MOL,2.9G,J30	J30_CMNPTS,CPU_2_9GHZ,SODIMM:MOLEX,EEEE_F1YK
639-3756	PCBA,MLB,HYB,2.9G,J30	J30_CMNPTS,CPU_2_9GHZ,SODIMM:HYBRID,EEEE_F1YH
639-3753	PCBA,MLB,FOX,2.5G,J30	J30_CMNPTS,CPU_2_5GHZ,SODIMM:FOXCONN,EEEE_F1YL
639-3755	PCBA,MLB,HYB,2.5G,J30	J30_CMNPTS,CPU_2_5GHZ,SODIMM:HYBRID,EEEE_F1YJ
639-3751	PCBA,MLB,MOL,2.5G,J30	J30_CMNPTS,CPU_2_5GHZ,SODIMM:MOLEX,EEEE_F1YM
639-3754	PCBA,MLB,FOX,2.9G,J30	J30_CMNPTS,CPU_2_9GHZ,SODIMM:FOXCONN,EEEE_F1YG

## J30 BOM GROUPS

BOM GROUP	BOM OPTIONS
J30_COMMON	ALTERNATE,COMMON,J30_COMMON1,J30_COMMON2,J30_DEBUG:ENG,J30_PROGPARTS,T29BST:Y,TBTHV:P15V
J30_COMMON1	BATT_3S,CFUMEM_S0,USBHUB2513B,HUB_3NONREM,T29:YES,SDRV_PD,SDRV12C:MCU,AXG_PHASE1,BTPWR:S4,UV_GLUE_J30
J30_COMMON2	MIKEY,TPAD:E2,RAMCFG_SLOT
J30_PROGPARTS	BOOTROM_PROG,SMC_PROG,TPAD_PROG,ENET_PROG,T29ROM:PROG,T29MCU:PROG
J30_DEVEL:ENG	BKLT:ENG,XDP_CONN,XDP_CPU:BPM,XDP_PCH,LPCLPLUS_CONN:YES,LOADISNS:YES,SDRVREF_DAC,S0FGOOD_ISL
J30_DEVEL:PVT	LPCLPLUS_CONN:YES,XDP_CONN
J30_DEBUG:ENG	DEVEL_BOM,MOJO:YES,XDP,LPCLPLUS_R:YES,VREFDQ:M1_M3,VREFCA:LDO_DAC
J30_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,MOJO:YES,XDP,LPCLPLUS_R:YES,VREFDQ:M1_M3,VREFCA:LDO,USBHUB2514B
J30_DEBUG:PROD	BKLT:PROD,MOJO:YES,XDP,LPCLPLUS_R:YES,LOADISNS:NO,VREFDQ:M1_M3,VREFCA:LDO,USBHUB2513B

## Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4113	1	IC, IVB, 2C, 35W, 1023MSA	U1000	CRITICAL	CPU_IVB_2C
337S4264	1	IVB, S ROND, PRQ, L1, 2, 5, 35W, 2+2, 1, 1, 3M, BGA	U1000	CRITICAL	CPU_2_5GHZ
337S4265	1	IVB, S ROND, PRQ, L1, 2, 9, 35W, 2+2, 1, 25, 4M, BGA	U1000	CRITICAL	CPU_2_9GHZ
337S4269	1	PANTHERPOINT, C1, BLJRC, PRQ, BD82HM77	U1800	CRITICAL	
343S0534	1	IC, BCM57765B0, ENET&D, 8X8	U3900	CRITICAL	
338S0753	1	IC, FW418, 13448 PIV/DMT 1.0M, PCS 4-12	U4100	CRITICAL	
338S1072	1	IC, T29, PRQ, S LJ3Y, FCBGA, 15x15MM, C1	U3600	CRITICAL	T29: YES
353S3055	1	IC, 013VEDP212, X2 DISPLAYPORT 2:1 MIX, QFN	U9390	CRITICAL	
946-3827	1	J30 MIA SYMAX ADDRESSIVE 29993-BC 0.480	UV_GLUE_J30	CRITICAL	UV_GLUE_J30
516S0806	1	CONN, 204P, SODIMM, SOCKET, DDR3, RAM, BGA, FOXCONN	J3100	CRITICAL	SODIMM: FOXCONN
516-0246	1	CONN, 204P, SODIMM, DDR3, P=0.6MM, FOXCONN	J2900	CRITICAL	SODIMM: FOXCONN
516S0805	1	CONN, 204P, SODIMM, SOCKET, DDR3, RAM, BGA, MOLEX	J3100	CRITICAL	SODIMM: MOLEX
516-0245	1	CONN, 204P, SODIMM, DDR3, P=0.6MM, MOLEX	J2900	CRITICAL	SODIMM: MOLEX
516S0805	1	CONN, 204P, SODIMM, SOCKET, DDR3, RAM, BGA, MOLEX	J3100	CRITICAL	SODIMM: HYBRID
516-0246	1	CONN, 204P, SODIMM, DDR3, P=0.6MM, FOXCONN	J2900	CRITICAL	SODIMM: HYBRID

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:FLYG]	CRITICAL	EEEE_FLYG
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:FLYH]	CRITICAL	EEEE_FLYH
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:FLYJ]	CRITICAL	EEEE_FLYJ
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:FLYK]	CRITICAL	EEEE_FLYK
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:FLYL]	CRITICAL	EEEE_FLYL
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:FLYM]	CRITICAL	EEEE_FLYM

## Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
33S0862	1	IC,FLASH,SERIAL,SP1,1MBIT,V27,REV F	U3990	CRITICAL	ENET_BLANK
341S3096	1	IC ENET,11MBITFLAN,CIV REV01,K9x	U3990	CRITICAL	ENET_PROG
33S0550	1	IC,EEPROM,SERIAL,SP1,4Kx8,1.8V,MLP8,LF	U3690	CRITICAL	T29ROM:BLANK
341S3430	1	IC,T29 EEPROM,LR,J30/J31	U3690	CRITICAL	T29ROM:PROG
337S3997	1	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29MCU:BLANK
341S3365	1	IC,PROGMRD,T29,PORT MCU,K901A,K91A,K92A	U9330	CRITICAL	T29MCU:PROG
336S1098	1	IC,SMC12-A3,40MHZ/50MDIPS MCU,9x9,157HGA	U4900	CRITICAL	SMC_BLANK
341S3300	1	IC,SMC,EXTERNAL,FSB,A3,J30	U4900	CRITICAL	SMC_PROG
33S0807	1	IC,SP1 SML 50MHZ FLASH,64MBT,820P,FUSE=1	U6100	CRITICAL	BOOTROM_BLANK
33S08012	1	64 MBIT SP1 SRL DUAL I/O FLASH,801CS	U6100	CRITICAL	BOOTROM_BLANK
341S3558	1	IC,EFI,V00c7,J30/J31	U6100	CRITICAL	BOOTROM_PROG
341S2384	1	IP,ENCORE-LQ, C7063803-LQMC	U4800	CRITICAL	
341S3522	1	IC,PSOC,TP/KB,J30/J31	U5701	CRITICAL	TPAD_PROG


## Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
11880603	11880602		ALL	Murata alt to Samsung
15780958	15780984		ALL	Sella alt to NW Magnetics
12880303	12880353		ALL	Panasonic alt to Sanyo
13880676	13880691		ALL	Murata alt to Samsung
15200778	15200693		ALL	Cyber alt to Vishay
37680855	37681032		ALL	Cincoe alt to Toshiba
37680977	37680859		ALL	Cincoe alt to Toshiba
37680972	37681017		ALL	Kohs alt to Toshiba
37680937	37680845		ALL	Fairchild alt to Renesas
37680777	37680761		ALL	ADM alt to Siliconix
37680957	37680958		ALL	Fairchild alt to Fairchild
37680953	37680958		ALL	Fairchild alt to Renesas
37780107	37780126		ALL	Omron alt to Omron
37180709	37180652		ALL	NSP alt to Infineon
514-0788	514-0761		ALL	Analog Devices alt to Analog
607-8732	607-8722		ALL	Renesas alternate to fairchild
607-9311	607-8723		ALL	Renesas alternate to fairchild

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
15201499	15208064		ALL	Collcraft alt to Murata
15201493	15201300		ALL	Collcraft alt to Murata
13800652	13800648		ALL	Samsung/Murata alt to Taiyo
13800684	13800660		ALL	Murata alt to Taiyo
15201512	15201295		ALL	Cypress alt to SST
15201019	15201271		ALL	Cypress alt to TSM
37601023	37600960		ALL	Siliconix alt to Renesas
35303312	35303055		ALL	MDP alt to Pericom
35303238	35301428		ALL	Intersil alt to TI
35303519	35302179		ALL	Intersil alt to TI
15500578	15500367		ALL	Taiyo alt to Murata
13800601	13800638		ALL	Taiyo alt to Samsung
13800671	13800673		ALL	Taiyo alt to Murata
37600903	37600796		ALL	Fairchild alt to Vishay
37700124	37700057		ALL	Analog alt to TSM
34103492	34103096		ALL	Monolithic alt to Micrel (REVIEW NOW)
37601053	37600604		ALL	Siemens alt to Fairchild
37601076	37600634		ALL	Siemens alt to micrel

## Sub BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-3092	1	J30 MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM
607-8895	1	CMN PTS,PCBA,MLB,J30	CMNPTS	CRITICAL	J30_CMNPTS
607-8721	1	POWER_FETS PAIR,FAIRCHILD,DDR,J30	CSET1	CRITICAL	FET_PAIR
607-8732	1	POWER_FETS PAIR, FAIRCHILD, 5V,S3,J30	CSET2	CRITICAL	FET_PAIR
607-8723	1	POWER_FETS PAIR, FAIRCHILD, P808_CHARGER,J30	CSET3	CRITICAL	FET_PAIR

SYNC MASTER=K901 MLR		SYNC DATE=02/15/2011	
PAGE TITLE			
BOM Configuration			
	Apple Inc.	DRAWING NUMBER	051-9058
		SIZE	D
		REVISION	6.0.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		PAGE	
		5 OF 109	
		SHEET	
		5 OF 86	



# Functional Test Points

D

Fan Connectors		
612	TRUE	PP5V_S0
615	TRUE	FAN_RT_PWM
616	TRUE	FAN_RT_TACH
(NEED TO ADD 1 GND TP)		

MIC_FUNC_TEST		
650	TRUE	BI_MIC_LO
650	TRUE	BI_MIC_HI
650	TRUE	BI_MIC_SHIELD
(NEED TO ADD 1 GND TP)		

SPEAKER_FUNC_TEST		
660	TRUE	SPKRAMP_L_N_OUT
660	TRUE	SPKRAMP_L_P_OUT
660	TRUE	SPKRAMP_R_N_OUT
660	TRUE	SPKRAMP_R_P_OUT
660	TRUE	SPKRAMP_SUB_N_OUT
660	TRUE	SPKRAMP_SUB_P_OUT

LVDS_FUNC_TEST		
620	TRUE	PP3V3_LCDVDD_SW_F (NEED 2 TP)
620	TRUE	PP3V3_S0_LCD_F
620	TRUE	PPVOUT_SW_LCDCLK (NEED 2 TP)
620	TRUE	LVDS_DDC_CLK
620	TRUE	LVDS_DDC_DATA
620	TRUE	LVDS_IG_A_DATA_N<0>
620	TRUE	LVDS_IG_A_DATA_P<0>
620	TRUE	LVDS_IG_A_DATA_N<1>
620	TRUE	LVDS_IG_A_DATA_P<1>
620	TRUE	LVDS_IG_A_DATA_N<2>
620	TRUE	LVDS_IG_A_DATA_P<2>
620	TRUE	LVDS_CONN_A_CLK_F_N
620	TRUE	LVDS_CONN_A_CLK_F_P
620	TRUE	LED_RETURN_1
620	TRUE	LED_RETURN_2
620	TRUE	LED_RETURN_3
620	TRUE	LED_RETURN_4
620	TRUE	LED_RETURN_5
620	TRUE	LED_RETURN_6
(NEED TO ADD 5 GND TP)		

SATA_ODD_CONN		
604	TRUE	PP5V_SW_ODD (NEED 2 TP)
604	TRUE	SMC_ODD_DETECT
604	TRUE	SATA_ODD_D2R_C_P
604	TRUE	SATA_ODD_D2R_C_N
604	TRUE	SATA_ODD_R2D_P
604	TRUE	SATA_ODD_R2D_N
604	TRUE	SMC_SSD_TEMP_CTL_R
604	TRUE	HDD_OOB_TEMP
(NEED TO ADD 3 GND TP)		

SATA_HDD/IR/SIL		
600	TRUE	PP5V_S0_HDD_FLT (NEED 2 TP)
600	TRUE	SATA_HDD_R2D_P
600	TRUE	SATA_HDD_R2D_N
600	TRUE	SATA_HDD_D2R_C_P
600	TRUE	SATA_HDD_D2R_C_N
600	TRUE	SYS_LED_ANODE_R
600	TRUE	IR_RX_OUT
600	TRUE	SMC_SSD_THROTTLE_R
600	TRUE	PP5V_S3_IR_R
(NEED TO ADD 3 GND TP)		

BATT_POWER_CONN		
600	TRUE	SMBUS_SMC_5_G3_SCL
600	TRUE	SMBUS_SMC_5_G3_SDA
600	TRUE	SYS_DETECT_L
600	TRUE	PPVBAT_G3H_CONN (NEED 5 TP)
(NEED TO ADD 5 GND TP)		

BIL_CONN		
600	TRUE	PP3V42_G3H
600	TRUE	SMBUS_SMC_5_G3_SCL
600	TRUE	SMBUS_SMC_5_G3_SDA
600	TRUE	SMC_BIL_BUTTON_L
600	TRUE	SMC_LID_R
(NEED TO ADD 2 GND TP)		

X19_CONN		
600	TRUE	PP3V3_WLAN (NEED 3 TP)
600	TRUE	PCIE_AP_D2R_PI_P
600	TRUE	PCIE_AP_D2R_PI_N
600	TRUE	PCIE_AP_R2D_P
600	TRUE	PCIE_AP_R2D_N
600	TRUE	PCIE_CLK100M_AP_CONN_P
600	TRUE	PCIE_CLK100M_AP_CONN_N
600	TRUE	PP3V3_S3RS4_BT_F
600	TRUE	PCIE_WAKE_L
600	TRUE	USB_BT_CONN_P
600	TRUE	USB_BT_CONN_N
600	TRUE	AP_CLKREQ_Q_L
600	TRUE	AP_RESET_CONN_L
600	TRUE	AP_TEMP_SMB_SDA_R
600	TRUE	AP_TEMP_SMB_SCL_R
600	TRUE	WIFI_EVENT_L_R
(NEED TO ADD 5 GND TP)		

IPD_FLEX_CONN		
600	TRUE	PP3V3_S4
600	TRUE	PP18V5_Z2
600	TRUE	Z2_CS_L
600	TRUE	Z2_DEBUG3
600	TRUE	Z2_MOS1
600	TRUE	Z2_MISO
600	TRUE	Z2_SCLK
600	TRUE	Z2_BOOST_EN
600	TRUE	Z2_HOST_INTN
600	TRUE	Z2_CLKIN
600	TRUE	Z2_KEY_ACT_L
600	TRUE	Z2_RESET
600	TRUE	PSOC_MISO
600	TRUE	PSOC_MOSI
600	TRUE	PSOC_SCLK
600	TRUE	SMBUS_SMC_2_S3_SCL
600	TRUE	SMBUS_SMC_2_S3_SDA
600	TRUE	PSOC_F_CS_L
600	TRUE	PICKB_L
600	TRUE	PP5V_S5_CUMULUS
(NEED TO ADD 2 GND TP)		

KEYBOARD_CONN		
600	TRUE	PP3V3_S4
600	TRUE	PP3V42_G3H
600	TRUE	WS_KBD1
600	TRUE	WS_KBD2
600	TRUE	WS_KBD3
600	TRUE	WS_KBD5
600	TRUE	WS_KBD6
600	TRUE	WS_KBD7
600	TRUE	WS_KBD8
600	TRUE	WS_KBD9
600	TRUE	WS_KBD10
600	TRUE	WS_KBD11
600	TRUE	WS_KBD12
600	TRUE	WS_KBD13
600	TRUE	WS_KBD14
600	TRUE	WS_KBD15_CAP
600	TRUE	WS_KBD16_NUM
600	TRUE	WS_KBD17
600	TRUE	WS_KBD18
600	TRUE	WS_KBD19
600	TRUE	WS_KBD20
600	TRUE	WS_KBD21
600	TRUE	WS_KBD22
600	TRUE	WS_KBD23
600	TRUE	WS_KBD_ONOFF_L
600	TRUE	WS_LEFT_SHIFT_KBD
600	TRUE	WS_LEFT_OPTION_KBD
600	TRUE	WS_CONTROL_KBD
(NEED TO ADD 2 GND TP)		

KBD_BACKLIGHT_CONN		
600	TRUE	KBDLED_ANODE
600	TRUE	SMC_KBDLED_PRESENT_L
(NEED TO ADD 1 GND TP)		

CAMERA/ALS_CONN		
600	TRUE	PP5V_S3_ALSCAMERA_F
600	TRUE	SMBUS_SMC_2_S3_SCL
600	TRUE	SMBUS_SMC_2_S3_SDA
600	TRUE	USB_CAMERA_CONN_P
600	TRUE	USB_CAMERA_CONN_N
(NEED TO ADD 2 GND TP)		

DEBUG_VOLTAGE		
600	TRUE	PPVCORE_S0_CPU
600	TRUE	PPVCORE_S0_AXG
600	TRUE	PP1V2_S3_ENET_INTREG
600	TRUE	PP1V05_S0
600	TRUE	PP1V5_S3RS0
600	TRUE	PP1V8_S0
600	TRUE	PP3V3_S0
600	TRUE	PP5V_S0
600	TRUE	PP3V3_S3
600	TRUE	PP5V_S3
600	TRUE	PPVCCSA_S0_CPU
600	TRUE	PP3V3_S5
600	TRUE	PP3V42_G3H
600	TRUE	PPBUS_G3H
600	TRUE	PP3V3_ENET
600	TRUE	PP3V3_WLAN
600	TRUE	PP5V_SW_ODD
600	TRUE	PP5V_S0_HDD_FLT
600	TRUE	PP18V5_Z2
600	TRUE	PP3V3_S0_LCD_F
600	TRUE	PP3V3_LCDVDD_SW_F
600	TRUE	PP4V5_AUDIO_ANALOG
600	TRUE	PP1V5_S3
600	TRUE	SMC_PM_G2_EN
600	TRUE	PM_SLP_S4_L
600	TRUE	PM_SLP_S3_L
(NEED TO ADD 6 GND TP)		

DC_POWER_CONN		
600	TRUE	PP18V5_DCIN_FUSE
600	TRUE	ADAPTER_SENSE
(NEED TO ADD 4 GND TP)		

LPC+SPI_DEBUG_CONN		
600	TRUE	LEC_AD<0>
600	TRUE	LPC_AD<1>
600	TRUE	LPC_AD<2>
600	TRUE	LPC_AD<3>
600	TRUE	LPC_CLK33M_LPCPLUS
600	TRUE	LPC_FRAME_L
600	TRUE	LPC_PWRDWN_L
600	TRUE	LPC_SERIRO
600	TRUE	LPCPLUS_GPIO
600	TRUE	LPCPLUS_RESET_L
600	TRUE	PM_CLKRUN_L
600	TRUE	PP3V42_G3H
600	TRUE	PP5V_S0
600	TRUE	SMC_RX_L
600	TRUE	SMC_TCK
600	TRUE	SMC_TDI
600	TRUE	SMC_TDO
600	TRUE	SMC_TMS
600	TRUE	SMC_TX_L
600	TRUE	SPI_ALT_CLK
600	TRUE	SPI_ALT_CS_L
600	TRUE	SPI_ALT_MISO
600	TRUE	SPI_ALT_MOSI
600	TRUE	SPIROM_USE_MLB
(NEED TO ADD 2 GND TP)		

NC_NO_TESTS		
17	TP_CRT_IG_BLUE	NC_CRT_IG_BLUE
17	TP_CRT_IG_GREEN	NC_CRT_IG_GREEN
17	TP_CRT_IG_RED	NC_CRT_IG_RED
17	TP_CRT_IG_DDC_CLK	NC_CRT_IG_DDC_CLK
17	TP_CRT_IG_DDC_DATA	NC_CRT_IG_DDC_DATA
17	TP_CRT_IG_HSYNC	NC_CRT_IG_HSYNC
17	TP_CRT_IG_VSYNC	NC_CRT_IG_VSYNC
17	TP_LVDS_IG_CTRL_CLK	NC_LVDS_IG_CTRL_CLK
17	TP_LVDS_IG_CTRL_DATA	NC_LVDS_IG_CTRL_DATA
17	TP_PCH_LVDS_VBG	NC_PCH_LVDS_VBG
16	TP_HDA_SDIN1	NC_HDA_SDIN1
16	TP_HDA_SDIN2	NC_HDA_SDIN2
16	TP_HDA_SDIN3	NC_HDA_SDIN3
18	TP_PCI_PME_L	NC_PCI_PME_L
18	TP_PCI_CLK33M_OUT3	NC_PCI_CLK33M_OUT3

16	TP_CLINK_CLK	NC_CLINK_CLK
16	TP_CLINK_DATA	NC_CLINK_DATA
16	TP_CLINK_RESET_L	NC_CLINK_RESET_L
16	TP_PCIE_CLK100M_PEBN	NC_PCIE_CLK100M_PEBN
16	TP_PCIE_CLK100M_PEBP	NC_PCIE_CLK100M_PEBP
38	TP_FW643_SDA	NC_FW643_SDA
38	TP_FW643_SM	NC_FW643_SM
38	TP_FW643_TCK	NC_FW643_TCK
38	TP_FW643_TMS	NC_FW643_TMS
38	TP_FW643_FW620_L	NC_FW643_FW620_L
38	TP_FW643_VBUE	NC_FW643_VBUE
38	TP_FW643_OCR10_CTL	NC_FW643_OCR10_CTL
38	TP_FW643_AVREG	NC_FW643_AVREG
38	TP_FW643_TDI	NC_FW643_TDI
23	TP_XDP_PCH_OBSFN_A<0..1>	NC_TP_XDP_PCH_OBSFN_A<0..1>
23	TP_XDP_PCH_OBSFN_B<0..1>	NC_TP_XDP_PCH_OBSFN_B<0..1>
23	TP_XDP_PCH_HOOK2	NC_TP_XDP_PCH_HOOK2
23	TP_XDP_PCH_HOOK3	NC_TP_XDP_PCH_HOOK3
23	TP_XDP_PCH_OBSFN_D<0..1>	NC_TP_XDP_PCH_OBSFN_D<0..1>
23	TP_XDP_PCH_HOOK4	NC_TP_XDP_PCH_HOOK4
23	TP_XDP_PCH_HOOK5	NC_TP_XDP_PCH_HOOK5

16	TP_PCH_GPIO64_CLKOUTFLEX0	NC_PCH_GPIO64_CLKOUTFLEX0
16	TP_PCH_GPIO65_CLKOUTFLEX1	NC_PCH_GPIO65_CLKOUTFLEX1
16	TP_PCH_GPIO66_CLKOUTFLEX2	NC_PCH_GPIO66_CLKOUTFLEX2
16	TP_PCH_GPIO67_CLKOUTFLEX3	NC_PCH_GPIO67_CLKOUTFLEX3

NC_NO_TESTS		
600	TRUE	NC_FW2_TBPB
600	TRUE	NC_FW2_TBPB
600	TRUE	NC_FW2_TBPBIAS
600	TRUE	NC_FW2_TPAP
600	TRUE	NC_FW2_TPAN
600	TRUE	NC_FW0_TBPB
600	TRUE	NC_FW0_TBPB
600	TRUE	NC_FW0_TPAP

600	TRUE	XDP_PCH_AP_PWR_EN
600	TRUE	XDP_PCH_USB_HUB_SOFT_RST_L
600	TRUE	XDP_PCH_SDCONN_STATE_RST_L
600	TRUE	XDP_PCH_ENET_PWR_EN
600	TRUE	XDP_PCH_SDCONN_DET_L
600	TRUE	XDP_PCH_PWRBTN_L
600	TRUE	XDP_PCH_S5_PWRGD
600	TRUE	XDP_PCH_ISOLATE_CPU_MEM_L
600	TRUE	XDP_FW_CLKREQ_L
600	TRUE	XDP_AP_CLKREQ_L
600	TRUE	XDP_PCH_AUD_IPHS_SWITCH_EN

17	TP_SDVO_TVCLKINN	NC_SDVO_TVCLKINN
17	TP_SDVO_TVCLKINP	NC_SDVO_TVCLKINP
17	TP_SDVO_STALLN	NC_SDVO_STALLN
17	TP_SDVO_STALLP	NC_SDVO_STALLP
17	TP_SDVO_INTN	NC_SDVO_INTN
17	TP_SDVO_INTP	NC_SDVO_INTP

NC_EDP_TXP<0..3>	TRUE	TP_EDP_TX_P<0..3>
NC_EDP_TXN<0..3>	TRUE	TP_EDP_TX_N<0..3>
NC_EDP_AUXP	TRUE	TP_EDP_AUX_P
NC_EDP_AUXN	TRUE	TP_EDP_AUX_N
NC_CPU_THERMDA	TRUE	TP_CPU_THERMDA
NC_CPU_THERMDC	TRUE	TP_CPU_THERMDC
NC_CPU_RSVD<30..45>	TRUE	TP_CPU_RSVD<30..45>
NC_CPU_RSVD<8..27>	TRUE	TP_CPU_RSVD<8..27>

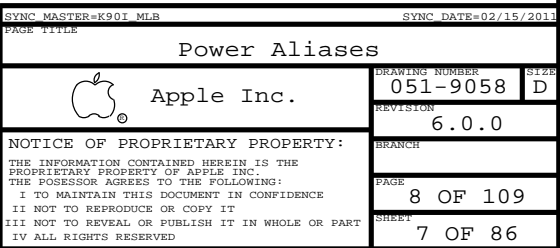
NC_PEG_R2D_CP<0..7>	TRUE	=PEG_R2D_C_P<0..7>
NC_PEG_R2D_CN<0..7>	TRUE	=PEG_R2D_C_N<0..7>
NC_PEG_D2RP<0..7>	TRUE	=PEG_D2R_P<0..7>
NC_PEG_D2RN<0..7>	TRUE	=PEG_D2R_N<0..7>
NC_PEG_R2D_CP<8..11>	TRUE	=PEG_R2D_C_P<8..11>
NC_PEG_R2D_CN<8..11>	TRUE	=PEG_R2D_C_N<8..11>
NC_PEG_D2RP<8..11>	TRUE	=PEG_D2R_P<8..11>
NC_PEG_D2RN<8..11>	TRUE	=PEG_D2R_N<8..11>

16	TP_PCIE_CLK100M_PEA4N	NC_PCIE_CLK100M_PEA4N
16	TP_PCIE_CLK100M_PEA4P	NC_PCIE_CLK100M_PEA4P
16	TP_PCIE_CLK100M_PEA5N	NC_PCIE_CLK100M_PEA5N
16	TP_PCIE_CLK100M_PEA5P	NC_PCIE_CLK100M_PEA5P
16	TP_PCIE_CLK100M_PEB6N	NC_PCIE_CLK100M_PEB6N
16	TP_PCIE_CLK100M_PEB6P	NC_PCIE_CLK100M_PEB6P
16	TP_PCIE_CLK100M_PEB7N	NC_PCIE_CLK100M_PEB7N
16	TP_PCIE_CLK100M_PEB7P	NC_PCIE_CLK100M_PEB7P
53	TP_PSOC_P1_3	NC_PSOC_P1_3
16	TP_SATA_C_D2RN	NC_SATA_C_D2RN
16	TP_SATA_C_D2RP	NC_SATA_C_D2RP
16	TP_SATA_C_R2D_CN	NC_SATA_C_R2D_CN
16	TP_SATA_C_R2D_CP	NC_SATA_C_R2D_CP
16	TP_SATA_D_D2RN	NC_SATA_D_D2RN
16	TP_SATA_D_D2RP	NC_SATA_D_D2RP
16	TP_SATA_D_R2D_CN	NC_SATA_D_R2D_CN
16	TP_SATA_D_R2D_CP	NC_SATA_D_R2D_CP
16	TP_SATA_E_D2RN	NC_SATA_E_D2RN
16	TP_SATA_E_D2RP	NC_SATA_E_D2RP
16	TP_SATA_E_R2D_CN	NC_SATA_E_R2D_CN
16	TP_SATA_E_R2D_CP	NC_SATA_E_R2D_CP
16	TP_SATA_F_D2RN	NC_SATA_F_D2RN
16	TP_SATA_F_D2RP	NC_SATA_F_D2RP
16	TP_SATA_F_R2D_CN	NC_SATA_F_R2D_CN
16	TP_SATA_F_R2D_CP	NC_SATA_F_R2D_CP

33	TP_TBT_MONDC0	NC_TBT_MONDC0
33	TP_TBT_MONDC1	NC_TBT_MONDC1
33	TP_TBT_MONOBSP	NC_TBT_MONOBSP
33	TP_TBT_MONOBSN	NC_TBT_MONOBSN
33	TP_DP_T29SRC_ML_CP<0..3>	NC_DP_T29SRC_ML_CP<0..3>
33	TP_DP_T29SRC_ML_CN<0..3>	NC_DP_T29SRC_ML_CN<0..3>
33	TP_DP_T29SRC_AUXCH_CP	NC_DP_T29SRC_AUXCH_CP
33	TP_DP_T29SRC_AUXCH_CN	NC_DP_T29SRC_AUXCH_CN
33	TP_T29_PCIE_RESET0_L	NC_TP_T29_PCIE_RESET0_L
33	TP_T29_PCIE_RESET1_L	NC_TP_T29_PCIE_RESET1_L
33	TP_T29_PCIE_RESET2_L	NC_TP_T29_PCIE_RESET2_L
33	TP_T29_PCIE_RESET3_L	NC_TP_T29_PCIE_RESET3_L

600	TRUE	PCH_VSS_NCTF<1>
600	TRUE	PCH_VSS_NCTF<2>
600	TRUE	PCH_VSS_NCTF<5>
600	TRUE	PCH_VSS_NCTF<9>
600	TRUE	PCH_VSS_NCTF<11>
600	TRUE	PCH_VSS_NCTF<12>
600	TRUE	PCH_VSS_NCTF<15>
600	TRUE	PCH_VSS_NCTF<17>
600	TRUE	PCH_VSS_NCTF<19>
600	TRUE	PCH_VSS_NCTF<19>
600	TRUE	PCH_VSS_NCTF<21>
600	TRUE	PCH_VSS_NCTF<25>
600	TRUE	PCH_VSS_NCTF<27>
600	TRUE	PCH_VSS_NCTF<29>

8	TP_LVDS_IG_B_CLKN	NC_LVDS_IG_B_CLKN</
---	-------------------	---------------------







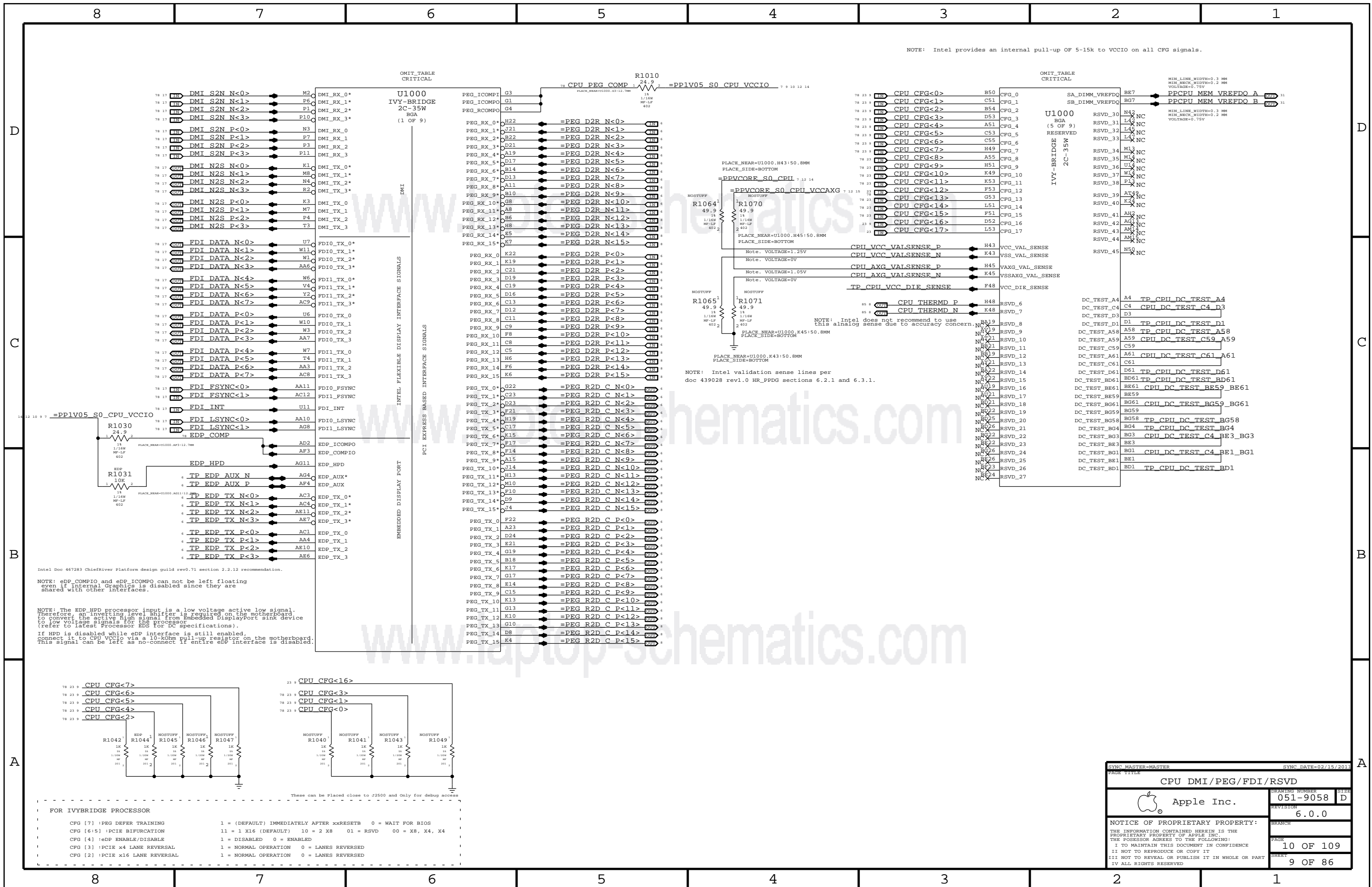




Diagram illustrating the CPU DDR3 Interfaces, showing memory channels (A, B, C, D) and various memory modules (MEM A, MEM B) connected to the CPU. The diagram is divided into four main sections: 8, 7, 6, 5, 4, 3, 2, 1.

**Memory Channel A:**

- MEM A DO<0> to MEM A DO<63>
- MEM A BA<0> to MEM A BA<2>
- MEM A CAS L
- MEM A RAS L
- MEM A WE L

**Memory Channel B:**

- MEM B DO<0> to MEM B DO<63>
- MEM B BA<0> to MEM B BA<2>
- MEM B CAS L
- MEM B RAS L
- MEM B WE L

**Memory Channel C:**

- MEM C DO<0> to MEM C DO<63>
- MEM C BA<0> to MEM C BA<2>
- MEM C CAS L
- MEM C RAS L
- MEM C WE L

**Memory Channel D:**

- MEM D DO<0> to MEM D DO<63>
- MEM D BA<0> to MEM D BA<2>
- MEM D CAS L
- MEM D RAS L
- MEM D WE L

**Memory Modules:**

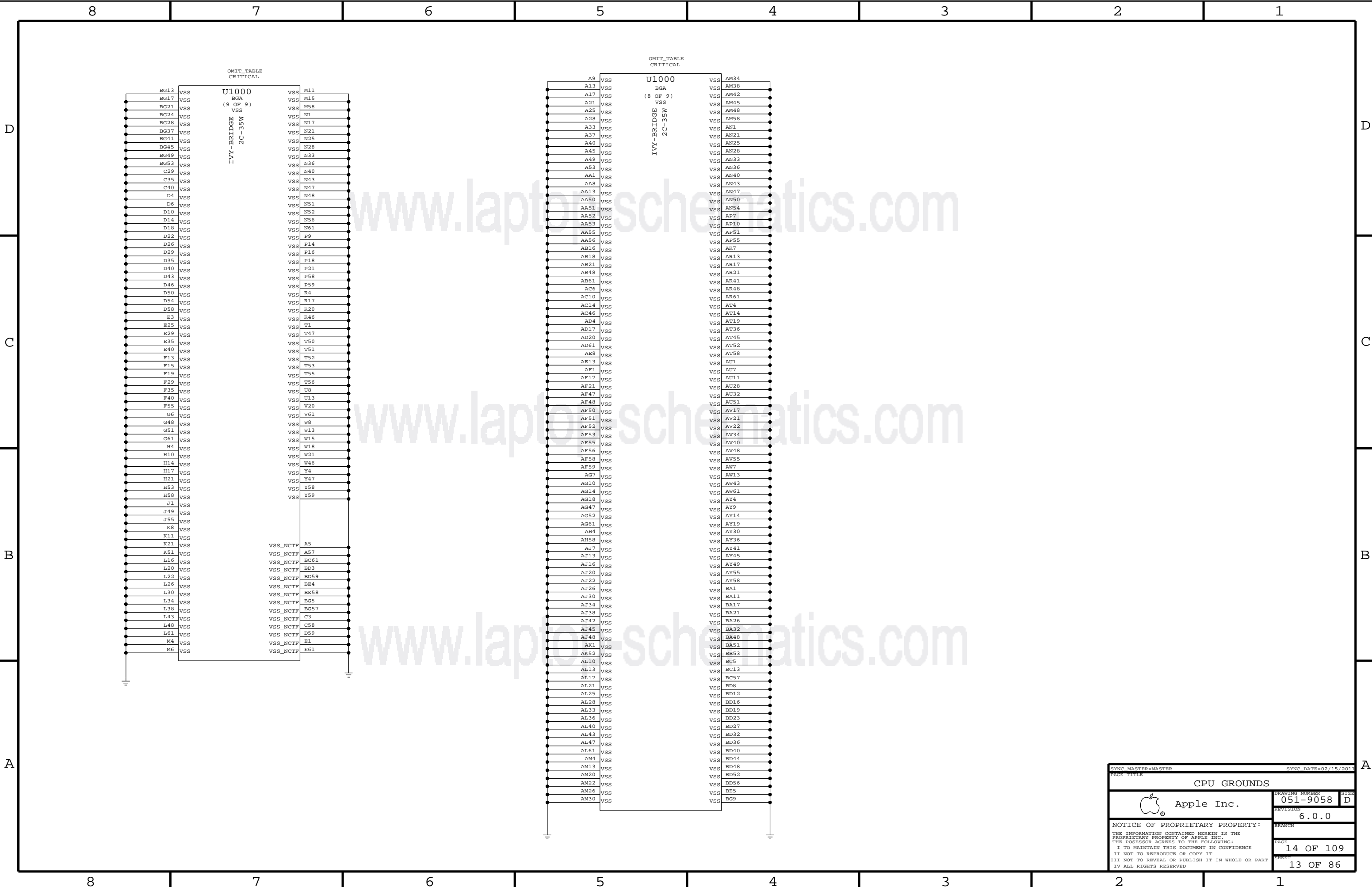
- MEM A DO<0> to MEM A DO<63>
- MEM B DO<0> to MEM B DO<63>
- MEM C DO<0> to MEM C DO<63>
- MEM D DO<0> to MEM D DO<63>

**Memory Channels:**

- MEM A DO<0> to MEM A DO<63>
- MEM B DO<0> to MEM B DO<63>
- MEM C DO<0> to MEM C DO<63>
- MEM D DO<0> to MEM D DO<63>

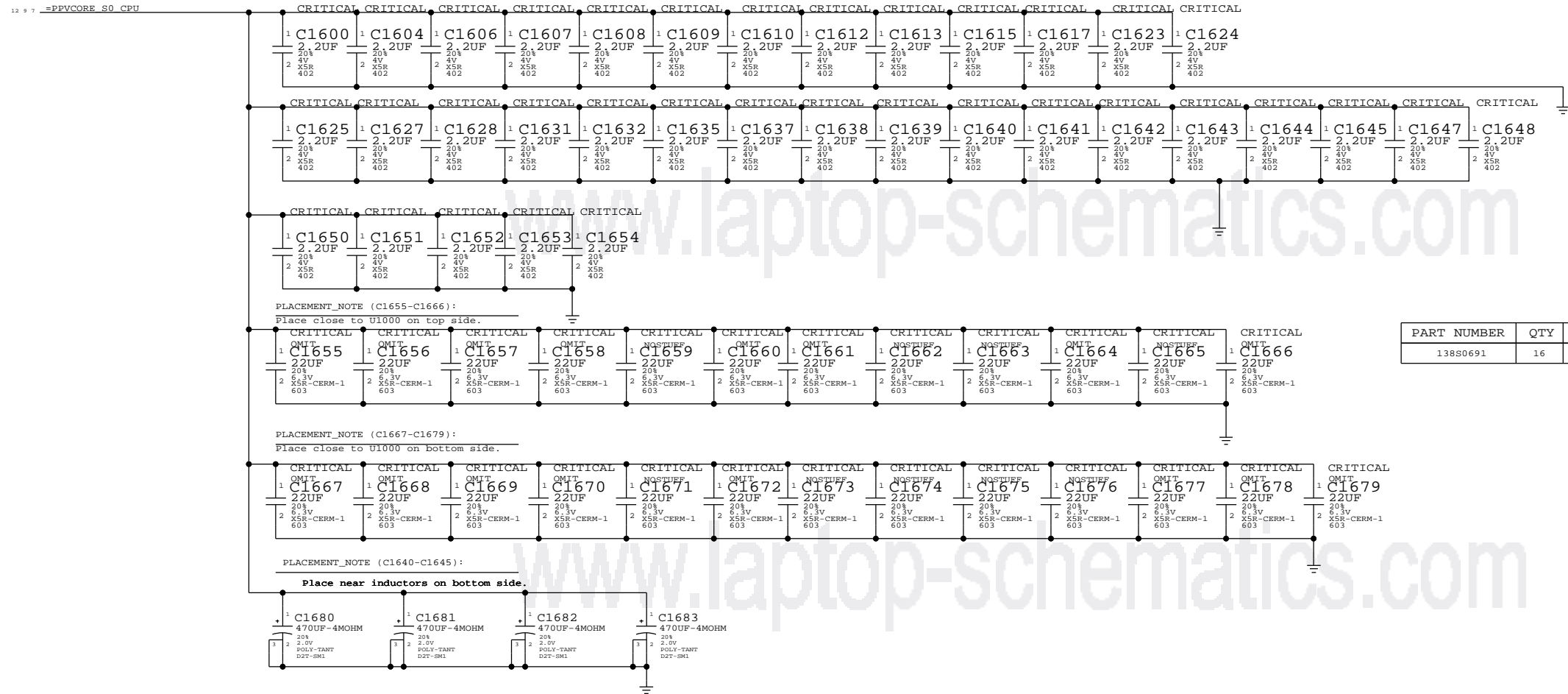






## CPU VCORE DECOUPLING

Intel recommendation (Section 6.2): 35x 2.2uF, 25x 22uF, 4x 470uF



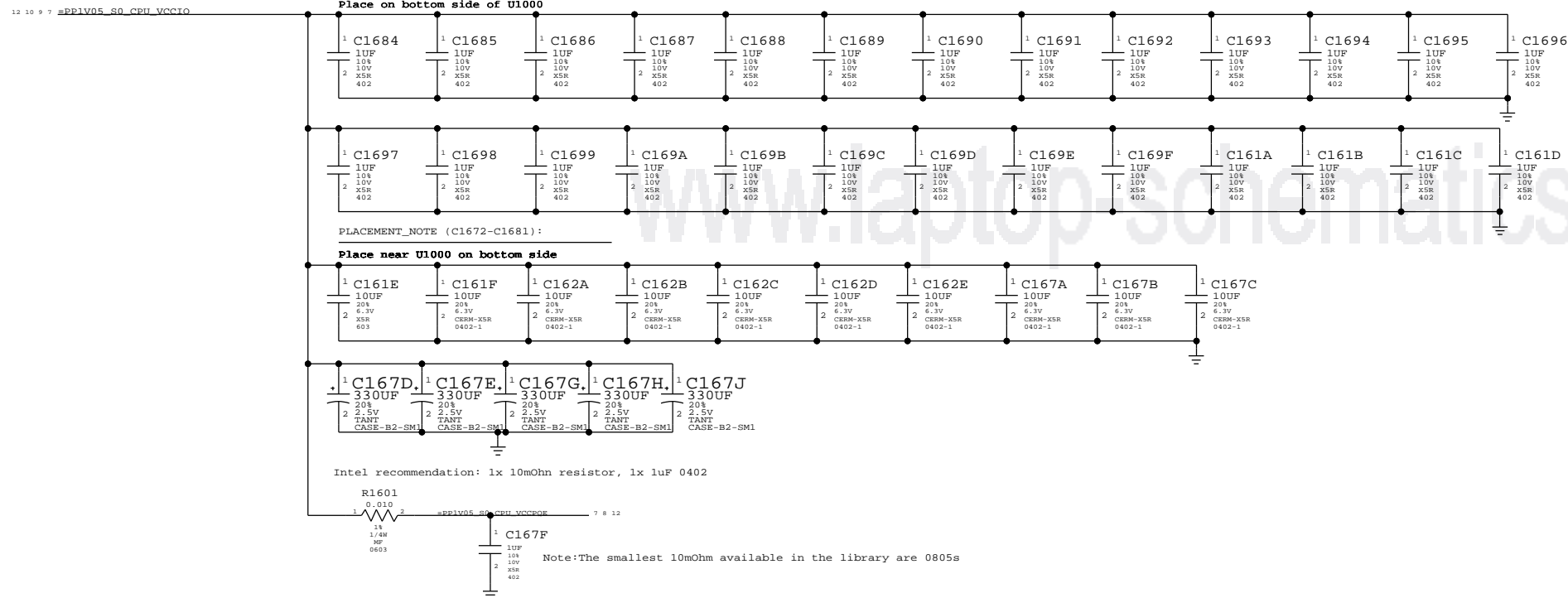
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0691	16	CAP, CER, XSR, 22uF, 20%, 6.3V, 0603, SAMSUNG		CRITICAL	

## CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Section 6.5): 26x 1uF, 10x 10uF, 2x 330uF

PLACEMENT\_NOTE (C1684-C167F):

Place on bottom side of U1000

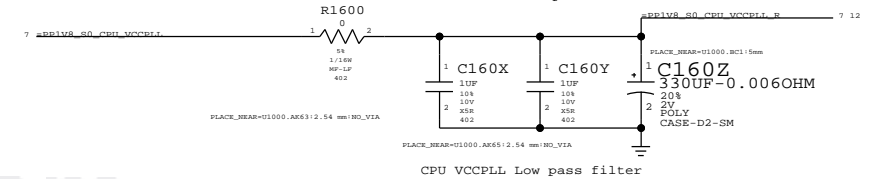



## CPU VCCPLL DECOUPLING

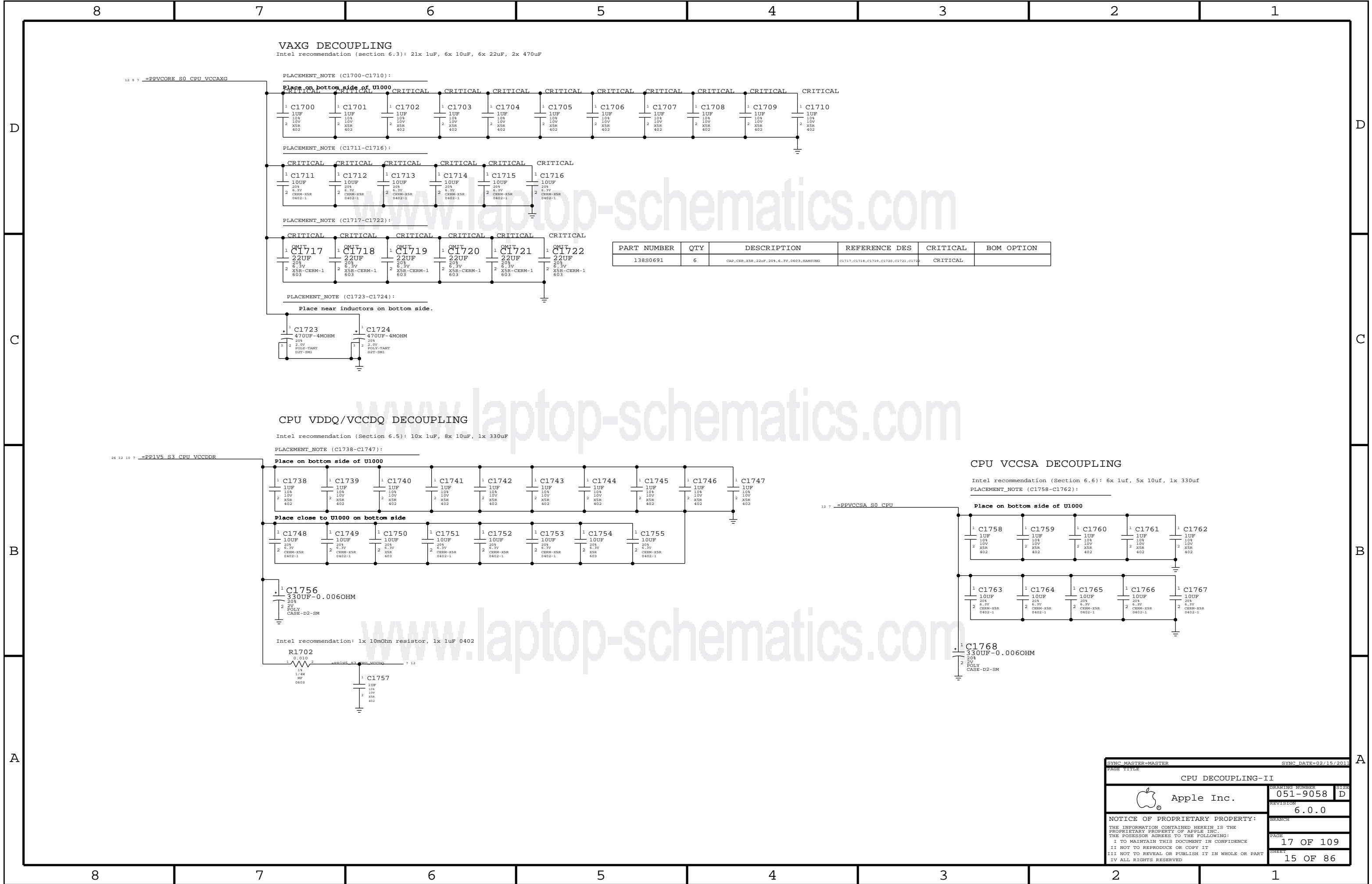
Intel recommendation (section 6.4): 2x 1uF, 1x 330uF

PLACEMENT\_NOTE (C1646-C1671):

Place near U1000 on top side

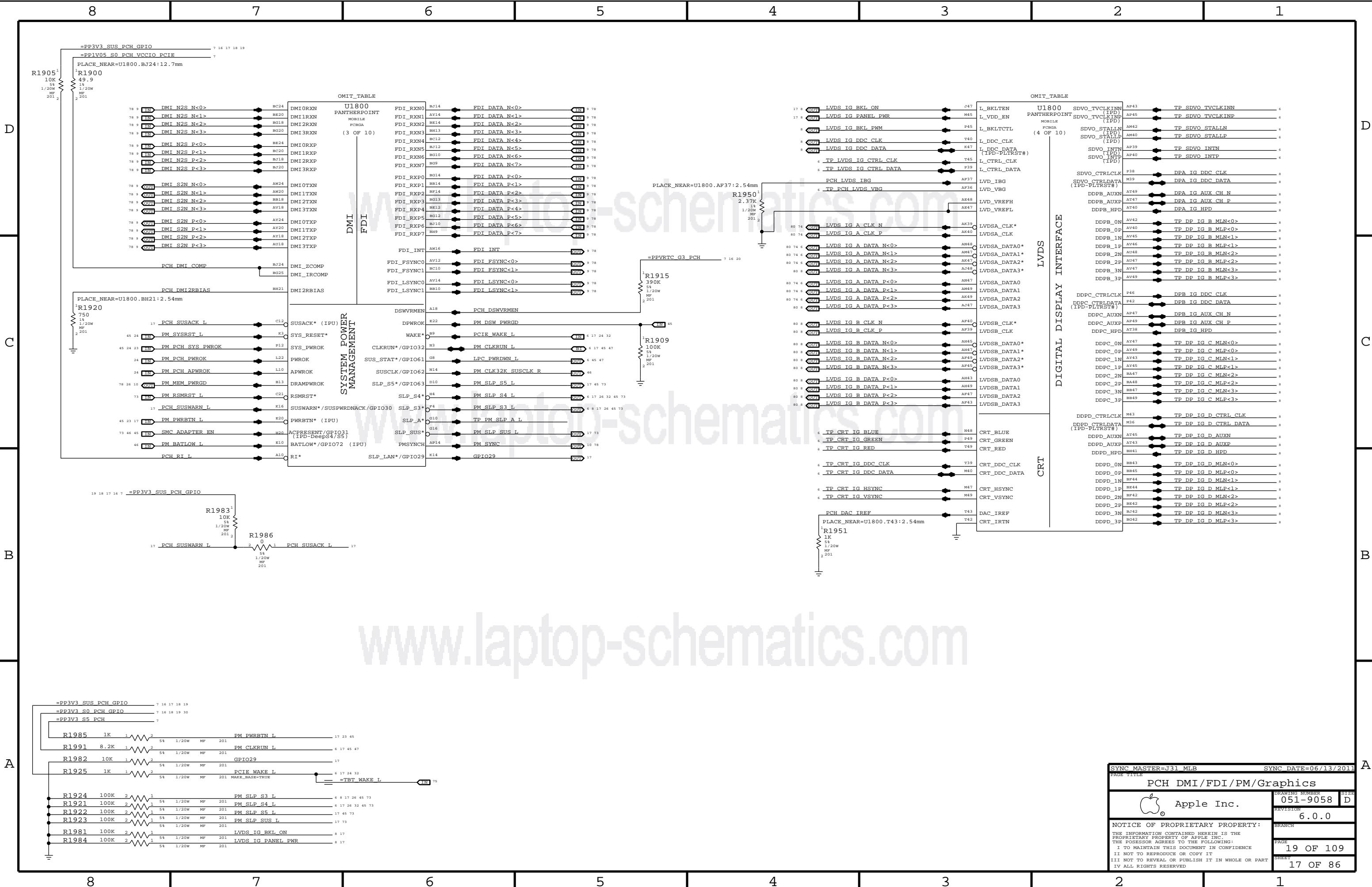


SYNCH MASTER=JACK J30		SYNCH DATE=09/27/2011	
PAGE TITLE			
CPU DECOUPLING-I			
	Apple Inc.	DRAWING NUMBER	051-9058
		SIZE	D
		REVISION	6.0.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE			
PROPERTY OF APPLE INC.			
THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		16 OF 109	
I NOT TO REPRODUCE OR COPY IT			
I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		SHEET	
I V ALL RIGHTS RESERVED		14 OF 86	







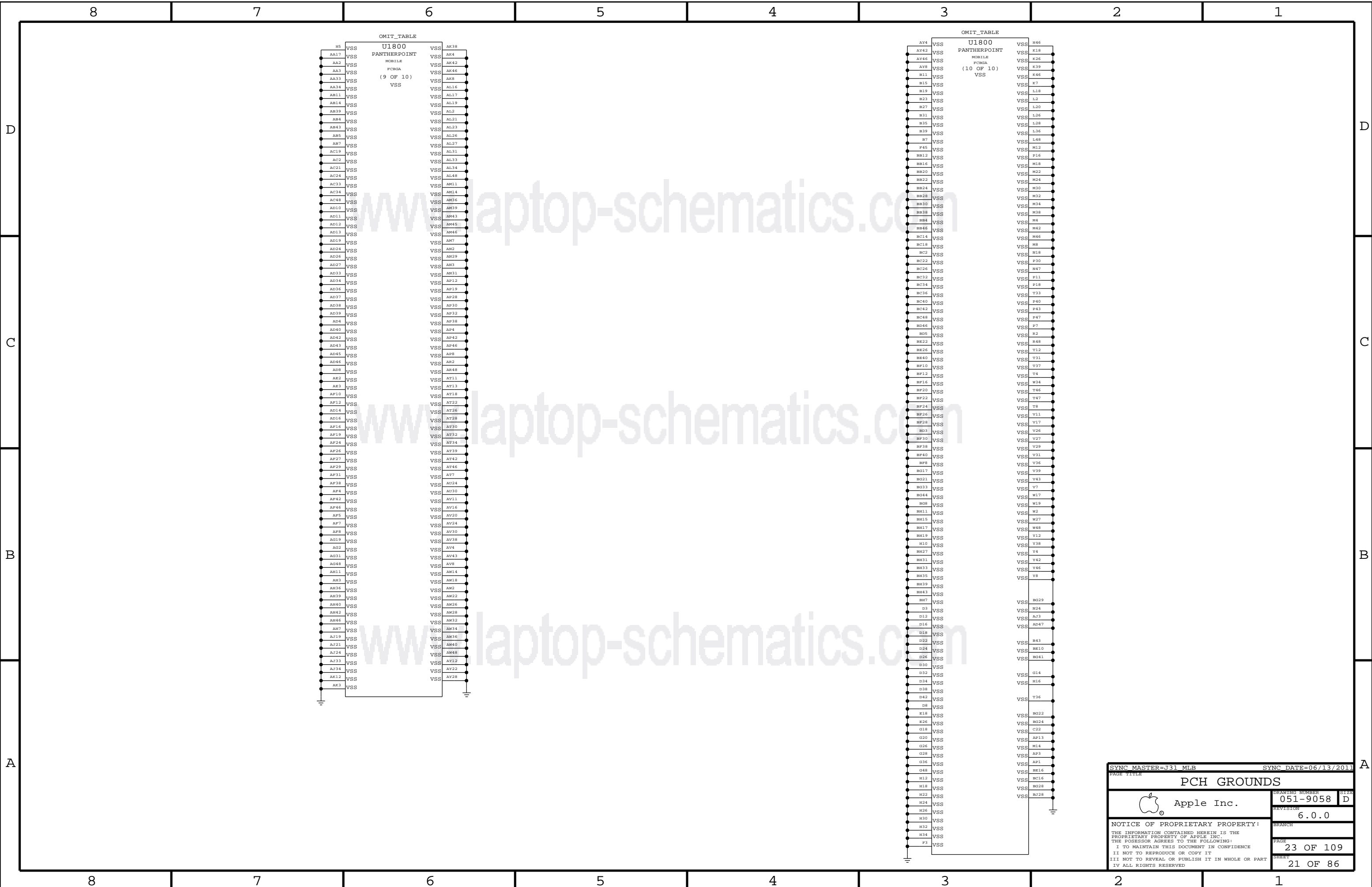


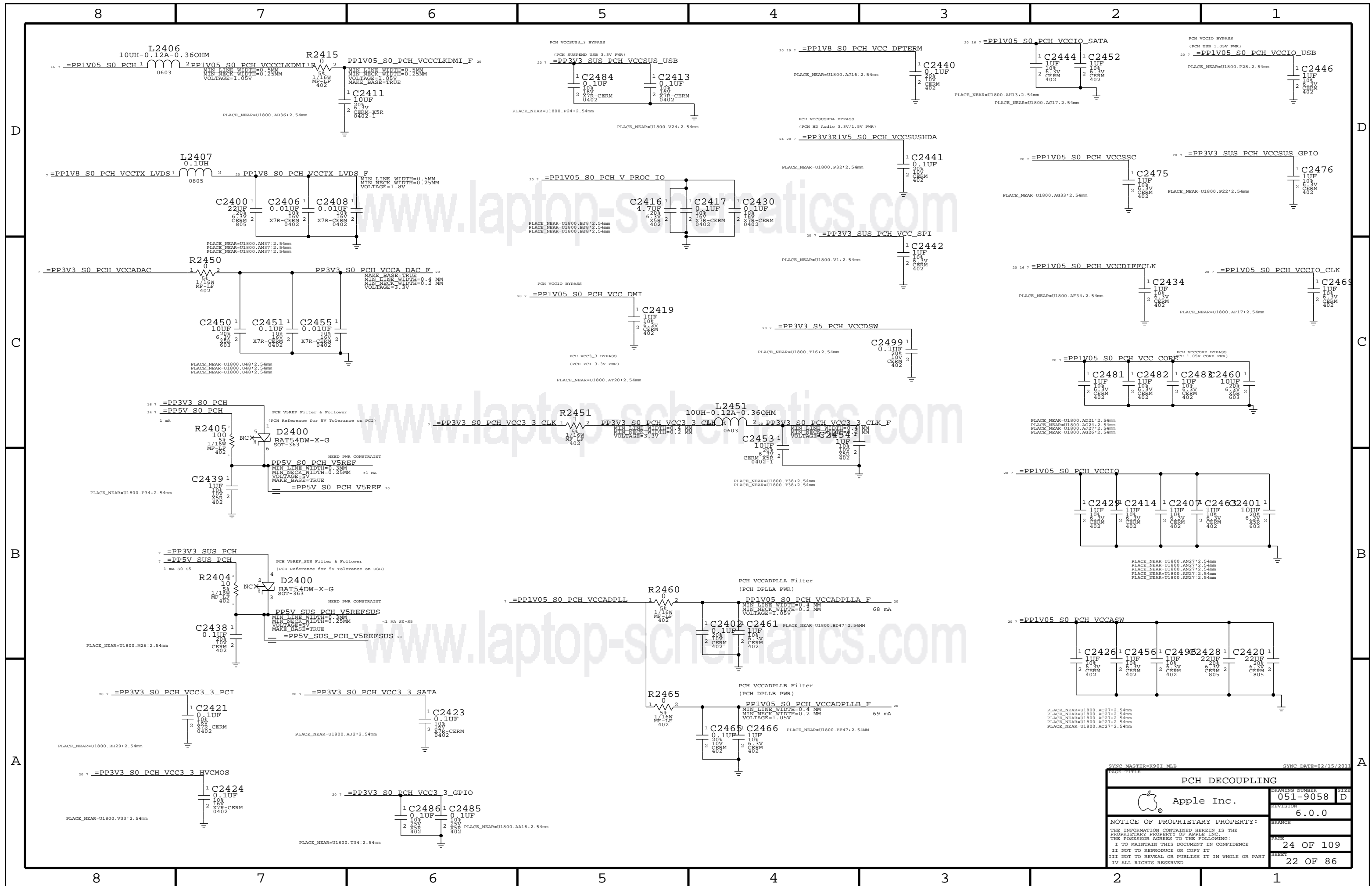




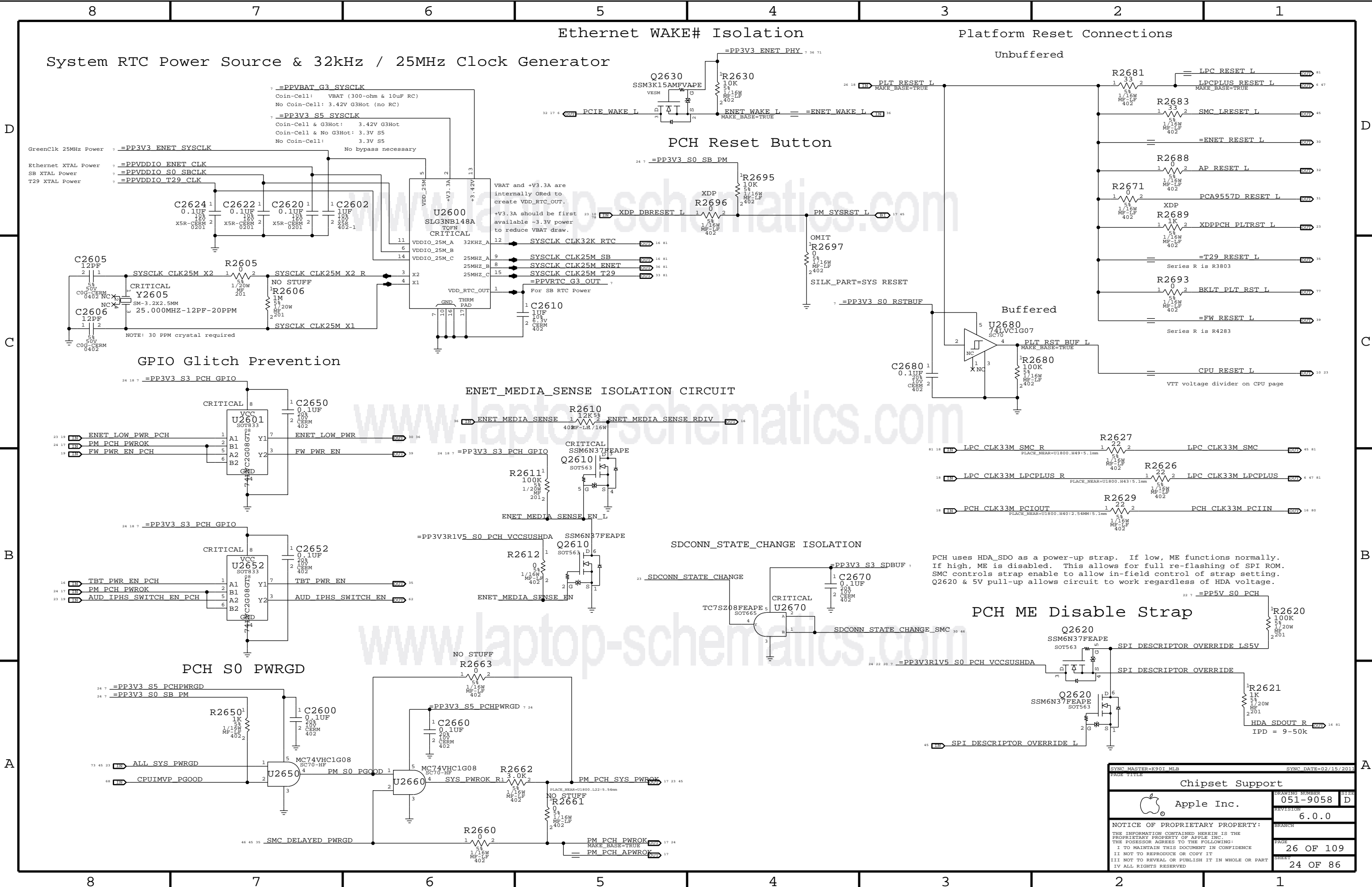












Ethernet WAKE# Isolation

Platform Reset Connections

System RTC Power Source & 32kHz / 25MHz Clock Generator

Unbuffered

PCH Reset Button

Buffered

ENET\_MEDIA\_SENSE ISOLATION CIRCUIT

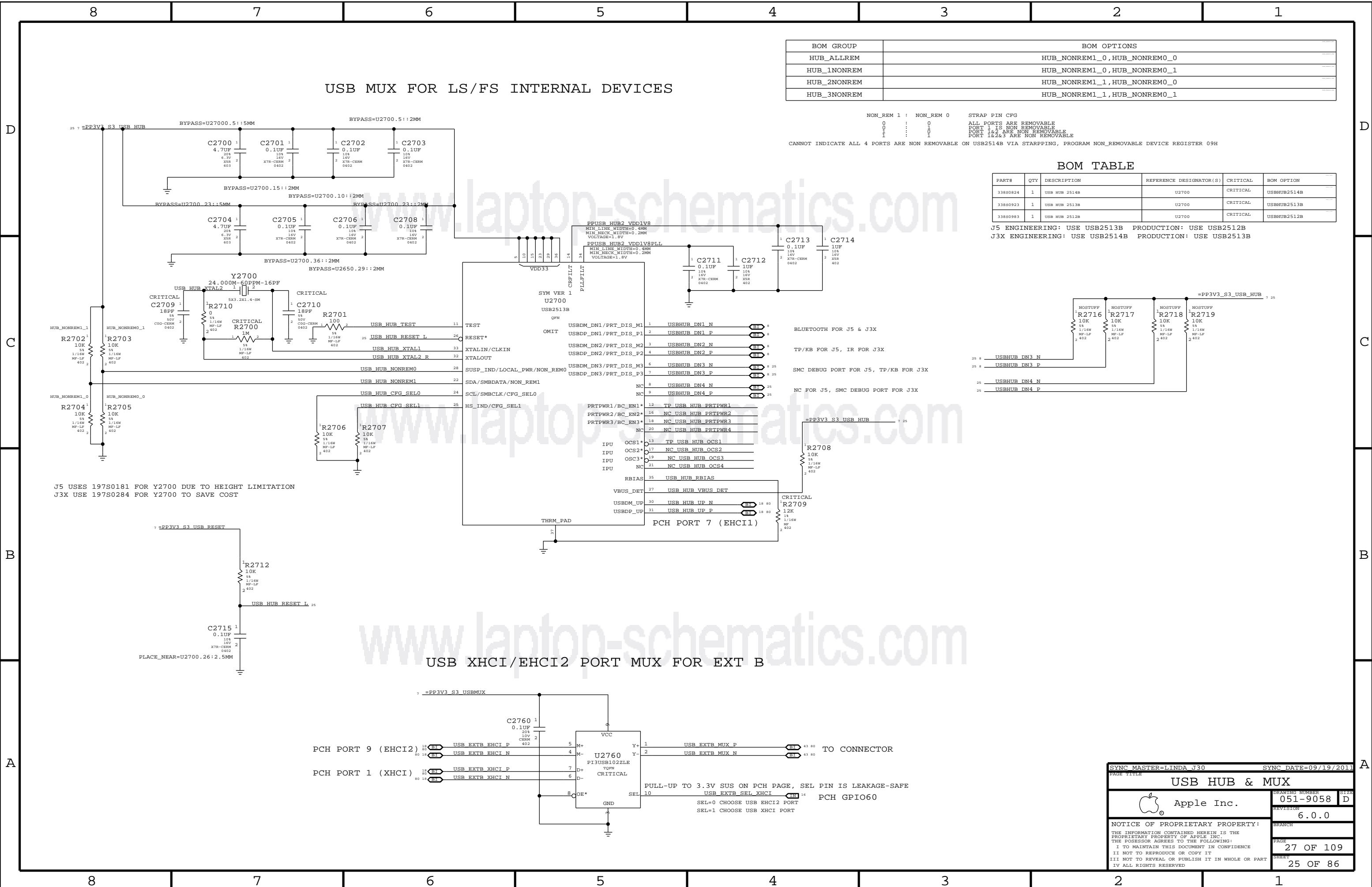
SDCONN\_STATE\_CHANGE ISOLATION

PCH ME Disable Strap

PCH uses HDA\_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of HDA voltage. Q2620 & 5V pull-up allows circuit to work regardless of HDA voltage.

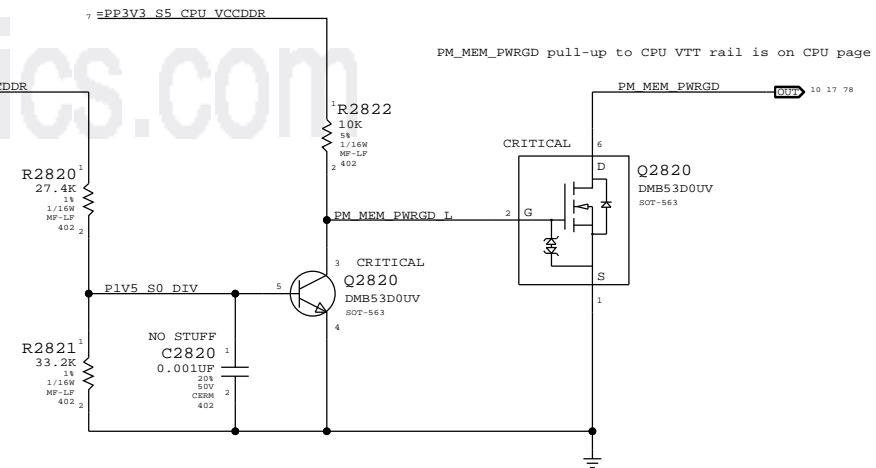
PAGE TITLE		PAGE NUMBER	
Chipset Support		051-9058	
Apple Inc.		6.0.0	
NOTICE OF PROPRIETARY PROPERTY:		26 OF 109	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:		24 OF 86	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			



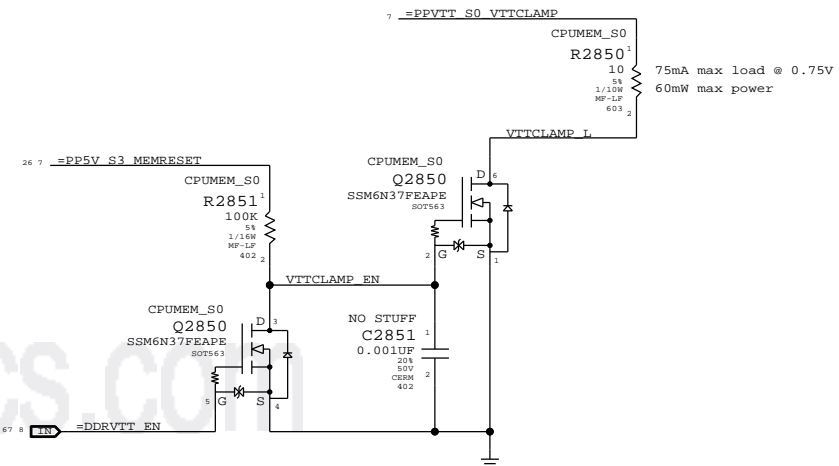


WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM\_RESET\_L isolated.


```
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L
```

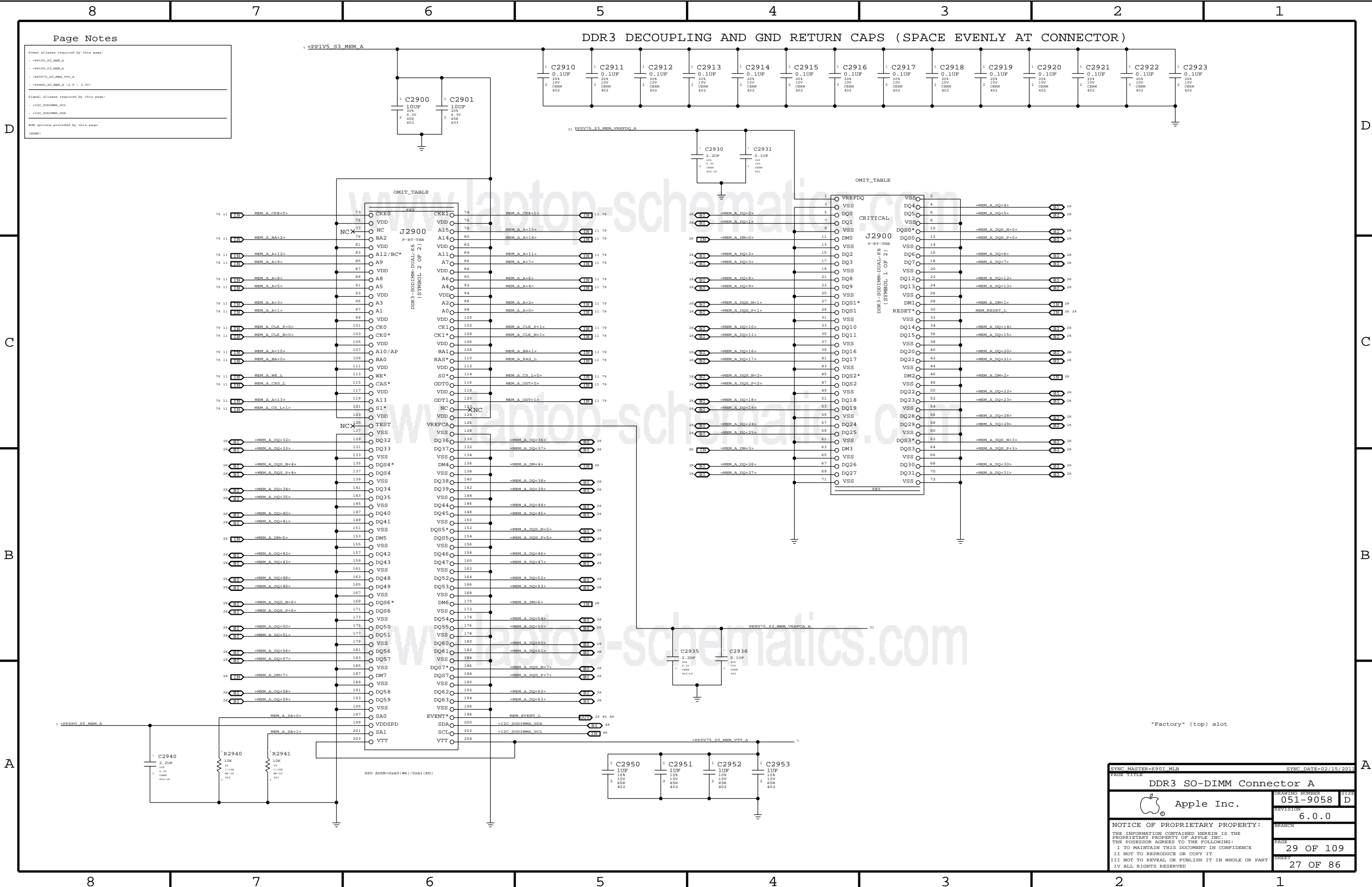


Ensures CKE signals are held low in S3



(\*) CPU\_MEM\_RESET\_L asserts due to loss of PM\_MEM\_PWRGD, must wait for software to clear before deasserting ISOLATE\_CPU\_MEM\_L GPIO.

SYNC MASTER#K90I MLB		SYNC DATE=02/15/2011	
PAGE 111111			
CPU Memory S3 Support			
	Apple Inc.	DRAWING NUMBER	SIZE
		051-9058	D
		REVISION	
		6.0.0	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE			
PROPERTY OF APPLE INC.			
THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		28 OF 109	
I NOT TO REPRODUCE OR COPY IT			
I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		SHEET	
I ALL RIGHTS RESERVED		26 OF 86	



Page Notes

Power aliases required by this page:

- PPIV5\_S3\_MEM\_A
- PPIV5\_S3\_MEM\_B
- PPIV5\_S3\_MEM\_VTT\_A
- PPIV5\_S3\_MEM\_VTT\_B
- PPIV5\_S3\_MEM\_A (2.5 - 3.3V)

Signal aliases required by this page:

- I2C\_S0D1MMA\_SCL
- I2C\_S0D1MMA\_SDA


DOM options provided by this page:

(None)

SYNC MASTER=K901 MLB

SYNC DATE=02/15/2011

DDR3 SO-DIMM Connector A

 Apple Inc.

DRAWING NUMBER  
051-9058

REVISION  
6.0.0

NOTICE OF PROPRIETARY PROPERTY:  
THE INFORMATION CONTAINED HEREIN IS THE  
PROPRIETARY PROPERTY OF APPLE INC.  
THE POSSESSOR AGREES TO THE FOLLOWING:  
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE  
II NOT TO REPRODUCE OR COPY IT  
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART  
IV ALL RIGHTS RESERVED

BRANCH

PAGE  
29 OF 109

SHEET  
27 OF 86

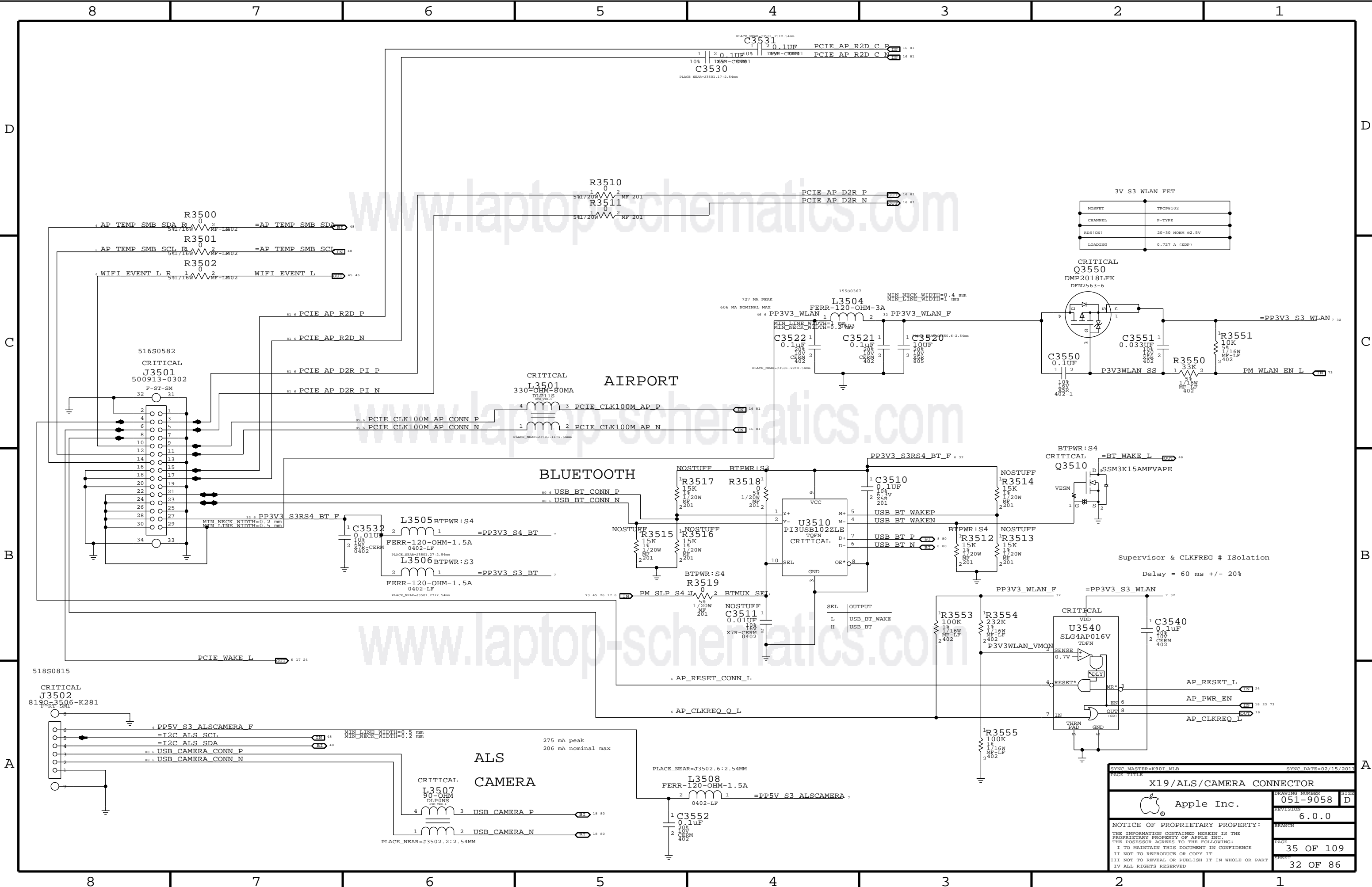
[illegible]






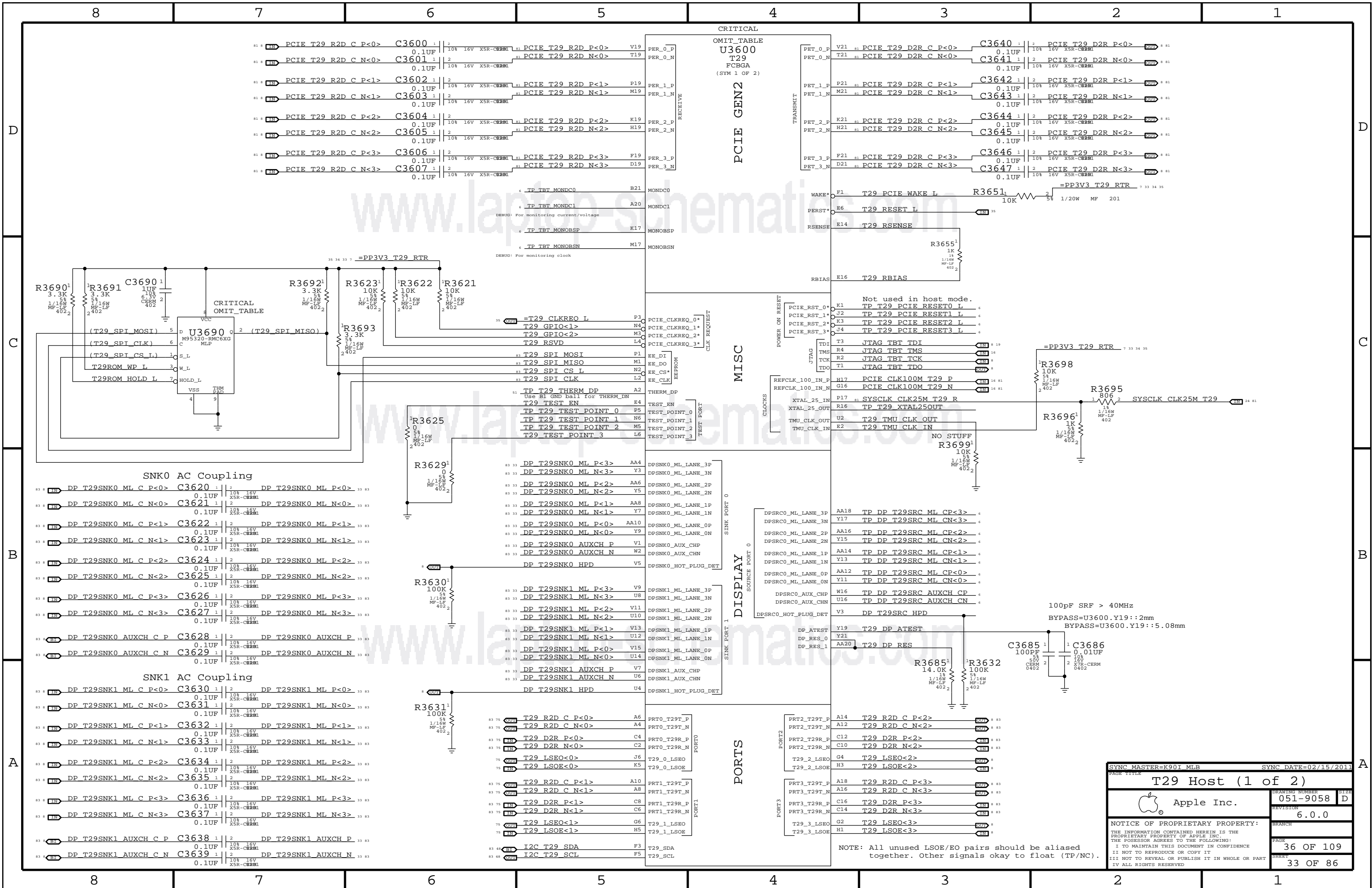






SYNC MASTER=K901 MLB		SYNC DATE=02/15/2013	
PAGE TITLE			
X19/ALS/CAMERA CONNECTOR			
 Apple Inc.		DRAWING NUMBER	051-9058
		REVISION	6.0.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	35 OF 109
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	32 OF 86
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			





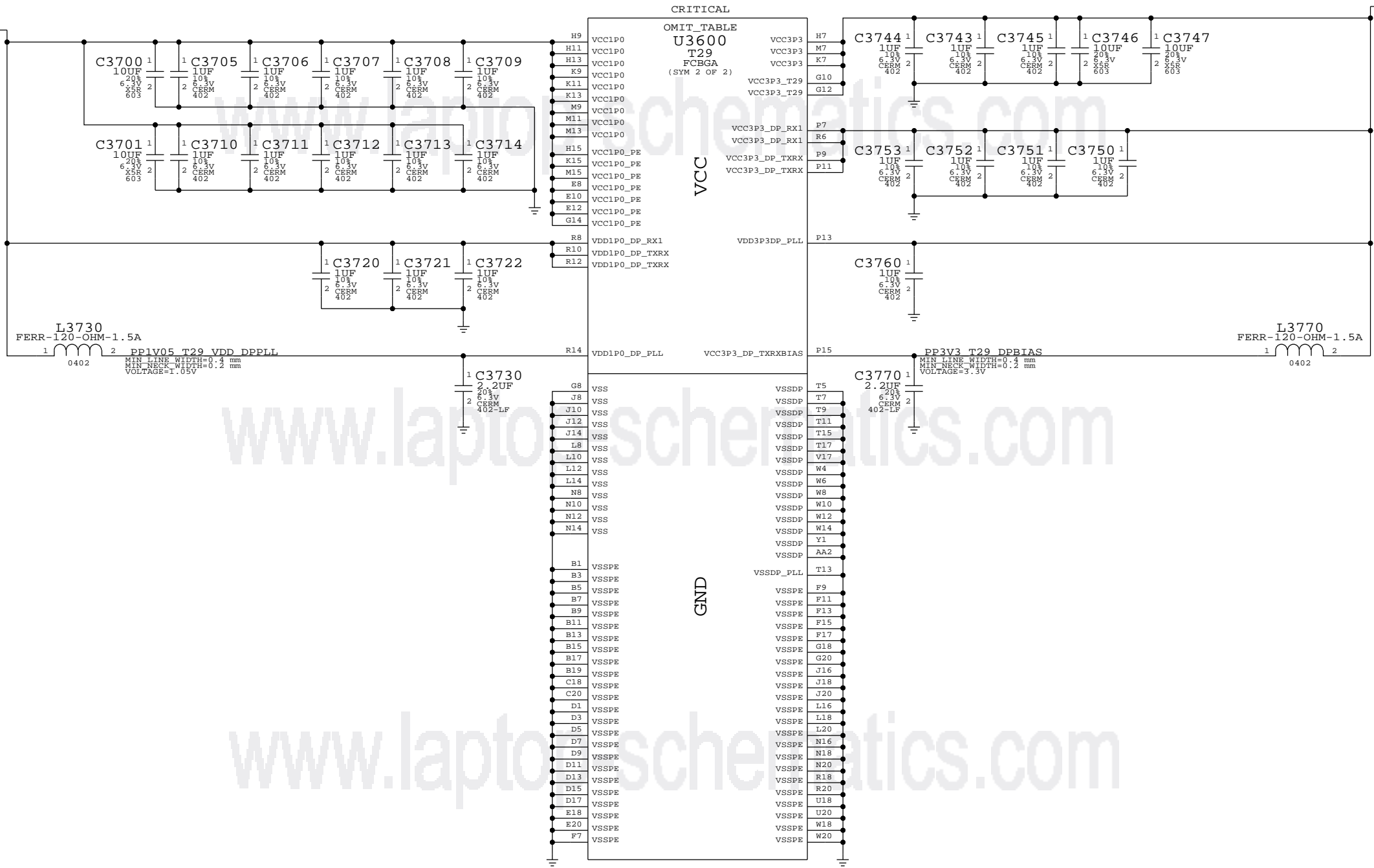
D  
C  
B  
A

D  
C  
B  
A

8 7 6 5 4 3 2 1


=PP1V05 T29\_RTR  
2100 mA (Single Port)  
2250 mA (Dual Port)  
EDP: 3000 mA

=PP3V3 T29\_RTR  
135 mA (Single-Port)  
152 mA (Dual-Port)  
EDP: 200 mA



Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

8 7 6 5 4 3 2 1

SYNC MASTER=K901 MLB		SYNC DATE=02/15/2011	
PAGE TITLE			
T29 Host (2 of 2)			
	Apple Inc.	DRAWING NUMBER	051-9058
		D	
		REVISION	6.0.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		37 OF 109	
II NOT TO REPRODUCE OR COPY IT		SHEET	
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		34 OF 86	
IV ALL RIGHTS RESERVED			

## D

C


B

A



## C

A

SYNCH MASTER-K90I MLE		SYNCH DATE-02/15/2011	
PAGE TITLE			
T29 Power Support			
	Apple Inc.		DRAWING NUMBER 051-9058
			SIZE D
			REVISION 6.0.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		PAGE 38 OF 109	
		SHEET 35 OF 86	



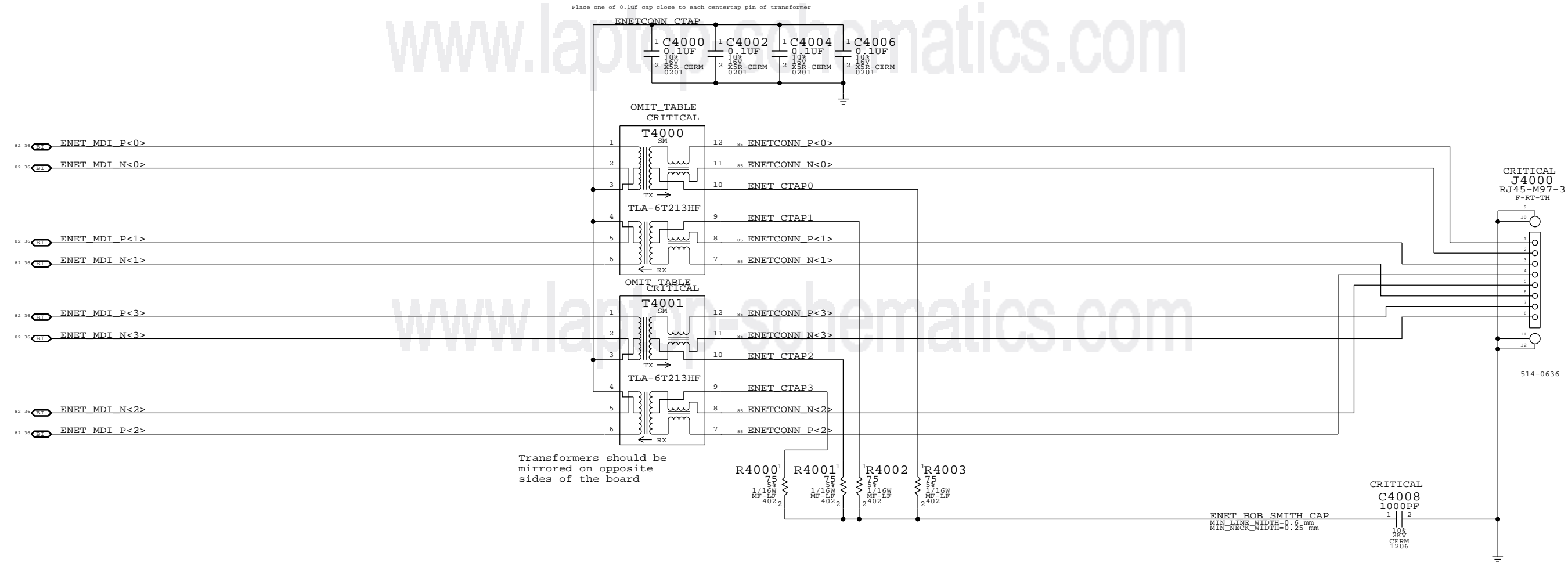


Page Notes


Power aliases required by this page:  
(NONE)

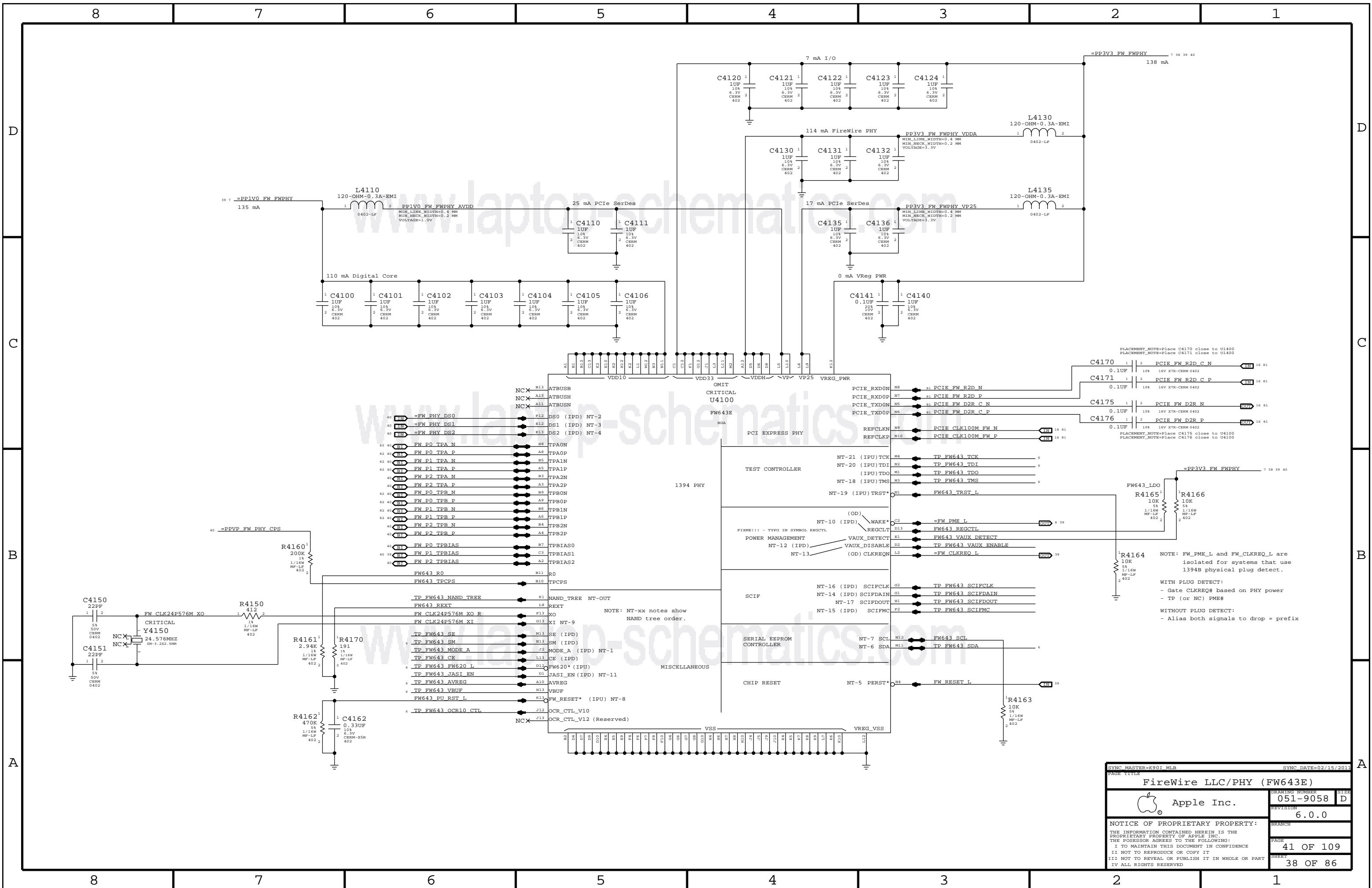
Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
157S0084	2	XFMR, ISO, HALF-PORT, 1000T, 12P, SMD, HF	T4000, T4001	CRITICAL	

SYNC MASTER=K901 MLB		SYNC DATE=02/15/2013	
PAGE TITLE			
Ethernet Connector			
 Apple Inc.		DRAWING NUMBER	051-9058
		REVISION	6.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		BRANCH	
		PAGE	40 OF 109
		SHEET	37 OF 86



Page Notes

Power aliases required by this page:

- =PPBUS\_S5\_FWPWRSW (FW VP FET Input)
- =PPBUS\_FW\_FET (FW VP FET Output)
- =PP3V3\_FW\_P3V3FWEET (3.3V FET Input)
- =PP3V3\_FW\_FET (3.3V FET Output)
- =PP3V3\_FW\_FWPHY (PHY 3.3V Power)
- =PP3V3\_S0\_FWLATEVG
- =PP3V3\_S0\_FWPWRCTL
- =PP1V05\_S0\_FWPWRCTL (5KPD Bias Rail)
- =PP1V05\_FW\_P1V0FWFET (1.0V FET Input)
- =PP1V0\_FW\_FET\_R (1.0V FET Output)
- =PP1V0\_FW\_FWPHY (PHY 1.0V)

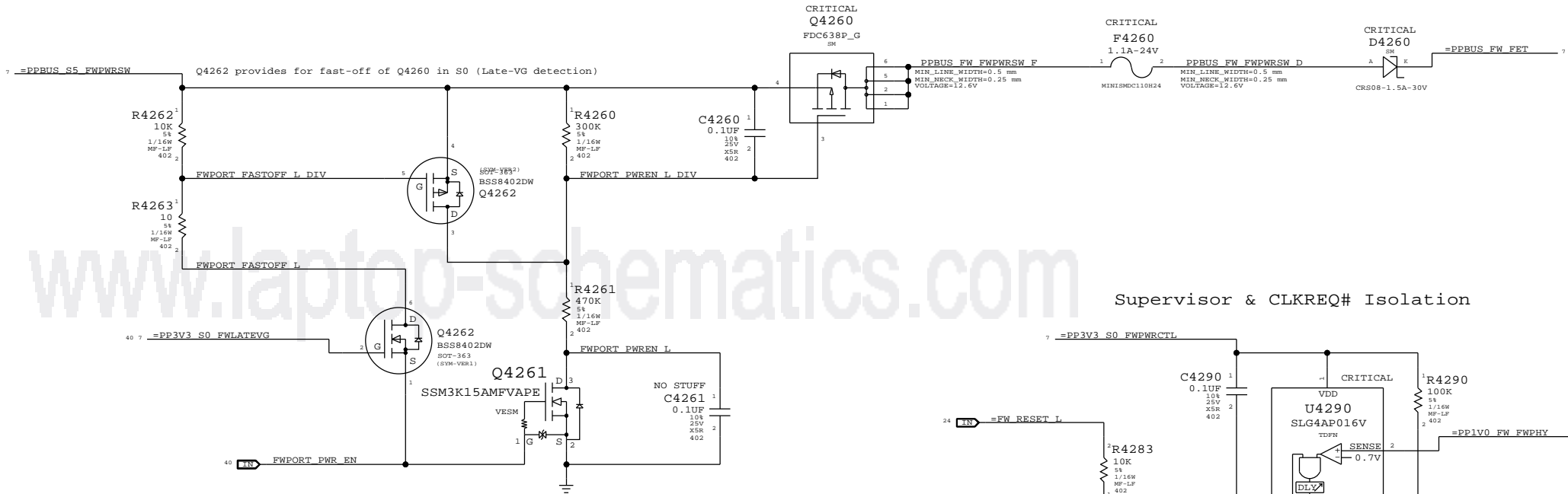
Signal aliases required by this page:

- =FW\_CLKREQ\_L
- =FW\_PME\_L

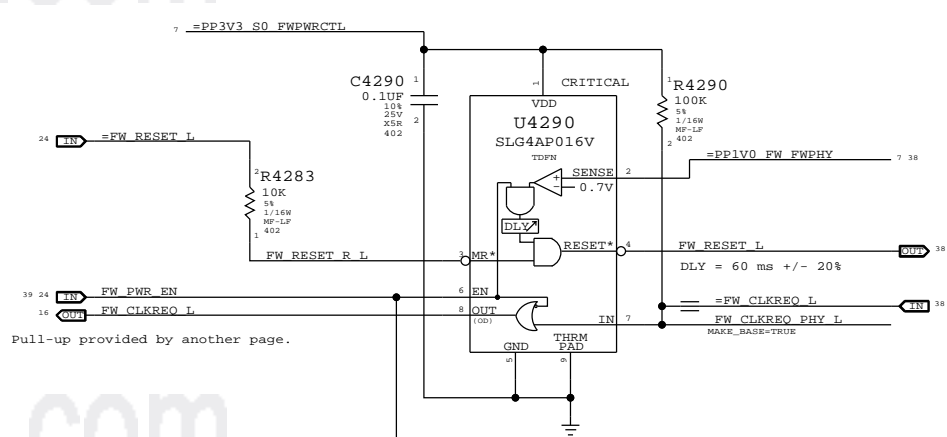
BOM options provided by this page:

(NONE)

FireWire Port Power Switch

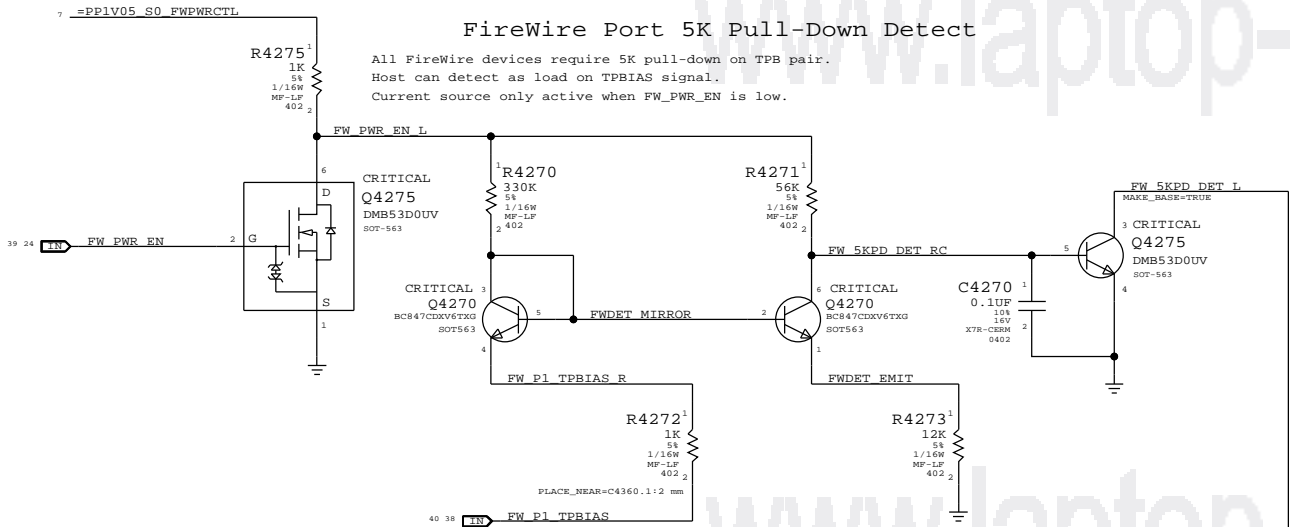


Supervisor & CLKREQ# Isolation



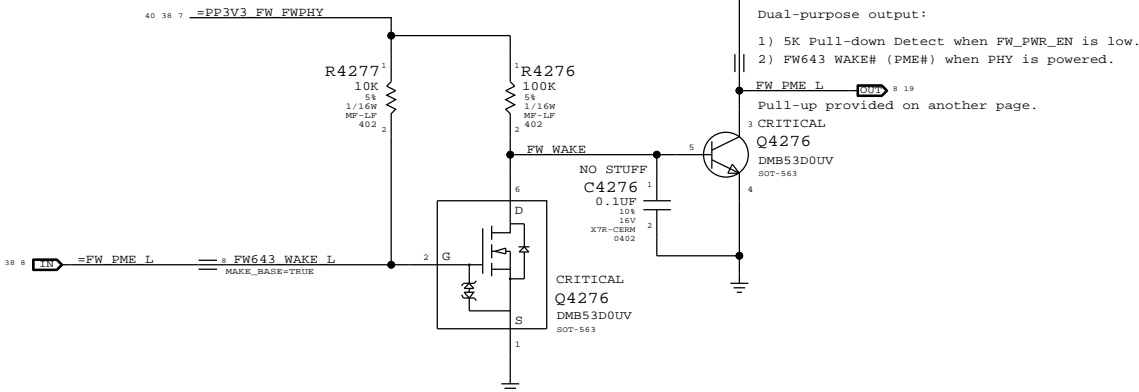
FireWire Port 5K Pull-Down Detect

All FireWire devices require 5K pull-down on TPBIAS signal.  
Host can detect as load on TPBIAS signal.  
Current source only active when FW\_PWR\_EN is low.



FireWire PHY WAKE# Support

When PHY is powered, FW\_5KPD\_DET\_L acts as legacy PME# signal.

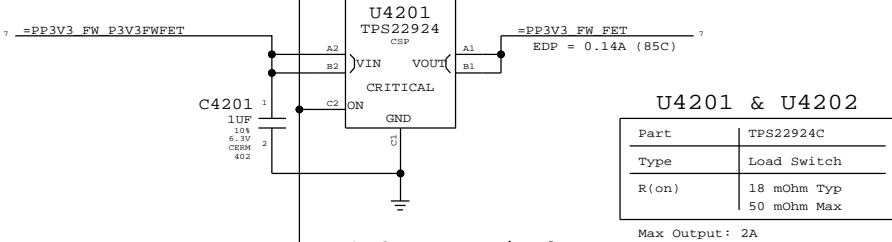


Dual-purpose output:

- 1) 5K Pull-down Detect when FW\_PWR\_EN is low.
- 2) FW643 WAKE# (PME#) when PHY is powered.

Pull-up provided on another page.

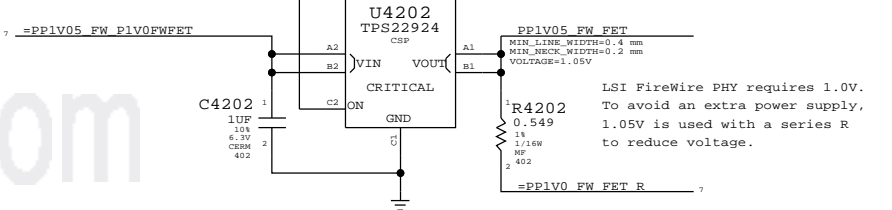
3.3V FW Switch



U4201 & U4202	
Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

1.0V FW Switch



LSI FireWire PHY requires 1.0V.  
To avoid an extra power supply,  
1.05V is used with a series R  
to reduce voltage.

TEXT NOTE FOR 3.3V RAIL CURRENT CHANGED TO EDP NUMBER.

SYNC MASTER=K901 MLB		SYNC DATE=06/23/2011	
PAGE TITLE			
FireWire Port & PHY Power		DRAWING NUMBER	051-9058
Apple Inc.		REVISION	6.0.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	42 OF 109
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	39 OF 86
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			

Page Notes

Power aliases required by this page:

- =PPVP\_FW\_PORT1
- =PPVP\_FW\_PHY\_CPS\_FET (From Port)
- =PPVP\_FW\_PHY\_CPS (To PHY)
- =PP3V3\_FW\_FWPHY
- =PP3V3\_S0\_FWLATEVG

Signal aliases required by this page:

- =FW\_PHY\_DS0
- =FW\_PHY\_DS1
- =FW\_PHY\_DS2

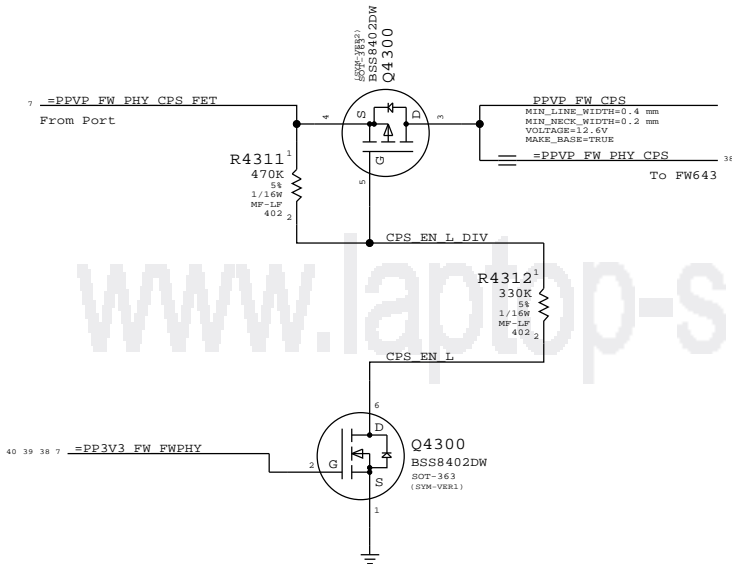
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:

(NONE)  
1394b implementation based on Apple  
FireWire Design Guide (FWDG 0.6, 5/14/03)

FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VDD33.  
FET blocks current to TPCPS until VDD33 is powered.



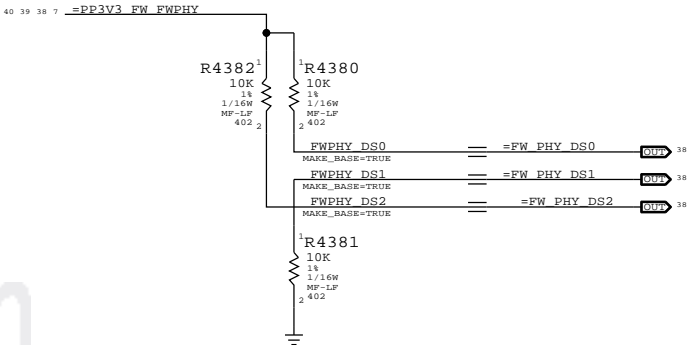
Unused FireWire Ports

Disabled per LSI instructions  
(All unused port signals TP/NC)



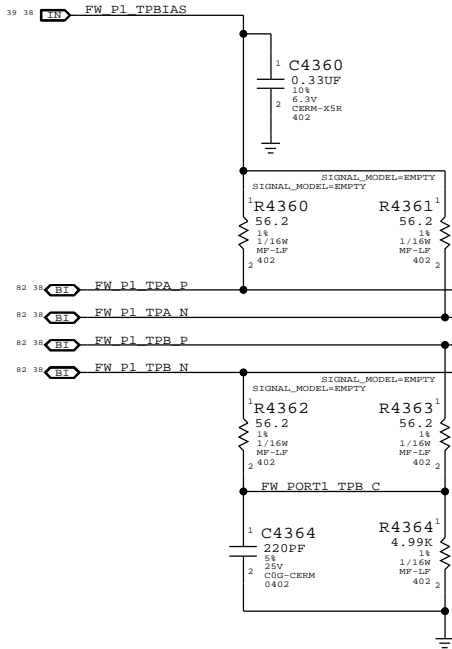
FireWire PHY Config Straps

Configures PHY for:  
- Port "1" Bilingual (1394B)



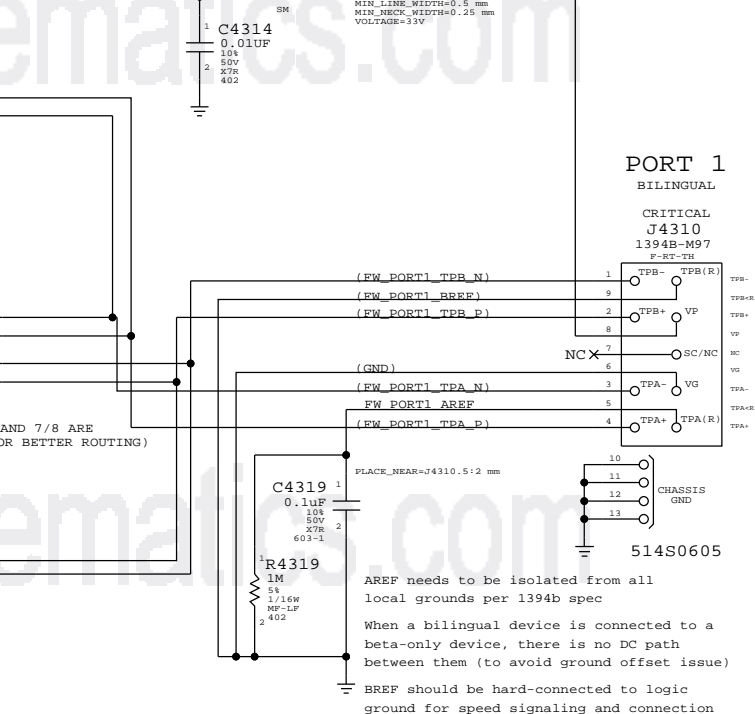
Termination

Place close to FireWire PHY



Cable Power

Note: Trace PPVP\_FW\_PORT1 must handle up to 5A



PORT 1

BILINGUAL

CRITICAL

J4310

1394B-M97

F-RT-TH

TPB(R)

TPB+

TPB-

VP

NC/NC

VG

TPA-

TPA(R)

TPA+

CHASSIS

GND

514S0605

AREF needs to be isolated from all local grounds per 1394b spec  
When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)  
BREF should be hard-connected to logic ground for speed signaling and connection

CANNOT SYNC THIS PAGE FROM T27, TPA AND TPB FOR U4350 IS SWAPPED

FireWire Connector

Apple Inc.

DRAWING NUMBER

051-9058

REVISION

6.0.0

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.

THE POSSESSOR AGREES TO THE FOLLOWING:

I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART

IV ALL RIGHTS RESERVED

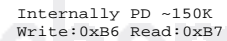
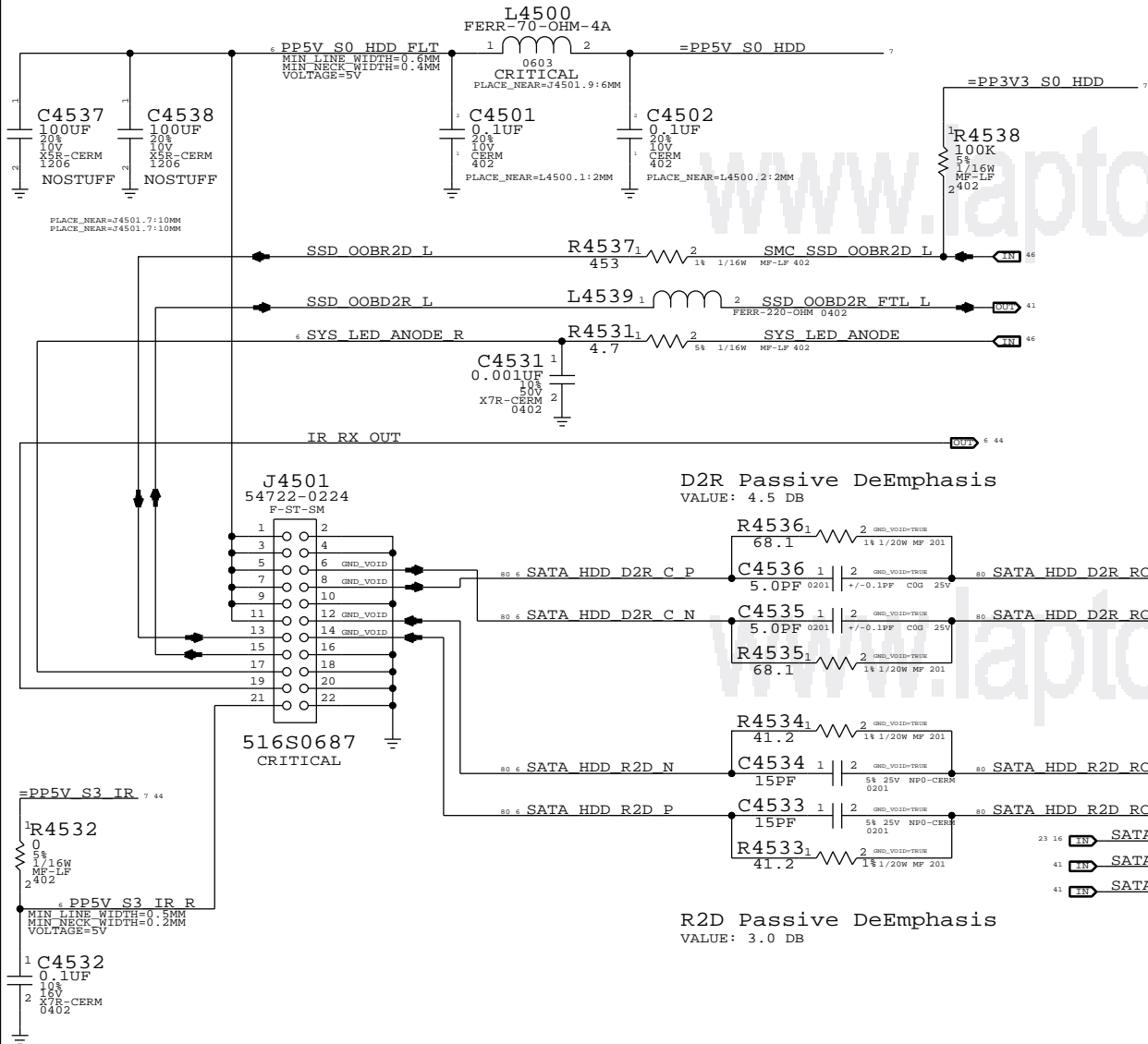
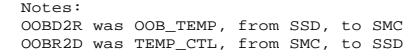
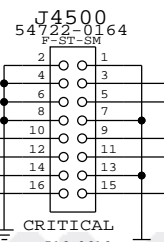
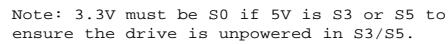
PAGE

43 OF 109

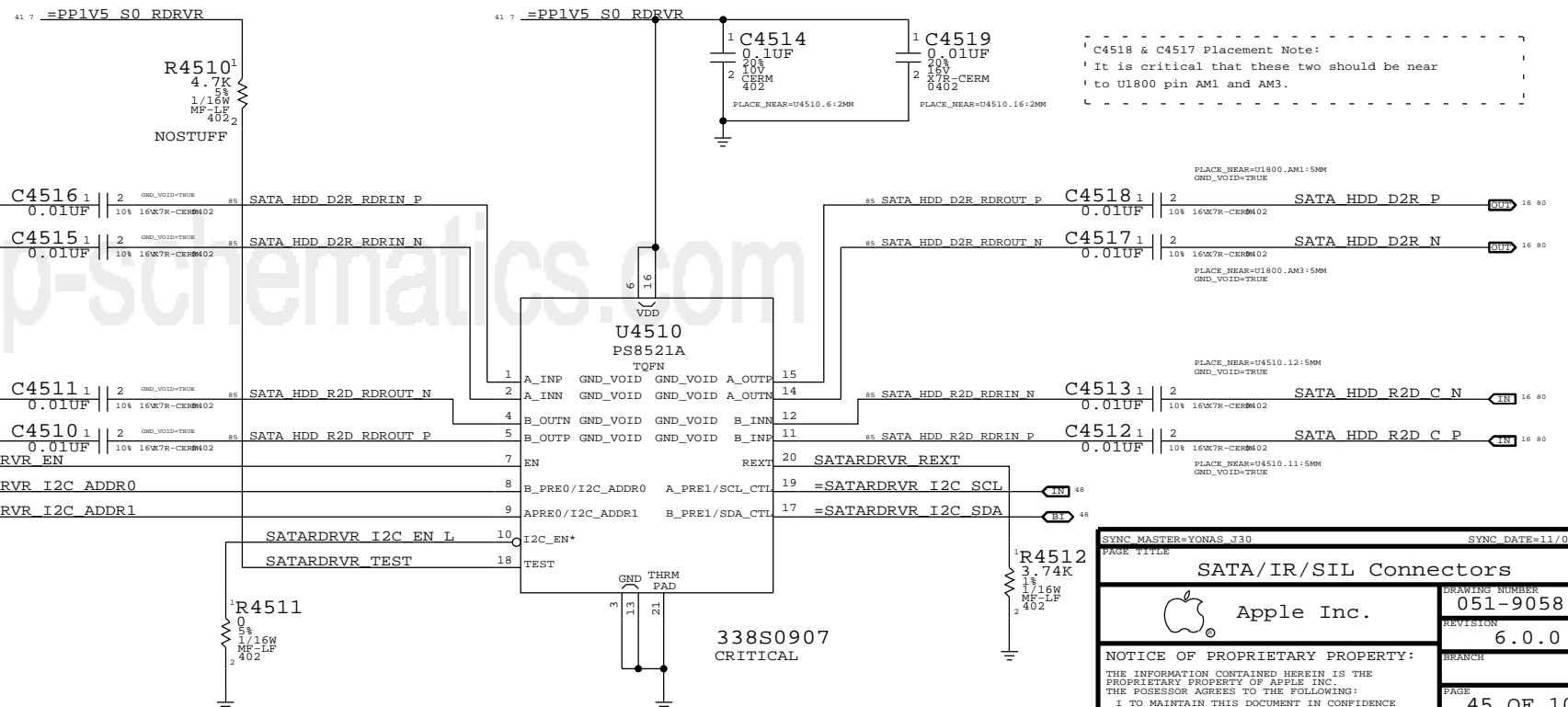
SHEET

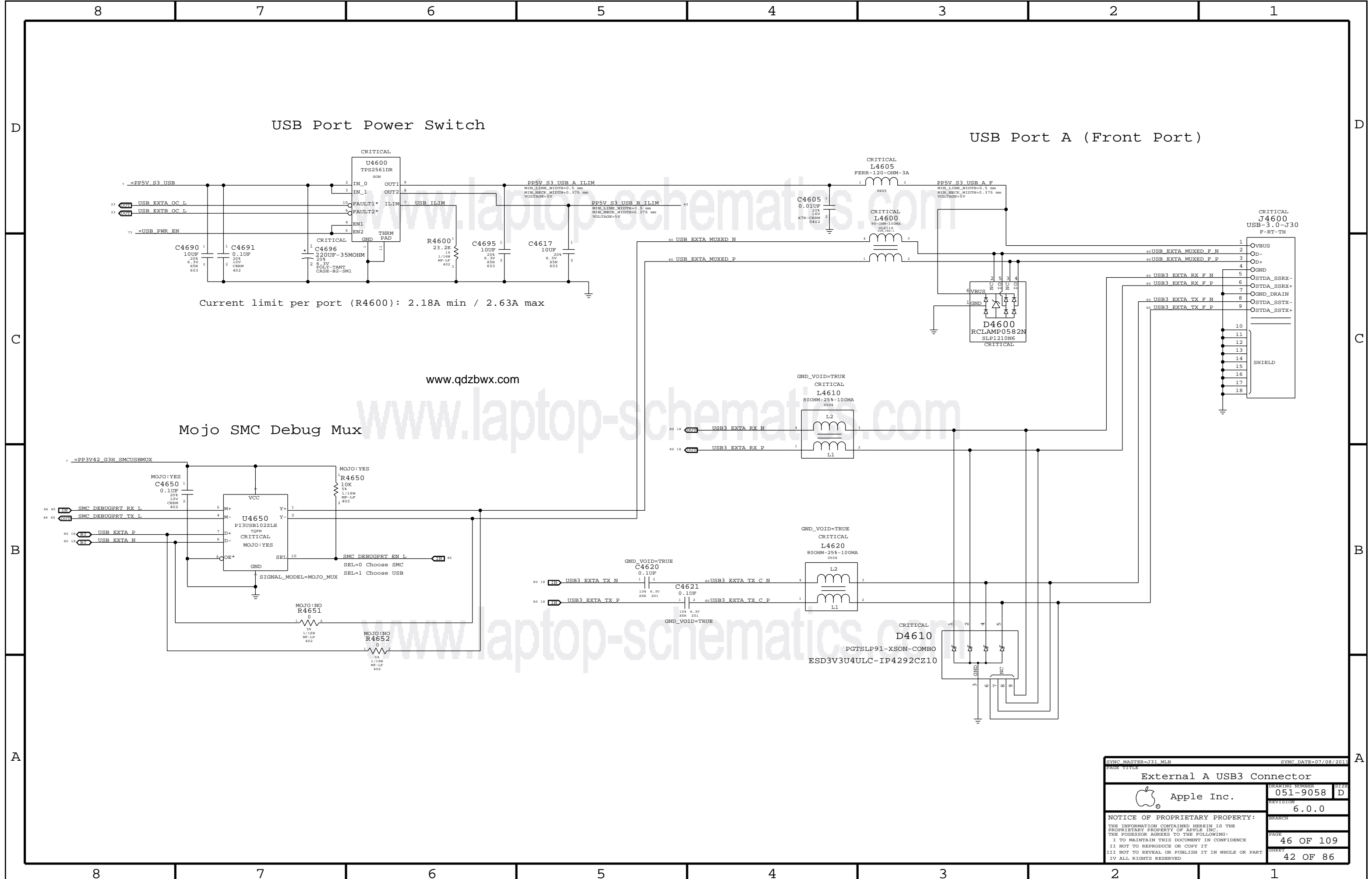
40 OF 86

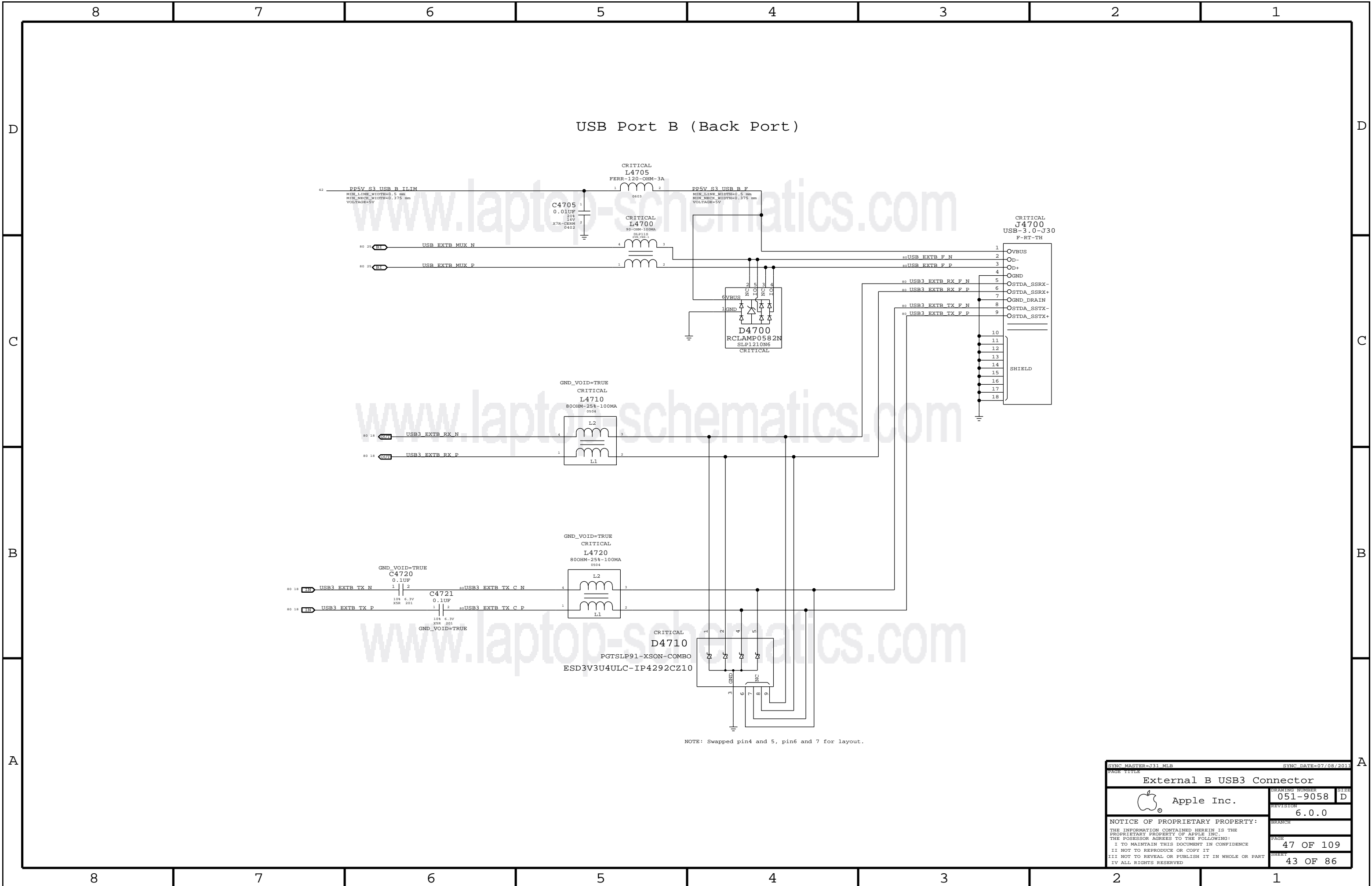





ADDR1	ADD0	Address (R/W)
L	L	0x96/0x97
L	H	0x98/0x99
H	L	0xB6/0xB7
H	H	0xB8/0xB9






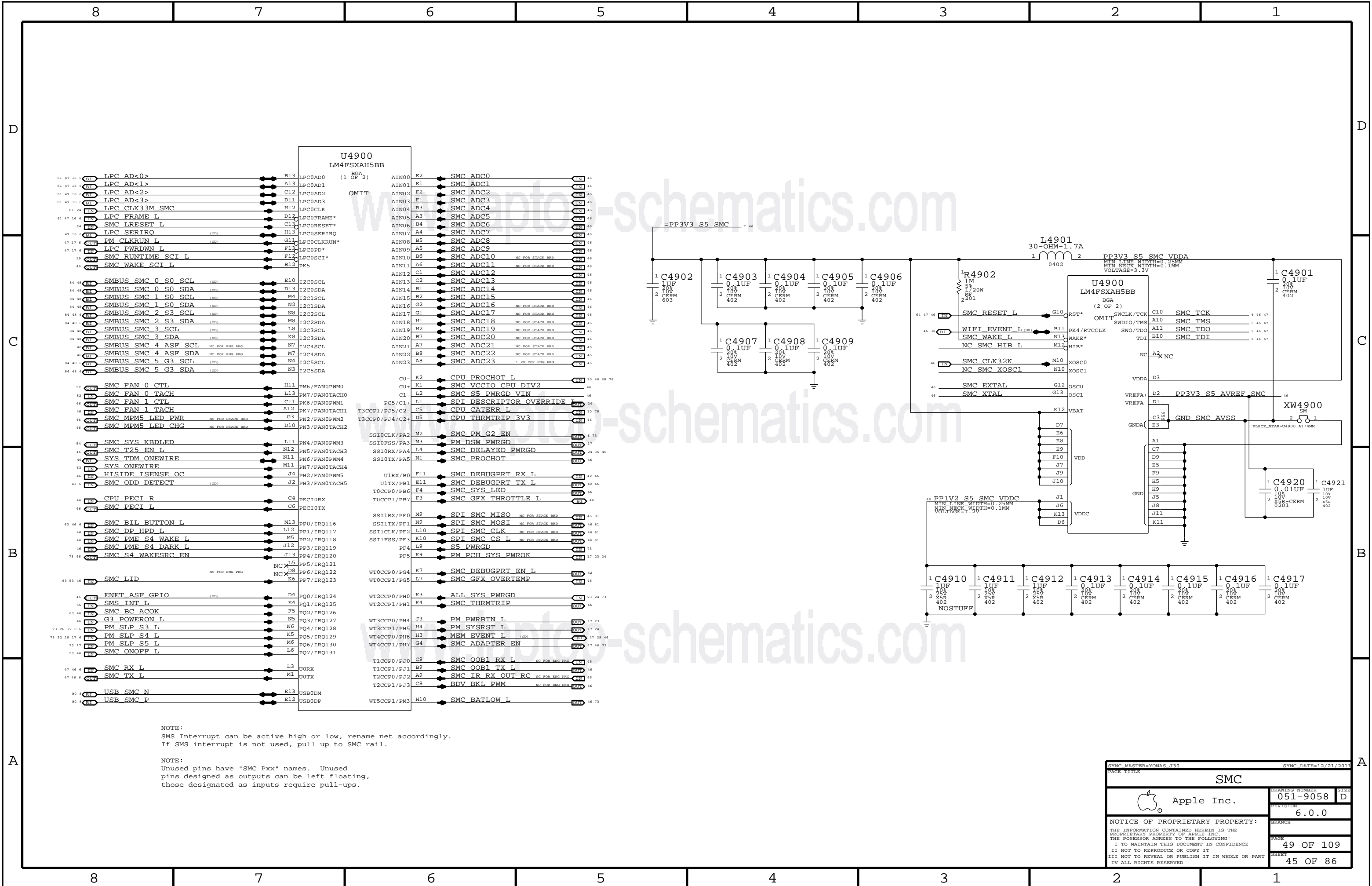


SYNC MASTER=J31 MLB		SYNC DATE=07/08/2011	
PAGE TITLE			
External B USB3 Connector			
 Apple Inc.		DRAWING NUMBER	051-9058
		SIZE	D
		REVISION	6.0.0
NOTICE OF PROPRIETARY PROPERTY:			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.			
THE POSSESSOR AGREES TO THE FOLLOWING:			
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			
		BRANCH	
		PAGE	47 OF 109
		SHEET	43 OF 86

The schematic shows a USB to RS485 module using a CY7C6803-LQXC IC. The IC is connected to a USB port (pins 1, 2, 3, 4) and an RS485 port (pins 1, 2, 3, 4). The IC is labeled U4800 and CY7C6803-LQXC. The USB pins are labeled USB\_IR\_P, USB\_IR\_N, and USB\_TPAD. The RS485 pins are labeled RS485\_P, RS485\_N, and RS485\_TPAD. The IC is connected to a 5V supply and ground.


SYMC MASTER=K901 MLB		SYMC DATE=02/15/2013	
PAGE TITLE			
Front Flex Support			
	Apple Inc.		DRAWING NUMBER 051-9058
			SIZE D
		REVISION 6.0.0	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I NOT TO REPRODUCE OR COPY IT I IT NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I IV ALL RIGHTS RESERVED		PAGE 48 OF 109	
		SHEET 44 OF 86	

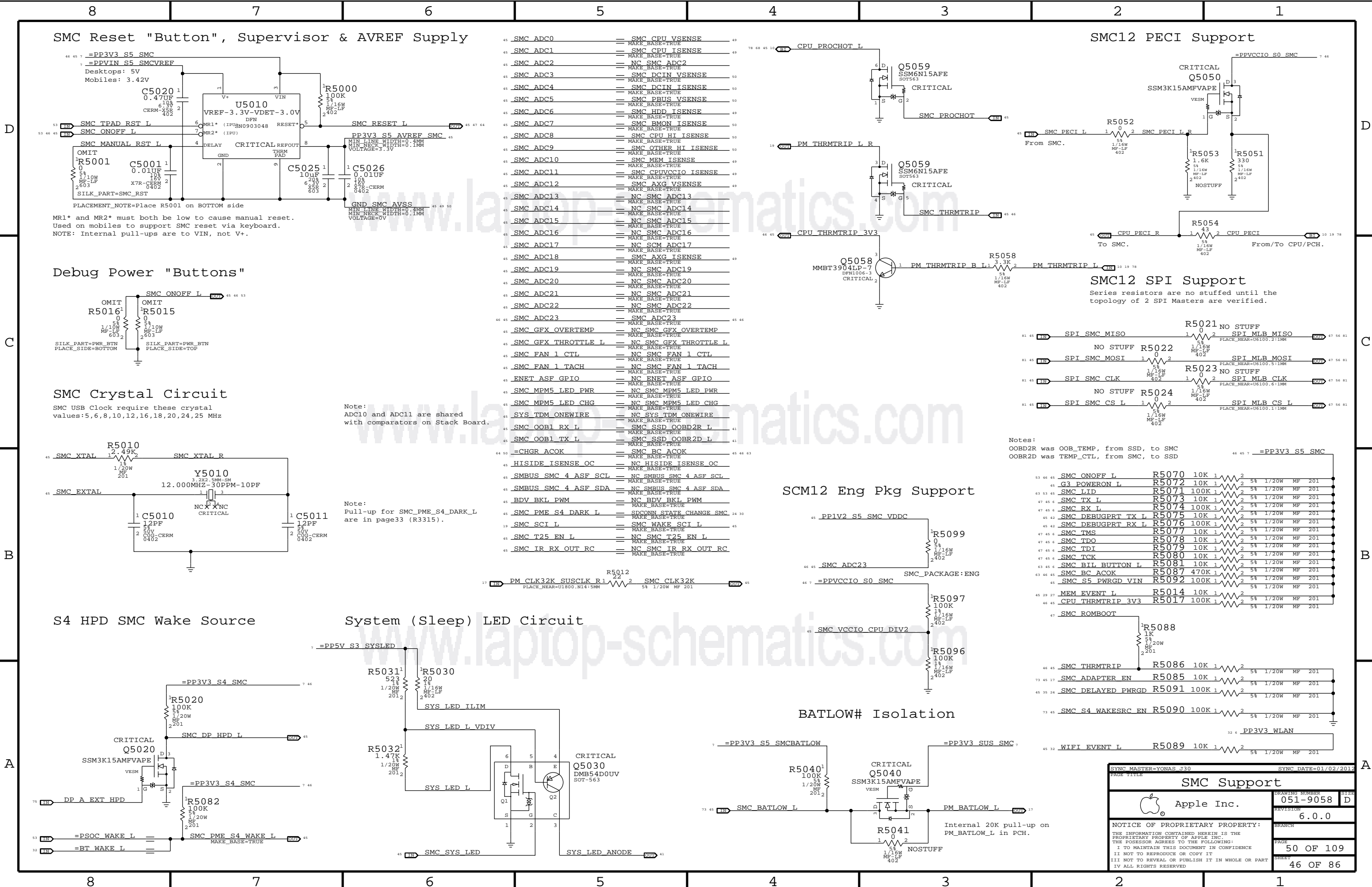




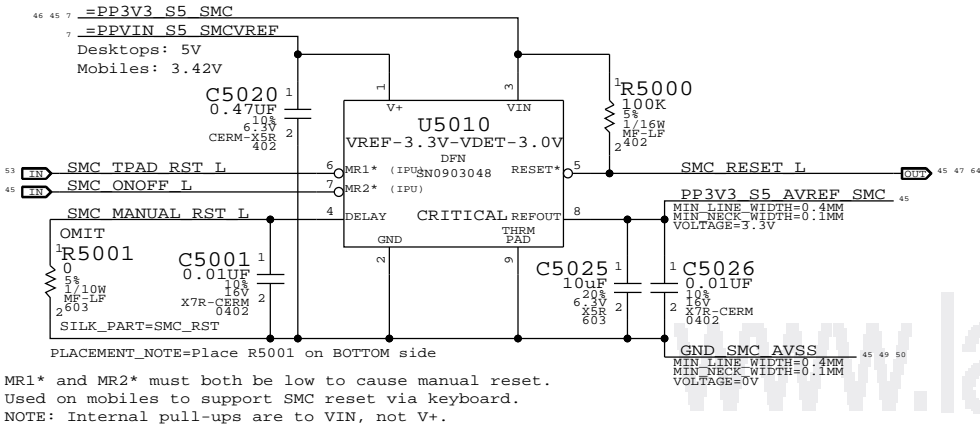
NOTE:  
SMS Interrupt can be active high or low, rename net accordingly.  
If SMS interrupt is not used, pull up to SMC rail.

NOTE:  
Unused pins have "SMC\_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

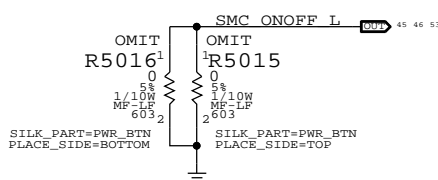
SYNC MASTER=YONAS J30		SYNC DATE=12/21/2011	
PAGE TITLE			
SMC		DRAWING NUMBER	SIZE
 Apple Inc.		051-9058	D
		REVISION	
NOTICE OF PROPRIETARY PROPERTY:		6.0.0	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.		BRANCH	
THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	
I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		49 OF 109	
II NOT TO REPRODUCE OR COPY IT		SHEET	
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		45 OF 86	
IV ALL RIGHTS RESERVED			



### SMC Reset "Button", Supervisor & AVREF Supply

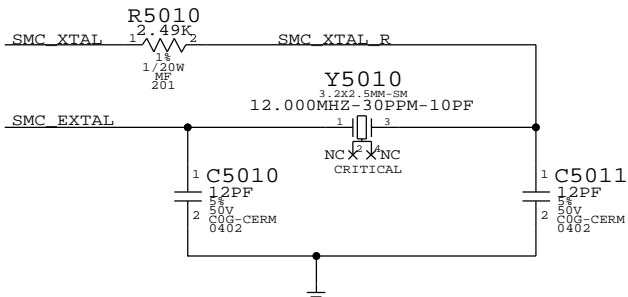


### Debug Power "Buttons"

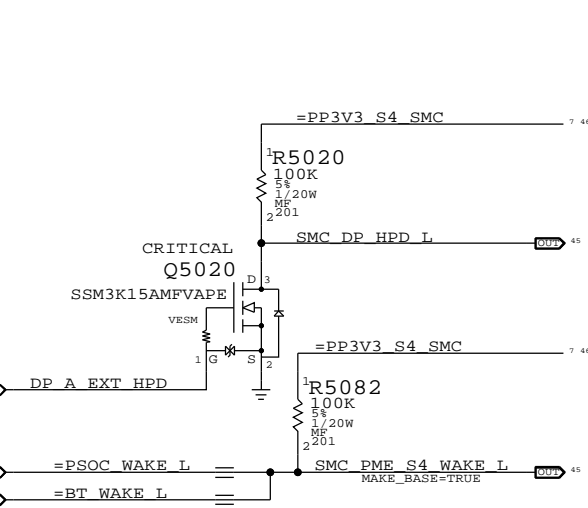


### SMC Crystal Circuit

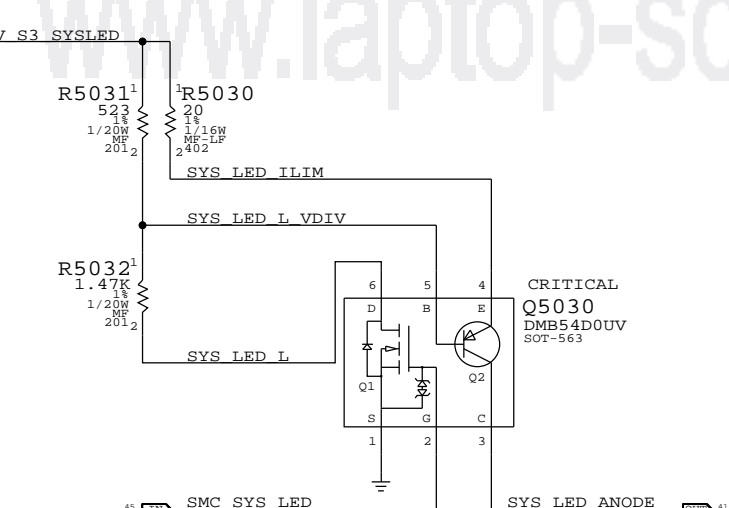
SMC USB Clock require these crystal values:5,6,8,10,12,16,18,20,24,25 MHz



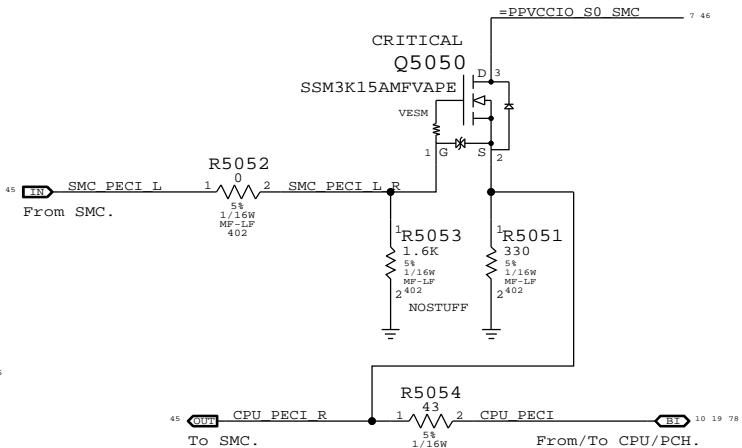
### S4 HPD SMC Wake Source



### System (Sleep) LED Circuit

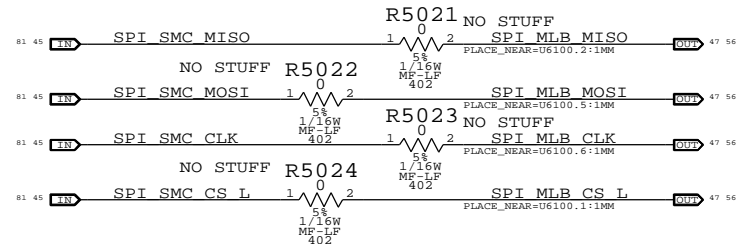


### SMC12 PECCI Support



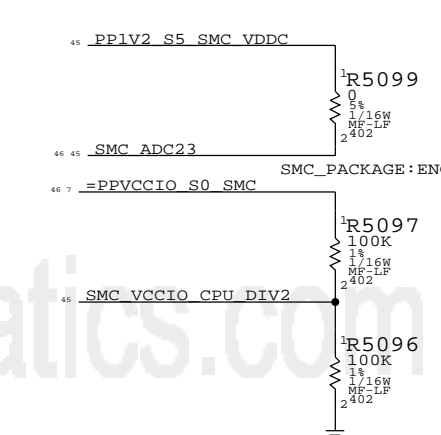
### SMC12 SPI Support

Series resistors are no stuffed until the topology of 2 SPI Masters are verified.

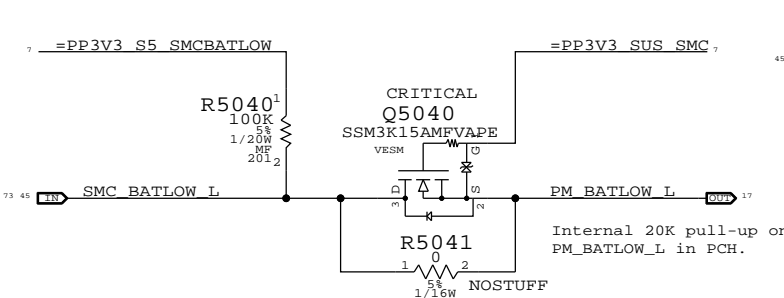


Notes:  
O0BD2R was OOB\_TEMP, from SSD, to SMC  
O0BR2D was TEMP\_CTL, from SMC, to SSD

### SCM12 Eng Pkg Support



### BATLOW# Isolation



SYNC MASTER=YONAS J30		SYNC DATE=01/02/2012	
PAGE TITLE		PAGE	
SMC Support		6.0.0	
Apple Inc.		50 OF 109	
NOTICE OF PROPRIETARY PROPERTY:		46 OF 86	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:			
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			

LPCPLUS\_CONN:YES  
J5100  
55909-0374

7 =PP3V3 S5 LPCPLUS  
7 =PP5V\_S0 LPCPLUS


32 32

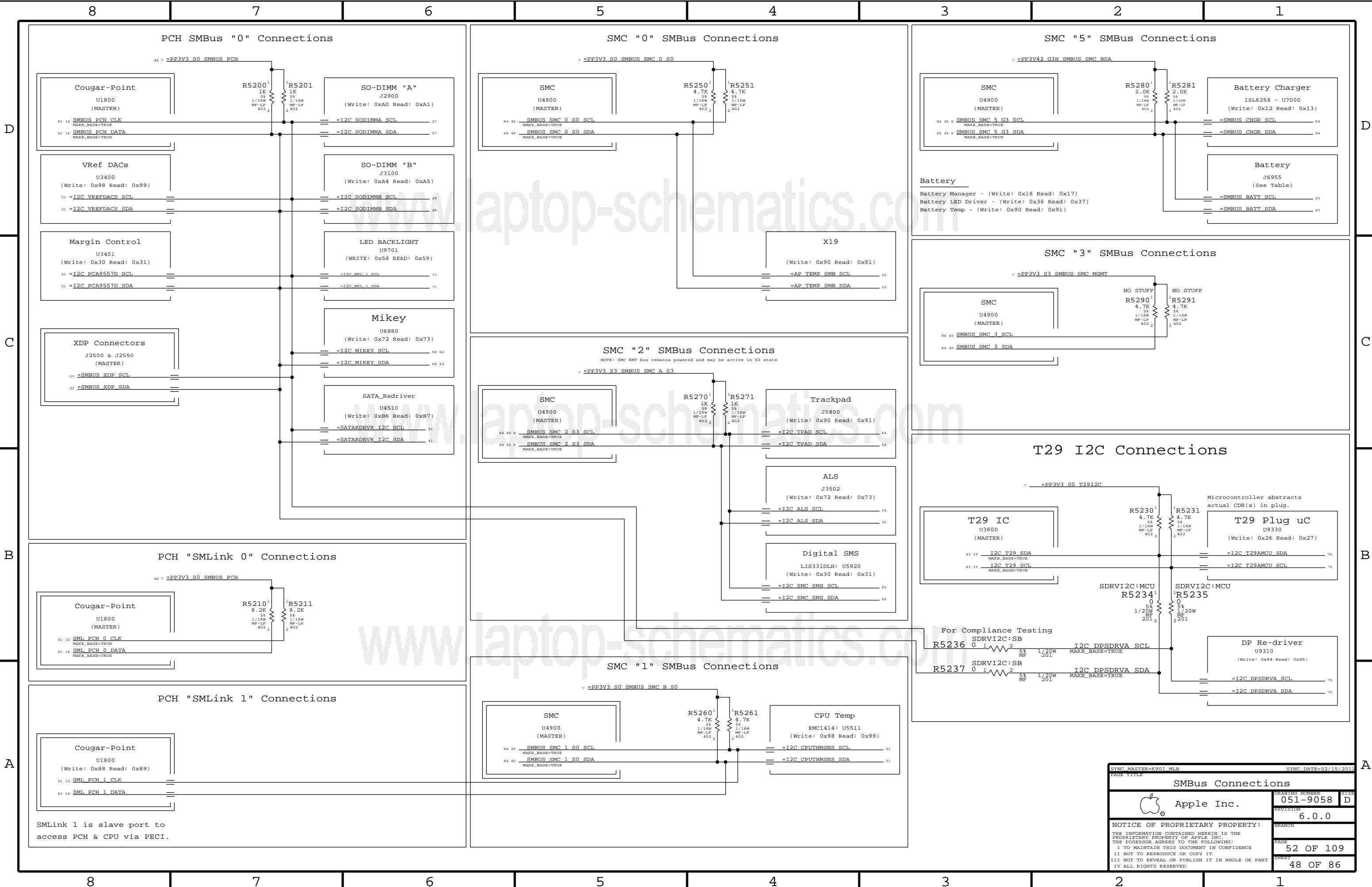
1 2  
3 4  
5 6

81 40 16 6 24 81  
LPC AD<0>  
LPC AD<1>

LPC CLK33M LPCPLUS  
LPC AD<2>  
LPC AD<3>



SYNC MASTER=J31 MLB		SYNC DATE=06/15/2011	
PAGE TITLE			
LPC+SPI Debug Connector			
	DRAWING NUMBER		SIZE
	051-9058		D
Apple Inc.	REVISION		
	6.0.0		
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		51 OF 109	
II NOT TO REPRODUCE OR COPY IT		SHEET	
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		47 OF 86	
IV ALL RIGHTS RESERVED			





8

7

6

5

4

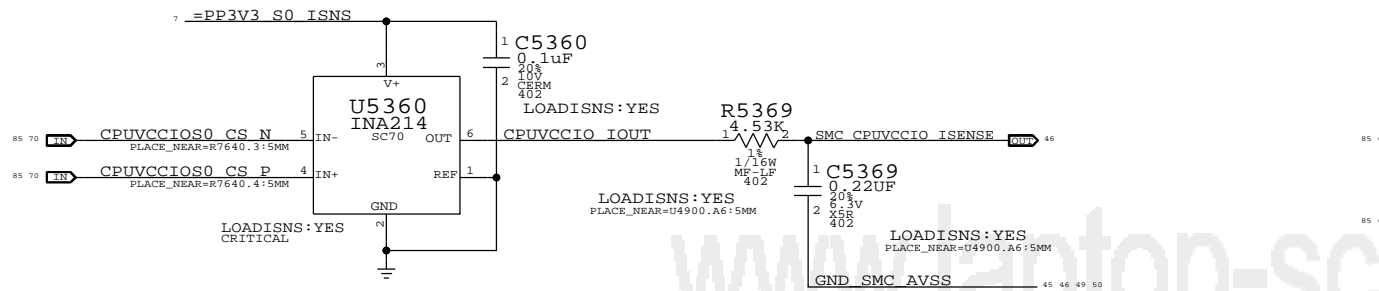
3

2

1

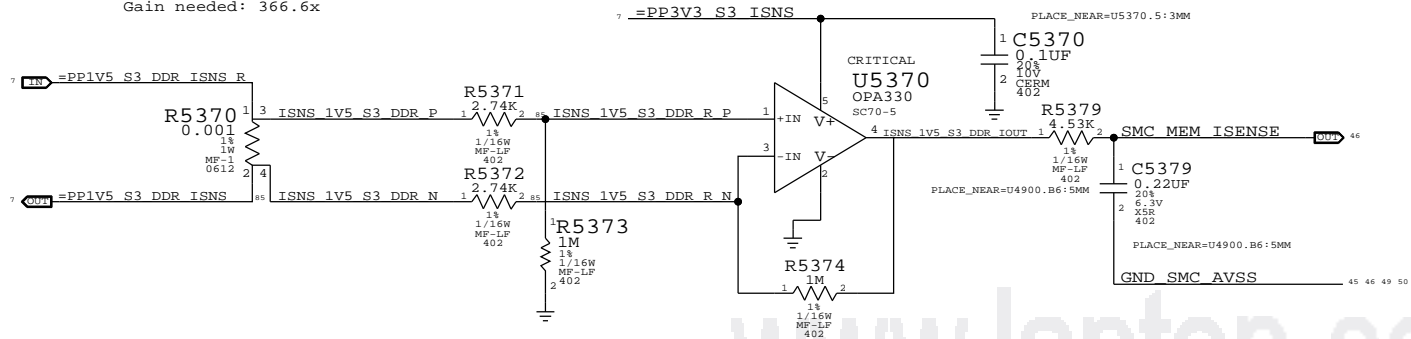
## CPU VCCIO 1.05V Load Side Current Sense (IC1C)

Gain: 100x, EDP: 20.1 A  
Rsense: 0.001 (R7640)  
V across Rsense: 20.1 mV  
Gain needed: 164.2x



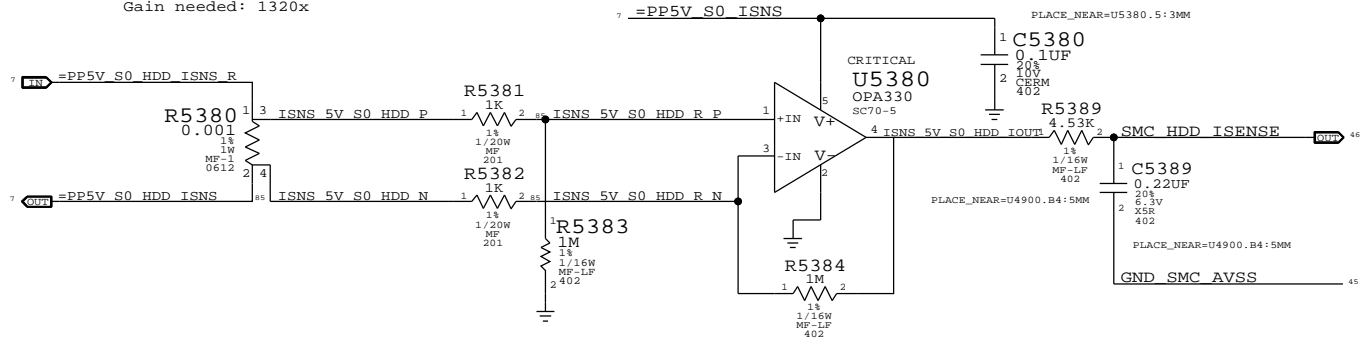
## DDR 1.5V S3 (Memory) Current Sense (IM0C)

Gain: 364.9x, EDP: 9 A  
Rsense: 0.001 (R5370)  
V across Rsense: 9 mV  
Gain needed: 366.6x

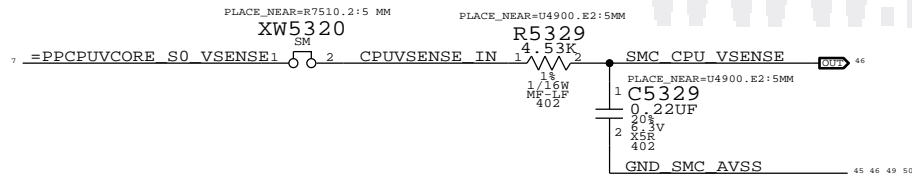


## HDD Current Sense (IHDC)

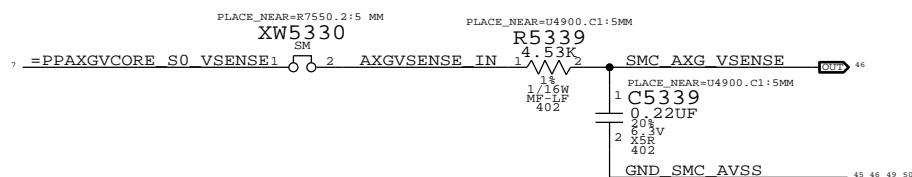
Gain: 1000x, EDP: 2.5 A (12.5 W)  
Rsense: 0.001 (R5380)  
V across Rsense: 2.5 mV  
Gain needed: 1320x



## CPU Core Voltage Sense (VC0C)

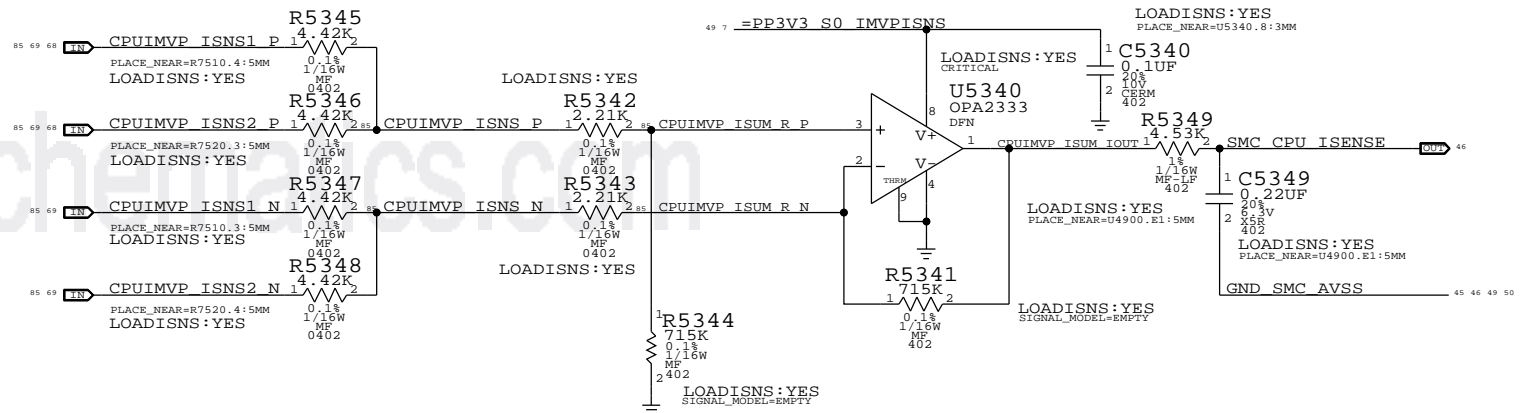


## AXG Core Voltage Sense (VN0C)



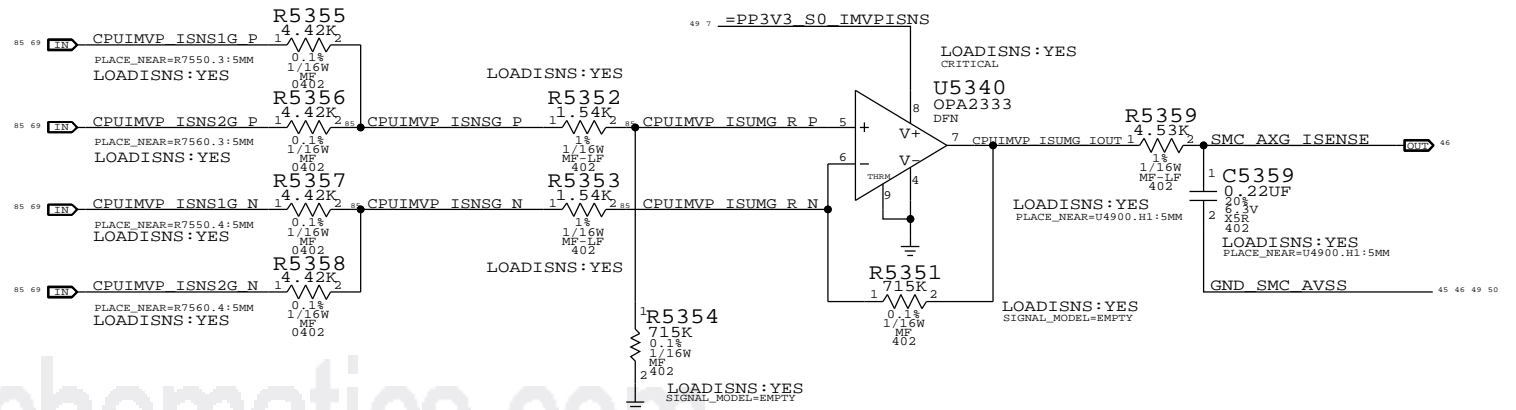
## CPU Core Load Side Current Sense (IC0C)

Gain: 161.5x, EDP: 53 A  
Rsense: 2x of 0.00075 (R7510, R7520), Rsum: 0.000375  
V across Rsense: 19.8 mV  
Gain needed: 166.1x




## AXG Core Load Side Current Sense (IN0C)

Gain: 190.6x, EDP: 46 A  
Rsense: 2x of 0.00075 (R7550, R7560), Rsum: 0.000375  
V across Rsense: 17.25 mV  
Gain needed: 191.3x

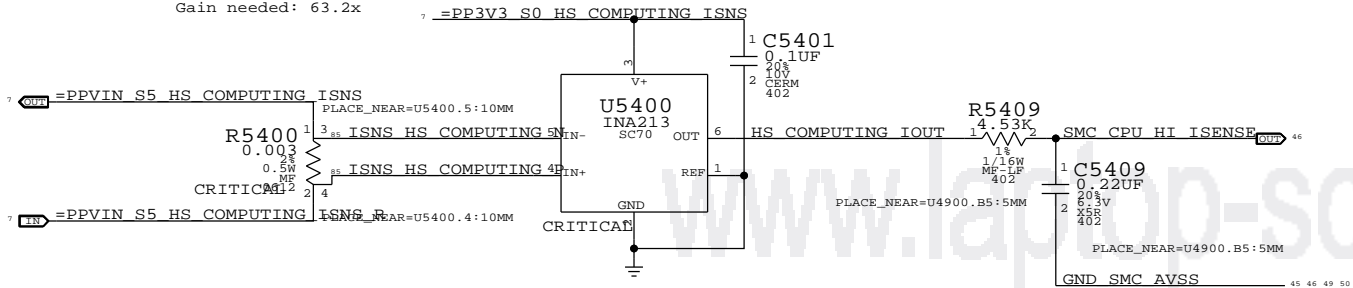


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0114	3	RES, MTL, FLIM, 100K, 1/16W, 0402, SMD, LF	C5349, C5359, C5369		LOADISNS: NO

SYNC MASTER=LINDA J30		SYNC DATE=09/28/2011	
PAGE TITLE			
Power Sensors: Load Side			
 Apple Inc.		DRAWING NUMBER	051-9058
		REVISION	6.0.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	53 OF 109
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	49 OF 86
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			

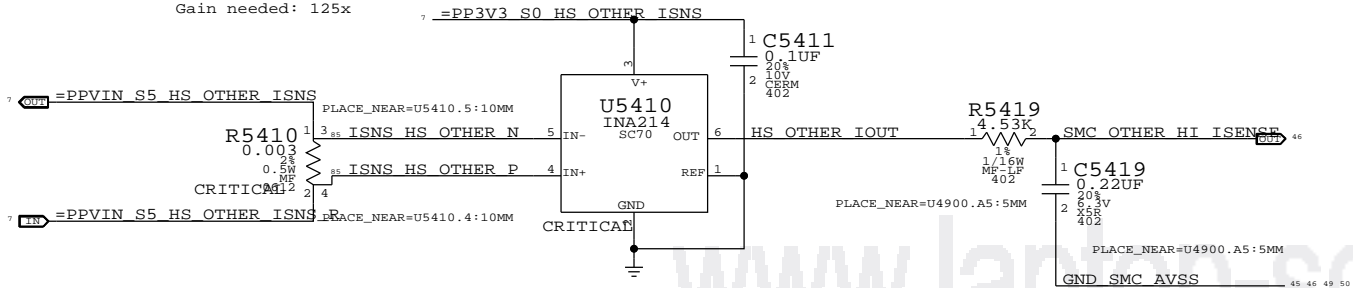
CPU High Side Current Sense (IC0R)

Gain: 50x, EDP: 17.4 A  
Rsense: 0.003 (R5400)  
V across Rsense: 52.2 mV  
Gain needed: 63.2x

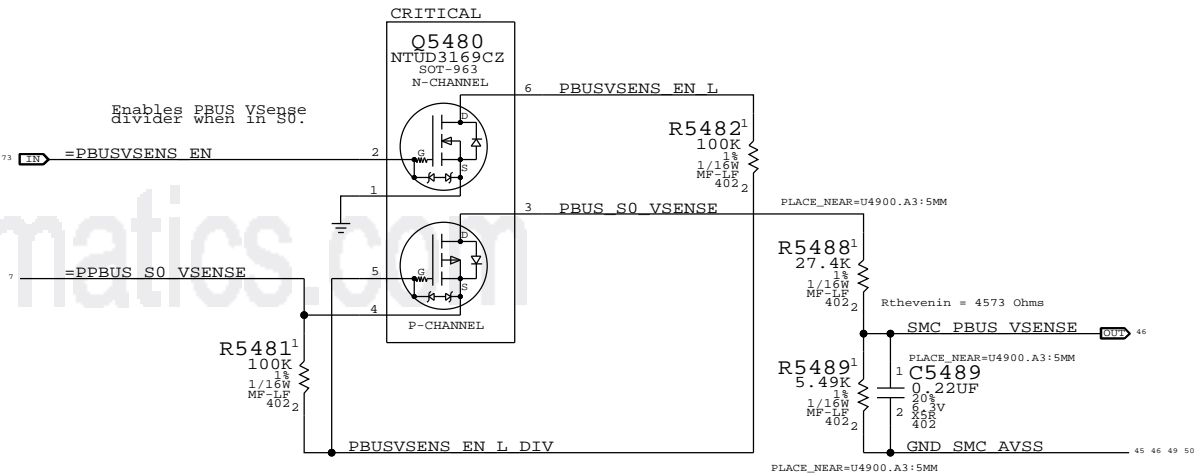


OTHER High Side Current Sense (IO0R)

Gain: 100x, EDP: 8.8 A  
Rsense: 0.003 (R5410)  
V across Rsense: 26.4 mV  
Gain needed: 125x

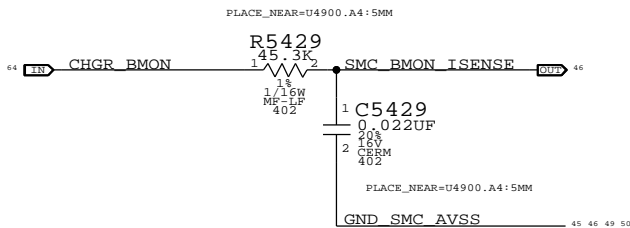


PBUS Voltage Sense & Enable (VP0R)



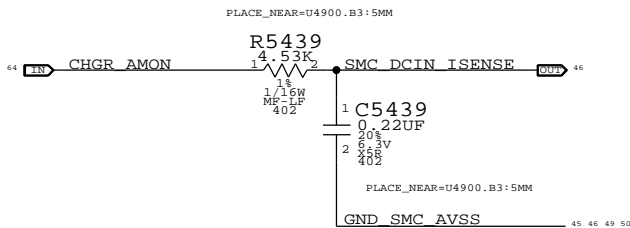
Charger (BMON Production) Current Sense (IPBR)

Charger Gain: 36x  
Rsense: 0.010 (R7050)  
Max Current Measured: 9.2 A

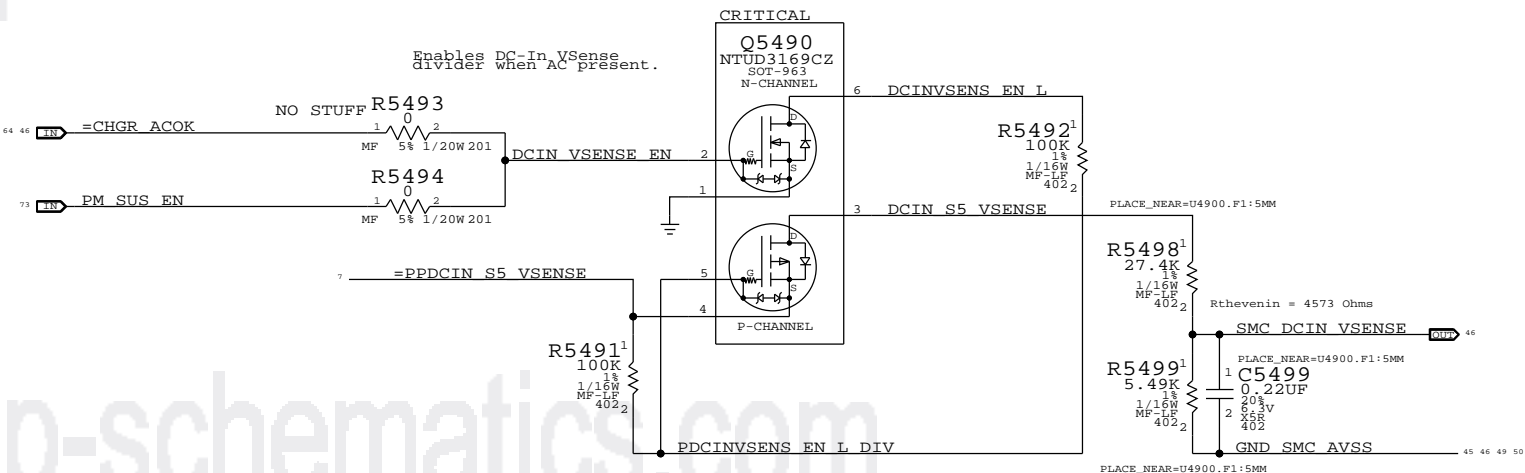


DC-In (AMON) Current Sense (ID0R)

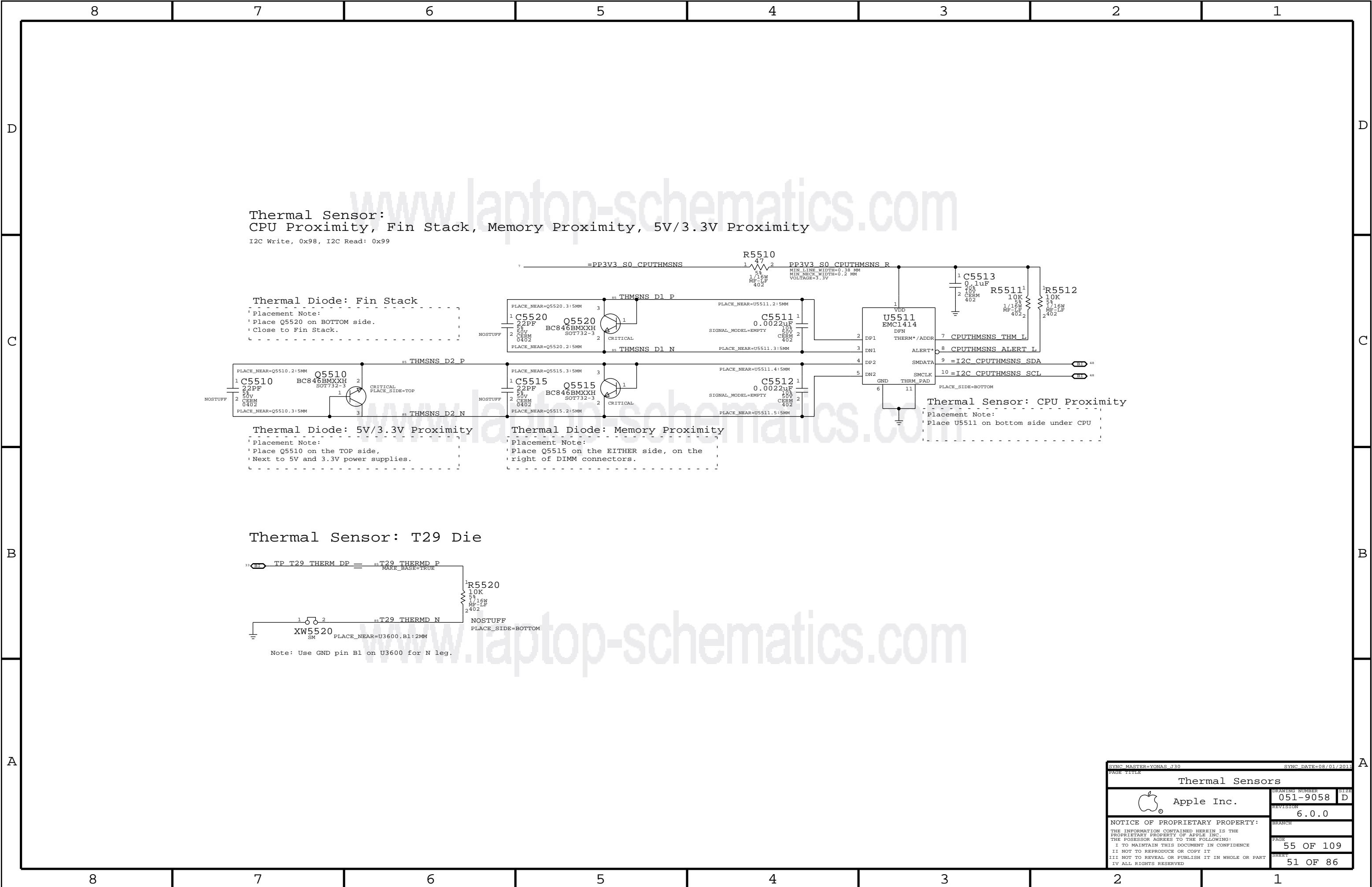
Charger Gain: 20x  
Rsense: 0.020 (R7020)  
Max Current Measured: 8.3 A



DC In Voltage Sense & Enable (VD0R)



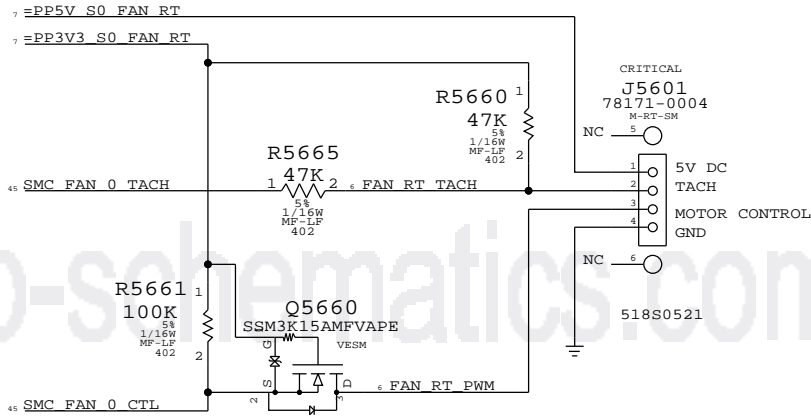
SYNC MASTER=YONAS J30		SYNC DATE=11/03/2011	
PAGE TITLE		Power Sensors: High Side	
Apple Inc.		DRAWING NUMBER	051-9058
		REVISION	6.0.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	54 OF 109
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	50 OF 86
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			




www.laptop-schematics.com

www.laptop-schematics.com

www.laptop-schematics.com

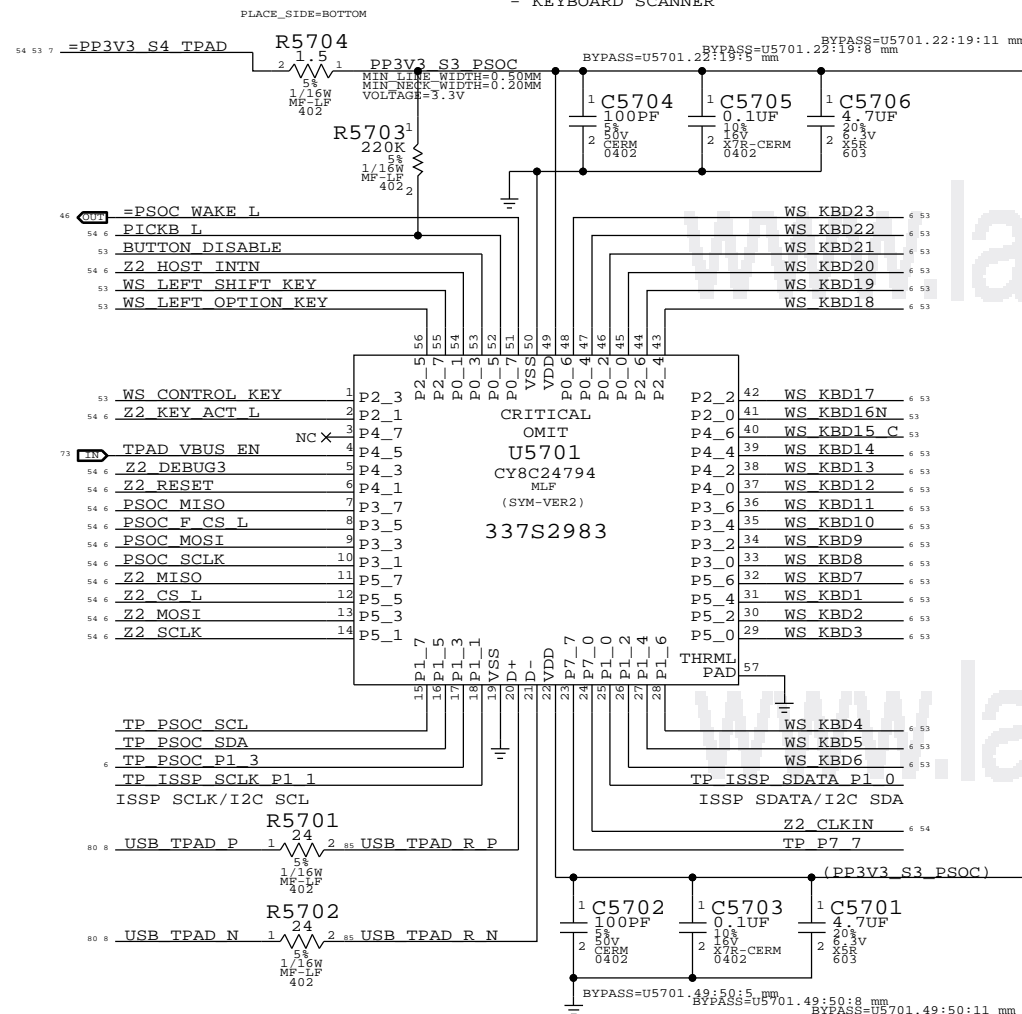


SYNC MASTER=K901 MLB		SYNC DATE=02/15/2011	
PAGE TITLE			
Fan			
 Apple Inc.		DRAWING NUMBER	051-9058
		REVISION	6.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		BRANCH	
		PAGE	56 OF 109
		SHEET	52 OF 86

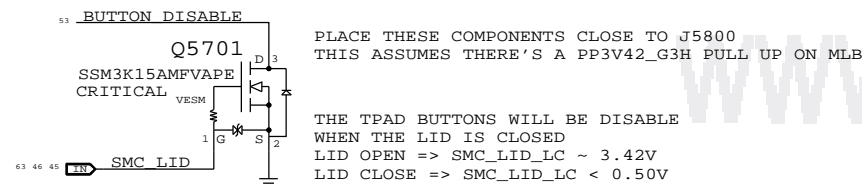


## PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER

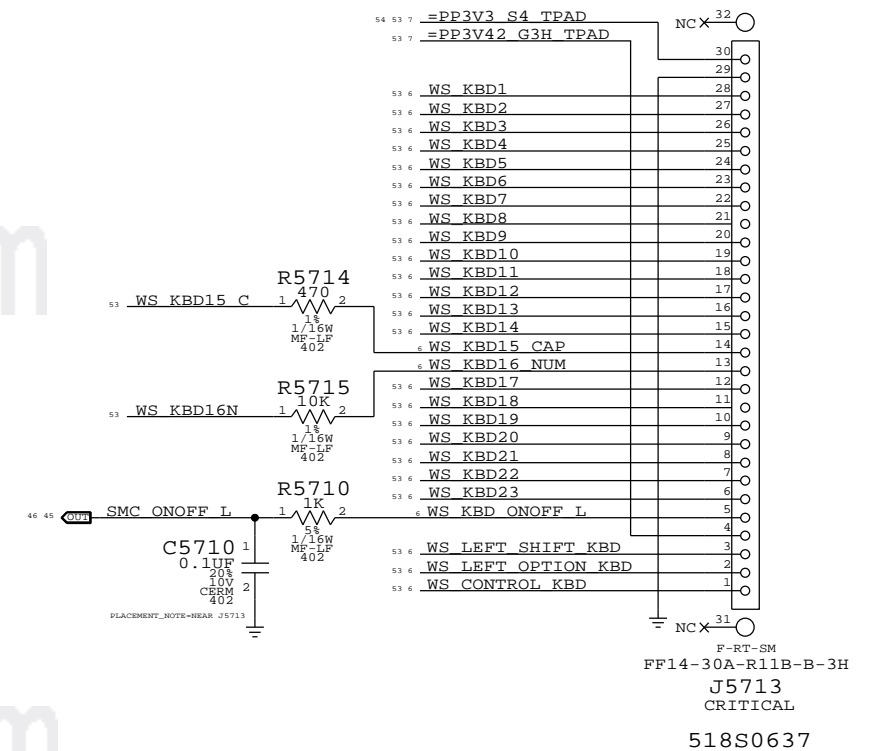


## TPAD Buttons Disable



IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6
		80UA		0.204 V	16.32E-6
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6
		14MA (MAX)		0.021 V	294E-6
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6

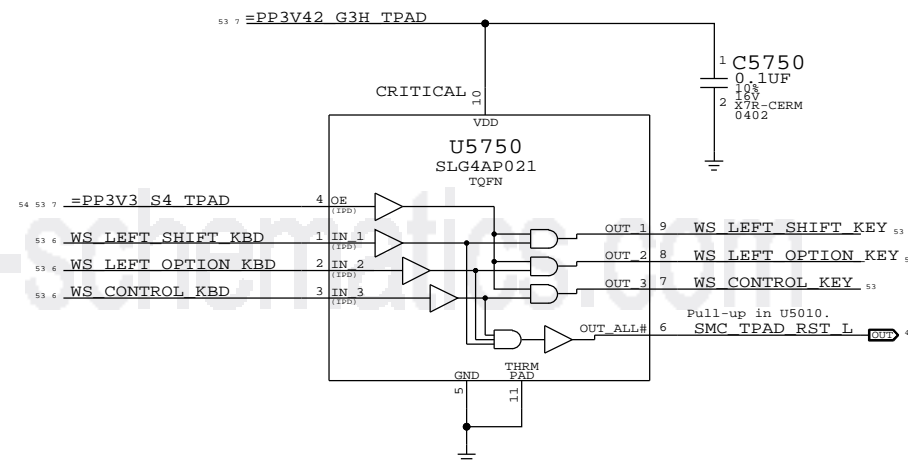
## Keyboard Connector



## SMC Manual Reset & Isolation

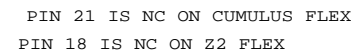
Left shift, option & control keys combined with power button cause SMC RESET# assertion.

Keys ANDed with MSP power to isolate when MSP is not powered. No IPD on OE input pin PP3V3\_S4 (symbol error).



BOOSTER DESIGN CONSIDERATION:

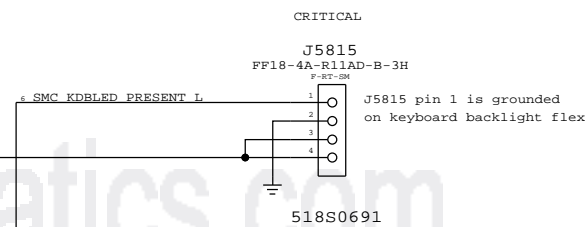
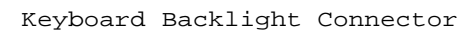
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED

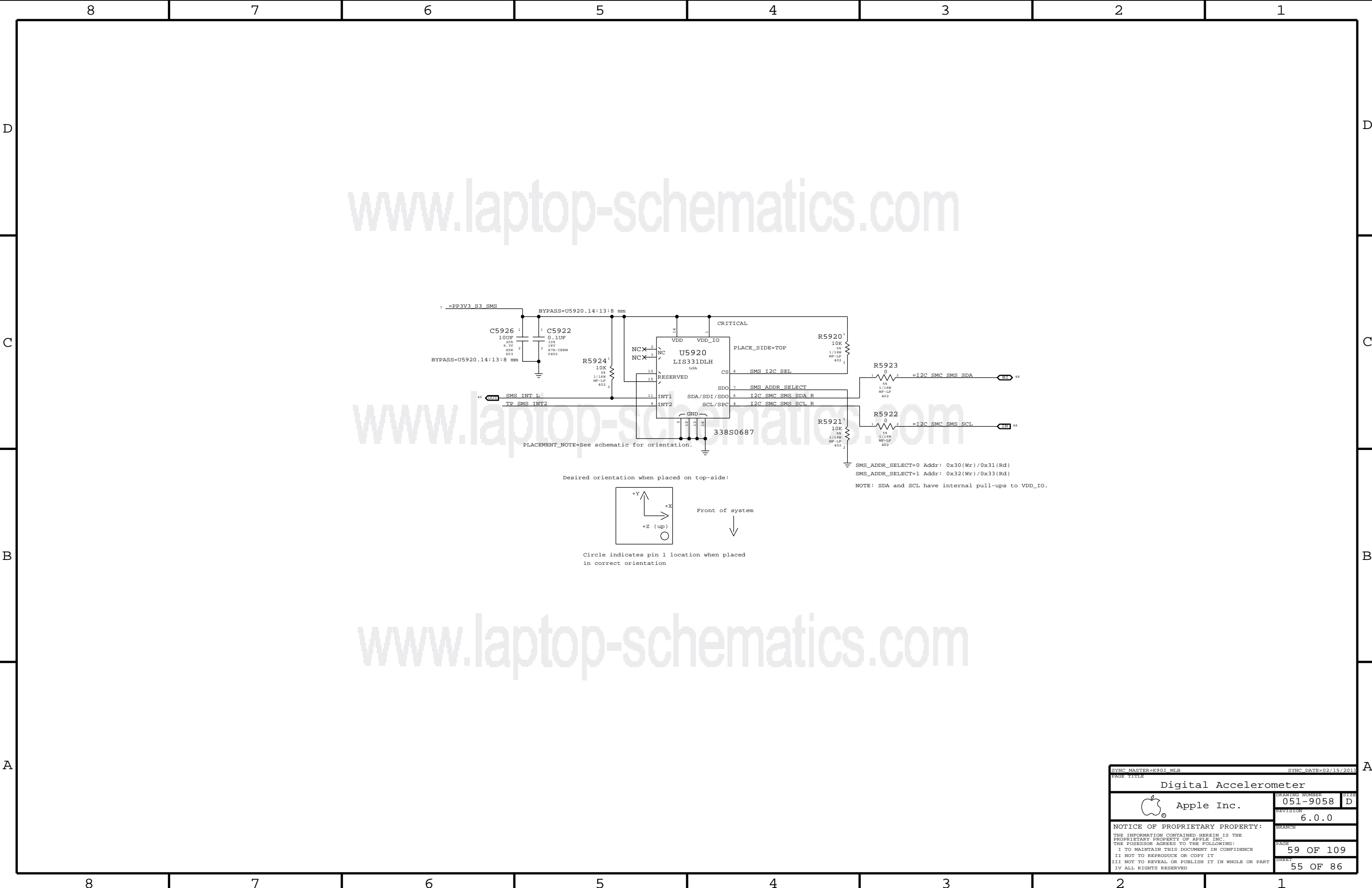


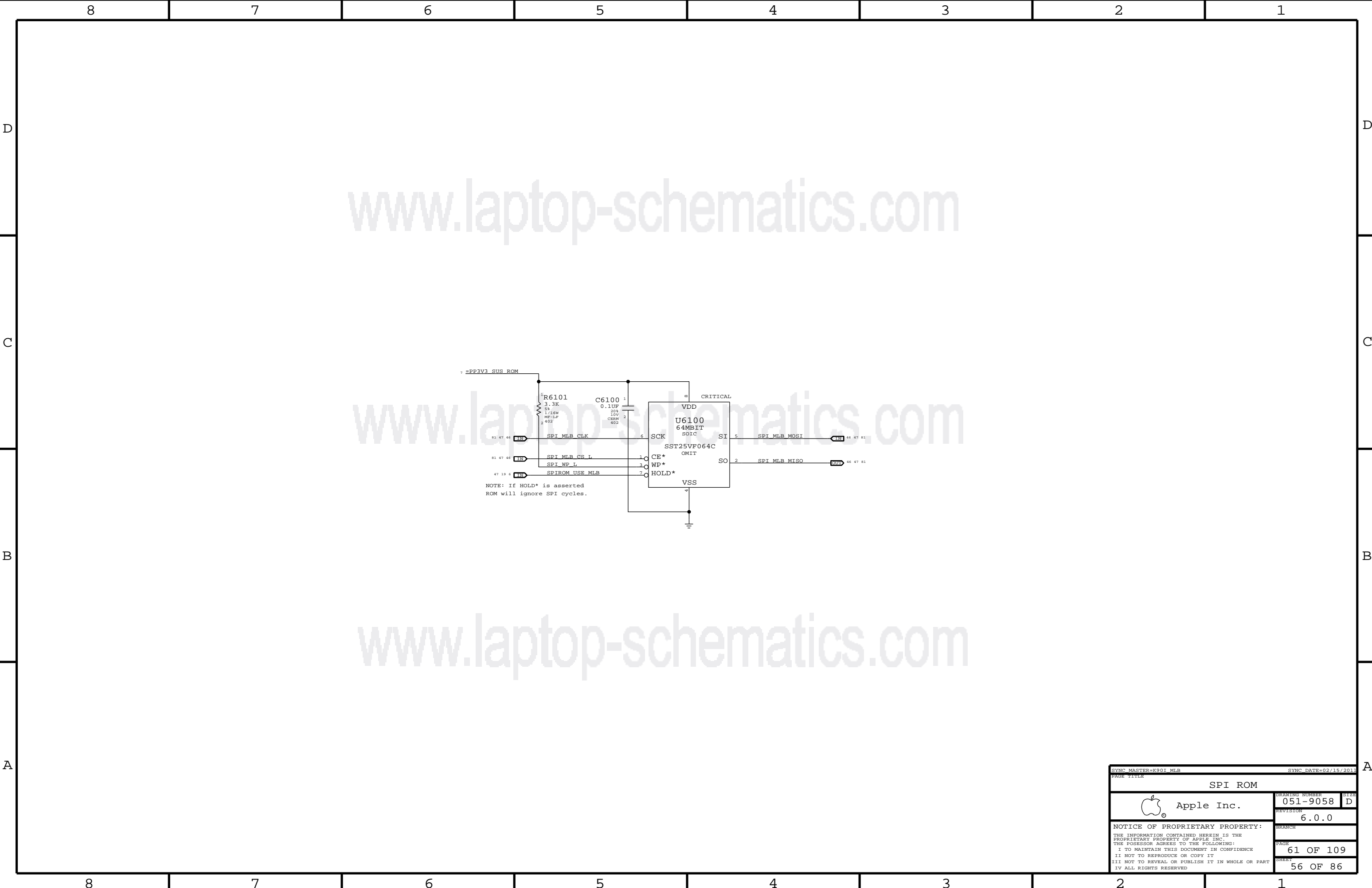
To detect Keyboard backlight, SMC will tristate and read SMC\_SYS\_KBDLED:

If LOW, keyboard backlight present  
If HIGH, keyboard backlight not present

R5853 always stuffed, R5854 only grounded when KB BL flex connected.



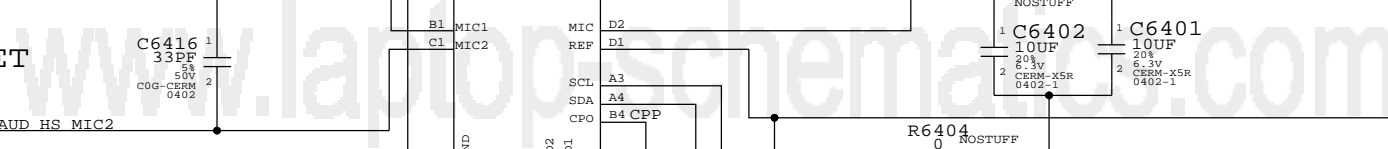









EXTERNAL (HEADSET) MIC INPUT CIRCUITRY APN:353S3066 as o

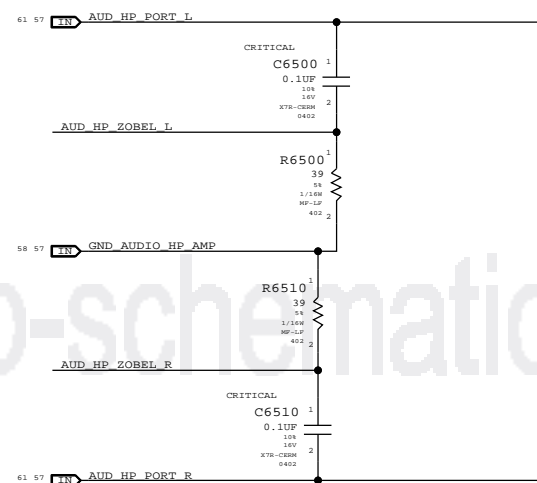



```
SMBus 0 connections
0111 0111 0x77
0111 0110 0x76
```

CHS	U6400	READ	0111	0111	0x77
CHS	U6400	WRITE	0111	0110	0x76



ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



SYNC MASTER-KAVITHA J39		SYNC DATE=07/25/2011	
PAGE TITLE			
AUDIO: HEADPHONE FILTER			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-9058		
	REVISION		
		6.0.0	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		PAGE 65 OF 109	
		SHEET 59 OF 86	

D

C

B

A

D

C

B

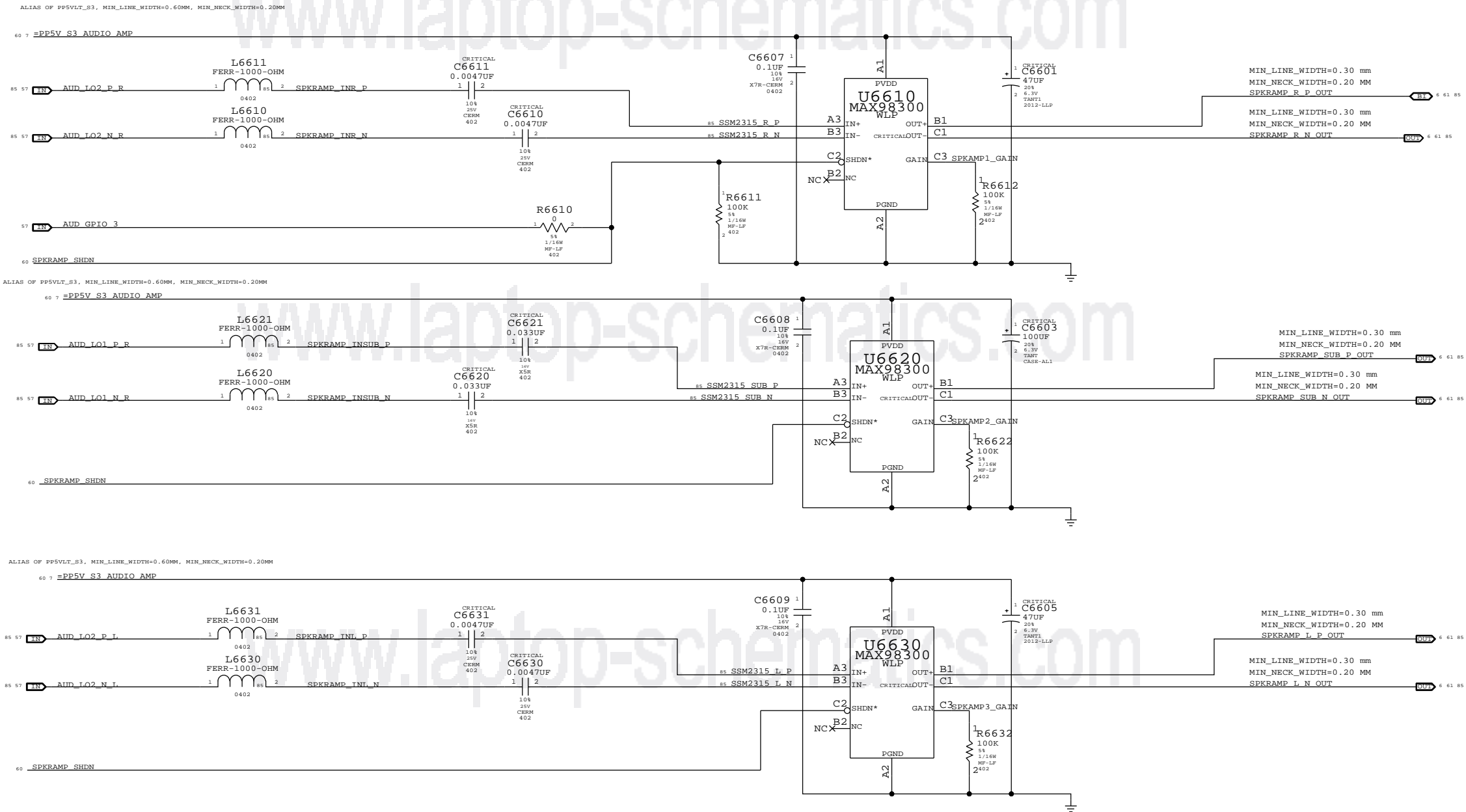
A


SATELLITE & SUB TWEETER AMPLIFIER

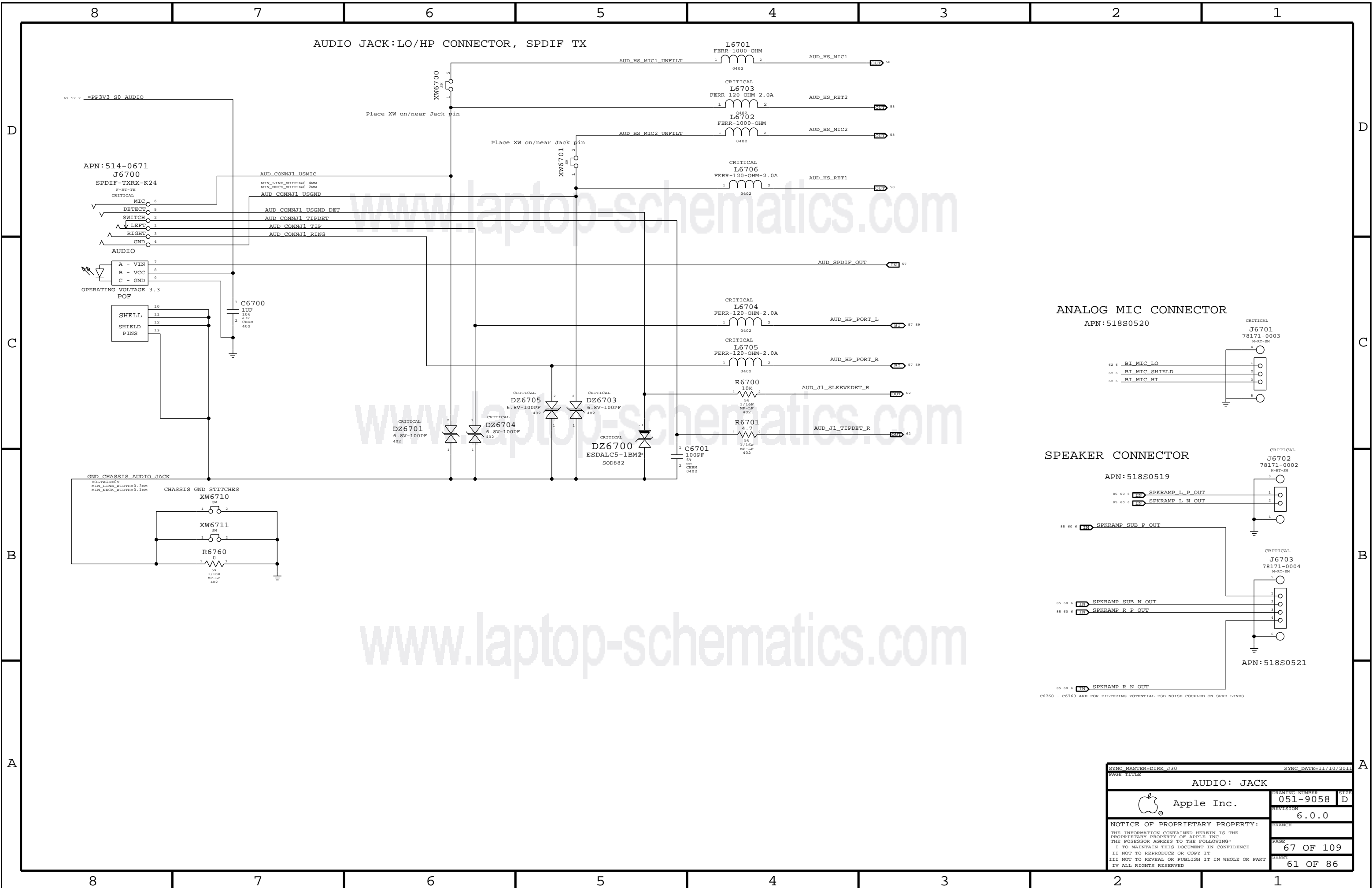
APN:353S2888 as of July 2011

SATELLITE	FC=1.2kHz typical
SUB	FC= 172 HZ typical
GAIN	3DB with Rin=28k typical

Gain Pin	Gain dB
Connect to VDD	12
Connect to VDD through 100k	9
Not connected	6
Connect to GND through 100k	3
Connect to GND	0

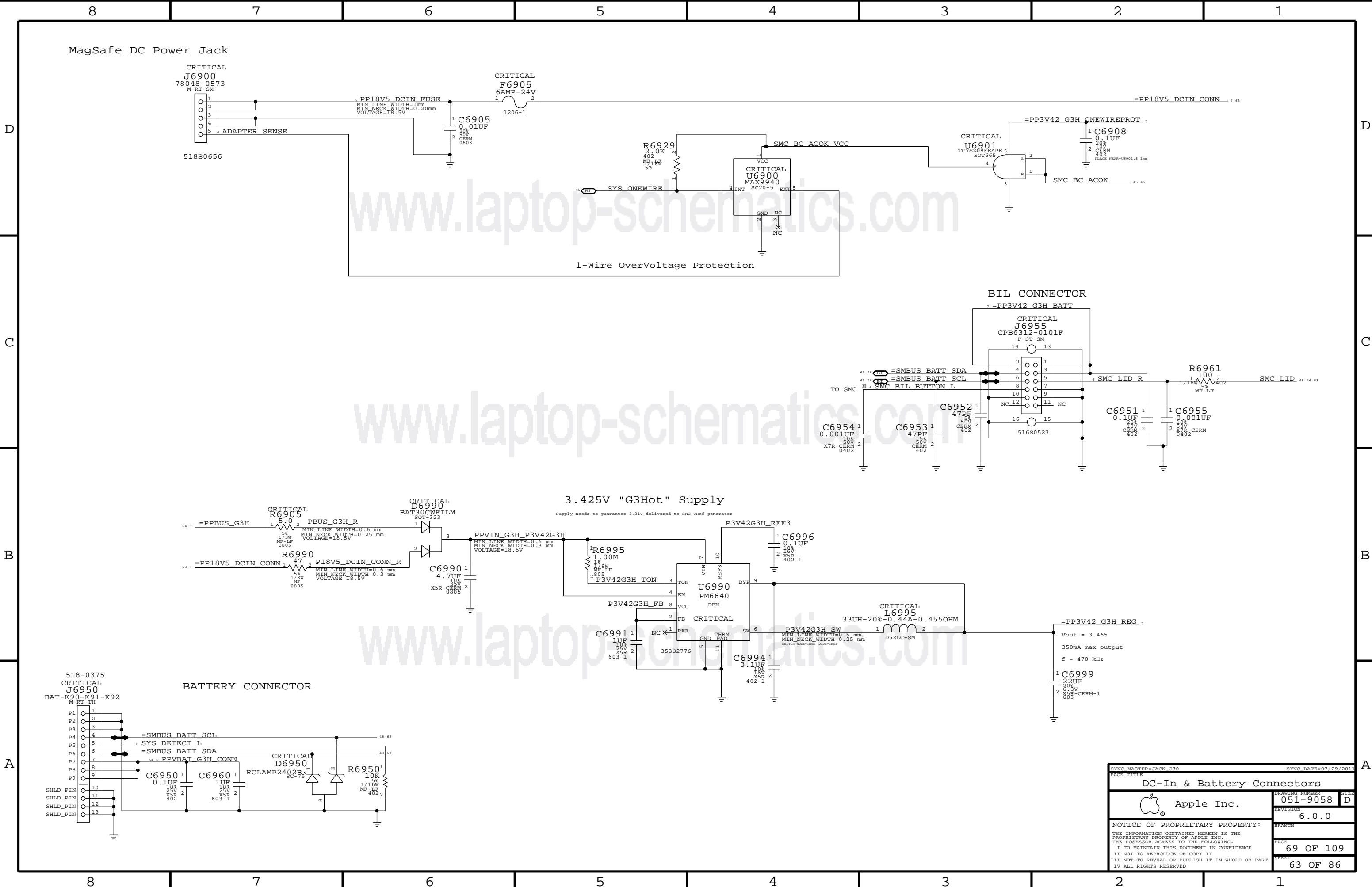


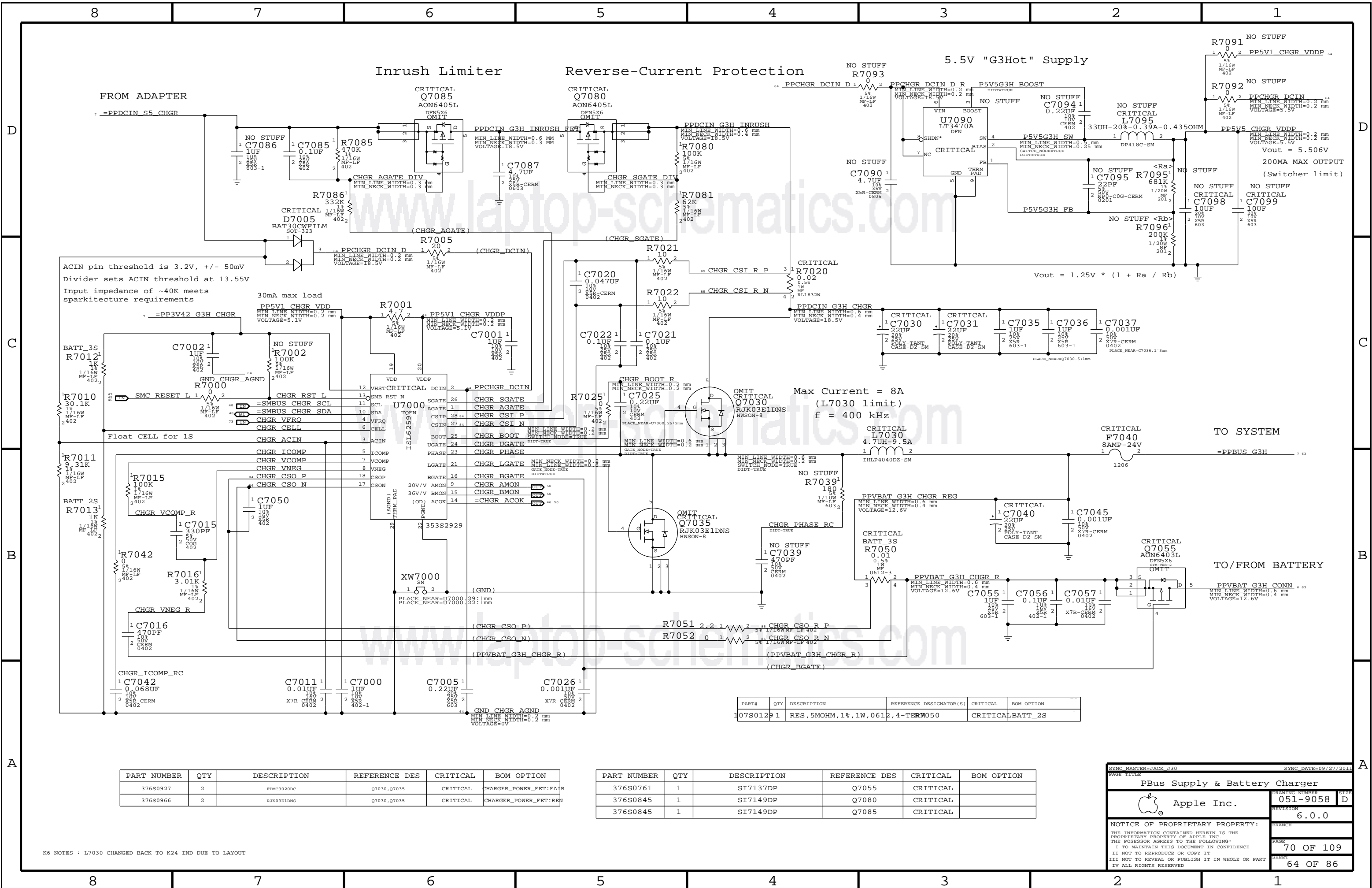
SYNC MASTER=KAVITHA J30		SYNC DATE=07/25/2011	
PAGE TITLE			
AUDIO10: SPEAKER AMP			
	DRAWING NUMBER		SIZE
	051-9058		D
Apple Inc.		REVISION	
		6.0.0	
NOTICE OF PROPRIETARY PROPERTY:			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.			
THE POSSESSOR AGREES TO THE FOLLOWING:			
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			
		BRANCH	
		PAGE	66 OF 109
		SHEET	60 OF 86



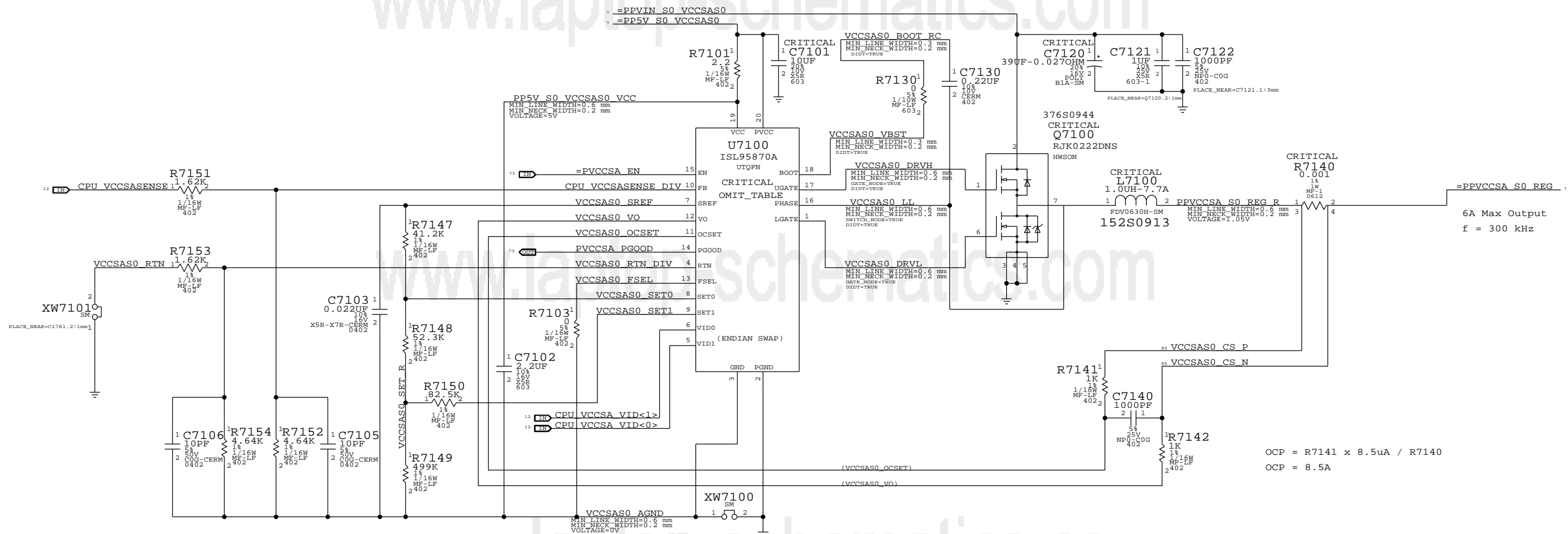









# System Agent Power Supply



INTEL TABLE:		
VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V
0	1	0.725V
1	1	0.675V

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3074	IC	ISL95870A, PWM, 2BIT-VID, RMOT-SNSE, 20V	U7100	CRITICAL	


SYNC MASTER=JACK J30		SYNC DATE=09/28/2011	
PAGE TITLE			
System Agent Supply			
 Apple Inc.		DRAWING NUMBER	051-9058
		SIZE	D
		REVISION	6.0.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		71 OF 109	
II NOT TO REPRODUCE OR COPY IT		SHEET	
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		65 OF 86	
IV ALL RIGHTS RESERVED			

5V\_S3 / 3.3V\_S5 POWER SUPPLY

VOUT = (2 \* RA / RB) + 2

VOUT = (2 \* RC / RD) + 2

www.laptop-schematics.com

SYNC MASTER-JACK J30		SYNC DATE-05/22/2013	
PAGE TITLE			
5V/3.3V SUPPLY			
 Apple Inc.		DRAWING NUMBER	SHEET
		051-9058	D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I. I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II. NOT TO REPRODUCE OR COPY IT III. NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV. ALL RIGHTS RESERVED		REVISION	
		6.0.0	
		BRANCH	
		PAGE	72 OF 109
		SHEET	
		66 OF 86	

D

C

B

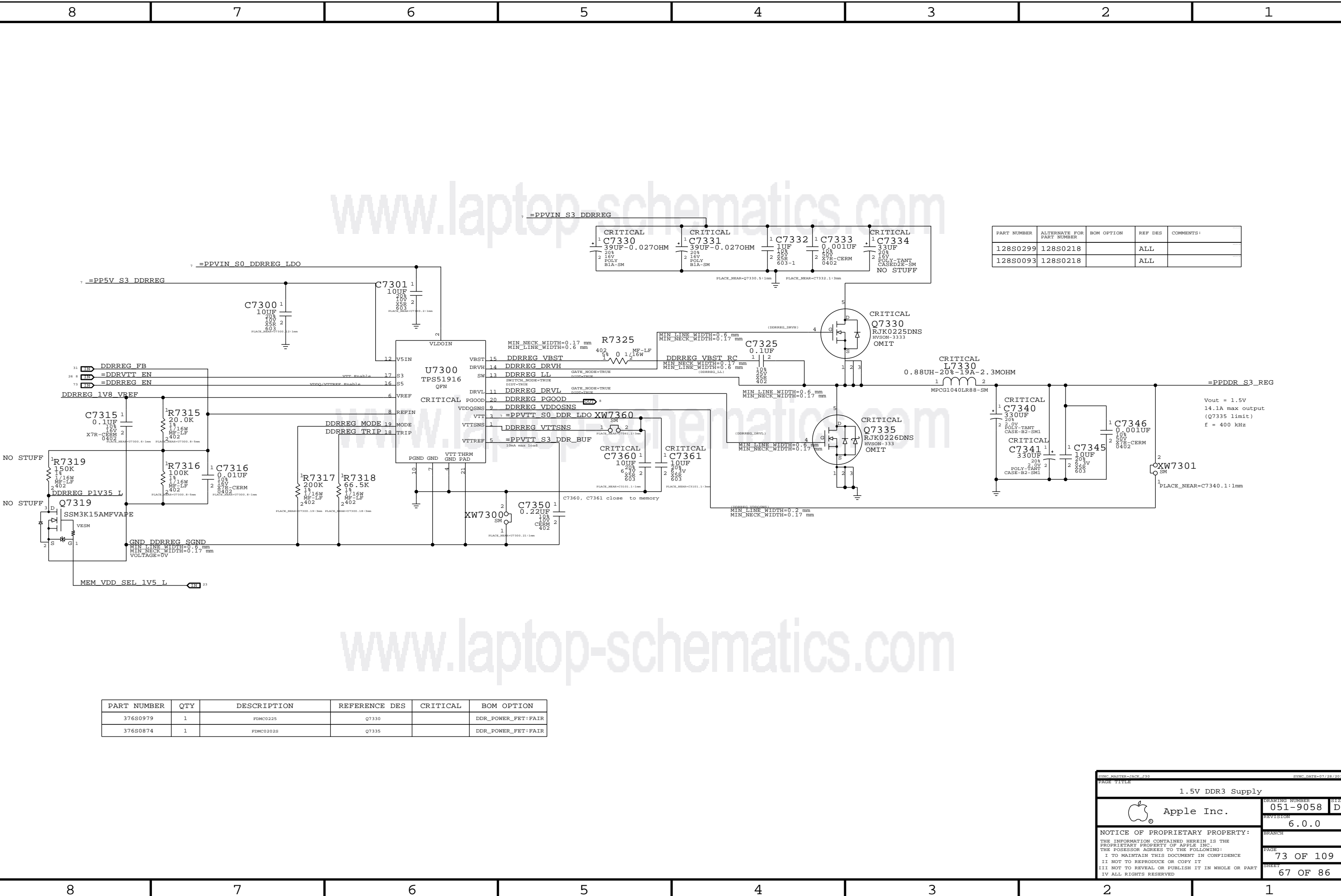
A

D

C

B

A



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0979	1	FDMC0225	Q7330		DDR_POWER_FET:FAIR
376S0874	1	FDMC0202S	Q7335		DDR_POWER_FET:FAIR

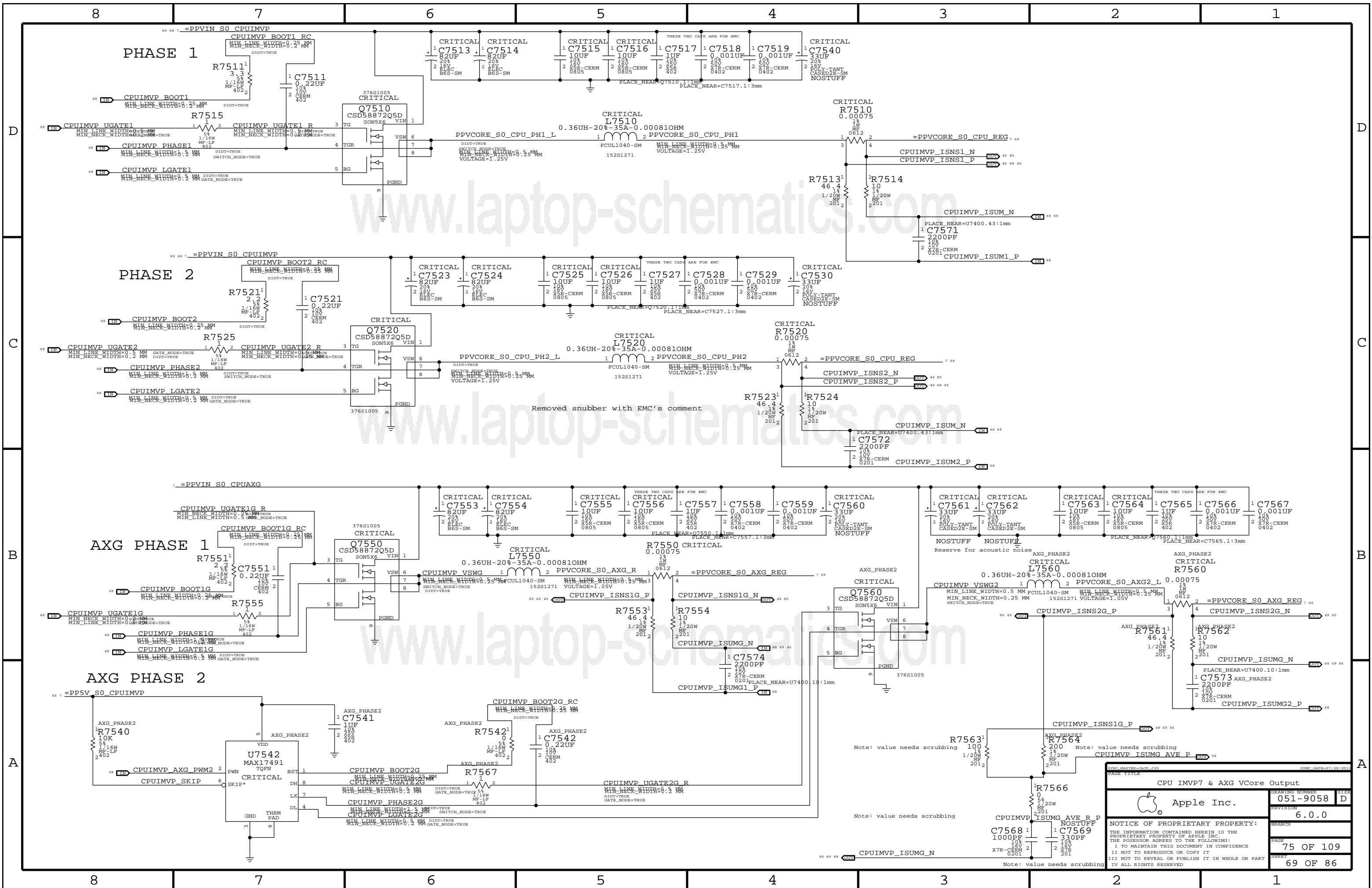
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0299	128S0218		ALL	
128S0093	128S0218		ALL	

Vout = 1.5V  
14.1A max output  
(Q7335 limit)  
f = 400 kHz

SYNCHARTER-JACK-710				SYNCHARTER-JACK-710			
PAGE TITLE				PAGE TITLE			
1.5V DDR3 Supply				1.5V DDR3 Supply			
Apple Inc.				Apple Inc.			
DRAWING NUMBER				DRAWING NUMBER			
051-9058				051-9058			
REVISION				REVISION			
6.0.0				6.0.0			
BRANCH				BRANCH			
PAGE				PAGE			
73 OF 109				73 OF 109			
SHEET				SHEET			
67 OF 86				67 OF 86			

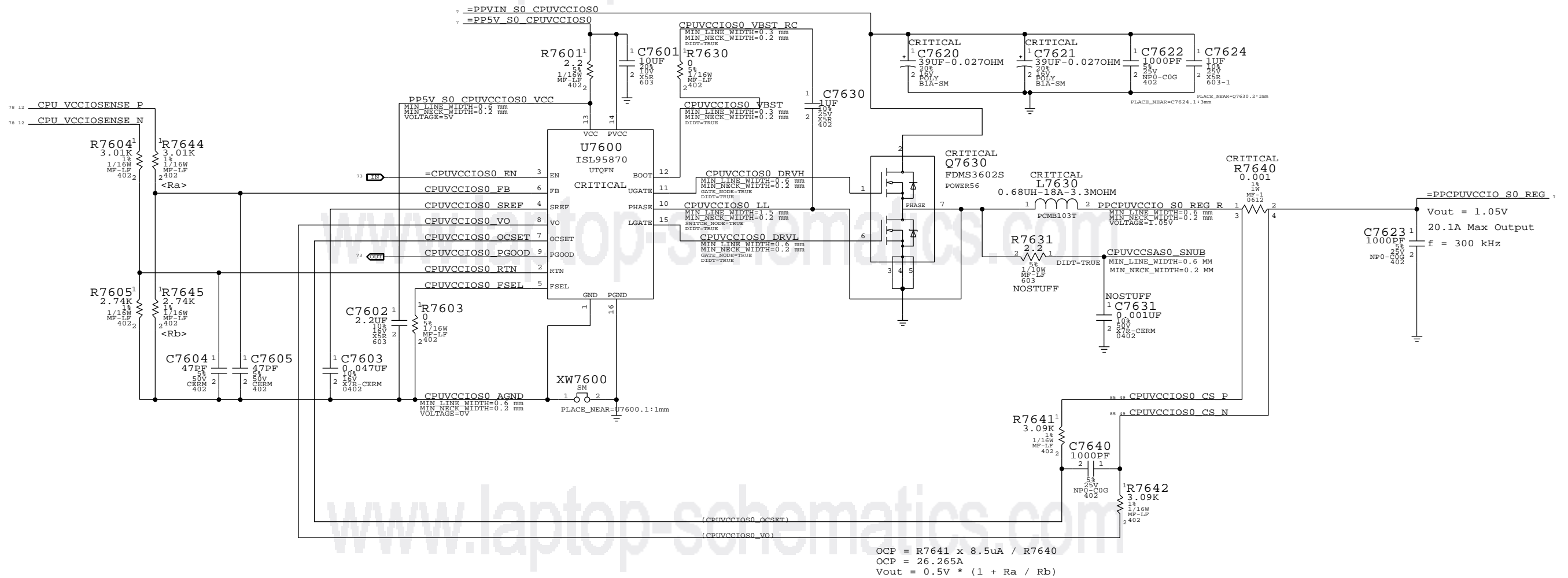







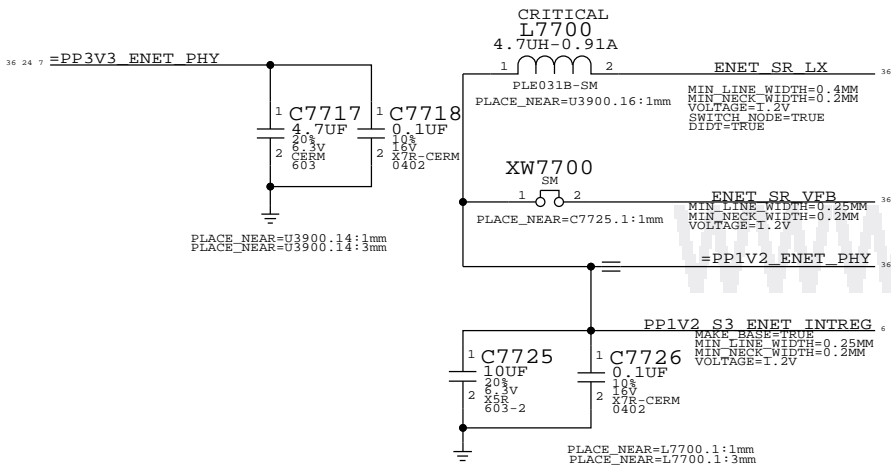
CPU IMVP7 & AXG VCore Output	
Apple Inc.	DRAWING NUMBER 051-9058
REVISION 6.0.0	SIZE D
NOTICE OF PROPRIETARY PROPERTY:	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE	
II NOT TO REPRODUCE OR COPY IT	
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART	
IV ALL RIGHTS RESERVED	
PAGE 75 OF 109	SHEET 69 OF 86

# CPU VCCIO (1.05V S0) Regulator



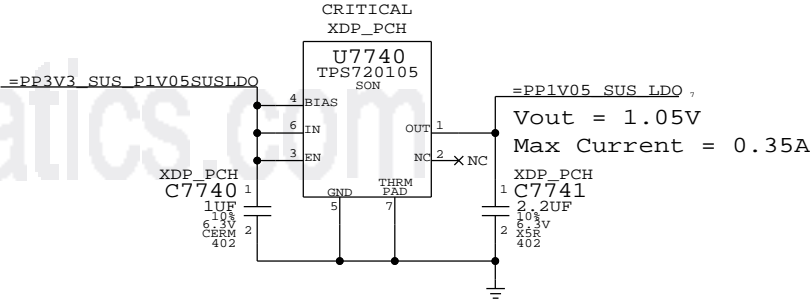
SYNC MASTER=JACK J30		SYNC DATE=09/28/2011	
PAGE TITLE			
CPUVCCIO (1.05V) Power Supply			
 Apple Inc.	DRAWING NUMBER	051-9058	SIZE D
	REVISION	6.0.0	
	BRANCH		
NOTICE OF PROPRIETARY PROPERTY:			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:			
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			
		PAGE	76 OF 109
		SHEET	70 OF 86

CAESAR IV 1.2V INT.VR CMPTS



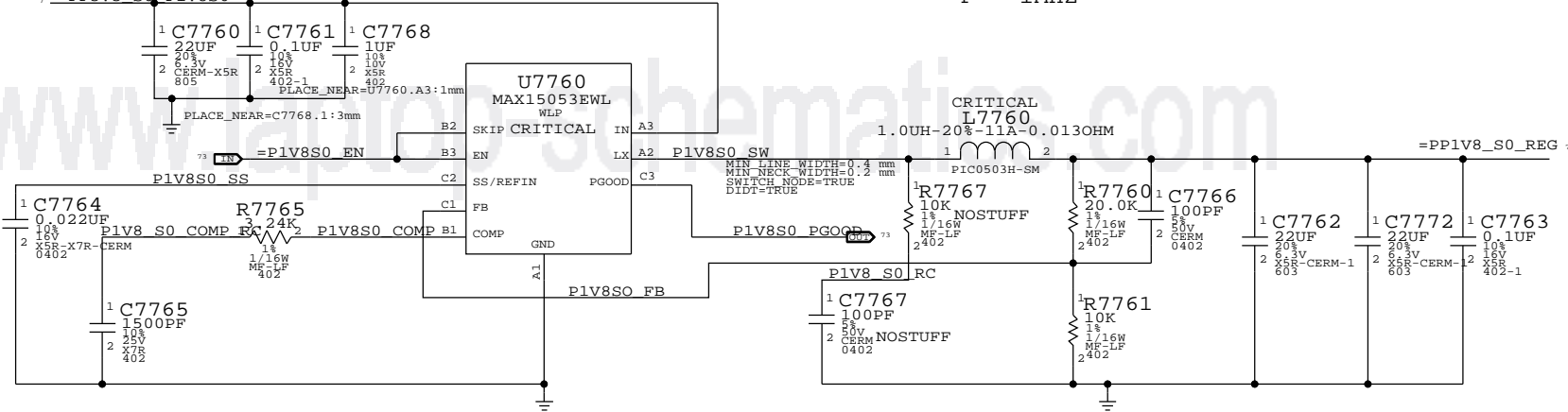
1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V in SUS. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



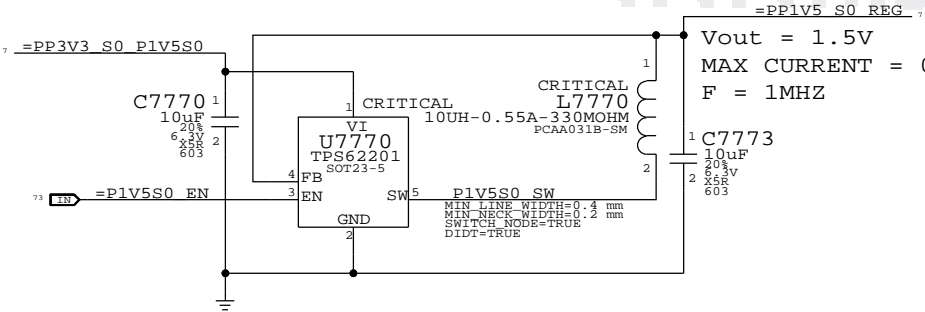
1.8V S0 Switcher

Vout = 1.8V  
MAX CURRENT = 2A  
F = 1MHZ



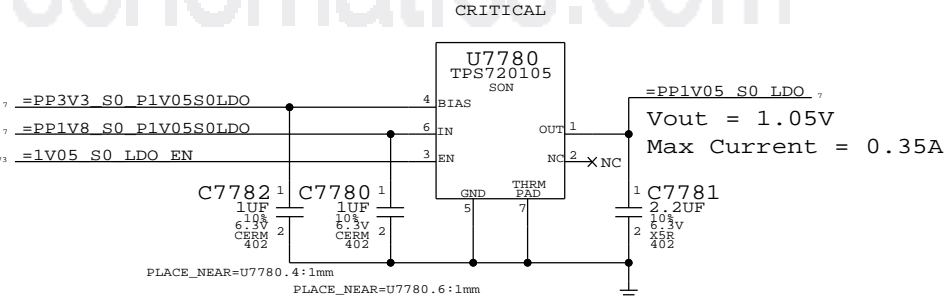
1.5V S0 Switcher


Vout = 1.5V  
MAX CURRENT = 0.3A  
F = 1MHZ

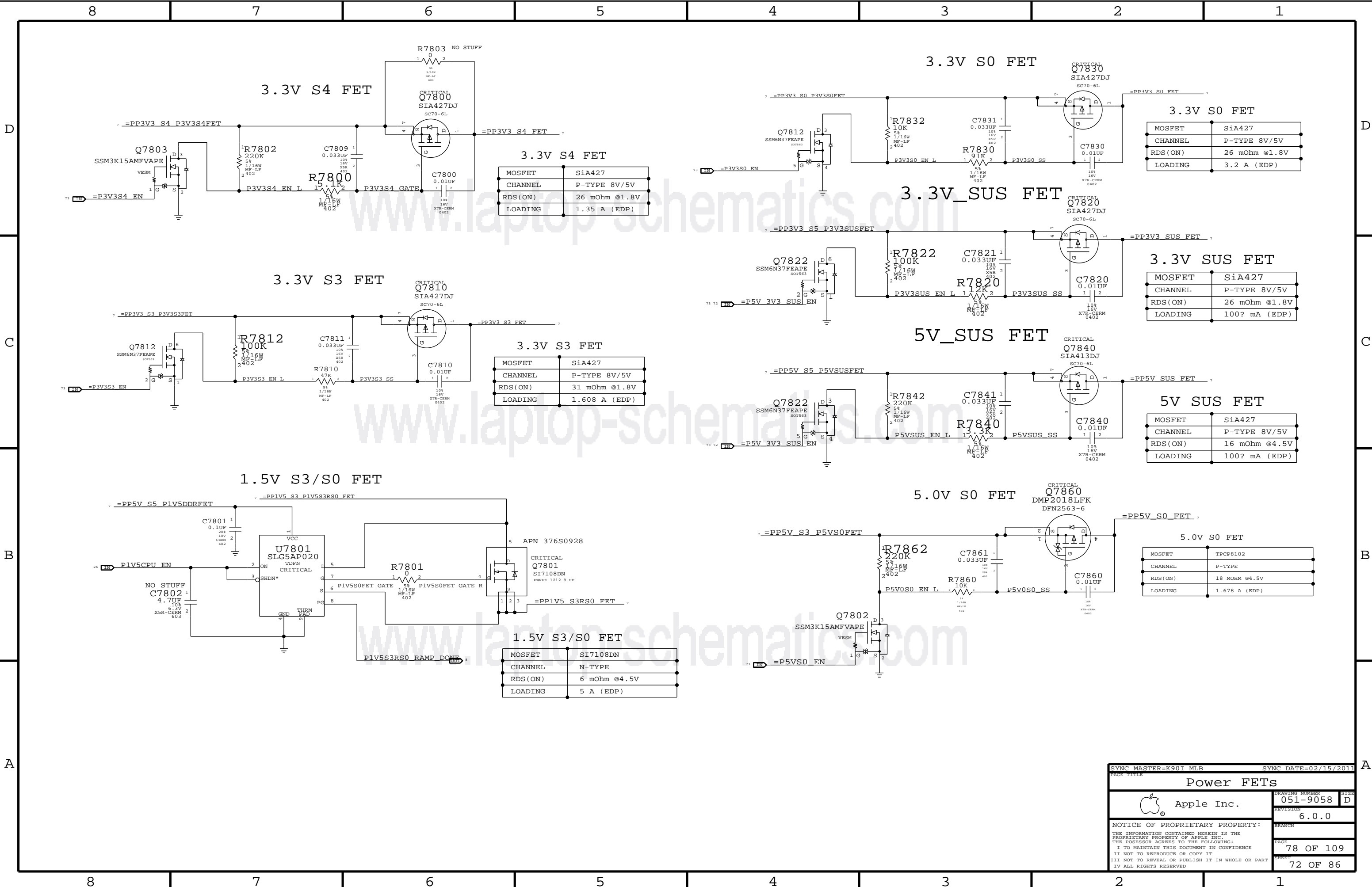


1.05V S0 LDO

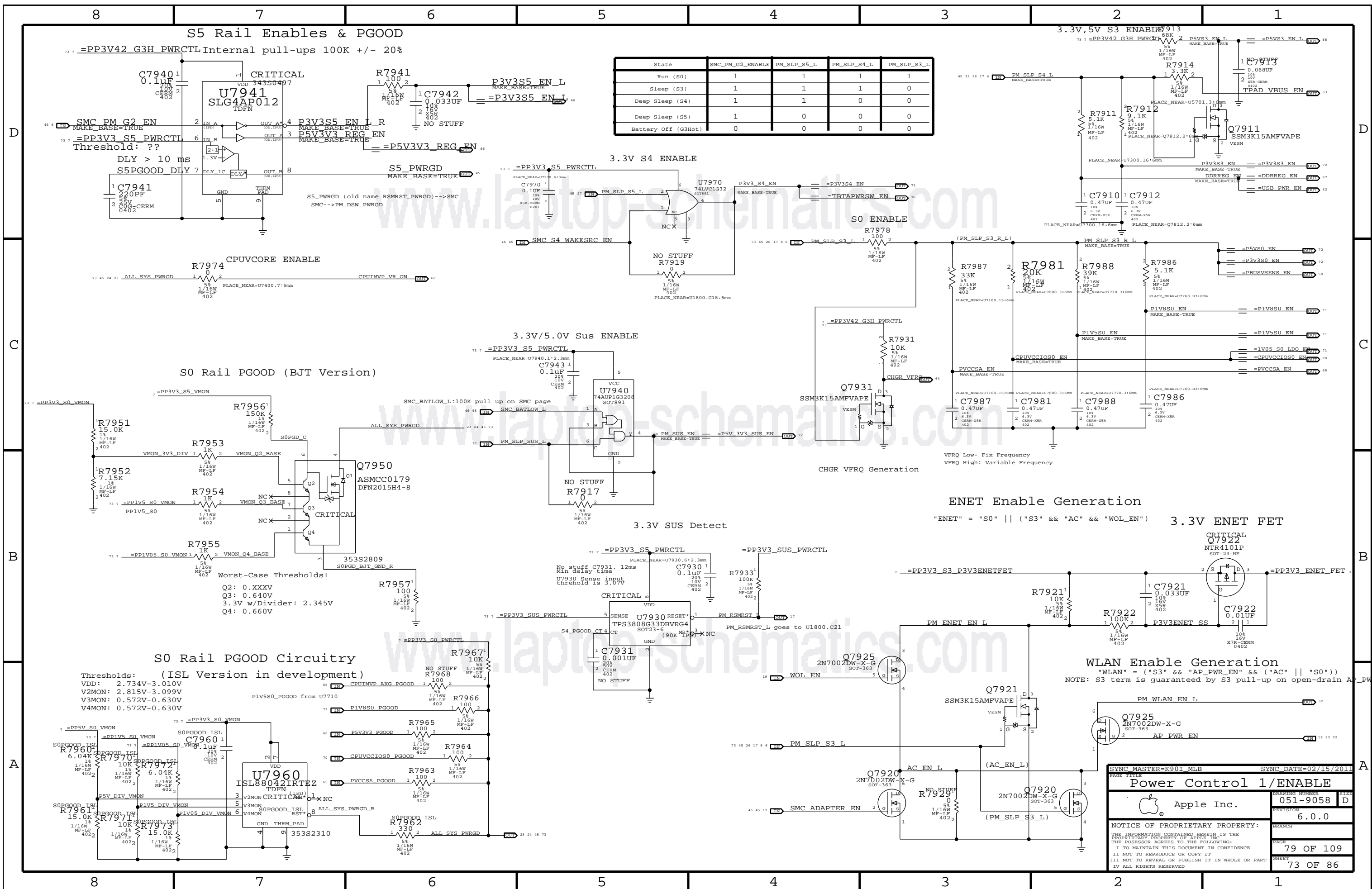
Vout = 1.05V  
Max Current = 0.35A

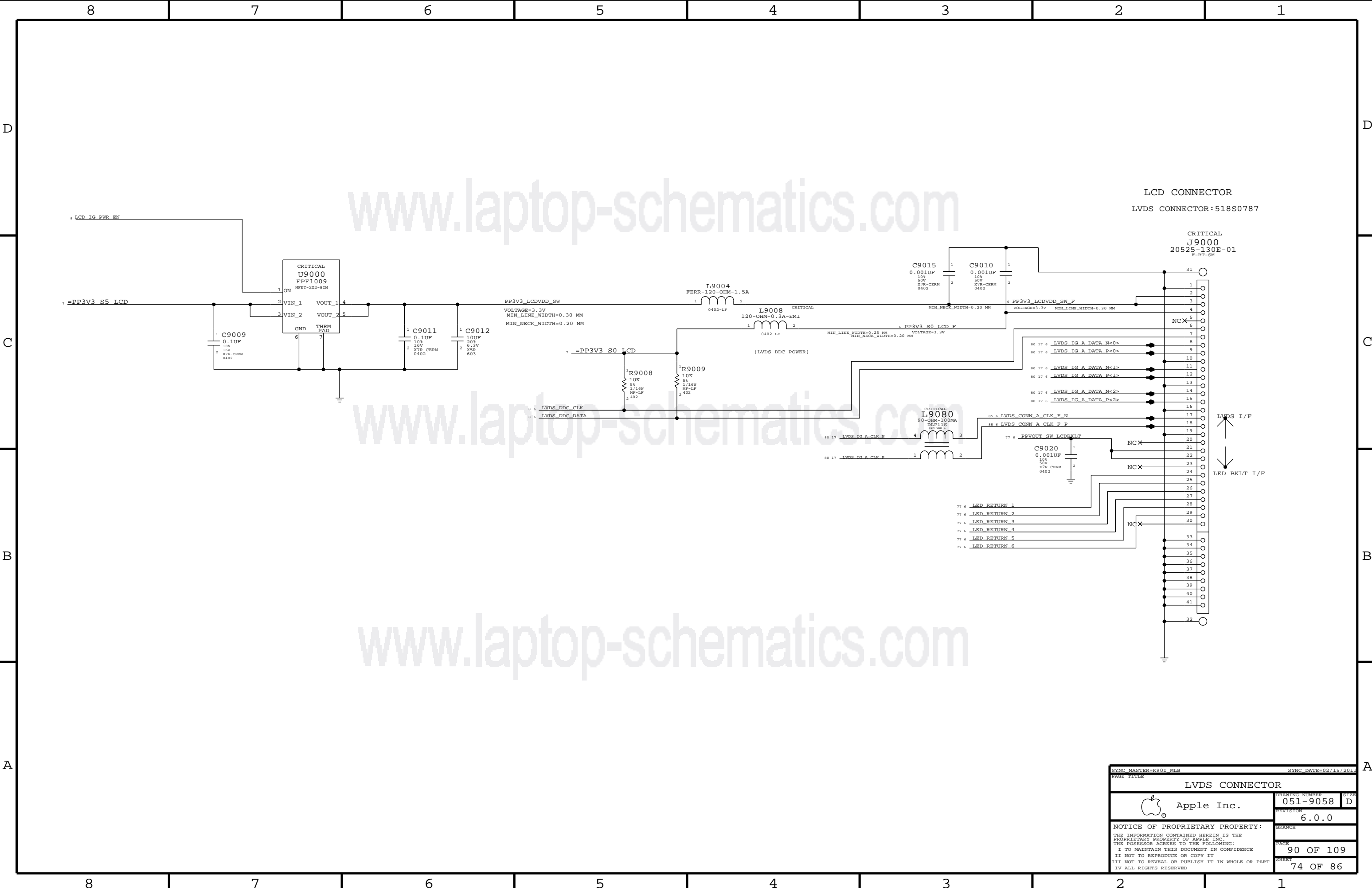



SYNC MASTER=JACK J30		SYNC DATE=07/28/2011	
PAGE TITLE			
Misc Power Supplies			
 Apple Inc.		DRAWING NUMBER	SHEET
		051-9058	D
		REVISION	
		6.0.0	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		77	OF 109
II NOT TO REPRODUCE OR COPY IT		SHEET	
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		71	OF 86
IV ALL RIGHTS RESERVED			

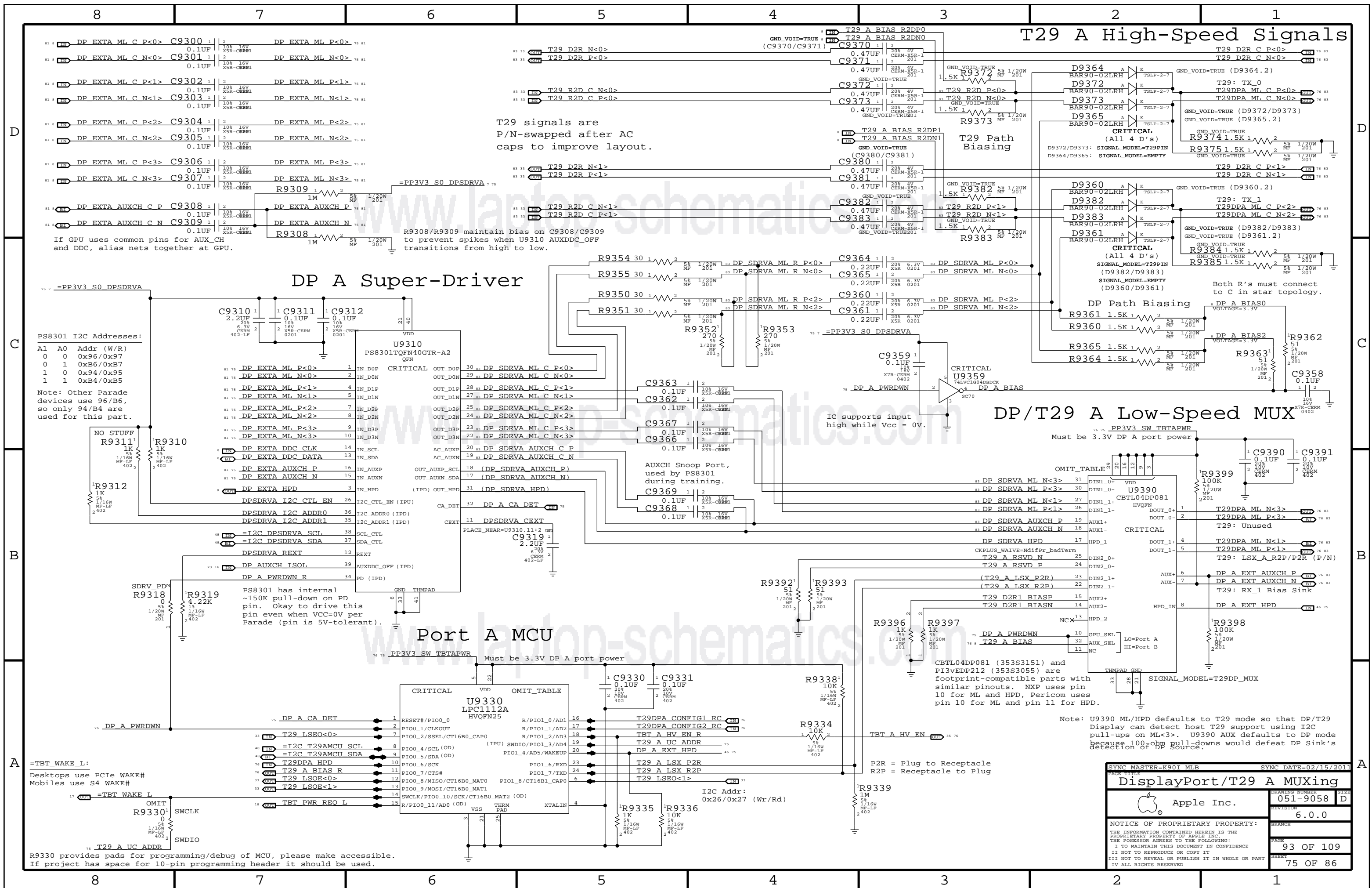








SYNC MASTER=K901 MLB		SYNC DATE=02/15/2011	
PAGE TITLE			
LVDS CONNECTOR			
 Apple Inc.		DRAWING NUMBER	051-9058
		SIZE	D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		REVISION	6.0.0
		BRANCH	
		PAGE	90 OF 109
		SHEET	74 OF 86



8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

D

BA

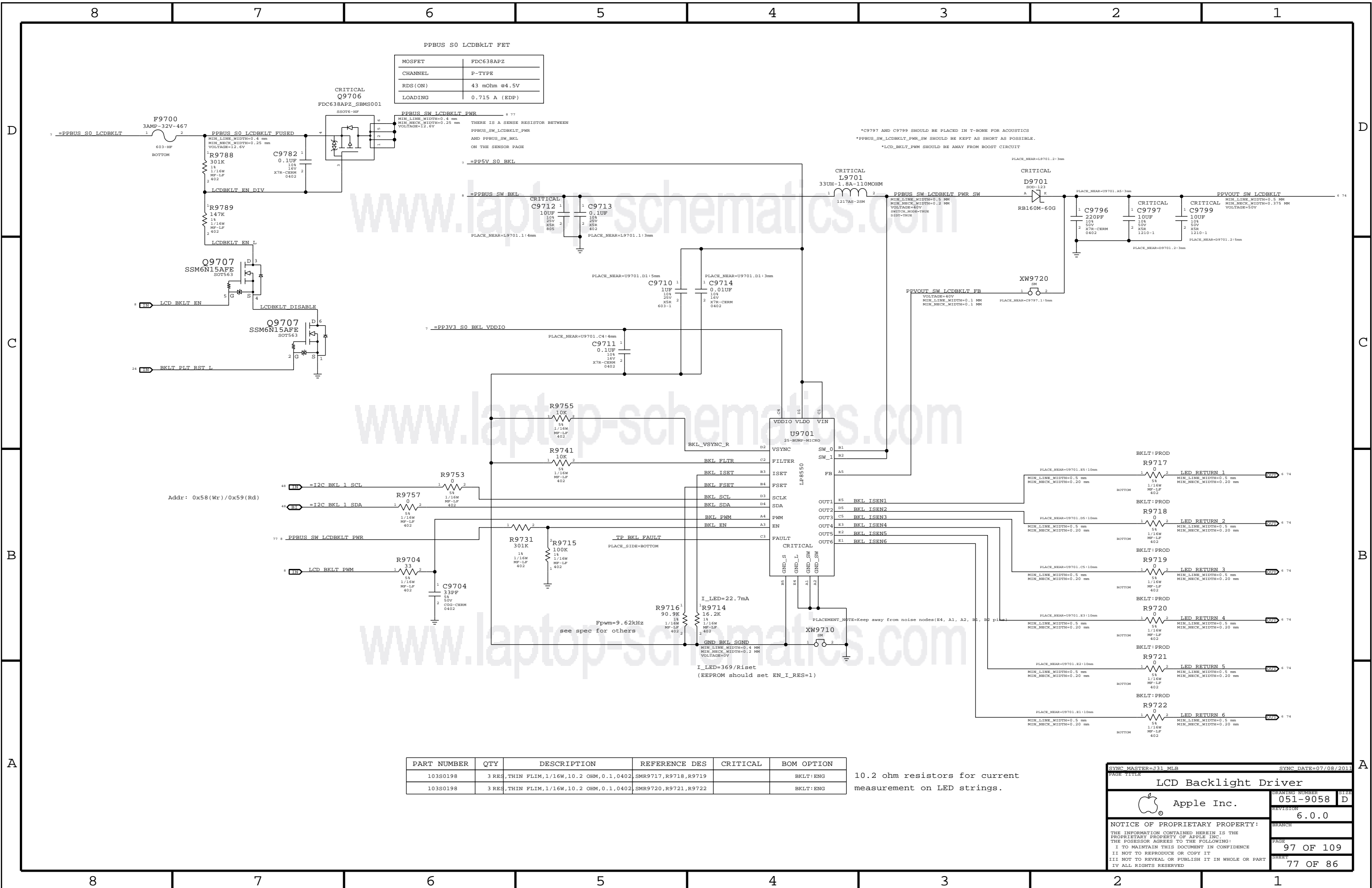
## D



B

A





PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3 RES	THIN FLIM, 1/16W, 10.2 OHM, 0.1, 0402	SMR9717, R9718, R9719		BKLT:ENG
103S0198	3 RES	THIN FLIM, 1/16W, 10.2 OHM, 0.1, 0402	SMR9720, R9721, R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC MASTER=J31 MLR		SYNC DATE=07/08/2011	
PAGE TITLE			
LCD Backlight Driver			
DRAWING NUMBER		SIZE	
051-9058		D	
REVISION		BRANCH	
6.0.0			
NOTICE OF PROPRIETARY PROPERTY:			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:			
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			
PAGE		SHEET	
97 OF 109		77 OF 86	





PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	TOP, BOTTOM	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	TOP, BOTTOM	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
MEM_50S	ISL10	N	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	ISL10	N	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
MEM_50S	ISL3, ISL4, ISL9	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	ISL3, ISL4, ISL9	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM\*-style wildcards!

DDR3: Sandybridge SFF 2C when routed on Type-3 (Through hole) should follow rPGA guidelines per Huron River SFF DG rev1.0 (#438297).

DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.

DQ to DQS matching per byte lane should be within 0.127mm.

DQS to clock matching should be within [CLK-63.5mm] and [CLK+38.1mm].

CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.0508mm.

CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0.0mm] of CLK pairs.

A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs A/BA/CMD signals to each other should match within 5.08mm.

DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.

Maximum length of any signal from die pad to SODIMM pad is 119.83mm, from procesor ball to SODIMM pad is 88.9mm.

SOURCE: Huron River Platform DG, Rev 1.01 (#436735), Section 2.5

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM A CLK	MEM_72D	MEM_CLK	MEM A CLK P<5..0>	11 27
MEM A CLK	MEM_72D	MEM_CLK	MEM A CLK N<5..0>	11 27
MEM A CMT	MEM_37S	MEM_CTRL	MEM A CKE<3..0>	11 27
MEM A CMT	MEM_37S	MEM_CTRL	MEM A CS L<3..0>	11 27
MEM A CMT	MEM_37S	MEM_CTRL	MEM A ODT<3..0>	11 27
MEM A CMD	MEM_40S	MEM_CMD	MEM A A<15..0>	11 27
MEM A CMD	MEM_40S	MEM_CMD	MEM A BA<2..0>	11 27
MEM A CMD	MEM_40S	MEM_CMD	MEM A RAS L	11 27
MEM A CMD	MEM_40S	MEM_CMD	MEM A CAS L	11 27
MEM A CMD	MEM_40S	MEM_CMD	MEM A WE L	11 27
MEM A DQ BYTE0	MEM_50S	MEM_DATA	MEM A DQ<7..0>	11 28
MEM A DQ BYTE1	MEM_50S	MEM_DATA	MEM A DQ<15..8>	11 28
MEM A DQ BYTE2	MEM_50S	MEM_DATA	MEM A DQ<23..16>	11 28
MEM A DQ BYTE3	MEM_50S	MEM_DATA	MEM A DQ<31..24>	11 28
MEM A DQ BYTE4	MEM_50S	MEM_DATA	MEM A DQ<39..32>	11 28
MEM A DQ BYTE5	MEM_50S	MEM_DATA	MEM A DQ<47..40>	11 28
MEM A DQ BYTE6	MEM_50S	MEM_DATA	MEM A DQ<55..48>	11 28
MEM A DQ BYTE7	MEM_50S	MEM_DATA	MEM A DQ<63..56>	11 28
MEM A DQS0	MEM_85D	MEM_DQS	MEM A DQS P<0>	11 28
MEM A DQS0	MEM_85D	MEM_DQS	MEM A DQS N<0>	11 28
MEM A DQS1	MEM_85D	MEM_DQS	MEM A DQS P<1>	11 28
MEM A DQS1	MEM_85D	MEM_DQS	MEM A DQS N<1>	11 28
MEM A DQS2	MEM_85D	MEM_DQS	MEM A DQS P<2>	11 28
MEM A DQS2	MEM_85D	MEM_DQS	MEM A DQS N<2>	11 28
MEM A DQS3	MEM_85D	MEM_DQS	MEM A DQS P<3>	11 28
MEM A DQS3	MEM_85D	MEM_DQS	MEM A DQS N<3>	11 28
MEM A DQS4	MEM_85D	MEM_DQS	MEM A DQS P<4>	11 28
MEM A DQS4	MEM_85D	MEM_DQS	MEM A DQS N<4>	11 28
MEM A DQS5	MEM_85D	MEM_DQS	MEM A DQS P<5>	11 28
MEM A DQS5	MEM_85D	MEM_DQS	MEM A DQS N<5>	11 28
MEM A DQS6	MEM_85D	MEM_DQS	MEM A DQS P<6>	11 28
MEM A DQS6	MEM_85D	MEM_DQS	MEM A DQS N<6>	11 28
MEM A DQS7	MEM_85D	MEM_DQS	MEM A DQS P<7>	11 28
MEM A DQS7	MEM_85D	MEM_DQS	MEM A DQS N<7>	11 28
MEM B CLK	MEM_72D	MEM_CLK	MEM B CLK P<5..0>	11 29
MEM B CLK	MEM_72D	MEM_CLK	MEM B CLK N<5..0>	11 29
MEM B CMT	MEM_37S	MEM_CTRL	MEM B CKE<3..0>	11 29
MEM B CMT	MEM_37S	MEM_CTRL	MEM B CS L<3..0>	11 29
MEM B CMT	MEM_37S	MEM_CTRL	MEM B ODT<3..0>	11 29
MEM B CMD	MEM_40S	MEM_CMD	MEM B A<15..0>	11 29
MEM B CMD	MEM_40S	MEM_CMD	MEM B BA<2..0>	11 29
MEM B CMD	MEM_40S	MEM_CMD	MEM B RAS L	11 29
MEM B CMD	MEM_40S	MEM_CMD	MEM B CAS L	11 29
MEM B CMD	MEM_40S	MEM_CMD	MEM B WE L	11 29
MEM B DQ BYTE0	MEM_50S	MEM_DATA	MEM B DQ<7..0>	11 28
MEM B DQ BYTE1	MEM_50S	MEM_DATA	MEM B DQ<15..8>	11 28
MEM B DQ BYTE2	MEM_50S	MEM_DATA	MEM B DQ<23..16>	11 28
MEM B DQ BYTE3	MEM_50S	MEM_DATA	MEM B DQ<31..24>	11 28
MEM B DQ BYTE4	MEM_50S	MEM_DATA	MEM B DQ<39..32>	11 28
MEM B DQ BYTE5	MEM_50S	MEM_DATA	MEM B DQ<47..40>	11 28
MEM B DQ BYTE6	MEM_50S	MEM_DATA	MEM B DQ<55..48>	11 28
MEM B DQ BYTE7	MEM_50S	MEM_DATA	MEM B DQ<63..56>	11 28
MEM B DQS0	MEM_85D	MEM_DQS	MEM B DQS P<0>	11 28
MEM B DQS0	MEM_85D	MEM_DQS	MEM B DQS N<0>	11 28
MEM B DQS1	MEM_85D	MEM_DQS	MEM B DQS P<1>	11 28
MEM B DQS1	MEM_85D	MEM_DQS	MEM B DQS N<1>	11 28
MEM B DQS2	MEM_85D	MEM_DQS	MEM B DQS P<2>	11 28
MEM B DQS2	MEM_85D	MEM_DQS	MEM B DQS N<2>	11 28
MEM B DQS3	MEM_85D	MEM_DQS	MEM B DQS P<3>	11 28
MEM B DQS3	MEM_85D	MEM_DQS	MEM B DQS N<3>	11 28
MEM B DQS4	MEM_85D	MEM_DQS	MEM B DQS P<4>	11 28
MEM B DQS4	MEM_85D	MEM_DQS	MEM B DQS N<4>	11 28
MEM B DQS5	MEM_85D	MEM_DQS	MEM B DQS P<5>	11 28
MEM B DQS5	MEM_85D	MEM_DQS	MEM B DQS N<5>	11 28
MEM B DQS6	MEM_85D	MEM_DQS	MEM B DQS P<6>	11 28
MEM B DQS6	MEM_85D	MEM_DQS	MEM B DQS N<6>	11 28
MEM B DQS7	MEM_85D	MEM_DQS	MEM B DQS P<7>	11 28
MEM B DQS7	MEM_85D	MEM_DQS	MEM B DQS N<7>	11 28

## Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFFAIR PRIMARY GAP	DIFFFAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_PCH	*	=3x_DIELECTRIC	?	DP_PCH	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_PCH_TX	*	=3x_DIELECTRIC	?	DP_PCH_TX	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS_PCH_TX	*	=3x_DIELECTRIC	?	LVDS_PCH_TX	TOP,BOTTOM	=4x_DIELECTRIC	?

## SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_PCH_TX	*	=3x_DIELECTRIC	?
SATA_PCH_RX	*	=3x_DIELECTRIC	?
SATA_ICOMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA3_PCH_TX2TX	*	=4X_DIELECTRIC	?	SATA3_PCH_TX2TX	TOP, BOTTOM	=5X_DIELECTRIC	?
SATA3_PCH_TX2RX	*	=5X_DIELECTRIC	?	SATA3_PCH_TX2RX	TOP, BOTTOM	=6X_DIELECTRIC	?
SATA3_PCH_RX2RX	*	=4x_DIELECTRIC	?	SATA3_PCH_RX2RX	TOP, BOTTOM	=5x_DIELECTRIC	?
SATA3_PCH_RX2TX	*	=5x_DIELECTRIC	?	SATA3_PCH_RX2TX	TOP, BOTTOM	=6x_DIELECTRIC	?
SATA3_PCH_20THER	*	=4x_DIELECTRIC	?	SATA3_PCH_20THER	TOP, BOTTOM	=5x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA3_PCH_TX	*_PCH_TX	*	SATA3_PCH_TX2TX
SATA3_PCH_TX	*_PCH_RX	*	SATA3_PCH_TX2RX
SATA3_PCH_RX	*_PCH_RX	*	SATA3_PCH_RX2RX
SATA3_PCH_RX	*_PCH_TX	*	SATA3_PCH_RX2TX
SATA3_PCH_TX	*	*	SATA3_PCH_2OTHER
SATA3_PCH_RX	*	*	SATA3_PCH_2OTHER

SOURCE: 471984\_Cheif\_River\_MS\_PDG\_1.0 and the spacing rule is adjusted per SI team feedback.

## USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?	USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905\_v1.5), Section 3.8

## USB 3.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF


SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_PCH_TX2TX	*	=4X_DIELECTRIC	?	USB3_PCH_TX2TX	TOP, BOTTOM	=5X_DIELECTRIC	?
USB3_PCH_TX2RX	*	=5X_DIELECTRIC	?	USB3_PCH_TX2RX	TOP, BOTTOM	=6X_DIELECTRIC	?
USB3_PCH_RX2RX	*	=4x_DIELECTRIC	?	USB3_PCH_RX2RX	TOP, BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_RX2TX	*	=5x_DIELECTRIC	?	USB3_PCH_RX2TX	TOP, BOTTOM	=6x_DIELECTRIC	?
USB3_PCH_2OTHER	*	=4x_DIELECTRIC	?	USB3_PCH_2OTHER	TOP, BOTTOM	=5x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_PCH_TX	*_PCH_TX	*	USB3_PCH_TX2TX
USB3_PCH_TX	*_PCH_RX	*	USB3_PCH_TX2RX
USB3_PCH_RX	*_PCH_RX	*	USB3_PCH_RX2RX
USB3_PCH_RX	*_PCH_TX	*	USB3_PCH_RX2TX
USB3_PCH_TX	*	*	USB3_PCH_2OTHER
USB3_PCH_RX	*	*	USB3_PCH_2OTHER

SOURCE: 471984\_Cheif\_River\_MS\_PDG\_1.0 and the spacing rule is adjusted per SI team feedback.

## PCH Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
LVDS_IG_A_CLK	LVDS_90D	LVDS_RCH_TX	LVDS_IG_A_CLK_P	17 74
LVDS_IG_A_CLK	LVDS_90D	LVDS_RCH_TX	LVDS_IG_A_CLK_N	17 74
LVDS_IG_A_DATA	LVDS_90D	LVDS_RCH_TX	LVDS_IG_A_DATA_P<2..0>	6 17 74
LVDS_IG_A_DATA	LVDS_90D	LVDS_RCH_TX	LVDS_IG_A_DATA_N<2..0>	6 17 74
	LVDS_90D	LVDS_RCH_TX	LVDS_IG_A_DATA_P<3>	8 17
	LVDS_90D	LVDS_RCH_TX	LVDS_IG_A_DATA_N<3>	8 17
	LVDS_90D	LVDS_RCH_TX	LVDS_IG_B_DATA_P<3..0>	8 17
	LVDS_90D	LVDS_RCH_TX	LVDS_IG_B_DATA_N<3..0>	8 17
	LVDS_90D	LVDS_RCH_TX	LVDS_IG_B_CLK_P	8 17
	LVDS_90D	LVDS_RCH_TX	LVDS_IG_B_CLK_N	8 17
SATA_HDD_R2D	SATA_90D	SATA3_RCH_TX	SATA_HDD_R2D_C_P	16 41
SATA_HDD_R2D	SATA_90D	SATA3_RCH_TX	SATA_HDD_R2D_C_N	16 41
SATA_HDD_R2D_CONN	SATA_90D	SATA3_RCH_TX	SATA_HDD_R2D_P	6 41
SATA_HDD_R2D_CONN	SATA_90D	SATA3_RCH_TX	SATA_HDD_R2D_N	6 41
SATA_HDD_D2R	SATA_90D	SATA3_RCH_RX	SATA_HDD_D2R_P	16 41
SATA_HDD_D2R	SATA_90D	SATA3_RCH_RX	SATA_HDD_D2R_N	16 41
SATA_HDD_D2R_CONN	SATA_90D	SATA3_RCH_RX	SATA_HDD_D2R_C_P	6 41
SATA_HDD_D2R_CONN	SATA_90D	SATA3_RCH_RX	SATA_HDD_D2R_C_N	6 41
SATA_ODD_R2D	SATA_90D	SATA_RCH_TX	SATA_ODD_R2D_C_P	16 41
SATA_ODD_R2D	SATA_90D	SATA_RCH_TX	SATA_ODD_R2D_C_N	16 41
SATA_ODD_R2D	SATA_90D	SATA_RCH_TX	SATA_ODD_R2D_P	6 41
SATA_ODD_R2D	SATA_90D	SATA_RCH_TX	SATA_ODD_R2D_N	6 41
SATA_ODD_D2R	SATA_90D	SATA_RCH_RX	SATA_ODD_D2R_P	16 41
SATA_ODD_D2R	SATA_90D	SATA_RCH_RX	SATA_ODD_D2R_N	16 41
SATA_HDD_R2D_CONN	SATA_90D	SATA3_RCH_TX	SATA_HDD_R2D_RC_P	41
SATA_HDD_R2D_CONN	SATA_90D	SATA3_RCH_TX	SATA_HDD_R2D_RC_N	41
SATA_HDD_D2R_CONN	SATA_90D	SATA3_RCH_RX	SATA_HDD_D2R_RC_P	41
SATA_HDD_D2R_CONN	SATA_90D	SATA3_RCH_RX	SATA_HDD_D2R_RC_N	41
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP	16
USB_HUB1_UP	USB_85D	USB	USB_HUB_UP_P	16 25
USB_HUB1_UP	USB_85D	USB	USB_HUB_UP_N	16 25
USB_EXTA	USB_85D	USB	USB_EXTA_P	16 42
USB_EXTA	USB_85D	USB	USB_EXTA_N	16 42
USB_EXTB	USB_85D	USB	USB_EXTB_MUX_P	26 43
USB_EXTB	USB_85D	USB	USB_EXTB_MUX_N	26 43
USB_EXTB	USB_85D	USB	USB_EXTB_MIXED_F_P	42
USB_EXTB	USB_85D	USB	USB_EXTB_MIXED_F_N	42
USB_EXTB	USB_85D	USB	USB_EXTB_F_P	43
USB_EXTB	USB_85D	USB	USB_EXTB_F_N	43
USB_EXTB	USB_85D	USB	USB_EXTB_MIXED_P	42
USB_EXTB	USB_85D	USB	USB_EXTB_MIXED_N	42
USB_EXTB	USB_85D	USB	USB_EXTB_XHCI_P	8 18
USB_EXTB	USB_85D	USB	USB_EXTB_XHCI_N	8 18
USB_EXTB	USB_85D	USB	USB_EXTB_EHCI_P	16 25
USB_EXTB	USB_85D	USB	USB_EXTB_EHCI_N	16 25
USB_EXTB	USB_85D	USB	USB_EXTB_XHCI_P	16 25
USB_EXTB	USB_85D	USB	USB_EXTB_XHCI_N	16 25
USB3_EXT_RX	USB3_85D	USB3_RCH_RX	USB3_EXT_RX_P	16 42
USB3_EXT_RX	USB3_85D	USB3_RCH_RX	USB3_EXT_RX_N	16 42
USB3_EXT_TX	USB3_85D	USB3_RCH_TX	USB3_EXT_TX_P	16 42
USB3_EXT_TX	USB3_85D	USB3_RCH_TX	USB3_EXT_TX_N	16 42
USB3_EXT_RX	USB3_85D	USB3_RCH_RX	USB3_EXTB_RX_P	16 43
USB3_EXT_RX	USB3_85D	USB3_RCH_RX	USB3_EXTB_RX_N	16 43
USB3_EXT_TX	USB3_85D	USB3_RCH_TX	USB3_EXTB_TX_P	16 43
USB3_EXT_TX	USB3_85D	USB3_RCH_TX	USB3_EXTB_TX_N	16 43
USB3_EXT_RX	USB3_85D	USB3_RCH_RX	USB3_EXT_RX_F_P	42
USB3_EXT_RX	USB3_85D	USB3_RCH_RX	USB3_EXT_RX_F_N	42
USB3_EXT_TX	USB3_85D	USB3_RCH_TX	USB3_EXT_TX_F_P	42
USB3_EXT_TX	USB3_85D	USB3_RCH_TX	USB3_EXTB_RX_F_P	43
USB3_EXT_RX	USB3_85D	USB3_RCH_RX	USB3_EXTB_TX_F_P	43
USB3_EXT_RX	USB3_85D	USB3_RCH_RX	USB3_EXTB_TX_F_N	43
USB3_EXT_TX	USB3_85D	USB3_RCH_TX	USB3_EXT_TX_C_P	42
USB3_EXT_TX	USB3_85D	USB3_RCH_TX	USB3_EXT_TX_C_N	42
USB3_EXT_RX	USB3_85D	USB3_RCH_RX	USB3_EXT_RX_C_P	43
USB3_EXT_RX	USB3_85D	USB3_RCH_RX	USB3_EXTB_TX_C_N	43
USB_EXTA	USB_85D	USB	USB_SMC_P	8 45
USB_EXTA	USB_85D	USB	USB_SMC_N	8 45
USB_EXTC	USB_85D	USB	USB_EXTC_P	8 18
USB_EXTC	USB_85D	USB	USB_EXTC_N	8 18
USB_CAMERA	USB_85D	USB	USB_CAMERA_P	16 32
USB_CAMERA	USB_85D	USB	USB_CAMERA_N	16 32
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P	6 32
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_N	6 32
USB_BT	USB_85D	USB	USB_BT_P	8 32
USB_BT	USB_85D	USB	USB_BT_N	8 32
USB_BT	USB_85D	USB	USB_BT_CONN_P	6 32
USB_BT	USB_85D	USB	USB_BT_CONN_N	6 32
USB_TP4D	USB_85D	USB	USB_TP4D_P	8 53
USB_TP4D	USB_85D	USB	USB_TP4D_N	8 53
USB_IR	USB_85D	USB	USB_IR_P	8 44
USB_IR	USB_85D	USB	USB_IR_N	8 44
PCH_USB_RBIFAS	PCH_USB_RBIFAS		PCH_USB_RBIFAS	16
PCH_CLK100M_UNBIFAS	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	16
PCH_CLK100M_UNBIFAS	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	16
PCH_CLK100M_UNBIFAS	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	16
PCH_CLK100M_UNBIFAS	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	16
PCH_CLK100M_UNBIFAS	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	16
PCH_CLK100M_UNBIFAS	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	16
PCH_CLK100M_UNBIFAS	CLK_PCIE_90D	CLK_PCIE	PCH_CLK14P3M_REFCLK	16
PCH_CLK100M_UNBIFAS	CLK_PCIE_90D	CLK_PCIE	PCH_CLK33M_PCIEIN	16 24

SYNC MASTER=K901 M1B		SYNC DATE=02/15/2011	
PAGE TITLE			
PCH Constraints 1			
	Apple Inc.		DRAWING NUMBER 051-9058
			REVISION 6.0.0
			SIZE D
NOTICE OF PROPRIETARY PROPERTY:			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED			
		BRANCH	PAGE 102 OF 109
		SHEET 80 OF 86	







## DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

## T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2x_DIELECTRIC	?

## T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

## T29/DP Connector Signal Constraints

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?	T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

## T29 IC Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
REG0		DP_85D	DP_PCH_TX	DP_T29SNK0 ML C P<3..0>	0 33
REG1		DP_85D	DP_PCH_TX	DP_T29SNK0 ML C N<3..0>	0 33
REG2	DP_T29SNK0_ML	DP_85D	DP_PCH_TX	DP_T29SNK0 ML P<3..0>	33
REG3	DP_T29SNK0_ML	DP_85D	DP_PCH_TX	DP_T29SNK0 ML N<3..0>	33
REG4		DP_85D	DP_PCH	DP_T29SNK0 AUXCH C P	0 33
REG5		DP_85D	DP_PCH	DP_T29SNK0 AUXCH C N	0 33
REG6	DP_T29SNK0_AUXCH	DP_85D	DP_PCH	DP_T29SNK0 AUXCH P	33
REG7	DP_T29SNK0_AUXCH	DP_85D	DP_PCH	DP_T29SNK0 AUXCH N	33
REG8		DP_85D	DP_PCH_TX	DP_T29SNK1 ML C P<3..0>	0 33
REG9		DP_85D	DP_PCH_TX	DP_T29SNK1 ML C N<3..0>	0 33
REG10	DP_T29SNK1_ML	DP_85D	DP_PCH_TX	DP_T29SNK1 ML P<3..0>	33
REG11	DP_T29SNK1_ML	DP_85D	DP_PCH_TX	DP_T29SNK1 ML N<3..0>	33
REG12		DP_85D	DP_PCH	DP_T29SNK1 AUXCH C P	0 33
REG13		DP_85D	DP_PCH	DP_T29SNK1 AUXCH C N	0 33
REG14	DP_T29SNK1_AUXCH	DP_85D	DP_PCH	DP_T29SNK1 AUXCH P	33
REG15	DP_T29SNK1_AUXCH	DP_85D	DP_PCH	DP_T29SNK1 AUXCH N	33
REG16		DP_85D	DISPLAYPORT	DP_T29SRC ML C P<3..0>	33
REG17		DP_85D	DISPLAYPORT	DP_T29SRC ML C N<3..0>	33
REG18		DP_85D	DISPLAYPORT	DP_T29SRC AUXCH C P	33
REG19		DP_85D	DISPLAYPORT	DP_T29SRC AUXCH C N	33
REG20		T29_I2C_55S	T29_I2C	I2C T29_SCL	33 48
REG21		T29_I2C_55S	T29_I2C	I2C T29_SDA	33 48
REG22	T29_SEI_CLK	T29_SPT_55S	T29_SPT	T29 SPI_CLK	33
REG23	T29_SEI_MOST	T29_SPT_55S	T29_SPT	T29 SPI_MOST	33
REG24	T29_SEI_MISO	T29_SPT_55S	T29_SPT	T29 SPI_MISO	33
REG25	T29_SEI_CS_L	T29_SPT_55S	T29_SPT	T29 SPI_CS_L	33
REG26		T29DP_80D	T29DP	T29 R2D C P<3..0>	0 33 76
REG27		T29DP_80D	T29DP	T29 R2D C N<3..0>	0 33 76
REG28		T29DP_100D	T29DP	T29 D2R P<3..0>	0 33 76
REG29		T29DP_100D	T29DP	T29 D2R N<3..0>	0 33 76

Only used on hosts supporting T29 video-in

## T29/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		SPACING	
	PHYSICAL			
R10	T29_R2D0	T29DP 80D	T29DP	T29 R2D P<0>
R10	T29_R2D0	T29DP 80D	T29DP	T29 R2D N<0>
R10	T29_R2D1	T29DP 80D	T29DP	T29 R2D P<1>
R10	T29_R2D1	T29DP 80D	T29DP	T29 R2D N<1>
R10	T29_R2D C F	T29DP 80D	T29DP	T29 R2D C F P<1...0>
R10	T29_R2D C F	T29DP 80D	T29DP	T29 R2D C F N<1...0>
R10	T29_R2R0	T29DP 100D	T29DP	T29 D2R C P<0>
R10	T29_R2R0	T29DP 100D	T29DP	T29 D2R C N<0>
R10	T29_R2R1	T29DP 100D	T29DP	T29 D2R C P<1>
R10	T29_R2R1	T29DP 100D	T29DP	T29 D2R C N<1>
R10	T29DP 100D	T29DP		T29DPA D2R1 AUXCH P
R10	T29DP 100D	T29DP		T29DPA D2R1 AUXCH N
R10	T29DP 80D	T29DP		DP SDRVA ML C P<3...0>
R10	T29DP 80D	T29DP		DP SDRVA ML C N<3...0>
R10	T29DP 80D	T29DP		DP SDRVA ML R P<3...0>
R10	T29DP 80D	T29DP		DP SDRVA ML R N<3...0>
R10	DP_SDRVA_ML_EVEN	T29DP 80D	T29DP	DP SDRVA ML P<2...0:2>
R10	DP_SDRVA_ML_EVEN	T29DP 80D	T29DP	DP SDRVA ML N<2...0:2>
R10	DP_SDRVA_ML_ODD	T29DP 80D	T29DP	DP SDRVA ML P<3...1:2>
R10	DP_SDRVA_ML_ODD	T29DP 80D	T29DP	DP SDRVA ML N<3...1:2>
R10	DP_SDRVA_AUXCH	T29DP 80D	T29DP	DP SDRVA AUXCH P
R10	DP_SDRVA_AUXCH	T29DP 80D	T29DP	DP SDRVA AUXCH N
R10	T29DP 80D	T29DP		DP SDRVA AUXCH C P
R10	T29DP 80D	T29DP		DP SDRVA AUXCH C N
R10	T29DP 80D	T29DP		T29DPA ML P<3...0>
R10	T29DP 80D	T29DP		T29DPA ML N<3...0>
R10	T29DP 80D	T29DP		T29DPA ML C P<3...0>
R10	T29DP 80D	T29DP		T29DPA ML C N<3...0>
R10	T29DP 80D	T29DP		DP A EXT AUXCH P
R10	T29DP 80D	T29DP		DP A EXT AUXCH N
R10	T29_R2D2	T29DP 80D	T29DP	T29 R2D P<2>
R10	T29_R2D2	T29DP 80D	T29DP	T29 R2D N<2>
R10	T29_R2D3	T29DP 80D	T29DP	T29 R2D P<3>
R10	T29_R2D3	T29DP 80D	T29DP	T29 R2D N<3>
R10	T29DP 80D	T29DP		T29 R2D C F P<3...2>
R10	T29DP 80D	T29DP		T29 R2D C F N<3...2>
R10	T29_R2R2	T29DP 100D	T29DP	T29 D2R C P<2>
R10	T29_R2R2	T29DP 100D	T29DP	T29 D2R C N<2>
R10	T29_R2R3	T29DP 100D	T29DP	T29 D2R C P<3>
R10	T29_R2R3	T29DP 100D	T29DP	T29 D2R C N<3>
R10	T29DP 100D	T29DP		T29DPB D2R3 AUXCH P
R10	T29DP 100D	T29DP		T29DPB D2R3 AUXCH N
R10	T29DP 80D	T29DP		DP SDRVB ML C P<3...0>
R10	T29DP 80D	T29DP		DP SDRVB ML C N<3...0>
R10	T29DP 80D	T29DP		DP SDRVB ML R P<3...0>
R10	T29DP 80D	T29DP		DP SDRVB ML R N<3...0>
R10	DP_SDRVB_ML_EVEN	T29DP 80D	T29DP	DP SDRVB ML P<2...0:2>
R10	DP_SDRVB_ML_EVEN	T29DP 80D	T29DP	DP SDRVB ML N<2...0:2>
R10	DP_SDRVB_ML_ODD	T29DP 80D	T29DP	DP SDRVB ML P<3...1:2>
R10	DP_SDRVB_ML_ODD	T29DP 80D	T29DP	DP SDRVB ML N<3...1:2>
R10	DP_SDRVB_AUXCH	T29DP 80D	T29DP	DP SDRVB AUXCH P
R10	DP_SDRVB_AUXCH	T29DP 80D	T29DP	DP SDRVB AUXCH N
R10	T29DP 80D	T29DP		DP SDRVB AUXCH C P
R10	T29DP 80D	T29DP		DP SDRVB AUXCH C N
R10	T29DP 80D	T29DP		T29DPB ML P<3...0>
R10	T29DP 80D	T29DP		T29DPB ML N<3...0>
R10	T29DP 80D	T29DP		T29DPB ML C P<3...0>
R10	T29DP 80D	T29DP		T29DPB ML C N<3...0>
R10	T29DP 80D	T29DP		DP B EXT AUXCH P
R10	T29DP 80D	T29DP		DP B EXT AUXCH N

Only used on dual-port hosts.



www.laptop-schematics.com

www.laptop-schematics.com

www.laptop-schematics.com

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_I701_55S	*	+1:1_DIFFPAIR	+55_OHM_SE	+55_OHM_SE	+55_OHM_SE	+1:1_DIFFPAIR	+1:1_DIFFPAIR
THERM_I701_55S	*	+1:1_DIFFPAIR	+55_OHM_SE	+55_OHM_SE	+55_OHM_SE	+1:1_DIFFPAIR	+1:1_DIFFPAIR
DIFFPAIR	*	+1:1_DIFFPAIR			+1:1_DIFFPAIR	+1:1_DIFFPAIR	+1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENHTECOBH	*	25 MILS	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	-STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCIE	*	GND_P2004

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

GRD	PCIE*	*	GRD_P2061
GRD	DATA*	*	GRD_P2061
GRD	USB*	*	GRD_P2061
SB_POWER	CLK_PCIE	*	PWR_P2061
SB_POWER	DATA*	*	PWR_P2061
SB_POWER	DATA*	*	PWR_P2061

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLE	QND	*	QND_P2984
MEM_CND	QND	*	QND_P2984
MEM_CTLG	QND	*	QND_P2984
MEM_DATA	QND	*	QND_P2984
MEM_PQS	QND	*	QND_P2984

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	LVSIS*	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_4QS OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIB_85D OVERRIDE	*	OVERRIDE	OVERRIDE	0.076 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	TOP	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
CLK_PCIE_90D OVERRIDE	TOP	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE

## Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.


PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

### J30 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
	ENET-10G0	ENETCONN	ENETCONN P<3...0>
	ENET-10G0	ENETCONN	ENETCONN N<3...0>
	SATA-90D	SATA-RCH-RX	SATA-00D-D28-C-P
	SATA-90D	SATA-RCH-RX	SATA-00D-D28-C-N
	SATA-90D	SATA3-RCH-RX	SATA-HDD-D28-REROUT-F
	SATA-90D	SATA3-RCH-RX	SATA-HDD-D28-REROUT-N
	SATA-90D	SATA3-RCH-TV	SATA-HDD-R2D-REDIR-N
	SATA-90D	SATA3-RCH-TV	SATA-HDD-R2D-REDIR-N
	SATA-90D	SATA3-RCH-TV	SATA-HDD-D28-REDIR-N
	SATA-90D	SATA3-RCH-TV	SATA-HDD-D28-REDIR-N
	SATA-90D	SATA3-RCH-TV	SATA-HDD-R2D-REROUT-F
	SATA-90D	SATA3-RCH-TV	SATA-HDD-R2D-REROUT-N
	ENSE-000000	ENSE-1001-550	THMSNS-D1-P
	ENSE-000000	ENSE-1001-550	THMSNS-D1-N
	ENSE-000000	ENSE-1001-550	THMSNS-D2-P
	ENSE-000000	ENSE-1001-550	THMSNS-D2-N
	ENSE-000000	ENSE-1001-550	T29-THERMD-F
	ENSE-000000	ENSE-1001-550	T29-THERMD-N
	ENSE-000000	ENSE-1001-550	T29THMSNS-D2-P
	ENSE-000000	ENSE-1001-550	T29THMSNS-D2-N
	ENSE-000000	ENSE-1001-550	ISNS-HS-COMPUTING-N
	ENSE-000000	ENSE-1001-550	ISNS-HS-COMPUTING-P
	ENSE-000000	ENSE-1001-550	ISNS-HS-OTHER-N
	ENSE-000000	ENSE-1001-550	ISNS-HS-OTHER-P
	ENSE-000000	ENSE-1001-550	CPUVCCIOS0-CS-N
	ENSE-000000	ENSE-1001-550	CPUVCCIOS0-CS-P
	ENSE-000000	ENSE-1001-550	CPUIMVP-ISNS1-P
	ENSE-000000	ENSE-1001-550	CPUIMVP-ISNS1-N
	ENSE-000000	ENSE-1001-550	CPUIMVP-ISNS2-P
	ENSE-000000	ENSE-1001-550	CPUIMVP-ISNS2-N
	ENSE-000000	ENSE-1001-550	CPUIMVP-ISNS1G-P
	ENSE-000000	ENSE-1001-550	CPUIMVP-ISNS1G-N
	ENSE-000000	ENSE-1001-550	CPUIMVP-ISNS2G-P
	ENSE-000000	ENSE-1001-550	CPUIMVP-ISNS2G-N
	ENSE-000000	ENSE-1001-550	CPUIMVP-ISUM-R-P
	ENSE-000000	ENSE-1001-550	CPUIMVP-ISUM-R-N
	ENSE-000000	ENSE-1001-550	CPUIMVP-ISUMG-R-P
	ENSE-000000	ENSE-1001-550	CPUIMVP-ISUMG-R-N
	ENSE-000000	ENSE-1001-550	CPUIMVP-ISNSG-P
	ENSE-000000	ENSE-1001-550	CPUIMVP-ISNSG-N
	ENSE-000000	ENSE-1001-550	CPUIMVP-ISNS-P
	ENSE-000000	ENSE-1001-550	CPUIMVP-ISNS-N
	ENSE-000000	ENSE-1001-550	VCCBAS0-CS-P
	ENSE-000000	ENSE-1001-550	VCCBAS0-CS-N
	ENSE-000000	ENSE-1001-550	CPUIMVP-ISUMG-R
	ENSE-000000	ENSE-1001-550	CPUIMVP-ISUMG-N
	ENSE-000000	ENSE-1001-550	CPU-THERMD-P
	ENSE-000000	ENSE-1001-550	CPU-THERMD-N
	ENSE-000000	ENSE-1001-550	ISNS-5V-80-HDD-N
	ENSE-000000	ENSE-1001-550	ISNS-5V-80-HDD-P
	ENSE-000000	ENSE-1001-550	ISNS-5V-80-HDD-R-N
	ENSE-000000	ENSE-1001-550	ISNS-5V-80-HDD-R-P
	ENSE-000000	ENSE-1001-550	ISNS-LC00WLT-N
	ENSE-000000	ENSE-1001-550	ISNS-LC00WLT-P
	ENSE-000000	ENSE-1001-550	ISNS-1V5-83-D0W-P
	ENSE-000000	ENSE-1001-550	ISNS-1V5-83-D0W-N
	ENSE-000000	ENSE-1001-550	ISNS-1V5-83-D0W-R-P
	ENSE-000000	ENSE-1001-550	ISNS-1V5-83-D0W-R-N
	LVDS-80D	LVDS-RCH-TV	LVDS-C00N-A-CLK-F-N
	LVDS-80D	LVDS-RCH-TV	LVDS-C00N-A-CLK-F-P

## J30 Specific Net Properties

[illegible]

SYNCH MASTER-K907.WLB		SYNCH DATE=02/15/2013	
PAGE TITLE			
Project Specific Constraints			
 Apple Inc.		DRAWING NUMBER	051-9058
		SIZE	D
		REVISION	6.0.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:			
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		PAGE	
II NOT TO REPRODUCE OR COPY IT		108 OF 109	
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		SHEET	
IV ALL RIGHTS RESERVED		85 OF 86	

8		7		6		5		4		3		2		1	
K90i Board-Specific Spacing & Physical Constraints															
BOARD LAYERS								BOARD AREAS				BOARD UNITS (MIL or MM)		ALLEGRO VERSION	
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM								NO_TYPE, BGA				MM		16.2	
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
DEFAULT		*	Y	~50_OHM_SR	~50_OHM_SR	10 MM	0 MM	0 MM							
STANDARD		*	Y	~DEFAULT	~DEFAULT	10 MM	~DEFAULT	~DEFAULT							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
50_OHM_SR		TOP, BOTTOM	Y	0.110 MM	0.090 MM										
50_OHM_SR		*	Y	0.080 MM	0.080 MM	~STANDARD	~STANDARD	~STANDARD							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
40_OHM_SR		TOP, BOTTOM	Y	0.165 MM	0.165 MM										
40_OHM_SR		ISL10	N	0.126 MM	0.126 MM	~STANDARD	~STANDARD	~STANDARD							
40_OHM_SR		ISL3, ISL4, ISL9	Y	0.126 MM	0.126 MM	~STANDARD	~STANDARD	~STANDARD							
40_OHM_SR		*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
37_OHM_SR		TOP, BOTTOM	Y	0.190 MM	0.1 MM										
37_OHM_SR		ISL10	N	0.145 MM	0.1 MM	~STANDARD	~STANDARD	~STANDARD							
37_OHM_SR		ISL3, ISL4, ISL9	Y	0.145 MM	0.1 MM	~STANDARD	~STANDARD	~STANDARD							
37_OHM_SR		*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
27P4_OHM_SR		TOP, BOTTOM	Y	0.310 MM	0.2 MM										
27P4_OHM_SR		*	Y	0.235 MM	0.2 MM	~STANDARD	~STANDARD	~STANDARD							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
55_OHM_SR		TOP, BOTTOM	Y	0.090 MM	0.090 MM										
55_OHM_SR		*	Y	0.070 MM	0.070 MM	~STANDARD	~STANDARD	~STANDARD							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
72_OHM_DIFF		*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD							
72_OHM_DIFF		ISL3, ISL4, ISL9	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM							
72_OHM_DIFF		ISL10	N	0.140MM	0.140 MM		0.190 MM	0.190 MM							
72_OHM_DIFF		TOP, BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
85_OHM_DIFF		*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD							
85_OHM_DIFF		ISL3, ISL4	Y	0.101 MM	0.1 MM		0.170 MM	0.170 MM							
85_OHM_DIFF		ISL9, ISL10	Y	0.101 MM	0.1 MM		0.170 MM	0.170 MM							
85_OHM_DIFF		TOP, BOTTOM	Y	0.125 MM	0.1 MM		0.190 MM	0.190 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
90_OHM_DIFF		*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD							
90_OHM_DIFF		ISL3, ISL4	Y	0.091 MM	0.091 MM		0.180 MM	0.180 MM							
90_OHM_DIFF		ISL9, ISL10	Y	0.091 MM	0.091 MM		0.180 MM	0.180 MM							
90_OHM_DIFF		TOP, BOTTOM	Y	0.111 MM	0.111 MM		0.200 MM	0.200 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
100_OHM_DIFF		*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD							
100_OHM_DIFF		ISL3, ISL4	Y	0.076 MM	0.076 MM		0.250 MM	0.250 MM							
100_OHM_DIFF		ISL9, ISL10	Y	0.076 MM	0.076 MM		0.250 MM	0.250 MM							
100_OHM_DIFF		TOP, BOTTOM	Y	0.085 MM	0.085 MM		0.200 MM	0.200 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
110_OHM_DIFF		*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD							
110_OHM_DIFF		ISL3, ISL4	Y	0.068 MM	0.068 MM		0.250 MM	0.250 MM							
110_OHM_DIFF		ISL9, ISL10	Y	0.068 MM	0.068 MM		0.250 MM	0.250 MM							
110_OHM_DIFF		TOP, BOTTOM	Y	0.081 MM	0.081 MM		0.250 MM	0.250 MM							
NOTE: These are Intel recommended impedances for PEG, unused on K90i.															
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
48_OHM_SR		TOP, BOTTOM	Y	0.165 MM	0.165 MM										
48_OHM_SR		*	Y	0.090 MM	0.090 MM	~STANDARD	~STANDARD	~STANDARD							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
80_OHM_DIFF		*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD							
80_OHM_DIFF		ISL3, ISL4	Y	0.115 MM	0.115 MM		0.180 MM	0.180 MM							
80_OHM_DIFF		ISL9, ISL10	Y	0.115 MM	0.115 MM		0.180 MM	0.180 MM							
80_OHM_DIFF		TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
100_OHM_DIFF		*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD							
100_OHM_DIFF		ISL3, ISL4	Y	0.075 MM	0.075 MM		0.250 MM	0.250 MM							
100_OHM_DIFF		ISL9, ISL10	Y	0.075 MM	0.075 MM		0.250 MM	0.250 MM							
100_OHM_DIFF		TOP, BOTTOM	Y	0.085 MM	0.085 MM		0.200 MM	0.200 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
110_OHM_DIFF		*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD							
110_OHM_DIFF		ISL3, ISL4	Y	0.068 MM	0.068 MM		0.250 MM	0.250 MM							
110_OHM_DIFF		ISL9, ISL10	Y	0.068 MM	0.068 MM		0.250 MM	0.250 MM							
110_OHM_DIFF		TOP, BOTTOM	Y	0.081 MM	0.081 MM		0.250 MM	0.250 MM							
NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.															
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
100_OHM_DIFF		*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD							
100_OHM_DIFF		ISL3, ISL4	Y	0.075 MM	0.075 MM		0.250 MM	0.250 MM							
100_OHM_DIFF		ISL9, ISL10	Y	0.075 MM	0.075 MM		0.250 MM	0.250 MM							
100_OHM_DIFF		TOP, BOTTOM	Y	0.085 MM	0.085 MM		0.200 MM	0.200 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
110_OHM_DIFF		*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD							
110_OHM_DIFF		ISL3, ISL4	Y	0.068 MM	0.068 MM		0.250 MM	0.250 MM							
110_OHM_DIFF		ISL9, ISL10	Y	0.068 MM	0.068 MM		0.250 MM	0.250 MM							
110_OHM_DIFF		TOP, BOTTOM	Y	0.081 MM	0.081 MM		0.250 MM	0.250 MM							
NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.															
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
100_OHM_DIFF		*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD							
100_OHM_DIFF		ISL3, ISL4	Y	0.075 MM	0.075 MM		0.250 MM	0.250 MM							
100_OHM_DIFF		ISL9, ISL10	Y	0.075 MM	0.075 MM		0.250 MM	0.250 MM							
100_OHM_DIFF		TOP, BOTTOM	Y	0.085 MM	0.085 MM		0.200 MM	0.200 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
110_OHM_DIFF		*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD							
110_OHM_DIFF		ISL3, ISL4	Y	0.068 MM	0.068 MM		0.250 MM	0.250 MM							
110_OHM_DIFF		ISL9, ISL10	Y	0.068 MM	0.068 MM		0.250 MM	0.250 MM							
110_OHM_DIFF		TOP, BOTTOM	Y	0.081 MM	0.081 MM		0.250 MM	0.250 MM							
NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.															
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
100_OHM_DIFF		*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD							
100_OHM_DIFF		ISL3, ISL4	Y	0.075 MM	0.075 MM		0.250 MM	0.250 MM							
100_OHM_DIFF		ISL9, ISL10	Y	0.075 MM	0.075 MM		0.250 MM	0.250 MM							
100_OHM_DIFF		TOP, BOTTOM	Y	0.085 MM	0.085 MM		0.200 MM	0.200 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
110_OHM_DIFF		*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD							
110_OHM_DIFF		ISL3, ISL4	Y	0.068 MM	0.068 MM		0.250 MM	0.250 MM							
110_OHM_DIFF		ISL9, ISL10	Y	0.068 MM	0.068 MM		0.250 MM	0.250 MM							
110_OHM_DIFF		TOP, BOTTOM	Y	0.081 MM	0.081 MM		0.250 MM	0.250 MM							
NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.															
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
100_OHM_DIFF		*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD							
100_OHM_DIFF		ISL3, ISL4	Y	0.075 MM	0.075 MM		0.250 MM	0.250 MM							
100_OHM_DIFF		ISL9, ISL10	Y	0.075 MM	0.075 MM		0.250 MM	0.250 MM							
100_OHM_DIFF		TOP, BOTTOM	Y	0.085 MM	0.085 MM		0.200 MM	0.200 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
110_OHM_DIFF		*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD							
110_OHM_DIFF		ISL3, ISL4	Y	0.068 MM	0.068 MM		0.250 MM	0.250 MM							
110_OHM_DIFF		ISL9, ISL10	Y	0.068 MM	0.068 MM		0.250 MM	0.250 MM							
110_OHM_DIFF		TOP, BOTTOM	Y	0.081 MM	0.081 MM		0.250 MM	0.250 MM							
NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.															
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
100_OHM_DIFF		*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD							
100_OHM_DIFF		ISL3, ISL4	Y	0.075 MM	0.075 MM		0.250 MM	0.250 MM							
100_OHM_DIFF		ISL9, ISL10	Y	0.075 MM	0.075 MM		0.250 MM	0.250 MM							
100_OHM_DIFF		TOP, BOTTOM	Y	0.085 MM	0.085 MM		0.200 MM	0.200 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
110_OHM_DIFF		*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD							
110_OHM_DIFF		ISL3, ISL4	Y	0.068 MM	0.068 MM		0.250 MM	0.250 MM							
110_OHM_DIFF		ISL9, ISL10	Y	0.068 MM	0.068 MM		0.250 MM	0.250 MM							
110_OHM_DIFF		TOP, BOTTOM	Y	0.081 MM	0.081 MM		0.250 MM	0.250 MM							
NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.															
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
100_OHM_DIFF		*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD							
100_OHM_DIFF		ISL3, ISL4	Y	0.075 MM	0.075 MM		0.250 MM	0.250 MM							
100_OHM_DIFF		ISL9, ISL10	Y	0.075 MM	0.075 MM		0.250 MM	0.250 MM							
100_OHM_DIFF		TOP, BOTTOM	Y	0.085 MM	0.085 MM		0.200 MM	0.200 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
110_OHM_DIFF		*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD							
110_OHM_DIFF		ISL3, ISL4	Y	0.068 MM	0.068 MM		0.250 MM	0.250 MM							
110_OHM_DIFF		ISL9, ISL10	Y	0.068 MM	0.068 MM		0.250 MM	0.250 MM							
110_OHM_DIFF		TOP, BOTTOM	Y	0.081 MM	0.081 MM		0.250 MM	0.250 MM							
NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.															
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
100_OHM_DIFF		*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD							
100_OHM_DIFF		ISL3, ISL4	Y	0.075 MM	0.075 MM		0.250 MM	0.250 MM							