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Functional Test Points

Fan Connectors

PP5V	TRUE	PP5V_S0	7 8 57
FAN	TRUE	FAN_RT_PWM	45
FAN	TRUE	FAN_RT_TACH	45

(NEED TO ADD 1 GND TP)

SPEAKER FUNC\_TEST

SPKR	TRUE	SPKRAMP_R_N_OUT	48 49
SPKR	TRUE	SPKRAMP_R_P_OUT	48 49

INT DP FUNC\_TEST

PP3V3	TRUE	PP3V3_SW_LCD	7 59 (NEED 2 TP)
PPVOUT	TRUE	PPVOUT_SW_LCDBKLT	2, 42 59 (NEED 2 TP)
DP	TRUE	DP_INT_ML_F_N<0>	59 71
DP	TRUE	DP_INT_ML_F_P<0>	59 71
DP	TRUE	DP_INT_ML_F_N<1>	59 71
DP	TRUE	DP_INT_ML_F_P<1>	59 71
DP	TRUE	DP_INT_AUX_CH_C_N	59 71
DP	TRUE	DP_INT_AUX_CH_C_P	59 71
DP	TRUE	DP_INT_HPD_CONN	59
LED	TRUE	LED_RETURN_1	59 62
LED	TRUE	LED_RETURN_2	59 62
LED	TRUE	LED_RETURN_3	59 62
LED	TRUE	LED_RETURN_4	59 62
LED	TRUE	LED_RETURN_5	59 62
LED	TRUE	LED_RETURN_6	59 62
I2C	TRUE	=I2C_TCON_SCL	41 59
I2C	TRUE	=I2C_TCON_SDA	41 59

(NEED TO ADD 5 GND TP)

HALL EFFECT CONN (PLACEHOLDER)

SMC	TRUE	SMC_LID_R	49
PP3V42	TRUE	=PP3V42_G3H_HALL	8 49

SATA HDD

PP3V3	TRUE	PP3V3_S0_HDD_R	7 35 (NEED 5 TP)
SATA	TRUE	SATA_HDD_R2D_P	35 67
SATA	TRUE	SATA_HDD_R2D_N	35 67
SATA	TRUE	SATA_HDD_D2R_C_P	35 67
SATA	TRUE	SATA_HDD_D2R_C_N	35 67
SMC	TRUE	SMC_HDD_OOB_TEMP	35 38
SMC	TRUE	SMC_HDD_TEMP_CTL	35 38

(NEED TO ADD 6 GND TP)

BATT POWER CONN

SMBUS	TRUE	SMBUS_SMC_BSA_SCL	41 70
SMBUS	TRUE	SMBUS_SMC_BSA_SDA	41 70
SYS	TRUE	SYS_DETECT_L	49
PPVBAT	TRUE	PPVBAT_G3H_CONN	49 50 (NEED 4 TP)

(NEED TO ADD 4 GND TP NEAR J6950 AND 1 FOR SHIELD)

LIO CONNECTOR

PP3V3	TRUE	=PP3V3_S0_AUDIO	37 (NEED 2 TP)
PP3V42	TRUE	=PP3V42_G3H_ONEWIRE	8 37
SMC	TRUE	SMC_BC_ACOK	9 37 38 39
SYS	TRUE	SYS_ONEWIRE	37 38
USB	TRUE	=USB_PWR_EN	36 37 57
USB	TRUE	USB_EXTD_OC_L	18 37
USB	TRUE	USB_CAMERA_P	18 37 68
USB	TRUE	USB_CAMERA_N	18 37 68
USB	TRUE	USB_EXTD_P	18 37 68
USB	TRUE	USB_EXTD_N	18 37 68
PP1V8R1V5	TRUE	=PP1V8R1V5_S0_AUDIO	8 37
I2C	TRUE	=I2C_LIO_SDA	37 41
I2C	TRUE	=I2C_LIO_SCL	37 41
AUD	TRUE	AUD_GPIO_3	37 48
AUD	TRUE	AUD_I2C_INT_L	19 37
I2C	TRUE	=I2C_MIKEY_SDA	37 41
I2C	TRUE	=I2C_MIKEY_SCL	37 41
AUD	TRUE	AUD_IP_PERIPHERAL_DET	37 37
SPKRAMP	TRUE	SPKRAMP_INR_P	37 48 71
SPKRAMP	TRUE	SPKRAMP_INR_N	37 48 71
HDA	TRUE	HDA_SDIN0	19 37 68
HDA	TRUE	HDA_SDOUT	19 37 68
HDA	TRUE	HDA_BIT_CLK	19 37 68
HDA	TRUE	HDA_SYNC	19 37 68
HDA	TRUE	HDA_RST_L	19 37 68
AUD	TRUE	AUD_IPHS_SWITCH_EN	19 37

(NEED TO ADD 5 GND TP)

AIRPORT / BT

PCIE	TRUE	PCIE_AP_R2D_P	34 67
PCIE	TRUE	PCIE_AP_R2D_N	34 67
PCIE	TRUE	PCIE_AP_D2R_P	16 34 67
PCIE	TRUE	PCIE_AP_D2R_N	16 34 67
PCIE	TRUE	PCIE_CLK100M_AP_P	16 34 67
PCIE	TRUE	PCIE_CLK100M_AP_N	16 34 67
USB	TRUE	USB_BT_P	18 34 68
USB	TRUE	USB_BT_N	18 34 68
WIFI	TRUE	WIFI_EVENT_L	34 38 39
PP3V3	TRUE	=PP3V3_S3_BT	8 34
PP3V3	TRUE	PP3V3_WLAN_F	(NEED 6 TP) 7 34 39
PCIE	TRUE	PCIE_WAKE_L	16 34
AP	TRUE	AP_RESET_CONN_L	34
AP	TRUE	AP_CLKREQ_O_L	34

(NEED TO ADD 8 GND TP)

IPD\_FLEX\_CONN

SMC	TRUE	SMC_TPAD_RST_L	39 46
SMC	TRUE	SMC_LID	38 39 46 49
SMC	TRUE	SMC_ONOFF_L	38 39 46
I2C	TRUE	=I2C_TPAD_SCL	41 46
I2C	TRUE	=I2C_TPAD_SDA	41 46
PP3V42	TRUE	=PP3V42_G3H_TPAD	8 46
PP3V3	TRUE	PP3V3_TPAD_CONN	46
PP5V	TRUE	PP5V_TPAD_FILT	46
USB	TRUE	USB_TPAD_CONN_N	46 71
USB	TRUE	USB_TPAD_CONN_P	46 71

(NEED TO ADD 5 GND TP)

LCP + SPI CONN

PP3V3	TRUE	=PP3V3_S5_LPCPLUS	8 40
PP5V	TRUE	=PP5V_S0_LPCPLUS	8 40
LPC	TRUE	LPC_AD<3..0>	19 38 40 68
SPI	TRUE	SPI_ALT_MOSI	40 68
SPI	TRUE	SPI_ALT_MISO	40 68
LPC	TRUE	LPC_FRAME_L	19 38 40 68
PM	TRUE	PM_CLKRUN_L	19 38 40
SMC	TRUE	SMC_TMS	38 39 40
LPCPLUS	TRUE	LPCPLUS_RESET_L	25 40
SMC	TRUE	SMC_TDO	38 39 40
SMC	TRUE	SMC_TRST_L	38 40
SMC	TRUE	SMC_MD1	38 40
SMC	TRUE	SMC_TX_L	36 38 39 40
LPC	TRUE	LPC_CLK33M_LPCPLUS	25 40 68
SPIROM	TRUE	SPIROM_USE_MLB	19 40 47
SPI	TRUE	SPI_ALT_CLK	40 68
SPI	TRUE	SPI_ALT_CS_L	40 68
LPC	TRUE	LPC_SERIRO	19 38 40
LPC	TRUE	LPC_PWRDWN_L	19 38 40
SMC	TRUE	SMC_TDI	38 39 40
SMC	TRUE	SMC_TCK	38 39 40
SMC	TRUE	SMC_RESET_L	38 39 40 50
SMC	TRUE	SMC_NMI	38 40
SMC	TRUE	SMC_RX_L	36 38 39 40
LPCPLUS	TRUE	LPCPLUS_GPIO	19 40

(NEED TO ADD 6 GND TP)

DC POWER CONN

PP18V5	TRUE	=PP18V5_DCIN_CONN	(NEED 6 TP) 8 49
PP5V	TRUE	=PP5V_S3_LIO_CONN	8 49

(NEED TO ADD 6 GND TP)


DEBUG VOLTAGE

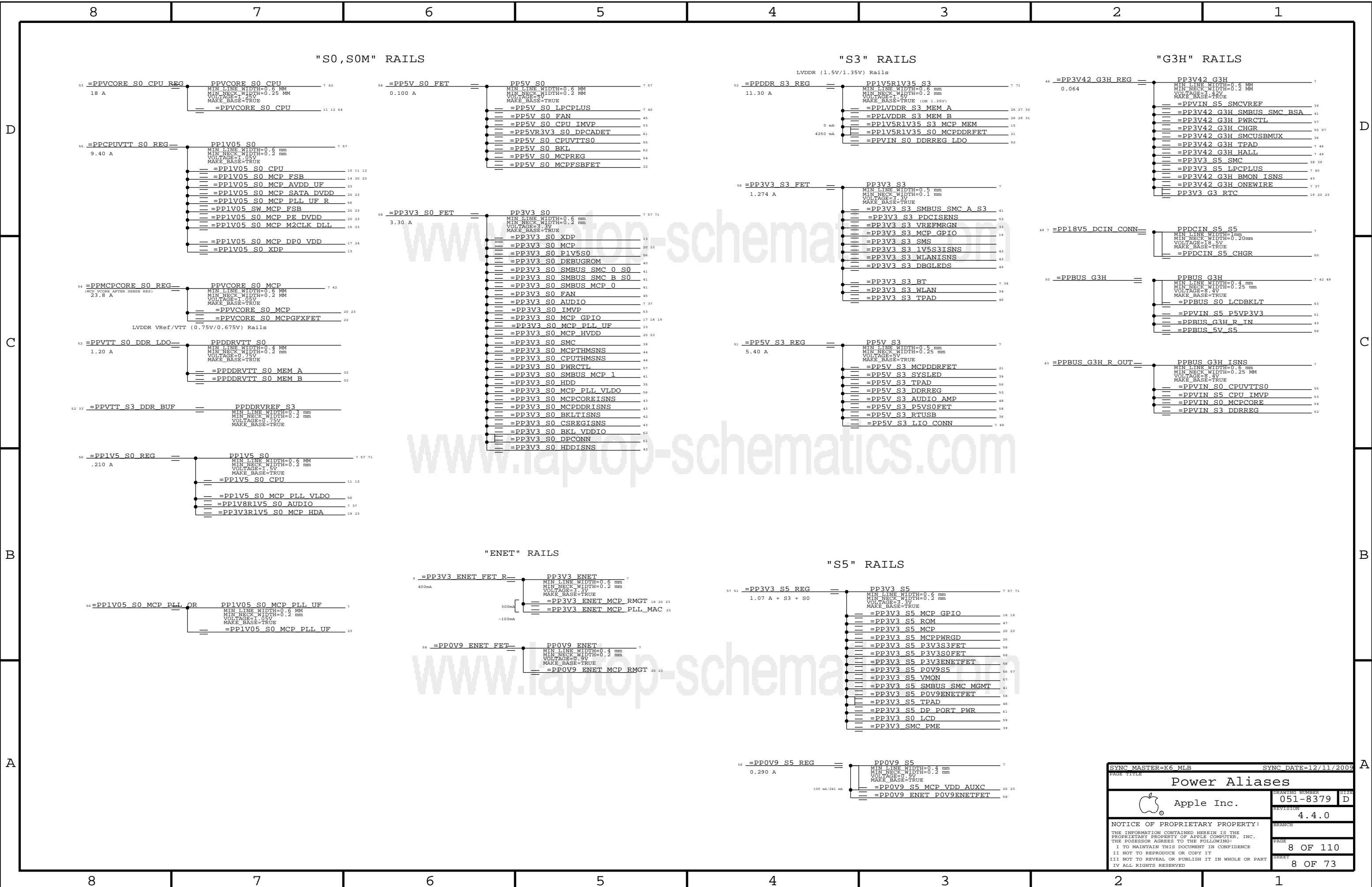
PPVCORE	TRUE	PPVCORE_S0_CPU	8 42
PPVCORE	TRUE	PPVCORE_S0_MCP	8 42
PP1V05	TRUE	PP1V05_S0	8 57
PP1V5	TRUE	PP1V5_S0	8 57 71
PP3V3	TRUE	PP3V3_S0	8 57 71
PP5V	TRUE	PP5V_S0	7 8 57
PP3V3	TRUE	PP3V3_S3	8
PP5V	TRUE	PP5V_S3	8
PP0V9	TRUE	PP0V9_S5	8
PP3V3	TRUE	PP3V3_S5	8 57 71
PP3V42	TRUE	PP3V42_G3H	8
PPBUS	TRUE	PPBUS_G3H	8 42 49
PP3V3	TRUE	PP3V3_WLAN_F	7 34 39
PP3V3	TRUE	PP3V3_S0_HDD_R	7 35
PPDCIN	TRUE	PPDCIN_S5_S5	8
PPVOUT	TRUE	PPVOUT_SW_LCDBKLT	7 42 59 62
PP3V3	TRUE	PP3V3_SW_LCD	7 59
PP1V5R1V35	TRUE	PP1V5R1V35_S3	8 71
SMC	TRUE	SMC_PM_G2_EN	38 57
PM	TRUE	PM_SLP_S4_L	19 38 57
PM	TRUE	PM_SLP_S3_L	19 38 39 57
PP0V9	TRUE	PP0V9_ENET	8
PP1V05	TRUE	PP1V05_S0_MCP_PLL_UF	8
PP3V3	TRUE	PP3V3_ENET	8
PP3V3	TRUE	PP3V3_SW_DPPWR	61
PP5V	TRUE	PP5V_S3_RTUSB_A_F	36
PPBUS	TRUE	PPBUS_G3H_ISNS	8

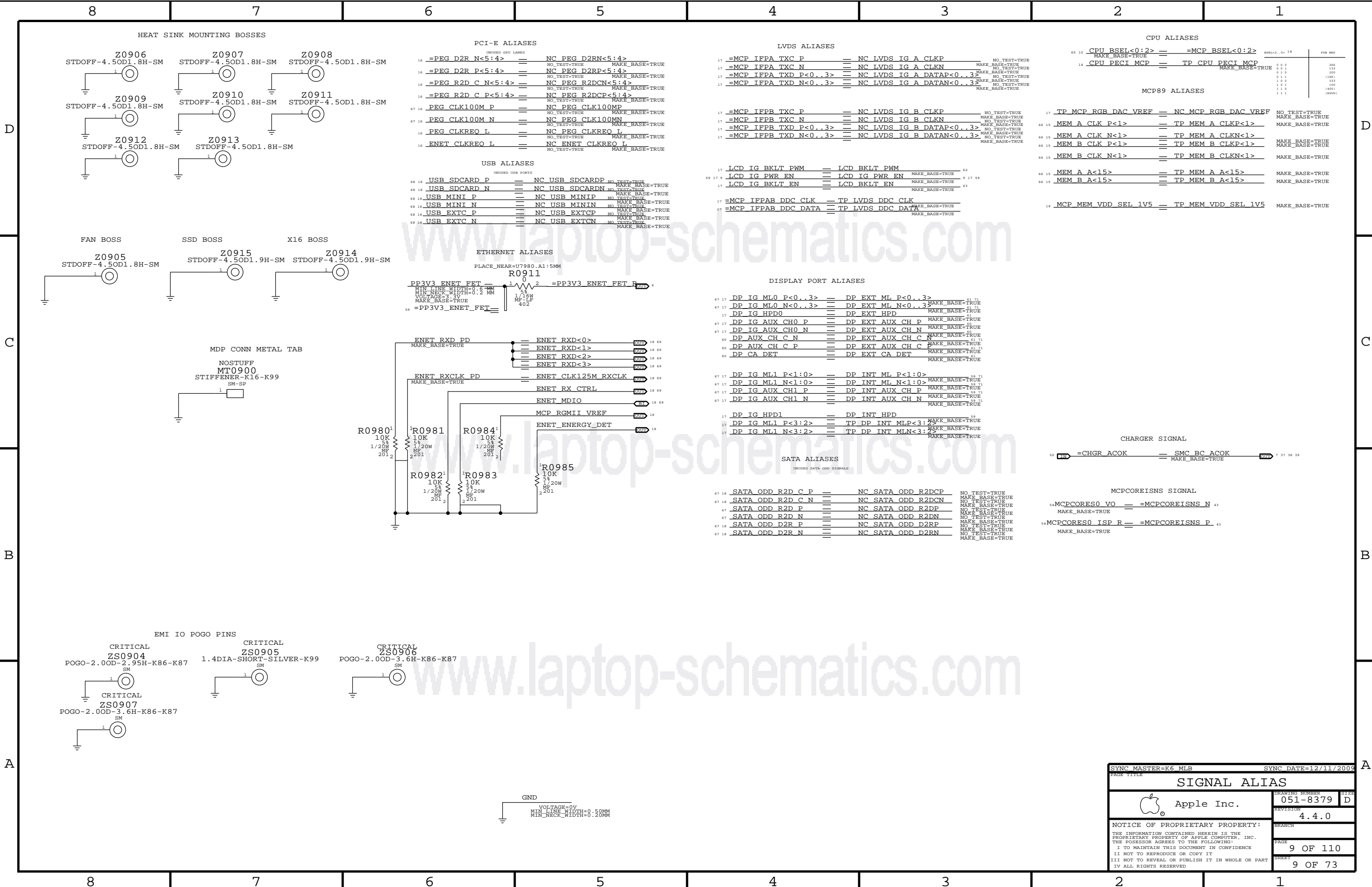
(NEED TO ADD 27 GND TP)

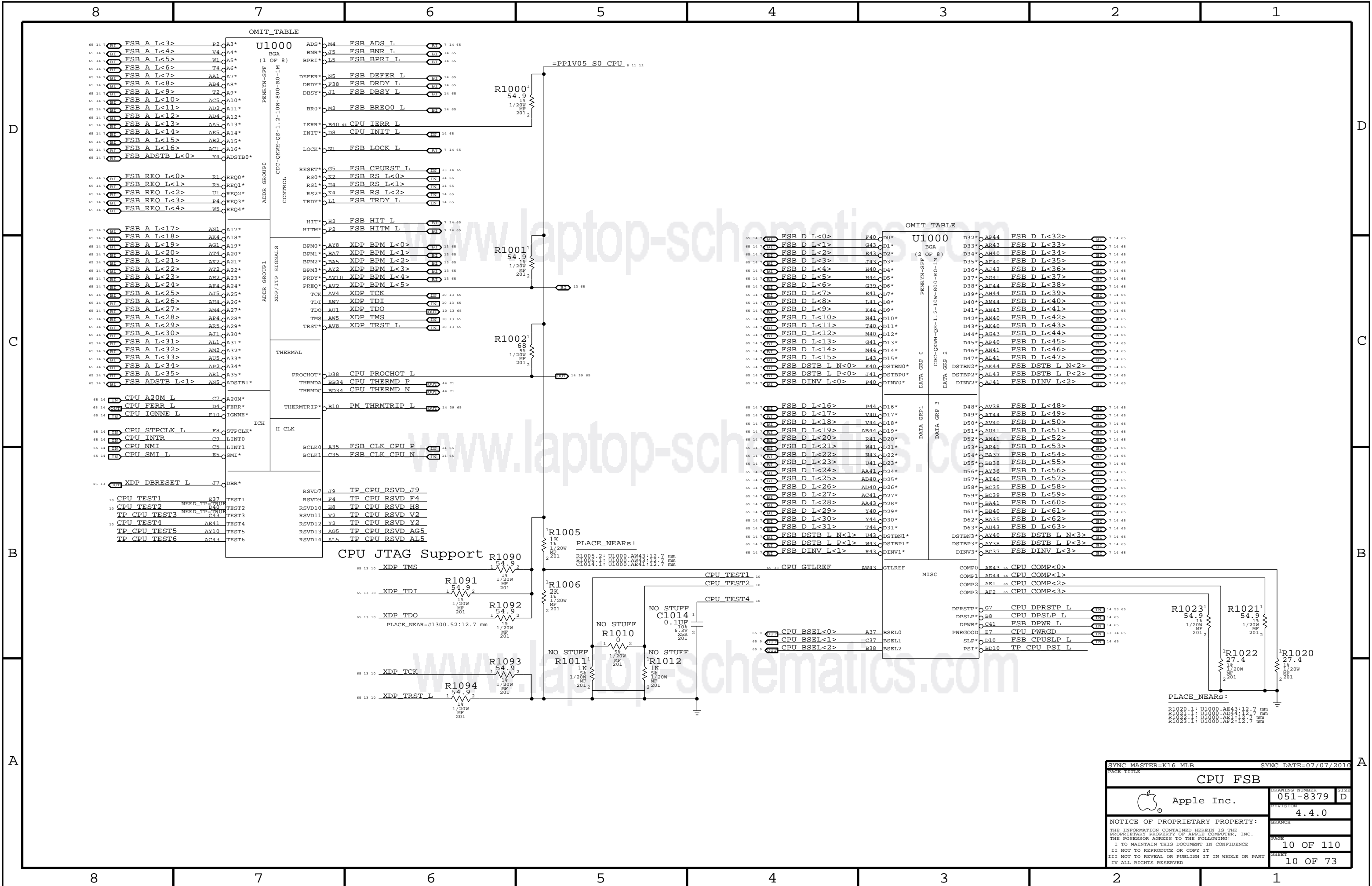
FSB SIGNALS WITH NOTEST

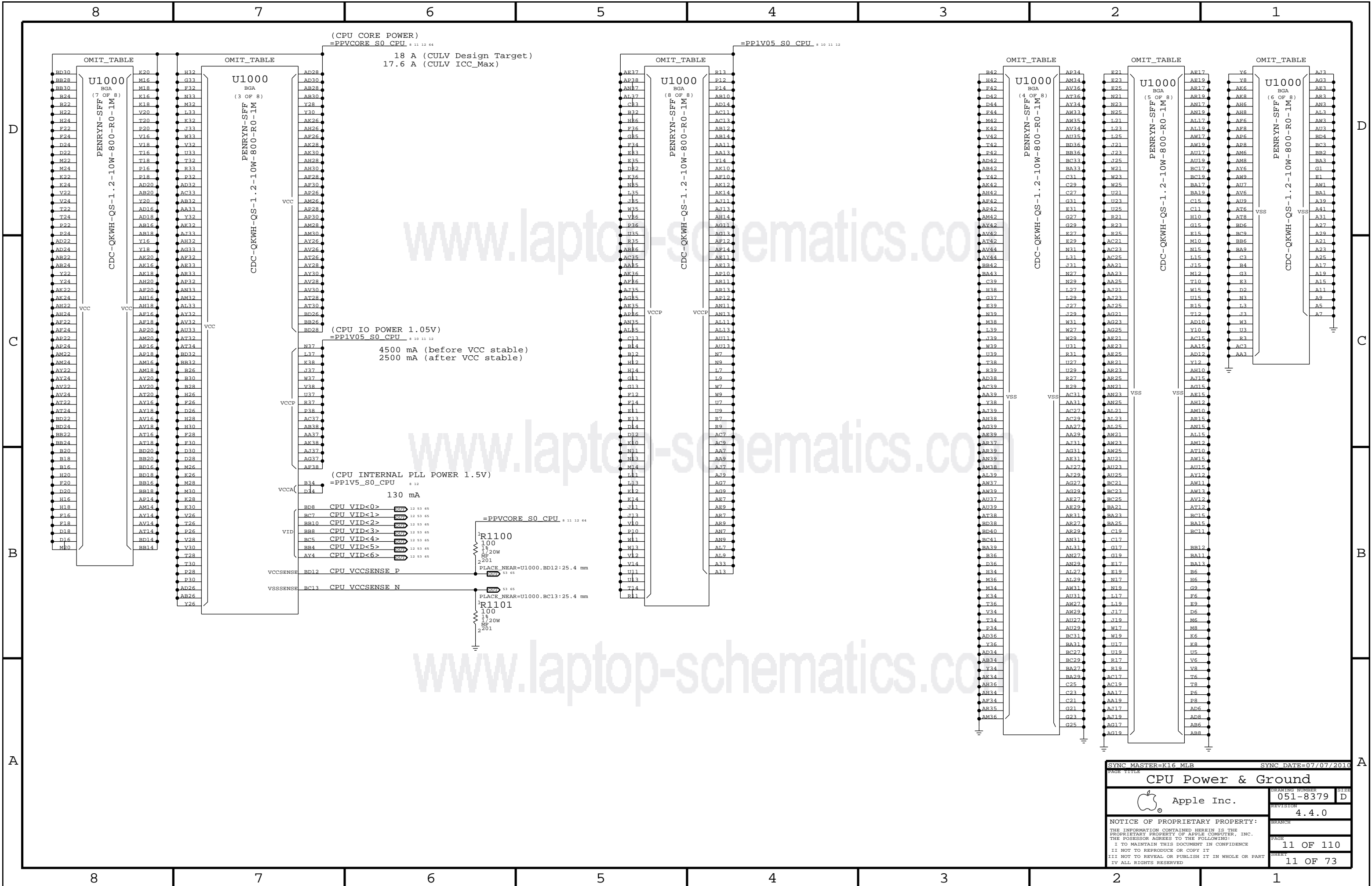
NO_TEST=TRUE	FSB_A_L<35..3>	10 14 65
NO_TEST=TRUE	FSB_ADS_L	10 14 65
NO_TEST=TRUE	FSB_ADSTB_L<1..0>	10 14 65
NO_TEST=TRUE	FSB_D_L<63..0>	10 14 65
NO_TEST=TRUE	FSB_DINV_L<3..0>	10 14 65
NO_TEST=TRUE	FSB_DSTB_L_N<3..0>	10 14 65
NO_TEST=TRUE	FSB_DSTB_L_P<3..0>	10 14 65
NO_TEST=TRUE	FSB_HIT_L	10 14 65
NO_TEST=TRUE	FSB_HITM_L	10 14 65
NO_TEST=TRUE	FSB_LOCK_L	10 14 65
NO_TEST=TRUE	FSB_REO_L<4..0>	10 14 65

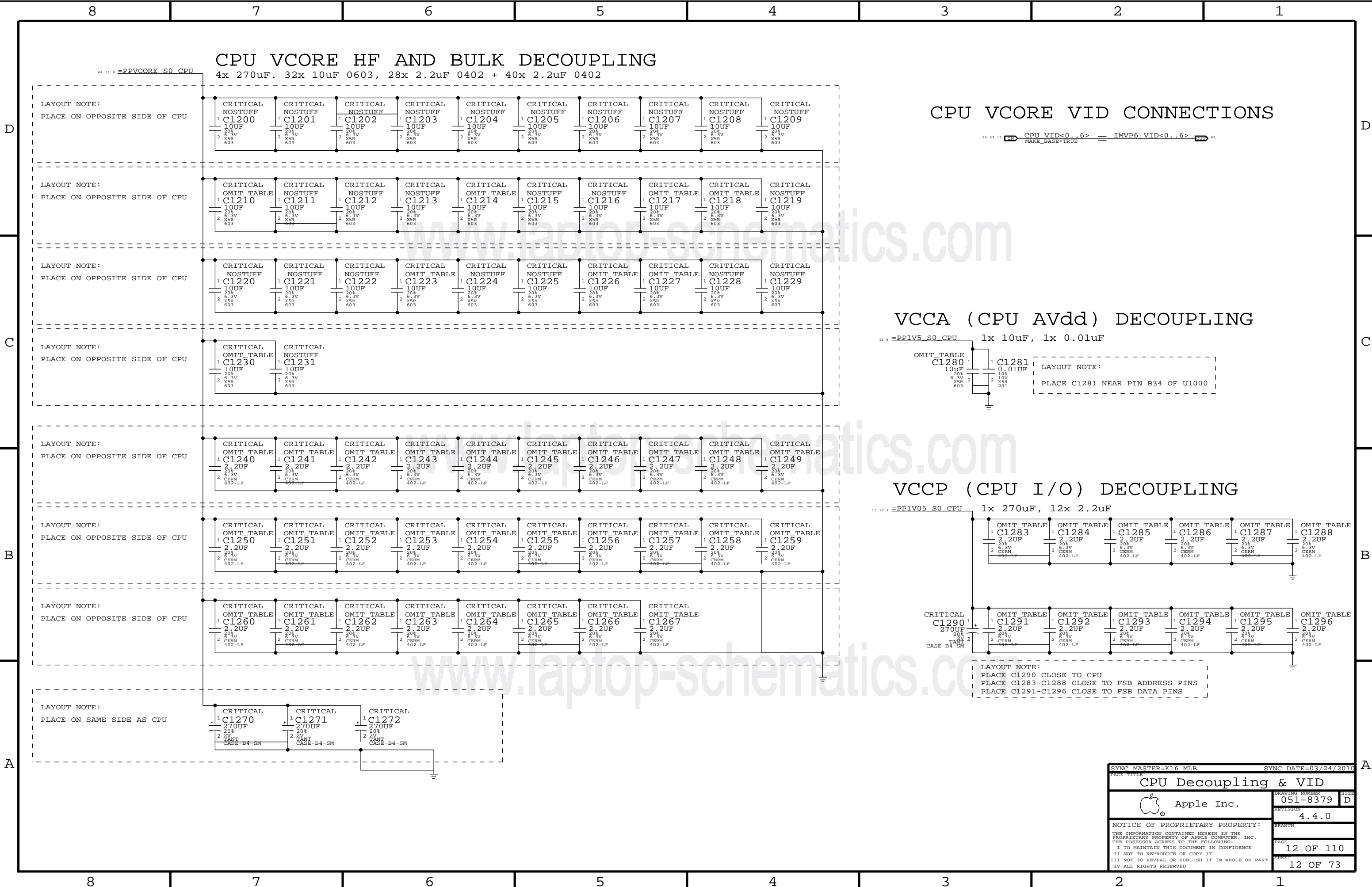
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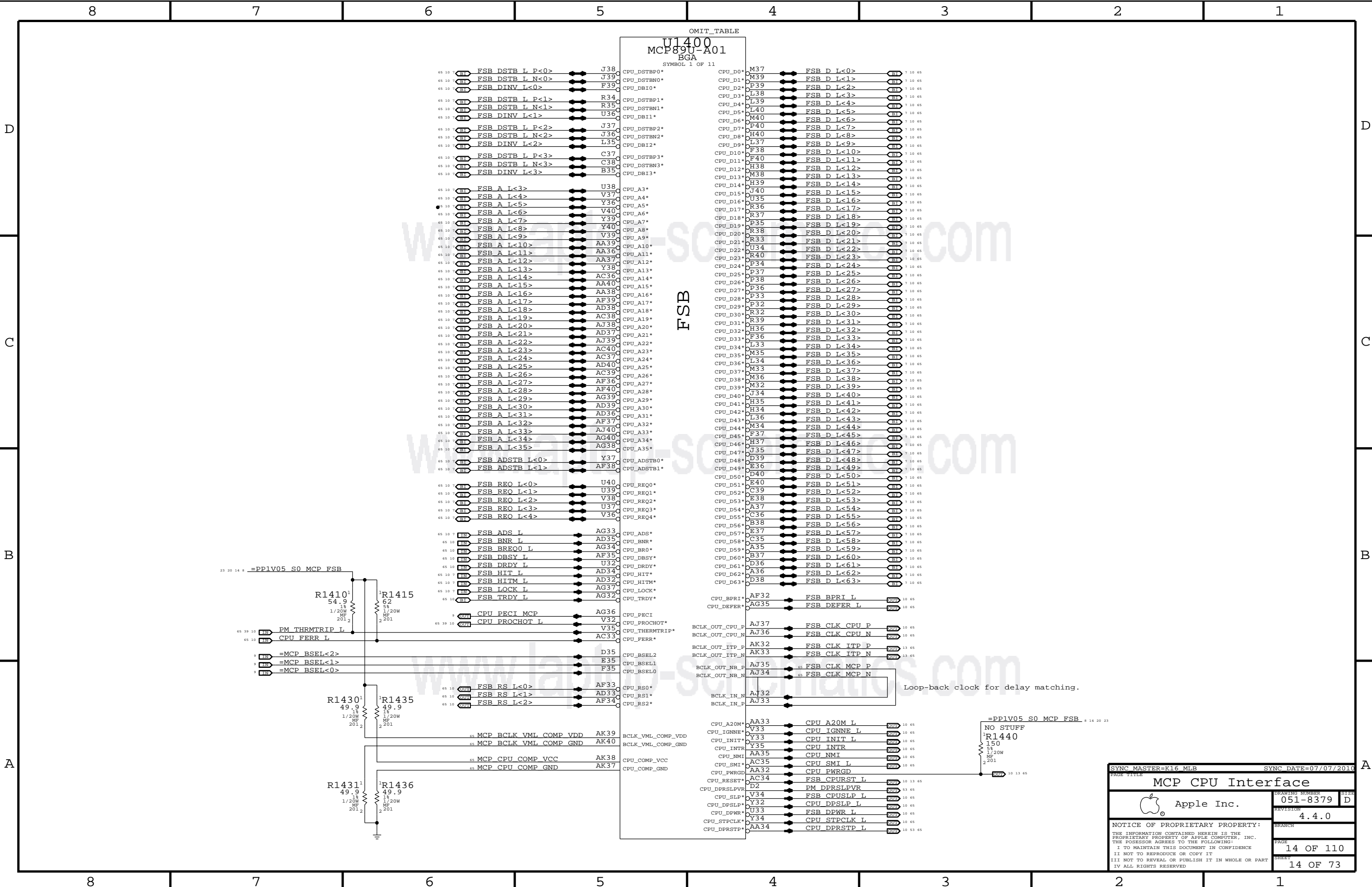
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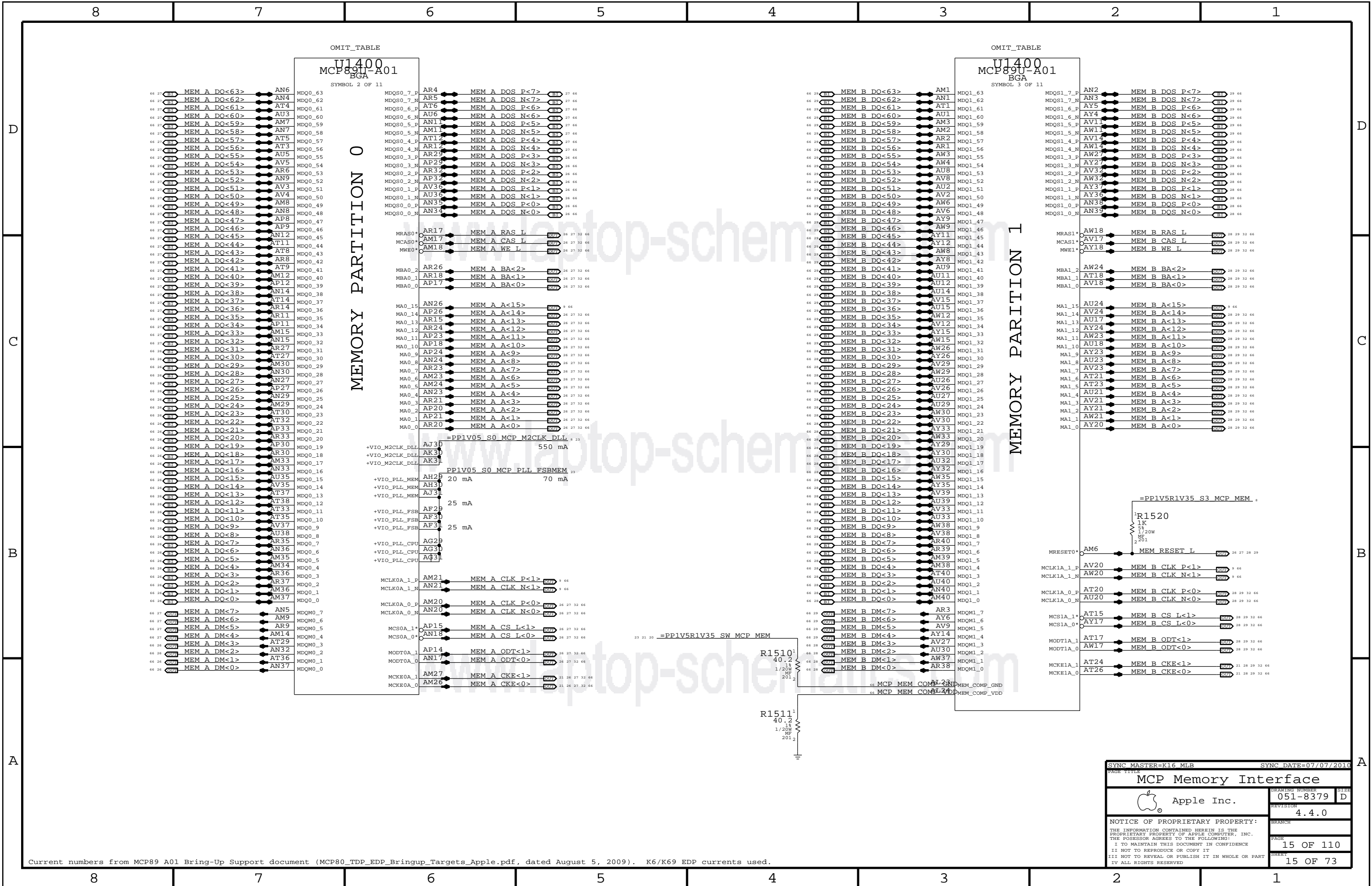
4

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SYNC DATE=07/07/2010

MCP Memory Interface

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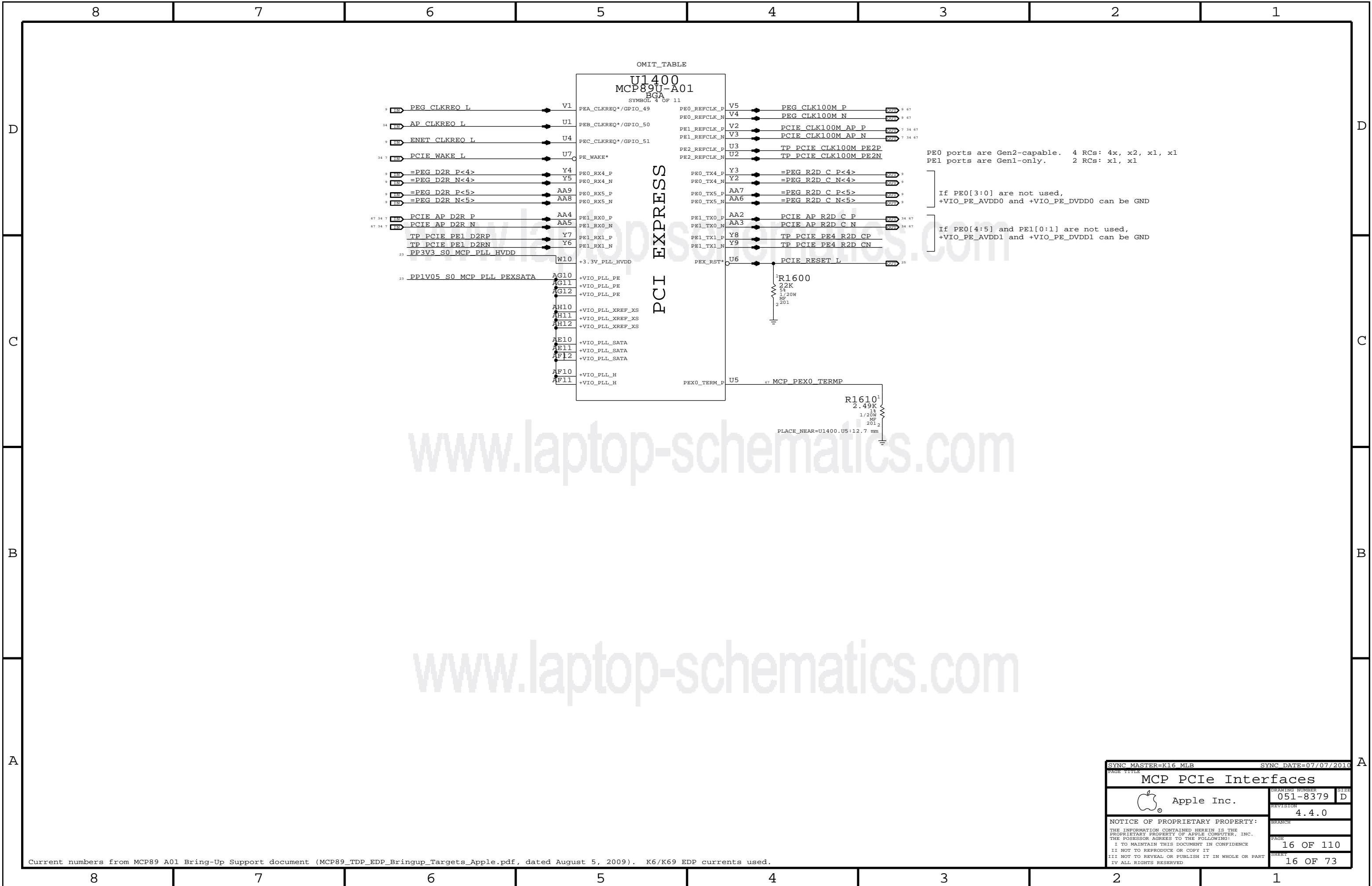
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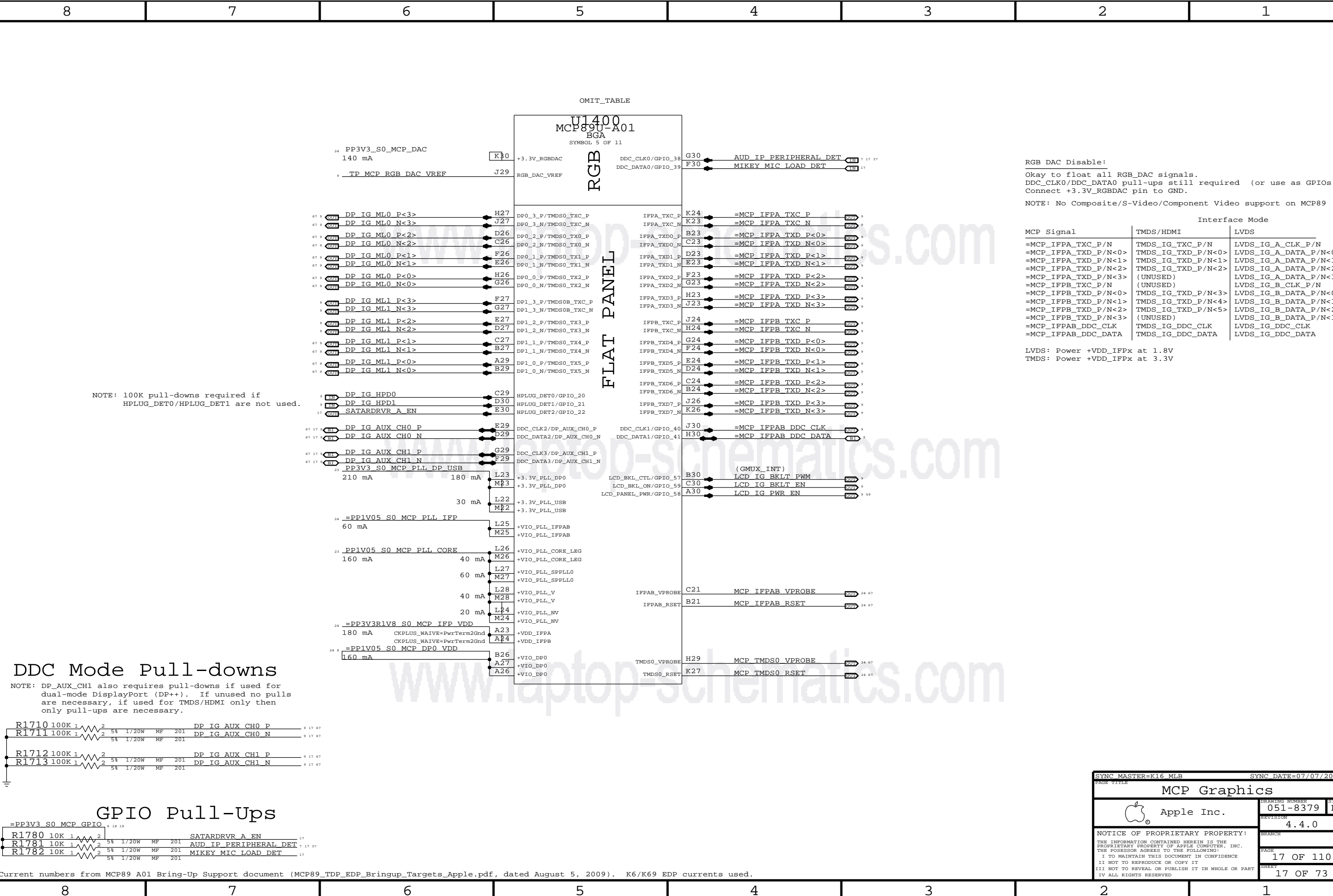
A

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A



RGB DAC Disable:  
Okay to float all RGB\_DAC signals.  
DDC\_CLK0/DDC\_DATA0 pull-ups still required (or use as GPIOs).  
Connect +3.3V\_RGBDAC pin to GND.  
NOTE: No Composite/S-Video/Component Video support on MCP89

SYNC MASTER=K16 MLB

SYNC DATE=07/07/2010

MCP Graphics

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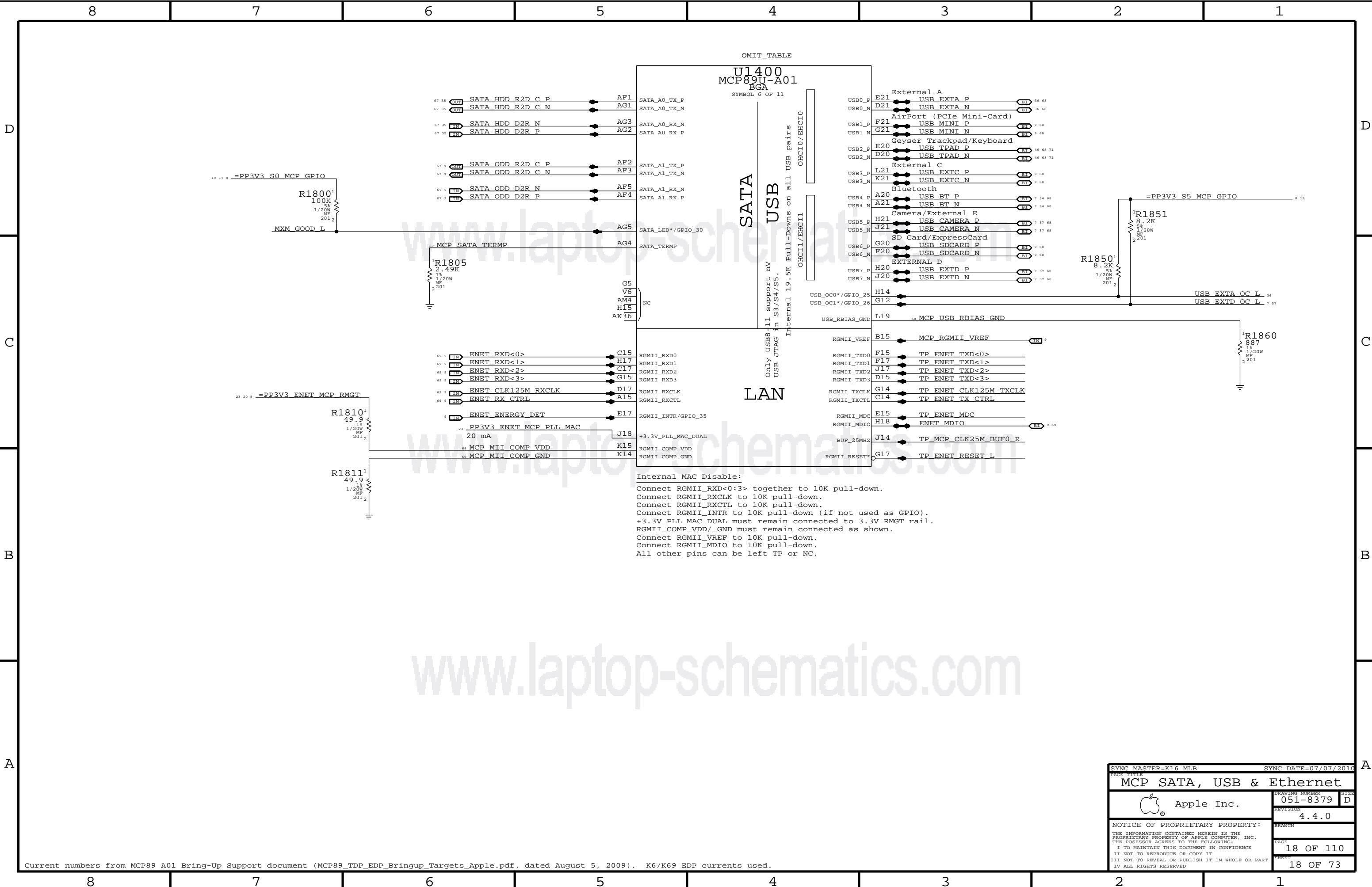
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Internal MAC Disable:  
Connect RGMII\_RXD<0:3> together to 10K pull-down.  
Connect RGMII\_RXCLK to 10K pull-down.  
Connect RGMII\_RXCTL to 10K pull-down.  
Connect RGMII\_INTR to 10K pull-down (if not used as GPIO).  
+3.3V\_PLL\_MAC\_DUAL must remain connected to 3.3V RMGT rail.  
RGMII\_COMP\_VDD/\_GND must remain connected as shown.  
Connect RGMII\_VREF to 10K pull-down.  
Connect RGMII\_MDIO to 10K pull-down.  
All other pins can be left TP or NC.

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MCP SATA, USB & Ethernet

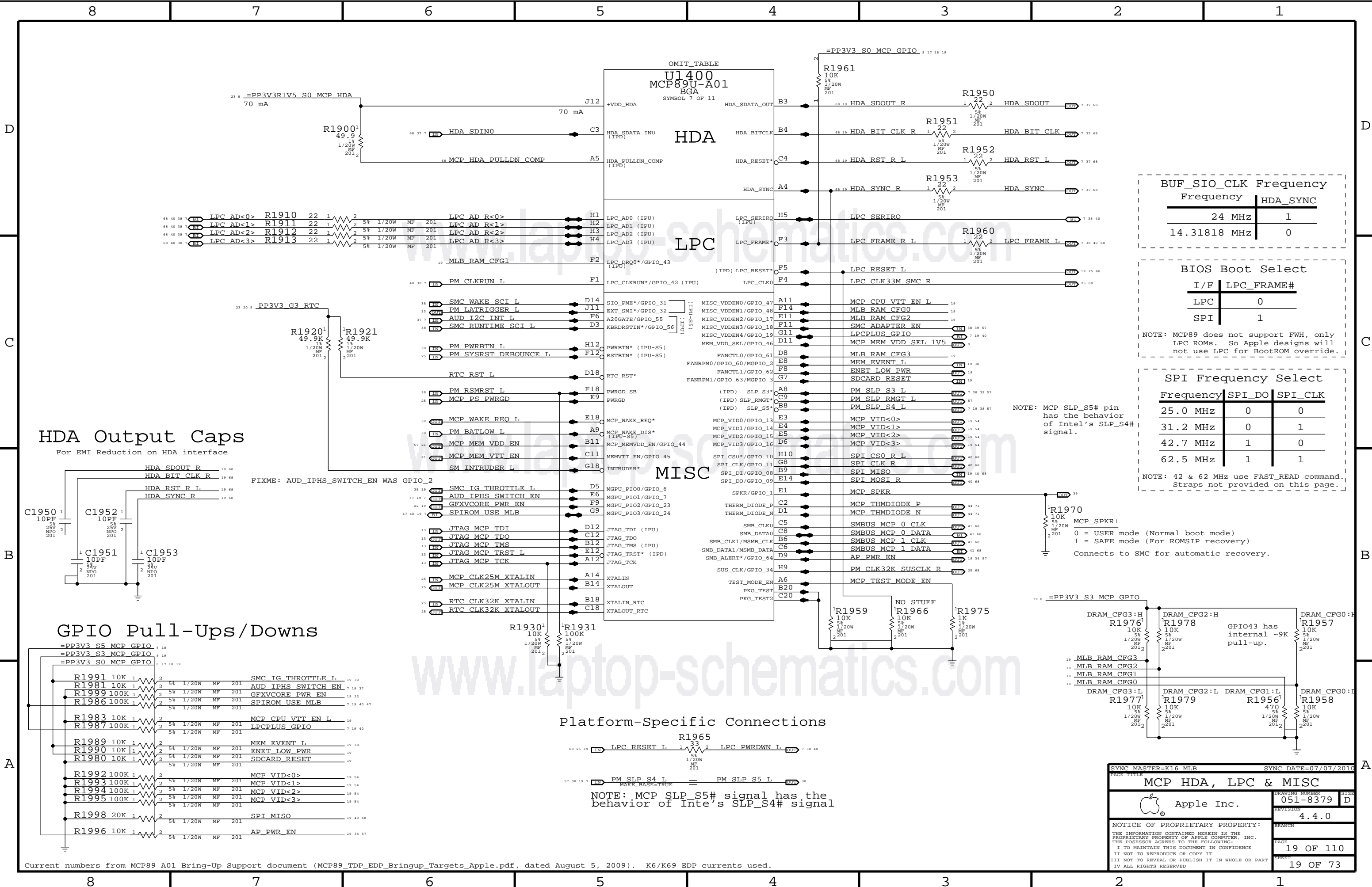
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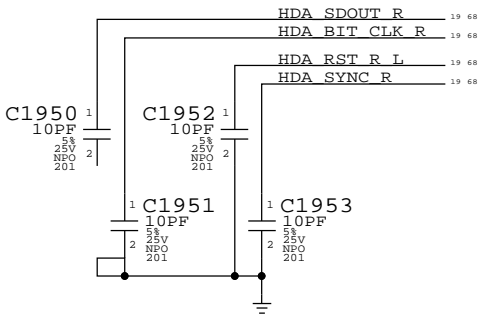
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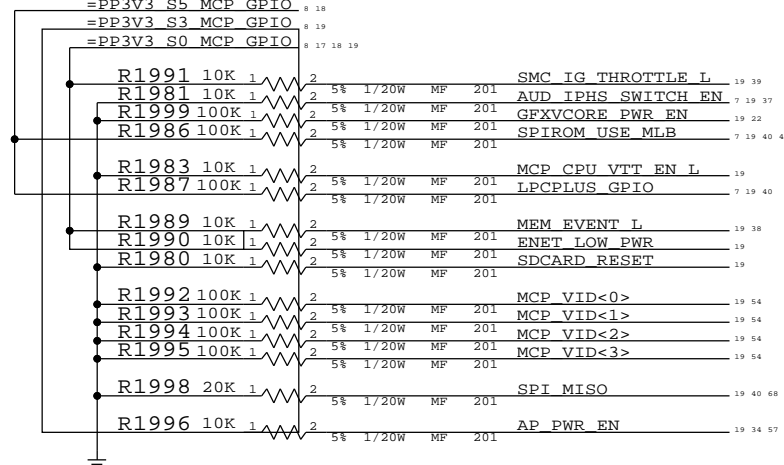


HDA Output Caps

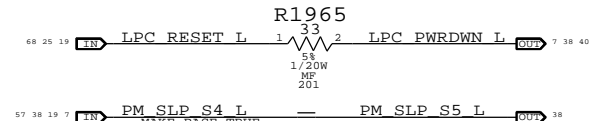
For EMI Reduction on HDA interface



GPIO Pull-Ups/Downs



Platform-Specific Connections



NOTE: MCP SLP\_S5# signal has the behavior of Intel's SLP\_S4# signal

BUF_SIO_CLK Frequency	
Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

BIOS Boot Select

I/F	LPC_FRAME#
LPC	0
SPI	1

NOTE: MCP89 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
42.7 MHz	1	0
62.5 MHz	1	1

NOTE: 42 & 62 Mhz use FAST\_READ command. Straps not provided on this page.

NOTE: MCP SLP\_S5# pin has the behavior of Intel's SLP\_S4# signal.

MCP\_SPKR:  
0 = USER mode (Normal boot mode)  
1 = SAFE mode (For ROMSIP recovery)  
Connects to SMC for automatic recovery.

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SYNC DATE=07/07/2010

MCP HDA, LPC & MISC

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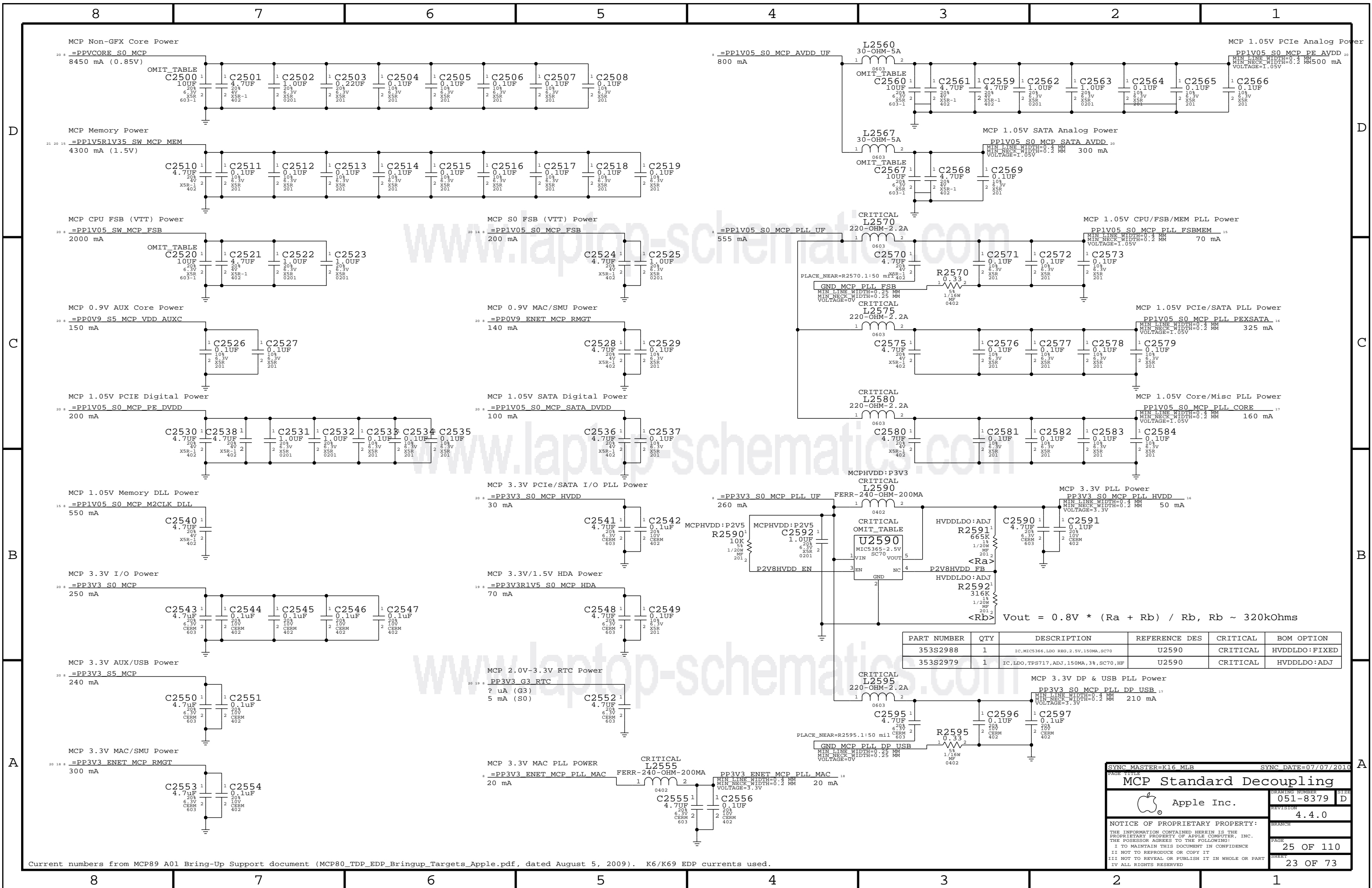
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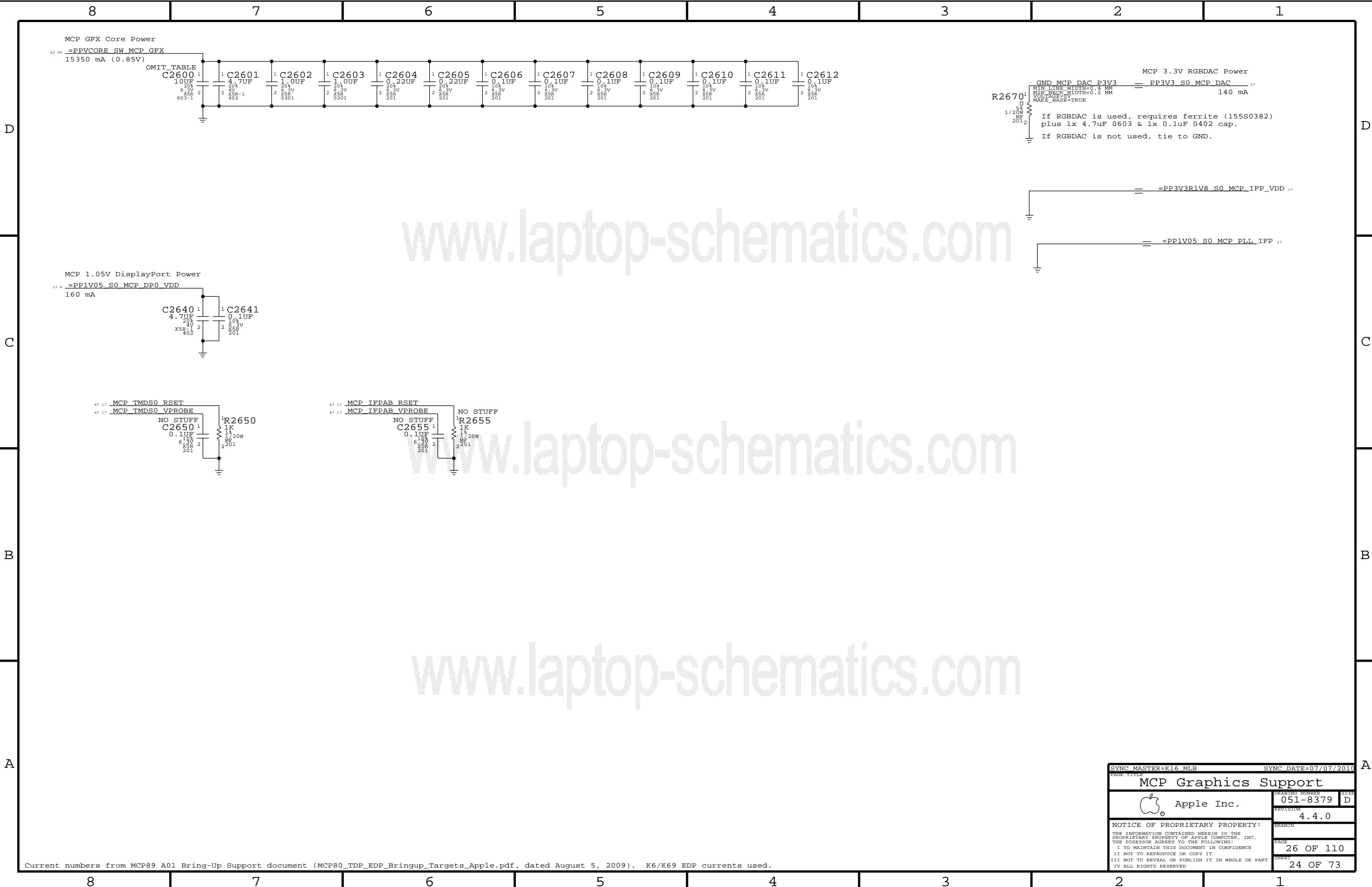





PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2988	1	IC, MIC5366, LDO REG, 2.5V, 150mA, SC70	U2590	CRITICAL	HVDDLDO: FIXED
353S2979	1	IC, LDO, TPS717, ADJ, 150mA, 3%, SC70, HF	U2590	CRITICAL	HVDDLDO: ADJ

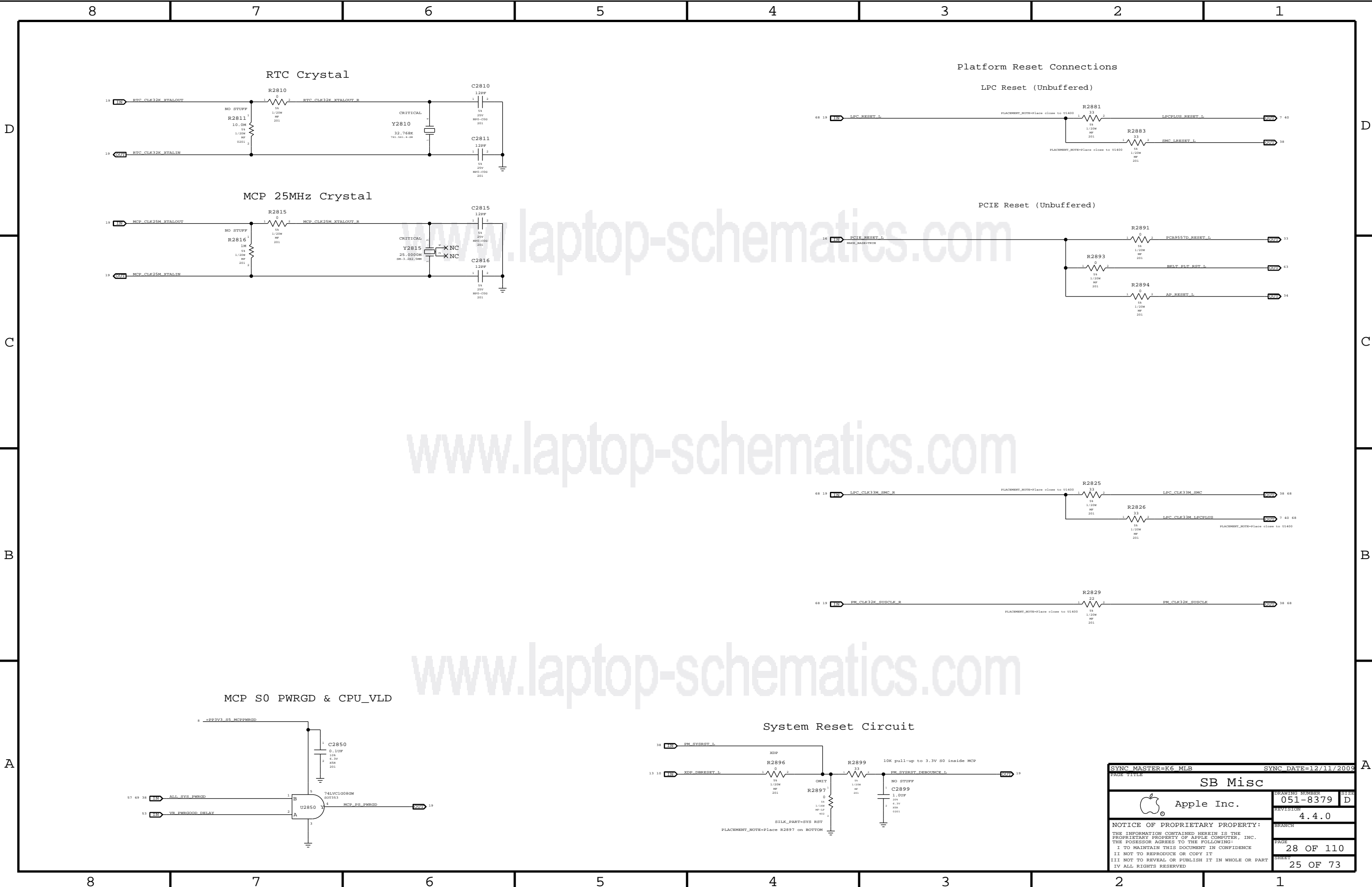
$$V_{out} = 0.8V * (R_a + R_b) / R_b, R_b \sim 320k\Omega$$

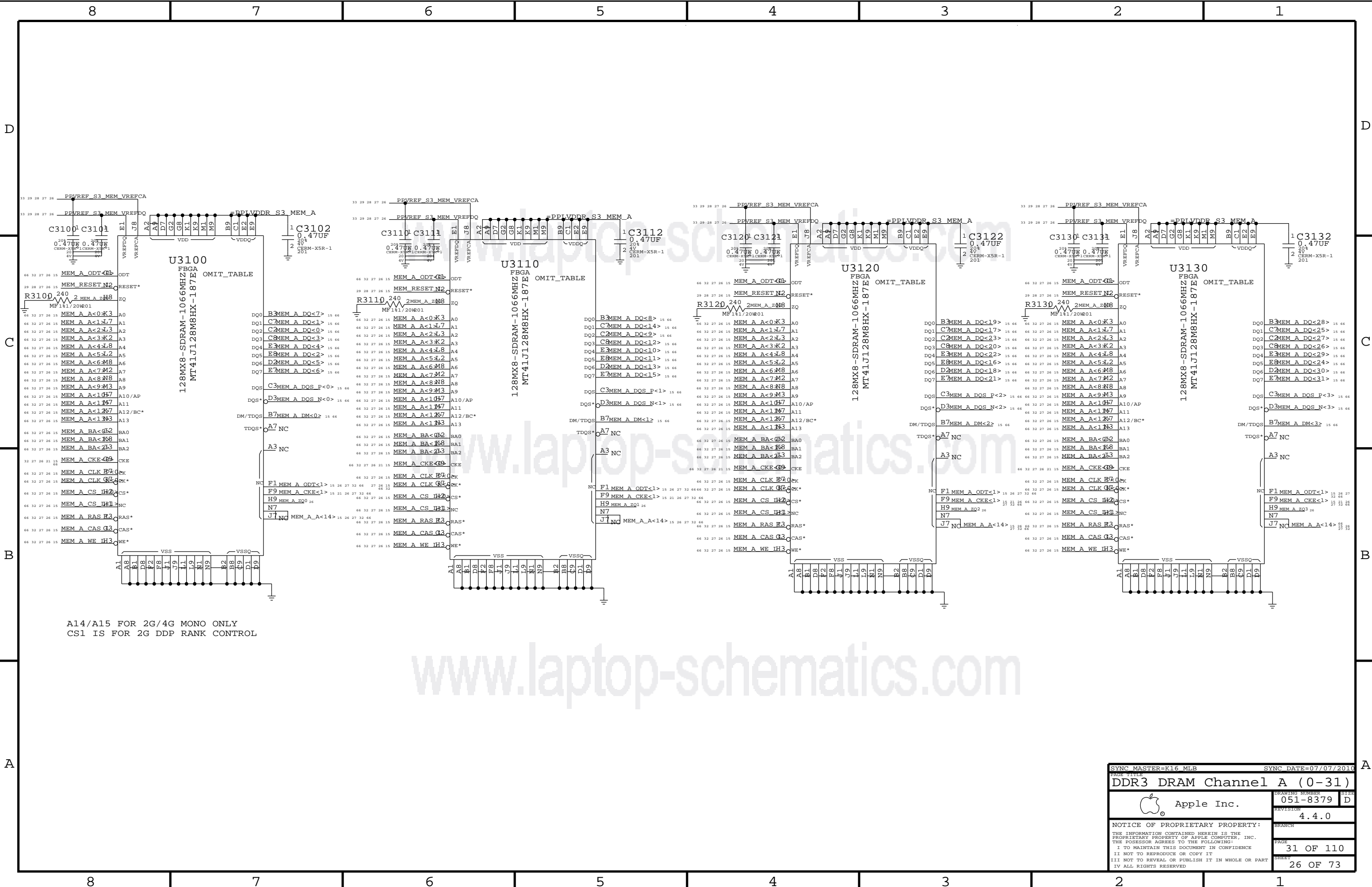
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Current numbers from MCP89 A01 Bring-Up Support document (MCP80\_TDP\_EDP\_Bringup\_Targets\_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

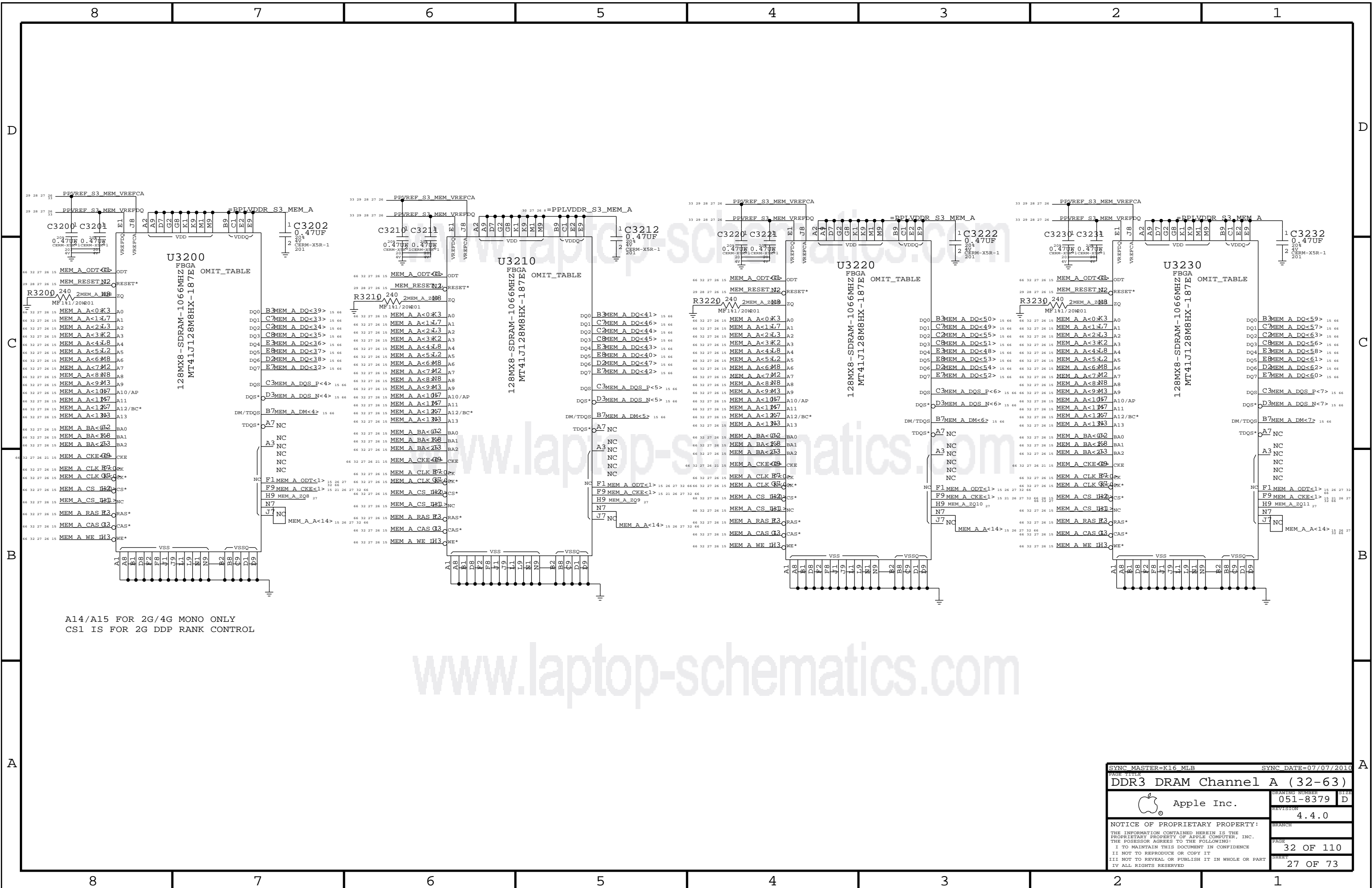
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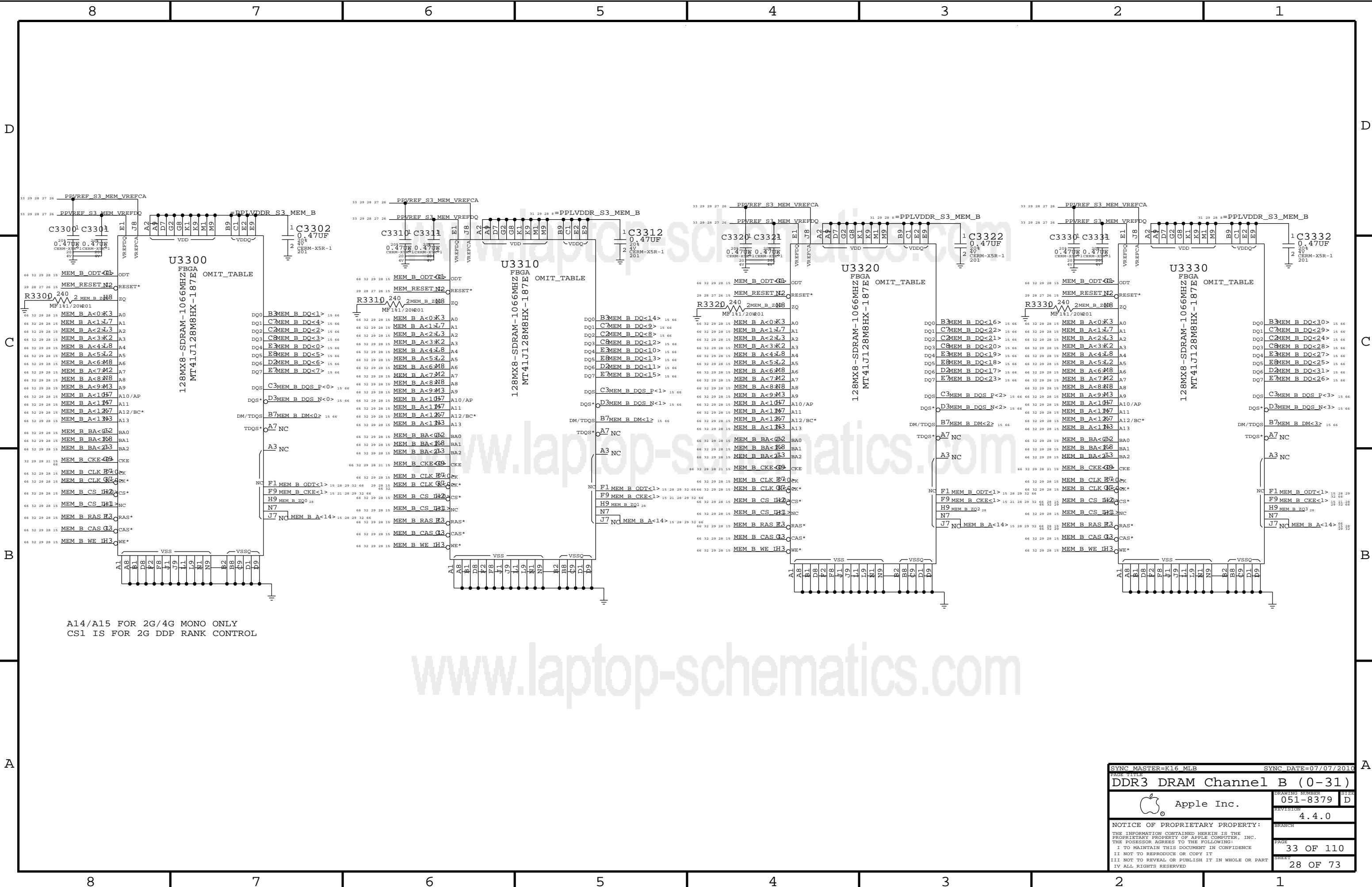
A14/A15 FOR 2G/4G MONO ONLY  
CS1 IS FOR 2G DDP RANK CONTROL

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DDR3 DRAM Channel A		(0-31)	
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


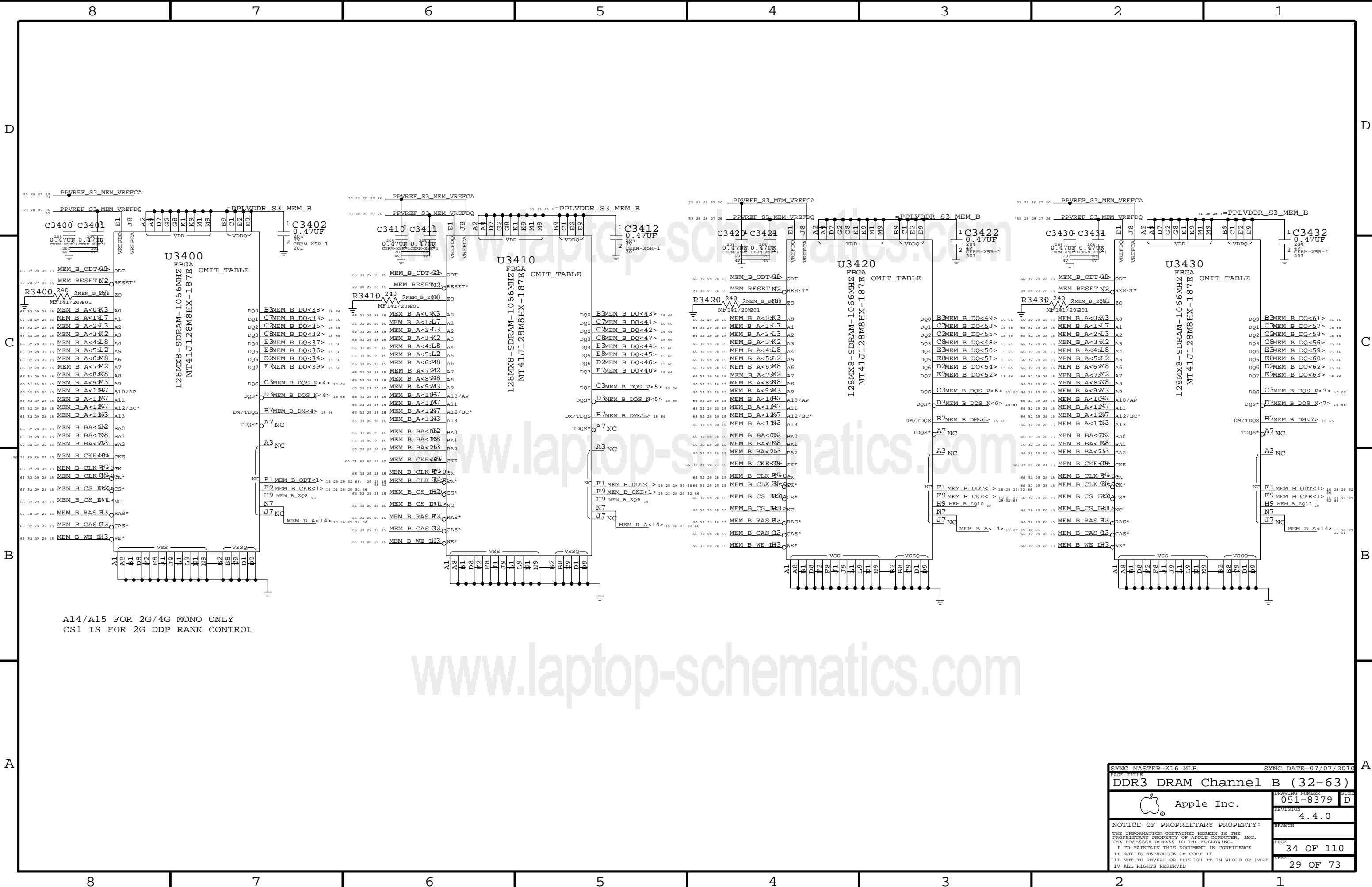
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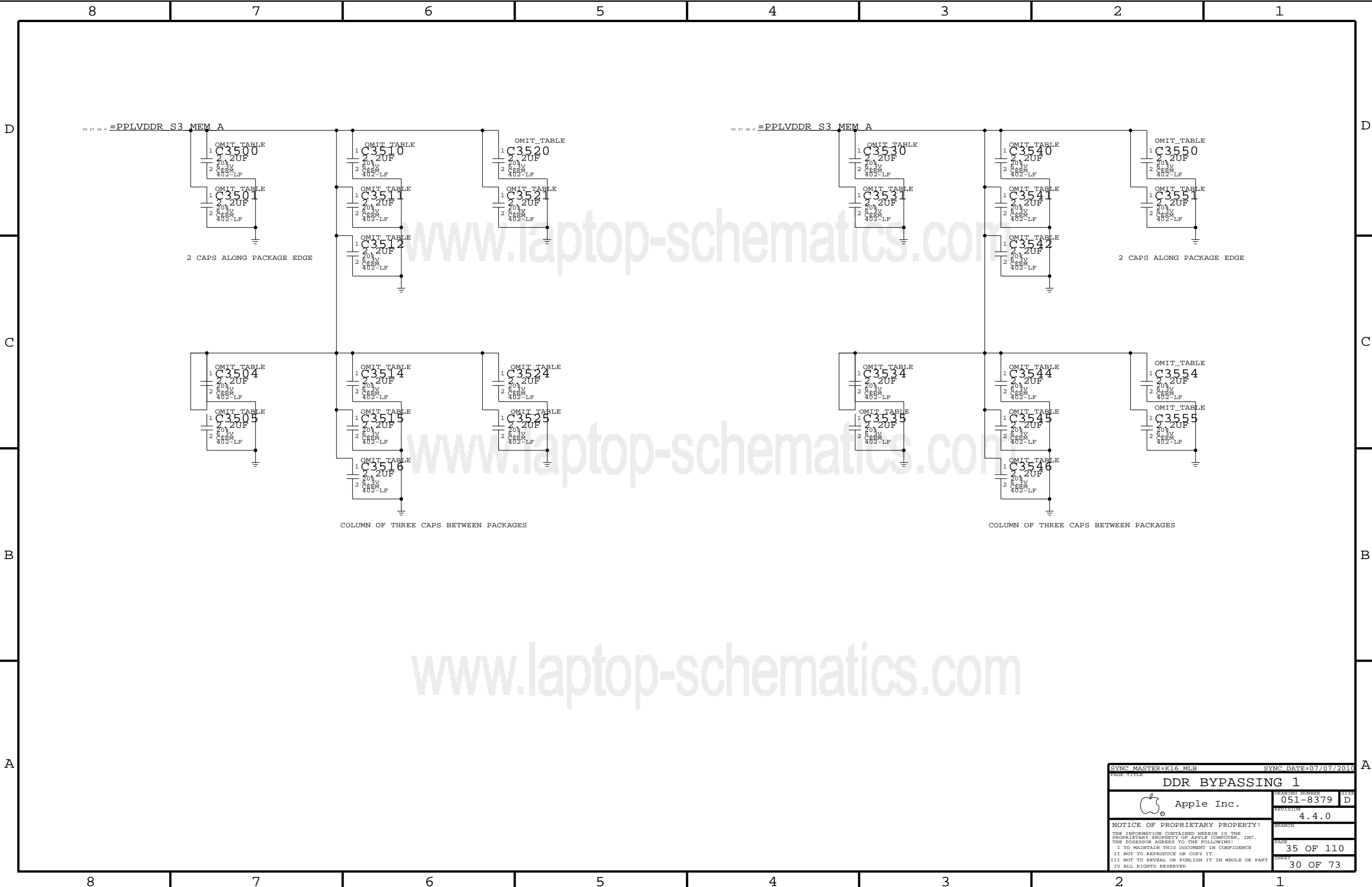
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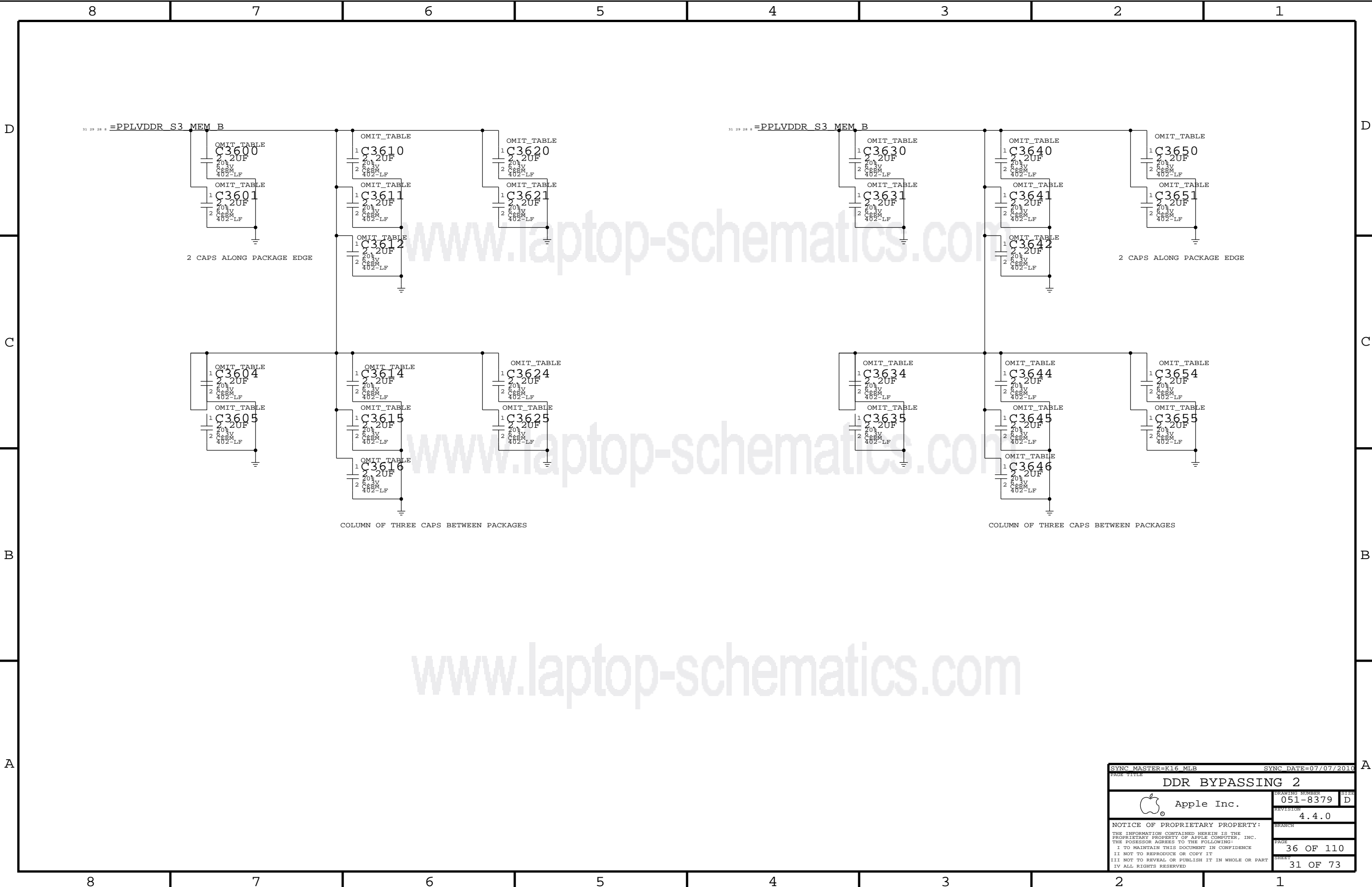
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CS1 IS FOR 2G DDP RANK CONTROL

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		PAGE	34 OF 110
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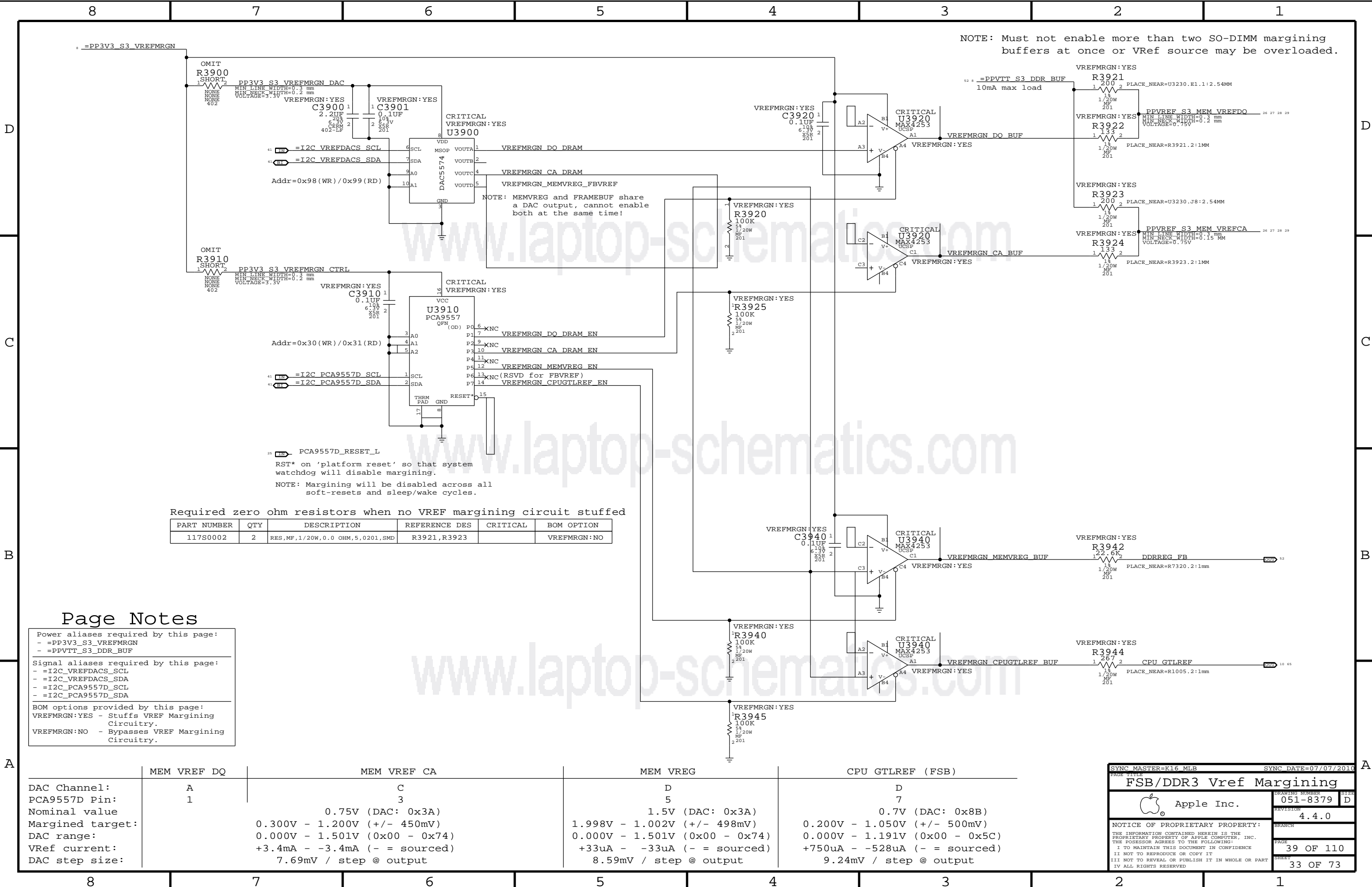
8	7	6	5	4	3	2	1
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D



D

A



Page Notes

Power aliases required by this page:  
- =PP3V3\_S3\_VREFMRGN  
- =PPVTT\_S3\_DDR\_BUF

Signal aliases required by this page:  
- =I2C\_VREFDACS\_SCL  
- =I2C\_VREFDACS\_SDA  
- =I2C\_PCA9557D\_SCL  
- =I2C\_PCA9557D\_SDA

BOM options provided by this page:  
VREFMRGN:YES - Stuffs VREF Margining Circuitry.  
VREFMRGN:NO - Bypasses VREF Margining Circuitry.

	MEM VREF DQ	MEM VREF CA	MEM VREG	CPU GTLREF (FSB)
DAC Channel:	A	C	D	D
PCA9557D Pin:	1	3	5	7
Nominal value		0.75V (DAC: 0x3A)	1.5V (DAC: 0x3A)	0.7V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)	1.998V - 1.002V (+/- 498mV)	0.200V - 1.050V (+/- 500mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)	0.000V - 1.501V (0x00 - 0x74)	0.000V - 1.191V (0x00 - 0x5C)
Vref current:		+3.4mA - -3.4mA (- = sourced)	+33uA - -33uA (- = sourced)	+750uA - -528uA (- = sourced)
DAC step size:		7.69mV / step @ output	8.59mV / step @ output	9.24mV / step @ output

SYNC MASTER=K16 MLB

SYNC DATE=07/07/2010

FSB/DDR3 Vref Margining

Apple Inc.

051-8379

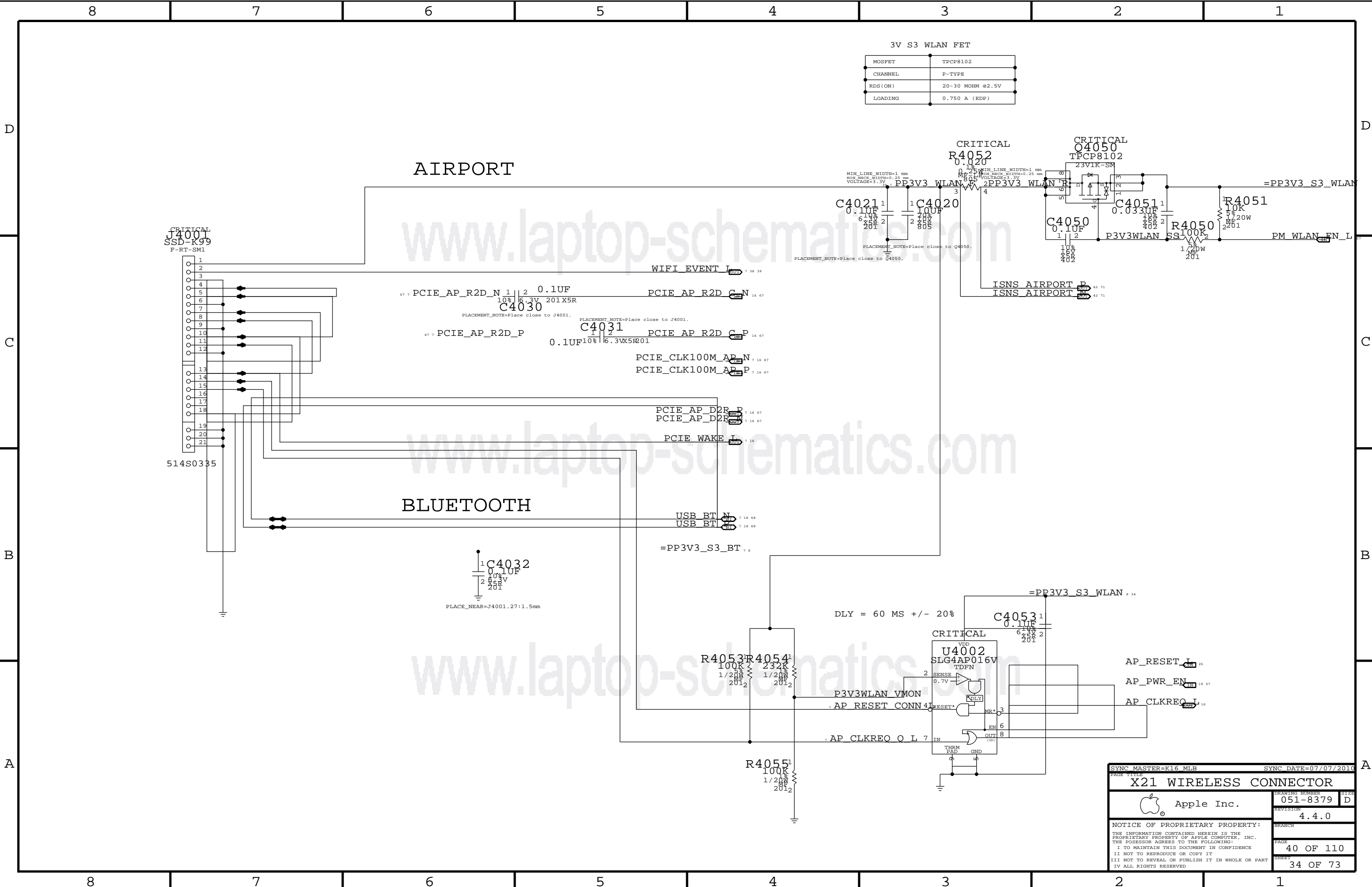
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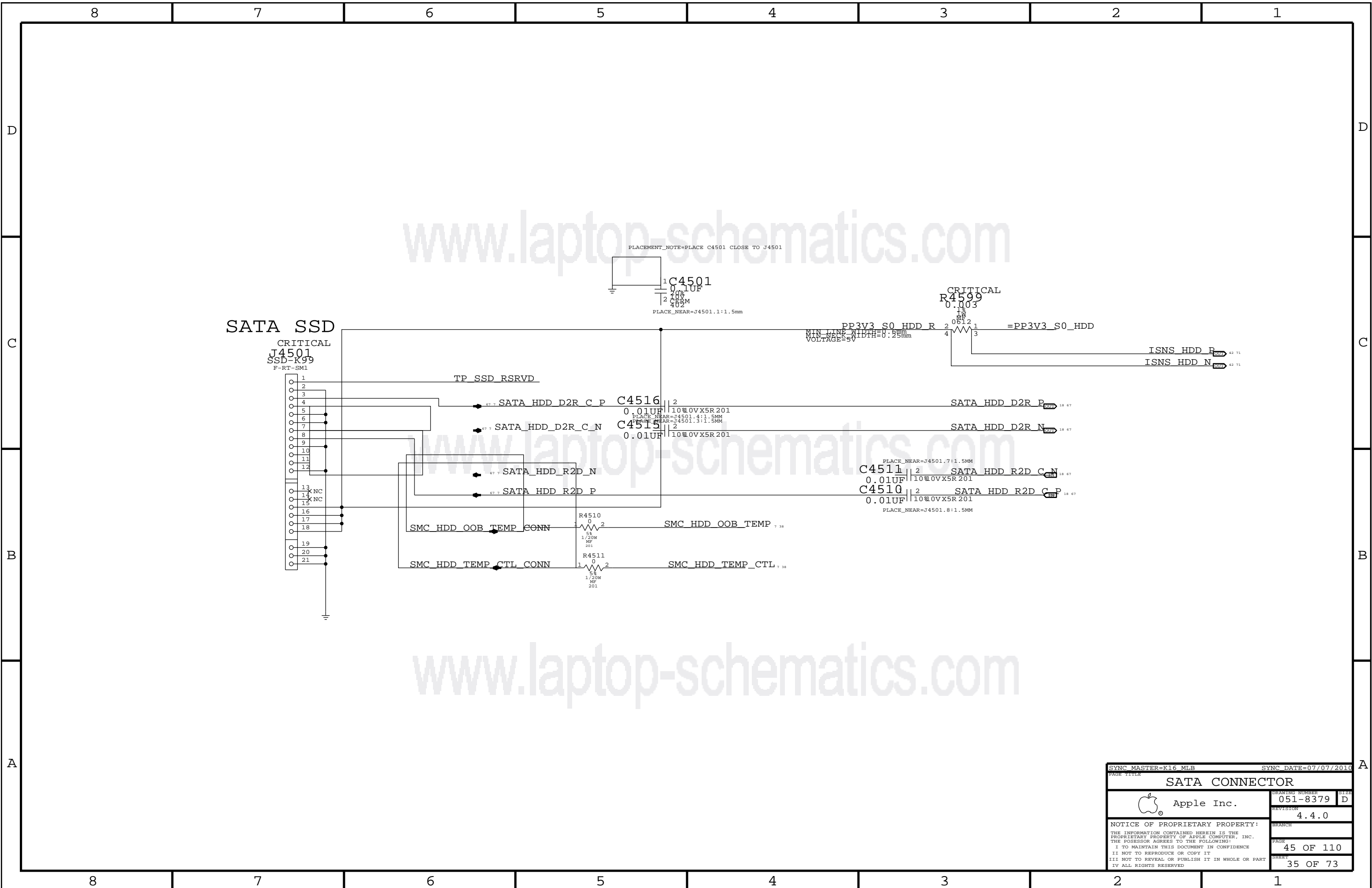
39 OF 110


33 OF 73



3V S3 WLAN FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS (ON)	20-30 MOHM @2.5V
LOADING	0.750 A (EDP)

SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
PAGE TITLE		X21 WIRELESS CONNECTOR	
DRAWING NUMBER		051-8379	SIZE D
REVISION		4.4.0	BRANCH
PAGE		40 OF 110	SHEET
SHEET		34 OF 73	



SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
PAGE TITLE			
SATA CONNECTOR			
 Apple Inc.		DRAWING NUMBER	051-8379
		REVISION	4.4.0
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		PAGE	45 OF 110
		SHEET	35 OF 73
		SIZE	D

D

C

B

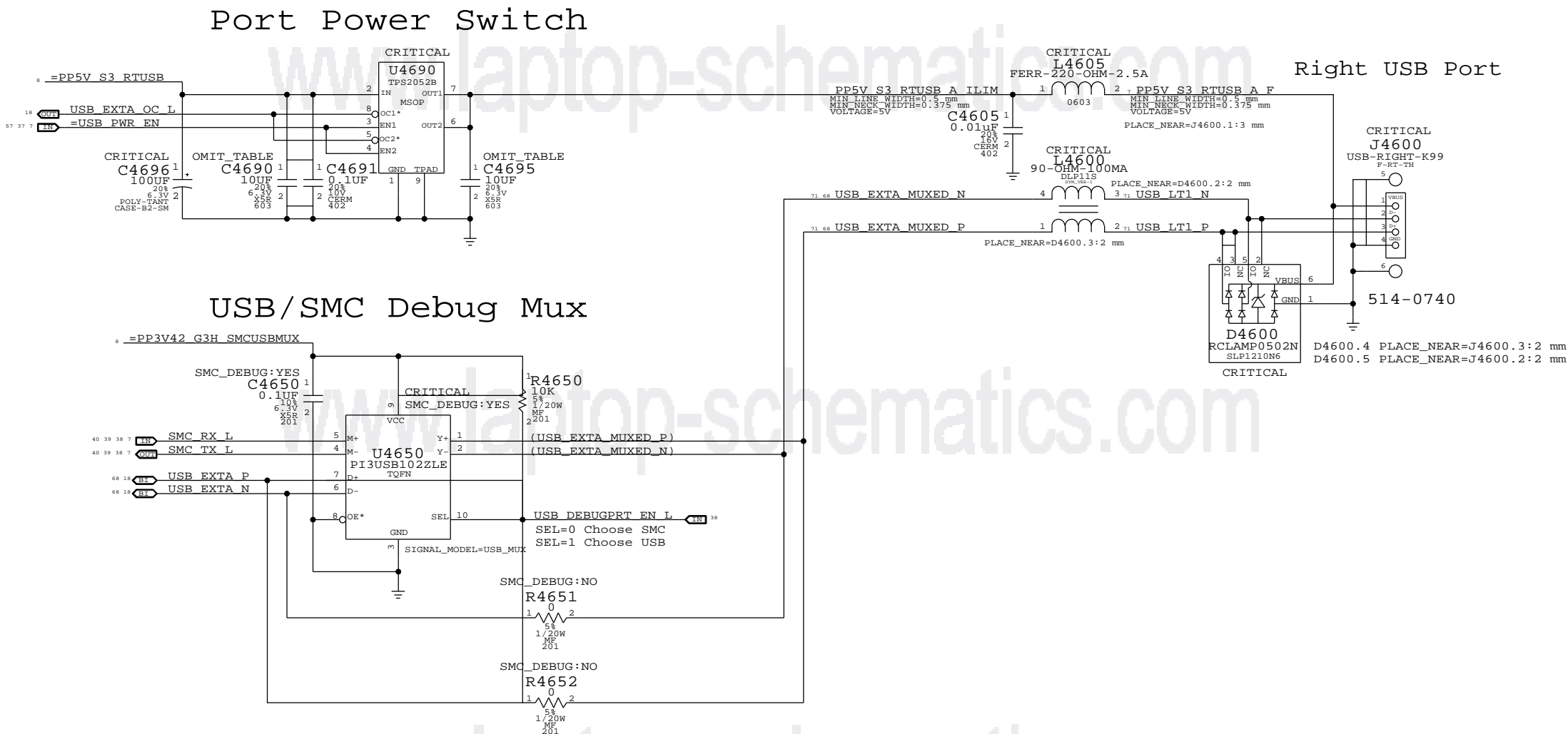
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
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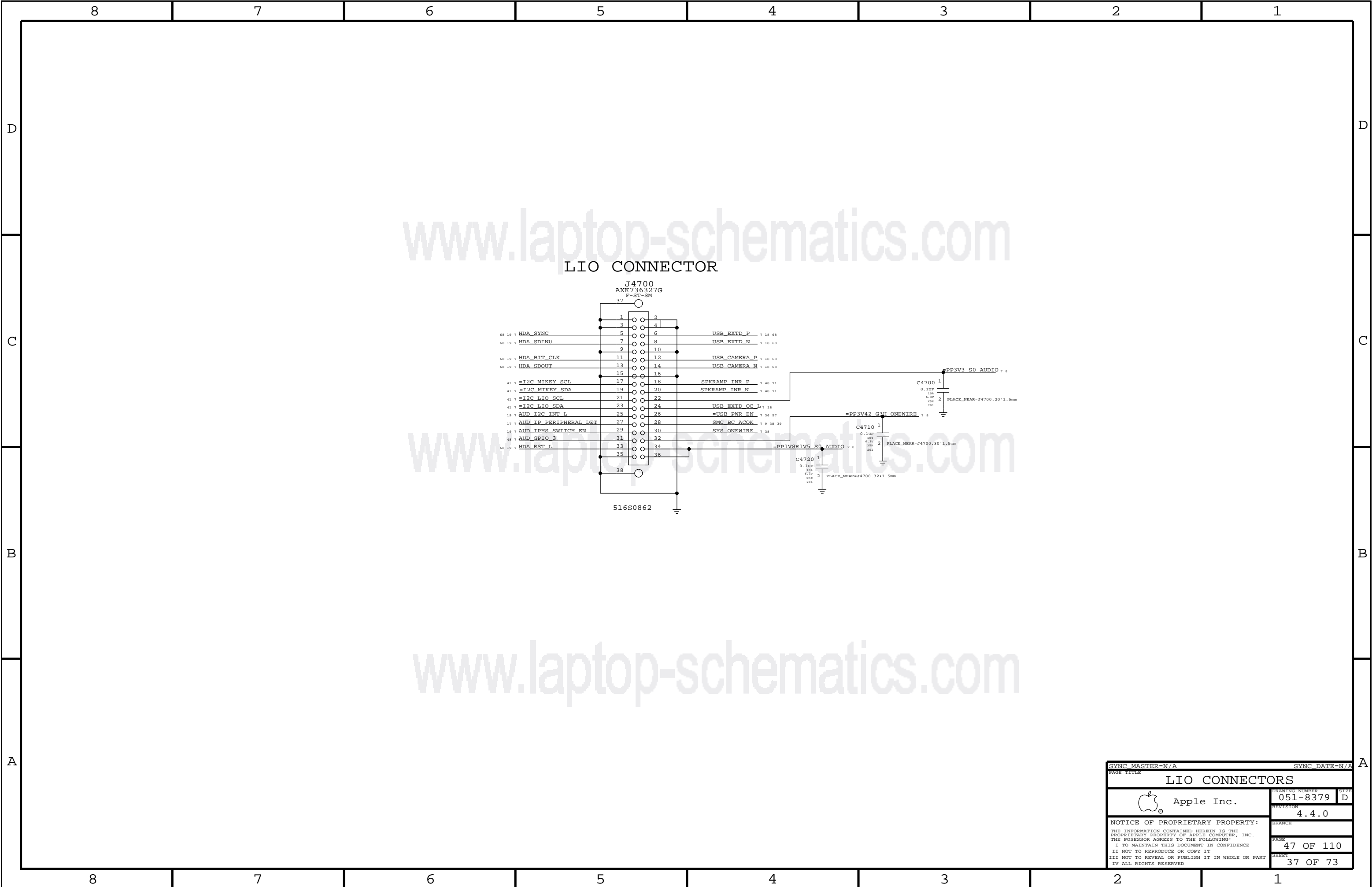
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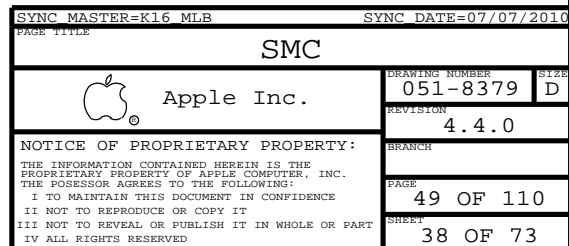
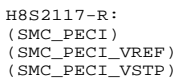
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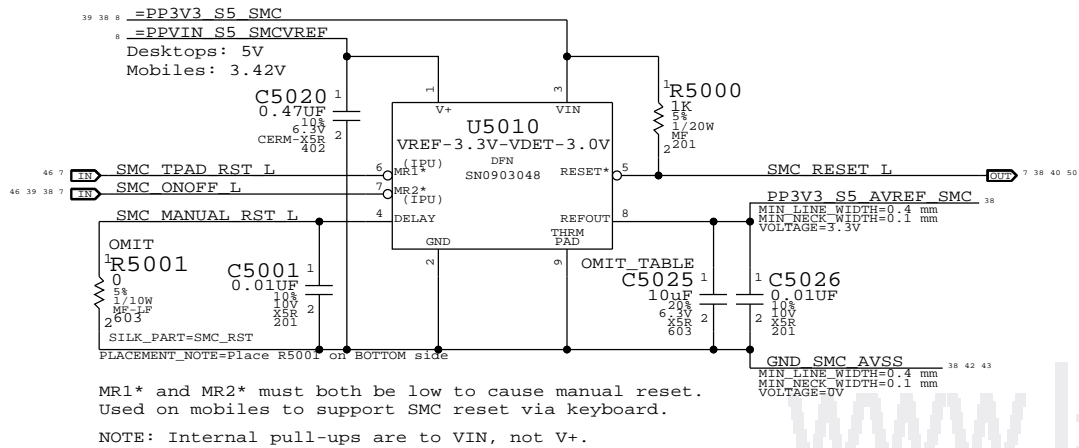
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PAGE TITLE			
External USB Connectors			
 Apple Inc.		DRAWING NUMBER	051-8379
		REVISION	4.4.0
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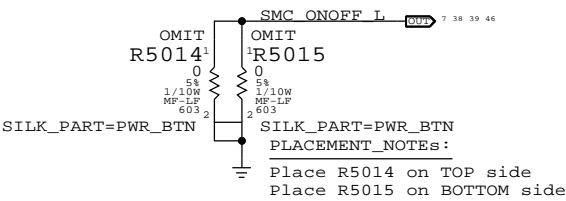
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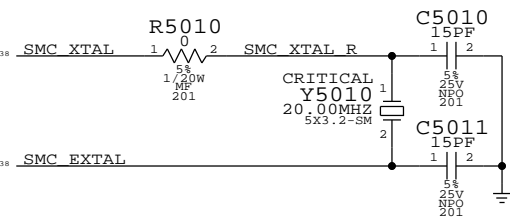
SMC Reset "Button", Supervisor & AVREF Supply



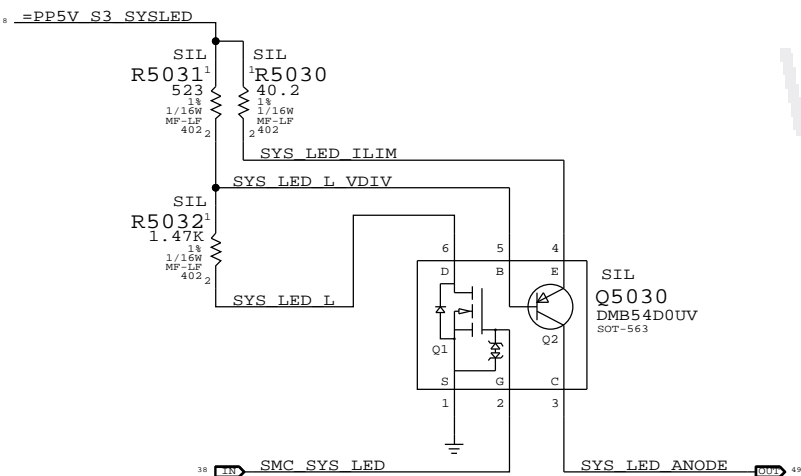
Debug Power "Buttons"



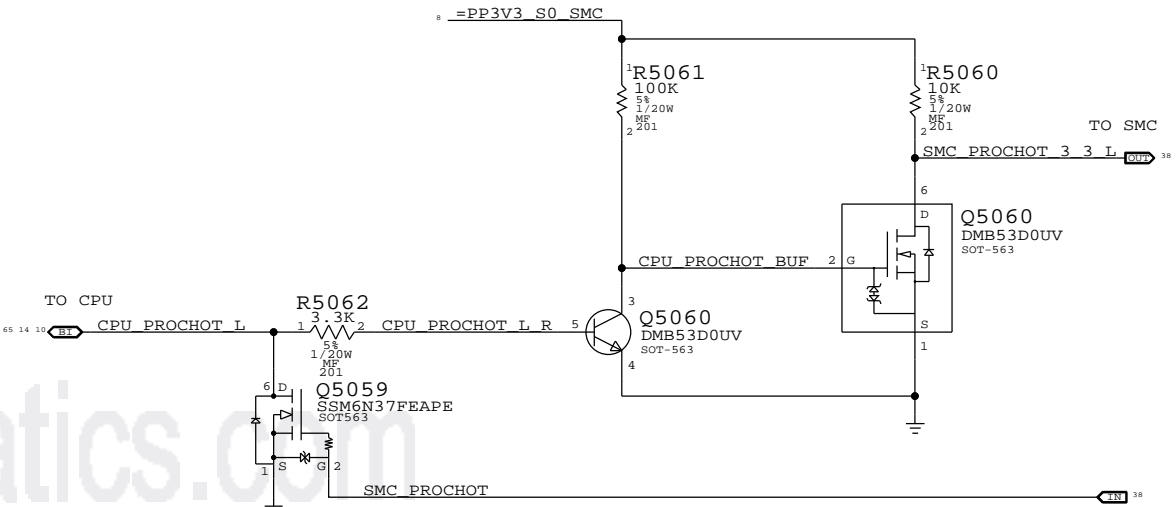
SMC Crystal Circuit



System (Sleep) LED Circuit

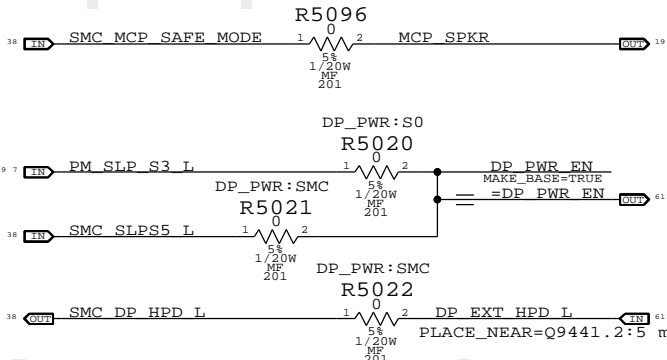


SMC FSB to 3.3V Level Shifting



SMC Aliases

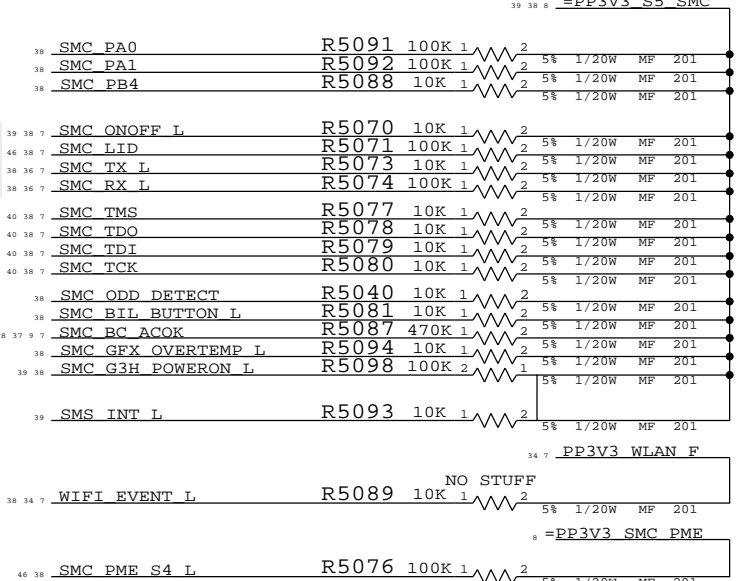
SMC LCDCLK ISENSE	=	SMS X AXIS
SMC WLAN ISENSE	=	SMS Y AXIS
SMC HDD ISENSE	=	SMS Z AXIS
SMC CSREG ISENSE	=	SMC ADC14
SMC LCDCLK VSENSE	=	SMC ADC15
SMC MCP CORE ISENSE	=	SMC NB CORE ISENSE
SMC MCP DDR ISENSE	=	SMC NB DDR ISENSE
SMC 1V5S3 ISENSE	=	SMC NB MISC ISENSE
TP SMC ANALOG ID	=	SMC ANALOG ID
TP SMC GPU ISENSE	=	SMC GPU ISENSE
SMC MCP VSENSE	=	SMC GPU VSENSE
SMC GFX THROTTLE L	=	SMC IG THROTTLE L
SMS INT L	=	SMC SMS INT
MCP WAKE REQ L	=	SMC G3H POWERON L



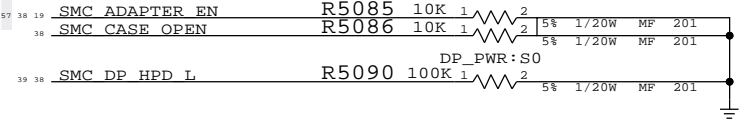
Unused Pins

SMS ONOFF L	=	TP SMS ONOFF L
SMC SYS KBDLED	=	TP SMC SYS KBDLED
SMC FAN 1 CTL	=	TP SMC FAN 1 CTL
TP SMC FAN 1 TACH	=	SMC FAN 1 TACH
SMC FAN 2 CTL	=	NC SMC FAN 2 CTL
NC SMC FAN 2 TACH	=	SMC FAN 2 TACH
SMC FAN 3 CTL	=	NC SMC FAN 3 CTL
NC SMC FAN 3 TACH	=	SMC FAN 3 TACH
SMC RSTGATE L	=	TP SMC RSTGATE L
SMC P10	=	TP SMC P10
SMC P20	=	TP SMC P20
SMC P24	=	TP SMC P24
SMC PH3	=	TP SMC PH3

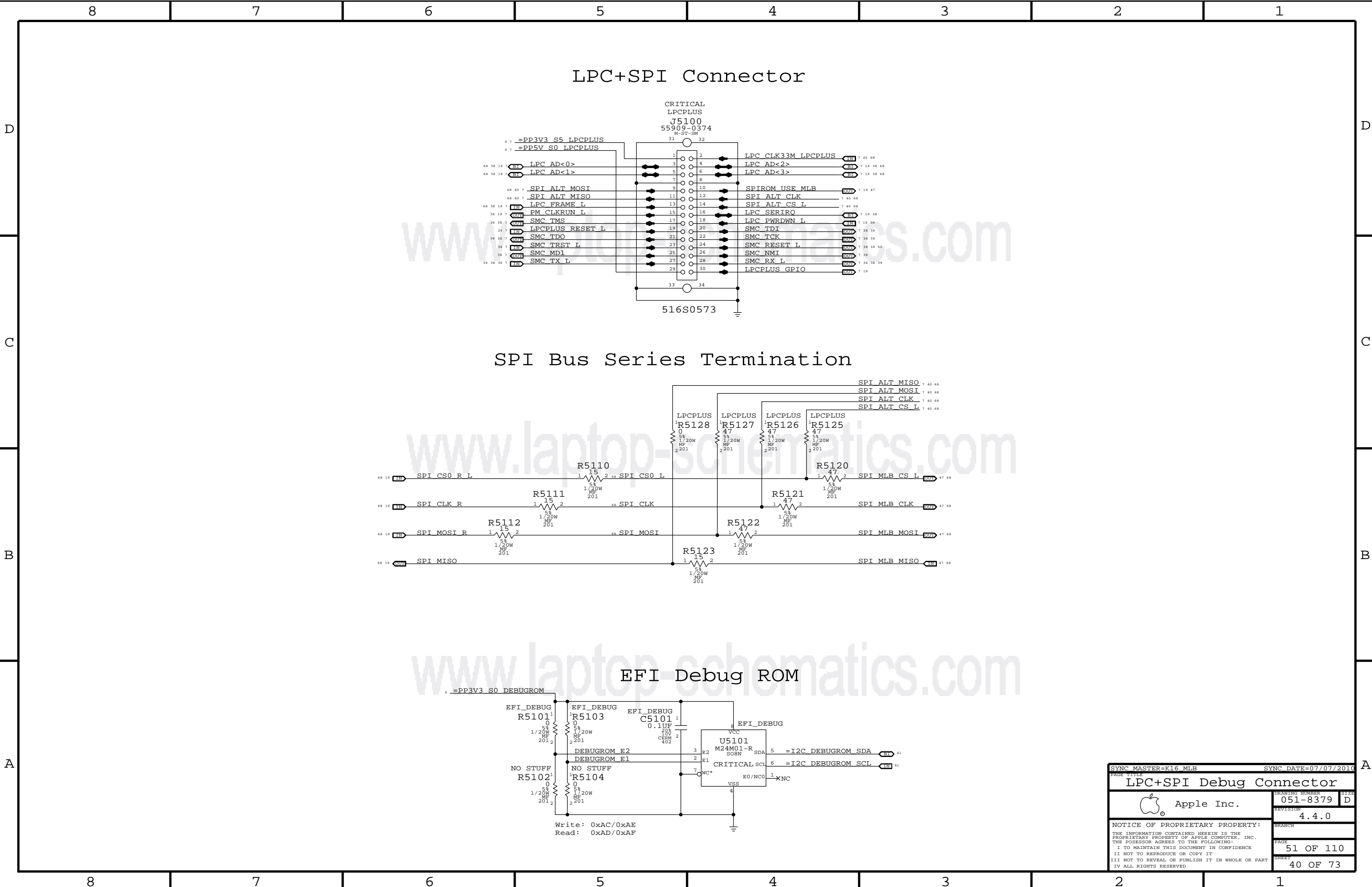
SMC Pull-ups



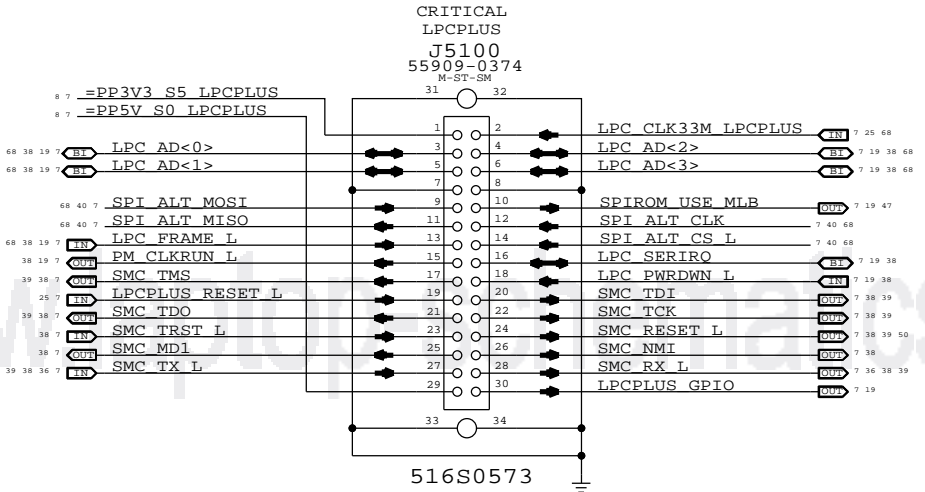
SMC Pull-downs



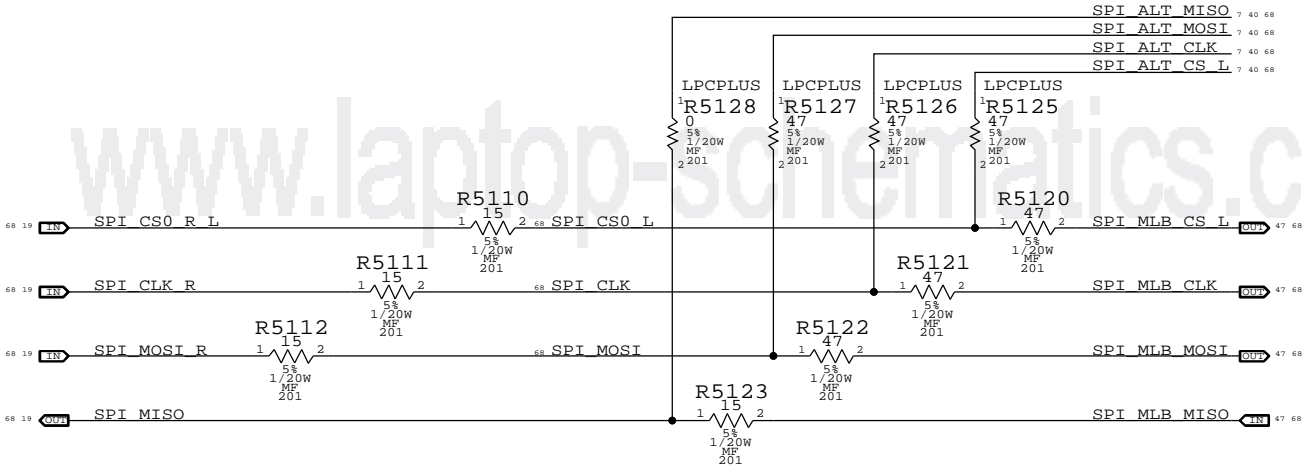
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PAGE TITLE			
SMC Support		DRAWING NUMBER 051-8379	
Apple Inc.		REVISION 4.4.0	
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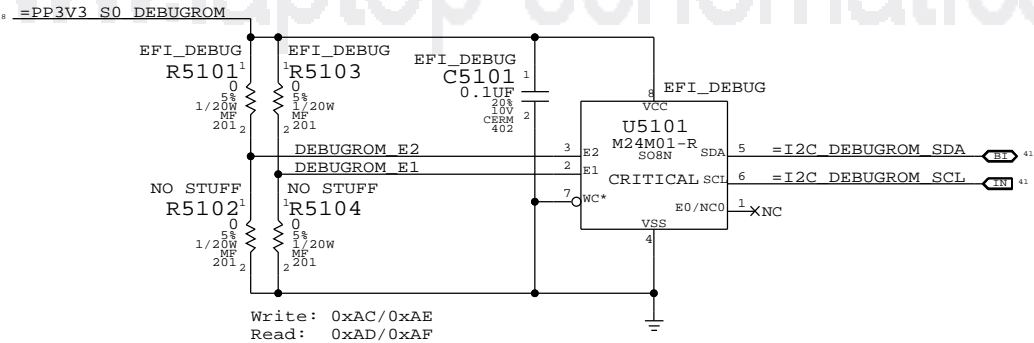
LPC+SPI Connector




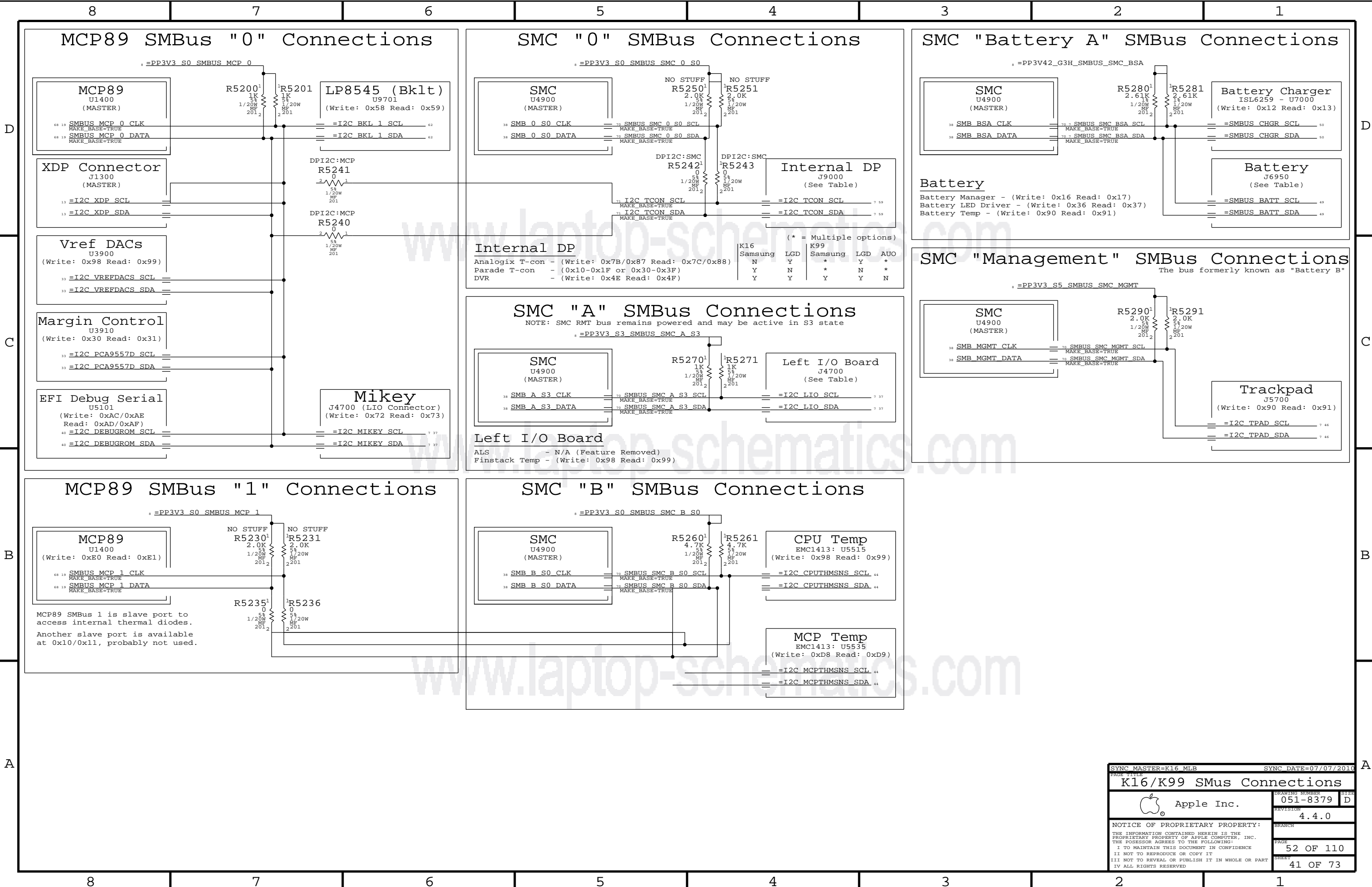
SPI Bus Series Termination



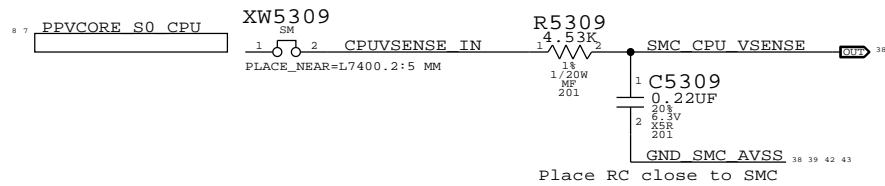
EFI Debug ROM



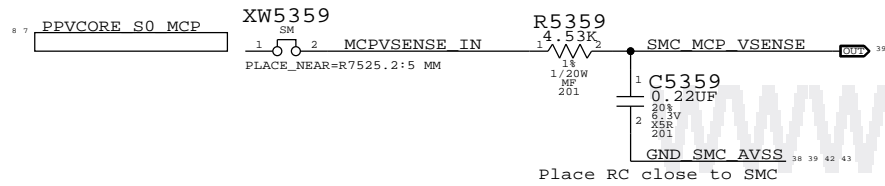
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PAGE TITLE			
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 Apple Inc.		DRAWING NUMBER	051-8379
		REVISION	4.4.0
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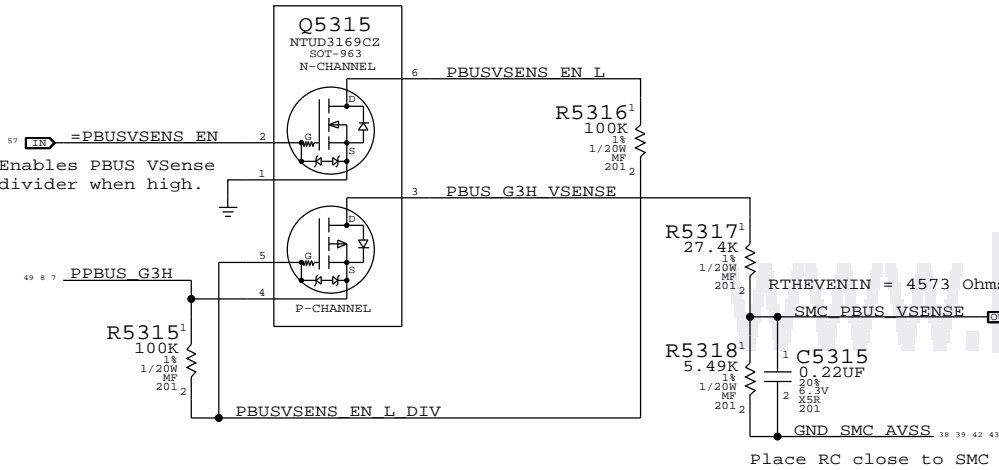
CPU Voltage Sense / Filter



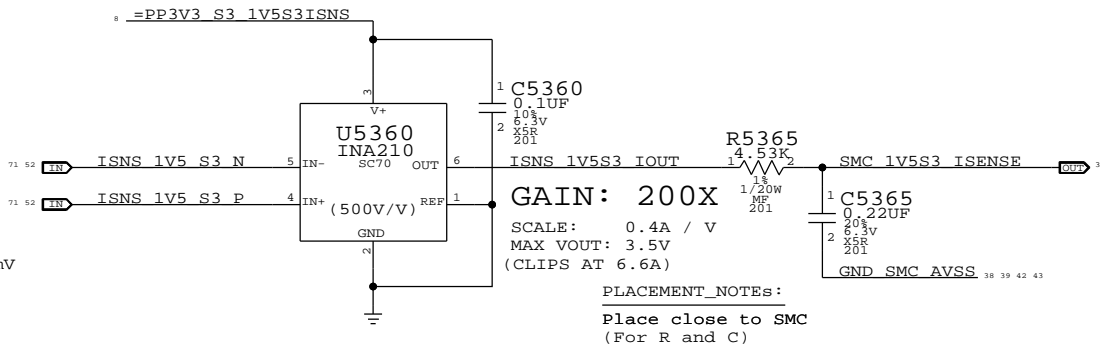
MCP Voltage Sense / Filter



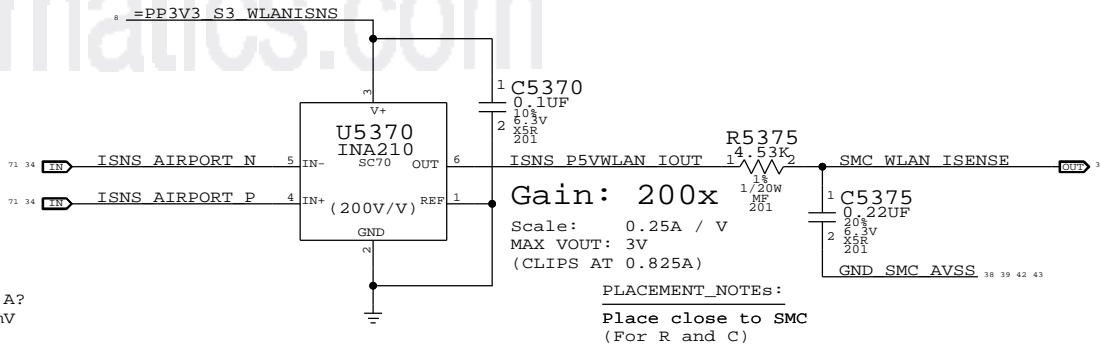
PBUS Voltage Sense Enable & Filter



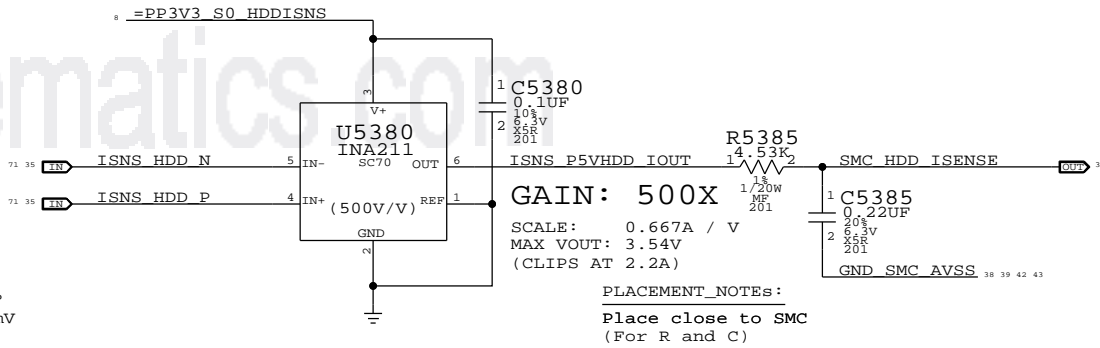
DDR3 1V5R1V35 Current Sense / Filter



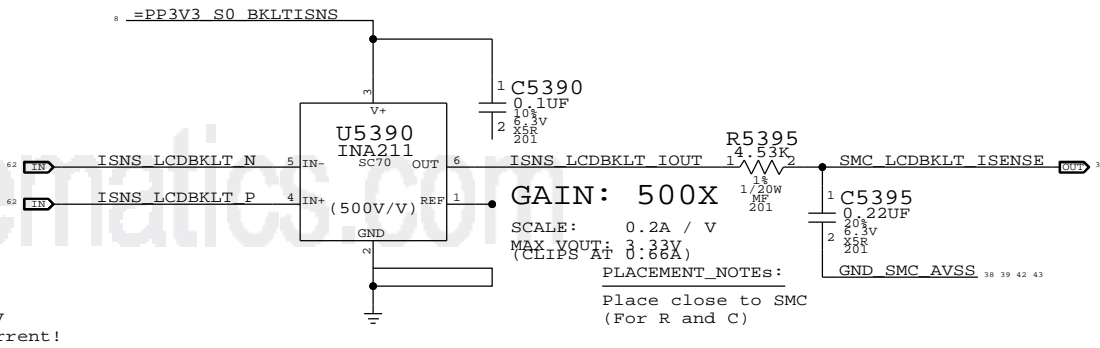
AirPort Current Sense / Filter



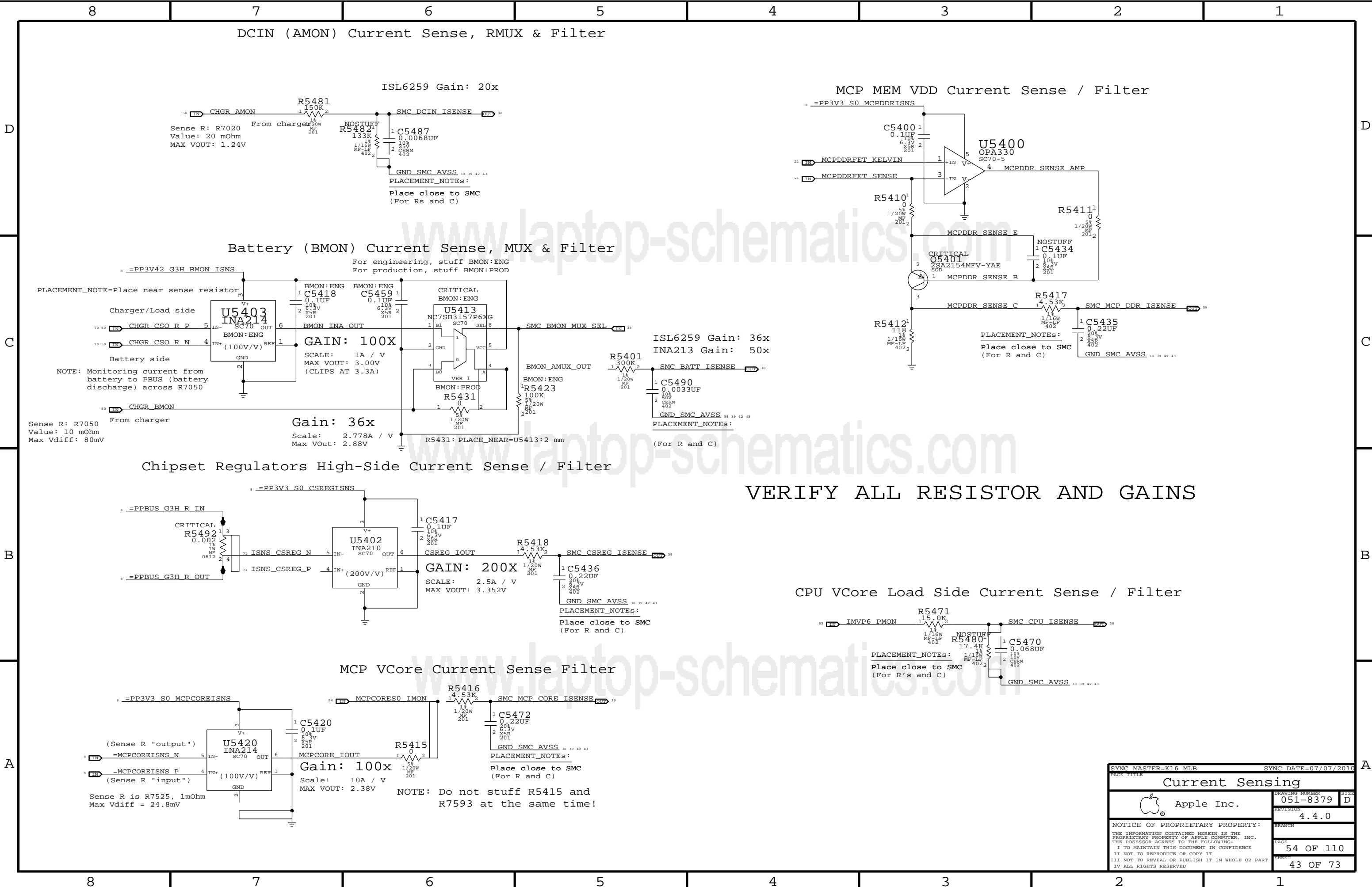
HDD Current Sense / Filter




LCD Backlight Driver Input Current Sense / Filter

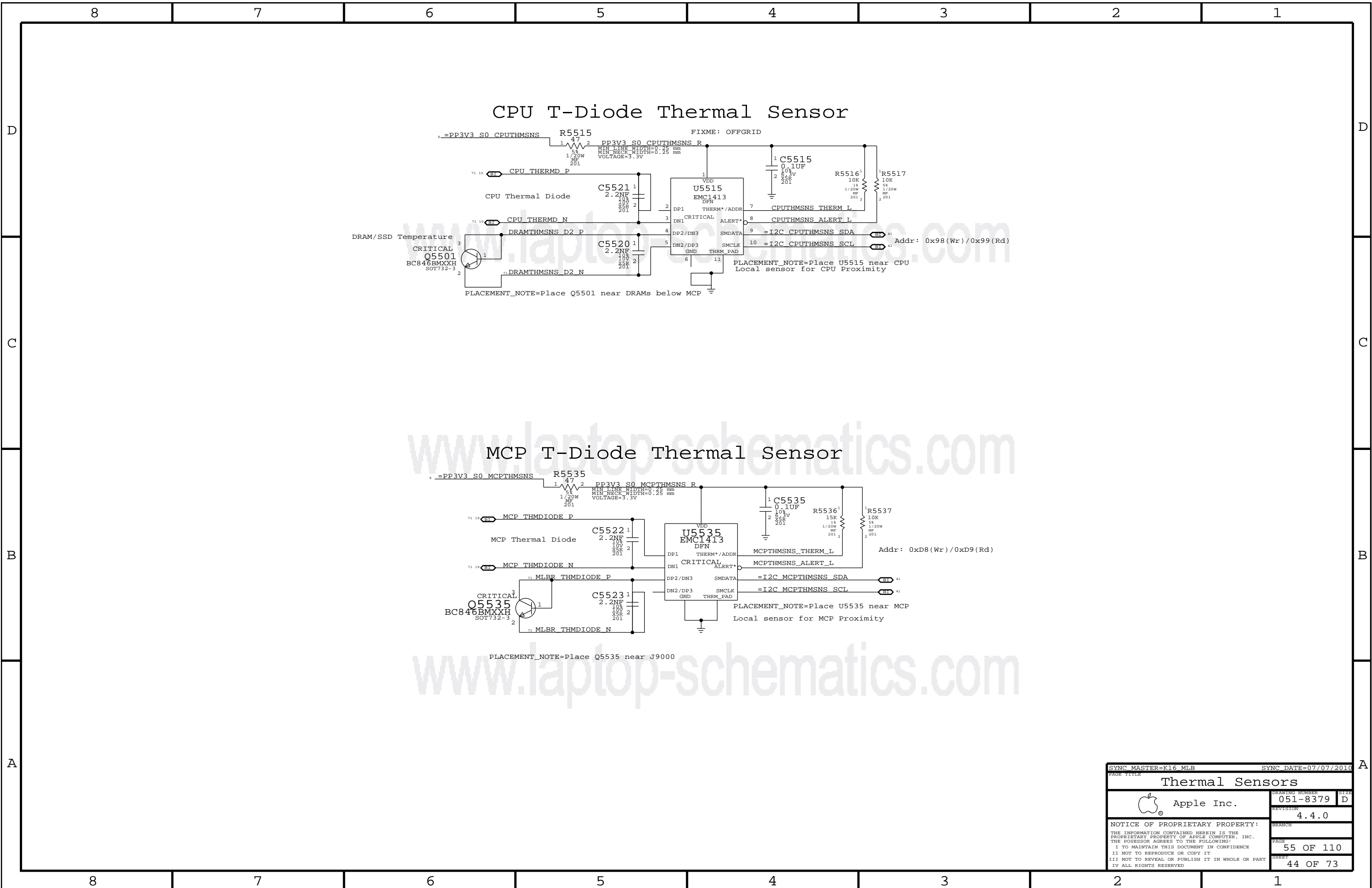


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PAGE TITLE		Voltage & Current Sensing	
DRAWING NUMBER		051-8379	SIZE D
REVISION		4.4.0	BRANCH
PAGE		53 OF 110	SHEET
SHEET		42 OF 73	



VERIFY ALL RESISTOR AND GAINS

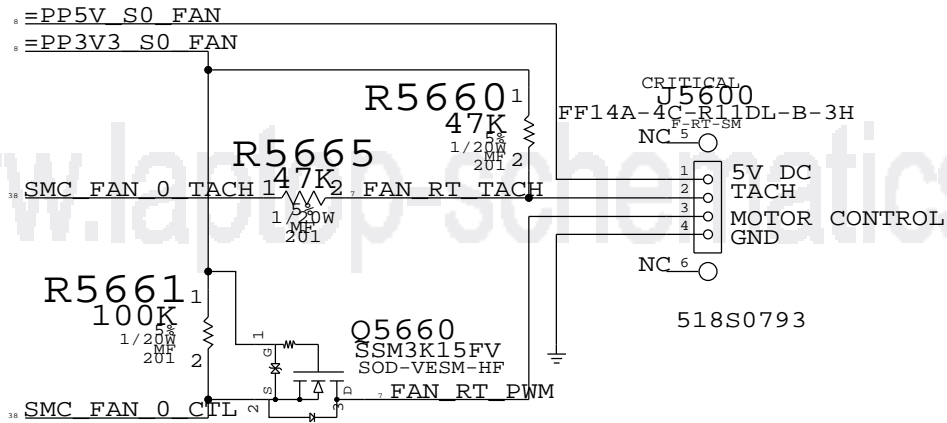
SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
PAGE TITLE			
Current Sensing			
 Apple Inc.		DRAWING NUMBER	051-8379
		SHEET	D
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		SHEET	43 OF 73



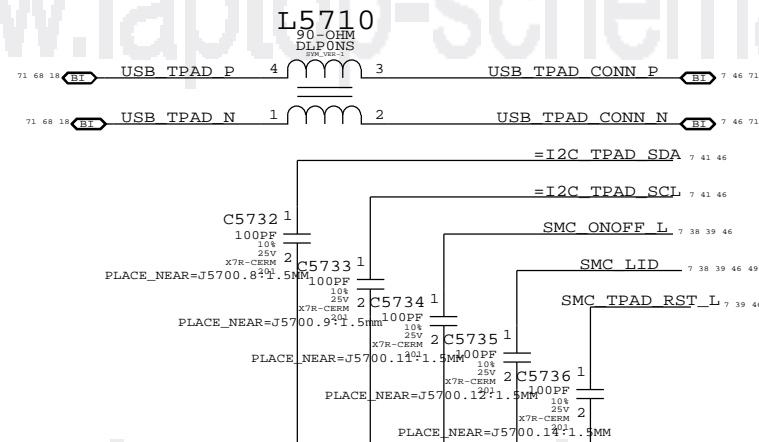
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# FAN CONNECTOR

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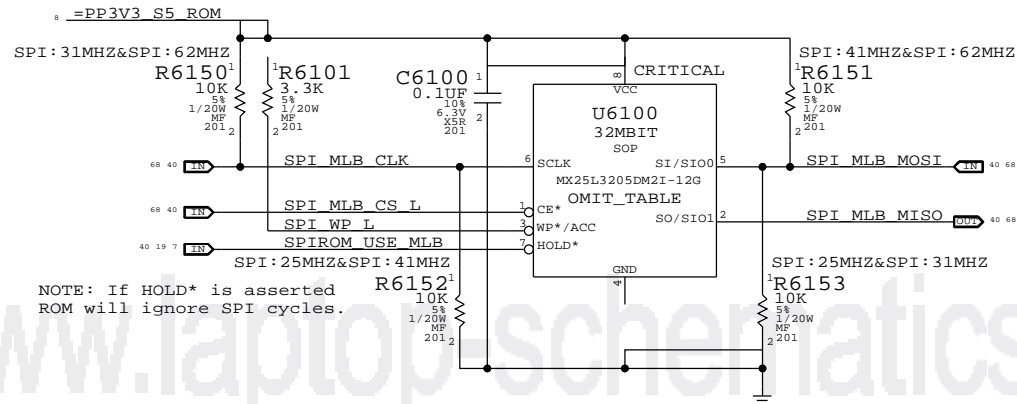
IPD\_3V3:S5  
R5730  
=PP3V3 S5 TPAD 1 0 2  
581/16W MF-LF  
104  
402  
IPD\_3V3:S3  
R5731  
=PP3V3 S3 TPAD 1 0 2  
581/16W MF-LF  
104  
402  
VOLTAGE=3.3V  
MIN\_NECK\_WIDTH=0.20mm  
MIN\_LINE\_WIDTH=0.5 mm  
PP3V3 TPAD CONN  
C5700 1  
0.1uF  
104  
6.3V  
X5R  
201  
2  
PLACE\_NEAR=J5700.1:1.5MM  
L5720  
FERR-120-OHM-1.5A  
0402-LF  
PP5V S5\_LDO  
C5710 1  
0.1uF  
104  
20V  
10V  
C5710  
402  
PLACE\_NEAR=J5700.10:1.5MM  
VOLTAGE=5V  
MIN\_NECK\_WIDTH=0.20mm  
MIN\_LINE\_WIDTH=0.5 mm  
PP5V TPAD FILT  
=I2C TPAD SDA  
=I2C TPAD SCL  
SMC ONOFF L  
SMC LID  
SMC TPAD RST L  
FF14A-14C-R1IDL-B-3H  
J5700  
P-RT-SM  
15  
1  
2  
3  
4  
5  
6  
7  
8  
9  
10  
11  
12  
13  
14  
16  
518S0794  
=PP3V4 S3 TPAD 1 0 2  
581/16W MF-LF  
104  
402  
VOLTAGE=3.3V  
MIN\_NECK\_WIDTH=0.20mm  
MIN\_LINE\_WIDTH=0.5 mm  
PP3V4 TPAD CONN  
C5720 1  
0.1uF  
104  
6.3V  
X5R  
201  
2  
PLACE\_NEAR=J5700.13:1.5MM



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NOTE: If HOLD\* is asserted ROM will ignore SPI cycles.

MCP89 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
41.7 MHz	1	0
62.5 MHz	1	1

NOTE: 42 & 62 MHz use FAST\_READ command.

## D

C

B


A



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SYNCH MASTER=AUDIO		SYNCH DATE=02/09/2010	
PAGE TITLE			
AUDIO0: SPEAKER AMP			
 Apple Inc.		DRAWING NUMBER	SIZE
		051-8379	D
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		SHEET 48 OF 73	

## D



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CRITICAL

J6903

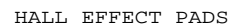
78171-0002

M-RT-SM

48 7 SPKRAMP\_S\_P\_OUT

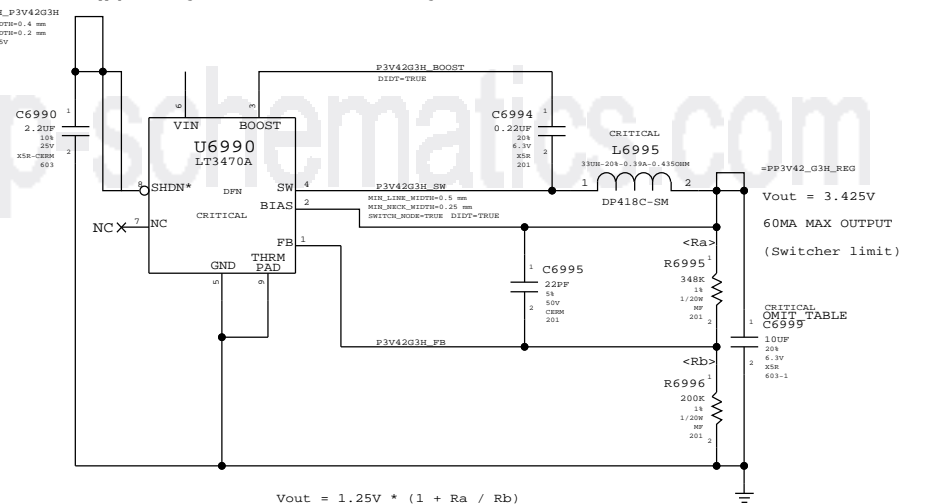
48 7 SPKRAMP\_S\_N\_OUT

SPKR

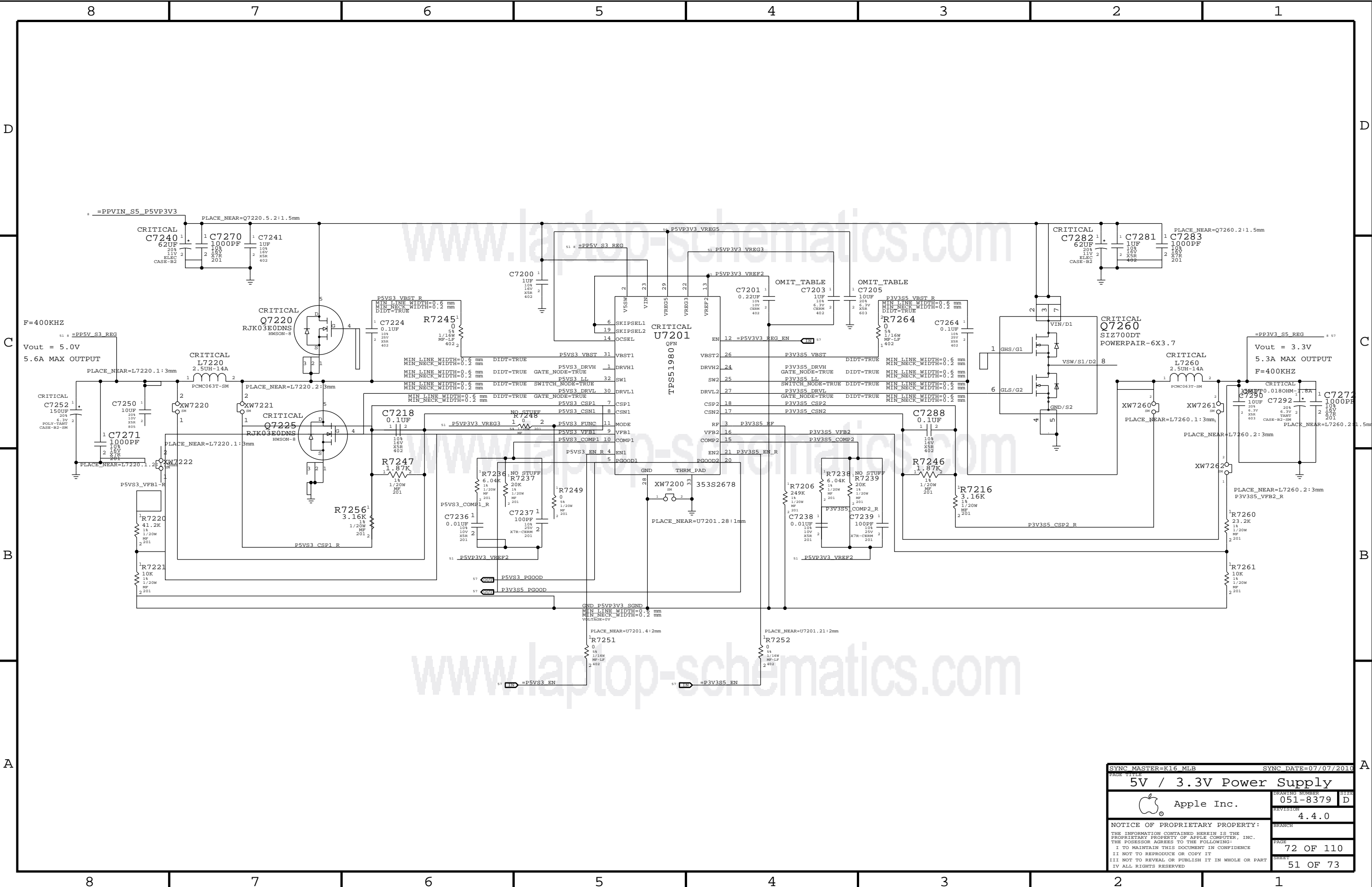



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PAGE TITLE			
DC-In & Battery Connectors			
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		PAGE	69 OF 110
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Supply needs to guarantee 3.31V delivered to SMC VRef generator





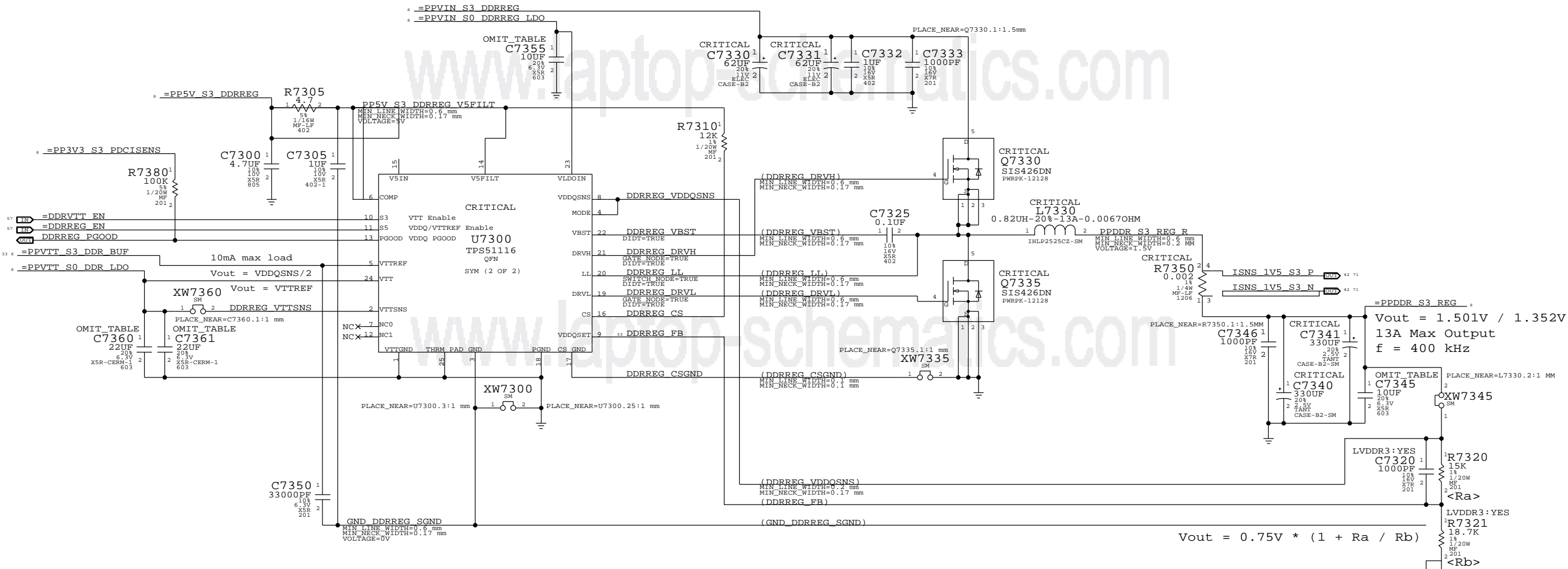


SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
PAGE TITLE			
5V / 3.3V Power Supply		DRAWING NUMBER	
 Apple Inc.		051-8379	SIZE D
		REVISION	
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B  
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C  
B  
A

8 7 6 5 4 3 2 1



Use LVDDR3:YES for fixed 1.35V operation or LVDDR3:NO for fixed 1.5V operation.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0331	1	RES,15K,1%,1/16W,MF-LF,0402	R7321		LVDDR3:NO

SYNC MASTER=K16 MLB

SYNC DATE=07/07/2010

1.5V/1.35V LVDDR3 Supply

Apple Inc.

051-8379

4.4.0

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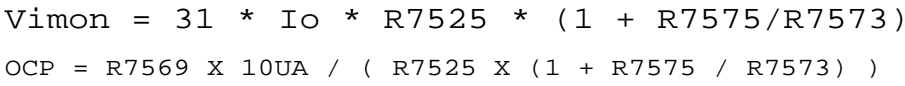


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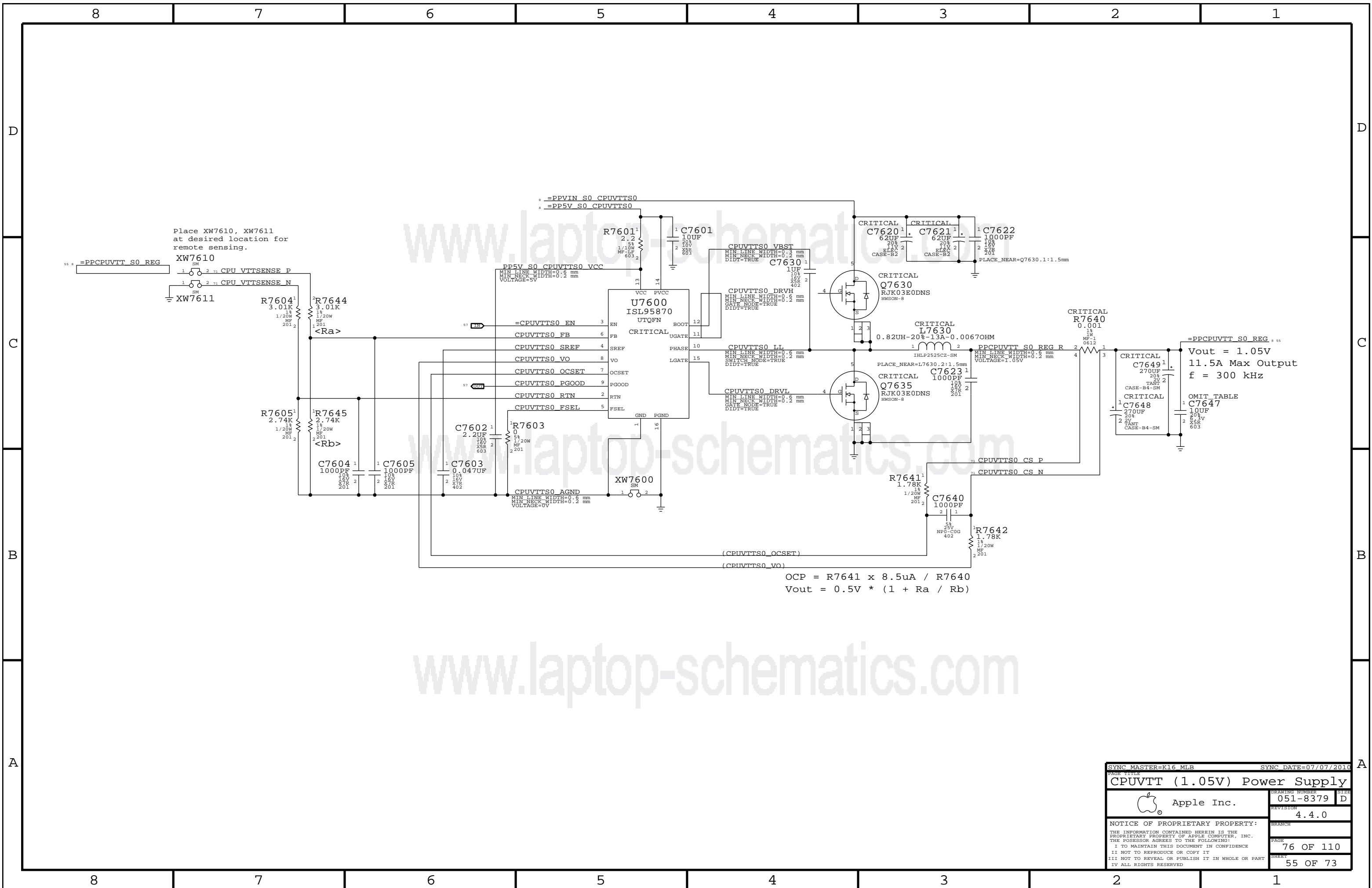
S1	IMVP6_THERM	0.25 MM	0.20 MM
S1	IMVP6_ISLEW	0.25 MM	0.20 MM
S1	PP1V7_S0_IMVP6_VREF	0.25 MM	0.20 MM
S1	PP5V_S0_IMVP6_V5FILT	0.25 MM	0.20 MM


 $\Delta$



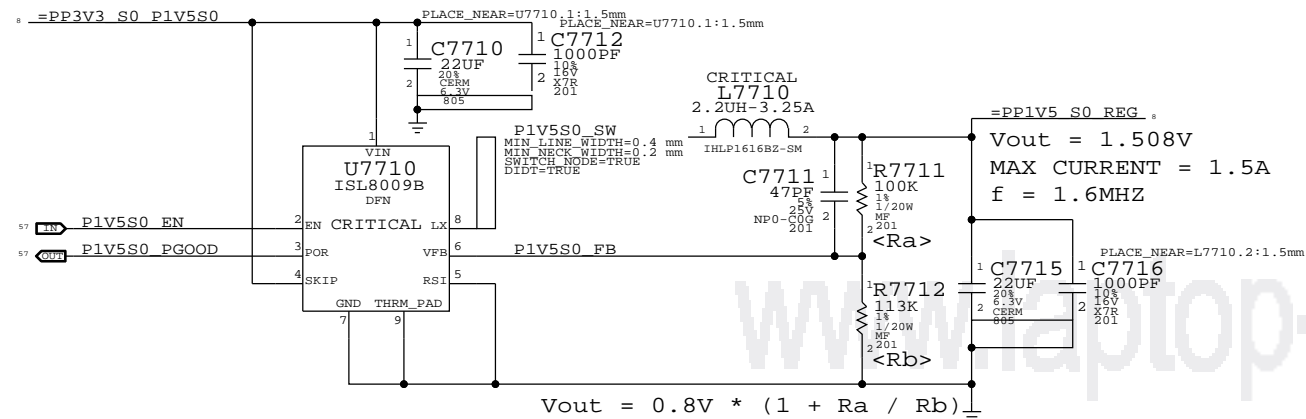
VID<3:0>	VOLTAGE
1100	0.9750V
1101	0.9625V
1110	0.9500V
1111	0.9375V
0000	0.9250V
0001	0.9125V
0010	0.9000V
0011	0.8875V
0100	0.8750V
0101	0.8625V
0110	0.8500V
0111	0.8375V
1000	0.8250V
1001	0.8125V
1010	0.8000V
1011	0.7875V

SYNC MASTER=K6 MLB		SYNC DATE=12/11/2009	
PAGE TITLE			
MCP VCore Regulator			
 Apple Inc.	DRAWING NUMBER		SIZE
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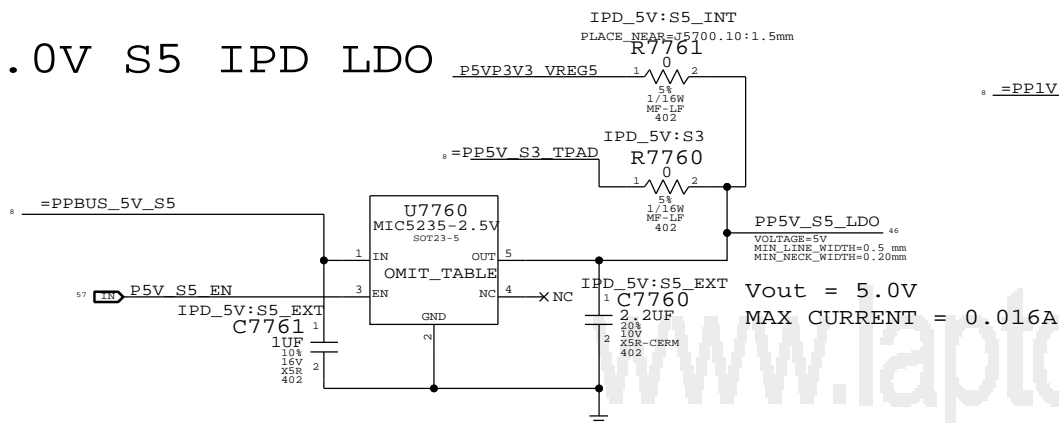


SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
PAGE TITLE			
CPUVTT (1.05V) Power Supply			
	DRAWING NUMBER		SIZE
	051-8379		D
	REVISION		
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## 1.5V S0 Regulator

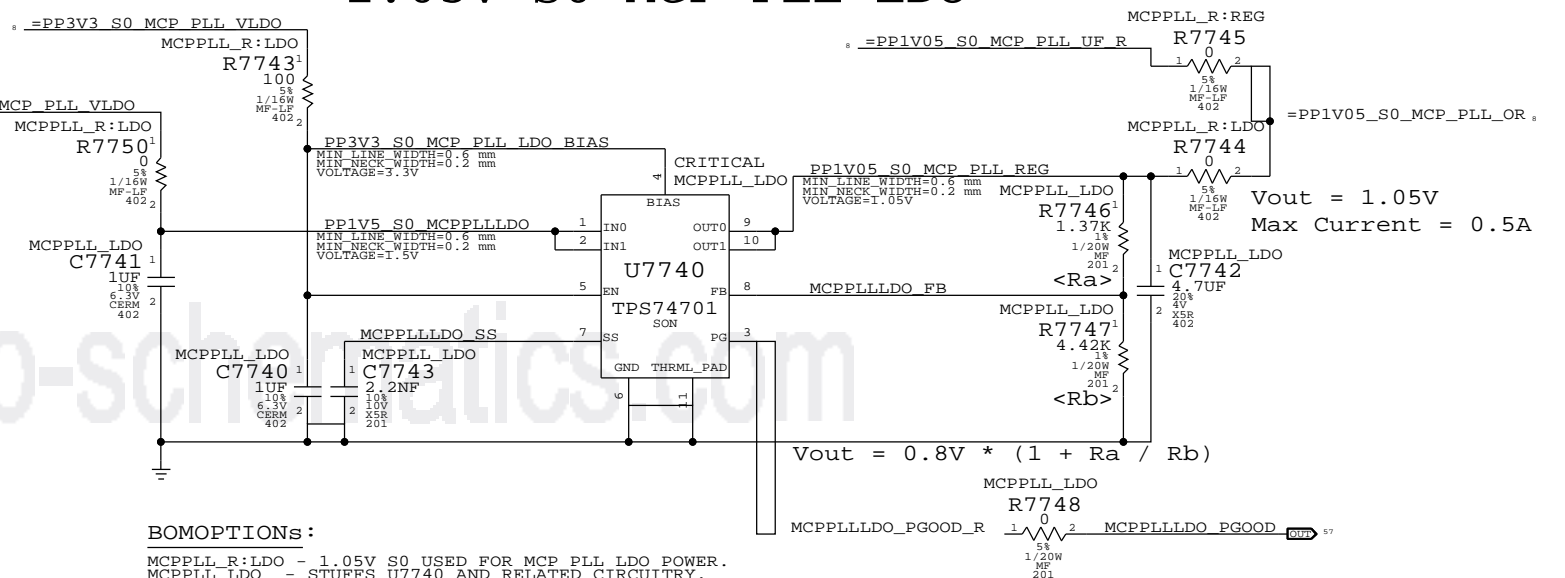


## 5.0V S5 IPD LDO



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3034	1	IC,LDO,MIC5235,5V,1A,150MA,SOT23-5	U7760		IPD_5V:S5_EXT

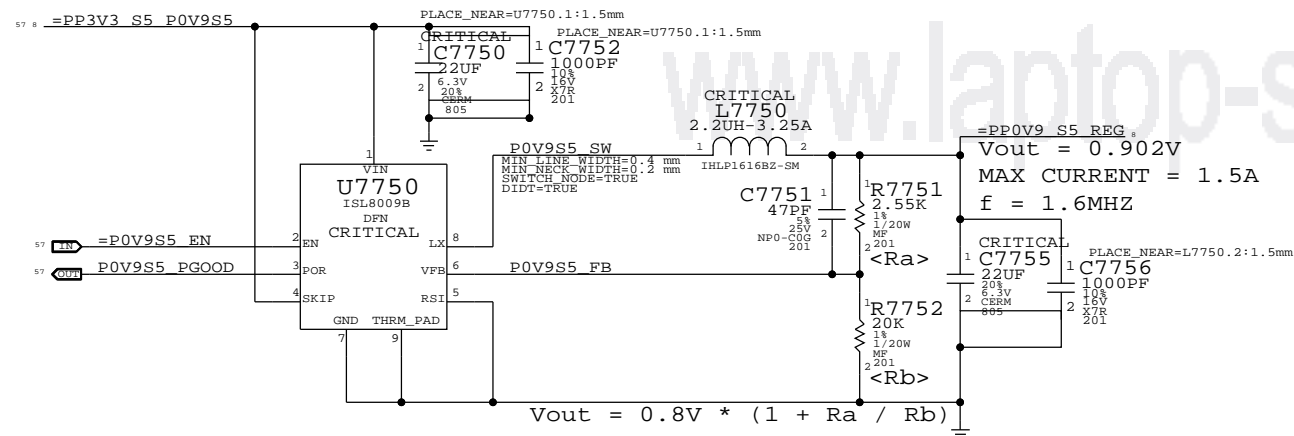
## 1.05V S0 MCP PLL LDO




### BOMOPTIONS:

MCPPLL\_R:LDO - 1.05V S0 USED FOR MCP PLL LDO POWER.  
MCPPLL\_LDO - STUFFS U7740 AND RELATED CIRCUITRY.  
TO USE U7740, MCPPLL\_R:LDO AND MCPPLL\_LDO MUST BE ACTIVE.  
TO USE 1.05V S0, MCPPLL\_R:REG MUST BE ACTIVE, MCPPLL\_LDO CAN BE ACTIVE, MCPPLL\_R:LDO MUST BE INACTIVE.

## MCP 0.9V S5 (AUXC) Switcher



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Misc Power Supplies			
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		SHEET	56 OF 73

8	7	6	5	4	3	2	1
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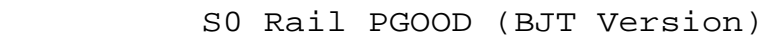
## C



## A



## S0 Rail PGOOD (ISL Version)

[illegible]

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

50 8 1 PP3V42 G3H\_CHGR

VFRQ:SLPS4&VFRQ:SLPS3&VFRQ:HIGH

R7861<sup>1</sup>

10K 5 1/20W MF 201 2

VFRQ:SLPS4&VFRQ:SLPS3

Q7860

SSM3K15FV

SOD-VESM-HF

CHGR\_VFRO

50

VFRQ:LOW

R7860<sup>1</sup>

10K 5 1/20W MF 201 2

VFRQ:SLPS4

R7864

5V 1/20W MF 201 0

PM\_SLP\_S4\_L

1 2

CHGR\_VFRO GATE

VFRQ:SLPS3


R7863

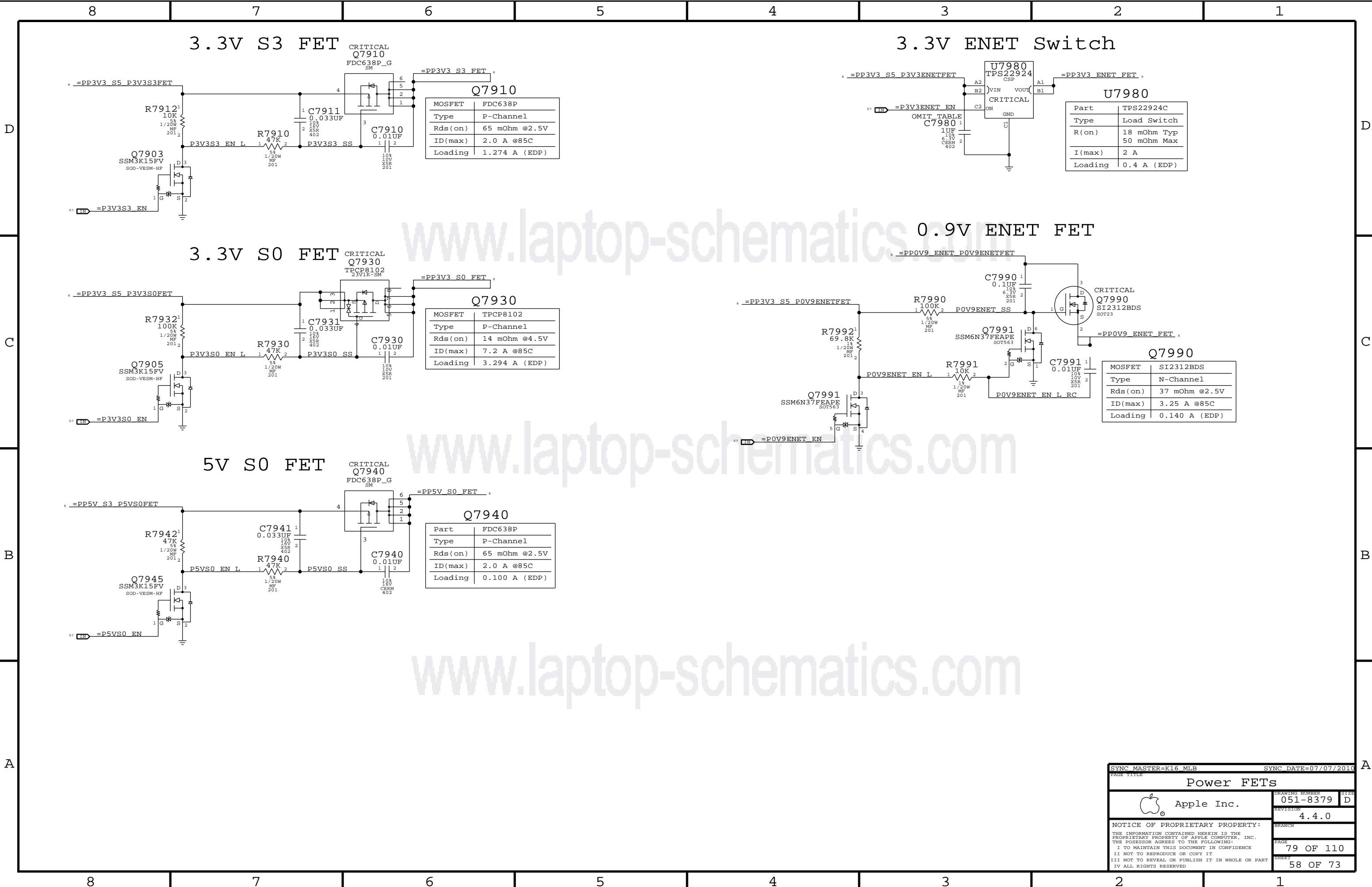
5V 1/20W MF 201 0

PM\_SLP\_S3\_L

1 2

VTT rail must ramp up in about the same time as MEMVDD rail (Q2300).

SYMC MASTER=K16 MLB		SYMC DATE=07/07/2010	
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Power Sequencing			
 Apple Inc.		DRAWING NUMBER	SIZE
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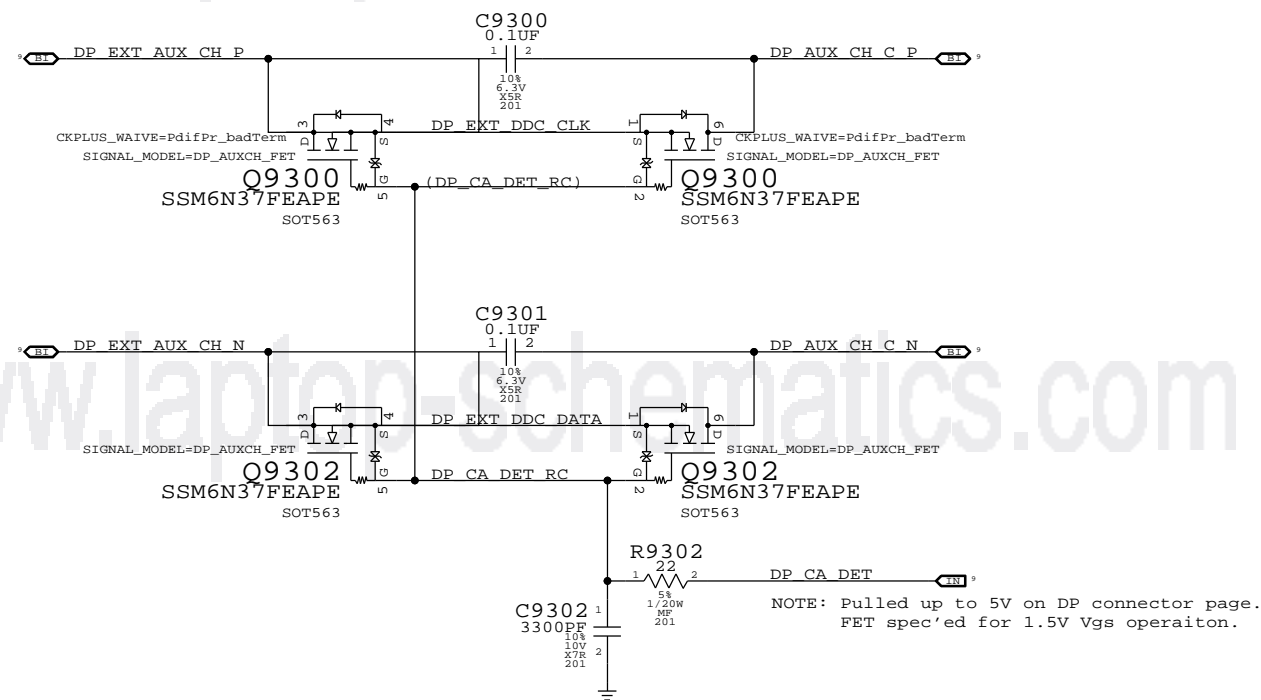





www.laptop-schematics.com

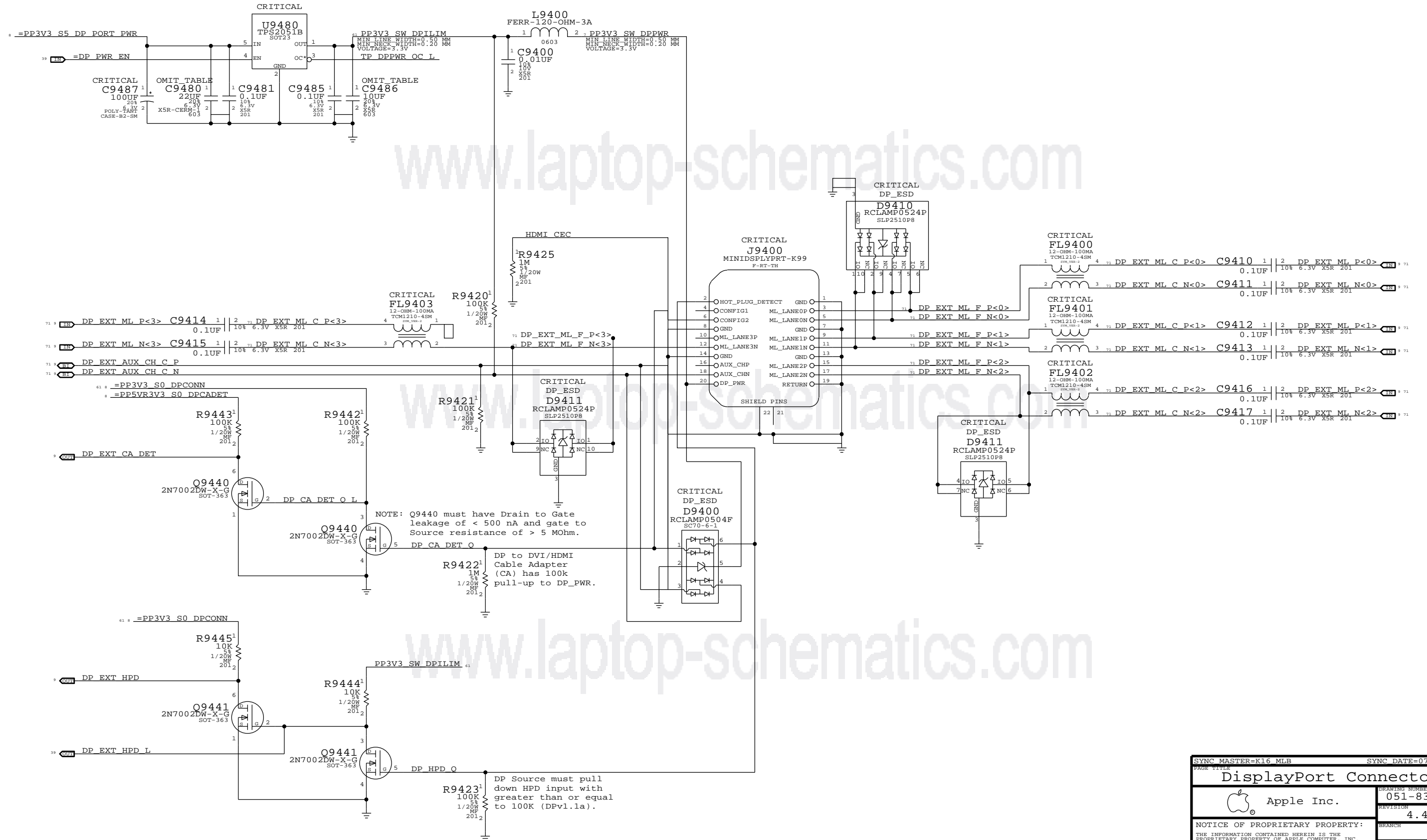
www.laptop-schematics.com

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SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
PART TITLE			
External DisplayPort Support			
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# Port Power Switch



D

C

B

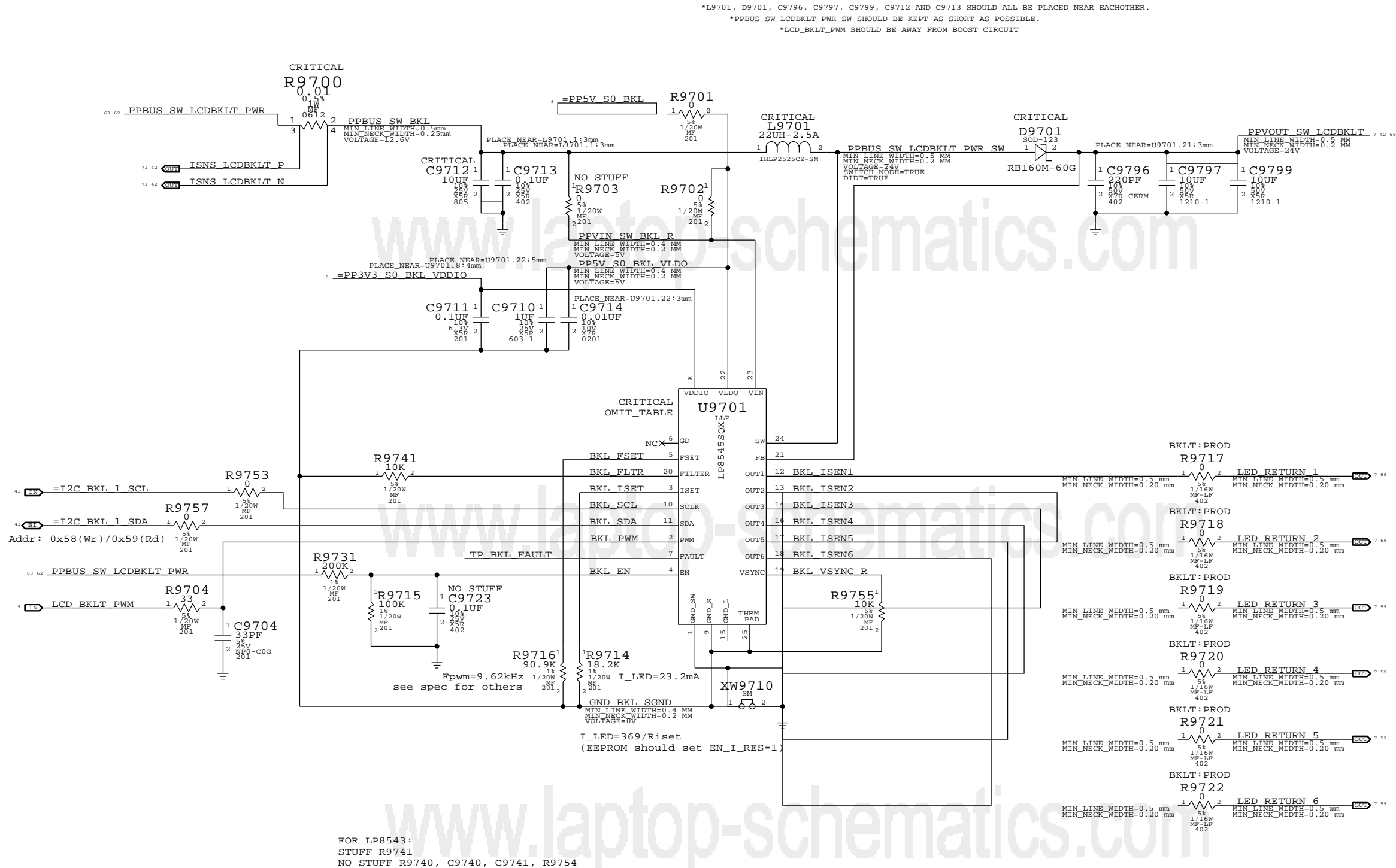
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D

C


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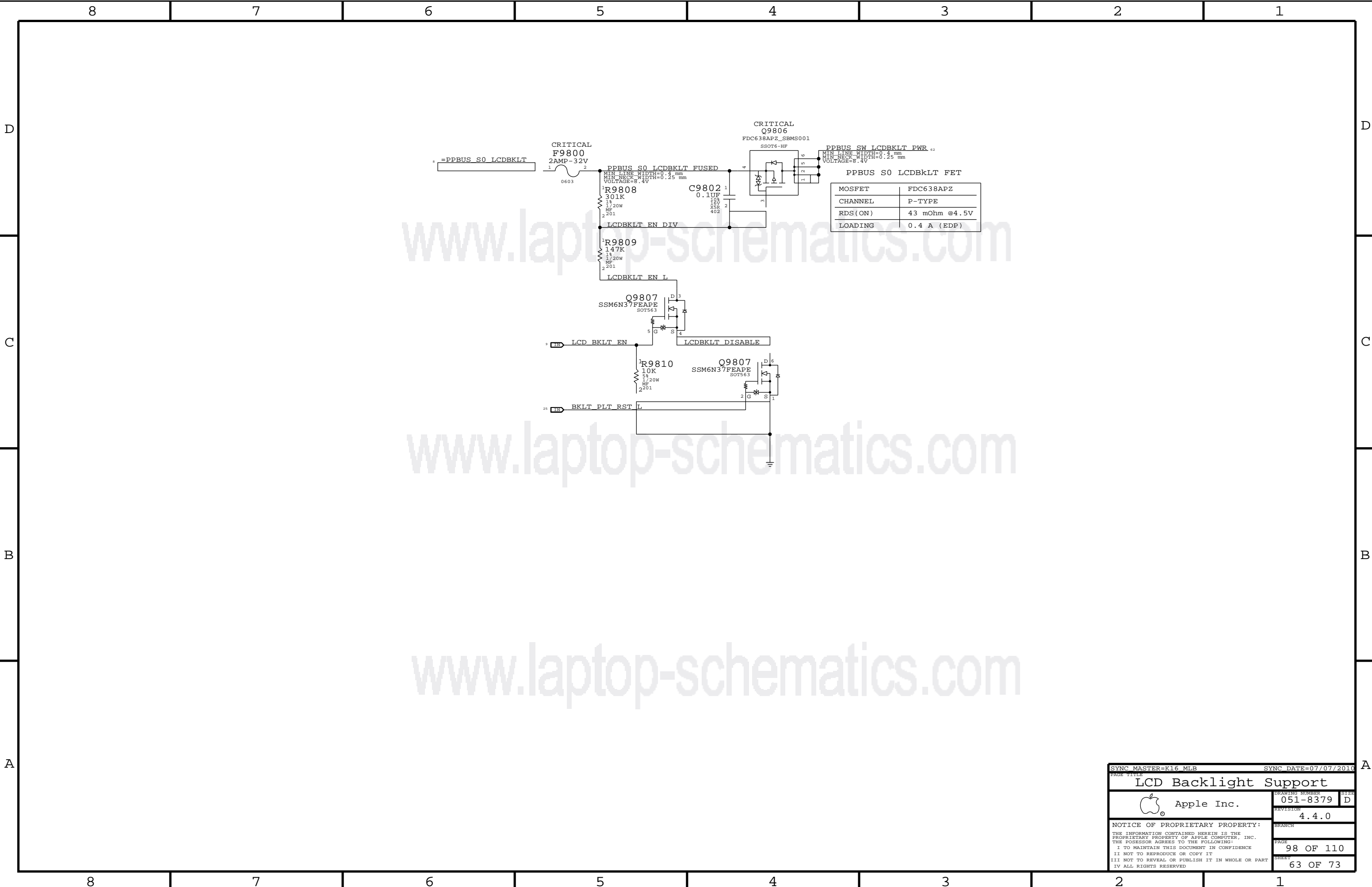
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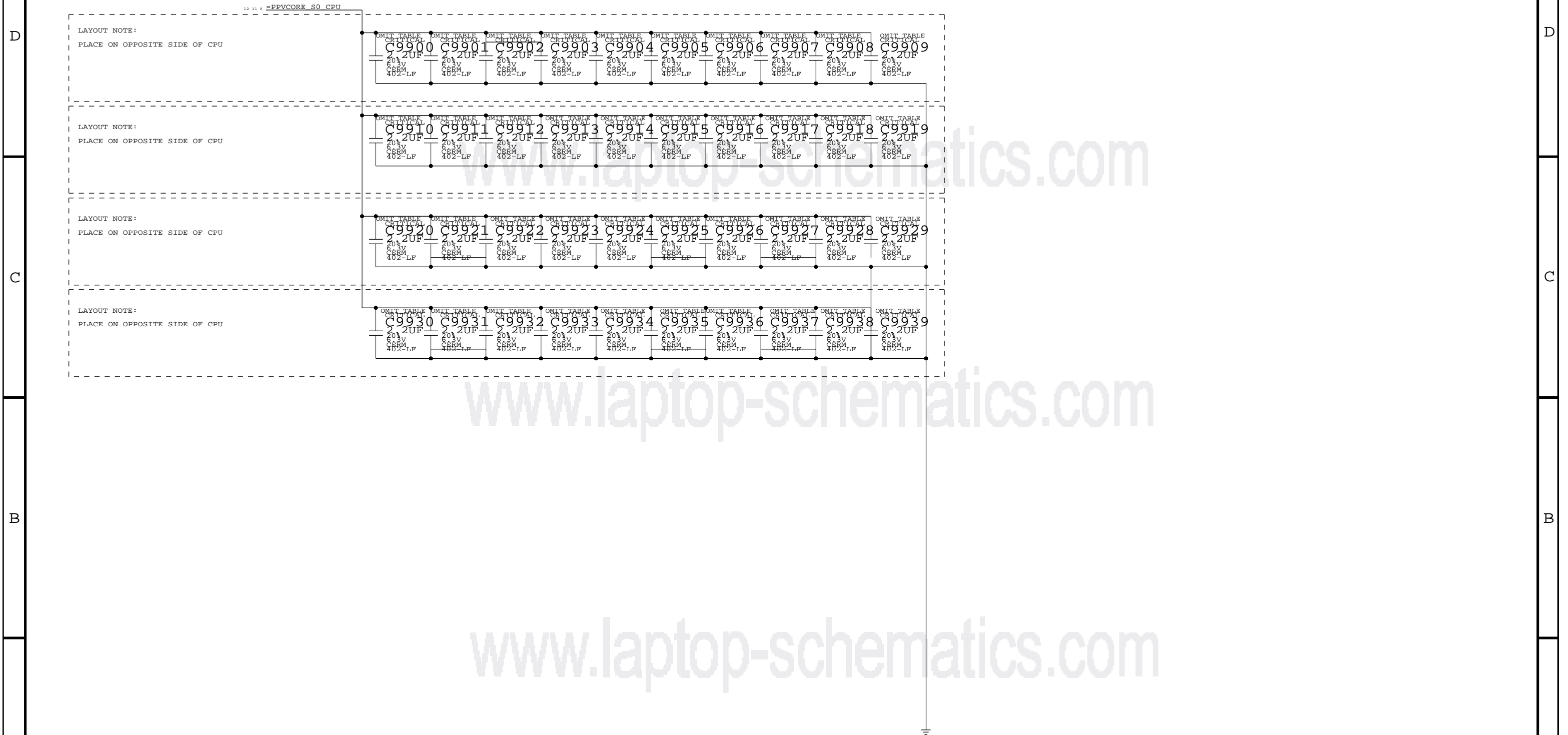
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG
353S2896	1	IC,LP8545,LED BKLT CTRLR,PRODUCTIO,LLP24	U9701	CRITICAL	PROJ:K16
353S2967	1	IC,LP8545,LED BKLT CTRLR,LLP24,K99 VER	U9701	CRITICAL	PROJ:K99


10.2 ohm resistors for current measurement on LED strings.

SYNC MASTER=K16 MLB		SYNC DATE=03/31/2010	
PAGE TITLE			
LCD Backlight Driver		DRAWING NUMBER	
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ADDITIONAL CPU VCORE HF DECOUPLING  
40x 1uF 0402



SYNC MASTER=K16 MLB PAGE 1 OF 1		SYNC DATE=07/07/2010 PAGE 1 OF 1	
Additional CPU/GPU Decoupling			
 Apple Inc.		DRAWING NUMBER 051-8379	SIZE D
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## FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.

Signals within each 4x group should be matched within 5 ps of strobe.

DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 135 ps.

Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

ESP 2Y signals / groups shown in signal table on right

FSB 2x signals / groups shown in signal table on right.  
Signals within each 2x group should be matched within 2

Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 270 ps. Spacing is 1x dielectric between ADDR# BEO# signals, with 2x dielectric spacing to ADTSB#

spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADS1B#.

FSB 1X signals shown in signal table on right.

Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.1

SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

## CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.

Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCD88 Interface PG (PG 04635 001 v0.9) Section 3.1

SOURCE: MCP89 Interface DG (DG-04625-001\_V0.9), Section 2.1  
SOURCE: Santa Rosa Platform DG Rev 0.9 (#20517) Sections 4.4 & 5.8.2.4

## MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.1.4

## FSB Clock Constraints


[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?	CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2.5

## CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB D L<15..0>	7 10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB DINV L<0>	7 10 14
FSB_DSTB0	FSB DSTB 55S	FSB_DSTB	FSB DSTB L P<0>	7 10 14
FSB_DSTB0	FSB DSTB 55S	FSB_DSTB	FSB DSTB L N<0>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB D L<31..16>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB DINV L<1>	7 10 14
FSB_DSTB1	FSB DSTB 55S	FSB_DSTB	FSB DSTB L P<1>	7 10 14
FSB_DSTB1	FSB DSTB 55S	FSB_DSTB	FSB DSTB L N<1>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB D L<47..32>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB DINV L<2>	7 10 14
FSB_DSTB2	FSB DSTB 55S	FSB_DSTB	FSB DSTB L P<2>	7 10 14
FSB_DSTB2	FSB DSTB 55S	FSB_DSTB	FSB DSTB L N<2>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB D L<63..48>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB DINV L<3>	7 10 14
FSB_DSTB3	FSB DSTB 55S	FSB_DSTB	FSB DSTB L P<3>	7 10 14
FSB_DSTB3	FSB DSTB 55S	FSB_DSTB	FSB DSTB L N<3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB A L<16..3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB REQ L<4..0>	7 10 14
FSB_ADSTR0	FSB_55S	FSB_ADSTR	FSB ADSTB L<0>	7 10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB A L<35..17>	7 10 14
FSB_ADSTR1	FSB_55S	FSB_ADSTR	FSB ADSTB L<1>	7 10 14
FSB_1X	FSB_55S	FSB_1X	FSB ADS L	7 10 14
FSB_BREQ0_L	FSB_55S	FSB_1X	FSB BREQ0 L	10 14
FSB_1X	FSB_55S	FSB_1X	FSB BNR L	10 14
FSB_1X	FSB_55S	FSB_1X	FSB BPRI L	10 14
FSB_1X	FSB_55S	FSB_1X	FSB DBSY L	10 14
FSB_1X	FSB_55S	FSB_1X	FSB DEFER L	10 14
FSB_1X	FSB_55S	FSB_1X	FSB DRDY L	10 14
FSB_1X	FSB_55S	FSB_1X	FSB HIT L	7 10 14
FSB_1X	FSB_55S	FSB_1X	FSB HITM L	7 10 14
FSB_1X	FSB_55S	FSB_1X	FSB LOCK L	7 10 14
FSB_CPUST L	FSB_55S	FSB_1X	FSB CPURST L	10 13 14
FSB_1X	FSB_55S	FSB_1X	FSB RS L<2..0>	10 14
FSB_1X	FSB_55S	FSB_1X	FSB TRDY L	10 14
CPU_ASYNC	CPU_55S	CPU_AGTL	CPU A20M L	10 14
CPU_BSEL	CPU_55S	CPU_AGTL	CPU BSEL<2..0>	9 10
CPU_FERR L	CPU_55S	CPU_SMIL	CPU FERR L	10 14
CPU_ASYNC	CPU_55S	CPU_AGTL	CPU IGNNE L	10 14
CPU_INIT L	CPU_55S	CPU_AGTL	CPU INIT L	10 14
CPU_ASYNC R	CPU_55S	CPU_AGTL	CPU INTR	10 14
CPU_ASYNC R	CPU_55S	CPU_AGTL	CPU NMI	10 14
CPU_PROCHOT L	CPU_55S	CPU_AGTL	CPU PROCHOT L	14 39
CPU_PWRGD	CPU_55S	CPU_AGTL	CPU PWRGD	10 13 14
CPU_ASYNC	CPU_55S	CPU_AGTL	CPU SMI L	10 14
CPU_ASYNC	CPU_55S	CPU_AGTL	CPU STPCLK L	10 14
PM_THRMTRIP L	CPU_55S	CPU_SMIL	PM THRMTRIP L	10 14 39
FSB_CPUISL P L	CPU_55S	CPU_AGTL	FSB CPUISL P L	10 14 39
CPU_FROM_SB	CPU_55S	CPU_AGTL	CPU DPSLP L	10 14
CPU_DERSTP L	CPU_55S	CPU_AGTL	CPU DPRSTP L	10 14 53
CPU_ASYNC	CPU_55S	CPU_AGTL	FSB DPWR L	10 14
FSB_CLK_CPU	CLK_FSB 100D	CLK_FSB	FSB CLK CPU P	10 14
FSB_CLK_CPU	CLK_FSB 100D	CLK_FSB	FSB CLK CPU N	10 14
FSB_CLK_ITP	CLK_FSB 100D	CLK_FSB	FSB CLK ITP P	13 14
FSB_CLK_ITP	CLK_FSB 100D	CLK_FSB	FSB CLK ITP N	13 14
FSB_CLK_MCP	CLK_FSB 100D	CLK_FSB	FSB CLK MCP P	14
FSB_CLK_MCP	CLK_FSB 100D	CLK_FSB	FSB CLK MCP N	14
CPU_IERR L	CPU_55S		CPU IERR L	10
PM DPRSLPVR	CPU_55S	CPU_AGTL	PM DPRSLPVR	14 53
(See above)	CPU_55S	CPU_AGTL	IMVP DPRSLPVR	
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP VDD	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP GND	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP VCC	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP GND	14

SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
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CPU/FSB Constraints			
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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

DDR3:  
DQ signals should be matched within 5 ps of associated DQS pair.  
DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 360 ps  
No DQS to clock matching requirement.  
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.  
CMD/CTRL signals should be matched within 150 ps.  
All memory signals maximum length is 1.030 ps.

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.2.3  
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.2.2

MEM\_A/B\_CKE EC SET NAME IS CHANGED ON K6, CANNOT SYNC THIS PAGE FROM T27

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM A CLK P<5..0>	9 15 26 27 32
MEM_A_CLK	MEM_70D	MEM_CLK	MEM A CLK N<5..0>	9 15 26 27 32
MEM_A_CKE	MEM_50S	MEM_CTRL	MEM A CKE<3..0>	15 21 26 27 32
MEM_A_CNTRL	MEM_50S	MEM_CTRL	MEM A CS L<3..0>	15 26 27 32
MEM_A_CNTRL	MEM_50S	MEM_CTRL	MEM A ODT<3..0>	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A A<15..0>	9 15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A BA<2..0>	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A RAS L	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A CAS L	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A WE L	15 26 27 32
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM A DQ<7..0>	15 26
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM A DQ<15..8>	15 26
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM A DQ<23..16>	15 26
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM A DQ<31..24>	15 26
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM A DQ<39..32>	15 27
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM A DQ<47..40>	15 27
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM A DQ<55..48>	15 27
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM A DQ<63..56>	15 27
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM A DM<0>	15 26
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM A DM<1>	15 26
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM A DM<2>	15 26
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM A DM<3>	15 26
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM A DM<4>	15 27
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM A DM<5>	15 27
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM A DM<6>	15 27
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM A DM<7>	15 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS P<0>	15 26
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS N<0>	15 26
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS P<1>	15 26
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS N<1>	15 26
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS P<2>	15 26
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS N<2>	15 26
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS P<3>	15 26
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS N<3>	15 26
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS P<4>	15 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS N<4>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS P<5>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS N<5>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS P<6>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS N<6>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS P<7>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS N<7>	15 27
MEM_B_CLK	MEM_70D	MEM_CLK	MEM B CLK P<5..0>	9 15 28 29 32
MEM_B_CLK	MEM_70D	MEM_CLK	MEM B CLK N<5..0>	9 15 28 29 32
MEM_B_CKE	MEM_50S	MEM_CTRL	MEM B CKE<3..0>	15 21 28 29 32
MEM_B_CNTRL	MEM_50S	MEM_CTRL	MEM B CS L<3..0>	15 28 29 32
MEM_B_CNTRL	MEM_50S	MEM_CTRL	MEM B ODT<3..0>	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B A<15..0>	9 15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B BA<2..0>	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B RAS L	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B CAS L	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B WE L	15 28 29 32
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM B DQ<7..0>	15 28
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM B DQ<15..8>	15 28
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM B DQ<23..16>	15 28
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM B DQ<31..24>	15 28
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM B DQ<39..32>	15 29
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM B DQ<47..40>	15 29
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM B DQ<55..48>	15 29
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM B DQ<63..56>	15 29
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM B DM<0>	15 28
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM B DM<1>	15 28
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM B DM<2>	15 28
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM B DM<3>	15 28
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM B DM<4>	15 29
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM B DM<5>	15 29
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM B DM<6>	15 29
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM B DM<7>	15 29
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS P<0>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS N<0>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS P<1>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS N<1>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS P<2>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS N<2>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS P<3>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS N<3>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS P<4>	15 29
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS N<4>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS P<5>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS N<5>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS P<6>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS N<6>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS P<7>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS N<7>	15 29
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP VDD	15
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP GND	15

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## PCI-Express

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.3

NEED PCIe Gen1/Gen2 notes!

## Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	20 MIL	?
CRT_2CRT	*	15 MIL	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	=4x_DIELECTRIC	?
MCP_DAC_COMP	*	=2x_DIELECTRIC	?

CRT signal single-ended impedance varies by location:

- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.4.1.

# Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be matched within 100 mils.  
 NOTE: NV DG recommends 90 ohm differential for LVDS, but cable/display assume 100 ohm.  
 DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 100 ps.  
 DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.  
 Max trace length: LVDS 10 inches, DP 8.5 inches.

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.4.2

## SATA Interface Constraints


PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=3x_DIELECTRIC	?
SATA_TERMPP	*	8 MIL	?

SATA intra-pair matching should be 1 ps.  
Max trace length: 12 inches for SATA Gen1/Gen2, TBD for SATA Gen3.  
SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.6

## MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
	PCIE_90D	PCIE	PEG R2D P<15..0>
	PCIE_90D	PCIE	PEG R2D N<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG R2D C P<15..0>
	PCIE_90D	PCIE	PEG R2D C N<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R P<15..0>
	PCIE_90D	PCIE	PEG D2R N<15..0>
	PCIE_90D	PCIE	PEG D2R C P<15..0>
	PCIE_90D	PCIE	PEG D2R C N<15..0>
	PCIE_90D	PCIE	PCIE AP R2D P
	PCIE_90D	PCIE	PCIE AP R2D N
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE AP R2D C P
	PCIE_90D	PCIE	PCIE AP R2D C N
PCIE_AP_D2R	PCIE_90D	PCIE	PCIE AP D2R P
	PCIE_90D	PCIE	PCIE AP D2R N
	PCIE_90D	PCIE	PCIE ENET R2D P
	PCIE_90D	PCIE	PCIE ENET R2D N
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE ENET R2D C P
	PCIE_90D	PCIE	PCIE ENET R2D C N
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE ENET D2R P
	PCIE_90D	PCIE	PCIE ENET D2R N
	PCIE_90D	PCIE	PCIE ENET D2R C P
	PCIE_90D	PCIE	PCIE ENET D2R C N
	PCIE_90D	PCIE	PCIE FW R2D P
	PCIE_90D	PCIE	PCIE FW R2D N
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE FW R2D C P
	PCIE_90D	PCIE	PCIE FW R2D C N
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE FW D2R P
	PCIE_90D	PCIE	PCIE FW D2R N
	PCIE_90D	PCIE	PCIE FW D2R C P
	PCIE_90D	PCIE	PCIE FW D2R C N
MCP_PEO_REECLK	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M P
	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M N
MCP_PE1_REECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M AP P
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M AP N
MCP_PE2_REECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET P
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET N
MCP_PE3_REECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW P
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW N
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP PEX0 TERMP
CRT_RED	CRT_50S	CRT	CRT IG R C PR
CRT_GREEN	CRT_50S	CRT	CRT IG G Y Y
CRT_BLUE	CRT_50S	CRT	CRT IG B COMP PB
CRT_SYNC	CRT_50S	CRT_SYNC	CRT IG HSYNC
CRT_SYNC	CRT_50S	CRT_SYNC	CRT IG VSYNC
MCP_DAC_RSET		MCP_DAC_COMP	MCP TV DAC RSET
MCP_DAC_VREF		MCP_DAC_COMP	MCP TV DAC VREF
DP_INT_ML	DP_90D	DISPLAYPORT	DP IG ML1 P<1..0>
DP_INT_ML	DP_90D	DISPLAYPORT	DP IG ML1 N<1..0>
DP_INT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH1 P
DP_INT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH1 N
DP_EXT_ML	DP_90D	DISPLAYPORT	DP IG ML0 P<3..0>
DP_EXT_ML	DP_90D	DISPLAYPORT	DP IG ML0 N<3..0>
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH0 P
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH0 N
MCP_TMDS0_RSET	MCP_TV_COMP		MCP TMDS0 RSET
MCP_TMDS0_VPROBE			MCP TMDS0 VPROBE
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK P
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK N
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS IG A DATA P<2..0>
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS IG A DATA N<2..0>
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS IG A DATA P<3>
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS IG A DATA N<3>
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS IG B CLK P
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS IG B CLK N
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS IG B DATA P<2..0>
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS IG B DATA N<2..0>
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS IG B DATA P<3>
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS IG B DATA N<3>
MCP_IFFAB_RSET	MCP_TV_COMP		MCP IFFAB RSET
MCP_IFFAB_VPROBE			MCP IFFAB VPROBE
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D C P
	SATA_90D	SATA	SATA HDD R2D C N
	SATA_90D	SATA	SATA HDD R2D P
	SATA_90D	SATA	SATA HDD R2D N
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R P
	SATA_90D	SATA	SATA HDD D2R N
	SATA_90D	SATA	SATA HDD D2R C P
	SATA_90D	SATA	SATA HDD D2R C N
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D C P
	SATA_90D	SATA	SATA ODD R2D C N
	SATA_90D	SATA	SATA ODD R2D P
	SATA_90D	SATA	SATA ODD R2D N
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R P
	SATA_90D	SATA	SATA ODD D2R N
	SATA_90D	SATA	SATA ODD D2R C P
	SATA_90D	SATA	SATA ODD D2R C N
MCP_SATA_TERMP		SATA_TERMP	MCP SATA TERMP

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## LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=1.5x_DIELECTRIC	?
CLK_LPC	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.7

## USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIA5	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?	USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.8

## SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.9

## HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.10

## SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.11

## SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.12

## MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	LPC_AD	LPC_55S	LPC	LPC AD<3..0>	7 19 38 40
	LPC_FRAME_L	LPC_55S	LPC	LPC FRAME_L	7 19 38 40
	LPC_RESET_L	LPC_55S	LPC	LPC RESET_L	19 25
	MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC R	19 25
		CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC	25 38
		CLK_LPC_55S	CLK_LPC	LPC CLK33M LPCPLUS	7 25 40
	USB_EXT_A	USB_90D	USB	USB EXT_A P	18 36
		USB_90D	USB	USB EXT_A N	18 36
		USB_90D	USB	USB EXT_A MUXED P	16 71
		USB_90D	USB	USB EXT_A MUXED N	16 71
	USB_MINI	USB_90D	USB	USB MINI P	0 18
		USB_90D	USB	USB MINI N	0 18
	USB_EXTD	USB_90D	USB	USB EXT_D P	7 18 37
		USB_90D	USB	USB EXT_D N	7 18 37
	USB_CAMERA	USB_90D	USB	USB CAMERA P	7 18 37
		USB_90D	USB	USB CAMERA N	7 18 37
	USB_BT	USB_90D	USB	USB BT P	7 18 34
		USB_90D	USB	USB BT N	7 18 34
	USB_TPAD	USB_90D	USB	USB TPAD P	18 46 71
		USB_90D	USB	USB TPAD N	18 46 71
	USB_IR	USB_90D	USB	USB IR P	
		USB_90D	USB	USB IR N	
	USB_EXTB	USB_90D	USB	USB EXTB P	
		USB_90D	USB	USB EXTB N	
	USB_T57	USB_90D	USB	USB T57 P	
		USB_90D	USB	USB T57 N	
	USB_EXTC	USB_90D	USB	USB EXTC P	0 18
		USB_90D	USB	USB EXTC N	0 18
	USB_SDCARD	USB_90D	USB	USB SDCARD P	0 18
		USB_90D	USB	USB SDCARD N	0 18
	USB_WM	USB_90D	USB	USB WM P	
		USB_90D	USB	USB WM N	
	MCP_USB_RBIA5	MCP_USB_RBIA5		MCP USB RBIA5 GND	18
	SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS MCP 0 CLK	19 41
	SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS MCP 0 DATA	19 41
	(SMBUS_SMC_MGMT_SCL)	SMB_55S	SMB	SMBUS MCP 1 CLK	19 41
	(SMBUS_SMC_MGMT_SDA)	SMB_55S	SMB	SMBUS MCP 1 DATA	19 41
	HDA_BIT_CLK	HDA_55S	HDA	HDA BIT_CLK	0 19 37
		HDA_55S	HDA	HDA BIT_CLK_R	
	HDA_SYNC	HDA_55S	HDA	HDA SYNC	7 19 37
		HDA_55S	HDA	HDA SYNC_R	19
	HDA_RST_L	HDA_55S	HDA	HDA RST_R_L	19
		HDA_55S	HDA	HDA_RST_L	7 19 37
	HDA_SPIN0	HDA_55S	HDA	HDA SPIN0	7 19 37
		HDA_55S	HDA	HDA SDIN CODEC	
	HDA_SDOUIT	HDA_55S	HDA	HDA SDOUIT	7 19 37
		HDA_55S	HDA	HDA_SDOUIT_R	19
	MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP	19
	MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM CLK32K SUSCLK_R	19 25
		CLK_SLOW_55S	CLK_SLOW	PM CLK32K SUSCLK	25 38
	SPI_CLK	SPT_55S	SPT	SPI_CLK_R	19 40
		SPT_55S	SPT	SPI_CLK	
	SPI_MOSI	SPT_55S	SPT	SPI_MOSI_R	19 40
		SPT_55S	SPT	SPI_MOSI	40
	SPI_MISO	SPT_55S	SPT	SPI_MISO	19 40
	SPI_CS0	SPT_55S	SPT	SPI_CS0_R_L	19 40
		SPT_55S	SPT	SPI_CS0_L	40
		SPT_55S	SPT	SPI_MLB_CLK	40 47
		SPT_55S	SPT	SPI_MLB_MOSI	40 47
		SPT_55S	SPT	SPI_MLB_MISO	40 47
		SPT_55S	SPT	SPI_MLB_CS_L	40 47
		SPT_55S	SPT	SPI_ALT_CLK	7 40
		SPT_55S	SPT	SPI_ALT_MOSI	7 40
		SPT_55S	SPT	SPI_ALT_MISO	7 40
		SPT_55S	SPT	SPI_ALT_CS_L	7 40

## D

CB

A

B

## C

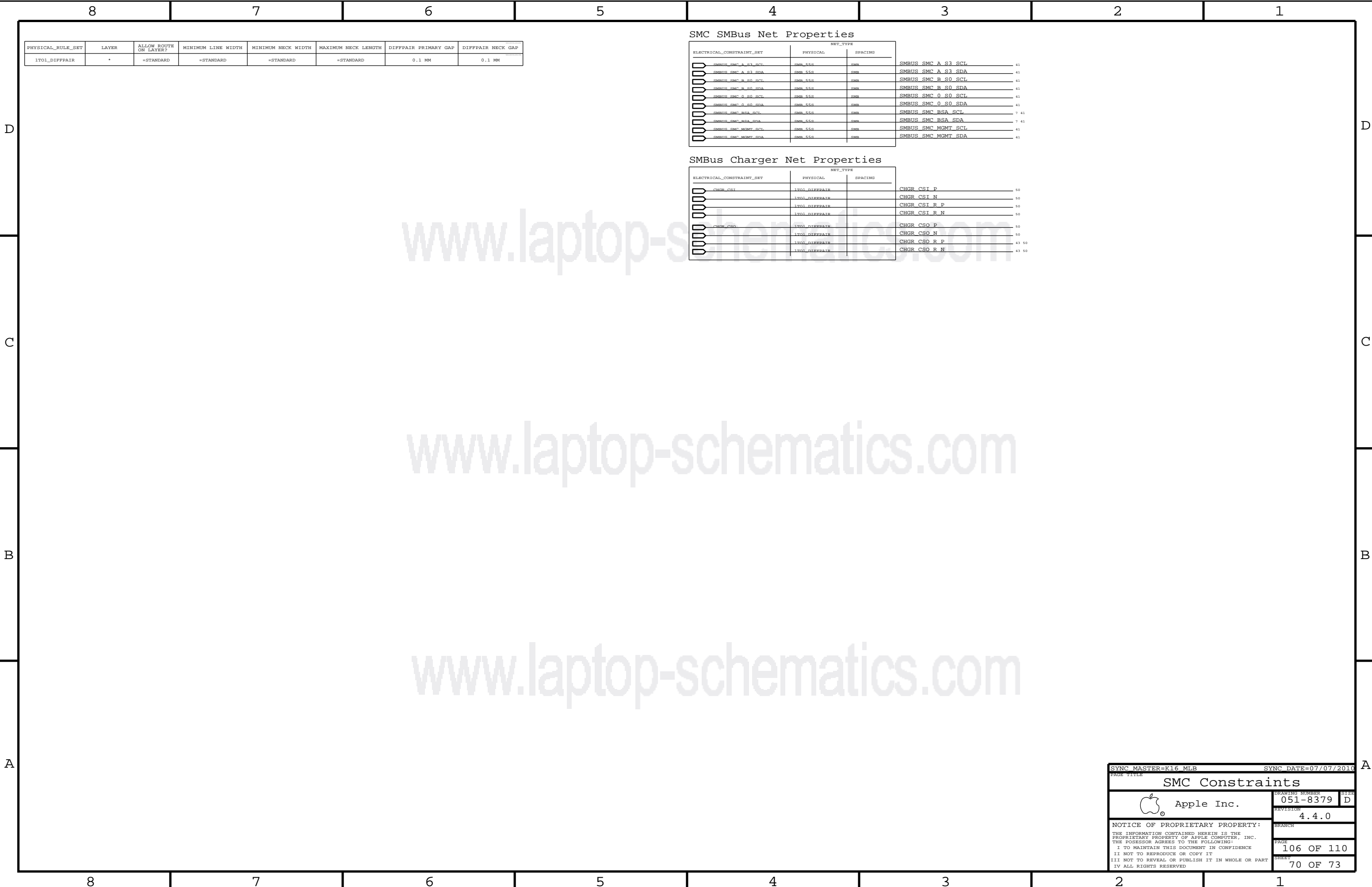
AB

## D

C

## B

A



D

C

B

A

D

C

B

A

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=1:1_SPACING	?
THERM	*	=1:1_SPACING	?
AUDIO	*	=1:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
MEM_POWER	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_POWER	*	PWR_P2MM
MEM_CMD	MEM_POWER	*	PWR_P2MM
MEM_CTRL	MEM_POWER	*	PWR_P2MM
MEM_DATA	MEM_POWER	*	PWR_P2MM
MEM_DQS	MEM_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

## SD CARD READER LAYOUT RELAXATIONS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_5S5 OVERRIDE	* OVERRIDE	OVERRIDE	=STANDARD OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

## MCP Fanout Constraint Relaxations

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	5.8 MM OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	TOP	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP OVERRIDE	TOP	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP OVERRIDE	TOP	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS OVERRIDE	TOP	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	*	OVERRIDE	OVERRIDE	0.25 MM OVERRIDE	250 MIL OVERRIDE	OVERRIDE	OVERRIDE


































## Misc Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	(USB_EXTN)	1500 90D	1500	USB_EXTN_MUXED_P	36 68
	(USB_EXTN)	1500 90D	1500	USB_EXTN_MUXED_N	36 68
	(USB_EXTN)	1500 90D	1500	USB LT1_P	36
	(USB_EXTN)	1500 90D	1500	USB LT1_N	36
	(USB_TPAD)	1500 90D	1500	USB_TPAD_P	18 46
	(USB_TPAD)	1500 90D	1500	USB_TPAD_N	18 46
	(USB_TPAD)	1500 90D	1500	USB_TPAD_CONN_P	7 46
	(USB_TPAD)	1500 90D	1500	USB_TPAD_CONN_N	7 46
	SMR512C_SMC_MGMT_SDA	SMR_55G	SMR	I2C_SMC_SMS_SDA_R	
	SMR512C_SMC_MGMT_SCL	SMR_55G	SMR	I2C_SMC_SMS_SCL_R	
		SMR_55G	SMR	I2C_TCON_SCL	41
		SMR_55G	SMR	I2C_TCON_SDA	41
		SMR_55G	SMR	I2C_TCON_SCL_CONN	
		SMR_55G	SMR	I2C_TCON_SDA_CONN	





## Graphics Net Properties


ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
	DP_90D	DISPLAYPORT	DP INT ML P<1..0>	9 59
	DP_90D	DISPLAYPORT	DP INT ML N<1..0>	9 59
	DP_90D	DISPLAYPORT	DP INT ML C P<1..0>	59
	DP_90D	DISPLAYPORT	DP INT ML C N<1..0>	59
	DP_90D	DISPLAYPORT	DP INT ML F P<1..0>	7 59
	DP_90D	DISPLAYPORT	DP INT ML F N<1..0>	7 59
	DP_90D	DISPLAYPORT	DP INT AUX CH C P	7 59
	DP_90D	DISPLAYPORT	DP INT AUX CH C N	7 59
	DP_90D	DISPLAYPORT	DP INT AUX CH P	9 59
	DP_90D	DISPLAYPORT	DP INT AUX CH N	9 59
(DP_EXT_ML)	DP_90D	DISPLAYPORT	DP EXT ML P<3..0>	9 61
	DP_90D	DISPLAYPORT	DP EXT ML N<3..0>	9 61
	DP_90D	DISPLAYPORT	DP EXT ML C P<3..0>	61
	DP_90D	DISPLAYPORT	DP EXT ML C N<3..0>	61
	DP_90D	DISPLAYPORT	DP EXT ML F P<3..0>	61
	DP_90D	DISPLAYPORT	DP EXT ML F N<3..0>	61
(DP_EXT_AUX_CH)	DP_90D	DISPLAYPORT	DP EXT AUX CH C P	9 61
	DP_90D	DISPLAYPORT	DP EXT AUX CH C N	9 61

## Power Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		SPACING			
		PHYSICAL	SPACING				
	CPIPTHMSNS_D2	THERM_1T01_55S	THERM	DRAMTHMSNS D2 P		44	
		THERM_1T01_55S	THERM	DRAMTHMSNS D2 N			
	CPU_THERMD	THERM_1T01_55S	THERM	CPU THERMD P		10	44
		THERM_1T01_55S	THERM	CPU THERMD N		10	44
	MCPPTHMSNS_D2	THERM_1T01_55S	THERM	MLBR THMDIODE P		44	
		THERM_1T01_55S	THERM	MLBR THMDIODE N			
	MCP_THMDIODE	THERM_1T01_55S	THERM	MCP THMDIODE P		19	44
		THERM_1T01_55S	THERM	MCP THMDIODE N		19	44
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS 1V5_S3 P		42	52
		SENSE_1T01_55S	SENSE	ISNS 1V5_S3 N			
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS AIRPORT P		34	42
		SENSE_1T01_55S	SENSE	ISNS AIRPORT N		34	42
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS CSREG P		43	
		SENSE_1T01_55S	SENSE	ISNS CSREG N			
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS HDD P		35	42
		SENSE_1T01_55S	SENSE	ISNS HDD N		35	42
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS LCDBKLT P		42	62
		SENSE_1T01_55S	SENSE	ISNS LCDBKLT N		42	62
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUVTT50 CS P		55	
		SENSE_1T01_55S	SENSE	CPUVTT50 CS N		55	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	IMVP6 CS P		53	
		SENSE_1T01_55S	SENSE	IMVP6 CS N		53	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	IMVP6 CS R P		53	
		SENSE_1T01_55S	SENSE	IMVP6 CS R N		53	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPU VTTSENSE P		55	
		SENSE_1T01_55S	SENSE	CPU VTTSENSE N		55	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	MPCCORES0 VSEN P		22	54
		SENSE_1T01_55S	SENSE	MPCCORES0 VSEN N		22	54
			MEM_POWER	PPIV5R1V35 S3		7	8
			SB_POWER	PP3V3 S5		7	8 57
			SB_POWER	PP3V3 S0		7	8 57
			SB_POWER	PPIV5 S0		7	8 57
			GND	GND			

## Audio Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	SPKRAMP_INR	DIFFPAIR	AUDIO	SPKRAMP_INR_P 7 37 48
		DIFFPAIR	AUDIO	SPKRAMP_INR_N 7 37 48
	MAX98300_R	DIFFPAIR	AUDIO	MAX98300_R_P 48
		DIFFPAIR	AUDIO	MAX98300_R_N 48

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K99 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS			BOARD AREAS			BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM			NO_TYPE, BGA			MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.100 MM	0.076 MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
27P4_OHM_SE	ISL3, ISL10	Y	0.250 MM	0.250 MM			
27P4_OHM_SE	ISL4, ISL9	Y	0.250 MM	0.250 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	TOP, BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL3, ISL4, ISL9, ISL10	Y	0.140 MM	0.140 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP, BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	ISL3, ISL4, ISL9, ISL10	Y	0.090 MM	0.090 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	ISL3, ISL4, ISL9, ISL10	Y	0.076 MM	0.076 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	TOP, BOTTOM	Y	0.175 MM	0.175 MM		0.130 MM	0.130 MM
70_OHM_DIFF	ISL3, ISL10	Y	0.135 MM	0.135 MM		0.130 MM	0.130 MM
70_OHM_DIFF	ISL4, ISL9	Y	0.155 MM	0.155 MM		0.130 MM	0.130 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.160 MM	0.160 MM
80_OHM_DIFF	ISL3, ISL10	Y	0.109 MM	0.109 MM		0.160 MM	0.160 MM
80_OHM_DIFF	ISL4, ISL9	Y	0.125 MM	0.125 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
75_OHM_DIFF	TOP, BOTTOM	Y	0.160 MM	0.160 MM		0.160 MM	0.160 MM
75_OHM_DIFF	ISL3, ISL10	Y	0.120 MM	0.120 MM		0.140 MM	0.140 MM
75_OHM_DIFF	ISL4, ISL9	Y	0.140 MM	0.140 MM		0.140 MM	0.140 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL3, ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL4, ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
95_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
95_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM
95_OHM_DIFF	ISL3, ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
95_OHM_DIFF	ISL4, ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	TOP, BOTTOM	Y	0.091 MM	0.091 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL3, ISL10	Y	0.075 MM	0.075 MM		0.300 MM	0.300 MM
100_OHM_DIFF	ISL4, ISL9	Y	0.085 MM	0.085 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.28:1_SPACING	*	0.228 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PPIV5_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
NB_STATIC	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
1.5X_DIELECTRIC	*	0.105 MM	?
5X_DIELECTRIC	*	0.350 MM	?

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SYNC MASTER=K16 MLB

SYNC DATE=07/07/2010

K99 RULE DEFINITIONS

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1UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS																	
SAMSUNG						MURATA						TAIYO YUDEN					
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0629	2	CAP, 1UF, 6.3V, 10%, 0402	C7303,C7360	CRITICAL	SS_CAP_1UF	138S0628	2	CAP, 1UF, 6.3V, 10%, 0402	C7303,C7360	CRITICAL	MU_CAP_1UF	138S0630	2	CAP, 1UF, 6.3V, 10%, 0402	C7303,C7360	CRITICAL	TY_CAP_1UF
2.2UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS																	
SAMSUNG						MURATA						TAIYO YUDEN					
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1246,C1246,C1247,C1247,C1248,C1248	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1246,C1246,C1247,C1247,C1248,C1248	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1246,C1246,C1247,C1247,C1248,C1248	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1261,C1262,C1263,C1264,C1266,C1266,C1267,C1267,C1268,C1268	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1261,C1262,C1263,C1264,C1266,C1266,C1267,C1267,C1268,C1268	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1261,C1262,C1263,C1264,C1266,C1266,C1267,C1267,C1268,C1268	CRITICAL	TY_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1289,C1291,C1292,C1293,C1294,C1295,C1296,C1296	CRITICAL	SS_CAP_2_2UF	138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1289,C1291,C1292,C1293,C1294,C1295,C1296,C1296	CRITICAL	MU_CAP_2_2UF	138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1289,C1291,C1292,C1293,C1294,C1295,C1296,C1296	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3901,C3902,C3903,C3904,C3905,C3906,C3907,C3907	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3901,C3902,C3903,C3904,C3905,C3906,C3907,C3907	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3901,C3902,C3903,C3904,C3905,C3906,C3907,C3907	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3911,C3912,C3913,C3914,C3915,C3916,C3917,C3917	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3911,C3912,C3913,C3914,C3915,C3916,C3917,C3917	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3911,C3912,C3913,C3914,C3915,C3916,C3917,C3917	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3921,C3922,C3923,C3924,C3925,C3926,C3927,C3927	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3921,C3922,C3923,C3924,C3925,C3926,C3927,C3927	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3921,C3922,C3923,C3924,C3925,C3926,C3927,C3927	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3931,C3932,C3933,C3934,C3935,C3936,C3937,C3937	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3931,C3932,C3933,C3934,C3935,C3936,C3937,C3937	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3931,C3932,C3933,C3934,C3935,C3936,C3937,C3937	CRITICAL	TY_CAP_2_2UF
138S0632	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1289,C1289,C1287,C1288,C1291,C1292,C1293,C1293	CRITICAL	SS_CAP_2_2UF	138S0633	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1289,C1289,C1287,C1288,C1291,C1292,C1293,C1293	CRITICAL	MU_CAP_2_2UF	138S0634	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1289,C1289,C1287,C1288,C1291,C1292,C1293,C1293	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3901,C3904,C3905,C3910,C3911,C3912,C3914,C3914	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3901,C3904,C3905,C3910,C3911,C3912,C3914,C3914	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3901,C3904,C3905,C3910,C3911,C3912,C3914,C3914	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3921,C3924,C3925,C3930,C3931,C3934,C3935,C3935	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3921,C3924,C3925,C3930,C3931,C3934,C3935,C3935	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3921,C3924,C3925,C3930,C3931,C3934,C3935,C3935	CRITICAL	TY_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3943,C3944,C3945,C3946,C3950,C3951,C3954,C3954	CRITICAL	SS_CAP_2_2UF	138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3943,C3944,C3945,C3946,C3950,C3951,C3954,C3954	CRITICAL	MU_CAP_2_2UF	138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3943,C3944,C3945,C3946,C3950,C3951,C3954,C3954	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3901,C3904,C3905,C3910,C3911,C3912,C3914,C3914	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3901,C3904,C3905,C3910,C3911,C3912,C3914,C3914	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3901,C3904,C3905,C3910,C3911,C3912,C3914,C3914	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3921,C3924,C3925,C3930,C3931,C3934,C3935,C3935	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3921,C3924,C3925,C3930,C3931,C3934,C3935,C3935	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3921,C3924,C3925,C3930,C3931,C3934,C3935,C3935	CRITICAL	TY_CAP_2_2UF
138S0632	9	CAP, 2.2UF, 6.3V, 20%, 0402	C3943,C3944,C3945,C3946,C3950,C3951,C3954,C3955	CRITICAL	SS_CAP_2_2UF	138S0633	9	CAP, 2.2UF, 6.3V, 20%, 0402	C3943,C3944,C3945,C3946,C3950,C3951,C3954,C3955	CRITICAL	MU_CAP_2_2UF	138S0634	9	CAP, 2.2UF, 6.3V, 20%, 0402	C3943,C3944,C3945,C3946,C3950,C3951,C3954,C3955	CRITICAL	TY_CAP_2_2UF
10UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS																	
SAMSUNG						MURATA						TAIYO YUDEN					
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0626	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	SS_CAP_10UF	138S0625	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	MU_CAP_10UF	138S0627	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	TY_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C3900,C4909,C5025,C7209,C7209,C7349,C7355,C7355	CRITICAL	SS_CAP_10UF	138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C3900,C4909,C5025,C7209,C7209,C7349,C7355,C7355	CRITICAL	MU_CAP_10UF	138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C3900,C4909,C5025,C7209,C7209,C7349,C7355,C7355	CRITICAL	TY_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C3911,C3946,C3950,C3920,C3960,C3967,C3967,C3967	CRITICAL	SS_CAP_10UF	138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C3911,C3946,C3950,C3920,C3960,C3967,C3967,C3967	CRITICAL	MU_CAP_10UF	138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C3911,C3946,C3950,C3920,C3960,C3967,C3967,C3967	CRITICAL	TY_CAP_10UF
22UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS																	
SAMSUNG						MURATA						TAIYO YUDEN					
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0635	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1214,C1217,C1218	CRITICAL	SS_CAP_22UF	138S0676	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1214,C1217,C1218	CRITICAL	MU_CAP_22UF	138S0688	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1214,C1217,C1218	CRITICAL	TY_CAP_22UF
138S0635	3	CAP, 22UF, 6.3V, 20%, 0603	C1223,C1226,C1227	CRITICAL	SS_CAP_22UF	138S0676	3	CAP, 22UF, 6.3V, 20%, 0603	C1223,C1226,C1227	CRITICAL	MU_CAP_22UF	138S0688	3	CAP, 22UF, 6.3V, 20%, 0603	C1223,C1226,C1227	CRITICAL	TY_CAP_22UF
138S0635	5	CAP, 22UF, 6.3V, 20%, 0603	C1230,C4902,C7360,C7361,C9480	CRITICAL	SS_CAP_22UF	138S0676	5	CAP, 22UF, 6.3V, 20%, 0603	C1230,C4902,C7360,C7361,C9480	CRITICAL	MU_CAP_22UF	138S0688	5	CAP, 22UF, 6.3V, 20%, 0603	C1230,C4902,C7360,C7361,C9480	CRITICAL	TY_CAP_22UF
SYNC MASTER=K16 MLB SYNC DATE=07/07/2010																	
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