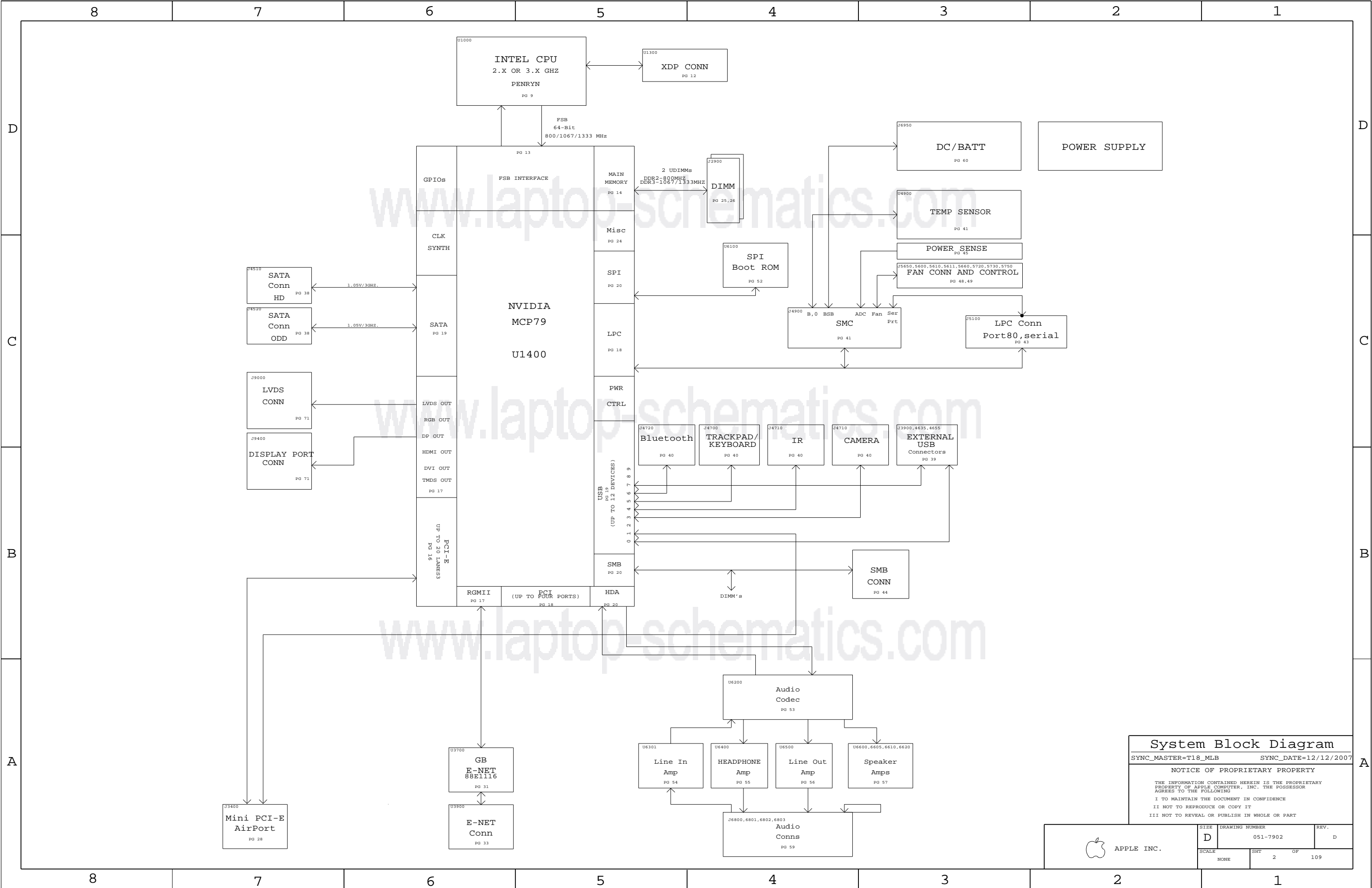
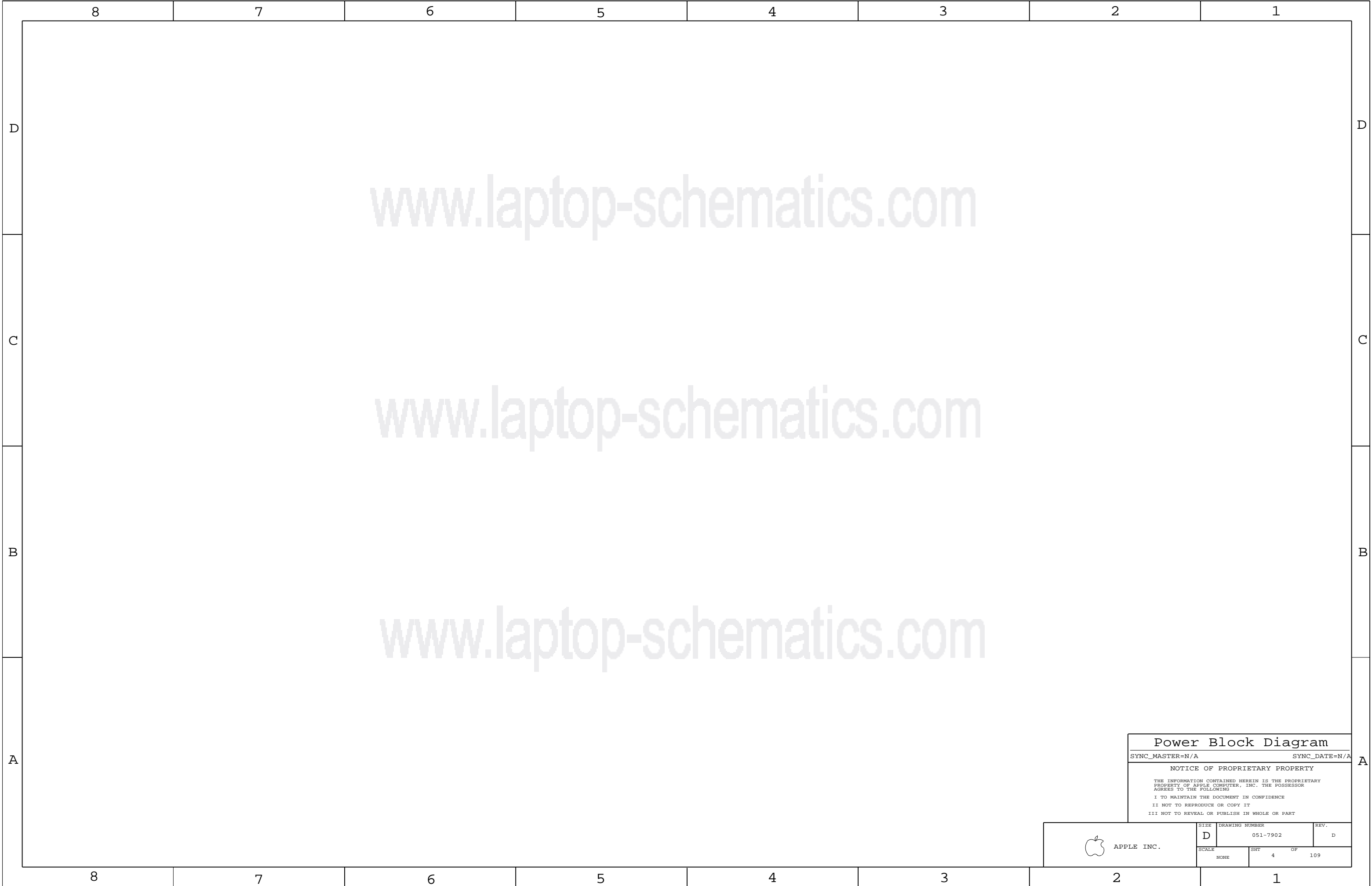



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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.												REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD				
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.																DATE	DATE				
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.												D		669438	PRODUCTION RELEASED	02/02/09	09				
SCHEMATIC , MBP15 " , "Contuba " MLB																					
D	Page		Contents		Sync		Page		Contents		Sync		Page		Contents		Sync		D		
	1		Table of Contents		N/A		46		Current & Voltage Sensing		SENSOR		91		Ethernet Constraints		MUXGFX				
	2		System Block Diagram		T18_MLB		47		Current Sensing		SENSOR		92		FireWire Constraints		MUXGFX				
	3		Power Block Diagram		T18_MLB		48		Thermal Sensors		SENSOR		93		SMC Constraints		MUXGFX				
	4		Power Block Diagram		N/A		49		Fan Connectors		M87_MLB		94		GPU (G96) Constraints		MUXGFX				
	5		BOM Configuration		N/A		50		WELLSPRING 1		AMASON_M98_MLB		95		Project Specific Constraints		MUXGFX				
	6		JTAG Scan Chain		DDR		51		WELLSPRING 2		PWRSQNC		96		PCB Rule Definitions		M99_MLB				
	7		Functional / ICT Test		N/A		52		Sudden Motion Sensor (SMS)		SENSOR										
	8		Power Aliases		(MASTER)		53		SPI ROM		CHANG_M98_MLB										
	9		Signal Aliases		(MASTER)		54		AUDIO:CODEC		AUDIO										
	10		CPU FSB		M87_MLB		55		AUDIO: LINE IN		AUDIO										
	11		CPU Power & Ground		M87_MLB		56		AUDIO: HEADPHONE AMP		AUDIO										
	12		CPU Decoupling & VID		M87_MLB		57		AUDIO:SPEAKER AMP		AUDIO										
	13		eXtended Debug Port(MiniXDP)		M99_MLB		58		AUDIO: JACKS		AUDIO										
	14		MCP CPU Interface		T18_MLB		59		AUDIO: JACK TRANSLATORS		AUDIO										
	15		MCP Memory Interface		T18_MLB		60		DC-In & Battery Connectors		T18_MLB										
	16		MCP Memory Misc		T18_MLB		61		PBus Supply & Battery Charger		M99_MLB										
	17		MCP PCIe Interfaces		T18_MLB		62		IMVP6 CPU VCore Regulator		M87_MLB										
	18		MCP Ethernet & Graphics		T18_MLB		63		5V / 3.3V Power Supply		M99_MLB										
	19		MCP PCI & LPC		T18_MLB		64		1.5V DDR3 Supply		M99_MLB										
	20		MCP SATA & USB		T18_MLB		65		5V_S0 / MCP Core Regulator		M99_MLB										
	21		MCP HDA & MISC		T18_MLB		66		CPU VTT Power Supply		M99_MLB										
	22		MCP Power & Ground		T18_MLB		67		Misc Power Supplies		M99_MLB										
	23		MCP79 A01 Silicon Support		T18_MLB		68		Power Control		PWRSQNC										
	24		MCP Standard Decoupling		T18_MLB		69		Power FETs		PWRSQNC										
	25		MCP Graphics Support		AMASON_M98_MLB		70		NV G96 PCI-E		MUXGFX										
	26		SB Misc		T18_MLB		71		NV G96 Core/FB Power		MUXGFX										
	27		FSB/DDR3/FRAMEBUF Vref Margining		DDR		72		NV G96 Frame Buffer I/F		MUXGFX										
	28		DDR3 SO-DIMM Connector A		DDR		73		GDDR3 Frame Buffer A (Top)		MUXGFX										
	29		DDR3 SO-DIMM Connector B		DDR		74		GDDR3 Frame Buffer B (Top)		MUXGFX										
	30		DDR3 Support		T18_MLB		75		NV G96 GPIO/MIO/Misc		MUXGFX										
	31		Right Clutch Connector		YITE_M98_MLB		76		G96 GPIOs & Straps		MUXGFX										
	32		ExpressCard Connector		YITE_M98_MLB		77		NV G96 Video Interfaces		MUXGFX										
	33		Ethernet PHY (RTL8211CL)		SUMA_M98_MLB		78		GPU (G84M) Core Supply		M87_MLB										
	34		Ethernet & AirPort Support		SUMA_M98_MLB		79		LVDS Display Connector		MUXGFX										
	35		Ethernet Connector		SUMA_M98_MLB		80		Muxed Graphics Support		MUXGFX										
	36		FireWire LLC/PHY (FW643)		SENSOR		81		DisplayPort Connector		MUXGFX										
	37		FireWire Port Power		K19_MLB		82		1.1V / 1V8 FB Power Supply		MUXGFX										
	38		FireWire Ports		SENSOR		83		Graphics MUX (GMUX)		MUXGFX										
	39		SATA Connectors		CHANG_M98_MLB		84		LCD BACKLIGHT DRIVER		YITE_M98_MLB										
	40		External USB Connectors		AMASON_M98_MLB		85		LCD Backlight Support		YITE_M98_MLB										
	41		Front Flex Support		CHANG_M98_MLB		86		Misc Power Supplies		MUXGFX										
	42		SMC		T18_MLB		87		CPU/FSB Constraints		MUXGFX										
	43		SMC Support		AMASON_M98_MLB		88		Memory Constraints		MUXGFX										
	44		LPC+SPI Debug Connector		CHANG_M98_MLB		89		MCP Constraints 1		MUXGFX										
	45		M98 SMBus Connections		DDR		90		MCP Constraints 2		MUXGFX										
02/02/2009																					
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Power Block Diagram		
SYNC_MASTER=N/A		SYNC_DATE=N/A
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D	051-7902	D
SCALE	SHT OF	
NONE	4 109	

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9911	PCBA, 2.4GHZ, 256SAM_VRAM, HB_AUDIO, M98A	M98_COMMON, EEE_6DZ, CPU_2_4GHZ, FB_256_SAMSUNG, AUDIO_HB
630-9912	PCBA, 2.4GHZ, 256HYN_VRAM, HB_AUDIO, M98A	M98_COMMON, EEE_6EA, CPU_2_4GHZ, FB_256_HYNIX, AUDIO_HB
630-9913	PCBA, 2.5GHZ, 512SAM_VRAM, HB_AUDIO, M98A	M98_COMMON, EEE_6EB, CPU_2_5GHZ, FB_512_SAMSUNG, AUDIO_HB
630-9914	PCBA, 2.5GHZ, 512QIM_VRAM, HB_AUDIO, M98A	M98_COMMON, EEE_6EC, CPU_2_5GHZ, FB_512_QIMONDA, AUDIO_HB
630-9915	PCBA, 2.8GHZ, 512SAM_VRAM, HB_AUDIO, M98A	M98_COMMON, EEE_6ED, CPU_2_8GHZ, FB_512_SAMSUNG, AUDIO_HB
630-9916	PCBA, 2.8GHZ, 512QIM_VRAM, HB_AUDIO, M98A	M98_COMMON, EEE_6EE, CPU_2_8GHZ, FB_512_QIMONDA, AUDIO_HB
630-9949	PCBA, 2.66GHZ, 512SAM_VRAM, HB_AUDIO, M98A	M98_COMMON, EEE_6MT, CPU_2_66GHZ, FB_512_SAMSUNG, AUDIO_HB
630-9950	PCBA, 2.66GHZ, 512QIM_VRAM, HB_AUDIO, M98A	M98_COMMON, EEE_6MU, CPU_2_66GHZ, FB_512_QIMONDA, AUDIO_HB
630-9951	PCBA, 2.93GHZ, 512SAM_VRAM, HB_AUDIO, M98A	M98_COMMON, EEE_6N1, CPU_2_93GHZ, FB_512_SAMSUNG, AUDIO_HB
630-9952	PCBA, 2.93GHZ, 512QIM_VRAM, HB_AUDIO, M98A	M98_COMMON, EEE_6N2, CPU_2_93GHZ, FB_512_QIMONDA, AUDIO_HB
630-9956	PCBA, 2.5GHZ, 512HYN_VRAM, HB_AUDIO, M98A	M98_COMMON, EEE_6VG, CPU_2_5GHZ, FB_512_HYNIX, AUDIO_HB
630-9957	PCBA, 2.66GHZ, 512HYN_VRAM, HB_AUDIO, M98A	M98_COMMON, EEE_6VH, CPU_2_66GHZ, FB_512_HYNIX, AUDIO_HB
630-9958	PCBA, 2.8GHZ, 512HYN_VRAM, HB_AUDIO, M98A	M98_COMMON, EEE_6VJ, CPU_2_8GHZ, FB_512_HYNIX, AUDIO_HB
630-9959	PCBA, 2.93GHZ, 512HYN_VRAM, HB_AUDIO, M98A	M98_COMMON, EEE_6VK, CPU_2_93GHZ, FB_512_HYNIX, AUDIO_HB

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:6DZ]	CRITICAL	EEE_6DZ
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:6EA]	CRITICAL	EEE_6EA
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:6EB]	CRITICAL	EEE_6EB
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:6EC]	CRITICAL	EEE_6EC
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:6ED]	CRITICAL	EEE_6ED
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:6EE]	CRITICAL	EEE_6EE
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:6MT]	CRITICAL	EEE_6MT
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:6MU]	CRITICAL	EEE_6MU
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:6N1]	CRITICAL	EEE_6N1
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:6N2]	CRITICAL	EEE_6N2
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:6VG]	CRITICAL	EEE_6VG
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:6VH]	CRITICAL	EEE_6VH
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:6VJ]	CRITICAL	EEE_6VJ
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:6VK]	CRITICAL	EEE_6VK

Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602		ALL	Murata alt to Samsung
353S1681	353S1294		ALL	LMV2011, GPAMP, GEM
152S0276	152S0683		ALL	Maglayers alt to Dale/Tishay
341S2367	341S2366		ALL	Maximic alt to SST
152S0876	152S0867		ALL	Maglayers alt to Delta
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
152S0915	152S0796		ALL	Maglayers alt to Cyntec IHD
128S0262	128S0220		ALL	Kemet alt to Sanyo
127S0108	127S0062		ALL	Kohm alt to Kemet
338S0714	338S0554		ALL	Low Leakage G96 GPU

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7902	1	SCHEM, FIBBA, M98	SCH	CRITICAL	
820-2532	1	PCBF, FIBBA, M98	PCB	CRITICAL	

BOM Groups

BOM GROUP	BOM OPTIONS
M98_COMMON	ALTERNATE,COMMON,M98_COMMON1,M98_COMMON2,M98_COMMON3,M98_DEBUG,M98_PROGPARTS
M98_COMMON1	ONEWIRE_PU,ISL6258A,MEMRESET_HW,MEMRESET_MCP,MCP_B03,MCP_PROD,MCPSEQ_SMC
M98_COMMON2	FW_LVG_NEW,BKLT_PLL_NOT,BMON_PROD,MIKEY,BOOT_MODE_USER,GPUVID_1P00V,MUXGFX
M98_COMMON3	DPMUX_EN_S0,DP_ESD,EG_PWRSEQ_HW,DP_CA_DET_EG_PLD,MCP_CS1_NO,NO_VREFMRGN,PROD_DIGSMS
M98_DEBUG	SMC_DEBUG_YES,XDP,LPCPLUS_NOT
M98_PROGPARTS	GMUX_PROG,BOOTROM_PROG,SMC_PROG,TPAD_PROG

BOM GROUP	BOM OPTIONS
FB_256_SAMSUNG	VRAM4 , VRAM_256_SAMSUNG
FB_256_HYNIX	VRAM4 , VRAM_256_HYNIX
FB_512_SAMSUNG	VRAM4 , VRAM_512_SAMSUNG
FB_512_HYNIX	VRAM4 , VRAM_512_HYNIX
FB_512_QIMONDA	VRAM4 , VRAM_512_QIMONDA

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3680	1	IC,PDC,LDZD,FRQ,2.40,35W,1066,R0,3M,BGA	U1000	CRITICAL	CPU_2_4GHZ
337S3681	1	IC,PDC,SLGEK,FRQ,2.53,35W,1066,R0,6M,BGA	U1000	CRITICAL	CPU_2_5GHZ
337S3710	1	IC,PDC,SLGEL,FRQ,2.66,35W,1066,R0,6M,BGA	U1000	CRITICAL	CPU_2_66GHZ
337S3682	1	IC,PDC,SLGEM,FRQ,2.80,35W,1066,R0,6M,BGA	U1000	CRITICAL	CPU_2_8GHZ
337S3711	1	IC,PDC,SLGEP,FRQ,2.93,35W,1066,R0,6M,BGA	U1000	CRITICAL	CPU_2_93GHZ
338S0635	1	IC,GMCP,MCP79-B02,35x35MM,BGA1437	U1400	CRITICAL	MCP_B02
338S0710	1	IC,MCP79XT-B3,35x35MM,BGA1437	U1400	CRITICAL	MCP_B03
338S0694	1	IC,RTL8251CA-V8-GR,GIGE TRANSCEIVER,48P TQFP	U3700	CRITICAL	
338S0654	1	IC,PW43-E,1394B PHY/ONCI LINK/PCI-E,12	U4100	CRITICAL	
341S2384	1	IR,ENCORE II, CV7C63803-LQXC	U4800	CRITICAL	
338S0563	1	IC,SMC,HS8/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341S2448	1	IC,SMC,DEVELOPMENT,M98	U4900	CRITICAL	SMC_PROG
341S2383	1	IC,PSOC +W/USB,56PIN,MLF,M98	U5701	CRITICAL	TPAD_PROG
335S0384	1	IC,32MBIT 8-PIN SPI SERIAL FLASH,SOIC8	U6100	CRITICAL	BOOTROM_BLANK
341S2447	1	IC,EPI ROM,DEVELOPMENT,M98	U6100	CRITICAL	BOOTROM_PROG
514-0612	1	CONN,RCPT,S/PDIF,3.5MM,COMBO,XCVR,FL	J6700	CRITICAL	AUDIO_NOHB
514-0634	1	CONN,RCPT,S/PDIF,3.5MM,COMBO,HB,FL	J6700	CRITICAL	AUDIO_HB
514-0613	1	CONN,RCPT,S/PDIF,3.5MM,COMBO,RX,FL	J6750	CRITICAL	AUDIO_NOHB
514-0635	1	CONN,RCPT,S/PDIF,3.5MM,COMBO,RX,HB,FL	J6750	CRITICAL	AUDIO_HB
353S2312	1	IC,ISL6236C,DUAL PWM CNTL,QFN32	U7500	CRITICAL	
338S0554	1	IC,GPU,55nm,NV GS-6G,BGA969,LF	U8000	CRITICAL	
333S0482	4	IC,SGRAM,GDDR3,16Mx32,800MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_SAMSUNG
333S0483	4	IC,SGRAM,GDDR3,16Mx32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_HYNIX
333S0481	4	IC,SGRAM,GDDR3,32Mx32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_SAMSUNG
333S0506	4	IC,SGRAM,GDDR3,32Mx32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_HYNIX
333S0472	4	IC,SGRAM,GDDR3,32Mx32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_QIMONDA
341S2272	1	IC,HDCP ROM,NV96G, 8 PIN SOIC,LF,HF	U8770	CRITICAL	HDCP_YES

BOM Configuration

SYNC_MASTER=N/A	SYNC_DATE=N/A
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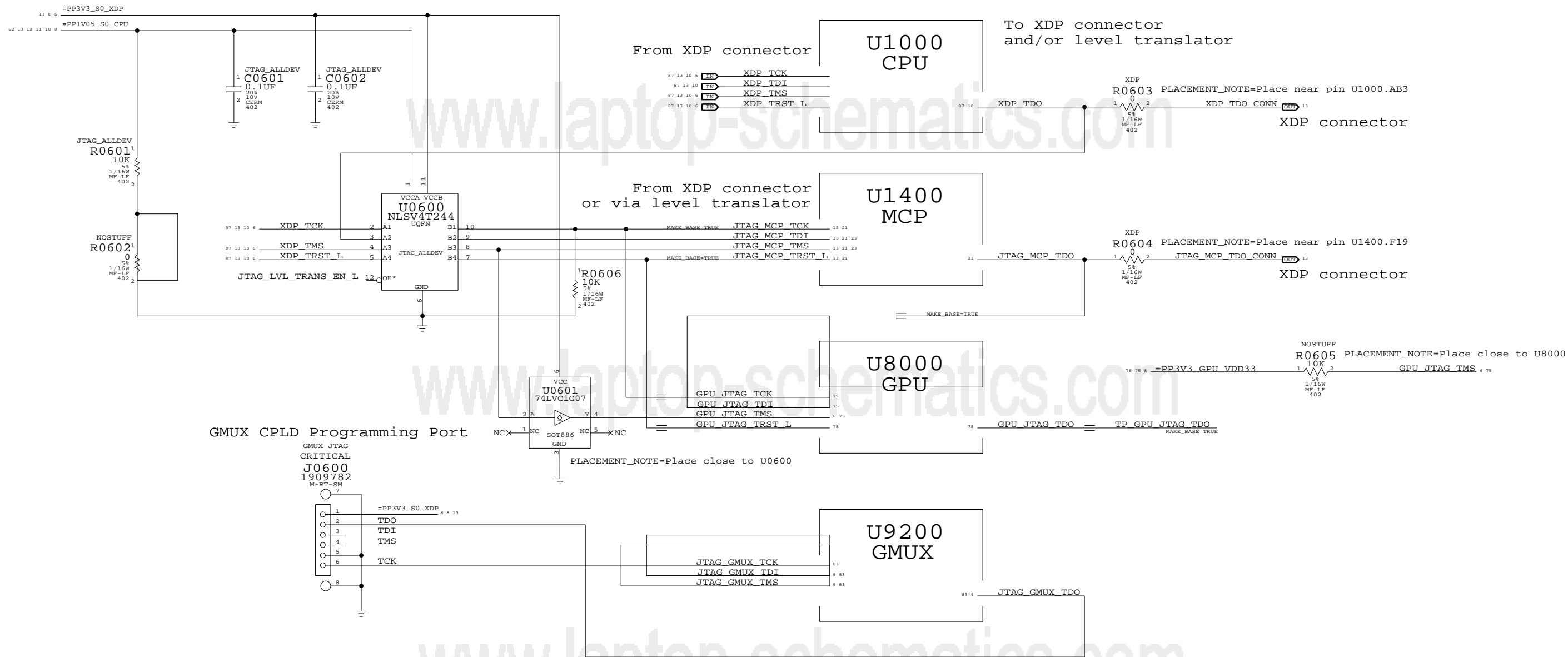
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1.05V TO 3.3V LEVEL TRANSLATOR (M98: ON ICT FIXTURE)



JTAG Scan Chain	
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8	7	6	5	4	3	2	1			
Functional Test Points				ICT Test Points						
Fan Connectors				CPU FSB NO_TESTS						
FUNC_TEST				NO_TEST						
D	3 TPs per Fan			TRUE FSB A L<31..3> 10 14 87						
	TRUE FAN LT PWM 49			TRUE FSB ADS L 10 14 87						
	TRUE FAN LT TACH 49			TRUE FSB ADSTB L<1..0> 10 14 87						
	TRUE FAN RT PWM 49			TRUE FSB D L<63..0> 10 14 87						
	TRUE FAN RT TACH 49			TRUE FSB DINV L<3..0> 10 14 87						
5 TPs per Fan				TRUE FSB DSTB L N<3..0> 10 14 87						
TRUE FSB DSTB L P<3..0> 10 14 87										
TRUE FSB HIT L 10 14 87										
LVDS Connectors				TRUE FSB HITM L 10 14 87						
TRUE FSB LOCK L 10 14 87										
TRUE FSB REQ L<4..0> 10 14 87										
C	FUNC_TEST			IPD_FLEX_CONN						
	TRUE =PP3V3_S0_DDC_LCD 8 76 79			TRUE PP3V3_S3_LDO 51						
	TRUE PP3V3_SW_LCD 79			TRUE PP18V5_S3 51						
	TRUE BKL_SYNC 79 84			TRUE TPAD_GND_F 7 51						
	TRUE LVDS_DDC_CLK 79 80			TRUE Z2_CS_L 50 51						
TRUE LVDS_DDC_DATA 79 80				TRUE Z2_DEBUG3 50 51						
TRUE LVDS_CONN_A_DATA_N<0> 79 80 94				TRUE Z2_MOSI 50 51						
TRUE LVDS_CONN_A_DATA_P<0> 79 80 94				TRUE Z2_MISO 50 51						
TRUE LVDS_CONN_A_DATA_N<1> 79 80 94				TRUE Z2_SCLK 50 51						
TRUE LVDS_CONN_A_DATA_P<1> 79 80 94				TRUE Z2_BOOST_EN 51						
TRUE LVDS_CONN_A_DATA_N<2> 79 80 94				TRUE Z2_HOST_INTN 50 51						
TRUE LVDS_CONN_A_DATA_P<2> 79 80 94				TRUE Z2_BOOT_CFG1 50 51						
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TRUE LVDS_CONN_A_CLK_F_P 79 94				TRUE Z2_KEY_ACT_L 50 51						
TRUE LVDS_CONN_B_DATA_N<0> 79 80 94				TRUE Z2_RESET 50 51						
TRUE LVDS_CONN_B_DATA_P<0> 79 80 94				TRUE PSOC_MISO 50 51						
TRUE LVDS_CONN_B_DATA_N<1> 79 80 94				TRUE PSOC_MOSI 50 51						
TRUE LVDS_CONN_B_DATA_P<1> 79 80 94				TRUE PSOC_SCLK 50 51						
TRUE LVDS_CONN_B_DATA_N<2> 79 80 94				TRUE SMBUS_SMC_A_S3_SDA 45 93						
TRUE LVDS_CONN_B_DATA_P<2> 79 80 94				TRUE SMBUS_SMC_A_S3_SCL 45 93						
TRUE LVDS_CONN_B_CLK_F_N 79 94				TRUE PSOC_F_CS_L 50 51						
TRUE LVDS_CONN_B_CLK_F_P 79 94				TRUE PICKB_L 50 51						
B	LED_RETURN_1 79 84									
	LED_RETURN_2 79 84									
	LED_RETURN_3 79 84									
	LED_RETURN_4 79 84									
	LED_RETURN_5 79 84									
LED_RETURN_6 79 84										
EXCARD Connector										
FUNC_TEST				KEYBOARD CONN						
TRUE USB2_EXCARD_CONN_N 32 95				TRUE PP3V42_G3H 7 8 43						
TRUE USB2_EXCARD_CONN_P 32 95				TRUE WS_KBD1 50						
TRUE PCIE_CLK100M_EXCARD_CONN_N 32 95				TRUE WS_KBD2 50						
TRUE PCIE_CLK100M_EXCARD_CONN_P 32 95				TRUE WS_KBD3 50						
TRUE PCIE_EXCARD_R2D_N 32 89 95				TRUE WS_KBD4 50						
TRUE PCIE_EXCARD_R2D_P 32 89 95				TRUE WS_KBD5 50						
TRUE PCIE_EXCARD_D2R_P 17 32 89				TRUE WS_KBD6 50						
TRUE PCIE_EXCARD_D2R_N 17 32 89				TRUE WS_KBD7 50						
TRUE PP3V3_S3_EXCARD_SWITCH 32				TRUE WS_KBD8 50						
TRUE PP3V3_S0_EXCARD_SWITCH 32				TRUE WS_KBD9 50						
TRUE PP1V5_S0_EXCARD_SWITCH 32				TRUE WS_KBD10 50						
TRUE PLT_RESET_SWITCH_L 32				TRUE WS_KBD11 50						
TRUE EXCARD_CPPE_L 32				TRUE WS_KBD12 50						
TRUE EXCARD_CPUSB_L 32				TRUE WS_KBD13 50						
TRUE EXCARD_CLKREO_CONN_L 32				TRUE WS_KBD14 50						
TRUE SMBUS_MCP_0_CLK 13 21 45 90				TRUE WS_KBD15_CAP 50						
TRUE SMBUS_MCP_0_DATA 13 21 45 90				TRUE WS_KBD16_NUM 50						
				TRUE WS_KBD17 50						
				TRUE WS_KBD18 50						
				TRUE WS_KBD19 50						
				TRUE WS_KBD20 50						
				TRUE WS_KBD21 50						
				TRUE WS_KBD22 50						
				TRUE WS_KBD23 50						
				TRUE WS_KBD_ONOFF_L 50						
				TRUE WS_LEFT_SHIFT_KBD 50						
				TRUE WS_LEFT_OPTION_KBD 50						
				TRUE WS_CONTROL_KBD 50						
				TRUE KBDLED_ANODE 51						
				TRUE TPAD_GND_F 7 51						
A	POWER RAILS									
	TRUE PM_SLP_S3_L 21 34 37 42 44 68 81 83									
	TRUE PPBUS_G3H 8 46									
	TRUE PPBUS_CPU_IMVP_ISNS 8									
	TRUE PP3V42_G3H 7 8 43									
TRUE PP5V_S3 8										
TRUE PP5V_S0 8										
TRUE PPVCORE_S0_CPU 8										
TRUE PPVCORE_S0_MCP_REG 8										
TRUE PPVCORE_S0_MCP 8										
TRUE PP3V3_S5 8 95										
TRUE PP3V3_S3 8										
TRUE PP3V3_S0 8 95										
TRUE PP2V5_S0 8										
TRUE PP1V2_S0 8										
TRUE PP1V8_S0 8										
TRUE PP1V8R1V5_S3 8										
TRUE PP1V8R1V5_S0_FET 8										
TRUE PPMCPDDR_ISNS 8										
TRUE PP1V05_S0_REG 8										
TRUE PP1V2R1V05_S5 8										
TRUE PPCPUVTT_S0 8										
TRUE PPCPUFSB_ISNS_R 8										
TRUE PP0V9R0V75_S0_DDRVTT 8										
TRUE PP1V2R1V05_ENET 8										
TRUE PP3V3_ENET_PHY 8										
TRUE PPVP_FW 8										
TRUE PP1V0_FW 8										
TRUE PP3V3_S0GPU 8										
TRUE PP1V1_S0GPU_REG 8										
TRUE PP1V8_S0GPU_ISNS 8										
TRUE PPVCORE_GPU 8										
TRUE PP1V8_S0GPU_ISNS_R 8										
TRUE PP3V3_S5_AVREF_SMC 42 43										
TRUE PPVOUT_S0_LCDBKLT 79 84										
TRUE PPDCIN_G3H 8										
TRUE PPVTDDR_S3 8										
TRUE PP1V8_GPUIFPX 8										

Functional / ICT Test

SYNC_MASTER=N/A

SYNC_DATE=N/A

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D

051-7902

D

SCALE

NONE

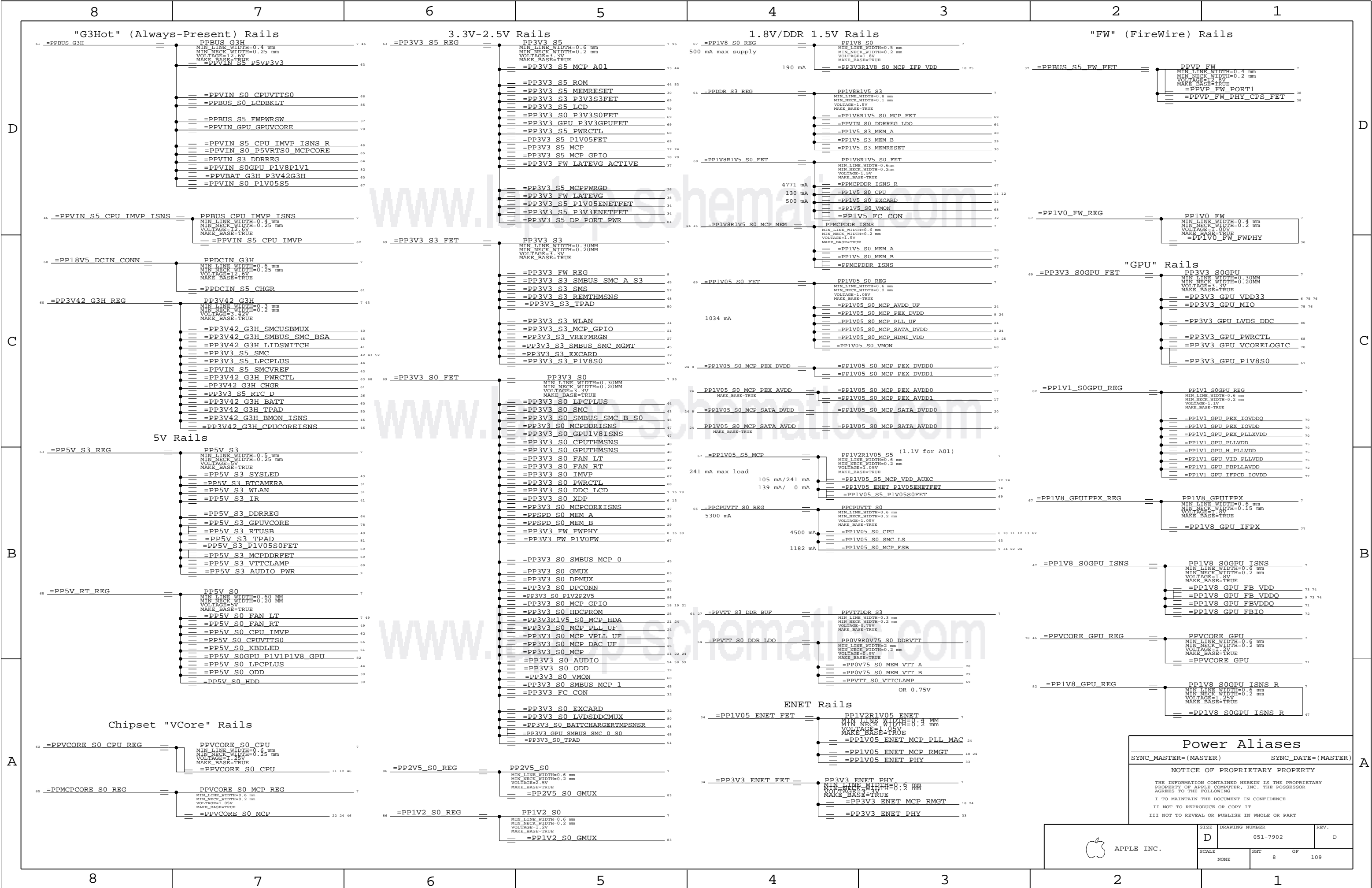
SHT

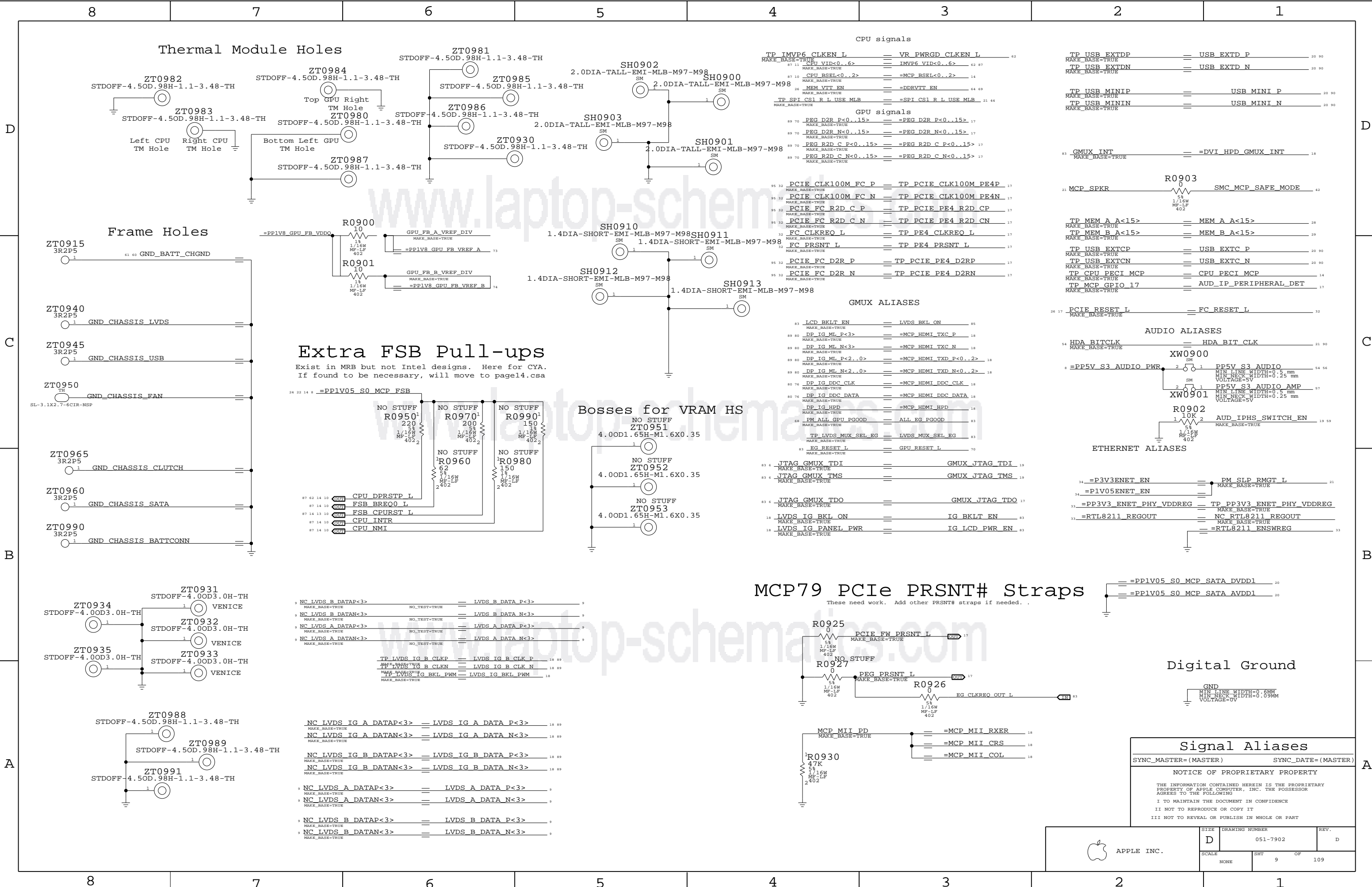
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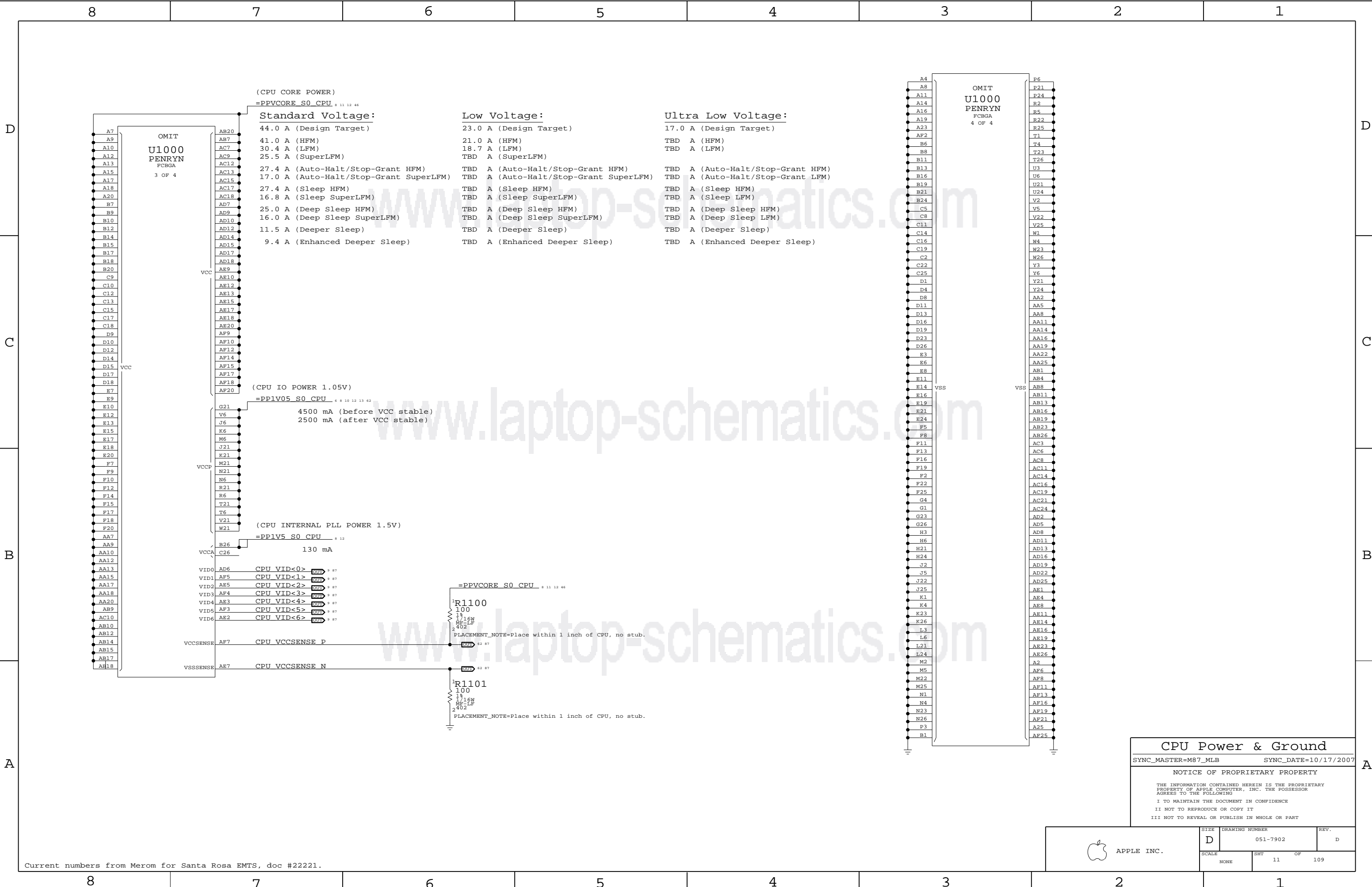
OF

109

8	7	6	5	4	3	2	1
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CPU Power & Ground

SYNC_MASTER=M87_MLB

SYNC_DATE=10/17/2007


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SIZE

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DRAWING NUMBER

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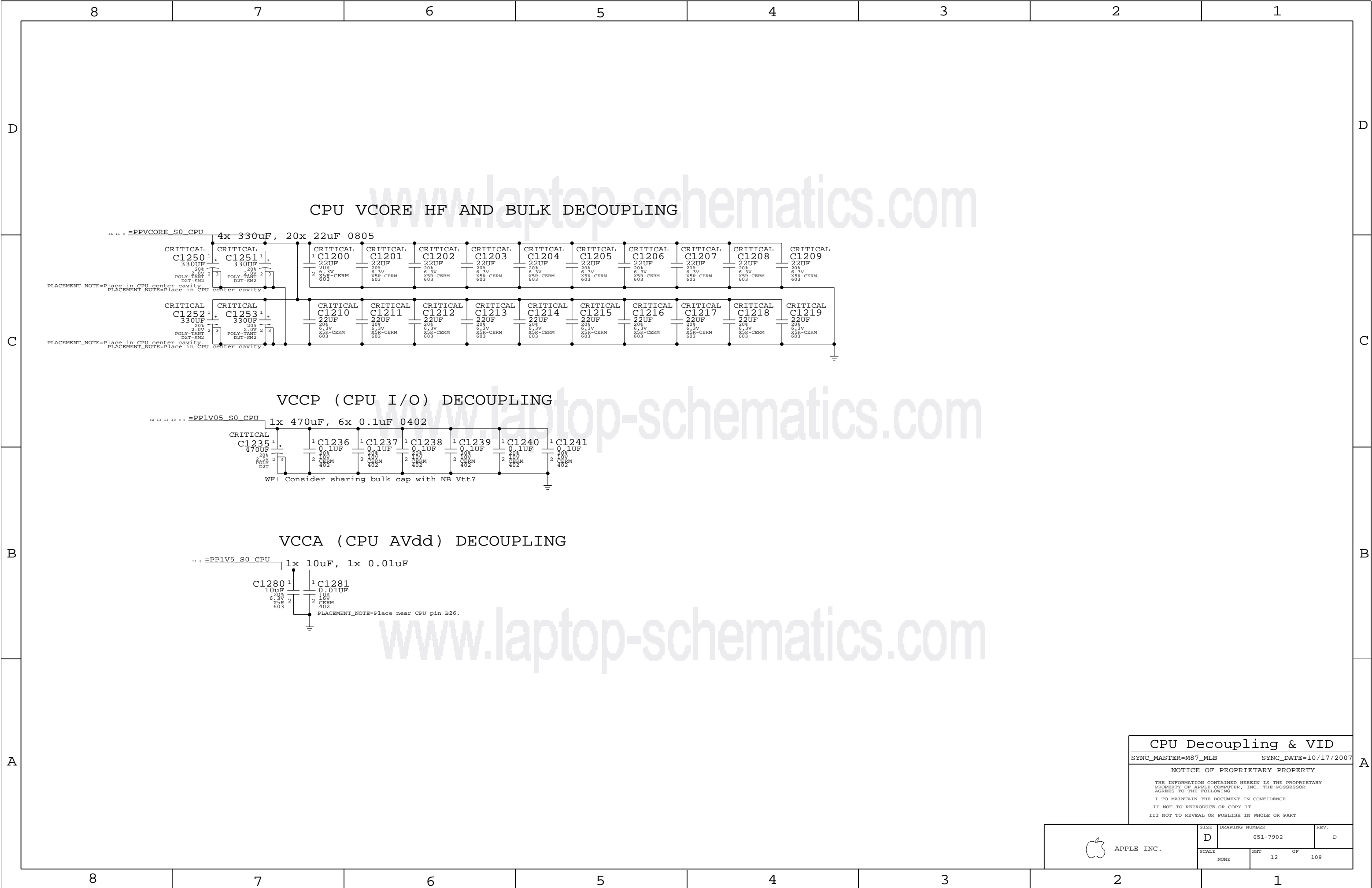
NONE

SHT

11

OF

109



CPU Decoupling & VID

SYNC_MASTER=M87_MLB

SYNC_DATE=10/17/2007


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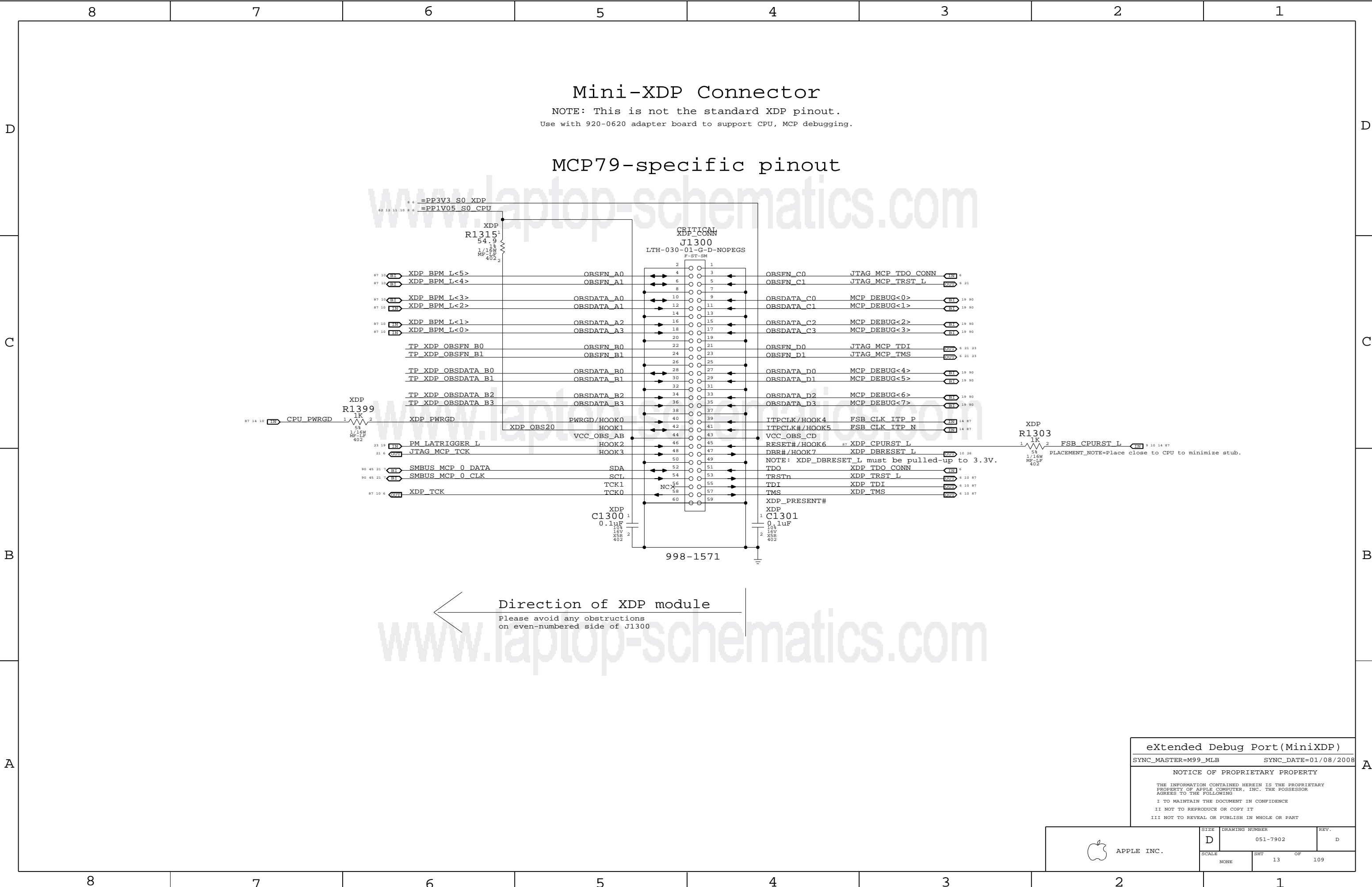
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	D	051-7902	D
SCALE	SHT	OF	REV.
NONE	12	109	



eXtended Debug Port (MiniXDP)

SYNC_MASTER=M99_MLB SYNC_DATE=01/08/2008

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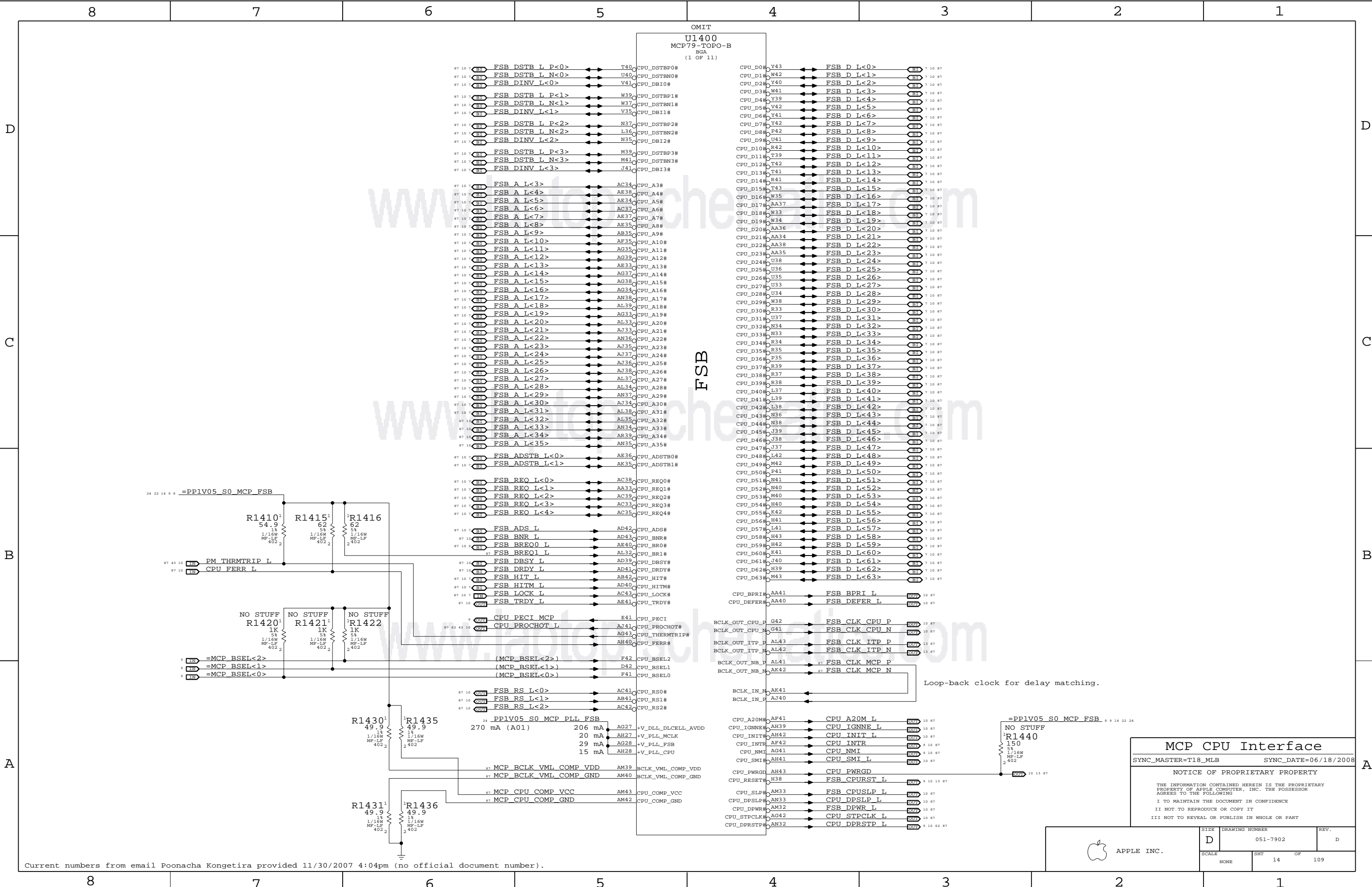
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	SCALE NONE	SHT 13	OF 109



MCP CPU Interface

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

NOTICE OF PROPRIETARY PROPERTY

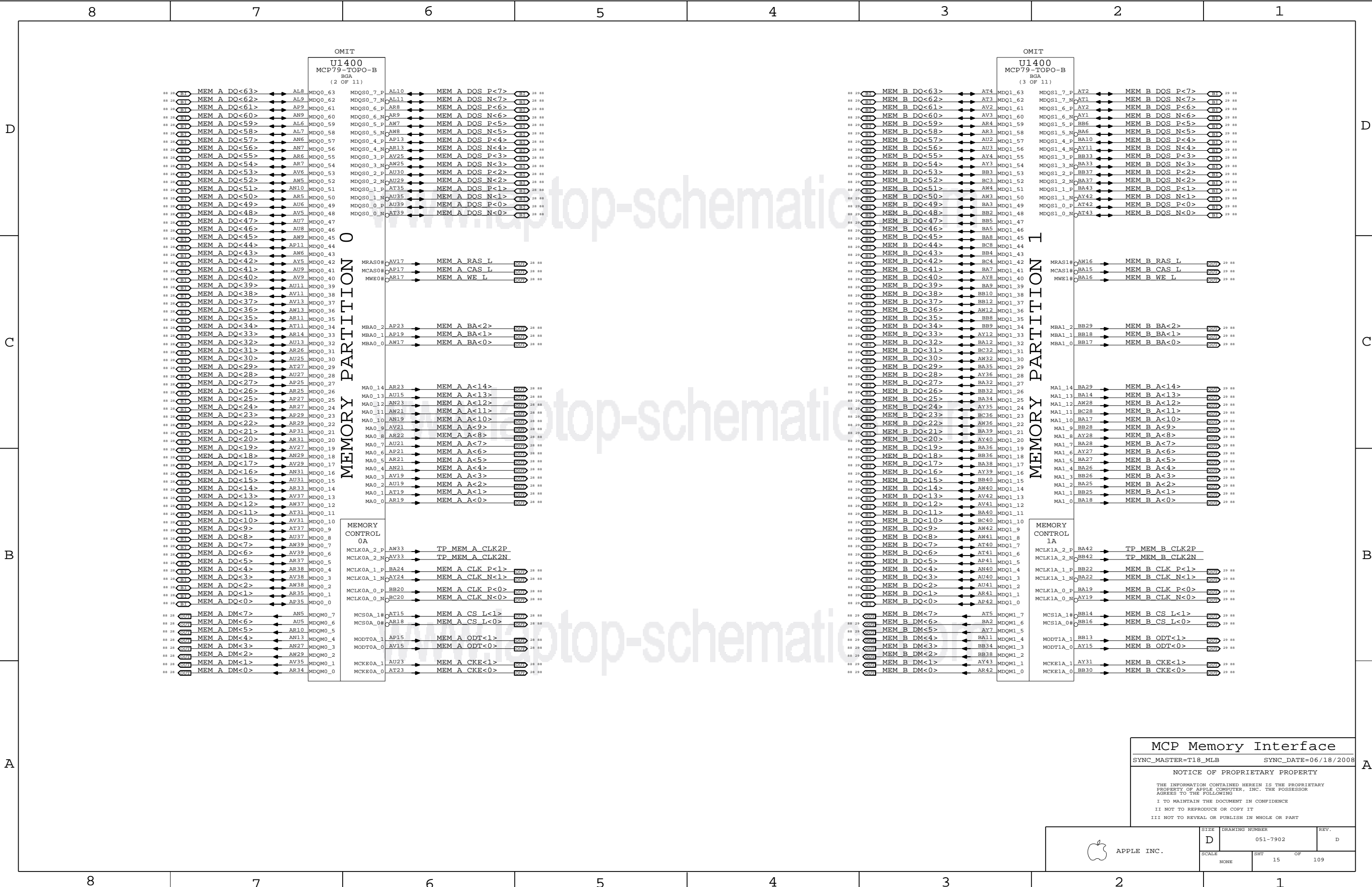
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NONE		14	109



MCP Memory Interface

SYNC_MASTER=T18_MLB

SYNC_DATE=06/18/2008

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DRAWING NUMBER

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SCALE

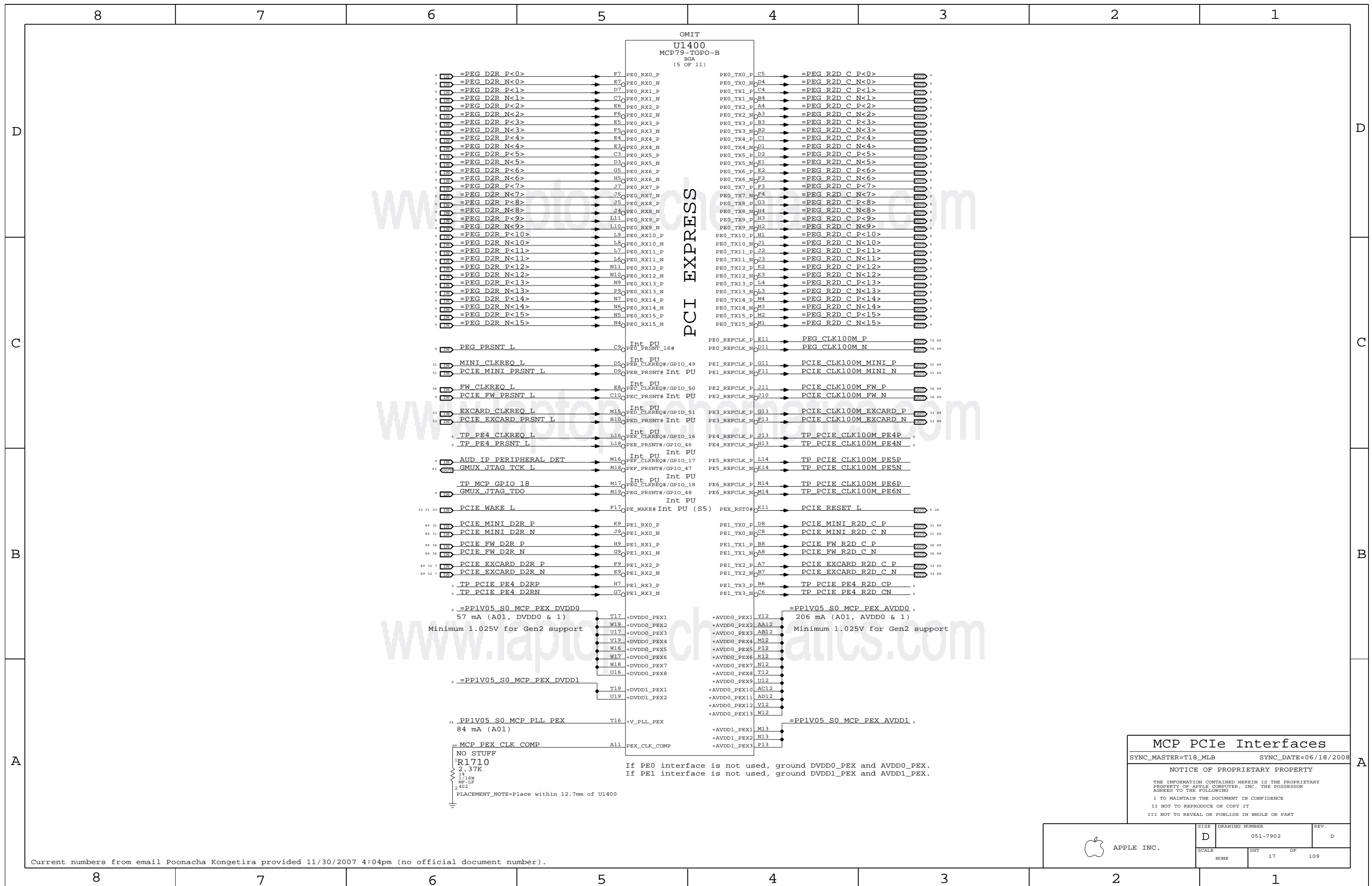
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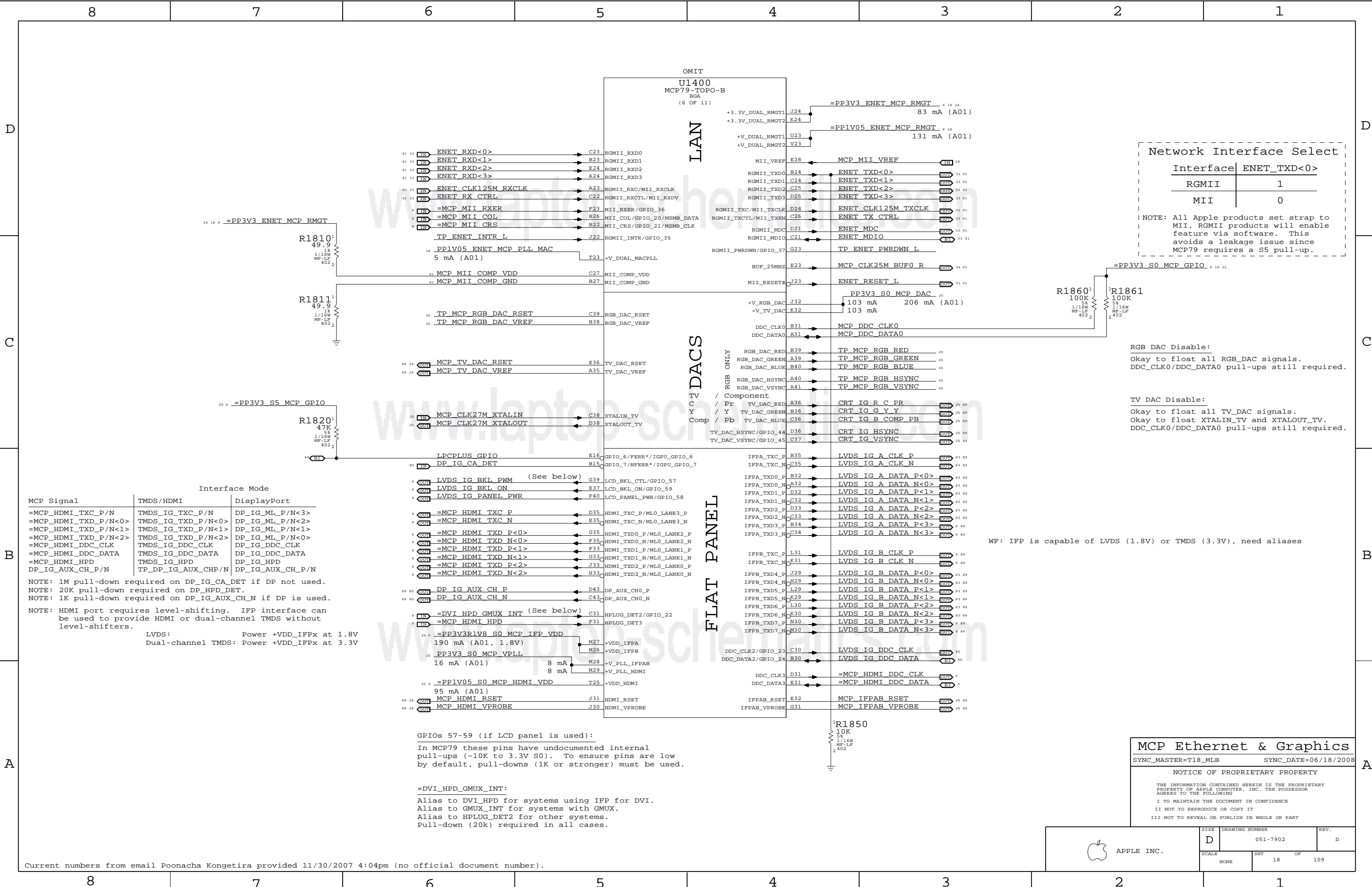
SHT

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Interface Mode		
MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CH_P/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.
NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

GPIOs 57-59 (if LCD panel is used):

In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:

Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.

Network Interface Select	
Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

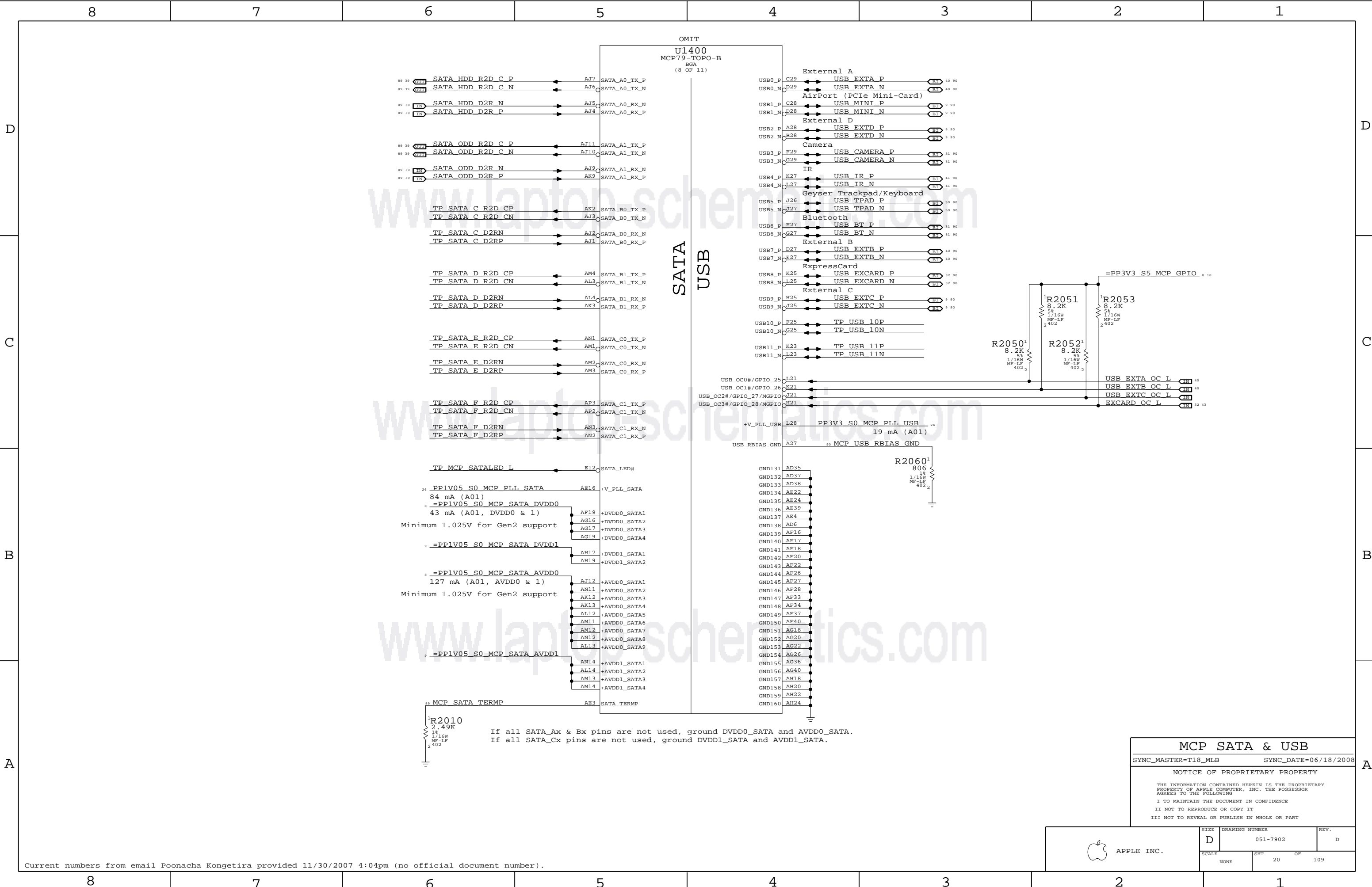
RGB DAC Disable:
Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:
Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

MCP Ethernet & Graphics		
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MCP SATA & USB

SYNC_MASTER=T18_MLB

SYNC_DATE=06/18/2008

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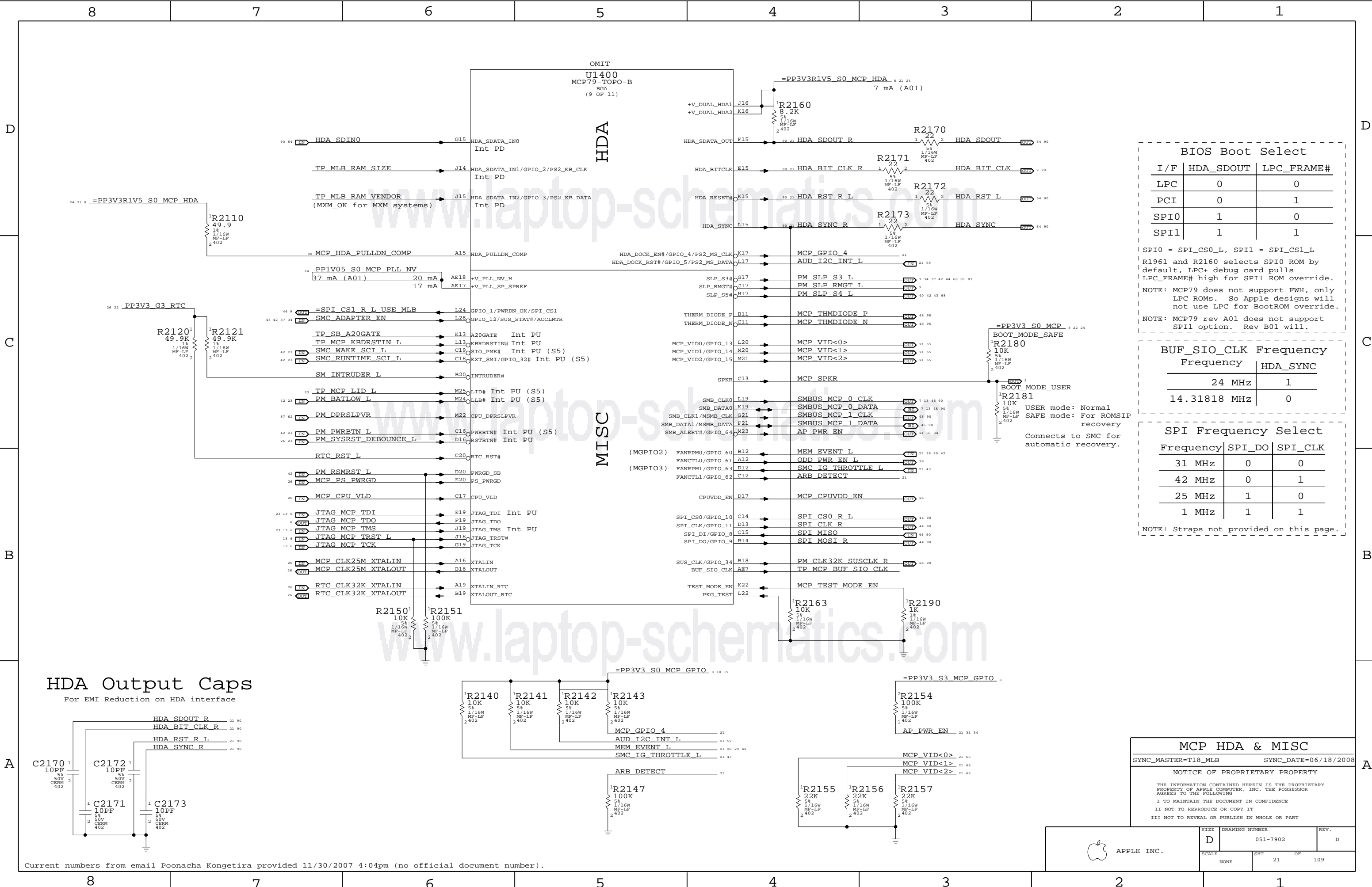
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SCALE		SHT	OF
NONE		20	109



BIOS Boot Select		
I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L
R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.
NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.
NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

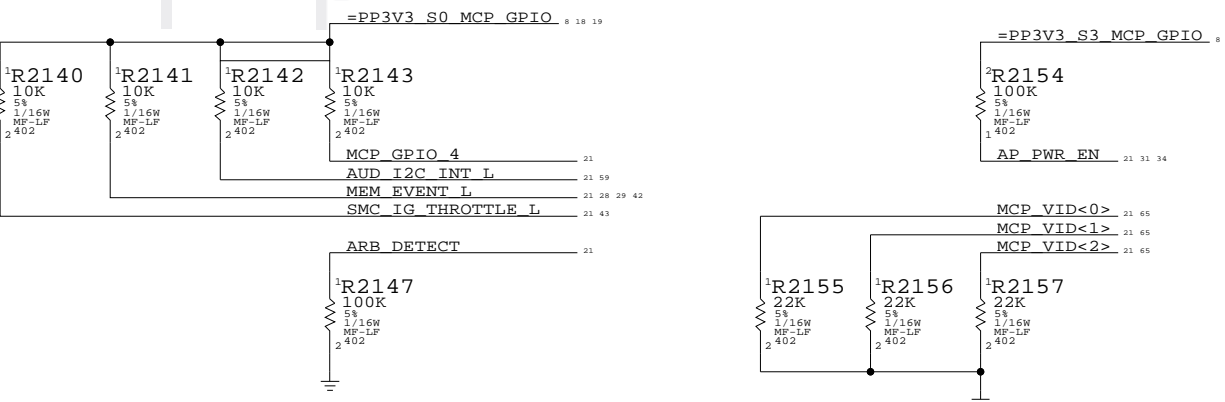
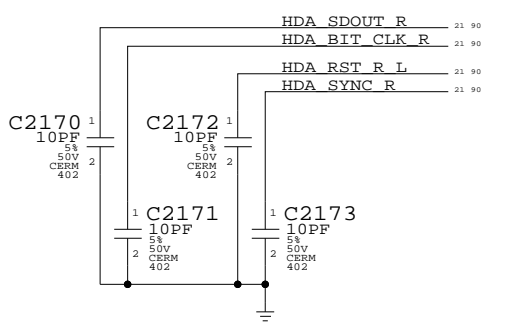
BUF_SIO_CLK Frequency	
Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select		
Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

HDA Output Caps

For EMI Reduction on HDA interface



MCP HDA & MISC

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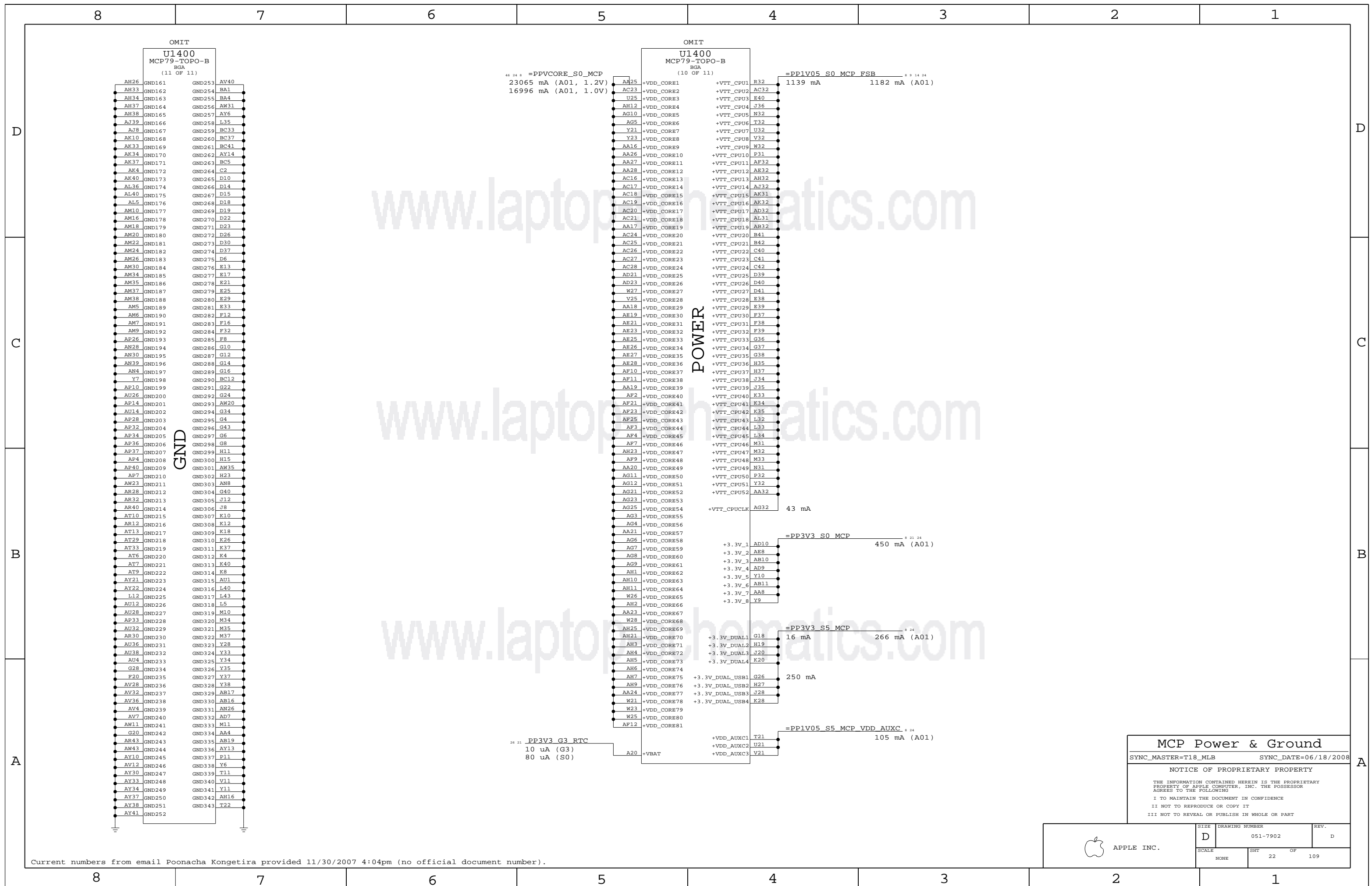
SIZE	DRAWING NUMBER	REV.
D	051-7902	D
SCALE	SHT	OF
NONE	21	109



APPLE INC.

SCALE	SHT	OF
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MCP79 A01 Silicon Support

SYNC_MASTER=T18_MLB SYNC_DATE=03/31/2008

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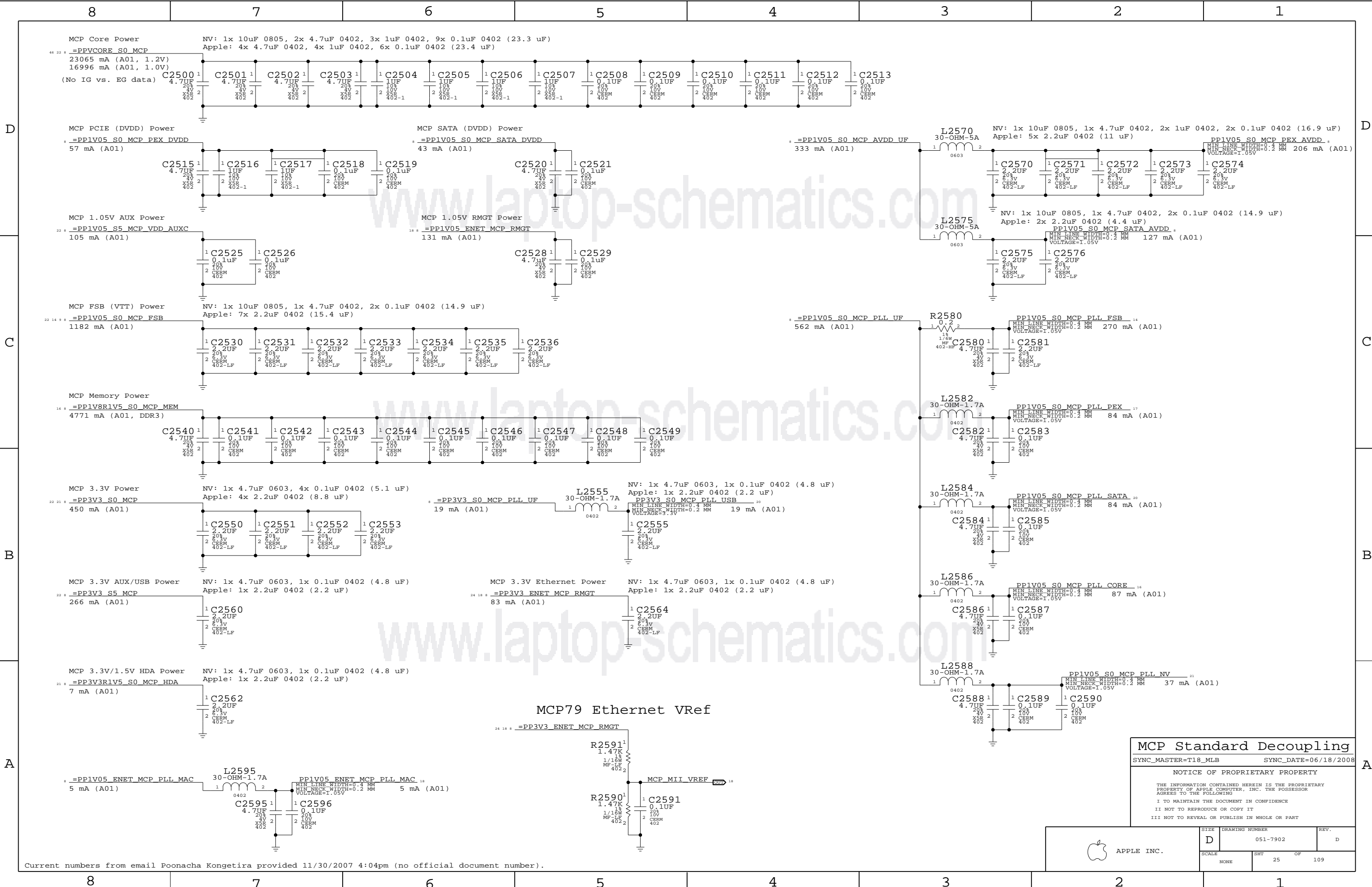
NONE

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OF

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MCP Standard Decoupling

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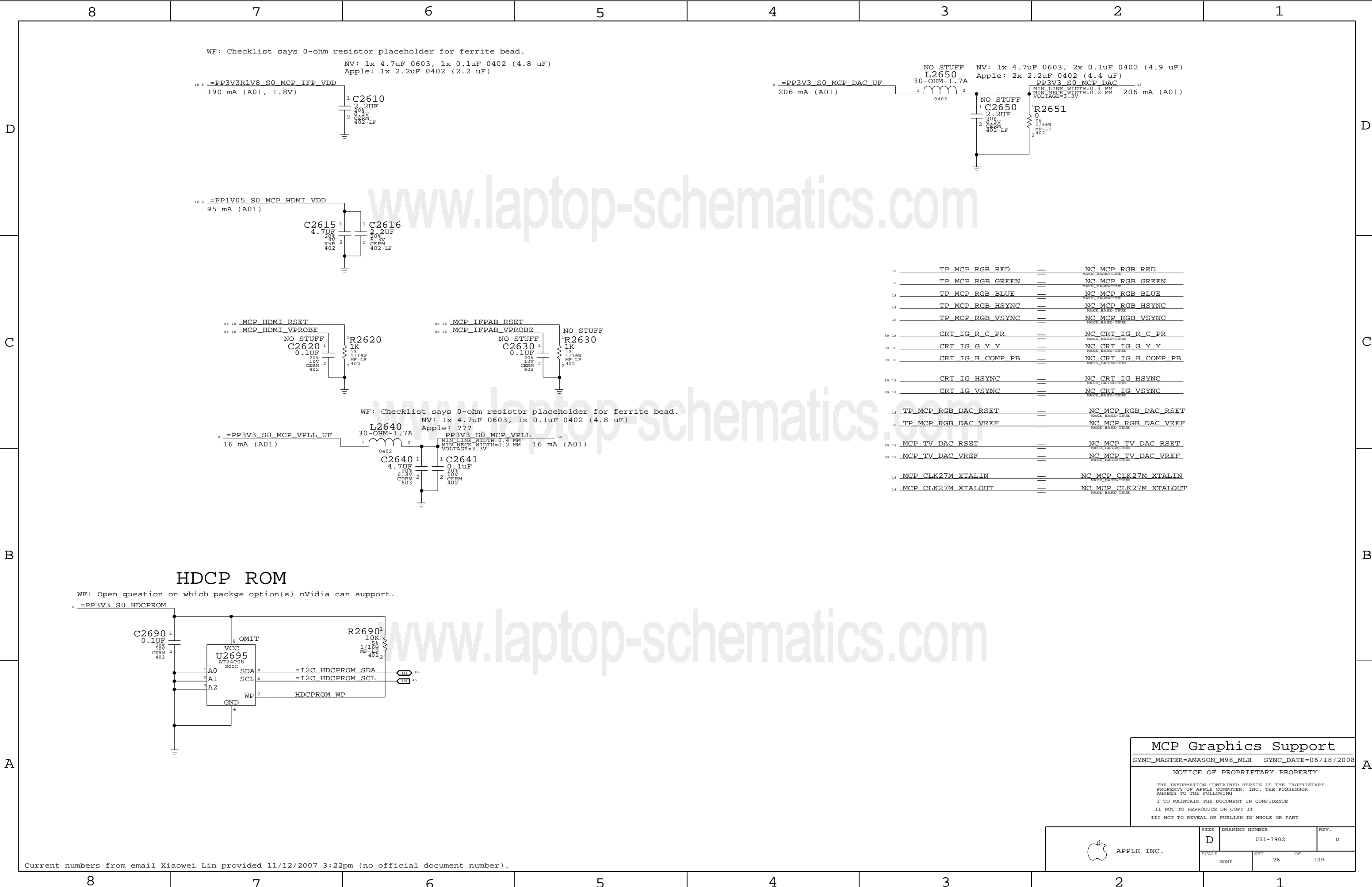
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SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF
NONE	25	109



RTC CLK32K XTALOUT

NO STUFF

R2811¹
10M
9%
1/16W
MF-LF
402₂

R2810
0
1/16W
MF-LF
402

RTC CLK32K XTALOUT R

CRITICAL
Y2810
32.768K
7X1.5X1.4-SM

C2810
12pF
1
2
5%
50V
CERM
402

RTC CLK32K XTALIN

C2811
12pF
1
2
5%
50V
CERM
402

MCP 25MHz Crystal

MCP_CLK25M_XTALOUT

NO STUFF

R2816

1M

5%

1/16W

MF-LP

402

R2815

5%

1/16W

MF-LP

402

MCP_CLK25M_XTALOUT_R

CRITICAL

Y2815

25.0000M

SM-3.2X2.5MM

C2815

12pF

5%

50V

CERM

402

MCP_CLK25M_XTALIN

[illegible]

Reset Button

Reset Button

40 **PM_SYSRST_L**

XDP

R2896 10K pull-up to 3.3V S0 inside MCP

1 0 2

10 **XDP_DBRESET_L**

1 5 2

1/16W MF-LF 402

OMIT

R2897 1 0 2

1/16W MF-LF 402

33 2

R2899 10K pull-up to 3.3V S0 inside MCP

1 2

NO STUFF

C2899 1 2

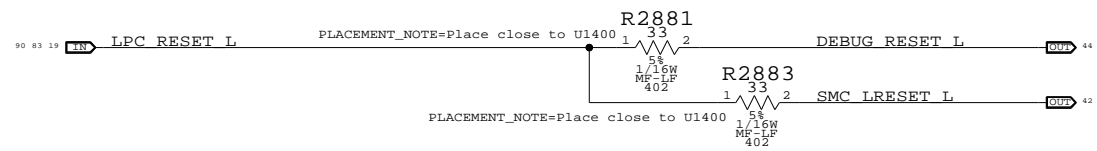
100µF

10V XSR 402

21 23

SILK_PART=FP SYS RESET

LPC Reset (Unbuffered)



PCB layout showing signal traces and component footprints for various reset and clock signals. The layout includes components like R2890, R2891, R2893, R2894, R2895, R2870, R2825, R2826, R2827, and R2829, all with 1/16W MF-LP 402 footprints. Signal traces are labeled with names like PCIE RESET L, FW RESET L, GMUX PCIE RESET L, MAKE_BASE=TRUE, PCA9557D RESET L, BKLIT PLT RST L, MINI RESET L, EXCARD RESET L, MEM VTT EN R, LPC_CLK33M_SMC R, LPC_CLK33M_SMC, LPC_CLK33M LPCPLUS, LPC_CLK33M GMUX, and PM CLK32K_SUSCLK R. The layout also shows placement notes like "Place close to U1400".

45 PM_SYSRST_L

XDP

R2896

1 0 2

5% 1/16W MF-LF 402

OMIT R2897

1 0 2

5% 1/16W MF-LF 402

SILK_PART=FP SYS RESET

10K pull-up to 3.3V S0 inside MCP

R2899

1 3 2

5% 1/16W MF-LF 402

PM_SYSRST_DEBOUNCE_L

NO STUFF

C2899

1 2

100nF 100V X50 402

21 23

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Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

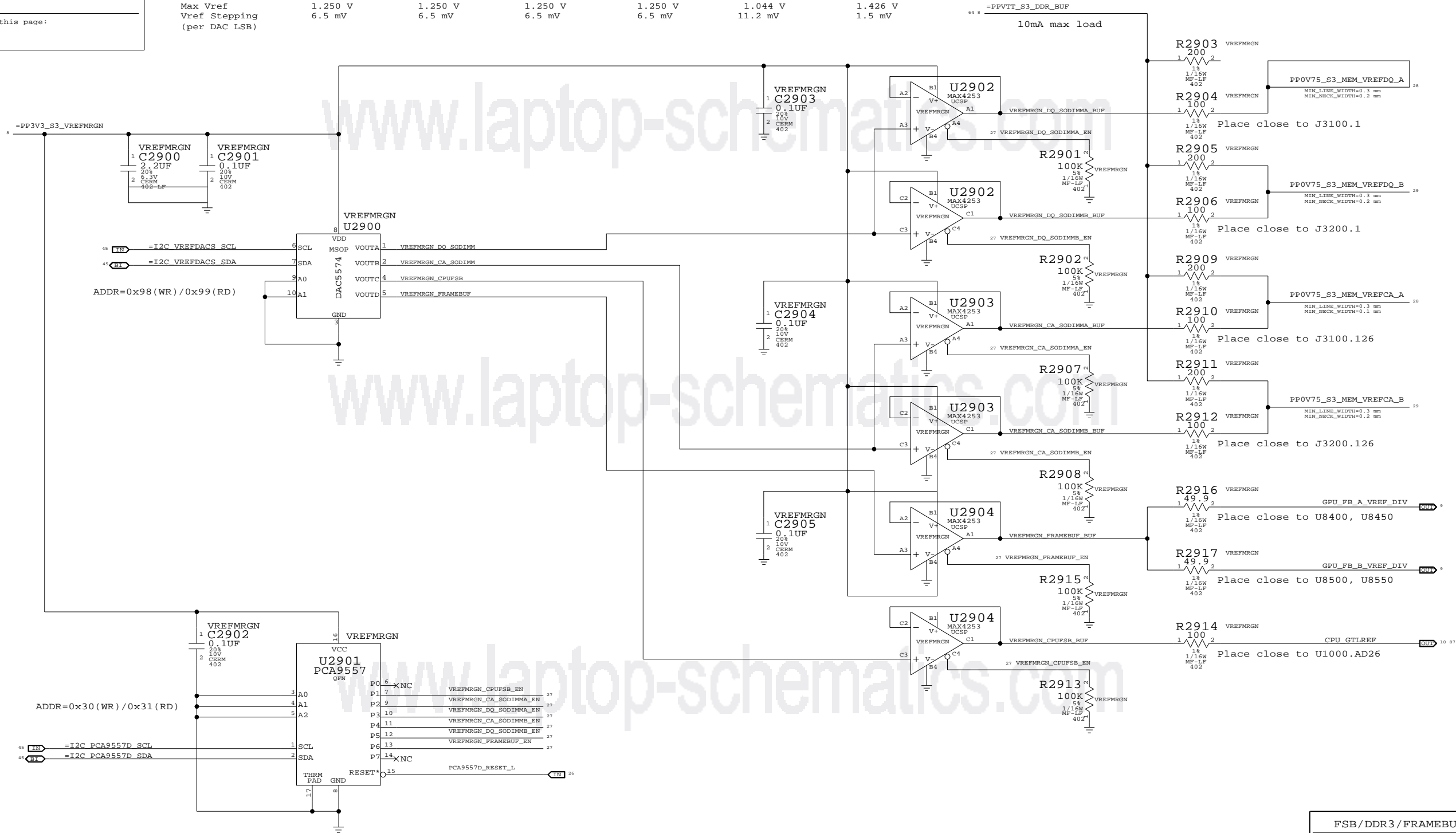
Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
NO_VREFMRGN

DAC channel
Min DAC code
Max DAC code
Max sink I
Max source I
Nominal Vref
Min Vref
Max Vref
Vref Stepping
(per DAC LSB)

MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF	FRAME BUFFER VREF
A	B	A	B	C	D
0x00	0x00	0x00	0x00	0x00	0x00
0x87	0x87	0x87	0x87	0x55	0xFF
-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA	-59.04 mA
5 mA	5 mA	5 mA	5 mA	0.52 mA	51.15 mA
0.75 V	0.75 V	0.75 V	0.75 V	0.70 V	1.248 V
0.375 V	0.375 V	0.375 V	0.375 V	0.091 V	1.042 V
1.250 V	1.250 V	1.250 V	1.250 V	1.044 V	1.426 V
6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV	1.5 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately (i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

FSB/DDR3/FRAMEBUF Vref Margining

SYNC_MASTER=DDR SYNC_DATE=07/22/2008

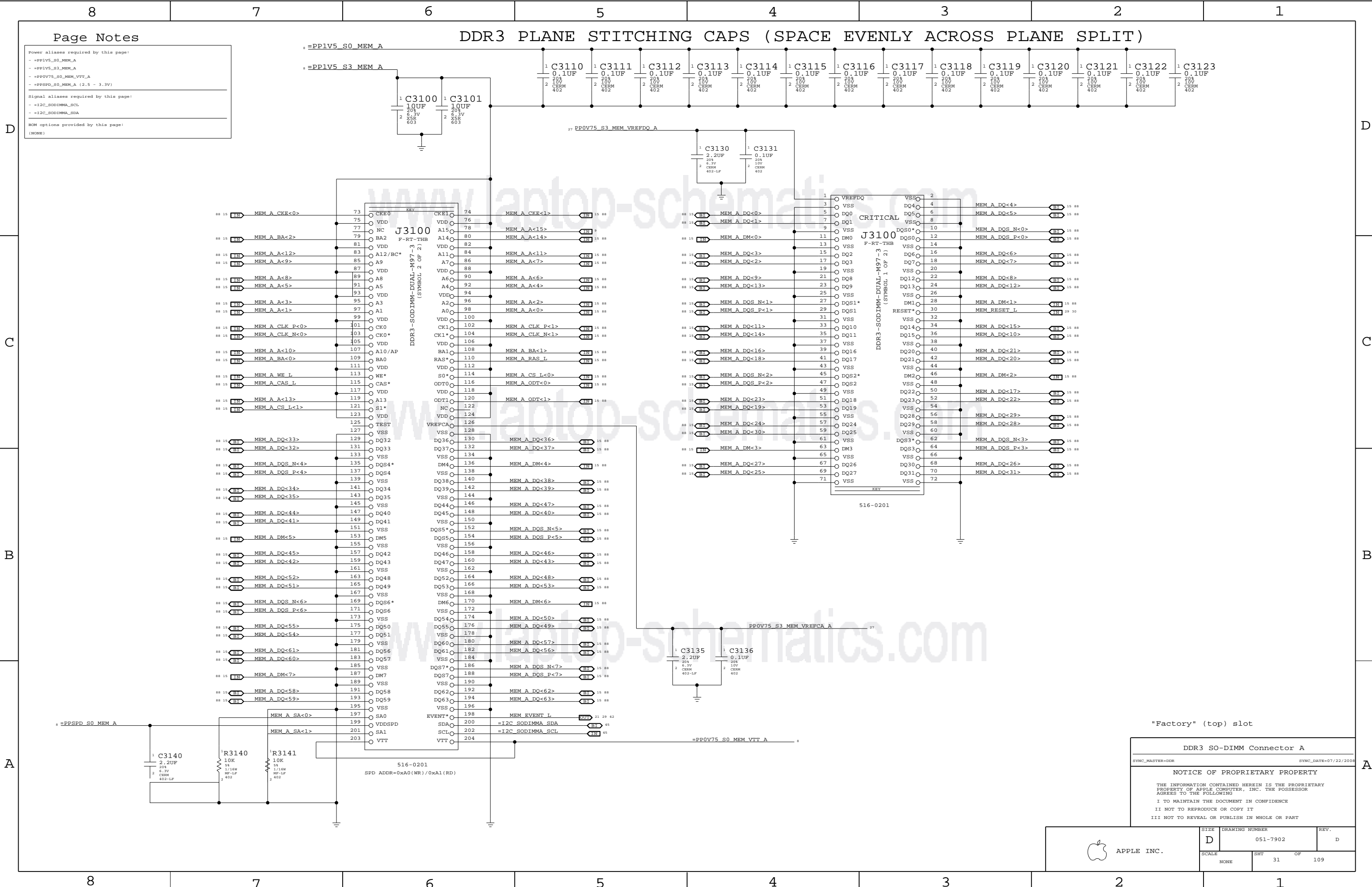
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Page Notes

Power aliases required by this page:

- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:

(NONE)

DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)

"Factory" (top) slot

DDR3 SO-DIMM Connector A

SYNC_MASTER=DDR SYNC_DATE=07/22/2008

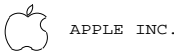
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SIZE D DRAWING NUMBER 051-7902 REV. D

SCALE NONE SHT 31 OF 109

DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)

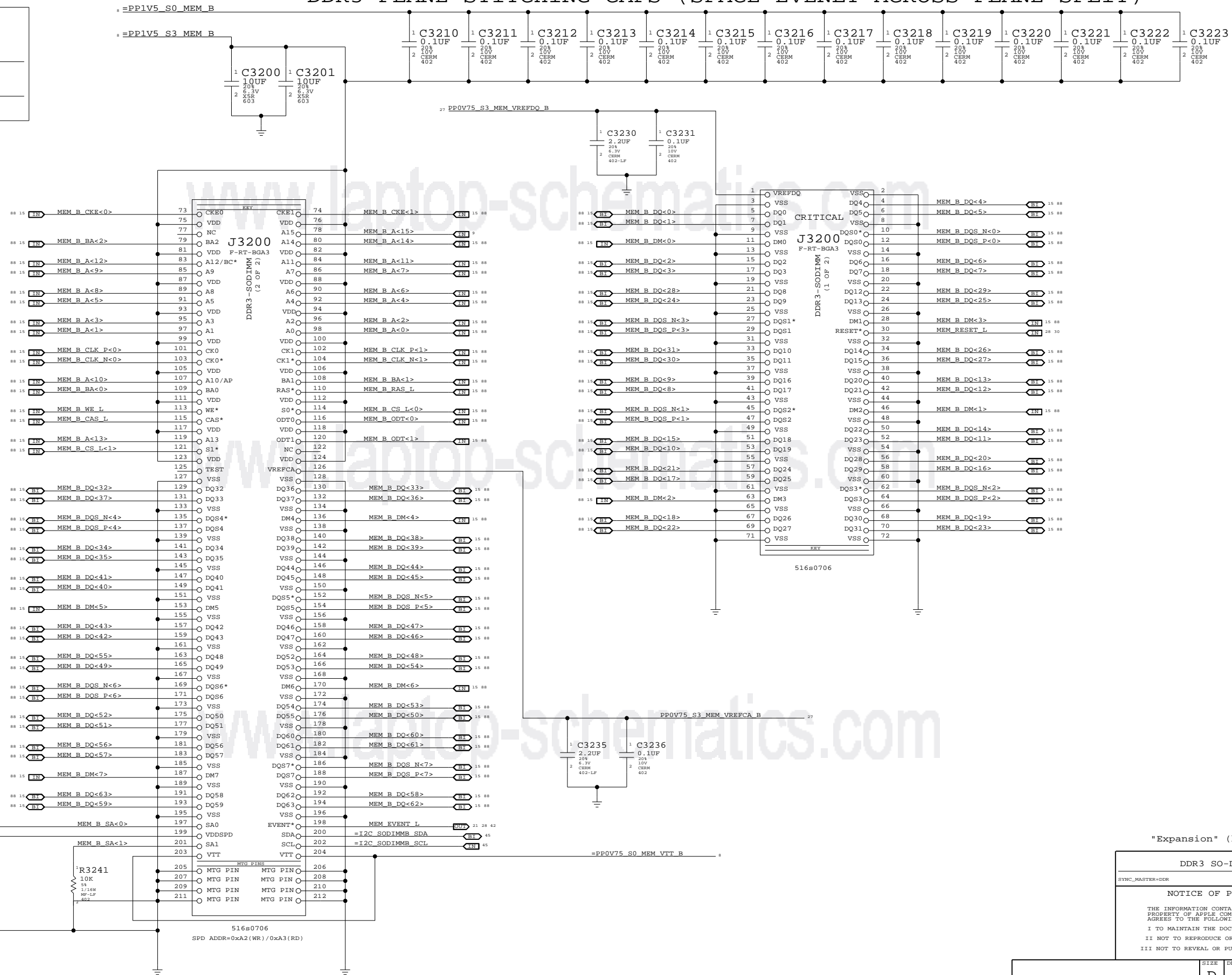
Power aliases required by this page:

```
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)
```

Signal aliases required by this page:

```
- #I2C_SODIMMB_SCL
- #I2C_SODIMMB_SDA
```

BOM options provided by this page
(NONE)



"Expansion" (bottom) slot

DDR3 SO-DIMM Connector B

SYNC_MASTER=DDR	SYNC_DATE=07/22/2008
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SIZE	DRAWING NUMBER	REV.
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D	051-7902	D
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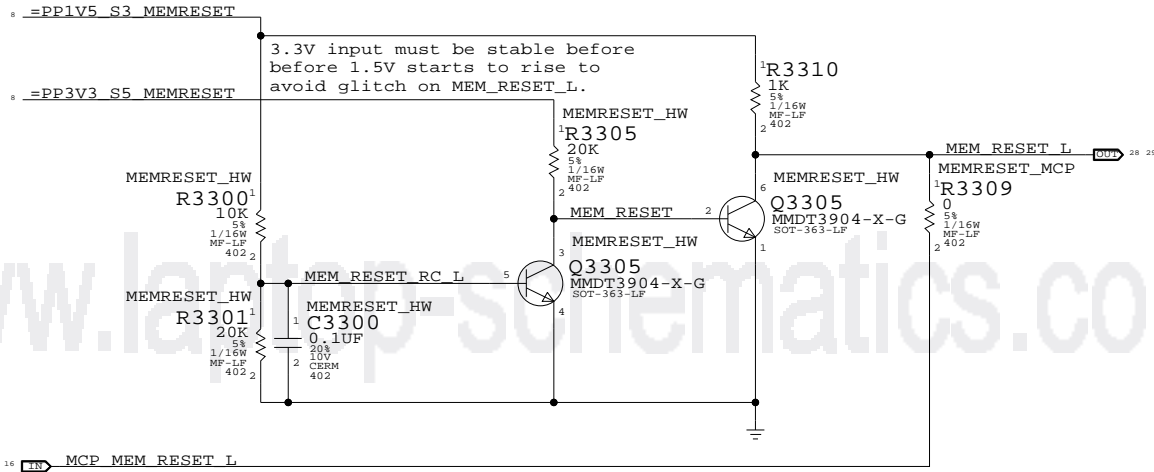
D		
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SCALE	SHT	OF
	32	109

www.laptop-schematics.com

DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



www.laptop-schematics.com

DDR3 Support

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

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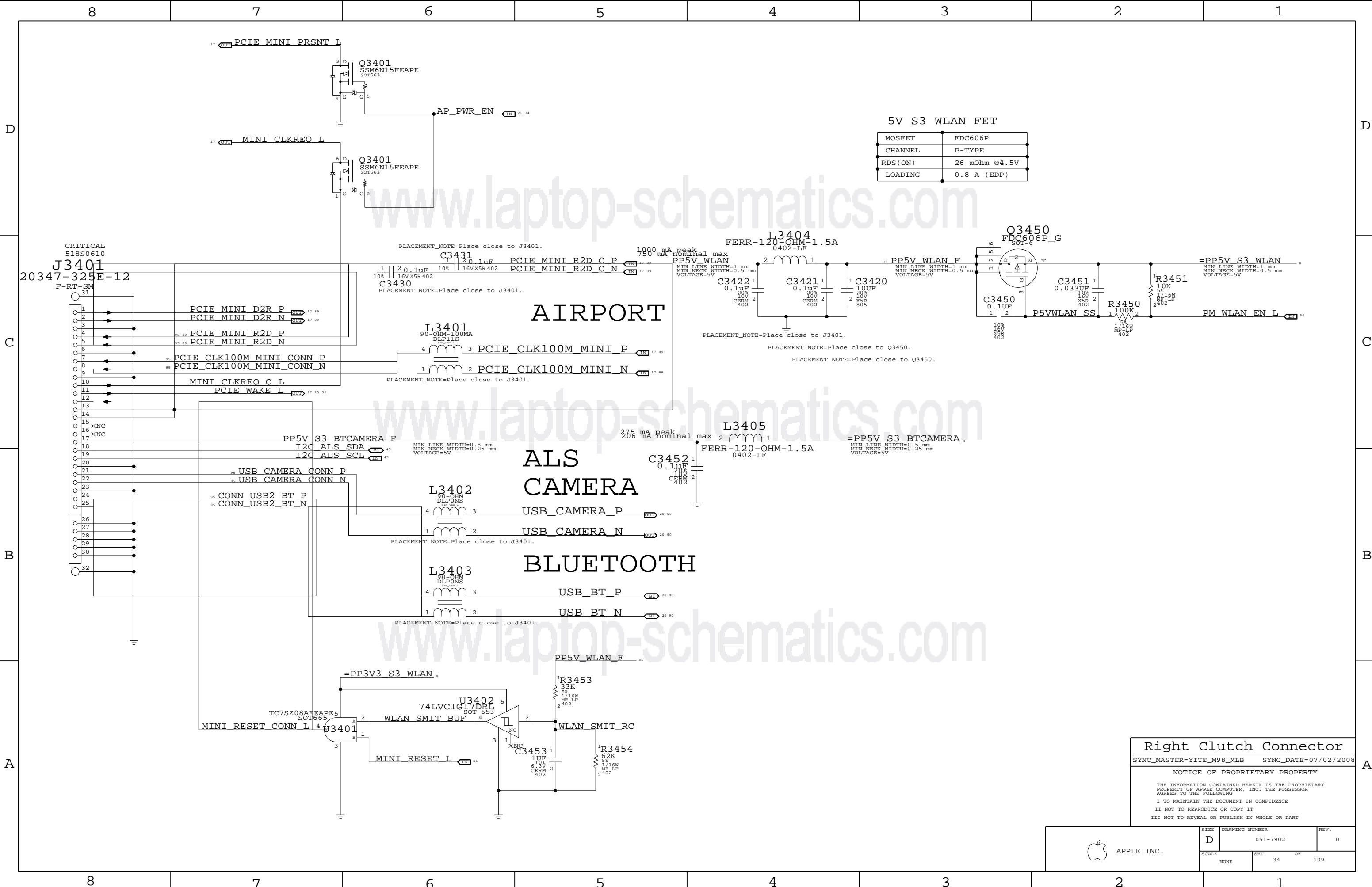
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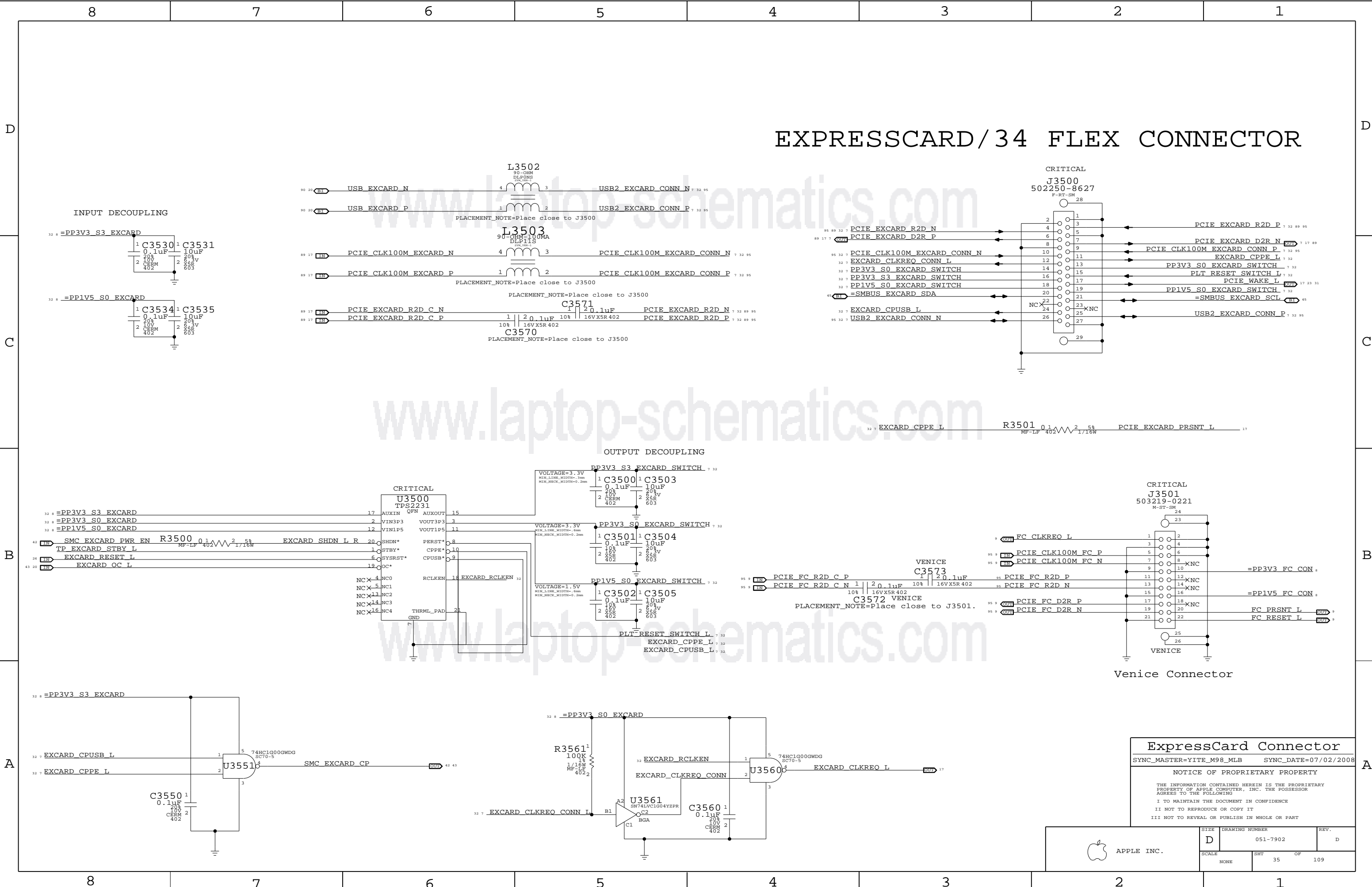
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	D	051-7902	D
SCALE		SHT	OF
NONE		33	109





EXPRESSCARD/34 FLEX CONNECTOR

ExpressCard Connector

SYNC_MASTER=YITE_M98_MLB SYNC_DATE=07/02/2008

NOTICE OF PROPRIETARY PROPERTY

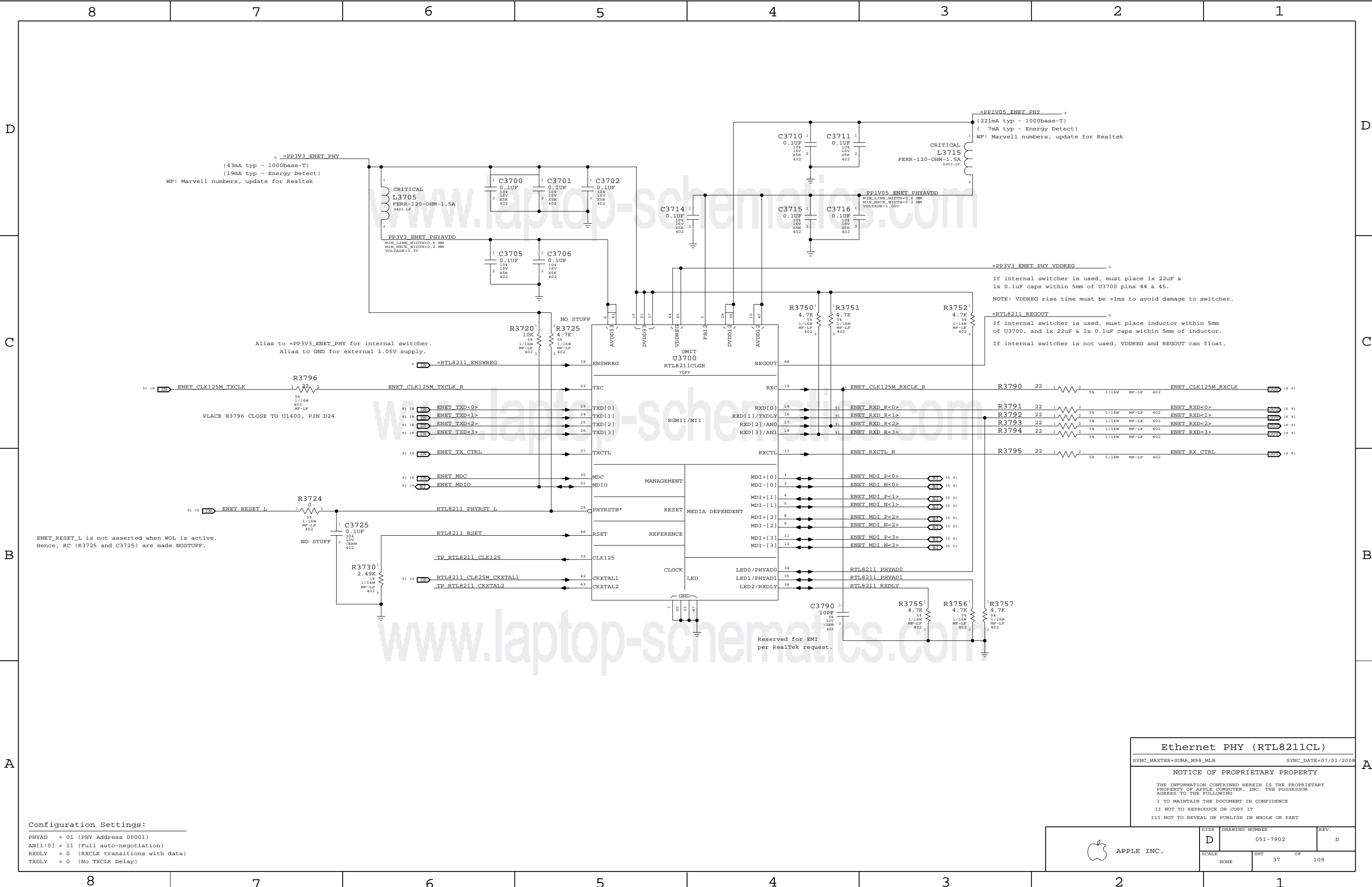
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	D	051-7902	D
SCALE		SHT	OF
NONE		35	109



Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

Ethernet PHY (RTL8211CL)

SYNC_MASTER=SUMA_M98_MLB SYNC_DATE=07/01/2008

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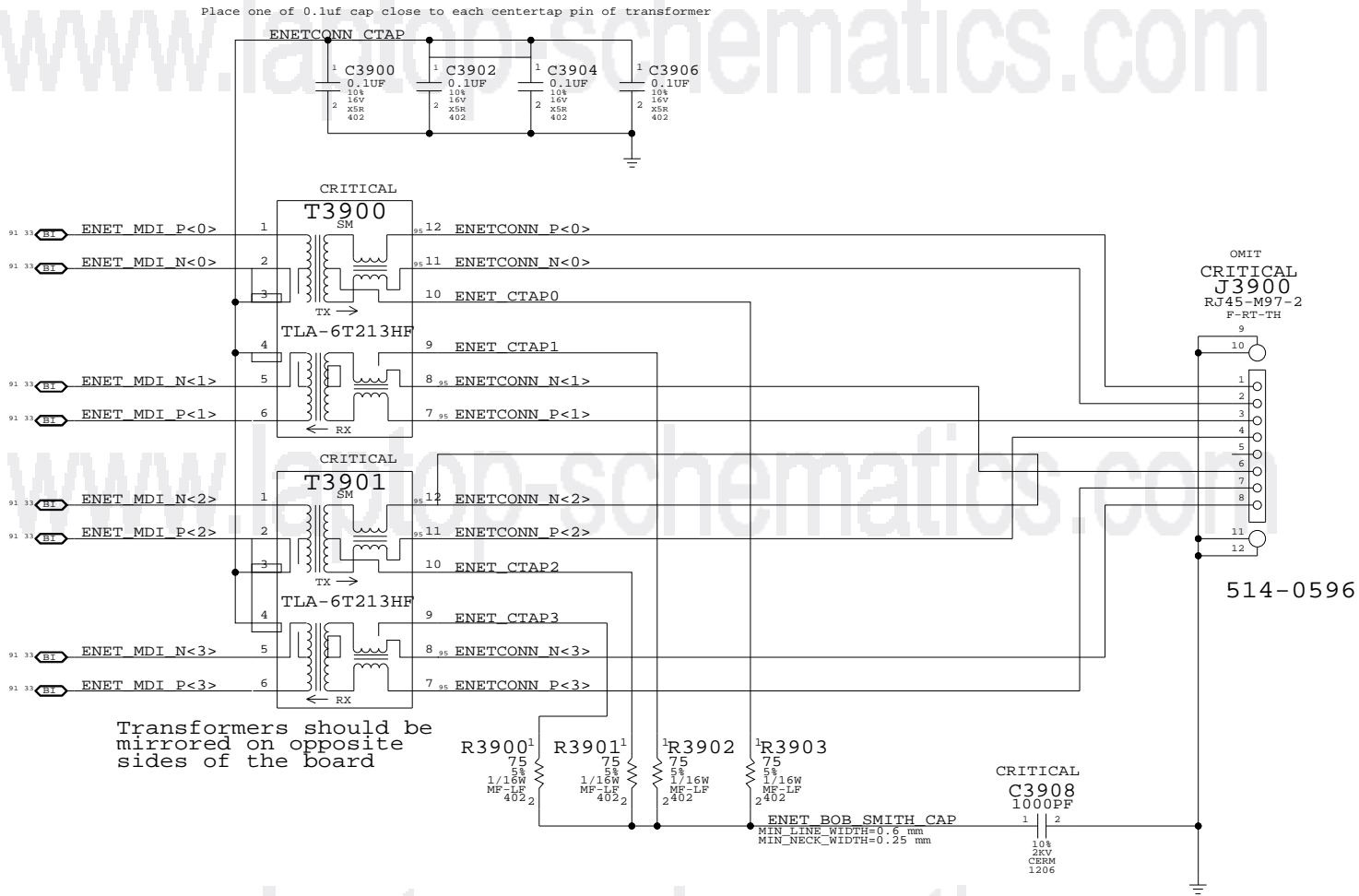
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7902	D
SCALE		SHT	OF
NONE		37	109

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Ethernet Connector

SYNC_MASTER=SUMA_M98_MLB SYNC_DATE=07/01/2008

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APPLE INC.

SIZE

D

DRAWING NUMBER

051-7902

REV.

D

SCALE

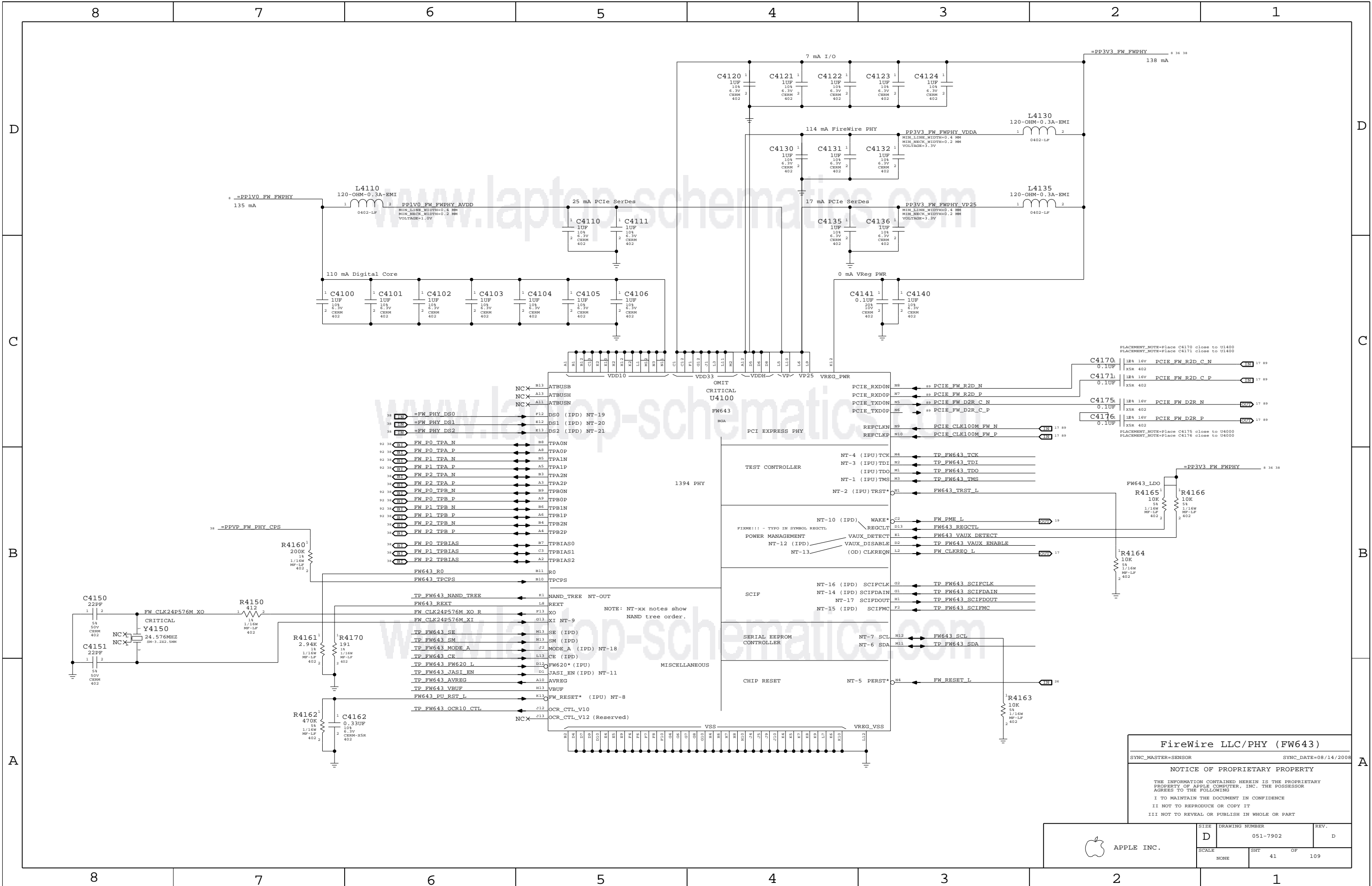
NONE

SHT

39

OF

109



FireWire LLC/PHY (FW643)

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

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Page Notes

Power aliases required by this page:

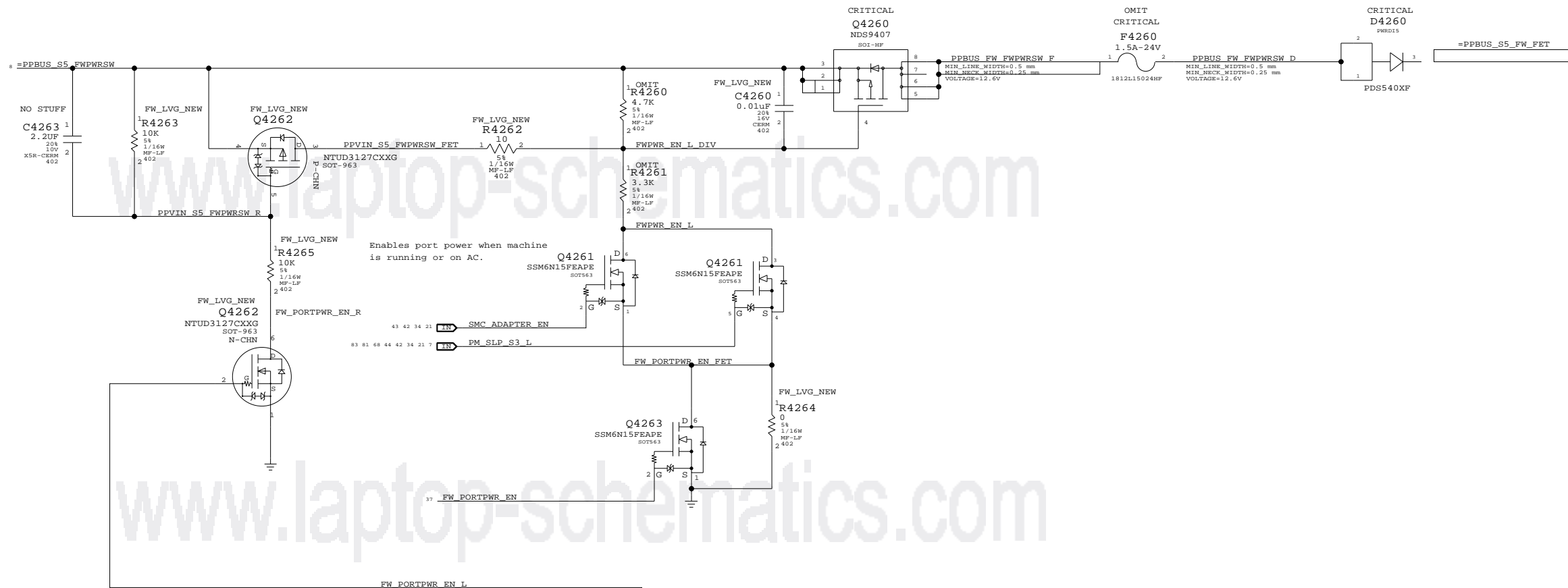
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

Signal aliases required by this page:
(NONE)

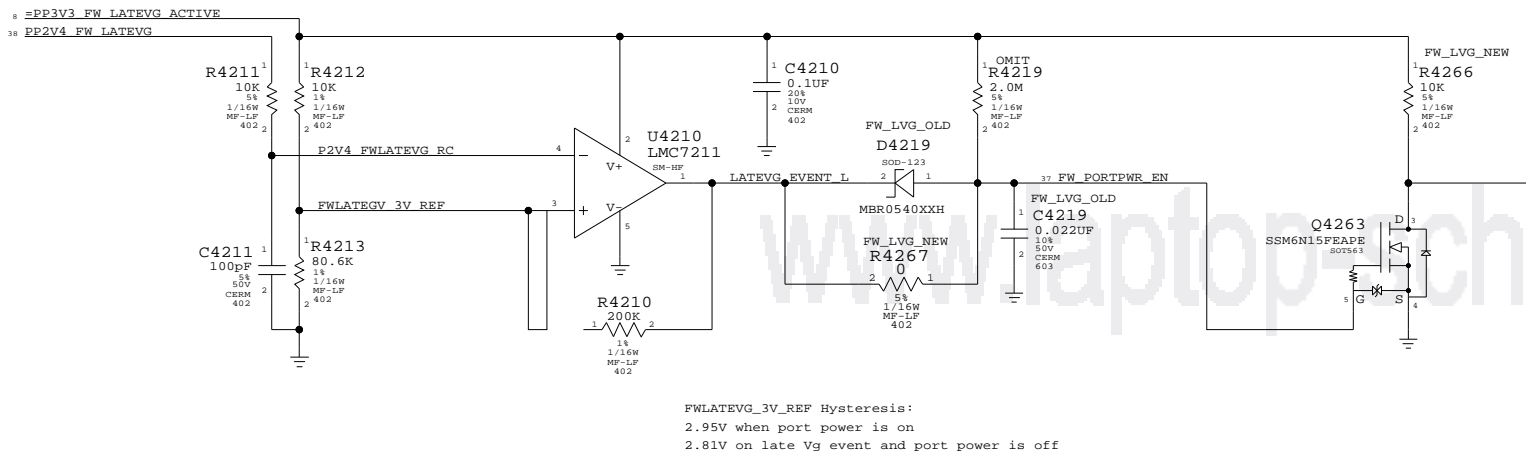
BOM options provided by this page:

- FW_PORT_FAULT_PU

FireWire Port Power Switch



Late-VG Event Detection



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
740S0080	1	LITTLEFUSE, 1.5A RESETTABLE 24V	F4260	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0145	1	RES,MTL FILM,2.0M,5%,0402,SM,LF	R4219		FW_LVG_OLD
116S0082	1	RES,MTL FILM,4.7K,5%,0402,SM,LF	R4260		FW_LVG_OLD
116S0078	1	RES,MTL FILM,3.3K,5%,0402,SM,LF	R4261		FW_LVG_OLD
116S0149	1	RES,MTL FILM,10K,5%,0402,SM,LF	R4219		FW_LVG_NEW
116S0130	1	RES,MTL FILM,470K,5%,0402,SM,LF	R4260		FW_LVG_NEW
116S0126	1	RES,MTL FILM,330K,5%,0402,SM,LF	R4261		FW_LVG_NEW

FireWire Port Power

SYNC_MASTER=K19_MLB SYNC_DATE=11/02/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7902	D
SCALE	SHT	OF
NONE	42	109

FireWire PHY Config Straps

Configures PHY for:

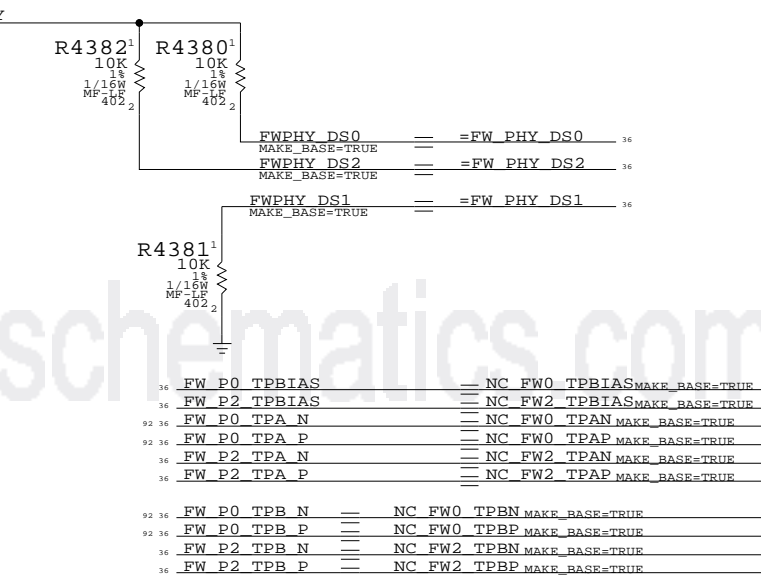
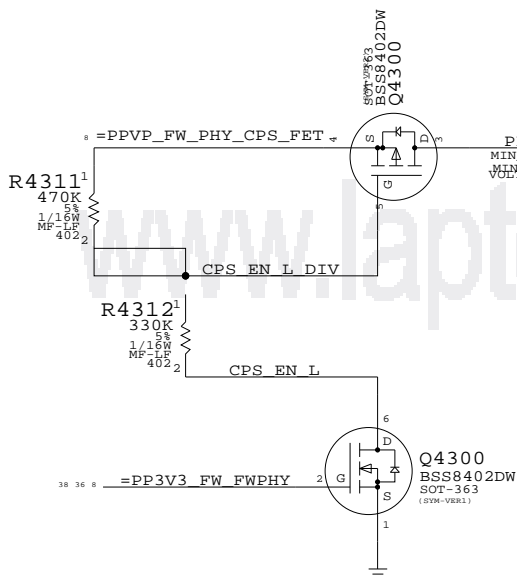
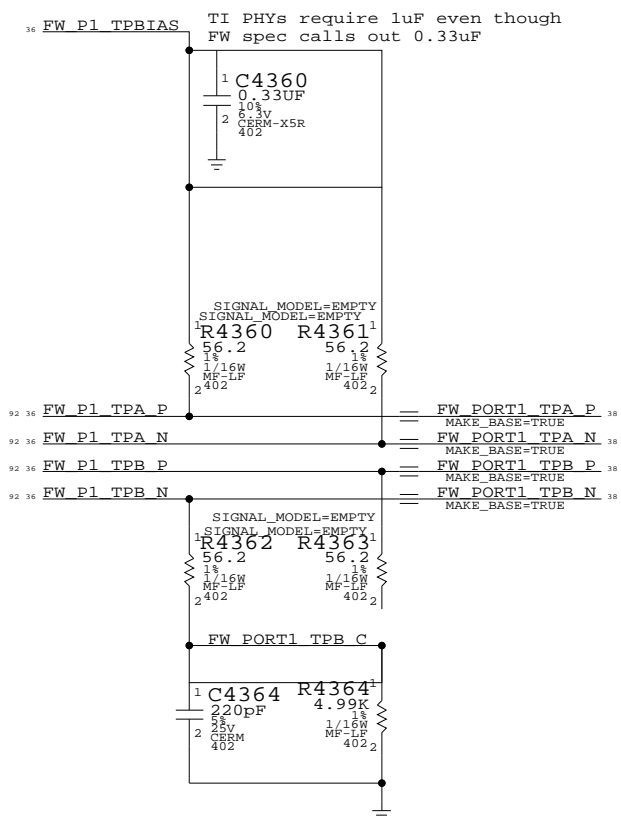
- 1-port Portable Power Class (0)
- Port "1" Bilingual (1394B)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

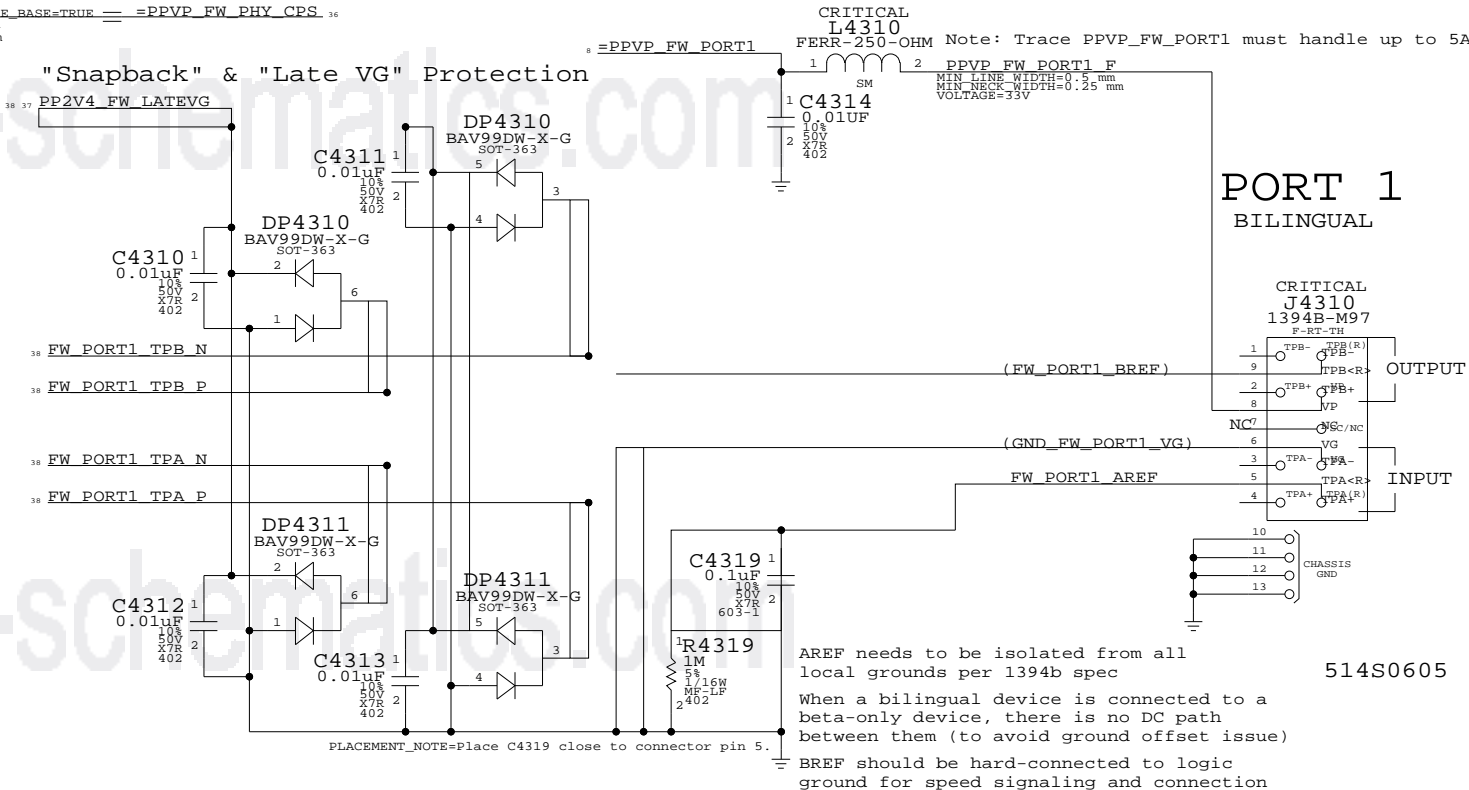
NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

Termination

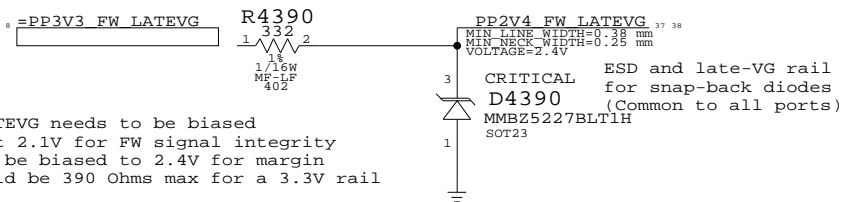
Place close to FireWire PHY



Cable Power



Late-VG Protection Power



PP2V4_FWLATEVG needs to be biased
to at least 2.1V for FW signal integrity
and should be biased to 2.4V for margin
R4390 should be 390 Ohms max for a 3.3V rail

FireWire Ports

SYNC_MASTER=SENSOR	SYNC_DATE=08/14/2008
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APPLE INC.

SIZE
D

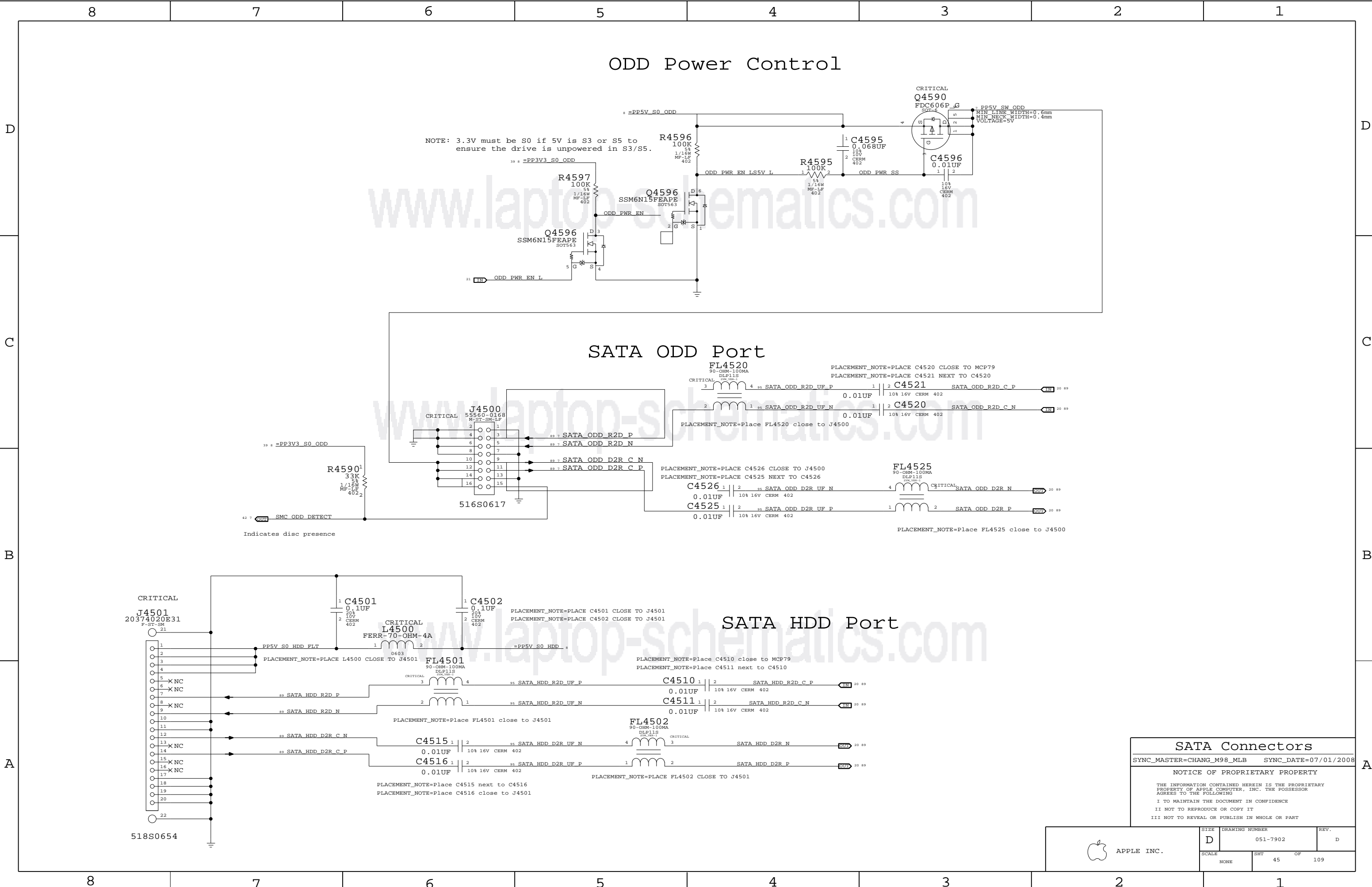
DRAWING NUMBER
051

EV.


SCALE	
	NONE

SHT

109

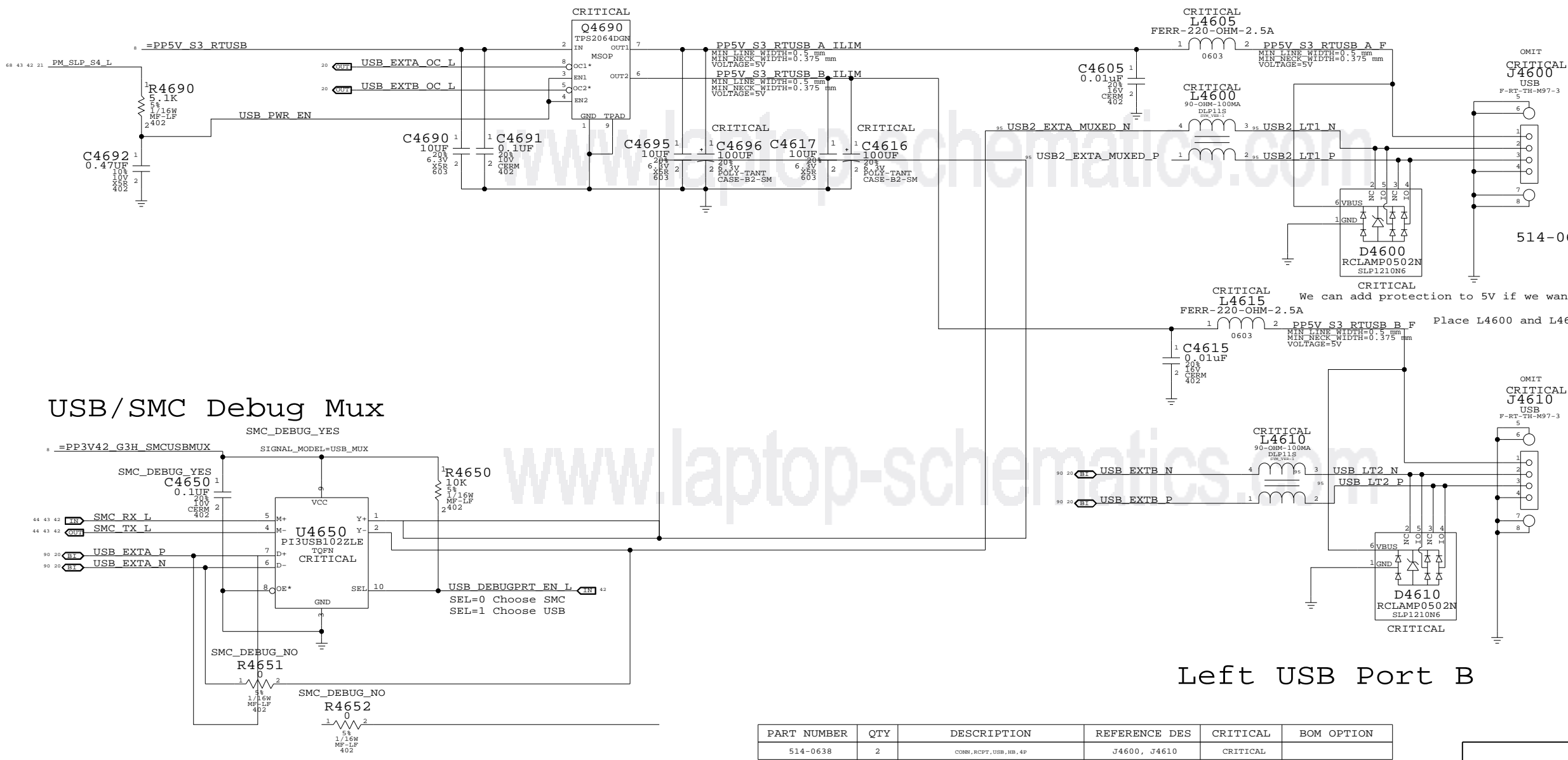


SATA Connectors		
SYNC_MASTER=CHANG_M98_MLB SYNC_DATE=07/01/2008		
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	D	051-7902	D
SCALE		SHT	OF
NONE		45	109

Port Power Switch

Left USB Port A



Left USB Port B

External USB Connectors

SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=07/02/2008

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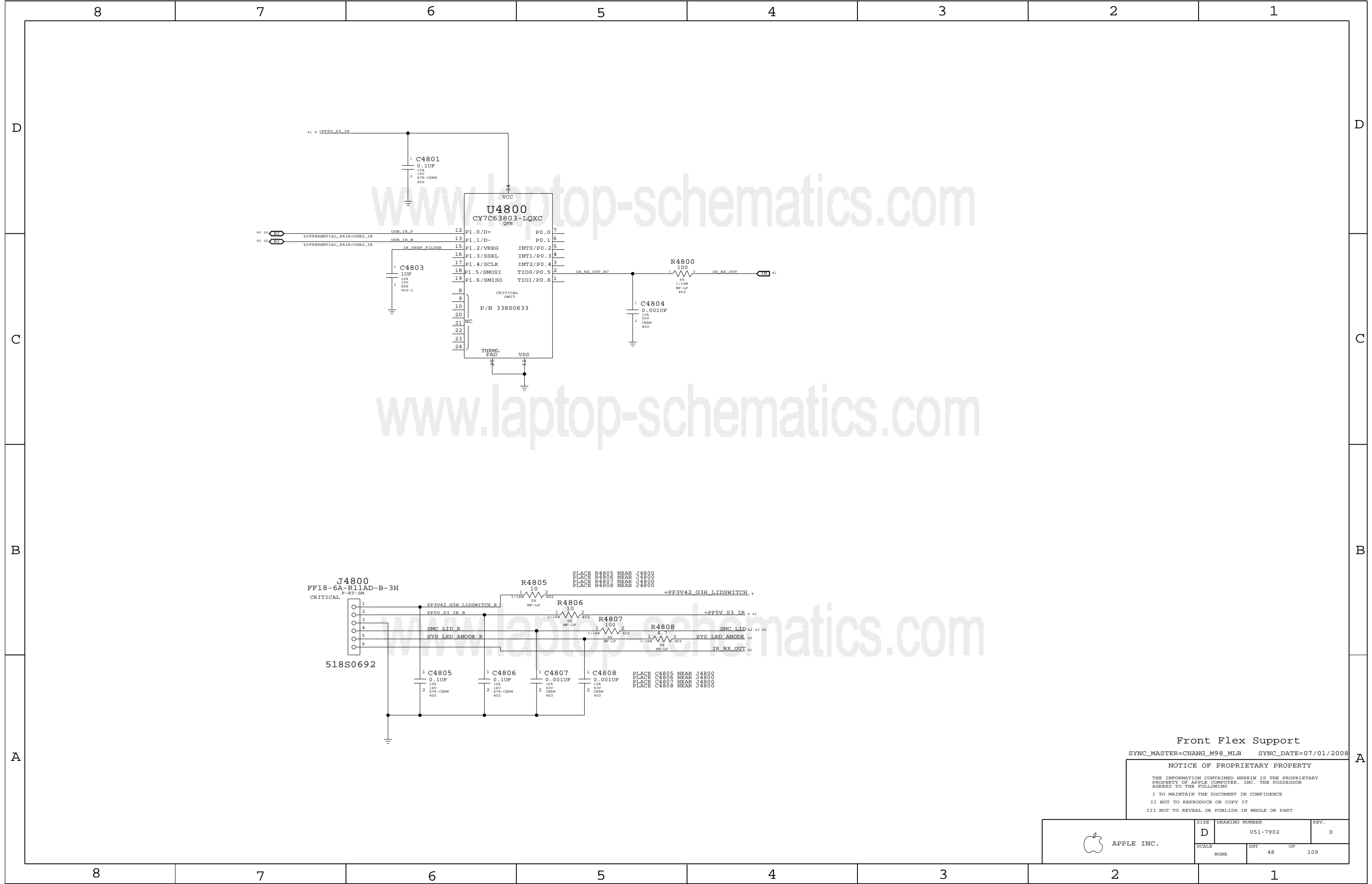
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SIZE	DRAWING NUMBER	REV.
D	051-7902	D
SCALE	SHT	OF
NONE	46	109

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-0638	2	CONN, RCPT, USB, HB, 4P	J4600, J4610	CRITICAL	



Front Flex Support
SYNC_MASTER=CHANG_M98_MLB SYNC_DATE=07/01/2008


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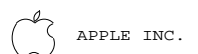
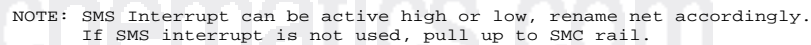
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 APPLE INC.	SIZE D	DRAWING NUMBER 051-7902	REV. D
	SCALE NONE	SHT 48	OF 109

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SMC

SYNC_MASTER=T18_MLB	SYNC_DATE=06/18/2008	7
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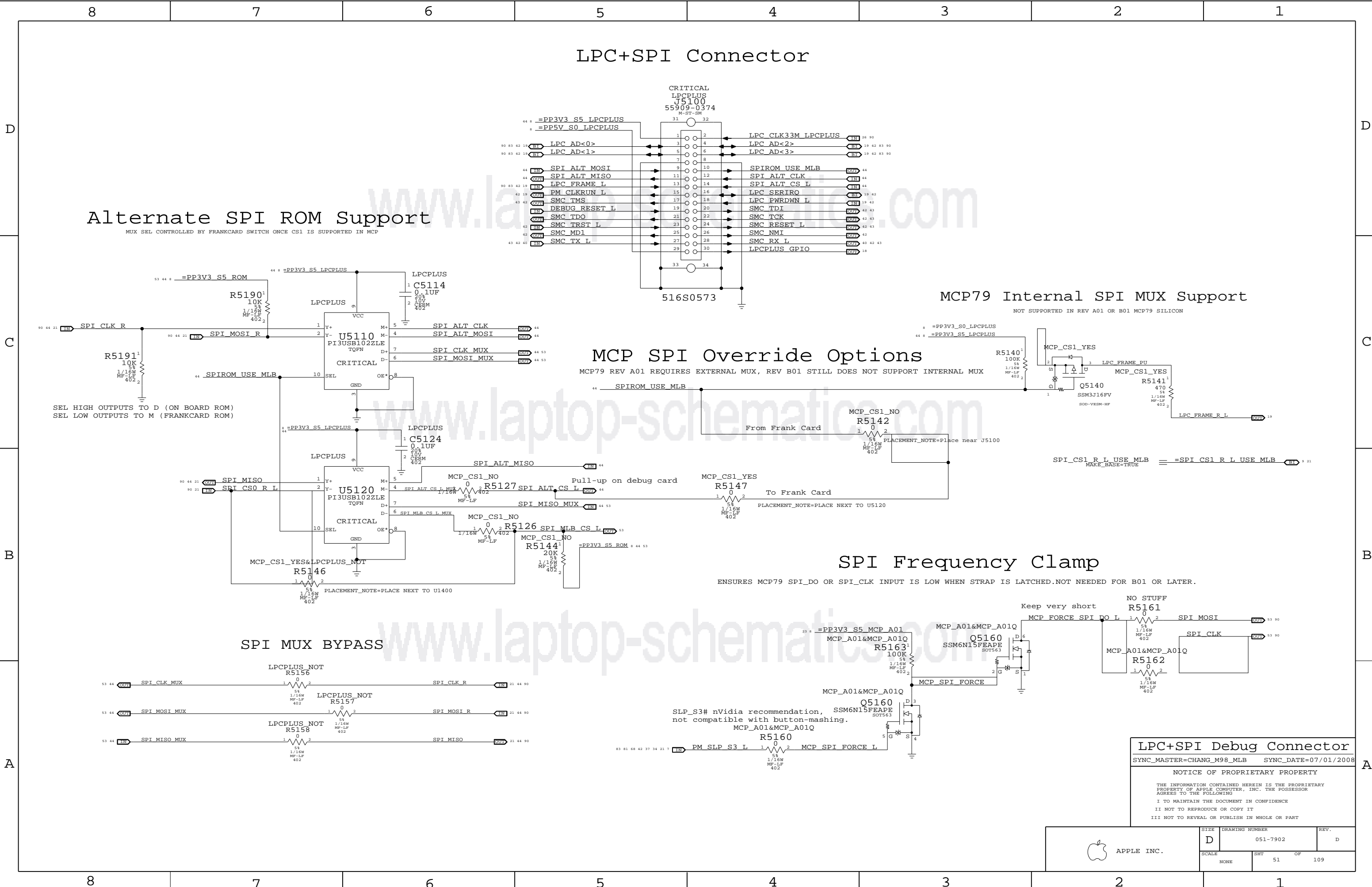
SIZE	DRAWING NUMBER
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SIZE	DRAWING NUMBER	REV.
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D	051-7902	D
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SCALE	SHT	OF
	49	109



LPC+SPI Debug Connector

SYNC_MASTER=CHANG_M98_MLB SYNC_DATE=07/01/2008

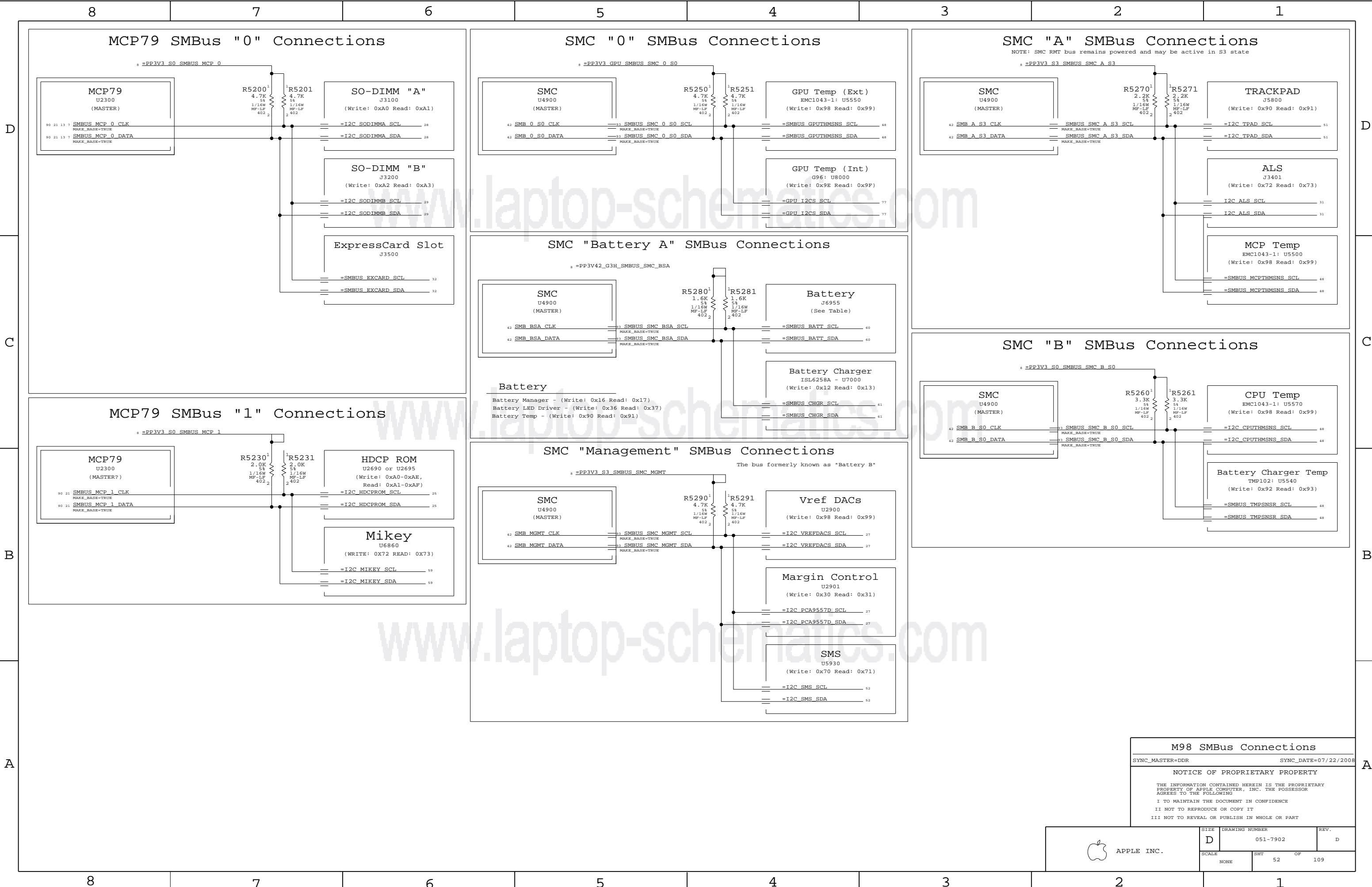
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SCALE	SHT	OF
NONE	51	109



M98 SMBus Connections

SYNC_MASTER=DDR

SYNC_DATE=07/22/2008

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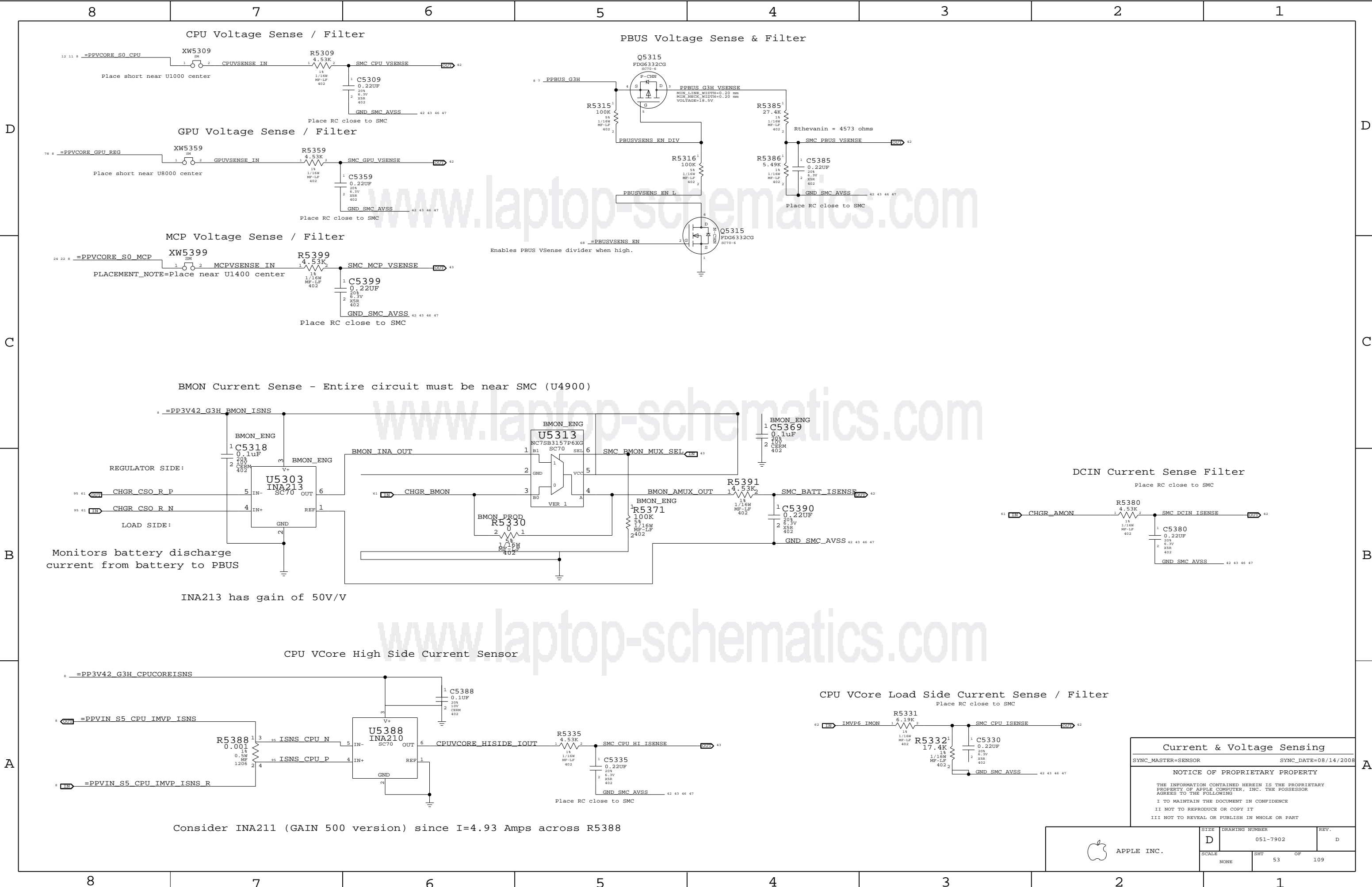
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SCALE		SHT	OF	REV.
NONE		52	109	



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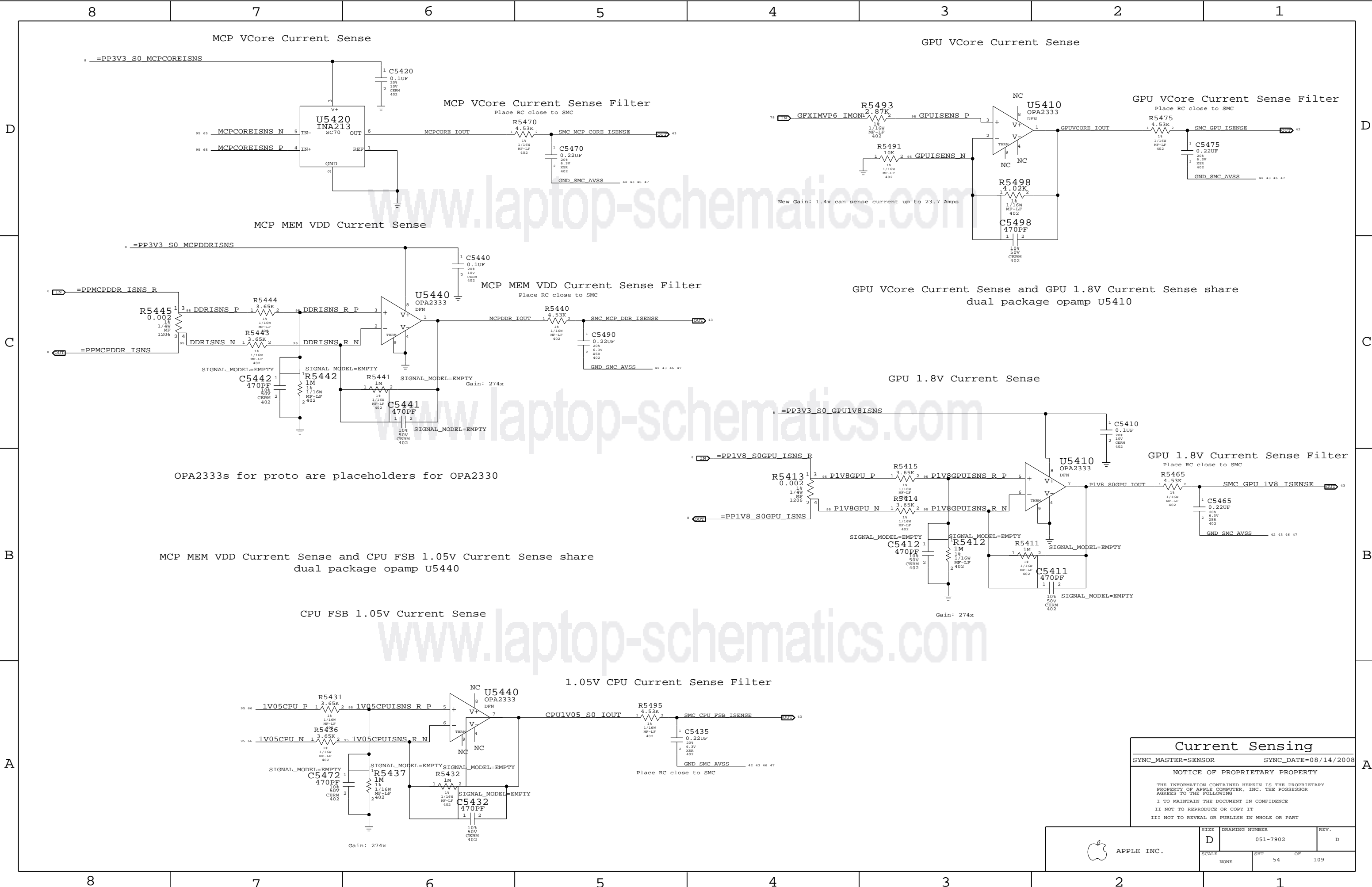
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Current & Voltage Sensing	
SYNC_MASTER=SENSOR	SYNC_DATE=08/14/2008
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SCALE		SHT	OF
NONE		53	109



MCP VCore Current Sense

GPU VCore Current Sense

MCP VCore Current Sense Filter

GPU VCore Current Sense Filter

MCP MEM VDD Current Sense

MCP MEM VDD Current Sense Filter

GPU VCore Current Sense and GPU 1.8V Current Sense share dual package opamp U5410

GPU 1.8V Current Sense

GPU 1.8V Current Sense Filter

1.05V CPU Current Sense Filter

Current Sensing

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

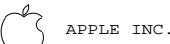
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SIZE D DRAWING NUMBER 051-7902 REV. D

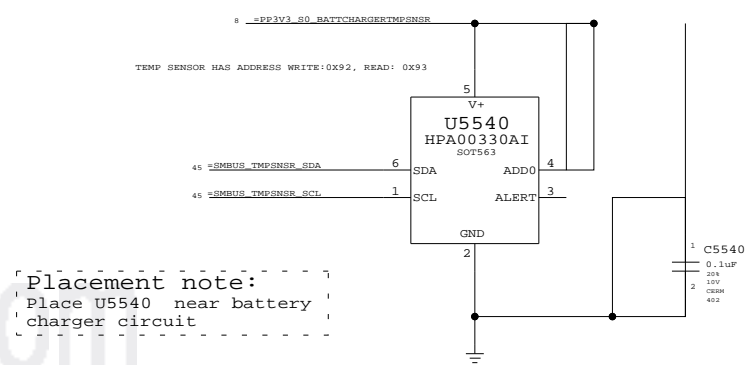
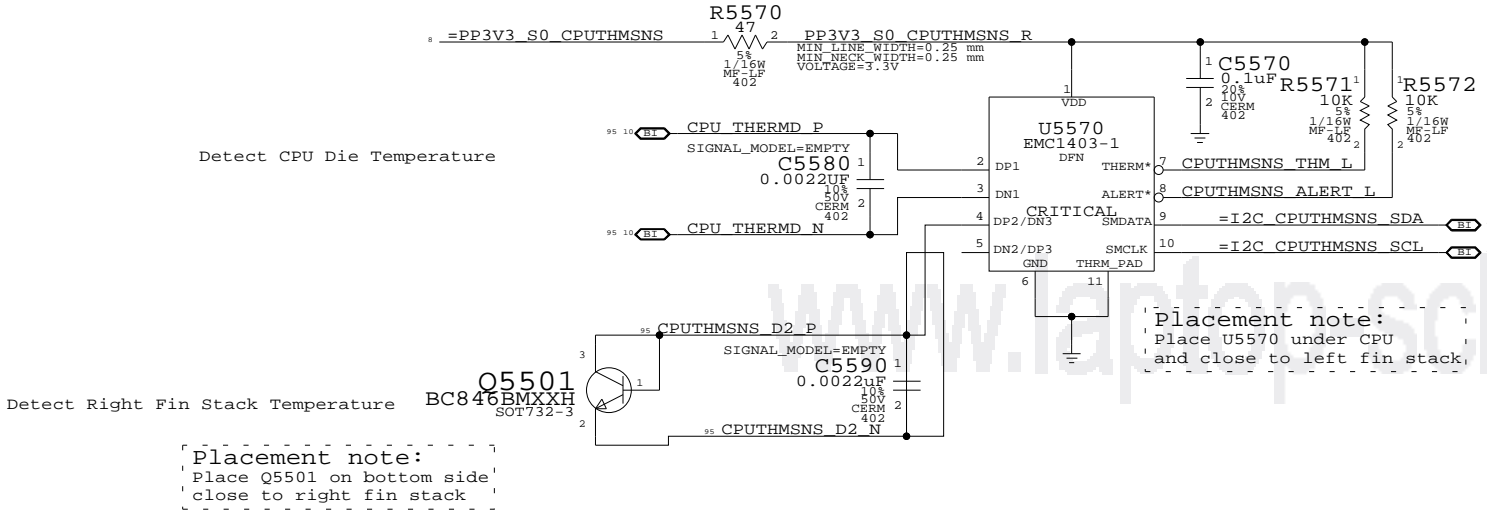
SCALE NONE SHT 54 OF 109

CPU Proximity/CPU Die/Right Fin Stack

Battery Charger Proximity

D

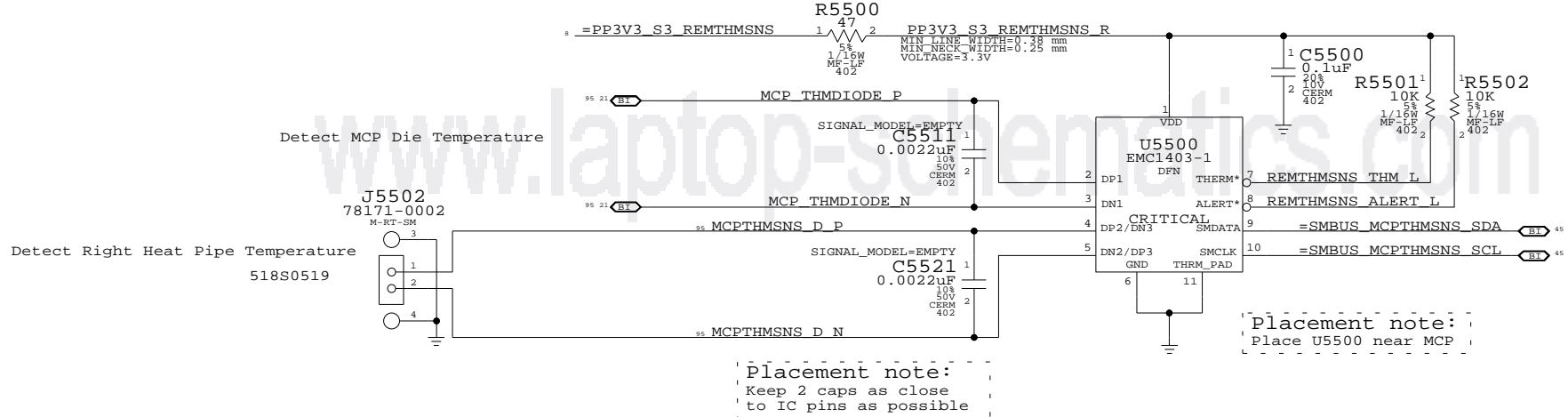
D



MCP Proximity/MCP Die/Right Heat Pipe

C

C

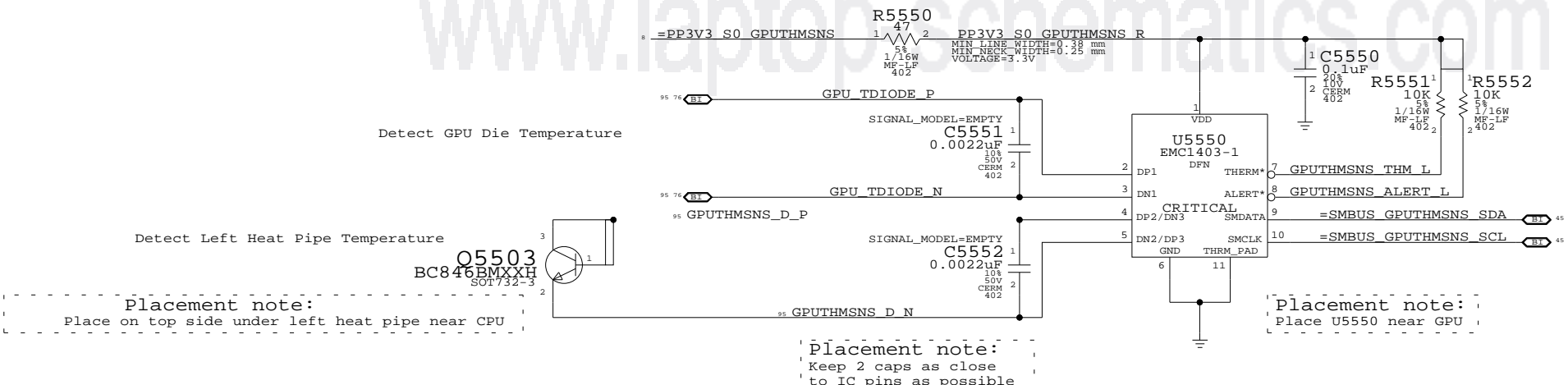


Note: EMC1403 can perform Beta Compensation for External Diode 1 only

GPU Proximity/GPU Die/Left Heat Pipe

B

B

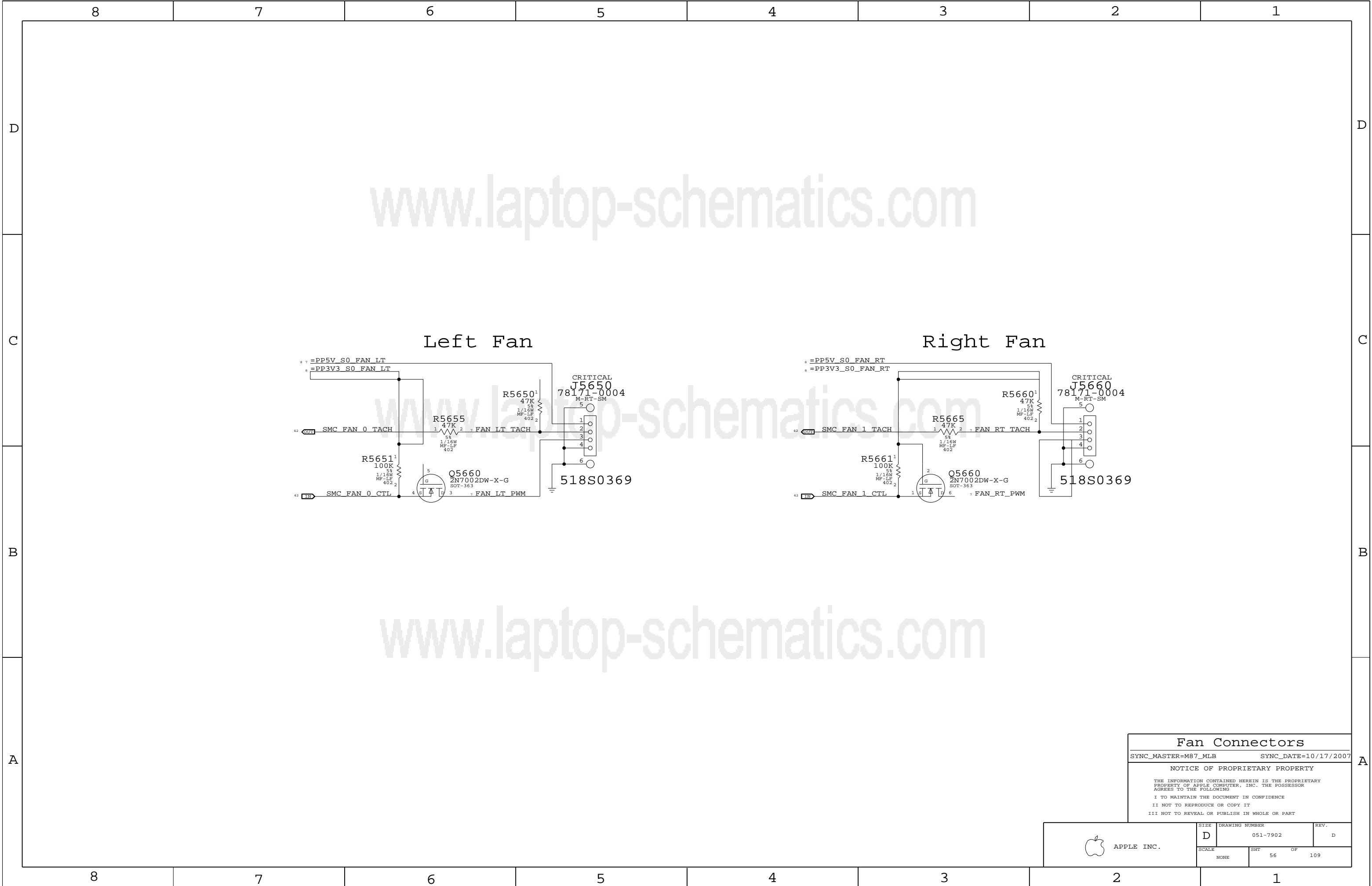


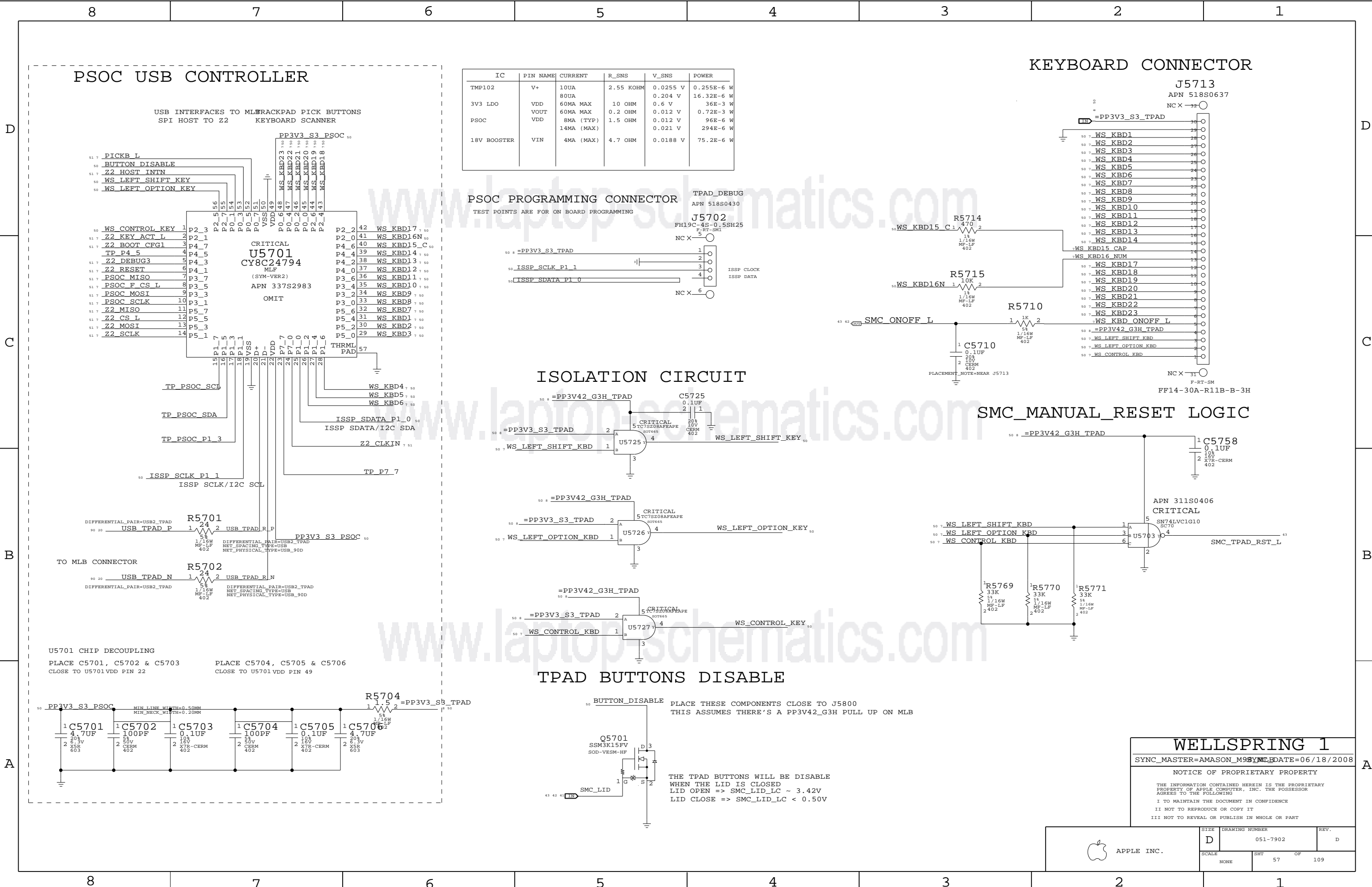
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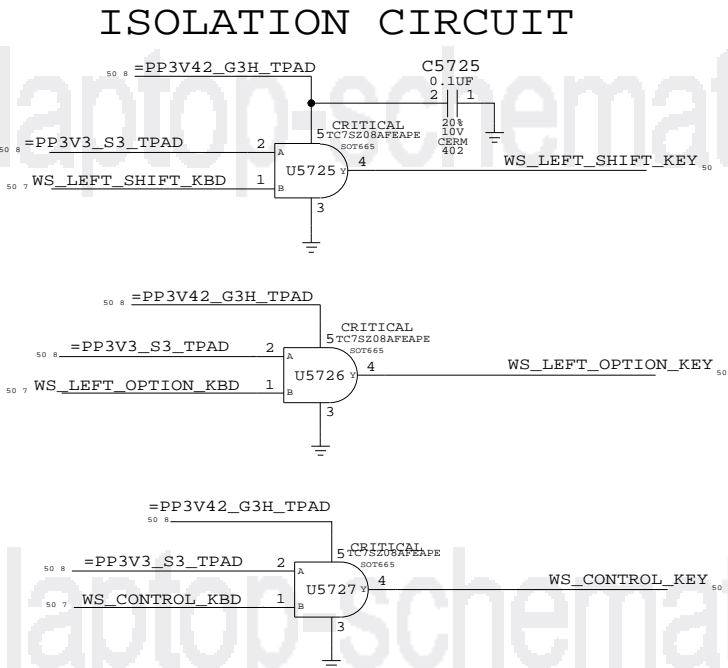
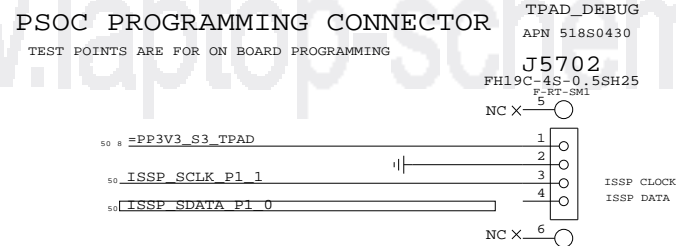
Thermal Sensors	
SYNC_MASTER=SENSOR	SYNC_DATE=08/14/2008
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	D	051-7902	D
SCALE		SHT	OF
NONE		55	109





IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	100UA	2.55 KOHM	0.0255 V	0.255E-6 W
3V3 LDO	VDD	80UA	0.204 V	16.32E-6 W	
PSOC	VOUT	60MA MAX	10 OHM	0.6 V	36E-3 W
	VDD	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
		8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

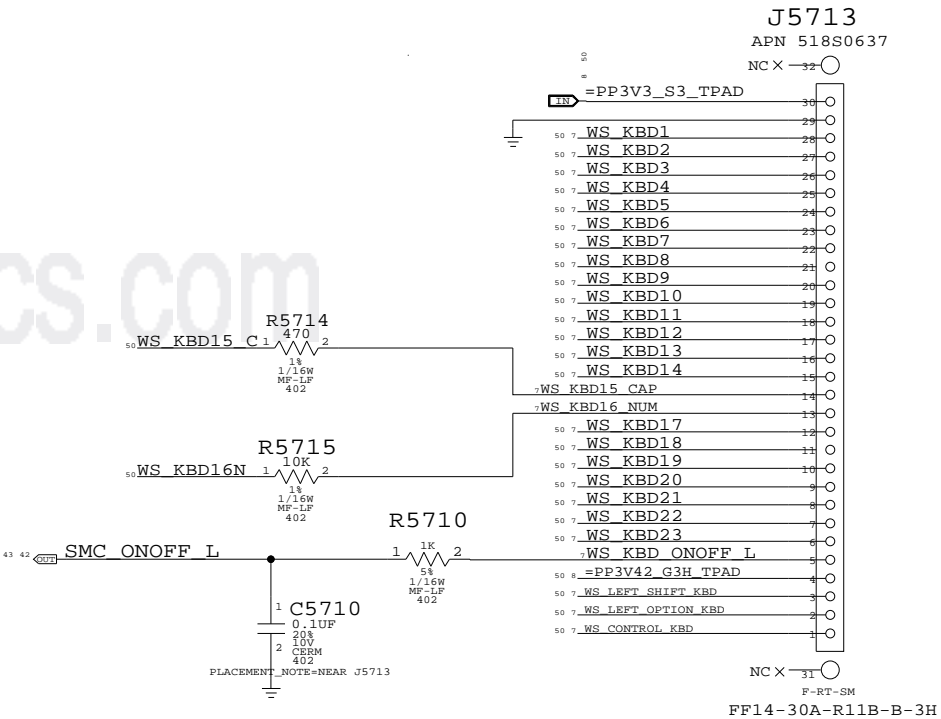


TPAD BUTTONS DISABLE

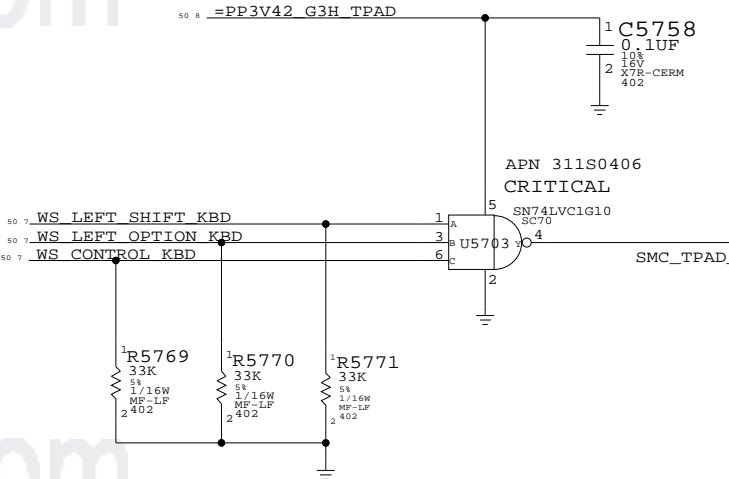
PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

KEYBOARD CONNECTOR



SMC_MANUAL_RESET LOGIC



WELLSPRING 1

SYNC_MASTER=AMASON_M9 SYNC_DATE=06/18/2008

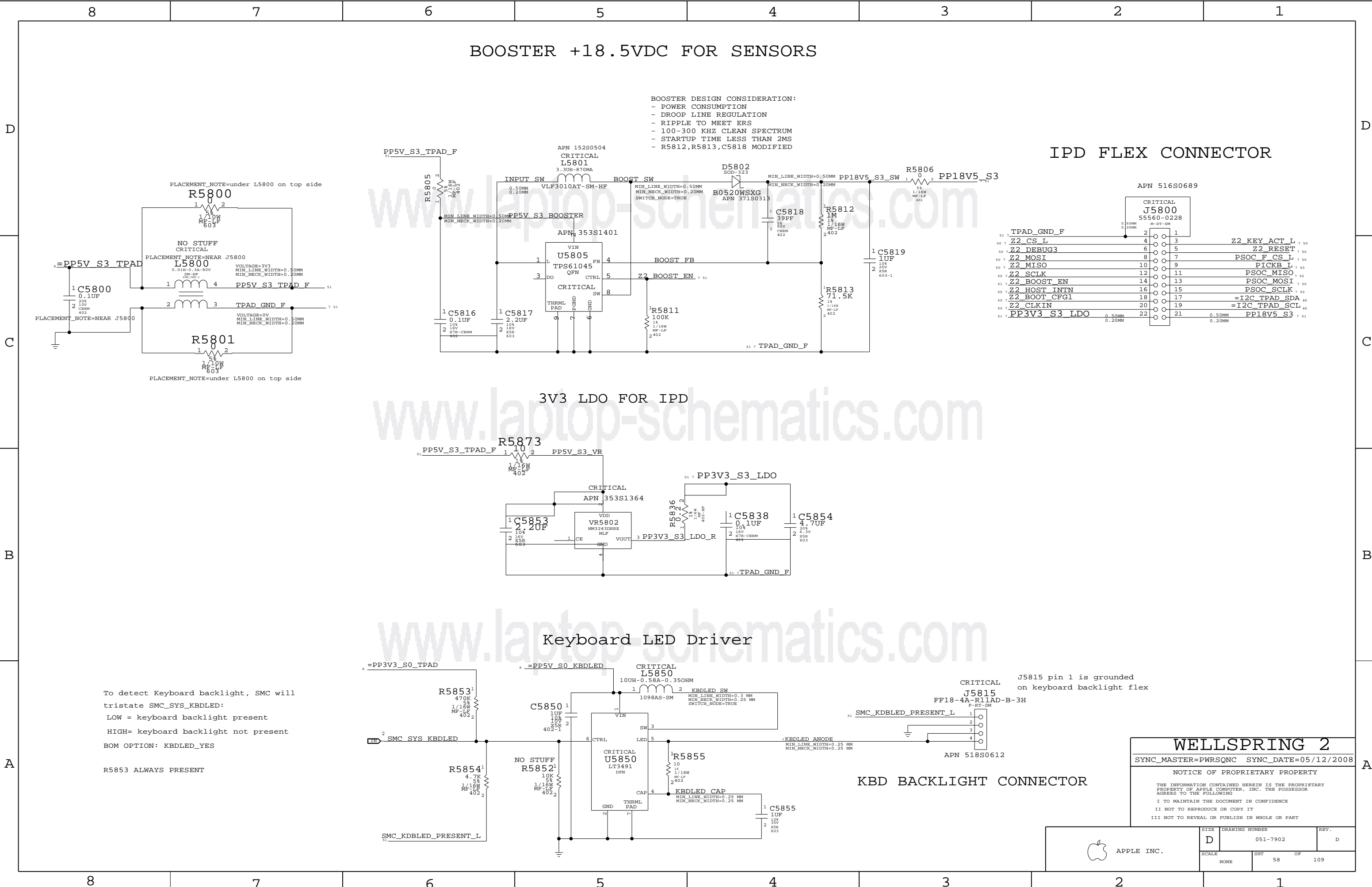
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SIZE	DRAWING NUMBER	REV.
D	051-7902	D
SCALE	SHT	OF
NONE	57	109



not used.

32 =PP3V3_S3_SMS

45 =I2C_SMS_SCL

PROD_DIGSMS

U5930

ENG_DIGSMS

C5931

C5932

A diagram showing a rectangular box. Inside the box, there is a central dot with two arrows pointing away from it: one pointing upwards and slightly to the left, and another pointing to the right. Above the box, there is a small circle. To the left of the box, the text "+Z (up)" is written. To the right of the box, the text "+X" is written. Below the box, the text "Front of system" is written, with a downward-pointing arrow below it.

Circle indicates pin 1 in correct orientation

Circle indicates pin 1 in correct orientation

Circle indicates pin 1 in correct orientation

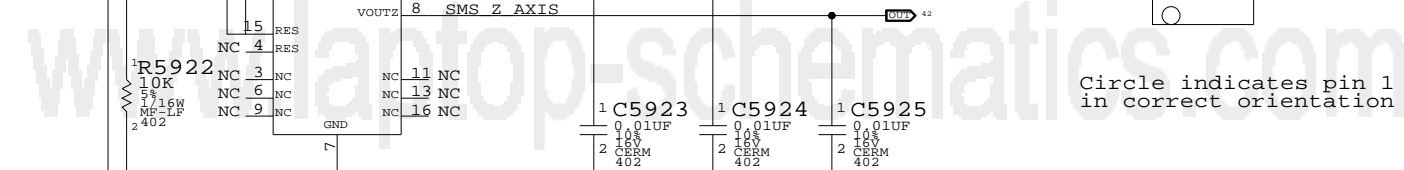

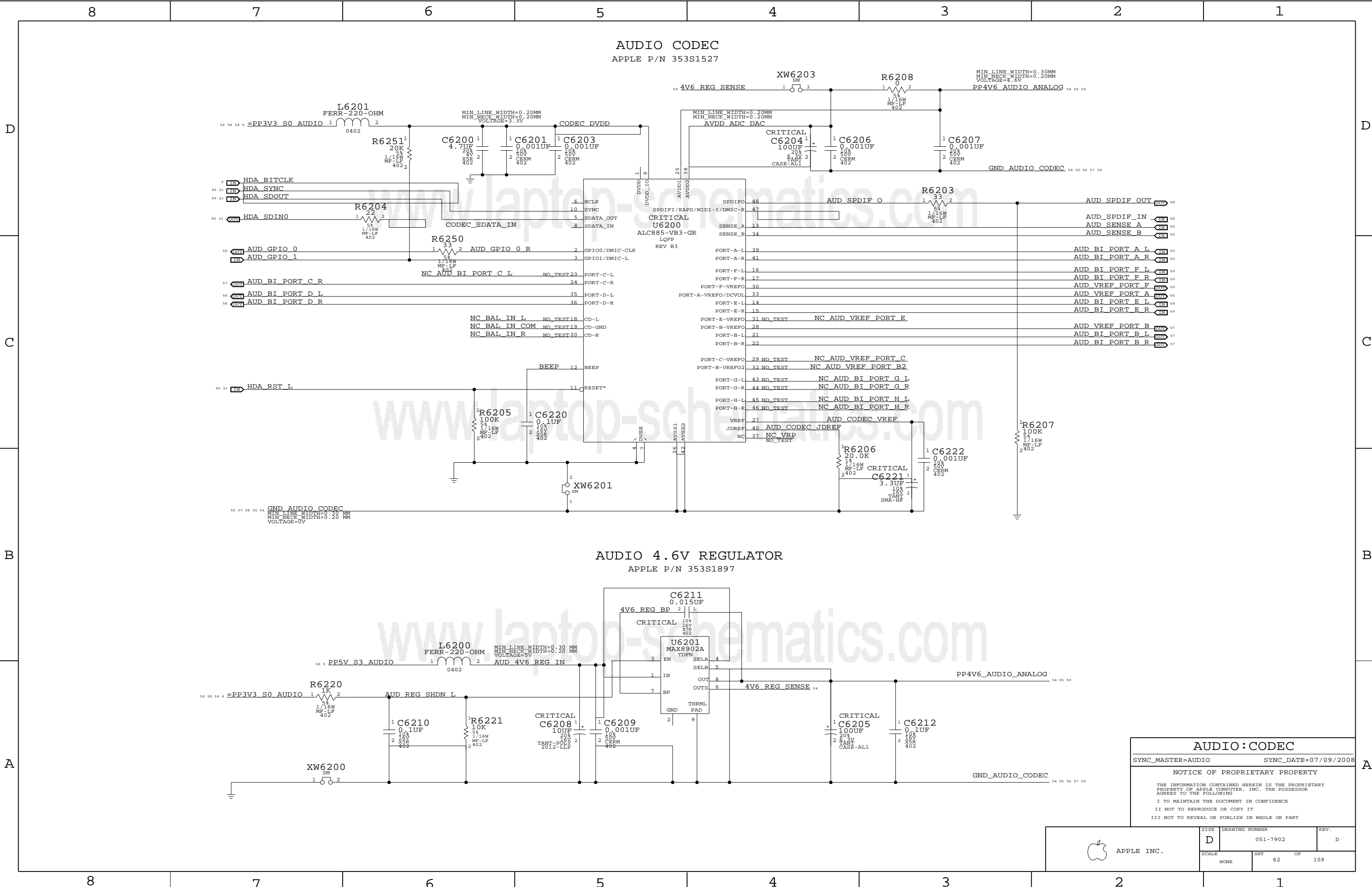


Diagram illustrating a coordinate system for a system. The system is represented by a box. The vertical axis is labeled $+Y$ (up) and the horizontal axis is labeled $+X$ (right). The vertical axis is also labeled $+Z$ (up). The horizontal axis is also labeled Front of system with a downward arrow pointing to a dot.

 APPLE INC.	SIZE D	DRAWING NUMBER 051-7902	REV. D
	SCALE NONE	SHT OF 59 109	



AUDIO:CODEC

SYNC_MASTER=AUDIO

SYNC_DATE=07/09/2008


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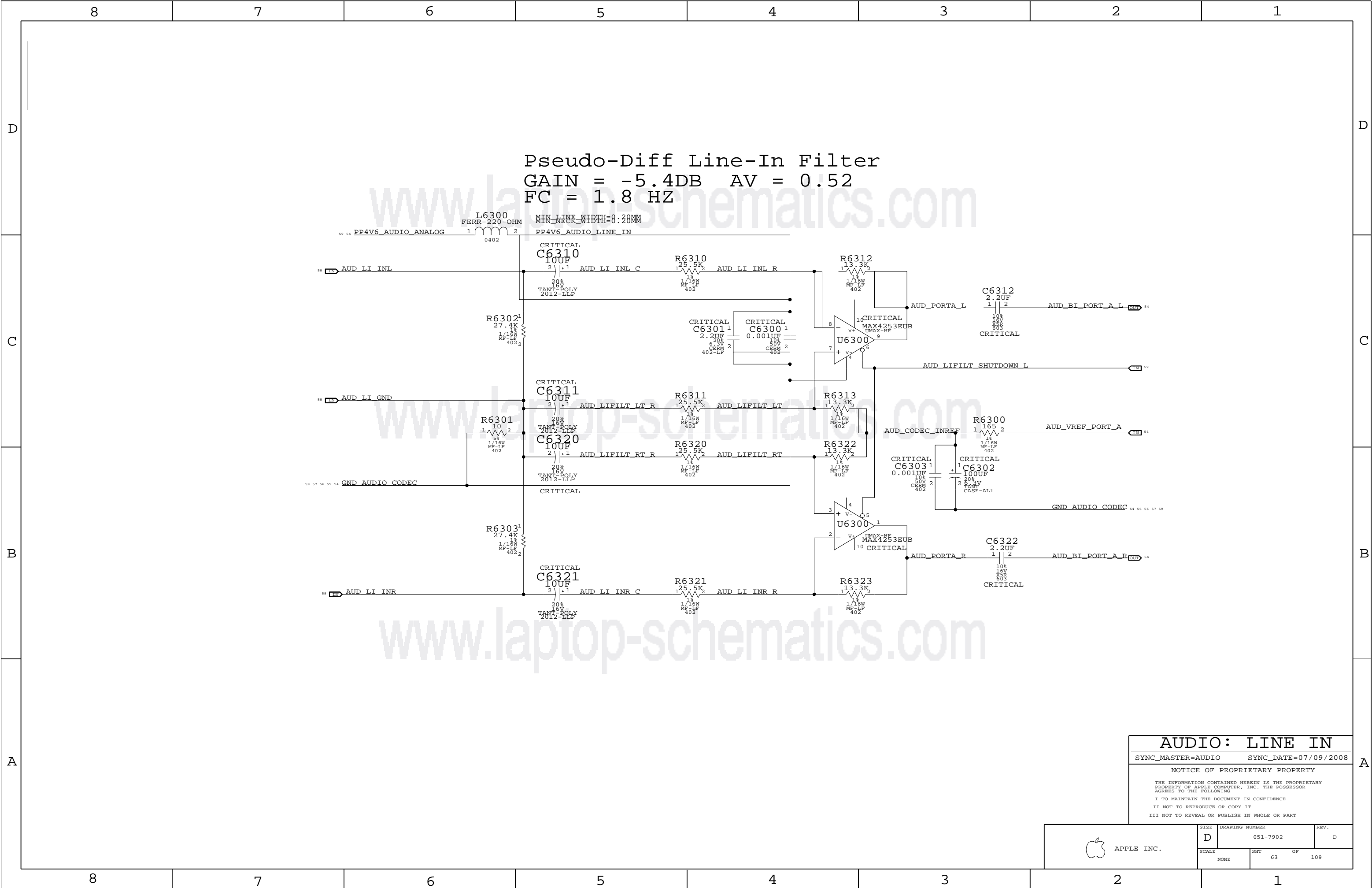
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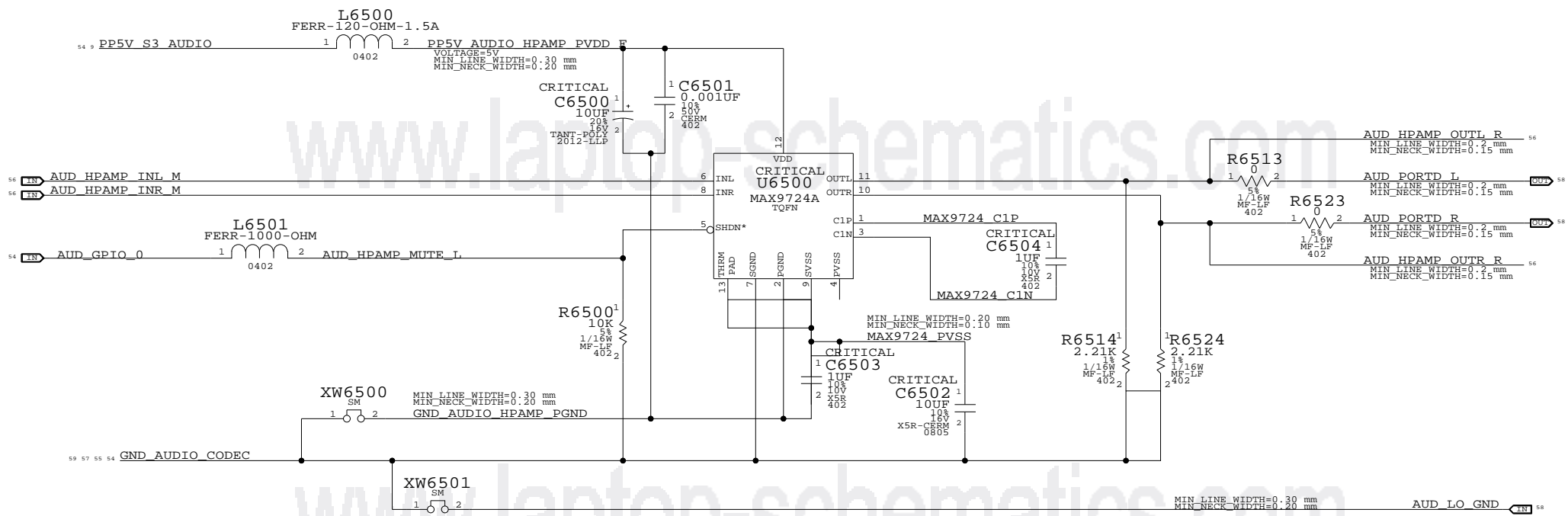
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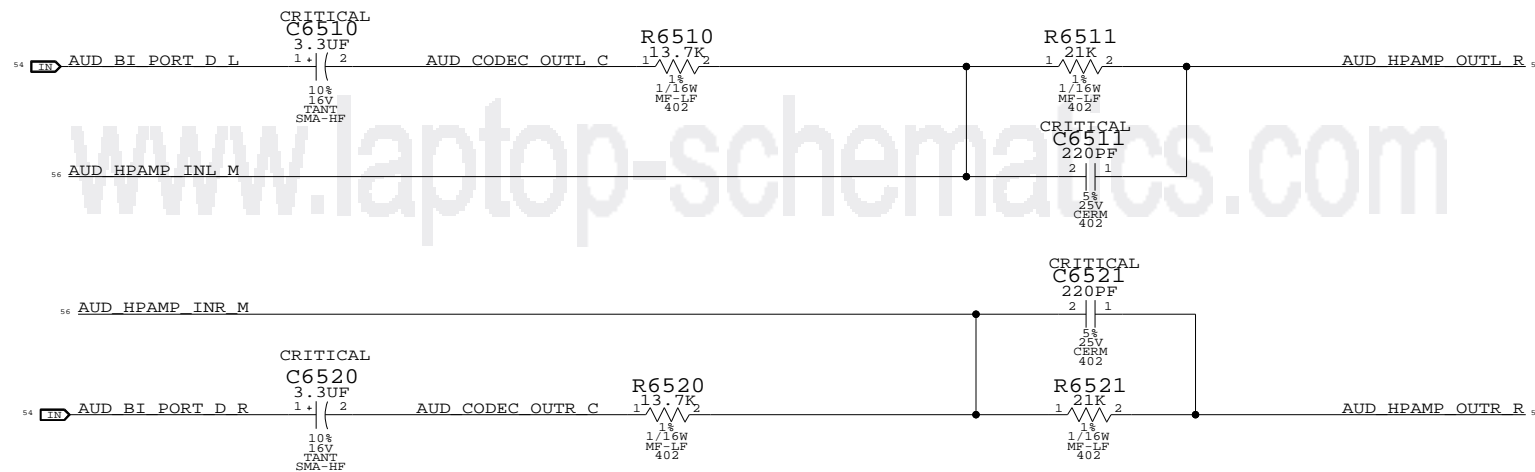
 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7902	D
SCALE		SHT	OF
NONE		62	109



Headphone Amplifier (MAX9724A)
APN:353S1637

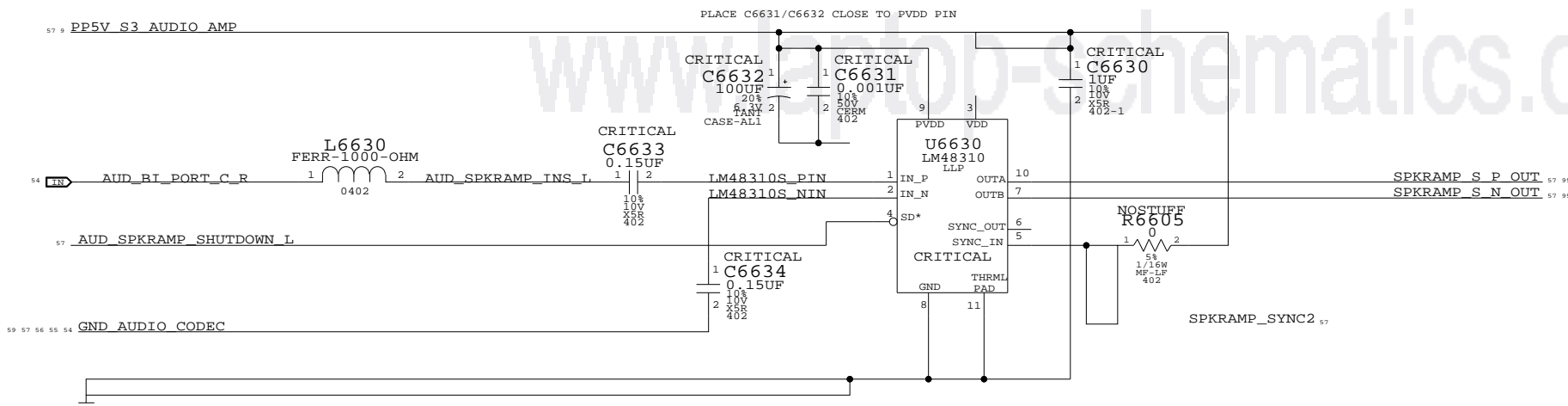
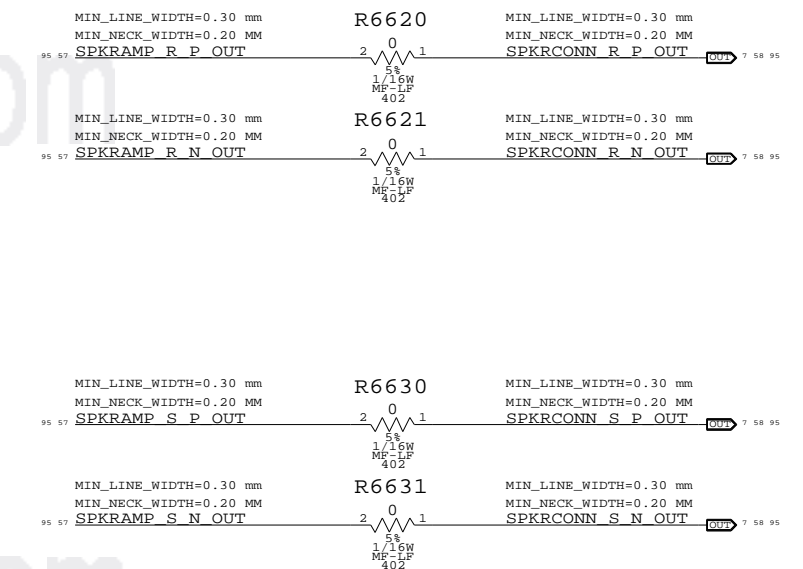
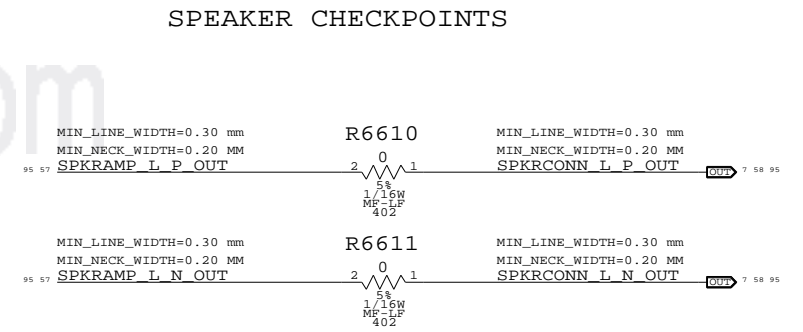



1st Order DAC Filter
HP:3.52 HZ LP:34 KHZ
VOLTAGE GAIN:1.53



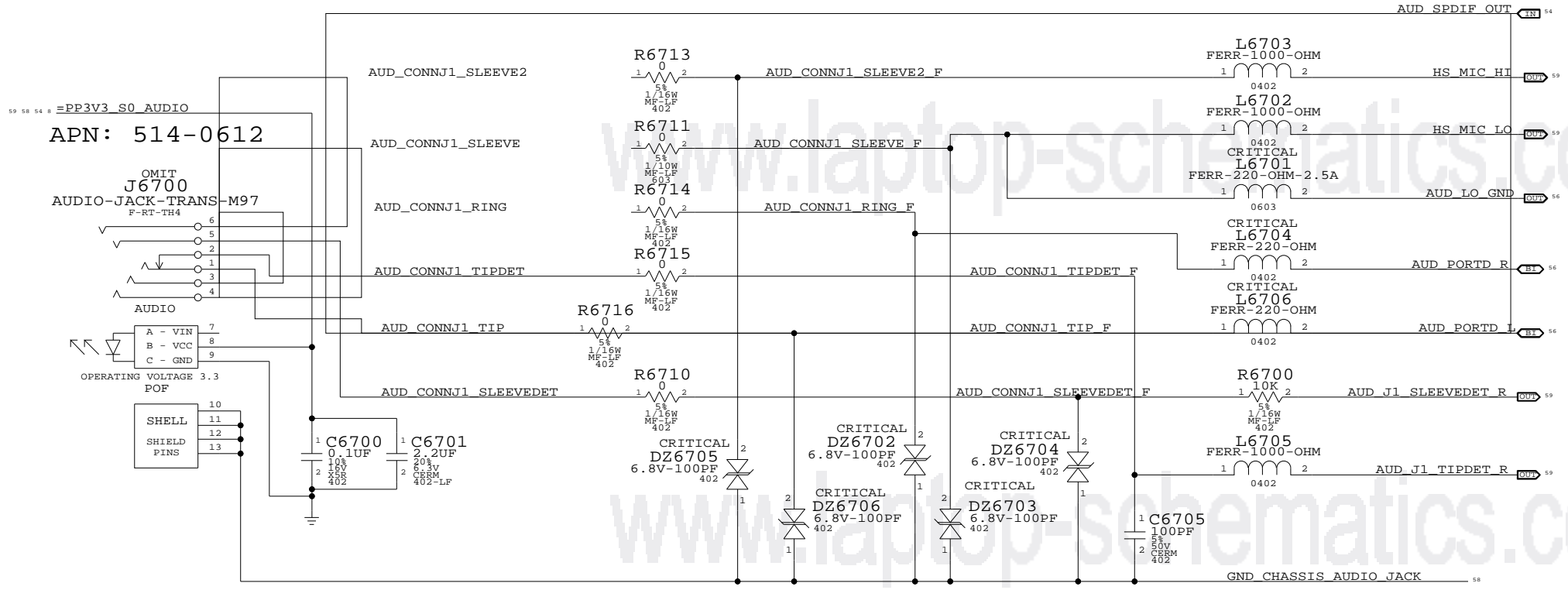
AUDIO: HEADPHONE AMP
SYNC_MASTER=AUDIO SYNC_DATE=07/09/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7902	D
SCALE		SHT	OF
NONE		65	109

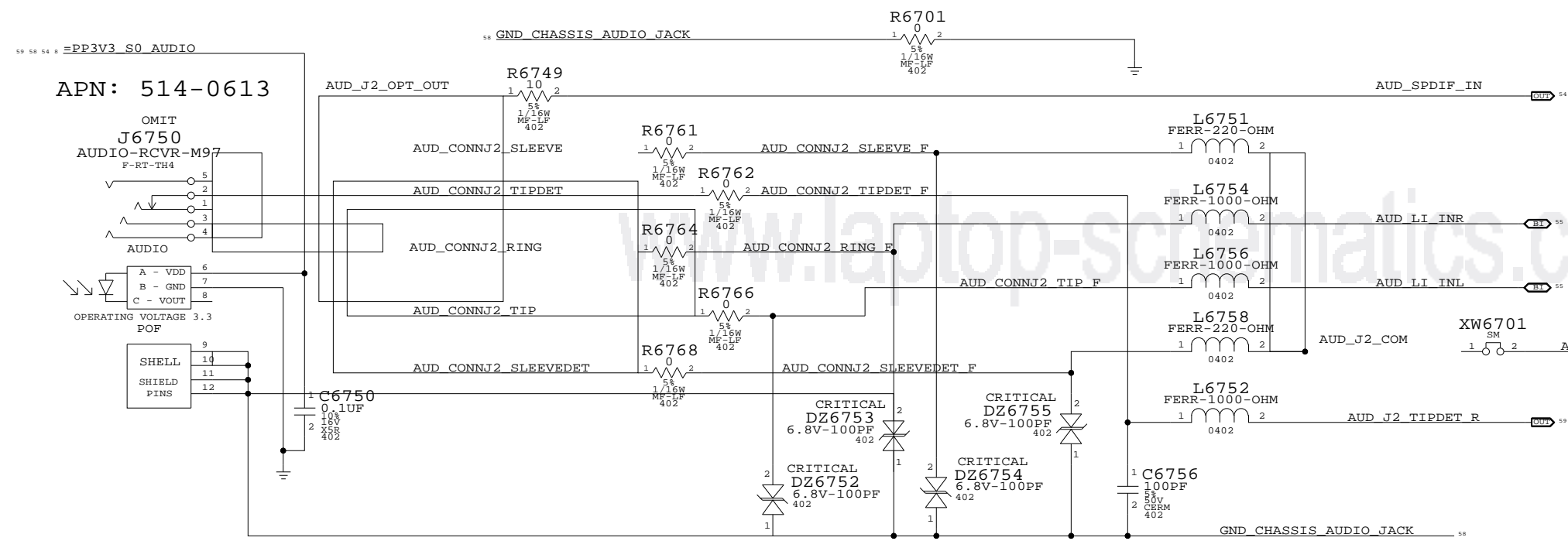
$$53\text{Hz} < \text{FC (SUB)} < 62\text{Hz}$$


 APPLE INC.	SIZE	DRAWING NUMBER		REV.
	D	051-7902		D
	SCALE	SHT	OF	
	NONE	66	109	

AUDIO JACK 1 LO/HP JACK, SPDIF TX



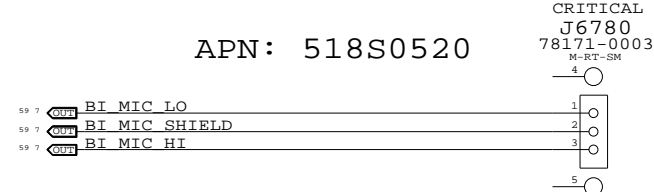
RETURN FOR HF NOISE



AUDIO JACK 2 LINE IN JACK, SPDIF RX

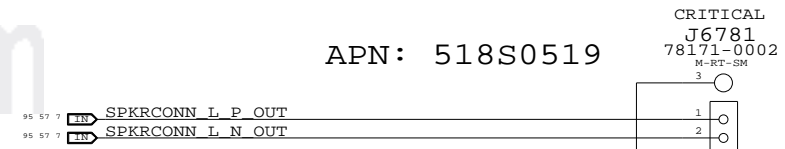
MIC CONNECTOR

APN: 518S0520

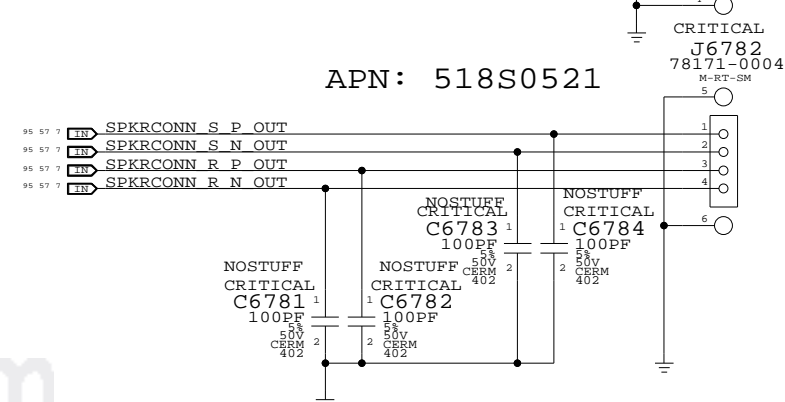


SPEAKER CONNECTOR

APN: 518S0519



APN: 518S0521



AUDIO: JACKS

SYNC_MASTER=AUDIO SYNC_DATE=07/09/2008

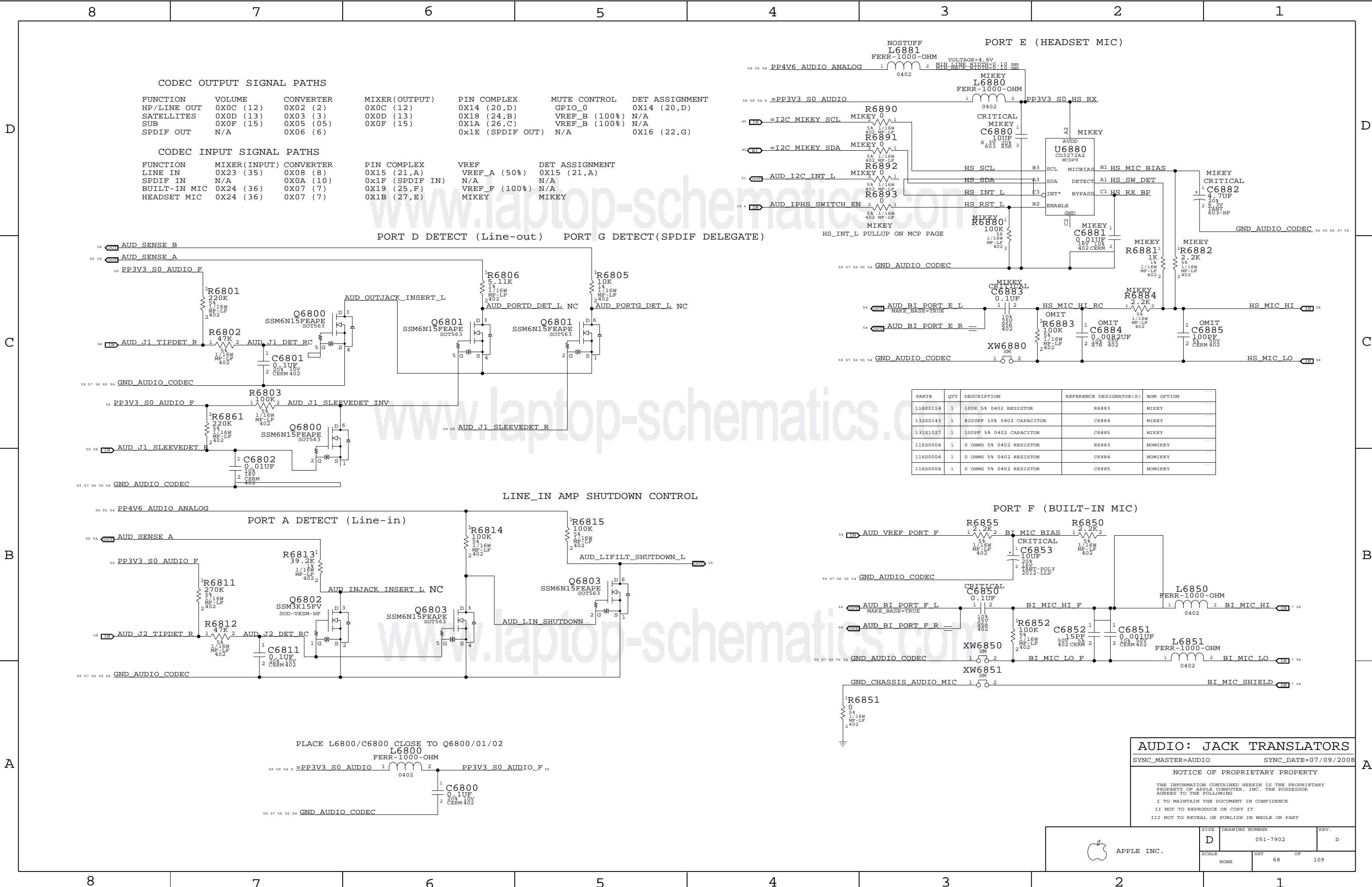
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SIZE	DRAWING NUMBER	REV.
D	051-7902	D
SCALE	SHT	OF
NONE	67	109



CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	MIXER(OUTPUT)	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X0C (12)	0X02 (2)	0X0C (12)	0X14 (20,D)	GPIO_0	0X14 (20,D)
SATELLITES	0X0D (13)	0X03 (3)	0X0D (13)	0X18 (24,B)	VREF_B (100%)	N/A
SUB	0X0F (15)	0X05 (05)	0X0F (15)	0X1A (26,C)	VREF_B (100%)	N/A
SPDIF OUT	N/A	0X06 (6)		0x1E (SPDIF OUT)	N/A	0X16 (22,G)

CODEC INPUT SIGNAL PATHS

FUNCTION	MIXER(INPUT)	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X23 (35)	0X08 (8)	0X15 (21,A)	VREF_A (50%)	0X15 (21,A)
SPDIF IN	N/A	0X0A (10)	0x1F (SPDIF IN)	N/A	N/A
BUILT-IN MIC	0X24 (36)	0X07 (7)	0X19 (25,F)	VREF_F (100%)	N/A
HEADSET MIC	0X24 (36)	0X07 (7)	0X1B (27,E)	MIKEY	MIKEY

PORT D DETECT (Line-out) PORT G DETECT (SPDIF DELEGATE)

PORT E (HEADSET MIC)

PORT F (BUILT-IN MIC)

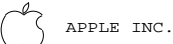
PLACE L6800/C6800 CLOSE TO Q6800/01/02

AUDIO: JACK TRANSLATORS

SYNC_MASTER=AUDIO SYNC_DATE=07/09/2008

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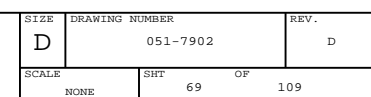
APPLE INC.

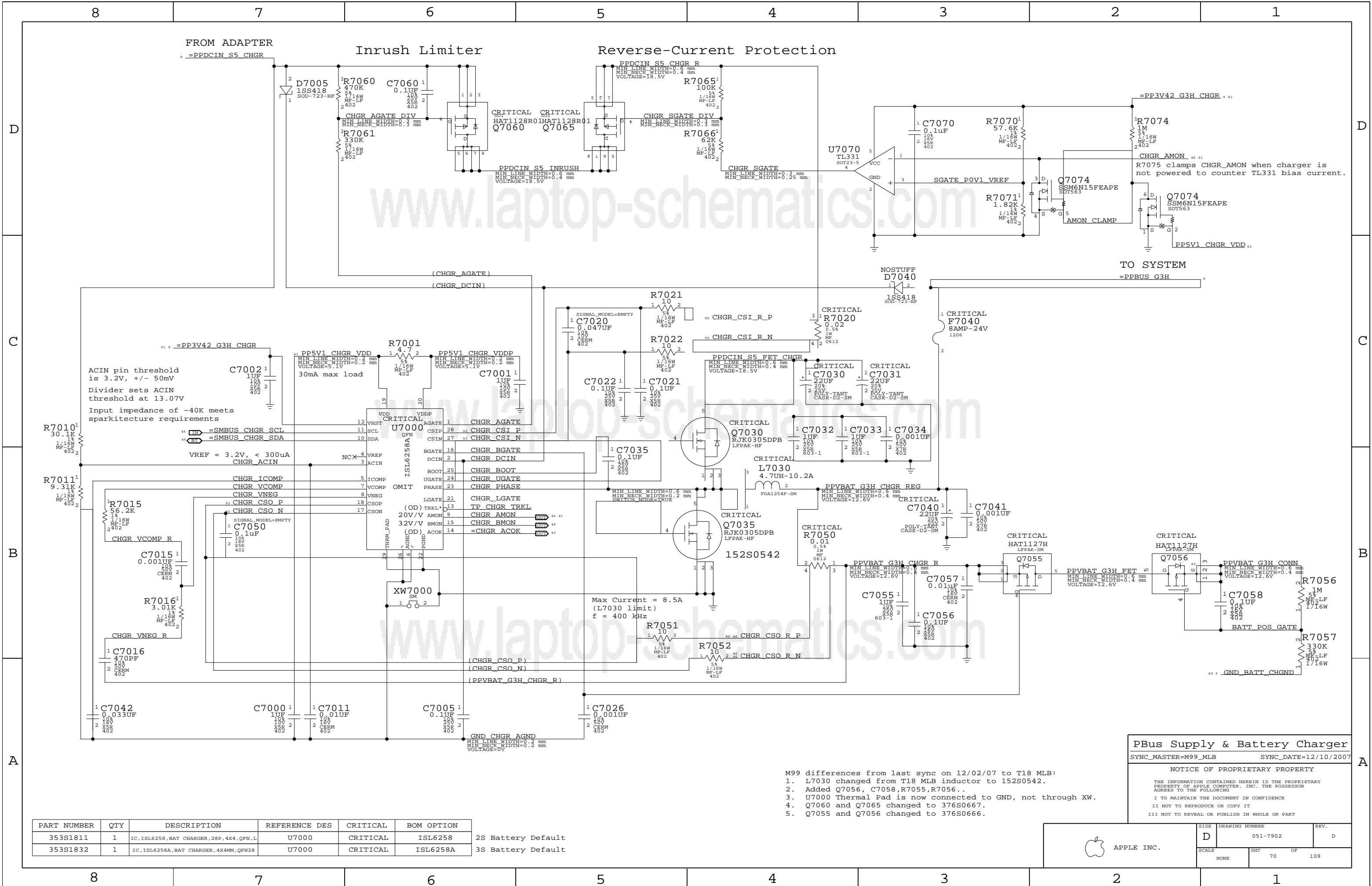
SIZE	DRAWING NUMBER	REV.
D	051-7902	D
SCALE	SHT	OF
NONE	68	109

D



B

A



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S1811	1	IC, ISL6258, BAT CHARGER, 28P, 4X4, QFN, L	U7000	CRITICAL	ISL6258
353S1832	1	IC, ISL6258A, BAT CHARGER, 4X4MM, QFN28	U7000	CRITICAL	ISL6258A

2S Battery Default
3S Battery Default

- M99 differences from last sync on 12/02/07 to T18 MLB:
1. L7030 changed from T18 MLB inductor to 152S0542.
 2. Added Q7056, C7058, R7055, R7056..
 3. U7000 Thermal Pad is now connected to GND, not through XW.
 4. Q7060 and Q7065 changed to 376S0667.
 5. Q7055 and Q7056 changed to 376S0666.

PBus Supply & Battery Charger
SYNC_MASTER=M99_MLB
SYNC_DATE=12/10/2007

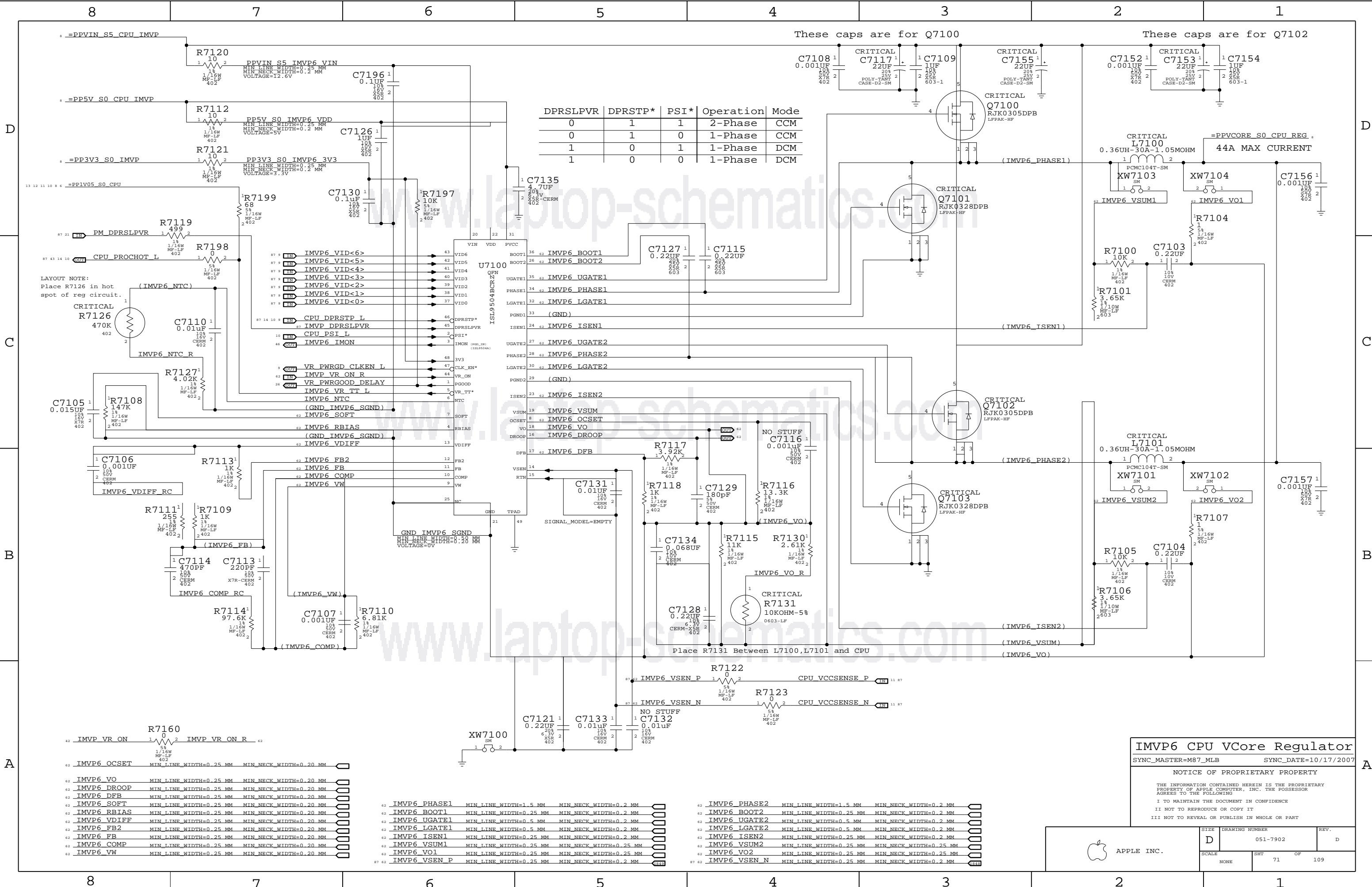
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7902	D
SCALE	SHT	OF
NONE	70	109



DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM

IMVP6 CPU VCore Regulator

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7902	D
SCALE	SHT	OF
NONE	71	109

D

C

B

A

D

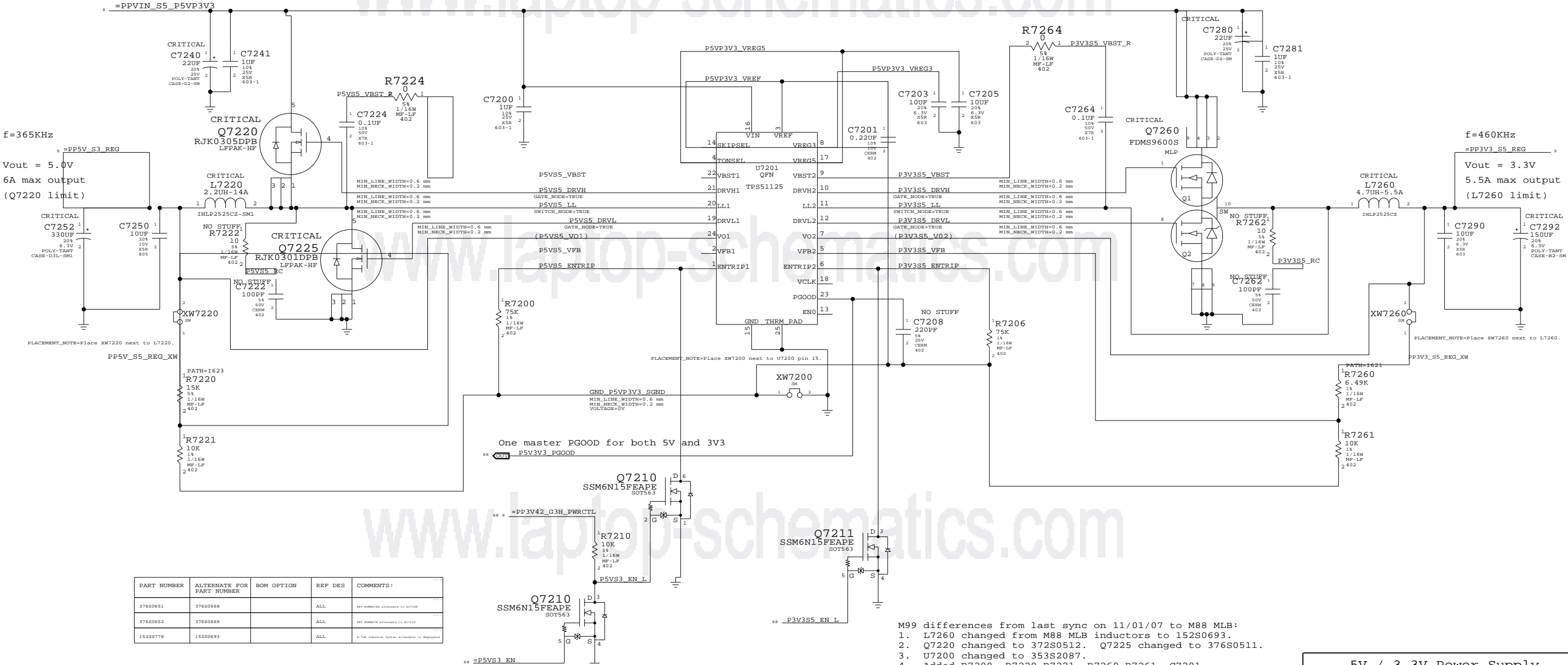
C

B

A

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1



5V / 3.3V Power Supply

SYNC_MASTER=M99_MLB SYNC_DATE=01/09/2008

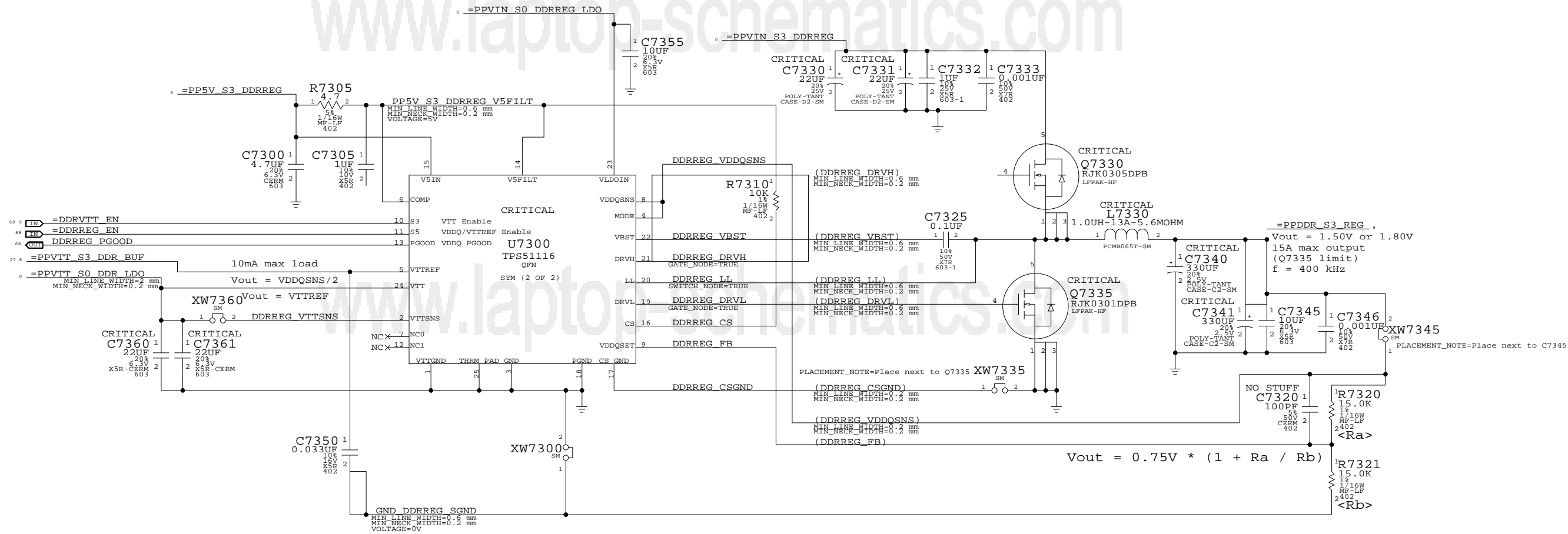
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1.5V DDR3 Supply

SYNC_MASTER=M99_MLB SYNC_DATE=12/13/2007

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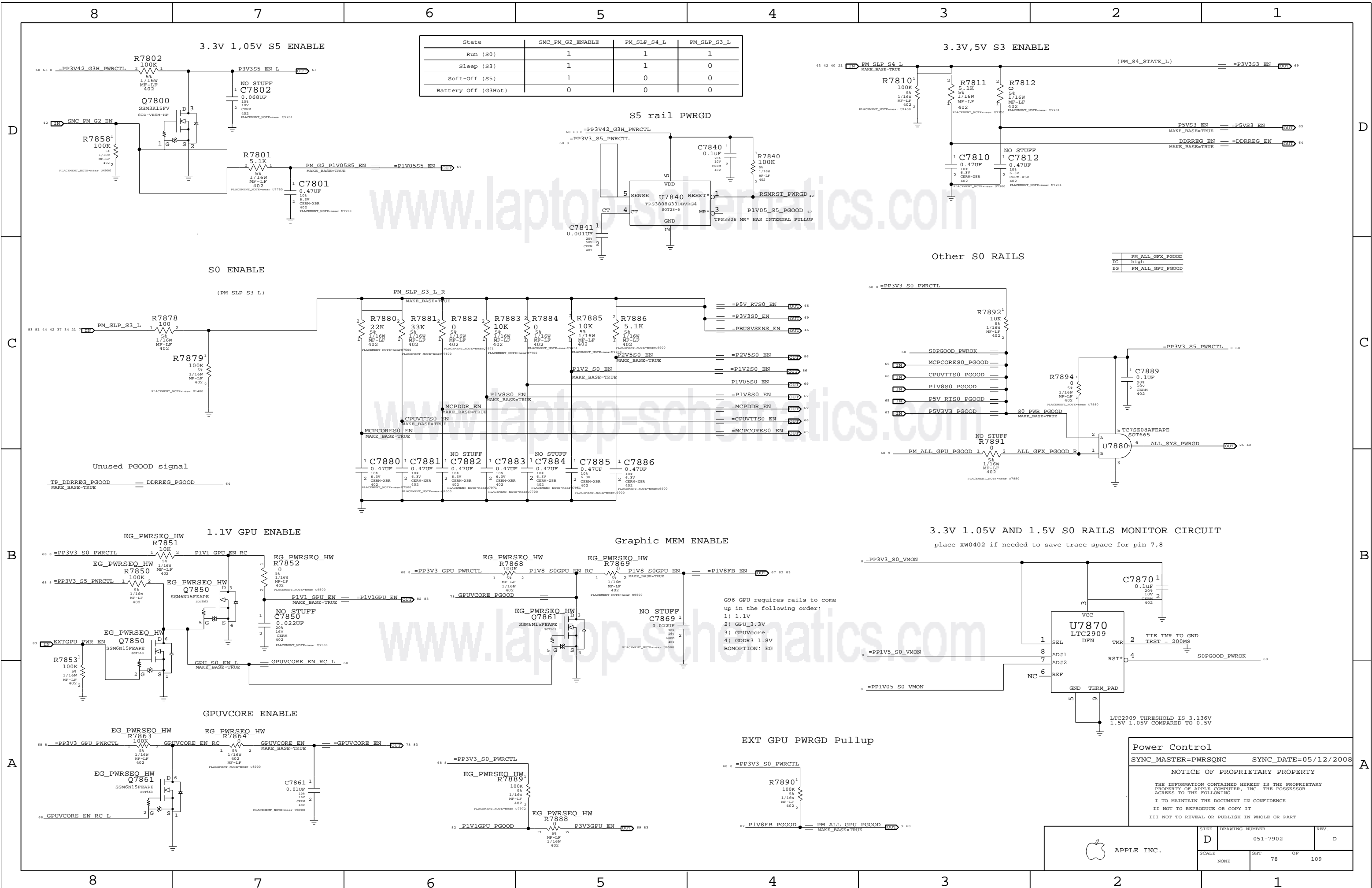
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

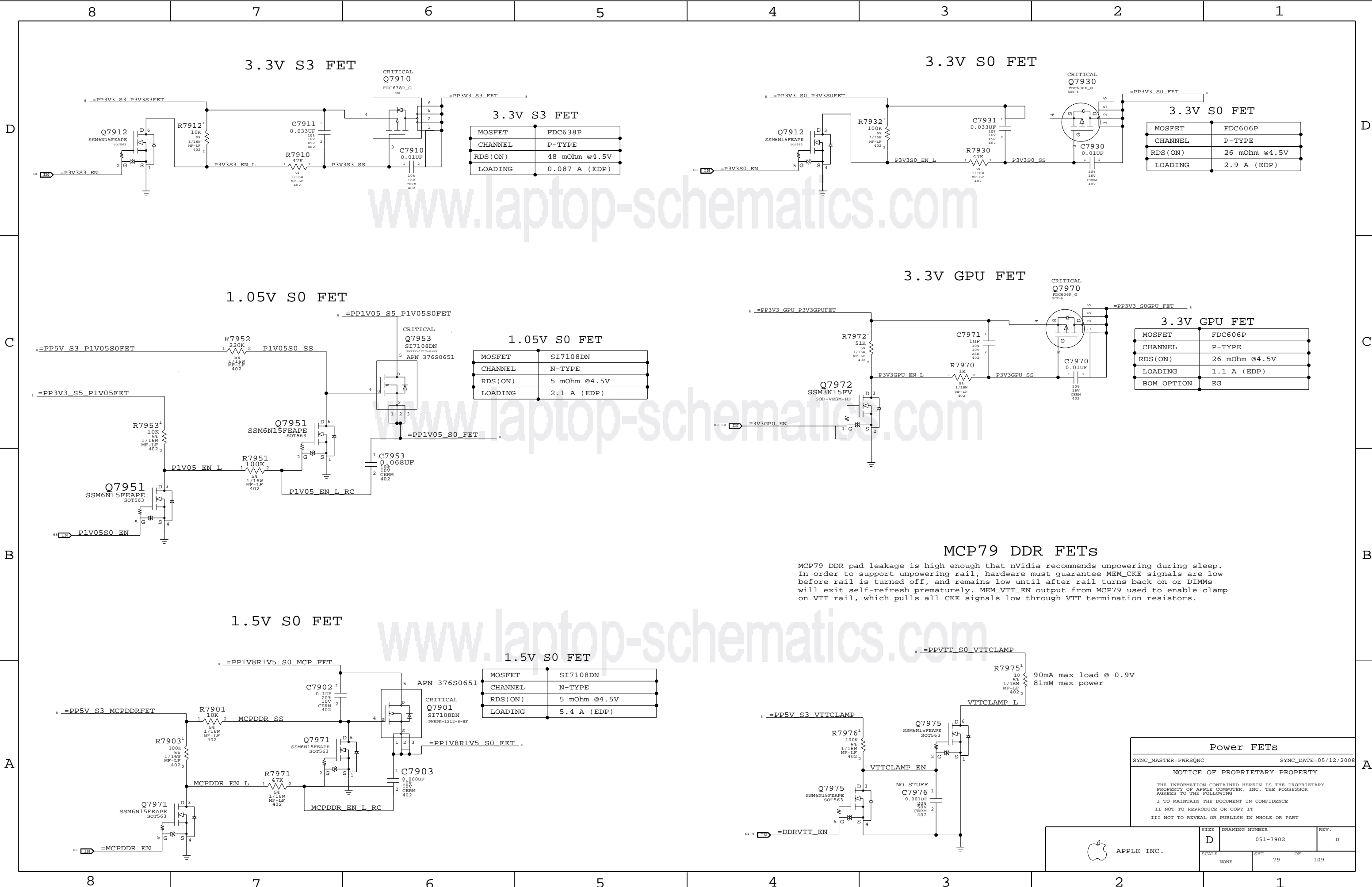


APPLE INC.

SIZE D DRAWING NUMBER 051-7902 REV. D

SCALE NONE SHT 73 OF 109





MCP79 DDR FETs

MCP79 DDR pad leakage is high enough that nVidia recommends unpowering during sleep. In order to support unpowering rail, hardware must guarantee MEM_CKE signals are low before rail is turned off, and remains low until after rail turns back on or DIMMs will exit self-refresh prematurely. MEM_VTT_EN output from MCP79 used to enable clamp on VTT rail, which pulls all CKE signals low through VTT termination resistors.

Power FETs

SYNC_MASTER=PWRSONC SYNC_DATE=05/12/2008

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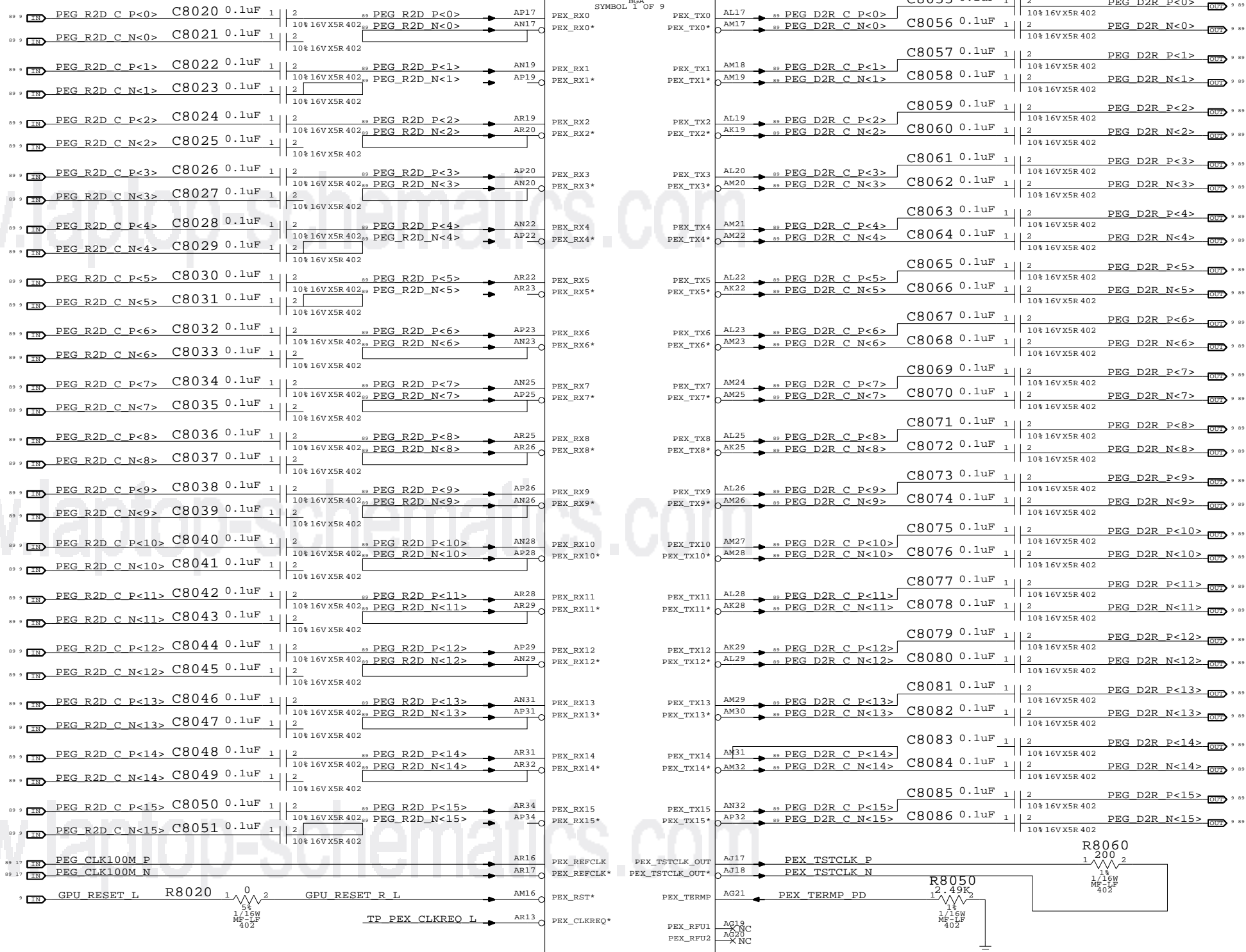
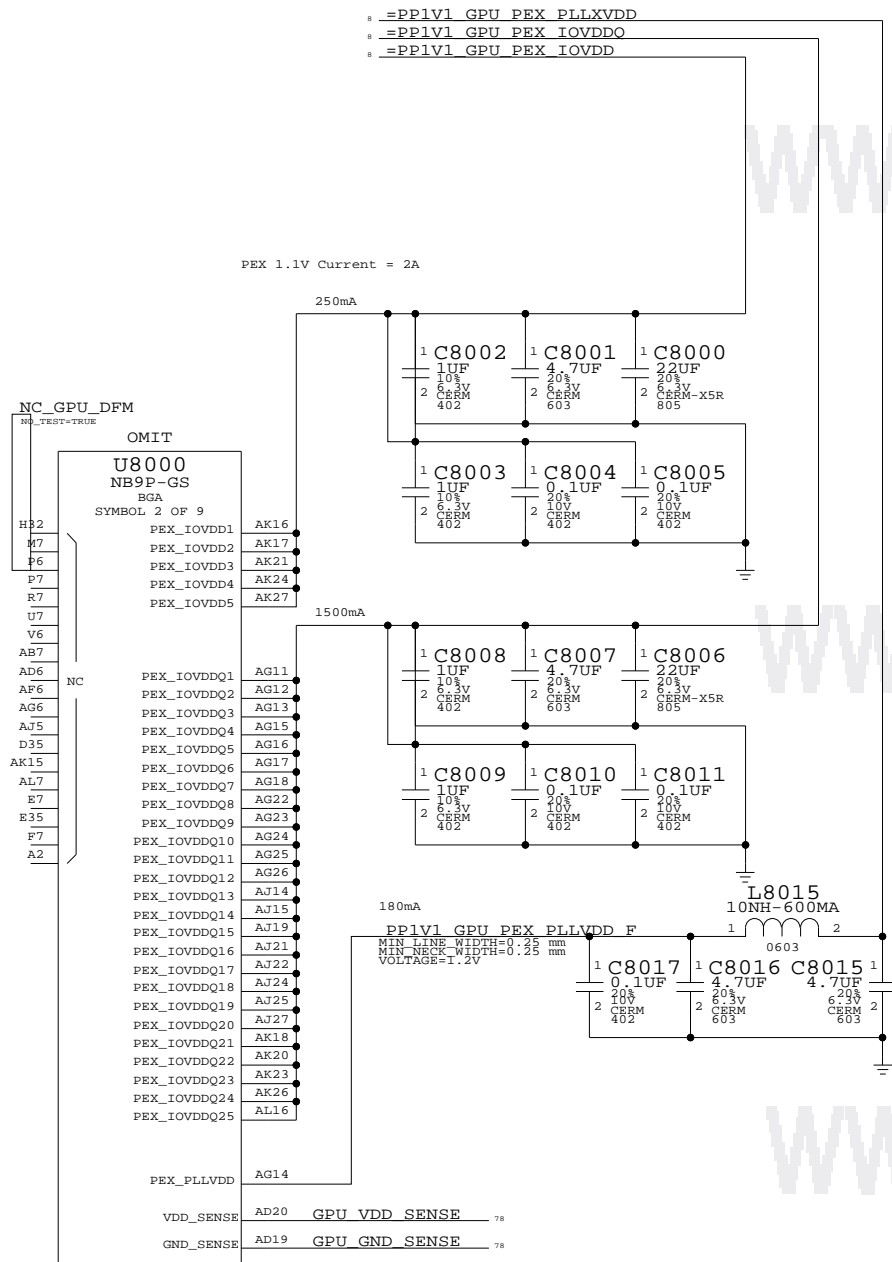
Page Notes

Power aliases required by this page:

```
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD
```

```
Signal aliases required by this page:
(NONE)
```

BOM options provided by this page:
(NONE)



NV G96 PCI-E

```

SYNC_MASTER=MUXGFX

```

SYNC_DATE=07/10/2008

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	Q322	EDWARDS AUBREY
--	------	----------------

SIZE	DRAWING NUMBER
D	251-5000



APPLE INC.

SIZE

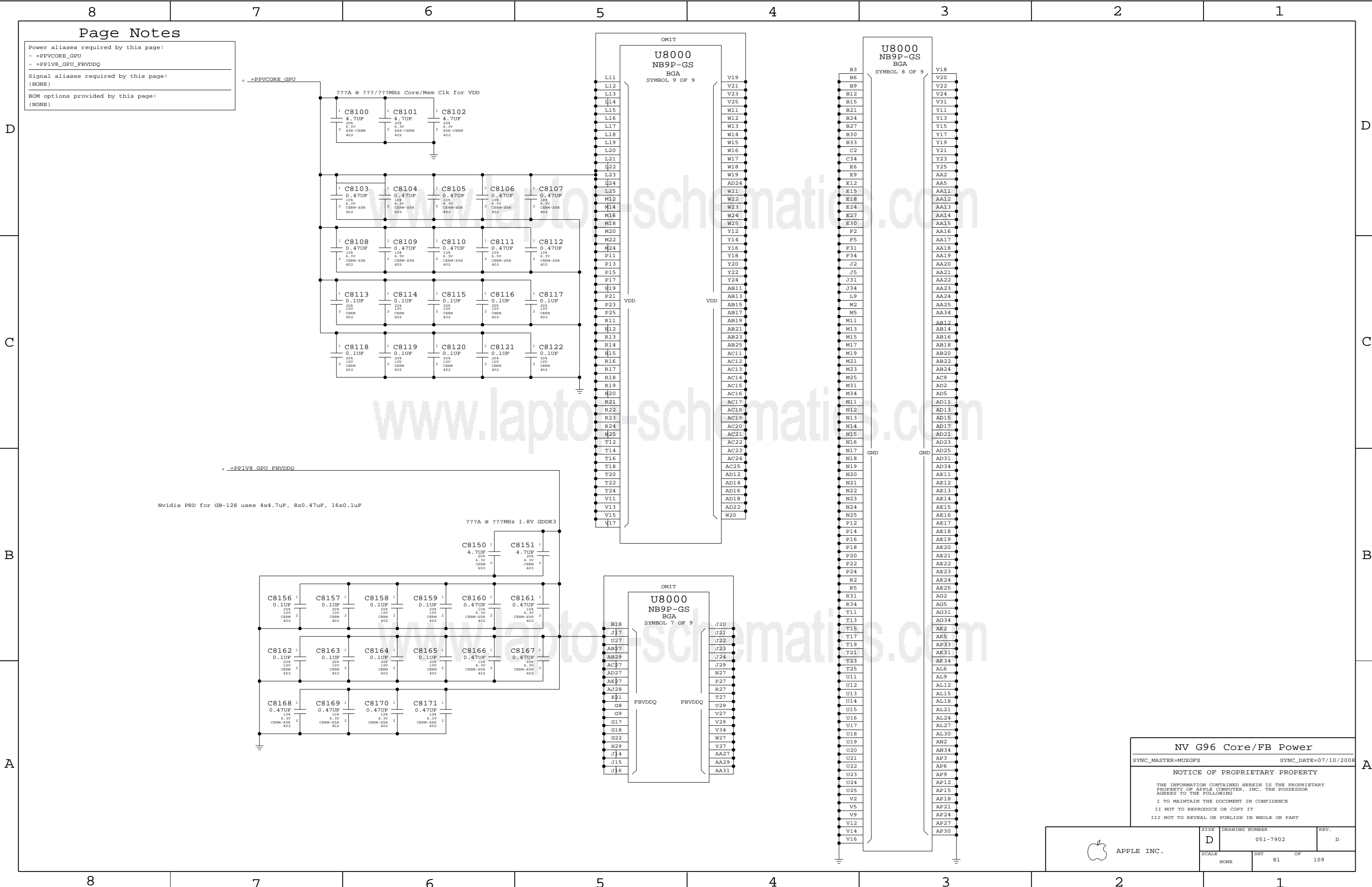
DRAWING NUMBER

REV.

SCALE	

SHT

--	--



Page Notes

Power aliases required by this page:

- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

NV G96 Core/FB Power

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

NOTICE OF PROPRIETARY PROPERTY

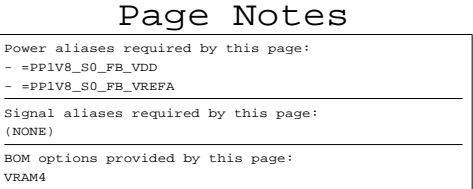
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7902	D
SCALE		SHT	OF
NONE		81	109



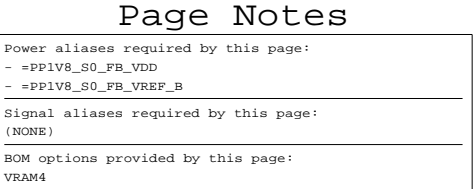
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8

7

6

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4

3

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1

Page Notes

Power aliases required by this page:

- =PP3V3_GPU_VDD33
- =PP3V3_GPU_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:

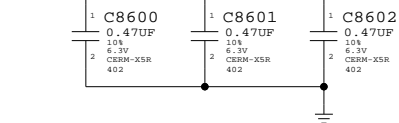
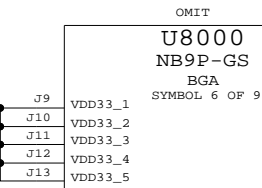
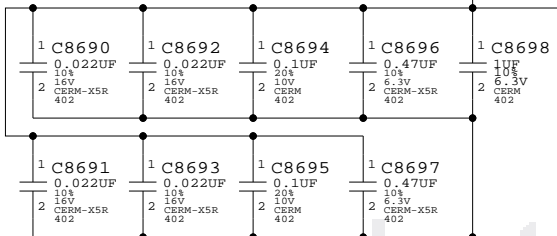
(NONE)

BOM options provided by this page:

(NONE)

76 75 8 6 =PP3V3_GPU_VDD33

Typically <??mA

110mA
76 75 8 6 =PP3V3_GPU_VDD33

NC

NC

AK14

K9

C3

D4

D3

C4

ROM_CS*

ROM_SCLK

ROM_SI

ROM_SO

GPU_ROM_CS_L

GPU_ROM_SCLK

GPU_ROM_SI

GPU_ROM_SO

GPU_STRAP_REF_3V3_PD

GPU_STRAP_REF_MIOB_PD

STRAP_REF_3V3

STRAP_REF_MIOB

(IPD)

MIOA_VDDQ_1

MIOA_VDDQ_2

MIOA_VDDQ_3

MIOA_VDDQ_4

MIOB_VDDQ_1

MIOB_VDDQ_2

MIOB_VDDQ_3

MIOB_VDDQ_4

GPU_TESTMODE_PD

GPU_MIOA_VREF

MIOB_VREF

GPU_MIOA_PD_VDDQ

GPU_MIOA_PU_GND

GPU_MIOB_PD_VDDQ

GPU_MIOB_PU_GND

SP_PLLVDD

PLLVDD

VID_PLLVDD

XTAL_IN

XTAL_OUT

XTAL_OUTBUFF

XTAL_SSIN

GPU_XTALIN

GPU_XTALOUT

GPU_XTALOUTBUFF

GPU_XTALSSIN

GPU_XTALIN

GPU_XTALOUT

GPU_XTALOUTBUFF

GPU_XTALSSIN

GPU_XTALIN

GPU_XTALOUT

GPU_XTALOUTBUFF

GPU_XTALSSIN

GPU_XTALIN

GPU_XTALOUT

GPU_XTALOUTBUFF

GPU_XTALSSIN

GPU_XTALIN

GPU_XTALOUT

GPU_XTALOUTBUFF

GPU_XTALSSIN

GPU_XTALIN

GPU_XTALOUT

GPU_XTALOUTBUFF

GPU_XTALSSIN

GPU_XTALIN

GPU_XTALOUT

GPU_XTALOUTBUFF

GPU_XTALSSIN

GPU_XTALIN

GPU_XTALOUT

GPU_XTALOUTBUFF

GPU_XTALSSIN

GPU_XTALIN

GPU_XTALOUT

GPU_XTALOUTBUFF

GPU_XTALSSIN

GPU_XTALIN

GPU_XTALOUT

GPU_XTALOUTBUFF

GPU_XTALSSIN

U8000
NB9P-GS
BGA
SYMBOL 6 OF 9

VDD33_1

VDD33_2

VDD33_3

VDD33_4

VDD33_5

RFU0

RFU1

RFU0_GND

RFU1_GND

ROM_CS*

ROM_SCLK

ROM_SI

ROM_SO

STRAP_REF_3V3

STRAP_REF_MIOB

(IPD)

MIOA_VDDQ_1

MIOA_VDDQ_2

MIOA_VDDQ_3

MIOA_VDDQ_4

MIOB_VDDQ_1

MIOB_VDDQ_2

MIOB_VDDQ_3

MIOB_VDDQ_4

TESTMODE

MIOA_VREF

MIOB_VREF

MIOA_CAL_PD_VDDQ

MIOA_CAL_PU_GND

MIOB_CAL_PD_VDDQ

MIOB_CAL_PU_GND

TP_GPU_BUFRST_L

GPU_JTAG_TCK

GPU_JTAG_TDI

GPU_JTAG_TDO

GPU_JTAG_TMS

GPU_JTAG_TRST_L

GPU_MIOA_CLKIN

GPU_MIOA_CLKOUT_P

GPU_MIOA_CLKOUT_N

GPU_MIOA_CTL3

GPU_MIOA_DE

GPU_MIOA_D<0>

GPU_MIOA_D<1>

GPU_MIOA_D<2>

GPU_MIOA_D<3>

GPU_MIOA_D<4>

GPU_MIOA_D<5>

GPU_MIOA_D<6>

GPU_MIOA_D<7>

GPU_MIOA_D<8>

GPU_MIOA_D<9>

GPU_MIOA_D<10>

GPU_MIOA_D<11>

GPU_MIOA_D<12>

GPU_MIOA_D<13>

GPU_MIOA_D<14>

GPU_MIOA_HSYNC

GPU_MIOA_VSYNC

GPU_MIOB_CLKIN

GPU_MIOB_CLKOUT_P

GPU_MIOB_CLKOUT_N

GPU_MIOB_CTL3

GPU_MIOB_DE

GPU_MIOB_D<0>

GPU_MIOB_D<1>

GPU_MIOB_D<2>

GPU_MIOB_D<3>

GPU_MIOB_D<4>

GPU_MIOB_D<5>

GPU_MIOB_D<6>

GPU_MIOB_D<7>

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GPU_MIOB_D<11>

GPU_MIOB_D<12>

GPU_MIOB_D<13>

GPU_MIOB_D<14>

GPU_STRAP<0>

GPU_STRAP<1>

GPU_STRAP<2>

GPU_MIOB_HSYNC

GPU_MIOB_VSYNC

GPU_THERMD_P

GPU_THERMD_N

TP_GPU_PGOOD_OUT_L

TP_GPU_PGOOD_OUT_L

TP_GPU_PGOOD_OUT_L

TP_GPU_PGOOD_OUT_L

NV G96 GPIO/MIO/Misc

SYNC_MASTER=MUXGFX

SYNC_DATE=07/10/2008

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APPLE INC.

SIZE

DRAWING NUMBER

REV.

D

051-7902

D

SCALE

SHT

OF

109

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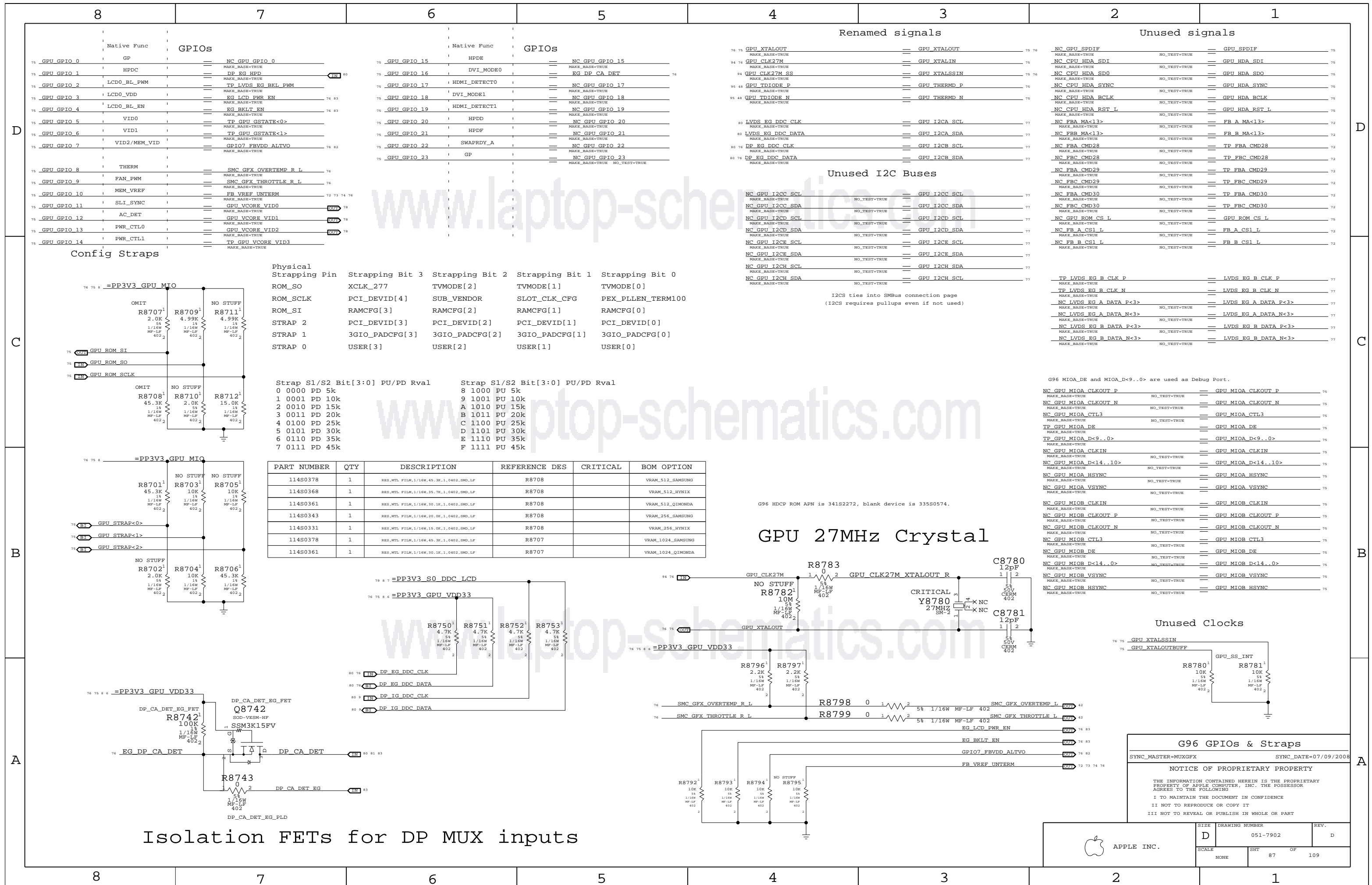
5

4

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2

1



Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IPFX
- =PP3V3_GPU_IPPCD_IOVDD

Signal aliases required by this page:
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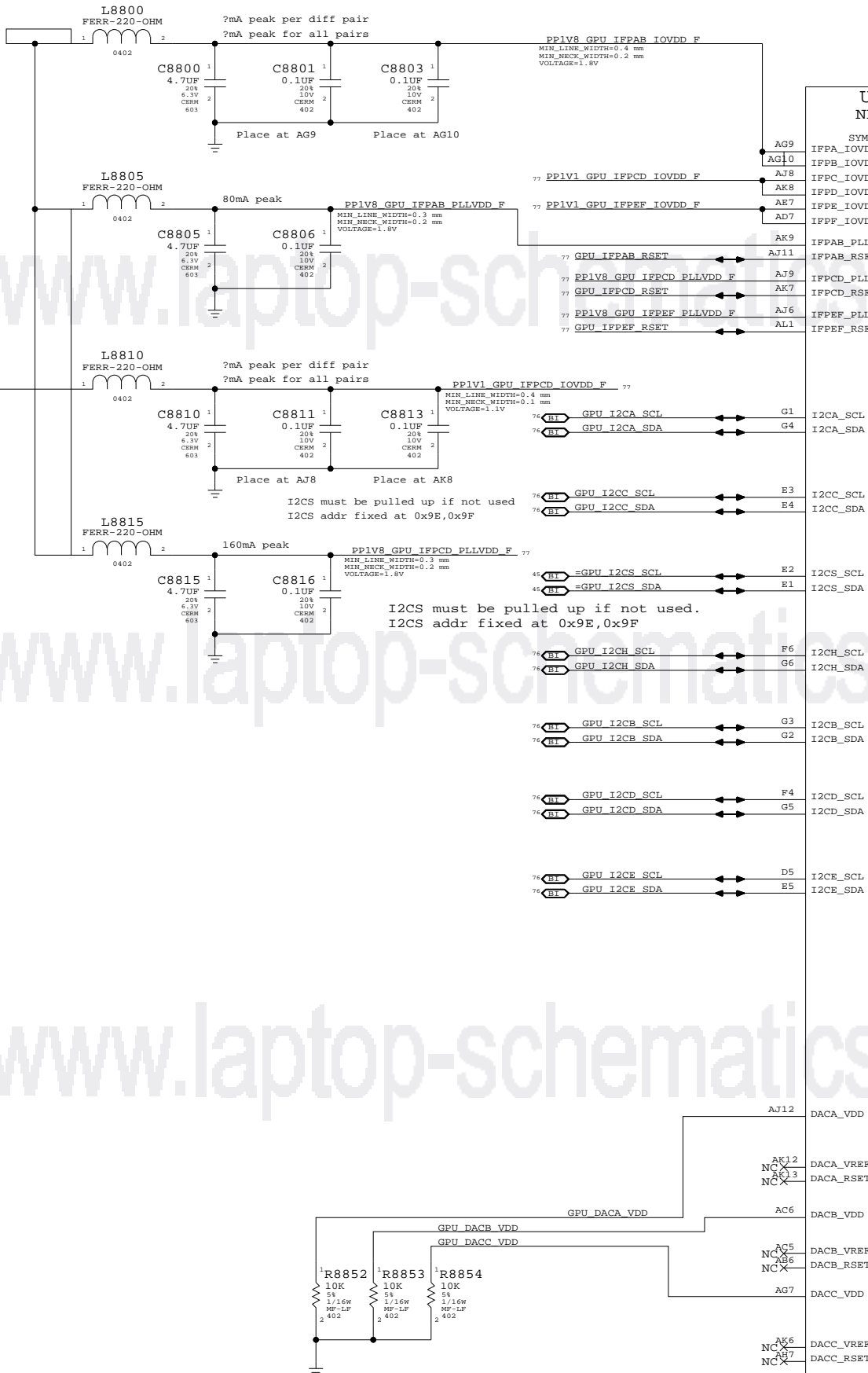
BOM options provided by this page:
(NONE)

Sum of peak currents: 240mA

=PP1V8_GPU_IPFX

=PP1V1_GPU_IPPCD_IOVDD

Power inputs must be pulled down if not used



U8000

NB9P-GS

BGA

SYMBOL 5 OF 9

IFPA_TXC

IFPA_TXC*

IFPA_TXD0

IFPA_TXD0*

IFPA_TXD1

IFPA_TXD1*

IFPA_TXD2

IFPA_TXD2*

IFPA_TXD3

IFPA_TXD3*

IFPB_TXC

IFPB_TXC*

IFPB_TXD4

IFPB_TXD4*

IFPB_TXD5

IFPB_TXD5*

IFPB_TXD6

IFPB_TXD6*

IFPB_TXD7

IFPB_TXD7*

IFPC_AUX

IFPC_AUX*

IFPC_L0

IFPC_L0*

IFPC_L1

IFPC_L1*

IFPC_L2

IFPC_L2*

IFPC_L3

IFPC_L3*

IFPD_AUX

IFPD_AUX*

IFPD_L0

IFPD_L0*

IFPD_L1

IFPD_L1*

IFPD_L2

IFPD_L2*

IFPD_L3

IFPD_L3*

IFPE_AUX

IFPE_AUX*

IFPE_L0

IFPE_L0*

IFPE_L1

IFPE_L1*

IFPE_L2

IFPE_L2*

IFPE_L3

IFPE_L3*

IFPF_AUX

IFPF_AUX*

IFPF_L0

IFPF_L0*

IFPF_L1

IFPF_L1*

IFPF_L2

IFPF_L2*

IFPF_L3

IFPF_L3*

DACA_RED

DACA_GREEN

DACA_BLUE

DACA_HSYNC

DACA_VSYNC

DACA_VREF

DACA_RSET

DACB_RED

DACB_GREEN

DACB_BLUE

DACB_HSYNC

DACB_VSYNC

DACB_VREF

DACB_RSET

DACC_RED

DACC_GREEN

DACC_BLUE

DACC_HSYNC

DACC_VSYNC

DACC_VREF

DACC_RSET

NV G96 Video Interfaces

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

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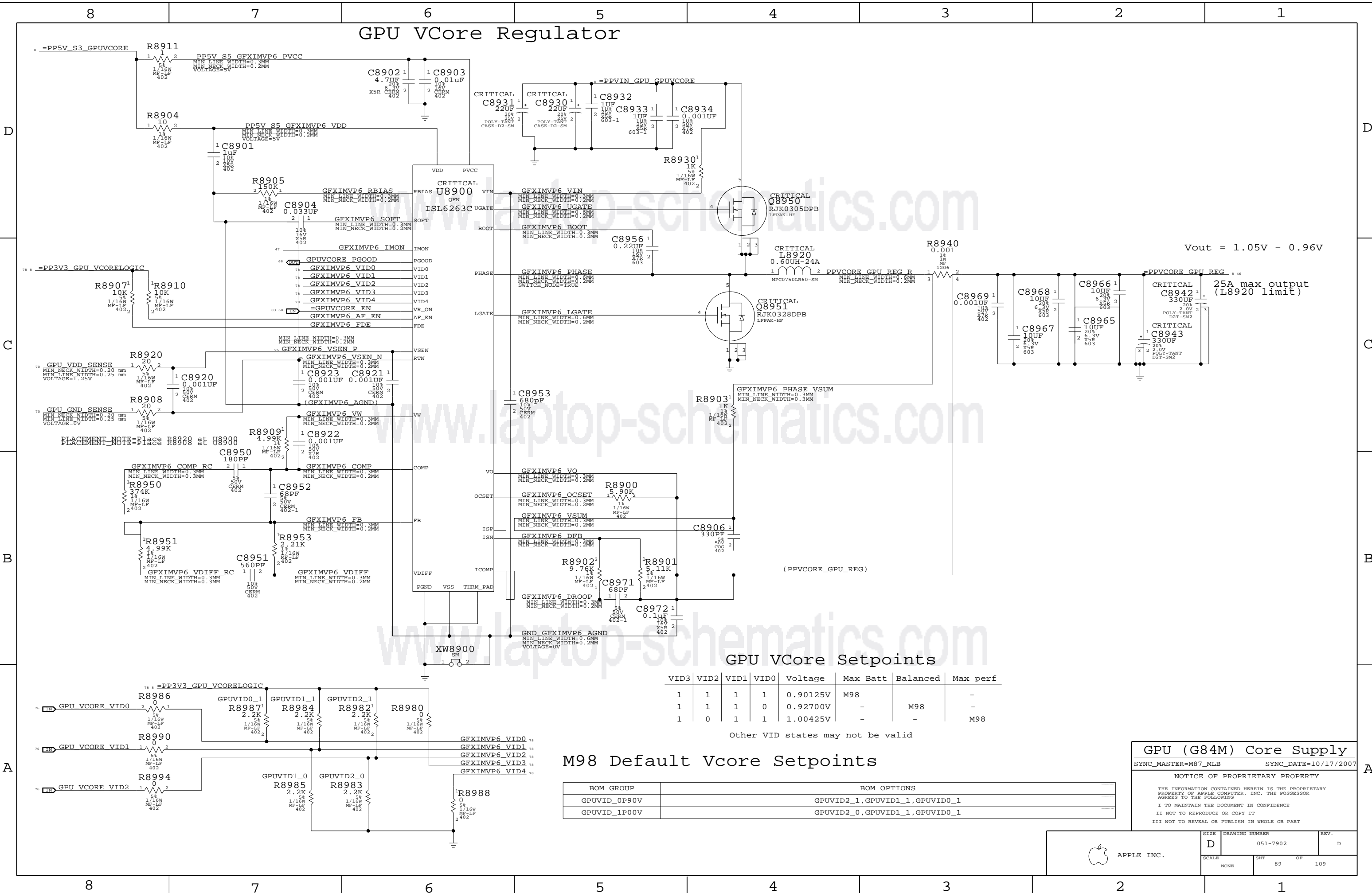
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APPLE INC.

SIZE D DRAWING NUMBER 051-7902 REV. D

SCALE NONE SHT 88 OF 109



Other VID states may not be valid

BOM GROUP	BOM OPTIONS
GPUVID_0P90V	GPUVID2_1,GPUVID1_1,GPUVID0_1
GPUVID_1P00V	GPUVID2_0,GPUVID1_1,GPUVID0_1

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

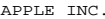
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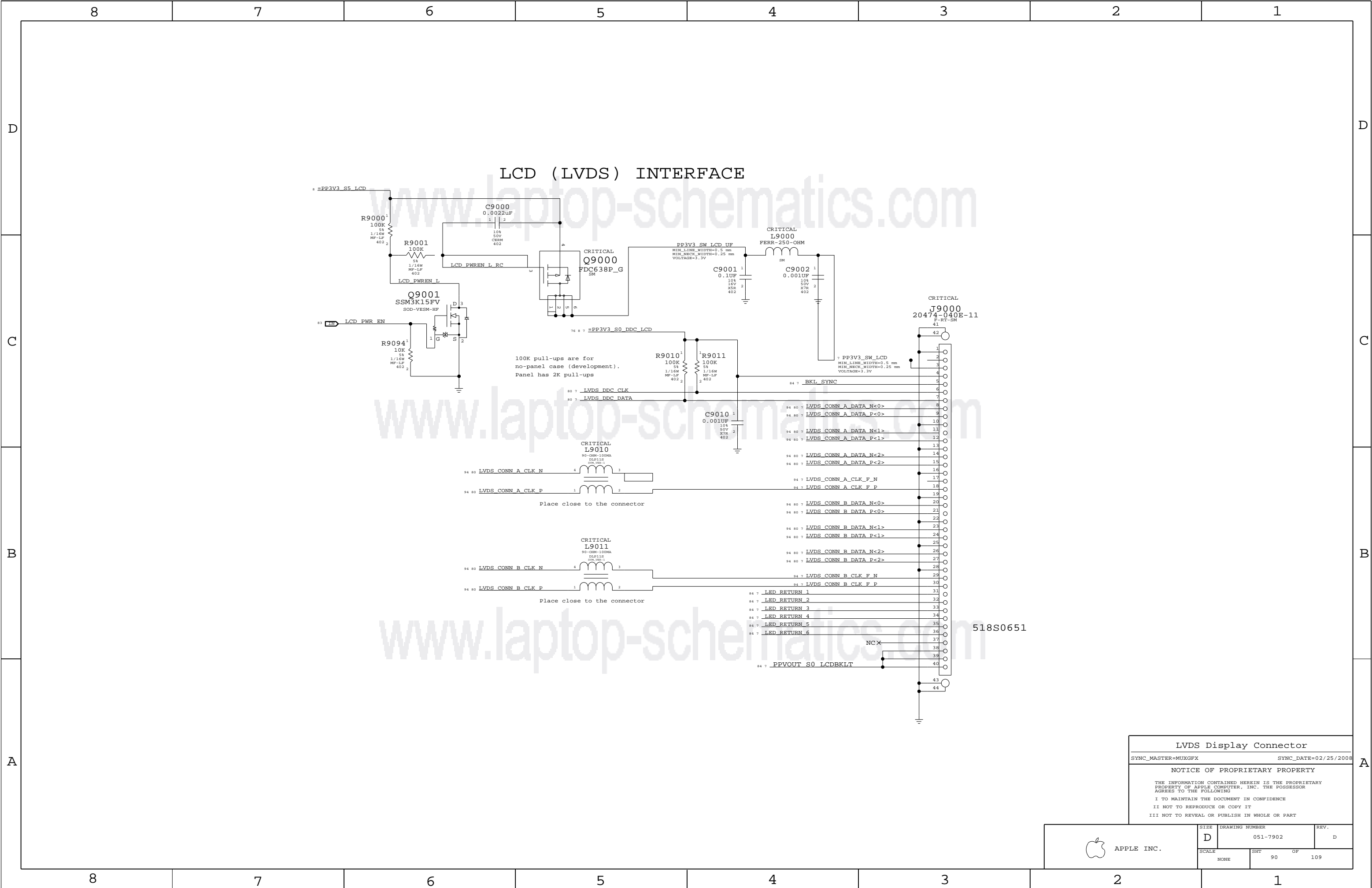
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SIZE	DRAWING NUMBER	REV.
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D	051-7902
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SCALE	SH1	OF
NONE	89	109



LVDS Display Connector	
SYNC_MASTER=MUXGFX	SYNC_DATE=02/25/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7902	D
SCALE		SHT	OF
NONE		90	109

D

C

B

A

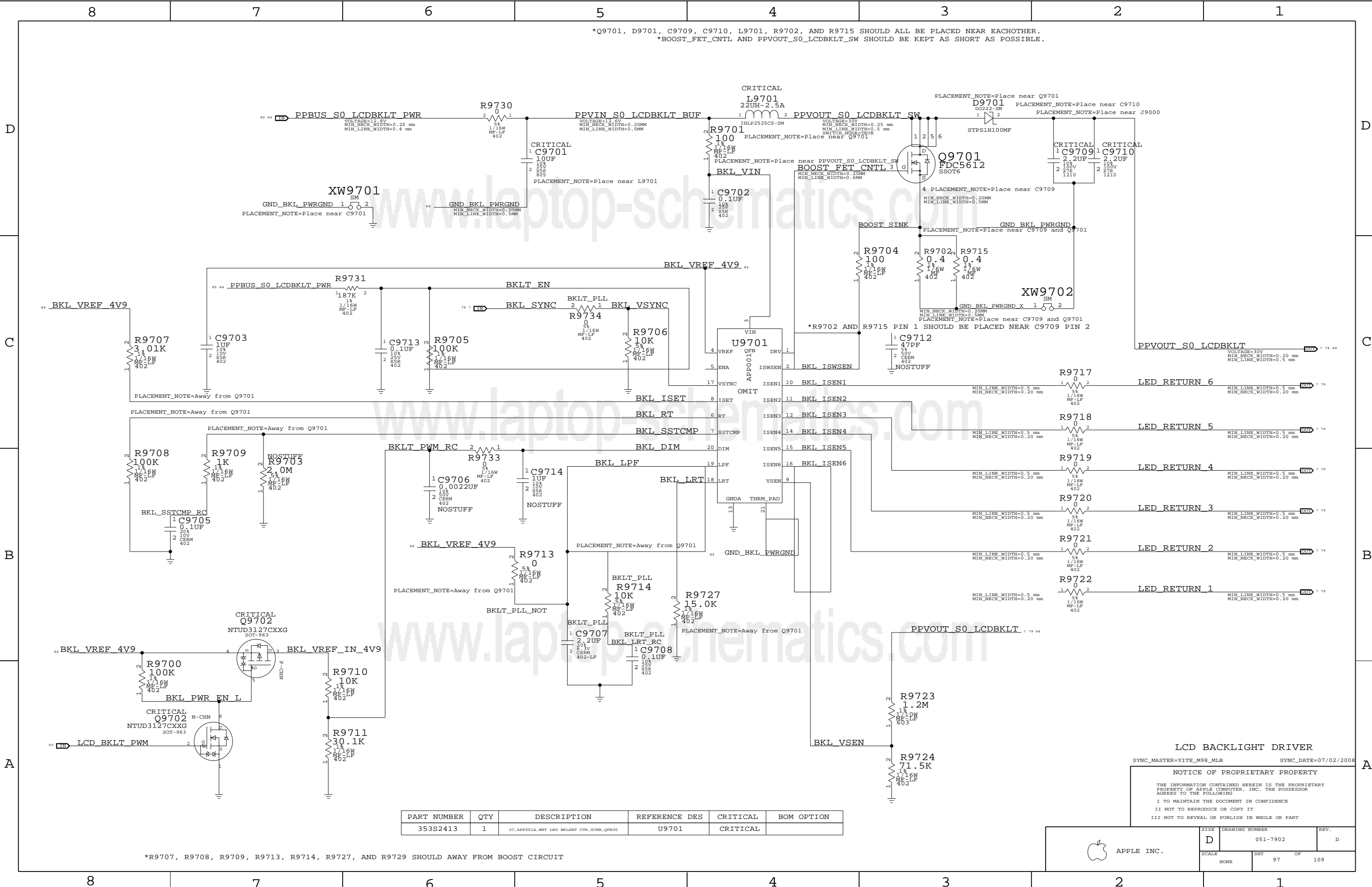
D



B



SIZE D	DRAWING NUMBER 051-7902	REV. D
SCALE NONE	SHT 93	OF 109



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2413	1	IC,APP001A,WHIT LED BRIGHT CTR,SCRN,Q9720	U9701	CRITICAL	

LCD BACKLIGHT DRIVER

SYNC_MASTER=YITE_M98_MLB SYNC_DATE=07/02/2008

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APPLE INC.

SIZE D

DRAWING NUMBER 051-7902

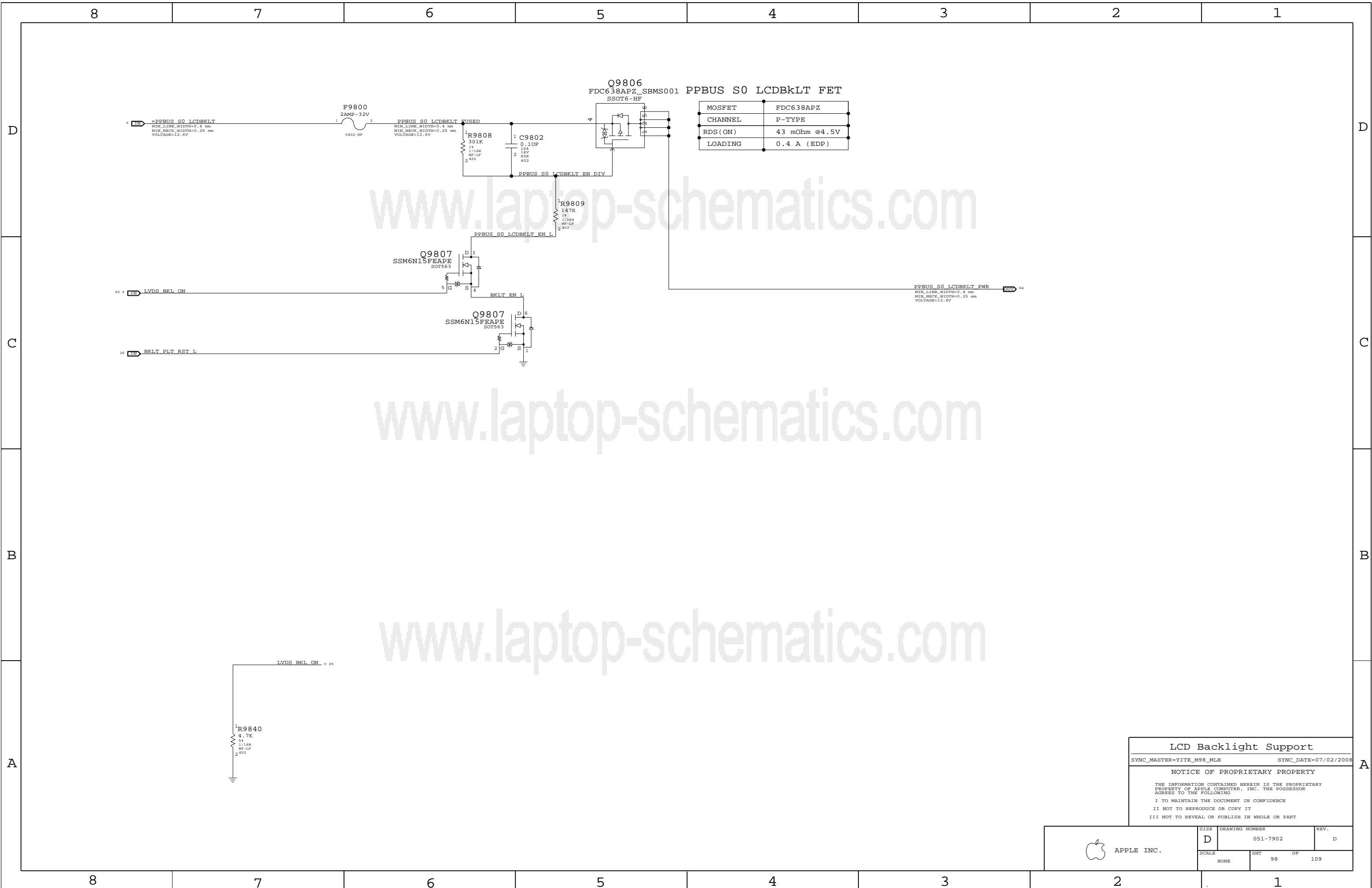
REV. D

SCALE NONE

SHT 97

OF 109

*R9707, R9708, R9709, R9713, R9714, R9727, AND R9729 SHOULD AWAY FROM BOOST CIRCUIT





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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_20THER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM_*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM A CLK P<5..0>	15 28
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM A CLK N<5..0>	15 28
MEM_A_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM A CKE<3..0>	15 28
MEM_A_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM A CS_L<3..0>	15 28
MEM_A_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM A ODT<3..0>	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A A<14..0>	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A BA<2..0>	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A RAS_L	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A CAS_L	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A WE_L	15 28
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DQ<7..0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DQ<15..8>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DQ<23..16>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DQ<31..24>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DQ<39..32>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DQ<47..40>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DQ<55..48>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DQ<63..56>	15 28
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DM<0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DM<1>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DM<2>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DM<3>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DM<4>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DM<5>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DM<6>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DM<7>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS P<0>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS N<0>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS P<1>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS N<1>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS P<2>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS N<2>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS P<3>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS N<3>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS P<4>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS N<4>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS P<5>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS N<5>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS P<6>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS N<6>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS P<7>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS N<7>	15 28
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM B CLK P<5..0>	15 29
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM B CLK N<5..0>	15 29
MEM_B_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM B CKE<3..0>	15 29
MEM_B_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM B CS_L<3..0>	15 29
MEM_B_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM B ODT<3..0>	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B A<14..0>	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B BA<2..0>	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B RAS_L	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B CAS_L	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B WE_L	15 29
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DQ<7..0>	15 29
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DQ<15..8>	15 29
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DQ<23..16>	15 29
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DQ<31..24>	15 29
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DQ<39..32>	15 29
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DQ<47..40>	15 29
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DQ<55..48>	15 29
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DQ<63..56>	15 29
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DM<0>	15 29
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DM<1>	15 29
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DM<2>	15 29
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DM<3>	15 29
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DM<4>	15 29
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DM<5>	15 29
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DM<6>	15 29
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DM<7>	15 29
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS P<0>	15 29
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS N<0>	15 29
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS P<1>	15 29
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS N<1>	15 29
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS P<2>	15 29
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS N<2>	15 29
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS P<3>	15 29
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS N<3>	15 29
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS P<4>	15 29
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS N<4>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS P<5>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS N<5>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS P<6>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS N<6>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS P<7>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS N<7>	15 29
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP VDD	16
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP GND	16

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Memory Constraints

SYNC_MASTER=MUXGFX

SYNC_DATE=02/18/2008

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SIZE D

DRAWING NUMBER 051-7902

REV. D

SCALE NONE

SHT 101

OF 109

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	13.1 MM	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	=4:1_SPACING	?
CRT_2CRT	*	=STANDARD	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	16 MIL	?
MCP_DAC_COMP	*	=2:1_SPACING	?

CRT signal single-ended impedance varies by location:
- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).
R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.1 & 2.5.2.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3X_DIELECTRIC	?
LVDS	*	=3X_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length. DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps. DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals. Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4X_DIELECTRIC	?
SATA_TERM	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

NET_TYPE

ELECTRICAL_CONSTRAINT_SET

PHYSICAL

SPACING

PEG_R2D

PCIE_90D

PCIE

PEG_R2D P<15..0>

70

PEG_R2D

PCIE_90D

PCIE

PEG_R2D N<15..0>

70

PEG_R2D

PCIE_90D

PCIE

PEG_R2D C P<15..0>

9 70

PEG_R2D

PCIE_90D

PCIE

PEG_R2D C N<15..0>

9 70

PEG_D2R

PCIE_90D

PCIE

PEG_D2R P<15..0>

9 70

PEG_D2R

PCIE_90D

PCIE

PEG_D2R N<15..0>

9 70

PEG_D2R

PCIE_90D

PCIE

PEG_D2R C P<15..0>

70

PEG_D2R

PCIE_90D

PCIE

PEG_D2R C N<15..0>

70

PCIE_MINI_R2D_P

PCIE_90D

PCIE

PCIE MINI_R2D_P

31 95

PCIE_MINI_R2D_N

PCIE_90D

PCIE

PCIE MINI_R2D_N

31 95

PCIE_MINI_R2D_C_P

PCIE_90D

PCIE

PCIE MINI_R2D_C_P

17 31

PCIE_MINI_R2D_C_N

PCIE_90D

PCIE

PCIE MINI_R2D_C_N

17 31

PCIE_MINI_D2R_P

PCIE_90D

PCIE

PCIE MINI_D2R_P

17 31

PCIE_MINI_D2R_N

PCIE_90D

PCIE

PCIE MINI_D2R_N

17 31

PCIE_FW_R2D_P

PCIE_90D

PCIE

PCIE FW_R2D_P

36

PCIE_FW_R2D_N

PCIE_90D

PCIE

PCIE FW_R2D_N

36

PCIE_FW_R2D_C_P

PCIE_90D

PCIE

PCIE FW_R2D_C_P

17 36

PCIE_FW_R2D_C_N

PCIE_90D

PCIE

PCIE FW_R2D_C_N

17 36

PCIE_FW_D2R_P

PCIE_90D

PCIE

PCIE FW_D2R_P

17 36

PCIE_FW_D2R_N

PCIE_90D

PCIE

PCIE FW_D2R_N

17 36

PCIE_FW_D2R_C_P

PCIE_90D

PCIE

PCIE FW_D2R_C_P

36

PCIE_FW_D2R_C_N

PCIE_90D

PCIE

PCIE FW_D2R_C_N

36

PCIE_EXCARD_R2D_P

PCIE_90D

PCIE

PCIE EXCARD_R2D_P

7 32 95

PCIE_EXCARD_R2D_N

PCIE_90D

PCIE

PCIE EXCARD_R2D_N

7 32 95

PCIE_EXCARD_R2D_C_P

PCIE_90D

PCIE

PCIE EXCARD_R2D_C_P

17 32

PCIE_EXCARD_R2D_C_N

PCIE_90D

PCIE

PCIE EXCARD_R2D_C_N

17 32

PCIE_EXCARD_D2R_P

PCIE_90D

PCIE

PCIE EXCARD_D2R_P

7 17 32

PCIE_EXCARD_D2R_N

PCIE_90D

PCIE

PCIE EXCARD_D2R_N

7 17 32

PEG_CLK100M_P

CLK_PCIE_100D

CLK_PCIE

PEG_CLK100M_P

17 70

PEG_CLK100M_N

CLK_PCIE_100D

CLK_PCIE

PEG_CLK100M_N

17 70

PCIE_CLK100M_MINI_P

CLK_PCIE_100D

CLK_PCIE

PCIE_CLK100M_MINI_P

17 31

PCIE_CLK100M_MINI_N

CLK_PCIE_100D

CLK_PCIE

PCIE_CLK100M_MINI_N

17 31

PCIE_CLK100M_FW_P

CLK_PCIE_100D

CLK_PCIE

PCIE_CLK100M_FW_P

17 36

PCIE_CLK100M_FW_N

CLK_PCIE_100D

CLK_PCIE

PCIE_CLK100M_FW_N

17 36

PCIE_CLK100M_EXCARD_P

CLK_PCIE_100D

CLK_PCIE

PCIE_CLK100M_EXCARD_P

17 32

PCIE_CLK100M_EXCARD_N

CLK_PCIE_100D

CLK_PCIE

PCIE_CLK100M_EXCARD_N

17 32

MCP_PEX_CLK_COMP

MCP_PEX_COMP

MCP_PEX_CLK_COMP

MCP_PEX_CLK_COMP

17

CRT_IG_R_C_PR

CRT_50S

CRT

CRT_IG_R_C_PR

18 25

CRT_IG_G_Y_Y

CRT_50S

CRT

CRT_IG_G_Y_Y

18 25

CRT_IG_B_COMP_PB

CRT_50S

CRT

CRT_IG_B_COMP_PB

18 25

CRT_IG_HSYNC

CRT_50S

CRT_SYNC

CRT_IG_HSYNC

18 25

CRT_IG_VSYNC

CRT_50S

CRT_SYNC

CRT_IG_VSYNC

18 25

MCP_TV_DAC_RSET

MCP_DAC_COMP

MCP_TV_DAC_RSET

MCP_TV_DAC_RSET

18 25

MCP_TV_DAC_VREF

MCP_DAC_COMP

MCP_TV_DAC_VREF

MCP_TV_DAC_VREF

18 25

TMDS_IG_TXC_P

DP_100D

DISPLAYPORT

TMDS_IG_TXC_P

TMDS_IG_TXC_N

DP_100D

DISPLAYPORT

TMDS_IG_TXC_N

TMDS_IG_TXD_P<2..0>

DP_100D

DISPLAYPORT

TMDS_IG_TXD_P<2..0>

TMDS_IG_TXD_N<2..0>

DP_100D

DISPLAYPORT

TMDS_IG_TXD_N<2..0>

DP_IG_ML_P<3..0>

DP_100D

DISPLAYPORT

DP_IG_ML_P<3..0>

9 80

DP_IG_ML_N<3..0>

DP_100D

DISPLAYPORT

DP_IG_ML_N<3..0>

9 80

DP_IG_AUX_CH_P

DP_100D

DISPLAYPORT

DP_IG_AUX_CH_P

18 80

DP_IG_AUX_CH_N

DP_100D

DISPLAYPORT

DP_IG_AUX_CH_N

18 80

MCP_HDMI_RSET

MCP_DV_COMP

MCP_HDMI_RSET

MCP_HDMI_RSET

18 25

MCP_HDMI_VPROBE

MCP_DV_COMP

MCP_HDMI_VPROBE

MCP_HDMI_VPROBE

18 25

LVDS_IG_A_CLK_P

LVDS_100D

LVDS

LVDS_IG_A_CLK_P

18 83

LVDS_IG_A_CLK_N

LVDS_100D

LVDS

LVDS_IG_A_CLK_N

18 83

LVDS_IG_A_DATA_P<2..0>

LVDS_100D

LVDS

LVDS_IG_A_DATA_P<2..0>

18 83

LVDS_IG_A_DATA_N<2..0>

LVDS_100D

LVDS

LVDS_IG_A_DATA_N<2..0>

18 83

LVDS_IG_A_DATA_P<3>

LVDS_100D

LVDS

LVDS_IG_A_DATA_P<3>

9 18

LVDS_IG_A_DATA_N<3>

LVDS_100D

LVDS

LVDS_IG_A_DATA_N<3>

9 18

LVDS_IG_B_CLK_P

LVDS_100D

LVDS

LVDS_IG_B_CLK_P

9 18

LVDS_IG_B_CLK_N

LVDS_100D

LVDS

LVDS_IG_B_CLK_N

9 18

LVDS_IG_B_DATA_P<2..0>

LVDS_100D

LVDS

LVDS_IG_B_DATA_P<2..0>

18 83

LVDS_IG_B_DATA_N<2..0>

LVDS_100D

LVDS

LVDS_IG_B_DATA_N<2..0>

18 83

LVDS_IG_B_DATA_P<3>

LVDS_100D

LVDS

LVDS_IG_B_DATA_P<3>

9 18

LVDS_IG_B_DATA_N<3>

LVDS_100D

LVDS

LVDS_IG_B_DATA_N<3>

9 18

MCP_IFPAB_RSET

MCP_DV_COMP

MCP_IFPAB_RSET

MCP_IFPAB_RSET

18 25

MCP_IFPAB_VPROBE

MCP_DV_COMP

MCP_IFPAB_VPROBE

MCP_IFPAB_VPROBE

18 25

SATA_HDD_R2D_C_P

SATA_100D

SATA

SATA_HDD_R2D_C_P

20 39

SATA_HDD_R2D_C_N

SATA_100D

SATA

SATA_HDD_R2D_C_N

20 39

SATA_HDD_R2D_P

SATA_100D

SATA

SATA_HDD_R2D_P

39

SATA_HDD_R2D_N

SATA_100D

SATA

SATA_HDD_R2D_N

39

SATA_HDD_D2R_P

SATA_100D

SATA

SATA_HDD_D2R_P

20 39

SATA_HDD_D2R_N

SATA_100D

SATA

SATA_HDD_D2R_N

20 39

SATA_HDD_D2R_C_P

SATA_100D

SATA

SATA_HDD_D2R_C_P

39

SATA_HDD_D2R_C_N

SATA_100D

SATA

SATA_HDD_D2R_C_N

39

SATA_ODD_R2D_C_P

SATA_100D

SATA

SATA_ODD_R2D_C_P

20 39

SATA_ODD_R2D_C_N

SATA_100D

SATA

SATA_ODD_R2D_C_N

20 39

SATA_ODD_R2D_P

SATA_100D

SATA

SATA_ODD_R2D_P

7 39

SATA_ODD_R2D_N

SATA_100D

SATA

SATA_ODD_R2D_N

7 39

SATA_ODD_D2R_P

SATA_100D

SATA

SATA_ODD_D2R_P

20 39

SATA_ODD_D2R_N

SATA_100D

SATA

SATA_ODD_D2R_N

20 39

SATA_ODD_D2R_C_P

SATA_100D

SATA

SATA_ODD_D2R_C_P

7 39

SATA_ODD_D2R_C_N

SATA_100D

SATA

SATA_ODD_D2R_C_N

7 39

MCP_SATA_TERM

SATA_TERM

MCP_SATA_TERM

MCP_SATA_TERM

20

MCP Constraints 1

SYNC_MASTER=MUXGFX

SYNC_DATE=02/18/2008

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SCALE

NONE

SHT

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OF

109

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2

1

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIA5	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?	USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints


PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

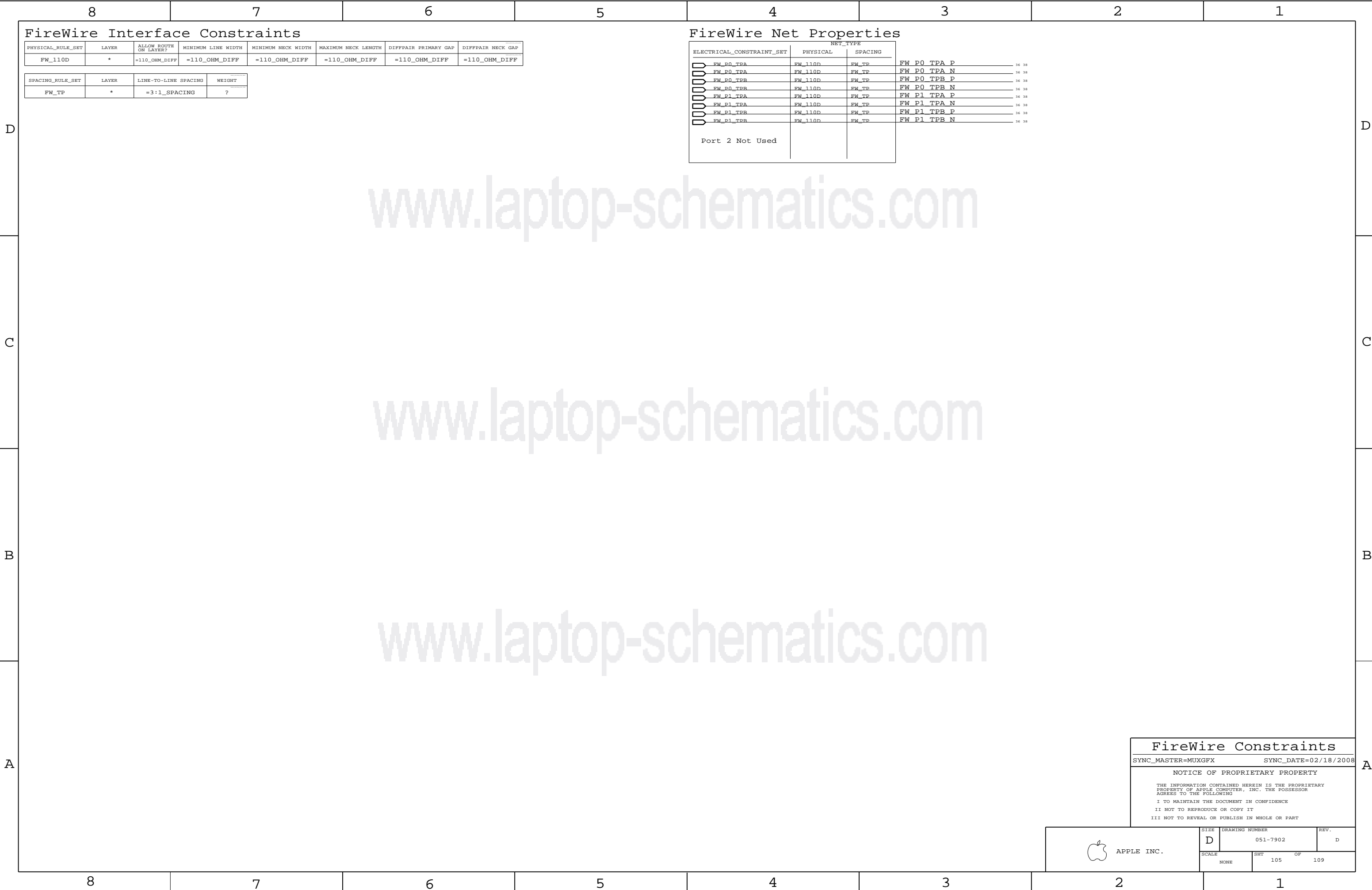
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

ELECTRICAL_CONSTRAINT_SFT		NET_TYPE		
		PHYSICAL	SPACING	
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7..0>	13 19
PCI_AD	PCI_55S	PCI	PCI_AD<23..8>	
PCI_AD24	PCI_55S	PCI	PCI_AD<24>	
PCI_AD	PCI_55S	PCI	PCI_AD<31..25>	
PCI_AD	PCI_55S	PCI	PCI_PAR	
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>	
PCI_CNTRL	PCI_55S	PCI	PCI_IRDY_L	
PCI_CNTRL	PCI_55S	PCI	PCI_DEVSEL_L	
PCI_CNTRL	PCI_55S	PCI	PCI_PERR_L	
PCI_CNTRL	PCI_55S	PCI	PCI_SERR_L	
PCI_CNTRL	PCI_55S	PCI	PCI_STOP_L	
PCI_CNTRL	PCI_55S	PCI	PCI_TRDY_L	
PCI_CNTRL	PCI_55S	PCI	PCI_FRAME_L	
PCI_REQ0_L	PCI_55S	PCI	PCI_REQ0_L	19
PCI_GNT0_L	PCI_55S	PCI	PCI_GNT0_L	
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	19
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L	
PCI_INTW_L	PCI_55S	PCI	PCI_INTW_L	
PCI_INTX_L	PCI_55S	PCI	PCI_INTX_L	
PCI_INTY_L	PCI_55S	PCI	PCI_INTY_L	
PCI_INTZ_L	PCI_55S	PCI	PCI_INTZ_L	
MCP_PCI_CLK2	CLK_PCI_55S	CLK_PCI	PCI_CLK33M MCP_R	19
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M MCP	19
LPC_AD	LPC_55S	LPC	LPC_AD<3..0>	19 42 44 83
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L	19 42 44 83
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L	19 26 83
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M SMC_R	19 26
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M SMC	26 42
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M LPCPLUS	26 44
USB_EXT_A	USB_90D	USB	USB_EXT_A_P	20 40
	USB_90D	USB	USB_EXT_A_N	20 40
	USB_90D	USB	USB_EXT_A_MUXED_P	
	USB_90D	USB	USB_EXT_A_MUXED_N	
USB_MINI	USB_90D	USB	USB_MINI_P	9 20
	USB_90D	USB	USB_MINI_N	9 20
USB_EXTD	USB_90D	USB	USB_EXTD_P	9 20
	USB_90D	USB	USB_EXTD_N	9 20
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	20 31
	USB_90D	USB	USB_CAMERA_N	20 31
USB_BT	USB_90D	USB	USB_BT_P	20 31
	USB_90D	USB	USB_BT_N	20 31
USB_TPAD	USB_90D	USB	USB_TPAD_P	20 50
	USB_90D	USB	USB_TPAD_N	20 50
USB_IR	USB_90D	USB	USB_IR_P	20 41
	USB_90D	USB	USB_IR_N	20 41
USB_EXTR	USB_90D	USB	USB_EXTR_P	20 40
	USB_90D	USB	USB_EXTR_N	20 40
USB_EXCARD	USB_90D	USB	USB_EXCARD_P	20 32
	USB_90D	USB	USB_EXCARD_N	20 32
USB_EXTC	USB_90D	USB	USB_EXTC_P	9 20
	USB_90D	USB	USB_EXTC_N	9 20
MCP_USB_RBIA5	MCP_USB_RBIA5		MCP_USB_RBIA5_GND	20
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK	7 13 21 65
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA	7 13 21 65
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK	21 45
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA	21 45
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	9 21
	HDA_55S	HDA	HDA_BIT_CLK_R	21
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	21 54
	HDA_55S	HDA	HDA_SYNC_R	21
HDA_RST_L	HDA_55S	HDA	HDA_RST_L	21
	HDA_55S	HDA	HDA_RST_L	21 54
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	21 54
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	21 54
	HDA_55S	HDA	HDA_SDOUT_R	21
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP	21
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R	21 26
	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	26 42
SPI_CLK	SPT_55S	SPT	SPI_CLK_R	21 44
	SPT_55S	SPT	SPI_CLK	44 53
SPI_MOSI	SPT_55S	SPT	SPI_MOSI_R	21 44
	SPT_55S	SPT	SPI_MOSI	44 53
SPI_MISO	SPT_55S	SPT	SPI_MISO	21 44
	SPT_55S	SPT	SPI_MISO_R	53
SPI_CS0	SPT_55S	SPT	SPI_CS0_R_L	21 44
	SPT_55S	SPT	SPI_CS0_L	

MCP Constraints 2	
SYNC_MASTER=MUXGFX	SYNC_DATE=02/18/2008
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FireWire Constraints

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	GDDR3 Frame Buffer Signal Constraints																																																																																																																																																																																																																																																												
	<table><tr><th>PHYSICAL_RULE_SET</th><th>LAYER</th><th>ALLOW ROUTE ON LAYER?</th><th>MINIMUM LINE WIDTH</th><th>MINIMUM NECK WIDTH</th><th>MAXIMUM NECK LENGTH</th><th>DIFFPAIR PRIMARY GAP</th><th>DIFFPAIR NECK GAP</th></tr><tr><td>GDDR3_40R55SE</td><td>*</td><td>=55_OHM_SE</td><td>=40_OHM_SE</td><td>0.095 MM</td><td>12.7 MM</td><td>=STANDARD</td><td>=STANDARD</td></tr><tr><td>GDDR3_40SE</td><td>*</td><td>=40_OHM_SE</td><td>=40_OHM_SE</td><td>0.095 MM</td><td>=40_OHM_SE</td><td>=STANDARD</td><td>=STANDARD</td></tr><tr><td>GDDR3_80D</td><td>*</td><td>=80_OHM_DIFF</td><td>=80_OHM_DIFF</td><td>0.095 MM</td><td>=80_OHM_DIFF</td><td>=80_OHM_DIFF</td><td>=80_OHM_DIFF</td></tr></table>								PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	GDDR3_40R55SE	*	=55_OHM_SE	=40_OHM_SE	0.095 MM	12.7 MM	=STANDARD	=STANDARD	GDDR3_40SE	*	=40_OHM_SE	=40_OHM_SE	0.095 MM	=40_OHM_SE	=STANDARD	=STANDARD	GDDR3_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	0.095 MM	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF																																																																																																																																																																																																																					
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																																																																																																																																																																																																																																																						
GDDR3_40R55SE	*	=55_OHM_SE	=40_OHM_SE	0.095 MM	12.7 MM	=STANDARD	=STANDARD																																																																																																																																																																																																																																																						
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D	<table><tr><th>SPACING_RULE_SET</th><th>LAYER</th><th>LINE-TO-LINE SPACING</th><th>WEIGHT</th></tr><tr><td>GDDR3_CLK</td><td>*</td><td>=2.5:1_SPACING</td><td>?</td></tr><tr><td>GDDR3_CMD</td><td>*</td><td>=2.5:1_SPACING</td><td>?</td></tr><tr><td>GDDR3_DATA</td><td>*</td><td>=2.5:1_SPACING</td><td>?</td></tr><tr><td>GDDR3_DQS</td><td>*</td><td>=2.5:1_SPACING</td><td>?</td></tr></table>								SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	GDDR3_CLK	*	=2.5:1_SPACING	?	GDDR3_CMD	*	=2.5:1_SPACING	?	GDDR3_DATA	*	=2.5:1_SPACING	?	GDDR3_DQS	*	=2.5:1_SPACING	?																																																																																																																																																																																																																																	
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	LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length. DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps. DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals. Max length of LVDS/DisplayPort/TMDS traces: 12 inches. SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.																																																																																																																																																																																																																																																												
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73	72	FB_AB_CS0	GDDR3_40R55SE	GDDR3_CMD	FB A_CS0_L 72 73	72	FB_AB_CMD_RN	GDDR3_40R55SE	GDDR3_CMD	FB A_DRAM_RST 72 73	72	FB_A_CMD	GDDR3_40SE	GDDR3_CMD	FB A_LMA<5..2> 72 73	72	FB_B_CMD	GDDR3_40SE	GDDR3_CMD	FB A_UMA<5..2> 72 73	72	FB_A_WDQS0	GDDR3_40SE	GDDR3_DQS	FB A_WDQS<0> 72 73	72	FB_A_WDQS1	GDDR3_40SE	GDDR3_DQS	FB A_WDQS<1> 72 73	72	FB_A_WDQS2	GDDR3_40SE	GDDR3_DQS	FB A_WDQS<2> 72 73	72	FB_A_WDQS3	GDDR3_40SE	GDDR3_DQS	FB A_WDQS<3> 72 73	72	FB_A_RDQS0	GDDR3_40SE	GDDR3_DQS	FB A_RDQS<0> 72 73	72	FB_A_RDQS1	GDDR3_40SE	GDDR3_DQS	FB A_RDQS<1> 72 73	72	FB_A_RDQS2	GDDR3_40SE	GDDR3_DQS	FB A_RDQS<2> 72 73	72	FB_A_RDQS3	GDDR3_40SE	GDDR3_DQS	FB A_RDQS<3> 72 73	72	FB_A_DQ_RVTR0	GDDR3_40SE	GDDR3_DATA	FB A_DQ<7..0> 72 73	72	FB_A_DQ_RVTR1	GDDR3_40SE	GDDR3_DATA	FB A_DQ<15..8> 72 73	72	FB_A_DQ_RVTR2	GDDR3_40SE	GDDR3_DATA	FB A_DQ<23..16> 72 73	72	FB_A_DQ_RVTR3	GDDR3_40SE	GDDR3_DATA	FB A_DQ<31..24> 72 73	72	FB_A_DQM0	GDDR3_40SE	GDDR3_DATA	FB A_DQM_L<0> 72 73	72	FB_A_DQM1	GDDR3_40SE	GDDR3_DATA	FB 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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_I101_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_I101_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CFU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	FSB_DSTB	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_70D	BOTTOM			0.127 MM	6.35 MM		

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	BGA	100_DIFF_BGA
DP_100D	BGA	100_DIFF_BGA
SATA_100D	BGA	100_DIFF_BGA

M99 Specific Net Properties

ELECTRICAL_CONSTRAINT_SKT		NET_TYPE		
		PHYSICAL	SPACING	
		ENET_MDI_100D	ENETCONN	ENETCONN P<3...0>
		ENET_MDI_100D	ENETCONN	ENETCONN N<3...0>
8340		SATA_100D	SATA	SATA_ODD_R2D_UF_P
8341		SATA_100D	SATA	SATA_ODD_R2D_UF_N
8342		SATA_100D	SATA	SATA_ODD_D2R_UF_P
8343		SATA_100D	SATA	SATA_ODD_D2R_UF_N
8344		SATA_100D	SATA	SATA_HDD_D2R_UF_P
8345		SATA_100D	SATA	SATA_HDD_D2R_UF_N
8346		SATA_100D	SATA	SATA_HDD_R2D_UF_P
8347		SATA_100D	SATA	SATA_HDD_R2D_UF_N
8348	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	GFXXIMVP6_VSEN_P
8349	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	GFXXIMVP6_VSEN_N
8350	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	MPCOREISNS_P
8351	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	MPCOREISNS_N
8352	CPUTHMSNS_D2_DP	THERM_170I_55S	THERM	CPUTHMSNS_D2_P
8353	CPUTHMSNS_D2_DP	THERM_170I_55S	THERM	CPUTHMSNS_D2_N
8354	CPU_THERMD_DP	THERM_170I_55S	THERM	CPU_THERMD_P
8355	CPU_THERMD_DP	THERM_170I_55S	THERM	CPU_THERMD_N
8356	CPUTHMSNS_D_P	THERM_170I_55S	THERM	GPUTHMSNS_D_P
8357	CPUTHMSNS_D_P	THERM_170I_55S	THERM	GPUTHMSNS_D_N
8358	GPU_THERMD_DP	THERM_170I_55S	THERM	GPU_TDIODE_P
8359	GPU_THERMD_DP	THERM_170I_55S	THERM	GPU_TDIODE_N
8360	MCPTHMSNS_D_P	THERM_170I_55S	THERM	MCPTHMSNS_D_P
8361	MCPTHMSNS_D_P	THERM_170I_55S	THERM	MCPTHMSNS_D_N
8362	MCP_THERMD_DP	THERM_170I_55S	THERM	MCP_THMDIODE_P
8363	MCP_THERMD_DP	THERM_170I_55S	THERM	MCP_THMDIODE_N
8364	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	1V05CPUISNS_R_P
8365	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	1V05CPUISNS_R_N
8366	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	DDRISNS_R_P
8367	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	DDRISNS_R_N
8368	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	GPUISNS_P
8369	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	GPUISNS_N
8370	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	1V05CPU_P
8371	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	1V05CPU_N
8372	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	DDRISNS_P
8373	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	DDRISNS_N
8374	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	PIV8GPU_P
8375	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	PIV8GPU_N
8376	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	ISNS_CPU_P
8377	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	ISNS_CPU_N
			GND	GND
			SB_POWER	PP3V3_S5
			SB_POWER	PP3V3_S0
			SB_POWER	PEIV5_S0
8378	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	PIV8GPUISNS_P
8379	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	PIV8GPUISNS_N
8380	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	PIV8GPUISNS_R_P
8381	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	PIV8GPUISNS_R_N

M99 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
E888	(PCIE_EXCARD)	PCIE_90D	PCIE	PCIE EXCARD R2D P 7 32 89
E889	(PCIE_EXCARD)	PCIE_90D	PCIE	PCIE EXCARD R2D N 7 32 89
E890	(PCIE_MINI)	PCIE_90D	PCIE	PCIE MINI R2D P 31 89
E891	(PCIE_MINI)	PCIE_90D	PCIE	PCIE MINI R2D N 31 89
E892		CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI CONN P 31
E893		CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI CONN N 31
E894		1T01_DIFFPAIR		CHGR CSI R P 61
E895		1T01_DIFFPAIR		CHGR CSI R N 61
E896		1T01_DIFFPAIR		CHGR CSO R P 46 61
E897		1T01_DIFFPAIR		CHGR CSO R N 46 61
E898	(USB_EXTX)	USB_90D	USB	USB2 EXTA MIXED P 40
E899	(USB_EXTX)	USB_90D	USB	USB2 EXTA MIXED N 40
E900	(USB_EXTX)	USB_90D	USB	USB2 LT1 P 40
E901	(USB_EXTX)	USB_90D	USB	USB2 LT1 N 40
E902	(USB_EXSTD)	USB_90D	USB	CONN TPAD USB P
E903	(USB_EXSTD)	USB_90D	USB	CONN TPAD USB N
E904	(USB_CAMERA)	USB_90D	USB	USB CAMERA CONN P 31
E905	(USB_CAMERA)	USB_90D	USB	USB CAMERA CONN N 31
E906		USB_90D	USB	CONN USB2_BT P 31
E907		USB_90D	USB	CONN USB2_BT N 31
E908		USB_90D	USB	USB LT2 P 40
E909		USB_90D	USB	USB LT2 N 40
E910		USB_90D	USB	USB2 EXCARD CONN P 7 32
E911		USB_90D	USB	USB2 EXCARD CONN N 7 32
E912		DP_100D	DISPLAYPORT	DP IG AUX CH C P 80
E913		DP_100D	DISPLAYPORT	DP IG AUX CH C N 80
E914	MCP_PE4_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M_FC P 9 32
E915		CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M_FC N 9 32
E916	PCIE_FC_R2D	PCIE_90D	PCIE	PCIE FC R2D C P 9 32
E917		PCIE_90D	PCIE	PCIE FC R2D C N 9 32
E918	PCIE_FC_D2R	PCIE_90D	PCIE	PCIE FC D2R P 9 32
E919		PCIE_90D	PCIE	PCIE FC D2R N 9 32
E920		PCIE_90D	PCIE	PCIE FC R2D P 32
E921		PCIE_90D	PCIE	PCIE FC R2D N 32
E922		CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M_EXCARD CONN N 9 32
E923		CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M_EXCARD CONN P 9 32
E924	SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN L_P_OUT 7 57
E925		DIFFPAIR	AUDIO	SPKRCONN L_N_OUT 7 57
E926	SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN S_P_OUT 7 57
E927		DIFFPAIR	AUDIO	SPKRCONN S_N_OUT 7 57
E928	SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN R_P_OUT 7 57
E929		DIFFPAIR	AUDIO	SPKRCONN R_N_OUT 7 57
E930		DIFFPAIR	AUDIO	SPKRAMP L_P_OUT 67
E931		DIFFPAIR	AUDIO	SPKRAMP L_N_OUT 67
E932		DIFFPAIR	AUDIO	SPKRAMP R_P_OUT 67
E933		DIFFPAIR	AUDIO	SPKRAMP R_N_OUT 67
E934		DIFFPAIR	AUDIO	SPKRAMP S_P_OUT 67
E935		DIFFPAIR	AUDIO	SPKRAMP S_N_OUT 67

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	5.8 MM OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	5.8 MM OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	5.8 MM OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D_VDD OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_90D OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
USB_90D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MI1_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIA5 OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	*	OVERRIDE	OVERRIDE	0.25 MM OVERRIDE	250 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	ISL4, ISL9 OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD OVERRIDE	ISL3, ISL10 OVERRIDE	N OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	ISL4, ISL9 OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D_VDD OVERRIDE	ISL3, ISL10 OVERRIDE	N OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

Ground-referenced memory signals (DQ,DQM,DQS) MAY route on ISL9 (VDD-referenced plane)but not next to VDD island. Forces power-referenced memory signals (CLK,ADDR,CTRL) to not route on ISL3, ISL4 & ISL10(GND-referenced planes).

Project Specific Constraints	
SYNC_MASTER=MUXGFX	SYNC_DATE=02/21/2008

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M99 Board-Specific Spacing & Physical Constraints																			
BOARD LAYERS								BOARD AREAS				BOARD UNITS (MIL or MM)		ALLEGRO VERSION					
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM								NO_TYPE, BGA				MM		15.5.1					
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT					
DEFAULT		*	Y	=50_OHM_SE	=50_OHM_SE	14 MM	0 MM	0 MM		DEFAULT		*	0.1 MM	?					
STANDARD		*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT		STANDARD		*	=DEFAULT	?					
BGA_F1MM		*								BGA_F1MM		*	=DEFAULT	?					
BGA_P2MM		*								BGA_P2MM		*	=DEFAULT	?					
BGA_F3MM		*								BGA_F3MM		*	=DEFAULT	?					
NET_SPACING_TYPE1		NET_SPACING_TYPE2		AREA_TYPE		SPACING_RULE_SET				NET_SPACING_TYPE1		NET_SPACING_TYPE2		AREA_TYPE					
*		*		BGA		BGA_F1MM				*		*		BGA					
MEM_CLK		*		BGA		BGA_P2MM				MEM_CLK		*		BGA					
CLK_FSB		*		BGA		BGA_P2MM				CLK_FSB		*		BGA					
CLK_PCIE		*		BGA		BGA_P2MM				CLK_PCIE		*		BGA					
CLK_SLOW		*		BGA		BGA_P2MM				CLK_SLOW		*		BGA					
FSB_DSTB		FSB_DSTB		BGA		BGA_F3MM				FSB_DSTB		FSB_DSTB		BGA					
SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT						SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT					
1.5:1_SPACING		*	0.15 MM	?						1.5:1_SPACING		*	0.15 MM	?					
1.8:1_SPACING		*	0.18 MM	?						1.8:1_SPACING		*	0.18 MM	?					
2:1_SPACING		*	0.2 MM	?						2:1_SPACING		*	0.2 MM	?					
2.5:1_SPACING		*	0.25 MM	?						2.5:1_SPACING		*	0.25 MM	?					
3:1_SPACING		*	0.3 MM	?						3:1_SPACING		*	0.3 MM	?					
4:1_SPACING		*	0.4 MM	?						4:1_SPACING		*	0.4 MM	?					
SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT						SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT					
2X_DIELECTRIC		*	0.140 MM	?						2X_DIELECTRIC		*	0.140 MM	?					
3X_DIELECTRIC		*	0.210 MM	?						3X_DIELECTRIC		*	0.210 MM	?					
4X_DIELECTRIC		*	0.280 MM	?						4X_DIELECTRIC		*	0.280 MM	?					
5X_DIELECTRIC		*	0.350 MM	?						5X_DIELECTRIC		*	0.350 MM	?					
NOTE: From T18 MLB, changed to reflect M99 stackup.																			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
40_OHM_SE		TOP, BOTTOM	Y	0.165 MM	0.095 MM					1:1_DIFFPAIR		*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	
40_OHM_SE		*	Y	0.135 MM	0.135 MM	=STANDARD	=STANDARD	=STANDARD										0.1 MM	
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
27P4_OHM_SE		TOP, BOTTOM	Y	0.310 MM	0.095 MM					70_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
27P4_OHM_SE		*	Y	0.250 MM	0.250 MM	=STANDARD	=STANDARD	=STANDARD		70_OHM_DIFF		ISL3, ISL4	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM	
										70_OHM_DIFF		ISL9, ISL10	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM	
										70_OHM_DIFF		ISL2, ISL11	Y	0.170 MM	0.170 MM		0.150 MM	0.150 MM	
										70_OHM_DIFF		TOP, BOTTOM	Y	0.170 MM	0.095 MM		0.150 MM	0.150 MM	
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
80_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD		80_OHM_DIFF		ISL3, ISL4	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM	
80_OHM_DIFF		ISL3, ISL4	Y	0.125 MM	0.125 MM					80_OHM_DIFF		ISL9, ISL10	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM	
80_OHM_DIFF		ISL9, ISL10	Y	0.125 MM	0.125 MM					80_OHM_DIFF		ISL2, ISL11	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM	
80_OHM_DIFF		ISL2, ISL11	Y	0.140 MM	0.140 MM					80_OHM_DIFF		TOP, BOTTOM	Y	0.140 MM	0.095 MM		0.190 MM	0.190 MM	
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
90_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD		90_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
90_OHM_DIFF		ISL3, ISL4	Y	0.102 MM	0.102 MM					90_OHM_DIFF		ISL3, ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM	
90_OHM_DIFF		ISL9, ISL10	Y	0.102 MM	0.102 MM					90_OHM_DIFF		ISL9, ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM	
90_OHM_DIFF		ISL2, ISL11	Y	0.115 MM	0.115 MM					90_OHM_DIFF		ISL2, ISL11	Y	0.115 MM	0.115 MM		0.230 MM	0.230 MM	
90_OHM_DIFF		TOP, BOTTOM	Y	0.115 MM	0.095 MM					90_OHM_DIFF		TOP, BOTTOM	Y	0.115 MM	0.095 MM		0.230 MM	0.230 MM	
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
100_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD		100_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
100_OHM_DIFF		ISL3, ISL4	Y	0.080 MM	0.080 MM					100_OHM_DIFF		ISL3, ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM	
100_OHM_DIFF		ISL9, ISL10	Y	0.080 MM	0.080 MM					100_OHM_DIFF		ISL9, ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM	
100_OHM_DIFF		ISL2, ISL11	Y	0.089 MM	0.089 MM					100_OHM_DIFF		ISL2, ISL11	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM	
100_OHM_DIFF		TOP, BOTTOM	Y	0.089 MM	0.089 MM					100_OHM_DIFF		TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM	
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
110_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD		110_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
110_OHM_DIFF		ISL3, ISL4	Y	0.077 MM	0.077 MM					110_OHM_DIFF		ISL3, ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM	
110_OHM_DIFF		ISL9, ISL10	Y	0.077 MM	0.077 MM					110_OHM_DIFF		ISL9, ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM	
110_OHM_DIFF		ISL2, ISL11	Y	0.077 MM	0.077 MM					110_OHM_DIFF		ISL2, ISL11	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM	
110_OHM_DIFF		TOP, BOTTOM	Y	0.077 MM	0.077 MM					110_OHM_DIFF		TOP, BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM	
PCB Rule Definitions		SYNC_MASTER=M99_MLB SYNC_DATE=01/22/2008																	
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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

NOTE: From T18 MLB, changed to reflect M99 stackup.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PCB Rule Definitions

SYNC_MASTER=M99_MLB

SYNC_DATE=01/22/2008


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