

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM, MLB, M96

EVT

08/01/2008

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE



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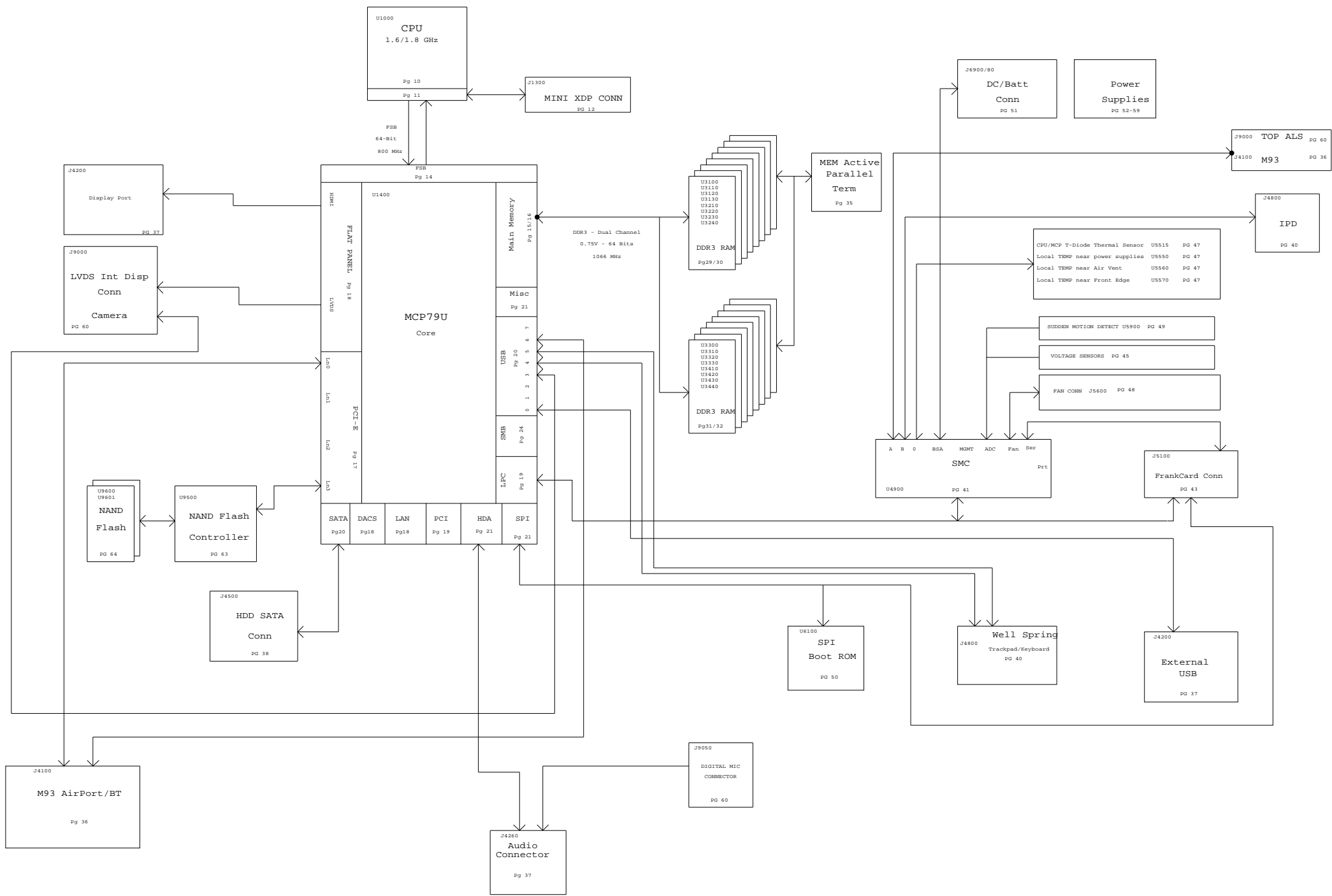
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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7631	1	SCHEM, MLB, M96	SCH	CRITICAL	
820-2375	1	PCBF, MLB, M96	PCB	CRITICAL	

DRAWING
TITLE=M96_MLB
ABBREV=DRAWING
LAST_MODIFIED=PV1 Aug 1 09:54:13 2008

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	DRAFTER	DESIGN CK		
	QA APPD	DESIGNER	TITLE	
	RELEASE	SCALE	SIZE	
MATERIAL/FINISH NOTED AS APPLICABLE		D	SCHEM, MLB, M96	
DRAWING NUMBER		REV.		
051-7631		2.3.0		
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System Block Diagram

SYNC_MASTER=WFERRY-WF SYNC_DATE=05/11/2006

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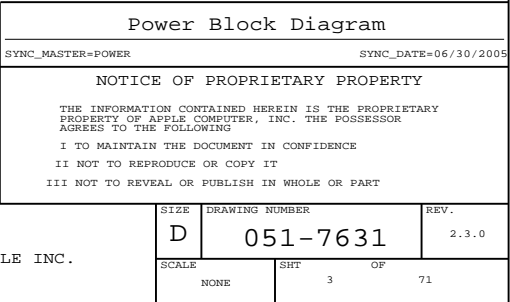
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REV.

2.3.0



Functional Test Points

NB NO_TESTS
These are normally testpoints but become NC
NO_TEST

FUNC TEST - BATTERY CONNECTOR
x2
TRUE BATT_POS 49
TRUE GND 49
TRUE SMC_BS_ALRT_L 39 40 49
TRUE SMBUS_SMC_BSA_SCL 42 69
TRUE SMBUS_SMC_BSA_SDA 42 69

FUNC TEST - DC-IN CONNECTOR
x6
TRUE PP18V5_DCIN 49 70
TRUE ADAPTER_SENSE 49
TRUE GND 49

FUNC TEST - FAN CONNECTOR
TRUE =PP5V_S0_FAN 7 46
TRUE FAN_RT_PWM 46
TRUE FAN_RT_TACH 46
TRUE GND 46

FUNC TEST - AIRPORT
TRUE CK505_SRC_CLKREQ6_L 6
TRUE PCIE_WAKE_L 6 16 34
TRUE AIRPORT_RST_L 6 24 34
TRUE =SMB_AIRPORT_CLK 6 34 42
TRUE =SMB_AIRPORT_DATA 6 34 42
TRUE GND 6 34 42

FUNC TEST - MIC
TRUE PP3V3_S0_MIC_F 59 70
TRUE AUD_MIC_DATA_F 59
TRUE AUD_MIC_CLK_F 59
TRUE GND_MIC_F 59

FUNC TEST - AUDIO CONNECTOR
TRUE HDA_SYNC 20 35 68
TRUE HDA_BIT_CLK 20 35 68
TRUE AUD_MIC_DATA 35 59
TRUE HDA_SDOUT 20 35 68
TRUE =PPVIN_S0_AUDIO 7 35
TRUE HDA_SDIN0 20 35 68
TRUE AUD_MIC_CLK 35 59
TRUE PM_SLP_S3_L 20 34 35 39 56

FUNC TEST - IPD CONNECTOR
TRUE SMC_LID 38 39 40
TRUE PP3V42_G3H_IPD_F 38 70
TRUE SMC_SYS_KBDLED 38 39
TRUE SMC_SYS_LED 38 39
TRUE =USB2_TPAD_N 8 38
TRUE =USB2_TPAD_P 8 38
TRUE SMC_ONOFF_L 6 38 39 40
TRUE =USB2_IR_N 6 8 38
TRUE =USB2_IR_P 6 8 38
TRUE PP5V_S0_KBDLED_F 6 38 70
TRUE PP5V_S3_TOPCASE_F 38 70
TRUE =I2C_TPAD_SCL 38 42
TRUE =I2C_TPAD_SDA 38 42
TRUE SMC_ONOFF_L 6 38 39 40
TRUE =USB2_IR_N 6 8 38
TRUE =USB2_IR_P 6 8 38
TRUE PP5V_S0_KBDLED_F 6 38 70
TRUE LSOC_PRESS_H_R 38

FUNC TEST - M93 WIRELESS CONNECTOR
TRUE AIRPORT_RST_L 6 24 34
TRUE PCIE_WAKE_L 6 16 34
TRUE CK505_SRC_CLKREQ6_L 6
TRUE PCIE_CLK100M_MINI_N_F 34
TRUE PCIE_CLK100M_MINI_P_F 34
TRUE PCIE_E_D2R_N_F 34
TRUE PCIE_E_D2R_P_F 34
TRUE PCIE_E_R2D_C_N_F 6 34
TRUE PCIE_E_R2D_C_P_F 6 34
TRUE AIRPORT_RST_L 6 24 34
TRUE =SMB_AIRPORT_DATA 6 34 42
TRUE =SMB_AIRPORT_CLK 6 34 42
TRUE PCIE_E_R2D_C_N_F 6 34
TRUE PCIE_E_R2D_C_P_F 6 34
TRUE PP3V3_S3_AP_AUX 34 70

FUNC TEST - Power Supplies
PPVCORE_S0_CPU 7 70
PP0V75_S0 7 70
PP1V05_S0 7 70
PP1V5_S0 7 70
PP1V5_S3 7 70
PP1V05_S5 7 70
PPMCPCORE_S0 7 70
PP5V_S0 7 70
PP3V3_S0 7 70
PP3V3_S3 7 70
PP5V_S3 7 70
PP3V3_S5 7 70
PP3V42_G3H 7 70
PP18V5_G3H 7 70
PPDCIN_G3H 7 70
PPBUS_G3H 7 70
PPBUS_R_G3H 7 70
PP1V8_S0 7 70

FUNC TEST - SATA HDD
TRUE PP3V3_S0_HDD_F 36 70
TRUE SATA_HDD_R2D_N 36 67
TRUE SATA_HDD_R2D_P 36 67
TRUE SATA_HDD_D2R_C_N 36 67
TRUE SATA_HDD_D2R_C_P 36 67
TRUE GND 36 67

FUNC TEST - RIO HATCH CONNECTOR
TRUE DP_ML_C_N<3..0> 61 67
TRUE DP_ML_C_P<3..0> 61 67
TRUE DP_AUX_CH_C_N 35 60 61 67
TRUE DP_AUX_CH_C_P 35 60 61 67
TRUE DP_CA_DET_Q 35 61
TRUE HDMI_CEC 35 61
TRUE DP_HPD_Q 35 61
TRUE PP3V3_S0_DPPWR 35 61 70
TRUE USB2_EXT_A_F_P 35 37
TRUE USB2_EXT_A_F_N 35 37
TRUE PP5V_S3_USB2_EXT_A_F 35 37 70
TRUE GND 35 37 70

x1 TRUE GND

FUNC TEST - XDP/ITP CONNECTOR
TRUE XDP_BPM_L<0..5> 9 12
TRUE TP_XDP_OBSFN_B0 12
TRUE TP_XDP_OBSFN_B1 12
TRUE TP_XDP_OBSDATA_B0 12
TRUE TP_XDP_OBSDATA_B1 12
TRUE TP_XDP_OBSDATA_B2 12
TRUE TP_XDP_OBSDATA_B3 12
TRUE XDP_PWRGD 12
TRUE XDP_OBS20 12
TRUE SMBUS_MCP_0_DATA 12 20 42 68
TRUE SMBUS_MCP_0_CLK 12 20 42 68
TRUE XDP_TCK 9 12
TRUE JTAG_MCP_TDO_CONN 9 12
TRUE JTAG_MCP_TRST_L 12 20
TRUE MCP_DEBUG<7..0> 12 18 68
TRUE JTAG_MCP_TDI 12 20
TRUE JTAG_MCP_TMS 12 20
TRUE FSB_CLK_ITP_P 12 13 65
TRUE FSB_CLK_ITP_N 12 13 65
TRUE XDP_CPURST_L 12 65
TRUE XDP_DBRESET_L 9 12
TRUE XDP_TDO_CONN 12
TRUE XDP_TRST_L 9 12
TRUE XDP_TDI 9 12
TRUE XDP_TMS 9 12
TRUE =PP3V3_S0_XDP 7 12
TRUE =PP1V05_S0_CPU 7 10 11 12

FUNC TEST - CAMERA USB, LVDS, ALS
x2 TRUE PP5V_S3_CAMERA_F 59 70
TRUE USB2_CAMERA_F_P 59
TRUE USB2_CAMERA_F_N 59
TRUE LCDBKLT_RTIN<1..6> 59 62
TRUE LVDS_IG_A_DATA_N<0..2> 17 59 67
TRUE LVDS_IG_A_DATA_P<0..2> 17 59 67
TRUE PPVOUT_S0_LCDBKLT 59 62 70
TRUE LVDS_IG_A_CLK_F_N 59 67
TRUE LVDS_IG_A_CLK_F_P 59 67
TRUE LVDS_IG_DDC_CLK 17 59
TRUE LVDS_IG_DDC_DATA 17 59
TRUE PP3V3_S0_LCD_F 59 70
TRUE PP3V3_LCDVDD_SW_F 59 70
x2 TRUE =I2C_ALS_SDA 42 59
TRUE =I2C_ALS_SCL 42 59
x10 TRUE GND 42 59

REQUIRED NETS

NICE2HAVE NETS

Power Supply NO_TESTS
NO_TEST

CLOCK NO_TESTS
NO_TEST

LVDS NO_TESTS
NO_TEST

Functional Test and No-Tests

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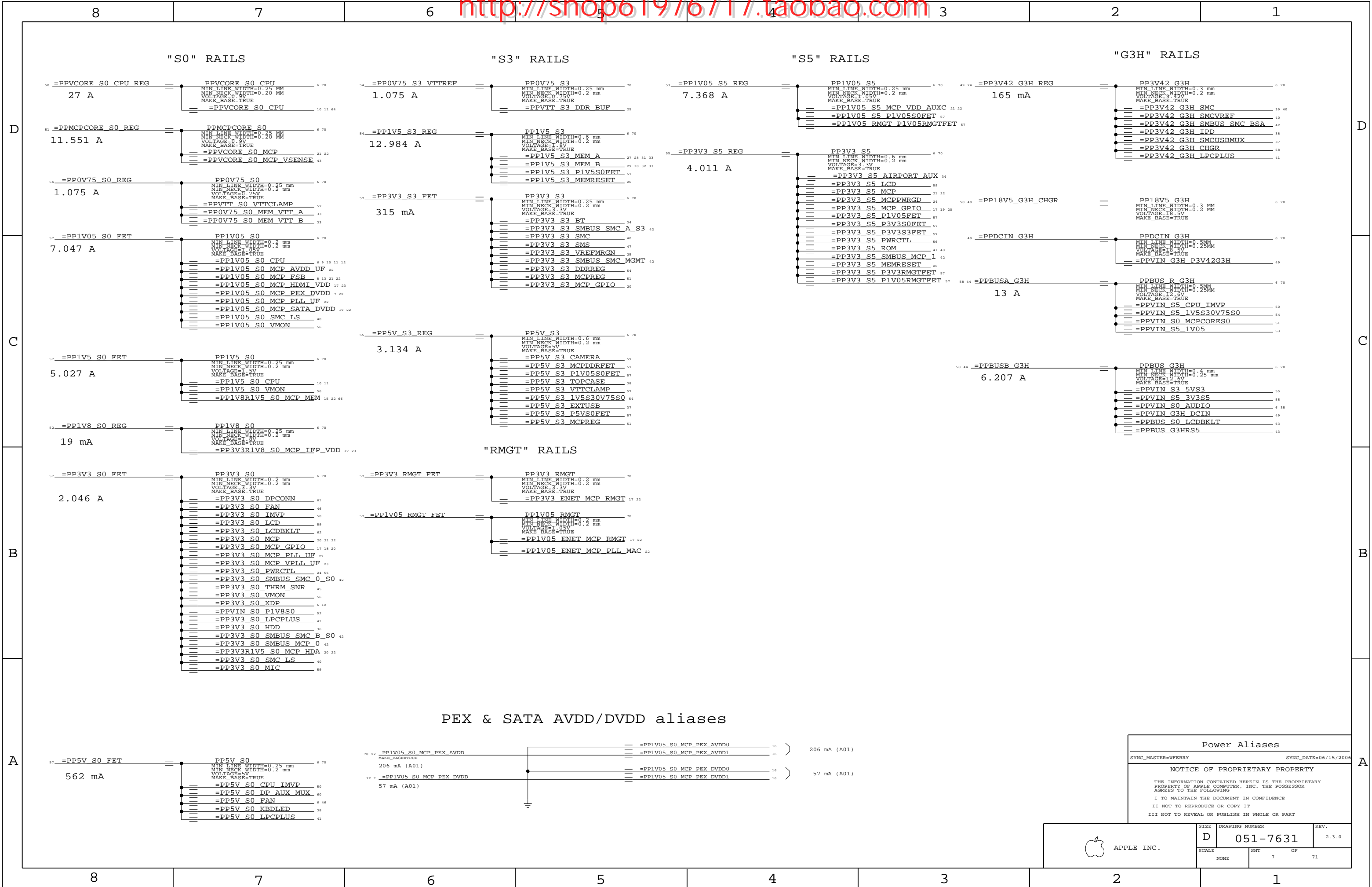
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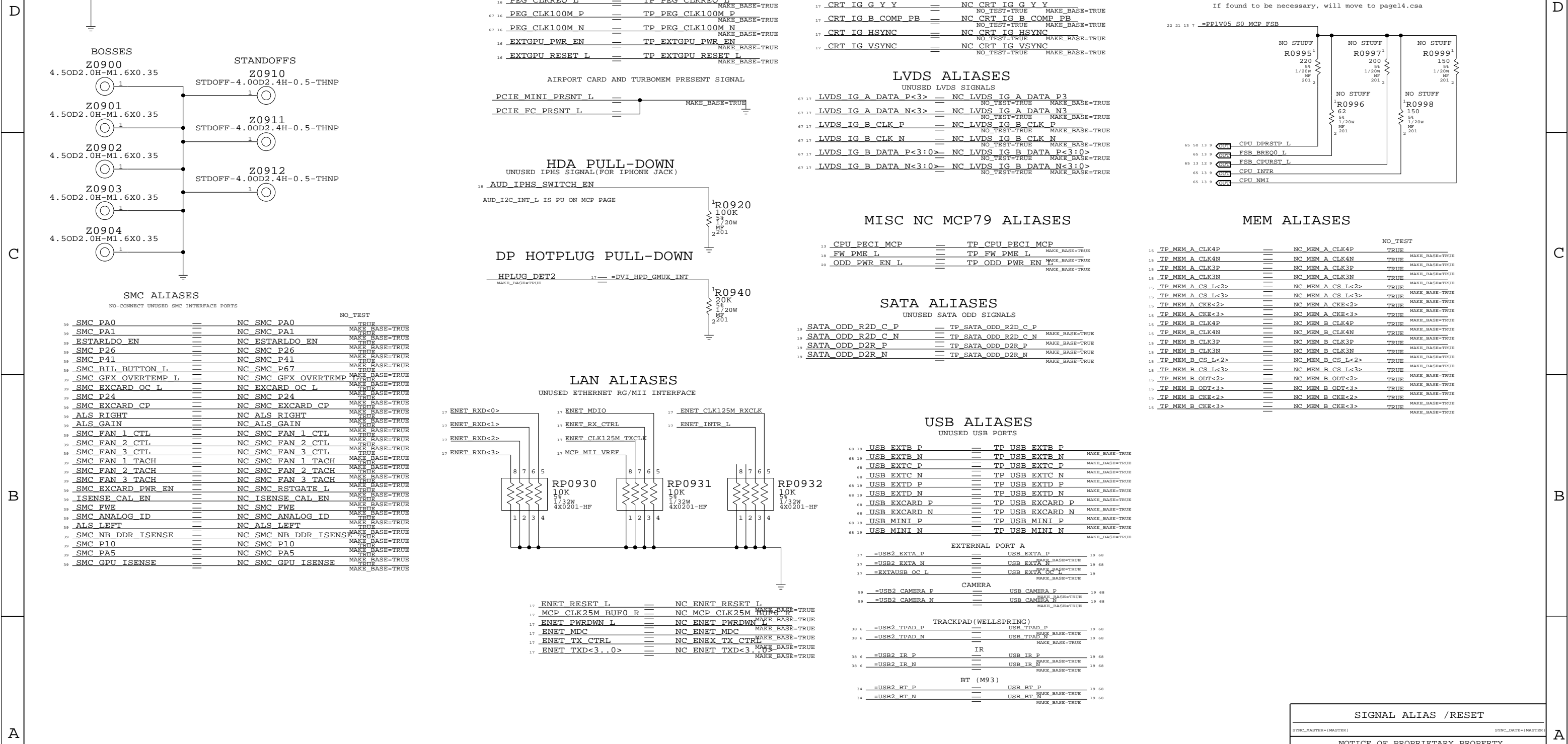
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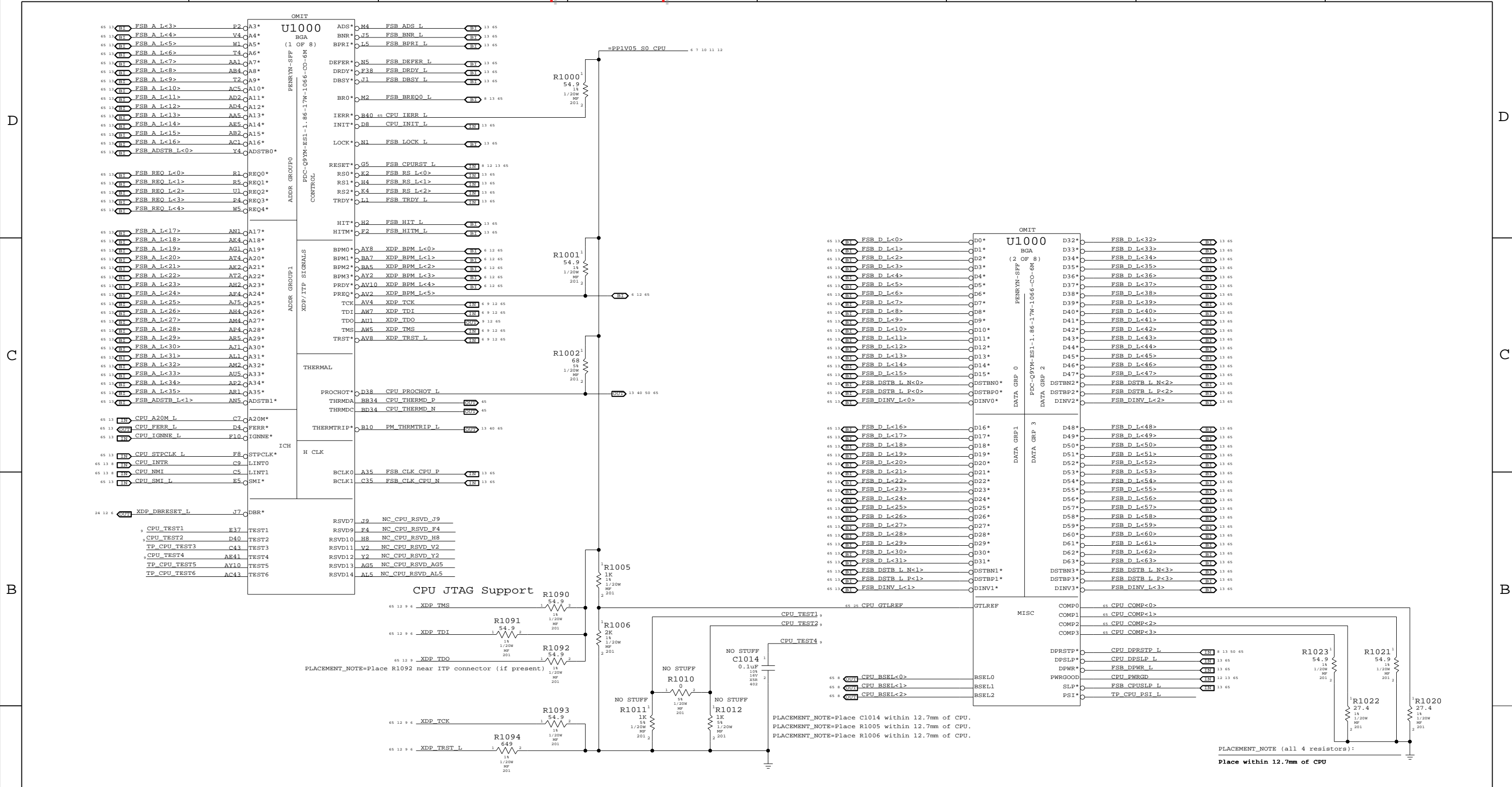
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SYNC FROM M97

CPU FSB	
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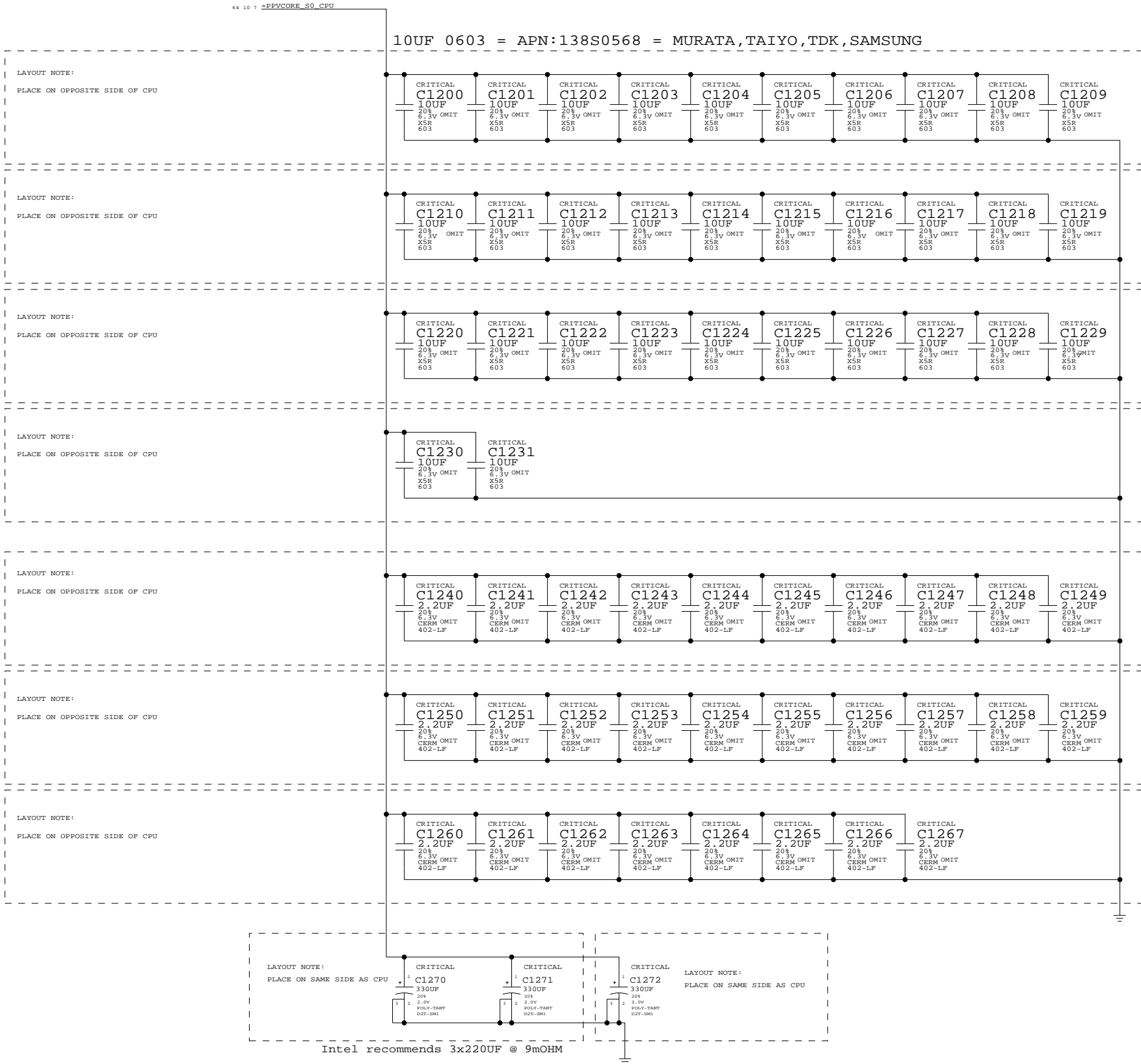
3x 330uF. 32x 10uF 0603, 28x 2.2uF 0402 + 40x 2.2uF 0402

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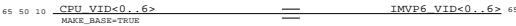
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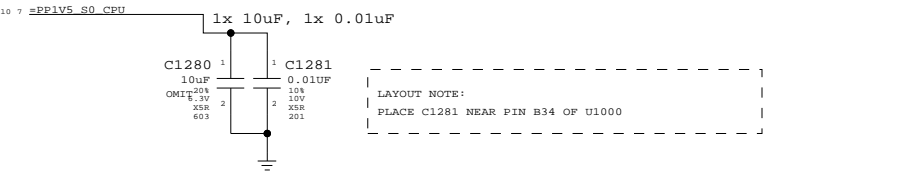
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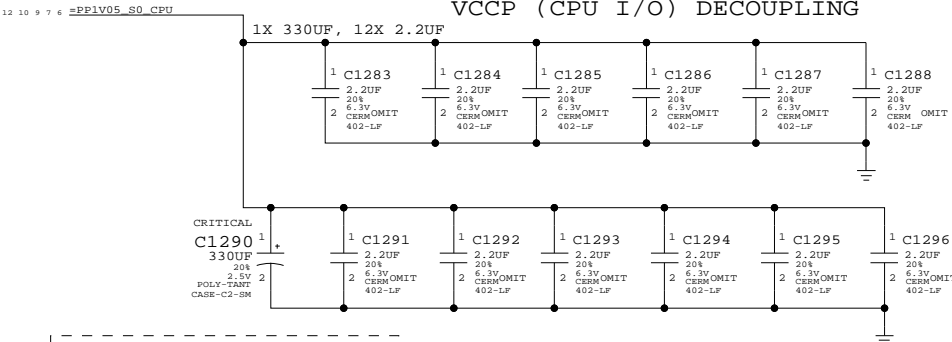
CPU VCORE VID CONNECTIONS



VCCA (CPU AVdd) DECOUPLING



VCCP (CPU I/O) DECOUPLING



LAYOUT NOTE:

PLACE C1290 CLOSE TO CPU

PLACE C1283-C1288 CLOSE TO FSB ADDRESS PINS

PLACE C1291-C1296 CLOSE TO FSB DATA PINS

CPU Decoupling & VID

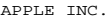
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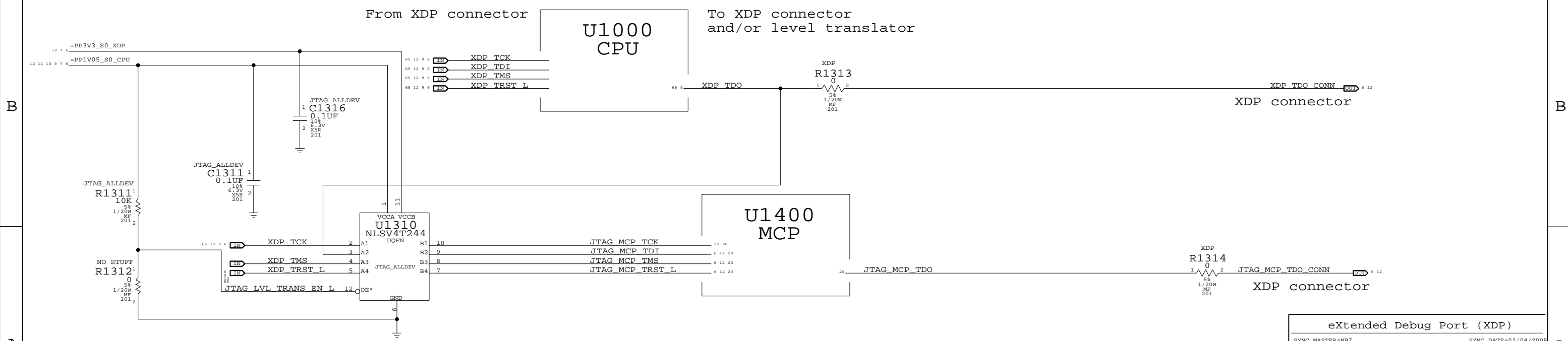
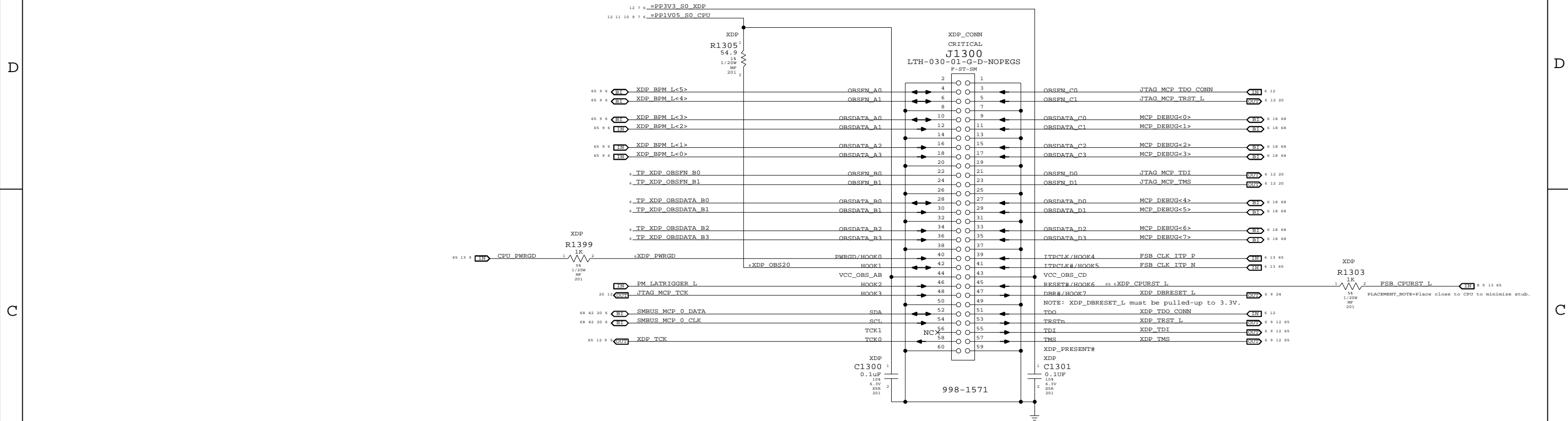


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NONE	11	71

MCP79-specific pinout	
1	NC
2	NC
3	NC
4	NC
5	NC
6	NC
7	NC
8	NC
9	NC
10	NC
11	NC
12	NC
13	NC
14	NC
15	NC
16	NC
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99	NC
100	NC



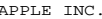
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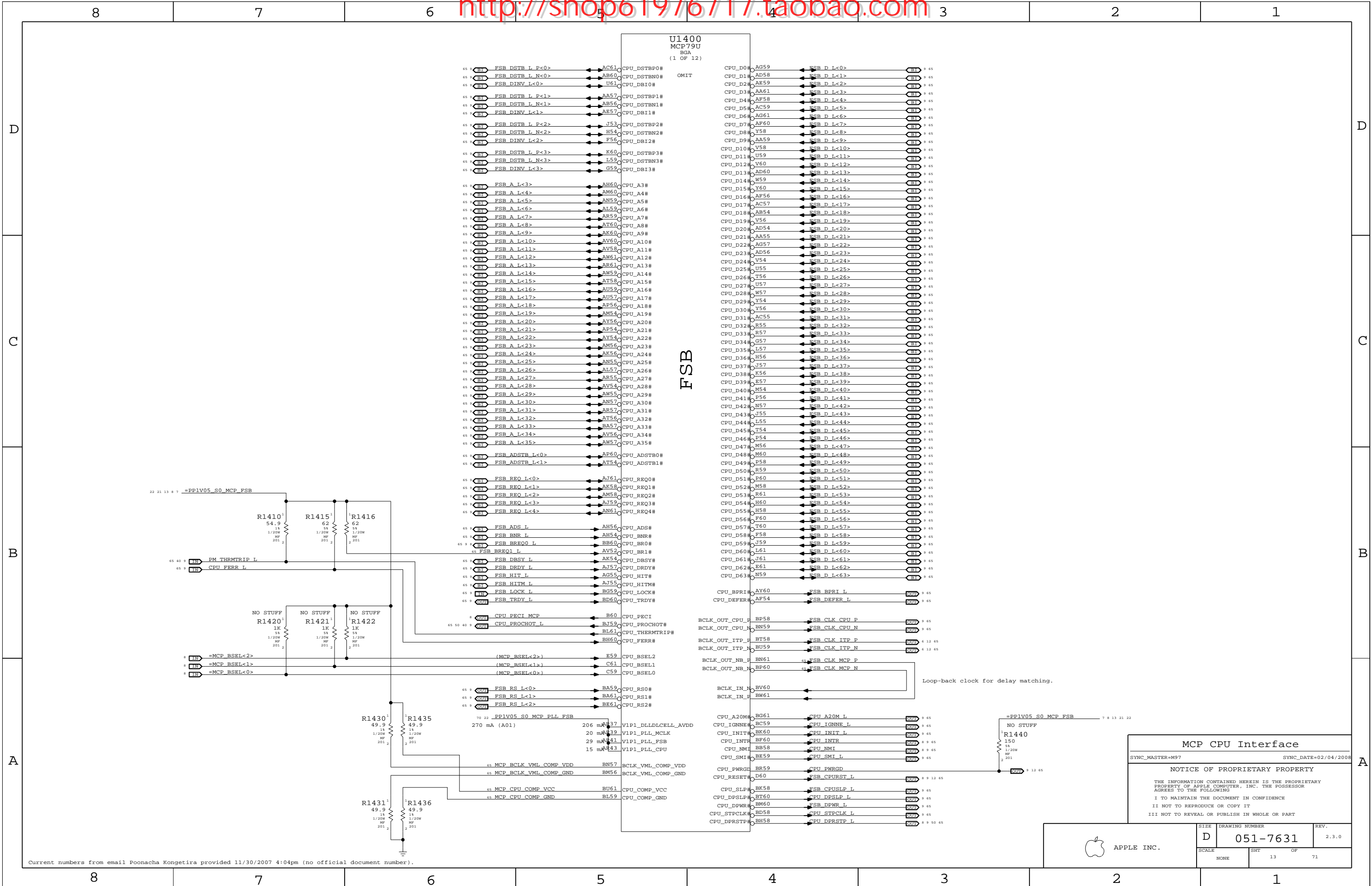
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MCP CPU Interface

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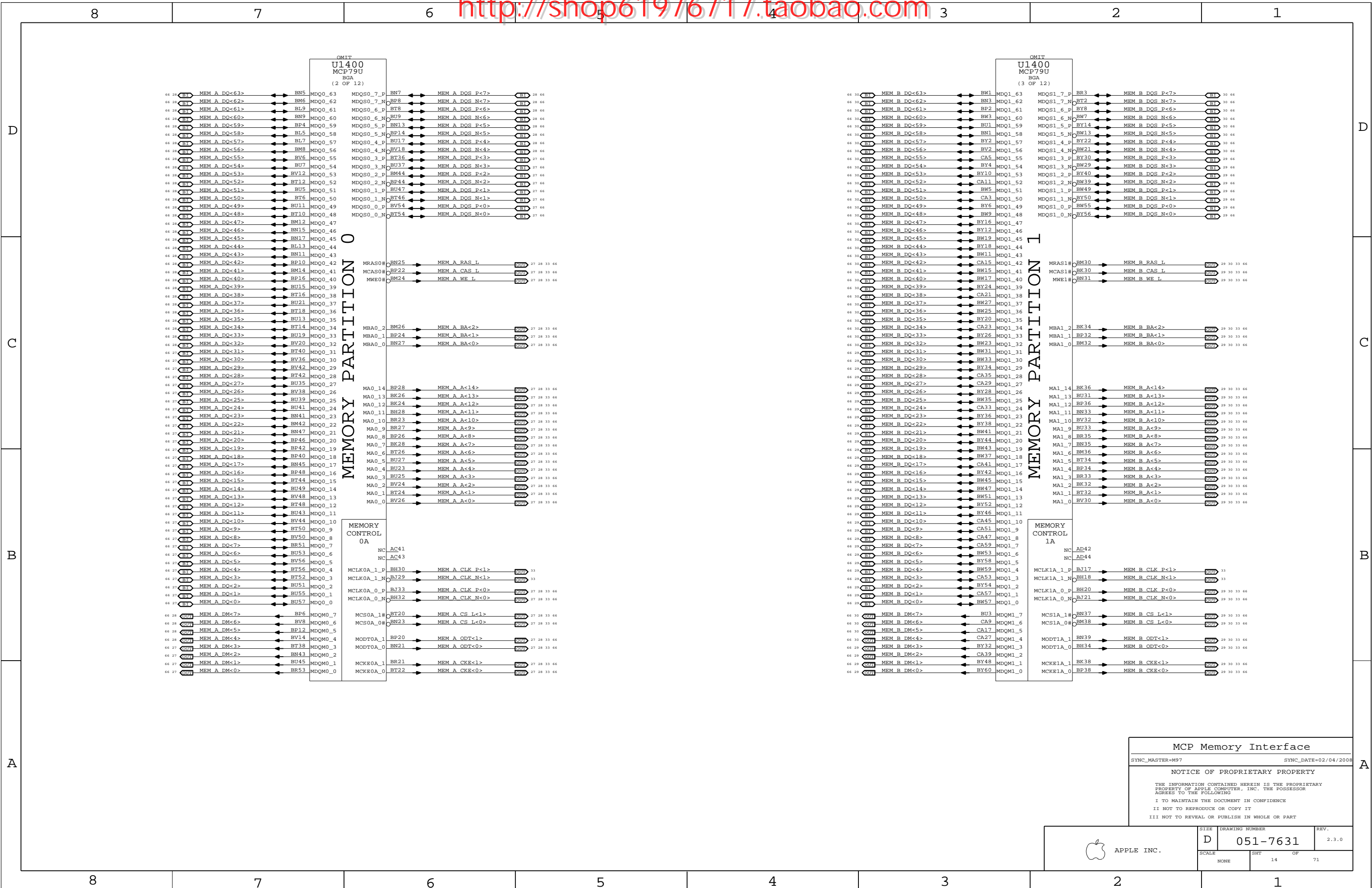
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MCP Memory Interface

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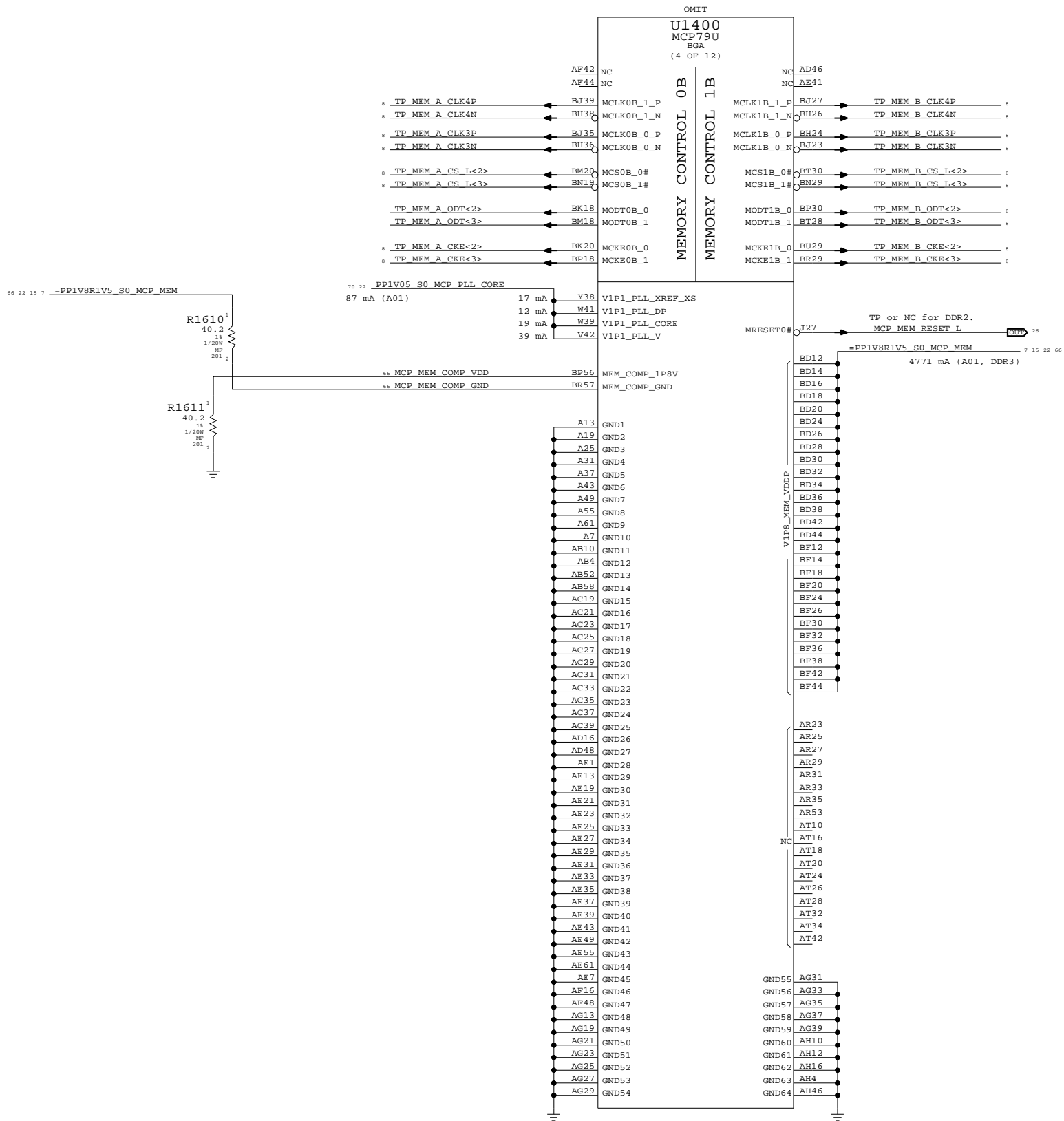
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MCP Memory Misc

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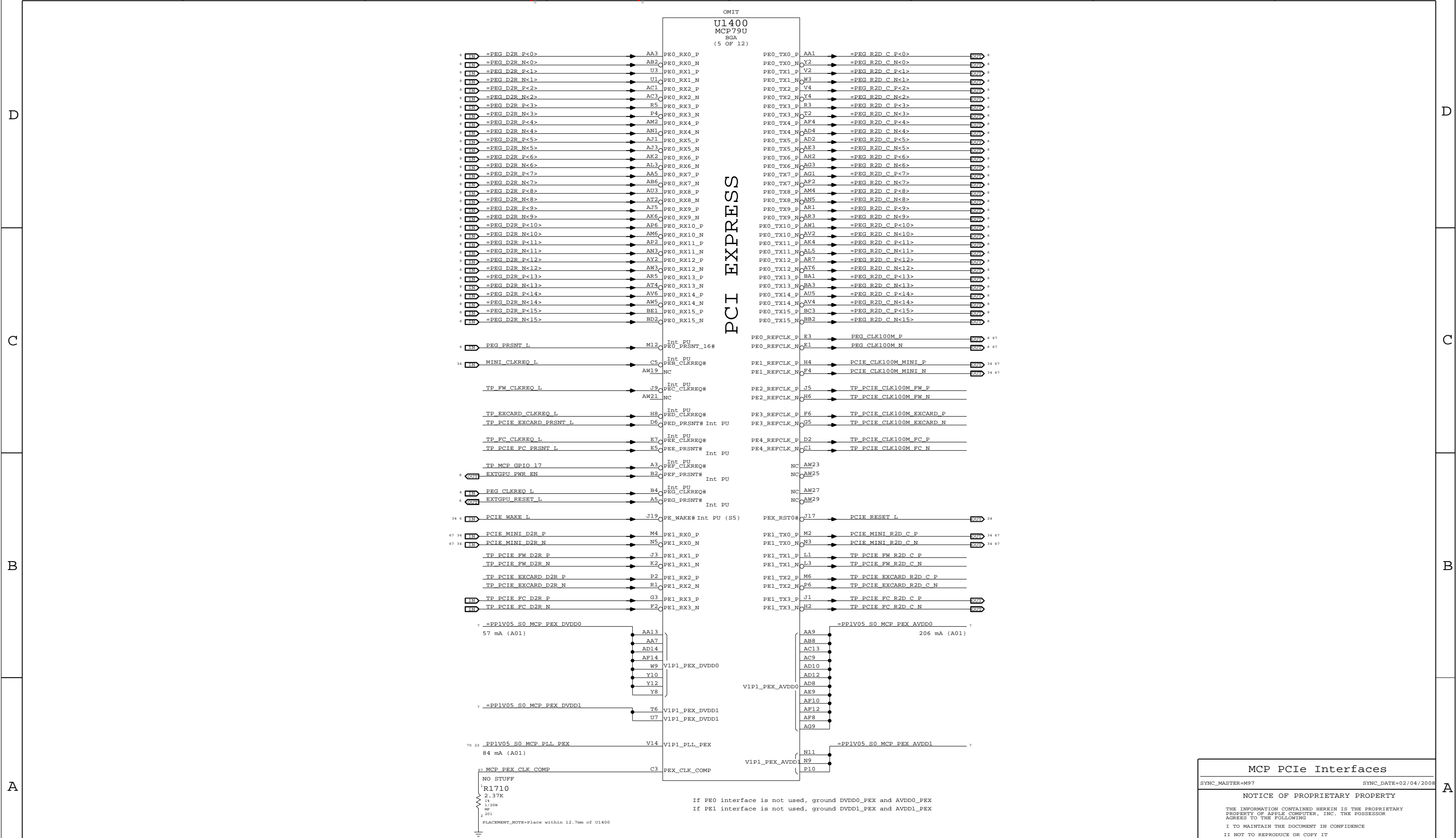
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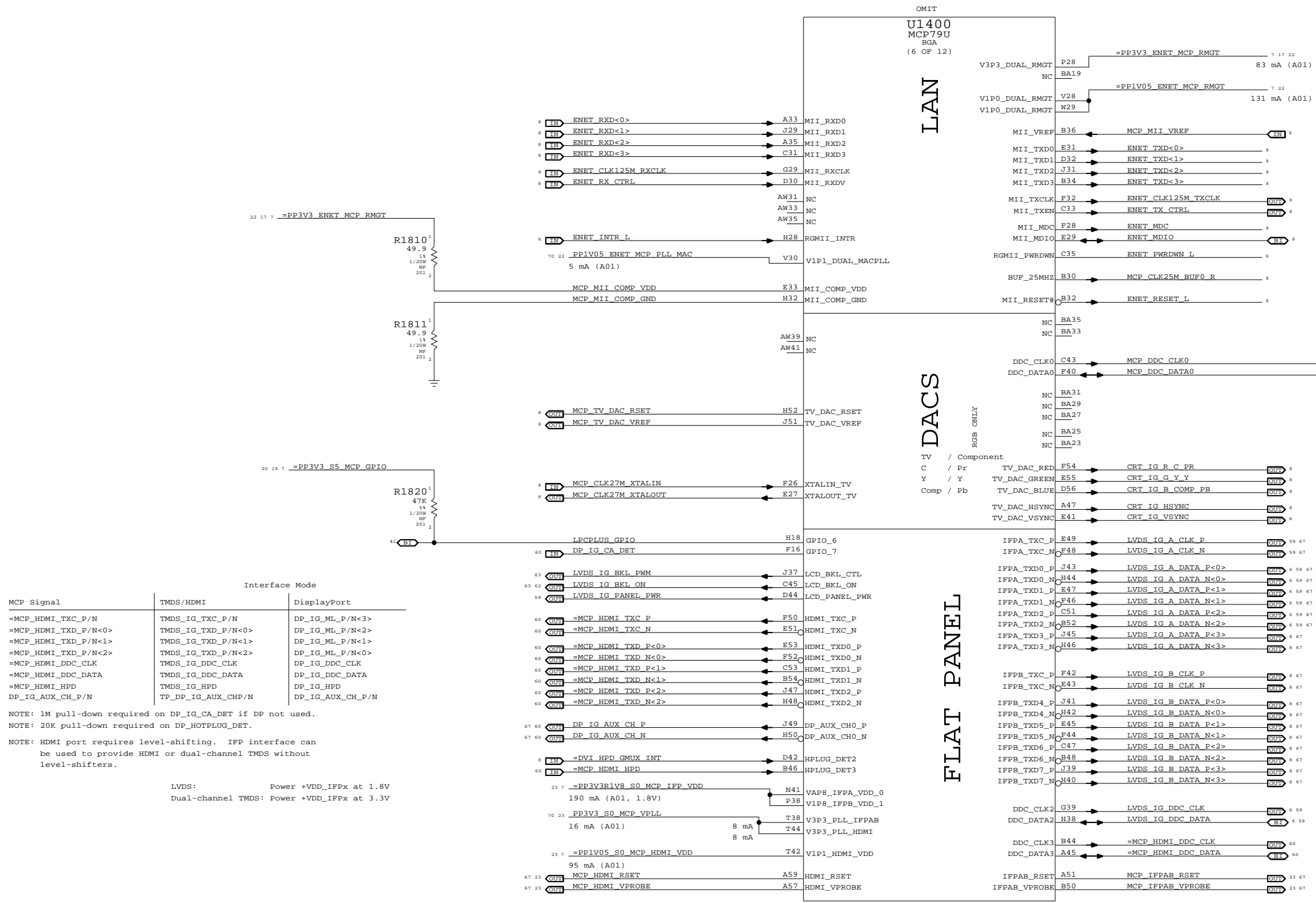
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D

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B

A



Network Interface Select	
Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable: _____
Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable: _____
Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

Interface Mode		
MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CH_P/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HOTPLUG_DET.

NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

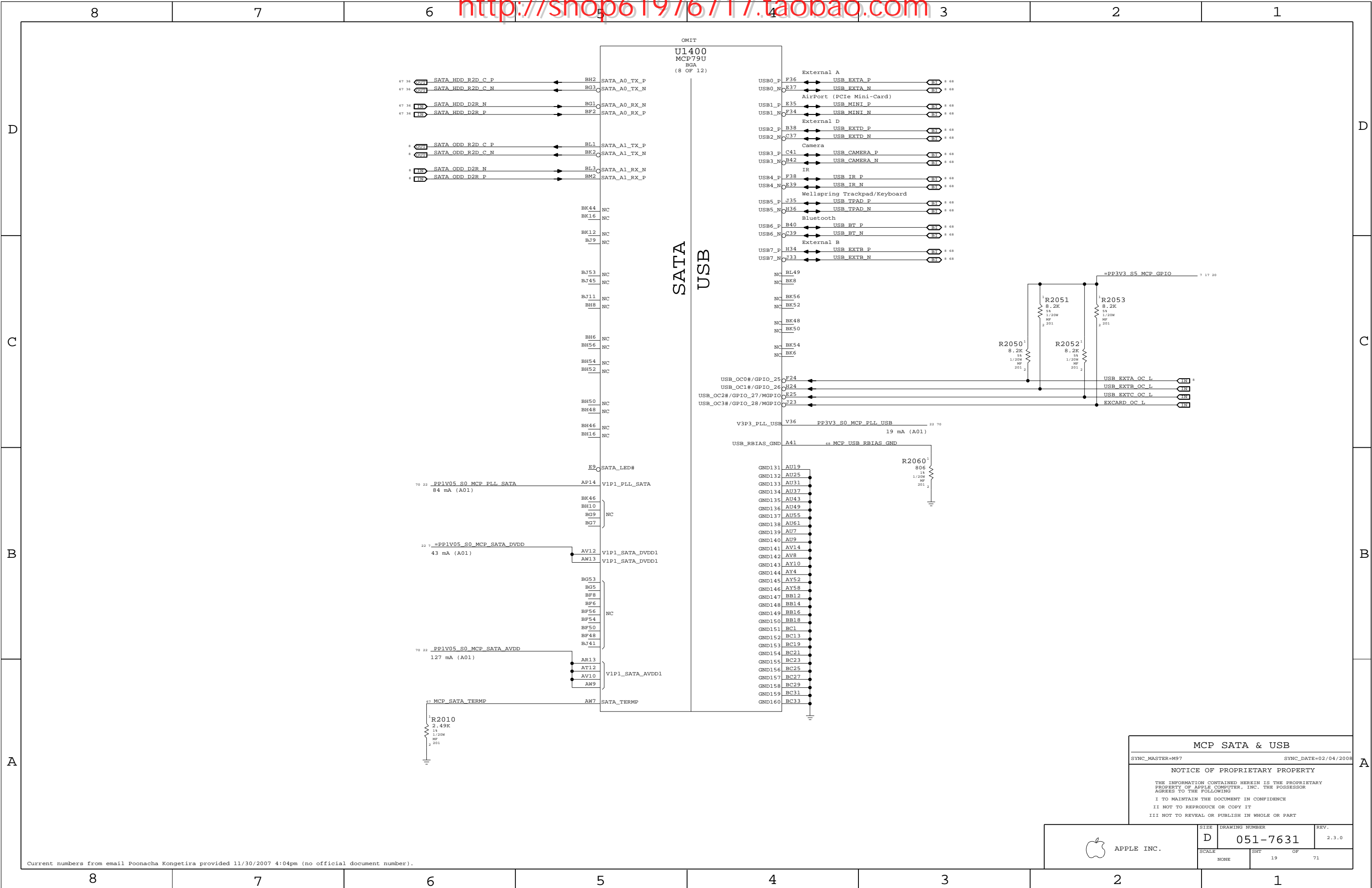
LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

MCP Ethernet & Graphics	
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MCP SATA & USB

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

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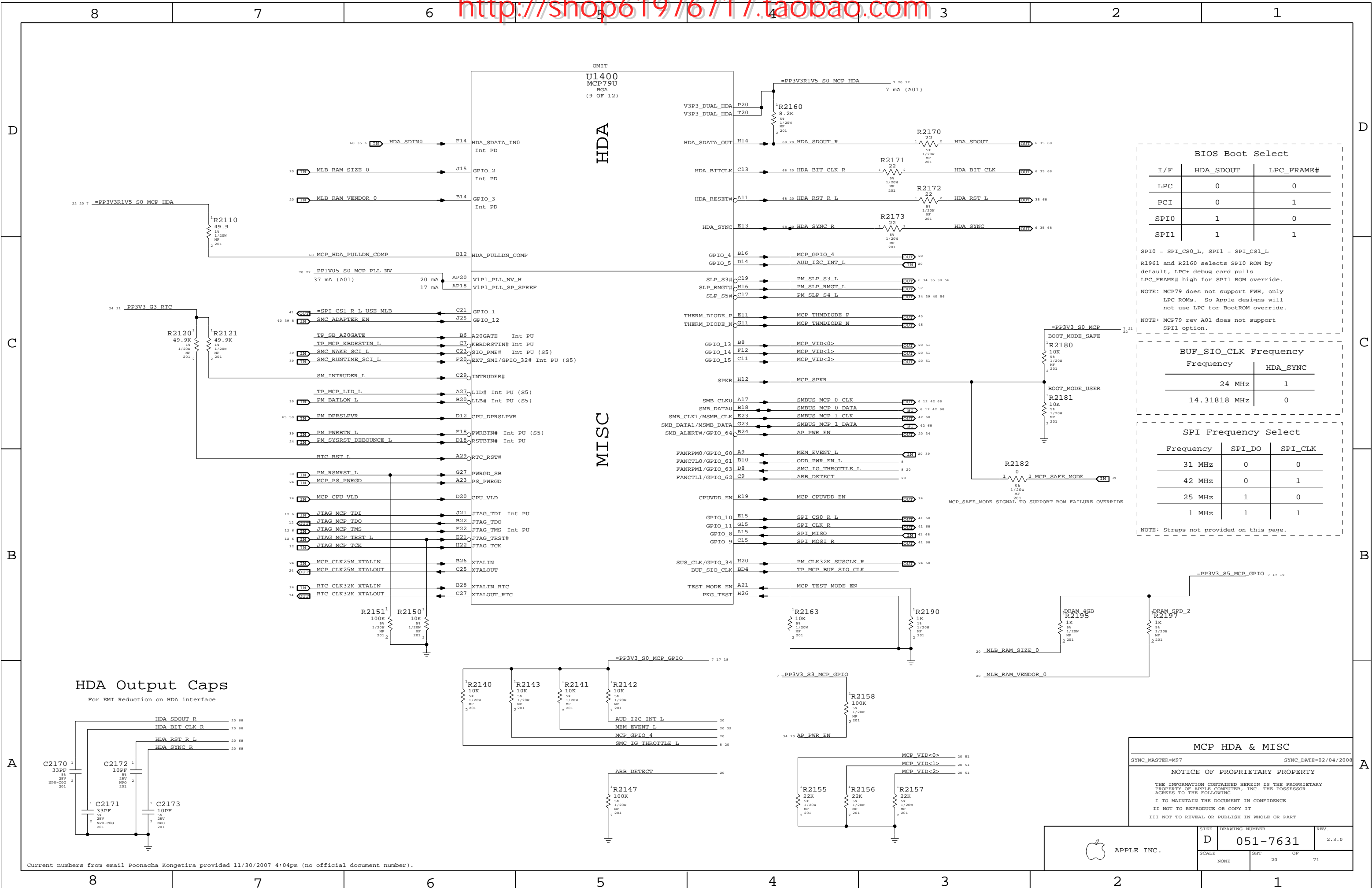
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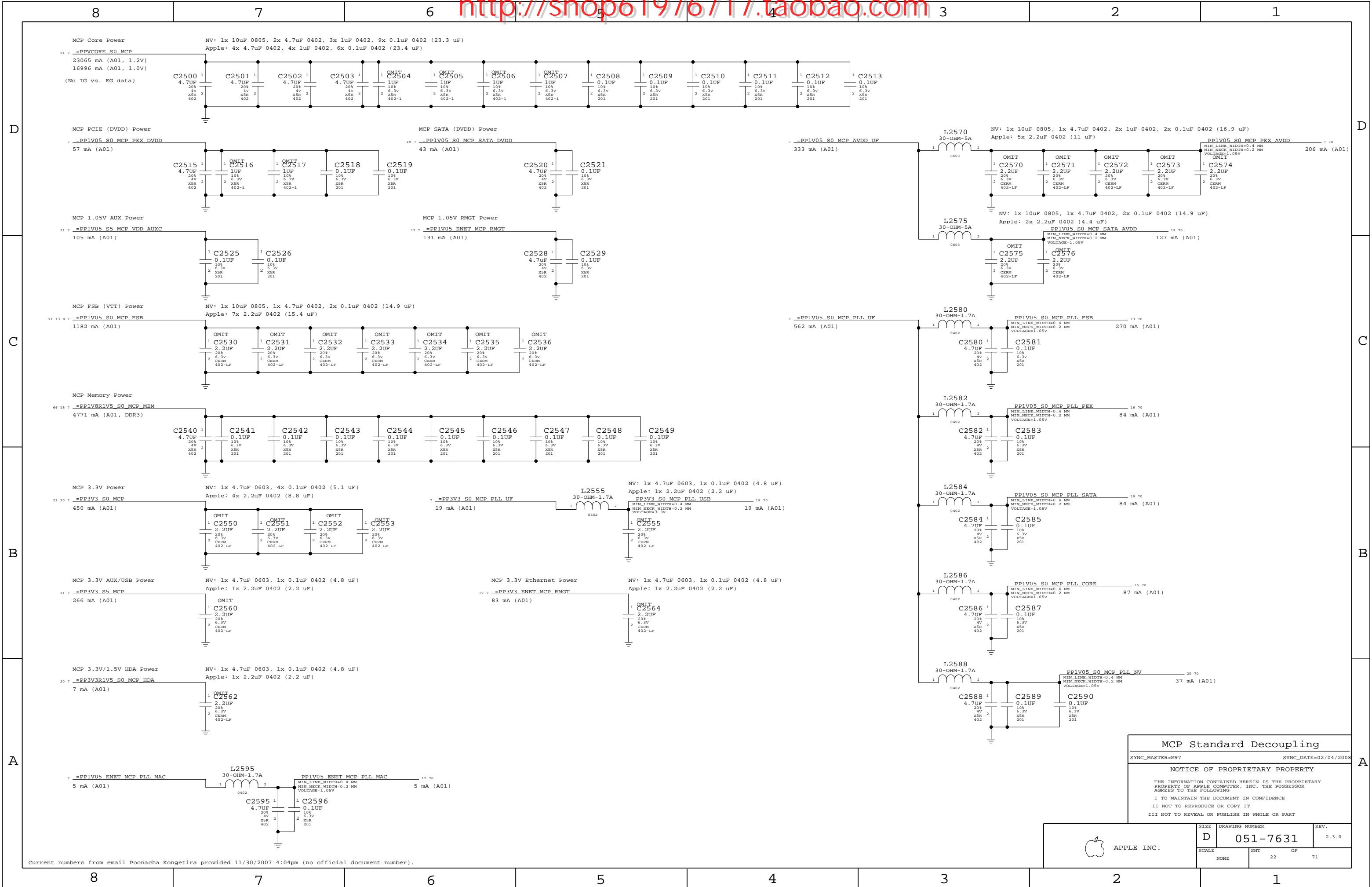
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE		SHT	OF
NONE		19	71





MCP Standard Decoupling

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

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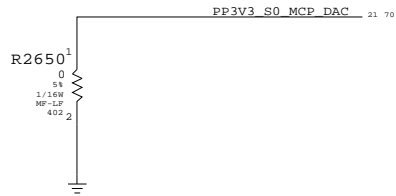
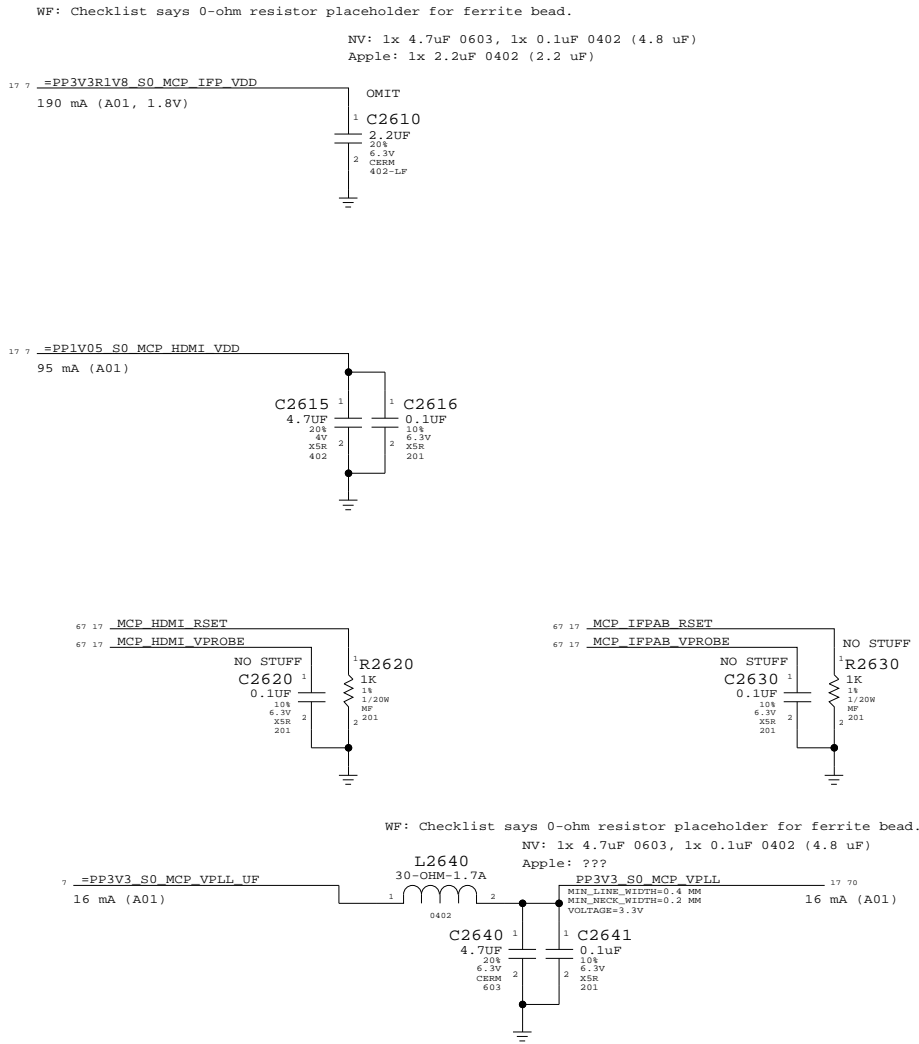
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	2.3.0
SCALE	SHT	OF
NONE	22	71



SYNC FROM M97

MCP Graphics Support

SYNC_MASTER=M97

SYNC_DATE=02/04/2008

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APPLE INC.

SIZE

D

DRAWING NUMBER

051-7631

REV.

2.3.0

SCALE

NONE

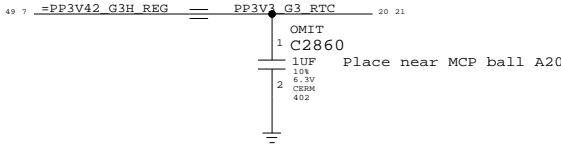
SHT

23

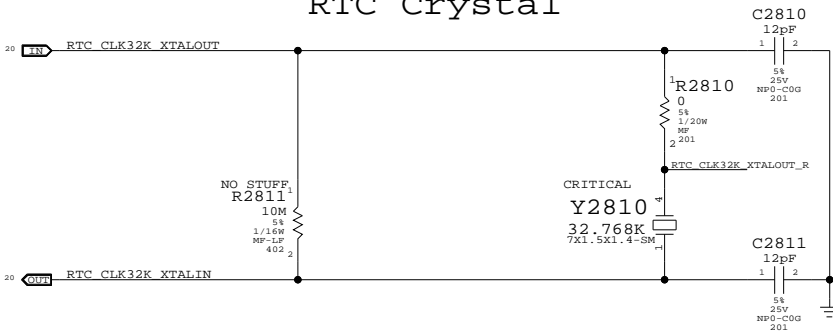
OF

71

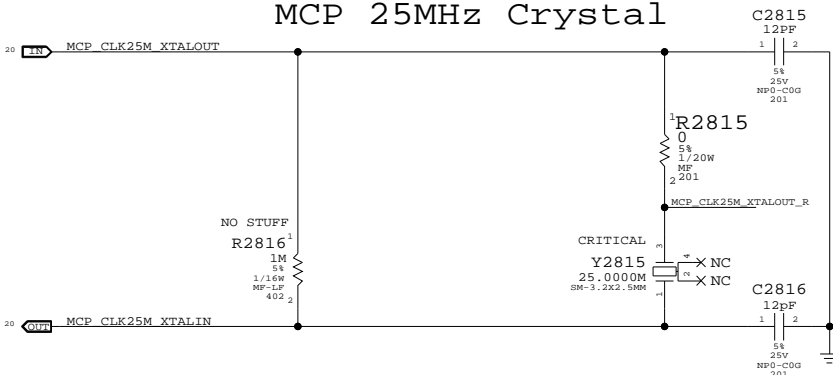
RTC Power Sources



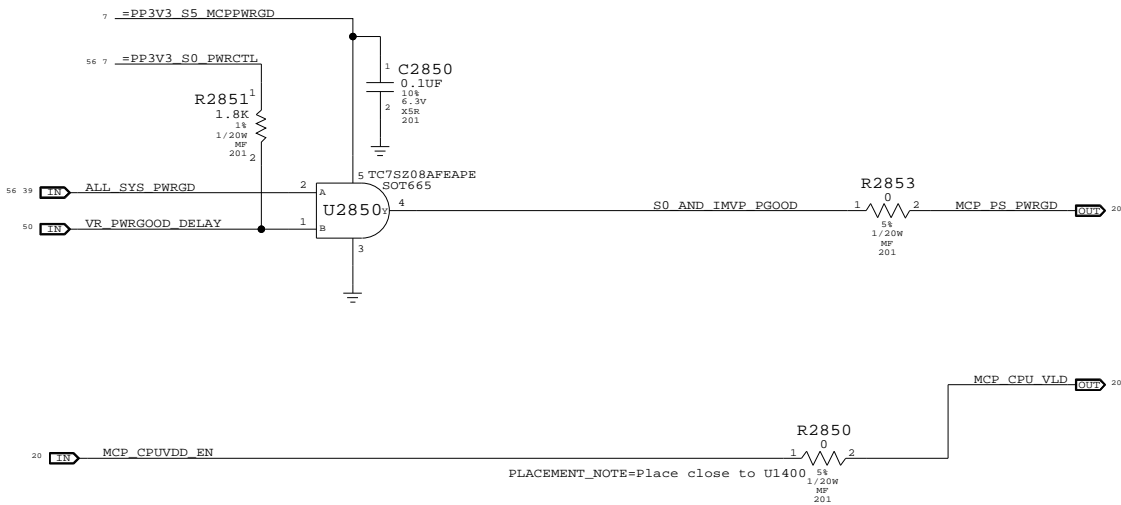
RTC Crystal



MCP 25MHz Crystal



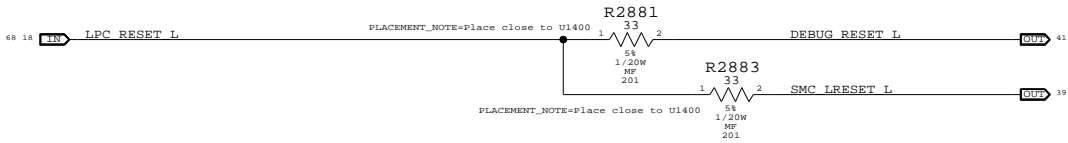
MCP S0 PWRGD & CPU_VLD



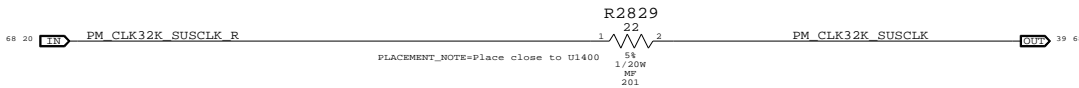
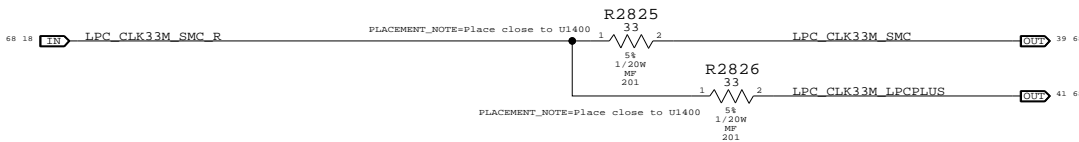
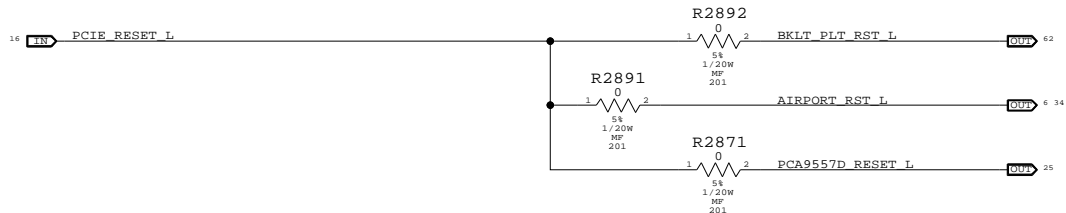
SYNC FROM M97
CHANGED RTC POWER SOURCE TO DIRECT CONNECTION
ADDED MCPSEQ_SMC LOGIC

Platform Reset Connections

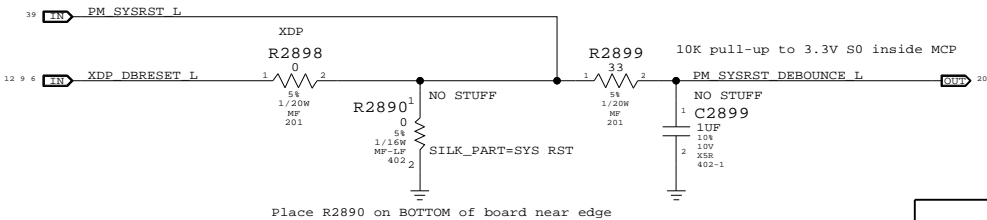
LPC Reset (Unbuffered)



PCIE Reset (Unbuffered)



Reset Button



SB Misc	
SYNC_MASTER=M97	SYNC_DATE=02/04/2008
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	2.3.0
SCALE	SHT	OF
NONE	24	71

Page Notes

Power aliases required by this page:

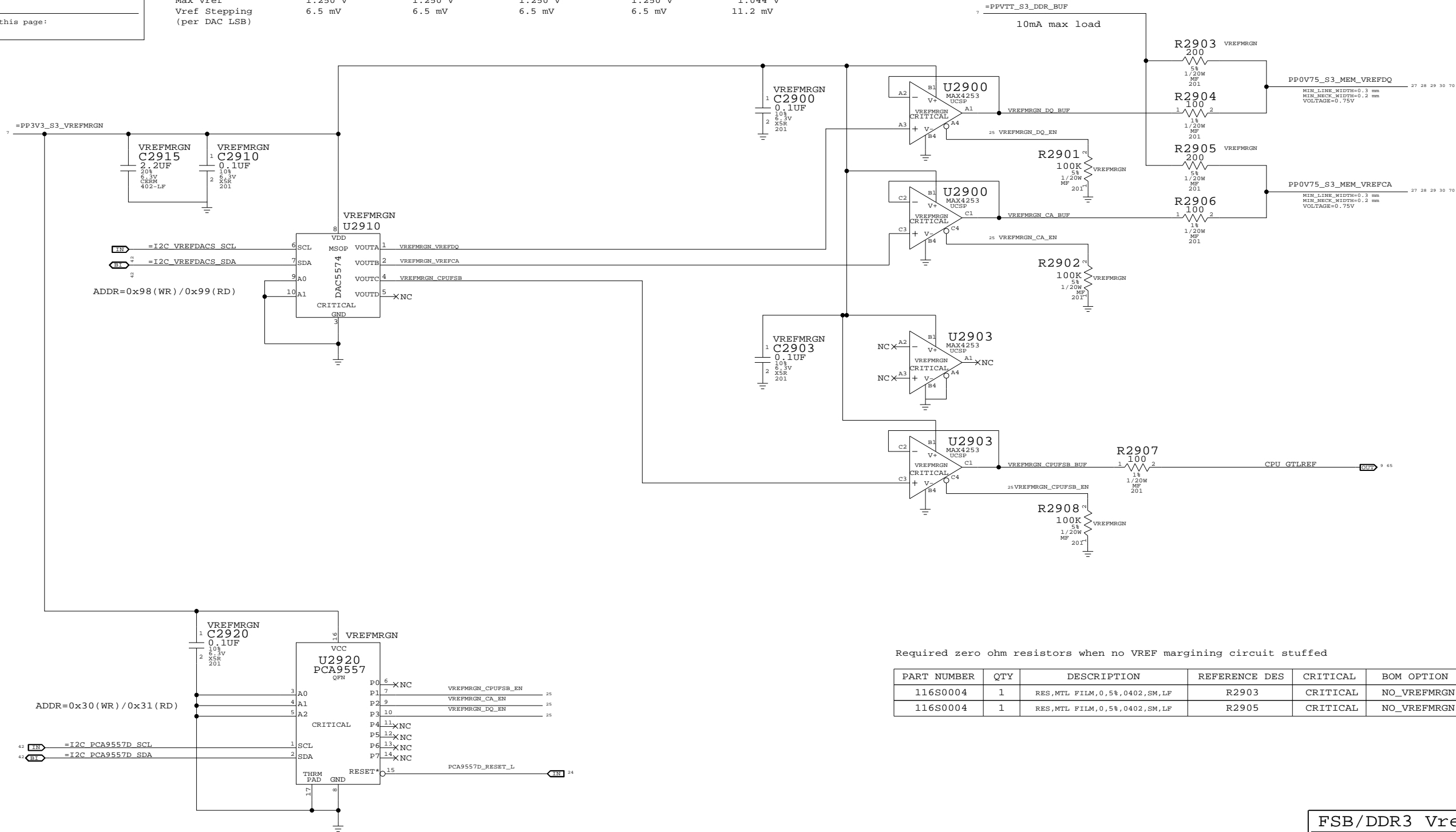
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:

- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

D	BOM options provided by this page: VREFMRGN
---	--

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF
DAC channel	A	B	A	B	C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN

FSB/DDR3 Vref Margining


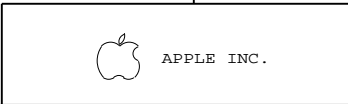
SYNC_MASTER=BEN SYNC_DATE=01/15/2008

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SIZE D	DRAWING NUMBER 051-7631	REV. 2.3.0
SCALE NONE	SHT 25	OF 71

SIZE D	DRAWING NUMBER 051-7631	REV. 2.3.0
SCALE NONE	SHT 25	OF 71

SIZE D	DRAWING NUMBER 051-7631	REV. 2.3.0
SCALE NONE	SHT 25	OF 71

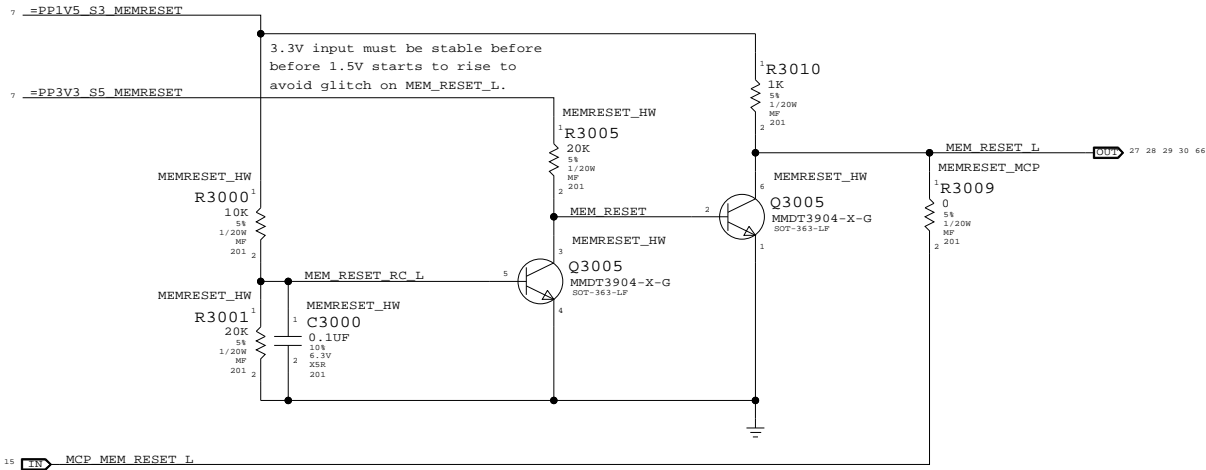
SIZE D	DRAWING NUMBER 051-7631	REV. 2.3.0
SCALE NONE	SHT 25	OF 71

SIZE D	DRAWING NUMBER 051-7631	REV. 2.3.0
SCALE NONE	SHT 25	OF 71

SIZE D	DRAWING NUMBER 051-7631	REV. 2.3.0
SCALE NONE	SHT 25	OF 71

DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



DDR3 Support

SYNC_MASTER=T18_MLB SYNC_DATE=01/30/2008


NOTICE OF PROPRIETARY PROPERTY

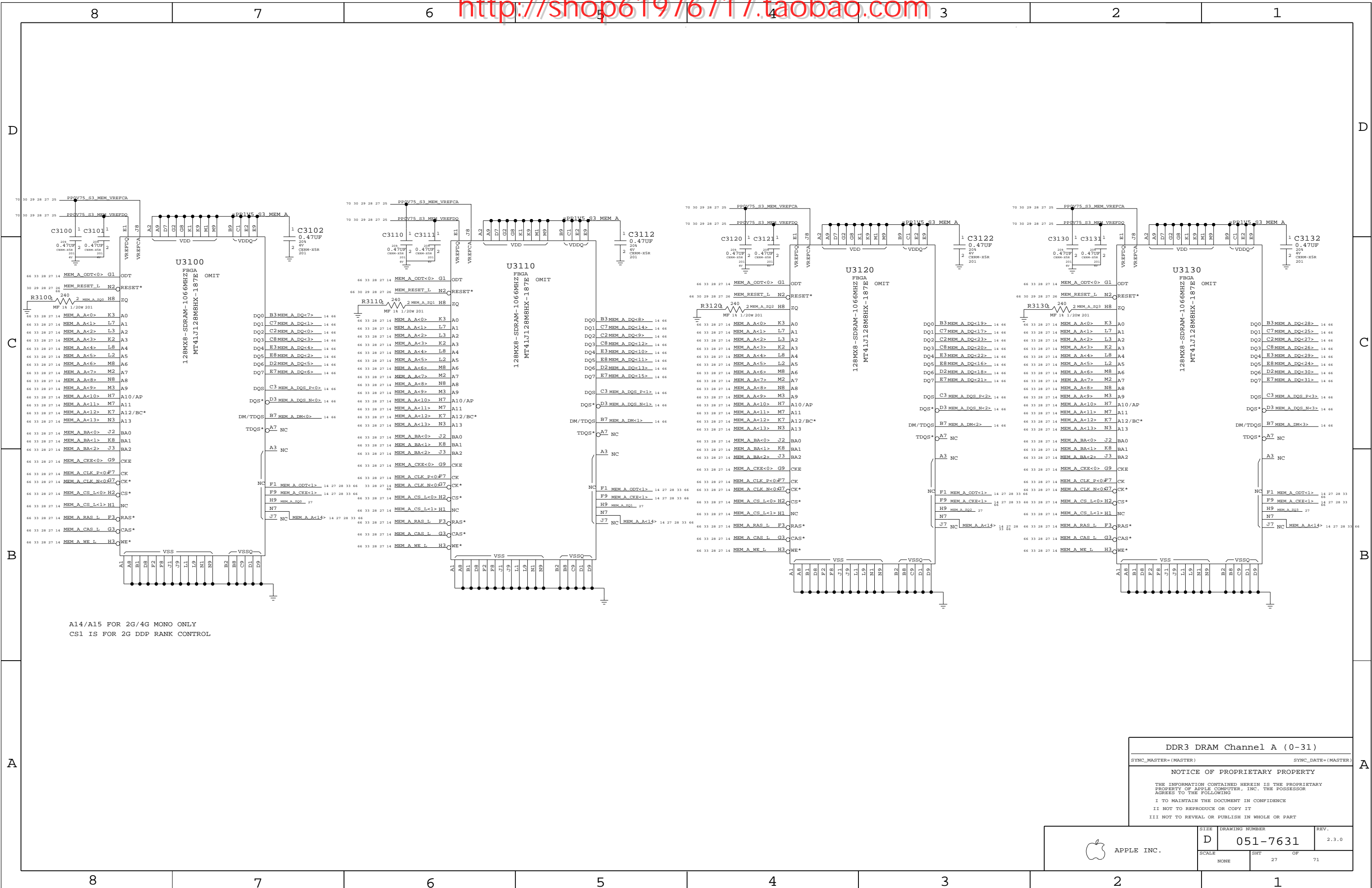
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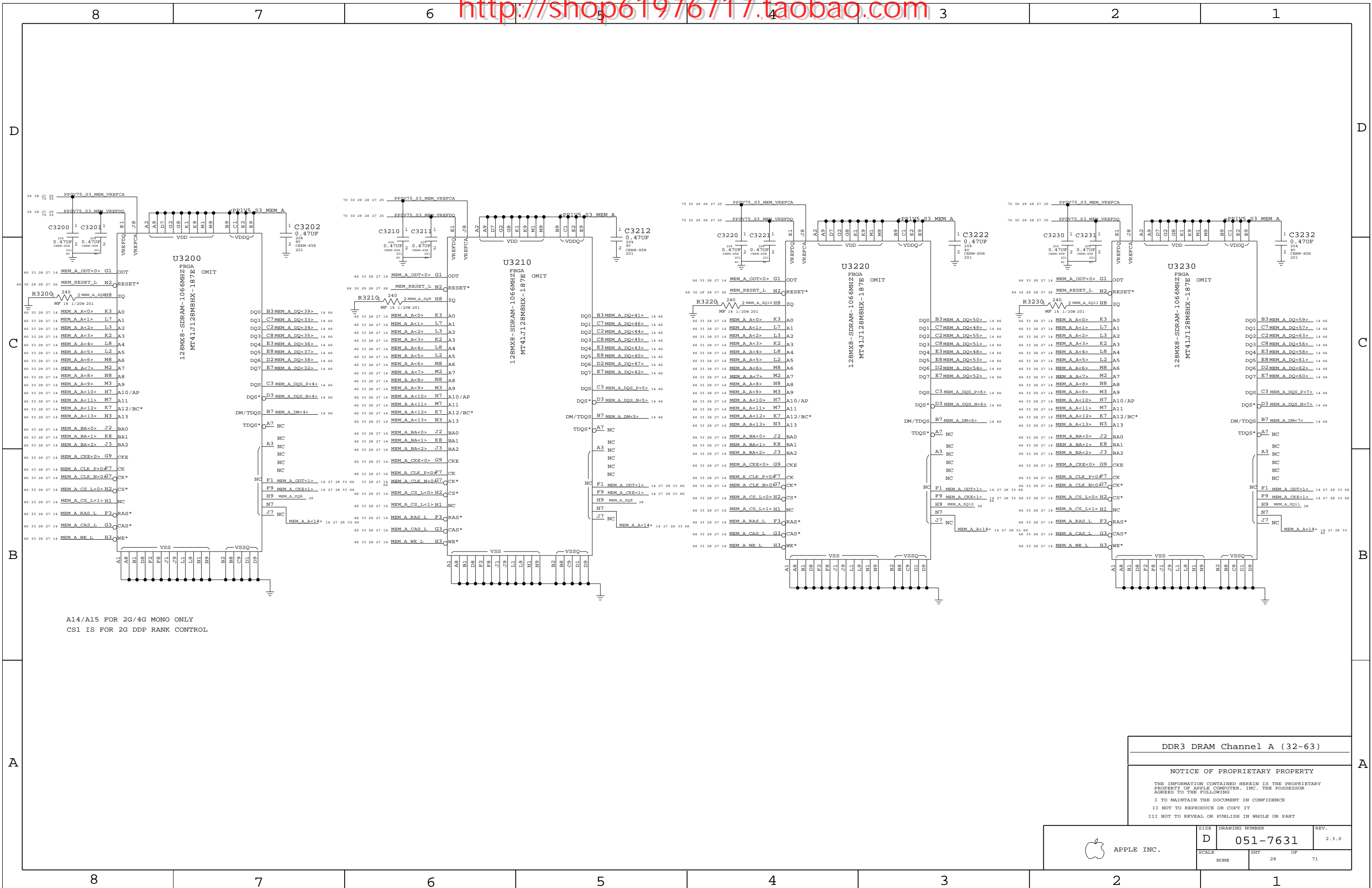
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 APPLE INC.	SIZE	DRAWING NUMBER		REV.
	D	051-7631		2.3.0
SCALE		SHT	OF	
NONE		26	71	





DDR3 DRAM Channel A (32-63)

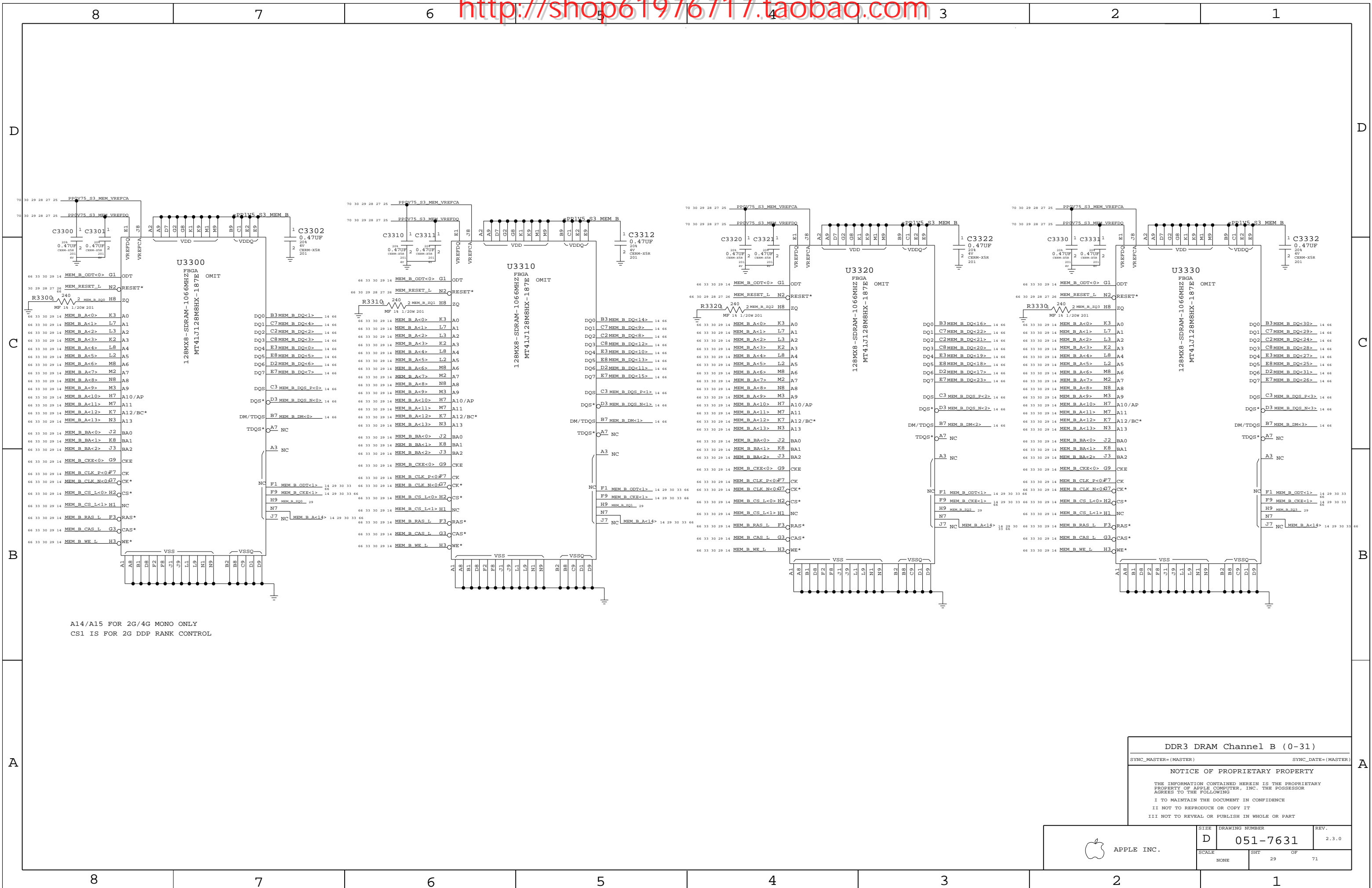
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DDR3 DRAM Channel B (0-31)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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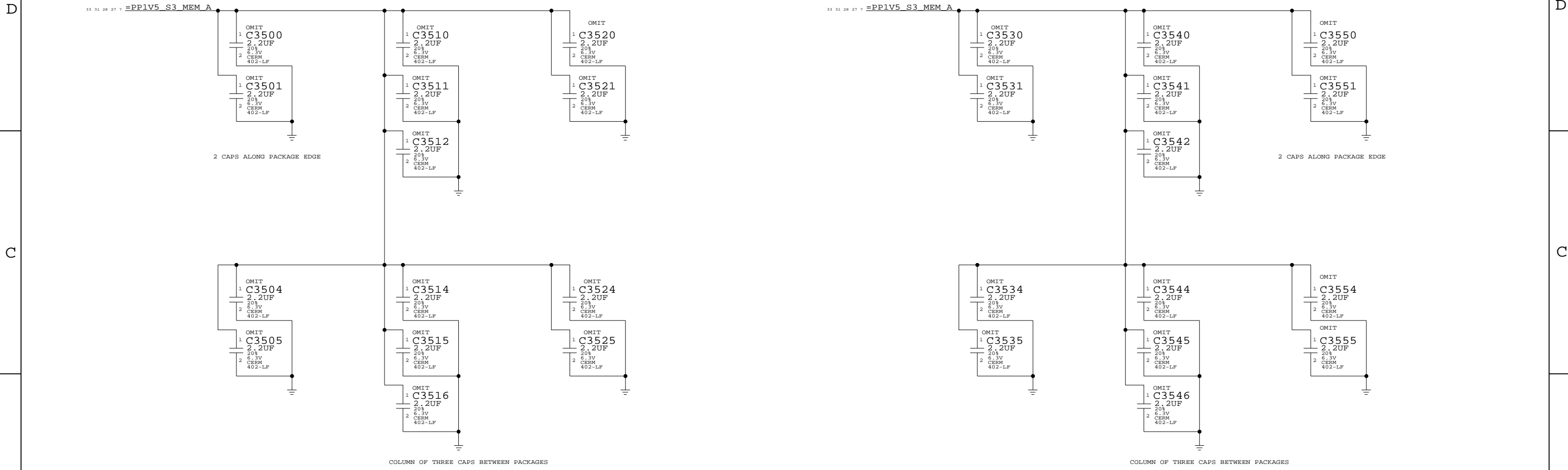
B

A

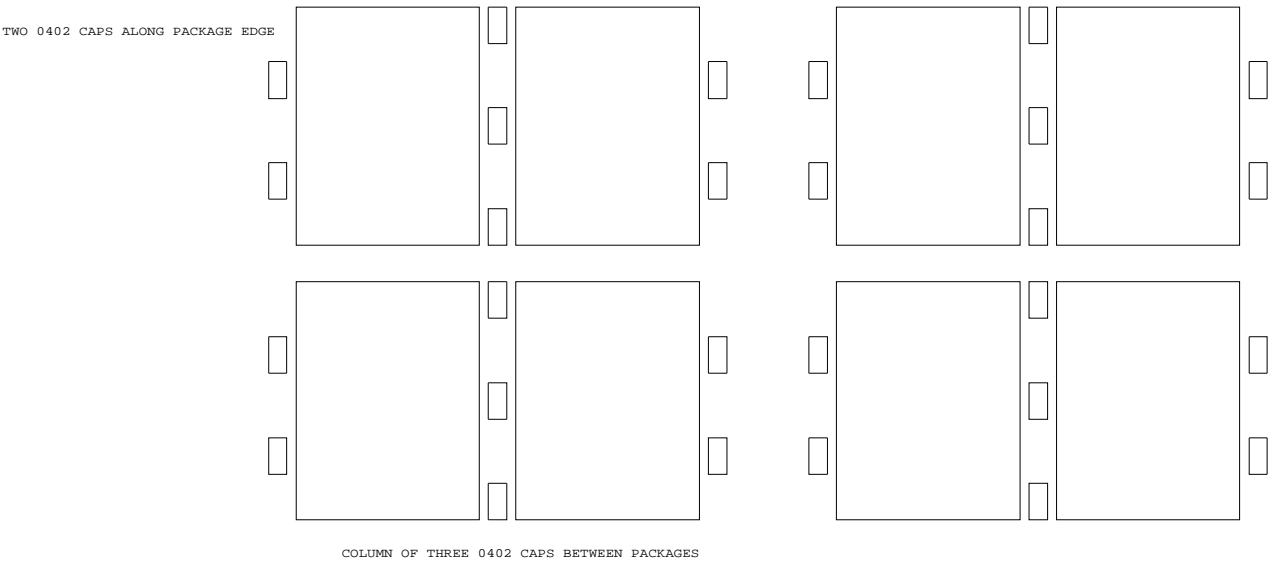
A



SCALE	SHT	OF
NONE	30	71



APPROXIMATE CAP ARRANGEMENT



DDR BYPASSING 1

SYNC_MASTER=MEMORY SYNC_DATE=06/20/2005

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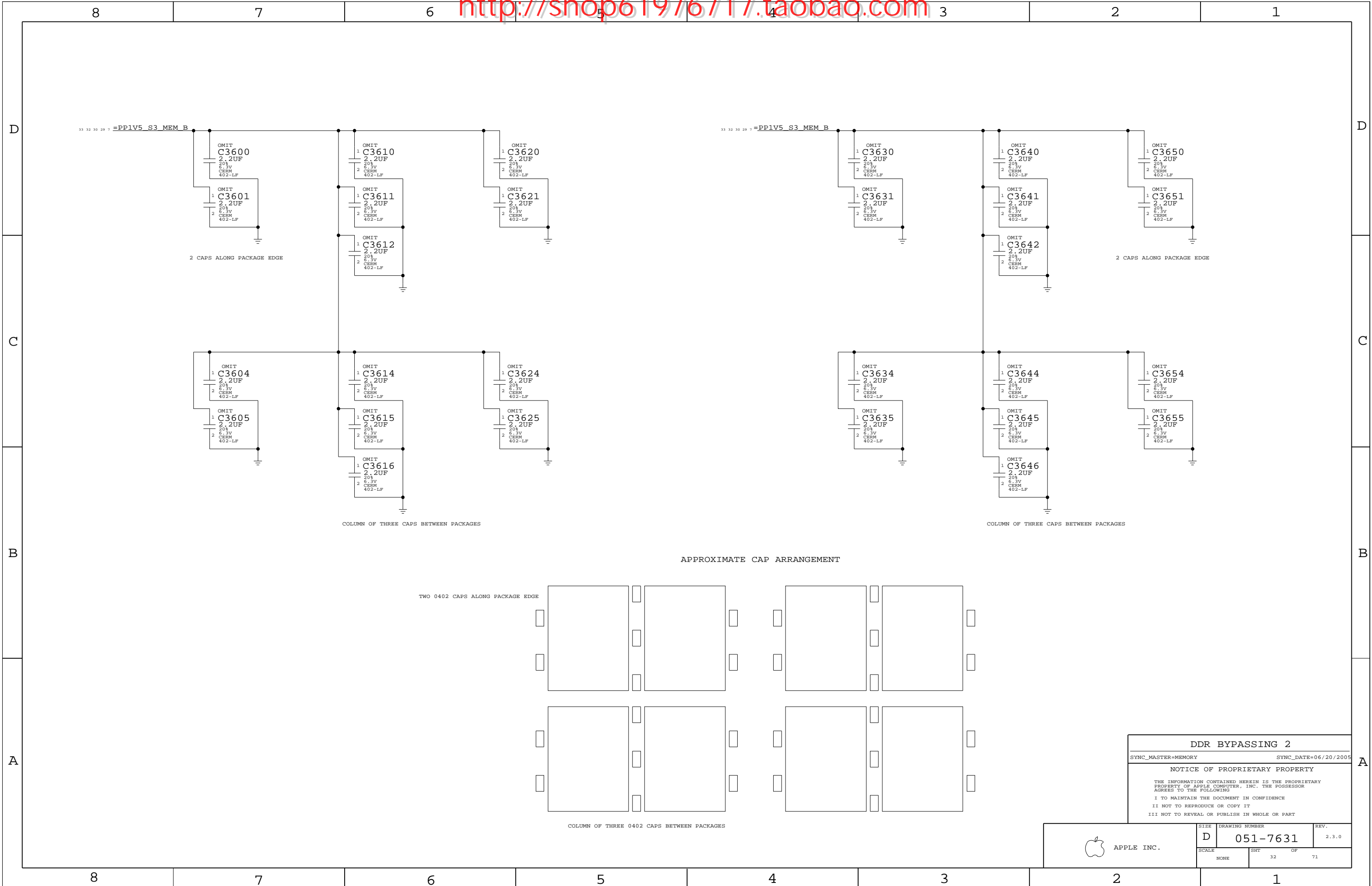
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

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APPLE INC.

SIZE	D	DRAWING NUMBER	051-7631	REV.	2.3.0
SCALE	NONE	SHT	31	OF	71



DDR BYPASSING 2

SYNC_MASTER=MEMORY SYNC_DATE=06/20/2005

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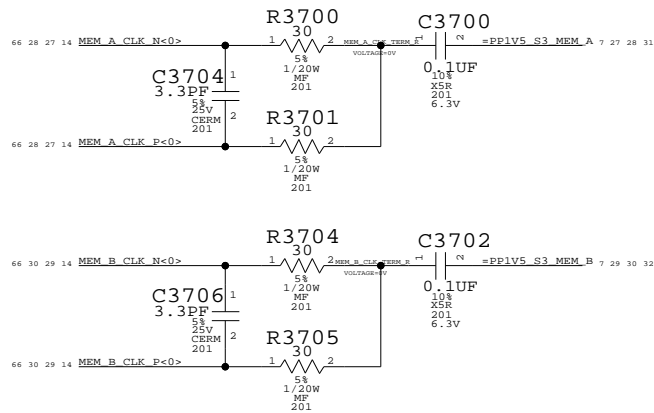
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II NOT TO REPRODUCE OR COPY IT

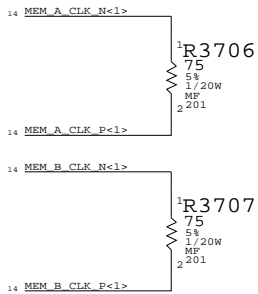
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

MEM CLOCK TERMINATION

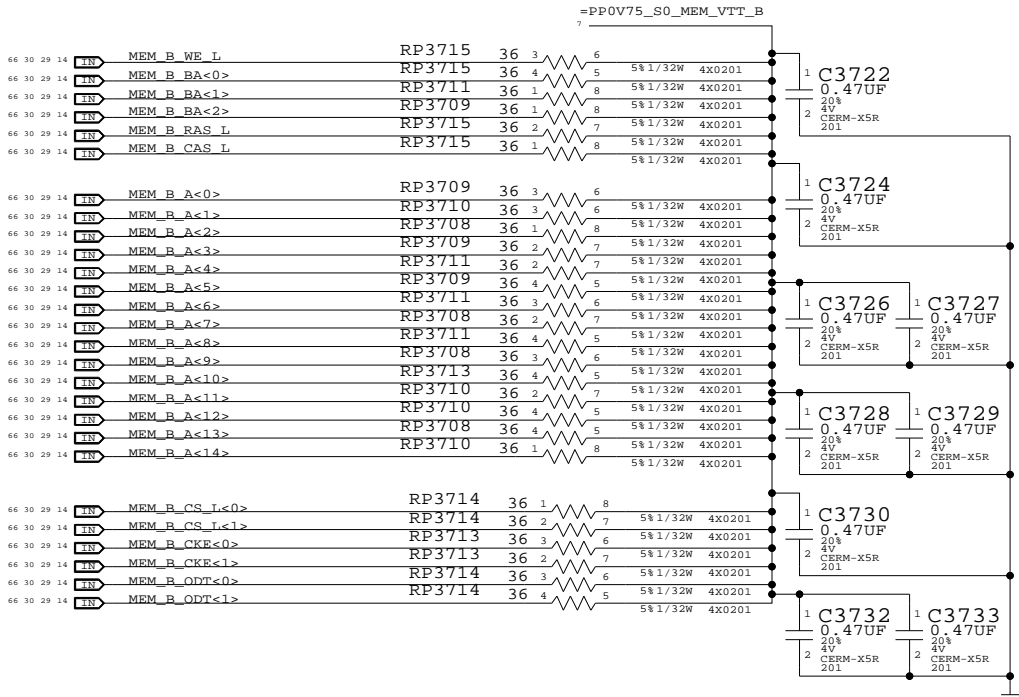
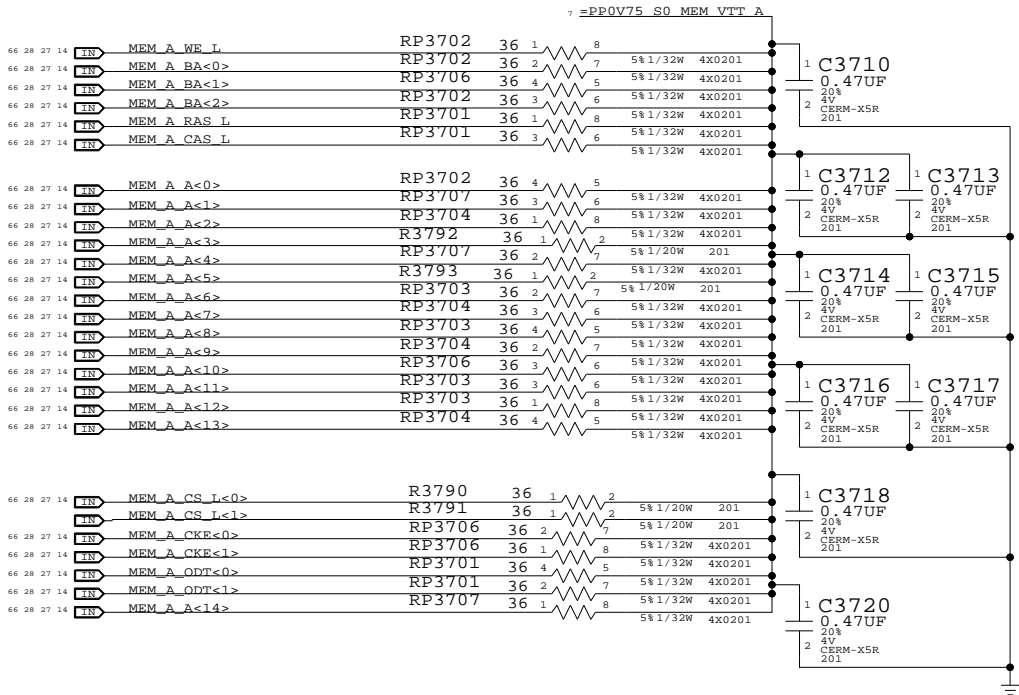
Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



Unused Clock Termination



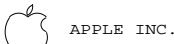
JEDEC recommends 30 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE



Memory Active Termination

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	2.3.0
SCALE	SHT	OF
NONE	33	71

8 7 6 5 4 3 2 1

D

D

C

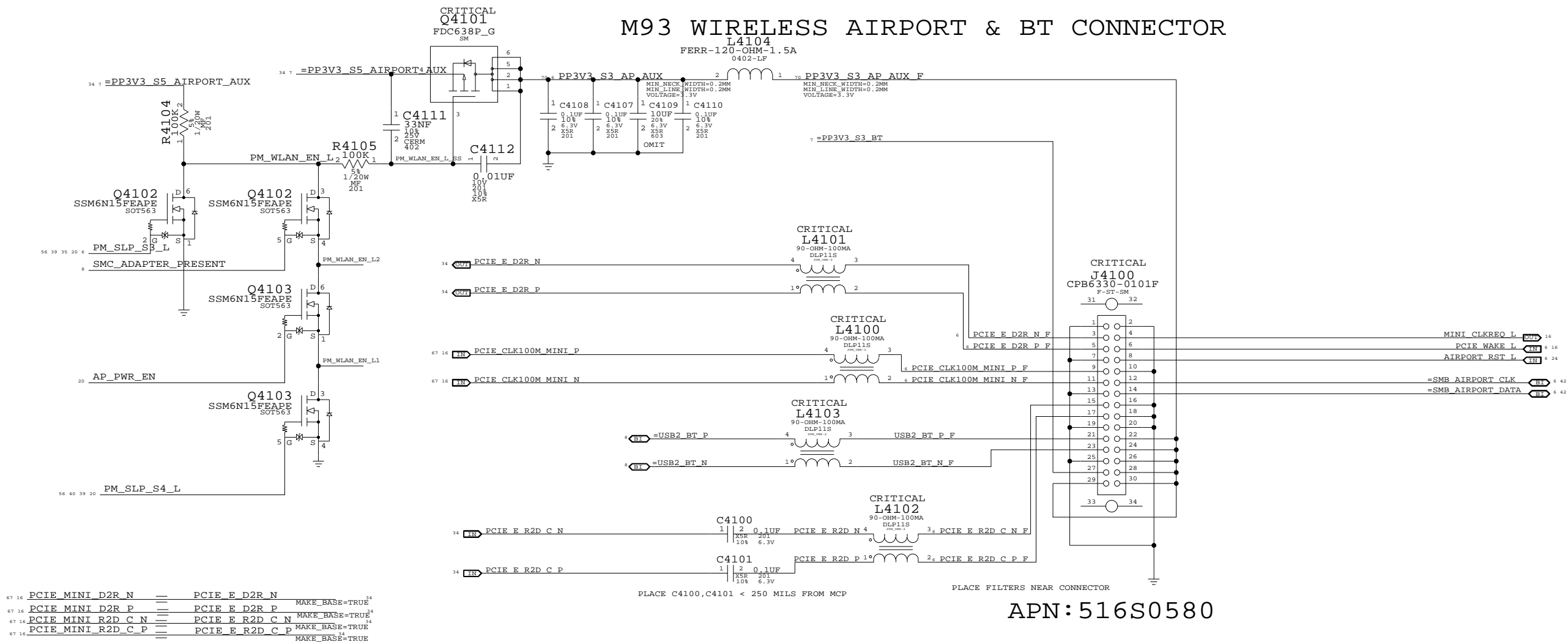
C

B

B

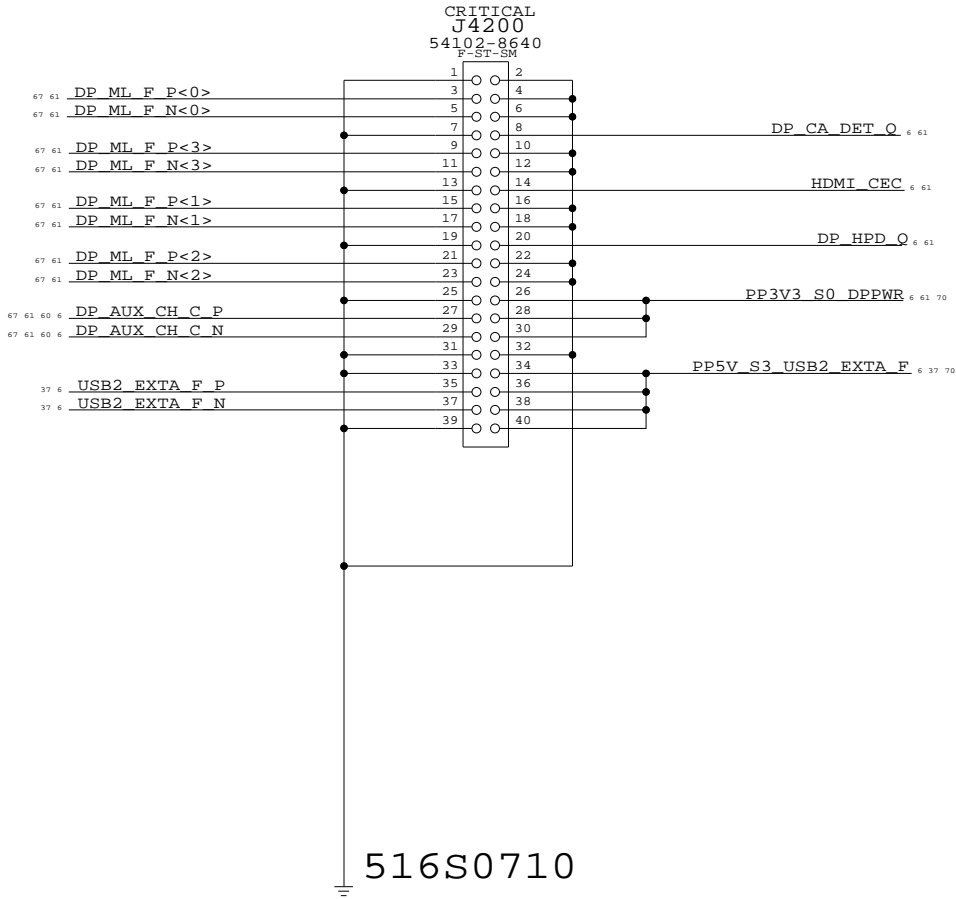
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A

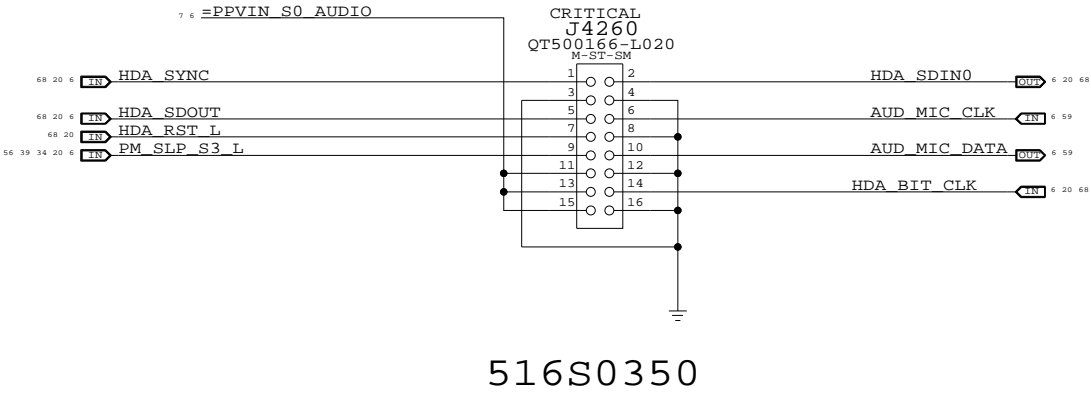


8 7 6 5 4 3 2 1

Micro-DisplayPort / USB to RIO Hatch Assembly



Audio Connector



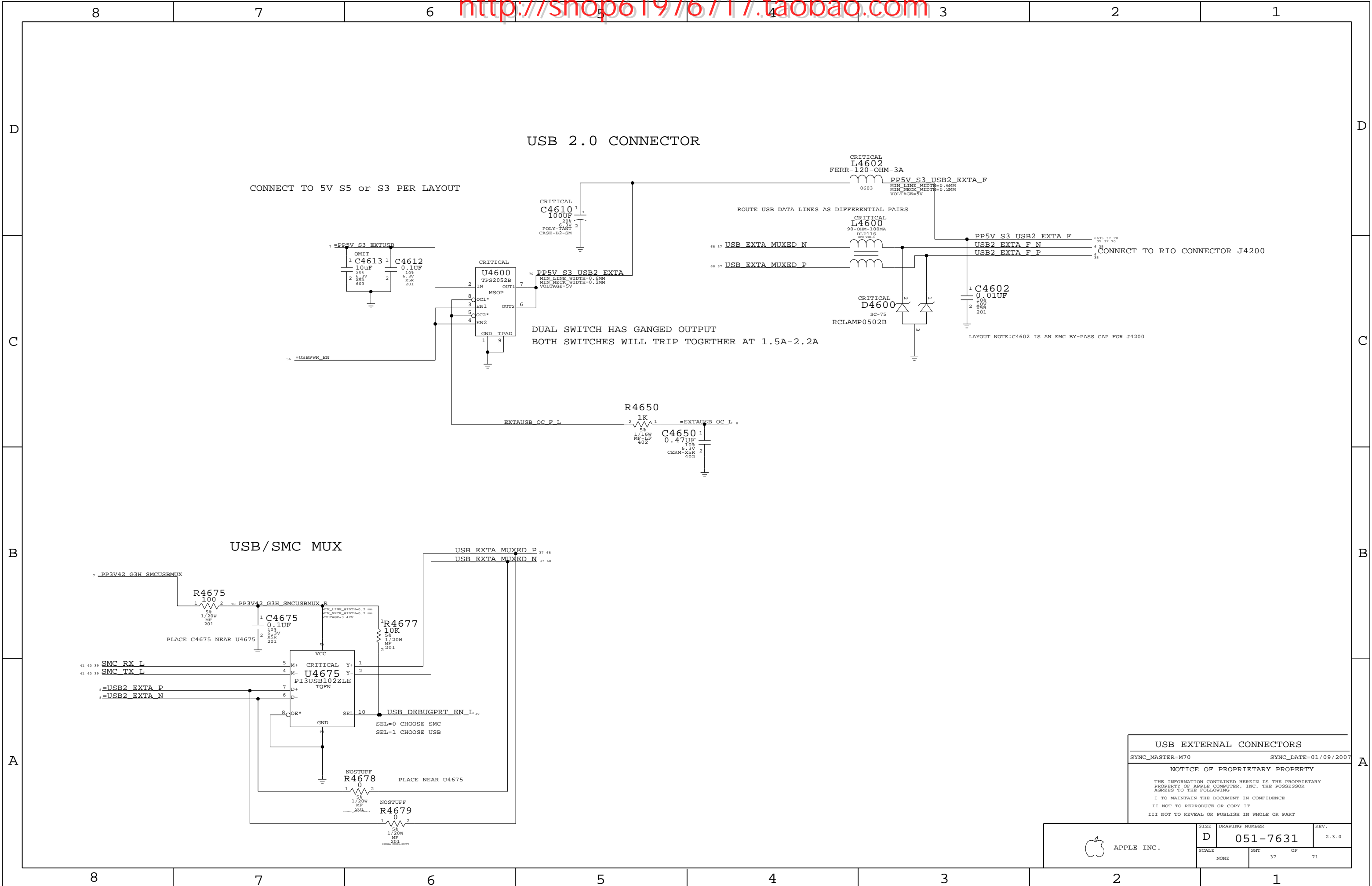
Hatch and Audio Connectors			
SYNC_MASTER=(MASTER)		SYNC_DATE=(MASTER)	
NOTICE OF PROPRIETARY PROPERTY			
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II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART			
SIZE		DRAWING NUMBER	REV.
D		051-7631	2.3.0
LE INC.			
SCALE		SHT	OF
NONE		35	71



APPLE INC.

SIZE D	DRAWING NUMBER 051-7631	REV. 2.3.0
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USB EXTERNAL CONNECTORS

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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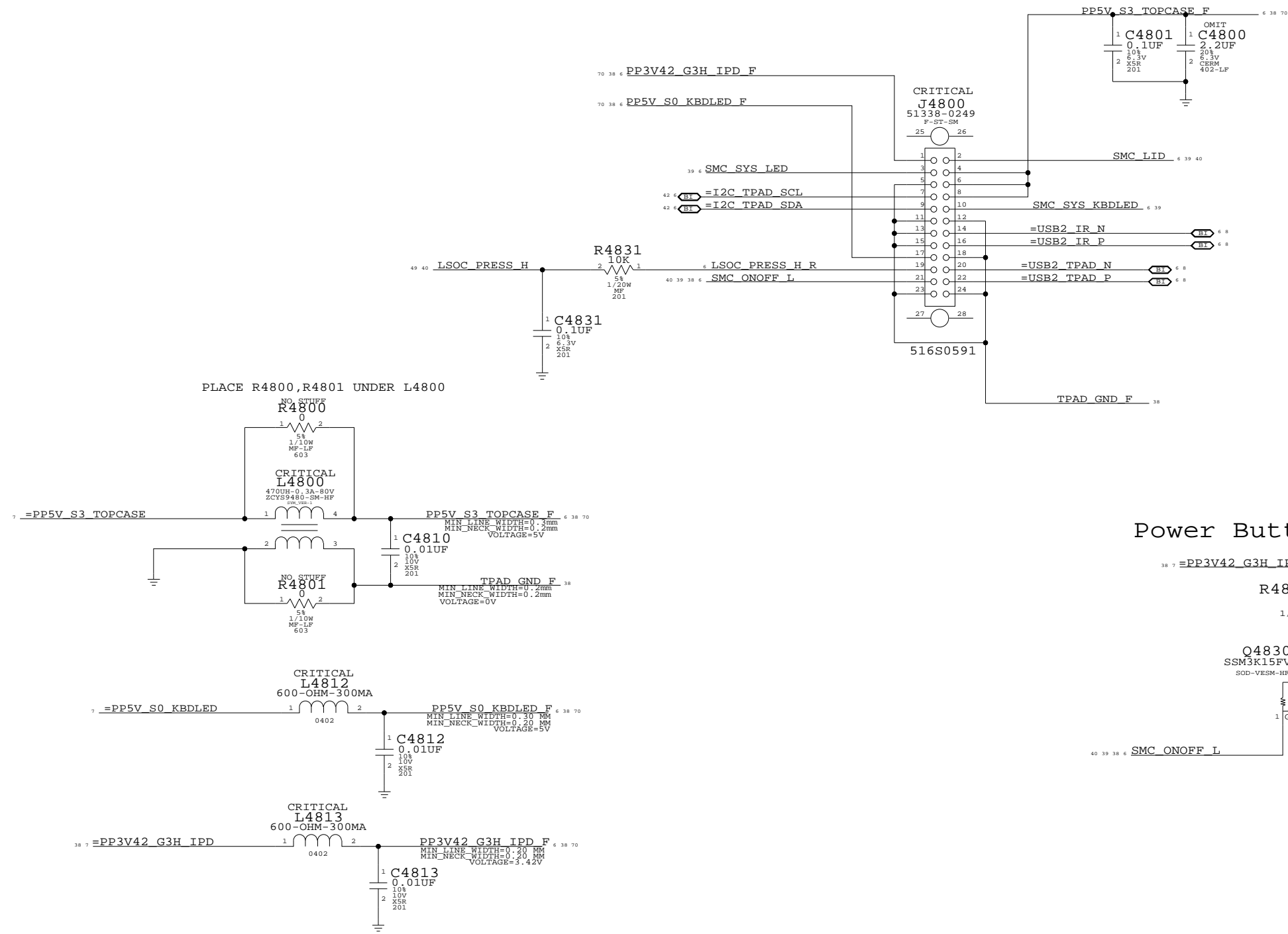
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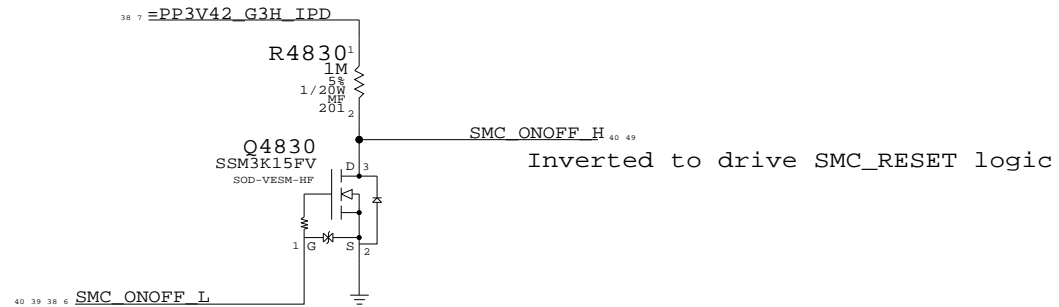
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IPD Connector



Power Button Inverter



IPD Connector		
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SIZE	DRAWING NUMBER	REV.
D	051-7631	2.3.0
SCALE	SHT	OF
NONE	38	71



APPLE INC.

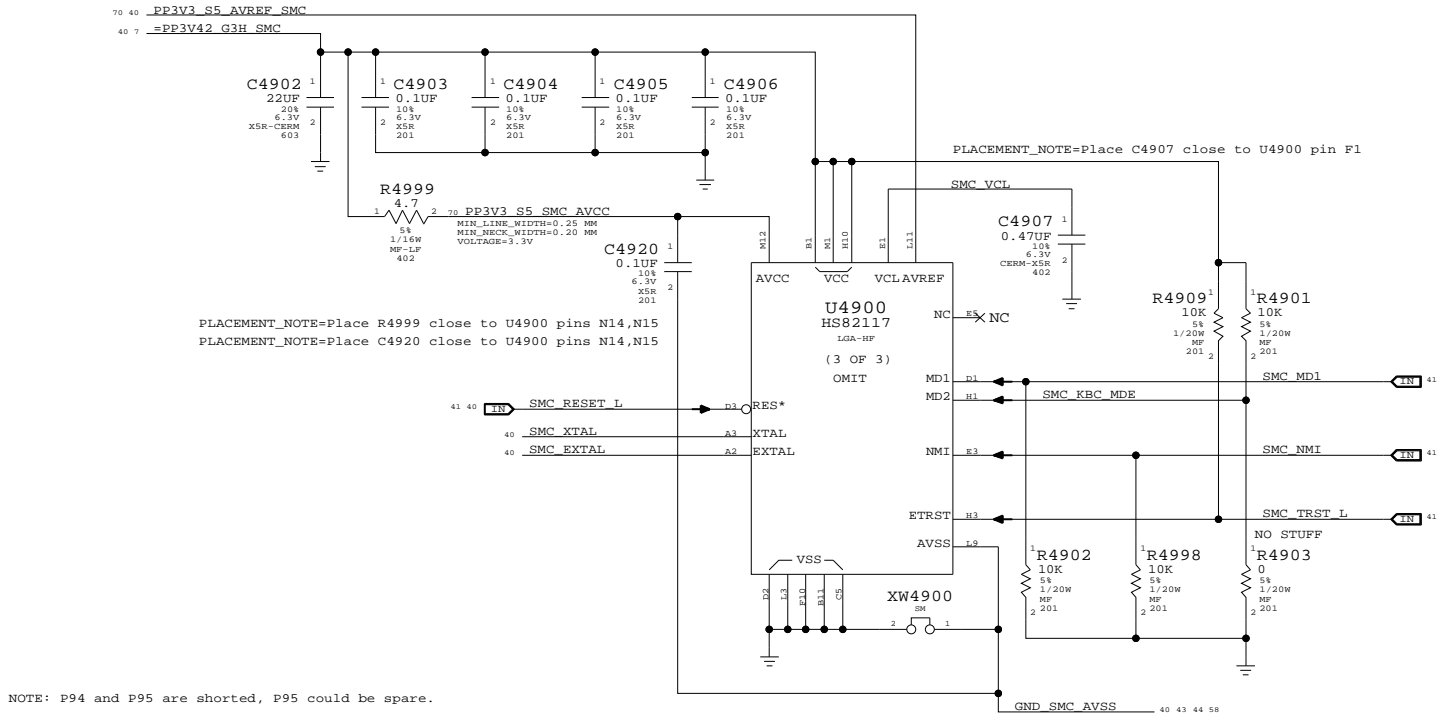
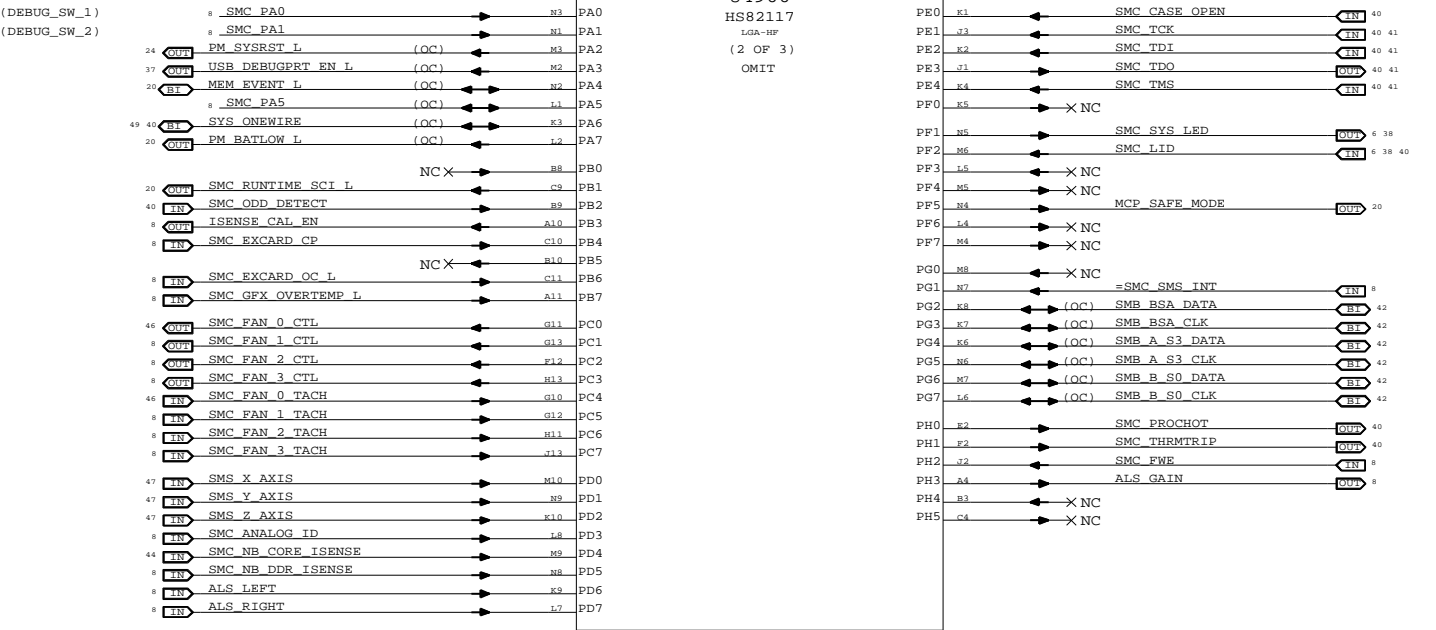
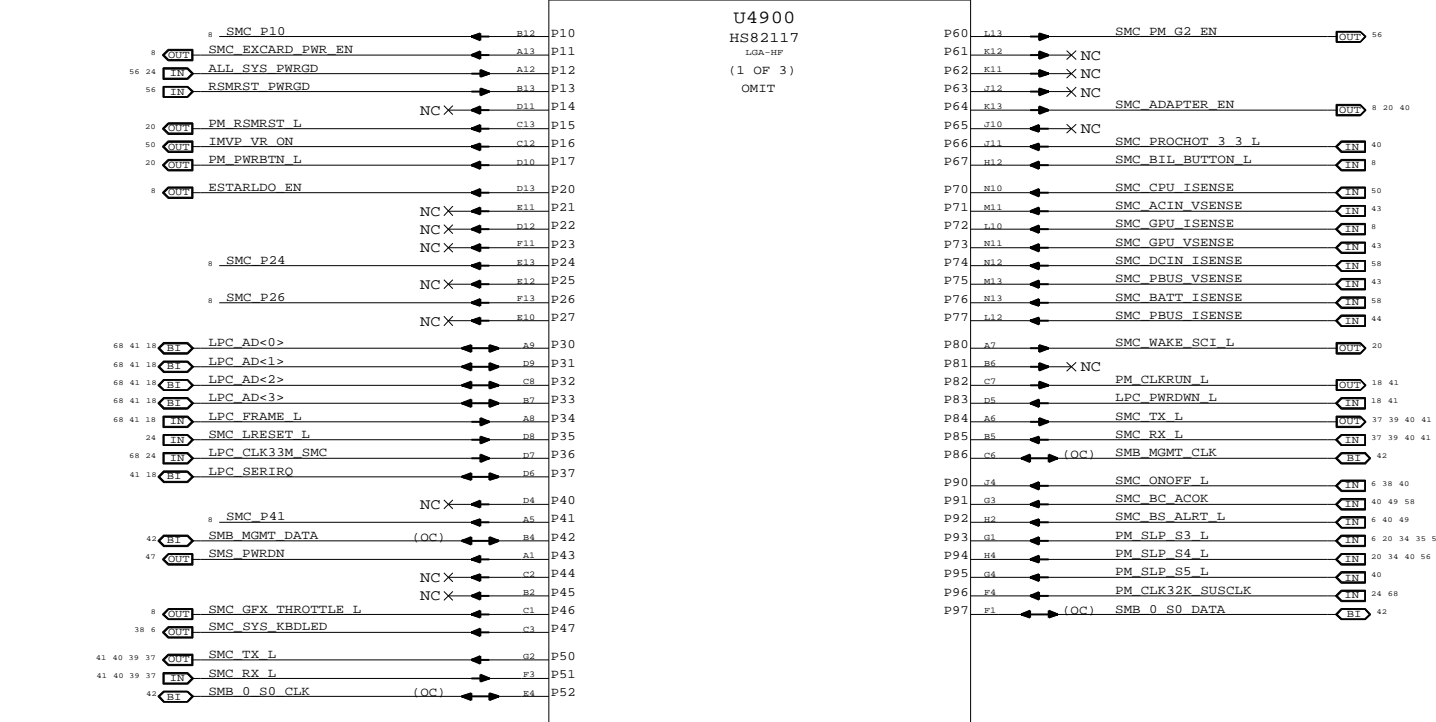
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

D

C

B

A



NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS Interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

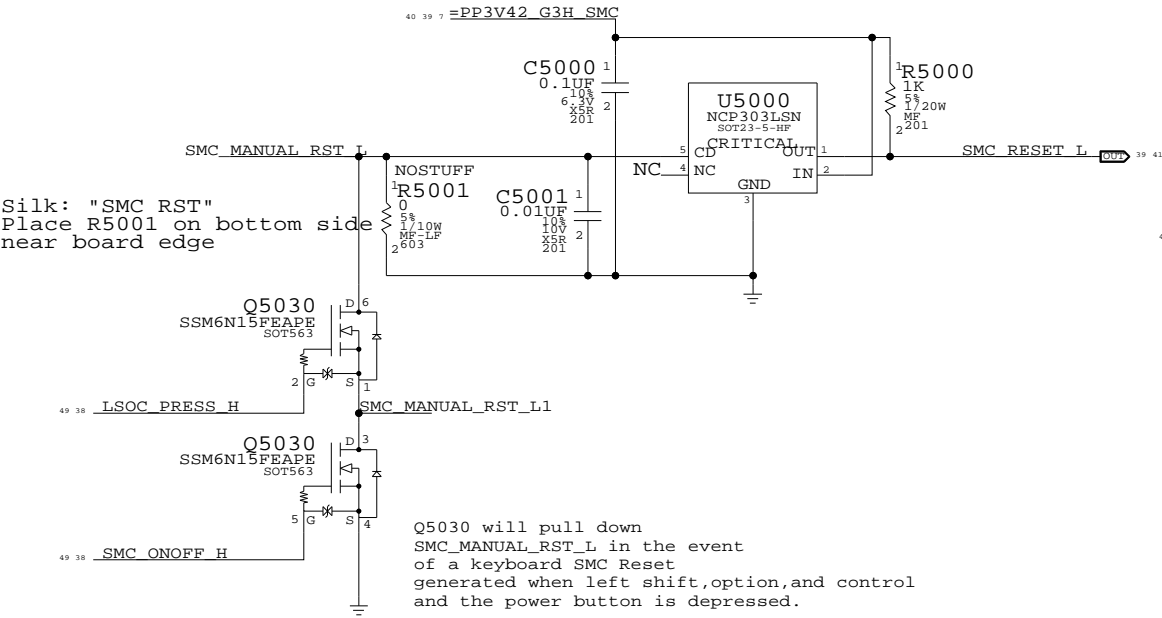
SMC
SYNC_MASTER=M97
SYNC_DATE=02/21/2008
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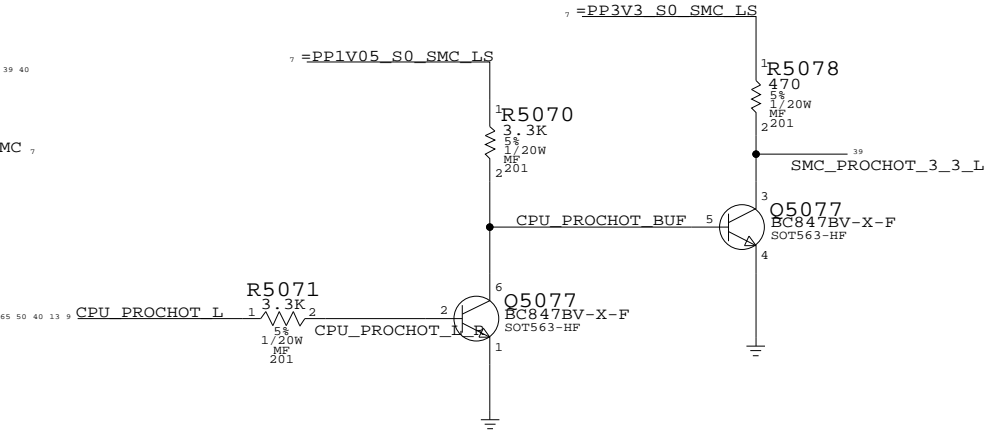
APPLE INC.

SIZE D
DRAWING NUMBER 051-7631
SCALE NONE
SHT 39 OF 71
REV. 2.3.0

SMC Reset Button / Brownout Detect

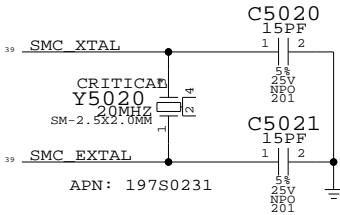
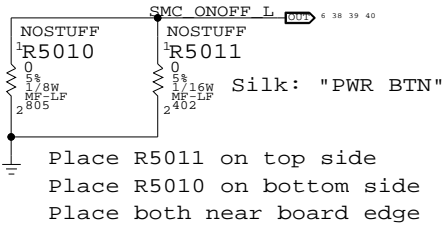


SMC 1.05V to 3.3V Level Shifting

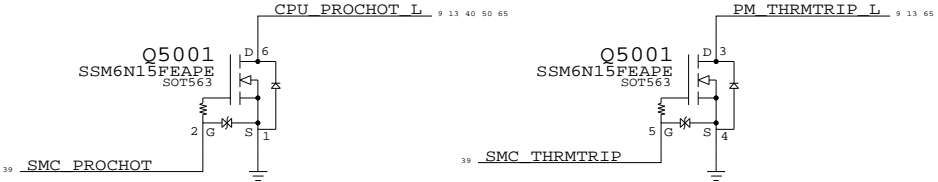


SMC Crystal Circuit

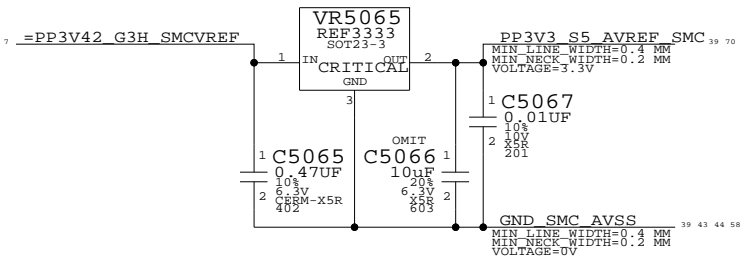
Debug Power Button



SMC 3.3V to 1.05V Level Shifting



SMC AVREF Supply



SMC SUPPORT

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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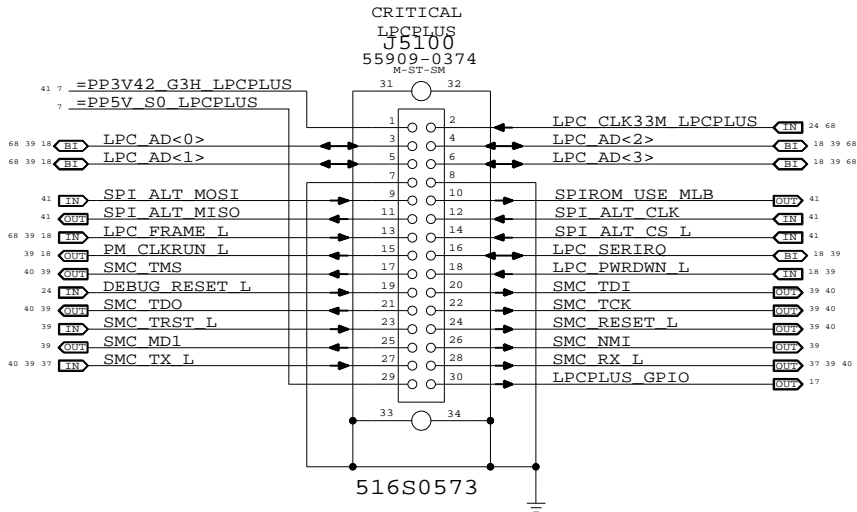
SIZE	DRAWING NUMBER	REV.
D	051-7631	2.3.0
SCALE	SHT	OF
NONE	40	71

LPC+SPI Connector

MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
Any of the 4 frequencies can be selected w/ R5190,R5191,R5192,R5193

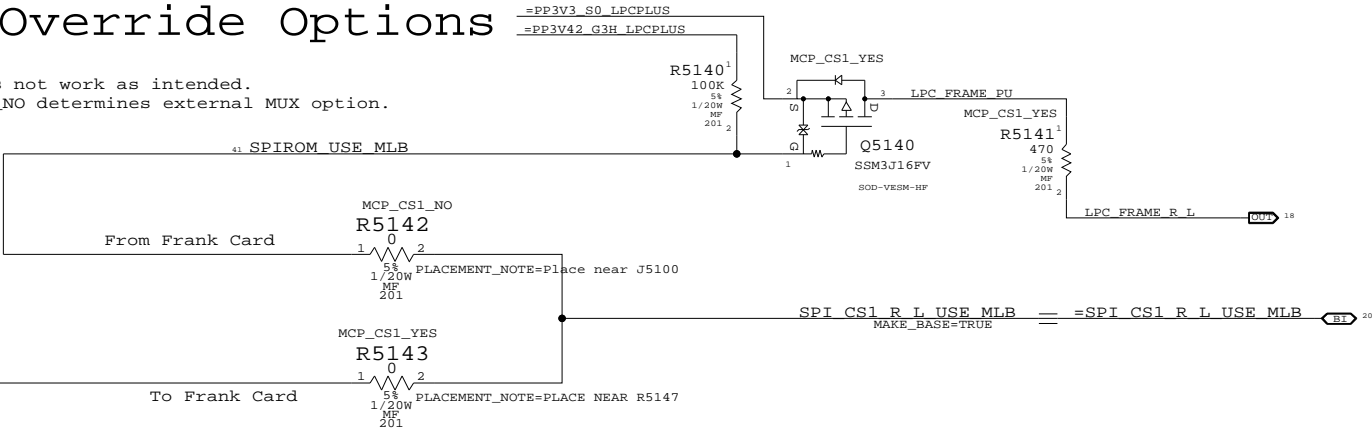


MCP79 Internal SPI MUX Support

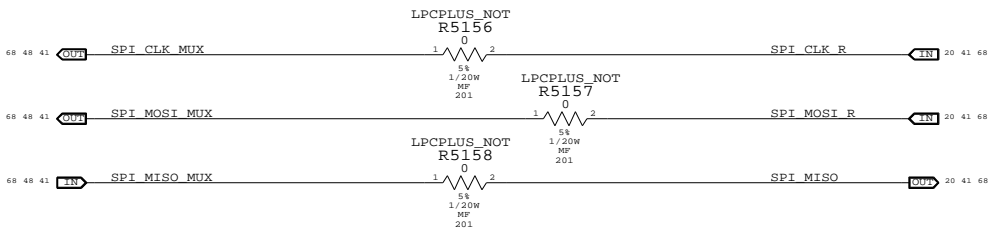
Not supported in Rev A01 MCP79 silicon

MCP SPI Override Options

Internal MUX in rev B01 does not work as intended.
Now MCP_CS1_YES and MCP_CS1_NO determines external MUX option.



SPI MUX BYPASS

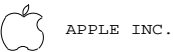


LPC+SPI Debug Connector

SYNC_MASTER=CHANGZHANG SYNC_DATE=01/24/2008

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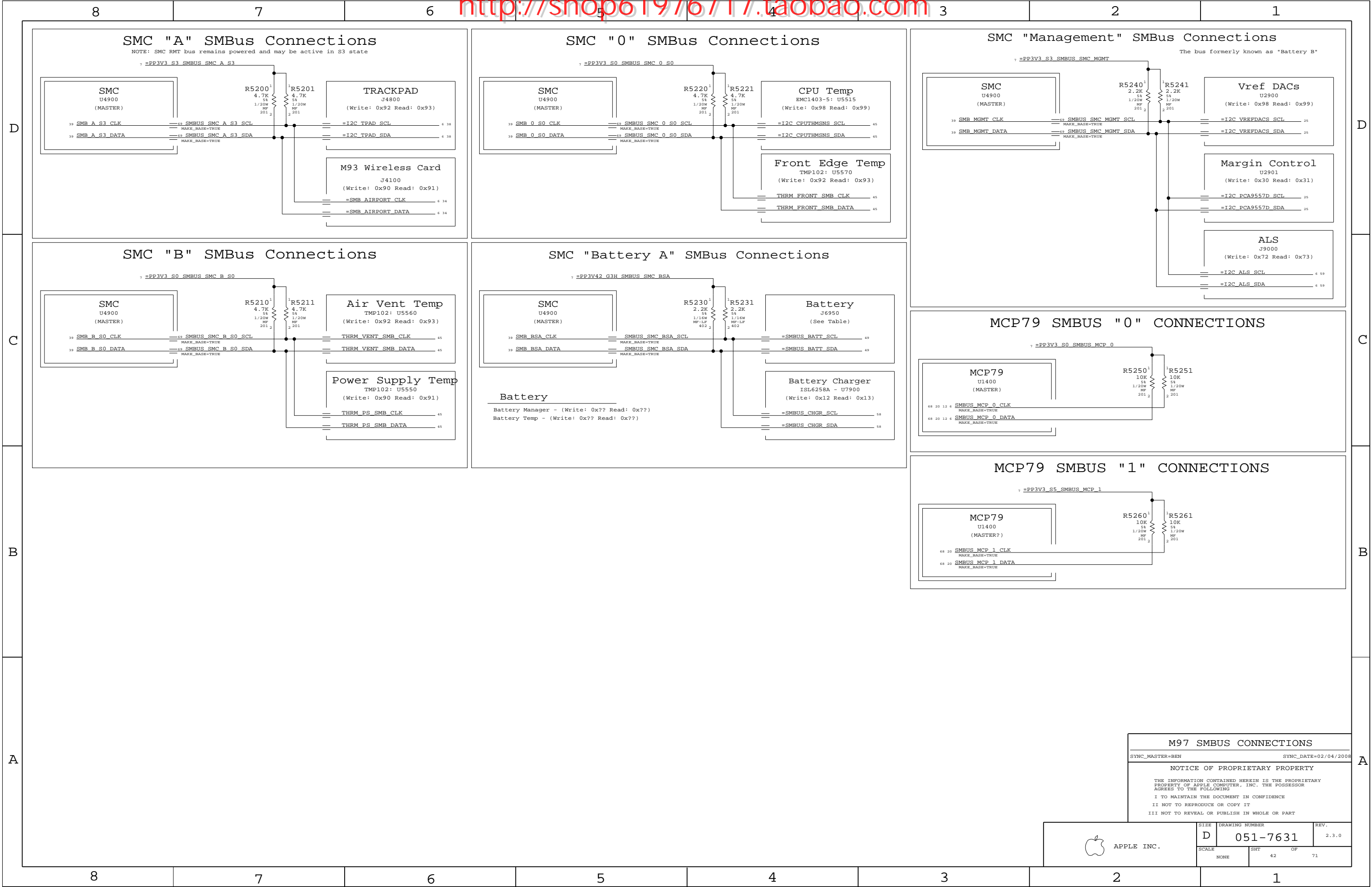


APPLE INC.

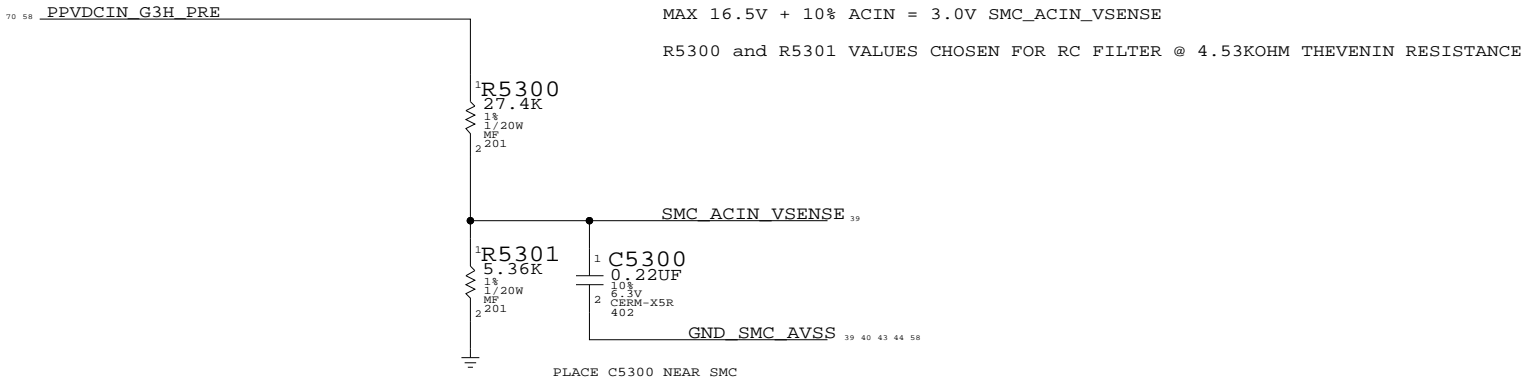
SIZE DRAWING NUMBER REV.

D 051-7631 2.3.0

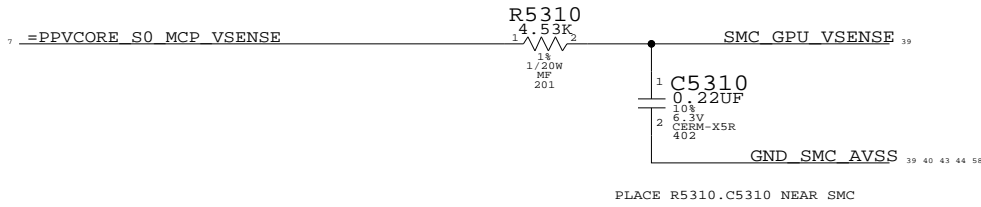
SCALE NONE SHT 41 OF 71



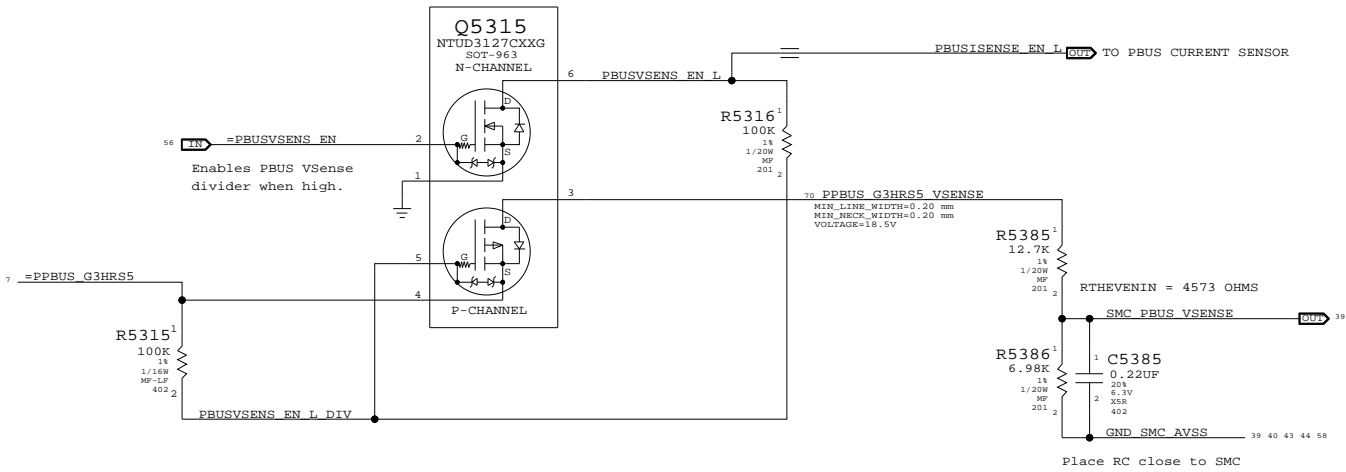
ACIN VOLTAGE SENSE



MCP VOLTAGE SENSE



PBUS VOLTAGE SENSE



Voltage Sensors

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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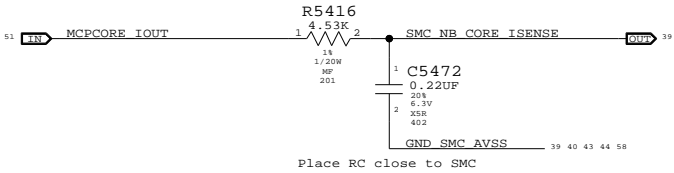


APPLE INC.

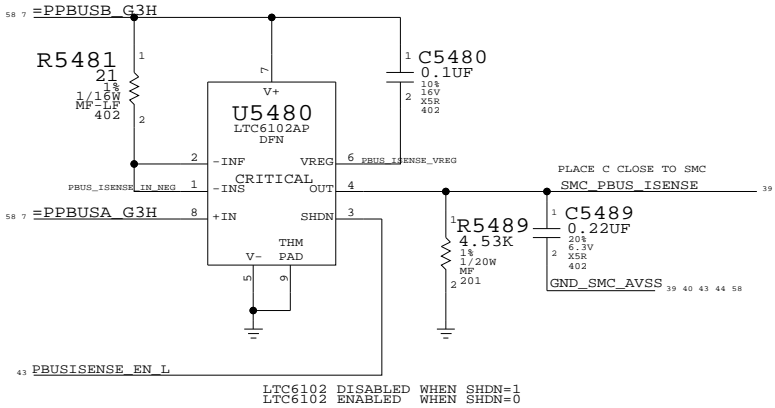
SIZE	DRAWING NUMBER	REV.
D	051-7631	2.3.0
SCALE	SHT	OF
NONE	43	71

MCP VCore Current Sense

MCP VCore Current Sense Filter



PBUS Current Sense



Current Sensing

SYNC_MASTER=YUNWU SYNC_DATE=02/04/2008


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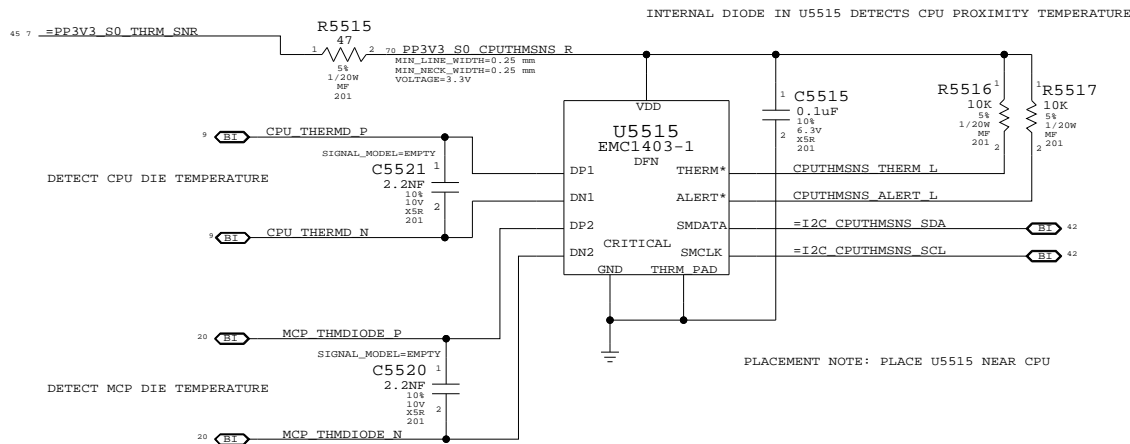
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

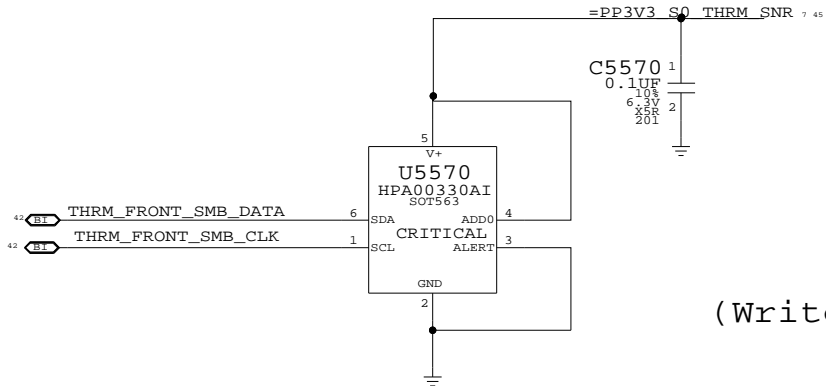
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	NONE	SHT	OF
		44	71

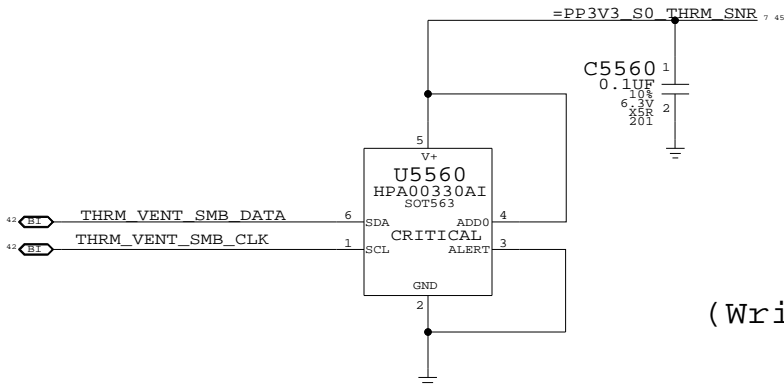
CPU/MCP T-Diode Thermal Sensor



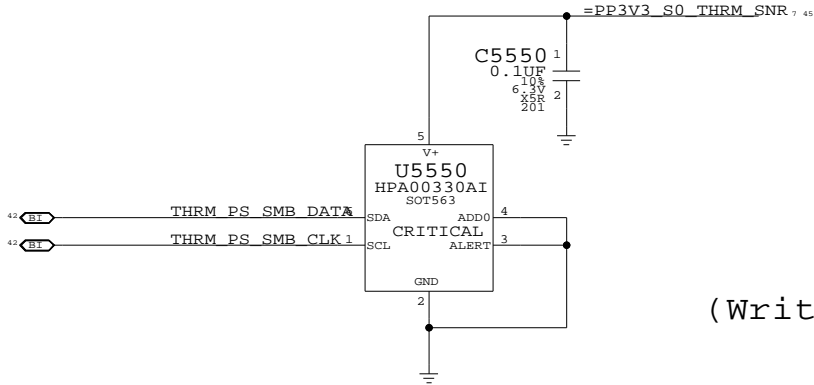
LOCAL TEMP NEAR FRONT EDGE



LOCAL TEMP NEAR AIR VENT



LOCAL TEMP NEAR POWER SUPPLIES



TEMPERATURE SENSORS

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

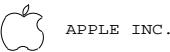
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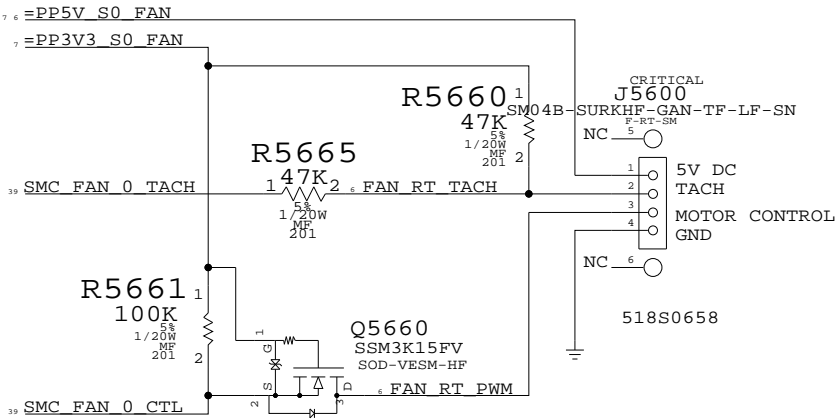
APPLE INC.

SIZE DRAWING NUMBER REV.

D 051-7631 2.3.0

SCALE NONE SHT 45 OF 71

FAN CONNECTOR



Fan

SYNC_MASTER=M70

SYNC_DATE=01/09/2007


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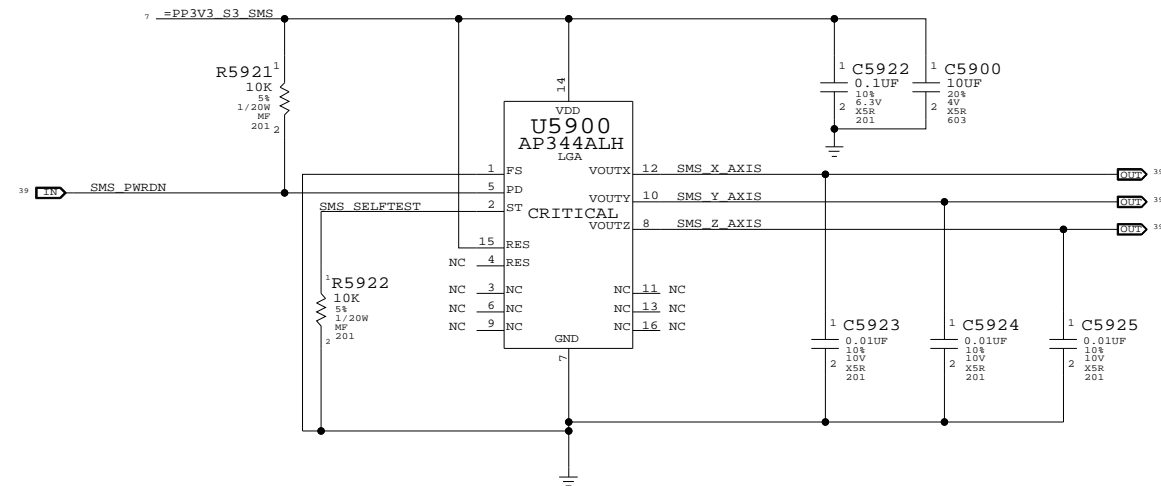
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

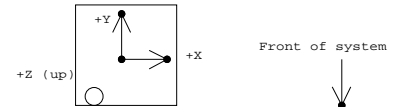
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE INC.	SIZE	DRAWING NUMBER		REV.
	D	051-7631		2.3.0
SCALE		SHT	OF	
NONE		46	71	

SUDDEN MOTION SENSOR



Desired orientation when placed on board top-side:



Circle indicates pin 1 location when placed in correct orientation

Sudden Motion Sensor (SMS)

SYNC_MASTER=M76_MLB

SYNC_DATE=01/12/2007


NOTICE OF PROPRIETARY PROPERTY

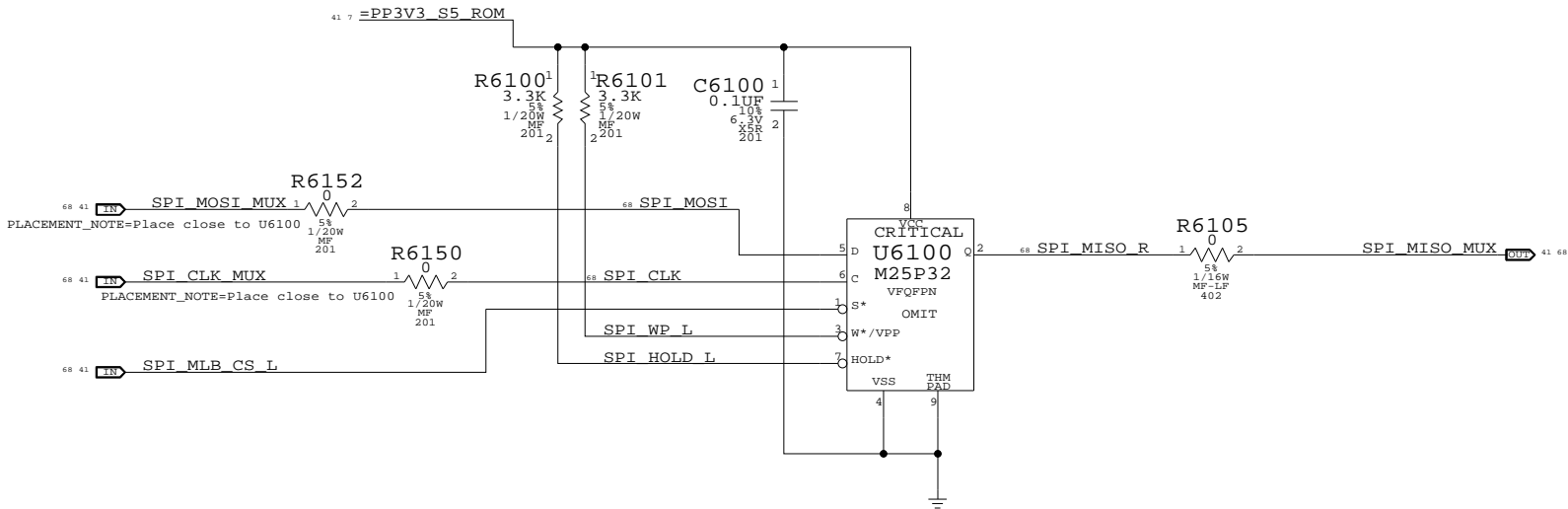
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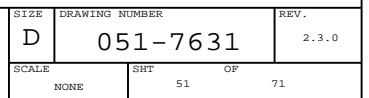
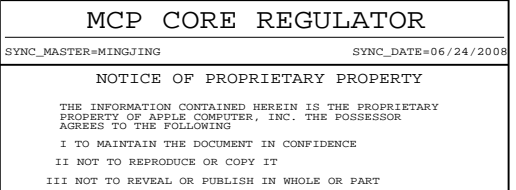
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	D	051-7631		2.3.0
SCALE		SHT	OF	
NONE		47	71	



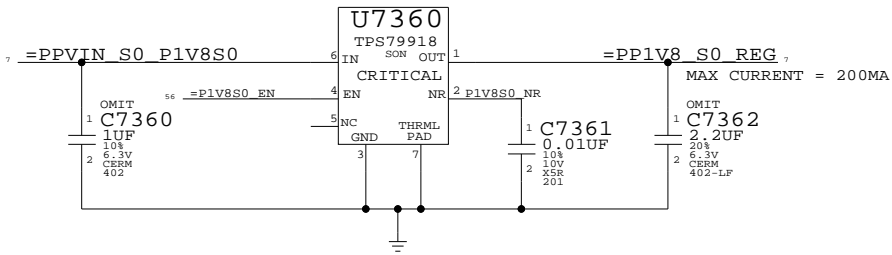
SPI ROM	
SYNC_MASTER=CHANGZHANG	SYNC_DATE=02/15/2008
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 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	NONE	SHT	OF
		48	71

A



1.8V S0 LDO



1.8V LDO Supply

SYNC_MASTER=

SYNC_DATE=


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	D	051-7631		2.3.0
SCALE		SHT	OF	
NONE		52	71	

1V05 S5 POWER SUPPLY

PWM FREQ = 400KHZ

1V05 S5 Power Supply	
SYNC_MASTER=RXU_K20	SYNC_DATE=05/21/2008
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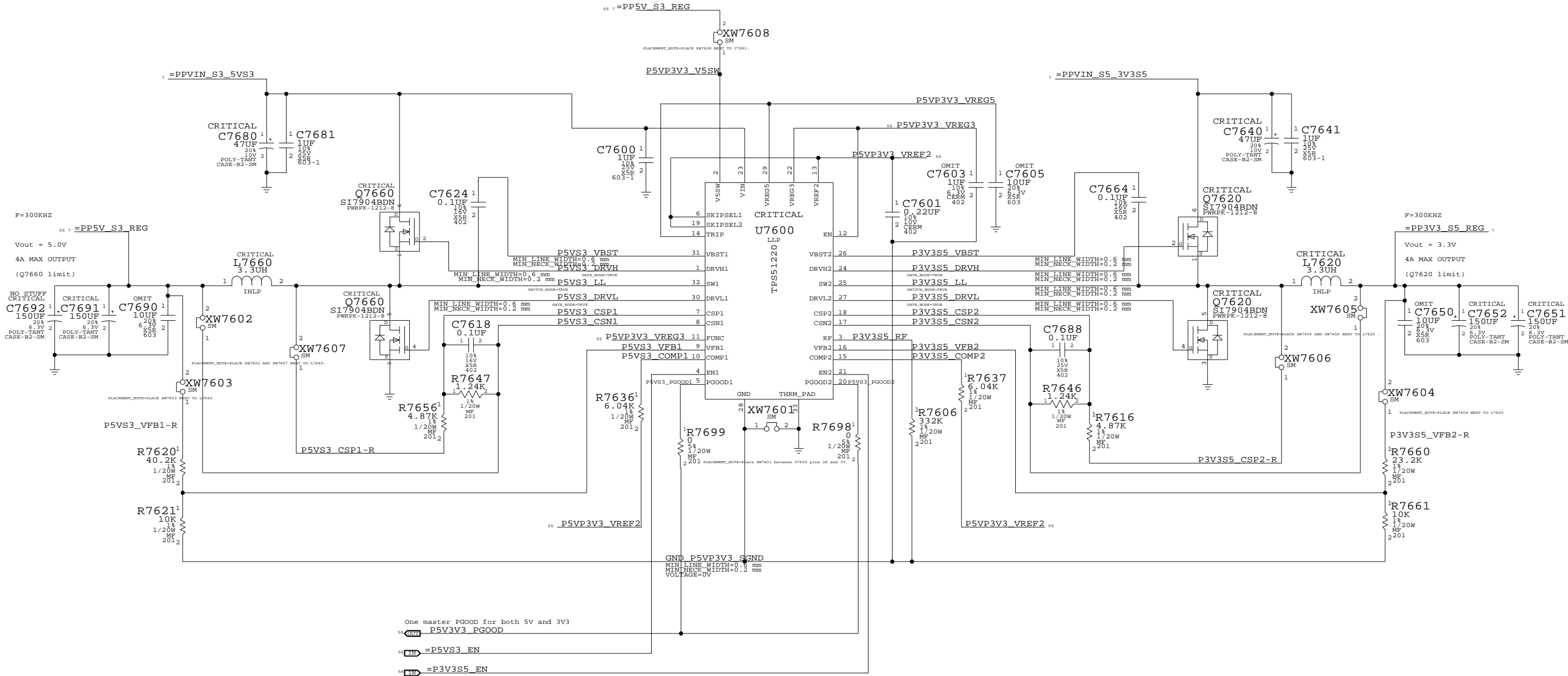
SIZE D	DRAWING NUMBER 051-7631	REV. 2.3.0
SCALE NONE	SHT OF 53 71	

D

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5V_S3 / 3V3_S5 POWER SUPPLY



5V / 3.3V Power Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

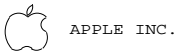
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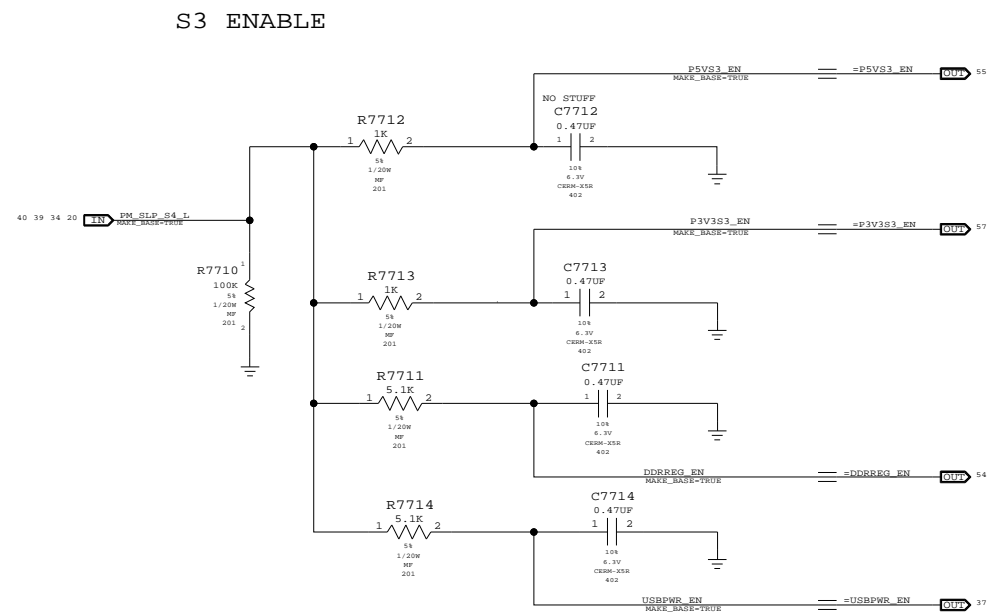
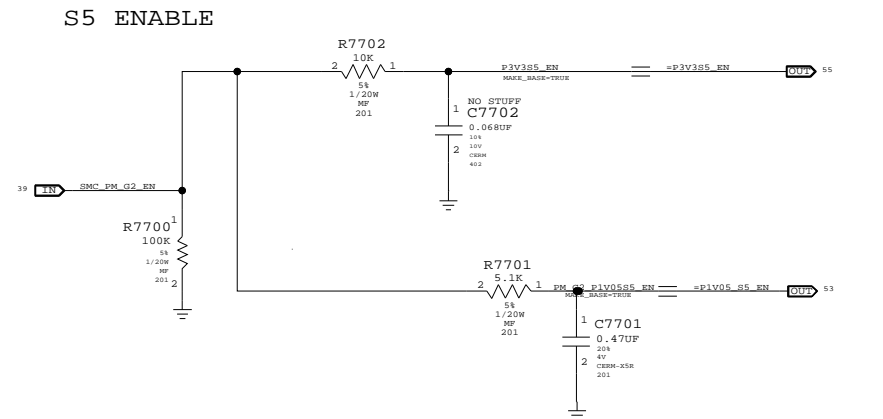
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



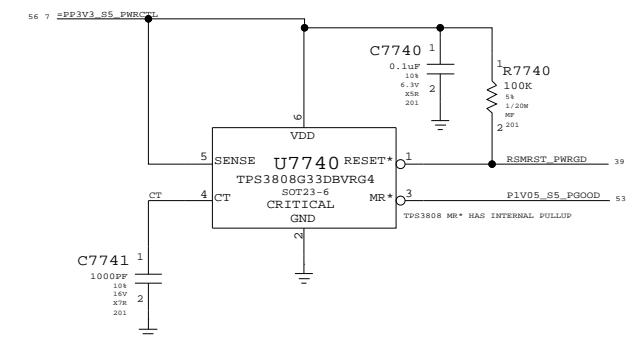
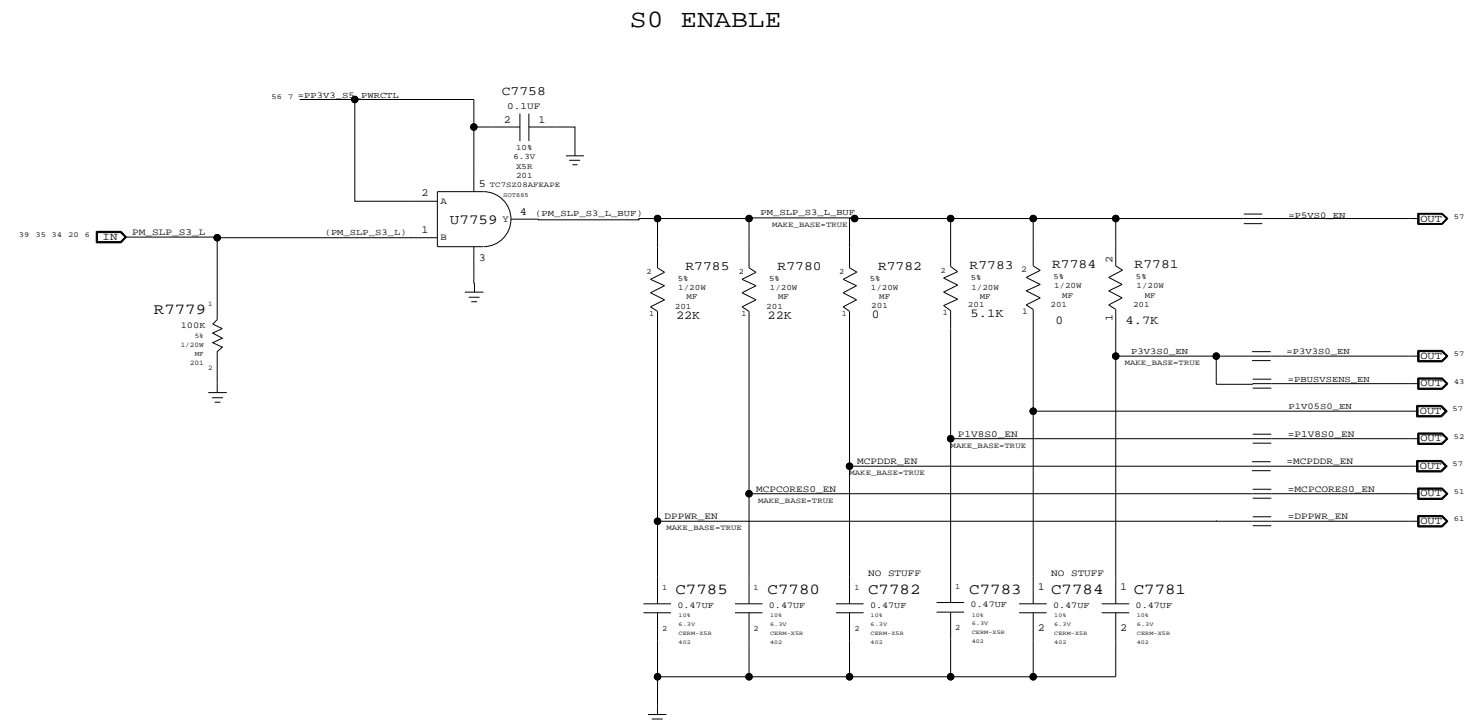
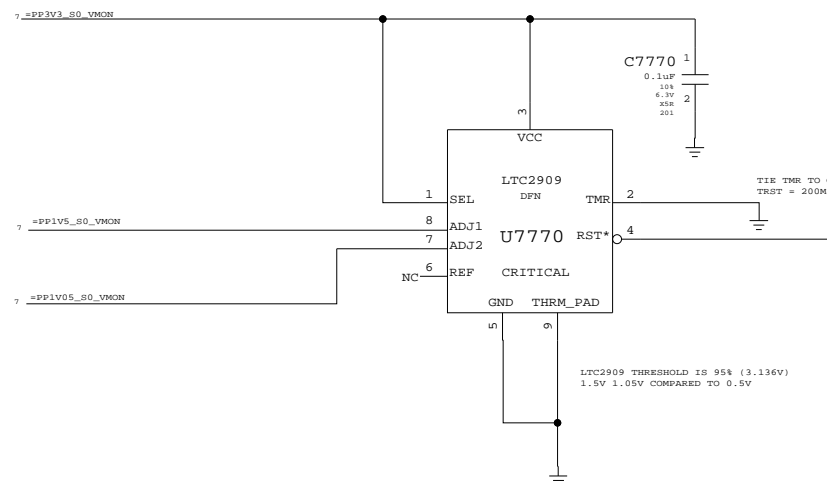
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	2.3.0
SCALE	SHT	OF
NONE	55	71

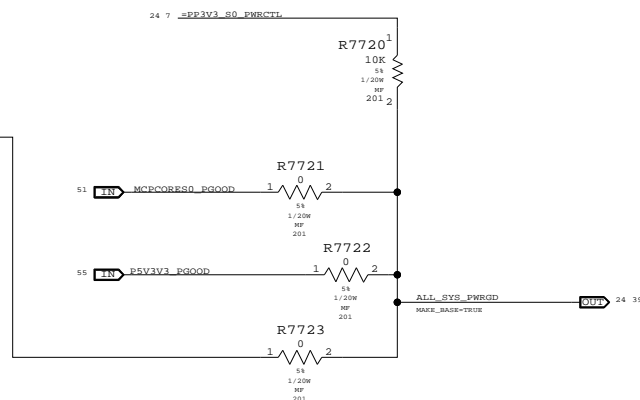
Power Control Signals



3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT



OTHER S0 RAILS PGOOD



Unused PGOOD signal

TP_DDRREG_PGOOD — DDRREG_PGOOD 54

POWER SEQUENCING

SYNC_MASTER=YUAN.MA	SYNC_DATE=02/04/2008
---------------------	----------------------

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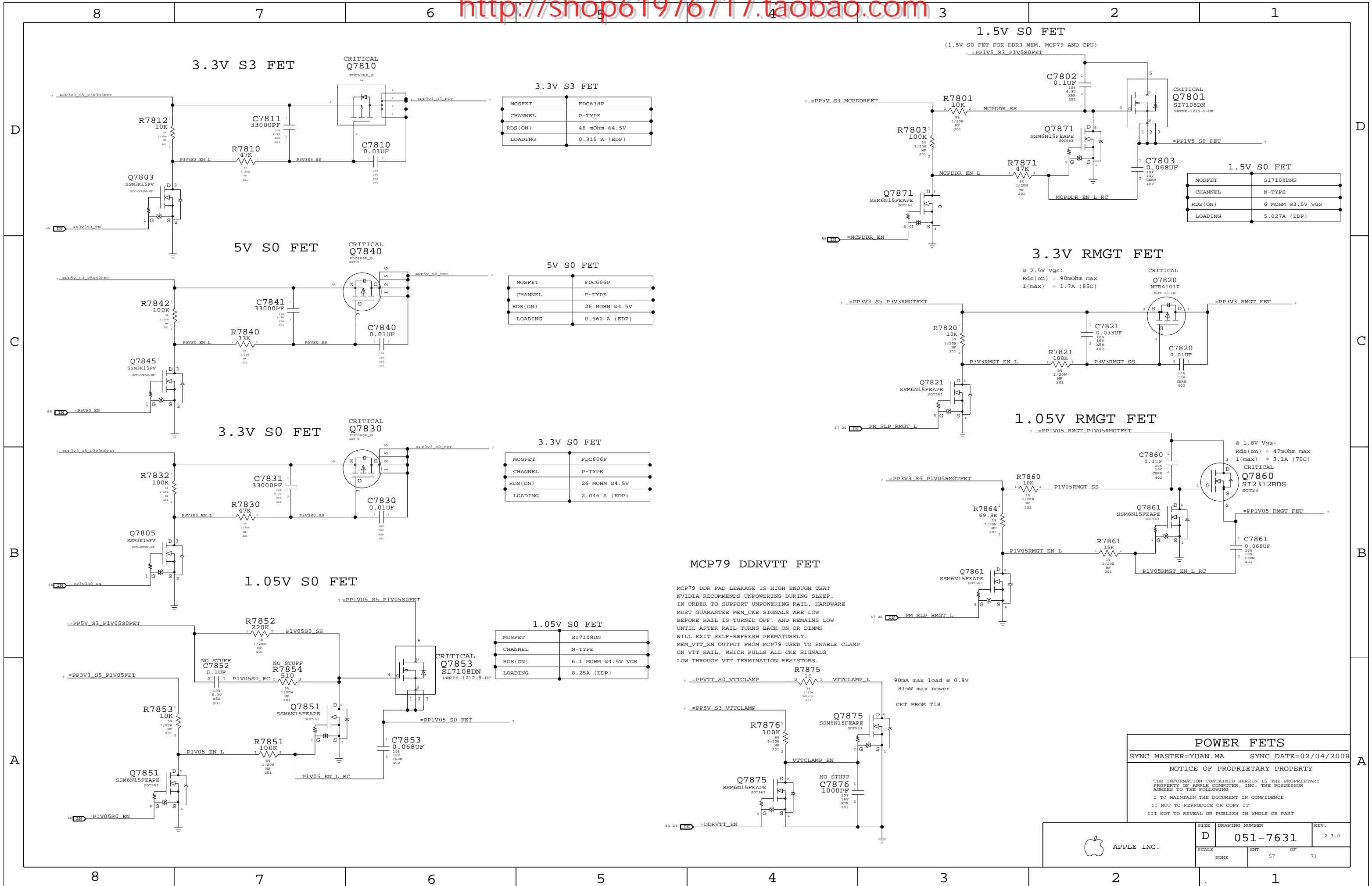
APPLE INC.

SIZE	DRAWING NUMBER	REV.
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D	051-7631	2.3.0
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SCALE	SHT	OF
	56	71

NONE	56	71
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PBUS SUPPLY / BATTERY CHARGER

D

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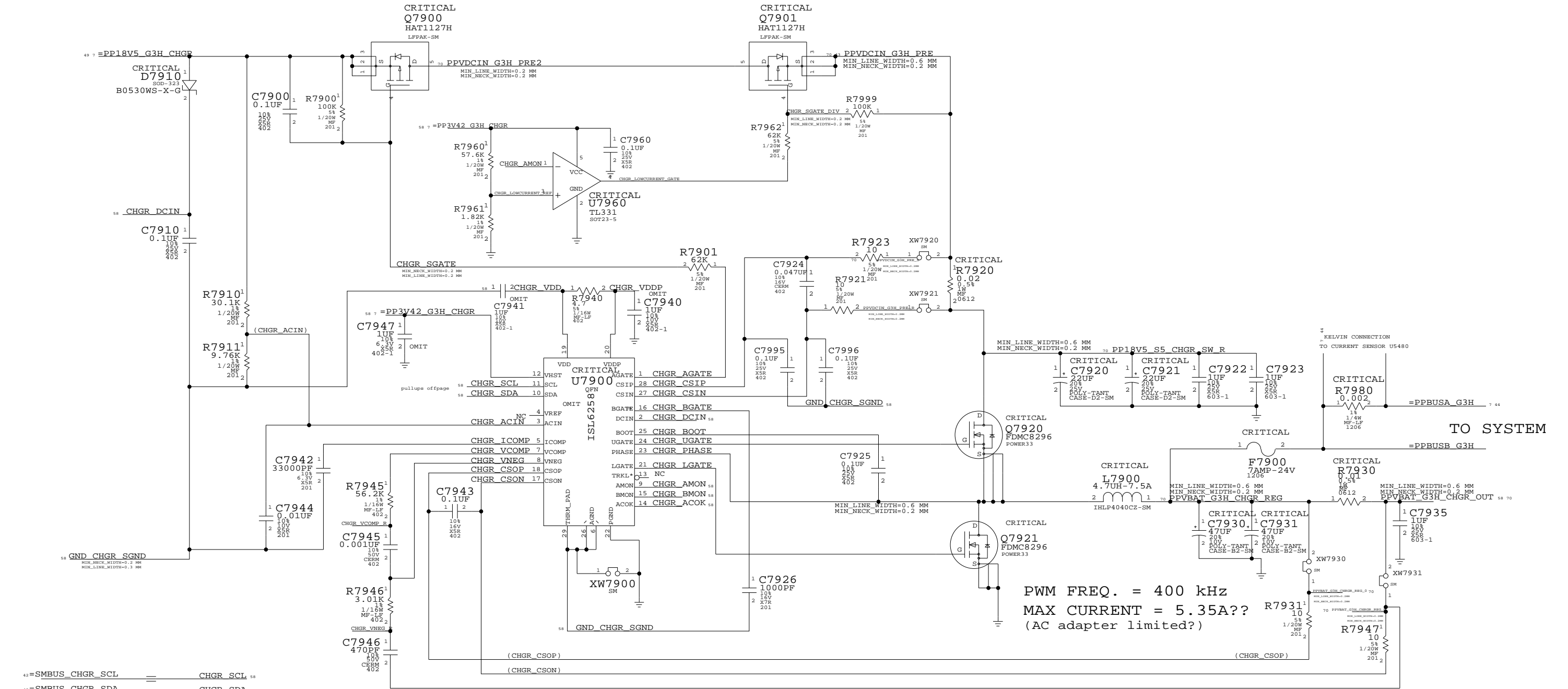
A

D

C

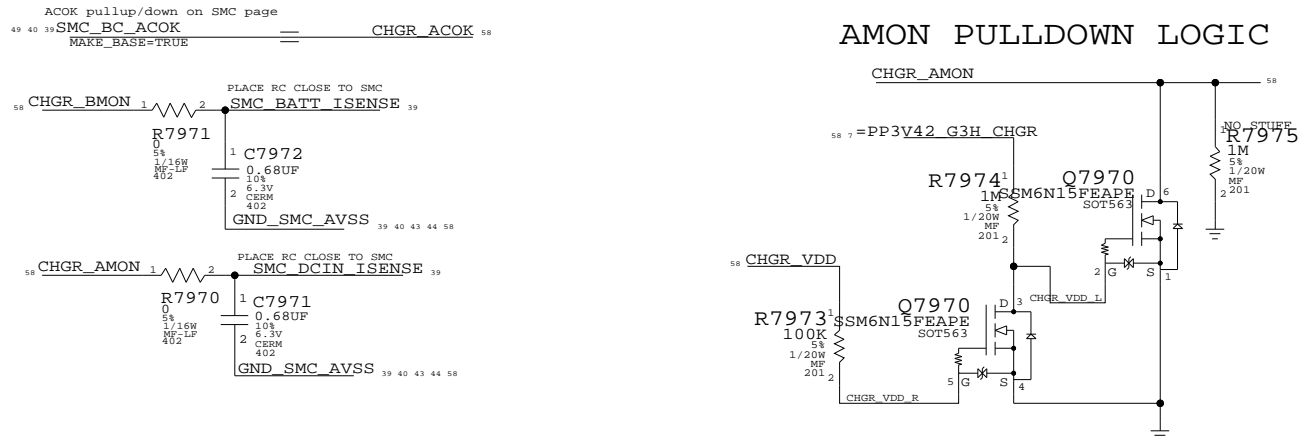
B

A

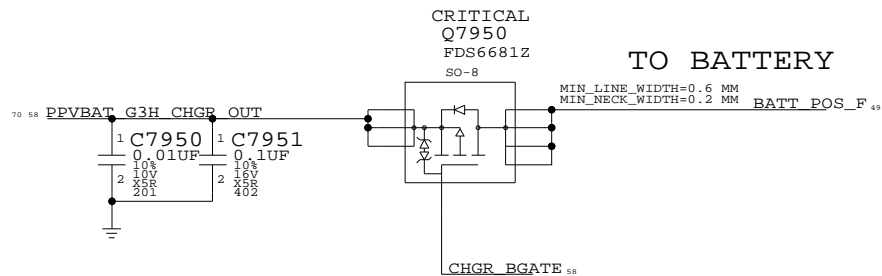


PWM FREQ. = 400 kHz
MAX CURRENT = 5.35A??
(AC adapter limited?)

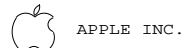
AMON PULLDOWN LOGIC



BATTERY CHARGING

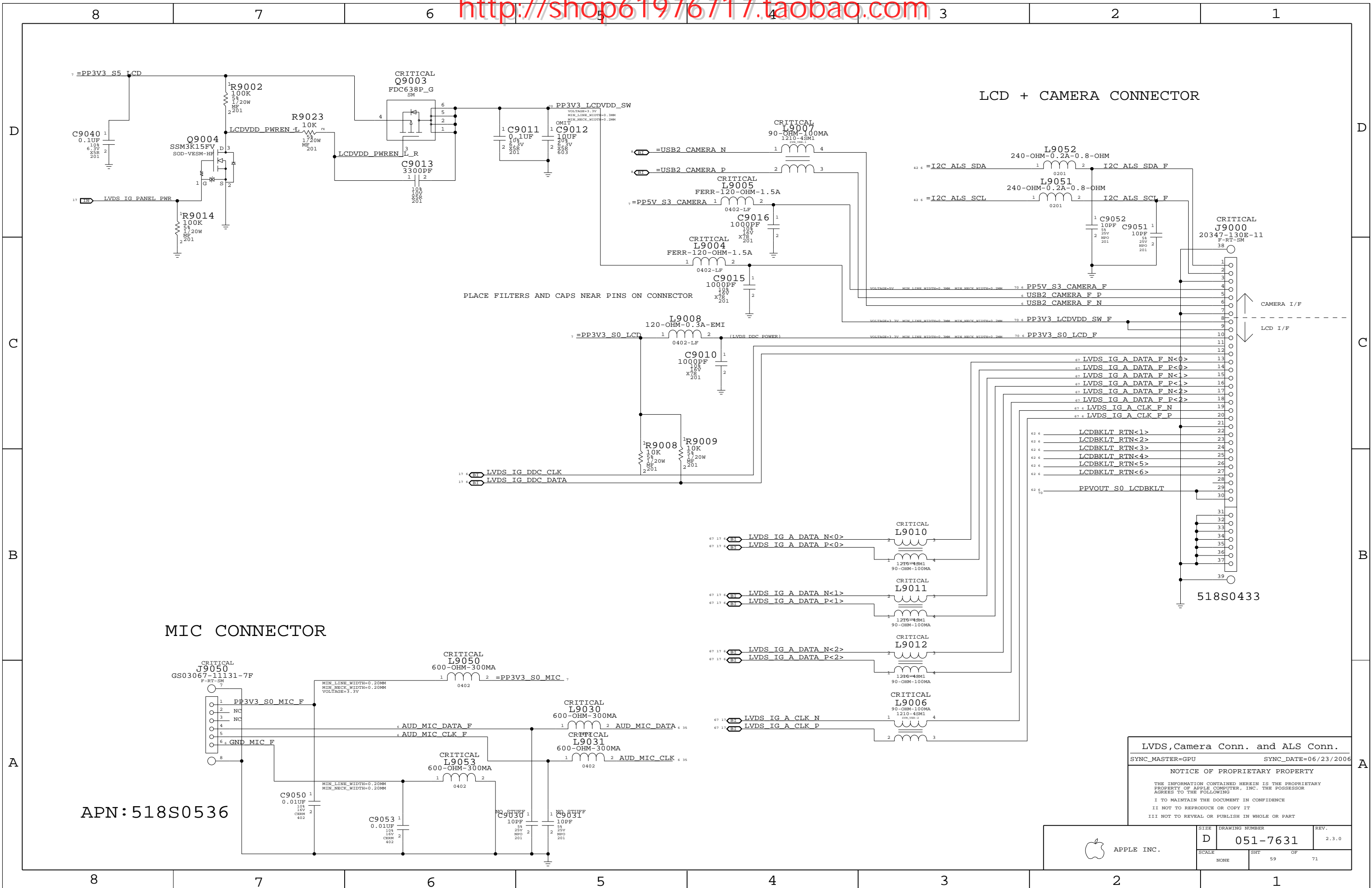


PBUS Supply/Battery Charger	
SYNC_MASTER=M70	SYNC_DATE=01/09/2007
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	2.3.0
SCALE	SHT	OF
NONE	58	71



MIC CONNECTOR

LCD + CAMERA CONNECTOR

APN:518S0536

518S0433

LVDS, Camera Conn. and ALS Conn.
SYNC_MASTER=GPU SYNC_DATE=06/23/2006
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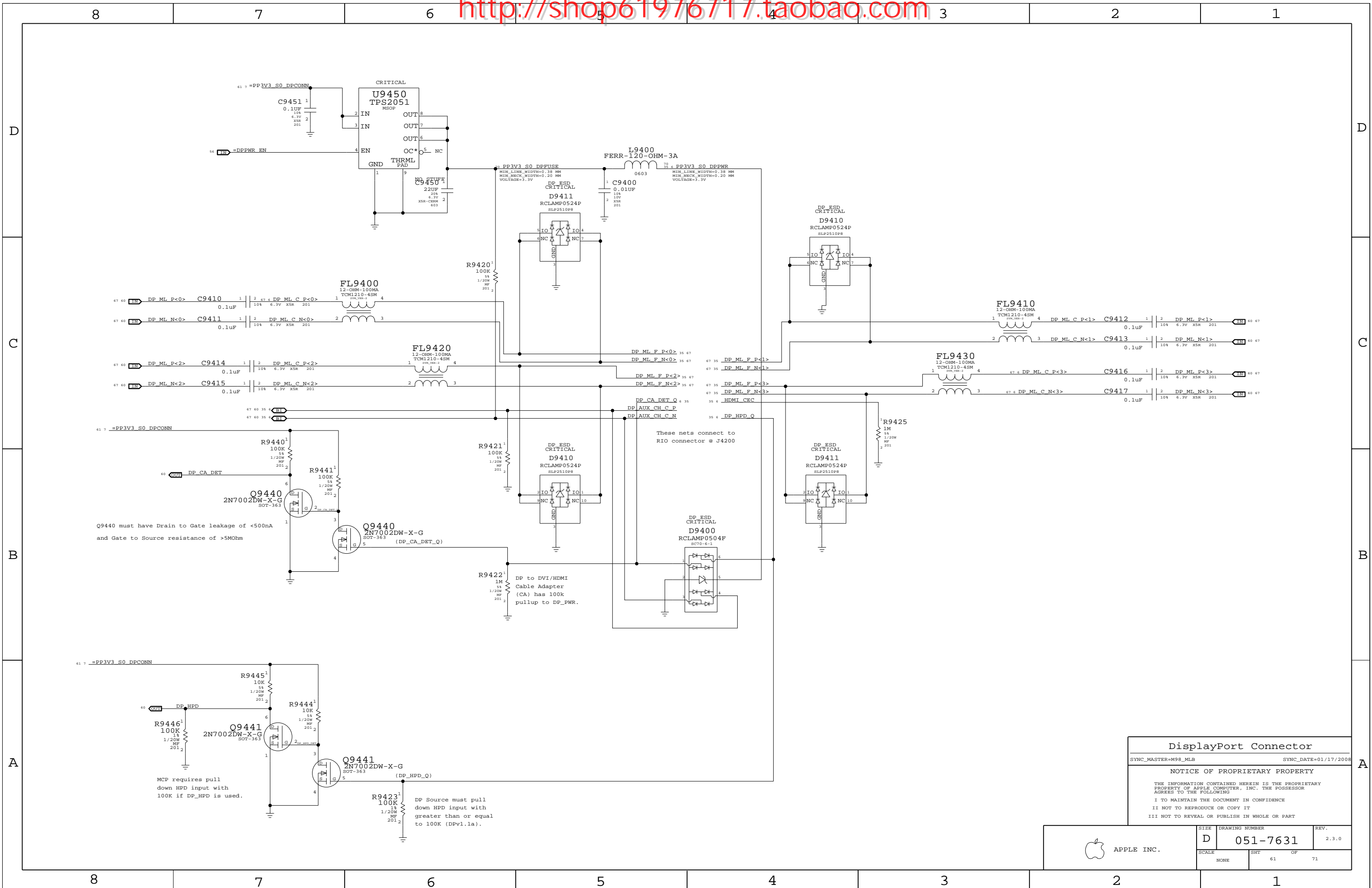
SIZE	DRAWING NUMBER	REV.
D	051-7631	2.3.0
SCALE	SHT	OF
NONE	59	71



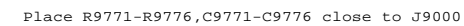
17	=MCP_HDMI_TXC_P	==	DP_ML_P<3>		61	67
17	=MCP_HDMI_TXC_N	==	DP_ML_N<3>	MAKE_BASE=TRUE	61	67
17	=MCP_HDMI_TXD_P<0>	==	DP_ML_P<2>	MAKE_BASE=TRUE	61	67
17	=MCP_HDMI_TXD_N<0>	==	DP_ML_N<2>	MAKE_BASE=TRUE	61	67
17	=MCP_HDMI_TXD_P<1>	==	DP_ML_P<1>	MAKE_BASE=TRUE	61	67
17	=MCP_HDMI_TXD_N<1>	==	DP_ML_N<1>	MAKE_BASE=TRUE	61	67
17	=MCP_HDMI_TXD_P<2>	==	DP_ML_P<0>	MAKE_BASE=TRUE	61	67
17	=MCP_HDMI_TXD_N<2>	==	DP_ML_N<0>	MAKE_BASE=TRUE	61	67
17	=MCP_HDMI_HPD	==	DP_HPD	MAKE_BASE=TRUE	61	67
17	=MCP_HDMI_DDC_CLK	==	DP_IG_DDC_CLK	MAKE_BASE=TRUE	60	60
17	=MCP_HDMI_DDC_DATA	==	DP_IG_DDC_DATA	MAKE_BASE=TRUE	60	60


DISPLAYPORT SUPPORT	
SYNC_MASTER=NMARTIN	SYNC_DATE=12/18/2007
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	D	051-7631	2.3.0
	SCALE	SHT	OF
	NONE	60	71



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 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
	SCALE	SHT	OF
	NONE	62	71



APPLE INC.

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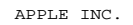
A



SYNC_MASTER=	SYNC_DATE=
1	2017-01-01
2	2017-01-02
3	2017-01-03
4	2017-01-04
5	2017-01-05
6	2017-01-06
7	2017-01-07
8	2017-01-08
9	2017-01-09
10	2017-01-10
11	2017-01-11
12	2017-01-12
13	2017-01-13
14	2017-01-14
15	2017-01-15
16	2017-01-16
17	2017-01-17
18	2017-01-18
19	2017-01-19
20	2017-01-20
21	2017-01-21
22	2017-01-22
23	2017-01-23
24	2017-01-24
25	2017-01-25
26	2017-01-26
27	2017-01-27
28	2017-01-28
29	2017-01-29
30	2017-01-30
31	2017-01-31
32	2017-02-01
33	2017-02-02
34	2017-02-03
35	2017-02-04
36	2017-02-05
37	2017-02-06
38	2017-02-07
39	2017-02-08
40	2017-02-09
41	2017-02-10
42	2017-02-11
43	2017-02-12
44	2017-02-13
45	2017-02-14
46	2017-02-15
47	2017-02-16
48	2017-02-17
49	2017-02-18
50	2017-02-19
51	2017-02-20
52	2017-02-21
53	2017-02-22
54	2017-02-23
55	2017-02-24
56	2017-02-25
57	2017-02-26
58	2017-02-27
59	2017-02-28
60	2017-03-01
61	2017-03-02
62	2017-03-03
63	2017-03-04
64	2017-03-05
65	2017-03-06
66	2017-03-07
67	2017-03-08
68	2017-03-09
69	2017-03-10
70	2017-03-11
71	2017-03-12
72	2017-03-13
73	2017-03-14
74	2017-03-15
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96	2017-04-06
97	2017-04-07
98	2017-04-08
99	2017-04-09
100	2017-04-10

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SIZE D	DRAWING NUMBER 051-7631	REV. 2.3.0
SCALE	SHT OF	

D

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C

B

A

SR DG recommends at least 25 mils, >50 mils preferred

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

FSB Clock Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	= 3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5


D

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8	7	6	5	4	3	2	1
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D

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C

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BA8

D

CBA

D

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C

Digital Video Signal Constraints











B

SATA Interface Constraints





A

 APPLE INC.	SIZE	DRAWING NUMBER		REV.
	D	051-7631		2.3.0
	SCALE	SHT	OF	
	NONE	67	71	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties				
		NET_TYPE		
ELECTRICAL_CONSTRAINT_SET		PHYSICAL	SPACING	
	SMBUS_SMC_A_S3_SCL	SMR_550	SMR	SMBUS_SMC_A_S3_SCL 42
	SMBUS_SMC_A_S3_SDA	SMR_550	SMR	SMBUS_SMC_A_S3_SDA 42
	SMBUS_SMC_B_S0_SCL	SMR_550	SMR	SMBUS_SMC_B_S0_SCL 42
	SMBUS_SMC_B_S0_SDA	SMR_550	SMR	SMBUS_SMC_B_S0_SDA 42
	SMBUS_SMC_0_S0_SCL	SMR_550	SMR	SMBUS_SMC_0_S0_SCL 42
	SMBUS_SMC_0_S0_SDA	SMR_550	SMR	SMBUS_SMC_0_S0_SDA 42
	SMBUS_SMC_BSA_SCL	SMR_550	SMR	SMBUS_SMC_BSA_SCL 6 42
	SMBUS_SMC_BSA_SDA	SMR_550	SMR	SMBUS_SMC_BSA_SDA 6 42
	SMBUS_SMC_MGMT_SCL	SMR_550	SMR	SMBUS_SMC_MGMT_SCL 42
	SMBUS_SMC_MGMT_SDA	SMR_550	SMR	SMBUS_SMC_MGMT_SDA 42

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
 	CHGR_CSI	1701_DIFFPAIR		CHGR_CSI_P
		1701_DIFFPAIR		CHGR_CSI_N
 	CHGR_CSO	1701_DIFFPAIR		CHGR_CSO_P
		1701_DIFFPAIR		CHGR_CSO_N

SYMC Constraints		SYMC_MASTER=97		SYMC_DATE=02/04/2008	
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D		051-7631		2.3.0	
SCALE		SHT		OF	
NONE		69		71	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR	*	=STANDARD	?
BUS2PWR_GND	*	0.228 MM	?

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DCBAA

SIZE D	DRAWING NUMBER 051-7631	REV. 2.3.0
SCALE NONE	SHT OF 71 71	