

8

7

6

5

4

3

2

1

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV

ZONE

ECN

DESCRIPTION OF CHANGE

CK APPD

DATE

ENG APPD

DATE

?

?

?

?

?

SCHEM, MBP 15 " MLB

08/18/2008

Page

(.csa)

Contents

Sync

Date

1

Table of Contents

N/A

N/A

2

System Block Diagram

T18_MLB

12/12/2007

3

Power Block Diagram

T18_MLB

12/12/2007

4

Power Block Diagram

N/A

N/A

5

BOM Configuration

N/A

N/A

6

JTAG Scan Chain

DDR

07/22/2008

7

Functional / ICT Test

N/A

N/A

8

Power Aliases

(MASTER)

(MASTER)

9

Signal Aliases

(MASTER)

(MASTER)

10

CPU FSB

M87_MLB

10/17/2007

11

CPU Power & Ground

M87_MLB

10/17/2007

12

CPU Decoupling & VID

M87_MLB

10/17/2007

13

eXtended Debug Port(MiniXDP)

M99_MLB

01/08/2008

14

MCP CPU Interface

T18_MLB

06/18/2008

15

MCP Memory Interface

T18_MLB

06/18/2008

16

MCP Memory Misc

T18_MLB

06/18/2008

17

MCP PCIe Interfaces

T18_MLB

06/18/2008

18

MCP Ethernet & Graphics

T18_MLB

06/18/2008

19

MCP PCI & LPC

T18_MLB

06/18/2008

20

MCP SATA & USB

T18_MLB

06/18/2008

21

MCP HDA & MISC

T18_MLB

06/18/2008

22

MCP Power & Ground

T18_MLB

06/18/2008

23

MCP79 A01 Silicon Support

T18_MLB

03/31/2008

24

MCP Standard Decoupling

T18_MLB

06/18/2008

25

MCP Graphics Support

AMASON_M98_MLB

06/18/2008

26

SB Misc

T18_MLB

12/17/2007

27

FSB/DDR3/FRAMEBUF Vref Margining

DDR

07/22/2008

28

DDR3 SO-DIMM Connector A

DDR

07/22/2008

29

DDR3 SO-DIMM Connector B

DDR

07/22/2008

30

DDR3 Support

T18_MLB

06/18/2008

31

Right Clutch Connector

YITE_M98_MLB

07/02/2008

32

ExpressCard Connector

YITE_M98_MLB

07/02/2008

33

Ethernet PHY (RTL8211CL)

SUMA_M98_MLB

07/01/2008

34

Ethernet & AirPort Support

SUMA_M98_MLB

07/01/2008

35

Ethernet Connector

SUMA_M98_MLB

07/01/2008

36

FireWire LLC/PHY (FW643)

SENSOR

08/14/2008

37

FireWire Port Power

SENSOR

08/14/2008

38

FireWire Ports

SENSOR

08/14/2008

39

SATA Connectors

CHANG_M98_MLB

07/01/2008

40

External USB Connectors

AMASON_M98_MLB

07/02/2008

41

Front Flex Support

CHANG_M98_MLB

07/01/2008

42

SMC

T18_MLB

06/18/2008

43

SMC Support

AMASON_M98_MLB

06/18/2008

44

LPC+SPI Debug Connector

CHANG_M98_MLB

07/01/2008

45

M98 SMBus Connections

DDR

07/22/2008

Page

(.csa)

Contents

Sync

Date

46

Current & Voltage Sensing

SENSOR

08/14/2008

47

Current Sensing

SENSOR

08/14/2008

48

Thermal Sensors

SENSOR

08/14/2008

49

Fan Connectors

M87_MLB

10/17/2007

50

WELLSPRING 1

AMASON_M98_MLB

06/18/2008

51

WELLSPRING 2

PWRSQNC

05/12/2008

52

Sudden Motion Sensor (SMS)

SENSOR

08/14/2008

53

SPI ROM

CHANG_M98_MLB

07/01/2008

54

AUDIO:CODEC

AUDIO

07/09/2008

55

AUDIO: LINE IN

AUDIO

07/09/2008

56

AUDIO: HEADPHONE AMP

AUDIO

07/09/2008

57

AUDIO:SPEAKER AMP

AUDIO

07/09/2008

58

AUDIO: JACKS

AUDIO

07/09/2008

59

AUDIO: JACK TRANSLATORS

AUDIO

07/09/2008

60

DC-In & Battery Connectors

T18_MLB

12/10/2007

61

PBus Supply & Battery Charger

M99_MLB

10/17/2007

62

IMVP6 CPU VCore Regulator

M87_MLB

01/09/2008

63

5V / 3.3V Power Supply

M99_MLB

12/13/2007

64

1.5V DDR3 Supply

M99_MLB

01/08/2008

65

1.05V / MCP Core Regulator

M99_MLB

12/14/2007

66

CPU VTT Power Supply

M99_MLB

12/14/2007

67

Misc Power Supplies

M99_MLB

05/12/2008

68

Power Control

PWRSQNC

05/12/2008

69

Power FETs

PWRSQNC

05/12/2008

70

NV G96 PCI-E

MUXGFX

07/10/2008

71

NV G96 Core/FB Power

MUXGFX

07/10/2008

72

NV G96 Frame Buffer I/F

MUXGFX

07/10/2008

73

GDDR3 Frame Buffer A (Top)

MUXGFX

07/10/2008

74

GDDR3 Frame Buffer B (Top)

MUXGFX

07/10/2008

75

NV G96 GPIO/MIO/Misc

MUXGFX

07/10/2008

76

G96 GPIOs & Straps

MUXGFX

07/09/2008

77

NV G96 Video Interfaces

MUXGFX

07/10/2008

78

GPU (G84M) Core Supply

M87_MLB

10/17/2007

79

LVDS Display Connector

MUXGFX

02/25/2008

80

Muxed Graphics Support

MUXGFX

07/10/2008

81

DisplayPort Connector

MUXGFX

07/10/2008

82

1.1V / 1V8 FB Power Supply

MUXGFX

07/10/2008

83

Graphics MUX (GMUX)

MUXGFX

07/10/2008

84

LCD BACKLIGHT DRIVER

YITE_M98_MLB

07/02/2008

85

LCD Backlight Support

YITE_M98_MLB

07/02/2008

86

Misc Power Supplies

MUXGFX

02/01/2008

87

CPU/FSB Constraints

MUXGFX

02/18/2008

88

Memory Constraints

MUXGFX

02/18/2008

89

MCP Constraints 1

MUXGFX

02/18/2008

90

MCP Constraints 2

MUXGFX

02/18/2008

Page

(.csa)

Contents

Sync

Date

91

Ethernet Constraints

MUXGFX

02/18/2008

92

FireWire Constraints

MUXGFX

02/18/2008

93

SMC Constraints

MUXGFX

02/18/2008

94

GPU (G96) Constraints

MUXGFX

02/18/2008

95

Project Specific Constraints

MUXGFX

02/21/2008

96

PCB Rule Definitions

M99_MLB

01/22/2008

DIMENSIONS ARE IN MILLIMETERS

XX : _____

X.XX : _____

X.XXX : _____

ANGLES : _____

DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER

ENG APPD

QA APPD

RELEASE

DESIGN CK

MFG APPD

DESIGNER

SCALE

NONE

MATERIAL/FINISH

NOTED AS APPLICABLE

SIZE

D

APPLE INC.

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

TITLE

SCHEM, MBP 15MLB

DRAWING NUMBER

051-7546

REV.

A.0.0

SHT

1

OF

96

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7546	1	SCHEM, FIBBO, M98	SCH	CRITICAL	
820-2330	1	PCBF, FIBBO, M98	PCB	CRITICAL	

DRAWING

TITLE=MLB

ABBREV=DRAWING

LAST_MODIFIED=Mon Aug 18 01:48:34 2008

8

7

6

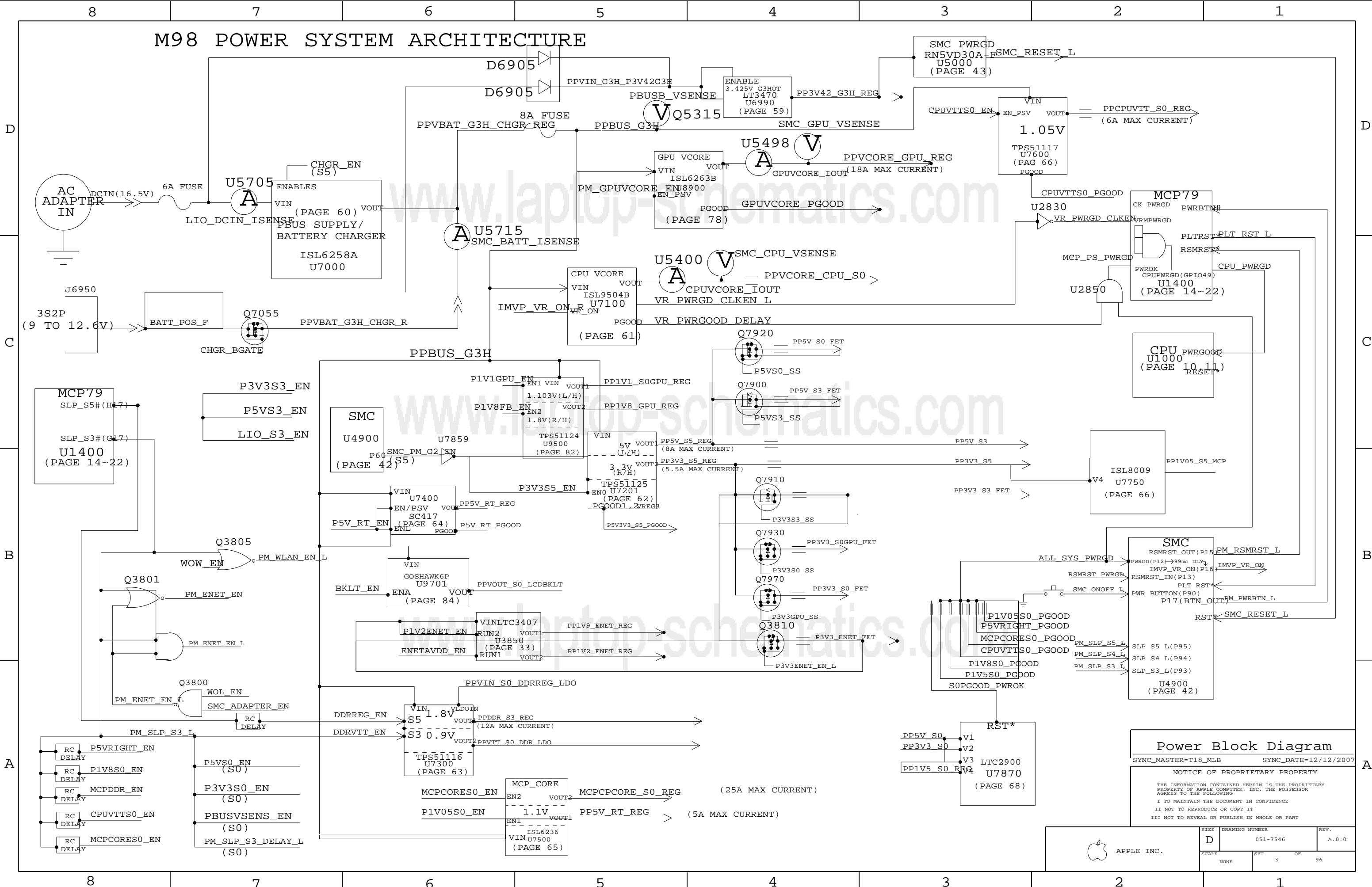
5

4

3

2

1



Power Block Diagram

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

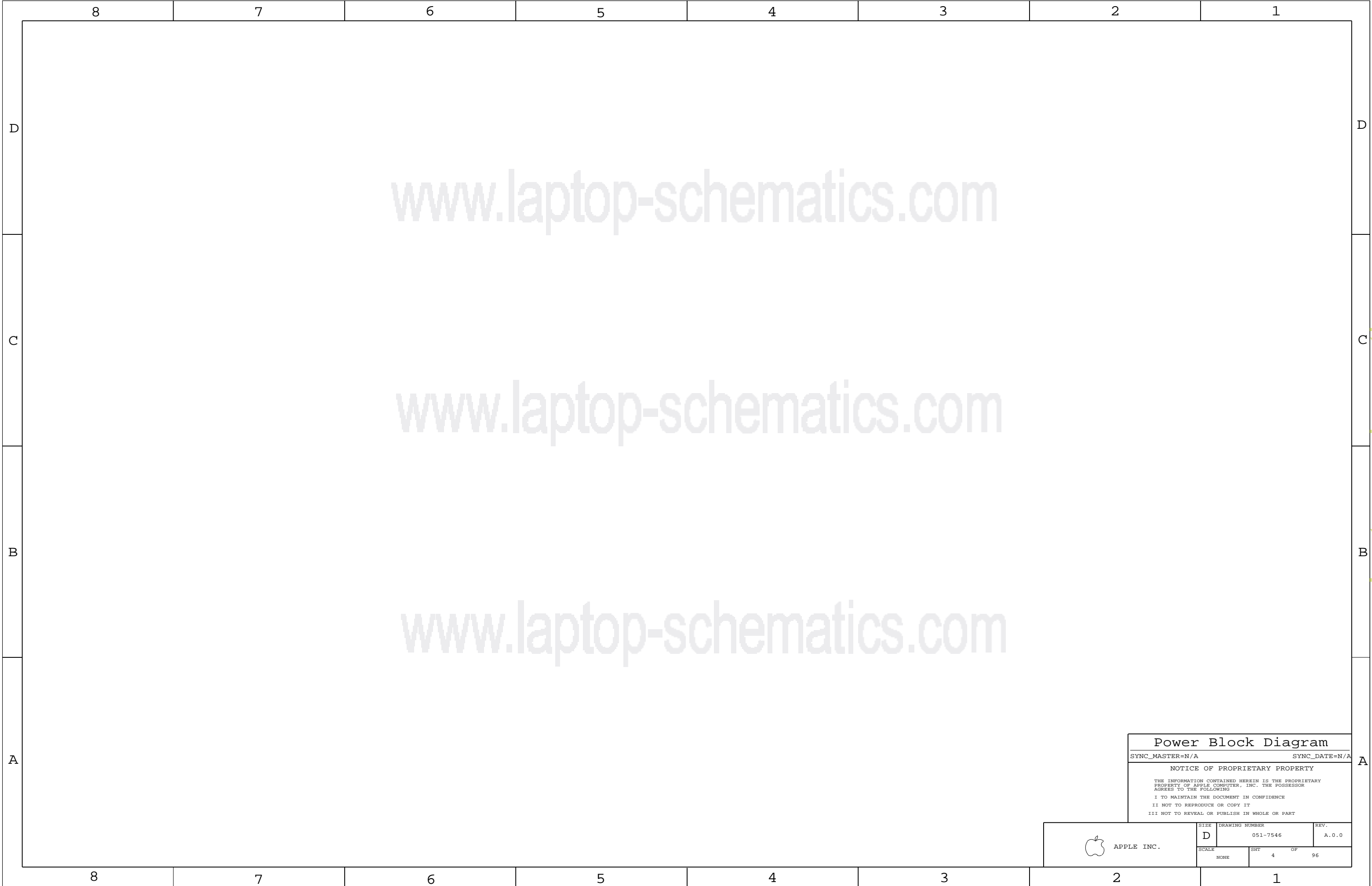
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

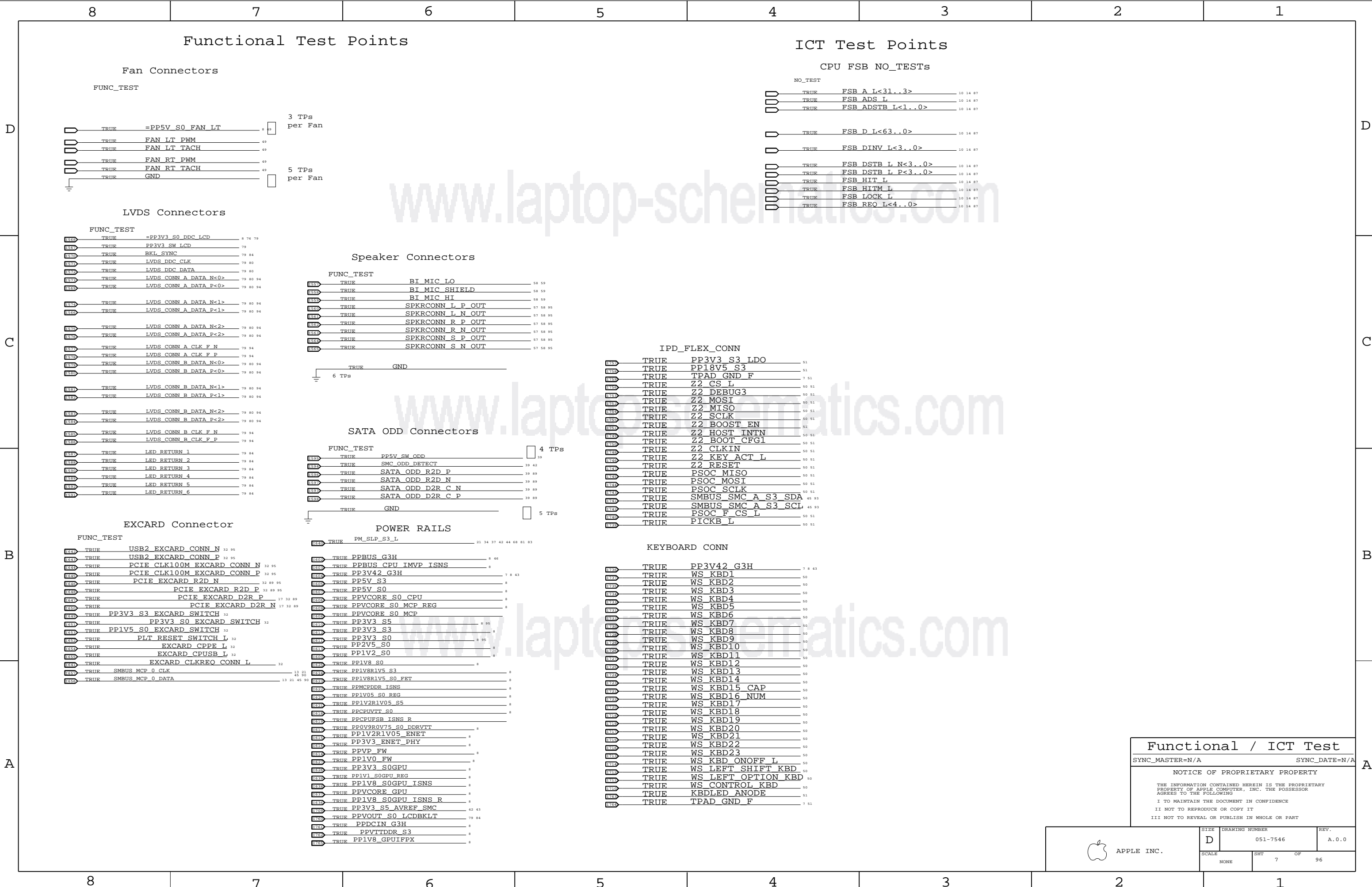
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

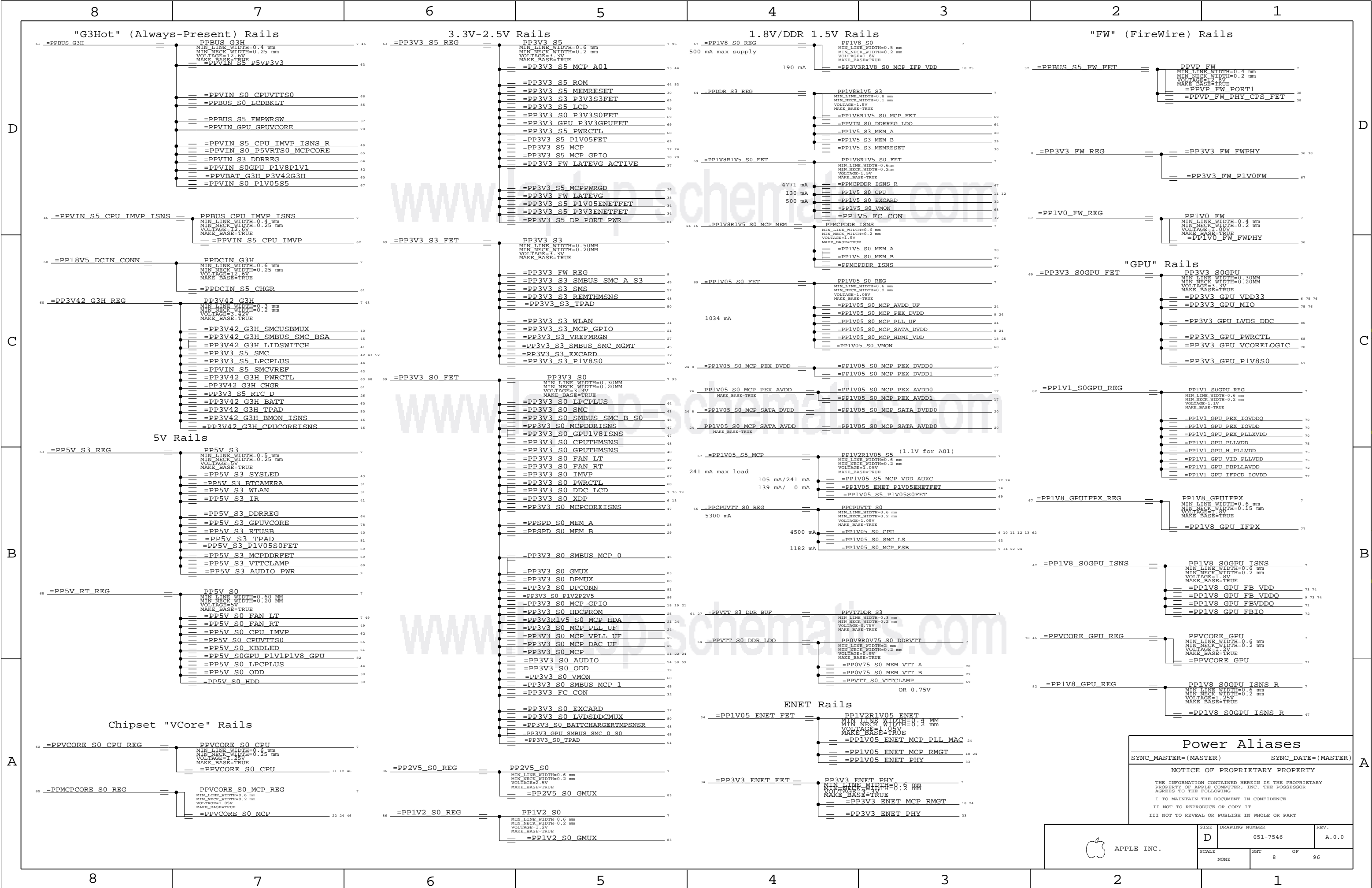
APPLE INC.

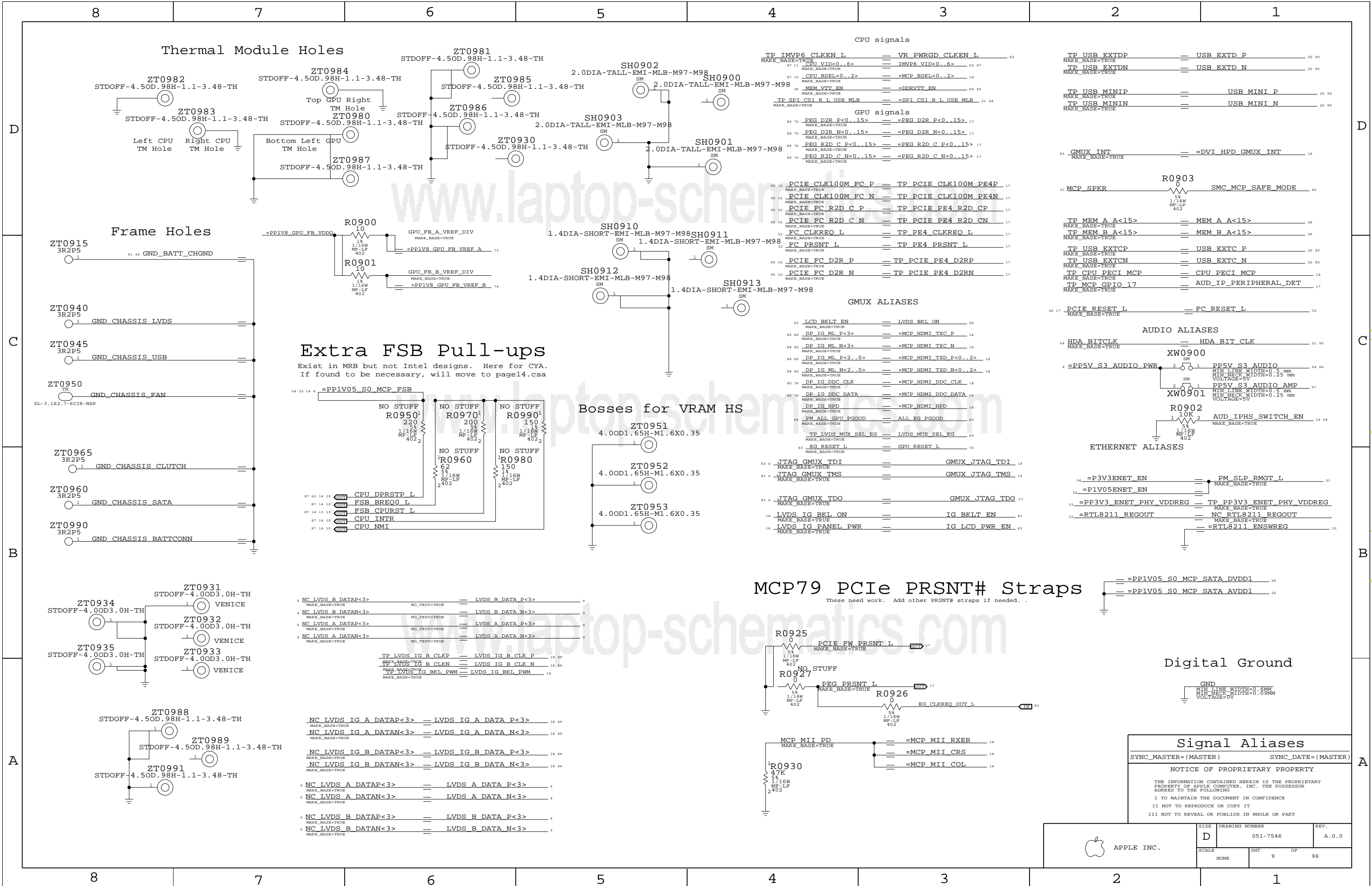
SIZE	D	DRAWING NUMBER	051-7546	REV.	A.0.0
SCALE	NONE	SHT	3	OF	96

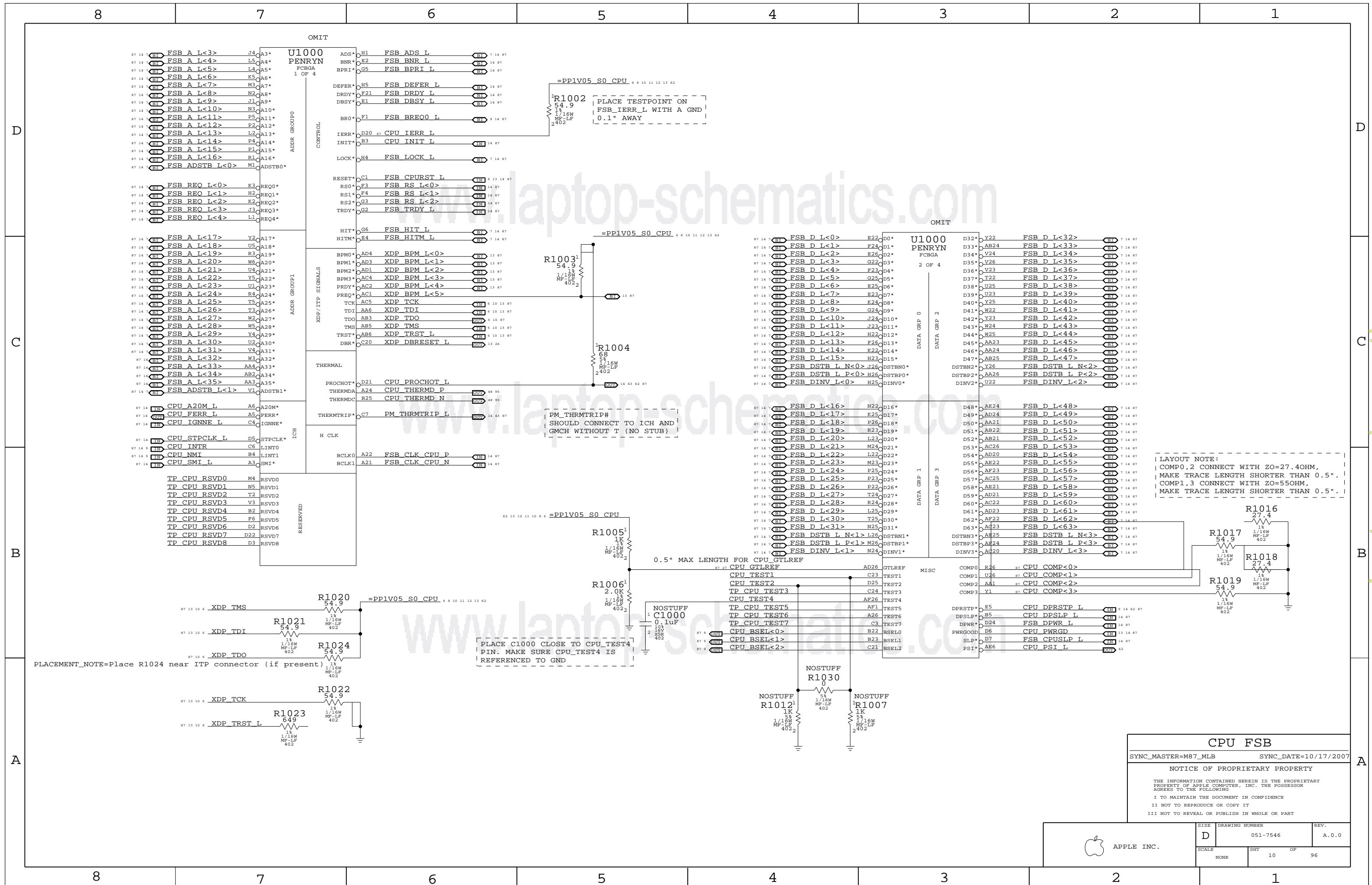


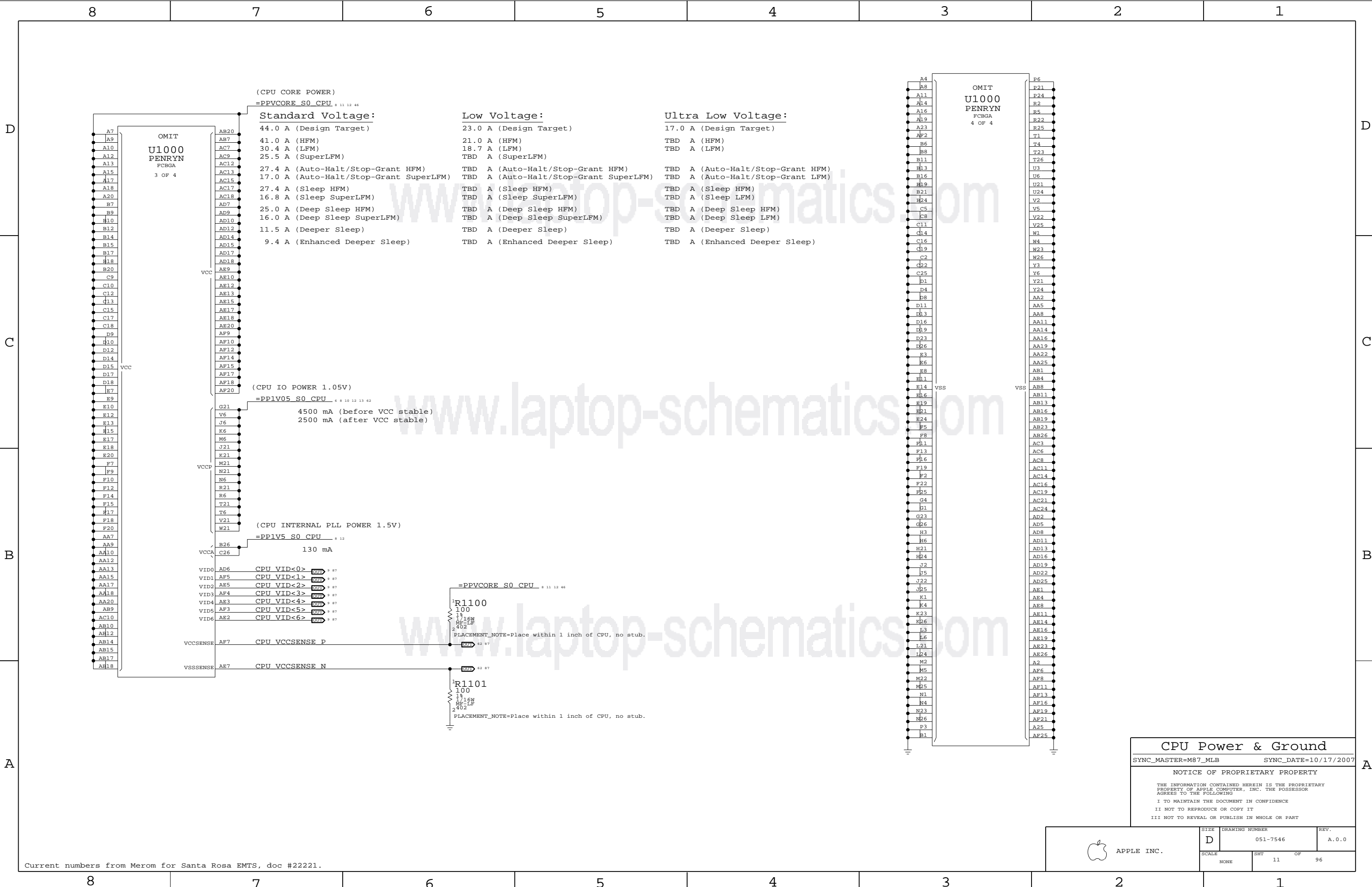
	8	7	6	5	4	3	2	1																																																																																																																								
D	BOM Variants																																																																																																																															
	<table><tr><th>BOM NUMBER</th><th>BOM NAME</th><th>BOM OPTIONS</th></tr><tr><td>630-9334</td><td>PCBA, 2.4GHZ, 256SAM_VRAM, M98</td><td>M98_COMMON, EEE_OZA, CPU_2_4GHZ, FB_256_SAMSUNG</td></tr><tr><td>630-9335</td><td>PCBA, 2.4GHZ, 256HYN_VRAM, M98</td><td>M98_COMMON, EEE_OZB, CPU_2_4GHZ, FB_256_HYNIX</td></tr><tr><td>630-9336</td><td>PCBA, 2.5GHZ, 512SAM_VRAM, M98</td><td>M98_COMMON, EEE_OZC, CPU_2_5GHZ, FB_512_SAMSUNG</td></tr><tr><td>630-9337</td><td>PCBA, 2.5GHZ, 512QIM_VRAM, M98</td><td>M98_COMMON, EEE_OZD, CPU_2_5GHZ, FB_512_QIMONDA</td></tr><tr><td>630-9585</td><td>PCBA, 2.8GHZ, 512SAM_VRAM, M98</td><td>M98_COMMON, EEE_2NH, CPU_2_8GHZ, FB_512_SAMSUNG</td></tr><tr><td>630-9586</td><td>PCBA, 2.8GHZ, 512QIM_VRAM, M98</td><td>M98_COMMON, EEE_2NJ, CPU_2_8GHZ, FB_512_QIMONDA</td></tr></table>								BOM NUMBER	BOM NAME	BOM OPTIONS	630-9334	PCBA, 2.4GHZ, 256SAM_VRAM, M98	M98_COMMON, EEE_OZA, CPU_2_4GHZ, FB_256_SAMSUNG	630-9335	PCBA, 2.4GHZ, 256HYN_VRAM, M98	M98_COMMON, EEE_OZB, CPU_2_4GHZ, FB_256_HYNIX	630-9336	PCBA, 2.5GHZ, 512SAM_VRAM, M98	M98_COMMON, EEE_OZC, CPU_2_5GHZ, FB_512_SAMSUNG	630-9337	PCBA, 2.5GHZ, 512QIM_VRAM, M98	M98_COMMON, EEE_OZD, CPU_2_5GHZ, FB_512_QIMONDA	630-9585	PCBA, 2.8GHZ, 512SAM_VRAM, M98	M98_COMMON, EEE_2NH, CPU_2_8GHZ, FB_512_SAMSUNG	630-9586	PCBA, 2.8GHZ, 512QIM_VRAM, M98	M98_COMMON, EEE_2NJ, CPU_2_8GHZ, FB_512_QIMONDA																																																																																																			
	BOM NUMBER	BOM NAME	BOM OPTIONS																																																																																																																													
	630-9334	PCBA, 2.4GHZ, 256SAM_VRAM, M98	M98_COMMON, EEE_OZA, CPU_2_4GHZ, FB_256_SAMSUNG																																																																																																																													
	630-9335	PCBA, 2.4GHZ, 256HYN_VRAM, M98	M98_COMMON, EEE_OZB, CPU_2_4GHZ, FB_256_HYNIX																																																																																																																													
	630-9336	PCBA, 2.5GHZ, 512SAM_VRAM, M98	M98_COMMON, EEE_OZC, CPU_2_5GHZ, FB_512_SAMSUNG																																																																																																																													
	630-9337	PCBA, 2.5GHZ, 512QIM_VRAM, M98	M98_COMMON, EEE_OZD, CPU_2_5GHZ, FB_512_QIMONDA																																																																																																																													
	630-9585	PCBA, 2.8GHZ, 512SAM_VRAM, M98	M98_COMMON, EEE_2NH, CPU_2_8GHZ, FB_512_SAMSUNG																																																																																																																													
	630-9586	PCBA, 2.8GHZ, 512QIM_VRAM, M98	M98_COMMON, EEE_2NJ, CPU_2_8GHZ, FB_512_QIMONDA																																																																																																																													
	M98 BOM Groups																																																																																																																															
<table><tr><th>BOM GROUP</th><th>BOM OPTIONS</th></tr><tr><td>M98_COMMON</td><td>ALTERNATE, COMMON, M98_COMMON1, M98_COMMON2, M98_COMMON3, M98_DEBUG, M98_PROGPARTS</td></tr><tr><td>M98_COMMON1</td><td>ONEWIRE_PU, ISL6258A, MEMRESET_HW, MEMRESET_MCP, MCP_B02, MCP_PROD, MCPSEQ_SMC</td></tr><tr><td>M98_COMMON2</td><td>BKLT_PLL_NOT, BMON_ENG, MIKEY, BOOT_MODE_USER, GPUVID_1P00V, MUXGFX</td></tr><tr><td>M98_COMMON3</td><td>DPMUX_EN_S0, DP_ESD, EG_PWRSEQ_HW, DP_CA_DET_EG_PLD, MCP_CS1_NO</td></tr><tr><td>M98_DEBUG</td><td>SMC_DEBUG_YES, XDP, LPCPLUS, VREFMRGN</td></tr><tr><td>M98_PROGPARTS</td><td>GMUX_PROG, BOOTROM_PROG, SMC_PROG, TPAD_PROG</td></tr></table>								BOM GROUP	BOM OPTIONS	M98_COMMON	ALTERNATE, COMMON, M98_COMMON1, M98_COMMON2, M98_COMMON3, M98_DEBUG, M98_PROGPARTS	M98_COMMON1	ONEWIRE_PU, ISL6258A, MEMRESET_HW, MEMRESET_MCP, MCP_B02, MCP_PROD, MCPSEQ_SMC	M98_COMMON2	BKLT_PLL_NOT, BMON_ENG, MIKEY, BOOT_MODE_USER, GPUVID_1P00V, MUXGFX	M98_COMMON3	DPMUX_EN_S0, DP_ESD, EG_PWRSEQ_HW, DP_CA_DET_EG_PLD, MCP_CS1_NO	M98_DEBUG	SMC_DEBUG_YES, XDP, LPCPLUS, VREFMRGN	M98_PROGPARTS	GMUX_PROG, BOOTROM_PROG, SMC_PROG, TPAD_PROG																																																																																																											
BOM GROUP	BOM OPTIONS																																																																																																																															
M98_COMMON	ALTERNATE, COMMON, M98_COMMON1, M98_COMMON2, M98_COMMON3, M98_DEBUG, M98_PROGPARTS																																																																																																																															
M98_COMMON1	ONEWIRE_PU, ISL6258A, MEMRESET_HW, MEMRESET_MCP, MCP_B02, MCP_PROD, MCPSEQ_SMC																																																																																																																															
M98_COMMON2	BKLT_PLL_NOT, BMON_ENG, MIKEY, BOOT_MODE_USER, GPUVID_1P00V, MUXGFX																																																																																																																															
M98_COMMON3	DPMUX_EN_S0, DP_ESD, EG_PWRSEQ_HW, DP_CA_DET_EG_PLD, MCP_CS1_NO																																																																																																																															
M98_DEBUG	SMC_DEBUG_YES, XDP, LPCPLUS, VREFMRGN																																																																																																																															
M98_PROGPARTS	GMUX_PROG, BOOTROM_PROG, SMC_PROG, TPAD_PROG																																																																																																																															
<table><tr><th>BOM GROUP</th><th>BOM OPTIONS</th></tr><tr><td>FB_256_SAMSUNG</td><td>VRAM4, VRAM_256_SAMSUNG</td></tr><tr><td>FB_256_HYNIX</td><td>VRAM4, VRAM_256_HYNIX</td></tr><tr><td>FB_512_SAMSUNG</td><td>VRAM4, VRAM_512_SAMSUNG</td></tr><tr><td>FB_512_QIMONDA</td><td>VRAM4, VRAM_512_QIMONDA</td></tr></table>								BOM GROUP	BOM OPTIONS	FB_256_SAMSUNG	VRAM4, VRAM_256_SAMSUNG	FB_256_HYNIX	VRAM4, VRAM_256_HYNIX	FB_512_SAMSUNG	VRAM4, VRAM_512_SAMSUNG	FB_512_QIMONDA	VRAM4, VRAM_512_QIMONDA																																																																																																															
BOM GROUP	BOM OPTIONS																																																																																																																															
FB_256_SAMSUNG	VRAM4, VRAM_256_SAMSUNG																																																																																																																															
FB_256_HYNIX	VRAM4, VRAM_256_HYNIX																																																																																																																															
FB_512_SAMSUNG	VRAM4, VRAM_512_SAMSUNG																																																																																																																															
FB_512_QIMONDA	VRAM4, VRAM_512_QIMONDA																																																																																																																															
Bar Code Labels / EEE #'s																																																																																																																																
<table><tr><th>PART NUMBER</th><th>QTY</th><th>DESCRIPTION</th><th>REFERENCE DES</th><th>CRITICAL</th><th>BOM OPTION</th></tr><tr><td>826-4393</td><td>1</td><td>LBL, P/N LABEL, PCB, 28MM X 6 MM</td><td>[EEE:OZA]</td><td>CRITICAL</td><td>EEE_OZA</td></tr><tr><td>826-4393</td><td>1</td><td>LBL, P/N LABEL, PCB, 28MM X 6 MM</td><td>[EEE:OZB]</td><td>CRITICAL</td><td>EEE_OZB</td></tr><tr><td>826-4393</td><td>1</td><td>LBL, P/N LABEL, PCB, 28MM X 6 MM</td><td>[EEE:OZC]</td><td>CRITICAL</td><td>EEE_OZC</td></tr><tr><td>826-4393</td><td>1</td><td>LBL, P/N LABEL, PCB, 28MM X 6 MM</td><td>[EEE:OZD]</td><td>CRITICAL</td><td>EEE_OZD</td></tr><tr><td>826-4393</td><td>1</td><td>LBL, P/N LABEL, PCB, 28MM X 6 MM</td><td>[EEE:2NH]</td><td>CRITICAL</td><td>EEE_2NH</td></tr><tr><td>826-4393</td><td>1</td><td>LBL, P/N LABEL, PCB, 28MM X 6 MM</td><td>[EEE:2NJ]</td><td>CRITICAL</td><td>EEE_2NJ</td></tr></table>								PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:OZA]	CRITICAL	EEE_OZA	826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:OZB]	CRITICAL	EEE_OZB	826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:OZC]	CRITICAL	EEE_OZC	826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:OZD]	CRITICAL	EEE_OZD	826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:2NH]	CRITICAL	EEE_2NH	826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:2NJ]	CRITICAL	EEE_2NJ																																																																															
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION																																																																																																																											
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:OZA]	CRITICAL	EEE_OZA																																																																																																																											
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:OZB]	CRITICAL	EEE_OZB																																																																																																																											
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:OZC]	CRITICAL	EEE_OZC																																																																																																																											
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:OZD]	CRITICAL	EEE_OZD																																																																																																																											
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:2NH]	CRITICAL	EEE_2NH																																																																																																																											
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:2NJ]	CRITICAL	EEE_2NJ																																																																																																																											
C	Module Parts																																																																																																																															
	<table><tr><th>PART NUMBER</th><th>QTY</th><th>DESCRIPTION</th><th>REFERENCE DES</th><th>CRITICAL</th><th>BOM OPTION</th></tr><tr><td>337S3639</td><td>1</td><td>IC, PDC, SLB4N, FRQ, 2.4G, 25W, 1066, M0, 3M, BGA</td><td>U1000</td><td>CRITICAL</td><td>CPU_2_4GHZ</td></tr><tr><td>337S3640</td><td>1</td><td>IC, PDC, SL3BX, FRQ, 2.53G, 35W, 1066, C0, 6M, BGA</td><td>U1000</td><td>CRITICAL</td><td>CPU_2_5GHZ</td></tr><tr><td>338S0554</td><td>1</td><td>IC, GPU, 55nm, NV G96-GS, BGA969, LF</td><td>U8000</td><td>CRITICAL</td><td></td></tr><tr><td>338S0570</td><td>1</td><td>IC, RTL8211CL, GIGE TRANSCEIVER, 48P TQFP</td><td>U3700</td><td>CRITICAL</td><td></td></tr><tr><td>338S0523</td><td>1</td><td>IC, FW643-06, 1394B PHY/ONCI LINK/PCI-E, 12</td><td>U4100</td><td>CRITICAL</td><td></td></tr><tr><td>338S0600</td><td>1</td><td>IC, GMCP, MCP79-B01, 35x35MM, BGA1437</td><td>U1400</td><td>CRITICAL</td><td>MCP_B01</td></tr><tr><td>338S0563</td><td>1</td><td>IC, SMC, HS8/2117, 9MMX9MM, TLP</td><td>U4900</td><td>CRITICAL</td><td>SMC_BLANK</td></tr><tr><td>341S2289</td><td>1</td><td>IC, SMC, DEVELOPMENT, M98</td><td>U4900</td><td>CRITICAL</td><td>SMC_PROG</td></tr><tr><td>335S0384</td><td>1</td><td>IC, 32MBIT 8-PIN SPI SERIAL FLASH, SOIC8</td><td>U6100</td><td>CRITICAL</td><td>BOOTROM_BLANK</td></tr><tr><td>341S2366</td><td>1</td><td>IC, EFI ROM, DEVELOPMENT, M98</td><td>U6100</td><td>CRITICAL</td><td>BOOTROM_PROG</td></tr><tr><td>341S2272</td><td>1</td><td>IC, HDCP ROM, NVG96, 8 PIN SOIC, LF, HF</td><td>U8770</td><td>CRITICAL</td><td>HDCP_YES</td></tr><tr><td>341S2384</td><td>1</td><td>IR, ENCORE II, CY7C63803-LQXC</td><td>U4800</td><td>CRITICAL</td><td></td></tr><tr><td>338S0635</td><td>1</td><td>IC, GMCP, MCP79-B02, 35x35MM, BGA1437</td><td>U1400</td><td>CRITICAL</td><td>MCP_B02</td></tr><tr><td>341S2383</td><td>1</td><td>IC, PSOC +W/USB, 56PIN, MLF, M98</td><td>U5701</td><td>CRITICAL</td><td>TPAD_PROG</td></tr><tr><td>337S3641</td><td>1</td><td>IC, PDC, SLB43, FRQ, 2.8G, 35W, 1066, C0, 6M, BGA</td><td>U1000</td><td>CRITICAL</td><td>CPU_2_8GHZ</td></tr><tr><td>333S0482</td><td>4</td><td>IC, SGRAM, GDDR3, 16Mx32, 800MHZ, 136 FBGA</td><td>U8400, U8450, U8500, U8550</td><td>CRITICAL</td><td>VRAM_256_SAMSUNG</td></tr><tr><td>333S0483</td><td>4</td><td>IC, SGRAM, GDDR3, 16Mx32, 900MHZ, 136 FBGA</td><td>U8400, U8450, U8500, U8550</td><td>CRITICAL</td><td>VRAM_256_HYNIX</td></tr><tr><td>333S0481</td><td>4</td><td>IC, SGRAM, GDDR3, 32Mx32, 900MHZ, 136 FBGA</td><td>U8400, U8450, U8500, U8550</td><td>CRITICAL</td><td>VRAM_512_SAMSUNG</td></tr><tr><td>333S0472</td><td>4</td><td>IC, SGRAM, GDDR3, 32Mx32, 900MHZ, 136 FBGA</td><td>U8400, U8450, U8500, U8550</td><td>CRITICAL</td><td>VRAM_512_QIMONDA</td></tr></table>								PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	337S3639	1	IC, PDC, SLB4N, FRQ, 2.4G, 25W, 1066, M0, 3M, BGA	U1000	CRITICAL	CPU_2_4GHZ	337S3640	1	IC, PDC, SL3BX, FRQ, 2.53G, 35W, 1066, C0, 6M, BGA	U1000	CRITICAL	CPU_2_5GHZ	338S0554	1	IC, GPU, 55nm, NV G96-GS, BGA969, LF	U8000	CRITICAL		338S0570	1	IC, RTL8211CL, GIGE TRANSCEIVER, 48P TQFP	U3700	CRITICAL		338S0523	1	IC, FW643-06, 1394B PHY/ONCI LINK/PCI-E, 12	U4100	CRITICAL		338S0600	1	IC, GMCP, MCP79-B01, 35x35MM, BGA1437	U1400	CRITICAL	MCP_B01	338S0563	1	IC, SMC, HS8/2117, 9MMX9MM, TLP	U4900	CRITICAL	SMC_BLANK	341S2289	1	IC, SMC, DEVELOPMENT, M98	U4900	CRITICAL	SMC_PROG	335S0384	1	IC, 32MBIT 8-PIN SPI SERIAL FLASH, SOIC8	U6100	CRITICAL	BOOTROM_BLANK	341S2366	1	IC, EFI ROM, DEVELOPMENT, M98	U6100	CRITICAL	BOOTROM_PROG	341S2272	1	IC, HDCP ROM, NVG96, 8 PIN SOIC, LF, HF	U8770	CRITICAL	HDCP_YES	341S2384	1	IR, ENCORE II, CY7C63803-LQXC	U4800	CRITICAL		338S0635	1	IC, GMCP, MCP79-B02, 35x35MM, BGA1437	U1400	CRITICAL	MCP_B02	341S2383	1	IC, PSOC +W/USB, 56PIN, MLF, M98	U5701	CRITICAL	TPAD_PROG	337S3641	1	IC, PDC, SLB43, FRQ, 2.8G, 35W, 1066, C0, 6M, BGA	U1000	CRITICAL	CPU_2_8GHZ	333S0482	4	IC, SGRAM, GDDR3, 16Mx32, 800MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_256_SAMSUNG	333S0483	4	IC, SGRAM, GDDR3, 16Mx32, 900MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_256_HYNIX	333S0481	4	IC, SGRAM, GDDR3, 32Mx32, 900MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_512_SAMSUNG	333S0472	4	IC, SGRAM, GDDR3, 32Mx32, 900MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_512_QIMONDA
	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION																																																																																																																										
	337S3639	1	IC, PDC, SLB4N, FRQ, 2.4G, 25W, 1066, M0, 3M, BGA	U1000	CRITICAL	CPU_2_4GHZ																																																																																																																										
	337S3640	1	IC, PDC, SL3BX, FRQ, 2.53G, 35W, 1066, C0, 6M, BGA	U1000	CRITICAL	CPU_2_5GHZ																																																																																																																										
	338S0554	1	IC, GPU, 55nm, NV G96-GS, BGA969, LF	U8000	CRITICAL																																																																																																																											
	338S0570	1	IC, RTL8211CL, GIGE TRANSCEIVER, 48P TQFP	U3700	CRITICAL																																																																																																																											
	338S0523	1	IC, FW643-06, 1394B PHY/ONCI LINK/PCI-E, 12	U4100	CRITICAL																																																																																																																											
	338S0600	1	IC, GMCP, MCP79-B01, 35x35MM, BGA1437	U1400	CRITICAL	MCP_B01																																																																																																																										
	338S0563	1	IC, SMC, HS8/2117, 9MMX9MM, TLP	U4900	CRITICAL	SMC_BLANK																																																																																																																										
341S2289	1	IC, SMC, DEVELOPMENT, M98	U4900	CRITICAL	SMC_PROG																																																																																																																											
335S0384	1	IC, 32MBIT 8-PIN SPI SERIAL FLASH, SOIC8	U6100	CRITICAL	BOOTROM_BLANK																																																																																																																											
341S2366	1	IC, EFI ROM, DEVELOPMENT, M98	U6100	CRITICAL	BOOTROM_PROG																																																																																																																											
341S2272	1	IC, HDCP ROM, NVG96, 8 PIN SOIC, LF, HF	U8770	CRITICAL	HDCP_YES																																																																																																																											
341S2384	1	IR, ENCORE II, CY7C63803-LQXC	U4800	CRITICAL																																																																																																																												
338S0635	1	IC, GMCP, MCP79-B02, 35x35MM, BGA1437	U1400	CRITICAL	MCP_B02																																																																																																																											
341S2383	1	IC, PSOC +W/USB, 56PIN, MLF, M98	U5701	CRITICAL	TPAD_PROG																																																																																																																											
337S3641	1	IC, PDC, SLB43, FRQ, 2.8G, 35W, 1066, C0, 6M, BGA	U1000	CRITICAL	CPU_2_8GHZ																																																																																																																											
333S0482	4	IC, SGRAM, GDDR3, 16Mx32, 800MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_256_SAMSUNG																																																																																																																											
333S0483	4	IC, SGRAM, GDDR3, 16Mx32, 900MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_256_HYNIX																																																																																																																											
333S0481	4	IC, SGRAM, GDDR3, 32Mx32, 900MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_512_SAMSUNG																																																																																																																											
333S0472	4	IC, SGRAM, GDDR3, 32Mx32, 900MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_512_QIMONDA																																																																																																																											
B																																																																																																																																
A	<table><tr><th>PART NUMBER</th><th>ALTERNATE FOR PART NUMBER</th><th>BOM OPTION</th><th>REF DES</th><th>COMMENTS:</th></tr><tr><td>138S0603</td><td>138S0602</td><td></td><td>ALL</td><td>Murate alt to Samsung</td></tr><tr><td>353S1681</td><td>353S1294</td><td></td><td>ALL</td><td>ONYO211, ONAMP, GMS</td></tr><tr><td>152S0276</td><td>152S0683</td><td></td><td>ALL</td><td>Maplayers alt to Delta/Vishay</td></tr><tr><td>341S2367</td><td>341S2366</td><td></td><td>ALL</td><td>Macronix alt to SST</td></tr><tr><td>152S0876</td><td>152S0867</td><td></td><td>ALL</td><td>Maplayer alt to Delta</td></tr><tr><td>157S0058</td><td>157S0055</td><td></td><td>ALL</td><td>Delta alt to TDK Magnetics</td></tr><tr><td>353S2312</td><td>353S1466</td><td></td><td>ALL</td><td>INTERSEIL ALT TO INTERSEIL</td></tr><tr><td>514-0612</td><td>514-0607</td><td></td><td>ALL</td><td>FOXLINK ACVR ALT TO FOMCON</td></tr><tr><td>514-0613</td><td>514-0608</td><td></td><td>ALL</td><td>FOXLINK ACVR ALT TO FOMCON</td></tr><tr><td>152S0915</td><td>152S0796</td><td></td><td>ALL</td><td>Maplayers alt to Cytacoe LTD</td></tr></table>								PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	138S0603	138S0602		ALL	Murate alt to Samsung	353S1681	353S1294		ALL	ONYO211, ONAMP, GMS	152S0276	152S0683		ALL	Maplayers alt to Delta/Vishay	341S2367	341S2366		ALL	Macronix alt to SST	152S0876	152S0867		ALL	Maplayer alt to Delta	157S0058	157S0055		ALL	Delta alt to TDK Magnetics	353S2312	353S1466		ALL	INTERSEIL ALT TO INTERSEIL	514-0612	514-0607		ALL	FOXLINK ACVR ALT TO FOMCON	514-0613	514-0608		ALL	FOXLINK ACVR ALT TO FOMCON	152S0915	152S0796		ALL	Maplayers alt to Cytacoe LTD																																																																	
	PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:																																																																																																																											
	138S0603	138S0602		ALL	Murate alt to Samsung																																																																																																																											
	353S1681	353S1294		ALL	ONYO211, ONAMP, GMS																																																																																																																											
	152S0276	152S0683		ALL	Maplayers alt to Delta/Vishay																																																																																																																											
	341S2367	341S2366		ALL	Macronix alt to SST																																																																																																																											
	152S0876	152S0867		ALL	Maplayer alt to Delta																																																																																																																											
	157S0058	157S0055		ALL	Delta alt to TDK Magnetics																																																																																																																											
	353S2312	353S1466		ALL	INTERSEIL ALT TO INTERSEIL																																																																																																																											
	514-0612	514-0607		ALL	FOXLINK ACVR ALT TO FOMCON																																																																																																																											
514-0613	514-0608		ALL	FOXLINK ACVR ALT TO FOMCON																																																																																																																												
152S0915	152S0796		ALL	Maplayers alt to Cytacoe LTD																																																																																																																												
<table><tr><td colspan="4"></td><td colspan="4">BOM Configuration</td></tr><tr><td colspan="4">SYNC_MASTER=N/A</td><td colspan="4">SYNC_DATE=N/A</td></tr><tr><td colspan="8">NOTICE OF PROPRIETARY PROPERTY</td></tr><tr><td colspan="8">THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</td></tr><tr><td colspan="8">I I TO MAINTAIN THE DOCUMENT IN CONFIDENCE</td></tr><tr><td colspan="8">II NOT TO REPRODUCE OR COPY IT</td></tr><tr><td colspan="8">III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</td></tr></table>												BOM Configuration				SYNC_MASTER=N/A				SYNC_DATE=N/A				NOTICE OF PROPRIETARY PROPERTY								THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING								I I TO MAINTAIN THE DOCUMENT IN CONFIDENCE								II NOT TO REPRODUCE OR COPY IT								III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART																																																																								
				BOM Configuration																																																																																																																												
SYNC_MASTER=N/A				SYNC_DATE=N/A																																																																																																																												
NOTICE OF PROPRIETARY PROPERTY																																																																																																																																
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING																																																																																																																																
I I TO MAINTAIN THE DOCUMENT IN CONFIDENCE																																																																																																																																
II NOT TO REPRODUCE OR COPY IT																																																																																																																																
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART																																																																																																																																
<table><tr><td colspan="2" rowspan="2"> APPLE INC.</td><td>SIZE</td><td>DRAWING NUMBER</td><td>REV.</td></tr><tr><td>D</td><td>051-7546</td><td>A.0.0</td></tr><tr><td colspan="2">SCALE</td><td>SHT</td><td colspan="2">OF</td></tr><tr><td colspan="2">NONE</td><td>5</td><td colspan="2">96</td></tr></table>								 APPLE INC.		SIZE	DRAWING NUMBER	REV.	D	051-7546	A.0.0	SCALE		SHT	OF		NONE		5	96																																																																																																								
 APPLE INC.		SIZE	DRAWING NUMBER	REV.																																																																																																																												
		D	051-7546	A.0.0																																																																																																																												
SCALE		SHT	OF																																																																																																																													
NONE		5	96																																																																																																																													
	8	7	6	5	4	3	2	1																																																																																																																								











(CPU CORE POWER)

=PPVCORE_S0_CPU_8 11 12 46

Standard Voltage:

- 44.0 A (Design Target)
- 41.0 A (HFM)
- 30.4 A (LFM)
- 25.5 A (SuperLFM)
- 27.4 A (Auto-Halt/Stop-Grant HFM)
- 17.0 A (Auto-Halt/Stop-Grant SuperLFM)
- 27.4 A (Sleep HFM)
- 16.8 A (Sleep SuperLFM)
- 25.0 A (Deep Sleep HFM)
- 16.0 A (Deep Sleep SuperLFM)
- 11.5 A (Deeper Sleep)
- 9.4 A (Enhanced Deeper Sleep)

Low Voltage:

- 23.0 A (Design Target)
- 21.0 A (HFM)
- 18.7 A (LFM)
- TBD A (SuperLFM)
- TBD A (Auto-Halt/Stop-Grant HFM)
- TBD A (Auto-Halt/Stop-Grant SuperLFM)
- TBD A (Sleep HFM)
- TBD A (Sleep SuperLFM)
- TBD A (Deep Sleep HFM)
- TBD A (Deep Sleep SuperLFM)
- TBD A (Deeper Sleep)
- TBD A (Enhanced Deeper Sleep)

Ultra Low Voltage:

- 17.0 A (Design Target)
- TBD A (HFM)
- TBD A (LFM)
- TBD A (Auto-Halt/Stop-Grant HFM)
- TBD A (Auto-Halt/Stop-Grant LFM)
- TBD A (Sleep HFM)
- TBD A (Sleep LFM)
- TBD A (Deep Sleep HFM)
- TBD A (Deep Sleep LFM)
- TBD A (Deeper Sleep)
- TBD A (Enhanced Deeper Sleep)

OMIT
U1000
PENRYN
FCBGA
4 OF 4

CPU Power & Ground

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE DRAWING NUMBER REV.

D

051-7546

A.0.0

SCALE

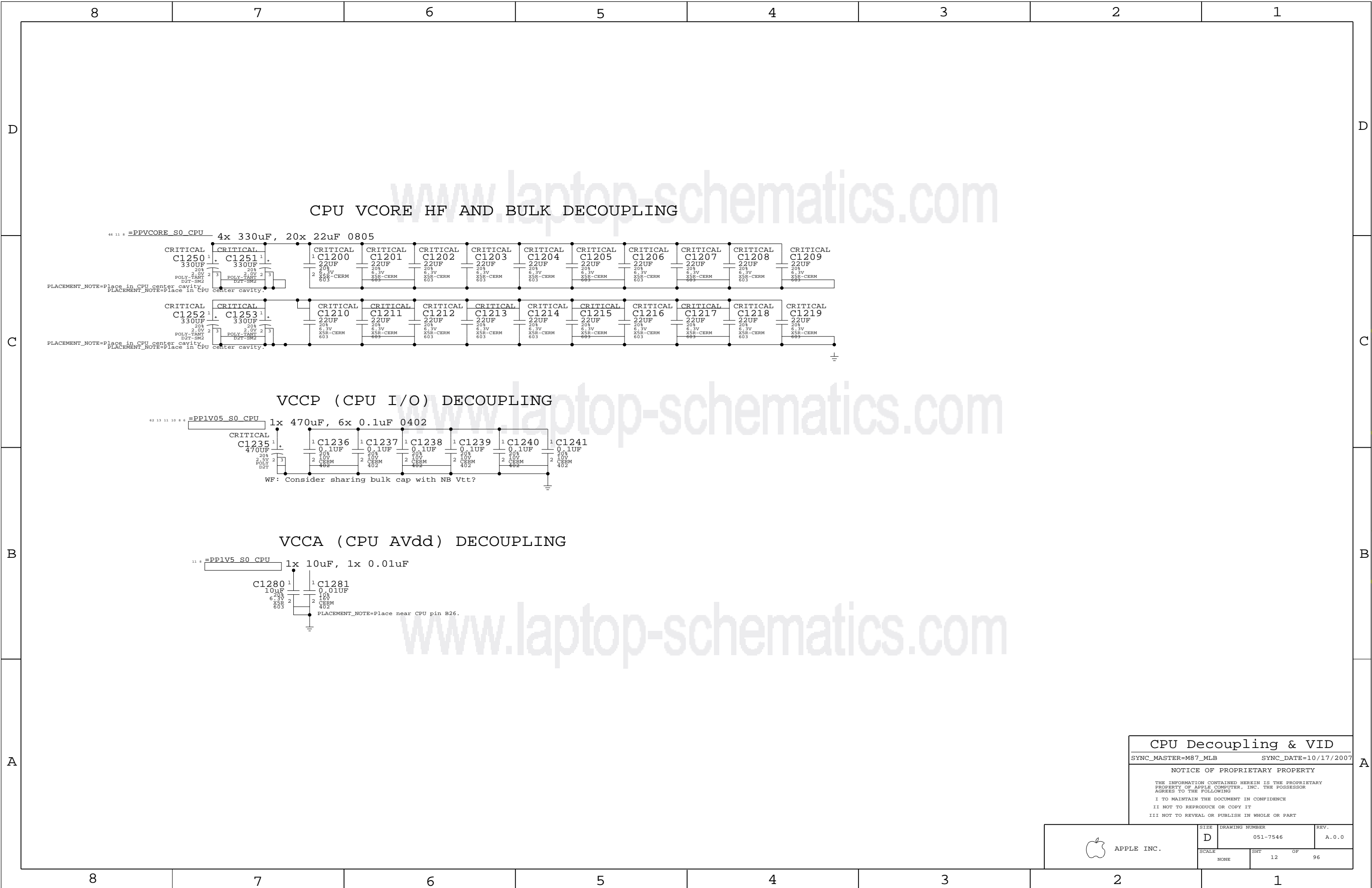
NONE

SHT

11

OF

96



CPU Decoupling & VID

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

NOTICE OF PROPRIETARY PROPERTY

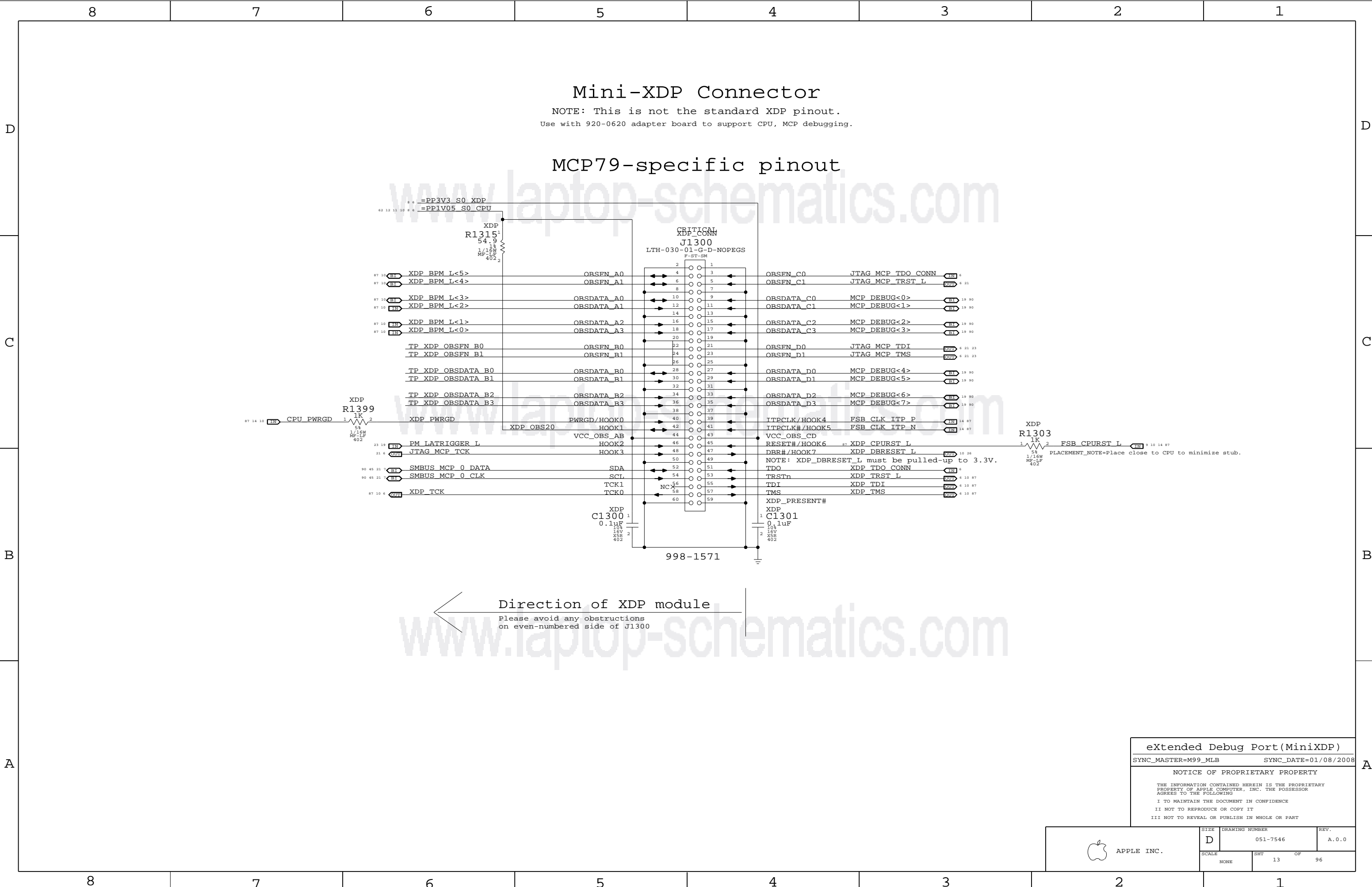
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE		SHT	OF
NONE		12	96



eXtended Debug Port (MiniXDP)

SYNC_MASTER=M99_MLB SYNC_DATE=01/08/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHT	OF
NONE	13	96





MCP Memory Interface

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008


NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE

D

DRAWING NUMBER

051-7546

REV.

A.0.0

SCALE

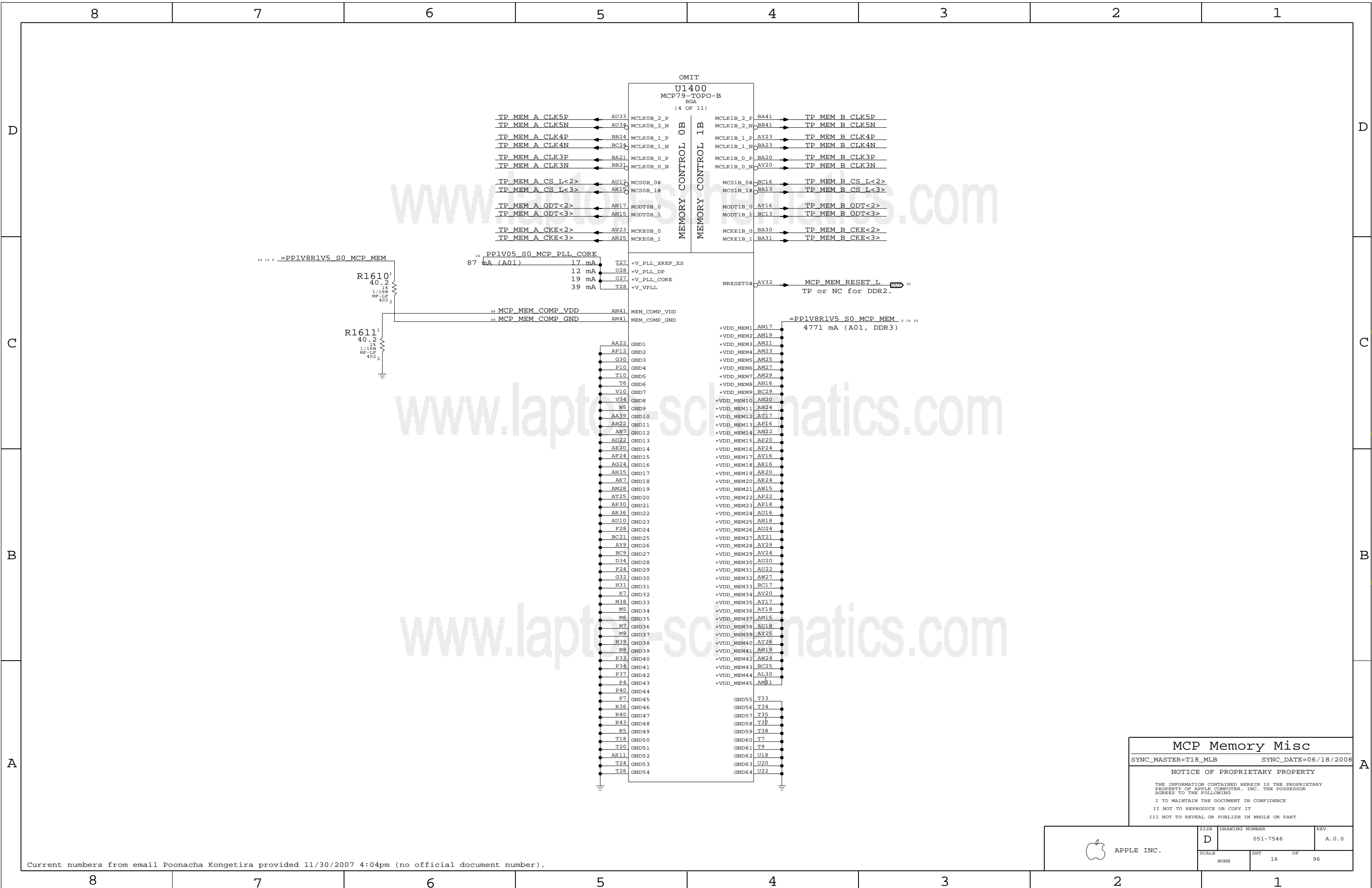
NONE

SHT

15

OF

96



Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Memory Misc

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008


NOTICE OF PROPRIETARY PROPERTY

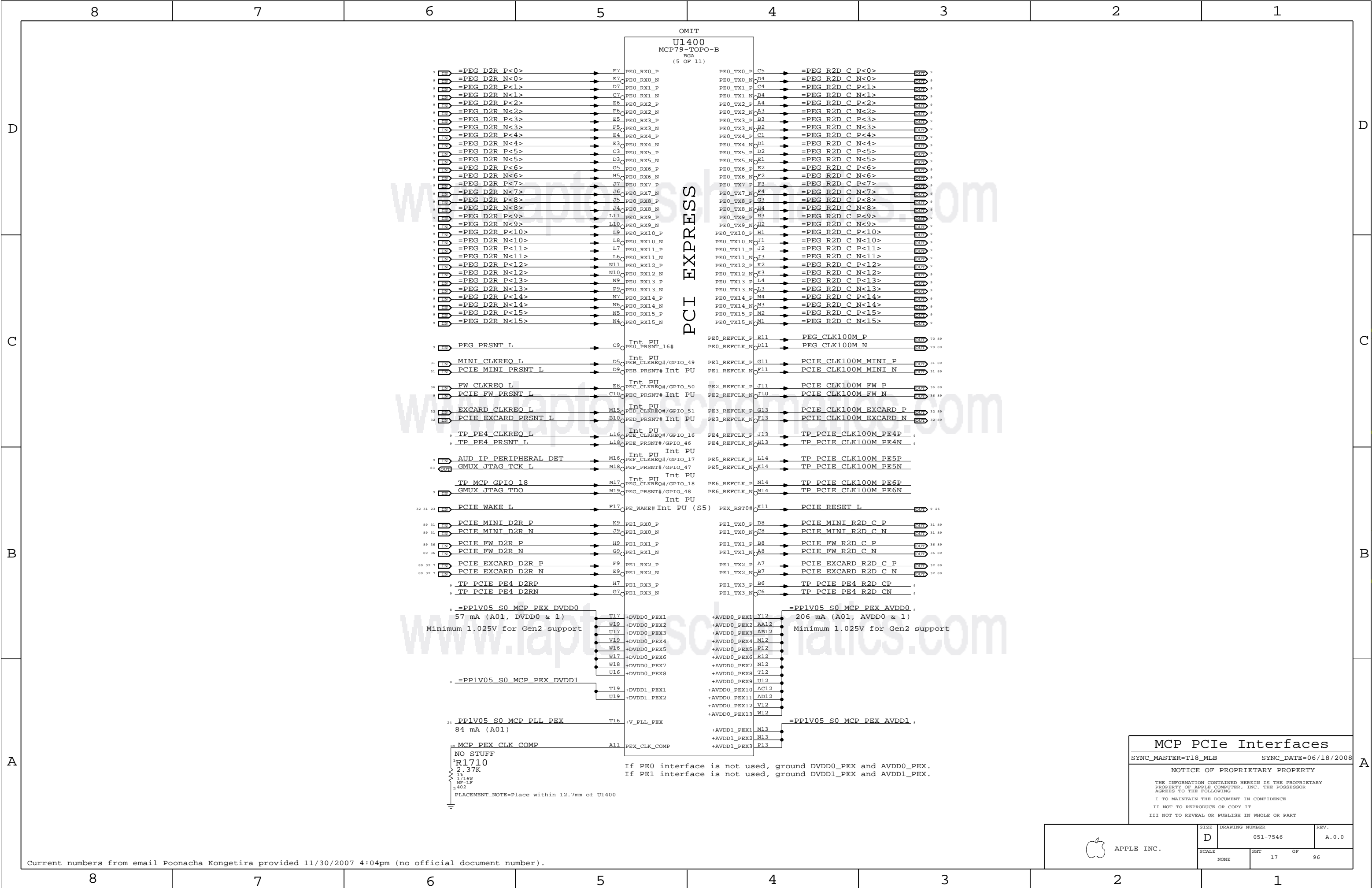
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE		SHT	OF
NONE		16	96



Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP PCIe Interfaces

SYNC_MASTER=T18_MLB

SYNC_DATE=06/18/2008

NOTICE OF PROPRIETARY PROPERTY

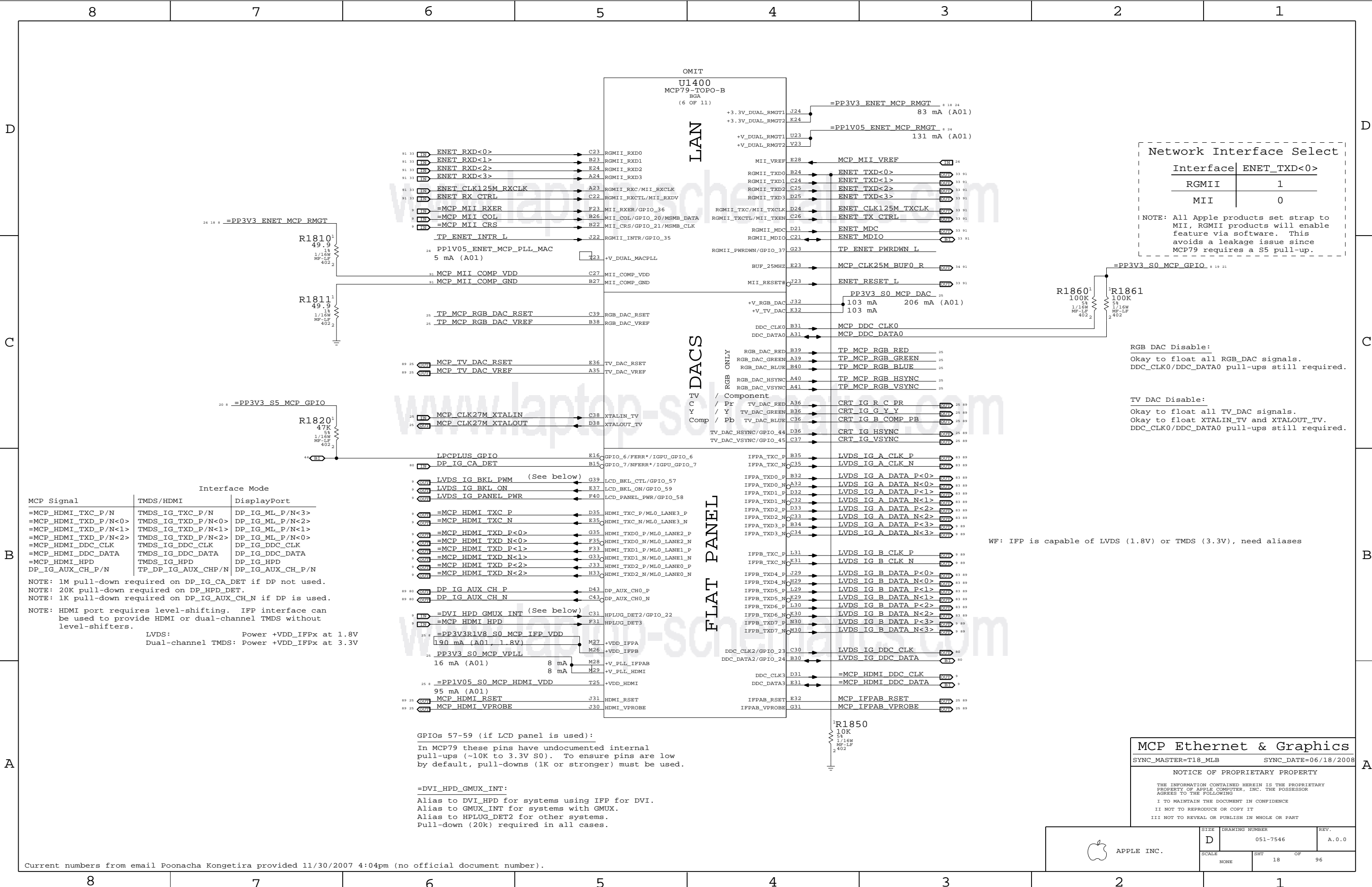
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE		SHT	OF
NONE		17	96



Interface Mode table with columns: MCP Signal, TMDS/HDMI, and DisplayPort. It lists various signal connections and includes notes about pull-down requirements and level-shifting for the HDMI port.

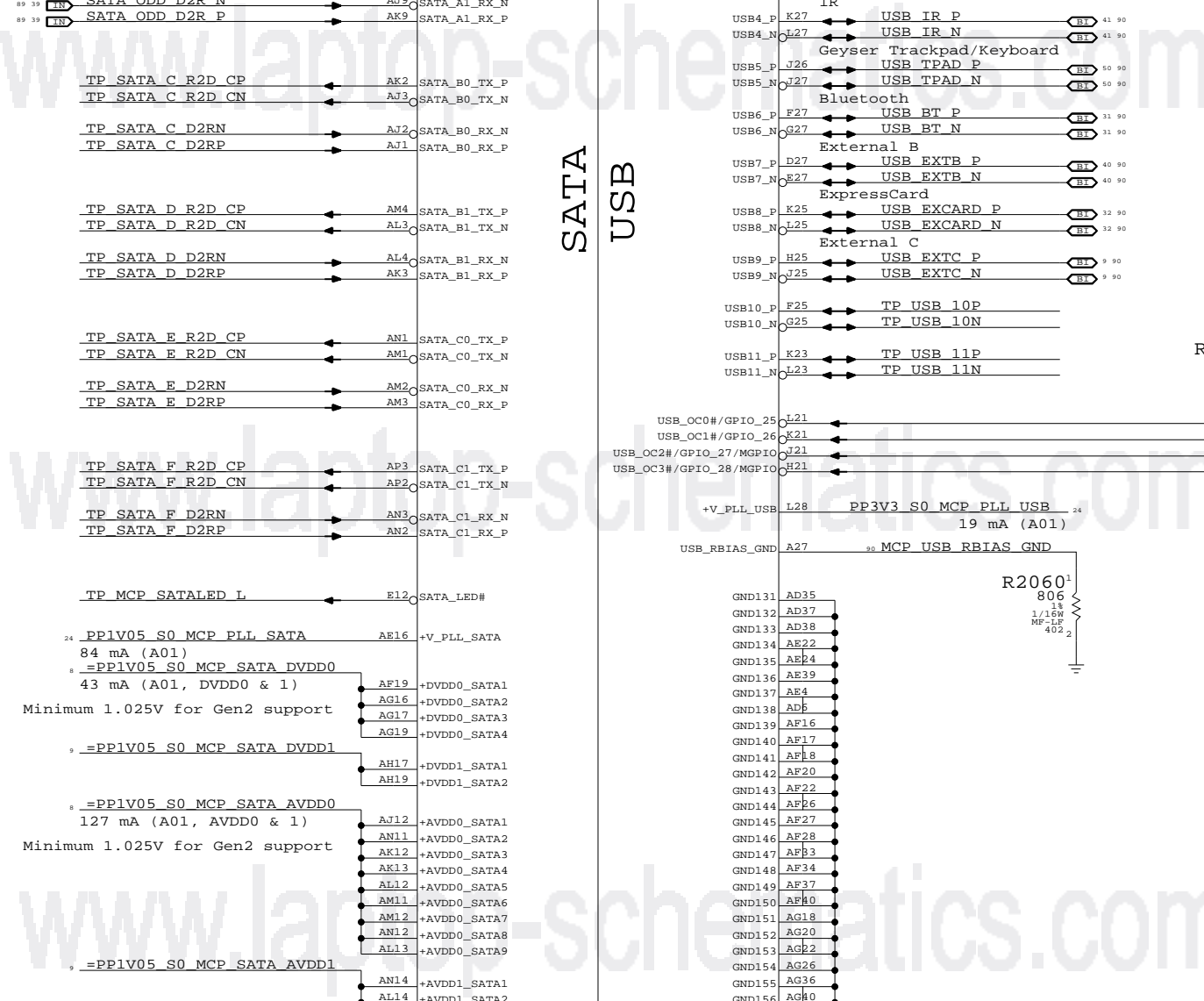
Network Interface Select table with columns: Interface and ENET_TXD<0>. It shows RGMII and MII interface options and includes a note about Apple products setting the strap to MII.

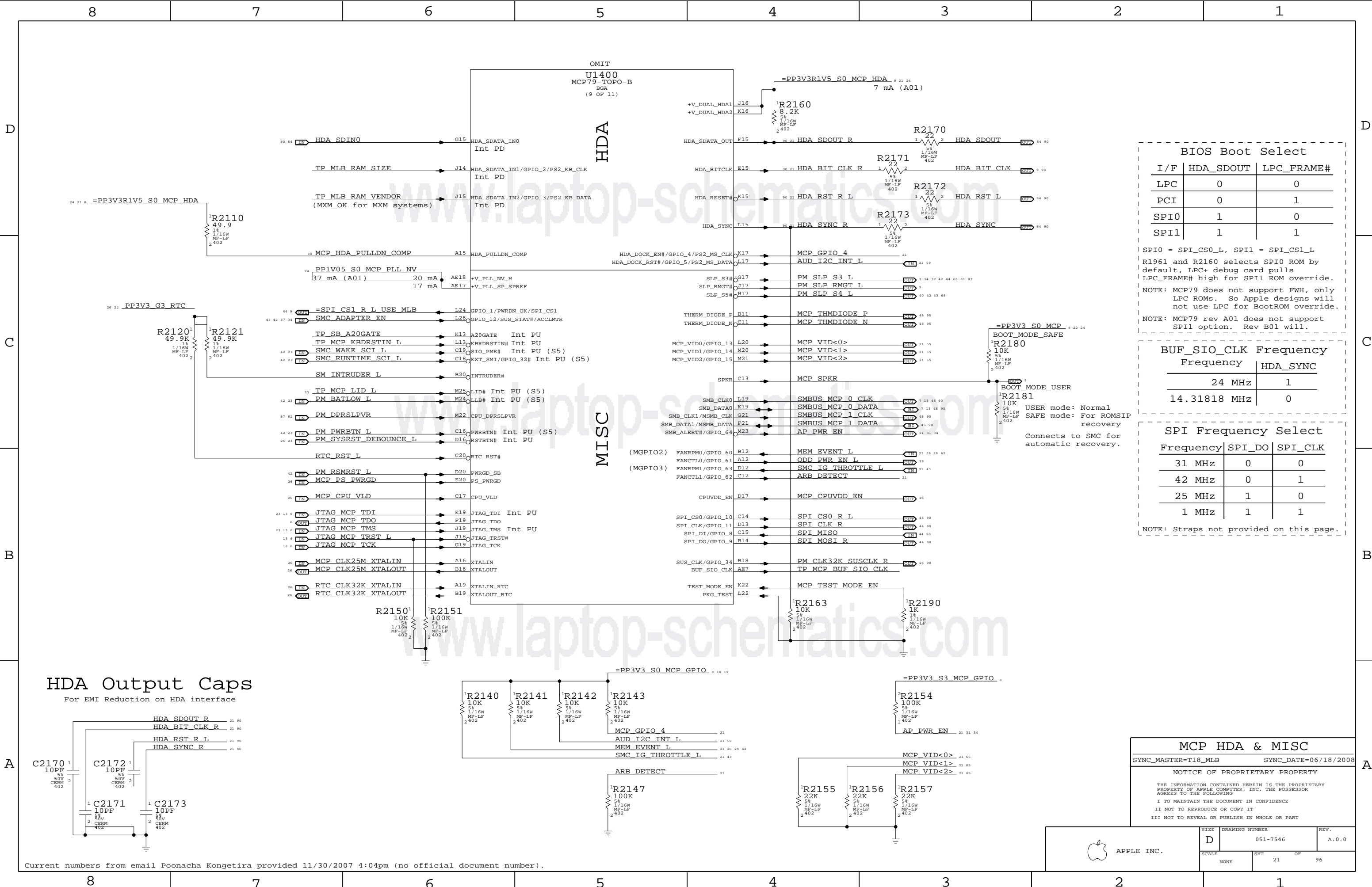
RGB DAC Disable: Okay to float all RGB_DAC signals. DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable: Okay to float all TV_DAC signals. Okay to float XTALIN_TV and XTALOUT_TV. DDC_CLK0/DDC_DATA0 pull-ups still required.

MCP Ethernet & Graphics section containing SYNC_MASTER=T18_MLB, SYNC_DATE=06/18/2008, and a NOTICE OF PROPRIETARY PROPERTY.

Apple Inc. logo and drawing information including size D, drawing number 051-7546, and revision A.0.0.





BIOS Boot Select		
I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

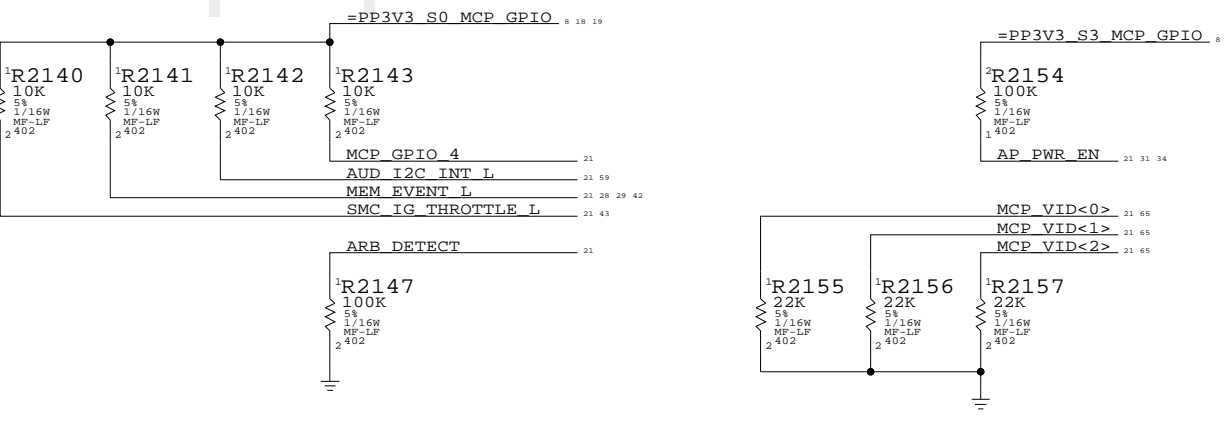
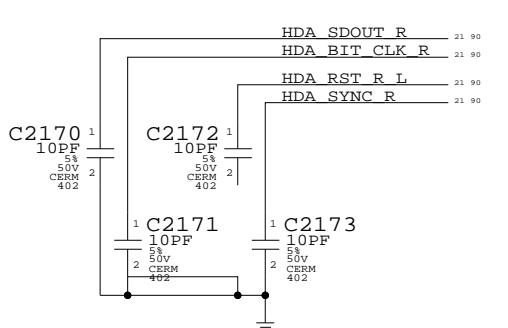
SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L
R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.
NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.
NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency	
Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select		
Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

HDA Output Caps
For EMI Reduction on HDA interface



MCP HDA & MISC

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE

D

DRAWING NUMBER

051-7546

REV.

A.0.0

SCALE

NONE

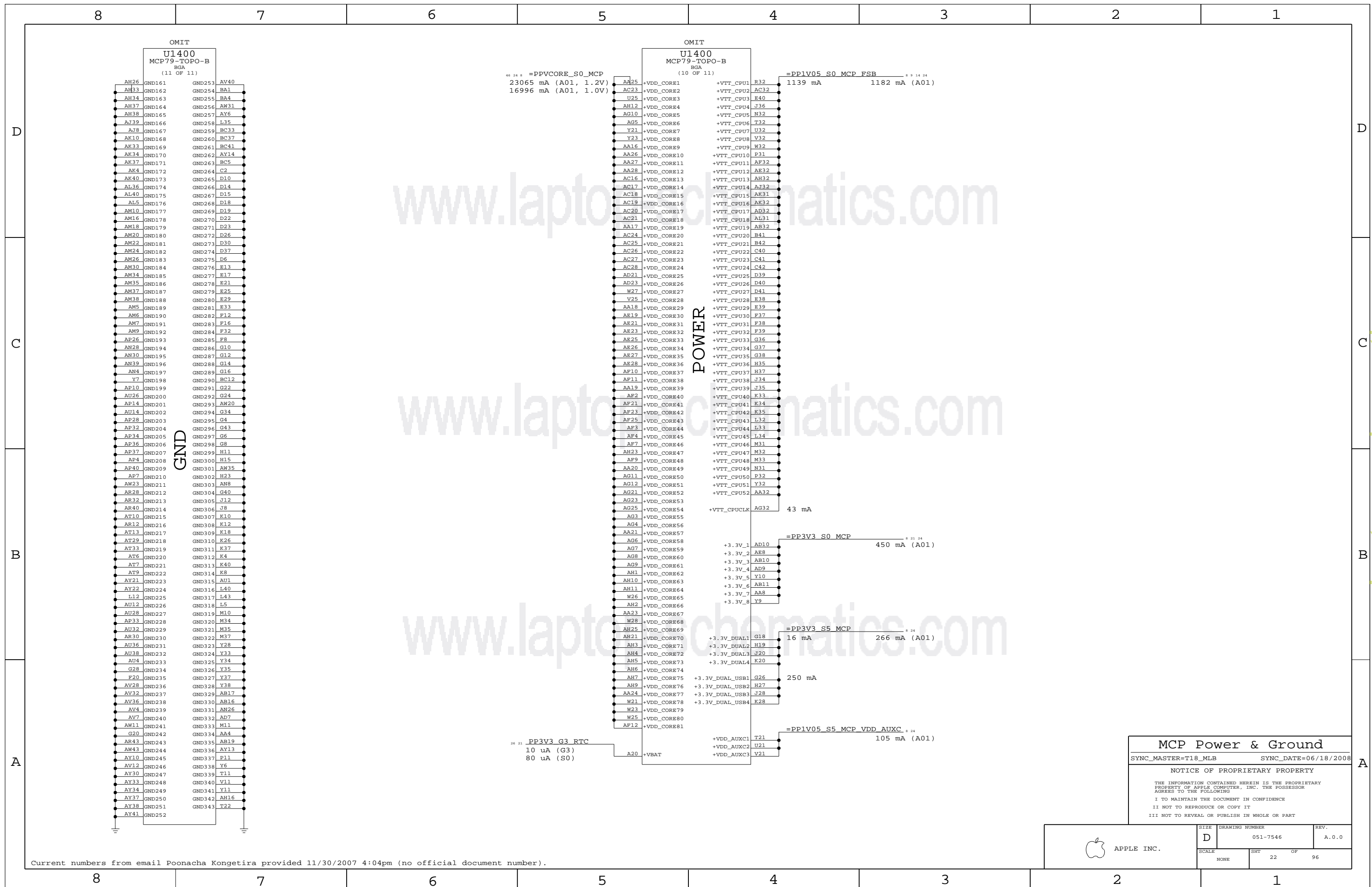
SHT

21

OF

96

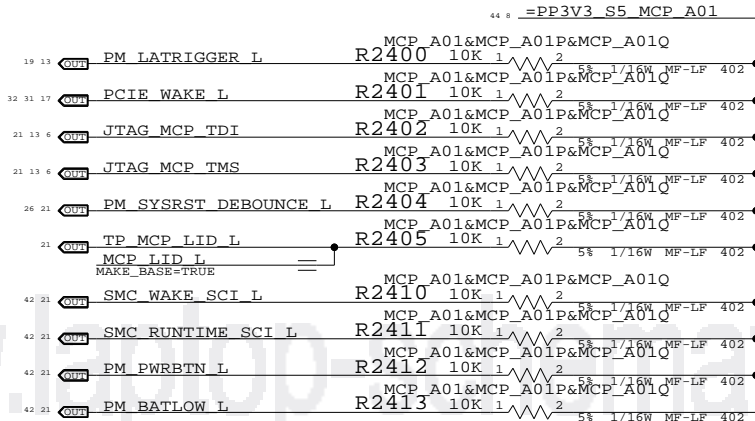
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



www.laptop-schematics.com

3.3V Interface Pull-ups

These internal pull-ups are missing in Revs A01 & A01P.



www.laptop-schematics.com

www.laptop-schematics.com

MCP79 A01 Silicon Support

SYNC_MASTER=T18_MLB SYNC_DATE=03/31/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE

D

DRAWING NUMBER

051-7546

REV.

A.0.0

SCALE

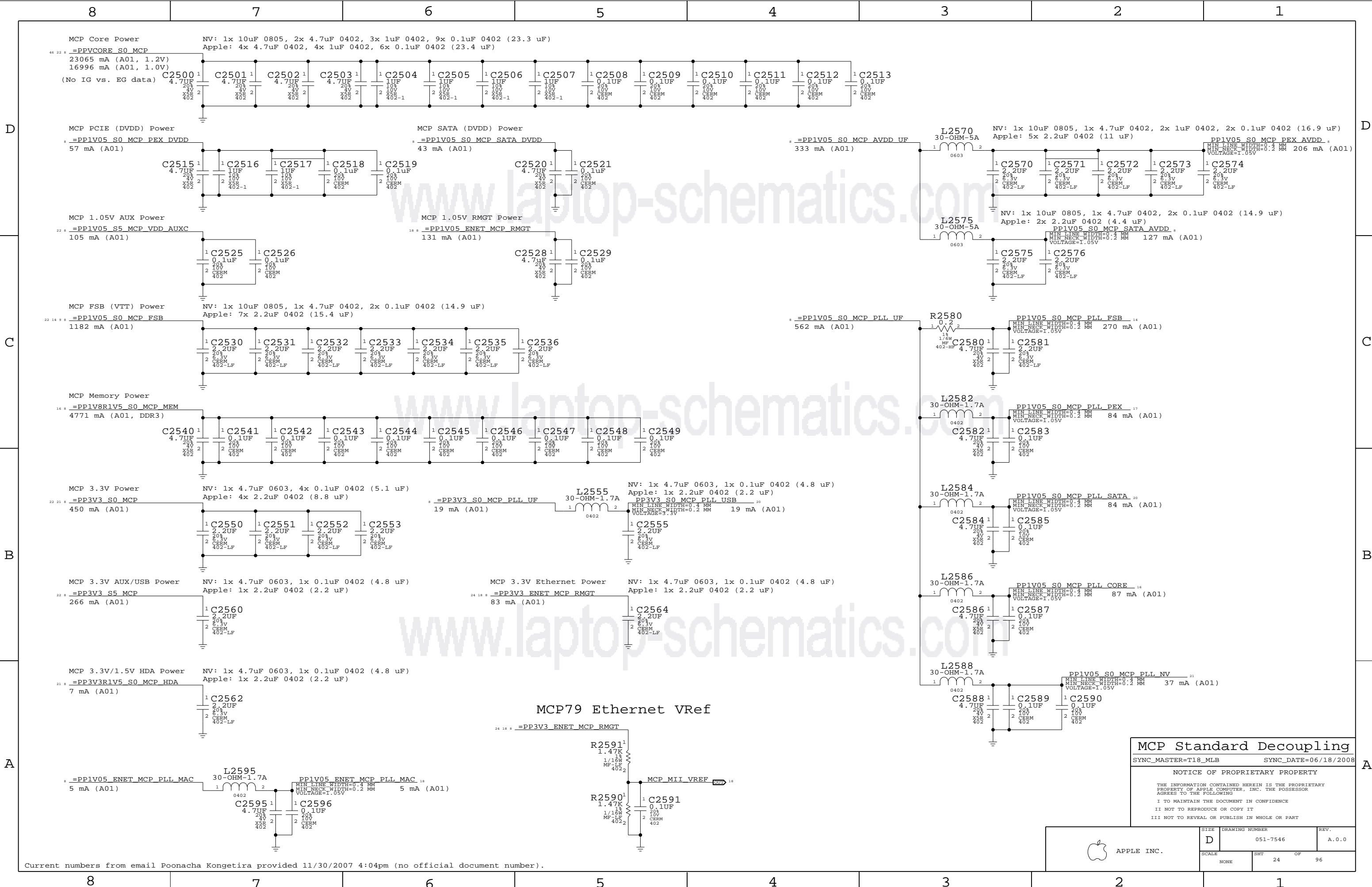
NONE

SHT

23

OF

96



Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Standard Decoupling

SYNC_MASTER=T18_MLB

SYNC_DATE=06/18/2008

NOTICE OF PROPRIETARY PROPERTY

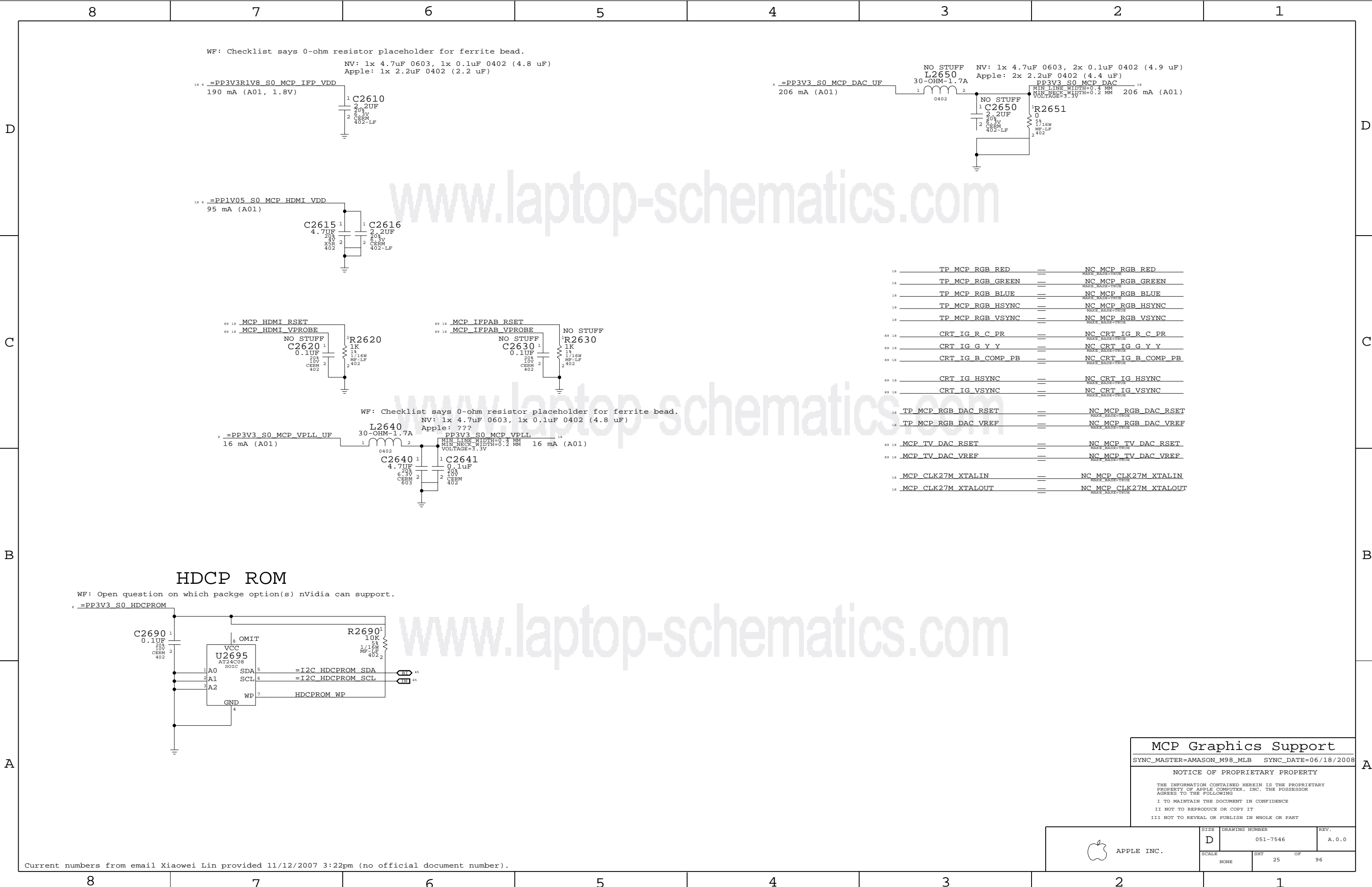
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER		REV.
	D	051-7546		A.0.0
SCALE		SHT	OF	96
NONE		24		



www.laptop-schematics.com

www.laptop-schematics.com

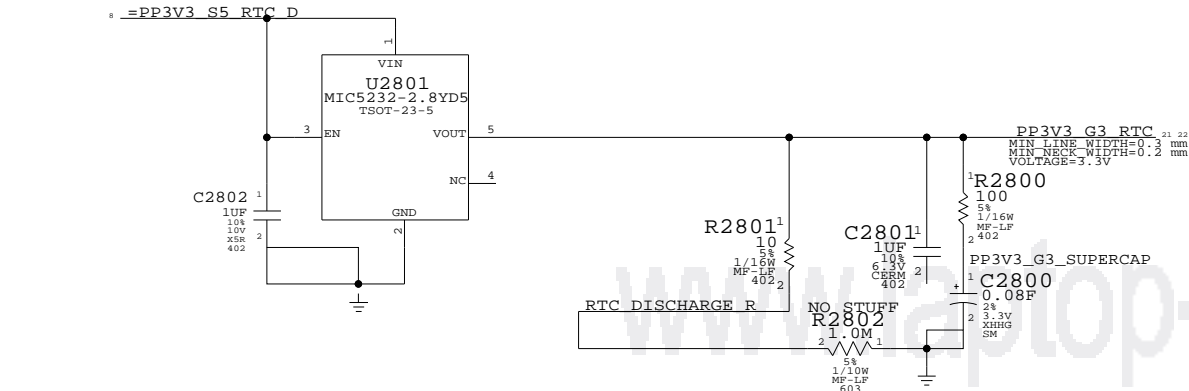
www.laptop-schematics.com

www.laptop-schematics.com

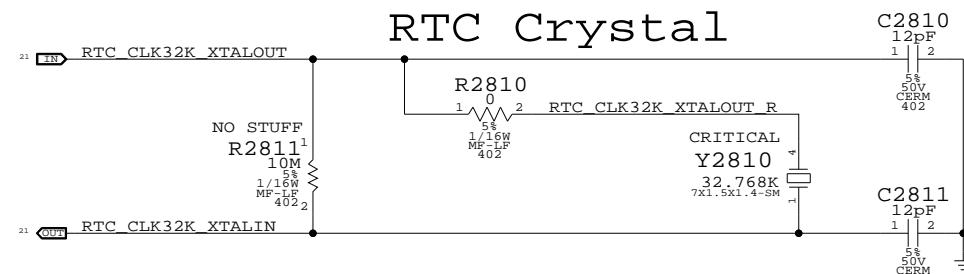
MCP Graphics Support
SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=06/18/2008
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER		REV.
	D	051-7546		A.0.0
SCALE		SHT	OF	REV.
NONE		25	96	

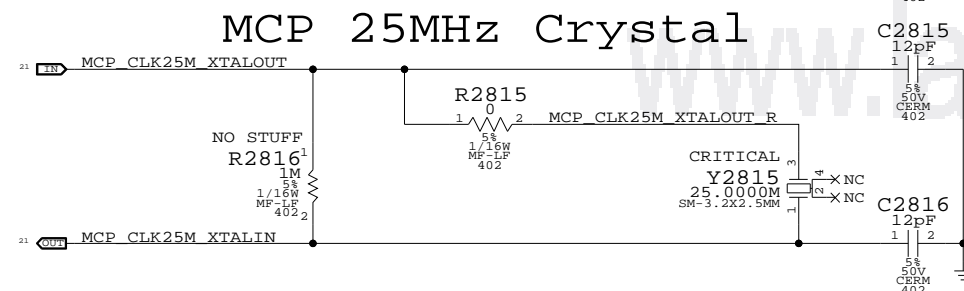
RTC Power Sources



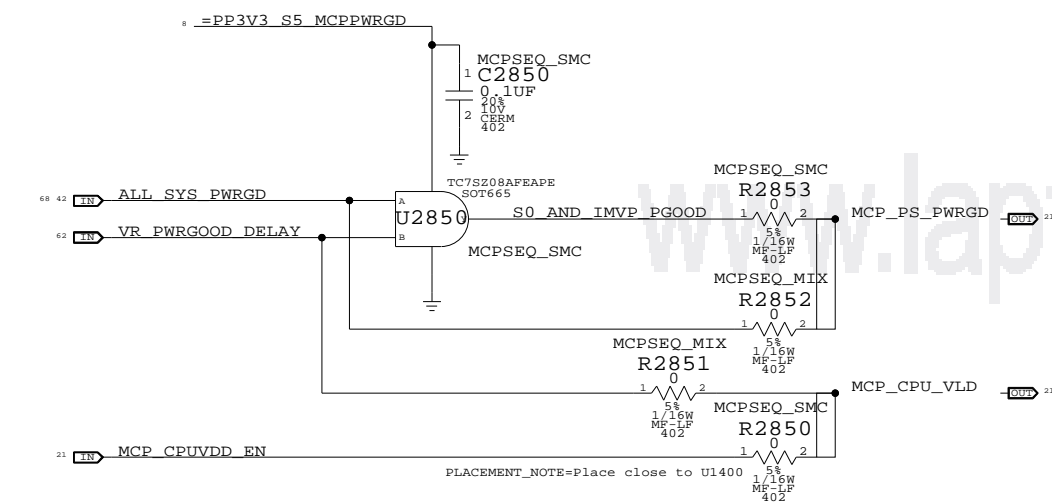
RTC Crystal



MCP 25MHz Crystal



MCP S0 PWRGD & CPU_VLD



MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up.

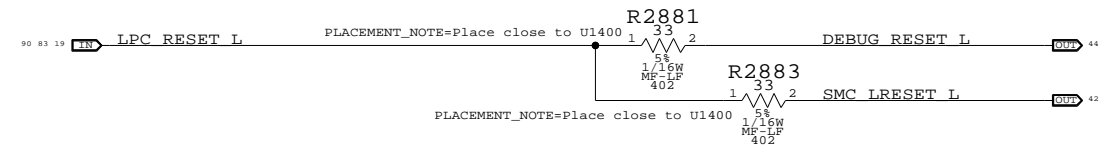
MCPSEQ_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP FSB I/O interface initialization.

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

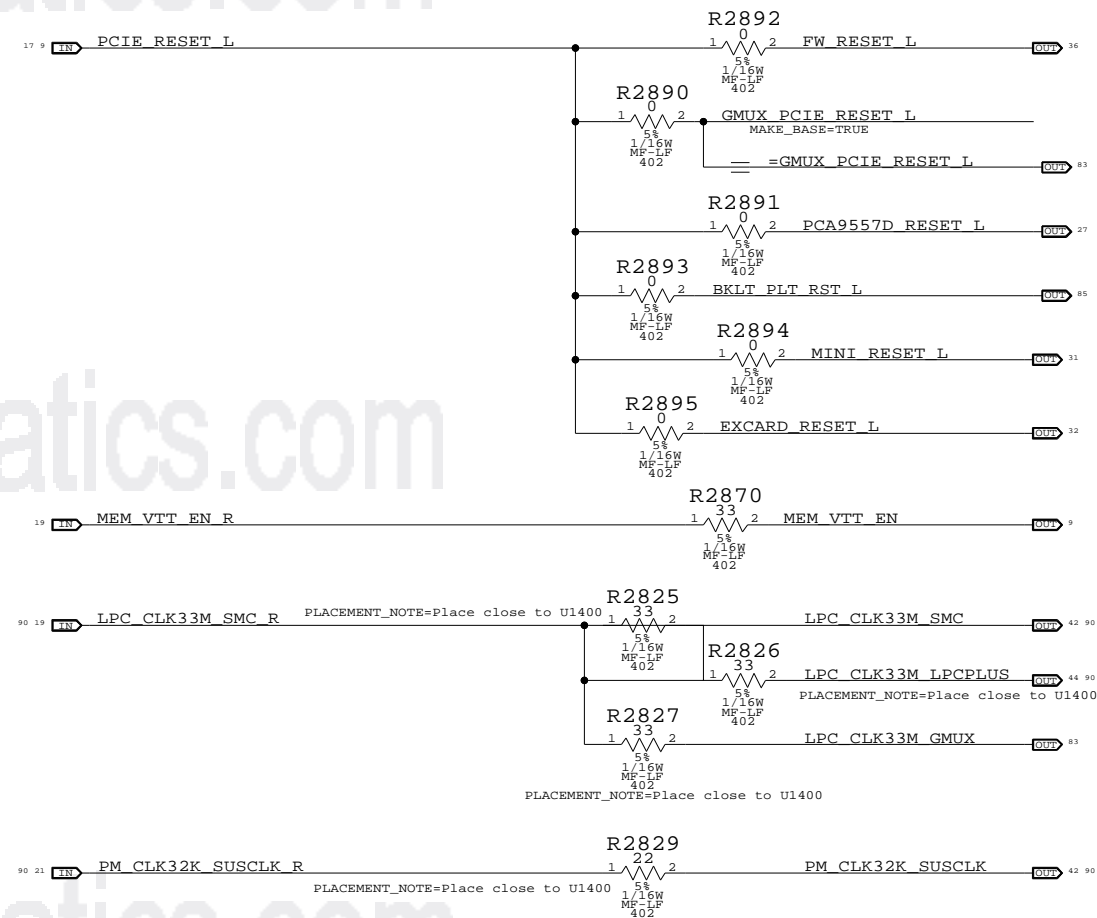
NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

Platform Reset Connections

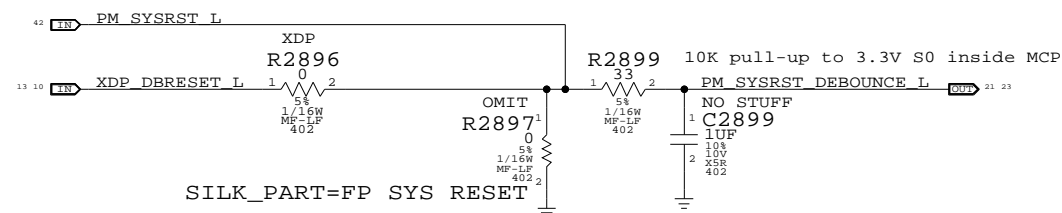
LPC Reset (Unbuffered)



PCIE Reset (Unbuffered)



Reset Button



<div>SB Misc</div>			
<div>SYNC_MASTER=TI8_MLB</div>		<div>SYNC_DATE=12/17/2007</div>	
<div>NOTICE OF PROPRIETARY PROPERTY</div>			
<div>THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</div>			
<div>I TO MAINTAIN THE DOCUMENT IN CONFIDENCE</div>			
<div>II NOT TO REPRODUCE OR COPY IT</div>			
<div>III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</div>			
<div>SIZE</div> <div>D</div>	<div>DRAWING NUMBER</div> <div>051-7546</div>	<div>REV.</div> <div>A.0.0</div>	
<div>SCALE</div> <div>NONE</div>	<div>SHT</div> <div>26</div>	<div>OF</div> <div>96</div>	

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
NO_VREFMRGN

DAC channel
Min DAC code
Max DAC code
Max sink I
Max source I
Nominal Vref
Min Vref
Max Vref
Vref Stepping
(per DAC LSB)

MEM A VREF DQ
A
0x00
0x87
-3.75 mA
5 mA
0.75 V
0.375 V
1.250 V
6.5 mV

MEM A VREF CA
B
0x00
0x87
-3.75 mA
5 mA
0.75 V
0.375 V
1.250 V
6.5 mV

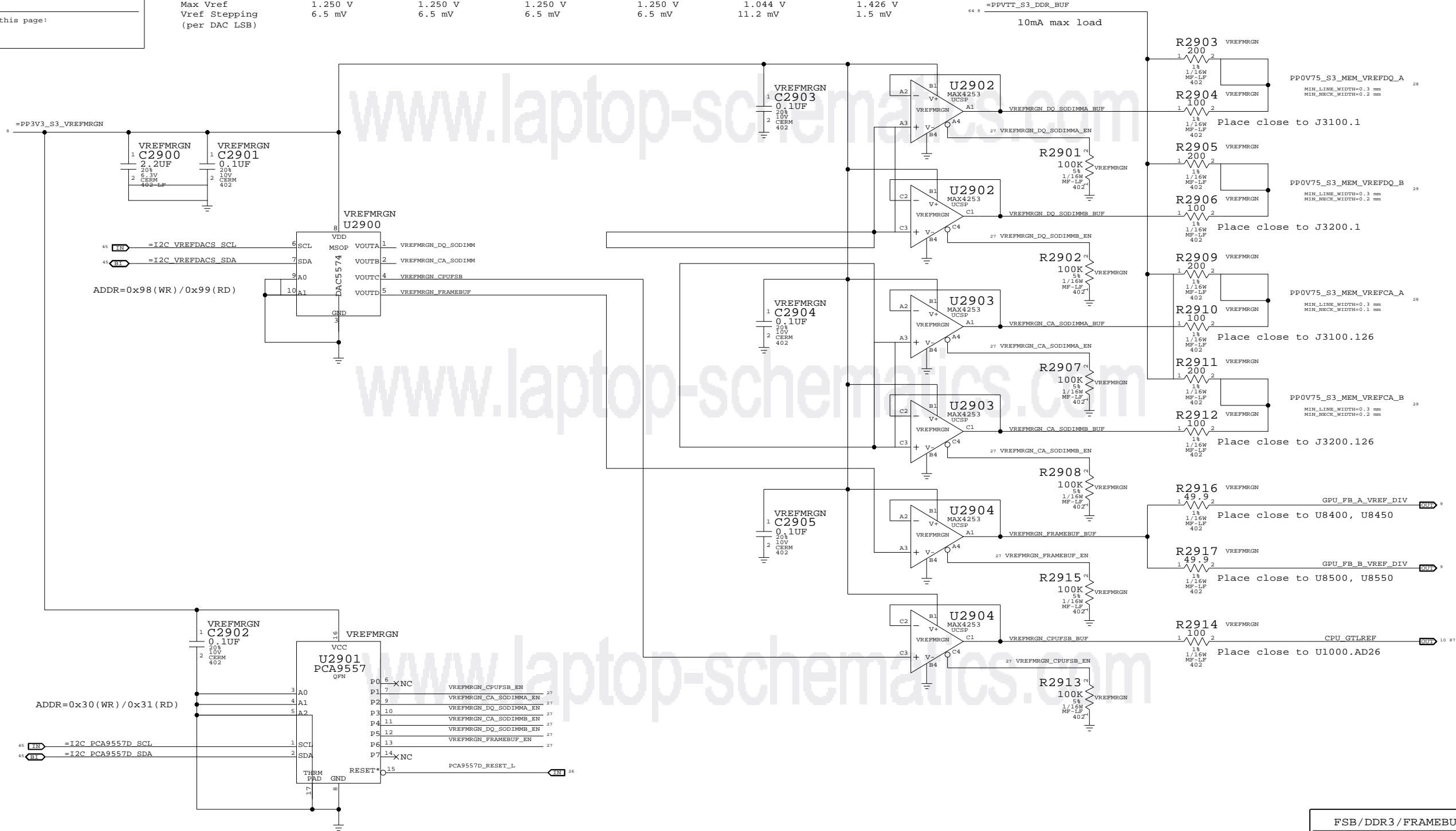
MEM B VREF DQ
A
0x00
0x87
-3.75 mA
5 mA
0.75 V
0.375 V
1.250 V
6.5 mV

MEM B VREF CA
B
0x00
0x87
-3.75 mA
5 mA
0.75 V
0.375 V
1.250 V
6.5 mV

CPU FSB VREF
C
0x00
0x55
-0.91 mA
0.52 mA
0.70 V
0.091 V
1.044 V
11.2 mV

FRAME BUFFER VREF
D
0x00
0xFF
-59.04 mA
51.15 mA
1.248 V
1.042 V
1.426 V
1.5 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately (i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

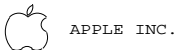
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

FSB/DDR3/FRAMEBUF Vref Margining

SYNC_MASTER=DDR SYNC_DATE=07/22/2008

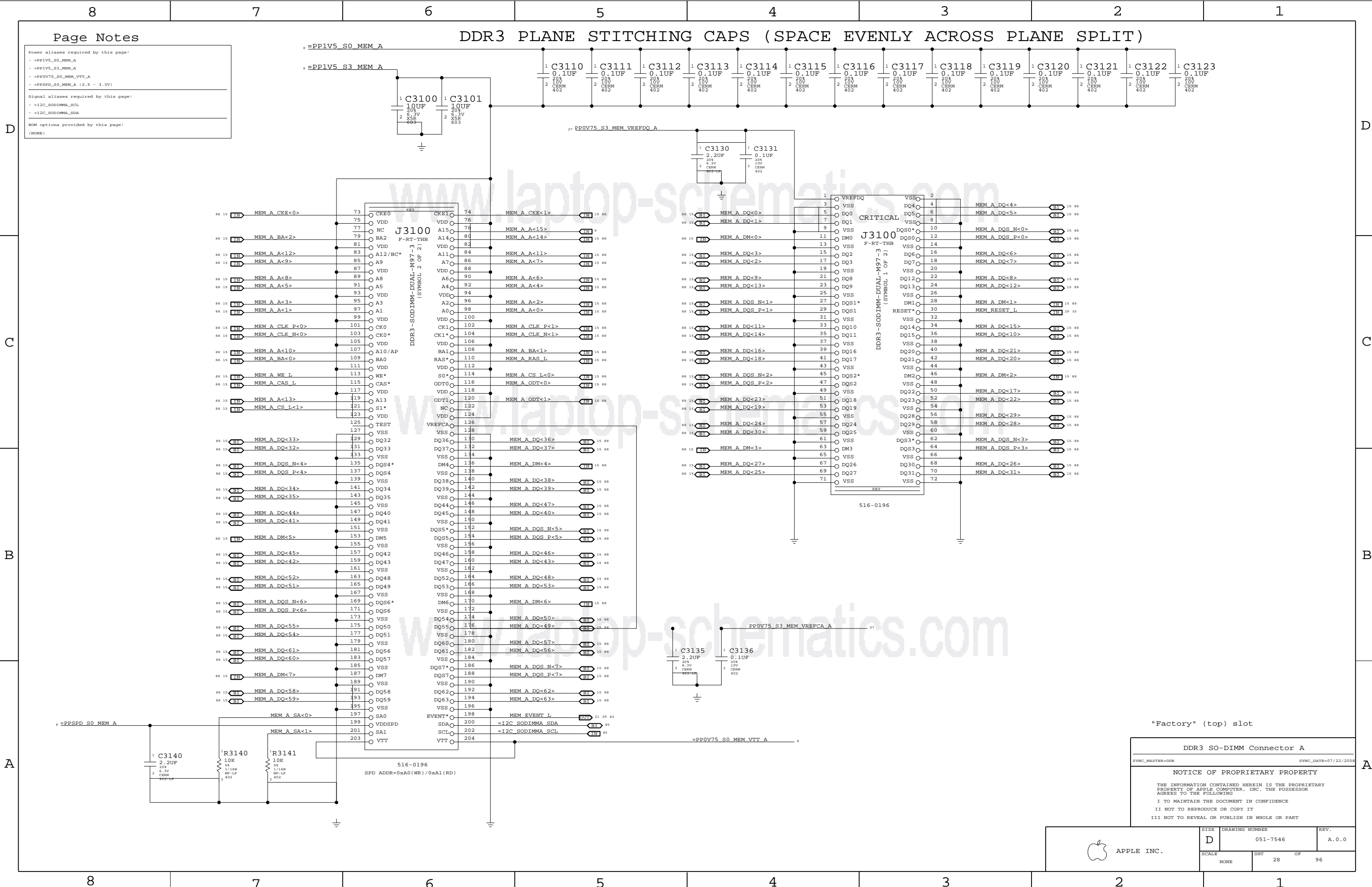
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHT	OF
NONE	27	96



Page Notes

Power aliases required by this page:

- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:

(NONE)

DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)

"Factory" (top) slot

DDR3 SO-DIMM Connector A

SYNC_MASTER=DDR SYNC_DATE=07/22/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

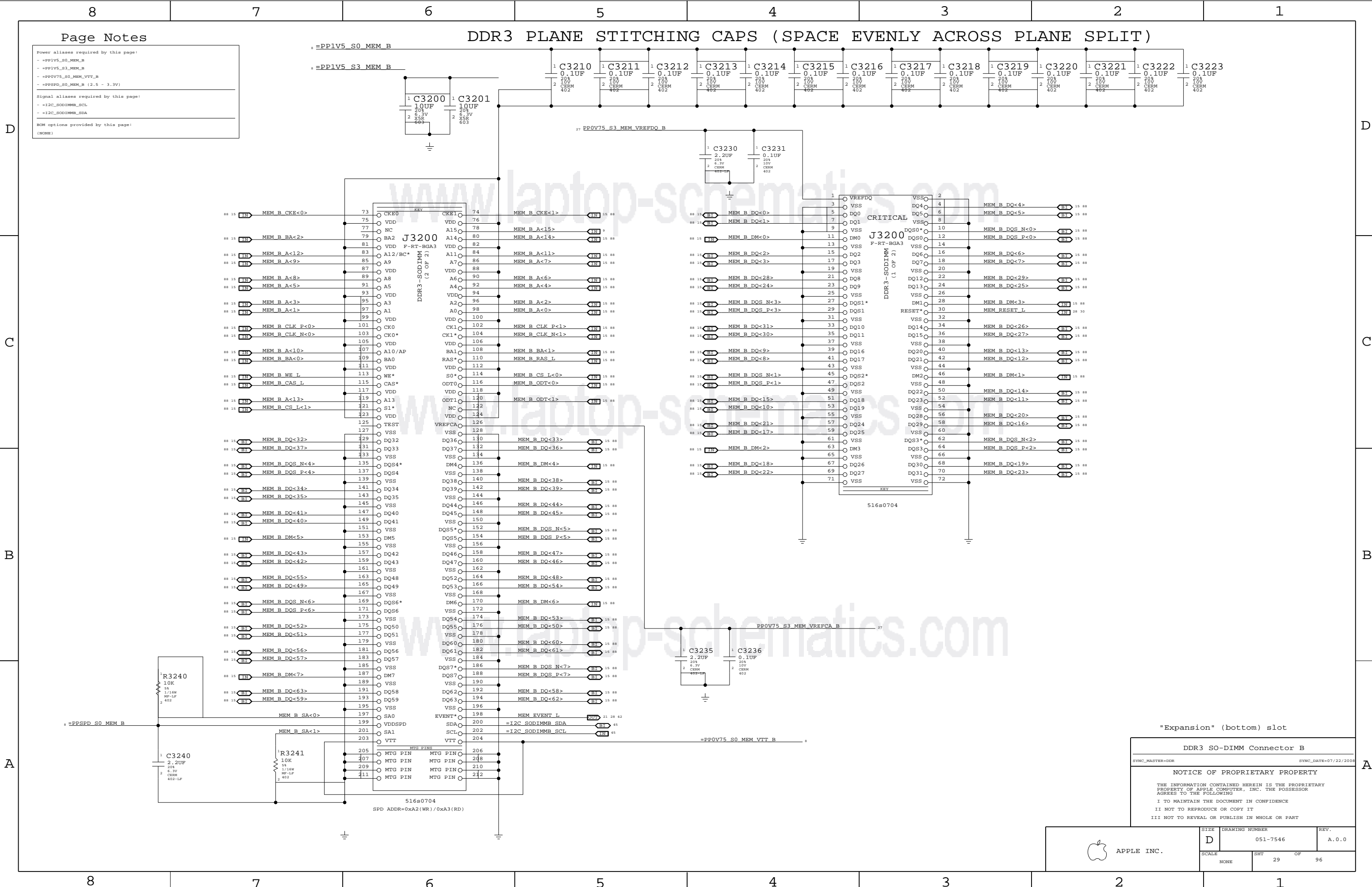
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE D DRAWING NUMBER 051-7546 REV. A.0.0

SCALE NONE SHT 28 OF 96



Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)

"Expansion" (bottom) slot

DDR3 SO-DIMM Connector B

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



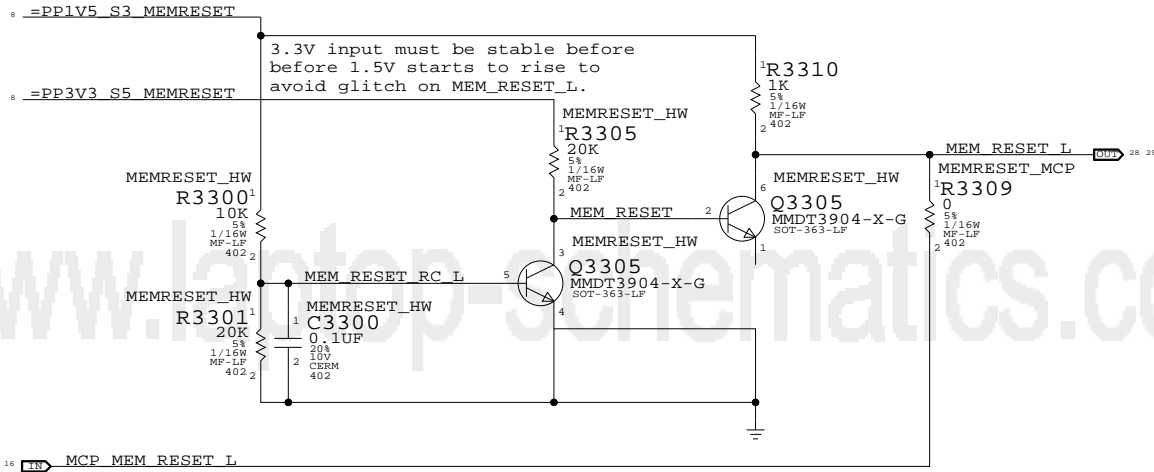
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHT	OF
NONE	29	96

www.laptop-schematics.com

DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



DDR3 Support

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

NOTICE OF PROPRIETARY PROPERTY

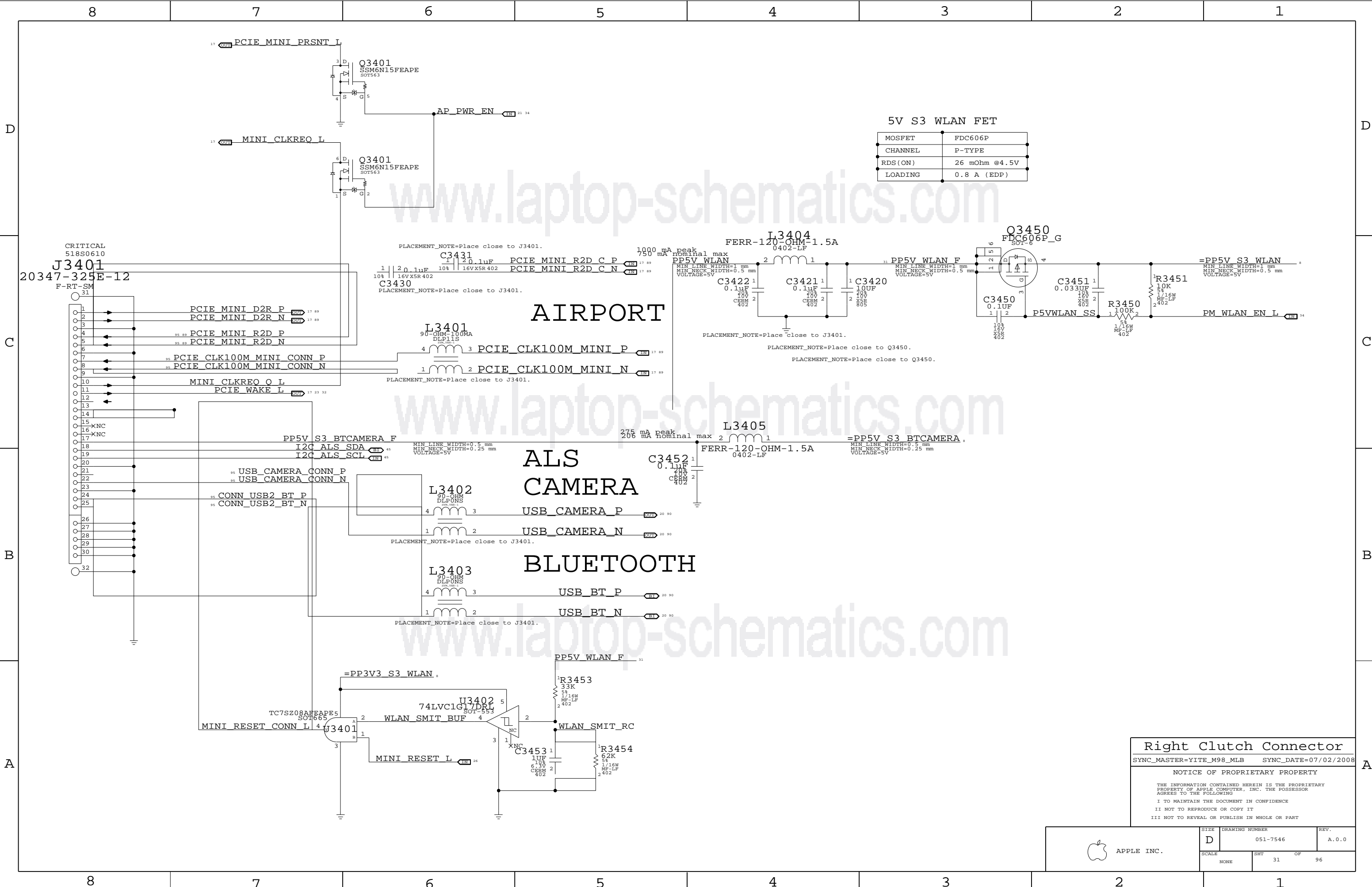
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE		SHT	OF
NONE		30	96



5V S3 WLAN FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	0.8 A (EDP)

Right Clutch Connector

SYNC_MASTER=YITE_M98_MLB SYNC_DATE=07/02/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

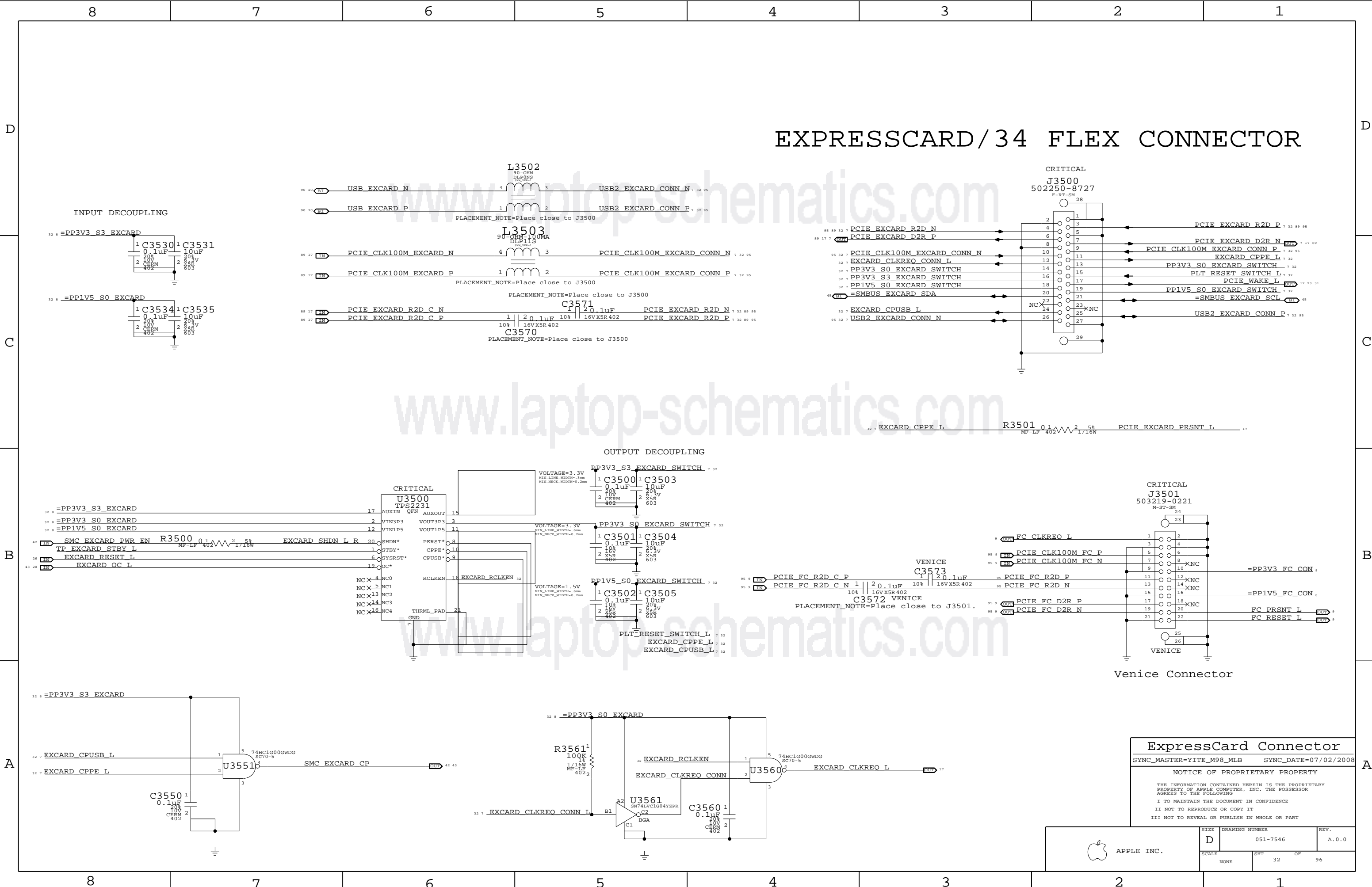
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE D DRAWING NUMBER 051-7546 REV. A.0.0

SCALE NONE SHT 31 OF 96



EXPRESSCARD/34 FLEX CONNECTOR

ExpressCard Connector

SYNC_MASTER=YITE_M98_MLB SYNC_DATE=07/02/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE

D

DRAWING NUMBER

051-7546

REV.

A.0.0

SCALE

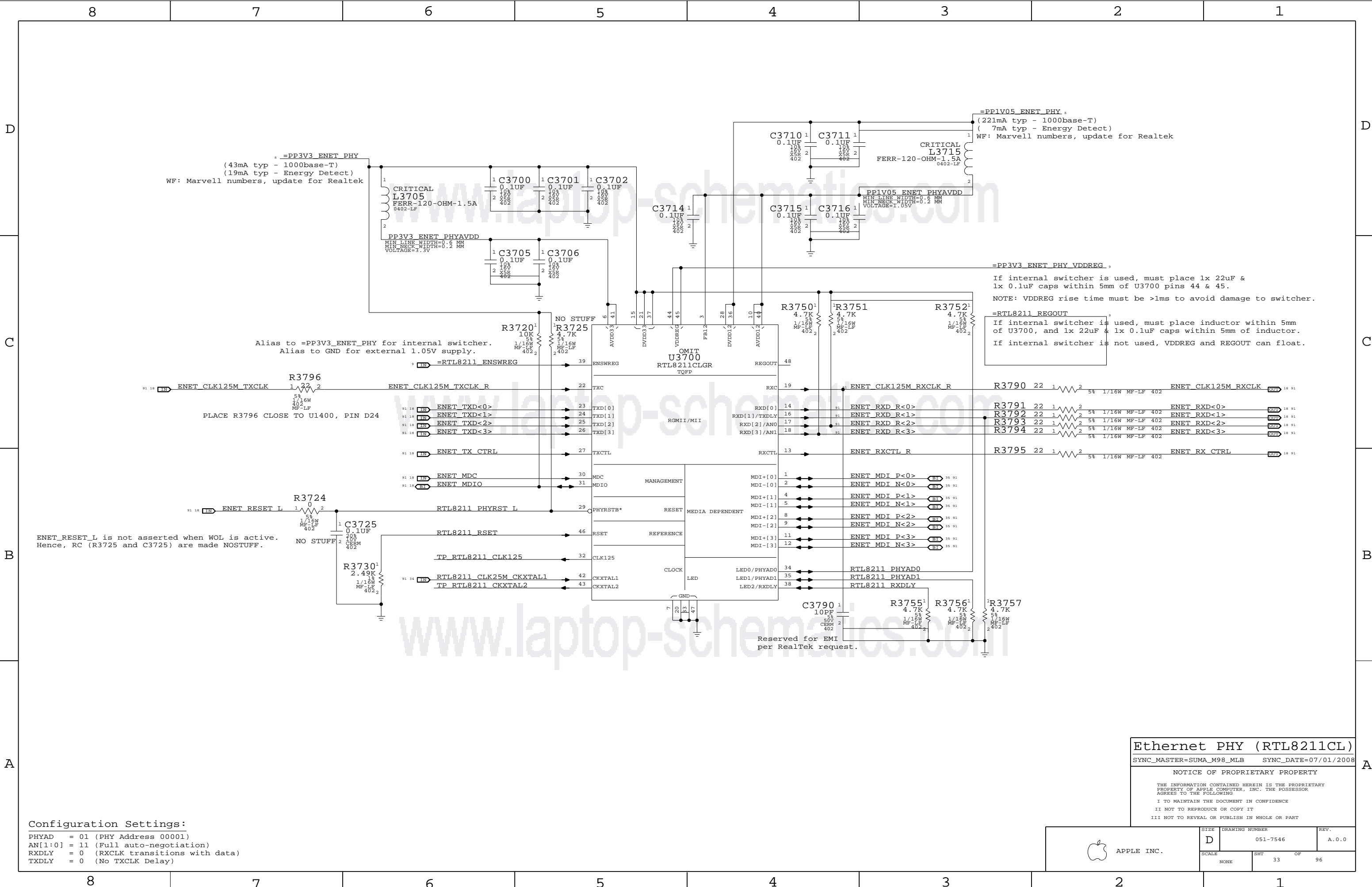
NONE

SHT

32

OF

96



Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

Ethernet PHY (RTL8211CL)

SYNC_MASTER=SUMA_M98_MLB SYNC_DATE=07/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

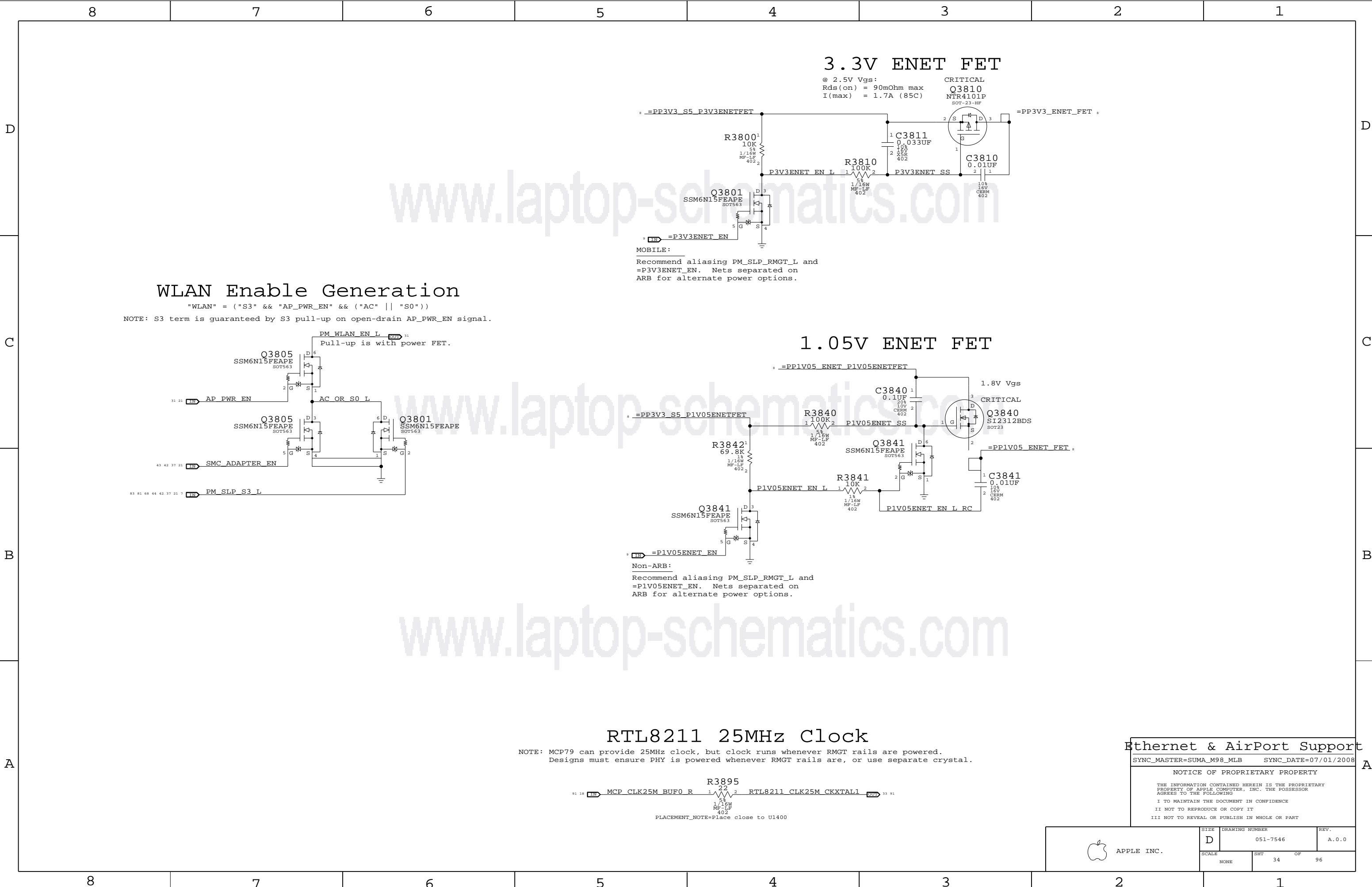
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHT	OF
NONE	33	96

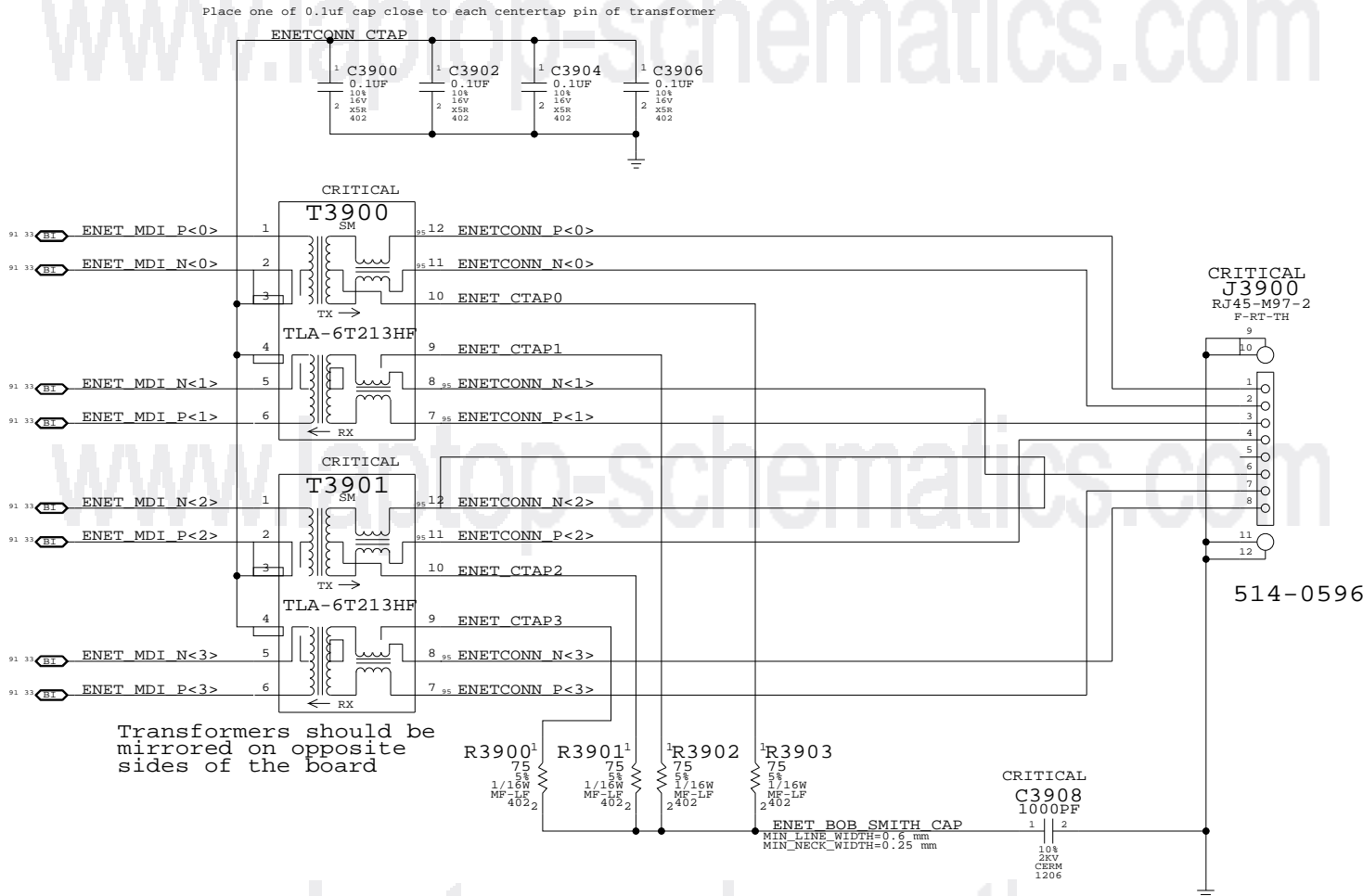


Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Ethernet Connector

SYNC_MASTER=SUMA_M98_MLB SYNC_DATE=07/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE

DRAWING NUMBER

REV.

D

051-7546

A.0.0

SCALE

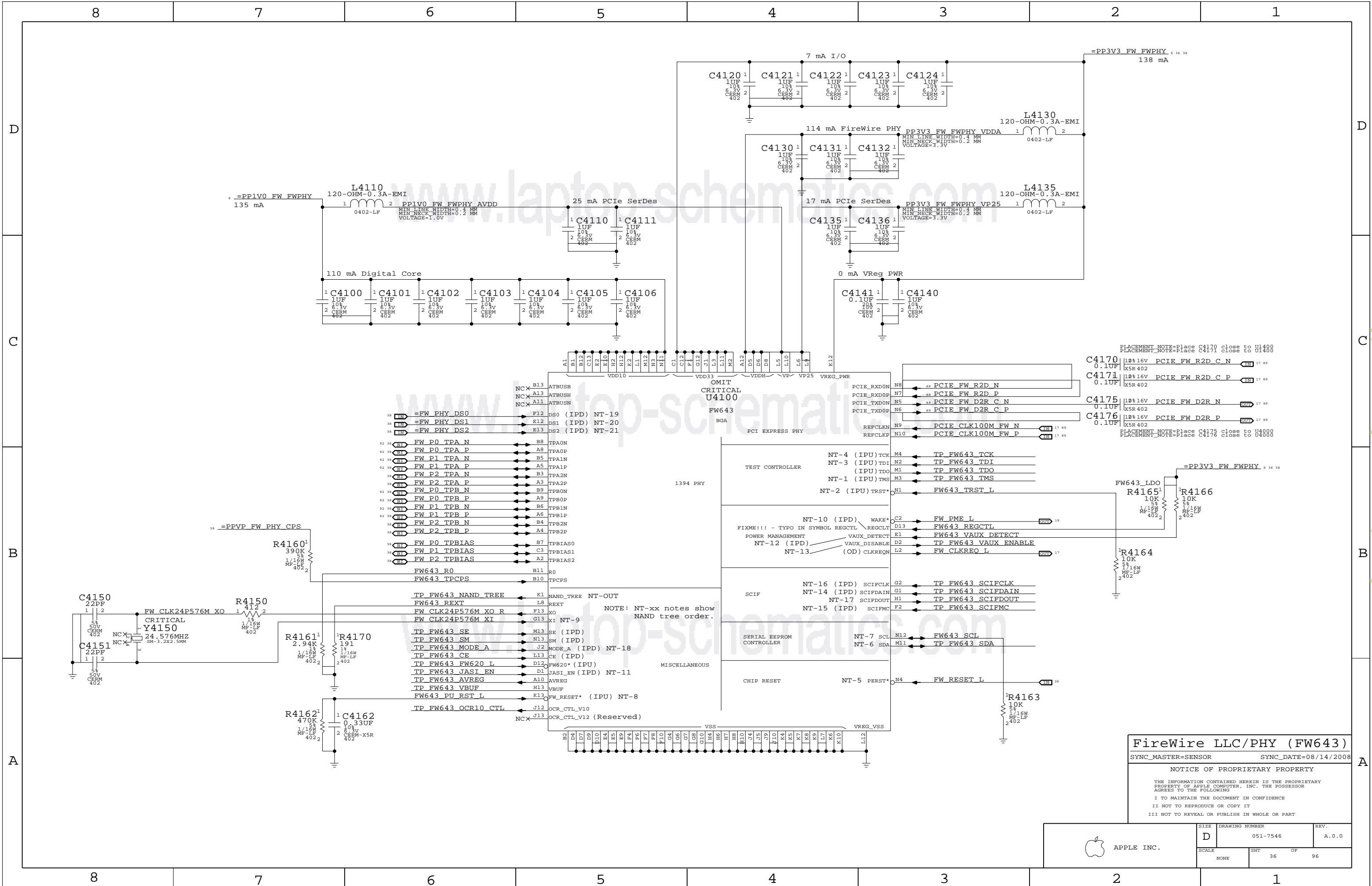
NONE

SHT

35

OF

96



FireWire LLC/PHY (FW643)

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



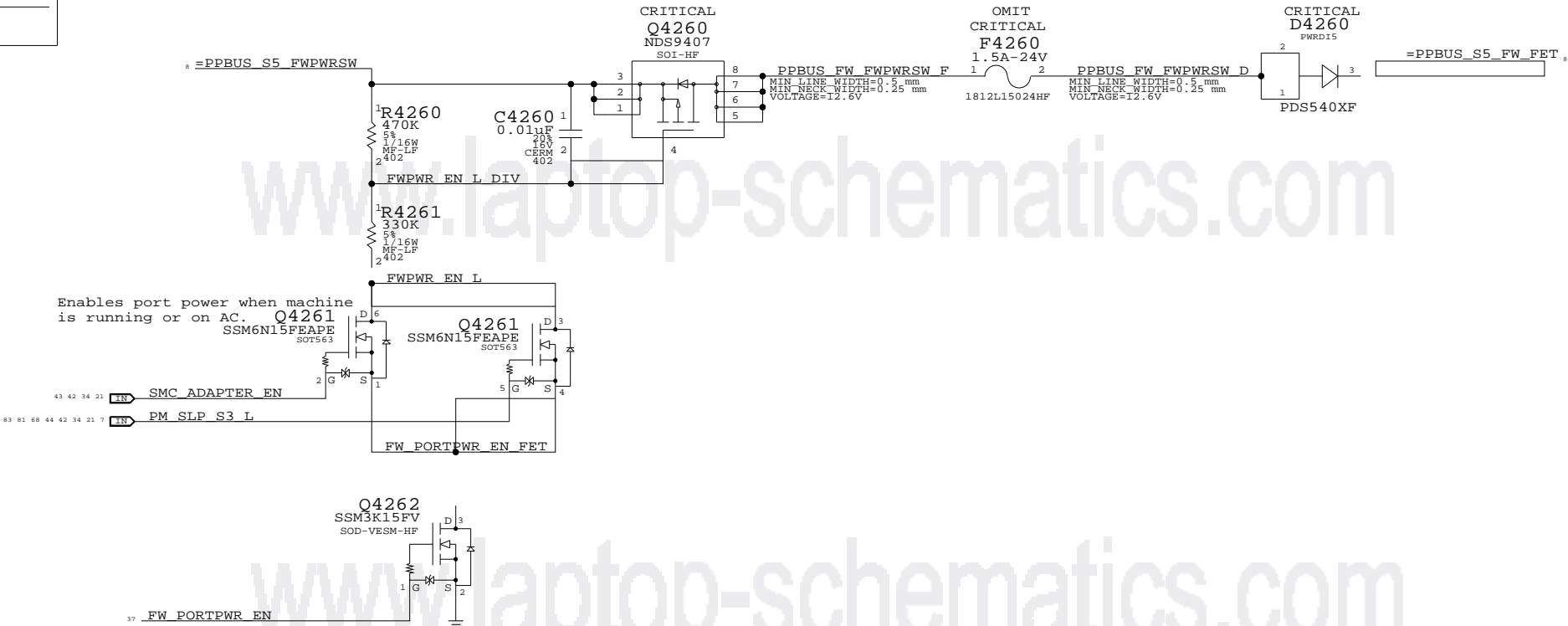
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHT	OF
NONE	36	96

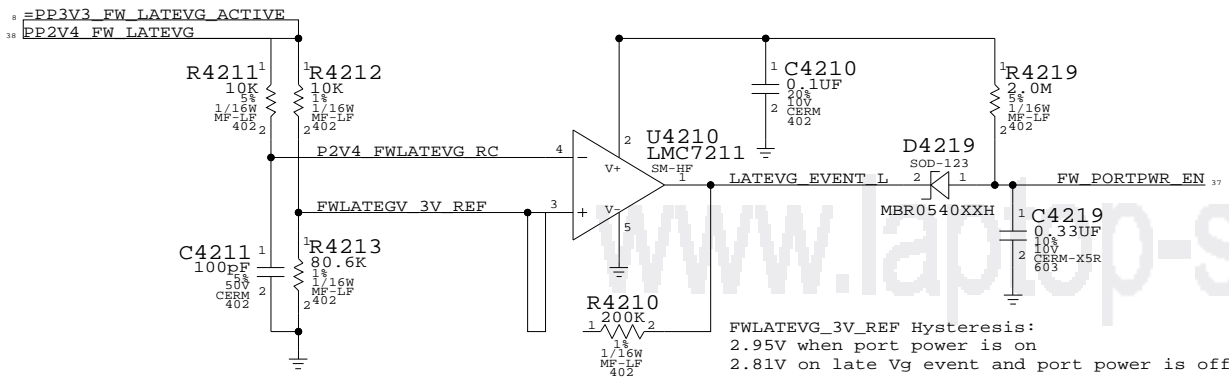
Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
- FW_PORT_FAULT_PU

FireWire Port Power Switch



Late-VG Event Detection



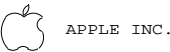
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
740S0080	1	LITTLEFUSE, 1.5A RESETTABLE 24V	F4260	CRITICAL	

FireWire Port Power

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

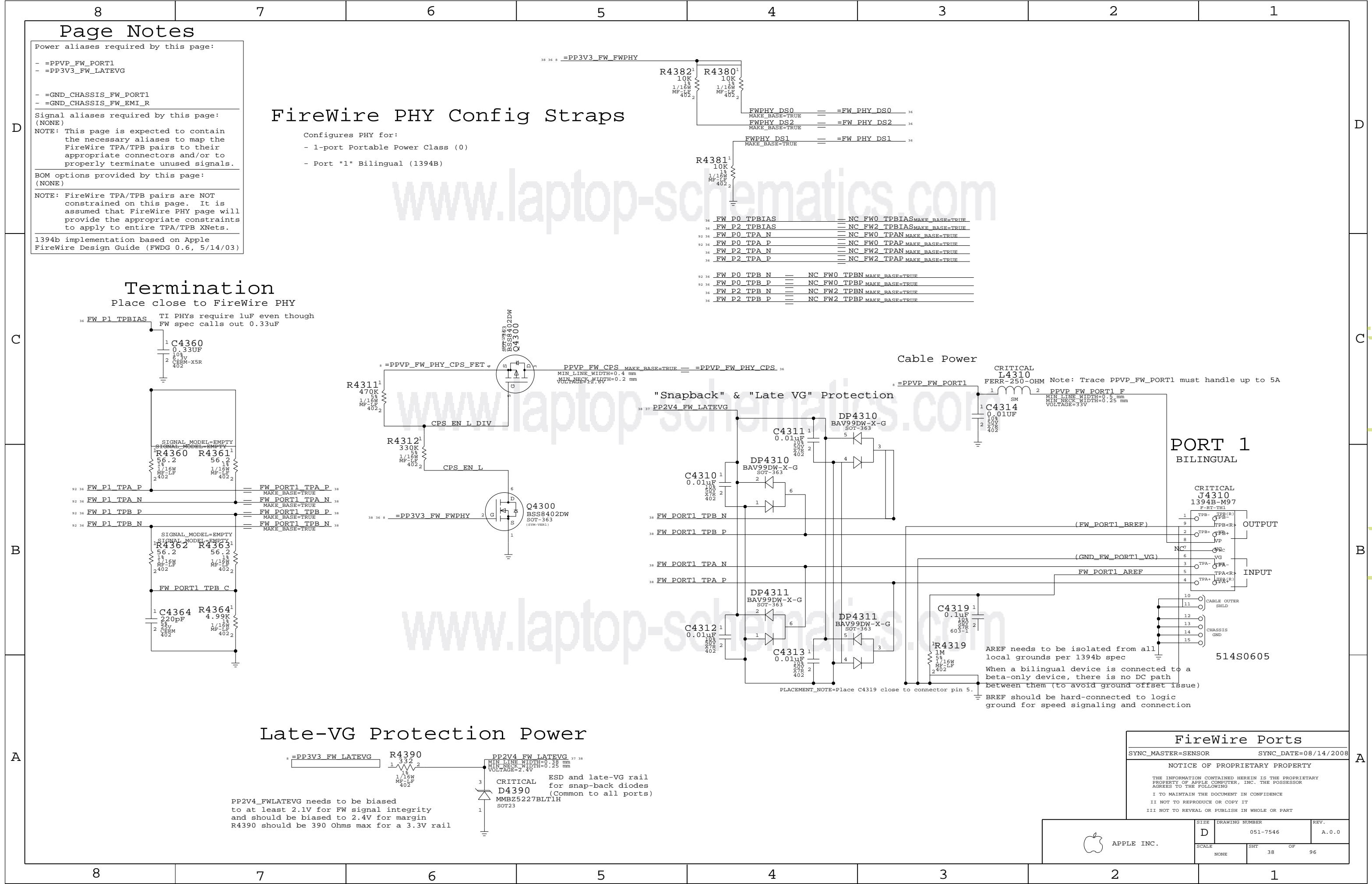
NOTICE OF PROPRIETARY PROPERTY

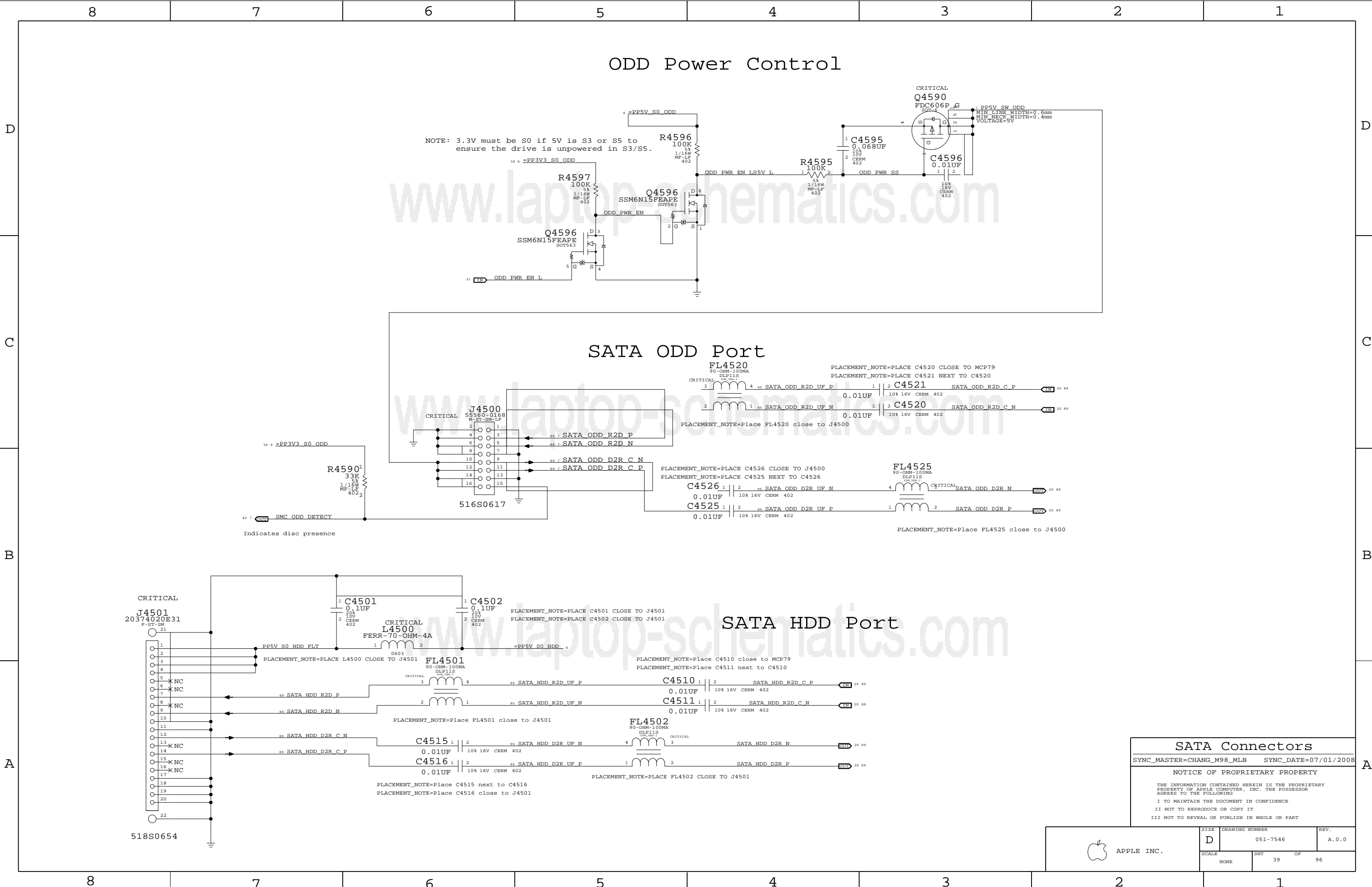
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



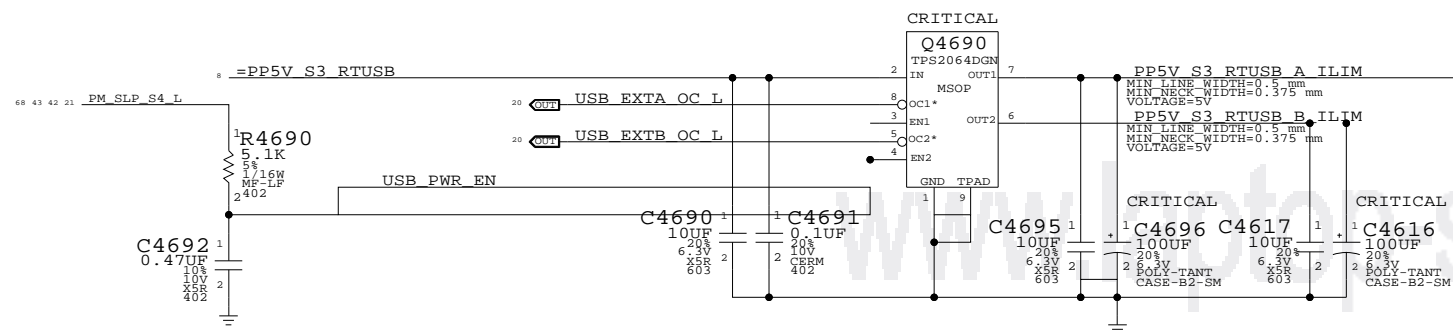
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHT	OF
NONE	37	96

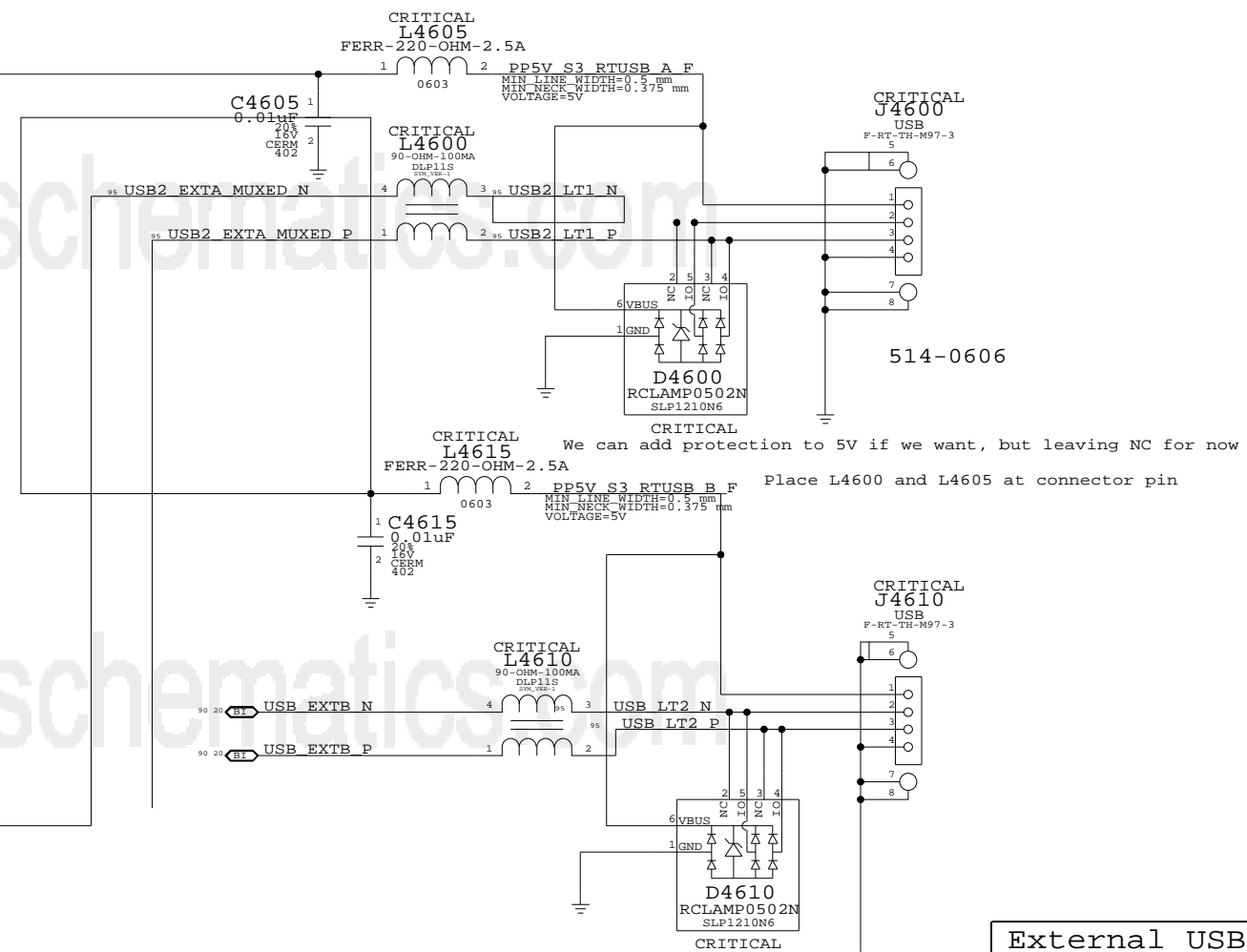




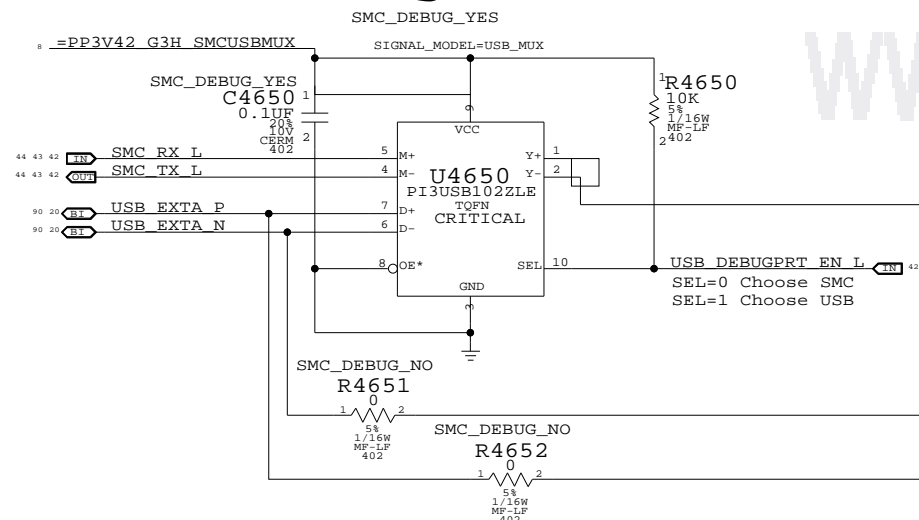
Port Power Switch



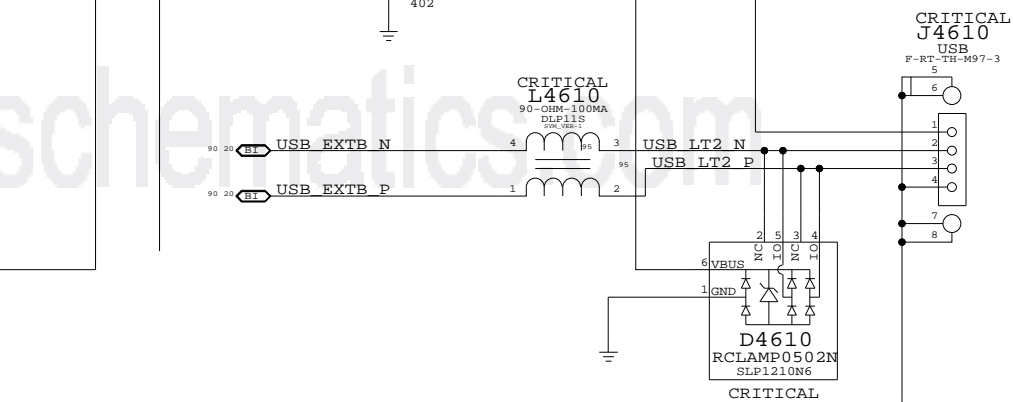
Left USB Port A



USB/SMC Debug Mux



Left USB Port B



External USB Connectors

SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=07/02/2008

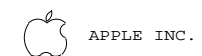
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

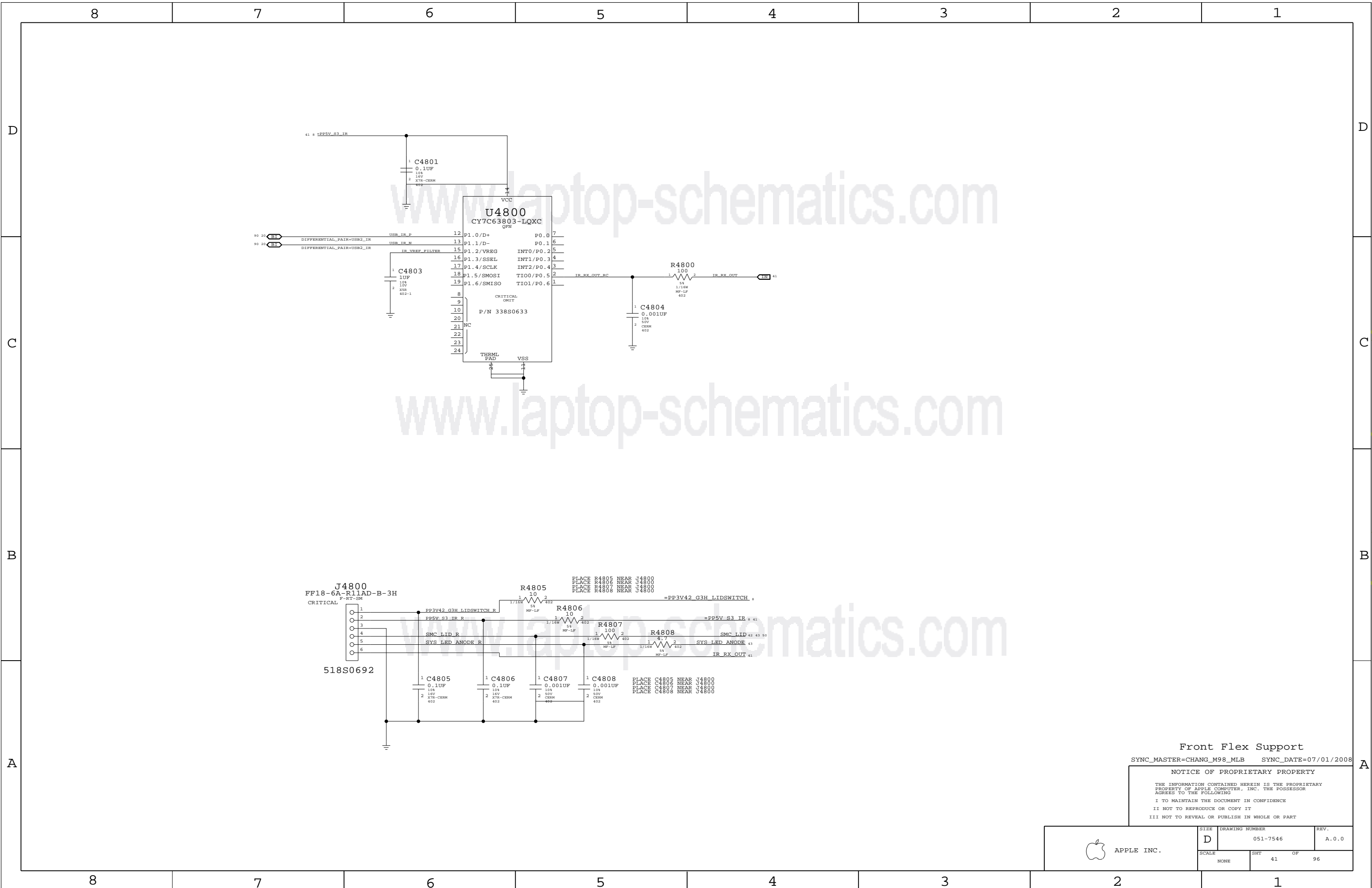
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

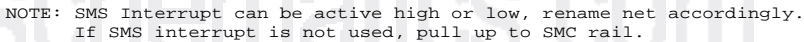


APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHT	OF
NONE	40	96

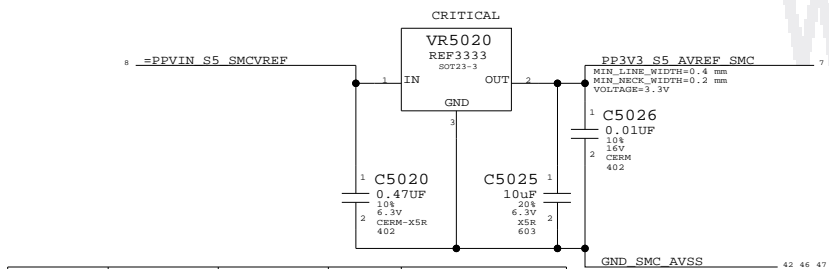
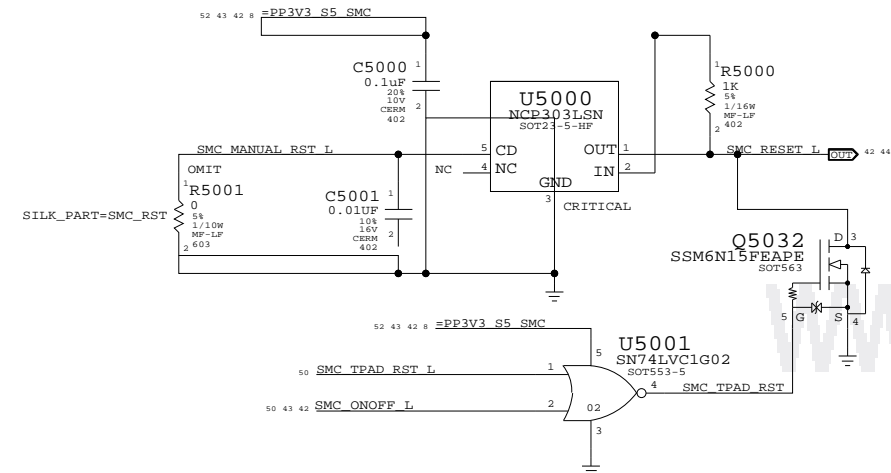


A

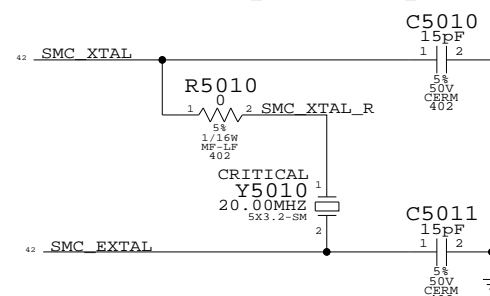


 APPLE INC.	SIZE	DRAWING NUMBER		REV.
	D	051-7546		A.0.0
	SCALE	SHT	OF	
	NONE	42	96	





SMC Crystal Circuit



SMC ONOFF L

42 43 50

OMIT

R5015

5.9k 10W

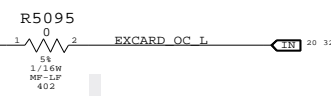
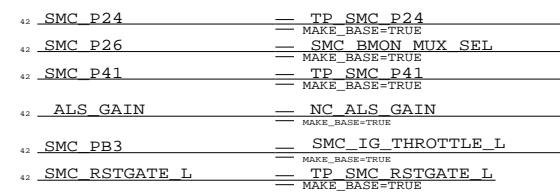
5V

0V

SILK_PART=PWR_BTN

Place R5015, R5001 on bottom side

The schematic diagram illustrates the LED driver circuit for the SMC SYS LED. The circuit is powered by a 5V supply (PP5V_S3_SYSLD). A 1.16W resistor (R5031) is connected to the supply. A 1.47K resistor (R5032) is connected to the supply. The LED is connected to the current source (Q5030) and the resistor. The circuit is powered by a 5V supply and a 1.16W resistor.



TO CPU

87 62 34 10 **NEW** CPU_PROCHOT_L

3.3K R5062

5V

1/2WEN HP-LP 4012

Q5059
SSM6N15FEAPE
SOT563

6 D 1 S 2 G

SMC_PROCHOT **NEW**

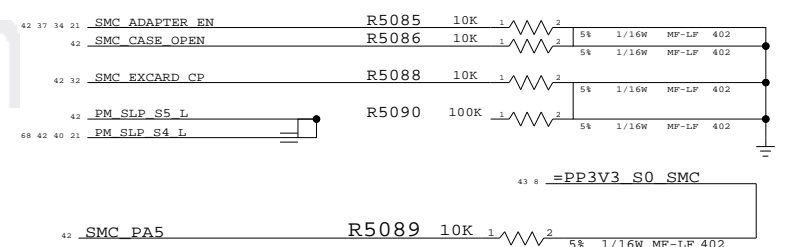
87 14 10 **NEW** PM_THERMTRIP_L


3 D 4 S 5 G

Q5059
SSM6N15FEAPE
SOT563

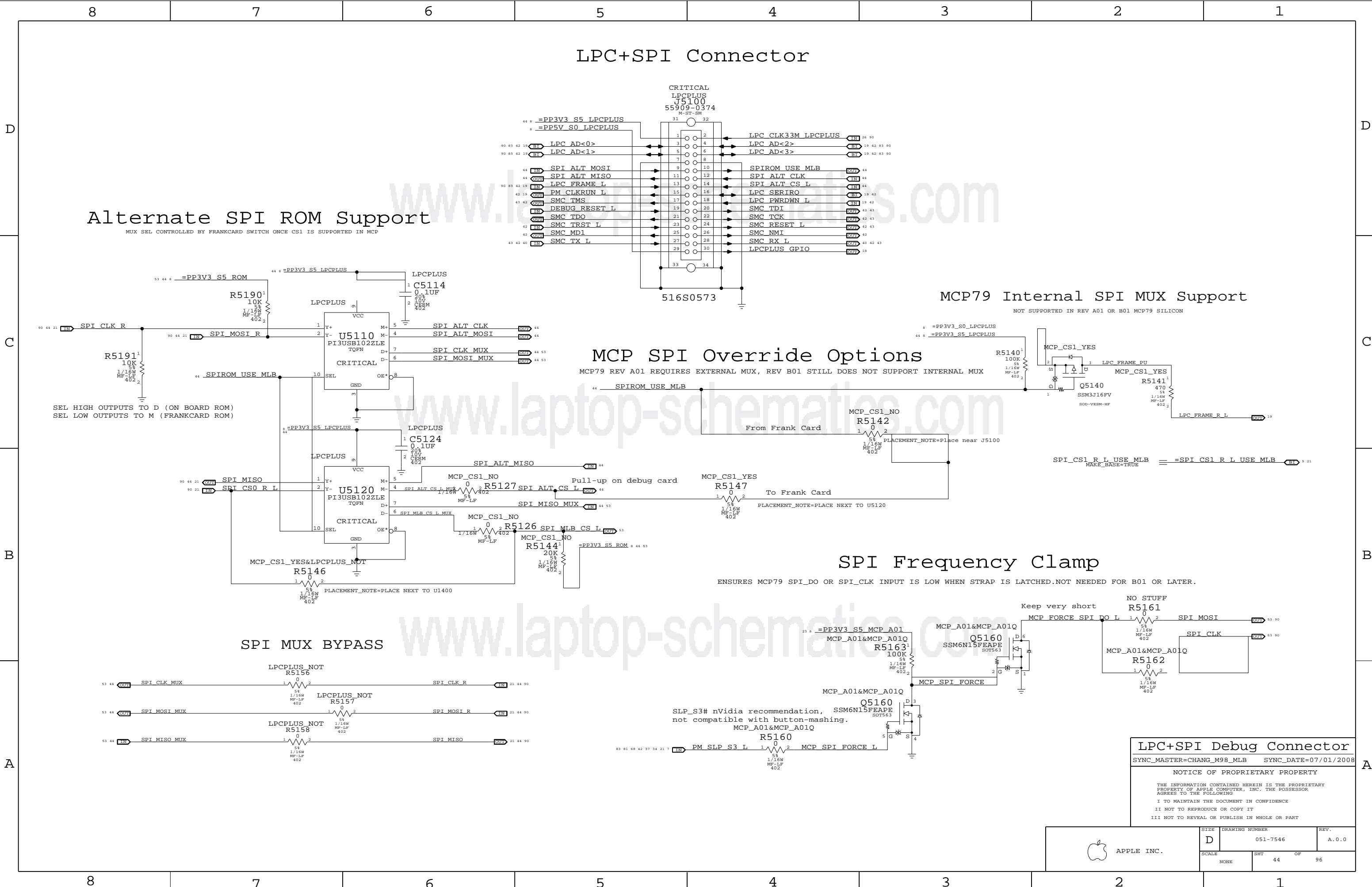
SMC_THRMTRIP **NEW**

42	SMC_PA0	R5091	100K	1	2	5%	1/16W	MF-LP	402
42	SMC_PA1	R5092	100K	1	2	5%	1/16W	MF-LP	402
50 43 42	SMC_ONOFF_L	R5070	10K	1	2	5%	1/16W	MF-LP	402
50 42	SMC_L1D	R5071	100K	1	2	5%	1/16W	MF-LP	402
42	SMC_PH2	R5072	10K	1	2	5%	1/16W	MF-LP	402
44 42 40	SMC_TX_L	R5073	10K	1	2	5%	1/16W	MF-LP	402
44 42 40	SMC_RX_L	R5074	100K	1	2	5%	1/16W	MF-LP	402
ONEWIRE_PU									
60 42	SYS_ONEWIRE	R5075	2.0K	1	2	5%	1/16W	MF-LP	402
42	SMC_BS_ALERT_L	R5076	100K	1	2	5%	1/16W	MF-LP	402
44 42	SMC_TMS	R5077	10K	1	2	5%	1/16W	MF-LP	402
44 42	SMC_TDO	R5078	10K	1	2	5%	1/16W	MF-LP	402
44 42	SMC_TDI	R5079	10K	1	2	5%	1/16W	MF-LP	402
44 42	SMC_TCK	R5080	10K	1	2	5%	1/16W	MF-LP	402
43 42	SMC_BTN_BUTTON_L	R5081	10K	1	2	5%	1/16W	MF-LP	402
60 43 42	SMC_BC_ACLK	R5087	470K	1	2	5%	1/16W	MF-LP	402



 APPLE INC.

SIZE D	DRAWING NUMBER 051-7546	REV. A.0.0
SCALE NONE	SHT 43	OF 96



LPC+SPI Debug Connector

SYNC_MASTER=CHANG_M98_MLB SYNC_DATE=07/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE

D

DRAWING NUMBER

051-7546

REV.

A.0.0

SCALE

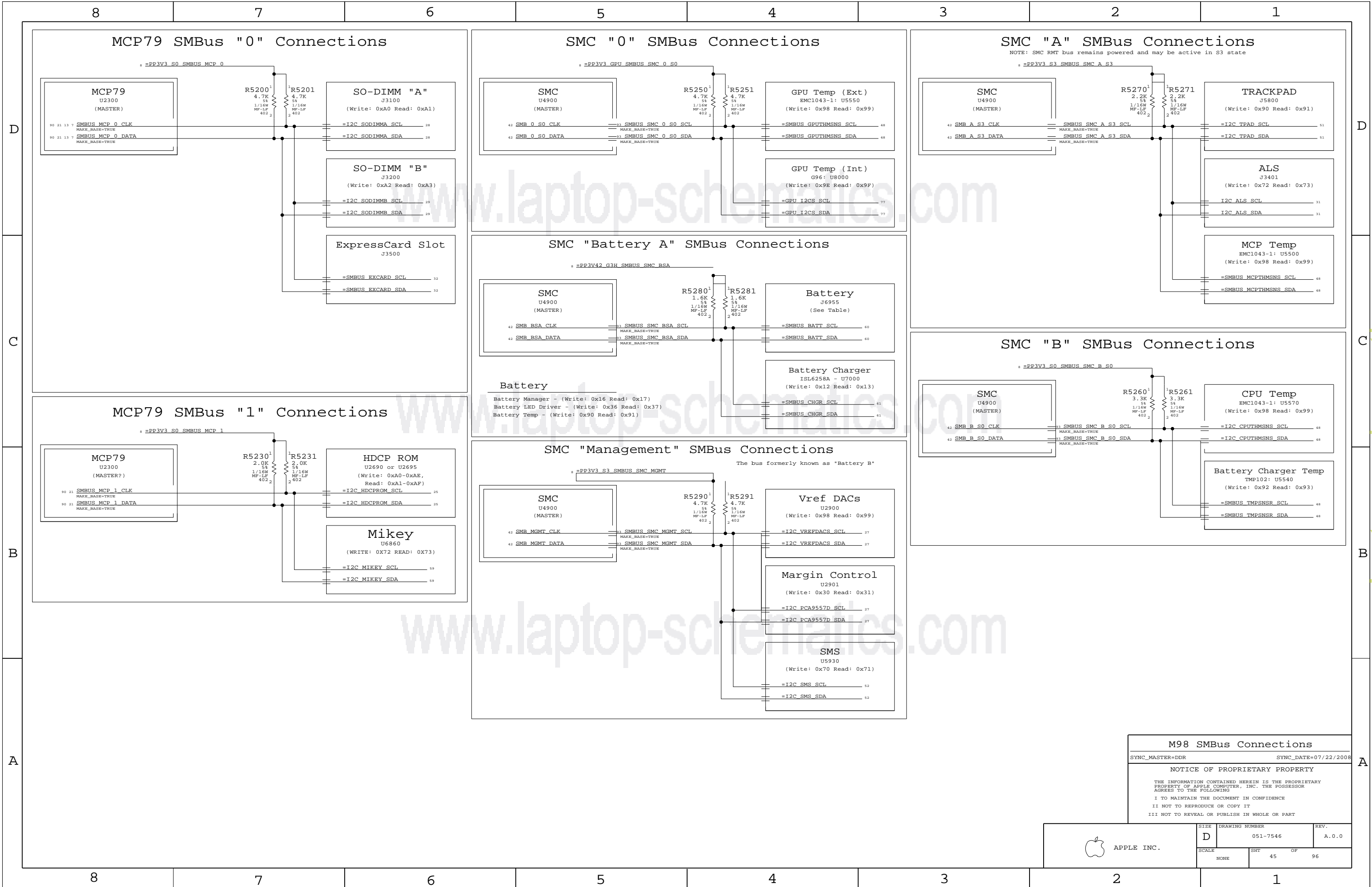
NONE

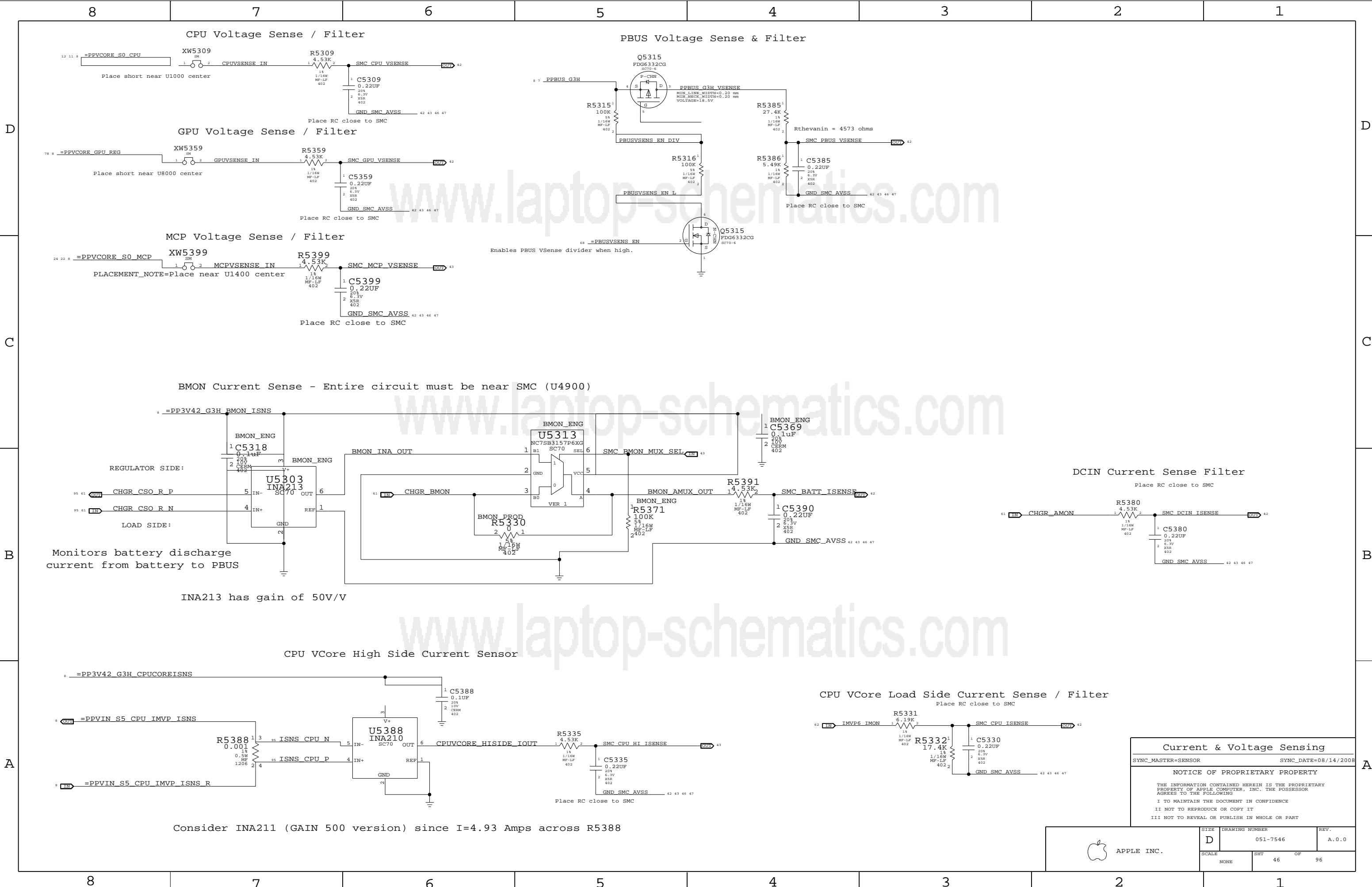
SHT

44

OF

96





D

C

B

A

D

C

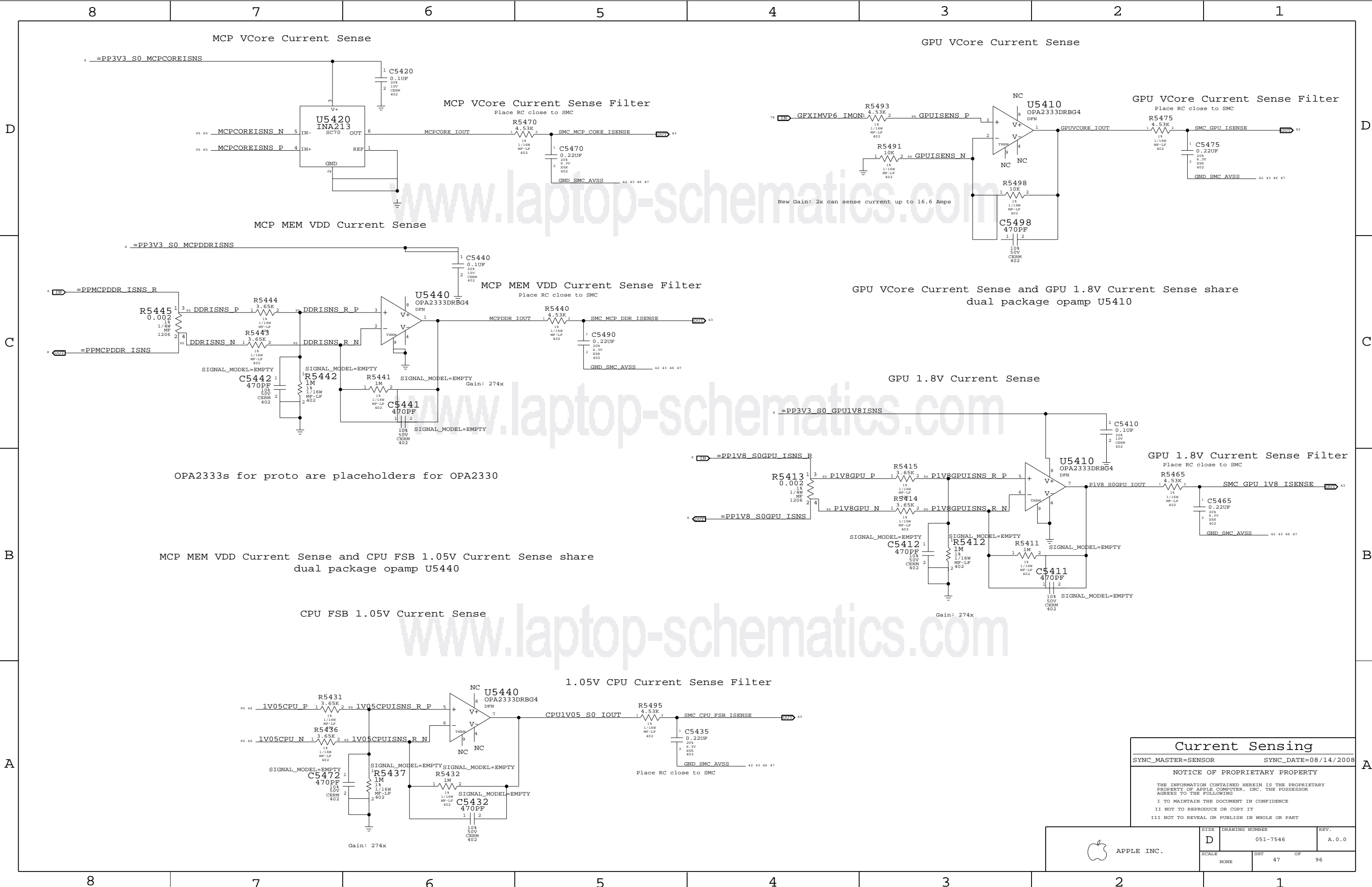
B

A

www.laptop-schematics.com

Current & Voltage Sensing		
SYNC_MASTER=SENSOR		SYNC_DATE=08/14/2008
NOTICE OF PROPRIETARY PROPERTY		
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING		
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE		
II NOT TO REPRODUCE OR COPY IT		
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART		

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE		SHT	OF
NONE		46	96



OPA2333s for proto are placeholders for OPA2330

MCP MEM VDD Current Sense and CPU FSB 1.05V Current Sense share dual package opamp U5440

CPU FSB 1.05V Current Sense

1.05V CPU Current Sense Filter

GPU VCore Current Sense

GPU VCore Current Sense Filter

GPU VCore Current Sense and GPU 1.8V Current Sense share dual package opamp U5410

GPU 1.8V Current Sense

GPU 1.8V Current Sense Filter

Current Sensing

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE

DRAWING NUMBER

REV.

D

051-7546

A.0.0

SCALE

SHT

OF

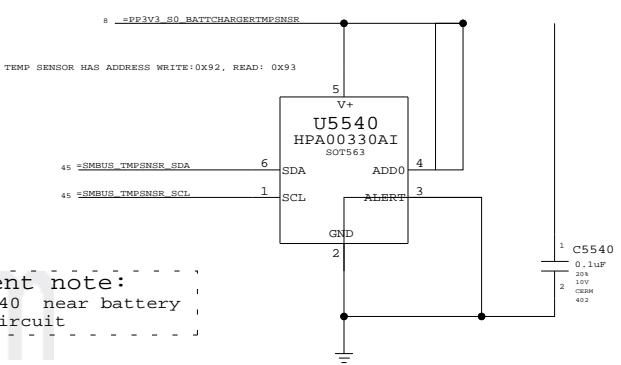
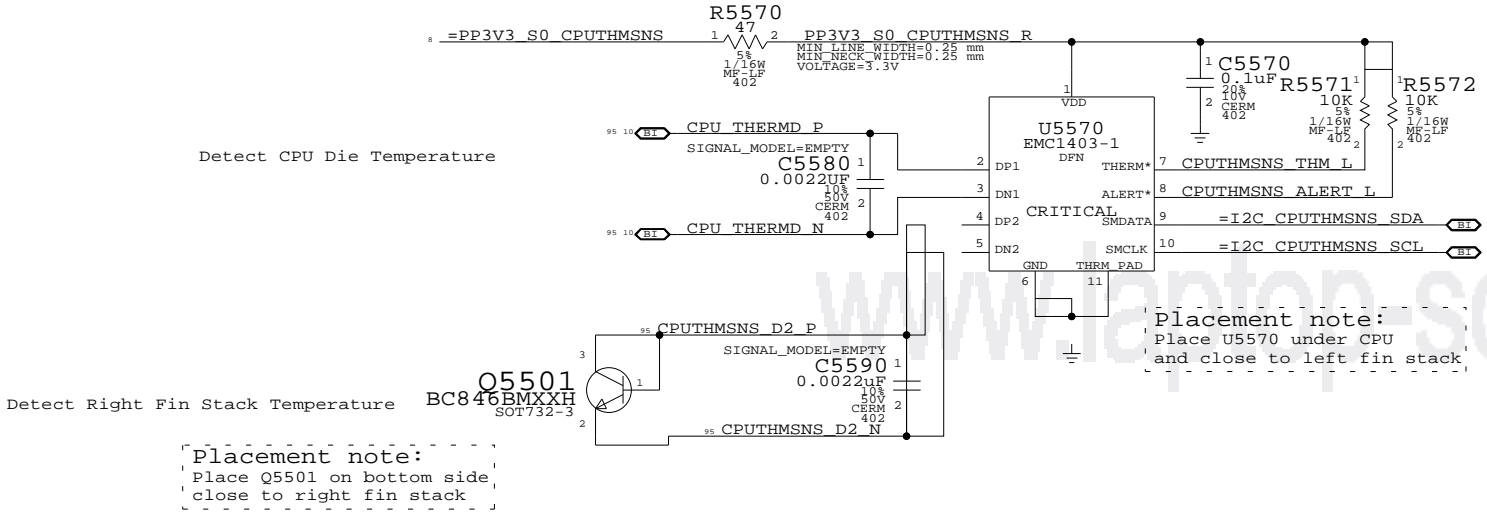
96

CPU Proximity/CPU Die/Right Fin Stack

Battery Charger Proximity

D

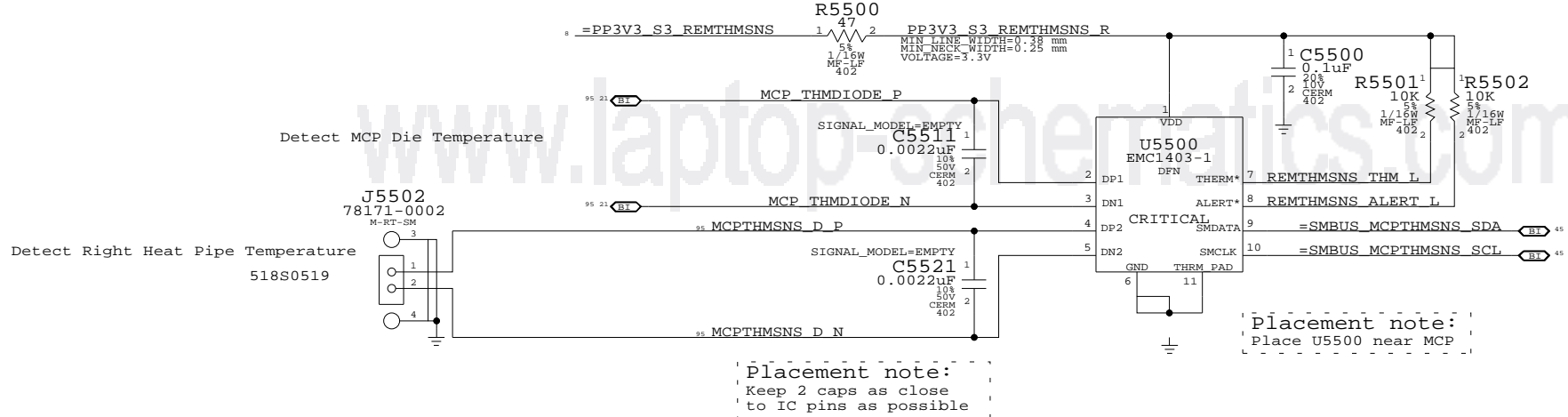
D



MCP Proximity/MCP Die/Right Heat Pipe

C

C

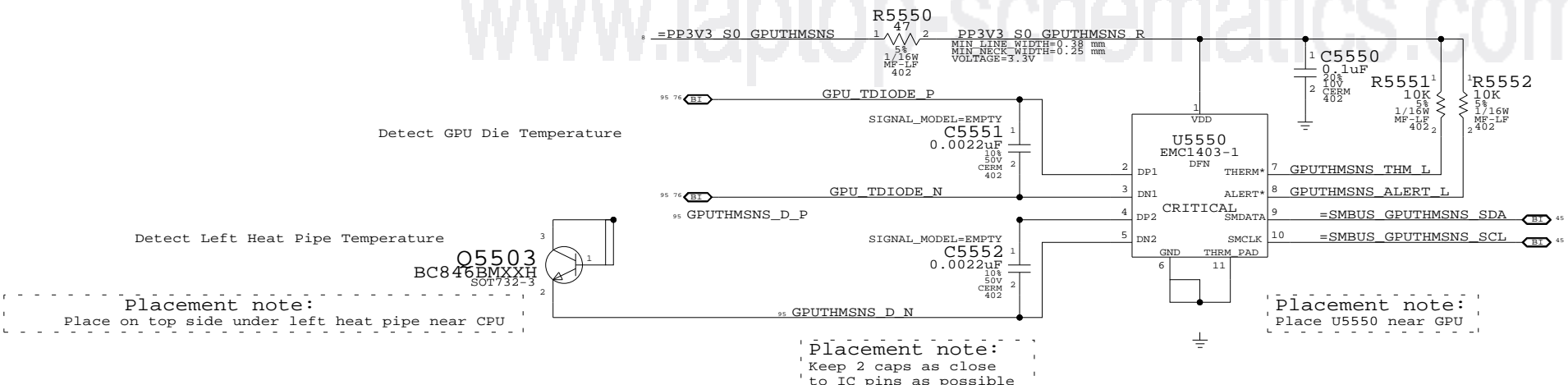


Note: EMC1403 can perform Beta Compensation for External Diode 1 only

GPU Proximity/GPU Die/Left Heat Pipe

B

B

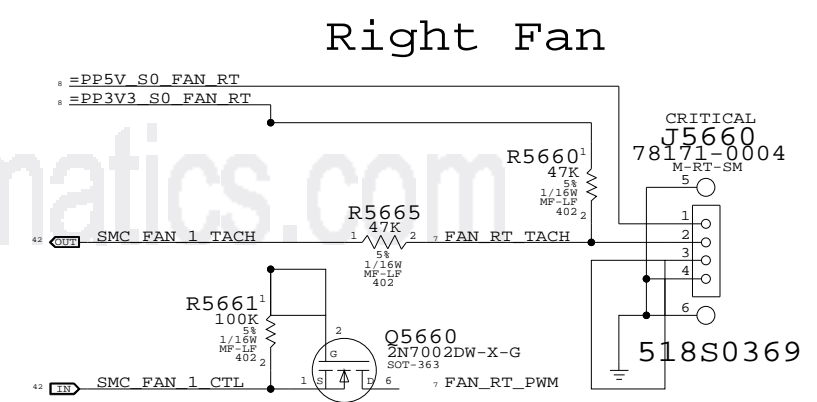
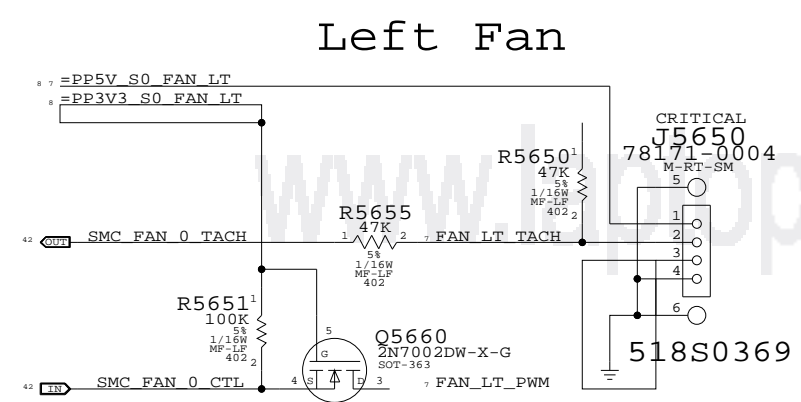


Thermal Sensors	
SYNC_MASTER=SENSOR	SYNC_DATE=08/14/2008
NOTICE OF PROPRIETARY PROPERTY	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING	
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE	
II NOT TO REPRODUCE OR COPY IT	
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	

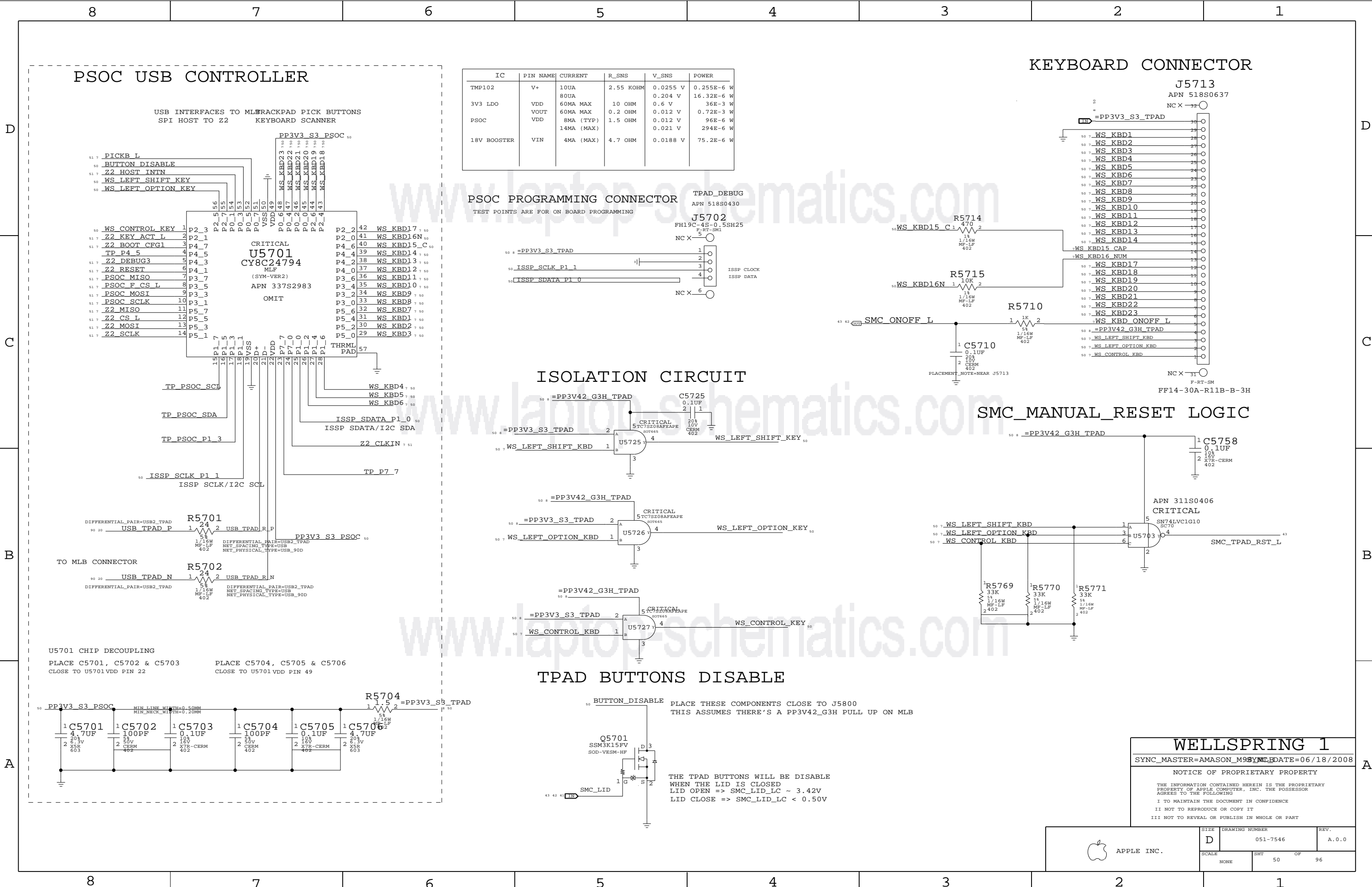
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE		SHT	OF
NONE		48	96

www.laptop-schematics.com

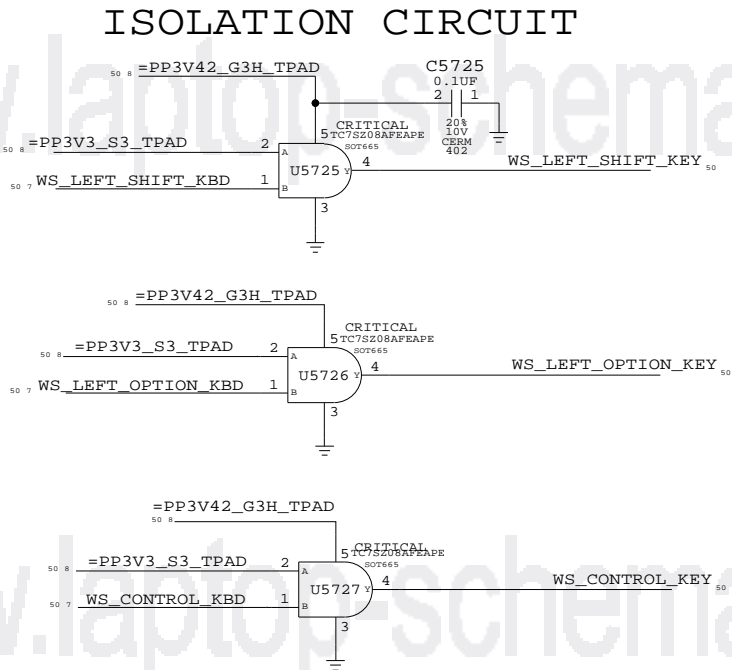
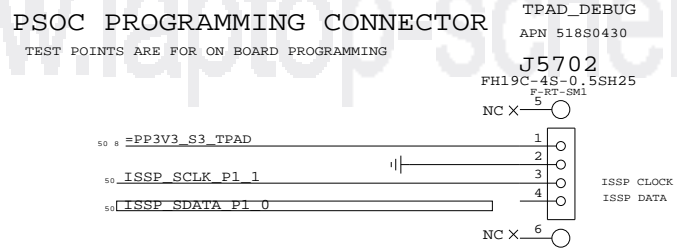
www.laptop-schematics.com



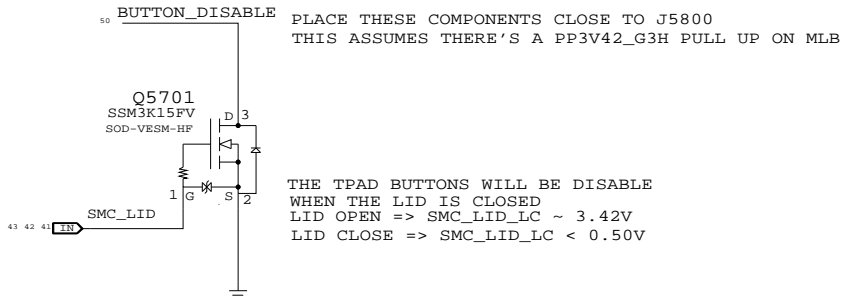
Fan Connectors			
SYNC_MASTER=M87_MLB		SYNC_DATE=10/17/2007	
NOTICE OF PROPRIETARY PROPERTY			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING			
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE			
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART			
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	NONE	SHT	49 OF 96



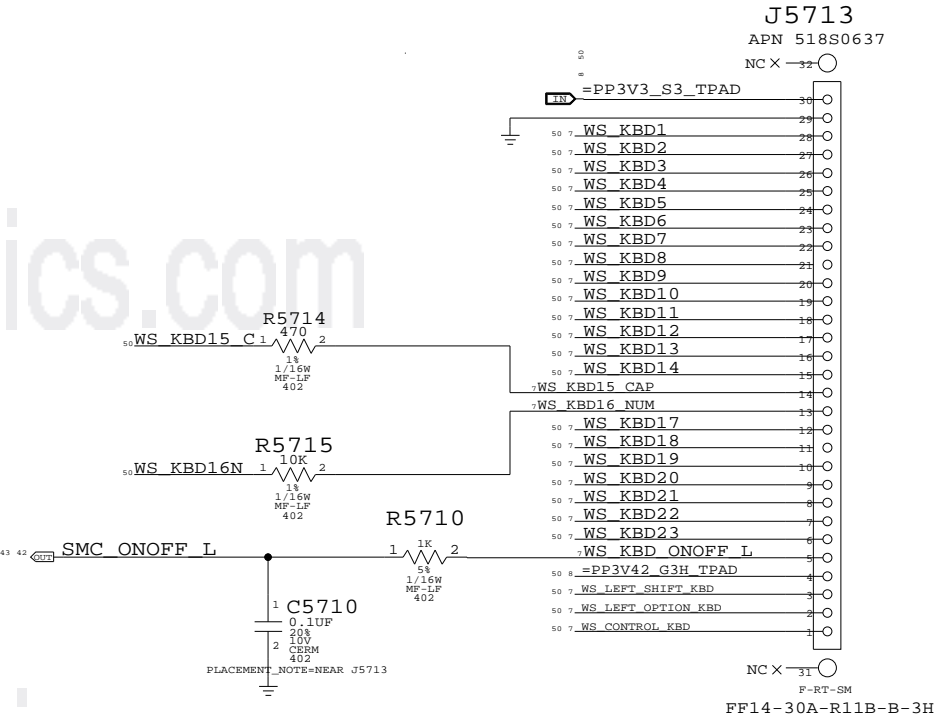
IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	100UA	2.55 KOHM	0.0255 V	0.255E-6 W
3V3 LDO	VDD	80UA	10 OHM	0.204 V	16.32E-6 W
PSOC	VOUT	60MA MAX	0.2 OHM	0.6 V	36E-3 W
	VDD	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
	VDD	14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W



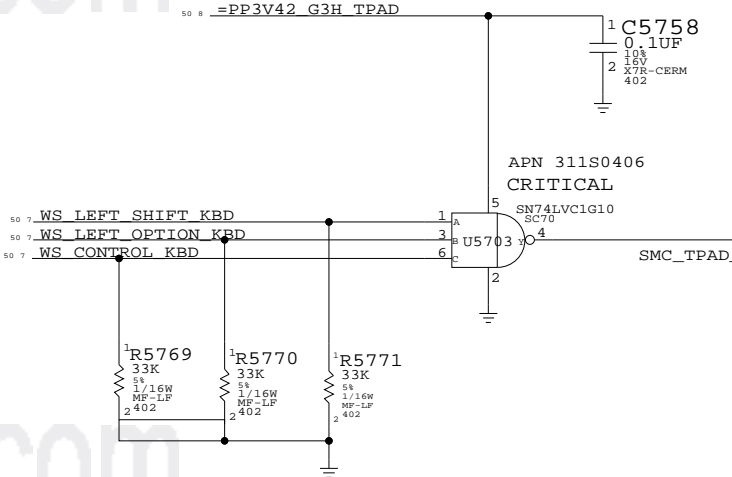
TPAD BUTTONS DISABLE



KEYBOARD CONNECTOR



SMC_MANUAL_RESET LOGIC



WELLSPRING 1

SYNC_MASTER=AMASON_M9SYNCLDATE=06/18/2008

NOTICE OF PROPRIETARY PROPERTY

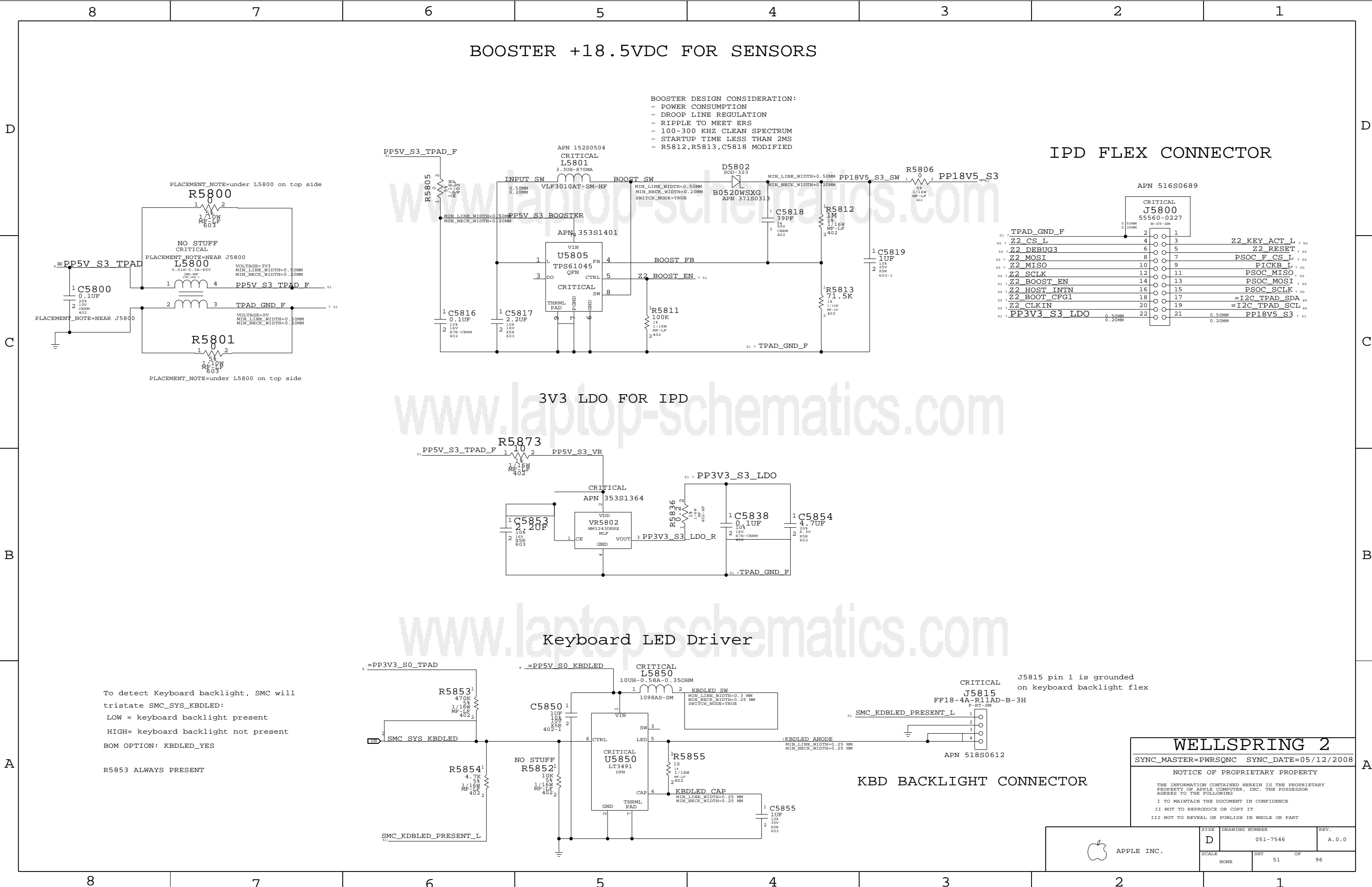
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

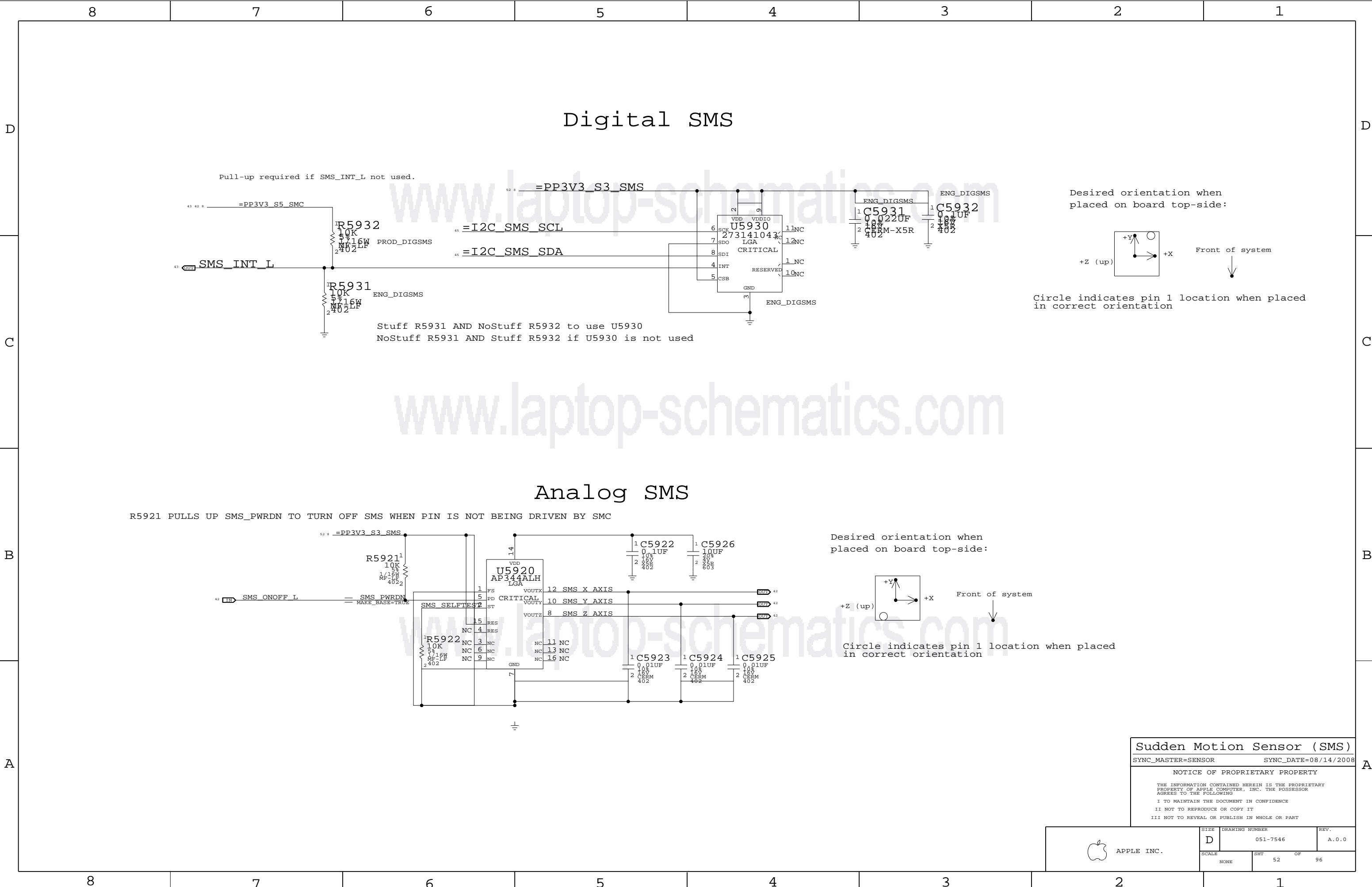
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

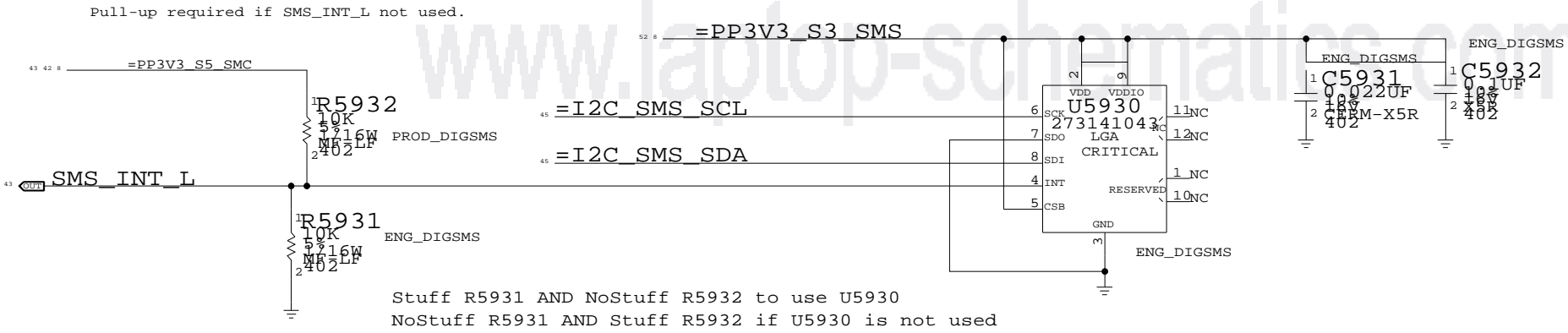
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	D	DRAWING NUMBER	051-7546	REV.	A.0.0
	SCALE	NONE	SHT	50	OF	96

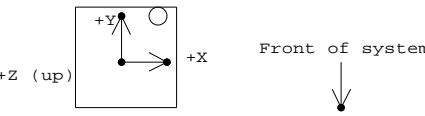




Digital SMS



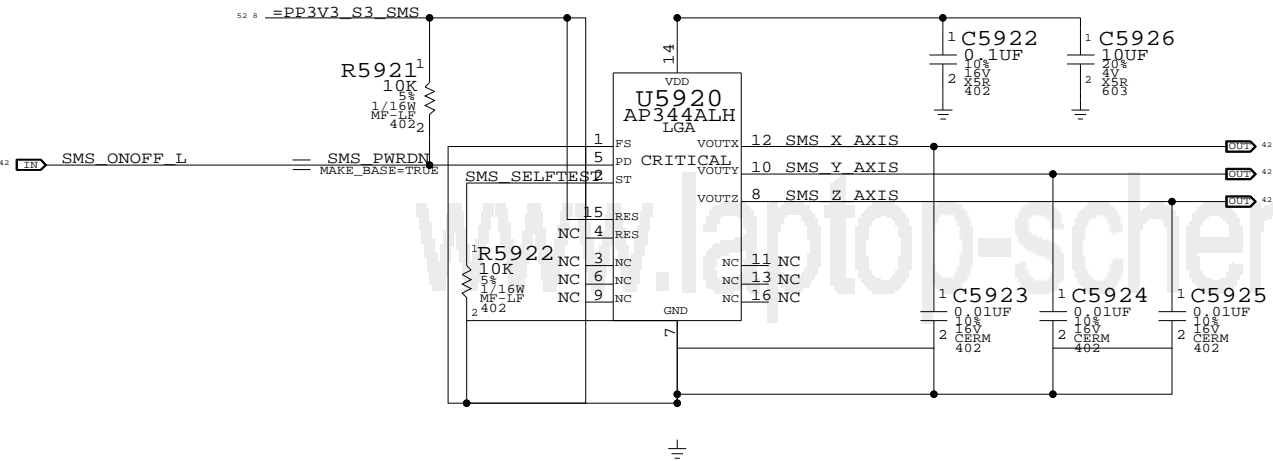
Desired orientation when placed on board top-side:



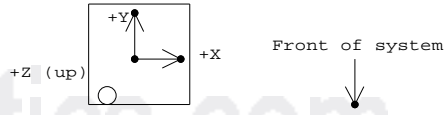
Circle indicates pin 1 location when placed in correct orientation

Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC



Desired orientation when placed on board top-side:



Circle indicates pin 1 location when placed in correct orientation

Sudden Motion Sensor (SMS)

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

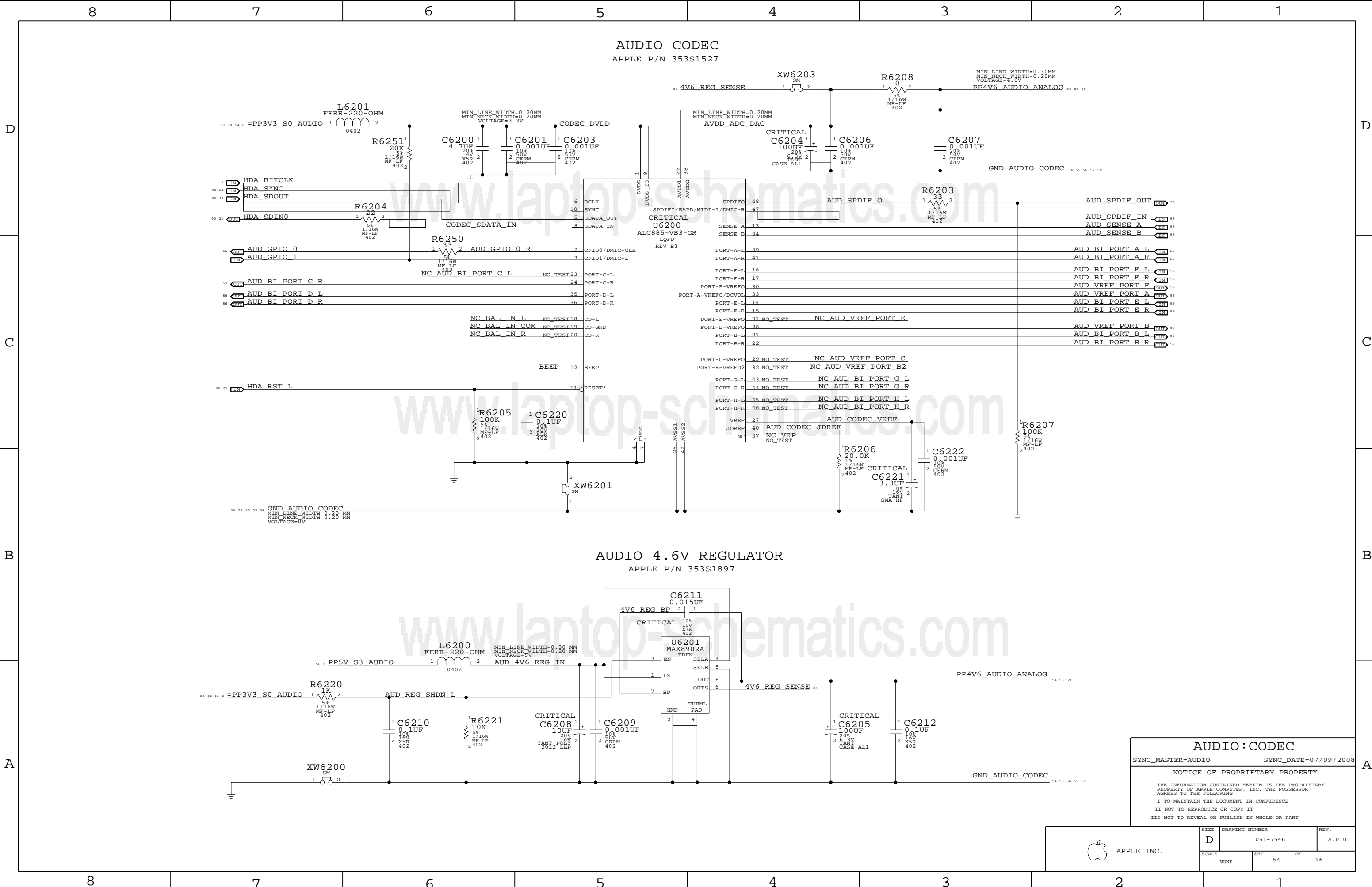
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHT	OF
NONE	52	96



AUDIO:CODEC

SYNC_MASTER=AUDIO

SYNC_DATE=07/09/2008


NOTICE OF PROPRIETARY PROPERTY

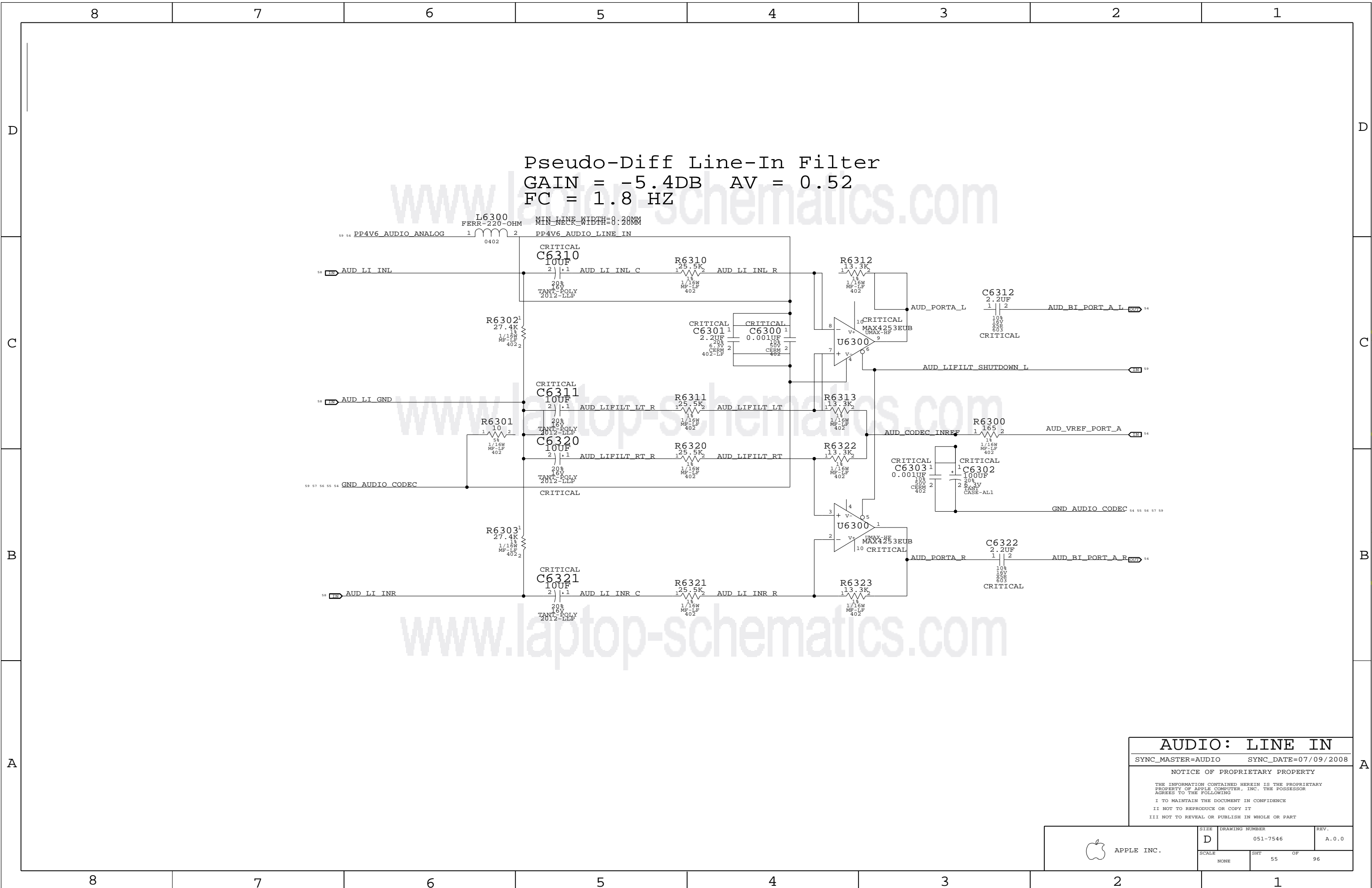
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	NONE	SHT	54 OF 96



AUDIO: LINE IN

SYNC_MASTER=AUDIO

SYNC_DATE=07/09/2008


NOTICE OF PROPRIETARY PROPERTY

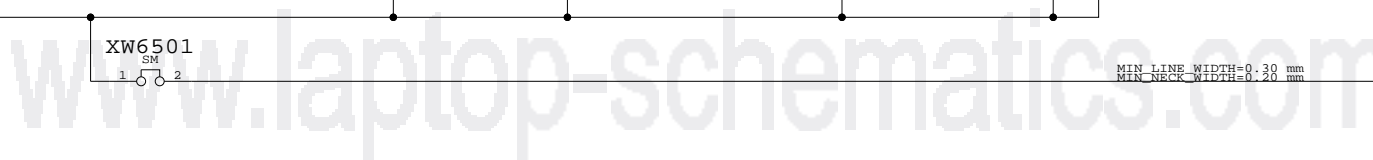
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART


 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	NONE	SHT	55 OF 96

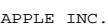


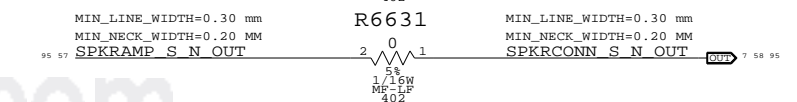
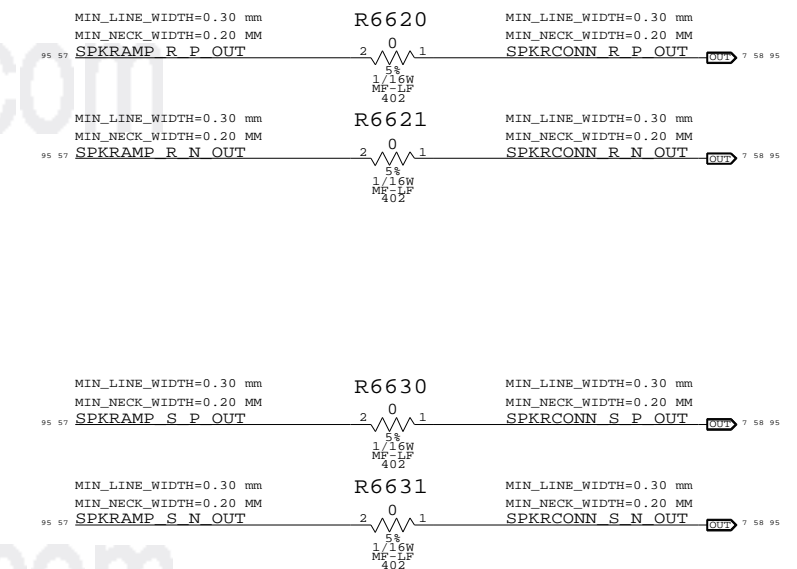
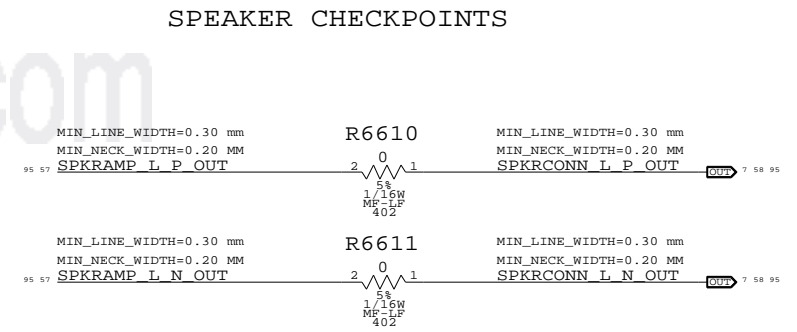
HPAMP_INL_M


Diagram illustrating the power supply section of the AD9229, showing connections for various pins and components:

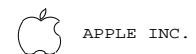
- HPAMP INR M** is connected to a **CRITICAL 6521 220PF** capacitor.
- RL PORT D B** is connected to a **CRITICAL 6520 3.30UF** capacitor.
- CODEC OUTR C** is connected to a **CRITICAL 6521 220PF** capacitor.
- HPAMP** is connected to a **CRITICAL 6521 21K** capacitor and a **25W CERN4 402** component.

 APPLE INC.	SIZE	DRAWING NUMBER		REV.
	D	051-7546		A.0.0
	SCALE	SHT	OF	
	NONE	56	96	



$$53\text{Hz} < \text{FC (SUB)} < 62\text{Hz}$$


 APPLE INC.	SIZE D	DRAWING NUMBER 051-7546	REV. A.0.0
	SCALE NONE	SHT OF 57 96	



D

C

B

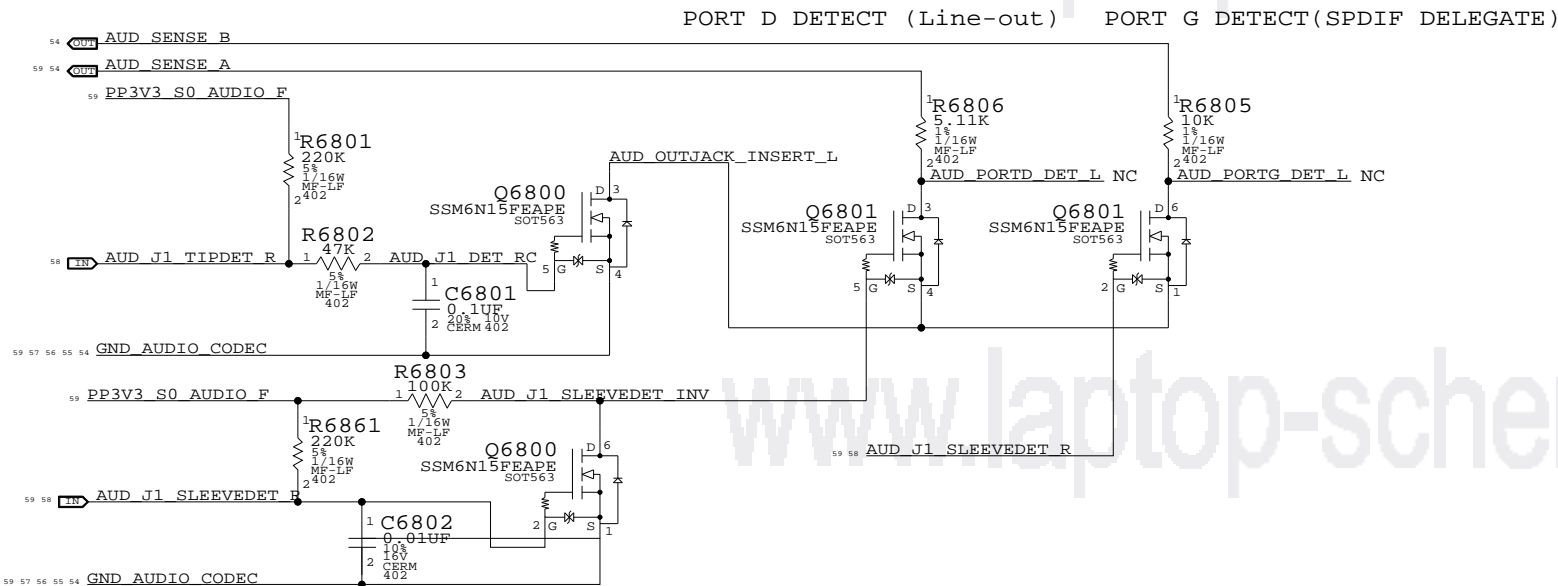
A

CODEC OUTPUT SIGNAL PATHS

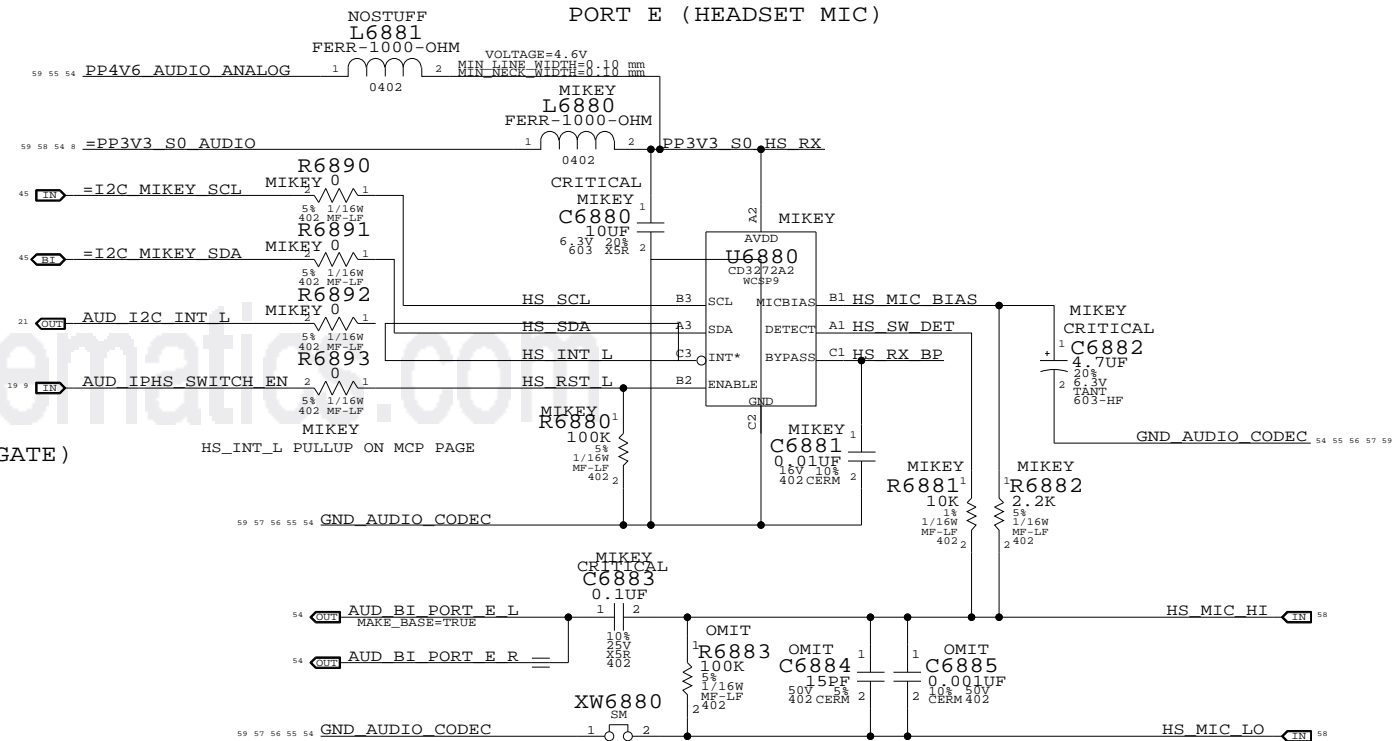
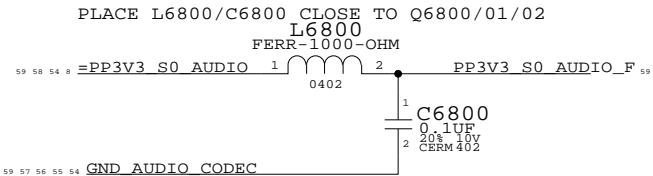
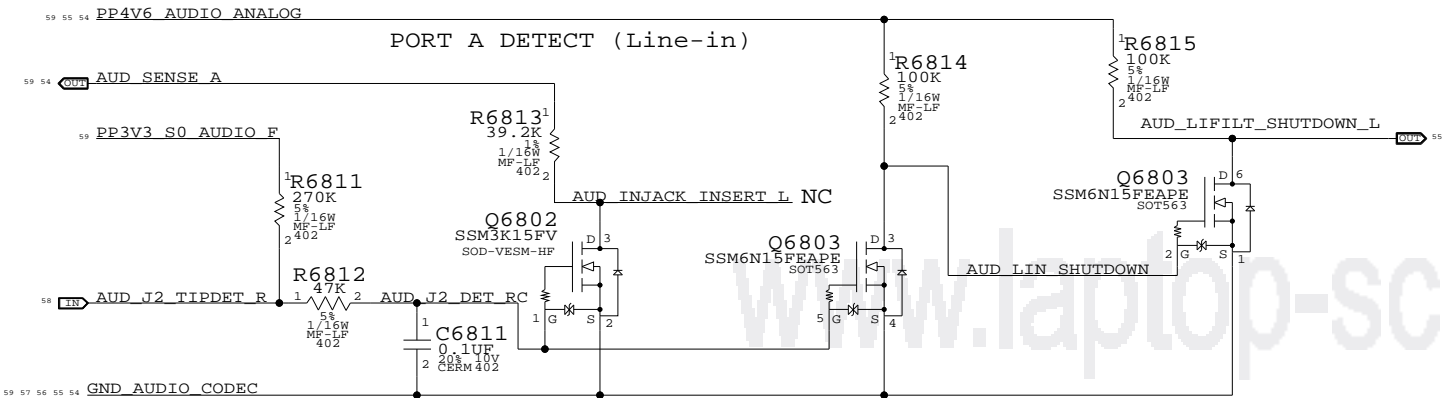
FUNCTION	VOLUME	CONVERTER	MIXER(OUTPUT)	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X0C (12)	0X02 (2)	0X0C (12)	0X14 (20,D)	GPIO_0	0X14 (20,D)
SATELLITES	0X0D (13)	0X03 (3)	0X0D (13)	0X18 (24,B)	VREF_B (100%)	N/A
SUB	0X0F (15)	0X05 (05)	0X0F (15)	0X1A (26,C)	VREF_B (100%)	N/A
SPDIF OUT	N/A	0X06 (6)		0X1E (SPDIF OUT)	N/A	0X16 (22,G)

CODEC INPUT SIGNAL PATHS

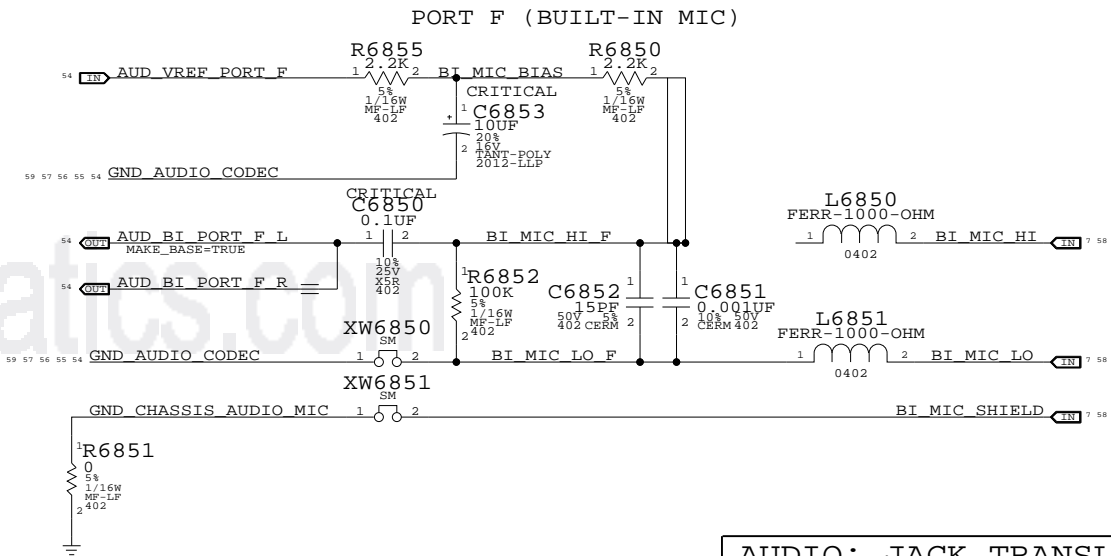
FUNCTION	MIXER(INPUT)	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X23 (35)	0X08 (8)	0X15 (21,A)	VREF_A (50%)	0X15 (21,A)
SPDIF IN	N/A	0X0A (10)	0X1F (SPDIF IN)	N/A	N/A
BUILT-IN MIC	0X24 (36)	0X07 (7)	0X19 (25,F)	VREF_F (100%)	N/A
HEADSET MIC	0X24 (36)	0X07 (7)	0X1B (27,E)	MIKEY	MIKEY



LINE_IN AMP SHUTDOWN CONTROL



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0114	1	100K 5% 0402 RESISTOR	R6883	MIKEY
131S1513	1	15PF 5% 0402 CAPACITOR	C6884	MIKEY
132S0045	1	100PF 10% 0402 CAPACITOR	C6885	MIKEY
116S0004	1	0 OHMS 5% 0402 RESISTOR	R6883	NOMIKEY
116S0004	1	0 OHMS 5% 0402 RESISTOR	C6884	NOMIKEY
116S0004	1	0 OHMS 5% 0402 RESISTOR	C6885	NOMIKEY



AUDIO: JACK TRANSLATORS

SYNC_MASTER=AUDIO SYNC_DATE=07/09/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

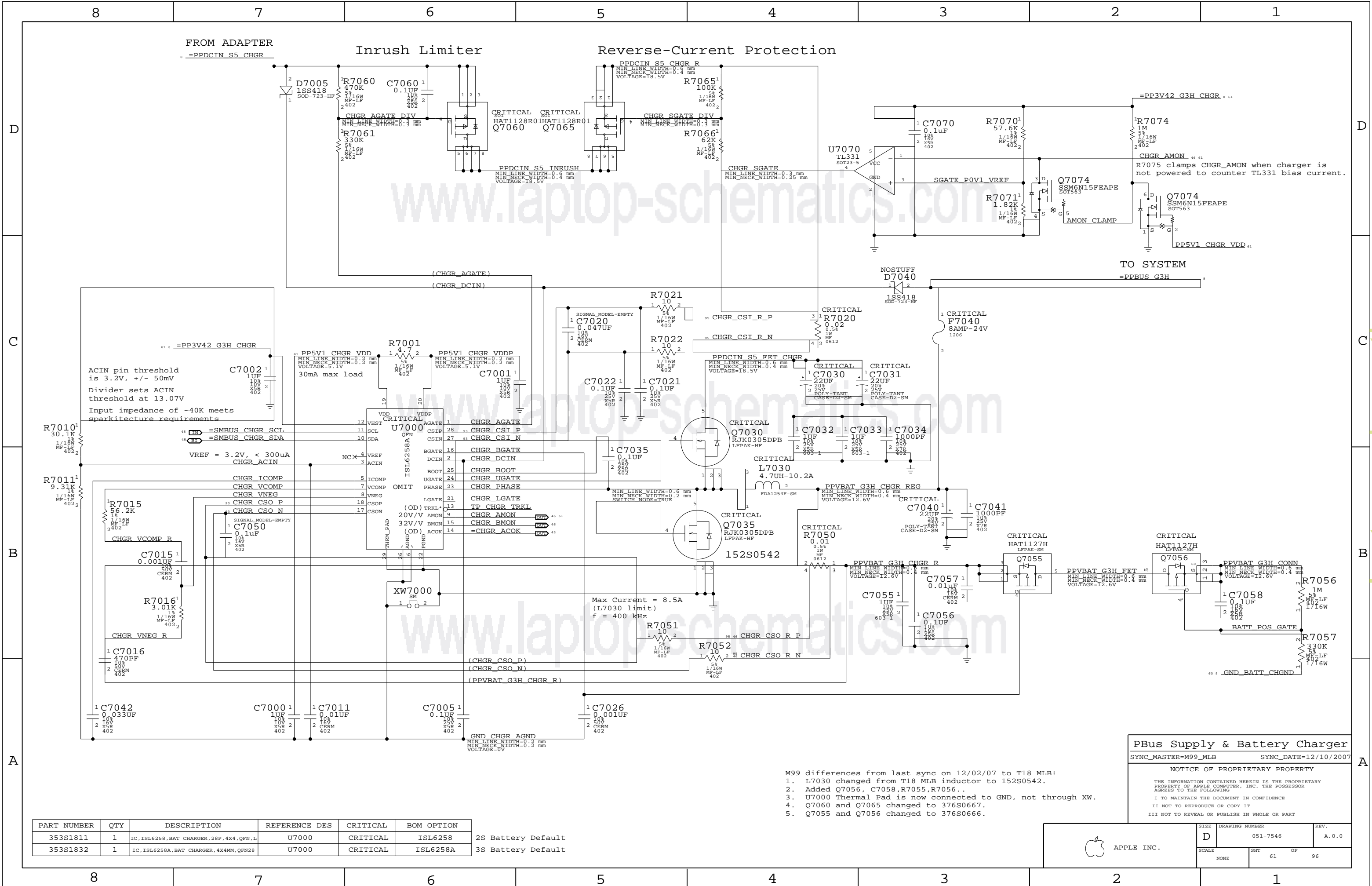
SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHT	OF
NONE	59	96

D



B

A



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S1811	1	IC, ISL6258, BAT CHARGER, 28P, 4X4, QFN, L	U7000	CRITICAL	ISL6258
353S1832	1	IC, ISL6258A, BAT CHARGER, 4X4MM, QFN28	U7000	CRITICAL	ISL6258A

2S Battery Default
3S Battery Default

- M99 differences from last sync on 12/02/07 to T18 MLB:
1. L7030 changed from T18 MLB inductor to 152S0542.
 2. Added Q7056, C7058, R7055, R7056..
 3. U7000 Thermal Pad is now connected to GND, not through XW.
 4. Q7060 and Q7065 changed to 376S0667.
 5. Q7055 and Q7056 changed to 376S0666.

PBus Supply & Battery Charger
SYNC_MASTER=M99_MLB SYNC_DATE=12/10/2007

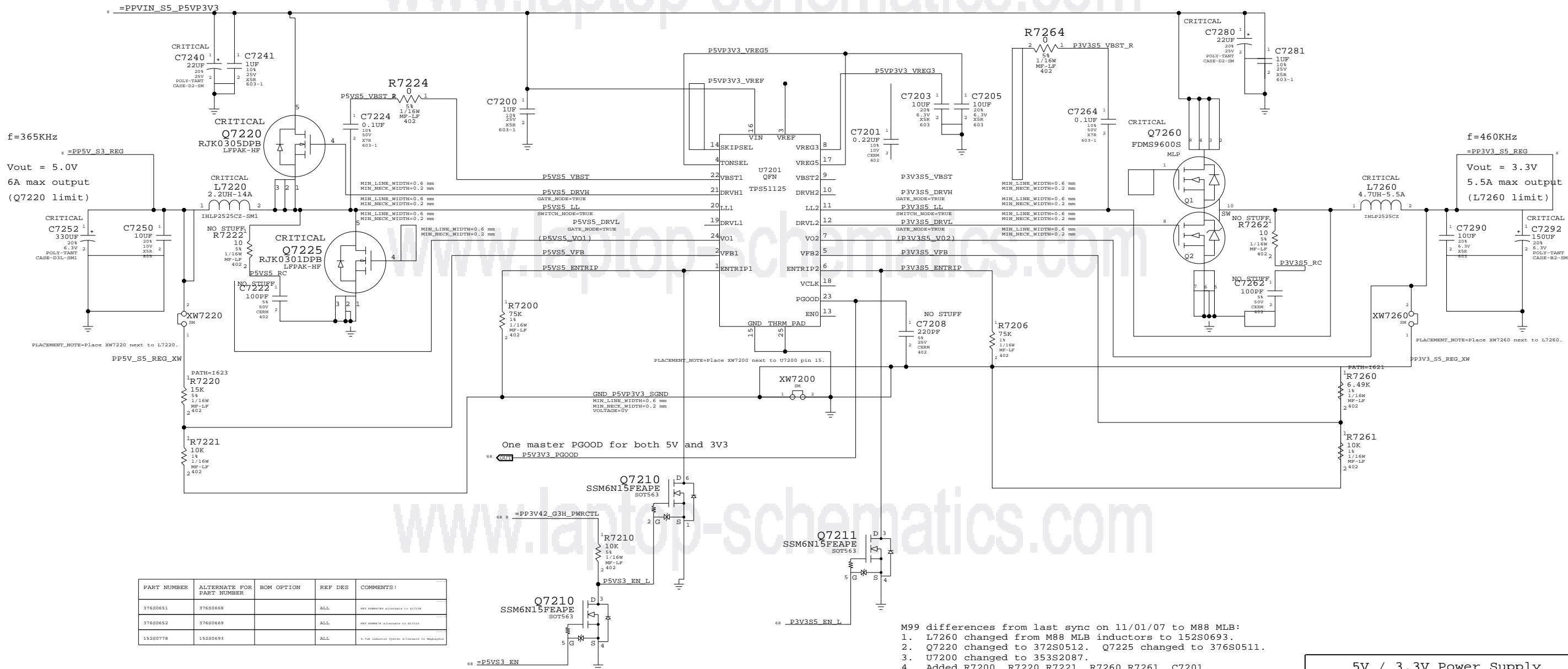
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHT	OF
NONE	61	96



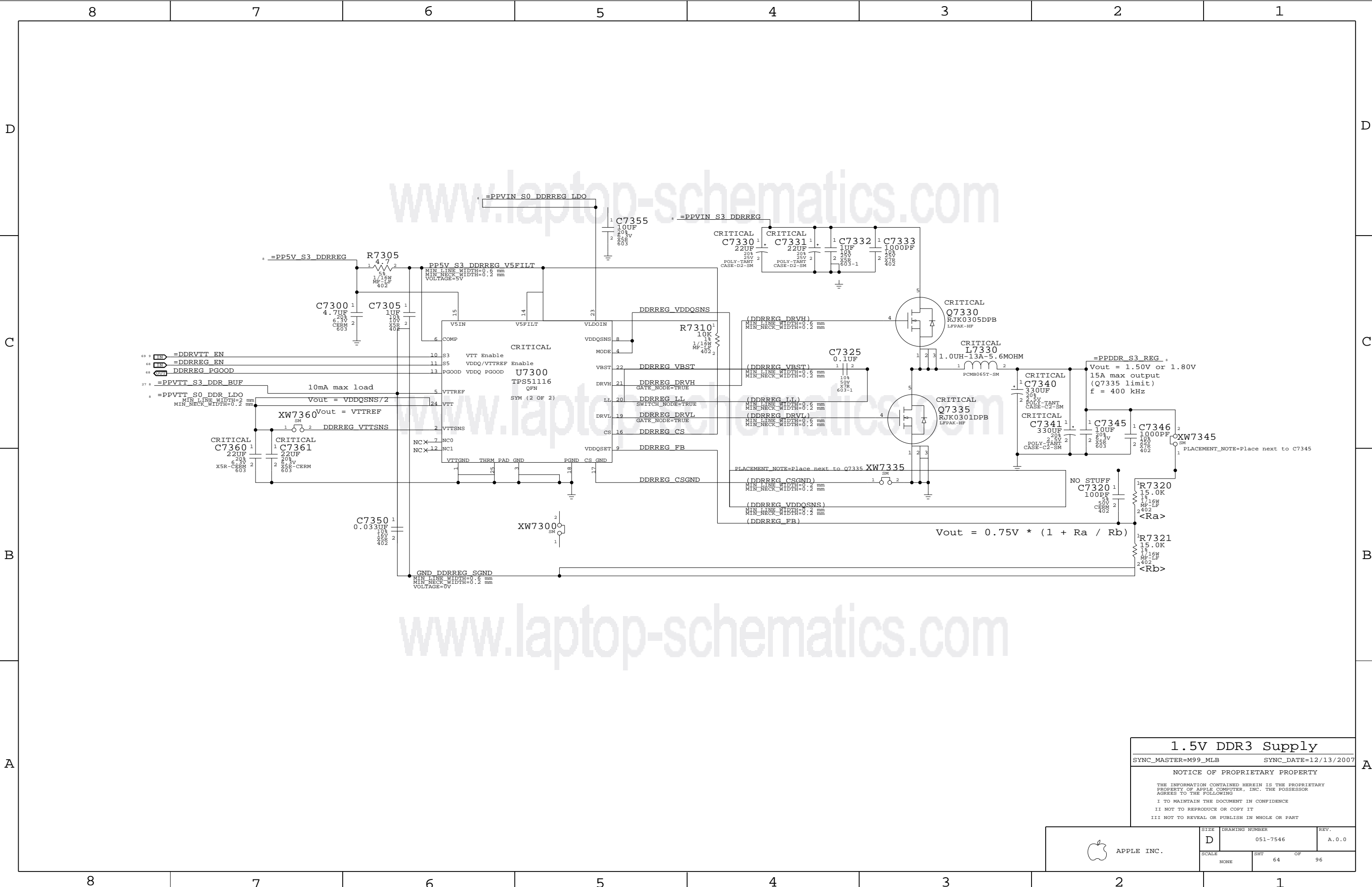


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
37680651	37680668		ALL	REV FORMERLY ASSIGNED TO 8100
37680652	37680669		ALL	REV FORMERLY ASSIGNED TO 8100
15280778	15280693		ALL	A Thin Inductive Output Inductor to Regulate

- M99 differences from last sync on 11/01/07 to M88 MLB:
1. L7260 changed from M88 MLB inductors to 152S0693.
 2. Q7220 changed to 372S0512. Q7225 changed to 376S0511.
 3. U7200 changed to 353S2087.
 4. Added R7200, R7220, R7221, R7260, R7261, C7201.

5V / 3.3V Power Supply	
SYNC_MASTER=M99_MLB	SYNC_DATE=01/09/2008
NOTICE OF PROPRIETARY PROPERTY	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING	
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE	
II NOT TO REPRODUCE OR COPY IT	
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE		SHT	OF
NONE		63	96



1.5V DDR3 Supply

SYNC_MASTER=M99_MLB SYNC_DATE=12/13/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

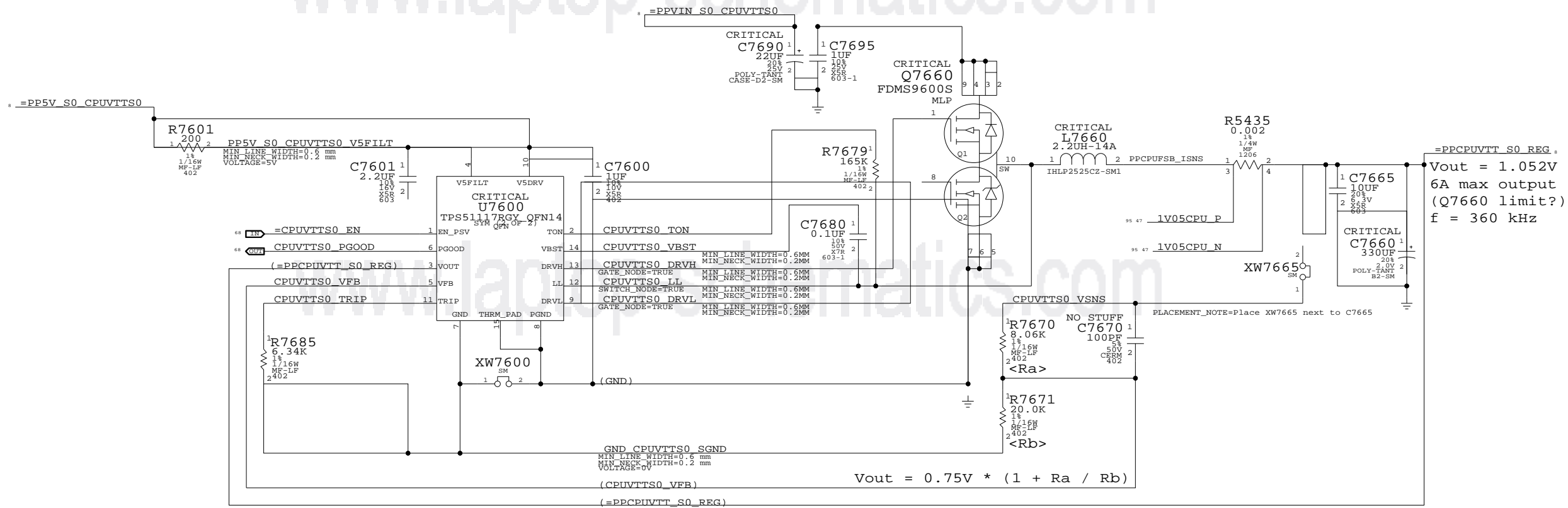
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE		SHT	OF
NONE		64	96

www.laptop-schematics.com



www.laptop-schematics.com

M99 differences from last sync on 12/03/07 to T18 MLB:
1. Tied THERMAL_PAD to PGND. GND and THERMAL_PAD disconnected.

CPU VTT Power Supply		
SYNC_MASTER=M99_MLB		SYNC_DATE=12/14/2007
NOTICE OF PROPRIETARY PROPERTY		
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING		
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE		
II NOT TO REPRODUCE OR COPY IT		
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART		

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE		SHT	OF
NONE		66	96

D

C



A



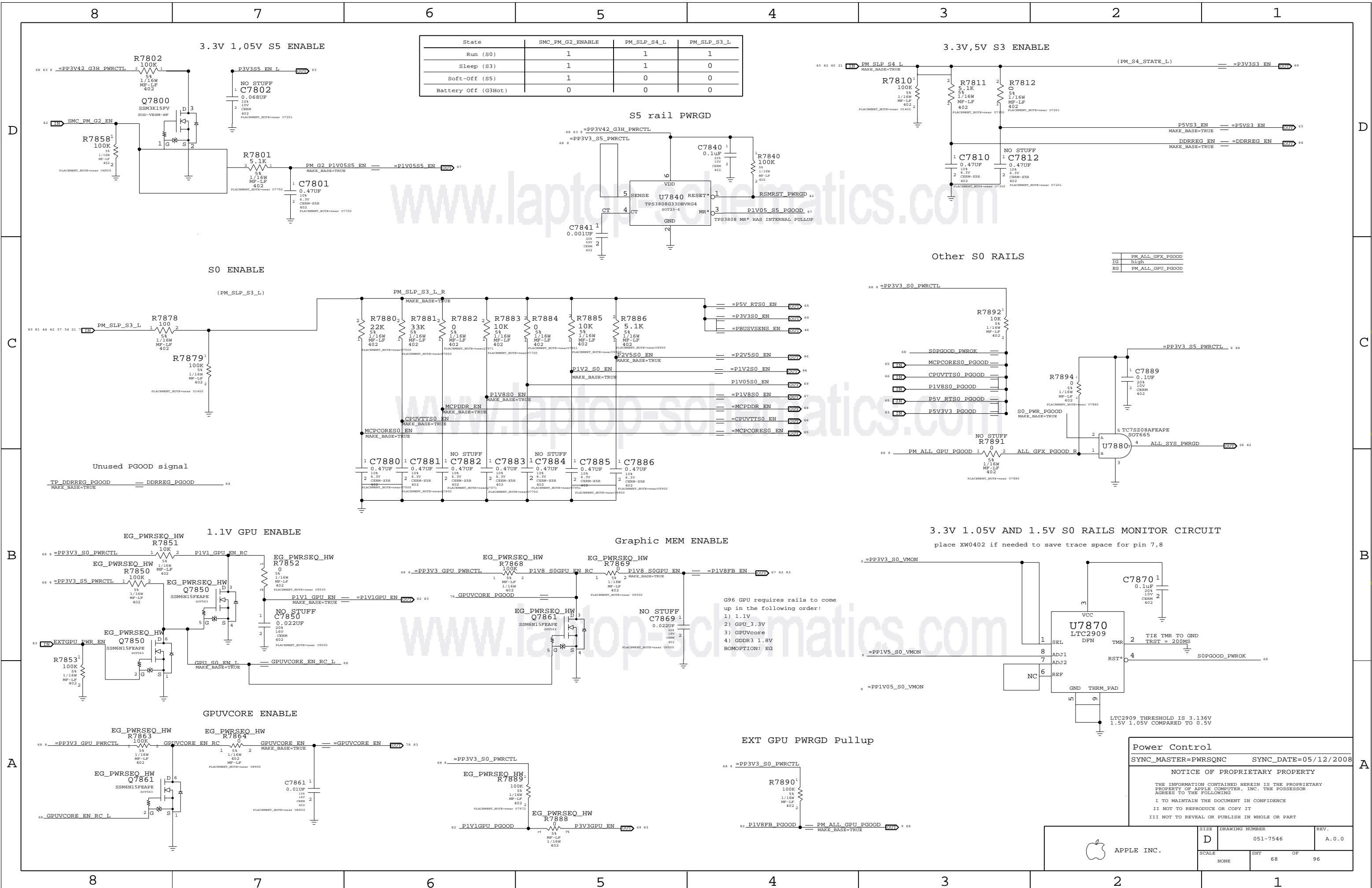
C

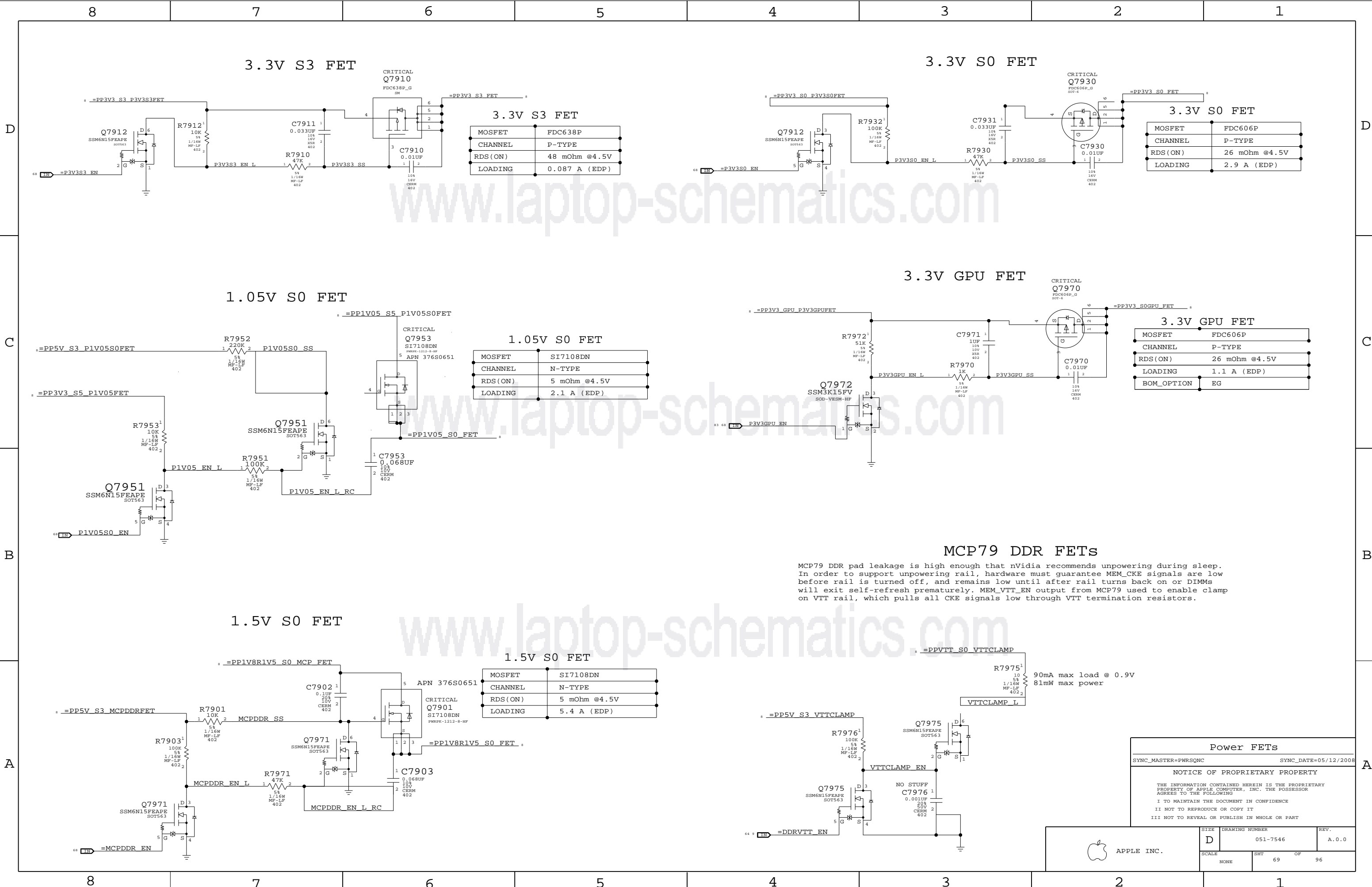


A



SIZE D	DRAWING NUMBER 051-7546	REV. A
SCALE NONE	SHT 67	OF 96





MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.087 A (EDP)

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	2.9 A (EDP)

MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	5 mOhm @4.5V
LOADING	2.1 A (EDP)

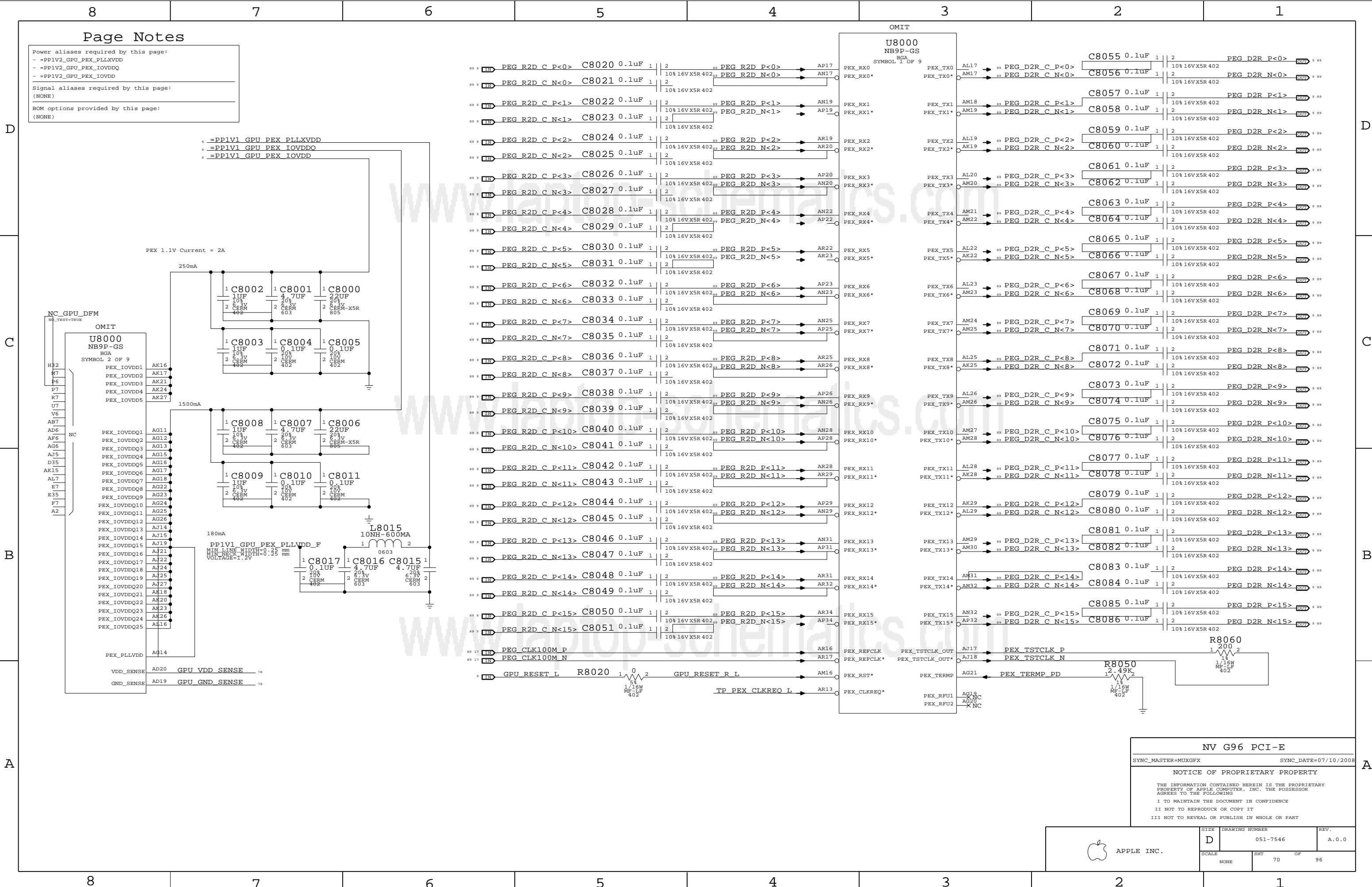
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	1.1 A (EDP)
BOM_OPTION	EG

MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	5 mOhm @4.5V
LOADING	5.4 A (EDP)

MCP79 DDR pad leakage is high enough that nVidia recommends unpowering during sleep. In order to support unpowering rail, hardware must guarantee MEM_CKE signals are low before rail is turned off, and remains low until after rail turns back on or DIMMs will exit self-refresh prematurely. MEM_VTT_EN output from MCP79 used to enable clamp on VTT rail, which pulls all CKE signals low through VTT termination resistors.

Power FETs		
SYNC_MASTER=PWRSONC		SYNC_DATE=05/12/2008
NOTICE OF PROPRIETARY PROPERTY		
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING		
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE		
II NOT TO REPRODUCE OR COPY IT		
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART		

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE		SHT	69 OF 96
NONE			



Page Notes

Power aliases required by this page:

- =PPIV2_GPU_PEX_PLLXVDD
- =PPIV2_GPU_PEX_IOVDDQ
- =PPIV2_GPU_PEX_IOVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

NV G96 PCI-E

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

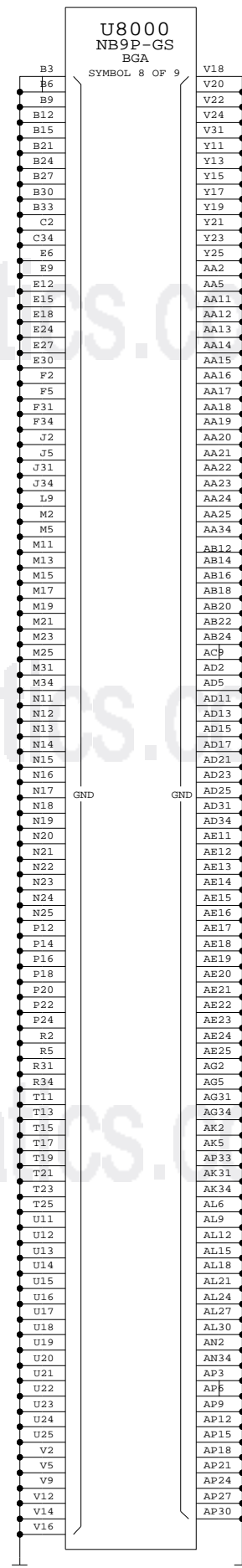
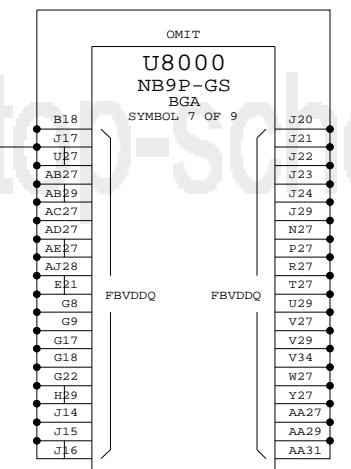
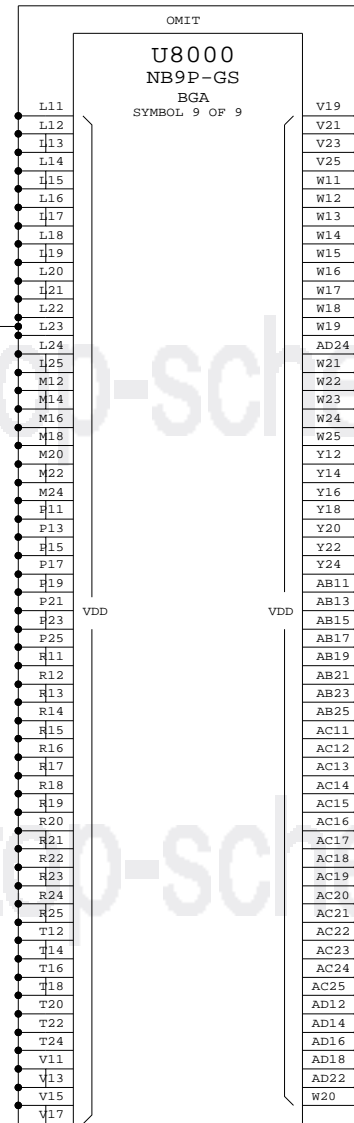
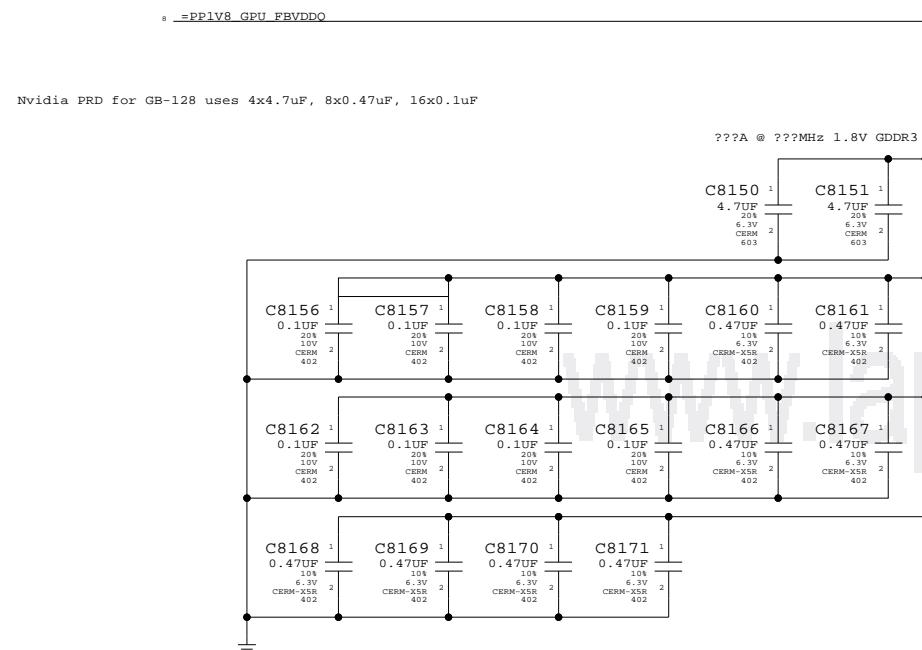
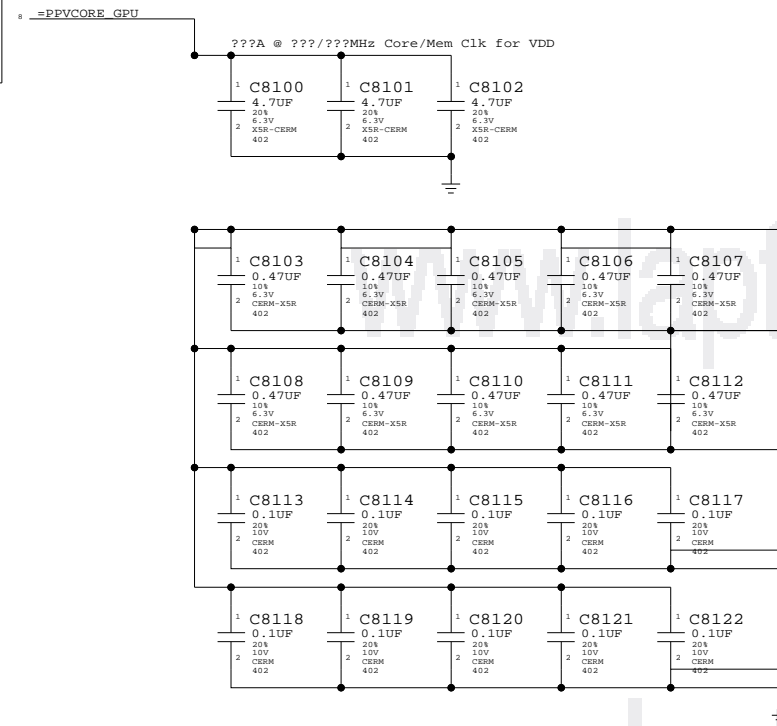
SIZE D DRAWING NUMBER 051-7546 REV. A.0.0

SCALE NONE SHIT 70 OF 96

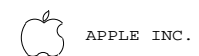
```
Power aliases required by this page:
- =PPVCORE_GPU
- =PPIV8_GPU_FBVDDQ
```

```
Signal aliases required by this page:
(NONE)
```

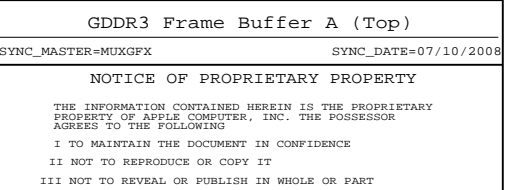
```
BOM options provided by this page:
(NONE)
```



NV G96 Core/FB Power	
SYNC_MASTER=MUXGFX	SYNC_DATE=07/10/2008
NOTICE OF PROPRIETARY PROPERTY	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING	
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE	
II NOT TO REPRODUCE OR COPY IT	
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	



SIZE D	DRAWING NUMBER 051-7546	REV. A.0.0
SCALE NONE	SHT 71	OF 96





8

7

6

5

4

3

2

1

Page Notes

Power aliases required by this page:

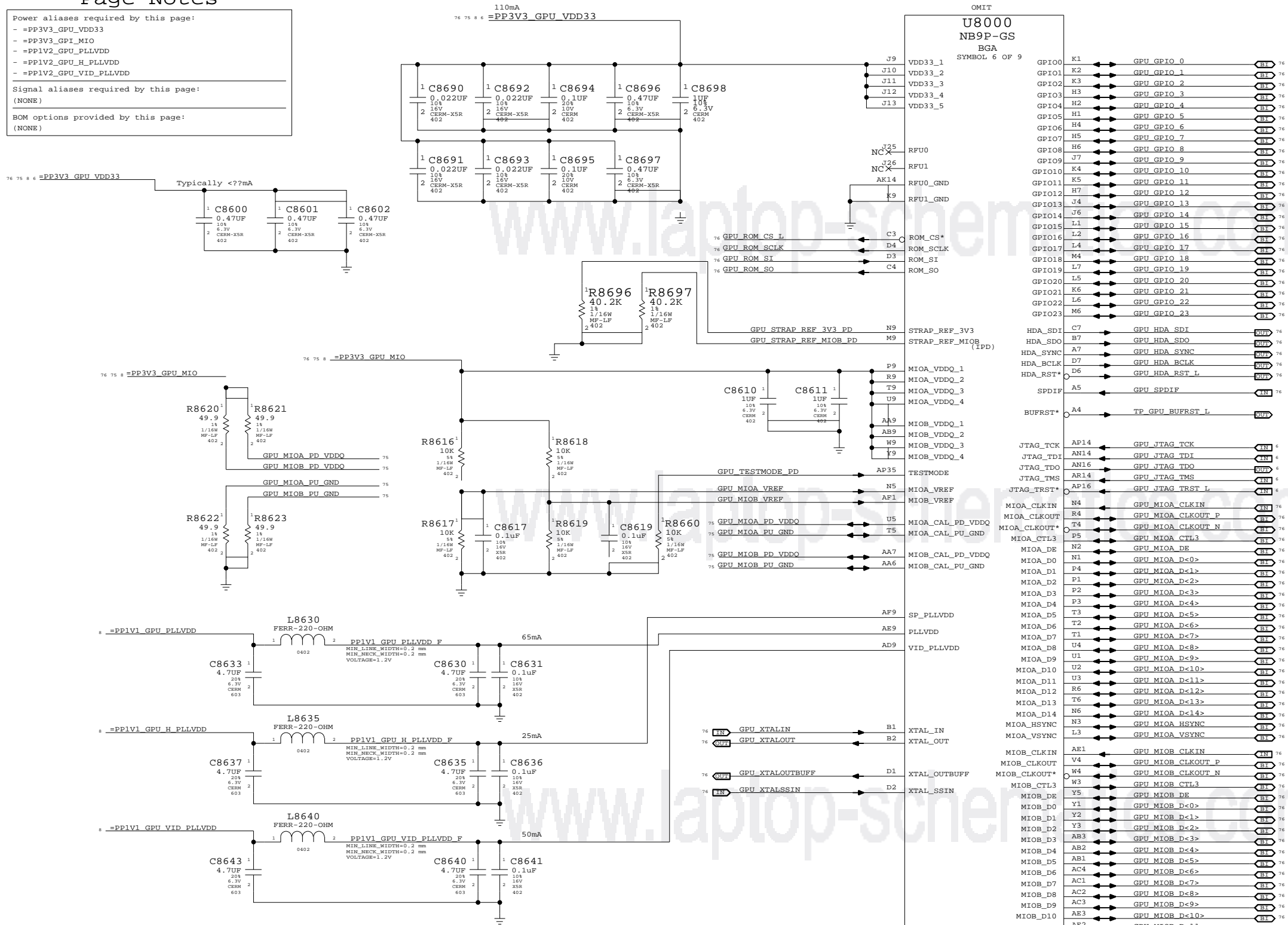
- =PP3V3_GPU_VDD33
- =PP3V3_GPU_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)



NV G96 GPIO/MIO/Misc

SYNC_MASTER=MUXGFX

SYNC_DATE=07/10/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE

D

SCALE

NONE

DRAWING NUMBER

051-7546

SHT

75

OF

96

REV.

A.0.0

8

7

6

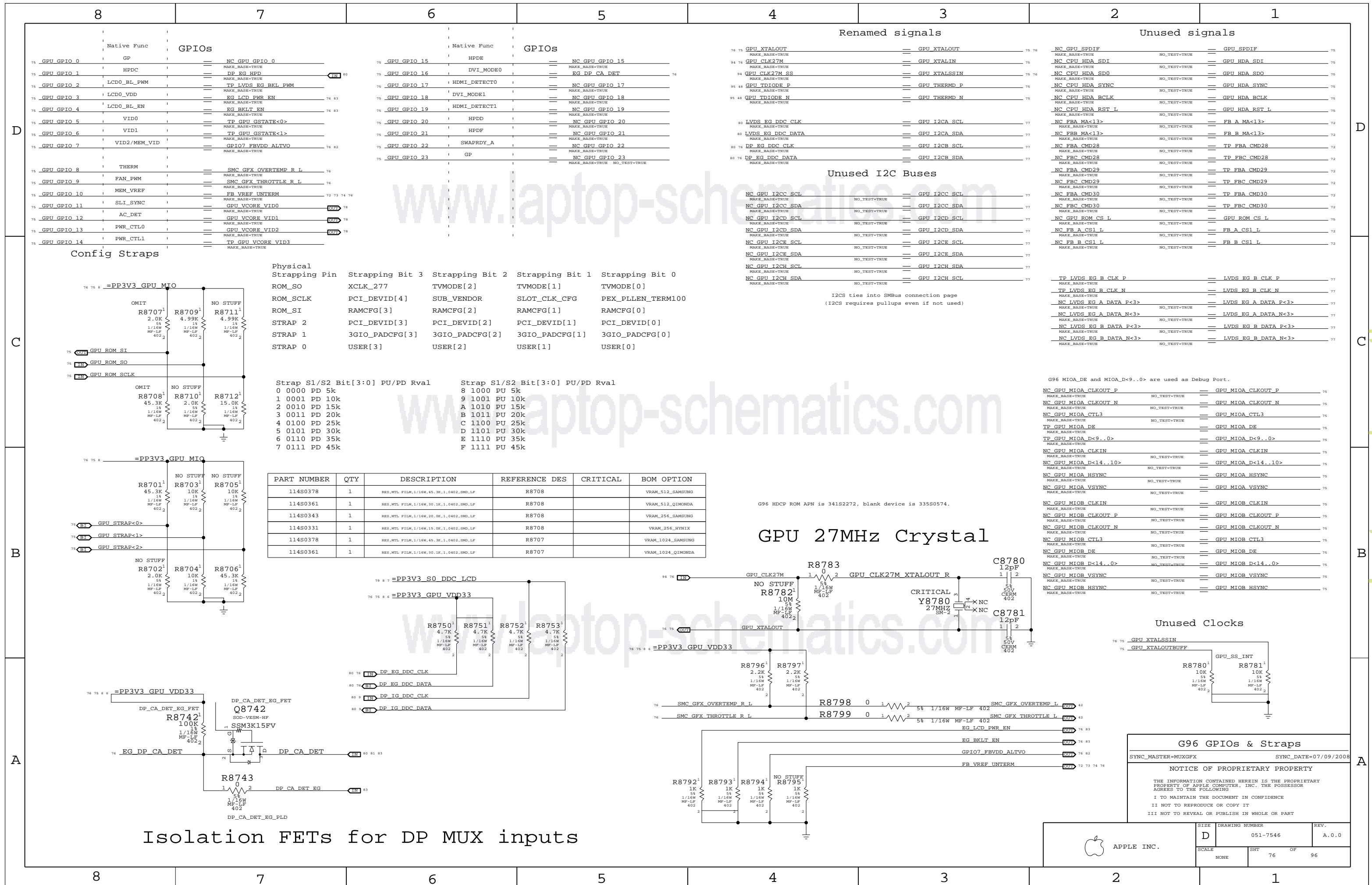
5

4

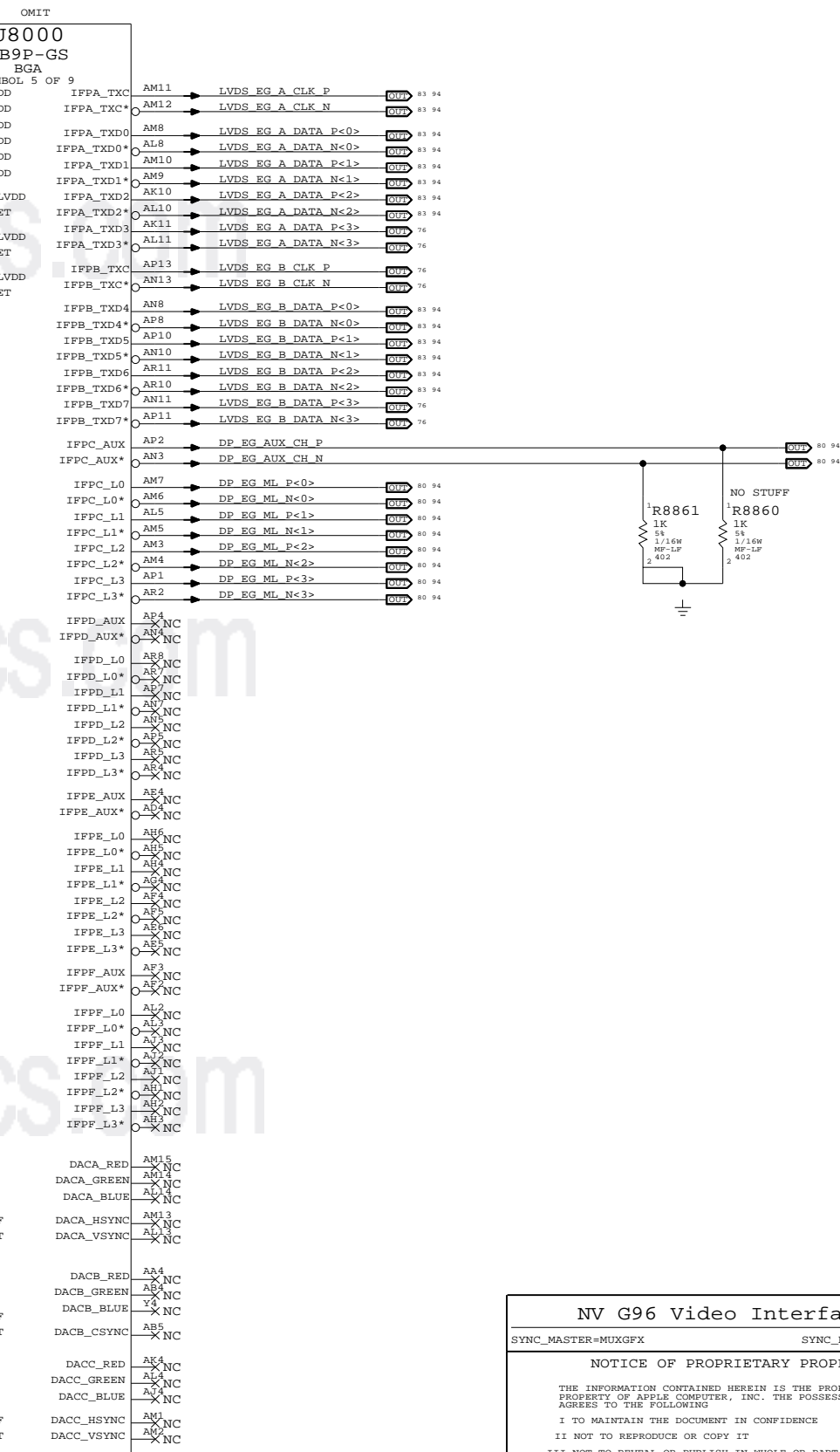
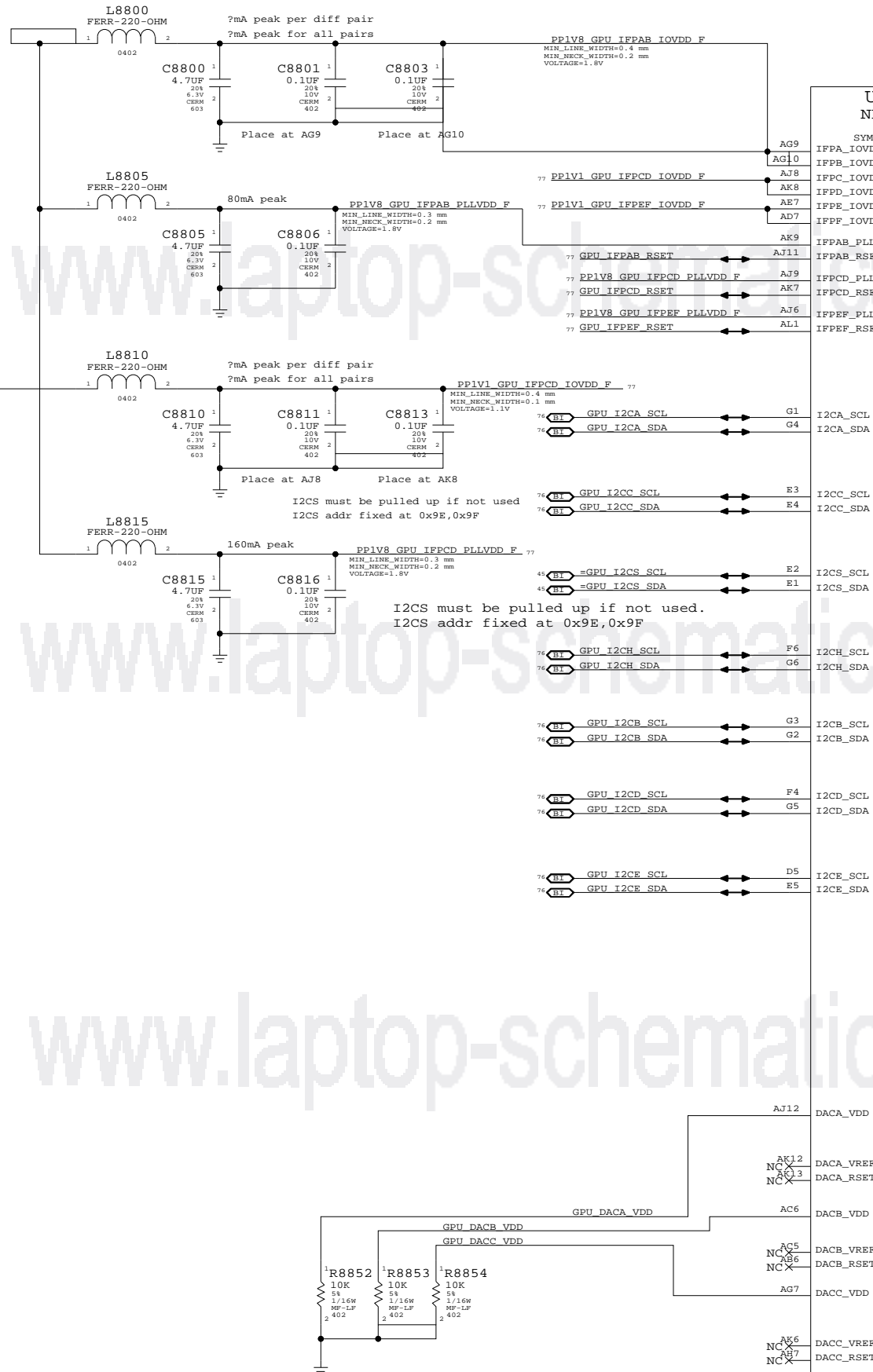
3

2

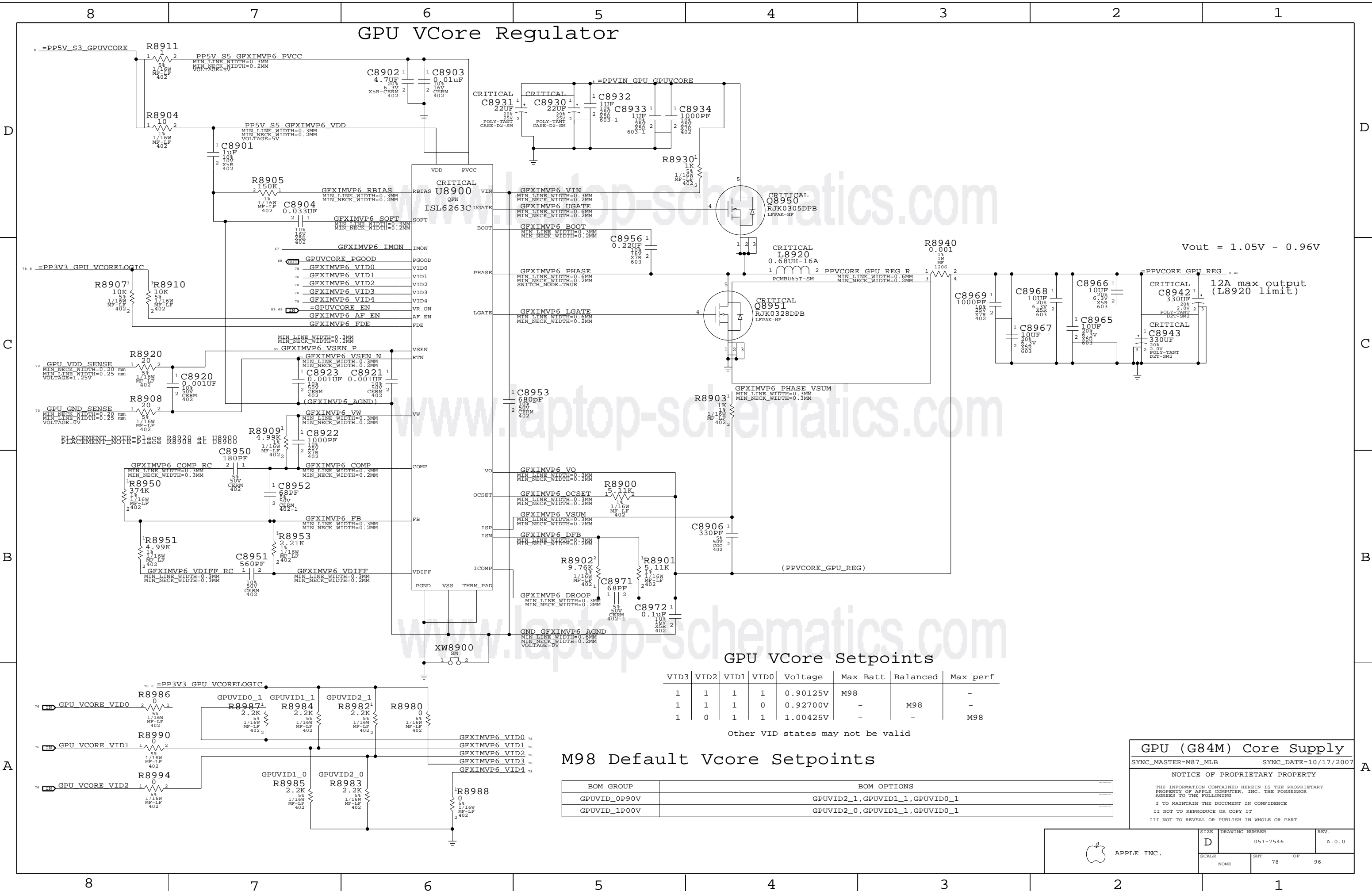
1



<u>IFPEF RSET</u>	77
<u>IFPCD RSET</u>	77
<u>IFPAB RSET</u>	77



NV G96 Video Interfaces	
SYNC_MASTER=MUXGFXX	SYNC_DATE=07/10/2008
NOTICE OF PROPRIETARY PROPERTY	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:	
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE	
I NOT TO REPRODUCE OR COPY IT	
I II NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	



D

C

B

A

D

C

B

A

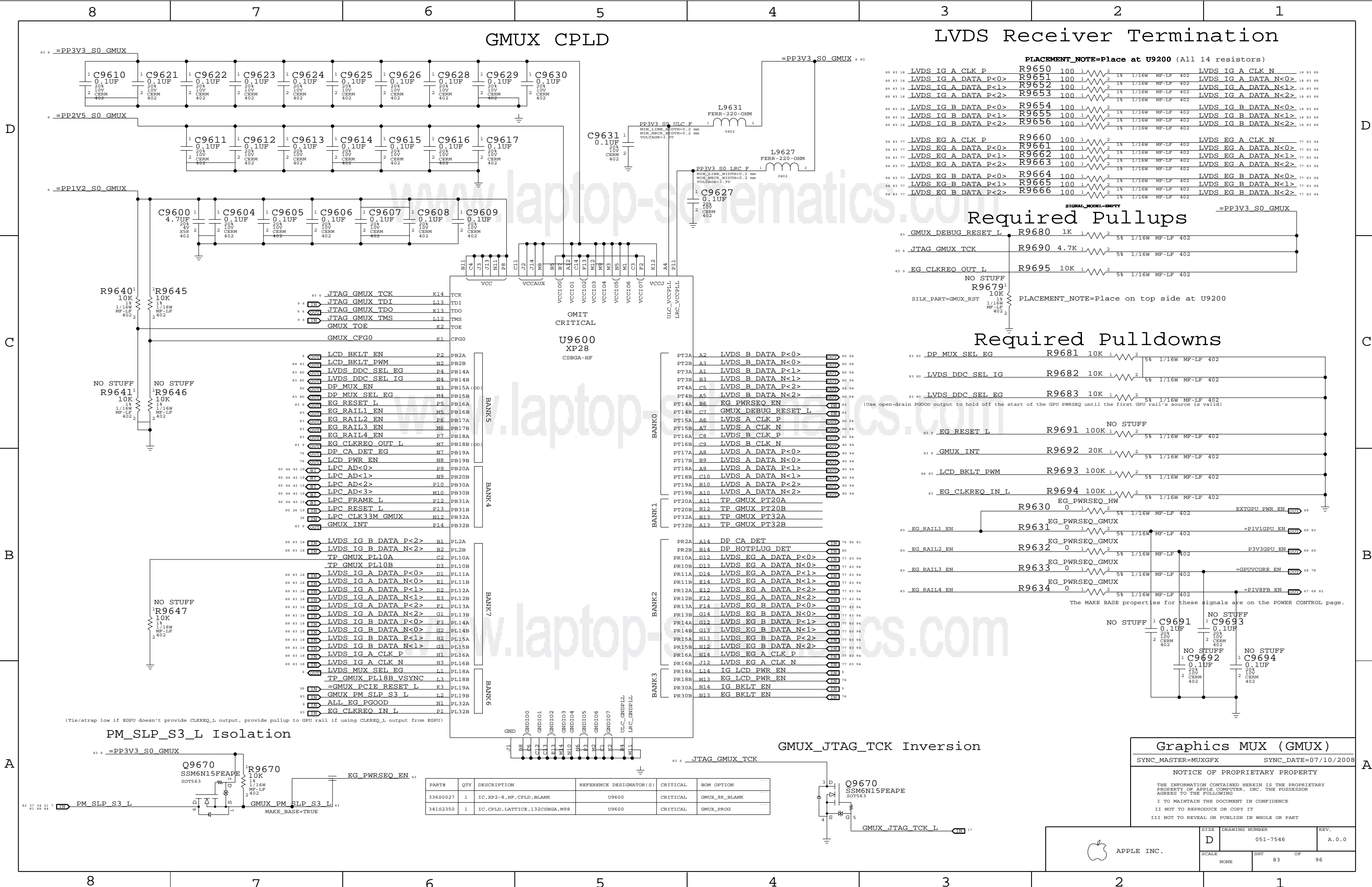
D



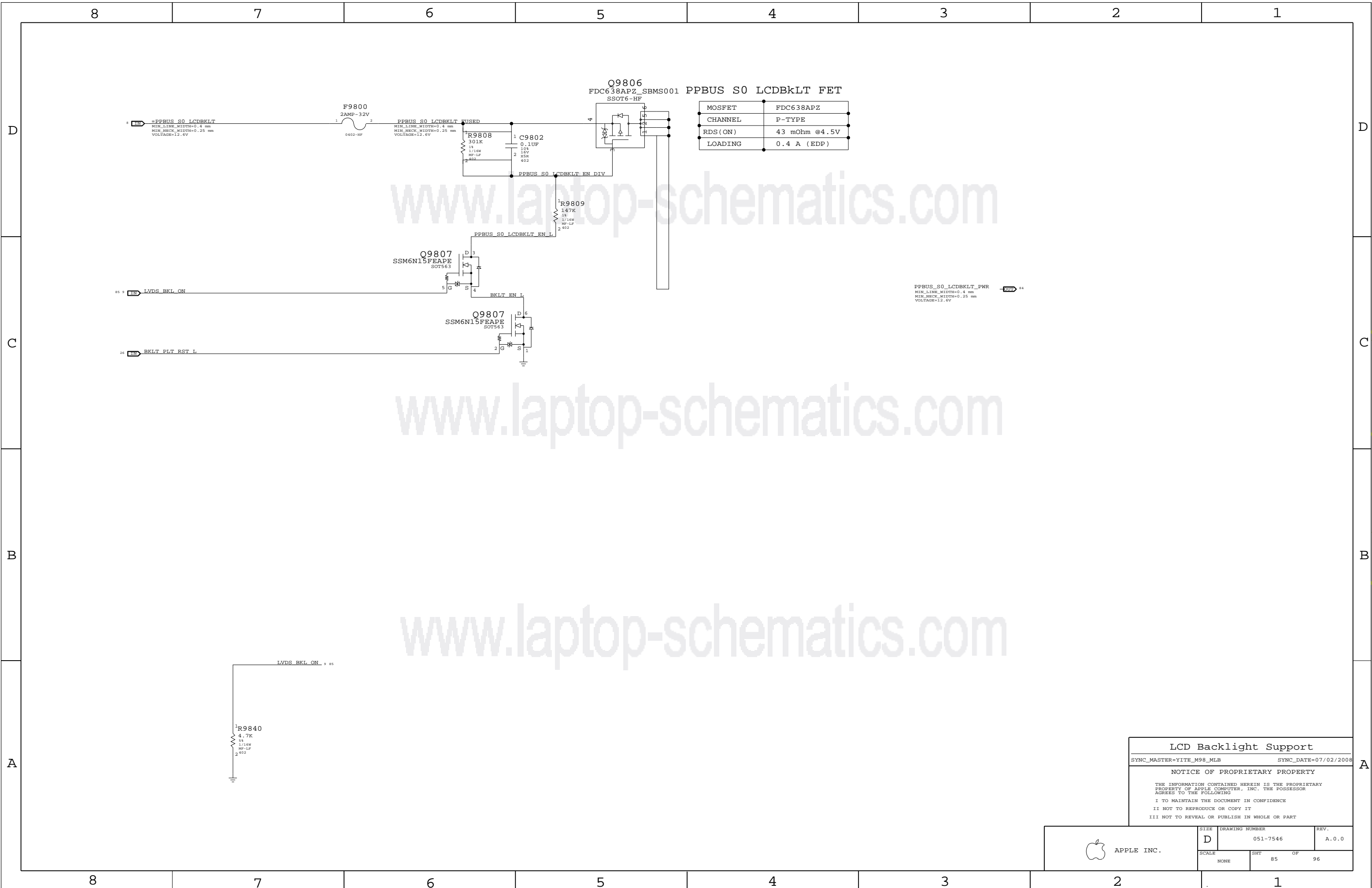
B



SIZE D	DRAWING NUMBER 051-7546	REV. A.0.0
SCALE NONE	SHT 80	OF 96



www.laptop-schematics.com



www.laptop-schematics.com

www.laptop-schematics.com

www.laptop-schematics.com

www.laptop-schematics.com

LCD Backlight Support

SYNC_MASTER=YITE_M98_MLB SYNC_DATE=07/02/2008

NOTICE OF PROPRIETARY PROPERTY

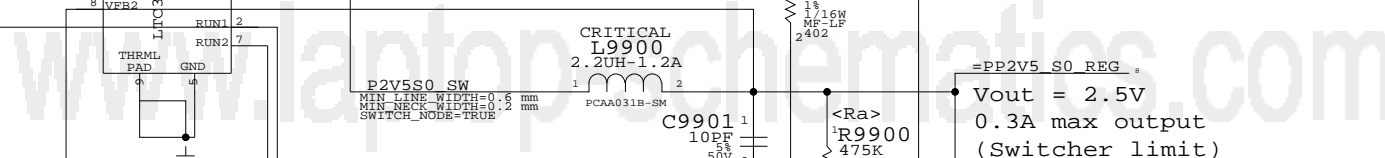
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING


I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE		SHT	OF
NONE		85	96



 APPLE INC.	SIZE D	DRAWING NUMBER 051-7546		REV. A.0.0
	SCALE NONE	SHT 86	OF 96	



8		7		6		5		4		3		2		1	
FSB (Front-Side Bus) Constraints															
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
FSB_50S		*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD							
FSB_DSTB_50S		*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR							
SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT			SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT					
FSB_DATA		*	=2x_DIELECTRIC	?			FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?					
FSB_DSTB		*	=3x_DIELECTRIC	?			FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?					
FSB_ADDR		*	=STANDARD	?			FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?					
FSB_ADSTB		*	=2x_DIELECTRIC	?			FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?					
FSB_1X		*	=STANDARD	?			FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?					
All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.															
FSB 4X signals / groups shown in signal table on right.															
Signals within each 4x group should be matched within 5 ps of strobe.															
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.															
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.															
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.															
FSB 2X signals / groups shown in signal table on right.															
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.															
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.															
FSB 1X signals shown in signal table on right.															
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.															
Design Guide recommends each strobe/signal group is routed on the same layer.															
Intel Design Guide recommends FSB signals be routed only on internal layers.															
NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.															
SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2															
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3															
CPU Signal Constraints															
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
CPU_50S		*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD							
CPU_27P4S		*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL							
NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.															
SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT			SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT					
CPU_AGTL		*	=STANDARD	?			CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?					
CPU_8MIL		*	8 MIL	?											
CPU_COMP		*	25 MIL	?											
CPU_GTLREF		*	25 MIL	?											
CPU_ITP		*	=2:1_SPACING	?											
CPU_VCCSENSE		*	25 MIL	?											
SR DG recommends at least 25 mils, >50 mils preferred															
Most CPU signals with impedance requirements are 55-ohm single-ended.															
Some signals require 27.4-ohm single-ended impedance.															
SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2															
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4															
MCP FSB COMP Signal Constraints															
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
MCP_50S		*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD							
SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT			SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT					
MCP_FSB_COMP		*	8 MIL	?											
SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4															
FSB Clock Constraints															
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
CLK_FSB_100D		*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF							
SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT			SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT					
CLK_FSB		*	=3x_DIELECTRIC	?			CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?					
SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5															
CPU / FSB Net Properties															
ELECTRICAL_CONSTRAINT_SET		NET_TYPE													
		PHYSICAL	SPACING												
FSB 4X Signal Groups	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB D L<15..0>		7 10 14									
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB DINV L<0>		7 10 14									
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<0>		7 10 14									
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<0>		7 10 14									
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB D L<31..16>		7 10 14									
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB DINV L<1>		7 10 14									
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<1>		7 10 14									
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<1>		7 10 14									
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB D L<47..32>		7 10 14									
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB DINV L<2>		7 10 14									
FSB 2X Signals	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<2>		7 10 14									
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<2>		7 10 14									
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB D L<63..48>		7 10 14									
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB DINV L<3>		7 10 14									
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<3>		7 10 14									
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<3>		7 10 14									
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB A L<16..3>		7 10 14									
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB REO L<4..0>		7 10 14									
	FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB ADSTB L<0>		7 10 14									
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB A L<35..17>		7 10 14									
FSB 1X Signals	FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB ADSTB L<1>		7 10 14									
	FSB_1X	FSB_50S	FSB_1X	FSB ADS L		7 10 14									
	FSB_BREQ0_L	FSB_50S	FSB_1X	FSB BREQ0 L		9 10 14									
	FSB_BREQ1_L	FSB_50S	FSB_1X	FSB BREQ1 L		14									
	FSB_1X	FSB_50S	FSB_1X	FSB BNR L		10 14									
	FSB_1X	FSB_50S	FSB_1X	FSB BPRI L		10 14									
	FSB_1X	FSB_50S	FSB_1X	FSB DBSY L		10 14									
	FSB_1X	FSB_50S	FSB_1X	FSB DEFER L		10 14									
	FSB_1X	FSB_50S	FSB_1X	FSB DRDY L		10 14									
	FSB_1X	FSB_50S	FSB_1X	FSB HIT L		7 10 14									
FSB_1X	FSB_50S	FSB_1X	FSB HITM L		7 10 14										
FSB_1X	FSB_50S	FSB_1X	FSB LOCK L		7 10 14										
FSB_CPURST_L	FSB_50S	FSB_1X	FSB CPURST L		9 10 13 14										
FSB_1X	FSB_50S	FSB_1X	FSB RS L<2..0>		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L		10 14										

8

7

6

5

4

3

2

1

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair.

DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.

All DQS pairs should be matched within 100 ps of clocks.

CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.

A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.

All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).

DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.

DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 180 ps

No DQS to clock matching requirement.

CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.

A/BA/cmd signals should be matched within 5 ps of CLK pairs.

All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).

DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM A CLK P<5..0>	15 28
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM A CLK N<5..0>	15 28
MEM_A_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM A CKE<3..0>	15 28
MEM_A_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM A CS_L<3..0>	15 28
MEM_A_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM A ODT<3..0>	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A A<14..0>	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A BA<2..0>	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A RAS_L	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A CAS_L	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A WE_L	15 28
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DQ<7..0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DQ<15..8>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DQ<23..16>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DQ<31..24>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DQ<39..32>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DQ<47..40>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DQ<55..48>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DQ<63..56>	15 28
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DM<0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DM<1>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DM<2>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DM<3>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DM<4>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DM<5>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DM<6>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DM<7>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS P<0>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS N<0>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS P<1>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS N<1>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS P<2>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS N<2>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS P<3>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS N<3>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS P<4>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS N<4>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS P<5>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS N<5>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS P<6>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS N<6>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS P<7>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS N<7>	15 28
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM B CLK P<5..0>	15 29
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM B CLK N<5..0>	15 29
MEM_B_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM B CKE<3..0>	15 29
MEM_B_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM B CS_L<3..0>	15 29
MEM_B_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM B ODT<3..0>	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B A<14..0>	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B BA<2..0>	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B RAS_L	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B CAS_L	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B WE_L	15 29
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DQ<7..0>	15 29
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DQ<15..8>	15 29
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DQ<23..16>	15 29
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DQ<31..24>	15 29
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DQ<39..32>	15 29
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DQ<47..40>	15 29
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DQ<55..48>	15 29
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DQ<63..56>	15 29
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DM<0>	15 29
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DM<1>	15 29
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DM<2>	15 29
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DM<3>	15 29
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DM<4>	15 29
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DM<5>	15 29
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DM<6>	15 29
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DM<7>	15 29
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS P<0>	15 29
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS N<0>	15 29
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS P<1>	15 29
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS N<1>	15 29
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS P<2>	15 29
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS N<2>	15 29
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS P<3>	15 29
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS N<3>	15 29
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS P<4>	15 29
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS N<4>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS P<5>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS N<5>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS P<6>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS N<6>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS P<7>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS N<7>	15 29
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP VDD	16
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP GND	16

Memory Constraints

SYNC_MASTER=MUXGFX

SYNC_DATE=02/18/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE D

DRAWING NUMBER 051-7546

REV. A.0.0

SCALE NONE

SHT 88

OF 96

8

7

6

5

4

3

2

1

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	= 2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

ELECTRICAL_CONSTRAINT_SET	NET TYPE		
	PHYSICAL	SPACING	
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7..0>
PCI_AD	PCI_55S	PCI	PCI_AD<23..8>
PCI_AD24	PCI_55S	PCI	PCI_AD<24>
PCI_AD	PCI_55S	PCI	PCI_AD<31..25>
PCI_AD	PCI_55S	PCI	PCI_PAR
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L
PCI_REQ0_L	PCI_55S	PCI	PCI_REQ0_L
PCI_GNT0_L	PCI_55S	PCI	PCI_GNT0_L
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L
PCI_INTW_L	PCI_55S	PCI	PCI_INTW_L
PCI_INTX_L	PCI_55S	PCI	PCI_INTX_L
PCI_INTY_L	PCI_55S	PCI	PCI_INTY_L
PCI_INTZ_L	PCI_55S	PCI	PCI_INTZ_L
MCP_PCI_CLK2	CLK_PCI_55S	CLK_PCI	PCI_CLK33M MCP_R
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M MCP
LPC_AD	LPC_55S	LPC	LPC_AD<3..0>
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M SMC_R
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M SMC
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M LPCPLUS
USB_EXT_A	USB_90D	USB	USB_EXT_A_P
	USB_90D	USB	USB_EXT_A_N
	USB_90D	USB	USB_EXT_A_MUXED_P
	USB_90D	USB	USB_EXT_A_MUXED_N
USB_MINI	USB_90D	USB	USB_MINI_P
	USB_90D	USB	USB_MINI_N
USB_EXTD	USB_90D	USB	USB_EXTD_P
	USB_90D	USB	USB_EXTD_N
USB_CAMERA	USB_90D	USB	USB_CAMERA_P
	USB_90D	USB	USB_CAMERA_N
USB_BT	USB_90D	USB	USB_BT_P
	USB_90D	USB	USB_BT_N
USB_TPAD	USB_90D	USB	USB_TPAD_P
	USB_90D	USB	USB_TPAD_N
USB_IR	USB_90D	USB	USB_IR_P
	USB_90D	USB	USB_IR_N
USB_EXTB	USB_90D	USB	USB_EXTB_P
	USB_90D	USB	USB_EXTB_N
USB_EXCARD	USB_90D	USB	USB_EXCARD_P
	USB_90D	USB	USB_EXCARD_N
USB_EXTC	USB_90D	USB	USB_EXTC_P
	USB_90D	USB	USB_EXTC_N
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND
SMBUS_MCP_0_CLK	SMR_55S	SMR	SMBUS_MCP_0_CLK
SMBUS_MCP_0_DATA	SMR_55S	SMR	SMBUS_MCP_0_DATA
SMBUS_MCP_1_CLK	SMR_55S	SMR	SMBUS_MCP_1_CLK
SMBUS_MCP_1_DATA	SMR_55S	SMR	SMBUS_MCP_1_DATA
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK
	HDA_55S	HDA	HDA_BIT_CLK_R
HDA_SYNC	HDA_55S	HDA	HDA_SYNC
	HDA_55S	HDA	HDA_SYNC_R
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L
	HDA_55S	HDA	HDA_RST_L
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0
	HDA_55S	HDA	HDA_SDIN_CODEC
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT
	HDA_55S	HDA	HDA_SDOUT_R
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R
	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK
SPI_CLK	SPI_55S	SPI	SPI_CLK_R
	SPI_55S	SPI	SPI_CLK
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R
	SPI_55S	SPI	SPI_MOSI
SPI_MISO	SPI_55S	SPI	SPI_MISO
	SPI_55S	SPI	SPI_MISO_R
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L
	SPI_55S	SPI	SPI_CS0_L


```

MCP Constraints 2
-----
SYNC_MASTER=MUXGFX                      SYNC_DATE=02/18/2008
-----
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY
PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR
AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

```

 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
	SCALE	SHT OF	
	NONE	90	96



D

C

B

A

D

C

B

A

www.laptop-schematics.com



www.laptop-schematics.com

www.laptop-schematics.com

www.laptop-schematics.com

www.laptop-schematics.com

	8	7	6	5	4	3	2	1
D	GDDR3 Frame Buffer Signal Constraints							
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	GDDR3_40R55SE	*	=55_OHM_SE	=40_OHM_SE	0.095 MM	12.7 MM	=STANDARD	=STANDARD
C	GDDR3 FB A/B Net Properties							
	NET_TYPE	PHYSICAL	SPACING					
	ELECTRICAL_CONSTRAINT_SET							
B	GDDR3 FB C/D Net Properties							
	NET_TYPE	PHYSICAL	SPACING					
	ELECTRICAL_CONSTRAINT_SET							
A	MUXGFX Net Properties							
	NET_TYPE	PHYSICAL	SPACING					
	ELECTRICAL_CONSTRAINT_SET							
	G96 Net Properties							
	NET_TYPE	PHYSICAL	SPACING					
	ELECTRICAL_CONSTRAINT_SET							
	GPU (G96) Constraints							
	SYNC_MASTER=MUXGFX							
	SYNC_DATE=02/18/2008							
	NOTICE OF PROPRIETARY PROPERTY							
	THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING							
	I TO MAINTAIN THE DOCUMENT IN CONFIDENCE							
	II NOT TO REPRODUCE OR COPY IT							
	III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART							
	DRAWING NUMBER							
	051-7546							
	REV. A.0.0							
	SCALE							
	NONE							
	SHT 94 OF 96							
	APPLE INC.							

