

8

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1

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM, MLB, MBP17

05/18/2007

REV

ZONE

ECN

DESCRIPTION OF CHANGE

CK APPD

ENG APPD

B

505154

PRODUCTION RELEASED

05/18/07

07

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N/A

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(T9_MLB)

08/23/2006

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(T9_MLB)

08/23/2006

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Power Block Diagram

N/A

N/A

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BOM Configuration

N/A

N/A

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N/A

N/A

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MASTER

MASTER

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(MASTER)

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M75/M76 Rule Definitions

M76_MLB

02/02/2007

SCHEMATIC / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7430	1	SCHEM, MLB, MBP17	SCH	CRITICAL	
820-2132	1	PCBF, MLB, MBP17	PCB	CRITICAL	

DRAWING

TITLE=MLB

ABBREV=DRAWING

LAST_MODIFIED=Fri May 18 17:08:49 2007

DIMENSIONS ARE IN MILLIMETERS

XX : _____

X.XX : _____

X.XXX : _____

ANGLES : _____

DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER	/	DESIGN CK	/
ENG APPD	/	MFG APPD	/
QA APPD	/	DESIGNER	/
RELEASE	/	SCALE	NONE
MATERIAL/FINISH		SIZE	D
NOTED AS APPLICABLE			

Apple Computer Inc.

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SCHEM, MLB, MBP17

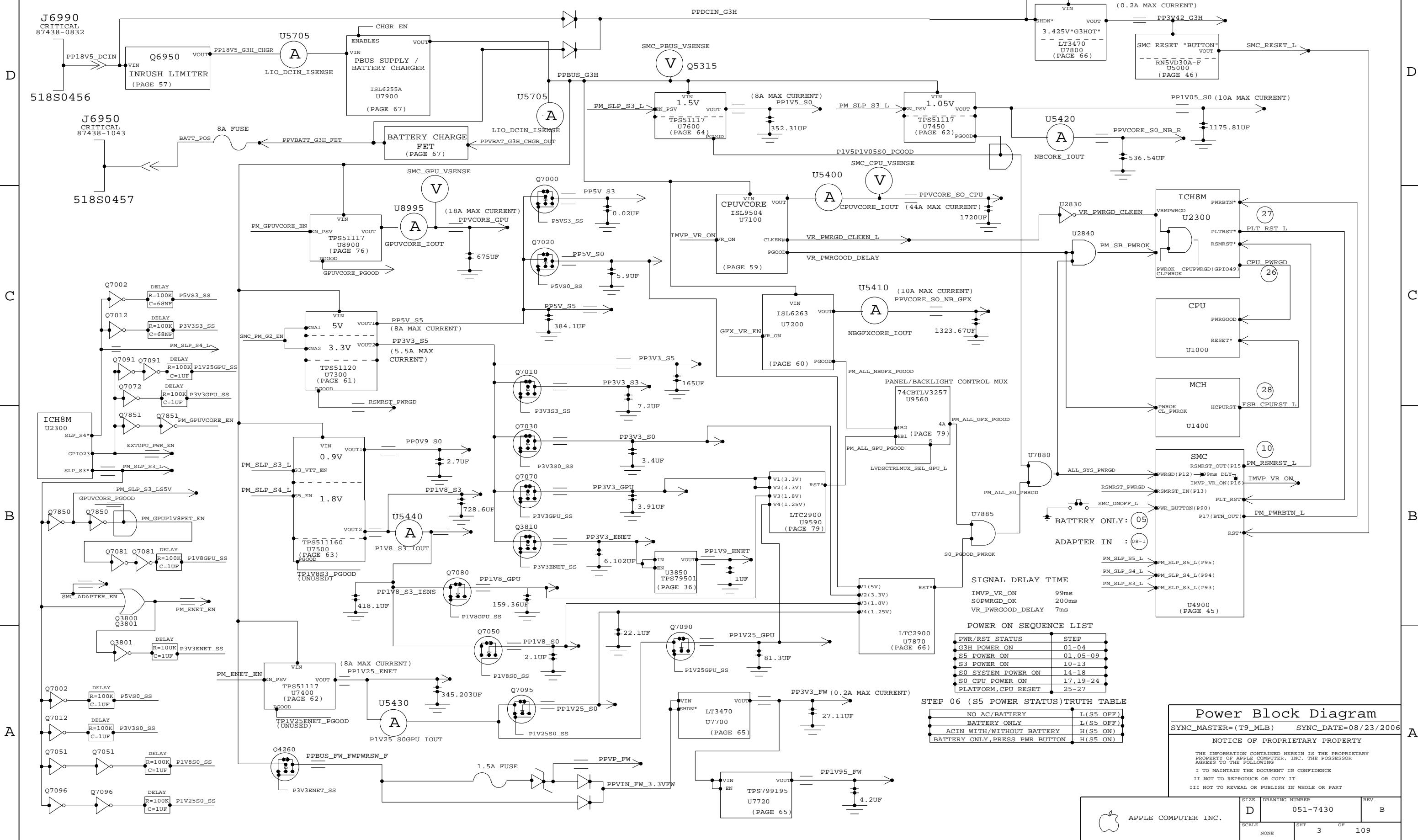
DRAWING NUMBER 051-7430

REV. B

SHT 1 OF 109

www.laptop-schematics.com

M76 POWER SYSTEM ARCHITECTURE



POWER ON SEQUENCE LIST

PWR/RST STATUS	STEP
G3H POWER ON	01-04
S5 POWER ON	01,05-09
S3 POWER ON	10-13
S0 SYSTEM POWER ON	14-18
S0 CPU POWER ON	17,19-24
PLATFORM,CPU RESET	25-27

STEP 06 (S5 POWER STATUS) TRUTH TABLE

NO AC/BATTERY	L(S5 OFF)
BATTERY ONLY	L(S5 OFF)
ACIN WITH/WITHOUT BATTERY	H(S5 ON)
BATTERY ONLY,PRESS PWR BUTTON	H(S5 ON)

Power Block Diagram

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/23/2006

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Power Block Diagram

SYNC_MASTER=N/A

SYNC_DATE=N/A

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APPLE COMPUTER INC.

SIZE
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SIZE	DRAWING NUMBER
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051-7430

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SCALE

NONE

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9048	PCBA, 2.4GHZ, BTR, VRAM-SAM, MBP17	M76_COMMON, CPU_2_4GHZ, FB_256_SAMSUNG, INV_BYPASS, EEE_YRC
630-9047	PCBA, 2.4GHZ, BTR, VRAM-HY, MBP17	M76_COMMON, CPU_2_4GHZ, FB_256_HYNIX, INV_BYPASS, EEE_YRB

M76 BOM Groups

BOM GROUP	BOM OPTIONS
M76_COMMON	COMMON, ALTERNATE, M76_COMMON1, M76_COMMON2, M76_DEBUG, M76_PROGPARTS, ISL6257H
M76_COMMON1	EXTGPU_RST_HW, ISL9504B, LVDS_SEL_RESUME, ONEWIRE_PU, CPU_NTC_A, GPU_XW1
M76_COMMON2	P1V8S3_1V825_GPUFB, SLG2AP101, SMS_MOT_DIS, YUKON_ULTRA, VGA_TERM_CONN
M76_CTO	INV_SPLIT, INV_17INCH
M76_DEBUG	SMC_DEBUG_NO, XDP, LPCPLUS
M76_PROGPARTS	BOOTROM_PROG, SMC_PROG

BOM GROUP	BOM OPTIONS
FB_256_SAMSUNG	VRAM_256, VRAM_SAMSUNG, VRAM_256_SAMSUNG
FB_256_HYNIX	VRAM_256, VRAM_HYNIX, VRAM_256_HYNIX

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:YRC]	CRITICAL	EEE_YRC
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:YRB]	CRITICAL	EEE_YRB

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0388	1	IC, GPU, NV G84M, BGA	U8000	CRITICAL	
338S0432	1	IC, NB, CRESTLINE, GM, CO, PRQ, ROHS-SPECIAL, 965PM	U1400	CRITICAL	
338S0434	1	IC, SB, ICH8M, B1, PRQ, BGA	U2300	CRITICAL	
353S1461	1	IC, ISL9504, SYNC REG CTRL, 2PHAS, QFN48, LF	U7100	CRITICAL	ISL9504A
353S1651	1	IC, ISL9504B, 2PH IMVP6 REG, PMON, QFN48	U7100	CRITICAL	ISL9504B

359S0127	1	IC, 68 PIN, CK505, LOW POWER CLOCK GENER	U2900	CRITICAL	SLG8LP537
359S0130	1	IC, SLG2AP101, LM PWR CLK GEN, CK505, QFN68	U2900	CRITICAL	SLG2AP101
338S0386	1	IC, 88E8058, GIGABIT ENET XCVR, 64P QFN	U3700	CRITICAL	
338S0274	1	IC, SMC, HS8/2116	U4900	CRITICAL	SMC_BLANK
341S2050	1	IC, SMC, DEVELOPMENT, M76	U4900	CRITICAL	SMC_PROG
335S0384	1	IC, 16MBIT 8-PIN SPI SERIAL FLASH, SOIC8	U6100	CRITICAL	BOOTROM_BLANK
341S2002	1	IC, EFI ROM, DEVELOPMENT, M75	U6100	CRITICAL	BOOTROM_PROG

333S0382	4	IC, SGRAM, GDDR3, 16MX32, 700MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_256_SAMSUNG
333S0401	4	IC, SGRAM, GDDR3, 16MX32, 700MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_256_HYNIX
337S3465	1	IC, MDC, SR, E1, PRQ, 2.4G, 35W, 800FSB, 4M, BGA	U1000	CRITICAL	CPU_2_4GHZ

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0011	157S0030		ALL	See alt to TR/BitTech magnetics
152S0476	152S0276		ALL	Inductor alternate
138S0603	138S0602		ALL	Migrate alt to Samsung 2808 4000 4000 4000
353S1681	353S1294		ALL	TV alternate to National
376S0543	376S0466		ALL	See alternate to SAMSUNG 2808 4000 4000 4000
376S0526	376S0451		ALL	Palcohol PRIMER altmate to 1007707

APPLE COMPUTER INC.

SIZE

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DRAWING NUMBER

051-7430

REV.

B

SCALE

NONE

SHT

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OF

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BOM Configuration

SYNC_MASTER=N/A

SYNC_DATE=N/A

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SYNC_MASTER=N/A

SYNC_DATE=N/A




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	8	7	6	5	4	3	2	1																																						
D	<div>DVT</div> <div>13.1.0:</div> <div>3/05/07 -- Integrated m75/mlb pages 22,25,28,30-32,50,53-55,72,74,76,78,80-82,84-90,94,95 through:</div> <div>Change 46833 by cerickso@m75_mlb_051-7225_12.5.0_tmp.Ecad on 2007/03/02 09:49:13</div> <div>Changes since previous major release (12.3.0):</div> <div>- LVDS Connector: Changed pin 5 of connector from NC to PP3V3_SW_LCD (in case we add extra cable for power - rdar://5024882)</div> <div>- NB GFX Decoupling: Added R2260 (0.3 ohm, 0603) to bring ESR of regulator output cap in spec (rdar://5000272)</div> <div>Changes since previous major release (12.2.0):</div> <div>- Left Clutch IC: Updated both I-PEX connectors to new APN (part update for shell plating)</div> <div>- NB GFX Core: Changed Vcore controller to ISL6263B (part consolidation effort between Apple/Intersil - rdar://5009109)</div> <div>- Power Supplies: Replaced APN 152S0511 with 152S0368 (duplicate APNs for same part - rdar://5009109)</div> <div>- Thermal Sensors: Updated topology of EMC1033 sensors (removed shorts, changed connector caps to 18pF)</div> <div>- NB GFX Decoupling/Power Aliases: Connected VCCD_CRT of NB to GND per CRT disable guidelines</div> <div>Changes since previous bom release (12.0.0):</div> <div>- GPU FB: Changed cal resistors per NVidia PUN (R8290 to 45.3 ohm and R8291 to 24.9 ohm)</div> <div>- GPU FB: Changed unterminated-mode reference voltage to 40% (R8297 -> 1.02k, R8432/82, R8532/82 -> 2.21K)</div> <div>- Power Sequencing: Removed U7885/C7885 to take GFX_PGOOD out of PWR_OK chain (rdar://4974927)</div> <div>- GPU Vcore: NO STUFFed all PWRCTL related components (feature not to be supported)</div> <div>- GPU Vcore: Updated voltage setpoints to 1.000/1.070/1.125V</div> <div>- SB GPIOs: Sync'd page25.csa to T9_MLB to get pullup updates</div> <div>- Thermal Sensors: Updated topology of EMC1033 filter caps (added C5515 next to IC, moved other caps to connectors)</div> <div>3/5/07 -- Added GPU Vcore VFB resistor BOM table and GCORE_M76 BOM Option to M76_COMMON BOM group.</div> <div>3/5/07 -- Removed RX3920-RX3927.</div> <div>3/5/07 -- FireWire: Changed to Rev C of TI FireWire MCM (APN: 338S0435)</div> <div>3/5/07 -- ODD Conn: Changed ODD power FET to FDC606P (from FDC638P) for reduced Rds(on)</div> <div>3/5/07 -- Changed 1.8V supply feedback resistors R7520 to 21.5K 0.1% and R7521 15.0K 0.1%.%</div> <div>13.2.0</div> <div>3/07/07 -- Integrated m75/mlb pages 25,42,70 through:</div> <div>Change 47192 by cerickso@m75_mlb_051-7225_12.7.0_tmp.Ecad on 2007/03/06 18:36:54</div> <div>Changes since previous major release (12.6.0):</div> <div>- FireWire Ports: Changed D4260 to PDS540 for higher current capacity</div> <div>- SB GPIOs: Changed R2514 from pulldown to pulldown to correct auto power-on issue (Linda card detect GPIO)</div> <div>3/07/07 -- Q7080 PP1V8_GPU FET changed for lower Rds on from FDM6296 to RJK0301DPB</div> <div>13.3.0</div> <div>3/08/07 -- Removed =PP1V5_S0_NB_VCCD_CRT alias to PP1V5_S0 since VCCD_CRT is GNDed per CRT disable guidelines.</div> <div>3/08/07 -- Battery charge current limit circuit changes.</div> <div>3/08/07 -- Changed R9811 from 15.0K to 14.0K. This is so that M57 inverter and split inverter can use same backlight table.</div> <div>3/08/07 -- Changed R9950 from 220K to NOSTUFF to improve current and voltage asymmetry ratio.</div> <div>3/08/07 -- Changed BOM option on R9960 511K from NOSTUFF to INV_SPLIT to improve current and voltage asymmetry ratio.</div> <div>3/08/07 -- Integrated CSA pg. 55 through:</div> <div>Change 47450 by cerickso@m75_mlb_051-7225_12.8.0_tmp.Ecad on 2007/03/08 10:49:26</div> <div>Changes since previous major release (12.7.0):</div> <div>- Thermal Sensors: Added R5515/R5516 in case low pass filter is needed for EMC1033</div> <div>3/08/07 -- Integrated CSA pg. 79 through:</div> <div>Change 47440 by xyang@m75_lio_051-7226_7.9.0_tmp.Ecad on 2007/03/08 10:25:46</div> <div>Changed Charger PWM limit resistor according to MARC K.'S M70 values</div> <div>13.4.0</div> <div>3/12/07 -- Added BOM option P1V8S3_1V825 to M76_COMMON2 BOM group.</div> <div>3/12/07 -- Modified R7520 and R7521 to use symbols for 0.1% resistors.</div> <div>Removed OMIT BOM option from R7521.</div> <div>Changed BOM options for R7520 to choose between 1.8V or 1.825V 0.1% resistors.</div> <div>14.0.0</div> <div>3/14/07 -- Removed BOM option for HDCP as feature is removed.</div> <div>3/14/07 -- Moved =PP1V8_GPU_P1V8GPUFET from PP1V8_S3_ISNS to PP1V8_S3. This is to remove the current sense resistor from the GPU 1.8V path.</div> <div>Cleaned up unused aliases.</div> <div>3/14/07 -- Constraints: Constrained WWAN_SIM signals to 50 ohms</div> <div>3/14/07 -- Integrated m75/mlb CSA pages 55 & 78 through:</div> <div>Change 48122 by cerickso@cerickso_m75.Ecad on 2007/03/14 15:27:36</div> <div>- Thermal Sensors/Aliases: Changed mounting pads of Th2H sensor connector to left clutch chassis gnd</div> <div>- Power Control: Corrected alias connections for 5V/3V3 S5 enable signals</div> <div>14.1.0</div> <div>3/14/07 -- Moved =PP1V8_S0_P1V8S0FET from PP1V8_S3_ISNS to PP1V8_S3.</div> <div>14.2.0</div> <div>3/15/07 -- Changes to low voltage inverter for M76 piezo.</div> <div>14.5.0</div> <div>3/19/07 --</div> <div>Integrated m75/mlb CSA pgs. 28,30-32,50,53-55,80-82,84-88,90,94,95 through:</div> <div>Change 48405 by cerickso@m75_mlb_051-7225_13.3.0_tmp.Ecad on 2007/03/16 12:18:46</div> <div>Changes since previous major release (13.2.0):</div> <div>- Thermal Sensors: Moved remote sensor U5500 to SMC SMBus A and S3 power rail to clear I2C addr clash</div> <div>3/19/07 --Integrated t9/mlb_noME CSA pgs. 15 & 38 through:</div> <div>Change 48372 by wferry@wferry_projects.Ecad on 2007/03/16 09:11:01</div> <div>Quick submit of T9 noME branch. Major release will follow once changes are properly documented in Radar and revision history.</div> <div>Page 15: Sync from main-line (renamed LVDS_VREFx nets).</div> <div>Page 38: Changed Yukon crystal load caps to 18pF per radar://4946795 (really radar://4945362).</div> <div>3/19/07 -- Added OMIT BOM option to L4731 and L4741.</div> <div>3/19/07 -- Added BOM table with 0 Ohm 0603 resistors at L4731,L4741.</div> <div>3/19/07 -- SMBus: moved Remote Temps from SMC B to SMC A in order to use EMC1043-5.</div> <div>3/19/07 --</div> <div><rdar://problem/5070179> BOM update: boost circuit open causes MLB & SIMM damage (see 5064997)</div> <div>Deleted R7364 and made C7364 0603 size, still 0.1uF (132S0100).</div> <div>Deleted R7420 and R7470 and made C7420 and C7470 0603 size, still 0.1uF (132S0100).</div> <div>Deleted R7525 and made C7525 0805 size, still 0.1uF (132S0201).</div> <div>Deleted R7615 and made C7615 0603 size, still 0.1uF (132S0100).</div> <div>Deleted R8915 and made C8915 0603 size, still 0.1uF (132S0100).</div> <div>3/19/07 -- Changes to low voltage inverter for M76 piezo.</div> <div>L9950 changed from 152S0527 (15uH, 2.8A, 115mOhm) to 152S0585 (22uH, 2.8A, 129mOhm).</div> <div>14.6.0</div> <div>3/19/07 -- Integrated m75/mlb CSA pgs. 55 & 78 through:</div> <div>Change 48590 by cerickso@m75_mlb_051-7225_13.4.0_tmp.Ecad on 2007/03/19 14:26:14</div> <div>Changes since previous major release (13.3.0):</div> <div>- Thermal Sensors: Updated U5500 power alias to indicate device should be on S3 rail</div> <div>- Power Control: Added U7858 to level shift PM_G2_EN to 3.42V to 5V</div> <div>3/19/07 -- Updated SMC A SMBus information for Left I/O Board and Top-Case.</div> <div>3/19/07 -- Deleted R7324 and made C7324 0603 size, still 0.1uF (132S0100).</div> <div>14.7.0</div> <div>3/19/07 -- Added three 0603 0 ohm resistors R4740-R4742 for EMC return current path.</div> <div>3/19/07 -- Battery charge current limit circuit changes for max charge current of 4.5A.</div> <div>3/19/07 -- Integrated m75/mlb CSA pgs. 22 & 78 through:</div> <div>Change 48660 by cerickso@m75_mlb_051-7225_13.5.0_tmp.Ecad on 2007/03/19 20:17:1 Changes since previous major release (13.4.0):</div> <div>- Power Control: Tied all 4 5V/3.3V enables (EN1, EN2, EN3 and EN5) together as part of PM_G2_EN</div> <div>14.8.0</div> <div>3/21/07 -- Integrated m75/mlb CSA pgs. 84,85 & 89 through:</div> <div>Change 48885 by cerickso@m75_mlb_051-7225_14.0.0_tmp.Ecad on 2007/03/20 21:27:14</div> <div>This fab release is for DVT!</div> <div>Changes since previous major release (13.5.0):</div> <div>- GPU Vcore: Updated setpoints for GPU Vcore based upon Nvidia Vmin (i.e. 1.05V, 1.05V, 1.05V, 1.125V)</div> <div>- FB: Changed FB VREF caps to 2x0.0047uF as required by Nvidia PUN 02736-001-v07 (which requests 1x0.01uF)</div> <div>3/21/07 -- <rdar://problem/4838347> EMC - M76 MLB changes</div> <div>Change BOM option on L4764 to OMIT and added BOM table entry for 0 ohm resistor at L4764.</div> <div>3/21/07 -- <rdar://problem/5073301> M76: Change GPU Vmin</div> <div>Changed resistors for M76 Vcore setpoints (i.e. 1.05V, 1.05V, 1.125V, 1.25V)</div> <div>Removed NOSTUFF BOM option from R8924.</div> <div>Changed R8924 to 28K.</div> <div>Changed R8925 to 16.9K.</div> <div>Changed table text notes.</div> <div>3/22/07 -- Items relating to <rdar://problem/5061583> Task: Current Surge When Insert Battery Without AC Plugged-In</div> <div>3/22/07 -- Added D7903 for voltage ripple on ISL6257 BOOT and PHASE pins.</div> <div>3/22/07 -- Added Q7970 for potential battery inrush current.</div> <div>15.0.0</div> <div>3/26/07 -- Removed C7930 and R7903 for space reasons.</div> <div>15.2.0</div> <div>3/28/07 -- Change BOM option for 1.8V regulator feedback to 1.8V GPU FET input.</div> <div>3/28/07 -- Added XW7580 and R7580 for option to tie 1.8V S3 regulator feedback point to input of 1.8V GPU FET.</div> <div>3/28/07 -- Integrated m75/mlb CSA pg. 87 through</div> <div>Change 49919 by cerickso@cerickso_m75.Ecad on 2007/03/28 14:28:29</div> <div>Changes since previous fab release (14.0.0):</div> <div>- GPU Straps: Added PCI_DEVID<3..0> pullup straps</div> <div>15.3.0</div> <div>3/29/07-- Moved XW7580 to XW0980, and R7580 to R0980.</div> <div>15.4.0</div> <div>3/31/97 -- Changed C9950 from 22uF to 10uF for acoustic noise per Flo Kim.</div> <div>3/31/97 --Added C9951 B2 case size as placeholder for new cap for acoustic noise per Flo Kim.</div>																																													
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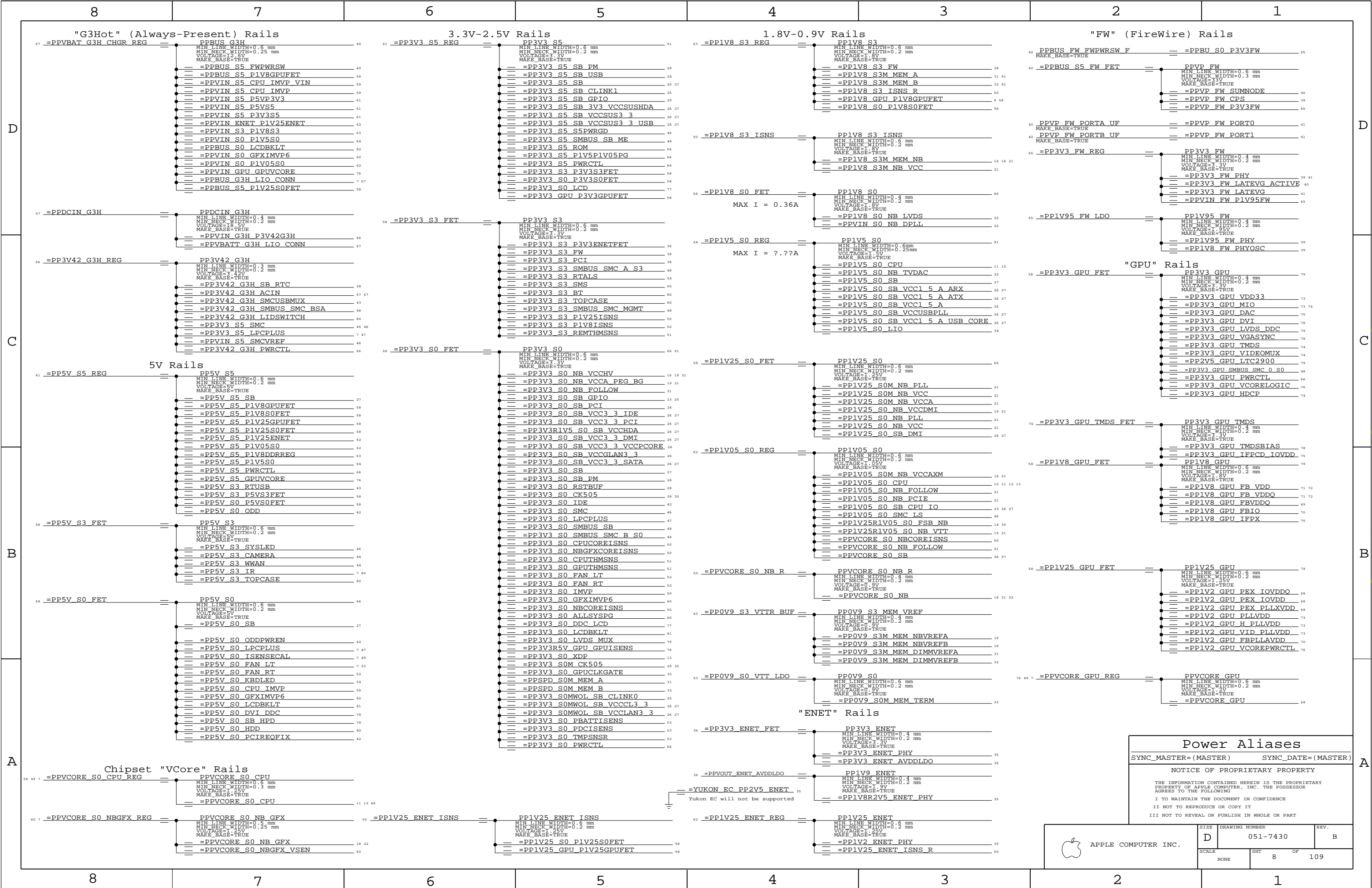
NONE

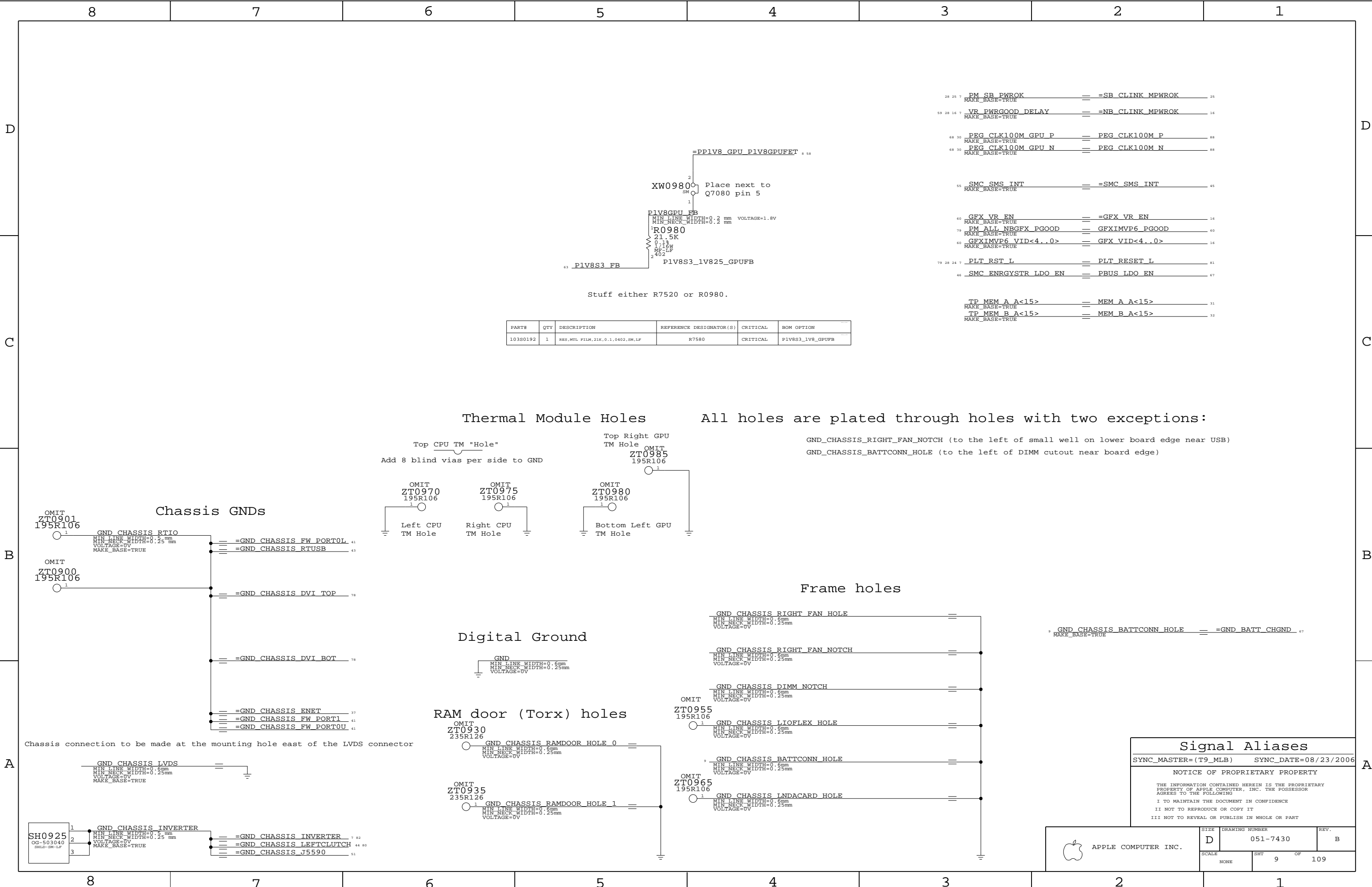
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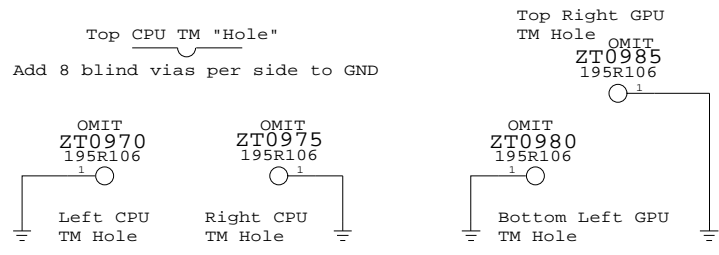




PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
103S0192	1	RES,MTL FILM,21K,0.1,0402,SM,LF	R7580	CRITICAL	P1V8S3_1V8_GPUFB

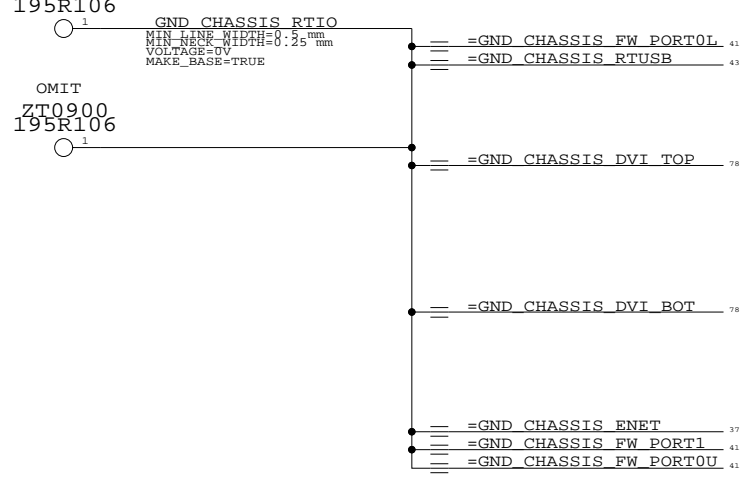
Thermal Module Holes

All holes are plated through holes with two exceptions:

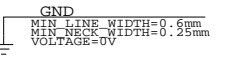


GND_CHASSIS_RIGHT_FAN_NOTCH (to the left of small well on lower board edge near USB)
GND_CHASSIS_BATTCONN_HOLE (to the left of DIMM cutout near board edge)

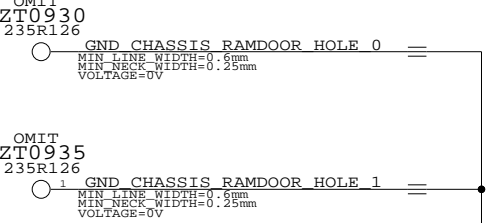
Chassis GNDS



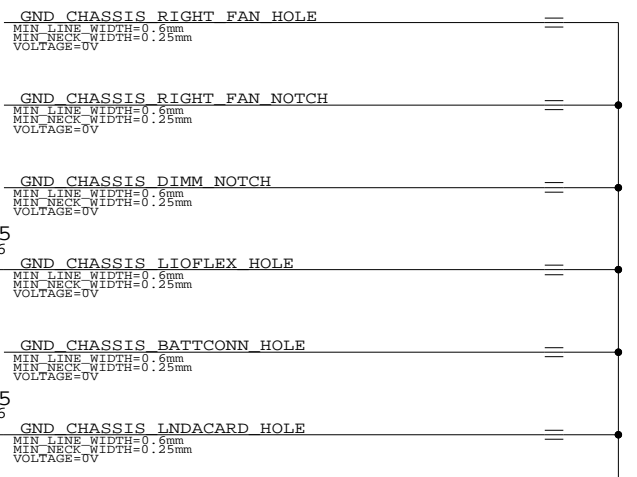
Digital Ground



RAM door (Torx) holes

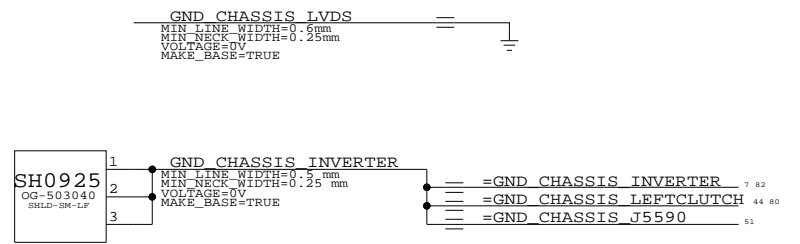


Frame holes



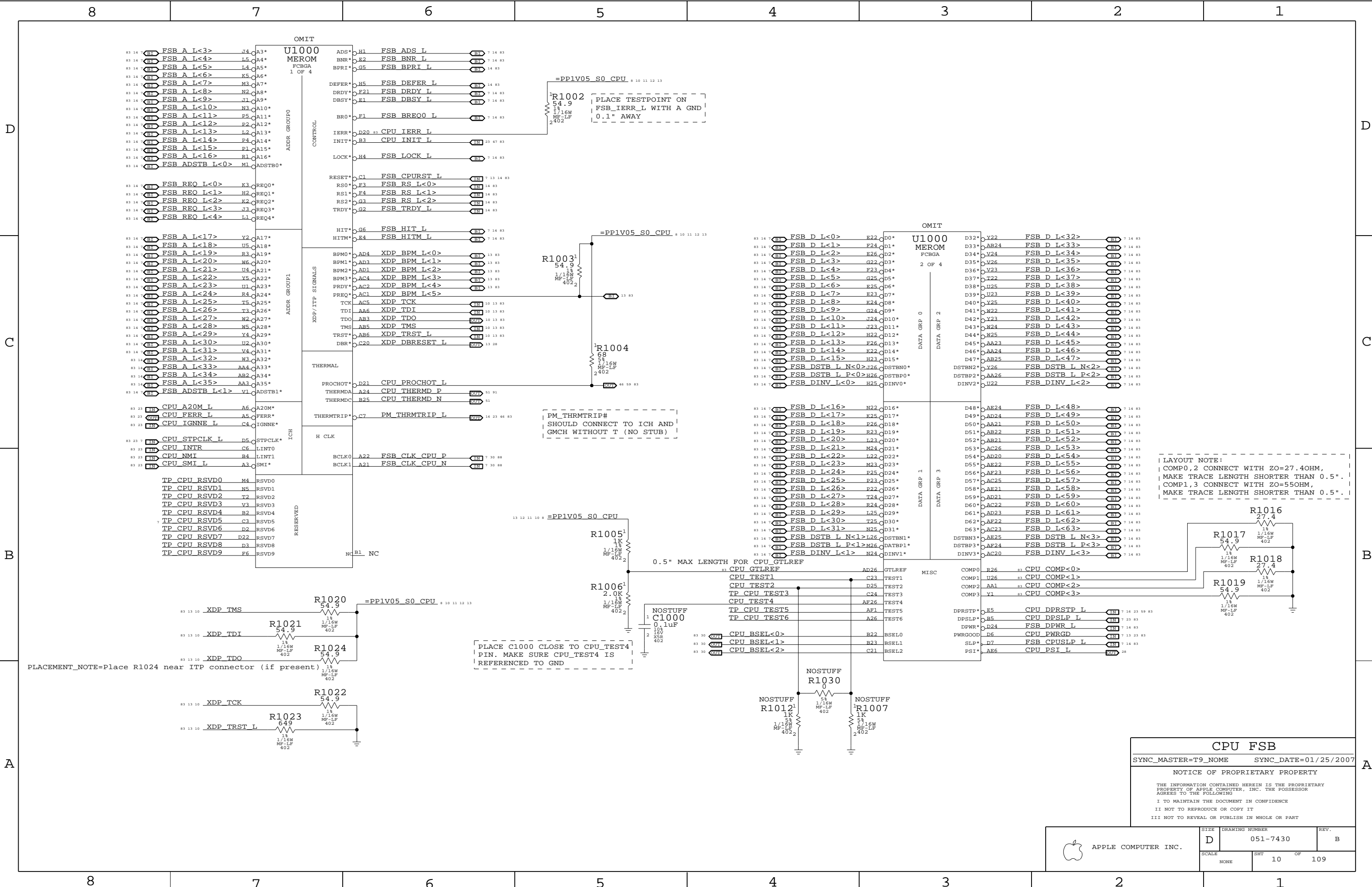
GND_CHASSIS_BATTCONN_HOLE == GND_BATT_CHGND

Chassis connection to be made at the mounting hole east of the LVDS connector

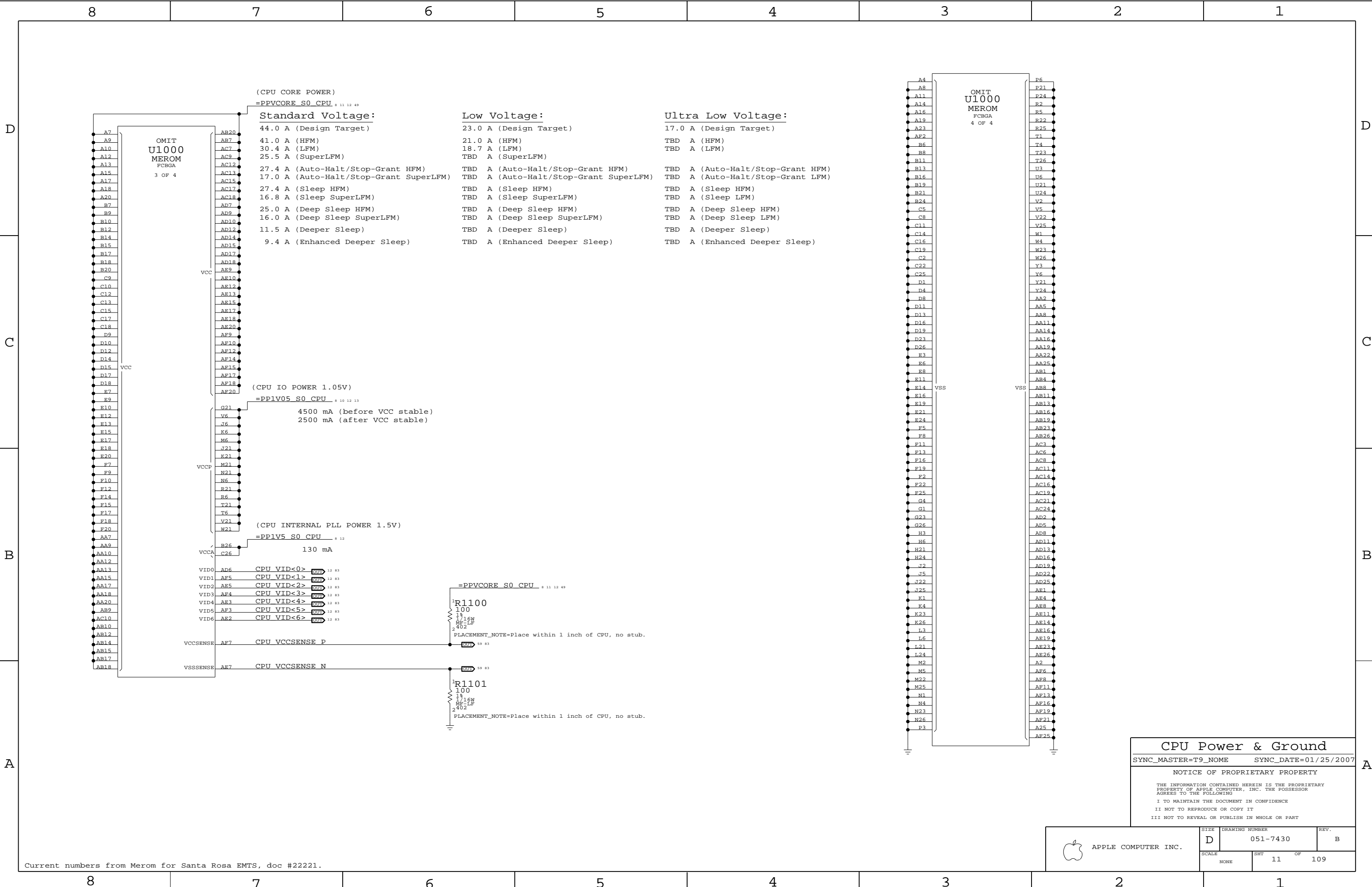


Signal Aliases		
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CPU FSB
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(CPU CORE POWER)

=PPVCORE_S0_CPU_8 11 12 49

Standard Voltage:

- 44.0 A (Design Target)
- 41.0 A (HFM)
- 30.4 A (LFM)
- 25.5 A (SuperLFM)
- 27.4 A (Auto-Halt/Stop-Grant HFM)
- 17.0 A (Auto-Halt/Stop-Grant SuperLFM)
- 27.4 A (Sleep HFM)
- 16.8 A (Sleep SuperLFM)
- 25.0 A (Deep Sleep HFM)
- 16.0 A (Deep Sleep SuperLFM)
- 11.5 A (Deeper Sleep)
- 9.4 A (Enhanced Deeper Sleep)

Low Voltage:

- 23.0 A (Design Target)
- 21.0 A (HFM)
- 18.7 A (LFM)
- TBD A (SuperLFM)
- TBD A (Auto-Halt/Stop-Grant HFM)
- TBD A (Auto-Halt/Stop-Grant SuperLFM)
- TBD A (Sleep HFM)
- TBD A (Sleep SuperLFM)
- TBD A (Deep Sleep HFM)
- TBD A (Deep Sleep SuperLFM)
- TBD A (Deeper Sleep)
- TBD A (Enhanced Deeper Sleep)

Ultra Low Voltage:

- 17.0 A (Design Target)
- TBD A (HFM)
- TBD A (LFM)
- TBD A (Auto-Halt/Stop-Grant HFM)
- TBD A (Auto-Halt/Stop-Grant LFM)
- TBD A (Sleep HFM)
- TBD A (Sleep LFM)
- TBD A (Deep Sleep HFM)
- TBD A (Deep Sleep LFM)
- TBD A (Deeper Sleep)
- TBD A (Enhanced Deeper Sleep)

OMIT
U1000
MEROM
FCBGA
4 OF 4

CPU Power & Ground

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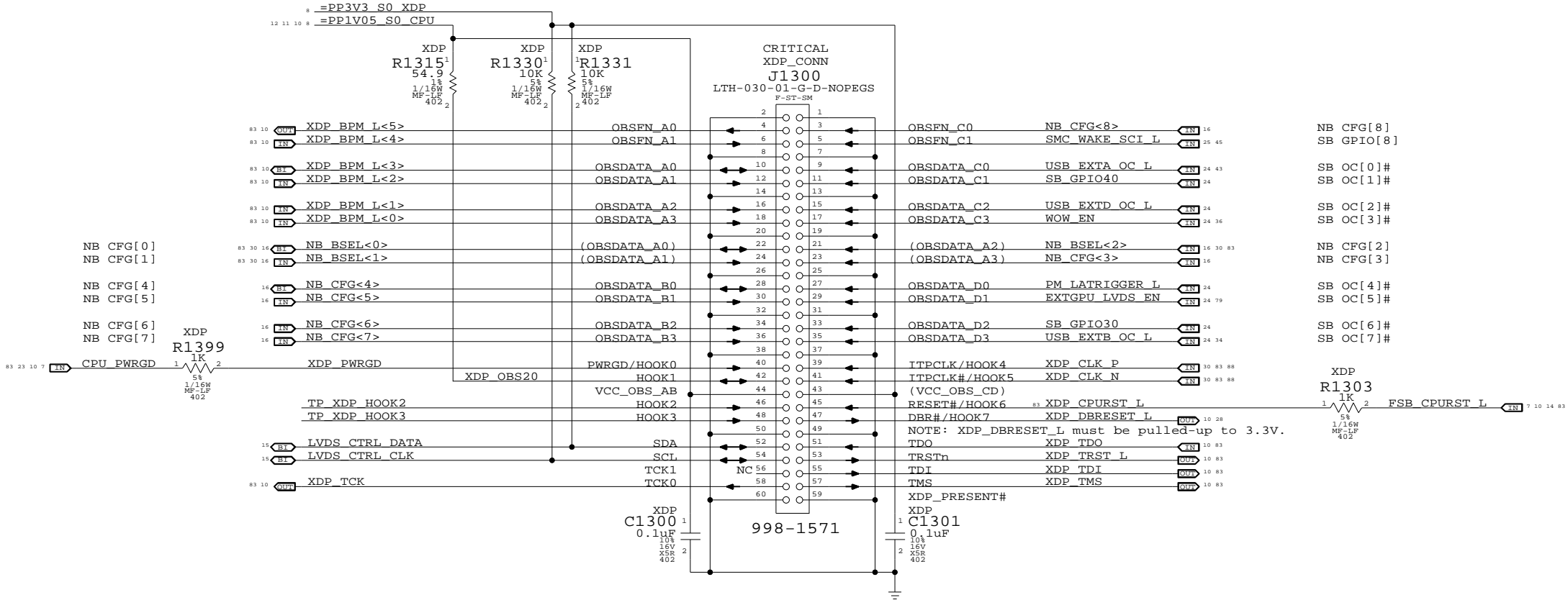
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Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with 920-0451 adapter board to support CPU, NB & SB debugging.



Direction of XDP module

Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port (XDP)

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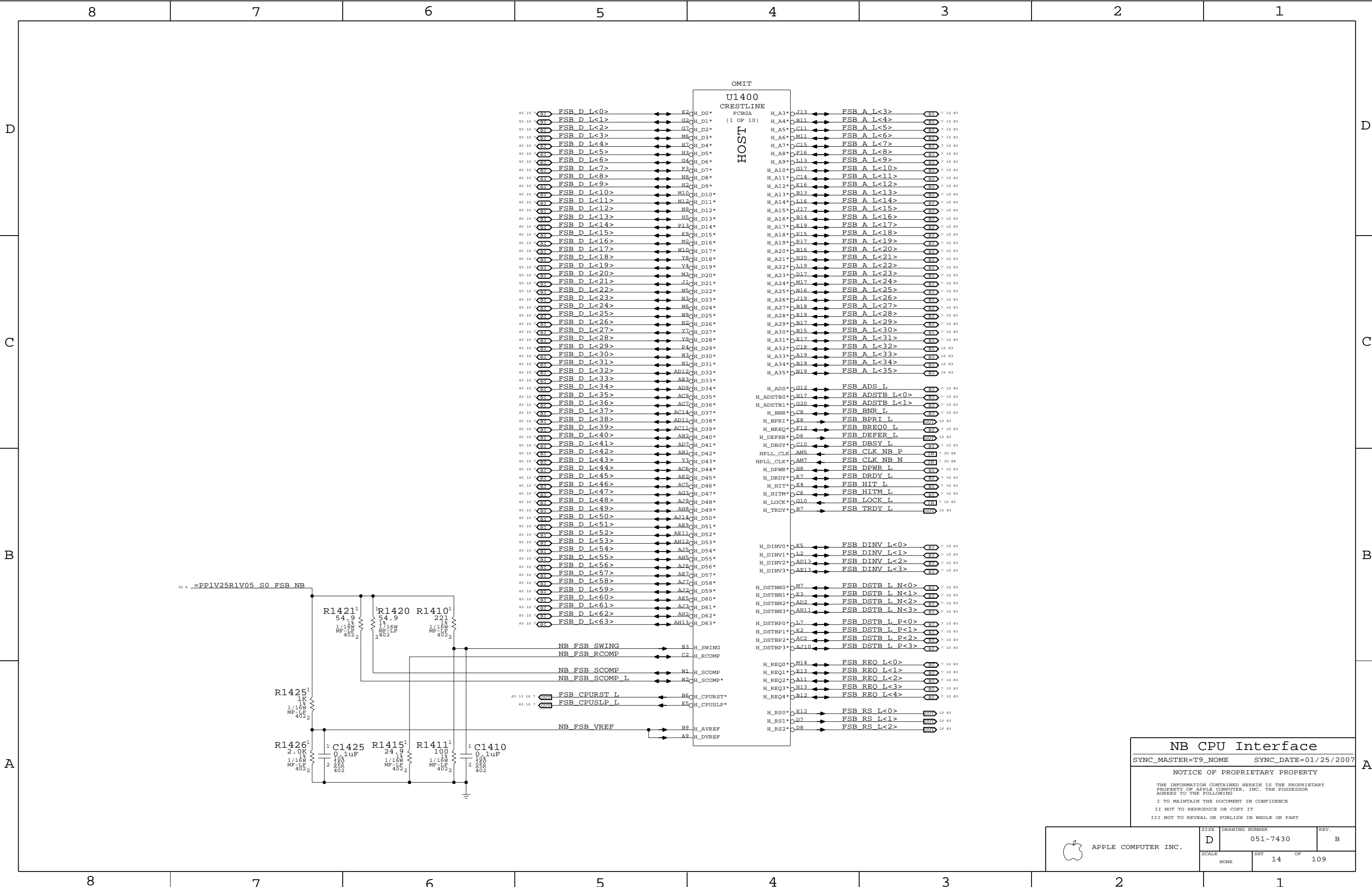
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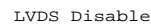
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NB CPU Interface		
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Can leave all signals NC if LVDS is not implemented.
Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

Note: SR DG says to tie LVDS_VREFH/L to GND. This causes a glitch during wake-up on LVDS DATA/CLK pairs. New recommendation is to float both signals, see Radar #5067636.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

CRT & TV-Out Disable

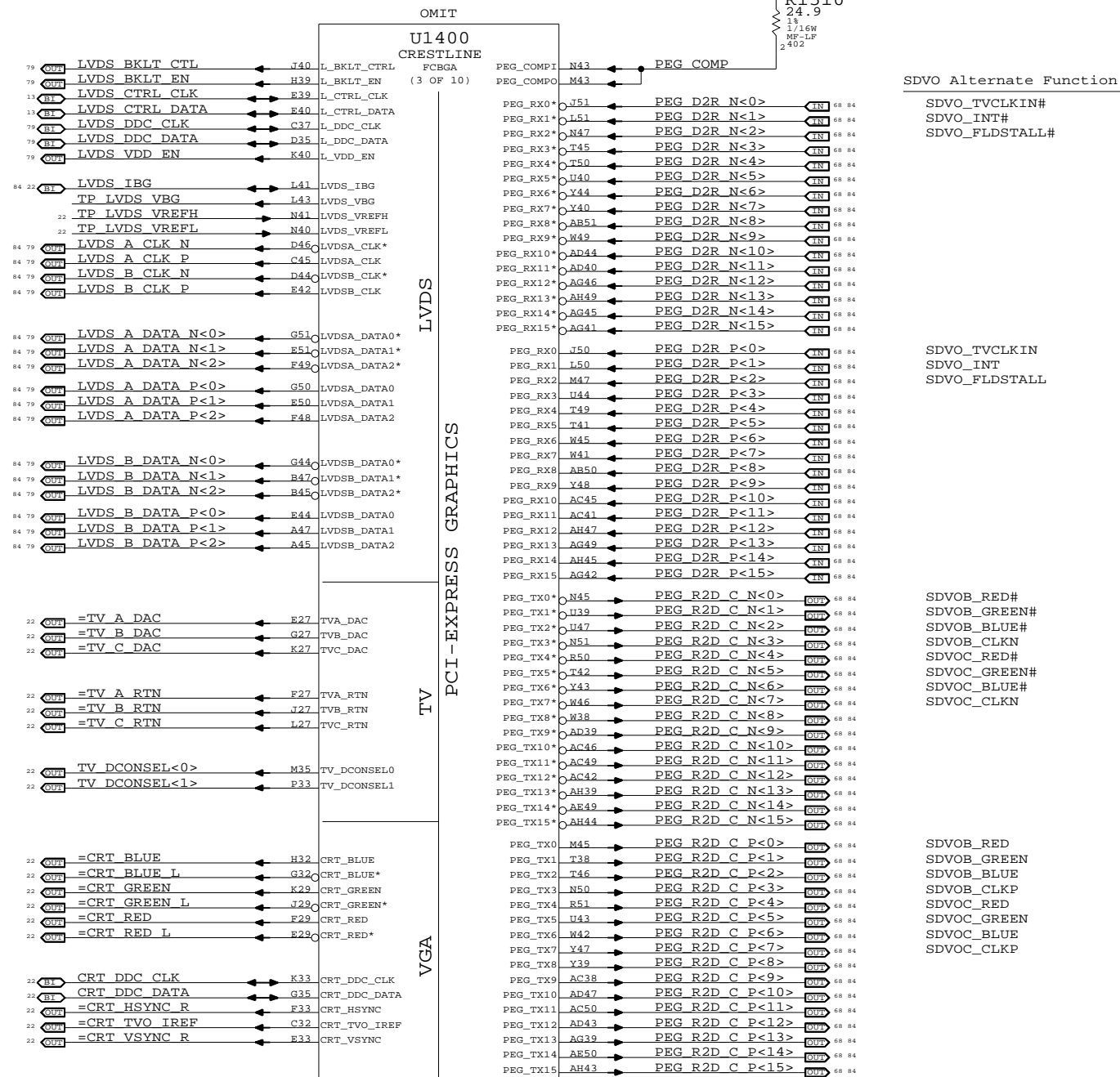
Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TVO_IREF to GND.
Can tie the following rails to GND:
VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC,
VCCD_CRT, VCCD_QDAC and VCC_SYNC.

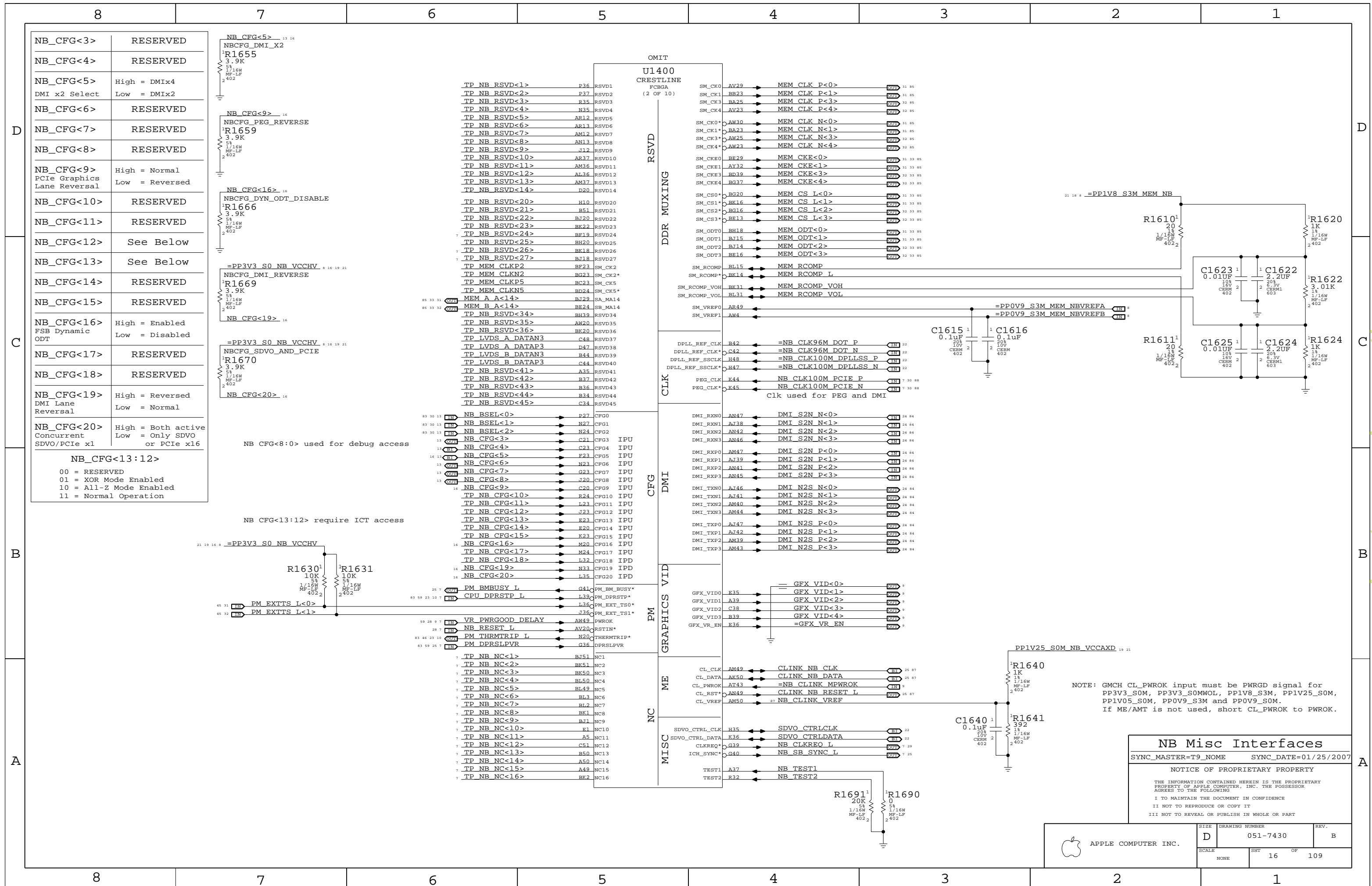
NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

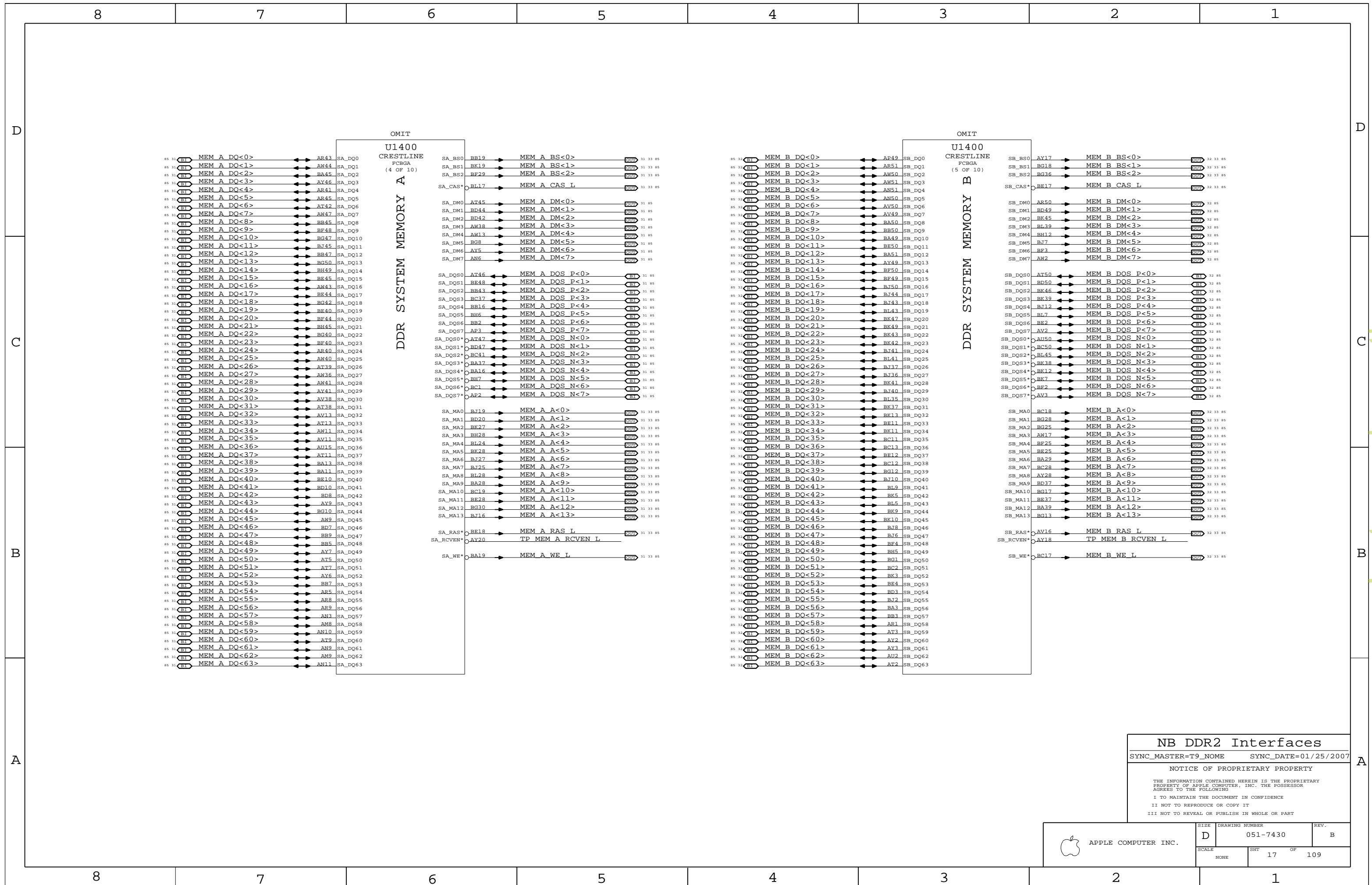
Internal Graphics Disable

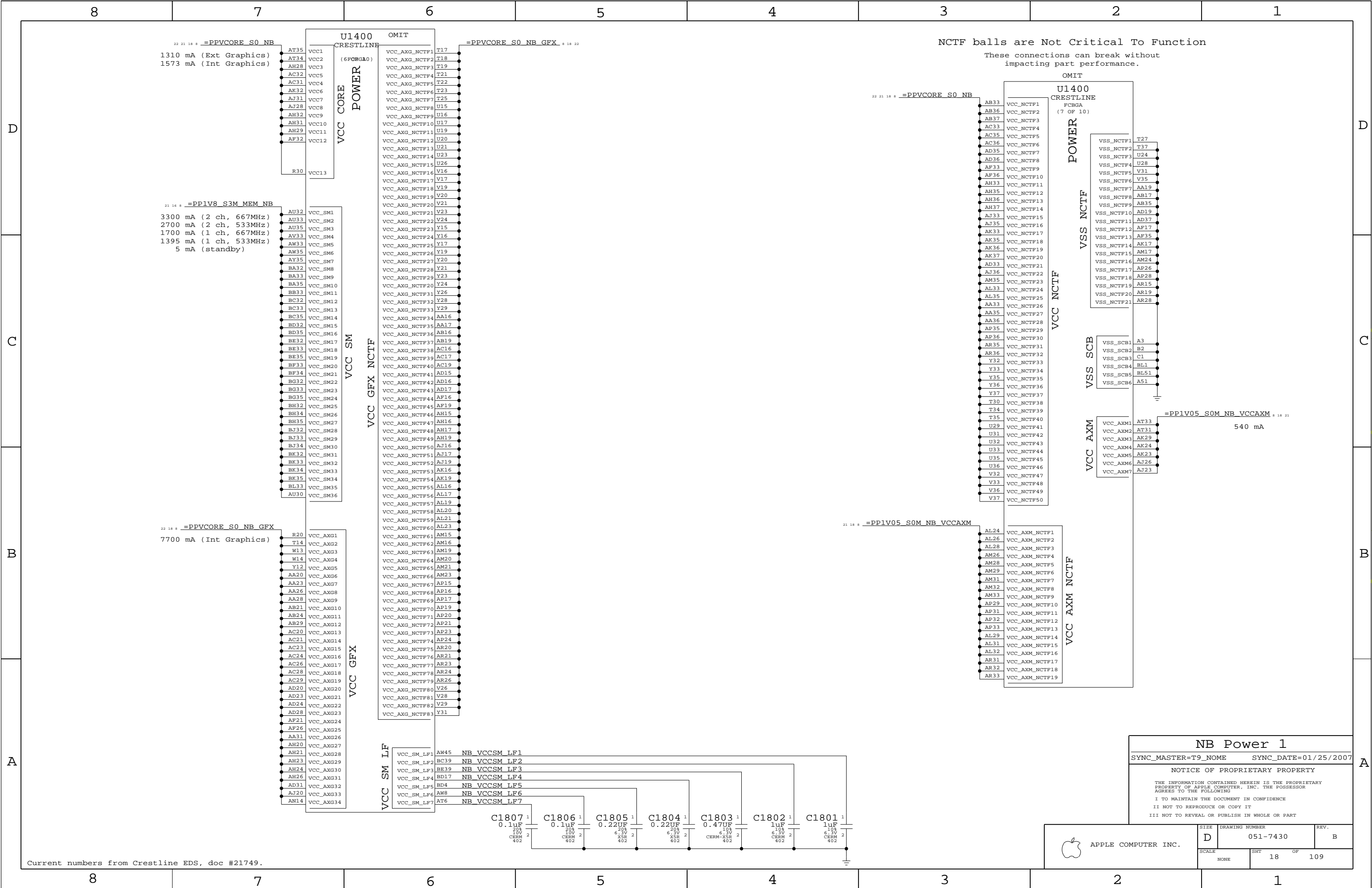
Follow instructions for LVDS and CRT & TV-Out Disable above.
Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and
TV_DCONSELx to GND.

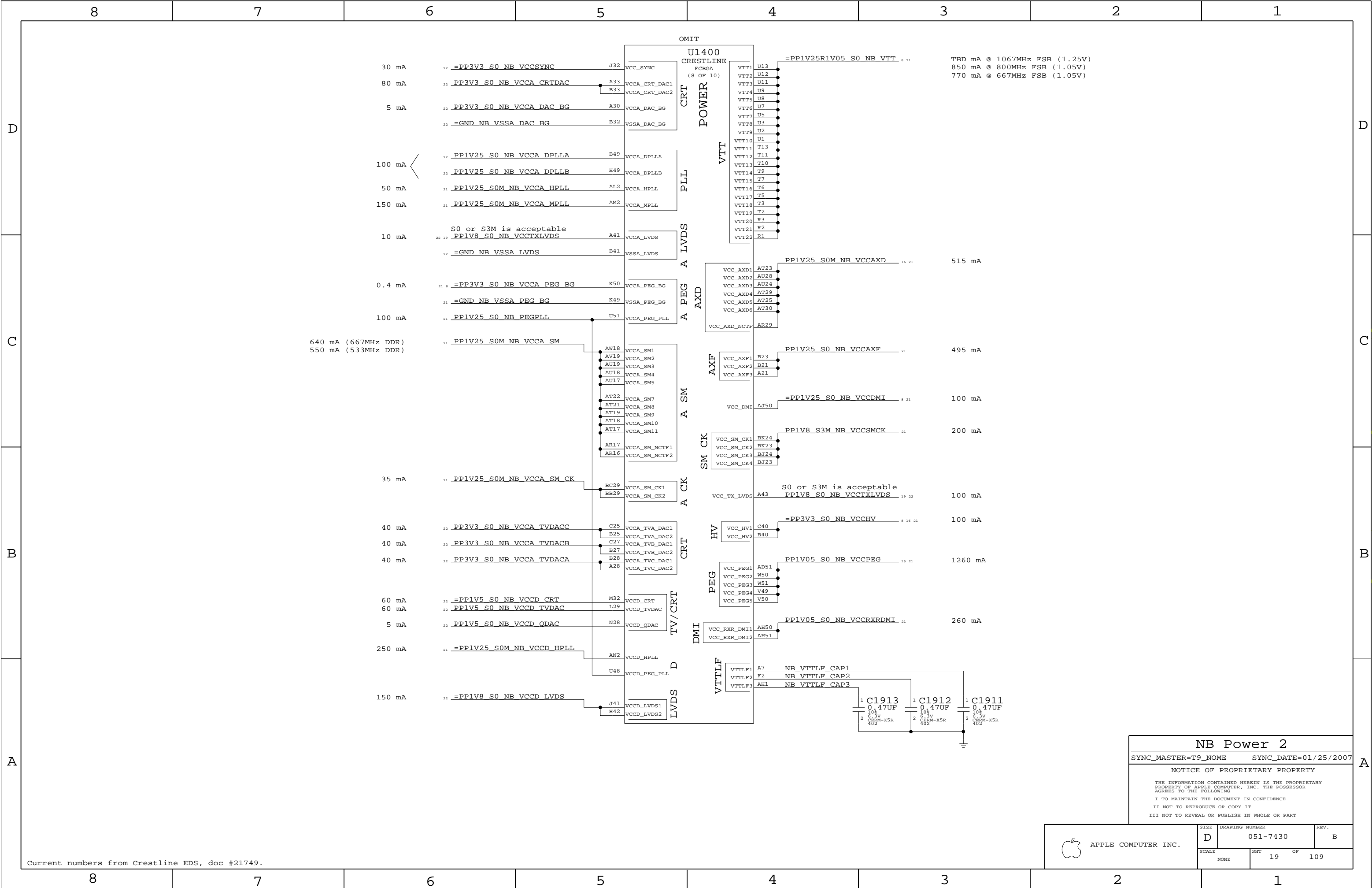
Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
Tie VCCA_DPLL and VCCA_DPLLB to VCC (VCore).
Tie VCCA_AXG and VCCA_AXG_NCTF to GND.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.











NB Power 2

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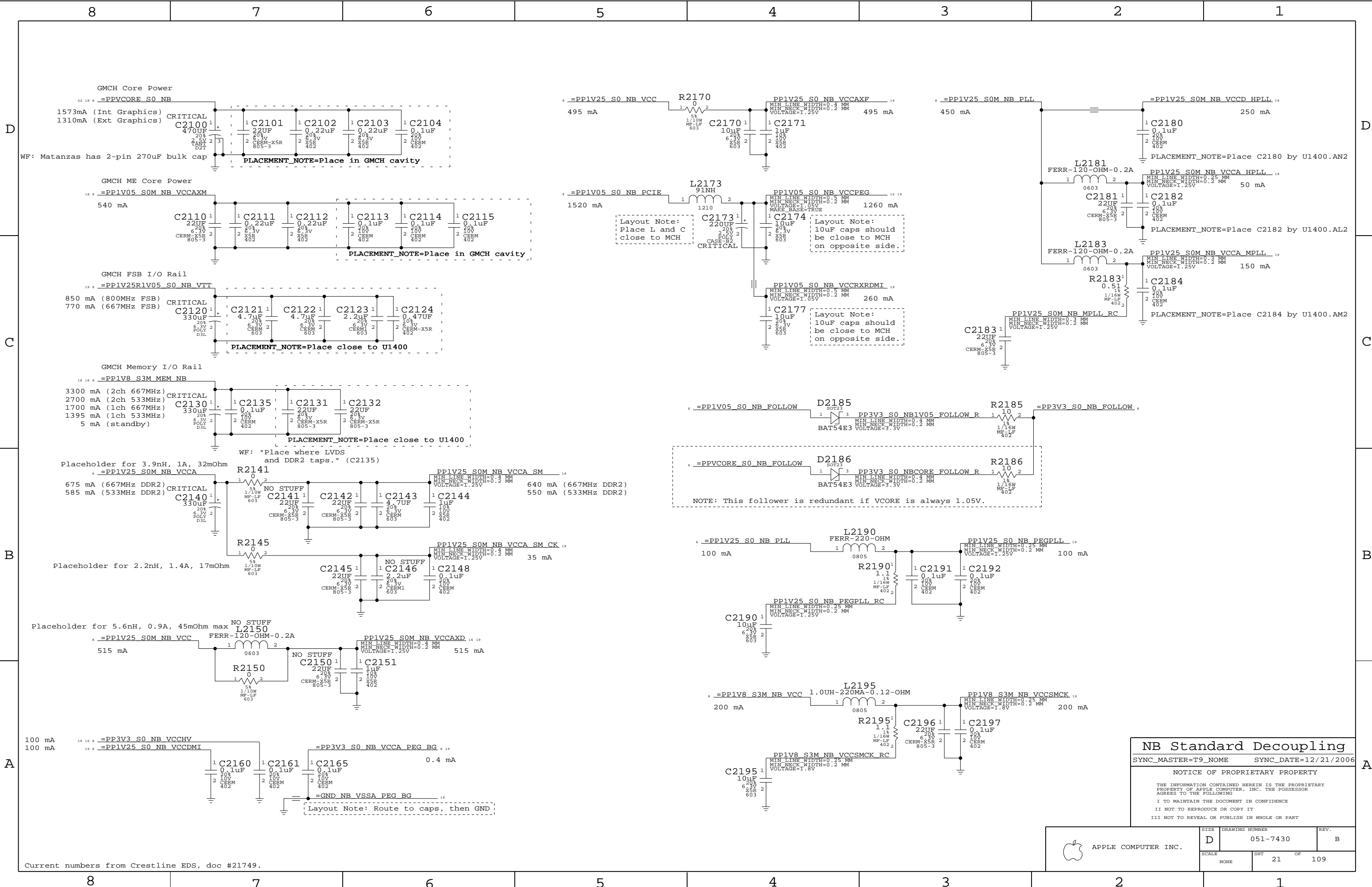
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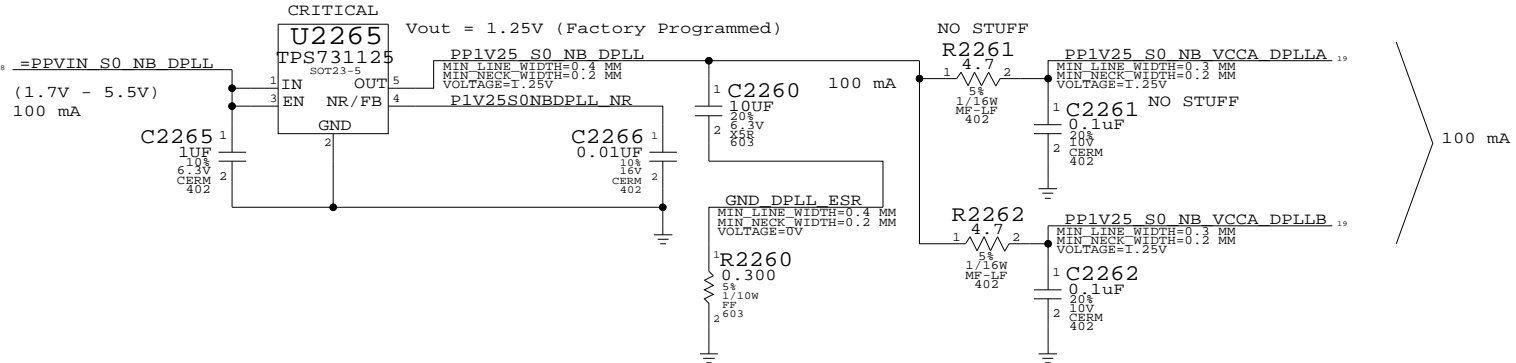
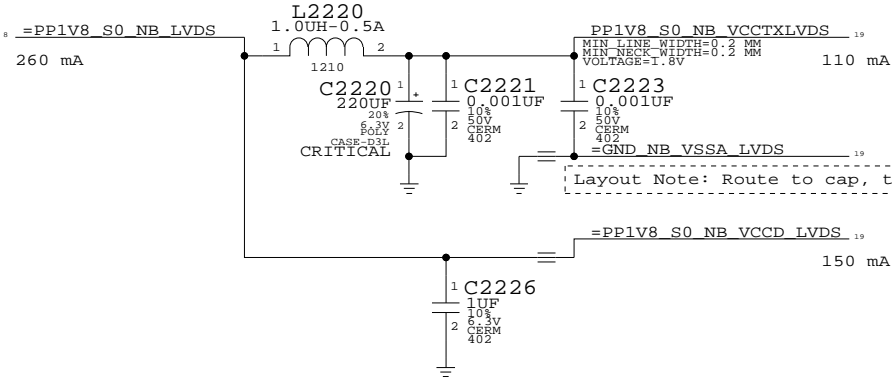
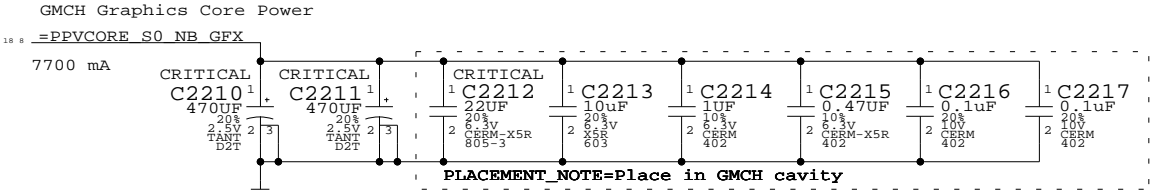
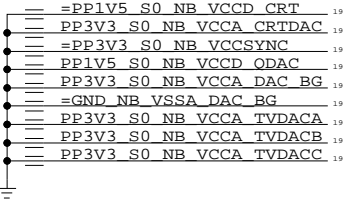
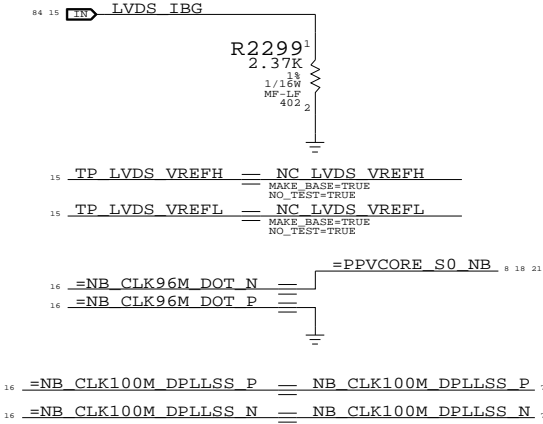
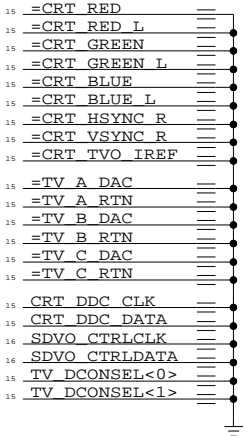
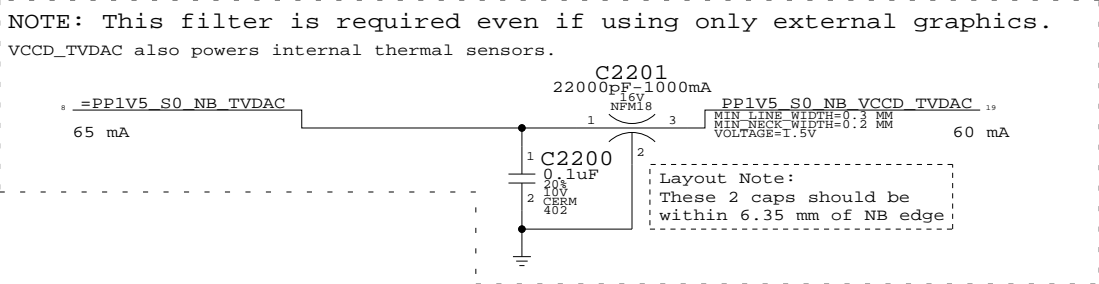
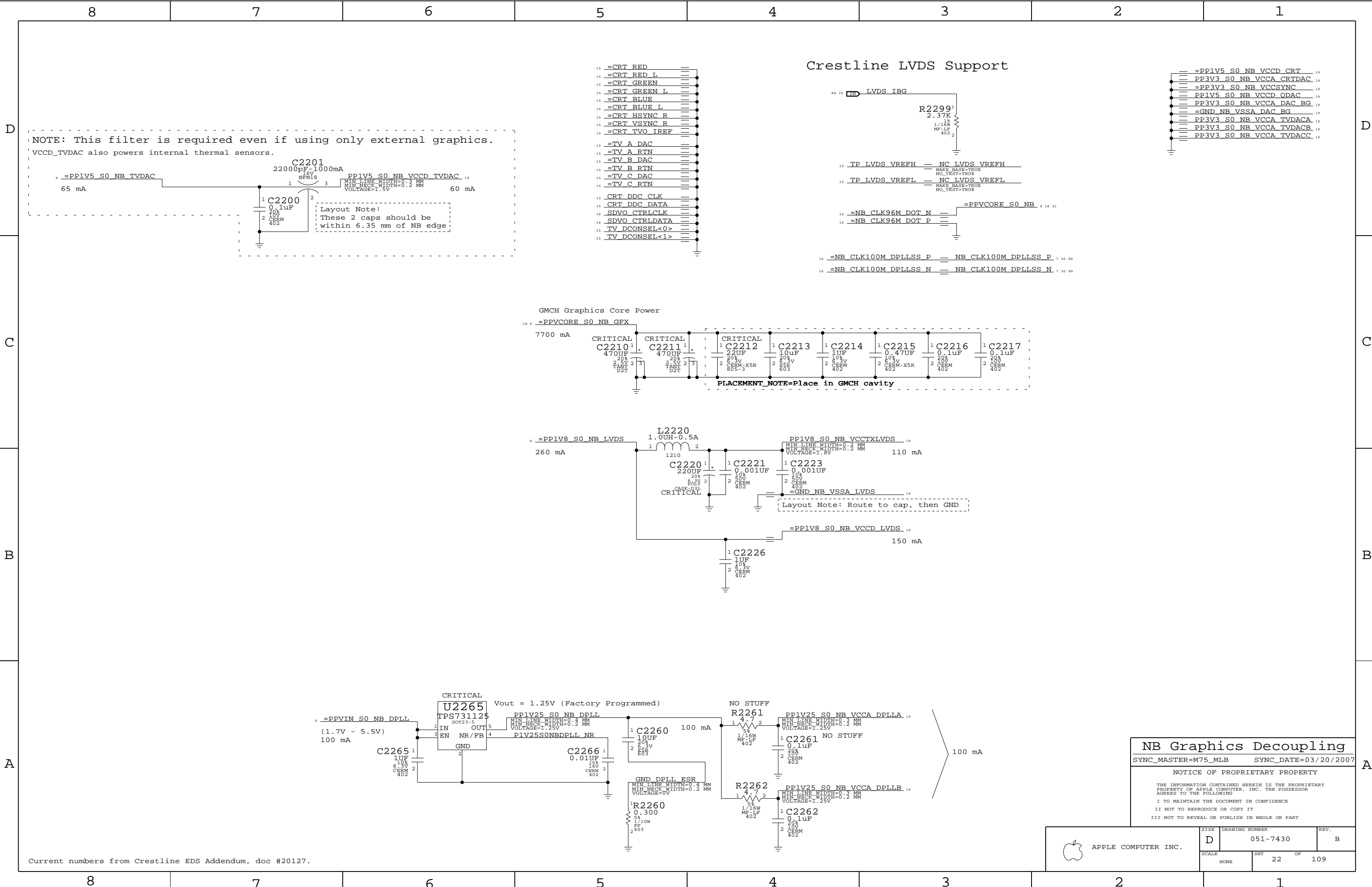




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NB Standard Decoupling		
SYNC_MASTER=T9_NOME		SYNC_DATE=12/21/2006
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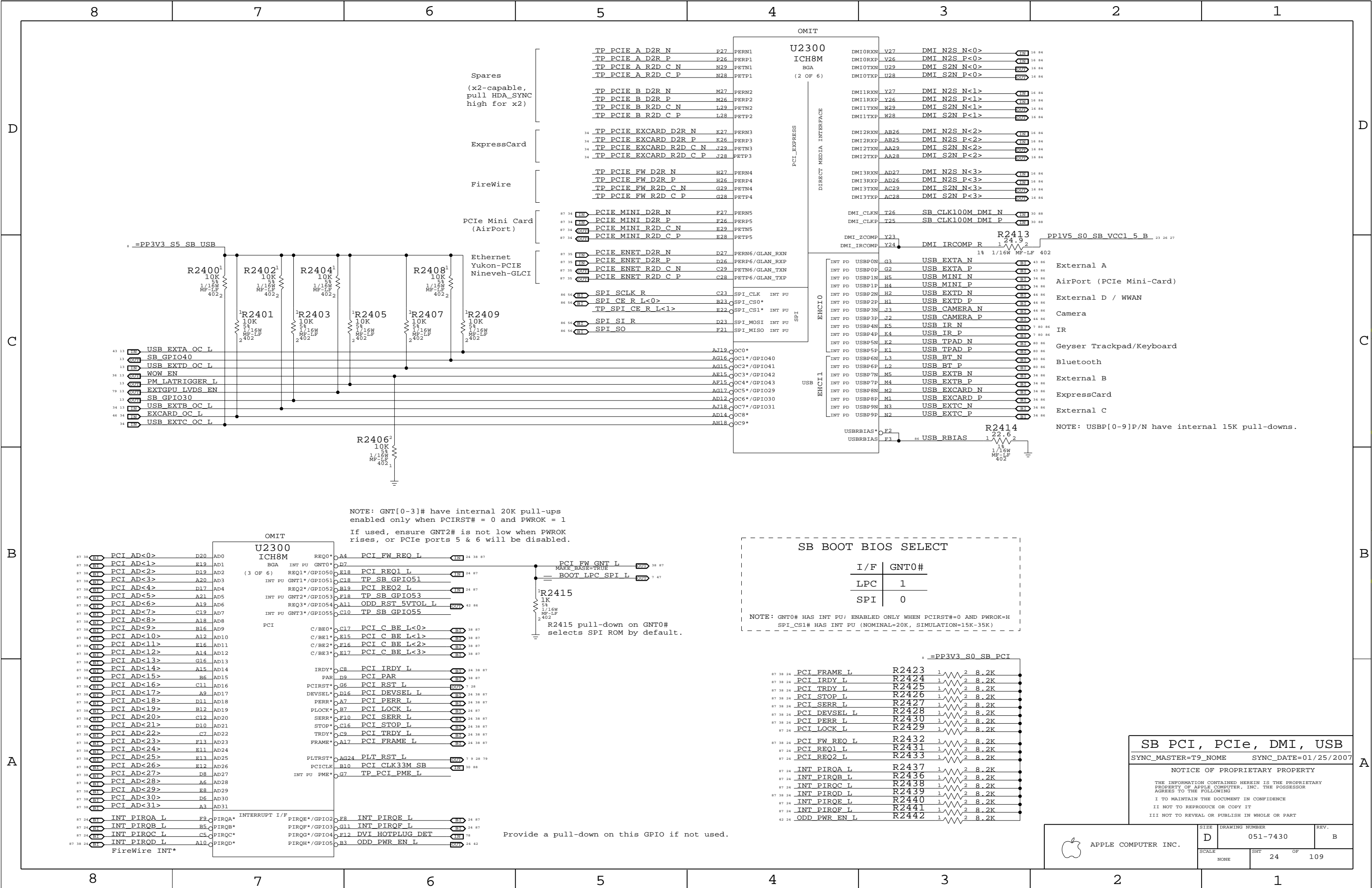
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7430	B
SCALE		SHT	OF
NONE		21	109

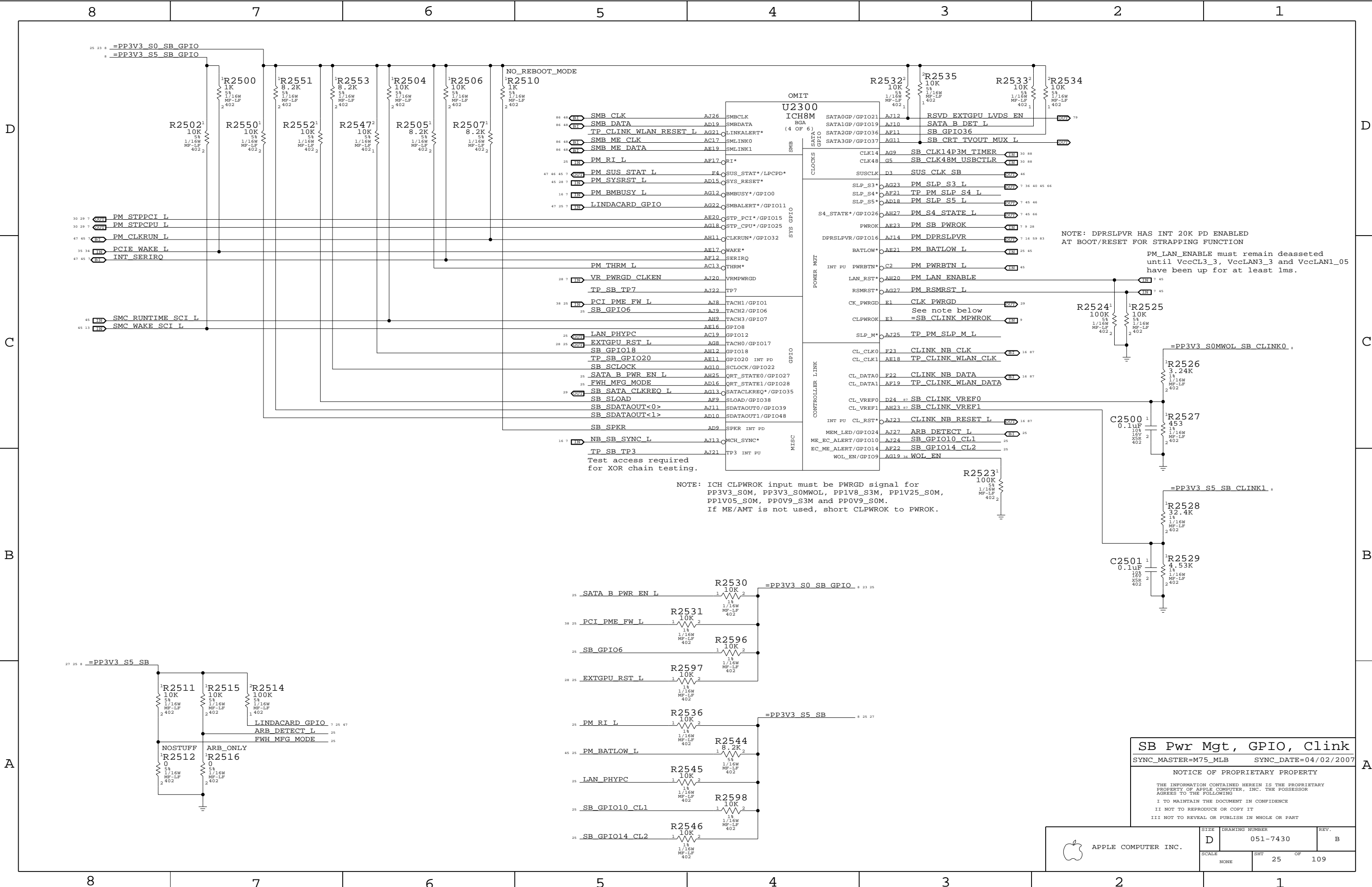


NB Graphics Decoupling		
SYNC_MASTER=M75_MLB	SYNC_DATE=03/20/2007	
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NONE		22	109

Current numbers from Crestline EDS Addendum, doc #20127.





NOTE: ICH CLPWROK input must be PWRGD signal for PP3V3_S0M, PP3V3_S0MWOL, PP1V8_S3M, PP1V25_S0M, PP1V05_S0M, PP0V9_S3M and PP0V9_S0M. If ME/AMT is not used, short CLPWROK to PWROK.

NOTE: DPRSLPVR HAS INT 20K PD ENABLED AT BOOT/RESET FOR STRAPPING FUNCTION
PM_LAN_ENABLE must remain deasserted until VccCL3_3, VccLAN3_3 and VccLAN1_05 have been up for at least 1ms.

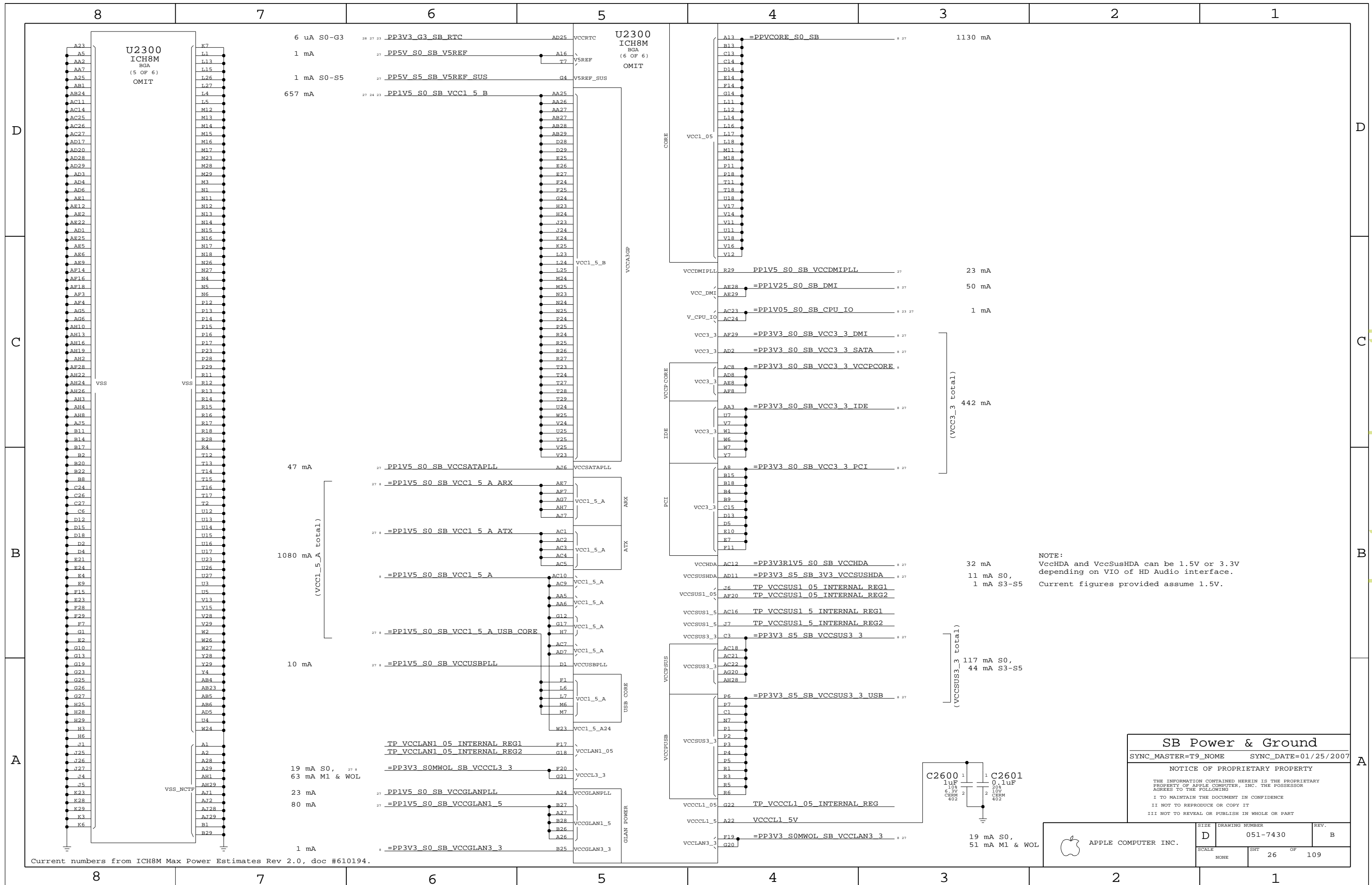
SB Pwr Mgt, GPIO, Clink

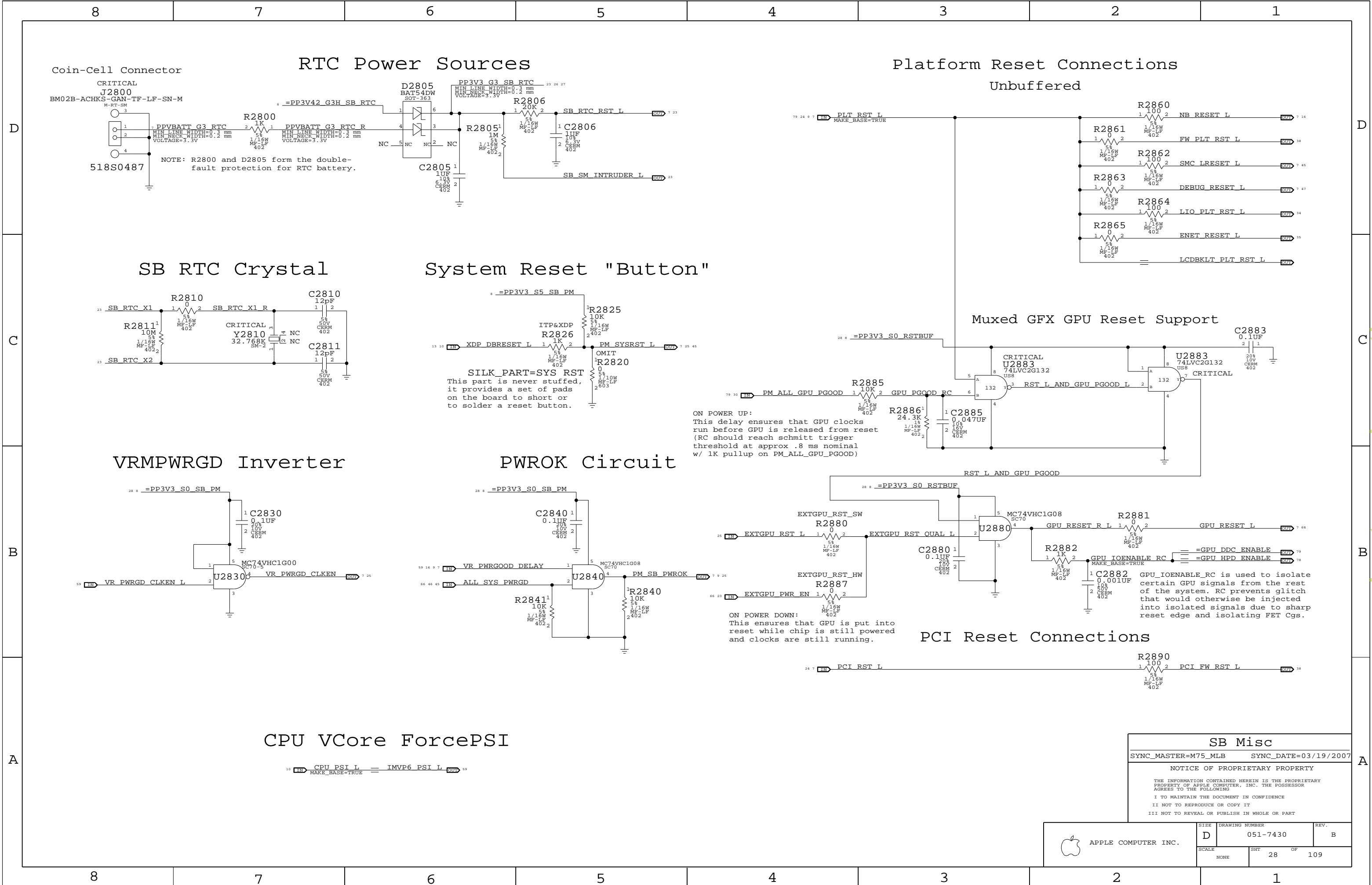
SYNC_MASTER=M75_MLB SYNC_DATE=04/02/2007

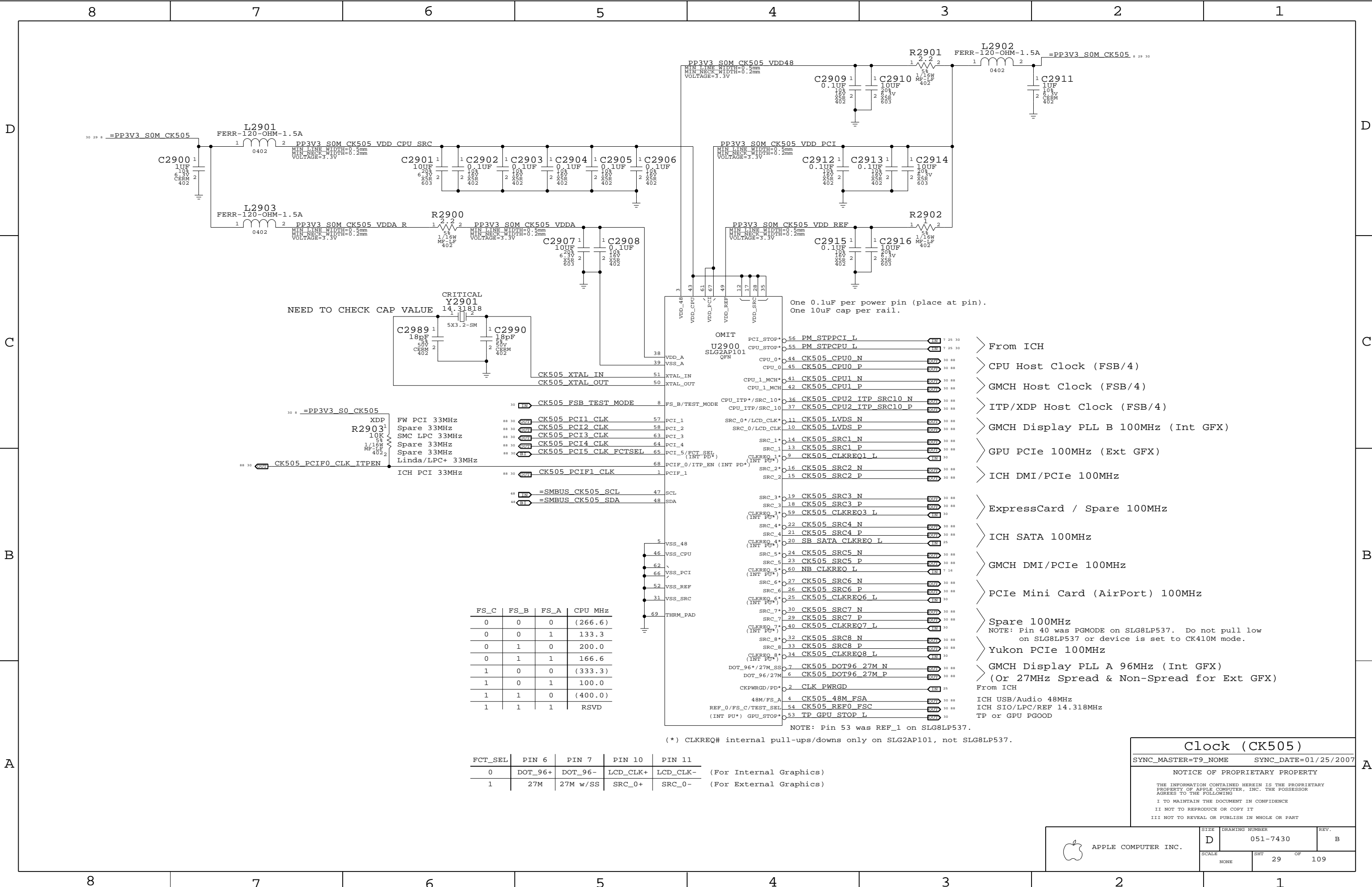
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	D	051-7430	B
SCALE		SHT	OF
NONE		25	109







FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

FCT_SEL	PIN 6	PIN 7	PIN 10	PIN 11
0	DOT_96+	DOT_96-	LCD_CLK+	LCD_CLK-
1	27M	27M w/SS	SRC_0+	SRC_0-

(For Internal Graphics)
(For External Graphics)

Clock (CK505)

SYNC_MASTER=T9_NAME SYNC_DATE=01/25/2007

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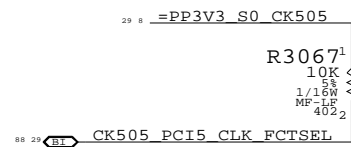
APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-7430 REV. B

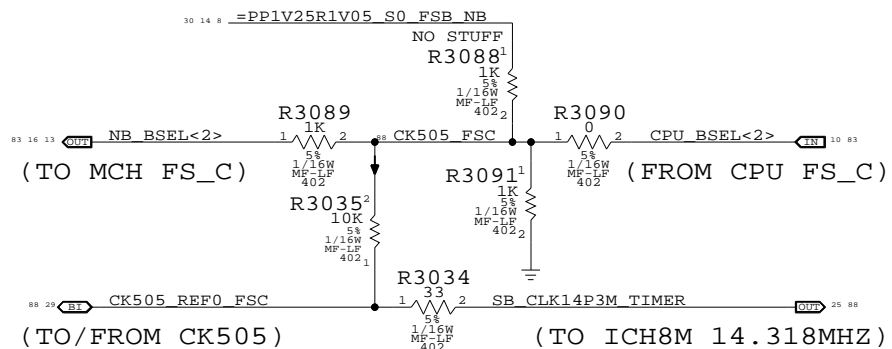
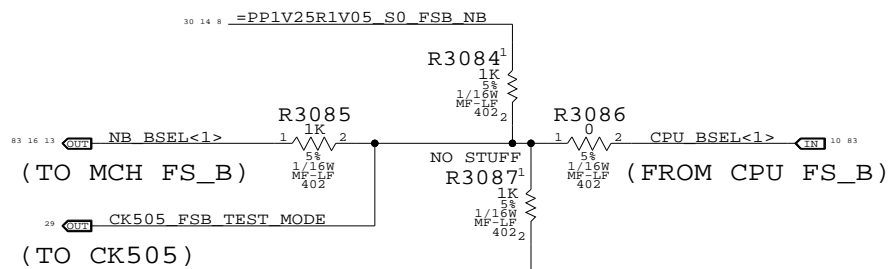
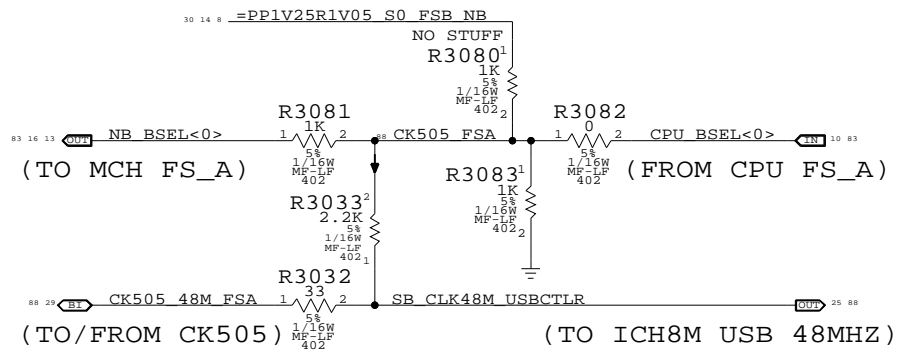
SCALE NONE SHT 29 OF 109

CK505 Configuration Straps

FCT_SEL (GFX clock select)



FS_A, FS_B, FS_C (Host clock freq select)



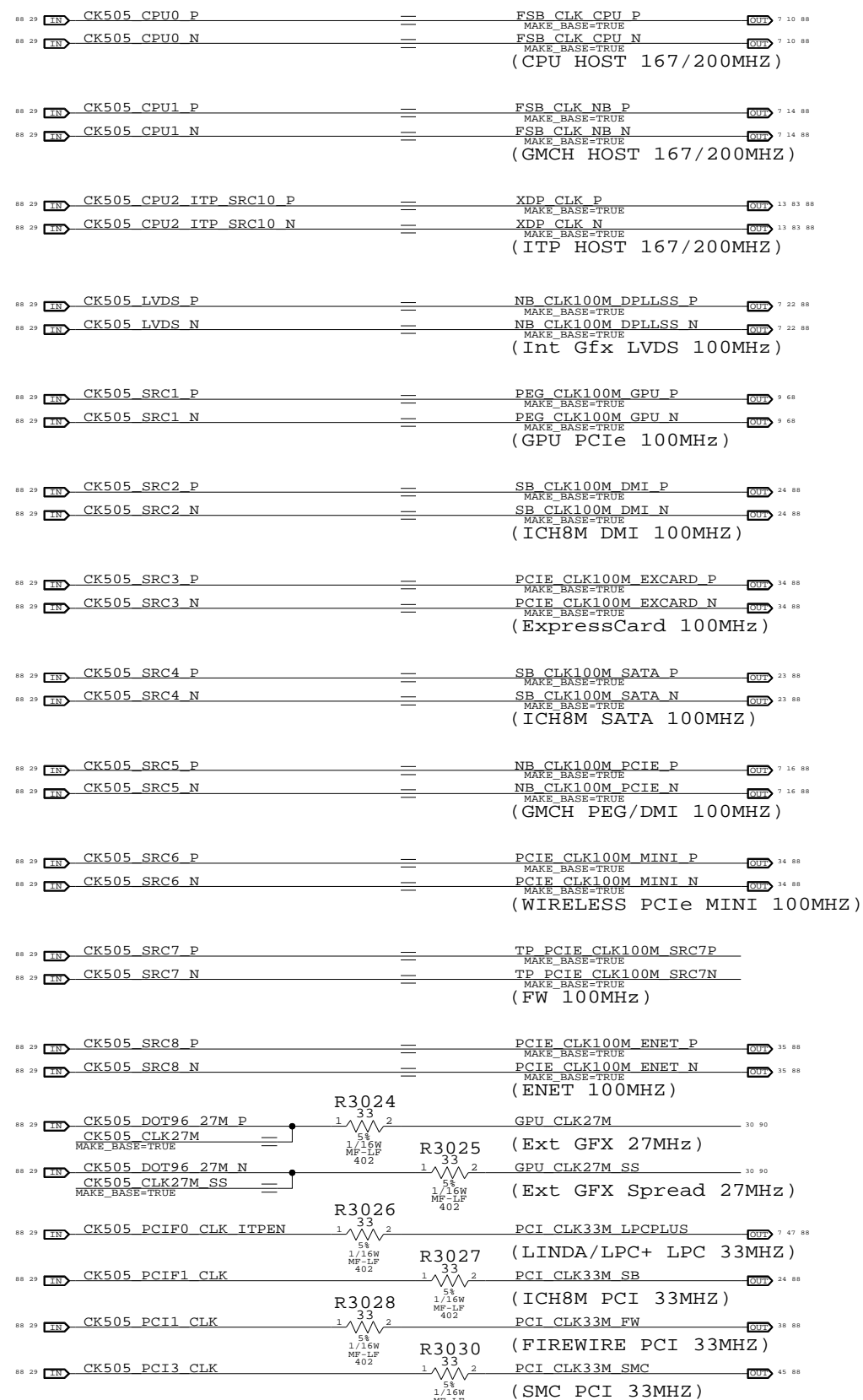
FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

NO STUFF R3082, R3086 & R3090
for manual CPU clk frequency.

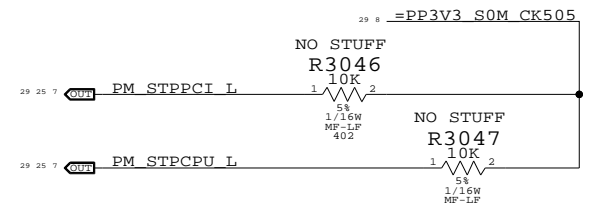
(Only 100-200MHz supported by
SLG8LP536 and CY28545-5)

CLK Termination

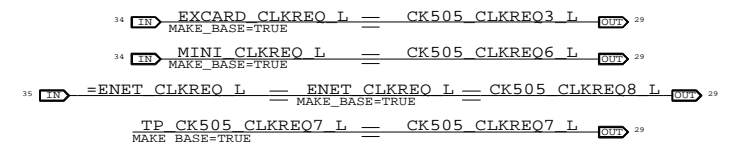
(Note: HOST/SRC/GFX clock termination removed. Silego SL8GLP536 or equiv. support only)



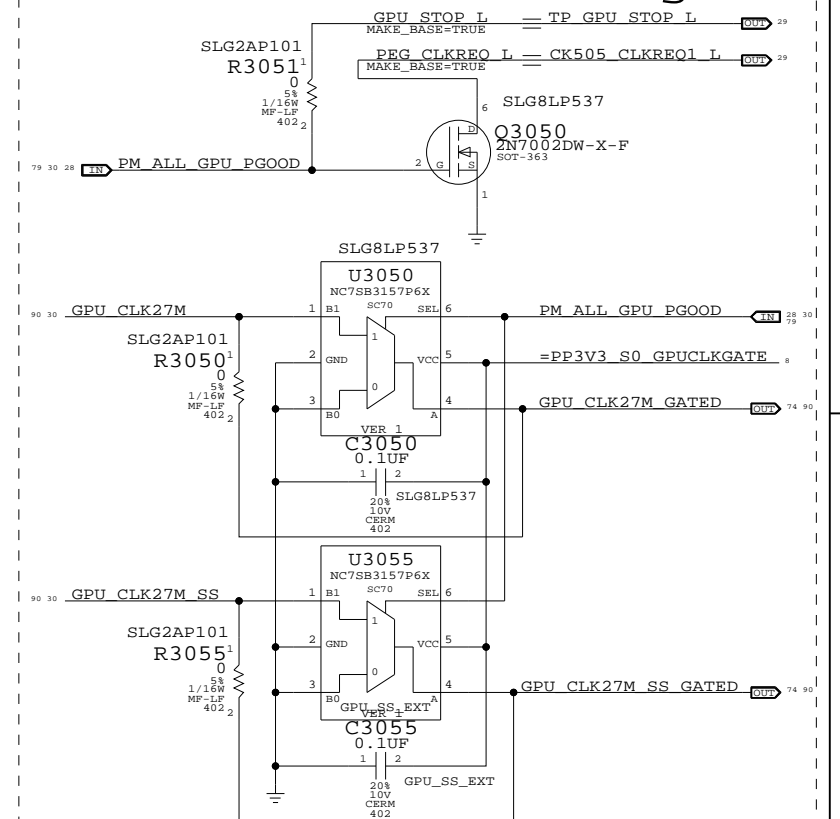
CLKREQ Controls



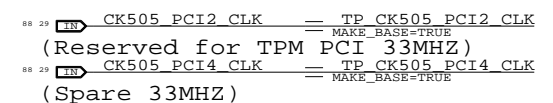
Silego SLG2AP101 has internal pull-ups⁴⁰² on all CLKRE# pins. Support for SL8GLP537 or equiv. only. NB and SATA CLKREQs are not remappable (and thus are not shown here).



GPU Clock Gating



Unused Clocks



Clock Termination

SYNC_MASTER=M75_MLB	SYNC_DATE=03/19/2007
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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D	051-7430	B
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D		
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SCALE	SHT	OF
	30	109

NONE	50	100
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[illegible]

1

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```

Power aliases required by this page:
- =PPIV8_S3M_MEM_A
- =PPOV9_S3M_MEM_DIMMVREFA
- =PPSPD_S0M_MEM_A (2.5V - 3.3V)

```

```

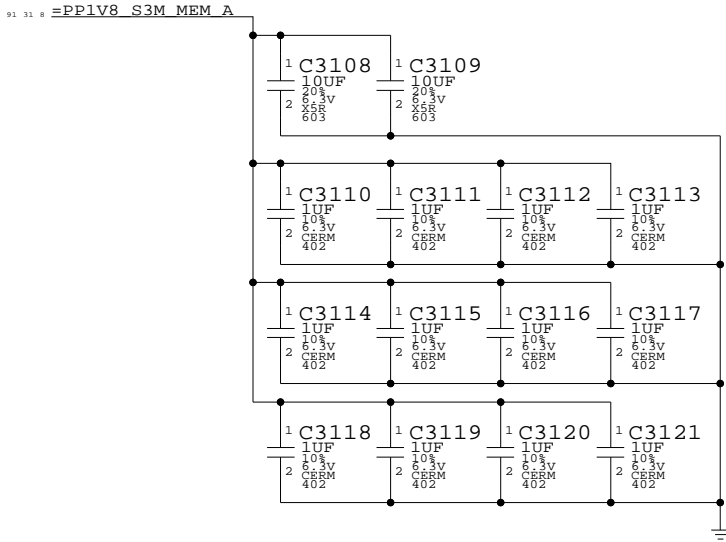
Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

```

```

BOM options provided by this page:
(NONE)

```



DDR2 SO-DIMM Connector A

SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007


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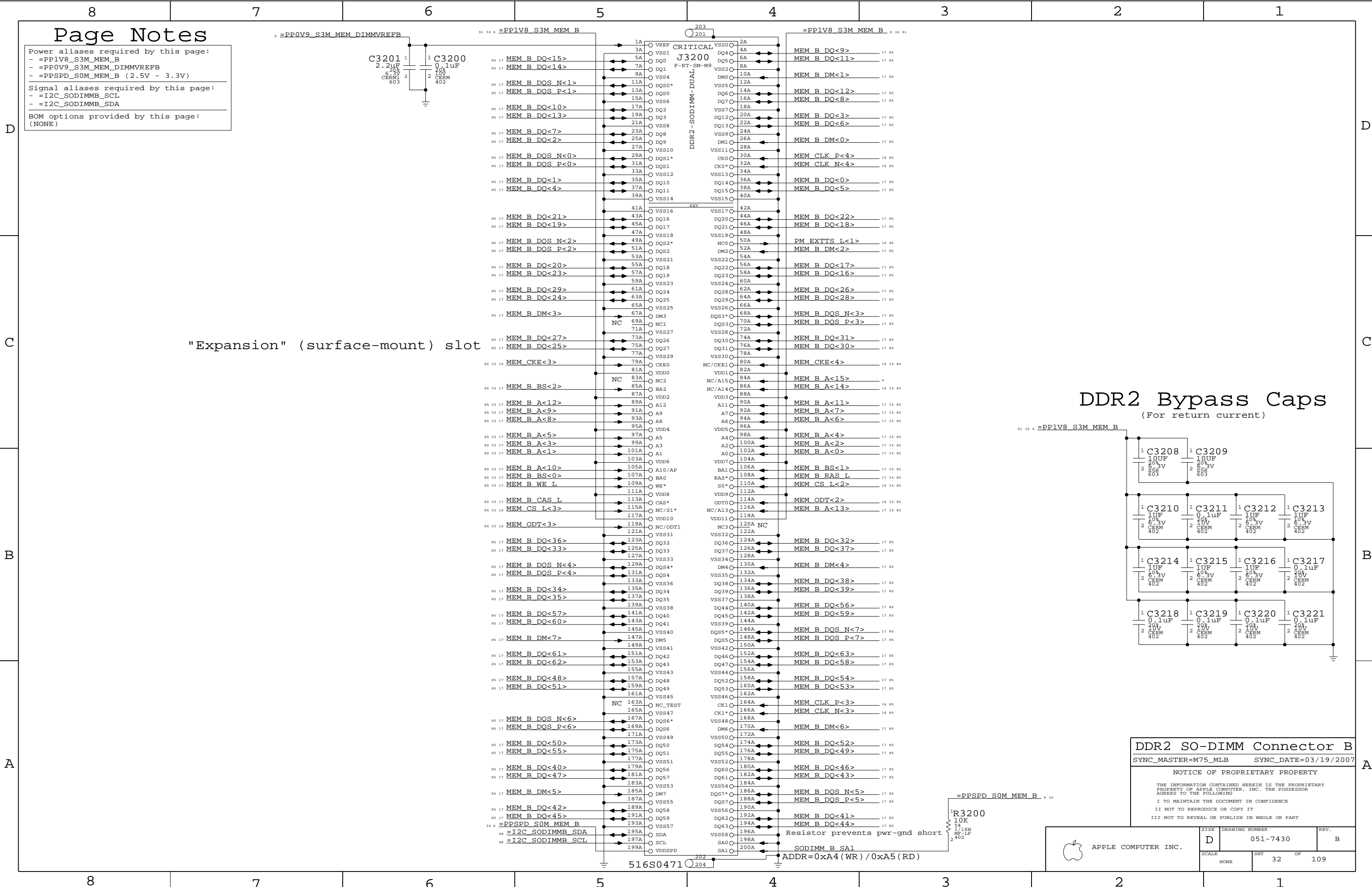
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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7430	B
	SCALE	SHT	OF
	NONE	31	109



Page Notes

Power aliases required by this page:
- =PP1V8_S3M_MEM_B
- =PP0V9_S3M_MEM_DIMMVREFB
- =PPSPD_S0M_MEM_B (2.5V - 3.3V)

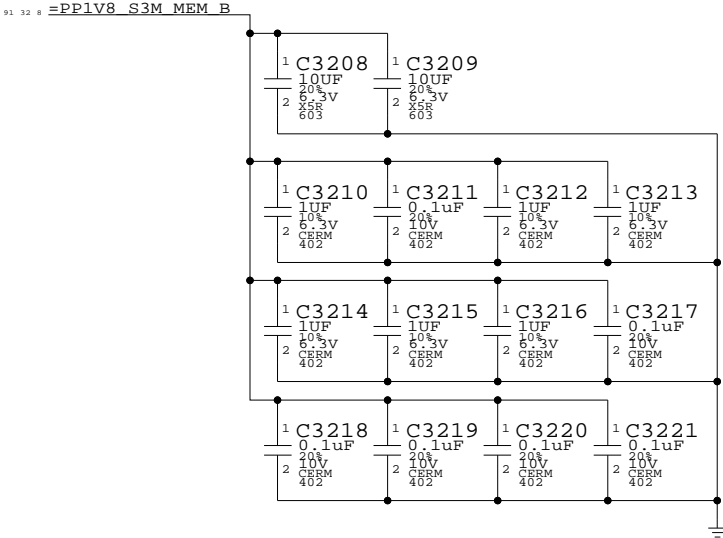
Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

"Expansion" (surface-mount) slot

DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector B

SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

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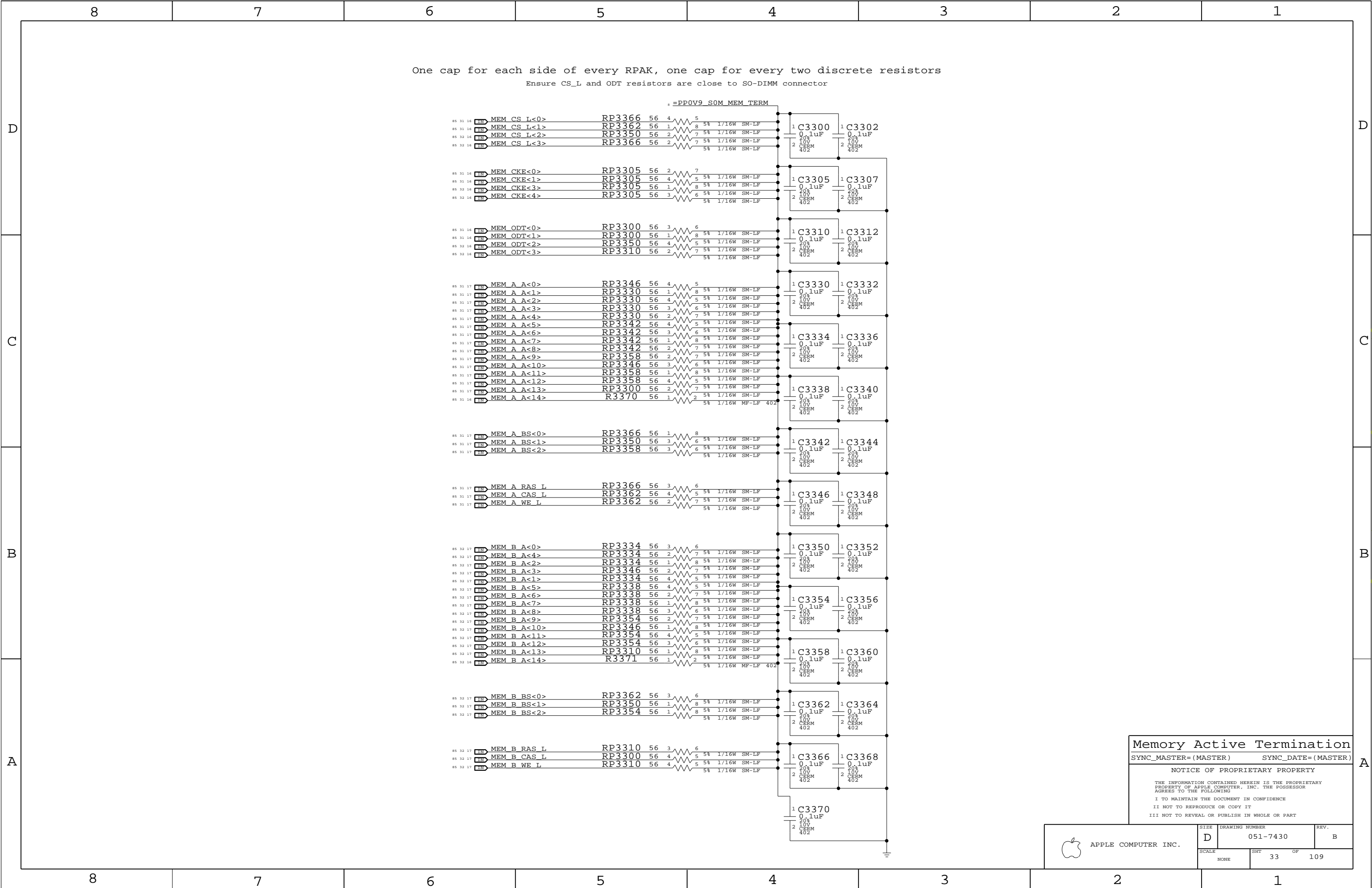
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APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-7430 REV. B

SCALE NONE SHT 32 OF 109



Memory Active Termination

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

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SIZE

D

DRAWING NUMBER

051-7430

REV.

B

SCALE

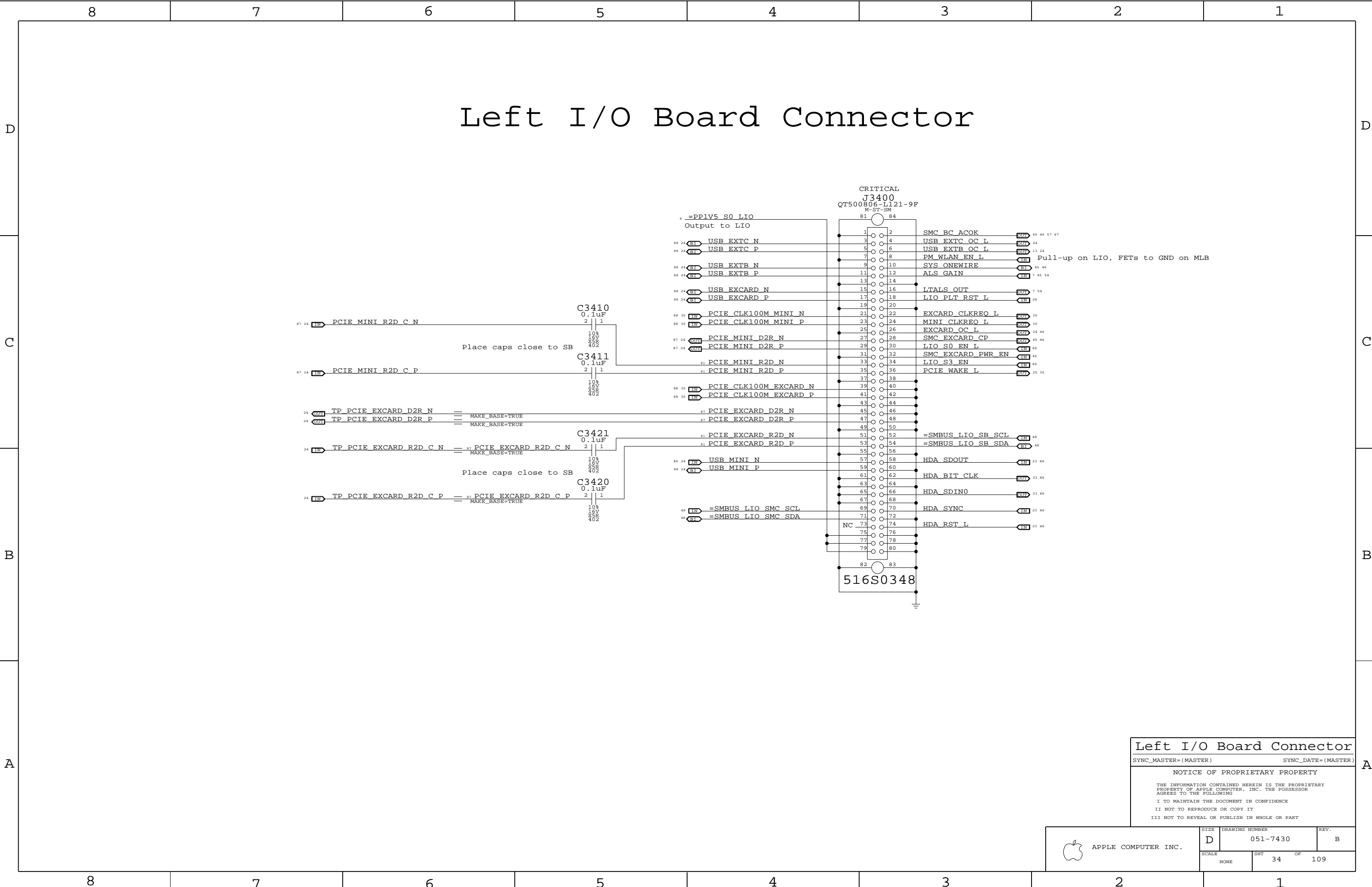
NONE

SHT

33

OF

109



Left I/O Board Connector

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Left I/O Board Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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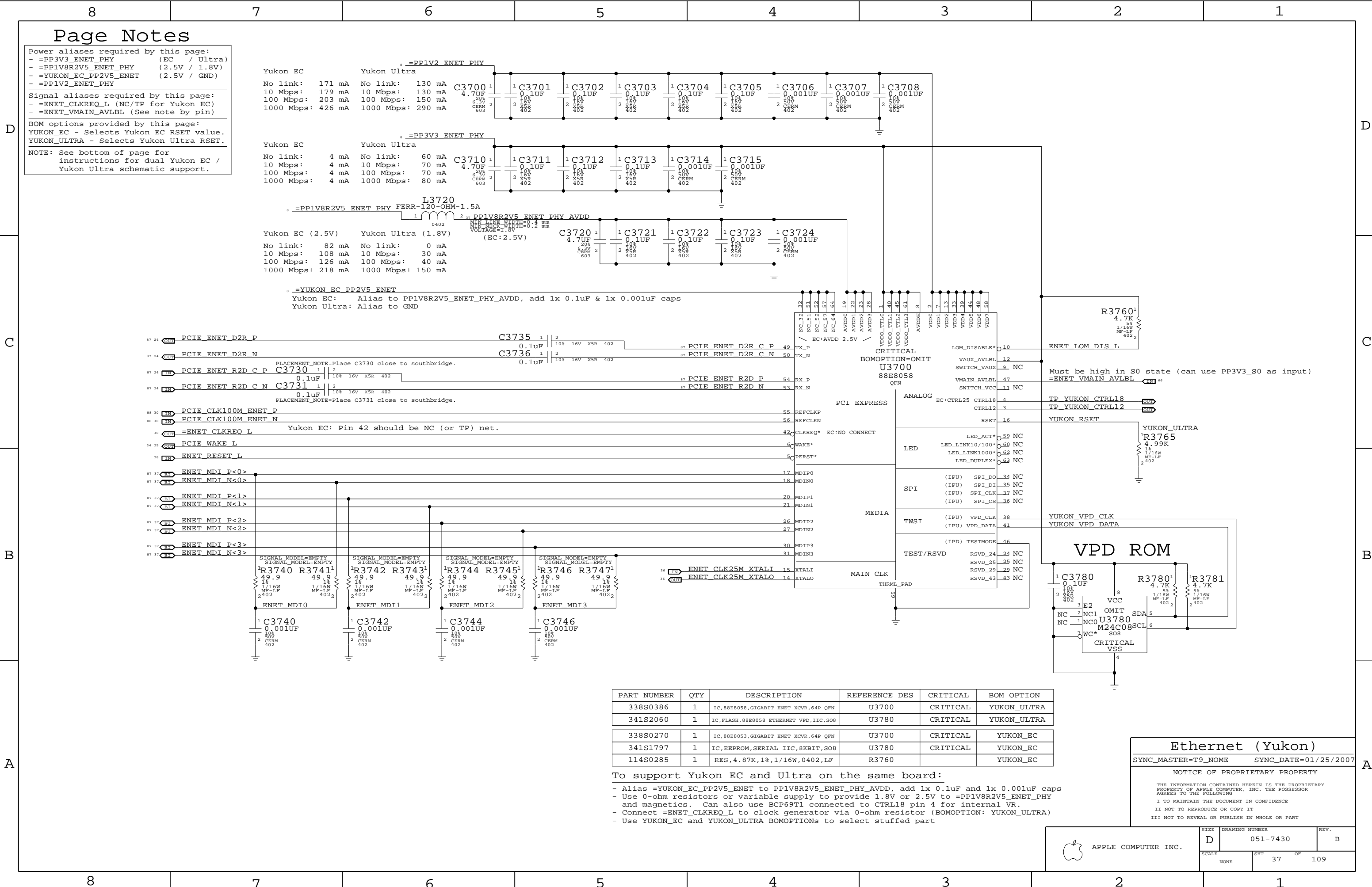
II NOT TO REPRODUCE OR COPY IT

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SIZE	DRAWING NUMBER	REV.
D	051-7430	B
SCALE	SHT	OF
NONE	34	109



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0386	1	IC, 88E8058, GIGABIT ENET XCVR, 64P QFN	U3700	CRITICAL	YUKON_ULTRA
341S2060	1	IC, FLASH, 88E8058 ETHERNET VPD, IIC, SO8	U3780	CRITICAL	YUKON_ULTRA
338S0270	1	IC, 88E8053, GIGABIT ENET XCVR, 64P QFN	U3700	CRITICAL	YUKON_EC
341S1797	1	IC, EEPROM, SERIAL IIC, 8KBIT, SO8	U3780	CRITICAL	YUKON_EC
114S0285	1	RES, 4.87K, 1%, 1/16W, 0402, LF	R3760		YUKON_EC

To support Yukon EC and Ultra on the same board:

- Alias =YUKON_EC_PP2V5_ENET to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF and 1x 0.001uF caps
- Use 0-ohm resistors or variable supply to provide 1.8V or 2.5V to =PP1V8R2V5_ENET_PHY and magnetics. Can also use BCP69T1 connected to CTRL18 pin 4 for internal VR.
- Connect =ENET_CLKREQ_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON_ULTRA)
- Use YUKON_EC and YUKON_ULTRA BOMOPTIONS to select stuffed part

Ethernet (Yukon)

SYNC_MASTER=T9_NAME SYNC_DATE=01/25/2007

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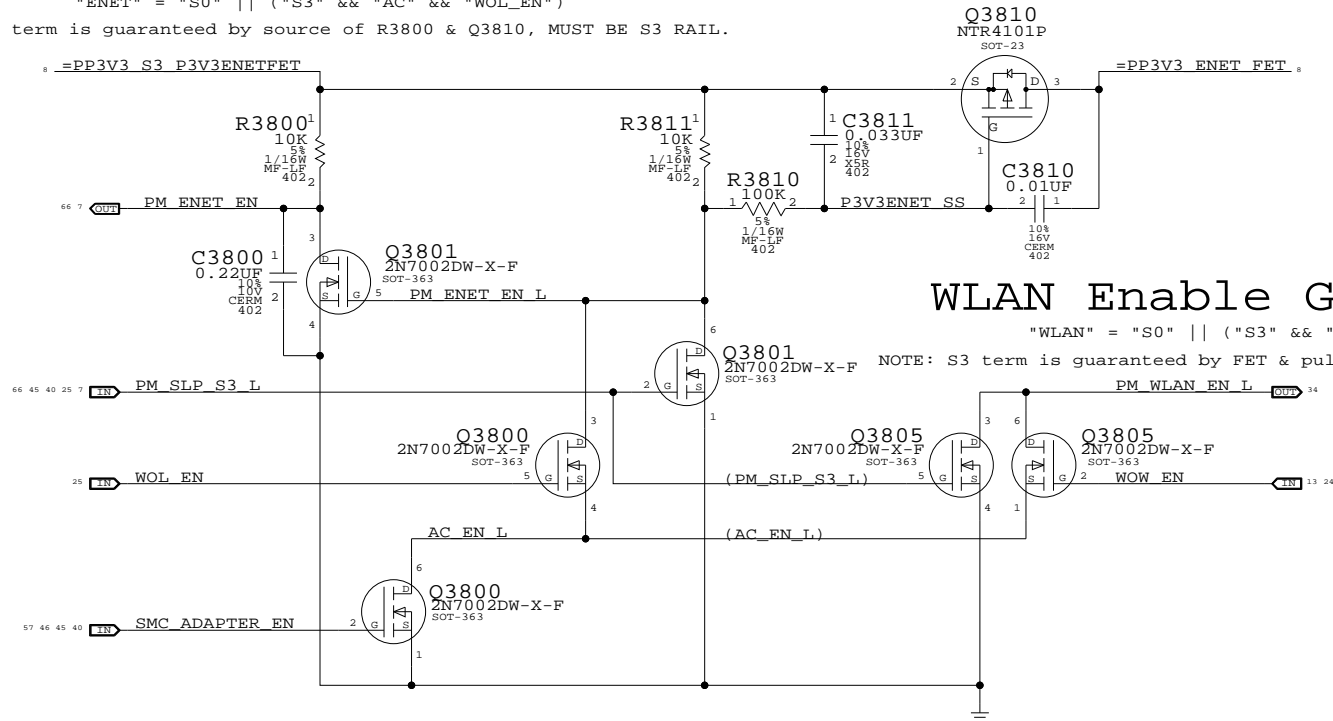
APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-7430 REV. B

SCALE NONE SHT 37 OF 109

ENET Enable Generation

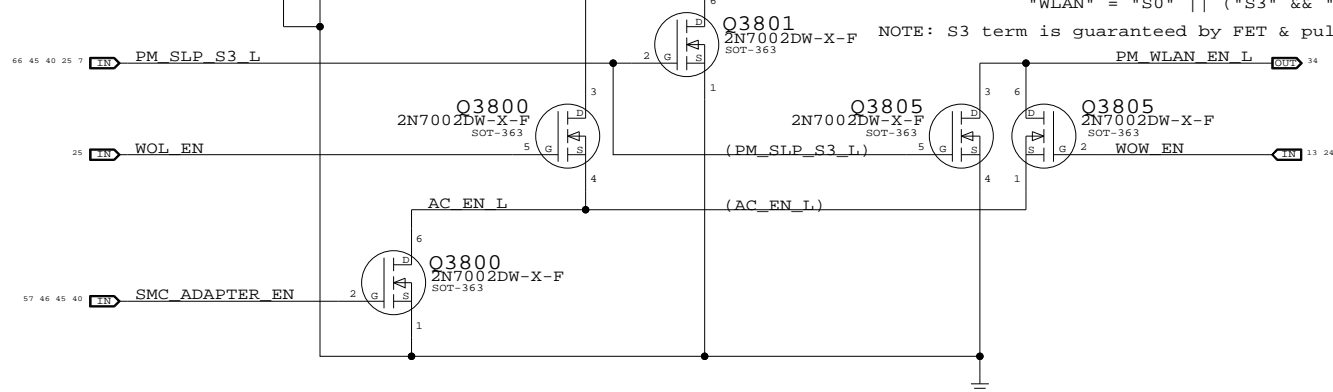
"ENET" = "S0" || ("S3" && "AC" && "WOL_EN")
NOTE: S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.



3.3V ENET FET

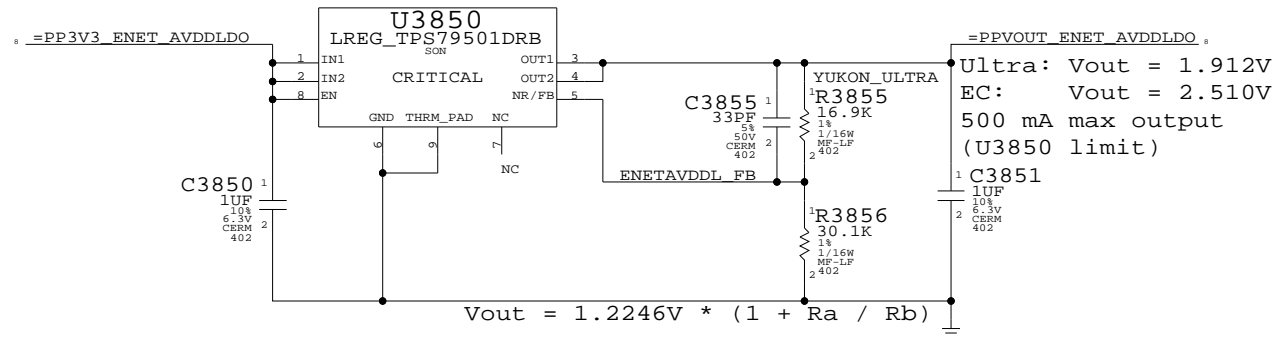
WLAN Enable Generation

"WLAN" = "S0" || ("S3" && "AC" && "WOW_EN")
NOTE: S3 term is guaranteed by FET & pull-up source, MUST BE S3 RAIL.



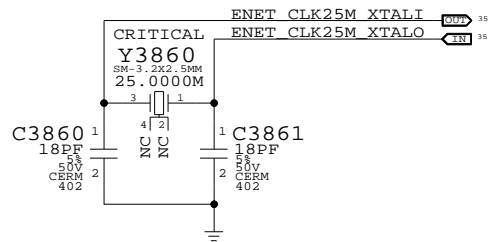
Yukon AVDDL LDO

1.9V for Yukon Ultra, 2.5V for Yukon EC
Yukon Ultra requires 1.9V on its magnetics to pass compliance tests



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0363	1	RES,31.6K,1%,1/16W,402,LF	R3855		YUKON_EC

Yukon Crystal



Yukon Power Control

SYNC_MASTER=T9_NOME SYNC_DATE=03/19/2007

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NONE	38	109

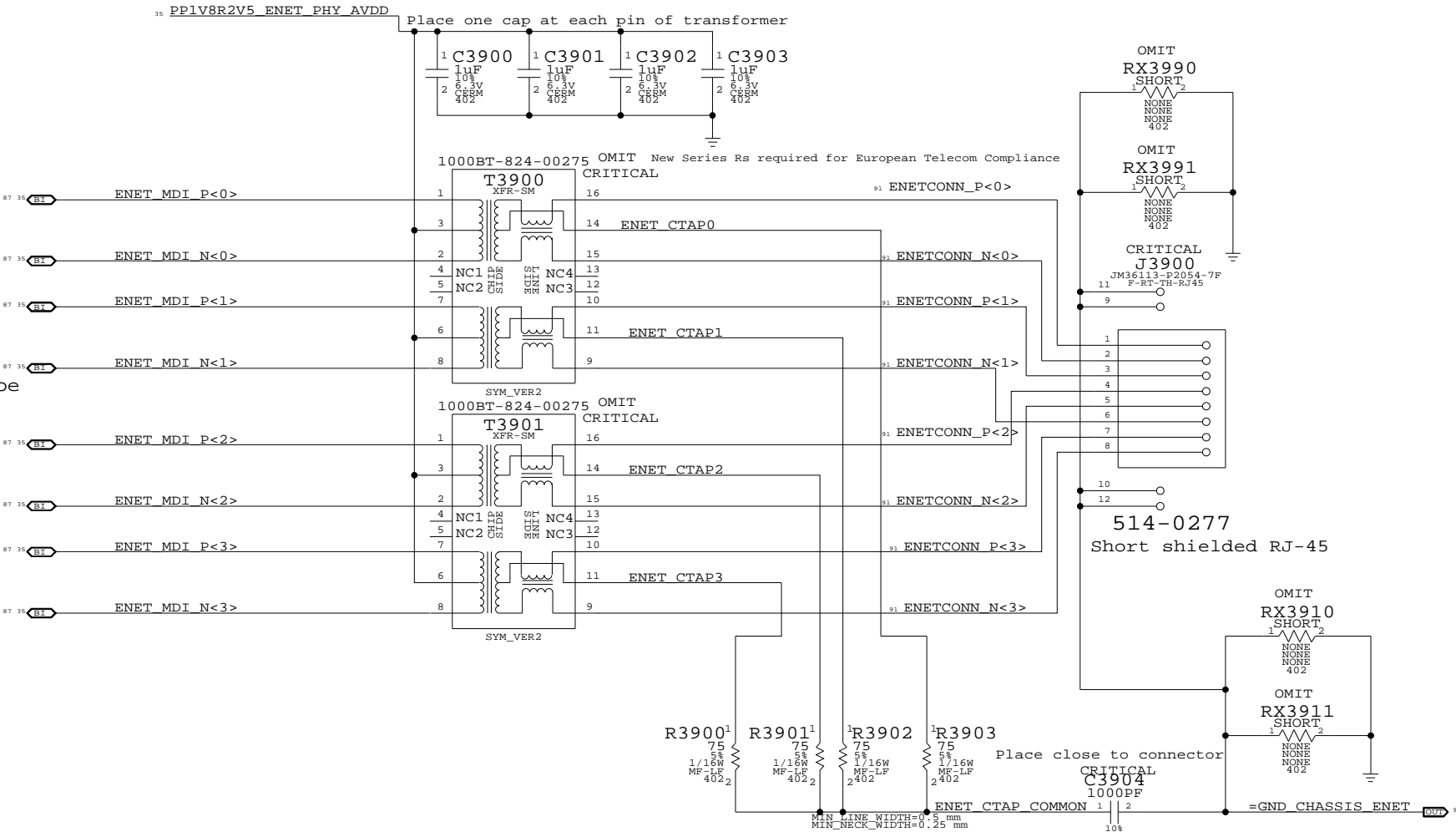
Page Notes

Power aliases required by this page:
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Transformers should be mirrored on opposite sides of the board



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
157S0030	2	XFRM_ISO_HALF-PORT,1000T,16P,SMD,2MM	T3900,T3901	CRITICAL	

Ethernet Connector

SYNC_MASTER=M75_MLB SYNC_DATE=12/21/2006

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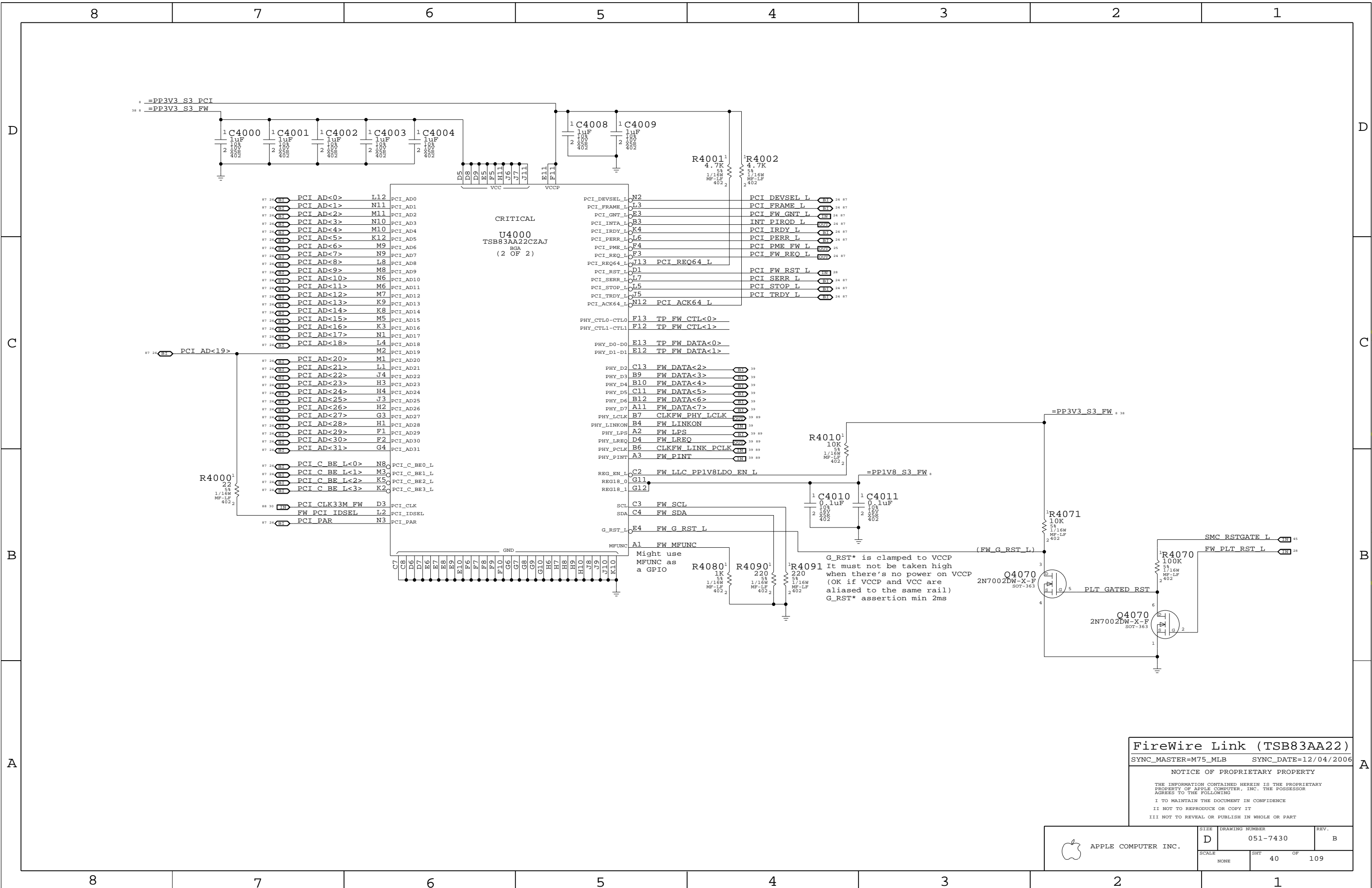
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SIZE D DRAWING NUMBER 051-7430 REV. B

SCALE NONE SHT 39 OF 109



FireWire Link (TSB83AA22)

SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006

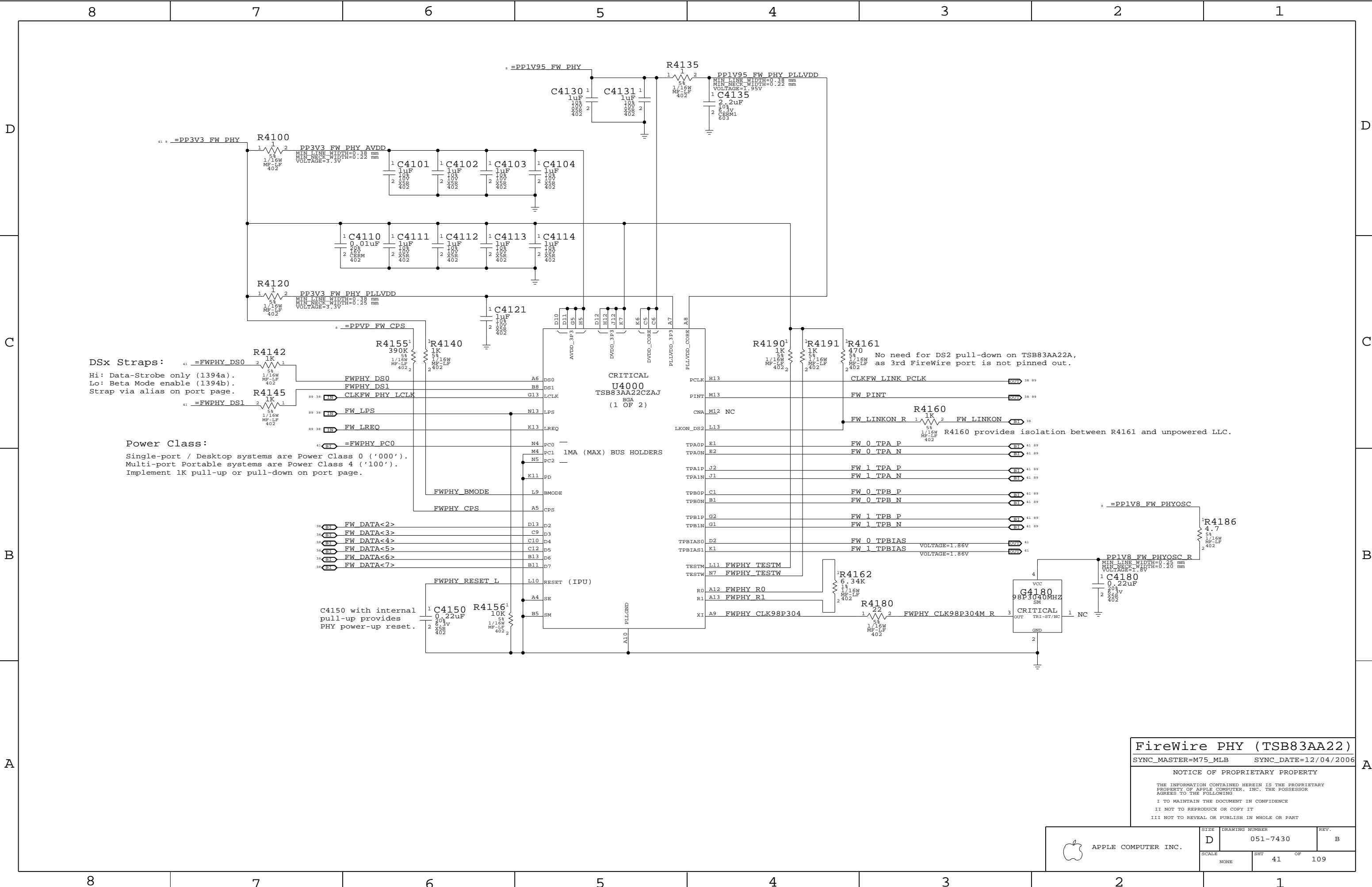
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D	051-7430	B
SCALE	SHT	OF
NONE	40	109



8 7 6 5 4 3 2 1

D

D

C

C

B

B

A

A

FireWire PHY (TSB83AA22)

SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006

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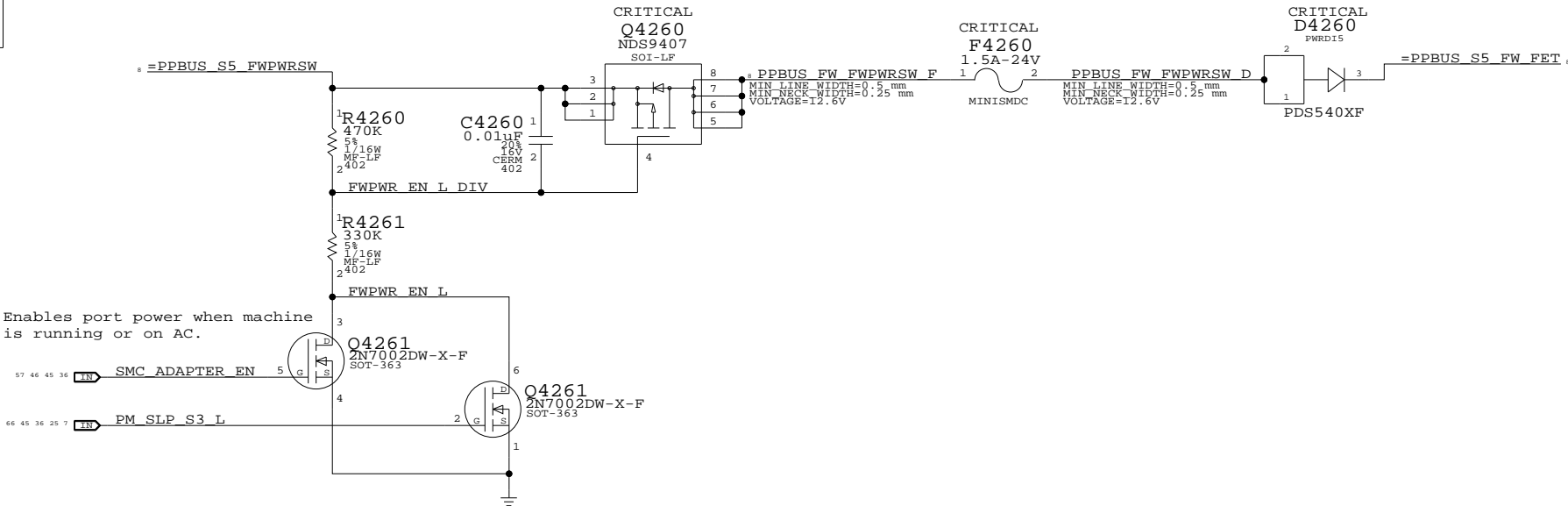
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	D	051-7430	B
SCALE		SHT	OF
NONE		41	109

Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
- FW_PORT_FAULT_PU

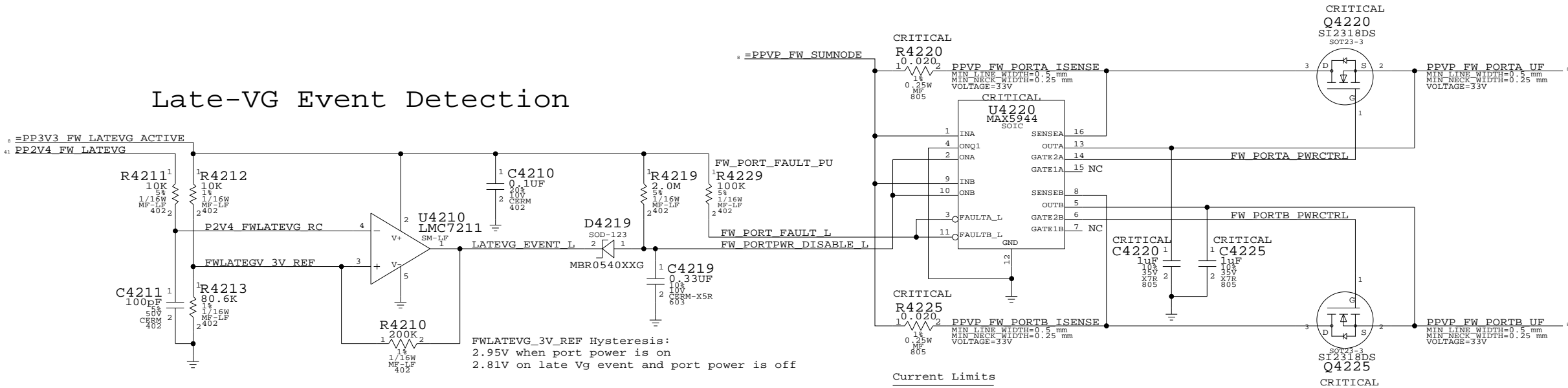
FireWire Port Power Switch



Current Limit/Active Late-VG Protection

R4220 & R4225 PADS SHOULD BE ROUTED DIRECTLY TO MAX5944 SENSEA & SENSEB PINS RESPECTIVELY. SENSEA & SENSEB PINS SHOULD NOT BE PART OF THE MAIN CURRENT PATH

Late-VG Event Detection



Current Limits
0.020 ohm => 2.4A
0.025 ohm => 2A
0.030 ohm => 1.66A (Ideal)
0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

FireWire Port Power

SYNC_MASTER=M75_MLB SYNC_DATE=03/07/2007

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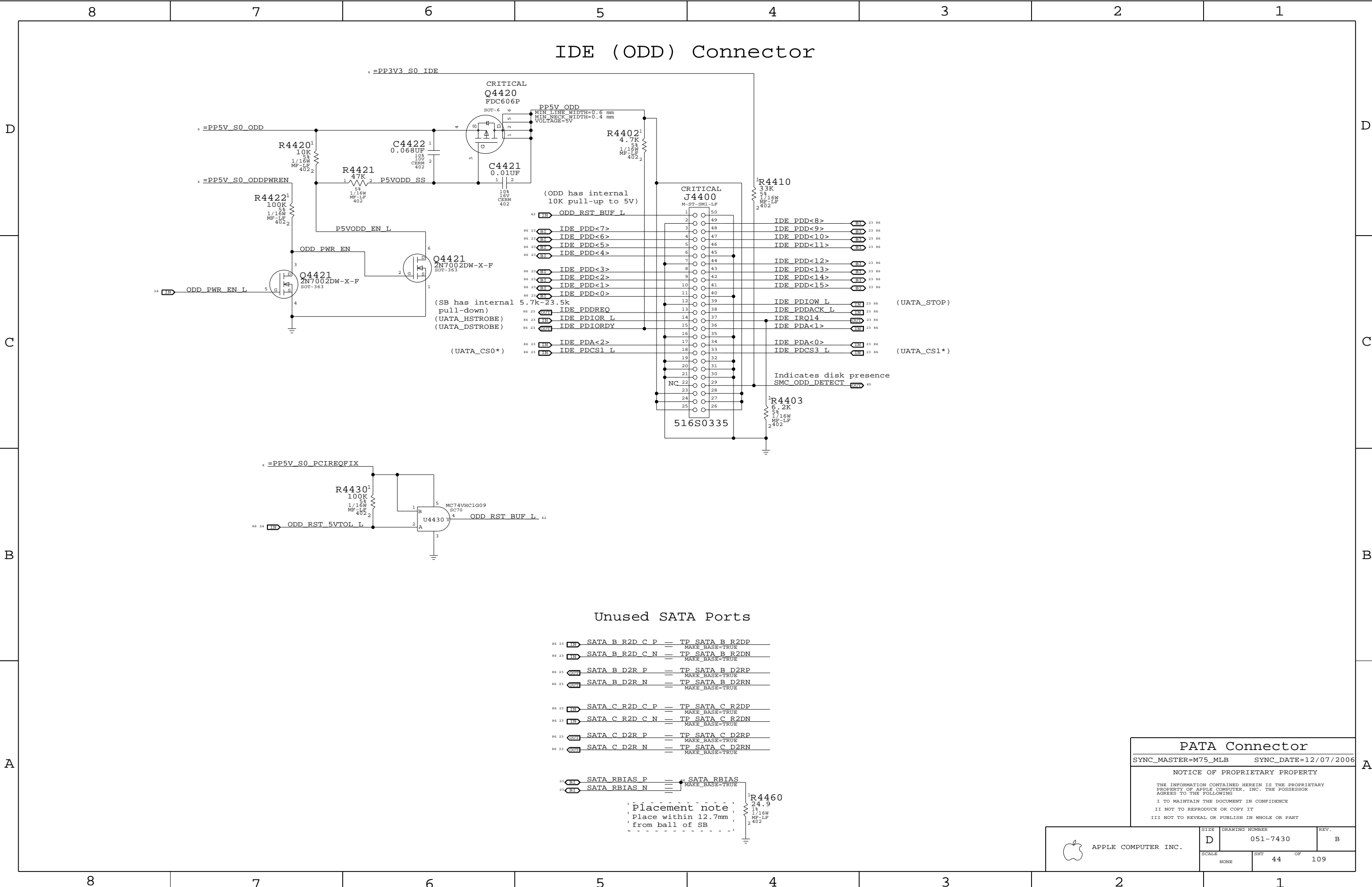


APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7430	B
SCALE	SHT	OF
NONE	42	109

[illegible]

10



IDE (ODD) Connector

(ODD has internal 10K pull-up to 5V)

(SB has internal pull-down) (UATA_HSTROBE) (UATA_DSTROBE)

(UATA_CS0*)

(UATA_STOP)

(UATA_CS1*)

Indicates disk presence SMC_ODD_DETECT

Unused SATA Ports

- SATA B R2D C P == TP SATA B R2DP MAKE_BASE=TRUE
- SATA B R2D C N == TP SATA B R2DN MAKE_BASE=TRUE
- SATA B D2R P == TP SATA B D2RP MAKE_BASE=TRUE
- SATA B D2R N == TP SATA B D2RN MAKE_BASE=TRUE
- SATA C R2D C P == TP SATA C R2DP MAKE_BASE=TRUE
- SATA C R2D C N == TP SATA C R2DN MAKE_BASE=TRUE
- SATA C D2R P == TP SATA C D2RP MAKE_BASE=TRUE
- SATA C D2R N == TP SATA C D2RN MAKE_BASE=TRUE

- SATA RBIAS P == SATA RBIAS MAKE_BASE=TRUE
- SATA RBIAS N == SATA RBIAS MAKE_BASE=TRUE

Placement note Place within 12.7mm from ball of SB

PATA Connector

SYNC_MASTER=M75_MLB SYNC_DATE=12/07/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7430	B
SCALE	SHT	OF
NONE	44	109

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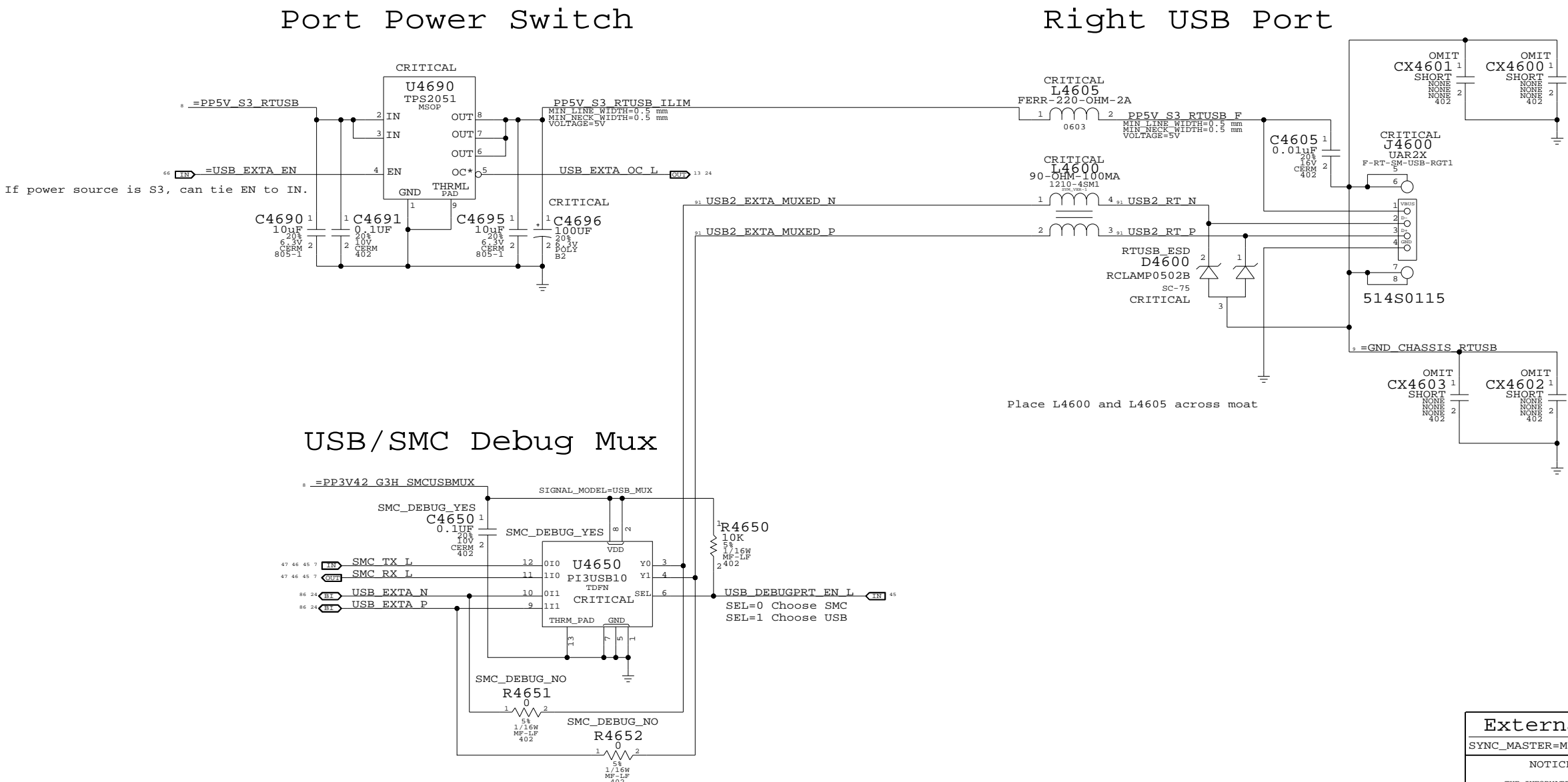
A

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External USB Connector

SYNC_MASTER=M75_MLB

SYNC_DATE=12/04/2006

NOTICE OF PROPRIETARY PROPERTY

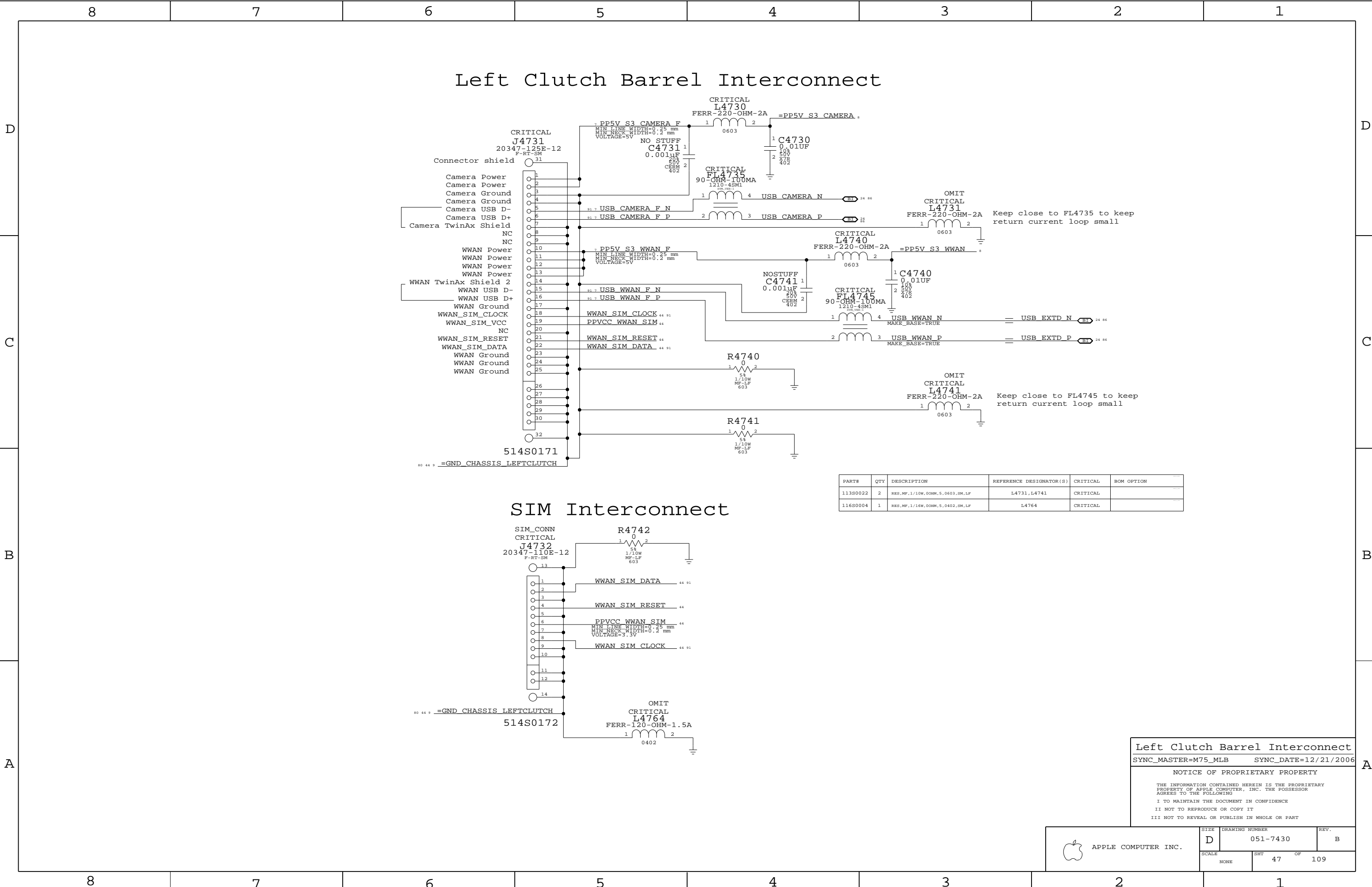
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7430	B
SCALE		SHT	OF
NONE		46	109



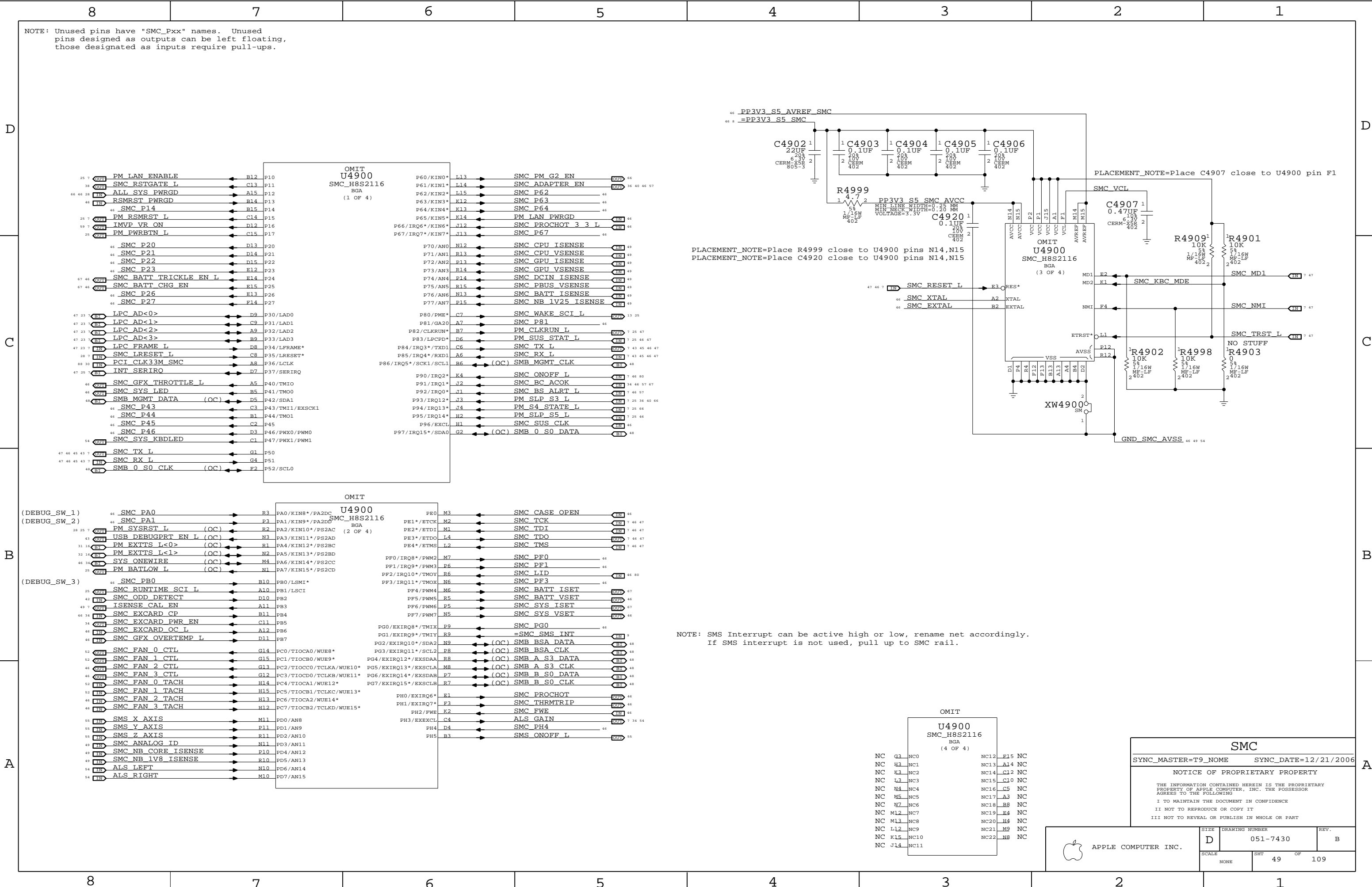
www.laptop-schematics.com

Left Clutch Barrel Interconnect
SYNC_MASTER=M75_MLB SYNC_DATE=12/21/2006

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7430	REV. B
	SCALE NONE	SHT 47	OF 109




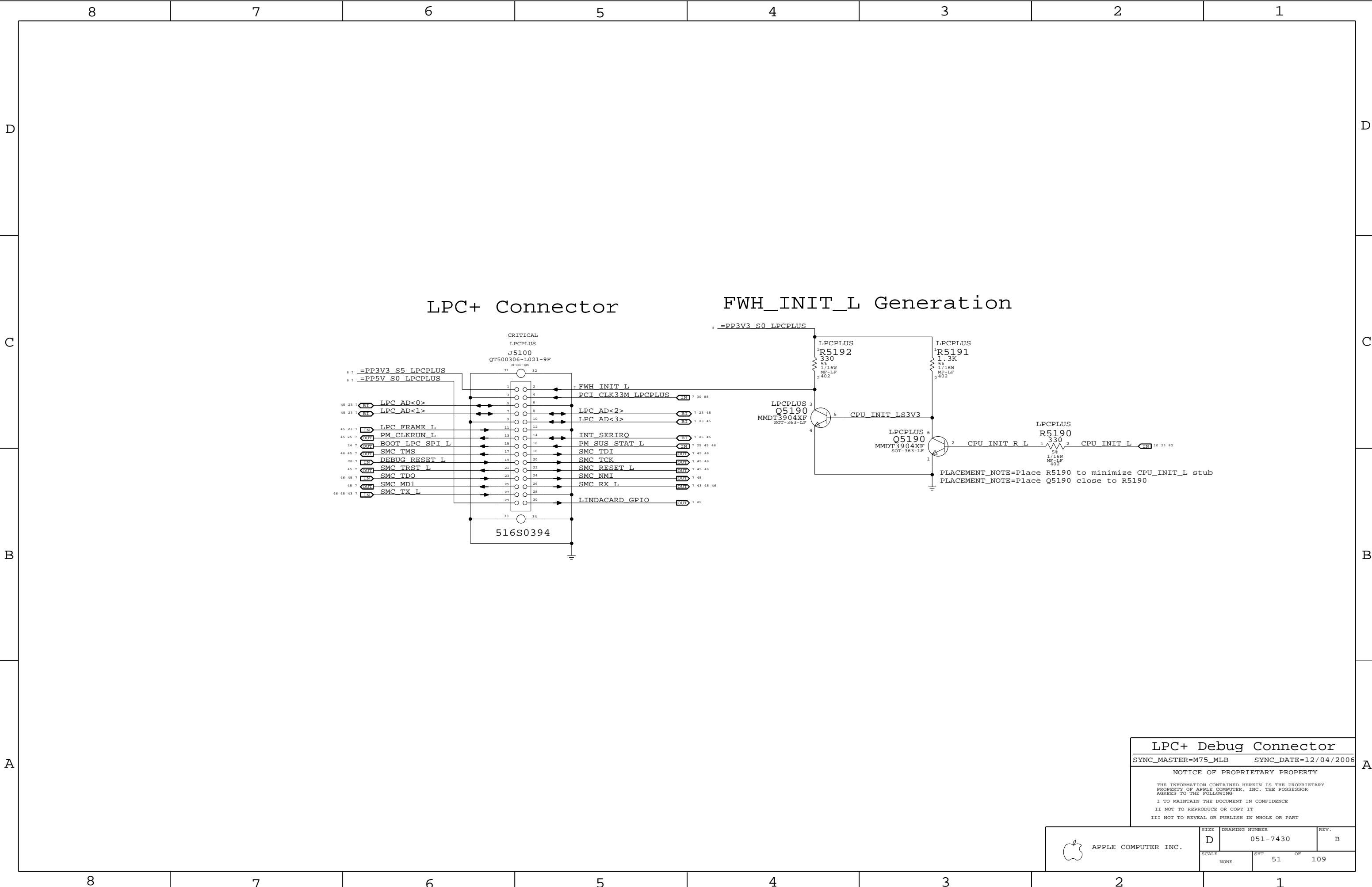
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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7430	B
	SCALE	SHT OF	
	NONE	50 109	



LPC+ Debug Connector

SYNC_MASTER=M75_MLB

SYNC_DATE=12/04/2006

NOTICE OF PROPRIETARY PROPERTY

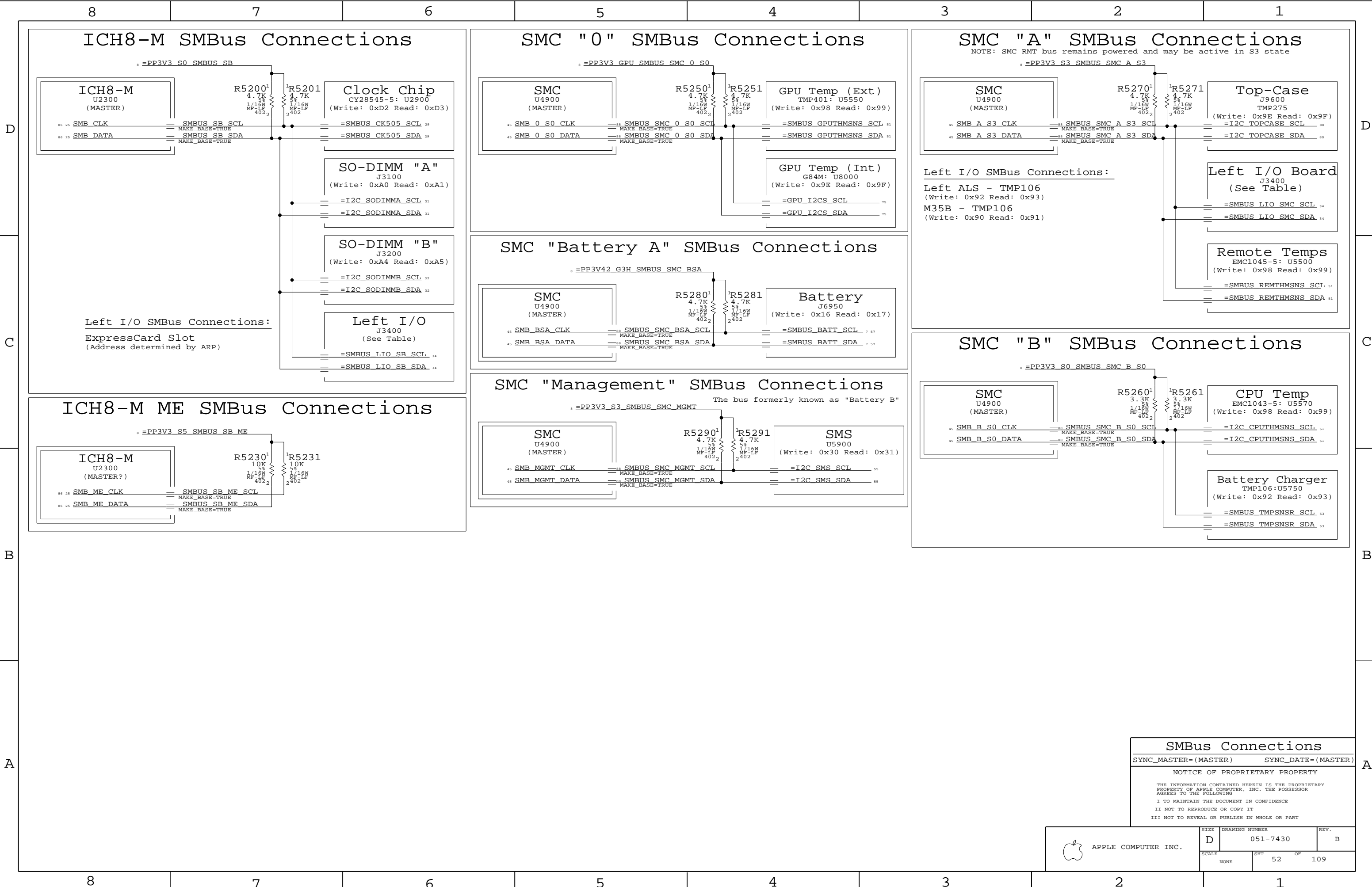
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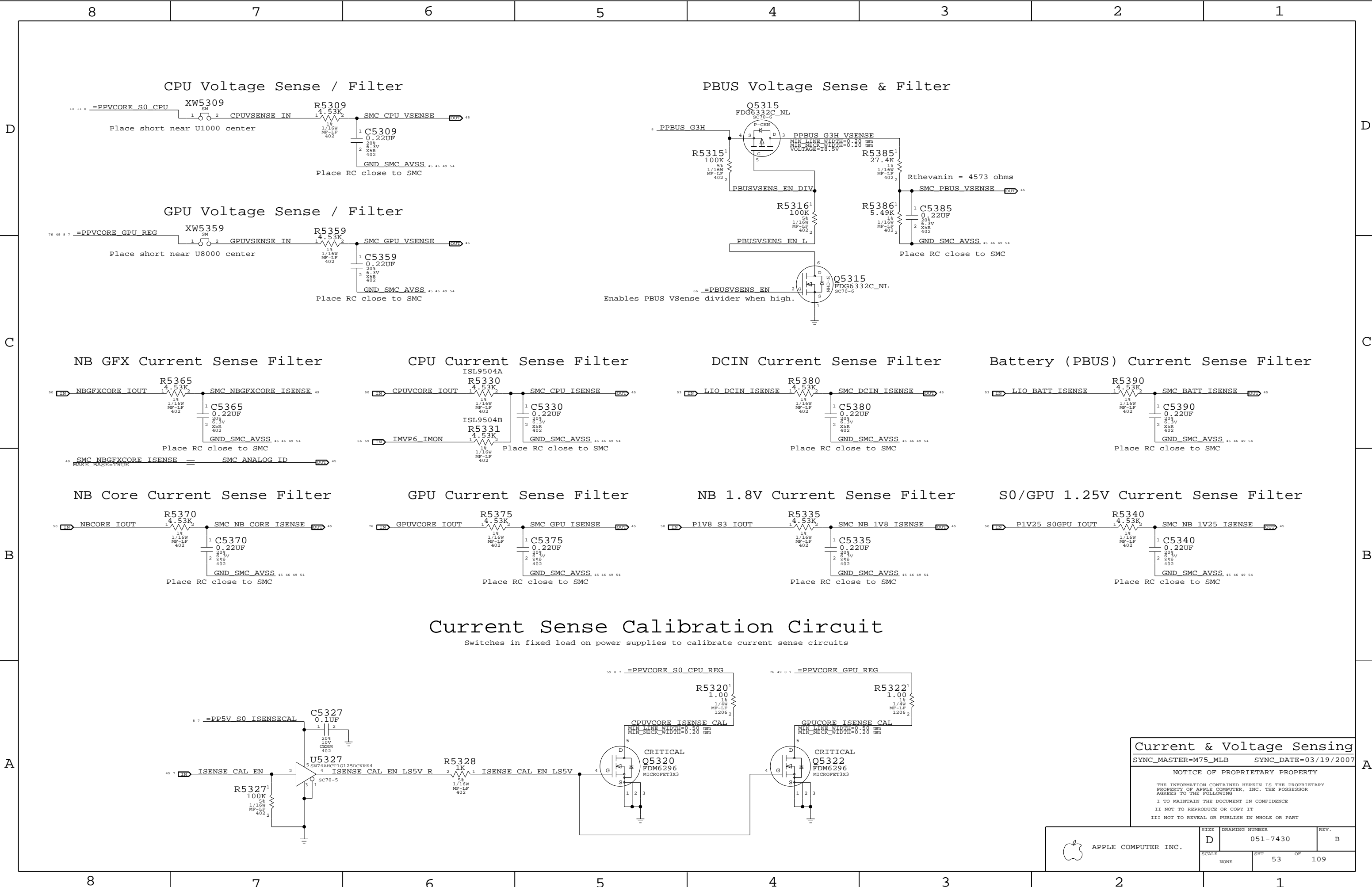
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7430	B
SCALE		SHT	OF
NONE		51	109



SMBus Connections		
SYNC_MASTER= (MASTER)		SYNC_DATE= (MASTER)
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 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7430	REV. B
	SCALE NONE	SHT 52	OF 109



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www.laptop-schematics.com

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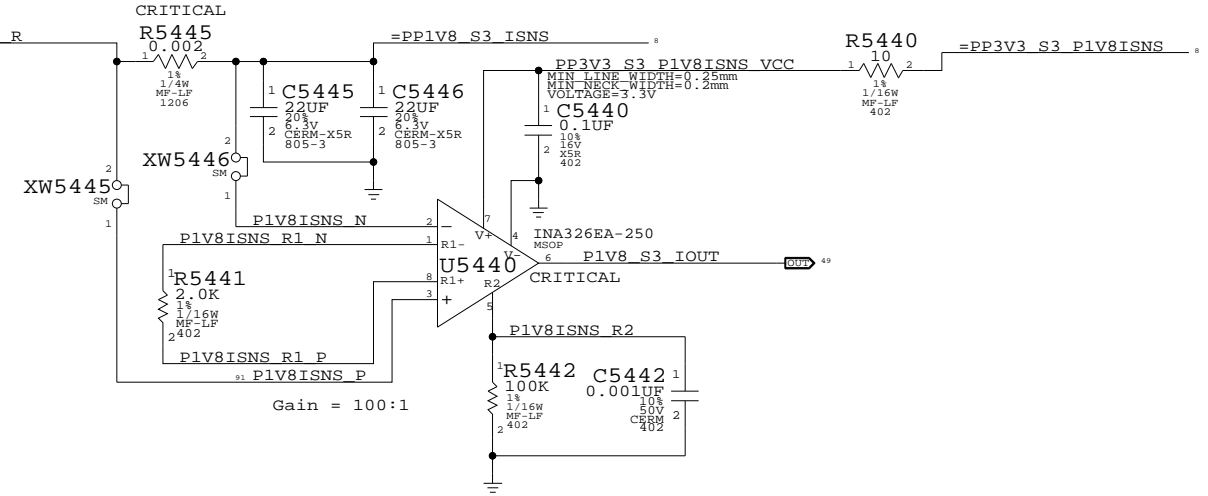
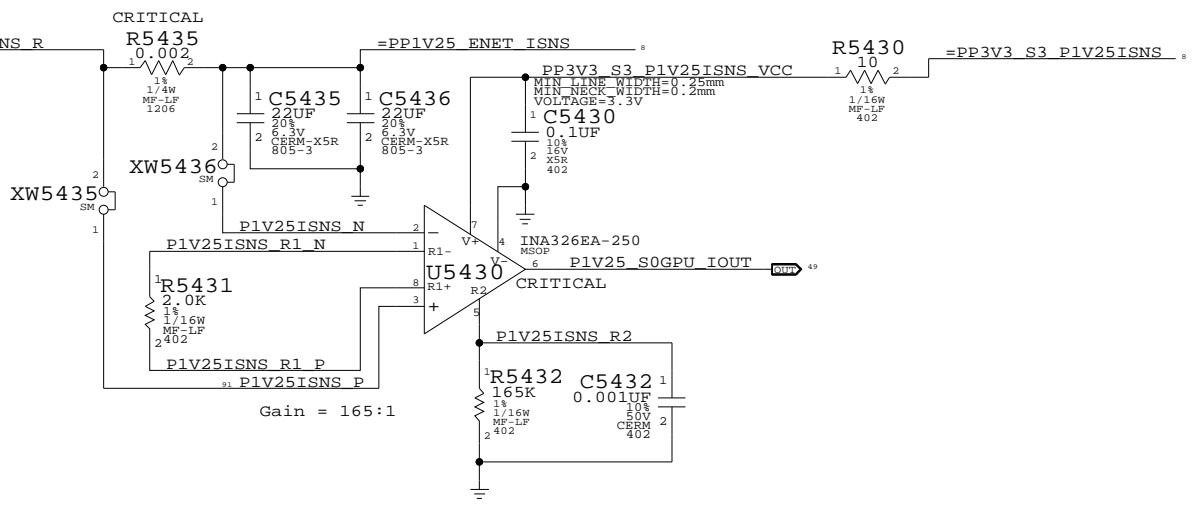
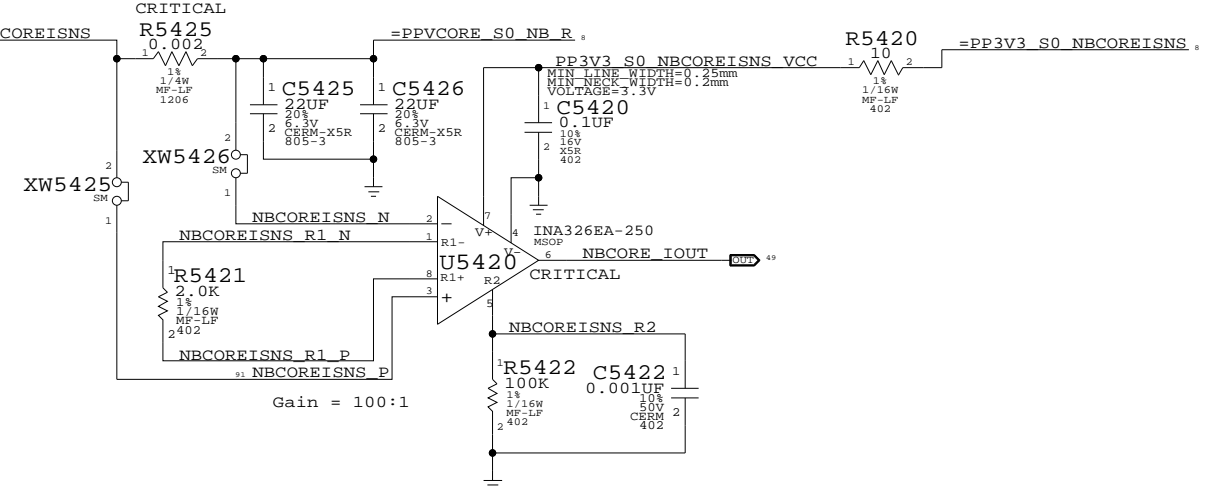
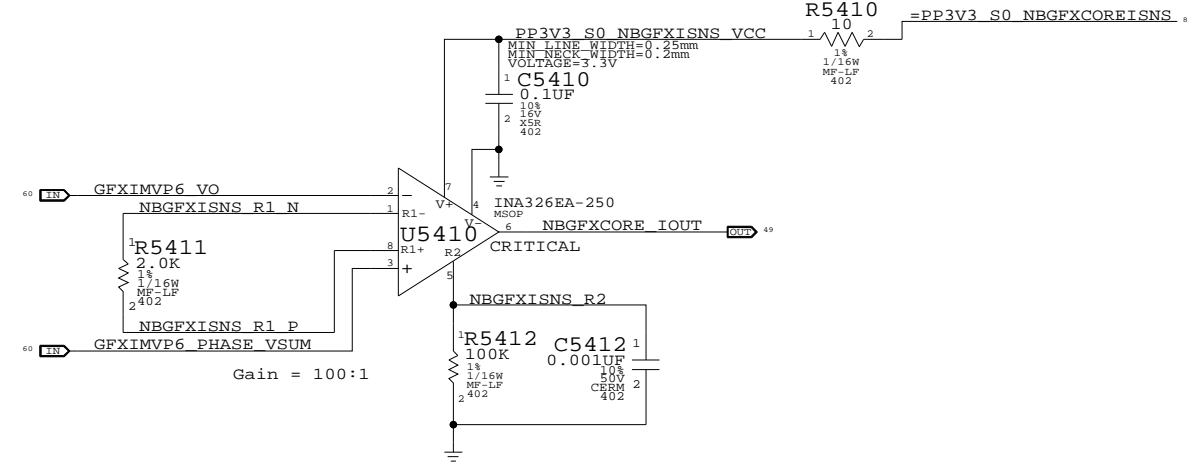
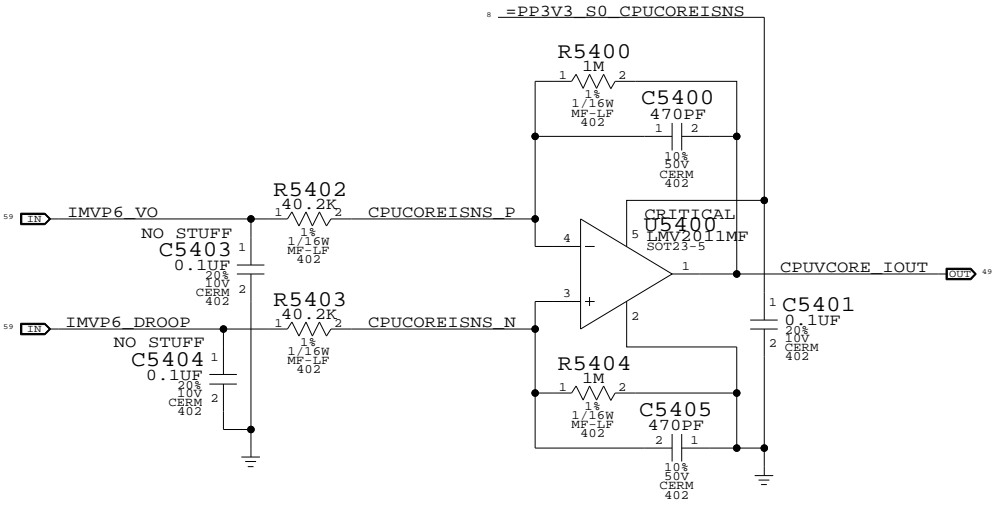
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Current Sensing

SYNC_MASTER=M75_MLB

SYNC_DATE=03/19/2007

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7430	B
SCALE		SHT	OF
NONE		54	109

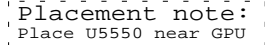
8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

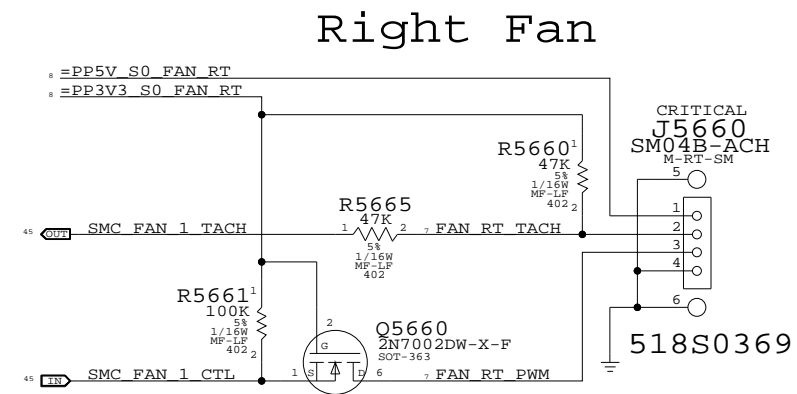
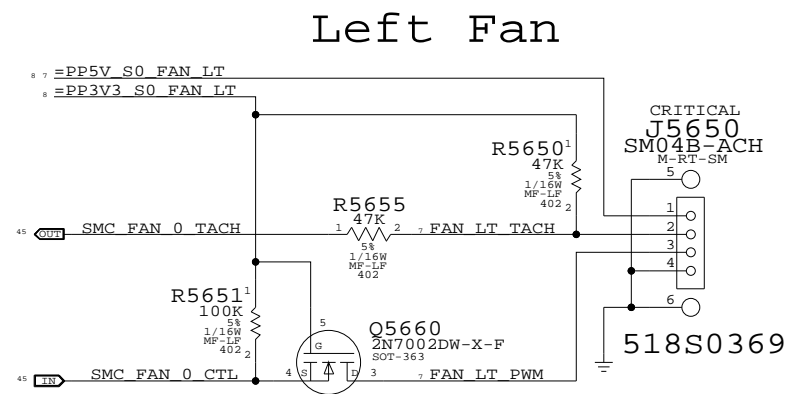


C

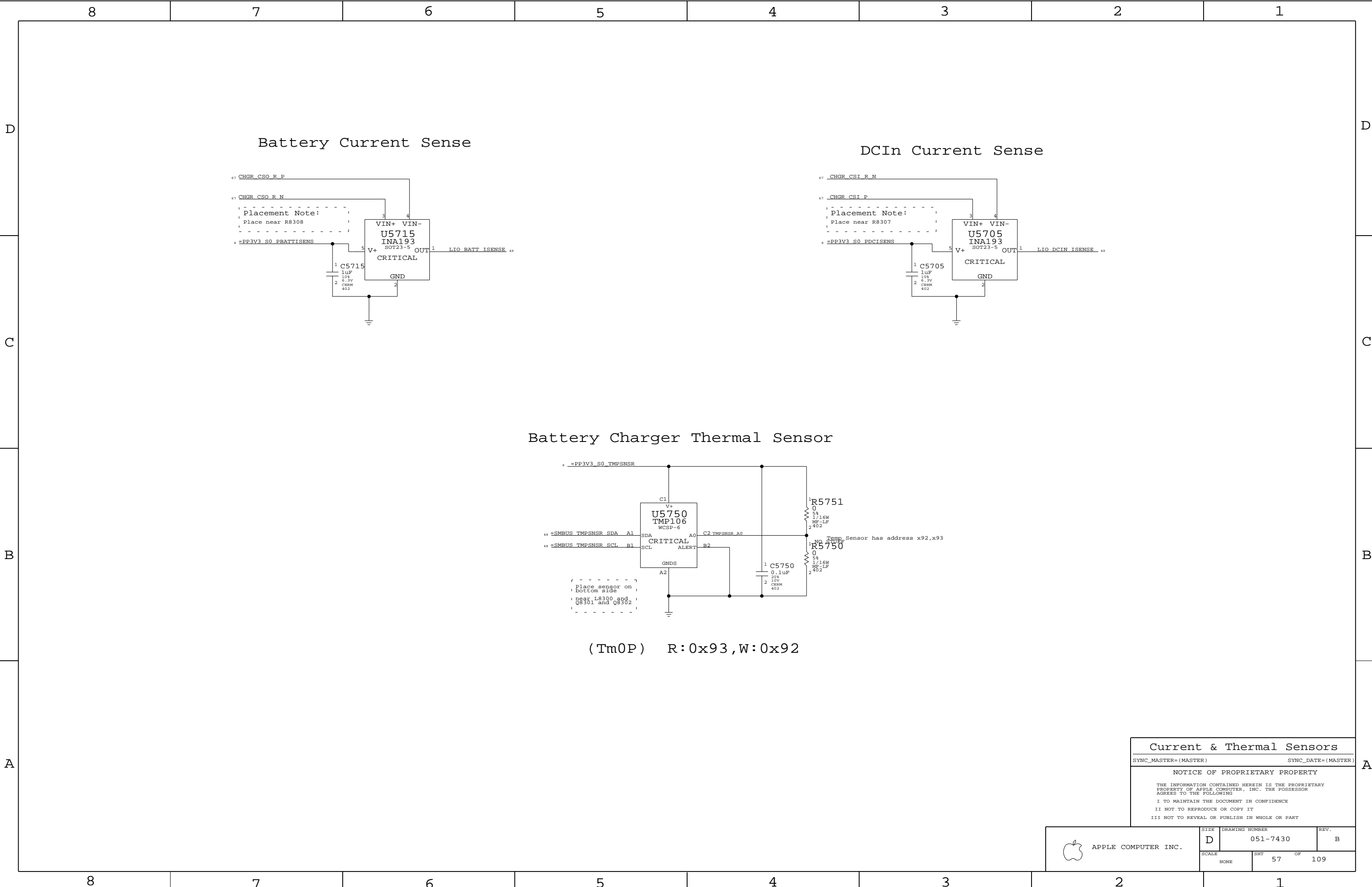


A





Fan Connectors			
SYNC_MASTER=M75_MLB		SYNC_DATE=12/04/2006	
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SIZE	DRAWING NUMBER		REV.
D	051-7430		B
SCALE		SHT	OF
NONE		56	109



Current & Thermal Sensors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7430	REV. B
	SCALE NONE	SHT 57	OF 109

D

C

B

A

D

C

B

A

8

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6

5

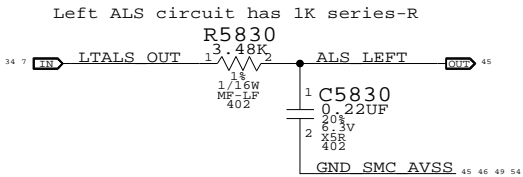
4

3

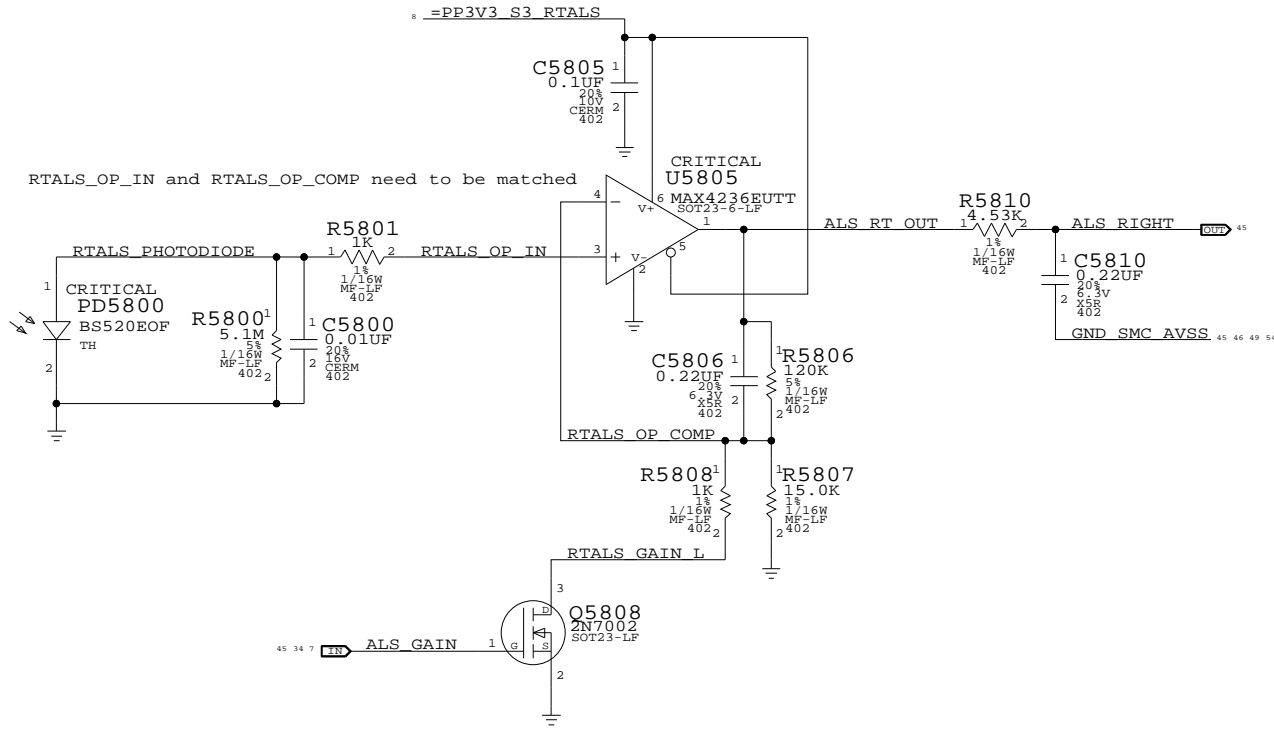
2

1

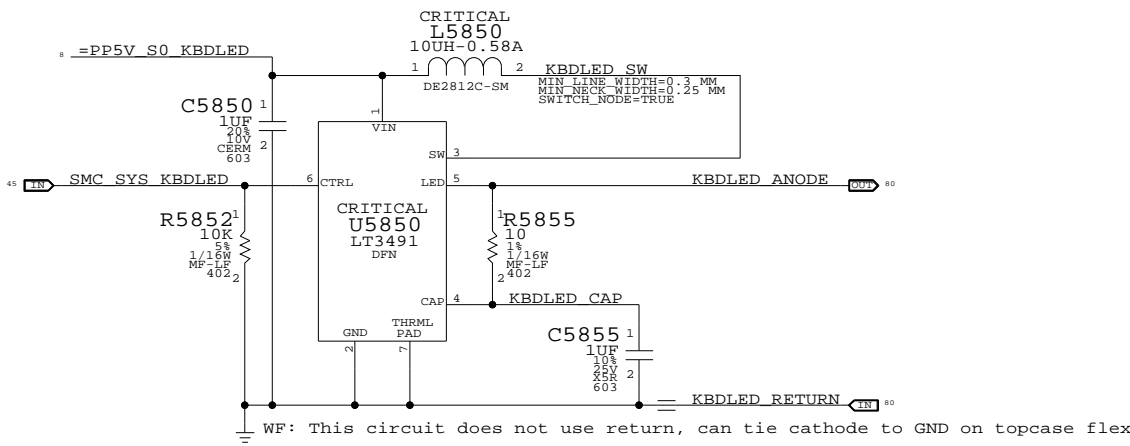
Left ALS Filter



Right ALS Circuit



Keyboard LED Driver



ALS Support

SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006

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APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-7430

REV.

B

SCALE

NONE

SHT

58

OF

109

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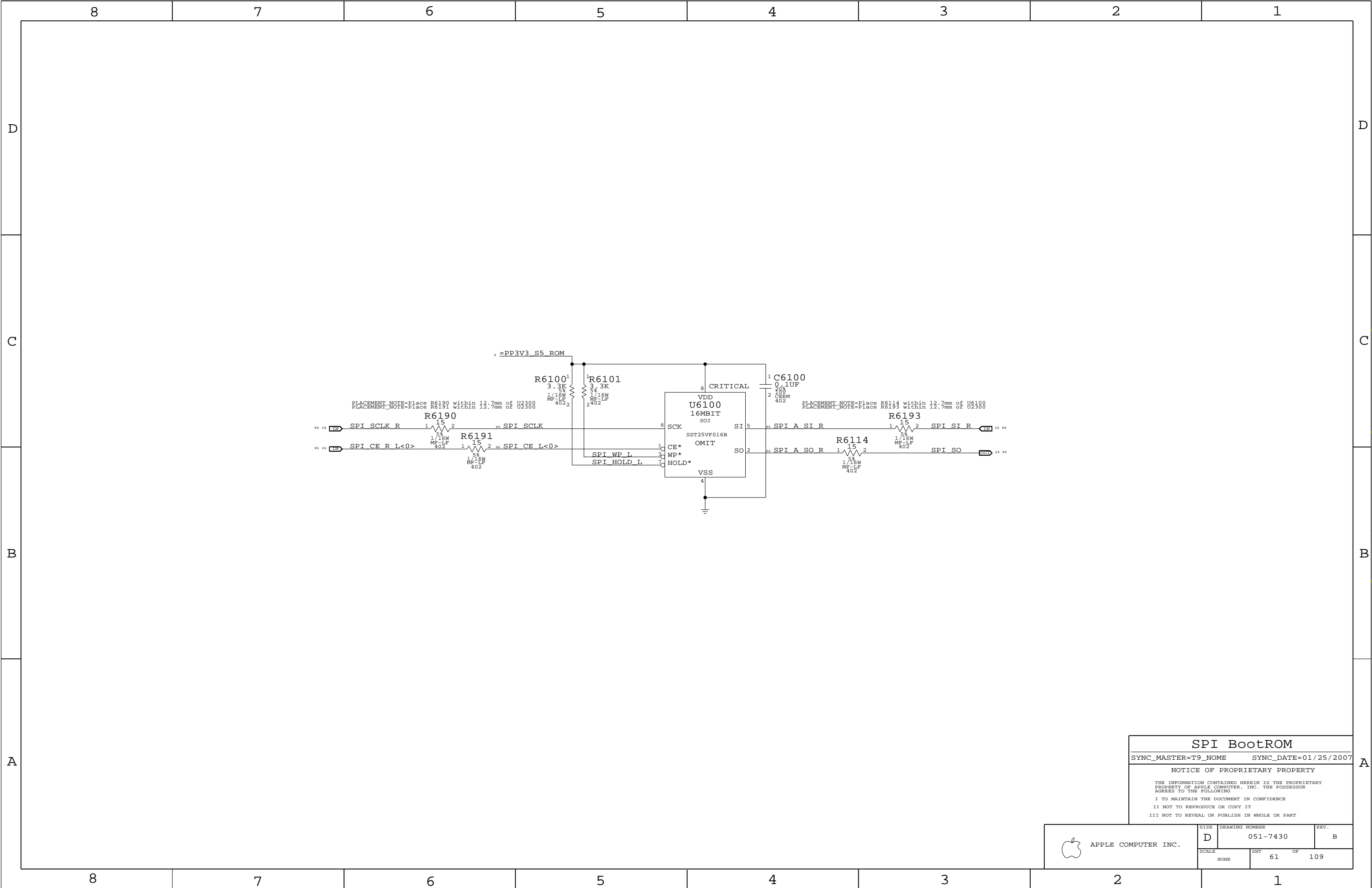
5

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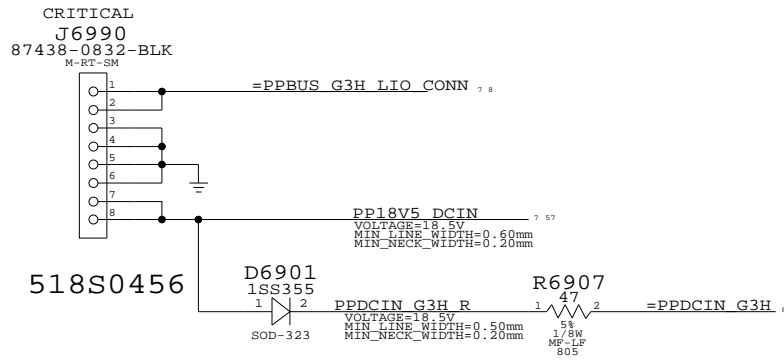
1



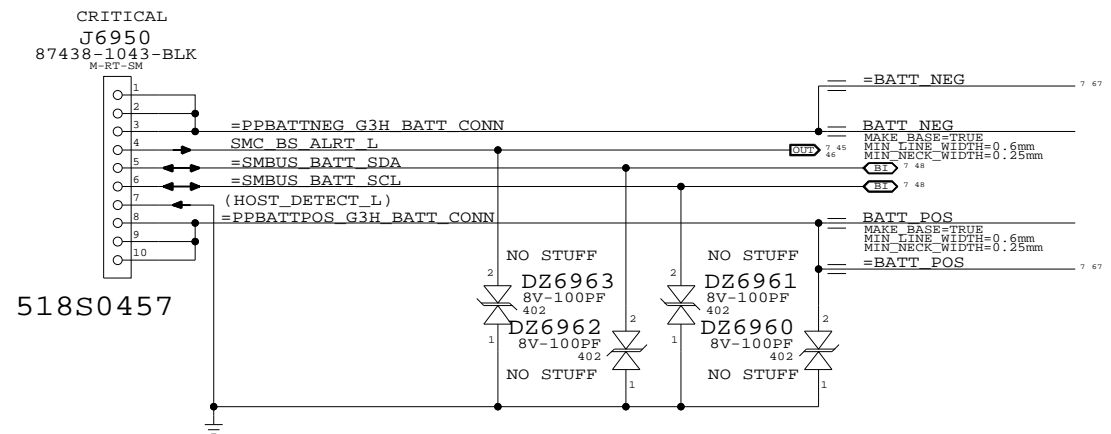
SPI BootROM		
SYNC_MASTER=T9_NOME	SYNC_DATE=01/25/2007	
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 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7430	REV. B
	SCALE NONE	SHT 61 OF 109	

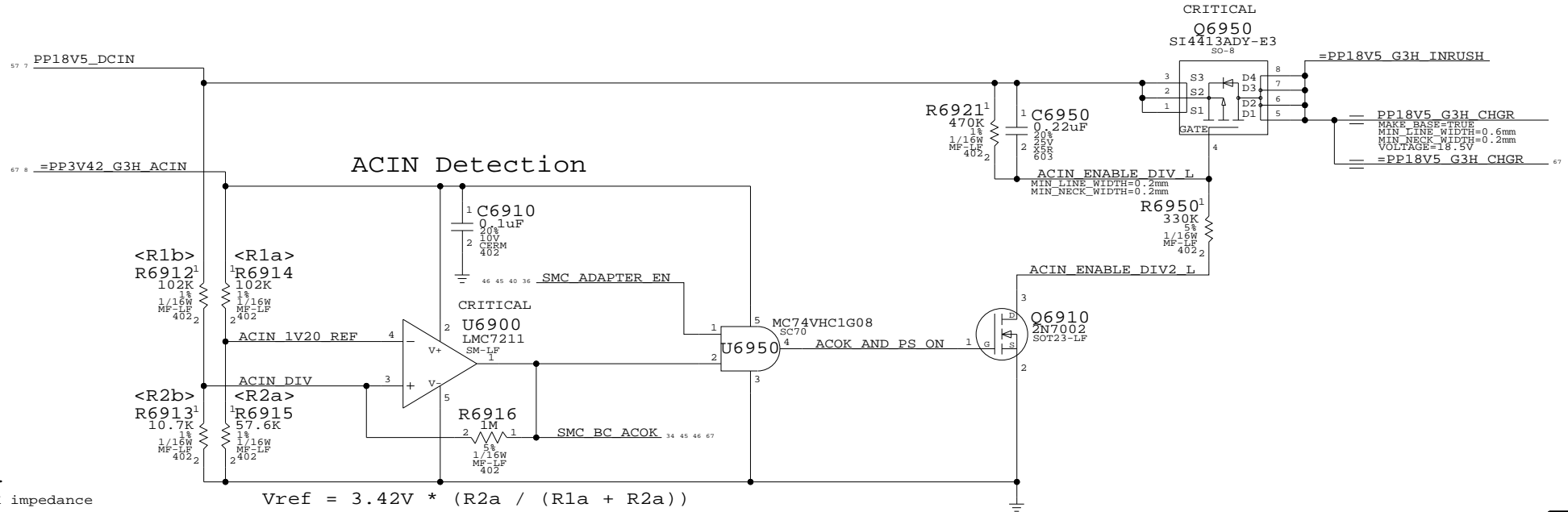
DC-In Connector



Battery Connector



Inrush Limiter

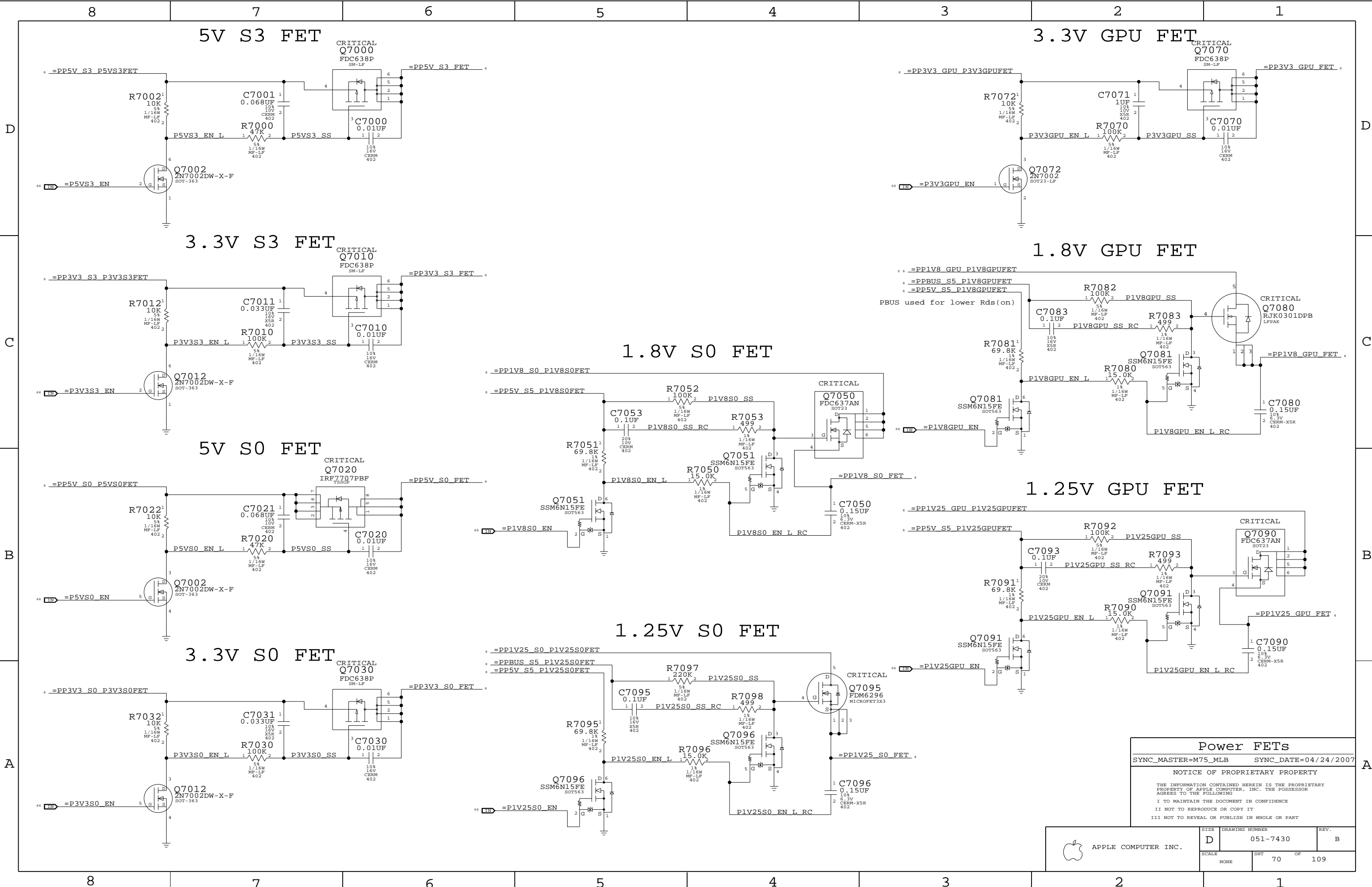


NOTE: R6910 is on LIO.
System must provide 10K-70K impedance
to A52 adapter for system load detection.
REQ of R6910 (on LIO), R6912, & R6913 is 36.9K.

$V_{ref} = 3.42V * (R2a / (R1a + R2a))$
 $V_{th} = (V_{ref} / (R2b / (R1b + R2b)))$
 $V_{ref} = 1.23V$
 $V_{th} = 13.0V$
Assuming 1% variance for R6910-R6915 and 3.42V:
Worst case V_{th} : min:12.47V, max: 13.54V

DC-In & Battery Connectors
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7430	REV. B
	SCALE NONE	SHT 69	OF 109

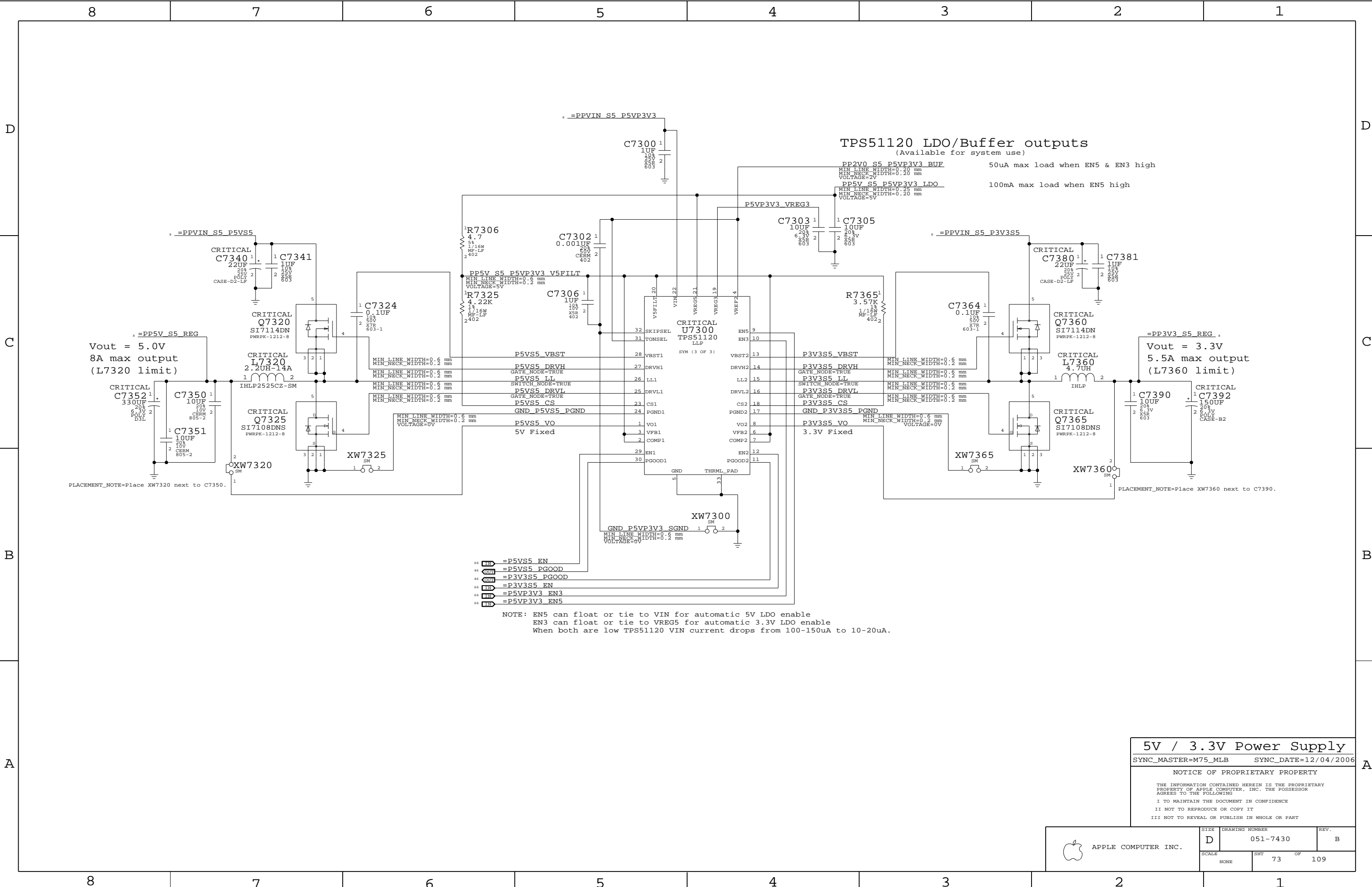


Power FETs
SYNC_MASTER=M75_MLB SYNC_DATE=04/24/2007
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7430	REV. B
	SCALE NONE	SHT 70	OF 109







5V / 3.3V Power Supply

SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006

NOTICE OF PROPRIETARY PROPERTY

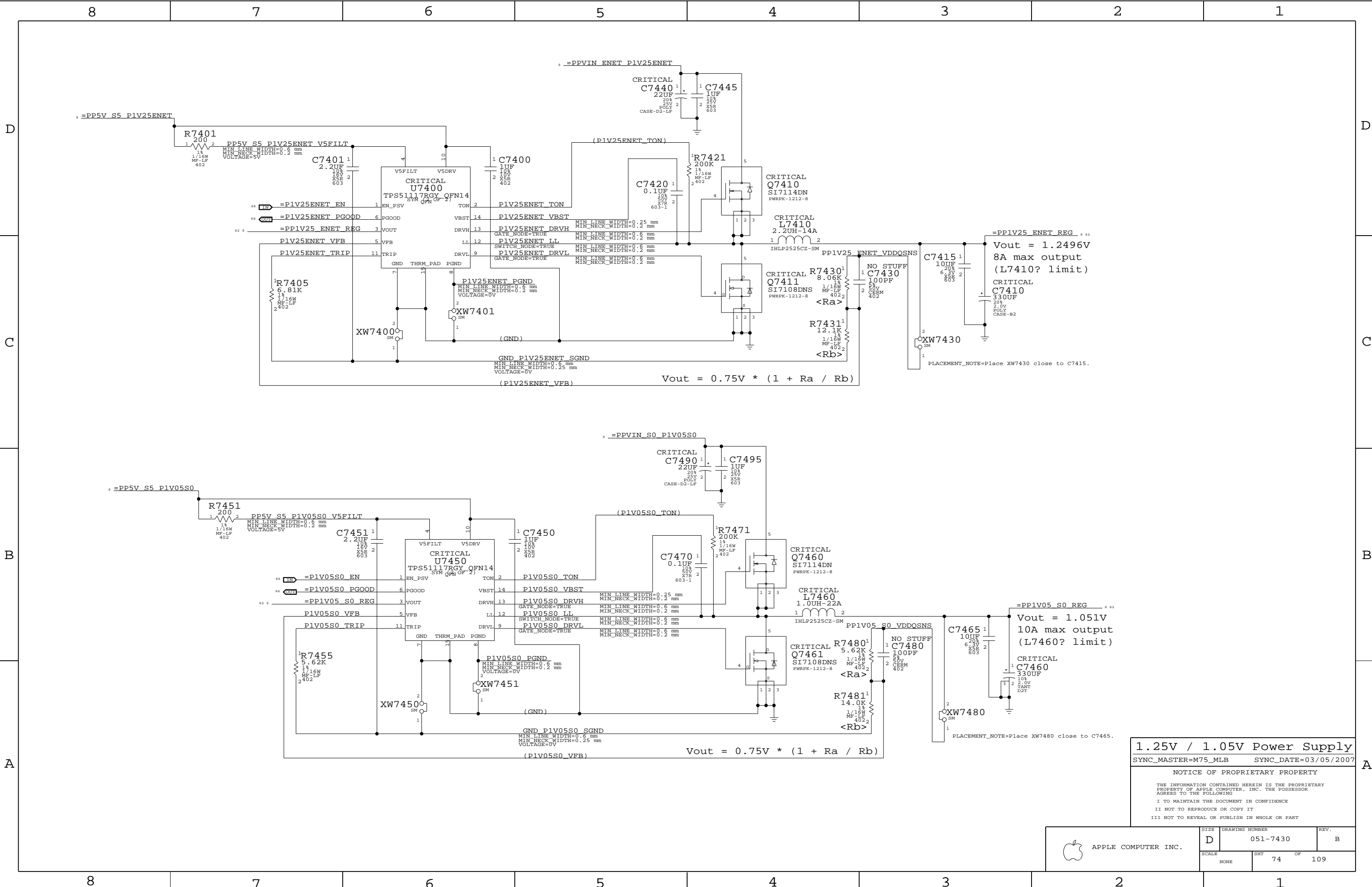
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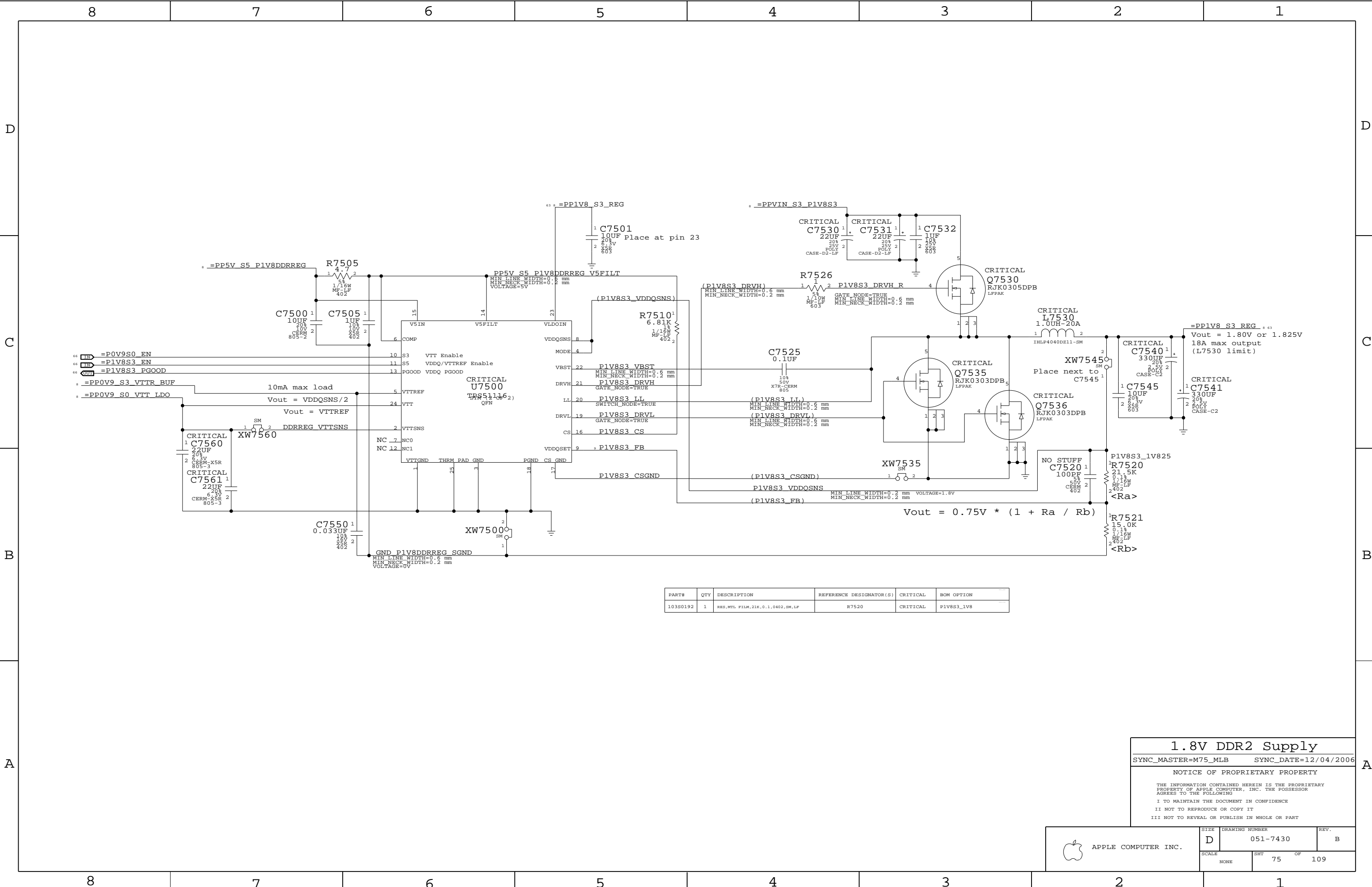
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7430	B
SCALE		SHT	OF
NONE		73	109



1.25V / 1.05V Power Supply
SYNC_MASTER=M75_MLB SYNC_DATE=03/05/2007

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7430	REV. B
	SCALE NONE	SHT 74	OF 109



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
103S0192	1	RES,MTL FILM,21K,0.1,0402,SM,LF	R7520	CRITICAL	PIV8S3_1V8

1.8V DDR2 Supply

SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006

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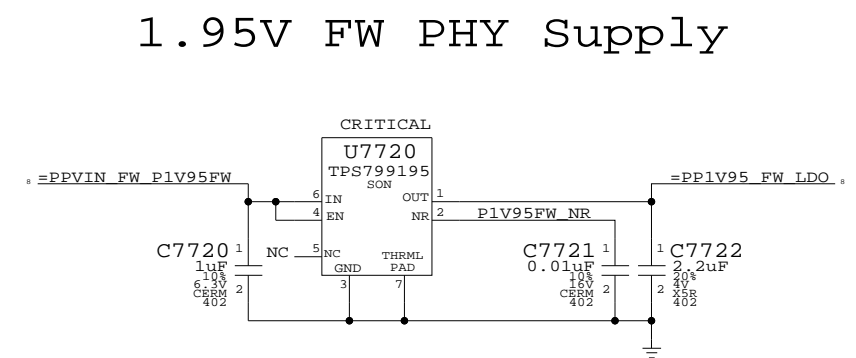
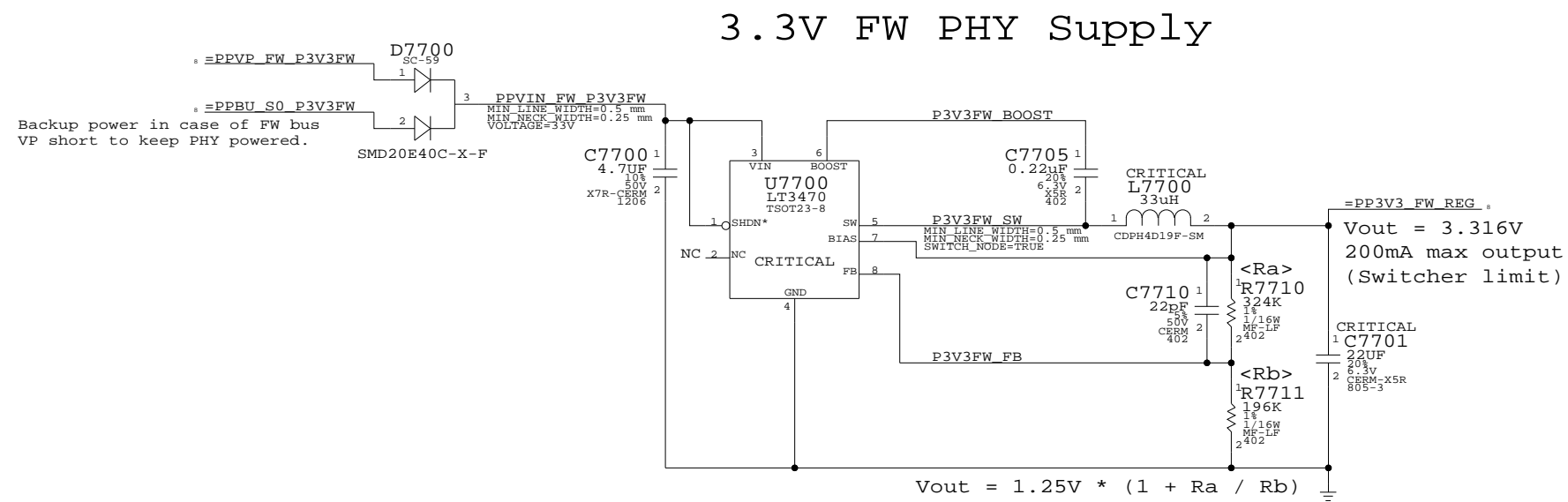
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APPLE COMPUTER INC.

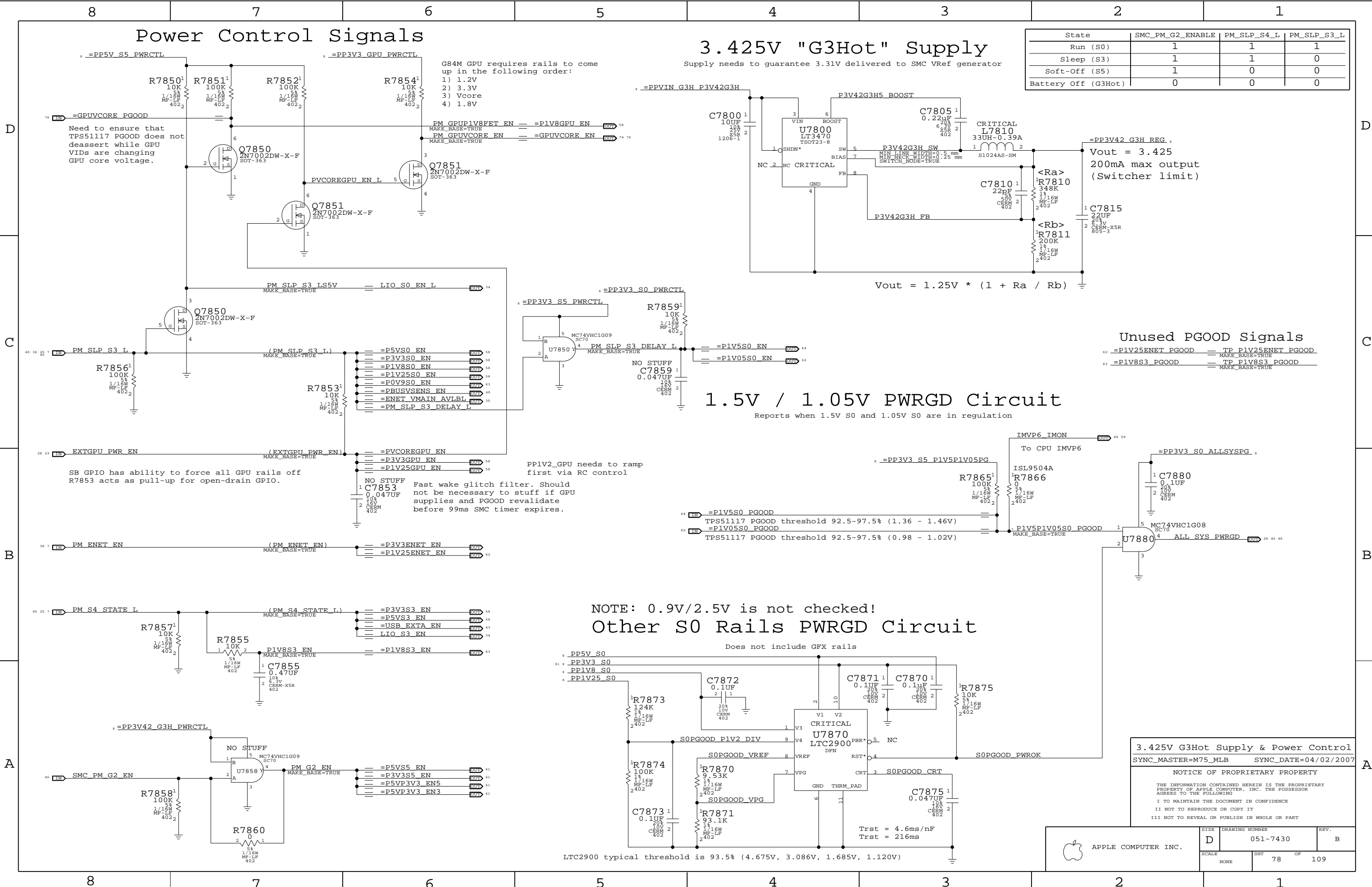
SIZE D DRAWING NUMBER 051-7430 REV. B

SCALE NONE SHT 75 OF 109



FW PHY Power Supplies	
SYNC_MASTER=M75_MLB	SYNC_DATE=12/04/2006
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 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7430	REV. B
	SCALE NONE	SHT OF 77 109	



State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

Vout = 3.425
200mA max output
(Switcher limit)

Unused PGOOD Signals

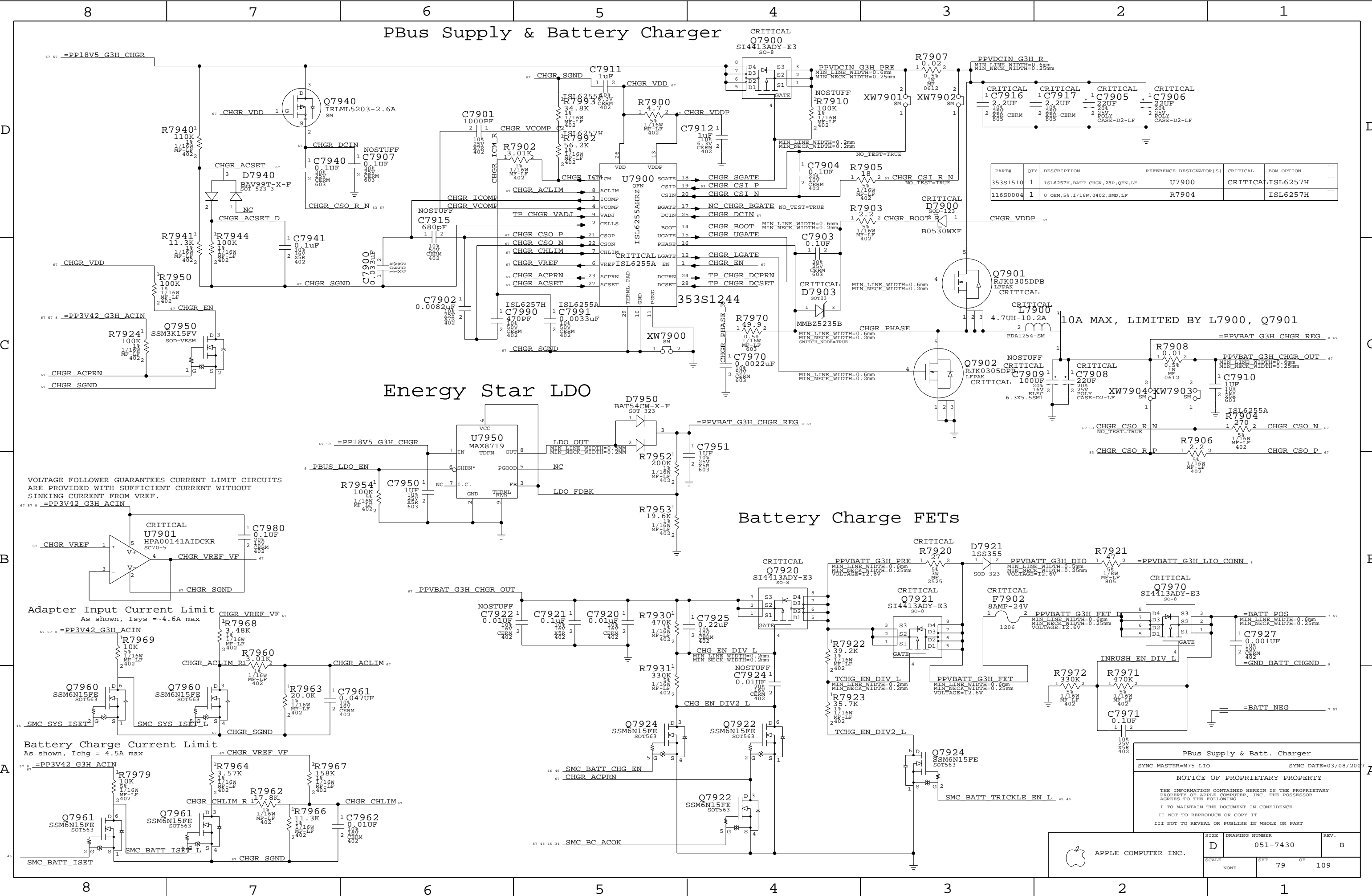
=P1V25ENET PGOOD	=TP P1V25ENET PGOOD
=P1V8S3 PGOOD	=TP P1V8S3 PGOOD

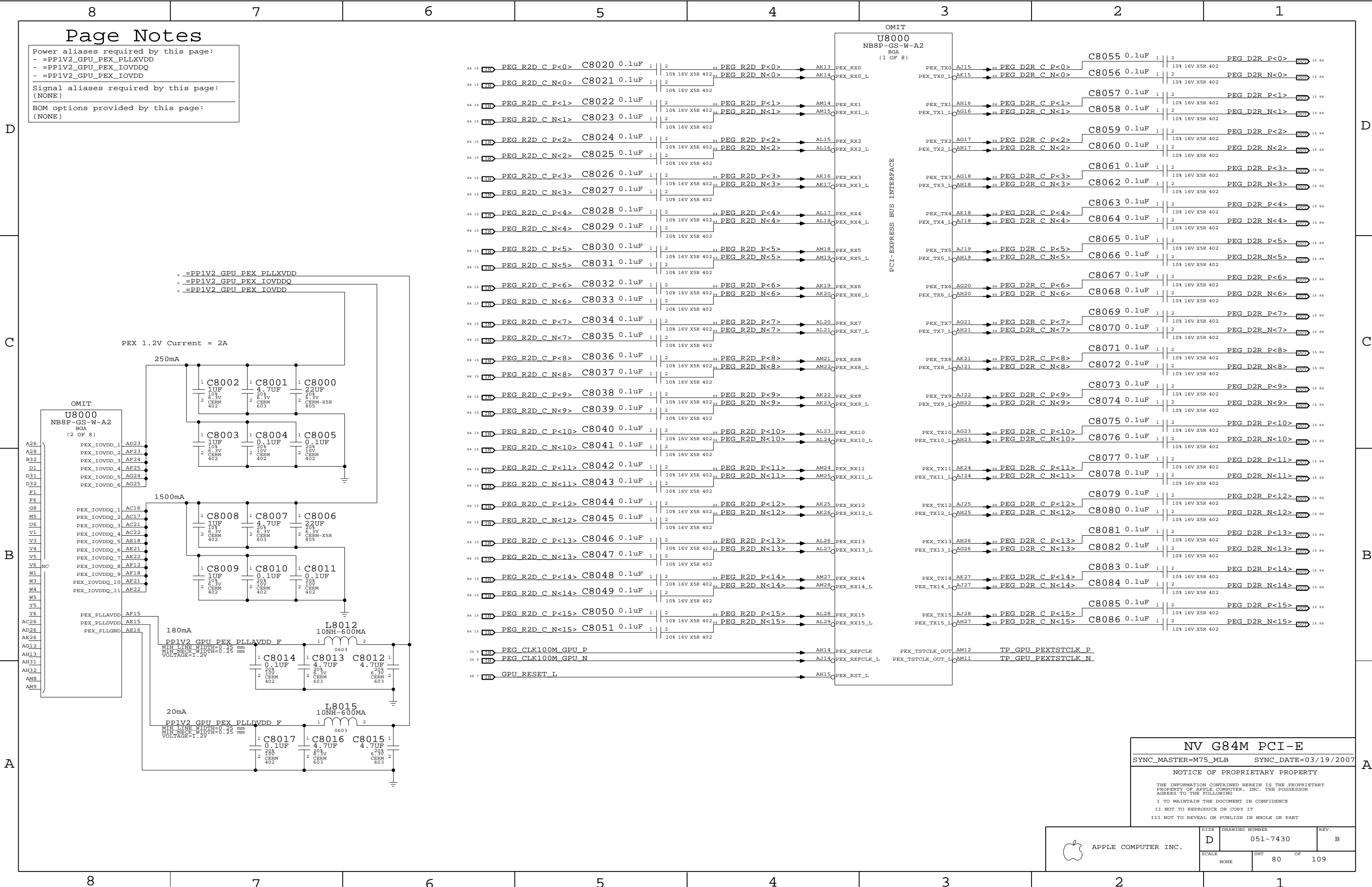
NOTE: 0.9V/2.5V is not checked!
Other S0 Rails PWRGD Circuit

3.425V G3Hot Supply & Power Control
SYNC_MASTER=M75_MLB SYNC_DATE=04/02/2007

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	D	051-7430	B
SCALE	NONE	SHT	78 OF 109





NV G84M PCI-E

SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

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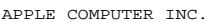
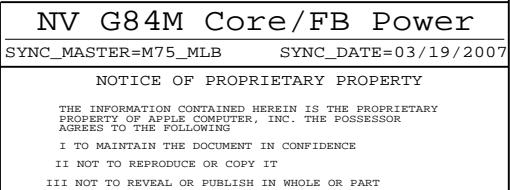
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7430	B
SCALE		SHT	OF
NONE		80	109


```
Power aliases required by this page:
    =PPVCORE_GPU
    -  =Pp1V8_GPU_FBVDDQ
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)
```

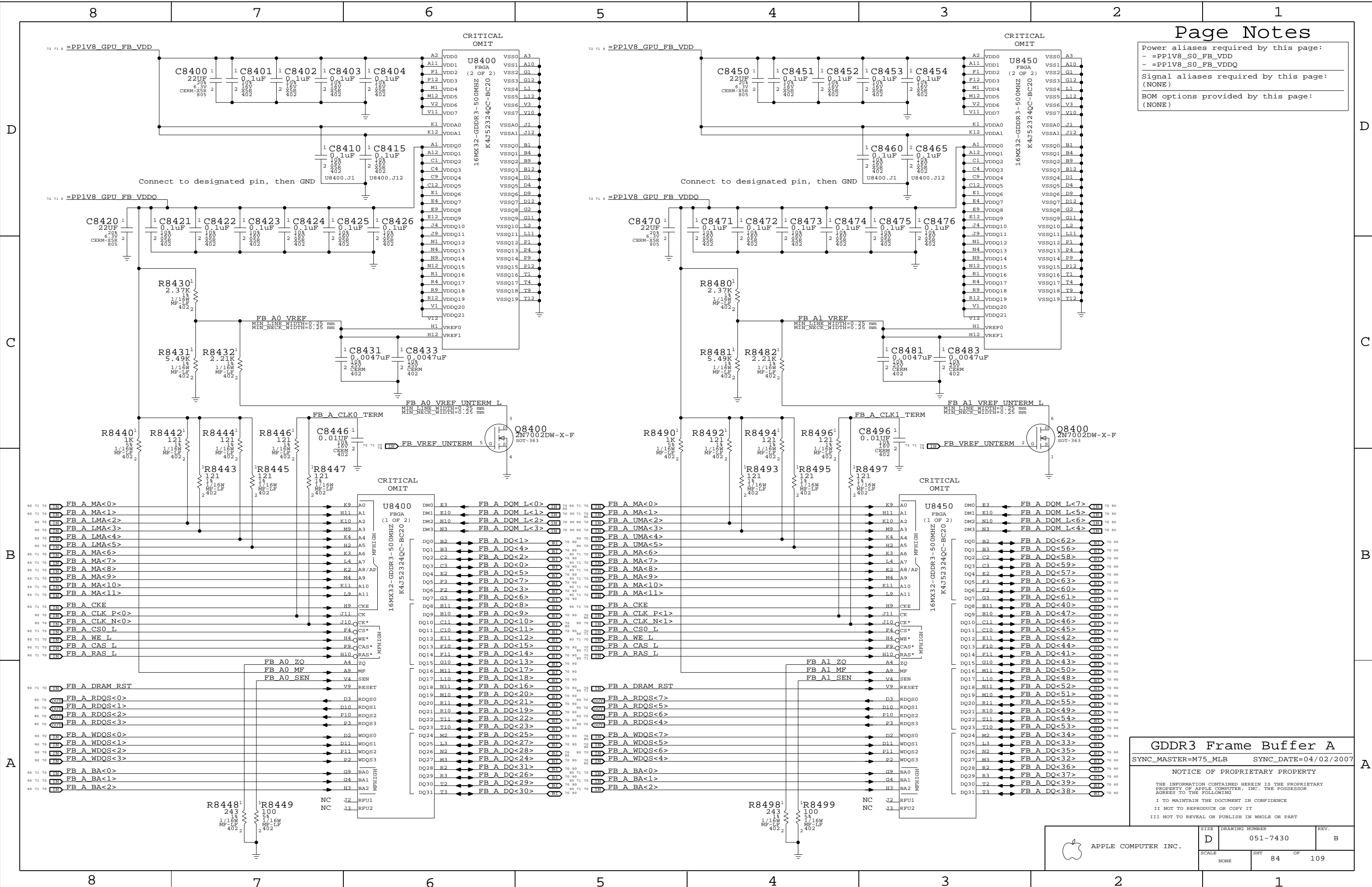


SIZE D	DRAWING NUMBER 051-7430	REV.
SCALE NONE	SHT 81	OF 109

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

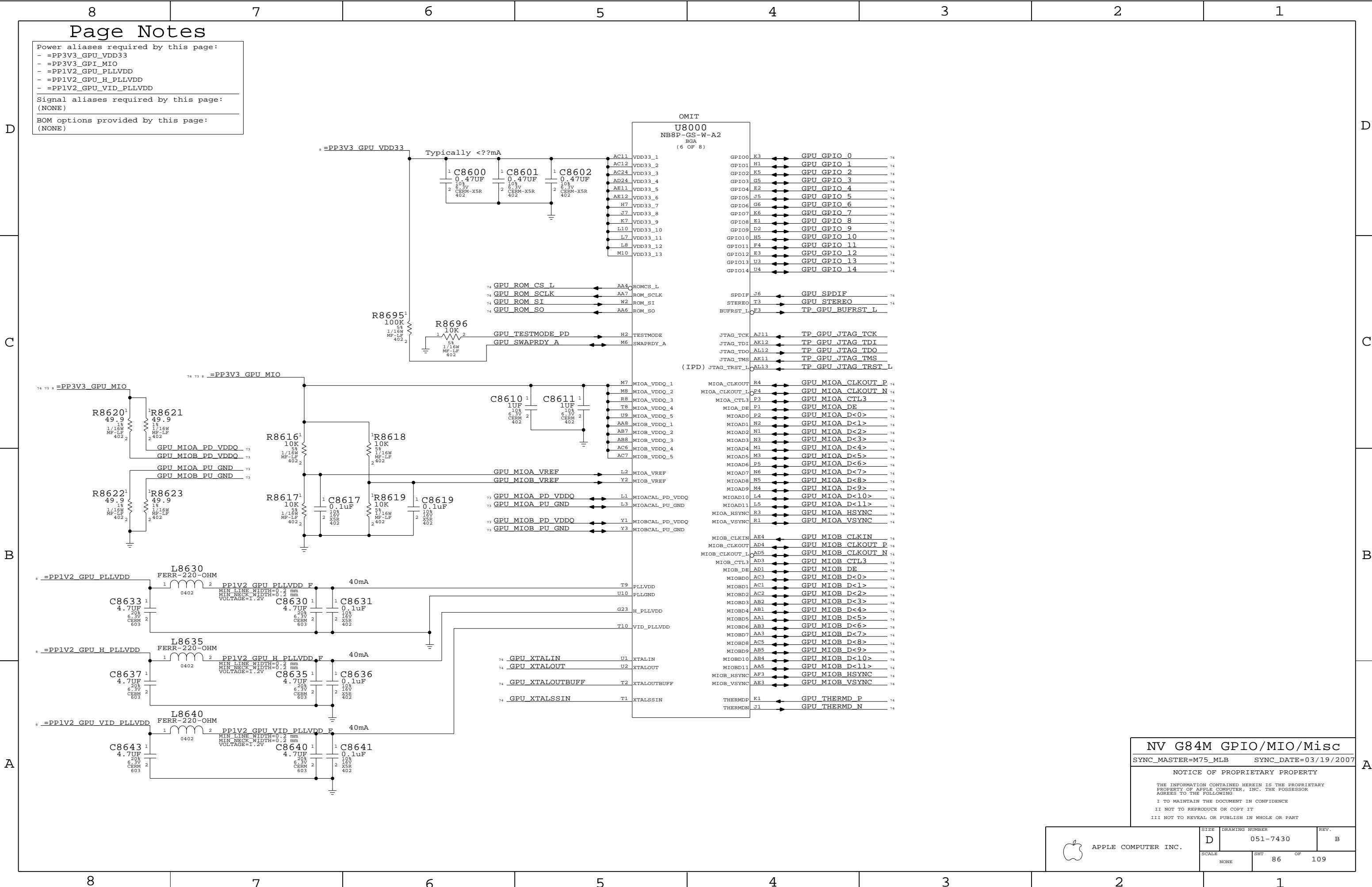
BOM options provided by this page:
(NONE)



GDDR3 Frame Buffer A
SYNC_MASTER=M75_MLB SYNC_DATE=04/02/2007

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Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP3V3_GPU_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NV G84M GPIO/MIO/Misc

SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

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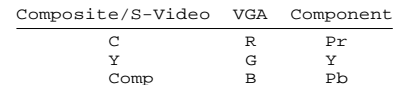
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7430	B
SCALE		SHT	OF
NONE		86	109


```
Power aliases required by this page:
- =PP1V8_GPU_IPFX
- =PP3V3_GPU_IPFCD_IOVDD
- =PP3V3_GPU_DAC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)
```




NOTICE OF PROPRIETARY PROPERTY

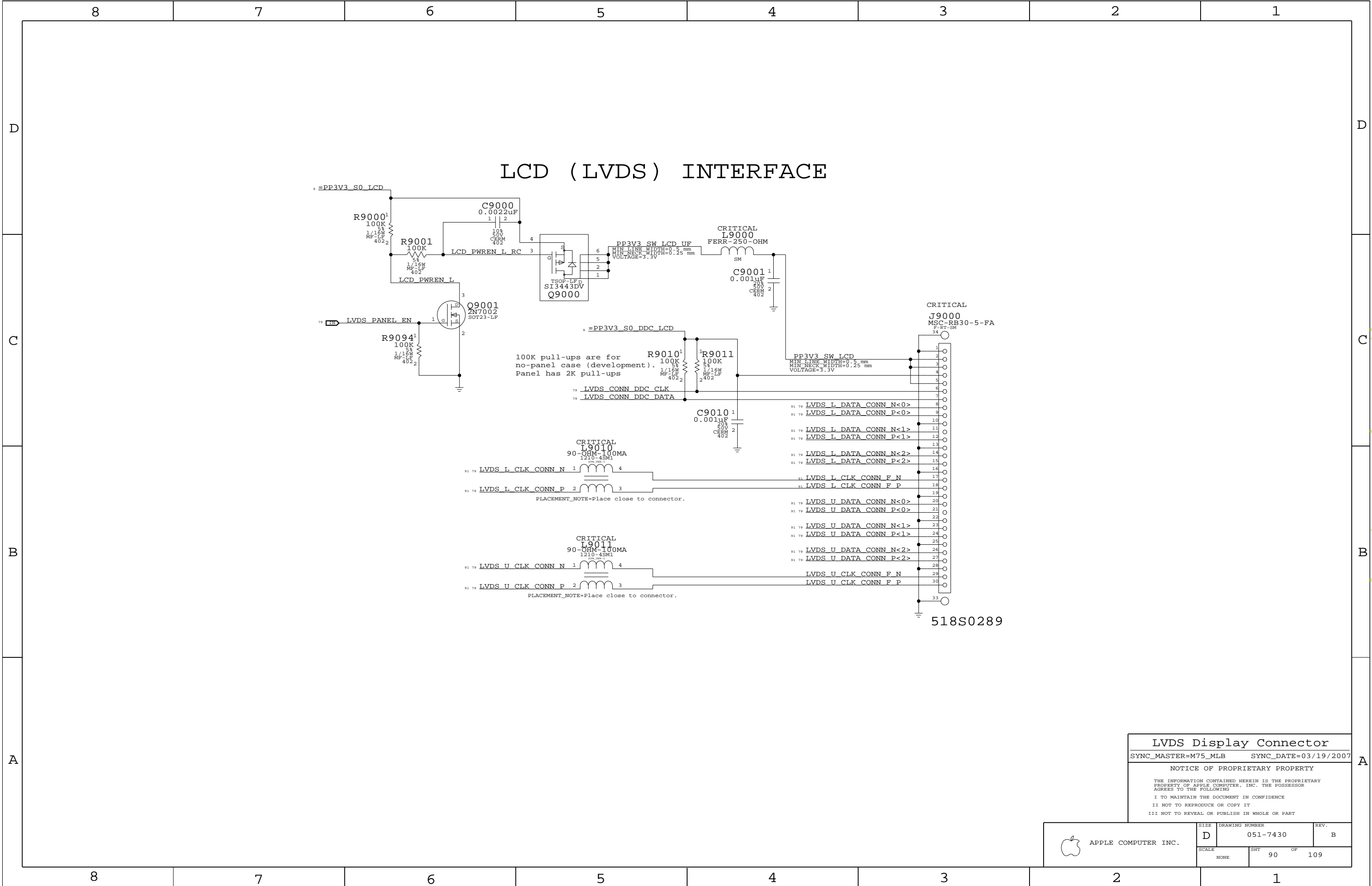
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	D	051-7430	B
	SCALE	SHT	OF
	NONE	88	109



LVDS Display Connector

SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

NOTICE OF PROPRIETARY PROPERTY

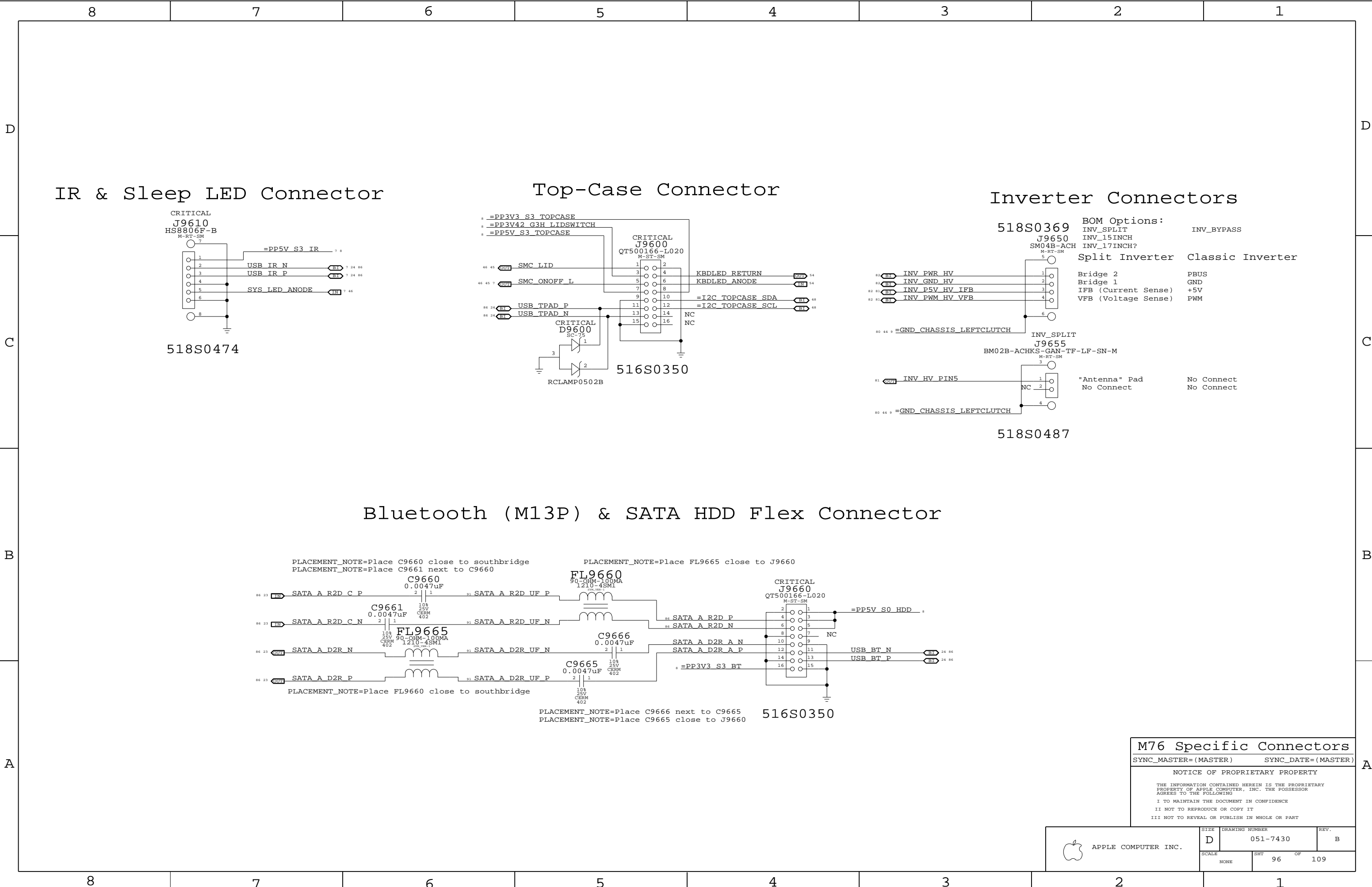
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7430	REV. B
	SCALE NONE	SHT 90	OF 109



IR & Sleep LED Connector

Top-Case Connector

Inverter Connectors

Bluetooth (M13P) & SATA HDD Flex Connector

M76 Specific Connectors

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

NOTICE OF PROPRIETARY PROPERTY

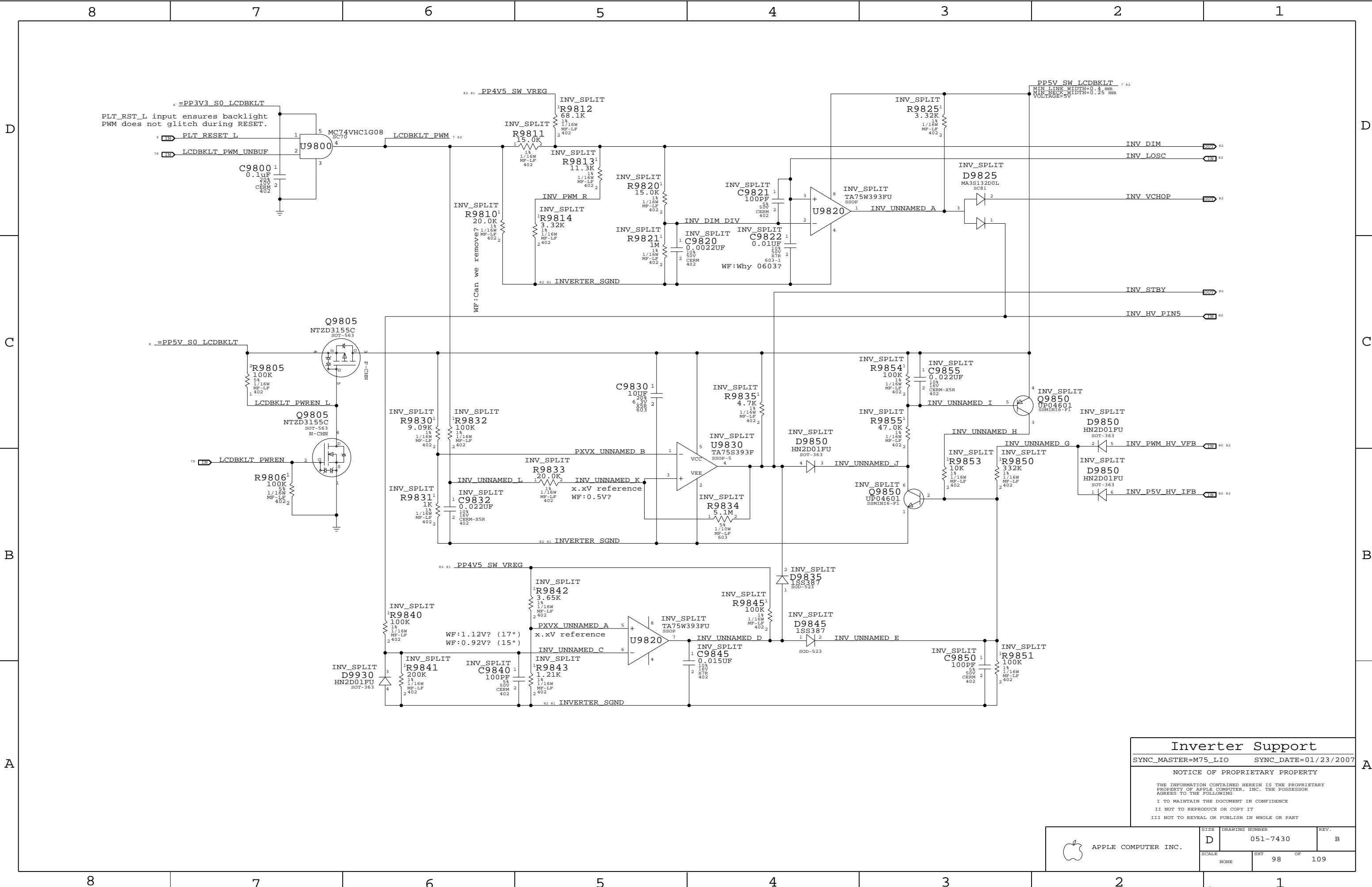
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	D	051-7430		B
SCALE		SHT	OF	REV.
NONE		96	109	



Inverter Support

SYNC_MASTER=M75_LIO SYNC_DATE=01/23/2007

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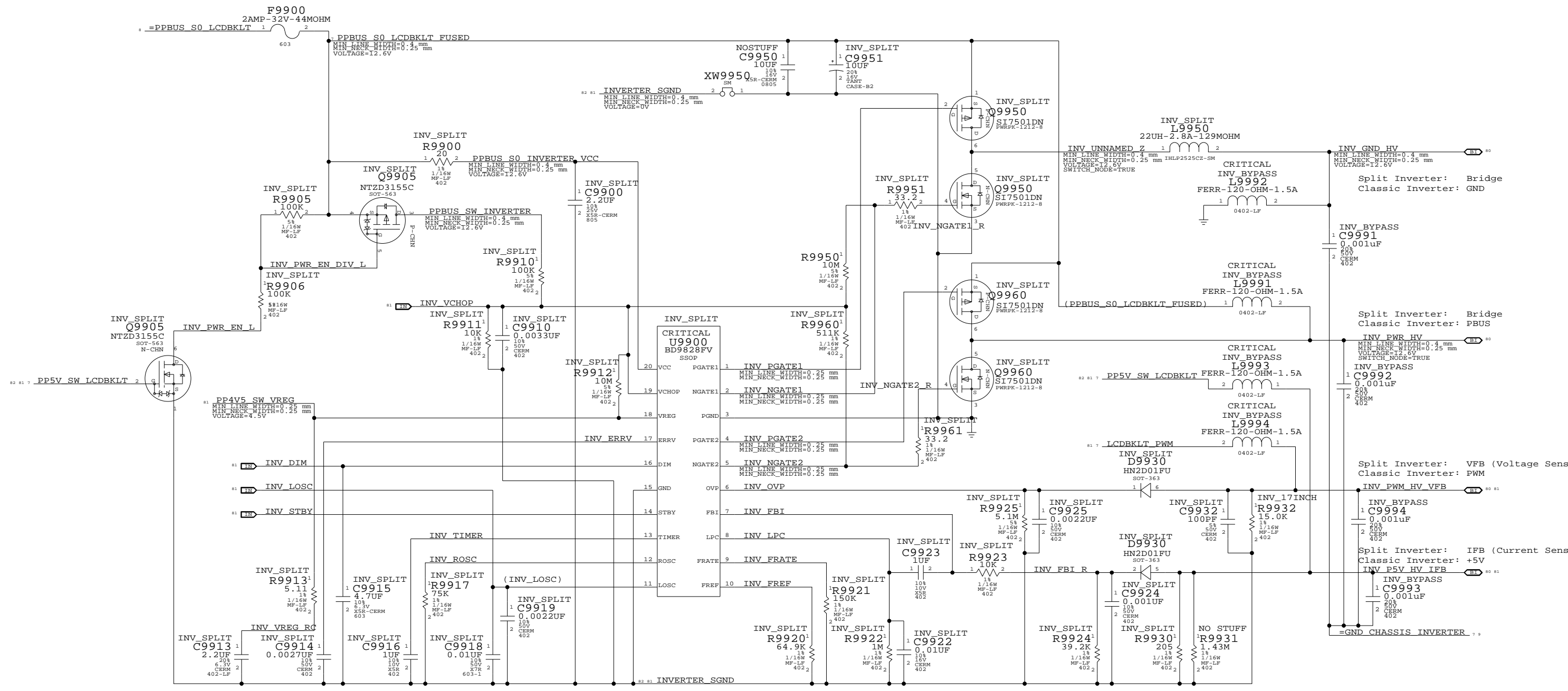
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	D	051-7430	B
SCALE		SHT	OF
NONE		98	109

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0319	1	RES,11.3K,1%,1/16W,MF,402,LF	R9932		INV_15INCH

Inverter Control IC

SYNC_MASTER=M75_LIO SYNC_DATE=01/23/2007

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NONE		99	109

8		7		6		5		4		3		2		1	
FSB (Front-Side Bus) Constraints															
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
FSB_55S		*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD							
FSB_DSTB_55S		*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR							
SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT						
FSB_ADDR		*	=3:1_SPACING	?	FSB_DATA		*	=3:1_SPACING	?						
FSB_ADDR2ADDR		*	=2:1_SPACING	?	FSB_DATA2DATA		*	=2:1_SPACING	?						
FSB_ADSTB		*	=3:1_SPACING	?	FSB_DSTB		*	=3:1_SPACING	?						
FSB_ADDR2ADSTB		*	=3:1_SPACING	?	FSB_DATA2DSTB		*	=3:1_SPACING	?						
SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT						
FSB_COMMON		*	=2:1_SPACING	?	FSB_COMMON		*	=2:1_SPACING	?						
NET_SPACING_TYPE1		NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	NET_SPACING_TYPE1		NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET						
FSB_ADDR		FSB_ADDR	*	FSB_ADDR2ADDR	FSB_ADDR		FSB_ADDR	*	FSB_ADDR2ADDR						
FSB_ADDR		FSB_ADSTB	*	FSB_ADDR2ADSTB	FSB_ADDR		FSB_ADSTB	*	FSB_ADDR2ADSTB						
FSB_DATA		FSB_DATA	*	FSB_DATA2DATA	FSB_DATA		FSB_DATA	*	FSB_DATA2DATA						
FSB_DATA		FSB_DSTB	*	FSB_DATA2DSTB	FSB_DATA		FSB_DSTB	*	FSB_DATA2DSTB						
All FSB signals with impedance requirements are 55-ohm single-ended. Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs. Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs. DSTB complementary pairs are spaced 1:1 and routed as differential pairs.															
Design Guide recommends each strobe/signal group is routed on the same layer. Design Guide recommends FSB signals be routed only on internal layers.															
NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.															
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.															
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3															
CPU Signal Constraints															
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
CPU_27P4S		*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL							
CPU_55S		*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD							
SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT						
CPU_2TO1		*	=2:1_SPACING	?	CPU_2TO1		*	=2:1_SPACING	?						
CPU_COMP		*	25 MIL	?	CPU_COMP		*	25 MIL	?						
CPU_GTLREF		*	25 MIL	?	CPU_GTLREF		*	25 MIL	?						
CPU_ITP		*	=2:1_SPACING	?	CPU_ITP		*	=2:1_SPACING	?						
CPU_VCCSENSE		*	25 MIL	?	CPU_VCCSENSE		*	25 MIL	?						
NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.															
Most CPU signals with impedance requirements are 55-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.															
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4															
CPU / FSB Net Properties															
ELECTRICAL_CONSTRAINT_SET		NET_TYPE		PHYSICAL	SPACING	ELECTRICAL_CONSTRAINT_SET		NET_TYPE		PHYSICAL	SPACING				
FSB_COMMON		FSB_55S		FSB_COMMON	FSB ADS L	FSB_COMMON		FSB_55S		FSB_COMMON	FSB ADS L	7 10 14			
FSB_COMMON		FSB_55S		FSB_COMMON	FSB BNR L	FSB_COMMON		FSB_55S		FSB_COMMON	FSB BNR L	7 10 14			
FSB_COMMON		FSB_55S		FSB_COMMON	FSB BPRI L	FSB_COMMON		FSB_55S		FSB_COMMON	FSB BPRI L	10 14			
FSB_COMMON		FSB_55S		FSB_COMMON	FSB BREQ0 L	FSB_COMMON		FSB_55S		FSB_COMMON	FSB BREQ0 L	7 10 14			
FSB_COMMON		FSB_55S		FSB_COMMON	FSB DBSY L	FSB_COMMON		FSB_55S		FSB_COMMON	FSB DBSY L	7 10 14			
FSB_COMMON		FSB_55S		FSB_COMMON	FSB DEFER L	FSB_COMMON		FSB_55S		FSB_COMMON	FSB DEFER L	10 14			
FSB_COMMON		FSB_55S		FSB_COMMON	FSB DPWR L	FSB_COMMON		FSB_55S		FSB_COMMON	FSB DPWR L	7 10 14			
FSB_COMMON		FSB_55S		FSB_COMMON	FSB DRDY L	FSB_COMMON		FSB_55S		FSB_COMMON	FSB DRDY L	7 10 14			
FSB_COMMON		FSB_55S		FSB_COMMON	FSB HIT L	FSB_COMMON		FSB_55S		FSB_COMMON	FSB HIT L	7 10 14			
FSB_COMMON		FSB_55S		FSB_COMMON	FSB HITM L	FSB_COMMON		FSB_55S		FSB_COMMON	FSB HITM L	7 10 14			
FSB_COMMON		FSB_55S		FSB_COMMON	FSB LOCK L	FSB_COMMON		FSB_55S		FSB_COMMON	FSB LOCK L	7 10 14			
FSB_COMMON		FSB_55S		FSB_COMMON	FSB RS L<2..0>	FSB_COMMON		FSB_55S		FSB_COMMON	FSB RS L<2..0>	10 14			
FSB_COMMON		FSB_55S		FSB_COMMON	FSB TRDY L	FSB_COMMON		FSB_55S		FSB_COMMON	FSB TRDY L	10 14			
FSB_CPURST_L		FSB_55S		FSB_COMMON	FSB CPURST L	FSB_CPURST_L		FSB_55S		FSB_COMMON	FSB CPURST L	7 10 13 14			
FSB_DATA_GROUP0		FSB_55S		FSB_DATA	FSB D L<15..0>	FSB_DATA_GROUP0		FSB_55S		FSB_DATA	FSB D L<15..0>	7 10 14			
FSB_DATA_GROUP0		FSB_55S		FSB_DATA	FSB DINV L<0>	FSB_DATA_GROUP0		FSB_55S		FSB_DATA	FSB DINV L<0>	7 10 14			
FSB_DSTB0		FSB_DSTB_55S		FSB_DSTB	FSB DSTB L P<0>	FSB_DSTB0		FSB_DSTB_55S		FSB_DSTB	FSB DSTB L P<0>	7 10 14			
FSB_DSTB_55S		FSB_DSTB		FSB_DSTB	FSB DSTB L N<0>	FSB_DSTB_55S		FSB_DSTB		FSB_DSTB	FSB DSTB L N<0>	7 10 14			
FSB_DATA_GROUP1		FSB_55S		FSB_DATA	FSB D L<31..16>	FSB_DATA_GROUP1		FSB_55S		FSB_DATA	FSB D L<31..16>	7 10 14			
FSB_DATA_GROUP1		FSB_55S		FSB_DATA	FSB DINV L<1>	FSB_DATA_GROUP1		FSB_55S		FSB_DATA	FSB DINV L<1>	7 10 14			
FSB_DSTB1		FSB_DSTB_55S		FSB_DSTB	FSB DSTB L P<1>	FSB_DSTB1		FSB_DSTB_55S		FSB_DSTB	FSB DSTB L P<1>	7 10 14			
FSB_DSTB_55S		FSB_DSTB		FSB_DSTB	FSB DSTB L N<1>	FSB_DSTB_55S		FSB_DSTB		FSB_DSTB	FSB DSTB L N<1>	7 10 14			
FSB_DATA_GROUP2		FSB_55S		FSB_DATA	FSB D L<47..32>	FSB_DATA_GROUP2		FSB_55S		FSB_DATA	FSB D L<47..32>	7 10 14			
FSB_DATA_GROUP2		FSB_55S		FSB_DATA	FSB DINV L<2>	FSB_DATA_GROUP2		FSB_55S		FSB_DATA	FSB DINV L<2>	7 10 14			
FSB_DSTB2		FSB_DSTB_55S		FSB_DSTB	FSB DSTB L P<2>	FSB_DSTB2		FSB_DSTB_55S		FSB_DSTB	FSB DSTB L P<2>	7 10 14			
FSB_DSTB_55S		FSB_DSTB		FSB_DSTB	FSB DSTB L N<2>	FSB_DSTB_55S		FSB_DSTB		FSB_DSTB	FSB DSTB L N<2>	7 10 14			
FSB_DATA_GROUP3		FSB_55S		FSB_DATA	FSB D L<63..48>	FSB_DATA_GROUP3		FSB_55S		FSB_DATA	FSB D L<63..48>	7 10 14			
FSB_DATA_GROUP3		FSB_55S		FSB_DATA	FSB DINV L<3>	FSB_DATA_GROUP3		FSB_55S		FSB_DATA	FSB DINV L<3>	7 10 14			
FSB_DSTB3		FSB_DSTB_55S		FSB_DSTB	FSB DSTB L P<3>	FSB_DSTB3		FSB_DSTB_55S		FSB_DSTB	FSB DSTB L P<3>	7 10 14			
FSB_DSTB_55S		FSB_DSTB		FSB_DSTB	FSB DSTB L N<3>	FSB_DSTB_55S		FSB_DSTB		FSB_DSTB	FSB DSTB L N<3>	7 10 14			
FSB_ADDR_GROUP0		FSB_55S		FSB_ADDR	FSB A L<16..3>	FSB_ADDR_GROUP0		FSB_55S		FSB_ADDR	FSB A L<16..3>	7 10 14			
FSB_ADDR_GROUP0		FSB_55S		FSB_ADDR	FSB REQ L<4..0>	FSB_ADDR_GROUP0		FSB_55S		FSB_ADDR	FSB REQ L<4..0>	7 10 14			
FSB_ADSTB0		FSB_55S		FSB_ADSTB	FSB ADSTB L<0>	FSB_ADSTB0		FSB_55S		FSB_ADSTB	FSB ADSTB L<0>	7 10 14			
FSB_ADDR_GROUP1		FSB_55S		FSB_ADDR	FSB A L<35..17>	FSB_ADDR_GROUP1		FSB_55S		FSB_ADDR	FSB A L<35..17>	7 10 14			
FSB_ADSTB1		FSB_55S		FSB_ADSTB	FSB ADSTB L<1>	FSB_ADSTB1		FSB_55S		FSB_ADSTB	FSB ADSTB L<1>	7 10 14			
CPU_IERR_L		CPU_55S			CPU IERR L	CPU_IERR_L		CPU_55S			CPU IERR L	10			
CPU_FERR_L		CPU_55S			CPU FERR L	CPU_FERR_L		CPU_55S			CPU FERR L	10 23			
CPU_PROCHOT_L		CPU_55S		CPU_2TO1	CPU PROCHOT L	CPU_PROCHOT_L		CPU_55S		CPU_2TO1	CPU PROCHOT L	10 46 59			
CPU_PWRGD		CPU_55S			CPU PWRGD	CPU_PWRGD		CPU_55S			CPU PWRGD	7 10 13 23			
CPU_FROM_SB		CPU_55S			CPU INTR	CPU_FROM_SB		CPU_55S			CPU INTR	10 23			
CPU_FROM_SB		CPU_55S			CPU NMI	CPU_FROM_SB		CPU_55S			CPU NMI	10 23			
CPU_FROM_SB		CPU_55S			CPU A20M L	CPU_FROM_SB		CPU_55S			CPU A20M L	10 23			
CPU_FROM_SB		CPU_55S			CPU DPSLP L	CPU_FROM_SB		CPU_55S			CPU DPSLP L	7 10 23			
CPU_FROM_SB		CPU_55S			CPU IGNNE L	CPU_FROM_SB		CPU_55S			CPU IGNNE L	10 23			
CPU_INIT_L		CPU_55S			CPU INIT L	CPU_INIT_L		CPU_55S			CPU INIT L	10 23 47			
CPU_FROM_SB		CPU_55S			CPU SMI L	CPU_FROM_SB		CPU_55S			CPU SMI L	10 23			
CPU_FROM_SB		CPU_55S			CPU STPCLK L	CPU_FROM_SB		CPU_55S			CPU STPCLK L	7 10 23			
PM_THRMTRIP_L		CPU_55S		CPU_2TO1	PM THRMTRIP L	PM_THRMTRIP_L		CPU_55S		CPU_2TO1	PM THRMTRIP L	10 16 23 46			
FSB_CPUSLP_L		CPU_55S			FSB CPUSLP L	FSB_CPUSLP_L		CPU_55S			FSB CPUSLP L	7 10 14			
PM DPRSLPVR		CPU_55S		CPU_2TO1	PM DPRSLPVR	PM DPRSLPVR		CPU_55S		CPU_2TO1	PM DPRSLPVR	7 16 25 59			
(See above)		CPU_55S		CPU_2TO1	IMVP DPRSLPVR	(See above)		CPU_55S		CPU_2TO1	IMVP DPRSLPVR	7 59			
CPU_BSEL0		CPU_55S		CPU_2TO1	CPU BSEL<0>	CPU_BSEL0		CPU_55S		CPU_2TO1	CPU BSEL<0>	10 30			
(See above)		CPU_55S		CPU_2TO1	NB BSEL<0>	(See above)		CPU_55S		CPU_2TO1	NB BSEL<0>	13 16 30			
CPU_BSEL1		CPU_55S		CPU_2TO1	CPU BSEL<1>	CPU_BSEL1		CPU_55S		CPU_2TO1	CPU BSEL<1>	10 30			
(See above)		CPU_55S		CPU_2TO1	NB BSEL<1>	(See above)		CPU_55S		CPU_2TO1	NB BSEL<1>	13 16 30			
CPU_BSEL2		CPU_55S		CPU_2TO1	CPU BSEL<2>	CPU_BSEL2		CPU_55S		CPU_2TO1	CPU BSEL<2>	10 30			
(See above)		CPU_55S		CPU_2TO1	NB BSEL<2>	(See above)		CPU_55S		CPU_2TO1	NB BSEL<2>	13 16 30			
CPU DPRSTP_L		CPU_55S		CPU_2TO1	CPU DPRSTP L	CPU_DPRSTP_L		CPU_55S		CPU_2TO1	CPU DPRSTP L	7 10 16 23 59			
CPU_GTLREF		CPU_55S		CPU_GTLREF	CPU GTLREF	CPU_GTLREF		CPU_55S		CPU_GTLREF	CPU GTLREF	10			
CPU_COMP		CPU_55S		CPU_COMP	CPU COMP<3>	CPU_COMP		CPU_55S		CPU_COMP	CPU COMP<3>	10			
CPU_COMP		CPU_27P4S		CPU_COMP	CPU COMP<2>	CPU_COMP		CPU_27P4S		CPU_COMP	CPU COMP<2>	10			
CPU_COMP		CPU_55S		CPU_COMP	CPU COMP<1>	CPU_COMP		CPU_55S		CPU_COMP	CPU COMP<1>	10			
CPU_COMP		CPU_27P4S		CPU_COMP	CPU COMP<0>	CPU_COMP		CPU_27P4S		CPU_COMP	CPU COMP<0>	10			
XDP_TDI		CPU_55S		CPU_ITP	XDP TDI	XDP_TDI		CPU_55S		CPU_ITP	XDP TDI	10 13			
XDP_TDO		CPU_55S		CPU_ITP	XDP TDO	XDP_TDO		CPU_55S		CPU_ITP	XDP TDO	10 13			
XDP_TMS		CPU_55S		CPU_ITP	XDP TMS	XDP_TMS		CPU_55S		CPU_ITP	XDP TMS	10 13			
XDP_TCK		CPU_55S		CPU_ITP	XDP TCK	XDP_TCK		CPU_55S		CPU_ITP	XDP TCK	10 13			
XDP_TRST_L		CPU_55S		CPU_ITP	XDP TRST L	XDP_TRST_L		CPU_55S		CPU_ITP	XDP TRST L	10 13			
XDP_BEN_L		CPU_55S		CPU_ITP	XDP BPM L<4..0>	XDP_BEN_L		CPU_55S		CPU_ITP	XDP BPM L<4..0>	10 13			
XDP_BEN_L5		CPU_55S		CPU_ITP	XDP BPM L<5>	XDP_BEN_L5		CPU_55S		CPU_ITP	XDP BPM L<5>	10 13			
CLK_FSB_100D		CLK_FSB		XDP CLK_P	CLK_FSB_100D		CLK_FSB		XDP_CLK_P	CLK_FSB_100D		13 30 88			
(FSB_CPURST_L)		CPU_55S		CPU_ITP	XDP CLK_N	(FSB_CPURST_L)		CPU_55S		CPU_ITP	XDP CLK_N	13 30 88			
CPU_55S		CPU_2TO1		CPU VID<6..0>	CPU_55S		CPU_2TO1		CPU VID<6..0>	CPU_55S		CPU_2TO1		11 12	
CPU_55S		CPU_2TO1		IMVP6_VID<6..0>	CPU_55S		CPU_2TO1		IMVP6_VID<6..0>	CPU_55S		CPU_2TO1		7 12 49	
CPU_VCCSENSE		CPU_27P4S		CPU_VCCSENSE_P	CPU_VCCSENSE		CPU_27P4S		CPU_VCCSENSE_P	CPU_VCCSENSE		CPU_27P4S		11 59	
CPU_VCCSENSE		CPU_27P4S		CPU_VCCSENSE_N	CPU_VCCSENSE		CPU_27P4S		CPU_VCCSENSE_N	CPU_VCCSENSE		CPU_27P4S		11 59	
CPU_27P4S		CPU_VCCSENSE		IMVP6_VSEN_P	CPU_27P4S		CPU_VCCSENSE		IMVP6_VSEN_P	CPU_27P4S		CPU_VCCSENSE		59	
CPU_27P4S		CPU_VCCSENSE		IMVP6_VSEN_N	CPU_27P4S		CPU_VCCSENSE		IMVP6_VSEN_N	CPU_27P4S		CPU_VCCSENSE		59	

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8		7		6		5		4		3		2		1	
CPU/FSB Constraints															
SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007															
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PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CRT_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS	*	20 MIL	?
CRT	*	25 MIL	?
CRT_2CRT	*	20 MIL	?
CRT_SYNC	*	25 MIL	?
CRT_SYNC2SYNC	*	20 MIL	?
TVDAC	*	25 MIL	?
TVDAC_2TVDAC	*	20 MIL	?

DG Says 40 mil spacing minimum

DG Says 30 mil spacing minimum

DG Says 40 mil spacing minimum

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT
CRT_SYNC	CRT_SYNC	*	CRT_SYNC2SYNC
TVDAC	TVDAC	*	TVDAC_2TVDAC

LVDS signals are 100-ohm +/- 20% differential impedance.
CRT & TVDAC signal single-ended impedance varies by location:
- 37.5-ohm +/- 15% from GMCH to first termination resistor.
- 50-ohm +/- 15% from first to second termination resistor.
- 55-ohm +/- 15% from second termination resistor to connector.
CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

ELECTRICAL_CONSTRAINT_SET

NET_TYPE

PHYSICAL

SPACING

PEG_R2D

PCIE_100D

PCIE

PEG_R2D_P<15..0>

68

PEG_R2D_N<15..0>

68

PEG_R2D_C_P<15..0>

15

68

PEG_R2D_C_N<15..0>

15

68

PEG_D2R

PCIE_100D

PCIE

PEG_D2R_P<15..0>

15

68

PEG_D2R_N<15..0>

15

68

PEG_D2R_C_P<15..0>

68

PEG_D2R_C_N<15..0>

68

DMI_N2S

DMI_100D

DMI

DMI_N2S_P<3..0>

16

24

DMI_N2S_N<3..0>

16

24

DMI_S2N

DMI_100D

DMI

DMI_S2N_P<3..0>

16

24

DMI_S2N_N<3..0>

16

24

LVDS_A_CLK

LVDS_100D

LVDS

LVDS_A_CLK_P

15

79

LVDS_A_CLK_N

15

79

LVDS_A_DATA

LVDS_100D

LVDS

LVDS_A_DATA_P<2..0>

15

79

LVDS_A_DATA_N<2..0>

15

79

LVDS_A_DATA_P<3>

15

79

LVDS_A_DATA_N<3>

15

79

LVDS_B_CLK

LVDS_100D

LVDS

LVDS_B_CLK_P

15

79

LVDS_B_CLK_N

15

79

LVDS_B_DATA

LVDS_100D

LVDS

LVDS_B_DATA_P<2..0>

15

79

LVDS_B_DATA_N<2..0>

15

79

LVDS_B_DATA_P<3>

15

79

LVDS_B_DATA_N<3>

15

79

LVDS_IBG

LVDS

LVDS_IBG

15

22

CRT_TVO_IREF

CRT

CRT_TVO_IREF

CRT_RED

CRT_50S

CRT

CRT_RED

CRT_GREEN

CRT_50S

CRT

CRT_GREEN

CRT_BLUE

CRT_50S

CRT

CRT_BLUE

CRT_SYNC

CRT_55S

CRT_SYNC

CRT_HSYNC_R

CRT_SYNC

CRT_55S

CRT_SYNC

CRT_VSYNC_R

TV_A_DAC

CRT_50S

TVDAC

TV_A_DAC

TV_B_DAC

CRT_50S

TVDAC

TV_B_DAC

TV_C_DAC

CRT_50S

TVDAC

TV_C_DAC

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NB Constraints

SYNC_MASTER=T9_NOME

SYNC_DATE=01/25/2007

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SIZE D

DRAWING NUMBER 051-7430

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SHT 101

OF 109

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DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM_*-style wildcards!

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_CLK P<2..0>	16 31
	MEM_70D	MEM_CLK	MEM_CLK N<2..0>	16 31
MEM_A_CNTRL	MEM_45S	MEM_CTRL	MEM_CKE<1..0>	16 31 33
MEM_A_CNTRL	MEM_45S	MEM_CTRL	MEM_CS L<1..0>	16 31 33
MEM_A_CNTRL	MEM_45S	MEM_CTRL	MEM_ODT<1..0>	16 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A A<14..0>	16 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A BS<2..0>	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A RAS L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A CAS L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A WE L	17 31 33
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A DQ<7..0>	17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A DQ<15..8>	17 31
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A DQ<23..16>	17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A DQ<31..24>	17 31
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A DQ<39..32>	17 31
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A DQ<47..40>	17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A DQ<55..48>	17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A DQ<63..56>	17 31
MEM_A_DM0	MEM_55S	MEM_DATA	MEM_A DM<0>	17 31
MEM_A_DM1	MEM_55S	MEM_DATA	MEM_A DM<1>	17 31
MEM_A_DM2	MEM_55S	MEM_DATA	MEM_A DM<2>	17 31
MEM_A_DM3	MEM_55S	MEM_DATA	MEM_A DM<3>	17 31
MEM_A_DM4	MEM_55S	MEM_DATA	MEM_A DM<4>	17 31
MEM_A_DM5	MEM_55S	MEM_DATA	MEM_A DM<5>	17 31
MEM_A_DM6	MEM_55S	MEM_DATA	MEM_A DM<6>	17 31
MEM_A_DM7	MEM_55S	MEM_DATA	MEM_A DM<7>	17 31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A DQS P<0>	17 31
	MEM_85D	MEM_DQS	MEM_A DQS N<0>	17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A DQS P<1>	17 31
	MEM_85D	MEM_DQS	MEM_A DQS N<1>	17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A DQS P<2>	17 31
	MEM_85D	MEM_DQS	MEM_A DQS N<2>	17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A DQS P<3>	17 31
	MEM_85D	MEM_DQS	MEM_A DQS N<3>	17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A DQS P<4>	17 31
	MEM_85D	MEM_DQS	MEM_A DQS N<4>	17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A DQS P<5>	17 31
	MEM_85D	MEM_DQS	MEM_A DQS N<5>	17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A DQS P<6>	17 31
	MEM_85D	MEM_DQS	MEM_A DQS N<6>	17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A DQS P<7>	17 31
	MEM_85D	MEM_DQS	MEM_A DQS N<7>	17 31
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_CLK P<5..3>	16 32
	MEM_70D	MEM_CLK	MEM_CLK N<5..3>	16 32
MEM_B_CNTRL	MEM_45S	MEM_CTRL	MEM_CKE<4..3>	16 32 33
MEM_B_CNTRL	MEM_45S	MEM_CTRL	MEM_CS L<3..2>	16 32 33
MEM_B_CNTRL	MEM_45S	MEM_CTRL	MEM_ODT<3..2>	16 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B A<14..0>	16 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B BS<2..0>	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B RAS L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B CAS L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B WE L	17 32 33
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B DQ<7..0>	17 32
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B DQ<15..8>	17 32
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B DQ<23..16>	17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B DQ<31..24>	17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B DQ<39..32>	17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B DQ<47..40>	17 32
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B DQ<55..48>	17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B DQ<63..56>	17 32
MEM_B_DM0	MEM_55S	MEM_DATA	MEM_B DM<0>	17 32
MEM_B_DM1	MEM_55S	MEM_DATA	MEM_B DM<1>	17 32
MEM_B_DM2	MEM_55S	MEM_DATA	MEM_B DM<2>	17 32
MEM_B_DM3	MEM_55S	MEM_DATA	MEM_B DM<3>	17 32
MEM_B_DM4	MEM_55S	MEM_DATA	MEM_B DM<4>	17 32
MEM_B_DM5	MEM_55S	MEM_DATA	MEM_B DM<5>	17 32
MEM_B_DM6	MEM_55S	MEM_DATA	MEM_B DM<6>	17 32
MEM_B_DM7	MEM_55S	MEM_DATA	MEM_B DM<7>	17 32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B DQS P<0>	17 32
	MEM_85D	MEM_DQS	MEM_B DQS N<0>	17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B DQS P<1>	17 32
	MEM_85D	MEM_DQS	MEM_B DQS N<1>	17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B DQS P<2>	17 32
	MEM_85D	MEM_DQS	MEM_B DQS N<2>	17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B DQS P<3>	17 32
	MEM_85D	MEM_DQS	MEM_B DQS N<3>	17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B DQS P<4>	17 32
	MEM_85D	MEM_DQS	MEM_B DQS N<4>	17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B DQS P<5>	17 32
	MEM_85D	MEM_DQS	MEM_B DQS N<5>	17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B DQS P<6>	17 32
	MEM_85D	MEM_DQS	MEM_B DQS N<6>	17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B DQS P<7>	17 32
	MEM_85D	MEM_DQS	MEM_B DQS N<7>	17 32

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Memory Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Controller Link (AMT) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLINK_12MIL	*	=STANDARD	12 MILS	5 MILS	300 MILS	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLINK	*	=1.8:1_SPACING	?
CLINK_VREF	*	12 MILS	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Ethernet (Yukon) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MILS	?

SOURCE: Based on Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
PCI_AD	PCI_55S	PCI	PCI AD<18..0>	24 38
PCI_AD19	PCI_55S	PCI	PCI AD<19>	24 38
PCI_AD20	PCI_55S	PCI	PCI AD<20>	24 38
PCI_AD	PCI_55S	PCI	PCI AD<31..21>	24 38
PCI_AD	PCI_55S	PCI	PCI PAR	24 38
PCI_C_BE_L	PCI_55S	PCI	PCI C BE L<3..0>	24 38
PCI_CNTRL	PCI_55S	PCI	PCI IRDY L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI DEVSEL L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI PERR L	24 38
PCI_LOCK_L	PCI_55S	PCI	PCI LOCK L	24
PCI_CNTRL	PCI_55S	PCI	PCI SERR L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI STOP L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI TRDY L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI FRAME L	24 38
PCI_FW_REQ_L	PCI_55S	PCI	PCI FW REQ L	24 38
PCI_FW_GNT_L	PCI_55S	PCI	PCI FW GNT L	24 38
PCI_REQ1_L	PCI_55S	PCI	PCI REQ1 L	24
PCI_GNT1_L	PCI_55S	PCI	PCI GNT1 L	24
PCI_REQ2_L	PCI_55S	PCI	PCI REQ2 L	24
PCI_GNT2_L	PCI_55S	PCI	PCI GNT2 L	24
INT_PIRQA_L	PCI_55S	PCI	INT PIRQA L	24
INT_PIRQB_L	PCI_55S	PCI	INT PIRQB L	24
INT_PIRQC_L	PCI_55S	PCI	INT PIRQC L	24
INT_PIRQD_L	PCI_55S	PCI	INT PIROD L	24 38
INT_PIROE_L	PCI_55S	PCI	INT PIRQE L	24 38
INT_PIRQF_L	PCI_55S	PCI	INT PIRQF L	24
PCIE_A_R2D	PCIE_100D	PCIE	PCIE A R2D C P	24
PCIE_A_R2D	PCIE_100D	PCIE	PCIE A R2D C N	24
PCIE_A_D2R	PCIE_100D	PCIE	PCIE A D2R P	24
PCIE_A_D2R	PCIE_100D	PCIE	PCIE A D2R N	24
PCIE_B_R2D	PCIE_100D	PCIE	PCIE B R2D C P	24
PCIE_B_R2D	PCIE_100D	PCIE	PCIE B R2D C N	24
PCIE_B_D2R	PCIE_100D	PCIE	PCIE B D2R P	24
PCIE_B_D2R	PCIE_100D	PCIE	PCIE B D2R N	24
PCIE_EXCARD_R2D	PCIE_100D	PCIE	PCIE EXCARD R2D C P	34
PCIE_EXCARD_R2D	PCIE_100D	PCIE	PCIE EXCARD R2D C N	34
PCIE_EXCARD_D2R	PCIE_100D	PCIE	PCIE EXCARD D2R P	34
PCIE_EXCARD_D2R	PCIE_100D	PCIE	PCIE EXCARD D2R N	34
PCIE_FW_R2D	PCIE_100D	PCIE	PCIE FW R2D C P	24
PCIE_FW_R2D	PCIE_100D	PCIE	PCIE FW R2D C N	24
PCIE_FW_D2R	PCIE_100D	PCIE	PCIE FW D2R P	24
PCIE_FW_D2R	PCIE_100D	PCIE	PCIE FW D2R N	24
PCIE_MINI_R2D	PCIE_100D	PCIE	PCIE MINI R2D C P	24 34
PCIE_MINI_R2D	PCIE_100D	PCIE	PCIE MINI R2D C N	24 34
PCIE_MINI_D2R	PCIE_100D	PCIE	PCIE MINI D2R P	24 34
PCIE_MINI_D2R	PCIE_100D	PCIE	PCIE MINI D2R N	24 34
GLAN_COMP			GLAN COMP	23
CLINK_NB	CLINK_55S	CLINK	CLINK NB CLK	16 25
CLINK_NB	CLINK_55S	CLINK	CLINK NB DATA	16 25
CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK NB RESET L	16 25
CLINK_WLAN	CLINK_55S	CLINK	CLINK WLAN CLK	24
CLINK_WLAN	CLINK_55S	CLINK	CLINK WLAN DATA	24
CLINK_WLAN_RESET_L	CLINK_55S	CLINK	CLINK WLAN RESET L	24
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB CLINK VREF	16
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB CLINK VREF0	25
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB CLINK VREF1	25
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET R2D C P	24 35
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET R2D C N	24 35
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET R2D P	35
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET R2D N	35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET D2R P	24 35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET D2R N	24 35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET D2R C P	35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET D2R C N	35
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<0>	35 37
ENET_100D	ENET_100D	ENET_MDI	ENET MDI N<0>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<1>	35 37
ENET_100D	ENET_100D	ENET_MDI	ENET MDI N<1>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<2>	35 37
ENET_100D	ENET_100D	ENET_MDI	ENET MDI N<2>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<3>	35 37
ENET_100D	ENET_100D	ENET_MDI	ENET MDI N<3>	35 37

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SB Constraints (2 of 2)

SYNC_MASTER=T9_NAME SYNC_DATE=01/25/2007

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M75/M76 Board-Specific Spacing & Physical Constraints																																																																																																																																																																																
<table><tr><td colspan="6">BOARD LAYERS</td><td colspan="2">BOARD AREAS</td><td>BOARD UNITS (MIL OR MM)</td><td>ALLEGRO VERSION</td></tr><tr><td colspan="6">TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM</td><td colspan="2">NO_TYPE, BGA</td><td>MM</td><td>15.5.1</td></tr></table>																BOARD LAYERS						BOARD AREAS		BOARD UNITS (MIL OR MM)	ALLEGRO VERSION	TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM						NO_TYPE, BGA		MM	15.5.1																																																																																																																																													
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TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM						NO_TYPE, BGA		MM	15.5.1																																																																																																																																																																							
D	PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																																																																																																																																																																							
	DEFAULT		*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM																																																																																																																																																																							
	STANDARD		*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT																																																																																																																																																																							
	PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																																																																																																																																																																							
	55_OHM_SE		TOP, BOTTOM	Y	0.100 MM	0.100 MM																																																																																																																																																																										
	55_OHM_SE		ISL2, ISL11	Y	0.250 MM	0.076 MM																																																																																																																																																																										
	55_OHM_SE		*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD																																																																																																																																																																							
	PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																																																																																																																																																																							
	50_OHM_SE		TOP, BOTTOM	Y	0.125 MM	0.125 MM																																																																																																																																																																										
	50_OHM_SE		*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD																																																																																																																																																																							
	PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																																																																																																																																																																							
	45_OHM_SE		TOP, BOTTOM	Y	0.150 MM	0.150 MM																																																																																																																																																																										
45_OHM_SE		*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD																																																																																																																																																																								
C	PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																																																																																																																																																																							
	40_OHM_SE		TOP, BOTTOM	Y	0.185 MM	0.185 MM																																																																																																																																																																										
	40_OHM_SE		*	Y	0.131 MM	0.131 MM	=STANDARD	=STANDARD	=STANDARD																																																																																																																																																																							
	PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																																																																																																																																																																							
	27P4_OHM_SE		TOP, BOTTOM	Y	0.335 MM	0.335 MM																																																																																																																																																																										
	27P4_OHM_SE		*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD																																																																																																																																																																							
	PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																																																																																																																																																																							
	70_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD																																																																																																																																																																							
	70_OHM_DIFF		ISL3, ISL4	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM																																																																																																																																																																							
	70_OHM_DIFF		ISL9, ISL10	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM																																																																																																																																																																							
	70_OHM_DIFF		ISL2, ISL11	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM																																																																																																																																																																							
	70_OHM_DIFF		TOP, BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM																																																																																																																																																																							
B	PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																																																																																																																																																																							
	80_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD																																																																																																																																																																							
	80_OHM_DIFF		ISL3, ISL4	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM																																																																																																																																																																							
	80_OHM_DIFF		ISL9, ISL10	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM																																																																																																																																																																							
	80_OHM_DIFF		ISL2, ISL11	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM																																																																																																																																																																							
	80_OHM_DIFF		TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM																																																																																																																																																																							
	PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																																																																																																																																																																							
	85_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD																																																																																																																																																																							
	85_OHM_DIFF		ISL3, ISL4	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM																																																																																																																																																																							
	85_OHM_DIFF		ISL9, ISL10	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM																																																																																																																																																																							
	85_OHM_DIFF		ISL2, ISL11	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM																																																																																																																																																																							
	85_OHM_DIFF		TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM																																																																																																																																																																							
A	PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																																																																																																																																																																							
	90_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD																																																																																																																																																																							
	90_OHM_DIFF		ISL3, ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM																																																																																																																																																																							
	90_OHM_DIFF		ISL9, ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM																																																																																																																																																																							
	90_OHM_DIFF		ISL2, ISL11	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM																																																																																																																																																																							
	90_OHM_DIFF		TOP, BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM																																																																																																																																																																							
	PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																																																																																																																																																																							
	100_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD																																																																																																																																																																							
	100_OHM_DIFF		ISL3, ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM																																																																																																																																																																							
	100_OHM_DIFF		ISL9, ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM																																																																																																																																																																							
	100_OHM_DIFF		ISL2, ISL11	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM																																																																																																																																																																							
	100_OHM_DIFF		TOP, BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM																																																																																																																																																																							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																																																																																																																																																																								
110_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD																																																																																																																																																																								
110_OHM_DIFF		ISL3, ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM																																																																																																																																																																								
110_OHM_DIFF		ISL9, ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM																																																																																																																																																																								
110_OHM_DIFF		ISL2, ISL11	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM																																																																																																																																																																								
110_OHM_DIFF		TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM																																																																																																																																																																								
<table><tr><td colspan="2">SPACING_RULE_SET</td><td>LAYER</td><td>LINE-TO-LINE SPACING</td><td>WEIGHT</td></tr><tr><td colspan="2">DEFAULT</td><td>*</td><td>0.1 MM</td><td>?</td></tr><tr><td colspan="2">STANDARD</td><td>*</td><td>=DEFAULT</td><td>?</td></tr><tr><td colspan="2">BGA_P1MM</td><td>*</td><td>=DEFAULT</td><td>?</td></tr><tr><td colspan="2">BGA_P2MM</td><td>*</td><td>=DEFAULT</td><td>?</td></tr><tr><td colspan="2">BGA_P3MM</td><td>*</td><td>=DEFAULT</td><td>?</td></tr></table> <table><tr><td colspan="2">SPACING_RULE_SET</td><td>LAYER</td><td>LINE-TO-LINE SPACING</td><td>WEIGHT</td></tr><tr><td colspan="2">1.5:1_SPACING</td><td>*</td><td>0.15 MM</td><td>?</td></tr><tr><td colspan="2">1.8:1_SPACING</td><td>*</td><td>0.18 MM</td><td>?</td></tr><tr><td colspan="2">2:1_SPACING</td><td>*</td><td>0.2 MM</td><td>?</td></tr><tr><td colspan="2">2.5:1_SPACING</td><td>*</td><td>0.25 MM</td><td>?</td></tr><tr><td colspan="2">3:1_SPACING</td><td>*</td><td>0.3 MM</td><td>?</td></tr><tr><td colspan="2">4:1_SPACING</td><td>*</td><td>0.4 MM</td><td>?</td></tr></table> <table><tr><td>NET_SPACING_TYPE1</td><td>NET_SPACING_TYPE2</td><td>AREA_TYPE</td><td>SPACING_RULE_SET</td></tr><tr><td>*</td><td>*</td><td>BGA</td><td>BGA_P1MM</td></tr><tr><td>MEM_CLK</td><td>*</td><td>BGA</td><td>BGA_P2MM</td></tr><tr><td>CLK_FSB</td><td>*</td><td>BGA</td><td>BGA_P2MM</td></tr><tr><td>CLK_PCIE</td><td>*</td><td>BGA</td><td>BGA_P2MM</td></tr><tr><td>CLK_MED</td><td>*</td><td>BGA</td><td>BGA_P2MM</td></tr><tr><td>CLK_SLOW</td><td>*</td><td>BGA</td><td>BGA_P2MM</td></tr><tr><td>FSB_DSTB</td><td>FSB_DSTB</td><td>BGA</td><td>BGA_P3MM</td></tr></table> <table><tr><td>PHYSICAL_RULE_SET</td><td>LAYER</td><td>ALLOW ROUTE ON LAYER?</td><td>MINIMUM LINE WIDTH</td><td>MINIMUM NECK WIDTH</td><td>MAXIMUM NECK LENGTH</td><td>DIFFPAIR PRIMARY GAP</td><td>DIFFPAIR NECK GAP</td></tr><tr><td>1:1_DIFFPAIR</td><td>*</td><td>Y</td><td>=STANDARD</td><td>=STANDARD</td><td>=STANDARD</td><td>0.1 MM</td><td>0.1 MM</td></tr></table> <table><tr><td>PHYSICAL_RULE_SET</td><td>LAYER</td><td>ALLOW ROUTE ON LAYER?</td><td>MINIMUM LINE WIDTH</td><td>MINIMUM NECK WIDTH</td><td>MAXIMUM NECK LENGTH</td><td>DIFFPAIR PRIMARY GAP</td><td>DIFFPAIR NECK GAP</td></tr><tr><td>100_DIFF_BGA</td><td>*</td><td>=100_OHM_DIFF</td><td>=100_OHM_DIFF</td><td>=100_OHM_DIFF</td><td>=100_OHM_DIFF</td><td>=100_OHM_DIFF</td><td>=100_OHM_DIFF</td></tr><tr><td>100_DIFF_BGA</td><td>ISL3, ISL4</td><td>Y</td><td></td><td>0.075 MM</td><td></td><td></td><td>0.125 MM</td></tr><tr><td>100_DIFF_BGA</td><td>ISL9, ISL10</td><td>Y</td><td></td><td>0.075 MM</td><td></td><td></td><td>0.125 MM</td></tr><tr><td>100_DIFF_BGA</td><td>ISL2, ISL11</td><td>Y</td><td></td><td>0.085 MM</td><td></td><td></td><td>0.140 MM</td></tr><tr><td>100_DIFF_BGA</td><td>TOP, BOTTOM</td><td>Y</td><td></td><td>0.085 MM</td><td></td><td></td><td>0.140 MM</td></tr></table> <div><div><div></div><div>APPLE COMPUTER INC.</div></div><div><div>SIZE</div><div>DRAWING NUMBER</div><div>REV.</div></div><div><div>SCALE</div><div>SHT</div><div>OF</div><div></div></div><div><div>D</div><div>051-7430</div><div>B</div></div><div><div>NONE</div><div>109</div><div>109</div></div></div> <div><div>M75/M76 Rule Definitions</div><div>SYNC_MASTER=M76_MLB SYNC_DATE=02/02/2007</div><div>NOTICE OF PROPRIETARY PROPERTY</div><div>THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</div><div>I TO MAINTAIN THE DOCUMENT IN CONFIDENCE</div><div>II NOT TO REPRODUCE OR COPY IT</div><div>III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</div></div> <p>NOTE: 100_DIFF_BGA is for select 100-ohm differential pairs with routing difficulties through BGAs. Default width/spacing is 100-ohm differential, but pairs can neck to 95-ohms without DRC.</p>																SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT	DEFAULT		*	0.1 MM	?	STANDARD		*	=DEFAULT	?	BGA_P1MM		*	=DEFAULT	?	BGA_P2MM		*	=DEFAULT	?	BGA_P3MM		*	=DEFAULT	?	SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT	1.5:1_SPACING		*	0.15 MM	?	1.8:1_SPACING		*	0.18 MM	?	2:1_SPACING		*	0.2 MM	?	2.5:1_SPACING		*	0.25 MM	?	3:1_SPACING		*	0.3 MM	?	4:1_SPACING		*	0.4 MM	?	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	*	*	BGA	BGA_P1MM	MEM_CLK	*	BGA	BGA_P2MM	CLK_FSB	*	BGA	BGA_P2MM	CLK_PCIE	*	BGA	BGA_P2MM	CLK_MED	*	BGA	BGA_P2MM	CLK_SLOW	*	BGA	BGA_P2MM	FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	100_DIFF_BGA	ISL3, ISL4	Y		0.075 MM			0.125 MM	100_DIFF_BGA	ISL9, ISL10	Y		0.075 MM			0.125 MM	100_DIFF_BGA	ISL2, ISL11	Y		0.085 MM			0.140 MM	100_DIFF_BGA	TOP, BOTTOM	Y		0.085 MM			0.140 MM
SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT																																																																																																																																																																												
DEFAULT		*	0.1 MM	?																																																																																																																																																																												
STANDARD		*	=DEFAULT	?																																																																																																																																																																												
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SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT																																																																																																																																																																												
1.5:1_SPACING		*	0.15 MM	?																																																																																																																																																																												
1.8:1_SPACING		*	0.18 MM	?																																																																																																																																																																												
2:1_SPACING		*	0.2 MM	?																																																																																																																																																																												
2.5:1_SPACING		*	0.25 MM	?																																																																																																																																																																												
3:1_SPACING		*	0.3 MM	?																																																																																																																																																																												
4:1_SPACING		*	0.4 MM	?																																																																																																																																																																												
NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET																																																																																																																																																																													
*	*	BGA	BGA_P1MM																																																																																																																																																																													
MEM_CLK	*	BGA	BGA_P2MM																																																																																																																																																																													
CLK_FSB	*	BGA	BGA_P2MM																																																																																																																																																																													
CLK_PCIE	*	BGA	BGA_P2MM																																																																																																																																																																													
CLK_MED	*	BGA	BGA_P2MM																																																																																																																																																																													
CLK_SLOW	*	BGA	BGA_P2MM																																																																																																																																																																													
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM																																																																																																																																																																													
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																																																																																																																																																																									
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM																																																																																																																																																																									
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																																																																																																																																																																									
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF																																																																																																																																																																									
100_DIFF_BGA	ISL3, ISL4	Y		0.075 MM			0.125 MM																																																																																																																																																																									
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100_DIFF_BGA	ISL2, ISL11	Y		0.085 MM			0.140 MM																																																																																																																																																																									
100_DIFF_BGA	TOP, BOTTOM	Y		0.085 MM			0.140 MM																																																																																																																																																																									
8		7		6		5		4		3		2		1																																																																																																																																																																		

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM


PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3, ISL4	Y		0.075 MM			0.125 MM
100_DIFF_BGA	ISL9, ISL10	Y		0.075 MM			0.125 MM
100_DIFF_BGA	ISL2, ISL11	Y		0.085 MM			0.140 MM
100_DIFF_BGA	TOP, BOTTOM	Y		0.085 MM			0.140 MM

NOTE: 100_DIFF_BGA is for select 100-ohm differential pairs with routing difficulties through BGAs. Default width/spacing is 100-ohm differential, but pairs can neck to 95-ohms without DRC.

M75/M76 Rule Definitions
SYNC_MASTER=M76_MLB SYNC_DATE=02/02/2007

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