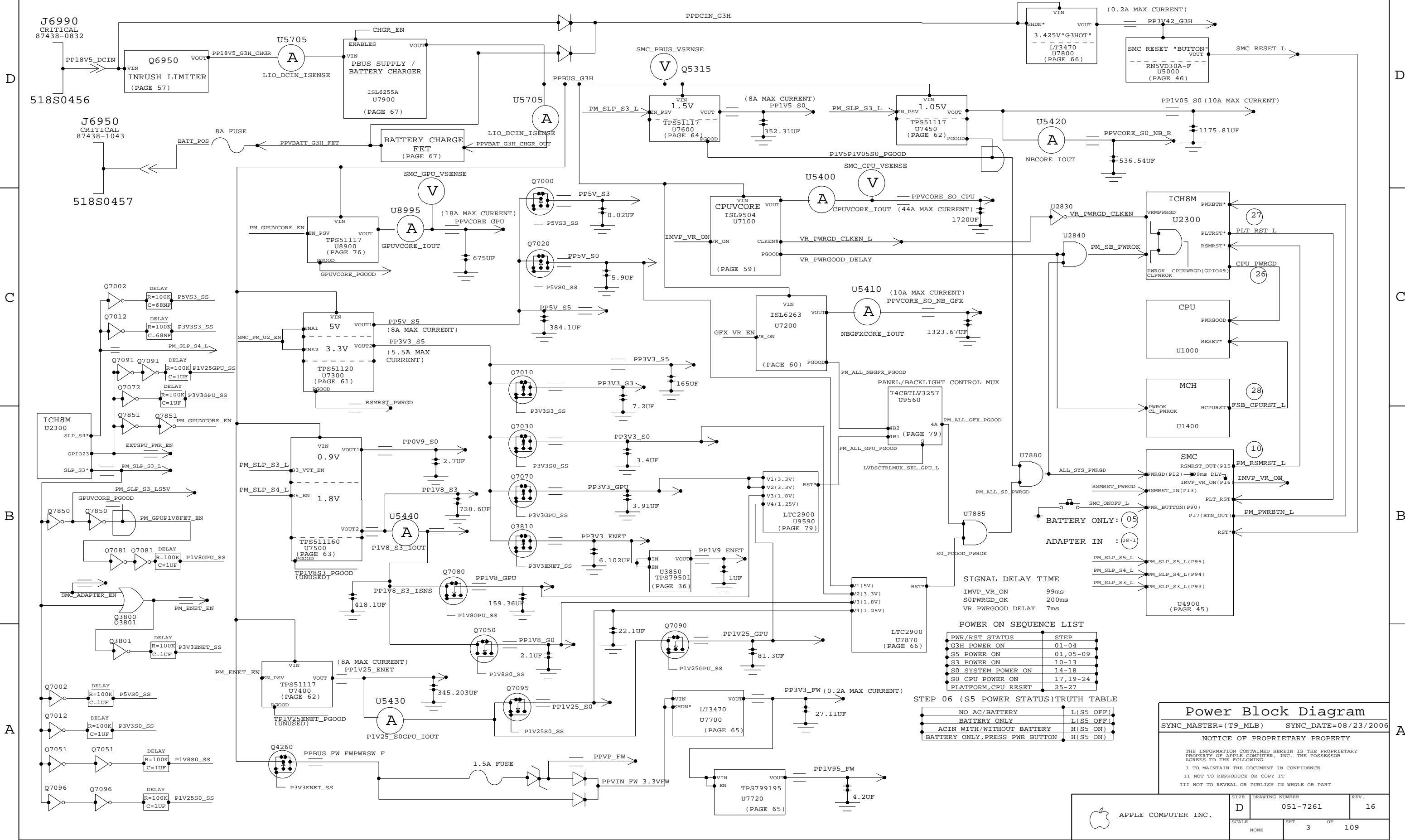
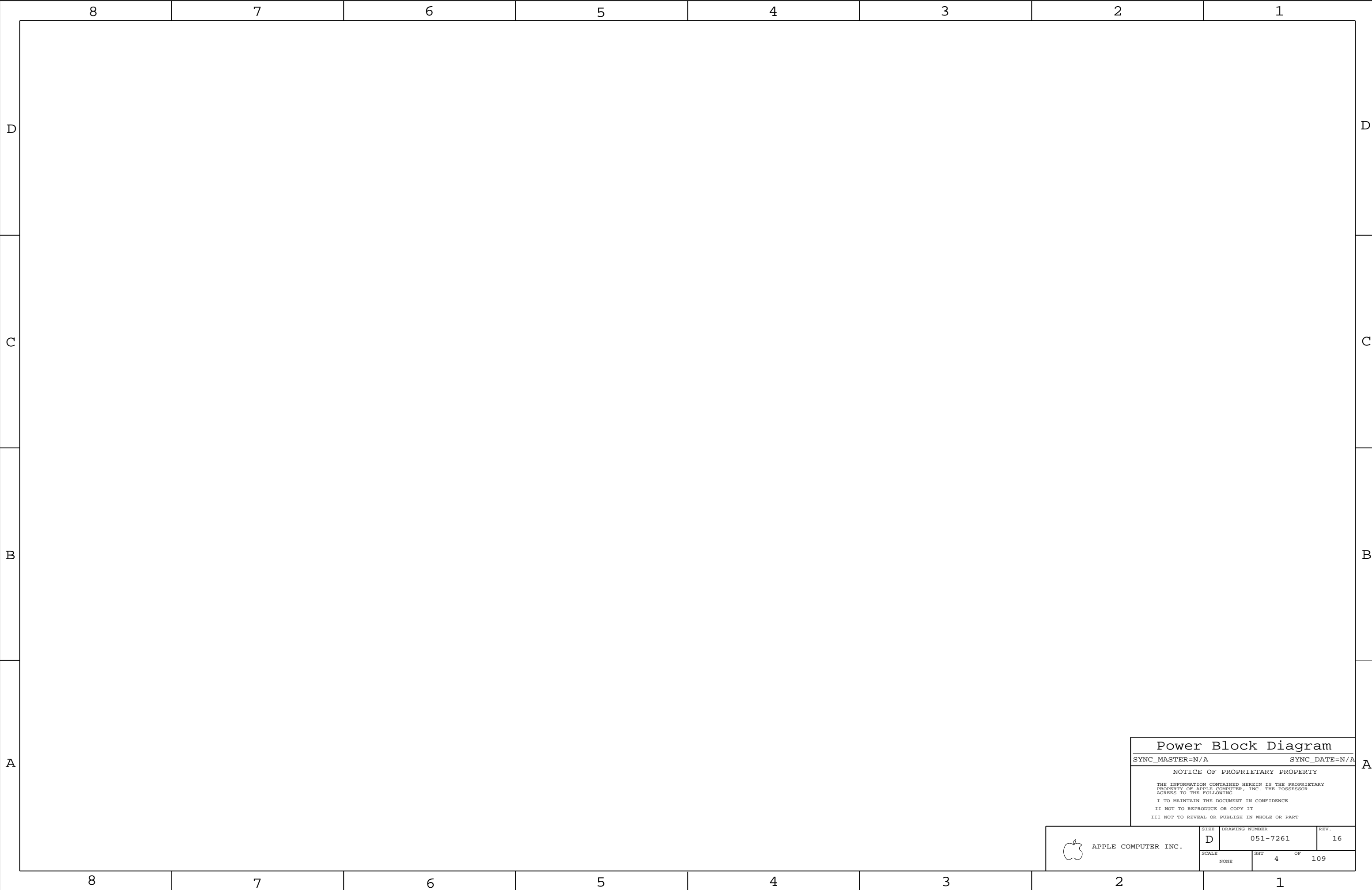



M76 POWER SYSTEM ARCHITECTURE





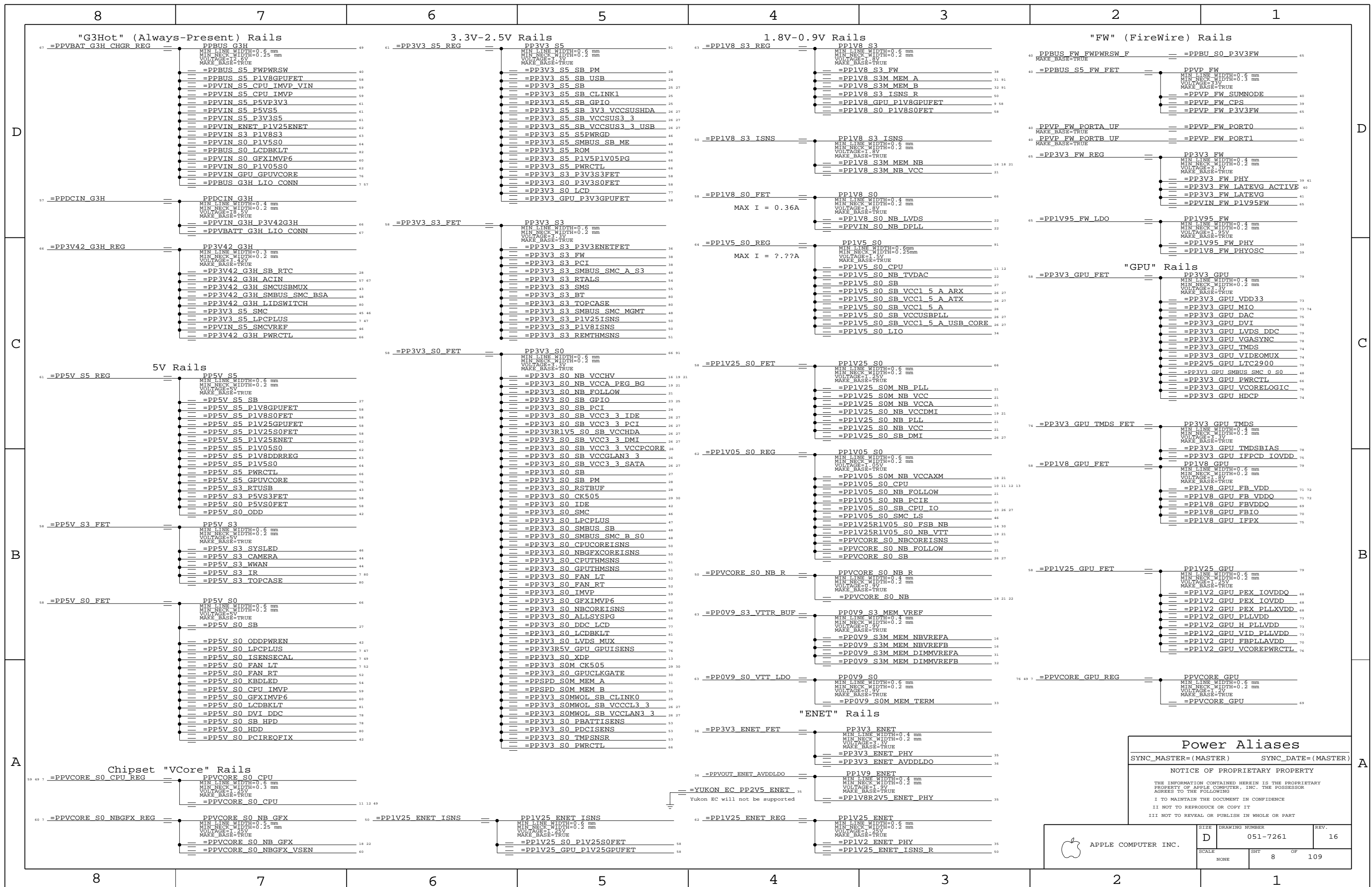
 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7261	REV. 16
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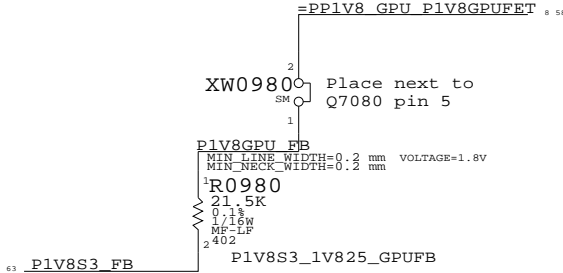
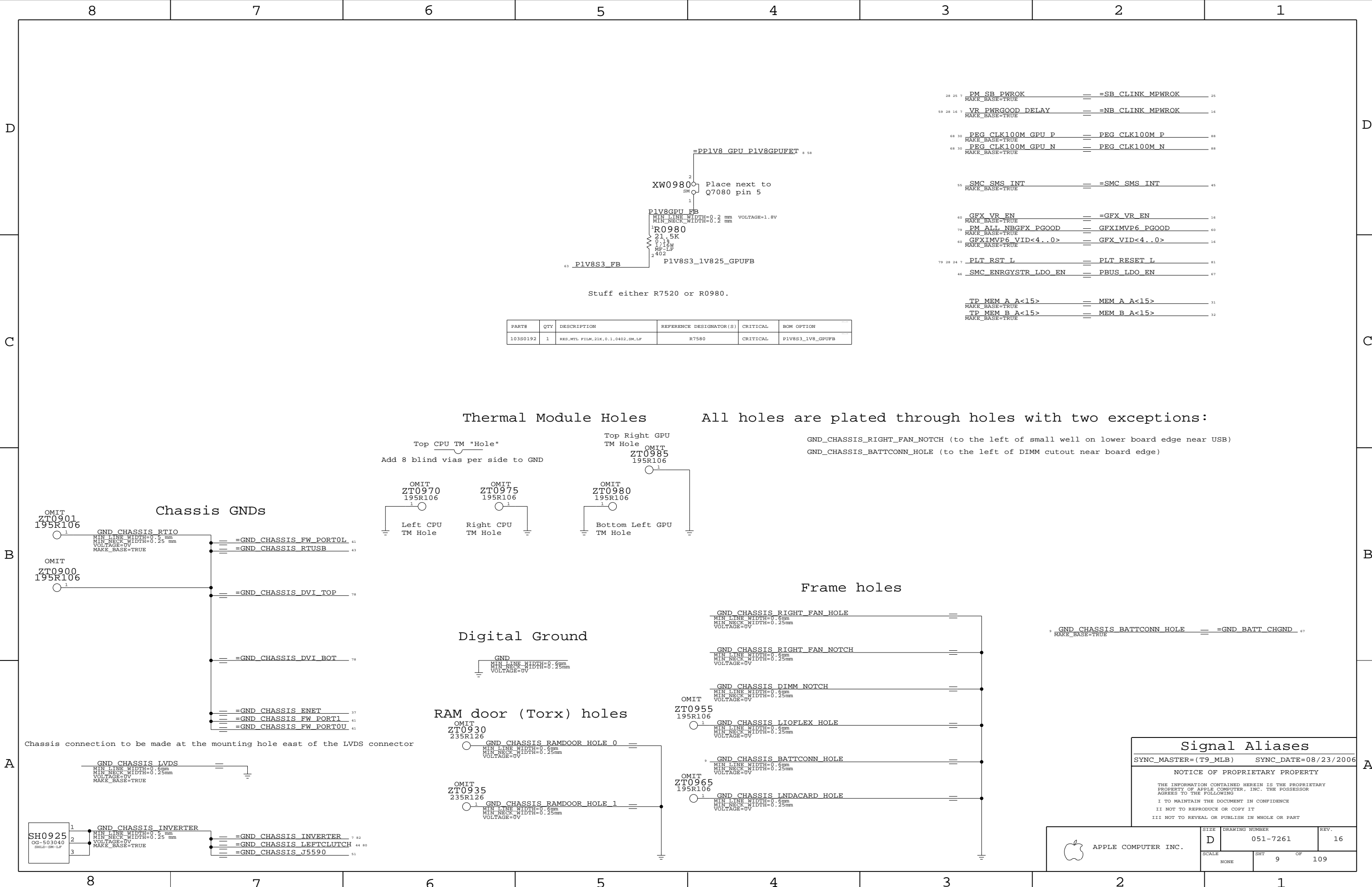
Power Block Diagram	
SYNC_MASTER=N/A	SYNC_DATE=N/A
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D	<div>DVT</div> <div>13.1.0:</div> <div>3/05/07 -- Integrated m75/mlb pages 22,25,28,30-32,50,53-55,72,74,76,78,80-82,84-90,94,95 through:</div> <div>Change 46833 by cerickso@m75_mlb_051-7225_12.5.0_tmp.Ecad on 2007/03/02 09:49:13</div> <div>Changes since previous major release (12.3.0):</div> <div>- LVDS Connector: Changed pin 5 of connector from NC to PP3V3_SW_LCD (in case we add extra cable for power - rdar://5024882)</div> <div>- NB GFX Decoupling: Added R2260 (0.3 ohm, 0603) to bring ESR of regulator output cap in spec (rdar://5000272)</div> <div>Changes since previous major release (12.2.0):</div> <div>- Left Clutch IC: Updated both I-PEX connectors to new APN (part update for shell plating)</div> <div>- NB GFX Core: Changed Vcore controller to ISL6263B (part consolidation effort between Apple/Intersil - rdar://5009109)</div> <div>- Power Supplies: Replaced APN 152S0511 with 152S0368 (duplicate APNs for same part - rdar://5009109)</div> <div>- Thermal Sensors: Updated topology of EMC1033 sensors (removed shorts, changed connector caps to 18pF)</div> <div>- NB GFX Decoupling/Power Aliases: Connected VCCD_CRT of NB to GND per CRT disable guidelines</div> <div>Changes since previous bom release (12.0.0):</div> <div>- GPU FB: Changed cal resistors per Nvidia PUN (R8290 to 45.3 ohm and R8291 to 24.9 ohm)</div> <div>- GPU FB: Changed unterminated-mode reference voltage to 40% (R8297 -> 1.02k, R8432/82, R8532/82 -> 2.21K)</div> <div>- Power Sequencing: Removed U7885/C7885 to take GFX_PGOOD out of PWR_OK chain (rdar://4974927)</div> <div>- GPU Vcore: NO STUFFed all PWRCTL related components (feature not to be supported)</div> <div>- GPU Vcore: Updated voltage setpoints to 1.000/1.070/1.125V</div> <div>- SB GPIOs: Sync'd page25.csa to T9_MLB to get pullup updates</div> <div>- Thermal Sensors: Updated topology of EMC1033 filter caps (added C5515 next to IC, moved other caps to connectors)</div> <div>3/5/07 -- Added GPU Vcore VFB resistor BOM table and GCORE_M76 BOM Option to M76_COMMON BOM group.</div> <div>3/5/07 -- Removed RX3920-RX3927.</div> <div>3/5/07 -- FireWire: Changed to Rev C of TI FireWire MCM (APN: 338S0435)</div> <div>3/5/07 -- ODD Conn: Changed ODD power FET to FDC606P (from FDC638P) for reduced Rds(on)</div> <div>3/5/07 -- Changed 1.8V supply feedback resistors R7520 to 21.5K 0.1% and R7521 15.0K 0.1%.%</div> <div>13.2.0</div> <div>3/07/07 -- Integrated m75/mlb pages 25,42,70 through:</div> <div>Change 47192 by cerickso@m75_mlb_051-7225_12.7.0_tmp.Ecad on 2007/03/06 18:36:54</div> <div>Changes since previous major release (12.6.0):</div> <div>- FireWire Ports: Changed D4260 to PDS540 for higher current capacity</div> <div>- SB GPIOs: Changed R2514 from pulldown to pulldown to correct auto power-on issue (Linda card detect GPIO)</div> <div>3/07/07 -- Q7080 PP1V8_GPU FET changed for lower Rds on from FDM6296 to RJK0301DPB</div> <div>13.3.0</div> <div>3/08/07 -- Removed =PP1V5_S0_NB_VCCD_CRT alias to PP1V5_S0 since VCCD_CRT is GNDed per CRT disable guidelines.</div> <div>3/08/07 -- Battery charge current limit circuit changes.</div> <div>3/08/07 -- Changed R9811 from 15.0K to 14.0K. This is so that M57 inverter and split inverter can use same backlight table.</div> <div>3/08/07 -- Changed R9950 from 220K to NOSTUFF to improve current and voltage asymmetry ratio.</div> <div>3/08/07 -- Changed BOM option on R9960 511K from NOSTUFF to INV_SPLIT to improve current and voltage asymmetry ratio.</div> <div>3/08/07 -- Integrated CSA pg. 55 through:</div> <div>Change 47450 by cerickso@m75_mlb_051-7225_12.8.0_tmp.Ecad on 2007/03/08 10:49:26</div> <div>Changes since previous major release (12.7.0):</div> <div>- Thermal Sensors: Added R5515/R5516 in case low pass filter is needed for EMC1033</div> <div>3/08/07 -- Integrated CSA pg. 79 through:</div> <div>Change 47440 by xyang@m75_lio_051-7226_7.9.0_tmp.Ecad on 2007/03/08 10:25:46</div> <div>Changed Charger PWM limit resistor according to MARC K.'S M70 values</div> <div>13.4.0</div> <div>3/12/07 -- Added BOM option P1V8S3_1V825 to M76_COMMON2 BOM group.</div> <div>3/12/07 -- Modified R7520 and R7521 to use symbols for 0.1% resistors.</div> <div>Removed OMIT BOM option from R7521.</div> <div>Changed BOM options for R7520 to choose between 1.8V or 1.825V 0.1% resistors.</div> <div>14.0.0</div> <div>3/14/07 -- Removed BOM option for HDCP as feature is removed.</div> <div>3/14/07 -- Moved =PP1V8_GPU_P1V8GPUFET from PP1V8_S3_ISNS to PP1V8_S3. This is to remove the current sense resistor from the GPU 1.8V path.</div> <div>Cleaned up unused aliases.</div> <div>3/14/07 -- Constraints: Constrained WWAN_SIM signals to 50 ohms</div> <div>3/14/07 -- Integrated m75/mlb CSA pages 55 & 78 through:</div> <div>Change 48122 by cerickso@cerickso_m75.Ecad on 2007/03/14 15:27:36</div> <div>- Thermal Sensors/Aliases: Changed mounting pads of Th2H sensor connector to left clutch chassis gnd</div> <div>- Power Control: Corrected alias connections for 5V/3V3 S5 enable signals</div> <div>14.1.0</div> <div>3/14/07 -- Moved =PP1V8_S0_P1V8S0FET from PP1V8_S3_ISNS to PP1V8_S3.</div> <div>14.2.0</div> <div>3/15/07 -- Changes to low voltage inverter for M76 piezo.</div> <div>14.5.0</div> <div>3/19/07 --</div> <div>Integrated m75/mlb CSA pgs. 28,30-32,50,53-55,80-82,84-88,90,94,95 through:</div> <div>Change 48405 by cerickso@m75_mlb_051-7225_13.3.0_tmp.Ecad on 2007/03/16 12:18:46</div> <div>Changes since previous major release (13.2.0):</div> <div>- Thermal Sensors: Moved remote sensor U5500 to SMC SMBus A and S3 power rail to clear I2C addr clash</div> <div>3/19/07 --Integrated t9/mlb_noME CSA pgs. 15 & 38 through:</div> <div>Change 48372 by wferry@wferry_projects.Ecad on 2007/03/16 09:11:01</div> <div>Quick submit of T9 noME branch. Major release will follow once changes are properly documented in Radar and revision history.</div> <div>Page 15: Sync from main-line (renamed LVDS_VREFx nets).</div> <div>Page 38: Changed Yukon crystal load caps to 18pF per radar://4946795 (really radar://4945362).</div> <div>3/19/07 -- Added OMIT BOM option to L4731 and L4741.</div> <div>3/19/07 -- Added BOM table with 0 Ohm 0603 resistors at L4731,L4741.</div> <div>3/19/07 -- SMBus: moved Remote Temps from SMC B to SMC A in order to use EMC1043-5.</div> <div>3/19/07 --</div> <div><rdar://problem/5070179> BOM update: boost circuit open causes MLB & SIMM damage (see 5064997)</div> <div>Deleted R7364 and made C7364 0603 size, still 0.1uF (132S0100).</div> <div>Deleted R7420 and R7470 and made C7420 and C7470 0603 size, still 0.1uF (132S0100).</div> <div>Deleted R7525 and made C7525 0805 size, still 0.1uF (132S0201).</div> <div>Deleted R7615 and made C7615 0603 size, still 0.1uF (132S0100).</div> <div>Deleted R8915 and made C8915 0603 size, still 0.1uF (132S0100).</div> <div>3/19/07 -- Changes to low voltage inverter for M76 piezo.</div> <div>L9950 changed from 152S0527 (15uH, 2.8A, 115mOhm) to 152S0585 (22uH, 2.8A, 129mOhm).</div> <div>14.6.0</div> <div>3/19/07 -- Integrated m75/mlb CSA pgs. 55 & 78 through:</div> <div>Change 48590 by cerickso@m75_mlb_051-7225_13.4.0_tmp.Ecad on 2007/03/19 14:26:14</div> <div>Changes since previous major release (13.3.0):</div> <div>- Thermal Sensors: Updated U5500 power alias to indicate device should be on S3 rail</div> <div>- Power Control: Added U7858 to level shift PM_G2_EN to 3.42V to 5V</div> <div>3/19/07 -- Updated SMC A SMBus information for Left I/O Board and Top-Case.</div> <div>3/19/07 -- Deleted R7324 and made C7324 0603 size, still 0.1uF (132S0100).</div> <div>14.7.0</div> <div>3/19/07 -- Added three 0603 0 ohm resistors R4740-R4742 for EMC return current path.</div> <div>3/19/07 -- Battery charge current limit circuit changes for max charge current of 4.5A.</div> <div>3/19/07 -- Integrated m75/mlb CSA pgs. 22 & 78 through:</div> <div>Change 48660 by cerickso@m75_mlb_051-7225_13.5.0_tmp.Ecad on 2007/03/19 20:17:1 Changes since previous major release (13.4.0):</div> <div>- Power Control: Tied all 4 5V/3.3V enables (EN1, EN2, EN3 and EN5) together as part of PM_G2_EN</div> <div>14.8.0</div> <div>3/21/07 -- Integrated m75/mlb CSA pgs. 84,85 & 89 through:</div> <div>Change 48885 by cerickso@m75_mlb_051-7225_14.0.0_tmp.Ecad on 2007/03/20 21:27:14</div> <div>This fab release is for DVT!</div> <div>Changes since previous major release (13.5.0):</div> <div>- GPU Vcore: Updated setpoints for GPU Vcore based upon Nvidia Vmin (i.e. 1.05V, 1.05V, 1.05V, 1.125V)</div> <div>- FB: Changed FB VREF caps to 2x0.0047uF as required by Nvidia PUN 02736-001-v07 (which requests 1x0.01uF)</div> <div>3/21/07 -- <rdar://problem/4838347> EMC - M76 MLB changes</div> <div>Change BOM option on L4764 to OMIT and added BOM table entry for 0 ohm resistor at L4764.</div> <div>3/21/07 -- <rdar://problem/5073301> M76: Change GPU Vmin</div> <div>Changed resistors for M76 Vcore setpoints (i.e. 1.05V, 1.05V, 1.125V, 1.25V)</div> <div>Removed NOSTUFF BOM option from R8924.</div> <div>Changed R8924 to 28K.</div> <div>Changed R8925 to 16.9K.</div> <div>Changed table text notes.</div> <div>3/22/07 -- Items relating to <rdar://problem/5061583> Task: Current Surge When Insert Battery Without AC Plugged-In</div> <div>3/22/07 -- Added D7903 for voltage ripple on ISL6257 BOOT and PHASE pins.</div> <div>3/22/07 -- Added Q7970 for potential battery inrush current.</div> <div>15.0.0</div> <div>3/26/07 -- Removed C7930 and R7903 for space reasons.</div> <div>15.2.0</div> <div>3/28/07 -- Change BOM option for 1.8V regulator feedback to 1.8V GPU FET input.</div> <div>3/28/07 -- Added XW7580 and R7580 for option to tie 1.8V S3 regulator feedback point to input of 1.8V GPU FET.</div> <div>3/28/07 -- Integrated m75/mlb CSA pg. 87 through</div> <div>Change 49919 by cerickso@cerickso_m75.Ecad on 2007/03/28 14:28:29</div> <div>Changes since previous fab release (14.0.0):</div> <div>- GPU Straps: Added PCI_DEVID<3..0> pullup straps</div> <div>15.3.0</div> <div>3/29/07-- Moved XW7580 to XW0980, and R7580 to R0980.</div> <div>15.4.0</div> <div>3/31/97 -- Changed C9950 from 22uF to 10uF for acoustic noise per Flo Kim.</div> <div>3/31/97 --Added C9951 B2 case size as placeholder for new cap for acoustic noise per Flo Kim.</div>														
	C														
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	<div>16</div> <div>SYNC_MASTER=N/A</div> <div>SYNC_DATE=N/A</div> <div>NOTICE OF PROPRIETARY PROPERTY</div> <div>THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</div> <div>I TO MAINTAIN THE DOCUMENT IN CONFIDENCE</div> <div>II NOT TO REPRODUCE OR COPY IT</div> <div>III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</div>														
											<div>APPLE COMPUTER INC.</div> <div>SIZE D</div> <div>DRAWING NUMBER 051-7261</div> <div>REV. 16</div> <div>SCALE NONE</div> <div>SHT 6 OF 109</div>				
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	Functional Test Points								
D	Fan Connectors		Battery Digital Connector		ICT Test Points		NB NO_TESTS		
	FUNC_TEST		FUNC_TEST		CPU FSB NO_TESTS		NO_TEST		
	R439 TRUE =PP5V_S0_FAN_LT 8 52		R500 TRUE SMC_BS_ALERT_L 45 46 57		R550 TRUE FSB_A_L<31..3> 10 14 83		R550 TRUE NC_NB_NC<1..16> == TP_NB_NC<1..16> 16		
	R439 TRUE FAN_LT_PWM 52		R500 TRUE =SMBUS_BATT_SCL 48 57		R550 TRUE FSB_ADS_L 10 14 83				
	R439 TRUE FAN_LT_TACH 52		R500 TRUE =SMBUS_BATT_SDA 48 57		R550 TRUE FSB_ADSTB_L<1..0> 10 14 83				
	R439 TRUE FAN_RT_PWM 52		R500 TRUE =BATT_POS 57 67		R550 TRUE FSB_BNR_L 10 14 83				
	R439 TRUE FAN_RT_TACH 52		R500 TRUE =BATT_NEG 57 67		R550 TRUE FSB_BREQ0_L 10 14 83				
			TRUE GND (HOST_DETECT_L)		R550 TRUE FSB_D_L<63..0> 10 14 83				
			Left I/O Power Connector		R550 TRUE FSB_DBSY_L 10 14 83				
			FUNC_TEST		R550 TRUE FSB_DINV_L<3..0> 10 14 83				
C	LPC+ Debug Connector		Request for 2 test points Request for 3 test points		R550 TRUE FSB_DRDY_L 10 14 83		GPU NO_TESTS		
	FUNC_TEST		R500 TRUE PPI8V5_DCIN 57		R550 TRUE FSB_DSTB_L_N<3..0> 10 14 83		NO_TEST		
	R439 TRUE =PP5V_S0_LPCPLUS 8 47		R439 TRUE =PPBUS_G3H_LIO_CONN 8 57		R550 TRUE FSB_DSTB_L_P<3..0> 10 14 83		R560 TRUE LVDS_L_CLK_P 75 79 90		
	R439 TRUE =PP5V_S0_LPCPLUS 8 47		TRUE GND		R550 TRUE FSB_HIT_L 10 14 83		R560 TRUE LVDS_L_DATA_P<0> 75 79 90		
	R439 TRUE LPC_AD<0> 23 45 47				R550 TRUE FSB_HITM_L 10 14 83		R560 TRUE TP_GPU_MIOB_CLKIN 74		
	R439 TRUE LPC_AD<1> 23 45 47				R550 TRUE FSB_LOCK_L 10 14 83		R560 TRUE TP_GPU_MIOB_CLKOUT_P 74		
	R439 TRUE LPC_FRAME_L 23 45 47				R550 TRUE FSB_REQ_L<4..0> 10 14 83		R560 TRUE TP_GPU_MIOB_CTL3 74		
	R439 TRUE PM_CLKRUN_L 25 45 47								
	R439 TRUE BOOT_LPC_SPI_L 24 47								
	R439 TRUE SMC_TMS 45 46 47								
B	R439 TRUE DEBUG_RESET_L 28 47		RTC Battery Connector						
	R439 TRUE SMC_TEST_L 45 47		FUNC_TEST						
	R439 TRUE SMC_TDO 45 46 47		R510 TRUE PPVBATT_G3_RTC 28						
	R439 TRUE SMC_MD1 45 47		TRUE GND						
	R439 TRUE SMC_TX_L 43 45 46 47								
	R439 TRUE FWH_INIT_L 47								
	R439 TRUE PCI_CLK33M_LPCPLUS 30 47 88								
	R439 TRUE LPC_AD<2> 23 45 47								
	R439 TRUE LPC_AD<3> 23 45 47								
	R439 TRUE INT_SERIRQ 25 45 47								
A	R439 TRUE PM_SUS_STAT_L 25 45 47		Current Sense Calibration		Inverter Connector				
	R439 TRUE SMC_TDI 45 46 47		FUNC_TEST		FUNC_TEST				
	R439 TRUE SMC_TCK 45 46 47		R439 TRUE ISENSE_CAL_EN 45 49		R550 TRUE PPBUS_S0_LCDBKLT_FUSED 82				
	R439 TRUE SMC_RESET_L 45 46 47		R439 TRUE =PP5V_S0_ISENSECAL 8 49		R550 TRUE =GND_CHASSIS_INVERTER 9 82				
	R439 TRUE SMC_NMI 45 47		R439 TRUE =PPVCORE_S0_NBQFX_REG 8 60		R550 TRUE PP5V_SW_LCDBKLT 81 82				
	R439 TRUE SMC_RX_L 43 45 46 47		R439 TRUE =PPVCORE_S0_CPU_REG 8 49 59		R550 TRUE LCDBKLT_PWM 81 82				
	R439 TRUE LINDACARD_GPIO 25 47		R439 TRUE =PPVCORE_GPU_REG 8 49 76		TRUE GND				
			TRUE GND						
			6 TPs, 2 with each of above TP pairs						
		Left Clutch Barrel Connector		IR & Sleep LED Connector					
		FUNC_TEST		FUNC_TEST					
		R500 TRUE PP5V_S3_CAMERA_F 44		R500 TRUE =PP5V_S3_IR 8 80					
		R500 TRUE USB_CAMERA_F_N 44 91		R500 TRUE USB_IR_N 24 80 86					
		R500 TRUE USB_CAMERA_F_P 44 91		R500 TRUE USB_IR_P 24 80 86					
		R500 TRUE PP5V_S3_WWAN_F 44		R500 TRUE SYS_LED_ANODE 46 80					
		R500 TRUE USB_WWAN_F_N 44 91		TRUE GND					
		R500 TRUE USB_WWAN_F_P 44 91							
		Other Func Test Points							
		FUNC_TEST							
		R439 TRUE PM_SYSRST_L 25 28 45							
		R439 TRUE SMC_ONOFF_L 45 46 80							



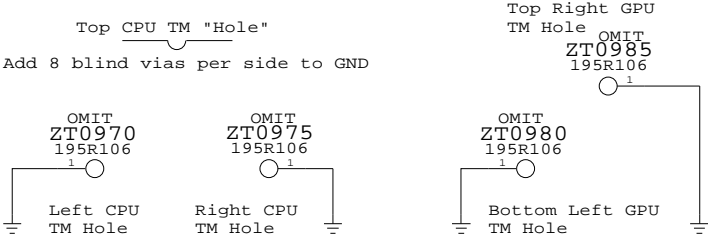


Stuff either R7520 or R0980.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
103S0192	1	RES,MTL FILM,21K,0.1,0402,SM,LF	R7580	CRITICAL	P1V8S3_1V8_GPUFB

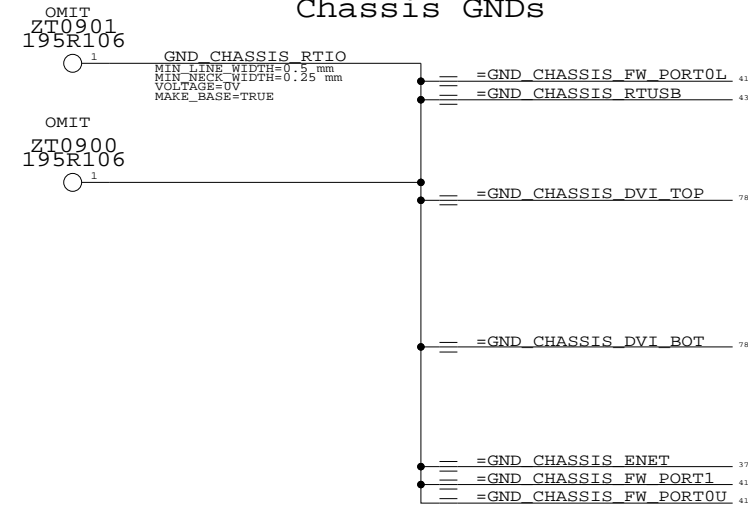
Thermal Module Holes

All holes are plated through holes with two exceptions:

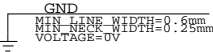


GND_CHASSIS_RIGHT_FAN_NOTCH (to the left of small well on lower board edge near USB)
GND_CHASSIS_BATTCONN_HOLE (to the left of DIMM cutout near board edge)

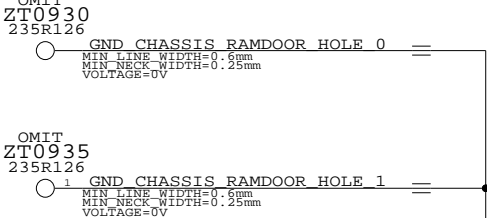
Chassis GNDS



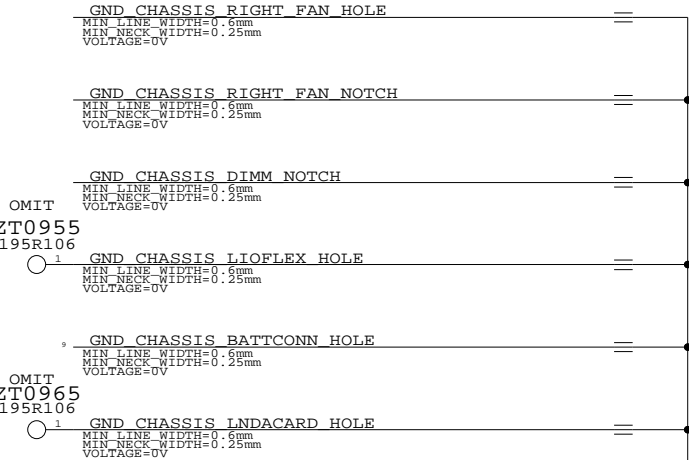
Digital Ground



RAM door (Torx) holes

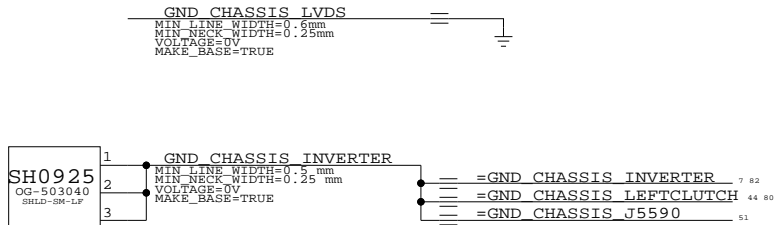


Frame holes



GND_CHASSIS_BATTCONN_HOLE (to the left of DIMM cutout near board edge)

Chassis connection to be made at the mounting hole east of the LVDS connector



Signal Aliases

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/23/2006

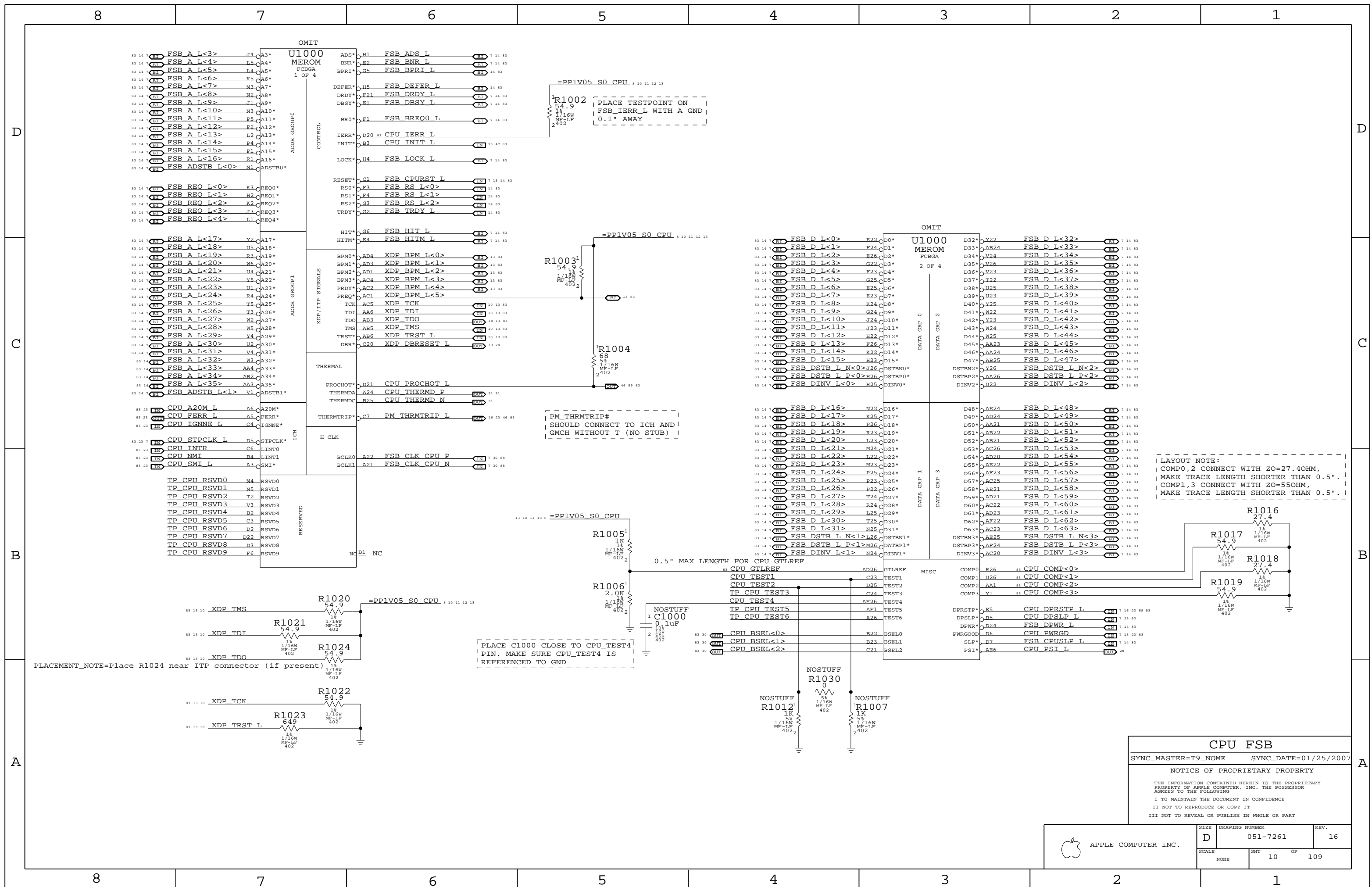
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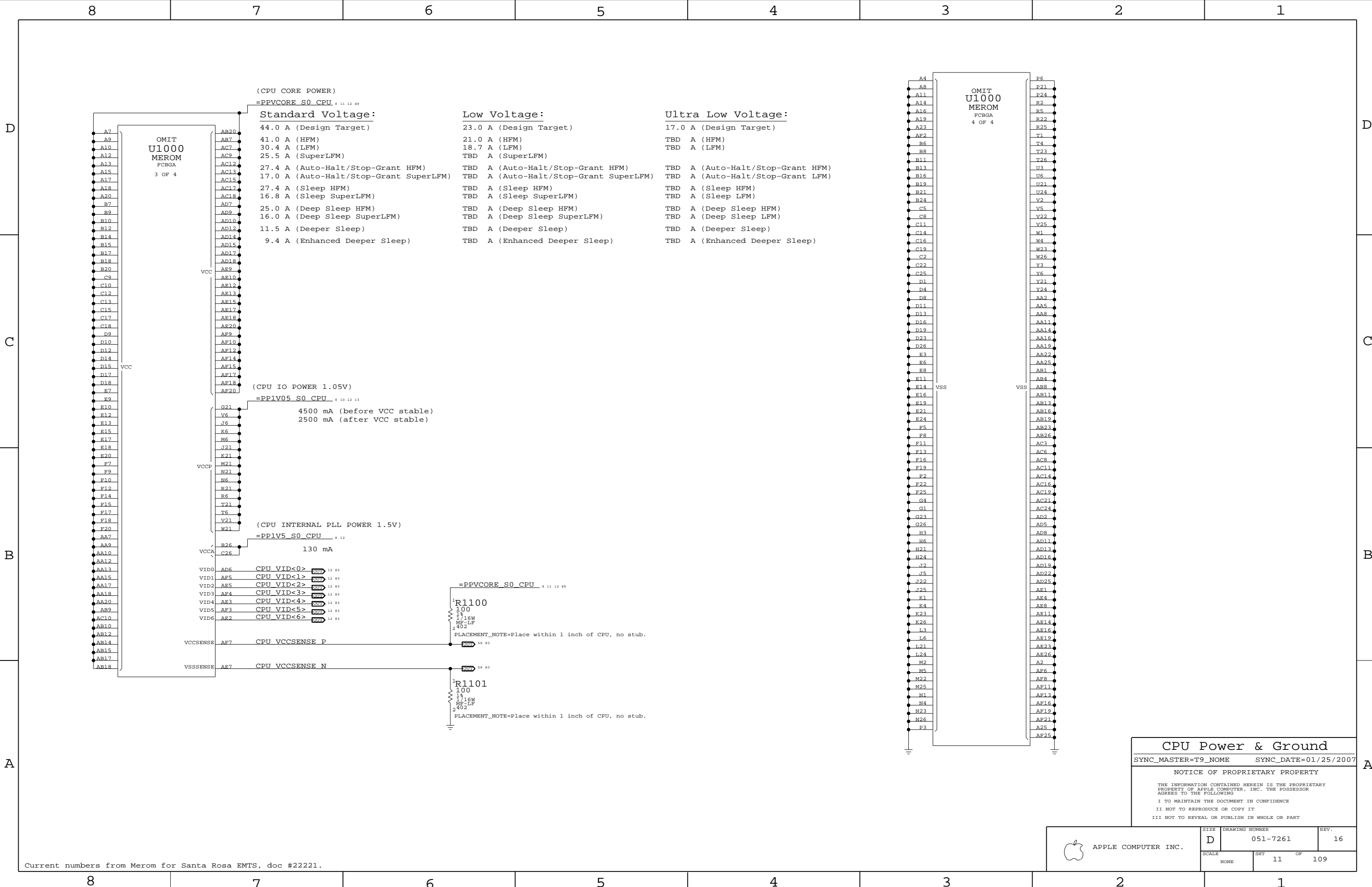
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NONE	9	109





CPU Power & Ground

SYNC_MASTER=T9_NOME

SYNC_DATE=01/25/2007


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	SCALE NONE	SHT 11	OF 109

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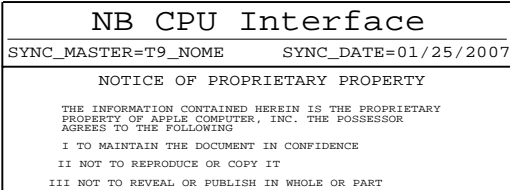
COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	16
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	NONE	13	109

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LVDS Disable

Can leave all signals NC if LVDS is not implemented.
Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

Note: SR DG says to tie LVDS_VREFH/L to GND. This causes a glitch during wake-up on LVDS DATA/CLK pairs. New recommendation is to float both signals, see Radar #5067636.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

CRT & TV-Out Disable

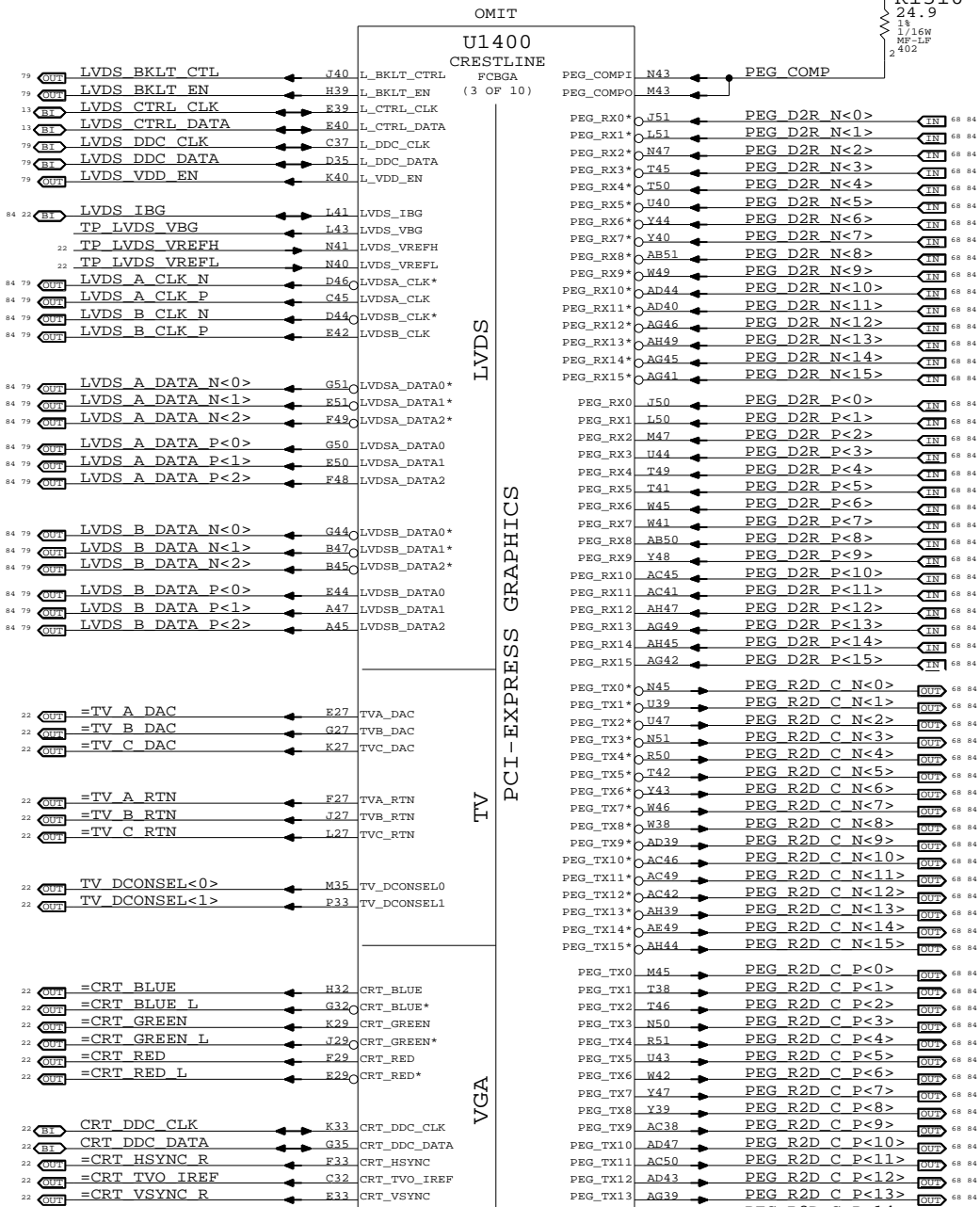
Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TVO_IREF to GND.
Can tie the following rails to GND:
VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above. Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and TV_DCONSELx to GND.

Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.



SDVO Alternate Function

SDVO_TVCLKIN#
SDVO_INT#
SDVO_FLDSTALL#

SDVO_TVCLKIN
SDVO_INT
SDVO_FLDSTALL

SDVOB_RED#
SDVOB_GREEN#
SDVOB_BLUE#
SDVOB_CLKN
SDVOC_RED#
SDVOC_GREEN#
SDVOC_BLUE#
SDVOC_CLKN

SDVOB_RED
SDVOB_GREEN
SDVOB_BLUE
SDVOB_CLKP
SDVOC_RED
SDVOC_GREEN
SDVOC_BLUE
SDVOC_CLKP

NB PEG / Video Interfaces

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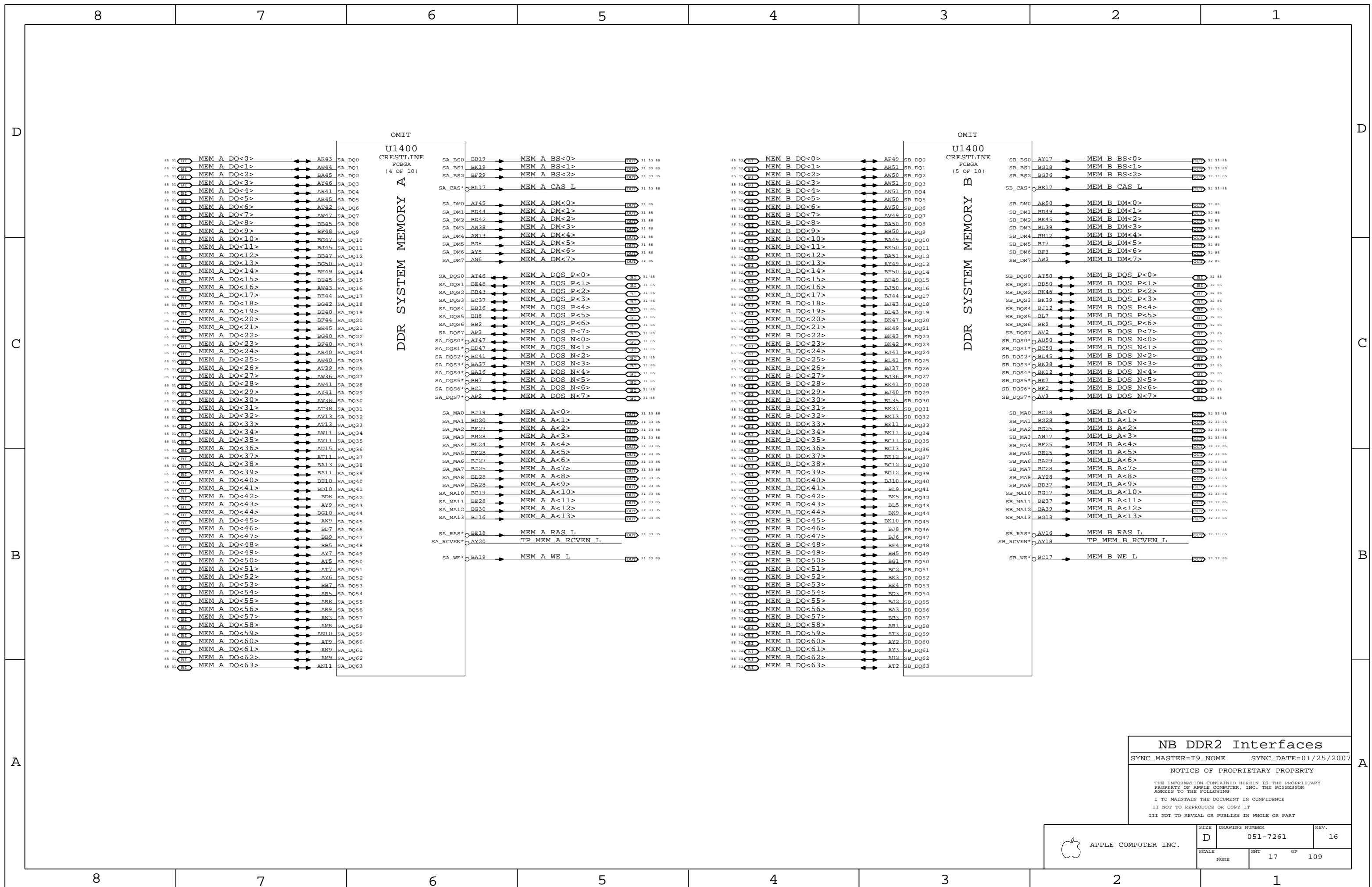
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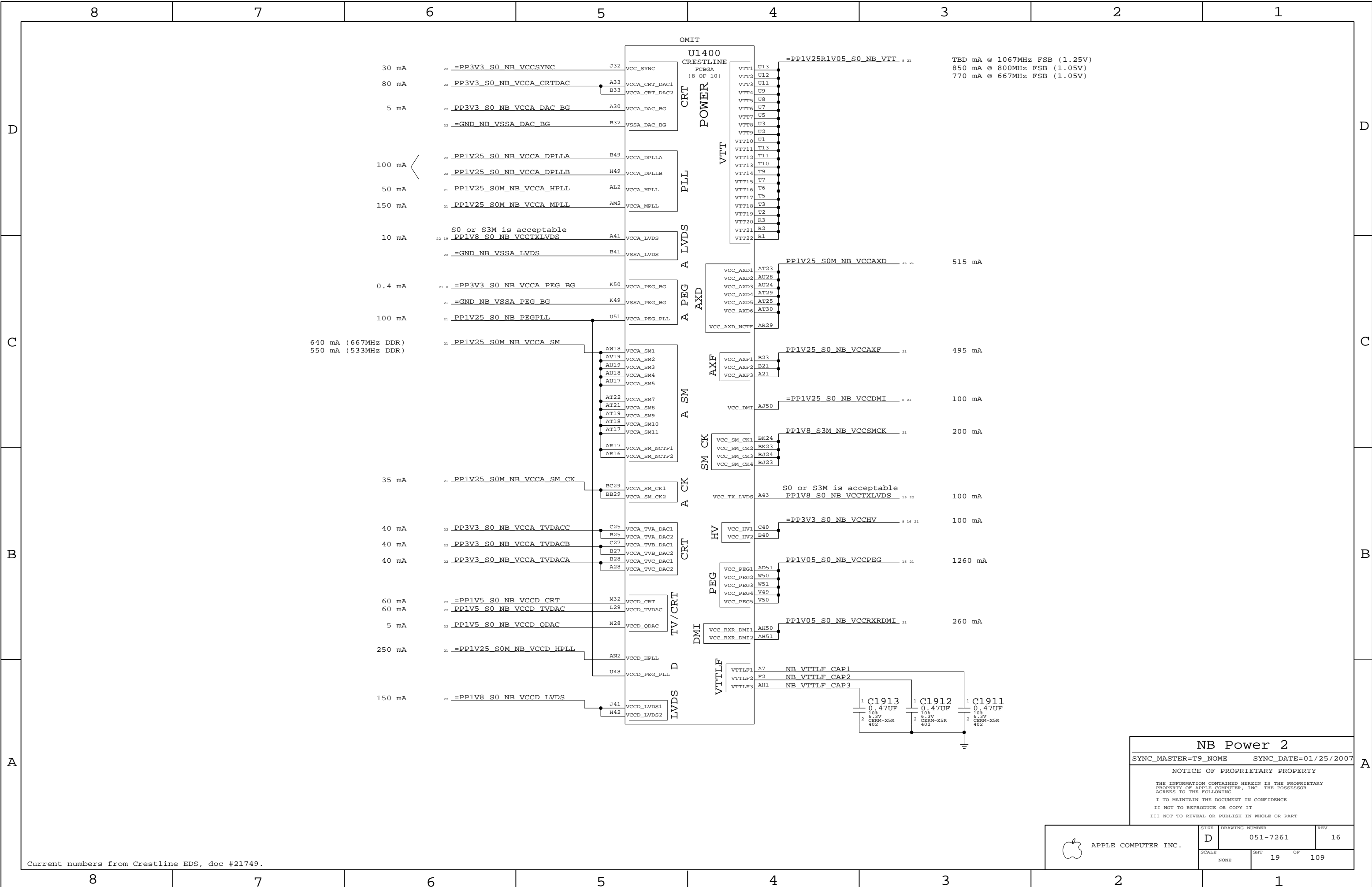
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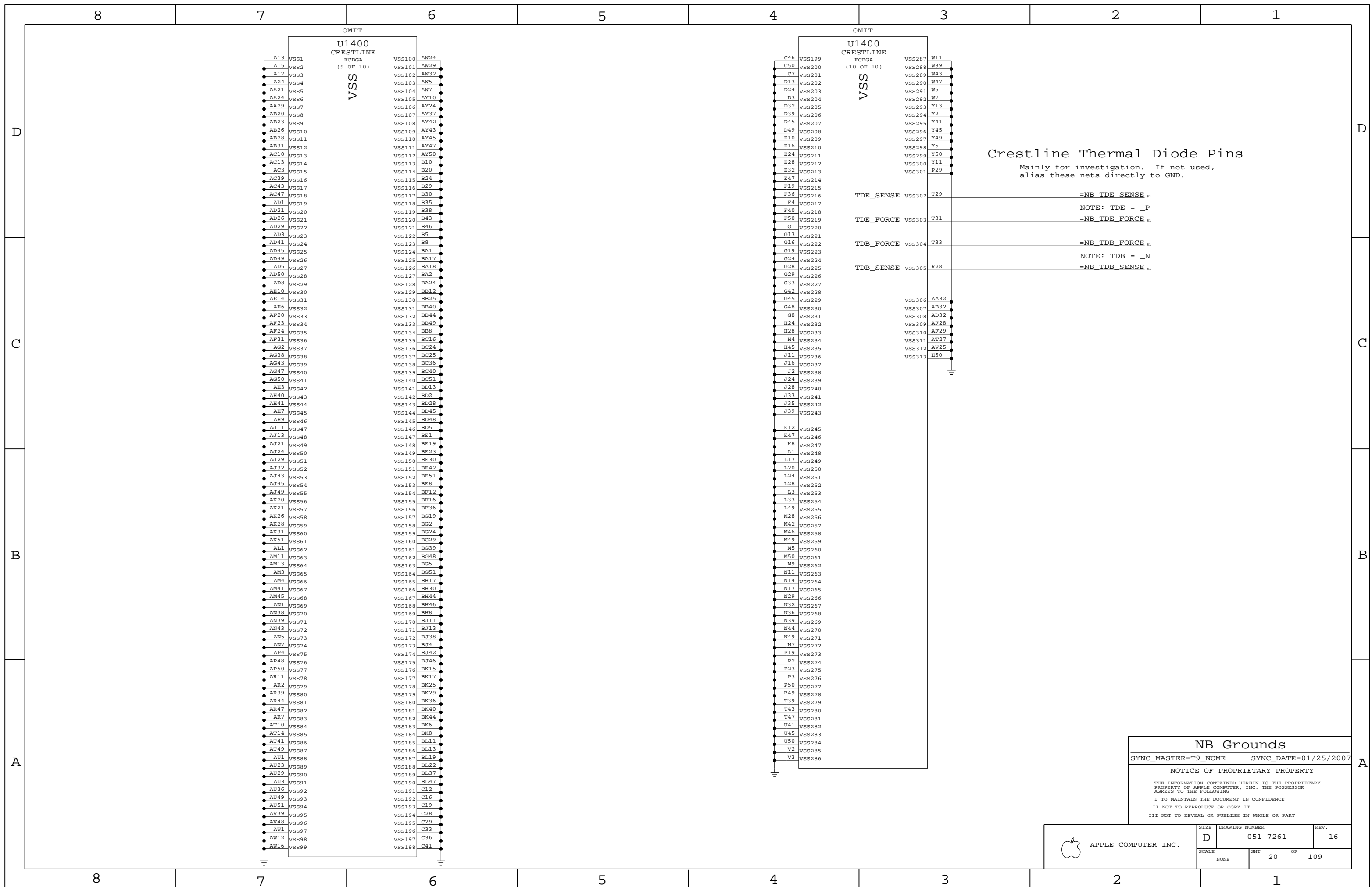
A

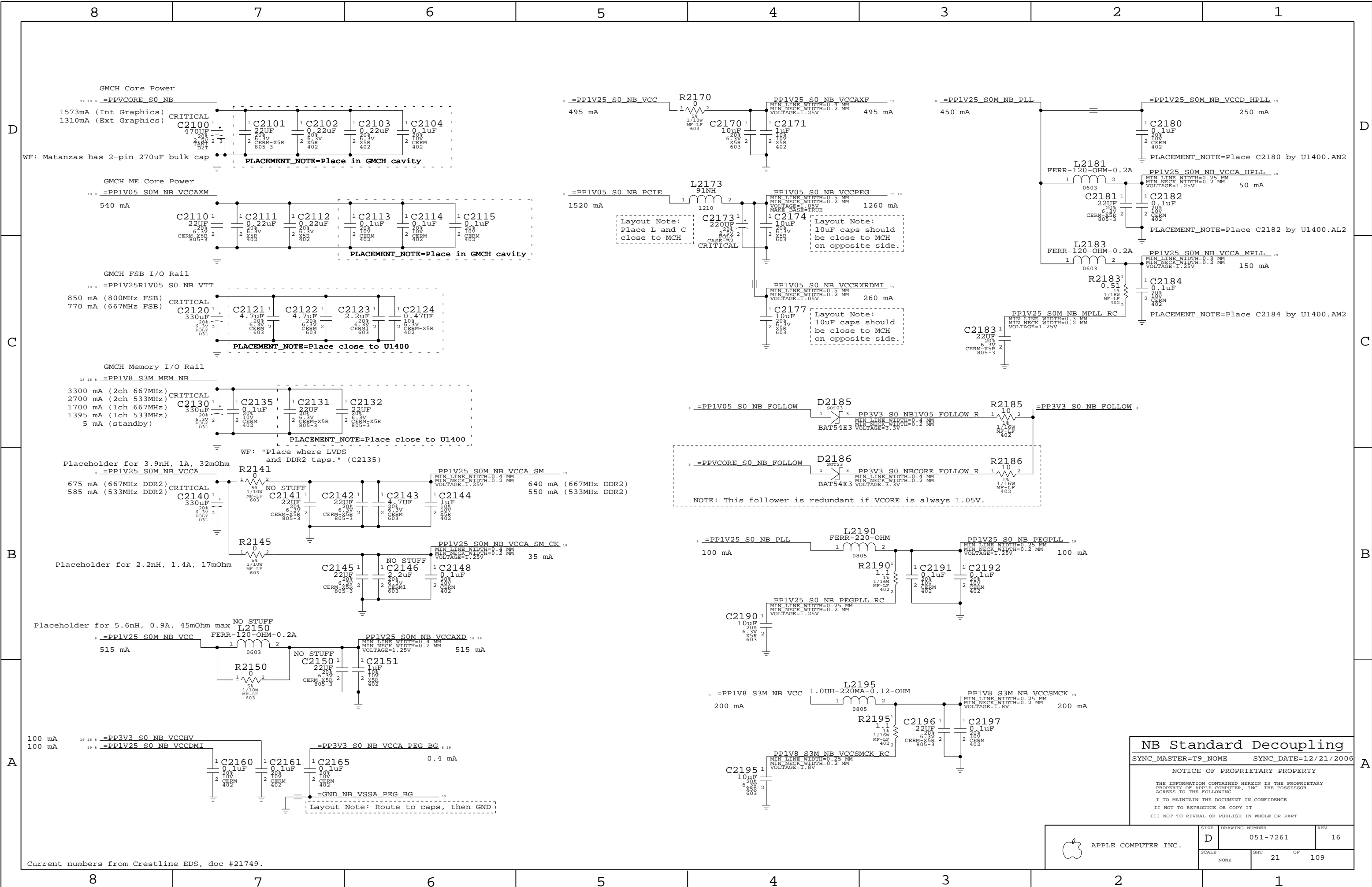
D

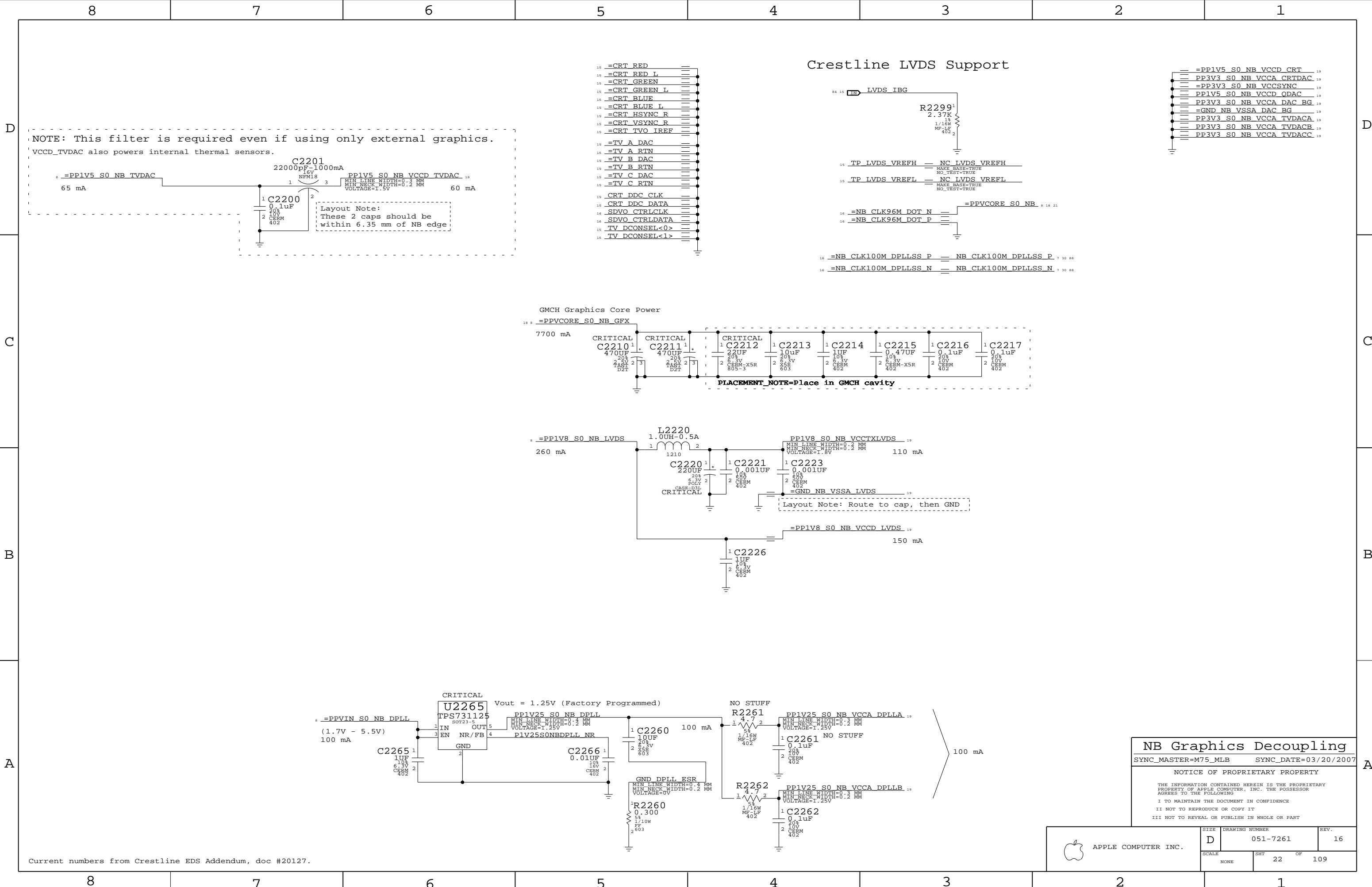
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NOTE: This filter is required even if using only external graphics.
VCCD_TV DAC also powers internal thermal sensors.

PP1V5 S0 NB TVDAC 65 mA

C2201 22000PF-1000mA 16V NFW18

PP1V5 S0 NB VCCD TVDAC 60 mA

C2200 0.1uF 20% 10V CERM 402

Layout Note:
These 2 caps should be within 6.35 mm of NB edge

=CRT RED
=CRT RED L
=CRT GREEN
=CRT GREEN L
=CRT BLUE
=CRT BLUE L
=CRT HSYNC R
=CRT VSYNC R
=CRT TWO IREF
=TV A DAC
=TV A RTN
=TV B DAC
=TV B RTN
=TV C DAC
=TV C RTN
CRT DDC CLK
CRT DDC DATA
SDVO CTRLCLK
SDVO CTRLDATA
TV DCONSEL<0>
TV DCONSEL<1>

Crestline LVDS Support

LVDS IBG

R2299 2.37K 1/16W MF-10 402

TP LVDS VREFH NC LVDS VREFH MAKE BASE=TRUE NO_TEST=TRUE

TP LVDS VREFL NC LVDS VREFL MAKE BASE=TRUE NO_TEST=TRUE

=NB CLK96M DOT N
=NB CLK96M DOT P

=PPVCORE S0 NB

=NB CLK100M DPLLSS P NB CLK100M DPLLSS P

=NB CLK100M DPLLSS N NB CLK100M DPLLSS N

=PP1V5 S0 NB VCCD CRT
PP3V3 S0 NB VCCA CRTDAC
PP3V3 S0 NB VCCSYN
PP1V5 S0 NB VCCD QDAC
PP3V3 S0 NB VCCA DAC BG
=GND NB VSSA DAC BG
PP3V3 S0 NB VCCA TVDAC
PP3V3 S0 NB VCCA TVDACB
PP3V3 S0 NB VCCA TVDACC

GMCH Graphics Core Power

=PPVCORE S0 NB GFX 7700 mA

CRITICAL C2210 470UF 20% 25V TANT D27

CRITICAL C2211 470UF 20% 25V TANT D27

CRITICAL C2212 22UF 20% 25V CERM-X5R 805-3

C2213 10uF 20% 25V CERM 402

C2214 1uF 20% 25V CERM 402

C2215 0.47UF 20% 25V CERM-X5R 402

C2216 0.1uF 20% 25V CERM 402

C2217 0.1uF 20% 25V CERM 402

PLACEMENT NOTE=Place in GMCH cavity

=PP1V8 S0 NB LVDS 260 mA

L2220 1.00UH-0.5A 1210

C2220 220UF 20% 6.3V POLY CASE-032 CRITICAL

C2221 0.001UF 20% 50V CERM 402

C2223 0.001UF 20% 50V CERM 402

=GND NB VSSA LVDS

Layout Note: Route to cap, then GND

=PP1V8 S0 NB VCCD LVDS 150 mA

C2226 1uF 20% 50V CERM 402

CRITICAL U2265 TPS731125 SOT23-5

Vout = 1.25V (Factory Programmed)

=PPVIN S0 NB DPLL 100 mA (1.7V - 5.5V)

C2265 1uF 20% 6.3V CERM 402

PP1V25 S0 NB DPLL 100 mA

P1V25S0NBDPLL NR

C2266 0.01UF 20% 16V CERM 402

GND DPLL ESR

R2260 0.300 5% 1/10W PF 603

NO STUFF R2261 4.7 1/16W MF-10 402

PP1V25 S0 NB VCCA DPLLA 100 mA

C2261 0.1uF 20% 50V CERM 402

R2262 4.7 1/16W MF-10 402

PP1V25 S0 NB VCCA DPLLB 100 mA

C2262 0.1uF 20% 50V CERM 402

NB Graphics Decoupling

SYNC_MASTER=M75_MLB SYNC_DATE=03/20/2007

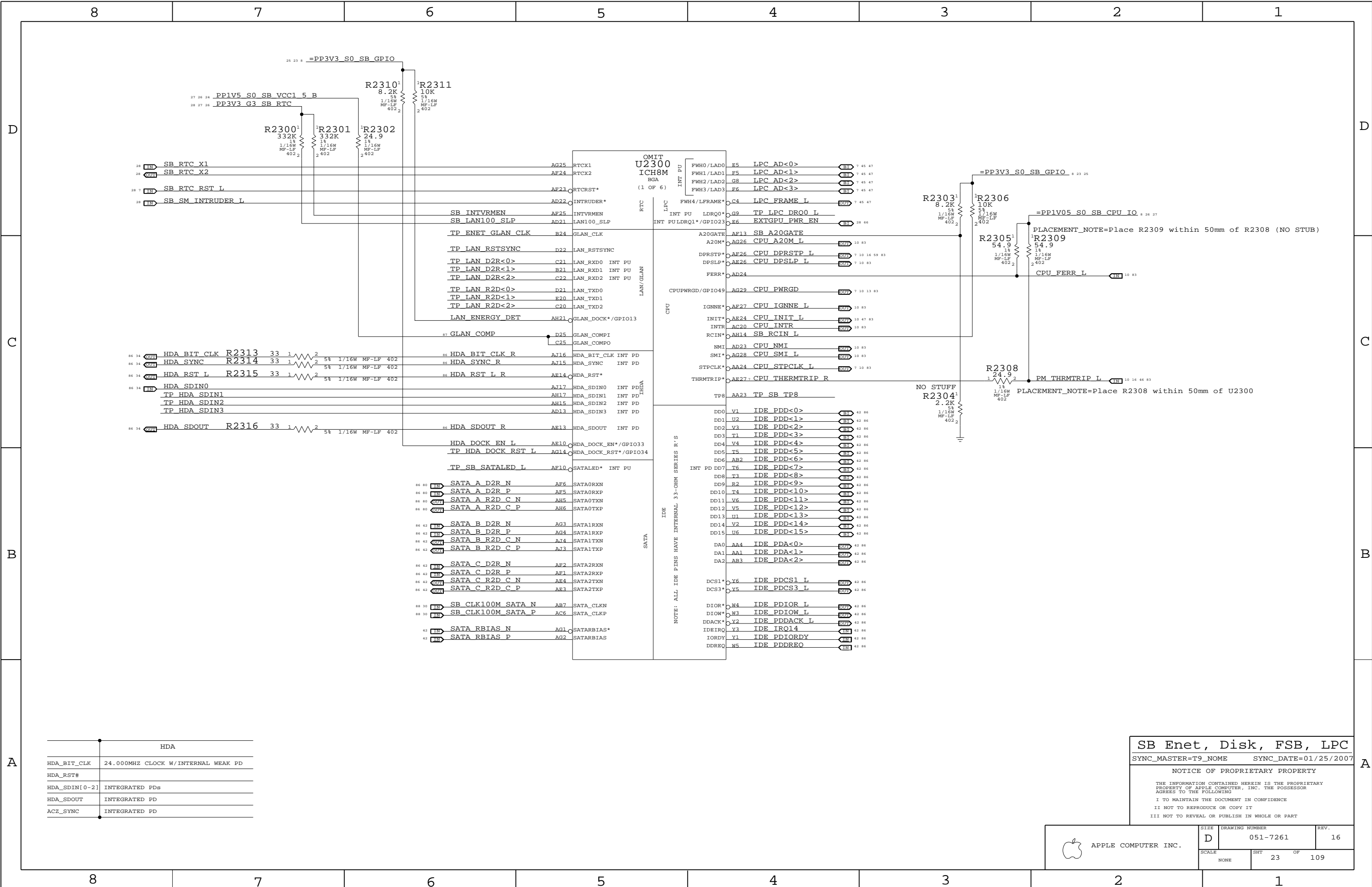
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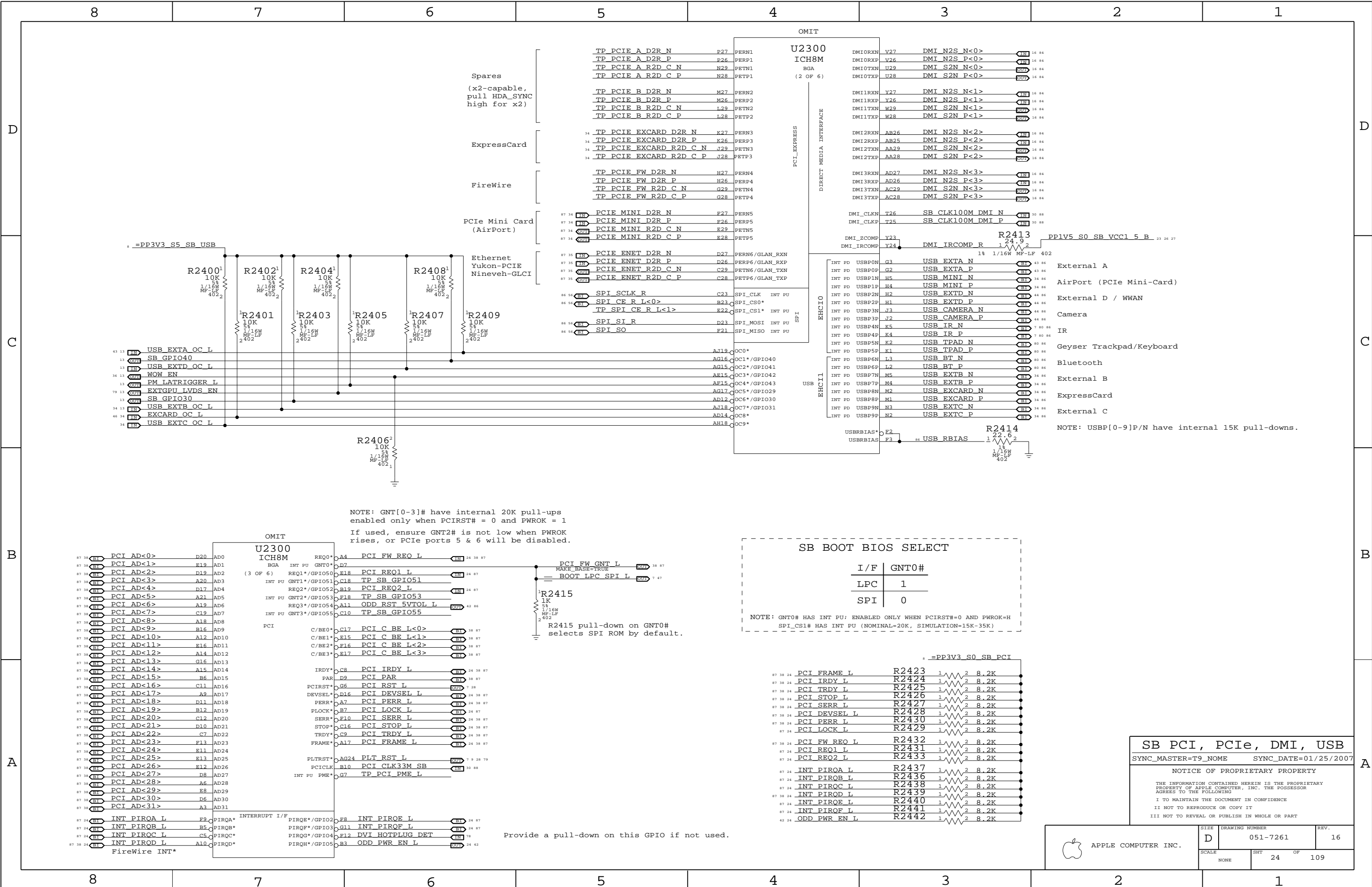
SIZE	DRAWING NUMBER	REV.
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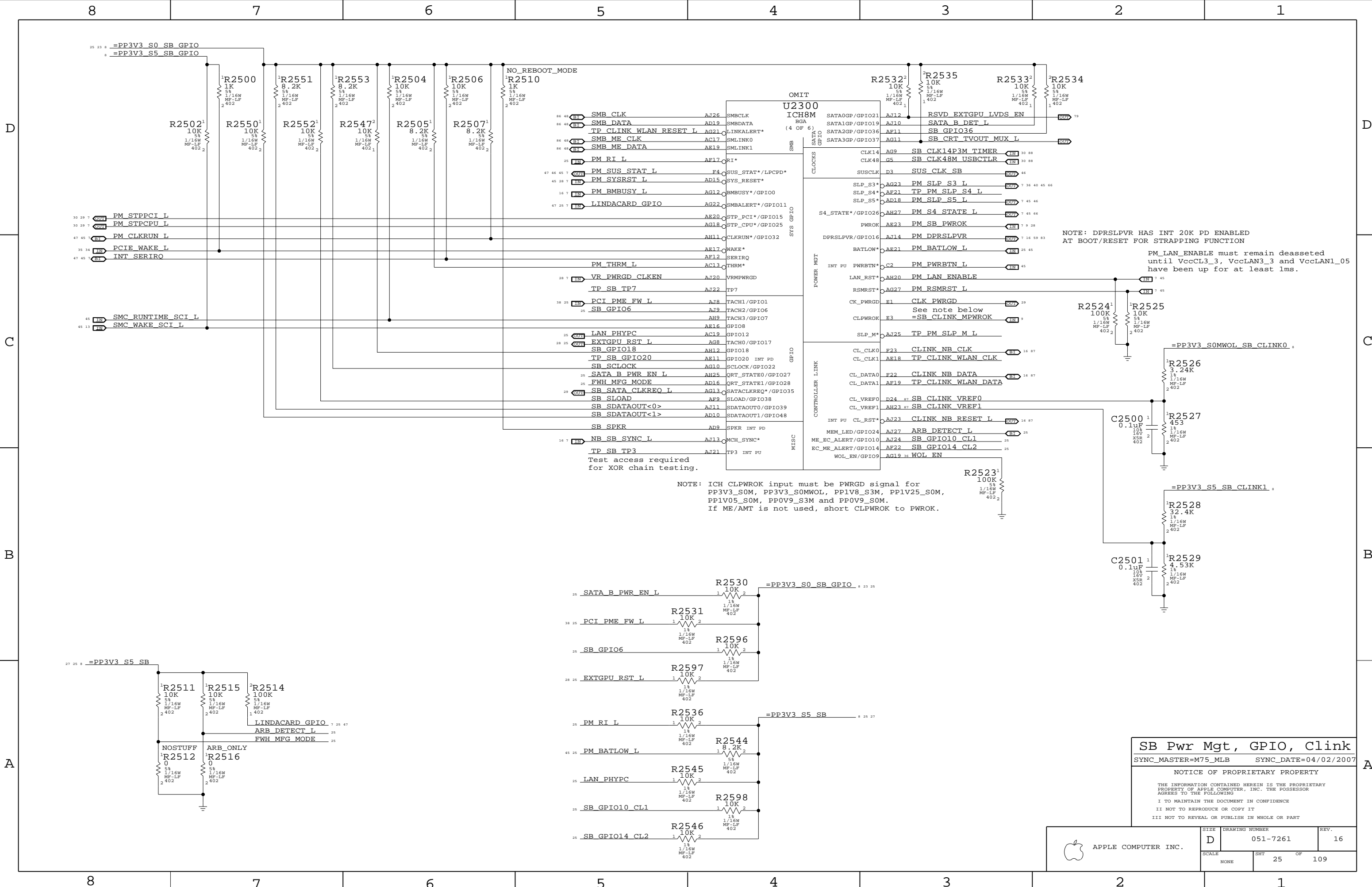


HDA	
HDA_BIT_CLK	24.000MHZ CLOCK W/INTERNAL WEAK PD
HDA_RST#	
HDA_SDIN[0-2]	INTEGRATED PDs
HDA_SDOUT	INTEGRATED PD
ACZ_SYNC	INTEGRATED PD

SB Enet, Disk, FSB, LPC	
SUB_MASTER=T9_NOME	SUB_DATE=01/25/2007
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NOTE: ICH CLPWROK input must be PWRGD signal for
PP3V3_S0M, PP3V3_S0MWOL, PP1V8_S3M, PP1V25_S0M,
PP1V05_S0M, PP0V9_S3M and PP0V9_S0M.
If ME/AMT is not used, short CLPWROK to PWROK.

NOTE: DPRSLPVR HAS INT 20K PD ENABLED
AT BOOT/RESET FOR STRAPPING FUNCTION

PM_LAN_ENABLE must remain deasserted
until VccCL3_3, VccLAN3_3 and VccLAN1_05
have been up for at least 1ms.

SB Pwr Mgt, GPIO, Clink

SYNC_MASTER=M75_MLB SYNC_DATE=04/02/2007

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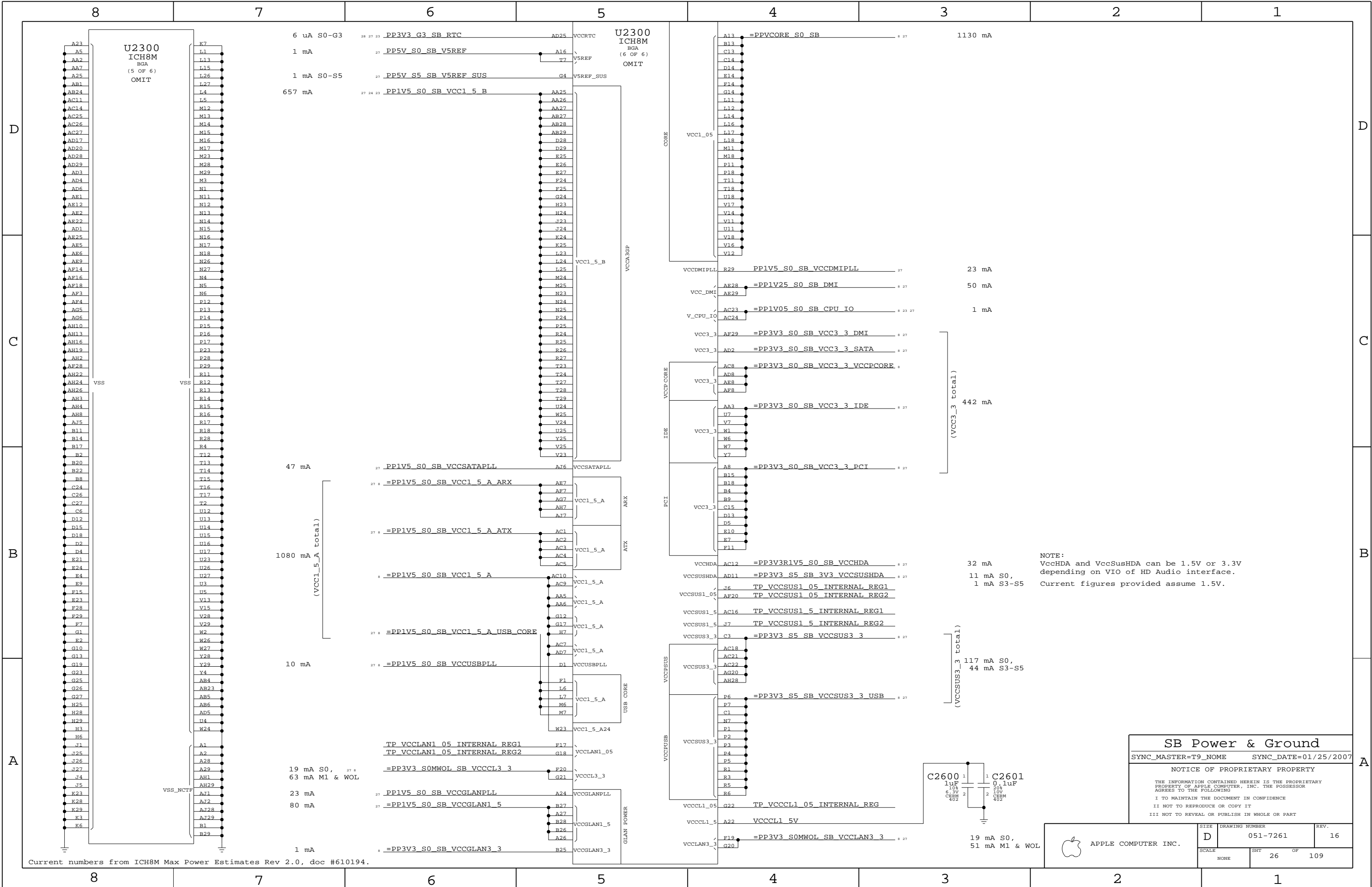
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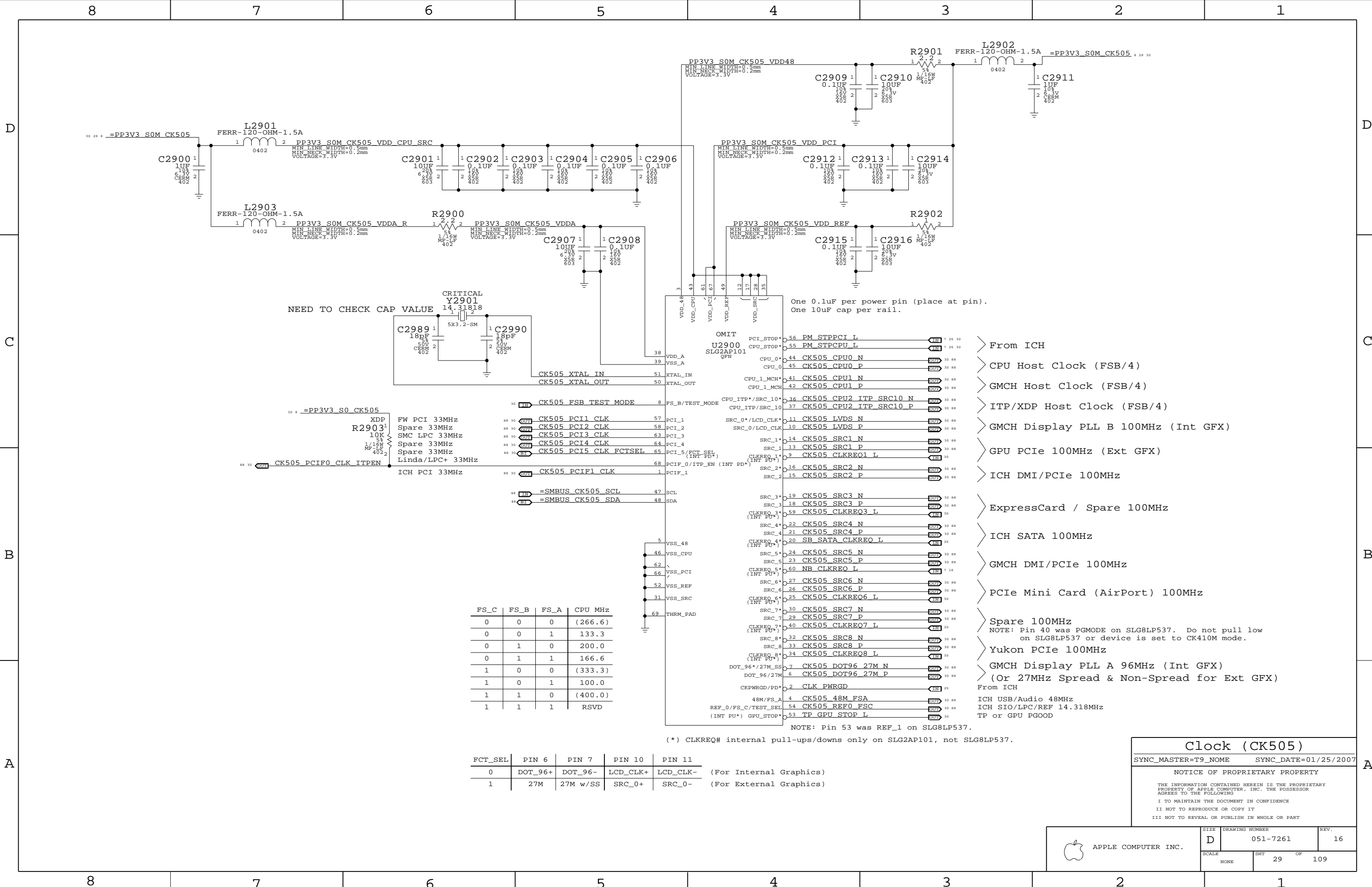


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Clock (CK505)

SYNC_MASTER=T9_NOME

SYNC_DATE=01/25/2007

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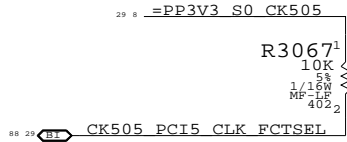
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

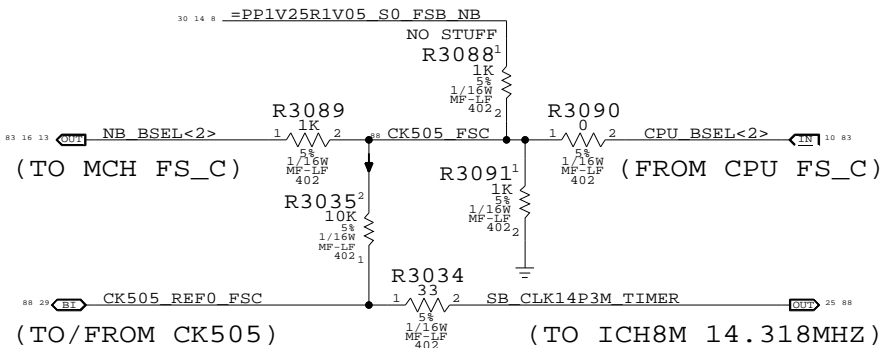
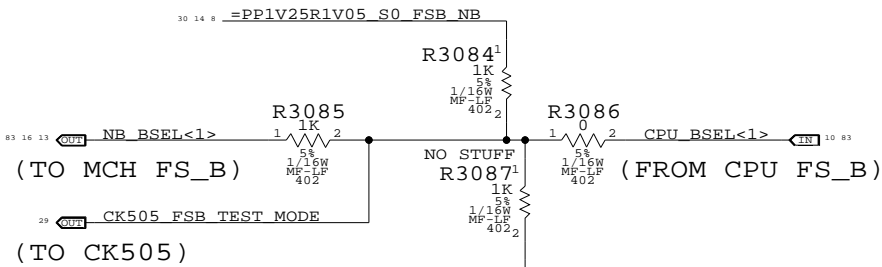
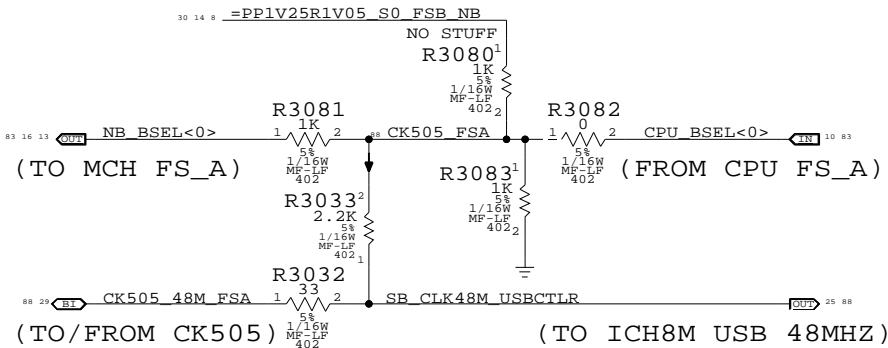
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CK505 Configuration Straps

FCT_SEL (GFX clock select)



FS_A, FS_B, FS_C (Host clock freq select)



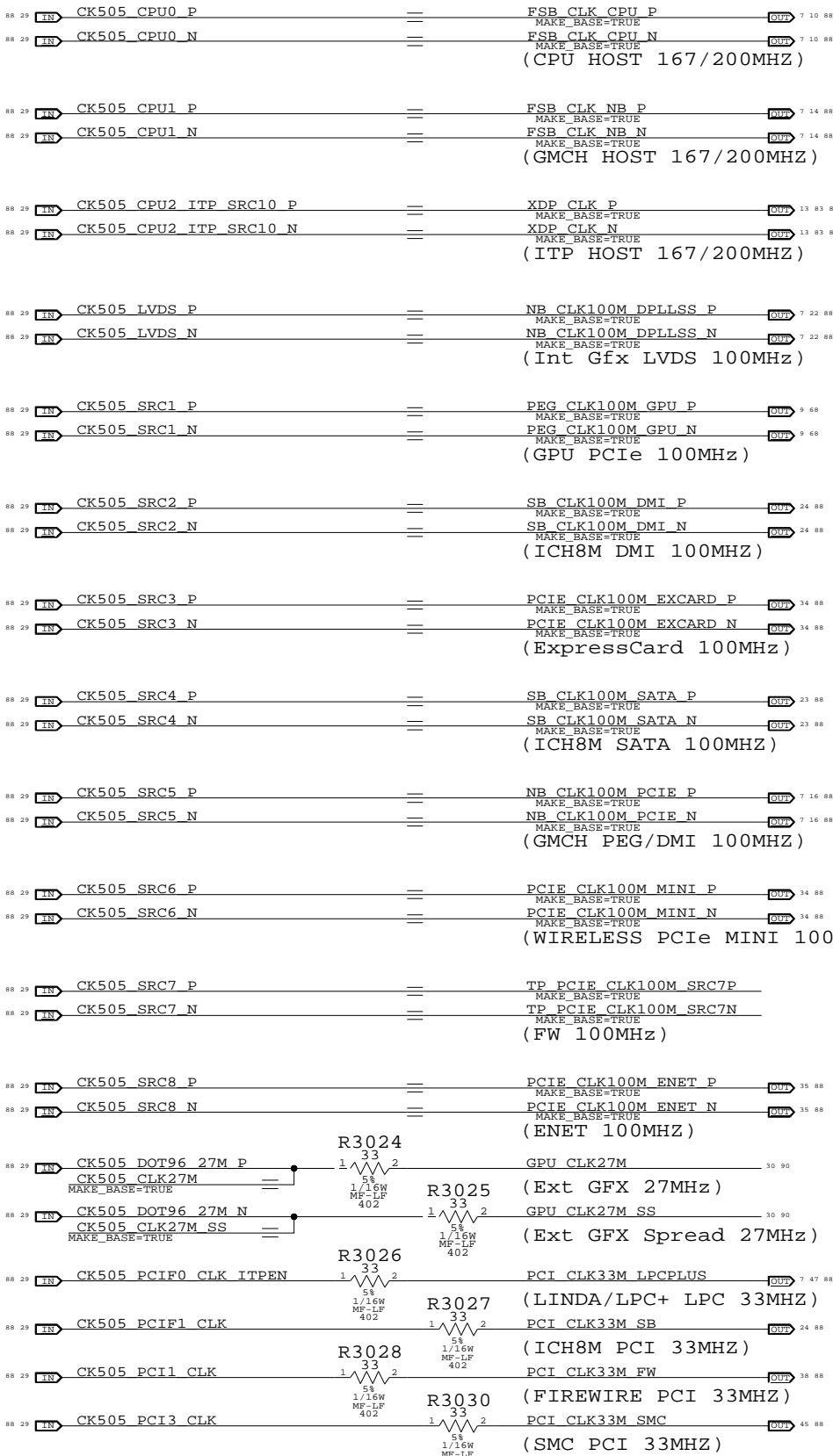
FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

NO STUFF R3082, R3086 & R3090 for manual CPU clk frequency.

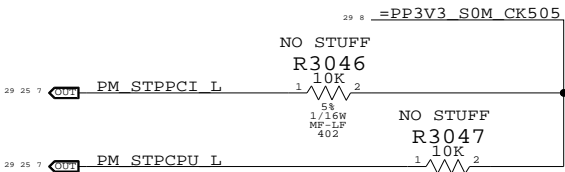
(Only 100-200MHz supported by SLG8LP536 and CY28545-5)

CLK Termination

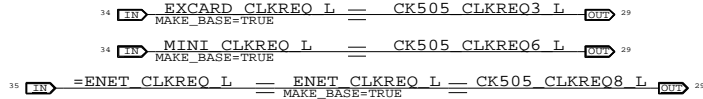
(Note: HOST/SRC/GFX clock termination removed. Silego SL8GLP536 or equiv. support only)



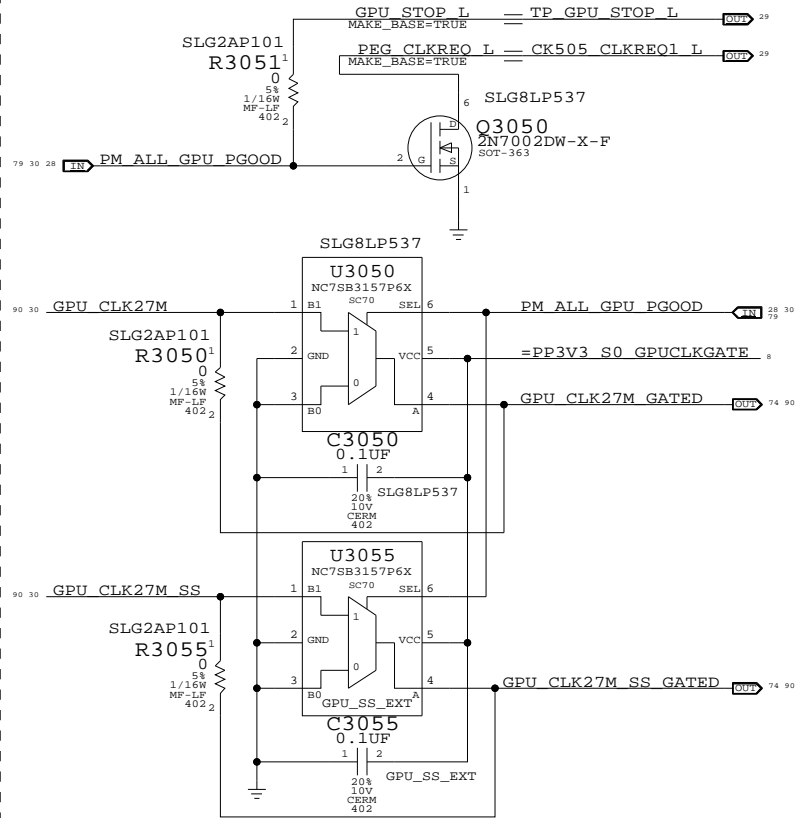
CLKREQ Controls



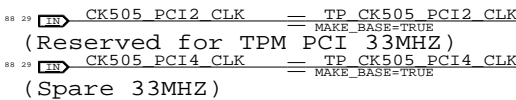
Silego SLG2AP101 has internal pull-ups on all CLKREQ# pins. Support for SL8GLP537 or equiv. only. NB and SATA CLKREQs are not remappable (and thus are not shown here).



GPU Clock Gating



Unused Clocks



Clock Termination

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Page Notes

Power aliases required by this page:

- =PP1V8_S3M_MEM_B
- =PP0V9_S3M_MEM_DIMMVREFB
- =PPSPD_S0M_MEM_B (2.5V - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:

(NONE)

"Expansion" (surface-mount) slot

DDR2 Bypass Caps

(For return current)

DDR2 SO-DIMM Connector B

SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

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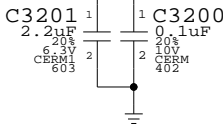
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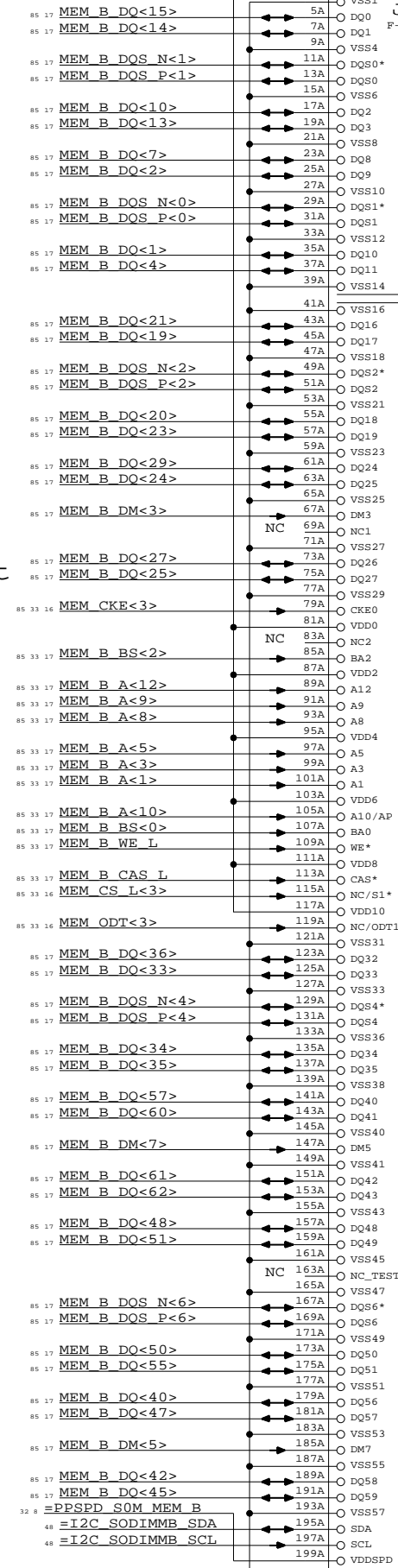
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=PP0V9_S3M_MEM_DIMMVREFB



=PP1V8_S3M_MEM_B

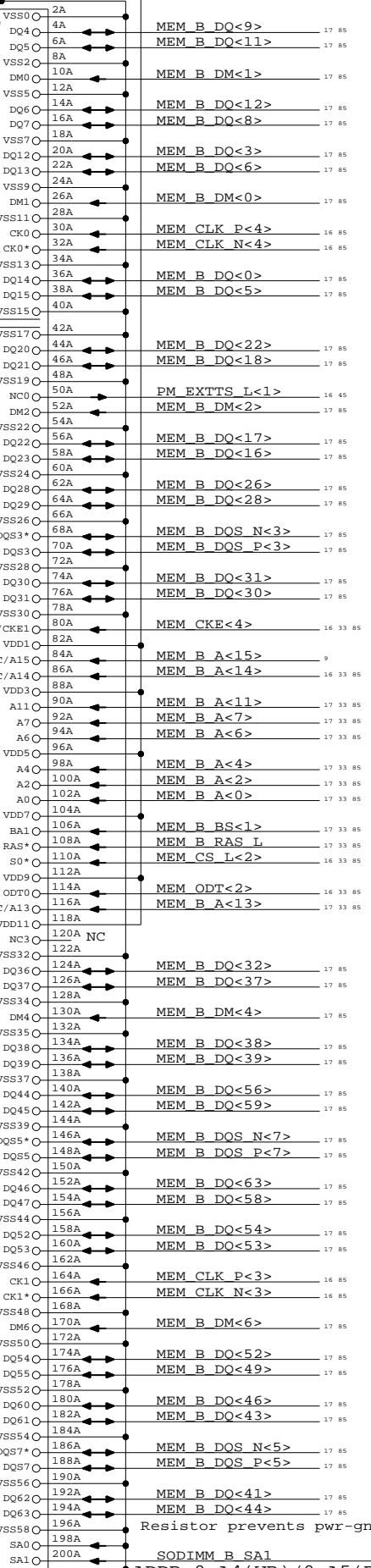


203
201

CRITICAL
J3200
F-RT-SM-M9

DDR2-SODIMM-DUAL

=PP1V8_S3M_MEM_B

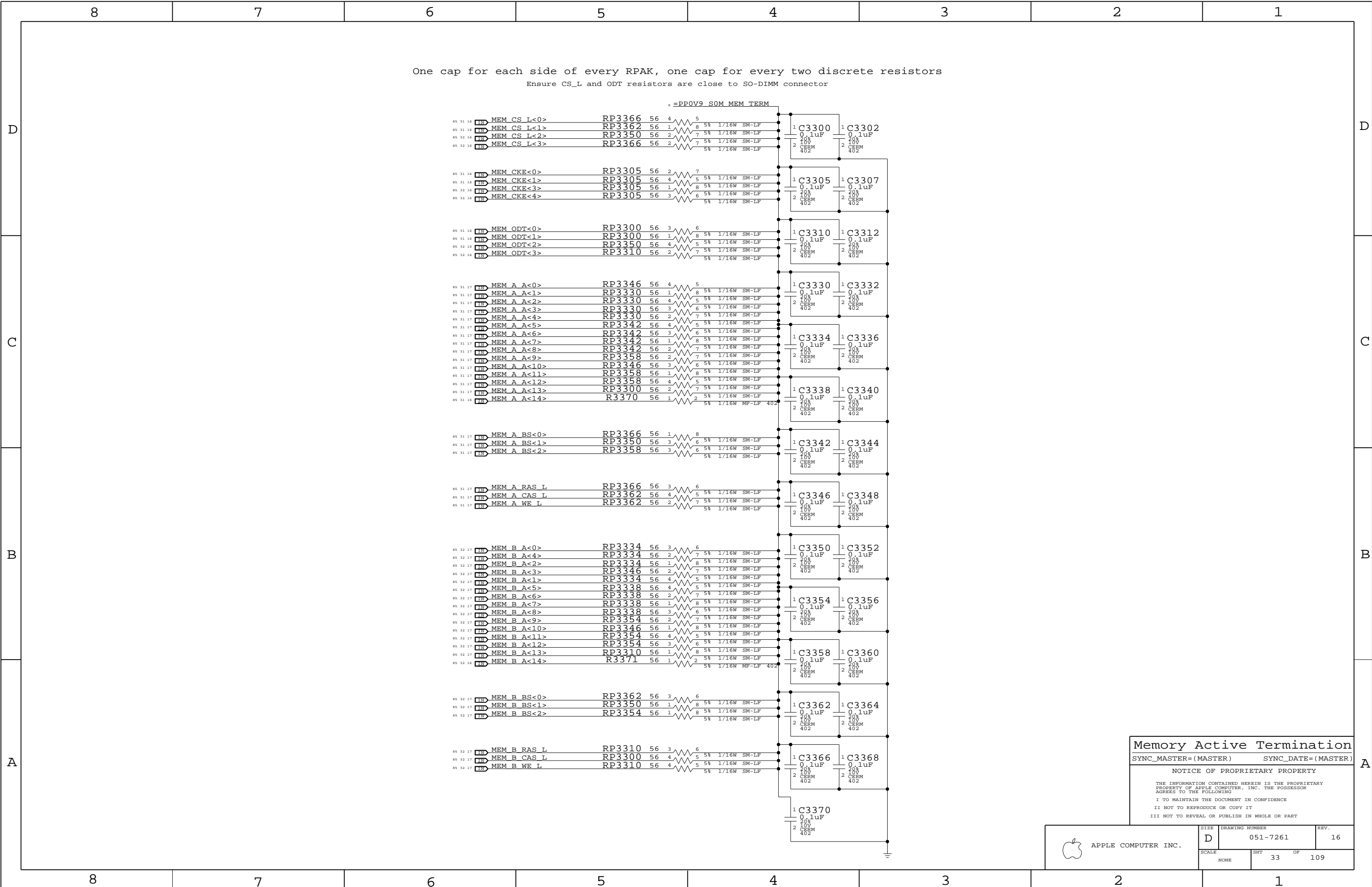


=PPSPD_S0M_MEM_B



ADDR=0xA4 (WR) / 0xA5 (RD)

516S0471



Memory Active Termination

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

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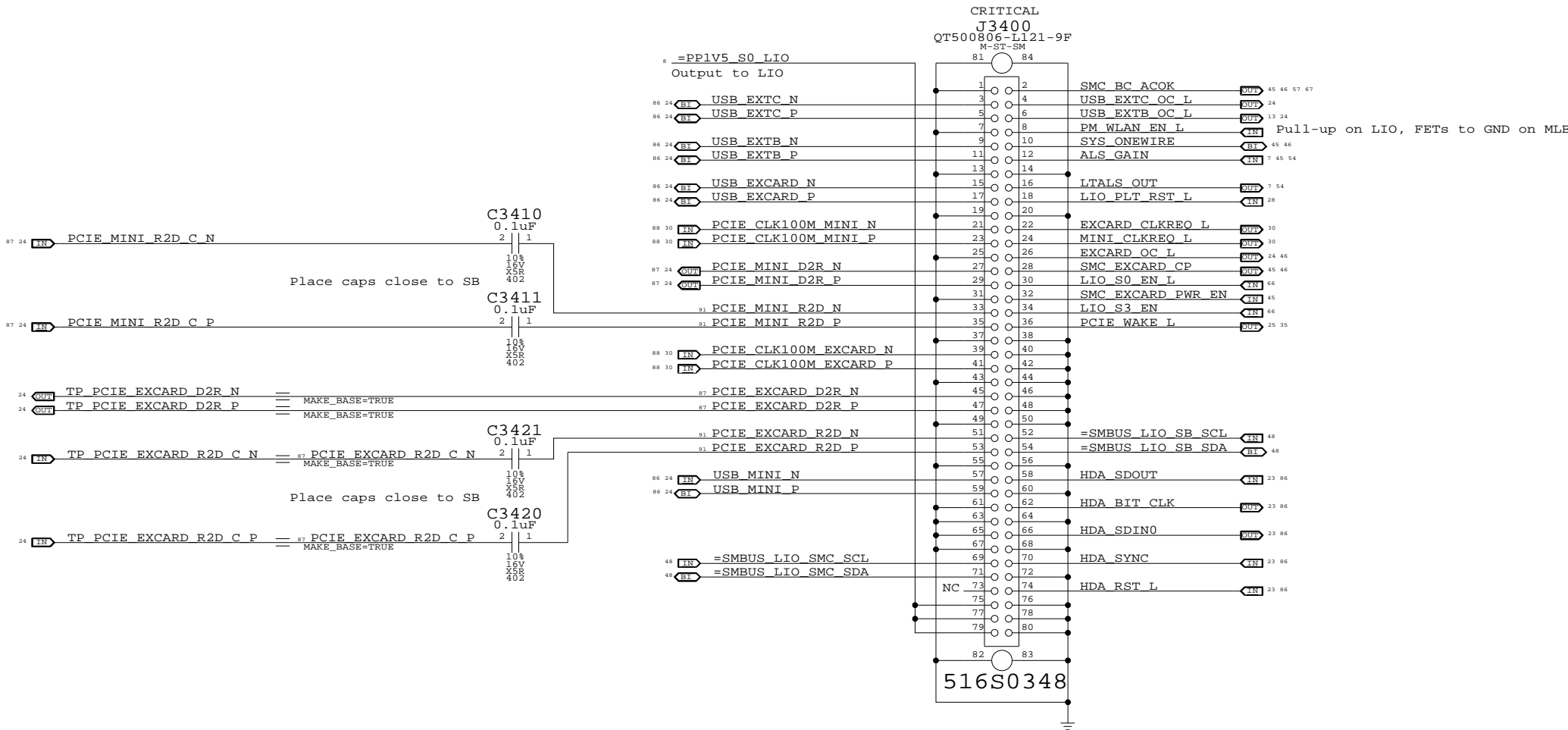
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Left I/O Board Connector



Left I/O Board Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0386	1	IC,88E058,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	YUKON_ULTRA
341S2060	1	IC,FLASH,88E058 ETHERNET VPD,IIC,S08	U3780	CRITICAL	YUKON_ULTRA
338S0270	1	IC,88E053,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	YUKON_EC
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,S08	U3780	CRITICAL	YUKON_EC
114S0285	1	RES,4.87K,1%,1/16W,0402,LF	R3760		YUKON_EC

- Alias =YUKON_EC_PP2V5_ENET to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF and 1x 0.001uF caps
- Use 0-ohm resistors or variable supply to provide 1.8V or 2.5V to =PP1V8R2V5_ENET_PHY and magnetics. Can also use BCP69T1 connected to CTRL18 pin 4 for internal VR.
- Connect =ENET_CLKREQ_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON_ULTRA)
- Use YUKON_EC and YUKON_ULTRA BOMOPTIONS to select stuffed part

Ethernets (Yukon)

SYNC_MASTER=T9_NOME	SYNC_DATE=01/25/2007	7
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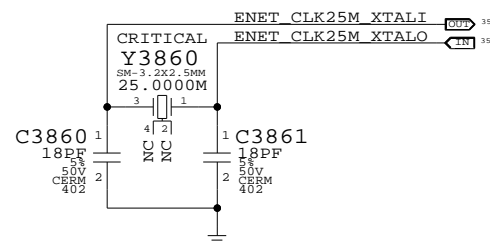


NOTE: S3 term is guaranteed by FET & pull-up source, MUST BE S3 RAIL.

1.9V for Yukon Ultra, 2.5V for Yukon EC
Yukon Ultra requires 1.9V on its magnetics to pass compliance tests

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0363	1	RES,31.6K,1%,1/16W,402,LF	R3855		YUKON_EC

Yukon Crystal



Yukon Power Control

SYNC_MASTER=T9_NOME	SYNC_DATE=03/19/2007	7
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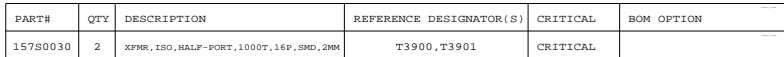
SCALE	SHT	OF
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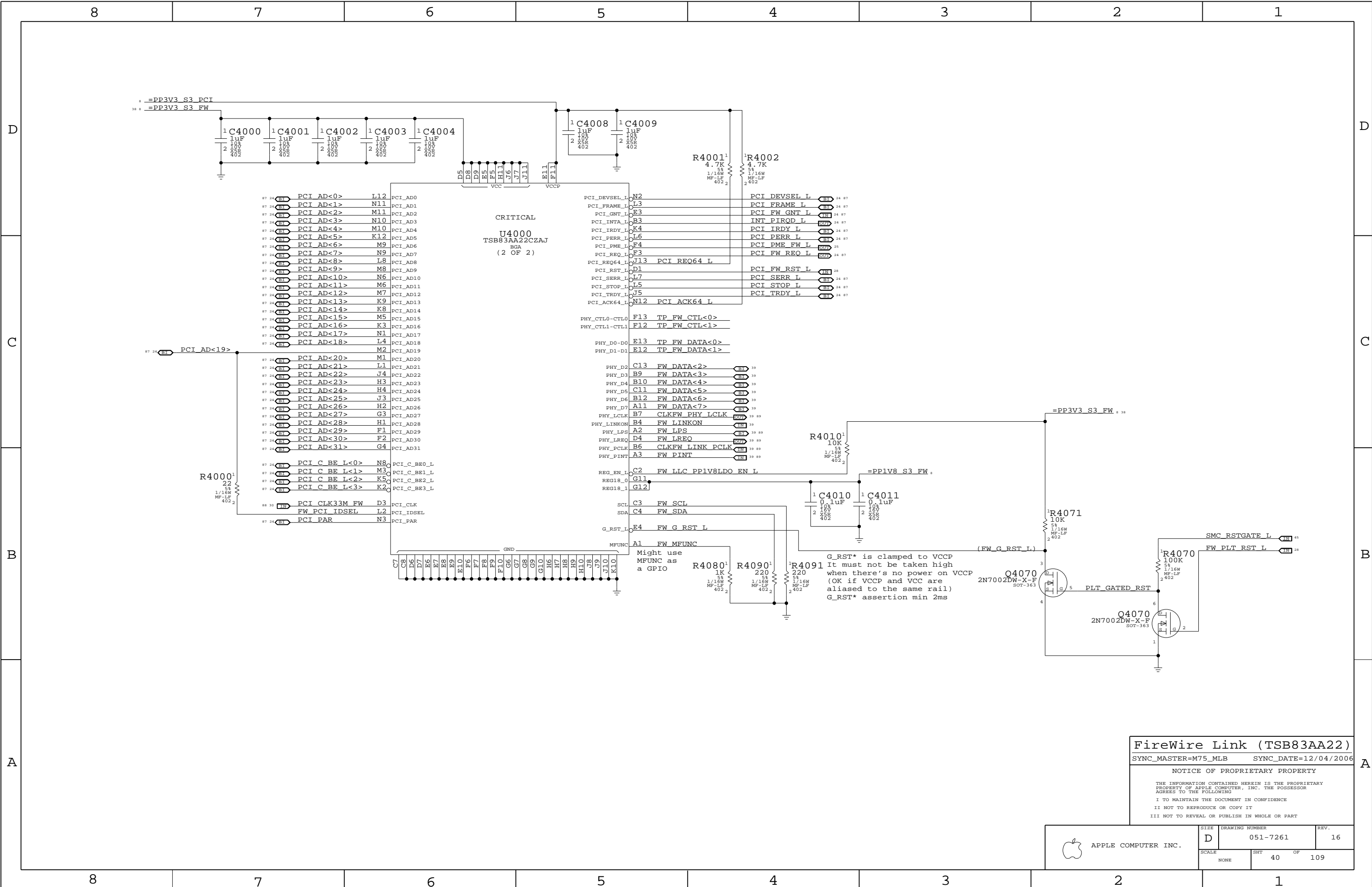
```
Power aliases required by this page:
- =GND_CHASSIS_ENET
```

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Signal aliases required by this page:
(NONE)
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BOM options provided by this page:
(NONE)
```



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FireWire Link (TSB83AA22)

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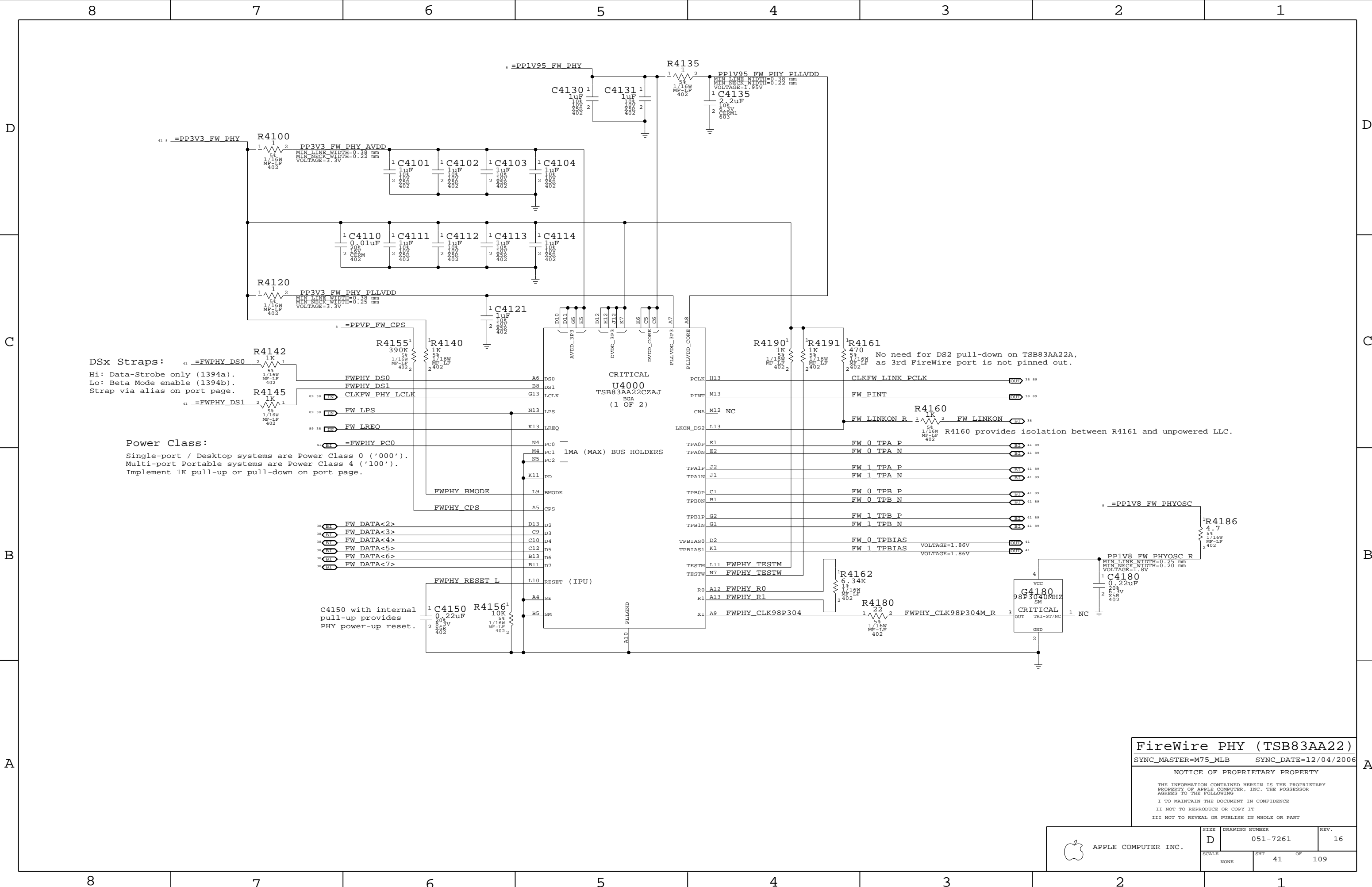
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FireWire PHY (TSB83AA22)

SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006

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Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

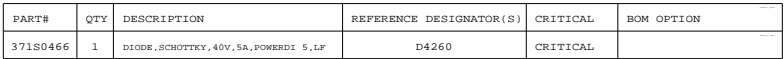
```

```
Signal aliases required by this page:
(NONE)

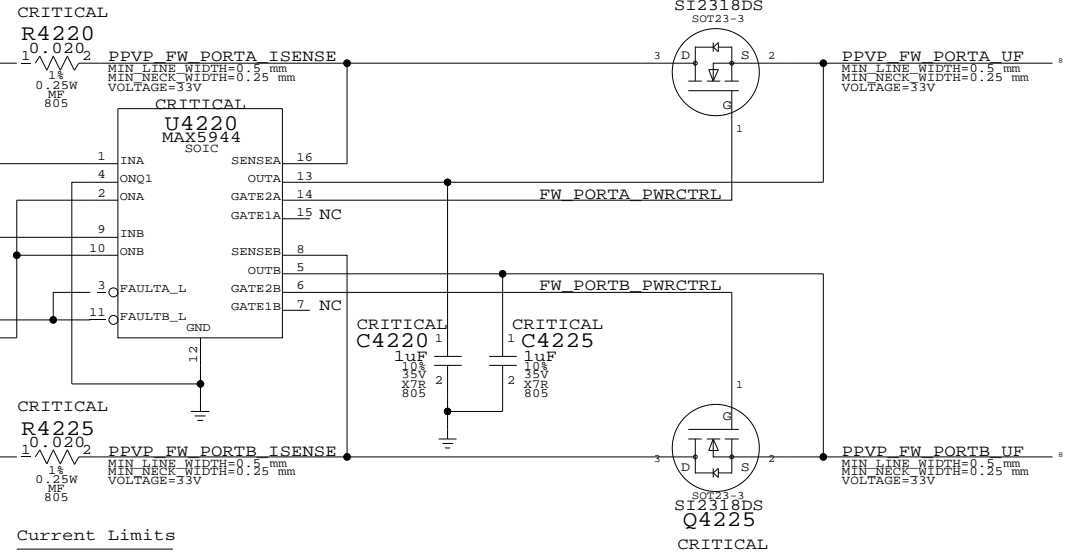
```

```
BOM options provided by this page:
- FW_PORT_FAULT_PU

```



Late-VG Event Detection



MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

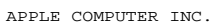
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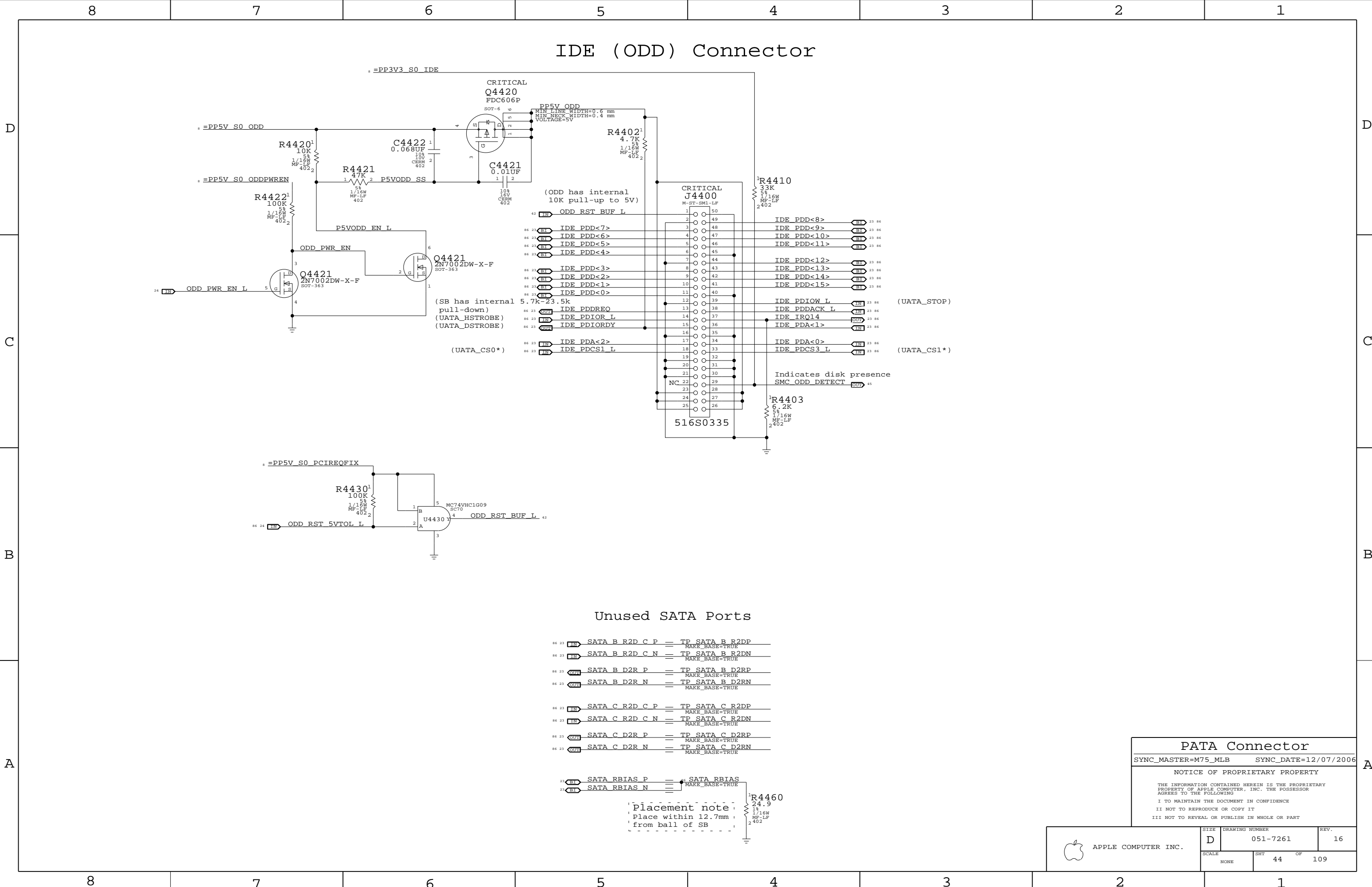
SIZE D	DRAWING NUMBER 051-7261	REV. 16
SCALE NONE	SHT 42	OF 109

8	7	6	5	4	3	2	1
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108

D

D



IDE (ODD) Connector

Unused SATA Ports

86 23	IN	SATA B R2D C P	=	TP SATA B R2DP	MAKE_BASE=TRUE
86 23	IN	SATA B R2D C N	=	TP SATA B R2DN	MAKE_BASE=TRUE
86 23	OUT	SATA B D2R P	=	TP SATA B D2RP	MAKE_BASE=TRUE
86 23	OUT	SATA B D2R N	=	TP SATA B D2RN	MAKE_BASE=TRUE
86 23	IN	SATA C R2D C P	=	TP SATA C R2DP	MAKE_BASE=TRUE
86 23	IN	SATA C R2D C N	=	TP SATA C R2DN	MAKE_BASE=TRUE
86 23	OUT	SATA C D2R P	=	TP SATA C D2RP	MAKE_BASE=TRUE
86 23	OUT	SATA C D2R N	=	TP SATA C D2RN	MAKE_BASE=TRUE

23	IN	SATA RBIAS P	=	SATA RBIAS	MAKE_BASE=TRUE
23	IN	SATA RBIAS N	=	SATA RBIAS	MAKE_BASE=TRUE

Placement note
Place within 12.7mm
from ball of SB

PATA Connector

SYNC_MASTER=M75_MLB SYNC_DATE=12/07/2006

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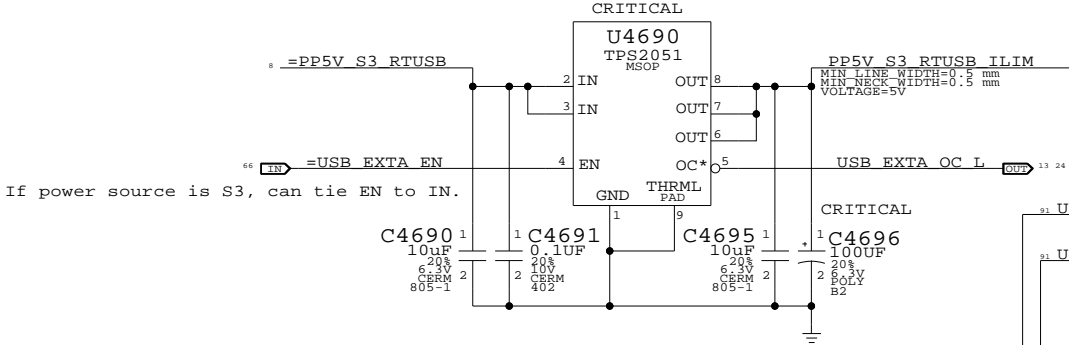
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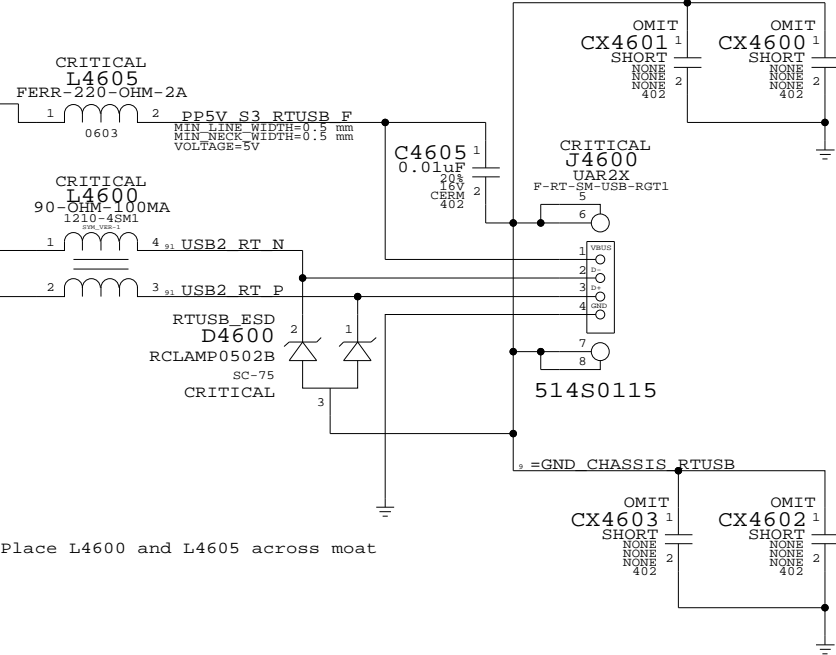
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7261	16
SCALE	SHT	OF
NONE	44	109

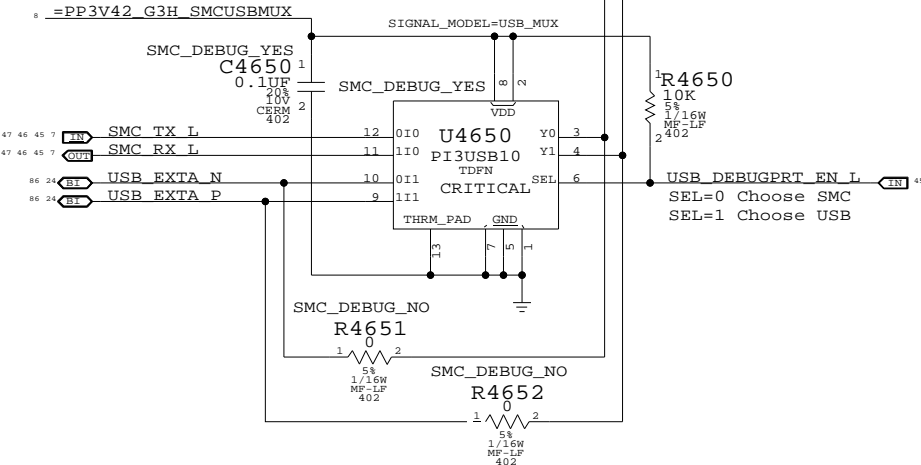
Port Power Switch



Right USB Port



USB/SMC Debug Mux



External USB Connector

SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006

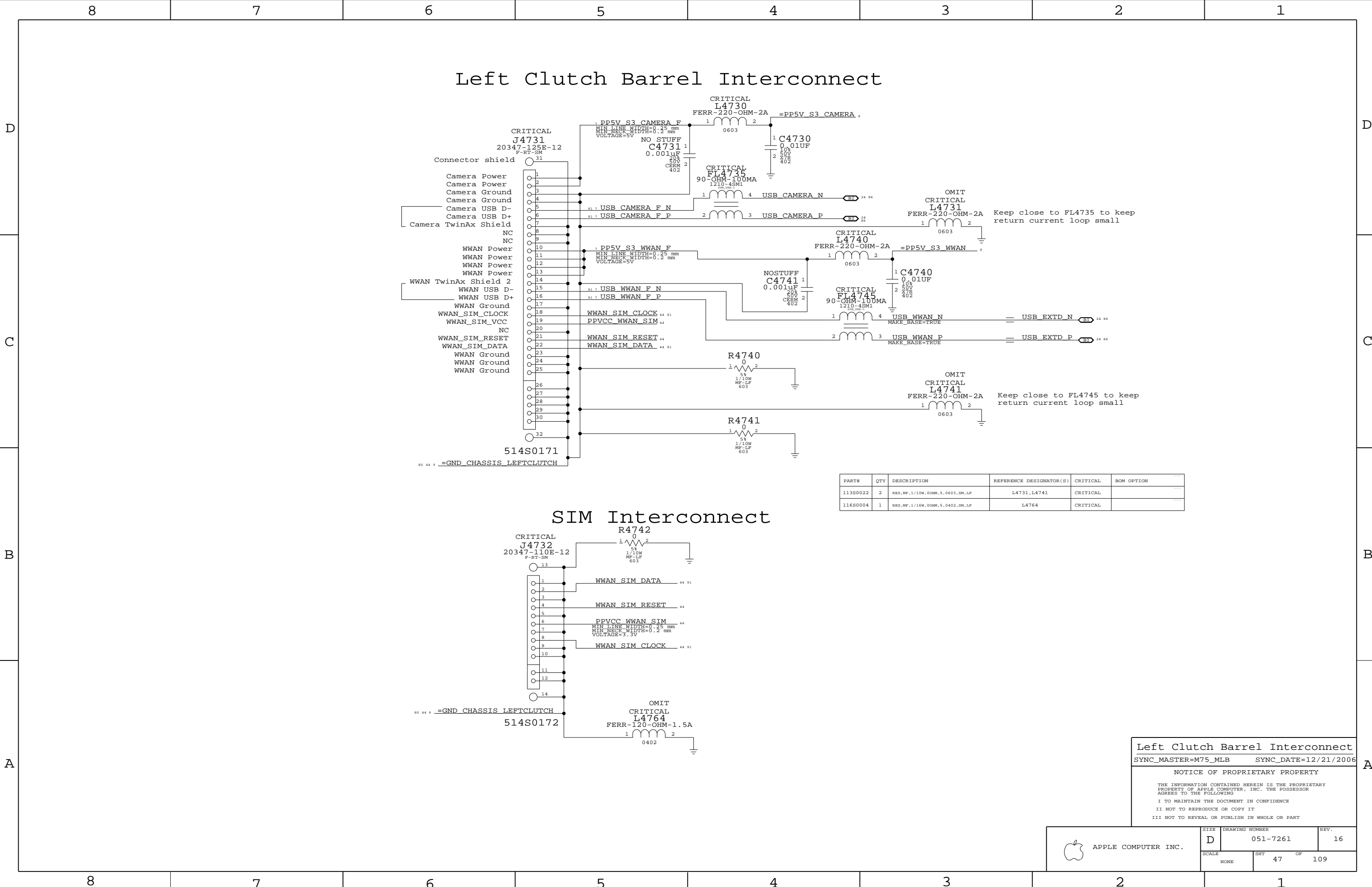
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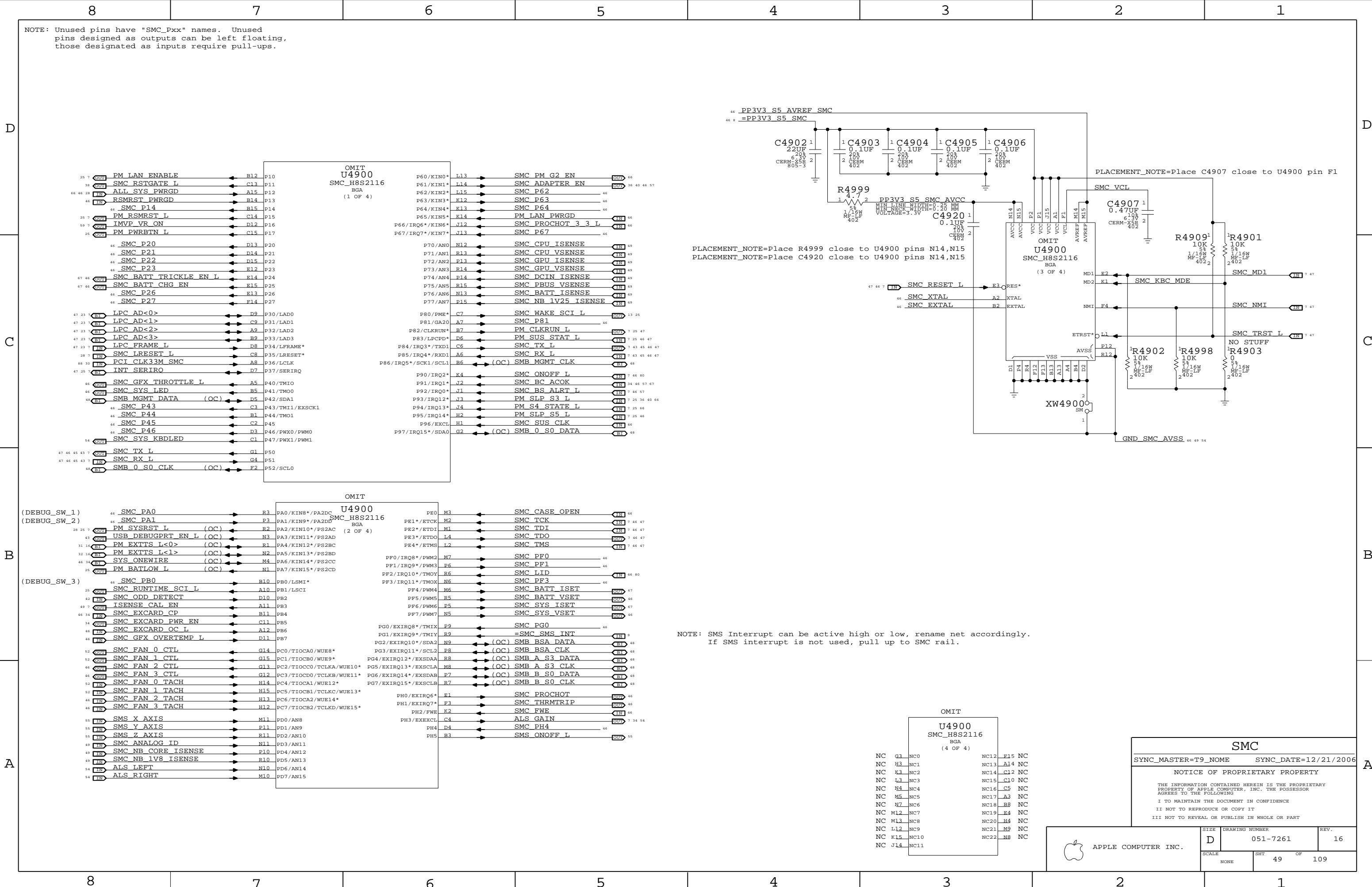
SIZE	DRAWING NUMBER	REV.
D	051-7261	16
SCALE	SHT	OF
NONE	46	109



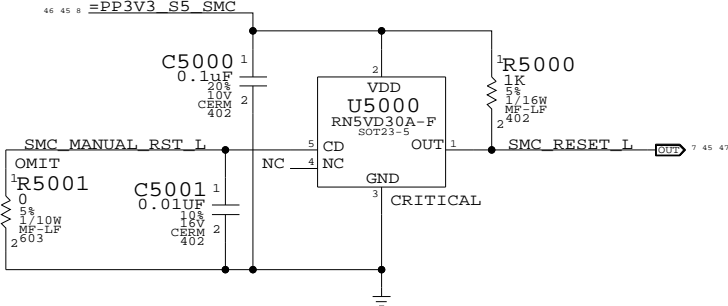
Left Clutch Barrel Interconnect
SYNC_MASTER=M75_MLB SYNC_DATE=12/21/2006

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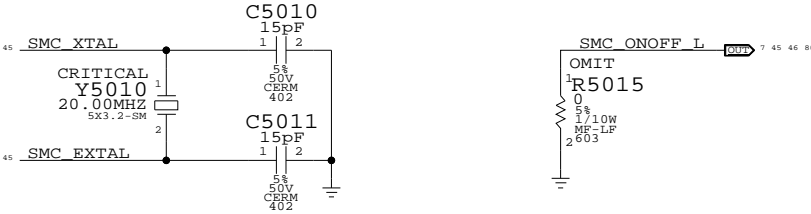
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7261	REV. 16
	SCALE NONE	SHT 47	OF 109



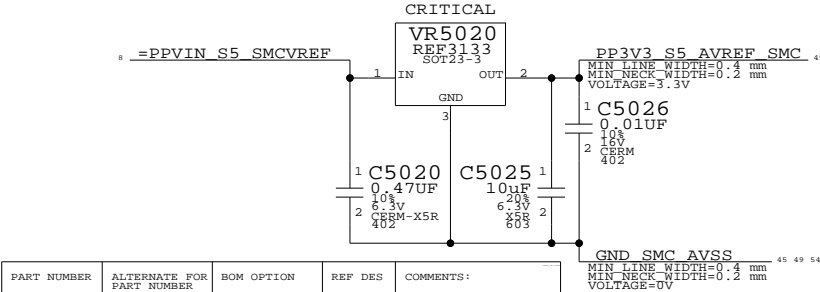
SMC Reset "Button" / Brownout Detect



SMC Crystal Circuit Debug Power "Button"

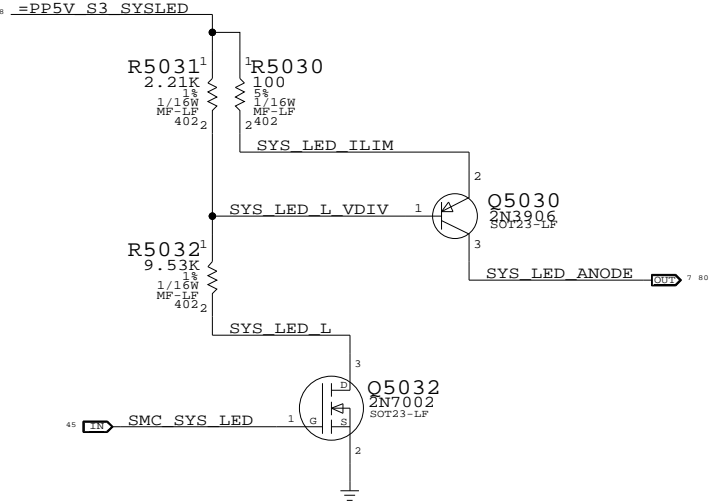


SMC AVREF Supply



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
35381381	35381278		ALL	Intersil ISL60002-33

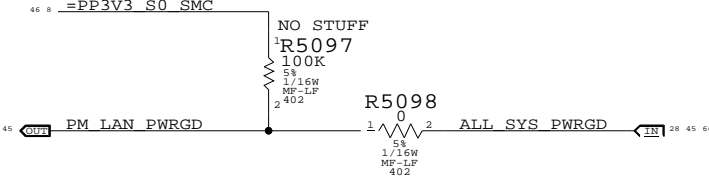
System (Sleep) LED Circuit



SMC_FAN_2_CTL	=	TP_SMC_FAN_2_CTL
SMC_FAN_2_TACH	=	TP_SMC_FAN_2_TACH
SMC_FAN_3_CTL	=	TP_SMC_FAN_3_CTL
SMC_FAN_3_TACH	=	TP_SMC_FAN_3_TACH
SMC_GFX_OVERTEMP_L	=	TP_SMC_GFX_OVERTEMP_L
SMC_GFX_THROTTLE_L	=	TP_SMC_GFX_THROTTLE_L
SMC_BATT_VSET	=	TP_SMC_BATT_VSET
SMC_SYS_VSET	=	TP_SMC_SYS_VSET
SMC_P14	=	TP_SMC_P14
SMC_P20	=	TP_SMC_P20
SMC_P21	=	TP_SMC_P21
SMC_P22	=	TP_SMC_P22
SMC_P23	=	TP_SMC_P23
SMC_P26	=	TP_SMC_P26
SMC_P27	=	TP_SMC_P27
SMC_P43	=	TP_SMC_P43
SMC_P44	=	TP_SMC_P44
SMC_P46	=	TP_SMC_P46
SMC_P62	=	TP_SMC_P62
SMC_P63	=	TP_SMC_P63
SMC_P64	=	TP_SMC_P64
SMC_P81	=	TP_SMC_P81
SMC_FF0	=	TP_SMC_FF0
SMC_FF1	=	TP_SMC_FF1

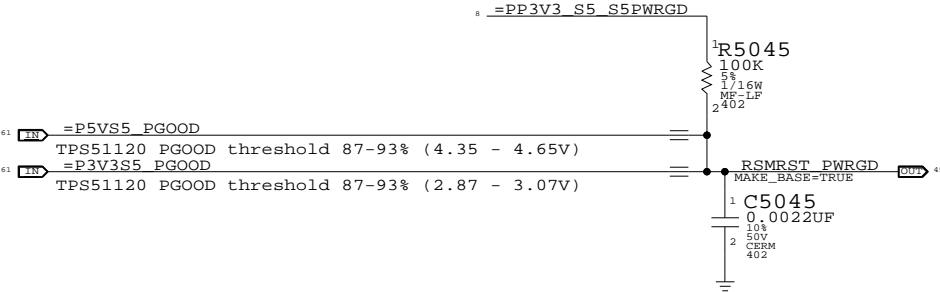
SMC_EXCARD_OC_L	=	EXCARD_OC_L
SMC_SUS_CLK	=	SUS_CLK_SB
SMC_P45	=	SMC_ENRGYSTR_LDO_EN

LAN PWRGD Circuit

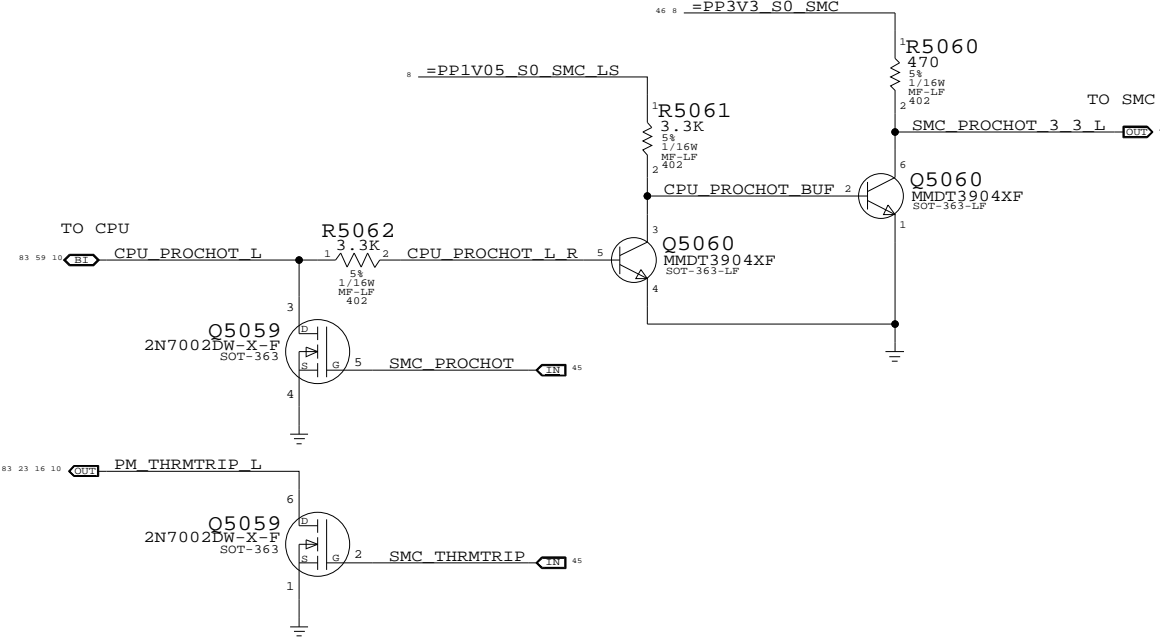


S5 Rail PWRGD Circuit

Reports when 5V S5 and 3.3V S5 are in regulation



SMC FSB to 3.3V Level Shifting



SMC_PA0	=	R5091 100K
SMC_PA1	=	R5092 100K
SMC_PB0	=	R5093 100K
SMC_ONOFF_L	=	R5070 10K
SMC_LID	=	R5071 100K
SMC_FWE	=	R5072 10K
SMC_TX_L	=	R5073 10K
SMC_RX_L	=	R5074 100K
SYS_ONEWIRE	=	R5075 2.0K
SMC_BS_ALRT_L	=	R5076 100K
SMC_TMS	=	R5077 10K
SMC_TDO	=	R5078 10K
SMC_TDI	=	R5079 10K
SMC_TCK	=	R5080 10K
SMC_P67	=	R5094 10K
SMC_FF3	=	R5081 10K
SMC_PG0	=	R5096 10K
SMC_PH4	=	R5082 10K
SMC_BATT_TRICKLE_EN_L	=	R5083 10K
SMC_BATT_CHG_EN	=	R5084 10K
SMC_ADAPTER_EN	=	R5085 10K
SMC_CASE_OPEN	=	R5086 10K
SMC_BC_ACOK	=	R5087 470K
SMC_EXCARD_CP	=	R5088 10K
PM_SUS_STAT_L	=	R5089 100K
PM_SLP_S5_L	=	R5090 100K

SMC Support

SYNC_MASTER=M75_MLB SYNC_DATE=04/02/2007

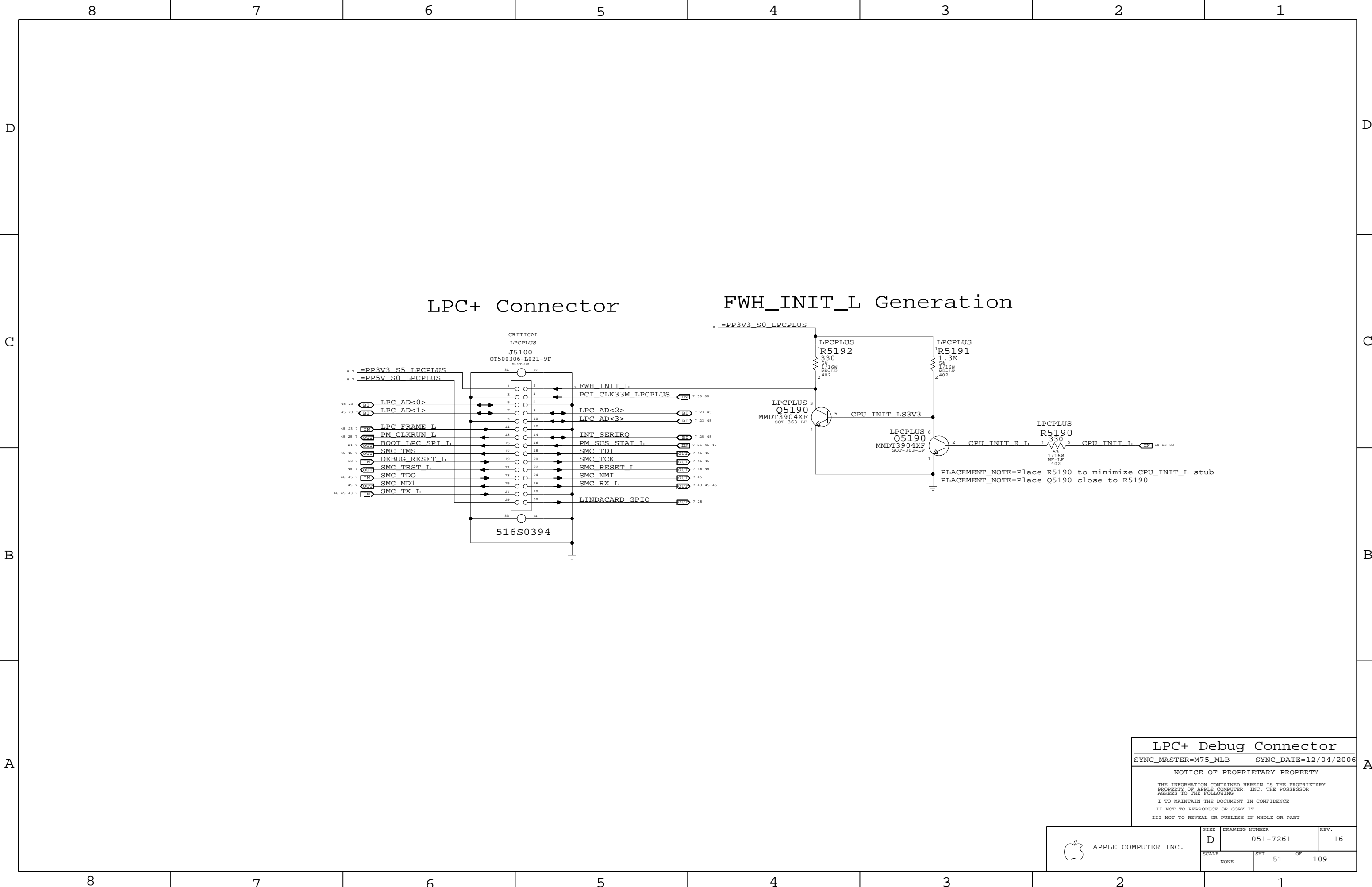
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SIZE	DRAWING NUMBER	REV.
D	051-7261	16
SCALE	SHT	OF
NONE	50	109



LPC+ Debug Connector

SYNC_MASTER=M75_MLB

SYNC_DATE=12/04/2006

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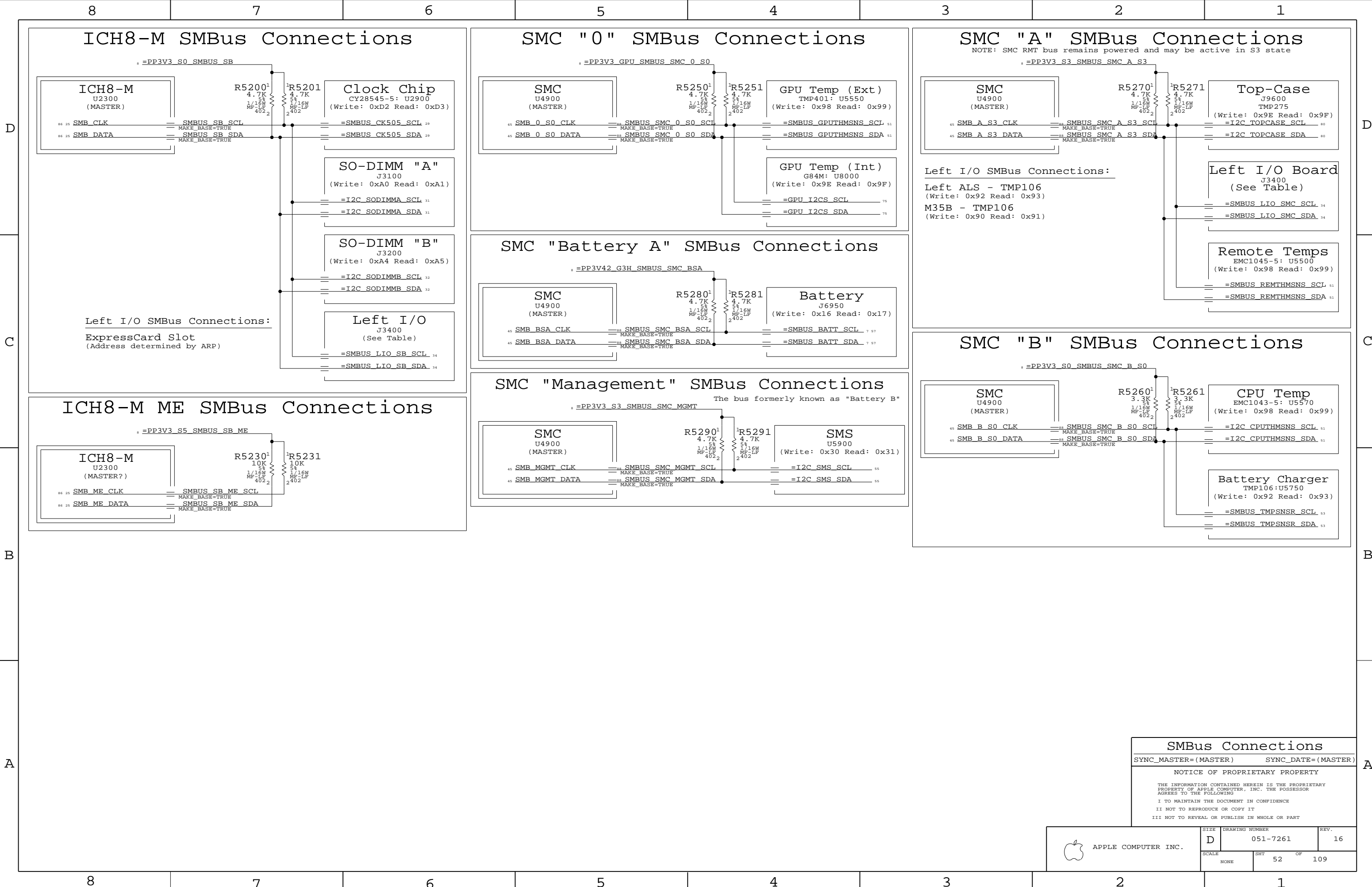
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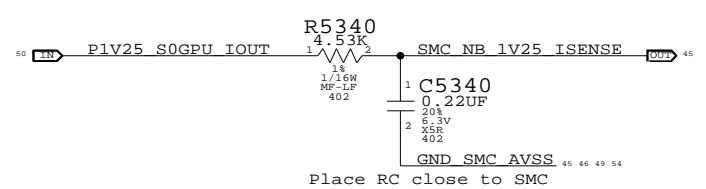
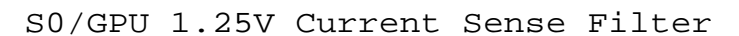
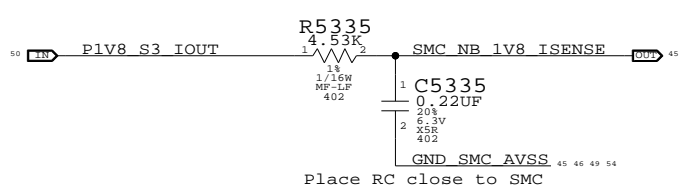
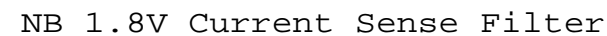
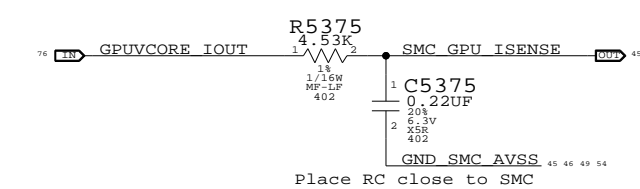
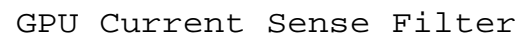
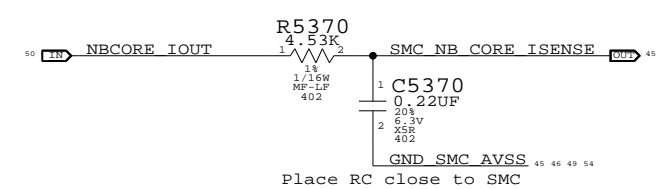
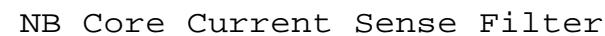
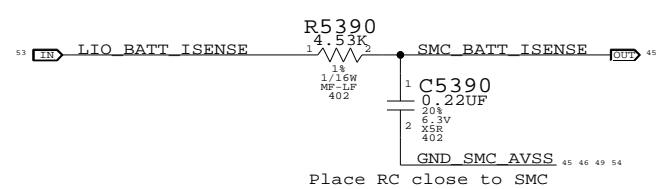
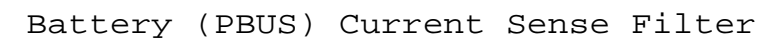
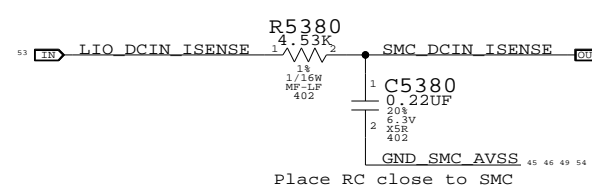
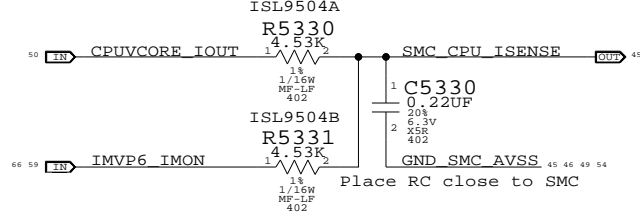
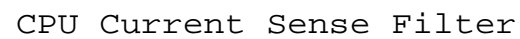
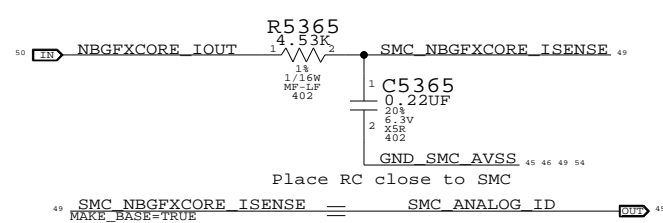
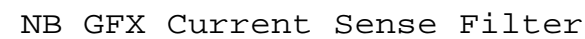
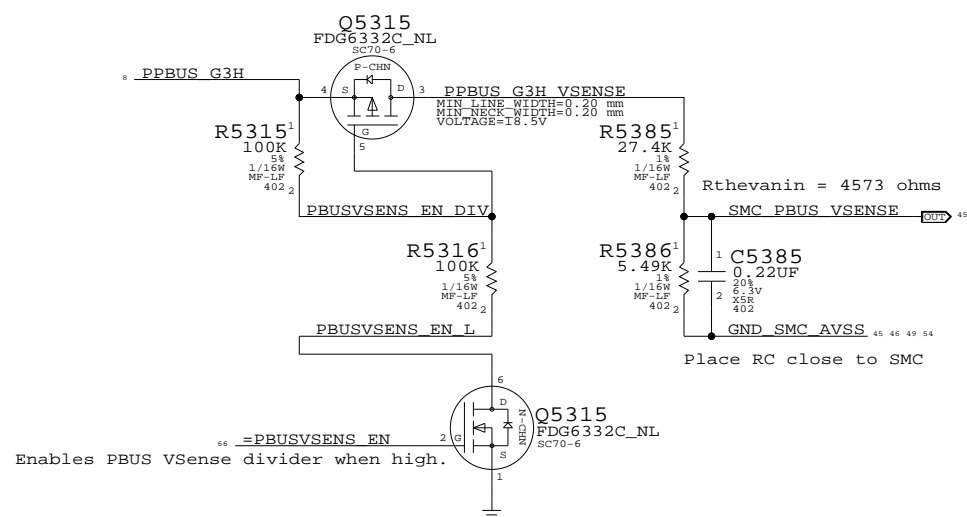
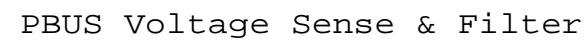
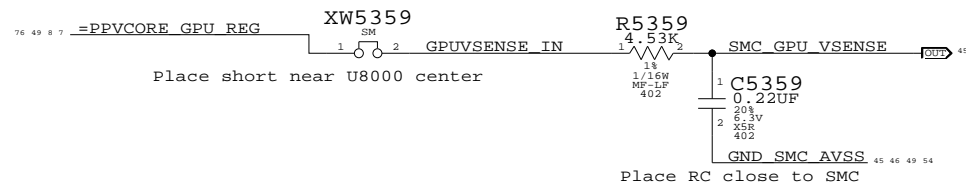
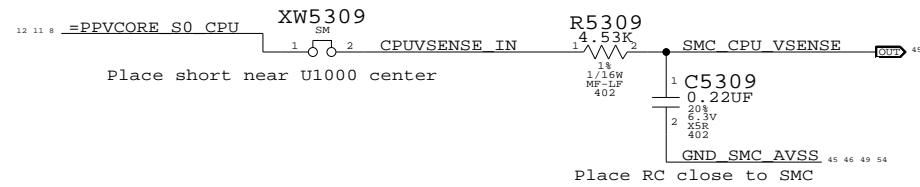
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	D	051-7261	16
SCALE		SHT	OF
NONE		51	109



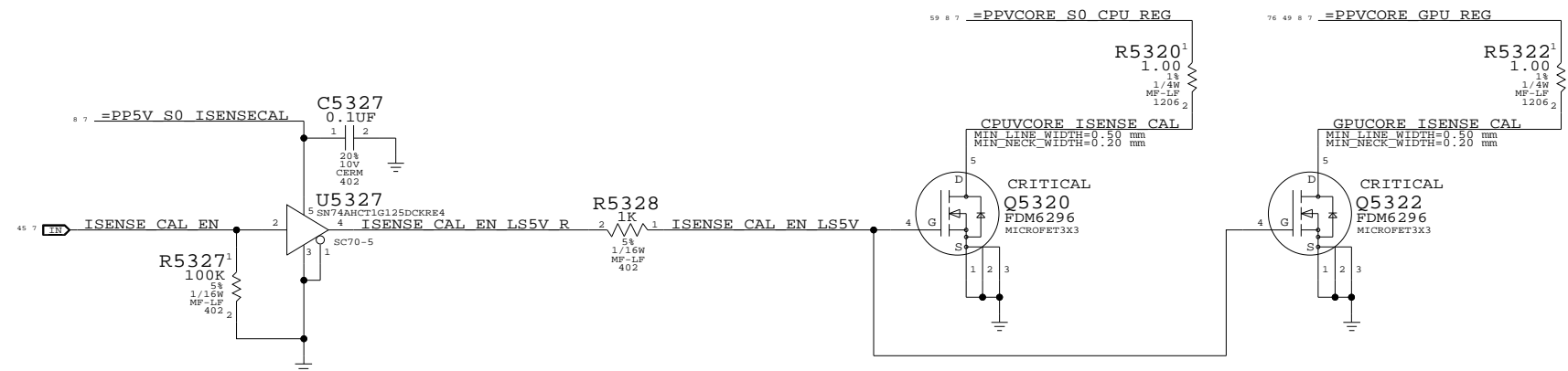
SMBus Connections		
SYNC_MASTER=(MASTER)		SYNC_DATE=(MASTER)
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	SCALE NONE	SHT 52 OF 109	



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



Current & Voltage Sensing
SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007


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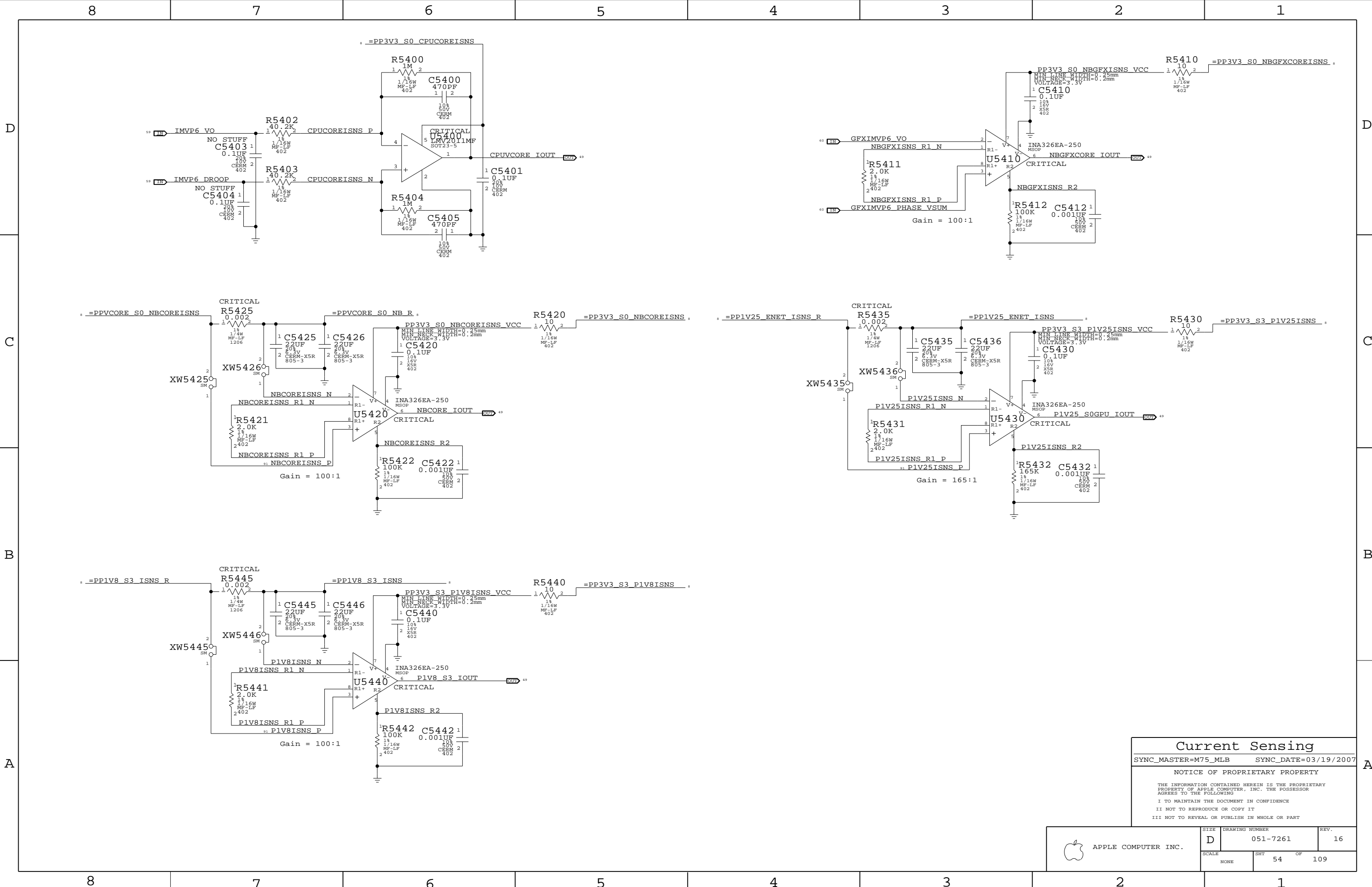
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	D	051-7261	16
	SCALE	SHT OF	
	NONE	53 109	



Current Sensing

SYNC_MASTER=M75_MLB

SYNC_DATE=03/19/2007

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	D	051-7261	16
SCALE		SHT	OF
NONE		54	109

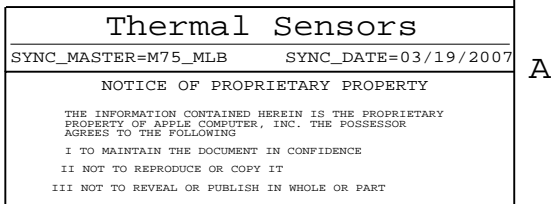
8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

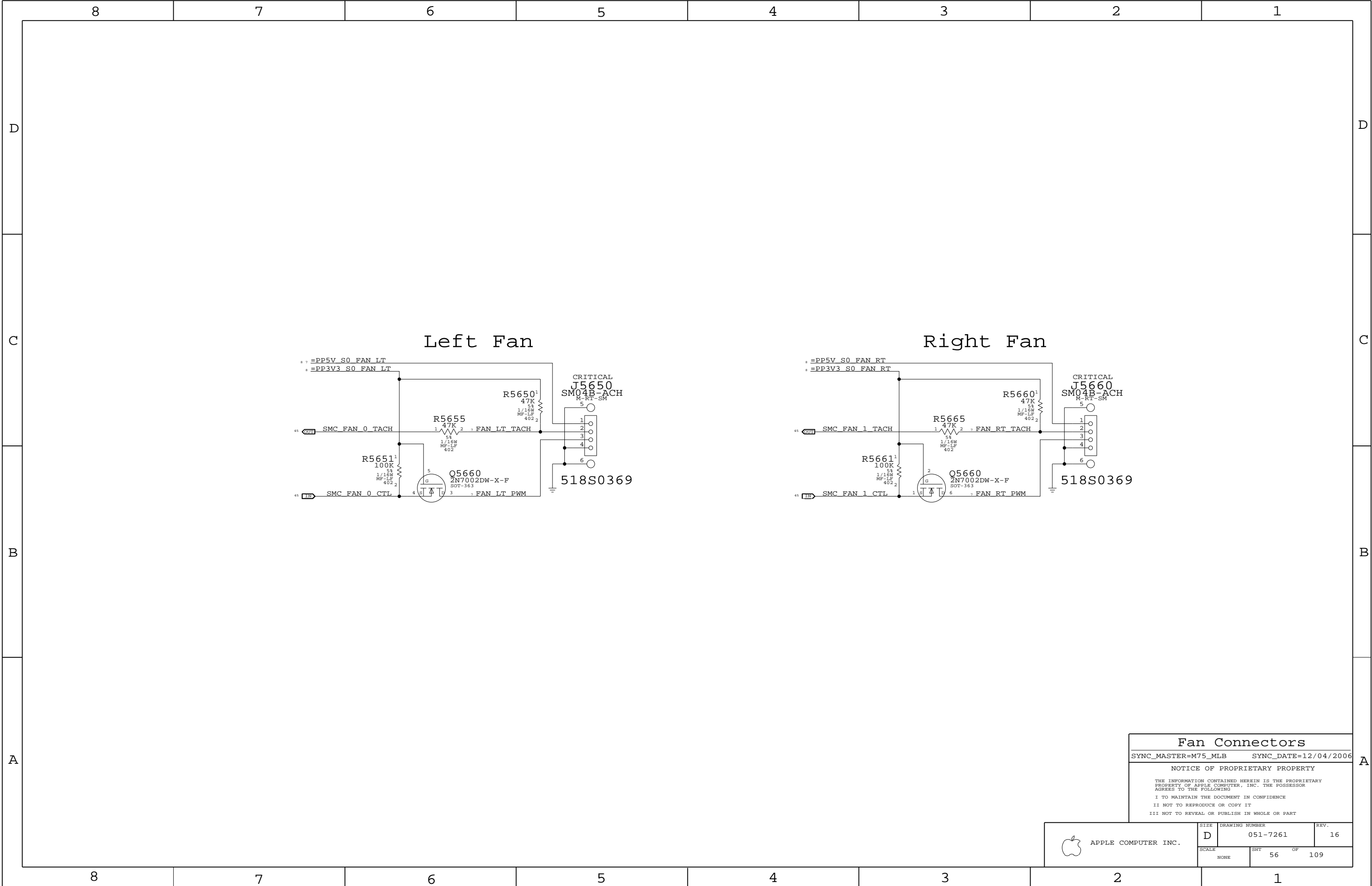


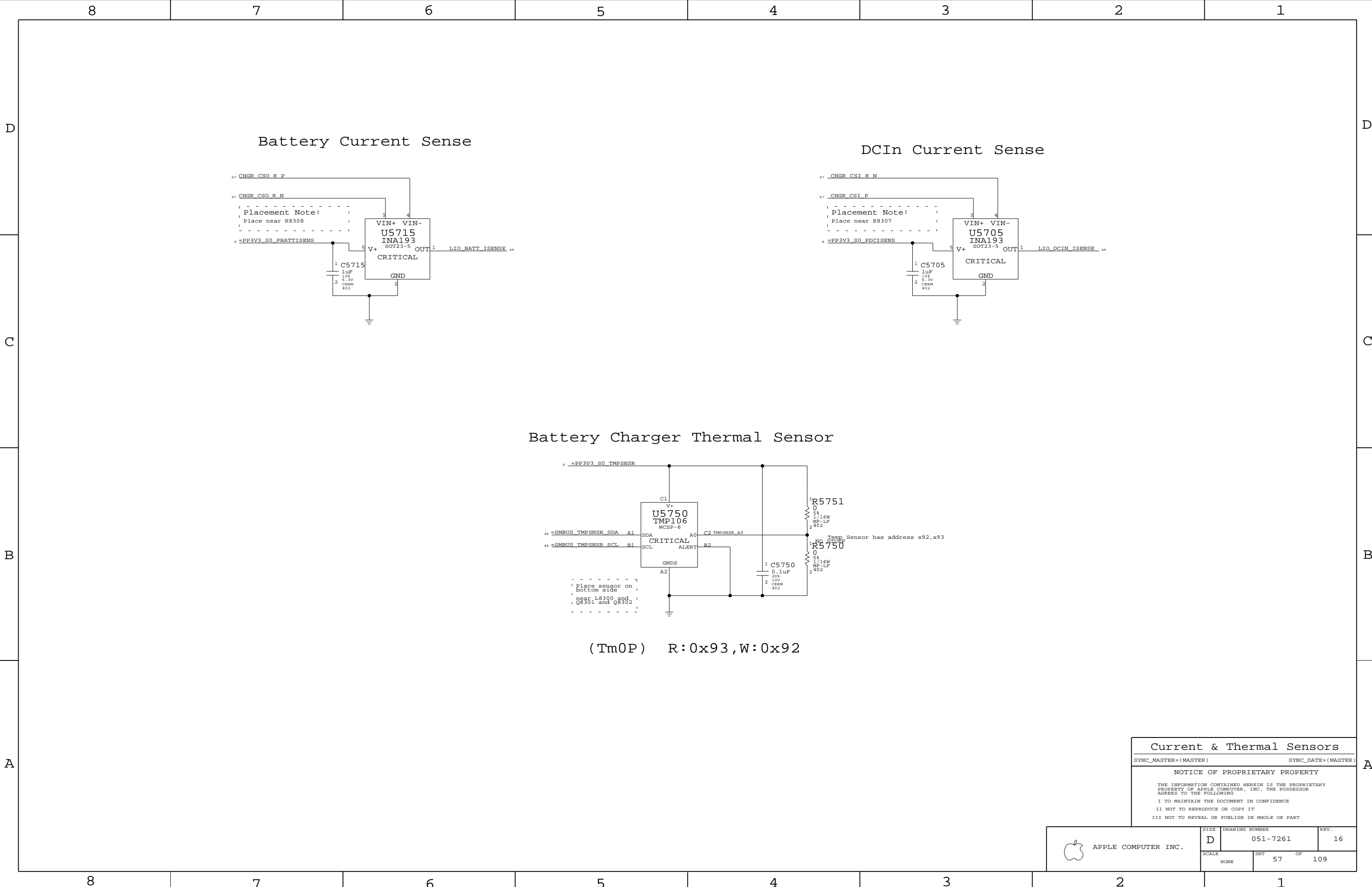
C



A







Current & Thermal Sensors

SYNC_MASTER=(MASTER)

SYNC_DATE=(MASTER)

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	SCALE NONE	SHT 57	OF 109

D



D



B



B

A

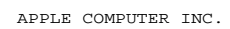
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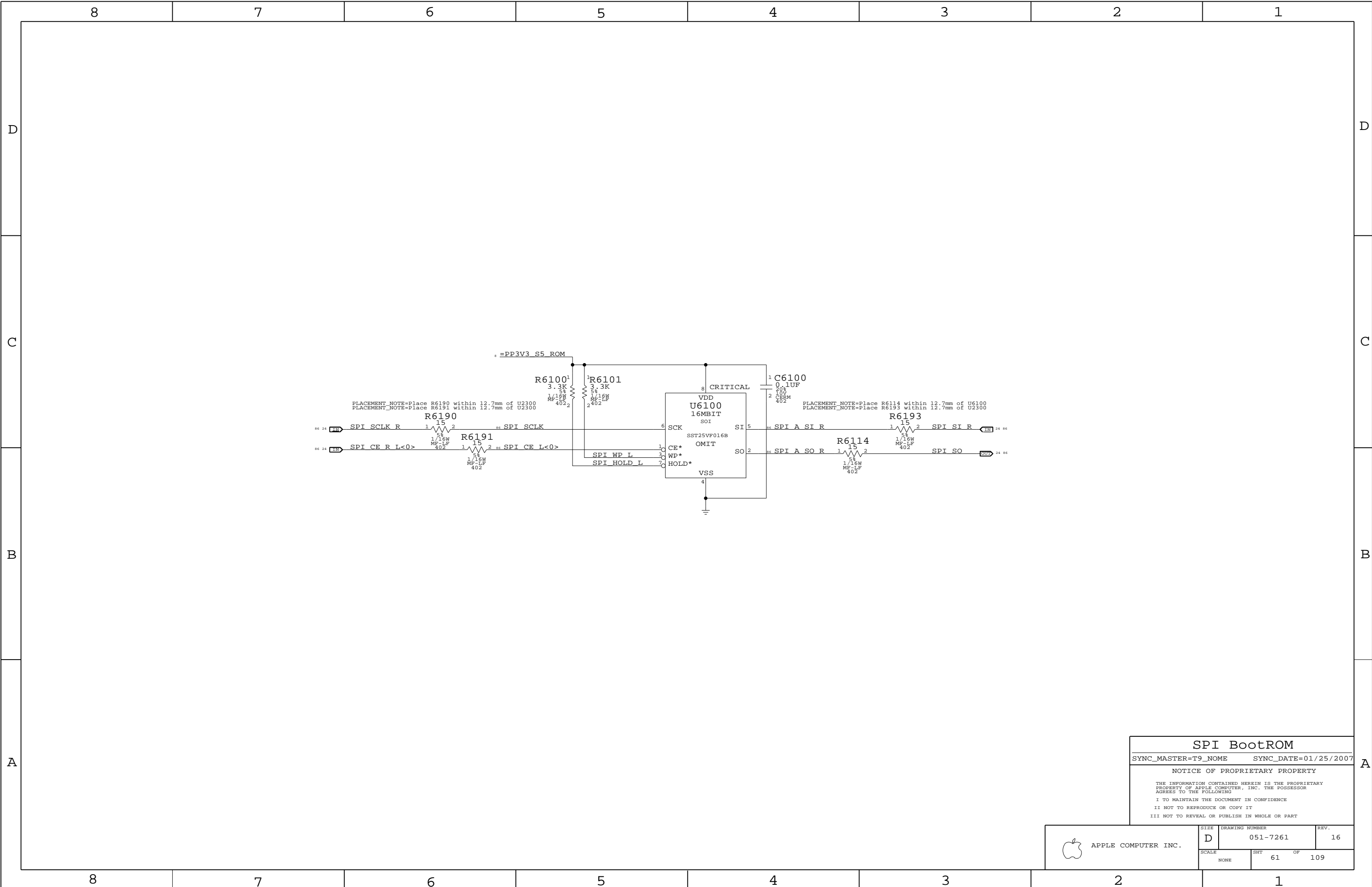
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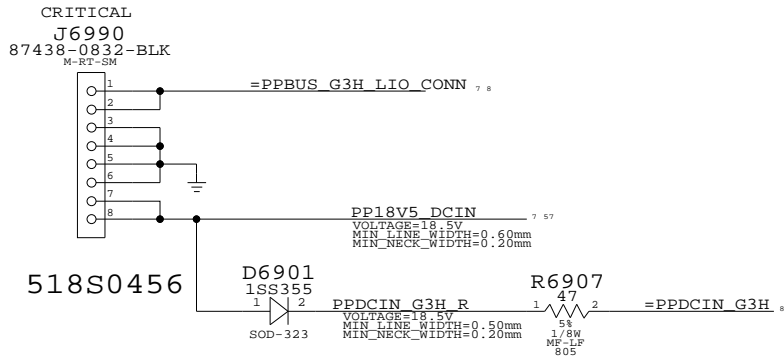
8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---



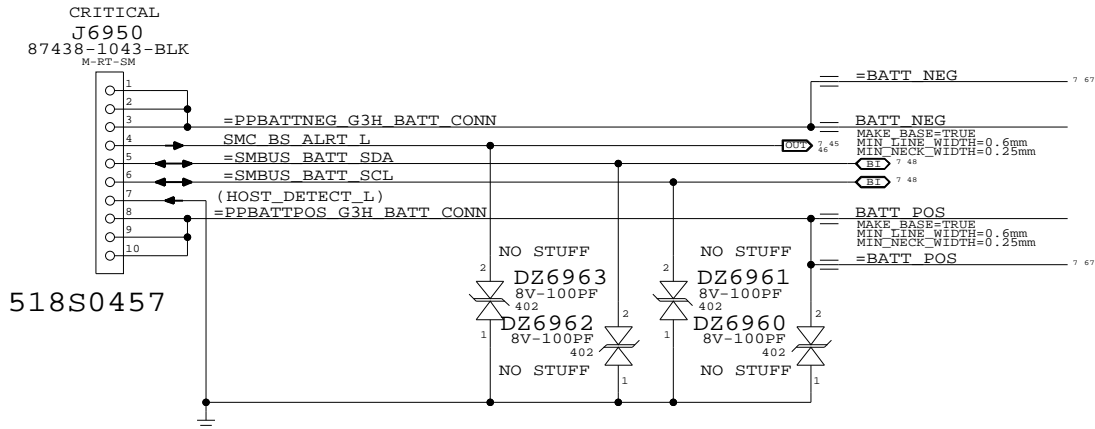
SPI BootROM	
SYNC_MASTER=T9_NOME	SYNC_DATE=01/25/2007
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 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7261	REV. 16
	SCALE NONE	SHT 61	OF 109

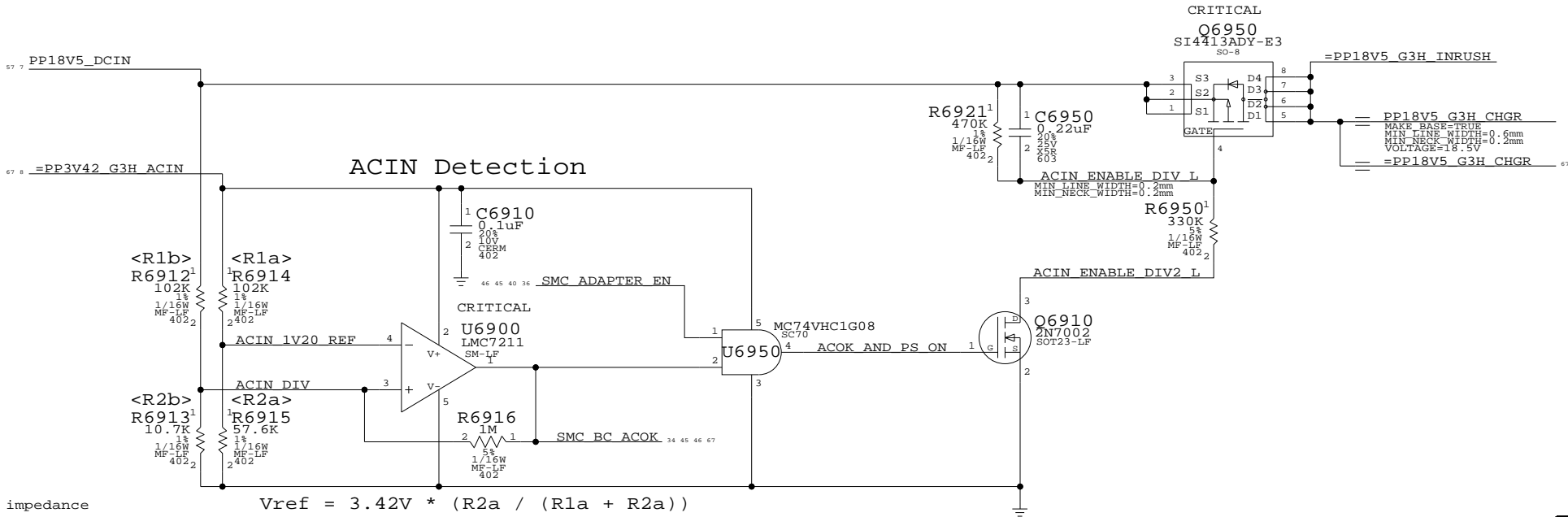
DC-In Connector



Battery Connector



Inrush Limiter



NOTE: R6910 is on LIO.

System must provide 10K-70K impedance to A52 adapter for system load detection.

REQ of R6910 (on LIO), R6912, & R6913 is 36.9K.

$$V_{ref} = 3.42V * (R2a / (R1a + R2a))$$
$$V_{th} = (V_{ref} / (R2b / (R1b + R2b)))$$

$$V_{ref} = 1.23V$$

$$V_{th} = 13.0V$$

Assuming 1% variance for R6910-R6915 and 3.42V:
Worst case Vth: min:12.47V, max: 13.54V

DC-In & Battery Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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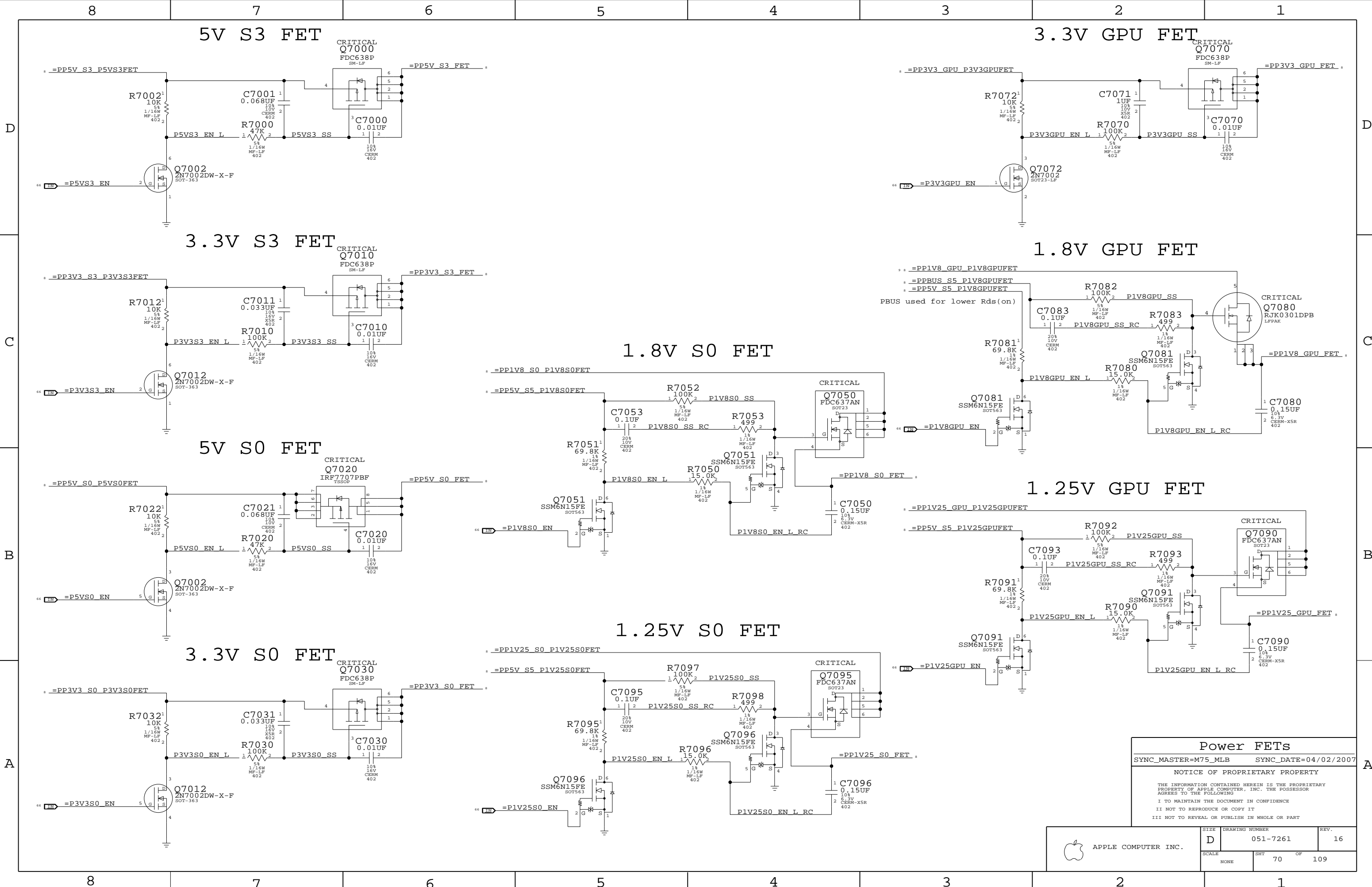
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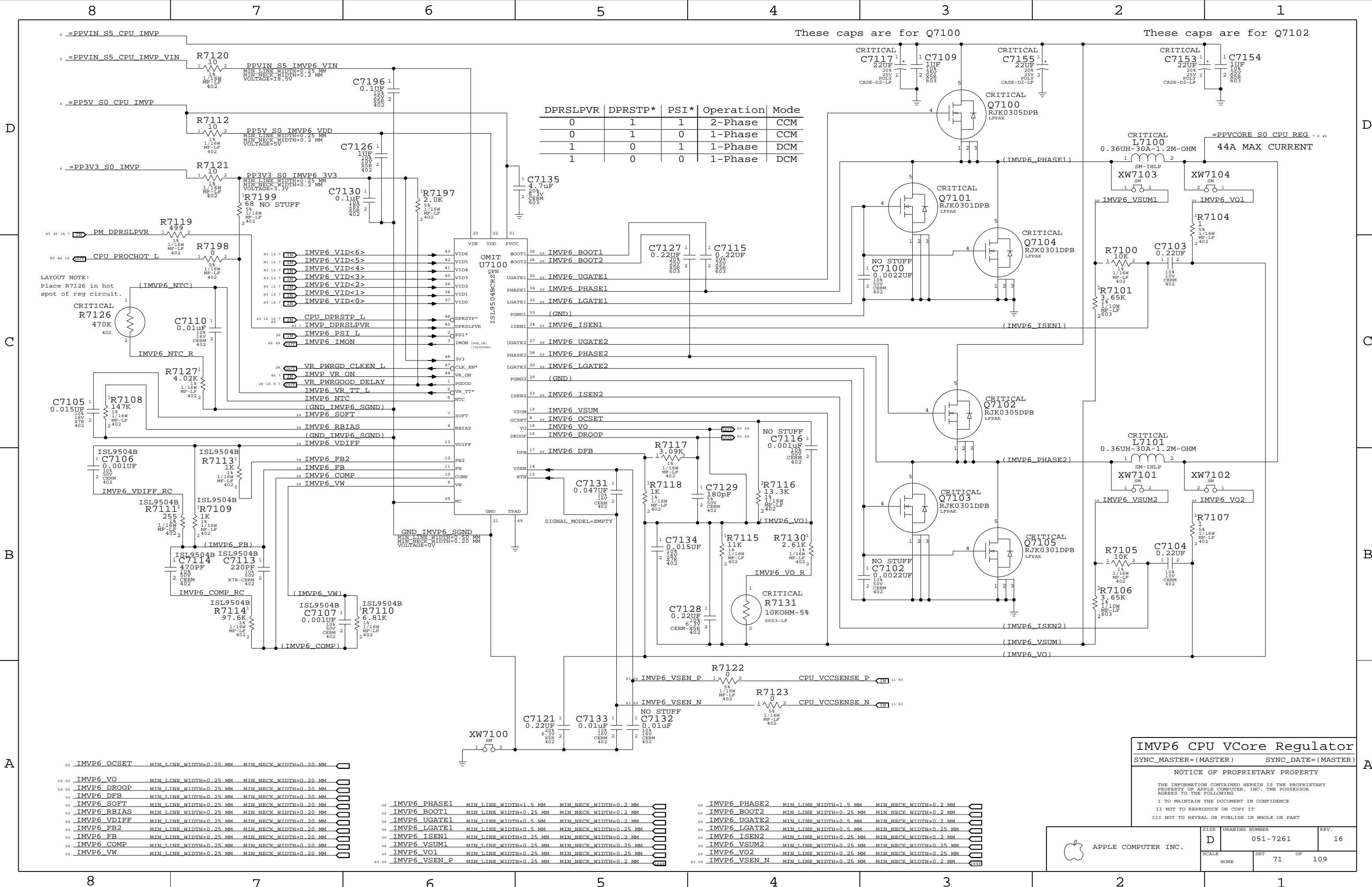
SIZE D DRAWING NUMBER 051-7261 REV. 16

SCALE NONE SHT 69 OF 109



Power FETs		
SYNC_MASTER=M75_MLB		SYNC_DATE=04/02/2007
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	16
SCALE		SHT	OF
NONE		70	109



IMVP6 CPU VCore Regulator

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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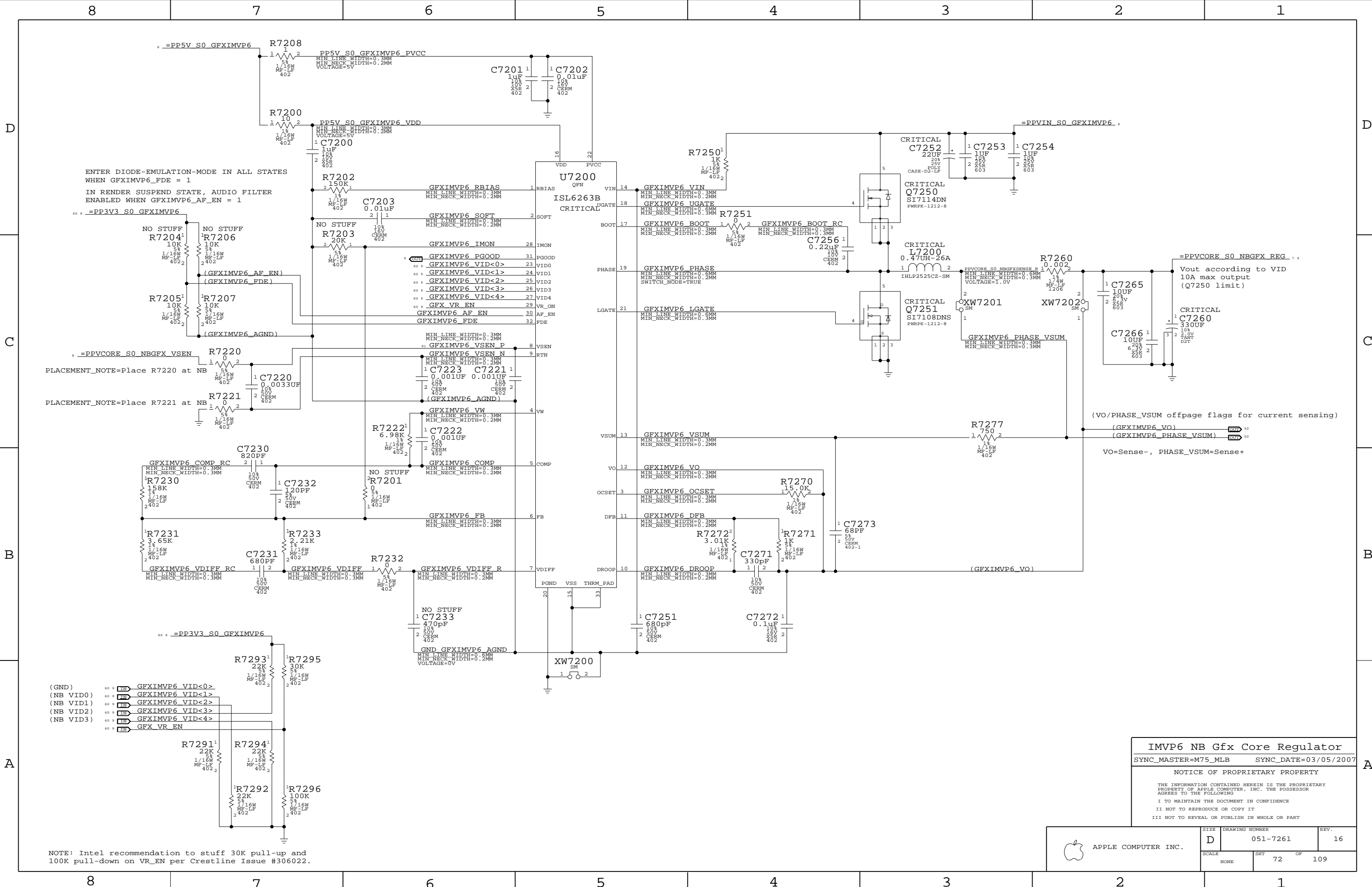
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APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-7261 REV. 16

SCALE NONE SHT 71 OF 109



8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

ENTER DIODE-EMULATION-MODE IN ALL STATES
WHEN GFXIMVP6_FDE = 1
IN RENDER SUSPEND STATE, AUDIO FILTER
ENABLED WHEN GFXIMVP6_AF_EN = 1

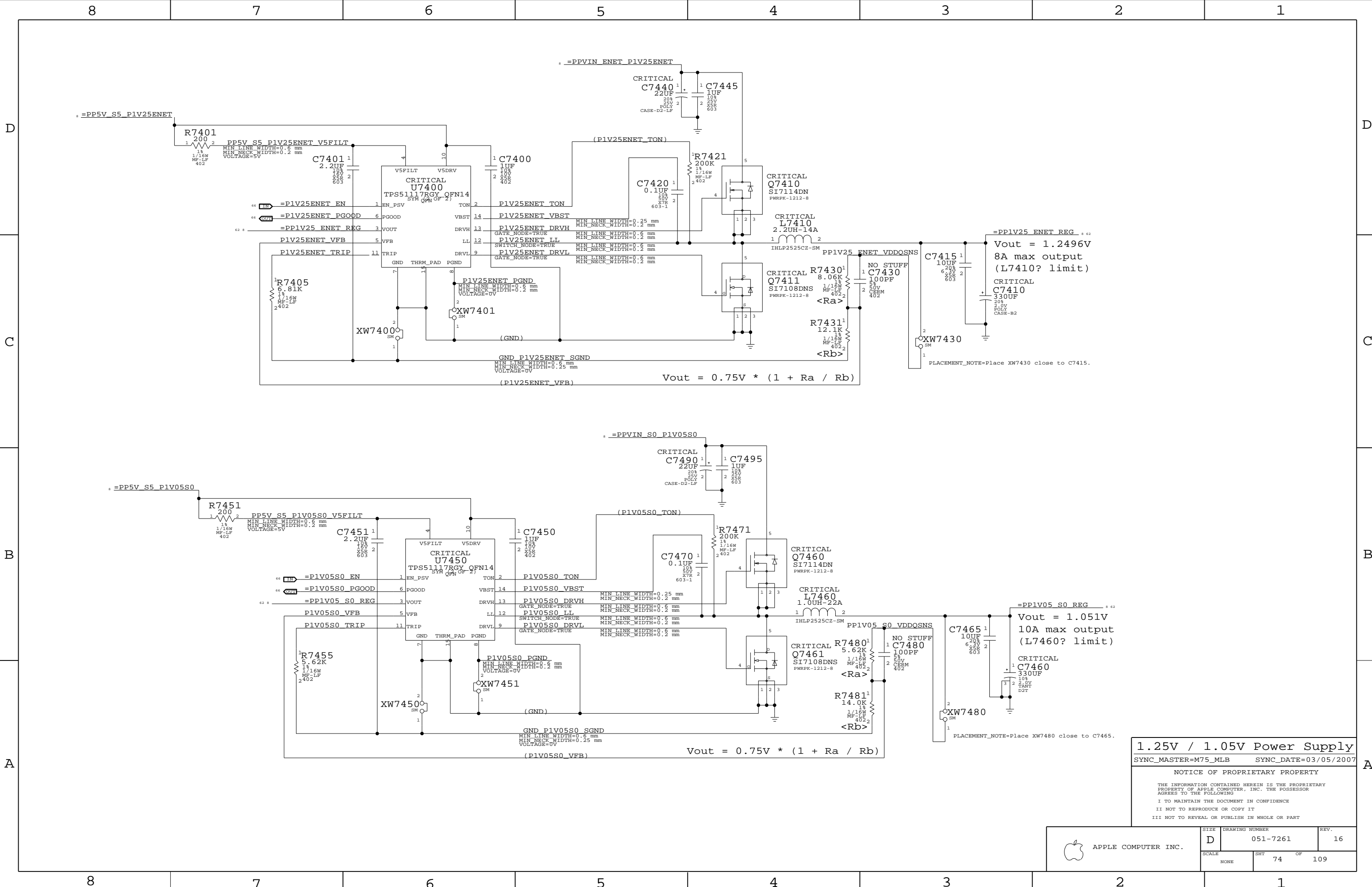
PLACEMENT_NOTE=Place R7220 at NB
PLACEMENT_NOTE=Place R7221 at NB

(GND)
(NB VID0)
(NB VID1)
(NB VID2)
(NB VID3)
(NB VID4)
(NB VR_EN)

NOTE: Intel recommendation to stuff 30K pull-up and
100K pull-down on VR_EN per Crestline Issue #306022.

IMVP6 NB Gfx Core Regulator
SYNC_MASTER=M75_MLB SYNC_DATE=03/05/2007
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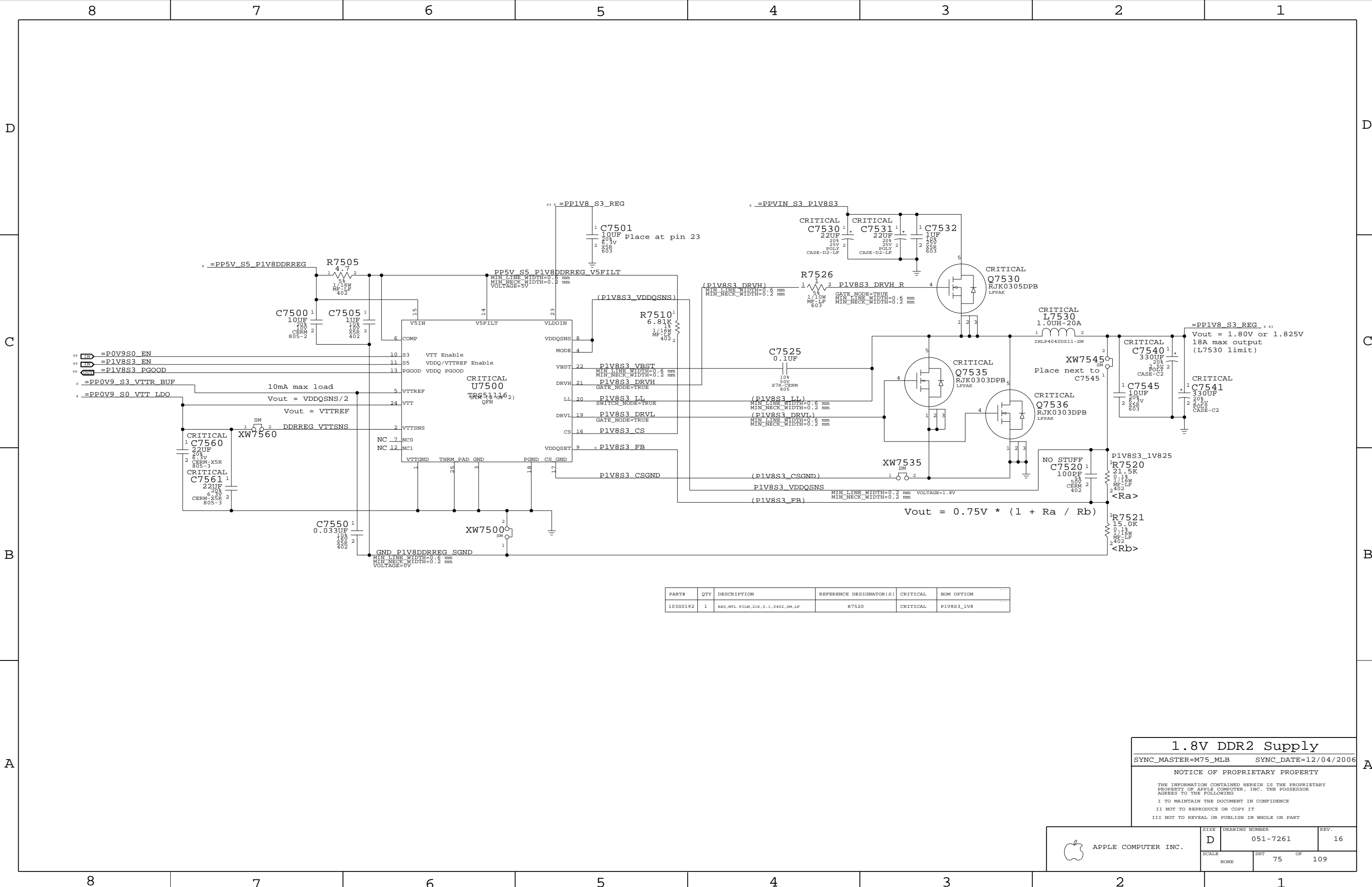
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	16
	SCALE	SHT	OF
	NONE	72	109



1.25V / 1.05V Power Supply
SYNC_MASTER=M75_MLB SYNC_DATE=03/05/2007

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7261	REV. 16
	SCALE NONE	SHT 74	OF 109



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
10380192	1	REG,MTL FILM,21K,0.1,0402,SM,LF	R7520	CRITICAL	Plv8S3_1V8

1.8V DDR2 Supply

SYNC_MASTER=M75_MLB

SYNC_DATE=12/04/2006

NOTICE OF PROPRIETARY PROPERTY

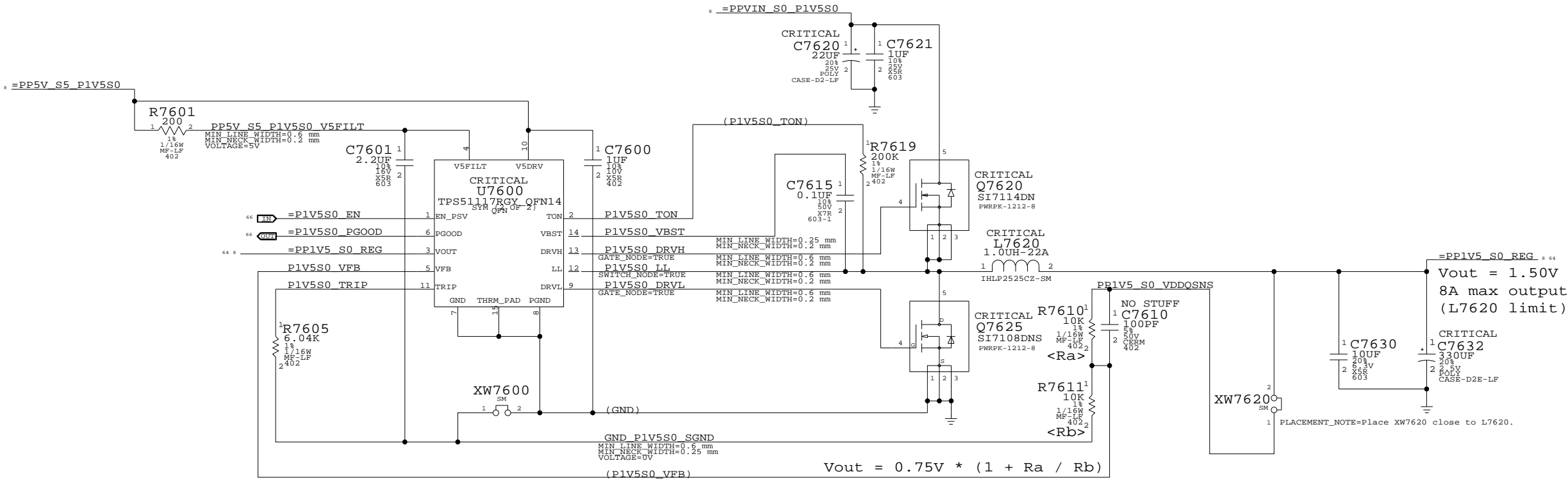
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	D	051-7261	16
SCALE		SHT	OF
NONE		75	109



1.5V Power Supply

SYNC_MASTER=M75_MLB SYNC_DATE=03/05/2007

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	16
SCALE		SHT	OF
NONE		76	109

D

C

B

A

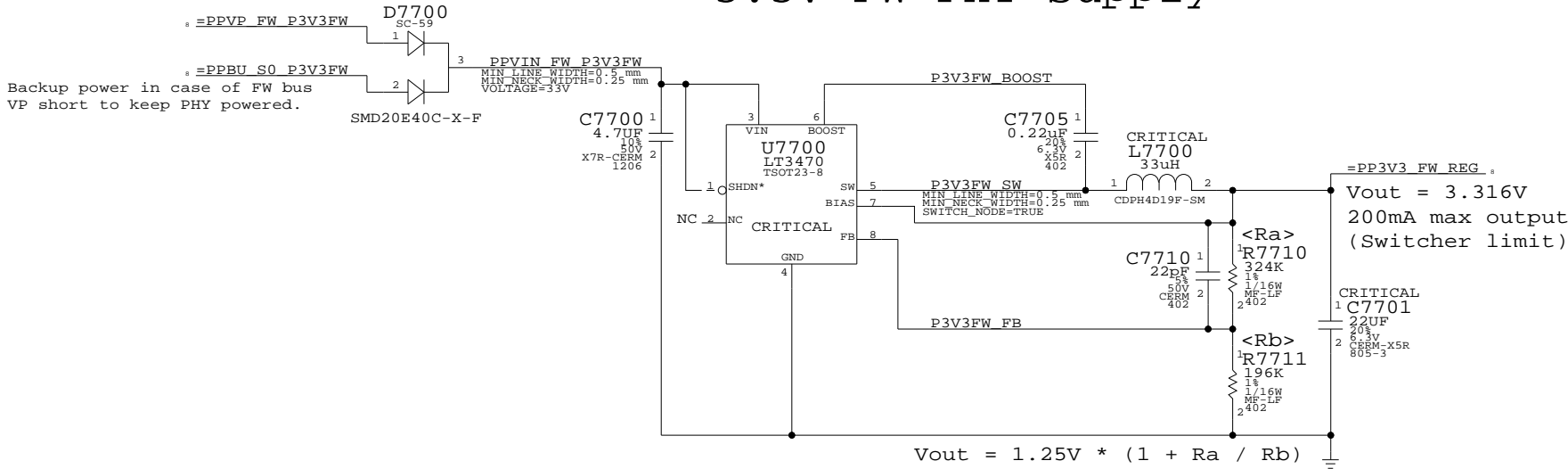
D

C

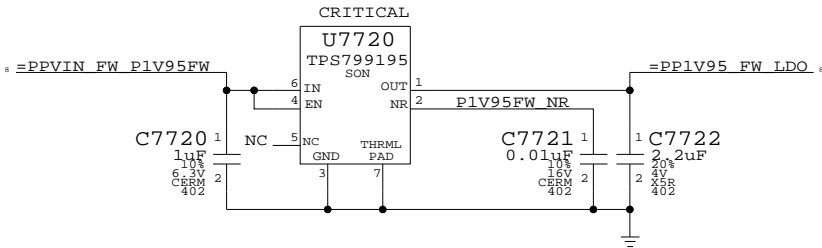
B

A

3.3V FW PHY Supply



1.95V FW PHY Supply



FW PHY Power Supplies

SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006

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APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-7261

REV.

16

SCALE

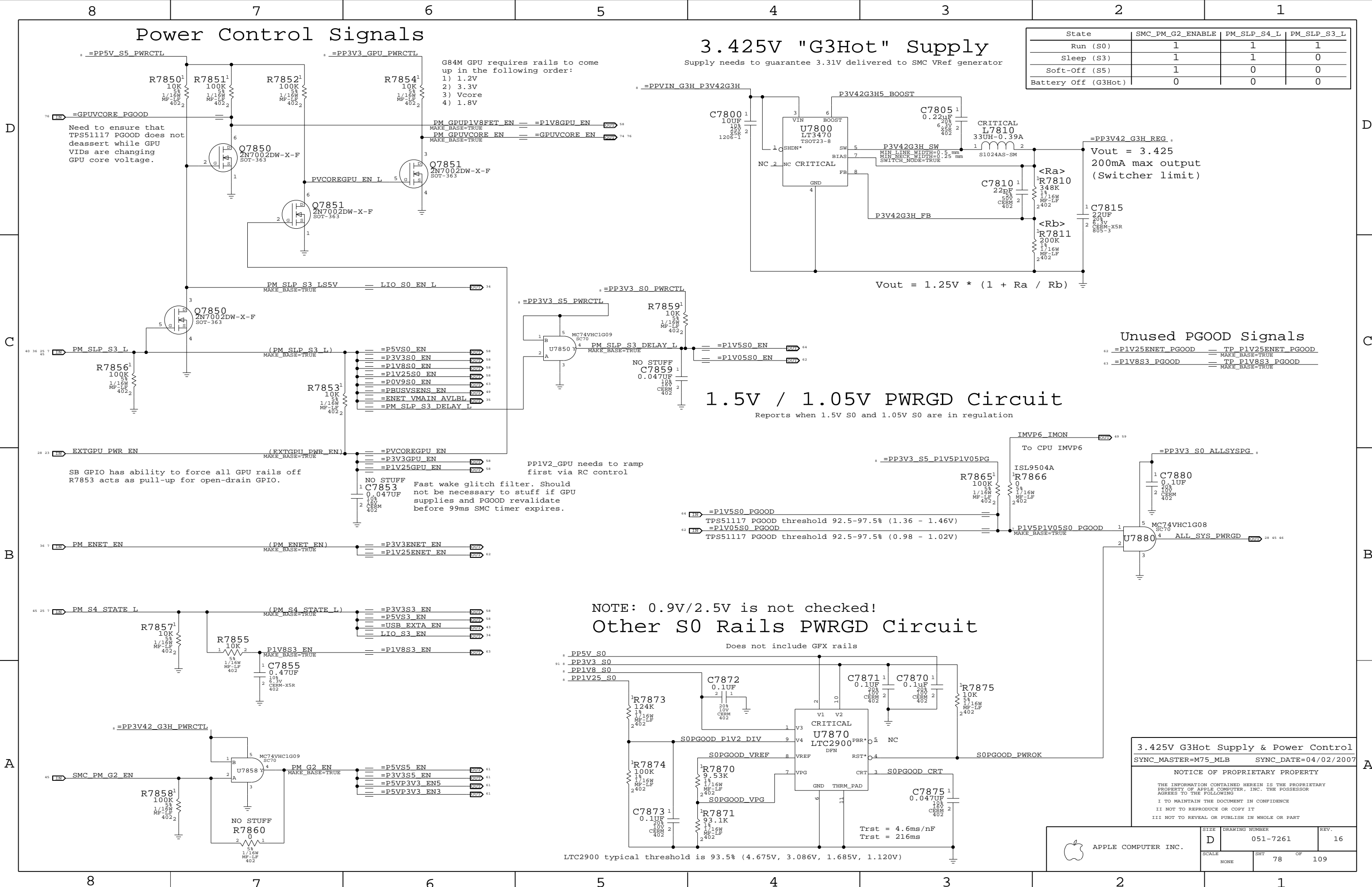
NONE

SHT

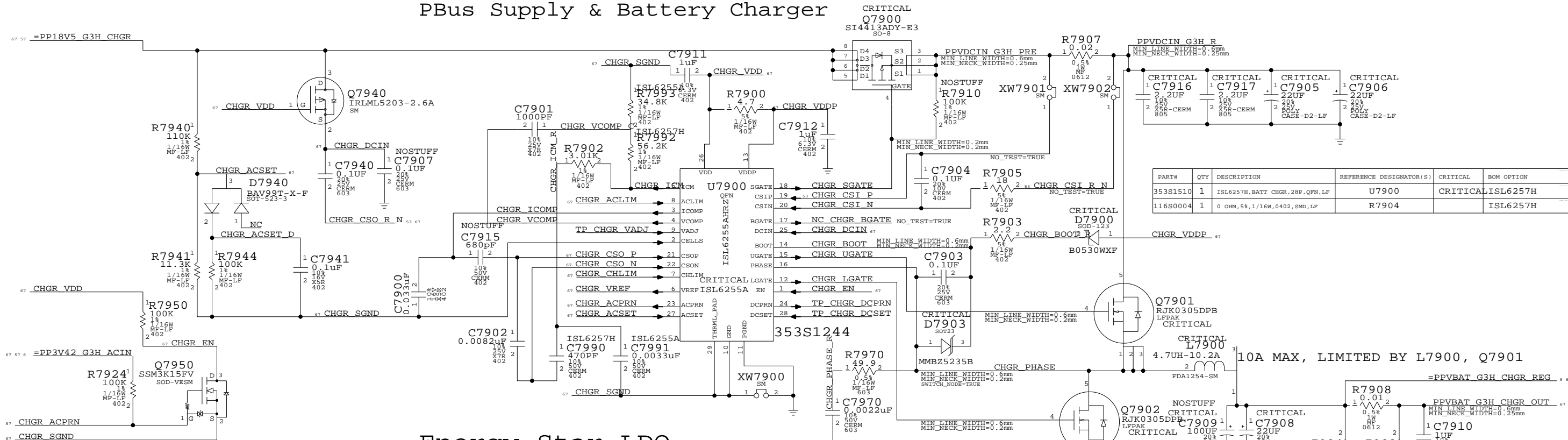
77

OF

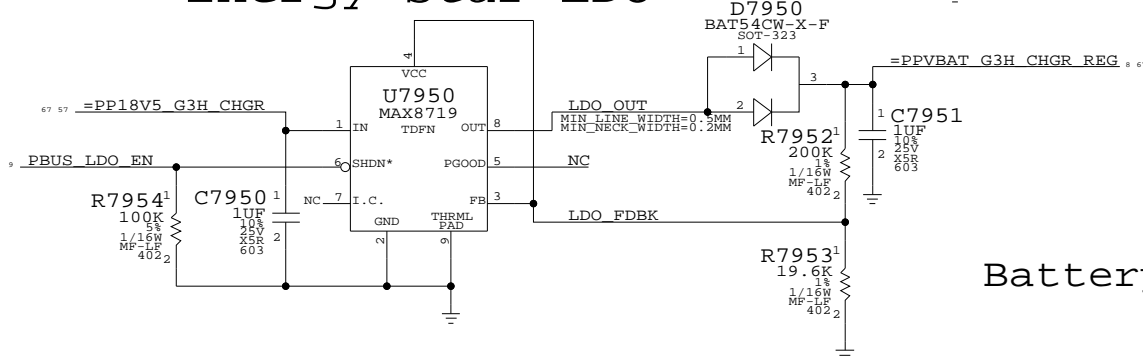
109



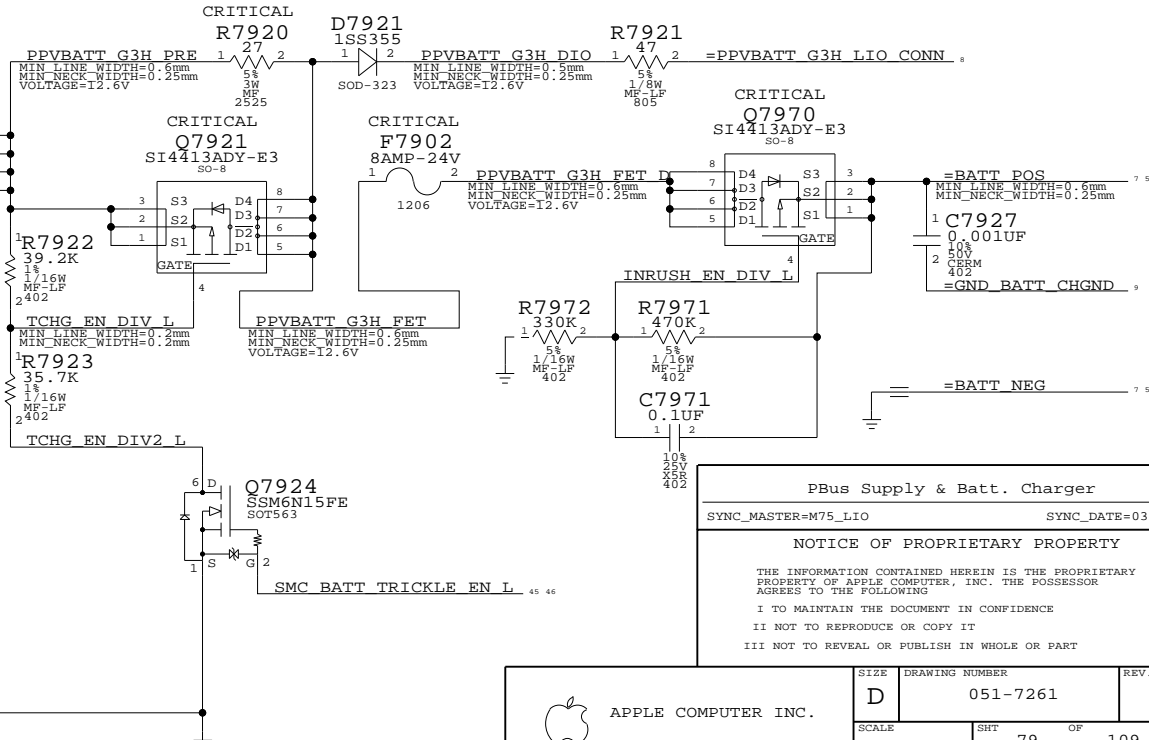
PBus Supply & Battery Charger



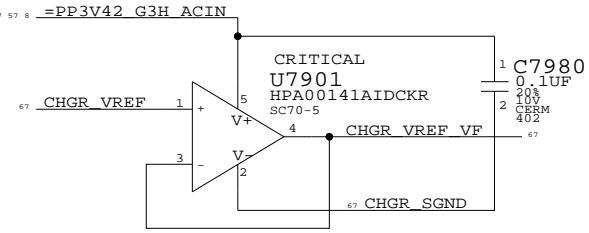
Energy Star LDO



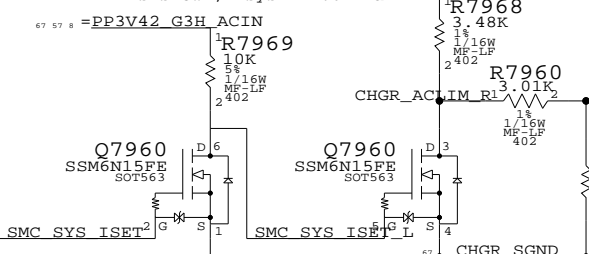
Battery Charge FETs



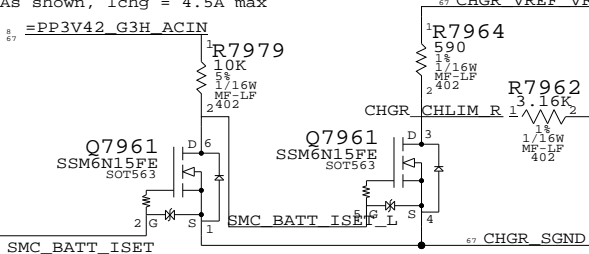
VOLTAGE FOLLOWER GUARANTEES CURRENT LIMIT CIRCUITS ARE PROVIDED WITH SUFFICIENT CURRENT WITHOUT SINKING CURRENT FROM VREF.



Adapter Input Current Limit
As shown, Isys ~4.6A max



Battery Charge Current Limit
As shown, Ichg = 4.5A max



PBus Supply & Batt. Charger
SYNC_MASTER=M75_LIO SYNC_DATE=03/08/2007
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Page Notes

Power aliases required by this page:

- =PPIV2_GPU_PEX_PLLXVDD
- =PPIV2_GPU_PEX_IOVDDQ
- =PPIV2_GPU_PEX_IOVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

=PPIV2_GPU_PEX_PLLXVDD
=PPIV2_GPU_PEX_IOVDDQ
=PPIV2_GPU_PEX_IOVDD

PEX 1.2V Current = 2A

250mA

1500mA

180mA

20mA

PPIV2 GPU PEX PLLAVDD F

MIN LINE WIDTH=0.25 mm
MIN NECK WIDTH=0.25 mm
VOLTAGE=1.2V

PPIV2 GPU PEX PLLVDD F

MIN LINE WIDTH=0.25 mm
MIN NECK WIDTH=0.25 mm
VOLTAGE=1.2V



OMIT

U8000
NB8P-GS-W-A2
BGA
(1 OF 8)

PCI-EXPRESS BUS INTERFACE

PEX_TSTCLK_OUT
PEX_TSTCLK_OUT_L
TP GPU PEXTSTCLK_P
TP GPU PEXTSTCLK_N

NV G84M PCI-E

SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

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APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-7261

REV.

16

SCALE

NONE

SHT

80

OF

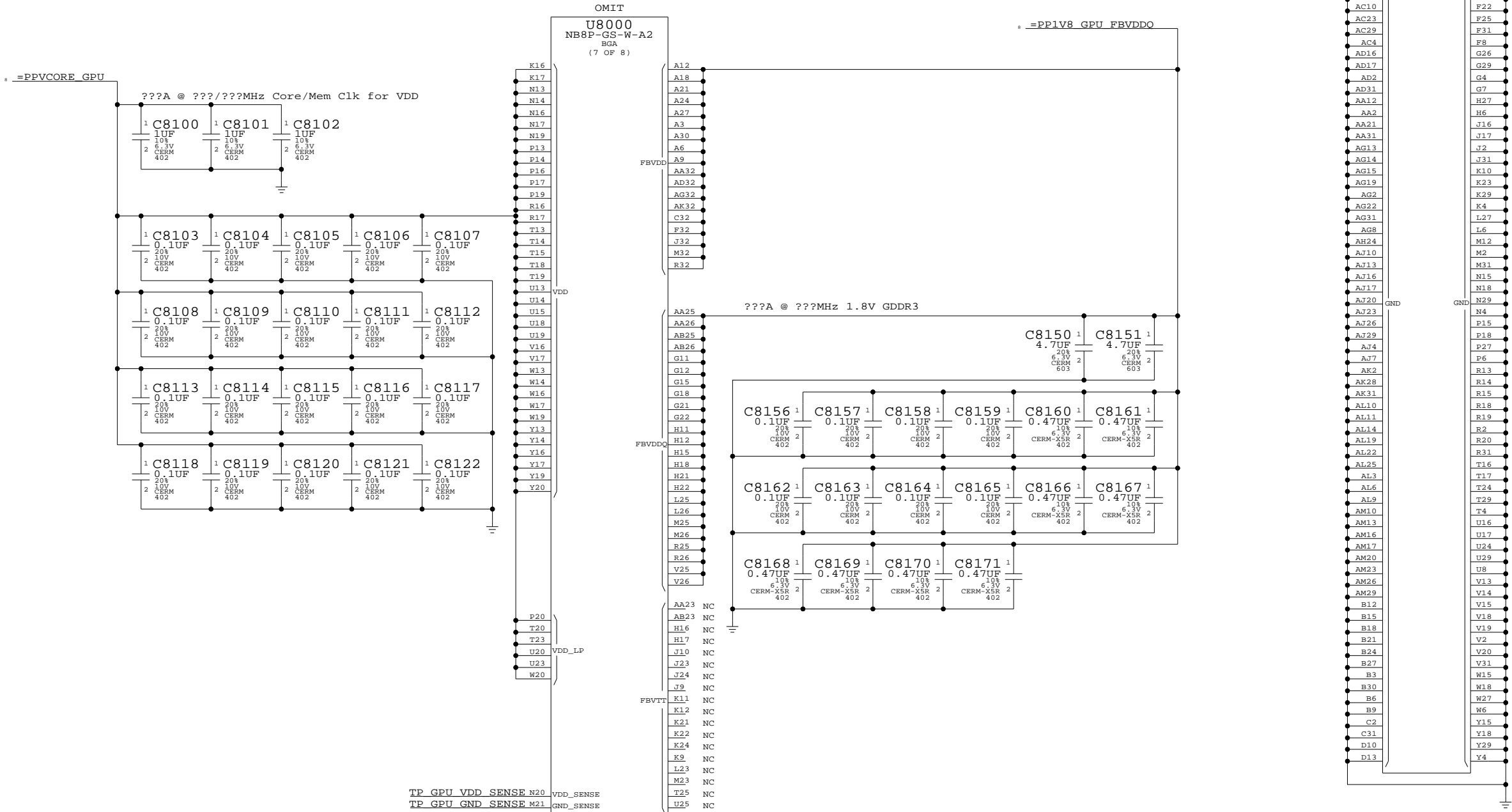
109

Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G84M Core/FB Power

SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

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APPLE COMPUTER INC.

SIZE DRAWING NUMBER REV.

D 051-7261 16

SCALE NONE SHT 81 OF 109

```
Power aliases required by this page:
- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO
```

```
Signal aliases required by this page:
(NONE)
```

```
BOM options provided by this page:
(NONE)
```



NV G84M Frame Buffer I/F
SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

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 APPLE COMPUTER INC.

SIZE D	DRAWING NUMBER 051-7261	REV. 16
SCALE NONE	SHT 82	OF 109

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer A

SYNC_MASTER=M75_MLB SYNC_DATE=04/02/2007

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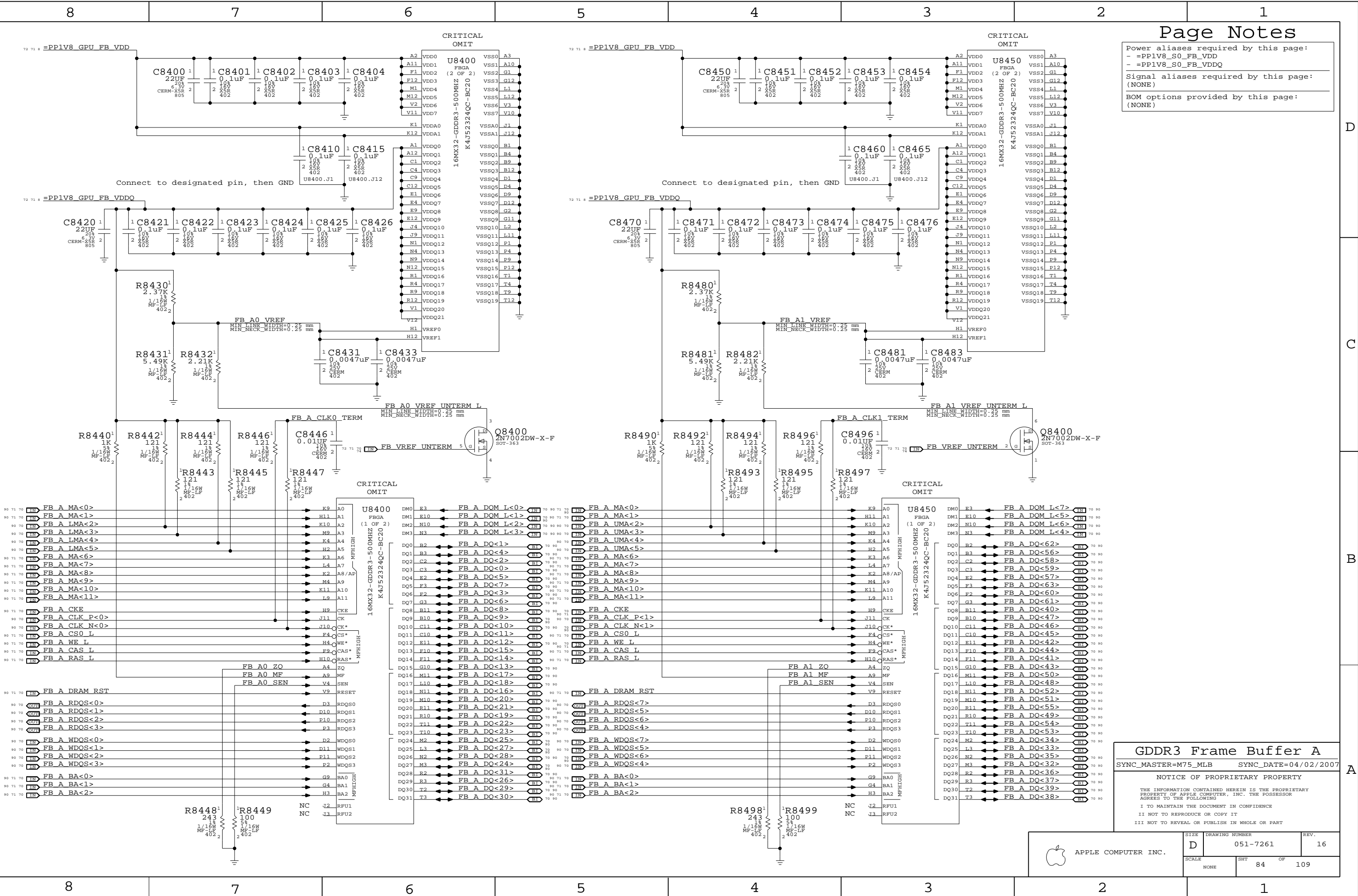
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7261	16
SCALE	SHT	OF
NONE	84	109



Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer B

SYNC_MASTER=M75_MLB SYNC_DATE=04/02/2007

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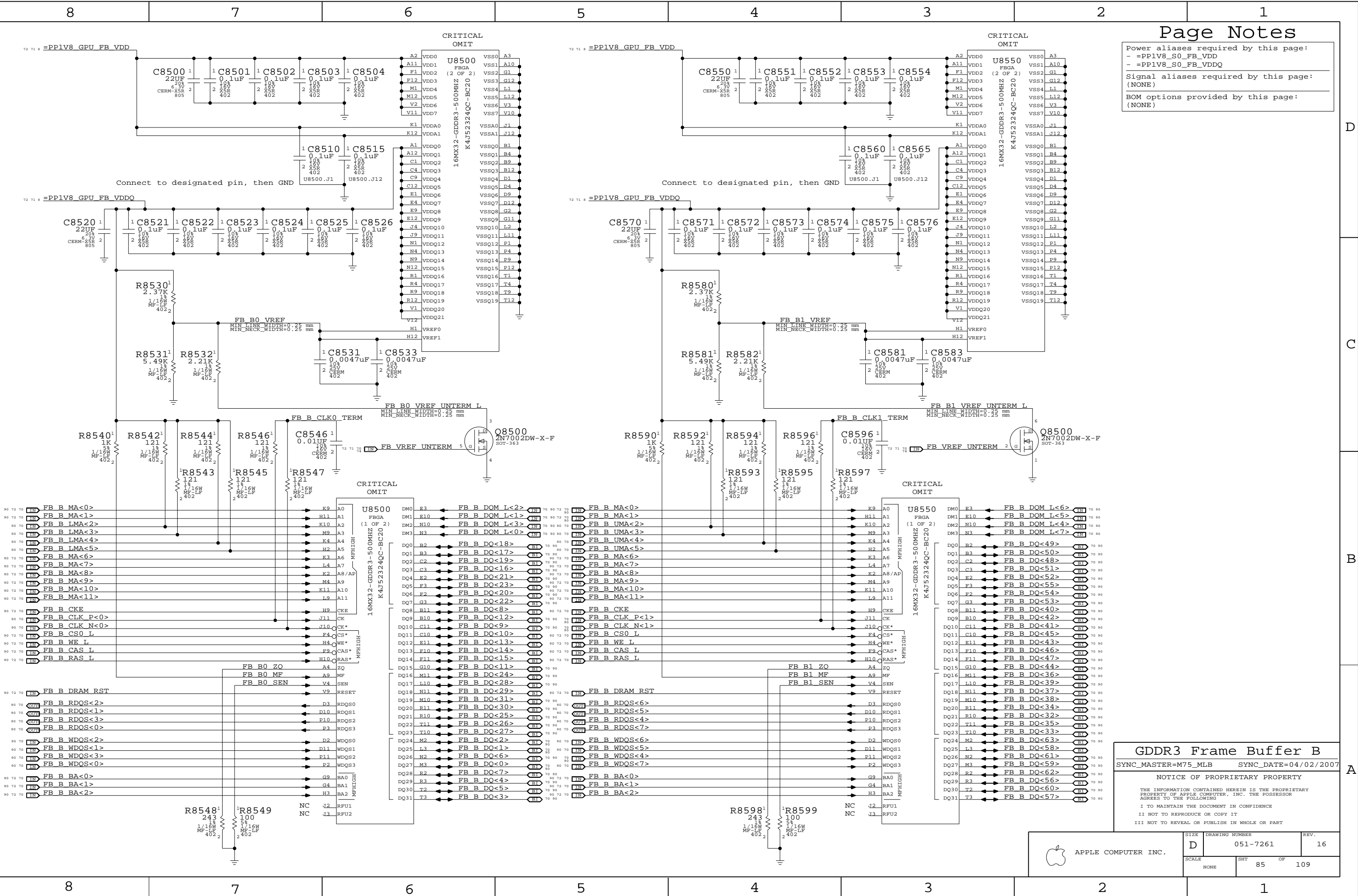
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SIZE	DRAWING NUMBER	REV.
D	051-7261	16
SCALE	SHT	OF
NONE	85	109

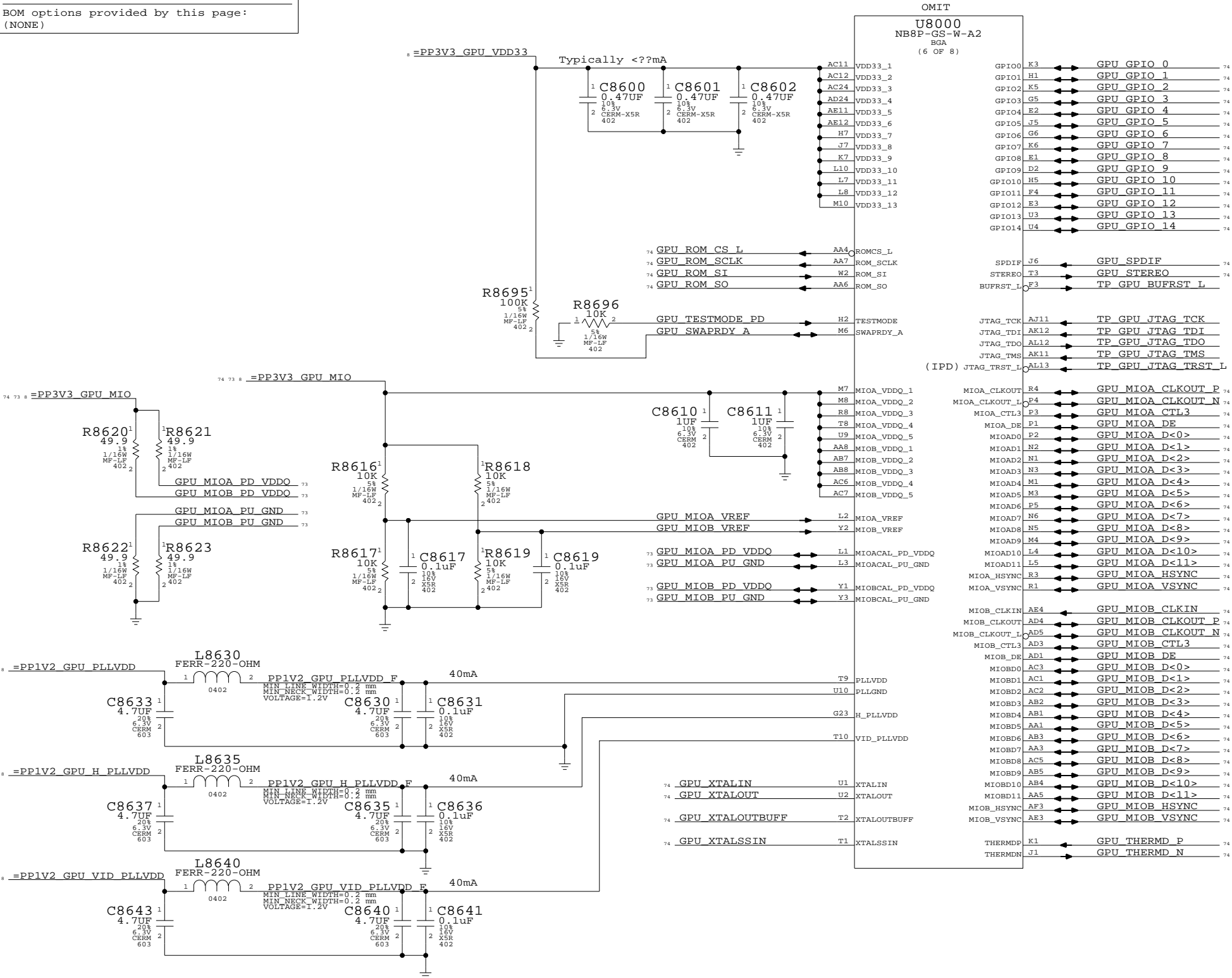


Page Notes

Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP3V3_GPU_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G84M GPIO/MIO/Misc

SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

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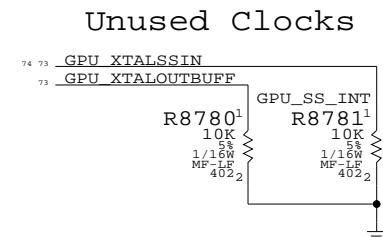
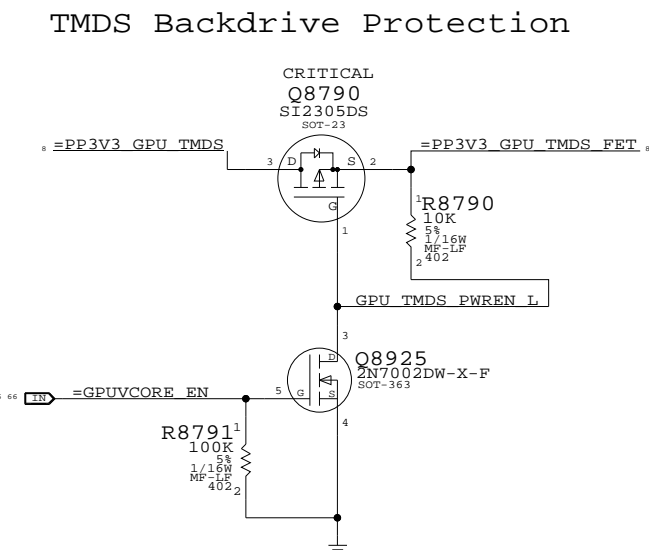
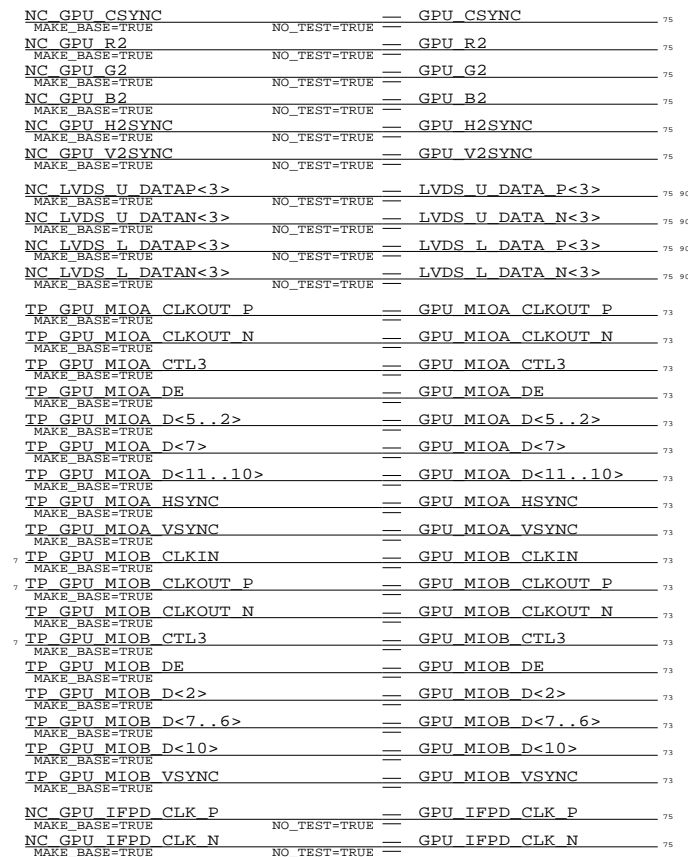
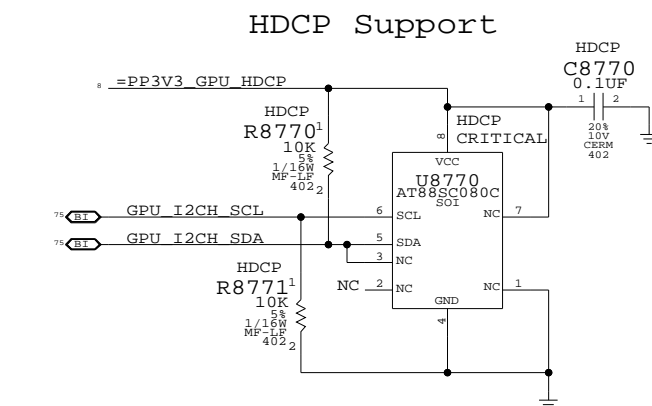
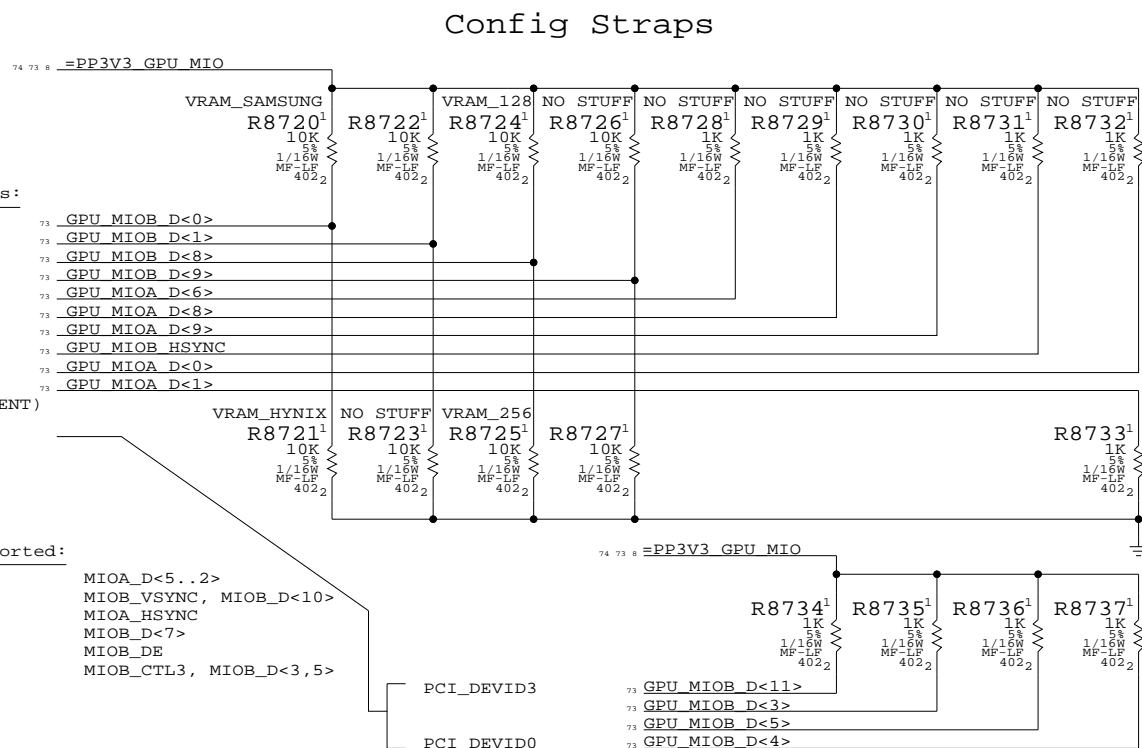
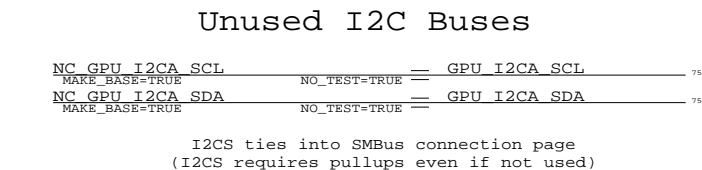
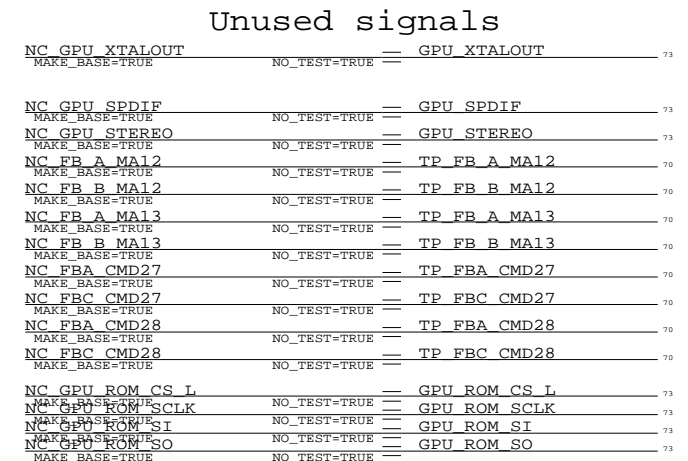
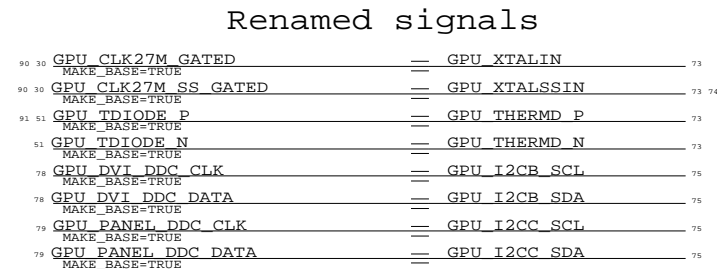
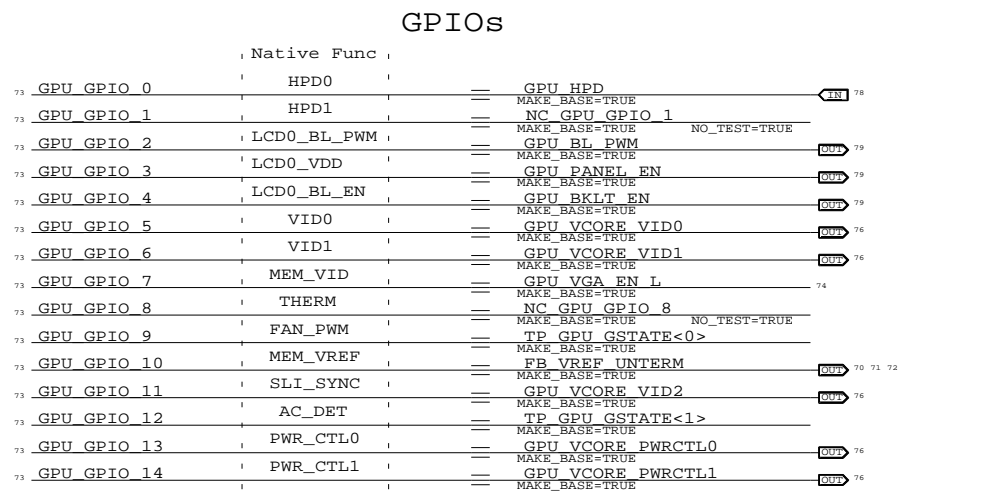
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SIZE D DRAWING NUMBER 051-7261 REV. 16

SCALE NONE SHT 86 OF 109



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1718	1	1C,TS3V340,QUAD VIDEO SW,BFN16	U8700	CRITICAL	
PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
353S1579	353S1718		ALL (U8700)	TS3V330 alt to TS3V340	

GPU Straps			
SYNC_MASTER=M75_MLB		SYNC_DATE=04/02/2007	
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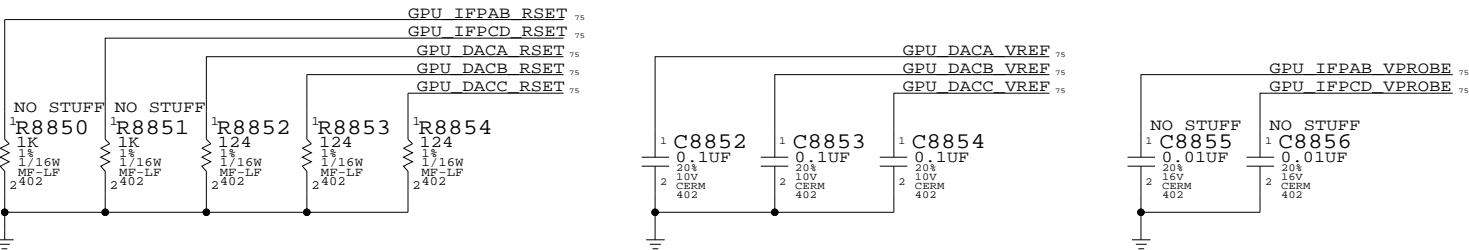
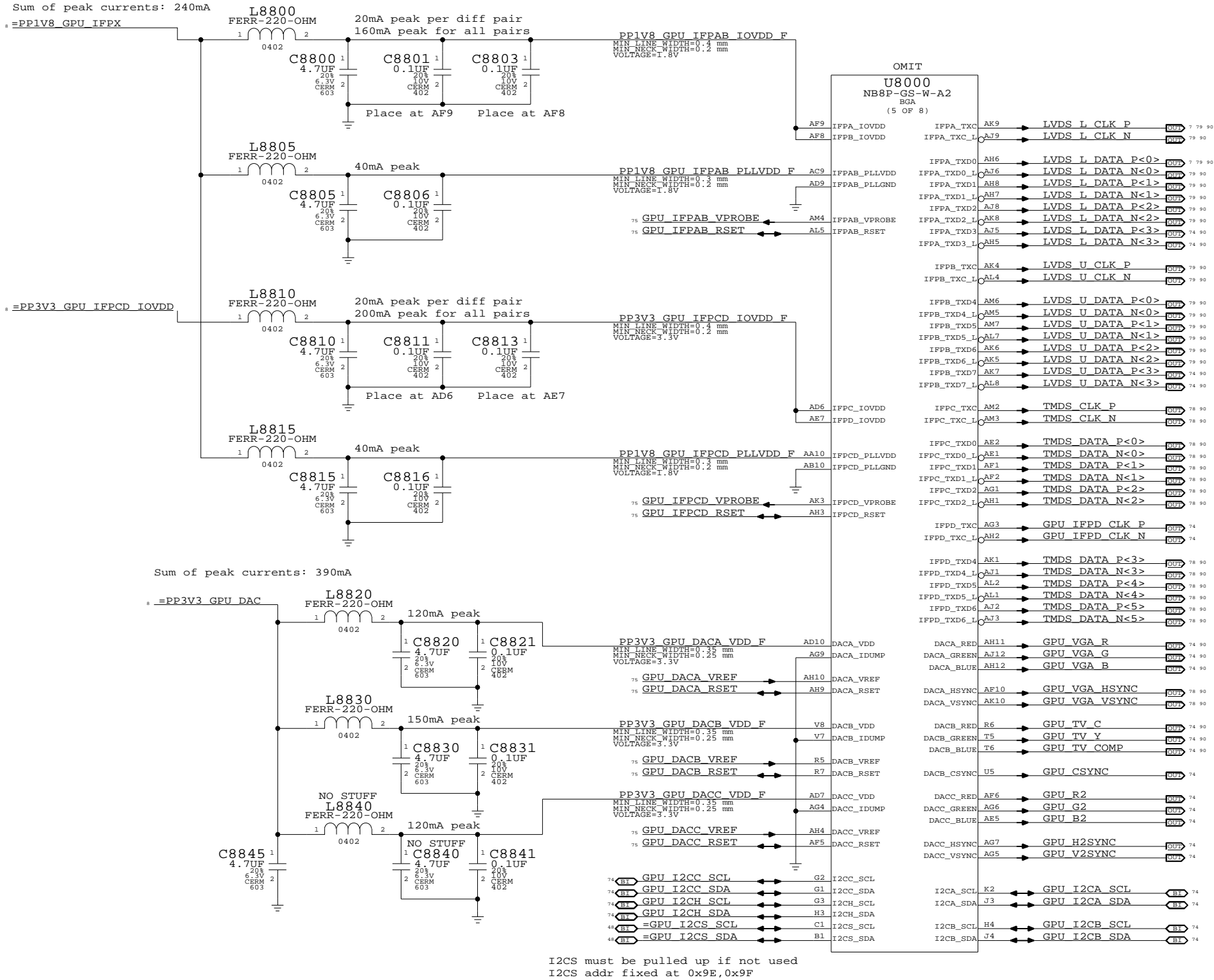
 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	16
	SCALE	SHT	OF
	NONE	87	109

Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD
- =PP3V3_GPU_DAC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G84M Video Interfaces

SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

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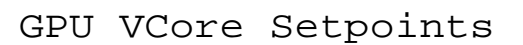
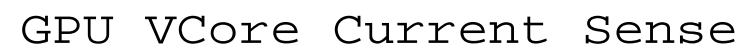
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SIZE	DRAWING NUMBER	REV.
D	051-7261	16
SCALE	SHT	OF
NONE	88	109



VID2	VID1	VID0	C	D	E	State
0	0	0	-	-	-	1.050V (rsvd state)
0	0	1	Y	-	-	1.050V (max batt)
0	1	1	Y	Y	-	1.125V (balanced)
1	1	1	Y	Y	Y	1.250V (max perf)

All other states not defined

GPU (G84M)	Core	Supply
------------	------	--------

SYNC_MASTER=M75_MLB	SYNC_DATE=03/21/2007
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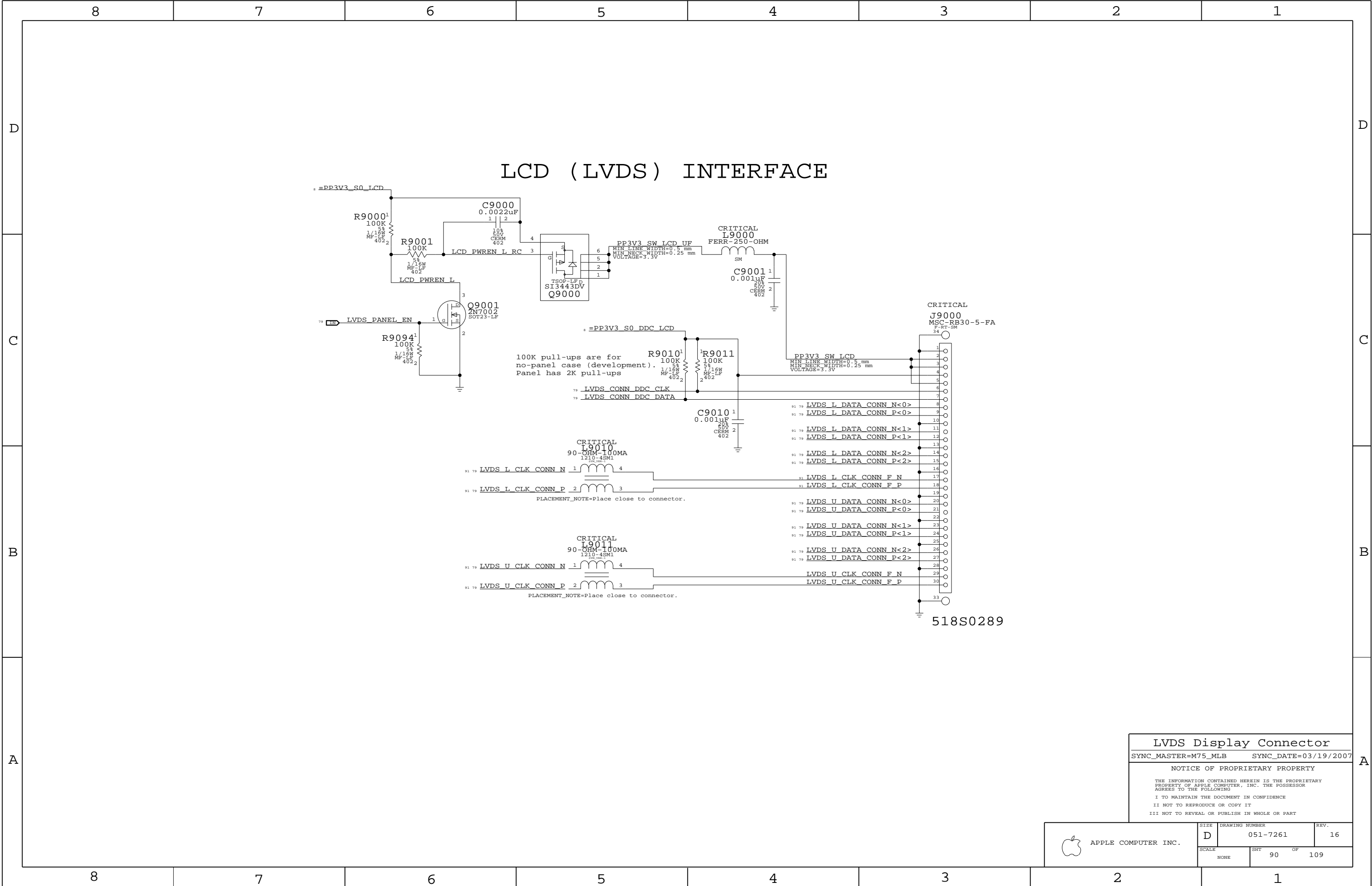
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SIZE	DRAWING NUMBER
------	----------------


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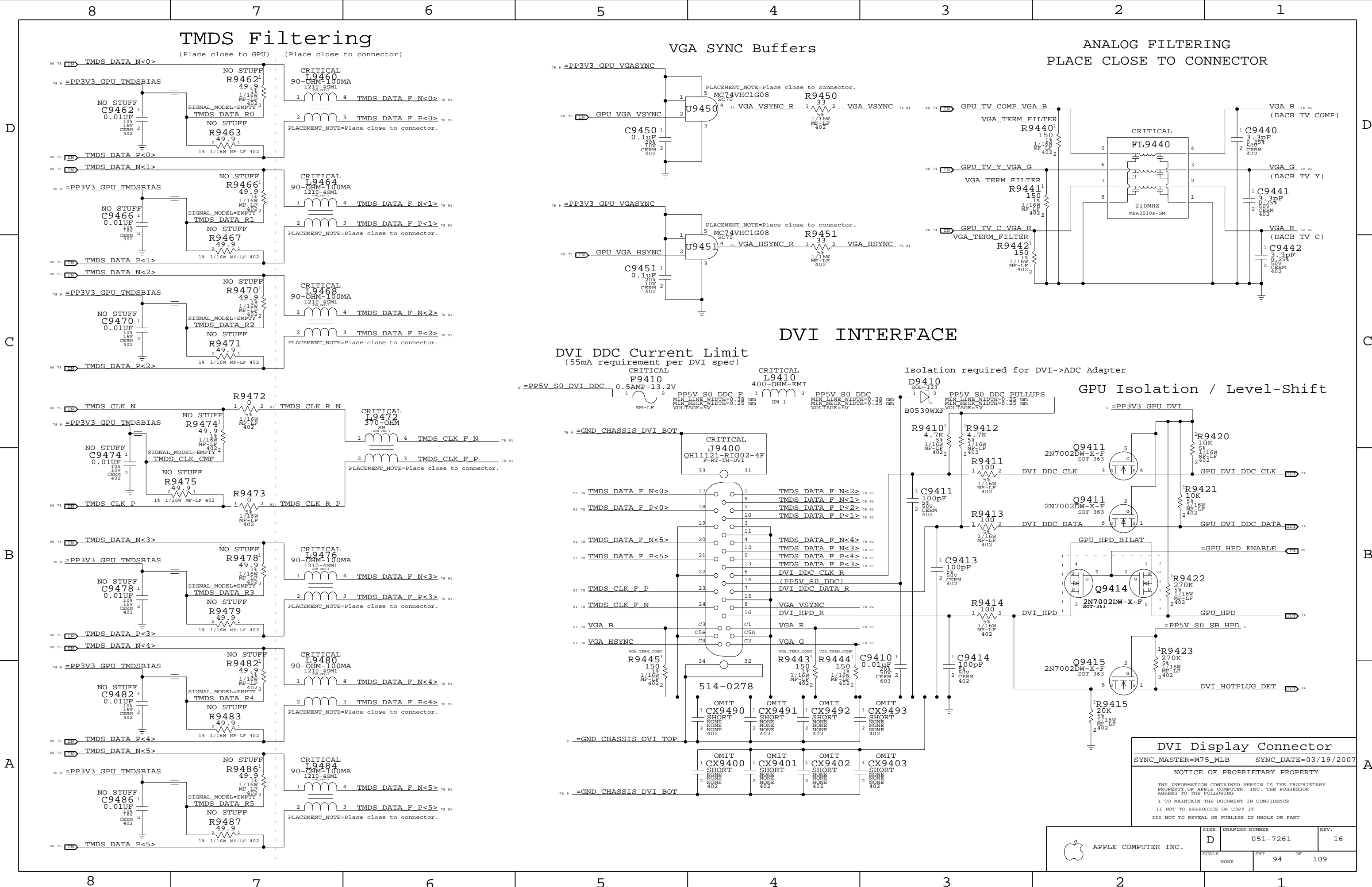
SIZE	DRAWING NUMBER	REV.
D	051-7261	16

SCALE	SHT	OF
NONE	89	109



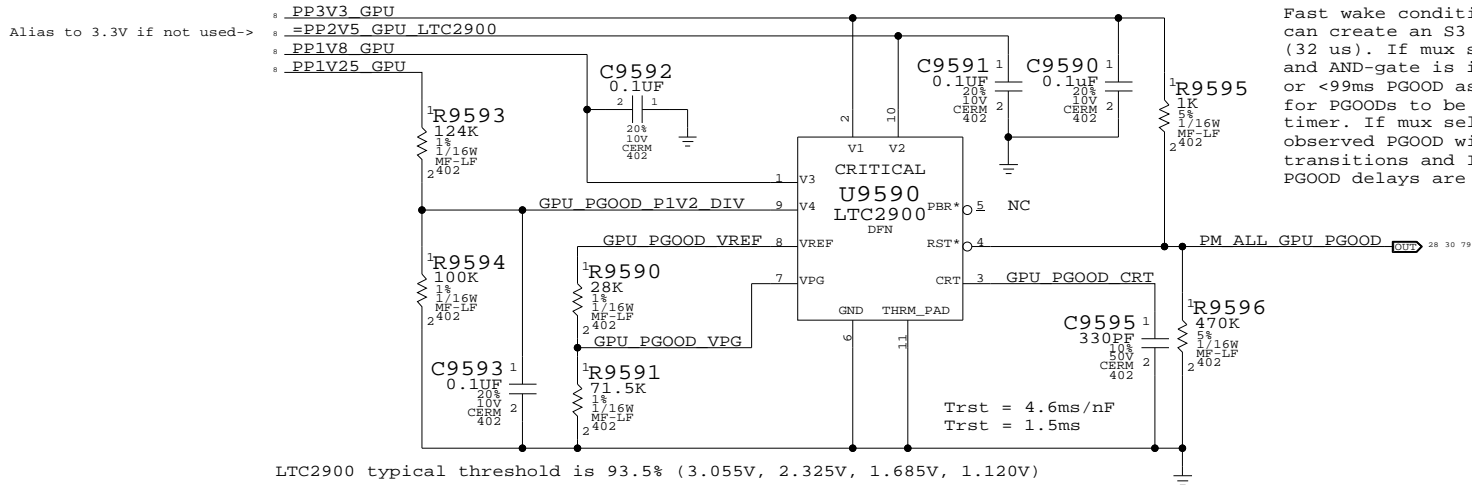
LVDS Display Connector	
SYNC_MASTER=M75_MLB	SYNC_DATE=03/19/2007
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 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7261	REV. 16
	SCALE NONE	SHT 90	OF 109

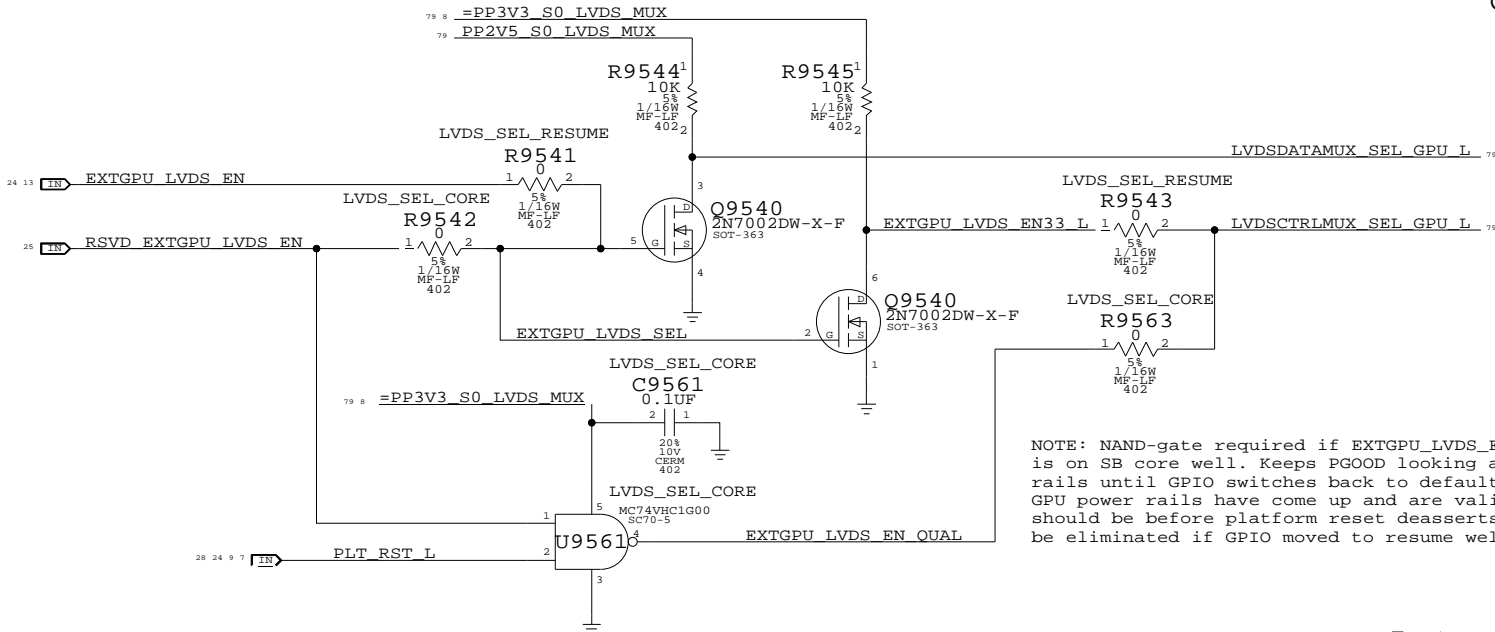


PGOOD Monitor for GPU Rails

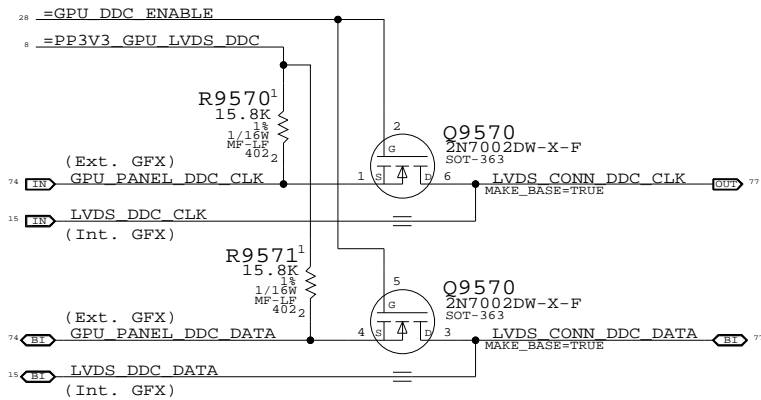
LTC2900 provides programmable reset delay which is required to play nice with ICHx PGOOD circuit



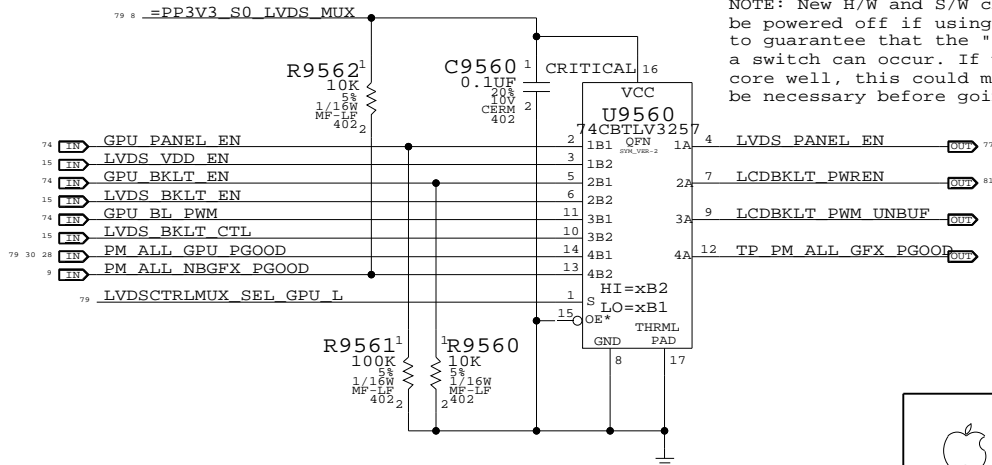
Mux Select Conditioning



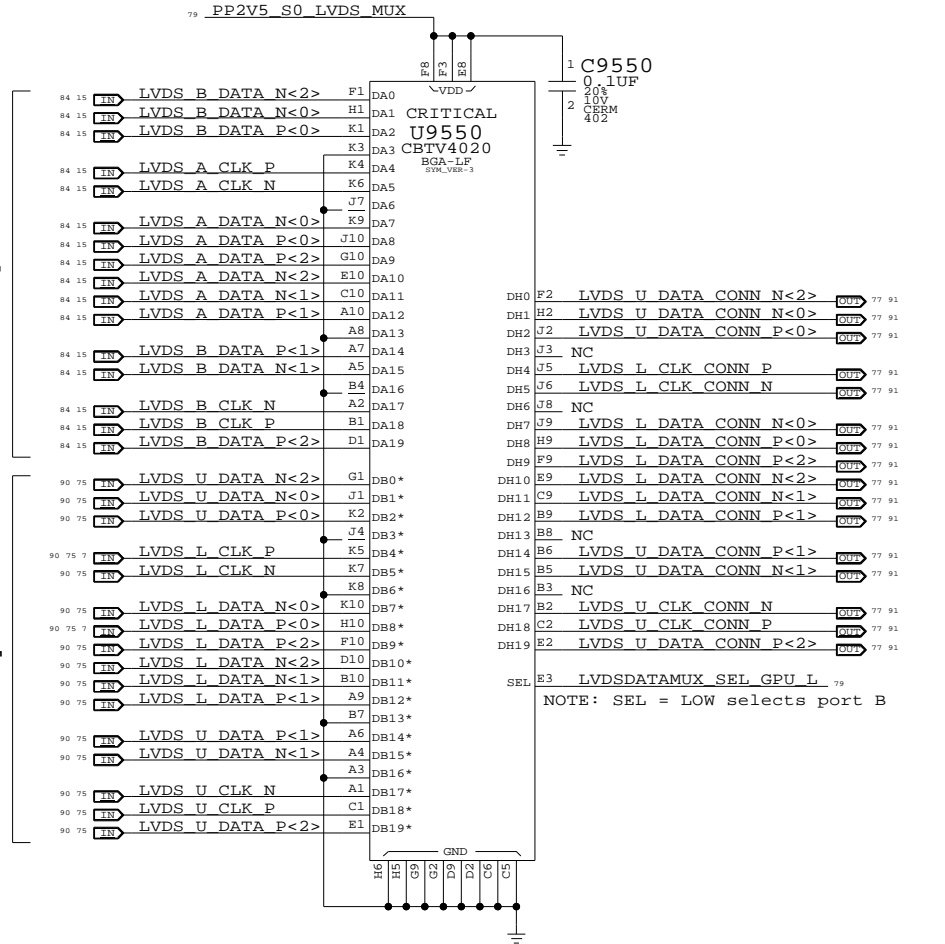
GPU DDC Pass FETs



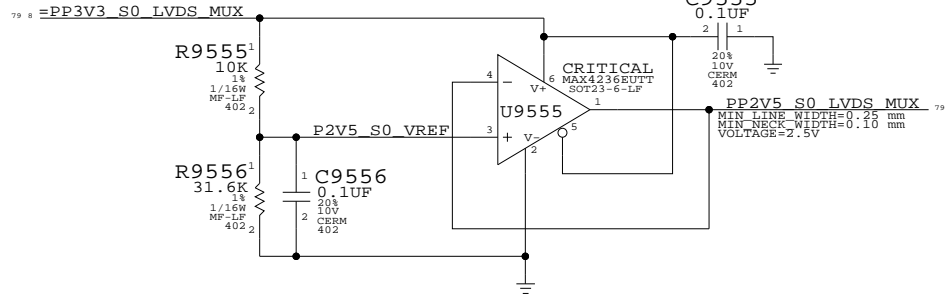
Panel/Backlight Control Mux



LVDS I/F Mux



LVDS Data Mux Power Supply



LVDS Interface Mux

SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

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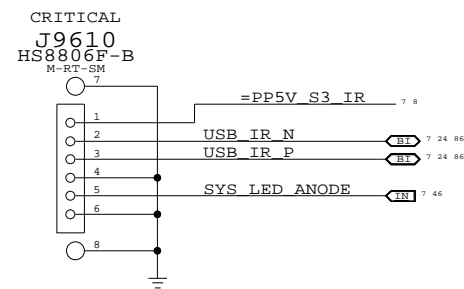
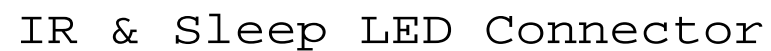
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



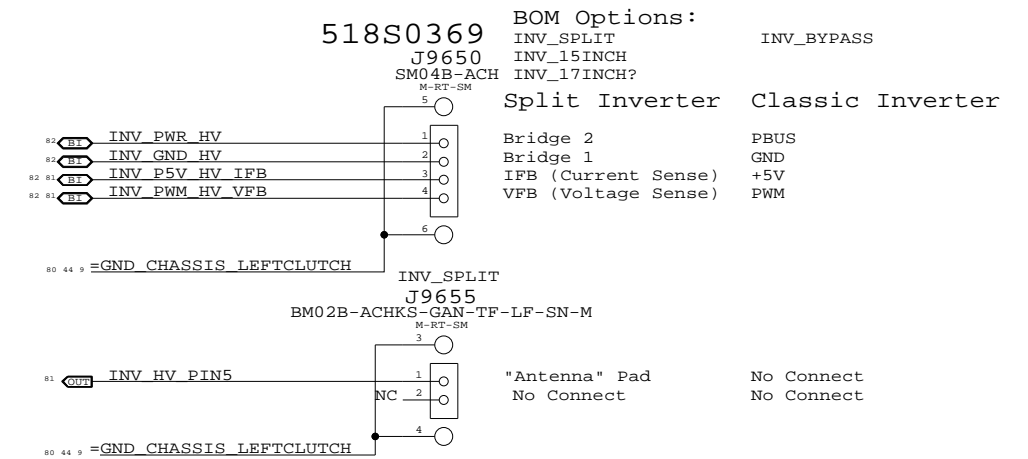
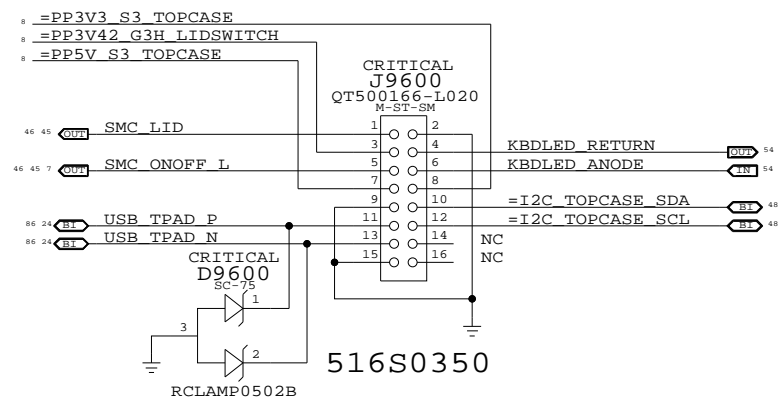
APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-7261 REV. 16

SCALE NONE SHT 95 OF 109

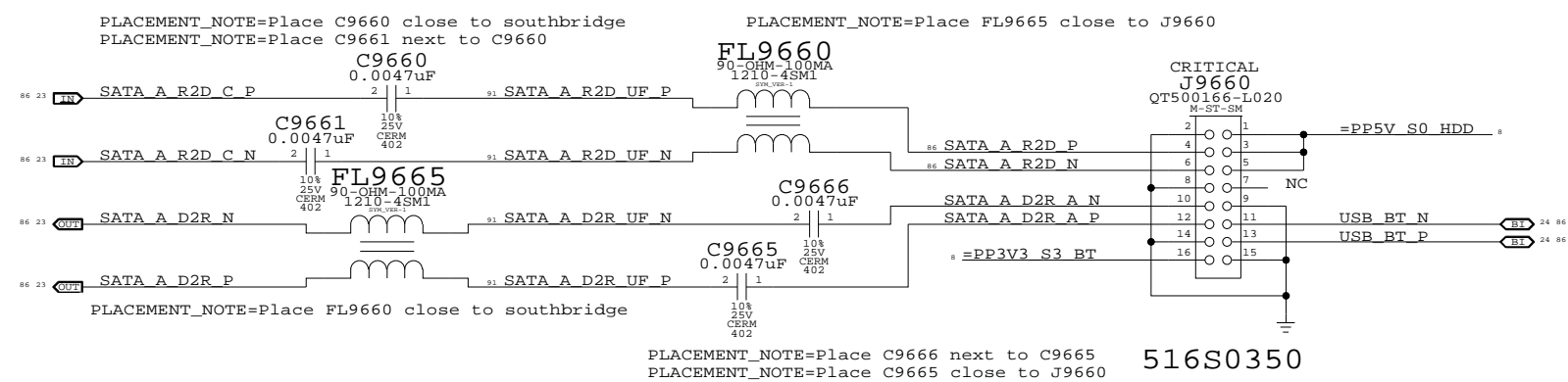


518S0474



518S0487

Bluetooth (M13P) & SATA HDD Flex Connector



M76 Specific Connectors

SYNC_MASTER= (MASTER)	SYNC_DATE= (MASTER)
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SIZE	DRAWING NUMBER
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APPLE COMPUTER INC.

SIZE D	DRAWING NUMBER 051-7261	REV. 16
SCALE NONE	SHT 96	OF 109

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	?
FSB_DATA2DATA	*	=2:1_SPACING	?
FSB_DSTB	*	=3:1_SPACING	?
FSB_DATA2DSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended. Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs. Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs. DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
FSB_COMMON	FSB_55S	FSB_COMMON	FSB ADS L 7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BNR L 7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BPRI L 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BRE00 L 7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DBSY L 7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DEFER L 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DPWR L 7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DRDY L 7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB HIT L 7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB HITM L 7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB LOCK L 7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB RS L<2..0> 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB TRDY L 10 14
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB CPURST L 7 10 13 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB D L<15..0> 7 10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB DINV L<0> 7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<0> 7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<0> 7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB D L<31..16> 7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB DINV L<1> 7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<1> 7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<1> 7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB D L<47..32> 7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB DINV L<2> 7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<2> 7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<2> 7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB D L<63..48> 7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB DINV L<3> 7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<3> 7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<3> 7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB A L<16..3> 7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB REQ L<4..0> 7 10 14
FSB_ADSTR0	FSB_55S	FSB_ADSTR	FSB ADSTB L<0> 7 10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB A L<35..17> 7 10 14
FSB_ADSTR1	FSB_55S	FSB_ADSTR	FSB ADSTB L<1> 7 10 14
CPU_IERR_L	CPU_55S		CPU IERR L 10
CPU_FERR_L	CPU_55S		CPU FERR L 10 23
CPU_PROCHOT_L	CPU_55S	CPU_2T01	CPU PROCHOT L 10 46 59
CPU_PWRGD	CPU_55S		CPU PWRGD 7 10 13 23
CPU_FROM_SB	CPU_55S		CPU INTR 10 23
CPU_FROM_SB	CPU_55S		CPU NMI 10 23
CPU_FROM_SB	CPU_55S		CPU A20M L 10 23
CPU_FROM_SB	CPU_55S		CPU DPSLP L 7 10 23
CPU_FROM_SB	CPU_55S		CPU IGNN L 10 23
CPU_INIT_L	CPU_55S		CPU INIT L 10 23 47
CPU_FROM_SB	CPU_55S		CPU SMI L 10 23
CPU_FROM_SB	CPU_55S		CPU STPCLK L 10 23 47
PM_THERMTRIP_L	CPU_55S	CPU_2T01	PM THERMTRIP L 10 16 23 47
FSB_CPUSLP_L	CPU_55S		FSB CPUSLP L 7 10 16 23 47
PM_DPSRLEVR	CPU_55S	CPU_2T01	PM DPSRLEVR 7 16 25 59
(See above)	CPU_55S	CPU_2T01	IMVP DPSRLEVR 7 59
CPU_BSEL0	CPU_55S	CPU_2T01	CPU BSEL<0> 10 30
(See above)	CPU_55S	CPU_2T01	NB BSEL<0> 13 16 30
CPU_BSEL1	CPU_55S	CPU_2T01	CPU BSEL<1> 10 30
(See above)	CPU_55S	CPU_2T01	NB BSEL<1> 13 16 30
CPU_BSEL2	CPU_55S	CPU_2T01	CPU BSEL<2> 10 30
(See above)	CPU_55S	CPU_2T01	NB BSEL<2> 13 16 30
CPU_DPRSTP_L	CPU_55S	CPU_2T01	CPU DPRSTP L 7 10 16 23
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU GTLREF 10
CPU_COMP	CPU_55S	CPU_COMP	CPU COMP<3> 10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2> 10
CPU_COMP	CPU_55S	CPU_COMP	CPU COMP<1> 10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0> 10
XDP_TDI	CPU_55S	CPU_ITP	XDP TDI 10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP TDO 10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP TMS 10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP TCK 10 13
XDP_TRST_L	CPU_55S	CPU_ITP	XDP TRST L 10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP BPM L<4..0> 10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP BPM L<5> 10 13
	CLK_FSB_100D	CLK_FSB	XDP CLK_P 13 30 48
	CLK_FSB_100D	CLK_FSB	XDP CLK_N 13 30 48
(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP CPURST_L 13
	CPU_55S	CPU_2T01	CPU VID<6..0> 13 12
	CPU_55S	CPU_2T01	IMVP6_VID<6..0> 7 12 59
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P 13 59
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N 13 59
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P 59
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N 59

CPU/FSB Constraints

SYNC_MASTER=T9_NOME	SYNC_DATE=01/25/2007	7
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SIZE D	DRAWING NUMBER 051-7261	REV. 16
SCALE NONE	SHT 100	OF 109

87654321

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CRT_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS	*	20 MIL	?
CRT	*	25 MIL	?
CRT_2CRT	*	20 MIL	?
CRT_SYNC	*	25 MIL	?
CRT_SYNC2SYNC	*	20 MIL	?
TVDAC	*	25 MIL	?
TVDAC_2TVDAC	*	20 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT
CRT_SYNC	CRT_SYNC	*	CRT_SYNC2SYNC
TVDAC	TVDAC	*	TVDAC_2TVDAC

LVDS signals are 100-ohm +/- 20% differential impedance.
CRT & TVDAC signal single-ended impedance varies by location:
- 37.5-ohm +/- 15% from GMCH to first termination resistor.
- 50-ohm +/- 15% from first to second termination resistor.
- 55-ohm +/- 15% from second termination resistor to connector.
CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

NET TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
PEG_R2D	PCIE_100D	PCIE	PEG R2D P<15..0>	68
	PCIE_100D	PCIE	PEG R2D N<15..0>	68
	PCIE_100D	PCIE	PEG R2D C P<15..0>	15 68
	PCIE_100D	PCIE	PEG R2D C N<15..0>	15 68
PEG_D2R	PCIE_100D	PCIE	PEG D2R P<15..0>	15 68
	PCIE_100D	PCIE	PEG D2R N<15..0>	15 68
	PCIE_100D	PCIE	PEG D2R C P<15..0>	68
	PCIE_100D	PCIE	PEG D2R C N<15..0>	68
DMI_N2S	DMI_100D	DMI	DMI N2S P<3..0>	16 24
	DMI_100D	DMI	DMI N2S N<3..0>	16 24
DMI_S2N	DMI_100D	DMI	DMI S2N P<3..0>	16 24
	DMI_100D	DMI	DMI S2N N<3..0>	16 24
LVDS_A_CLK	LVDS_100D	LVDS	LVDS A CLK P	15 79
LVDS_A_CLK	LVDS_100D	LVDS	LVDS A CLK N	15 79
LVDS_A_DATA	LVDS_100D	LVDS	LVDS A DATA P<2..0>	15 79
LVDS_A_DATA	LVDS_100D	LVDS	LVDS A DATA N<2..0>	15 79
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS A DATA P<3>	
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS A DATA N<3>	
LVDS_B_CLK	LVDS_100D	LVDS	LVDS B CLK P	15 79
LVDS_B_CLK	LVDS_100D	LVDS	LVDS B CLK N	15 79
LVDS_B_DATA	LVDS_100D	LVDS	LVDS B DATA P<2..0>	15 79
LVDS_B_DATA	LVDS_100D	LVDS	LVDS B DATA N<2..0>	15 79
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS B DATA P<3>	
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS B DATA N<3>	
LVDS_IBG		LVDS	LVDS IBG	15 22
CRT_TVO_IREF		CRT	CRT TVO_IREF	
CRT_RED	CRT_50S	CRT	CRT RED	
CRT_GREEN	CRT_50S	CRT	CRT GREEN	
CRT_BLUE	CRT_50S	CRT	CRT BLUE	
CRT_SYNC	CRT_55S	CRT_SYNC	CRT HSYNC R	
CRT_SYNC	CRT_55S	CRT_SYNC	CRT VSYNC R	
TV_A_DAC	CRT_50S	TVDAC	TV A DAC	
TV_B_DAC	CRT_50S	TVDAC	TV B DAC	
TV_C_DAC	CRT_50S	TVDAC	TV C DAC	

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NB Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

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SCALE	SHT	OF
NONE	101	109

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3

2

1

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM_*-style wildcards!

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_CLK P<2..0>	16 31
	MEM_70D	MEM_CLK	MEM_CLK N<2..0>	16 31
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<1..0>	16 31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CS L<1..0>	16 31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_ODT<1..0>	16 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A A<14..0>	16 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A BS<2..0>	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A RAS L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A CAS L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A WE L	17 31 33
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A DQ<7..0>	17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A DQ<15..8>	17 31
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A DQ<23..16>	17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A DQ<31..24>	17 31
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A DQ<39..32>	17 31
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A DQ<47..40>	17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A DQ<55..48>	17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A DQ<63..56>	17 31
MEM_A_DM0	MEM_55S	MEM_DATA	MEM_A DM<0>	17 31
MEM_A_DM1	MEM_55S	MEM_DATA	MEM_A DM<1>	17 31
MEM_A_DM2	MEM_55S	MEM_DATA	MEM_A DM<2>	17 31
MEM_A_DM3	MEM_55S	MEM_DATA	MEM_A DM<3>	17 31
MEM_A_DM4	MEM_55S	MEM_DATA	MEM_A DM<4>	17 31
MEM_A_DM5	MEM_55S	MEM_DATA	MEM_A DM<5>	17 31
MEM_A_DM6	MEM_55S	MEM_DATA	MEM_A DM<6>	17 31
MEM_A_DM7	MEM_55S	MEM_DATA	MEM_A DM<7>	17 31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A DQS P<0>	17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A DQS N<0>	17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A DQS P<1>	17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A DQS N<1>	17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A DQS P<2>	17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A DQS N<2>	17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A DQS P<3>	17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A DQS N<3>	17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A DQS P<4>	17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A DQS N<4>	17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A DQS P<5>	17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A DQS N<5>	17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A DQS P<6>	17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A DQS N<6>	17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A DQS P<7>	17 31
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_CLK P<5..3>	16 32
	MEM_70D	MEM_CLK	MEM_CLK N<5..3>	16 32
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<4..3>	16 32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CS L<3..2>	16 32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_ODT<3..2>	16 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B A<14..0>	16 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B BS<2..0>	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B RAS L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B CAS L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B WE L	17 32 33
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B DQ<7..0>	17 32
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B DQ<15..8>	17 32
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B DQ<23..16>	17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B DQ<31..24>	17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B DQ<39..32>	17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B DQ<47..40>	17 32
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B DQ<55..48>	17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B DQ<63..56>	17 32
MEM_B_DM0	MEM_55S	MEM_DATA	MEM_B DM<0>	17 32
MEM_B_DM1	MEM_55S	MEM_DATA	MEM_B DM<1>	17 32
MEM_B_DM2	MEM_55S	MEM_DATA	MEM_B DM<2>	17 32
MEM_B_DM3	MEM_55S	MEM_DATA	MEM_B DM<3>	17 32
MEM_B_DM4	MEM_55S	MEM_DATA	MEM_B DM<4>	17 32
MEM_B_DM5	MEM_55S	MEM_DATA	MEM_B DM<5>	17 32
MEM_B_DM6	MEM_55S	MEM_DATA	MEM_B DM<6>	17 32
MEM_B_DM7	MEM_55S	MEM_DATA	MEM_B DM<7>	17 32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B DQS P<0>	17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B DQS N<0>	17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B DQS P<1>	17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B DQS N<1>	17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B DQS P<2>	17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B DQS N<2>	17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B DQS P<3>	17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B DQS N<3>	17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B DQS P<4>	17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B DQS N<4>	17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B DQS P<5>	17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B DQS N<5>	17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B DQS P<6>	17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B DQS N<6>	17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B DQS P<7>	17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B DQS N<7>	17 32

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Memory Constraints

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

Need to support MEM_*-style wildcards!

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

Memory Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Controller Link (AMT) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLINK_12MIL	*	=STANDARD	12 MILS	5 MILS	300 MILS	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLINK	*	=1.8:1_SPACING	?
CLINK_VREF	*	12 MILS	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Ethernet (Yukon) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MILS	?

SOURCE: Based on Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
PCI_AD	PCI_55S	PCI	PCI_AD<18..0>	24 38
PCI_AD19	PCI_55S	PCI	PCI_AD<19>	24 38
PCI_AD20	PCI_55S	PCI	PCI_AD<20>	24 38
PCI_AD	PCI_55S	PCI	PCI_AD<31..21>	24 38
PCI_AD	PCI_55S	PCI	PCI_PAR	24 38
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>	24 38
PCI_CNTRL	PCI_55S	PCI	PCI_IRDY_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI_DEVSEL_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI_PERR_L	24 38
PCI_LOCK_L	PCI_55S	PCI	PCI_LOCK_L	24
PCI_CNTRL	PCI_55S	PCI	PCI_SERR_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI_STOP_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI_TRDY_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI_FRAME_L	24 38
PCI_FW_REQ_L	PCI_55S	PCI	PCI_FW_REQ_L	24 38
PCI_FW_GNT_L	PCI_55S	PCI	PCI_FW_GNT_L	24 38
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	24
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L	
PCI_REQ2_L	PCI_55S	PCI	PCI_REQ2_L	24
PCI_GNT2_L	PCI_55S	PCI	PCI_GNT2_L	
INT_PIRQA_L	PCI_55S	PCI	INT_PIRQA_L	24
INT_PIRQB_L	PCI_55S	PCI	INT_PIRQB_L	24
INT_PIROC_L	PCI_55S	PCI	INT_PIROC_L	24
INT_PIROD_L	PCI_55S	PCI	INT_PIROD_L	24 38
INT_PIROE_L	PCI_55S	PCI	INT_PIROE_L	24
INT_PIROF_L	PCI_55S	PCI	INT_PIROF_L	24
PCIE_A_R2D	PCIE_100D	PCIE	PCIE_A_R2D_C_P	
PCIE_100D	PCIE		PCIE_A_R2D_C_N	
PCIE_A_D2R	PCIE_100D	PCIE	PCIE_A_D2R_P	
PCIE_100D	PCIE		PCIE_A_D2R_N	
PCIE_B_R2D	PCIE_100D	PCIE	PCIE_B_R2D_C_P	
PCIE_100D	PCIE		PCIE_B_R2D_C_N	
PCIE_B_D2R	PCIE_100D	PCIE	PCIE_B_D2R_P	
PCIE_100D	PCIE		PCIE_B_D2R_N	
PCIE_EXCARD_R2D	PCIE_100D	PCIE	PCIE_EXCARD_R2D_C_P	34
PCIE_100D	PCIE		PCIE_EXCARD_R2D_C_N	34
PCIE_EXCARD_D2R	PCIE_100D	PCIE	PCIE_EXCARD_D2R_P	34
PCIE_100D	PCIE		PCIE_EXCARD_D2R_N	34
PCIE_FW_R2D	PCIE_100D	PCIE	PCIE_FW_R2D_C_P	
PCIE_100D	PCIE		PCIE_FW_R2D_C_N	
PCIE_FW_D2R	PCIE_100D	PCIE	PCIE_FW_D2R_P	
PCIE_100D	PCIE		PCIE_FW_D2R_N	
PCIE_MINI_R2D	PCIE_100D	PCIE	PCIE_MINI_R2D_C_P	24 34
PCIE_100D	PCIE		PCIE_MINI_R2D_C_N	24 34
PCIE_MINI_D2R	PCIE_100D	PCIE	PCIE_MINI_D2R_P	24 34
PCIE_100D	PCIE		PCIE_MINI_D2R_N	24 34
GLAN_COMP			GLAN_COMP	23
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_CLK	16 25
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_DATA	16 25
CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK_NB_RESET_L	16 25
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_CLK	
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_DATA	
CLINK_WLAN_RESET_L	CLINK_55S	CLINK	CLINK_WLAN_RESET_L	
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB_CLINK_VREF	16
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF0	25
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF1	25
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE_ENET_R2D_C_P	24 35
PCIE_100D	PCIE		PCIE_ENET_R2D_C_N	24 35
PCIE_100D	PCIE		PCIE_ENET_R2D_P	35
PCIE_100D	PCIE		PCIE_ENET_R2D_N	35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE_ENET_D2R_P	24 35
PCIE_100D	PCIE		PCIE_ENET_D2R_N	24 35
PCIE_100D	PCIE		PCIE_ENET_D2R_C_P	35
PCIE_100D	PCIE		PCIE_ENET_D2R_C_N	35
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<0>	35 37
ENET_100D	ENET_MDI		ENET_MDI_N<0>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<1>	35 37
ENET_100D	ENET_MDI		ENET_MDI_N<1>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<2>	35 37
ENET_100D	ENET_MDI		ENET_MDI_N<2>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3>	35 37
ENET_100D	ENET_MDI		ENET_MDI_N<3>	35 37

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SB Constraints (2 of 2)

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

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GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R50SE	*	=50_OHM_SE	=40_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR3_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TMD5_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
VGA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TMDS	*	20 MIL	?
VGA	*	20 MIL	?
VGA_SYNC	*	20 MIL	?

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	FB_A_CLK_P	GDDR3_80D	GDDR3_CLK	FB A CLK P<0>	70 71
		GDDR3_80D	GDDR3_CLK	FB A CLK N<0>	70 71
	FB_B_CLK_P	GDDR3_80D	GDDR3_CLK	FB A CLK P<1>	70 71
		GDDR3_80D	GDDR3_CLK	FB A CLK N<1>	70 71
	FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB A MA<1..0>	70 71
	FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB A MA<11..6>	70 71
	FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB A BA<2..0>	70 71
	FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB A RAS_L	70 71
	FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB A CAS_L	70 71
	FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB A WE_L	70 71
	FB_AB_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB A CKE	70 71
	FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB A CS0_L	70 71
	FB_AB_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB A DRAM_RST	70 71
	FB_A_CMD	GDDR3_50SE	GDDR3_CMD	FB A LMA<5..2>	70 71
	FB_B_CMD	GDDR3_50SE	GDDR3_CMD	FB A UMA<5..2>	70 71
	FB_A_WDQS0	GDDR3_50SE	GDDR3_DQS	FB A WDQS<0>	70 71
	FB_A_WDQS1	GDDR3_50SE	GDDR3_DQS	FB A WDQS<1>	70 71
	FB_A_WDQS2	GDDR3_50SE	GDDR3_DQS	FB A WDQS<2>	70 71
	FB_A_WDQS3	GDDR3_50SE	GDDR3_DQS	FB A WDQS<3>	70 71
	FB_A_RDQS0	GDDR3_50SE	GDDR3_DQS	FB A RDQS<0>	70 71
	FB_A_RDQS1	GDDR3_50SE	GDDR3_DQS	FB A RDQS<1>	70 71
	FB_A_RDQS2	GDDR3_50SE	GDDR3_DQS	FB A RDQS<2>	70 71
	FB_A_RDQS3	GDDR3_50SE	GDDR3_DQS	FB A RDQS<3>	70 71
	FB_A_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB A DQ<7..0>	70 71
	FB_A_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB A DQ<15..8>	70 71
	FB_A_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB A DQ<23..16>	70 71
	FB_A_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB A DQ<31..24>	70 71
	FB_A_DQM0	GDDR3_50SE	GDDR3_DATA	FB A DQM_L<0>	70 71
	FB_A_DQM1	GDDR3_50SE	GDDR3_DATA	FB A DQM_L<1>	70 71
	FB_A_DQM2	GDDR3_50SE	GDDR3_DATA	FB A DQM_L<2>	70 71
	FB_A_DQM3	GDDR3_50SE	GDDR3_DATA	FB A DQM_L<3>	70 71
	FB_B_WDQS0	GDDR3_50SE	GDDR3_DQS	FB B WDQS<4>	70 71
	FB_B_WDQS1	GDDR3_50SE	GDDR3_DQS	FB B WDQS<5>	70 71
	FB_B_WDQS2	GDDR3_50SE	GDDR3_DQS	FB B WDQS<6>	70 71
	FB_B_WDQS3	GDDR3_50SE	GDDR3_DQS	FB B WDQS<7>	70 71
	FB_B_RDQS0	GDDR3_50SE	GDDR3_DQS	FB B RDQS<4>	70 71
	FB_B_RDQS1	GDDR3_50SE	GDDR3_DQS	FB B RDQS<5>	70 71
	FB_B_RDQS2	GDDR3_50SE	GDDR3_DQS	FB B RDQS<6>	70 71
	FB_B_RDQS3	GDDR3_50SE	GDDR3_DQS	FB B RDQS<7>	70 71
	FB_B_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB B DQ<39..32>	70 71
	FB_B_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB B DQ<47..40>	70 71
	FB_B_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB B DQ<55..48>	70 71
	FB_B_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB B DQ<63..56>	70 71
	FB_B_DQM0	GDDR3_50SE	GDDR3_DATA	FB B DQM_L<4>	70 71
	FB_B_DQM1	GDDR3_50SE	GDDR3_DATA	FB B DQM_L<5>	70 71
	FB_B_DQM2	GDDR3_50SE	GDDR3_DATA	FB B DQM_L<6>	70 71
	FB_B_DQM3	GDDR3_50SE	GDDR3_DATA	FB B DQM_L<7>	70 71

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	FB_C_CLK_P	GDDR3_80D	GDDR3_CLK	FB B CLK P<0>
		GDDR3_80D	GDDR3_CLK	FB B CLK N<0>
	FB_D_CLK_P	GDDR3_80D	GDDR3_CLK	FB B CLK P<1>
		GDDR3_80D	GDDR3_CLK	FB B CLK N<1>
	FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB B MA<1..0>
	FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB B MA<11..6>
	FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB B BA<2..0>
	FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB B RAS_L
	FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB B CAS_L
	FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB B WE_L
	FB_CD_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB B CKE
	FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB B CS0_L
	FB_CD_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB B DRAM_RST
	FB_C_CMD	GDDR3_50SE	GDDR3_CMD	FB B LMA<5..2>
	FB_D_CMD	GDDR3_50SE	GDDR3_CMD	FB B UMA<5..2>
	FB_C_WDQS0	GDDR3_50SE	GDDR3_QDS	FB B WDQS<0>
	FB_C_WDQS1	GDDR3_50SE	GDDR3_QDS	FB B WDQS<1>
	FB_C_WDQS2	GDDR3_50SE	GDDR3_QDS	FB B WDQS<2>
	FB_C_WDQS3	GDDR3_50SE	GDDR3_QDS	FB B WDQS<3>
	FB_C_RDQS0	GDDR3_50SE	GDDR3_QDS	FB B RDQS<0>
	FB_C_RDQS1	GDDR3_50SE	GDDR3_QDS	FB B RDQS<1>
	FB_C_RDQS2	GDDR3_50SE	GDDR3_QDS	FB B RDQS<2>
	FB_C_RDQS3	GDDR3_50SE	GDDR3_QDS	FB B RDQS<3>
	FB_C_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB B DQ<7..0>
	FB_C_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB B DQ<15..8>
	FB_C_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB B DQ<23..16>
	FB_C_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB B DQ<31..24>
	FB_C_DQM0	GDDR3_50SE	GDDR3_DATA	FB B DQM_L<0>
	FB_C_DQM1	GDDR3_50SE	GDDR3_DATA	FB B DQM_L<1>
	FB_C_DQM2	GDDR3_50SE	GDDR3_DATA	FB B DQM_L<2>
	FB_C_DQM3	GDDR3_50SE	GDDR3_DATA	FB B DQM_L<3>
	FB_D_WDQS0	GDDR3_50SE	GDDR3_QDS	FB B WDQS<4>
	FB_D_WDQS1	GDDR3_50SE	GDDR3_QDS	FB B WDQS<5>
	FB_D_WDQS2	GDDR3_50SE	GDDR3_QDS	FB B WDQS<6>
	FB_D_WDQS3	GDDR3_50SE	GDDR3_QDS	FB B WDQS<7>
	FB_D_RDQS0	GDDR3_50SE	GDDR3_QDS	FB B RDQS<4>
	FB_D_RDQS1	GDDR3_50SE	GDDR3_QDS	FB B RDQS<5>
	FB_D_RDQS2	GDDR3_50SE	GDDR3_QDS	FB B RDQS<6>
	FB_D_RDQS3	GDDR3_50SE	GDDR3_QDS	FB B RDQS<7>
	FB_D_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB B DQ<39..32>
	FB_D_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB B DQ<47..40>
	FB_D_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB B DQ<55..48>
	FB_D_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB B DQ<63..56>
	FB_D_DQM0	GDDR3_50SE	GDDR3_DATA	FB B DQM_L<4>
	FB_D_DQM1	GDDR3_50SE	GDDR3_DATA	FB B DQM_L<5>
	FB_D_DQM2	GDDR3_50SE	GDDR3_DATA	FB B DQM_L<6>
	FB_D_DQM3	GDDR3_50SE	GDDR3_DATA	FB B DQM_L<7>

G84M Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	(CK505_DOT96)	CLK_SLOW_55S	CLK_SLOW	GPU CLK27M	30
		CLK_SLOW_55S	CLK_SLOW	GPU CLK27M_GATED	30 74
	CK505_CLK27MSS	CLK_SLOW_55S	CLK_SLOW	GPU CLK27M_SS	30
		CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS_GATED	30 74
		LVDS_100D	LVDS	LVDS_L_CLK_P	7 75 79
		LVDS_100D	LVDS	LVDS_L_CLK_N	75 79
		LVDS_100D	LVDS	LVDS_L_DATA_P<3..0>	7 74 75 79
		LVDS_100D	LVDS	LVDS_L_DATA_N<3..0>	74 75 79
		LVDS_100D	LVDS	LVDS_U_CLK_P	75 79
		LVDS_100D	LVDS	LVDS_U_CLK_N	75 79
		LVDS_100D	LVDS	LVDS_U_DATA_P<3..0>	74 75 79
		LVDS_100D	LVDS	LVDS_U_DATA_N<3..0>	74 75 79
	TMDS_CLK	TMDS_100D	TMDS	TMDS_CLK_P	75 78
	TMDS_CLK	TMDS_100D	TMDS	TMDS_CLK_N	75 78
	TMDS_DATA	TMDS_100D	TMDS	TMDS_DATA_P<5..0>	75 78
	TMDS_DATA	TMDS_100D	TMDS	TMDS_DATA_N<5..0>	75 78
	VGA_R_TV_C	VGA_50S	VGA	GPU_TV_C_VGA_R	74 78
	VGA_G_TV_Y	VGA_50S	VGA	GPU_TV_Y_VGA_G	74 78
	VGA_R_TV_COMP	VGA_50S	VGA	GPU_TV_COMP_VGA_B	74 78
		VGA_50S	VGA	GPU_VGA_R	74 75
		VGA_50S	VGA	GPU_VGA_G	74 75
		VGA_50S	VGA	GPU_VGA_B	74 75
		VGA_50S	VGA	GPU_TV_C	74 75
		VGA_50S	VGA	GPU_TV_Y	74 75
		VGA_50S	VGA	GPU_TV_COMP	74 75
	VGA_SYNC	VGA_55S	VGA_SYNC	GPU_VGA_HSYNC	75 78
	VGA_SYNC	VGA_55S	VGA_SYNC	GPU_VGA_VSYNC	75 78

GPU (G84M) Constraints

SYNC_MASTER=M75_MLB	SYNC_DATE=01/26/2007
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M75/M76 Board-Specific Spacing & Physical Constraints															
BOARD LAYERS								BOARD AREAS				BOARD UNITS (MIL OR MM)		ALLEGRO VERSION	
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM								NO_TYPE, BGA				MM		15.5.1	
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT	
DEFAULT		*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM		DEFAULT		*	0.1 MM	?	
STANDARD		*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT		STANDARD		*	=DEFAULT	?	
BGA_P1MM		*								BGA_P1MM		*	=DEFAULT	?	
BGA_P2MM		*								BGA_P2MM		*	=DEFAULT	?	
BGA_P3MM		*								BGA_P3MM		*	=DEFAULT	?	
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT	
55_OHM_SE		TOP, BOTTOM	Y	0.100 MM	0.100 MM					1.5:1_SPACING		*	0.15 MM	?	
55_OHM_SE		ISL2, ISL11	Y	0.250 MM	0.076 MM					1.8:1_SPACING		*	0.18 MM	?	
55_OHM_SE		*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD		2:1_SPACING		*	0.2 MM	?	
55_OHM_SE		*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD		2.5:1_SPACING		*	0.25 MM	?	
55_OHM_SE		*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD		3:1_SPACING		*	0.3 MM	?	
55_OHM_SE		*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD		4:1_SPACING		*	0.4 MM	?	
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT	
50_OHM_SE		TOP, BOTTOM	Y	0.125 MM	0.125 MM					1.5:1_SPACING		*	0.15 MM	?	
50_OHM_SE		*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD		1.8:1_SPACING		*	0.18 MM	?	
50_OHM_SE		*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD		2:1_SPACING		*	0.2 MM	?	
50_OHM_SE		*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD		2.5:1_SPACING		*	0.25 MM	?	
50_OHM_SE		*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD		3:1_SPACING		*	0.3 MM	?	
50_OHM_SE		*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD		4:1_SPACING		*	0.4 MM	?	
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT	
45_OHM_SE		TOP, BOTTOM	Y	0.150 MM	0.150 MM					1.5:1_SPACING		*	0.15 MM	?	
45_OHM_SE		*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD		1.8:1_SPACING		*	0.18 MM	?	
45_OHM_SE		*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD		2:1_SPACING		*	0.2 MM	?	
45_OHM_SE		*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD		2.5:1_SPACING		*	0.25 MM	?	
45_OHM_SE		*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD		3:1_SPACING		*	0.3 MM	?	
45_OHM_SE		*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD		4:1_SPACING		*	0.4 MM	?	
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT	
40_OHM_SE		TOP, BOTTOM	Y	0.185 MM	0.185 MM					1.5:1_SPACING		*	0.15 MM	?	
40_OHM_SE		*	Y	0.131 MM	0.131 MM	=STANDARD	=STANDARD	=STANDARD		1.8:1_SPACING		*	0.18 MM	?	
40_OHM_SE		*	Y	0.131 MM	0.131 MM	=STANDARD	=STANDARD	=STANDARD		2:1_SPACING		*	0.2 MM	?	
40_OHM_SE		*	Y	0.131 MM	0.131 MM	=STANDARD	=STANDARD	=STANDARD		2.5:1_SPACING		*	0.25 MM	?	
40_OHM_SE		*	Y	0.131 MM	0.131 MM	=STANDARD	=STANDARD	=STANDARD		3:1_SPACING		*	0.3 MM	?	
40_OHM_SE		*	Y	0.131 MM	0.131 MM	=STANDARD	=STANDARD	=STANDARD		4:1_SPACING		*	0.4 MM	?	
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT	
27P4_OHM_SE		TOP, BOTTOM	Y	0.335 MM	0.335 MM					1.5:1_SPACING		*	0.15 MM	?	
27P4_OHM_SE		*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD		1.8:1_SPACING		*	0.18 MM	?	
27P4_OHM_SE		*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD		2:1_SPACING		*	0.2 MM	?	
27P4_OHM_SE		*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD		2.5:1_SPACING		*	0.25 MM	?	
27P4_OHM_SE		*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD		3:1_SPACING		*	0.3 MM	?	
27P4_OHM_SE		*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD		4:1_SPACING		*	0.4 MM	?	
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT	
70_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD		1.5:1_SPACING		*	0.15 MM	?	
70_OHM_DIFF		ISL3, ISL4	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM		1.8:1_SPACING		*	0.18 MM	?	
70_OHM_DIFF		ISL9, ISL10	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM		2:1_SPACING		*	0.2 MM	?	
70_OHM_DIFF		ISL2, ISL11	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM		2.5:1_SPACING		*	0.25 MM	?	
70_OHM_DIFF		TOP, BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM		3:1_SPACING		*	0.3 MM	?	
70_OHM_DIFF		TOP, BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM		4:1_SPACING		*	0.4 MM	?	
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT	
80_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD		1.5:1_SPACING		*	0.15 MM	?	
80_OHM_DIFF		ISL3, ISL4	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM		1.8:1_SPACING		*	0.18 MM	?	
80_OHM_DIFF		ISL9, ISL10	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM		2:1_SPACING		*	0.2 MM	?	
80_OHM_DIFF		ISL2, ISL11	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM		2.5:1_SPACING		*	0.25 MM	?	
80_OHM_DIFF		TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM		3:1_SPACING		*	0.3 MM	?	
80_OHM_DIFF		TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM		4:1_SPACING		*	0.4 MM	?	
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT	
85_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD		1.5:1_SPACING		*	0.15 MM	?	
85_OHM_DIFF		ISL3, ISL4	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM		1.8:1_SPACING		*	0.18 MM	?	
85_OHM_DIFF		ISL9, ISL10	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM		2:1_SPACING		*	0.2 MM	?	
85_OHM_DIFF		ISL2, ISL11	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM		2.5:1_SPACING		*	0.25 MM	?	
85_OHM_DIFF		TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM		3:1_SPACING		*	0.3 MM	?	
85_OHM_DIFF		TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM		4:1_SPACING		*	0.4 MM	?	
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT	
90_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD		1.5:1_SPACING		*	0.15 MM	?	
90_OHM_DIFF		ISL3, ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM		1.8:1_SPACING		*	0.18 MM	?	
90_OHM_DIFF		ISL9, ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM		2:1_SPACING		*	0.2 MM	?	
90_OHM_DIFF		ISL2, ISL11	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM		2.5:1_SPACING		*	0.25 MM	?	
90_OHM_DIFF		TOP, BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM		3:1_SPACING		*	0.3 MM	?	
90_OHM_DIFF		TOP, BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM		4:1_SPACING		*	0.4 MM	?	
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT	
100_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD		1.5:1_SPACING		*	0.15 MM	?	
100_OHM_DIFF		ISL3, ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM		1.8:1_SPACING		*	0.18 MM	?	
100_OHM_DIFF		ISL9, ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM		2:1_SPACING		*	0.2 MM	?	
100_OHM_DIFF		ISL2, ISL11	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM		2.5:1_SPACING		*	0.25 MM	?	
100_OHM_DIFF		TOP, BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM		3:1_SPACING		*	0.3 MM	?	
100_OHM_DIFF		TOP, BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM		4:1_SPACING		*	0.4 MM	?	
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT	
110_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD		1.5:1_SPACING		*	0.15 MM	?	
110_OHM_DIFF		ISL3, ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM		1.8:1_SPACING		*	0.18 MM	?	
110_OHM_DIFF		ISL9, ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM		2:1_SPACING		*	0.2 MM	?	
110_OHM_DIFF		ISL2, ISL11	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM		2.5:1_SPACING		*	0.25 MM	?	
110_OHM_DIFF		TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM		3:1_SPACING		*	0.3 MM	?	
110_OHM_DIFF		TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM		4:1_SPACING		*	0.4 MM	?	
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT	
100_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD		1.5:1_SPACING		*	0.15 MM	?	
100_OHM_DIFF		ISL3, ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM		1.8:1_SPACING		*	0.18 MM	?	
100_OHM_DIFF		ISL9, ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM		2:1_SPACING		*	0.2 MM	?	
100_OHM_DIFF		ISL2, ISL11	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM		2.5:1_SPACING		*	0.25 MM	?	
100_OHM_DIFF		TOP, BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM		3:1_SPACING		*	0.3 MM	?	
100_OHM_DIFF		TOP, BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM		4:1_SPACING		*	0.4 MM	?	
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT	
100_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD		1.5:1_SPACING		*	0.15 MM	?	
100_OHM_DIFF		ISL3, ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM		1.8:1_SPACING		*	0.18 MM	?	
100_OHM_DIFF		ISL9, ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM		2:1_SPACING		*	0.2 MM	?	
100_OHM_DIFF		ISL2, ISL11	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM		2.5:1_SPACING		*	0.25 MM	?	
100_OHM_DIFF		TOP, BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM		3:1_SPACING		*	0.3 MM	?	
100_OHM_DIFF		TOP, BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM		4:1_SPACING		*	0.4 MM	?	
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT	
110_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD		1.5:1_SPACING		*	0.15 MM	?	
110_OHM_DIFF		ISL3, ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM		1.8:1_SPACING		*	0.18 MM	?	
110_OHM_DIFF		ISL9, ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM		2:1_SPACING		*	0.2 MM	?	
110_OHM_DIFF		ISL2, ISL11	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM		2.5:1_SPACING		*	0.25 MM	?	
110_OHM_DIFF		TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM		3:1_SPACING		*	0.3 MM	?	
110_OHM_DIFF		TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM		4:1_SPACING		*	0.4 MM	?	
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT	
100_OHM_DIFF		*	N	=STANDARD	=STANDARD										