

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM, MLB-PRQ, M59

02/12/2007

## BOM Update for Post Ramp Qualifications

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
B		486797	PRODUCTION RELEASED	02/12/07	



Page	Contents	Sync	Date
1	Table of Contents	N/A	N/A
2	System Block Diagram	N/A	N/A
3	Power Block Diagram	N/A	N/A
4	BOM Configuration	N/A	N/A
5	Functional / ICT Test	N/A	N/A
6	Signal Aliases/Misc Comps	N/A	N/A
7	CPU 1 OF 2-FSB	(MASTER)	(MASTER)
8	CPU 2 OF 2-PWR/GND	(MASTER)	(MASTER)
9	CPU Decoupling & VID	(MASTER)	(MASTER)
10	CPU MISC1-TEMP SENSOR	(MASTER)	(MASTER)
11	CPU ITP700FLEX DEBUG	(MASTER)	(MASTER)
12	NB CPU Interface	(MASTER)	(MASTER)
13	NB PEG / Video Interfaces	(MASTER)	(MASTER)
14	NB Misc Interfaces	(MASTER)	(MASTER)
15	NB DDR2 Interfaces	(MASTER)	(MASTER)
16	NB Power 1	(MASTER)	(MASTER)
17	NB Power 2	(MASTER)	(MASTER)
18	NB Grounds	(MASTER)	(MASTER)
19	NB (GM) Decoupling	M59_MG	07/25/2006
20	NB Config Straps	(MASTER)	(MASTER)
21	SB: 1 OF 4	(MASTER)	(MASTER)
22	SB: 2 of 4	(MASTER)	(MASTER)
23	SB: 3 OF 4	M59_MG	07/25/2006
24	SB: 4 OF 4	(MASTER)	(MASTER)
25	SB Decoupling	(MASTER)	(MASTER)
26	SB Misc	(MASTER)	(MASTER)
27	M1 SMBus Connections	(MASTER)	(MASTER)
28	DDR2 SO-DIMM Connector A	(MASTER)	(MASTER)
29	DDR2 SO-DIMM Connector B	(MASTER)	(MASTER)
30	Memory Active Termination	(MASTER)	(MASTER)
31	Memory Vtt Supply	(MASTER)	(MASTER)
32	DDR2 VRef	(MASTER)	(MASTER)
33	CLOCKS	(MASTER)	(MASTER)
34	Clock Termination	M59_MG	05/07/2006
35	Mobile Clocking	(MASTER)	(MASTER)
36	PATA Connector	(MASTER)	(MASTER)
37	FireWire Link (TSB83AA22)	(MASTER)	(MASTER)
38	FireWire PHY (TSB83AA22)	(MASTER)	(MASTER)
39	ETHERNET CONTROLLER	(MASTER)	(MASTER)
40	Ethernet Connector	(MASTER)	(MASTER)
41	Yukon Power Control	(MASTER)	(MASTER)

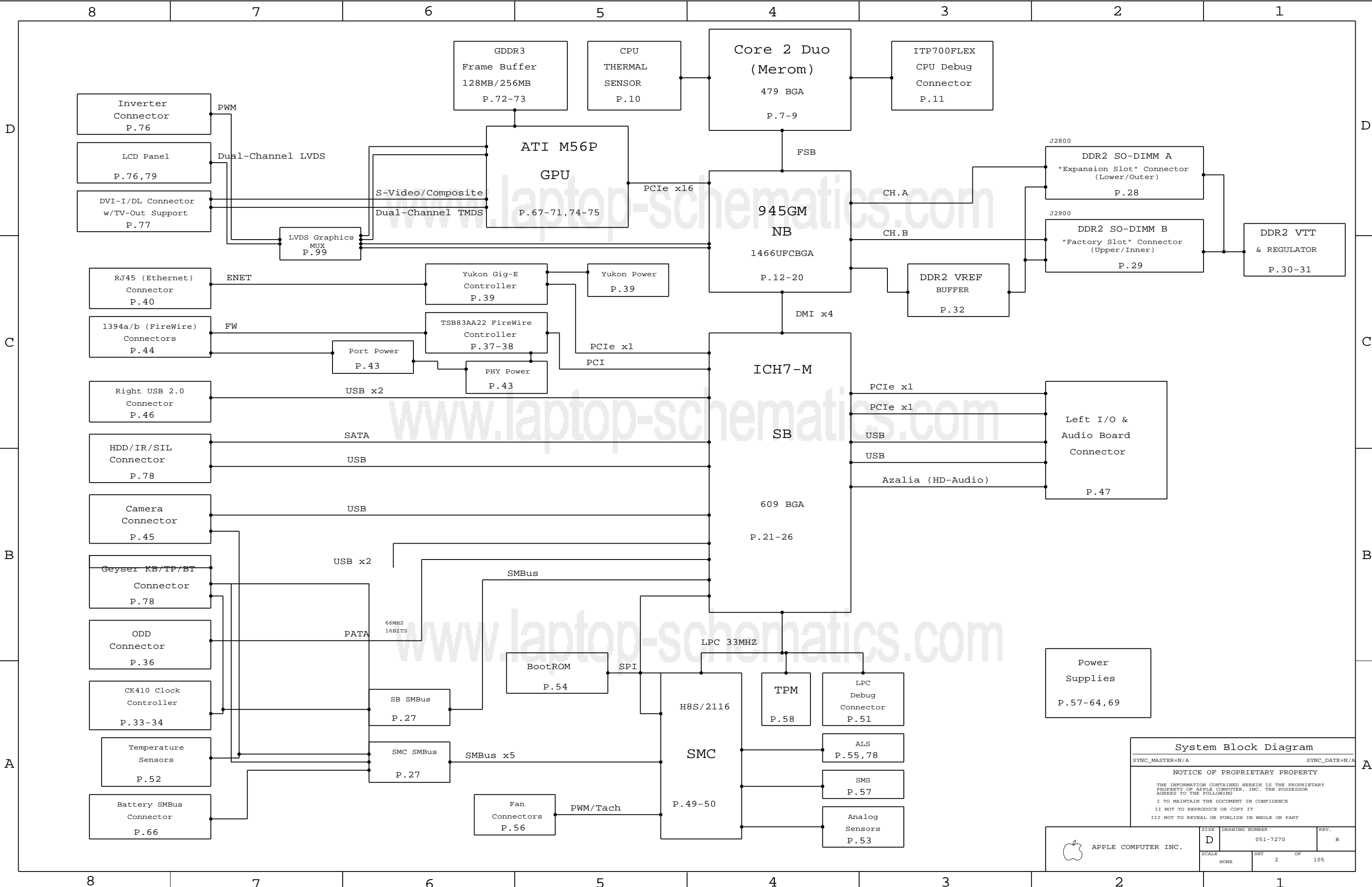
Page	Contents	Sync	Date
42	FW PHY Power Supply	(MASTER)	(MASTER)
43	FireWire Port Power	(MASTER)	(MASTER)
44	FireWire Ports	(MASTER)	(MASTER)
45	Camera Connector	(MASTER)	(MASTER)
46	External USB Connector	(MASTER)	(MASTER)
47	Left I/O Board Connector	(MASTER)	(MASTER)
48	PCI-E Connections	(MASTER)	(MASTER)
49	SMC	(MASTER)	(MASTER)
50	SMC Support	(MASTER)	(MASTER)
51	LPC+ Debug Connector	(MASTER)	(MASTER)
52	Thermal Sensors	(MASTER)	(MASTER)
53	Current & Voltage Sensing	(MASTER)	(MASTER)
54	SPI BOOTROM	(MASTER)	(MASTER)
55	ALS Support	(MASTER)	(MASTER)
56	Fan Connectors	(MASTER)	(MASTER)
57	Sudden Motion Sensor (SMS)	(MASTER)	(MASTER)
58	TPM	(MASTER)	(MASTER)
59	IMVP6 CPU VCore Regulator	(MASTER)	(MASTER)
60	5V / 1.5V Power Supply	(MASTER)	(MASTER)
61	2.5V & 1.2V Regulators	M59_MG	05/07/2006
62	1.8V Supply	M59_MG	05/07/2006
63	3.3V / 1.05V Power Supplies	M59_MG	05/07/2006
64	3.3V G3Hot Supply & Power Control	M59_MG	08/01/2006
65	Power Aliases	M59_MG	05/07/2006
66	PBus-In,Batt. & 3G Pwr Connectors	(MASTER)	(MASTER)
67	ATI M56 PCI-E	(MASTER)	(MASTER)
68	GPU (M56) Core Supplies	(MASTER)	(MASTER)
69	ATI M56 Core Power	(MASTER)	(MASTER)
70	ATI M56 Frame Buffer I/F	(MASTER)	(MASTER)
71	GPU Straps	M59_MG	07/25/2006
72	GDDR3 Frame Buffer A	(MASTER)	(MASTER)
73	GDDR3 Frame Buffer B	(MASTER)	(MASTER)
74	ATI M56 GPIO/DVO/Misc	(MASTER)	(MASTER)
75	ATI M56 Video Interfaces	(MASTER)	(MASTER)
76	Internal Display Connectors	M59_MG	07/25/2006
77	External Display Connector	M59_MG	07/25/2006
78	M59 Specific Connectors	(MASTER)	(MASTER)
79	LVDS Interface Pull-downs	M59_MG	08/01/2006
80	Revision History	N/A	N/A
81	Napa Platform Constraints	(MASTER)	(MASTER)
82	More System Constraints	(MASTER)	(MASTER)
83	M59 Spacing & Physical Constraints	(MASTER)	(MASTER)
84	M59 Net Properties	(MASTER)	(MASTER)
85	22uF Capacitor BOM Configuration	N/A	N/A

## Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7270	1	SCHEM,MLB-PRQ,M59	SCH	CRITICAL	
820-2054	1	PCBF,MLB,M59	PCB	CRITICAL	

DRAWING  
TITLE=M59\_MLB  
ABBREV=DRAWING  
LAST\_MODIFIED=Mon Feb 12 10:35:04 2007

<div>DIMENSIONS ARE IN MILLIMETERS</div> <div>XX ± _____</div> <div>X.XX ± _____</div> <div>X.XXX ± _____</div> <div>ANGLES ± _____</div> <div>DO NOT SCALE DRAWING</div>	<div>METRIC</div>				<div> Apple Computer Inc.</div>			
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	<div>DRAFTER</div>	<div>/</div>	<div>DESIGN CK</div>	<div>/</div>	<div>TITLE</div> <div>SCHEM,MLB-PRQ,M59</div>			
	<div>ENG APPD</div>	<div>/</div>	<div>MFG APPD</div>	<div>/</div>				
<div>QA APPD</div>	<div>/</div>	<div>DESIGNER</div>	<div>/</div>					
<div></div> <div>THIRD ANGLE PROJECTION</div>	<div>RELEASE</div>	<div>/</div>	<div>SCALE</div> <div>NONE</div>		<div>DRAWING NUMBER</div> <div>051-7270</div>			<div>REV.</div> <div>B</div>
	<div>MATERIAL/FINISH NOTED AS APPLICABLE</div>		<div>SIZE</div> <div>D</div>		<div>SHEET 1 OF 105</div>			



**System Block Diagram**

SYNC\_MASTER=N/A SYNC\_DATE=N/A

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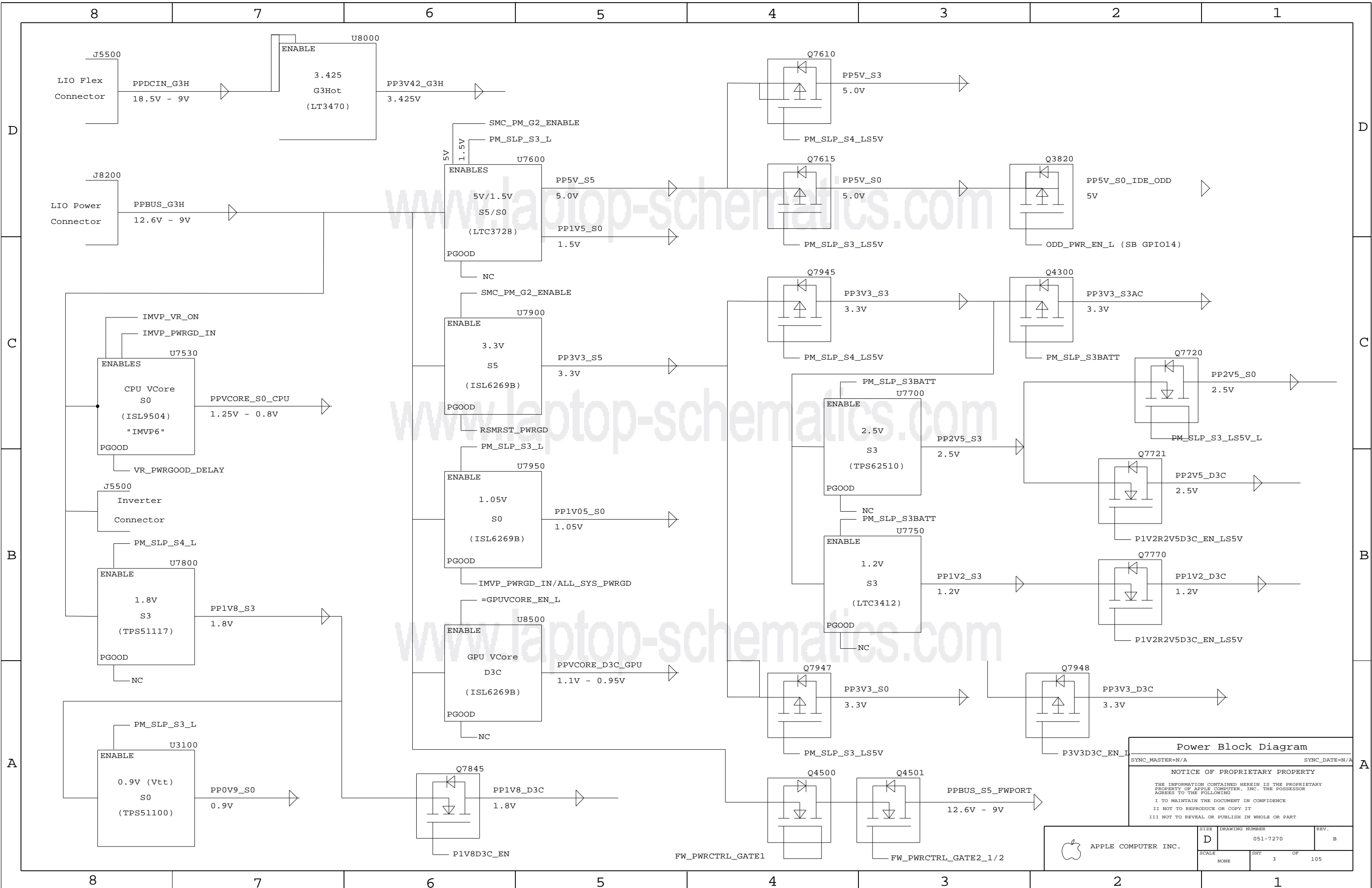
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

















































APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7270	REV. B
	SCALE NONE	SHT 2	OF 105



8		7		6		5		4		3		2		1	
Original Production BOMs (SS VRAM, All SS/MU Caps)															
BOM NUMBER		BOM NAME				BOM OPTIONS									
630-7849		PCBA, 2.16, 128VR-SS, SAM-CAP, M59, MBP15				EEE_WTE, M59_COMMON, CPU_2_16GHZ, VRAM_SAM128, CAP22UF_ALLSAM, ODD_NONLOCK_CONN									
630-7919		PCBA, 2.16, 128VR-SS, MUR-CAP, M59, MBP15				EEE_X34, M59_COMMON, CPU_2_16GHZ, VRAM_SAM128, CAP22UF_ALLMURA, ODD_NONLOCK_CONN									
630-7851		PCBA, 2.33, 256VR-SS, SAM-CAP, M59, MBP15				EEE_WTG, M59_COMMON, CPU_2_33GHZ, VRAM_SAM256, CAP22UF_ALLSAM, ODD_NONLOCK_CONN									
630-7920		PCBA, 2.33, 256VR-SS, MUR-CAP, M59, MBP15				EEE_X35, M59_COMMON, CPU_2_33GHZ, VRAM_SAM256, CAP22UF_ALLMURA, ODD_NONLOCK_CONN									
Mixed Cap BOMs															
BOM NUMBER		BOM NAME				BOM OPTIONS									
630-7964		PCBA, 2.16, 128VR-SS, SAM_TYO-CAP, M59, MBP15				EEE_XAC, M59_COMMON, CPU_2_16GHZ, VRAM_SAM128, CAP22UF_MIXSAM, ODD_NONLOCK_CONN									
630-7965		PCBA, 2.16, 128VR-SS, MUR_TYO-CAP, M59, MBP15				EEE_XAD, M59_COMMON, CPU_2_16GHZ, VRAM_SAM128, CAP22UF_MIXMURA, ODD_NONLOCK_CONN									
630-7966		PCBA, 2.33, 256VR-SS, SAM_TYO-CAP, M59, MBP15				EEE_XAE, M59_COMMON, CPU_2_33GHZ, VRAM_SAM256, CAP22UF_MIXSAM, ODD_NONLOCK_CONN									
630-7967		PCBA, 2.33, 256VR-SS, MUR_TYO-CAP, M59, MBP15				EEE_XAF, M59_COMMON, CPU_2_33GHZ, VRAM_SAM256, CAP22UF_MIXMURA, ODD_NONLOCK_CONN									
Qimonda (Infineon) VRAM BOMs															
BOM NUMBER		BOM NAME				BOM OPTIONS									
630-7982		PCBA, 2.16, 128VR-QM, SS-CAP, M59, MBP15				EEE_XBU, M59_COMMON, CPU_2_16GHZ, VRAM_INF128, CAP22UF_ALLSAM, ODD_NONLOCK_CONN									
630-7983		PCBA, 2.16, 128VR-QM, MU-CAP, M59, MBP15				EEE_XBV, M59_COMMON, CPU_2_16GHZ, VRAM_INF128, CAP22UF_ALLMURA, ODD_NONLOCK_CONN									
630-7984		PCBA, 2.33, 256VR-QM, SS-CAP, M59, MBP15				EEE_XBW, M59_COMMON, CPU_2_33GHZ, VRAM_INF256, CAP22UF_ALLSAM, ODD_NONLOCK_CONN									
630-7985		PCBA, 2.33, 256VR-QM, MU-CAP, M59, MBP15				EEE_XBX, M59_COMMON, CPU_2_33GHZ, VRAM_INF256, CAP22UF_ALLMURA, ODD_NONLOCK_CONN									
630-7986		PCBA, 2.16, 128VR-QM, SS_TY-CAP, M59, MBP15				EEE_XBY, M59_COMMON, CPU_2_16GHZ, VRAM_INF128, CAP22UF_MIXSAM, ODD_NONLOCK_CONN									
630-7987		PCBA, 2.16, 128VR-QM, MU_TY-CAP, M59, MBP15				EEE_XBZ, M59_COMMON, CPU_2_33GHZ, VRAM_INF128, CAP22UF_MIXMURA, ODD_NONLOCK_CONN									
630-7988		PCBA, 2.33, 256VR-QM, SS_TY-CAP, M59, MBP15				EEE_XC0, M59_COMMON, CPU_2_33GHZ, VRAM_INF256, CAP22UF_MIXSAM, ODD_NONLOCK_CONN									
630-7989		PCBA, 2.33, 256VR-QM, MU_TY-CAP, M59, MBP15				EEE_XC1, M59_COMMON, CPU_2_33GHZ, VRAM_INF256, CAP22UF_MIXMURA, ODD_NONLOCK_CONN									
Bar Code Label / EEE #'s															
PART NUMBER		QTY	DESCRIPTION			REFERENCE DES		CRITICAL	BOM OPTION						
826-4393		1	LBL, P/N LABEL, PCB, 28MM X 6 MM			[EEE:WTE]		CRITICAL	EEE_WTE						
826-4393		1	LBL, P/N LABEL, PCB, 28MM X 6 MM			[EEE:WTG]		CRITICAL	EEE_WTG						
826-4393		1	LBL, P/N LABEL, PCB, 28MM X 6 MM			[EEE:X34]		CRITICAL	EEE_X34						
826-4393		1	LBL, P/N LABEL, PCB, 28MM X 6 MM			[EEE:X35]		CRITICAL	EEE_X35						
826-4393		1	LBL, P/N LABEL, PCB, 28MM X 6 MM			[EEE:XAC]		CRITICAL	EEE_XAC						
826-4393		1	LBL, P/N LABEL, PCB, 28MM X 6 MM			[EEE:XAD]		CRITICAL	EEE_XAD						
826-4393		1	LBL, P/N LABEL, PCB, 28MM X 6 MM			[EEE:XAE]		CRITICAL	EEE_XAE						
826-4393		1	LBL, P/N LABEL, PCB, 28MM X 6 MM			[EEE:XAF]		CRITICAL	EEE_XAF						
826-4393		1	LBL, P/N LABEL, PCB, 28MM X 6 MM			[EEE:XBU]		CRITICAL	EEE_XBU						
826-4393		1	LBL, P/N LABEL, PCB, 28MM X 6 MM			[EEE:XBV]		CRITICAL	EEE_XBV						
826-4393		1	LBL, P/N LABEL, PCB, 28MM X 6 MM			[EEE:XBW]		CRITICAL	EEE_XBW						
826-4393		1	LBL, P/N LABEL, PCB, 28MM X 6 MM			[EEE:XBX]		CRITICAL	EEE_XBX						
826-4393		1	LBL, P/N LABEL, PCB, 28MM X 6 MM			[EEE:XBY]		CRITICAL	EEE_XBY						
826-4393		1	LBL, P/N LABEL, PCB, 28MM X 6 MM			[EEE:XBZ]		CRITICAL	EEE_XBZ						
826-4393		1	LBL, P/N LABEL, PCB, 28MM X 6 MM			[EEE:XC0]		CRITICAL	EEE_XC0						
826-4393		1	LBL, P/N LABEL, PCB, 28MM X 6 MM			[EEE:XC1]		CRITICAL	EEE_XC1						
BOMOPTION Groups															
BOM GROUP		BOM OPTIONS													
M59_COMMON		ALTERNATE, COMMON, M59_COMMON1, M59_COMMON2, M59_COMMON3													
M59_COMMON1		BOOTROM_FINAL, ENET_LOW_PWR_EN, ENETPWR_S3AC, GPU_BB_CTL, D3CPGOOD_3V3													
M59_COMMON2		ITP, KBDLED_HAS, LPCPLUS, LVDS_PD, MEMVREF_S3													
M59_COMMON3		MEMVTT_EN_PU, RTUSB_ESD, SMC_PRGRM, USB_C_OC_PU, USB_D_OC_PU, USB_E_OC_PU													
VRAM_INF128		GPU_MEM_NOT_SAM, VRAM_128_INFINEON													
VRAM_SAM128		VRAM_128_SAMSUNG													
VRAM_INF256		GPU_MEM_256M, GPU_MEM_NOT_SAM, VRAM_256_INFINEON													
VRAM_SAM256		GPU_MEM_256M, VRAM_256_SAMSUNG													
M59_TPM		TPM													
CAP22UF_ALLSAM		CAP22UF_SAM, CAP22UF_SAM_CRIT													
CAP22UF_ALLMURA		CAP22UF_MURA, CAP22UF_MURA_CRIT													
CAP22UF_MIXSAM		CAP22UF_TAIYO, CAP22UF_SAM_CRIT													
CAP22UF_MIXMURA		CAP22UF_TAIYO, CAP22UF_MURA_CRIT													
Module Parts															
PART NUMBER		QTY	DESCRIPTION			REFERENCE DES		CRITICAL	BOM OPTION						
333S0354		4	IC, SDRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA			U8900, U8950, U9000, U9050		CRITICAL	VRAM_128_SAMSUNG						
333S0350		4	IC, SDRAM, GDDR3, 16MX32, 700MHZ, 136 FBGA			U8900, U8950, U9000, U9050		CRITICAL	VRAM_256_SAMSUNG						
333S0358		4	IC, SDRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA			U8900, U8950, U9000, U9050		CRITICAL	VRAM_128_HYNIX						
333S0351		4	IC, SDRAM, GDDR3, 16MX32, 700MHZ, 136 FBGA			U8900, U8950, U9000, U9050		CRITICAL	VRAM_256_HYNIX						
333S0376		4	IC, SDRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA			U8900, U8950, U9000, U9050		CRITICAL	VRAM_128_INFINEON						
333S0377		4	IC, SDRAM, GDDR3, 16MX32, 600MHZ, 136 FBGA			U8900, U8950, U9000, U9050		CRITICAL	VRAM_256_INFINEON						
337S3391		1	IC, MDC, B2, PRQ, 2.16G, 34W, 667M, 4M, 479BGA			U0700		CRITICAL	CPU_2_16GHZ						
337S3393		1	IC, MDC, B2, PRQ, 2.33G, 34W, 667M, 4M, 479BGA			U0700		CRITICAL	CPU_2_33GHZ						
341S1922		1	IC, EFI, BOOTROM DEVELOPMENT (UNLOCKED), M59			U6301		CRITICAL	BOOTROM_DEVEL						
341S2006		1	IC, EFI, BOOTROM FINAL (LOCKED), M59			U6301		CRITICAL	BOOTROM_FINAL						
338S0274		1	IC, SMC, M58/2116			U5800		CRITICAL	SMC_BLANK						
341S1929		1	IC, PRGRM, SMC (NEW), M59			U5800		CRITICAL	SMC_PRGRM						
338S0269		1	IC, 945GM, NORTHBRIDGE			U1200		CRITICAL							
338S0270		1	IC, 888S053, GIGABIT ENET XCVR, 64P QFN, WQ			U4101		CRITICAL							
338S0368		1	IC, ATI, M561-LLP, GRAPHICRTL, LP 880BGA			U8400		CRITICAL							
341S1789		1	IC, TPM, 28-PIN TSSOP			U6700		CRITICAL	TPM						
341S1797		1	IC, EEPROM, SERIAL IIC, 8KBIT, SO8			U4102		CRITICAL							
343S0385		1	IC, ICH7M, BGA			U2100		CRITICAL							
353S1461		1	IC, I2L9504, SYNC REG CTRL, QFN48			U7530		CRITICAL							
359S0109		1	LOW POWER CLOCK SYNTHESIZER, 68PIN			U3301		CRITICAL							
Alternate Parts															
PART NUMBER		ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:										
128S0094		128S0060		ALL	330uF, 2V, 9608M, D2										
128S0095		128S0060		ALL	330uF, 2V, 6008M, D2										
128S0081		128S0061		ALL	150uF, 6.3V, 2308M, C2										
376S0448		376S0445		ALL	SI7806ADM For FDM6286										
353S1465		353S1461		ALL	Screws for I2L9504										
152S0287		152S0435		ALL	Alternative for I2L9502 Memory										
128S0093		128S0092		ALL	33uF, 16V, D2										
157S0030		157S0011		ALL	TSM Ethernet XPM for EAE										
353S1381		353S1278		ALL	cda0002 for REP131 and other supply										
BOM Configuration															
SYNC_MASTER=N/A SYNC_DATE=N/A															
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 APPLE COMPUTER INC.			SIZE	DRAWING NUMBER				REV.							
			D	051-7270				B							
			SCALE		SHT		4		OF		105				
			NONE												

## Functional Test Points






## Power Supply NO\_TESTS

NO_TEST	EXPOSED_VIA	
	TRUE	IMVP6_RBIAS 59C7
	TRUE	IMVP6_COMP 59B7
	TRUE	P5V5S5_RUNSS 60C5 64A6
	TRUE	P1V5S0_RUNSS 5B7 60C4 64C6
	TRUE	P1V2S3_RT 61B6
	TRUE	P1V2S3_RUNSS 41C4 61B7
	TRUE	P3V3S5_COMP 5B7 63C6
	TRUE	P3V3S5_FSET 5B7 63D6
	TRUE	P1V05S0_COMP 5C7 63A7
	TRUE	P1V05S0_FSET 5B7 63B7
	TRUE	P3V42G3H_FB 64C3
	TRUE	GPUVCORE_COMP 68C7
	TRUE	GPUVCORE_FSET 68C7
	TRUE	GPUBBP_ADJ 68B7
	TRUE	GPUBBN_FB 68A3
	TRUE	GPUVCORE_FB 68C7
	TRUE	GPUVCORE_FB_RC 68C3
	TRUE	GPUVCORE_ISEN 68C5
	TRUE	GPUVCORE_LG 68C5
	TRUE	GPUVCORE_PHASE 68C5
	TRUE	GPUVCORE_UG 68D5
	TRUE	IMVP6_COMP_RC 59B8
	TRUE	IMVP6_DFB 59B6
	TRUE	IMVP6_FB 59B7
	TRUE	IMVP6_OCSET 59C6
	TRUE	IMVP6_VDIFF 59C7
	TRUE	IMVP6_VDIFF_RC 59B8
	TRUE	P1V05S0_BOOT 63B5
	TRUE	P1V05S0_BOOT_R 63B5
	TRUE	P1V05S0_COMP 5D7 63A7
	TRUE	P1V05S0_COMP_R 63A7
	TRUE	P1V05S0_FB 63A7
	TRUE	P1V05S0_FB_RC 63A3
	TRUE	P1V05S0_FSET 5D7 63B7
	TRUE	P1V05S0_ISEN 63A5
	TRUE	P1V05S0_LG 63A5
	TRUE	P1V05S0_PHASE 63B5
	TRUE	P1V05S0_UG 63B5
	TRUE	P1V5S0_RUNSS 5D7 60C4 64C6
	TRUE	P3V3S5_BOOT 63D4
	TRUE	P3V3S5_BOOT_R 63D4
	TRUE	P3V3S5_COMP 5D7 63C6
	TRUE	P3V3S5_COMP_R 63C6
	TRUE	P3V3S5_FB 63C6
	TRUE	P3V3S5_FB_RC 63C2
	TRUE	P3V3S5_FSET 5D7 63D6
	TRUE	P3V3S5_ISEN 63C4
	TRUE	P3V3S5_LG 63C4
	TRUE	P3V3S5_UG 63D4
	TRUE	CK410_XTAL_IN 33C6





## CPU FSB NO\_TESTS

NO_TEST	EXPOSED_VIA		
		FSB A L<31..3>	708 708 1204 1204 1204 8406
		FSB ADS L	706 1204 8406
	TRUE	FSB ADSTB L<1..0>	708 708 1204 8406
		FSB BNR L	706 1204 8406
		FSB BREQ0 L	706 1204 8406
		FSB D L<63..0>	783 784 703 704 1286 1206 1206 8406
		FSB DBSY L	706 1284 8406
	TRUE	FSB DINV L<3..0>	783 784 703 704 1284 8406
		FSB DRDY L	706 1284 8406
	TRUE	FSB DSTBN L<3..0>	783 784 703 704 1284 8406
	TRUE	FSB DSTBP L<3..0>	783 784 703 704 1284 8406
		FSB HIT L	706 1284 8406
		FSB HITM L	706 1284 8406
		FSB LOCK L	706 1284 8406
		FSB REQ L<4..0>	708 1244 1284 8406

## Fan Connectors

FUNC_TEST		
	TRUE	=PP5V S0 FAN LT 56C7 65A1
	TRUE	FAN LT PWM 56B6
	TRUE	FAN LT TACH 56B6
	TRUE	FAN RT PWM 56B3
	TRUE	FAN RT TACH 56B3

## Battery Digital Connector

FUNC_TEST			
	TRUE	SMC BS ALERT L	49CS 50B2 66B5
	TRUE	=SMBUS BATT_SCL	27C1 66B5
	TRUE	=SMBUS BATT_SDA	27C1 66B5
	TRUE	GND_BATT	66B5





## Left I/O Data Connector

FUNC_TEST		
	TRUE	=PP1V5_S0_LIO 4706 6506
	TRUE	=PPDCIN_G3H_LIO 4706 6508
	TRUE	=PP5V_S5_LIO 4706 6581
	TRUE	=PP3V42_G3H_LIO 4706 6503
C6	TRUE	PP5V_S0_AUDIO_PWR 4704
	TRUE	PP5V_S0_AUDIO 4704
C6	TRUE	GND_AUDIO_PWR 4744
	TRUE	GND_AUDIO 4744
	TRUE	ACZ_SDATAIN<0> 2107 4786 8484
	TRUE	ACZ_SDATACOUT 2107 4786 8484
	TRUE	ACZ_BITCLK 2107 4786 8484
	TRUE	ACZ_RST_L 2107 4783 8484
	TRUE	EXCARD_OC_L 603 4706 5083
	TRUE	LTUSB_OC_L 603 4706
B3	TRUE	LIO_BATT_ISENSE 4706 5303
	TRUE	SMC_SYS_ISET 4706 4985
	TRUE	SMC_BATT_ISET 4786 4985
C6	TRUE	SMC_BATT_CHG_EN 4706 4907 50A2
C6	TRUE	SMC_BC_ACOK 4786 4905 50A2
	TRUE	SMC_ADAPTER_EN 4387 4706 4905
B5	TRUE	LIO_P3V3S0_EN_L 4786 6406
	TRUE	LIO_DCIN_ISENSE 4786 5305
	TRUE	LIO_P3V3S3_EN 4786 6406
	TRUE	SMC_BATT_TRICKLE_EN_L 4786 4907 50A2
	TRUE	SYS_ONEWIRE 4706 4987 50B2
	TRUE	MINI_CLKREQ_L 3443 4706
	TRUE	SMC_EXCARD_CP 4786 4987 50A2
	TRUE	EXCARD_CLKREQ_L 3443 4706
	TRUE	SMC_EXCARD_PWR_EN 4786 4987
	TRUE	LIO_PLT_RESET_L 2601 4706
	TRUE	ACZ_SYNC 2107 4786 8484
	TRUE	=USB2_LT_N 603 4703
	TRUE	=USB2_LT_P 603 4703
	TRUE	=USB2_EXCARD_N 603 4703
	TRUE	=PCIE2_EXCARD_P 603 4703
	TRUE	=PCIE_EXCARD_R2D_N 4783 4806
	TRUE	=PCIE_EXCARD_R2D_P 4783 4806
	TRUE	=PCIE_EXCARD_D2R_N 4783 4806
	TRUE	=PCIE_EXCARD_D2R_P 4783 4806
	TRUE	PCIE_CLK100M_EXCARD_P 3403 4783
	TRUE	PCIE_CLK100M_EXCARD_N 3483 4783
	TRUE	=PCIE_MINI_R2D_N 4783 4806
	TRUE	=PCIE_MINI_R2D_P 4783 4806
	TRUE	=PCIE_MINI_D2R_N 4703 4806
	TRUE	=PCIE_MINI_D2R_P 4703 4806
	TRUE	PCIE_CLK100M_MINI_P 3404 4703
	TRUE	PCIE_CLK100M_MINI_N 3404 4703
	TRUE	=SMBUS_LIO_SMC_SCL 2701 4703
	TRUE	=SMBUS_LIO_SMC_SDA 2701 4703
	TRUE	=SMBUS_LIO_SB_SCL 2786 4703
	TRUE	=SMBUS_LIO_SB_SDA 2786 4703
	TRUE	PCIE_WAKE_L 2308 3906 4703





## LPC+ Debug Connector

FUNC_TEST		
TRUE	=PP3V3 S5 LECPLUS	5104 6503
TRUE	=PP5V S0 LECPLUS	5104 6504
TRUE	LPC AD<0>	2104 49
TRUE	LPC AD<1>	2104 4907
TRUE	LPC FRAME L	2105 4907
TRUE	PM CLKRUN L	2108 4905
TRUE	BOOT LPC SPI L	2203 4907
TRUE	SMC TMS	4905 5082
TRUE	DEBUG_RST L	2601 5184
TRUE	SMC TRST L	4901 5184
TRUE	SMC TDO	4905 5082
TRUE	SMC MD1	4901 5184
TRUE	SMC TX L	4605 4907
TRUE	FWH INIT L	5184 5003
TRUE	PCI CLK_PORT80_LPC	3406 5105
TRUE	LPC AD<2>	2104 4907
TRUE	LPC AD<3>	2104 4907
TRUE	INT_SERIRQ	2108 4907
TRUE	PM_SUS_STAT L	2105 4905
TRUE	SMC TDI	4905 5082
TRUE	SMC TCK	4905 5082
TRUE	SMC_RST L	4903 5006
TRUE	SMC NMI	4901 5185
TRUE	SMC_RX L	4605 4907
TRUE	SV_SET UP	5185 2303

## Left ALS Connector

FUNC_TEST			
	TRUE	=PP3V3_S3_LTALS	6503 7803
	TRUE	ALS_GAIN	605 4995
	TRUE	LTALS_OUT	5507 7803
	TRUE	GND	

## Thermal Diode Connectors

FUNC_TEST		
	TRUE	HSTHMSNS_DX_P 5205
	TRUE	HSTHMSNS_DX_N 5205
	TRUE	RSFSTHMSNS_D_P 5205
	TRUE	RSFSTHMSNS_D_N 5205

## Other Func Test Points

FUNC_TEST			
TRUE	=PP1V05_S0_REG	53A4	63A
TRUE	PM_SYSRST_L	23C5	26C
TRUE	SMC_ONOFF_L	48C5	50B




## Current Sense Calibration

FUNC_TEST		
<input type="checkbox"/>	TRUE	ISENSE_CAL_EN 4987 53A
<input type="checkbox"/>	TRUE	=P5V_S0_ISENSECAL 53AB 65A
<input type="checkbox"/>	TRUE	=PP1V8_S3_REG 62C1 65B
<input type="checkbox"/>	TRUE	=PP1V5_S0_REG 60C1 65C
<input type="checkbox"/>	TRUE	PPVCORE_S0_GPU 65D1
<input type="checkbox"/>	TRUE	GND

2 TPs per

8 TPs, 2 with each of above TP pairs

## Camera Connector

FUNC_TEST		
	TRUE	=PP5V S3 CAMERA 45C3 65B1
		=USB2 CAMERA_N 6C3 45C3
		=USB2 CAMERA_P 6D3 45B3

## RTC Battery Connector

FUNC_TEST		
TRUE	PPVBATT G3C RTC	26D6
TRUE	GND	

## Inverter Connector

FUNC_TEST		
TRUE	GND CHASSIS INVERTER	6A8
TRUE	PPBUS_S0 INVERTER	76B5
TRUE	GND INVERTER	76A5
TRUE	INVERTER PWM	76A5
TRUE	PP5V INVERTER SW	76B5

## Functional / ICT Test

SYNC_MASTER=N/A	SYNC_DATE=N/A
-----------------	---------------

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APPLE COMPUTER INC.

SIZE	
TYPE	

051-7270





REV. B

SCALE	NONE
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SHT	OF
5	105

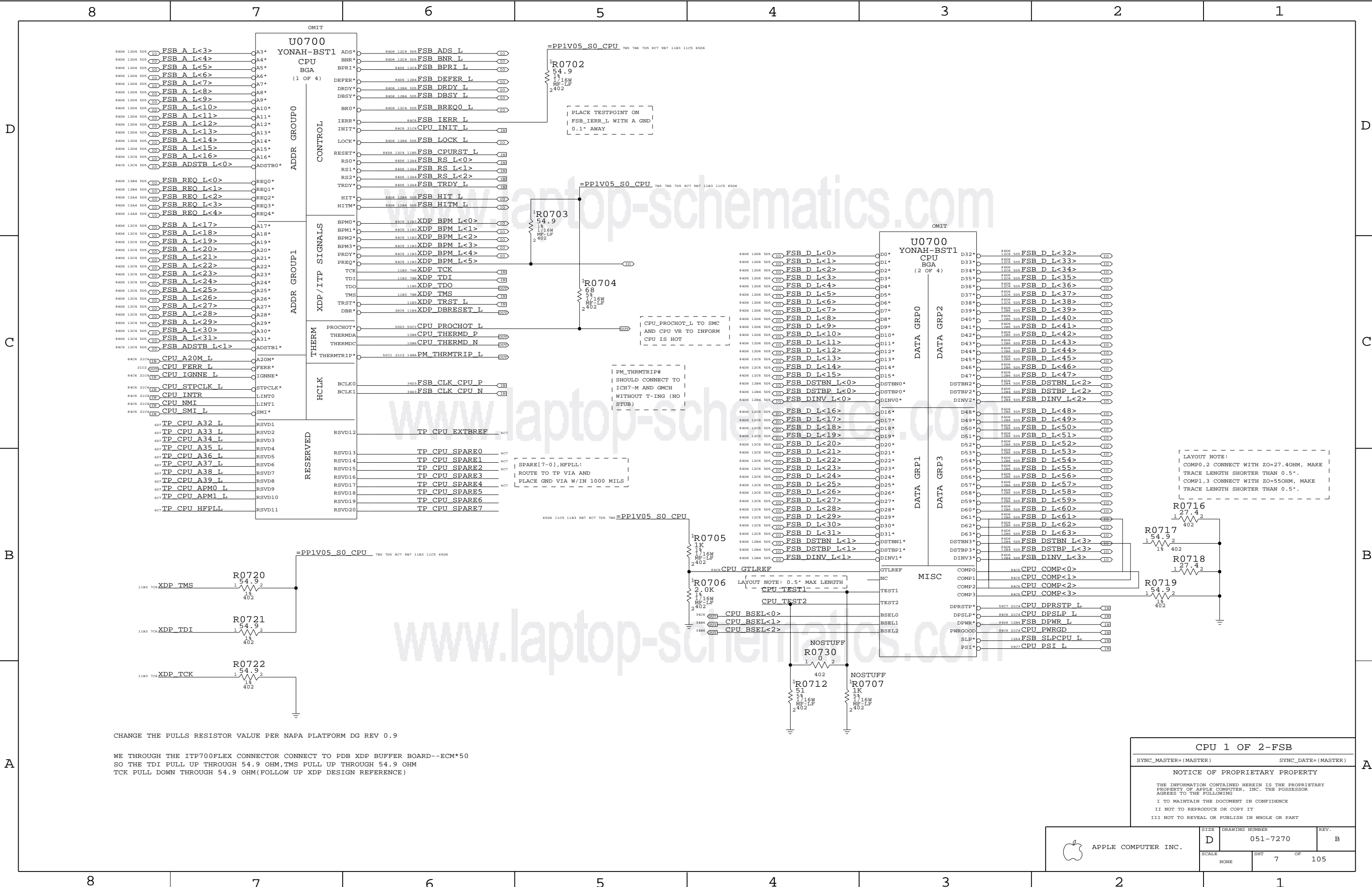
EXPOSED\_VIA property indicates that the net should have a via with 10-mil soldermask opening for use as engineering probe point.

## Misc EXPOSED\_VIA Nets

EXPOSED_VIA			
	TRUE	DMI N2S P<1..0>	1484 2202
	TRUE	DMI N2S N<1..0>	1484 2202
	TRUE	SB CLK100M SATA P	2186 34C3
	TRUE	SB CLK100M SATA N	2186 34C3

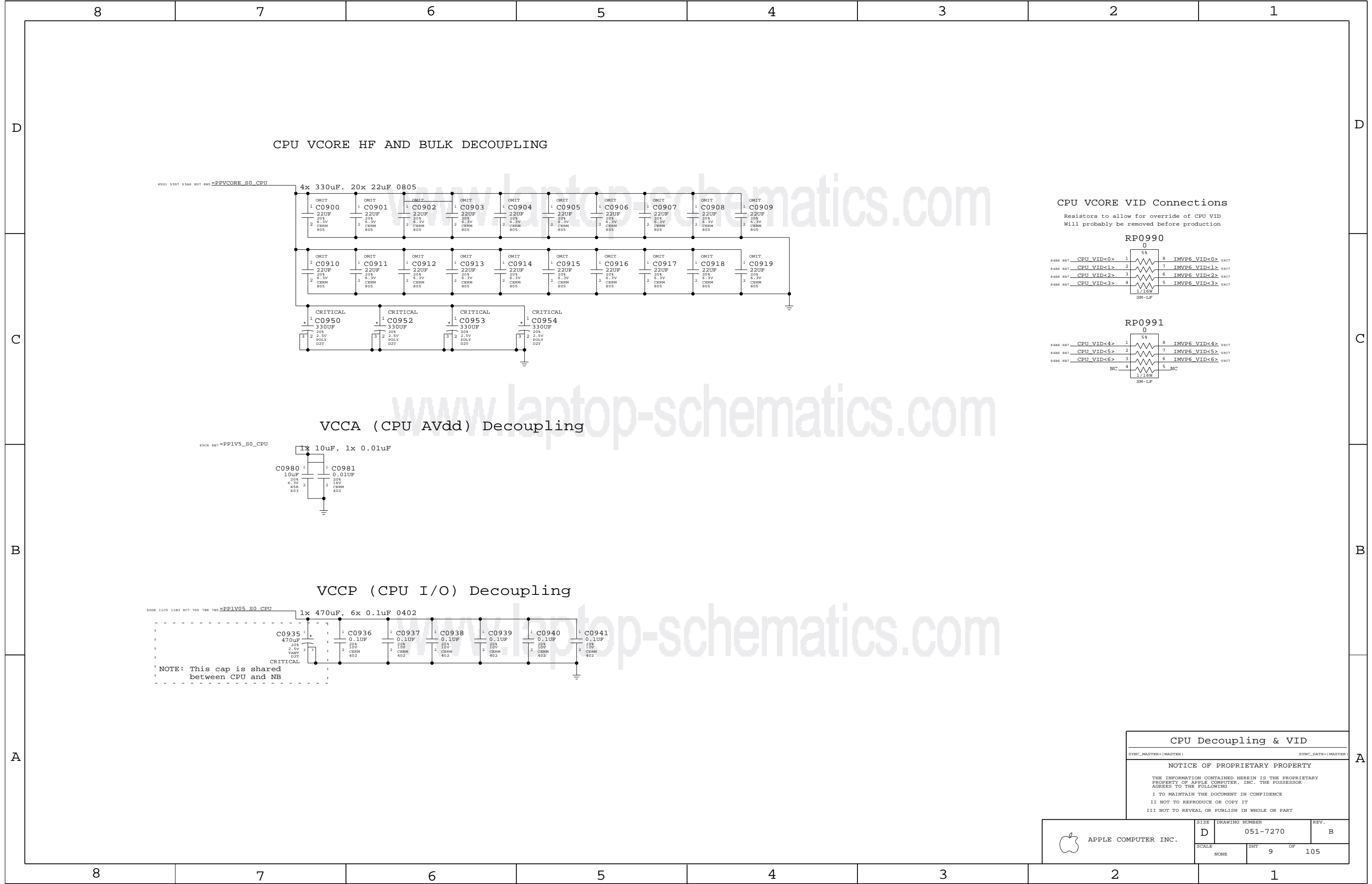


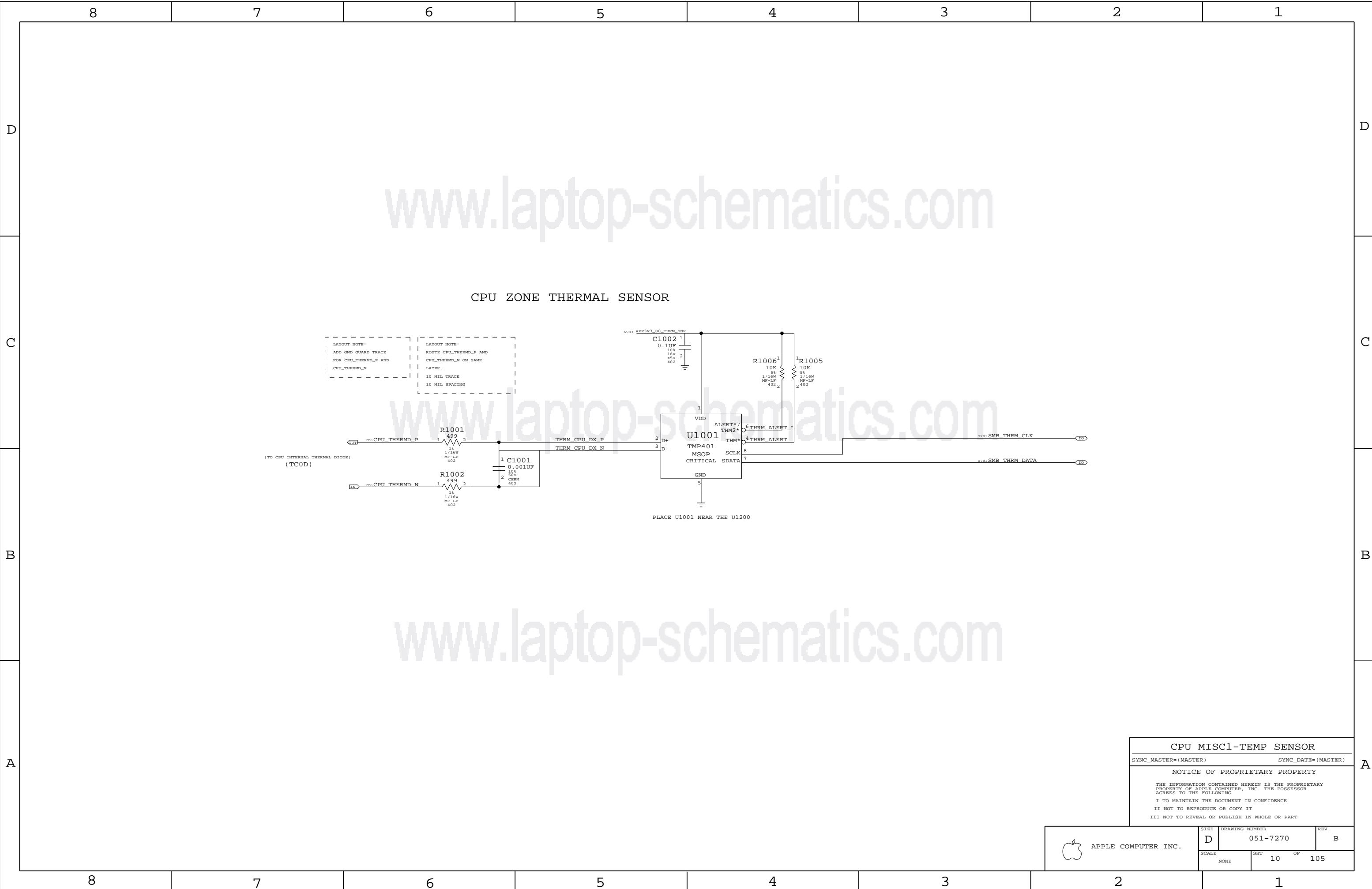










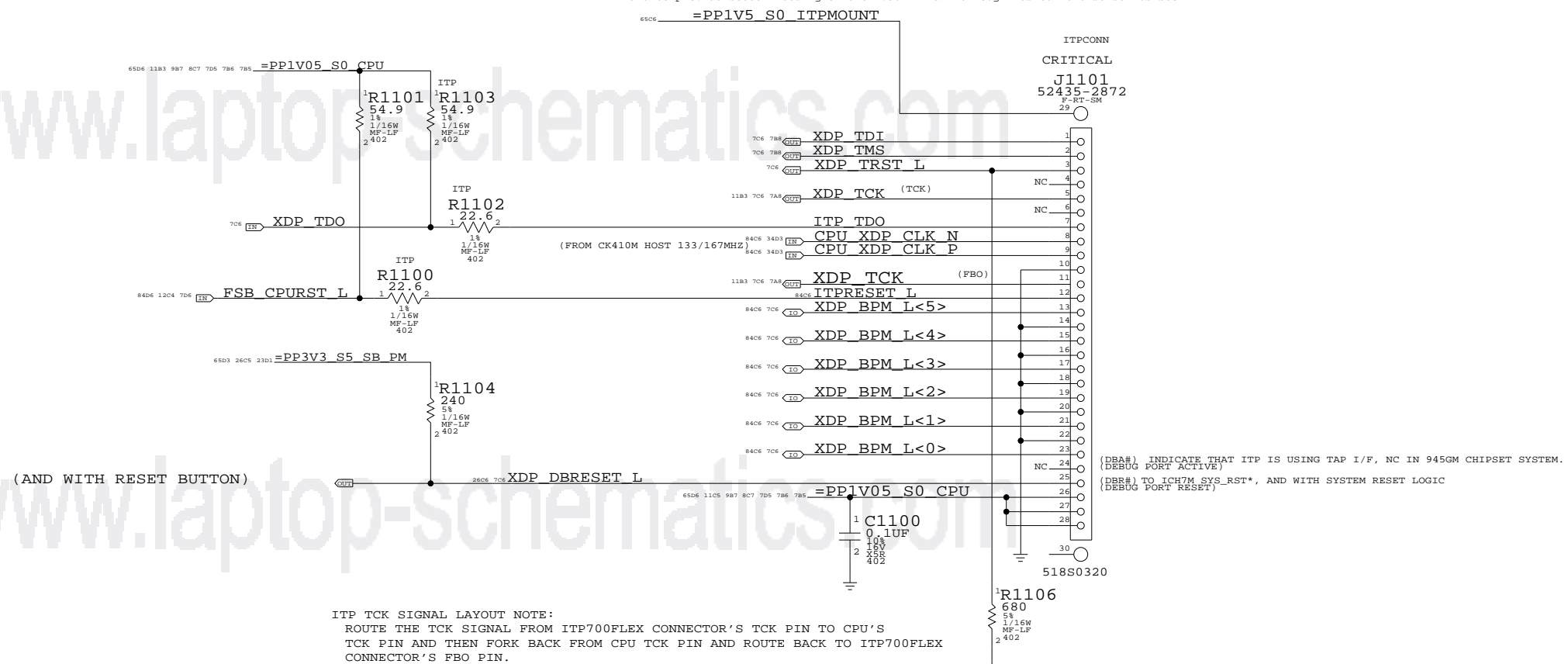


CPU MISC1-TEMP SENSOR	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7270	REV. B
	SCALE NONE	SHT 10	OF 105

## CPU ITP700FLEX DEBUG SUPPORT

Note: This connection to lv5\_S0 is to steal this mounting pad to add to the 1.5V S0 shape and to provide better feeding of the 1.5V NB rail through its current sense resistor



ITP TCK SIGNAL LAYOUT NOTE:  
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S  
TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX  
CONNECTOR'S FBO PIN.


```

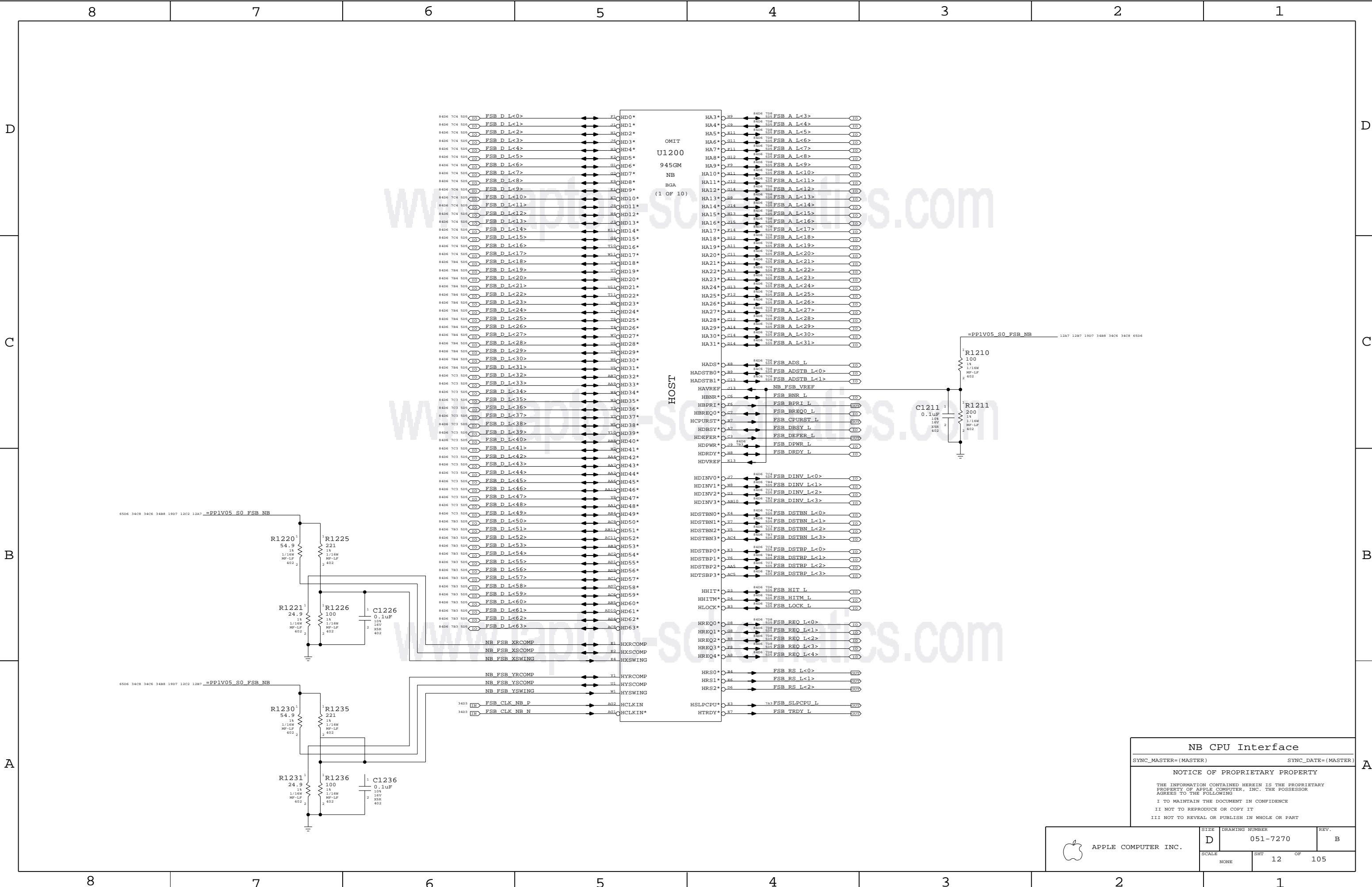
CPU ITP700FLEX DEBUG
-----
SYNC_MASTER=(MASTER)          SYNC_DATE=(MASTER)
-----
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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7270	B
	SCALE	SHT OF	
	NONE	11	105



NB CPU Interface

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

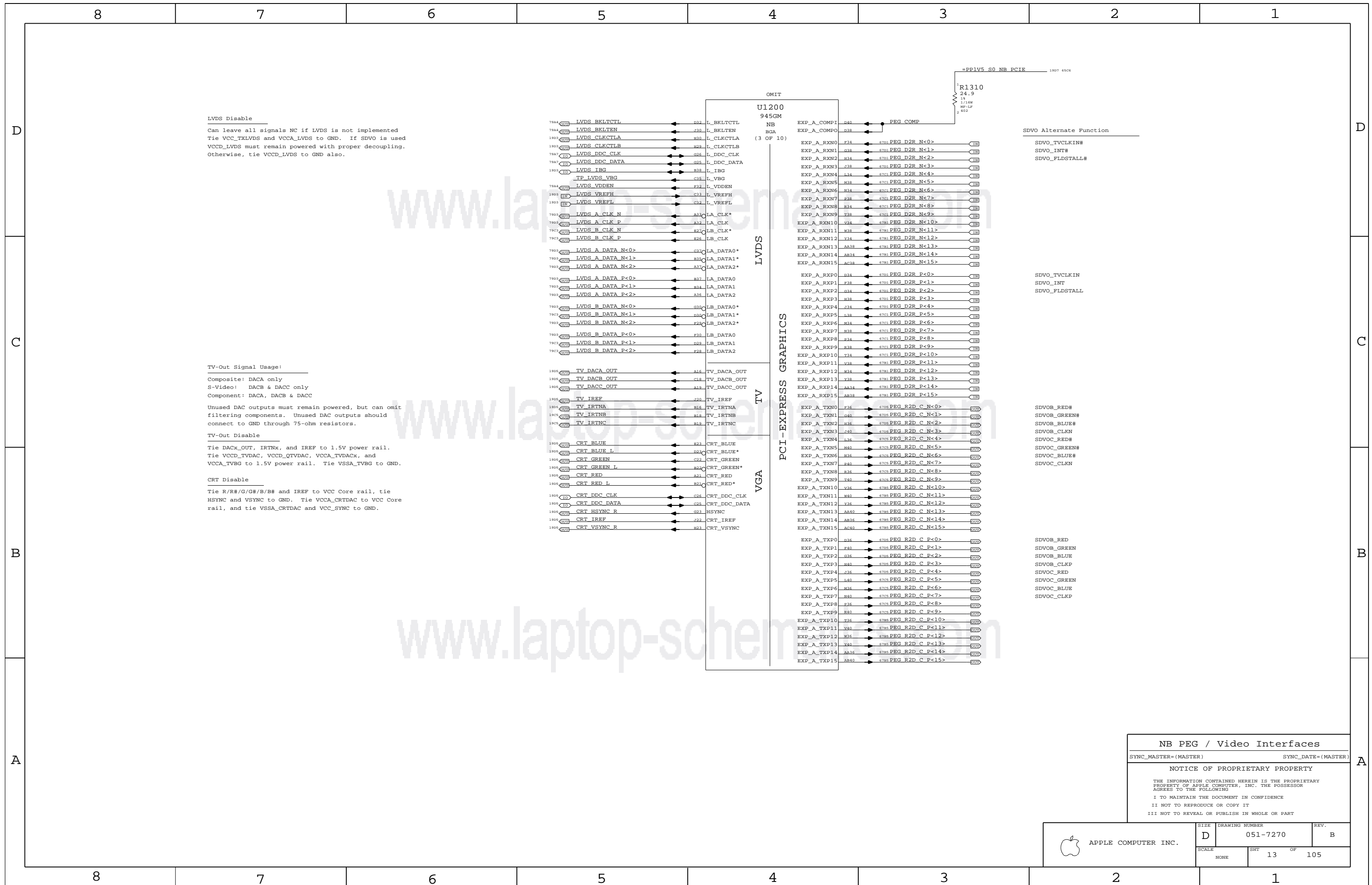
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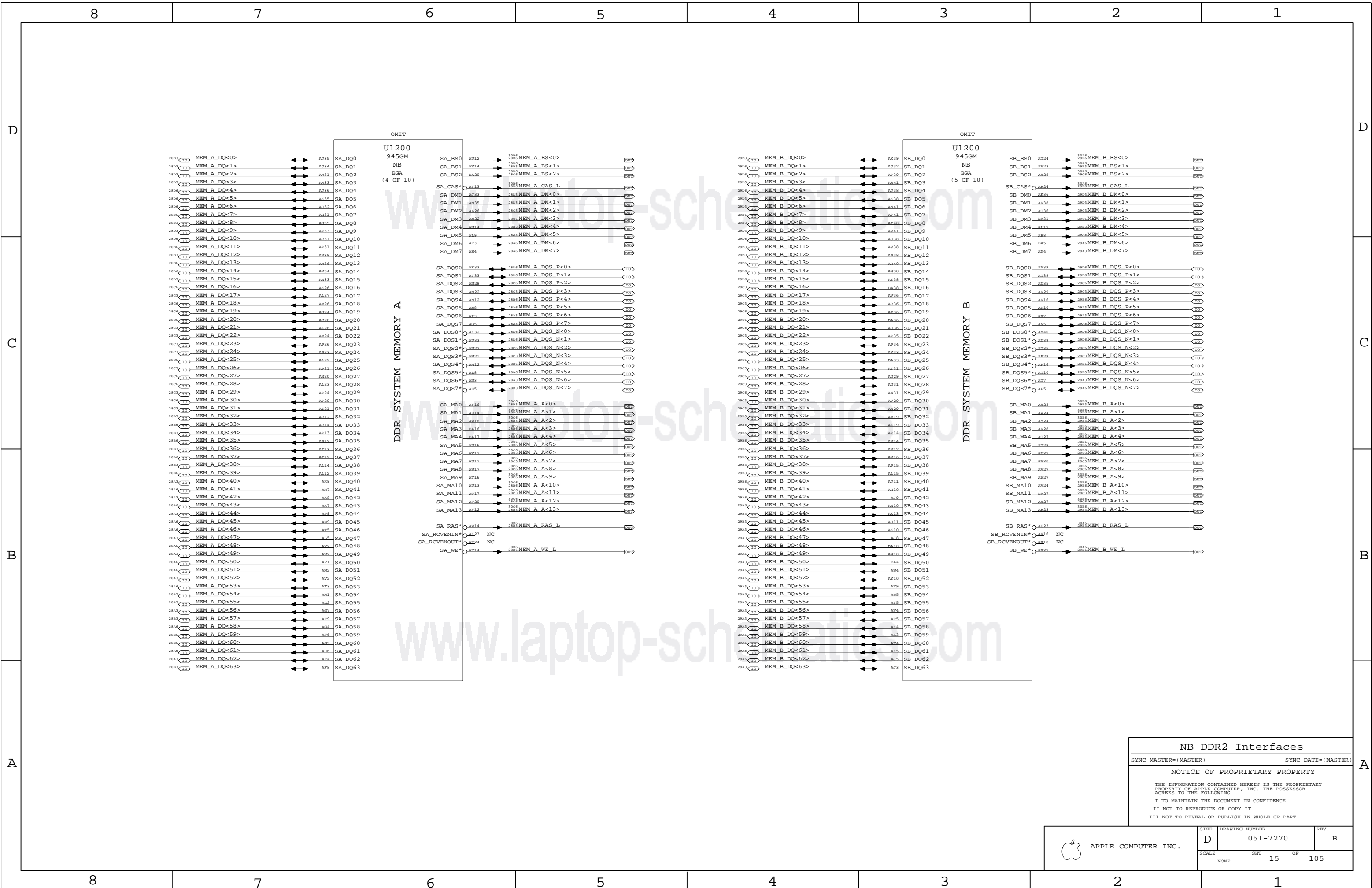
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NB DDR2 Interfaces

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

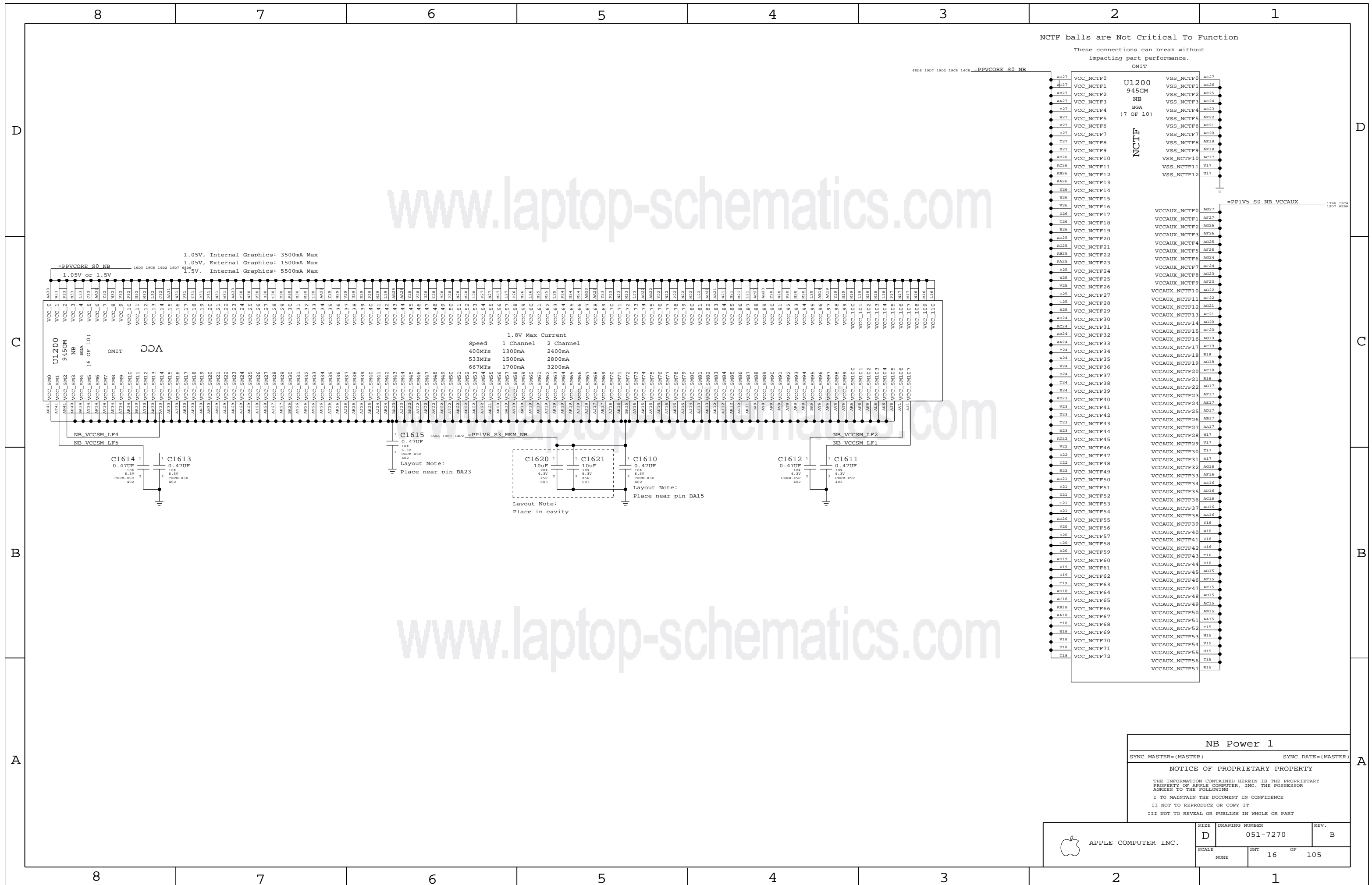
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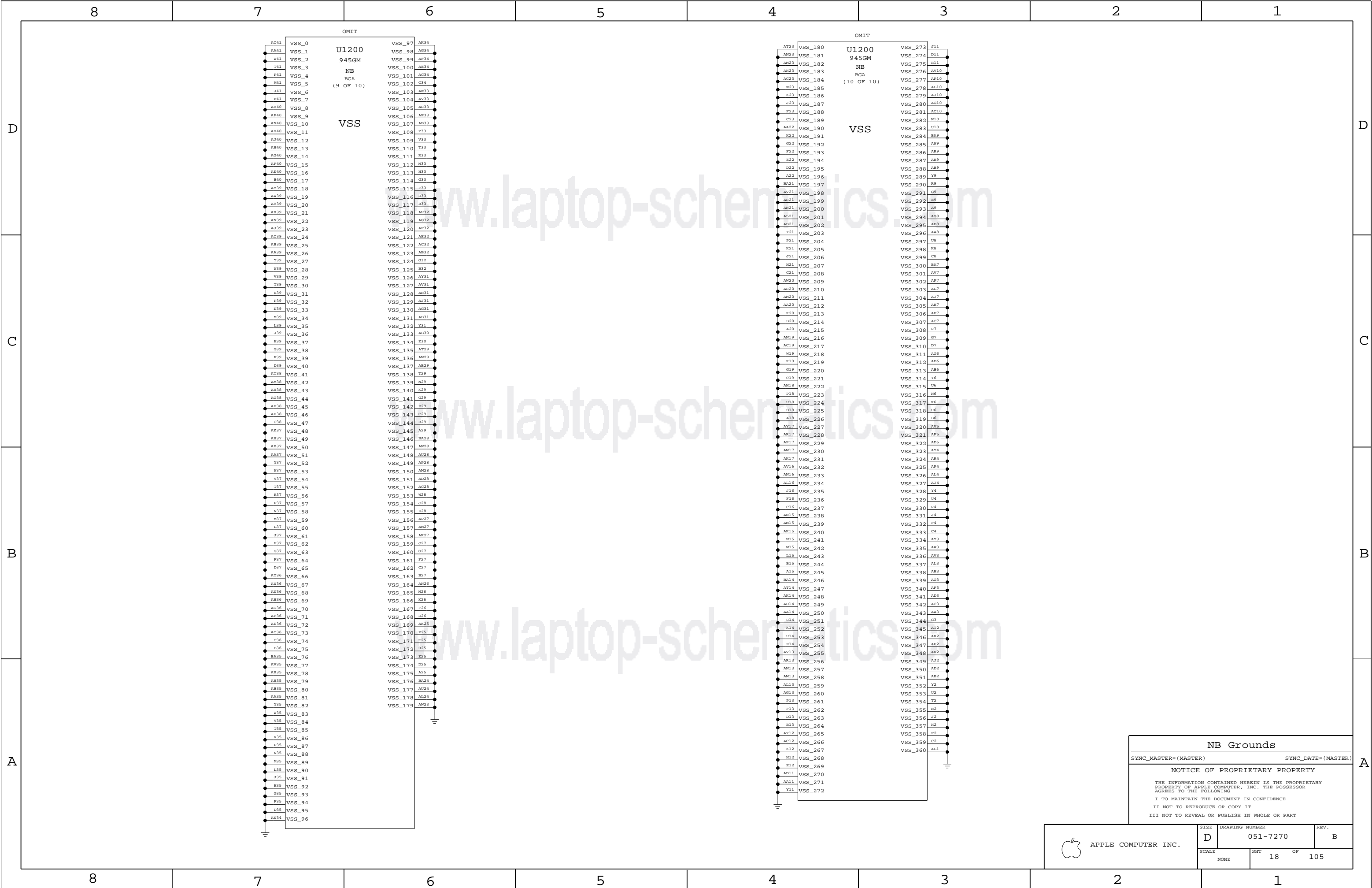
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D

C

B

A

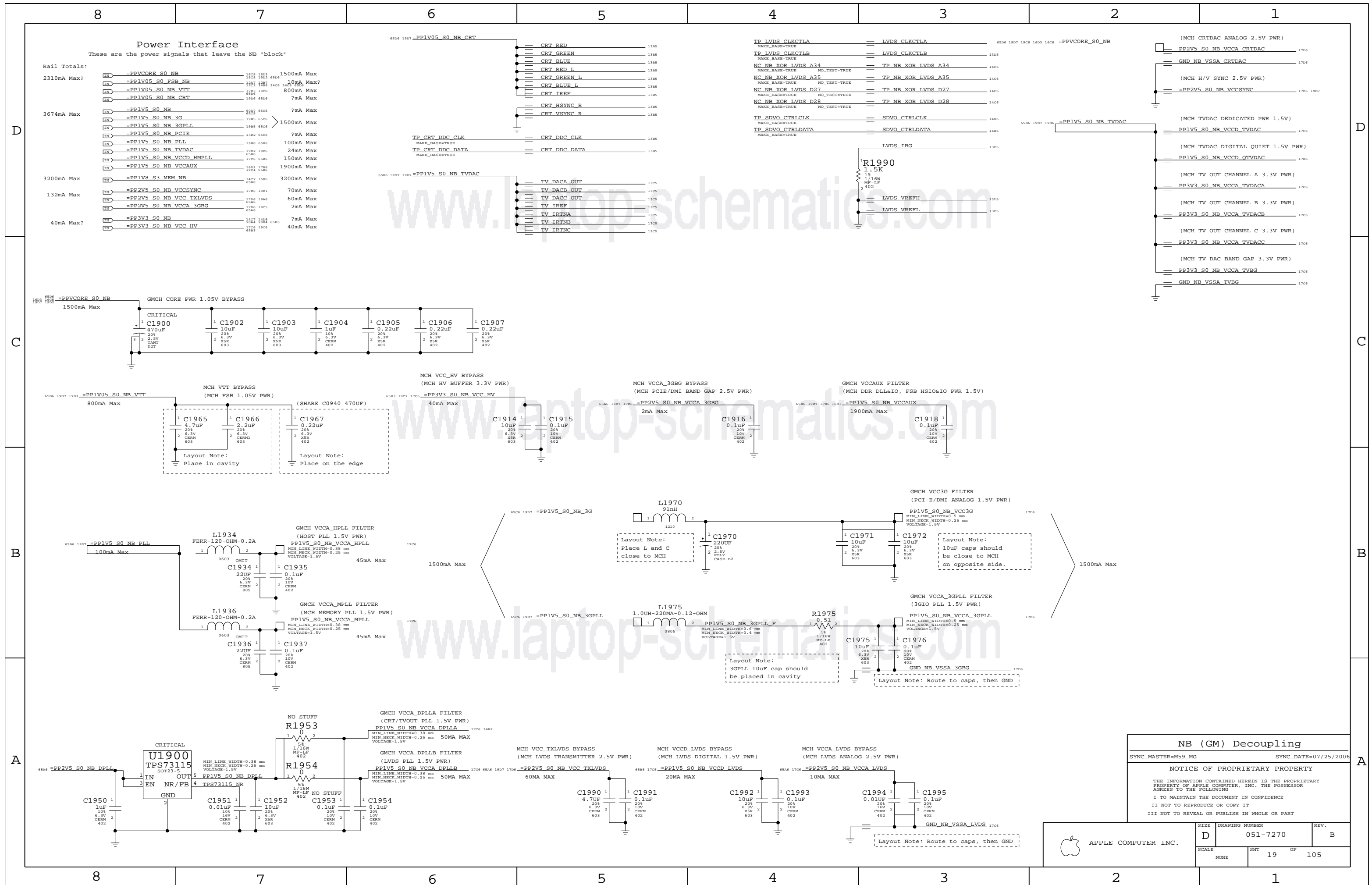
D

C

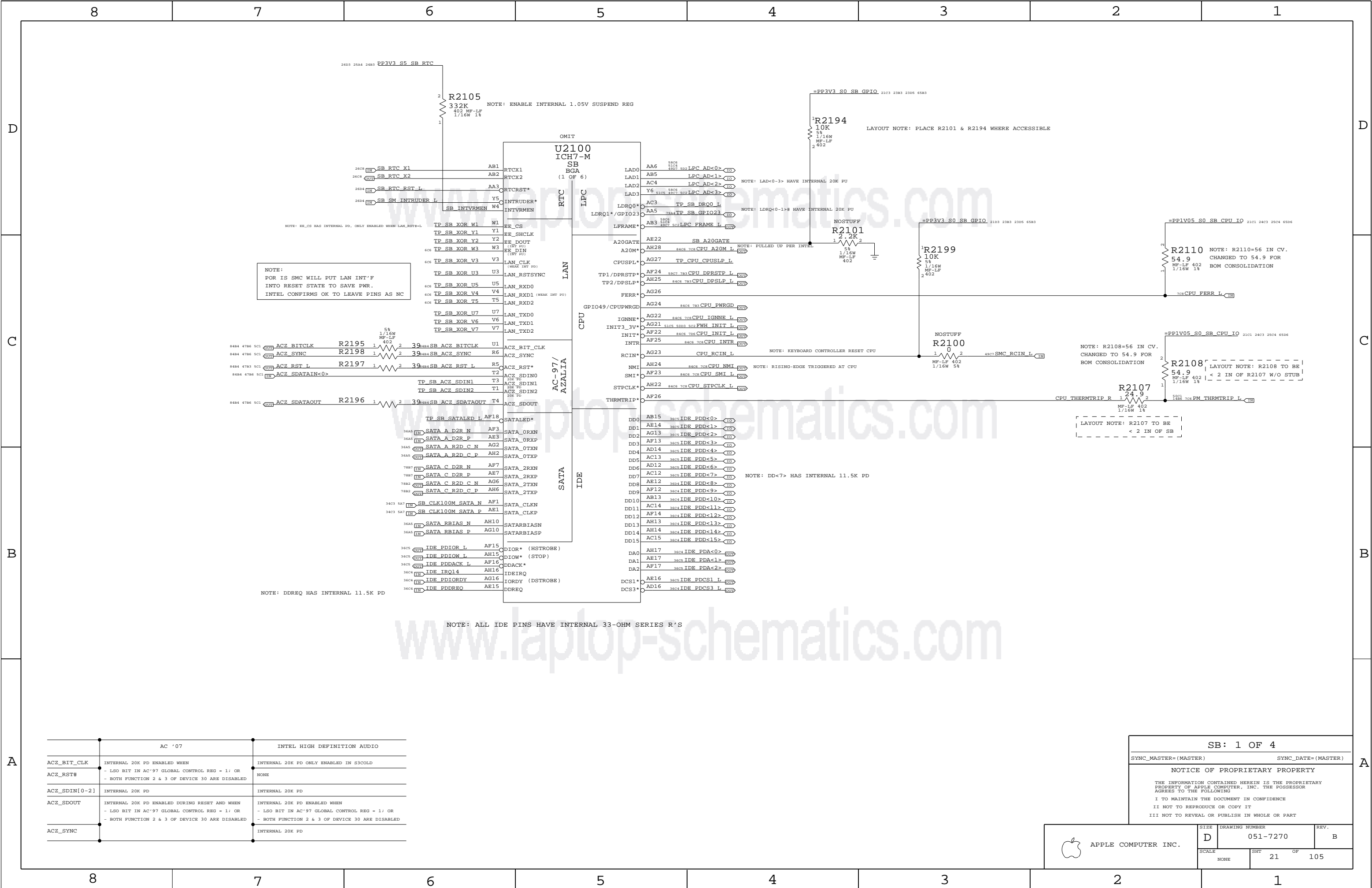
B

A

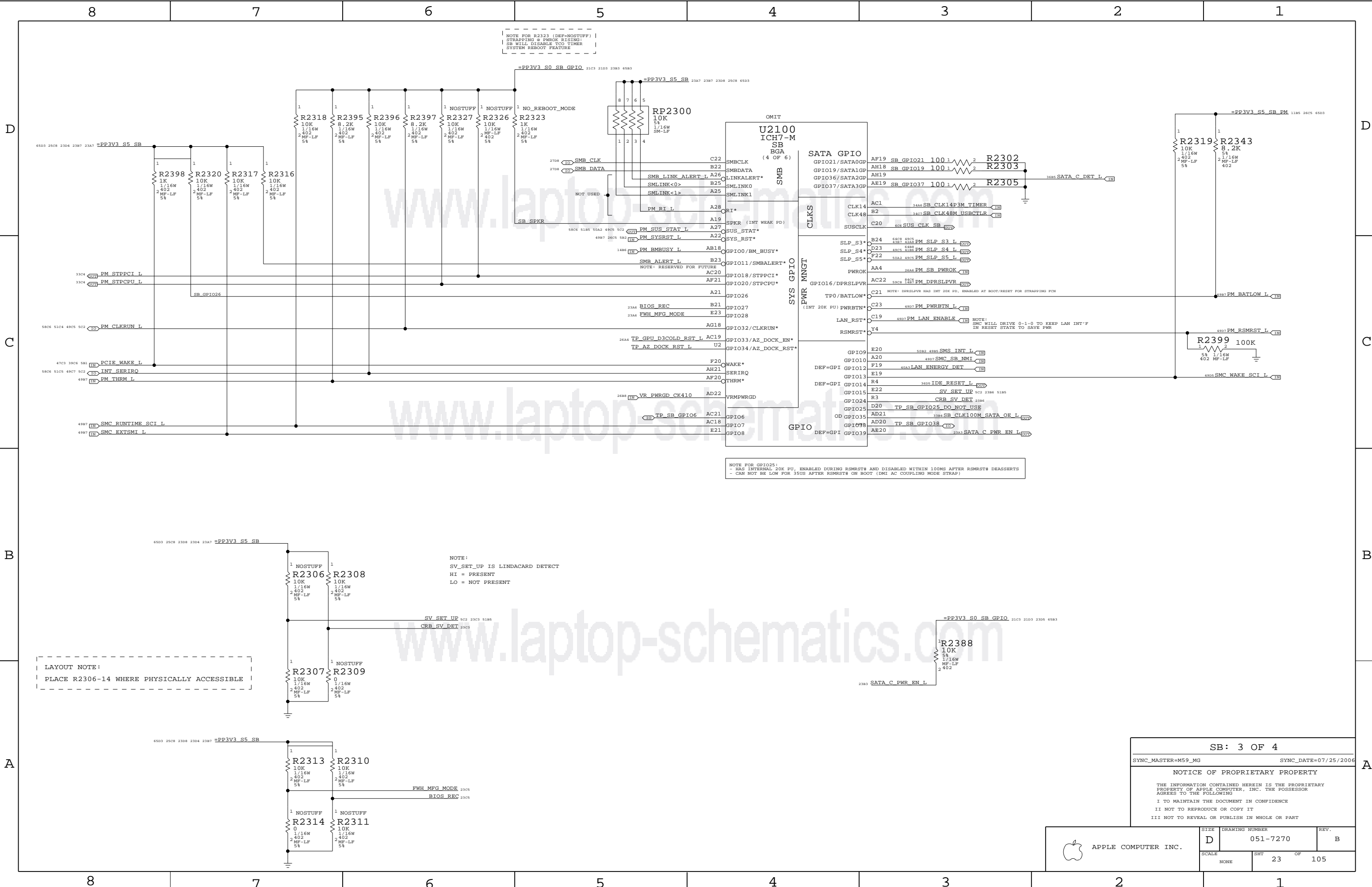












NOTE FOR GPIO25:  
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS  
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

LAYOUT NOTE:  
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

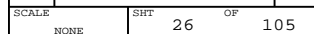
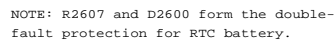
NOTE:  
SV\_SET\_UP IS LINDACARD DETECT  
HI = PRESENT  
LO = NOT PRESENT

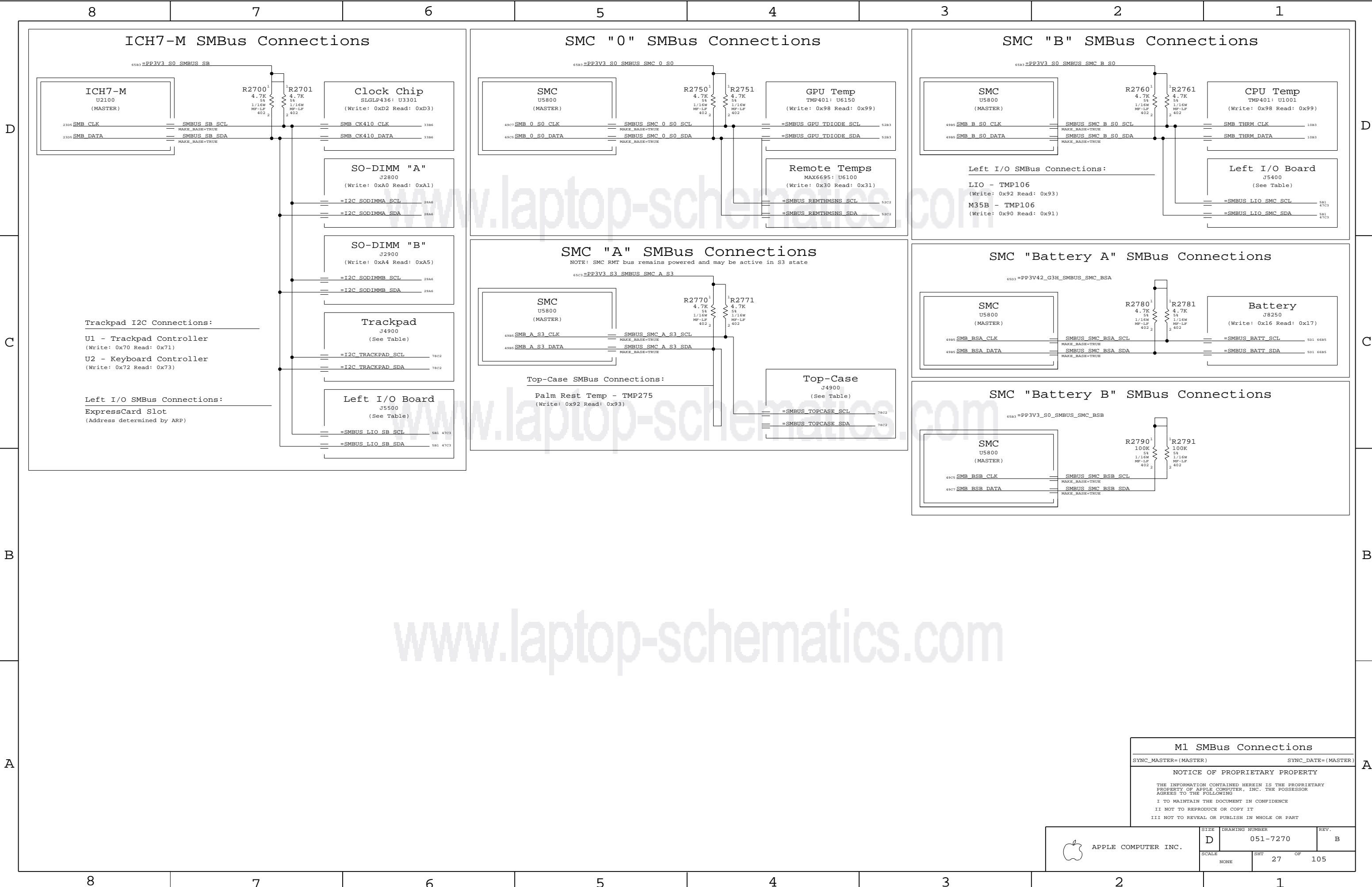
SB: 3 OF 4  
SYNC\_MASTER=M59\_MG SYNC\_DATE=07/25/2006  
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M1 SMBus Connections

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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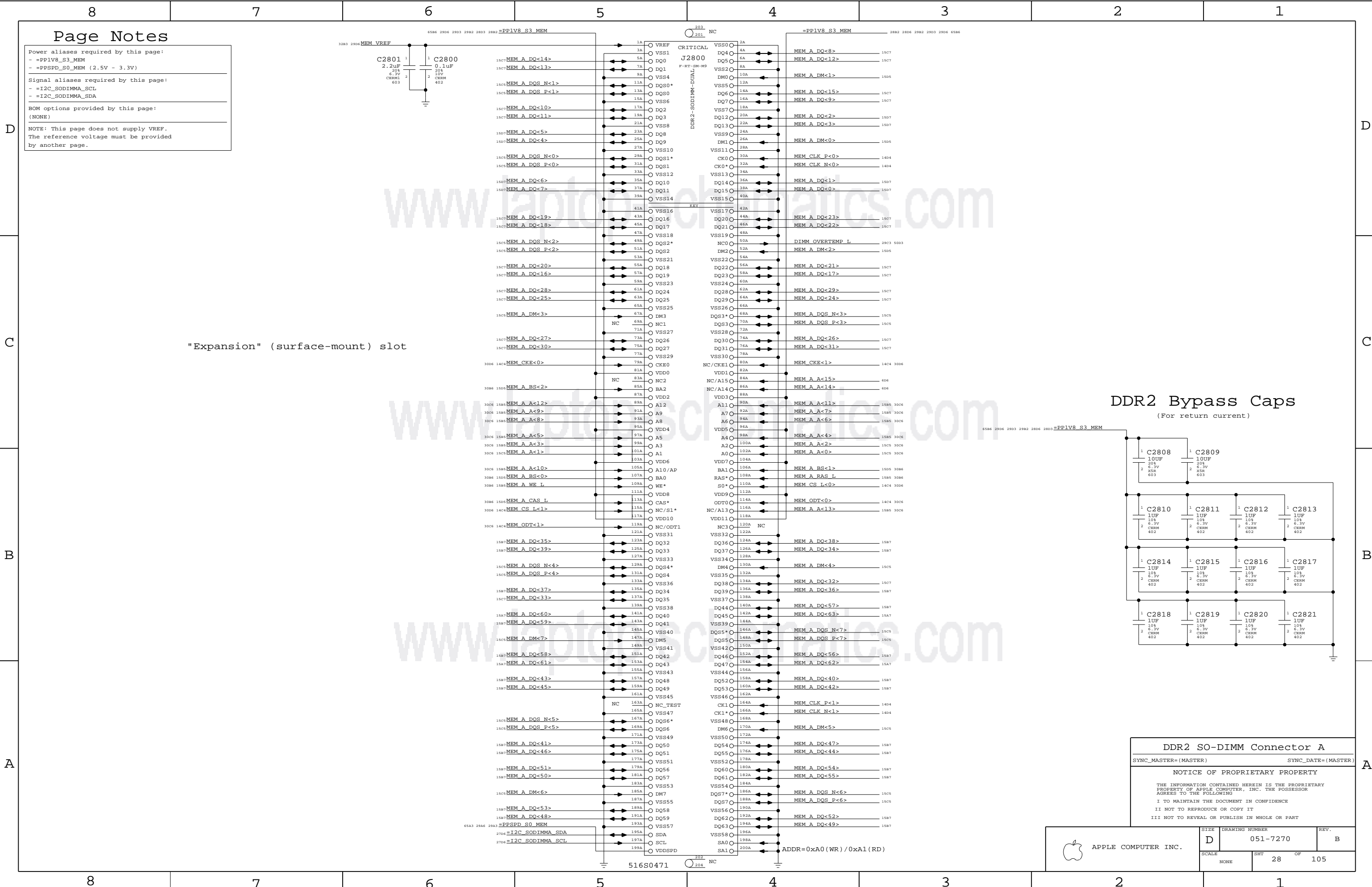
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7270	B
SCALE		SHT	OF
NONE		27	105



Page Notes

Power aliases required by this page:

- =PPIV8\_S3\_MEM
- =PPSPD\_S0\_MEM (2.5V - 3.3V)

Signal aliases required by this page:

- =I2C\_SODIMMA\_SCL
- =I2C\_SODIMMA\_SDA

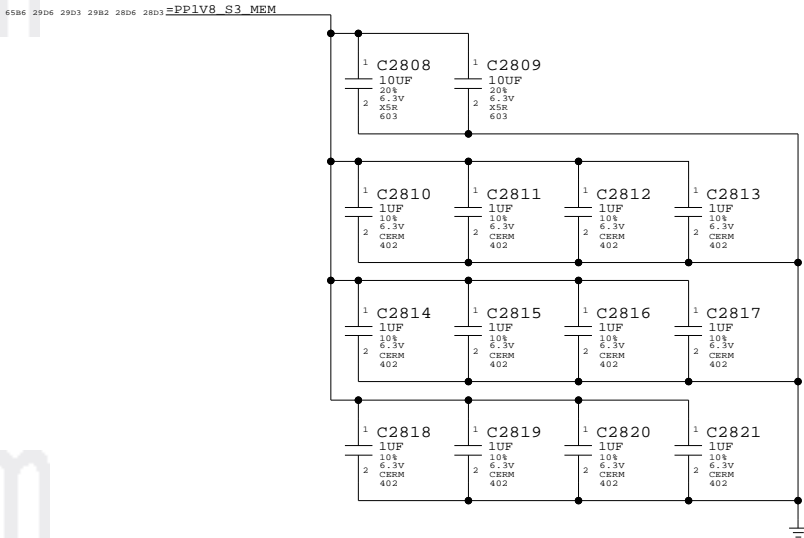
BOM options provided by this page:

(NONE)

NOTE: This page does not supply VREF.  
The reference voltage must be provided by another page.

"Expansion" (surface-mount) slot

DDR2 Bypass Caps  
(For return current)



DDR2 SO-DIMM Connector A

SYNC\_MASTER=(MASTER)

SYNC\_DATE=(MASTER)

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APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-7270

REV.

B

SCALE

NONE

SHT

28

OF

105



Power aliases required by this page:

- =PPIV8\_S3\_MEM
- =PPSPD\_S0\_MEM (2.5V - 3.3V)

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Signal aliases required by this page:

- =I2C\_SODIMMB\_SCL
- =I2C\_SODIMMB\_SDA

---

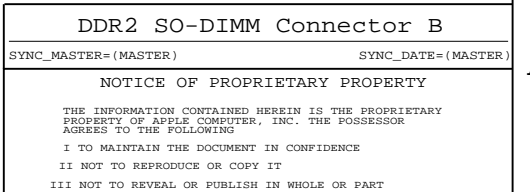
BOM options provided by this page:

(NONE)

---

NOTE: This page does not supply VREF.  
The reference voltage must be provided  
by another page.

## DDR2 Bypass Caps



APPLE COMPUTER INC.

SIZE D	DRAWING NUMBER 051-7270	REV. B
SCALE NONE	SHT 29	OF 105



8	7	6	5	4	3	2	1
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D

C

B

A

8	7	6	5	4	3	2	1
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B

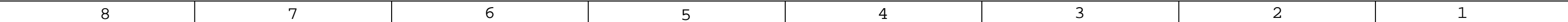
A

8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

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B

A



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B

A

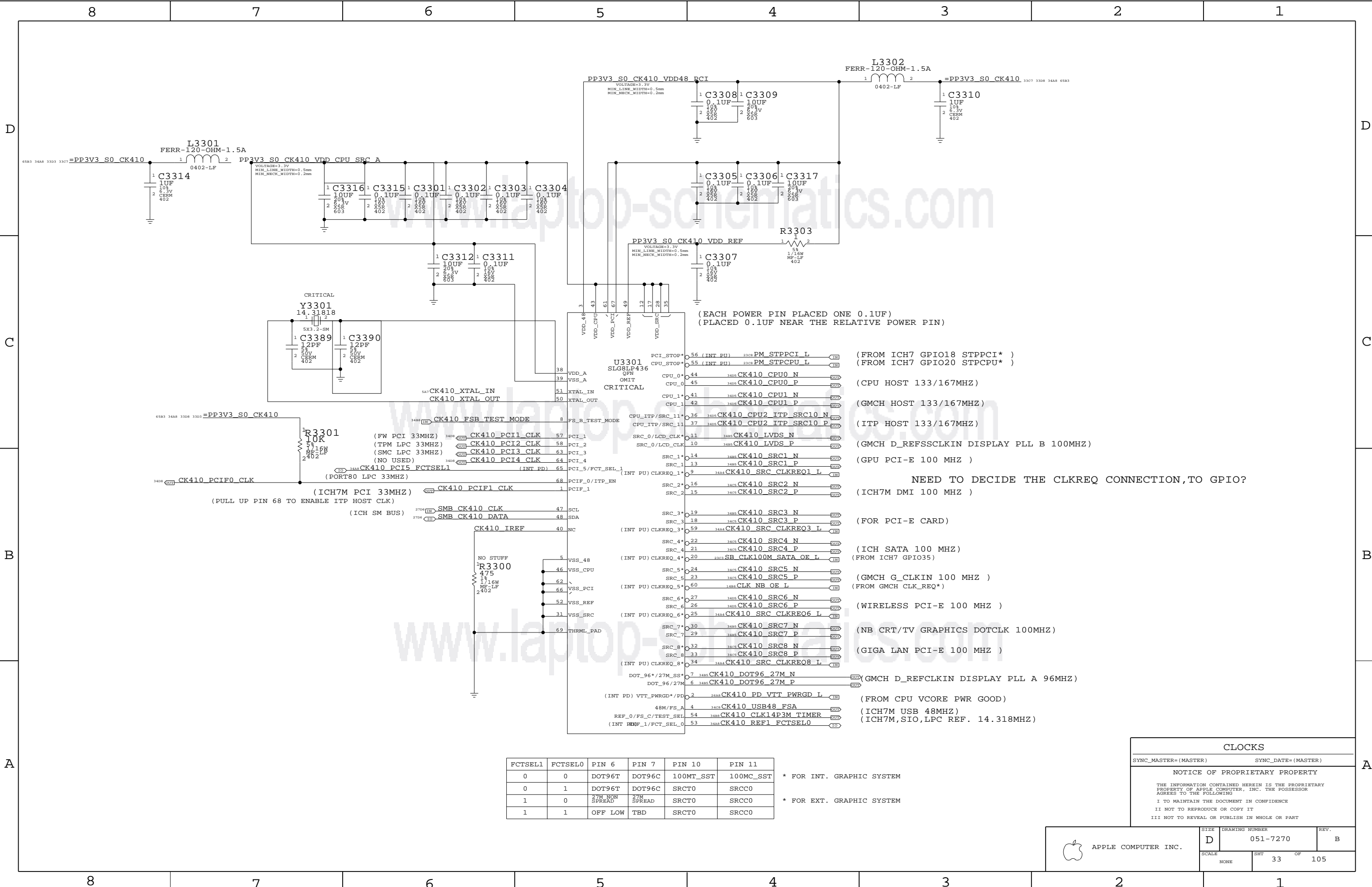
8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

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B

A





FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST
0	1	DOT96T	DOT96C	SRCT0	SRCC0
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0
1	1	OFF LOW	TBD	SRCT0	SRCC0

\* FOR INT. GRAPHIC SYSTEM

\* FOR EXT. GRAPHIC SYSTEM

CLOCKS

SYNC\_MASTER=(MASTER)

SYNC\_DATE=(MASTER)

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APPLE COMPUTER INC.

SIZE D

DRAWING NUMBER 051-7270

REV. B

SCALE NONE

SHT 33

OF 105



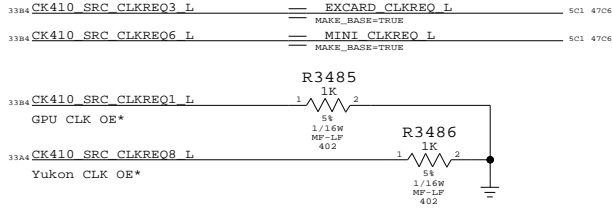
PLACEMENT of these caps should be close as possible to the resistors

NEED TO CHECK THE BSEL PULLS

NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

	FS_C	FS_B	FS_A	CPU
#	0	0	0	266M
#	0	0	1	133M
	0	1	0	166M
	0	1	1	200M
	1	0	0	100M
	1	0	1	333M
	1	1	0	400M
	1	1	1	RESERVED

# NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED



Clock Termination

SYNC\_MASTER=M59\_MG SYNC\_DATE=05/07/2006

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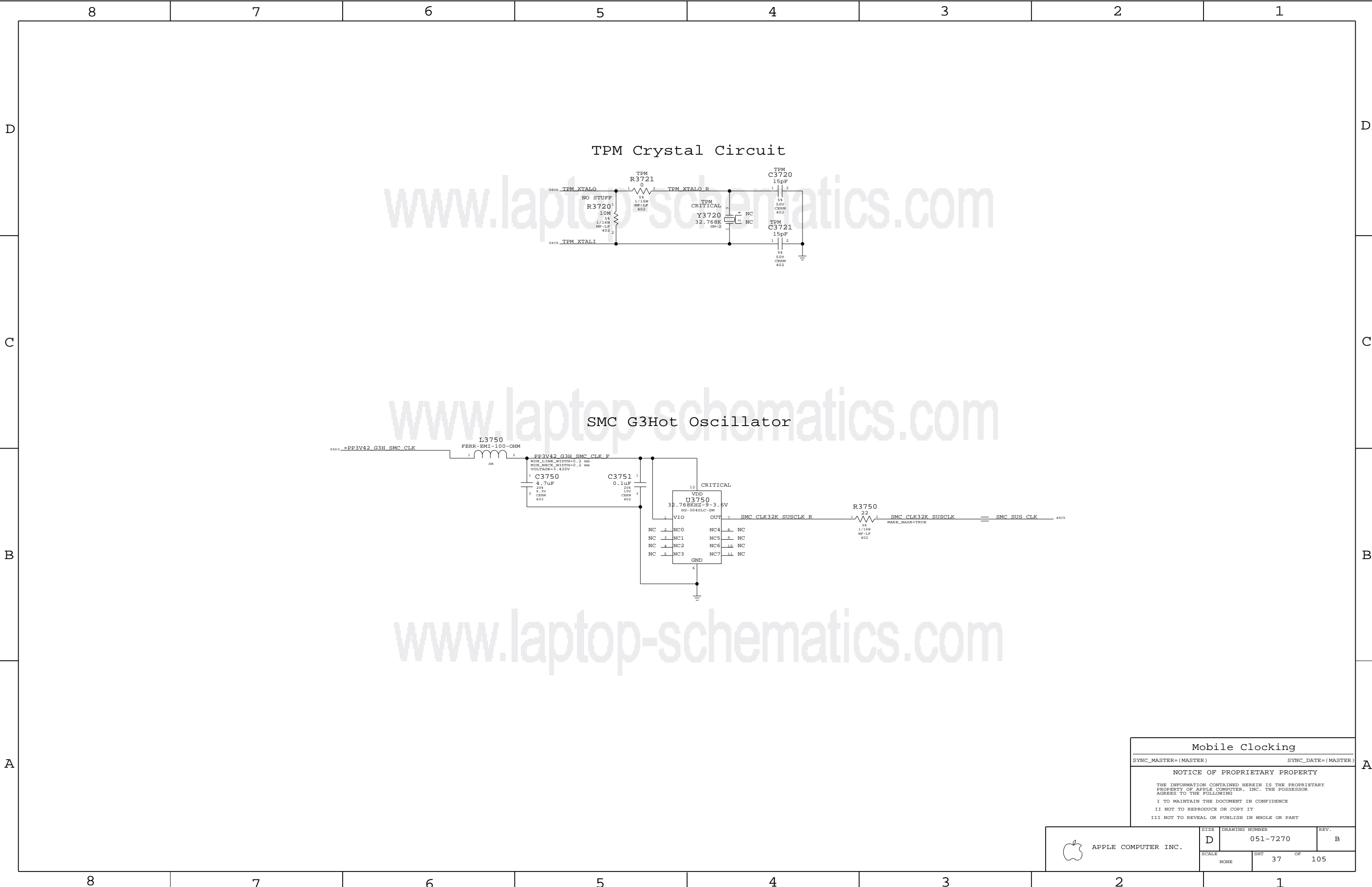
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SCALE	SHT	OF
NONE	34	105





Mobile Clocking

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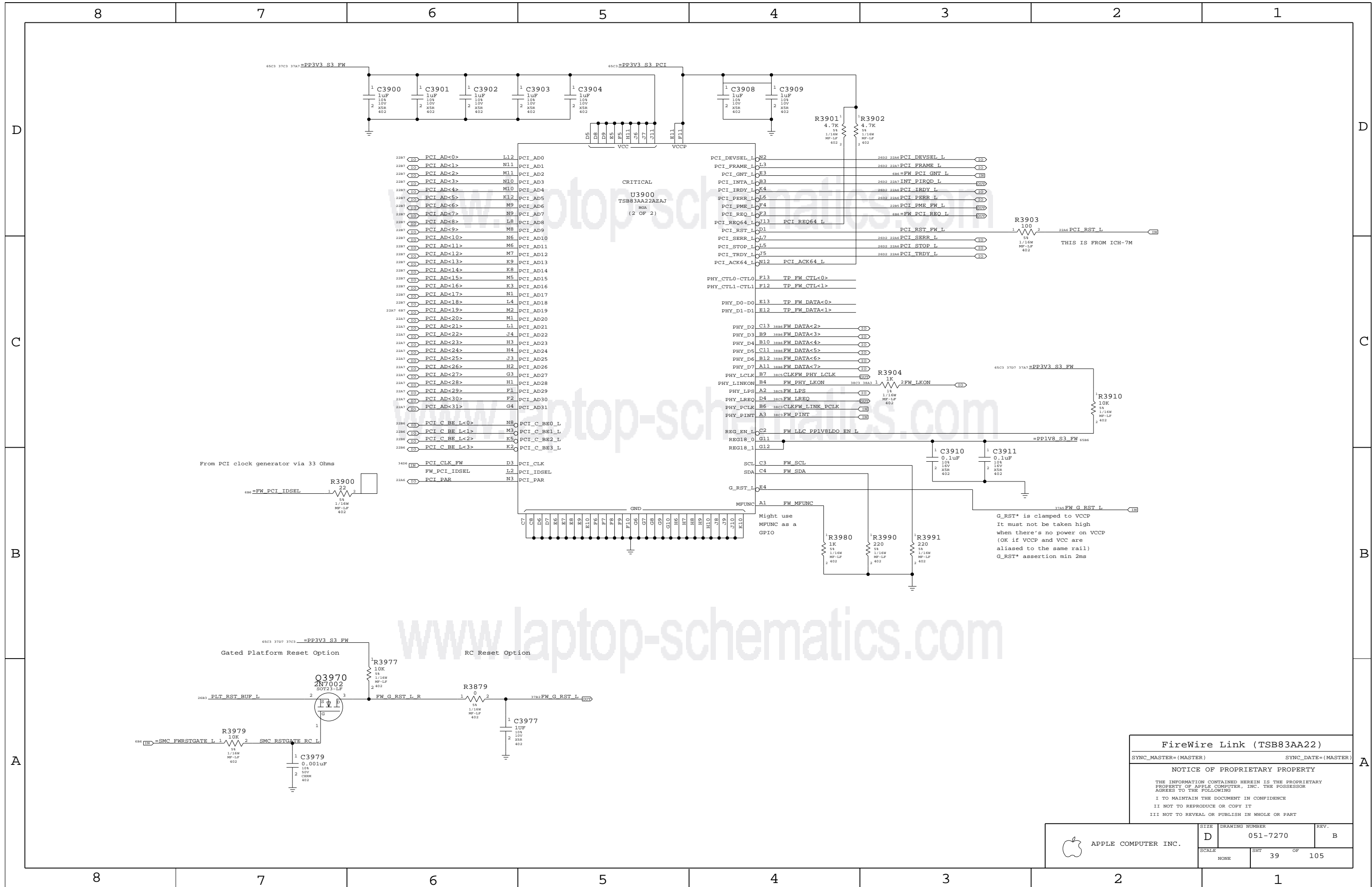
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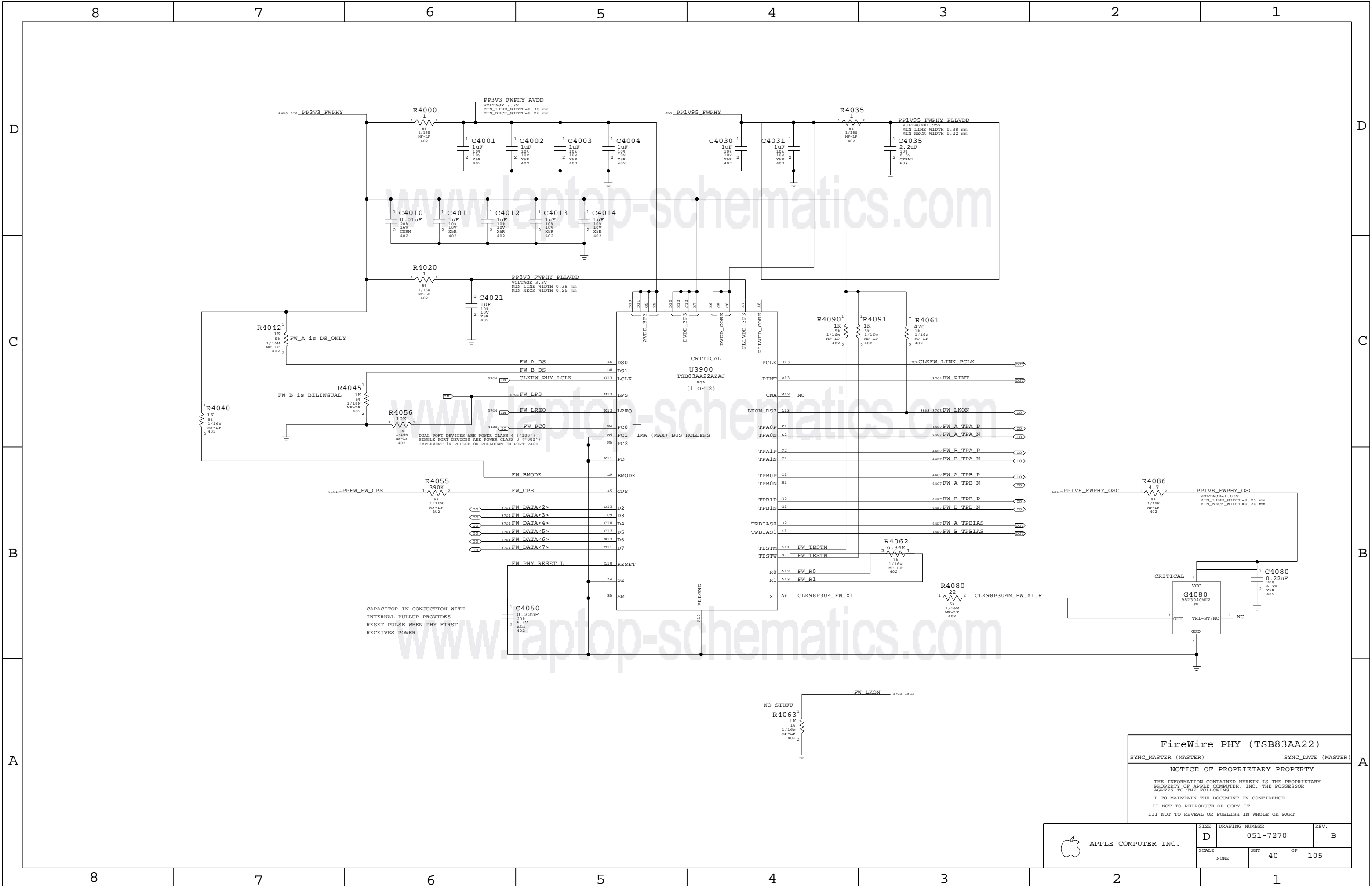
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	SCALE NONE	SHT 37	OF 105







FireWire PHY (TSB83AA22)

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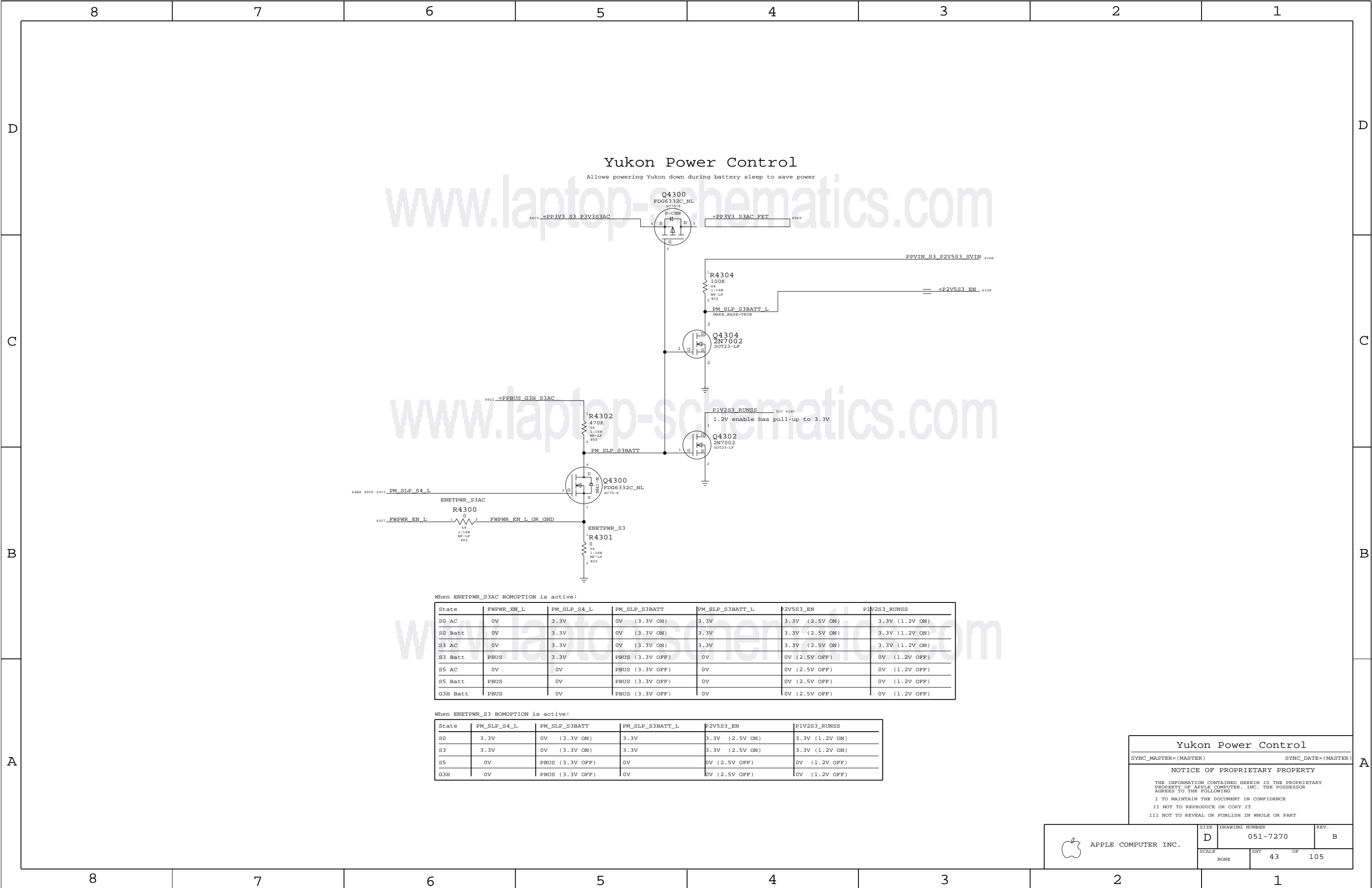
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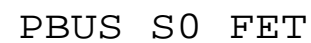
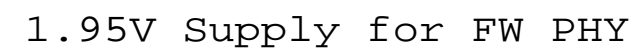
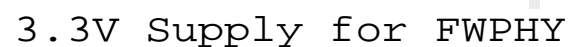
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	SCALE NONE	SHT 40	OF 105











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SIZE	DRAWING NUMBER	REV.
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D	051-7270
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D	931 7270
---	----------

SCALE	SHT	OF
	44	105

NONE	44	105
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Power aliases required by this page:

- =PPBUS\_S0\_FWPWRSW (system supply for bus power)
- =PD3V3\_S0\_FWPORTPWRSW

---

Signal aliases required by this page:

- =FWPWR\_PWRON (see related text note below)

---

BOM options provided by this page:

(NONE)

The schematic diagram illustrates the power management circuitry, centered around the U4500 MAX5943 QSOP1 power management IC. The IC is configured to control two power MOSFETs, Q4501 (SI7222DN) and Q4502 (MMDT3906XF), which are used for power regulation. The circuit includes several resistors (R4500, R4560, R4561, R4501, R4502, R4503, R4504) and capacitors (C4560, C4500) for timing and signal conditioning. The power management IC is connected to the power supply (PPBUS\_S5\_FWPWR) and the power MOSFETs. The diagram is labeled with component values and pin numbers.

**Component Values and Pin Numbers:**

- U4500 MAX5943 QSOP1:**
  - IN: 16
  - CRITICAL: 11
  - OUT: 11
  - SENSE: 15
  - GATE1: 14
  - GATE2: 12
  - ONQ1: 8
  - ILIM: 4
  - OR\_ADJ: 3
  - TIM: 6
  - LATCH: 5
  - ON: 1
  - IFAULT\*: 2
  - NC: 7, 10, 13
- Q4501 SI7222DN PWRPK-1212-8:**
  - Gate: 1
  - Source: 2
  - Drain: 3
- Q4502 MMDT3906XF SOT-363:**
  - Gate: 1
  - Source: 2
  - Drain: 3
- Q4560 2N7002DW-X-F SOT-363:**
  - Gate: 1
  - Source: 2
  - Drain: 3
- Q4561 2N7002DW-X-F SOT-363:**
  - Gate: 1
  - Source: 2
  - Drain: 3
- R4500 0.020 1% 0.25W MF 805:**
  - 1: 1
  - 2: 2
- R4560 10K 1% 1/16W MF-LF 402:**
  - 1: 1
  - 2: 2
- R4561 200K 1% 1/16W MF-LF 402:**
  - 1: 1
  - 2: 2
- R4501 100K 1% 1/16W MF-LF 402:**
  - 1: 1
  - 2: 2
- R4502 1K 1% 1/16W MF-LF 402:**
  - 1: 1
  - 2: 2
- R4503 100K 1% 1/16W MF-LF 402:**
  - 1: 1
  - 2: 2
- R4504 1K 1% 1/16W MF-LF 402:**
  - 1: 1
  - 2: 2
- C4560 0.01uF 20% 16V CROW 402:**
  - 1: 1
  - 2: 2
- C4500 1uF 10% 35V X5A 603:**
  - 1: 1
  - 2: 2

**Notes:**

- Current Limit determined by R4500:
  - 0.020 ohm => 2.4A
  - 0.025 ohm => 2A
  - 0.030 ohm => 1.66A (ideal)
  - 0.033 ohm => 1.5A
- Q4501 is a dual FET for redundancy and UL compliance for single-point failure protection.

FWLATEVG\_3V\_REF Hysteresis:  
 2.95v when port power is on  
 2.81v on late Vg event and port power is off

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	Q328	DRAWING NUMBER
--	------	----------------



SIZE	DRAWING NUMBER	REV.
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D	051-7270
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5517270

SCALE	SHT
	45

NONE	43
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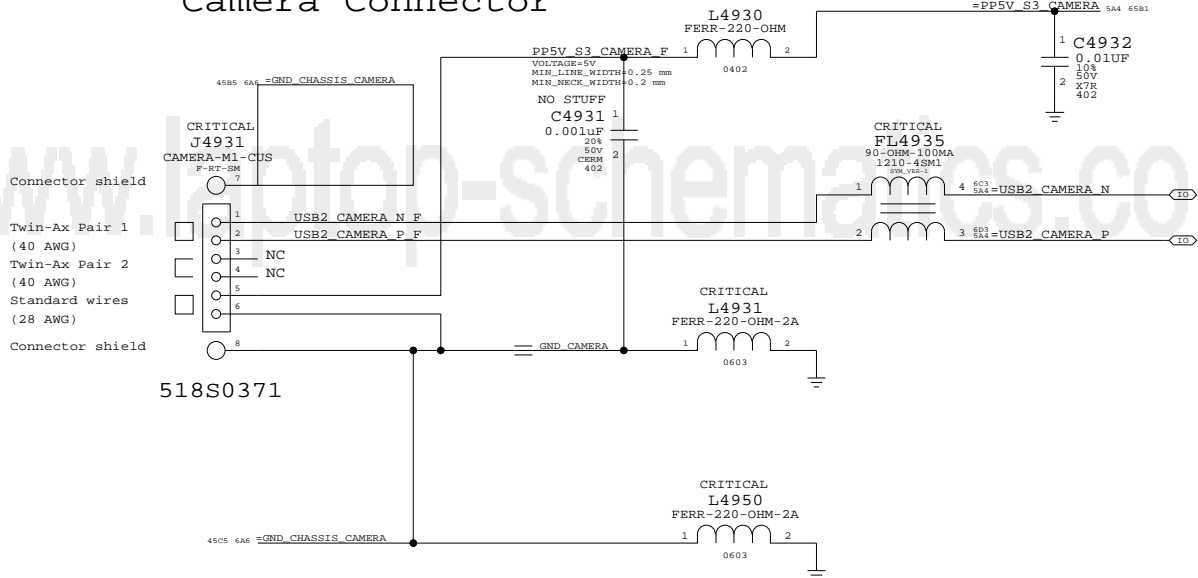

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AAAAA

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Camera Connector



Camera Connector

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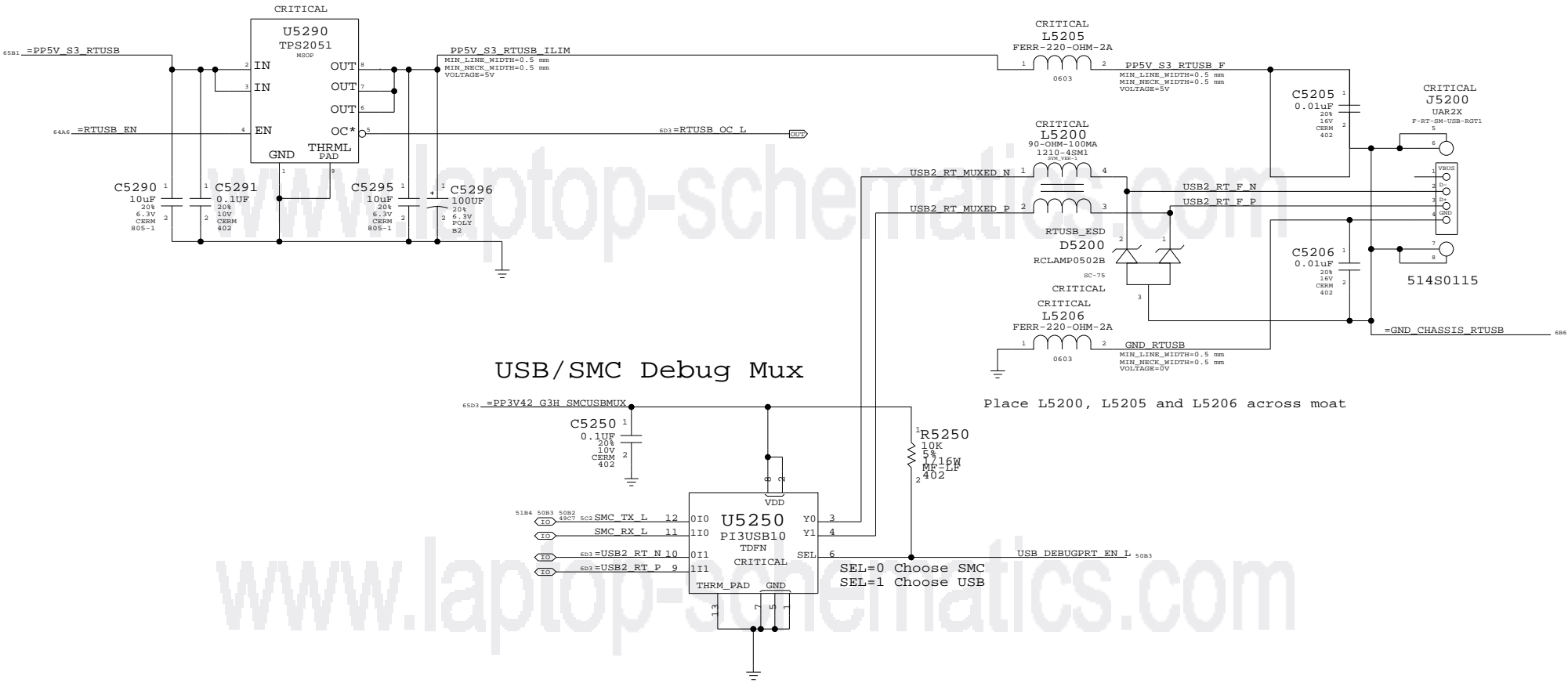
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	SCALE NONE	SHT 49	OF 105

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Port Power Switch

Right USB Port



External USB Connector

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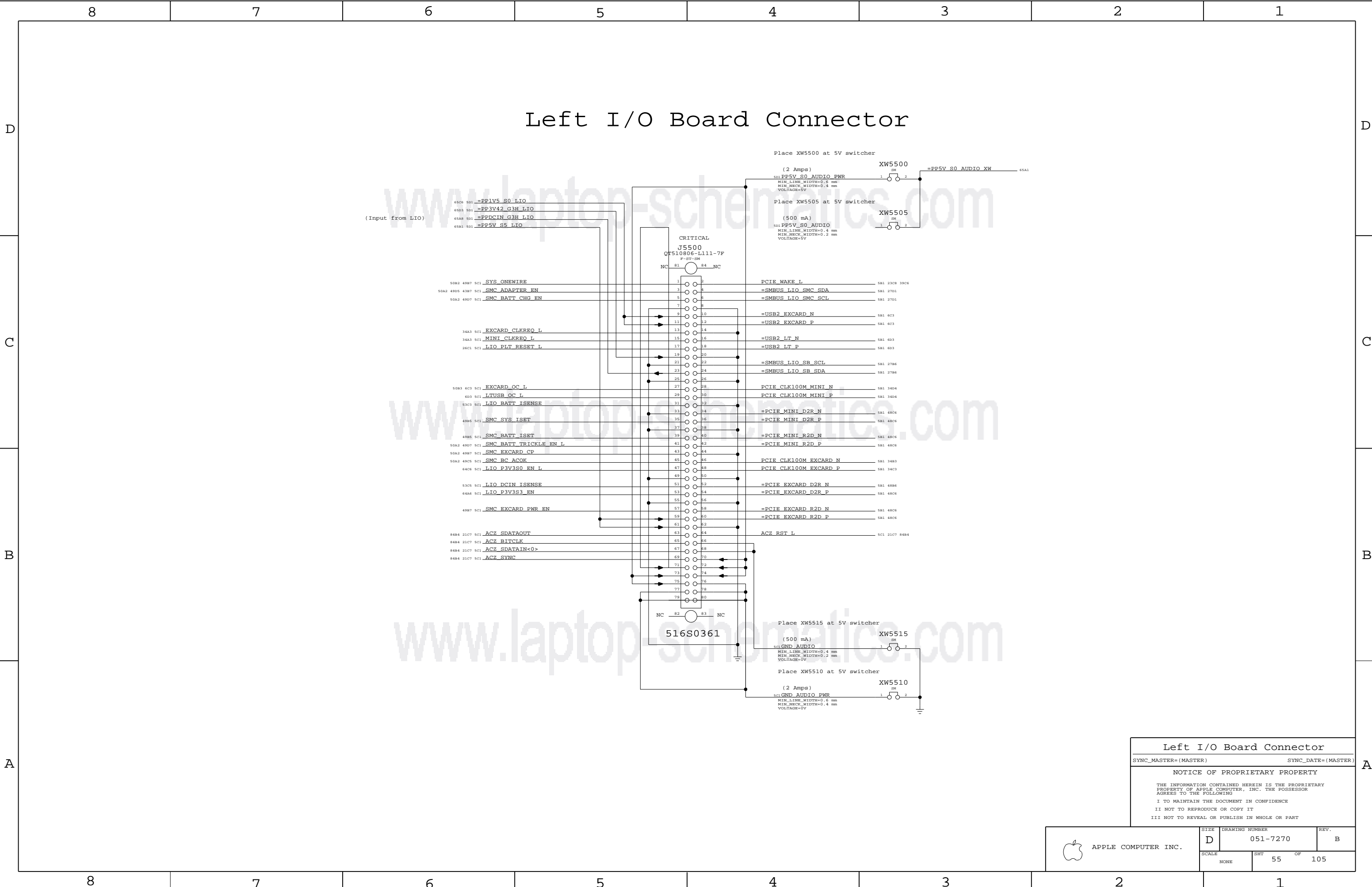
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	D	051-7270	B
SCALE		SHT	OF
NONE		52	105





Left I/O Board Connector

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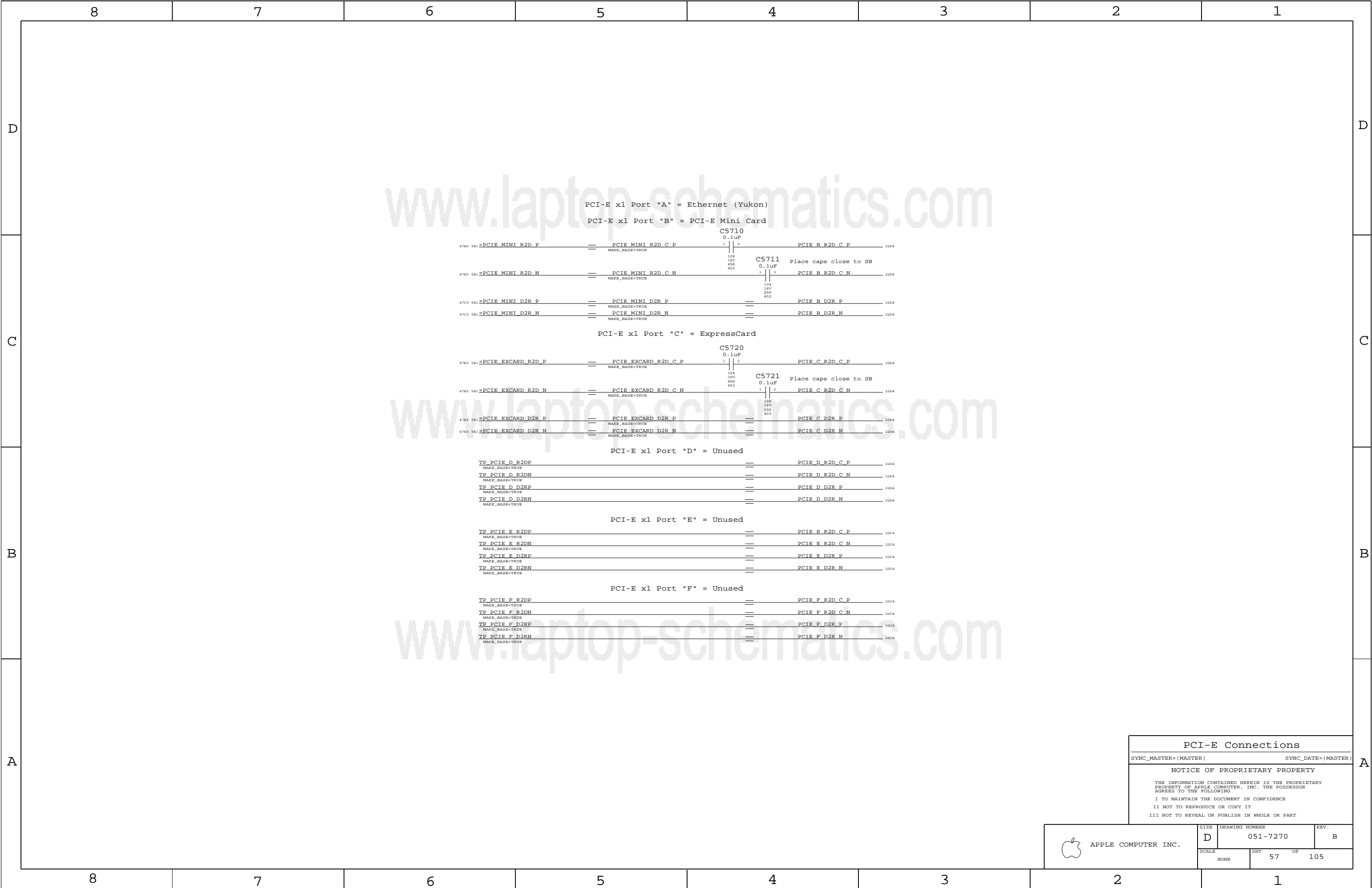
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NONE		55	105



PCI-E Connections

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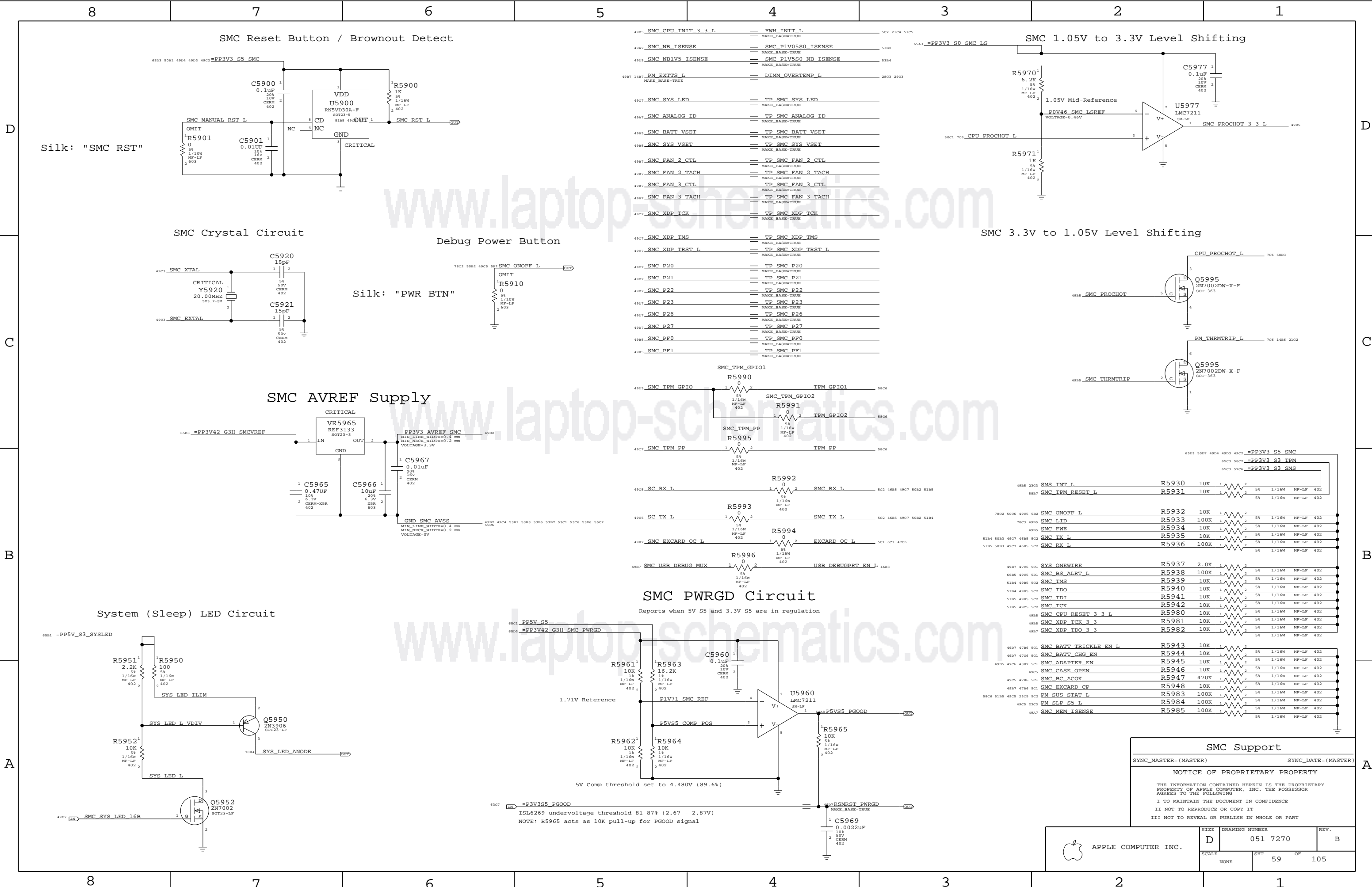
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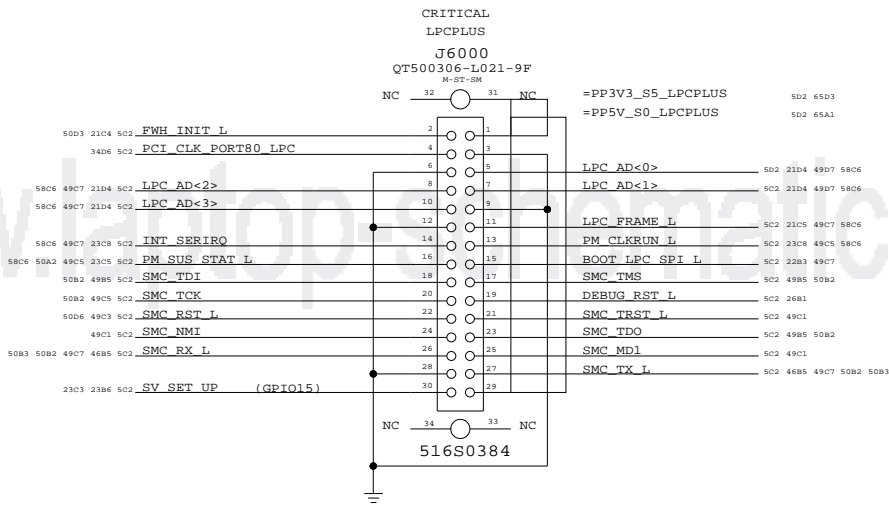




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LPC+ Debug Connector

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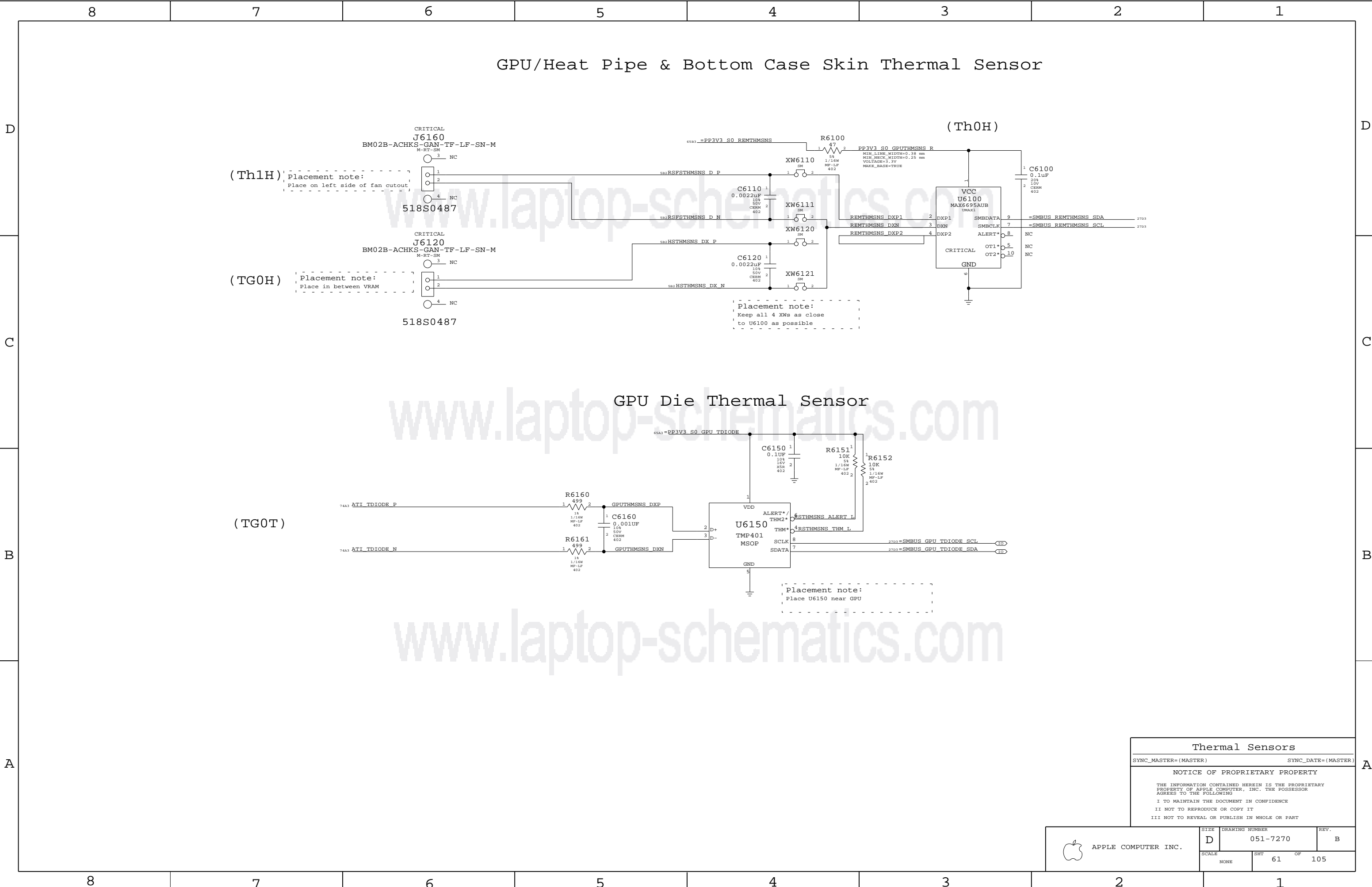
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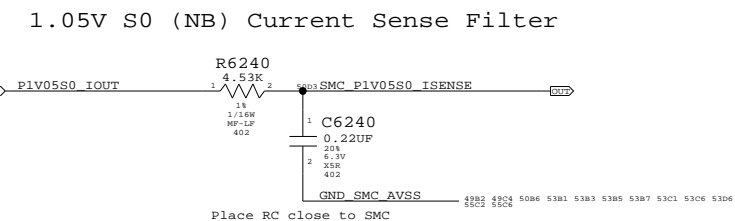
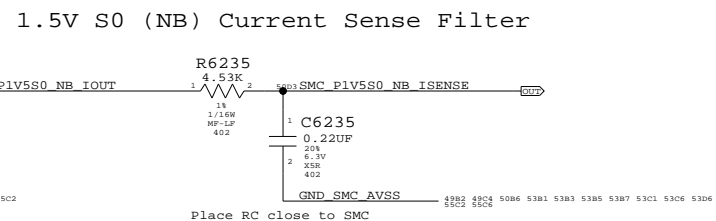
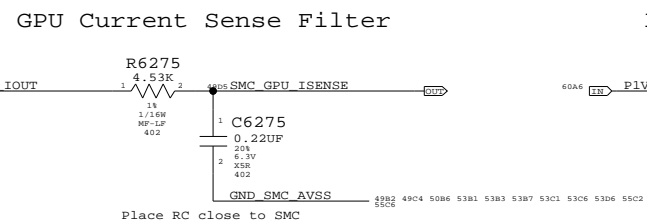
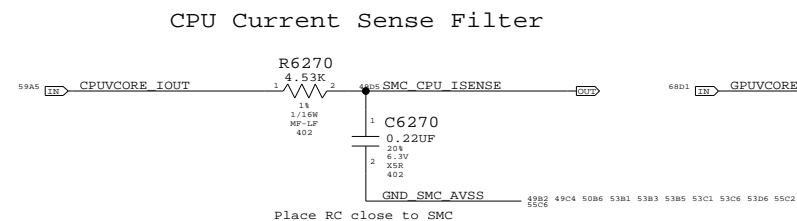
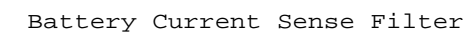
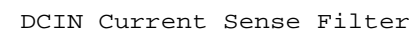
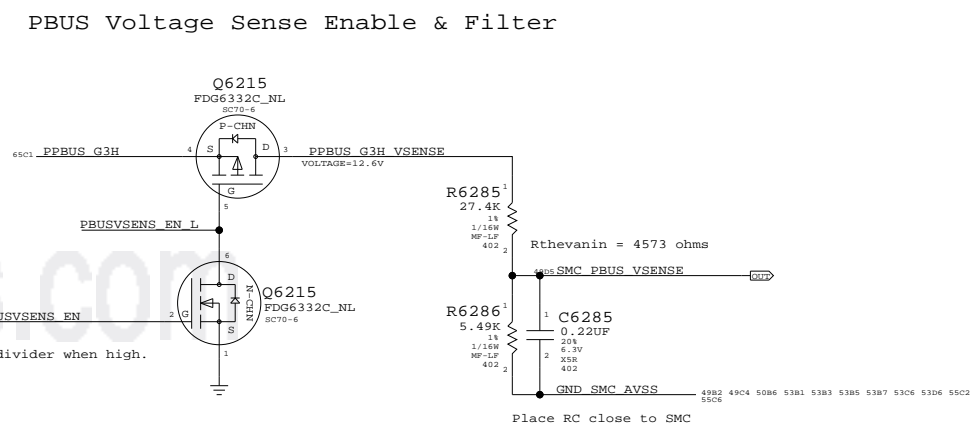
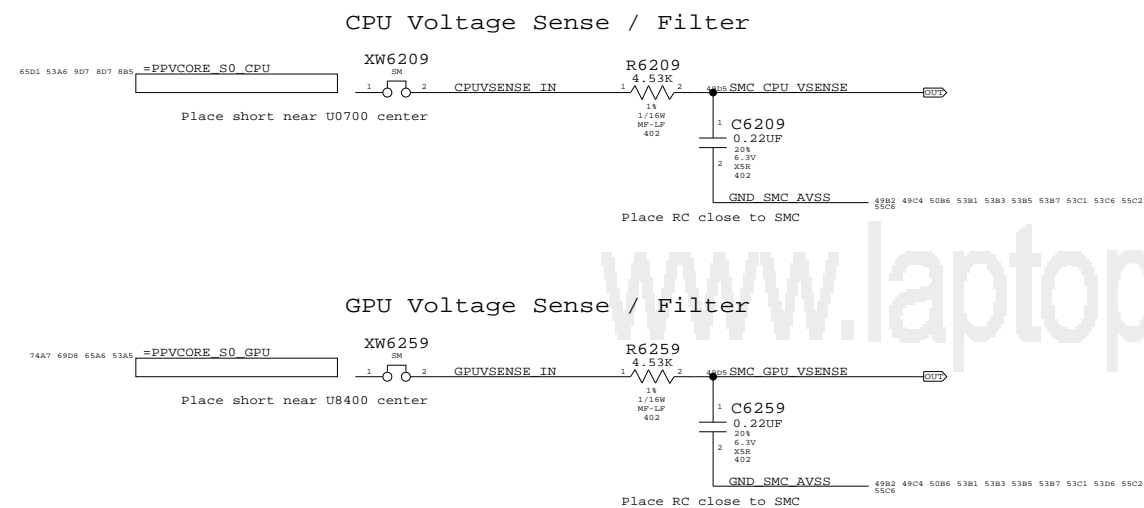


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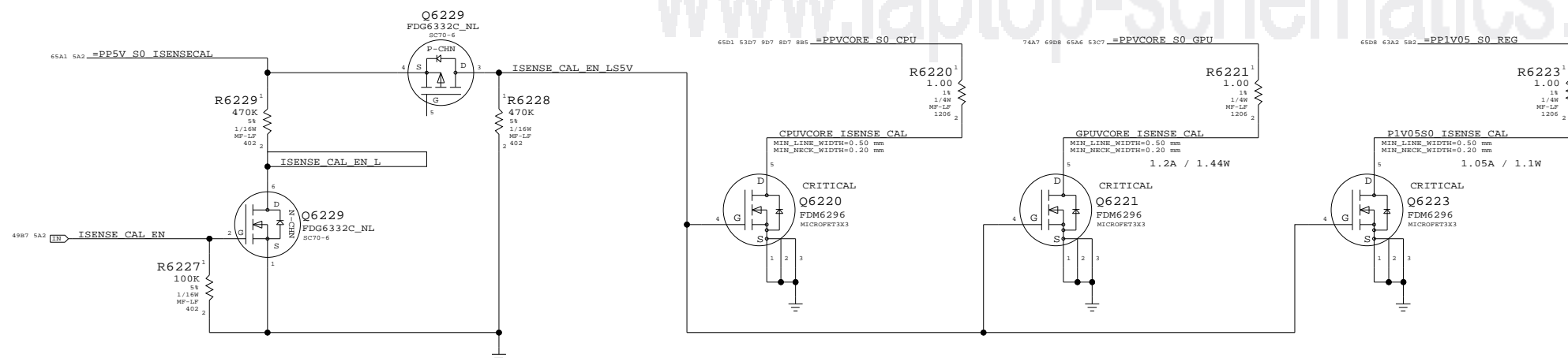
SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE	SHT	OF
NONE	60	105



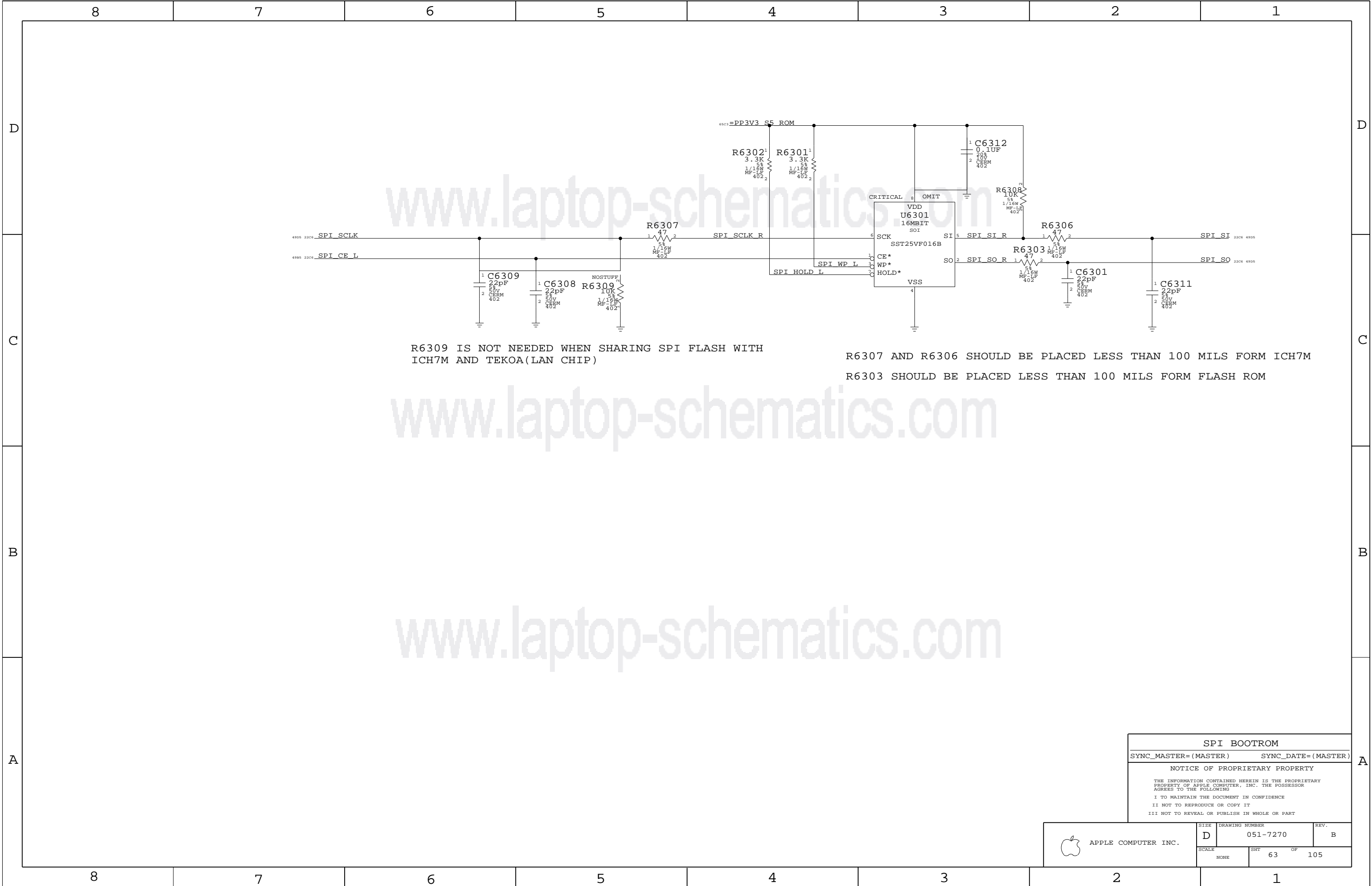


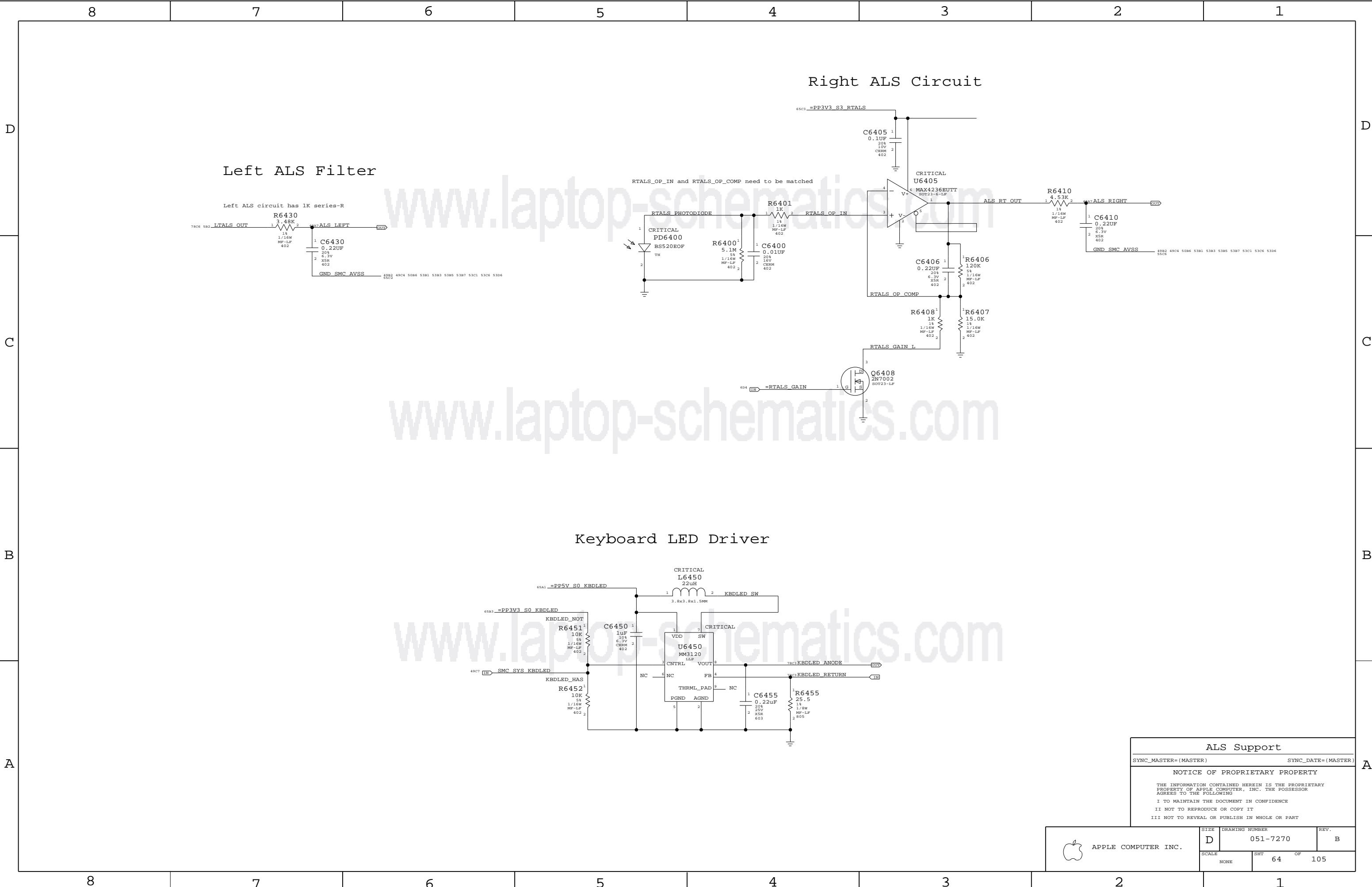


Switches in fixed load on power supplies to calibrate current sense circuits



Current & Voltage Sensing	
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ALS Support

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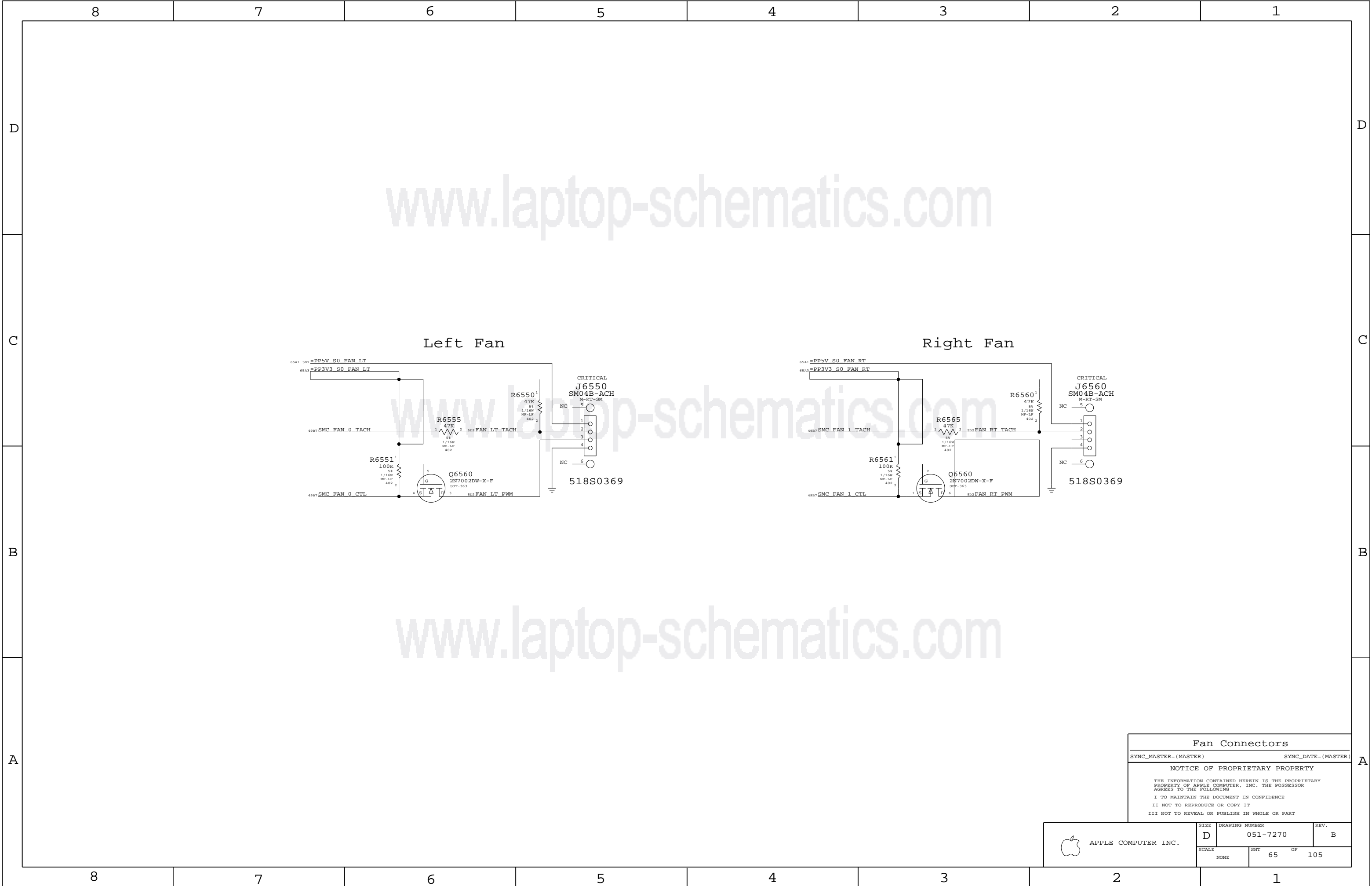
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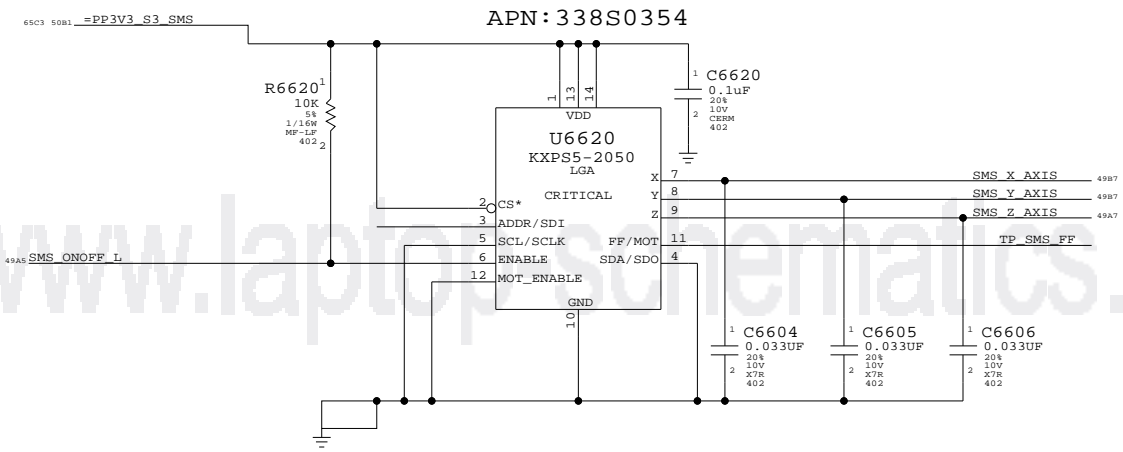
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	SCALE NONE	SHT 64	OF 105



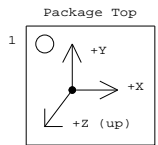
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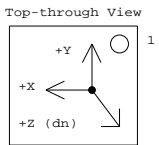
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Desired orientation when  
placed on board top-side:



Desired orientation when  
placed on board bottom-side:



M59 placement: Bottom-side

Sudden Motion Sensor (SMS)

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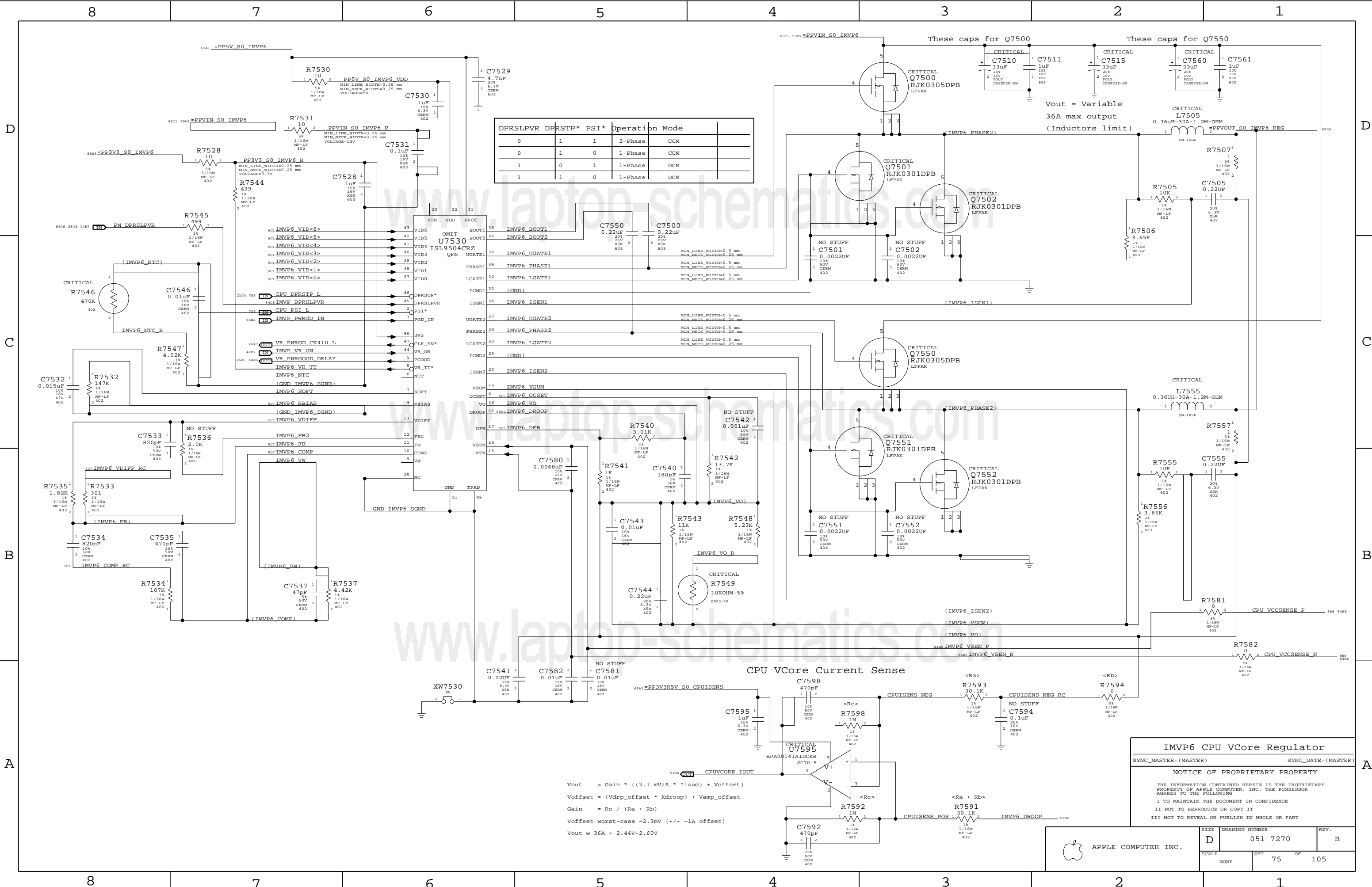
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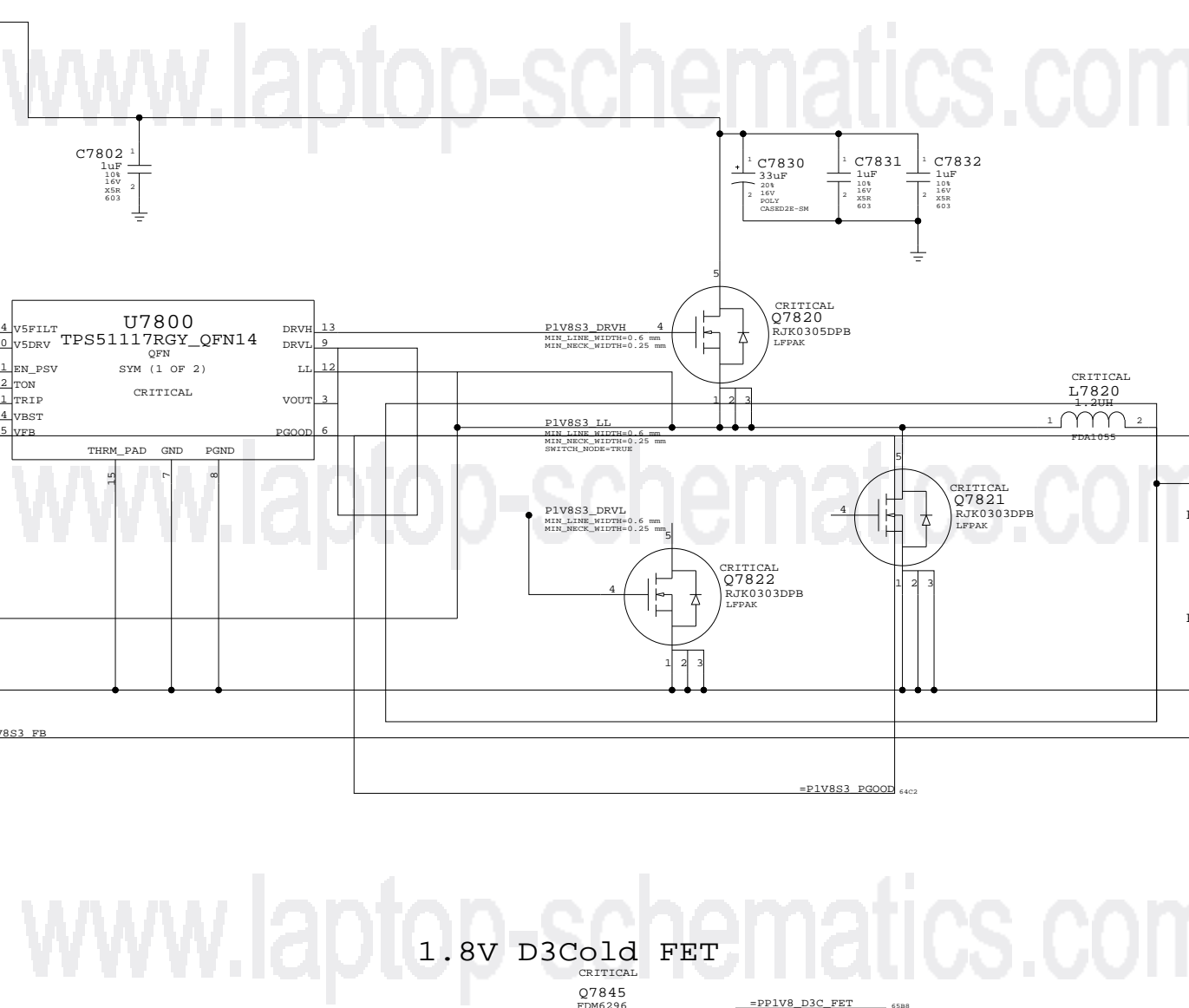


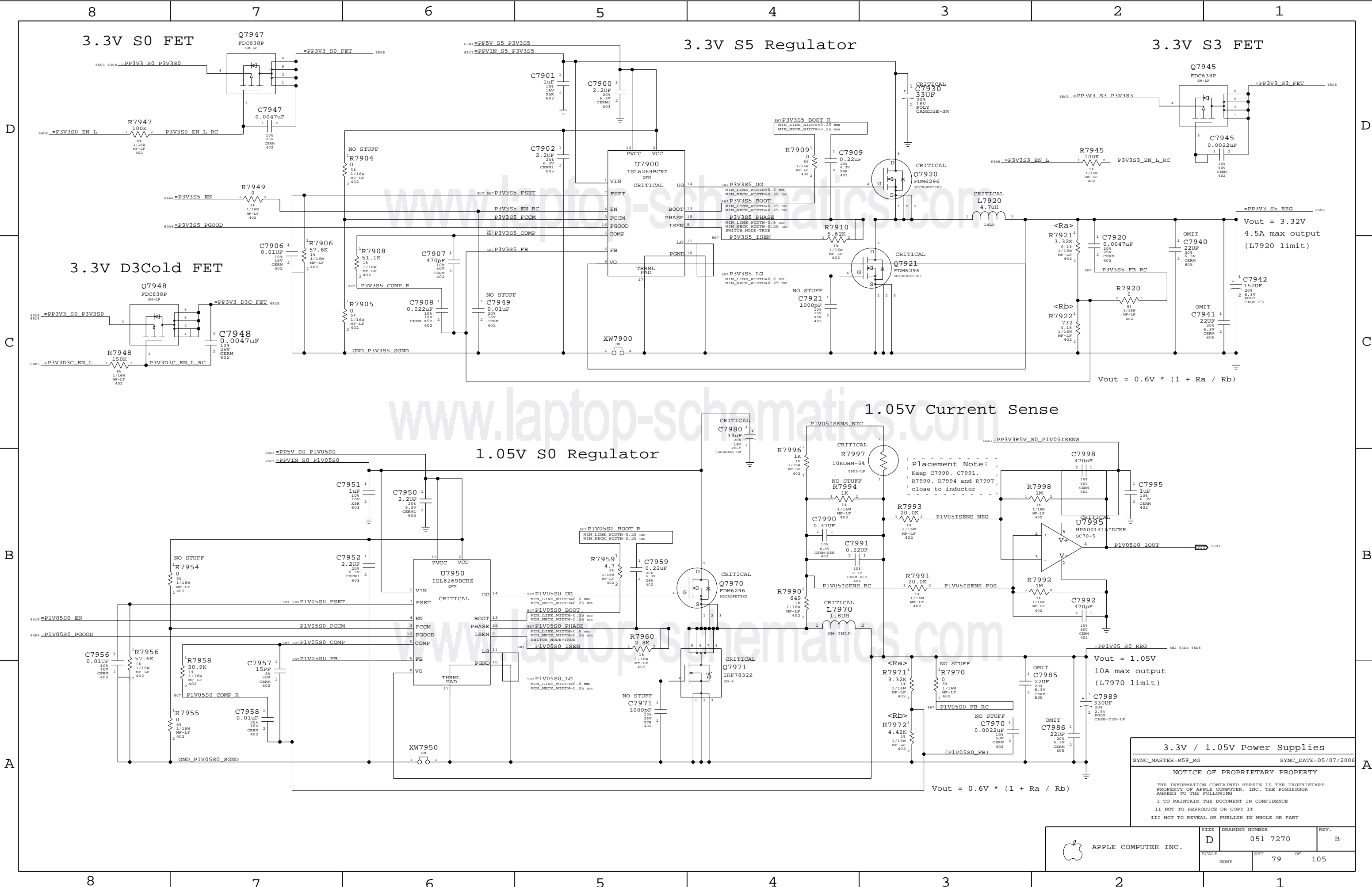






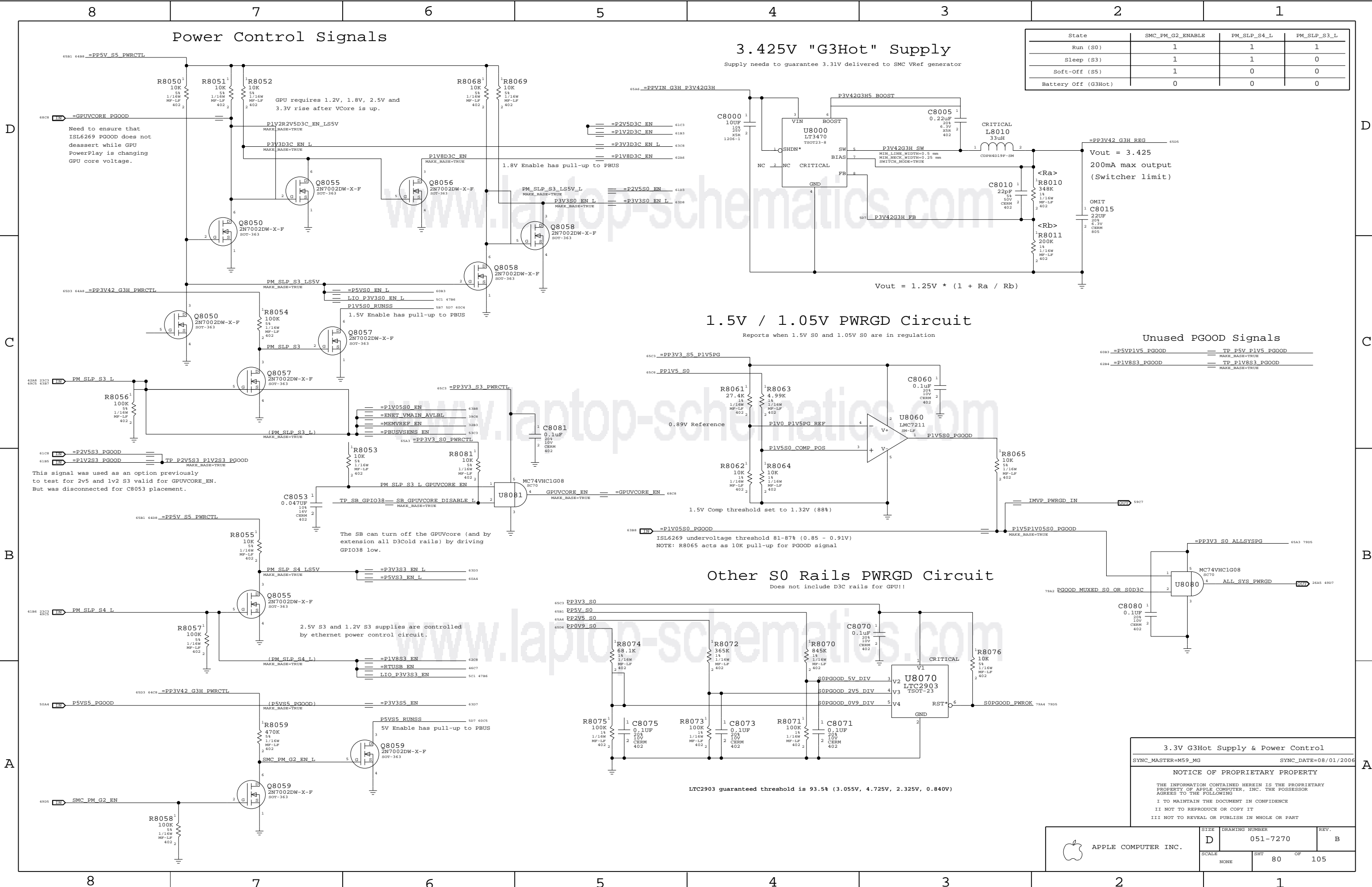






3.3V / 1.05V Power Supplies		
SYNC_MASTER=M59_MG		SYNC_DATE=05/07/2006
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	D	051-7270	B
SCALE		SHT	79 OF 105
NONE			



State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

### 3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

Vout = 3.425  
200mA max output  
(Switcher limit)

$$V_{out} = 1.25V * (1 + R_a / R_b)$$

### 1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

#### Unused PGOOD Signals

6081 =P5VP1V5 PGOOD	TP P5V P1V5 PGOOD
6284 =P1V8S3 PGOOD	TP P1V8S3 PGOOD
	MAKE_BASE=TRUE

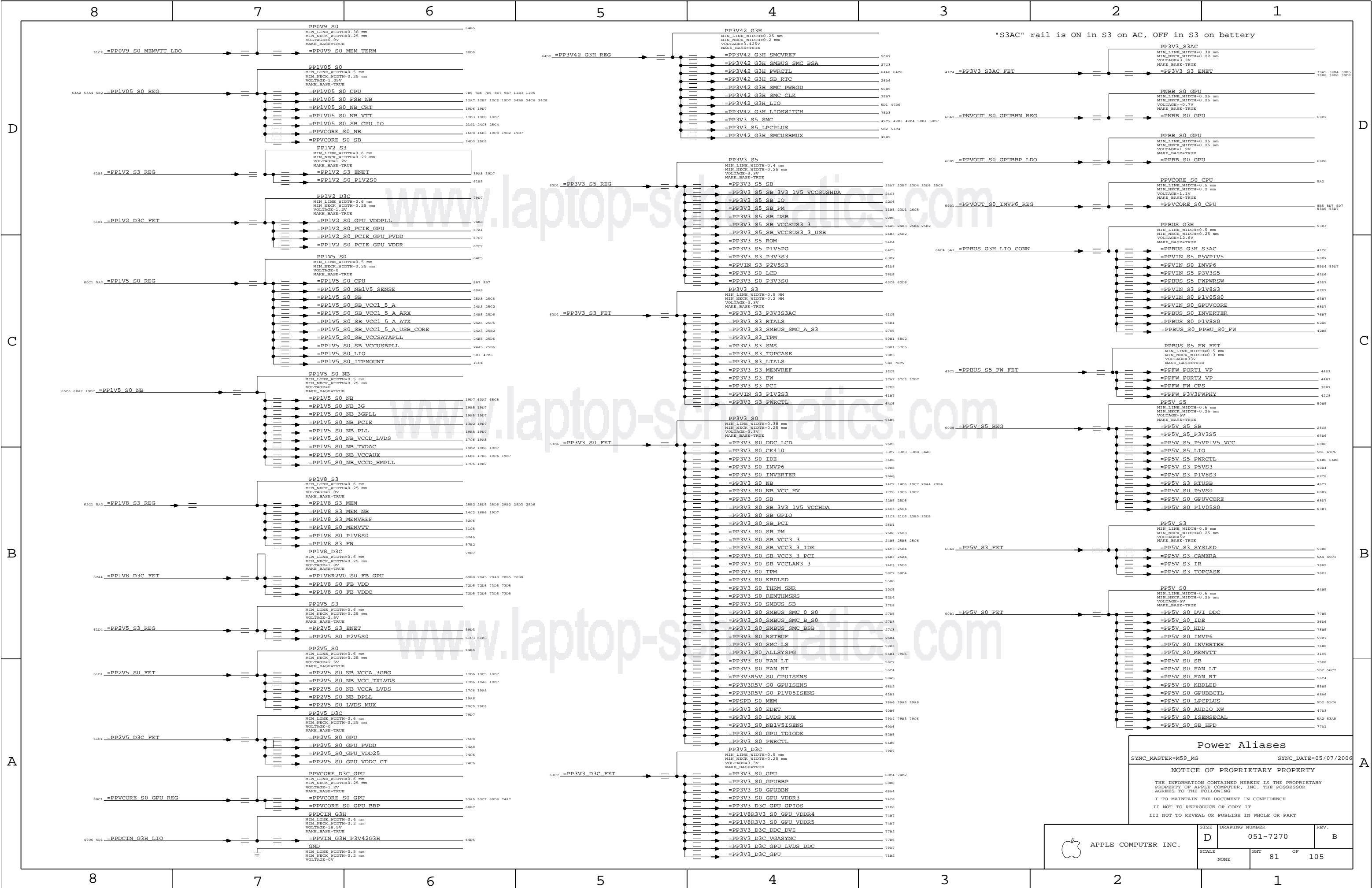
### Other S0 Rails PWRGD Circuit

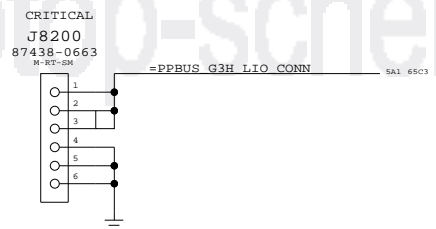
Does not include D3C rails for GPU!!

3.3V G3Hot Supply & Power Control	
SYNC_MASTER=M59_MG	SYNC_DATE=08/01/2006
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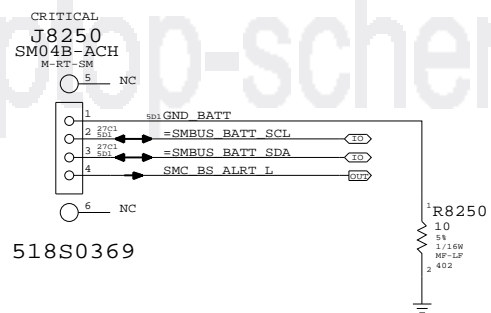
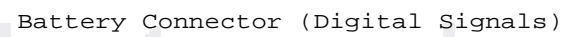
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	SCALE NONE	SHT 80	OF 105







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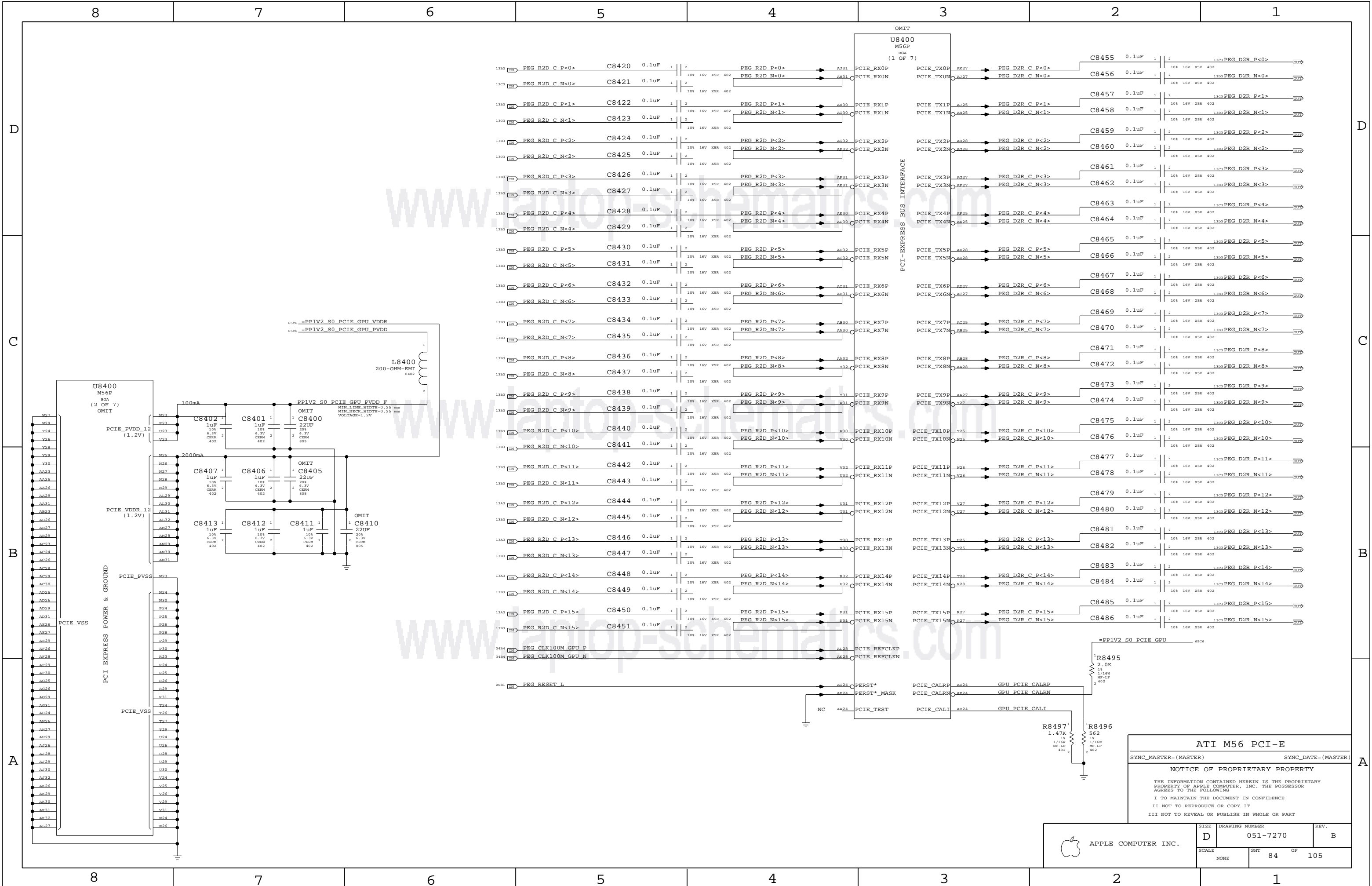


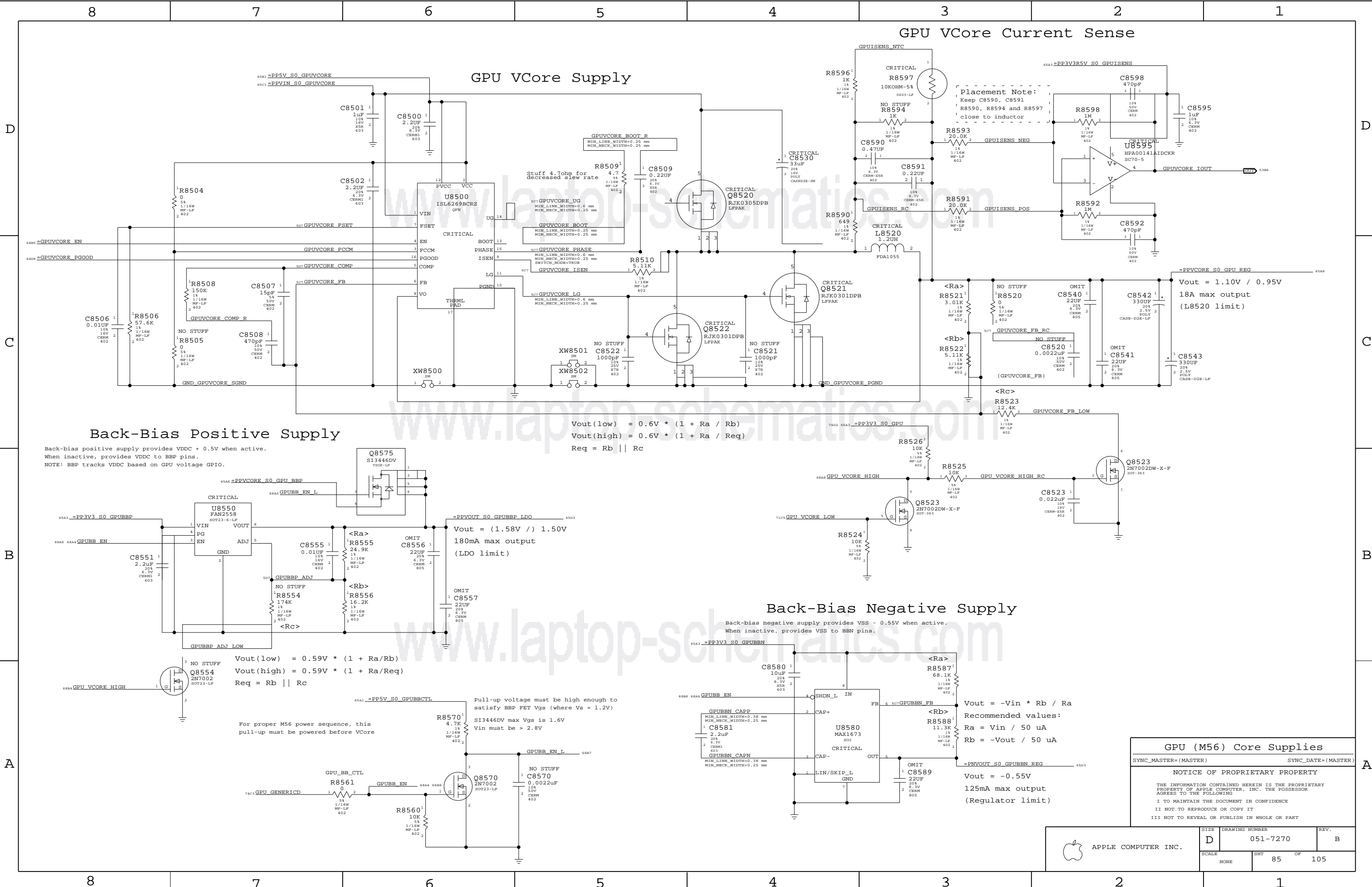
518S0369

PBus-In, Batt. & 3G Pwr Connectors	
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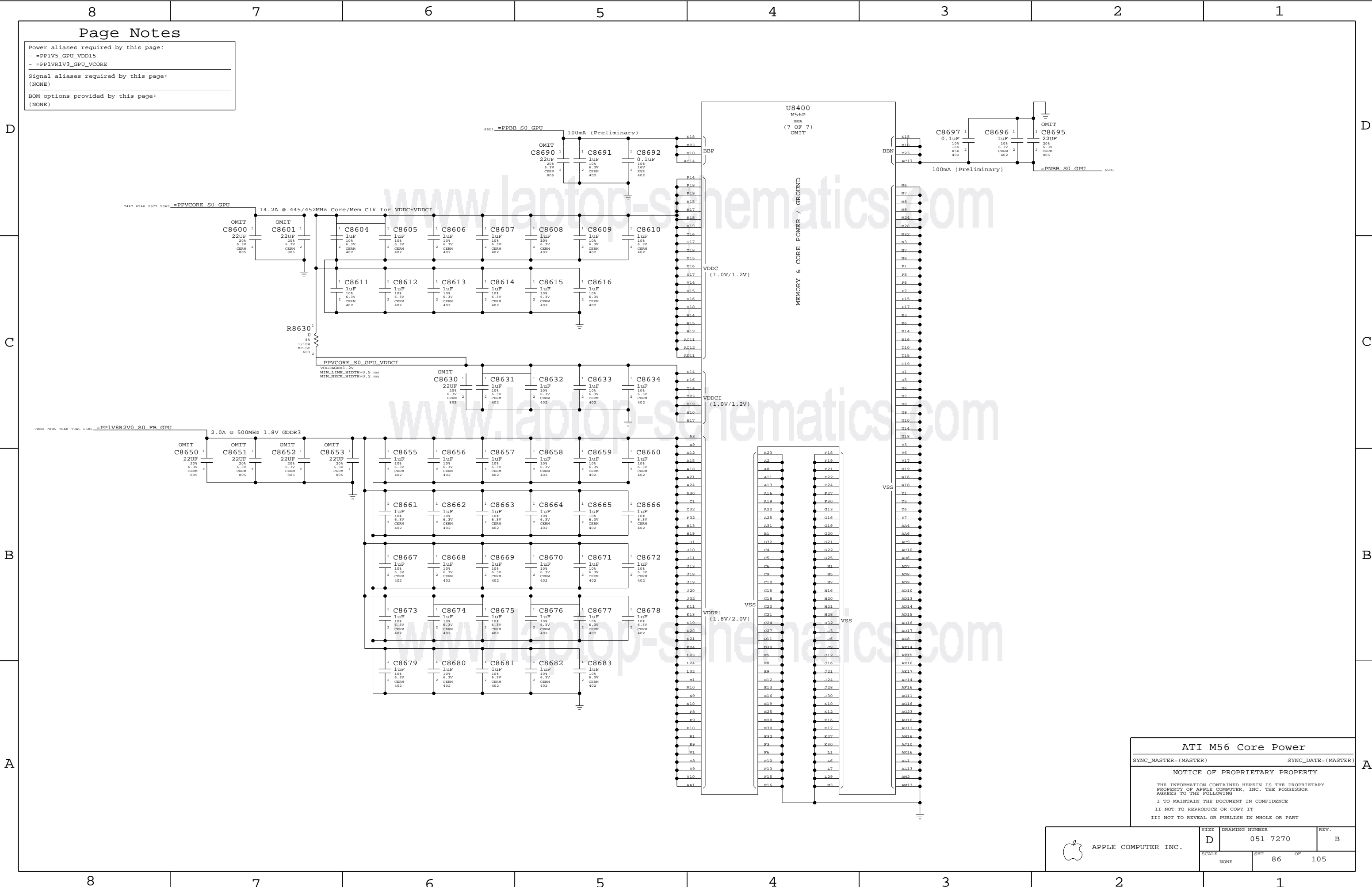
SIZE D	DRAWING NUMBER 051-7270	REV. B
SCALE NONE	SHT 82	OF 105





GPU (M56) Core Supplies		
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SCALE		SHT	OF
NONE		85	105



Page Notes

Power aliases required by this page:  
- =PP1V5\_GPU\_VDD15  
- =PP1VR1V3\_GPU\_VCORE

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)

ATI M56 Core Power

SYNC\_MASTER=(MASTER)SYNC\_DATE=(MASTER)

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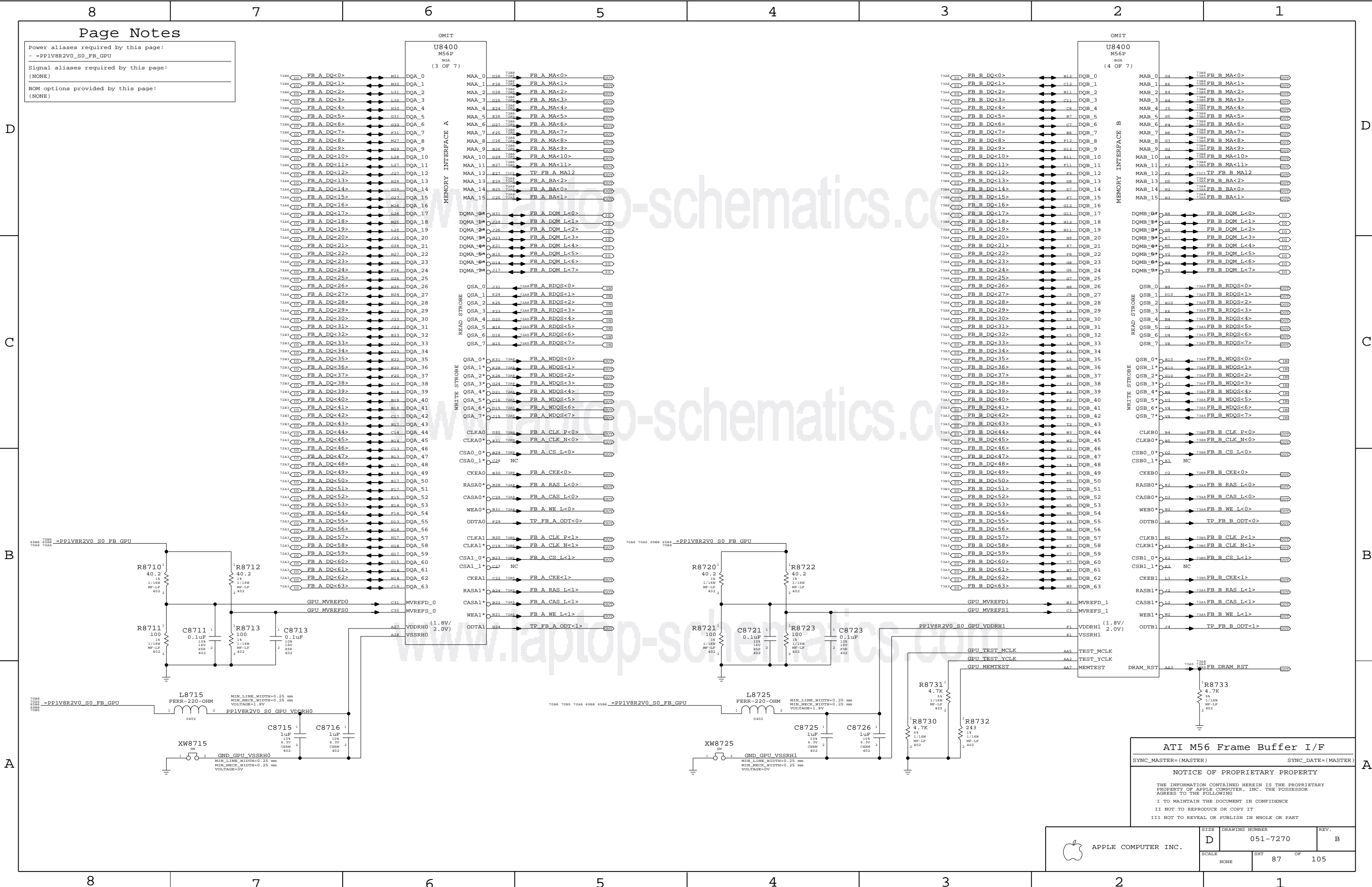
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SCALE		SHT	OF
NONE		86	105





**Page Notes**

Power aliases required by this page:  
- =PPIV8R2V0\_S0\_FB\_GPU

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)

**ATI M56 Frame Buffer I/F**

SYNC\_MASTER=(MASTER)      SYNC\_DATE=(MASTER)

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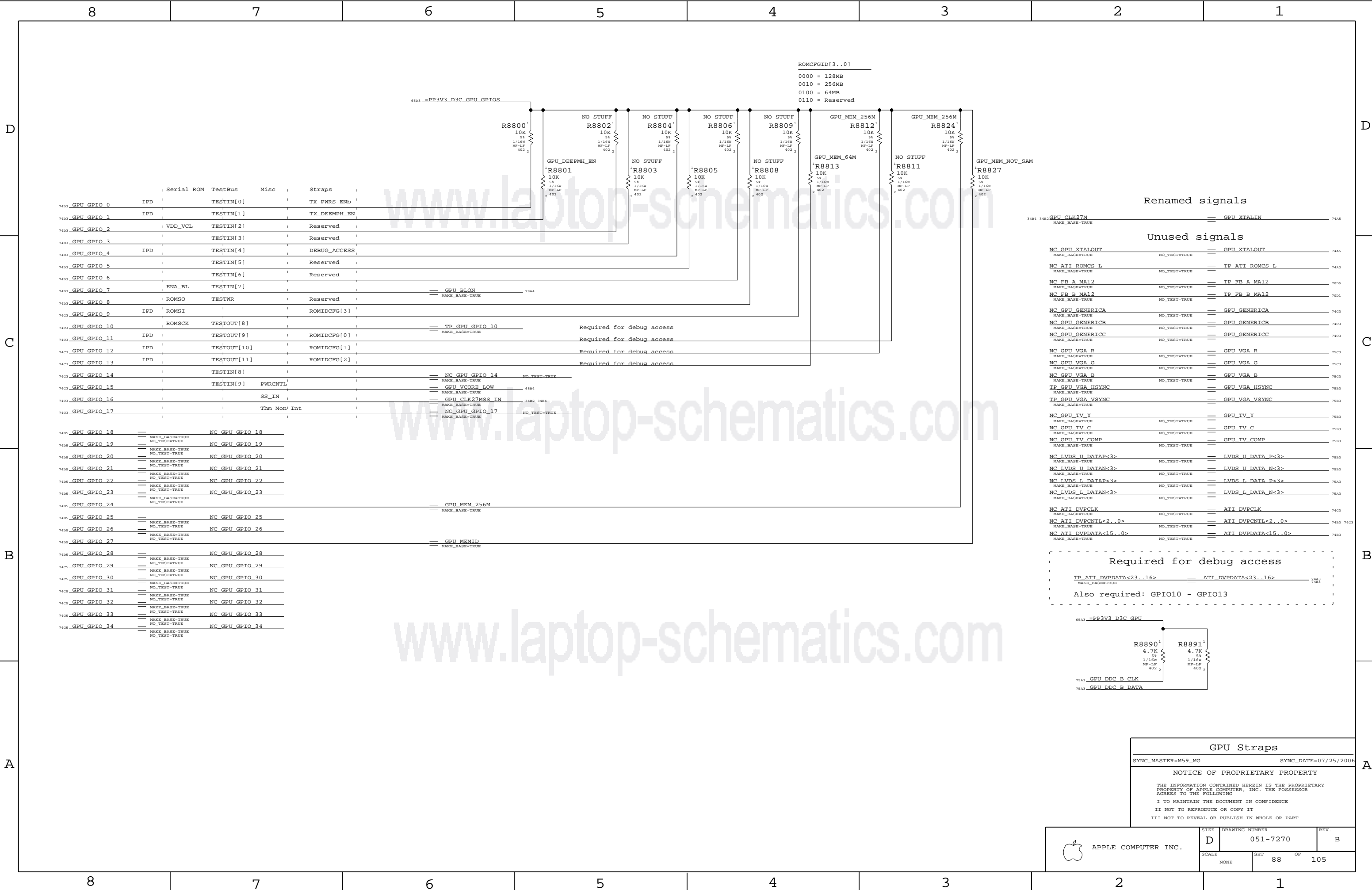
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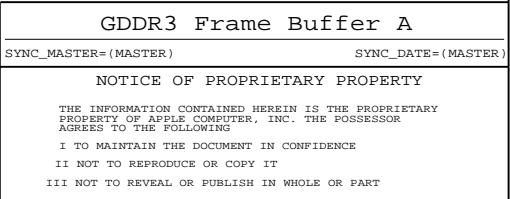
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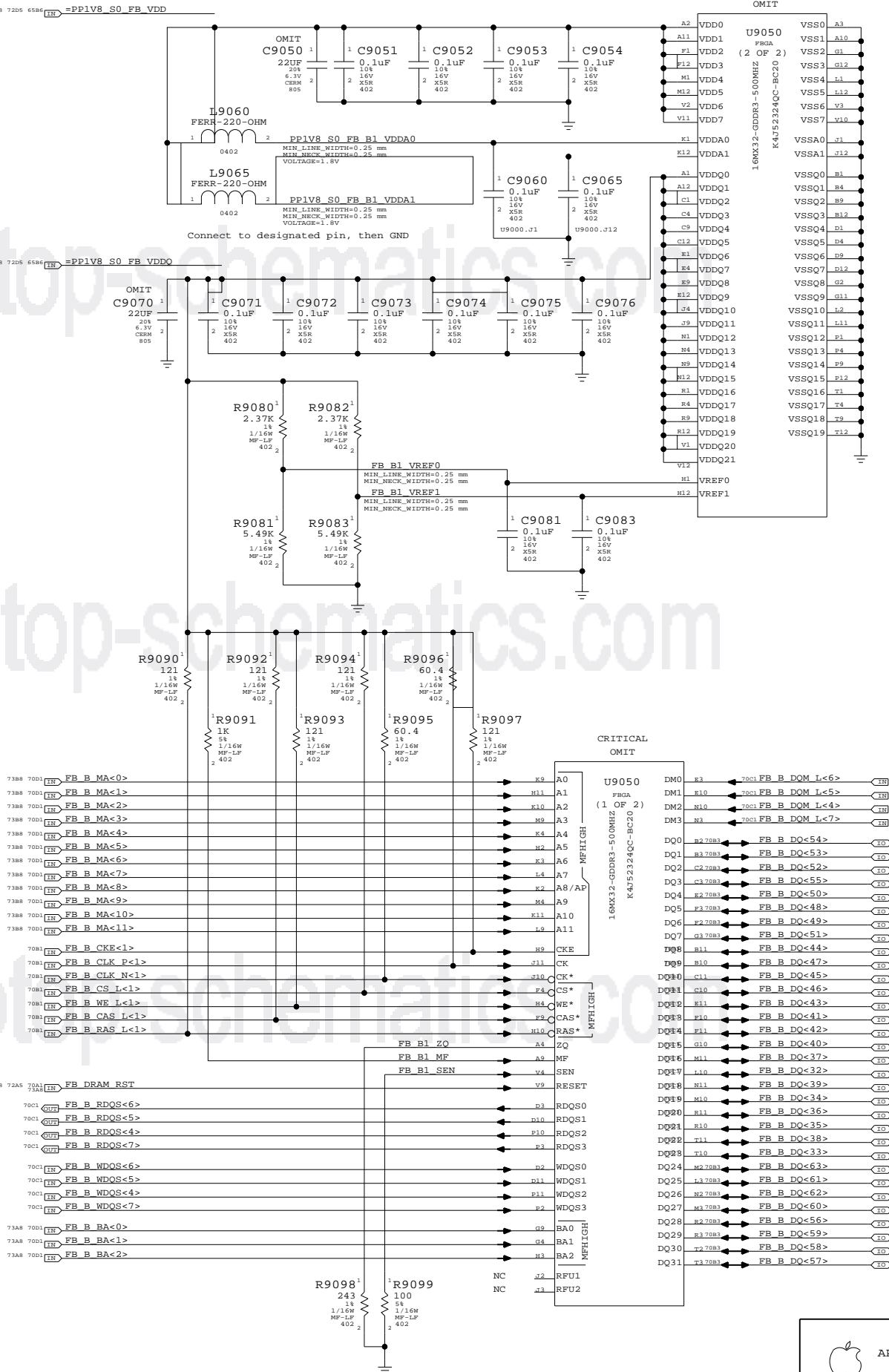
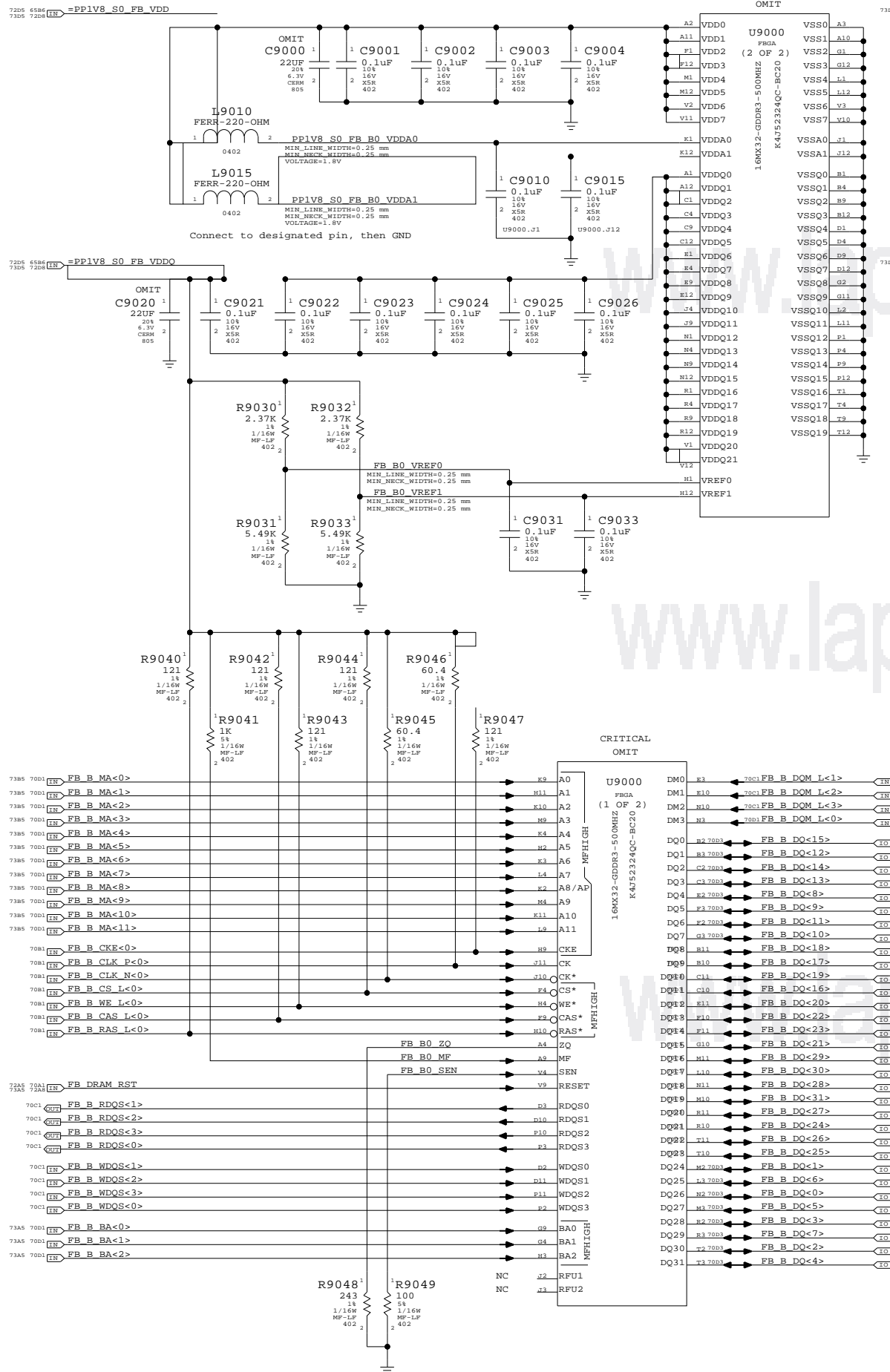




Power aliases required by this page:  
 - =PPIV8\_S0\_FB\_VDD  
 - =PPIV8\_S0\_FB\_VDDQ

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)



**GDDR3 Frame Buffer B**

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NONE	90	105

## Page Notes

Power aliases required by this page:

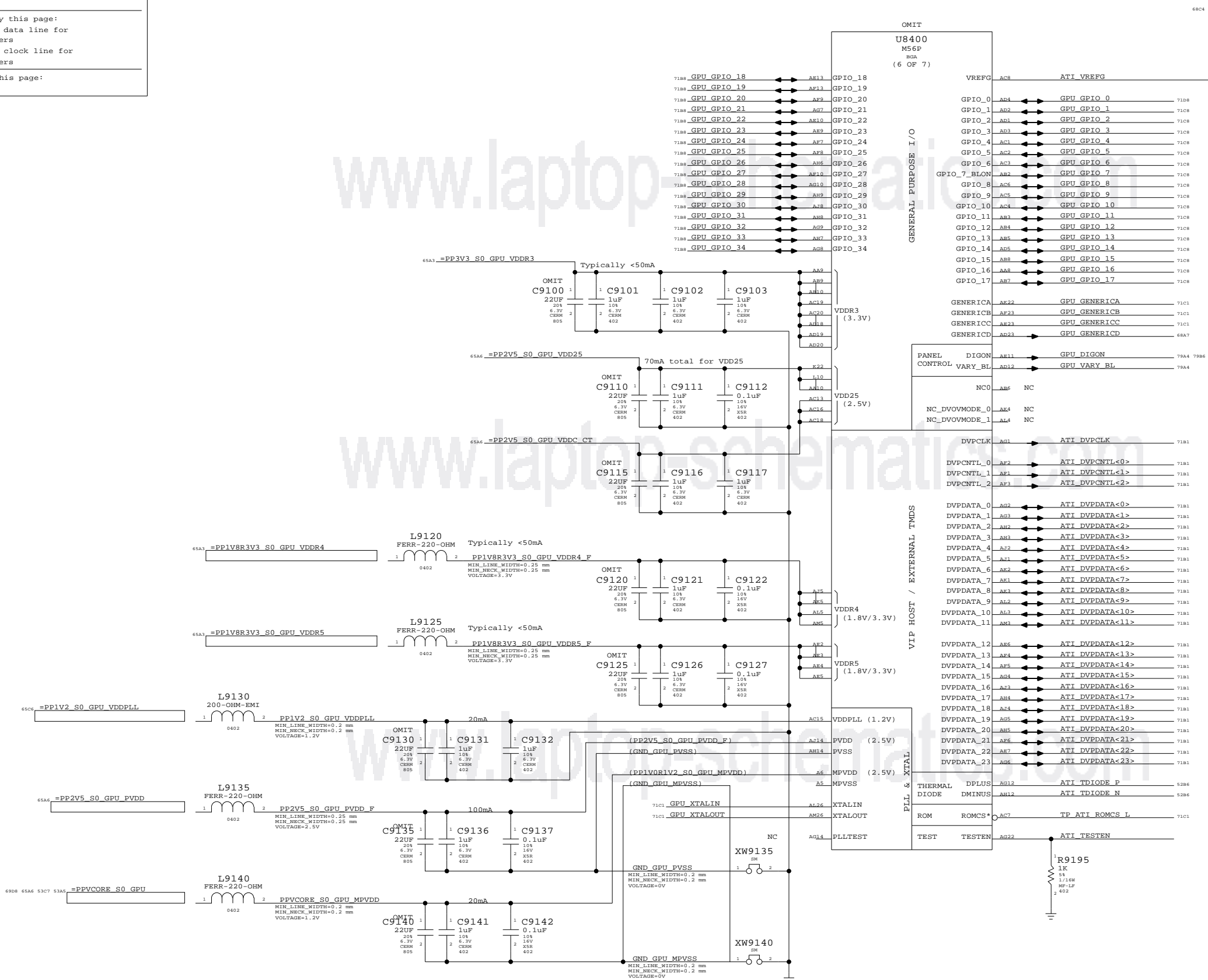
- =PP3V3\_GPU\_GPIOS  
- =PP2V5\_PVDD  
- =PP1V8\_GPU\_LVDS\_PLL

Signal aliases required by this page:

- =I2C\_GPU\_TMDS\_SDA - I2C data line for  
external TMDS transmitters  
- =I2C\_GPU\_TMDS\_SCL - I2C clock line for  
external TMDS transmitters

BOM options provided by this page:

(NONE)



## ATI M56 GPIO/DVO/Misc

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SIZE D DRAWING NUMBER 051-7270 REV. B

SCALE NONE SHT 91 OF 105



## Page Notes

Power aliases required by this page:

```
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR
```

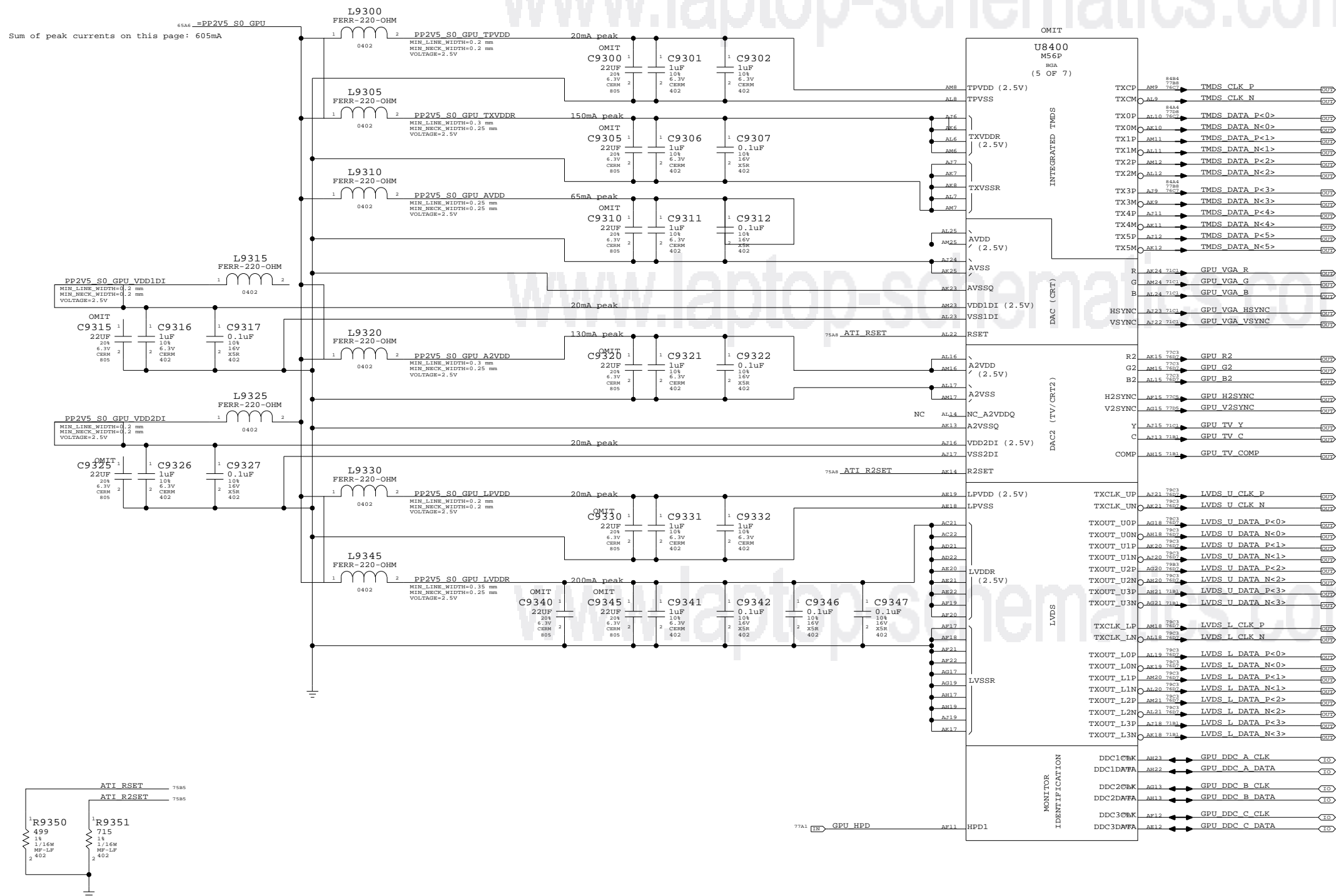
---

Signal aliases required by this page:

( NONE )

BOM options provided by this page:

( NONE )



Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

## ATI M56 Video Interfaces

```
SYNC_MASTER=(MASTER)
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SYNC_DATE= ( MASTER )	7
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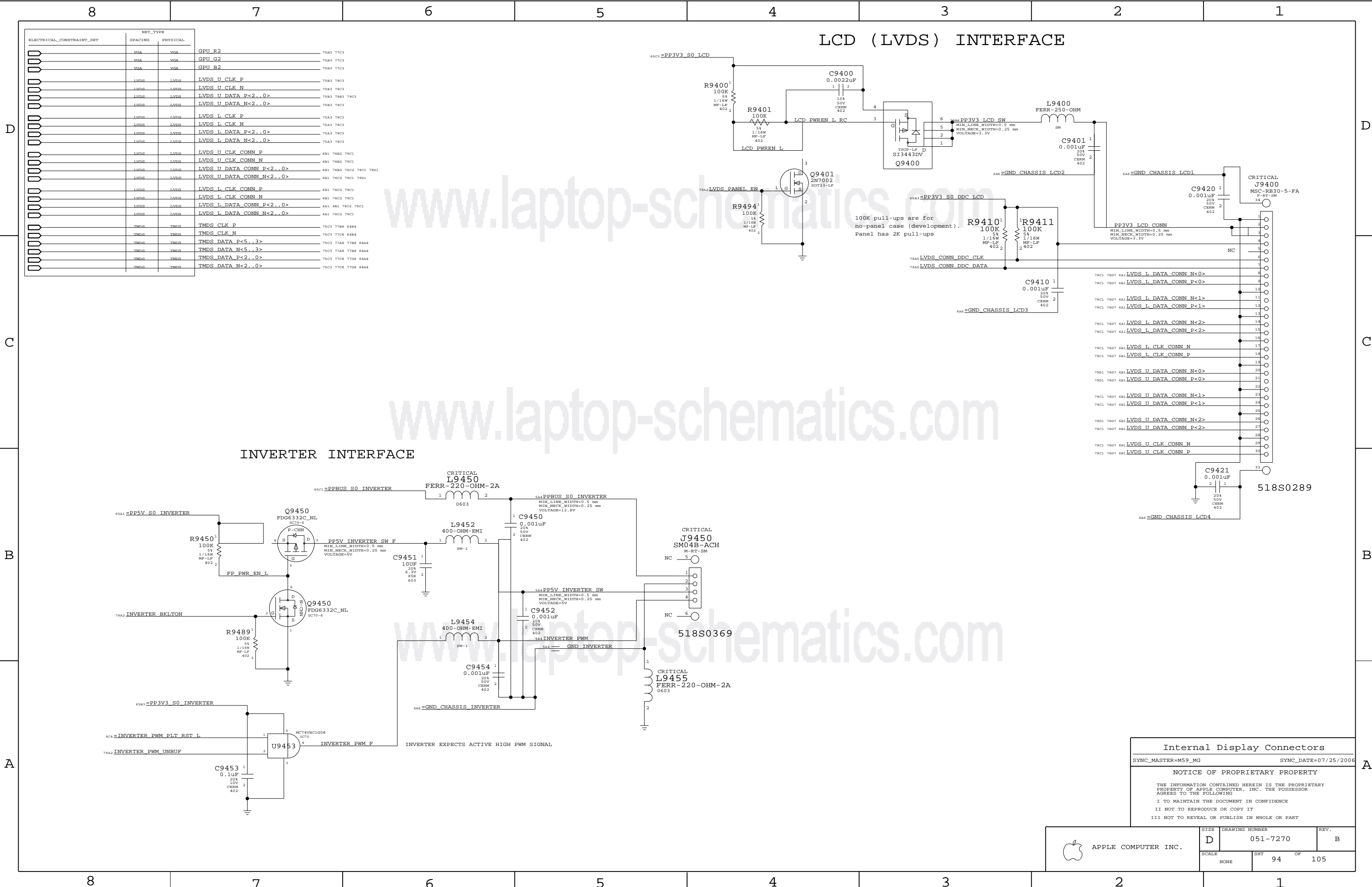
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SIZE	DRAWING NUMBER	REV.
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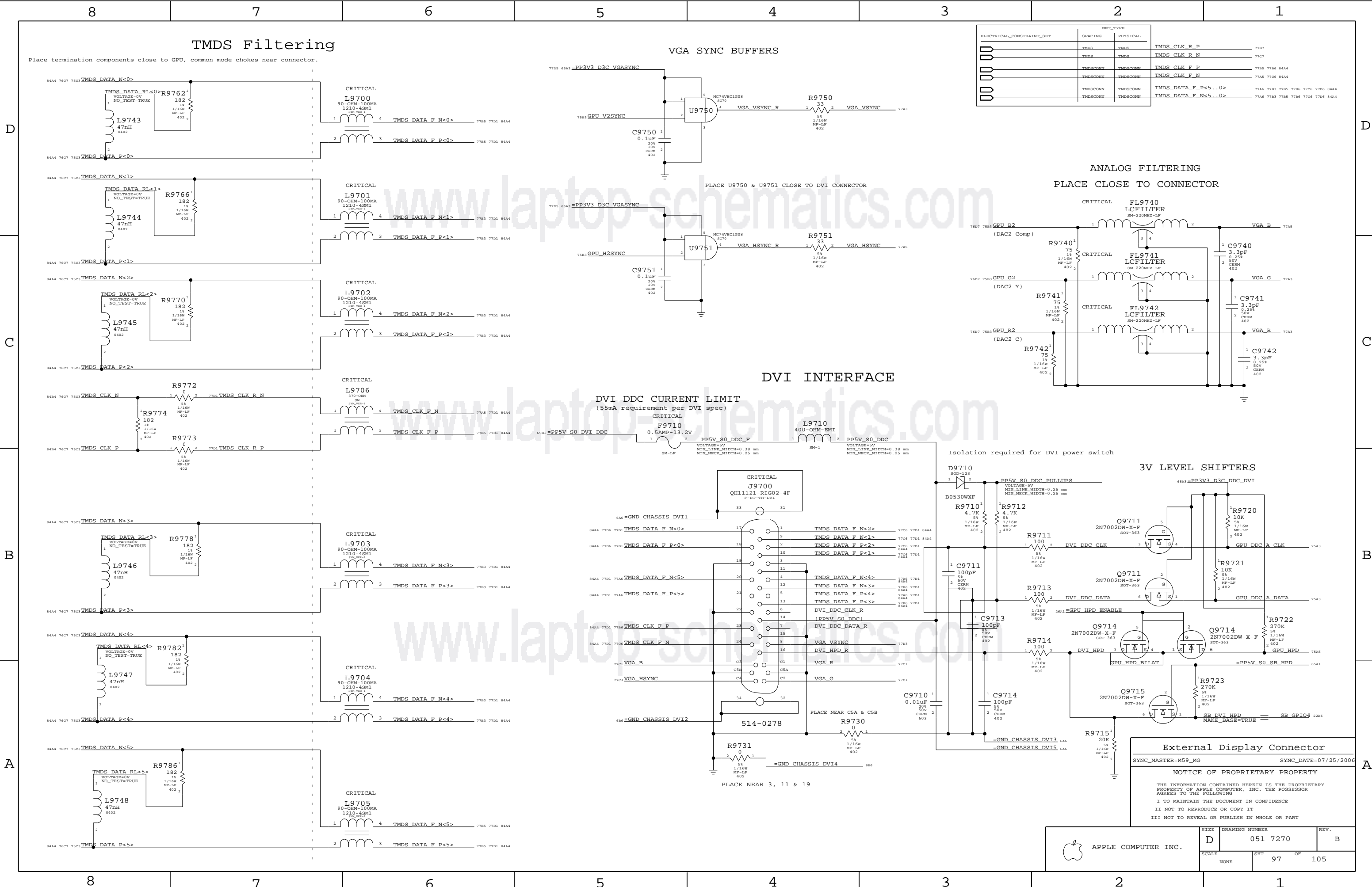
D	051-7270	E
---	----------	---

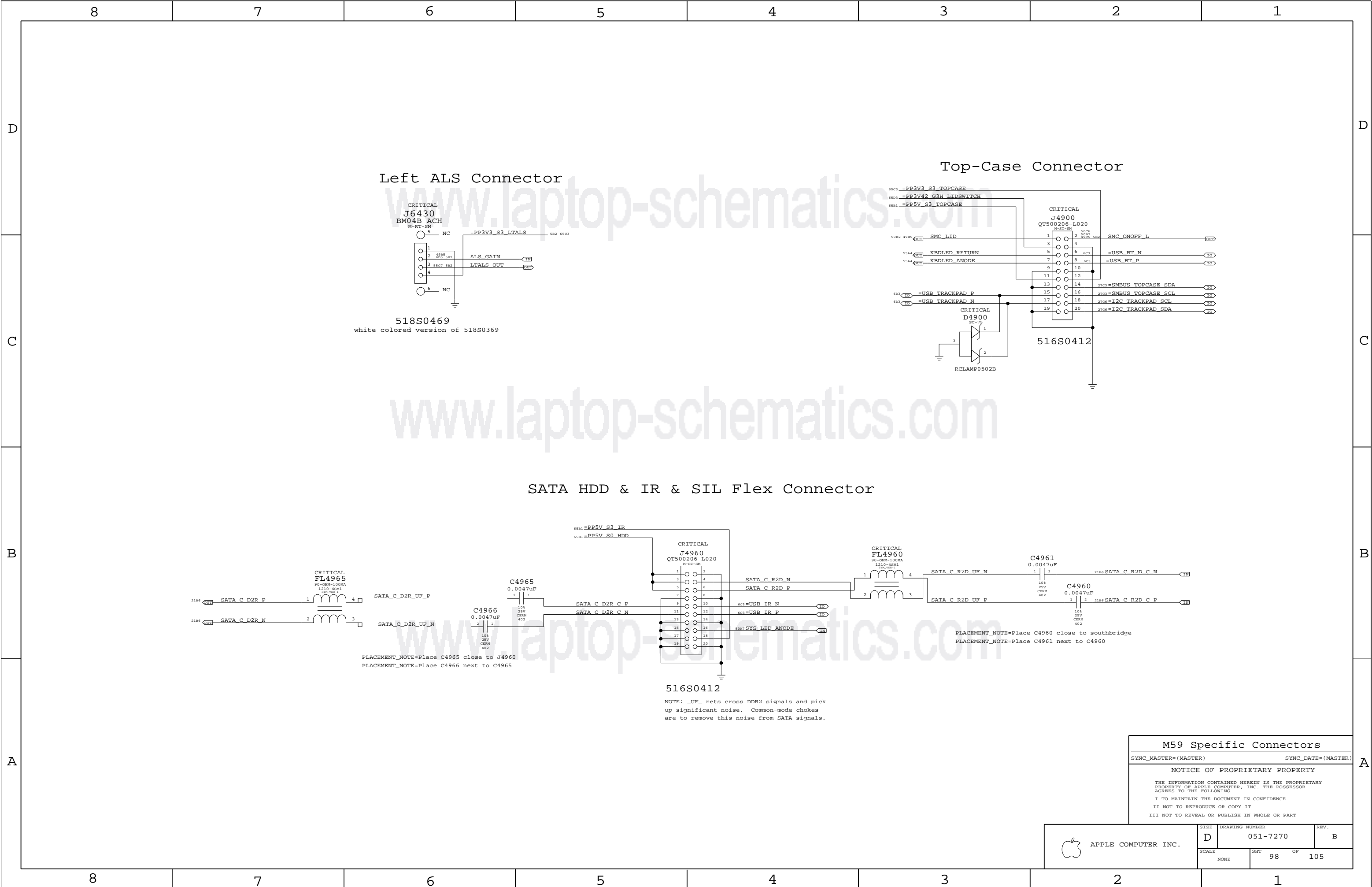
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SCALE	SHT	OF
	93	105



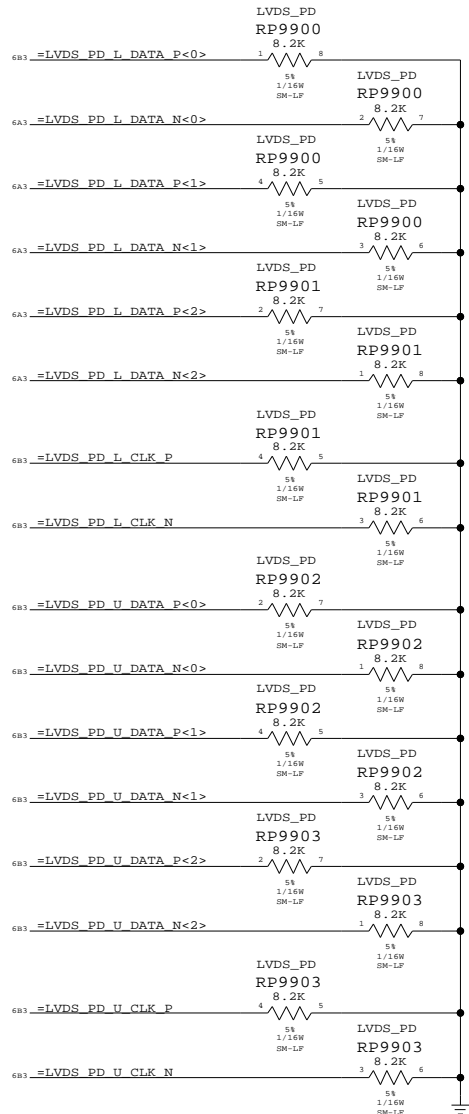






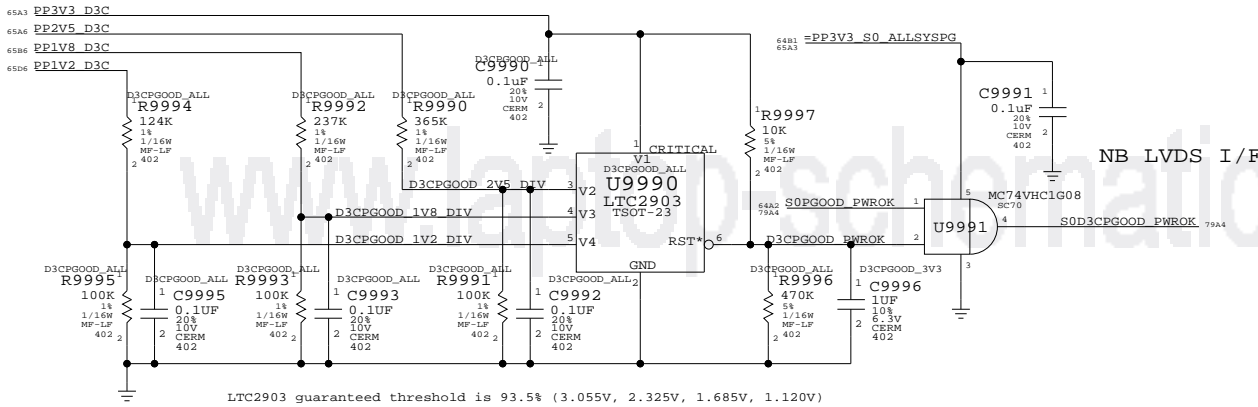
## LVDS Interface Pull-downs

NOTE: These parts are to counter an invalid state caused by the M56 part. Bias voltage is present on LVDS interface pins even when they should be tri-stated to meet panel power sequence requirements. Resulting pump-up in LCD panel can cause startup and long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be 0V.



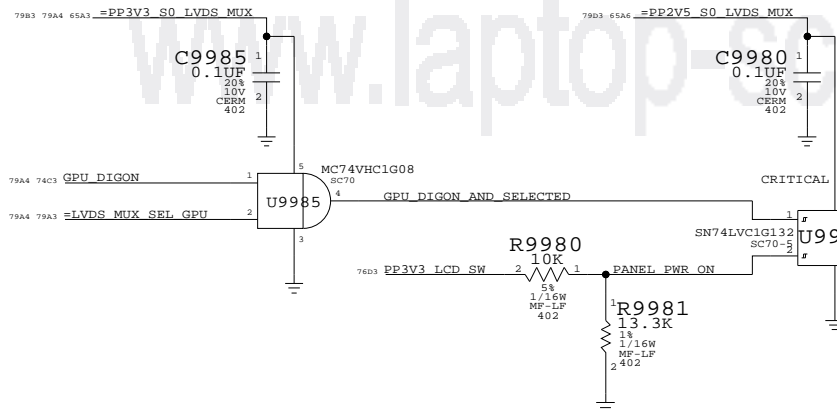
## PGOOD Monitor for GPU Rails

D3CPGOOD\_ALL BOM option stuffs LTC2903 circuit to monitor all D3C rails to qualify D3CPGOOD. D3CPGOOD\_3V3 BOM option uses only PP3V3\_D3C to qualify D3CPGOOD.



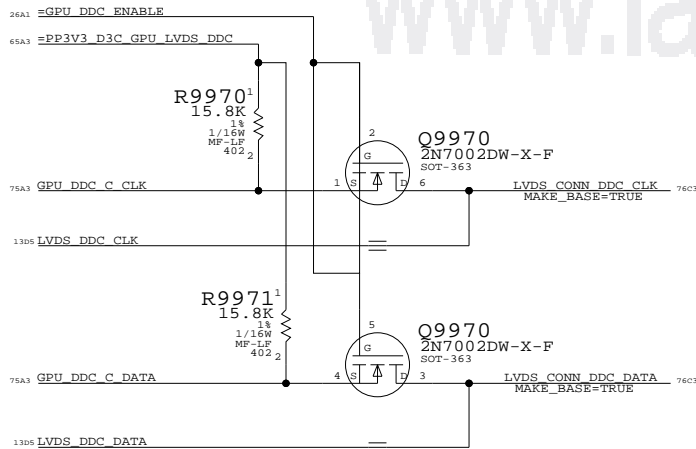
## LVDS Mux Selection Qualification

Enables the GPU LVDS path in the mux with the qualification that the GPU has turned on panel power and that the panel power has risen to (near) 3.3V. This should eliminate need for LVDS pulldowns

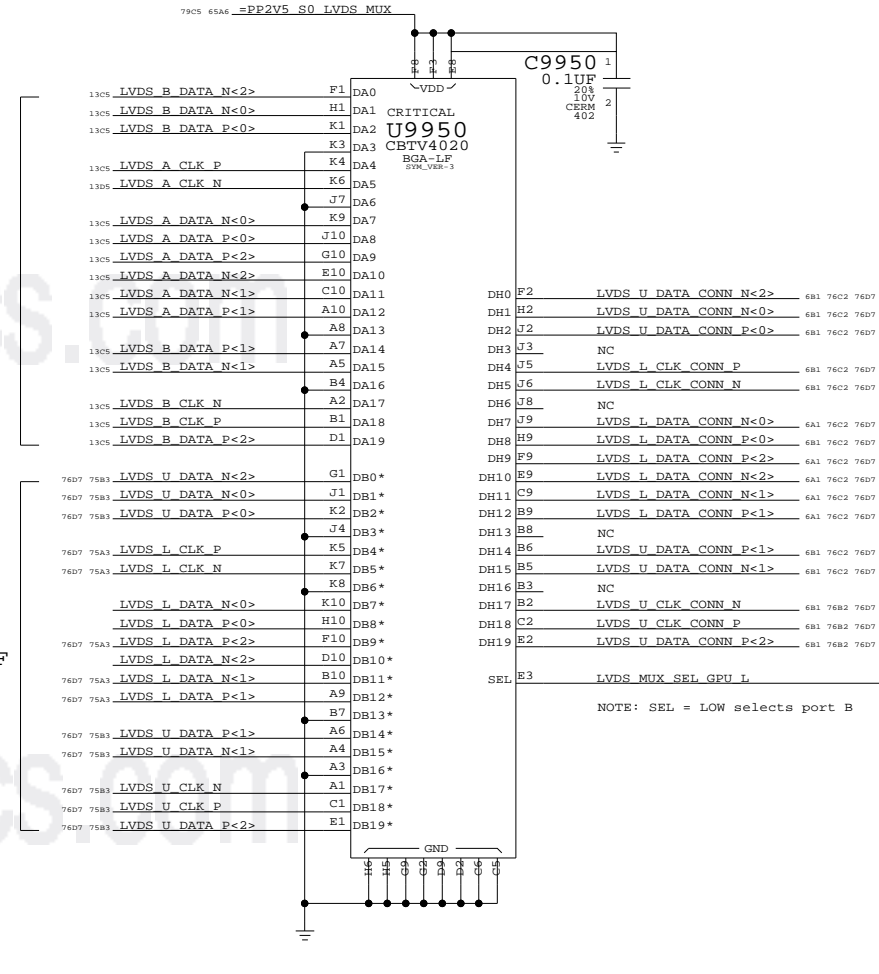


Divider set to rise to 1.88V nom/1.74V min when panel power is at 3.3V/3.315V. Schmitt trigger voltage max is 1.70V (@2.625V Vcc). R9981 can also be used as pad for cap, creating an RC filter.

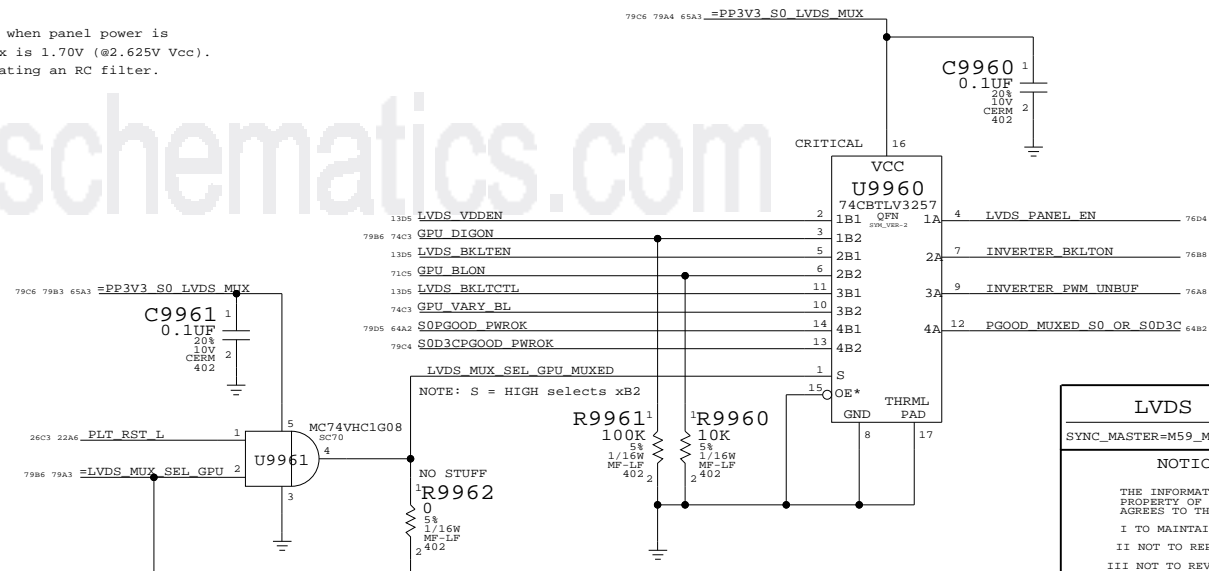
## GPU DDC Pass FETs



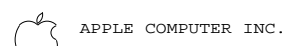
## LVDS I/F Mux



## Panel/Backlight Control Mux



LVDS Interface Pull-downs	
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NONE	99	105


8		7		6		5		4		3		2		1	
D	<div><div><div>Date - Radar # - Description</div><div>DMS Release #01000</div><div>2006/05/26 - 4508681 - Release for Proto</div><div>DMS Release #04000</div><div>2006/06/30 - 4566939 - Release for EVT</div><div>DMS Release #07000</div><div>2006/08/07 - 4607952 - Release for DVT</div><div>DMS Release #0A000</div><div>2006/09/19 - 4726575 - Release for PVT</div><div>DMS Release #0C000</div><div>2006/09/27 - 4726575 - Release for PVT</div></div></div>														D
C															C
B															B
A															A
8		7		6		5		4		3		2		1	

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B		
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SCALE	SHT	OF
NONE	100	105

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	8	7	6	5	4	3	2	1
D	FSB (Front-Side Bus) Constraints							
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	FSB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
	FSB_ADDR	*	=3:1_SPACING		FSB_DATA	*	=3:1_SPACING	
	FSB_ADDR2ADDR	*	=2:1_SPACING		FSB_DATA2DATA	*	=2:1_SPACING	
	FSB_ADSTB	*	=3:1_SPACING		FSB_DSTB	*	=3:1_SPACING	
	FSB_ADDR2ADSTB	*	=3:1_SPACING		FSB_DATA2DSTB	*	=3:1_SPACING	
	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
	FSB_COMMON	*	=2:1_SPACING					
All FSB signals with impedance requirements are 55-ohm single-ended. Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs. Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs. DSTB complementary pairs are spaced 3:1, even in constraint areas. Design Guide recommends each strobe/signal group is routed on the same layer. Design Guide recommends FSB signals be routed only on internal layers. NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1. NOTE: Design Guide allows closer spacing if signal lengths can be shortened. SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.2 & 4.3								
C	CPU Signal Constraints							
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=STANDARD	=STANDARD
	CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
	CPU_2T01	*	=2:1_SPACING		CPU_COMP	*	25 MIL	
	CPU_GTLREF	*	25 MIL		CPU_ITP	*	=2:1_SPACING	
	CPU_VCCSENSE	*	25 MIL					
	DG recommends at least 25 mils, >50 mils preferred							
	Most CPU signals with impedance requirements are 55-ohm single-ended. Some signals require 27.4-ohm single-ended impedance. SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.4, 4.6.2, & 5.8.2.4							
B	DDR2 Memory Bus Constraints							
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	MEM_45S	*	Y	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
	MEM_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
	MEM_70D	*	Y	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
	MEM_85D	*	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
	MEM_CLK2MEM	*	=4:1_SPACING		MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
	MEM_CTRL2CTRL	*	=2:1_SPACING		MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
	MEM_CTRL2MEM	*	=3:1_SPACING		MEM_CMD	MEM_CMD	*	MEM_CLK2MEM
A	MEM_CMD2CMD	*	=1.5:1_SPACING		MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
	MEM_CMD2MEM	*	=3:1_SPACING		MEM_CLK	MEM_DQS	*	MEM_CLK2MEM
	MEM_DATA2DATA	*	=1.5:1_SPACING		NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
	MEM_DATA2MEM	*	=3:1_SPACING		MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
	MEM_DQS2MEM	*	=3:1_SPACING		MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
	MEM_20OTHER	*	25 MIL		MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
	MEM_20OTHER	*	25 MIL		MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
	MEM_20OTHER	*	25 MIL		MEM_CMD	MEM_DQS	*	MEM_CMD2MEM
	MEM_20OTHER	*	25 MIL		MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
	MEM_20OTHER	*	25 MIL		MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
Need to support MEM_*-style wildcards!								
SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 6.2								

PCI-Express / DMI Bus Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL		DMI	*	20 MIL	
SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 7.2, 9.2 & 10.5.2							
Disk Interface Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING		SATA	*	20 MIL	
SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 10.6 & 10.7.2							
Audio Interface Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIO_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	=1.8:1_SPACING					
SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1							
USB 2.0 Interface Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB2_90D	*	Y	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2	*	=4:1_SPACING		USB2_2CLK	*	25 MIL	
DG says minimum spacing 50 mils to clocks							
SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.10.1.2							
Internal Interface Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING		SPI	*	=1.8:1_SPACING	
SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.17.1.1							
Clock Signal Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL		CLK_PCIE	*	20 MIL	
CLK_MED	*	20 MIL		CLK_SLOW	*	10 MIL	
SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 6.2							

Napa Platform Constraints							
SYNC_MASTER=(MASTER)				SYNC_DATE=(MASTER)			
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				SCALE NONE	SHT 101 OF 105		





	8	7	6	5	4	3	2	1
D	M59 Board-Specific Spacing & Physical Constraints							
	BOARD LAYERS				BOARD AREAS		BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
	TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA		MM	15.2
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM
	STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	55_OHM_SE	TOP, BOTTOM	Y	0.100 MM	0.100 MM			
	55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
C	50_OHM_SE	TOP, BOTTOM	Y	0.124 MM	0.124 MM			
	50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	45_OHM_SE	TOP, BOTTOM	Y	0.150 MM	0.150 MM			
	45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	40_OHM_SE	TOP, BOTTOM	Y	0.185 MM	0.185 MM			
	40_OHM_SE	*	Y	0.131 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	35_OHM_SE	TOP, BOTTOM	Y	0.230 MM	0.230 MM			
	35_OHM_SE	*	Y	0.165 MM	0.165 MM	=STANDARD	=STANDARD	=STANDARD
B	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	27P4_OHM_SE	TOP, BOTTOM	Y	0.335 MM	0.335 MM			
	27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	35_55_OHM_SE	TOP, BOTTOM	Y	0.230 MM	0.100 MM			
	35_55_OHM_SE	*	Y	0.165 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
	Unsupported rule							
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	75_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
A	70_OHM_DIFF	*	Y	0.149 MM	0.149 MM	=STANDARD	0.125 MM	0.125 MM
	70_OHM_DIFF	TOP, BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	75_OHM_DIFF	*	Y	0.131 MM	0.131 MM	=STANDARD	0.125 MM	0.125 MM
	75_OHM_DIFF	TOP, BOTTOM	Y	0.161 MM	0.161 MM		0.125 MM	0.125 MM
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	80_OHM_DIFF	*	Y	0.115 MM	0.111 MM	=STANDARD	0.125 MM	0.125 MM
	80_OHM_DIFF	TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	85_OHM_DIFF	*	Y	0.101 MM	0.101 MM	=STANDARD	0.125 MM	0.125 MM
	85_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	90_OHM_DIFF	*	Y	0.102 MM	0.102 MM	=STANDARD	0.220 MM	0.220 MM
	90_OHM_DIFF	TOP, BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	100_OHM_DIFF	*	Y	0.080 MM	0.080 MM	=STANDARD	0.200 MM	0.200 MM
	100_OHM_DIFF	TOP, BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	110_OHM_DIFF	*	Y	0.077 MM	0.077 MM	=STANDARD	0.330 MM	0.330 MM
	110_OHM_DIFF	TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM
	8	7	6	5	4	3	2	1

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	
STANDARD	*	=DEFAULT	
BGA_P1MM	*	=DEFAULT	
BGA_P2MM	*	=DEFAULT	
BGA_P3MM	*	=DEFAULT	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FB_CLK	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

Allow 0.1 MM on blind-to-buried via dogbones (layers 2 & 11)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	
1.8:1_SPACING	*	0.18 MM	
2:1_SPACING	*	0.2 MM	
2.5:1_SPACING	*	0.25 MM	
3:1_SPACING	*	0.3 MM	
4:1_SPACING	*	0.4 MM	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	ISL2, ISL11	0.1 MM	
1.8:1_SPACING	ISL2, ISL11	0.1 MM	
2:1_SPACING	ISL2, ISL11	0.1 MM	
2.5:1_SPACING	ISL2, ISL11	0.1 MM	
3:1_SPACING	ISL2, ISL11	0.1 MM	
4:1_SPACING	ISL2, ISL11	0.1 MM	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	ISL2, ISL11	0.1 MM	
CLK_PCIE	ISL2, ISL11	0.1 MM	
CLK_MED	ISL2, ISL11	0.1 MM	
CLK_SLOW	ISL2, ISL11	0.1 MM	
CPU_COMP	ISL2, ISL11	0.1 MM	
CPU_OTLREF	ISL2, ISL11	0.1 MM	
CPU_VCCSENSE	ISL2, ISL11	0.1 MM	
DMI	ISL2, ISL11	0.1 MM	
LVDS_PAIR2PAIR	ISL2, ISL11	0.1 MM	
MEM_2OTHER	ISL2, ISL11	0.1 MM	
PCIE	ISL2, ISL11	0.1 MM	
SATA	ISL2, ISL11	0.1 MM	
TMDS_PAIR2PAIR	ISL2, ISL11	0.1 MM	
VGA	ISL2, ISL11	0.1 MM	

Rules for "Topology #3" for FSB signals, Napa DG tables 4-7 & 4-12.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR_OVERRIDE	*	=2:1_SPACING_OVERRIDE	VERRIDE
FSB_ADDR2ADDR_OVERRIDE	*	=STANDARD_OVERRIDE	VERRIDE
FSB_ADSTB_OVERRIDE	*	=2:1_SPACING_OVERRIDE	VERRIDE
FSB_ADDR2ADSTB_OVERRIDE	*	=2:1_SPACING_OVERRIDE	VERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA_OVERRIDE	*	=2:1_SPACING_OVERRIDE	VERRIDE
FSB_DATA2DATA_OVERRIDE	*	=STANDARD_OVERRIDE	VERRIDE
FSB_DSTB_OVERRIDE	*	=2:1_SPACING_OVERRIDE	VERRIDE
FSB_DATA2DSTB_OVERRIDE	*	=2:1_SPACING_OVERRIDE	VERRIDE

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS	*	LVDS_100D
TMDS	*	TMDS_100D
TMDSCONN	*	TMDS_100D
VGA	*	VGA_75S

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_2OTHER_OVERRIDE	*	0.5 MM_OVERRIDE	VERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI_2PCI_OVERRIDE	*	0.1 MM_OVERRIDE	VERRIDE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCI	PCI	*	PCI_2PCI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENETCONN	*	*	ENET
TMDSCONN	*	*	TMDS


"Stale" physical / spacing types

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ANALOG	*	*	FSB_COMMON
FSB_P2MM	*	*	FSB_COMMON
I2C	*	*	SMB
GND	*	*	STANDARD
MEM_PP1V8_S3	*	*	STANDARD
FB_PP1V8	*	*	STANDARD

FSB_ANALOG	
FSB_P2MM	
I2C	
GND	
MEM_PP1V8_S3	
FB_PP1V8	
PCI	PCI 55S

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S_OVERRIDE	*	VERRIDE	VERRIDE	VERRIDE	0.100 MM_OVERRIDE	VERRIDE	VERRIDE
MEM_70D_OVERRIDE	*	VERRIDE	VERRIDE	VERRIDE	0.100 MM_OVERRIDE	VERRIDE	VERRIDE
MEM_85D_OVERRIDE	*	VERRIDE	VERRIDE	VERRIDE	0.100 MM_OVERRIDE	VERRIDE	VERRIDE

M59 Spacing & Physical Constraints	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)
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	SCALE NONE	SHT 103	OF 105





	8	7	6	5	4	3	2	1	
	Low Acoustic Noise 22uF Ceramic Capacitor options								
	Samsung								
	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION			
	138S0602	20	CAP,CER,22UF,20%,6.3V,XSR,0805		CRITICAL	CAP22UF_SAM_CRIT	CPU_VCORE		
	138S0602	2	CAP,CER,22UF,20%,6.3V,XSR,0805	C1934,C1936	CRITICAL	CAP22UF_SAM	PP1V5_30_NB_VCCA_PLL		
	138S0602	1	CAP,CER,22UF,20%,6.3V,XSR,0805	C5802	CRITICAL	CAP22UF_SAM	3V42_G3H		
	138S0602	8	CAP,CER,22UF,20%,6.3V,XSR,0805	CT616,CT617,CT660,CT661,CT671,CT672,CT680,CT681	CRITICAL	CAP22UF_SAM	5V_S0,5V_S5,1V5_NB,1V5_S0		
	138S0602	6	CAP,CER,22UF,20%,6.3V,XSR,0805	CT676,CT678,CT679,CT681,CT682	CRITICAL	CAP22UF_SAM	3V3_S5 (2V5_INPUT),2V5_S3,3V3_S3 (1V2_INPUT)		
	138S0602	4	CAP,CER,22UF,20%,6.3V,XSR,0805	CT682,CT683,CT684	CRITICAL	CAP22UF_SAM_CRIT	1V2_S3		
	138S0602	1	CAP,CER,22UF,20%,6.3V,XSR,0805	C7841	CRITICAL	CAP22UF_SAM	1V8_S3		
	138S0602	2	CAP,CER,22UF,20%,6.3V,XSR,0805	C7846,C7847	CRITICAL	CAP22UF_SAM	1V8_D3C		
	138S0602	2	CAP,CER,22UF,20%,6.3V,XSR,0805	C7940,C7941	CRITICAL	CAP22UF_SAM	3V3_S5		
	138S0602	2	CAP,CER,22UF,20%,6.3V,XSR,0805	C7985,C7986	CRITICAL	CAP22UF_SAM	1V05_S0		
	138S0602	1	CAP,CER,22UF,20%,6.3V,XSR,0805	C8015	CRITICAL	CAP22UF_SAM	3V42_G3H		
	138S0602	3	CAP,CER,22UF,20%,6.3V,XSR,0805	C8400,C8405,C8410	CRITICAL	CAP22UF_SAM_CRIT	GPU_PCIE		
	138S0602	5	CAP,CER,22UF,20%,6.3V,XSR,0805	C8540,C8541,C8546,C8557,C8589	CRITICAL	CAP22UF_SAM_CRIT	GPU_VCORE,GPU_BB		
	138S0602	9	CAP,CER,22UF,20%,6.3V,XSR,0805	DB00,DB01,DB02,DB03,DB04,DB05,DB06,DB07	CRITICAL	CAP22UF_SAM_CRIT	GPU_CORE		
	138S0602	4	CAP,CER,22UF,20%,6.3V,XSR,0805	C8900,C8920,C8950,C8970	CRITICAL	CAP22UF_SAM_CRIT	VRAM_A		
	138S0602	4	CAP,CER,22UF,20%,6.3V,XSR,0805	C9000,C9020,C9050,C9070	CRITICAL	CAP22UF_SAM_CRIT	VRAM_B		
	138S0602	8	CAP,CER,22UF,20%,6.3V,XSR,0805	CH010,CH011,CH013,CH020,CH021,CH030,CH031,CH040	CRITICAL	CAP22UF_SAM	GPU_MISC		
	138S0602	9	CAP,CER,22UF,20%,6.3V,XSR,0805	DB00,DB01,DB02,DB03,DB04,DB05,DB06,DB07,DB08	CRITICAL	CAP22UF_SAM	GPU_VIDEO		
	Murata								
	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION			
	138S0603	20	CAP,CER,22UF,20%,6.3V,XSR,0805		CRITICAL	CAP22UF_MURA_CRIT	CPU_VCORE		
	138S0603	2	CAP,CER,22UF,20%,6.3V,XSR,0805	C1934,C1936	CRITICAL	CAP22UF_MURA	PP1V5_30_NB_VCCA_PLL		
	138S0603	1	CAP,CER,22UF,20%,6.3V,XSR,0805	C5802	CRITICAL	CAP22UF_MURA	3V42_G3H		
	138S0603	8	CAP,CER,22UF,20%,6.3V,XSR,0805	CT616,CT617,CT660,CT661,CT671,CT672,CT680,CT681	CRITICAL	CAP22UF_MURA	5V_S0,5V_S5,1V5_NB,1V5_S0		
	138S0603	6	CAP,CER,22UF,20%,6.3V,XSR,0805	CT676,CT678,CT679,CT681,CT682	CRITICAL	CAP22UF_MURA	3V3_S5 (2V5_INPUT),2V5_S3,3V3_S3 (1V2_INPUT)		
	138S0603	4	CAP,CER,22UF,20%,6.3V,XSR,0805	CT682,CT683,CT684	CRITICAL	CAP22UF_MURA_CRIT	1V2_S3		
	138S0603	1	CAP,CER,22UF,20%,6.3V,XSR,0805	C7841	CRITICAL	CAP22UF_MURA	1V8_S3		
	138S0603	2	CAP,CER,22UF,20%,6.3V,XSR,0805	C7846,C7847	CRITICAL	CAP22UF_MURA	1V8_D3C		
	138S0603	2	CAP,CER,22UF,20%,6.3V,XSR,0805	C7940,C7941	CRITICAL	CAP22UF_MURA	3V3_S5		
	138S0603	2	CAP,CER,22UF,20%,6.3V,XSR,0805	C7985,C7986	CRITICAL	CAP22UF_MURA	1V05_S0		
	138S0603	1	CAP,CER,22UF,20%,6.3V,XSR,0805	C8015	CRITICAL	CAP22UF_MURA	3V42_G3H		
	138S0603	3	CAP,CER,22UF,20%,6.3V,XSR,0805	C8400,C8405,C8410	CRITICAL	CAP22UF_MURA_CRIT	GPU_PCIE		
	138S0603	5	CAP,CER,22UF,20%,6.3V,XSR,0805	C8540,C8541,C8546,C8557,C8589	CRITICAL	CAP22UF_MURA_CRIT	GPU_VCORE,GPU_BB		
	138S0603	9	CAP,CER,22UF,20%,6.3V,XSR,0805	DB00,DB01,DB02,DB03,DB04,DB05,DB06,DB07	CRITICAL	CAP22UF_MURA_CRIT	GPU_CORE		
	138S0603	4	CAP,CER,22UF,20%,6.3V,XSR,0805	C8900,C8920,C8950,C8970	CRITICAL	CAP22UF_MURA_CRIT	VRAM_A		
	138S0603	4	CAP,CER,22UF,20%,6.3V,XSR,0805	C9000,C9020,C9050,C9070	CRITICAL	CAP22UF_MURA_CRIT	VRAM_B		
	138S0603	8	CAP,CER,22UF,20%,6.3V,XSR,0805	CH010,CH011,CH013,CH020,CH021,CH030,CH031,CH040	CRITICAL	CAP22UF_MURA	GPU_MISC		
	138S0603	9	CAP,CER,22UF,20%,6.3V,XSR,0805	DB00,DB01,DB02,DB03,DB04,DB05,DB06,DB07,DB08	CRITICAL	CAP22UF_MURA	GPU_VIDEO		
	Taiyo - non critical locations only								
	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION			
	138S0606	2	CAP,CER,22UF,20%,6.3V,XSR,0805	C1934,C1936	CRITICAL	CAP22UF_TAIYO	PP1V5_30_NB_VCCA_PLL		
	138S0606	1	CAP,CER,22UF,20%,6.3V,XSR,0805	C5802	CRITICAL	CAP22UF_TAIYO	3V42_G3H		
	138S0606	8	CAP,CER,22UF,20%,6.3V,XSR,0805	CT616,CT617,CT660,CT661,CT671,CT672,CT680,CT681	CRITICAL	CAP22UF_TAIYO	5V_S0,5V_S5,1V5_NB,1V5_S0		
	138S0606	6	CAP,CER,22UF,20%,6.3V,XSR,0805	CT676,CT678,CT679,CT681,CT682	CRITICAL	CAP22UF_TAIYO	3V3_S5 (2V5_INPUT),2V5_S3,3V3_S3 (1V2_INPUT)		
	138S0606	1	CAP,CER,22UF,20%,6.3V,XSR,0805	C7841	CRITICAL	CAP22UF_TAIYO	1V8_S3		
	138S0606	2	CAP,CER,22UF,20%,6.3V,XSR,0805	C7846,C7847	CRITICAL	CAP22UF_TAIYO	1V8_D3C		
	138S0606	2	CAP,CER,22UF,20%,6.3V,XSR,0805	C7940,C7941	CRITICAL	CAP22UF_TAIYO	3V3_S5		
	138S0606	2	CAP,CER,22UF,20%,6.3V,XSR,0805	C7985,C7986	CRITICAL	CAP22UF_TAIYO	1V05_S0		
	138S0606	1	CAP,CER,22UF,20%,6.3V,XSR,0805	C8015	CRITICAL	CAP22UF_TAIYO	3V42_G3H		
	138S0606	8	CAP,CER,22UF,20%,6.3V,XSR,0805	CH010,CH011,CH013,CH020,CH021,CH030,CH031,CH040	CRITICAL	CAP22UF_TAIYO	GPU_MISC		
	138S0606	9	CAP,CER,22UF,20%,6.3V,XSR,0805	DB00,DB01,DB02,DB03,DB04,DB05,DB06,DB07,DB08	CRITICAL	CAP22UF_TAIYO	GPU_VIDEO		
	The vendors for 22uF ceramic capacitors are controlled on this page. The main BOMs must choose a vendor for critical and non-critical locations.								
	BOM options for crit. loc.      BOM options for non-crit. loc.								
	CAP22UF_SAM_CRIT CAP22UF_MURA_CRIT				CAP22UF_SAM CAP22UF_MURA CAP22UF_TAIYO				
	Note: all caps have CRITICAL BOM options regardless of location.								
	22uF Capacitor BOM Configuration								
	SYNC_MASTER=N/A      SYNC_DATE=N/A								
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	SCALE NONE						SHT 105	OF 105	
	8	7	6	5	4	3	2	1	