

System Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

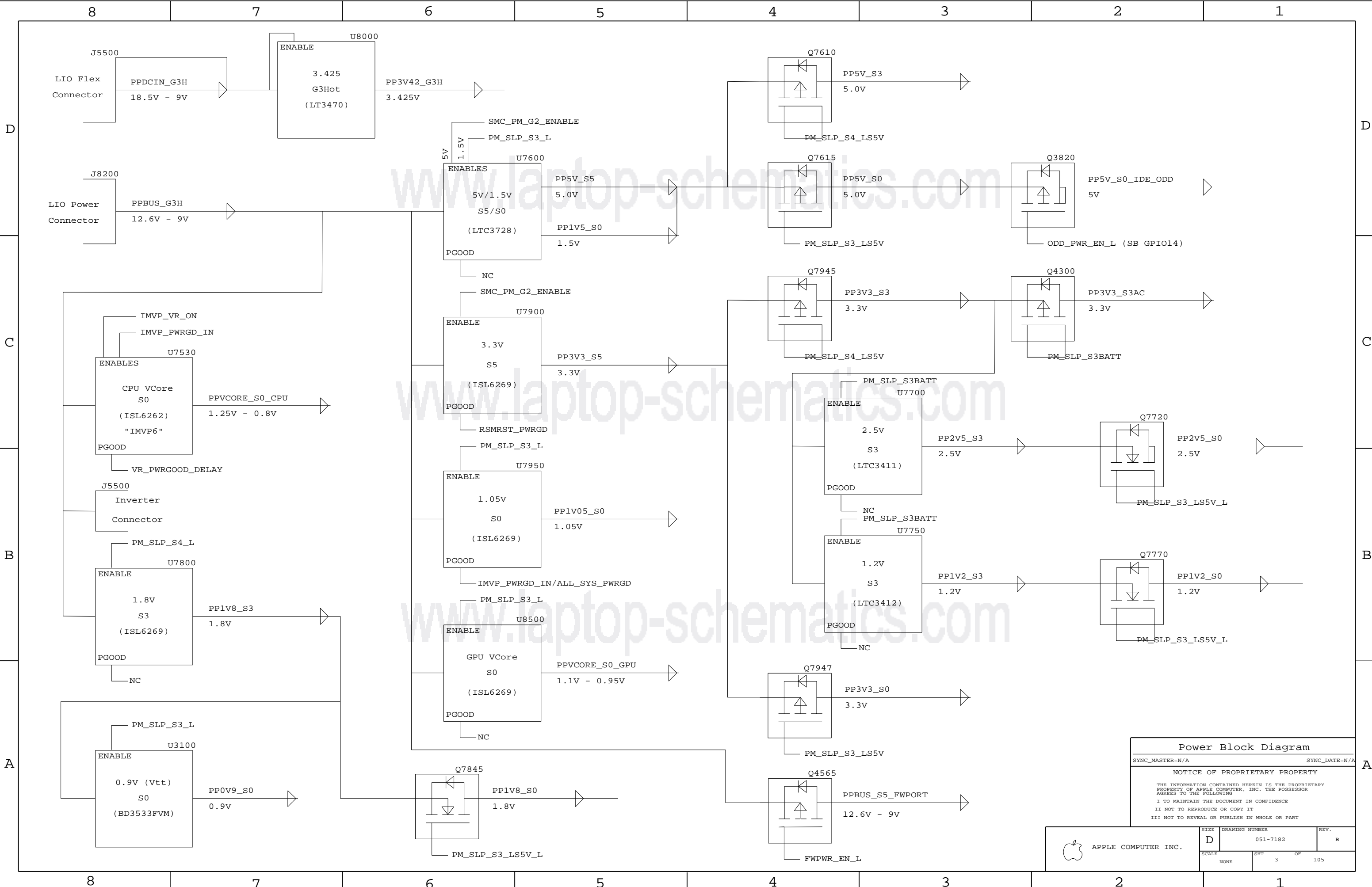
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Power Block Diagram

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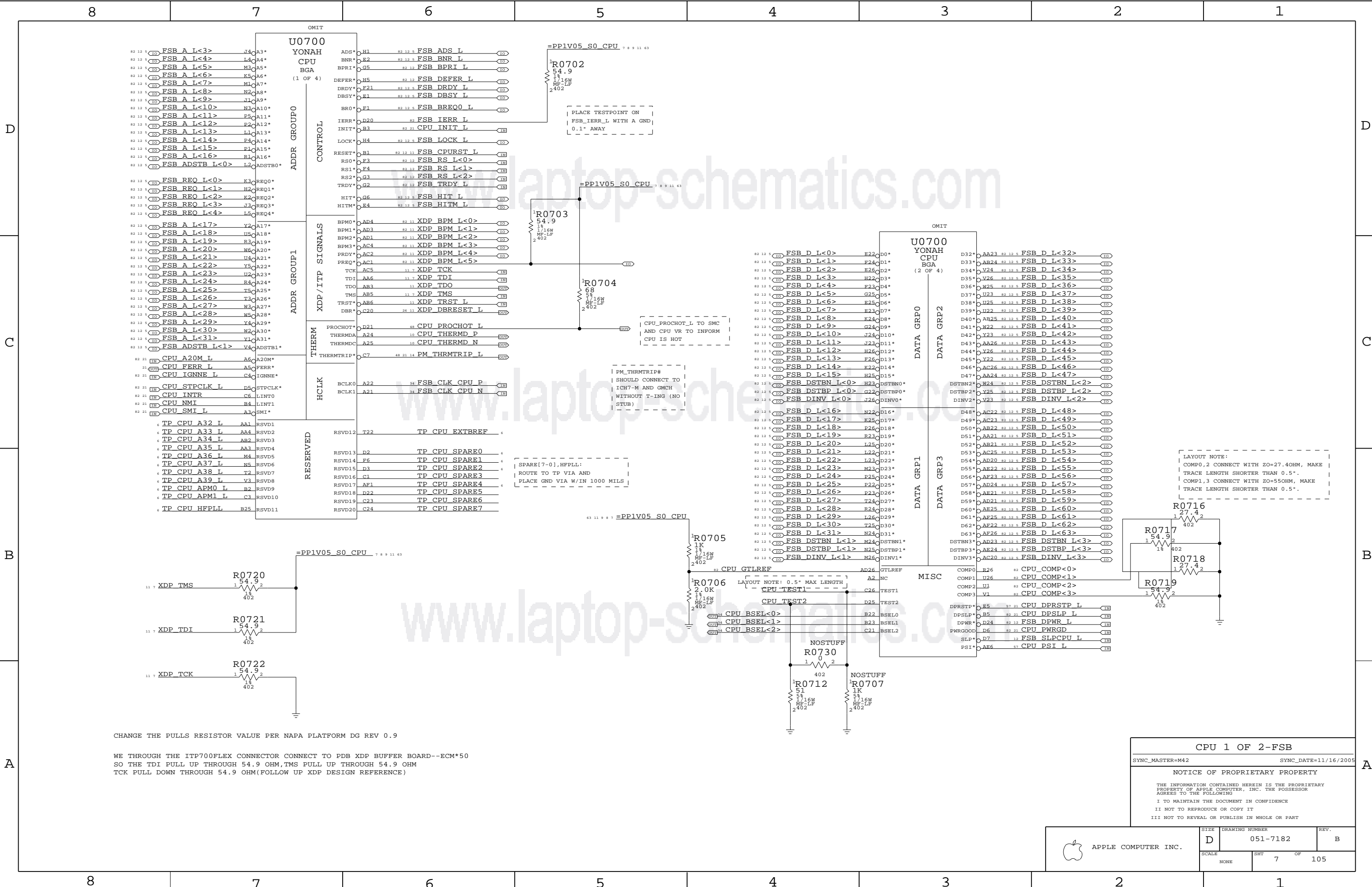
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	D	051-7182	B
SCALE	SHT	OF	REV.
NONE	3	105	

</



CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9

WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50
SO THE TDI PULL UP THROUGH 54.9 OHM,TMS PULL UP THROUGH 54.9 OHM
TCK PULL DOWN THROUGH 54.9 OHM(FOLLOW UP XDP DESIGN REFERENCE)

CPU 1 OF 2-FSB

SYNC_MASTER=M42

SYNC_DATE=11/16/2005

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SIZE D

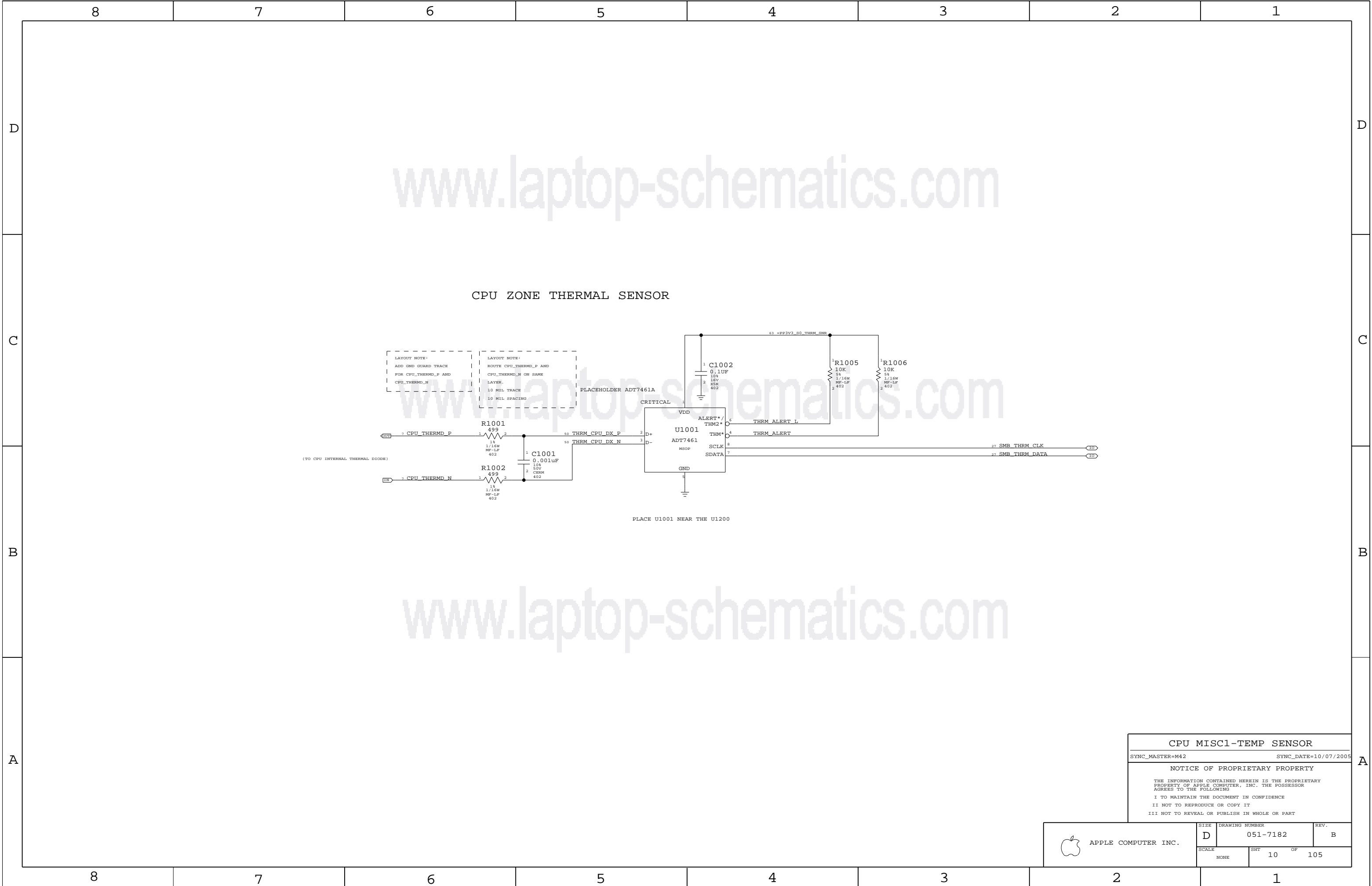
DRAWING NUMBER 051-7182

REV. B

SCALE NONE

SHT 7 OF 105





CPU MISC1-TEMP SENSOR	
SYNC_MASTER=M42	SYNC_DATE=10/07/2005
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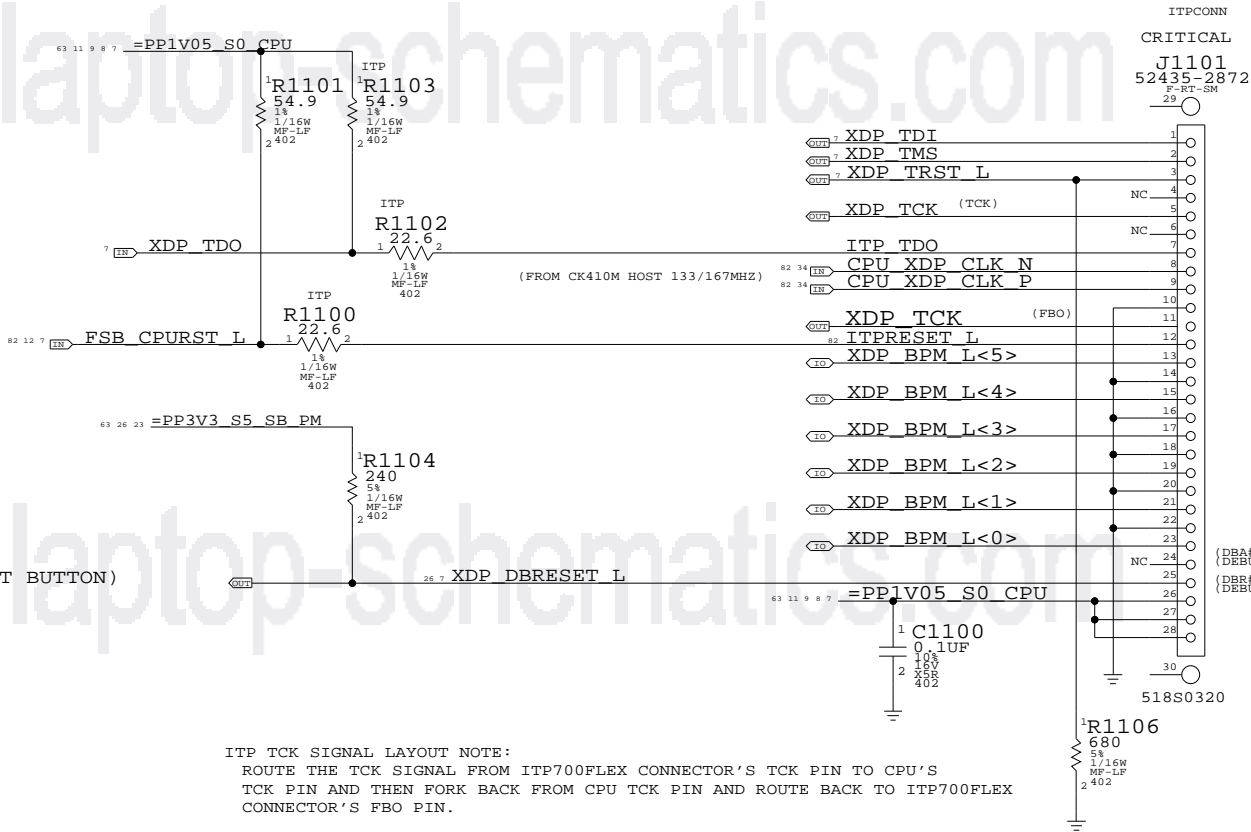
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7182	REV. B
	SCALE NONE	SHT 10	OF 105

www.laptop-schematics.com

CPU ITP700FLEX DEBUG SUPPORT

www.laptop-schematics.com

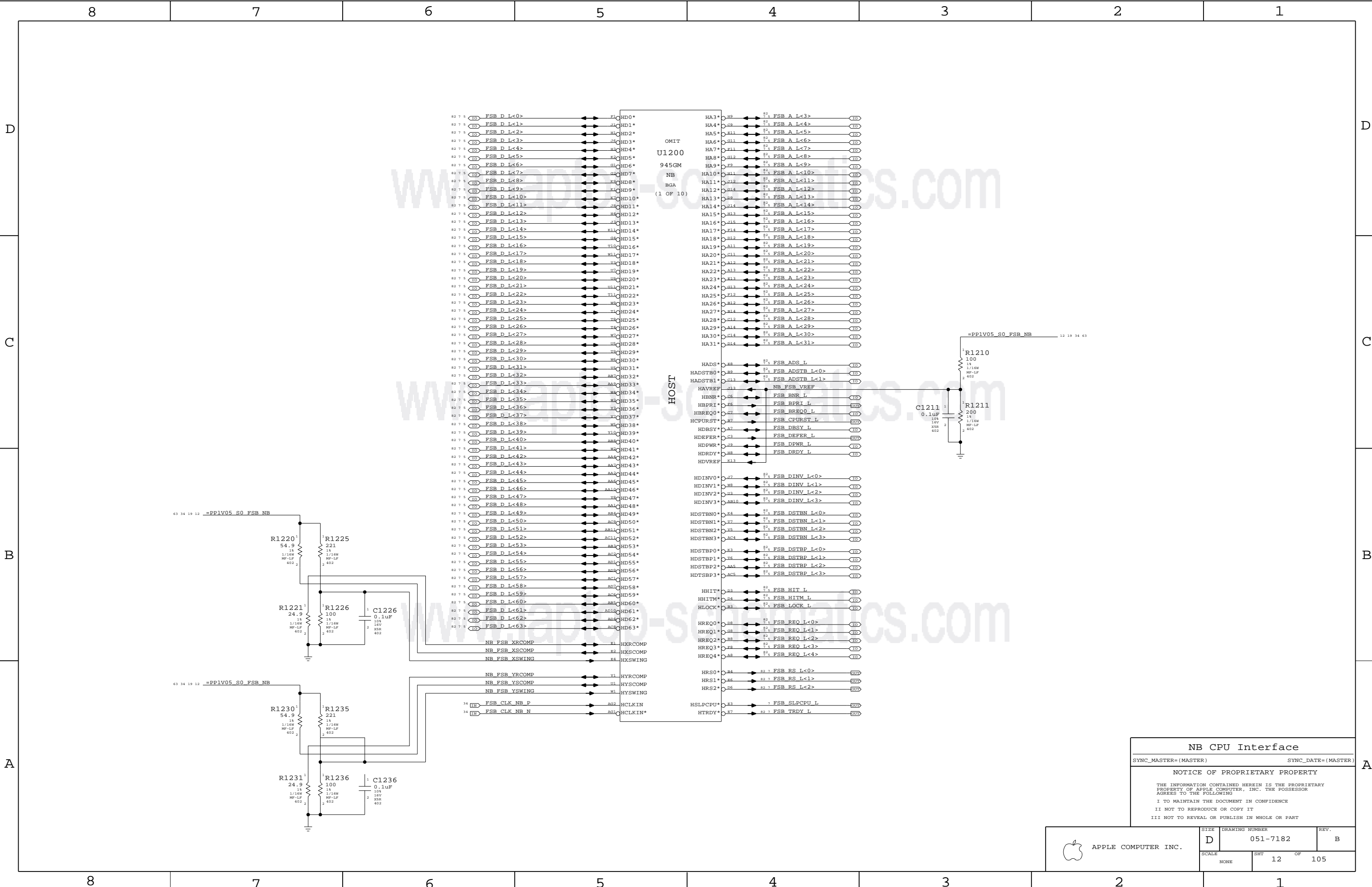
www.laptop-schematics.com



ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S
TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX
CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG	
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SCALE		SHT	OF
NONE		11	105



NB CPU Interface

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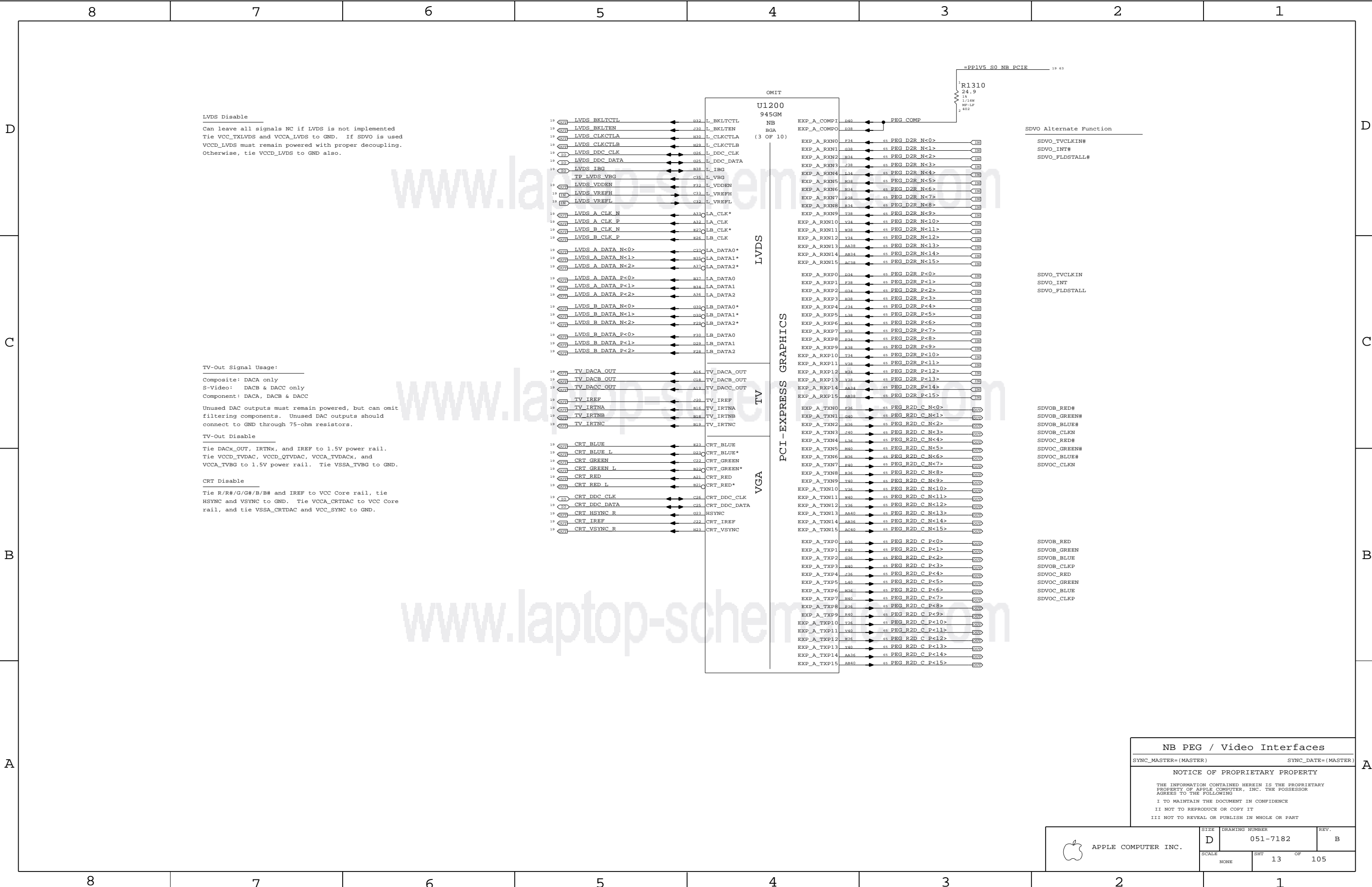
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SCALE		SHT	OF
NONE		12	105



LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACC & DACC only
Component: DACA, DACC & DACC

Unused DAC outputs must remain powered, but can omit
filtering components. Unused DAC outputs should
connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVVG to 1.5V power rail. Tie VSSA_TVVG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.

NB PEG / Video Interfaces

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SYNC_DATE=(MASTER)

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SIZE

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DRAWING NUMBER

051-7182

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SCALE

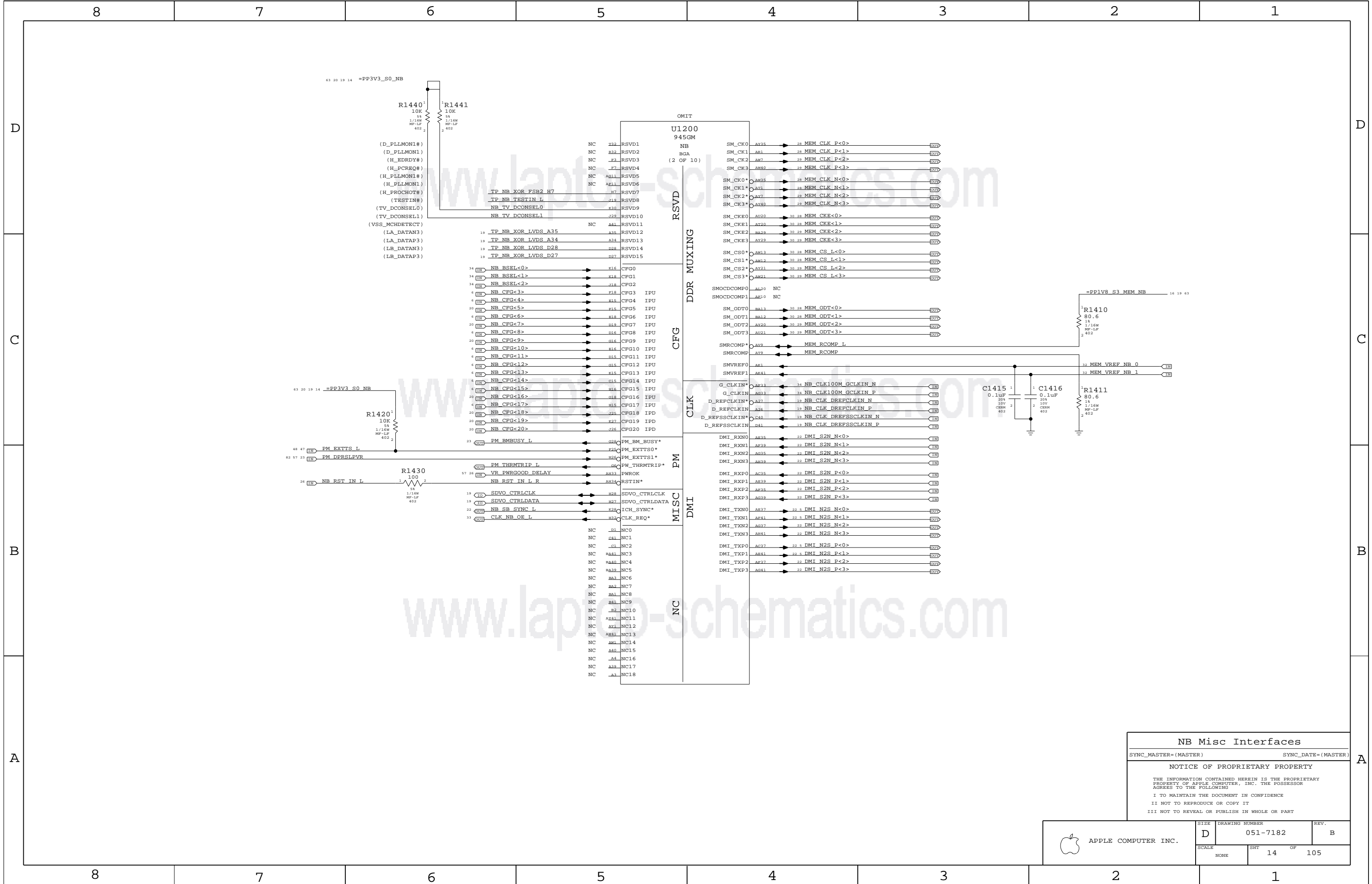
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OF

105



NB Misc Interfaces

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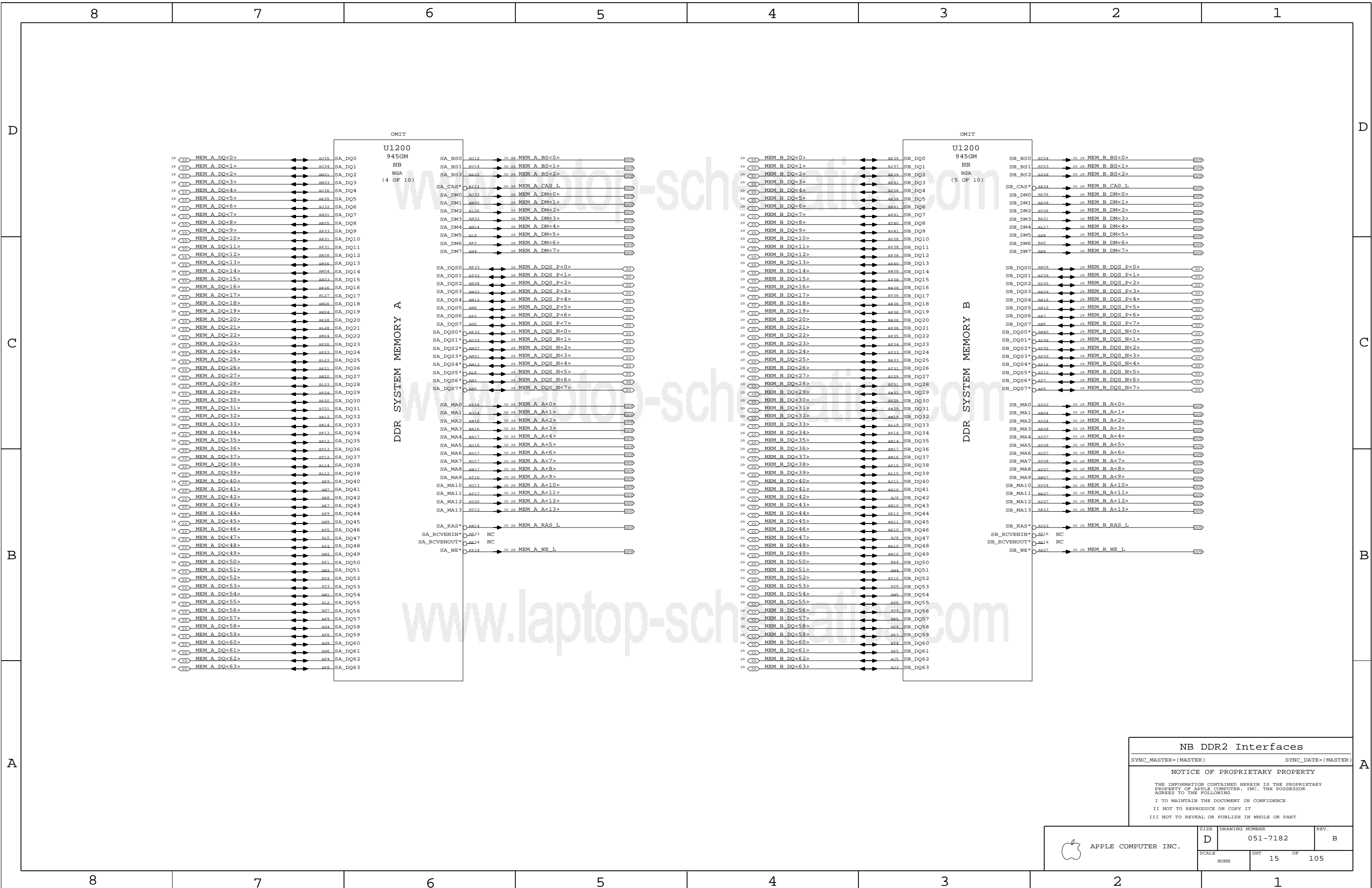
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APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-7182 REV. B

SCALE NONE SHT 14 OF 105



NB DDR2 Interfaces

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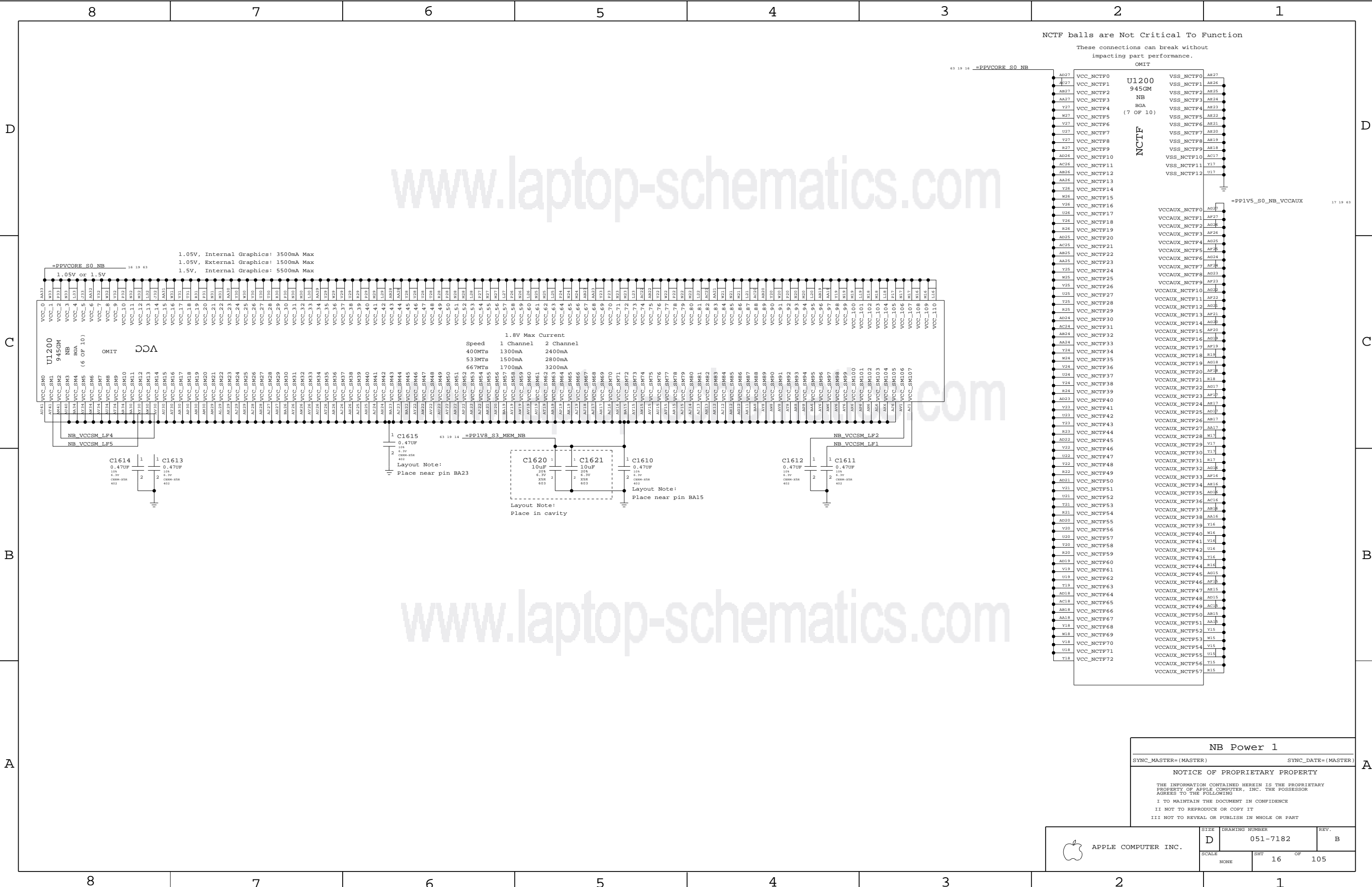
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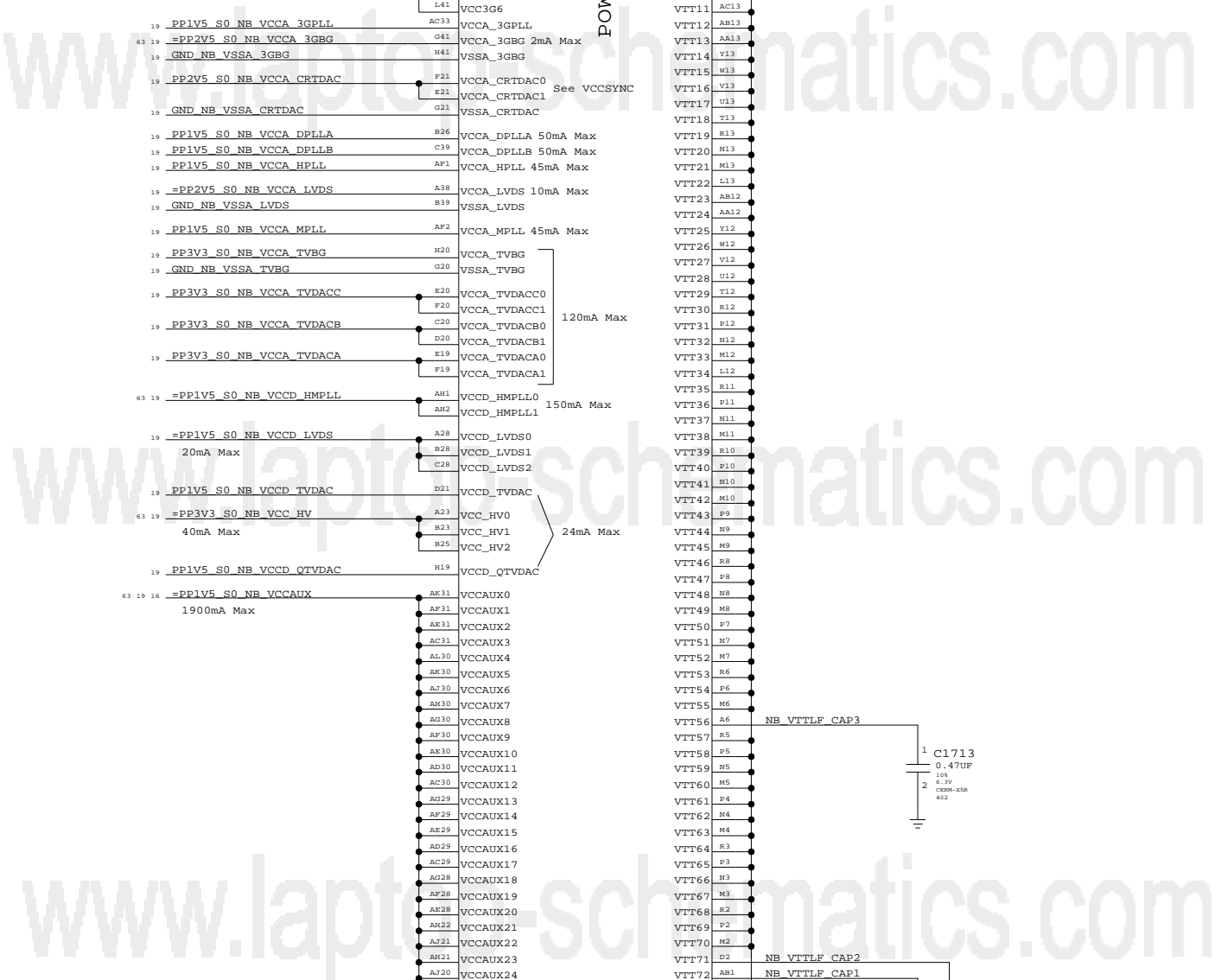
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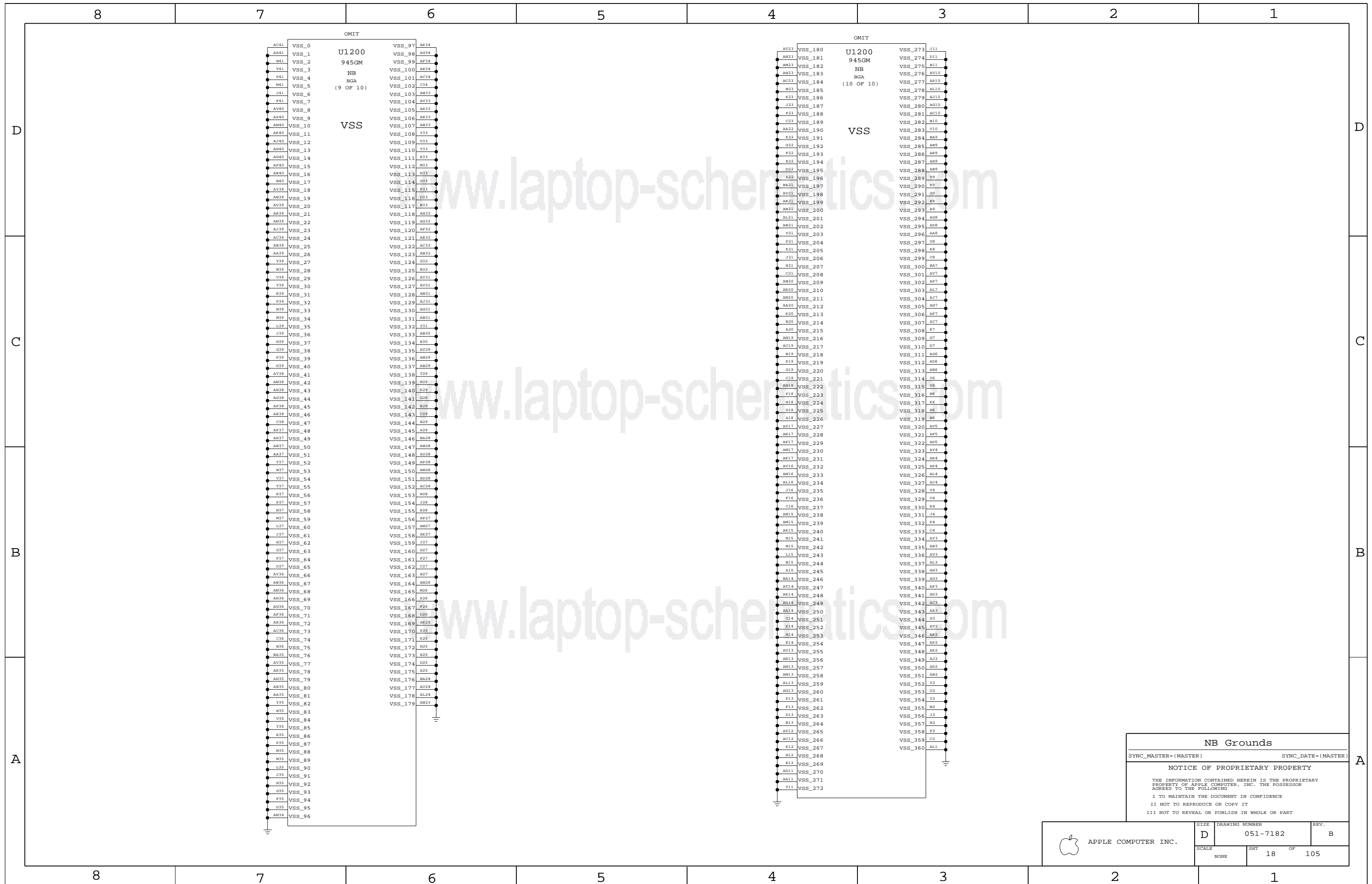
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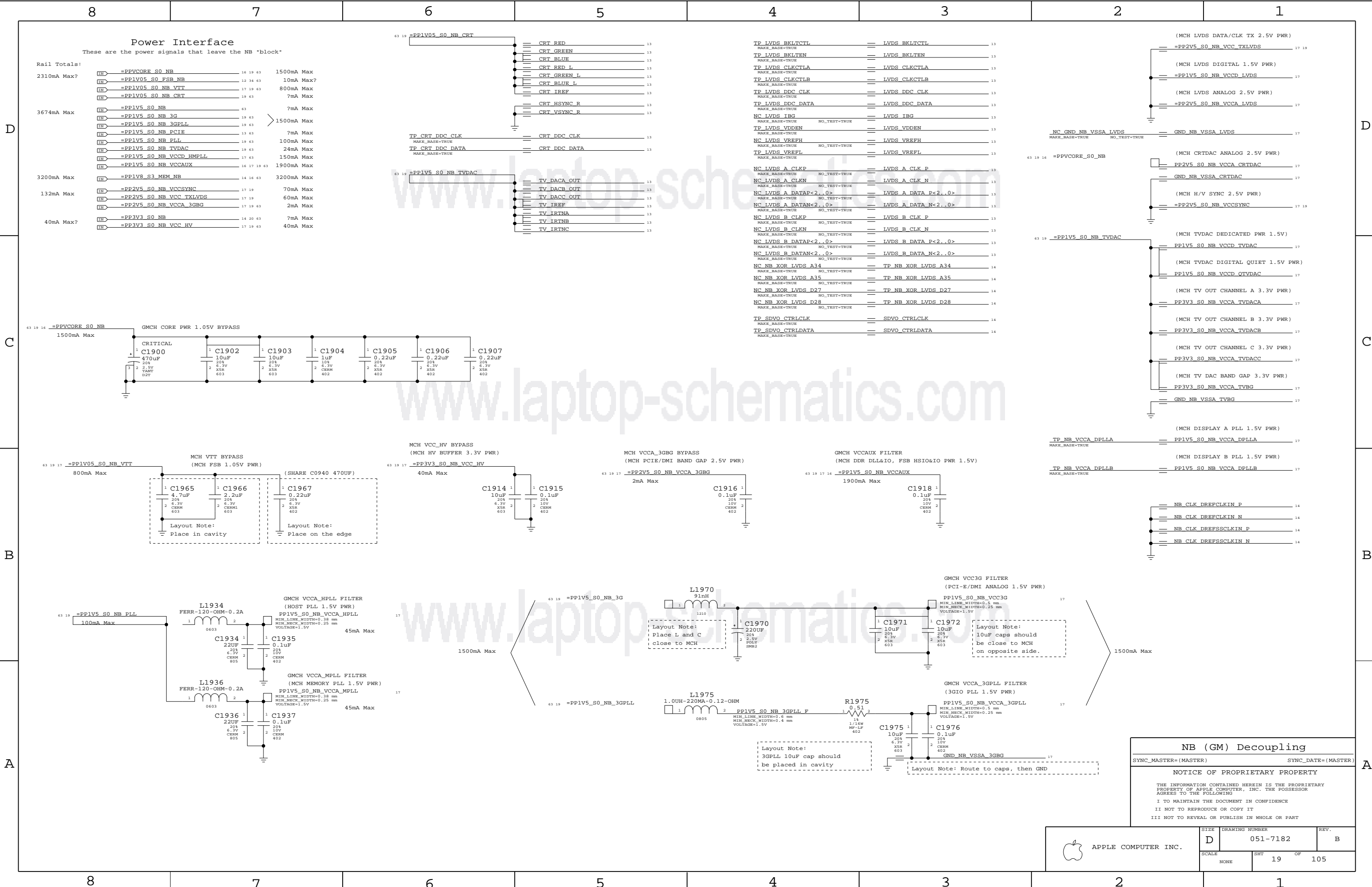
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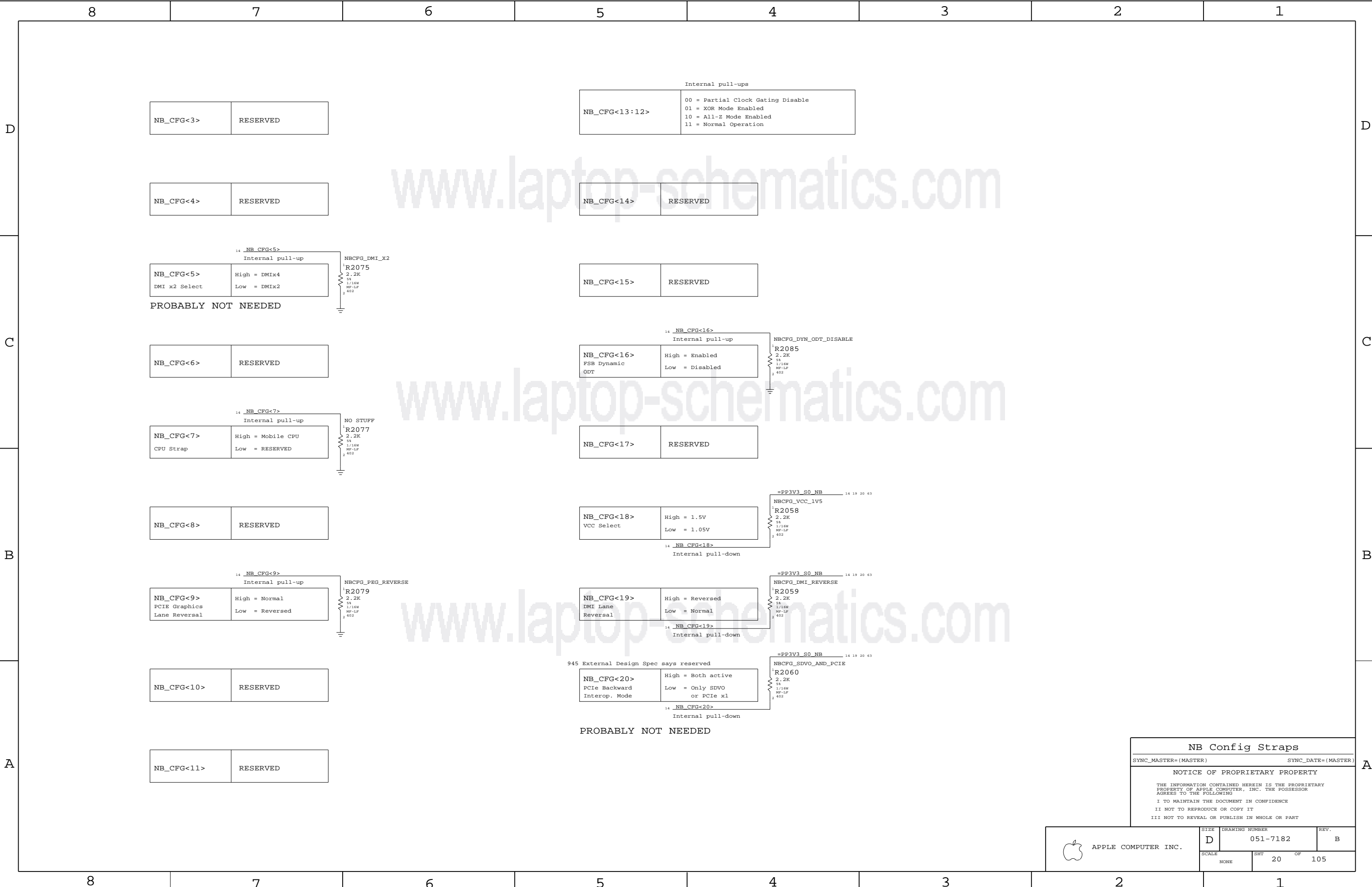
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NB Config Straps

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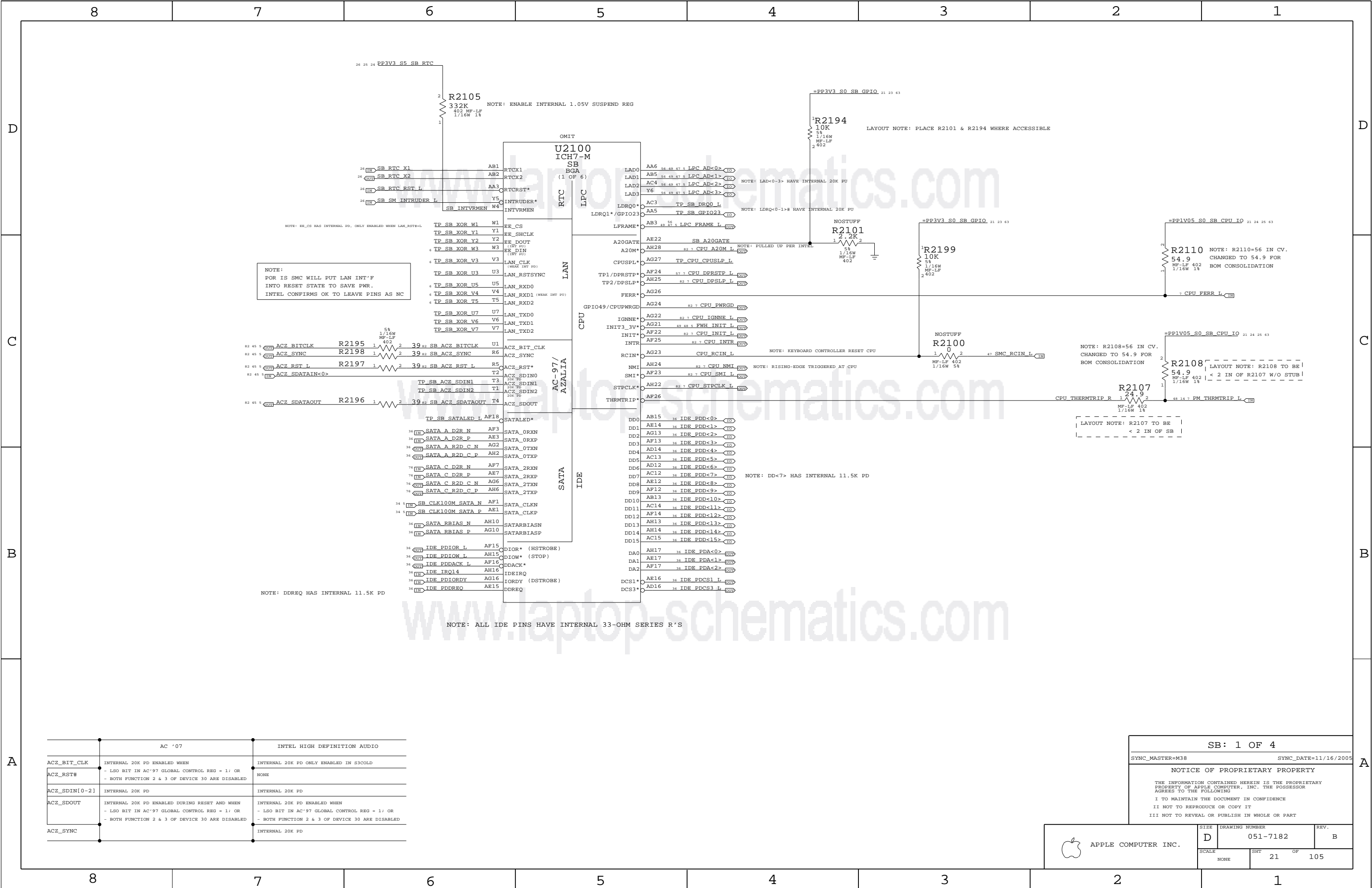
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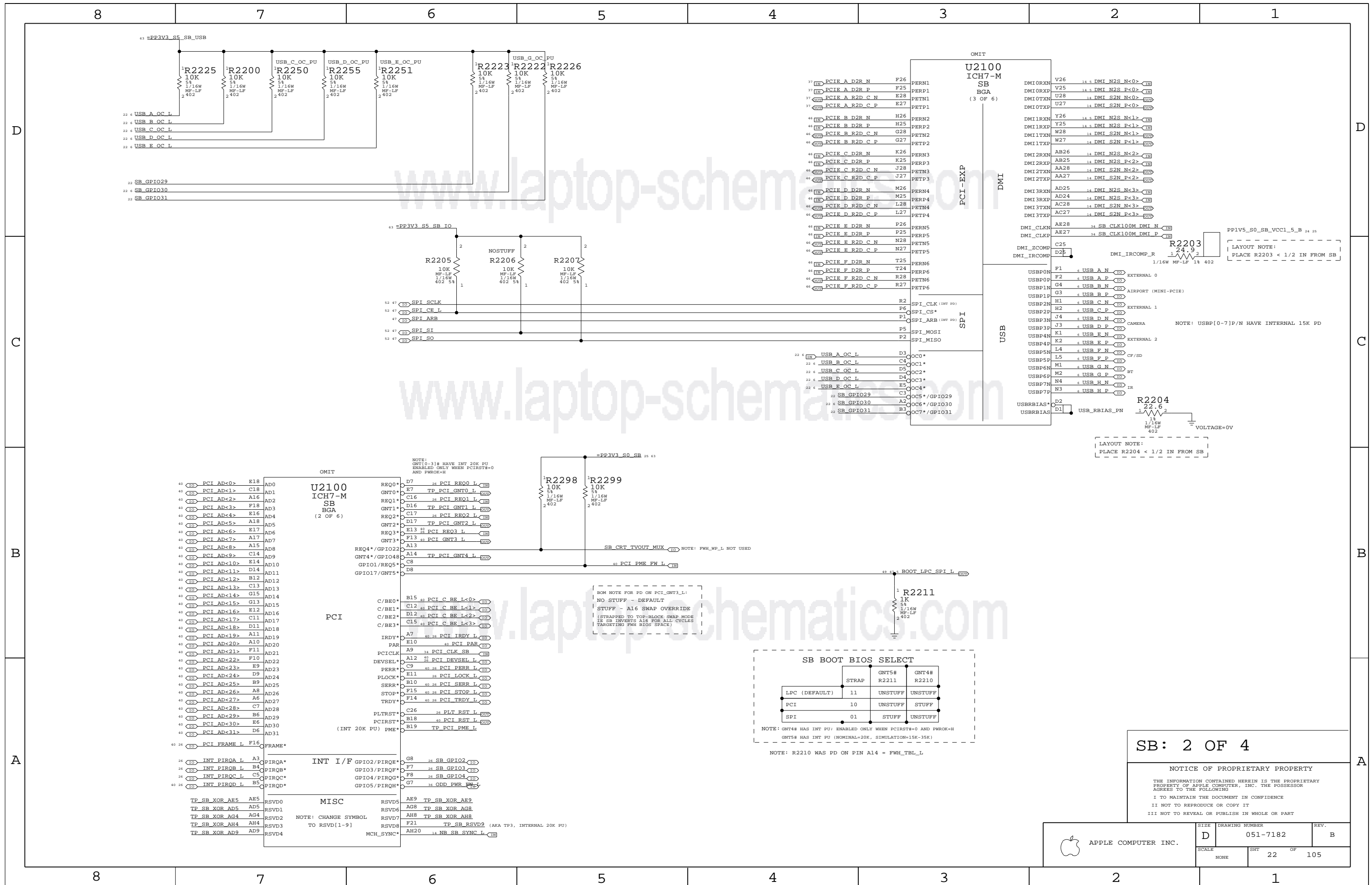
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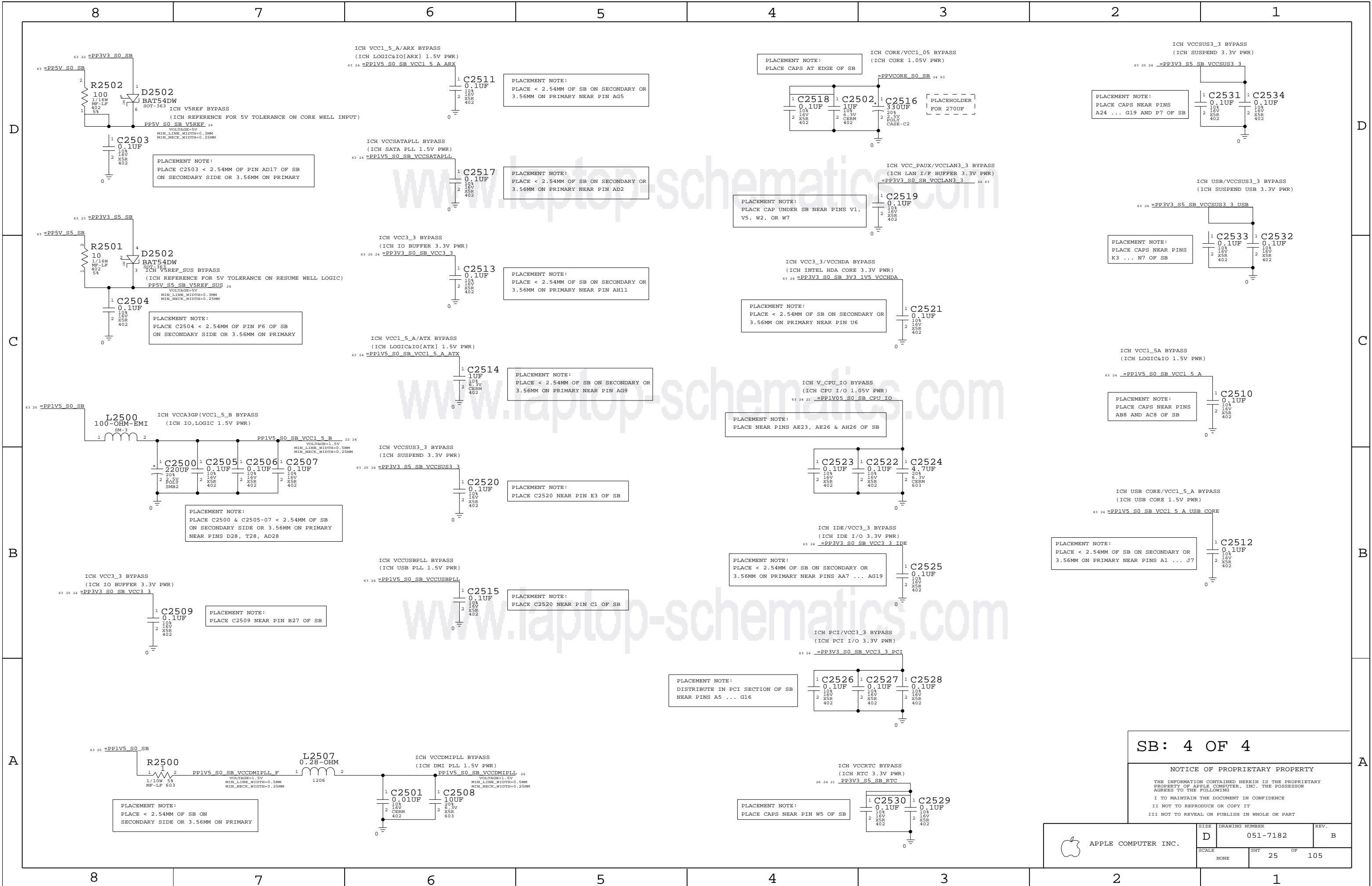
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SB: 4 OF 4

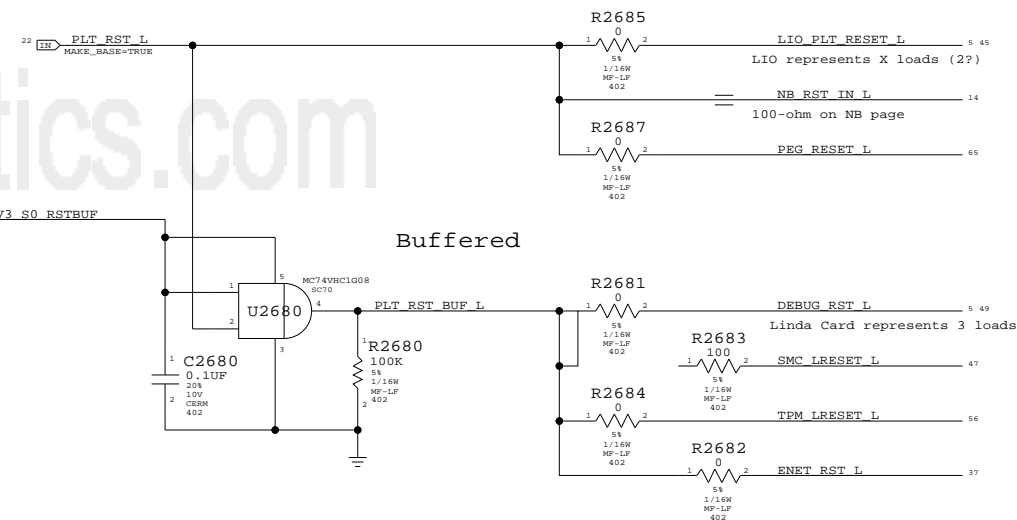
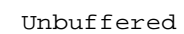
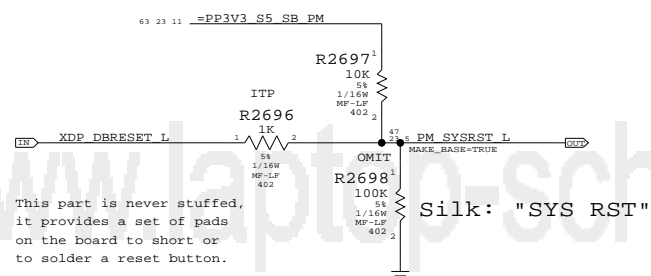
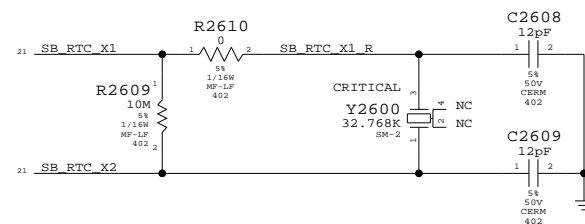
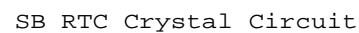
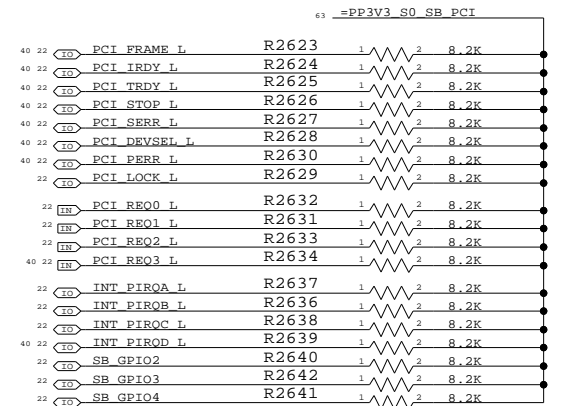
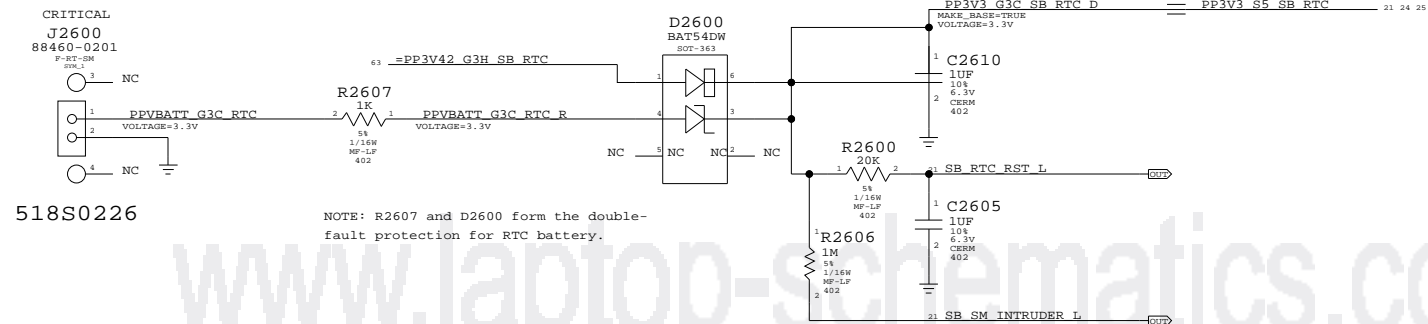
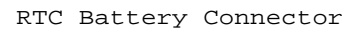
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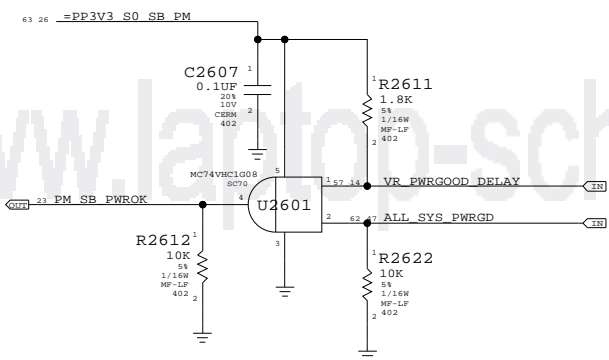
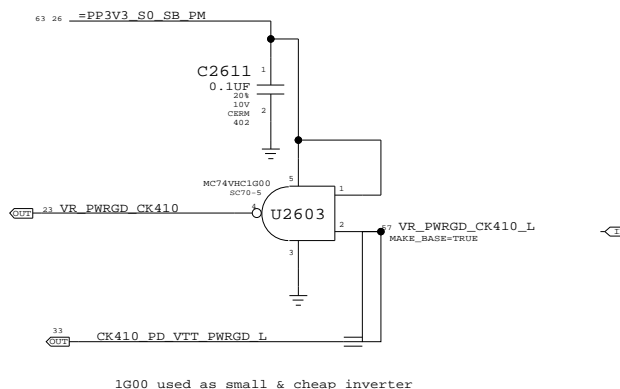


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SCALE	SHT	OF
NONE	25	105



Initial resistor values are based on CRB,
but may change after characterization.

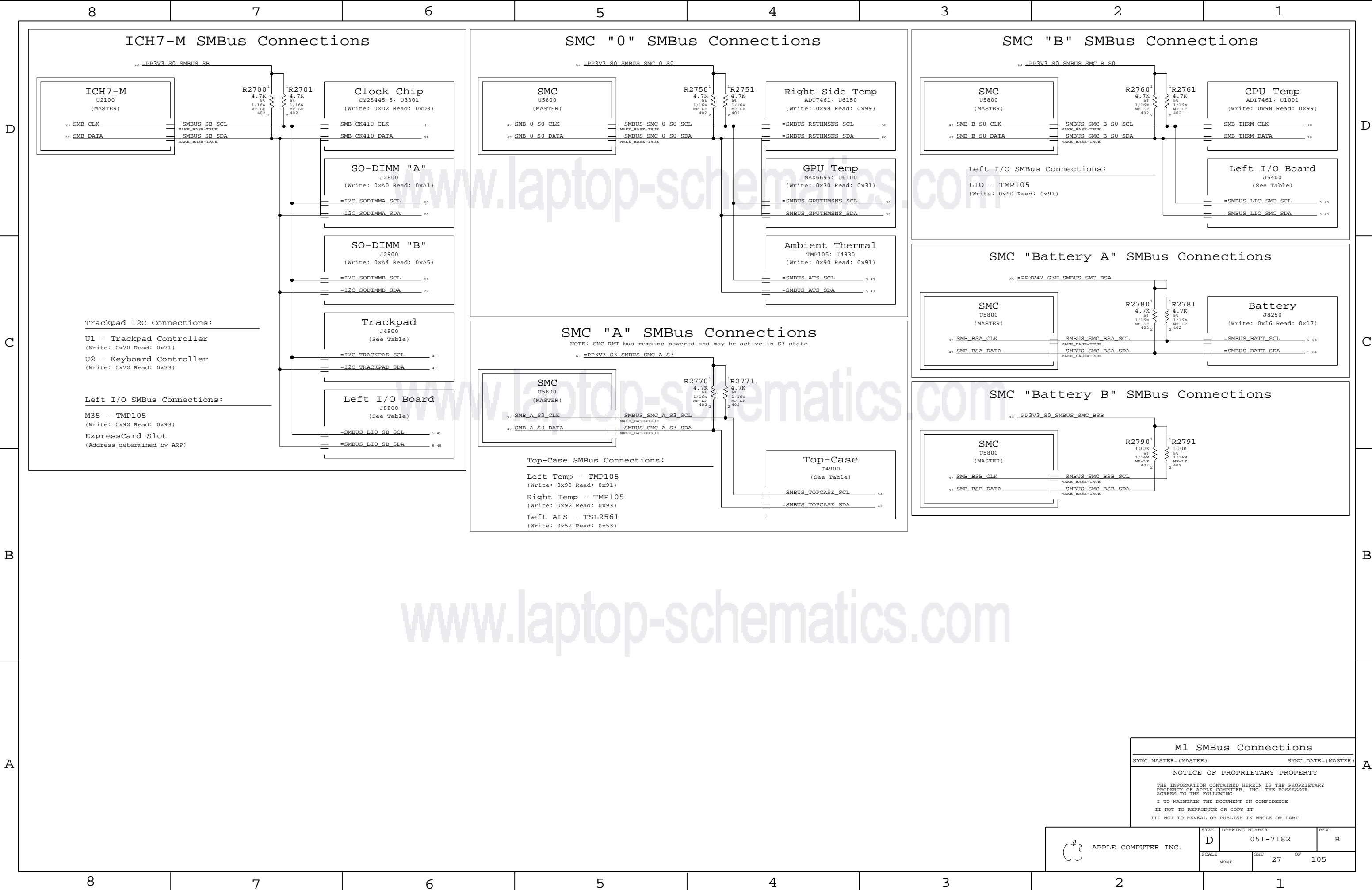


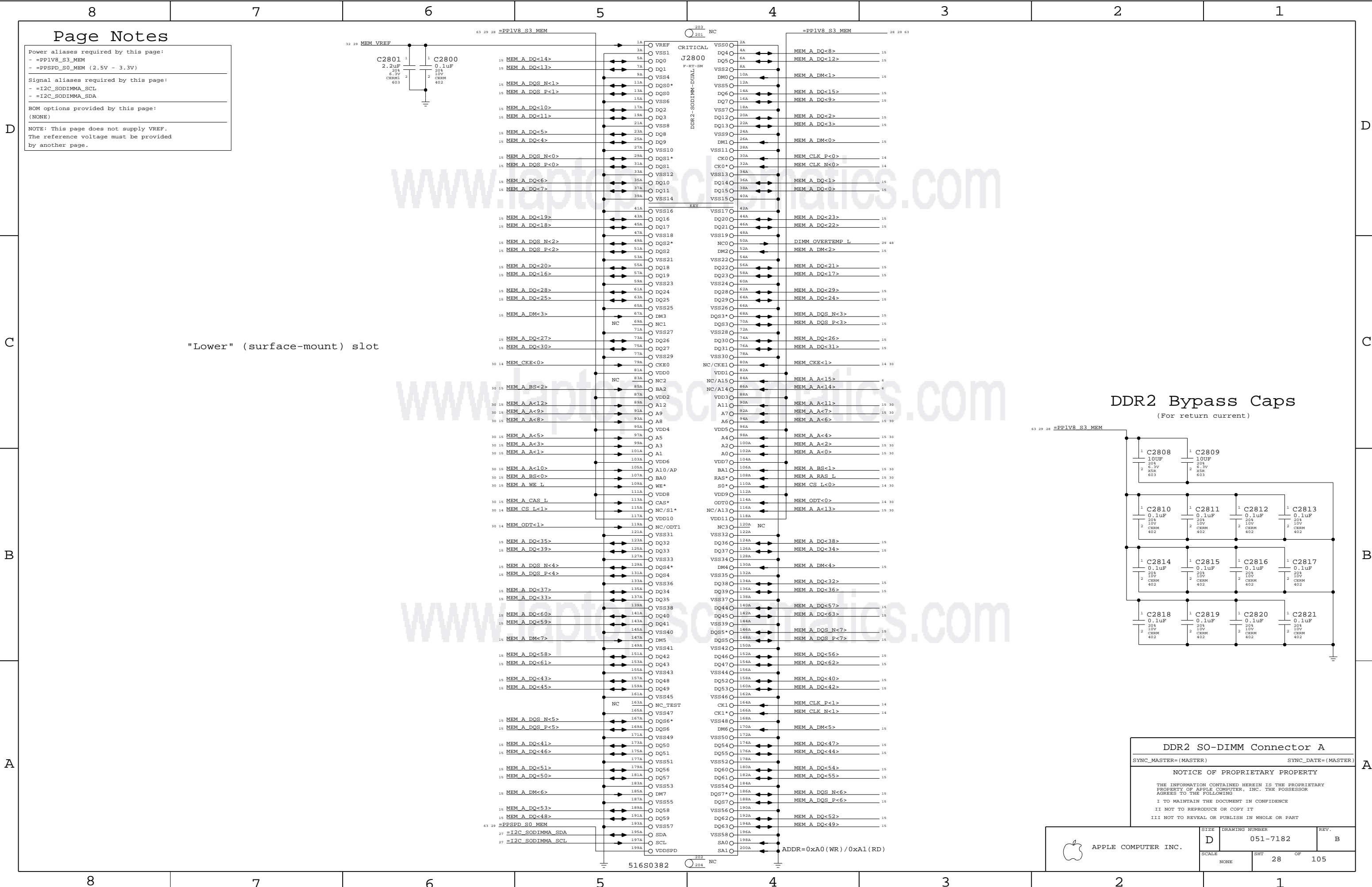
SB Misc	
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	SCALE	SHT	OF
	NONE	26	105



SIZE D	DRAWING NUMBER 051-7182	REV. B
SCALE NONE	SHT 26	OF 105





Page Notes

Power aliases required by this page:

- =PPIV8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

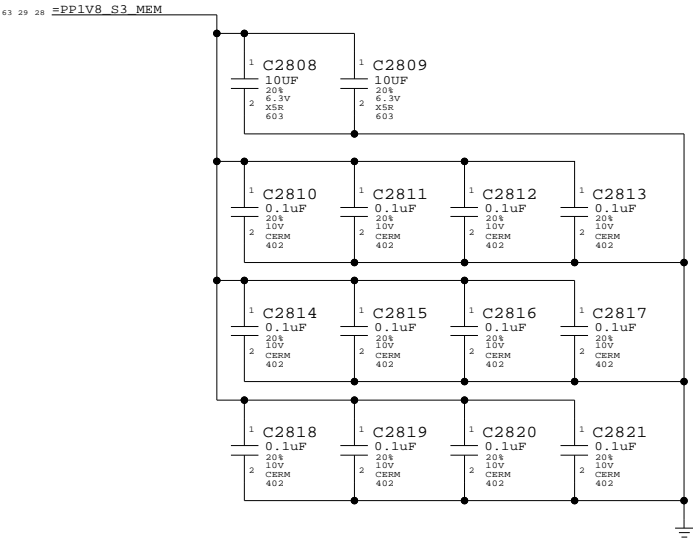
BOM options provided by this page:

(NONE)

NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

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SYNC_DATE=(MASTER)

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SIZE

D

DRAWING NUMBER

051-7182

REV.

B

SCALE

NONE

SHT

28

OF

105

Power aliases required by this page:

- =PPIV8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

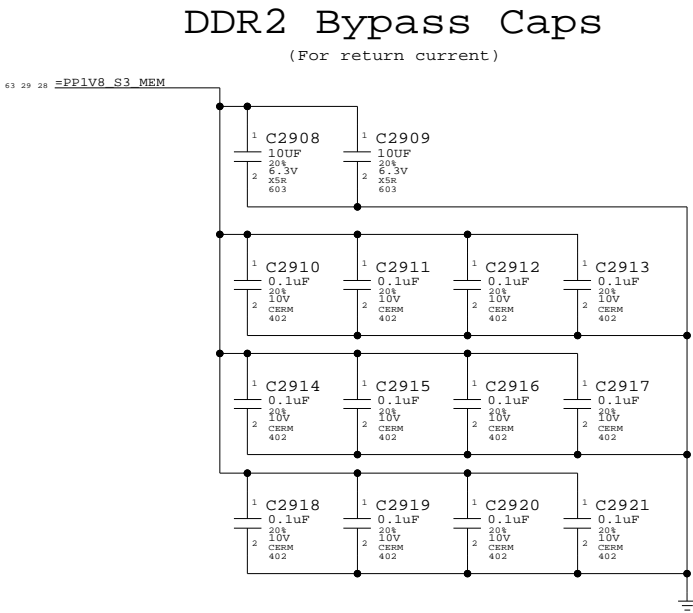
Signal aliases required by this page:

- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:

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NOTE: This page does not supply VREF.
The reference voltage must be provided
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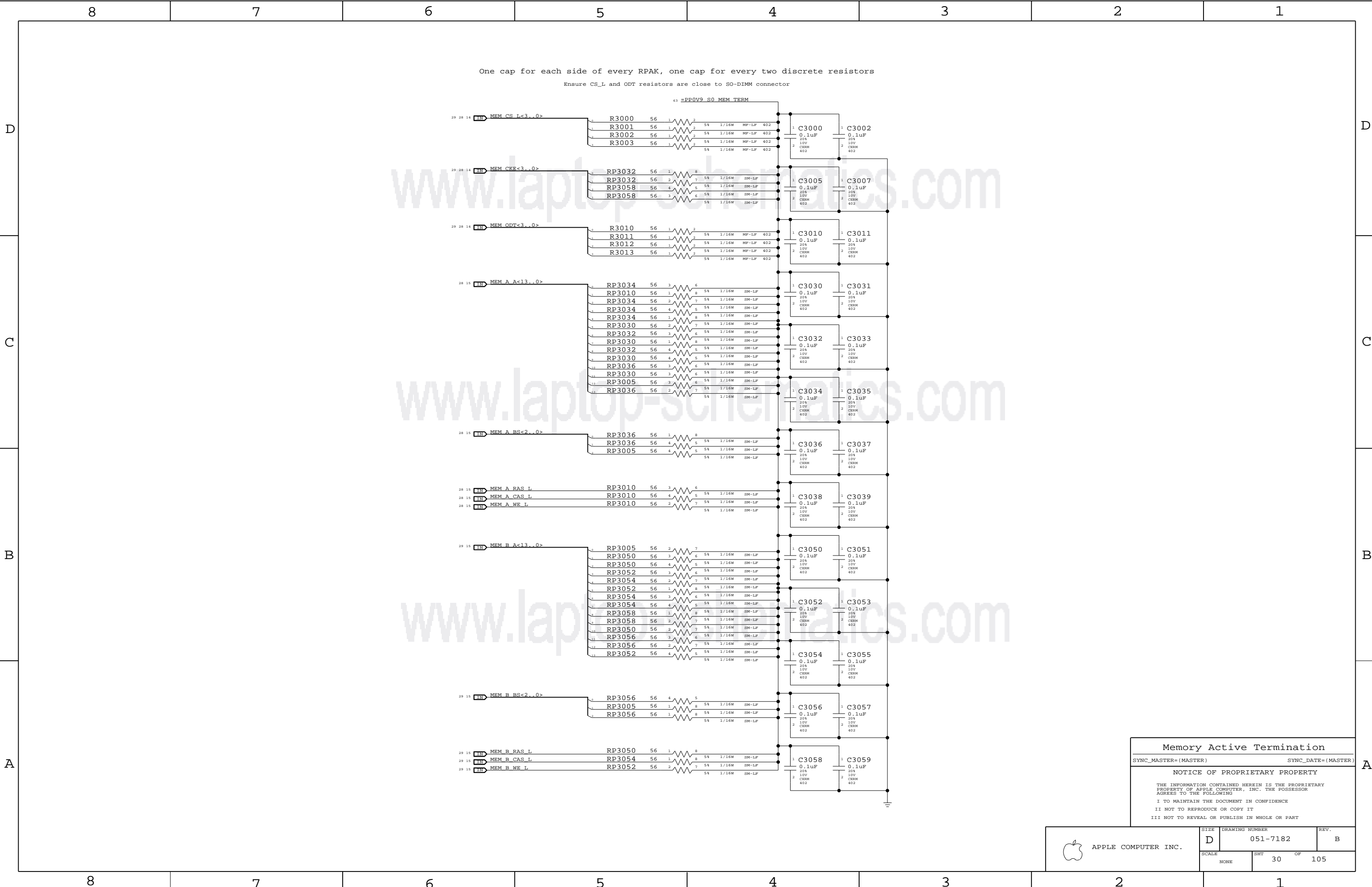
DDR2 Bypass Caps

DDR2 SO-DIMM Connector B	
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Memory Active Termination

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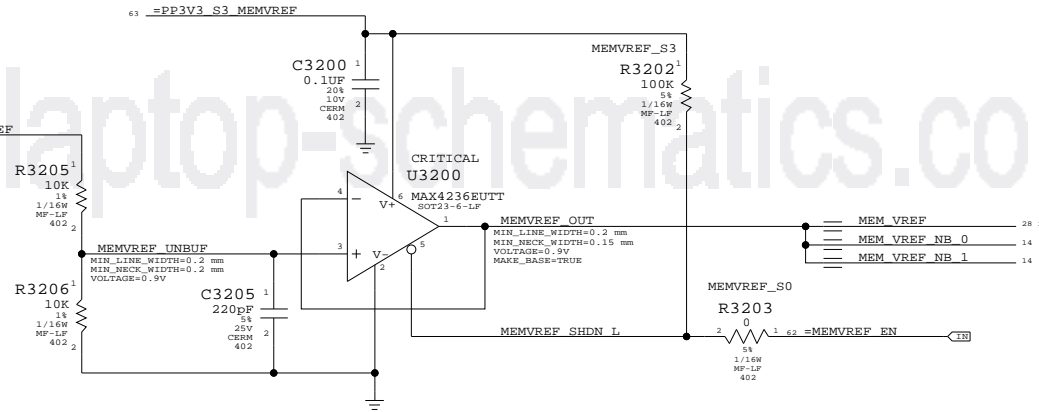
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DDR2 Vref

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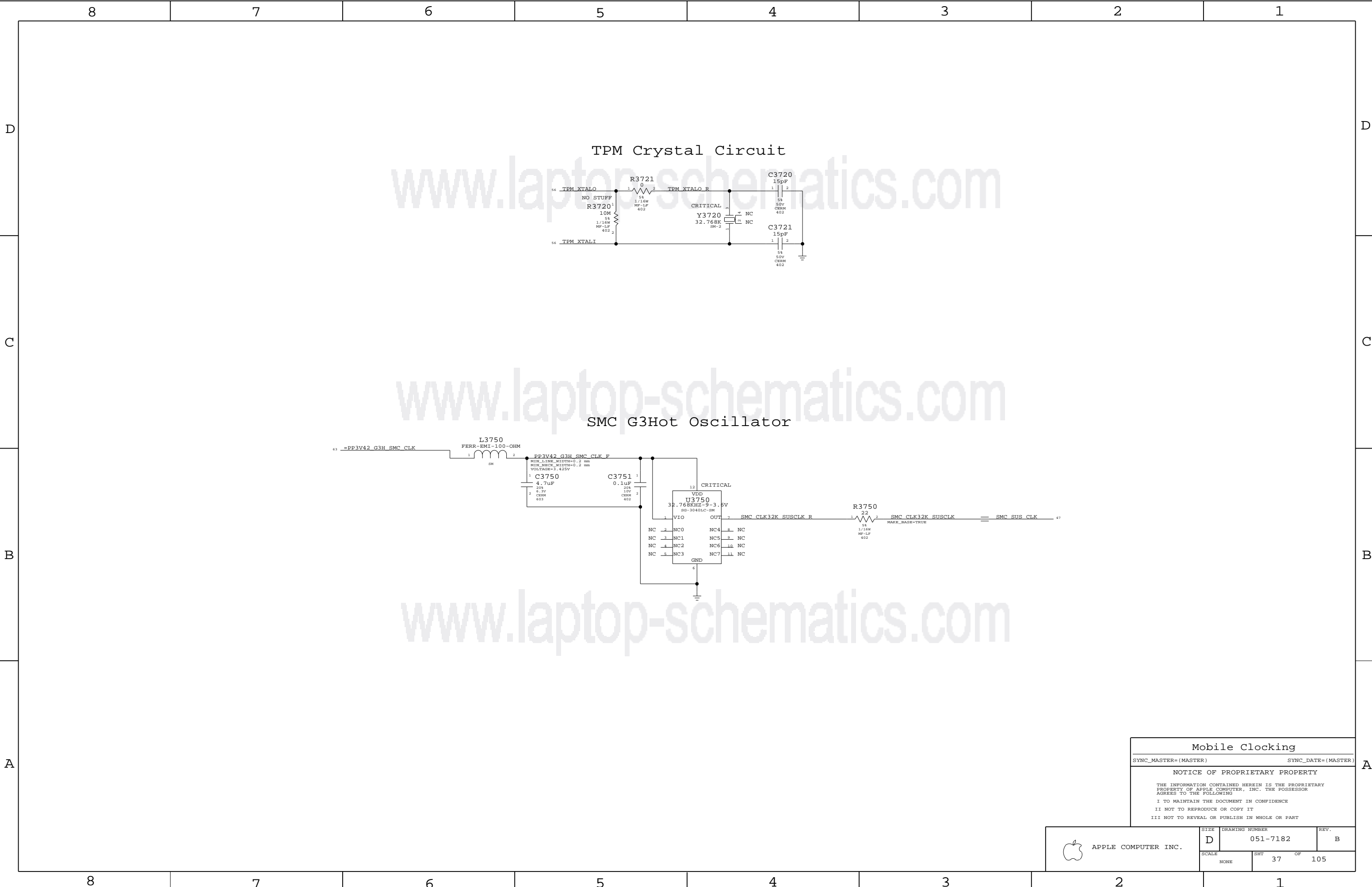
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NONE	32	105



Mobile Clocking

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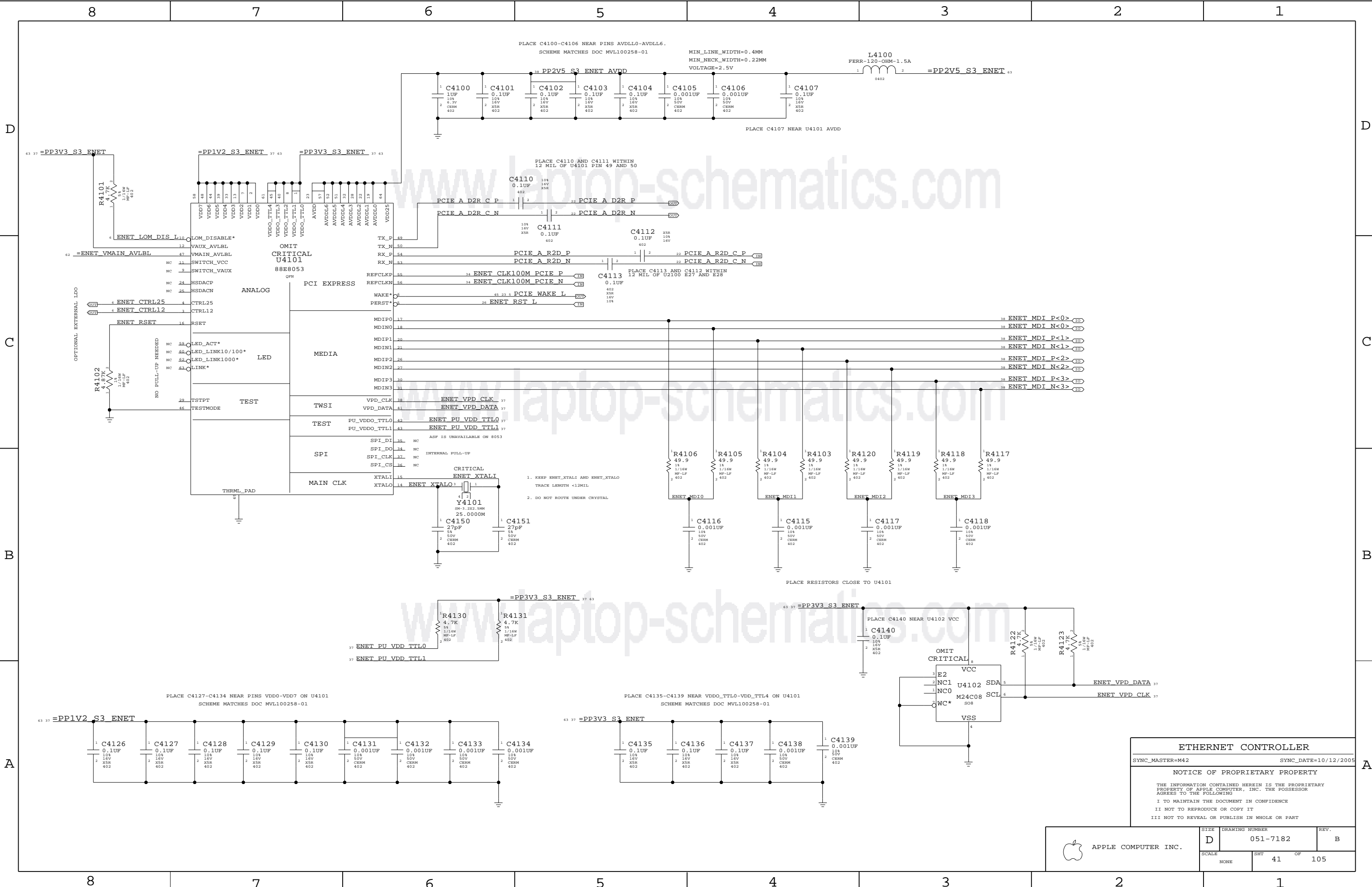
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	SCALE NONE	SHT 37	OF 105



ETHERNET CONTROLLER

SYNC_MASTER=M42 SYNC_DATE=10/12/2005

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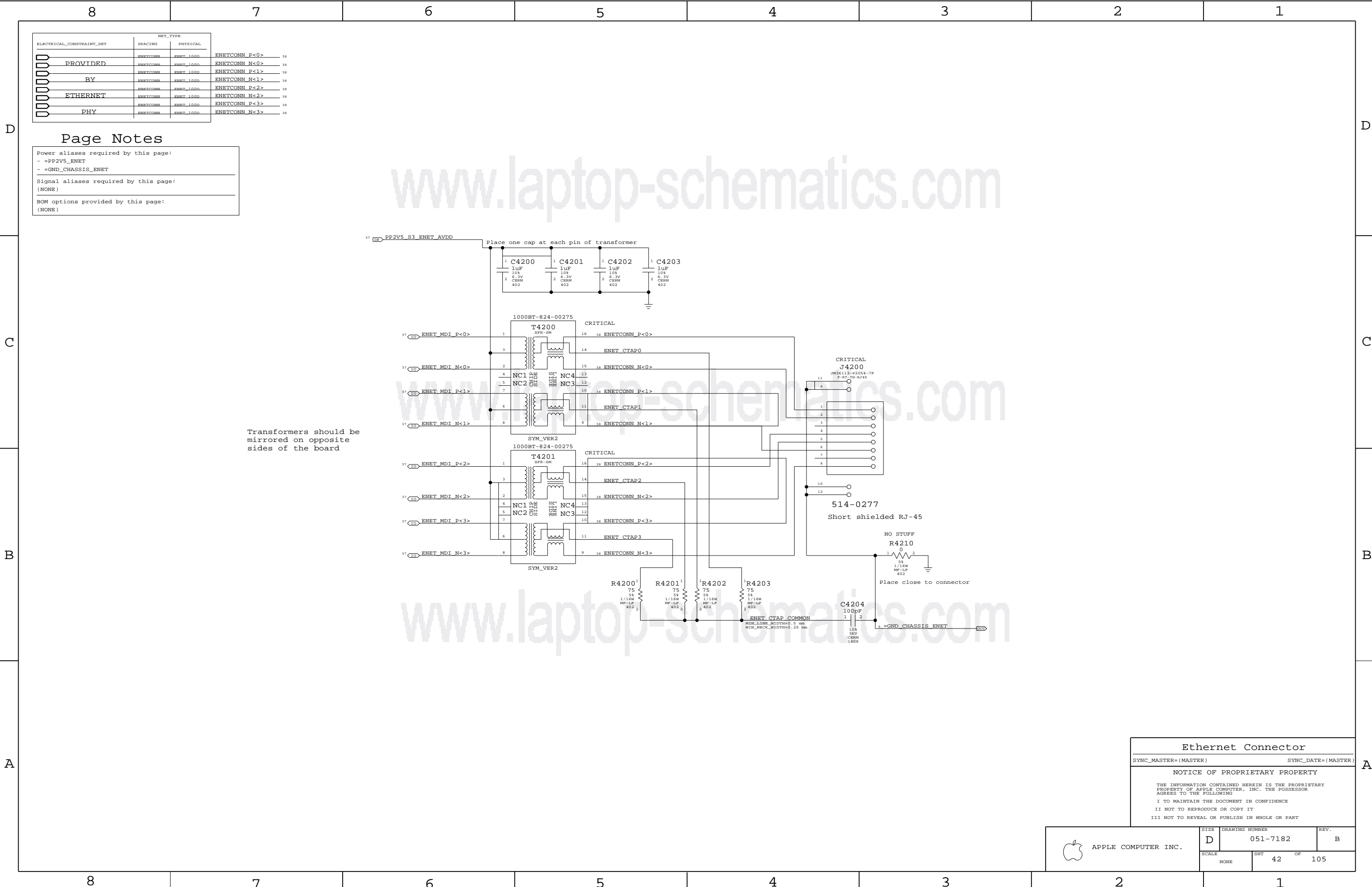
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SCALE		SHT	OF
NONE		41	105



ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	SPACING	PHYSICAL	
PROVIDED	ENETCONN	ENET_100D	ENETCONN_P<0>
	ENETCONN	ENET_100D	ENETCONN_N<0>
	ENETCONN	ENET_100D	ENETCONN_P<1>
BY	ENETCONN	ENET_100D	ENETCONN_N<1>
	ENETCONN	ENET_100D	ENETCONN_P<2>
	ENETCONN	ENET_100D	ENETCONN_N<2>
ETHERNET	ENETCONN	ENET_100D	ENETCONN_P<3>
	ENETCONN	ENET_100D	ENETCONN_N<3>
	ENETCONN	ENET_100D	ENETCONN_N<3>
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	ENETCONN	ENET_100D	ENETCONN_N<3>

Page Notes

Power aliases required by this page:
- =PP2V5_ENET
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Transformers should be mirrored on opposite sides of the board

Ethernet Connector

SYNC_MASTER=(MASTER)

SYNC_DATE=(MASTER)

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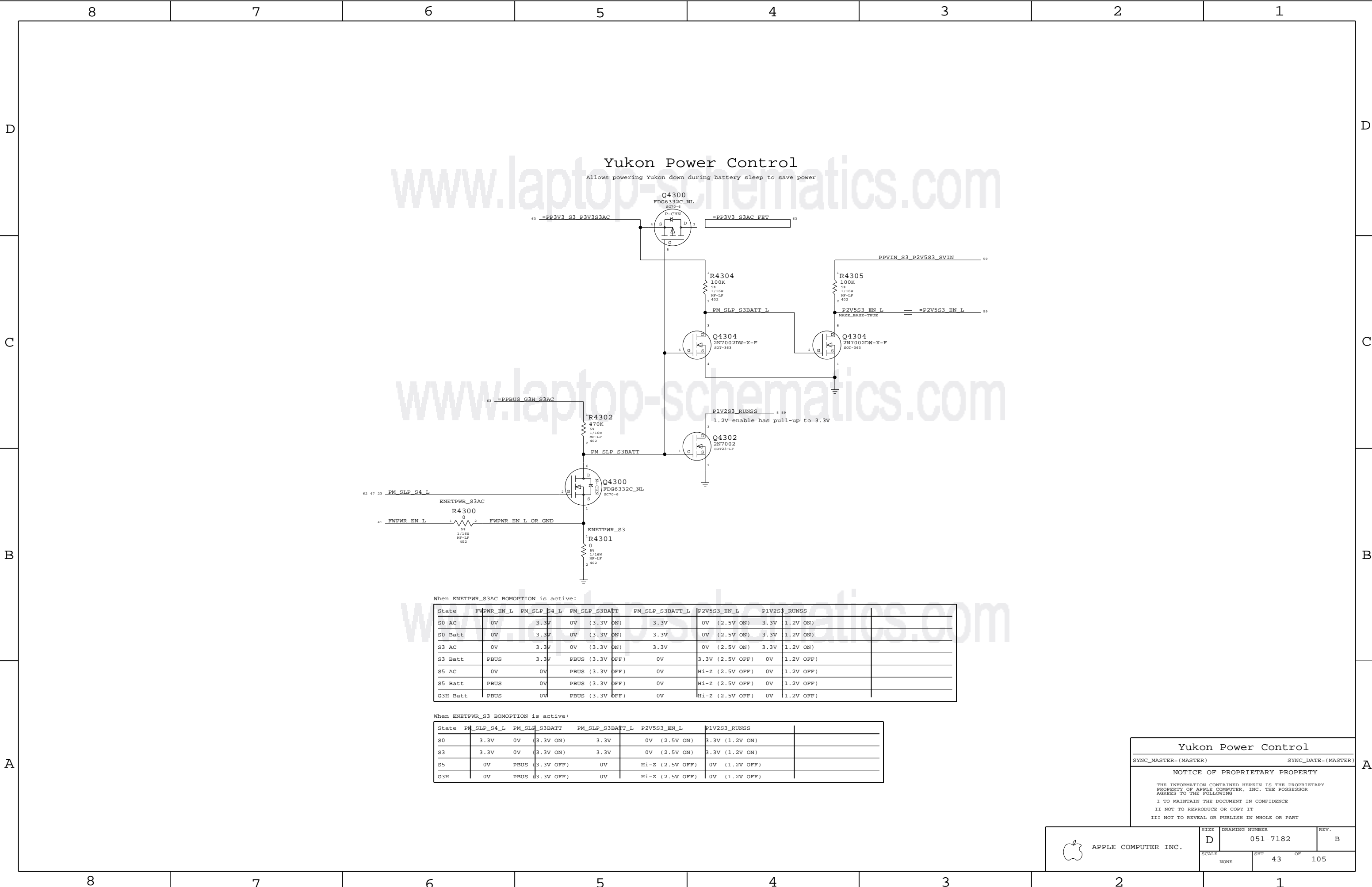
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NONE		42	105



PAGE NOTES

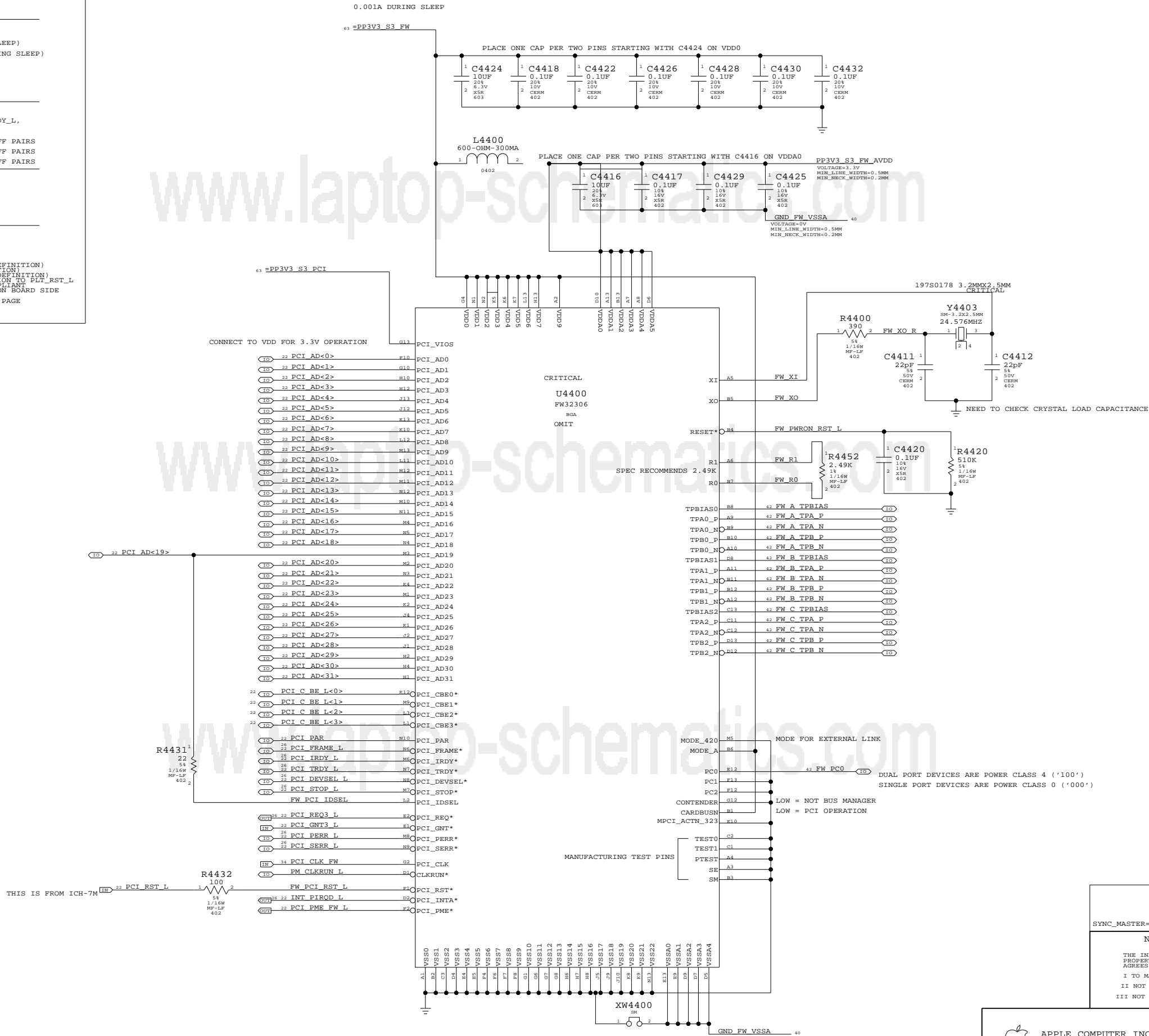
INPUT
=PP3V3_S0_FW - 3.3V POWER FOR FIREWIRE (MOBILE: OFF DURING SLEEP)
=PP3V3_S0_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)
PCI_GNT3_L - PCI GRANT FROM SB
PCI_CLK_FW - NEED TO REFERENCE TO ALIAS PAGE
PCI_RST_L - PCI RESET FROM SB
FW_PC0 - FIREWIRE POWER CLASS IDENTIFIER

INPUT/OUTPUT
PCI_AD<0..31>, PCI_C_BE_L<0..3>, PCI_FRAME_L, PCI_IRDY_L, PCI_TRDY_L,
PCI_DEVSEL_L, PCI_STOP_L, PCI_PAR, PCI_PERR_L, PCI_SERR_L
FW_A_TPA_P/N, FW_A_TPB_P/N, FW_A_TPBAS - PORT 0 FIREWIRE DIFF PAIRS
FW_B_TPA_P/N, FW_B_TPB_P/N, FW_B_TPBAS - PORT 1 FIREWIRE DIFF PAIRS
FW_C_TPA_P/N, FW_C_TPB_P/N, FW_C_TPBAS - PORT 2 FIREWIRE DIFF PAIRS

OUTPUT
PCI_REQ3_L - PCI REQUEST TO SB
PM_CLKRUN_L - CLOCK-RUN PCI PROTOCOL
INT_PIRQD_L - INTERRUPT TO SB
PCI_PME_FW_L - DEDICATED PME FOR FIREWIRE (SB GPIO1)

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
6/20/2005 - BGA VERSION OF FW323-06 ADDED
6/21/2005 - CHANGED INT* TO INT_PIRQD_L (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED PCI_ID TO AD19 (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED REQ/GNT TO REQ3/GNT3 (PER ARCHITECTURAL DEFINITION)
6/22/2005 - ADDED 510K PULL-DOWN ON RST* AND REMOVED CONNECTION TO PLT_RST_L
6/22/2005 - CHANGED CLK_PME DIFF PAIR NAMES TO BE RE-USE COMPLIANT
6/22/2005 - REMOVED CONSTRAINT SETS AS THEY WILL BE MANAGED ON BOARD SIDE
6/22/2005 - REMOVED C4421 - REDUNDANT
6/22/2005 - BRING OUT PC0 CONNECTION TO BE CONNECTED ON PORT PAGE
7/26/2005 - CONNECTED PIN E10 TO GND



FIREWIRE CONTROLLER

SYNC_MASTER=(M42) SYNC_DATE=08/29/2005

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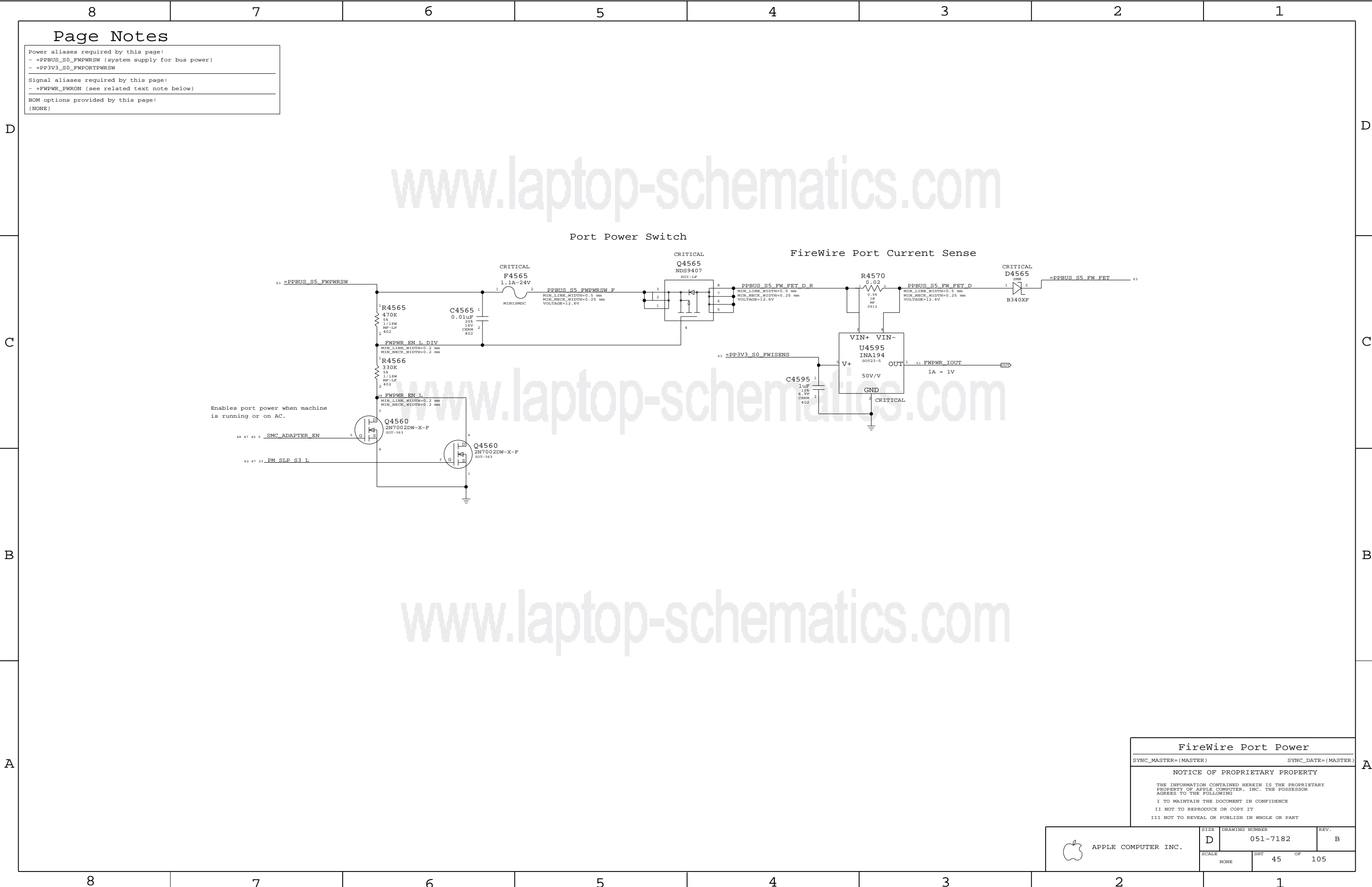
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7182	REV. B
	SCALE NONE	SHT 44	OF 105



Page Notes

Power aliases required by this page:

- =PPBUS_S0_FWPWRSW (system supply for bus power)
- =PP3V3_S0_FWPORTPWRSW

Signal aliases required by this page:

- =FWPWR_PWRON (see related text note below)

BOM options provided by this page:

(NONE)

FireWire Port Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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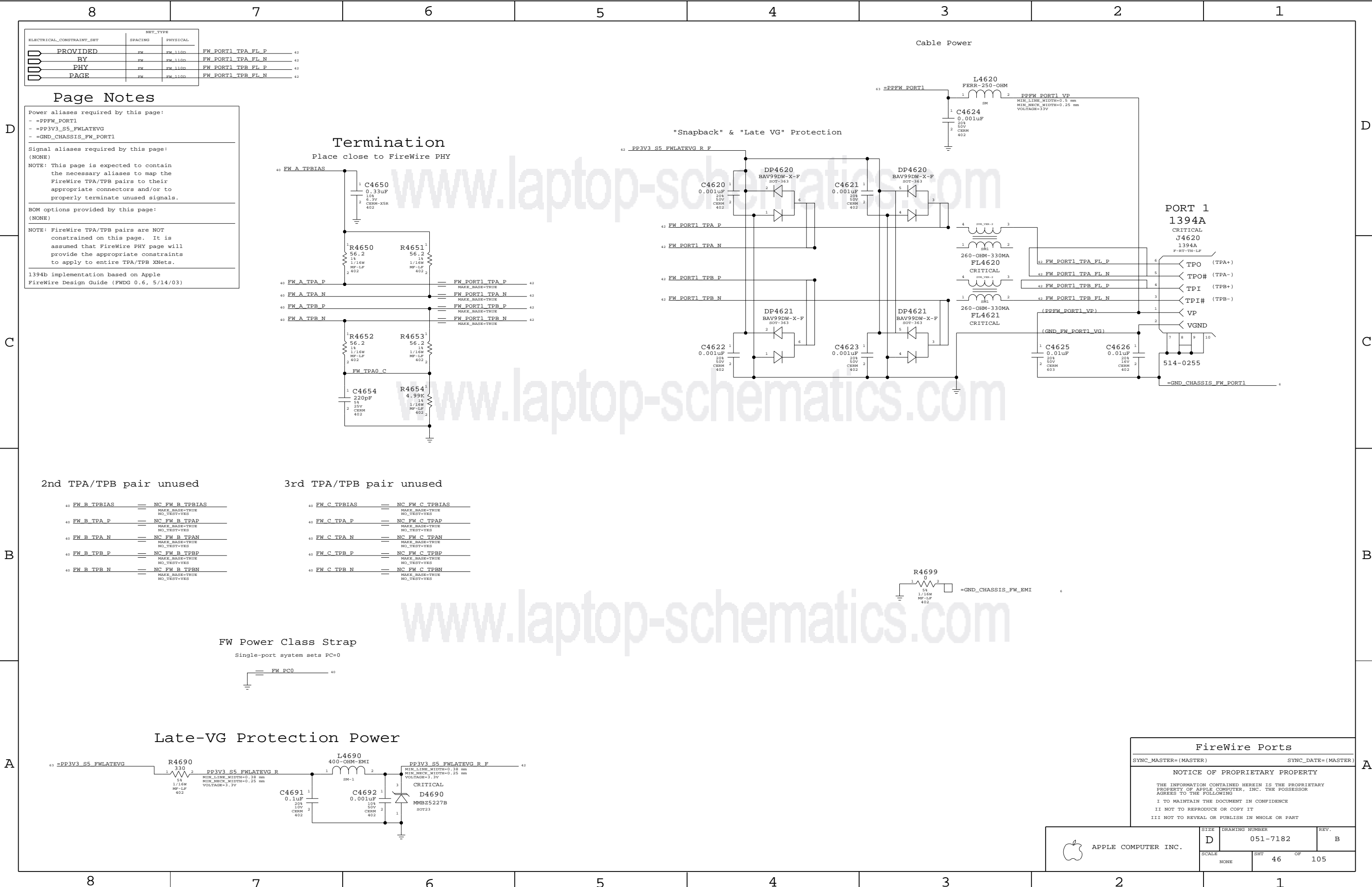
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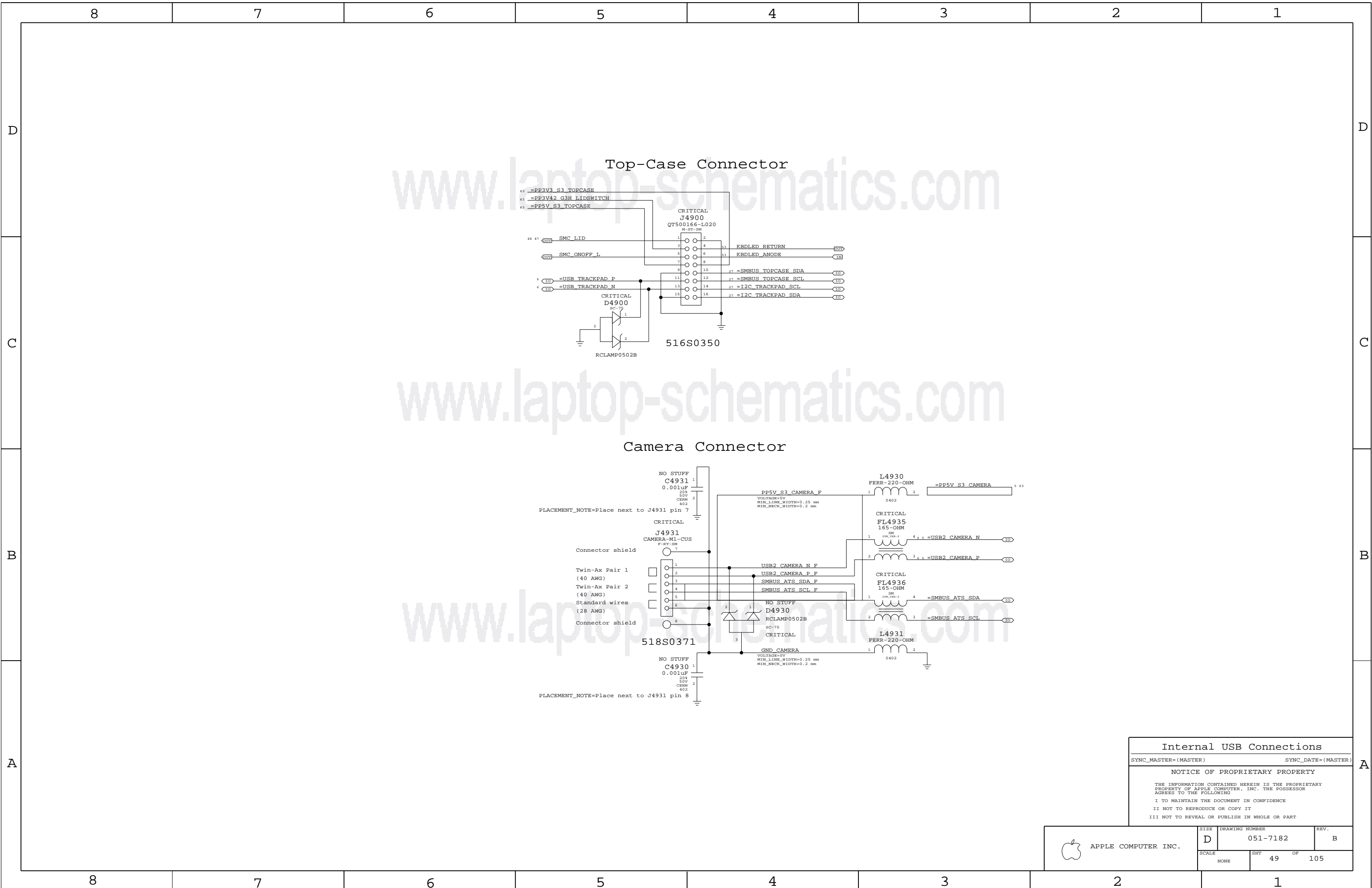
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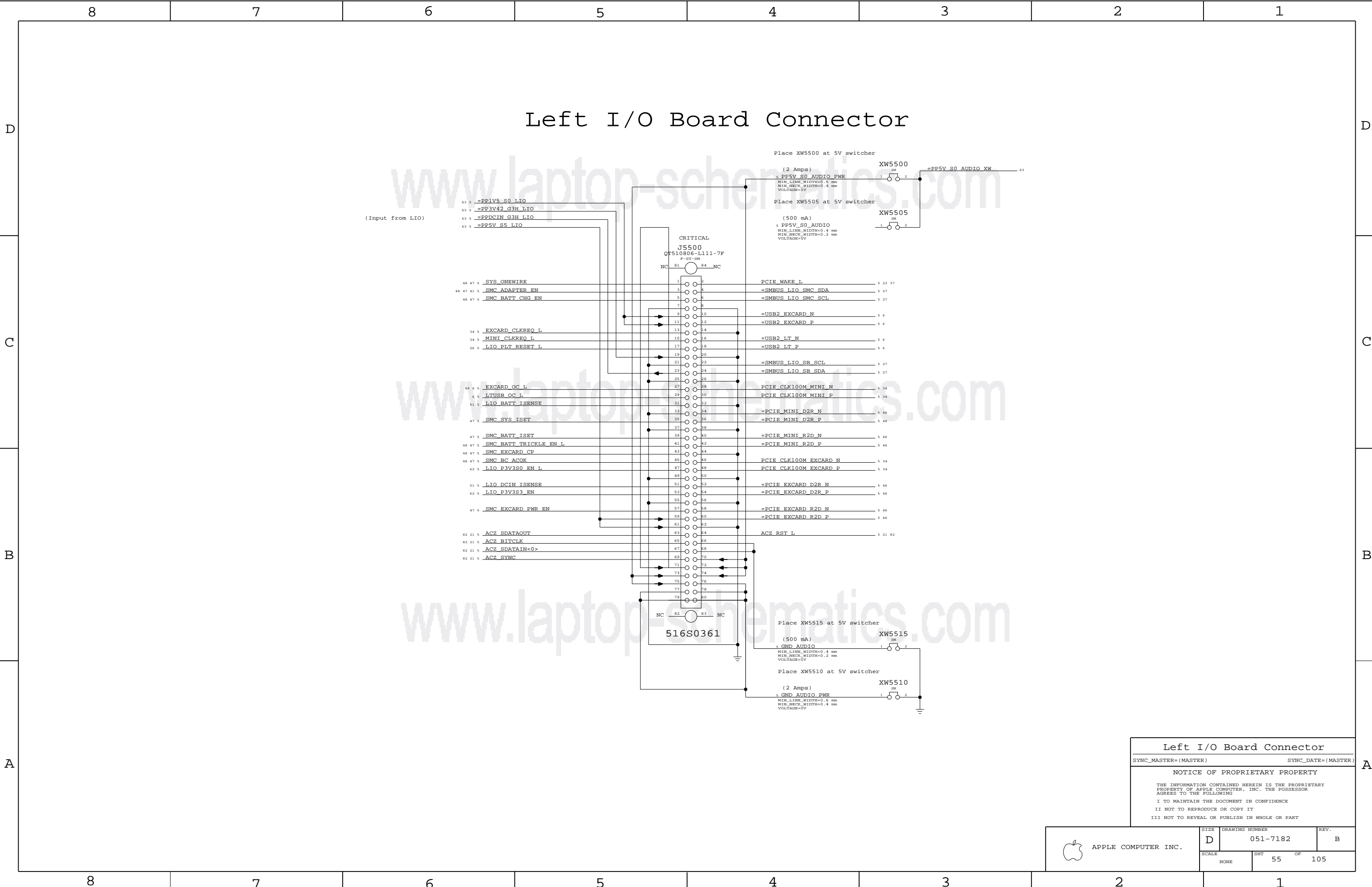
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7182	REV. B
	SCALE NONE	SHT 45	OF 105







Left I/O Board Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-7182	B
SCALE		SHT	OF
NONE		55	105



PCI-E Connections

SYNC_MASTER=(MASTER)

SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.

SCALE
NONE

D

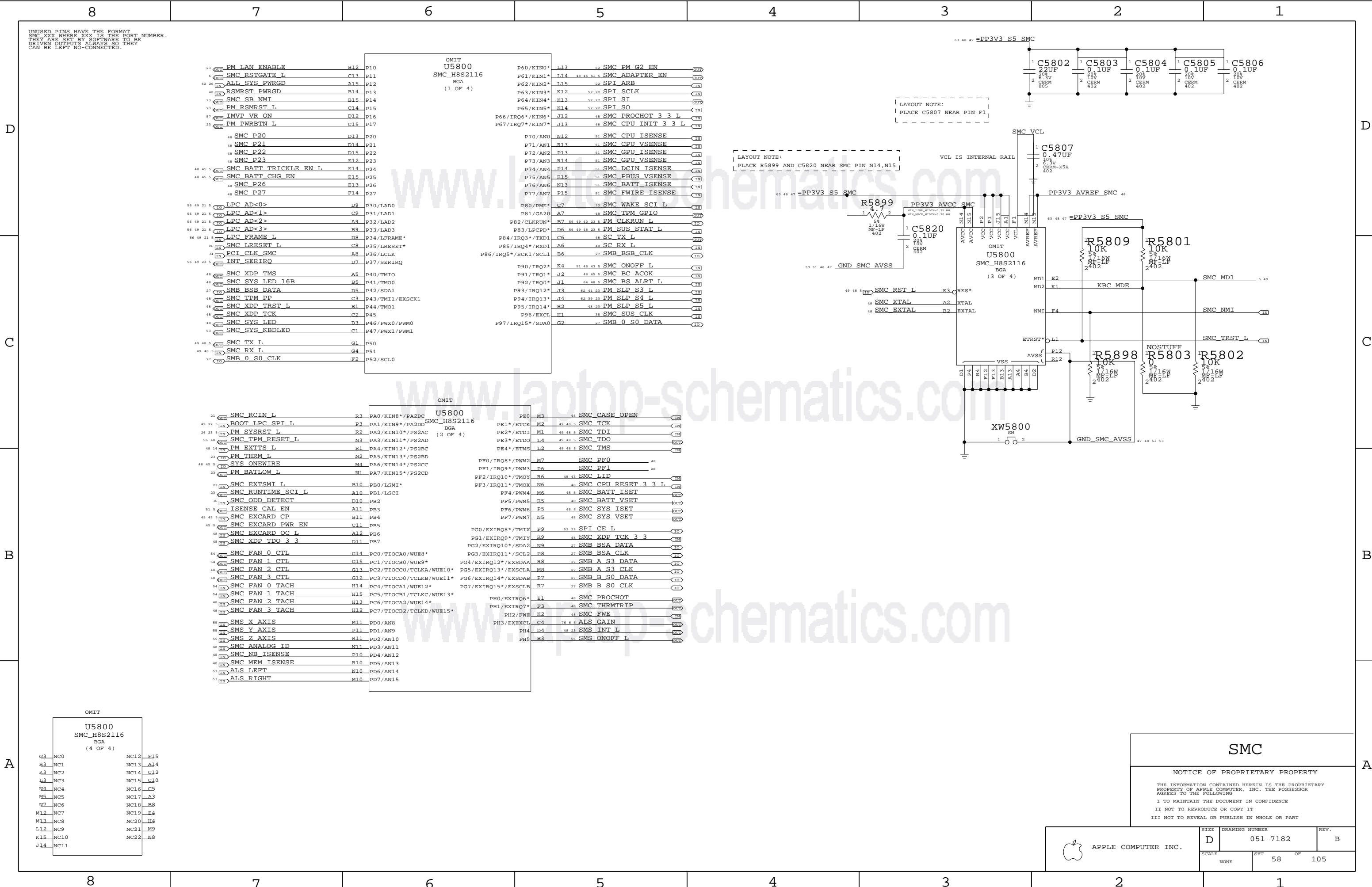
DRAWING NUMBER
051-7182

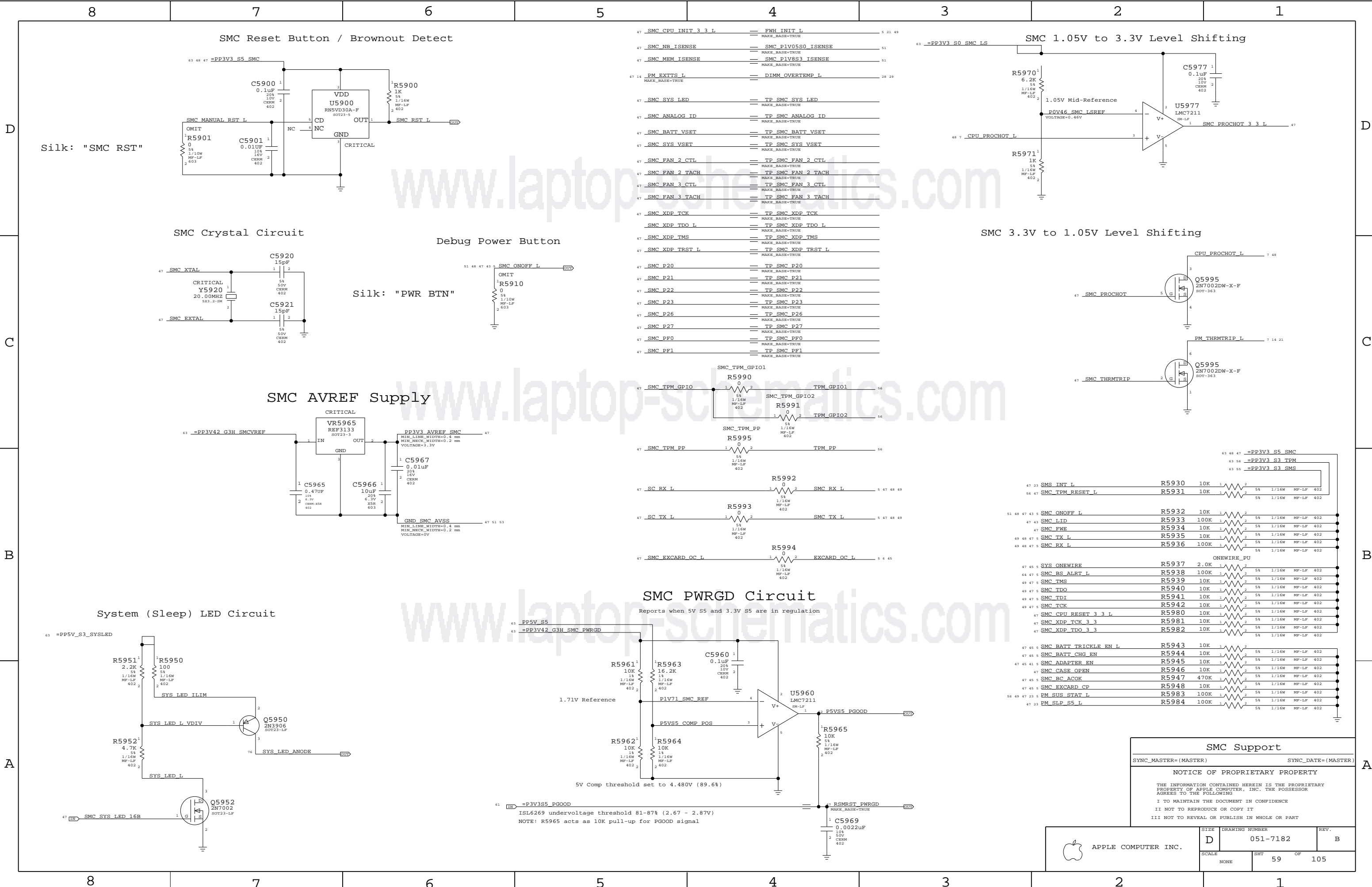
SHT
57

OF
105

B

REV.





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C

B

A

D

C

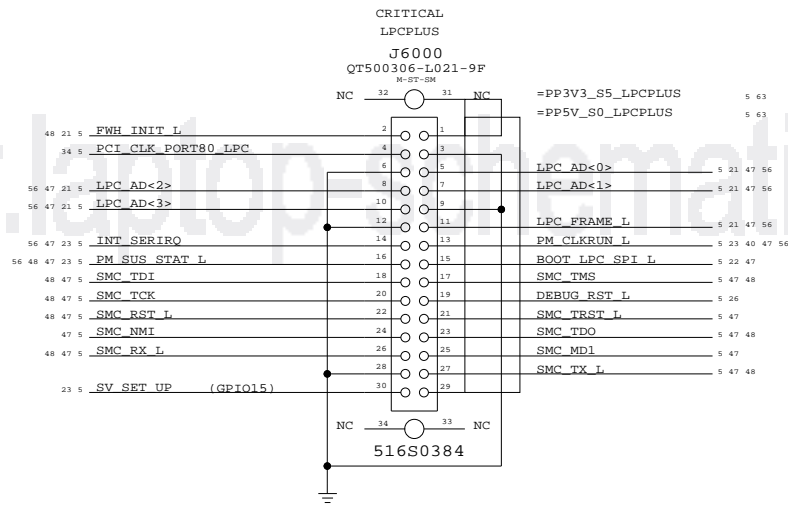
B

A

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www.laptop-schematics.com

www.laptop-schematics.com



LPC+ Debug Connector

SYNC_MASTER=M42 SYNC_DATE=07/20/2005

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APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-7182 REV. B

SCALE NONE SHT 60 OF 105

Placement note:
Place near GPU center

Placement note:
Place in between VRAM

Placement note:
Keep all 4 XWs as close to U6100 as possible

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,0,1/16W,0402	C6120		HSTHMSNS_NOT

Placement note:
place near CPU center

Q6190
2N3904LF
SOT23

CPUTHMSNS_DIO_P

R6190
56
1/16W
56K 1%
402

THRM_CPU_DX_P

CPUTHMSNS_DIO_N

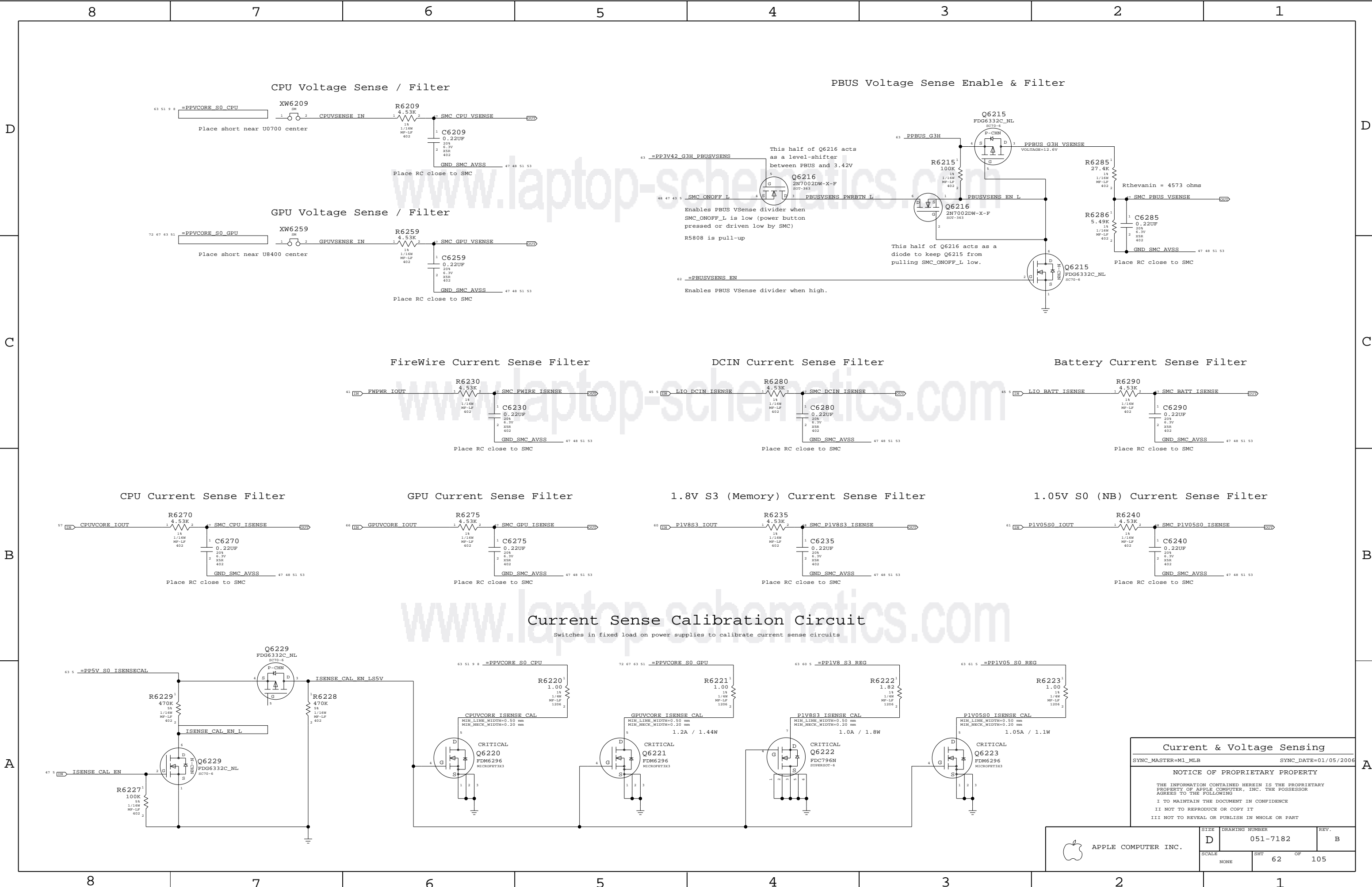
R6191
56
1/16W
56K 1%
402

THRM_CPU_DX_N

Layout note:
Minimize stubs between
these R's and R1001 & R1002

R1001 / R1002 are not currently BOMOPTIONed. Can not
programatically unstuff those parts to stuff these.

Thermal Sensors	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)
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D

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B

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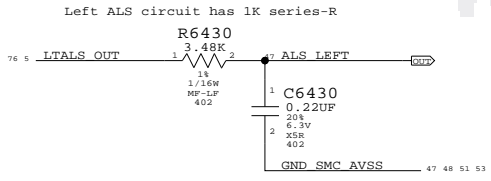
D

C

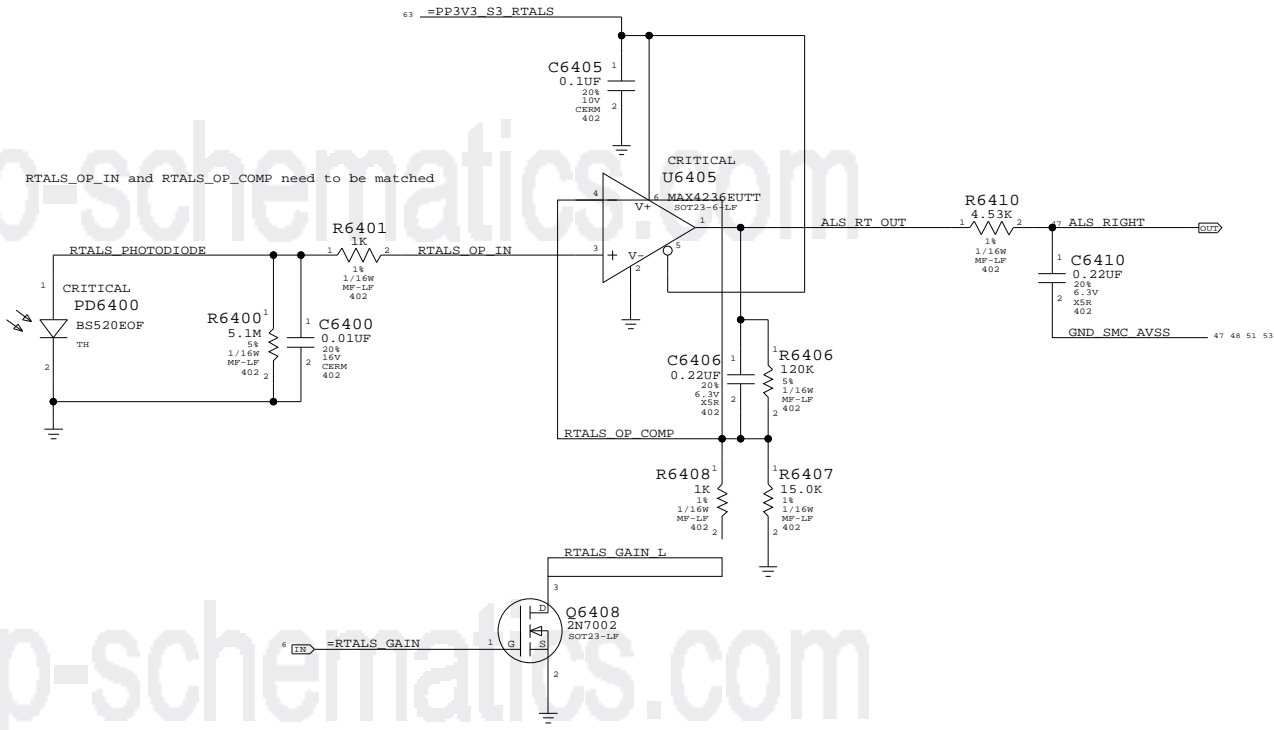
B

A

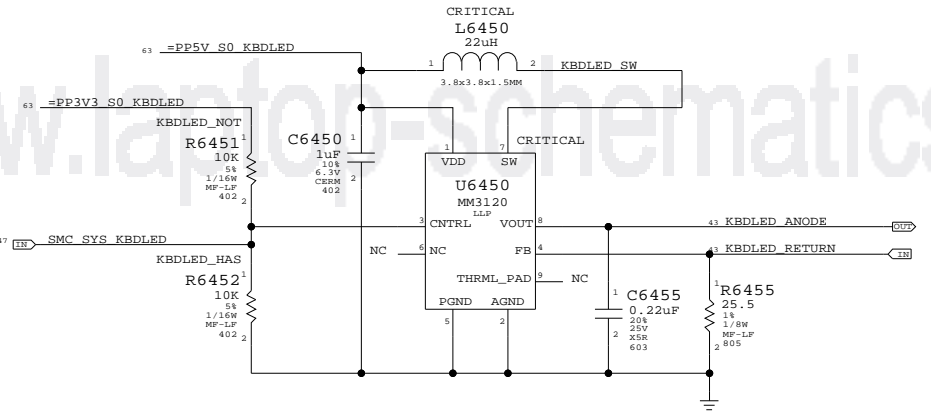
Left ALS Filter



Right ALS Circuit

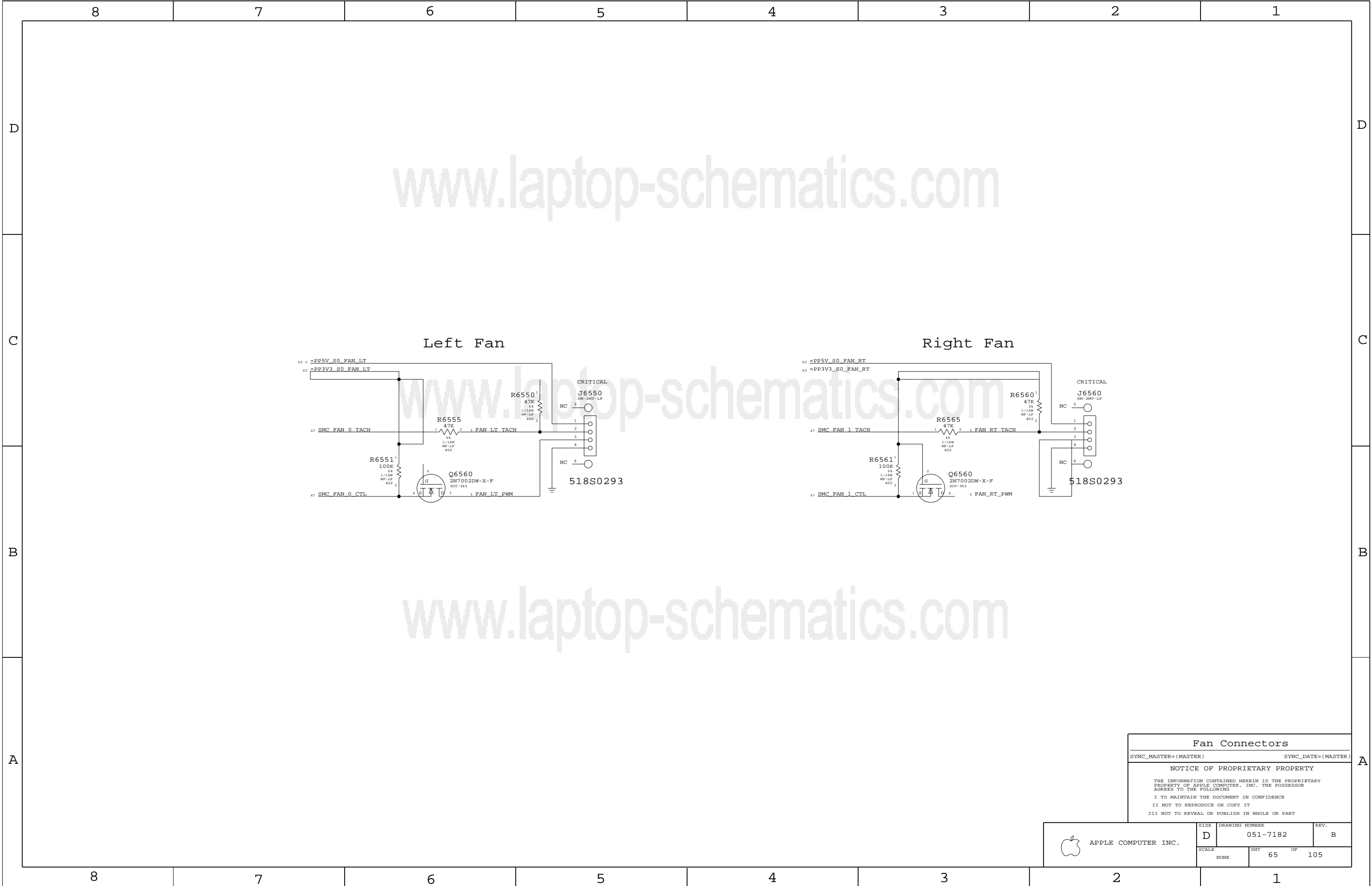


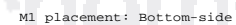
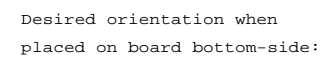
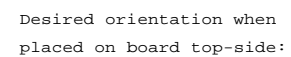
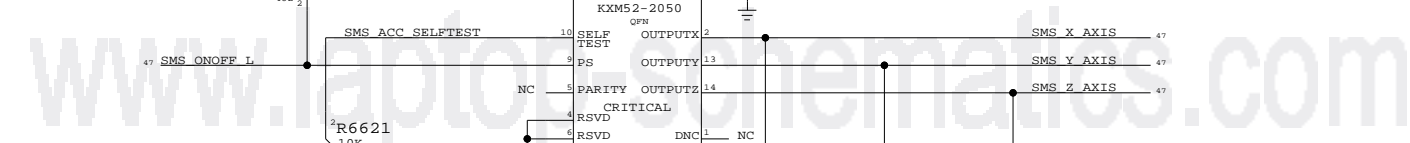
Keyboard LED Driver




ALS Support		
SYNC_MASTER=(MASTER)		SYNC_DATE=(MASTER)
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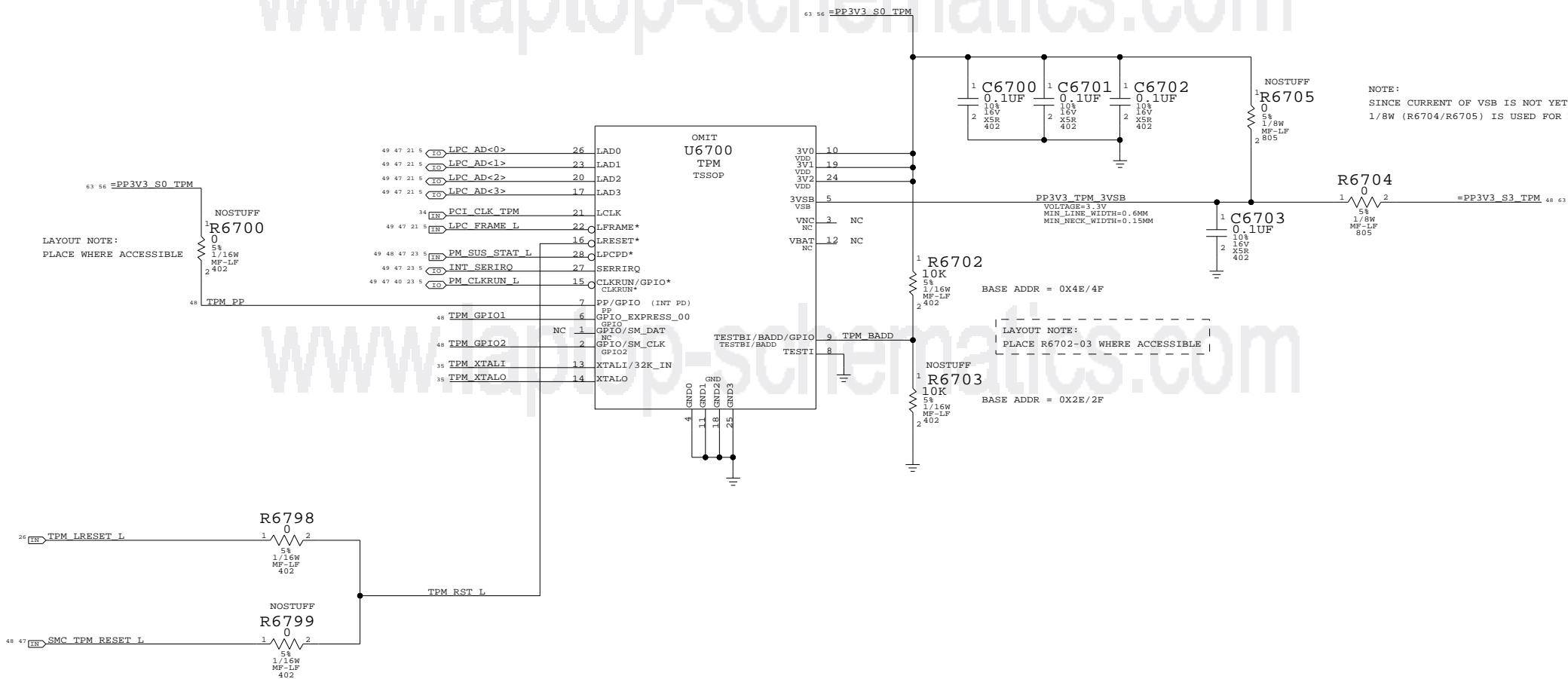
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7182	REV. B
	SCALE NONE	SHT 64 OF 105	





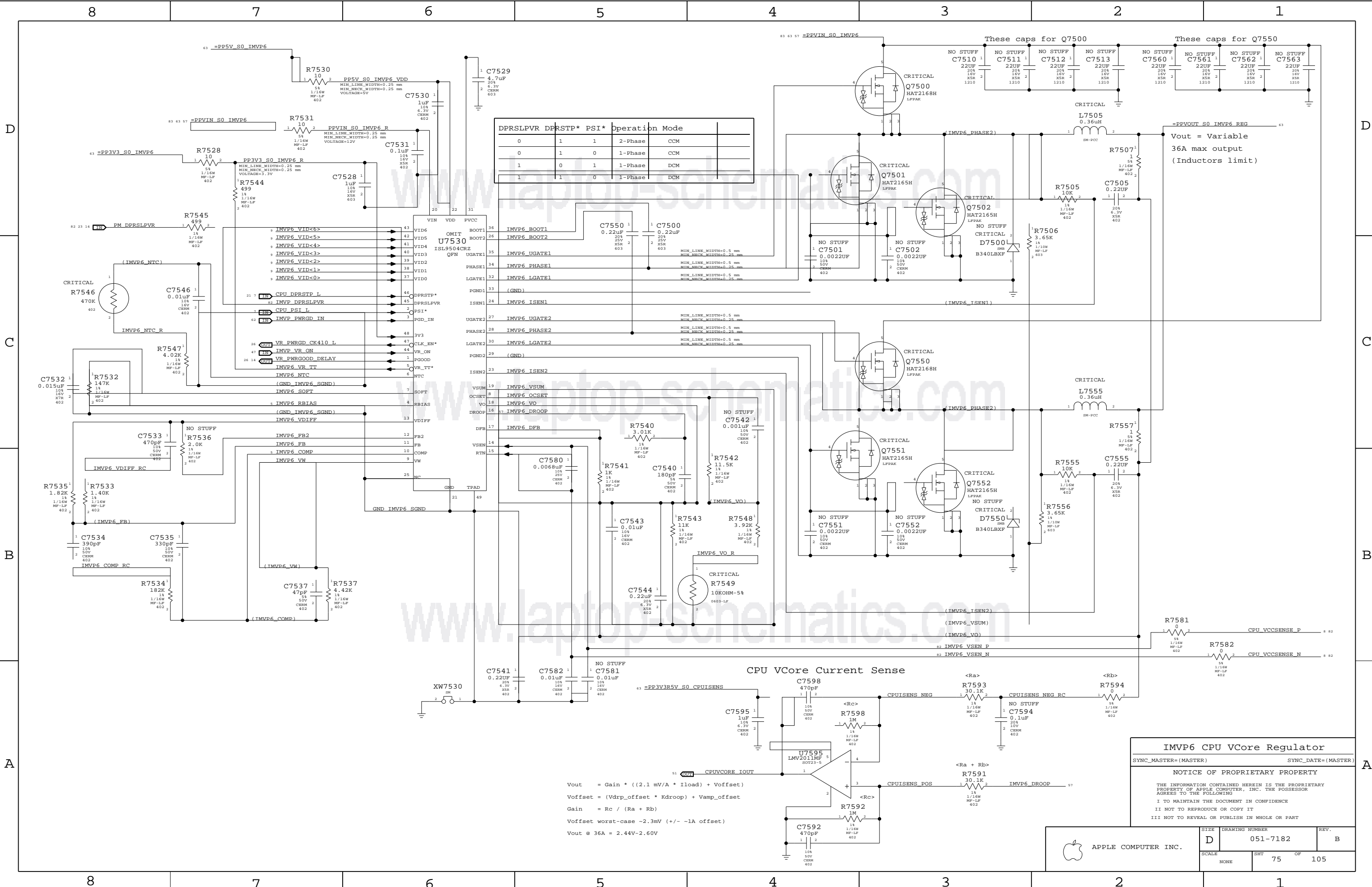
 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7182	B
	SCALE	SHT	OF
	NONE	66	105

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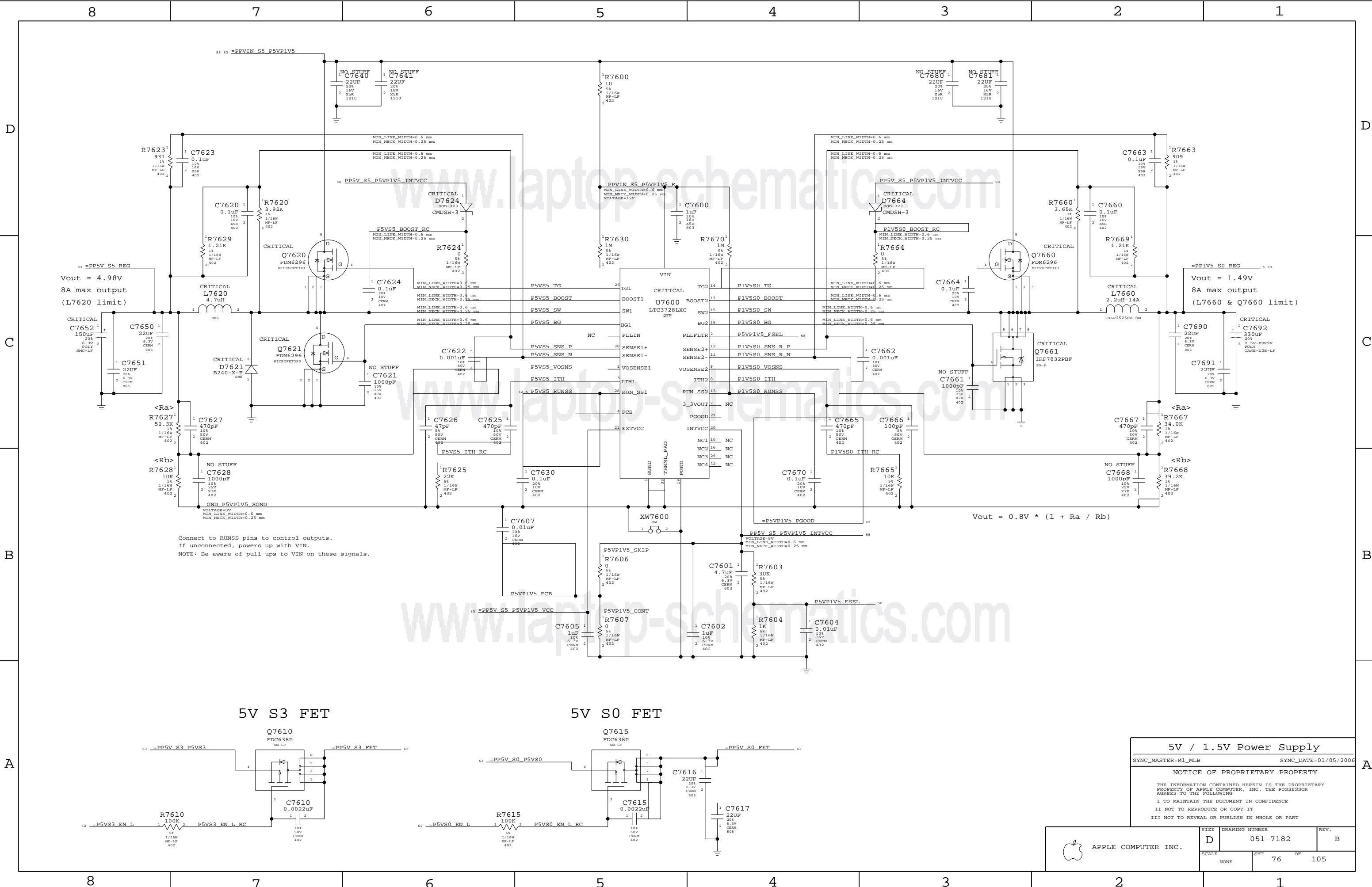


TPM	
SYNC_MASTER=M38	SYNC_DATE=11/16/2005
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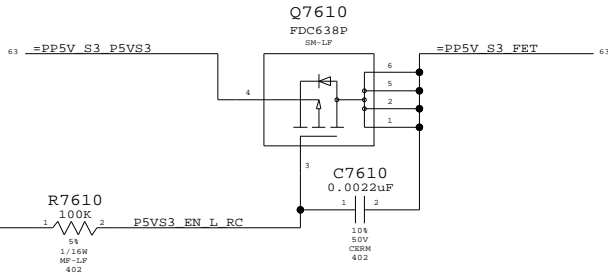
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7182	REV. B
	SCALE NONE	SHT 67	OF 105



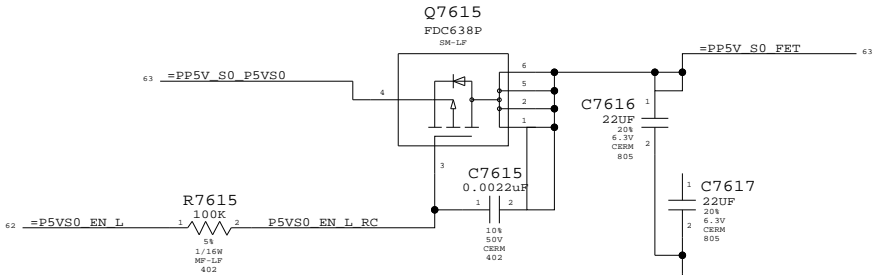
$$V_{out} = \text{Gain} * ((2.1 \text{ mV/A} * I_{load}) + V_{offset})$$
$$V_{offset} = (V_{drp_offset} * K_{droop}) + V_{amp_offset}$$
$$\text{Gain} = R_c / (R_a + R_b)$$
$$V_{offset \text{ worst-case}} \sim 2.3\text{mV (+/- -1A offset)}$$
$$V_{out @ 36A} = 2.44\text{V} - 2.60\text{V}$$



5V S3 FET



5V S0 FET



5V / 1.5V Power Supply

SYNC_MASTER=M1_MLB SYNC_DATE=01/05/2006

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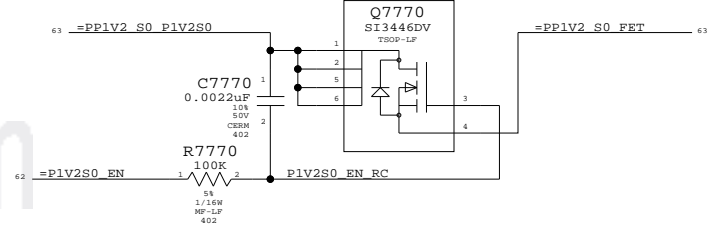
APPLE COMPUTER INC.

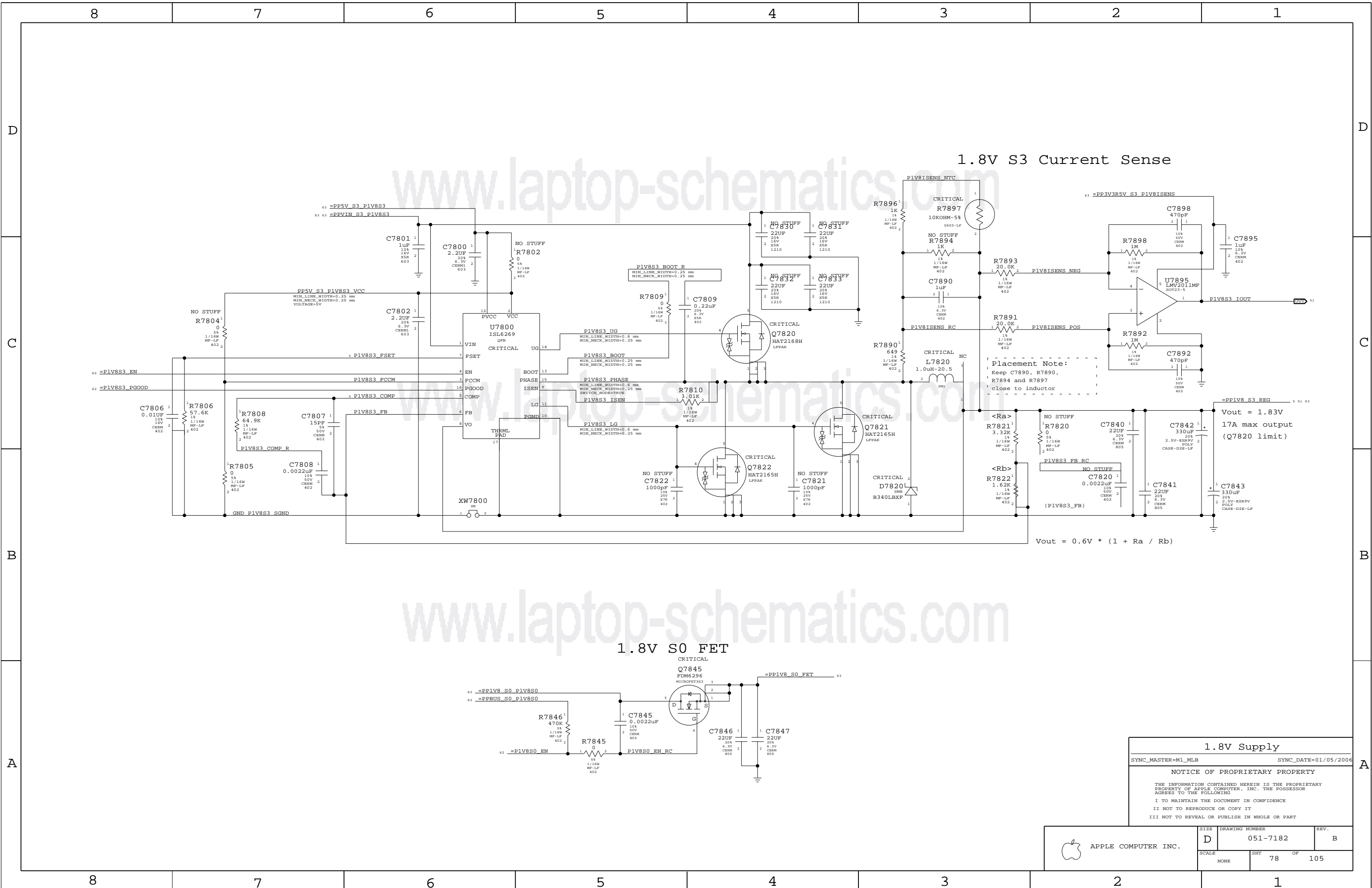
SIZE D DRAWING NUMBER 051-7182 REV. B

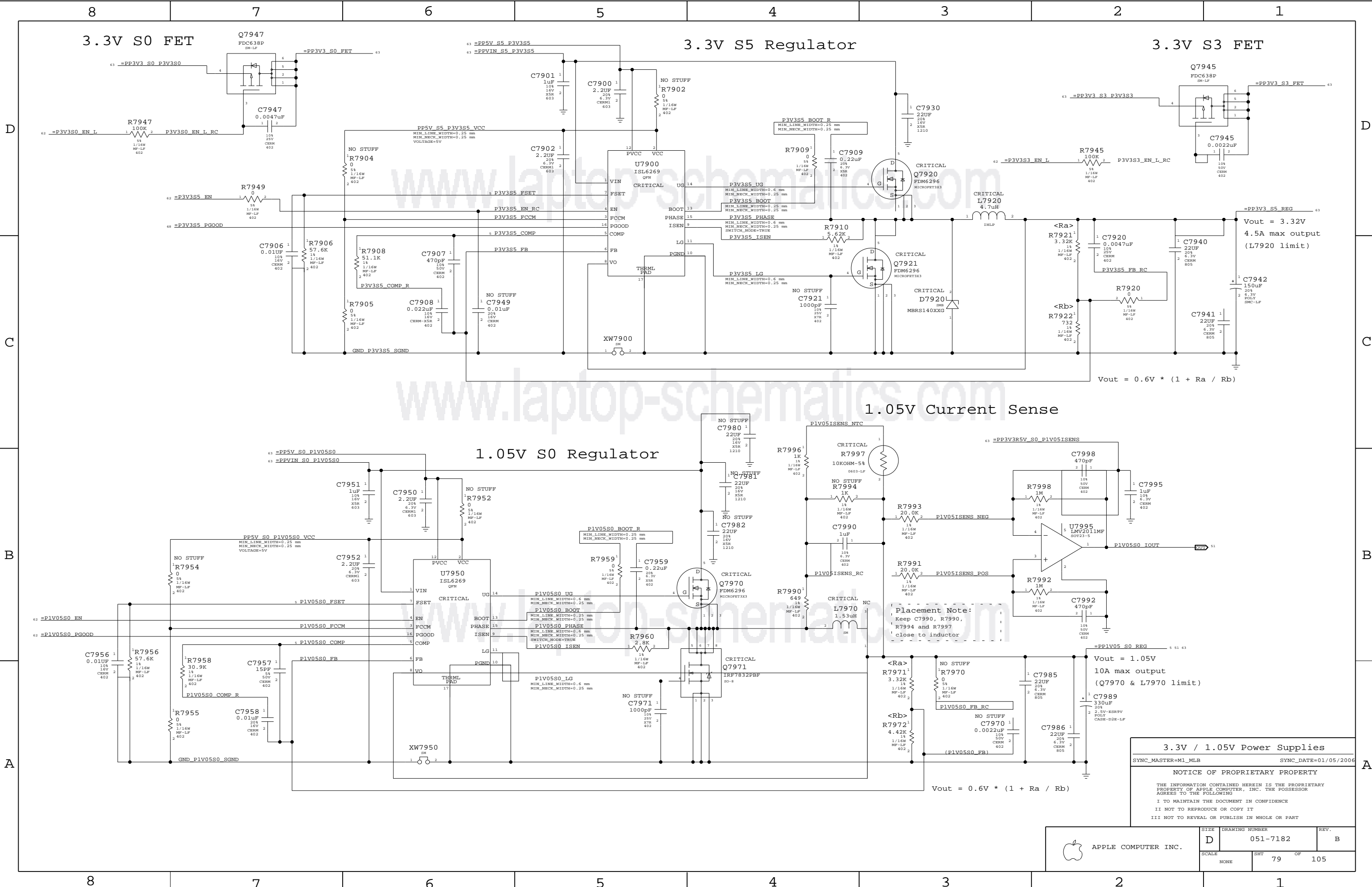
SCALE NONE SHT 76 OF 105



1.2V S0 FET







3.3V / 1.05V Power Supplies

SYNC_MASTER=M1_MLB SYNC_DATE=01/05/2006

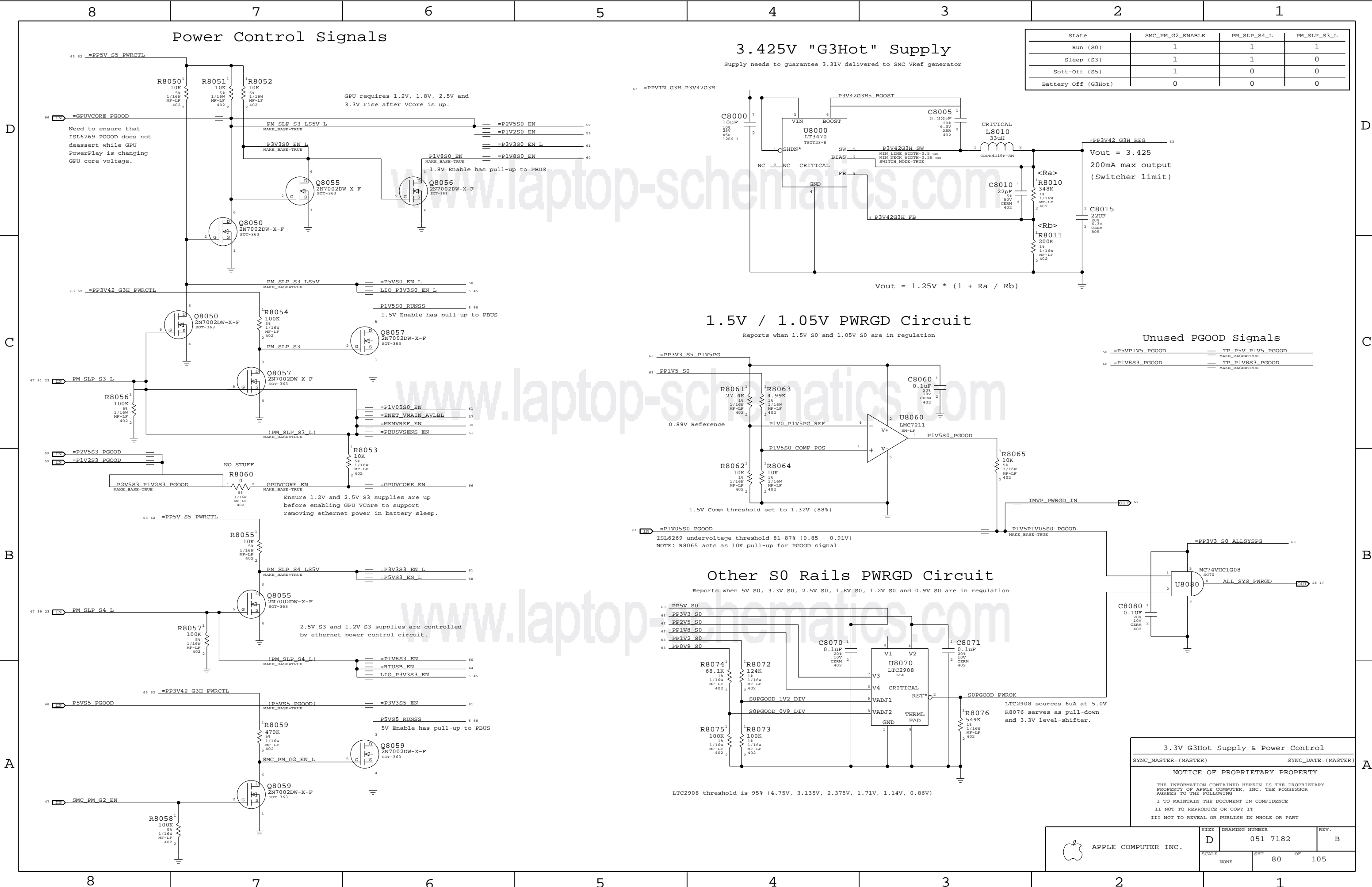
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Power Control Signals

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

Unused PGOOD Signals

Other S0 Rails PWRGD Circuit

Reports when 5V S0, 3.3V S0, 2.5V S0, 1.8V S0, 1.2V S0 and 0.9V S0 are in regulation

3.3V G3Hot Supply & Power Control

SYNC_MASTER=(MASTER)

SYNC_DATE=(MASTER)

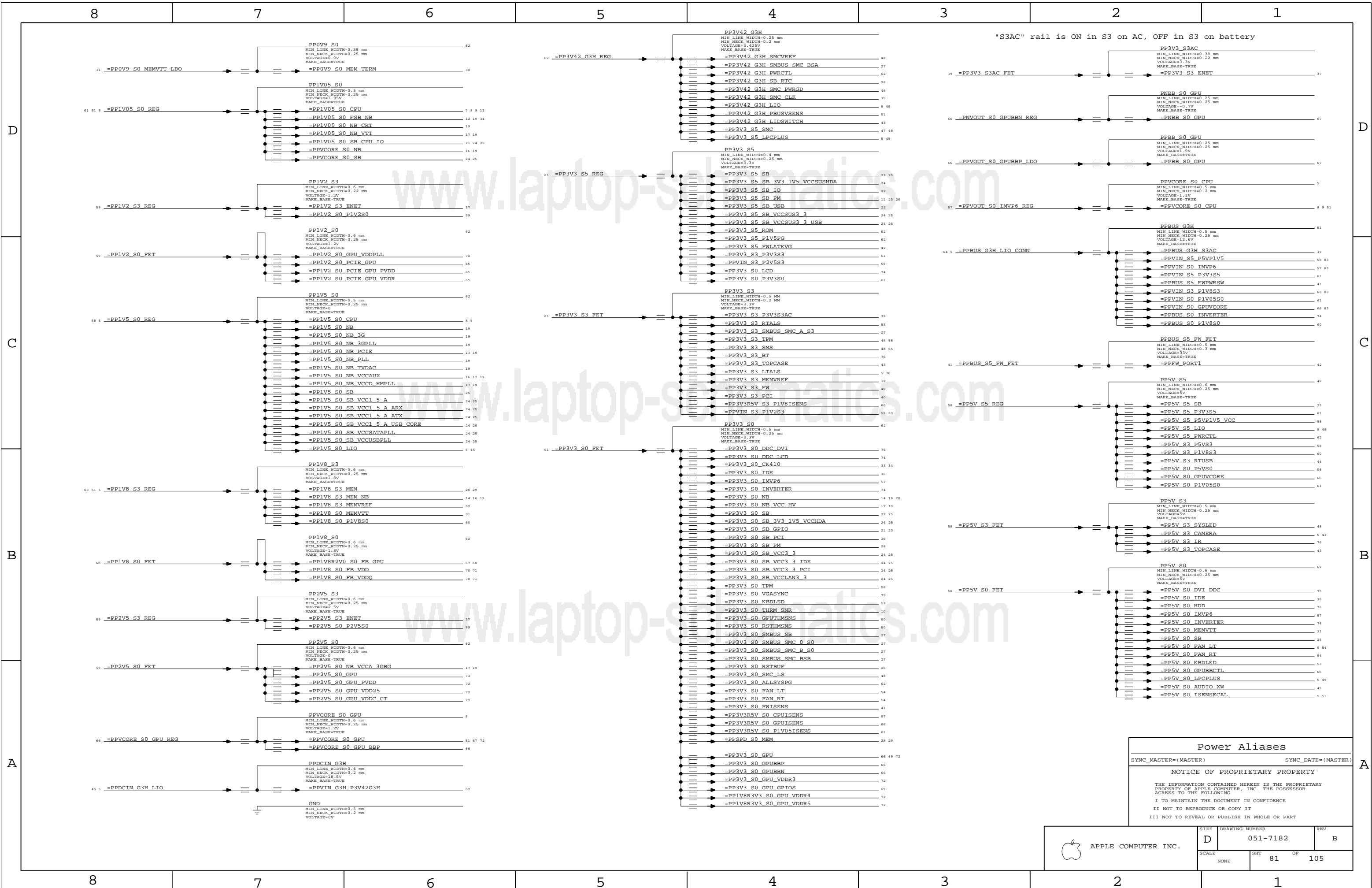
NOTICE OF PROPRIETARY PROPERTY

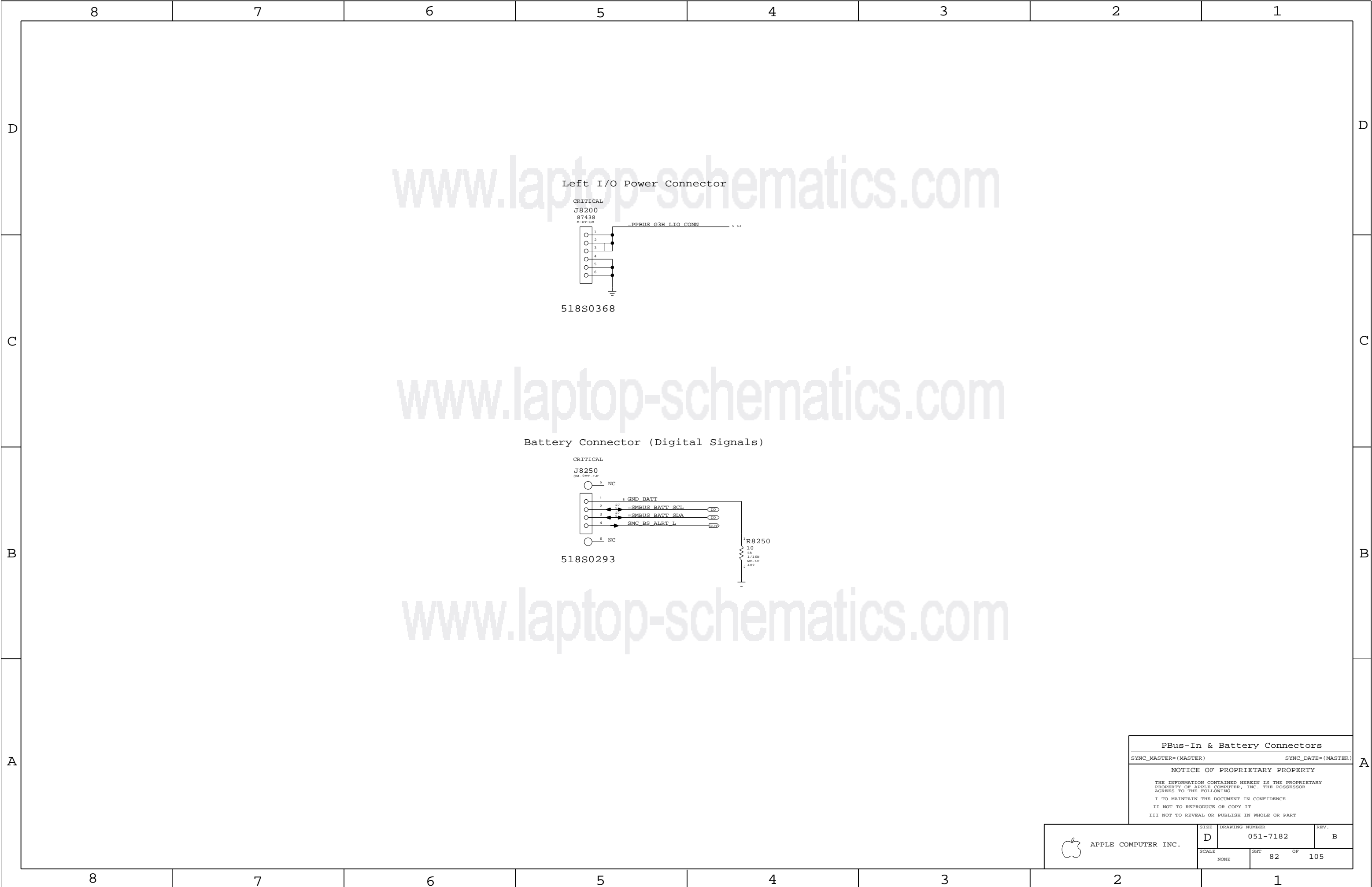
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PBus-In & Battery Connectors

SYNC_MASTER=(MASTER)SYNC_DATE=(MASTER)

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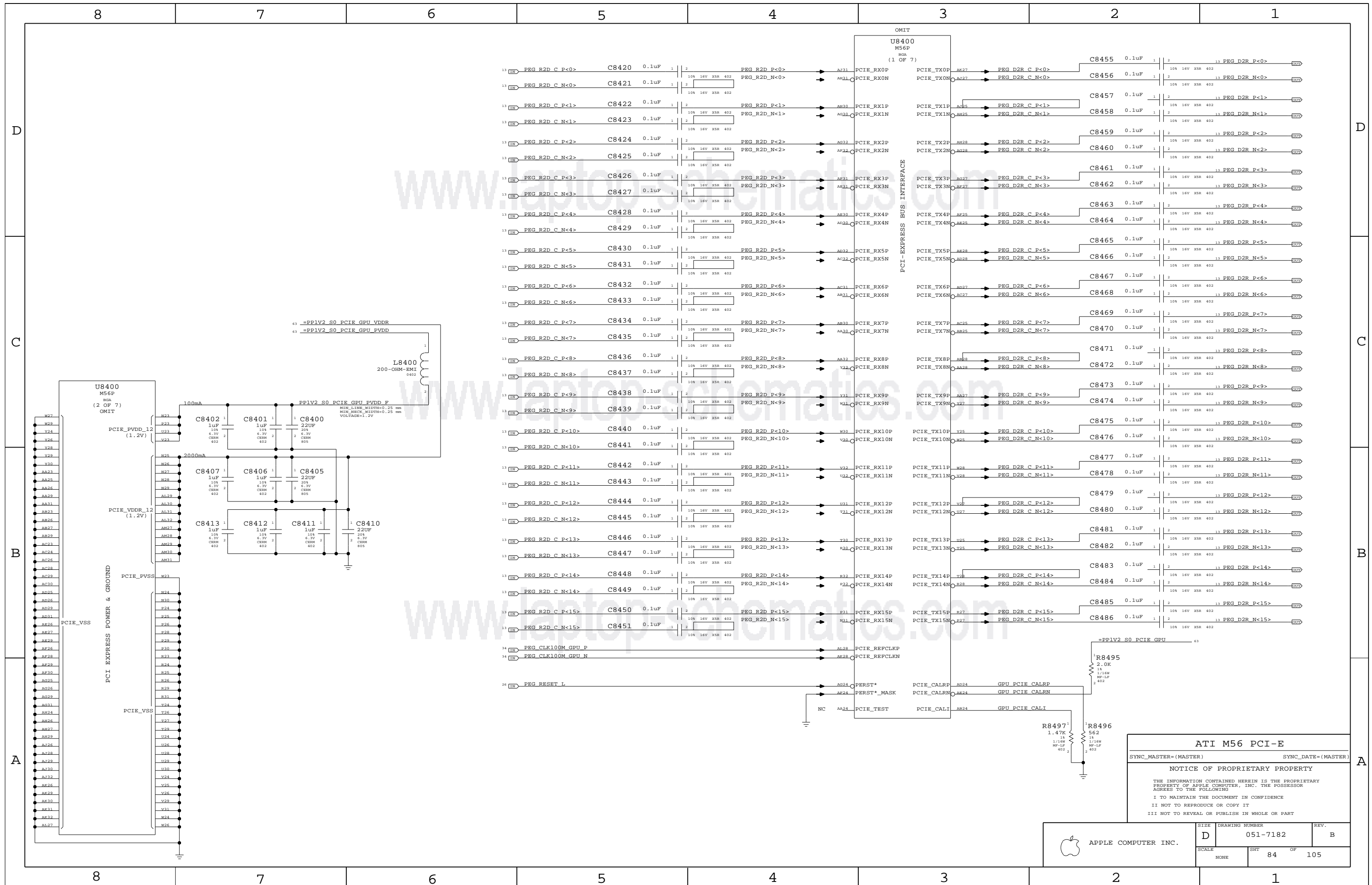
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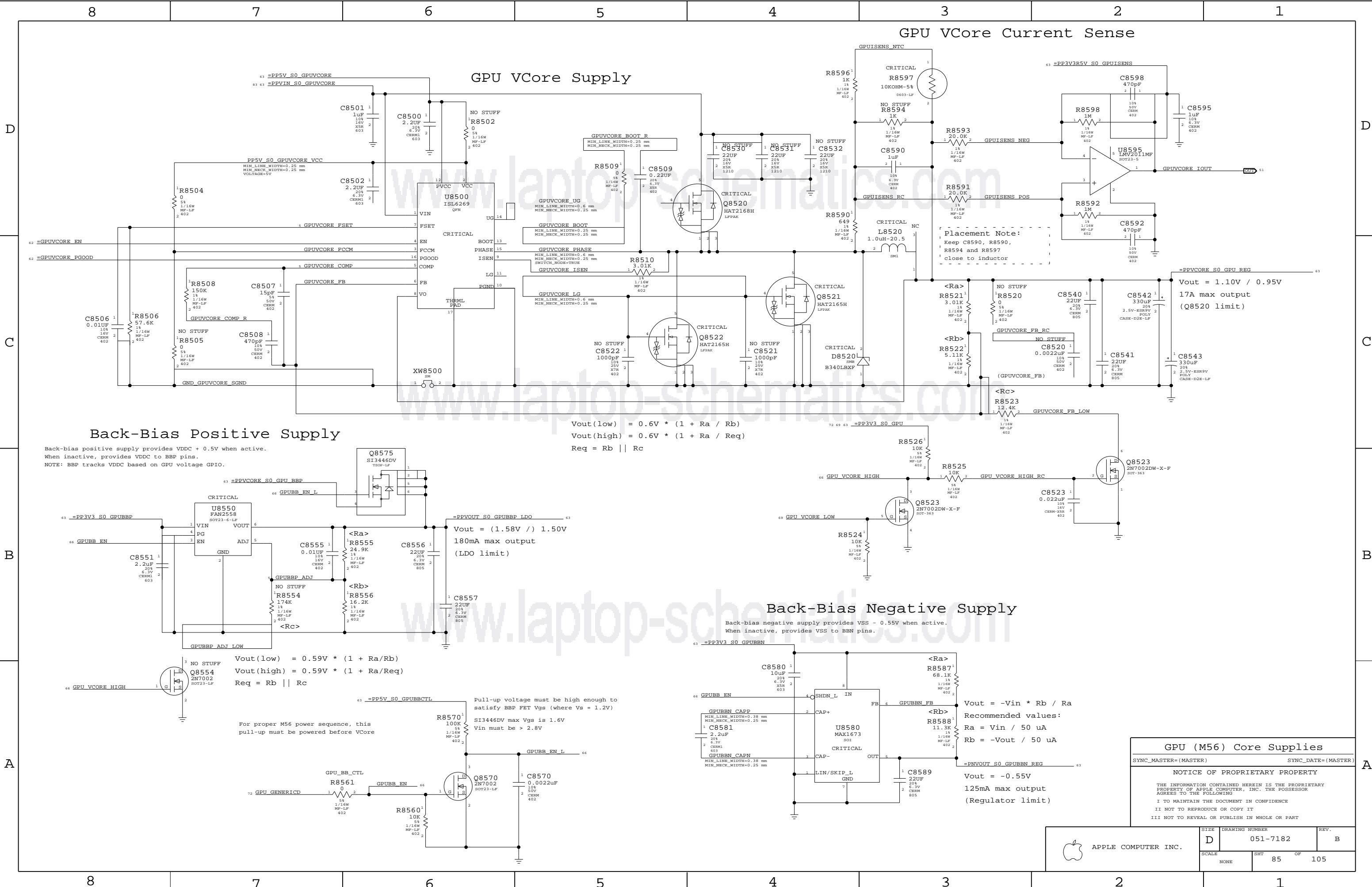
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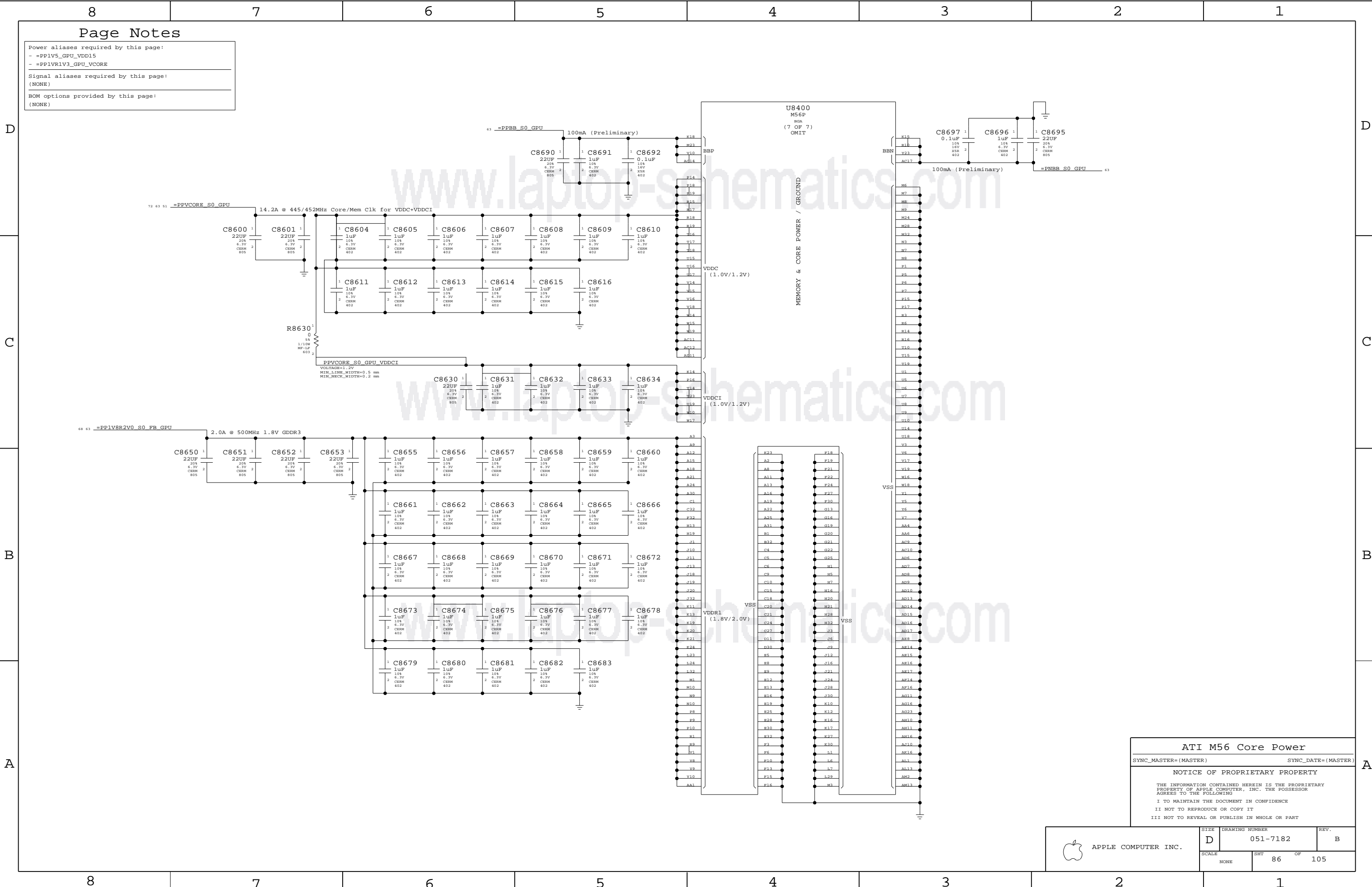
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7182	REV. B
	SCALE NONE	SHT 82	OF 105





GPU (M56) Core Supplies		
SYNC_MASTER=(MASTER)		SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7182	B
SCALE		SHT	OF
NONE		85	105



Page Notes

Power aliases required by this page:

- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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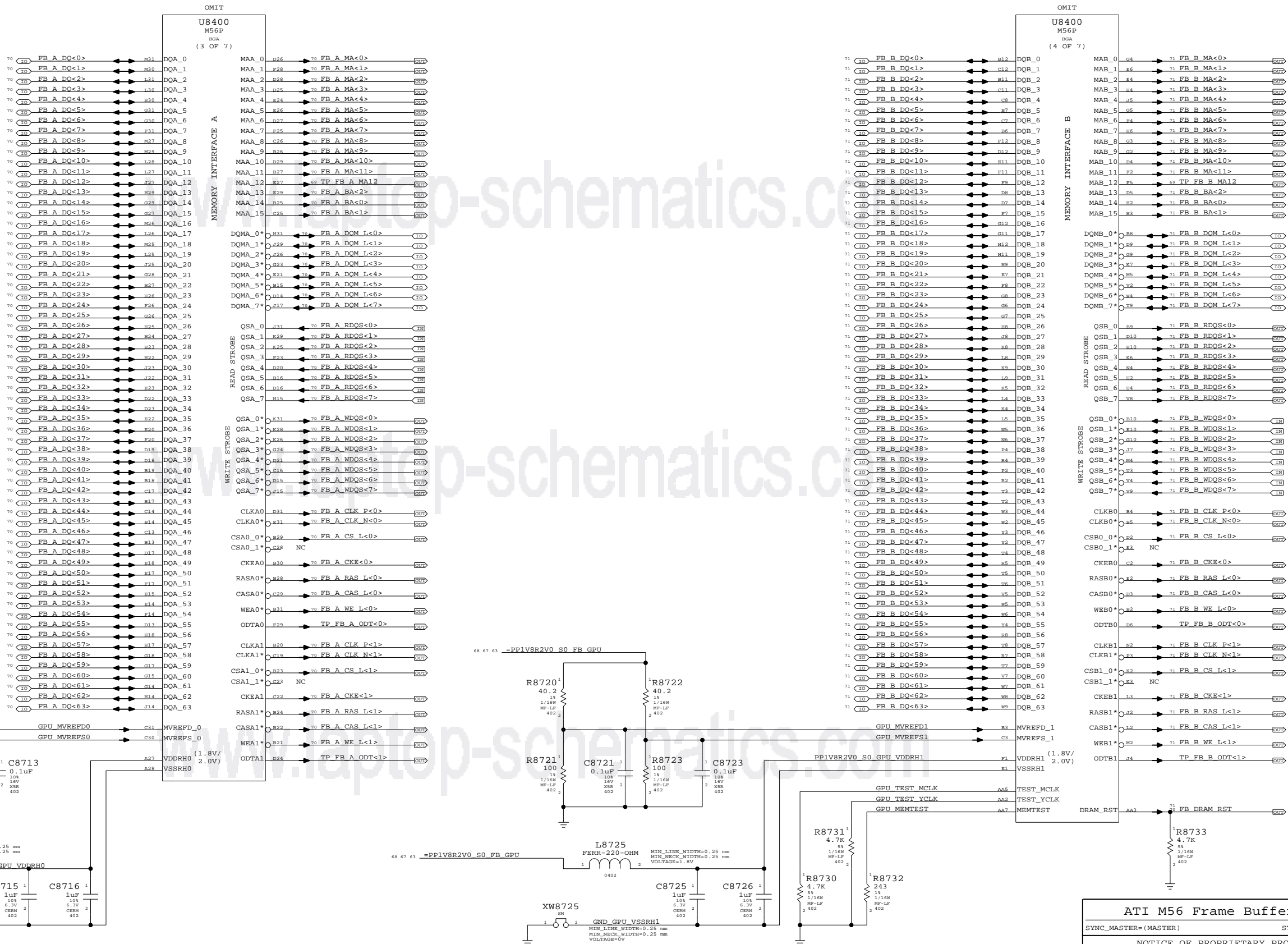
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7182	B
SCALE		SHT	OF
NONE		86	105

Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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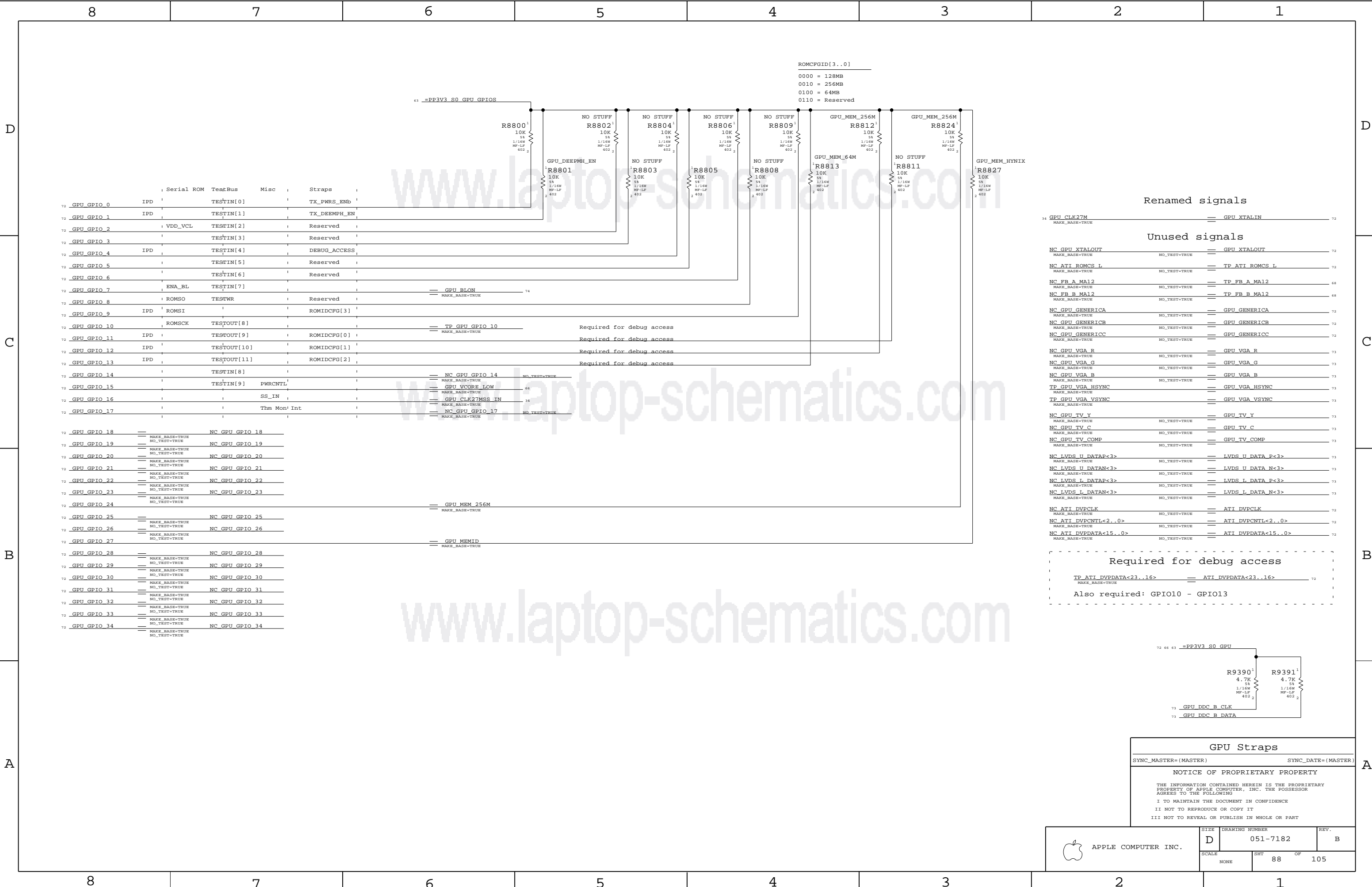
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SIZE D DRAWING NUMBER 051-7182 REV. B

SCALE NONE SHT 87 OF 105



Power aliases required by this page:

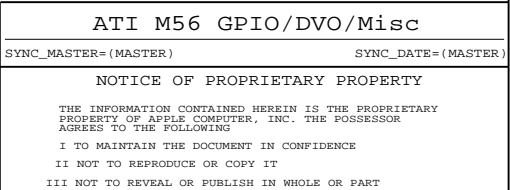
- PP3V3_GPU_GPIOS
- PP2V5_PVDD
- PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:

- I2C_GPU_TMD5_SDA - I2C data line for external TMD5 transmitters
- I2C_GPU_TMD5_SCL - I2C clock line for external TMD5 transmitters

BOM options provided by this page:

(NONE)



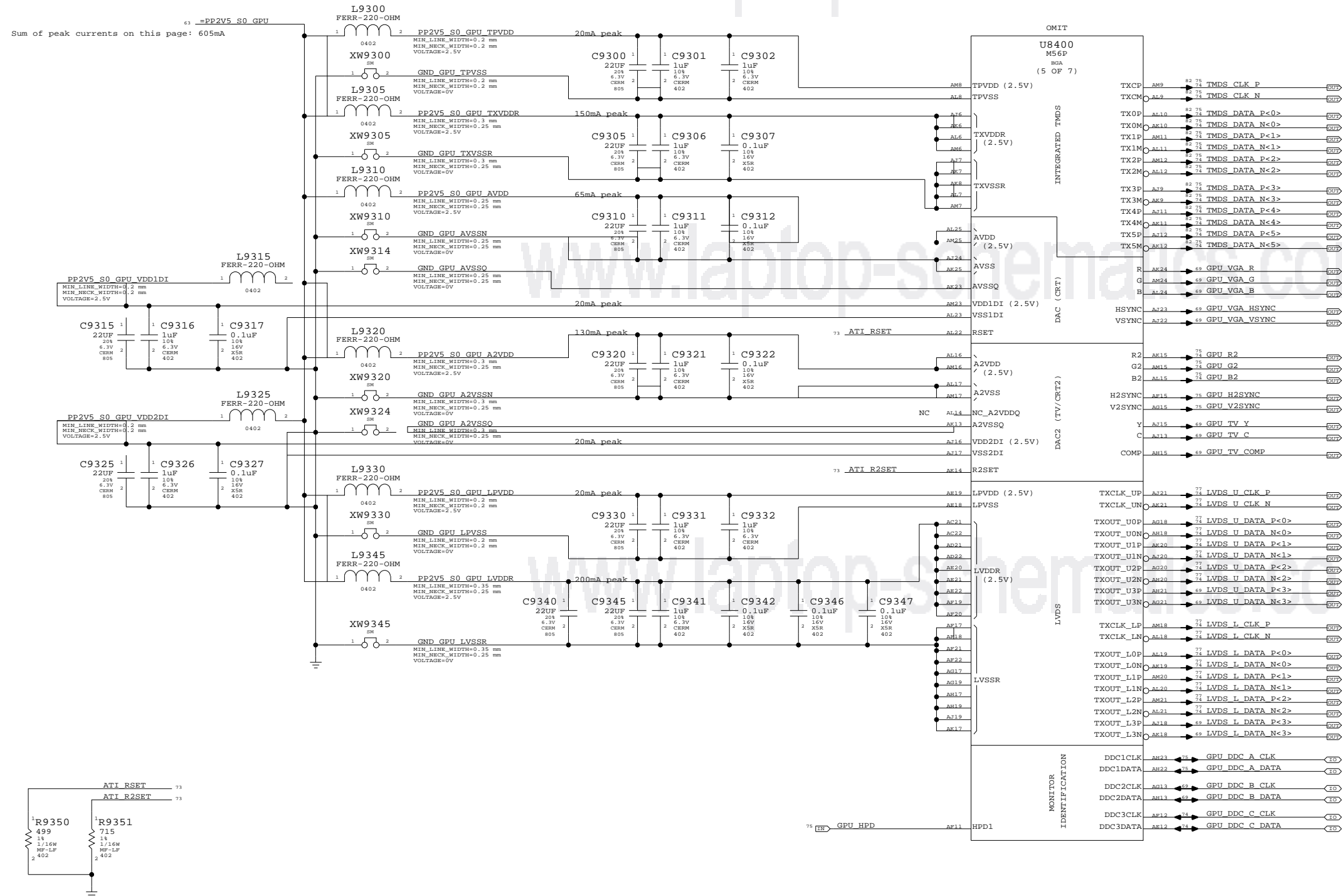
SIZE D	DRAWING NUMBER 051-7182	REV. B
SCALE NONE	SHT 91	OF 105

Power aliases required by this page:
<ul style="list-style-type: none">- =PP2V5_S0_GPU- =PPIV8R2V5_S0_GPU_LVDDR
Signal aliases required by this page:
(NONE)
BCM options provided by this page:
(NONE)

Power aliases required by this page:
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page
(NONE)

BOM options provided by this page:
(NONE)



Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

SYNC_MASTER= (MASTER)	SYNC_DATE= (MASTER)
------------------------	----------------------

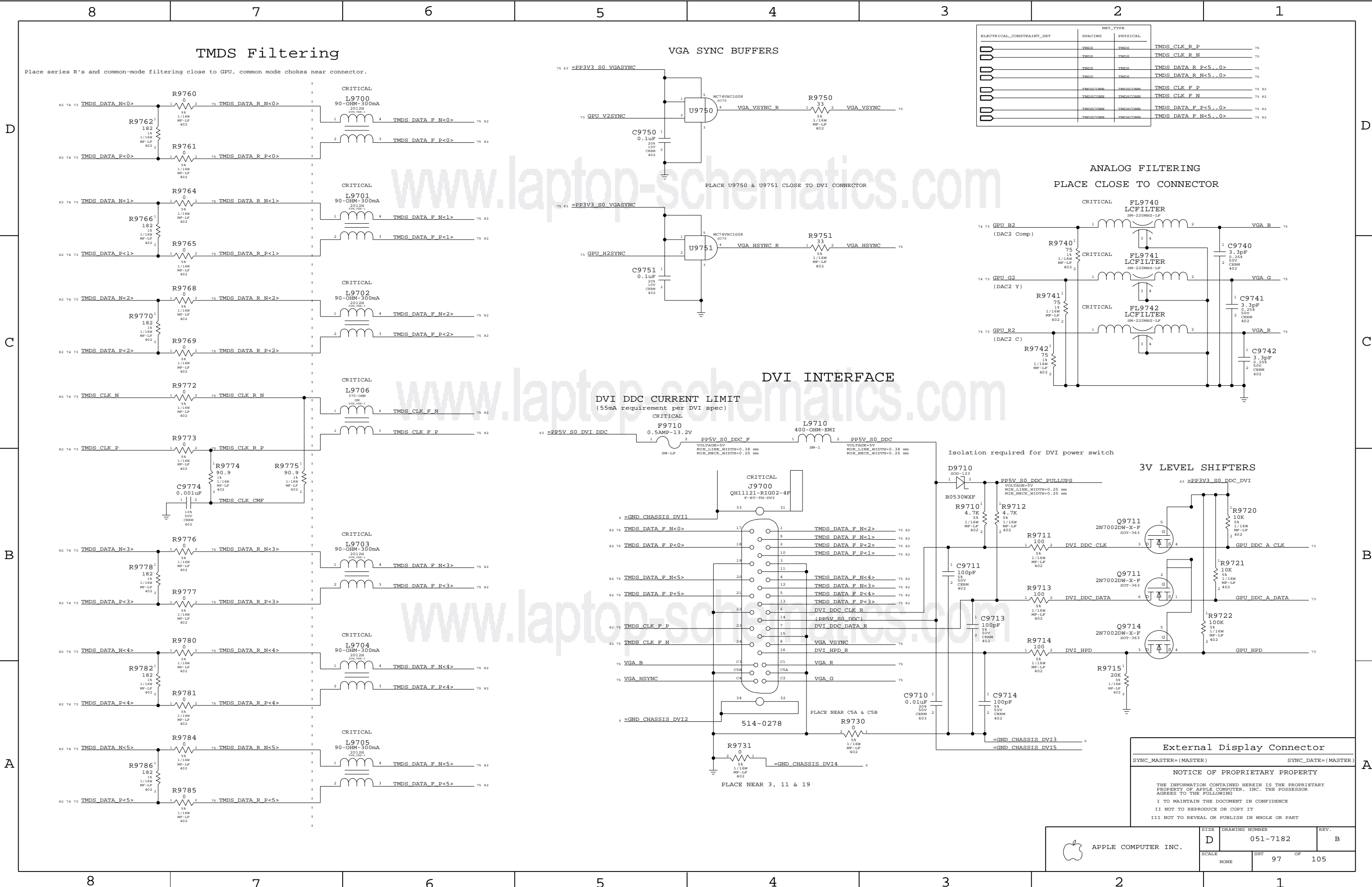
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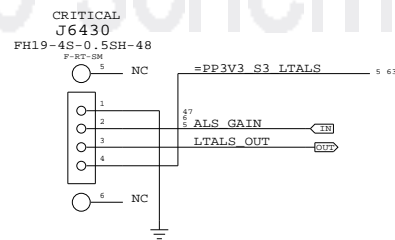
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APPLE COMPUTER INC.

SIZE D	DRAWING NUMBER 051-7182	REV. B
SCALE NONE	SHT 93	OF 105





63 =PP3V3_S3_BT
63 =PP5V_S3_IR
63 =PP5V_S0_HDD

CRITICAL
J4960
QT500206-L020
N-BT-2H

PLACEMENT_NOTE=Place FL4965 close to southbridge
CRITICAL
FL4965
90-ohm-100mA
2012H
10K

PLACEMENT_NOTE=Place C4965 close to J4960
CRITICAL
C4965
0.0047uF
25V
CERM
402

PLACEMENT_NOTE=Place C4966 next to C4965
CRITICAL
C4966
0.0047uF
25V
CERM
402


PLACEMENT_NOTE=Place C4960 close to southbridge
CRITICAL
FL4960
90-ohm-100mA
2012H
10K

PLACEMENT_NOTE=Place C4961 next to C4960
CRITICAL
C4961
0.0047uF
25V
CERM
402

PLACEMENT_NOTE=Place C4960 close to southbridge
CRITICAL
C4960
0.0047uF
25V
CERM
402

SATA_C_D2R_P
SATA_C_D2R_N
SATA_C_D2R_C_P
SATA_C_D2R_C_N
SATA_C_R2D_P
SATA_C_R2D_N
SATA_C_R2D_UF_P
SATA_C_R2D_UF_N
USB_BT_N
USB_BT_P
USB_IR_N
USB_IR_P
SYS_LED_ANODE

NOTE: _UF_ nets cross DDR2 signals and pick up significant noise. Common-mode chokes are to remove this noise from SATA signals.

 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7182	REV. B
	SCALE NONE	SHT OF 98 105	

	8	7	6	5	4	3	2	1					
	<div><div><div><div><div><div>Date</div><div>- Radar # - Description</div></div></div><div><div><div>DMS Release #03000 (RFA #394758)</div><div>2005/08/11 - 4214109 - Changed J4931 to proper 518S0342 part.</div><div>2005/08/12 - 4231030 - Changed pinout of J4960, added placement notes.</div><div>Changes from Proto Branch (DMS Release #04000):</div><div>2005/08/27 - 4230219 - Changed Y3301 to non-obsolete part.</div><div>2005/08/27 - 4235208 - Changed value of R7707 to fix 2.5V S3 supply.</div><div>2005/08/27 - 4235213 - Changed R8305, R8310, R8315 to slow down FET RCs.</div><div>2005/08/27 - 4235401 - Moved a few pins at LIO BTB connector.</div><div>2005/08/27 - 4227325 - Removed S0 option for camera, now S3-only.</div><div>2005/08/27 - 4227369 - Removed SMC options for display/backlight, now GPU-only.</div><div>2005/08/27 - 4225433 - Changed PBUS voltage sense circuit.</div><div>2005/08/28 - 4217535 - Added Left ALS FFC connector.</div><div>2005/08/28 - 4232563 - Changed analog video from Y/C/Comp to G2/R2/B2.</div><div>2005/08/28 - 4235203 - Changed BOM settings to stuff R2251.</div><div>2005/08/28 - 4217524 - Added LEFT ALS connector (J6430).</div><div>2005/08/28 - 4217535 - OMITs and tables to change 4-pin WTB connector parts.</div><div>2005/08/28 - 4221973 - Added pull-up for SB GPIO22 (REQ4#).</div><div>2005/08/28 - 4225369 - Changed ISL6269 PVCC aliases, added RC for 3.3V S5.</div><div>2005/08/28 - 4225433 - Changed PBUS Voltage Sense circuit.</div><div>2005/08/28 - 4227322 - Changed FW323 PCI_VIOS pin from 3.3V S0 to 3.3V S3.</div><div>2005/08/28 - 4235179 - OMIT and table to change 8-pin DC-In connector to 6-pin.</div><div>2005/08/28 - 4235179 - Changed PBUS net names to merge PBUS A & PBUS B.</div><div>2005/08/28 - 4237215 - Added FireWire iSense resistor, changed INA193 to INA194.</div><div>2005/08/28 - 4235217 - Added RC on Q3820 gate to slow down ODD FET turn-on.</div><div>2005/08/28 - 4225369 - OMITs and tables for staged LeMenu BOM approach.</div><div>2005/08/28 - 4227323 - Repinned Top-Case Flex connector.</div><div>DMS Checkin #04001</div><div>2005/08/29 - 4235179 - Changed J8200 to proper 6-pin part.</div><div>2005/08/29 - 4232826 - Changed MEM_ODT* from RPAKs to discrete Rs.</div><div>2005/08/29 - 4217524 - Changed R6430 from 4.5K to 3.5K.</div><div>2005/08/29 - 4237119 - Changed LIO 5V S3 to 5V S5.</div><div>2005/08/29 - 4225369 - Changed 3.3V S5 sequence to follow 5V S5 PGOOD.</div><div>2005/08/29 - 4227336 - Changed Y5920 to 197S0169.</div><div>2005/08/29 - 4227309 - Resolved sync issues with M38 (SB page 21).</div><div>2005/08/29 - 4227310 - Resolved sync issues with M38 (SB page 22).</div><div>2005/08/29 - 4227312 - Resolved sync issues with M38 (SB page 23).</div><div>2005/08/29 - 4227322 - Sync page 44 with M42 to fix FW power net S-states.</div><div>2005/08/29 - 4227332 - Resolved sync issues with M38 (SMC page 58).</div><div>2005/08/29 - 4227335 - Changed U5900 to resolve ROHS issue.</div><div>DMS Checkin #04002</div><div>2005/08/30 - 4225433 - Fixed voltage divider values in PBUS VSense circuit.</div><div>2005/08/30 - 4217535 - Removed BOM tables and OMITs for new 4-pin WTB connector.</div><div>2005/08/31 - 4214109 - Reversed pinout of J4931 to match updated PCB footprint.</div><div>2005/08/31 - 4227328 - Added ESD protection diode on right USB port.</div><div>2005/08/31 - 4223808 - Various power supply R/C updates, plus some R/C adds.</div><div>2005/08/31 - 4227315 - Changed BSA bus pull-ups from 2K to 10K.</div><div>2005/08/31 - 4237025 - Added R8824 and R8827 for GPU memory configuration straps.</div><div>DMS Checkin #04003</div><div>2005/08/31 - 4240157 - Corrected pinout at SATA/BT conn (J4960) to match flex.</div><div>2005/08/31 - 4240150 - Swapped PCIE Mini Card R2D/D2R connections at J5500.</div><div>2005/08/31 - 4232563 - Corrected net properties on R2/G2/B2 nets.</div><div>2005/08/31 - 4227306 - Swapped primary & alt part numbers for CPU VCore caps.</div><div>2005/08/31 - 4240300 - Changed C6455 to a smaller part for cost & MCO.</div><div>2005/08/31 - 4240486 - Power line width & neck reductions at PCB request.</div><div>2005/08/31 - 4240257 - Swapped some top & bottom EMC connections at DVI connector.</div><div>DMS Checkin #04004</div><div>2005/08/31 - 4227328 - Changed EMI caps from 50V to 16V to fid in ESD protection.</div><div>DMS Checkin #04005</div><div>2005/09/02 - 4241087 - Fixed pinout of USB D+/D- at camera connector to match FHB.</div><div>2005/09/02 - 4243269 - Inverted GPU VCore control, adjusted supply R values.</div><div>2005/09/02 - 4244019 - Moved GPU-related power alias from PP3V3_S0 to PP3V3_S0_GPU.</div><div>2005/09/02 - 4240486 - Adjusted line/neck widths, changed J4931 to 518S0371.</div><div>DMS Checkin #04006</div><div>2005/09/03 - 4232534 - Fixed documentation of battery address on I2C page.</div><div>2005/09/03 - 4244484 - Changed P1V5S0_RUNSS circuit to work properly in G3Hot.</div><div>2005/09/03 - 4244539 - Added GPUVCORE_PGOOD to 1.2V, 1.8V, & 2.5V S0 sequence.</div><div>2005/09/03 - 4227315 - Changed SMBus pull-ups to 4.7K.</div><div>2005/09/03 - 4232534 - Added notes for power supplies and connectors.</div><div>DMS Checkin #04007</div><div>2005/09/06 - 4240486 - Removed NO_TEST property from GPU HSYNC and VSYNC.</div><div>2005/09/06 - 4246683 - Removed NO_STUFF option from R8805 per ATI request.</div><div>2005/09/06 - 4232534 - Fixed label BOM tables to call out proper EEE #'s.</div><div>DMS Release #05000-07000 (Proto 2 releases)</div><div>2005/09/08 - 4247941 - Net property & name changes to support PCB/ICT requests.</div><div>2005/09/08 - 4248911 - Sync with M38 & M42.</div><div>2005/09/08 - 4214493 - Combined RTC coin cell diodes into dual-diode package.</div><div>2005/09/08 - 4229560 - First implementation of Physical Security Guidelines.</div><div>2005/09/16 - 4256660 - Updated FUNC_TEST property for merged PBUS.</div><div>2005/09/16 - 4229560 - Changed FW PCI REQ/GNT pair for Physical Security.</div><div>2005/09/19 - 4247941 - GND line/neck/voltage properties updated per PCB request.</div><div>2005/09/19 - 4235898 - Moved signal alias to improve schematic reuse.</div><div>2005/09/20 - 4214847 - Updated L1970 (old part no longer exists in library).</div><div>2005/09/21 - 4227306 - Changed CPU VCore caps to proper production part number.</div><div>2005/09/21 - 4234952 - Replaced FDG6324L parts with FDG6332C for cost & supply.</div><div>2005/09/26 - 4239505 - Updated J4200 (old part no longer exists in library).</div><div>2005/09/26 - 4274915 - Thermal sensor BOM updates from Proto 2 MLB branch.</div><div>2005/09/26 - 4274915 - U6301 part number updated to M1 development BootROM.</div></div></div></div></div></div>	<div><div><div><div><div><div>Date</div><div>- Radar # - Description</div></div></div><div><div><div>DMS Checkin #07001</div><div>2005/09/28 - 4221965 - Added 2.2uF caps on SO-DIMM VREF pins.</div><div>2005/09/28 - 4278828 - Adjusted P5VS5_PGOOD R's, added cap on PM_RSMRST_L.</div><div>2005/09/29 - 4232826 - Swapped Vtt RPAK functions to free up unnecessary part.</div><div>2005/09/30 - 4261313 - Added placeholder connector for IR FFC connector.</div><div>2005/09/30 - 4282162 - Changed GPU BBN supply to MAX1673.</div><div>2005/09/30 - 4248911 - Sync with M38 & M42.</div><div>2005/09/30 - 4282349 - Added CRITICAL flags to parts identified in scrub.</div><div>2005/09/30 - 4274915 - C1001 stuffing change from Proto 2 MLB branch.</div><div>DMS Checkin #07002</div><div>2005/10/04 - 4256409 - Changed fan CTL series R's to 2N7002 level-shifter.</div><div>2005/10/04 - 4261313 - Deleted placeholder connector, grew HDD connector for IR.</div><div>2005/10/04 - 4281394 - BOM option change to stuff right USB ESD protection part.</div><div>2005/10/06 - 4227330 - Added ESD protection on top-case USB port.</div><div>2005/10/07 - 4286888 - BOM restructuring per EVT build plan.</div><div>2005/10/07 - 4292633 - Changed IMVP6 10K NTC from 10% to 5% part.</div><div>2005/10/07 - 4248911 - Sync with M38 & M42.</div><div>DMS Checkin #07003</div><div>2005/10/08 - 4214493 - Simplified FireWire port power circuit for BOM consolidation.</div><div>2005/10/08 - 4293072 - Various BOM / connection changes at IMVP6 (CPU VCore).</div><div>2005/10/08 - 4286729 - Changed value of TPM Xtal caps.</div><div>2005/10/08 - 4290735 - Swapped trackpad & PCie Mini Card USB connections.</div><div>2005/10/09 - 4235898 - Part moves & rfdes changes to support sync with M9.</div><div>2005/10/09 - 4214494 - Changed GPU VCore supply enable to use 1.2V/2.5V S3 PGOODs.</div><div>2005/10/09 - 4272237 - Changed 2.5V S0 FET RC to 100K to slow down turn-on.</div><div>DMS Checkin #07004</div><div>2005/10/10 - 4232826 - Swapped Vtt RPAK functions to optimize layout.</div><div>2005/10/10 - 4247941 - Net property updates found via back-annotation.</div><div>DMS Checkin #07005</div><div>2005/10/10 - 4229560 - Removed Physical Security circuitry.</div><div>2005/10/10 - 4214493 - Cost reductions to GPU power supply circuitry.</div><div>2005/10/10 - 4214847 - Changed 0-ohm resistor to solder jumper.</div><div>2005/10/10 - 4248911 - Sync with M38 & M42.</div><div>2005/10/10 - 4295280 - Changed sleep LED connection per new SMC ERS.</div><div>DMS Checkin #07006</div><div>2005/10/11 - 4261313 - Updated SATA connector pinout to match latest flex.</div><div>2005/10/11 - 4227308 - Deleted unnecessary MCH TVDAC filtering.</div><div>2005/10/11 - 4229560 - Changed SB GNT3#/GNT4# back to test points.</div><div>2005/10/12 - 4248911 - Sync with M38 & M42.</div><div>2005/10/12 - 4298899 - Changed stuffing option to disable PLT_RST gating.</div><div>2005/10/12 - 4297684 - Split FW323 VSSA from VSS to reduce noise.</div><div>2005/10/12 - 4223808 - Power supply changes per vendor feedback.</div><div>2005/10/12 - 4227320 - Updated SB pin name for GPIO 5 (ODD_PWR_EN_L).</div><div>2005/10/12 - 4244539 - Retasked FET to control 3.3V S0 FET from GPU VCore PGOOD.</div><div>2005/10/12 - 4247941 - Added properties to resolve a PCB constraint issue.</div><div>2005/10/12 - 4214493 - Consolidated 0.22uF caps in design.</div><div>2005/10/12 - 4298905 - Changed ethernet VMMAIN_AVLBL connection.</div><div>2005/10/12 - 4298943 - Replaced last remaining non-RoHS compliant connector.</div><div>2005/10/12 - 4214494 - Implemented circuit to power down ethernet in S3 on battery.</div><div>DMS Checkin #07007</div><div>2005/10/13 - 4247941 - Swapped pins at trackpad ESD protection diode.</div><div>DMS Checkin #07008</div><div>2005/10/13 - 4247941 - Unswapped pins at trackpad ESD protection diode.</div><div>DMS Checkin #07009</div><div>2005/10/13 - 4247941 - Removed NO_TEST properties from CPU FSB strobe signals.</div><div>2005/10/13 - 4247941 - Spacing/Physical rule updates to match latest board database.</div><div>2005/10/14 - 4247941 - Restored NO_TEST properties, added EXPOSED_VIA properties.</div><div>2005/10/17 - 4292633 - Changed remaining 10K NTCs to new 5% part.</div><div>2005/10/17 - 4304248 - Updated GPU VCore / BBP voltages for B13/B24 support.</div><div>DMS Release #08000-11000 (EVT releases)</div><div>2005/10/20 - 4310267 - Synced 4 pages from mlb_evt branch back to trunk.</div><div>2005/10/21 - 4310267 - Synced 3 pages from mlb_evt branch back to trunk.</div><div>2005/10/21 - 4235898 - Synced 2 pages from m9/mlb.</div><div>2005/10/26 - 4310267 - Synced 4 pages from mlb_evt branch back to trunk.</div><div>2005/11/03 - 4310267 - Synced 6 pages from mlb_evt branch back to trunk.</div><div>2005/11/15 - 4310267 - Synced 5 pages from mlb_evt branch back to trunk.</div><div>2005/11/15 - 4298899 - Removed unused platform reset gate.</div><div>2005/11/15 - 4322537 - Updated thru-hole SO-DIMM connector part number.</div><div>2005/11/16 - 4345498 - Updated Ethernet & FireWire crystal part numbers.</div><div>2005/11/16 - 4235898 - Aliased connection to ALS_GAIN to support M9 request.</div><div>2005/11/16 - 4235898 - Changed Yukon power rail neck widths per M9 request.</div><div>2005/11/16 - 4227333 - Updated SMC net names per ERS v1.2.1.</div><div>2005/11/16 - 4345921 - FUNC_TEST updates per test team request.</div><div>2005/11/16 - 4346006 - Updated J5500 pinout to match updated LIO board pinout.</div><div>2005/11/16 - 4343202 - Changed USB overcurrent switch to TPS2051B, added OC* RC.</div><div>2005/11/16 - 4346184 - Inserted common-mode chokes on SATA R2D/D2R pairs.</div><div>DMS Checkin #11001</div><div>2005/11/16 - 4235898 - Sync with M38 & M42.</div><div>(11.1.0) 2005/11/16 - 4298899 - Fixed ethernet reset net name on page 26.</div><div>(11.2.0) 2005/11/16 - 4227333 - Fixed single-pin nets caused by SMC net name updates.</div><div>2005/11/18 - 4235898 - Changed R4210 package size per M9 request.</div><div>(11.3.0) 2005/11/18 - 4235898 - Changed C9710 GND connection per M9 request.</div><div>2005/11/19 - 4346184 - Fixed location of SATA R2D common-mode choke.</div><div>2005/11/19 - 4347717 - Changed SMS self-test pull-up to pull-down.</div><div>2005/11/19 - 4350840 - Simplified TMDS filtering to allow movement of filter.</div><div>2005/11/19 - 4229560 - Changed FW chip back to REQ/GNT3.</div><div>2005/11/19 - 4350849 - Added option to connect SB_GPIO30 to ENET_LOM_DIS_L.</div><div>2005/11/19 - 4340256 - Changed topcase flex trackpad power from 3.3V to 5V.</div><div>(11.4.0) 2005/11/19 - 4292165 - Refreshed schematic symbol for U3750 (library update).</div></div></div></div></div></div>	<div><div><div><div><div><div>Date</div><div>- Radar # - Description</div></div></div><div><div><div>DMS Checkin #11002</div><div>2005/11/21 - 4351196 - Added 1K pull-down on IDE_RESET_L.</div><div>(11.5.0) 2005/11/21 - 4343202 - Changed RC value and net name for USB OC.</div><div>2005/11/22 - 4350840 - Swapped TMDS termination components for placement.</div><div>(11.6.0) 2005/11/22 - 4352020 - Changed 2.5V S3 supply inductor & compensation values.</div><div>(11.7.0) 2005/11/28 - 4347845 - Added pull-down resistors on LVDS interface.</div><div>2005/11/30 - 4227340 - Removed CPU VCore current sense input RC.</div><div>2005/11/30 - 4331670 - Added CRITICAL flags to some more parts.</div><div>2005/11/30 - 4343864 - Added EMI/ESD parts at camera connector.</div><div>2005/11/30 - 4351181 - Changed ITP connector BOM option.</div><div>2005/11/30 - 4351196 - Changed IDE_RESET_L pull-down from 1K to 15K.</div><div>(11.8.0) 2005/11/30 - 4358831 - Added pull-downs on two SB-to-SMC signals.</div><div>2005/12/01 - 4362404 - Changed TMDS diff term from 100-ohm to 180-ohm.</div><div>2005/12/01 - 4352020 - Changed 2.5V supply inductor to RoHS-compliant part.</div><div>2005/12/01 - 4227340 - Changed supply for 1.8V S3 current sense amp.</div><div>2005/12/01 - 4362566 - Restructured BOM for thick/thin PCB versions.</div><div>2005/12/01 - 4347845 - RPAK pinswaps to LVDS pull-downs for PCB layout.</div><div>DMS Checkin #11003</div><div>2005/12/02 - 4256256 - Added BOMOPTION to R8801 to allow per-project control.</div><div>2005/12/02 - 4363848 - Removed M56 GPU die rev B13 support from BOM.</div><div>2005/12/02 - 4363870 - Removed M1a support from BOM.</div><div>2005/12/02 - 4217524 - Updated part number for J6430.</div><div>(11.10.0) DMS Release #12000-13000 (DVT releases)</div><div>2005/12/07 - 4375840 - Synced 4 pages from mlb_dvt branch back to trunk.</div><div>2005/12/12 - 4235898 - Changes to LVDS net names to support mux option.</div><div>2005/12/12 - 4362451 - Added MAKE_BASE=TRUE to SMC 32KHz SUSCLK net.</div><div>2006/01/03 - 4375840 - Synced 1 page from mlb_dvt branch back to trunk.</div><div>2006/01/03 - 4290282 - Removed BOM table, changed L9455 to 155S0002.</div><div>2006/01/03 - 4347845 - Changed LVDS pull-downs from 10K to 8.2K.</div><div>2006/01/03 - 4391436 - Swapped N/P signal names on one portion of SATA_R2D.</div><div>2006/01/03 - 4362451 - Changed SCH/PCB/BOM part descriptions for Rev A.</div><div>(13.1.0) 2006/01/03 - 4362451 - Removed power jumpers and 0-ohm resistor.</div><div>2006/01/05 - 4362566 - Removed 920- number for thin PCB option.</div><div>2006/01/05 - 4394079 - Added BOMOPTION to SYS_ONEWIRE pull-up.</div><div>2006/01/05 - 4362451 - Removed power jumpers and 0-ohm resistor.</div><div>2006/01/05 - 4362451 - Restructured BOM tables to eliminate LeMenu.</div><div>2006/01/06 - 4402184 - Changed R7540 value for IMVP6 load-line improvement.</div><div>2006/01/06 - 4362451 - Added System Block Diagram, updated Power Diagram.</div><div>2006/01/06 - 4362451 - Changed BOM options for production SMC, BootROM.</div><div>(13.2.0) DMS Release #A000 (PVT Release)</div><div>2006/01/21 - 4412882 - Changed R7623 from 1.33K to 931 ohms.</div><div>(A.1.0) 2006/01/21 - 4414757 - Changed 138S0552 to 138S0580 & 138S0553 to 138S0581.</div><div>2006/01/26 - 4420815 - Changed 2x 128S0077 to 128S0068.</div><div>(B.0.0) DMS Release #B000 (PVT BOM Update)</div><div>2006/02/09 - 4440116 - Pulled new schematic part number (051-7099).</div><div>2006/02/09 - 4440116 - Restructured BOM for 3 CPU configs.</div><div>2006/02/09 - 4440116 - Updated BootROM / SMC part numbers.</div><div>(A.0.0) DMS Release #A000 (Ramp Config Update)</div><div>2006/02/13 - 4420815 - Changed remaining 128S0077 to 128S0086.</div><div>2006/02/13 - 4420815 - Added 128S0077 as alternate for 128S0086.</div><div>2006/02/13 - 4437189 - Changed R7757 to 1Mohm & R7770 to 100K.</div><div>(A.1.0) 2006/02/13 - 4431947 - Removed NO_STUFF option from C3309.</div><div>DMS Release #B000 (PVT BOM Roll-In)</div><div>2006/02/17 - 4449123 - Changed C7537: 4.7nF -> 47pF, R7537: 3.57K -> 4.42K.</div><div>(C.0.0) DMS Release #C000 (Ramp BOM Update)</div><div>2006/03/03 - 4457745 - Added 128S0094 & 128S0095 as alternates for 128S0060.</div><div>2006/03/03 - 4457801 - Added 128S0081 as alternate for 128S0061.</div><div>2006/03/03 - 4466770 - Changed R7920 from 5% to 1% to reduce variation.</div><div>2006/03/03 - 4399085 - Changed C7532 from 10nF to 15nF to slow CPU slew rate.</div><div>2006/03/03 - 4424175 - Changed 8 VRAM strap resistors to enable ICT testing.</div><div>(D.0.0) DMS Release #D000 (BOM Update)</div><div>2006/03/31 - 4485021 - Changed R7542 from 9.31K to 11.5K for CPU VCore OCP.</div><div>2006/03/31 - 4498859 - Updated BOM table for screened ISL6262.</div><div>(E.0.0) DMS Release #E000 (BOM Update)</div><div>2006/03/31 - 4436716 - Added BOM table for ATI rev B26.</div><div>2006/04/05 - 4502903 - Reset BOM part numbers & EEE codes for B26 change.</div><div>(F.0.0) DMS Release #F000 (New EEE/BOM Release)</div><div>(G.0.0) DMS Release #G000 (RFA Re-release)</div><div>2006/04/17 - 4517184 - Updated BOM part #s and EEE codes for config changes.</div><div>(H.0.0) DMS Release #H000 (BOM Update)</div></div></div></div></div></div>	<div><div><div><div><div><div>A</div><div>SYNC_MASTER=N/A</div><div>SYNC_DATE=N/A</div></div></div><div><div><div>NOTICE OF PROPRIETARY PROPERTY</div><div>THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</div><div>I TO MAINTAIN THE DOCUMENT IN CONFIDENCE</div><div>II NOT TO REPRODUCE OR COPY IT</div><div>III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</div></div></div></div></div><div><div><div><div><div><div></div><div>APPLE COMPUTER INC.</div></div></div></div></div></div></div>	<div><div><div><div><div>SIZE</div><div>D</div></div><div><div>DRAWING NUMBER</div><div>051-7182</div></div><div><div>REV.</div><div>B</div></div></div><div><div><div>SCALE</div><div>NONE</div></div><div><div>SHT</div><div>100</div></div><div><div>OF</div><div>105</div></div></div></div></div>	8	7	6	5	4	3	2	1

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CPU AREA

67 = PPVIN S0 IIMP6

63 58 = PPVIN S5 P5VP1V5

62 = PPVIN S5 P5VP1V5

1 OMIT CRWK01 330P 200 2 POLY CATED2E-SM

1 OMIT CRWK02 330P 200 2 POLY CATED2E-SM

1 OMIT CRWK03 330P 200 2 POLY CATED2E-SM

1 OMIT CRWK04 330P 200 2 POLY CATED2E-SM

1 OMIT CRWK05 10P 200 2 CERM 805

1 OMIT CRWK06 10P 200 2 CERM 805

1 OMIT CRWK07 10P 200 2 CERM 805

1 OMIT CRWK08 10P 200 2 CERM 805

(CPU VCORE, 5V/1.5V)

RefDes	Connection to unstuffed comp. pads
CRWK09	C7982.2 to C7980.1 (poscap + end)
CRWK10	C7982.1 to C7982.2
CRWK11	C8530.2 to C8532.1 (poscap + end)
CRWK12	C8530.1 to C8530.2

```

63 =PPVIN_S0_P1V05S0
+
1 OMIT
CRWK09
33UF
20V
2 POLY
CASED2E-SM
1 OMIT
CRWK10
1UF
20V
2 CERM
805
+
64 =PPVIN_S0_G5V0CORE
+
1 OMIT
CRWK11
33UF
20V
2 POLY
CASED2E-SM
1 OMIT
CRWK12
1UF
20V
2 CERM
805

```

(1.05V, GPU VCORE)

RefDes	Connection to unstuffed comp. pads
CRWK13	C7830.2 to C77831.1 (poscap + end)
CRWK14	C7833.2 to C7833.1
CRWK15	C7833.2 to C7833.1

60 =PPVIN S3 P1V8S3

1 OMIT

CRWK13

33UF

20V

POLY

CASRO2E-SM

2

1 OMIT

CRWK14

1UF

20V

CERM

805

2

1 OMIT

CRWK15

1UF

20V

CERM

805

2

0

(1.8V)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
128S0092	4	CAP,TANT,POLY,33UF,16V,,0708M,D2E CASE	CRWK01,CRWK02,CRWK03,CRWK04	CRITICAL	
128S0092	3	CAP,TANT,POLY,33UF,16V,,0708M,D2E CASE	CRWK09,CRWK15,CRWK13	CRITICAL	
138S0319	4	CAP,CER,3.0UF,10V,16V,X7R,0805,SMD	CRWK05,CRWK06,CRWK07,CRWK08	CRITICAL	
138S0319	4	CAP,CER,3.0UF,10V,16V,X7R,0805,SMD	CRWK10,CRWK12,CRWK14,CRWK15	CRITICAL	

ANGLED CAPS FOR C4 NOISE

SYNC_MASTER=N/A SYNC_DATE=N/A


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II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7182	B
	SCALE	SHT	OF
	NONE	105	105