

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHM, MLB, M1
04/17/2006

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
H		435494	PRODUCTION RELEASED	04/18/05	

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4	BOM Configuration	N/A	N/A
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





















Schematic / PCB #'s

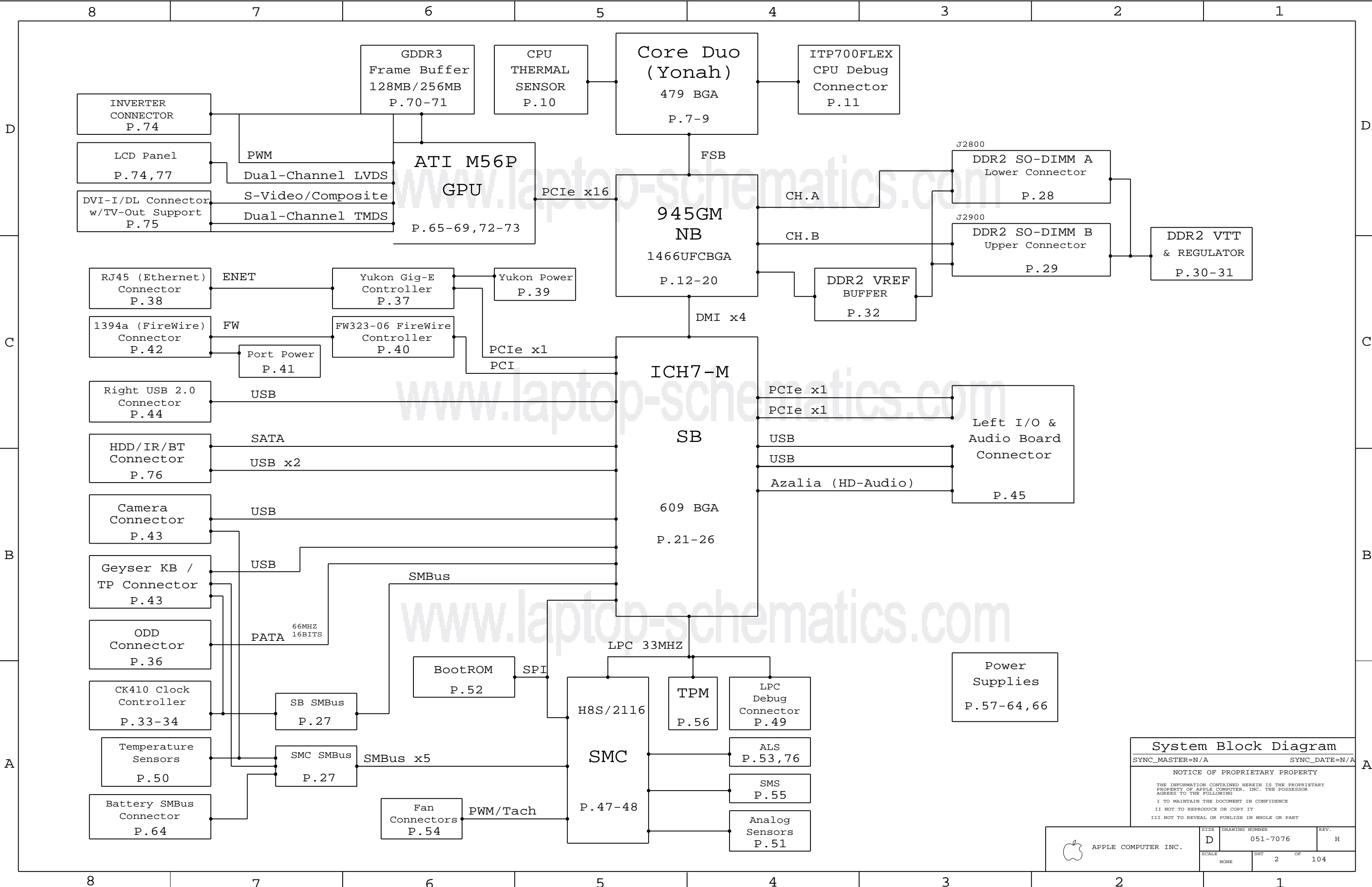
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7076	1	SCHEM,MLB,M1	SCH	CRITICAL	
820-1993	1	PCBF,MLB,M1	PCB	CRITICAL	

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DRAWING
TITLE=M1_MLB
ABBREV=DRAWING
LAST_MODIFIED=Mon Apr 17 16:23:07 2006

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X.XX : _____		<table><tr><td>DRAFTER</td><td></td><td>DESIGN CK</td><td></td></tr><tr><td>ENG APPD</td><td></td><td>MFG APPD</td><td></td></tr><tr><td>QA APPD</td><td></td><td>DESIGNER</td><td></td></tr><tr><td>RELEASE</td><td></td><td colspan="2">SCALE NONE</td></tr></table>				DRAFTER		DESIGN CK		ENG APPD		MFG APPD		QA APPD		DESIGNER		RELEASE		SCALE NONE		NOTICE OF PROPRIETARY PROPERTY	
DRAFTER						DESIGN CK																	
ENG APPD						MFG APPD																	
QA APPD		DESIGNER																					
RELEASE		SCALE NONE																					
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		TITLE																					
<div></div>		SCHEM, MLB, M1																					
THIRD ANGLE PROJECTION		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE D	DRAWING NUMBER 051-7076																		
					REV. H																		
					SHT 1 OF 104																		



System Block Diagram

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SYNC_DATE=N/A

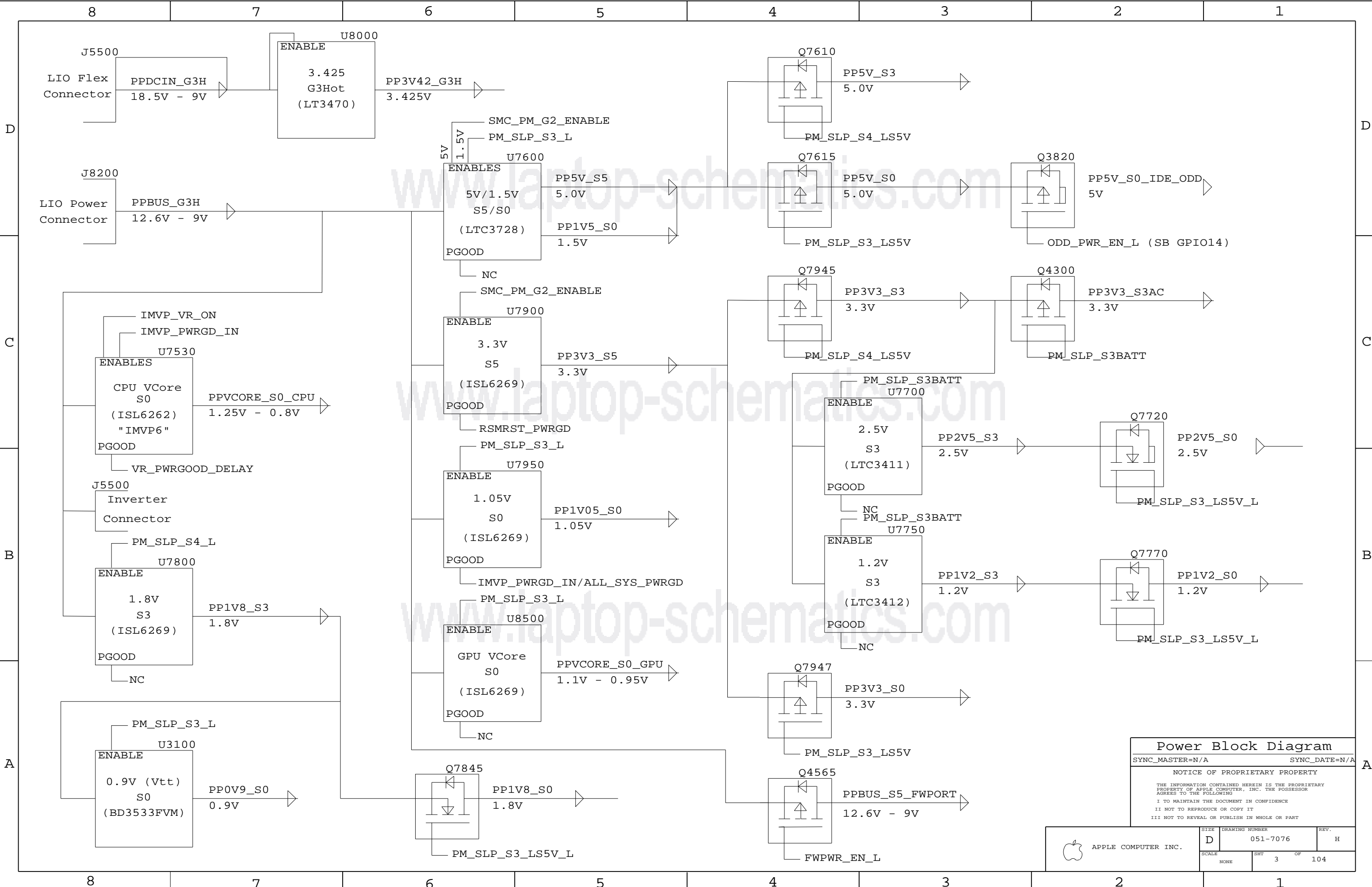
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Power Block Diagram

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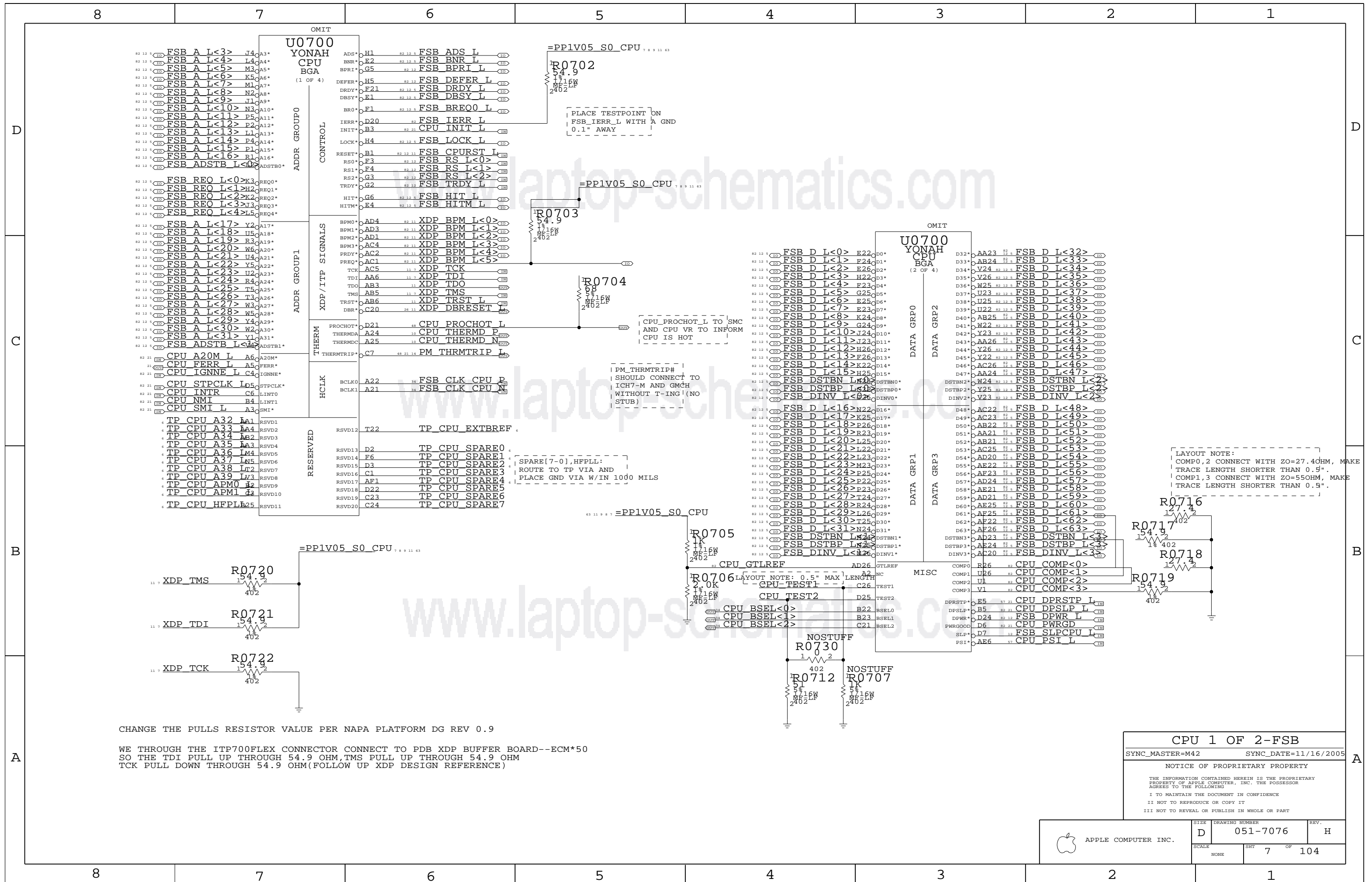
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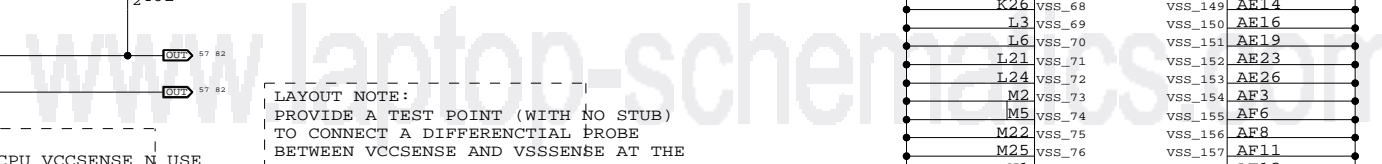
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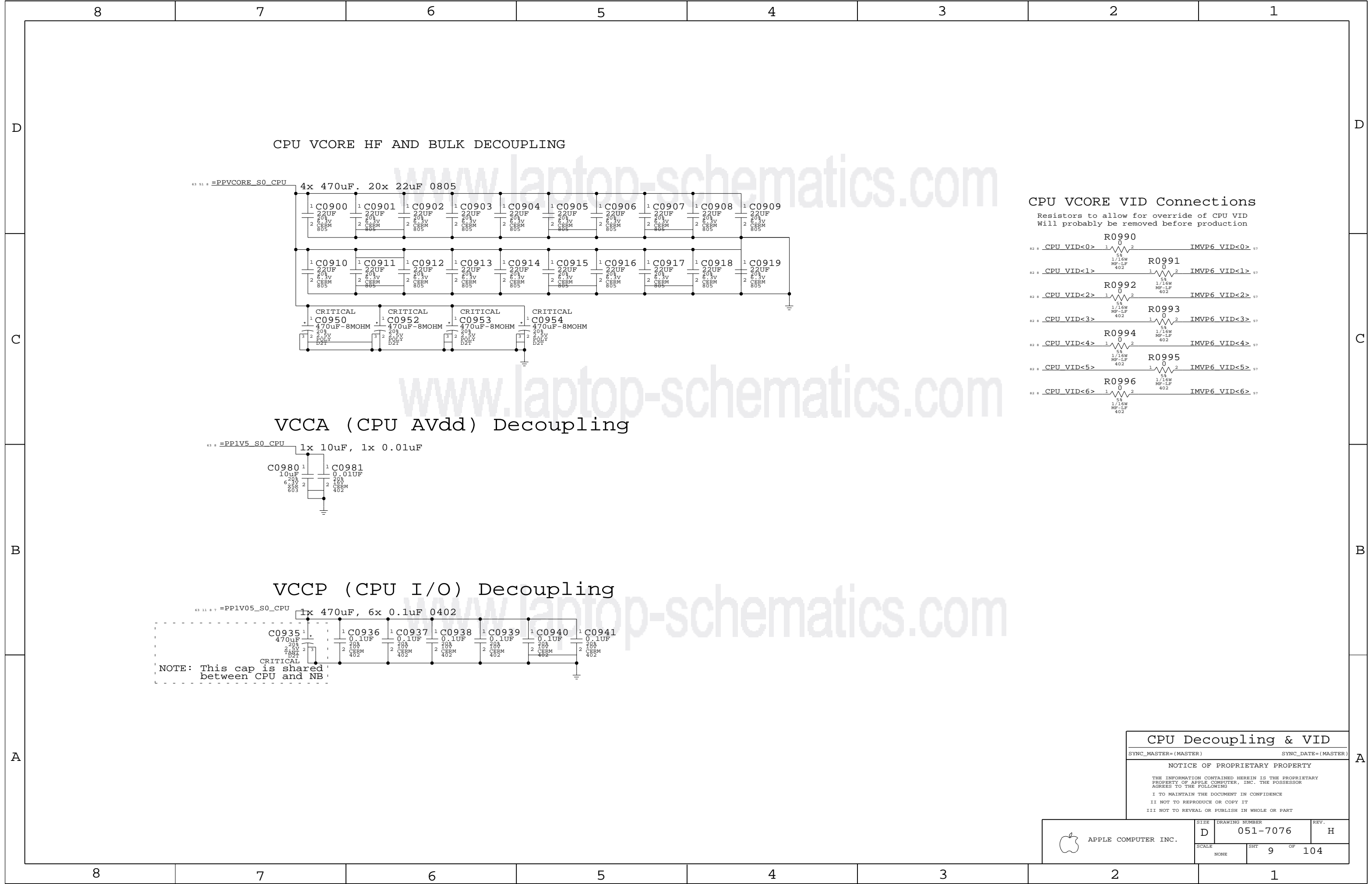
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	D	051-7076	H
SCALE		SHT	OF
NONE		3	104

8		7		6		5		4		3		2		1		
"Better" BOM																
BOM NUMBER		BOM NAME				BOM OPTIONS										
630-7700		PCBA, 2.0GHZ, 128VRAM, B26_M1-F_MBP15				EEE_VZU, M1_COMMON, CPU_2_0GHZ, VRAM_SAM128										
"Best" BOM																
BOM NUMBER		BOM NAME				BOM OPTIONS										
630-7675		PCBA, 2.16GHZ, 256VRAM, B26_M1-F_MBP15				EEE_VVQ, M1_COMMON, CPU_2_16GHZ, VRAM_SAM256										
BOMOPTION Groups																
BOM GROUP		BOM OPTIONS														
M1_COMMON		ALTERNATE, COMMON, M1_COMMON1, M1_COMMON2, M1_COMMON3														
M1_COMMON1		ATI_REV_B26, BOOTROM_DEVEL, ENET_LOM_DISABLE, ENETPWR_S3AC, GPU_BB_CTL, GPUTHM_A_GPU														
M1_COMMON2		HSTHMSNS_HAS, ITP, INVERTER_BUF, KBDLED_HAS, LPCPLUS, LVDS_PD, MEMVREF_S3														
M1_COMMON3		MEMVTT_EN_PU, RTUSB_ESD, SMC_PRGRM, USB_C_OC_PU, USB_D_OC_PU, USB_E_OC_PU														
VRAM_HY128		GPU_MEM_HYNIX, VRAM_128_HYNIX														
VRAM_SAM128		VRAM_128_SAMSUNG														
VRAM_HY256		GPU_MEM_256M, GPU_MEM_HYNIX, VRAM_256_HYNIX														
VRAM_SAM256		GPU_MEM_256M, VRAM_256_SAMSUNG														
Bar Code Label / EEE #'s																
PART NUMBER		QTY	DESCRIPTION			REFERENCE DES		CRITICAL		BOM OPTION						
826-4393		1	LBL, P/N LABEL, PCB, 28MM X 6 MM			[EEE:VZU]		CRITICAL		EEE_VZU		M1, 2.0GHZ, 128VRAM				
826-4393		1	LBL, P/N LABEL, PCB, 28MM X 6 MM			[EEE:VVQ]		CRITICAL		EEE_VVQ		M1, 2.16GHZ, 256VRAM				
Module Parts																
PART NUMBER		QTY	DESCRIPTION			REFERENCE DES		CRITICAL		BOM OPTION						
333S0354		4	IC, SGRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA			U8900, U8950, U9000, U9050		CRITICAL		VRAM_128_SAMSUNG						
333S0350		4	IC, SGRAM, GDDR3, 16MX32, 700MHZ, 136 FBGA			U8900, U8950, U9000, U9050		CRITICAL		VRAM_256_SAMSUNG						
333S0358		4	IC, SGRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA			U8900, U8950, U9000, U9050		CRITICAL		VRAM_128_HYNIX						
333S0351		4	IC, SGRAM, GDDR3, 16MX32, 700MHZ, 136 FBGA			U8900, U8950, U9000, U9050		CRITICAL		VRAM_256_HYNIX						
337S3282		1	IC, YDC, CO, 1.83G, 31W, 667M, 2M, 479BGA			U0700		CRITICAL		CPU_1_83GHZ						
337S3267		1	IC, YDC, CO, 2.0G, 31W, 667M, 2M, 479BGA			U0700		CRITICAL		CPU_2_0GHZ						
337S3268		1	IC, YDC, CO, 2.16G, 31W, 667M, 2M, 479BGA			U0700		CRITICAL		CPU_2_16GHZ						
341S1873		1	IC, EFI, BOOTROM DEVELOPMENT (NEW), M1			U6301		CRITICAL		BOOTROM_DEVEL						
338S0274		1	IC, SMC, HS8 / 2116			U5800		CRITICAL		SMC_BLANK						
341S1875		1	IC, PRGRM, SMC (NEW), M1			U5800		CRITICAL		SMC_PRGRM						
PART NUMBER		QTY	DESCRIPTION			REFERENCE DES		CRITICAL		BOM OPTION						
338S0268		1	IC, FW32306, 1394A LINK, BGA, 129P			U4400		CRITICAL								
338S0269		1	IC, 945GM, NORTHBRIDGE			U1200		CRITICAL								
338S0270		1	IC, 88E8053, GIGABIT ENET XCVR, 64P QFN, NO			U4101		CRITICAL								
338S0309		1	IC, ATI, M56P, GRPHSCTRL, 880BGA, LF			U8400		CRITICAL		ATI_REV_B24						
338S0315		1	IC, ATI, M56-LP, B26, GRPHXCRTL, LF 880BGA			U8400		CRITICAL		ATI_REV_B26						
341S1789		1	IC, TPM, 28-PIN TSSOP			U6700		CRITICAL								
341S1797		1	IC, EEPROM, SERIAL IIC, 8KBIT, SO8			U4102		CRITICAL								
343S0385		1	IC, ICH7M, BGA			U2100		CRITICAL								
353S1465		1	IC, ISL6262, SYNC REG CTRL, SCREENED, QFN48			U7530		CRITICAL								
359S0101		1	IC, CY28445-5, CLOCK GEN, 68PIN QFN			U3301		CRITICAL								
Alternate Parts																
PART NUMBER		ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES		COMMENTS:										
128S0094		128S0060		ALL		330uF, 2V, 9MOHM, D2										
128S0095		128S0060		ALL		330uF, 2V, 6MOHM, D2										
128S0081		128S0061		ALL		150uF, 6.3V, 25MOHM, C2										
376S0448		376S0445		ALL		SI7806ADN for FDM6296										
BOM Configuration																
SYNC_MASTER=N/A SYNC_DATE=N/A																
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										NONE						
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CPU Decoupling & VID

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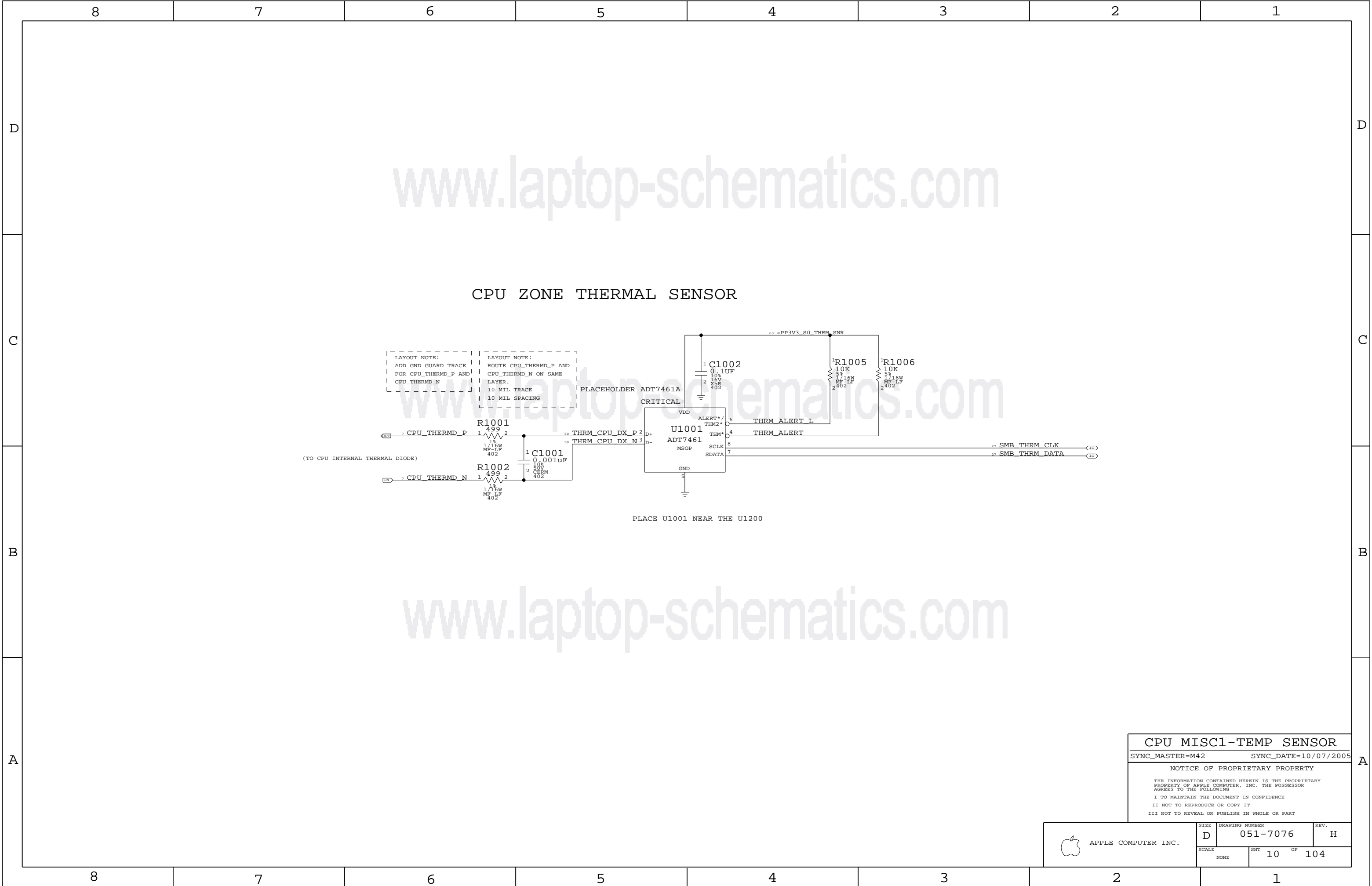
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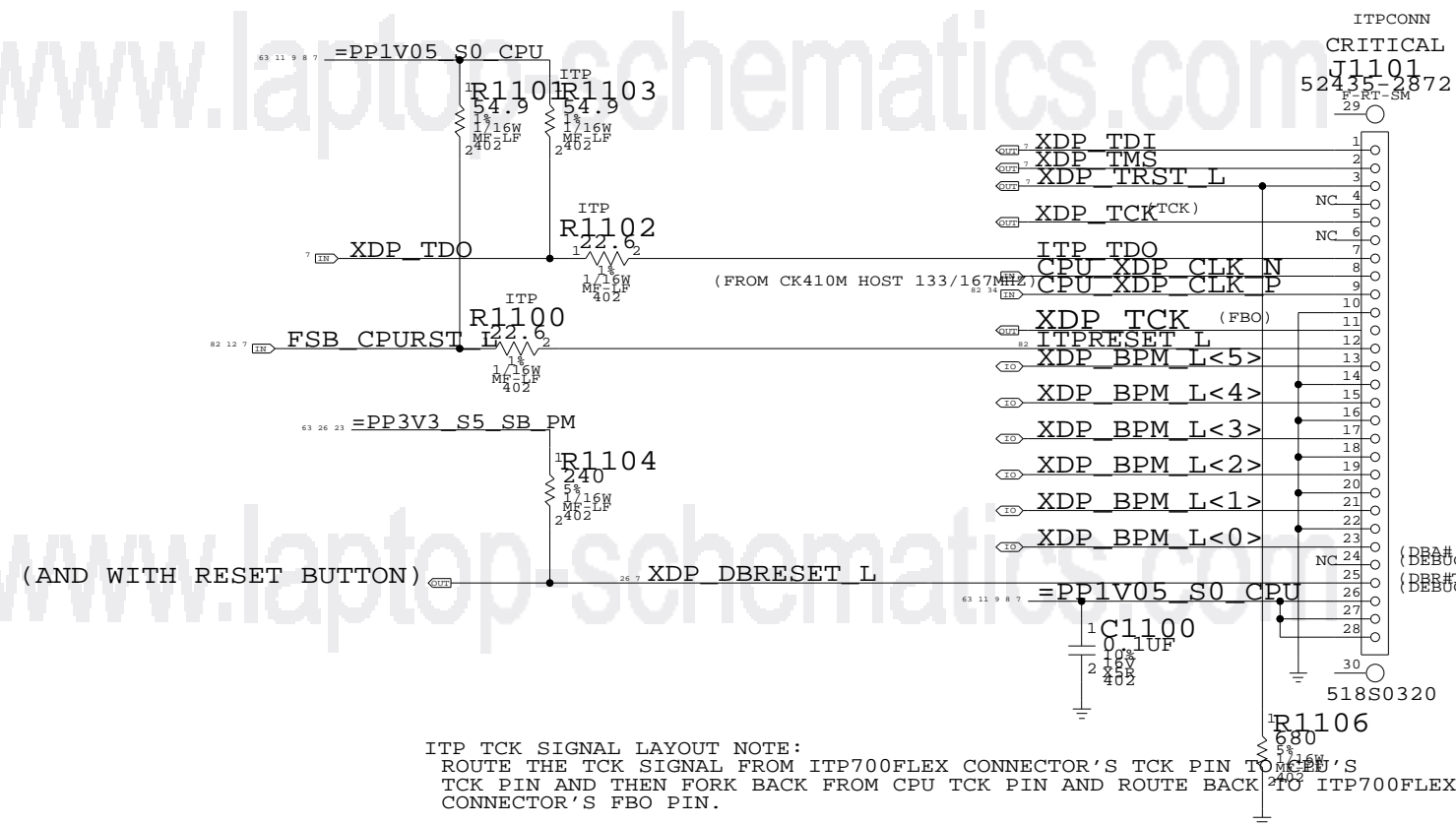
4

3

2

1

CPU ITP700FLEX DEBUG SUPPORT



ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S
TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX
CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG	
SYNC_MASTER=MS	SYNC_DATE=10/12/2005

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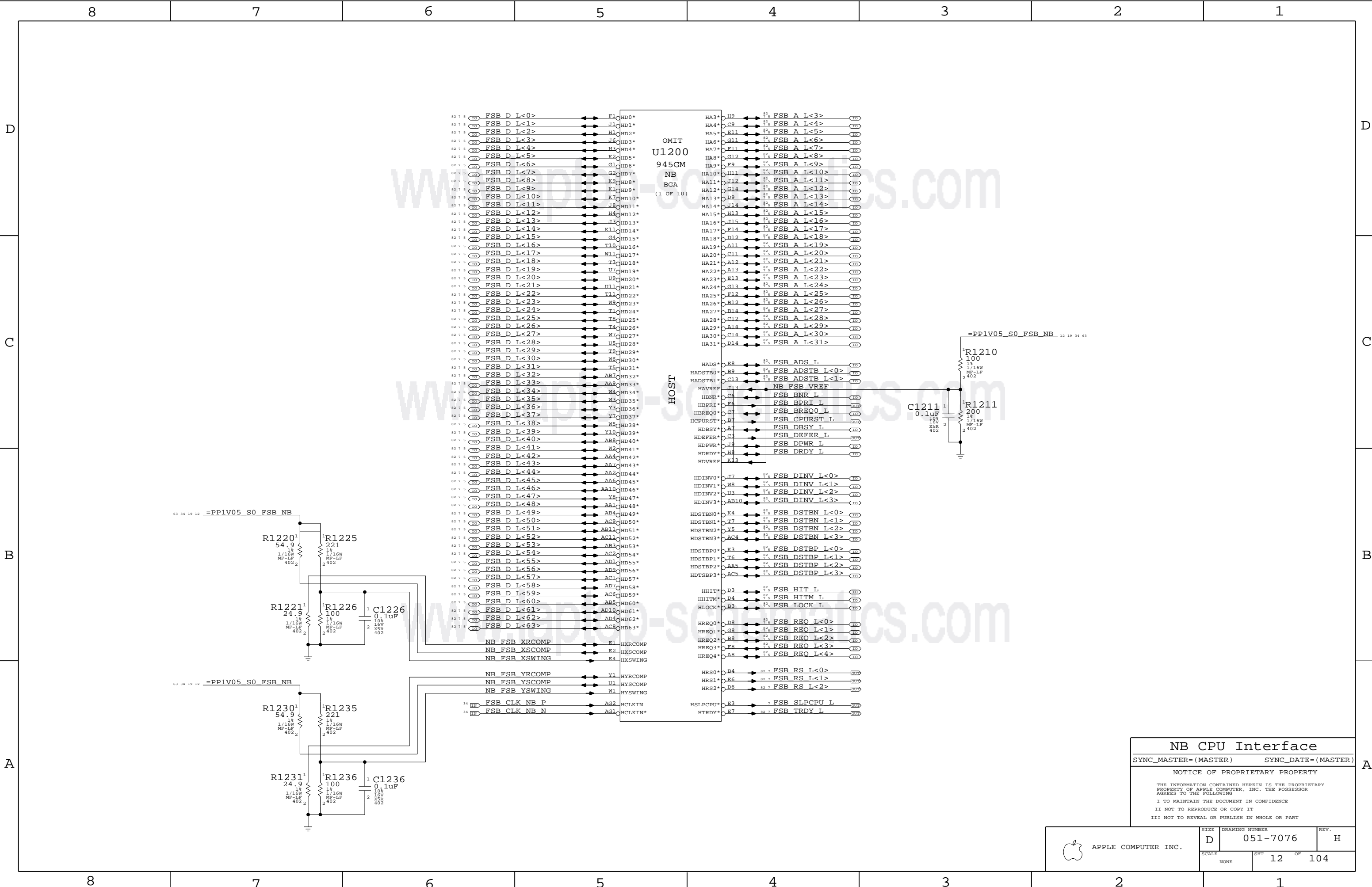
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SIZE D	DRAWING NUMBER 051-7076	REV. H
SCALE NONE	SHT 11 OF 104	



NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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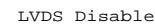
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	D	051-7076	H
SCALE		SHT	12 OF 104
NONE			



Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

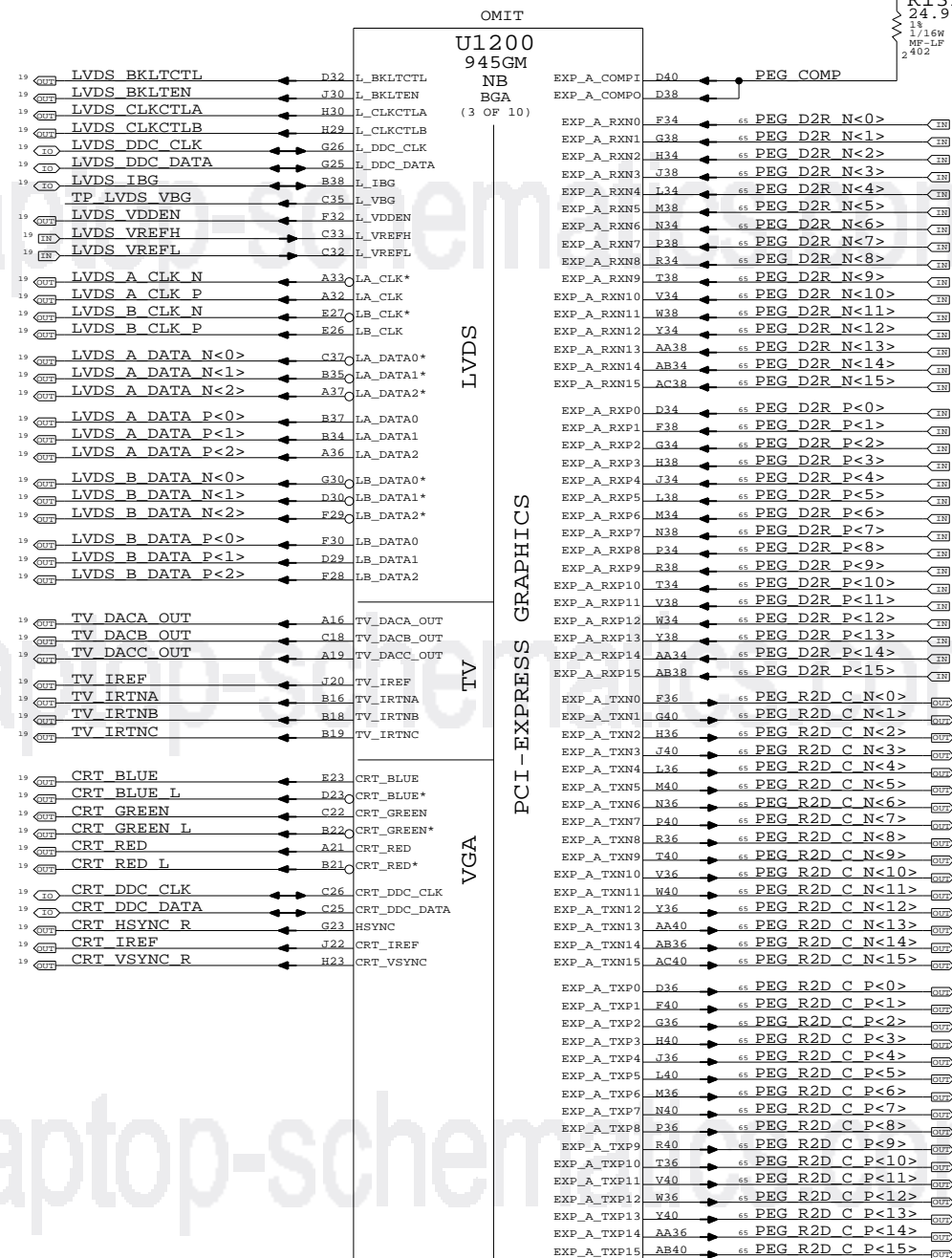
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



SDVO Alternate Function

SDVO_TVCLKIN#
SDVO_INT#
SDVO_FLDSTALL#

SDVO_TVCLKIN
SDVO_INT
SDVO_FLDSTALL

```
SDVOB_RED#
SDVOB_GREEN#
SDVOB_BLUE#
SDVOB_CLKN
SDVOC_RED#
SDVOC_GREEN#
SDVOC_BLUE#
SDVOC_CLKN
```

SDVOB_RED
SDVOB_GREEN
SDVOB_BLUE
SDVOB_CLKP
SDVOC_RED
SDVOC_GREEN
SDVOC_BLUE
SDVOC_CLKP

NB PEG / Video Interfaces

SYNC_MASTER= (MASTER)	SYNC_DATE= (MASTER)	7
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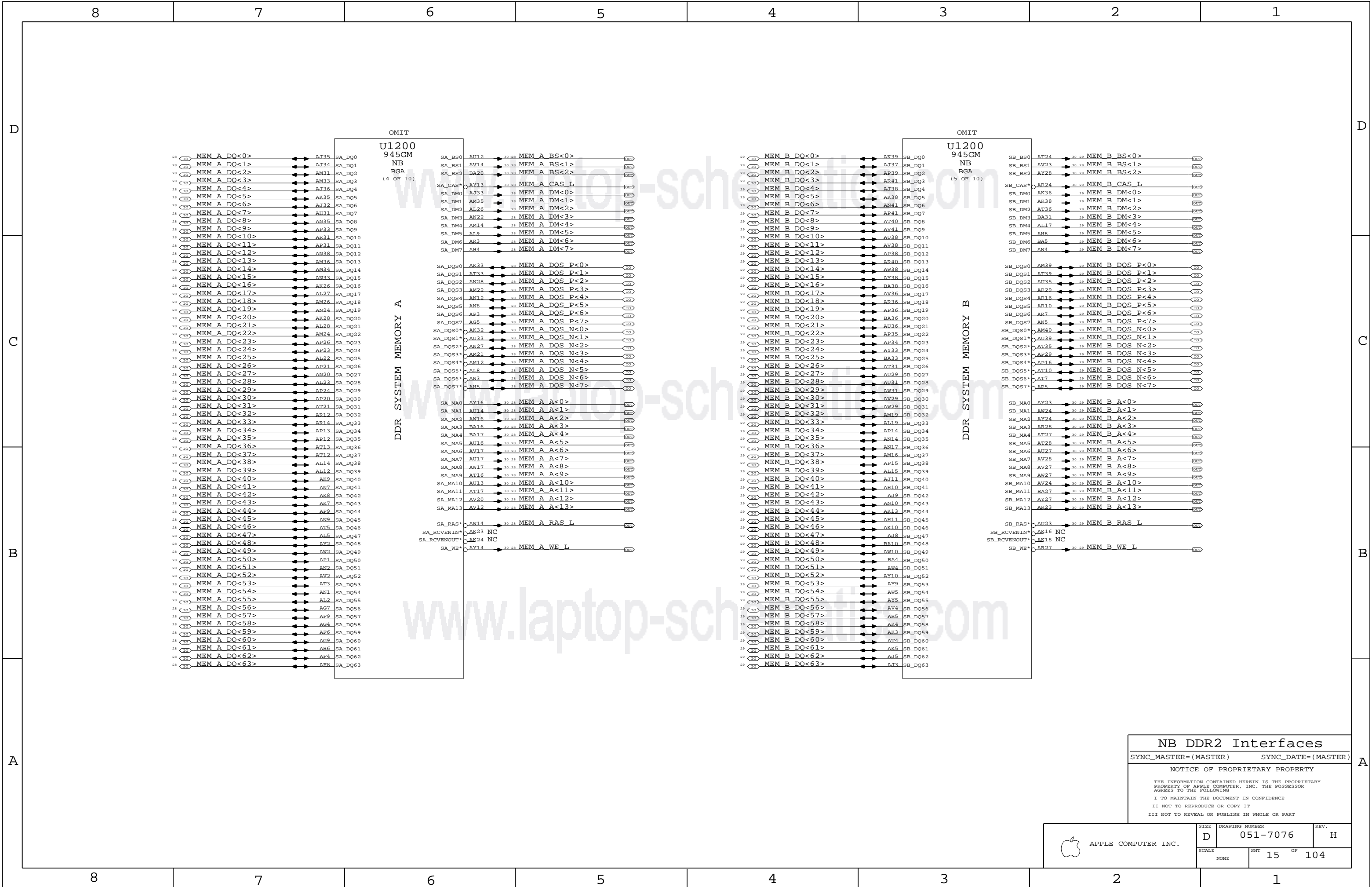
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SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF
NONE	13	104



NB DDR2 Interfaces

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

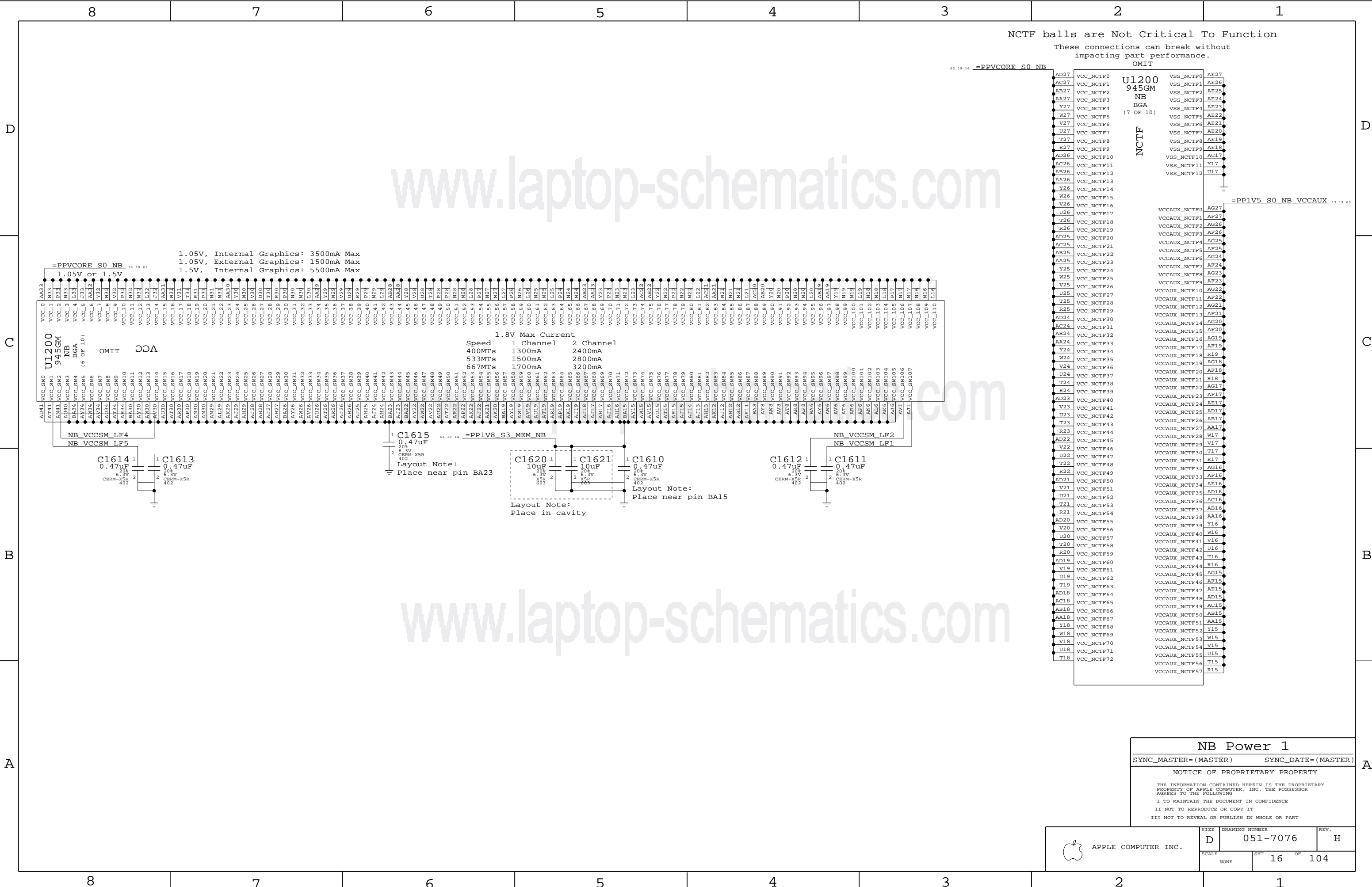
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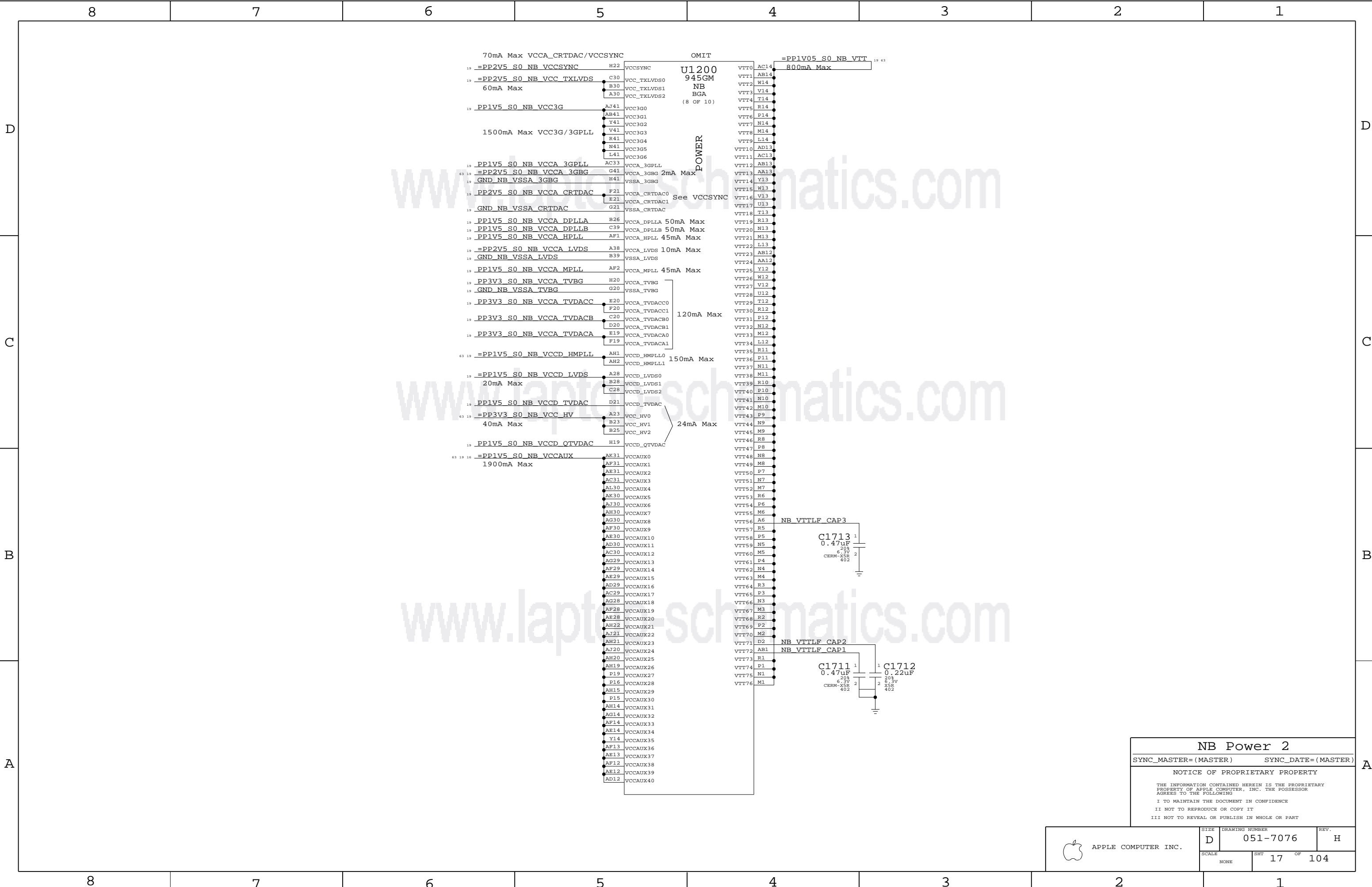
NCTF balls are Not Critical To Function
These connections can break without
impacting part performance.
OMIT

1.05V, Internal Graphics: 3500mA Max
1.05V, External Graphics: 1500mA Max
1.5V, Internal Graphics: 5500mA Max

1.8V Max Current
Speed 1 Channel 2 Channel
400MTs 1300mA 2400mA
533MTs 1500mA 2800mA
667MTs 1700mA 3200mA

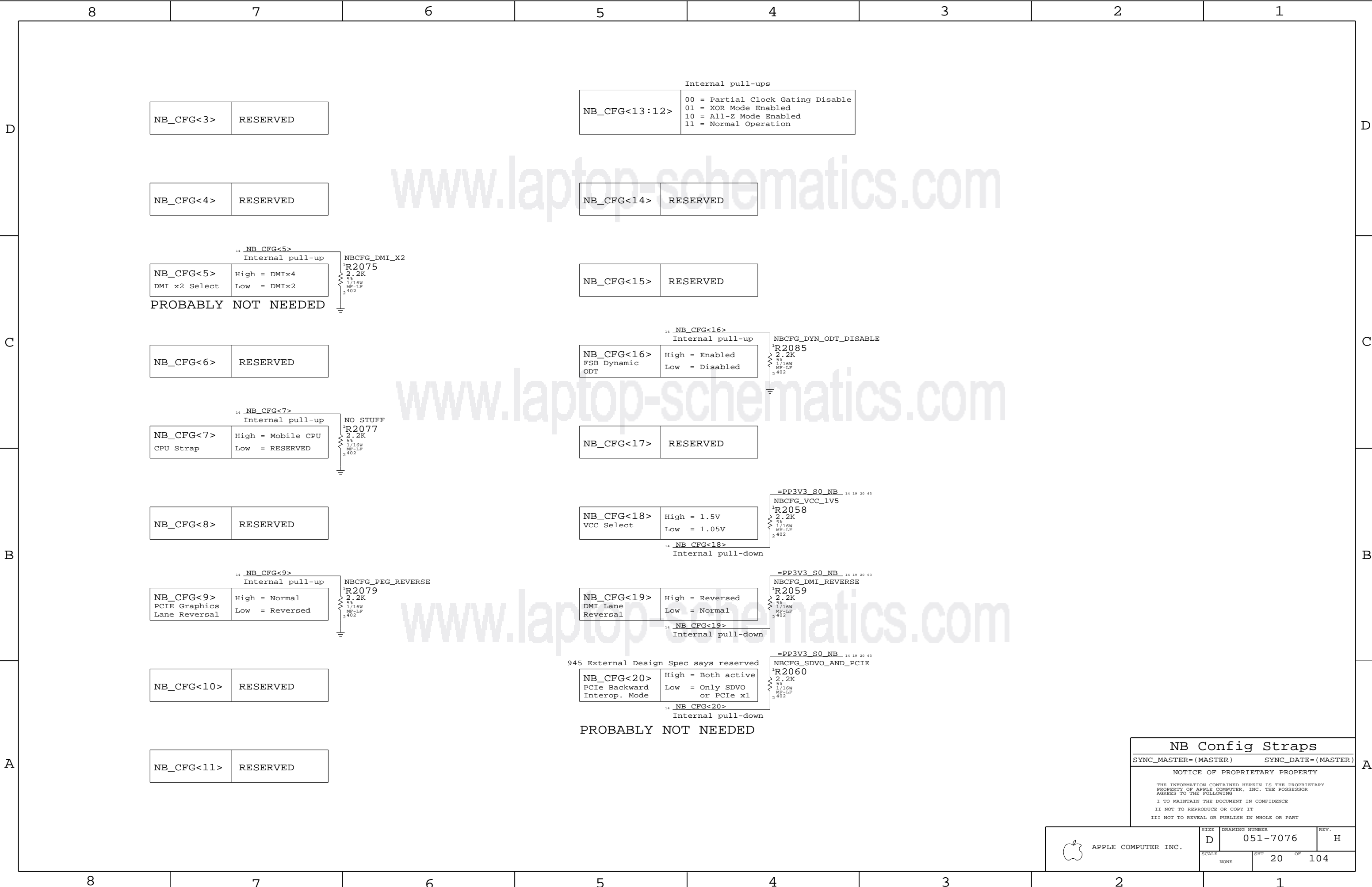
NB Power 1
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7076	REV. H
	SCALE NONE	SHT 16	OF 104

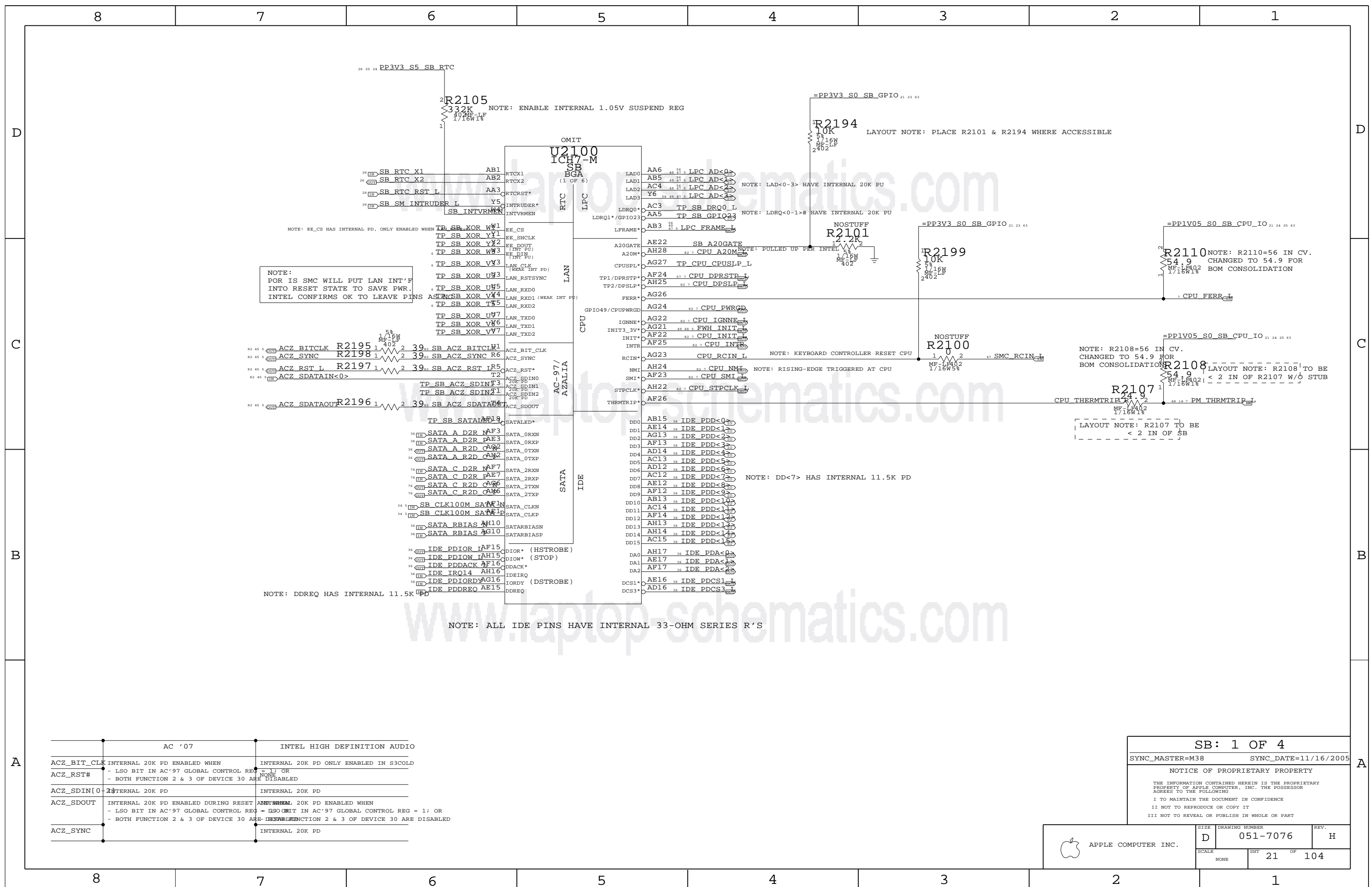


NB Power 2
SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7076	REV. H
	SCALE NONE	SHT 17	OF 104



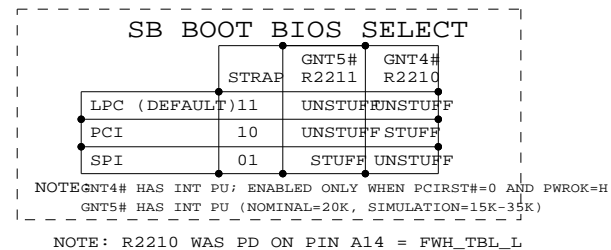
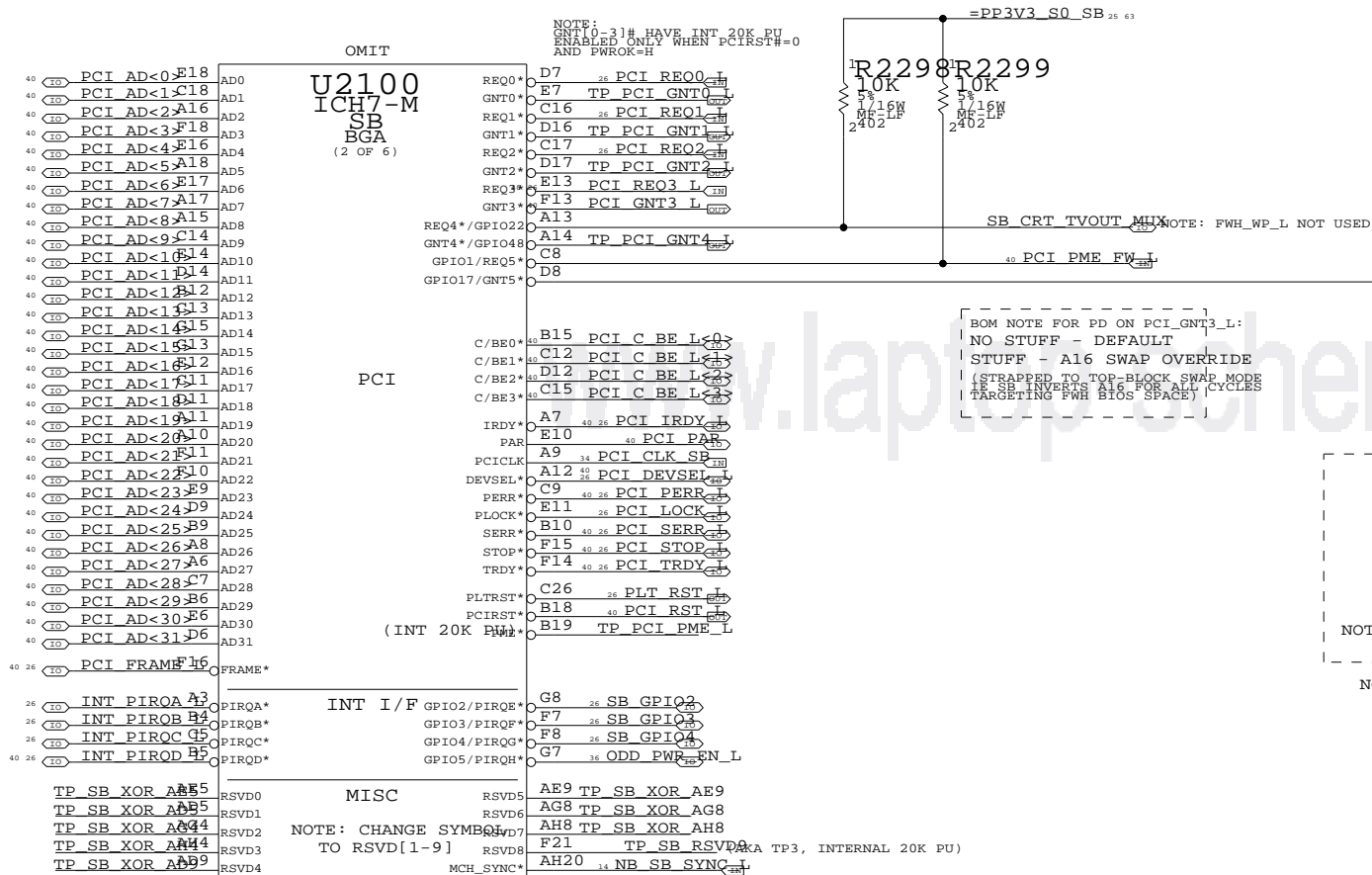
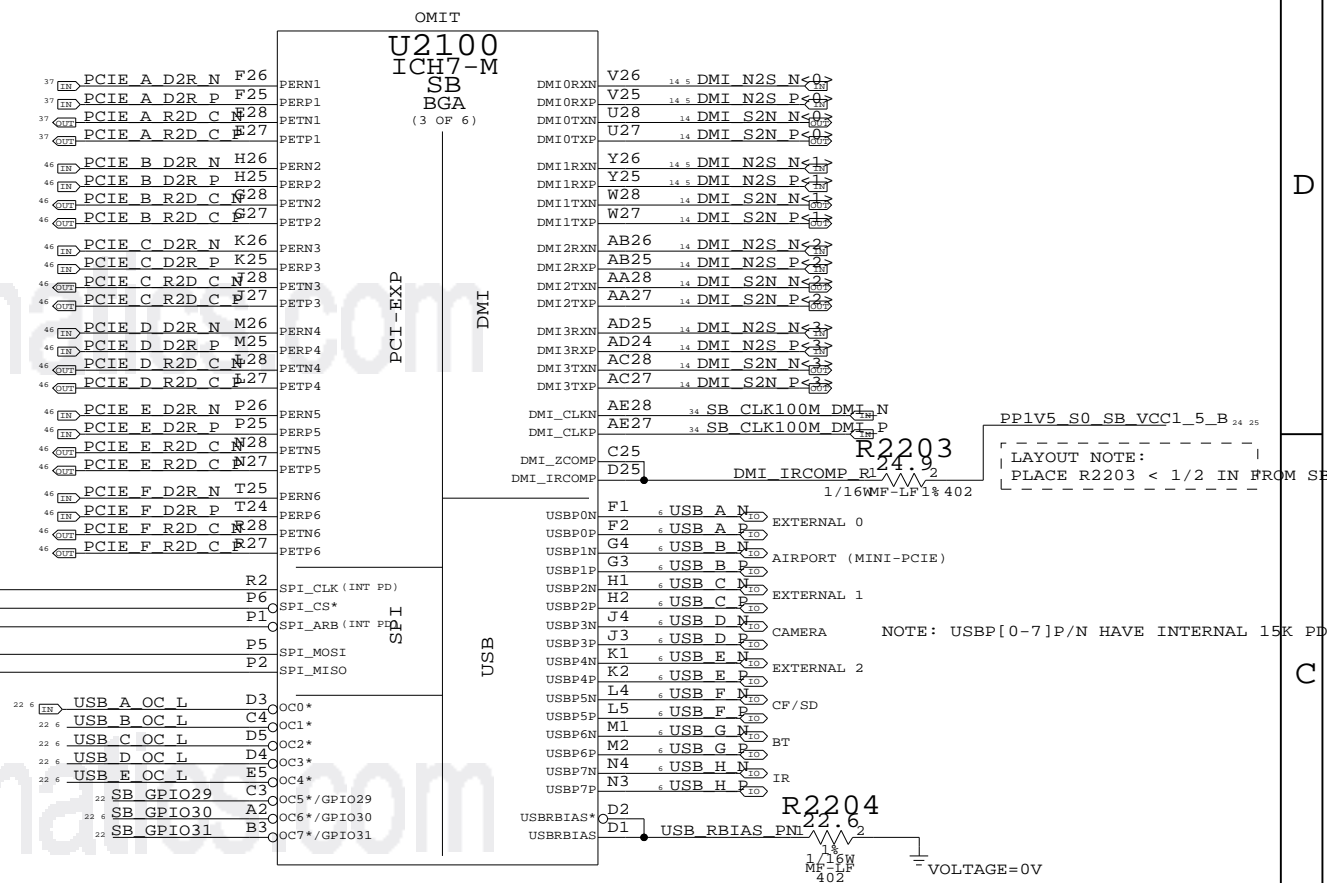
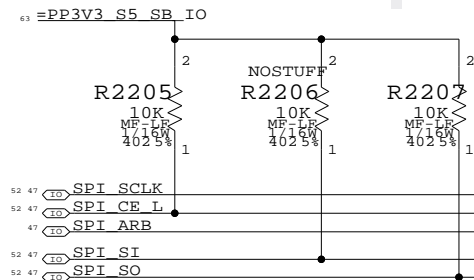
NB Config Straps		
SYNC_MASTER= (MASTER)		SYNC_DATE= (MASTER)
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```

22 SB_GPIO29
22 6 SB_GPIO30
22 SB_GPIO31

```



SB: 2 OF 4

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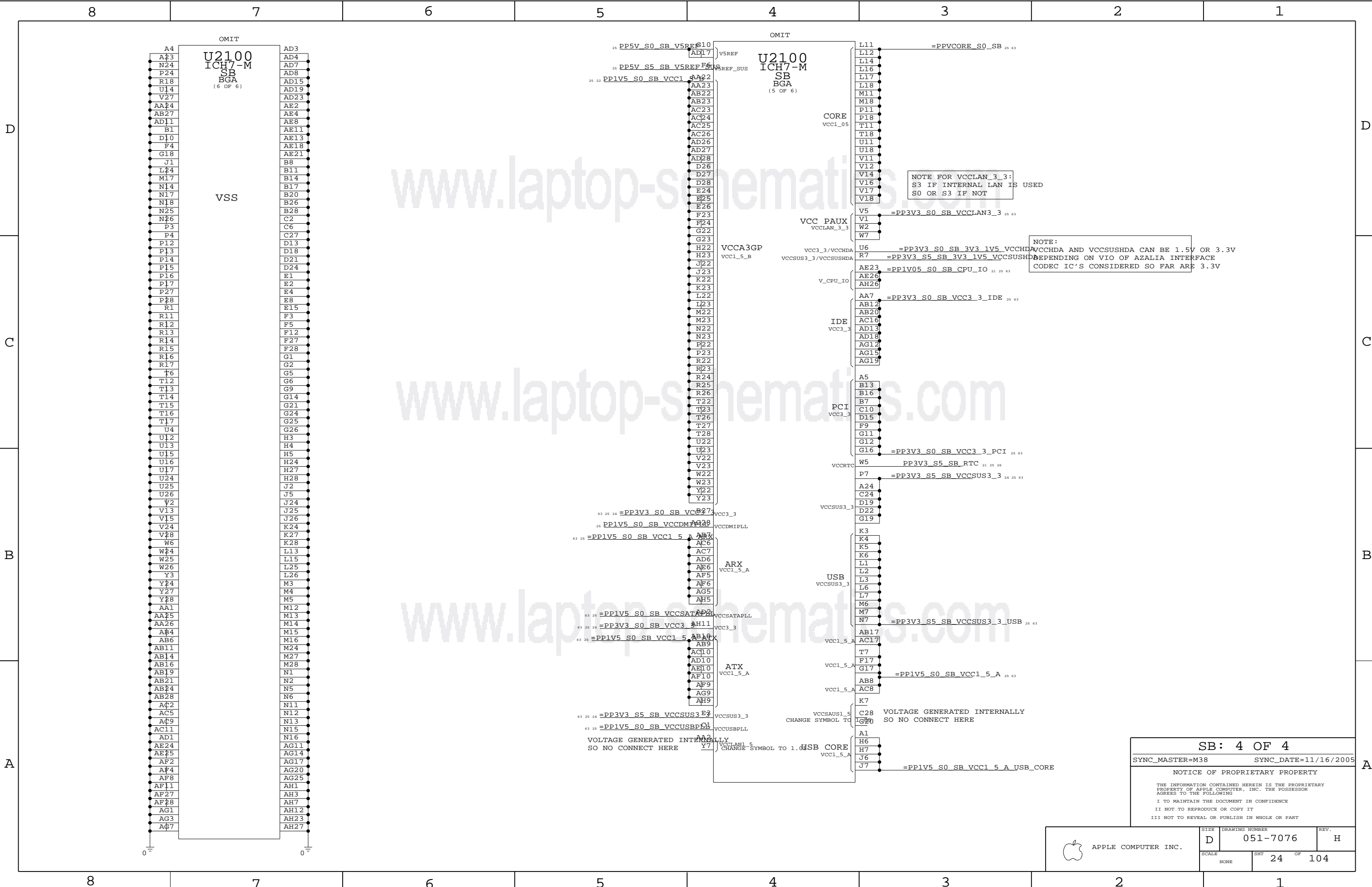
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APPLE COMPUTER INC

SIZE D	DRAWING NUMBER 051-7076		REV
SCALE NONE	SHT 22	OF 104	



NOTE FOR VCCLAN_3_3:
S3 IF INTERNAL LAN IS USED
S0 OR S3 IF NOT

NOTE:
VCC3_3/VCCCHDA AND VCCSUS3_3/VCCSUSHDA CAN BE 1.5V OR 3.3V
DEPENDENT ON VIO OF AZALIA INTERFACE
CODEC IC'S CONSIDERED SO FAR ARE 3.3V

VOLTAGE GENERATED INTERNALLY
SO NO CONNECT HERE

SB: 4 OF 4

SYNC_MASTER=M38 SYNC_DATE=11/16/2005

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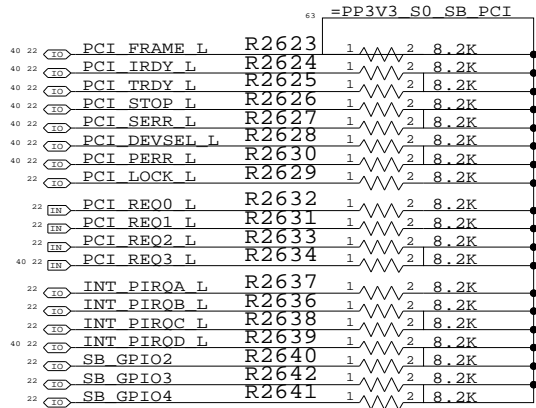
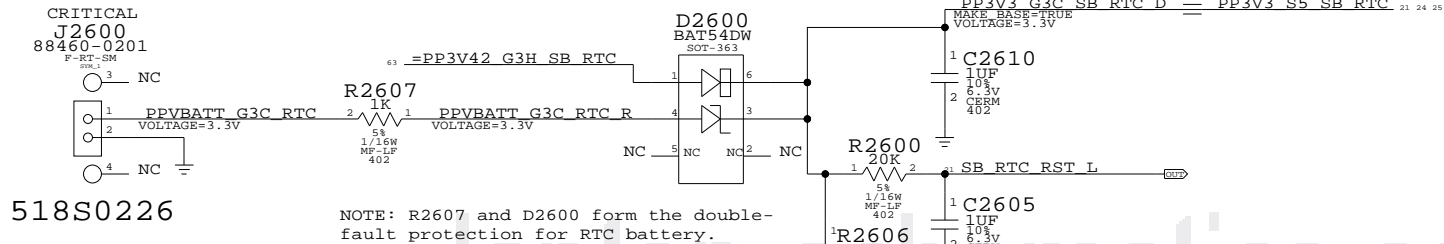
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

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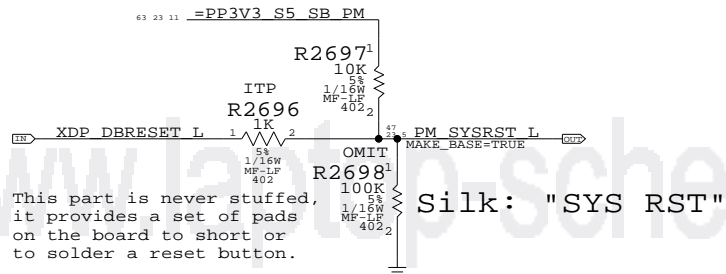
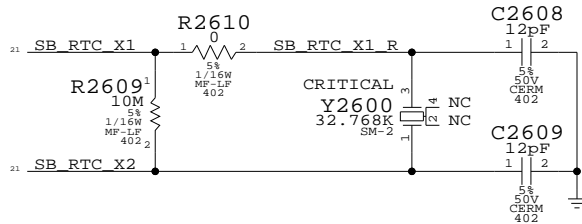
SIZE D DRAWING NUMBER 051-7076 REV. H

SCALE NONE SHT 24 OF 104

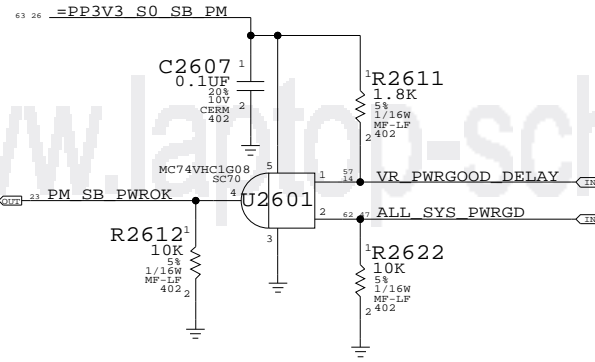
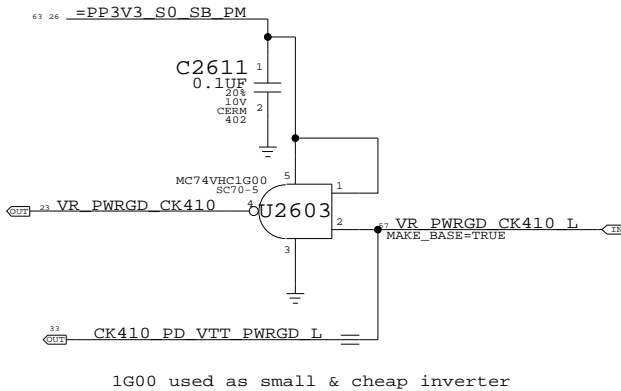
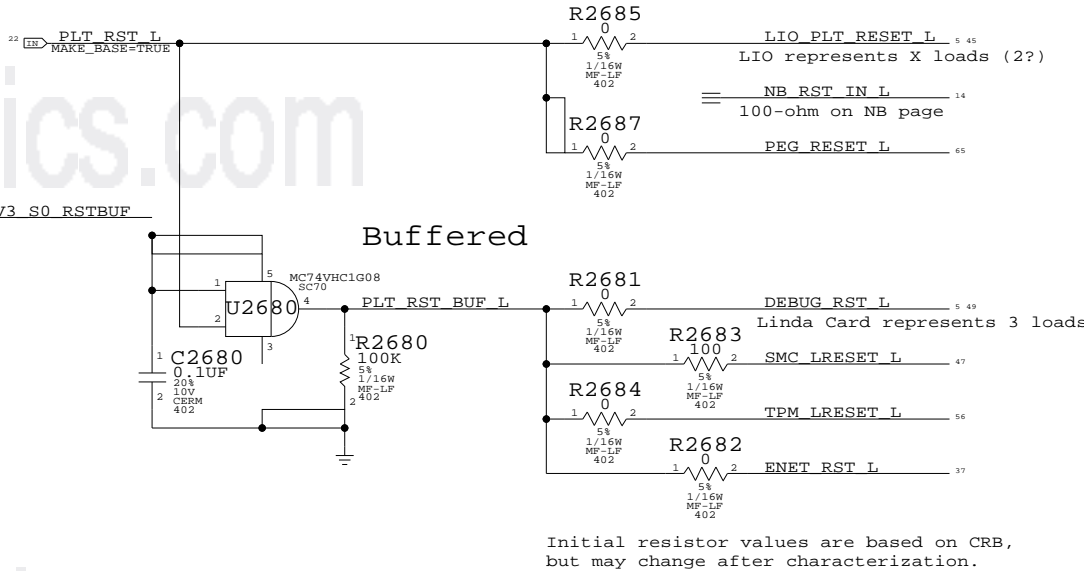
RTC Battery Connector



SB RTC Crystal Circuit

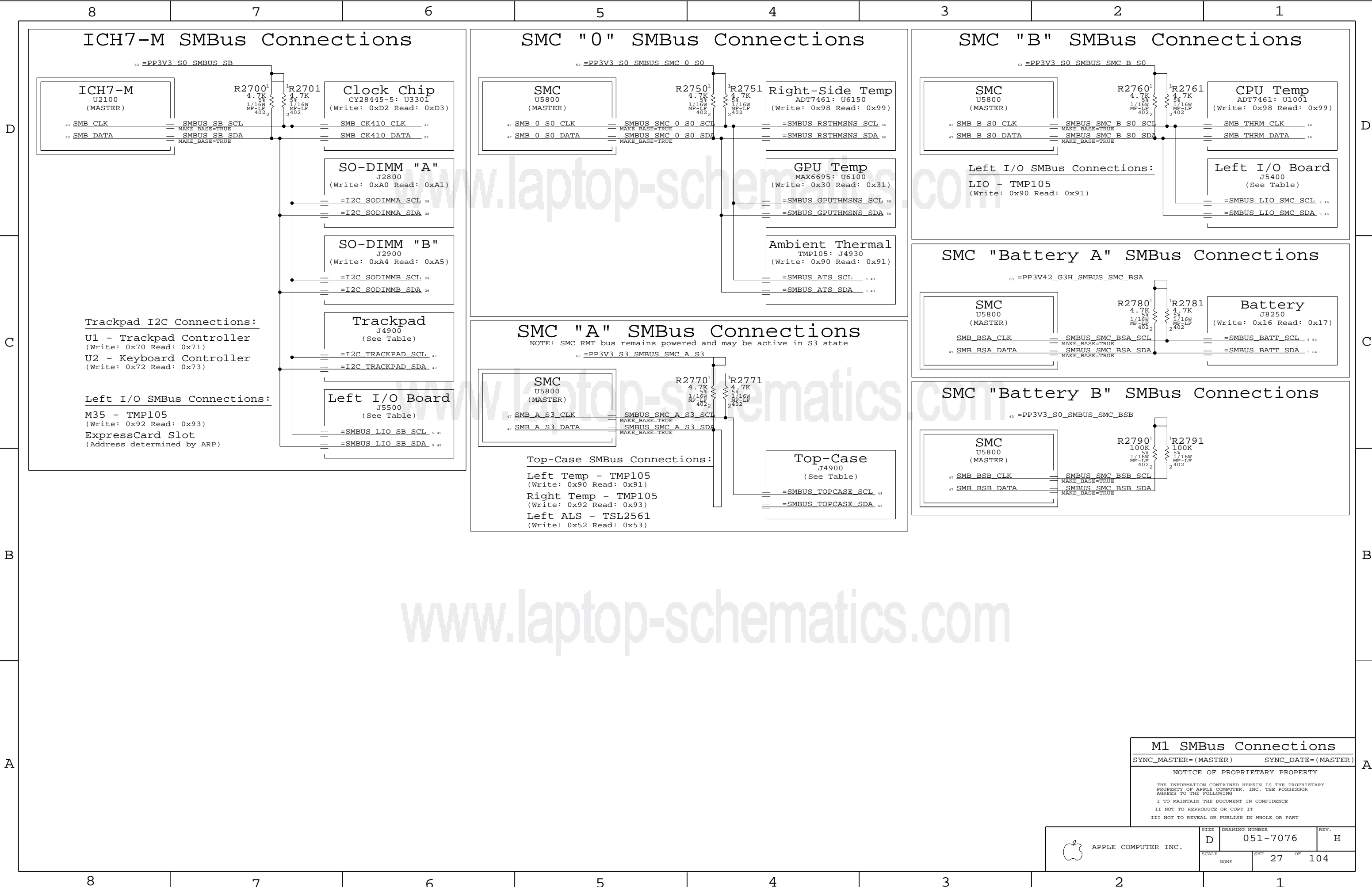


Platform Reset Connections
Unbuffered



SB Misc		
SYNC_MASTER=(MASTER)		SYNC_DATE=(MASTER)
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	D	051-7076	H
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NONE		26	104



M1 SMBus Connections
SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)
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Page Notes

Power aliases required by this page:

- =P1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:

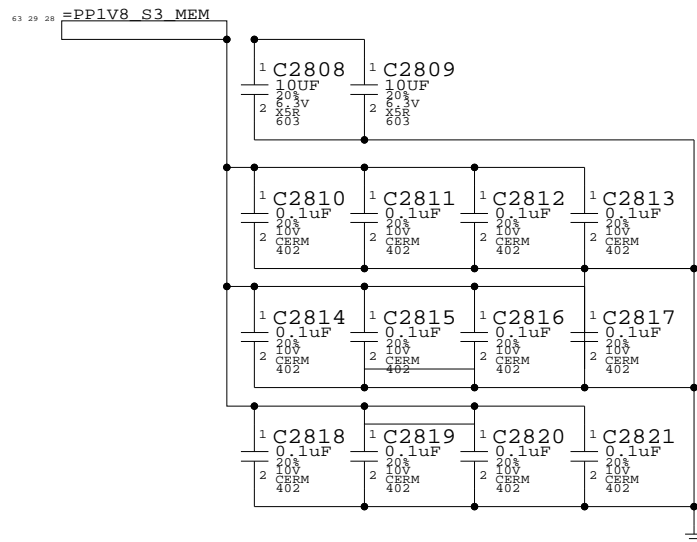
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided by another page.

"Lower" (surface-mount) slot

DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE D DRAWING NUMBER 051-7076 REV. H

SCALE NONE SHT 28 OF 104

Page Notes

Power aliases required by this page:

- =P1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:

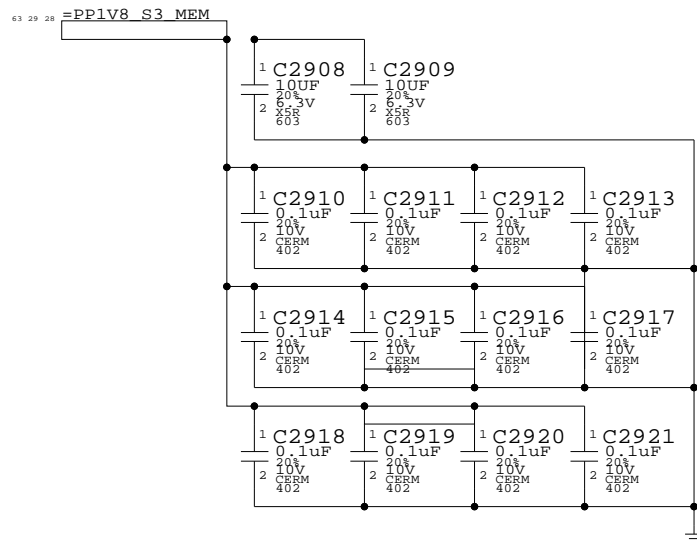
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

"Upper" (thru-hole) slot

DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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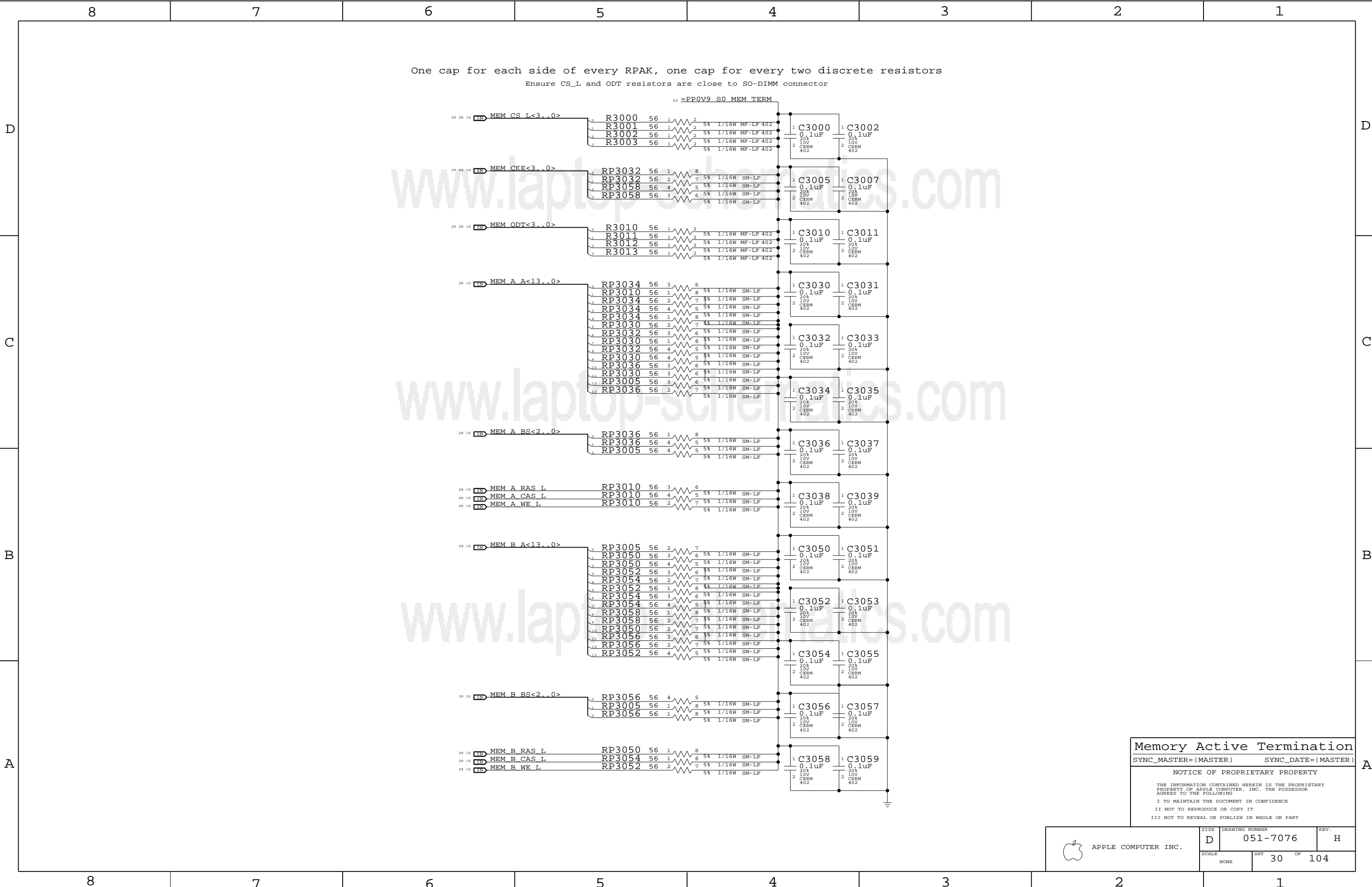
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SIZE D DRAWING NUMBER 051-7076 REV. H

SCALE NONE SHT 29 OF 104



Memory Active Termination

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

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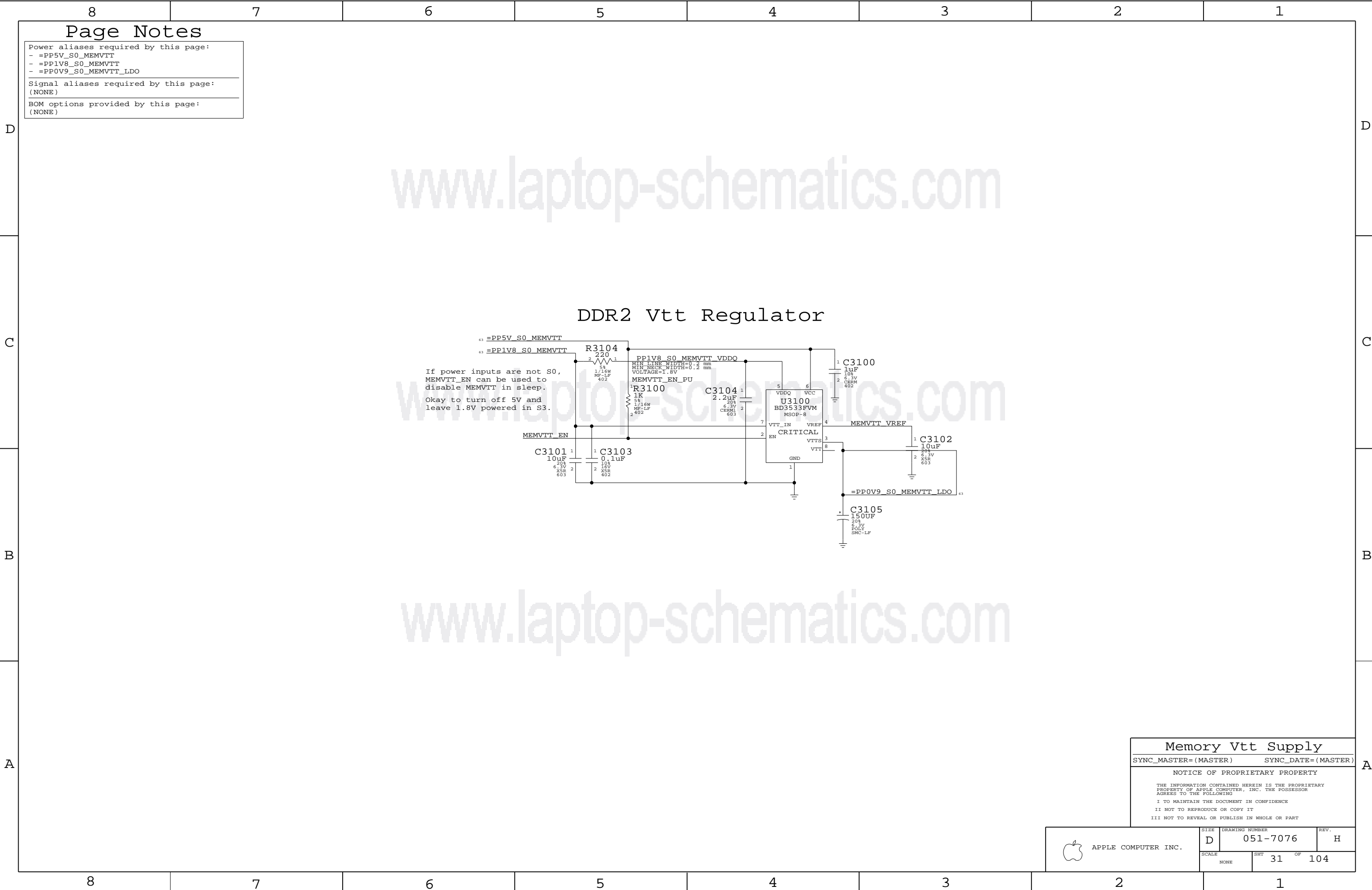
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART




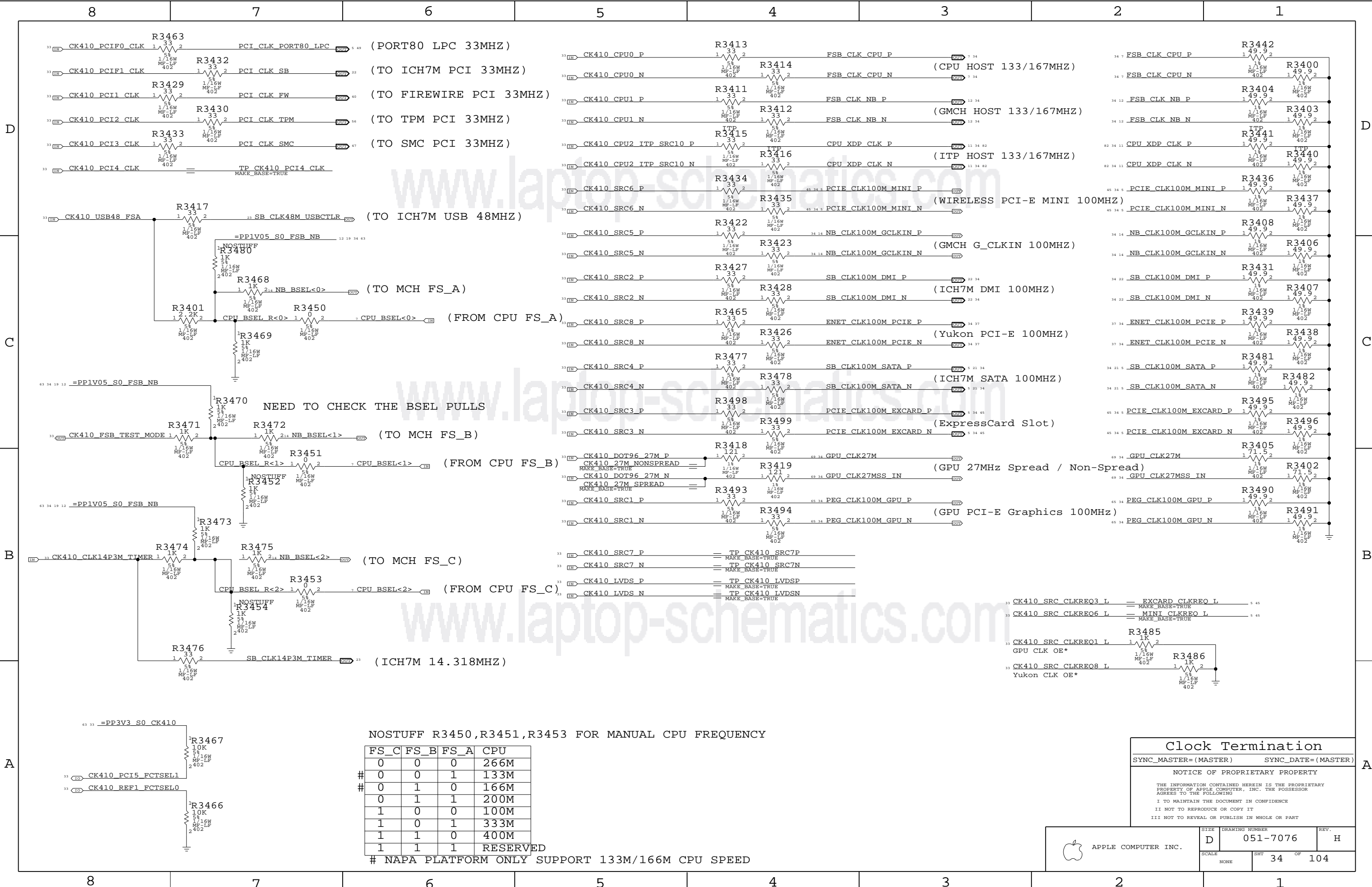
APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-7076 REV. H

SCALE NONE SHT 30 OF 104



 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7076	H
	SCALE	SHT OF	
	NONE	32 104	



NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

	FS_C	FS_B	FS_A	CPU
#	0	0	0	266M
#	0	0	1	133M
#	0	1	0	166M
	0	1	1	200M
	1	0	0	100M
	1	0	1	333M
	1	1	0	400M
	1	1	1	RESERVED

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED

Clock Termination

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE

D

DRAWING NUMBER

051-7076

REV.

H

SCALE

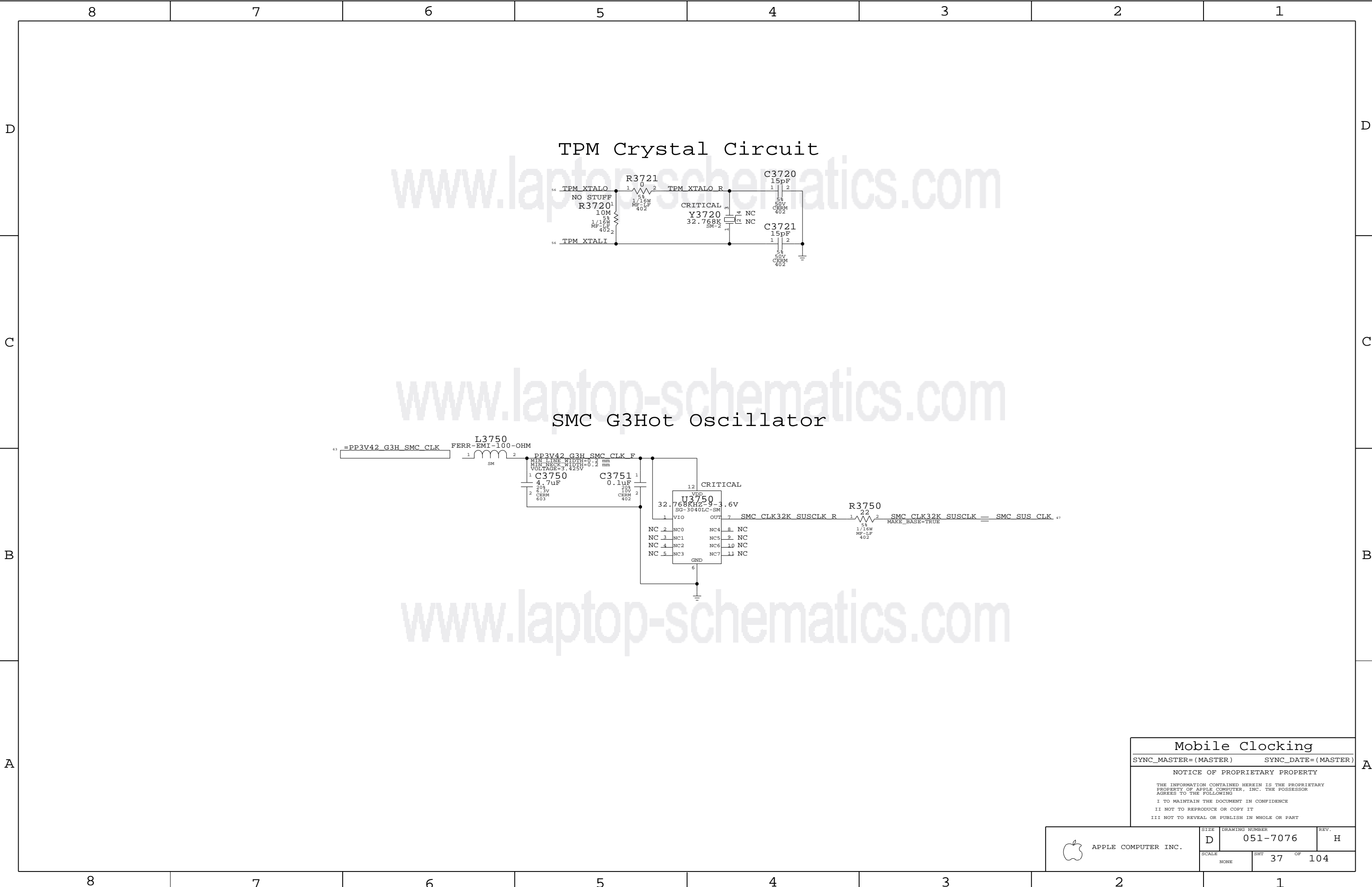
NONE

SHT

34

OF

104



Mobile Clocking

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

NOTICE OF PROPRIETARY PROPERTY

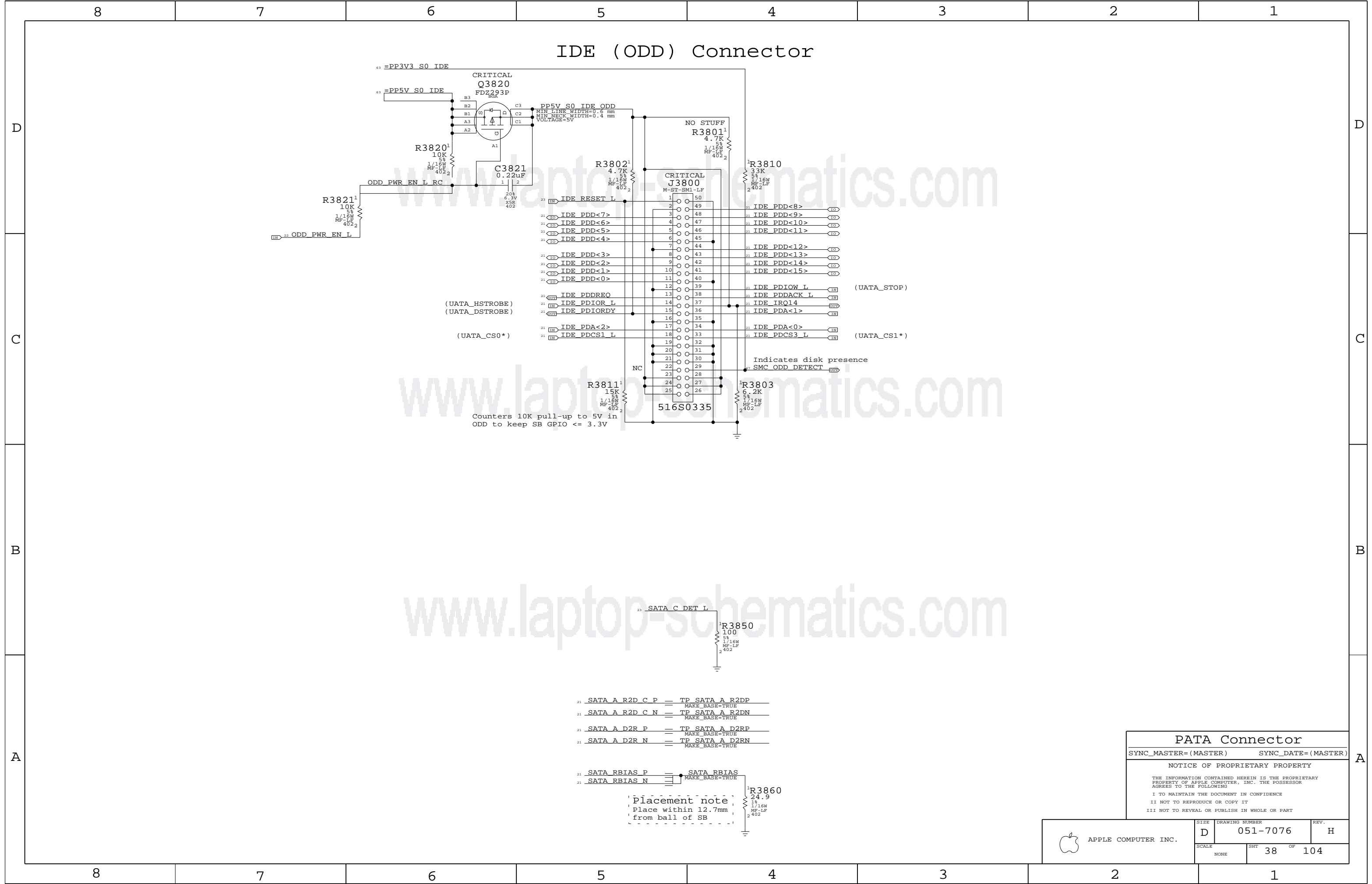
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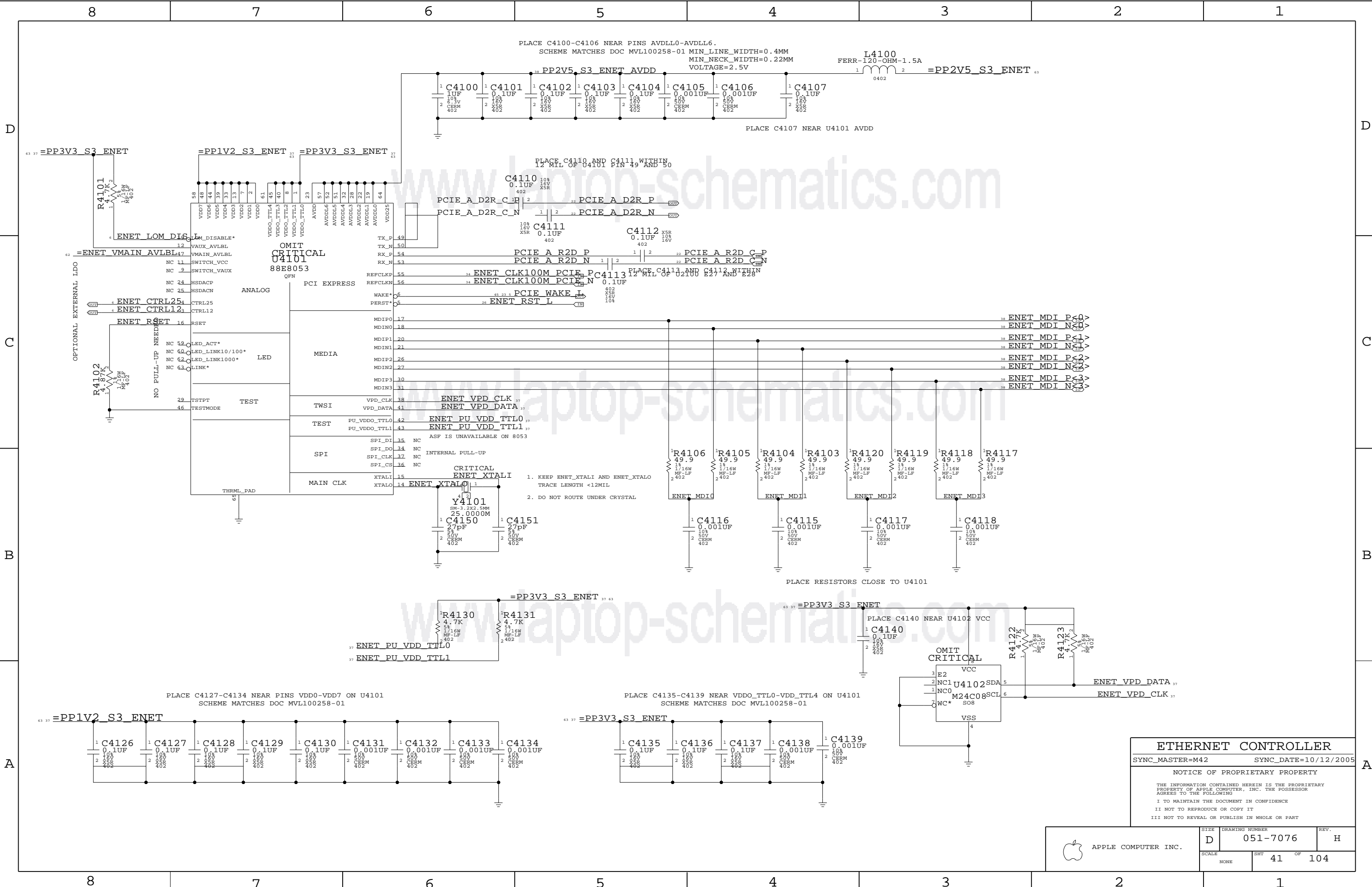
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ETHERNET CONTROLLER

SYNC_MASTER=M42

SYNC_DATE=10/12/2005

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE	
	SPACING	PHYSICAL
PROVIDED	ENETCONN	ENET_100D
	ENETCONN	ENET_100D
	ENETCONN	ENET_100D
	ENETCONN	ENET_100D
BY	ENETCONN	ENET_100D
	ENETCONN	ENET_100D
	ENETCONN	ENET_100D
	ENETCONN	ENET_100D
ETHERNET	ENETCONN	ENET_100D
	ENETCONN	ENET_100D
	ENETCONN	ENET_100D
	ENETCONN	ENET_100D
PHY	ENETCONN	ENET_100D
	ENETCONN	ENET_100D
	ENETCONN	ENET_100D
	ENETCONN	ENET_100D

Page Notes

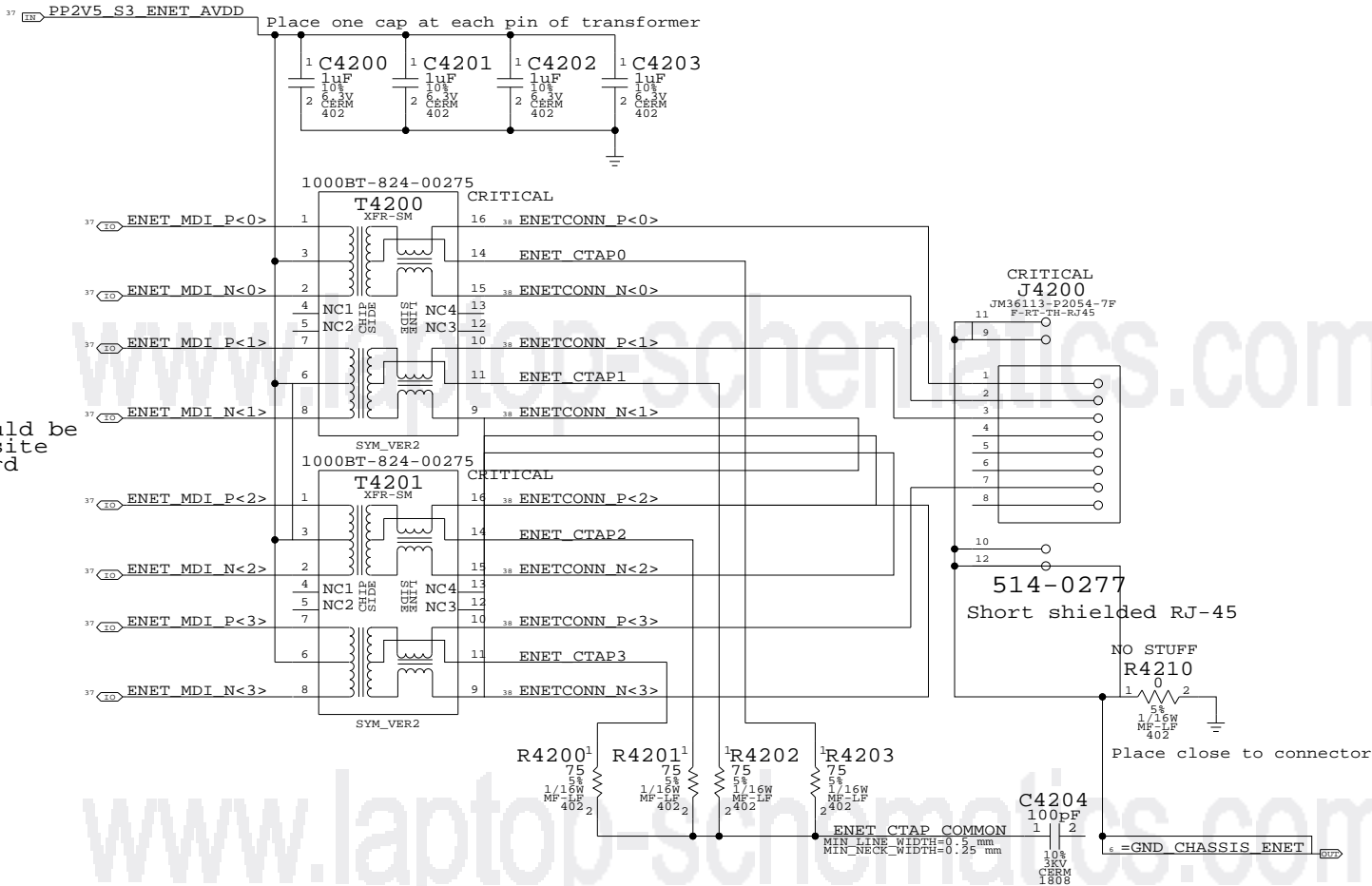
Power aliases required by this page:

- =PP2V5_ENET
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Transformers should be mirrored on opposite sides of the board



Ethernet Connector

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

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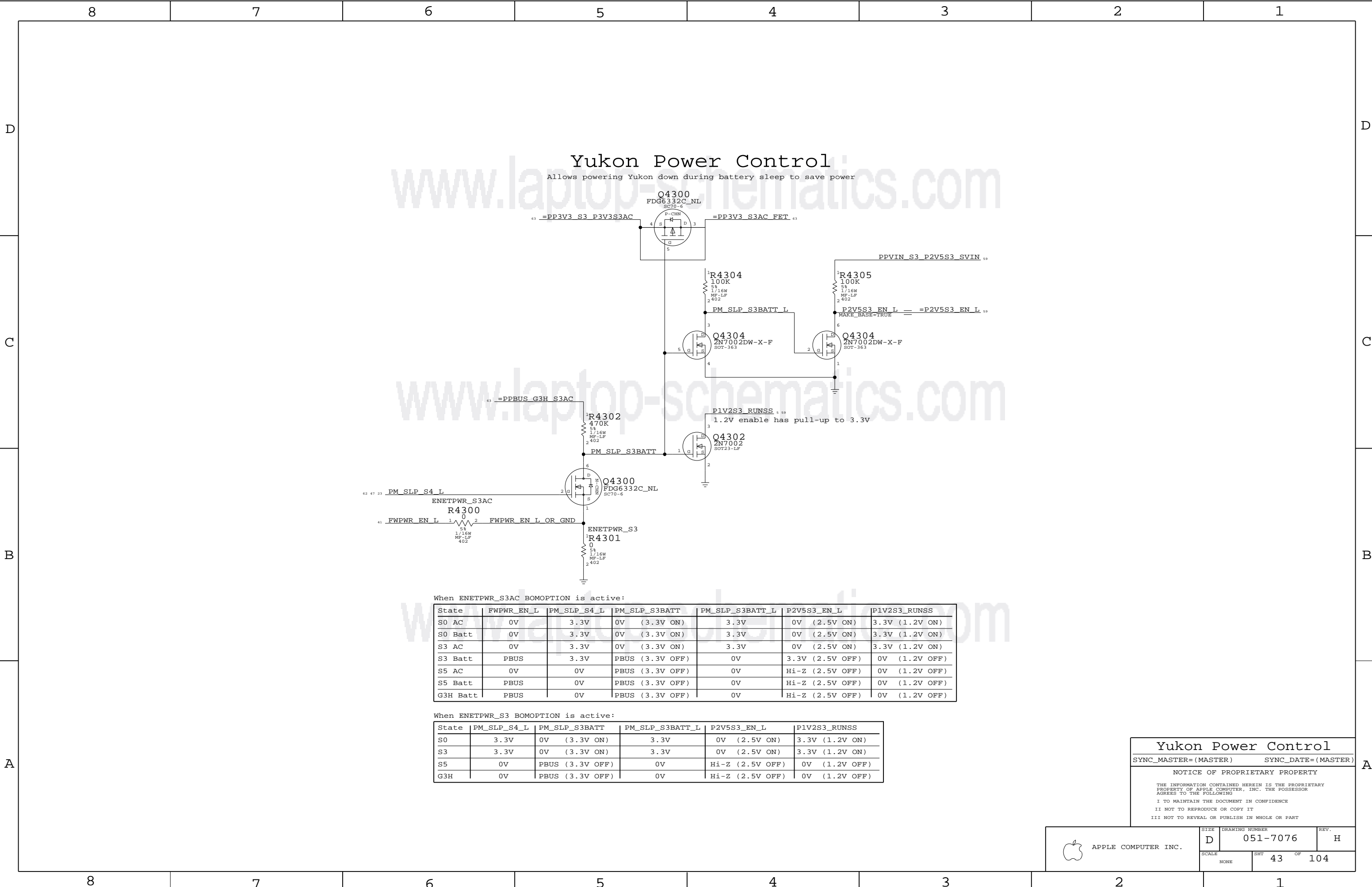
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	D	051-7076	H
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NONE		42	104



PAGE NOTES

INPUT
=PP3V3_S0_FW - 3.3V POWER FOR FIREWIRE (MOBILE: OFF DURING SLEEP)
=PP3V3_S0_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)
PCI_GNT3_L - PCI GRANT FROM SB
PCI_CLK_FW - NEED TO REFERENCE TO ALIAS PAGE
PCI_RST_L - PCI RESET FROM SB
FW_PC0 - FIREWIRE POWER CLASS IDENTIFIER

INPUT/OUTPUT

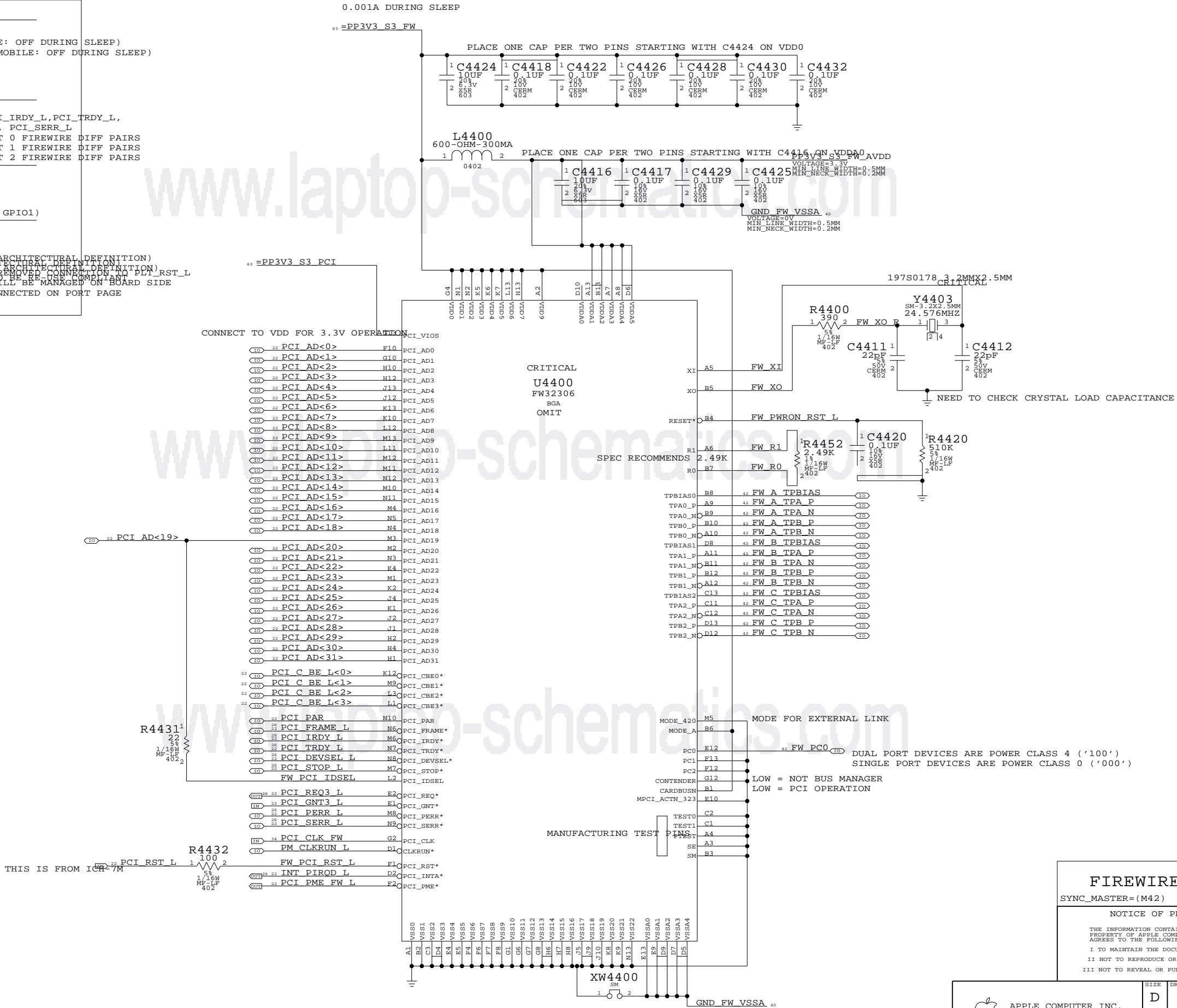
PCI_AD<0..31>, PCI_C_BE_L<0..3>, PCI_FRAME_L, PCI_IRDY_L, PCI_TRDY_L,
PCI_DEVSEL_L, PCI_STOP_L, PCI_PAR, PCI_PERR_L, PCI_SERR_L
FW_A_TPA_P/N, FW_A_TPB_P/N, FW_A_TPBias - PORT 0 FIREWIRE DIFF PAIRS
FW_B_TPA_P/N, FW_B_TPB_P/N, FW_B_TPBias - PORT 1 FIREWIRE DIFF PAIRS
FW_C_TPA_P/N, FW_C_TPB_P/N, FW_C_TPBias - PORT 2 FIREWIRE DIFF PAIRS

OUTPUT

PCI_REQ3_L - PCI REQUEST TO SB
PM_CLKRUN_L - CLOCK-RUN PCI PROTOCOL
INT_PIRQD_L - INTERRUPT TO SB
PCI_PME_FW_L - DEDICATED PME FOR FIREWIRE (SB GPIO1)

PAGE HISTORY

5/18/2005 - FIRST REVISION OF PAGE
6/22/2005 - BGA VERSION OF FW223-06 ADDED
7/21/2005 - CHANGED INT ID TO AD19 (PER ARCHITECTURAL DEFINITION)
8/22/2005 - CHANGED PCI_GNT3_L TO PCI_GNT3_L (PER ARCHITECTURAL DEFINITION)
9/22/2005 - ADDED PCI_RST_L - DOWN ON RST3 AND REMOVED CONNECTION TO PLT_RST_L
10/22/2005 - ADDED FW_PC0 - FIREWIRE POWER CLASS IDENTIFIER
11/22/2005 - REMOVED CONSTRAINTS AS THEY WILL BE MANAGED ON BOARD SIDE
12/22/2005 - REMOVED C4431 - REDUNDANT
1/26/2005 - BEING OUT PCI CONNECTION TO BE CONNECTED ON PORT PAGE
CONNECTED PIN E10 TO GND



FIREWIRE CONTROLLER

SYNC_MASTER=(M42) SYNC_DATE=08/29/2005

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE	
	SPACING	PHYSICAL
PROVIDED	FW	FW_110D
BY	FW	FW_110D
PHY	FW	FW_110D
PAGE	FW	FW_110D

Page Notes

Power aliases required by this page:

- =PPFW_PORT1
- =PP3V3_S5_FWLATEVG
- =GND_CHASSIS_FW_PORT1

Signal aliases required by this page:

(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:

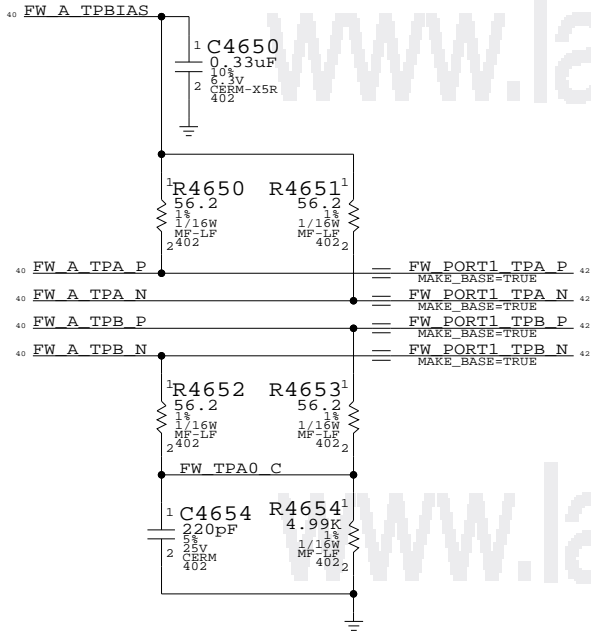
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

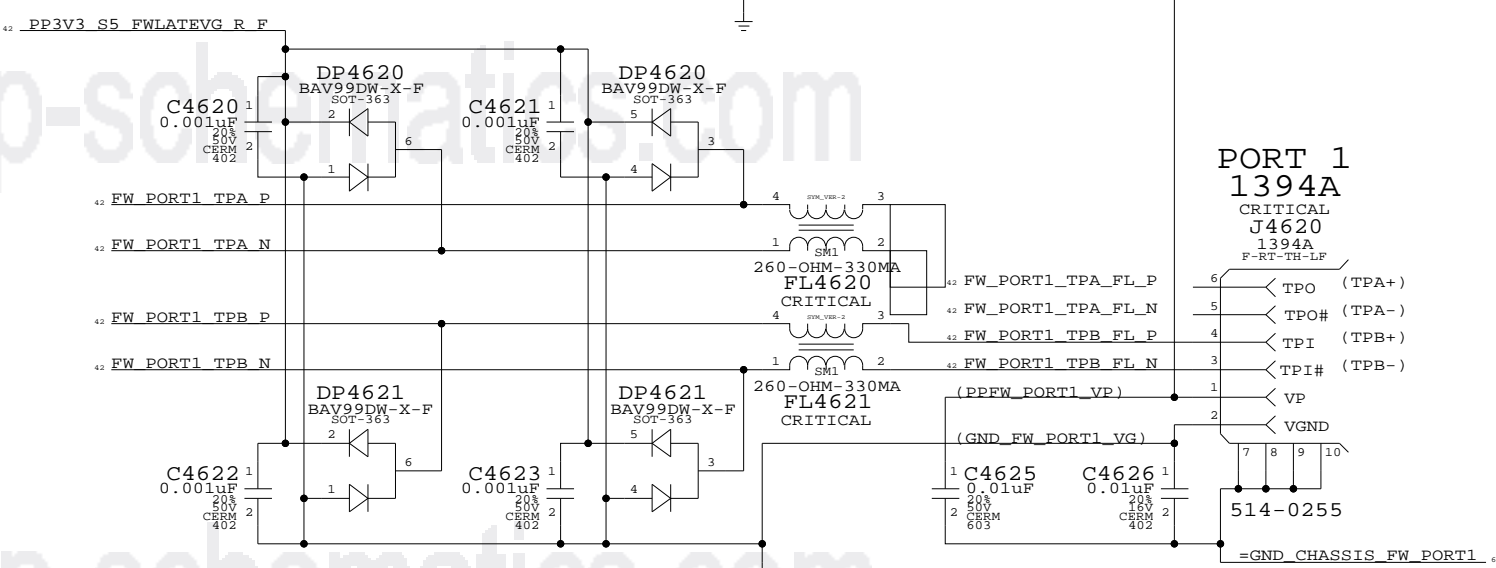
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

Termination

Place close to FireWire PHY



"Snapback" & "Late VG" Protection



PORT 1

1394A
CRITICAL
J4620
F-RT-TH-LF

6 TPO (TPA+)
5 TPO# (TPA-)
4 TPI (TPB+)
3 TPI# (TPB-)

1 VP
2 VGND

514-0255

=GND_CHASSIS_FW_PORT1

2nd TPA/TPB pair unused

FW_B TPBIAS = NC FW_B TPBIAS
MAKE_BASE=TRUE
NO_TEST=YES

FW_B TPA P = NC FW_B TPAP
MAKE_BASE=TRUE
NO_TEST=YES

FW_B TPA N = NC FW_B TPAN
MAKE_BASE=TRUE
NO_TEST=YES

FW_B TPB P = NC FW_B TPBP
MAKE_BASE=TRUE
NO_TEST=YES

FW_B TPB N = NC FW_B TPBN
MAKE_BASE=TRUE
NO_TEST=YES

3rd TPA/TPB pair unused

FW_C TPBIAS = NC FW_C TPBIAS
MAKE_BASE=TRUE
NO_TEST=YES

FW_C TPA P = NC FW_C TPAP
MAKE_BASE=TRUE
NO_TEST=YES

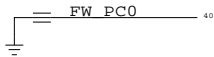
FW_C TPA N = NC FW_C TPAN
MAKE_BASE=TRUE
NO_TEST=YES

FW_C TPB P = NC FW_C TPBP
MAKE_BASE=TRUE
NO_TEST=YES

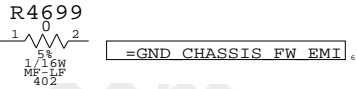
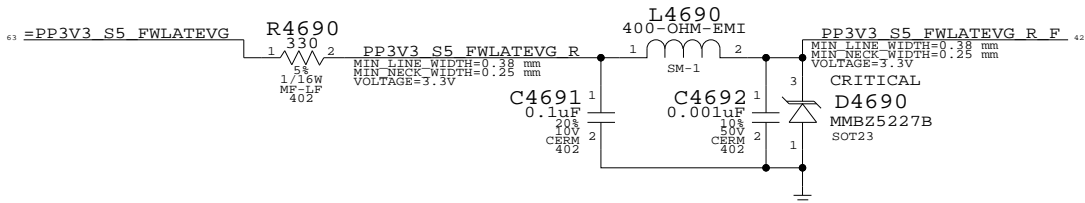
FW_C TPB N = NC FW_C TPBN
MAKE_BASE=TRUE
NO_TEST=YES

FW Power Class Strap

Single-port system sets PC=0



Late-VG Protection Power



FireWire Ports

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

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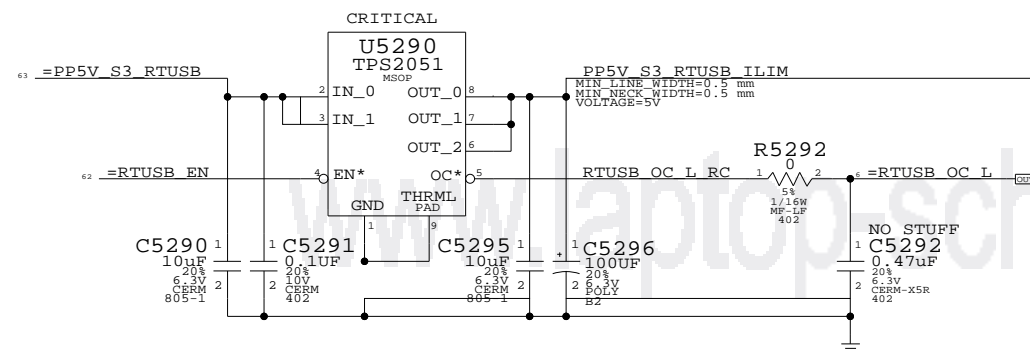


APPLE COMPUTER INC.

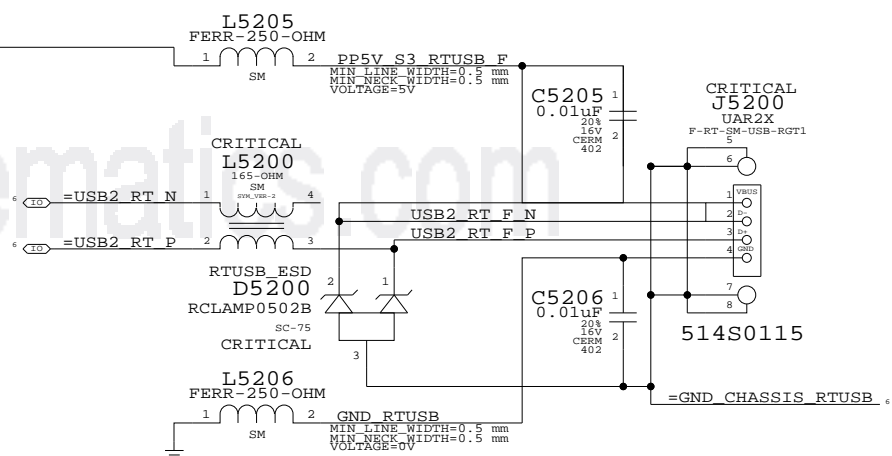
SIZE D DRAWING NUMBER 051-7076 REV. H

SCALE NONE SHT 46 OF 104

Port Power Switch



Right USB Port



Place L5200, L5205 and L5206 across moat

External USB Connector

SYNC_MASTER= (MASTER)	SYNC_DATE= (MASTER)
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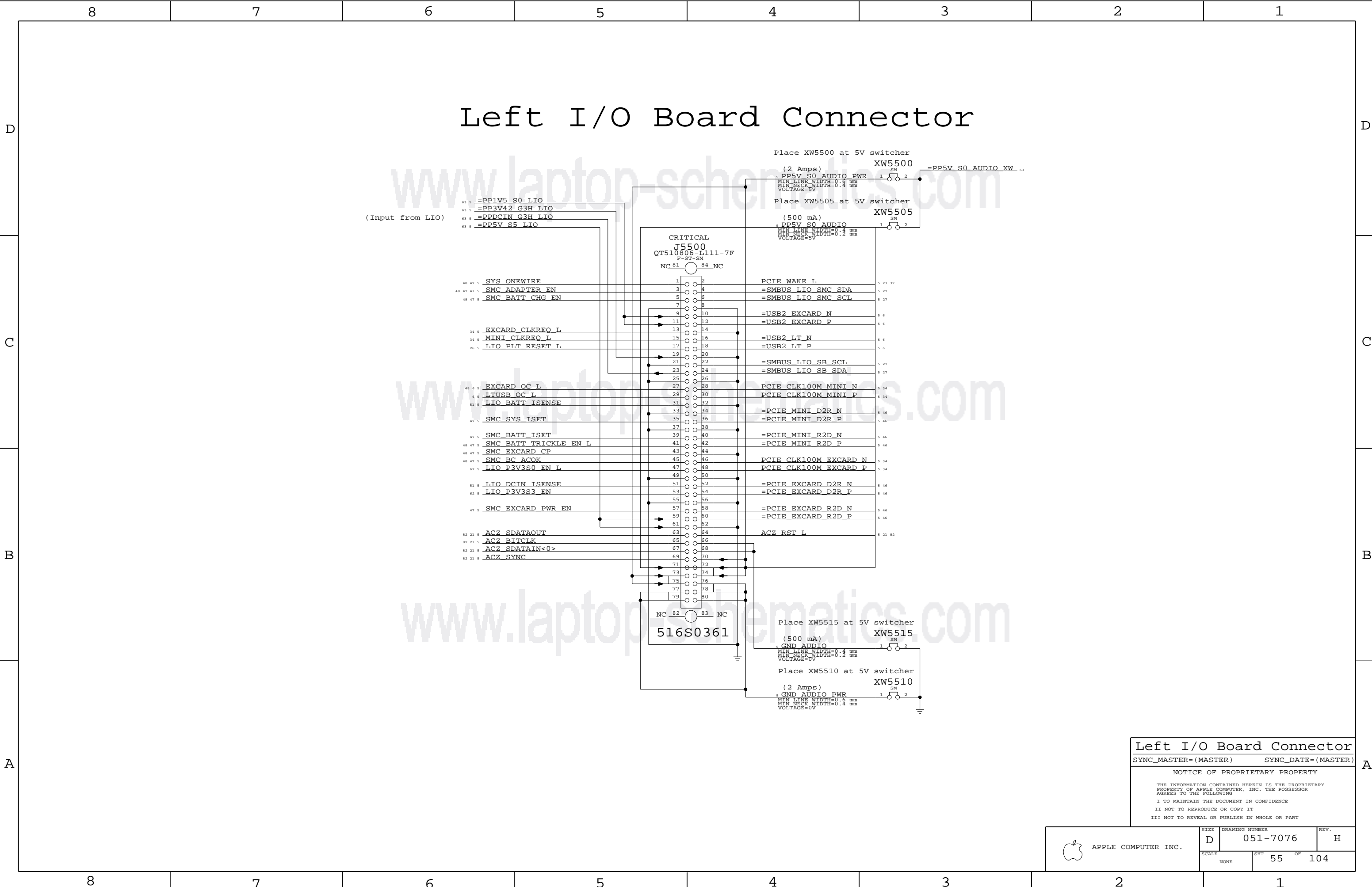
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SIZE	DRAWING NUMBER	REV
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SCALE	SHT	OF
NONE	52	104



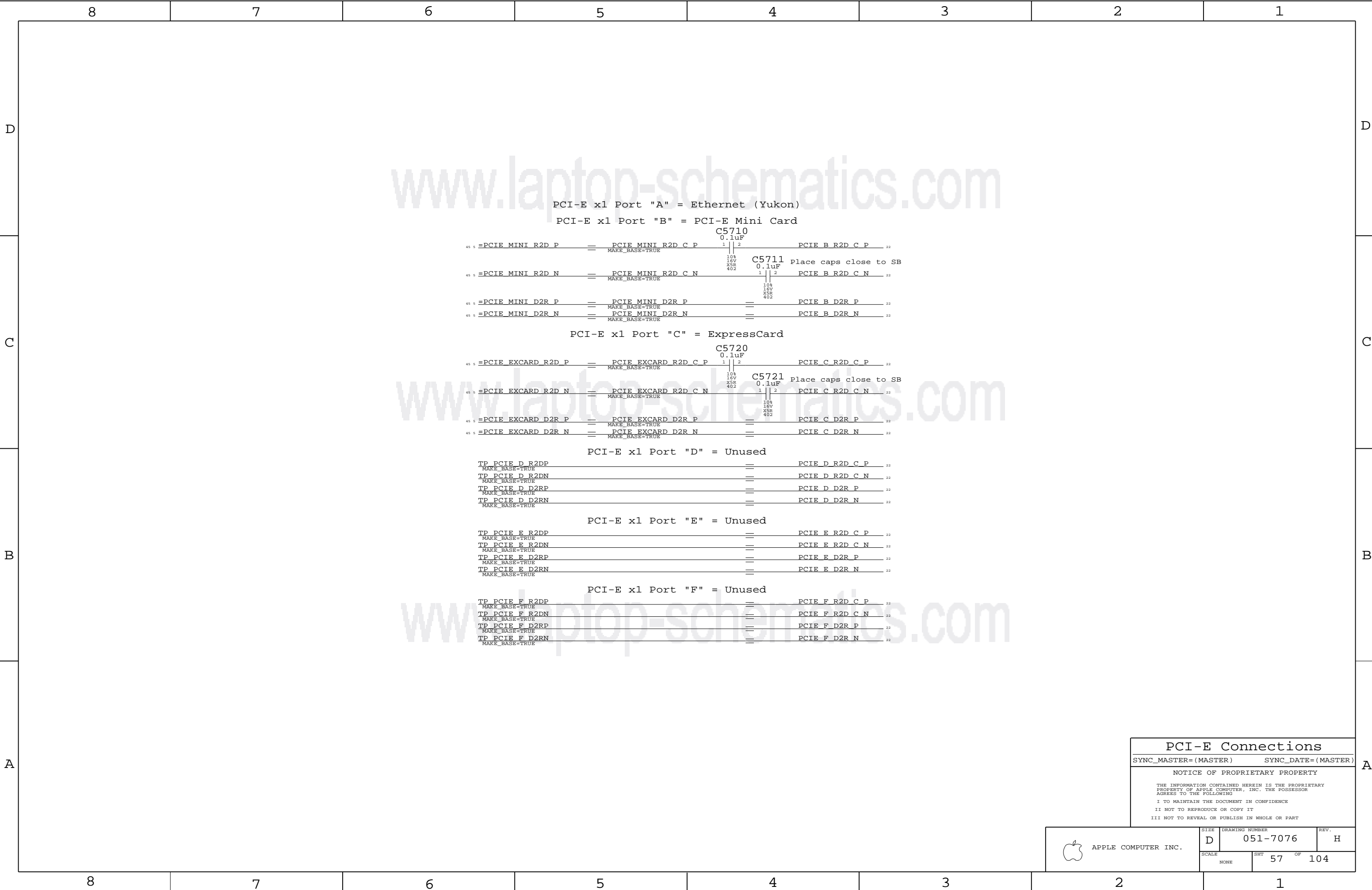
Left I/O Board Connector

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

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SCALE		SHT	OF
NONE		55	104



PCI-E Connections

SYNC_MASTER=(MASTER)

SYNC_DATE=(MASTER)


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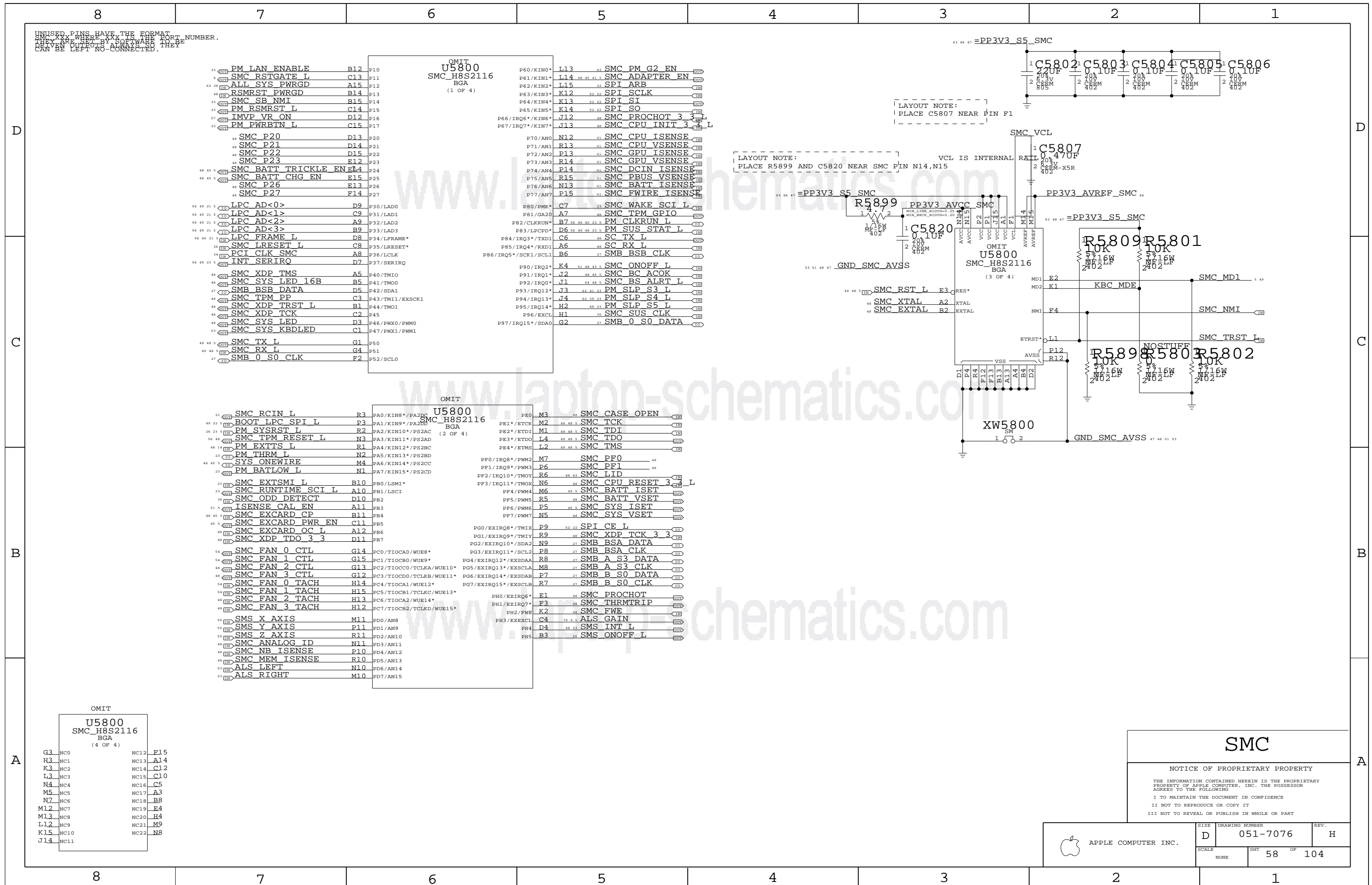
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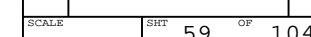
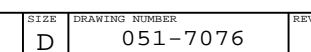
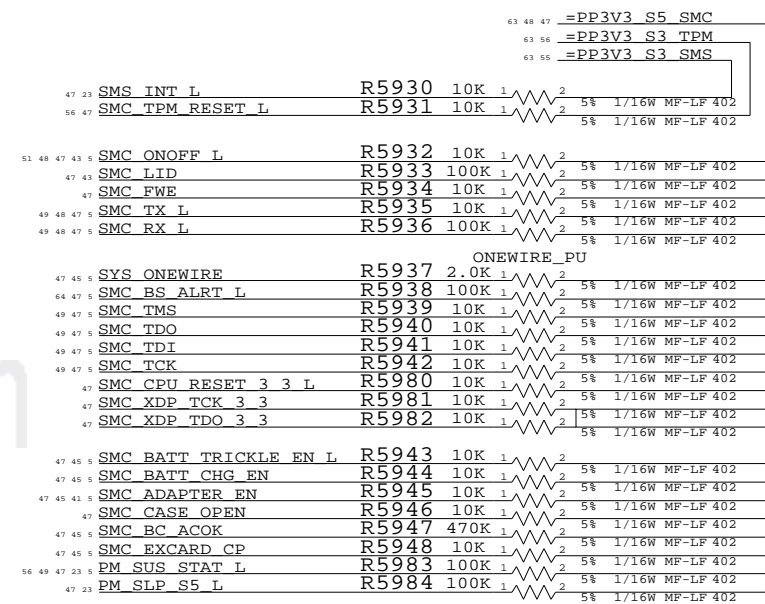
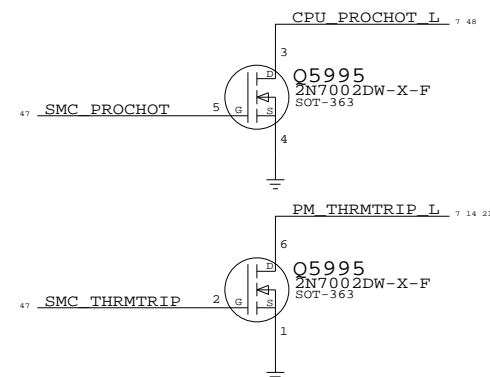
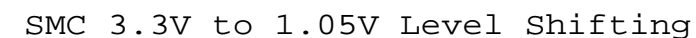
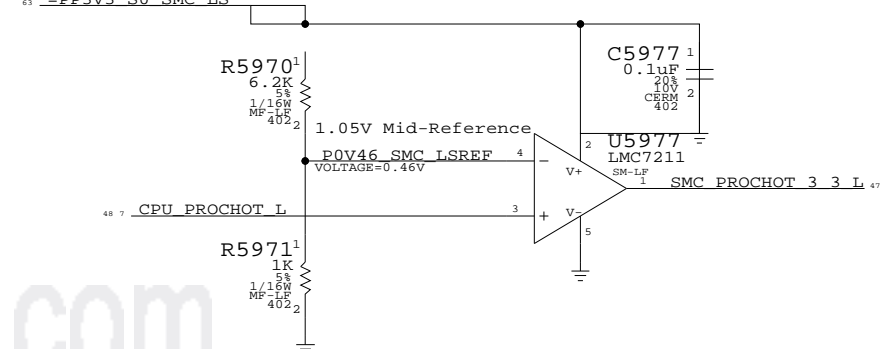
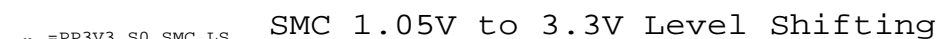
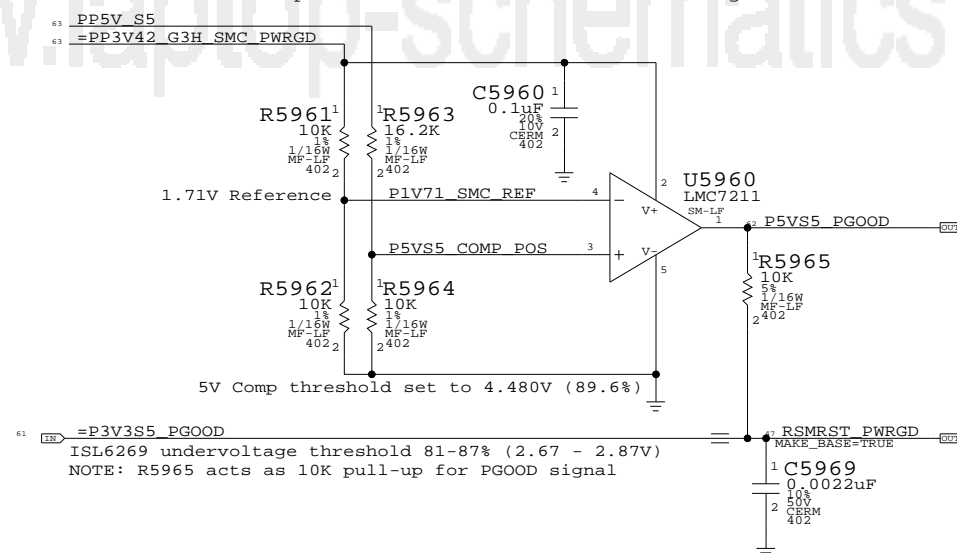
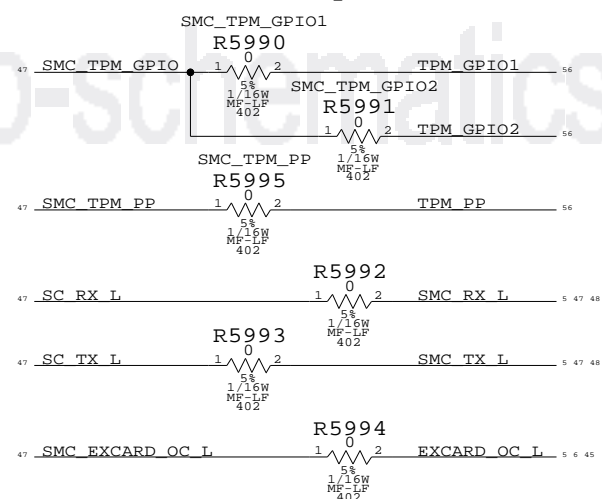
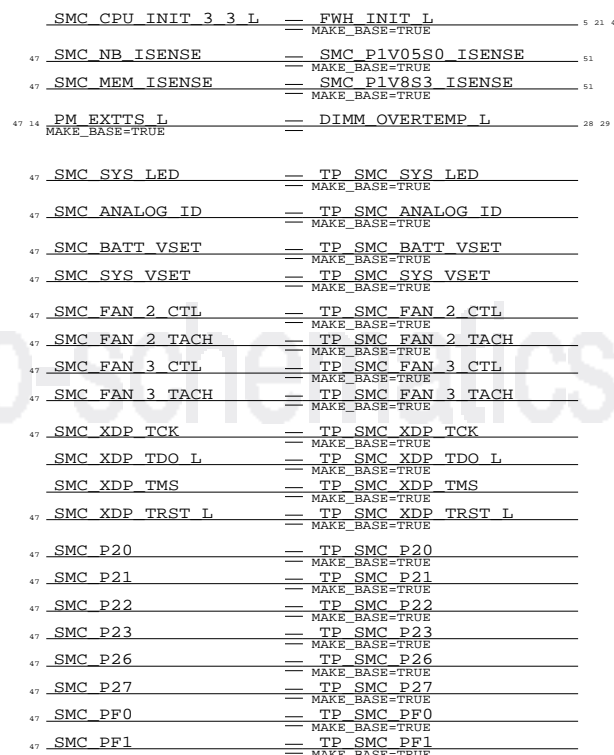
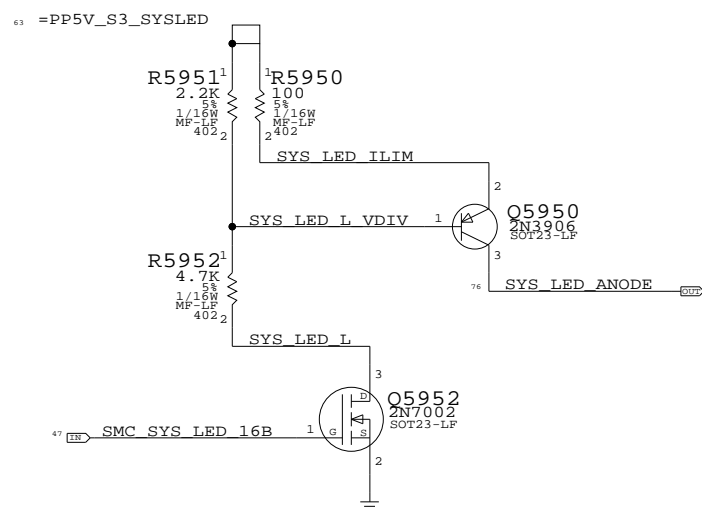
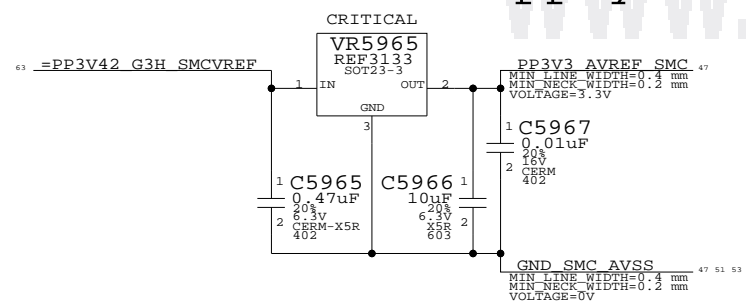
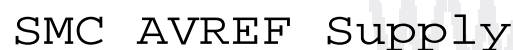
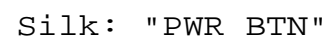
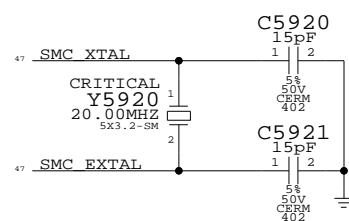
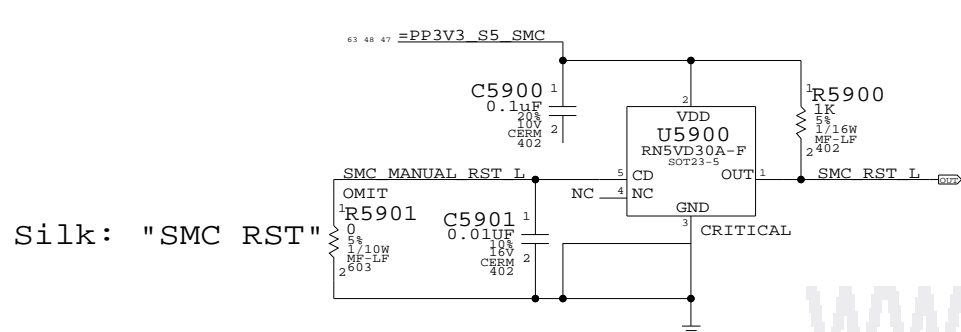
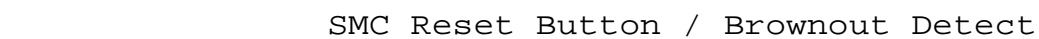
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	SCALE NONE	SHT 57	OF 104

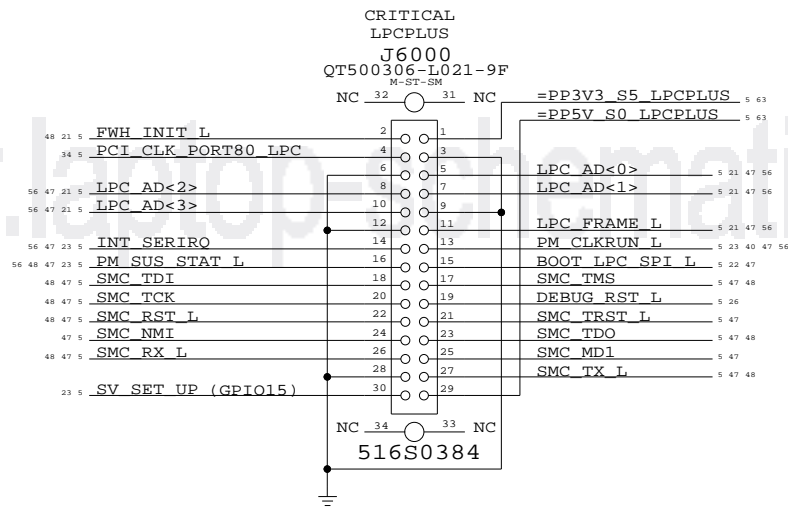




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LPC+ Debug Connector

SYNC_MASTER=M42

SYNC_DATE=07/20/2005


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	SCALE NONE	SHT 60	OF 104

[illegible]

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,0,1/16W,0402	C6120		HSTHMSNS_NO

CRITICAL

J6160
88460-0201
P=RT-204
20V

1 NC
2
4 NC

518S0226

RSFSTHMSNS D P
1 499
1 1/16W
MF 402

R6160
1 499
1 1/16W
MF 402

1 C6160
0.0001UF
2 40X
2 CERM
402

RSFSTHMSNS D R N
1 499
1 1/16W
MF 402

R6161
1 499
1 1/16W
MF 402

61 =PP3V3 S0 RSTHMSNS

C6150
0.1UF
1 10V
2 X55
402

1
2

U6150
ADT7461
MSOP
CRITICAL

VDD
1
2 D+
3 D-
4 THM+
5 GND
6
7
8
9

ALERT*/THM2*
THM+
SCLK
SDATA

RSTHMSNS ALERT L
RSTHMSNS THM L
SMBUS RSTHMSNS SCL
SMBUS RSTHMSNS SDA

R6151
10K
1 1/16W
MF 402

R6152
10K
1 1/16W
MF 402

1
2

Placement note:
Place U6150 below and to the left of the speaker hole.

Placement note:
Place near CPU center

CPUTHMSNS DIO P 1 0 2 THRM CPU DX P 10

CPUTHMSNS DIO N 1 0 2 THRM CPU DX N 10

CPUTHM_DIODE R6190

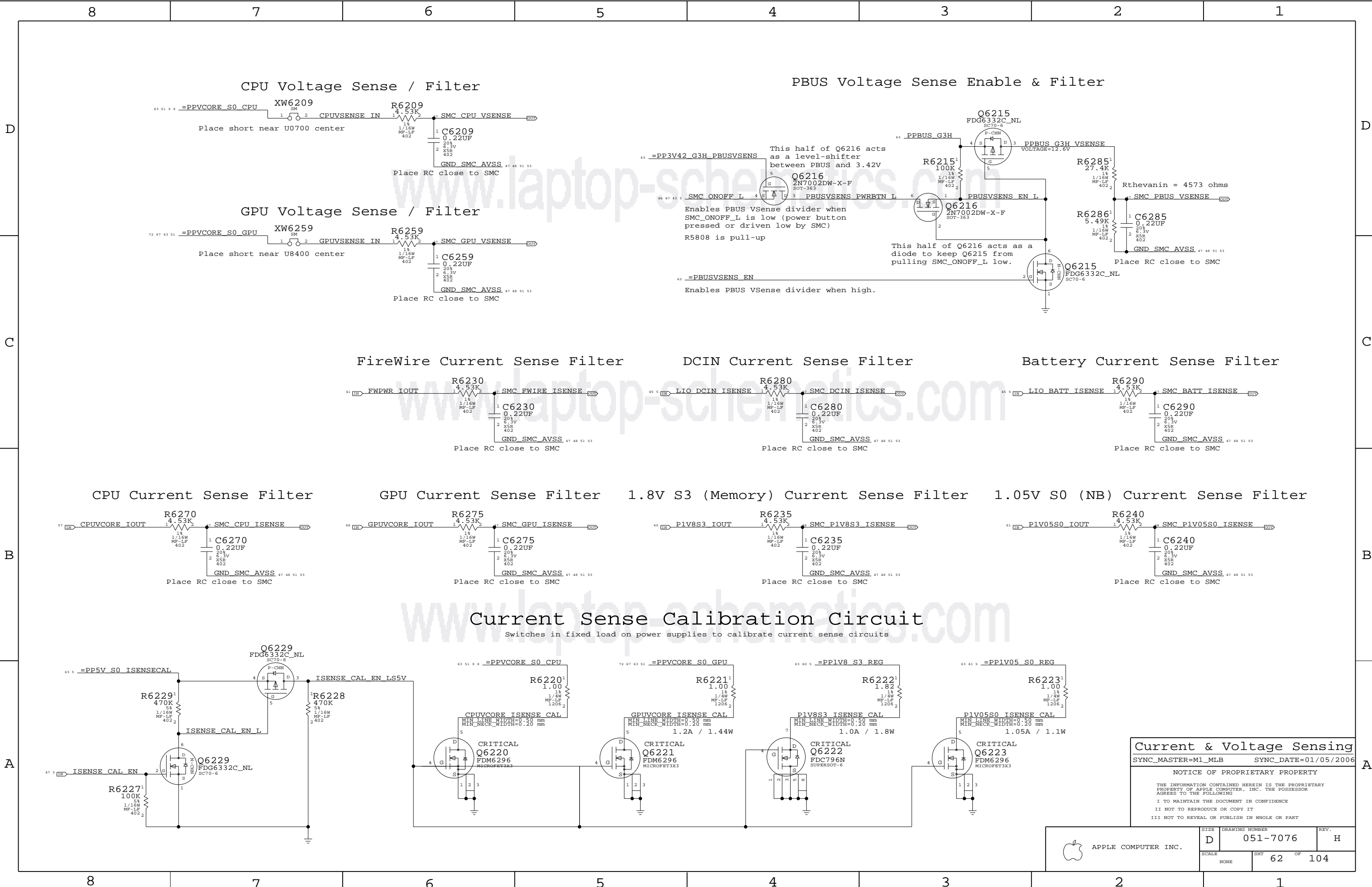
CPUTHM_DIODE R6191

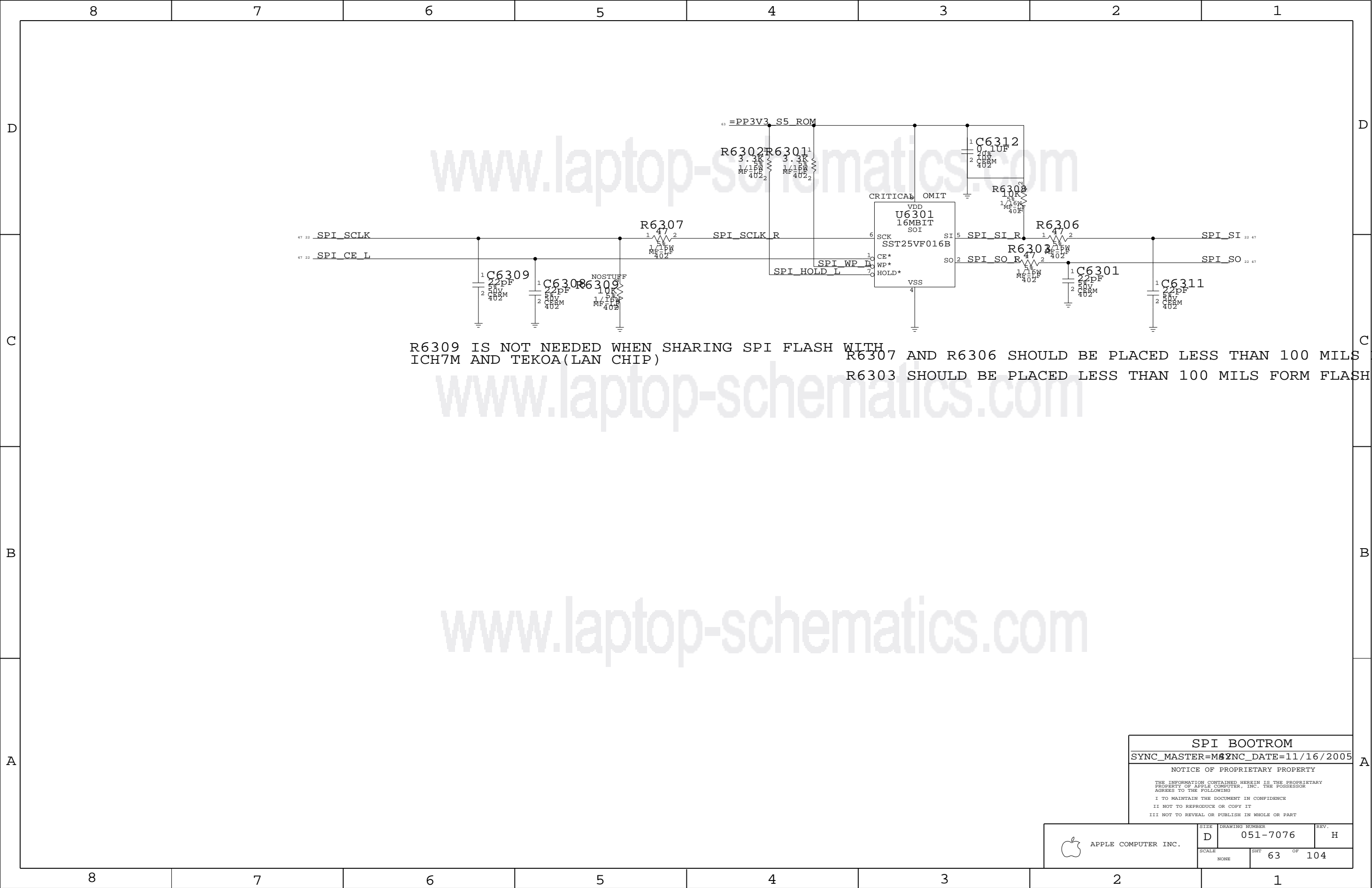
Q6190 2N3904LF SOT23

Layout note:
Minimize stubs between these R's and R1001 & R1002

R1001 / R1002 are not currently BOMOPTIONEd. Can not programatically unstuff those parts to stuff these.

<h1>Thermal Sensors</h1>	
<code>SYNC_MASTER=(MASTER)</code>	<code>SYNC_DATE=(MASTER)</code>
<p>NOTICE OF PROPRIETARY PROPERTY</p> <p>THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</p> <ul style="list-style-type: none">I TO MAINTAIN THE DOCUMENT IN CONFIDENCEII NOT TO REPRODUCE OR COPY ITIII NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	





R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)
R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M
R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

SPI BOOTROM

SYNC_MASTER=MSYNC_DATE=11/16/2005

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	D	051-7076	H
	SCALE	SHT	OF
	NONE	63	104

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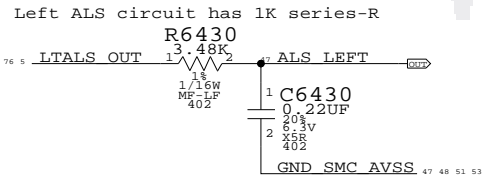
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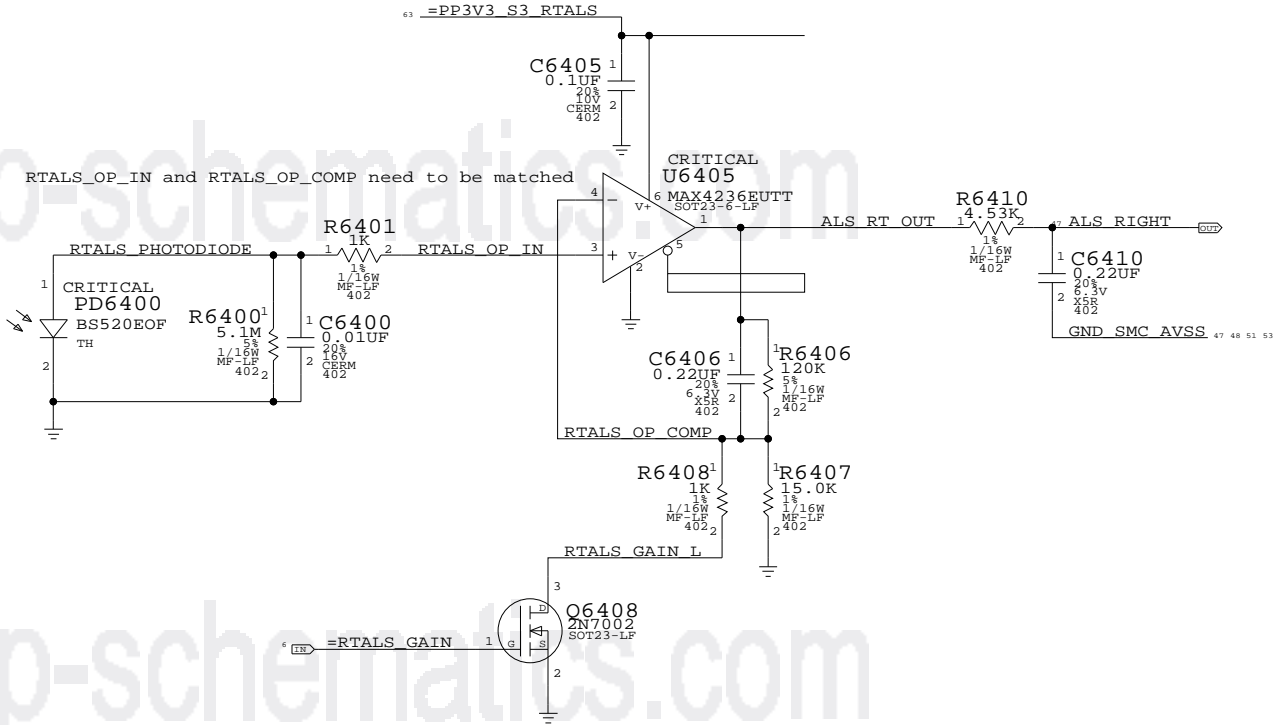
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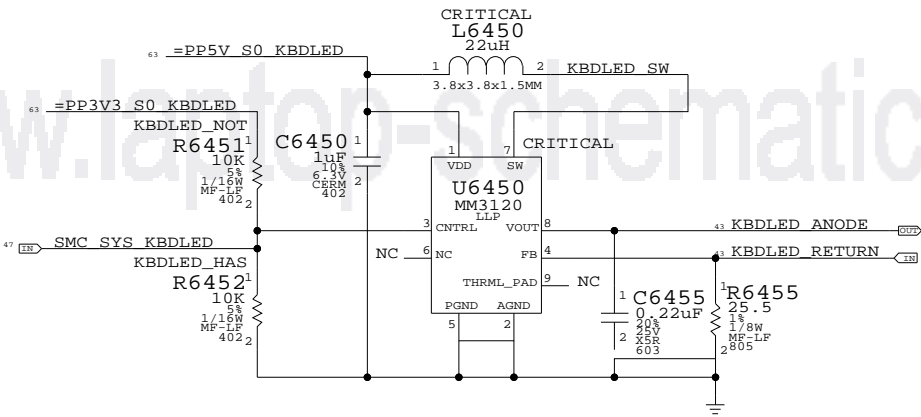
Left ALS Filter



Right ALS Circuit



Keyboard LED Driver



ALS Support

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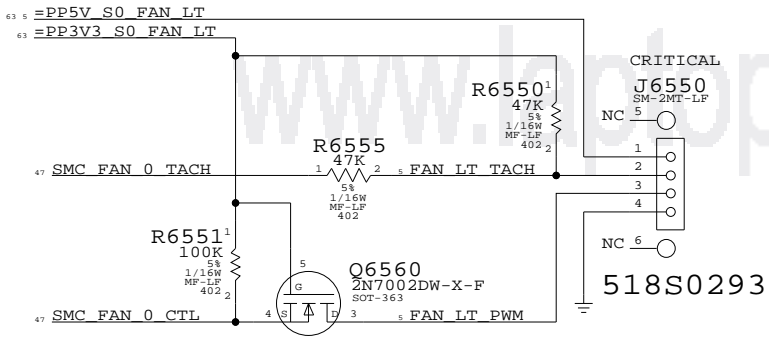
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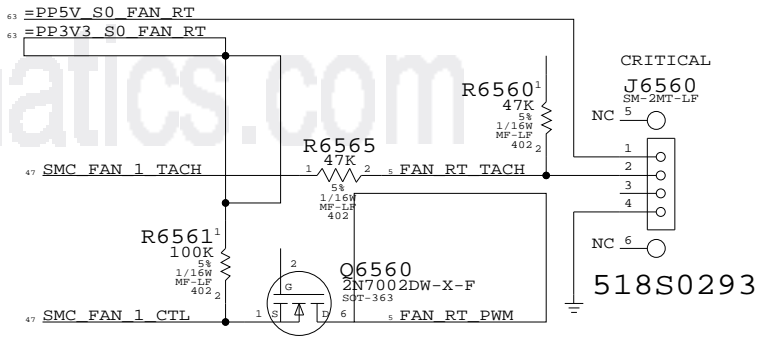
SCALE NONE SHT 64 OF 104

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Left Fan



Right Fan



Fan Connectors

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

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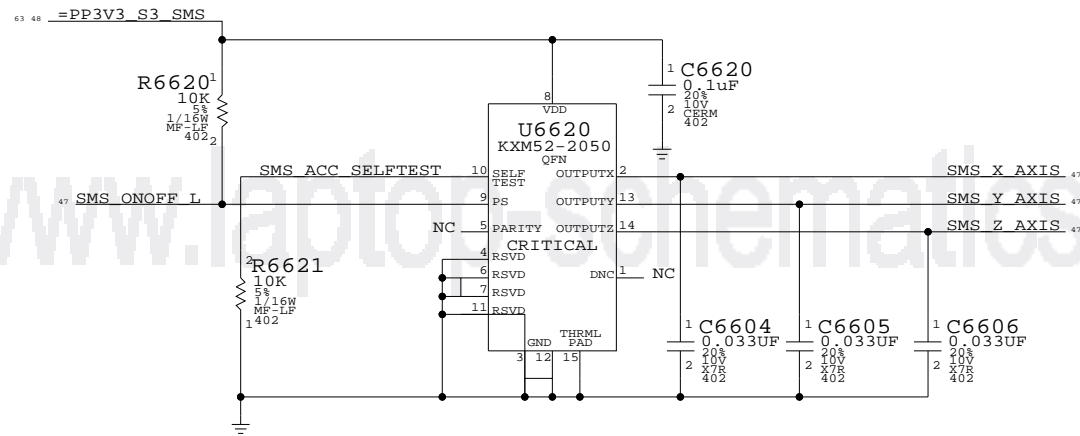
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SCALE	SHT	OF
NONE	65	104

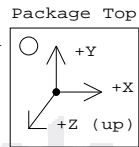
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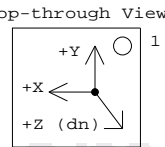
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Desired orientation when placed on board top-side:



Desired orientation when placed on board bottom-side:



M1 placement: Bottom-side

Sudden Motion Sensor (SMS)

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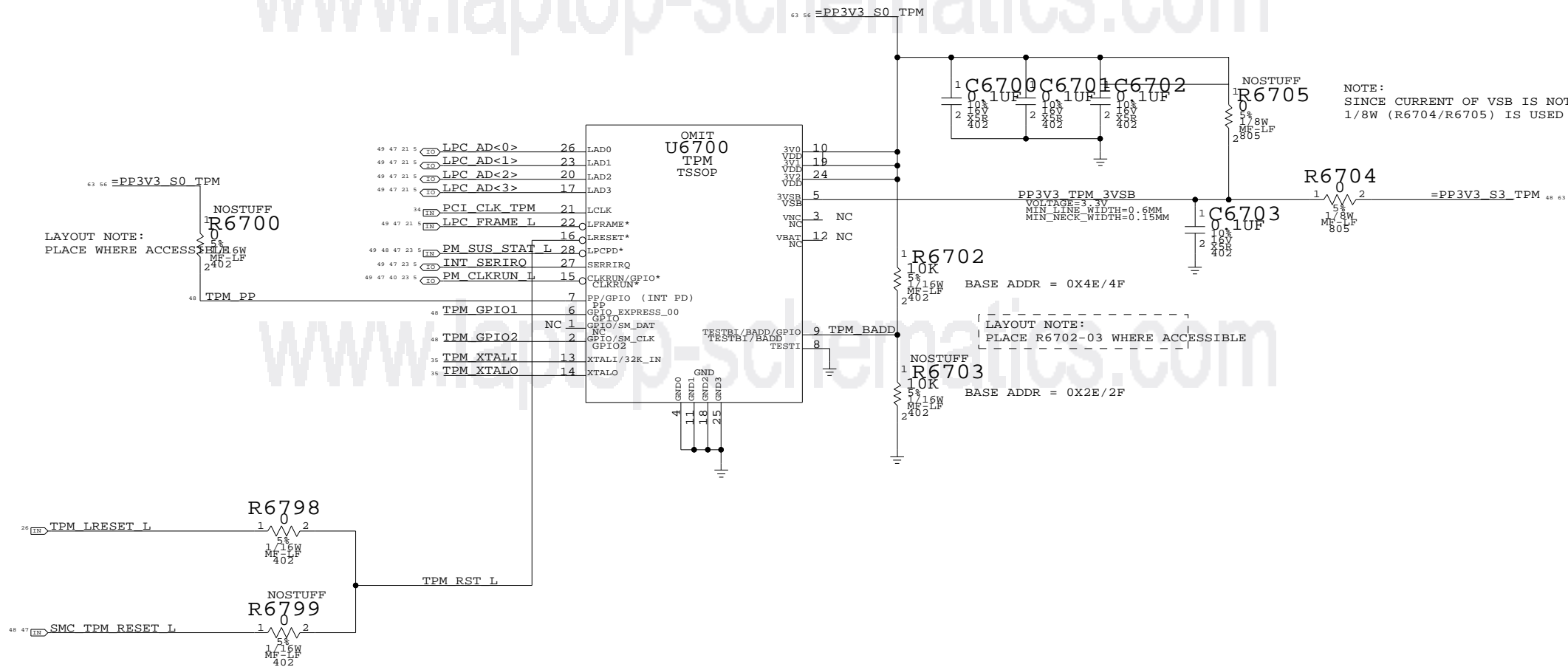
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TPM	
SYNC_MASTER=M38	SYNC_DATE=11/16/2005
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	SCALE NONE	SHT 67	OF 104



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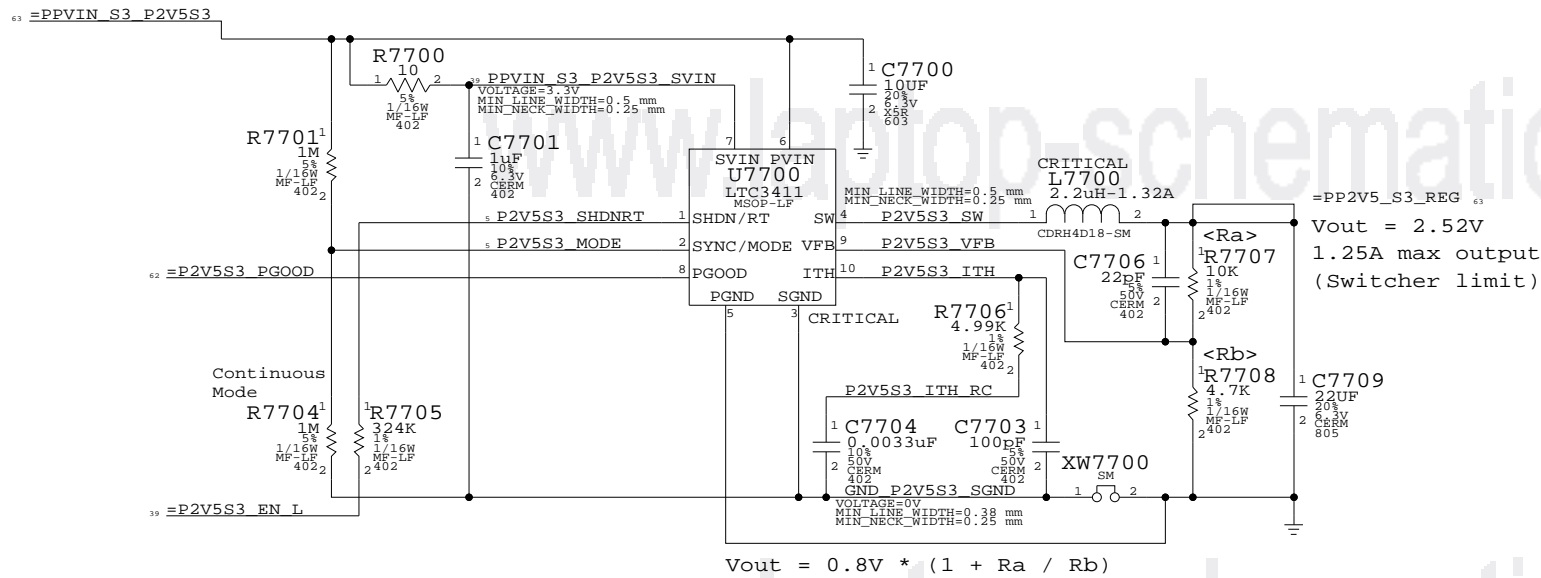
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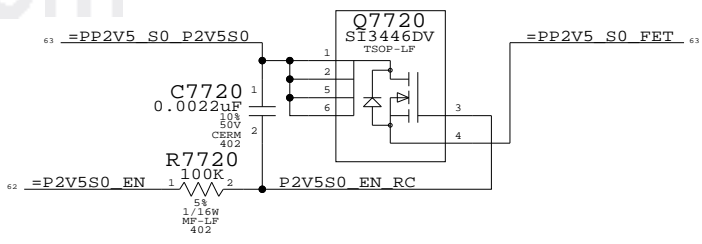
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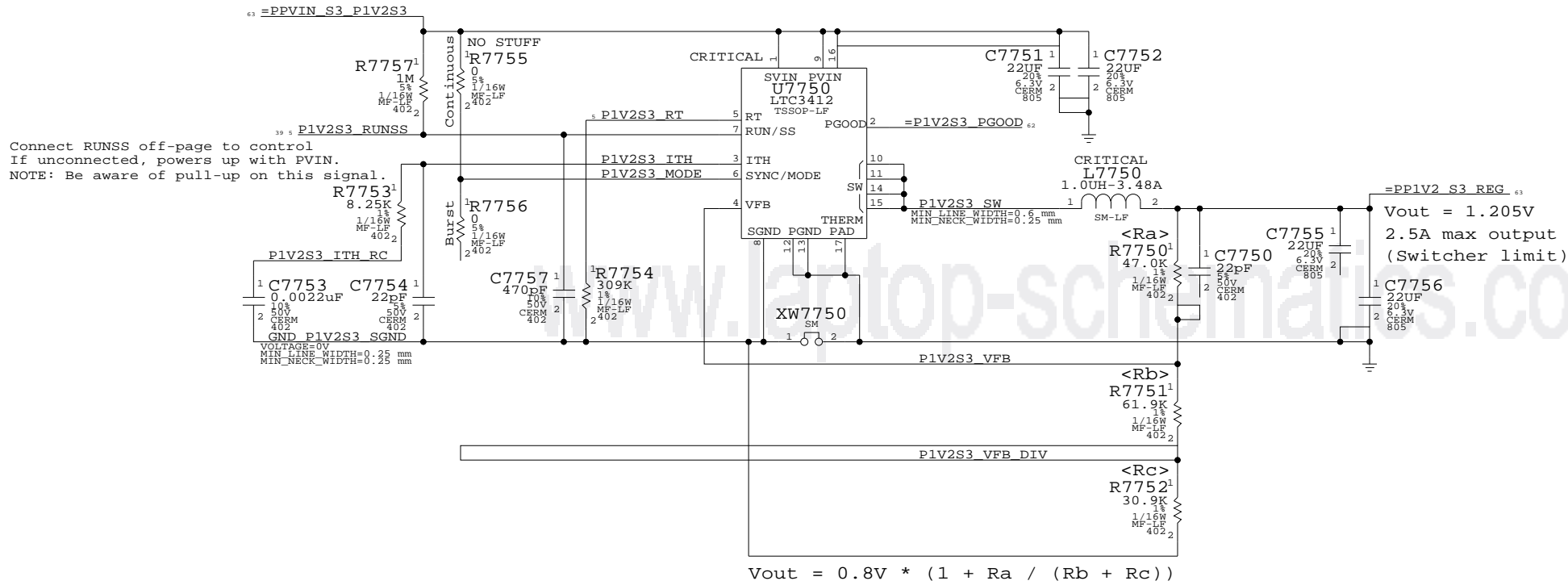
2.5V S3 Regulator



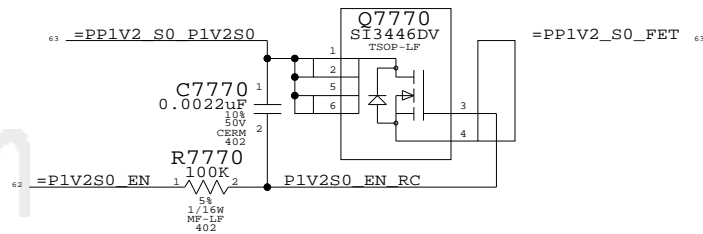
2.5V S0 FET



1.2V S3 Regulator



1.2V S0 FET



2.5V & 1.2V Regulators

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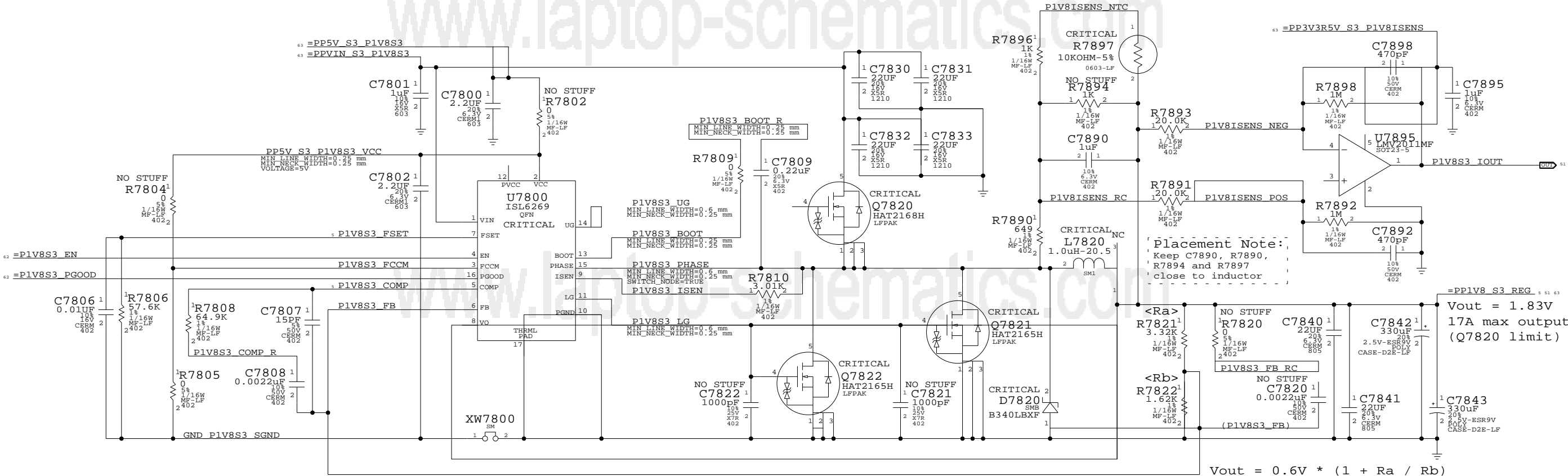
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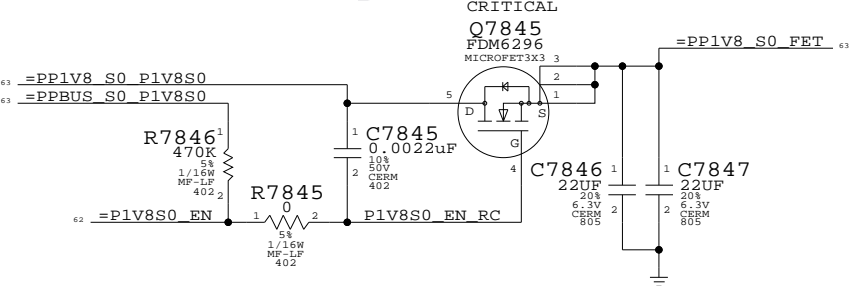
A

8 7 6 5 4 3 2 1

1.8V S3 Current Sense



1.8V S0 FET



1.8V Supply

SYNC_MASTER=M1_MLB SYNC_DATE=01/05/2006

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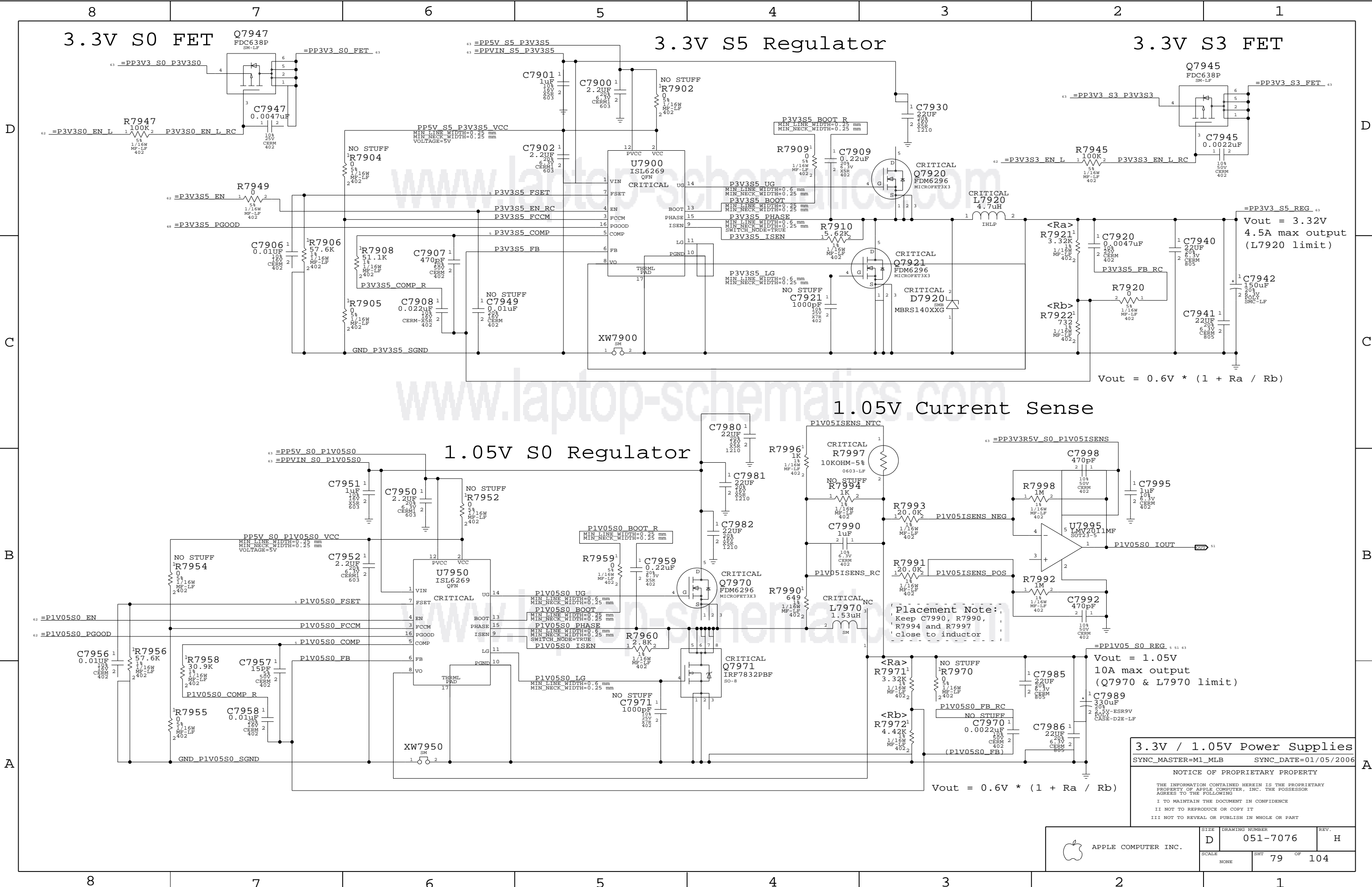
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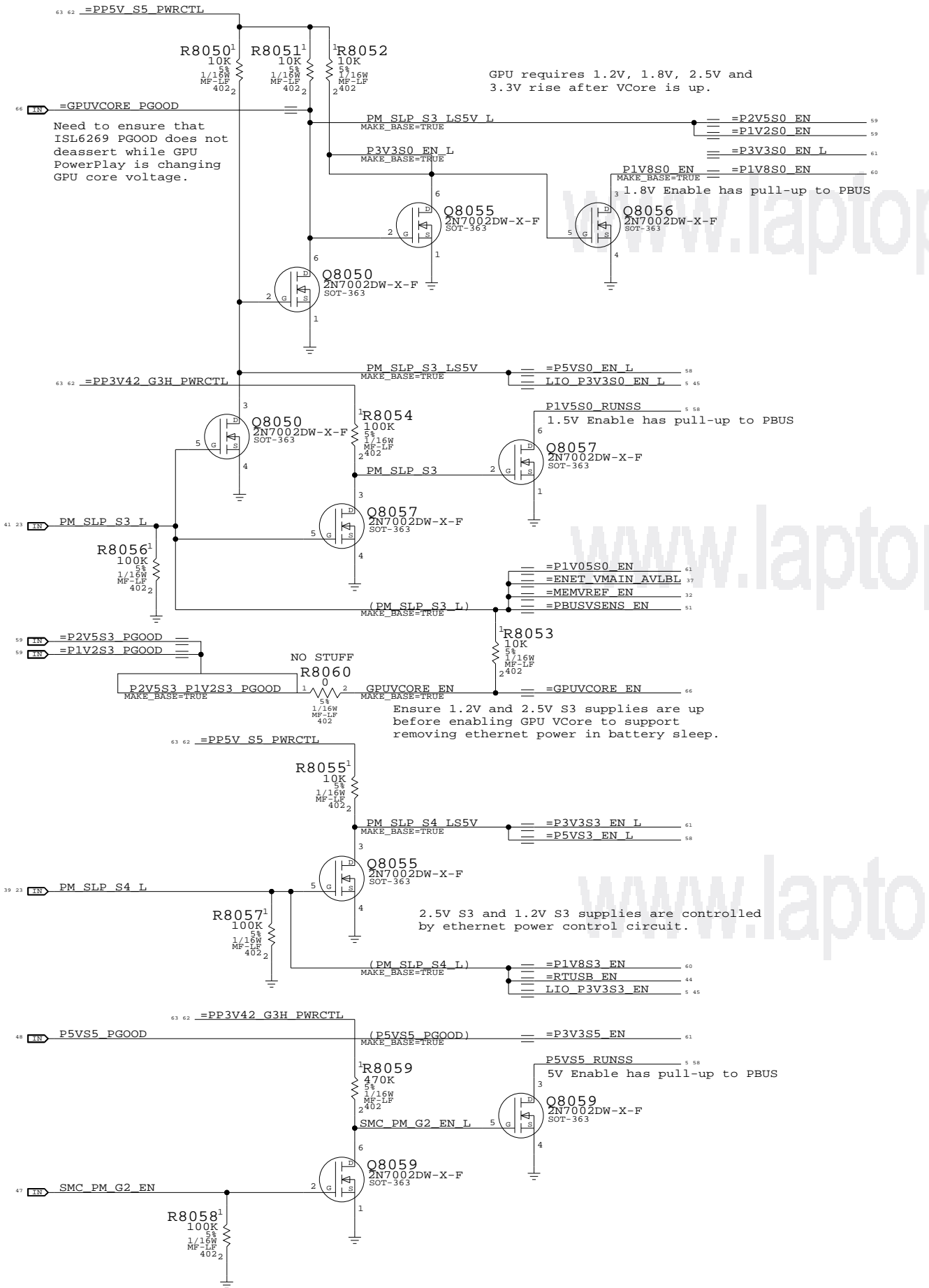
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	D	051-7076	H
SCALE		SHT	OF
NONE		78	104

8 7 6 5 4 3 2 1



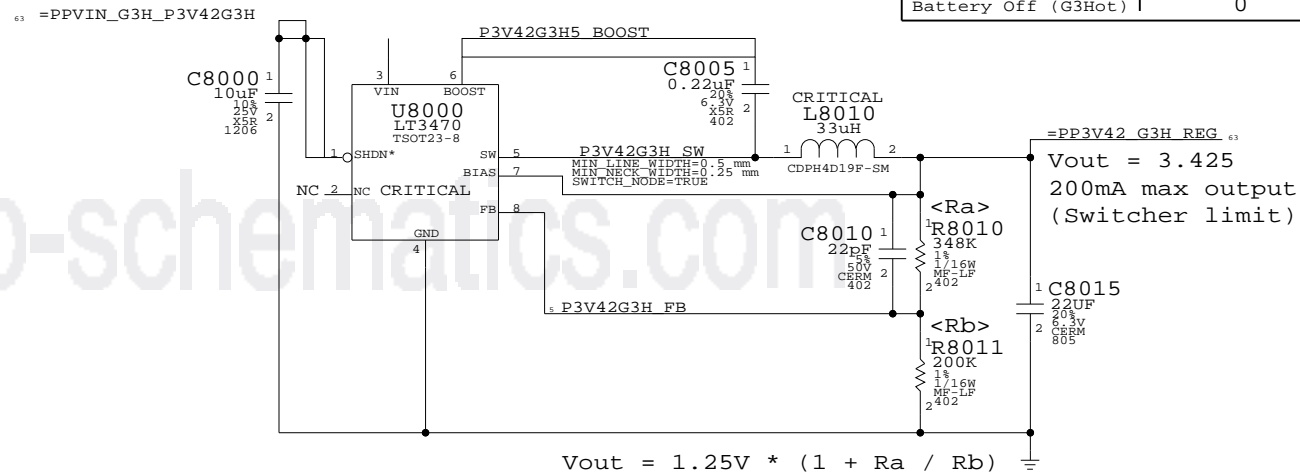
Power Control Signals



3.425V "G3Hot" Supply

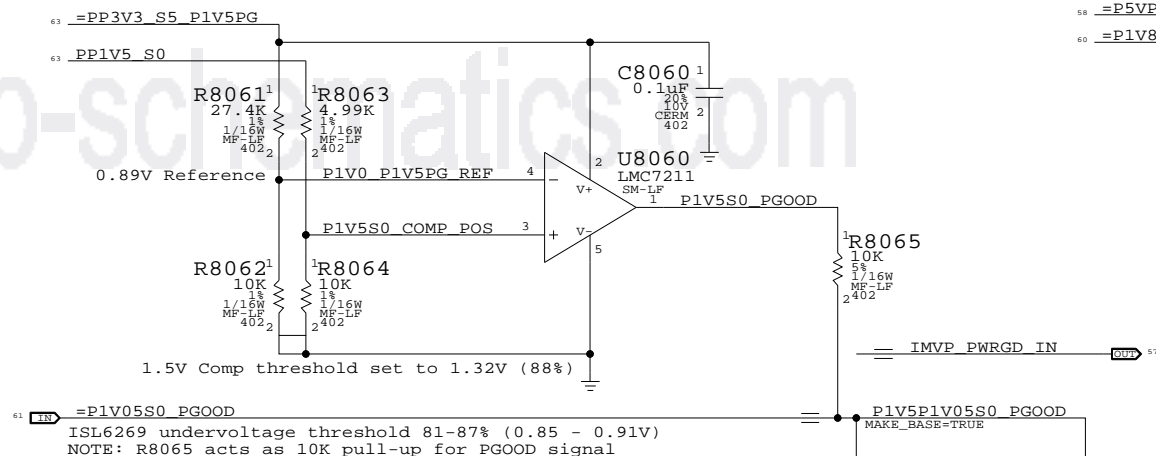
Supply needs to guarantee 3.31V delivered to SMC VRef generator

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0



1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation



Unused PGOOD Signals

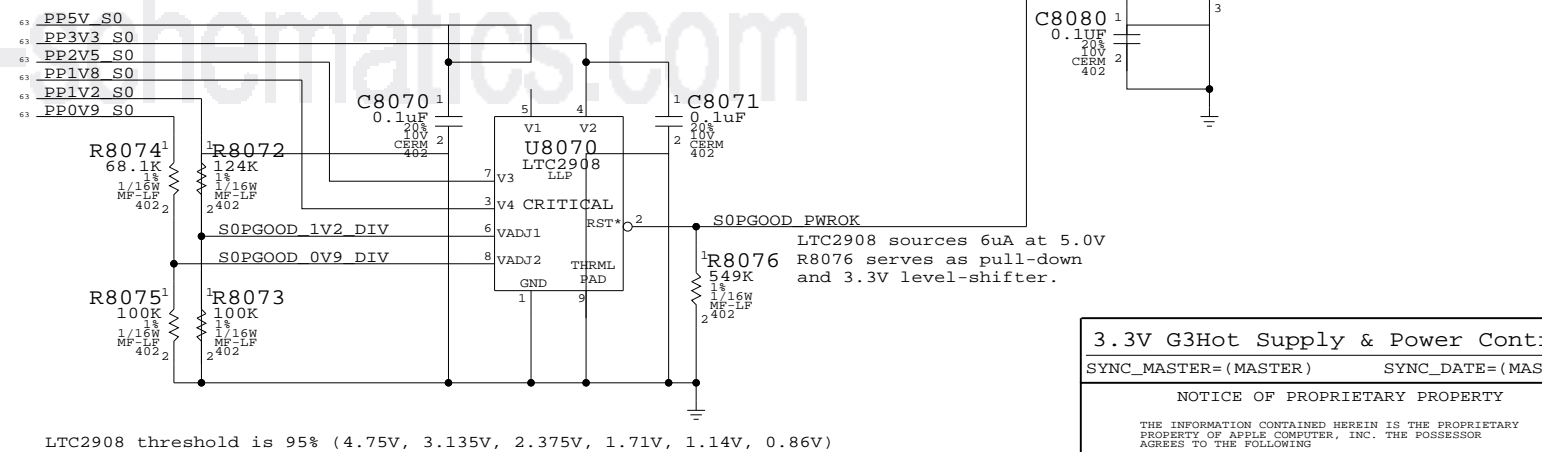
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58  =P5VP1V5 PGOOD      = TP P5V P1V5 PGOOD
                             MAKE_BASE=TRUE
60  =P1V8S3 PGOOD      = TP P1V8S3 PGOOD
                             MAKE_BASE=TRUE

```

Other S0 Rails PWRGD Circuit

Reports when 5V S0, 3.3V S0, 2.5V S0, 1.8V S0, 1.2V S0 and 0.9V S0 are in regulation



3.3V G3Hot Supply & Power Control	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)

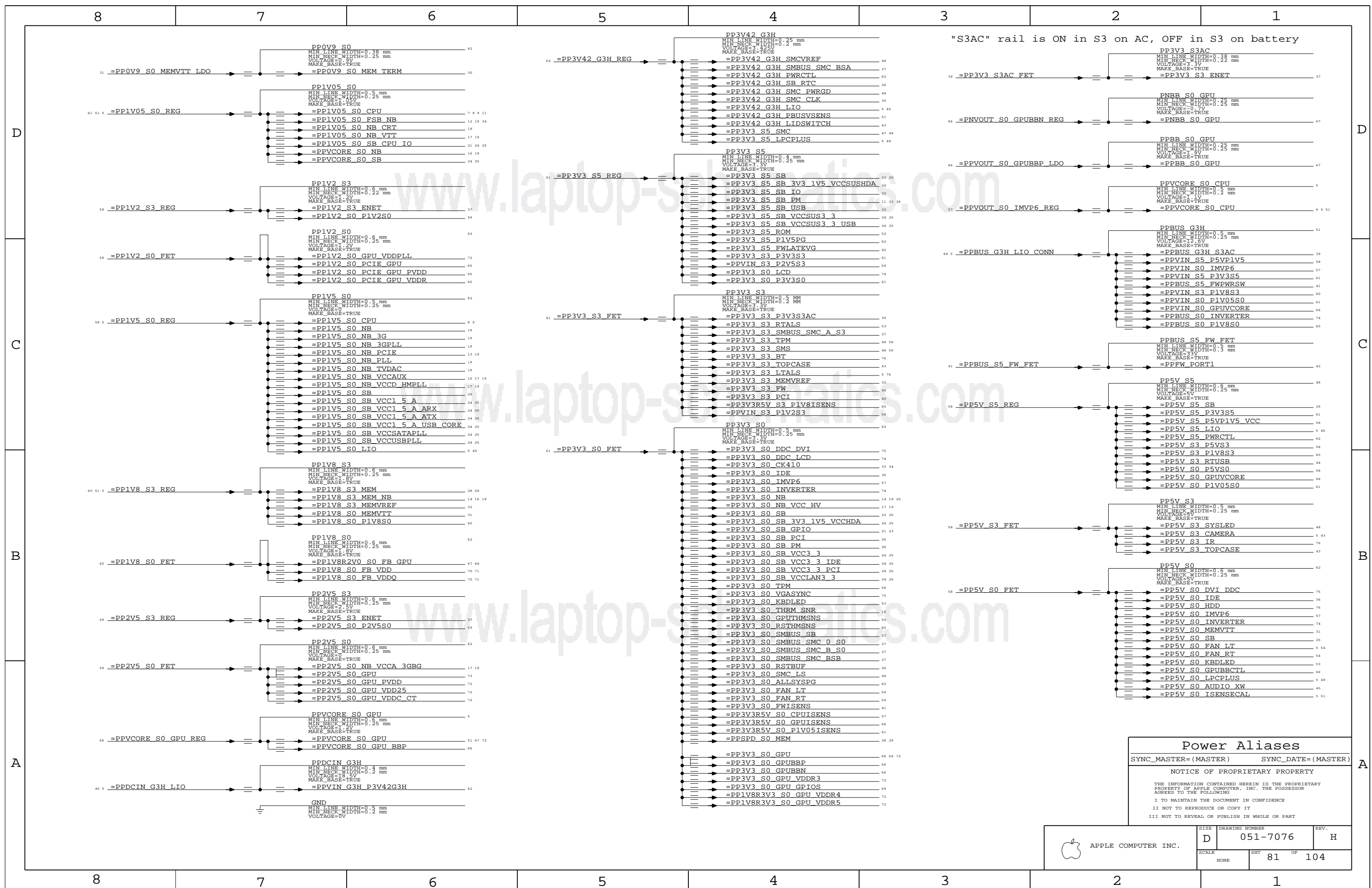
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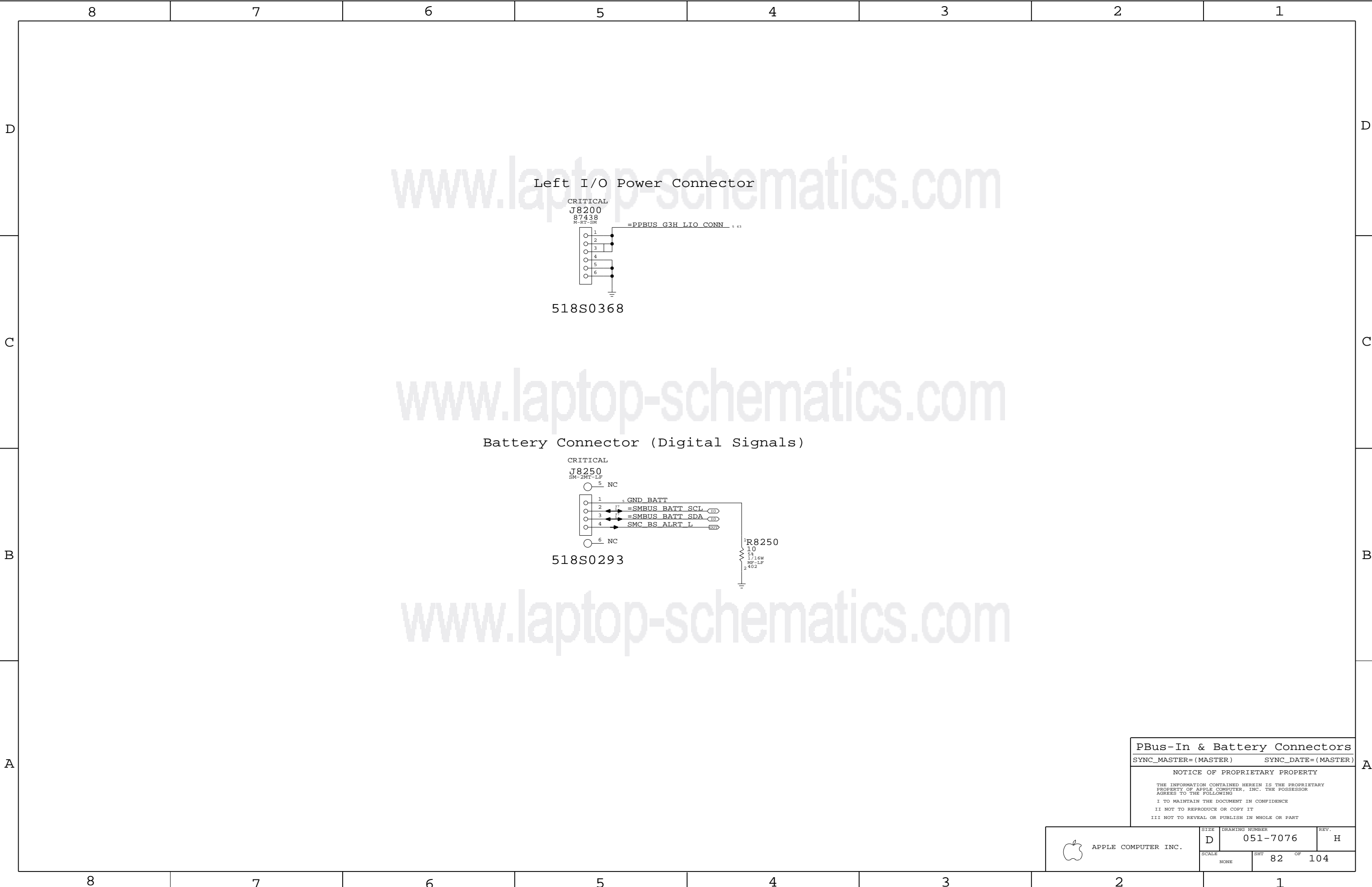
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PBus-In & Battery Connectors

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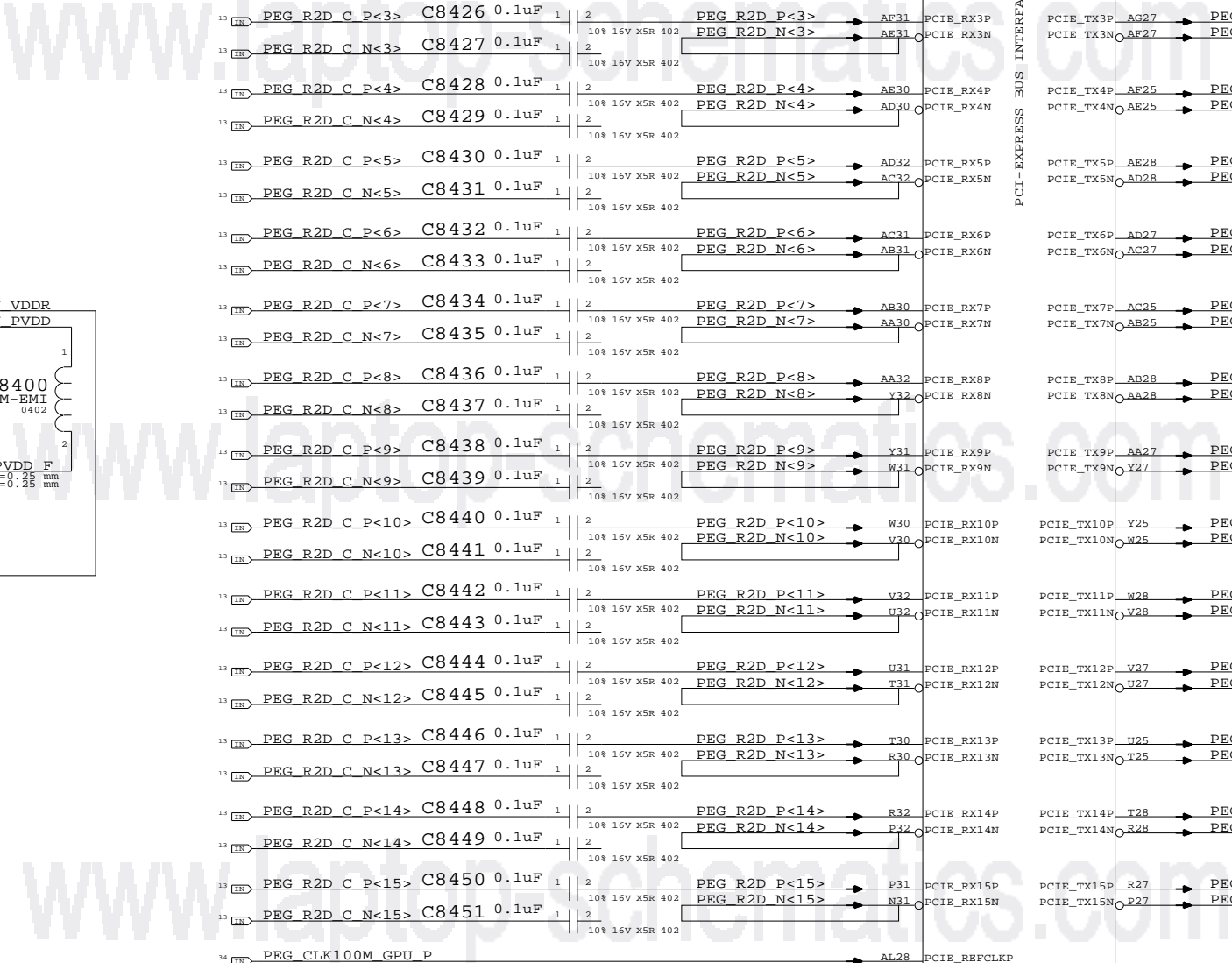
II NOT TO REPRODUCE OR COPY IT

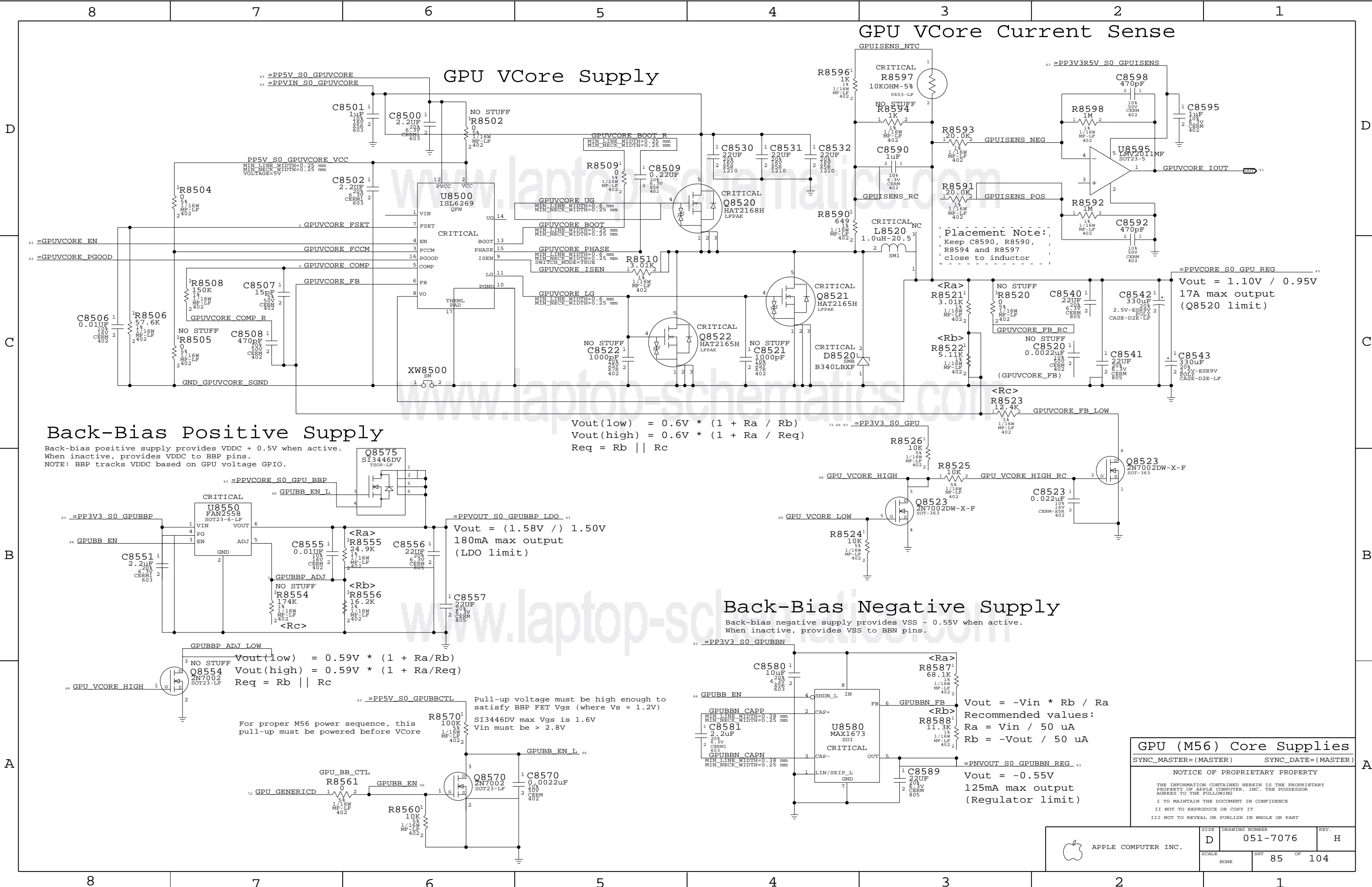
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SIZE	DRAWING NUMBER	REV.
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Back-Bias Positive Supply

Back-bias positive supply provides VDDC + 0.5V when active. When inactive, provides VDDC to BBP pins.
NOTE: BBP tracks VDDC based on GPU voltage GPIO.

$$V_{out}(low) = 0.6V * (1 + R_a / R_b)$$
$$V_{out}(high) = 0.6V * (1 + R_a / R_{eq})$$
$$R_{eq} = R_b || R_c$$

Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.55V when active. When inactive, provides VSS to BEN pins.

$$V_{out} = -V_{in} * R_b / R_a$$

Recommended values:
 $R_a = V_{in} / 50 \mu A$
 $R_b = -V_{out} / 50 \mu A$

GPU (M56) Core Supplies

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE D DRAWING NUMBER 051-7076 REV. H

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Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Core Power

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

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Page Notes

Power aliases required by this page:
- =PPIV8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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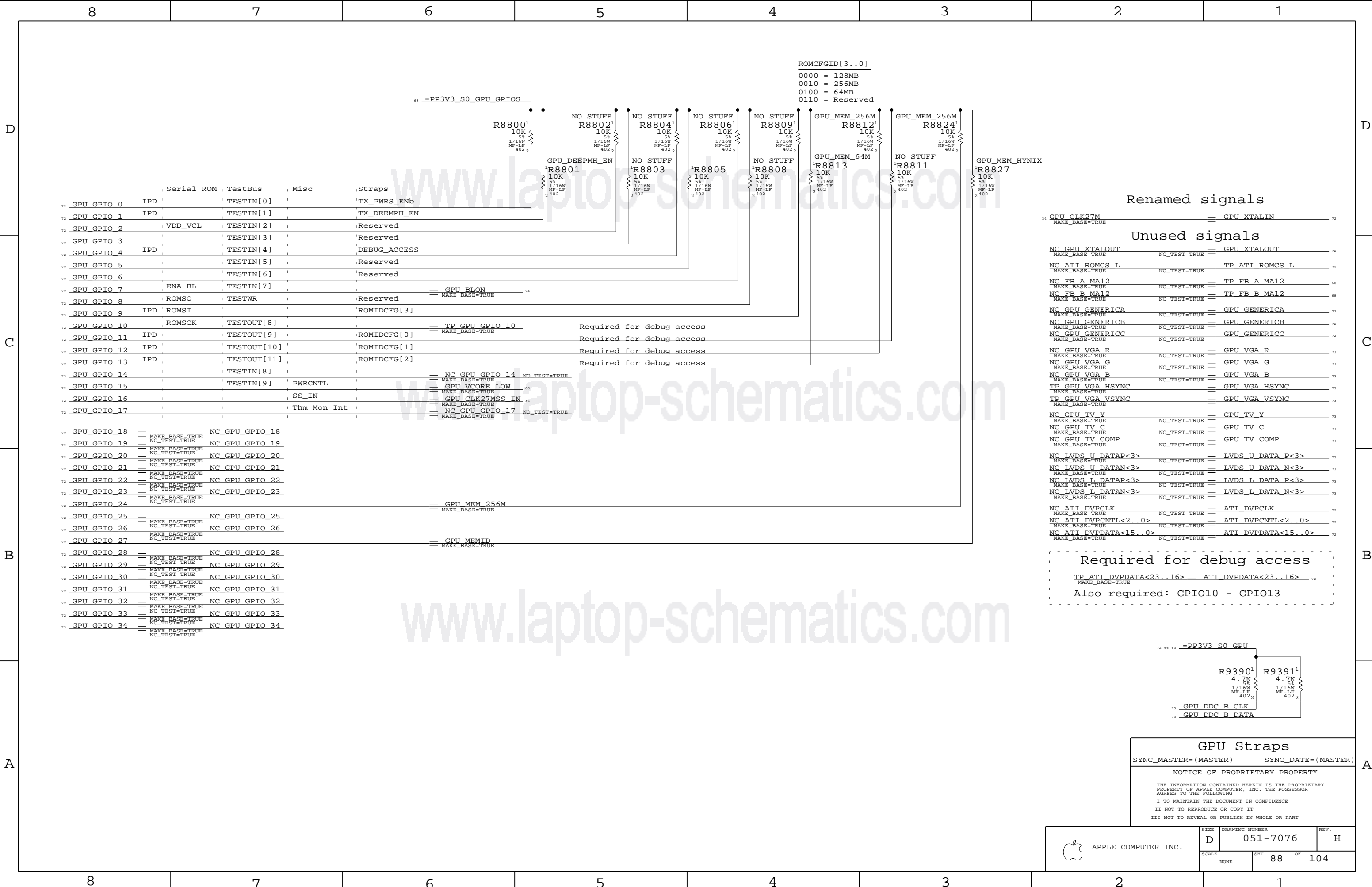


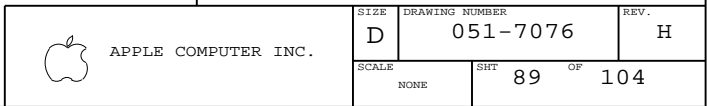
APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-7076

REV. H

SCALE NONE SHT 87 OF 104





Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

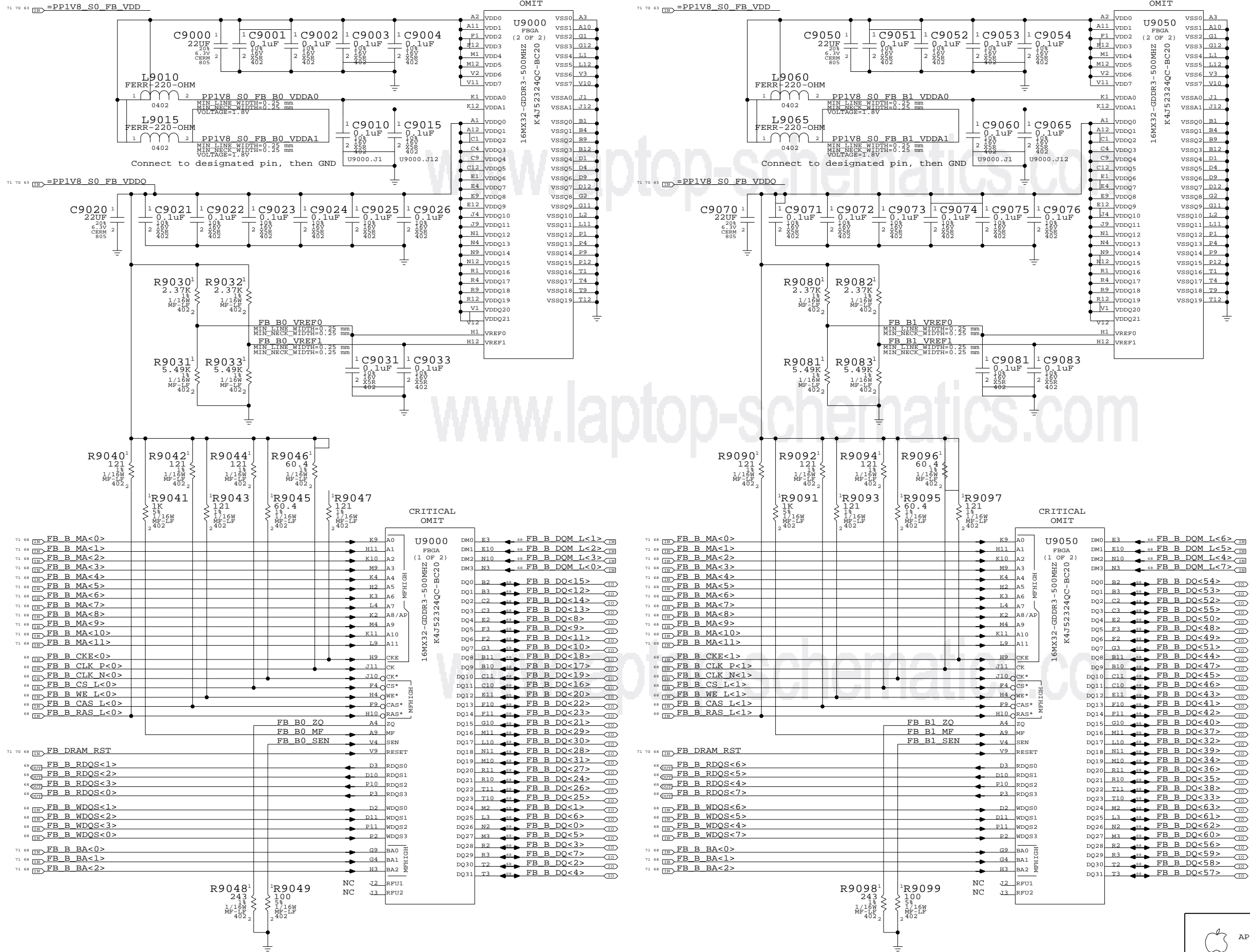
NOTICE OF PROPRIETARY PROPERTY

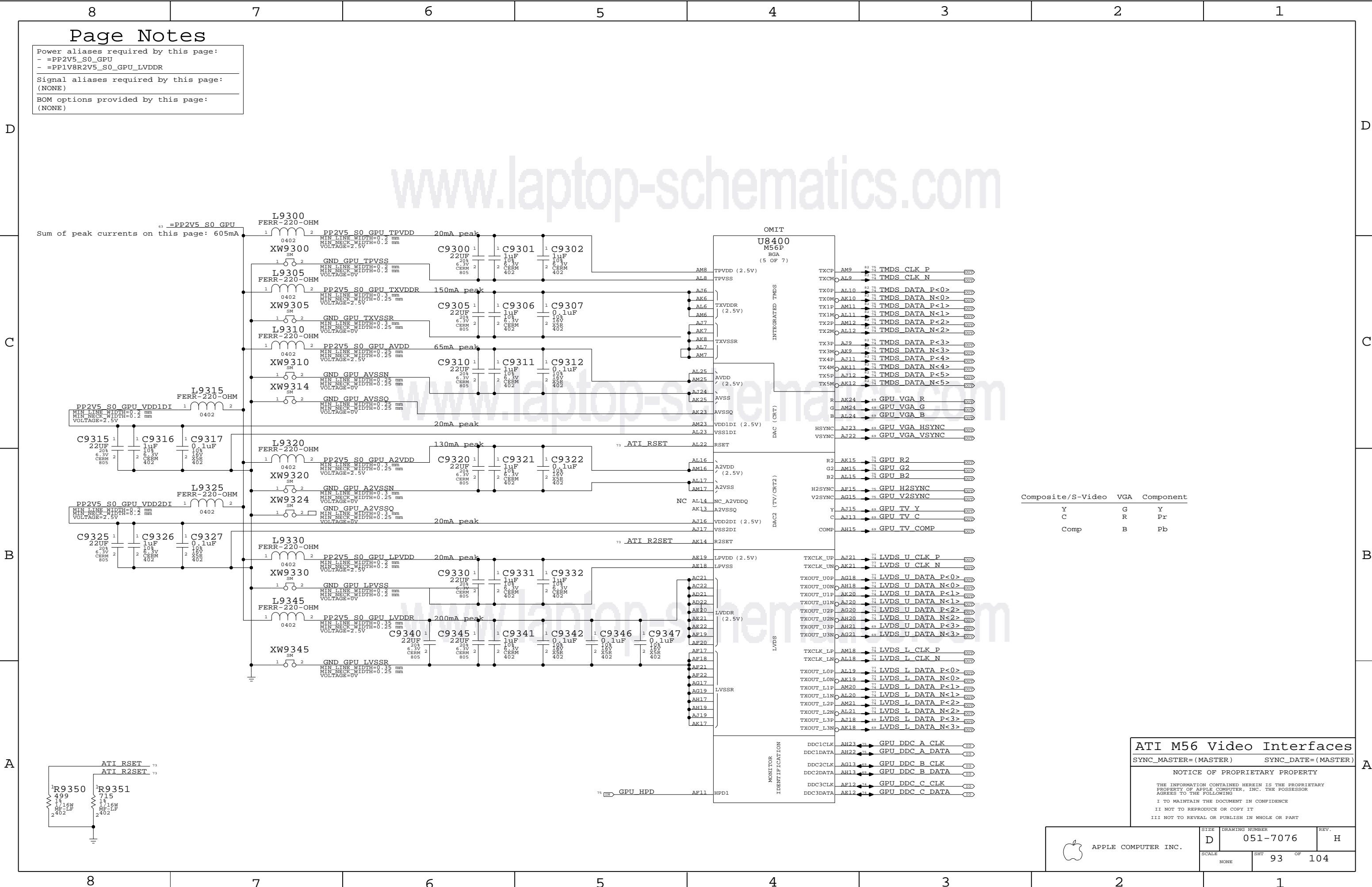
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NONE	90	104





Page Notes

Power aliases required by this page:
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

ATI M56 Video Interfaces

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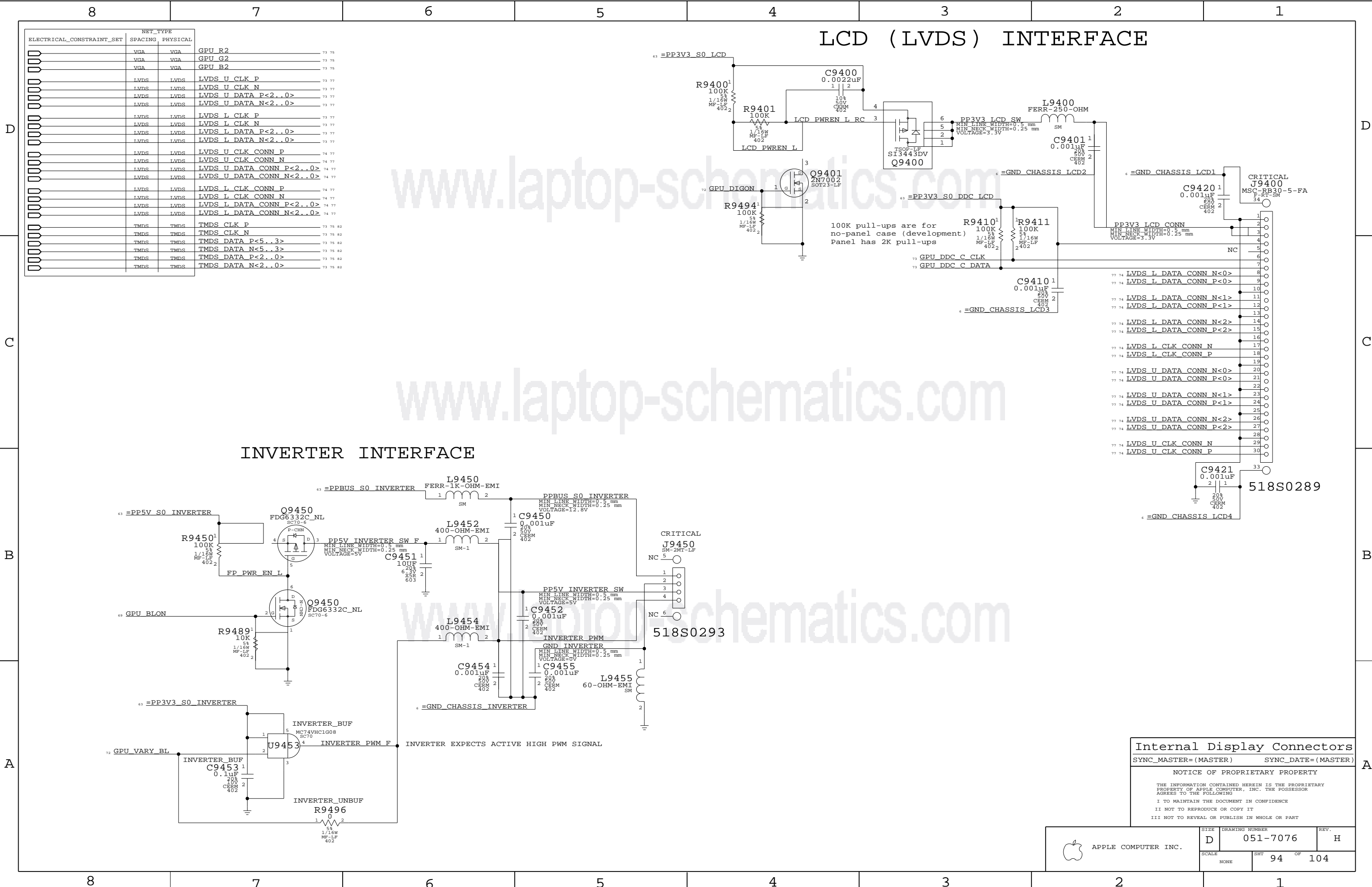
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D	051-7076	H
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NONE	93	104



LCD (LVDS) INTERFACE

INVERTER INTERFACE

Internal Display Connectors

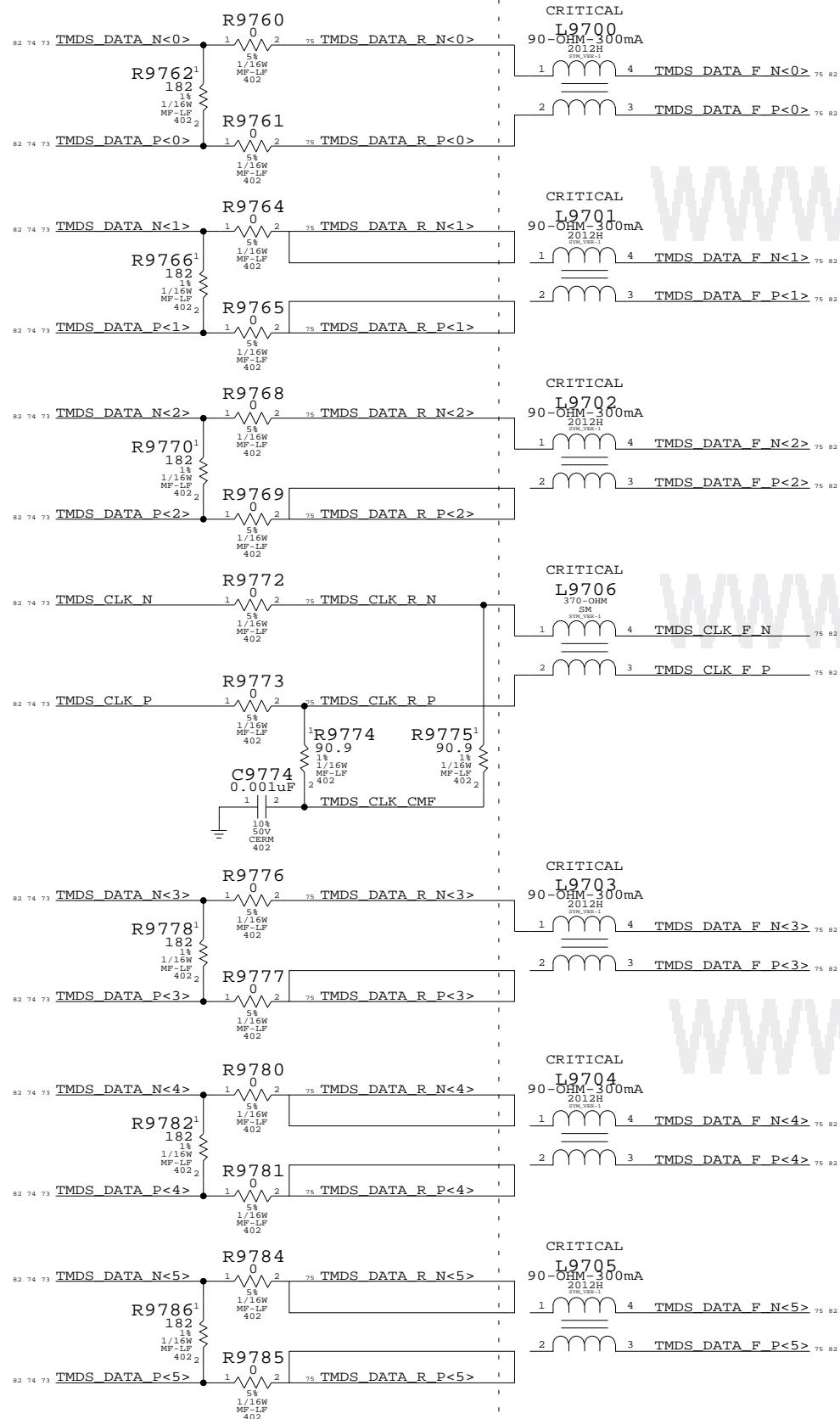
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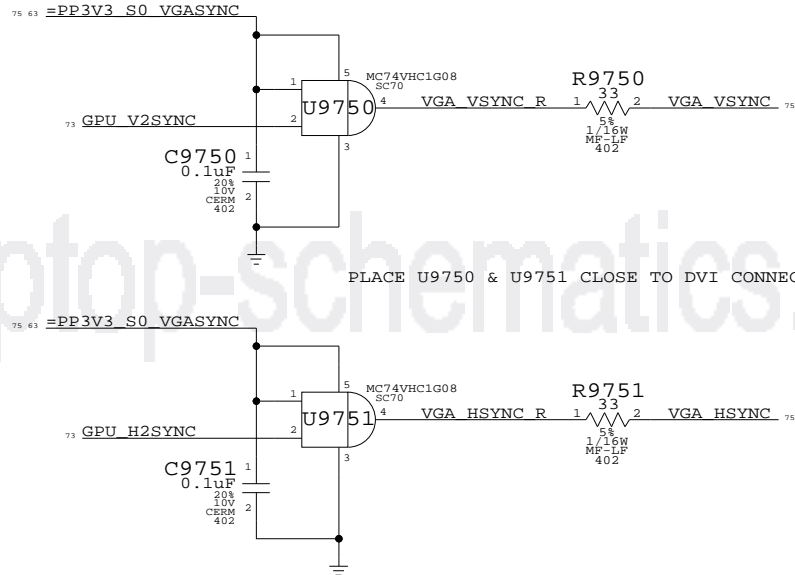
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TMDS Filtering

Place series R's and common-mode filtering close to GPU, common mode chokes near connector.



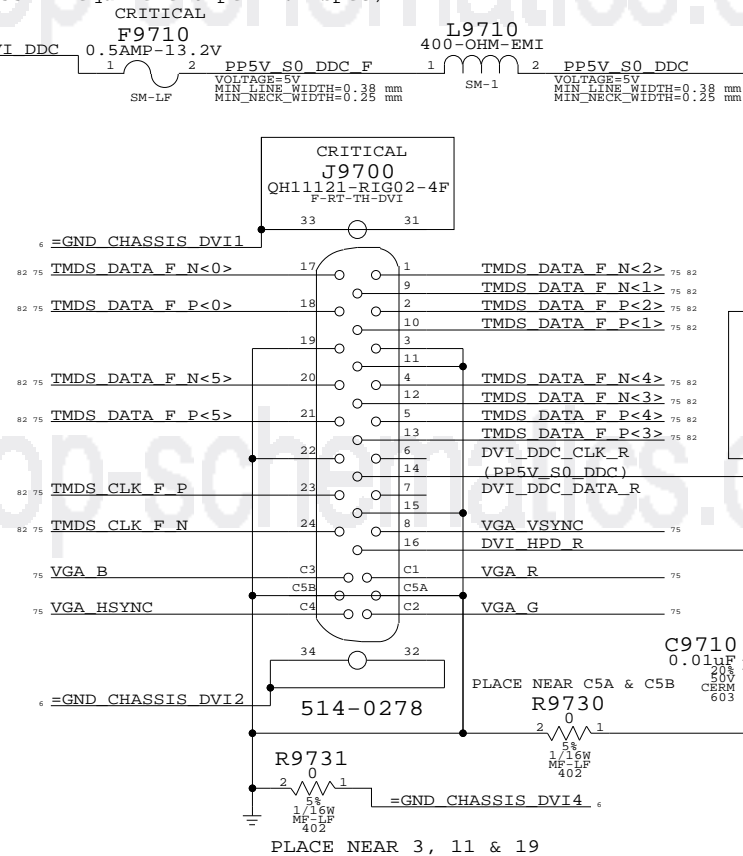
VGA SYNC BUFFERS



PLACE U9750 & U9751 CLOSE TO DVI CONNECTOR

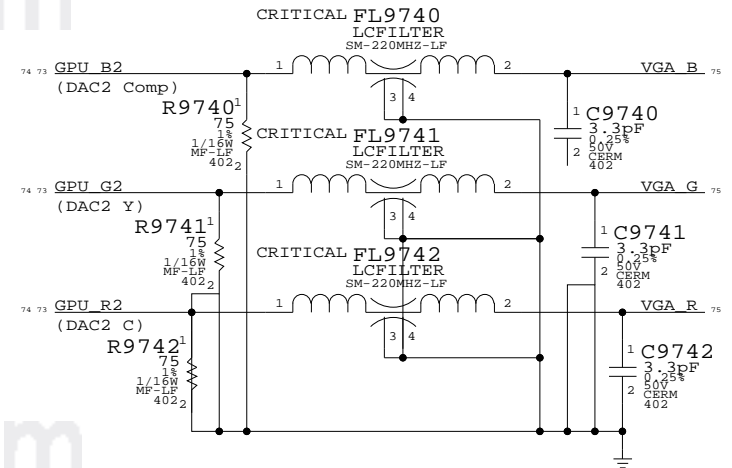
DVI INTERFACE

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

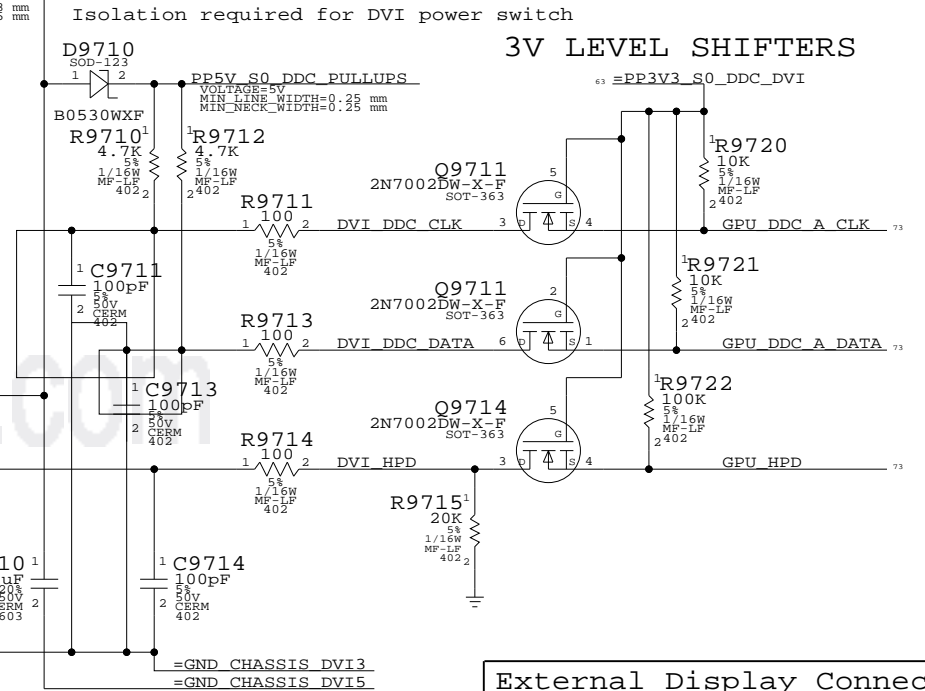


ELECTRICAL_CONSTRAINT_SET	NET_TYPE	
	SPACING	PHYSICAL
TMDS	TMDS	TMDS CLK R_P
	TMDS	TMDS CLK R_N
	TMDS	TMDS DATA R_P<5..0>
	TMDS	TMDS DATA R_N<5..0>
TMDSCONN	TMDSCONN	TMDS CLK F_P
	TMDSCONN	TMDS CLK F_N
	TMDSCONN	TMDS DATA F_P<5..0>
	TMDSCONN	TMDS DATA F_N<5..0>

ANALOG FILTERING PLACE CLOSE TO CONNECTOR



3V LEVEL SHIFTERS



External Display Connector

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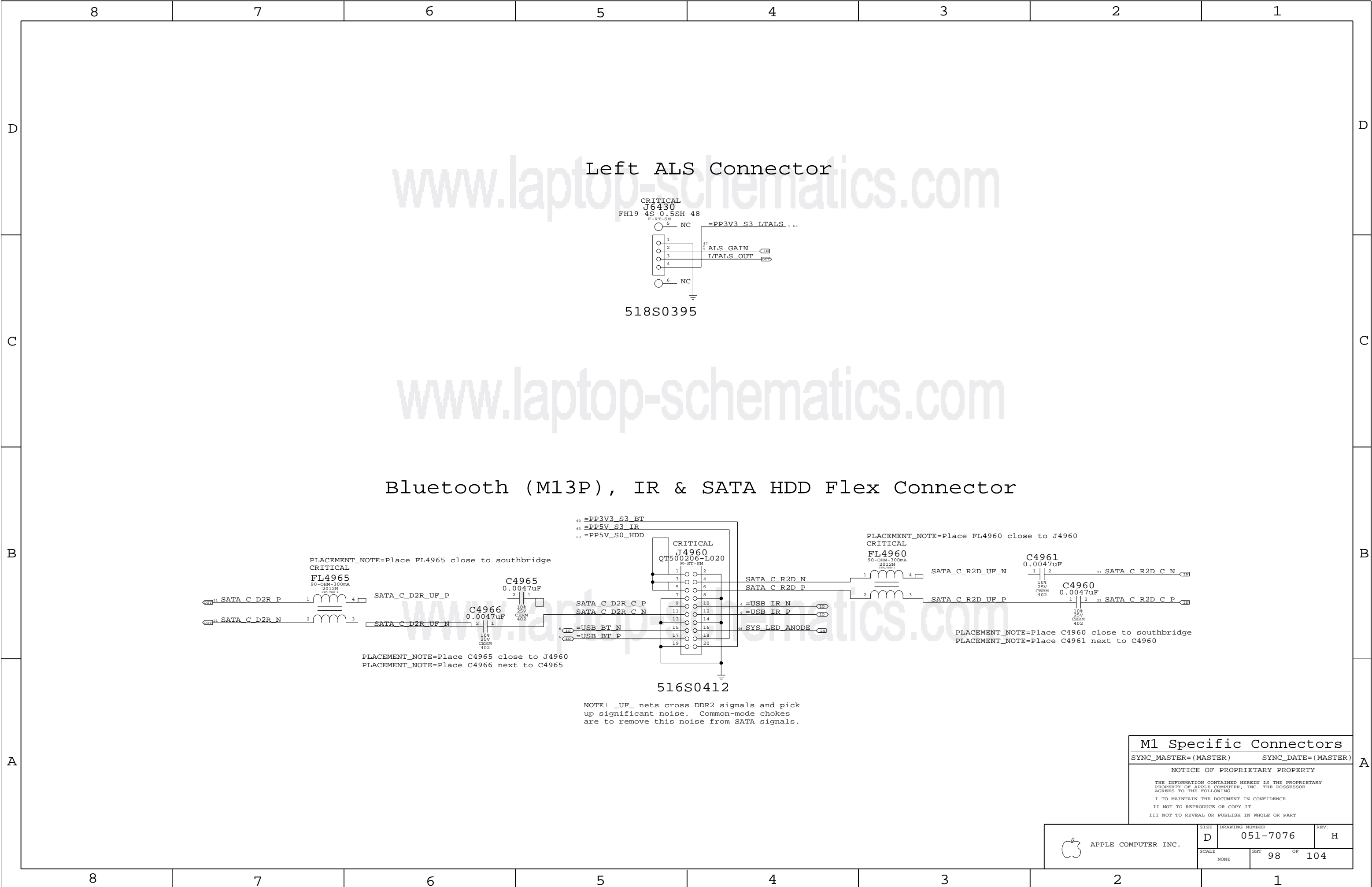
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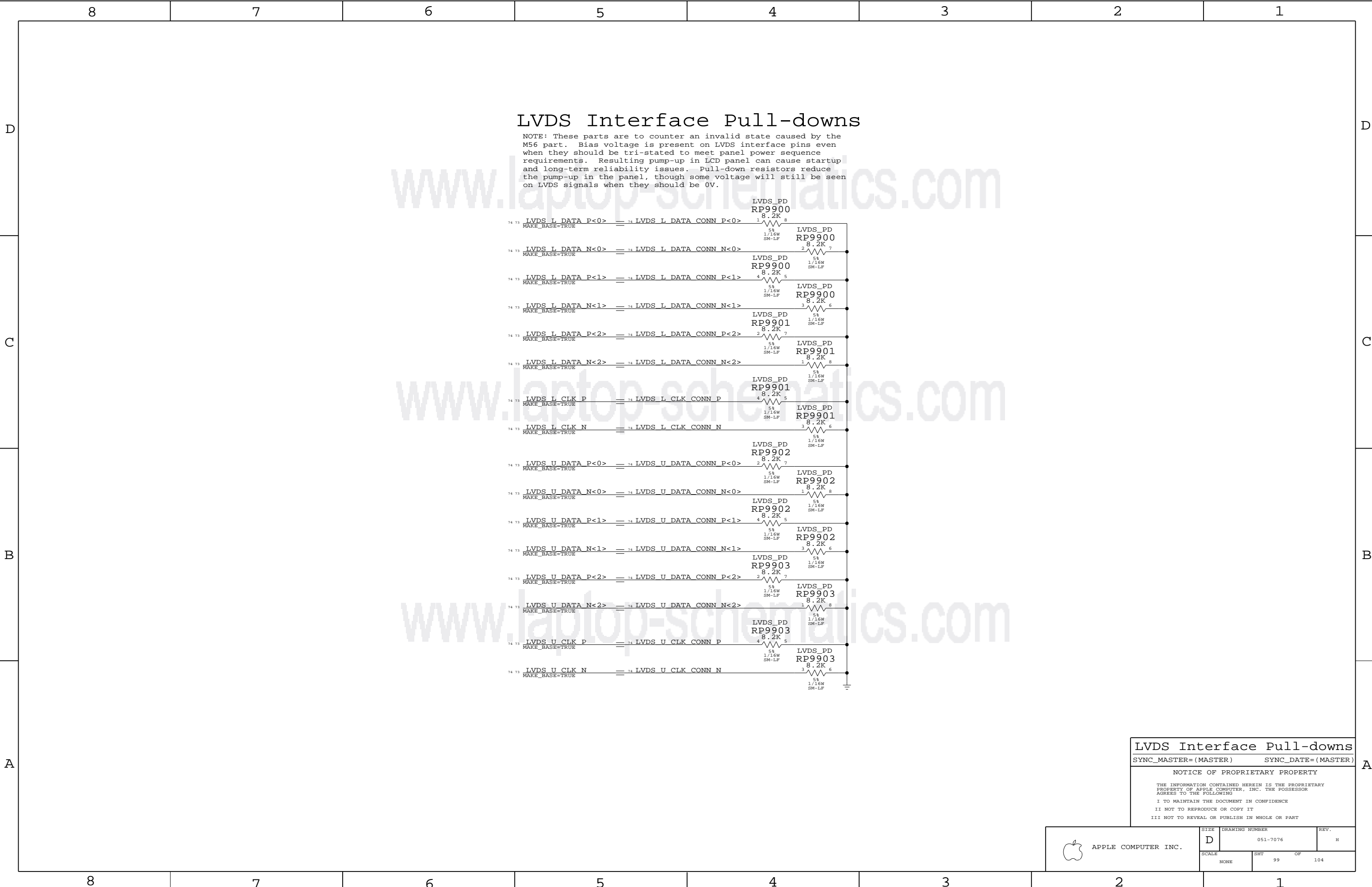
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LVDS Interface Pull-downs

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8	7	6	5	4	3	2	1
Date - Radar # - Description			Date - Radar # - Description			Date - Radar # - Description	
DMS Release #03000 (RFA #394758)			DMS Checkin #07001			DMS Checkin #11002	
2005/08/11 - 4214109 - Changed J4931 to proper 518S0342 part.			2005/09/28 - 4221965 - Added 2.2uF caps on SO-DIMM VREF pins.			2005/11/21 - 4351196 - Added 1K pull-down on IDE_RESET_L.	
2005/08/12 - 4231030 - Changed pinout of J4960, added placement notes.			2005/09/28 - 4278828 - Adjusted P5VS5_PGOOD R's, added cap on PM_RSMRST_L.			(11.5.0)	2005/11/21 - 4343202 - Changed RC value and net name for USB OC.
Changes from Proto Branch (DMS Release #04000):			2005/09/29 - 4232826 - Swapped Vtt RPAK functions to free up unnecessary part.			(11.6.0)	2005/11/22 - 4350840 - Swapped TMDS termination components for placement.
2005/08/27 - 4230219 - Changed Y3301 to non-obsolete part.			2005/09/30 - 4261313 - Added placeholder connector for IR FFC connector.			(11.7.0)	2005/11/22 - 4352020 - Changed 2.5V S3 supply inductor & compensation values.
2005/08/27 - 4235208 - Changed value of R7707 to fix 2.5V S3 supply.			2005/09/30 - 4282162 - Changed GPU BBN supply to MAX1673.			2005/11/28 - 4347845 - Added pull-down resistors on LVDS interface.	
2005/08/27 - 4235213 - Changed R8305, R8310, R8315 to slow down FET RCs.			2005/09/30 - 4248911 - Sync with M38 & M42.			2005/11/30 - 4227340 - Removed CPU VCore current sense input RC.	
2005/08/27 - 4235401 - Moved a few pins at LIO BTB connector.			2005/09/30 - 4282349 - Added CRITICAL flags to parts identified in scrub.			2005/11/30 - 4331670 - Added CRITICAL flags to some more parts.	
2005/08/27 - 4227325 - Removed S0 option for camera, now S3-only.			2005/09/30 - 4274915 - C1001 stuffing change from Proto 2 MLB branch.			2005/11/30 - 4343864 - Added EMI/ESD parts at camera connector.	
2005/08/27 - 4227369 - Removed SMC options for display/backlight, now GPU-only.			DMS Checkin #07002			2005/11/30 - 4351181 - Changed ITP connector BOM option.	
2005/08/27 - 4225433 - Changed PBUS voltage sense circuit.			2005/10/04 - 4256409 - Changed fan CTL series R's to 2N7002 level-shifter.			2005/11/30 - 4351196 - Changed IDE_RESET_L pull-down from 1K to 15K.	
2005/08/28 - 4217535 - Added Left ALS FFC connector.			2005/10/04 - 4261313 - Deleted placeholder connector, grew HDD connector for IR.			(11.8.0)	2005/11/30 - 4358831 - Added pull-downs on two SB-to-SMC signals.
2005/08/28 - 4232563 - Changed analog video from Y/C/Comp to G2/R2/B2.			2005/10/04 - 4281394 - BOM option change to stuff right USB ESD protection part.			2005/12/01 - 4362404 - Changed TMDS diff term from 100-ohm to 180-ohm.	
2005/08/28 - 4235203 - Changed BOM settings to stuff R2251.			2005/10/06 - 4227330 - Added ESD protection on top-case USB port.			2005/12/01 - 4352020 - Changed 2.5V supply inductor to RoHS-compliant part.	
2005/08/28 - 4217524 - Added LEFT ALS connector (J6430).			2005/10/07 - 4286888 - BOM restructuring per EVT build plan.			2005/12/01 - 4227340 - Changed supply for 1.8V S3 current sense amp.	
2005/08/28 - 4217535 - OMITs and tables to change 4-pin WTB connector parts.			2005/10/07 - 4292633 - Changed IMVP6 10K NTC from 10% to 5% part.			2005/12/01 - 4362566 - Restructured BOM for thick/thin PCB versions.	
2005/08/28 - 4221973 - Added pull-up for SB GPIO22 (REQ4#).			2005/10/07 - 4248911 - Sync with M38 & M42.			2005/12/01 - 4347845 - RPAK pinswaps to LVDS pull-downs for PCB layout.	
2005/08/28 - 4225369 - Changed ISL6269 PVCC aliases, added RC for 3.3V S5.			DMS Checkin #07003			(11.9.0)	DMS Checkin #11003
2005/08/28 - 4225433 - Changed PBUS Voltage Sense circuit.			2005/10/08 - 4214493 - Simplified FireWire port power circuit for BOM consolidation.			2005/12/02 - 4256256 - Added BOMOPTION to R8801 to allow per-project control.	
2005/08/28 - 4227322 - Changed FW323 PCI_VIOS pin from 3.3V S0 to 3.3V S3.			2005/10/08 - 4293072 - Various BOM / connection changes at IMVP6 (CPU VCore).			2005/12/02 - 4363870 - Removed M56 GPU die rev B13 support from BOM.	
2005/08/28 - 4235179 - OMIT and table to change 8-pin DC-In connector to 6-pin.			2005/10/08 - 4286729 - Changed value of TPM Xtal caps.			2005/12/02 - 4368848 - Removed M1a support from BOM.	
2005/08/28 - 4235179 - Changed PBUS net names to merge PBUS A & PBUS B.			2005/10/08 - 4290735 - Swapped trackpad & PCIe Mini Card USB connections.			2005/12/02 - 4217524 - Updated part number for J6430.	
2005/08/28 - 4232715 - Added FireWire ISense resistor, changed INA193 to INA194.			2005/10/09 - 4235898 - Part moves & refiles changes to support sync with M9.			(11.10.0)	DMS Release #12000-13000 (DVT releases)
2005/08/28 - 4235217 - Added RC on Q3820 gate to slow down ODD FET turn-on.			2005/10/09 - 4214494 - Changed GPU VCore supply enable to use 1.2V/2.5V S3 PGOODs.			2005/12/07 - 4375840 - Synced 4 pages from m1b_dvt branch back to trunk.	
2005/08/28 - 4225369 - OMITs and tables for staged LeMenu BOM approach.			2005/10/09 - 4272237 - Changed 2.5V S0 FET RC to 100K to slow down turn-on.			2005/12/12 - 4235898 - Changes to LVDS net names to support mux option.	
2005/08/28 - 4227323 - Repinned Top-Case Flex connector.			DMS Checkin #07004			2005/12/12 - 4362451 - Added MAKE_BASE=TRUE to SMC 32KHz SUSCLK net.	
DMS Checkin #04001			2005/10/10 - 4232826 - Swapped Vtt RPAK functions to optimize layout.			2006/01/03 - 4375840 - Synced 1 page from m1b_dvt branch back to trunk.	
2005/08/29 - 4235179 - Changed J8200 to proper 6-pin part.			2005/10/10 - 4247941 - Net property updates found via back-annotation.			2006/01/03 - 4290282 - Removed BOM table, changed L9455 to 155S0002.	
2005/08/29 - 4232826 - Changed MEM_ODT* from RPAKs to discrete Rs.			DMS Checkin #07005			2006/01/03 - 4347845 - Changed LVDS pull-downs from 10K to 8.2K.	
2005/08/29 - 4217524 - Changed R6430 from 4.5K to 3.5K.			2005/10/10 - 4229560 - Removed Physical Security circuitry.			2006/01/03 - 4391436 - Swapped N/P signal names on one portion of SATA_R2D.	
2005/08/29 - 4237119 - Changed LIO 5V S3 to 5V S5.			2005/10/10 - 4214493 - Cost reductions to GPU power supply circuitry.			2006/01/03 - 4362451 - Changed SCH/PCB/BOM part descriptions for Rev A.	
2005/08/29 - 4225369 - Changed 3.3V S5 sequence to follow 5V S5 PGOOD.			2005/10/10 - 4214847 - Changed 0-ohm resistor to solder jumper.			2006/01/03 - 4362451 - Removed power jumpers and 0-ohm resistor.	
2005/08/29 - 4227336 - Changed Y5920 to 197S0169.			2005/10/10 - 4214847 - Changed 0-ohm resistor to solder jumper.			2006/01/05 - 4362566 - Removed 920- number for thin PCB option.	
2005/08/29 - 4227309 - Resolved sync issues with M38 (SB page 21).			2005/10/10 - 4248911 - Sync with M38 & M42.			2006/01/05 - 4394079 - Added BOMOPTION to SYS_ONEWIRE pull-up.	
2005/08/29 - 4227310 - Resolved sync issues with M38 (SB page 22).			2005/10/10 - 4295280 - Changed sleep LED connection per new SMC ERS.			2006/01/05 - 4362451 - Removed power jumpers and 0-ohm resistor.	
2005/08/29 - 4227312 - Resolved sync issues with M38 (SB page 23).			DMS Checkin #07006			2006/01/05 - 4362451 - Restructured BOM tables to eliminate LeMenu.	
2005/08/29 - 4227322 - Sync page 44 with M42 to fix FW power net S-states.			2005/10/11 - 4261313 - Updated SATA connector pinout to match latest flex.			2006/01/06 - 4402184 - Changed R7540 value for IMVP6 load-line improvement.	
2005/08/29 - 4227332 - Resolved sync issues with M38 (SMC page 58).			2005/10/11 - 4227308 - Deleted unnecessary MCH TVDAC filtering.			2006/01/06 - 4362451 - Added System Block Diagram, updated Power Diagram.	
2005/08/29 - 4227335 - Changed U5900 to resolve ROHS issue.			2005/10/11 - 4229560 - Changed SB GNT3#/GNT4# back to test points.			2006/01/06 - 4362451 - Changed BOM options for production SMC, BootROM.	
DMS Checkin #04002			2005/10/12 - 4248911 - Sync with M38 & M42.			(13.2.0)	DMS Release #A000 (PVT Release)
2005/08/30 - 4225433 - Fixed voltage divider values in PBUS VSense circuit.			2005/10/12 - 4298899 - Changed stuffing option to disable PLT_RST gating.			2006/01/21 - 4412882 - Changed R7623 from 1.33K to 931 ohms.	
2005/08/30 - 4217535 - Removed BOM tables and OMITs for new 4-pin WTB connector.			2005/10/12 - 4297684 - Split FW323 VSSA from VSS to reduce noise.			(A.1.0)	2006/01/21 - 4414757 - Changed 138S0552 to 138S0580 & 138S0553 to 138S0581.
2005/08/31 - 4214109 - Reversed pinout of J4931 to match updated PCB footprint.			2005/10/12 - 4223808 - Power supply changes per vendor feedback.			2006/01/26 - 4420815 - Changed 2x 128S0077 to 128S0068.	
2005/08/31 - 4227328 - Added ESD protection diode on right USB port.			2005/10/12 - 4227320 - Updated SB pin name for GPIO 5 (ODD_PWR_EN_L).			(B.0.0)	DMS Release #B000 (PVT BOM Update)
2005/08/31 - 4223808 - Various power supply R/C updates, plus some R/C adds.			2005/10/12 - 4244539 - Retasked FET to control 3.3V S0 FET from GPU VCore PGOOD.			2006/02/09 - 4440116 - Pulled new schematic part number (051-7099).	
2005/08/31 - 4227315 - Changed BSA bus pull-ups from 2K to 10K.			2005/10/12 - 4247941 - Added properties to resolve a PCB constraint issue.			2006/02/09 - 4440116 - Restructured BOM for 3 CPU configs.	
2005/08/31 - 4237025 - Added R8824 and R8827 for GPU memory configuration straps.			2005/10/12 - 4214493 - Consolidated 0.22uF caps in design.			2006/02/09 - 4440116 - Updated BootROM / SMC part numbers.	
DMS Checkin #04003			2005/10/12 - 4298905 - Changed ethernet VMAIN_AVLBL connection.			(A.0.0)	DMS Release #A000 (Ramp Config Update)
2005/08/31 - 4240157 - Corrected pinout at SATA/BT conn (J4960) to match flex.			2005/10/12 - 4298943 - Replaced last remaining non-RoHS compliant connector.			2006/02/13 - 4420815 - Changed remaining 128S0077 to 128S0086.	
2005/08/31 - 4240150 - Swapped PCIe Mini Card R2D/D2R connections at J5500.			2005/10/12 - 4214494 - Implemented circuit to power down ethernet in S3 on battery.			2006/02/13 - 4420815 - Added 128S0077 as alternate for 128S0086.	
2005/08/31 - 4232563 - Corrected net properties on R2/G2/B2 nets.			DMS Checkin #07007			2006/02/13 - 4437189 - Changed R7757 to 1Mohm & R7770 to 100K.	
2005/08/31 - 4227306 - Swapped primary & alt part numbers for CPU VCore caps.			2005/10/13 - 4247941 - Swapped pins at trackpad ESD protection diode.			(A.1.0)	2006/02/13 - 4431947 - Removed NO STUFF option from C3309.
2005/08/31 - 4240300 - Changed C6455 to a smaller part for cost & MCO.			DMS Checkin #07008			(B.0.0)	DMS Release #B000 (PVT BOM Roll-In)
2005/08/31 - 4240486 - Power line width & neck reductions at PCB request.			2005/10/13 - 4247941 - Unswapped pins at trackpad ESD protection diode.			2006/02/17 - 4449123 - Changed C7537: 4.7nF -> 47pF, R7537: 3.57K -> 4.42K.	
2005/08/31 - 4240257 - Swapped some top & bottom EMC connections at DVI connector.			DMS Checkin #07009			(C.0.0)	DMS Release #C000 (Ramp BOM Update)
DMS Checkin #04004			2005/10/13 - 4247941 - Removed NO_TEST properties from CPU FSB strobe signals.			2006/03/03 - 4457745 - Added 128S0094 & 128S0095 as alternates for 128S0060.	
2005/08/31 - 4227328 - Changed EMI caps from 50V to 16V to fid in ESD protection.			2005/10/13 - 4247941 - Spacing/Physical rule updates to match latest board database.			2006/03/03 - 4457801 - Added 128S0081 as alternate for 128S0061.	
DMS Checkin #04005			2005/10/14 - 4247941 - Restored NO_TEST properties, added EXPOSED_VIA properties.			2006/03/03 - 4466770 - Changed R7920 from 5% to 1% to reduce variation.	
2005/09/02 - 4241087 - Fixed pinout of USB D+/D- at camera connector to match FHB.			2005/10/17 - 4292633 - Changed remaining 10K NTCs to new 5% part.			2006/03/03 - 4399085 - Changed C7532 from 10nF to 15nF to slow CPU slew rate.	
2005/09/02 - 4243269 - Inverted GPU VCore control, adjusted supply R values.			2005/10/17 - 4304248 - Updated GPU VCore / BBP voltages for B13/B24 support.			2006/03/03 - 4424175 - Changed 8 VRAM strap resistors to enable ICT testing.	
2005/09/02 - 4244019 - Moved GPU-related power alias from PP3V3_S0 to PP3V3_S0_GPU.			DMS Release #08000-11000 (EVT releases)			(D.0.0)	DMS Release #D000 (BOM Update)
2005/09/02 - 4240486 - Adjusted line/neck widths, changed J4931 to 518S0371.			2005/10/20 - 4310267 - Synced 4 pages from m1b_evt branch back to trunk.			2006/03/31 - 4485021 - Changed R7542 from 9.31K to 11.5K for CPU VCore OCP.	
DMS Checkin #04006			2005/10/21 - 4310267 - Synced 3 pages from m1b_evt branch back to trunk.			2006/03/31 - 4498859 - Updated BOM table for screened ISL6262.	
2005/09/03 - 4232534 - Fixed documentation of battery address on I2C page.			2005/10/21 - 4235898 - Synced 2 pages from m9/mlb.			(E.0.0)	DMS Release #E000 (BOM Update)
2005/09/03 - 4244484 - Changed P1V5S0_RUNSS circuit to work properly in G3Hot.			2005/10/26 - 4310267 - Synced 4 pages from m1b_evt branch back to trunk.			2006/03/31 - 4436716 - Added BOM table for ATI rev B26.	
2005/09/03 - 4244539 - Added GPUVCORE_PGOOD to 1.2V, 1.8V, & 2.5V S0 sequence.			2005/11/03 - 4310267 - Synced 6 pages from m1b_evt branch back to trunk.			2006/04/05 - 4502903 - Reset BOM part numbers & EEE codes for B26 change.	
2005/09/03 - 4227315 - Changed SMBus pull-ups to 4.7K.			2005/11/15 - 4310267 - Synced 5 pages from m1b_evt branch back to trunk.			(F.0.0)	DMS Release #F000 (New EEE/BOM Release)
2005/09/03 - 4232534 - Added notes for power supplies and connectors.			2005/11/15 - 4298899 - Removed unused platform reset gate.			(G.0.0)	DMS Release #G000 (RFA Re-release)
DMS Checkin #04007			2005/11/15 - 4322537 - Updated thru-hole SO-DIMM connector part number.			2006/04/17 - 4517184 - Updated BOM part #s and EEE codes for config changes.	
2005/09/06 - 4240486 - Removed NO_TEST property from GPU HSYNC and VSYNC.			2005/11/16 - 4345498 - Updated Ethernet & FireWire crystal part numbers.			(H.0.0)	DMS Release #H000 (BOM Update)
2005/09/06 - 4246683 - Removed NO STUFF option from R8805 per ATI request.			2005/11/16 - 4235898 - Aliased connection to ALS_GAIN to support M9 request.				
2005/09/06 - 4232534 - Fixed label BOM tables to call out proper EEE #'s.			2005/11/16 - 4235898 - Changed Yukon power rail neck widths per M9 request.				
DMS Release #05000-07000 (Proto 2 releases)			2005/11/16 - 4227333 - Updated SMC net names per ERS v1.2.1.				
2005/09/08 - 4247941 - Net property & name changes to support PCB/ICT requests.			2005/11/16 - 4345921 - FUNC_TEST updates per test team request.				
2005/09/08 - 4248911 - Sync with M38 & M42.			2005/11/16 - 4346006 - Updated J5500 pinout to match updated LIO board pinout.				
2005/09/08 - 4214493 - Combined RTC coin cell diodes into dual-diode package.			2005/11/16 - 4343202 - Changed USB overcurrent switch to TPS2051B, added OC* RC.				
2005/09/08 - 4229560 - First implementation of Physical Security Guidelines.			2005/11/16 - 4346184 - Inserted common-mode chokes on SATA R2D/D2R pairs.				
2005/09/16 - 4256660 - Updated FUNC_TEST property for merged PBUS.			DMS Checkin #11001				
2005/09/16 - 4229560 - Changed FW PCI REQ/GNT pair for Physical Security.			2005/11/16 - 4235898 - Sync with M38 & M42.				
2005/09/19 - 4247941 - GND line/neck/voltage properties updated per PCB request.			2005/11/16 - 4298899 - Fixed ethernet reset net name on page 26.				
2005/09/19 - 4235898 - Moved signal alias to improve schematic reuse.			2005/11/16 - 4227333 - Fixed single-pin nets caused by SMC net name updates.				
2005/09/20 - 4214847 - Updated L1970 (old part no longer exists in library).			2005/11/18 - 4235898 - Changed R4210 package size per M9 request.				
2005/09/21 - 4227306 - Changed CPU VCore caps to proper production part number.			2005/11/18 - 4235898 - Changed C9710 GND connection per M9 request.				
2005/09/21 - 4234952 - Replaced FDG6324L parts with FDG6332C for cost & supply.			2005/11/19 - 4346184 - Fixed location of SATA R2D common-mode choke.				
2005/09/26 - 4239505 - Updated J4200 (old part no longer exists in library).			2005/11/19 - 4347717 - Changed SMS self-test pull-up to pull-down.				
2005/09/26 - 4274915 - Thermal sensor BOM updates from Proto 2 MLB branch.			2005/11/19 - 4350840 - Simplified TMDS filtering to allow movement of filter.				
2005/09/26 - 4274915 - U6301 part number updated to M1 development BootROM.			2005/11/19 - 4229560 - Changed FW chip back to REQ/GNT3.				
			2005/11/19 - 4350849 - Added option to connect SB_GPIO30 to ENET_LOM_DIS_L.				
			2005/11/19 - 4340256 - Changed topcase flex trackpad power from 3.3V to 5V.				
			2005/11/19 - 4292165 - Refreshed schematic symbol for U3750 (library update).				

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8		7		6		5		4		3		2		1	
M1 Board-Specific Spacing & Physical Constraints															
BOARD LAYERS								BOARD AREAS				BOARD UNITS (MIL OR MM)		ALLEGRO VERSION	
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM								NO_TYPE, BGA				MM		15.2	
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
DEFAULT		*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM							
STANDARD		*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
55_OHM_SE		TOP, BOTTOM	Y	0.100 MM	0.100 MM										
55_OHM_SE		*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
50_OHM_SE		TOP, BOTTOM	Y	0.124 MM	0.124 MM										
50_OHM_SE		*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
45_OHM_SE		TOP, BOTTOM	Y	0.150 MM	0.150 MM										
45_OHM_SE		*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
40_OHM_SE		TOP, BOTTOM	Y	0.185 MM	0.185 MM										
40_OHM_SE		*	Y	0.131 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
35_OHM_SE		TOP, BOTTOM	Y	0.230 MM	0.230 MM										
35_OHM_SE		*	Y	0.165 MM	0.165 MM	=STANDARD	=STANDARD	=STANDARD							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
27P4_OHM_SE		TOP, BOTTOM	Y	0.335 MM	0.335 MM										
27P4_OHM_SE		*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
35_55_OHM_SE		TOP, BOTTOM	Y	0.230 MM	0.100 MM										
35_55_OHM_SE		*	Y	0.165 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD							
Unsupported rule															
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
75_OHM_SE		*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
70_OHM_DIFF		*	Y	0.149 MM	0.149 MM	=STANDARD	0.125 MM	0.125 MM							
70_OHM_DIFF		TOP, BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
75_OHM_DIFF		*	Y	0.131 MM	0.131 MM	=STANDARD	0.125 MM	0.125 MM							
75_OHM_DIFF		TOP, BOTTOM	Y	0.161 MM	0.161 MM		0.125 MM	0.125 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
80_OHM_DIFF		*	Y	0.115 MM	0.111 MM	=STANDARD	0.125 MM	0.125 MM							
80_OHM_DIFF		TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
85_OHM_DIFF		*	Y	0.101 MM	0.101 MM	=STANDARD	0.125 MM	0.125 MM							
85_OHM_DIFF		TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
90_OHM_DIFF		*	Y	0.102 MM	0.102 MM	=STANDARD	0.220 MM	0.220 MM							
90_OHM_DIFF		TOP, BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
100_OHM_DIFF		*	Y	0.080 MM	0.080 MM	=STANDARD	0.200 MM	0.200 MM							
100_OHM_DIFF		TOP, BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
110_OHM_DIFF		*	Y	0.077 MM	0.077 MM	=STANDARD	0.330 MM	0.330 MM							
110_OHM_DIFF		TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM							
M1 Spacing & Physical Constraints															
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)															
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												SCALE NONE	SHEET 103 OF 104		
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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	
STANDARD	*	=DEFAULT	
BGA_P1MM	*	=DEFAULT	
BGA_P2MM	*	=DEFAULT	
BGA_P3MM	*	=DEFAULT	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FB_CLK	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	
1.8:1_SPACING	*	0.18 MM	
2:1_SPACING	*	0.2 MM	
2.5:1_SPACING	*	0.25 MM	
3:1_SPACING	*	0.3 MM	
4:1_SPACING	*	0.4 MM	

Allow 0.1 MM on blind-to-buried via dogbones (layers 2 & 11)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	ISL2, ISL11	0.1 MM	
1.8:1_SPACING	ISL2, ISL11	0.1 MM	
2:1_SPACING	ISL2, ISL11	0.1 MM	
2.5:1_SPACING	ISL2, ISL11	0.1 MM	
3:1_SPACING	ISL2, ISL11	0.1 MM	
4:1_SPACING	ISL2, ISL11	0.1 MM	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	ISL2, ISL11	0.1 MM	
CLK_PCIE	ISL2, ISL11	0.1 MM	
CLK_MED	ISL2, ISL11	0.1 MM	
CLK_SLOW	ISL2, ISL11	0.1 MM	
CPU_COMP	ISL2, ISL11	0.1 MM	
CPU_GTLREF	ISL2, ISL11	0.1 MM	
CPU_VCCSENSE	ISL2, ISL11	0.1 MM	
DMI	ISL2, ISL11	0.1 MM	
LVDS_PAIR2PAIR	ISL2, ISL11	0.1 MM	
MEM_20THER	ISL2, ISL11	0.1 MM	
PCIE	ISL2, ISL11	0.1 MM	
SATA	ISL2, ISL11	0.1 MM	
TMDS_PAIR2PAIR	ISL2, ISL11	0.1 MM	
VGA	ISL2, ISL11	0.1 MM	

Rules for "Topology #3" for FSB signals, Napa DG tables 4-7 & 4-12.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR_OVERRIDE	*	=2:1_SPACING_OVERRIDE	VERRIDE
FSB_ADDR2ADDR_OVERRIDE	*	=STANDARD_OVERRIDE	VERRIDE
FSB_ADSTB_OVERRIDE	*	=2:1_SPACING_OVERRIDE	VERRIDE
FSB_ADDR2ADSTB_OVERRIDE	*	=2:1_SPACING_OVERRIDE	VERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA_OVERRIDE	*	=2:1_SPACING_OVERRIDE	VERRIDE
FSB_DATA2DATA_OVERRIDE	*	=STANDARD_OVERRIDE	VERRIDE
FSB_DSTB_OVERRIDE	*	=2:1_SPACING_OVERRIDE	VERRIDE
FSB_DATA2DSTB_OVERRIDE	*	=2:1_SPACING_OVERRIDE	VERRIDE

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS	*	LVDS_100D
TMDS	*	TMDS_100D
TMDSCONN	*	TMDS_100D
VGA	*	VGA_75S

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_20THER_OVERRIDE	*	0.5 MM_OVERRIDE	VERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI_2PCI_OVERRIDE	*	0.1 MM_OVERRIDE	VERRIDE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCI	PCI	*	PCI_2PCI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENETCONN	*	*	ENET
TMDSCONN	*	*	TMDS

"Stale" physical / spacing types

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ANALOG	*	*	FSB_COMMON
FSB_P2MM	*	*	FSB_COMMON
I2C	*	*	SMB
GND	*	*	STANDARD
MEM_PP1V8_S3	*	*	STANDARD

