

# PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN  
1/2 OZ CU THICKNESS: 0.7 MILS  
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%  
DIELECTRIC: FR-4  
LAYER COUNT: 10  
SIGNAL TRACE WIDTH: 4 MILS  
SIGNAL TRACE SPACING: 4 MILS  
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

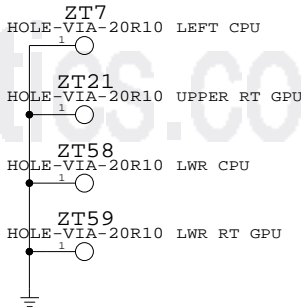
## BOARD STACK-UP AND CONSTRUCTION

1-8-1 BLIND MICROVIA/20R10 BURIED VIA/20R10 TH VIA		
1		SIGNAL (1/2 OZ + COPPER PLATING)
2	PREPREG (3 MIL)	SIGNAL (1/2 OZ)
3	PREPREG (3 MIL)	GROUND (1/2 OZ)
4	CORE (3 MIL)	SIGNAL (1/2 OZ)
5	PREPREG (5 MIL)	CUT POWER PLANE (1 OZ)
6	CORE (5 MIL)	CUT POWER PLANE (1 OZ)
7	PREPREG (5 MIL)	SIGNAL (1/2 OZ)
8	CORE (3 MIL)	GROUND (1/2 OZ)
9	PREPREG (3 MIL)	SIGNAL (1/2 OZ)
10	PREPREG (3 MIL)	SIGNAL (1/2 OZ + COPPER PLATING)

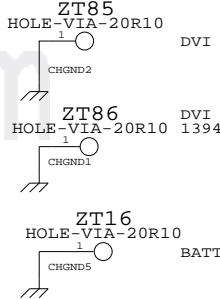
## BOARD HOLES

### CHASSIS MOUNTS

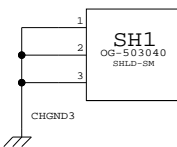
#### ASICS HEATSINK MOUNTS



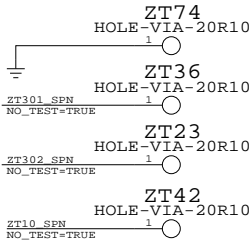
#### I/O AREA



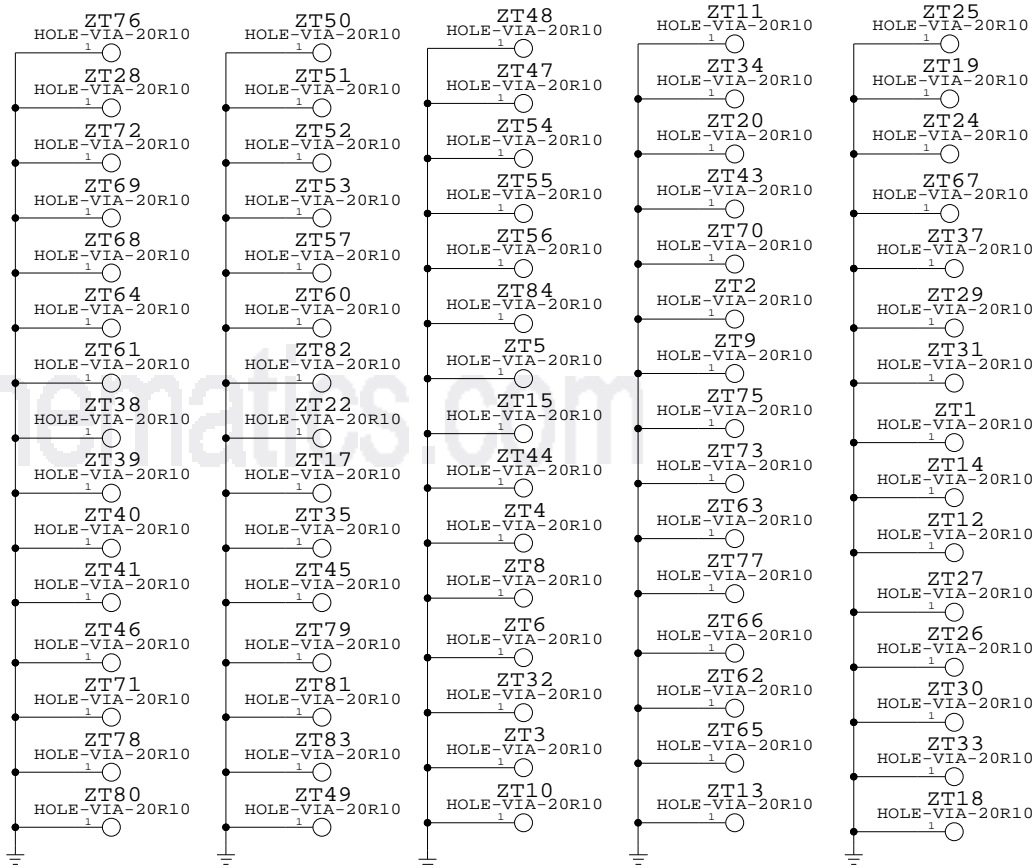
#### INVERTER



#### MECH. HOLES



## GROUND VIAS



## BOARD INFORMATION

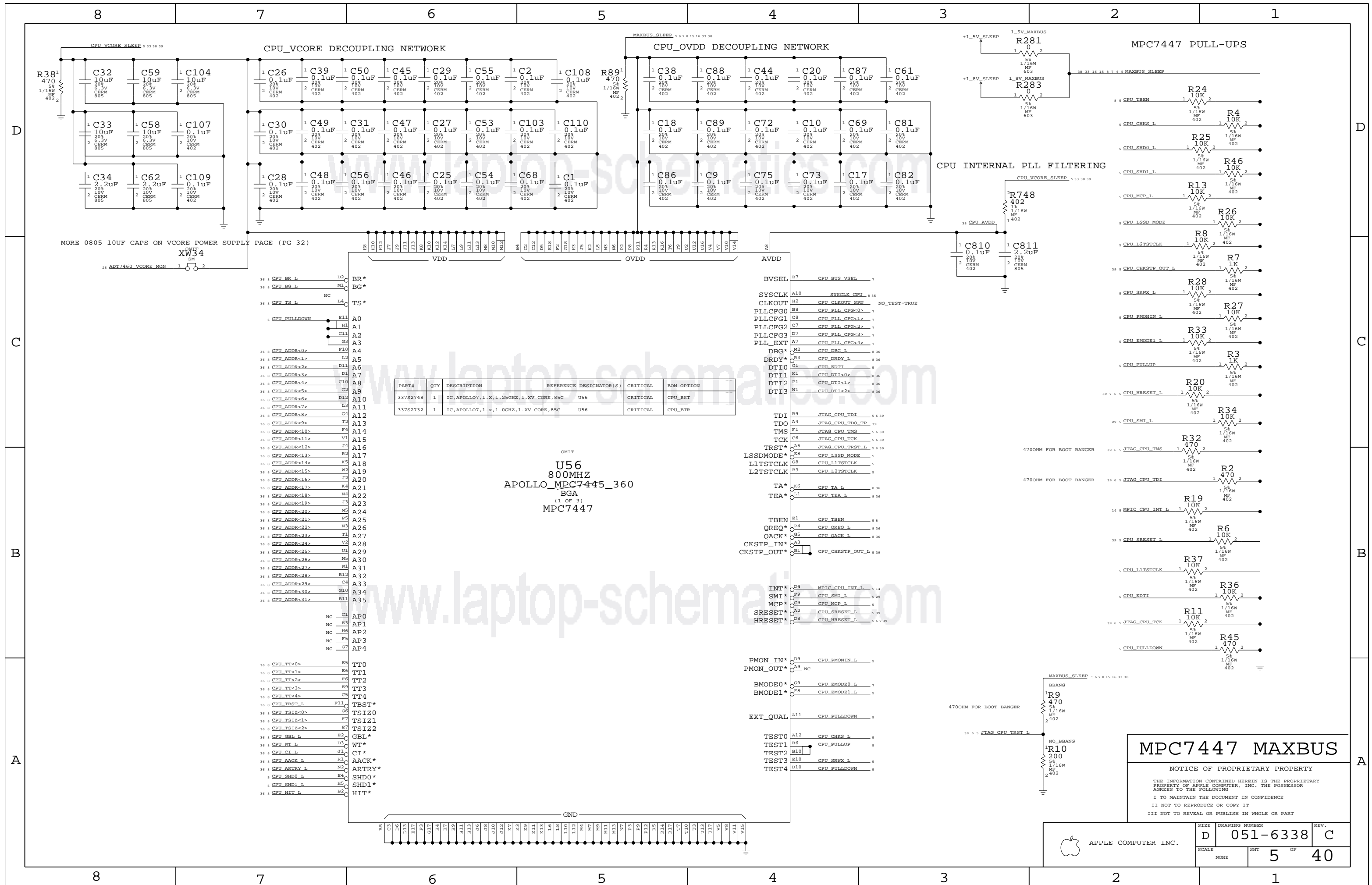
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SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE	SHT	OF
NONE	4	40



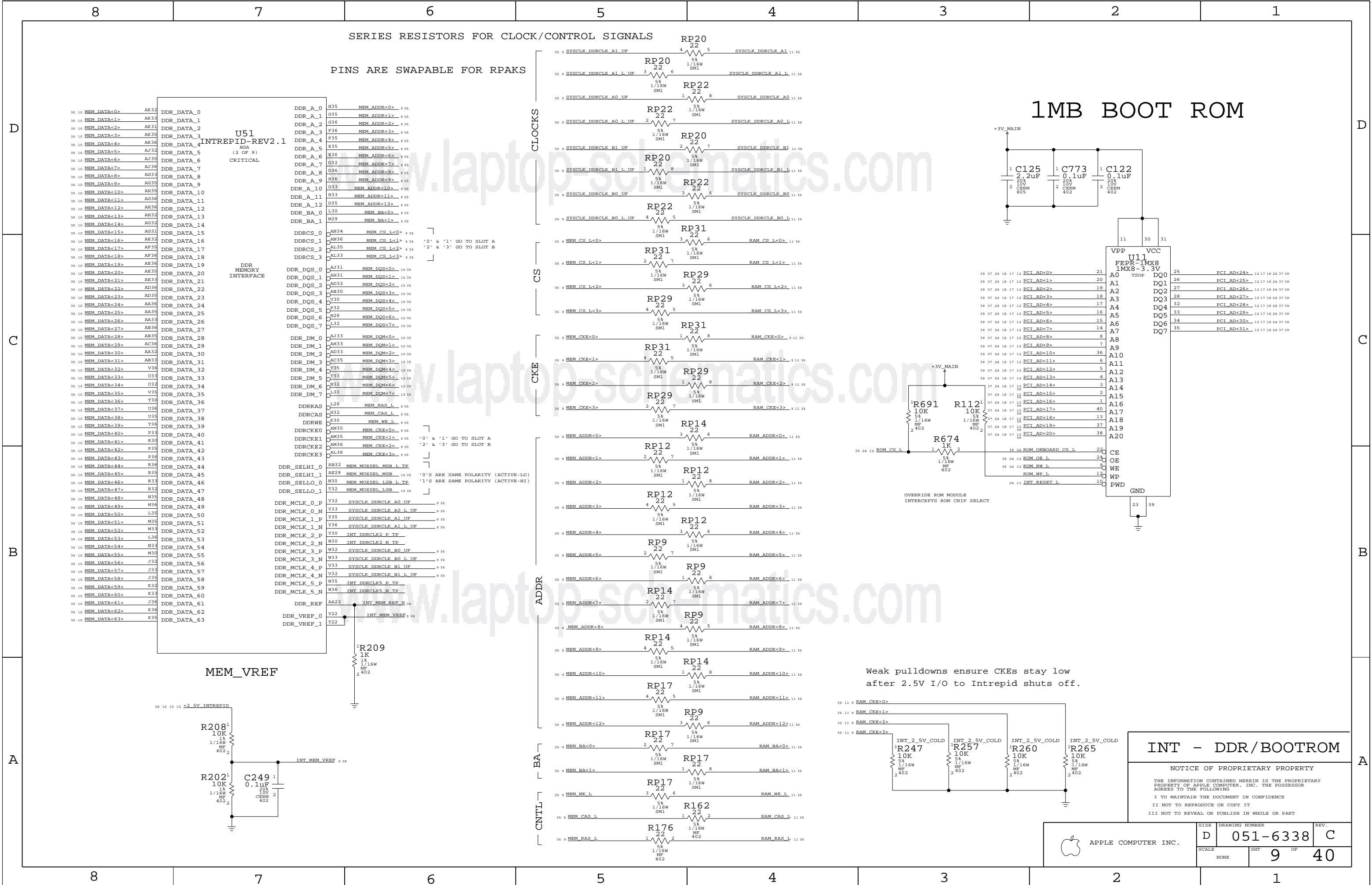


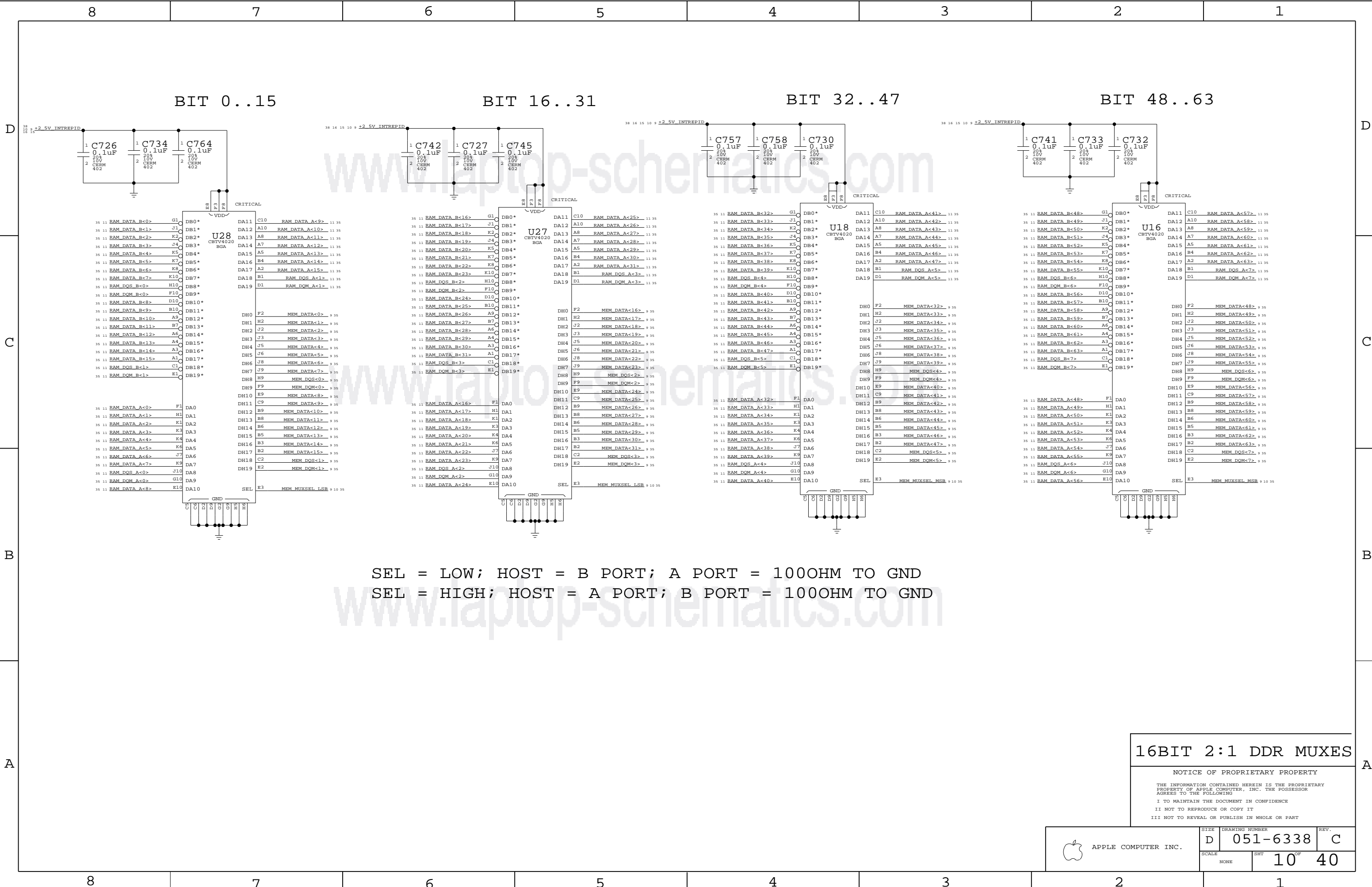










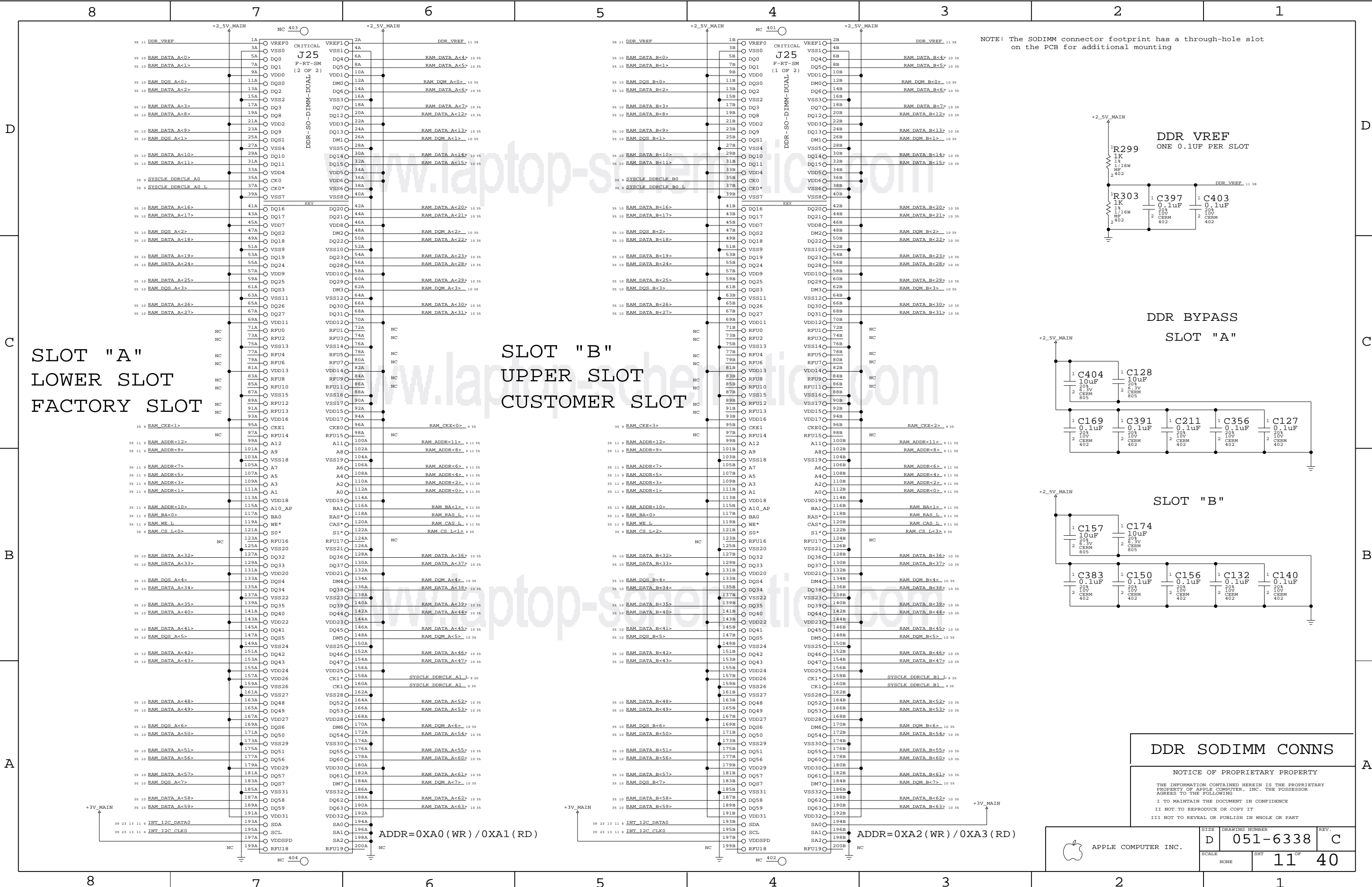


SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND  
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND

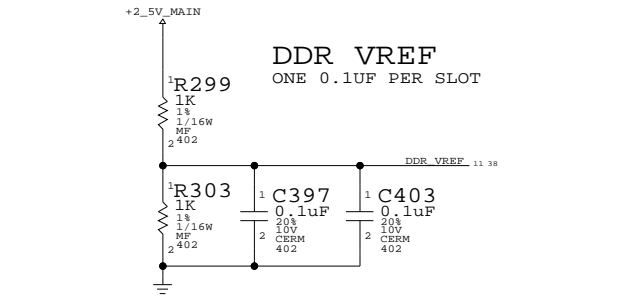
16BIT 2:1 DDR MUXES

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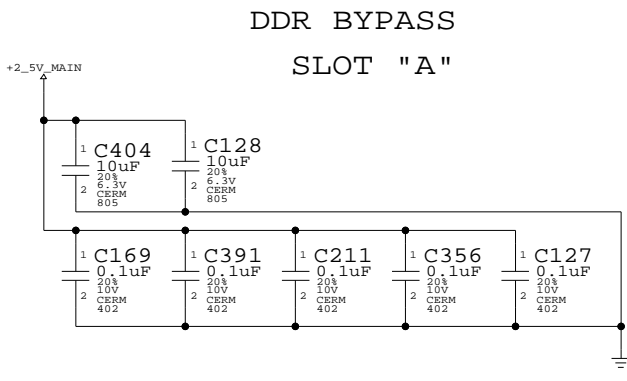
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6338	C
SCALE	SHT	10 <sup>OF</sup>	40
NONE			



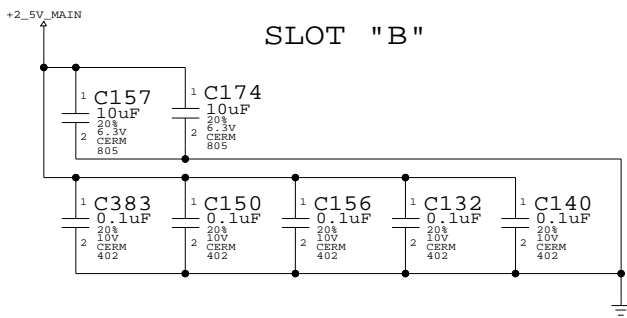
NOTE: The SODIMM connector footprint has a through-hole slot on the PCB for additional mounting



DDR VREF  
ONE 0.1UF PER SLOT



DDR BYPASS  
SLOT "A"



SLOT "B"

DDR SODIMM CONNS

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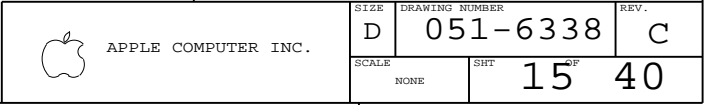
SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE	SHT	11 OF 40
NONE		

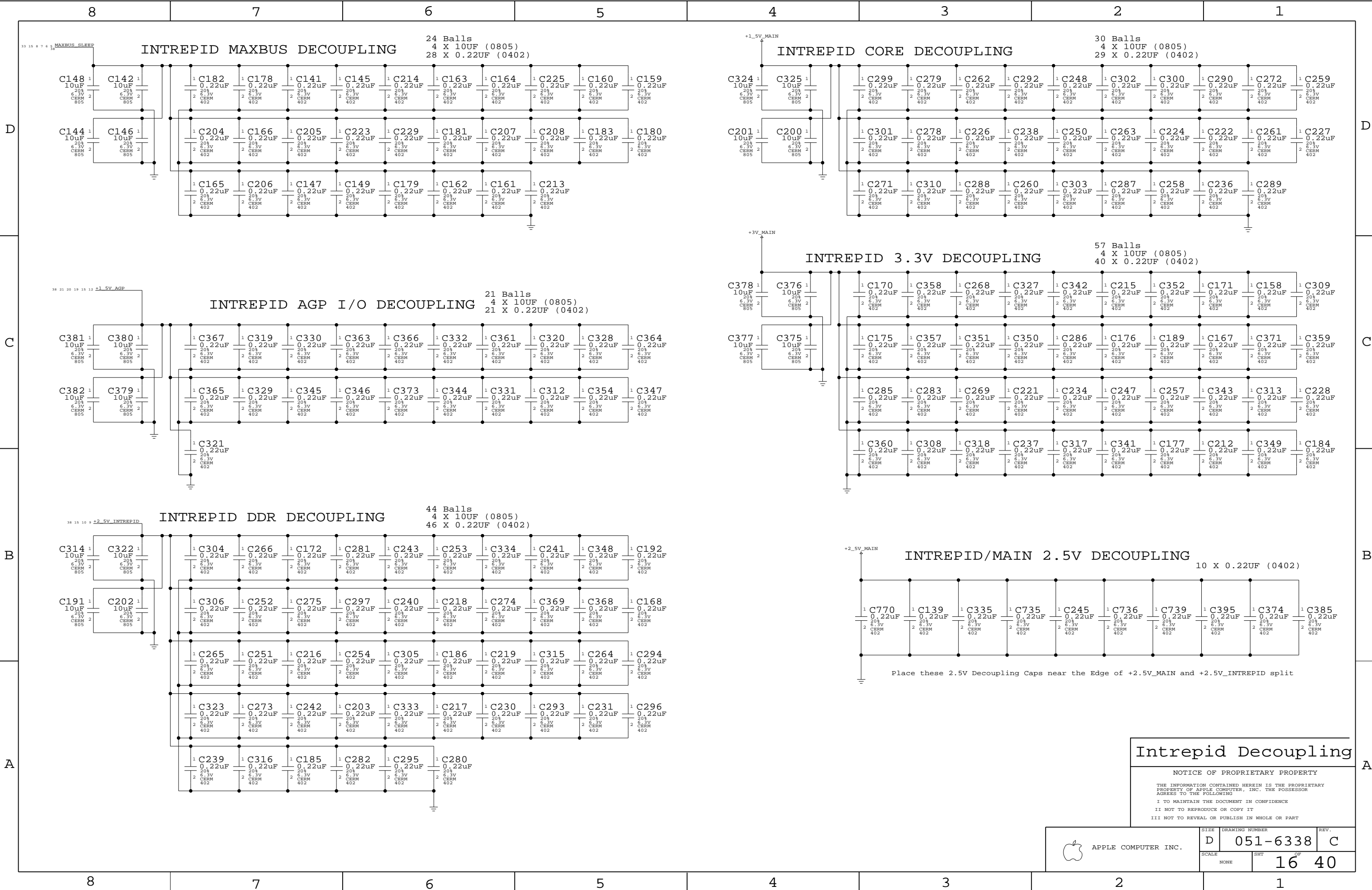












# Intrepid Decoupling

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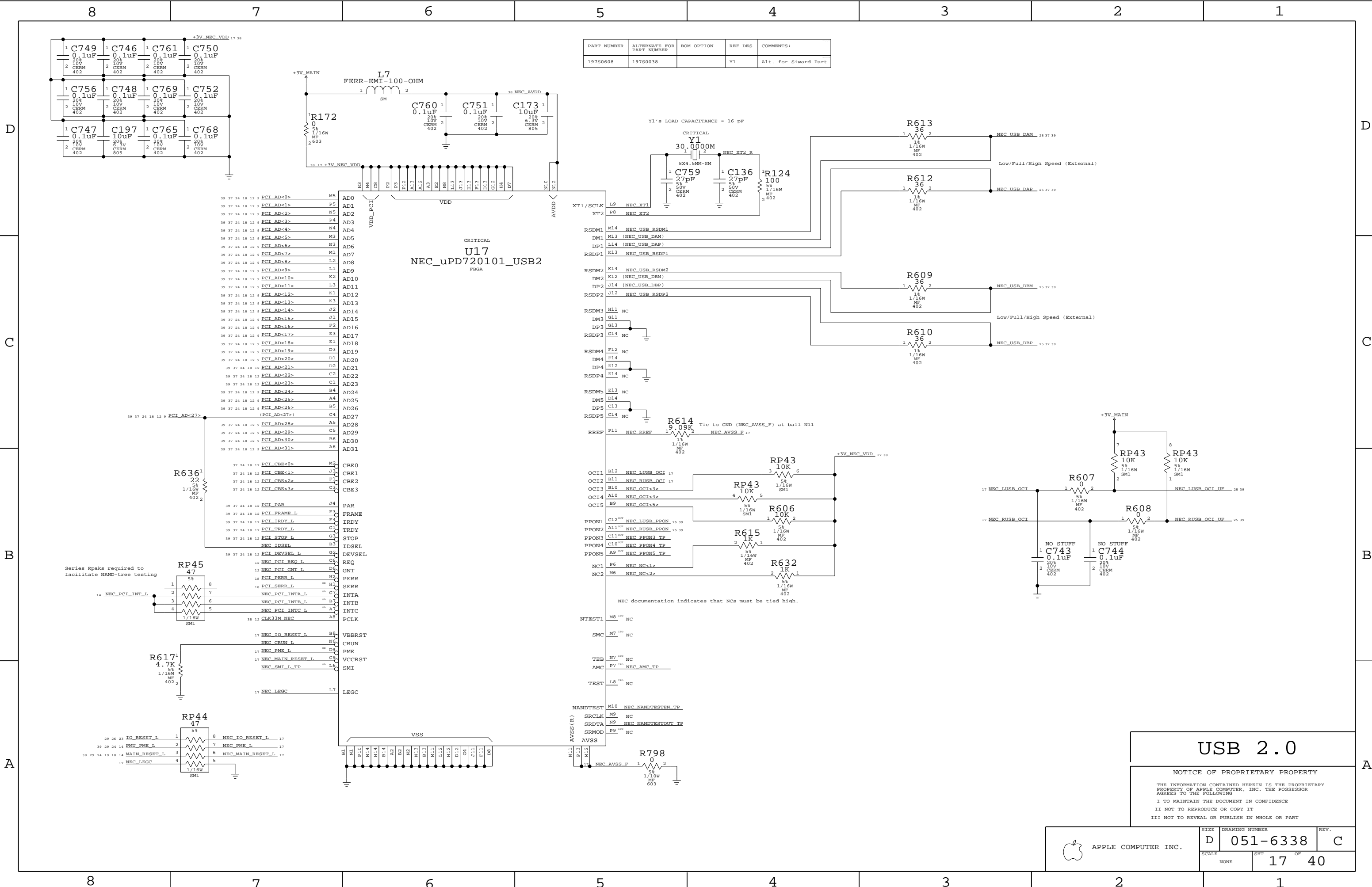
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6338	C
SCALE		SHT	OF
NONE		16	40





PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
197S0608	197S0038		Y1	Alt. for Siward Part

USB 2.0

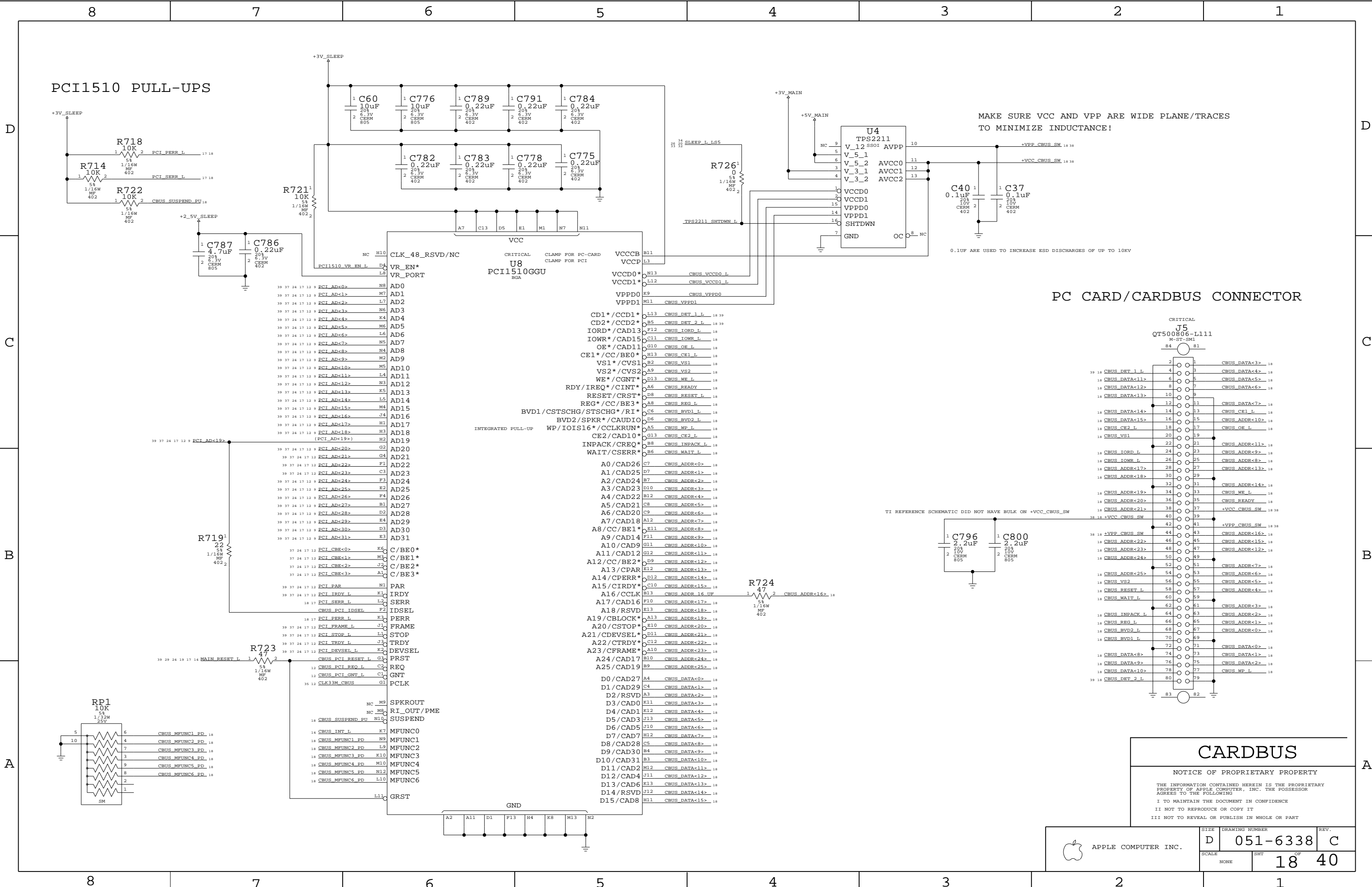
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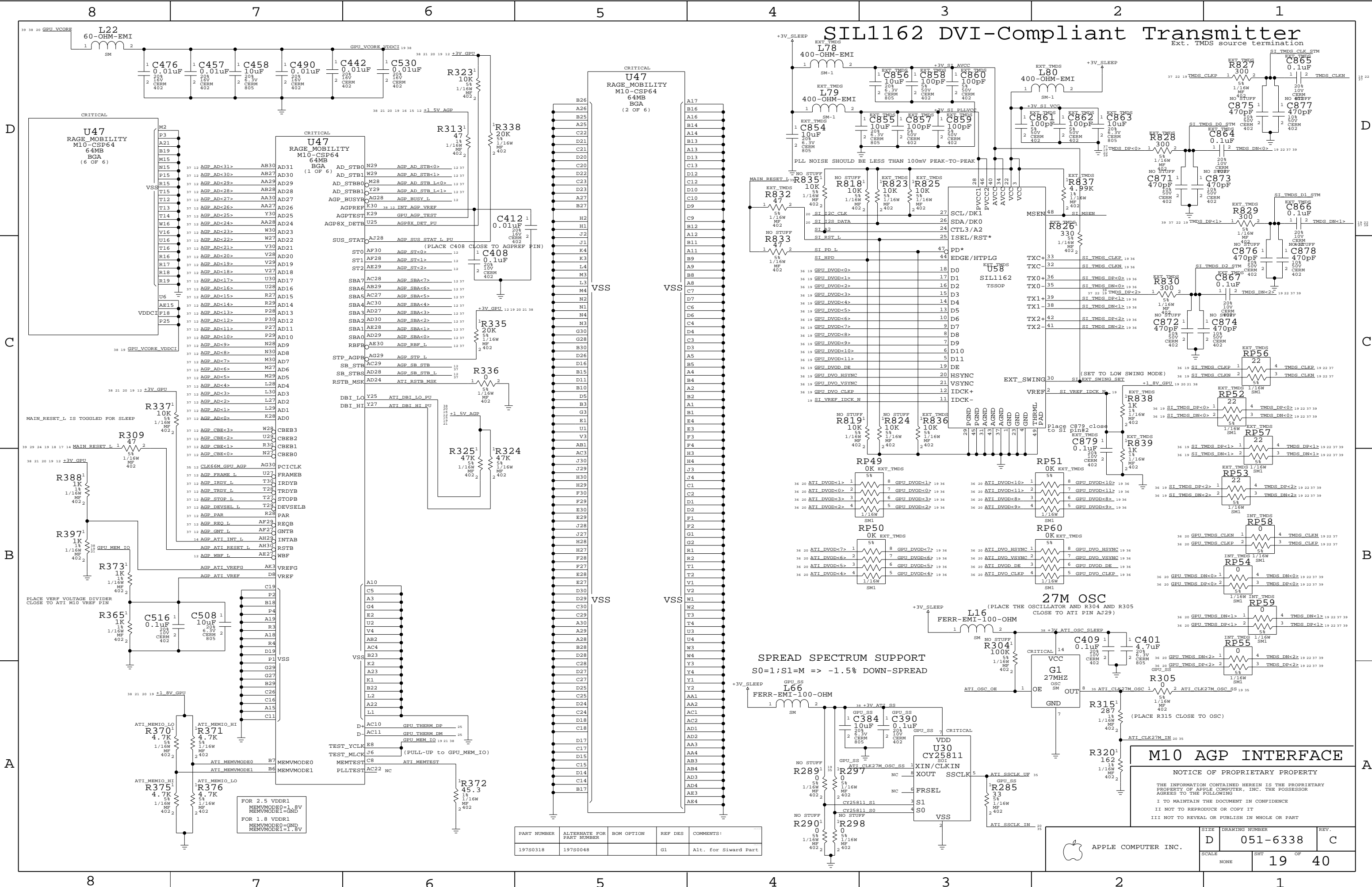
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0318	197S0048		G1	Alt. for Siward Part

APPLE COMPUTER INC.

SIZE

D

SCALE

NONE

DRAWING NUMBER

051-6338

SHT

19

OF

40

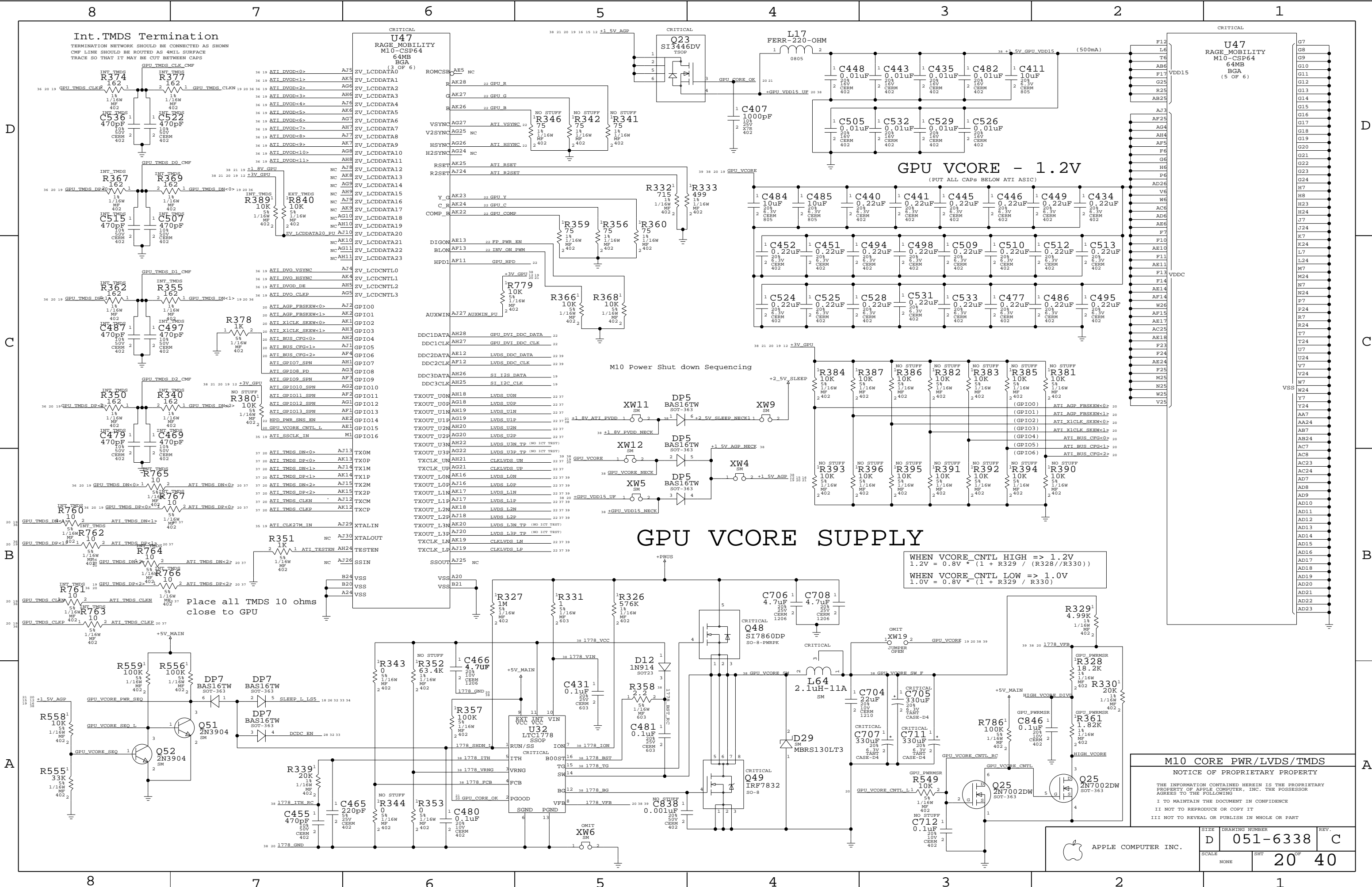
REV.

C

M10 AGP INTERFACE

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Int.TMDS Termination

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN  
CMP LINE SHOULD BE ROUTED AS ANTL SURFACE  
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

GPU VCORE - 1.2V

(PUT ALL CAPS BELOW ATI ASIC)

GPU VCORE SUPPLY

WHEN VCORE\_CNTL HIGH => 1.2V  
1.2V = 0.8V \* (1 + R329 / (R328//R330))  
WHEN VCORE\_CNTL LOW => 1.0V  
1.0V = 0.8V \* (1 + R329 / R330)

M10 CORE PWR/LVDS/TMDS

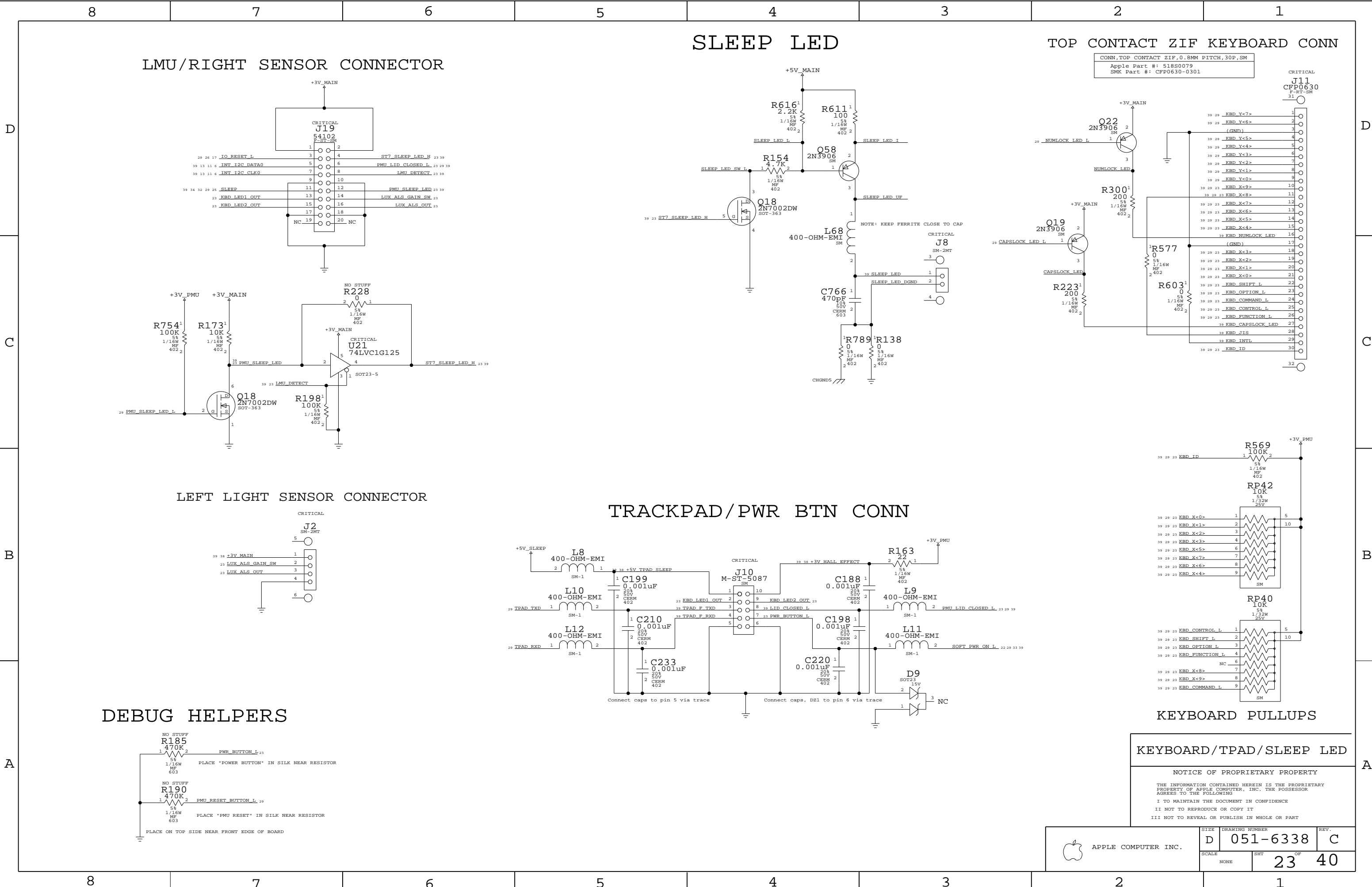
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KEYBOARD/TPAD/SLEEP LED

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	D	051-6338	C
SCALE	NONE	SHT	23 OF 40





# LEFT I/O & AUDIO BOARD (LIO)

# USB MODEM/SOFT MODEM

# RIGHT USB BOARD

# SERIAL DEBUG INTERFACE

# FAN INTERFACE FAN CONTROLLER

D

D

C

C

B

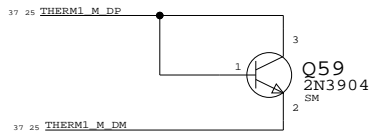
B

A

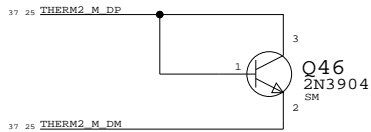
A

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0154	1	CONN,PLUG,0.5MM PITCH,1.5MM STACK,40P,GOLD	J3	CRITICAL	?

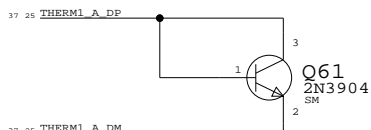
PLACE CLOSE TO CPU  
MAIN1



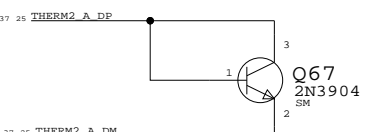
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY  
MAIN2



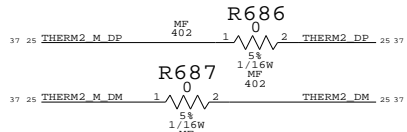
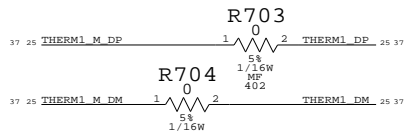
PLACE UNDERNEATH UPPER RAM  
ALTERNATE1



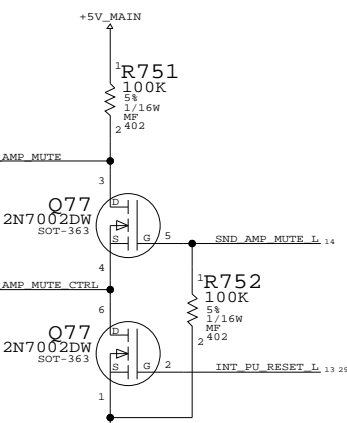
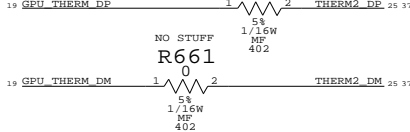
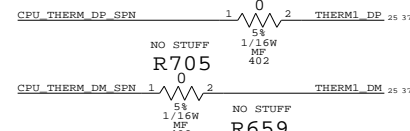
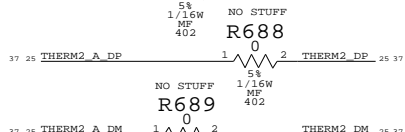
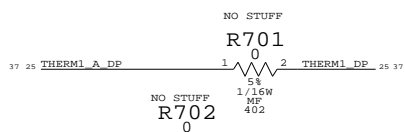
PLACE CLOSE TO BATTERY CHARGER/VCORE  
ALTERNATE2



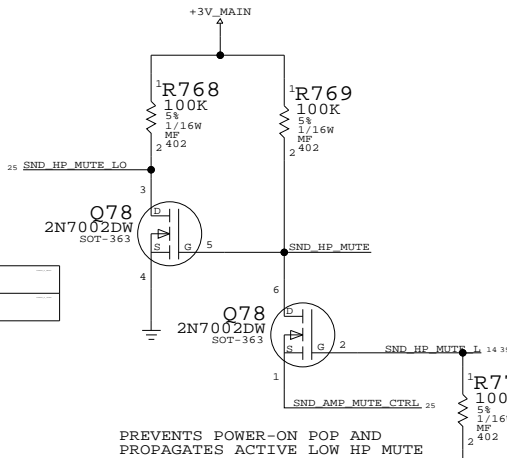
KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER



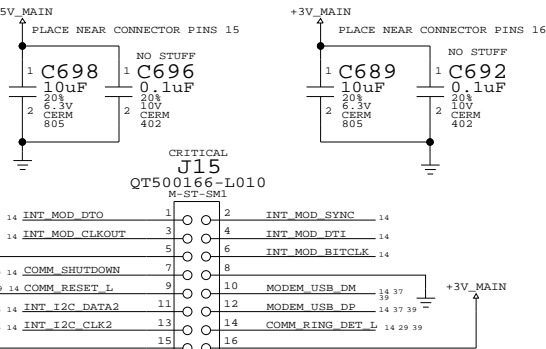
KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER



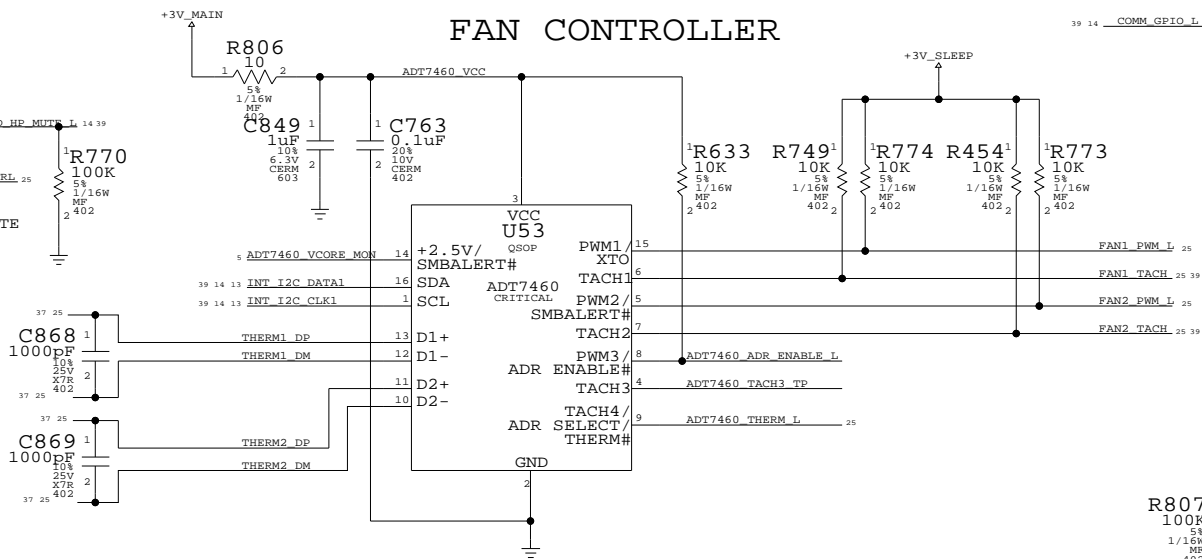
PREVENTS POWER-ON POP AND  
GENERATES ACTIVE HIGH SPKR MUTE



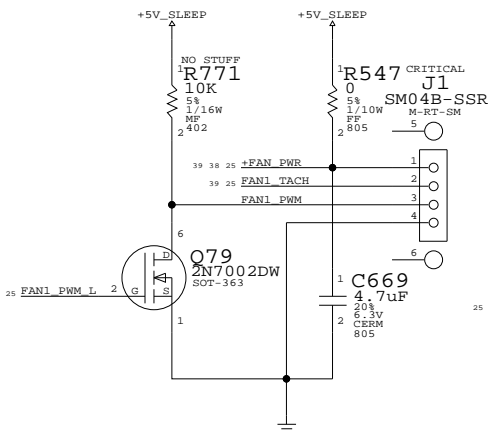
PREVENTS POWER-ON POP AND  
PROPAGATES ACTIVE LOW HP MUTE



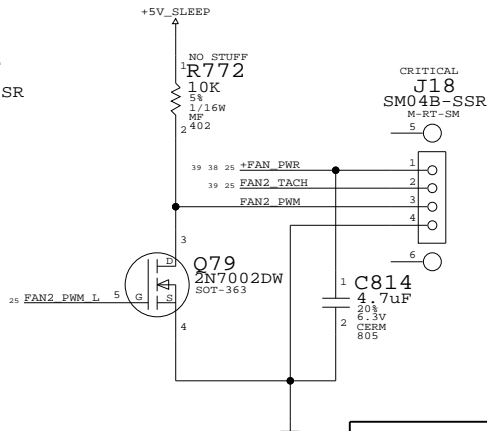
MODEM I2C ADDR ASSIGNED VIA FLEX CABLE



## CPU FAN



## GPU FAN



FAN/MODEM/SOUND/BACKUP BATT. .

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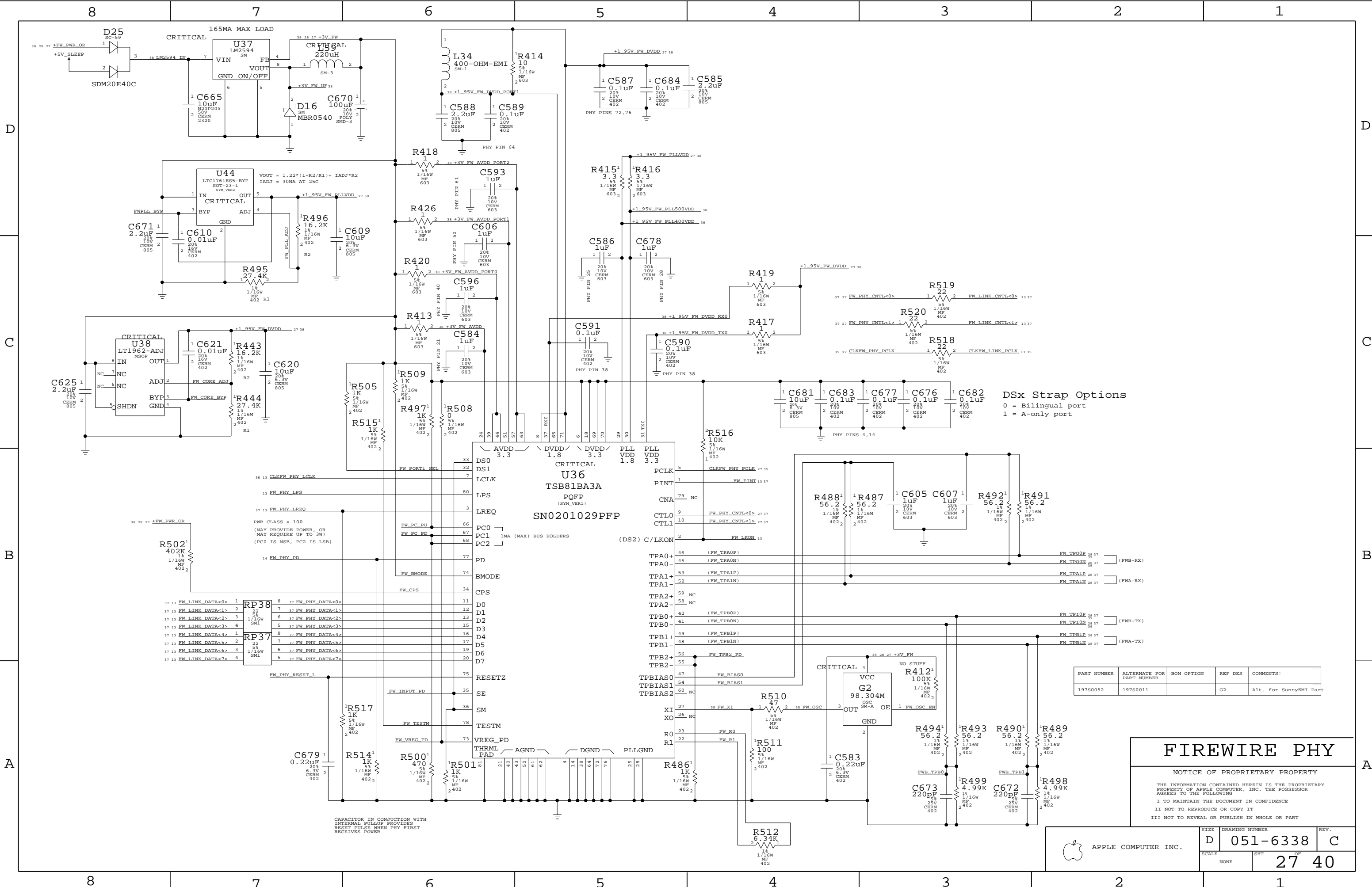


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SIZE D DRAWING NUMBER 051-6338 REV. C

SCALE NONE SHT 25 OF 40





DSx Strap Options  
0 = Bilingual port  
1 = A-only port

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0052	197S0011		G2	Alt. for SunnyEMI Part

**FIREWIRE PHY**

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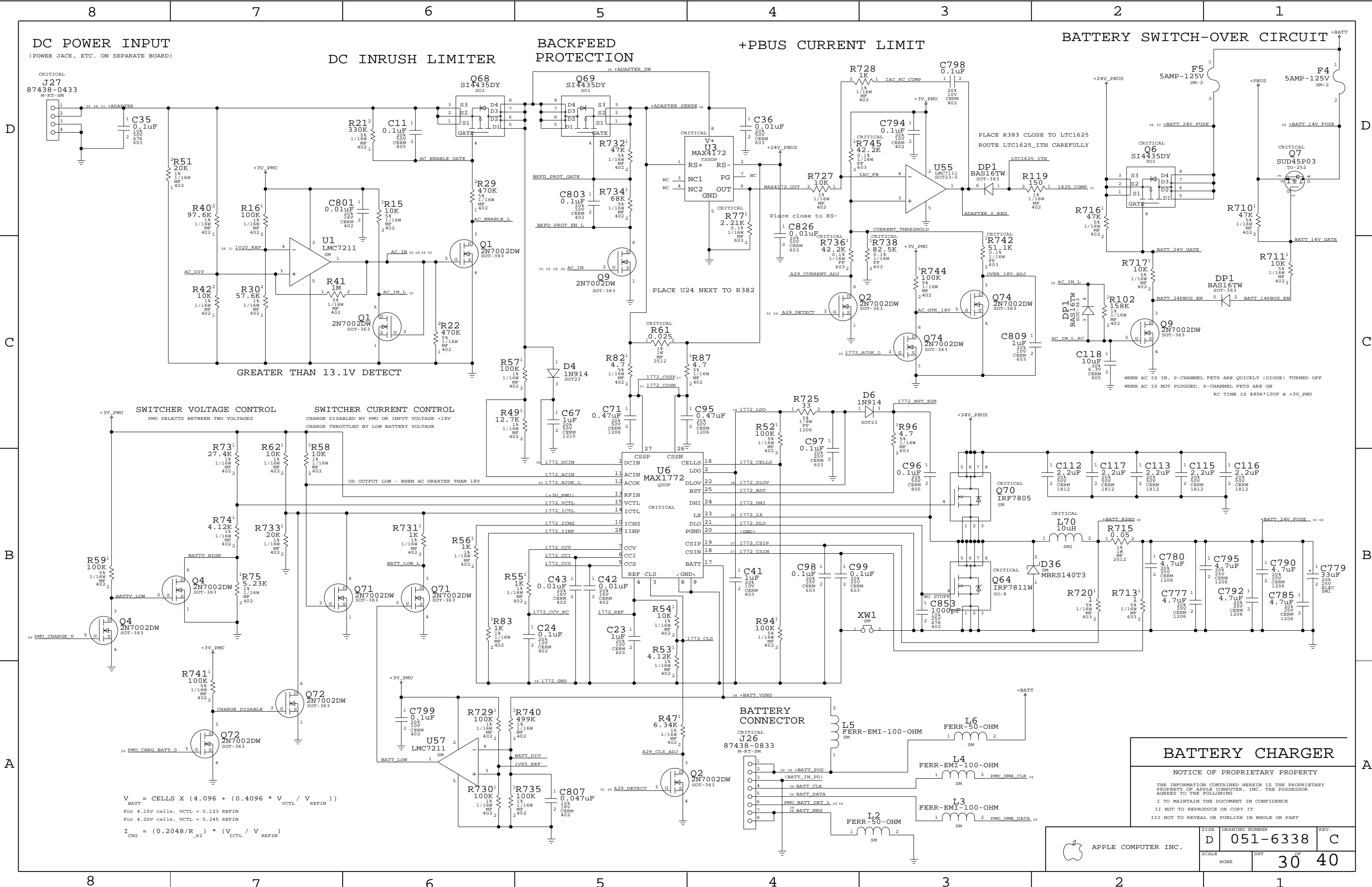
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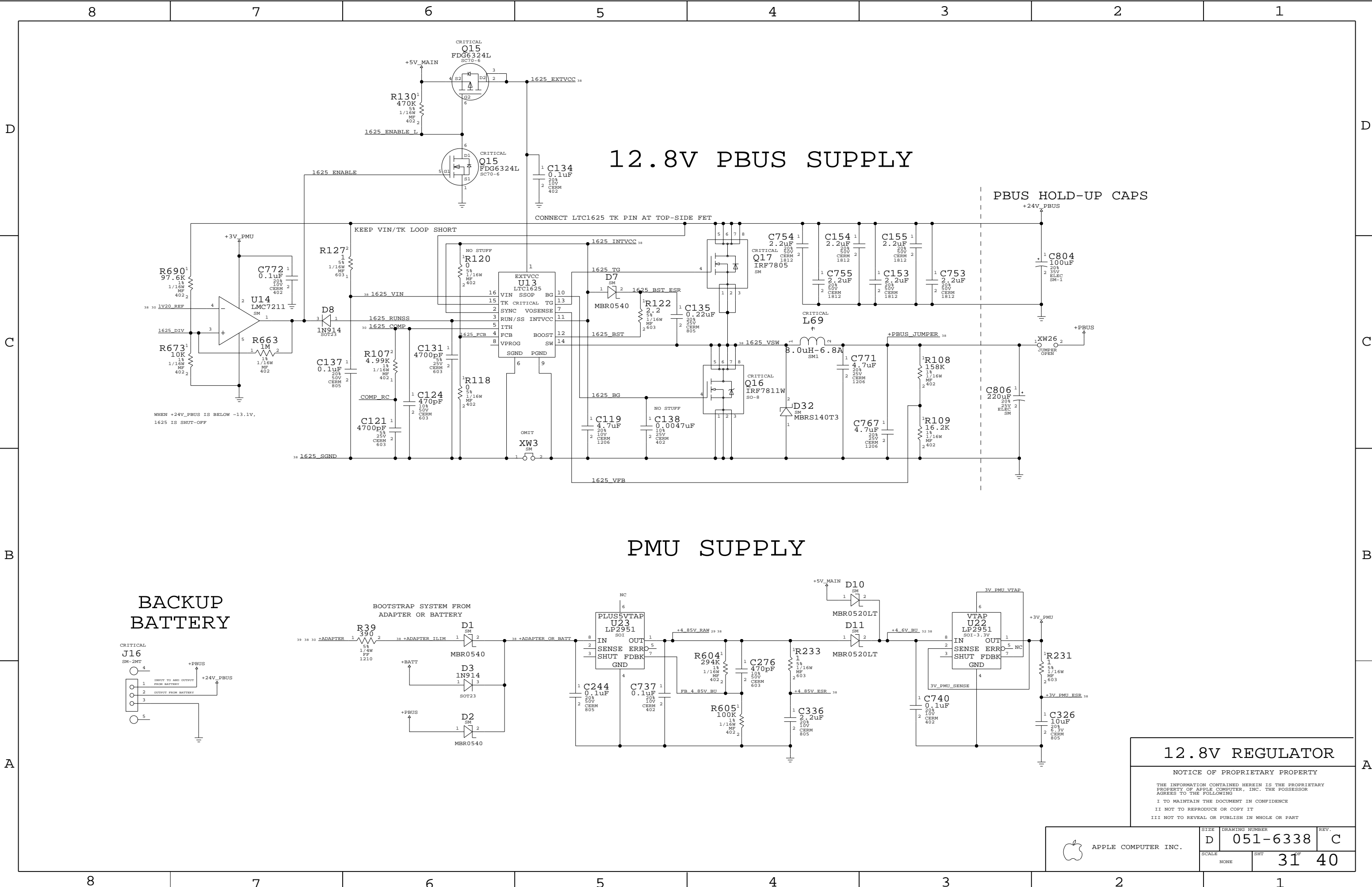
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6338	C
SCALE	SHT		OF
	NONE		27 40











# 12.8V PBUS SUPPLY

# PMU SUPPLY

## BACKUP BATTERY

## 12.8V REGULATOR

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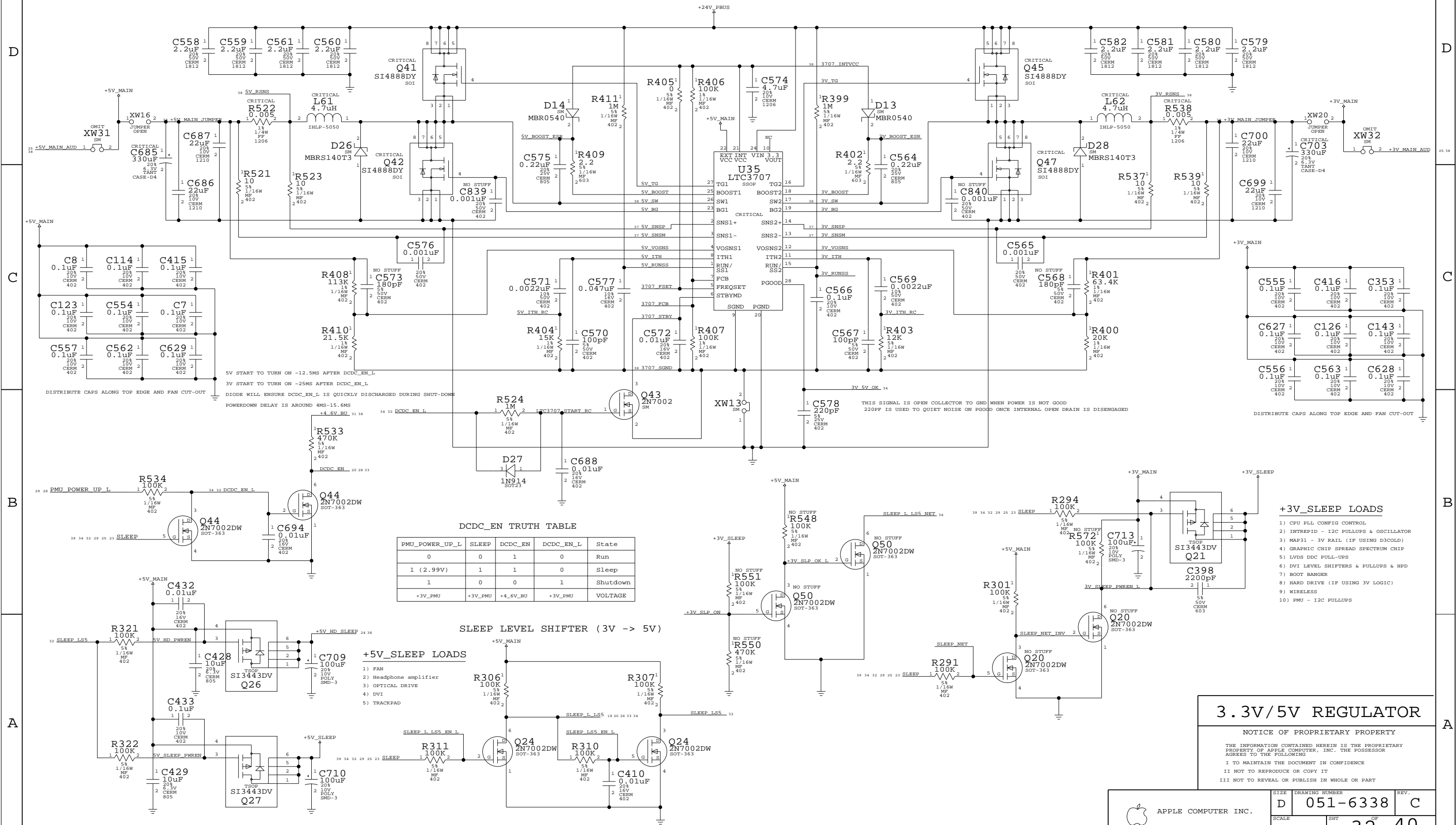
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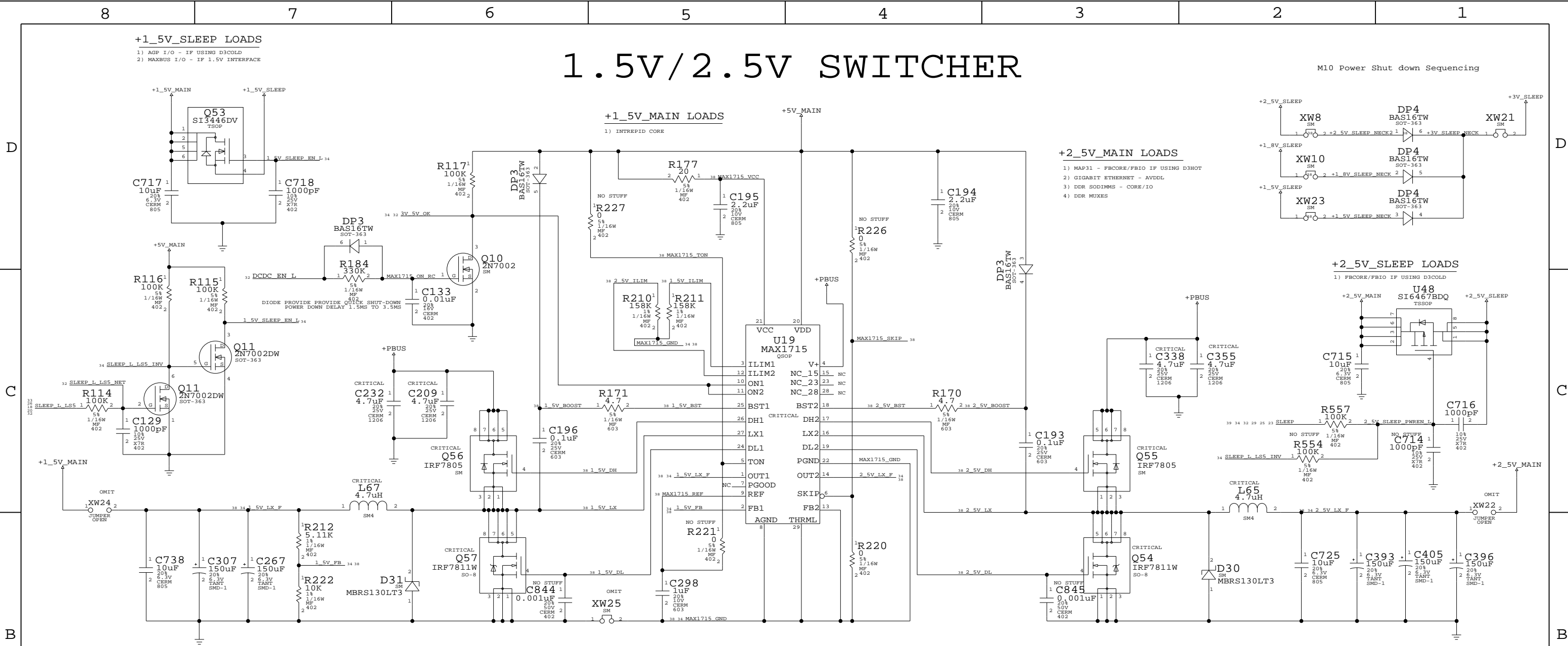
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6338	C
SCALE		SHT	31 40
NONE			

# 3.3V/5V MAIN SUPPLY

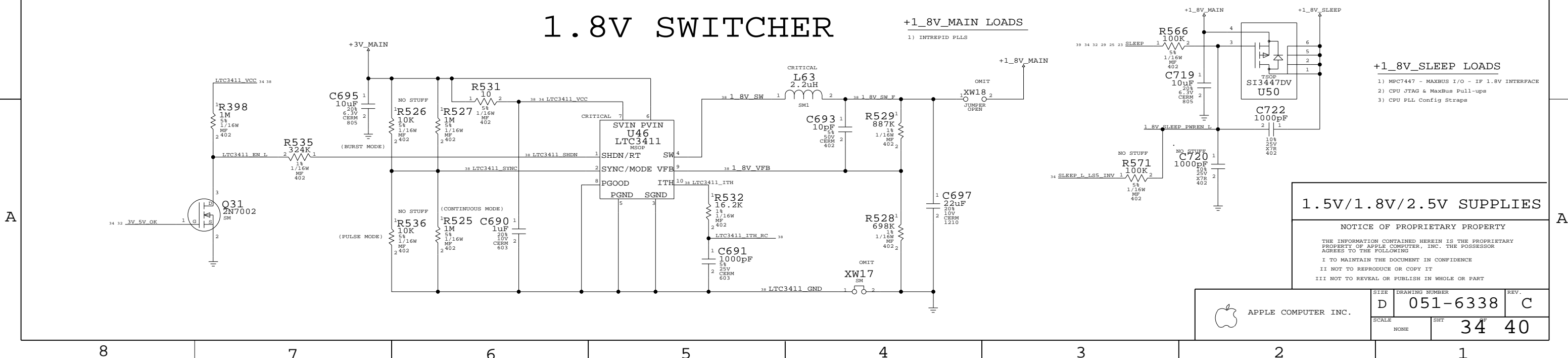




1.5V/2.5V SWITCHER



1.8V SWITCHER



<







8					7					6					5					4					3					2					1																																					
POWER NET CONSTRAINTS																									SIGNAL CONSTRAINTS - PAGE 3																																															
GROUP					SIG_NAME					VOLTAGE					MIN_LINE_WIDTH					MIN_NECK_WIDTH					GROUP					SIG_NAME					VOLTAGE					MIN_LINE_WIDTH					MIN_NECK_WIDTH																											
D	MAIN/SLEEP	+24V PBUS VOLTAGE=24V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 39																							CPU	CPU_VCORE_SLEEP VOLTAGE=1.4V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 5 33 39																							LTC1625 14V SWITCHER	1625_VIN VOLTAGE=24V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 31																						
		+BATT VOLTAGE=12.6V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 39																								CPU_AVDD VOLTAGE=1.4V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 5																								1625_VSM VOLTAGE=14V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 31																						
		+PBUS VOLTAGE=12.8V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 39																								MAXBUS_SLEEP VOLTAGE=1.8V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 5 6 7 8 15 16 33																								+PBUS_JUMPER VOLTAGE=14V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 31																						
		+5V_MAIN VOLTAGE=5V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 39																																																1625_EXTVCC VOLTAGE=5V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 31																						
		+5V_SLEEP VOLTAGE=5V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 39																																																1625_INTVCC VOLTAGE=5V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 31																						
		+3V_MAIN VOLTAGE=3.3V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 23 39																																																1625_SGND VOLTAGE=0V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 31																						
		+3V_SLEEP VOLTAGE=3.3V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=6 39																																																1V20_REF VOLTAGE=1.2V MIN_LINE_WIDTH=15 MIN_NECK_WIDTH=10 30 31																						
		+3V_PMU VOLTAGE=3.3V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 39																																																3707_INTVCC VOLTAGE=5V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 32																						
		+2.5V_MAIN VOLTAGE=2.5V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 39																																																5V_SW VOLTAGE=5V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 32																						
		+2.5V_SLEEP VOLTAGE=2.5V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 39																																																+5V_MAIN_JUMPER VOLTAGE=5V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 32																						
		+1.8V_MAIN VOLTAGE=1.8V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=6 39																																																3V_SW VOLTAGE=3.3V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 32																						
		+1.8V_SLEEP VOLTAGE=1.8V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 39																																																3V_RSNS VOLTAGE=3.3V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 32																						
		+1.5V_MAIN VOLTAGE=1.5V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 39																																																+3V_MAIN_JUMPER VOLTAGE=3.3V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 32																						
		+1.5V_SLEEP VOLTAGE=1.5V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 39																																																3707_SGND VOLTAGE=0V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 32																						
		+1.5V_LDO VOLTAGE=1.5V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 39																																																2.5V_LX VOLTAGE=2.5V MIN_LINE_WIDTH=50 MIN_NECK_WIDTH=10 34																						
		+1.5V_SLEEP_VIN VOLTAGE=1.5V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 39																																																2.5V_LX_F VOLTAGE=2.5V MIN_LINE_WIDTH=50 MIN_NECK_WIDTH=10 34																						
C	ADAPTER	+ADAPTER VOLTAGE=24V MIN_LINE_WIDTH=50 MIN_NECK_WIDTH=10 30 31 39																							REFERENCE	INT_MEM_VREF VOLTAGE=1.25V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 9																							MAX1715 2.5V SWITCHER	1.5V_FB VOLTAGE=1.5V MIN_LINE_WIDTH=8 MIN_NECK_WIDTH=10 34																						
		+ADAPTER_SW VOLTAGE=24V MIN_LINE_WIDTH=50 MIN_NECK_WIDTH=10 38																								INT_AGP_VREF VOLTAGE=1.25V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 12 19																								1.5V_LX_F VOLTAGE=1.5V MIN_LINE_WIDTH=50 MIN_NECK_WIDTH=10 34																						
		+ADAPTER_SW VOLTAGE=24V MIN_LINE_WIDTH=50 MIN_NECK_WIDTH=10 38																								INT_MEM_REF_H VOLTAGE=0V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 9																								1.5V_LX_F VOLTAGE=1.5V MIN_LINE_WIDTH=50 MIN_NECK_WIDTH=10 34																						
		+ADAPTER_SENSE VOLTAGE=24V MIN_LINE_WIDTH=50 MIN_NECK_WIDTH=10 30																								UIDE_REF VOLTAGE=0V MIN_LINE_WIDTH=8 MIN_NECK_WIDTH=10 13																								1.5V_BST VOLTAGE=5V MIN_LINE_WIDTH=15 MIN_NECK_WIDTH=10 34																						
																																																		1.5V_BOOST VOLTAGE=5V MIN_LINE_WIDTH=15 MIN_NECK_WIDTH=10 34																						
																																																		1.5V_DH VOLTAGE=1.5V MIN_LINE_WIDTH=20 MIN_NECK_WIDTH=10 34																						
																																																		1.5V_DL VOLTAGE=1.5V MIN_LINE_WIDTH=20 MIN_NECK_WIDTH=10 34																						
																																																		1.5V_ILIM VOLTAGE=5V MIN_LINE_WIDTH=8 MIN_NECK_WIDTH=10 34																						
																																																		2.5V_ILIM VOLTAGE=2.5V MIN_LINE_WIDTH=8 MIN_NECK_WIDTH=10 34																						
																																																		MAX1715_TON VOLTAGE=5V MIN_LINE_WIDTH=20 MIN_NECK_WIDTH=10 34																						
																																																		MAX1715_SKIP VOLTAGE=0V MIN_LINE_WIDTH=30 MIN_NECK_WIDTH=10 34																						
																																																		MAX1715_REF VOLTAGE=2.0V MIN_LINE_WIDTH=8 MIN_NECK_WIDTH=10 34																						
																																																		MAX1715_VCC VOLTAGE=5V MIN_LINE_WIDTH=20 MIN_NECK_WIDTH=10 34																						
																																																		MAX1715_GND VOLTAGE=0V MIN_LINE_WIDTH=30 MIN_NECK_WIDTH=10 34																						
																																																		VCORE_VCC VOLTAGE=5V MIN_LINE_WIDTH=20 MIN_NECK_WIDTH=10 33																						
																																																		VCORE_LX VOLTAGE=1.4V MIN_LINE_WIDTH=200 MIN_NECK_WIDTH=10 33																						
B	BATTERY CHARGER	+BATT_POS VOLTAGE=16.8V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 30 39																							AIRPORT CARDBUS ATI M10	+3V_AIRPORT VOLTAGE=3.3V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 39																							LTC1778	VCORE_DH VOLTAGE=5V MIN_LINE_WIDTH=20 MIN_NECK_WIDTH=10 33																						
		BATT_NEG VOLTAGE=0V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 39																								+VCC_CBUS_SW VOLTAGE=3.3V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 18																								VCORE_DL VOLTAGE=5V MIN_LINE_WIDTH=15 MIN_NECK_WIDTH=10 33																						
		1772_DCIN VOLTAGE=24V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 30																								+VFP_CBUS_SW VOLTAGE=5V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 18																								VCORE_BOOST VOLTAGE=5V MIN_LINE_WIDTH=15 MIN_NECK_WIDTH=10 33																						
		1772_LX VOLTAGE=12.6V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 30																								GPU_VCORE VOLTAGE=1.2V MIN_LINE_WIDTH=30 MIN_NECK_WIDTH=10 19 20 39																								VCORE_BST VOLTAGE=5V MIN_LINE_WIDTH=15 MIN_NECK_WIDTH=10 33																						
		+BATT_14V_FUSE VOLTAGE=12.6V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 30																								+3V_GPU VOLTAGE=3.3V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 12 19 20 21																								VCORE_ILIM VOLTAGE=5V MIN_LINE_WIDTH=8 MIN_NECK_WIDTH=10 33																						
		+BATT_RSN VOLTAGE=12.6V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 30																								+3V_GPU_FLT VOLTAGE=3.3V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 21																								VCORE_REF VOLTAGE=5V MIN_LINE_WIDTH=8 MIN_NECK_WIDTH=10 33																						
		+BATT_VSNS VOLTAGE=12.6V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 30																								+2.5V_GPU VOLTAGE=2.5V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 21																								VCORE_TON VOLTAGE=5V MIN_LINE_WIDTH=8 MIN_NECK_WIDTH=10 33																						
		1772_LDO VOLTAGE=5.4V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 30																								GPU_MEM_IO VOLTAGE=2.5V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 21																								VCORE_CC VOLTAGE=1.4V MIN_LINE_WIDTH=8 MIN_NECK_WIDTH=10 33																						
		1772_DLOV VOLTAGE=5.4V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 30																								GPU_MEM_IO_TO_FLT VOLTAGE=2.5V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 21																								VCORE_FB VOLTAGE=1.4V MIN_LINE_WIDTH=8 MIN_NECK_WIDTH=10 33 39																						
		1772_GND VOLTAGE=0V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 30																								+2.5V_GPU_MEMCORE VOLTAGE=2.5V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 21																								VCORE_TIME VOLTAGE=1.4V MIN_LINE_WIDTH=8 MIN_NECK_WIDTH=10 33																						
		+ADAPTER_ILIM VOLTAGE=24V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 31																								+1.8V_GPU VOLTAGE=1.8V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 19 20 21																								VCORE_VGATE VOLTAGE=0V MIN_LINE_WIDTH=8 MIN_NECK_WIDTH=10 33																						
		+ADAPTER_OR_BATT VOLTAGE=24V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 31																								+1.5V_AGP VOLTAGE=1.5V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 12 15 16 19 20 21																								VCORE_GND VOLTAGE=0V MIN_LINE_WIDTH=30 MIN_NECK_WIDTH=10 33																						
		+4.85V_RAW VOLTAGE=4.85V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 29 31																								+1.8V_ATI_PVDD VOLTAGE=1.8V MIN_LINE_WIDTH=20 MIN_NECK_WIDTH=10 20 21																								VCORE_GNDSNS VOLTAGE=0V MIN_LINE_WIDTH=8 MIN_NECK_WIDTH=10 33																						
		+4.6V_BU VOLTAGE=4.6V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 31 32																								+1.5V_AGP_GPU VOLTAGE=1.5V MIN_LINE_WIDTH=20 MIN_NECK_WIDTH=10 21																								VCORE_SNS VOLTAGE=1.4V MIN_LINE_WIDTH=8 MIN_NECK_WIDTH=10 33																						
		+4.85V_ESR VOLTAGE=4.85V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 31																								+1.5V_GPU_VDD15 VOLTAGE=1.5V MIN_LINE_WIDTH=20 MIN_NECK_WIDTH=10 20																								VCORE_GNDDIV VOLTAGE=0V MIN_LINE_WIDTH=8 MIN_NECK_WIDTH=10 33																						
		+3V_PMU_ESR VOLTAGE=3.3V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 25 29																								+1.8V_GPU_PIL VOLTAGE=1.8V MIN_LINE_WIDTH=15 MIN_NECK_WIDTH=10 21																								VCORE_GNDA VOLTAGE=0V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 33																						
A	MISC	+5V_HD_SLEEP VOLTAGE=5V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 24 32																							ETHERNET 88E1111 NEC USB2.0	+1.8V_GPU_VDDI VOLTAGE=1.8V MIN_LINE_WIDTH=15 MIN_NECK_WIDTH=10 21																							LTC3411	LTC3411_VCC VOLTAGE=3.3V MIN_LINE_WIDTH=20 MIN_NECK_WIDTH=10 34																						
		+HD_LOGIC_SLEEP VOLTAGE=3.3V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 24																								GPU_VCORE_VDDCI VOLTAGE=1.2V MIN_LINE_WIDTH=15 MIN_NECK_WIDTH=10 19																								LTC3411_GND VOLTAGE=0V MIN_LINE_WIDTH=30 MIN_NECK_WIDTH=10 34																						
		+5V_TPAD_SLEEP VOLTAGE=5V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 23 39																								+2.5V_GPU_AZVDD VOLTAGE=2.5V MIN_LINE_WIDTH=15 MIN_NECK_WIDTH=10 21																								1.8V_SW VOLTAGE=1.8V MIN_LINE_WIDTH=30 MIN_NECK_WIDTH=10 34																						
																										+1.8V_GPU_AVDD VOLTAGE=1.8V MIN_LINE_WIDTH=15 MIN_NECK_WIDTH=10 21																								1.8V_SW_F VOLTAGE=1.8V MIN_LINE_WIDTH=30 MIN_NECK_WIDTH=10 34																						
																										+1.8V_GPU_PNL1 VOLTAGE=1.8V MIN_LINE_WIDTH=15 MIN_NECK_WIDTH=10 21																								1.8V_VFB VOLTAGE=1.8V MIN_LINE_WIDTH=8 MIN_NECK_WIDTH=10 34																						
																										+1.8V_GPU_PNL10 VOLTAGE=1.8V MIN_LINE_WIDTH=15 MIN_NECK_WIDTH=10 21																								LTC3411_I1TH_RC VOLTAGE=12.8V MIN_LINE_WIDTH=12 MIN_NECK_WIDTH=12 28																						
																										+2.5V_GPU_MCLK VOLTAGE=2.5V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 21																								LTC3411_I1TH VOLTAGE=12.8V MIN_LINE_WIDTH=12 MIN_NECK_WIDTH=12 28																						
																										+1.8V_GPU_AVDD0 VOLTAGE=1.8V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 21																								LTC3411_SYNC VOLTAGE=12.8V MIN_LINE_WIDTH=12 MIN_NECK_WIDTH=12 28																						
																										+1.8V_GPU_MEMPLL VOLTAGE=1.8V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 21																								LTC3411_SHDN VOLTAGE=12.8V MIN_LINE_WIDTH=12 MIN_NECK_WIDTH=12 28																						
																										+3V_ATI_QSC_SLEEP VOLTAGE=3.3V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 19																								LTC1962_INT_VIN VOLTAGE=20 MIN_LINE_WIDTH=20 MIN_NECK_WIDTH=10 14																						
																										+3V_ATI_SS VOLTAGE=3.3V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 19																																														
																										+GPU_VDD15_UF VOLTAGE=1.5V MIN_LINE_WIDTH=20 MIN_NECK_WIDTH=10 20																																														
																										+2.5V_SLEEP_NECK1 VOLTAGE=2.5V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 20																																														
																										+3V_SLEEP_NECK VOLTAGE=3V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 34																																														
																										+1.5V_AGP_NECK VOLTAGE=1.5V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 20																																														
																										+1.8V_PVDD_NECK VOLTAGE=1.8V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 20																																														
A	VIDEO	GPU_VCORE_NECK VOLTAGE=1.2V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 20																							FW	+2.5V_SLEEP_NECK2 VOLTAGE=2.5V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 34																							LTC1962 INT PLLS	LTC1962_INT_VIN VOLTAGE=20 MIN_LINE_WIDTH=20 MIN_NECK_WIDTH=10 14																						
		+GPU_VDD15_NECK VOLTAGE=1.5V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 20																								+1.8V_SLEEP_NECK VOLTAGE=1.8V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 34																								LTC1962_INT_VIN VOLTAGE=20 MIN_LINE_WIDTH=20 MIN_NECK_WIDTH=10 14																						
		+2.5V_SLEEP_NECK VOLTAGE=3V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 34																								+1.5V_SLEEP_NECK VOLTAGE=1.5V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 34																																														
		+1.5V_AGP_NECK VOLTAGE=1.5V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 20																								+1.8V_ATI_TP_VDD VOLTAGE=1.8V MIN_LINE_WIDTH=20 MIN_NECK_WIDTH=10 21																																														
		+1.8V_PVDD_NECK VOLTAGE=1.8V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 20																								+1.8V_GPU_TP_PLL VOLTAGE=1.8V MIN_LINE_WIDTH=15 MIN_NECK_WIDTH=10 21																																														
		GPU_VCORE_NECK VOLTAGE=1.2V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 20																																																																						
		+GPU_VDD15_NECK VOLTAGE=1.5V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 20																																																																						
		+2.5V_SLEEP_NECK2 VOLTAGE=2.5V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 34																																																																						
		+1.8V_SLEEP_NECK VOLTAGE=1.8V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 34																																																																						
		+1.5V_SLEEP_NECK VOLTAGE=1.5V MIN_LINE_WIDTH=10 MIN_NECK_WIDTH=10 34																																																																						
		+1.8V_ATI_TP_VDD VOLTAGE=1.8V MIN_LINE_WIDTH=20 MIN_NECK_WIDTH=10 21																																																																						
		+1.8V_GPU_TP_PLL VOLTAGE=1.8V MIN_LINE_WIDTH=15 MIN_NECK_WIDTH=10 21																																																																						
																										+2.5V_MARVELL VOLTAGE=2.5V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 26																																														
																										+2.5V_MARVELL_AVDD VOLTAGE=2.5V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 26																																														
																										+1.0V_MARVELL VOLTAGE=1.0V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 26																																														
																										LTC1405_SW VOLTAGE=1.0V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 16																																														
																							+3V_NEC_VDD VOLTAGE=3.3V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=10 17																																																	

# FUNCTIONAL TEST POINTS

PROBES ARE ON BOTTOM SIDE. MINIMUM PAD/HOLE SIZE IS 25 MIL.

FUNC\_TEST IS ONLY PROPERTY USED BY THE TOOLS. FUNC\_QTY IS FOR REFERENCE AND LISTS THE NUMBER OF TEST POINTS ON THAT NET AND WITHIN THAT GROUP/CONNECTOR. FUNC\_DIST IS SIMILARLY USED TO DEFINE MAXIMUM DISTANCE FROM A CONNECTOR.

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST
SCAN/TEST	JTAG ASIC TMS	TRUE		13 26
	JTAG ASIC TDI	TRUE		13
	JTAG ASIC TDO TP	TRUE		26
	JTAG ASIC TCK	TRUE		13 26
	JTAG ASIC TRST L	TRUE		13 26
	CPU CHKSTP_OUT_L	TRUE		5
	CPU SRESET_L	TRUE		5
	CPU HRESET_L	TRUE		5 6 7
	JTAG CPU TMS	TRUE		5 6
	JTAG CPU TDI	TRUE		5 6
	JTAG CPU TDO TP	TRUE		5
	JTAG CPU TCK	TRUE		5 6
	JTAG CPU TRST L	TRUE		5 6
	INT_JTAG_TDI	TRUE		13
	INT_TST_MONIN_PD	TRUE		13
	INT_TST_MONOUT_TP	TRUE		13
	INT_TST_PLEEN_PD	TRUE		13
	INT_I2C_CLK0	TRUE		6 11 13 23
	INT_I2C_DATA0	TRUE		6 11 13 23
	INT_I2C_CLK1	TRUE		13 14 25
INT I2C	INT_I2C_DATA1	TRUE		13 14 25
	+PBUS	TRUE		38
PWR/GND	+24V_PBUS	TRUE		38
	GPU_VCORE	TRUE		19 20 38
	1778_VFB	TRUE		20 38
	CPU_VCORE_SLEEP	TRUE		5 13 38
	VCORE_FB	TRUE		23 38
	+1_8V_MAIN	TRUE		38
	+2_5V_MAIN	TRUE		38
	+5V_MAIN	TRUE	2	38 39
	+5V_SLEEP	TRUE	2	38 39
	+3V_MAIN	TRUE	4	23 38
CARDBUS	+3V_PMU	TRUE		38
	CBUS_DET_1_L	TRUE		2000
	CBUS_DET_2_L	TRUE		2000
	TMDS_DM<0...2>	TRUE		1000
	TMDS_DP<0...2>	TRUE		1000
	TMDS_CONN_CLKN	TRUE		1000
	TMDS_CONN_CLKP	TRUE		1000
	VGA_R	TRUE		1000
	VGA_G	TRUE		1000
	VGA_B	TRUE		1000
DVI	VGA_HSYNC	TRUE		1000
	VGA_VSYNC	TRUE		1000
	DVI_DDC_CLK_UP	TRUE		1000
	DVI_DDC_DATA_UP	TRUE		1000
	DVI_HPD_UP	TRUE		1000
	+5V_DDC_SLEEP	TRUE		2000
		TRUE	2	2000
		TRUE	6	2000
		TRUE		2000
		TRUE		2000
LVDS	LVDS_L0N	TRUE		1000
	LVDS_L0P	TRUE		1000
	LVDS_L1N	TRUE		1000
	LVDS_L1P	TRUE		1000
	LVDS_L2N	TRUE		1000
	LVDS_L2P	TRUE		1000
	CLKLVDS_LN	TRUE		1000
	CLKLVDS_LP	TRUE		1000
	LVDS_DDC_CLK	TRUE		1000
	LVDS_DDC_DATA	TRUE		1000
INVERTER	+3V_LCD	TRUE	2	2000
	+3V_SLEEP	TRUE	2	2000
		TRUE	6	2000
	+14V_INV	TRUE		2000
	+5V_INV_SW	TRUE		2000
	BRIGHT_PWM	TRUE		2000
	INV_GND	TRUE		2000
	TV_C	TRUE		1000
	TV_Y	TRUE		1000
	TV_COMP	TRUE		1000
S-VIDEO	TV_GND1	TRUE		2000
	TV_GND2	TRUE		2000
	INT_I2S0_SND_TO_DAC	TRUE		1000
	INT_I2S0_SND_LRCLK	TRUE		1000
	INT_I2S0_SND_MCLK	TRUE		1000
	INT_I2S0_SND_SCLK	TRUE		1000
	INT_I2S0_SND_FROM_ADC	TRUE		1000
	SND_HP_MUTE_L	TRUE		1000
	SND_AMP_MUTE	TRUE		1000
	SND_HW_RESET_L	TRUE		1000
LIO	SND_HP_SENSE_L	TRUE		1000
	SND_LIN_SENSE_L	TRUE		1000
	INT_I2C_CLK2	TRUE		1000
	INT_I2C_DATA2	TRUE		1000
	ADAPTER_DET	TRUE		1000
	CHARGE_LED_L	TRUE		1000
	NEC_LUSB_OCI_UF	TRUE		1000
	NEC_LUSB_PPON	TRUE		1000
	+5V_MAIN	TRUE	2	2000
	+5V_SLEEP	TRUE	2	2000
	+3V_SLEEP	TRUE		2000
		TRUE		2000

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST
USB	NEC_USB_DAM	TRUE		17 25 37
	NEC_USB_DAP	TRUE		17 25 37
	NEC_USB_DBM	TRUE		17 25 37
	NEC_USB_DBP	TRUE		17 25 37
	BT_USB_DM	TRUE		14 25 37
	BT_USB_DP	TRUE		14 25 37
	MODEM_USB_DM	TRUE		14 25 37
	MODEM_USB_DP	TRUE		14 25 37
	NEC_RUSB_PPON	TRUE		17 25
	NEC_RUSB_OCI_UF	TRUE		17 25
	PCI_AD<0...31>	TRUE	1000	9 12 17 18 24 37
	PCI_FRAME_L	TRUE	1000	12 17 18 24 37
	PCI_TRDY_L	TRUE	1000	12 17 18 24 37
	PCI_IRDY_L	TRUE	1000	12 17 18 24 37
	PCI_DEVSEL_L	TRUE	1000	12 17 18 24 37
	PCI_STOP_L	TRUE	1000	12 17 18 24 37
	PCI_PAR	TRUE	1000	12 17 18 24 37
	AIRPORT_FCI_REQ_L	TRUE	1000	12 24
	AIRPORT_FCI_GNT_L	TRUE	1000	12 24
	AIRPORT_FCI_INT_L	TRUE	1000	14 24
	MAIN_RESET_L	TRUE	1000	14 17 18 19 24 29
RT. USB WIRELESS	CLK33M_AIRPORT	TRUE		12 24 35
	PMU_PME_L	TRUE		1000
	ROM_ONBOARD_CS_L	TRUE		1000
	ROM_OE_L	TRUE		1000
	ROM_CS_L	TRUE		1000
	ROM_RW_L	TRUE		1000
	RF_DISABLE_L	TRUE		1000
	AIRPORT_CLKRUN_L	TRUE		1000
	+3V_AIRPORT	TRUE	4	2000
		TRUE	6	1000
OPTICAL	EIDE_OPTICAL_DATA<0...15>	TRUE		2000
	EIDE_OPTICAL_DMA_RQ	TRUE		2000
	EIDE_OPTICAL_READ_L	TRUE		2000
	EIDE_OPTICAL_DMAACK_L	TRUE		2000
	EIDE_OPTICAL_ADDR<0...2>	TRUE		2000
	EIDE_OPTICAL_CS0_L	TRUE		2000
	EIDE_OPTICAL_CSI_L	TRUE		2000
	EIDE_OPTICAL_RST_L	TRUE		2000
	EIDE_OPTICAL_WR_L	TRUE		2000
	EIDE_OPTICAL_IOCHRDY	TRUE		2000
TRACKPAD	EIDE_OPTICAL_INT	TRUE		2000
	+5V_TPAD_SLEEP	TRUE		3000
	TPAD_F_TXD	TRUE		3000
	TPAD_F_RXD	TRUE		3000
	LID_CLOSED_L	TRUE		3000
	+3V_HALL_EFFECT	TRUE		3000
	SOFT_PWR_ON_L	TRUE		3000
	COMM_RESET_L	TRUE		4000
	COMM_SHUTDOWN	TRUE		4000
	COMM_RING_DET_L	TRUE		4000
MODEM/SERIAL	COMM_TXD_L	TRUE		4000
	COMM_TRXC	TRUE		4000
	COMM_GPIO_L	TRUE		4000
	COMM_DTR_L	TRUE		4000
	COMM_RTS_L	TRUE		4000
	COMM_RXD	TRUE		4000
	KBD_ID	TRUE		3000
	KBD_INTL	TRUE		3000
	KBD_JIS	TRUE		3000
	KBD_CAPSLOCK_LED	TRUE		3000
KEYBOARD	KBD_NUMLOCK_LED	TRUE		3000
	KBD_FUNCTION_L	TRUE		3000
	KBD_COMMAND_L	TRUE		3000
	KBD_OPTION_L	TRUE		3000
	KBD_CONTROL_L	TRUE		3000
	KBD_SHIFT_L	TRUE		3000
	KBD_X<0...9>	TRUE		3000
	KBD_Y<0...7>	TRUE		3000
	+BATT_POS	TRUE	(100 MIL PROBE PREFERRED)	1000
	BATT_NEG	TRUE	(100 MIL PROBE PREFERRED)	1000
BATTERY	BATT_CLK	TRUE		1000
	BATT_DATA	TRUE		1000
FANS	PMU_BATT_DET_L	TRUE		1000
	+FAN_PWR	TRUE		3000
	FAN1_TACH	TRUE		3000
	FAN2_TACH	TRUE		3000
	FAN1_GND	TRUE		3000
	FAN2_GND	TRUE		3000
ETHERNET	MDI_P<0...3>	TRUE		1000
	MDI_M<0...3>	TRUE		1000
FIREWIRE	FW_TPO0P	TRUE		1000
	FW_TPO0N	TRUE		1000
	FW_TPO0R	TRUE		1000
	FW_TPI0P	TRUE		1000
	FW_TPI0N	TRUE		1000
	+FW_VP0	TRUE		1000
	FW_VGND	TRUE		1000
		TRUE		1000

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST
FIREWIRE (CONT.)	FW_TPO1P	TRUE		1000
	FW_TPO1N	TRUE		1000
	FW_TPI1P	TRUE		1000
	FW_TPI1N	TRUE		1000
	+FW_VP1	TRUE		1000
	FW_VGND	TRUE		1000
DC PWR IN	+ADAPTER	TRUE	3 (100 MIL PROBE PREFERRED)	1000
LMU/ALS	ST7_SLEEP_LED_H	TRUE		23
	PMU_SLEEP_LED	TRUE		23
	PMU_LID_CLOSED_L	TRUE		23 29
	LMU_DETECT	TRUE		23
MISC.			6	1000
			(100 MIL PROBE PREFERRED)	
	SLEEP_LED	TRUE		23
	PMU_KB_RESET_L	TRUE		29
	SLEEP	TRUE		23 25 29 32 34
	PMU_CPU_HRESET_L	TRUE		6 29
	BB_RESET_L	TRUE		6
	+3V_PMU_RESET	TRUE		29 33
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SCALE		NONE	SHT	OF
			39	40

	8	7	6	5	4	3	2	1	
REVISION HISTORY									
Proto Release									
D	7/22/02 - Initial acquisition of schematic (from 051-6278 Rev 01) Added P59 80-DIMM connector as placeholder (p.12) Added P59 LVDS connector as placeholder (p.22) Changed J9 to 10 pin Elco connector for modem (p.25) Changed PBUS holdup caps to P59 electrolytic cans (p.30)								
	7/23/02 - Removed L3 (p.8) Replaced processor with 360 pin Apollo (p.5,6) 7/24/02 - Added P68 Between battery and PBUS rails for airline power (p.29) 8/10/02 - Added USB 2.0 (p.18)								
	8/20/02 - Removed spare pullup straps for Intrepid (p.9) Removed USB overcurrent protection [to be placed on other boards] (p.18) Changed right USB board connector to 16 pin Hirose connector (p.26) Changed L10 board connector to 40 pin Molex connector (p.26) Added 6 bypass caps to MAXBUS_SLEEP and CPU_VCORE_SLEEP (p.5)								
	8/26/02 - Removed 32 bypass caps for +3V MAIN at Intrepid (p.16) Removed 5 bypass caps for +2.5V MAIN at Intrepid (p.6) Removed 3 bypass caps for +1.5V AGP at Intrepid (p.16) Removed 4 bypass caps for MAXBUS_MAIN at Intrepid (p.16)								
	8/27/02 - Changed main battery connector to BP24067-R1, which is close to final (p.29)								
	8/29/02 - Added dedicated Boot Banger circuit (p.6) Added 5 bypass caps to each 80-DIMM connector (p.11) Added quad voltage circuit for bus slewing architecture (p.32)								
	8/30/02 - Changed to low profile 32.768kHz crystal for PMU (p.28) Changed to Q11 adapter detection scheme (p.28)								
	9/03/02 - Corrected upper LVDS single pin nets (p.20) Removed unintentional extra pulldown resistor at Intrepid (p.14)								
	9/17/02 - Numerous changes to stay in sync with P84 (all)								
	9/18/02 - Changed battery connector back to P84 part (p.29) Added LMU circuitry to eliminate extra board (p.23) Changed to P84 dual channel LVDS connector to reduce 12R cable losses(p.22)								
C	9/19/02 - Removed unnecessary battery fuses (due to 3S only design) (p.29) Modified chassis gnds on some components (all) Corrected LMU resistor (same as P84) (p.29) Removed P93 support (p.25) Removed second fuse from FW ports [single fuse provides adequate power] (p.27)								
	9/23/02 - Replaced BCM5421 with Marvell 88E1111 (p.26) Increased MAX_VIA_COUNT by two on most nets with this constraint for uVia (p.34,35)								
	9/27/02 - Corrected cpu, memory bus constraints to match manhattan lengths (p.34) Swapped pins on L33, L35 for layout (p.31) Changed V6 to smaller form-factor crystal (p.26)								
	9/30/02 - Changed J19 (DC-in) to proper 4-pin connector (p.29) Corrected holes and chassis gnds (p.4,all)								
	10/01/02 - Removed Intrepid 1.x specific circuitry (p.13) 10/03/02 - Numerous pin-swaps to accommodate board layout (all) 10/08/02 - Added caps for functional test points (p.37) 10/09/02 - Changed 16 pin connectors (modem and right USB) to Foxconn parts (p.23) 10/10/02 - Changed NCL pins high per documentation (p.17) Added 10K pullup to CG_ADDRSEL and 10K pulldown to CG_FSEL on CY28512 (p.14) Added SSCQ/NO_SSCQ stuffing options for CY28512 circuit (p.14) Removed CPU_VGATE pullup to 5V to eliminate potential 3V/5V current path (p.32) Removed Zebra L45/L46 support (p.27) Added second FW port power fuse (p.27) Removed INT_CPUFB_IN cap per P84 (p.8) Replaced I8F782 FETs with I8F781N in battery charger and 14V PBUS switchers (p.29,30) Renamed optical interface for consistency (p.24,37) Corrected PLL_CFG<4> for Apollo 7 (needed to make keys be zero) (p.5,7) Removed temporary P84 constraints and finished up AGP clock changes (p.12,34) Added stuffing options to power fans off 3V or 5V (p.25)								
	10/11/02 - Replaced DVI EMI caps with 0201 versions (p.22)								
	10/14/02 - Changed J18 to RJ45 with integrated magnetics (p.26)								
	10/15/02 - Moved FireWire connectors and port power switch to separate page (p.28) Changed SMBus pullups to 7.15K, 1K as per 1Books/P84 [involved component net swaps] (p.29) Added 0603 resistors as shorting pads for power up and reset (p.23) Changed INT_MOD_SYNC, INT_MOD_DTI and INT_MOD_BITCLK to pulldowns per ERS [LA clk not used] (p.14) Added damping resistor option to LMU crystal (p.23) Changed INT_RST_FLEEN_PD to pulldown only [LA clk not used] (p.13) Changed JTAG_EMI_TDI to pulldown [LA clk not used] (p.13) Removed FW_LKON from Intrepid EXTINT3 [no longer used], pullup added (p.14) Changed BNRMS_HRMS to 3V_SLEEP (p.24) Changed FW_PC_PD, FW_PC_PU resistors to 5K (p.27) Added 1K pulldown and net FW_PD2 to FW_PHY (p.27)								
	10/16/02 - Implemented new FW power switch and current limit (p.28) Renamed +14V PBUS to +PBUS (p.all) Added A29 adapter detection circuit (p.29) Added +PBUS current limiting circuit, removed battery charging current limit circuit (p.30) Changed FW_PHY pin 081 to pulldown to make Port 1 1394s only (p.27)								
	B	10/21/02 - Updated CY28512 clock chip to Rev B (p.14) Changed FW_PHY pin 081 to pulldown to make Port 1 1394s only (p.27) 10/22/02 - Added full support for non-zero CPU_PLL_CFG<4> in run state (p.7) 10/23/02 - Changed keyboard ZTR to large SWM connector (p.23) Added full support for non-zero CPU_PLL_CFG<4> in run state (p.7) Changed LMU/sleep LED interface per P84 (p.23) Changed LMU JTAG/J2C pinout/pullup/pulldown strategy per P84 (p.23) Changed fan FETs to S13446DV per P84 (p.25) Pinned out audio connector (p.25) Pinned out right USB connector (p.25) Pinned out modem connector (p.25) Added 2 functional test points to wireless connector (p.24,38) Renamed FW low voltage power rails (p.27,37) Renamed Vcore VID nets to be consistent with P84 (p.33) Removed redundancy in DDR memory constraints (p.35) 10/24/02 - Changed FW DDI strap to pulldown to shut off port (p.27) Cleaned up CY28512B circuit as per P84 [powered off main, output divider and strap tweaks] (p.14) Updated PCI clock series B values per P84 (p.23) Changed power rail for ALS to +3V MAIN per P84 (p.23) Added 0 ohm shunt caps for FW_VDDOVD and FW_VDDOVD per P84 (p.21,37) Split FW_VGND into FW_VGND0 and FW_VGND1 (p.28,37) Added TP nets to GPU for XOR-tree testing (p.19-21) Changed fan PWM output pullups to +5V_SLEEP (p.25) Added FW thermal pad ground hole back in (p.27)							
10/28/02 - Replaced LMU layout (p.23) 10/30/02 - Changed fan power rails to common net (p.25) 10/31/02 - Added wireless RF_DISABLE_L pullup and AIRPORT_CLKRUN_L pulldown (p.24) Broke out quad OR-gate to discrete components for better placement (p.22,29) 11/06/02 - Changed 10 uF FW current limit output cap to two 4.7 uF caps (p.28) Added 3 decoupling caps to CPU_VCORE_SLEEP (p.4) Added 9 decoupling caps to each of +5V MAIN and +3V MAIN (p.32) Removed QW7, jumper for CPU_VCORE_SLEEP (p.35) 11/08/02 - Added decoupling cap to PMU reset OR gates (p.29) Changed FireWire PHY to Z17 (p.27) Added bulk caps to fan connectors (p.25) Added alternate chassis gnd connection for sleep LED (p.23)									
11/11/02 - Removed +3V MAIN option for P50 card (p.24) 11/13/02 - Removed LMU and associated circuitry (p.23) 11/21/02 - Implemented D3cold for all PCI devices (p.12,14,18) 11/25/02 - Renamed all components (all pages) 11/26/02 - Removed chokes from 1394s data pairs (p.27,28)									
EVT RELEASE									
12/13/02 - Added 12 pF caps to source of 33MHz PCI clocks since they can not be buried (p.12) Replaced ALM1031 with AD7460 [12C Address Change] (p.25) Added AD7460 hookups to GPU thermal diode (p.21,25) Added FireWire B ESD protection circuits (p.28) Removed hole from FireWire ground pad (p.7) 12/16/02 - DDR memory connector renamed to J25 (p.11) Removed J4210 from FireWire port power (p.28) 12/20/02 - Added F10,F20 as placeholders and experiment guides (p.28) Added diodes to OR +5V_SLEEP into FW_PHY power supply (p.27) 12/26/02 - Updated CPU p/ns to production p/ns (p.5) Added caps to FW EMI circuit that were missed (p.5,36) Updated PCI source clock and internal spreading straps (p.8) Changed bootROM FWD signal to INT_RESET_L per P84 (p.9) Added CKE pulldowns per P84 (p.9) Updated Ethernet series Rs per P84 [Clocks to 10 ohms, data to 22 ohms] (p.13) Updated SSCQ/NO_SSCQ BOM options (p.14) Renamed line-in and headphone sense lines to reflect active low signals (p.14,25,39) Added 0 ohm Rs to make 2.5V Intrepid rail hot or cold (p.15,16,38) NO STUFFED entire 1.5V LDO circuit (p.15) Stuffed USB OC1/FP0N filters for 0 Ohm constant [due to new port current limiters] (p.17) Renamed USB OC1/FP0N signals for left/right ports (p.17,39) Updated GPU VCore to stay in sync with P84 [jitter improvement] (p.20) Added EMI caps to LVDS_DDC_CLK, INT_I2S0_SND_MCLK, INT_I2S0_SND_SCLK per P84 (p.22,25) Added R800,R801 for eventual thermal diode in CPU (p.25) Renamed R2000 to R799, R2001 to R802, R2002 to R803 (p.25) Renamed F10 to F1, F20 to F2 [deleted old F1,F2] (p.28) Added caps to FW ESD circuit that were missed (p.28) Changed MAX4172 power source to save current on battery [per P84] (p.30) Updated 1.5V/2.5V switcher BOM to stay in sync with P84 [PST change and current limits] (p.34) Replaced all 132S1061 [1uF,0603,10V,20K] with 132S0046 [1uF,0603,10V,20K] (p.14,15,27,30,33,34) Replaced all 138S0251 [1uF,0603,6.3V,10K] with 132S0046 [1uF,0603,10V,20K] (p.27,30)									
A		01/02/03 - Updated FireWire fuse topology to that of P84 (p.28) Updated system and power block diagrams (p.2,3) 01/03/03 - Corrected +2.5V_INTREPID connections to muxes and reference (p.9,10) 01/07/03 - Added NO_TEST nets to pads of DDR connector arms (p.11) 01/08/03 - Added ZNY002 circuits to ensure speakers are muted during power-up (p.25) 01/09/03 - Changed R164 to 511 ohms to avoid low CPU clock amplitude (p.8) Added required pulldown to output of DVI_HPD sense comparator (p.22) Swapped R443 and R444 values to ensure Vgs < -4.5V (p.28) Updated S-video filter values to those of P84 (p.22)							
		01/10/03 - ZT7,ZT23,ZT61,ZT76,ZT89,ZT87,ZT22,ZT38,ZT60,ZT42 & ZT17 are changed to HOLE-VIA-20R10 (p.4)							
		01/13/03 - Add L53, L54, L55 for TMSD Data<0>2+ Diff Pair (p.22)							
		01/14/03 - Add C812 - C821 (Total 10 0.22uF caps) for 2.5V Intrepid Decoupling (p.16) Add C822 & C823 at Wireless Card connector MAIN_RESET_L & RF_DISABLE_L_SPN (p.24) Change MATCHED_DELAY to 50 for all TMSD DIFF PAIR (p.37) Change MATCHED_DELAY to 50 for all TMSD DIFF PAIR (p.37) Add R810 & R811 for ALWAYS-ON FANS in Acrylic Build (p.25) Remove NV31/17 components (p.19-21)							
		01/28/03 - Add M10 (p.19-21)							
	02/07/03 - Add Power Net Constraints for M10 (p.38) Replace Singing PBUS Cap C49,C50,C67,C68,C80,C81,C95,C96,C108,C109,C120,C121 with 1260035 (or alt. 1260036) (p.33)								
	02/11/03 - Add FW Power Net Constraints (p.38) Change signal constraints for AGP signals (p.36) Add LMU connector and components (p.23) Edit I2C table for LMU (p.13) Change R580 to 19.6K (p.14) Connect Clock Slewing RESET# to MAIN_RESET_L (p.14) Change Ferrite Bean of ATI power supply to correct values (p.21) Remove C141 PBUS CAP (p.31) Change and Rotate Keyboard Connector (p.23) Add ATI Power sequencing Circuit for M10 Power-up and Power-down (p.19-22, p.32-35)								
	02/12/03 -								
	EVT RELEASE (continue)								
	D	02/13/03 - Add C825 (p.30) 02/17/03 - Rename all Reference Designators							
EVT ENCLOSURE RELEASE									
03/13/03 - Change 3-P FAN connectors to 4-P (p.25) Add PU at PMU_SLEEP_LED_L for LMU (p.23) Change stuffing option for clock slewing (p.25) Change ATI M10 GPIO8 to Pull-down (p.20) Remove Memory MUX 0ohm Resistors (p.10)									
03/28/03 - Due to MLB outline change at DVI connector, CHGN01 has to be splitted into CHGN1 & CHGN2 (P 4 & 22) Separate +3V and +5V traces running from 3/5V supply to 40Pin LIO connector (P 25 & 32) R601 change from 100K to 4.7K (P 29) Change airline detect to 13.1V or greater, R40 and R690 to 97.6K ohm (P 30 & 31) Add C826 at U3 RS3 - pin (P 30) Change D3 to 1N914 PN Junction Diode(P 31)									
03/31/03 - Change AGPTST Pull-up to 470hm (it was 400hm) (P 20) Add C843 10uF Cap to 1206 package part (P 28) Change all 1210 4.7uF to 1206 4.7uF Cap (138S0531) (various pages) Modify FAN circuit to PWM active low signal (P25)									
04/08/03 - Add SOFT MODEM support (P 14 & 25) Add 10-pin ELCO connector for Serial Debug Interface (P 25) Change Q7 from S144350Y to S0D45P03-10 (P 30) Remove U34 RS3AB (P 30)									
04/11/03 - Change FW Schottky Diode to a 3A part 371S0159 (P 28) Change PBUS L69 and VCORE L71 inductor (P 31 & 33) Change U34 10uF Cap to 1206 package part (P 28) Change all 6 VCORE Caps to 220uF AL Poly Cap 128S0024 (P 33) Add Mitaumi MM1571J regulator to provide 1.8V TPVDD (P 21) Change U34 to Mitaumi MM1571J part for ATI FLL 1.8V rail(P 21)									
04/16/03 - Add FW Port Shutdown/PowerOn Circuit (P 28) Change the I2C Pull-up for Sound/Modem to 1K ohm (P 14)									
04/17/03 - Change 3V/5V inductors (152S0137) L61 & L62 (P 32)									
04/21/03 - Add 12 ICT JTAG TEST PADS (P 39)									
C	04/23/03 - Invert ATI GPIO15 signal, no stuff pull-up resistor (P 20) Combine Q35 and Q36 into a Dual Package Part (P 22) SWAP the AD7460 Temperature Sense pair (P 21) Change FW PHY to production part (P 26)								
	04/24/03 - Remove +3V_CBUS_SLEEP and U5, use +3V_SLEEP directly (P 14,18,24) Add 0402 Res between ATI PVD0/TPVDD rail and 10uF caps for stability purpose (P 21) Add 90ohm common mode choke at TMSD data <0,2> pairs (P 22) Add Sense Resistor to Vcore power rail, remove one 220uF cap <back to EVTA design> (P 33)								
	04/25/03 - Change C826 to 0.01uF 50V Cap (P 30)								
	04/30/03 - No stuff R676 to prevent +3V rail leakage (P 33)								
	05/02/03 - L45,L46,L47 is using Common Mode Choke TDK ACM2012D Part, will replace with ACM2012H Part if available (P 22)								
	DVT RELEASE								
	05/21/03 - Swap +PBUS and +24V_PBUS at Backup Battery Connector - J16 (p.31)								
	05/27/03 - Change Q62 timing specification (p.13) Change Q62 & Q65 to S17860DP part (p.33) Change Q64 Q65 Q66 Q67 Q68 Q69 Q70 Q71 Q72 Q73 Q74 Q75 Q76 Q77 Q78 Q79 Q80 Q81 Q82 Q83 Q84 Q85 Q86 Q87 Q88 Q89 Q90 Q91 Q92 Q93 Q94 Q95 Q96 Q97 Q98 Q99 Q100 Q101 Q102 Q103 Q104 Q105 Q106 Q107 Q108 Q109 Q110 Q111 Q112 Q113 Q114 Q115 Q116 Q117 Q118 Q119 Q120 Q121 Q122 Q123 Q124 Q125 Q126 Q127 Q128 Q129 Q130 Q131 Q132 Q133 Q134 Q135 Q136 Q137 Q138 Q139 Q140 Q141 Q142 Q143 Q144 Q145 Q146 Q147 Q148 Q149 Q150 Q151 Q152 Q153 Q154 Q155 Q156 Q157 Q158 Q159 Q160 Q161 Q162 Q163 Q164 Q165 Q166 Q167 Q168 Q169 Q170 Q171 Q172 Q173 Q174 Q175 Q176 Q177 Q178 Q179 Q180 Q181 Q182 Q183 Q184 Q185 Q186 Q187 Q188 Q189 Q190 Q191 Q192 Q193 Q194 Q195 Q196 Q197 Q198 Q199 Q200 Q201 Q202 Q203 Q204 Q205 Q206 Q207 Q208 Q209 Q210 Q211 Q212 Q213 Q214 Q215 Q216 Q217 Q218 Q219 Q220 Q221 Q222 Q223 Q224 Q225 Q226 Q227 Q228 Q229 Q230 Q231 Q232 Q233 Q234 Q235 Q236 Q237 Q238 Q239 Q240 Q241 Q242 Q243 Q244 Q245 Q246 Q247 Q248 Q249 Q250 Q251 Q252 Q253 Q254 Q255 Q256 Q257 Q258 Q259 Q260 Q261 Q262 Q263 Q264 Q265 Q266 Q267 Q268 Q269 Q270 Q271 Q272 Q273 Q274 Q275 Q276 Q277 Q278 Q279 Q280 Q281 Q282 Q283 Q284 Q285 Q286 Q287 Q288 Q289 Q290 Q291 Q292 Q293 Q294 Q295 Q296 Q297 Q298 Q299 Q300 Q301 Q302 Q303 Q304 Q305 Q306 Q307 Q308 Q309 Q310 Q311 Q312 Q313 Q314 Q315 Q316 Q317 Q318 Q319 Q320 Q321 Q322 Q323 Q324 Q325 Q326 Q327 Q328 Q329 Q330 Q331 Q332 Q333 Q334 Q335 Q336 Q337 Q338 Q339 Q340 Q341 Q342 Q343 Q344 Q345 Q346 Q347 Q348 Q349 Q350 Q351 Q352 Q353 Q354 Q355 Q356 Q357 Q358 Q359 Q360 Q361 Q362 Q363 Q364 Q365 Q366 Q367 Q368 Q369 Q370 Q371 Q372 Q373 Q374 Q375 Q376 Q377 Q378 Q379 Q380 Q381 Q382 Q383 Q384 Q385 Q386 Q387 Q388 Q389 Q390 Q391 Q392 Q393 Q394 Q395 Q396 Q397 Q398 Q399 Q400 Q401 Q402 Q403 Q404 Q405 Q406 Q407 Q408 Q409 Q410 Q411 Q412 Q413 Q414 Q415 Q416 Q417 Q418 Q419 Q420 Q421 Q422 Q423 Q424 Q425 Q426 Q427 Q428 Q429 Q430 Q431 Q432 Q433 Q434 Q435 Q436 Q437 Q438 Q439 Q440 Q441 Q442 Q443 Q444 Q445 Q446 Q447 Q448 Q449 Q450 Q451 Q452 Q453 Q454 Q455 Q456 Q457 Q458 Q459 Q460 Q461 Q462 Q463 Q464 Q465 Q466 Q467 Q468 Q469 Q470 Q471 Q472 Q473 Q474 Q475 Q476 Q477 Q478 Q479 Q480 Q481 Q482 Q483 Q484 Q485 Q486 Q487 Q488 Q489 Q490 Q491 Q492 Q493 Q494 Q495 Q496 Q497 Q498 Q499 Q500 Q501 Q50								