1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

SCHEM,MLB,VENUS,X425G

EVT 01/12/2015

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54	65	AUDIO: JACK	CLEAN_X305	06/24/2014
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56	70	DC-In & Battery Connectors	CLEAN_X425	11/04/2014
57	71	PBus Supply & Battery Charger	CLEAN_X305	01/15/2014
58	72	CPU VR12.5 VCC Regulator IC	CLEAN_X425	01/09/2015
59	73	CPU VR12.5 VCC Power Stage	CLEAN_X425	01/09/2015
60	74	1.35V DDR3L SUPPLY	CLEAN_X305	01/15/2014
61	75	5V / 3.3V Power Supply	CLEAN_X425	11/04/2014
62	76	1V05V POWER SUPPLY	CLEAN_X305_PEG	02/18/2014
63	77	LCD/KBD Backlight Driver	CLEAN_X425	10/30/2014
64	78	Misc Power Supplies	CLEAN_X305	01/15/2014
65	79	X249 POWER SUPPLY	CLEAN_MAXWELL	07/02/2014
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67	81	Power Control 1/ENABLE	J45_IG	07/01/2014
68	82	Power Sequencing EG/PGOOD	MARY_X425G	09/11/2014
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76	90	Venus HDMI/DP/GPIO	MARY_X425G	09/22/2014
77	91	Venus GPIOs & STRAPs	MARY_X425G	11/07/2014
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79	93	GFX IMVP VCore Regulator	ADITYA_X425G	09/15/2014
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91	113	PCH Constraints 2	CLEAN_X305_PEG	02/18/2014
92	114	Memory Constraints	SIDLE_J45	12/10/2012
93	115	Thunderbolt Constraints	SIDLE_J45	12/10/2012
94	116	Camera Constraints	SIDLE_J45	12/10/2012
95	117	SMC Constraints	SIDLE_J45	12/10/2012
96	118	Project Specific Constraints	SIDLE_J45	12/10/2012
97	119	GPU (AMD VENUS) Constraints	J45G_AMD	07/01/2014

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-00383	1	SCHEM,MLB,VENUS,X425G	SCH	CRITICAL	
820-00163	1	PCBF,MLB,VENUS,X425G	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=ABBREV
LAST_MODIFIED=Mon Jan 12 16:34:40 2015

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00042	COMMON PARTS,MLB,VENUS,X425G	X425_COMMON
985-00050	DEV BOM,MLB,VENUS,X425G	X425_DEVEL:ENG
639-00682	PCBA,MLB,VENUS,CTO,16GHYN,VR-4GHYN,X425G	BASE_BOM,DEVEL_BOM,GFX_BOM,CPU_CRW:CTO,RAM:HYNIX_1600,FB_4G_HYNIX
639-00703	PCBA,MLB,VENUS,CTO,16GMIC,VR-4GMIC,X425G	BASE_BOM,DEVEL_BOM,GFX_BOM,CPU_CRW:CTO,RAM:MICRON_1600,FB_4G_MICRON
639-00739	PCBA,MLB,VENUS,CTO,16GHYN,VR-4GMIC,X425G	BASE_BOM,DEVEL_BOM,GFX_BOM,CPU_CRW:CTO,RAM:HYNIX_1600,FB_4G_MICRON
639-00740	PCBA,MLB,VENUS,CTO,16GMIC,VR-4GHYN,X425G	BASE_BOM,DEVEL_BOM,GFX_BOM,CPU_CRW:CTO,RAM:MICRON_1600,FB_4G_HYNIX
639-00798	PCBA,MLB,VENUS,BEST,16GHYN,VR-4GHYN,X425G	BASE_BOM,DEVEL_BOM,GFX_BOM,CPU_CRW:BEST,RAM:HYNIX_1600,FB_4G_HYNIX
639-00799	PCBA,MLB,VENUS,BEST,16GMIC,VR-4GMIC,X425G	BASE_BOM,DEVEL_BOM,GFX_BOM,CPU_CRW:BEST,RAM:MICRON_1600,FB_4G_MICRON
639-00800	PCBA,MLB,VENUS,BEST,16GHYN,VR-4GMIC,X425G	BASE_BOM,DEVEL_BOM,GFX_BOM,CPU_CRW:BEST,RAM:HYNIX_1600,FB_4G_MICRON
639-00801	PCBA,MLB,VENUS,BEST,16GMIC,VR-4GHYN,X425G	BASE_BOM,DEVEL_BOM,GFX_BOM,CPU_CRW:BEST,RAM:MICRON_1600,FB_4G_HYNIX
639-00803	PCBA,MLB,VENUS,NOCPU,16GMIC,VR-4GHYN,X425G	BASE_BOM,DEVEL_BOM,GFX_BOM,RAM:MICRON_1600,FB_4G_HYNIX
639-00974	PCBA,MLB,NOGPU,CTO,16GMIC,VR-4GHYN,X425G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:MICRON_1600,FB_4G_HYNIX

X425 BOM Groups

BOM GROUP	BOM OPTIONS
X425_COMMON	ALTERNATE,COMMON,X425_COMMON1,X425_COMMON2,X425_PROGPARTS,ACAPS:A2
X425_COMMON1	CPUMEM:S0,TBTHV:P15V,SKIP_5V3V3:AUDIBLE,CPUPEG:X8X4X4,S2_PWR:S0,SMC_SUSACK:YES
X425_COMMON2	EDP:YES,XDP,SSD_PWR_EN:GPIO,CAM_WAKE:NO,SAMCONN,APCLKRQ:ISOL,CRW_SPRT,WLAN_SW:SIL
X425_PVT	BKLT:PROD,SENSOR_NONPROD:N
X425_PROGPARTS	SMC_PROG:BASE,BOOTROM_PROG:EVT,TBTROM:PROG,DPMUXMCU:PROG
X425_DEVEL:ENG	ALTERNATE,XDP_DEBUG,S0PGOOD_ISL,SENSOR_NONPROD:Y,SENSOR_NONPROD_R,BKLT:ENG,DBGLED,DPMUX_DEBUG,GPU_ROM:YES,SENSOR_GPU_NONPROD:Y
X425_DEVEL:DVT	ALTERNATE,XDP_DEBUG,BKLT:PROD,SENSOR_NONPROD:N,DBGLED
X425_DEVEL:PVT	XDP_DEBUG
GFX_BOM	VENUS:XTA
XDP_DEBUG	XDP_CONN,XDP_PCH

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00058	1	CRW,SR1ZX,PRQ,C0,2.5,47W,4+3E,1.2,6M,BGA	U0500	CRITICAL	CPU_CRW:BEST
337S00059	1	CRW,SR1ZY,PRQ,C0,2.8,47W,4+3E,1.2,6M,BGA	U0500	CRITICAL	CPU_CRW:CTO
337S4542	1	IC,QEWV,LPT-M,HM87,C2,SR199,PRQ,FCBGA	U1100	CRITICAL	
338S1247	1	IC,TBT,FR-4C,A0,PRQ,CIO,SR1JC,FCBGA288	U2800	CRITICAL	
338S1264	1	IC,BCM15700A2,S2 PCIE CMRA,8X8,208FCBGA	U3900	CRITICAL	
333S0700	1	IC,SDRAM,4GBIT,DDR3L-1600,GEMMA,96B FBGA	U4000	CRITICAL	
333S00032	32	IC,SDRAM,DDR3L-1600,4GBIT,78B FBGA		CRITICAL	HYNIX_1600
333S0660	32	IC,SDRAM,4GBIT,DDR3L-1600,V80A,78P,FBGA		CRITICAL	MICRON_1600
337S00116	1	IC,GPU,VENUS XTAA1,Q5,29X29MM,FCBGA962	U8400	CRITICAL	VENUS:XTA
333S00027	4	IC,GDDR5,4GBIT,6GBPS,1.5V,25NM,BGA170	U8800,U8850,U8900,U8950	CRITICAL	FB_4G_HYNIX
333S0766	4	IC,GDDR5,4GBIT,6GBPS,128MX32,25NM,170BGA	U8800,U8850,U8900,U8950	CRITICAL	FB_4G_MICRON

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM:HYNIX_1600	HYNIX_1600,RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM:MICRON_1600	MICRON_1600,RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L

COMMON/DEVEL BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00042	1	COMMON PARTS,MLB,VENUS,X425G	BASE	CRITICAL	BASE_BOM
985-00050	1	DEV,MLB,VENUS,X425G	DEVEL	CRITICAL	DEVEL_BOM

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Programmables - All builds

335S0915	1	IC,SERIAL SPI FLASH ROM,4MBIT,50MHZ,USON	U2890	CRITICAL	TBTROM:BLANK
341S00166	1	T29,FALCON RIDGE(V27.1)PROTO0,X425G	U2890	CRITICAL	TBTROM:PROG
335S0724	1	1MBIT SERIAL FLASH 2X3X0.6MM UFDFPN8 PKG	U9101	CRITICAL	GPUROM:BLANK
341S3565	1	IC,EDP MUX-95C,(RENESAS) V3.2.8,DVB,D2	U9600	CRITICAL	DPMUXMCU:PROG
337S4313	1	IC,MCU,H8S/2113,9X9MM,TLP-145V	U9600	CRITICAL	DPMUXMCU:BLANK

SMC

338S1214	1	IC,SMC-B1,40MHZ/50DMIPS,SCPL FW,157BGA	U5000	CRITICAL	SMC_PROG:BLANK
341S00157	1	IC,SMC-B1,EXT (V2.25A9) PROTO 0,X425G	U5000	CRITICAL	SMC_PROG:BASE

EFI ROM

335S00007	1	IC,SERIAL FLASH,64MB,3V,WSON,6X5MM	U6100	CRITICAL	BOOTROM_BLANK:WIN
335S00006	1	IC,SERIAL FLASH,64MB,3V,WSON,6X5MM	U6100	CRITICAL	BOOTROM_BLANK:MAC
341S00239	1	IC,EFI ROM (V0145) EVT,X425	U6100	CRITICAL	BOOTROM_PROG:EVT

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1053	376S0604		ALL	Diodes alt to Fairchild
128S0311	128S0329		ALL	NEC alt to Sanyo
138S0739	138S0706		ALL	Samsung alt to Murata
197S0481	197S0480		ALL	Epson Alt to NDK
197S0478	197S0479		ALL	NDK Alt to Epson
371S0713	371S0558		ALL	DDS alt to ST
152S0461	152S1645		ALL	Cyntec alt to Vishay
376S1080	376S0820		ALL	Diodes alt to On Semi
155S0667	155S00008		ALL	Panasonic alt to TDK
376S00074	376S0855		ALL	Toshiba alt to Diodes
376S1129	376S0855		ALL	NXP alt to Diodes
376S1089	376S1128		ALL	NXP alt to Diodes
128S0371	128S0376		ALL	Kemet alt to Sanyo
138S0803	138S0639		ALL	Samsung alt to Murata
138S0843	138S0674		ALL	Samsung alt to Murata
138S0846	138S0811		ALL	Samsung alt to Murata
127S0164	127S0162		ALL	Rohm alt to Vishay
138S0732	138S0715		ALL	Rohm alt to Vishay
128S0364	128S0264		ALL	Kemet alt to Sanyo
333S0704	333S0700		ALL	ELPIDA to HYNIX U4000
311S0649	311S0541		ALL	ON alt to Toshiba
376S00014	376S0761		ALL	Toshiba alt to Vishay
740S00003	740S0135		ALL	AEM alt to Tyco
740S00004	740S0134		ALL	AEM alt to Littlefuse
107S00029	107S00030		ALL	TFT alt to Cyntec
128S0398	128S0220		ALL	Kemet alt to Sanyo
128S0386	128S0284		ALL	Kemet alt to Sanyo
311S00008	311S0271		ALL	Diodes alt to NXP
128S0393	128S0334		ALL	Kemet alt to Sanyo
311S00007	311S0426		ALL	Diodes alt to NXP
371S00017	371S0749		ALL	Diodes alt to Onsemi
107S00033	107S00034		ALL	TFT alt to Cyntec
107S0240	107S0255		ALL	TFT alt to Cyntec
107S0248	107S0250		ALL	TFT alt to Cyntec
107S00031	107S00032		ALL	TFT alt to Cyntec
107S0249	107S0251		ALL	TFT alt to Cyntec
107S00037	107S00038		ALL	TFT alt to Cyntec
107S00015	107S00011		ALL	TFT alt to Cyntec
128S00008	128S0380		ALL	NEC alt to Sanyo
311S00060	311S0273		ALL	Diodes alt to NXP
353S00133	353S2741		ALL	ON Semi alt to TI
353S00394	353S2162		ALL	ON Semi alt to TI
376S00086	376S0761		ALL	Diodes alt to Vishay
112S00001	112S0254		ALL	Yageo alt to Cyntec
353S00095	353S3328		ALL	Pericom alt to TI
128S0397	128S0325		ALL	Kemet alt to Sanyo
311S00004	311S0370		ALL	ON Semi alt to NXP

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Frame Holes

ZT0415
2.8R2.3
GND

ZT0450
TH-NSP
SL-2.3X3.9-2.9X4.5
GND

ZT0470
TH-NSP
SL-1.1X0.45-1.4x0.75
GND

ZT0471
TH-NSP
SL-1.1X0.45-1.4x0.75
GND

ZT0472
TH-NSP
SL-1.1X0.45-1.4x0.75
GND

ZT0473
TH-NSP
SL-1.1X0.45-1.4x0.75
GND

SMT GND TEST PONTS

ZT0490
2.1SM2.0MM-CIR
SMT-PAD-NSP

ZT0491
2.1SM2.0MM-CIR
SMT-PAD-NSP

ZT0492
2.1SM2.0MM-CIR
SMT-PAD-NSP

APN 806-2247
BR0401
MLB-MTG-BRKT-J5
TH

X305G THERMAL MODULE STANDOFF

APN 860-3690
SH0424
STDOFF-4.5OD1.9H-SM-1

APN 817-0688
SH0446
STDOFF-4.9OD2.38H-SM-2

APN 817-0741
SH0445
STDOFF-4.9OD2.38H-SM-SL-2.6X2NP-2

GPU BOSS APN 860-4772

SH0430
4.5OD1.85ID-1.95H

SH0427
4.5OD1.85ID-1.95H

SH0428
4.5OD1.85ID-1.95H

GPU BOSS APN 817-4517

SH0421
4.5OD1.85ID-1.95H-1

CPU BOSS APN 860-2931

SH0429
5.0OD1.85ID-2.35H

SH0420
5.0OD1.85ID-2.35H

SH0422
5.0OD1.85ID-2.35H

SH0426
5.0OD1.85ID-2.35H

FAN BOSS APN 860-3428

SH0425
STDOFF-4.5OD1.8H-SM-1

SH0423
STDOFF-4.5OD1.8H-SM-1

Thermal Module gaskets APN 875-9290

OMIT
CG0400
6.0OD3.9H-SM

OMIT
CG0402
6.0OD3.9H-SM

OMIT
CG0401
6.0OD3.9H-SM

OMIT
CG0403
6.0OD3.9H-SM

PD parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
946-3819	1	D2 MLB DYMAX ADHESIVE SEE-CURE 29993-SC	EDGE_BOND	CRITICAL	

RIO FLEX BRACKET BOSS (860-00166)

SH0480
3.5OD1.85ID-2.0H

SH0481
3.5OD1.85ID-2.0H

IPD FLEX BRACKET BOSS (860-00166)

SH0482
3.5OD1.85ID-2.0H

SH0483
3.5OD1.85ID-2.0H

APN 806-9391
SH0450
SM
SHLD-MLB-USB-J45

806-00452
SH0451
SM
SHLD-FENCE-MLB-T29-X305

X305G POGO PINS

APN 870-2451

SH0431
POGO-2.30D-5.5H-X304
SM

SH0432
POGO-2.30D-5.5H-X304
SM

SH0433
POGO-2.30D-5.5H-X304
SM

SH0434
POGO-2.30D-5.5H-X304
SM

SH0435
POGO-2.30D-5.5H-X304
SM

SH0437
POGO-2.30D-5.5H-X304
SM

X305G STANDOFF

APN 860-1448

SH0440
2.90D1.2ID-1.35H-SM

SH0441
2.90D1.2ID-1.35H-SM

SH0444
2.90D1.2ID-1.35H-SM

SH0460
2.90D1.2ID-1.35H-SM

SH0461
2.90D1.2ID-1.35H-SM

SH0463
2.90D1.2ID-1.35H-SM

SH0464
2.90D1.2ID-1.35H-SM

SH0442
2.90D1.2ID-1.35H-SM

SH0443
2.90D1.2ID-1.35H-SM

SH0462
2.90D1.2ID-1.35H-SM

SH0465
2.90D1.2ID-1.35H-SM

SH0466
2.90D1.2ID-1.35H-SM

SH0467
2.90D1.2ID-1.35H-SM

SYNC_MASTER=CLEAN_X305G SYNC_DATE=08/08/2014

PAGE TITLE
PD Parts

Apple Inc.

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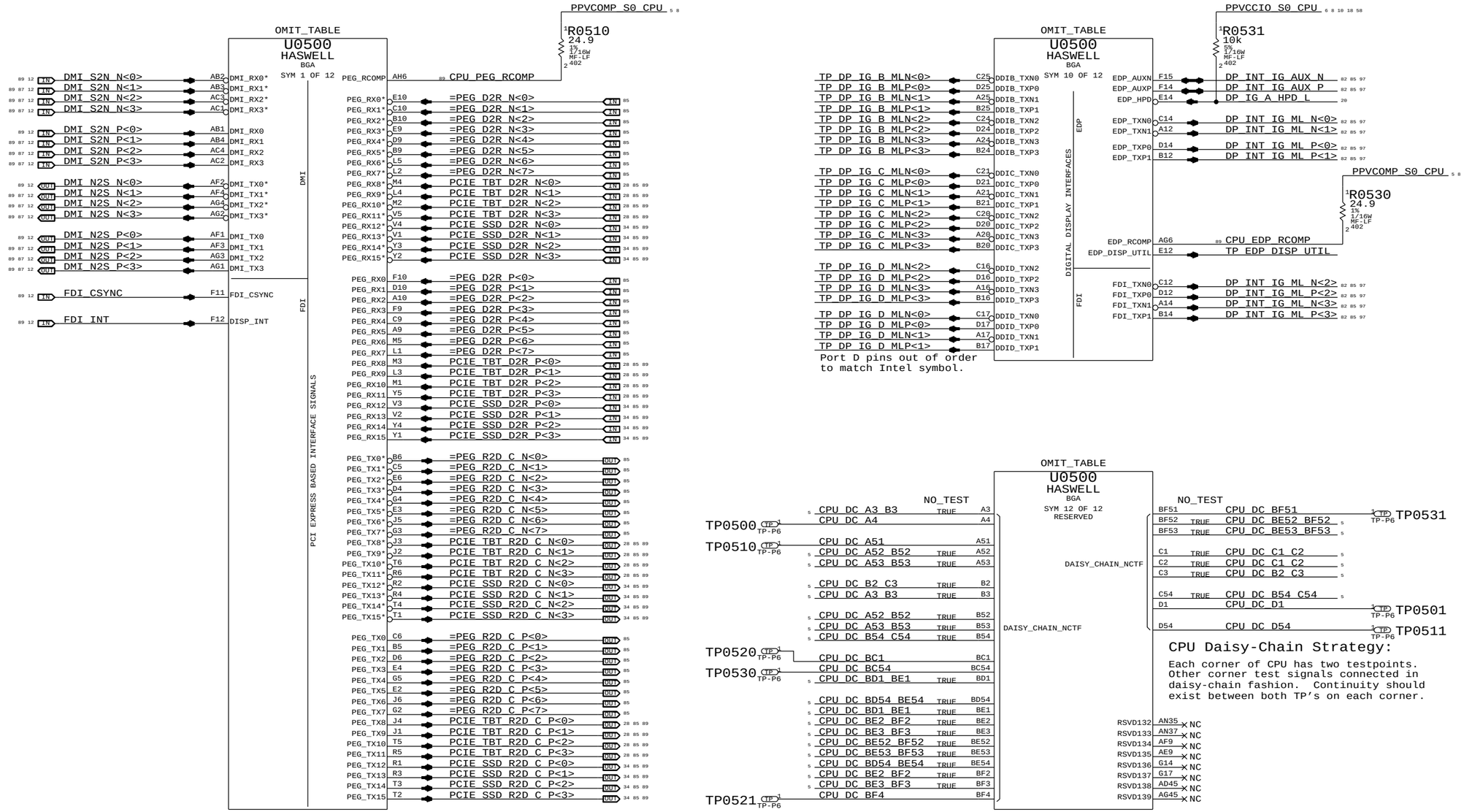

SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/18/2014

PAGE TITLE
CPU DMI/PEG/FDI/RSVD

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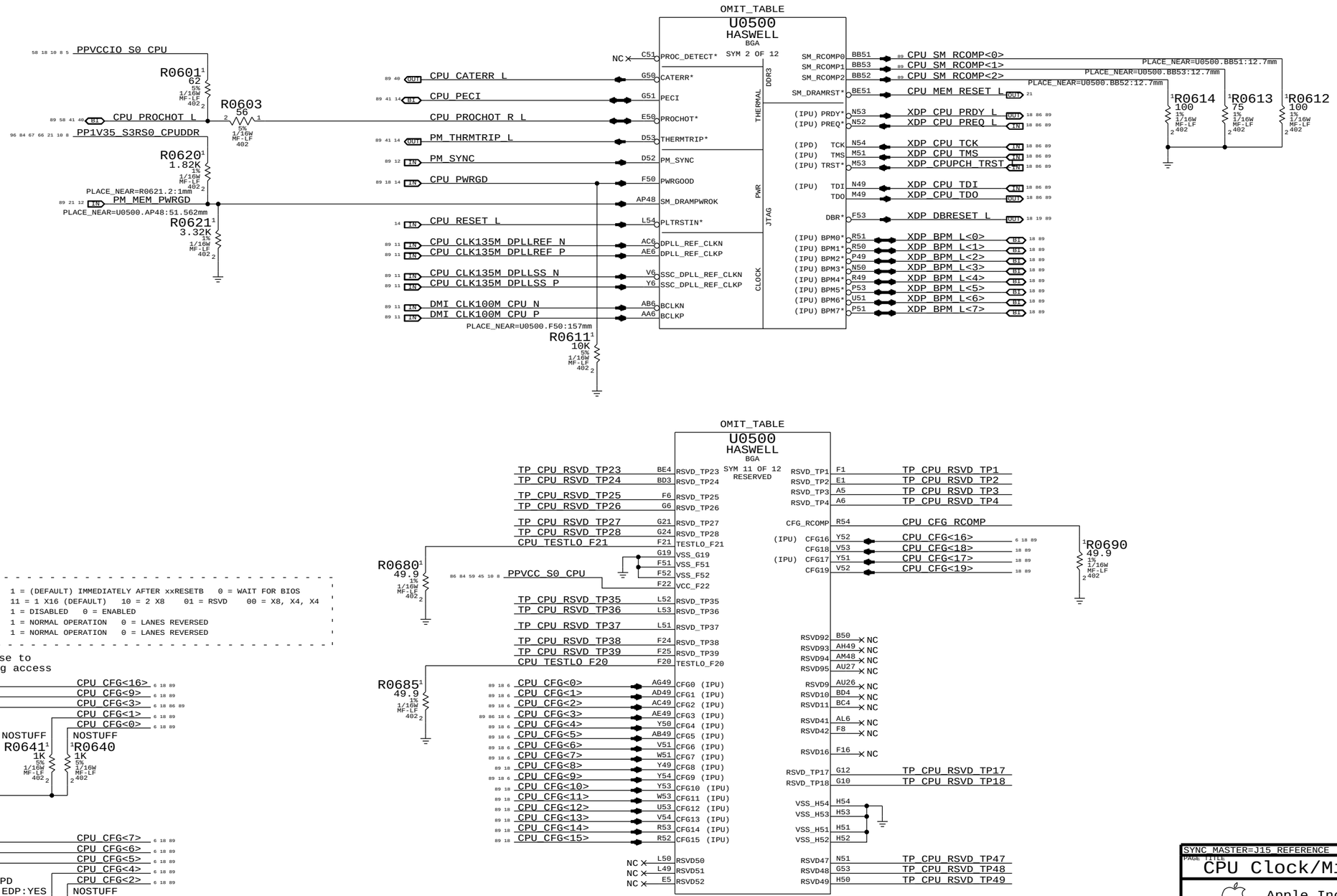
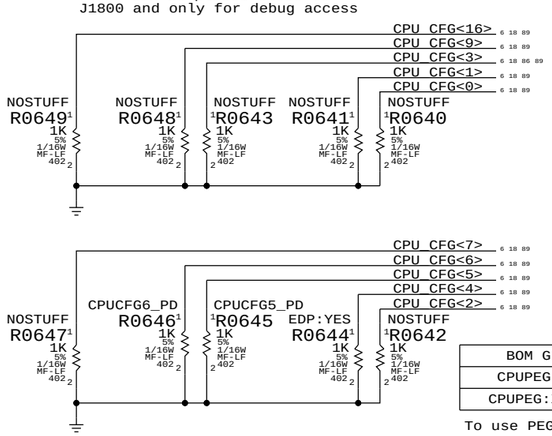



```
CFG [7] :PEG DEFER TRAINING          1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB   0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION          11 = 1 X16 (DEFAULT)   10 = 2 X8    01 = RSVD    00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE          1 = DISABLED   0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL       1 = NORMAL OPERATION   0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL      1 = NORMAL OPERATION   0 = LANES REVERSED
```

These can be placed close to J1800 and only for debug access



BOM GROUP	BOM OPTIONS
CPUPEG:X8X8	CPUCFG5_PD
CPUPEG:X8X4X4	CPUCFG6_PD,CPUCFG5_PD

To use PEG X16 configuration, simply remove CPUPEG:X8X8 and CPUPEG:X8X4X4 from BOMs.

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE
CPU Clock/Misc/JTAG/CFG

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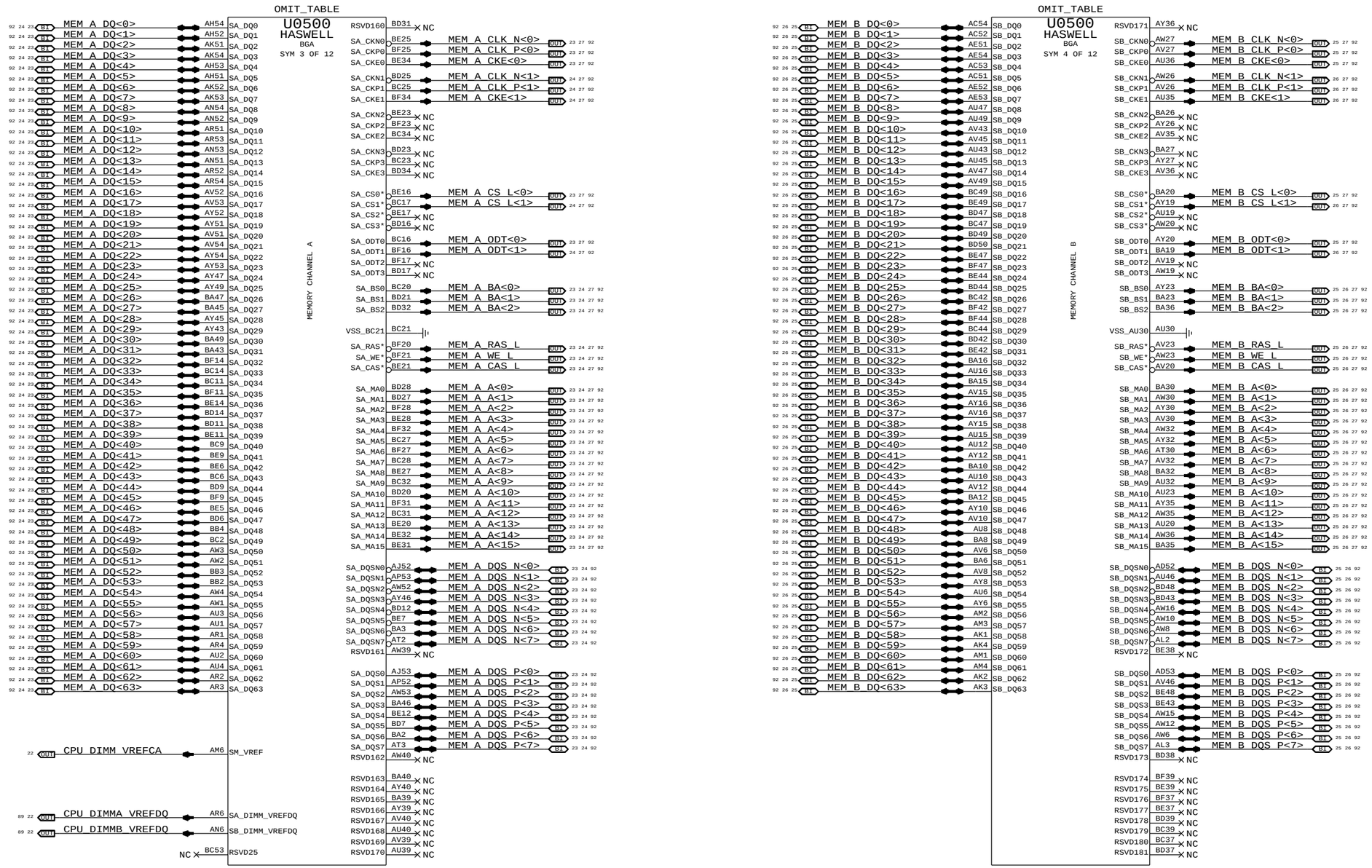

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CPU DDR3 Interfaces

Apple Inc.

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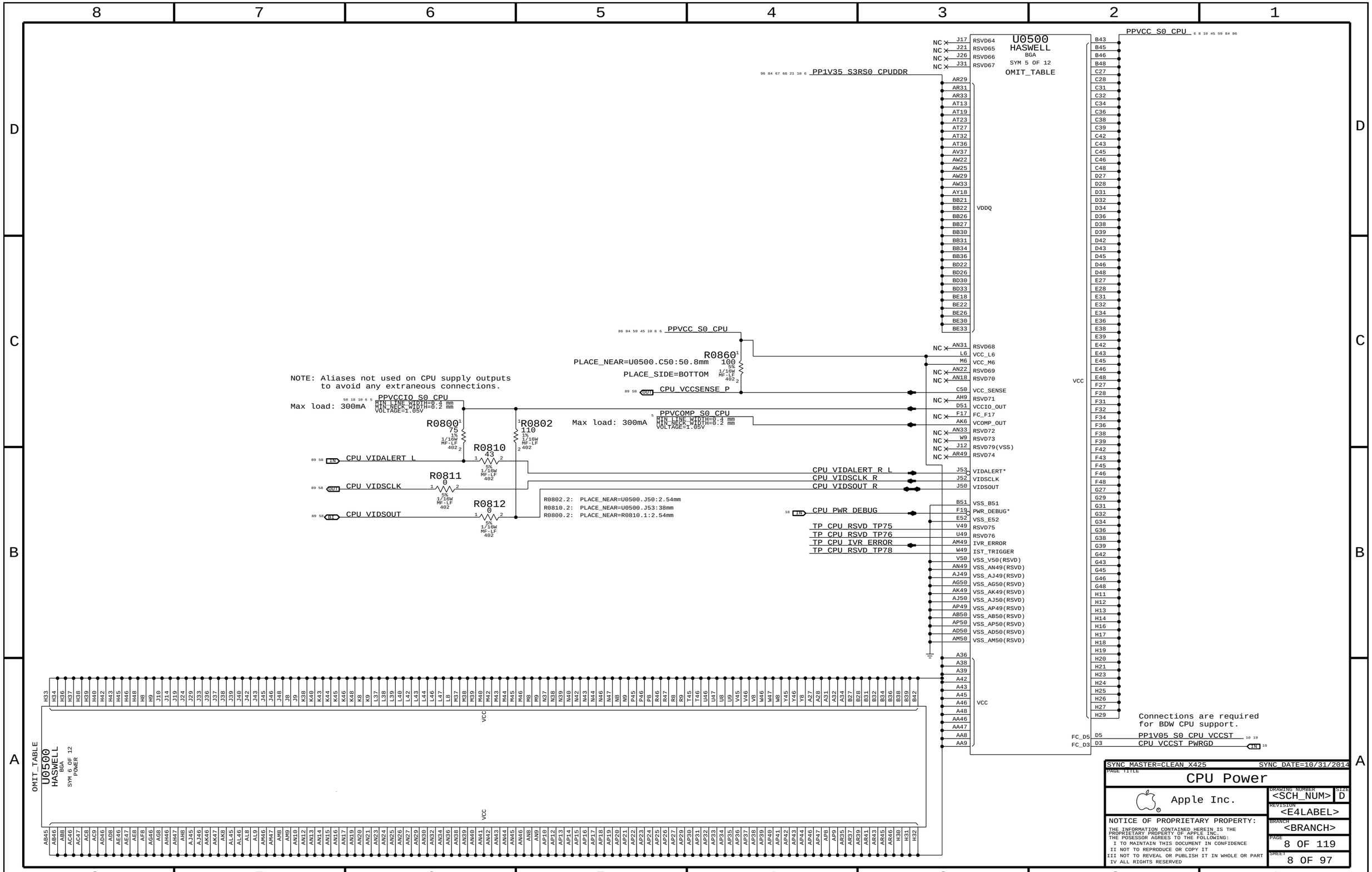
U0500
HASWELL
BGA
SYM 5 OF 12
OMIT_TABLE
PP1V35_S3RS0_CPUDDR
PPVCC_S0_CPU
VDDQ
VCC
VCC_SENSE
VCCIO_OUT
VCOMP_OUT
VIDALERT*
VIDSCLK
VIDSOUT
PWR_DEBUG*
IVR_ERROR
IST_TRIGGER
R0860
100
PLACE_NEAR=U0500.C50:50.8mm
PLACE_SIDE=BOTTOM
CPU_VCCSENSE_P
NOTE: Aliases not used on CPU supply outputs
to avoid any extraneous connections.
PPVCCIO_S0_CPU
Max load: 300mA
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
R0800
75
R0802
110
R0810
43
R0811
0
R0812
0
PPVCOMP_S0_CPU
Max load: 300mA
CPU_VIDALERT_L
CPU_VIDSCLK
CPU_VIDSOUT
CPU_VIDALERT_R_L
CPU_VIDSCLK_R
CPU_VIDSOUT_R
CPU_PWR_DEBUG
TP_CPU_RSVD_TP75
TP_CPU_RSVD_TP76
TP_CPU_IVR_ERROR
TP_CPU_RSVD_TP78
R0802.2: PLACE_NEAR=U0500.J50:2.54mm
R0810.2: PLACE_NEAR=U0500.J53:38mm
R0800.2: PLACE_NEAR=R0810.1:2.54mm
Connections are required
for BDW CPU support.
PP1V05_S0_CPU_VCCST
CPU_VCCST_PWRGD
OMIT_TABLE
U0500
HASWELL
BGA
SYM 6 OF 12
POWER
SYNC MASTER=CLEAN_X425
SYNC DATE=10/31/2014
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CPU Power
Apple Inc.
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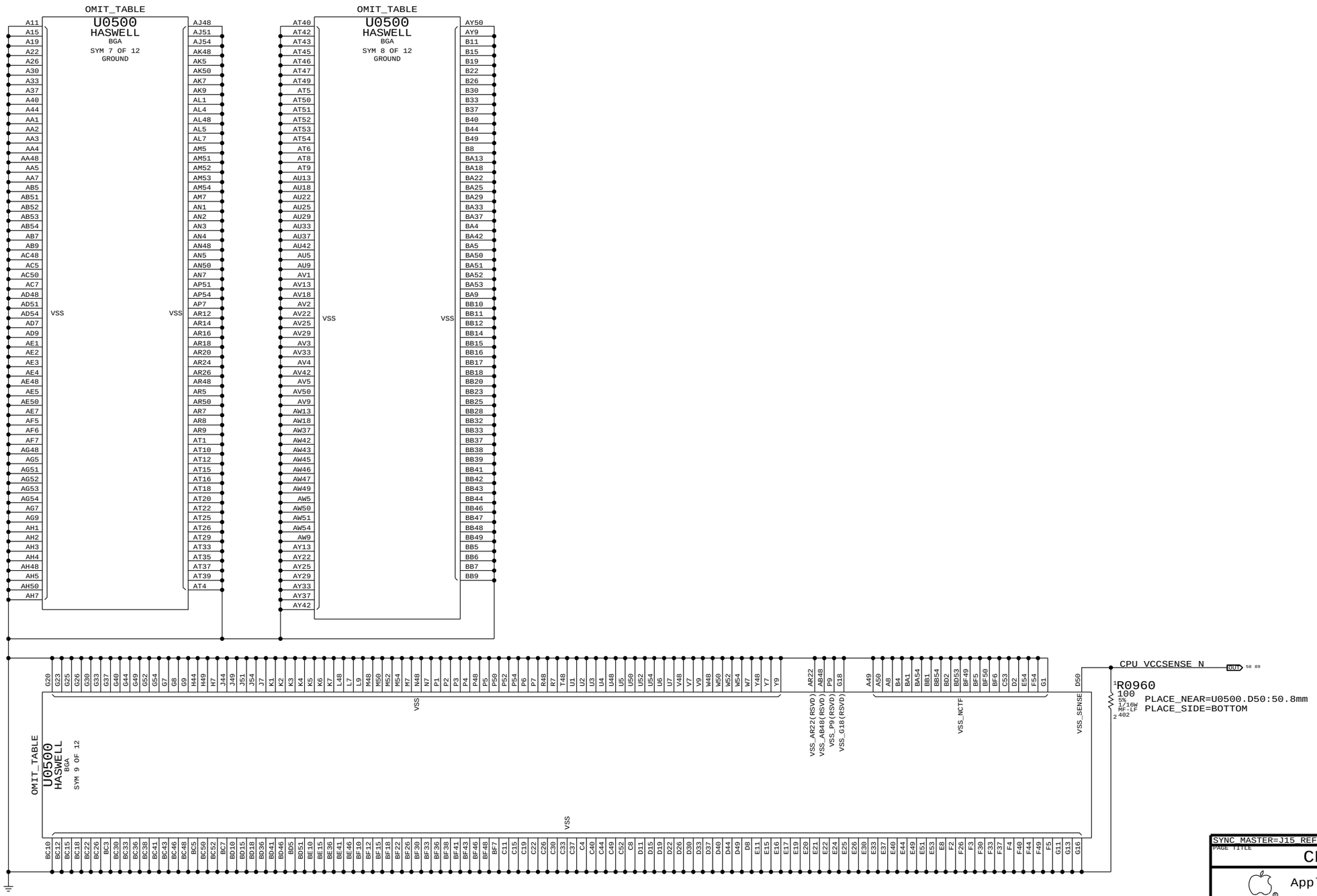

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CPU Ground

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CPU VCORE Decoupling

Intel recommendation: 4x 470uF 4mOhm (3 CPU-side, 1 opposite), 20x 22uF 0805 (10 CPU-side, 10 opposite near edge, 4x 10uF 0603 (2 CPU-side, 2 opposite), 20x 1uF 0402 (under CPU)
Apple Implementation: 9x 210uF 6mOhm, 44x 10uF 0402, 4x 10uF 0402, 20x 1uF 0402

86 84 59 45 8 6 PPVCC_S0_CPU

PLACEMENT_NOTE (C1000-C1019):
Place on bottom side of U0500

C1000 1UF 10% 10V X6S-CERM 0402 — NO STUFF
C1001 1UF 10% 10V X6S-CERM 0402 — NO STUFF
C1002 1UF 10% 10V X6S-CERM 0402 — NO STUFF
C1003 1UF 10% 10V X6S-CERM 0402
C1004 1UF 10% 10V X6S-CERM 0402
C1005 1UF 10% 10V X6S-CERM 0402
C1006 1UF 10% 10V X6S-CERM 0402
C1007 1UF 10% 10V X6S-CERM 0402
C1008 1UF 10% 10V X6S-CERM 0402
C1009 1UF 10% 10V X6S-CERM 0402
C1010 1UF 10% 10V X6S-CERM 0402
C1011 1UF 10% 10V X6S-CERM 0402
C1012 1UF 10% 10V X6S-CERM 0402
C1013 1UF 10% 10V X6S-CERM 0402
C1014 1UF 10% 10V X6S-CERM 0402
C1015 1UF 10% 10V X6S-CERM 0402
C1016 1UF 10% 10V X6S-CERM 0402
C1017 1UF 10% 10V X6S-CERM 0402
C1018 1UF 10% 10V X6S-CERM 0402
C1019 1UF 10% 10V X6S-CERM 0402

PLACEMENT_NOTE (C1020-C1023):
Place near U0500 on bottom side

C1020 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
C1021 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
C1022 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
C1023 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF

CAPS for Acoustic Control (C109A to C102D)

CRITICAL C109A 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C109B 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C109C 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C109D 20UF 20% 2.5V X6S-CERM 0402 — ACAPS:A1
CRITICAL C109E 20UF 20% 2.5V X6S-CERM 0402 — ACAPS:A1
CRITICAL C109F 20UF 20% 2.5V X6S-CERM 0402 — ACAPS:A2
CRITICAL C101A 20UF 20% 2.5V X6S-CERM 0402 — ACAPS:A1
CRITICAL C101B 20UF 20% 2.5V X6S-CERM 0402 — ACAPS:A1
CRITICAL C101C 20UF 20% 2.5V X6S-CERM 0402 — ACAPS:A1
CRITICAL C101D 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C101E 20UF 20% 2.5V X6S-CERM 0402 — ACAPS:A1
CRITICAL C101F 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C102A 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C102B 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C102C 20UF 20% 2.5V X6S-CERM 0402 — ACAPS:A2
CRITICAL C102D 20UF 20% 2.5V X6S-CERM 0402

PLACEMENT_NOTE (C1024-C1045):
Place near inductors on bottom side.

CRITICAL C1024 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C1025 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C1026 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C1027 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C1028 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C1029 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C1030 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C1031 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C1032 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C1033 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C1034 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C1035 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C1036 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C1037 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C1038 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C1039 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C1040 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C1041 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C1042 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C1043 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C1044 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C1045 20UF 20% 2.5V X6S-CERM 0402 — ACAPS:A2

PLACEMENT_NOTE (C1046-C1067):
Place near inductors on bottom side.

CRITICAL C1046 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C1047 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C1048 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C1049 20UF 20% 2.5V X6S-CERM 0402 — ACAPS:A1
CRITICAL C1050 20UF 20% 2.5V X6S-CERM 0402 — ACAPS:A2
CRITICAL C1051 20UF 20% 2.5V X6S-CERM 0402 — ACAPS:A1
CRITICAL C1052 20UF 20% 2.5V X6S-CERM 0402 — ACAPS:A1
CRITICAL C1053 20UF 20% 2.5V X6S-CERM 0402 — ACAPS:A2
CRITICAL C1054 20UF 20% 2.5V X6S-CERM 0402 — ACAPS:A2
CRITICAL C1055 20UF 20% 2.5V X6S-CERM 0402 — ACAPS:A1
CRITICAL C1056 20UF 20% 2.5V X6S-CERM 0402 — ACAPS:A2
CRITICAL C1057 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C1058 20UF 20% 2.5V X6S-CERM 0402 — ACAPS:A2
CRITICAL C1059 20UF 20% 2.5V X6S-CERM 0402 — ACAPS:A2
CRITICAL C1060 20UF 20% 2.5V X6S-CERM 0402 — ACAPS:A2
CRITICAL C1061 20UF 20% 2.5V X6S-CERM 0402 — ACAPS:A1
CRITICAL C1062 20UF 20% 2.5V X6S-CERM 0402 — ACAPS:A1
CRITICAL C1063 20UF 20% 2.5V X6S-CERM 0402 — ACAPS:A1
CRITICAL C1064 20UF 20% 2.5V X6S-CERM 0402 — ACAPS:A1
CRITICAL C1065 20UF 20% 2.5V X6S-CERM 0402 — ACAPS:A1
CRITICAL C1066 20UF 20% 2.5V X6S-CERM 0402 — ACAPS:A1
CRITICAL C1067 20UF 20% 2.5V X6S-CERM 0402

PLACEMENT_NOTE (C1068-C1076:
Place near inductors on bottom side.

CRITICAL C1068 210UF 20% 2.5V POLY-TANT CASE-B2S — NO STUFF
CRITICAL C1069 210UF 20% 2.5V POLY-TANT CASE-B2S — NO STUFF
CRITICAL C1070 210UF 20% 2.5V POLY-TANT CASE-B2S — NO STUFF
CRITICAL C1071 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1072 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1073 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1074 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1075 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1076 210UF 20% 2.5V POLY-TANT CASE-B2S — NO STUFF
CRITICAL C1077 330UF-9MOHM 20% 2.5V POLY-TANT D151-1 — NO STUFF

CAPS for Acoustic Control (C102E to C103F)

CRITICAL C102E 20UF 20% 2.5V X6S-CERM 0402 — ACAPS:A2
CRITICAL C102F 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C103A 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C103B 20UF 20% 2.5V X6S-CERM 0402 — NO STUFF
CRITICAL C103C 20UF 20% 2.5V X6S-CERM 0402 — ACAPS:A2
CRITICAL C103D 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C103E 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C103F 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C108D 12PF 5% NP0-C0G 0201 25V
CRITICAL C108E 12PF 5% NP0-C0G 0201 25V
CRITICAL C107A 3.0PF +/-0.1PF 25V NP0-C0G 0201

FOR DESENSE IMPROVEMENT
LOCATION DEPENDS ON DESENSE TEAM

CPU VDDQ Decoupling

Intel recommendation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 3x 270uF, 8x 10uF 0603, 10x 1uF 0402

67 66 23 8 6 96 84 PP1V35_S3RS0_CPUDDR

PLACEMENT_NOTE (C1080-C1089):
Place on bottom side of U0500

C1080 1UF 10% 10V X6S-CERM 0402
C1081 1UF 10% 10V X6S-CERM 0402
C1082 1UF 10% 10V X6S-CERM 0402
C1083 1UF 10% 10V X6S-CERM 0402
C1084 1UF 10% 10V X6S-CERM 0402
C1085 1UF 10% 10V X6S-CERM 0402
C1086 1UF 10% 10V X6S-CERM 0402
C1087 1UF 10% 10V X6S-CERM 0402
C1088 1UF 10% 10V X6S-CERM 0402
C1089 1UF 10% 10V X6S-CERM 0402

PLACEMENT_NOTE (C1090-C1097):
Place near U0500 on bottom side

C1090 10UF 20% 4V X6S 0402
C1091 10UF 20% 4V X6S 0402
C1092 10UF 20% 4V X6S 0402
C1093 10UF 20% 4V X6S 0402
C1094 10UF 20% 4V X6S 0402
C1095 10UF 20% 4V X6S 0402
C1096 10UF 20% 4V X6S 0402
C1097 10UF 20% 4V X6S 0402
CRITICAL C108B 12PF 5% NP0-C0G 0201 25V
CRITICAL C108C 12PF 5% NP0-C0G 0201 25V
CRITICAL C107B 3.0PF +/-0.1PF 25V NP0-C0G 0201

FOR DESENSE IMPROVEMENT
LOCATION DEPENDS ON DESENSE TEAM

PLACEMENT_NOTE (C1098-C1099):

CRITICAL C1098 270UF 20% 2V TANT CASE-B2-SM
CRITICAL C1099 270UF 20% 2V TANT CASE-B2-SM
CRITICAL C108A 270UF 20% 2V TANT CASE-B2-SM

(Z = 2mm, place on tall side next to CPU & under heat pipe)

C1098, C1099 and C108A use B size caps due to EG board placement constraints.

CPU VCCIO Decoupling

Intel recommendation: 2x 0.01uF 0402 (1 near CPU, 1 near SVID pull-ups)
Apple Implementation: 2x 0.01uF 0402 (second cap is on CPU VR page)

58 18 8 6 5 PPVCCIO_S0_CPU

C1079 0.01UF 10% 16V X7R-CERM 0402

CPU VCCST Decoupling

Intel recommendation: 1x 0.1uF 0402, 1x 4.7uF 0805
Apple Implementation: 1x 0.1uF 0201, 1x 4.7uF 0402

86 84 67 62 41 18 17 15 14 PP1V05_S0

BDW_SPRT R1080 0 5% 1/10W MF-LF 603

19 8 PP1V05_S0_CPU_VCCST
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

PLACE_NEAR=U0500.D5:25.4mm
PLACE_NEAR=U0500.D5:12.7mm

BDW_SPRT C106A 0.1UF 10% 6.3V CERM-X5R 0201
BDW_SPRT C106B 4.7UF 20% 6.3V X5R 402

NOTE: Intel decoupling recommendations from Shark Bay Mobile Platform Power Delivery Design Guide (doc #487822, Rev 0.8 dated January 2012), Section 5.

SYNC_MASTER=CLEAN_X305G SYNC_DATE=08/11/2014

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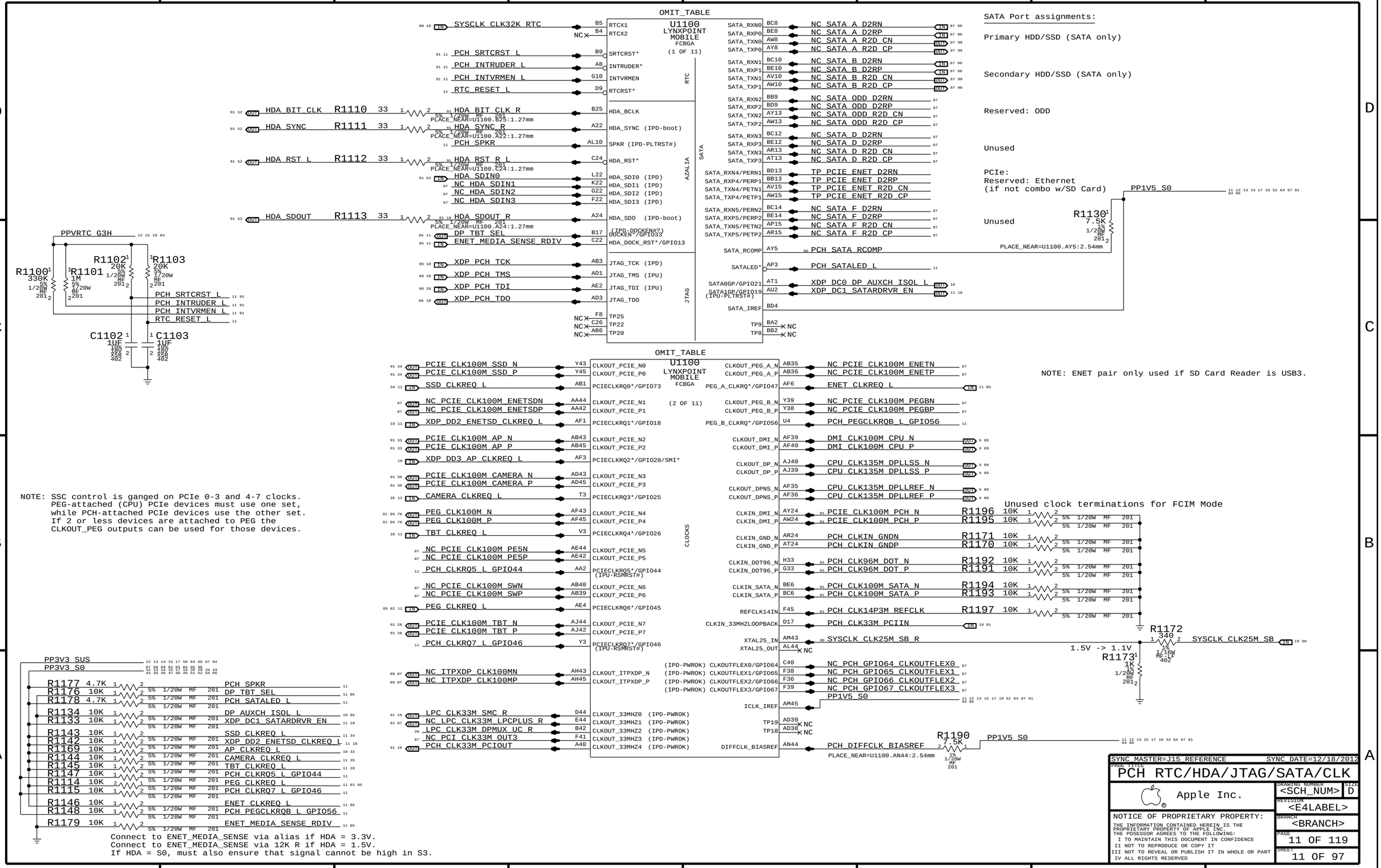
OMIT_TABLE
U1100
LYNXPOINT
MOBILE
FCBGA
(1 OF 11)
(2 OF 11)
RTC
SATA
AZALIA
JTAG
CLOCKS
SYSCLK CLK32K RTC
PCH SRTCRST L
PCH INTRUDER L
PCH INTVRMEN L
RTC RESET L
HDA BIT CLK
HDA SYNC
HDA RST L
HDA SDOUT
R1110 33
R1111 33
R1112 33
R1113 33
HDA BIT CLK R
HDA SYNC R
HDA RST R L
PLACE_NEAR=U1100.B25:1.27mm
PLACE_NEAR=U1100.A22:1.27mm
PLACE_NEAR=U1100.C24:1.27mm
PLACE_NEAR=U1100.A24:1.27mm
PCH SPKR
HDA SDIN0
NC HDA SDIN1
NC HDA SDIN2
NC HDA SDIN3
HDA SDOUT R
DP TBT SEL
ENET_MEDIA_SENSE_RDIV
XDP PCH TCK
XDP PCH TMS
XDP PCH TDI
XDP PCH TDO
NC SATA A D2RN
NC SATA A D2RP
NC SATA A R2D CN
NC SATA A R2D CP
NC SATA B D2RN
NC SATA B D2RP
NC SATA B R2D CN
NC SATA B R2D CP
NC SATA ODD D2RN
NC SATA ODD D2RP
NC SATA ODD R2D CN
NC SATA ODD R2D CP
NC SATA D D2RN
NC SATA D D2RP
NC SATA D R2D CN
NC SATA D R2D CP
TP PCIE ENET D2RN
TP PCIE ENET D2RP
TP PCIE ENET R2D CN
TP PCIE ENET R2D CP
NC SATA F D2RN
NC SATA F D2RP
NC SATA F R2D CN
NC SATA F R2D CP
PCH SATA RCOMP
PCH SATALED L
XDP DC0 DP AUXCH ISOL L
XDP DC1 SATARDRVR EN
SATA Port assignments:
Primary HDD/SSD (SATA only)
Secondary HDD/SSD (SATA only)
Reserved: ODD
Unused
PCIe:
Reserved: Ethernet
(if not combo w/SD Card)
Unused
PP1V5 S0
R1130 7.5K
PLACE_NEAR=U1100.AY5:2.54mm
PPVRTC G3H
R1100 330K
R1101 1M
R1102 20K
R1103 20K
C1102 1UF
C1103 1UF
PCH SRTCRST L
PCH INTRUDER L
PCH INTVRMEN L
RTC RESET L
PCIE CLK100M SSD N
PCIE CLK100M SSD P
SSD CLKREQ L
NC PCIE CLK100M ENETSDN
NC PCIE CLK100M ENETSDP
XDP DD2 ENETSD CLKREQ L
PCIE CLK100M AP N
PCIE CLK100M AP P
XDP DD3 AP CLKREQ L
PCIE CLK100M CAMERA N
PCIE CLK100M CAMERA P
CAMERA CLKREQ L
PEG CLK100M N
PEG CLK100M P
TBT CLKREQ L
NC PCIE CLK100M PE5N
NC PCIE CLK100M PE5P
PCH CLKRQ5 L GPIO44
NC PCIE CLK100M SWN
NC PCIE CLK100M SWP
PEG CLKREQ L
PCIE CLK100M TBT N
PCIE CLK100M TBT P
PCH CLKRQ7 L GPIO46
NC ITPXDP CLK100MN
NC ITPXDP CLK100MP
LPC CLK33M SMC R
NC LPC CLK33M LPCPLUS R
LPC CLK33M DPMUX UC R
NC PCI CLK33M OUT3
PCH CLK33M PCIOUT
NC PCIE CLK100M ENETN
NC PCIE CLK100M ENETP
ENET CLKREQ L
NC PCIE CLK100M PEGBN
NC PCIE CLK100M PEGBP
PCH PEGCLKRQB L GPIO56
DMI CLK100M CPU N
DMI CLK100M CPU P
CPU CLK135M DPLLSS N
CPU CLK135M DPLLSS P
CPU CLK135M DPLLREF N
CPU CLK135M DPLLREF P
PCIE CLK100M PCH N
PCIE CLK100M PCH P
PCH CLKIN GNDN
PCH CLKIN GNDP
PCH CLK96M DOT N
PCH CLK96M DOT P
PCH CLK100M SATA N
PCH CLK100M SATA P
PCH CLK14P3M REFCLK
PCH CLK33M PCIIN
SYSCLK CLK25M SB R
NC PCH GPIO64 CLKOUTFLEX0
NC PCH GPIO65 CLKOUTFLEX1
NC PCH GPIO66 CLKOUTFLEX2
NC PCH GPIO67 CLKOUTFLEX3
PP1V5 S0
PCH DIFFCLK BIASREF
PLACE_NEAR=U1100.AN44:2.54mm
R1190 7.5K
Unused clock terminations for FCIM Mode
R1196 10K
R1195 10K
R1171 10K
R1170 10K
R1192 10K
R1191 10K
R1194 10K
R1193 10K
R1197 10K
R1172 340
SYSCLK CLK25M SB
1.5V -> 1.1V
R1173 1K
NOTE: ENET pair only used if SD Card Reader is USB3.
NOTE: SSC control is ganged on PCIe 0-3 and 4-7 clocks.
PEG-attached (CPU) PCIe devices must use one set,
while PCH-attached PCIe devices use the other set.
If 2 or less devices are attached to PEG the
CLKOUT_PEG outputs can be used for those devices.
PP3V3 SUS
PP3V3 S0
R1177 4.7K PCH SPKR
R1176 10K DP TBT SEL
R1178 4.7K PCH SATALED L
R1134 10K DP AUXCH ISOL L
R1133 10K XDP DC1 SATARDRVR EN
R1143 10K SSD CLKREQ L
R1142 10K XDP DD2 ENETSD CLKREQ L
R1169 10K AP CLKREQ L
R1144 10K CAMERA CLKREQ L
R1145 10K TBT CLKREQ L
R1147 10K PCH CLKRQ5 L GPIO44
R1114 10K PEG CLKREQ L
R1115 10K PCH CLKRQ7 L GPIO46
R1146 10K ENET CLKREQ L
R1148 10K PCH PEGCLKRQB L GPIO56
R1179 10K ENET MEDIA SENSE RDIV
Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.
SYNC_MASTER=J15_REFERENCE
SYNC_DATE=12/18/2012
PAGE TITLE
PCH RTC/HDA/JTAG/SATA/CLK
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
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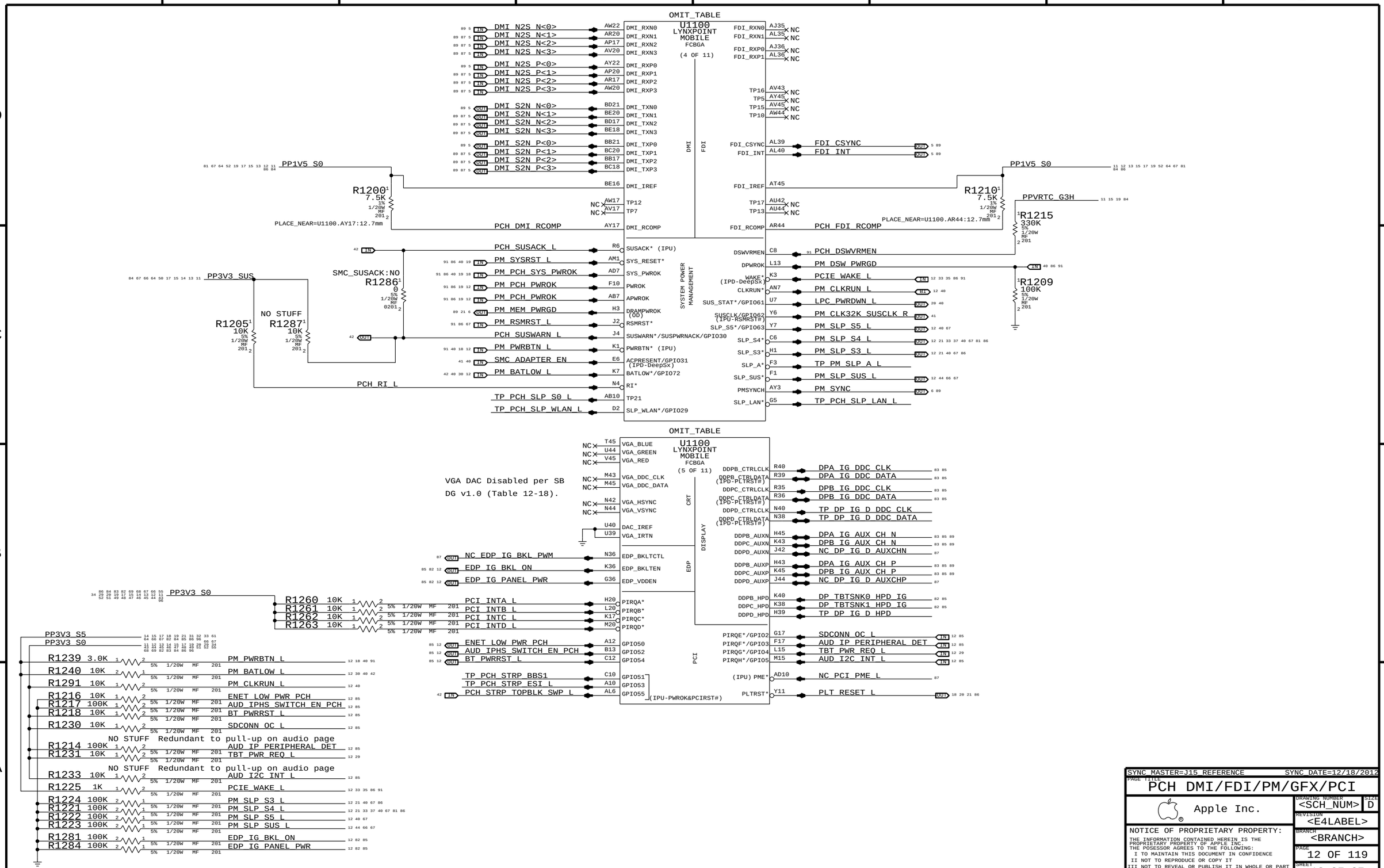

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE
PCH DMI/FDI/PM/GFX/PCI

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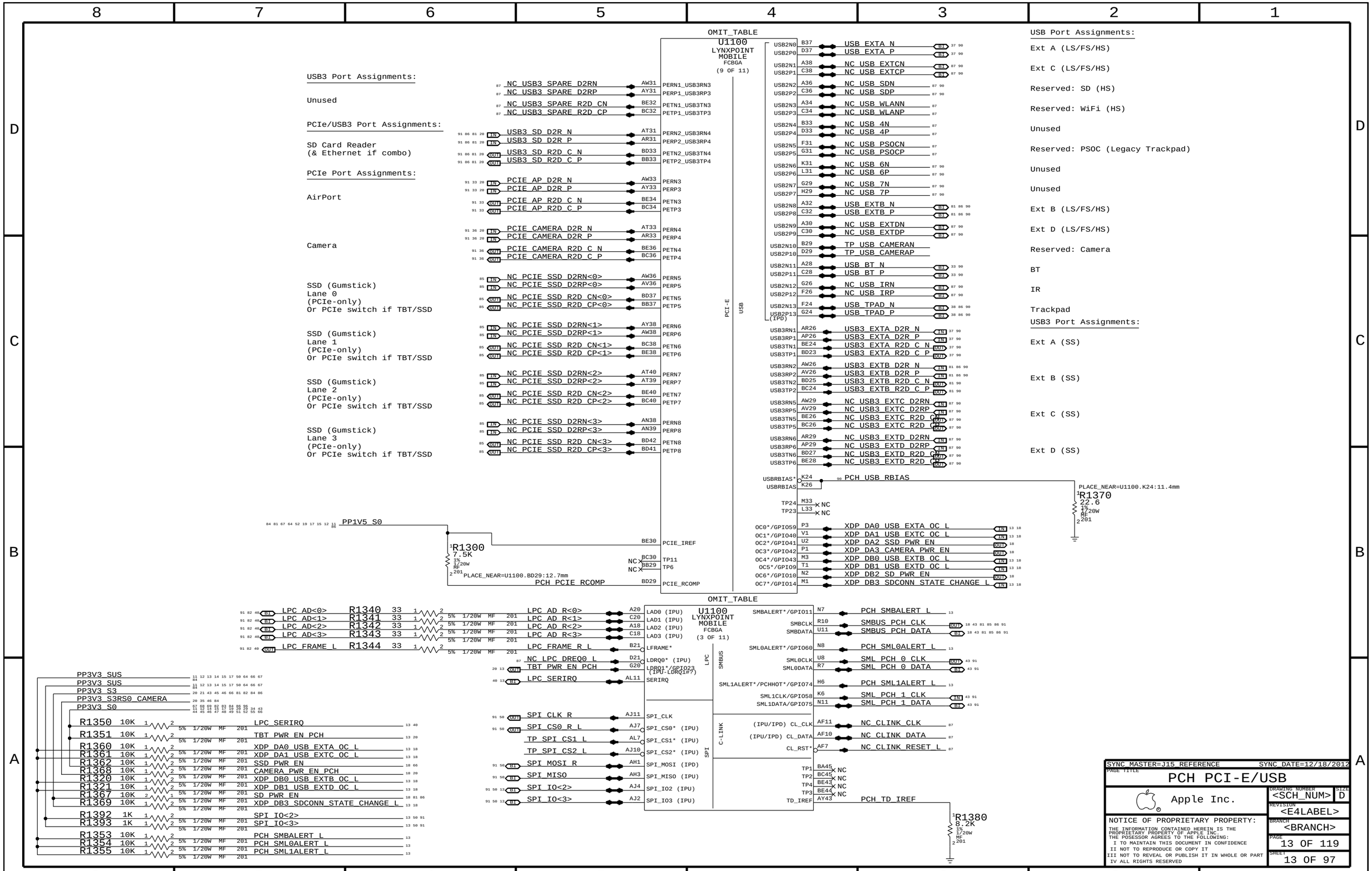
OMIT_TABLE
U1100
LYNXPOINT
MOBILE
FCBGA
(9 OF 11)
USB3 Port Assignments:
Unused
PCIe/USB3 Port Assignments:
SD Card Reader
(& Ethernet if combo)
PCIe Port Assignments:
AirPort
Camera
SSD (Gumstick)
Lane 0
(PCIe-only)
Or PCIe switch if TBT/SSD
SSD (Gumstick)
Lane 1
(PCIe-only)
Or PCIe switch if TBT/SSD
SSD (Gumstick)
Lane 2
(PCIe-only)
Or PCIe switch if TBT/SSD
SSD (Gumstick)
Lane 3
(PCIe-only)
Or PCIe switch if TBT/SSD
NC_USB3_SPARE_D2RN
NC_USB3_SPARE_D2RP
NC_USB3_SPARE_R2D_CN
NC_USB3_SPARE_R2D_CP
USB3_SD_D2R_N
USB3_SD_D2R_P
USB3_SD_R2D_C_N
USB3_SD_R2D_C_P
PCIE_AP_D2R_N
PCIE_AP_D2R_P
PCIE_AP_R2D_C_N
PCIE_AP_R2D_C_P
PCIE_CAMERA_D2R_N
PCIE_CAMERA_D2R_P
PCIE_CAMERA_R2D_C_N
PCIE_CAMERA_R2D_C_P
NC_PCIE_SSD_D2RN<0>
NC_PCIE_SSD_D2RP<0>
NC_PCIE_SSD_R2D_CN<0>
NC_PCIE_SSD_R2D_CP<0>
NC_PCIE_SSD_D2RN<1>
NC_PCIE_SSD_D2RP<1>
NC_PCIE_SSD_R2D_CN<1>
NC_PCIE_SSD_R2D_CP<1>
NC_PCIE_SSD_D2RN<2>
NC_PCIE_SSD_D2RP<2>
NC_PCIE_SSD_R2D_CN<2>
NC_PCIE_SSD_R2D_CP<2>
NC_PCIE_SSD_D2RN<3>
NC_PCIE_SSD_D2RP<3>
NC_PCIE_SSD_R2D_CN<3>
NC_PCIE_SSD_R2D_CP<3>
PERN1_USB3RN3
PERP1_USB3RP3
PETN1_USB3TN3
PETP1_USB3TP3
PERN2_USB3RN4
PERP2_USB3RP4
PETN2_USB3TN4
PETP2_USB3TP4
PERN3
PERP3
PETN3
PETP3
PERN4
PERP4
PETN4
PETP4
PERN5
PERP5
PETN5
PETP5
PERN6
PERP6
PETN6
PETP6
PERN7
PERP7
PETN7
PETP7
PERN8
PERP8
PETN8
PETP8
PCIE_IREF
TP11
TP6
PCIE_RCOMP
PCI-E
USB
USB2N0
USB2P0
USB2N1
USB2P1
USB2N2
USB2P2
USB2N3
USB2P3
USB2N4
USB2P4
USB2N5
USB2P5
USB2N6
USB2P6
USB2N7
USB2P7
USB2N8
USB2P8
USB2N9
USB2P9
USB2N10
USB2P10
USB2N11
USB2P11
USB2N12
USB2P12
USB2N13
USB2P13
(IPD)
USB_EXTA_N
USB_EXTA_P
NC_USB_EXTCN
NC_USB_EXTCP
NC_USB_SDN
NC_USB_SDP
NC_USB_WLANN
NC_USB_WLANP
NC_USB_4N
NC_USB_4P
NC_USB_PSOCN
NC_USB_PSOCP
NC_USB_6N
NC_USB_6P
NC_USB_7N
NC_USB_7P
USB_EXTB_N
USB_EXTB_P
NC_USB_EXTDN
NC_USB_EXTDP
TP_USB_CAMERAN
TP_USB_CAMERAP
USB_BT_N
USB_BT_P
NC_USB_IRN
NC_USB_IRP
USB_TPAD_N
USB_TPAD_P
USB Port Assignments:
Ext A (LS/FS/HS)
Ext C (LS/FS/HS)
Reserved: SD (HS)
Reserved: WiFi (HS)
Unused
Reserved: PSOC (Legacy Trackpad)
Unused
Unused
Ext B (LS/FS/HS)
Ext D (LS/FS/HS)
Reserved: Camera
BT
IR
Trackpad
USB3 Port Assignments:
Ext A (SS)
Ext B (SS)
Ext C (SS)
Ext D (SS)
USB3RN1
USB3RP1
USB3TN1
USB3TP1
USB3RN2
USB3RP2
USB3TN2
USB3TP2
USB3RN5
USB3RP5
USB3TN5
USB3TP5
USB3RN6
USB3RP6
USB3TN6
USB3TP6
USB3_EXTA_D2R_N
USB3_EXTA_D2R_P
USB3_EXTA_R2D_C_N
USB3_EXTA_R2D_C_P
USB3_EXTB_D2R_N
USB3_EXTB_D2R_P
USB3_EXTB_R2D_C_N
USB3_EXTB_R2D_C_P
NC_USB3_EXTC_D2RN
NC_USB3_EXTC_D2RP
NC_USB3_EXTC_R2D_CN
NC_USB3_EXTC_R2D_CP
NC_USB3_EXTD_D2RN
NC_USB3_EXTD_D2RP
NC_USB3_EXTD_R2D_CN
NC_USB3_EXTD_R2D_CP
USBRBIAS*
USBRBIAS
PCH_USB_RBIAS
PLACE_NEAR=U1100.K24:11.4mm
R1370
22.6
1%
1/20W
MF
201
TP24
TP23
NC
OC0*/GPIO59
OC1*/GPIO40
OC2*/GPIO41
OC3*/GPIO42
OC4*/GPIO43
OC5*/GPIO9
OC6*/GPIO16
OC7*/GPIO14
XDP_DA0_USB_EXTA_OC_L
XDP_DA1_USB_EXTC_OC_L
XDP_DA2_SSD_PWR_EN
XDP_DA3_CAMERA_PWR_EN
XDP_DB0_USB_EXTB_OC_L
XDP_DB1_USB_EXTD_OC_L
XDP_DB2_SD_PWR_EN
XDP_DB3_SDCONN_STATE_CHANGE_L
PP1V5_S0
R1300
7.5K
1%
1/20W
MF
201
PLACE_NEAR=U1100.BD29:12.7mm
PCH_PCIE_RCOMP
OMIT_TABLE
U1100
LYNXPOINT
MOBILE
FCBGA
(3 OF 11)
LPC
SMBUS
C-LINK
SPI
LAD0 (IPU)
LAD1 (IPU)
LAD2 (IPU)
LAD3 (IPU)
LFRAME*
LDRQ0* (IPU)
LDRQ1*/GPIO23
(IPU-LDRQ1#7)
SERIRQ
SPI_CLK
SPI_CS0* (IPU)
SPI_CS1* (IPU)
SPI_CS2* (IPU)
SPI_MOSI (IPD)
SPI_MISO (IPU)
SPI_IO2 (IPU)
SPI_IO3 (IPU)
LPC_AD<0>
LPC_AD<1>
LPC_AD<2>
LPC_AD<3>
LPC_FRAME_L
NC_LPC_DREQ0_L
TBT_PWR_EN_PCH
LPC_SERIRQ
SPI_CLK_R
SPI_CS0_R_L
TP_SPI_CS1_L
TP_SPI_CS2_L
SPI_MOSI_R
SPI_MISO
SPI_IO<2>
SPI_IO<3>
R1340
R1341
R1342
R1343
R1344
33
5%
1/20W
MF
201
LPC_AD_R<0>
LPC_AD_R<1>
LPC_AD_R<2>
LPC_AD_R<3>
LPC_FRAME_R_L
SMBALERT*/GPIO11
SMBCLK
SMBDATA
SML0ALERT*/GPIO60
SML0CLK
SML0DATA
SML1ALERT*/PCHHOT*/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
(IPU/IPD) CL_CLK
(IPU/IPD) CL_DATA
CL_RST*
TP1
TP2
TP4
TP3
TD_IREF
PCH_SMBALERT_L
SMBUS_PCH_CLK
SMBUS_PCH_DATA
PCH_SML0ALERT_L
SML_PCH_0_CLK
SML_PCH_0_DATA
PCH_SML1ALERT_L
SML_PCH_1_CLK
SML_PCH_1_DATA
NC_CLINK_CLK
NC_CLINK_DATA
NC_CLINK_RESET_L
PCH_TD_IREF
R1380
8.2K
1%
1/20W
MF
201
PP3V3_SUS
PP3V3_SUS
PP3V3_S3
PP3V3_S3RS0_CAMERA
PP3V3_S0
R1350 10K LPC_SERIRQ
R1351 10K TBT_PWR_EN_PCH
R1360 10K XDP_DA0_USB_EXTA_OC_L
R1361 10K XDP_DA1_USB_EXTC_OC_L
R1362 10K SSD_PWR_EN
R1368 10K CAMERA_PWR_EN_PCH
R1320 10K XDP_DB0_USB_EXTB_OC_L
R1321 10K XDP_DB1_USB_EXTD_OC_L
R1367 10K SD_PWR_EN
R1369 10K XDP_DB3_SDCONN_STATE_CHANGE_L
R1392 1K SPI_IO<2>
R1393 1K SPI_IO<3>
R1353 10K PCH_SMBALERT_L
R1354 10K PCH_SML0ALERT_L
R1355 10K PCH_SML1ALERT_L
5%
1/20W
MF
201
SYNC MASTER=J15 REFERENCE
SYNC DATE=12/18/2012
PAGE TITLE
PCH PCI-E/USB
Apple Inc.
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Pull-up/down on chipset support page (depends on TBT controller)
Falcon Ridge: TBT_CIO_PLUG_EVENT_L, requires pull-up (S0), no isolation necessary.
Cactus Ridge: TBT_CIO_PLUG_EVENT, requires pull-down & isolation.

OMIT_TABLE

U1100
LYNXPOINT MOBILE
FCBGA
(6 OF 11)

TBT_CIO_PLUG_EVENT_L	IN	AT8	BMBUSY*/GPIO0
FW_PME_L	IN	F13	TACH1/GPIO1
DPMUX_UC_IRQ	IN	A14	TACH2/GPIO6
SMC_RUNTIME_SCI_L	IN	G15	TACH3/GPIO7
XDP_FC0_HDD_PWR_EN	OUT	Y1	GPIO8 (IPU-RSMRST#)
WOL_EN	OUT	K13	LAN_PHY_PWR_CTRL/GPIO12
MEM_VDD_SEL_1V5_L	OUT	AB11	GPIO15
XDP_DD0_SSD_PCIE_SEL_L	IN	AN2	SATA4GP/GPIO16 (IPU-Boot/SATA4GP?)
LPCPLUS_GPIO	BI	C14	TACH0/GPIO17
JTAG_TBT_TMS_PCH	OUT	BB4	SCLOCK/GPIO22
TBT_GO2SX_BIDIR	BI	Y10	GPIO24
SMC_WAKE_SCI_L	IN	R11	GPIO27 (IPU-DeepSx)
ISOLATE_CPU_MEM_L	OUT	AD11	GPIO28
TBT_POC_RESET_L	OUT	AN6	GPIO34
XDP_FC1_GPU_GOOD	OUT	AP1	GPIO35/NMI*
XDP_DC2_ODD_PWR_EN_L	OUT	AT3	SATA2GP/GPIO36 (IPD-PLTRST#)
XDP_DC3_JTAG_ISP_TCK	OUT	AK1	SATA3GP/GPIO37 (IPD-PLTRST#)
JTAG_ISP_TDO	IN	AT7	SLOAD/GPIO38
JTAG_ISP_TDI	OUT	AM3	SDATAOUT0/GPIO39
FW_PWR_EN_PCH	OUT	AN4	SDATAOUT1/GPIO48
XDP_DD1_MLB_RAMCFG1		AK3	SATA5GP/GPIO49 (IPU-Boot/SATA5GP?)
SPIROM_USE_MLB	BI	U12	GPIO57
MLB_RAMCFG3		C16	TACH4/GPIO68
MLB_RAMCFG2		D13	TACH5/GPIO69
SD_SEL_PCIE_L_USB_H	IN	G13	TACH6/GPIO70 (IPU-Boot?)
MLB_RAMCFG0		H15	TACH7/GPIO71 (IPU-Boot?)
		BE41, BE5, C45, A5	VSS

GPIO

CPU/MISC

TP14	AN10	PCH_A20GATE
(IPD) PECI	AY1	PCH_PECI
RCIN*	AT6	PCH_RCIN_L
PROCPWRGD	AV3	PCH_PROCPWRGD
THRMTRIP*	AV1	PM_THRMTRIP_L_R
PLTRST_PROC*	AU4	CPU_RESET_L
VSS	N10	
VSS	A2, A41, A43, A44, B1, B2, B44, B45, BA1, BC1, BD1, BD2, BD44, BD45, BE2, BE3, D1, E1, E45, A4	

PP1V05_S0
BDW_SPRT
R1457 1K 5% 1/16W MF-LP 402

R1470 43 NO STUFF 5% 1/20W MF 201 — CPU_PECI
R1440 0 5% 1/20W MF 0201 — CPU_PWRGD
R1456 390 5% 1/20W MF 201 — PM_THRMTRIP_L
CRW_SPRT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	1	RES,MF,1A MAX,0.0 OHM,5%,0201,BLACK	R1456		BDW_SPRT

PP3V3_S0

R1475	10K	5% 1/20W MF 201	RAMCFG0:H
R1474	10K	5% 1/20W MF 201	RAMCFG1:H
R1473	10K	5% 1/20W MF 201	RAMCFG2:H
R1472	10K	5% 1/20W MF 201	RAMCFG3:H

BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.

PP3V3_S5
PP3V3_SUS
PP3V3_S0

NOTE: GPIO0 pull-up/down on project-specific page

R1485	10K	5% 1/20W MF 201	FW_PME_L
R1411	20K	5% 1/20W MF 201	DPMUX_UC_IRQ
R1496	10K	5% 1/20W MF 201	SMC_RUNTIME_SCI_L
R1494	10K	5% 1/20W MF 201	WOL_EN
R1489	10K	5% 1/20W MF 201	MEM_VDD_SEL_1V5_L
R1495	100K	5% 1/20W MF 201	XDP_DD0_SSD_PCIE_SEL_L
R1490	100K	5% 1/20W MF 201	LPCPLUS_GPIO
R1412	10K	5% 1/20W MF 201	JTAG_TBT_TMS_PCH
R1492	10K	5% 1/20W MF 201	TBT_GO2SX_BIDIR
R1491	10K	5% 1/20W MF 201	SMC_WAKE_SCI_L
R1498	10K	5% 1/20W MF 201	XDP_DC2_ODD_PWR_EN_L
R1413	10K	5% 1/20W MF 201	JTAG_ISP_TCK
R1486	10K	5% 1/20W MF 201	JTAG_ISP_TDO
R1499	10K	5% 1/20W MF 201	JTAG_ISP_TDI
R1484	10K	5% 1/20W MF 201	FW_PWR_EN_PCH
R1493	100K	5% 1/20W MF 201	SPIROM_USE_MLB

NOTE: GPIO70 pull-up/down on project-specific page

R1450	10K		PCH_A20GATE
R1455	10K	5% 1/20W MF 201	PCH_RCIN_L

SYNC_MASTER=CLEAN_X425 SYNC_DATE=10/31/2014

PAGE TITLE
PCH GPIO/MISC/NCTF

Apple Inc.

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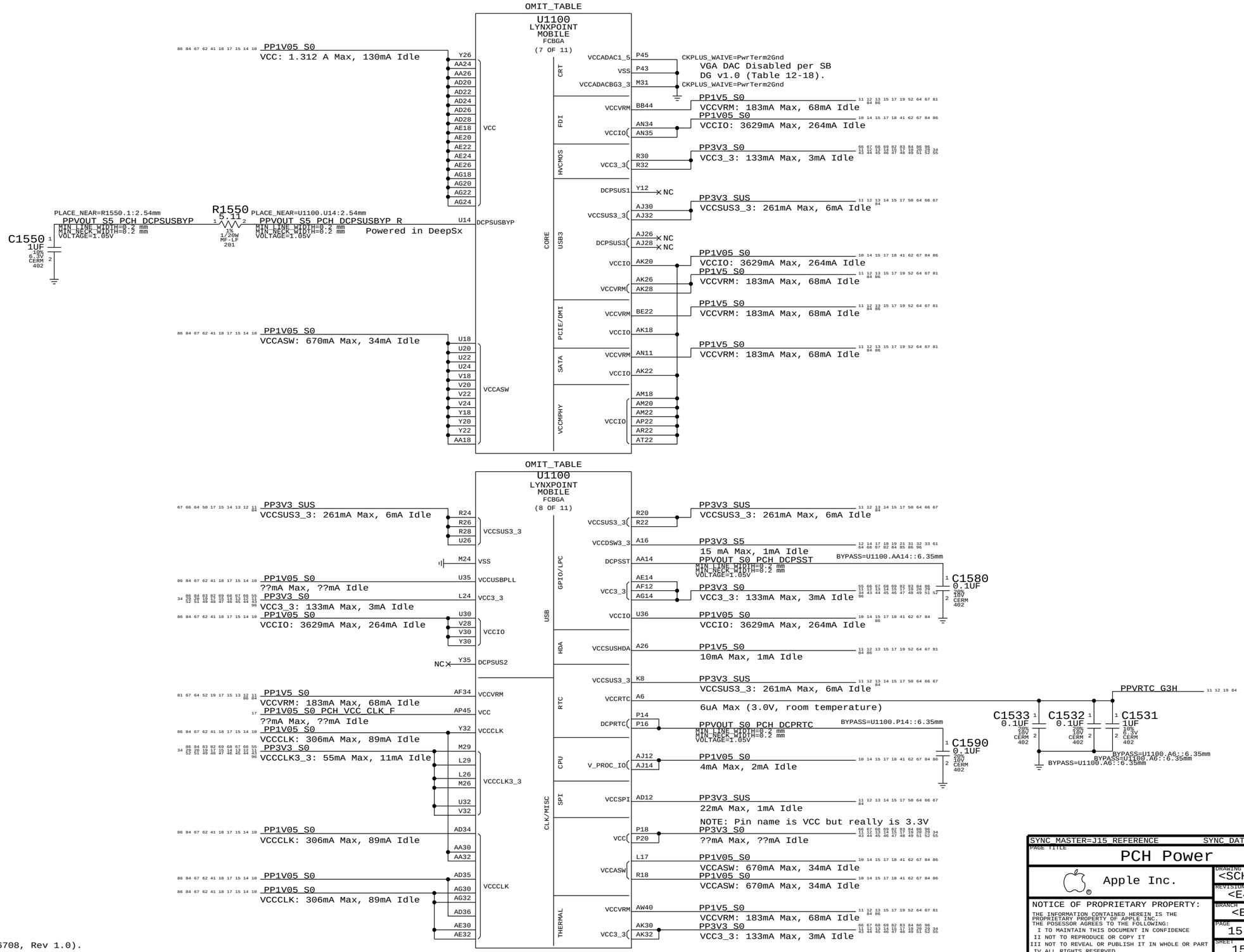

Current data from LPT EDS (doc #486708, Rev 1.0).

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

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PCH Power

Apple Inc.

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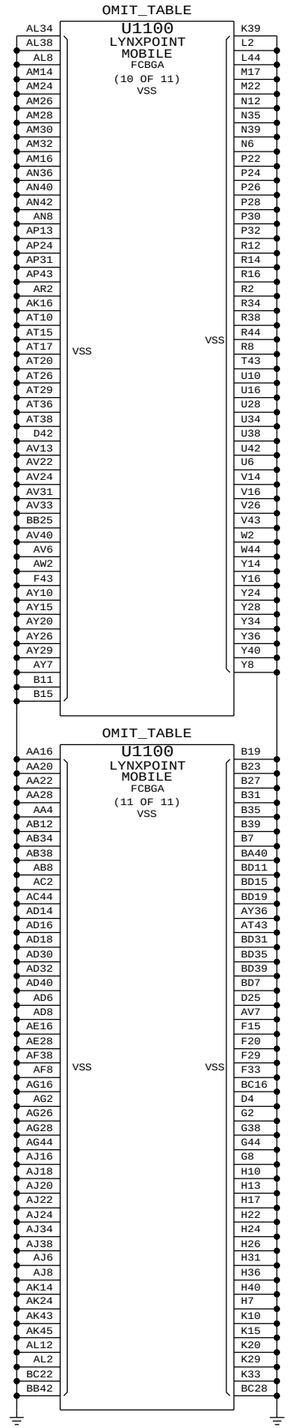

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE

PCH Grounds

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR)
PP3V3_S5

C1700 0.1UF 10% 25V X7R-CERM 0402
BYPASS=U1100.A16::6.35mm

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR)
PP3V3_SUS

C1702 1.0UF 10% 6.3V X6S 0402
BYPASS=U1100.AD12::6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR)
PP3V3_SUS

C1704 0.1UF 10% 25V X7R-CERM 0402
BYPASS=U1100.R20::6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND USB PWR)
PP3V3_SUS

C1706 0.1UF 10% 25V X7R-CERM 0402
BYPASS=U1100.R26::6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND RTC PWR)
PP3V3_SUS

C1708 1.0UF 10% 6.3V X6S 0402
BYPASS=U1100.K8::6.35mm

PCH VCCSUSHDA BYPASS
(PCH 3.3V/1.5V HDA PWR)
PP1V5_S0

C1710 0.1UF 10% 25V X7R-CERM 0402
BYPASS=U1100.A26::6.35mm

PCH VCCCLK3_3 BYPASS
(PCH 3.3V CLK PWR)
PP3V3_S0

C1720 1.0UF 10% 6.3V X6S 0402
C1721 1.0UF 10% 6.3V X6S 0402
C1722 1.0UF 10% 6.3V X6S 0402
C1723 1.0UF 10% 6.3V X6S 0402
BYPASS=U1100.L26::6.35mm
BYPASS=U1100.L29::6.35mm
BYPASS=U1100.M29::6.35mm
BYPASS=U1100.U32::6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V HVCMOS PWR)
PP3V3_S0

C1726 0.1UF 10% 25V X7R-CERM 0402
BYPASS=U1100.R30::6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR)
PP3V3_S0

C1728 0.01UF 10% 16V X7R-CERM 0402
BYPASS=U1100.AE14::6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V USB2 PWR)
PP3V3_S0

C1730 0.1UF 10% 25V X7R-CERM 0402
BYPASS=U1100.L24::6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR)
PP3V3_S0

C1732 0.1UF 10% 25V X7R-CERM 0402
BYPASS=U1100.AK30::6.35mm

PCH VCC BYPASS
(PCH 3.3V FUSE PWR)
PP3V3_S0

C1734 1.0UF 10% 6.3V X6S 0402
BYPASS=U1100.P18::6.35mm

PCH VCCVRM BYPASS
(PCH 1.5V VCCVRM PWR)
PP1V5_S0
183mA Max, 68mA Idle
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0

C1740 10UF 20% 16V X6S-CERM 0603
BYPASS=U1100.AF34::12.7mm

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR)
PP1V05_S0
670mA Max, 34mA Idle

C1750 22UF 20% 6.3V X5R-CERM-1 0603
C1751 1.0UF 10% 6.3V X6S 0402
C1752 1.0UF 10% 6.3V X6S 0402
CRITICAL
C1753 12PF 5% NP0-C0G 0201 25V
PLACE_NEAR=U1100.V20:2.54mm
PLACE_NEAR=U1100.V20:2.54mm
PLACE_NEAR=U1100.V20:2.54mm
Not documented in EDS!

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
PP1V05_S0

C1755 10UF 20% 16V X6S-CERM 0603
C1756 1.0UF 10% 6.3V X6S 0402
C1757 1.0UF 10% 6.3V X6S 0402
C1758 1.0UF 10% 6.3V X6S 0402
CRITICAL
C1759 12PF 5% NP0-C0G 0201 25V
BYPASS=U1100.AG18::12.7mm
BYPASS=U1100.AG22::6.35mm
BYPASS=U1100.AD20::6.35mm
BYPASS=U1100.AE18::6.35mm

PCH VCCIO BYPASS
(PCH 1.05V PCIe/DMI/SATA/USB3 PWR)
PP1V05_S0

C1760 10UF 20% 16V X6S-CERM 0603
C1761 1.0UF 10% 6.3V X6S 0402
C1762 1.0UF 10% 6.3V X6S 0402
C1763 1.0UF 10% 6.3V X6S 0402
C1764 1.0UF 10% 6.3V X6S 0402
CRITICAL
C1765 12PF 5% NP0-C0G 0201 25V
BYPASS=U1100.AK18::12.7mm
BYPASS=U1100.AK22::6.35mm
BYPASS=U1100.AK20::6.35mm
BYPASS=U1100.AM18::6.35mm

PCH VCCUSBPLL BYPASS
(PCH 1.05V USB2 PLL PWR)
PP1V05_S0

C1770 1.0UF 10% 6.3V X6S 0402
BYPASS=U1100.U35::6.35mm

PCH VCCIO BYPASS
(PCH 1.05V FDI PWR)
PP1V05_S0

C1772 1.0UF 10% 6.3V X6S 0402
BYPASS=U1100.AN34::6.35mm

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR)
PP1V05_S0

C1774 0.1UF 10% 25V X7R-CERM 0402
CRITICAL
C1775 12PF 5% NP0-C0G 0201 25V
BYPASS=U1100.U30::6.35mm

PCH V_PROC_IO BYPASS
(PCH 1.05V CPU I/F PWR)
PP1V05_S0

C1785 1.0UF 10% 6.3V X6S 0402
C1786 0.1UF 10% 25V X7R-CERM 0402
C1787 0.1UF 10% 25V X7R-CERM 0402
BYPASS=U1100.AJ12::12.7mm
BYPASS=U1100.AJ12::6.35mm
BYPASS=U1100.AJ12::6.35mm

PP1V05_S0
??mA Max, ??mA Idle

R1790 1 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCC_CLK_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

CRITICAL
OMIT_TABLE
L1790 4.7UH-170MA-0.321OHM 0603

PCH CLK VCC BYPASS
(PCH 1.05V CLK PLL PWR)
PP1V05_S0_PCH_VCC_CLK_F
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V

NO STUFF
C1790 10UF 20% 16V X6S-CERM 0603
C1791 1UF 10% 16V X6S-CERM 0402
BYPASS=U1100.AP45::12.7mm
BYPASS=U1100.AP45::6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V SSC100 PWR)
PP1V05_S0

C1776 1.0UF 10% 6.3V X6S 0402
C1777 1.0UF 10% 6.3V X6S 0402
BYPASS=U1100.AE30::6.35mm
BYPASS=U1100.AG30::6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK PWR)
PP1V05_S0

C1778 1.0UF 10% 6.3V X6S 0402
BYPASS=U1100.AD35::6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK135 PWR)
PP1V05_S0

C1780 1.0UF 10% 6.3V X6S 0402
BYPASS=U1100.AD34::6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V SSC PWR)
PP1V05_S0

C1782 1.0UF 10% 6.3V X6S 0402
BYPASS=U1100.AA30::6.35mm

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	1	RES,FF,0 OHM,(020OHM MAX),2A,0603	L1790		

Current data from LPT EDS (doc #486708, Rev 1.0).

SYNC_MASTER=CLEAN_X425 SYNC_DATE=10/30/2014

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PCH DECOUPLING

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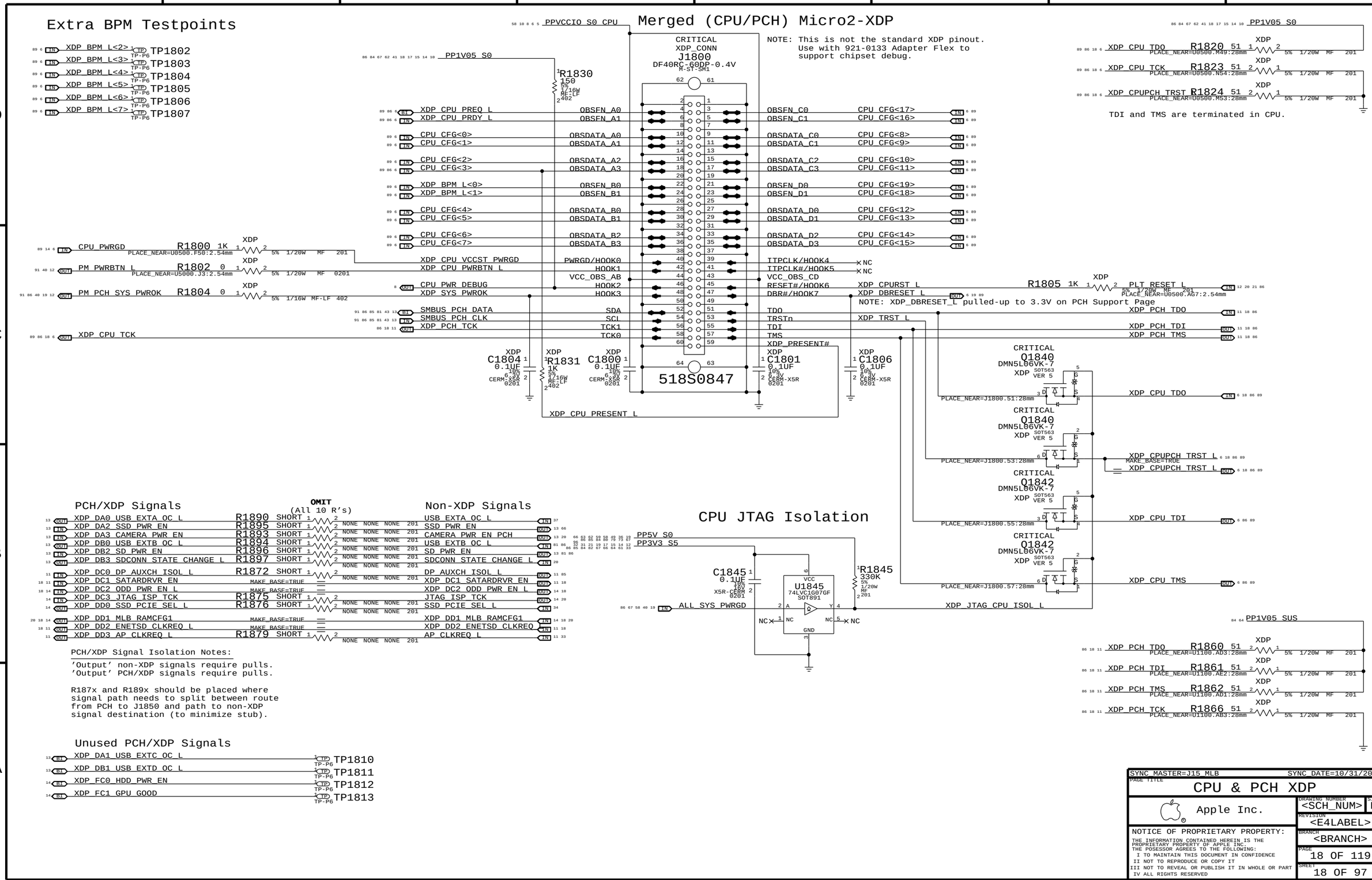
Extra BPM Testpoints
XDP_BPM_L<2> TP1802
XDP_BPM_L<3> TP1803
XDP_BPM_L<4> TP1804
XDP_BPM_L<5> TP1805
XDP_BPM_L<6> TP1806
XDP_BPM_L<7> TP1807
Merged (CPU/PCH) Micro2-XDP
NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.
CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM1
518S0847
PPVCCIO_S0_CPU
PP1V05_S0
R1830 150 5% 1/16W MF-LF 402
XDP_CPU_PREQ_L
XDP_CPU_PRDY_L
CPU_CFG<0>
CPU_CFG<1>
CPU_CFG<2>
CPU_CFG<3>
XDP_BPM_L<0>
XDP_BPM_L<1>
CPU_CFG<4>
CPU_CFG<5>
CPU_CFG<6>
CPU_CFG<7>
XDP_CPU_VCCST_PWRGD
XDP_CPU_PWRBTN_L
CPU_PWR_DEBUG
XDP_SYS_PWROK
SMBUS_PCH_DATA
SMBUS_PCH_CLK
XDP_PCH_TCK
OBSFN_A0
OBSFN_A1
OBSDATA_A0
OBSDATA_A1
OBSDATA_A2
OBSDATA_A3
OBSFN_B0
OBSFN_B1
OBSDATA_B0
OBSDATA_B1
OBSDATA_B2
OBSDATA_B3
PWRGD/HOOK0
HOOK1
VCC_OBS_AB
HOOK2
HOOK3
SDA
SCL
TCK1
TCK0
OBSFN_C0
OBSFN_C1
OBSDATA_C0
OBSDATA_C1
OBSDATA_C2
OBSDATA_C3
OBSFN_D0
OBSFN_D1
OBSDATA_D0
OBSDATA_D1
OBSDATA_D2
OBSDATA_D3
TTPCLK/HOOK4
TTPCLK#/HOOK5
VCC_OBS_CD
RESET#/HOOK6
DBR#/HOOK7
TDO
TRSTn
TDI
TMS
XDP_PRESENT#
CPU_CFG<17>
CPU_CFG<16>
CPU_CFG<8>
CPU_CFG<9>
CPU_CFG<10>
CPU_CFG<11>
CPU_CFG<19>
CPU_CFG<18>
CPU_CFG<12>
CPU_CFG<13>
CPU_CFG<14>
CPU_CFG<15>
NC
XDP_CPURST_L
XDP_DBRESET_L
XDP_TRST_L
XDP_CPU_PRESENT_L
C1804 0.1UF 10% 10V CERM-X5R 0201
R1831 1K 5% 1/16W MF-LF 402
C1800 0.1UF 10% 10V CERM-X5R 0201
C1801 0.1UF 10% 10V CERM-X5R 0201
C1806 0.1UF 10% 10V CERM-X5R 0201
XDP_CPU_TDO R1820 51 5% 1/20W MF 201
XDP_CPU_TCK R1823 51 5% 1/20W MF 201
XDP_CPUPCH_TRST R1824 51 5% 1/20W MF 201
PLACE_NEAR=U0500.M49:28mm
PLACE_NEAR=U0500.N54:28mm
PLACE_NEAR=U0500.M53:28mm
TDI and TMS are terminated in CPU.
CPU_PWRGD R1800 1K 5% 1/20W MF 201
PM_PWRBTN_L R1802 0 5% 1/20W MF 0201
PM_PCH_SYS_PWROK R1804 0 5% 1/16W MF-LF 402
PLACE_NEAR=U0500.F50:2.54mm
PLACE_NEAR=U5000.J3:2.54mm
R1805 1K 5% 1/20W MF 201
PLT_RESET_L
PLACE_NEAR=U0500.A67:2.54mm
NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page
XDP_PCH_TDO
XDP_PCH_TDI
XDP_PCH_TMS
XDP_CPU_TCK
CRITICAL
Q1840 DMN5L06VK-7 SOT563 VER 5
PLACE_NEAR=J1800.51:28mm
PLACE_NEAR=J1800.53:28mm
XDP_CPUPCH_TRST_L
MAKE_BASE=TRUE
Q1842 DMN5L06VK-7 SOT563 VER 5
PLACE_NEAR=J1800.55:28mm
PLACE_NEAR=J1800.57:28mm
XDP_CPU_TDI
XDP_CPU_TMS
PCH/XDP Signals
OMIT
(All 10 R's)
Non-XDP Signals
XDP_DA0_USB_EXTA_OC_L R1890 SHORT
XDP_DA2_SSD_PWR_EN R1895 SHORT
XDP_DA3_CAMERA_PWR_EN R1893 SHORT
XDP_DB0_USB_EXTB_OC_L R1894 SHORT
XDP_DB2_SD_PWR_EN R1896 SHORT
XDP_DB3_SDCONN_STATE_CHANGE_L R1897 SHORT
XDP_DC0_DP_AUXCH_ISOL_L R1872 SHORT
XDP_DC1_SATARDRVR_EN
XDP_DC2_ODD_PWR_EN_L
XDP_DC3_JTAG_ISP_TCK R1875 SHORT
XDP_DD0_SSD_PCIE_SEL_L R1876 SHORT
XDP_DD1_MLB_RAMCFG1
XDP_DD2_ENETSD_CLKREQ_L
XDP_DD3_AP_CLKREQ_L R1879 SHORT
USB_EXTA_OC_L
SSD_PWR_EN
CAMERA_PWR_EN_PCH
USB_EXTB_OC_L
SD_PWR_EN
SDCONN_STATE_CHANGE_L
DP_AUXCH_ISOL_L
XDP_DC1_SATARDRVR_EN
XDP_DC2_ODD_PWR_EN_L
JTAG_ISP_TCK
SSD_PCIE_SEL_L
XDP_DD1_MLB_RAMCFG1
XDP_DD2_ENETSD_CLKREQ
AP_CLKREQ_L
PCH/XDP Signal Isolation Notes:
'Output' non-XDP signals require pulls.
'Output' PCH/XDP signals require pulls.
R187x and R189x should be placed where
signal path needs to split between route
from PCH to J1850 and path to non-XDP
signal destination (to minimize stub).
CPU JTAG Isolation
PP5V_S0
PP3V3_S5
C1845 0.1UF 10% 16V X5R-CERM 0201
U1845 74LVC1G07GF SOT891
VCC
GND
R1845 330K 5% 1/20W MF 201
ALL_SYS_PWRGD
XDP_JTAG_CPU_ISOL_L
PP1V05_SUS
XDP_PCH_TDO R1860 51 5% 1/20W MF 201
XDP_PCH_TDI R1861 51 5% 1/20W MF 201
XDP_PCH_TMS R1862 51 5% 1/20W MF 201
XDP_PCH_TCK R1866 51 5% 1/20W MF 201
PLACE_NEAR=U1100.AD3:28mm
PLACE_NEAR=U1100.AE2:28mm
PLACE_NEAR=U1100.AD1:28mm
PLACE_NEAR=U1100.AB3:28mm
Unused PCH/XDP Signals
XDP_DA1_USB_EXTC_OC_L TP1810
XDP_DB1_USB_EXTD_OC_L TP1811
XDP_FC0_HDD_PWR_EN TP1812
XDP_FC1_GPU_GOOD TP1813
SYNC_MASTER=J15_MLB
SYNC_DATE=10/31/2012
PAGE TITLE
CPU & PCH XDP
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
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REVISION
<E4LABEL>
BRANCH
<BRANCH>
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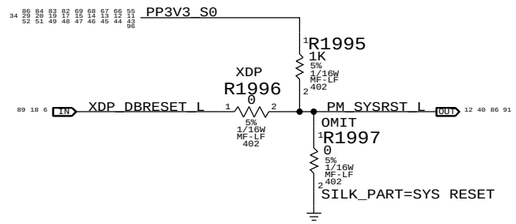
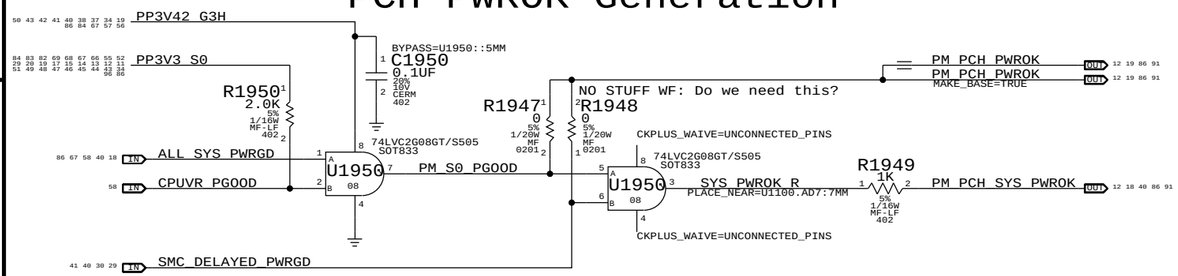
PCH Reset Button

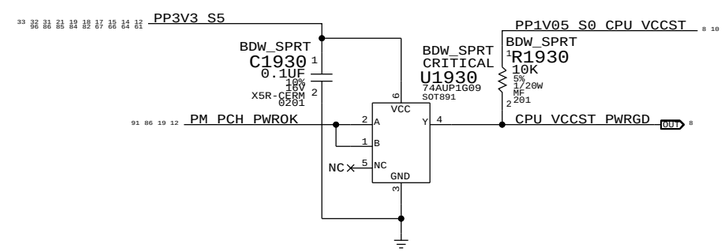


PCH PWROK Generation

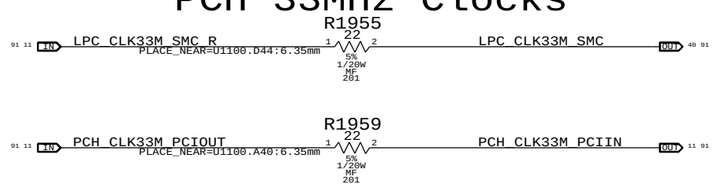


NOTE: ALL_SYS_PWRGD must remain low until at least 5ms after all rails are valid.

VCCST (1.05V S0) PWRGD



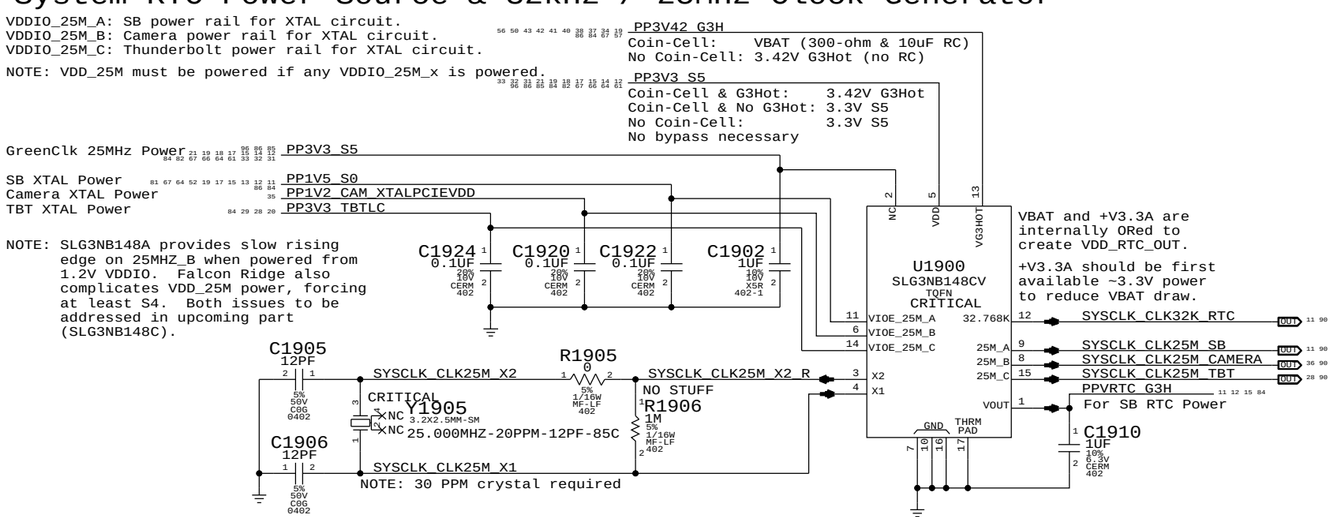
PCH 33MHz Clocks



System RTC Power Source & 32kHz / 25MHz Clock Generator

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Camera power rail for XTAL circuit.
VDDIO_25M_C: Thunderbolt power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.



VBAT and +V3.3A are internally ORed to create VDD_RTC_OUT.

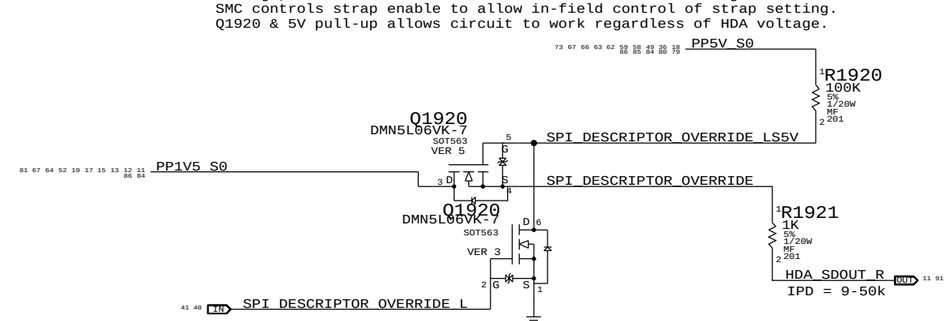
+V3.A should be first available ~3.3V power to reduce VBAT draw.

NOTE: SLG3NB148A provides slow rising edge on 25MHZ_B when powered from 1.2V VDDIO. Falcon Ridge also complicates VDD_25M power, forcing at least S4. Both issues to be addressed in upcoming part (SLG3NB148C).

NOTE: 30 PPM crystal required

PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.



SYNC MASTER=CLEAN X425 SYNC DATE=10/31/2014

PAGE TITLE
Chipset Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
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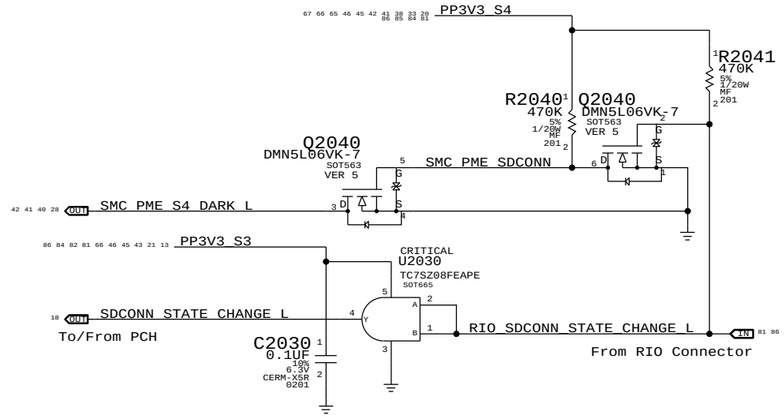
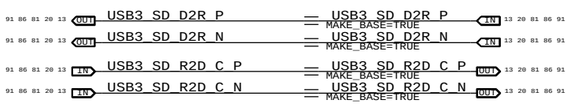
RIO SD Card Reader Support



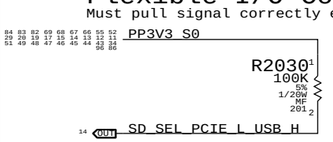
Flexible I/O Aliases

SD Card Reader is always USB3 in this implementaton.



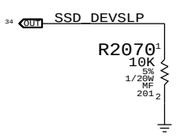
Flexible I/O Configuration Strap

Must pull signal correctly even if always USB or PCIe

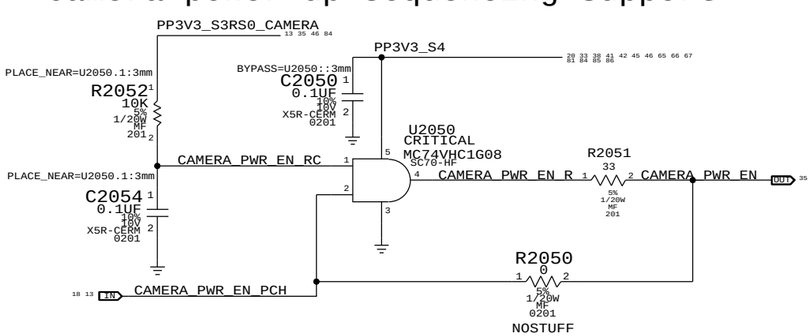


GS3 Connector Support

DEVSLP not supported on LPT-H

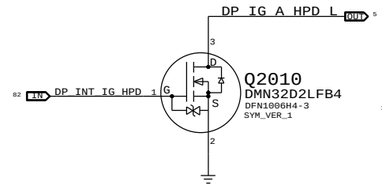


Camera power-up sequencing Support

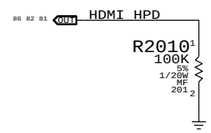


LCD HPD Inverter

(Pull-Up on CPU Page)

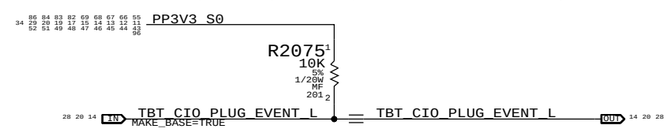


HDMI HPD pull-down



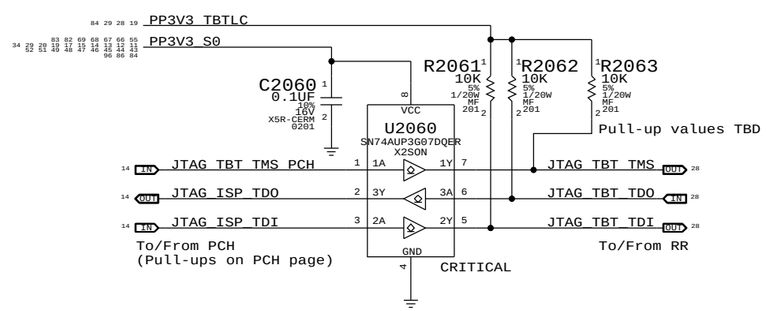
Falcon Ridge Support

RR output is open-drain, no isolation necessary



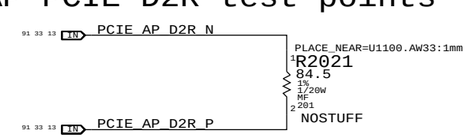
Falcon Ridge JTAG Isolation

TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH
U2060 supports I/O's powered when VCC=0V

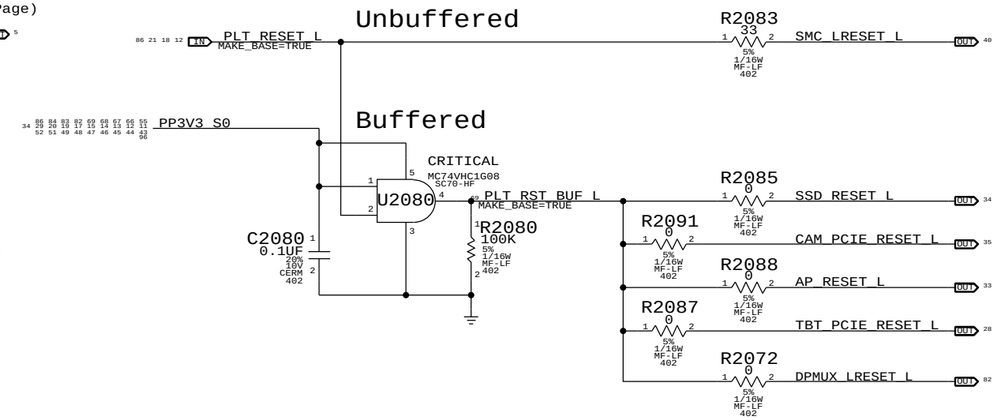


PCH 33MHz Clock for DPMUX

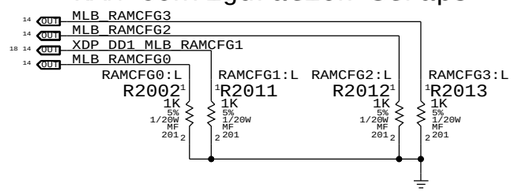
AP PCIE D2R test points



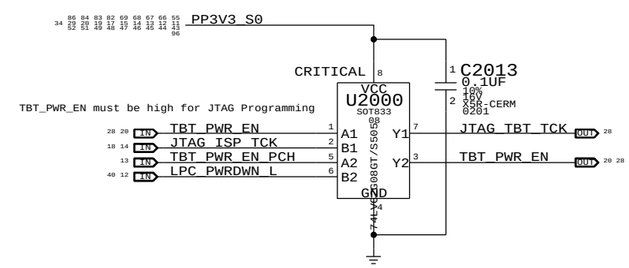
Platform Reset Connections



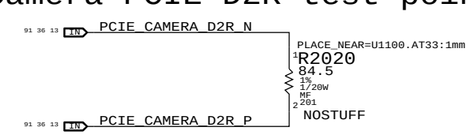
RAM Configuration Straps



GPIO Glitch Prevention



Camera PCIE D2R test points



SYNC_MASTER=J15_REFERENCE SYNC_DATE=01/14/2013

PAGE TITLE

Project Chipset Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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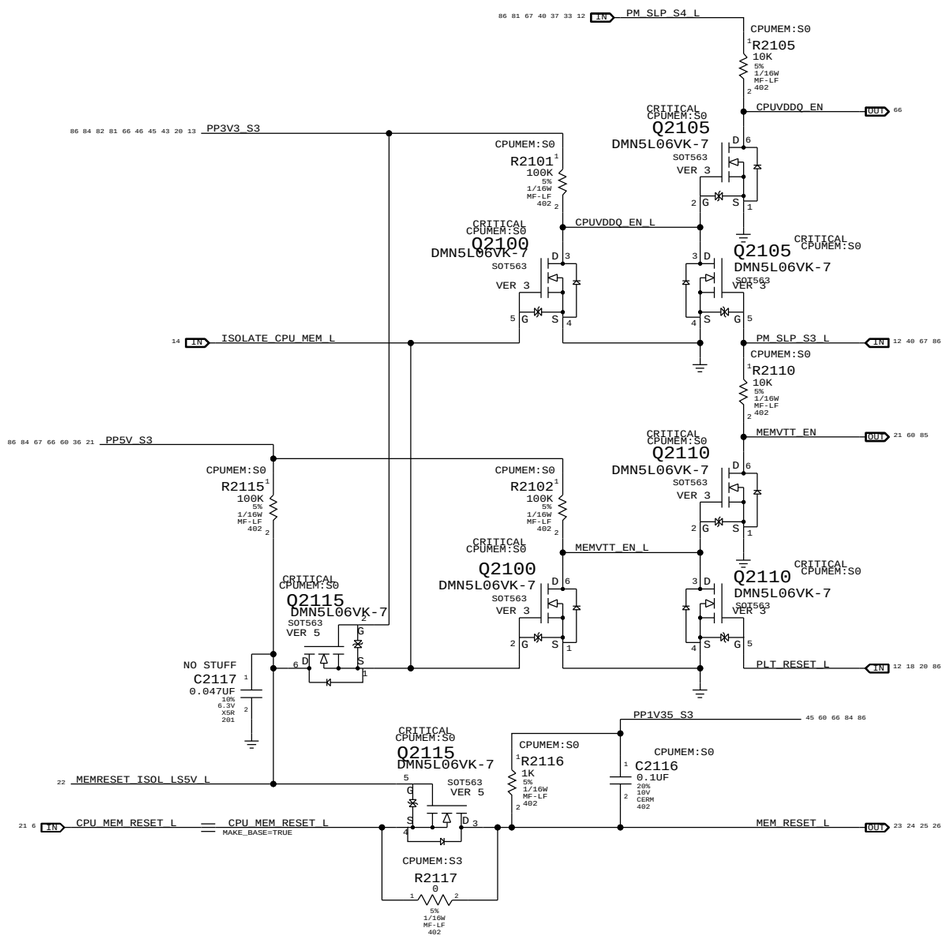
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

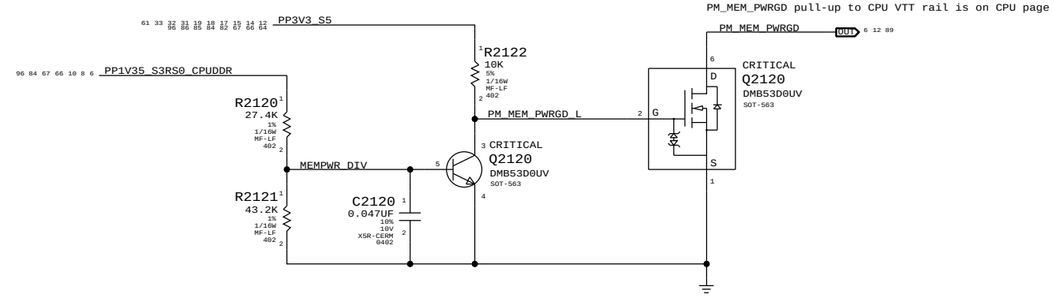
ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

CPUVDDQ_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L



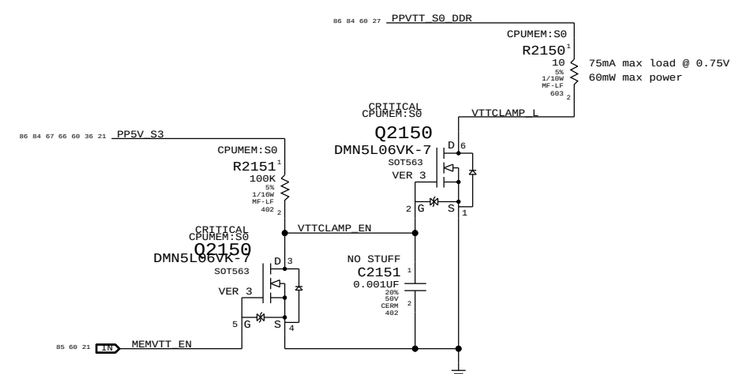
MEM S0 "PGOOD" for CPU

PM_MEM_PWRGD pull-up to CPU VTT rail is on CPU page



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	CPUVDDQ_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
	1	0	1	1	1	1	1	1	1
to	2	0	0	1	1	1	1	0	1
S3	3	0	0	0	1	X	1	0	0
	4	0	0	1	1	X	1	0	1
to	5	0	1	1	1	0 (*)	1	1	1
	6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC MASTER=CLEAN_MAXWELL SYNC DATE=07/02/2014

PAGE TITLE
CPU Memory S3 Support

Apple Inc.

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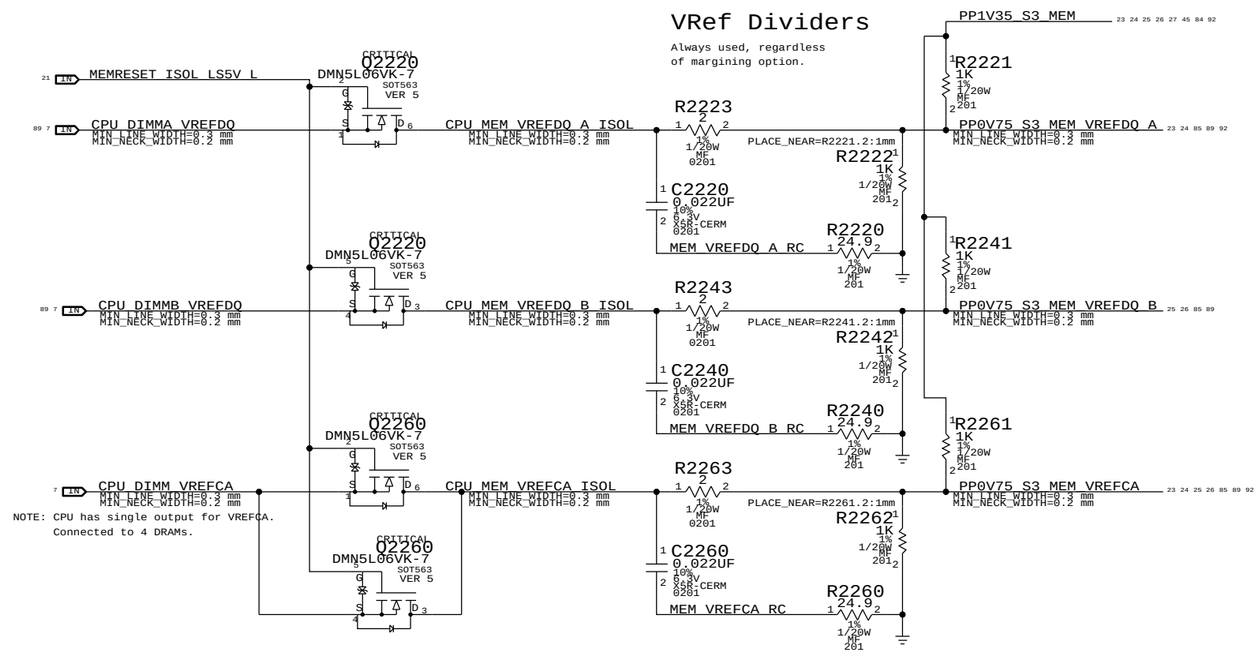
CPU-Based Margining

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step
LPDDR3 (1.2V) ?.??mV per step



SYNC MASTER=CLEAN X425 SYNC DATE=08/11/2014

PAGE TITLE
DDR3 VREF MARGINING

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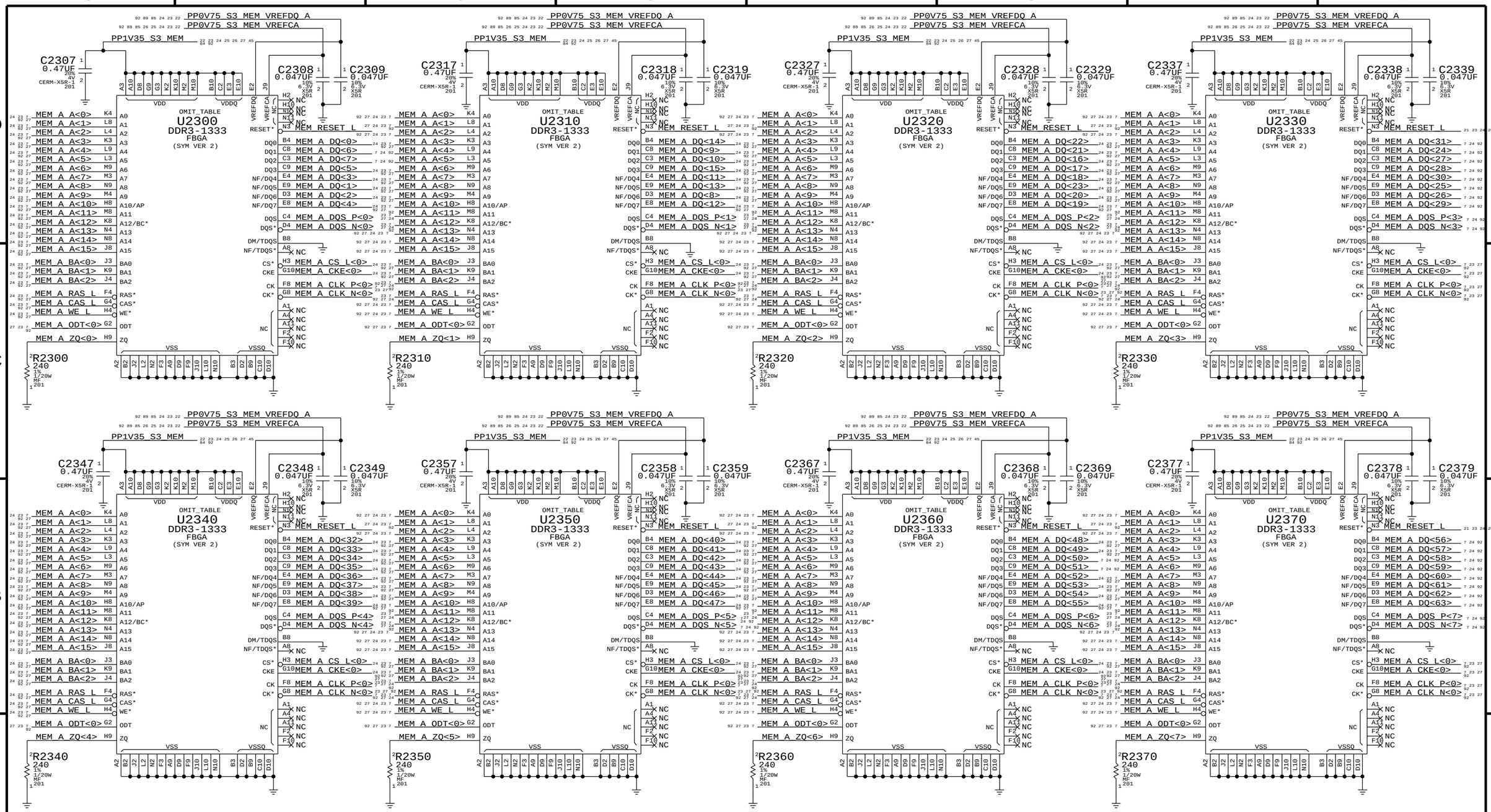
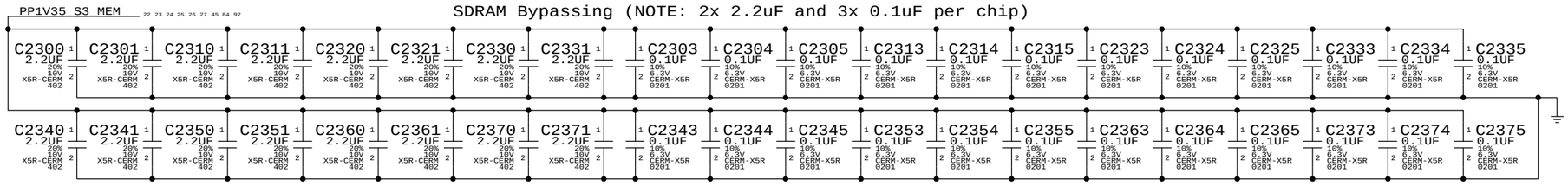


SDRAM Bypassing (NOTE: 2x 2.2uF and 3x 0.1uF per chip)



SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE
DDR3 SDRAM Bank A (1 OF 2)

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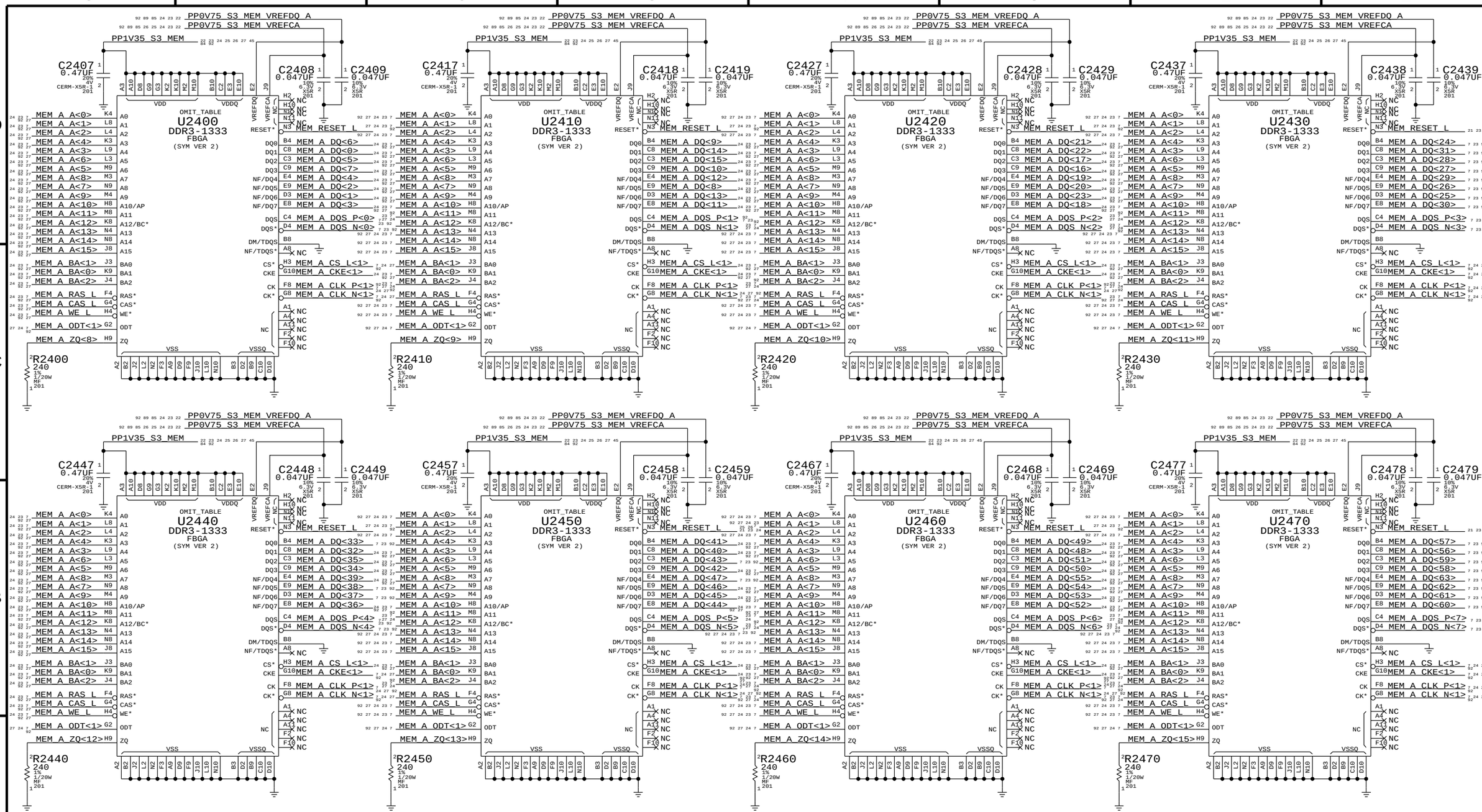

SYNC MASTER=J15 MLB SYNC DATE=10/31/2012

PAGE TITLE
DDR3 SDRAM Bank A (2 OF 2)

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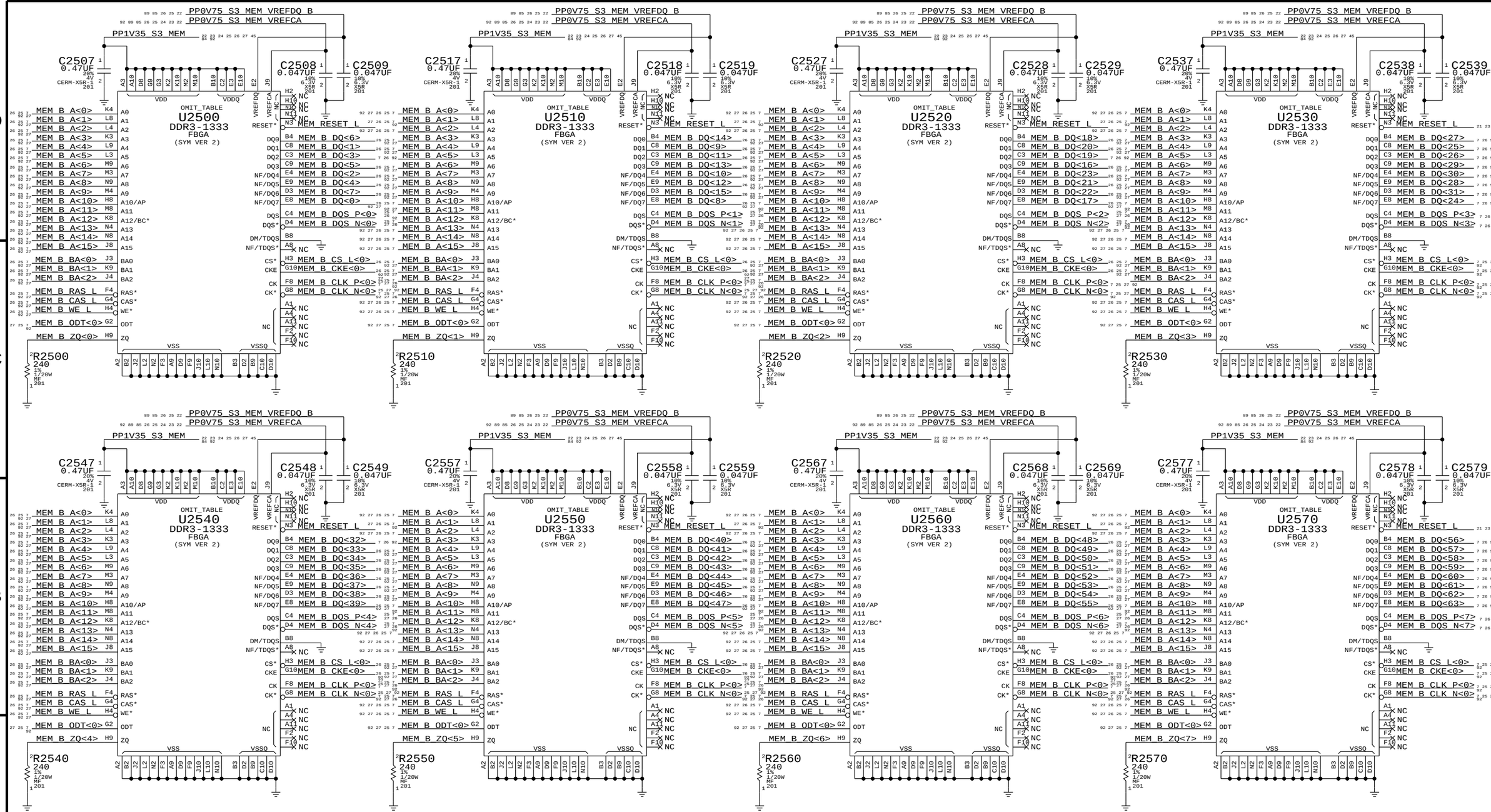
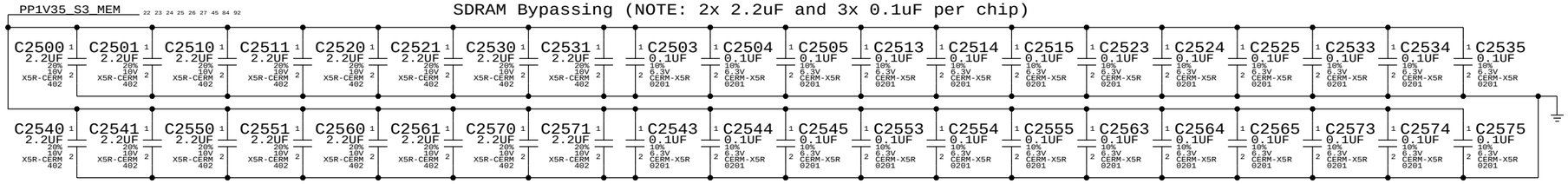


SDRAM Bypassing (NOTE: 2x 2.2uF and 3x 0.1uF per chip)



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PAGE TITLE
DDR3 SDRAM Bank B (1 OF 2)

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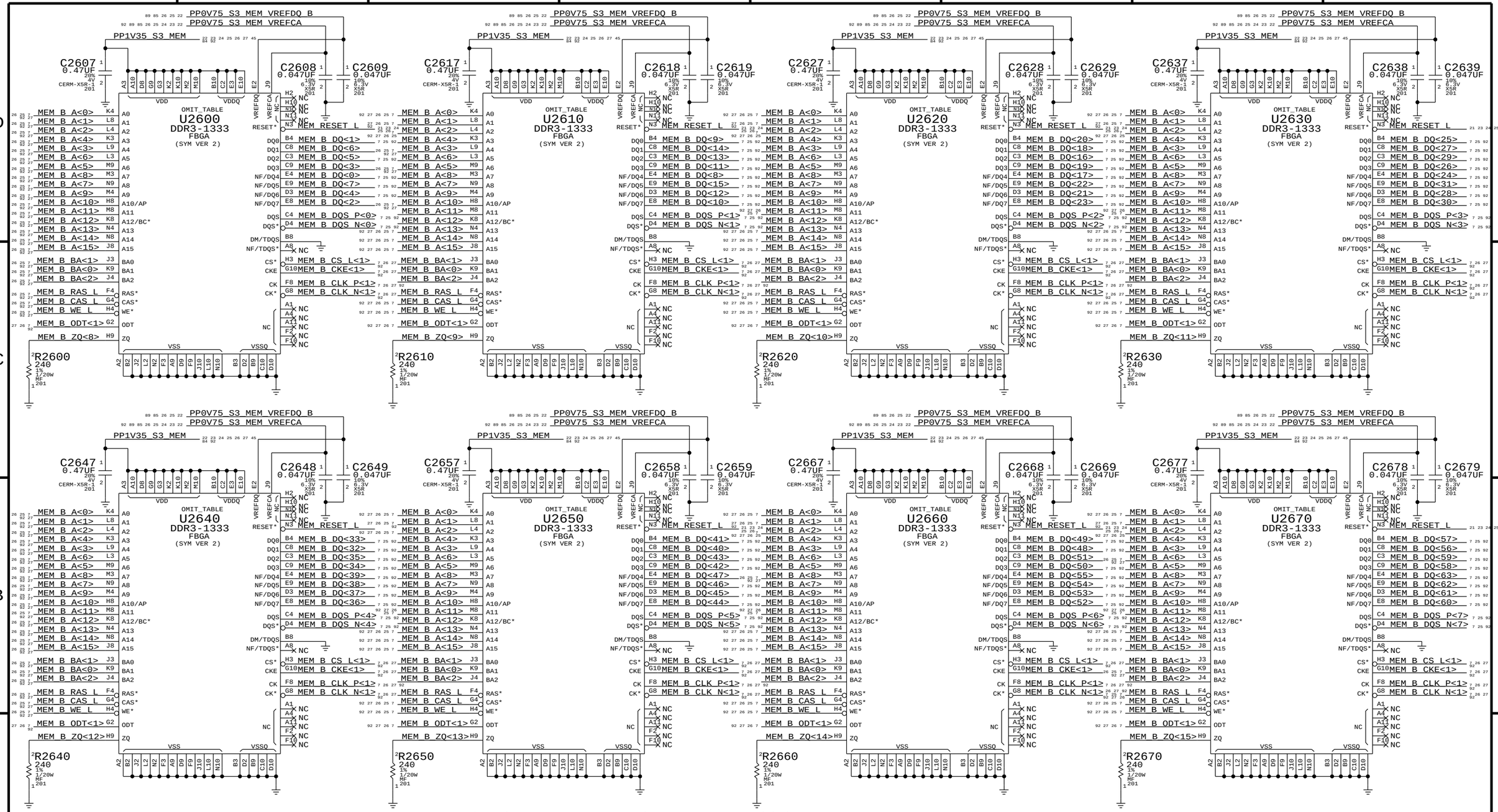

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DDR3 SDRAM Bank B (2 OF 2)

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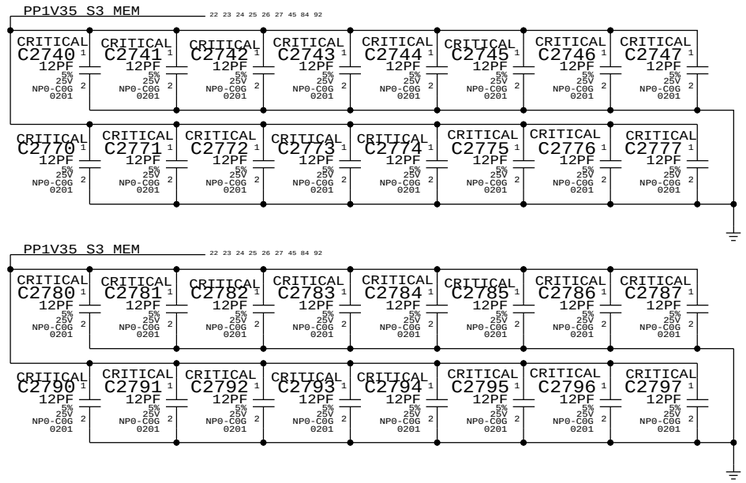
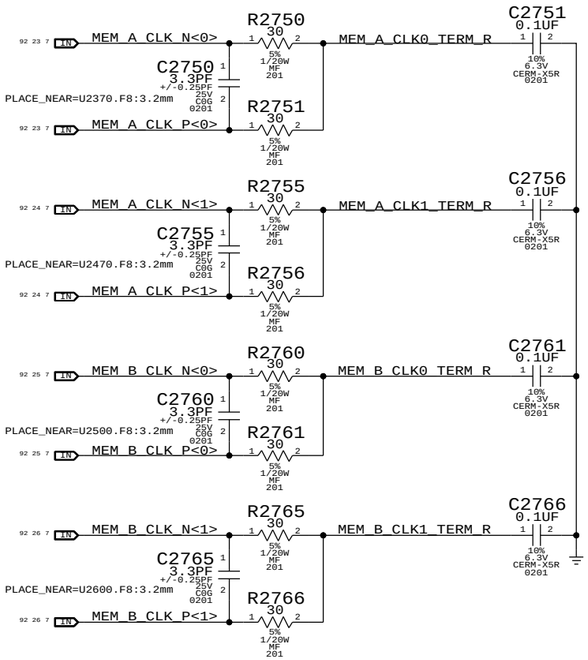
FOR DESENSE IMPROVEMENT
PLACE ONE AT EACH DDR3L MEMORY MODULE.



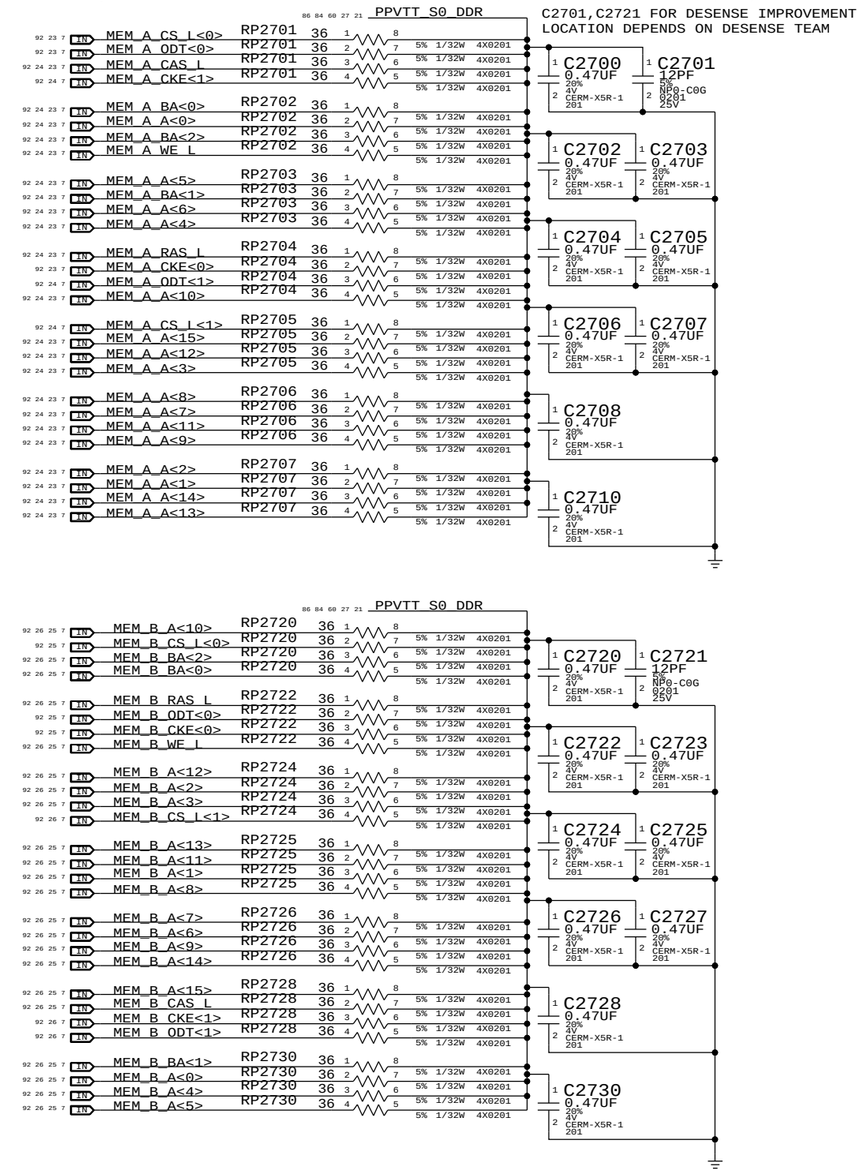
MEM Clock Termination

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



JEDEC 4.20.18 Unbuffered SODIMM Raw Card F spec recommends 36 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE

C2701,C2721 FOR DESENSE IMPROVEMENT
LOCATION DEPENDS ON DESENSE TEAM



SYNC_MASTER=CLEAN_X425 SYNC_DATE=10/30/2014

PAGE TITLE
DDR3 Termination

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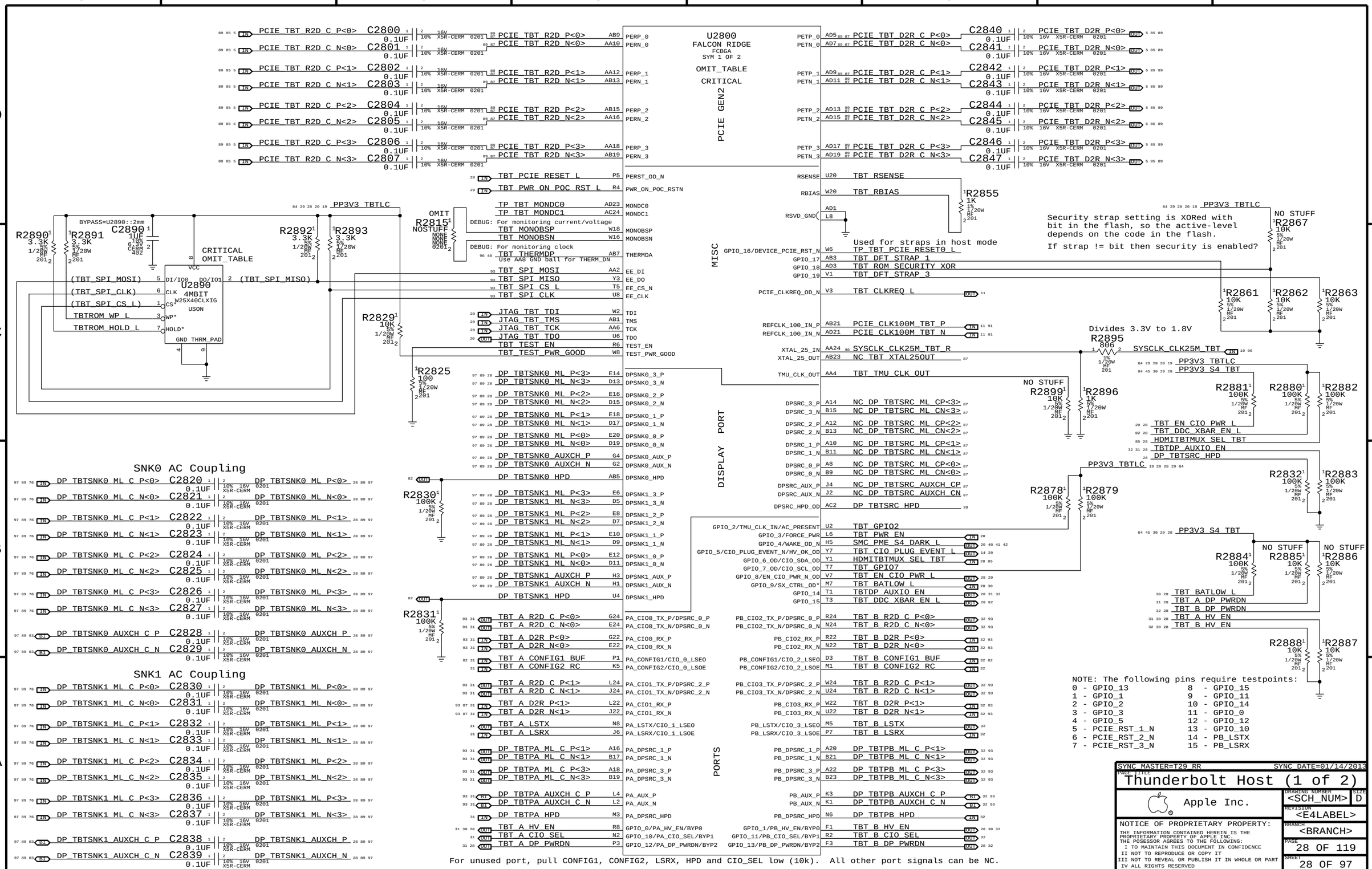
U2800
FALCON RIDGE
FCBGA
SYM 1 OF 2
OMIT_TABLE
CRITICAL
PCIE GEN2
MISC
DISPLAY PORT
PORTS
PCIE_TBT_R2D_C_P<0> C2800 0.1UF
PCIE_TBT_R2D_C_N<0> C2801 0.1UF
PCIE_TBT_R2D_C_P<1> C2802 0.1UF
PCIE_TBT_R2D_C_N<1> C2803 0.1UF
PCIE_TBT_R2D_C_P<2> C2804 0.1UF
PCIE_TBT_R2D_C_N<2> C2805 0.1UF
PCIE_TBT_R2D_C_P<3> C2806 0.1UF
PCIE_TBT_R2D_C_N<3> C2807 0.1UF
PCIE_TBT_R2D_P<0> PCIE_TBT_R2D_N<0> PCIE_TBT_R2D_P<1> PCIE_TBT_R2D_N<1> PCIE_TBT_R2D_P<2> PCIE_TBT_R2D_N<2> PCIE_TBT_R2D_P<3> PCIE_TBT_R2D_N<3>
PCIE_TBT_D2R_C_P<0> C2840 0.1UF
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PCIE_TBT_D2R_C_P<1> C2842 0.1UF
PCIE_TBT_D2R_C_N<1> C2843 0.1UF
PCIE_TBT_D2R_C_P<2> C2844 0.1UF
PCIE_TBT_D2R_C_N<2> C2845 0.1UF
PCIE_TBT_D2R_C_P<3> C2846 0.1UF
PCIE_TBT_D2R_C_N<3> C2847 0.1UF
TBT_PCIE_RESET_L
TBT_PWR_ON_POC_RST_L
TBT_RSENSE
TBT_RBIAS
R2855 1K
PP3V3_TBTLC
BYPASS=U2890::2mm
R2890 3.3K
R2891 3.3K
C2890 1UF
R2892 3.3K
R2893 3.3K
CRITICAL
OMIT_TABLE
U2890
4MBIT
W25X40CLXIG
USON
(TBT_SPI_MOSI)
(TBT_SPI_CLK)
(TBT_SPI_CS_L)
TBTROM_WP_L
TBTROM_HOLD_L
(TBT_SPI_MISO)
OMIT
R2815 NOSTUFF
DEBUG: For monitoring current/voltage
TBT_MONOBSP
TBT_MONOBSN
DEBUG: For monitoring clock
TBT_THERMDP
Use AA8 GND ball for THERM_DN
TBT_SPI_MOSI
TBT_SPI_MISO
TBT_SPI_CS_L
TBT_SPI_CLK
R2829 10K
JTAG_TBT_TDI
JTAG_TBT_TMS
JTAG_TBT_TCK
JTAG_TBT_TDO
TBT_TEST_EN
TBT_TEST_PWR_GOOD
R2825 100
Used for straps in host mode
TP_TBT_PCIE_RESET0_L
TBT_DFT_STRAP_1
TBT_ROM_SECURITY_XOR
TBT_DFT_STRAP_3
TBT_CLKREQ_L
PCIE_CLK100M_TBT_P
PCIE_CLK100M_TBT_N
SYSCLK_CLK25M_TBT_R
NC_TBT_XTAL25OUT
TBT_TMU_CLK_OUT
Security strap setting is XORed with bit in the flash, so the active-level depends on the code in the flash.
If strap != bit then security is enabled?
NO STUFF
R2867 10K
R2861 10K
R2862 10K
R2863 10K
Divides 3.3V to 1.8V
R2895 806
SYSCLK_CLK25M_TBT
PP3V3_TBTLC
PP3V3_S4_TBT
NO STUFF
R2899 10K
R2896 1K
R2881 100K
R2880 100K
R2882 100K
TBT_EN_CIO_PWR_L
TBT_DDC_XBAR_EN_L
HDMITBTMUX_SEL_TBT
TBTDP_AUXIO_EN
DP_TBTSRC_HPD
R2832 100K
R2883 100K
R2878 100K
R2879 100K
R2884 100K
NO STUFF
R2885 10K
NO STUFF
R2886 10K
TBT_BATLOW_L
TBT_A_DP_PWRDN
TBT_B_DP_PWRDN
TBT_A_HV_EN
TBT_B_HV_EN
R2888 10K
R2887 10K
SNK0 AC Coupling
DP_TBTSNK0_ML_C_P<0> C2820 0.1UF
DP_TBTSNK0_ML_C_N<0> C2821 0.1UF
DP_TBTSNK0_ML_C_P<1> C2822 0.1UF
DP_TBTSNK0_ML_C_N<1> C2823 0.1UF
DP_TBTSNK0_ML_C_P<2> C2824 0.1UF
DP_TBTSNK0_ML_C_N<2> C2825 0.1UF
DP_TBTSNK0_ML_C_P<3> C2826 0.1UF
DP_TBTSNK0_ML_C_N<3> C2827 0.1UF
DP_TBTSNK0_AUXCH_C_P C2828 0.1UF
DP_TBTSNK0_AUXCH_C_N C2829 0.1UF
SNK1 AC Coupling
DP_TBTSNK1_ML_C_P<0> C2830 0.1UF
DP_TBTSNK1_ML_C_N<0> C2831 0.1UF
DP_TBTSNK1_ML_C_P<1> C2832 0.1UF
DP_TBTSNK1_ML_C_N<1> C2833 0.1UF
DP_TBTSNK1_ML_C_P<2> C2834 0.1UF
DP_TBTSNK1_ML_C_N<2> C2835 0.1UF
DP_TBTSNK1_ML_C_P<3> C2836 0.1UF
DP_TBTSNK1_ML_C_N<3> C2837 0.1UF
DP_TBTSNK1_AUXCH_C_P C2838 0.1UF
DP_TBTSNK1_AUXCH_C_N C2839 0.1UF
R2830 100K
R2831 100K
NOTE: The following pins require testpoints:
0 - GPIO_13
1 - GPIO_1
2 - GPIO_2
3 - GPIO_3
4 - GPIO_5
5 - PCIE_RST_1_N
6 - PCIE_RST_2_N
7 - PCIE_RST_3_N
8 - GPIO_15
9 - GPIO_11
10 - GPIO_14
11 - GPIO_0
12 - GPIO_12
13 - GPIO_10
14 - PB_LSTX
15 - PB_LSRX
For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.
SYNC_MASTER=T29_RR
SYNC_DATE=01/14/2013
PAGE TITLE
Thunderbolt Host (1 of 2)
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
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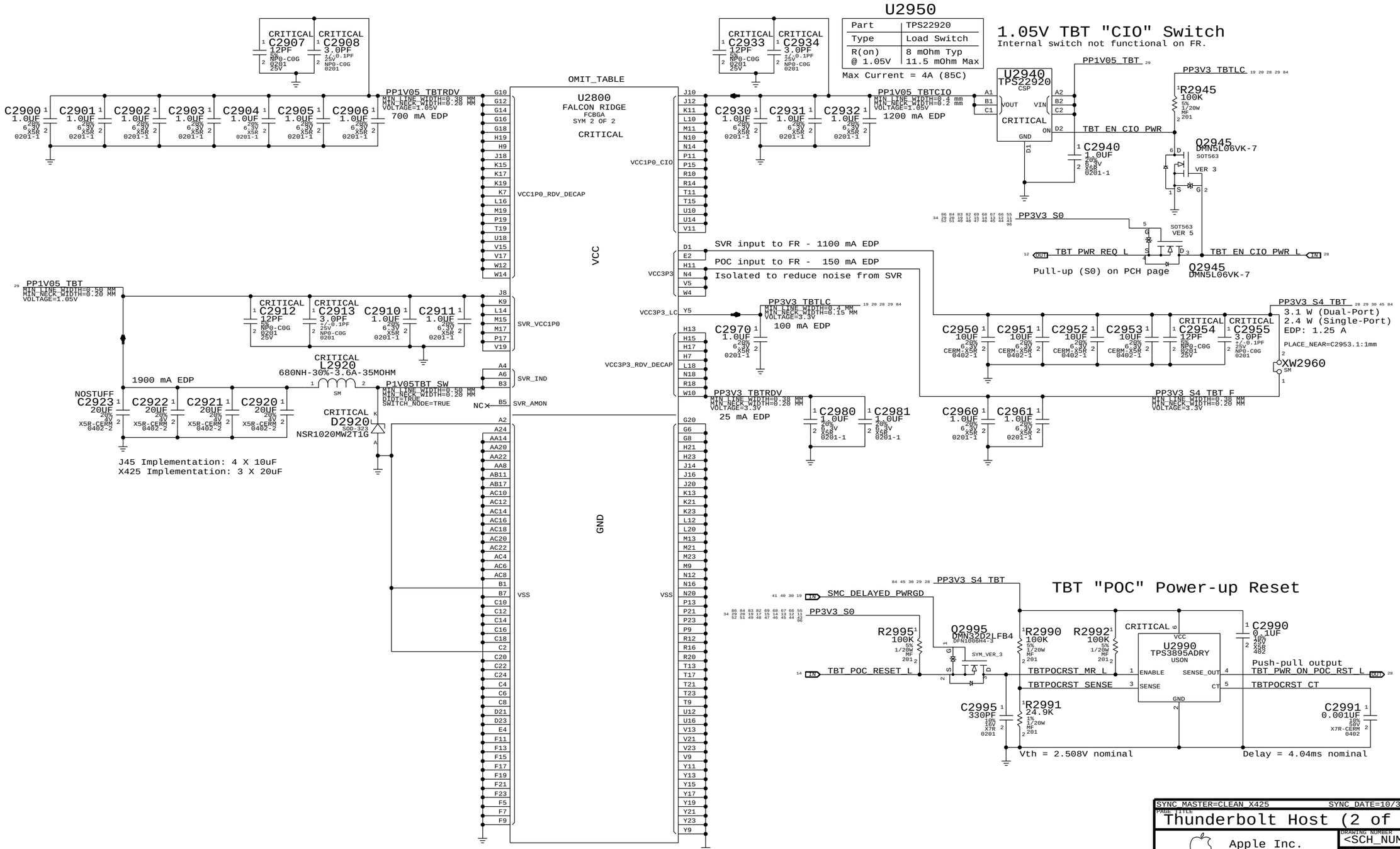

EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).

SYNC_MASTER=CLEAN_X425 SYNC_DATE=10/30/2014

PAGE TITLE: Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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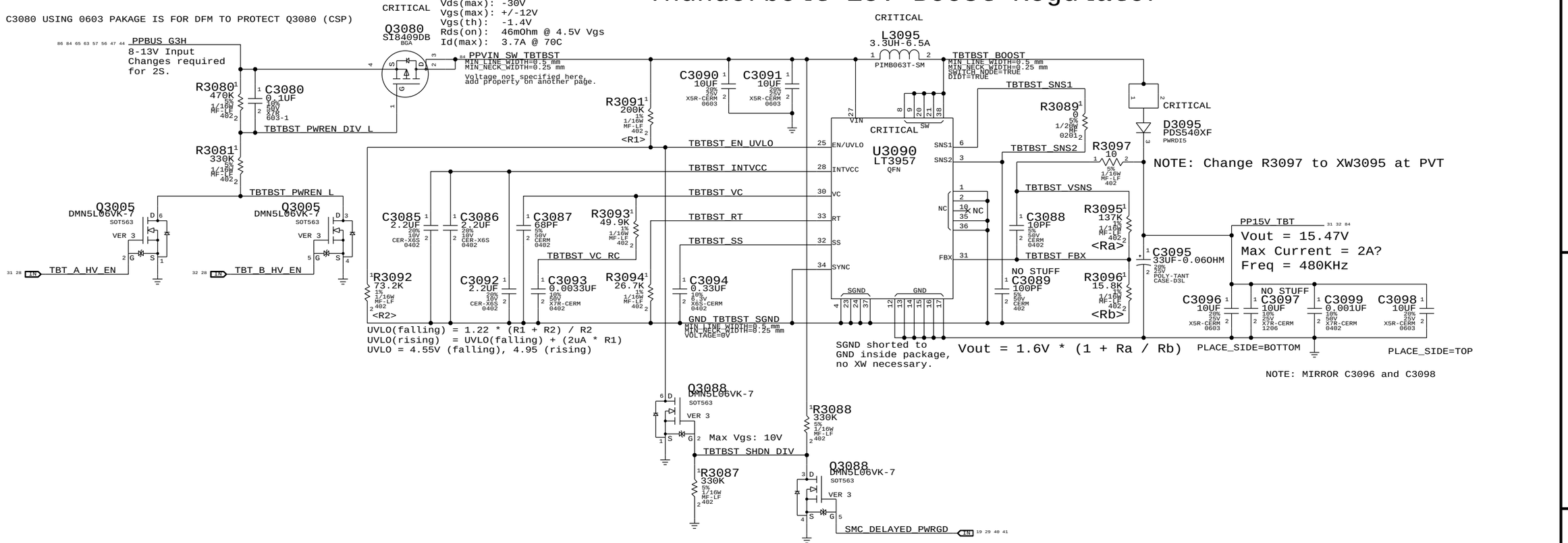
Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)

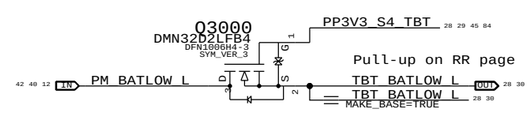
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Thunderbolt 15V Boost Regulator



BATLOW# Isolation



SYNC_MASTER=CLEAN_X305 SYNC_DATE=06/24/2014

PAGE TITLE: Thunderbolt Mobile Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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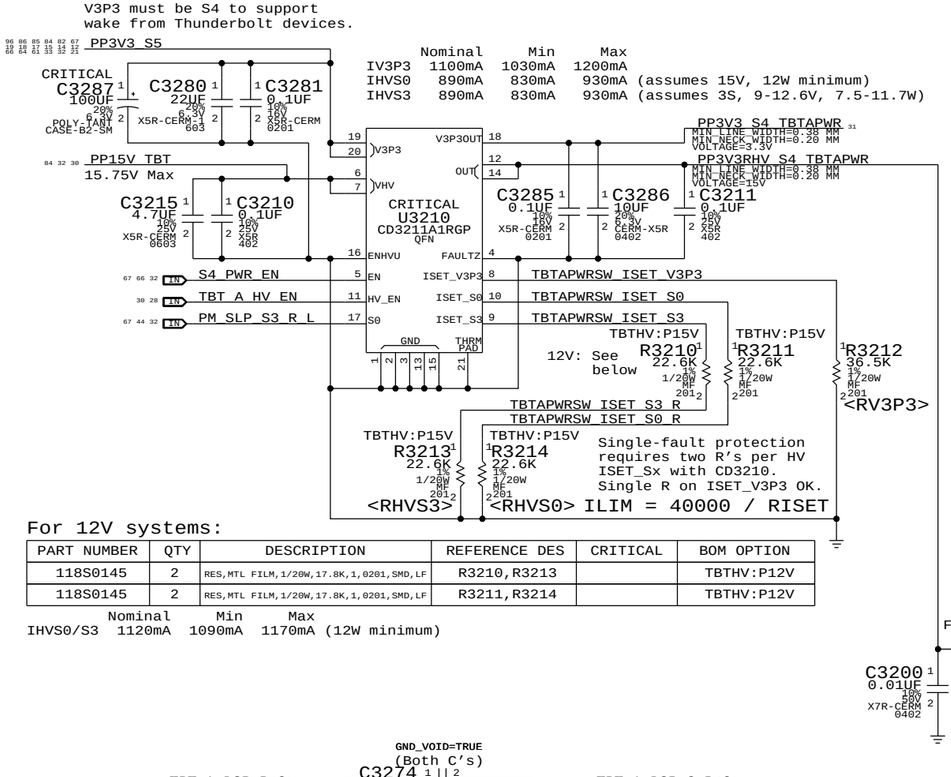
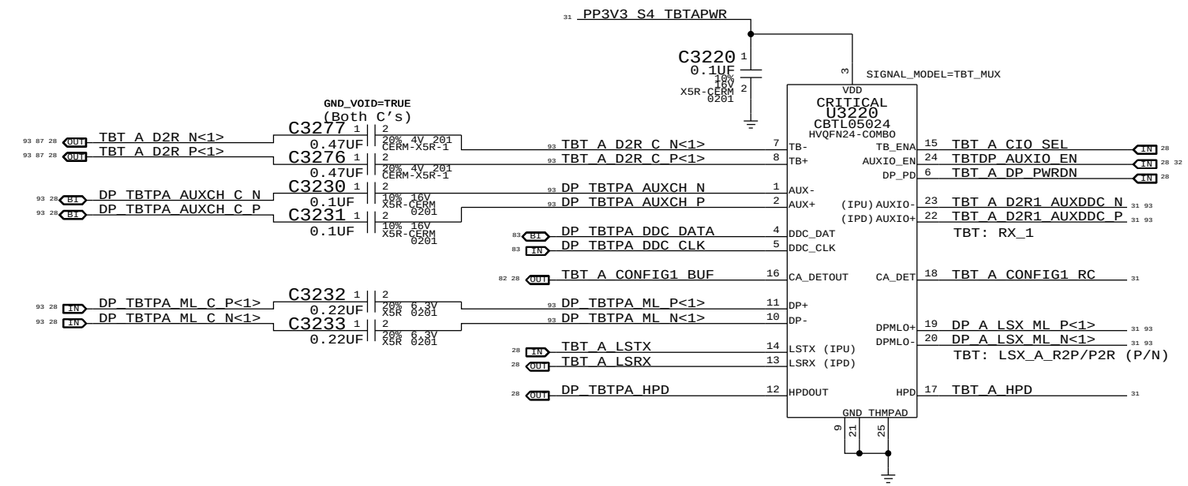
3.3V/HV Power MUX



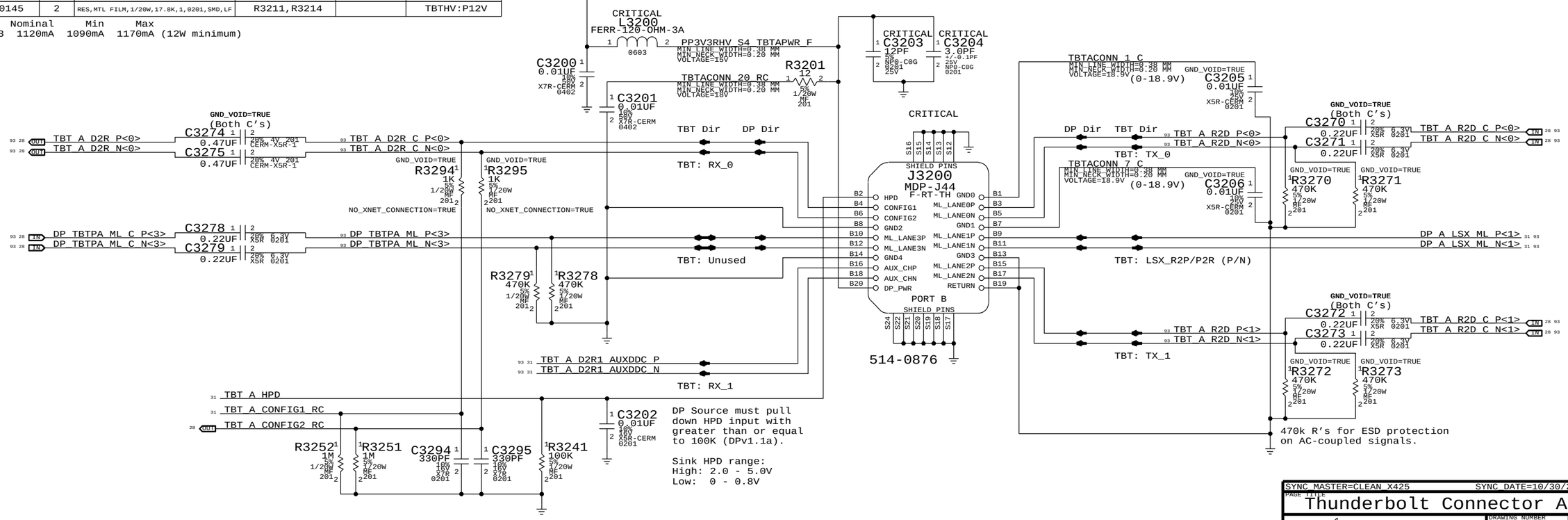
For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

Nominal Min Max
IHVS0/S3 1120mA 1090mA 1170mA (12W minimum)



Thunderbolt Connector A



SYNC_MASTER=CLEAN_X425 SYNC_DATE=10/30/2014

PAGE TITLE: Thunderbolt Connector A

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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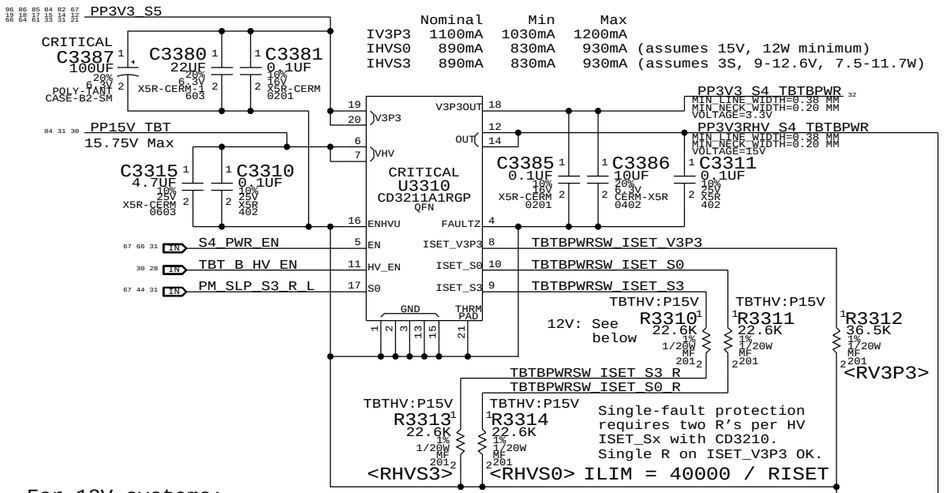
3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)

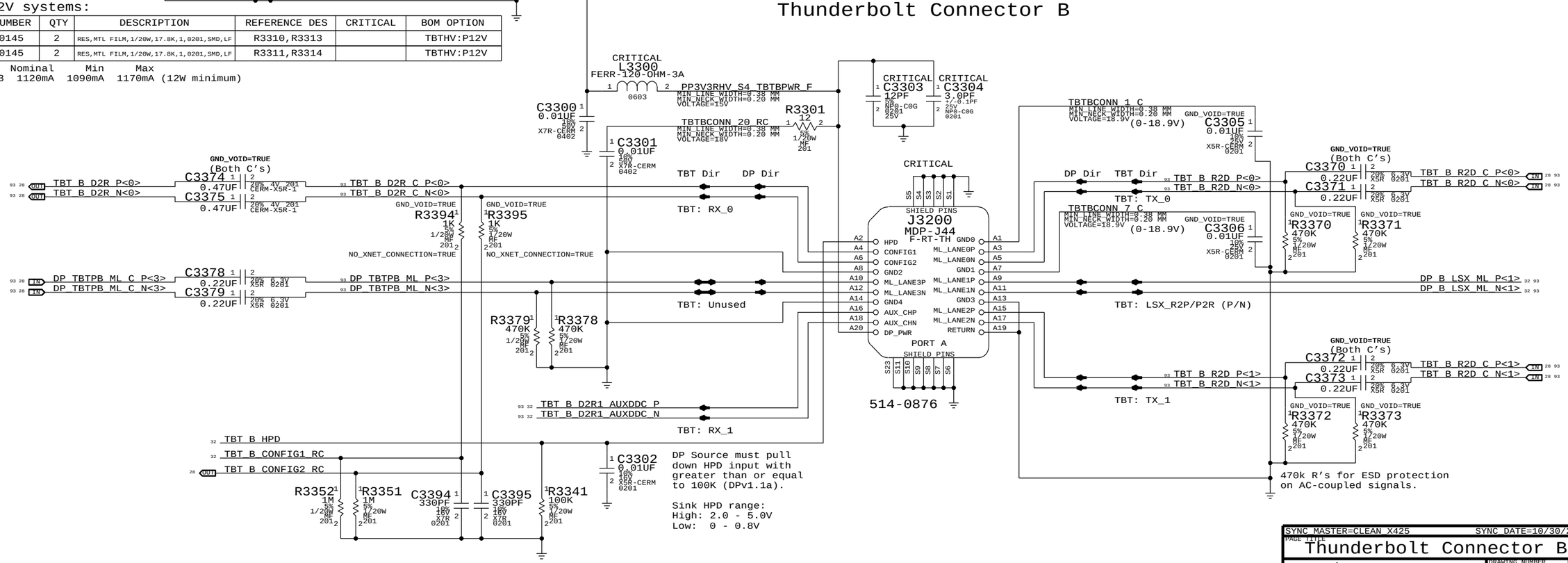


For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3310,R3313		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3311,R3314		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

Thunderbolt Connector B



SYNC_MASTER=CLEAN_X425 SYNC_DATE=10/30/2014

PAGE TITLE: Thunderbolt Connector B

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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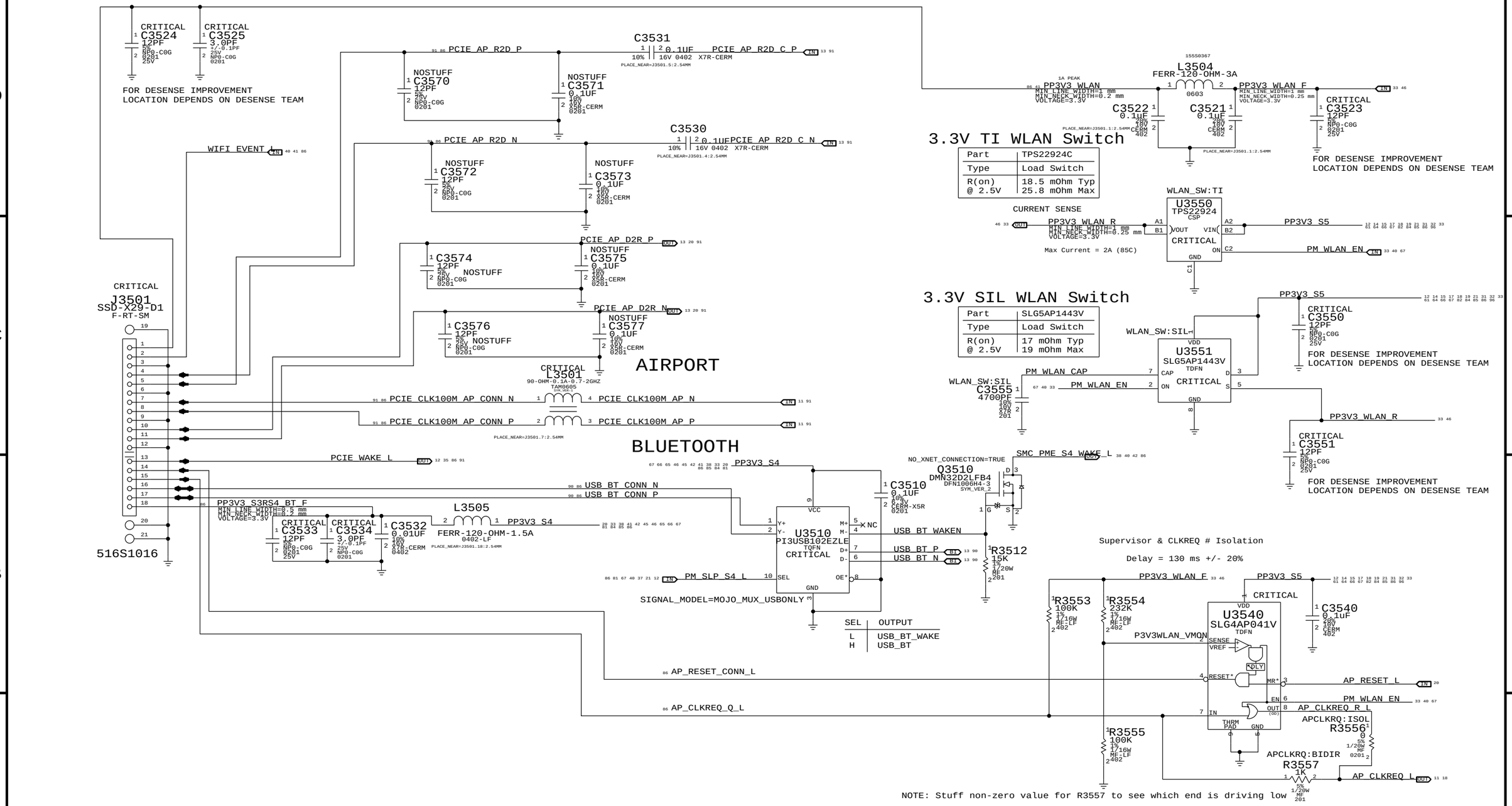

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X87 CONNECTOR

Apple Inc.

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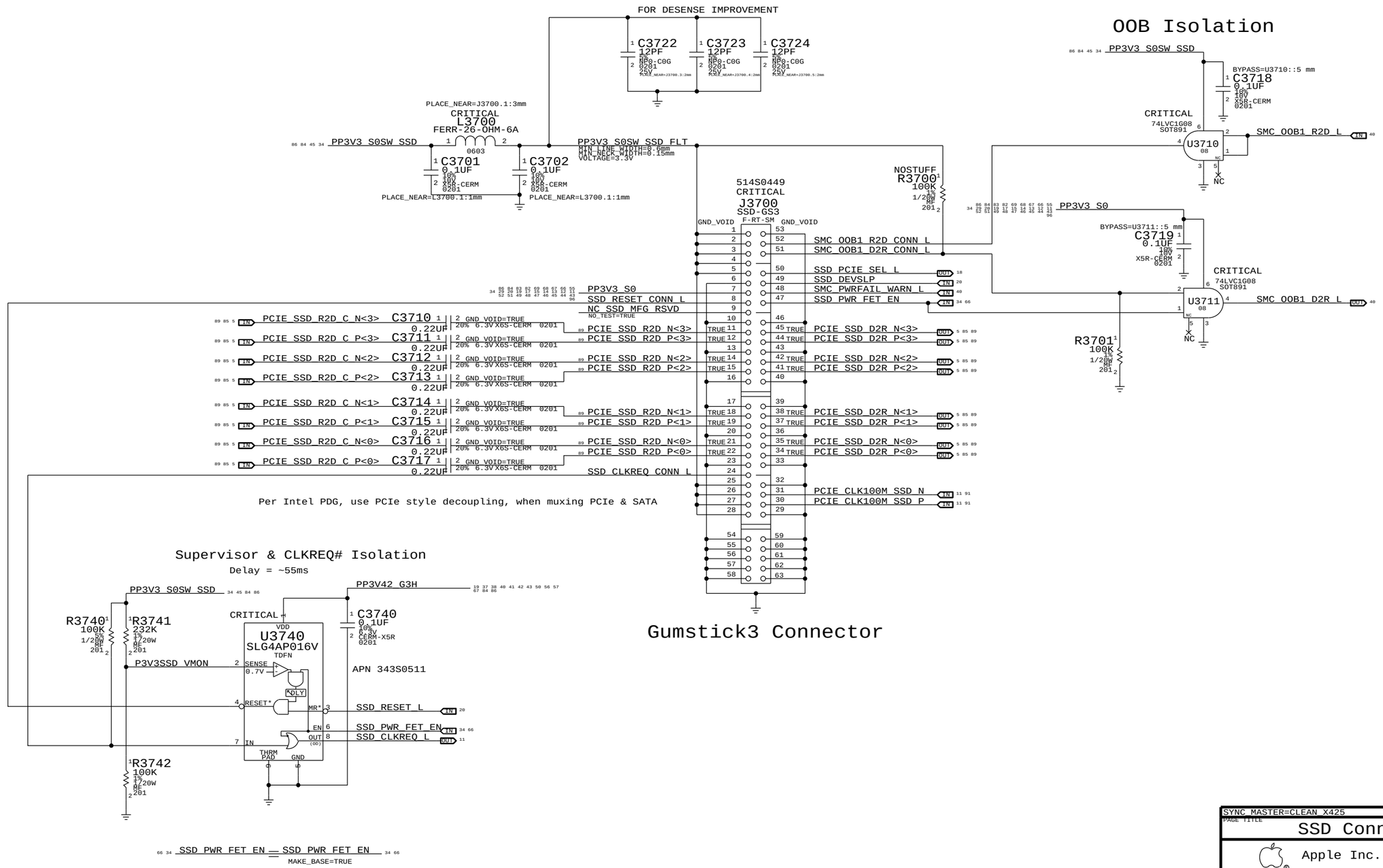

SYNC_MASTER=CLEAN_X425 SYNC_DATE=08/15/2014

PAGE TITLE

SSD Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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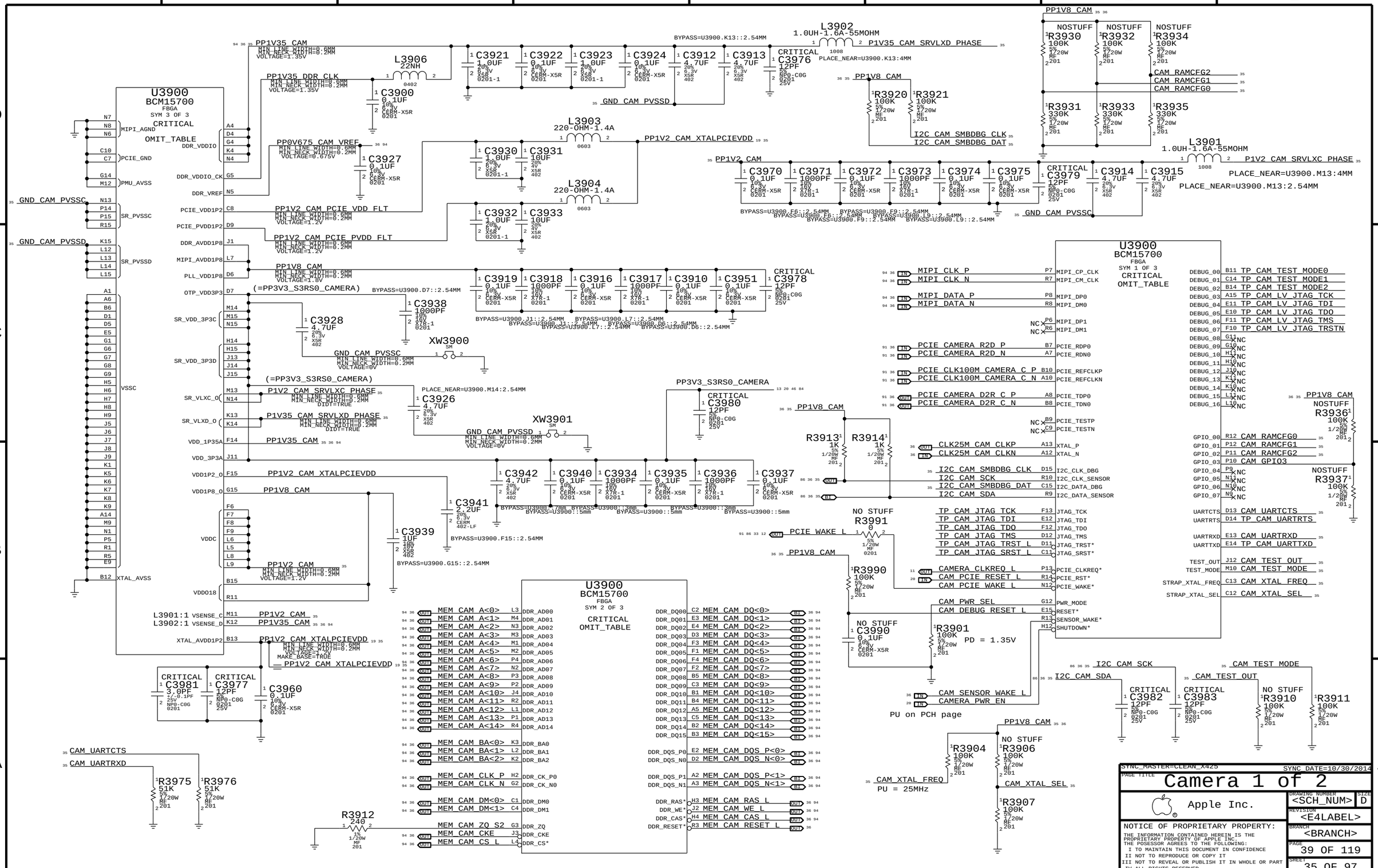
U3900
BCM15700
FBGA
SYM 3 OF 3
CRITICAL
OMIT_TABLE
U3900
BCM15700
FBGA
SYM 1 OF 3
CRITICAL
OMIT_TABLE
U3900
BCM15700
FBGA
SYM 2 OF 3
CRITICAL
OMIT_TABLE
PP1V35 CAM
PP1V35 DDR CLK
PP0V675 CAM VREF
PP1V2 CAM PCIE VDD FLT
PP1V2 CAM PCIE PVDD FLT
PP1V8 CAM
(=PP3V3_S3RS0_CAMERA)
P1V2 CAM SRVLXC PHASE
P1V35 CAM SRVLXD PHASE
PP1V2 CAM XTALPCIEVDD
GND CAM PVSSD
GND CAM PVSSC
PP3V3_S3RS0_CAMERA
L3902
1.0UH-1.6A-55MOHM
L3901
1.0UH-1.6A-55MOHM
L3906
22NH
L3903
220-OHM-1.4A
L3904
220-OHM-1.4A
XW3900
XW3901
R3930 100K
R3932 100K
R3934 100K
R3931 330K
R3933 330K
R3935 330K
R3920 100K
R3921 100K
I2C CAM SMBDBG CLK
I2C CAM SMBDBG DAT
MIPI CLK P
MIPI CLK N
MIPI DATA P
MIPI DATA N
PCIE CAMERA R2D P
PCIE CAMERA R2D N
PCIE CLK100M CAMERA C P
PCIE CLK100M CAMERA C N
PCIE CAMERA D2R C P
PCIE CAMERA D2R C N
CLK25M CAM CLKP
CLK25M CAM CLKN
I2C CAM SCK
I2C CAM SDA
TP CAM JTAG TCK
TP CAM JTAG TDI
TP CAM JTAG TDO
TP CAM JTAG TMS
TP CAM JTAG TRST L
TP CAM JTAG SRST L
CAMERA CLKREQ L
CAM PCIE RESET L
CAM PCIE WAKE L
CAM PWR SEL
CAM DEBUG RESET L
CAM SENSOR WAKE L
CAMERA PWR EN
PCIE WAKE L
R3913 1K
R3914 1K
R3991 0
R3990 100K
R3901 100K
PD = 1.35V
PU on PCH page
R3904 100K
R3906 100K
R3907 100K
CAM XTAL FREQ
PU = 25MHz
CAM XTAL SEL
R3936 100K
R3937 100K
R3910 100K
R3911 100K
R3975 51K
R3976 51K
R3912 240
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MEM CAM DQS N<1>
MEM CAM RAS L
MEM CAM WE L
MEM CAM CAS L
MEM CAM RESET L
TP CAM TEST MODE0
TP CAM TEST MODE1
TP CAM TEST MODE2
TP CAM LV JTAG TCK
TP CAM LV JTAG TDI
TP CAM LV JTAG TDO
TP CAM LV JTAG TMS
TP CAM LV JTAG TRSTN
CAM RAMCFG0
CAM RAMCFG1
CAM RAMCFG2
CAM GPIO3
CAM UARTCTS
TP CAM UARTRTS
CAM UARTRXD
TP CAM UARTTXD
CAM TEST OUT
CAM TEST MODE
CAM XTAL FREQ
CAM XTAL SEL
CAM UARTCTS
CAM UARTRXD
CAM TEST MODE
CAM TEST OUT
I2C CAM SCK
I2C CAM SDA
SYNC_MASTER=CLEAN_X425
SYNC DATE=10/30/2014
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Camera 1 of 2
Apple Inc.
DRAWING NUMBER
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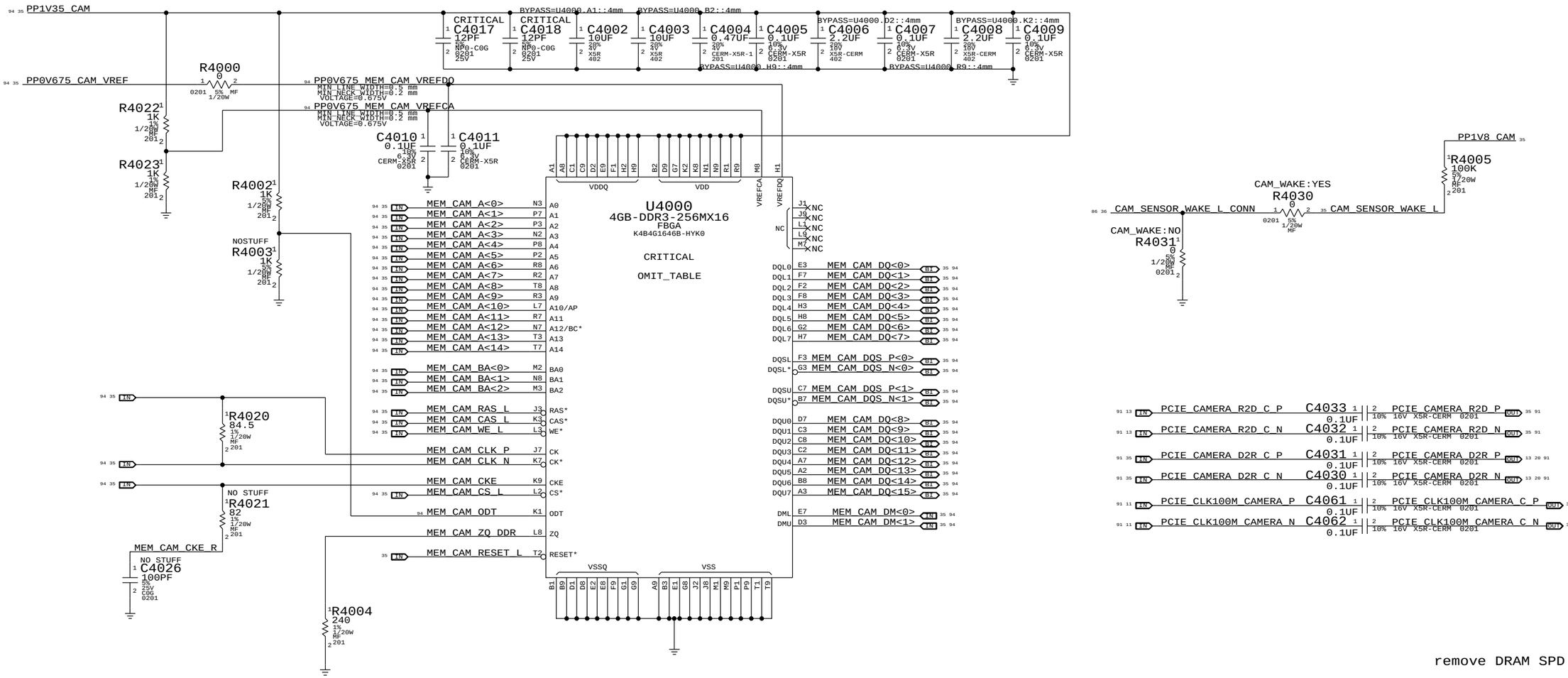


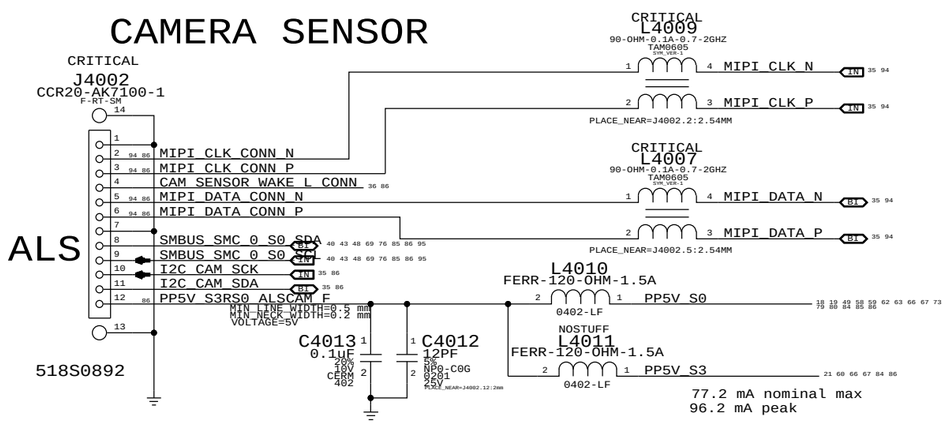
remove DRAM SPD Straps

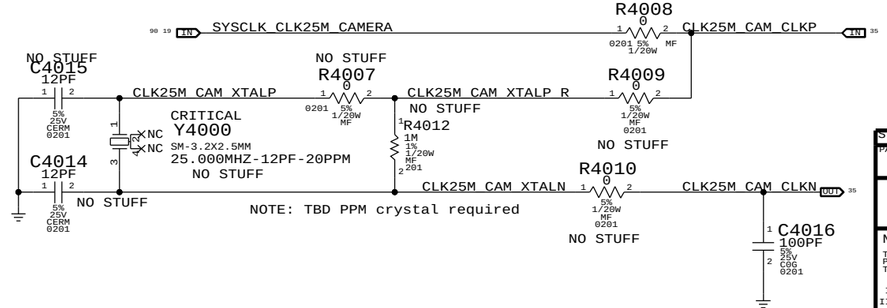
DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

DIE REV	CFG 2
A	0
B	1

CAMERA SENSOR





SYNC_MASTER=CLEAN_X425 SYNC_DATE=10/30/2014

PAGE TITLE: Camera 2 of 2

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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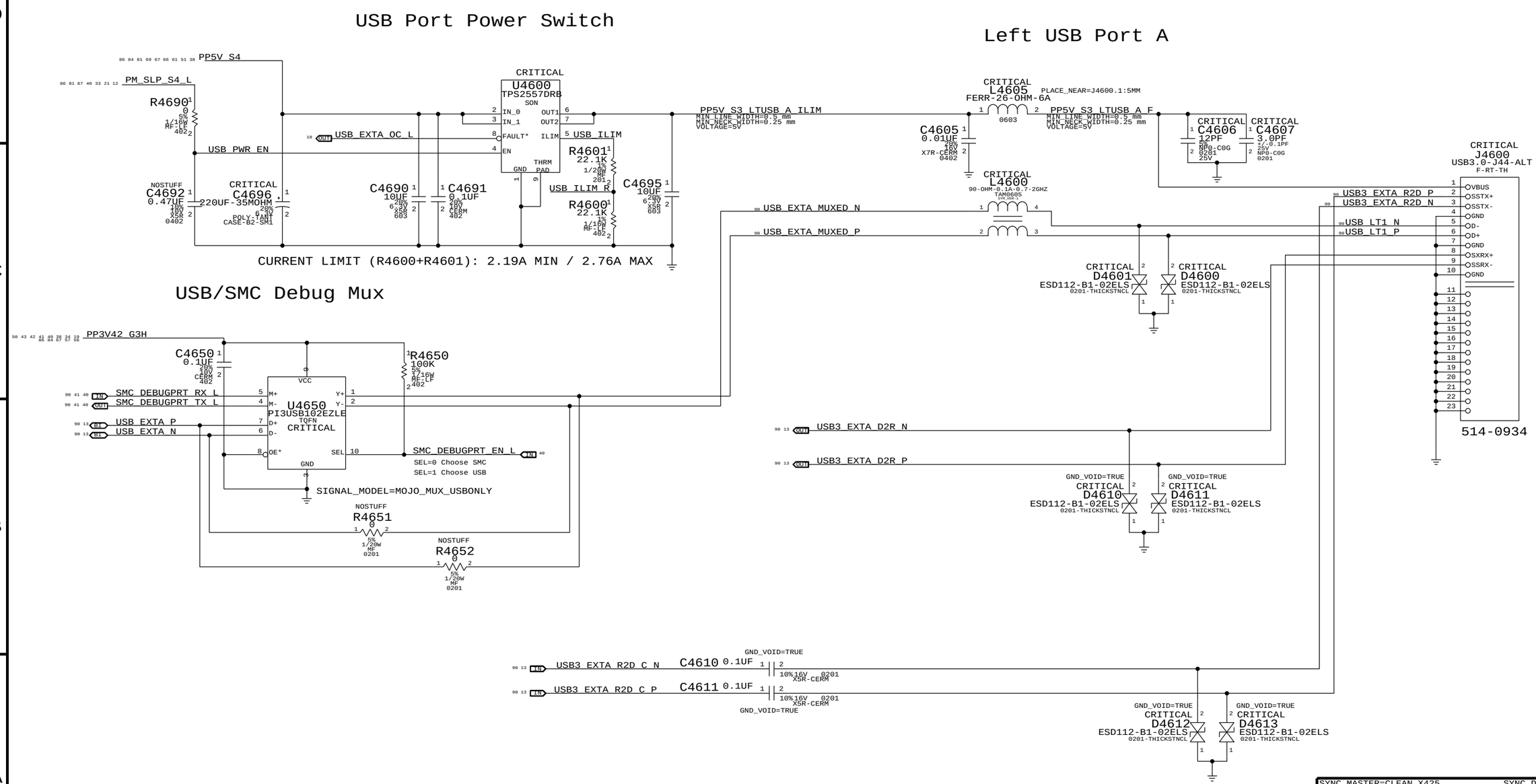

SYNC_MASTER=CLEAN_X425 SYNC_DATE=10/30/2014

PAGE TITLE

USB 3.0 CONNECTORS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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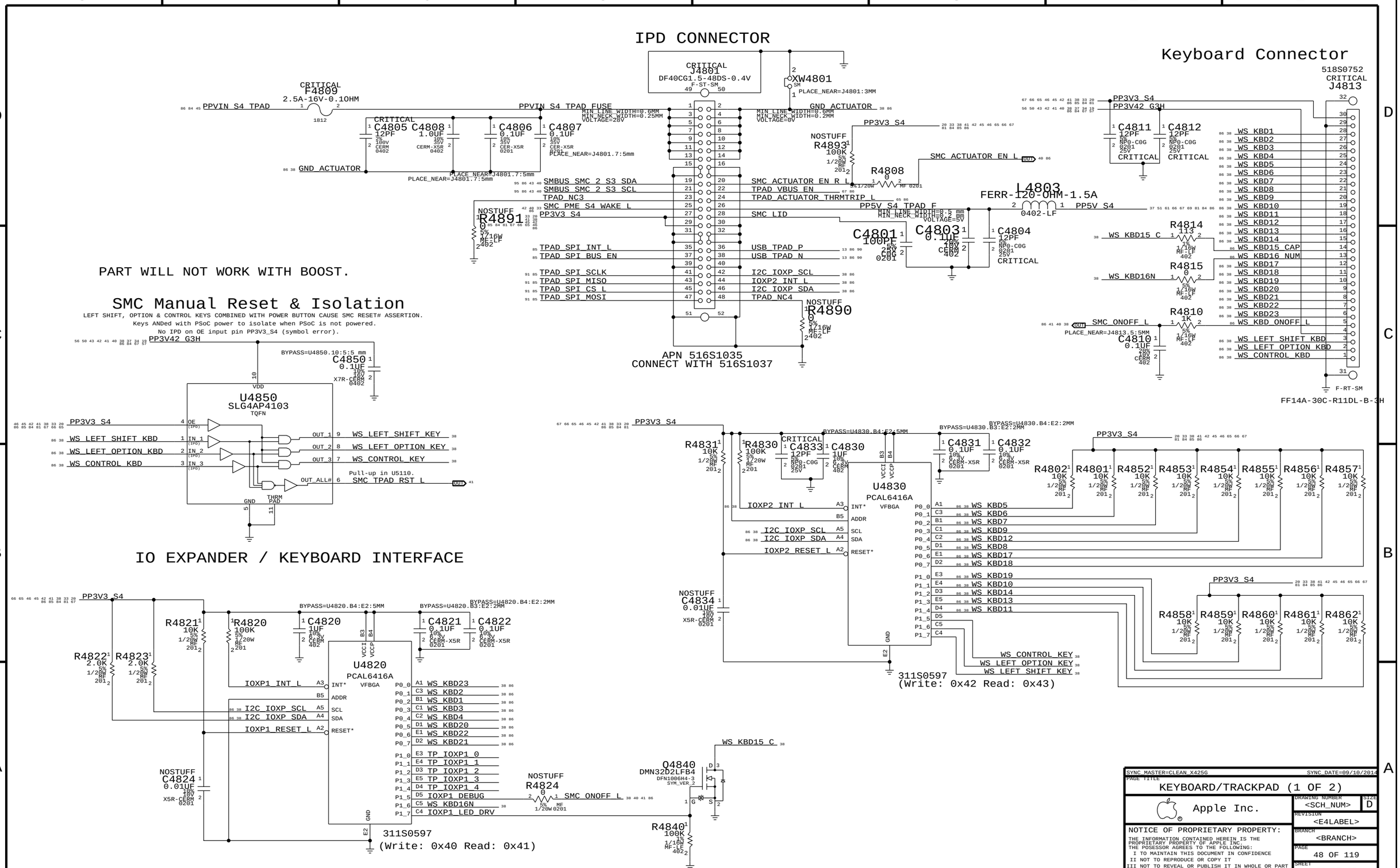

SYNC_MASTER=CLEAN_X425G SYNC_DATE=09/10/2014

PAGE TITLE: KEYBOARD/TRACKPAD (1 OF 2)

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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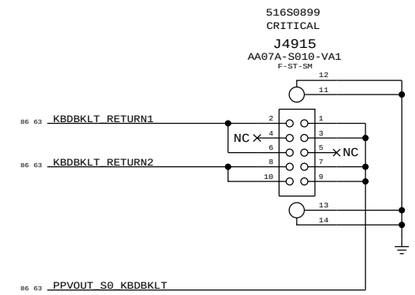
Keyboard Backlight Connector



SYNC_MASTER=CLEAN_MAXWELL SYNC_DATE=07/02/2014

PAGE TITLE
KEYBOARD/TRACKPAD (2 OF 2)

Apple Inc.

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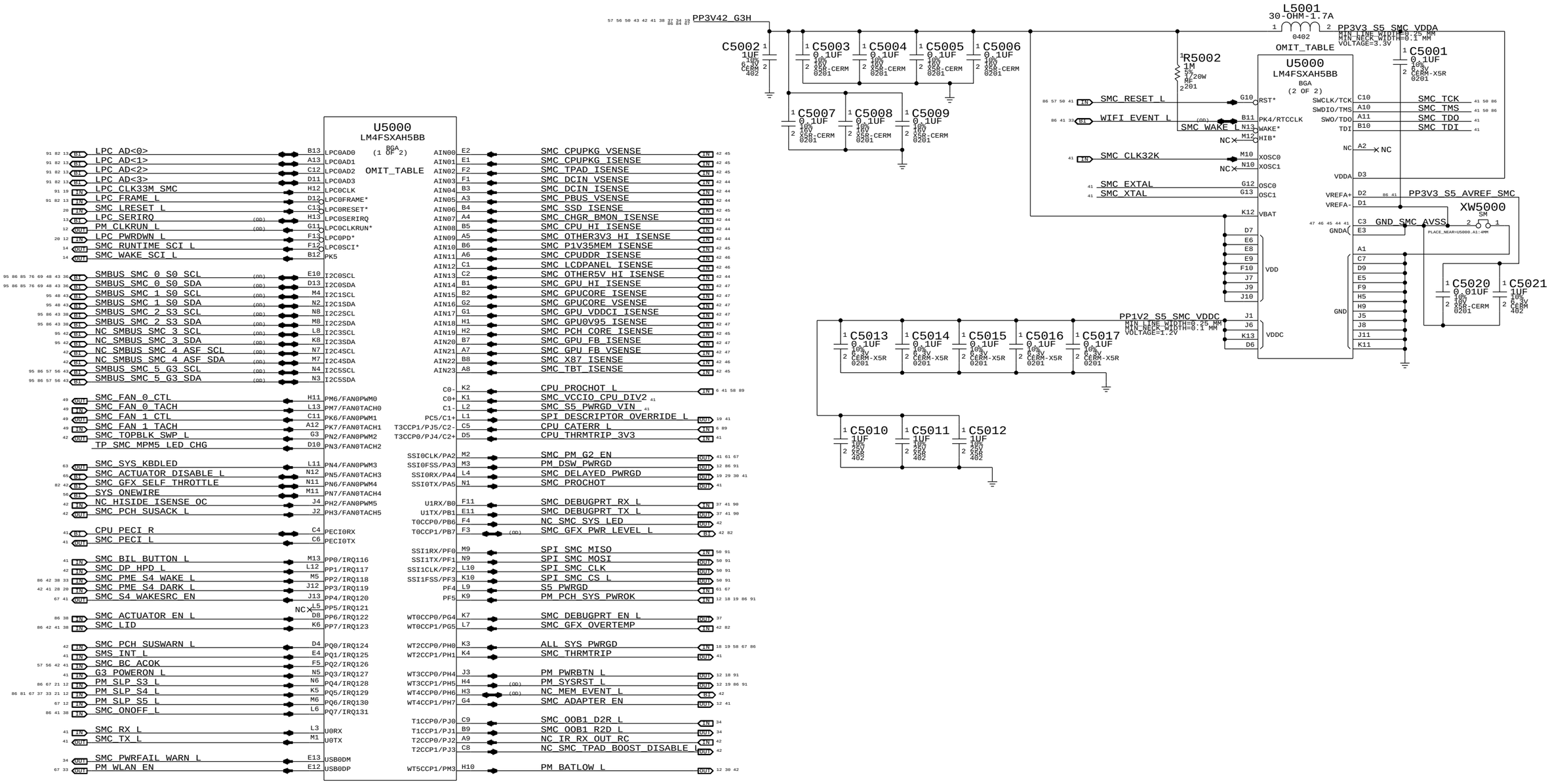
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC_MASTER=CLEAN_X305 SYNC_DATE=01/15/2014

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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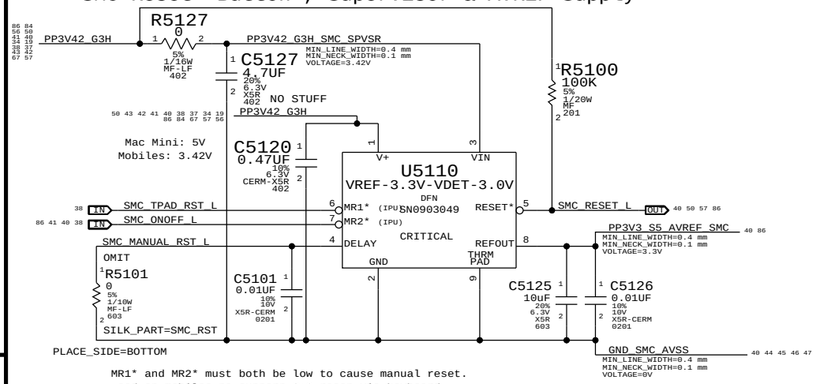
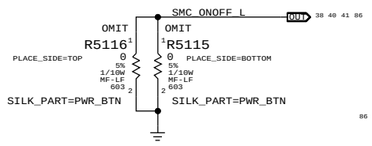
SMC Reset "Button", Supervisor & AVREF Supply



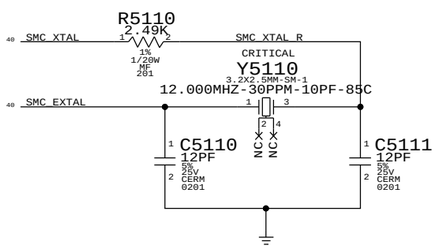
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

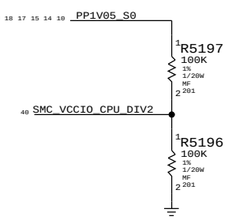
NOTE: Internal pull-ups are to VIN, not V+.

Debug Power "Buttons"



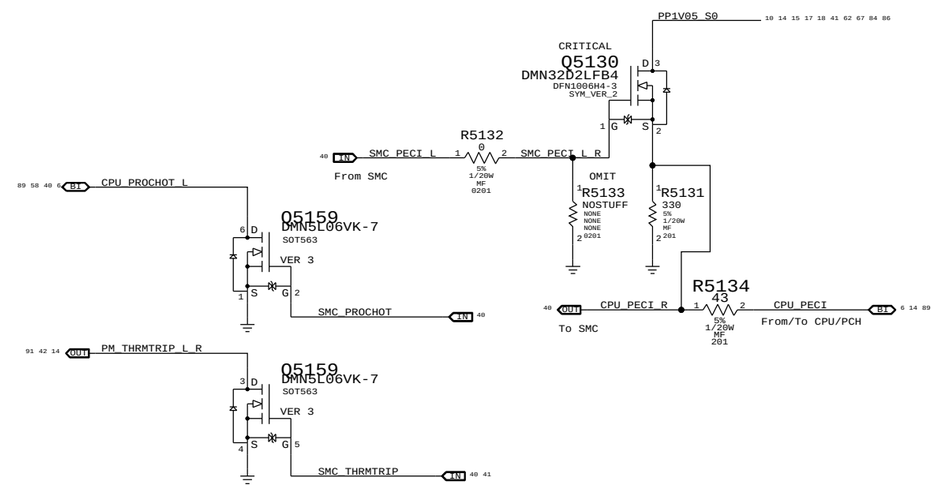
SMC Crystal Circuit

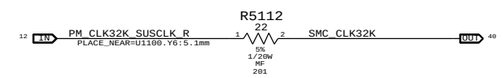


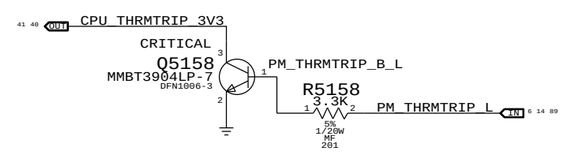


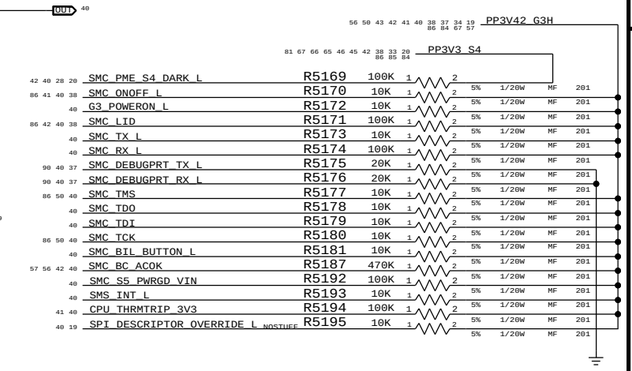
SMC USB CLOCK REQUIRE THESE CRYSTAL VALUES:5,6,8,10,12,16,18,20,24,25 MHZ

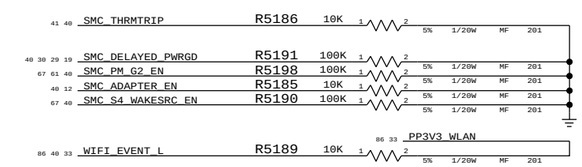
SMC12 PECI SUPPORT











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PAGE TITLE
SMC Shared Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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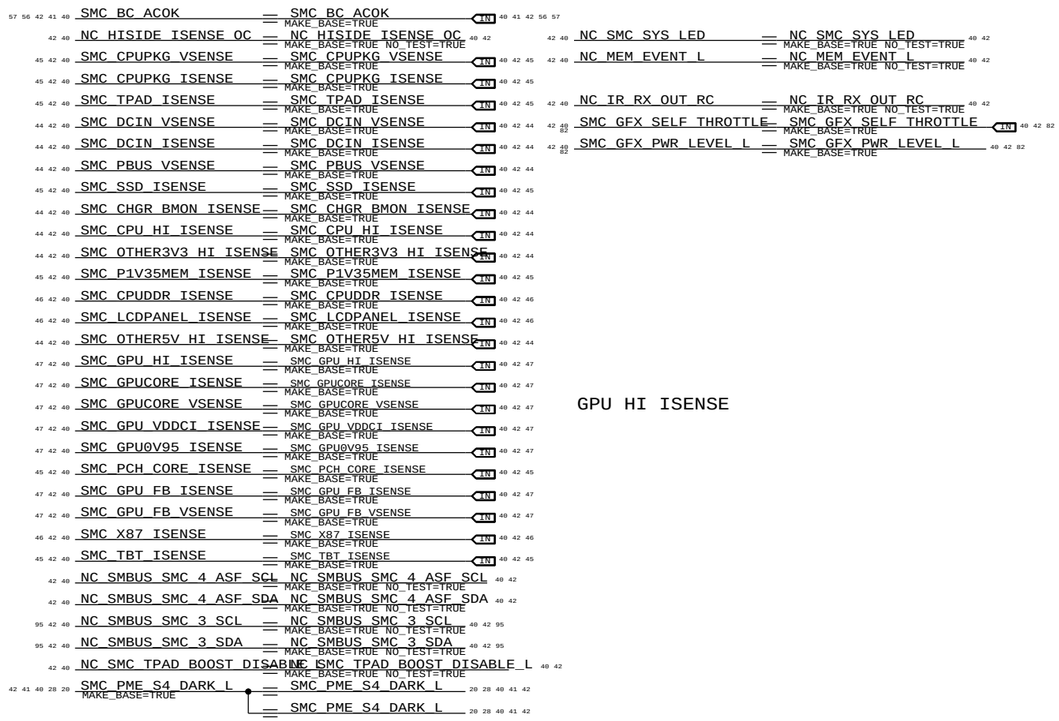
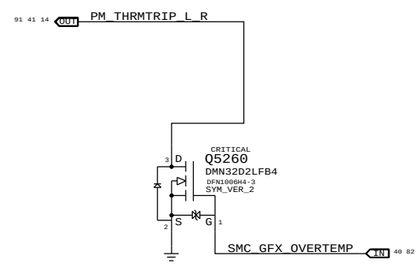
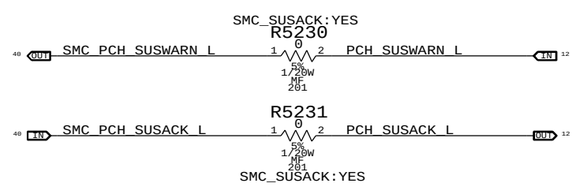
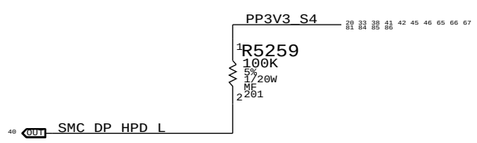


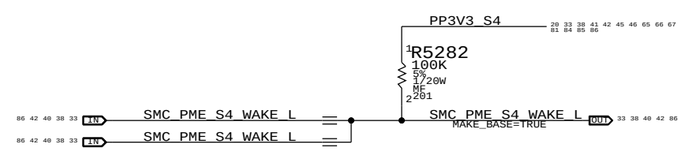
GPU HI ISENSE



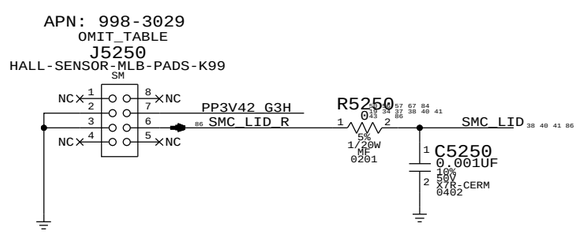


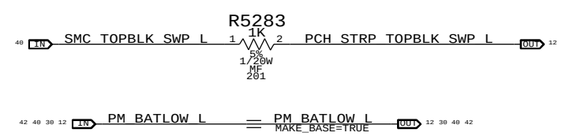
Spare S4 IRQ





Hall Effect pads





PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
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PAGE TITLE: SMC Project Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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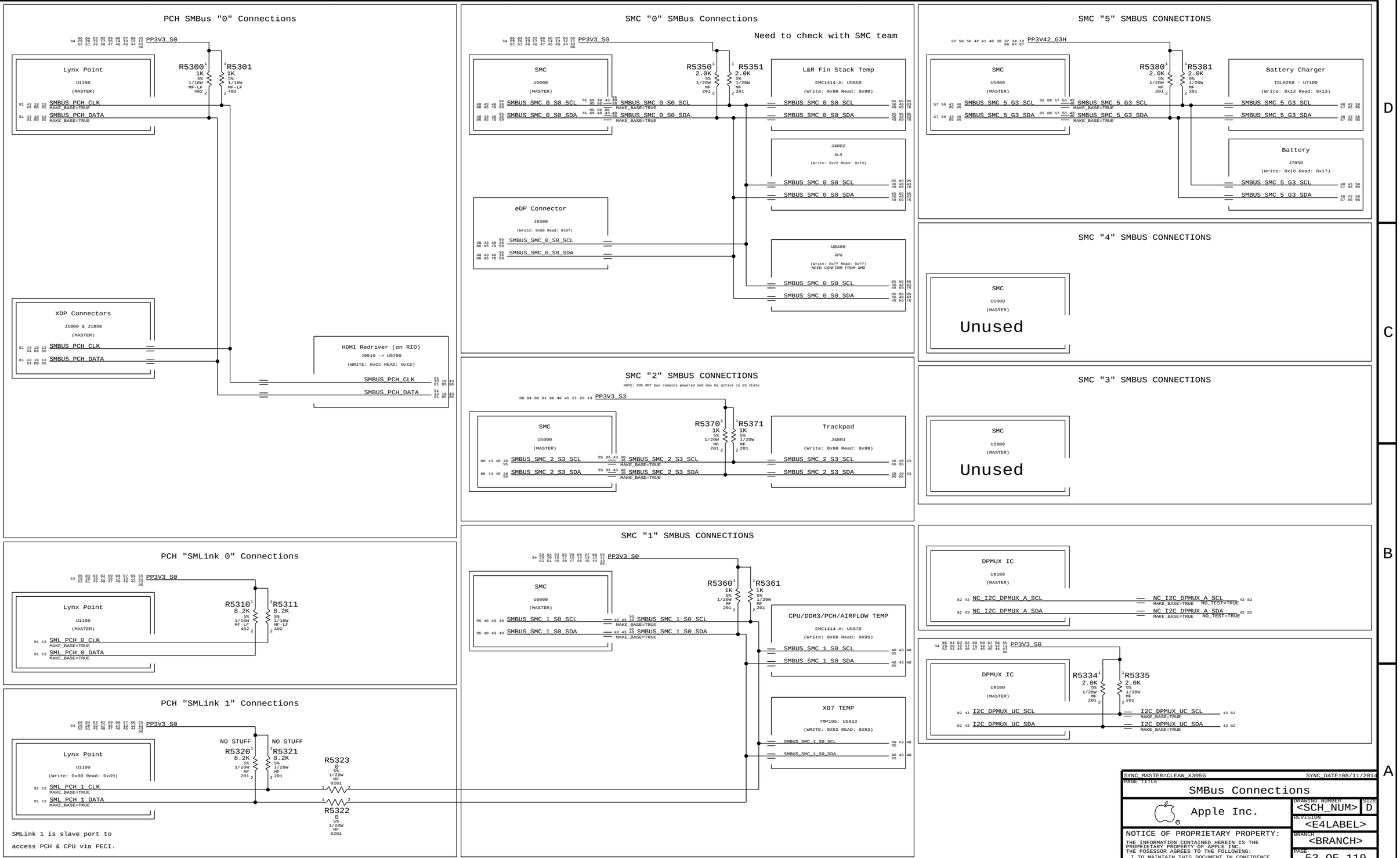

SYNC MASTER=CLEAN X305G SYNC DATE=08/11/2014

PAGE TITLE

SMBus Connections

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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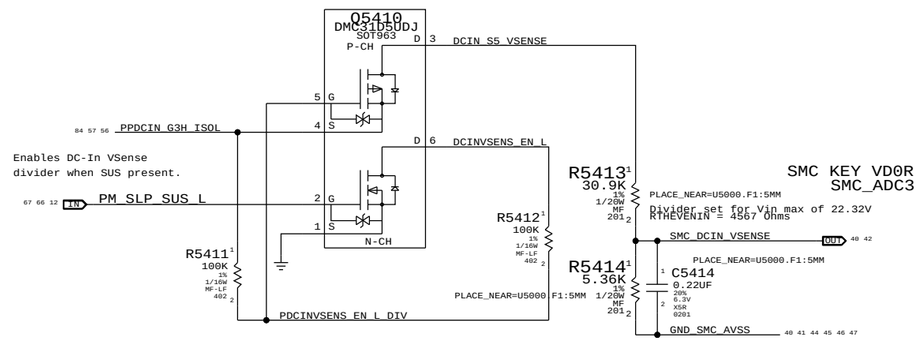
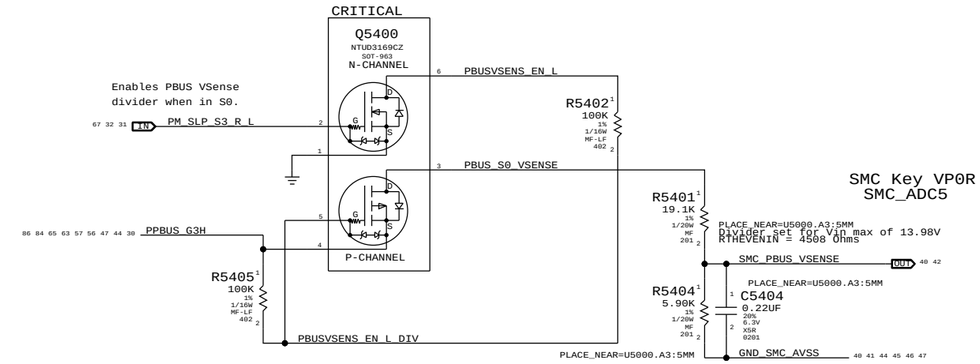
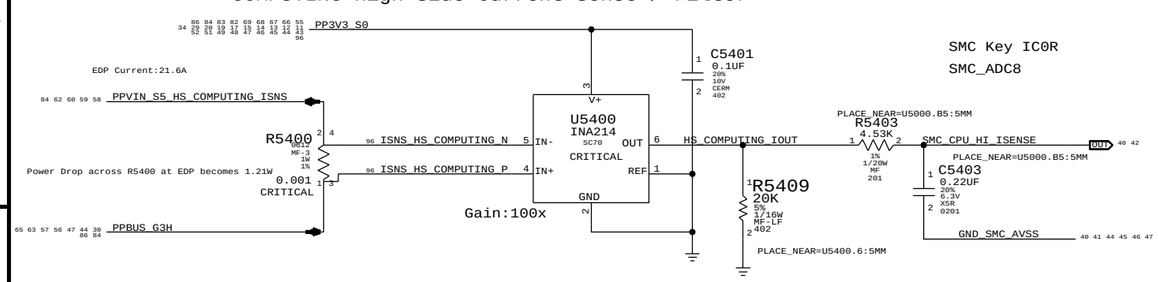
DC-In Voltage Sense Enable & Filter



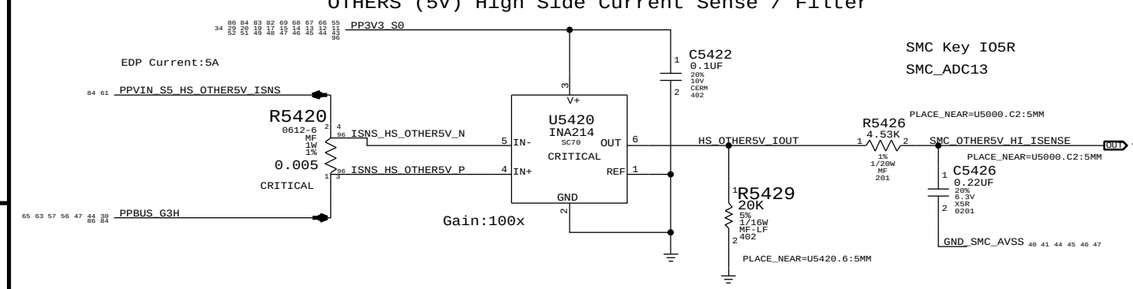
PBUS Voltage Sense Enable & Filter



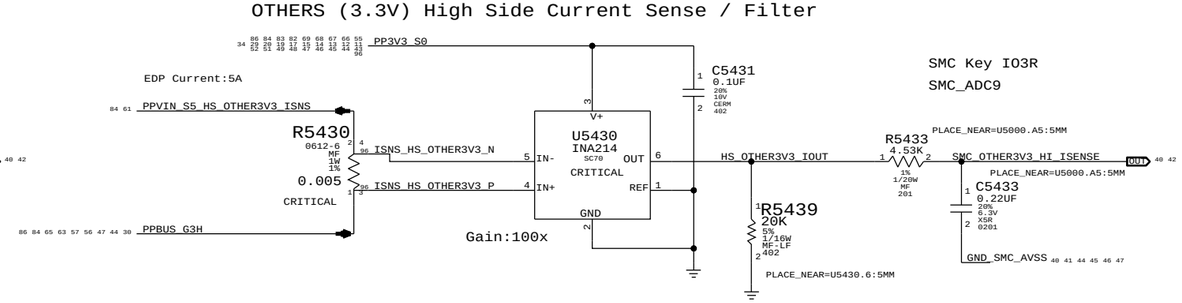
COMPUTING High Side Current Sense / Filter



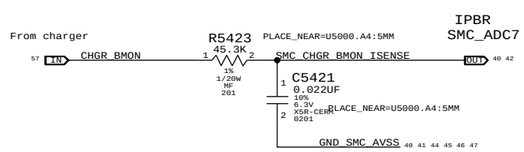
OTHERS (5V) High Side Current Sense / Filter



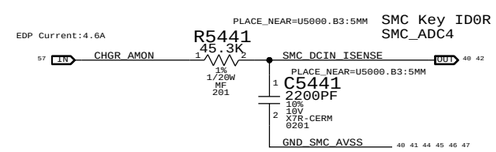
OTHERS (3.3V) High Side Current Sense / Filter



CHARGER BMON HIGH SIDE (BATTERY DISCHARGE) CURRENT SENSE & FILTER



DC-IN (AMON) Current Sense Filter



SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/18/2014

PAGE TITLE
High Side Voltage and Current Sensing

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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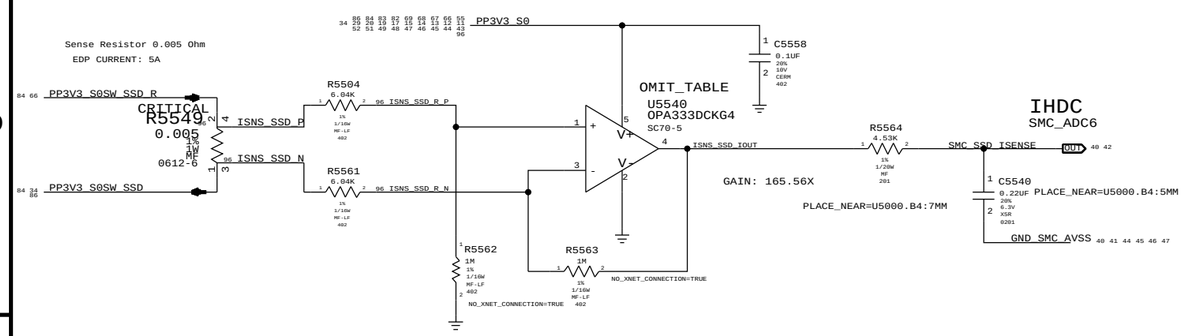
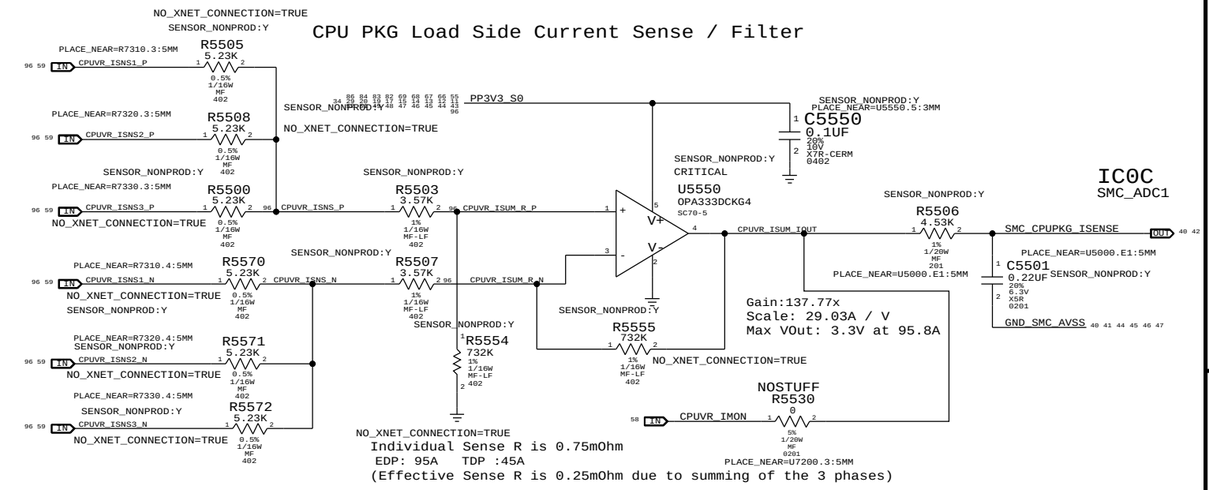
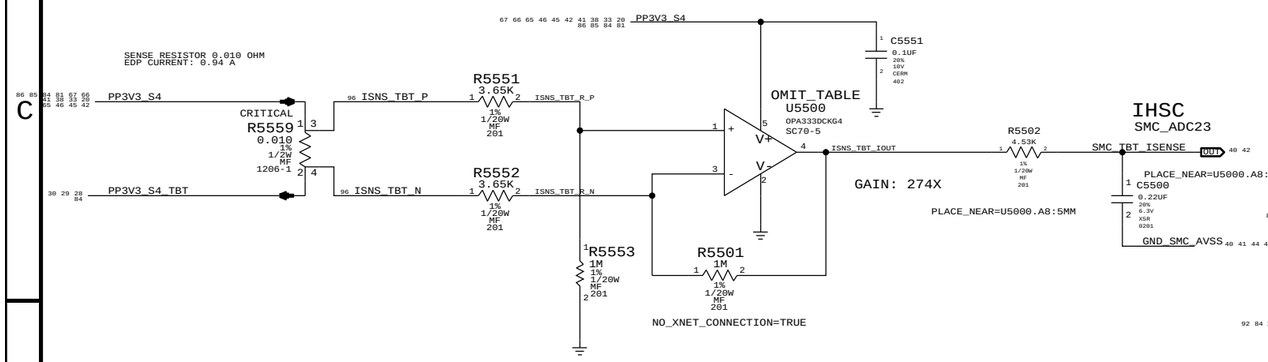
SSD CURRENT SENSE



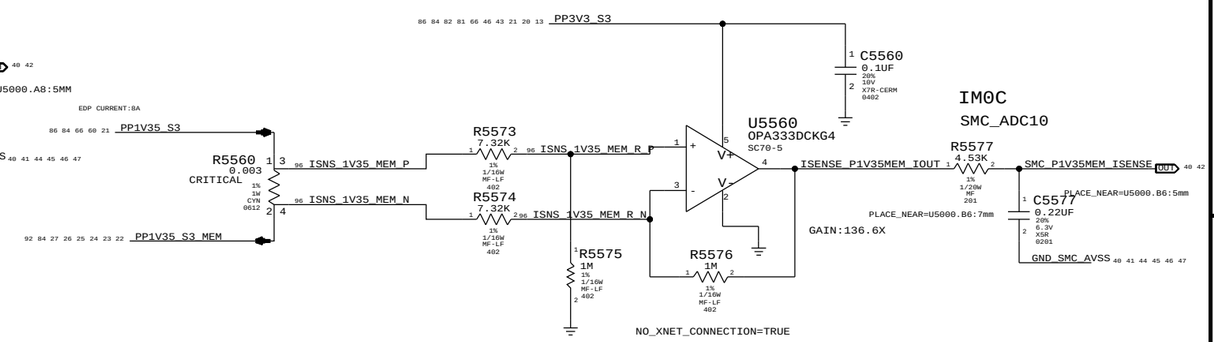
CPU PKG Load Side Current Sense / Filter



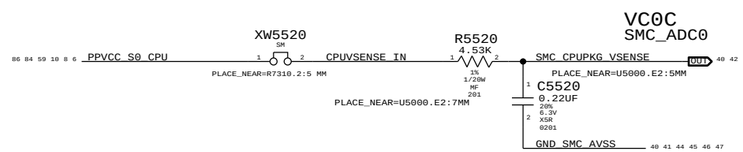
TBT Router CURRENT SENSE



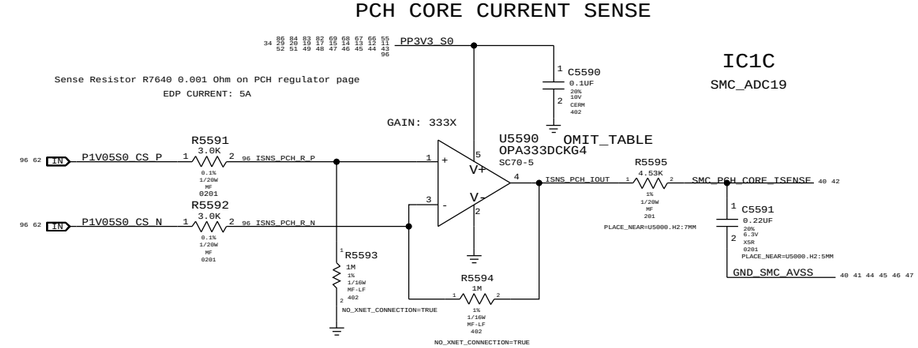
DDR3L 1.35V DRAM ONLY CURRENT SENSE / FILTER



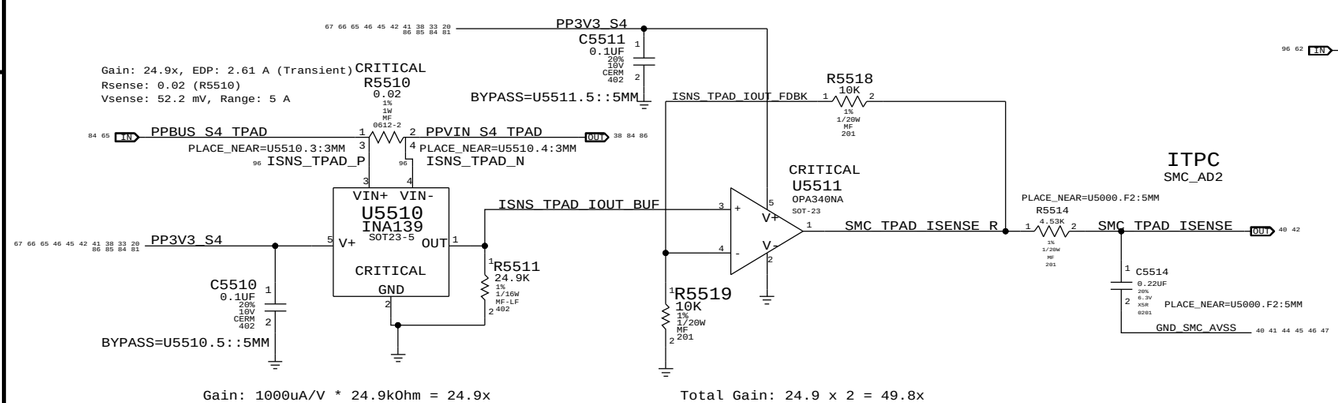
CPU Vcore Voltage Sense / Filter



PCH CORE CURRENT SENSE



TRACKPAD CURRENT SENSE



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
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SYNC_MASTER=CLEAN_X425G SYNC_DATE=09/10/2014

PAGE TITLE: Load Side Voltage and Current Sensing

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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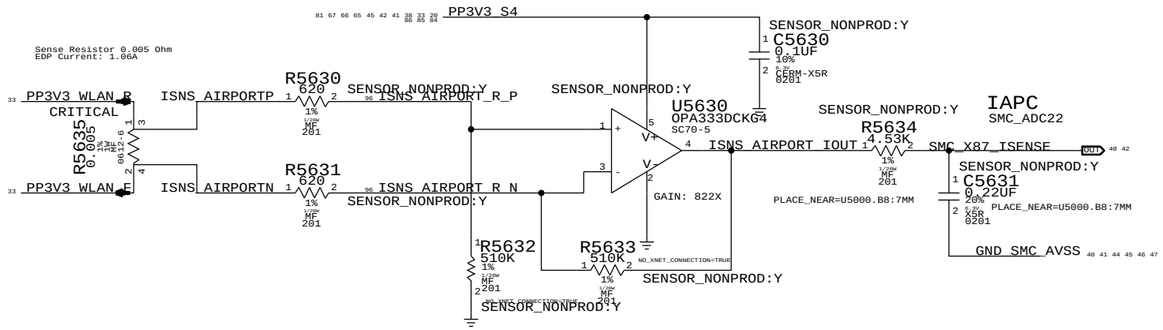
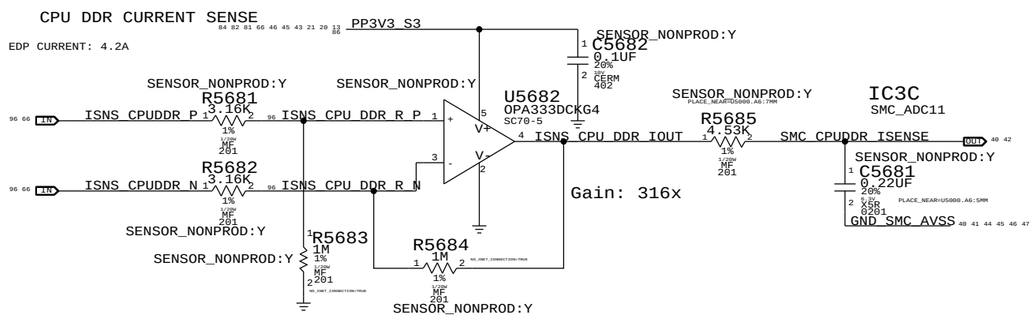
X87 AIRPORT CURRENT SENSE

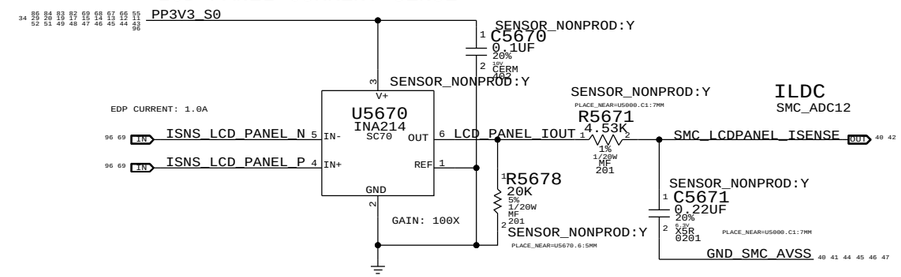


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	5	RES,MTL FILM,100K,5,1/20W,0201,SMD,LF	C5601,C5631,C5600,C5681,C5671		SENSOR_NONPROD:N

CPU DDR CURRENT SENSE

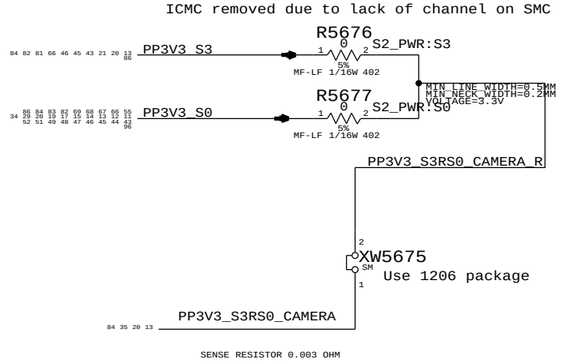


LCD PANEL CURRENT SENSE



S2 CAMERA CONTROLLER CURRENT SENSE

ICMC removed due to lack of channel on SMC



SYNC MASTER=CLEAN_X305 SYNC DATE=01/14/2014

PAGE TITLE
Debug Sensors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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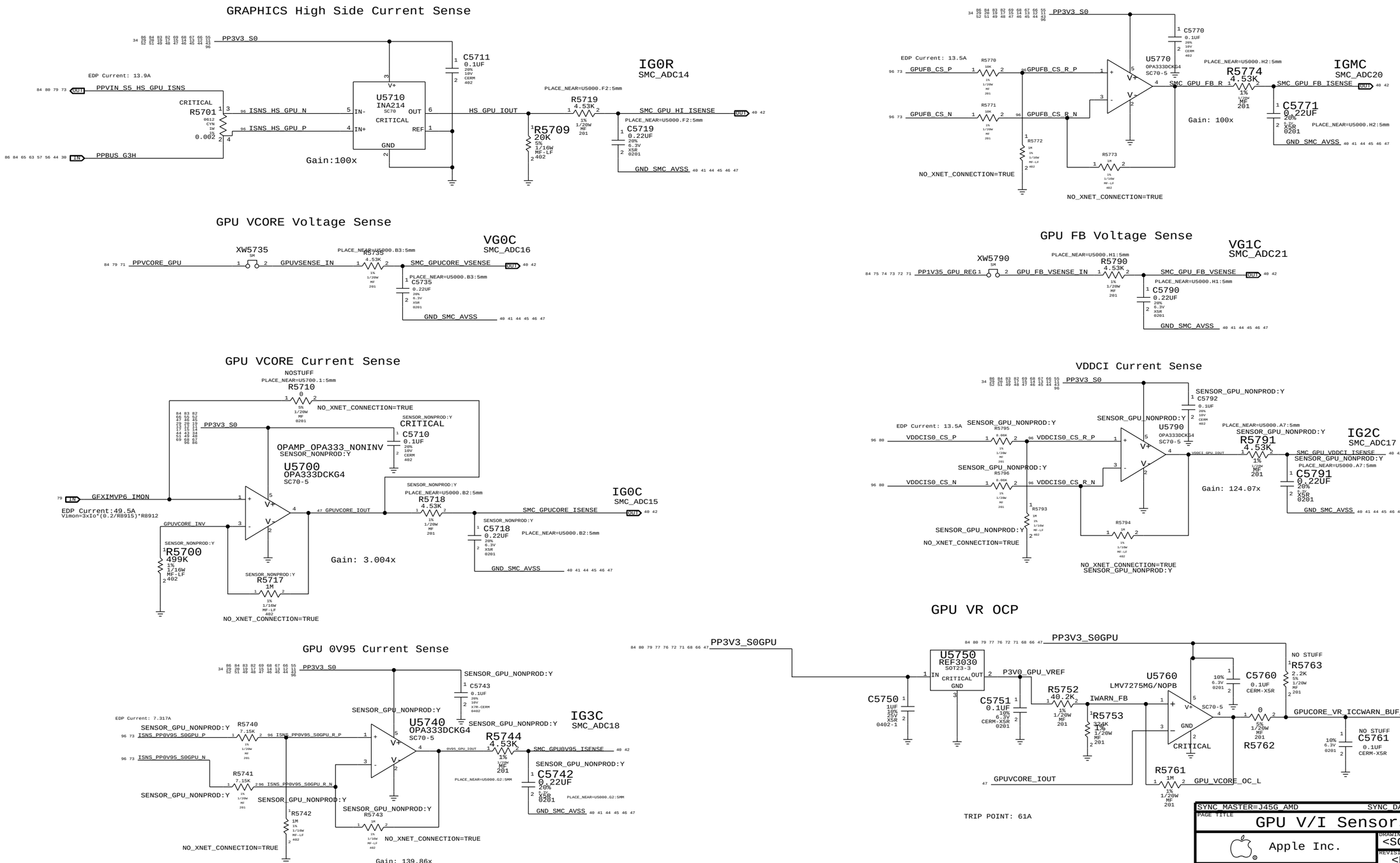

SYNC MASTER=J45G_AMD	SYNC DATE=07/01/2014
PAGE TITLE	GPU V/I Sensors
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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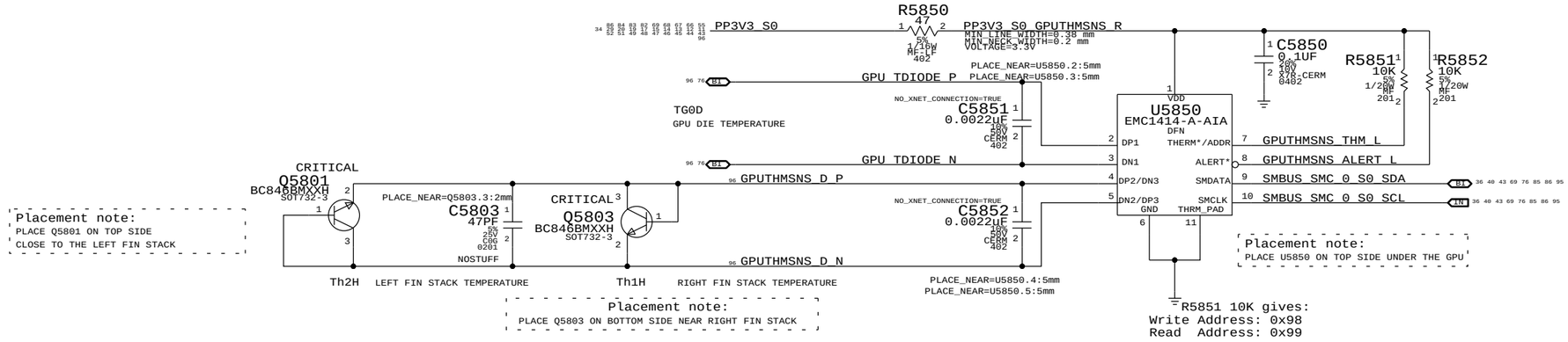
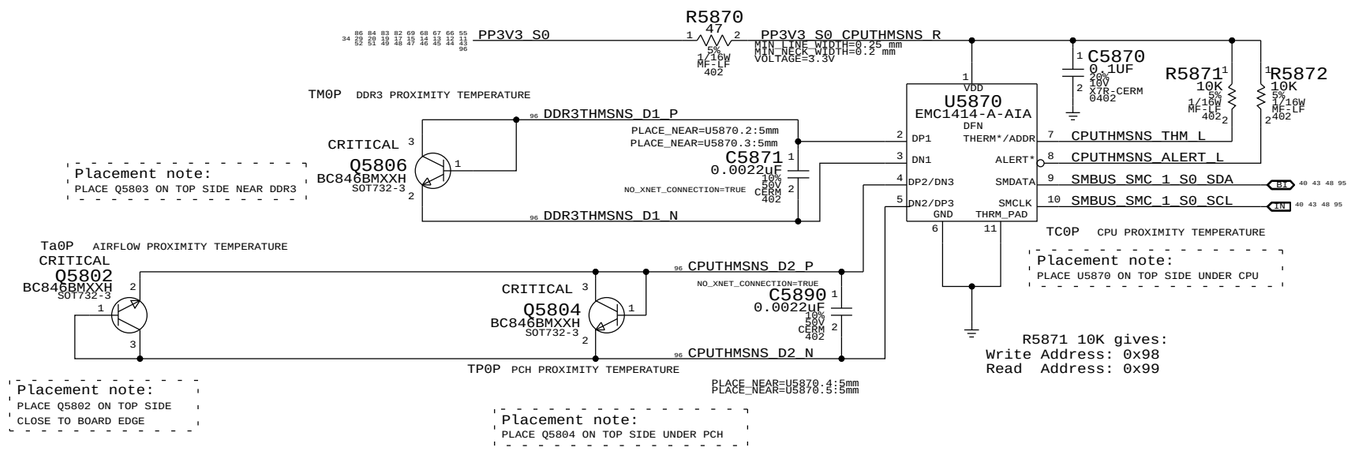
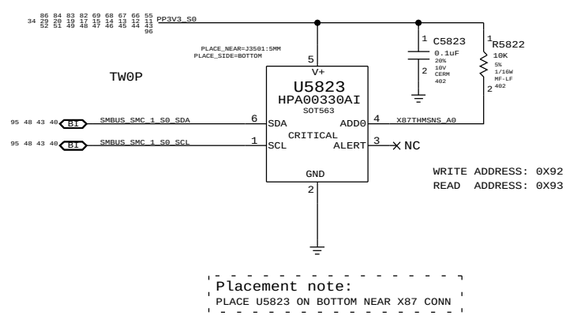
GPU PROXIMITY/GPU DIE/LEFT FIN STACK/RIGHT FIN STACK



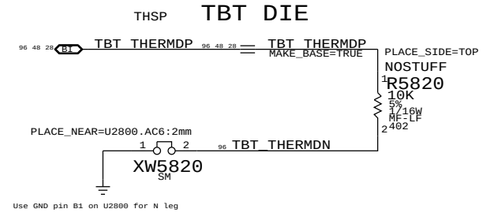
DDR3 PROXIMITY/CPU PROXIMITY/PCH PROXIMITY/AIRFLOW PROXIMITY



X87 PROXIMITY



TBT DIE



SYNC_MASTER=CHANG_J45 SYNC_DATE=11/26/2012

PAGE TITLE

Thermal Sensors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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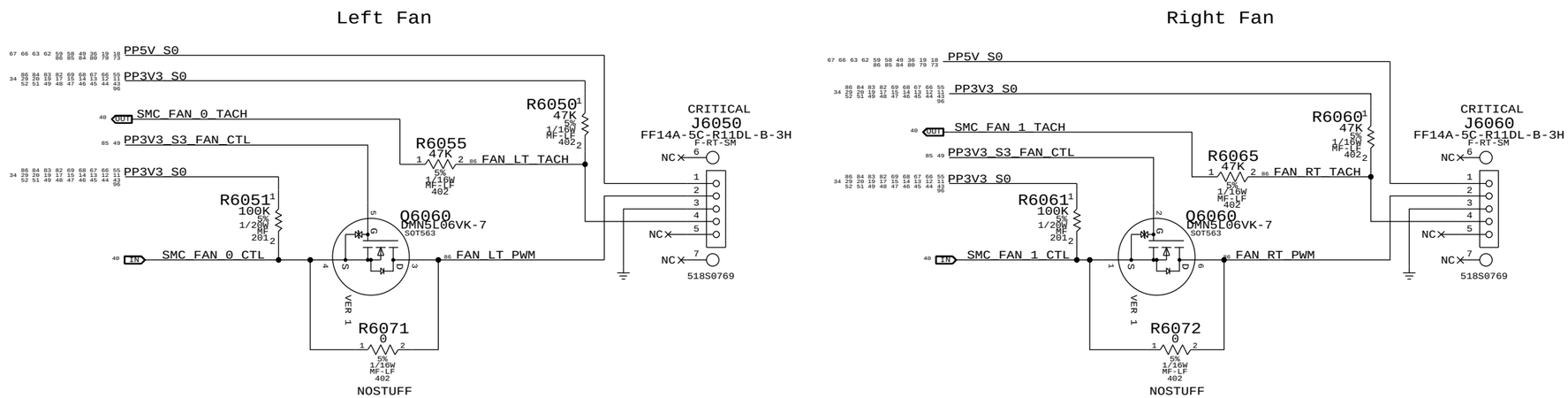

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE

Fan Connectors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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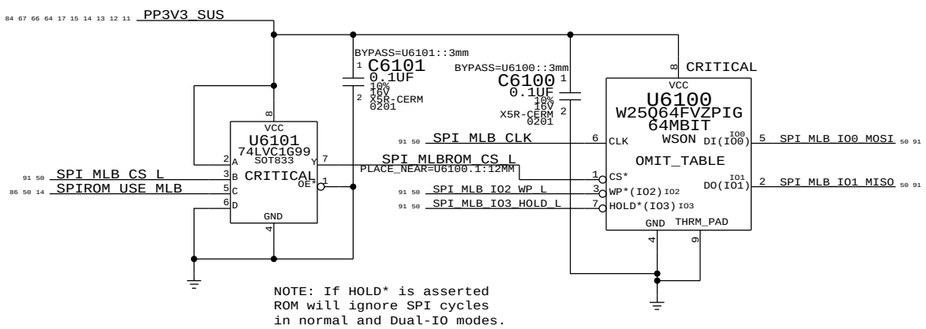
SPI ROM

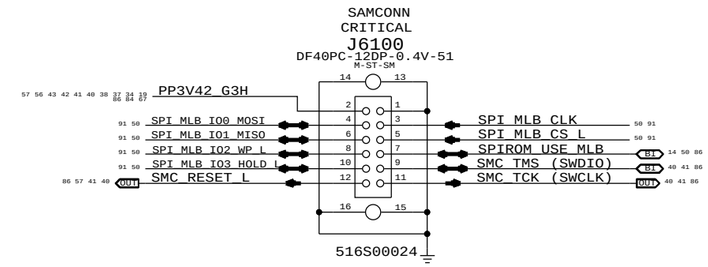
Quad-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.



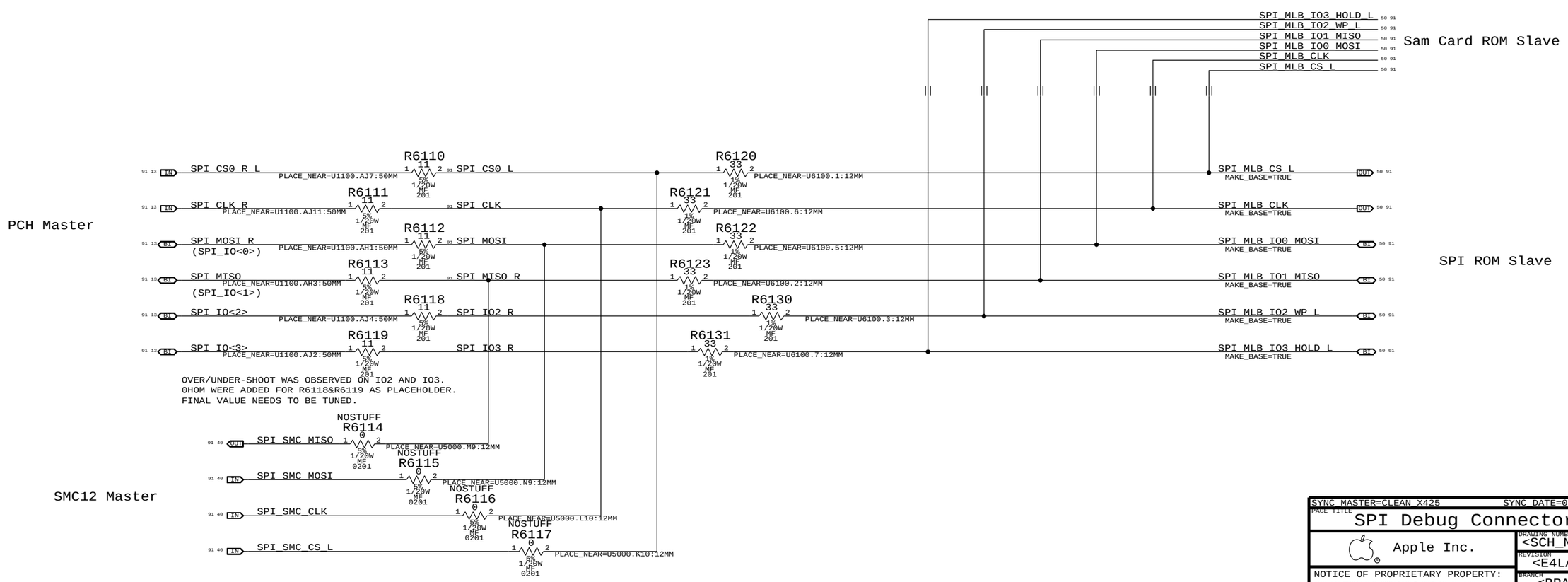
NOTE: If HOLD* is asserted
ROM will ignore SPI cycles
in normal and Dual-IO modes.

Quad SPI and QPI instructions require the non-volatile Quad Enable bit (QE)
in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

SPI+SWD SAM Connector



SPI Bus Series Termination



SYNC_MASTER=CLEAN_X425 SYNC_DATE=08/15/2014

PAGE TITLE
SPI Debug Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
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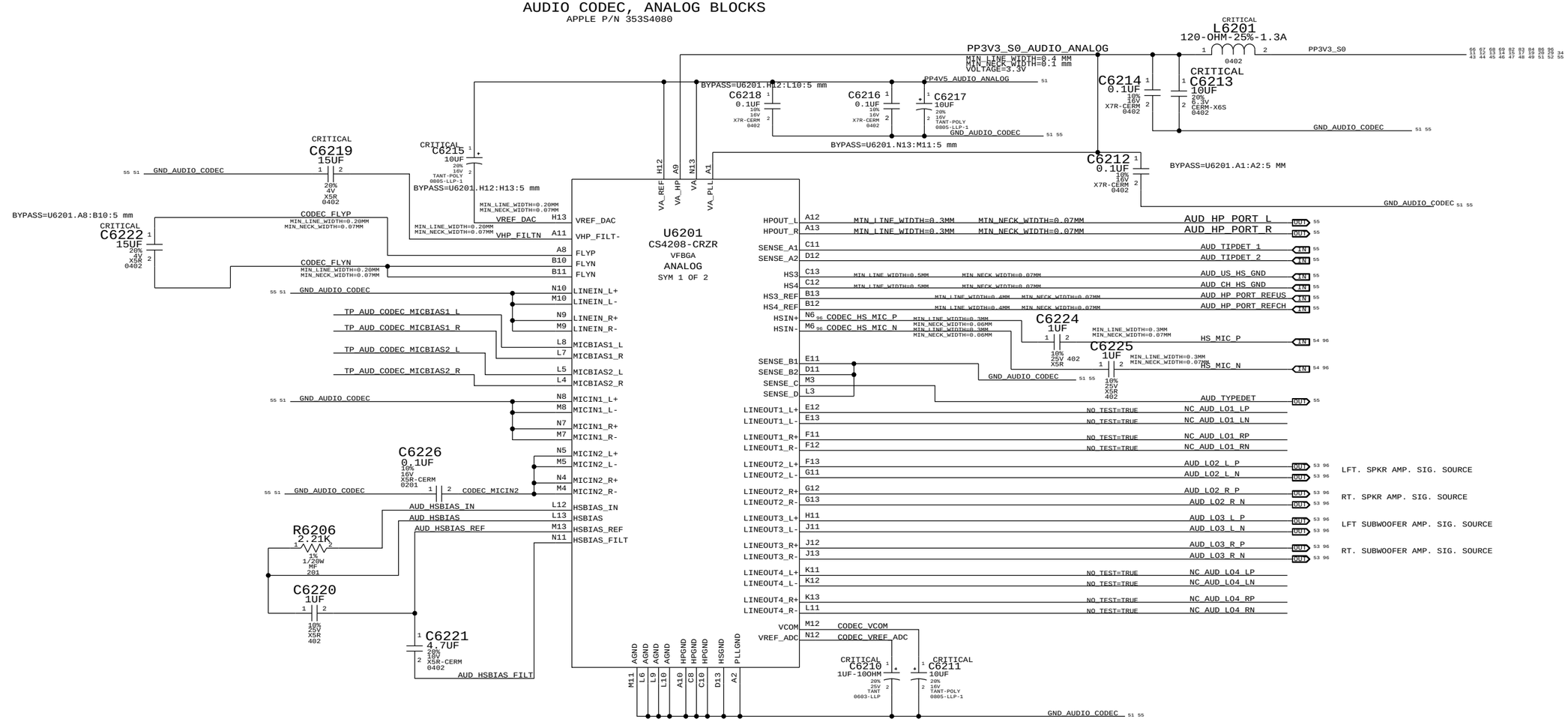
AUDIO CODEC, ANALOG BLOCKS

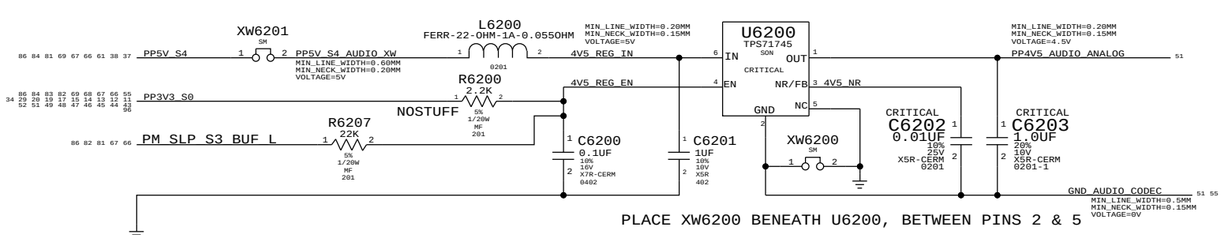
APPLE P/N 353S4080



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456

PLACE XW6201 NEAR 5V SOURCE



PLACE XW6200 BENEATH U6200, BETWEEN PINS 2 & 5

SYNC_MASTER=J0E_J45 SYNC_DATE=07/30/2013

PAGE TITLE
AUDIO:CODEC, ANALOG

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 62 OF 119

SHEET 51 OF 97

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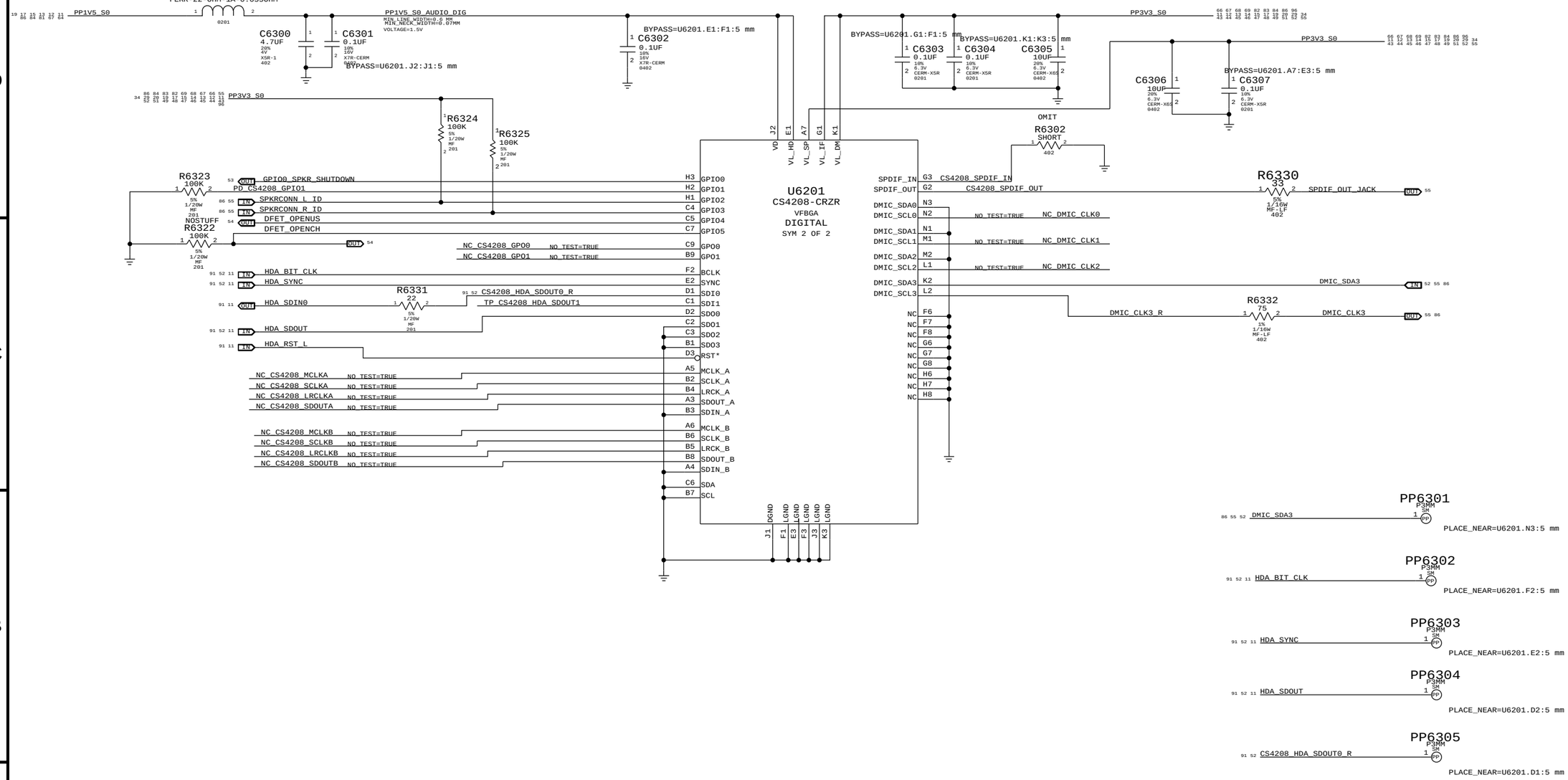
AUDIO CODEC, DIGITAL BLOCKS

APPLE P/N 353S4080



SYNC_MASTER=JOE_J45 SYNC_DATE=07/30/2013

PAGE TITLE

AUDIO:CODEC, DIGITAL

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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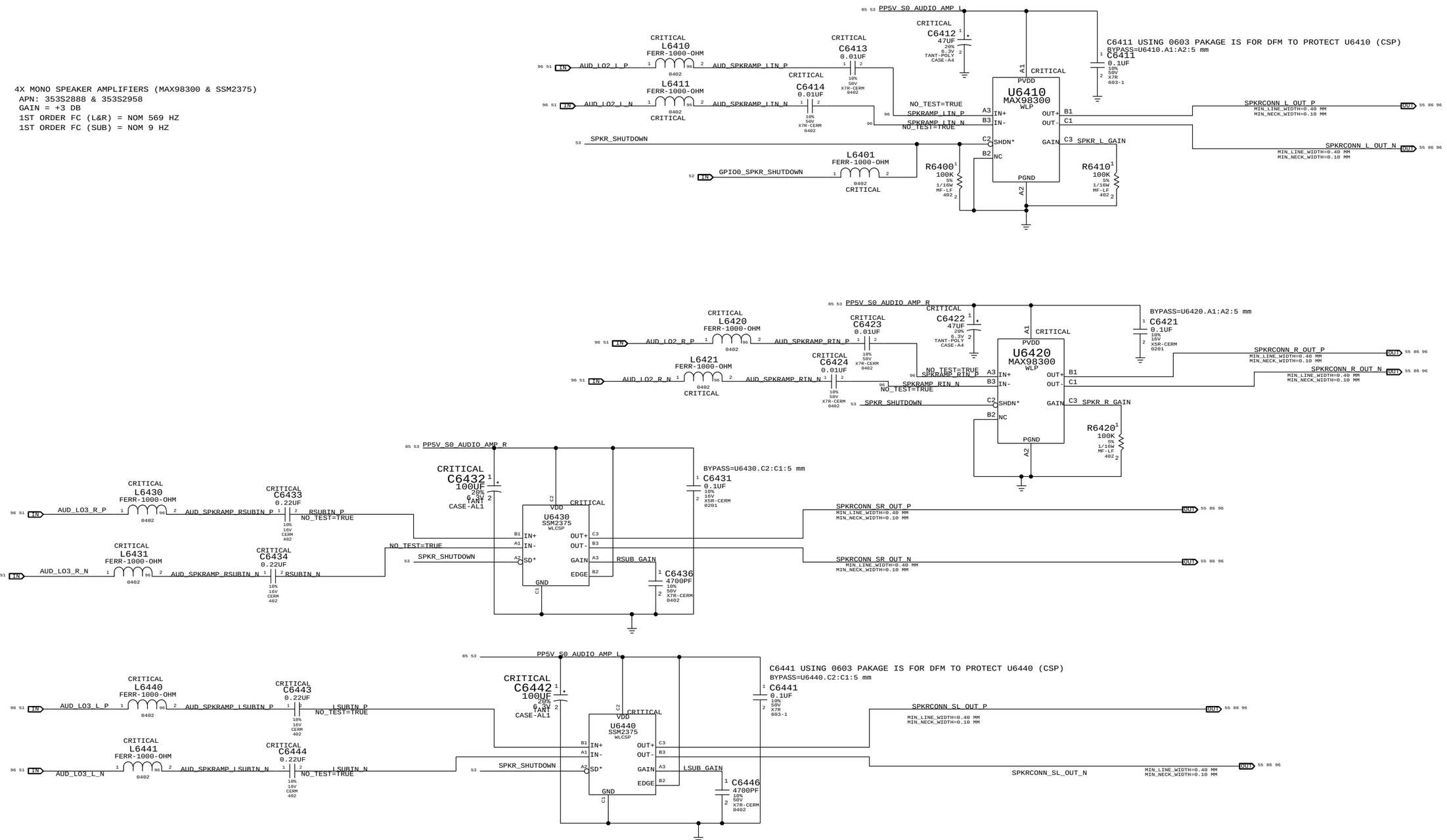
4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ



SYNC_MASTER=JOE_J45 SYNC_DATE=07/30/2013

PAGE TITLE
AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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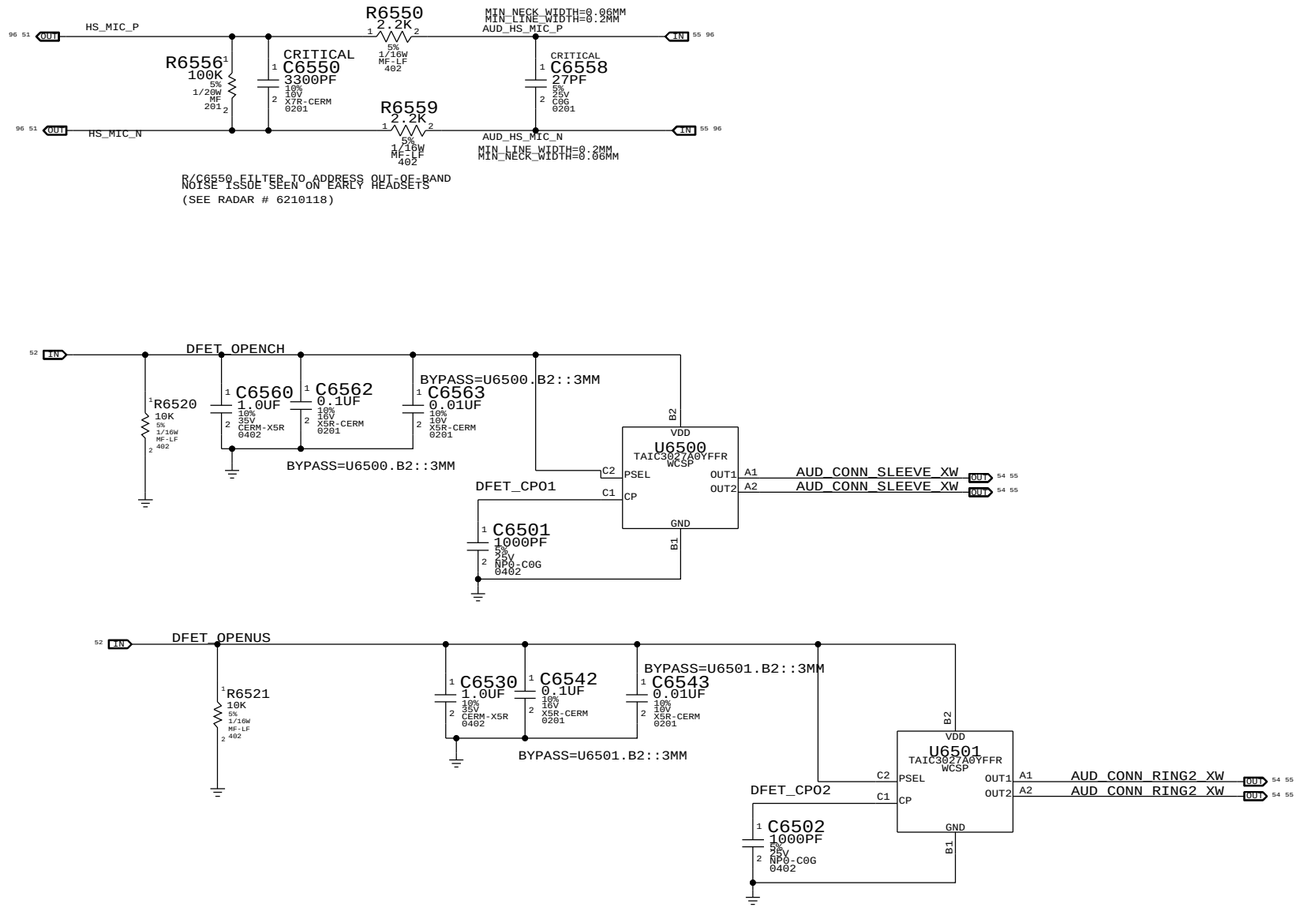

SYNC_MASTER=CLEAN_X305 SYNC_DATE=06/24/2014

PAGE TITLE

AUDIO: JACK

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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CODEC OUTPUT SIGNAL PATHS

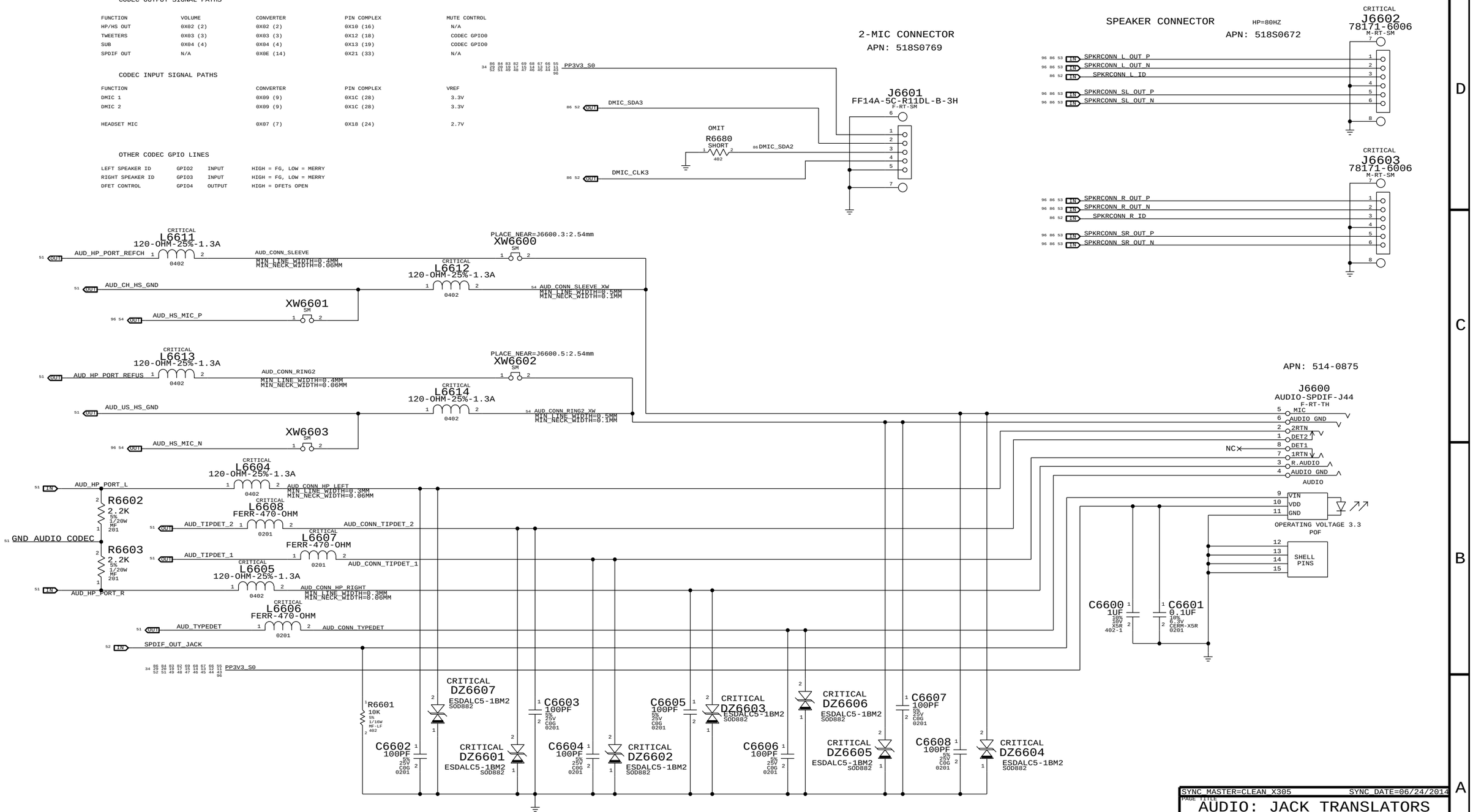
FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL
HP/HS OUT	0X02 (2)	0X02 (2)	0X10 (16)	N/A
TWEETERS	0X03 (3)	0X03 (3)	0X12 (18)	CODEC GPIO0
SUB	0X04 (4)	0X04 (4)	0X13 (19)	CODEC GPIO0
SPDIF OUT	N/A	0X0E (14)	0X21 (33)	N/A

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF
DMIC 1	0X09 (9)	0X1C (28)	3.3V
DMIC 2	0X09 (9)	0X1C (28)	3.3V
HEADSET MIC	0X07 (7)	0X18 (24)	2.7V

OTHER CODEC GPIO LINES

LEFT SPEAKER ID	GPIO2	INPUT	HIGH = FG, LOW = MERRY
RIGHT SPEAKER ID	GPIO3	INPUT	HIGH = FG, LOW = MERRY
DFET CONTROL	GPIO4	OUTPUT	HIGH = DFETs OPEN



SYNC_MASTER=CLEAN_X305 SYNC_DATE=06/24/2014

PAGE TITLE

AUDIO: JACK TRANSLATORS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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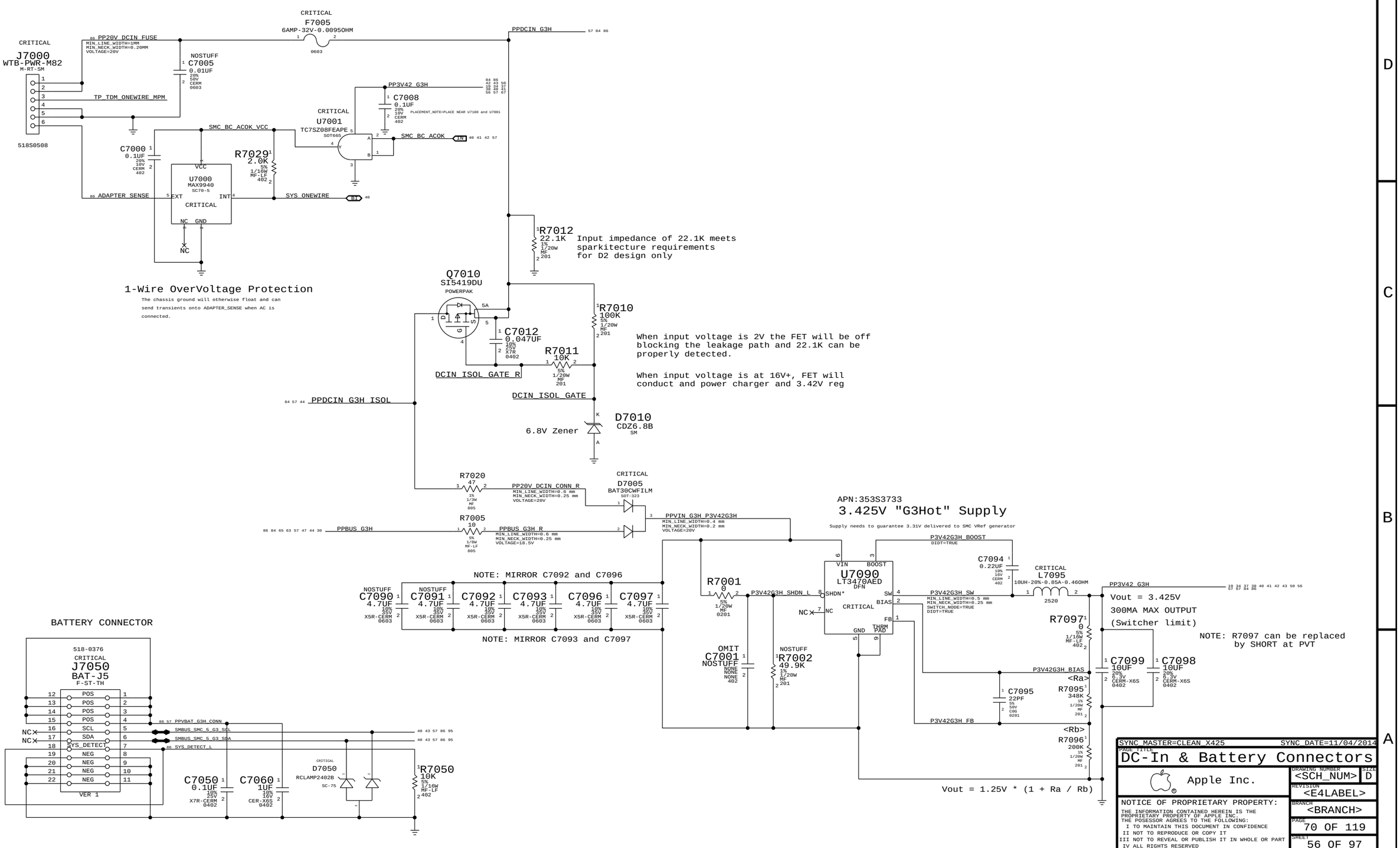
MagSafe DC Power Jack
CRITICAL
J7000
WTB-PWR-M82
M-RT-SM
518S0508
86 PP20V_DCIN_FUSE
MIN_LINE_WIDTH=1MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=20V
CRITICAL
F7005
6AMP-32V-0.00950HM
0603
PPDCIN_G3H
57 84 86
NOSTUFF
C7005
0.01UF
20%
50V
CERM
0603
TP_TDM_ONEWIRE_MPM
PP3V42_G3H
84 86
42 43 50
38 39 41
56 57 67
C7008
0.1UF
20%
10V
CERM
402
PLACEMENT_NOTE=PLACE NEAR U7100 and U7001
CRITICAL
U7001
TC7SZ08FEAPE
SOT665
SMC_BC_ACOK_VCC
SMC_BC_ACOK
IN 40 41 42 57
C7000
0.1UF
20%
10V
CERM
402
R7029
2.0K
5%
1/16W
MF-LF
402
VCC
U7000
MAX9940
SC70-5
CRITICAL
86 ADAPTER_SENSE
EXT
INT
SYS_ONEWIRE
B1 40
NC GND
NC
1-Wire OverVoltage Protection
The chassis ground will otherwise float and can
send transients onto ADAPTER_SENSE when AC is
connected.
R7012
22.1K
1%
1/20W
MF
201
Input impedance of 22.1K meets
sparkitecture requirements
for D2 design only
Q7010
SI5419DU
POWERPAK
5A
R7010
100K
5%
1/20W
MF
201
C7012
0.047UF
10%
25V
X7R
0402
R7011
10K
5%
1/20W
MF
201
When input voltage is 2V the FET will be off
blocking the leakage path and 22.1K can be
properly detected.
When input voltage is at 16V+, FET will
conduct and power charger and 3.42V reg
DCIN_ISOL_GATE_R
DCIN_ISOL_GATE
84 57 44 PPDCIN_G3H_ISOL
D7010
CDZ6.8B
SM
6.8V Zener
R7020
47
1%
1/3W
MF
805
PP20V_DCIN_CONN_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=20V
CRITICAL
D7005
BAT30CWFILM
SOT-323
R7005
10
5%
1/8W
MF-LF
805
86 84 65 63 57 47 44 30 PPBUS_G3H
PPBUS_G3H_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=18.5V
PPVIN_G3H_P3V42G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=20V
APN:353S3733
3.425V "G3Hot" Supply
Supply needs to guarantee 3.31V delivered to SMC VRef generator
NOTE: MIRROR C7092 and C7096
NOSTUFF
C7090
4.7UF
10%
35V
X5R-CERM
0603
NOSTUFF
C7091
4.7UF
10%
35V
X5R-CERM
0603
C7092
4.7UF
10%
35V
X5R-CERM
0603
C7093
4.7UF
10%
35V
X5R-CERM
0603
C7096
4.7UF
10%
35V
X5R-CERM
0603
C7097
4.7UF
10%
35V
X5R-CERM
0603
NOTE: MIRROR C7093 and C7097
R7001
0
5%
1/20W
MF
0201
P3V42G3H_SHDN_L
OMIT
C7001
NOSTUFF
NONE
NONE
NONE
402
NOSTUFF
R7002
49.9K
1%
1/20W
MF
201
U7090
LT3470AED
DFN
VIN
BOOST
SHDN*
NC
SW
BIAS
FB
THRM
GND
PAD
CRITICAL
P3V42G3H_BOOST
DIDT=TRUE
P3V42G3H_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE
C7094
0.22UF
10%
16V
CERM
402
CRITICAL
L7095
10UH-20%-0.85A-0.460HM
2520
PP3V42_G3H
19 24 37 38 40 41 42 43 50 56
57 67 84 86
Vout = 3.425V
300MA MAX OUTPUT
(Switcher limit)
NOTE: R7097 can be replaced
by SHORT at PVT
R7097
0
5%
1/16W
MF-LF
402
C7099
10UF
20%
6.3V
CERM-X6S
0402
C7098
10UF
20%
6.3V
CERM-X6S
0402
P3V42G3H_BIAS
<Ra>
C7095
22PF
5%
50V
C0G
0201
R7095
348K
1%
1/20W
MF
201
P3V42G3H_FB
<Rb>
R7096
200K
1%
1/20W
MF
201
Vout = 1.25V * (1 + Ra / Rb)
BATTERY CONNECTOR
518-0376
CRITICAL
J7050
BAT-J5
F-ST-TH
POS
SCL
SDA
SYS_DETECT
NEG
VER 1
NC
86 57 PPVBAT_G3H_CONN
SMBUS_SMC_5_G3_SCL
SMBUS_SMC_5_G3_SDA
86 SYS_DETECT_L
40 43 57 86 95
C7050
0.1UF
10%
25V
X7R-CERM
0402
C7060
1UF
10%
16V
CER-X6S
0402
CRITICAL
D7050
RCLAMP2402B
SC-75
R7050
10K
5%
1/16W
MF-LF
402
SYNC_MASTER=CLEAN X425
SYNC_DATE=11/04/2014
PAGE TITLE
DC-In & Battery Connectors
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
PAGE
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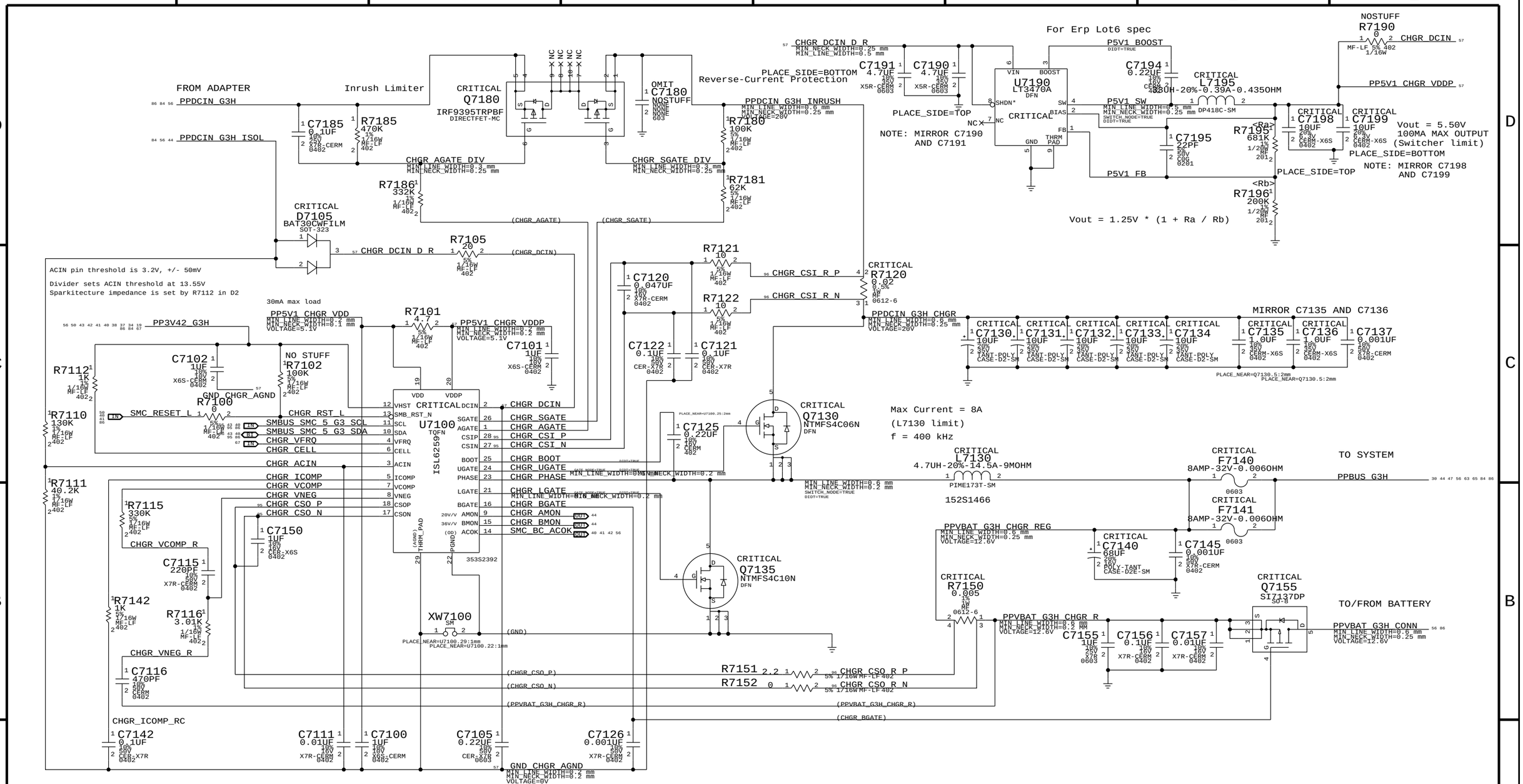

SYNC_MASTER=CLEAN X305 SYNC_DATE=01/15/2014

PAGE TITLE
PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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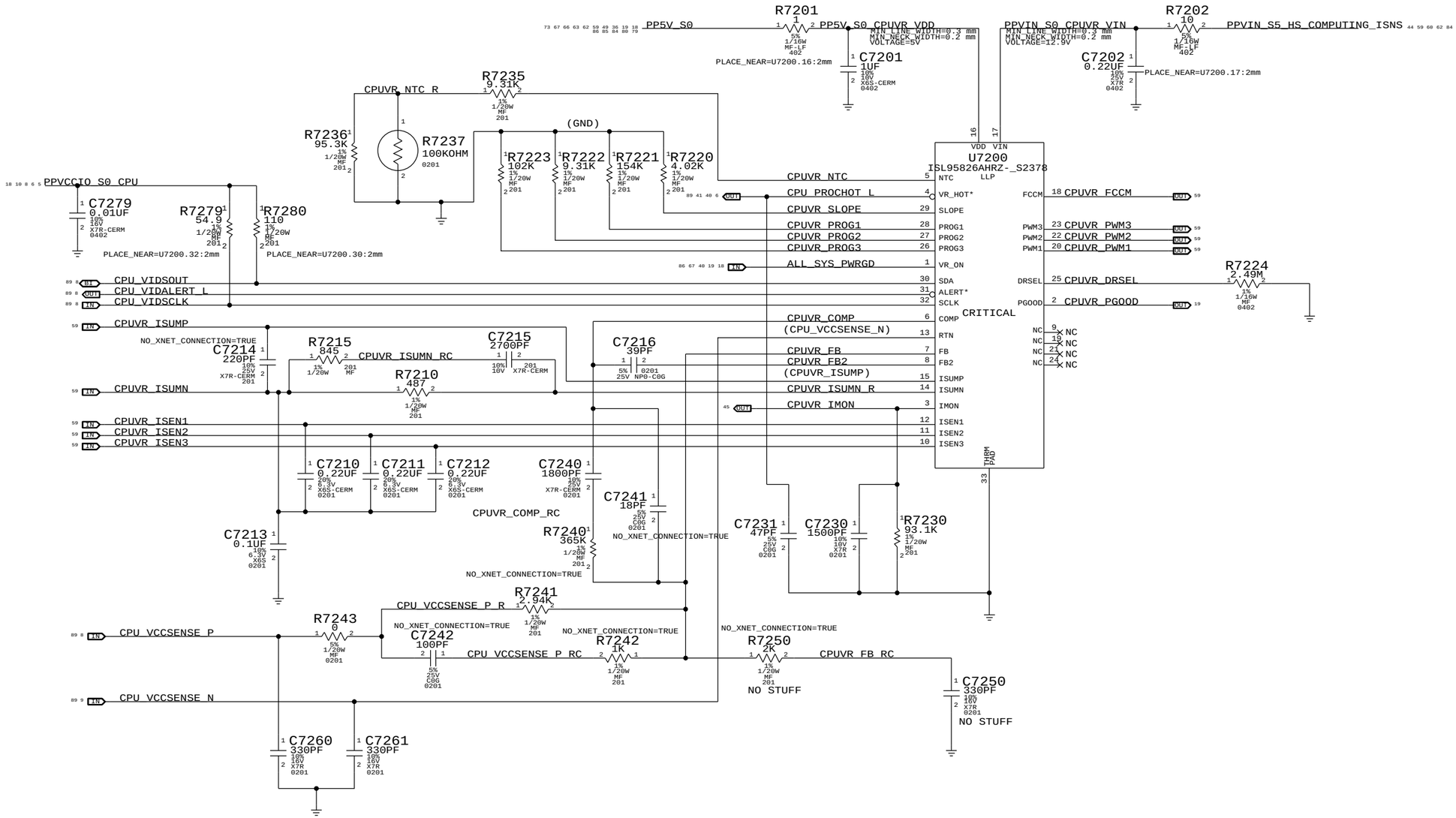

SYNC_MASTER=CLEAN_X425 SYNC_DATE=01/09/2015

PAGE TITLE
CPU VR12.5 VCC Regulator IC

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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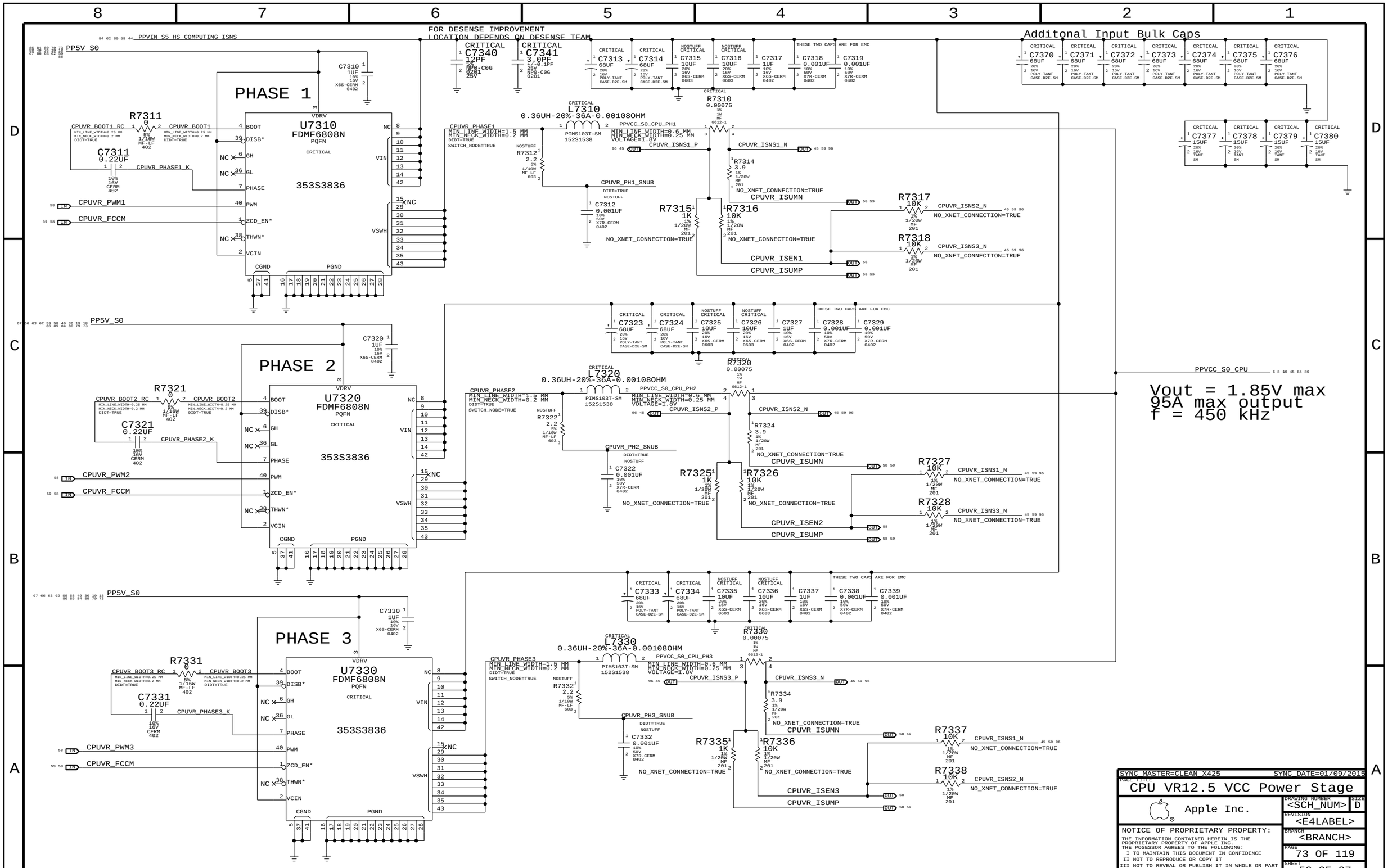
FOR DESENSE IMPROVEMENT
LOCATION DEPENDS ON DESENSE TEAM
PPVIN_S5_HS_COMPUTING_ISNS
PP5V_S0
PHASE 1
U7310
FDMF6808N
PQFN
CRITICAL
353S3836
R7311
0
C7311
0.22UF
CPUVR_BOOT1_RC
CPUVR_BOOT1
CPUVR_PHASE1_K
CPUVR_PWM1
CPUVR_FCCM
C7310
1UF
C7340
12PF
C7341
3.0PF
L7310
0.36UH-20%-36A-0.001080HM
PIMS103T-SM
152S1538
CPUVR_PHASE1
PPVCC_S0_CPU_PH1
R7310
0.00075
R7312
2.2
CPUVR_PH1_SNUB
C7312
0.001UF
R7314
3.9
NO_XNET_CONNECTION=TRUE
CPUVR_ISUMN
R7315
1K
R7316
10K
CPUVR_ISEN1
CPUVR_ISUMP
R7317
10K
CPUVR_ISNS2_N
R7318
10K
CPUVR_ISNS3_N
CPUVR_ISNS1_P
CPUVR_ISNS1_N
Additonal Input Bulk Caps
C7370
68UF
C7371
68UF
C7372
68UF
C7373
68UF
C7374
68UF
C7375
68UF
C7376
68UF
C7377
15UF
C7378
15UF
C7379
15UF
C7380
15UF
PHASE 2
U7320
FDMF6808N
PQFN
CRITICAL
353S3836
R7321
0
C7321
0.22UF
CPUVR_BOOT2_RC
CPUVR_BOOT2
CPUVR_PHASE2_K
CPUVR_PWM2
CPUVR_FCCM
C7320
1UF
C7323
68UF
C7324
68UF
C7325
10UF
C7326
10UF
C7327
1UF
C7328
0.001UF
C7329
0.001UF
L7320
0.36UH-20%-36A-0.001080HM
PIMS103T-SM
152S1538
CPUVR_PHASE2
PPVCC_S0_CPU_PH2
R7320
0.00075
R7322
2.2
CPUVR_PH2_SNUB
C7322
0.001UF
R7324
3.9
NO_XNET_CONNECTION=TRUE
CPUVR_ISUMN
R7325
1K
R7326
10K
CPUVR_ISEN2
CPUVR_ISUMP
R7327
10K
CPUVR_ISNS1_N
R7328
10K
CPUVR_ISNS3_N
CPUVR_ISNS2_P
CPUVR_ISNS2_N
PPVCC_S0_CPU
Vout = 1.85V max
95A max output
f = 450 kHz
PHASE 3
U7330
FDMF6808N
PQFN
CRITICAL
353S3836
R7331
0
C7331
0.22UF
CPUVR_BOOT3_RC
CPUVR_BOOT3
CPUVR_PHASE3_K
CPUVR_PWM3
CPUVR_FCCM
C7330
1UF
C7333
68UF
C7334
68UF
C7335
10UF
C7336
10UF
C7337
1UF
C7338
0.001UF
C7339
0.001UF
L7330
0.36UH-20%-36A-0.001080HM
PIMS103T-SM
152S1538
CPUVR_PHASE3
PPVCC_S0_CPU_PH3
R7330
0.00075
R7332
2.2
CPUVR_PH3_SNUB
C7332
0.001UF
R7334
3.9
NO_XNET_CONNECTION=TRUE
CPUVR_ISUMN
R7335
1K
R7336
10K
CPUVR_ISEN3
CPUVR_ISUMP
R7337
10K
CPUVR_ISNS1_N
R7338
10K
CPUVR_ISNS2_N
CPUVR_ISNS3_P
CPUVR_ISNS3_N
SYNC MASTER=CLEAN X425
SYNC DATE=01/09/2015
PAGE TITLE
CPU VR12.5 VCC Power Stage
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
PAGE
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SHEET
59 OF 97
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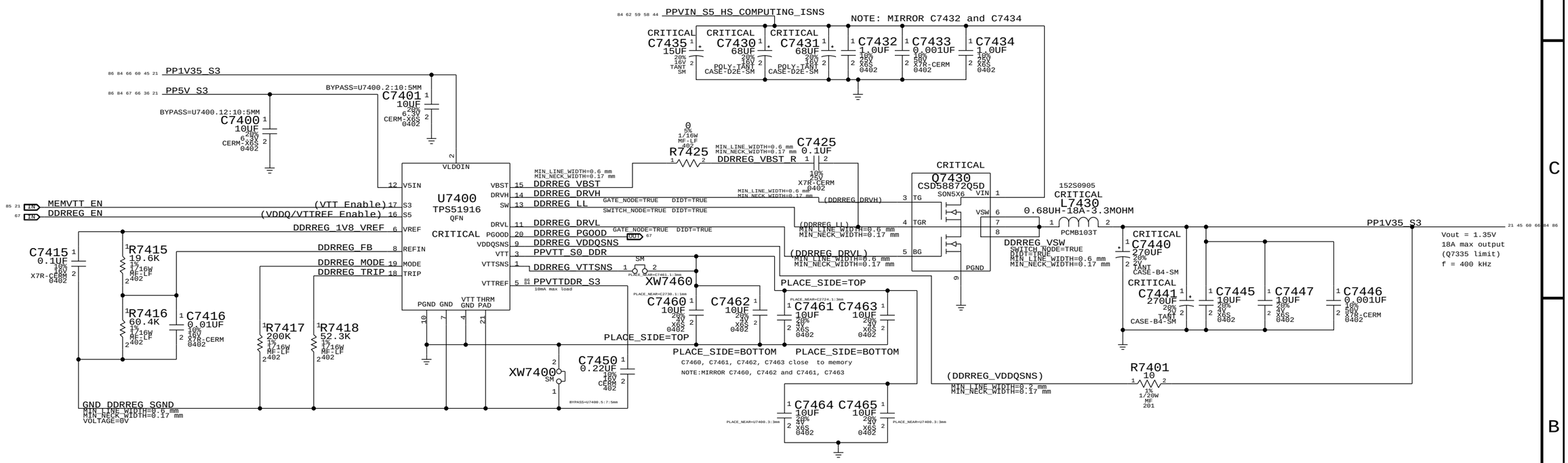
DDR3L (1V35 S3) REGULATOR



SYNC MASTER=CLEAN X305	SYNC DATE=01/15/2014
PAGE TITLE: 1.35V DDR3L SUPPLY	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
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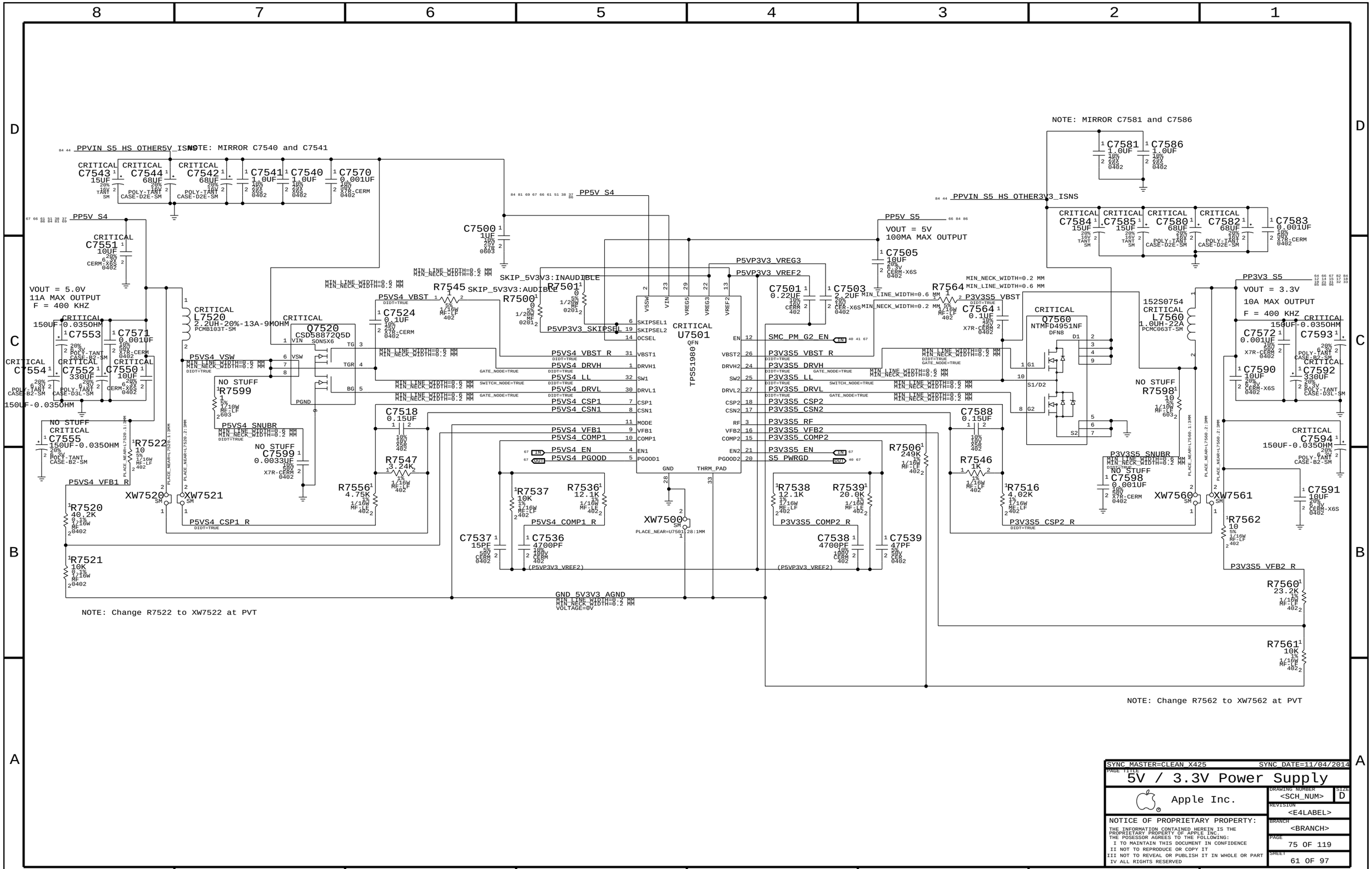
	PAGE: 74 OF 119
	SHEET: 60 OF 97


NOTE: MIRROR C7540 and C7541
NOTE: MIRROR C7581 and C7586
PPVIN S5 HS OTHER5V_ISNS
PPVIN S5 HS OTHER3V3_ISNS
PP5V S4
PP5V S5
VOUT = 5V
100MA MAX OUTPUT
PP3V3 S5
VOUT = 3.3V
10A MAX OUTPUT
F = 400 KHZ
VOUT = 5.0V
11A MAX OUTPUT
F = 400 KHZ
U7501
TPS51980
Q7520
CSD58872Q5D
Q7560
NTMFD4951NF
L7520
2.2UH-20%-13A-9MOHM
L7560
1.0UH-22A
SMC_PM_G2_EN
P3V3S5_VBST_R
P3V3S5_DRVH
P3V3S5_LL
P3V3S5_DRVL
P3V3S5_CSP2
P3V3S5_CSN2
P3V3S5_RF
P3V3S5_VFB2
P3V3S5_COMP2
P3V3S5_EN
S5_PWRGD
P5VS4_VBST
P5VS4_VSW
P5VS4_SNUBR
P5VS4_CSP1
P5VS4_CSN1
P5VS4_VFB1
P5VS4_COMP1
P5VS4_EN
P5VS4_PGOOD
P5VP3V3_VREG3
P5VP3V3_VREF2
P5VP3V3_SKIPSEL
SKIP_5V3V3:INAUDIBLE
SKIP_5V3V3:AUDIBLE
P3V3S5_SNUBR
P3V3S5_CSP2_R
P3V3S5_COMP2_R
P5VS4_CSP1_R
P5VS4_COMP1_R
P5VS4_VFB1_R
P3V3S5_VFB2_R
GND_5V3V3_AGND
NOTE: Change R7522 to XW7522 at PVT
NOTE: Change R7562 to XW7562 at PVT
SYNC MASTER=CLEAN X425
SYNC DATE=11/04/2014
PAGE TITLE
5V / 3.3V Power Supply
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
PAGE
75 OF 119
SHEET
61 OF 97
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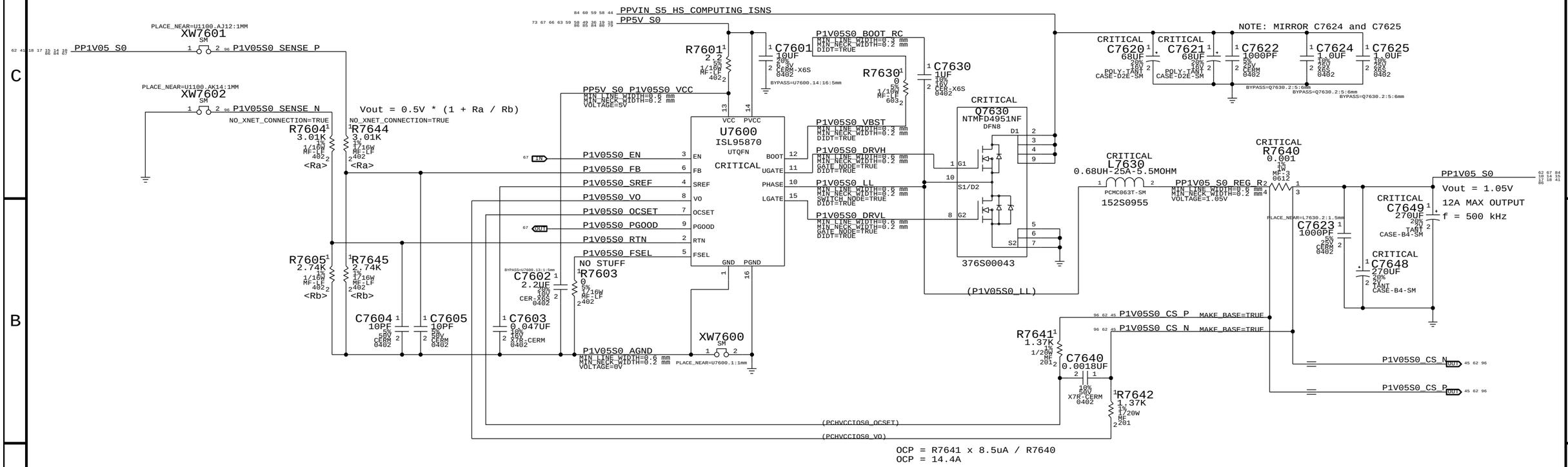
1V05 S0 REGULATOR



SYNC_MASTER=CLEAN X305 PEG SYNC_DATE=02/18/2014

PAGE TITLE
1V05V POWER SUPPLY

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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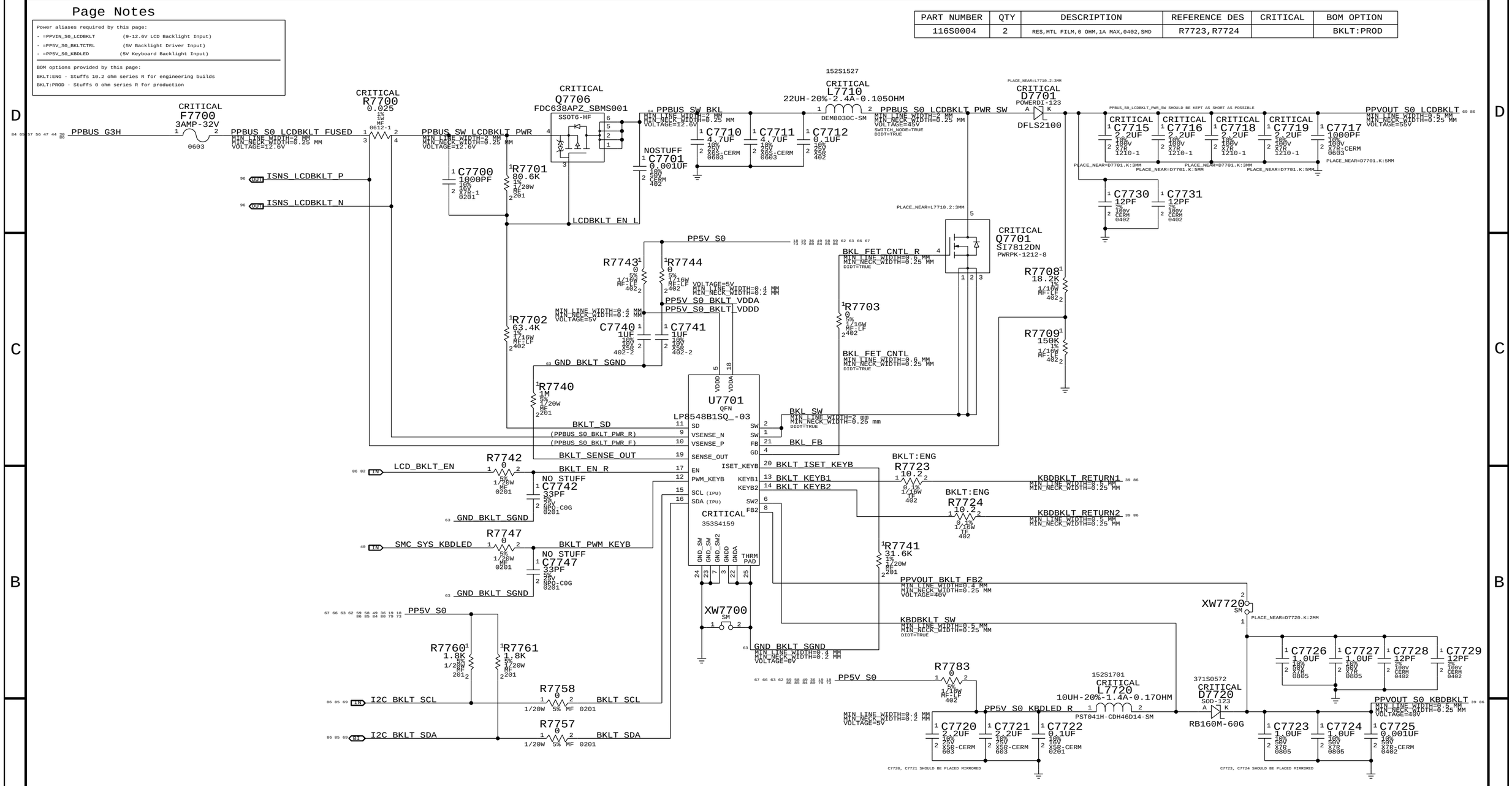
Page Notes

Power aliases required by this page:
- =PPVIN_S0_LCDBKLT (9-12.6V LCD Backlight Input)
- =PP5V_S0_BKLTCTRL (5V Backlight Driver Input)
- =PP5V_S0_KBDLED (5V Keyboard Backlight Input)

BOM options provided by this page:
BKLT:ENG - Stuffs 10.2 ohm series R for engineering builds
BKLT:PROD - Stuffs 0 ohm series R for production

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0 OHM,1A MAX,0402,SMD	R7723,R7724		BKLT:PROD



SYNC MASTER=CLEAN_X425 SYNC DATE=10/30/2014

PAGE TITLE: LCD/KBD Backlight Driver

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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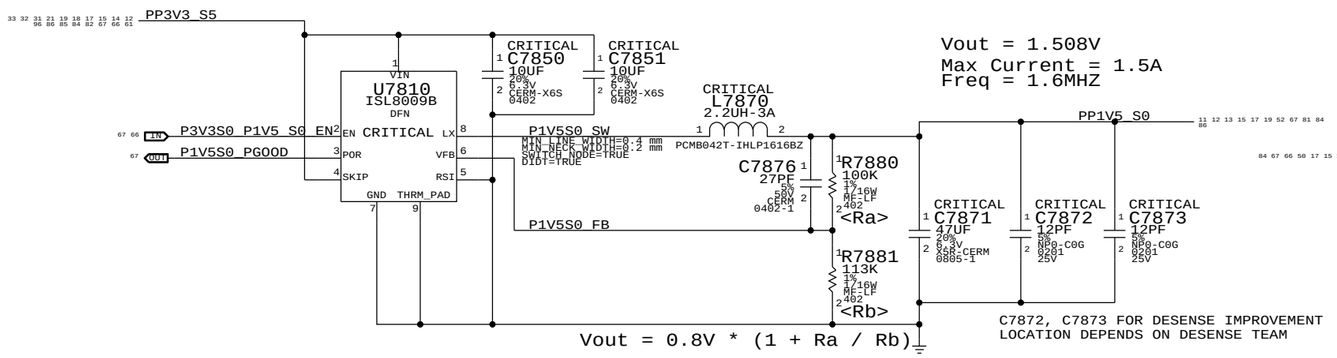
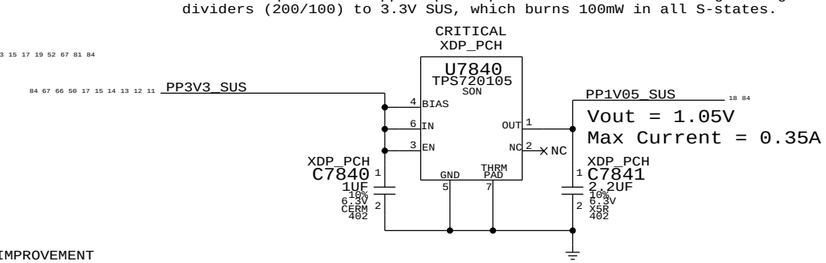
1.5V S0 Regulator



1.05V SUS LDO

Lynx Point-H requires JTAG pull-ups to be powered at 1.05V in SUS.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V SUS, which burns 100mW in all S-states.



SYNC_MASTER=CLEAN_X305 SYNC_DATE=01/15/2014

PAGE TITLE
Misc Power Supplies

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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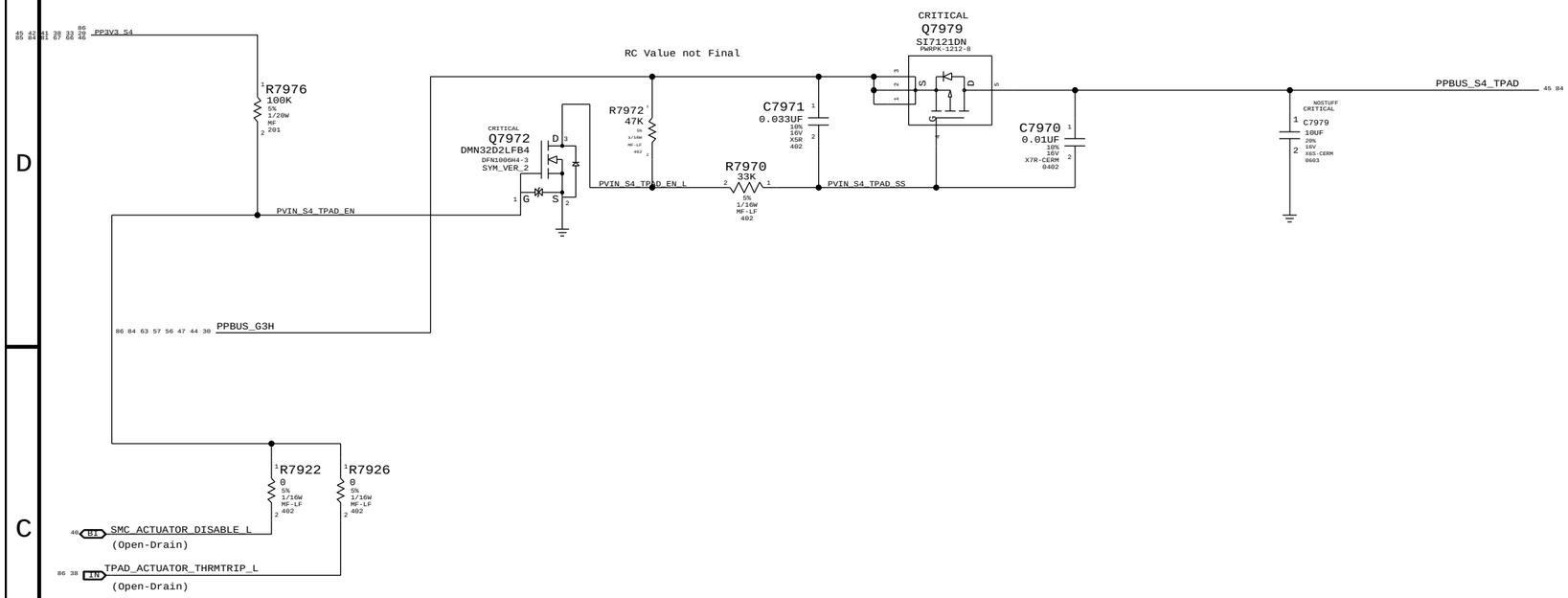

PBUS ONLY CONTROL INPUTS

SYSTEM STATE	SMC_ACTUATOR_DISABLE_L	TPAD_ACTUATOR_THRMTRIP_L	T101 POWER
G3H, S5	X	X	0 V
S4, S3, S0	Hi-Z	Hi-Z	PBUS
S4, S3, S0	0 V	X	0 V
S4, S3, S0	X	0 V	0 V

SYNC_MASTER=CLEAN_MAXWELL SYNC_DATE=07/02/2014

PAGE TITLE
X249 POWER SUPPLY

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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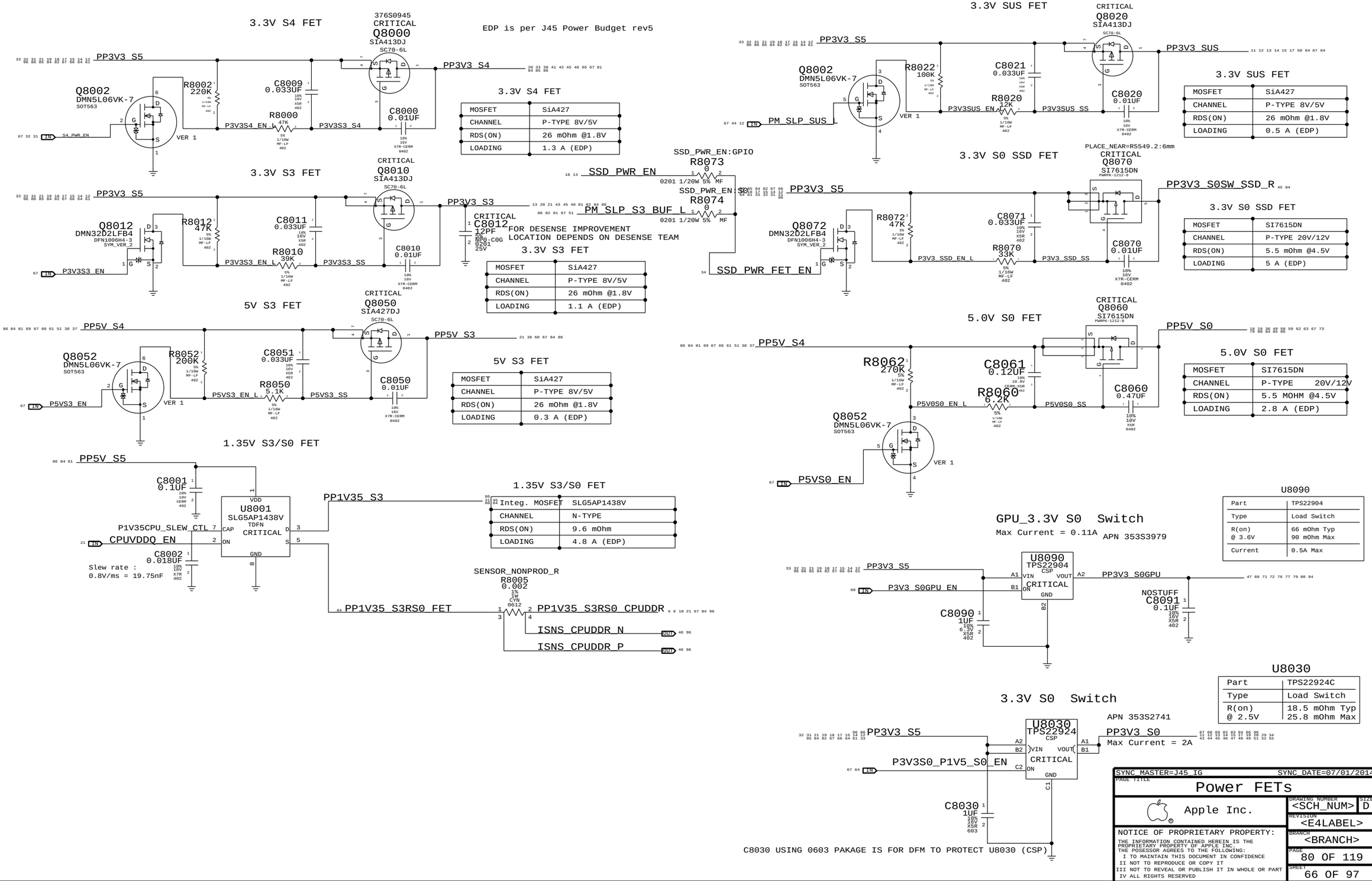

SYNC_MASTER=J45_IG SYNC_DATE=07/01/2014

PAGE TITLE

Power FETs

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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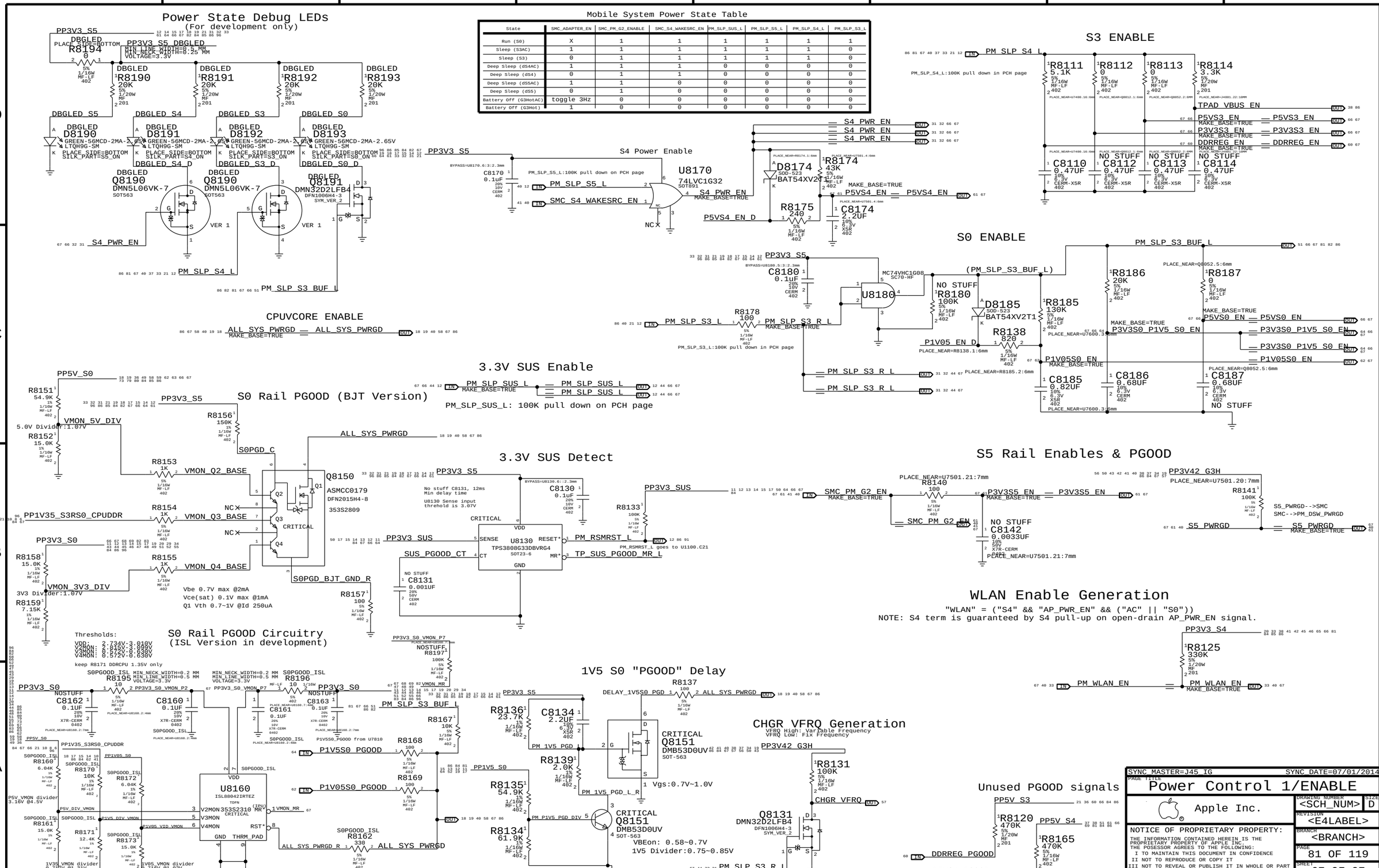
Power State Debug LEDs
(For development only)
Mobile System Power State Table
S3 ENABLE
S4 Power Enable
S0 ENABLE
CPUVCORE ENABLE
3.3V SUS Enable
S0 Rail PGOOD (BJT Version)
3.3V SUS Detect
S5 Rail Enables & PGOOD
S0 Rail PGOOD Circuitry
(ISL Version in development)
1V5 S0 "PGOOD" Delay
WLAN Enable Generation
"WLAN" = ("S4" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S4 term is guaranteed by S4 pull-up on open-drain AP_PWR_EN signal.
CHGR VFRQ Generation
Unused PGOOD signals
Power Control 1/ENABLE
Apple Inc.
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SYNC_MASTER=J45_IG
SYNC_DATE=07/01/2014
DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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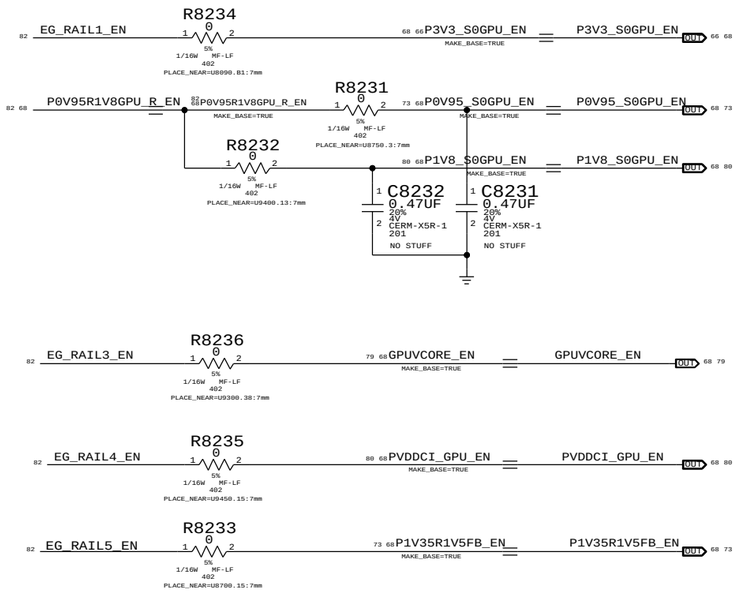
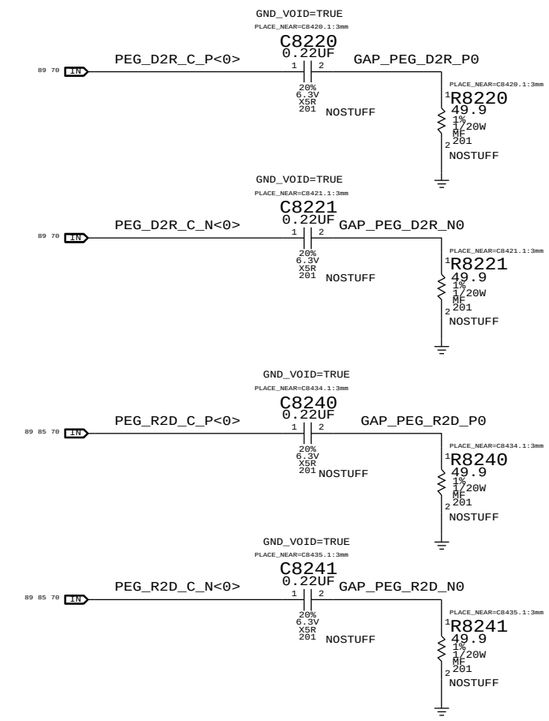
GPU Rails Power UP Sequencing

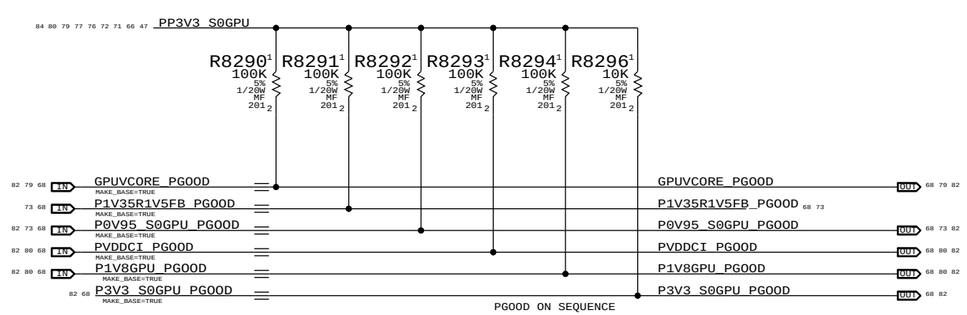
Venus GPU requires rails to come
up in the following order:
1) GPU_3.3V
2) GPU_0V95 (BIF_VDDC) & GPU_1V8 (VDD_CT)
3) GPUVCore
4) VDDCI
5) FB VRAM MVDD



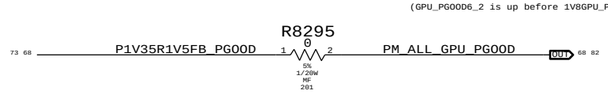
PCIE TEST STRUCTURES (FOR LAB USE)
Pending Layout. Can add more.



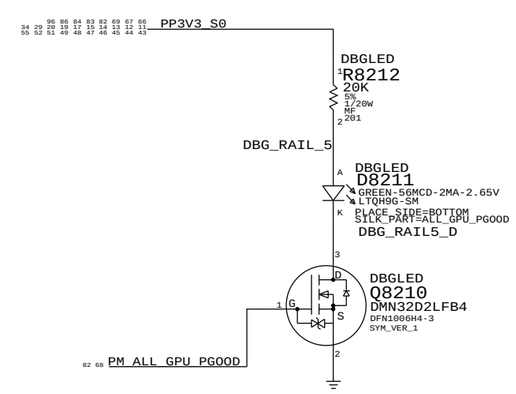
EXT GPU PWRGD Pullup



PGOOD ON SEQUENCE
1. GPU 3V3 GPU_PGOOD1
2. 0.95_S0GPU GPU_PGOOD6_2
3. 1V8_GPU GPU_PGOOD2
4. GPUVCORE GPU_PGOOD3
5. VDDCI GPU_PGOOD4
6. FB MVDD GPU_PGOOD5
(GPU_PGOOD6_2 is up before 1V8GPU_PGOOD after 3V3GPU_PGOOD)



Power State Debug LEDs
(For development only)



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SYNC_MASTER=MARY_X425G SYNC_DATE=09/11/2014
PAGE TITLE
Power Sequencing EG/PGOOD
Apple Inc.
DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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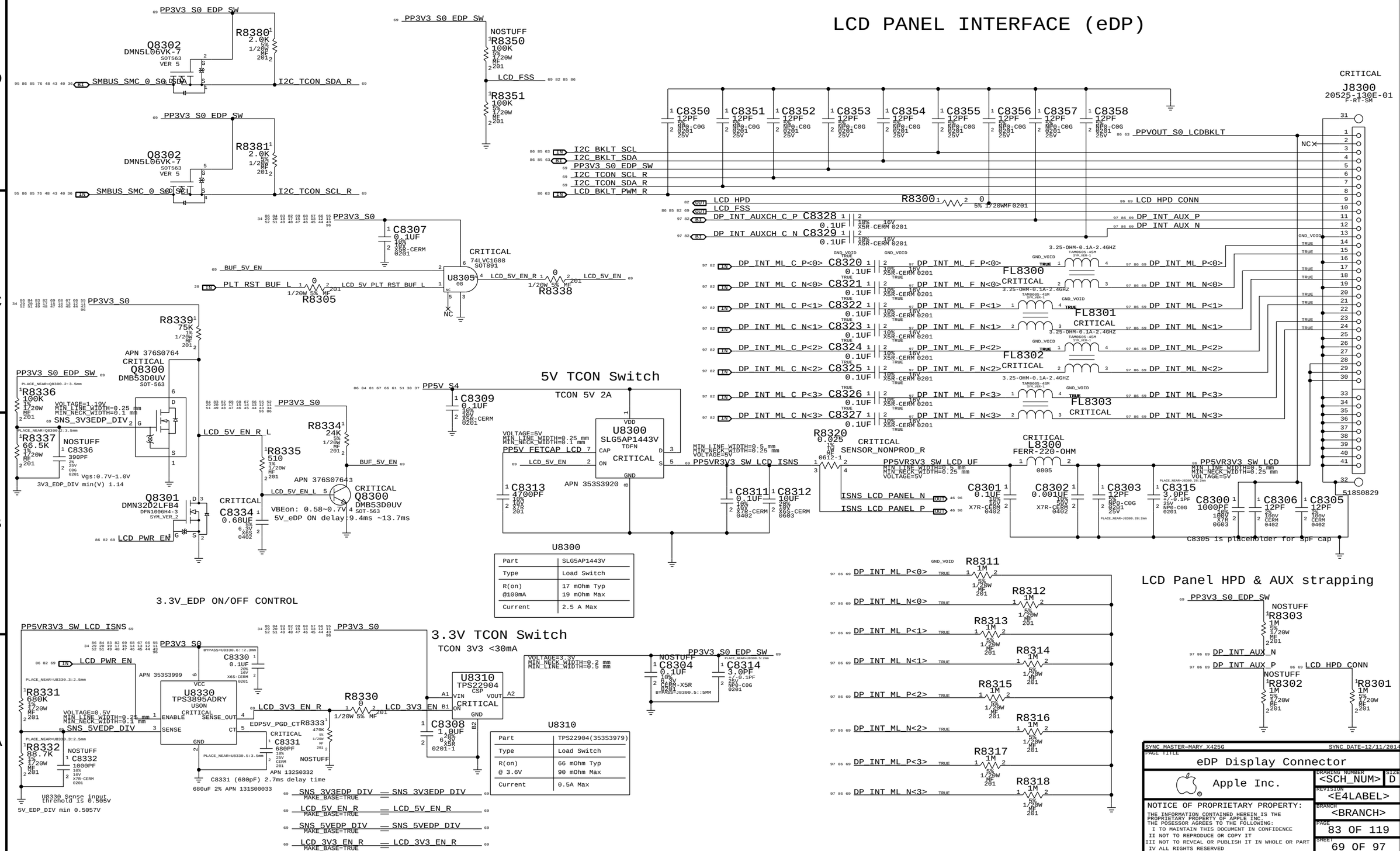
LCD PANEL INTERFACE (eDP)



SYNC_MASTER=MARY_X425G SYNC_DATE=12/11/2014

PAGE TITLE: eDP Display Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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Page Notes

Power aliases required by this page:

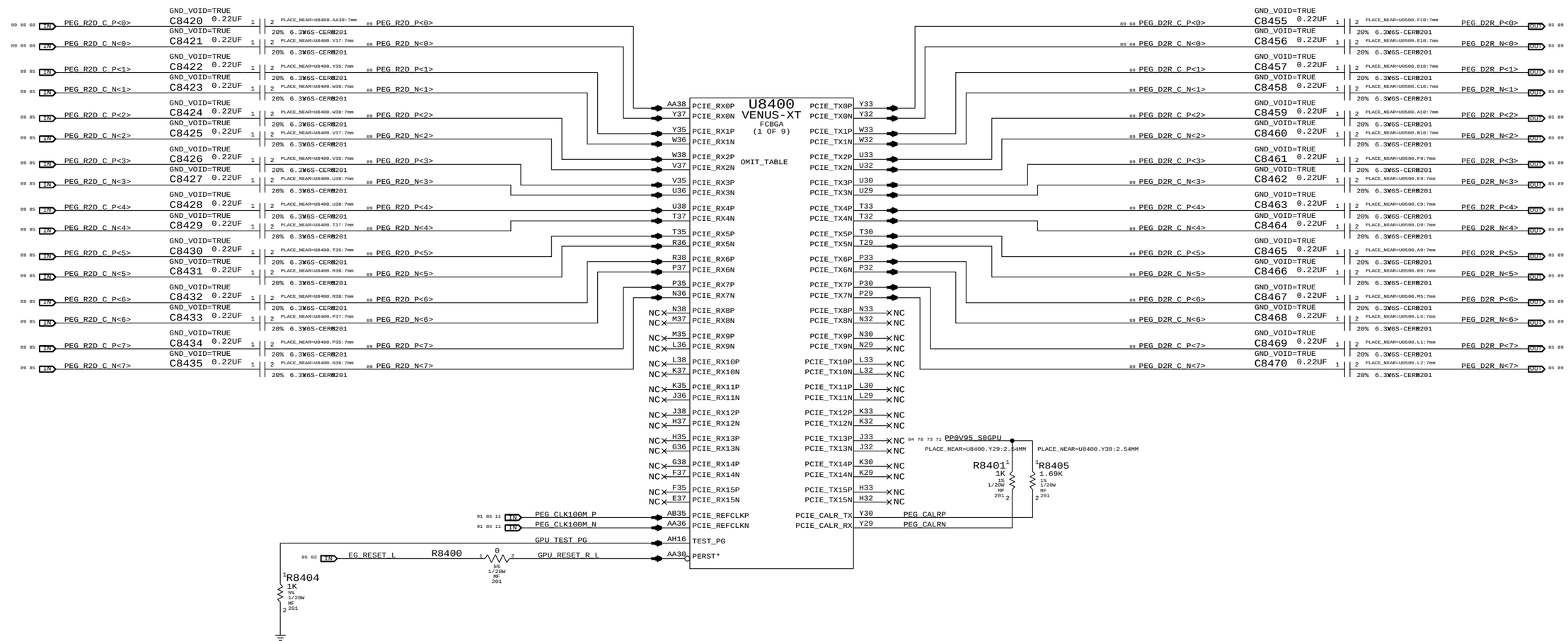
- =PPVS5_GPU_PCIE

Signal aliases required by this page:

{NONE}

BOM options provided by this page:

{NONE}



SYNC_MASTER=MARY_X425G SYNC_DATE=08/22/2014

PAGE TITLE

Venus PCI-E

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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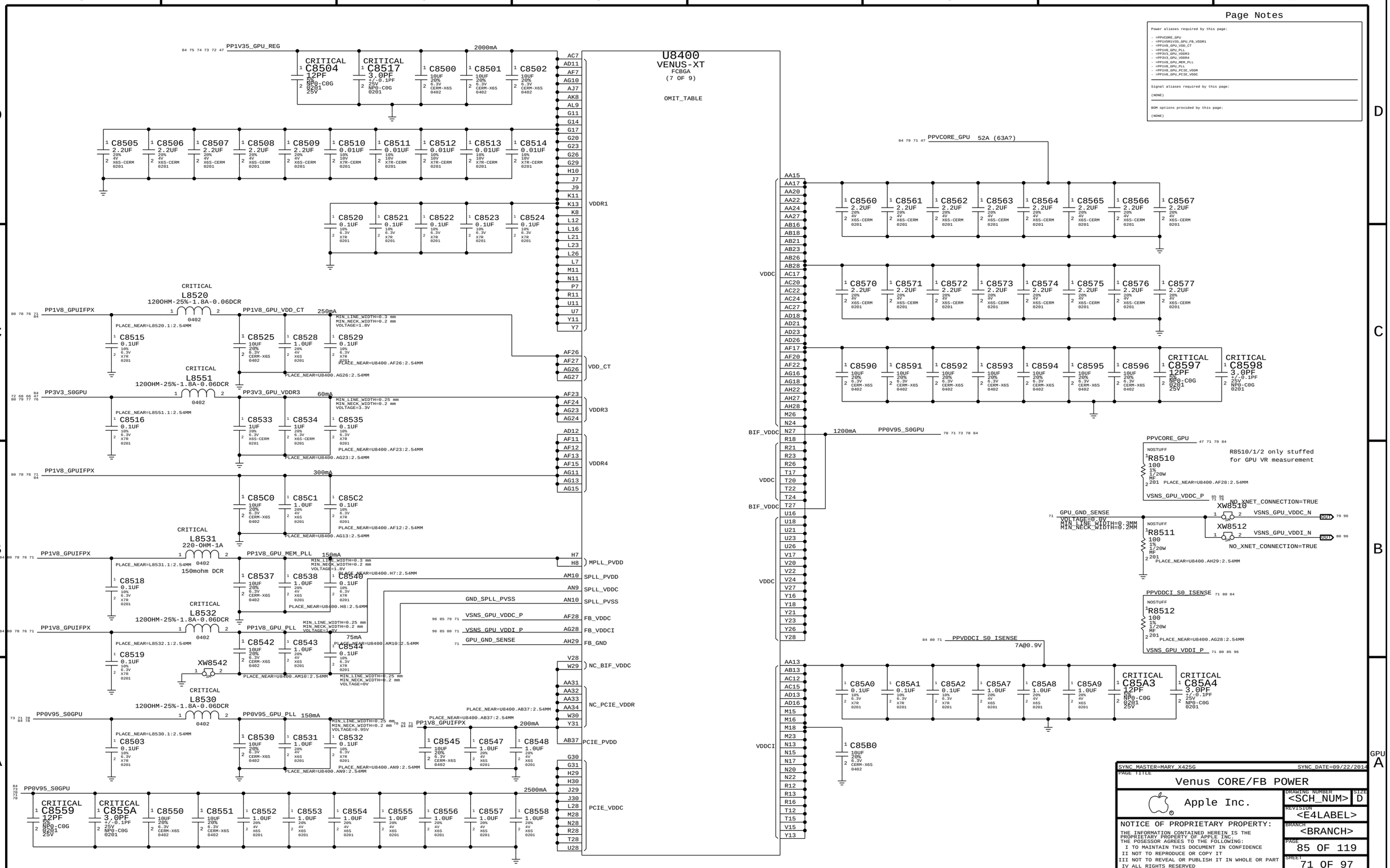
U8400
VENUS-XT
FCBGA
(7 OF 9)
OMIT_TABLE
PP1V35_GPU_REG
2000mA
CRITICAL C8504 12PF 5% NP0-C0G 0201 25V
CRITICAL C8517 3.0PF +/-0.1PF 25V NP0-C0G 0201
C8500 10UF 20% 6.3V CERM-X6S 0402
C8501 10UF 20% 6.3V CERM-X6S 0402
C8502 10UF 20% 6.3V CERM-X6S 0402
C8505 2.2UF 20% 4V X6S-CERM 0201
C8506 2.2UF 20% 4V X6S-CERM 0201
C8507 2.2UF 20% 4V X6S-CERM 0201
C8508 2.2UF 20% 4V X6S-CERM 0201
C8509 2.2UF 20% 4V X6S-CERM 0201
C8510 0.01UF 10% 10V X7R-CERM 0201
C8511 0.01UF 10% 10V X7R-CERM 0201
C8512 0.01UF 10% 10V X7R-CERM 0201
C8513 0.01UF 10% 10V X7R-CERM 0201
C8514 0.01UF 10% 10V X7R-CERM 0201
C8520 0.1UF 10% 6.3V X7R 0201
C8521 0.1UF 10% 6.3V X7R 0201
C8522 0.1UF 10% 6.3V X7R 0201
C8523 0.1UF 10% 6.3V X7R 0201
C8524 0.1UF 10% 6.3V X7R 0201
VDDR1
PP1V8_GPUIFPX
CRITICAL L8520 1200OHM-25%-1.8A-0.06DCR 0402
PP1V8_GPU_VDD_CT
250mA
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
C8515 0.1UF 10% 6.3V X7R 0201
C8525 10UF 20% 6.3V CERM-X6S 0402
C8528 1.0UF 20% 4V X6S 0201
C8529 0.1UF 10% 6.3V X7R 0201
PLACE_NEAR=U8400.AF26:2.54MM
PLACE_NEAR=U8400.AG26:2.54MM
VDD_CT
PP3V3_S0GPU
CRITICAL L8551 1200OHM-25%-1.8A-0.06DCR 0402
PP3V3_GPU_VDDR3
60mA
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
C8516 0.1UF 10% 6.3V X7R 0201
C8533 1UF 20% 6.3V X6S-CERM 0201
C8534 1UF 20% 6.3V X6S-CERM 0201
C8535 0.1UF 10% 6.3V X7R 0201
PLACE_NEAR=U8400.AF23:2.54MM
PLACE_NEAR=U8400.AG23:2.54MM
VDDR3
VDDR4
300mA
C85C0 10UF 20% 6.3V CERM-X6S 0402
C85C1 1.0UF 20% 4V X6S 0201
C85C2 0.1UF 10% 6.3V X7R 0201
PLACE_NEAR=U8400.AF12:2.54MM
PLACE_NEAR=U8400.AG13:2.54MM
CRITICAL L8531 220-OHM-1A 0402 150mohm DCR
PP1V8_GPU_MEM_PLL
150mA
C8518 0.1UF 10% 6.3V X7R 0201
C8537 10UF 20% 6.3V CERM-X6S 0402
C8538 1.0UF 20% 4V X6S 0201
C8540 0.1UF 10% 6.3V X7R 0201
PLACE_NEAR=U8400.H7:2.54MM
PLACE_NEAR=U8400.H8:2.54MM
MPLL_PVDD
SPLL_PVDD
SPLL_VDDC
SPLL_PVSS
GND_SPLL_PVSS
VSNS_GPU_VDDC_P
VSNS_GPU_VDDI_P
GPU_GND_SENSE
FB_VDDC
FB_VDDCI
FB_GND
CRITICAL L8532 1200OHM-25%-1.8A-0.06DCR 0402
PP1V8_GPU_PLL
75mA
C8519 0.1UF 10% 6.3V X7R 0201
XW8542
C8542 10UF 20% 6.3V CERM-X6S 0402
C8543 1.0UF 20% 4V X6S 0201
C8544 0.1UF 10% 6.3V X7R 0201
PLACE_NEAR=U8400.AM10:2.54MM
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0V
NC_BIF_VDDC
NC_PCIE_VDDR
CRITICAL L8530 1200OHM-25%-1.8A-0.06DCR 0402
PP0V95_S0GPU
PP0V95_GPU_PLL
150mA
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.95V
PP1V8_GPUIFPX
200mA
C8503 0.1UF 10% 6.3V X7R 0201
C8530 10UF 20% 6.3V CERM-X6S 0402
C8531 1.0UF 20% 4V X6S 0201
C8532 0.1UF 10% 6.3V X7R 0201
C8545 10UF 20% 6.3V CERM-X6S 0402
C8547 1.0UF 20% 4V X6S 0201
C8548 1.0UF 20% 4V X6S 0201
PCIE_PVDD
PCIE_VDDC
PP0V95_S0GPU
2500mA
CRITICAL C8559 12PF 5% NP0-C0G 0201 25V
CRITICAL C855A 3.0PF +/-0.1PF 25V NP0-C0G 0201
C8550 10UF 20% 6.3V CERM-X6S 0402
C8551 10UF 20% 6.3V CERM-X6S 0402
C8552 1.0UF 20% 4V X6S 0201
C8553 1.0UF 20% 4V X6S 0201
C8554 1.0UF 20% 4V X6S 0201
C8555 1.0UF 20% 4V X6S 0201
C8556 1.0UF 20% 4V X6S 0201
C8557 1.0UF 20% 4V X6S 0201
C8558 1.0UF 20% 4V X6S 0201
PPVCORE_GPU
52A (63A?)
C8560 2.2UF 20% 4V X6S-CERM 0201
C8561 2.2UF 20% 4V X6S-CERM 0201
C8562 2.2UF 20% 4V X6S-CERM 0201
C8563 2.2UF 20% 4V X6S-CERM 0201
C8564 2.2UF 20% 4V X6S-CERM 0201
C8565 2.2UF 20% 4V X6S-CERM 0201
C8566 2.2UF 20% 4V X6S-CERM 0201
C8567 2.2UF 20% 4V X6S-CERM 0201
VDDC
C8570 2.2UF 20% 4V X6S-CERM 0201
C8571 2.2UF 20% 4V X6S-CERM 0201
C8572 2.2UF 20% 4V X6S-CERM 0201
C8573 2.2UF 20% 4V X6S-CERM 0201
C8574 2.2UF 20% 4V X6S-CERM 0201
C8575 2.2UF 20% 4V X6S-CERM 0201
C8576 2.2UF 20% 4V X6S-CERM 0201
C8577 2.2UF 20% 4V X6S-CERM 0201
C8590 10UF 20% 6.3V CERM-X6S 0402
C8591 10UF 20% 6.3V CERM-X6S 0402
C8592 10UF 20% 6.3V CERM-X6S 0402
C8593 10UF 20% 6.3V CERM-X6S 0402
C8594 10UF 20% 6.3V CERM-X6S 0402
C8595 10UF 20% 6.3V CERM-X6S 0402
C8596 10UF 20% 6.3V CERM-X6S 0402
CRITICAL C8597 12PF 5% NP0-C0G 0201 25V
CRITICAL C8598 3.0PF +/-0.1PF 25V NP0-C0G 0201
BIF_VDDC
1200mA
PP0V95_S0GPU
PPVCORE_GPU
NOSTUFF
R8510 100 1% 1/20W MF 201
PLACE_NEAR=U8400.AF28:2.54MM
VSNS_GPU_VDDC_P
R8510/1/2 only stuffed
for GPU VR measurement
NO_XNET_CONNECTION=TRUE
XW8510
XW8512
GPU_GND_SENSE
VOLTAGE=0.0V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM
R8511 100 1% 1/20W MF 201
PLACE_NEAR=U8400.AH29:2.54MM
PPVDDCI_S0_ISENSE
R8512 100 1% 1/20W MF 201
PLACE_NEAR=U8400.AG28:2.54MM
VSNS_GPU_VDDI_P
PPVDDCI_S0_ISENSE
7A@0.9V
C85A0 0.1UF 10% 6.3V X7R 0201
C85A1 0.1UF 10% 6.3V X7R 0201
C85A2 0.1UF 10% 6.3V X7R 0201
C85A7 1.0UF 20% 4V X6S 0201
C85A8 1.0UF 20% 4V X6S 0201
C85A9 1.0UF 20% 4V X6S 0201
CRITICAL C85A3 12PF 5% NP0-C0G 0201 25V
CRITICAL C85A4 3.0PF +/-0.1PF 25V NP0-C0G 0201
VDDCI
C85B0 10UF 20% 6.3V CERM-X6S 0402
Page Notes
Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V5R1V35_GPU_FB_VDDR1
- =PP1V8_GPU_VDD_CT
- =PP1V8_GPU_PLL
- =PP3V3_GPU_VDDR3
- =PP3V3_GPU_VDDR4
- =PP1V8_GPU_MEM_PLL
- =PP1V8_GPU_PLL
- =PP1V8_GPU_PCIE_VDDR
- =PP1V8_GPU_PCIE_VDDC
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)
SYNC_MASTER=MARY_X425G
SYNC_DATE=09/22/2014
PAGE TITLE
Venus CORE/FB POWER
Apple Inc.
DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 85 OF 119
SHEET 71 OF 97
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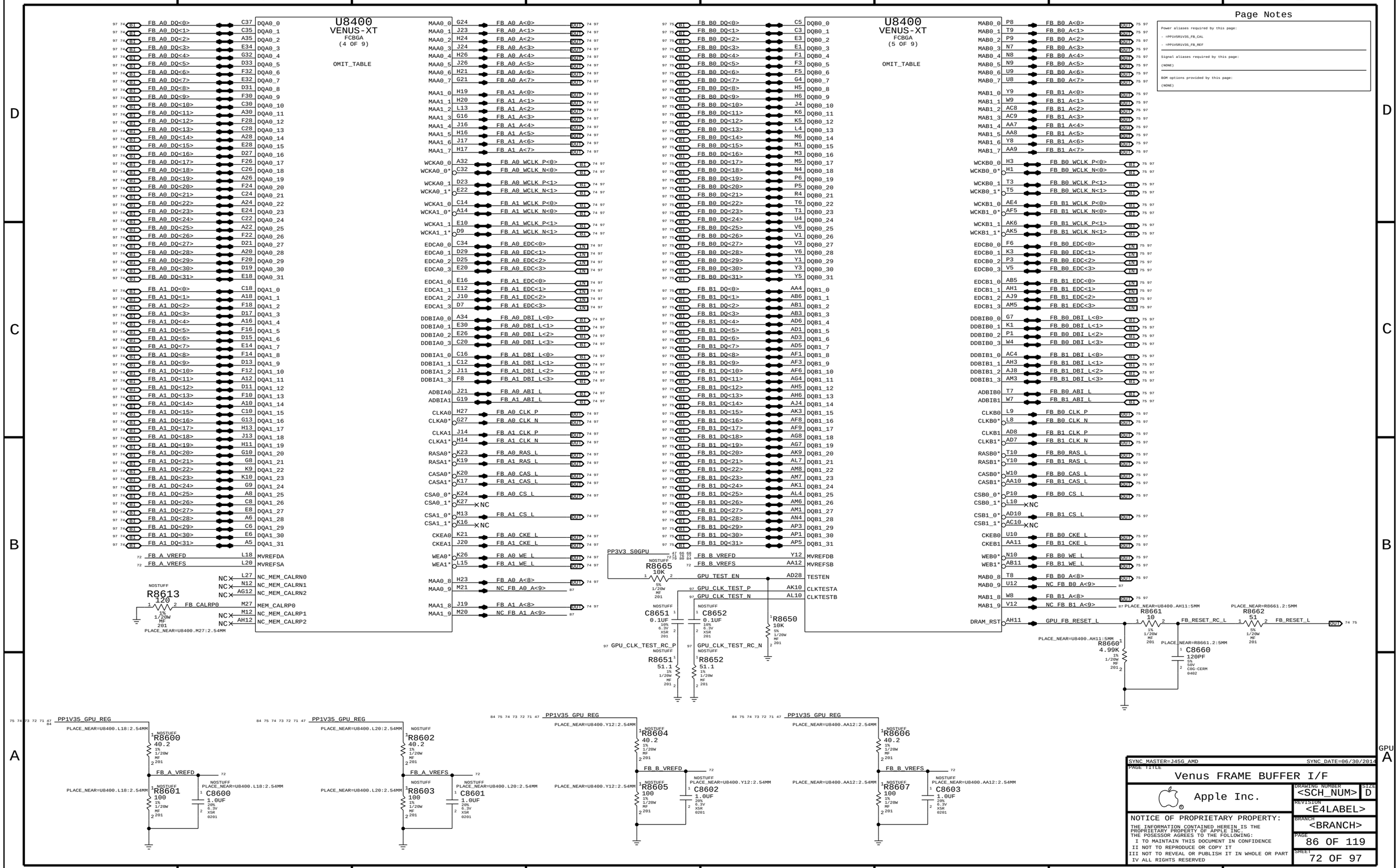
U8400
VENUS-XT
FCBGA
(4 OF 9)
OMIT_TABLE
U8400
VENUS-XT
FCBGA
(5 OF 9)
OMIT_TABLE
Page Notes
Power aliases required by this page:
- =PP1V5R1V35_FB_CAL
- =PP1V5R1V35_FB_REF
Signal aliases required by this page:
{NONE}
BOM options provided by this page:
{NONE}
R8613
120
R8665
10K
C8651
0.1UF
C8652
0.1UF
R8650
10K
R8651
51.1
R8652
51.1
R8660
4.99K
R8661
10
R8662
51
C8660
120PF
R8600
40.2
R8601
100
C8600
1.0UF
R8602
40.2
R8603
100
C8601
1.0UF
R8604
40.2
R8605
100
C8602
1.0UF
R8606
40.2
R8607
100
C8603
1.0UF
SYNC_MASTER=J45G_AMD
SYNC_DATE=06/30/2014
PAGE TITLE
Venus FRAME BUFFER I/F
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
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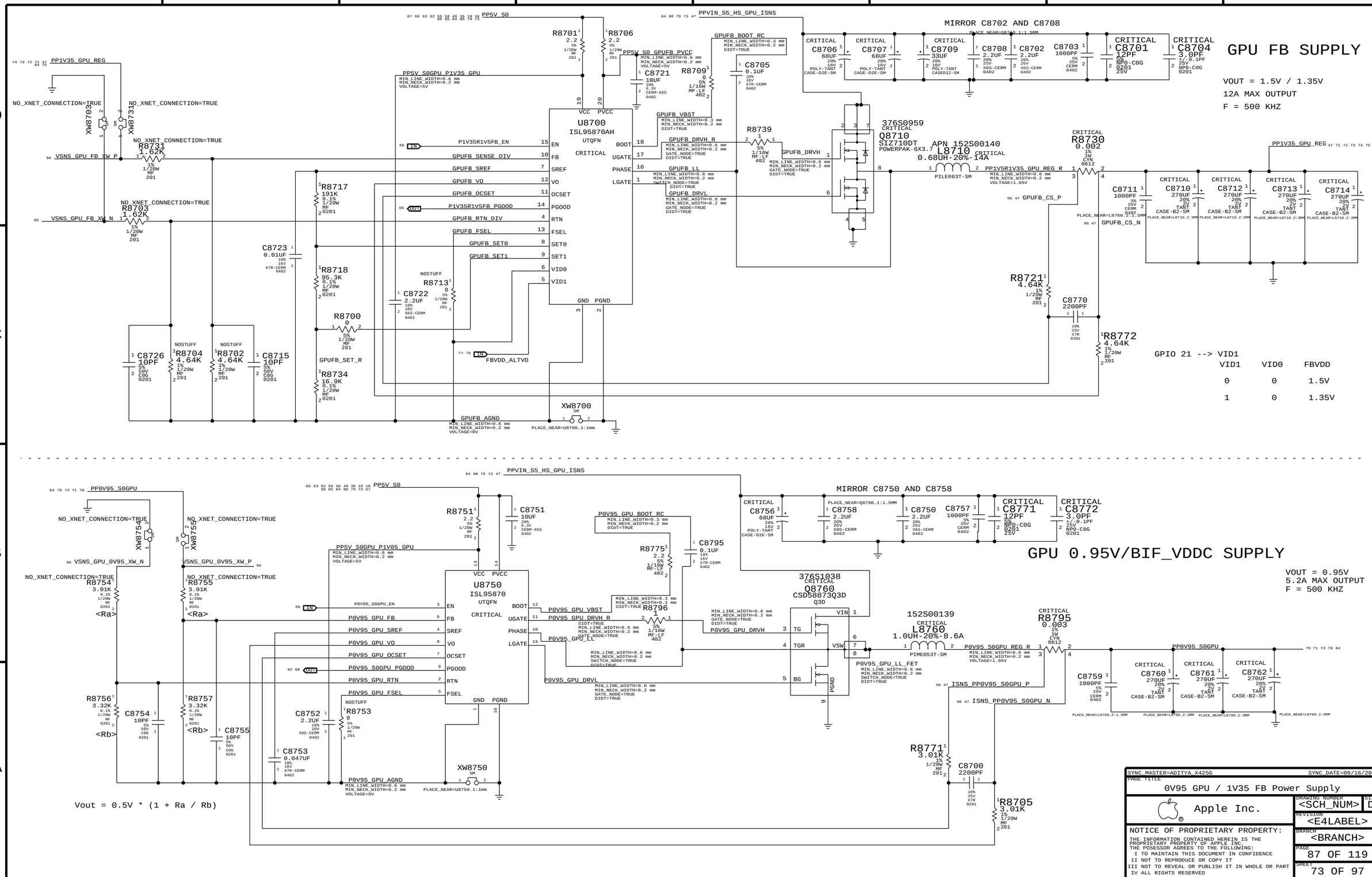
GPU FB SUPPLY
VOUT = 1.5V / 1.35V
12A MAX OUTPUT
F = 500 KHZ
MIRROR C8702 AND C8708
U8700
ISL95870AH
UTQFN
CRITICAL
Q8710
SIZ710DT
POWERPAK-6X3.7
376S0959
L8710
APN 152S00140
0.68UH-20%-14A
PIE063T-SM
R8730
0.002
PP1V5R1V35_GPU_REG_R
PP1V35_GPU_REG
PP5V_S0
PPVIN_S5_HS_GPU_ISNS
PP1V35_GPU_REG
NO_XNET_CONNECTION=TRUE
VSNS_GPU_FB_XW_P
VSNS_GPU_FB_XW_N
R8731
1.62K
R8703
1.62K
P1V35R1V5FB_EN
GPUFB_SENSE_DIV
GPUFB_SREF
GPUFB_VO
GPUFB_OCSET
P1V35R1V5FB_PGOOD
GPUFB_RTN_DIV
GPUFB_FSEL
GPUFB_SET0
GPUFB_SET1
FBVDD_ALTVO
GPUFB_SET_R
GPUFB_AGND
GPUFB_BOOT_RC
GPUFB_VBST
GPUFB_DRVH_R
GPUFB_LL
GPUFB_DRVL
GPUFB_DRVH
GPUFB_CS_P
GPUFB_CS_N
R8721
4.64K
C8770
2200PF
R8772
4.64K
GPIO 21 --> VID1
VID1 VID0 FBVDD
0 0 1.5V
1 0 1.35V
MIRROR C8750 AND C8758
U8750
ISL95870
376S1038
Q8760
CSD58873Q3D
Q3D
152S00139
L8760
1.0UH-20%-8.6A
PIME053T-SM
R8795
0.003
P0V95_S0GPU_REG_R
PP0V95_S0GPU
P0V95_GPU_LL_FET
ISNS_PP0V95_S0GPU_P
ISNS_PP0V95_S0GPU_N
R8771
3.01K
C8700
2200PF
R8705
3.01K
GPU 0.95V/BIF_VDDC SUPPLY
VOUT = 0.95V
5.2A MAX OUTPUT
F = 500 KHZ
Vout = 0.5V * (1 + Ra / Rb)
SYNC_MASTER=ADITYA_X425G
SYNC_DATE=09/16/2014
PAGE TITLE
0V95 GPU / 1V35 FB Power Supply
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
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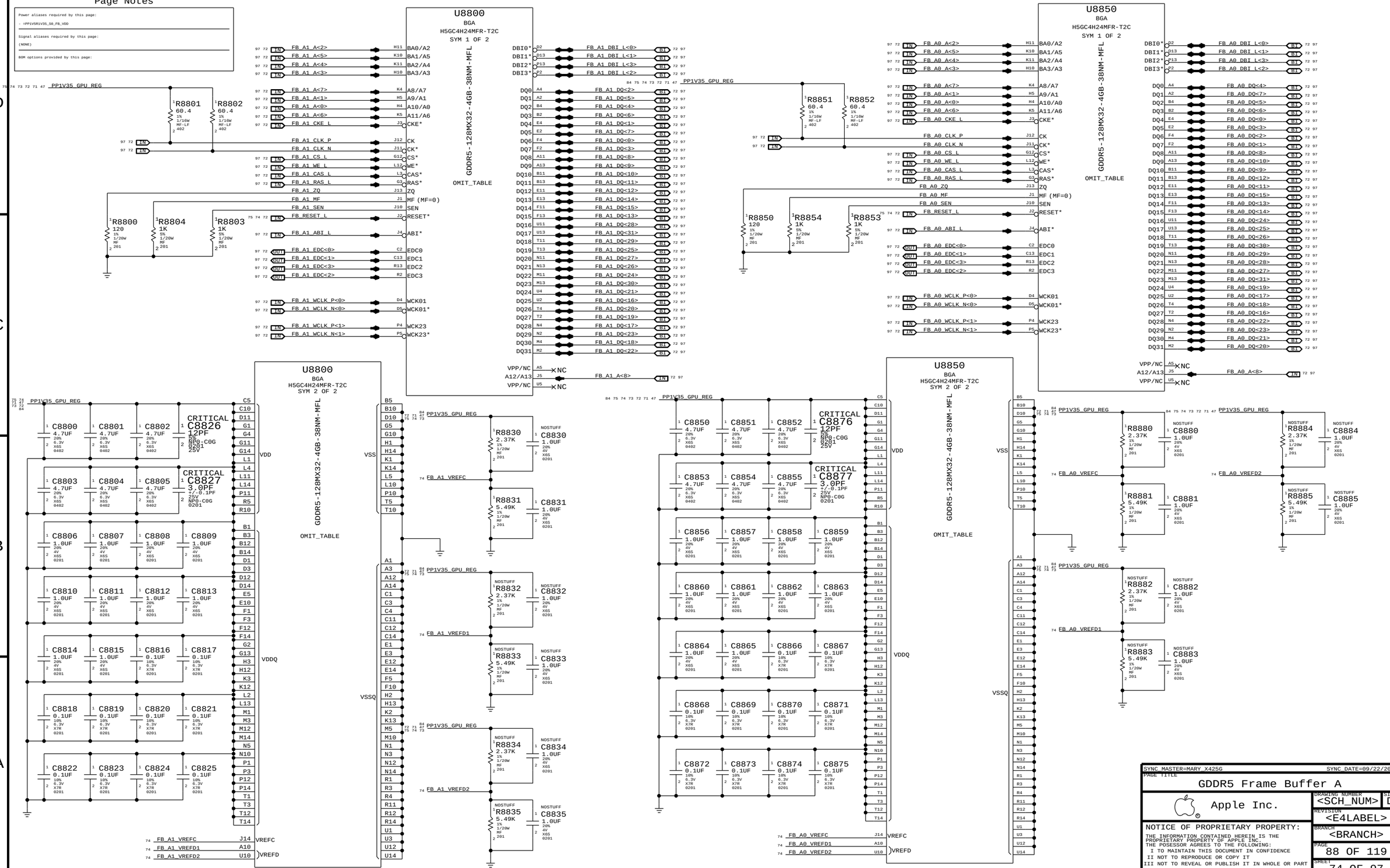
Page Notes

Power aliases required by this page:
- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:



SYNC_MASTER=MARY_X425G SYNC_DATE=09/22/2014

PAGE TITLE: GDDR5 Frame Buffer A

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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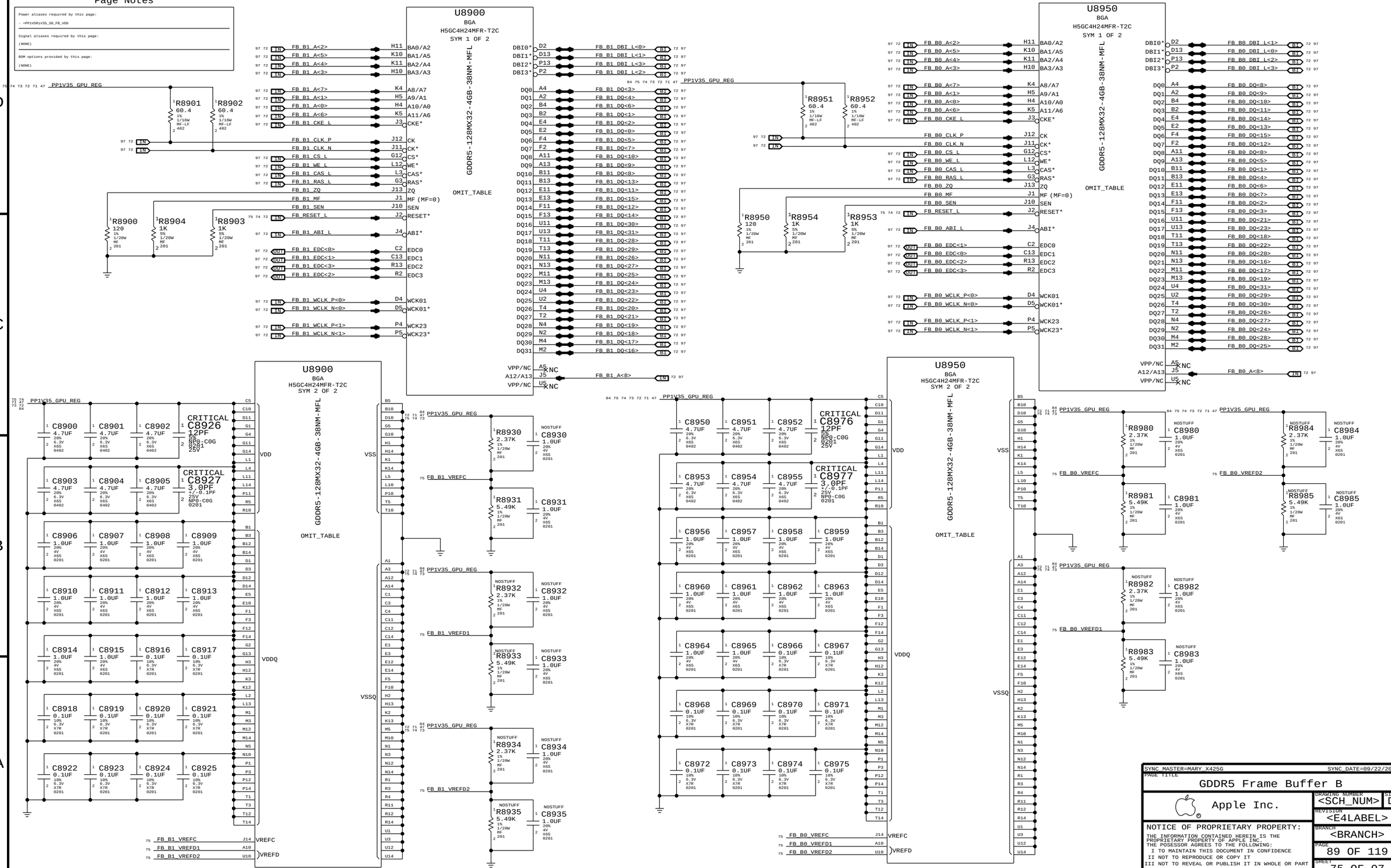
Page Notes

Power aliases required by this page:
- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC_MASTER=MARY_X425G SYNC_DATE=09/22/2014

PAGE TITLE: GDDR5 Frame Buffer B

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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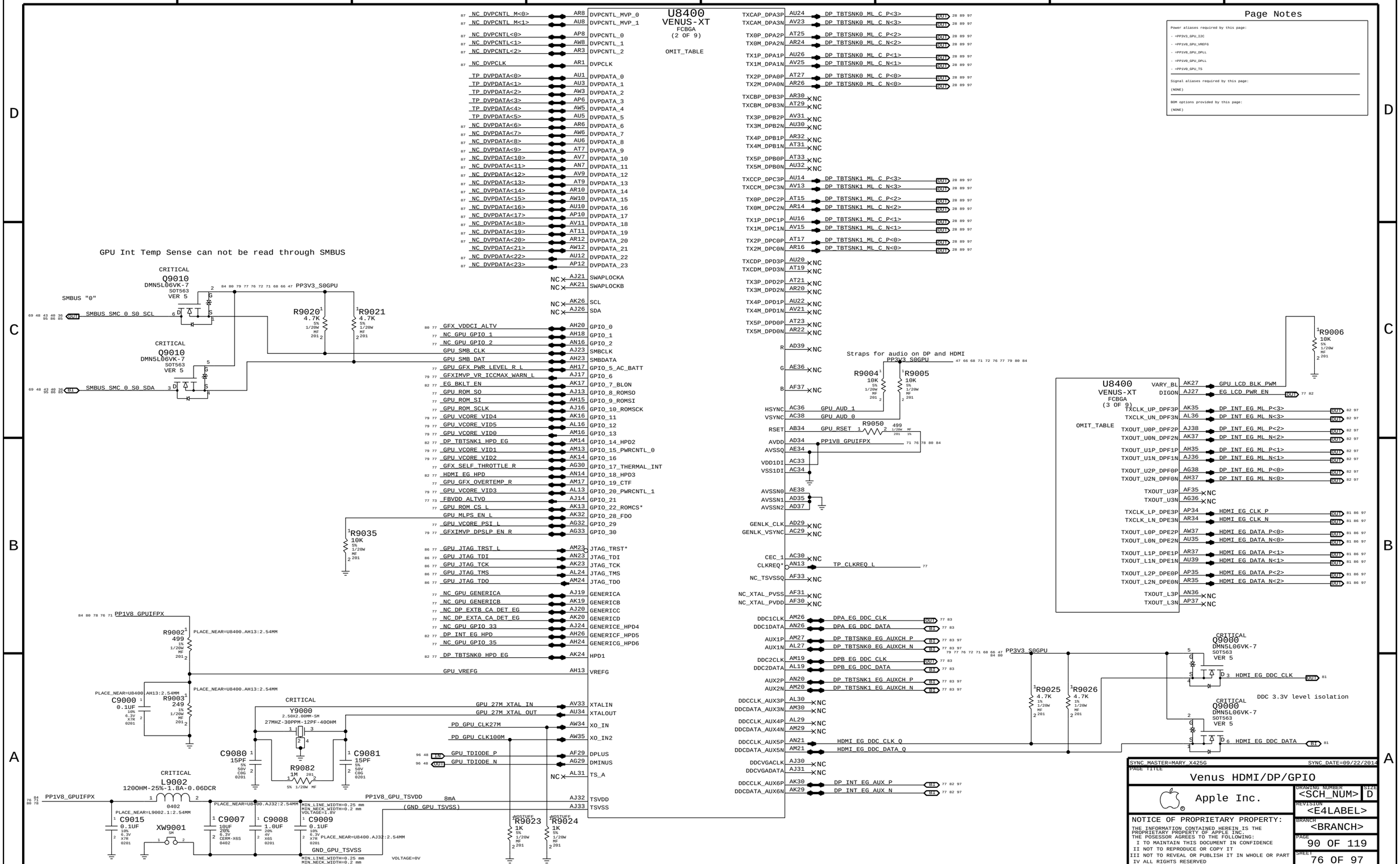
U8400
VENUS-XT
FCBGA
(2 OF 9)
OMIT_TABLE
GPU Int Temp Sense can not be read through SMBUS
Q9010
DMN5L06VK-7
SMBUS "0"
SMBUS_SMC_0_S0_SCL
SMBUS_SMC_0_S0_SDA
PP3V3_S0GPU
R9020
R9021
4.7K
R9035
10K
PP1V8_GPUIFPX
R9002
499
PLACE_NEAR=U8400.AH13:2.54MM
C9000
0.1UF
R9003
249
Y9000
27MHZ-30PPM-12PF-40OHM
C9080
15PF
R9082
1M
C9081
15PF
L9002
1200HM-25%-1.8A-0.06DCR
PP1V8_GPUIFPX
C9015
0.1UF
XW9001
C9007
10UF
C9008
1.0UF
C9009
0.1UF
GND_GPU_TSVSS
PP1V8_GPU_TSVDD
8mA
(GND_GPU_TSVSS)
R9023
1K
R9024
1K
Straps for audio on DP and HDMI
PP3V3_S0GPU
R9004
10K
R9005
10K
R9050
499
PP1V8_GPUIFPX
R9006
10K
U8400
VENUS-XT
FCBGA
(3 OF 9)
OMIT_TABLE
Q9000
DMN5L06VK-7
HDMI_EG_DDC_CLK
HDMI_EG_DDC_DATA
R9025
4.7K
R9026
4.7K
DDC 3.3V level isolation
Page Notes
Power aliases required by this page:
- =PP3V3_GPU_I2C
- =PP1V8_GPU_VREFG
- =PP1V8_GPU_DPLL
- =PP1V8_GPU_DPLL
- =PP1V8_GPU_TS
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)
SYNC MASTER=MARY_X425G
SYNC DATE=09/22/2014
PAGE TITLE
Venus HDMI/DP/GPIO
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
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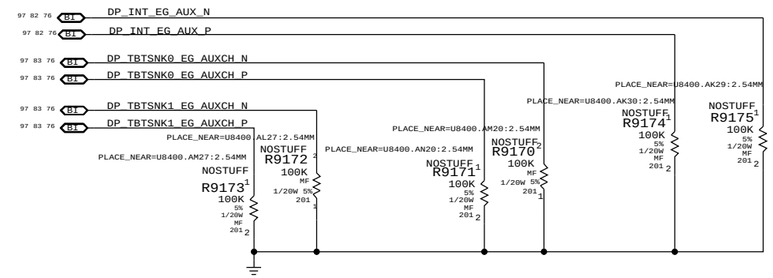
GPU GPIO TABLE

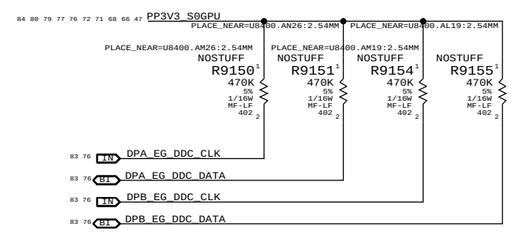
Native Func	GPIOs
GFX_VDDCI_ALTV	GFX_VDDCI_ALTV (MAKE_BASE=TRUE)
NC_GPU_GPIO_1	NC_GPU_GPIO_1 (MAKE_BASE=TRUE, NO_TEST=TRUE)
NC_GPU_GPIO_2	NC_GPU_GPIO_2 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GFX_PWR_LEVEL_R_L	GPU_GFX_PWR_LEVEL_R_L (MAKE_BASE=TRUE)
GFXIMVP_VR_ICCMAX_WARN_L	GFXIMVP_VR_ICCMAX_WARN_L (MAKE_BASE=TRUE)
EG_BKLT_EN	EG_BKLT_EN (MAKE_BASE=TRUE)
GPU_ROM_SO	GPU_ROM_SO (MAKE_BASE=TRUE)
GPU_ROM_SI	GPU_ROM_SI (MAKE_BASE=TRUE)
GPU_ROM_SCLK	GPU_ROM_SCLK (MAKE_BASE=TRUE)
GPU_VCORE_VID4	GPU_VCORE_VID4 (MAKE_BASE=TRUE)
GPU_VCORE_VID5	GPU_VCORE_VID5 (MAKE_BASE=TRUE)
GPU_VCORE_VID0	GPU_VCORE_VID0 (MAKE_BASE=TRUE)
DP_TBTSNK1_HPD_EG	DP_TBTSNK1_HPD_EG (MAKE_BASE=TRUE)
GPU_VCORE_VID1	GPU_VCORE_VID1 (MAKE_BASE=TRUE)

Native Func	GPIOs
GPU_VCORE_VID2	GPU_VCORE_VID2 (MAKE_BASE=TRUE)
GFX_SELF_THROTTLE_R	GFX_SELF_THROTTLE_R (MAKE_BASE=TRUE)
HDMI_EG_HPD	HDMI_EG_HPD (MAKE_BASE=TRUE)
GPU_GFX_OVERTEMP_R	GPU_GFX_OVERTEMP_R (MAKE_BASE=TRUE)
GPU_VCORE_VID3	GPU_VCORE_VID3 (MAKE_BASE=TRUE)
FBVDD_ALTVO	FBVDD_ALTVO (MAKE_BASE=TRUE)
GPU_ROM_CS_L	GPU_ROM_CS_L (MAKE_BASE=TRUE)
TP_CLKREQ_L	TP_CLKREQ_L (MAKE_BASE=TRUE)
NC_GPU_GENERICA	NC_GPU_GENERICA (MAKE_BASE=TRUE, NO_TEST=TRUE)
NC_GPU_GENERICB	NC_GPU_GENERICB (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_VCORE_PSI_L	GPU_VCORE_PSI_L (MAKE_BASE=TRUE)
GFXIMVP_DPSLP_EN_R	GFXIMVP_DPSLP_EN_R (MAKE_BASE=TRUE)
NC_DP_EXTB_CA_DET_EG	NC_DP_EXTB_CA_DET_EG (MAKE_BASE=TRUE, NO_TEST=TRUE)
NC_DP_EXTA_CA_DET_EG	NC_DP_EXTA_CA_DET_EG (MAKE_BASE=TRUE, NO_TEST=TRUE)
NC_GPU_GPIO_33	NC_GPU_GPIO_33 (MAKE_BASE=TRUE, NO_TEST=TRUE)
DP_INT_EG_HPD	DP_INT_EG_HPD (MAKE_BASE=TRUE)
NC_GPU_GPIO_35	NC_GPU_GPIO_35 (MAKE_BASE=TRUE, NO_TEST=TRUE)
DP_TBTSNK0_HPD_EG	DP_TBTSNK0_HPD_EG (MAKE_BASE=TRUE)

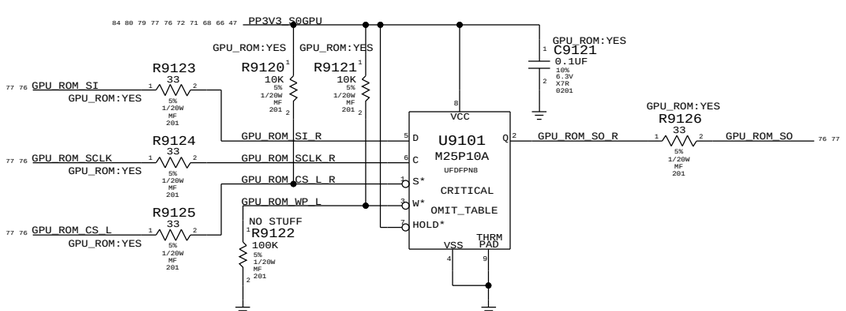
AMD AUX PD



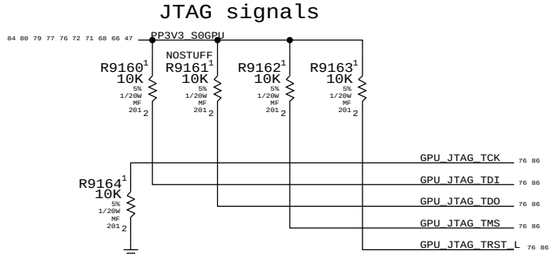
DDC PULL UP



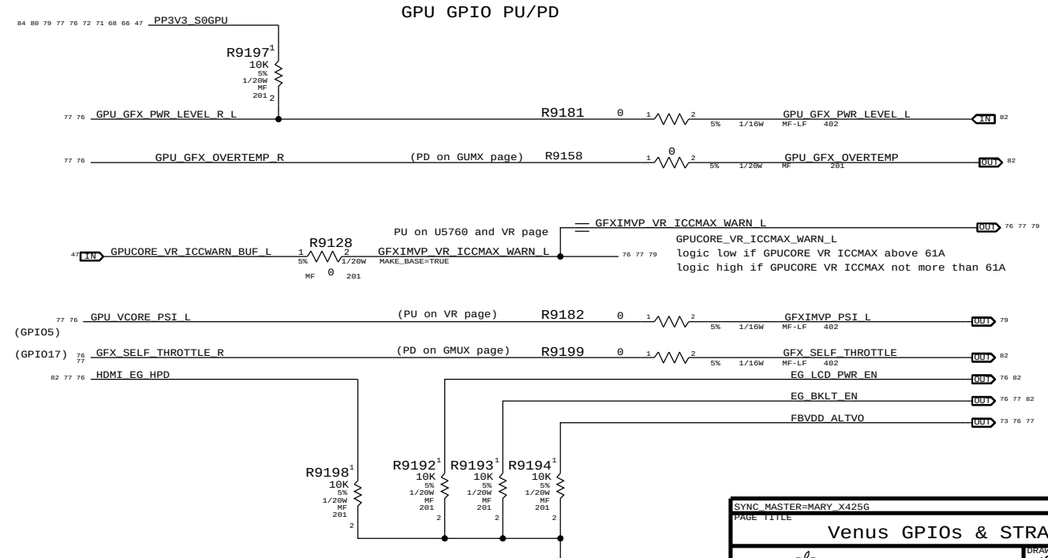
GPU ROM



JTAG signals



GPU GPIO PU/PD



SYNC_MASTER=MARY_X425G SYNC_DATE=11/07/2014

PAGE TITLE: Venus GPIOs & STRAPs

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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Page Notes

Power aliases required by this page:

- =PP1V8_GPU_DP_AB
- =PP1V8_GPU_DP_CD
- =PP1V8_GPU_DP_EF
- =PP1V0_GPU_DP_AB
- =PP1V0_GPU_DP_CD
- =PP1V0_GPU_DP_EF

Signal aliases required by this page:

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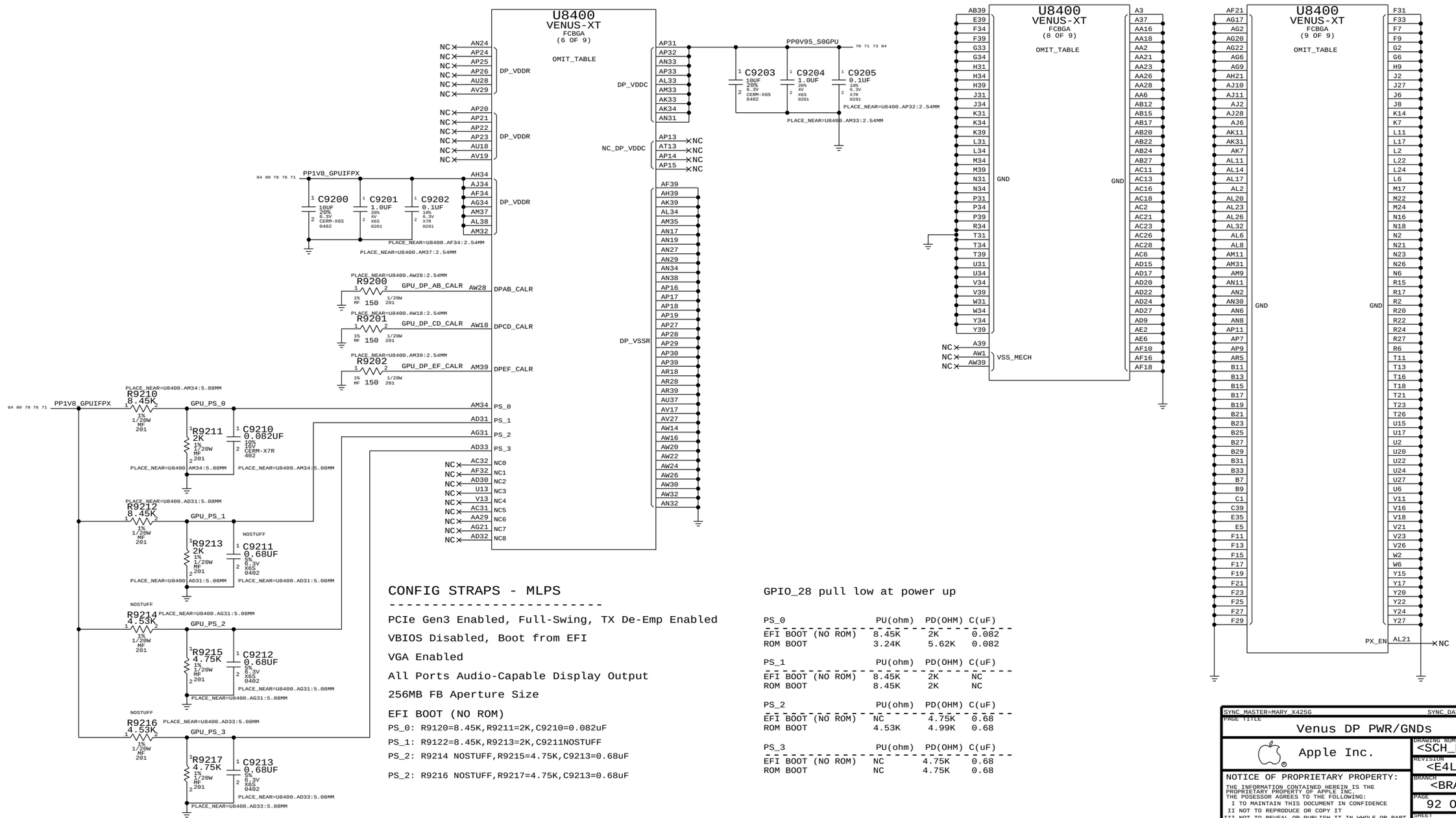
BOM options provided by this page:

(NONE)



CONFIG STRAPS - MLPS

PCIe Gen3 Enabled, Full-Swing, TX De-Emp Enabled

VBIOS Disabled, Boot from EFI

VGA Enabled

All Ports Audio-Capable Display Output

256MB FB Aperture Size

EFI BOOT (NO ROM)

PS_0: R9120=8.45K,R9211=2K,C9210=0.082uF

PS_1: R9122=8.45K,R9213=2K,C9211NOSTUFF

PS_2: R9214 NOSTUFF,R9215=4.75K,C9213=0.68uF

PS_2: R9216 NOSTUFF,R9217=4.75K,C9213=0.68uF

GPIO_28 pull low at power up

PS_0	PU(ohm)	PD(OHM)	C(uF)
EFI BOOT (NO ROM)	8.45K	2K	0.082
ROM BOOT	3.24K	5.62K	0.082

PS_1	PU(ohm)	PD(OHM)	C(uF)
EFI BOOT (NO ROM)	8.45K	2K	NC
ROM BOOT	8.45K	2K	NC

PS_2	PU(ohm)	PD(OHM)	C(uF)
EFI BOOT (NO ROM)	NC	4.75K	0.68
ROM BOOT	4.53K	4.99K	0.68

PS_3	PU(ohm)	PD(OHM)	C(uF)
EFI BOOT (NO ROM)	NC	4.75K	0.68
ROM BOOT	NC	4.75K	0.68

SYNC_MASTER=MARY_X425G SYNC_DATE=09/22/2014

PAGE TITLE: Venus DP PWR/GNDs

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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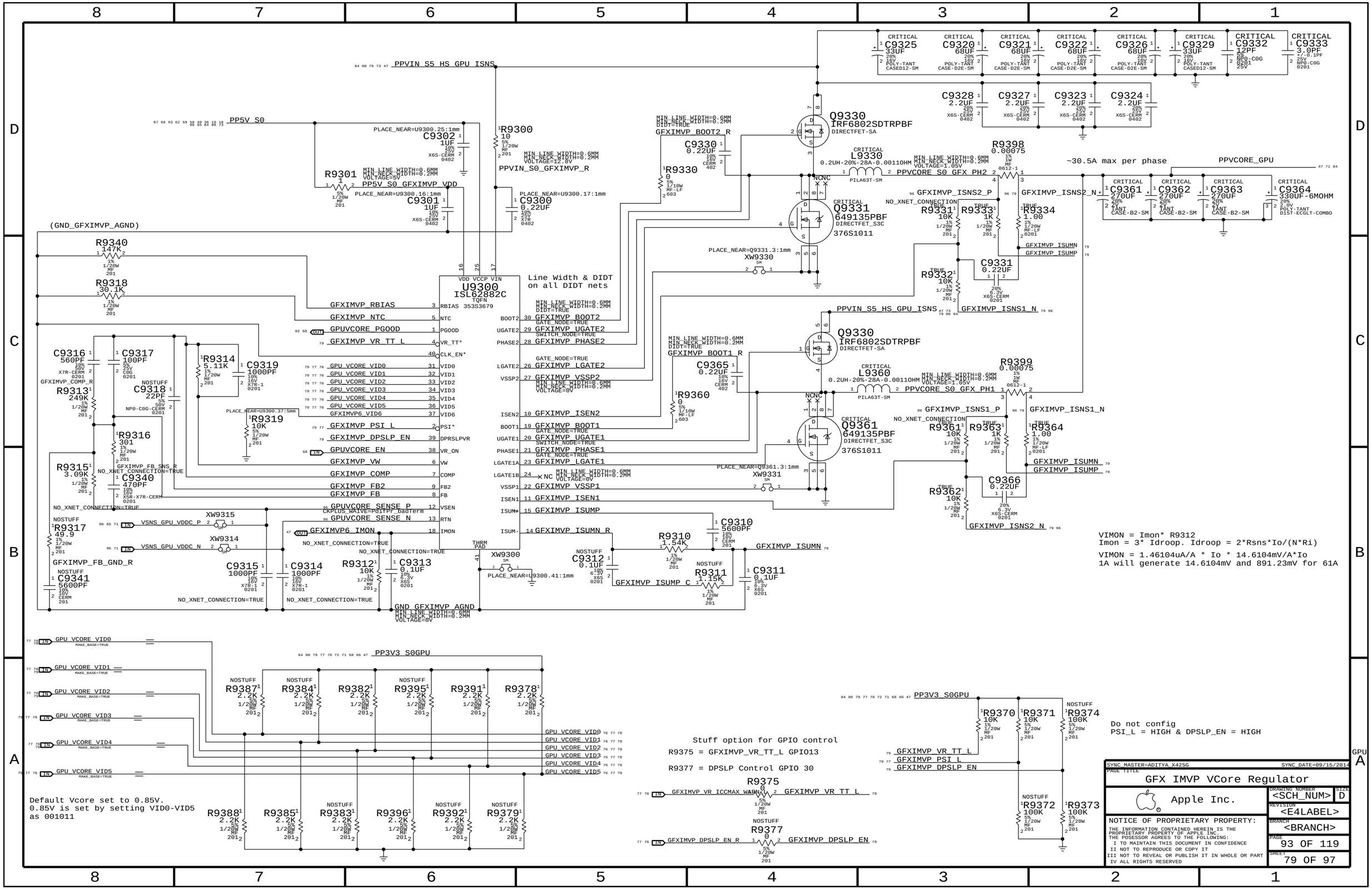
PPVIN S5 HS GPU ISNS
PP5V S0
(GND_GFXIMVP_AGND)
U9300
ISL62882C
TQFN
Q9330
IRF6802SDTRPBF
DIRECTFET-SA
Q9331
649135PBF
DIRECTFET_S3C
376S1011
Q9361
L9330
L9360
PPVCORE_GPU
~30.5A max per phase
PPVCORE S0 GFX PH2
PPVCORE S0 GFX PH1
Line Width & DIDT on all DIDT nets
GFXIMVP_BOOT2_R
GFXIMVP_BOOT1_R
PPVIN_S0_GFXIMVP_R
PP5V S0 GFXIMVP VDD
GND GFXIMVP AGND
GFXIMVP_FB_GND_R
GFXIMVP_ISNS2_P
GFXIMVP_ISNS2_N
GFXIMVP_ISNS1_P
GFXIMVP_ISNS1_N
GFXIMVP_ISUMN
GFXIMVP_ISUMP
GFXIMVP_ISUMP_C
GFXIMVP_ISUMN_R
GFXIMVP_ISNS2_N
VIMON = Imon* R9312
Imon = 3* Idroop. Idroop = 2*Rsns*Io/(N*Ri)
VIMON = 1.46104uA/A * Io * 14.6104mV/A*Io
1A will generate 14.6104mV and 891.23mV for 61A
PP3V3_S0GPU
Default Vcore set to 0.85V.
0.85V is set by setting VID0-VID5
as 001011
Stuff option for GPIO control
R9375 = GFXIMVP_VR_TT_L GPIO13
R9377 = DPSLP Control GPIO 30
Do not config
PSI_L = HIGH & DPSLP_EN = HIGH
GFX IMVP VCore Regulator
Apple Inc.
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DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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GPU VDDCI REGULATOR

VOUT = 0.9V
7A MAX OUTPUT
F = 500 KHZ

Note:
Regulator requires a minimum load to prevent noise in the audio frequencies

VSNS_GPU_VDDI_P
VSNS_GPU_VDDI_N
XW9470 SM PLACE_NEAR=U8400.AH28:5mm
XW9471 SM PLACE_NEAR=U8400.AG28:5mm
GPU_VDDCI_SENSE_XW_N NO_XNET_CONNECTION=TRUE
GPU_VDDCI_SENSE_XW_P NO_XNET_CONNECTION=TRUE
R9470 2.8K 0.1% 1/20W MF 0201
R9471 2.8K 0.1% 1/20W MF 0201
PP5V_S0
R9405 10 5% 1/20W MF 201
R9406 2.2 5% 1/20W MF 201
VOLTAGE=5V MIN_NECK_WIDTH=0.2 MM MIN_LINE_WIDTH=0.4 MM
PP5V_VDDCI_VCC
PP5V_VDDCI_PVCC
C9403 1UF 10% 10V CERAMIC 0402
C9404 2.2UF 10% 10V X6S-CERM 0402
AGND_GPU_VDDCI
R9407 2.2 5% 1/10W MF-LF 402
REG_BOOT_GPU_VDDCI_RC
C9405 0.1UF 10% 10V X7R-CERM 0402
MIN_NECK_WIDTH=0.2 mm MIN_LINE_WIDTH=0.6 mm DIDT=TRUE
REG_BOOT_GPU_VDDCI
U9450 ISL95870AH UTQFN CRITICAL
VCC PVCC EN FB SREF VO OCSET PGOOD RTN FSEL SET0 SET1 VID0 VID1 BOOT UGATE PHASE LGATE GND PGND
PVDDCI_GPU_EN
REG_GPU_VDDCI_FB
REG_GPU_VDDCI_SREF
REG_GPU_VDDCI_VO
REG_GPU_VDDCI_OCSET
PVDDCI_PGOOD
REG_GPU_VDDCI_RTN
REG_GPU_VDDCI_FSEL
REG_GPU_VDDCI_SET0
REG_GPU_VDDCI_SET1
C9490 0.033UF 10% 16V X5R 402
R9474 17.4K 0.1% 1/20W MF 0201
C9470 10PF 5% 50V C0G 0201
R9472 4.02K 0.1% 1/20W MF 0201
R9473 4.02K 0.1% 1/20W MF 0201
C9485 10PF 5% 50V C0G 0201
R9475 34.8K 0.1% 1/20W MF 0201-1
NOSTUFF R9476 0 5% 1/20W MF 0201
R9477 0 5% 1/20W MF 0201
REG_GPU_VDDCI_SET1_R
R9478 249K 0.1% 1/20W MF 0201
Vout = 0.5 * (1 + Ra / Rb)
MIN_NECK_WIDTH=0.2 mm MIN_LINE_WIDTH=0.6 mm VOLTAGE=0V
XW9473 SM PLACE_NEAR=U9450.3:1mm
PP3V3_S0GPU
R9484 0 5% 1/20W MF 0201
NOSTUFF R9485 0 5% 1/20W MF 0201
R9483 10K 5% 1/20W MF 201
GFX_VDDCI_ALTV0
GFX_VDDCI_ALTV1
GFX_VDDCI_ALTV
R9481 10K 5% 1/20W MF 201

VID1	VID0	GPU VDDCI
1	1	0.85V
1	0	0.9V --> DEFAULT

PPVIN_S5_HS_GPU_ISNS
CRITICAL C9402 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C9406 12PF 5% 50V NP0-C0G 0201
CRITICAL C9407 3.0PF +/-0.1PF 25V NP0-C0G 0201
EMC C9409 2.2UF 20% 25V X6S-CERM 0402
EMC C9410 2.2UF 20% 25V X6S-CERM 0402
C9408 1000PF 5% 25V CERM 0402
APN376S1005 CRITICAL Q9410 CSD58873Q3D Q3D
VIN TG TGR VSW BG PGND
REG_UGATE_VDDCI_R
REG_UGATE_VDDCI
REG_PHASE_GPU_VDDCI
REG_LGATE_GPU_VDDCI
VR_PHASE_GPU_VDDCI
APN152S1822 CRITICAL L9410 1.0UH-20%-15A-0.0066OHM PIME063T-SM
VRVDDCI_R
NOSTUFF C9411 0.001UF 10% 50V X7R-CERM 0402
REG_SNUBBER_GPU_VDDCI
NOSTUFF R9409 2.2 5% 1/10W MF-LF 603
CRITICAL R9400 0.003 1% 1W CSN 0612
PPVDDCI_S0_ISENSE
C9413 1000PF 5% 25V CERM 0402
R9412 200 5% 1/16W MF-LF 402
CRITICAL C9417 10UF 20% 10V X6S-CERM 0603
CRITICAL C9418 10UF 20% 10V X6S-CERM 0603
CRITICAL C9414 270UF 20% 2V TANT CASE-B2-SM
CRITICAL C9415 270UF 20% 2V TANT CASE-B2-SM
CRITICAL C9416 270UF 20% 2V TANT CASE-B2-SM
CRITICAL C9419 270UF 20% 2V TANT CASE-B2-SM
CRITICAL C9431 270UF 20% 2V TANT CASE-B2-SM
REG_GPU_VDDCI_OCSET_R
REG_GPU_VDDCI_VO_R
XW9480 SM
XW9481 SM
VDDCIS0_CS_P
VDDCIS0_CS_N
R9410 3.92K 1% 1/20W MF 201
C9412 0.0022UF 10% 50V CERM 402
PLACE_NEAR=R9410.2:3mm
R9411 3.92K 1% 1/20W MF 201
REG_GPU_VDDCI_OCSET
REG_GPU_VDDCI_VO

1.8V S0 GPU Regulator

PPVIN_S5_HS_GPU_ISNS
CRITICAL C9432 12PF 5% 50V NP0-C0G 0201
CRITICAL C9433 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL C9420 33UF 20% 16V POLY-TANT CASED12-SM
CRITICAL C9421 2.2UF 20% 25V X6S-CERM 0402
CRITICAL C9422 2.2UF 20% 25V X6S-CERM 0402
R9420 10 5% 1/20W MF 201
PPVIN_S0GPU_1V8_RC
MIN_LINE_WIDTH=0.2 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=8.4V
P1V8_S0GPU_EN
U9400 TPS62130ARGT QFN CRITICAL 353S4283
AVIN PVIN SW VOS FB PG SS/TR EN FSW PGND AGND THRM PAD
REG_PHASE_PVDDR
MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM SWITCH_NODE=TRUE DIDT=TRUE
APN152S00137 CRITICAL L9400 1.5UH-20%-2.61A-0.0680HM PIFE32251B-SM
REG_VOS_PVDDR
REG_FB_PVDDR
P1V8GPU_PGOOD
REG_SSTR_PVDDR
R9421 10 5% 1/20W MF 201
R9422 105K 0.1% 1/20W MF 0201-1 <Ra>
R9423 82.5K 0.1% 1/20W MF 0201-1 <Rb>
C9424 4700PF 10% 16V X7R 201
C9423 0.1UF 10% 16V X6S 0402
AGND_PVDDR
MIN_NECK_WIDTH=0.2 mm MIN_LINE_WIDTH=0.6 mm VOLTAGE=0V
XW9420 SM
Vout = 0.8V * (Ra + Rb) / Rb
PP1V8_GPUIFPX
CRITICAL C9425 47UF 20% 2V POLY-TANT 0805
CRITICAL C9426 47UF 20% 2V POLY-TANT 0805
CRITICAL C9427 47UF 20% 2V POLY-TANT 0805
CRITICAL C9428 47UF 20% 2V POLY-TANT 0805
CRITICAL C9429 47UF 20% 2V POLY-TANT 0805
CRITICAL C9430 47UF 20% 2V POLY-TANT 0805

Output voltage: 1.818 V
Max peak current: 1.5A
Switching freq: 1250 kHz

SYNC_MASTER=ADITYA_X425G SYNC_DATE=09/16/2014
PAGE TITLE: VREG GPU VDDCI
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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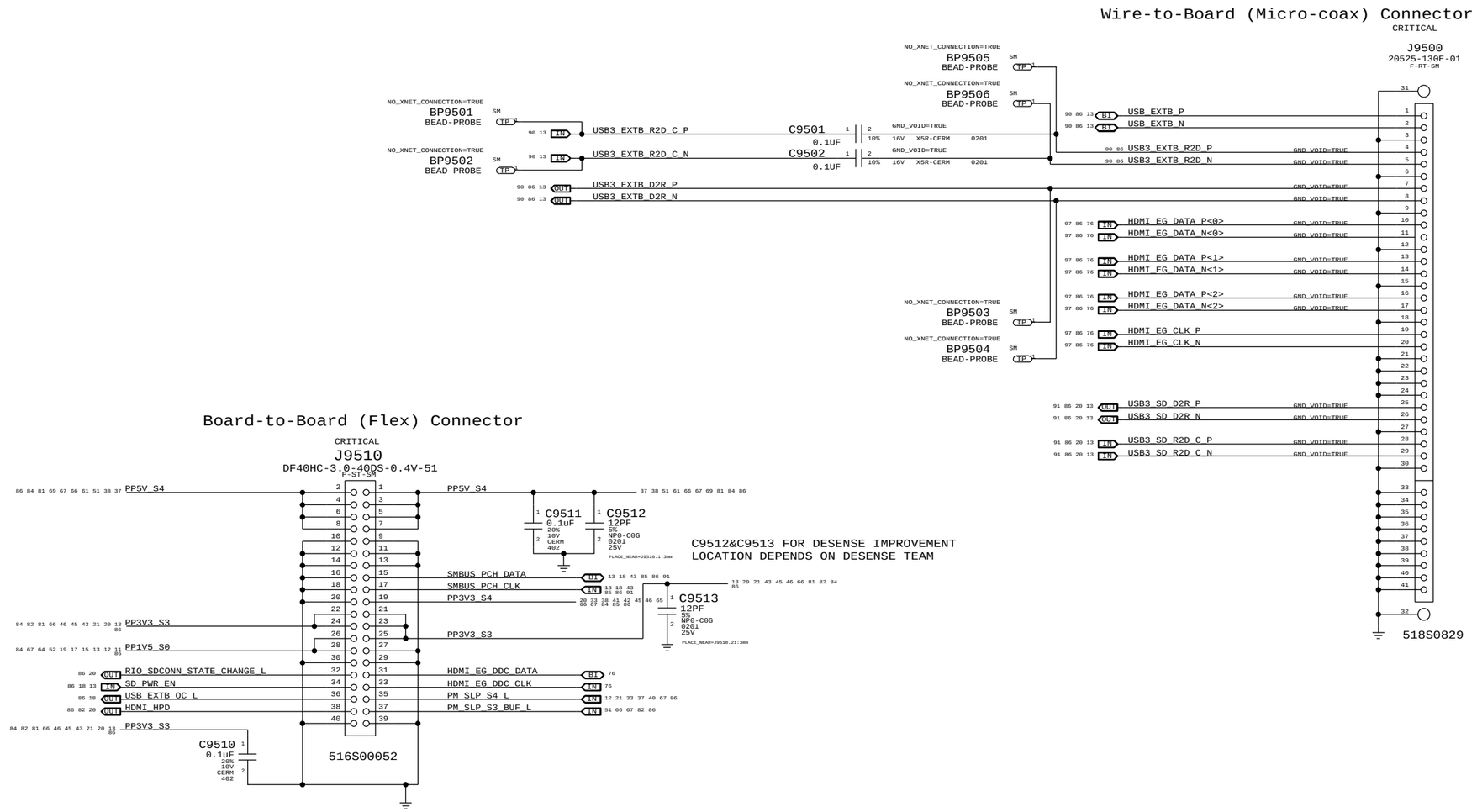

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PAGE TITLE

RIO Connectors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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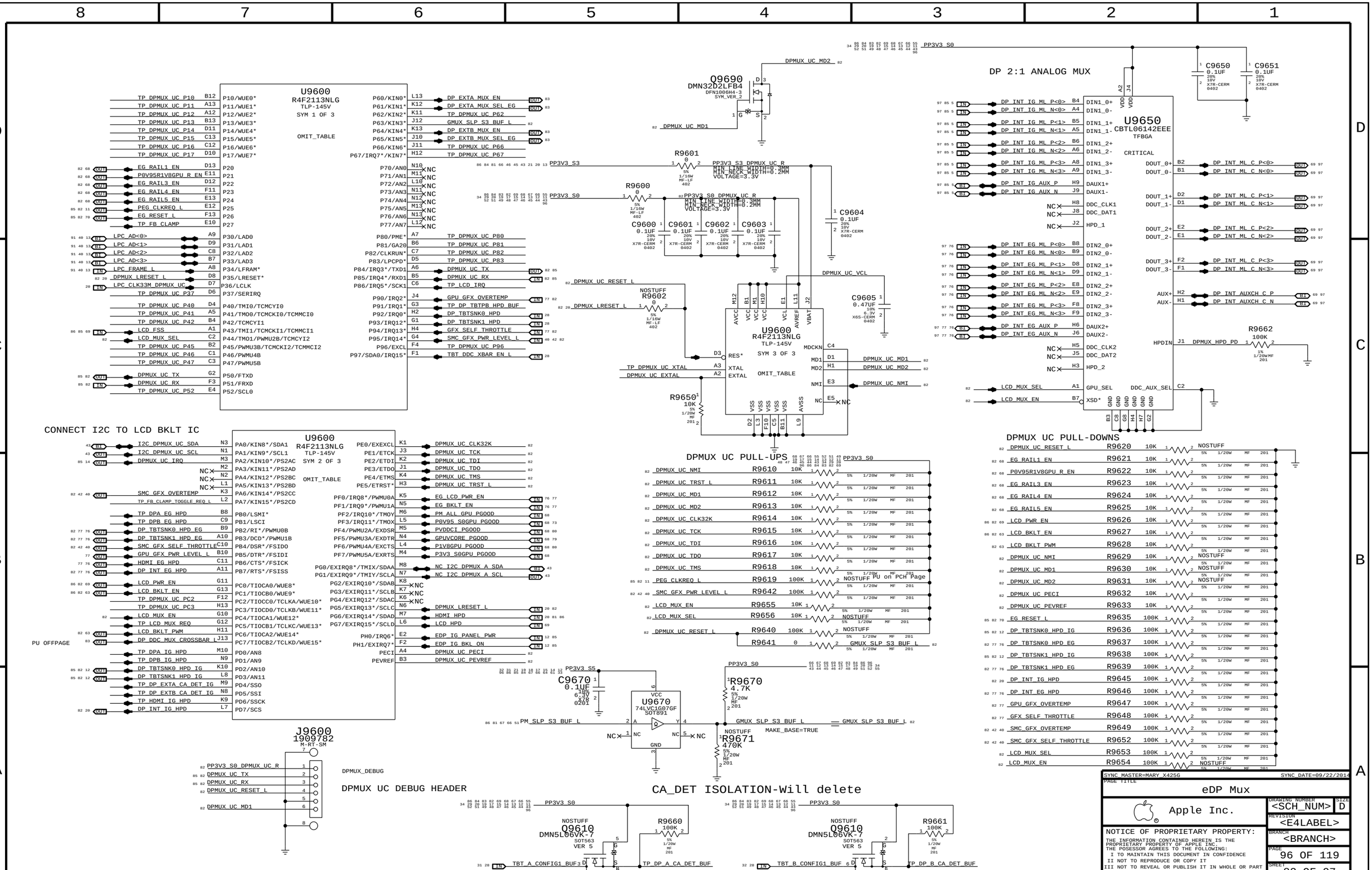
U9600
R4F2113NLG
TLP-145V
SYM 1 OF 3
OMIT_TABLE
CONNECT I2C TO LCD BKLT IC
SYM 2 OF 3
PU OFFPAGE
J9600
1909782
M-RT-SM
DPMUX_DEBUG
DPMUX UC DEBUG HEADER
Q9690
DMN32D2LFB4
DPMUX UC PULL-UPS
PU on PCH Page
SYM 3 OF 3
DP 2:1 ANALOG MUX
U9650
CBTL06142EEE
TFBGA
CRITICAL
DPMUX UC PULL-DOWNS
U9670
74LVC1G07GF
SOT891
MAKE_BASE=TRUE
CA_DET ISOLATION-Will delete
Q9610
DMN5L06VK-7
SOT563
VER 5
SYNC_MASTER=MARY_X425G
SYNC_DATE=09/22/2014
PAGE TITLE
eDP Mux
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
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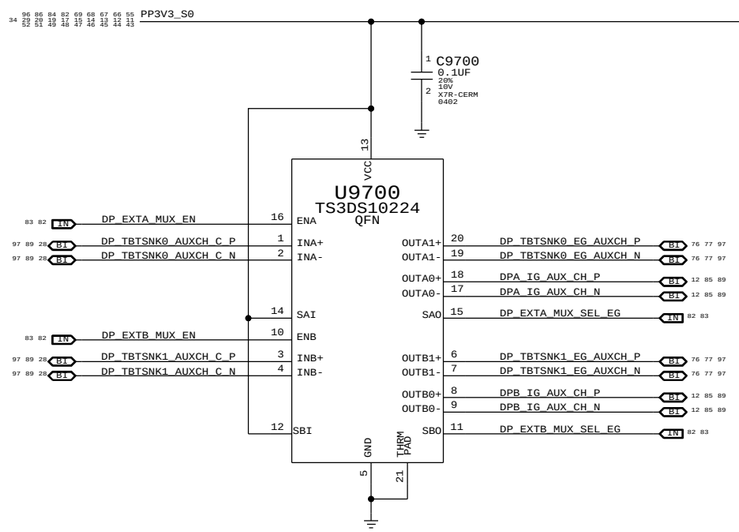
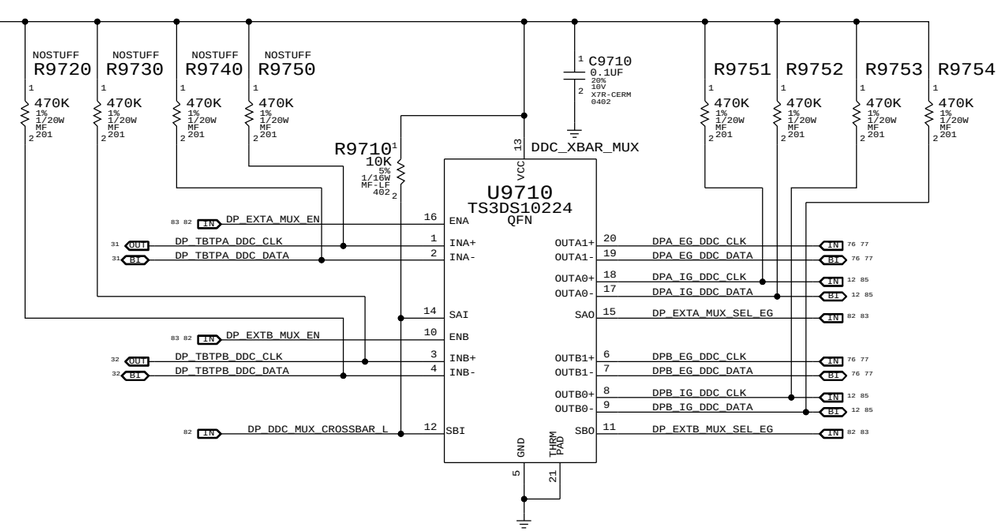
DP A & DP B AUX MUX



DP A & DP B DDC MUX



MUX TRUTH TABLE

SAI/SBI	SAO	SBO	INA	INB
0	0	0	OUTB0	OUTA0
0	0	1	OUTB1	OUTA0
0	1	0	OUTB0	OUTA1
0	1	1	OUTB1	OUTA1
1	0	0	OUTA0	OUTB0
1	0	1	OUTA0	OUTB1
1	1	0	OUTA1	OUTB0
1	1	1	OUTA1	OUTB1

SYNC_MASTER=MARY_X425G SYNC_DATE=10/15/2014

PAGE TITLE
eDP Muxed Graphics Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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G3H/5V Rails

PPBUS G3H
- PPBUS G3H — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=13.05V, MAKE_BASE=TRUE
- PPBUS G3H
- PPBUS G3H
- PPBUS G3H
- PPBUS G3H
- PPBUS G3H
- PPBUS G3H
- PPBUS G3H
- PPBUS G3H
- PPBUS G3H

PPVIN S5 HS COMPUTING ISNS
- PPVIN S5 HS COMPUTING ISNS — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=13.05V, MAKE_BASE=TRUE
- PPVIN S5 HS COMPUTING ISNS
- PPVIN S5 HS COMPUTING ISNS
- PPVIN S5 HS COMPUTING ISNS

PPVIN S5 HS OTHER3V3 ISNS
- PPVIN S5 HS OTHER3V3 ISNS — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=13.05V, MAKE_BASE=TRUE
- PPVIN S5 HS OTHER3V3 ISNS

PPVIN S5 HS OTHER5V ISNS
- PPVIN S5 HS OTHER5V ISNS — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=13.05V, MAKE_BASE=TRUE
- PPVIN S5 HS OTHER5V ISNS

PPBUS S4 TPAD
- PPBUS S4 TPAD — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=13.05V, MAKE_BASE=TRUE
- PPBUS S4 TPAD
- PPBUS S4 TPAD

PPVIN S4 TPAD
- PPVIN S4 TPAD — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=13.05V, MAKE_BASE=TRUE
- PPVIN S4 TPAD

PPVIN S5 HS GPU ISNS
- PPVIN S5 HS GPU ISNS — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=13.05V, MAKE_BASE=TRUE
- PPVIN S5 HS GPU ISNS
- PPVIN S5_HS_GPU_ISNS
- PPVIN S5 HS GPU ISNS
- PPVIN S5_HS_GPU_ISNS
- PPVIN S5_HS_GPU_ISNS

PPDCIN G3H
- PPDCIN G3H — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=20V, MAKE_BASE=TRUE
- PPDCIN G3H

PPDCIN G3H ISOL
- PPDCIN G3H ISOL — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=20V, MAKE_BASE=TRUE
- PPDCIN G3H ISOL
- PPDCIN G3H ISOL

PP3V42 G3H
- PP3V42 G3H — MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.42V, MAKE_BASE=TRUE
- PP3V42 G3H
- PP3V42 G3H
- PP3V42 G3H
- PP3V42 G3H
- PP3V42 G3H
- PP3V42 G3H
- PP3V42 G3H
- PP3V42 G3H
- PP3V42 G3H
- PP3V42 G3H
- PP3V42 G3H
- PP3V42 G3H

PPVRTC G3H
- PPVRTC G3H — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.42V, MAKE_BASE=TRUE
- PPVRTC G3H

PP5V S5
- PP5V S5 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.1 MM, VOLTAGE=5V, MAKE_BASE=TRUE
- PP5V_S5

PP5V S4
- PP5V S4 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=5V, MAKE_BASE=TRUE
- PP5V S4
- PP5V S4
- PP5V S4
- PP5V S4
- PP5V S4
- PP5V S4
- PP5V S4

PP5V S3
- PP5V S3 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=5V, MAKE_BASE=TRUE
- PP5V S3
- PP5V S3
- PP5V_S3

PP5V S0
- PP5V S0 — MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=5V, MAKE_BASE=TRUE
- PP5V S0
- PP5V S0
- PP5V S0
- PP5V S0
- PP5V S0
- PP5V S0
- PP5V S0
- PP5V S0
- PP5V S0
- PP5V S0
- PP5V S0
- PP5V S0
- PP5V S0
- PP5V S0
- PP5V S0

3.3V Rails

PP3V3 S5
- PP3V3 S5 — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V, MAKE_BASE=TRUE
- PP3V3 S5
- PP3V3 S5
- PP3V3 S5

Display Aliases

85 82 12	EDP_IG_PANEL_PWR (MAKE_BASE=TRUE)	EDP_IG_PANEL_PWR	12 82 85
85 82 12	EDP_IG_BKL_ON (MAKE_BASE=TRUE)	EDP_IG_BKL_ON	12 82 85
97 82 5	DP_INT_IG_ML_P<3..0> (MAKE_BASE=TRUE)	TP_DP_IG_A_MLP<3..0>	
97 82 5	DP_INT_IG_ML_N<3..0> (MAKE_BASE=TRUE)	TP_DP_IG_A_MLN<3..0>	
97 85 82 5	DP_INT_IG_AUX_P (MAKE_BASE=TRUE)	DP_INT_IG_AUX_P	5 82 85 97
97 85 82 5	DP_INT_IG_AUX_N (MAKE_BASE=TRUE)	DP_INT_IG_AUX_N	5 82 85 97
89 85 83 12	DPA_IG_AUX_CH_P (MAKE_BASE=TRUE)	DPA_IG_AUX_CH_P	12 83 85 89
89 85 83 12	DPA_IG_AUX_CH_N (MAKE_BASE=TRUE)	DPA_IG_AUX_CH_N	12 83 85 89
89 85 83 12	DPB_IG_AUX_CH_P (MAKE_BASE=TRUE)	DPB_IG_AUX_CH_P	12 83 85 89
89 85 83 12	DPB_IG_AUX_CH_N (MAKE_BASE=TRUE)	DPB_IG_AUX_CH_N	12 83 85 89
85 83 12	DPA_IG_DDC_CLK (MAKE_BASE=TRUE)	DPA_IG_DDC_CLK	12 83 85
85 83 12	DPA_IG_DDC_DATA (MAKE_BASE=TRUE)	DPA_IG_DDC_DATA	12 83 85
85 83 12	DPB_IG_DDC_CLK (MAKE_BASE=TRUE)	DPB_IG_DDC_CLK	12 83 85
85 83 12	DPB_IG_DDC_DATA (MAKE_BASE=TRUE)	DPB_IG_DDC_DATA	12 83 85
85 82 12	DP_TBTSNK0_HPD_IG (MAKE_BASE=TRUE)	DP_TBTSNK0_HPD_IG	12 82 85
85 82 12	DP_TBTSNK1_HPD_IG (MAKE_BASE=TRUE)	DP_TBTSNK1_HPD_IG	12 82 85
85 82	DPMUX_UC_RX (MAKE_BASE=TRUE)	DPMUX_UC_RX	82 85
85 82	DPMUX_UC_TX (MAKE_BASE=TRUE)	DPMUX_UC_TX	82 85
85 82 70	EG_RESET_L (MAKE_BASE=TRUE)	EG_RESET_L	70 82 85
85 82 11	PEG_CLKREQ_L (MAKE_BASE=TRUE)	PEG_CLKREQ_L	11 82 85
85 18 11	DP_AUXCH_ISOL_L (MAKE_BASE=TRUE)	DP_AUXCH_ISOL_L	11 18 85

86 85 82 69	LCD_FSS (MAKE_BASE=TRUE)	LCD_FSS	69 82 85 86
91 85 70 11	PEG_CLK100M_N (MAKE_BASE=TRUE)	PEG_CLK100M_N	11 70 85 91
91 85 70 11	PEG_CLK100M_P (MAKE_BASE=TRUE)	PEG_CLK100M_P	11 70 85 91
96 85 79 71	VSNS_GPU_VDDC_P (MAKE_BASE=TRUE)	VSNS_GPU_VDDC_P	71 79 85 96
96 85 80 71	VSNS_GPU_VDDI_P (MAKE_BASE=TRUE)	VSNS_GPU_VDDI_P	71 80 85 96

CPU signals

85 60 21	MEMVTT_EN (MAKE_BASE=TRUE)	MEMVTT_EN	21 60 85

J9510 RIO FLEX CONN

91 86 85 81 43 18 13	SMBUS_PCH_DATA	SMBUS_PCH_DATA	13 18 43 81 85 86 91
91 86 85 81 43 18 13	SMBUS_PCH_CLK	SMBUS_PCH_CLK	13 18 43 81 85 86 91

SSD Signals Through PEG

89 34 5 IN	PCIE_SSD_D2R_P<3..0> (MAKE_BASE=TRUE)	=PEG_D2R_P<15..12>	OUT
89 34 5 IN	PCIE_SSD_D2R_N<3..0> (MAKE_BASE=TRUE)	=PEG_D2R_N<15..12>	OUT
89 34 5 OUT	PCIE_SSD_R2D_C_P<3..0> (MAKE_BASE=TRUE)	=PEG_R2D_C_P<15..12>	IN
89 34 5 OUT	PCIE_SSD_R2D_C_N<3..0> (MAKE_BASE=TRUE)	=PEG_R2D_C_N<15..12>	IN

Thunderbolt Signals Through PEG

89 28 5 IN	PCIE_TBT_D2R_P<3..0> (MAKE_BASE=TRUE)	=PEG_D2R_P<11..8>	OUT
89 28 5 IN	PCIE_TBT_D2R_N<3..0> (MAKE_BASE=TRUE)	=PEG_D2R_N<11..8>	OUT
89 28 5 OUT	PCIE_TBT_R2D_C_P<3..0> (MAKE_BASE=TRUE)	=PEG_R2D_C_P<11..8>	IN
89 28 5 OUT	PCIE_TBT_R2D_C_N<3..0> (MAKE_BASE=TRUE)	=PEG_R2D_C_N<11..8>	IN

GUP PEG Lanes

89 70	PEG_D2R_P<7..0> (MAKE_BASE=TRUE)	=PEG_D2R_P<7..0>	5
89 70	PEG_D2R_N<7..0> (MAKE_BASE=TRUE)	=PEG_D2R_N<7..0>	5
89 70 68	PEG_R2D_C_P<7..0> (MAKE_BASE=TRUE)	=PEG_R2D_C_P<7..0>	5
89 70 68	PEG_R2D_C_N<7..0> (MAKE_BASE=TRUE)	=PEG_R2D_C_N<7..0>	5

Unused PCH PCIE Lanes

		MAKE_BASE	NO_TEST		
13	NC_PCIE_SSD_D2RP<3..0>	TRUE	TRUE	=PCIE_SSD_D2R_P<3..0>	
13	NC_PCIE_SSD_D2RN<3..0>	TRUE	TRUE	=PCIE_SSD_D2R_N<3..0>	
13	NC_PCIE_SSD_R2D_CP<3..0>	TRUE	TRUE	=PCIE_SSD_R2D_C_P<3..0>	
13	NC_PCIE_SSD_R2D_CN<3..0>	TRUE	TRUE	=PCIE_SSD_R2D_C_N<3..0>	

Unused TPAD SPI

67 66 65 46 45 42 41 38 33 20 86 85 84 81 PP3V3_S4

85 38	TPAD_SPI_BUS_EN	85 38	TPAD_SPI_BUS_EN	MAKE_BASE	RA294 100K 1% 1/20W MF 201
91 85 38	TPAD_SPI_CS_L	91 85 38	TPAD_SPI_CS_L	TRUE	RA295 100K 1% 1/20W MF 201
85 38	TPAD_SPI_INT_L	85 38	TPAD_SPI_INT_L	TRUE	RA296 100K 1% 1/20W MF 201
91 85 38	TPAD_SPI_MISO	91 85 38	TPAD_SPI_MISO	TRUE	RA297 100K 1% 1/20W MF 201
91 85 38	TPAD_SPI_MOSI	91 85 38	TPAD_SPI_MOSI	TRUE	RA298 100K 1% 1/20W MF 201
91 85 38	TPAD_SPI_SCLK	91 85 38	TPAD_SPI_SCLK	TRUE	RA299 100K 1% 1/20W MF 201

92 89 85 24 23 22	PP0V75_S3_MEM_VREFDQ_A	0.675V	TRUE	PP0V75_S3_MEM_VREFDQ_A	22 23 24 85 89 92
89 85 26 25 22	PP0V75_S3_MEM_VREFDQ_B	0.675V	TRUE	PP0V75_S3_MEM_VREFDQ_B	22 25 26 85 89
92 89 85 26 25 24 23 22	PP0V75_S3_MEM_VREFCA	0.675V	TRUE	PP0V75_S3_MEM_VREFCA	22 23 24 25 26 85 89 92
92 89 85 26 25 24 23 22	PP0V75_S3_MEM_VREFCA				
92 89 85 26 25 24 23 22	PP0V75_S3_MEM_VREFCA				

EDP CABLE

86 85 69 63	I2C_BKLT_SCL (MAKE_BASE=TRUE)	I2C_BKLT_SCL	63 69 85 86
86 85 69 63	I2C_BKLT_SDA (MAKE_BASE=TRUE)	I2C_BKLT_SDA	63 69 85 86
95 86 85 76 69 48 43 40 36	SMBUS_SMC_0_S0_SCL	SMBUS_SMC_0_S0_SCL	36 40 43 48 69 76 85 86 95
95 86 85 76 69 48 43 40 36	SMBUS_SMC_0_S0_SDA	SMBUS_SMC_0_S0_SDA	36 40 43 48 69 76 85 86 95

85 49 PP3V3_S3_FAN_CTL — PP3V3_S3_FAN_CTL (MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.2MM, VOLTAGE=3.3V, MAKE_BASE=TRUE) 49 85

RA201 0 5% 1/20W MF 0201

PP3V3_S5 — 12 14 15 17 18 19 21 31 32 33 61 64 66 67 82 84 86 96

PP3V3_S4 — 20 33 38 41 42 45 46 65 66 67 81 84 85 86

RA202 NOSTUFF

67 66 63 62 59 58 49 36 19 18 86 84 80 79 73 PP5V_S0

XWA202 SM — PP5V_S0_AUDIO_AMP_L (MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.2MM, VOLTAGE=5V) 53

XWA203 SM — PP5V_S0_AUDIO_AMP_R (MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.2MM, VOLTAGE=5V) 53

Unused signals

12	BT_PWRRST_L
14	MEM_VDD_SEL_1V5_L
14	FW_PWR_EN_PCH
14	WOL_EN
14	FW_PME_L
11	DP_TBT_SEL
11	ENET_MEDIA_SENSE_RDIV
12	AUD_IPHS_SWITCH_EN_PCH
12	AUD_IP_PERIPHERAL_DET
12	AUD_I2C_INT_L
14	TBT_GO2SX_BIDIR
82 14	DPMUX_UC_IRQ
85 82 11	PEG_CLKREQ_L
11	ENET_CLKREQ_L
12	ENET_LOW_PWR_PCH
28	HDMITBTMUX_SEL_TBT
12	SDCONN_OC_L
14	LPCPLUS_GPIO

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: Signal Aliases

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Functional Test Points

J3501 - airport

FUNC_TEST			
TRUE	AP_CLKREQ_Q_L	33	
TRUE	AP_RESET_CONN_L	33	
TRUE	PCIE_AP_D2R_PI_N	91	
TRUE	PCIE_AP_D2R_PI_P	91	
TRUE	PCIE_AP_R2D_N	33 91	
TRUE	PCIE_AP_R2D_P	33 91	
TRUE	PCIE_CLK100M_AP_CONN_N	33 91	
TRUE	PCIE_CLK100M_AP_CONN_P	33 91	
TRUE	PCIE_WAKE_L	12 33 35 91	
TRUE	PP3V3_S3RS4_BT_F	33	
TRUE	PP3V3_WLAN	33 41	
TRUE	USB_BT_CONN_N	33 90	
TRUE	USB_BT_CONN_P	33 90	
TRUE	WIFI_EVENT_L	33 40 41	
TRUE	GND	4X	

J4002 - Camera

TRUE	MIPI_CLK_CONN_N	36 94
TRUE	MIPI_CLK_CONN_P	36 94
TRUE	CAM_SENSOR_WAKE_L_CONN	36
TRUE	MIPI_DATA_CONN_N	36 94
TRUE	MIPI_DATA_CONN_P	36 94
TRUE	SMBUS_SMC_0_S0_SDA	36 40 43 48 69 76 85 86 95
TRUE	SMBUS_SMC_0_S0_SCL	36 40 43 48 69 76 85 86 95
TRUE	I2C_CAM_SCK	35 36
TRUE	I2C_CAM_SDA	35 36
TRUE	PP5V_S3RS0_ALSCAM_F	36
TRUE	GND	

J9500 - rio coax

TRUE	HDMI_EG_CLK_N	76 81 97
TRUE	HDMI_EG_CLK_P	76 81 97
TRUE	HDMI_EG_DATA_N<0>	76 81 97
TRUE	HDMI_EG_DATA_N<1>	76 81 97
TRUE	HDMI_EG_DATA_N<2>	76 81 97
TRUE	HDMI_EG_DATA_P<0>	76 81 97
TRUE	HDMI_EG_DATA_P<1>	76 81 97
TRUE	HDMI_EG_DATA_P<2>	76 81 97
TRUE	USB3_SD_D2R_N	13 20 81 91
TRUE	USB3_SD_D2R_P	13 20 81 91
TRUE	USB3_SD_R2D_C_N	13 20 81 91
TRUE	USB3_SD_R2D_C_P	13 20 81 91
TRUE	USB3_EXTB_D2R_N	13 81 90
TRUE	USB3_EXTB_D2R_P	13 81 90
TRUE	USB3_EXTB_R2D_N	81 90
TRUE	USB3_EXTB_R2D_P	81 90
TRUE	USB_EXTB_N	13 81 90
TRUE	USB_EXTB_P	13 81 90
TRUE	GND	19X

J9510 - rio flex

1200	TRUE	SD_PWR_EN	13 18 81
1200	TRUE	HDMI_DDC_CLK	
1200	TRUE	HDMI_DDC_DATA	
1200	TRUE	HDMI_HPD	20 81 82
1200	TRUE	SMBUS_PCH_CLK	13 18 43 81 85 91
1200	TRUE	SMBUS_PCH_DATA	13 18 43 81 85 91
1200	TRUE	PM_SLP_S3_BUF_L	51 66 67 81 82
1200	TRUE	PM_SLP_S4_L	12 21 33 37 40 67 81
1200	TRUE	PP3V3_S3	3X 13 20 21 43 45 46 66 81 82 84 86
1200	TRUE	PP3V3_S4	20 33 38 41 42 45 46 65 66 67 81 84 85 86
1200	TRUE	PP5V_S4	5X 37 38 51 61 66 67 69 81 84 86
1200	TRUE	RIO_SDCONN_STATE_CHANGE_L	20 81
1200	TRUE	USB_EXTB_OC_L	18 81
	TRUE	GND	10X

J5150 - hall effect

TRUE	PP3V42_G3H	19 34 37 38 40 41 42 43 50 56 57 67 84 86
TRUE	SMC_LID_R	42
TRUE	GND	

J6050 - left fan

TRUE	FAN_LT_PWM	49
TRUE	FAN_LT_TACH	49
TRUE	PP5V_S0	3X 18 19 36 49 58 59 62 63 66 67 73 79 80 84 85 86
TRUE	GND	5X

J6060 - right fan

TRUE	FAN_RT_PWM	49
TRUE	FAN_RT_TACH	49
TRUE	PP5V_S0	3X 18 19 36 49 58 59 62 63 66 67 73 79 80 84 85 86
TRUE	GND	5X

J6100 - spi

FUNC_TEST			
1200	TRUE	PP3V42_G3H	19 34 37 38 40 41 42 43 50 56 57 67 84 86
1200	TRUE	SMC_RESET_L	40 41 50 57
1200	TRUE	SMC_TCK	40 41 50
1200	TRUE	SMC_TMS	40 41 50
1200	TRUE	SPIROM_USE_MLB	14 50
	TRUE	GND	2X

J4801 - ipd flex

1200	TRUE	USB_TPAD_N	13 38 90
1200	TRUE	USB_TPAD_P	13 38 90
1200	TRUE	IOXP2_INT_L	38
1200	TRUE	I2C_IOXP_SCL	38
1200	TRUE	I2C_IOXP_SDA	38
1200	TRUE	SMC_PME_S4_WAKE_L	33 38 40 42
1200	TRUE	TPAD_ACTUATOR_THRMTRIP_L	38 65
1200	TRUE	TPAD_VBUS_EN	38 67
1200	TRUE	SMBUS_SMC_2_S3_SCL	38 40 43 95
1200	TRUE	SMBUS_SMC_2_S3_SDA	38 40 43 95
1200	TRUE	SMC_LID	38 40 41 42
1200	TRUE	SMC_ACTUATOR_EN_L	38 40
1200	TRUE	PPVIN_S4_TPAD	4X 38 45 84
1200	TRUE	GND_ACTUATOR	4X 38
1200	TRUE	PP3V3_S4	20 33 38 41 42 45 46 65 66 67 81 84 85 86
1200	TRUE	PP5V_S4	37 38 51 61 66 67 69 81 84 86
	TRUE	GND	2X

J4813 - keyboard

TRUE	PP3V3_S4	20 33 38 41 42 45 46 65 66 67 81 84 85 86
TRUE	PP3V42_G3H	19 34 37 38 40 41 42 43 50 56 57 67 84 86
TRUE	WS_CONTROL_KBD	38
TRUE	WS_KBD1	38
TRUE	WS_KBD10	38
TRUE	WS_KBD11	38
TRUE	WS_KBD12	38
TRUE	WS_KBD13	38
TRUE	WS_KBD14	38
TRUE	WS_KBD15_CAP	38
TRUE	WS_KBD16_NUM	38
TRUE	WS_KBD17	38
TRUE	WS_KBD18	38
TRUE	WS_KBD19	38
TRUE	WS_KBD2	38
TRUE	WS_KBD20	38
TRUE	WS_KBD21	38
TRUE	WS_KBD22	38
TRUE	WS_KBD23	38
TRUE	WS_KBD3	38
TRUE	WS_KBD4	38
TRUE	WS_KBD5	38
TRUE	WS_KBD6	38
TRUE	WS_KBD7	38
TRUE	WS_KBD8	38
TRUE	WS_KBD9	38
TRUE	WS_KBD_ONOFF_L	38
TRUE	WS_LEFT_OPTION_KBD	38
TRUE	WS_LEFT_SHIFT_KBD	38
TRUE	GND	2X

J4915 - kbd bklt

TRUE	KBDBKLT_RETURN1	2X 39 63
TRUE	KBDBKLT_RETURN2	2X 39 63
TRUE	PPVOUT_S0_KBDBKLT	39 63
TRUE	GND	4X

J6601 - mic

1190	TRUE	DMIC_CLK3	52 55
1190	TRUE	PP3V3_S0	66 67 68 69 82 83 84 86 96 11 12 13 14 15 17 19 20 29 34 11 14 45 46 47 48 49 51 52 55
1190	TRUE	DMIC_SDA2	55
1190	TRUE	DMIC_SDA3	52 55
	TRUE	GND	

J6602 - L speaker

1190	TRUE	SPKRCONN_L_ID	52 55
1190	TRUE	SPKRCONN_L_OUT_N	53 55 96
1190	TRUE	SPKRCONN_L_OUT_P	53 55 96
1190	TRUE	SPKRCONN_SL_OUT_N	53 55 96
1190	TRUE	SPKRCONN_SL_OUT_P	53 55 96
	TRUE	GND	

J6603 - R speaker

1190	TRUE	SPKRCONN_R_ID	52 55
1190	TRUE	SPKRCONN_R_OUT_N	53 55 96
1190	TRUE	SPKRCONN_R_OUT_P	53 55 96
1190	TRUE	SPKRCONN_SR_OUT_N	53 55 96
1190	TRUE	SPKRCONN_SR_OUT_P	53 55 96
	TRUE	GND	

J7000 - DC PWR

TRUE	ADAPTER_SENSE	56
TRUE	PP20V_DCIN_FUSE	2X 56
TRUE	GND	2X

J7050 - battery

TRUE	PPVBAT_G3H_CONN	8X 56 57
TRUE	SMBUS_SMC_5_G3_SCL	40 43 56 57 95
TRUE	SMBUS_SMC_5_G3_SDA	40 43 56 57 95
TRUE	SYS_DETECT_L	56
TRUE	GND	8X

J8300 - eDP

1200	TRUE	DP_INT_AUX_N	69 97
1200	TRUE	DP_INT_AUX_P	69 97
1200	TRUE	DP_INT_ML_N<0>	69 97
1200	TRUE	DP_INT_ML_N<1>	69 97
1200	TRUE	DP_INT_ML_N<2>	69 97
1200	TRUE	DP_INT_ML_N<3>	69 97
1200	TRUE	DP_INT_ML_P<0>	69 97
1200	TRUE	DP_INT_ML_P<1>	69 97
1200	TRUE	DP_INT_ML_P<2>	69 97
1200	TRUE	DP_INT_ML_P<3>	69 97
1200	TRUE	LCD_FSS	69 82 85
1200	TRUE	LCD_HPD_CONN	69
1200	TRUE	LCD_BKLT_PWM_R	63 69
1200	TRUE	SMBUS_SMC_0_S0_SDA	36 40 43 48 69 76 85 86 95
1200	TRUE	SMBUS_SMC_0_S0_SCL	36 40 43 48 69 76 85 86 95
1200	TRUE	I2C_BKLT_SDA	63 69 85
1200	TRUE	I2C_BKLT_SCL	63 69 85
1200	TRUE	PP5VR3V3_SW_LCD	3X 69
1200	TRUE	PPVOUT_S0_LCDBKLT	63 69
	TRUE	GND	16X

Power Rails

TRUE	PM_SLP_S3_L	12 21 40 67
TRUE	PPVTT_S0_DDR	21 27 60 84
TRUE	PP3V3_S0	66 67 68 69 82 83 84 86 96 11 12 13 14 15 17 19 20 29 34
TRUE	PP3V3_S3	43 44 45 46 47 48 49 51 52 55 13 20 21 43 45 46 66 81 82 84 86
TRUE	PP3V3_S5	12 14 15 17 18 19 21 31 32 33 61 64 66 67 82 84 85 86
TRUE	PP3V3_S5_AVREF_SMC	40 41
TRUE	PP3V42_G3H	19 34 37 38 40 41 42 43 50 56 57 67 84 86
TRUE	PP5V_S0	18 19 36 49 58 59 62 63 66 67 73 79 80 84 85 86
TRUE	PP5V_S3	21 36 60 66 67 84
TRUE	PP5V_S5	61 66 84
TRUE	PPBUS_G3H	30 44 47 56 57 63 65 84
TRUE	PPDCIN_G3H	56 57 84
TRUE	PPVCC_S0_CPU	6 8 10 45 59 84
TRUE	PPVTTDDR_S3	60 84
1150	PP3V3_S0SW_SSD	34 45 84
1150	PP1V5_S0	11 12 13 15 17 19 52 64 67 81 84
1150	PP1V35_S3	21 45 60 66 84

XDP

FUNC_TEST			
1190	TRUE	XDP_CPU_TCK	6 18 89
1190	TRUE	XDP_PCH_TCK	11 18
1190	TRUE	XDP_CPU_TDI	6 18 89
1190	TRUE	XDP_CPU_TDO	6 18 89
1190	TRUE	XDP_CPUPCH_TRST_L	6 18 89
1190	TRUE	XDP_CPU_TMS	6 18 89
1190	TRUE	XDP_PCH_TMS	11 18
1190	TRUE	XDP_PCH_TDI	11 18
1190	TRUE	XDP_PCH_TDO	11 18
1190	TRUE	XDP_CPU_PREQ_L	6 18 89
1190	TRUE	XDP_CPU_PRDY_L	6 18 89
1190	TRUE	PM_RSMRST_L	12 67 91
1190	TRUE	PM_PCH_PWROK	12 19 91
1190	TRUE	PM_SYSRST_L	12 19 40 91
1190	TRUE	CPU_CFG<3>	6 18 89
1190	TRUE	PP1V05_S0	10 14 15 17 18 41 62 67 84
	TRUE	GND	2X GND

Power Sequence

FUNC_TEST			
1190	TRUE	SMC_ONOFF_L	38 40 41
1190	TRUE	PM_DSW_PWRGD	12 40 91
1190	TRUE	ALL_SYS_PWRGD	18 19 40 58 67
1190	TRUE	PM_PCH_SYS_PWROK	12 18 19 40 91
1190	TRUE	PLT_RESET_L	12 18 20 21
1190	TRUE	LCD_PWR_EN	69 82
1190	TRUE	LCD_BKLT_EN	63 82

GPU_VENUS JTAG

FUNC_TEST			
1200	TRUE	GPU_JTAG_TCK	76 77
1200	TRUE	GPU_JTAG_TDI	76 77
1200	TRUE	GPU_JTAG_TDO	76 77
1200	TRUE	GPU_JTAG_TMS	76 77
1200	TRUE	GPU_JTAG_TRST_L	76 77
1200	TRUE	GPU_PWRGOOD	

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PAGE TITLE: Functional Test Points

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NC NO_TESTs

PCH

		NO_TEST	MAKE_BASE		
87 13	NC_USB3_SPARE_D2RN	TRUE	TRUE	NC_USB3_SPARE_D2RN	13 87
87 13	NC_USB3_SPARE_D2RP	TRUE	TRUE	NC_USB3_SPARE_D2RP	13 87
87 13	NC_USB3_SPARE_R2D_CN	TRUE	TRUE	NC_USB3_SPARE_R2D_CN	13 87
87 13	NC_USB3_SPARE_R2D_CP	TRUE	TRUE	NC_USB3_SPARE_R2D_CP	13 87
90 87 13	NC_USB3_EXTC_D2RN	TRUE	TRUE	NC_USB3_EXTC_D2RN	13 87 90
90 87 13	NC_USB3_EXTC_D2RP	TRUE	TRUE	NC_USB3_EXTC_D2RP	13 87 90
90 87 13	NC_USB3_EXTC_R2D_CN	TRUE	TRUE	NC_USB3_EXTC_R2D_CN	13 87 90
90 87 13	NC_USB3_EXTC_R2D_CP	TRUE	TRUE	NC_USB3_EXTC_R2D_CP	13 87 90
90 87 13	NC_USB3_EXTD_D2RN	TRUE	TRUE	NC_USB3_EXTD_D2RN	13 87 90
90 87 13	NC_USB3_EXTD_D2RP	TRUE	TRUE	NC_USB3_EXTD_D2RP	13 87 90
90 87 13	NC_USB3_EXTD_R2D_CN	TRUE	TRUE	NC_USB3_EXTD_R2D_CN	13 87 90
90 87 13	NC_USB3_EXTD_R2D_CP	TRUE	TRUE	NC_USB3_EXTD_R2D_CP	13 87 90
87	NC_PCIE_ENET_D2RN	TRUE	TRUE	NC_PCIE_ENET_D2RN	87
87	NC_PCIE_ENET_D2RP	TRUE	TRUE	NC_PCIE_ENET_D2RP	87
87	NC_PCIE_ENET_R2D_CN	TRUE	TRUE	NC_PCIE_ENET_R2D_CN	87
87	NC_PCIE_ENET_R2D_CP	TRUE	TRUE	NC_PCIE_ENET_R2D_CP	87
90 87 11	NC_SATA_A_D2RN	TRUE	TRUE	NC_SATA_A_D2RN	11 87 90
90 87 11	NC_SATA_A_D2RP	TRUE	TRUE	NC_SATA_A_D2RP	11 87 90
90 87 11	NC_SATA_A_R2D_CN	TRUE	TRUE	NC_SATA_A_R2D_CN	11 87 90
90 87 11	NC_SATA_A_R2D_CP	TRUE	TRUE	NC_SATA_A_R2D_CP	11 87 90
90 87 11	NC_SATA_B_D2RN	TRUE	TRUE	NC_SATA_B_D2RN	11 87 90
90 87 11	NC_SATA_B_D2RP	TRUE	TRUE	NC_SATA_B_D2RP	11 87 90
90 87 11	NC_SATA_B_R2D_CN	TRUE	TRUE	NC_SATA_B_R2D_CN	11 87 90
90 87 11	NC_SATA_B_R2D_CP	TRUE	TRUE	NC_SATA_B_R2D_CP	11 87 90
87 11	NC_SATA_ODD_D2RN	TRUE	TRUE	NC_SATA_ODD_D2RN	11 87
87 11	NC_SATA_ODD_D2RP	TRUE	TRUE	NC_SATA_ODD_D2RP	11 87
87 11	NC_SATA_ODD_R2D_CN	TRUE	TRUE	NC_SATA_ODD_R2D_CN	11 87
87 11	NC_SATA_ODD_R2D_CP	TRUE	TRUE	NC_SATA_ODD_R2D_CP	11 87
87 11	NC_SATA_D_D2RN	TRUE	TRUE	NC_SATA_D_D2RN	11 87
87 11	NC_SATA_D_D2RP	TRUE	TRUE	NC_SATA_D_D2RP	11 87
87 11	NC_SATA_D_R2D_CN	TRUE	TRUE	NC_SATA_D_R2D_CN	11 87
87 11	NC_SATA_D_R2D_CP	TRUE	TRUE	NC_SATA_D_R2D_CP	11 87
87 11	NC_SATA_F_D2RN	TRUE	TRUE	NC_SATA_F_D2RN	11 87
87 11	NC_SATA_F_D2RP	TRUE	TRUE	NC_SATA_F_D2RP	11 87
87 11	NC_SATA_F_R2D_CN	TRUE	TRUE	NC_SATA_F_R2D_CN	11 87
87 11	NC_SATA_F_R2D_CP	TRUE	TRUE	NC_SATA_F_R2D_CP	11 87
90 87 13	NC_USB_EXTCN	TRUE	TRUE	NC_USB_EXTCN	13 87 90
90 87 13	NC_USB_EXTCP	TRUE	TRUE	NC_USB_EXTCP	13 87 90
90 87 13	NC_USB_SDN	TRUE	TRUE	NC_USB_SDN	13 87 90
90 87 13	NC_USB_SDP	TRUE	TRUE	NC_USB_SDP	13 87 90
87 13	NC_USB_WLANN	TRUE	TRUE	NC_USB_WLANN	13 87
87 13	NC_USB_WLANP	TRUE	TRUE	NC_USB_WLANP	13 87
90 87 13	NC_USB_6N	TRUE	TRUE	NC_USB_6N	13 87 90
90 87 13	NC_USB_6P	TRUE	TRUE	NC_USB_6P	13 87 90
90 87 13	NC_USB_7N	TRUE	TRUE	NC_USB_7N	13 87 90
90 87 13	NC_USB_7P	TRUE	TRUE	NC_USB_7P	13 87 90
90 87 13	NC_USB_EXTDN	TRUE	TRUE	NC_USB_EXTDN	13 87 90
90 87 13	NC_USB_EXTDP	TRUE	TRUE	NC_USB_EXTDP	13 87 90
87 13	NC_USB_PSOCN	TRUE	TRUE	NC_USB_PSOCN	13 87
87 13	NC_USB_PSOCP	TRUE	TRUE	NC_USB_PSOCP	13 87
90 87 13	NC_USB_IRN	TRUE	TRUE	NC_USB_IRN	13 87 90
90 87 13	NC_USB_IRP	TRUE	TRUE	NC_USB_IRP	13 87 90
89 87 11	NC_ITPXDP_CLK100MN	TRUE	TRUE	NC_ITPXDP_CLK100MN	11 87 89
89 87 11	NC_ITPXDP_CLK100MP	TRUE	TRUE	NC_ITPXDP_CLK100MP	11 87 89
87 12	NC_PCI_PME_L	TRUE	TRUE	NC_PCI_PME_L	12 87
87 11	NC_PCI_CLK33M_OUT3	TRUE	TRUE	NC_PCI_CLK33M_OUT3	11 87
87 11	NC_HDA_SDIN1	TRUE	TRUE	NC_HDA_SDIN1	11 87
87 11	NC_HDA_SDIN2	TRUE	TRUE	NC_HDA_SDIN2	11 87
87 11	NC_HDA_SDIN3	TRUE	TRUE	NC_HDA_SDIN3	11 87
87 13	NC_LPC_DREQ0_L	TRUE	TRUE	NC_LPC_DREQ0_L	13 87
87 13	NC_CLINK_CLK	TRUE	TRUE	NC_CLINK_CLK	13 87
87 13	NC_CLINK_DATA	TRUE	TRUE	NC_CLINK_DATA	13 87
87 13	NC_CLINK_RESET_L	TRUE	TRUE	NC_CLINK_RESET_L	13 87
91 87 11	NC_LPC_CLK33M_LPCPLUS_R	TRUE	TRUE	NC_LPC_CLK33M_LPCPLUS_R	11 87 91
87 12	NC_EDP_IG_BKL_PWM	TRUE	TRUE	NC_EDP_IG_BKL_PWM	12 87
90 87	NC_USB_SMCP	TRUE	TRUE	NC_USB_SMCP	87 90
90 87	NC_USB_SMCN	TRUE	TRUE	NC_USB_SMCN	87 90
87	NC_SMC_INTERFACE_2	TRUE	TRUE	NC_SMC_INTERFACE_2	87

Thunderbolt

		NO_TEST	MAKE_BASE		
87 28	NC_TBT_XTAL25OUT	TRUE	TRUE	NC_TBT_XTAL25OUT	28 87
	TP_DP_TBTSRC_ML_CP<3..0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<3..0>	28
	TP_DP_TBTSRC_ML_CN<3..0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<3..0>	28
28 87	NC_DP_TBTSRC_AUXCH_CP	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CP	28 87
28 87	NC_DP_TBTSRC_AUXCH_CN	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CN	28 87
87 12	NC_DP_IG_D_AUXCHN	TRUE	TRUE	NC_DP_IG_D_AUXCHN	12 87
87 12	NC_DP_IG_D_AUXCHP	TRUE	TRUE	NC_DP_IG_D_AUXCHP	12 87
87 11	NC_PCIE_CLK100M_PE5N	TRUE	TRUE	NC_PCIE_CLK100M_PE5N	11 87
87 11	NC_PCIE_CLK100M_PE5P	TRUE	TRUE	NC_PCIE_CLK100M_PE5P	11 87
87 11	NC_PCIE_CLK100M_ENETSDN	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDN	11 87
87 11	NC_PCIE_CLK100M_ENETSDP	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDP	11 87
87 11	NC_PCIE_CLK100M_ENETN	TRUE	TRUE	NC_PCIE_CLK100M_ENETN	11 87
87 11	NC_PCIE_CLK100M_ENETP	TRUE	TRUE	NC_PCIE_CLK100M_ENETP	11 87
87 11	NC_PCIE_CLK100M_PEGBN	TRUE	TRUE	NC_PCIE_CLK100M_PEGBN	11 87
87 11	NC_PCIE_CLK100M_PEGBP	TRUE	TRUE	NC_PCIE_CLK100M_PEGBP	11 87
87 11	NC_PCIE_CLK100M_SWN	TRUE	TRUE	NC_PCIE_CLK100M_SWN	11 87
87 11	NC_PCIE_CLK100M_SWP	TRUE	TRUE	NC_PCIE_CLK100M_SWP	11 87
87 11	NC_PCH_GPIO64_CLKOUTFLEX0	TRUE	TRUE	NC_PCH_GPIO64_CLKOUTFLEX0	11 87
87 11	NC_PCH_GPIO65_CLKOUTFLEX1	TRUE	TRUE	NC_PCH_GPIO65_CLKOUTFLEX1	11 87
87 11	NC_PCH_GPIO66_CLKOUTFLEX2	TRUE	TRUE	NC_PCH_GPIO66_CLKOUTFLEX2	11 87
87 11	NC_PCH_GPIO67_CLKOUTFLEX3	TRUE	TRUE	NC_PCH_GPIO67_CLKOUTFLEX3	11 87
87 13	NC_USB_4N	TRUE	TRUE	NC_USB_4N	13 87
87 13	NC_USB_4P	TRUE	TRUE	NC_USB_4P	13 87
	TP_DVPCNTL_M<1..0>	TRUE	TRUE	NC_DVPCNTL_M<1..0>	76
	TP_DVPCNTL<2..0>	TRUE	TRUE	NC_DVPCNTL<2..0>	76
87 76	NC_DVPCLK	TRUE	TRUE	NC_DVPCLK	76 87
	TP_NC_DVPDATA<23..6>	TRUE	TRUE	NC_DVPDATA<23..6>	76
87 72	NC_FB_B0_A<9>	TRUE	TRUE	NC_FB_B0_A<9>	72 87
87 72	NC_FB_B1_A<9>	TRUE	TRUE	NC_FB_B1_A<9>	72 87
87 72	NC_FB_A0_A<9>	TRUE	TRUE	NC_FB_A0_A<9>	72 87
87 72	NC_FB_A1_A<9>	TRUE	TRUE	NC_FB_A1_A<9>	72 87
		TRUE		PCIE_TBT_R2D_P<3..0>	28 89
		TRUE		PCIE_TBT_R2D_N<3..0>	28 89
		TRUE		PCIE_TBT_D2R_C_P<3..0>	28 89
		TRUE		PCIE_TBT_D2R_C_N<3..0>	28 89
		TRUE		DMI_S2N_P<3..1>	5 12 89
		TRUE		DMI_S2N_N<3..1>	5 12 89
		TRUE		DMI_N2S_P<3..1>	5 12 89
		TRUE		DMI_N2S_N<3..1>	5 12 89

PLACEABLE BEAD-PROBES FOR TBT

93 31 28	TBT_A_D2R_P<1>	1	SM BEAD-PROBE	BPA531 NO_XNET_CONNECTION=TRUE
93 31 28	TBT_A_D2R_N<1>	1	SM BEAD-PROBE	BPA532 NO_XNET_CONNECTION=TRUE

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

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NC & No Test

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X425G BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,P65BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.186 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.146 MM	0.146 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.155 MM	0.155 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.105 MM	0.105 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.101 MM	0.101 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?

Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	·	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.053 MM	?
1X_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.101 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65_BGA

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PCB Rule Definitions

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?
CPU_VREF	*	12 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	*	=3X_DIELECTRIC	?
DMI_TXRX	*	=6X_DIELECTRIC	?
DMICLK2N2S	*	=6X_DIELECTRIC	?
DMICLK2S2N	*	=3X_DIELECTRIC	?
DMICLK2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
DMI_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICLK2N2S	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICLK2S2N	TOP,BOTTOM	=6X_DIELECTRIC	?
DMICLK2OTHER	TOP,BOTTOM	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_*	=SAME	*	DMI_2SAME
DMI_N2S	DMI_S2N	*	DMI_TXRX
DMI_S2N	DMI_N2S	*	DMI_TXRX
CLK_DMI	DMI_N2S	*	DMICLK2N2S
CLK_DMI	DMI_S2N	*	DMICLK2S2N
CLK_DMI	*	*	DMICLK2OTHER

PEG - SSD & TBT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PEG_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	*	=3X_DIELECTRIC	?
PEG_TXRX	*	=6X_DIELECTRIC	?
PEG_2OTHER	*	=4X_DIELECTRIC	?
PEG_2CLK	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PEG_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PEG_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PEG_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG3_2SAME	*	=4X_DIELECTRIC	?
PEG3_TXRX	*	=8X_DIELECTRIC	?
PEG3_2OTHER	*	=5X_DIELECTRIC	?
PEG3_2CLK	*	=8X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG3_2SAME	TOP,BOTTOM	=6X_DIELECTRIC	?
PEG3_TXRX	TOP,BOTTOM	=12X_DIELECTRIC	?
PEG3_2OTHER	TOP,BOTTOM	=8X_DIELECTRIC	?
PEG3_2CLK	TOP,BOTTOM	=12X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG_*	=SAME	*	PEG_2SAME
PEG_R2D	PEG_D2R	*	PEG_TXRX
PEG_*	*	*	PEG_2OTHER
PEG_*	CLK_*	*	PEG_2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG3_*	=SAME	*	PEG3_2SAME
PEG3_R2D	PEG3_D2R	*	PEG3_TXRX
PEG3_*	*	*	PEG3_2OTHER
PEG3_*	CLK_*	*	PEG3_2CLK

DIGITAL VIDEO SIGNAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	*	=3x_DIELECTRIC	?
DP_2OTHER	*	=4x_DIELECTRIC	?
HDMICLK_2CLK	*	=7x_DIELECTRIC	?
HDMICLK_2DP	*	=4x_DIELECTRIC	?
HDMICLK_2OTHER	*	=7x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2CLK	TOP,BOTTOM	=10x_DIELECTRIC	?
HDMICLK_2DP	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	=SAME	*	DP_2SAME
DISPLAYPORT	*	*	DP_2OTHER
HDMI_CLK	CLK_*	*	HDMICLK_2CLK
HDMI_CLK	DISPLAYPORT	*	HDMICLK_2DP
HDMI_CLK	*	*	HDMICLK_2OTHER

DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.
MAX LENGTH OF DISPLAYPORT/TMDS TRACES: 13 INCHES.

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N P<3:0>	5 12 87
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N N<3:0>	5 12 87
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S P<3:0>	5 12 87
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S N<3:0>	5 12 87
FDI_INT	CPU_50S	CPU_AGTL	FDI_INT	5 12
FDI_CSYNC	CPU_50S	CPU_AGTL	FDI_CSYNC	5 12
DMI_CLK	CPU_85D	CLK_DMI	DMI_CLK100M_CPU_P	6 11
DMI_CLK	CPU_85D	CLK_DMI	DMI_CLK100M_CPU_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLREF_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLREF_P	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLSS_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLSS_P	6 11
CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU_EDP_RCOMP	5
CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU_PEG_RCOMP	5
CPU_CFG	CPU_45S	CPU_ITP	CPU_CFG<19..0>	6 18 86
XDP_CLK_PCH	CLK_PCIE_85D	CLK_PCIE	NC_ITPXDP_CLK100MP	11 87
XDP_CLK_PCH	CLK_PCIE_85D	CLK_PCIE	NC_ITPXDP_CLK100MN	11 87
XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI	6 18 86
XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO	6 18 86
XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS	6 18 86
XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK	6 18 86
XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPUPCH_TRST_L	6 18 86
XDP_BPM	CPU_45S	CPU_ITP	XDP_BPM_L<3..0>	6 18
XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<7..4>	6 18
XDP_DBRESET_L	CPU_45S	CPU_ITP	XDP_DBRESET_L	6 18 19
XDP_PRDY_L	CPU_45S	CPU_ITP	XDP_CPU_PRDY_L	6 18 86
XDP_PREQ_L	CPU_45S	CPU_ITP	XDP_CPU_PREQ_L	6 18 86
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L	6 40
CPU_PECI	CPU_45S	CPU_VID	CPU_PECI	6 14 41
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	6 40 41 58
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD	6 14 18
PM_THRMTRIP_L	CPU_45S	CPU_8MTL	PM_THRMTRIP_L	6 14 41
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	6 12 21
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	6 12
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2..0>	6
CPU_VID	CPU_45S	CPU_VID	CPU_VIDSOUT	8 58
CPU_VID	CPU_45S	CPU_VID	CPU_VIDSCLK	8 58
CPU_VID	CPU_45S	CPU_VID	CPU_VIDALERT_L	8 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	9 58
CPU_MEM_VREF		MEM_12MTL	CPU_DIMMA_VREFDQ	7 22
CPU_MEM_VREF		MEM_12MTL	CPU_DIMMB_VREFDQ	7 22
CPU_MEM_VREF		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A	22 23 24 85 92
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_B	22 25 26 85
CPU_MEM_VREF		MEM_PWR	PP0V75_S3_MEM_VREFCA	22 23 24 25 26 85 89 92
CPU_MEM_VREF		MEM_PWR	PP0V75_S3_MEM_VREFCA	22 23 24 25 26 85 89 92
PCIE_D2R_GPU	PEG_80D	PEG3_D2R	PEG_D2R_C_P<7..0>	68 70
PCIE_D2R_GPU	PEG_80D	PEG3_D2R	PEG_D2R_C_N<7..0>	68 70
PCIE_D2R_GPU	PEG_80D	PEG3_D2R	PEG_D2R_P<7..0>	70 85
PCIE_D2R_GPU	PEG_80D	PEG3_D2R	PEG_D2R_N<7..0>	70 85
PCIE_R2D_GPU	PEG_80D	PEG3_R2D	PEG_R2D_C_P<7..0>	68 70 85
PCIE_R2D_GPU	PEG_80D	PEG3_R2D	PEG_R2D_C_N<7..0>	68 70 85
PCIE_R2D_GPU	PEG_80D	PEG3_R2D	PEG_R2D_P<7..0>	70
PCIE_R2D_GPU	PEG_80D	PEG3_R2D	PEG_R2D_N<7..0>	70
PCIE_D2R_SSD	CPU_85D	PEG3_D2R	PCIE_SSD_D2R_P<3..0>	5 34 85
PCIE_D2R_SSD	CPU_85D	PEG3_D2R	PCIE_SSD_D2R_N<3..0>	5 34 85
PCIE_R2D_SSD	CPU_85D	PEG3_R2D	PCIE_SSD_R2D_C_P<3..0>	5 34 85
PCIE_R2D_SSD	CPU_85D	PEG3_R2D	PCIE_SSD_R2D_C_N<3..0>	5 34 85
	CPU_85D	PEG3_R2D	PCIE_SSD_R2D_P<3..0>	34
	CPU_85D	PEG3_R2D	PCIE_SSD_R2D_N<3..0>	34
PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE_TBT_D2R_P<3..0>	5 28 85
PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE_TBT_D2R_N<3..0>	5 28 85
	CPU_85D	PEG_D2R	PCIE_TBT_D2R_C_P<3..0>	28 87
	CPU_85D	PEG_D2R	PCIE_TBT_D2R_C_N<3..0>	28 87
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE_TBT_R2D_P<3..0>	28 87
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE_TBT_R2D_N<3..0>	28 87
	CPU_85D	PEG_R2D	PCIE_TBT_R2D_C_P<3..0>	5 28 85
	CPU_85D	PEG_R2D	PCIE_TBT_R2D_C_N<3..0>	5 28 85

DP AUX NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DP_IG_AUX	DP_85D	DISPLAYPORT	DPA_IG_AUX_CH_P	12 83 85
DP_IG_AUX	DP_85D	DISPLAYPORT	DPA_IG_AUX_CH_N	12 83 85
DP_IG_AUX	DP_85D	DISPLAYPORT	DPB_IG_AUX_CH_P	12 83 85
DP_IG_AUX	DP_85D	DISPLAYPORT	DPB_IG_AUX_CH_N	12 83 85

DP / HDMI NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	28 76 97
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	28 76 97
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	28 97
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	28 97
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	28 76 97
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	28 76 97
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	28 97
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	28 97
TBTSNK_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_P	28 97
TBTSNK_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_N	28 97
	DP_85D		DP_TBTSNK0_AUXCH_C_P	28 83 97
	DP_85D		DP_TBTSNK0_AUXCH_C_N	28 83 97
TBTSNK_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_P	28 97
TBTSNK_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_N	28 97
	DP_85D		DP_TBTSNK1_AUXCH_C_P	28 83 97
	DP_85D		DP_TBTSNK1_AUXCH_C_N	28 83 97

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?
SATA_2OTHER	*	=4X_DIELECTRIC	?
SATA_RCOMP	*	=6X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
SATA_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
SATA_RCOMP	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	=SAME	*	SATA_2SAME
SATA_R2D	SATA_D2R	*	SATA_TXRX
SATA_*	*	*	SATA_2OTHER

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?
USB_RBIAS	*	=6X_DIELECTRIC	?
BT_WAKE	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=6X_DIELECTRIC	?
USB_RBIAS	TOP,BOTTOM	=10X_DIELECTRIC	?
BT_WAKE	TOP,BOTTOM	=6X_DIELECTRIC	?

USB 3.0 INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
USB3_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	=SAME	*	USB3_2SAME
USB3_R2D	USB3_D2R	*	USB3_TXRX
USB3_*	*	*	USB3_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.
NOTE: Latest Intel DG calls out 50ohms SE for sys clocks

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SATA_85D	SATA_R2D	NC_SATA_A_R2D_CP	11 87
	SATA_85D	SATA_R2D	NC_SATA_A_R2D_CN	11 87
T277	SATA_85D	SATA_D2R	NC_SATA_A_D2RP	11 87
T277	SATA_85D	SATA_D2R	NC_SATA_A_D2RN	11 87
T292	SATA_85D	SATA_R2D	NC_SATA_B_R2D_CP	11 87
T292	SATA_85D	SATA_R2D	NC_SATA_B_R2D_CN	11 87
T300	SATA_85D	SATA_D2R	NC_SATA_B_D2RP	11 87
T300	SATA_85D	SATA_D2R	NC_SATA_B_D2RN	11 87
T213 PCH_SATA_RCOMP	SATA_45SE	SATA_RCOMP	PCH_SATA_RCOMP	11
	USB_EXTA	USB_85D	USB_EXTA_P	13 37
	USB_EXTA	USB_85D	USB_EXTA_N	13 37
T243	USB_EXTA	USB_85D	USB_EXTA_MUXED_P	37
T243	USB_EXTA	USB_85D	USB_EXTA_MUXED_N	37
T243	USB_EXTA	USB_85D	USB_LT1_P	37
T243	USB_EXTA	USB_85D	USB_LT1_N	37
	USB_NC	USB_85D	NC_USB_EXTCP	13 87
	USB_NC	USB_85D	NC_USB_EXTCN	13 87
T238	USB_NC	USB_85D	NC_USB_SDP	13 87
T238	USB_NC	USB_85D	NC_USB_SDN	13 87
T277		CPU_45S	CPU_ITP	SMC_DEBUGPRT_RX_L	37 40 41
T274		CPU_45S	CPU_ITP	SMC_DEBUGPRT_TX_L	37 40 41
	USB_SMC	USB_85D	USB	NC_USB_SMCP	87
	USB_SMC	USB_85D	USB	NC_USB_SMCN	87
T238	USB_NC	USB_85D	USB	NC_USB_6P	13 87
T238	USB_NC	USB_85D	USB	NC_USB_6N	13 87
T238	USB_NC	USB_85D	USB	NC_USB_7P	13 87
T238	USB_NC	USB_85D	USB	NC_USB_7N	13 87
	USB_EXTB	USB_85D	USB	USB_EXTB_P	13 81 86
	USB_EXTB	USB_85D	USB	USB_EXTB_N	13 81 86
T259	USB_NC	USB_85D	USB	NC_USB_EXTDP	13 87
T259	USB_NC	USB_85D	USB	NC_USB_EXTDN	13 87
	USB_BT	USB_85D	USB	USB_BT_P	13 33
	USB_BT	USB_85D	USB	USB_BT_N	13 33
		USB_85D	USB	USB_BT_CONN_P	33 86
		USB_85D	USB	USB_BT_CONN_N	33 86
T288	USB_NC	USB_85D	USB	NC_USB_IRP	13 87
T288	USB_NC	USB_85D	USB	NC_USB_IRN	13 87
T289	USB_TPAD	USB_85D	USB	USB_TPAD_P	13 38 86
T289	USB_TPAD	USB_85D	USB	USB_TPAD_N	13 38 86
T302		USB_85D	USB	USB_TPAD_R_P	
T301		USB_85D	USB	USB_TPAD_R_N	
	PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	13
T222	USB3_EXTA_RX	USB_85D	USB3_D2R	USB3_EXTA_D2R_P	13 37
T223	USB3_EXTA_RX	USB_85D	USB3_D2R	USB3_EXTA_D2R_N	13 37
T240		USB_85D	USB3_D2R	USB3_EXTA_D2R_C_P	
T240		USB_85D	USB3_D2R	USB3_EXTA_D2R_C_N	
T223	USB3_EXTA_TX	USB_85D	USB3_R2D	USB3_EXTA_R2D_P	37
T222	USB3_EXTA_TX	USB_85D	USB3_R2D	USB3_EXTA_R2D_N	37
T240		USB_85D	USB3_R2D	USB3_EXTA_R2D_C_P	13 37
T240		USB_85D	USB3_R2D	USB3_EXTA_R2D_C_N	13 37
T222	USB3_EXTB_RX	USB_85D	USB3_D2R	USB3_EXTB_D2R_P	13 81 86
T222	USB3_EXTB_RX	USB_85D	USB3_D2R	USB3_EXTB_D2R_N	13 81 86
T240		USB_85D	USB3_D2R	USB3_EXTB_D2R_C_P	
T240		USB_85D	USB3_D2R	USB3_EXTB_D2R_C_N	
T222	USB3_EXTB_TX	USB_85D	USB3_R2D	USB3_EXTB_R2D_P	81 86
T223	USB3_EXTB_TX	USB_85D	USB3_R2D	USB3_EXTB_R2D_N	81 86
T240		USB_85D	USB3_R2D	USB3_EXTB_R2D_C_P	13 81
T240		USB_85D	USB3_R2D	USB3_EXTB_R2D_C_N	13 81
T240	NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RP	13 87
T240	NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RN	13 87
T242		USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CP	13 87
T242		USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CN	13 87
T240	NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RP	13 87
T240	NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RN	13 87
T242		USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CP	13 87
T242		USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CN	13 87

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
T260 SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTC	11 19
T255 SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB	11 19
T255	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB_R	11
T255 SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	19 36
T255 SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	19 28
T255	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	28

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?
SPI3X	*	=3x_DIELECTRIC	?

PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_SE	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_SE	TOP,BOTTOM	=3x_DIELECTRIC	?

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	*	=2X_DIELECTRIC	?
PCIE_TXRX	*	=6X_DIELECTRIC	?
PCIE_2OTHER	*	=4X_DIELECTRIC	?
PCIE_2CLK	*	=7X_DIELECTRIC	?
PCIECLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PCIE_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PCIE_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIECLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_R2D	PCIE_D2R	*	PCIE_TXRX
PCIE_*	*	*	PCIE_2OTHER
PCIE_*	CLK_*	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_2OTHER

PCH Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	LPC_AD	LPC_45S	LPC	LPC AD<3..0>	13 40 82
	LPC_FRAME_L	LPC_45S	LPC	LPC FRAME L	13 40 82
	SMBUS_PCH_CLK	SMB_45S	SMB	SMBUS PCH CLK	13 18 43 81 85 86
	SMBUS_PCH_DATA	SMB_45S	SMB	SMBUS PCH DATA	13 18 43 81 85 86
	SMBUS_PCH_0_CLK	SMB_45S	SMB	SML PCH 0 CLK	13 43
	SMBUS_PCH_0_DATA	SMB_45S	SMB	SML PCH 0 DATA	13 43
	SMBUS_PCH_1_CLK	SMB_45S	SMB	SML PCH 1 CLK	13 43
	SMBUS_PCH_1_DATA	SMB_45S	SMB	SML PCH 1 DATA	13 43
	HDA_BIT_CLK	HDA_45S	HDA	HDA BIT CLK	11 52
		HDA_45S	HDA	HDA BIT CLK R	11
	HDA_SYNC	HDA_45S	HDA	HDA SYNC	11 52
		HDA_45S	HDA	HDA SYNC R	11
		HDA_45S	HDA	HDA RST R L	11
	HDA_RST_L	HDA_45S	HDA	HDA RST L	11 52
	HDA_SDIN0	HDA_45S	HDA	HDA SDIN0	11 52
	HDA_SDIN0_R	HDA_45S	HDA	CS4208 HDA SDOUT0 R	52
	HDA_SDOUT	HDA_45S	HDA	HDA SDOUT	11 52
		HDA_45S	HDA	HDA SDOUT R	11 19
	USB3_SD_R2D	USB3_85D	USB3_R2D	USB3 SD R2D C P	13 20 81 86
	USB3_SD_R2D	USB3_85D	USB3_R2D	USB3 SD R2D C N	13 20 81 86
	USB3_SD_D2R	USB3_85D	USB3_D2R	USB3 SD D2R P	13 20 81 86
	USB3_SD_D2R	USB3_85D	USB3_D2R	USB3 SD D2R N	13 20 81 86
	PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE AP R2D P	33 86
	PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE AP R2D N	33 86
		PCIE_85D	PCIE_R2D	PCIE AP R2D C P	13 33
1804		PCIE_85D	PCIE_R2D	PCIE AP R2D C N	13 33
		PCIE_85D	PCIE_R2D	PCIE AP R2D PI P	
1805		PCIE_85D	PCIE_R2D	PCIE AP R2D PI N	
	PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE AP D2R P	13 20 33
	PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE AP D2R N	13 20 33
1226		PCIE_85D	PCIE_D2R	PCIE AP D2R PI P	86
1227		PCIE_85D	PCIE_D2R	PCIE AP D2R PI N	86
1825	PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE CAMERA R2D P	35 36
1826	PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE CAMERA R2D N	35 36
1827		PCIE_85D	PCIE_R2D	PCIE CAMERA R2D C P	13 36
1828		PCIE_85D	PCIE_R2D	PCIE CAMERA R2D C N	13 36
1829	PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE CAMERA D2R P	13 20 36
1830	PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE CAMERA D2R N	13 20 36
1831		PCIE_85D	PCIE_D2R	PCIE CAMERA D2R C P	35 36
1832		PCIE_85D	PCIE_D2R	PCIE CAMERA D2R C N	35 36
		CLK_LPC_45S	CLK_LPC	LPC CLK33M SMC R	11 19
	PCH_LPC_CLK0	CLK_LPC_45S	CLK_LPC	LPC CLK33M SMC	19 40
1240		CLK_LPC_45S	CLK_LPC	NC LPC CLK33M LPCPLUS R	11 87
1240	PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH CLK33M PCIIN	11 19
1250	PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH CLK14P3M REFCLK	11
1250	PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH CLK33M PCIOUT	11 19
1251	PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M PCH P	11
1251	PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M PCH N	11
1252	PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M TBT P	11 28
1252	PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M TBT N	11 28
1253	PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH CLK96M DOT P	11
1253	PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH CLK96M DOT N	11
1250	PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH CLK100M SATA P	11
1250	PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH CLK100M SATA N	11
	PCIE_CLK100M_ENET	PCIE_85D	CLK_PCIE	PCIE CLK100M SD P	
	PCIE_CLK100M_ENET	PCIE_85D	CLK_PCIE	PCIE CLK100M SD N	
	PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE CLK100M AP P	11 33
	PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE CLK100M AP N	11 33
1250		PCIE_85D	CLK_PCIE	PCIE CLK100M AP CONN P	33 86
1250		PCIE_85D	CLK_PCIE	PCIE CLK100M AP CONN N	33 86
	PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M CAMERA P	11 36
	PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M CAMERA N	11 36
1830		CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M CAMERA C P	35 36
1830		CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M CAMERA C N	35 36
1287	PCIE_CLK100M_FW	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M SSD P	11 34
1287		CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M SSD N	11 34
1837	PCIE_CLK100M_GPU	CLK_PCIE_85D	CLK_PCIE	PEG CLK100M P	11 70 85
1838		CLK_PCIE_85D	CLK_PCIE	PEG CLK100M N	11 70 85

PCH Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
1816	PCH_PM_NET	PCH_45S	PCH_SE	PCH INTRUDER L	11
1816	PCH_PM_NET	PCH_45S	PCH_SE	PCH INTVRMEN L	11
1816	PCH_PM_NET	PCH_45S	PCH_SE	PCH DSWVRMEN	12
1816	PCH_PM_NET	PCH_45S	PCH_SE	PCH SRTCRST L	11
1820	PCH_PM_NET	PCH_45S	PCH_SE	PM RSMRST L	12 67 86
1820	PCH_PM_NET	PCH_45S	PCH_SE	PM SYSRST L	12 19 40 86
1820	PCH_PM_NET	PCH_45S	PCH_SE	PM PCH PWROK	12 19 86 91
1820	PCH_PM_NET	PCH_45S	PCH_SE	PM PCH PWROK	12 19 86 91
1820	PCH_PM_NET	PCH_45S	PCH_SE	PM DSW PWRGD	12 40 86
1820	PCH_PM_NET	PCH_45S	PCH_SE	PM PCH SYS PWROK	12 18 19 40 86
1820	PCH_PM_NET	PCH_45S	PCH_SE	PM PWRBTN L	12 18 40
1820	PCH_PM_NET	PCH_45S	PCH_SE	PM THRMTRIP L R	14 41 42
1820	PCH_PCIE_WAKE	PCH_45S	PCH_SE	PCIE WAKE L	12 33 35 86
1820	PCH_PM_NET	PCH_45S	PCH_SE	PCH RCIN L	14
1836	SPI_MLB	SPI_45S	SPI3X	SPI ALT CLK	
1836	SPI_MLB	SPI_45S	SPI	SPI CLK	50
1836	SPI_MLB	SPI_45S	SPI	SPI CLK R	13 50
1836	SPI_MLB	SPI_45S	SPI3X	SPI MLB CLK	50
1836	SPI_MLB	SPI_45S	SPI3X	SPI SMC CLK	40 50
1836	SPI_MLB	SPI_45S	SPI3X	SPI ALT CS L	
1836	SPI_MLB	SPI_45S	SPI	SPI CS0 L	50
1836	SPI_MLB	SPI_45S	SPI	SPI CS0 R L	13 50
1836	SPI_MLB	SPI_45S	SPI3X	SPI MLB CS L	50
1836	SPI_MLB	SPI_45S	SPI3X	SPI SMC CS L	40 50
1836	SPI_MLB	SPI_45S	SPI3X	SPI ALT IO1 MISO	
1836	SPI_MLB	SPI_45S	SPI	SPI MISO	13 50
1836	SPI_MLB	SPI_45S	SPI	SPI MISO R	50
1836	SPI_MLB	SPI_45S	SPI3X	SPI MLB IO1 MISO	50
1836	SPI_MLB	SPI_45S	SPI3X	SPI SMC MISO	40 50
1836	SPI_MLB	SPI_45S	SPI3X	SPI ALT IO0 MOSI	
1836	SPI_MLB	SPI_45S	SPI	SPI MOSI	50
1836	SPI_MLB	SPI_45S	SPI	SPI MOSI R	13 50
1836	SPI_MLB	SPI_45S	SPI3X	SPI MLB IO0 MOSI	50
1836	SPI_MLB	SPI_45S	SPI3X	SPI SMC MOSI	40 50
1836	SPI_MLB_IO2	SPI_45S	SPI3X	SPI IO<2>	13 50
1836	SPI_MLB_IO2	SPI_45S	SPI3X	SPI MLB IO2 WP L	50
1836	SPI_MLB_IO2	SPI_45S	SPI3X	SPI ALT IO2 WP L	
1836	SPI_MLB_IO3	SPI_45S	SPI3X	SPI IO<3>	13 50
1836	SPI_MLB_IO3	SPI_45S	SPI3X	SPI MLB IO3 HOLD L	50
1836	SPI_MLB_IO3	SPI_45S	SPI3X	SPI ALT IO3 HOLD L	
1836	SPI_TPAD	SPI_45S	SPI	TPAD SPI SCLK	38 85
1836	SPI_TPAD_CS	SPI_45S	SPI	TPAD SPI CS L	38 85
1836	SPI_TPAD	SPI_45S	SPI	TPAD SPI MISO	38 85
1836	SPI_TPAD	SPI_45S	SPI	TPAD SPI MOSI	38 85

SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/18/2014

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PCH Constraints 2

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=2x_DIELECTRIC	?
MEM_CMD2CMD	*	=2x_DIELECTRIC	?
MEM_CMD2CTRL	*	=2x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=2x_DIELECTRIC	?
MEM_CLK2CLK	*	=4x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	?
MEM_2GND	*	=2x_DIELECTRIC	?
MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_DQS2OWNDATA	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CMD	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CTRL2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CLK2CLK	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2OTHERMEM	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	*	*	MEM_2OTHER
MEM_*_DQS_*	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

DDR3 (Memory Down):

DQ signals should be matched within 0.508mm of associated DQS pair
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Double checked with Doc#486985 Chief River SFF Platform DG: Memory Down
SOURCE: Need to re-confirm CRW DG for memory down (Intel not yet provided)

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK_P<0>	7 23 27
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK_N<0>	7 23 27
MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK_P<1>	7 24 27
MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK_N<1>	7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CKE<0>	7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CKE<1>	7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CS_L<0>	7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CS_L<1>	7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_ODT<0>	7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_ODT<1>	7 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L	7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L	7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L	7 23 24 27
MEM_A_DATA_0	MEM_45S	MEM_A_DATA_0	MEM_A_DQ<7..0>	7 23 24
MEM_A_DATA_1	MEM_45S	MEM_A_DATA_1	MEM_A_DQ<15..8>	7 23 24
MEM_A_DATA_2	MEM_45S	MEM_A_DATA_2	MEM_A_DQ<23..16>	7 23 24
MEM_A_DATA_3	MEM_45S	MEM_A_DATA_3	MEM_A_DQ<31..24>	7 23 24
MEM_A_DATA_4	MEM_45S	MEM_A_DATA_4	MEM_A_DQ<39..32>	7 23 24
MEM_A_DATA_5	MEM_45S	MEM_A_DATA_5	MEM_A_DQ<47..40>	7 23 24
MEM_A_DATA_6	MEM_45S	MEM_A_DATA_6	MEM_A_DQ<55..48>	7 23 24
MEM_A_DATA_7	MEM_45S	MEM_A_DATA_7	MEM_A_DQ<63..56>	7 23 24
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A_DQS_P<0>	7 23 24
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A_DQS_N<0>	7 23 24
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A_DQS_P<1>	7 23 24
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A_DQS_N<1>	7 23 24
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A_DQS_P<2>	7 23 24
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A_DQS_N<2>	7 23 24
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A_DQS_P<3>	7 23 24
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A_DQS_N<3>	7 23 24
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A_DQS_P<4>	7 23 24
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A_DQS_N<4>	7 23 24
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A_DQS_P<5>	7 23 24
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A_DQS_N<5>	7 23 24
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A_DQS_P<6>	7 23 24
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A_DQS_N<6>	7 23 24
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A_DQS_P<7>	7 23 24
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A_DQS_N<7>	7 23 24
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK_P<0>	7 25 27
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK_N<0>	7 25 27
MEM_B_CLK1	MEM_72D	MEM_CLK	MEM_B_CLK_P<1>	7 26 27
MEM_B_CLK1	MEM_72D	MEM_CLK	MEM_B_CLK_N<1>	7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CKE<0>	7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CKE<1>	7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CS_L<0>	7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CS_L<1>	7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_ODT<0>	7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_ODT<1>	7 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0>	7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L	7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L	7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L	7 25 26 27
MEM_B_DATA_0	MEM_45S	MEM_B_DATA_0	MEM_B_DQ<7..0>	7 25 26
MEM_B_DATA_1	MEM_45S	MEM_B_DATA_1	MEM_B_DQ<15..8>	7 25 26
MEM_B_DATA_2	MEM_45S	MEM_B_DATA_2	MEM_B_DQ<23..16>	7 25 26
MEM_B_DATA_3	MEM_45S	MEM_B_DATA_3	MEM_B_DQ<31..24>	7 25 26
MEM_B_DATA_4	MEM_45S	MEM_B_DATA_4	MEM_B_DQ<39..32>	7 25 26
MEM_B_DATA_5	MEM_45S	MEM_B_DATA_5	MEM_B_DQ<47..40>	7 25 26
MEM_B_DATA_6	MEM_45S	MEM_B_DATA_6	MEM_B_DQ<55..48>	7 25 26
MEM_B_DATA_7	MEM_45S	MEM_B_DATA_7	MEM_B_DQ<63..56>	7 25 26
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B_DQS_P<0>	7 25 26
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B_DQS_N<0>	7 25 26
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B_DQS_P<1>	7 25 26
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B_DQS_N<1>	7 25 26
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B_DQS_P<2>	7 25 26
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B_DQS_N<2>	7 25 26
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B_DQS_P<3>	7 25 26
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B_DQS_N<3>	7 25 26
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B_DQS_P<4>	7 25 26
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B_DQS_N<4>	7 25 26
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B_DQS_P<5>	7 25 26
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B_DQS_N<5>	7 25 26
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B_DQS_P<6>	7 25 26
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B_DQS_N<6>	7 25 26
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B_DQS_P<7>	7 25 26
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B_DQS_N<7>	7 25 26
		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A	22 23 24 85 89
		MEM_PWR	PP0V75_S3_MEM_VREFCA	22 23 24 25 26 85 89
		MEM_PWR	PP1V35_S3_MEM	22 23 24 25 26 27 45 84

SYNC_MASTER=SIDLE_J45 SYNC_DATE=12/10/2012

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Memory Constraints

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SOURCE: Bill Cornelius's Thunderbolt Routing Notes

TBT_DP Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	*	=3X_DIELECTRIC	?
TBTDP_TXRX	*	=6X_DIELECTRIC	?
TBTDP_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_*	=SAME	*	TBTDP_2SAME
TBTDP_R2D	TBTDP_D2R	*	TBTDP_TXRX
TBTDP_*	*	*	TBTDP_2OTHER

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_C_P<1..0>	28 31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_C_N<1..0>	28 31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_P<1..0>	31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_N<1..0>	31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1>	28 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1>	28 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1>	31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1>	31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1>	31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1>	31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3>	28 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3>	28 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3>	31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3>	31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_P<0>	31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_N<0>	31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_P<0>	28 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_N<0>	28 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_P<1>	31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_N<1>	31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_P<1>	28 31 87
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_N<1>	28 31 87
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R1_AUXDDC_P	31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R1_AUXDDC_N	31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_P	28 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_N	28 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_P	31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_N	31
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_P<1..0>	28 32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_N<1..0>	28 32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_P<1..0>	32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_N<1..0>	32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1>	28 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1>	28 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1>	32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1>	32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>	32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>	32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3>	28 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3>	28 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3>	32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3>	32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<0>	32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<0>	32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<0>	28 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<0>	28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<1>	32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<1>	32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<1>	28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<1>	28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_P	32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_N	32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_P	28 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_N	28 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_P	32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_N	32

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_P	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_N	
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK	28
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI	28
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO	28
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L	28

Only used on hosts supporting Thunderbolt video-in

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P	35 36
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N	35 36
	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE	35 36
F101	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L	35 36
F102		S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT	36
F103	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L	35 36
F104	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L	35 36
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L	35 36
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0>	35 36
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1>	35 36
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2>	35 36
F105	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0>	35 36
	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0>	35 36
F106	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1>	35 36
F107	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1>	35 36
F108	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0>	35 36
F109	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1>	35 36
F147	S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0>	35 36
	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0>	35 36
	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8>	35 36
F127	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P	35 36
F128	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N	35 36
F129		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P	36 86
F130		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N	36 86
F134	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P	35 36
F135	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N	35 36
F137		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P	36 86
F138		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N	36 86
F145			S2_MEM_PWR	PP1V35_CAM	35 36
F146			S2_MEM_PWR	PP0V675_CAM_VREF	35 36
F148			S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA	36
F149			S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ	36

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SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_2_S3_SCL	SMB_45S	SMB	SMBUS_SMC_2_S3_SCL	38 40 43 86
SMBUS_SMC_2_S3_SDA	SMB_45S	SMB	SMBUS_SMC_2_S3_SDA	38 40 43 86
SMBUS_SMC_1_S0_SCL	SMB_45S	SMB	SMBUS_SMC_1_S0_SCL	40 43 48
SMBUS_SMC_1_S0_SDA	SMB_45S	SMB	SMBUS_SMC_1_S0_SDA	40 43 48
SMBUS_SMC_0_S0_SCL	SMB_45S	SMB	SMBUS_SMC_0_S0_SCL	36 40 43 48 69 76 85 86
SMBUS_SMC_0_S0_SDA	SMB_45S	SMB	SMBUS_SMC_0_S0_SDA	36 40 43 48 69 76 85 86
SMBUS_SMC_5_SCL	SMB_45S	SMB	SMBUS_SMC_5_g3_SCL	40 43 56 57 86
SMBUS_SMC_5_SDA	SMB_45S	SMB	SMBUS_SMC_5_G3_SDA	40 43 56 57 86
SMBUS_SMC_3_SCL	SMB_45S	SMB	NC_SMBUS_SMC_3_SCL	40 42
SMBUS_SMC_3_SDA	SMB_45S	SMB	NC_SMBUS_SMC_3_SDA	40 42

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	1TO1_DIFFPAIR		CHGR_CSI_P	57
	1TO1_DIFFPAIR		CHGR_CSI_N	57
	1TO1_DIFFPAIR		CHGR_CSO_P	57
	1TO1_DIFFPAIR		CHGR_CSO_N	57

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_50S	*	=1:1_DIFFPAIR	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_50S	*	=1:1_DIFFPAIR	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
THERM_45S_CPUVRISNS1	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.2 MM	0.2 MM
THERM_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SENSE_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2X_DIELECTRIC	?
THERM	*	=2X_DIELECTRIC	?
AUDIO	*	=2X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
GND	PCIE_*	*	GND_P2MM
GND	SATA_*	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SB_POWER	SATA_*	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 MM OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.1 MM	500 MIL		
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
USB3_85D	TOP			0.1 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
1TO1_DIFFPAIR	*	1:1_DIFFPAIR

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_GPUVR	*	Y	0.300 MM	0.200 MM	3.000 MM	0.400 MM	0.200 MM

AMD Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
1640 SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GPUFB_CS_P	47 73
1641	THERM_1TO1_45S	THERM	GPUFB_CS_N	47 73
1642 SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GPU_TDIODE_P	48 76
1643	THERM_1TO1_45S	THERM	GPU_TDIODE_N	48 76
1644 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	GPU_VDDCISENSE_P	
1645 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	GPU_VDDCISENSE_N	
1646 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	GPU_VDDCI_SENSE_XW_P	80
1647 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	GPU_VDDCI_SENSE_XW_N	80
1648 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	GPUVCORE_SENSE_P	79
1649 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	GPUVCORE_SENSE_N	79
1650 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PP0V95_S0GPU_R_P	47
1651 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PP0V95_S0GPU_R_N	47
1652 SENSE_DIFFPAIR	THERM_1TO1_45S	SENSE	VSNS_GPU_0V95_XW_P	73
1653	THERM_1TO1_45S	SENSE	VSNS_GPU_0V95_XW_N	73
1654 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	VDDCIS0_CS_R_P	47
1655	SENSE_1TO1_45S	SENSE	VDDCIS0_CS_R_N	47
1656 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	GPUFB_CS_R_P	47
1657	SENSE_1TO1_45S	SENSE	GPUFB_CS_R_N	47
1658 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	VSNS_GPU_VDDC_P	71 79 85
1659 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	VSNS_GPU_VDDC_N	71 79
1660 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	VSNS_GPU_VDDI_P	71 80 85
1661 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	VSNS_GPU_VDDI_N	71 80
1662 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V8_GPU_R_P	
1663 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V8_GPU_R_N	
1664 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V8_GPU_P	
1665 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V8_GPU_N	
1666 SENSE_DIFFPAIR	THERM_1TO1_45S	SENSE	VSNS_GPU_FB_XW_P	73
1667	THERM_1TO1_45S	SENSE	VSNS_GPU_FB_XW_N	73

X425G Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
1424 SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_CPUDDR_P	46 66
1425 SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_CPUDDR_N	46 66
1422	THERM_1TO1_45S	THERM	ISNS_CPU_DDR_R_P	46
1423	THERM_1TO1_45S	THERM	ISNS_CPU_DDR_R_N	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUTHMSNS_D2_P	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUTHMSNS_D2_N	48
1422 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCD_PANEL_P	46 69 96
1423 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCD_PANEL_N	46 69 96
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	DDR3THMSNS_D1_P	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	DDR3THMSNS_D1_N	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	FINTHMSNS_D_P	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	FINTHMSNS_D_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_P	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_N	45
1419	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_R_P	45
1420	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_R_N	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_N	
	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_R_P	46
	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_R_N	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N	63
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P	63
1553 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCD_PANEL_N	46 69 96
1552 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCD_PANEL_P	46 69 96
1523	SENSE_1TO1_45S	SENSE	ISNS_PCH_R_P	45
1524	SENSE_1TO1_45S	SENSE	ISNS_PCH_R_N	45
1522 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_TPAD_P	45
1520 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_TPAD_N	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER5V_P	44
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER5V_N	44
1514 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER3V3_P	44
1515 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER3V3_N	44
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P	44
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N	44
	SENSE_1TO1_45S	SENSE	CPUVR_ISNS_P	45
	SENSE_1TO1_45S	SENSE	CPUVR_ISNS_N	45
1516 SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05_GPU_PEX_IOVDD_SNS_P	
1517 SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05_GPU_PEX_IOVDD_SNS_N	
			DIFFERENTIAL_PAIR	
1630 SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1 CPUVR_ISNS1_P	45 59
1631 SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1 CPUVR_ISNS1_N	45 59
1628 SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2 CPUVR_ISNS2_P	45 59
1629 SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2 CPUVR_ISNS2_N	45 59
1622 SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3 CPUVR_ISNS3_P	45 59
1620 SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3 CPUVR_ISNS3_N	45 59
1432 SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUVR_ISUM_R_P	45
1430 SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUVR_ISUM_R_N	45
1497 SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_P	79 96
1498 SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_N	79 96
1502 SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_P	79 96
1503 SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_N	79 96
1409 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_N	45
1408 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_P	45
1407	AUDIODIFF	AUDIO	ISNS_TBT_R_N	45
1406	AUDIODIFF	AUDIO	ISNS_TBT_R_P	45
1444 SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_SSD_P	45
1445	THERM_1TO1_45S	THERM	ISNS_SSD_N	45
1447 SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_SSD_R_P	45
1446	THERM_1TO1_45S	THERM	ISNS_SSD_R_N	45
1449 SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05S0_CS_P	45 62
1450	THERM_1TO1_45S	THERM	P1V05S0_CS_N	45 62
			DIFFERENTIAL_PAIR	
1453 SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05S0_SENSE P1V05S0_SENSE_P	62
1452	THERM_1TO1_45S	THERM	P1V05S0_SENSE P1V05S0_SENSE_N	62
1455 SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_THERMDP	28 48
1454	THERM_1TO1_45S	THERM	TBT_THERMDN	48
1459 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSI_R_P	57
1458	AUDIODIFF	AUDIO	CHGR_CSI_R_N	57
1457 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSO_R_P	57
1456	AUDIODIFF	AUDIO	CHGR_CSO_R_N	57
1637 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	GFXIMVP_ISNS2_P	79
1638 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	GFXIMVP_ISNS2_N	79
1636 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_GPU_P	47
1637 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_GPU_N	47
1634 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PP0V95_S0GPU_P	47 73
1635 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PP0V95_S0GPU_N	47 73
1641 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	VDDCIS0_CS_P	47 80
1640 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	VDDCIS0_CS_N	47 80
1643 SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GPUTHMSNS_D_P	48
1642 SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GPUTHMSNS_D_N	48

X425G Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
1468	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_P	53
1469	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_N	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_N	53
1430	AUDIODIFF	AUDIO	RSUBIN_P	53
1440	AUDIODIFF	AUDIO	RSUBIN_N	53
1441	AUDIODIFF	AUDIO	LSUBIN_P	53
1442	AUDIODIFF	AUDIO	LSUBIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	51 53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N	53
1493	AUDIODIFF	AUDIO	SPKRAMP_RIN_P	53
1492	AUDIODIFF	AUDIO	SPKRAMP_RIN_N	53
1490	AUDIODIFF	AUDIO	SPKRAMP_LIN_P	53
1491	AUDIODIFF	AUDIO	SPKRAMP_LIN_N	53
1836 AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_P	53 55 86
1837 AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_N	53 55 86
1860 AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_P	53 55 86
1859 AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_N	53 55 86
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P	53 55 86
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N	53 55 86
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P	53 55 86
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N	53 55 86
1480 AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_P	
1481 AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_N	
1482 AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	CODEC_HS_MIC_P	51
1483 AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	CODEC_HS_MIC_N	51
1484 AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_L_P	
1485	DIFFPAIR	AUDIO	AUD_MIC_IN1_L_N	
1486	DIFFPAIR	AUDIO	AUD_HS_MIC_P	54 55
1487	DIFFPAIR	AUDIO	AUD_HS_MIC_N	54 55
1488	DIFFPAIR	AUDIO	HS_MIC_P	51 54
1489	DIFFPAIR	AUDIO	HS_MIC_N	51 54
1490	DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_P	
1491	DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_N	
1494 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_P	51 53
1495 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_N	51 53
1496 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_P	51 53
1497 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_N	51 53
SB_POWER			PP3V3_S5	66 67 82 84 85 86 12 14 15 17 18 19 21 31 32 33 41 42
SB_POWER			PP3V3_S0	68 67 68 69 82 83 84 86 11 12 13 14 15 17 18 20 29 34 43 44 45 46 47 48 49 51 52 55
SB_POWER			PP1V35_S3RS0_CPUDDR	6 8 10 21 66 67 84
GND			GND	

SYNC_MASTER=SIDLE_J45 SYNC_DATE=12/10/2012

PAGE TITLE
Project Specific Constraints

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GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?
GDDR5_CMD	*	=3x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?
GDDR5_EDC	*	=7x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR5_CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
GDDR5_DATA	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR5_EDC	TOP,BOTTOM	=7x_DIELECTRIC	?

GDDR5_CMD spacing can be relaxed to 2x per AMD recommendation for x32_4.5G config.

Breakout Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR5_*	*	BGA	GDDR5_BGA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_BGA	*	=1.3x_DIELECTRIC	?

GDDR5 FB A Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
1455	FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_P	72 74
1454	FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_N	72 74
1452	FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_P	72 74
1451	FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_N	72 74
1450	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_A<8..0>	72 74
1449	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_A<8..0>	72 74
1448	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_ABI_L	72 74
1447	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_ABI_L	72 74
1446	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_RAS_L	72 74
1445	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_RAS_L	72 74
1443	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_CAS_L	72 74
1442	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_CAS_L	72 74
1441	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_WE_L	72 74
1440	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_WE_L	72 74
1444	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_CKE_L	72 74
1439	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_CKE_L	72 74
1437	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_CS_L	72 74
1438	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_CS_L	72 74
1436	FB_A0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<0>	72 74
1435	FB_A0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<1>	72 74
1406	FB_A0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<2>	72 74
1400	FB_A0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<3>	72 74
1404	FB_A1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<0>	72 74
1398	FB_A1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<1>	72 74
1399	FB_A1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<2>	72 74
1397	FB_A1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<3>	72 74
1393	FB_A0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<0>	72 74
1390	FB_A0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<1>	72 74
1392	FB_A0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<2>	72 74
1391	FB_A0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<3>	72 74
1389	FB_A1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<0>	72 74
1388	FB_A1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<1>	72 74
1386	FB_A1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<2>	72 74
1385	FB_A1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<3>	72 74
1388	FB_A0_WCLK0	GDDR5_80D	GDDR5_CLK	FB_A0_WCLK_P<0>	72 74
1387	FB_A0_WCLK0	GDDR5_80D	GDDR5_CLK	FB_A0_WCLK_N<0>	72 74
1385	FB_A0_WCLK1	GDDR5_80D	GDDR5_CLK	FB_A0_WCLK_P<1>	72 74
1386	FB_A0_WCLK1	GDDR5_80D	GDDR5_CLK	FB_A0_WCLK_N<1>	72 74
1383	FB_A1_WCLK0	GDDR5_80D	GDDR5_CLK	FB_A1_WCLK_P<0>	72 74
1384	FB_A1_WCLK0	GDDR5_80D	GDDR5_CLK	FB_A1_WCLK_N<0>	72 74
1382	FB_A1_WCLK1	GDDR5_80D	GDDR5_CLK	FB_A1_WCLK_P<1>	72 74
1380	FB_A1_WCLK1	GDDR5_80D	GDDR5_CLK	FB_A1_WCLK_N<1>	72 74
1381	FB_A0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<7..0>	72 74
1372	FB_A0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<15..8>	72 74
1373	FB_A0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<23..16>	72 74
1377	FB_A0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<31..24>	72 74
1379	FB_A1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<7..0>	72 74
1378	FB_A1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<15..8>	72 74
1374	FB_A1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<23..16>	72 74
1372	FB_A1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<31..24>	72 74
1371	FB_A0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A0_RESET_L	
1370	FB_A1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A1_RESET_L	

GDDR5 FB B Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
1473	FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_P	72 75
1474	FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_N	72 75
1472	FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_P	72 75
1471	FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_N	72 75
1470	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_A<8..0>	72 75
1469	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_A<8..0>	72 75
1468	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_ABI_L	72 75
1467	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_ABI_L	72 75
1466	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_RAS_L	72 75
1465	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_RAS_L	72 75
1463	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_CAS_L	72 75
1462	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_CAS_L	72 75
1461	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_WE_L	72 75
1460	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_WE_L	72 75
1464	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_CKE_L	72 75
1459	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_CKE_L	72 75
1457	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_CS_L	72 75
1458	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_CS_L	72 75
1456	FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<0>	72 75
1455	FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<1>	72 75
1436	FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<2>	72 75
1433	FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<3>	72 75
1434	FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<0>	72 75
1430	FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<1>	72 75
1431	FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<2>	72 75
1429	FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<3>	72 75
1425	FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<0>	72 75
1427	FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<1>	72 75
1426	FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<2>	72 75
1424	FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<3>	72 75
1423	FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<0>	72 75
1422	FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<1>	72 75
1421	FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<2>	72 75
1420	FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<3>	72 75
1428	FB_B0_WCLK0	GDDR5_80D	GDDR5_CLK	FB_B0_WCLK_P<0>	72 75
1445	FB_B0_WCLK0	GDDR5_80D	GDDR5_CLK	FB_B0_WCLK_N<0>	72 75
1443	FB_B0_WCLK1	GDDR5_80D	GDDR5_CLK	FB_B0_WCLK_P<1>	72 75
1441	FB_B0_WCLK1	GDDR5_80D	GDDR5_CLK	FB_B0_WCLK_N<1>	72 75
1410	FB_B1_WCLK0	GDDR5_80D	GDDR5_CLK	FB_B1_WCLK_P<0>	72 75
1412	FB_B1_WCLK0	GDDR5_80D	GDDR5_CLK	FB_B1_WCLK_N<0>	72 75
1411	FB_B1_WCLK1	GDDR5_80D	GDDR5_CLK	FB_B1_WCLK_P<1>	72 75
1413	FB_B1_WCLK1	GDDR5_80D	GDDR5_CLK	FB_B1_WCLK_N<1>	72 75
1444	FB_B0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<7..0>	72 75
1443	FB_B0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<15..8>	72 75
1414	FB_B0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<23..16>	72 75
1409	FB_B0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<31..24>	72 75
1408	FB_B1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<7..0>	72 75
1407	FB_B1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<15..8>	72 75
1406	FB_B1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<23..16>	72 75
1405	FB_B1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<31..24>	72 75
1404	FB_B0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B0_RESET_L	
1403	FB_B1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B1_RESET_L	

MUXGFX & DP AUX MUX NET PROPERTIES

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
1480		DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	69 82
1485		DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	69 82
1484		DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0>	69
1483		DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0>	69
1482	DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	69 86
1481	DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	69 86
1480		DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_P	69 82
1479		DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_N	69 82
1477	DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_P	69 86
1476	DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_N	69 86
1349		DP_85D	DISPLAYPORT	DP_INT_EG_AUX_P	76 77 82
1350		DP_85D	DISPLAYPORT	DP_INT_EG_AUX_N	76 77 82
1348	DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_EG_ML_P<3..0>	76 82
1347		DP_85D	DISPLAYPORT	DP_INT_EG_ML_N<3..0>	76 82
1513		DP_85D	DISPLAYPORT	DP_INT_IG_AUX_P	5 82 85
1519		DP_85D	DISPLAYPORT	DP_INT_IG_AUX_N	5 82 85
1518	DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_IG_ML_P<3..0>	5 82 85
1520		DP_85D	DISPLAYPORT	DP_INT_IG_ML_N<3..0>	5 82 85
1838	DP_EG_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_EG_AUXCH_P	76 77 83
1837	DP_EG_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_EG_AUXCH_N	76 77 83
1836	DP_EG_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_EG_AUXCH_P	76 77 83
1834	DP_EG_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_EG_AUXCH_N	76 77 83
1468	TBTSNK_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P	28 89
1469	TBTSNK_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N	28 89
1466		DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P	28 83 89
1465		DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N	28 83 89
1467	TBTSNK_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P	28 89
1464	TBTSNK_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N	28 89
1463		DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P	28 83 89
1462		DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N	28 83 89
1495	DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	28 89
1492	DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	28 89
1493		DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	28 76 89
1491		DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	28 76 89
1488	DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	28 89
1485	DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	28 89
1486		DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	28 76 89
1487		DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	28 76 89

Kepler Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
1844		1:1_DIFFPAIR		GPU_CLK_TEST_RC_P	72
1845		1:1_DIFFPAIR		GPU_CLK_TEST_RC_N	72
1846	GPU_CLK_TEST	1:1_DIFFPAIR		GPU_CLK_TEST_P	72
1847	GPU_CLK_TEST	1:1_DIFFPAIR		GPU_CLK_TEST_N	72
	HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_EG_DATA_P<2..0>	76 81 86
	HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_EG_DATA_N<2..0>	76 81 86
	HDMI_CLK	DP_85D	HDMI_CLK	HDMI_EG_CLK_P	76 81 86
	HDMI_CLK	DP_85D	HDMI_CLK	HDMI_EG_CLK_N	76 81 86

SYNC_MASTER=J45G_AMD SYNC_DATE=07/01/2014

PAGE TITLE

GPU (AMD VENUS) Constraints

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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