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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

J43 MLB SCHEMATIC DVT

REV 6.5.0

4/09/13

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REV

ECN

DESCRIPTION OF REVISION

CK APPD

<REV>

<ECN>

<ECO\_DESCRIPTION>

<ECODATE>

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9800	1	SCHEM,MLB,J43	SCH	CRITICAL	
820-3437	1	PCBF,MLB,J43	PCB	CRITICAL	

DRAWING

TITLE=MLB

ABBREV=DRAWING

LAST\_MODIFIED=Tom Apt 9 20/06/04 2013

PRODUCT SAFETY REQUIREMENTS:

PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.

PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE

NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

DRAWING TITLE

<PART\_DESCRIPTION>

Apple Inc.

Apple

DRAWING NUMBER

<SCH\_NUM>

REVISION

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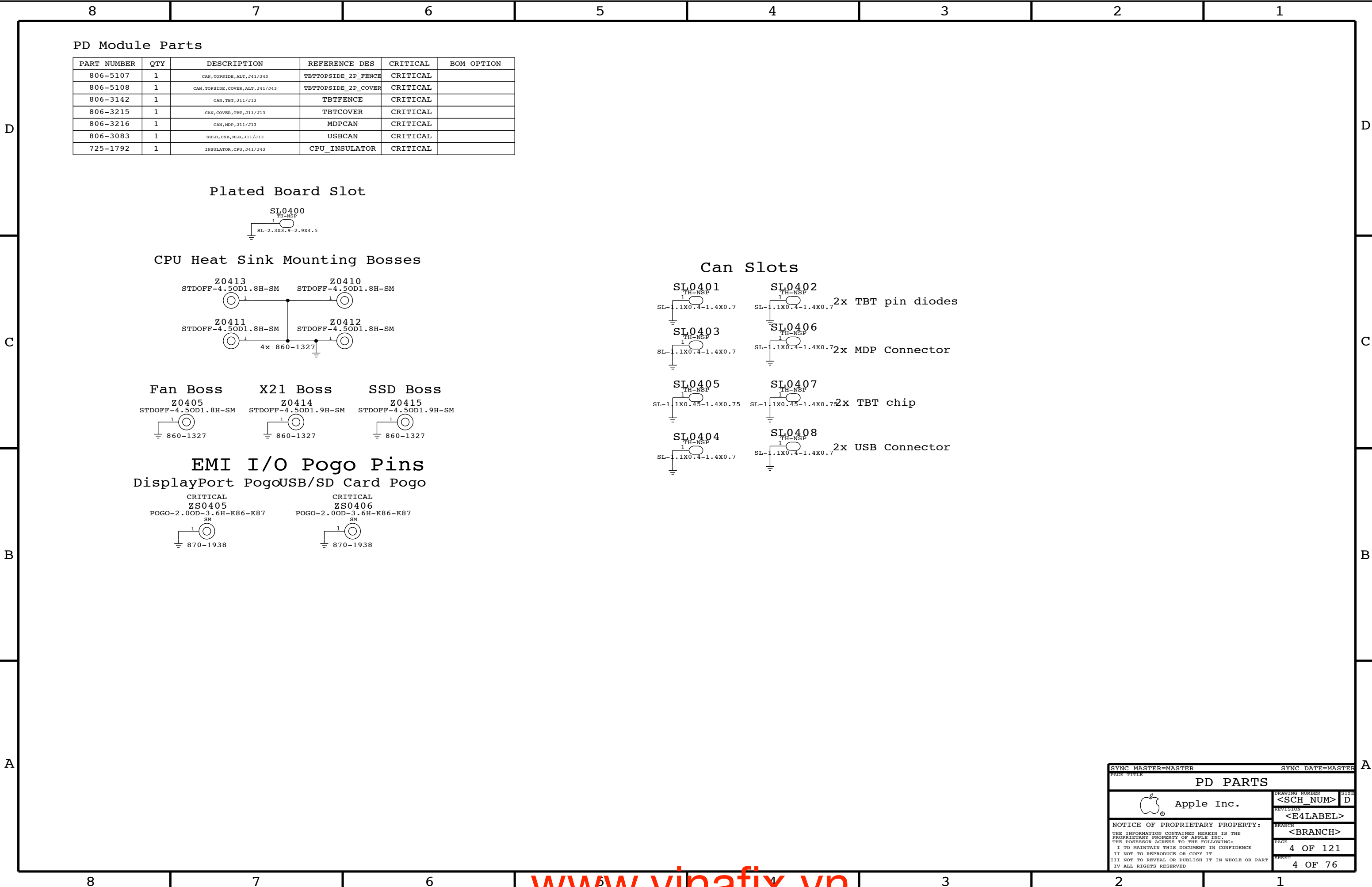
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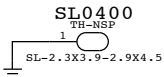




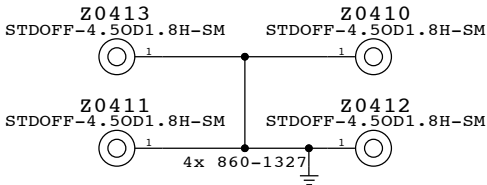
PD Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-5107	1	CAN,TOPSIDE,ALT,J41/J43	TBTTOPSIDE_2P_FENCE	CRITICAL	
806-5108	1	CAN,TOPSIDE,COVER,ALT,J41/J43	TBTTOPSIDE_2P_COVER	CRITICAL	
806-3142	1	CAN,TBT,J11/J13	TBTFENCE	CRITICAL	
806-3215	1	CAN,COVER,TBT,J11/J13	TBTCOVER	CRITICAL	
806-3216	1	CAN,MDP,J11/J13	MDPCAN	CRITICAL	
806-3083	1	SHLD,USB,MLB,J11/J13	USBCAN	CRITICAL	
725-1792	1	INSULATOR,CPU,J41/J43	CPU_INSULATOR	CRITICAL	

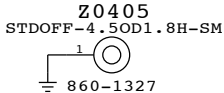
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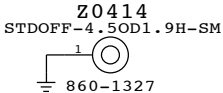
CPU Heat Sink Mounting Bosses



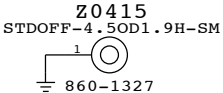
Fan Boss



X21 Boss

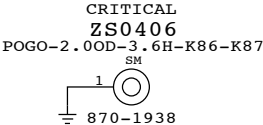
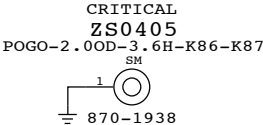


SSD Boss

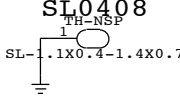
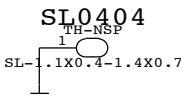
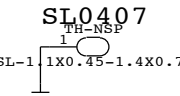
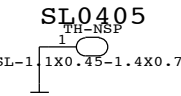
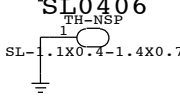
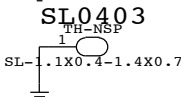
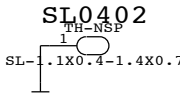
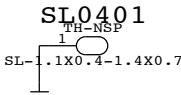


EMI I/O Pogo Pins

DisplayPort PogoUSB/SD Card Pogo



Can Slots




2x TBT pin diodes

2x MDP Connector

2x TBT chip

2x USB Connector

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PD PARTS			
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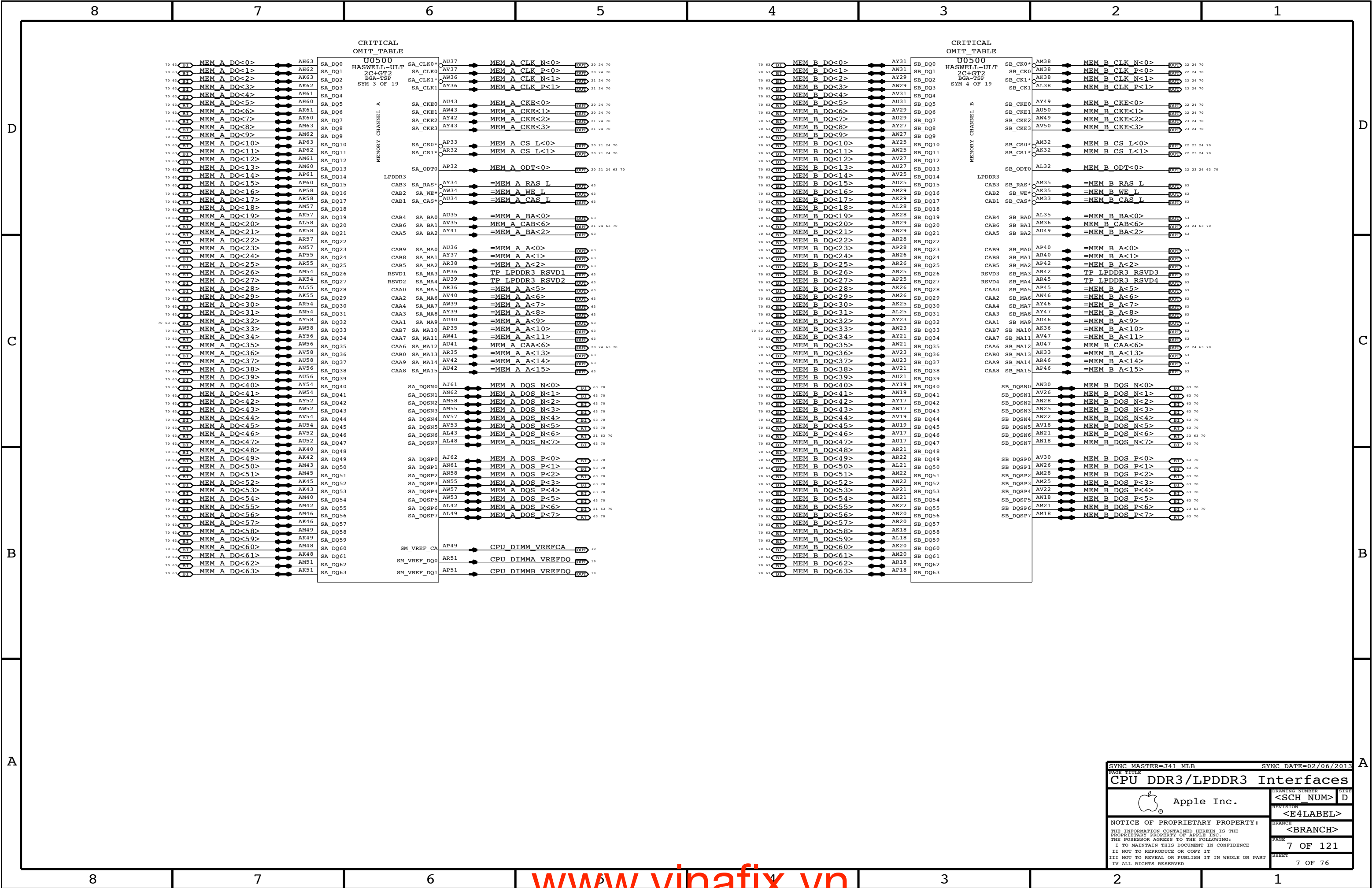


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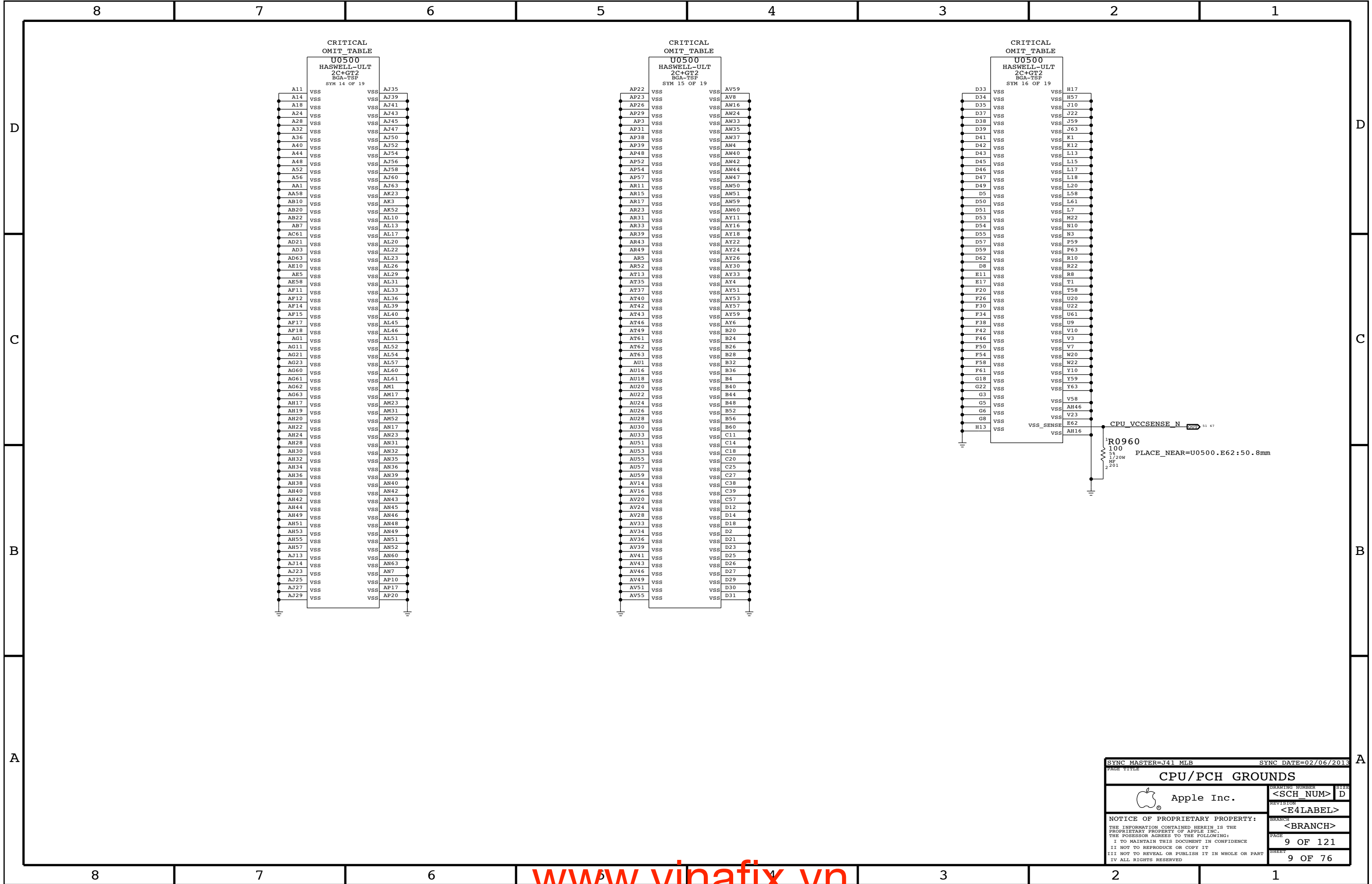
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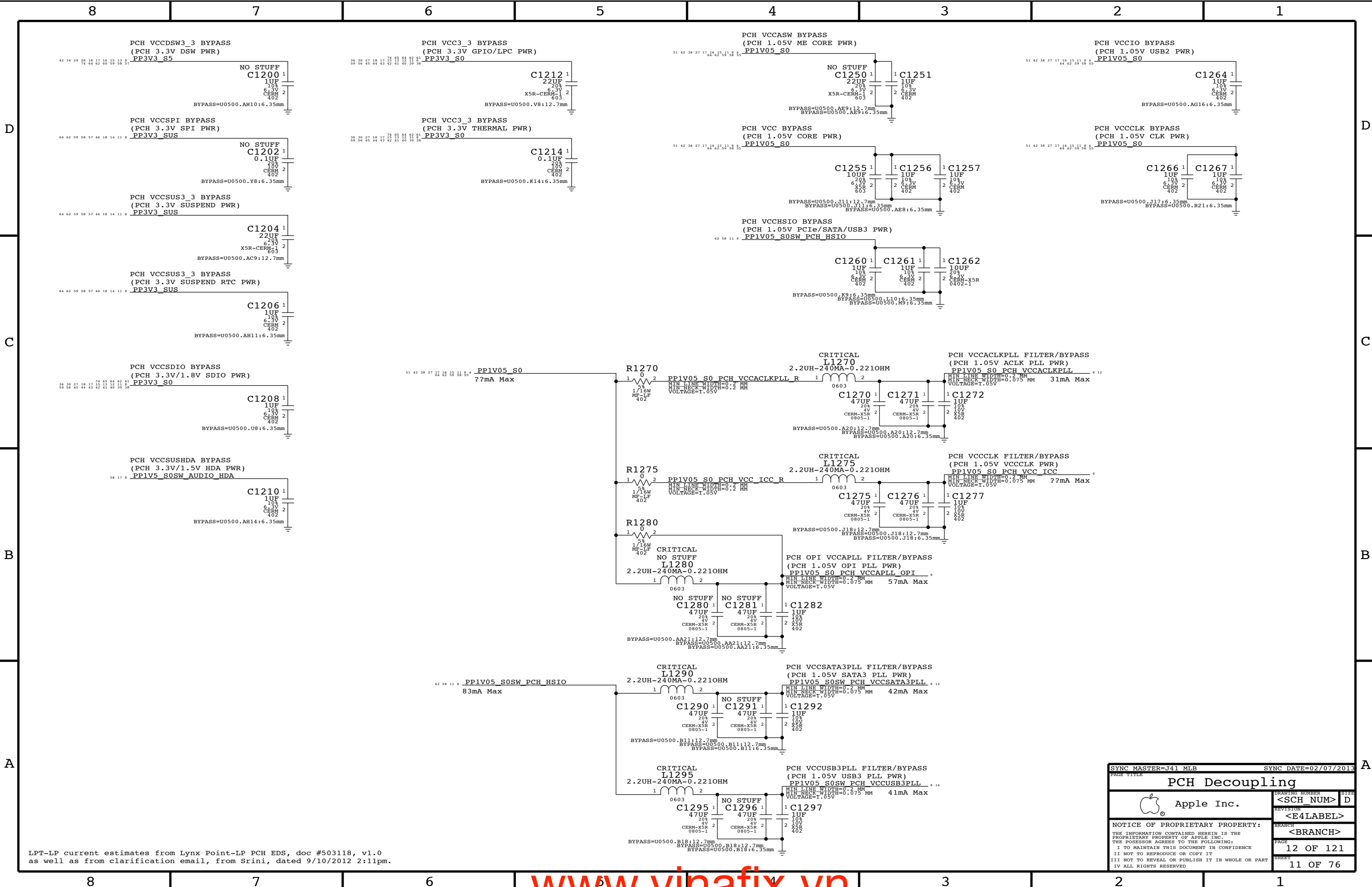







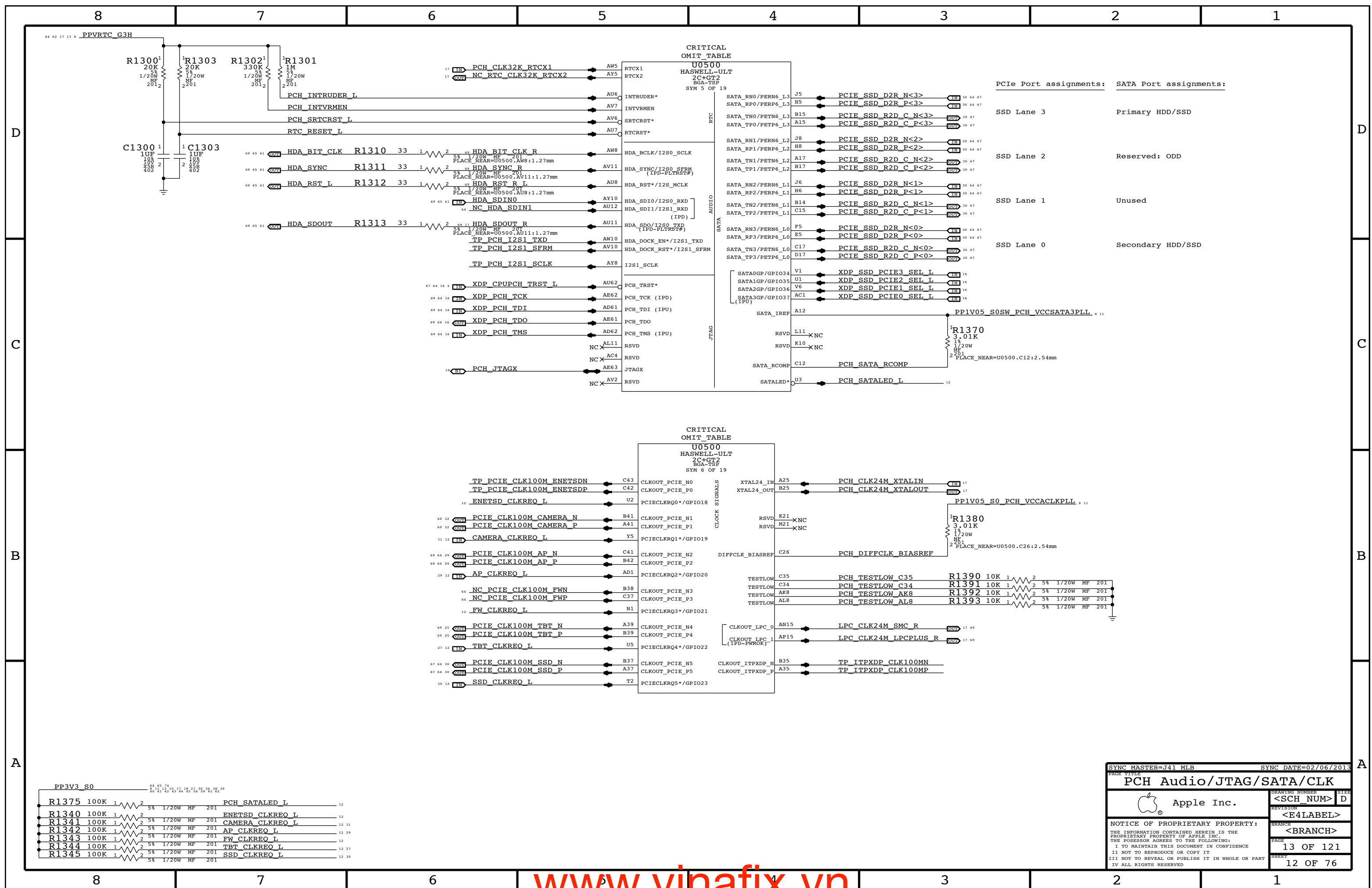


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LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0 as well as from clarification email, from Srinii, dated 9/10/2012 2:11pm.

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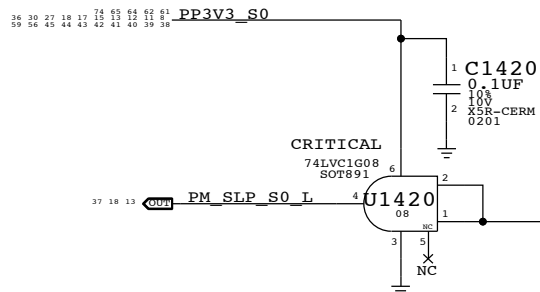
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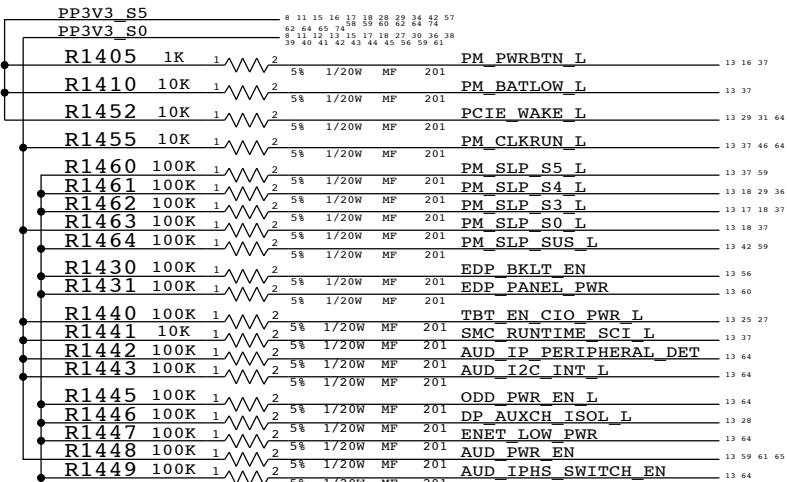
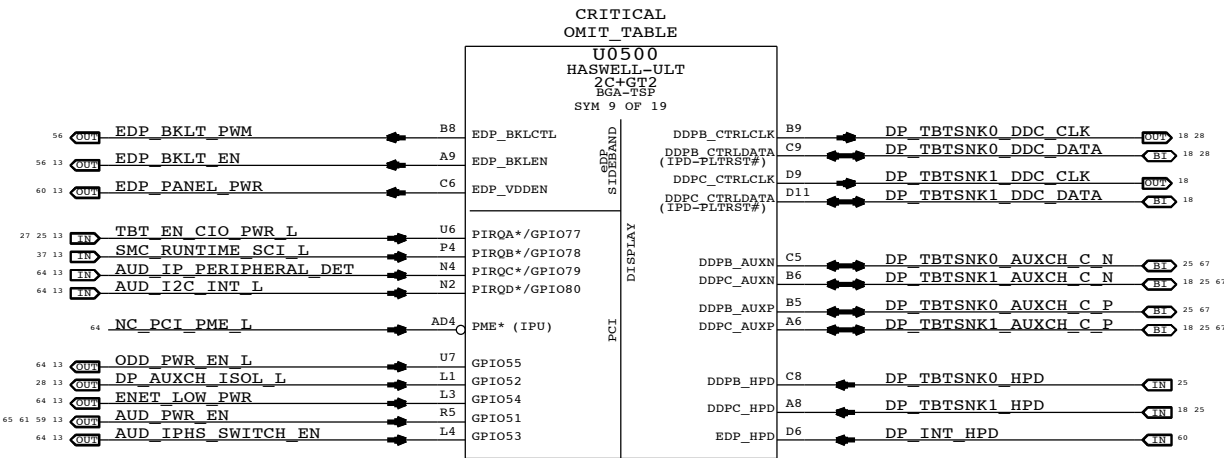
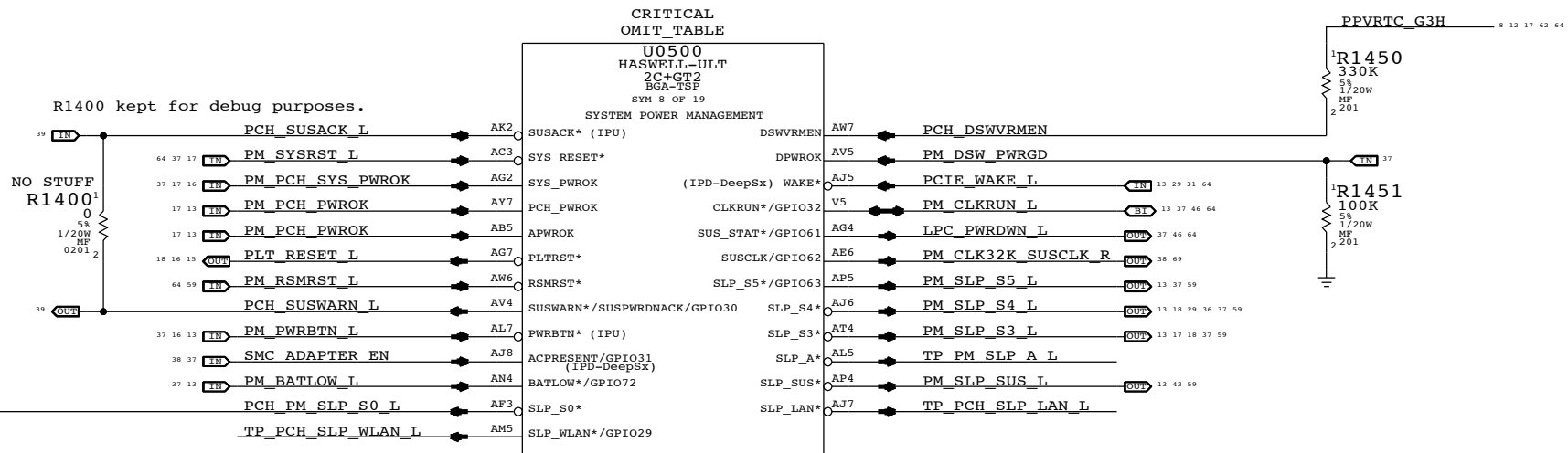
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SLP\_S0# Isolation



SLP\_S0# can be driven high outside of S0  
U1420 ensures signal will only be high in S0.

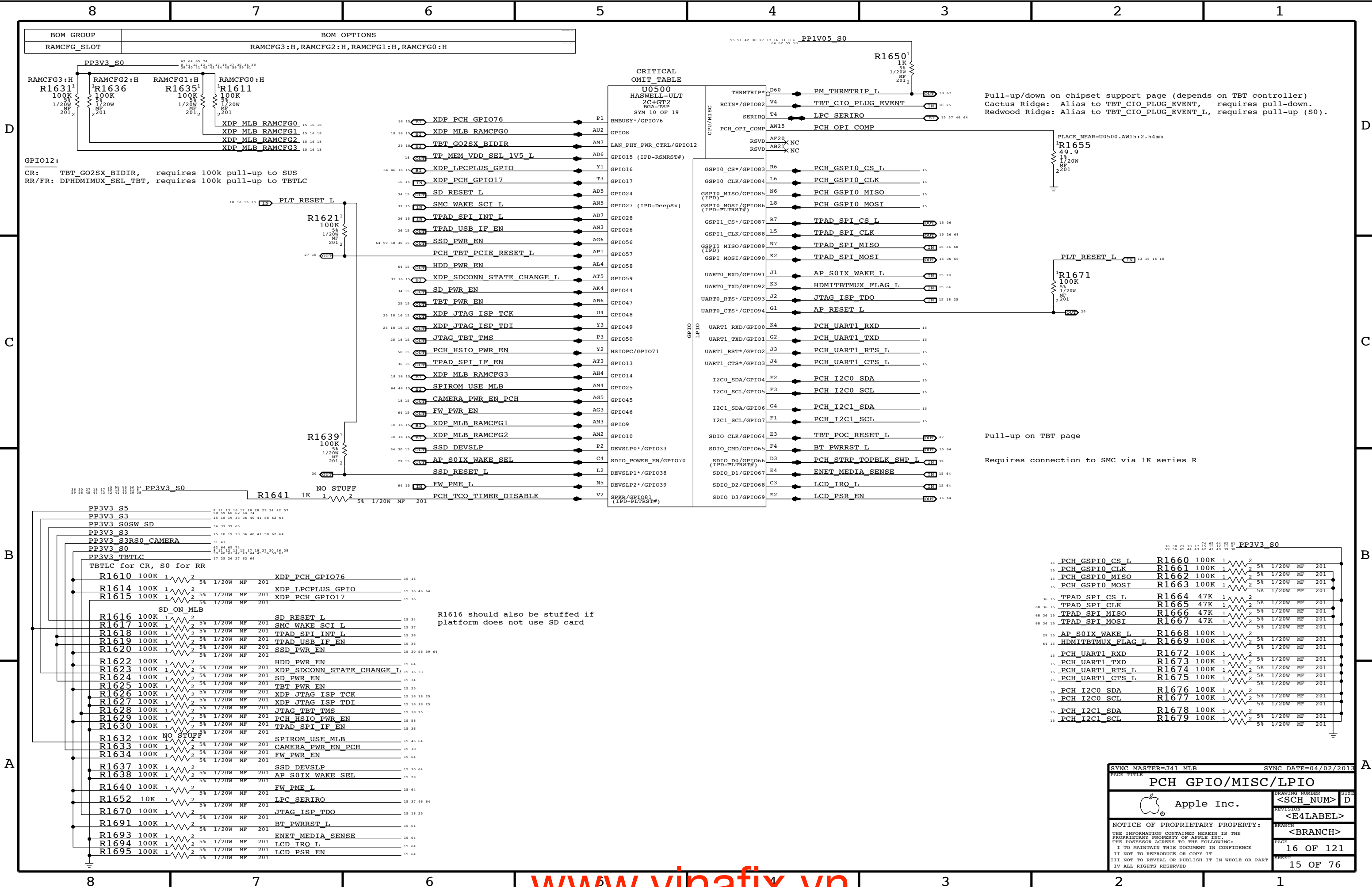


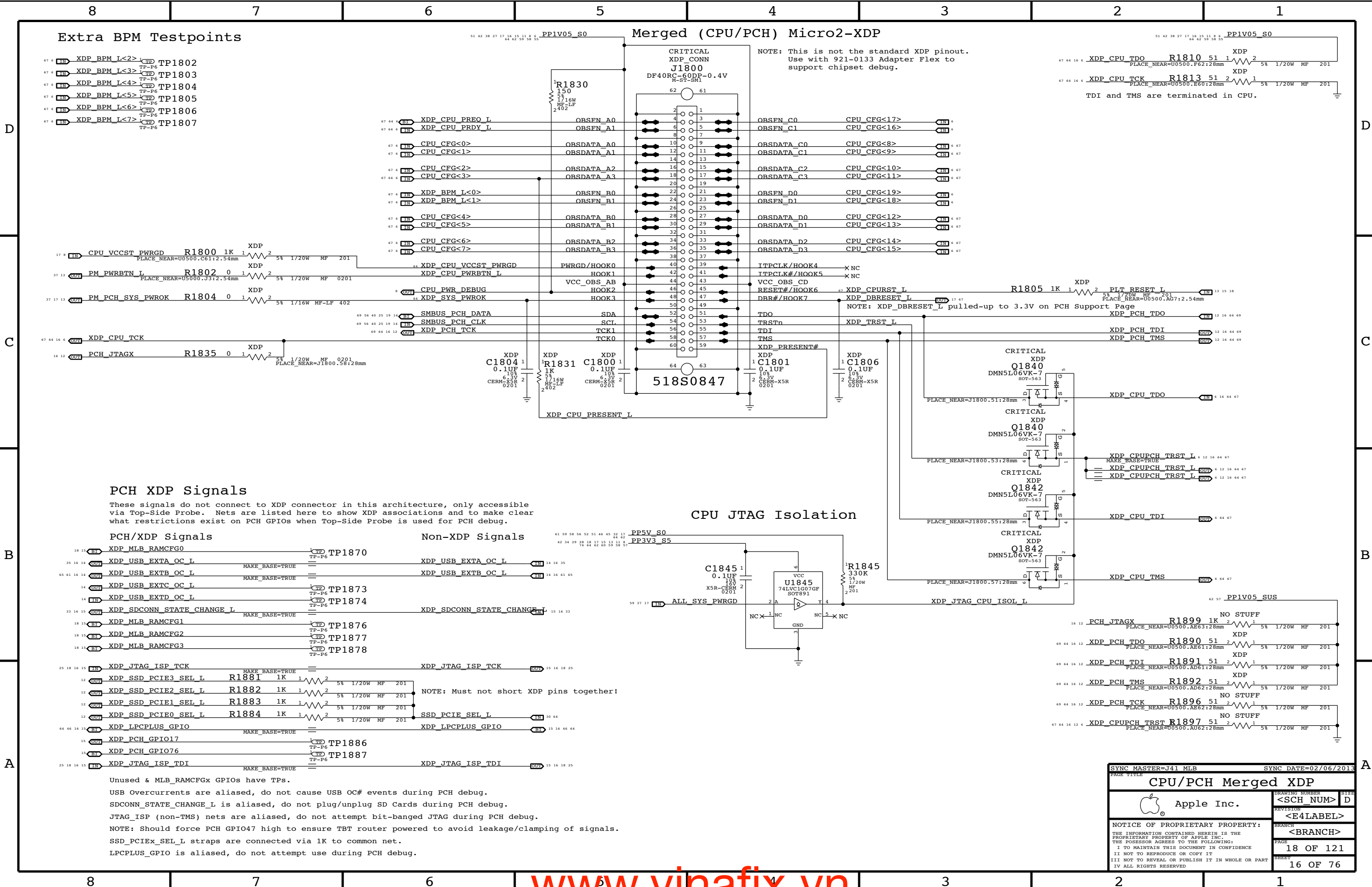
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### Extra BPM Testpoints

- XDP\_BPM\_L<2> TP1802
- XDP\_BPM\_L<3> TP1803
- XDP\_BPM\_L<4> TP1804
- XDP\_BPM\_L<5> TP1805
- XDP\_BPM\_L<6> TP1806
- XDP\_BPM\_L<7> TP1807

### PCH XDP Signals

These signals do not connect to XDP connector in this architecture, only accessible via Top-Side Probe. Nets are listed here to show XDP associations and to make clear what restrictions exist on PCH GPIOs when Top-Side Probe is used for PCH debug.

#### PCH/XDP Signals

- XDP\_MLB\_RAMCFG0 TP1870
- XDP\_USB\_EXT\_A\_OC\_L MAKE\_BASE=TRUE
- XDP\_USB\_EXT\_B\_OC\_L MAKE\_BASE=TRUE
- XDP\_USB\_EXT\_C\_OC\_L TP1873
- XDP\_USB\_EXT\_D\_OC\_L TP1874
- XDP\_SDCONN\_STATE\_CHANGE\_L MAKE\_BASE=TRUE
- XDP\_MLB\_RAMCFG1 TP1876
- XDP\_MLB\_RAMCFG2 TP1877
- XDP\_MLB\_RAMCFG3 TP1878

#### Non-XDP Signals

- XDP\_USB\_EXT\_A\_OC\_L
- XDP\_USB\_EXT\_B\_OC\_L
- XDP\_SDCONN\_STATE\_CHANGE\_L

- XDP\_JTAG\_ISP\_TCK MAKE\_BASE=TRUE
- XDP\_SSD\_PCIE3\_SEL\_L R1881 1K
- XDP\_SSD\_PCIE2\_SEL\_L R1882 1K
- XDP\_SSD\_PCIE1\_SEL\_L R1883 1K
- XDP\_SSD\_PCIE0\_SEL\_L R1884 1K
- XDP\_LPCPLUS\_GPIO MAKE\_BASE=TRUE
- XDP\_PCH\_GPIO17 TP1886
- XDP\_PCH\_GPIO76 TP1887
- XDP\_JTAG\_ISP\_TDI MAKE\_BASE=TRUE

Unused & MLB\_RAMCFGx GPIOs have TPs.

USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

SDCONN\_STATE\_CHANGE\_L is aliased, do not plug/unplug SD Cards during PCH debug.

JTAG\_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

NOTE: Should force PCH GPIO47 high to ensure TBT router powered to avoid leakage/clamping of signals.

SSD\_PCIEx\_SEL\_L straps are connected via 1K to common net.

LPCPLUS\_GPIO is aliased, do not attempt use during PCH debug.

### Merged (CPU/PCH) Micro2-XDP

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

CRITICAL XDP CONN J1800

DF40RC-60DP-0.4V

62 61

2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60

OBSFN\_A0 OBSFN\_A1 OBSFN\_A2 OBSFN\_A3 OBSFN\_B0 OBSFN\_B1 OBSFN\_B2 OBSFN\_B3

OBSDATA\_A0 OBSDATA\_A1 OBSDATA\_A2 OBSDATA\_A3 OBSDATA\_B0 OBSDATA\_B1 OBSDATA\_B2 OBSDATA\_B3

CPU\_CFG<0> CPU\_CFG<1> CPU\_CFG<2> CPU\_CFG<3> CPU\_CFG<4> CPU\_CFG<5> CPU\_CFG<6> CPU\_CFG<7>

XDP\_BPM\_L<0> XDP\_BPM\_L<1>

XDP\_CPU\_VCCST\_PWRGD XDP\_CPU\_PWRBTN\_L

CPU\_PWR\_DEBUG XDP\_SYS\_PWROK

SMBUS\_PCH\_DATA SMBUS\_PCH\_CLK XDP\_PCH\_TCK

SDA SCL TCK1 TCK0

ITPCLK/HOOK4 ITPCLK#/HOOK5

VCC\_OBS\_CD RESET#/HOOK6 DBR#/HOOK7

XDP\_CPU\_PRESENT\_L

518S0847

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60

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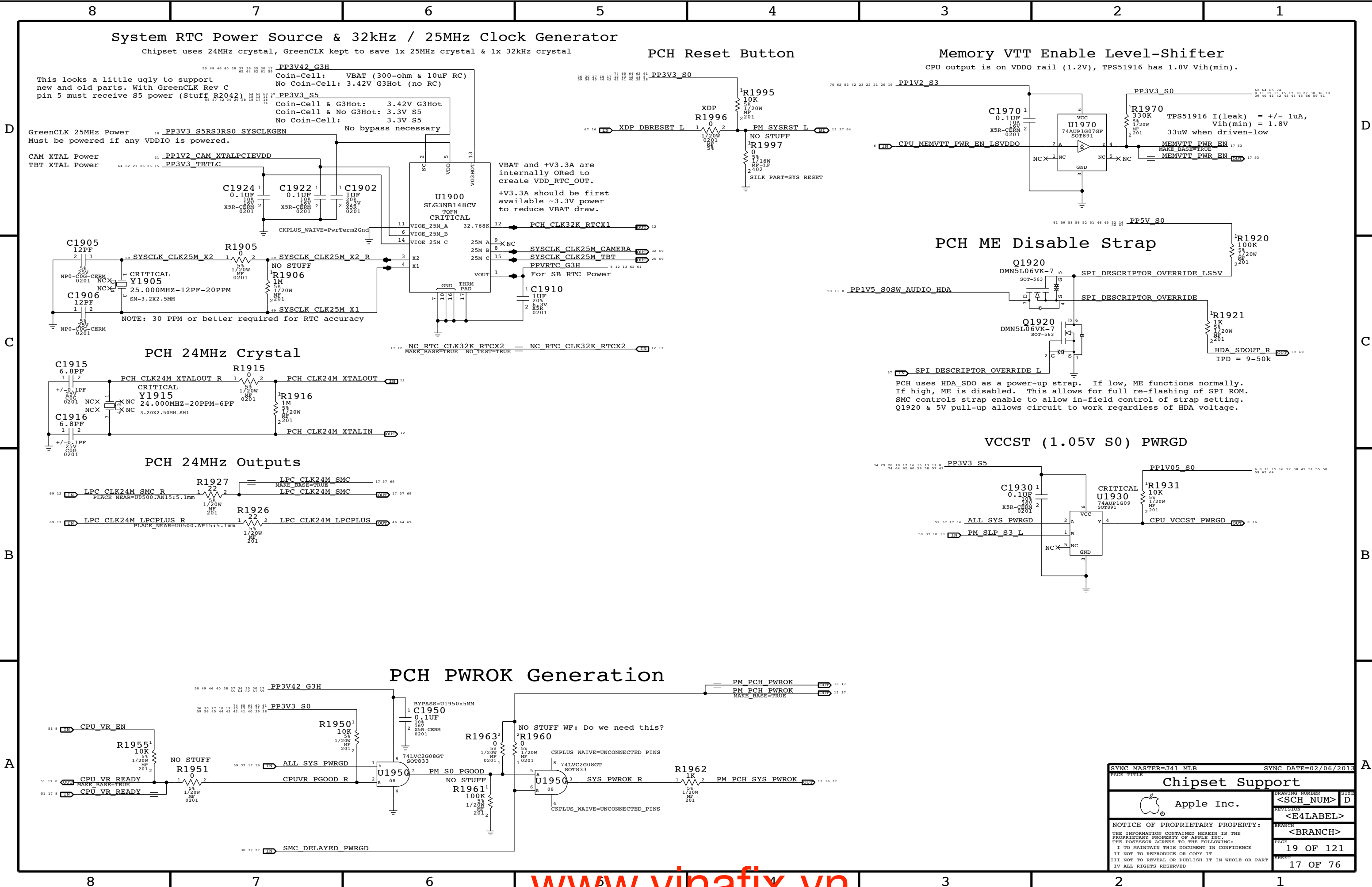
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```
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

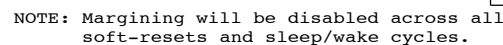
Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- DDRVREF_DAC - Stuffs DAC margining circuit.
```

## FETs for CPU isolation during DAC margining

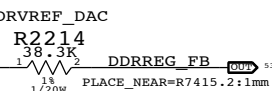
NOTE: CPU has single output for VREFOA. Split into two signals for independent DAC margining support. When DAC margining VREFOA ensure VREFMRGN\_CPU\_EN is low to remove short due to CPU.


DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.



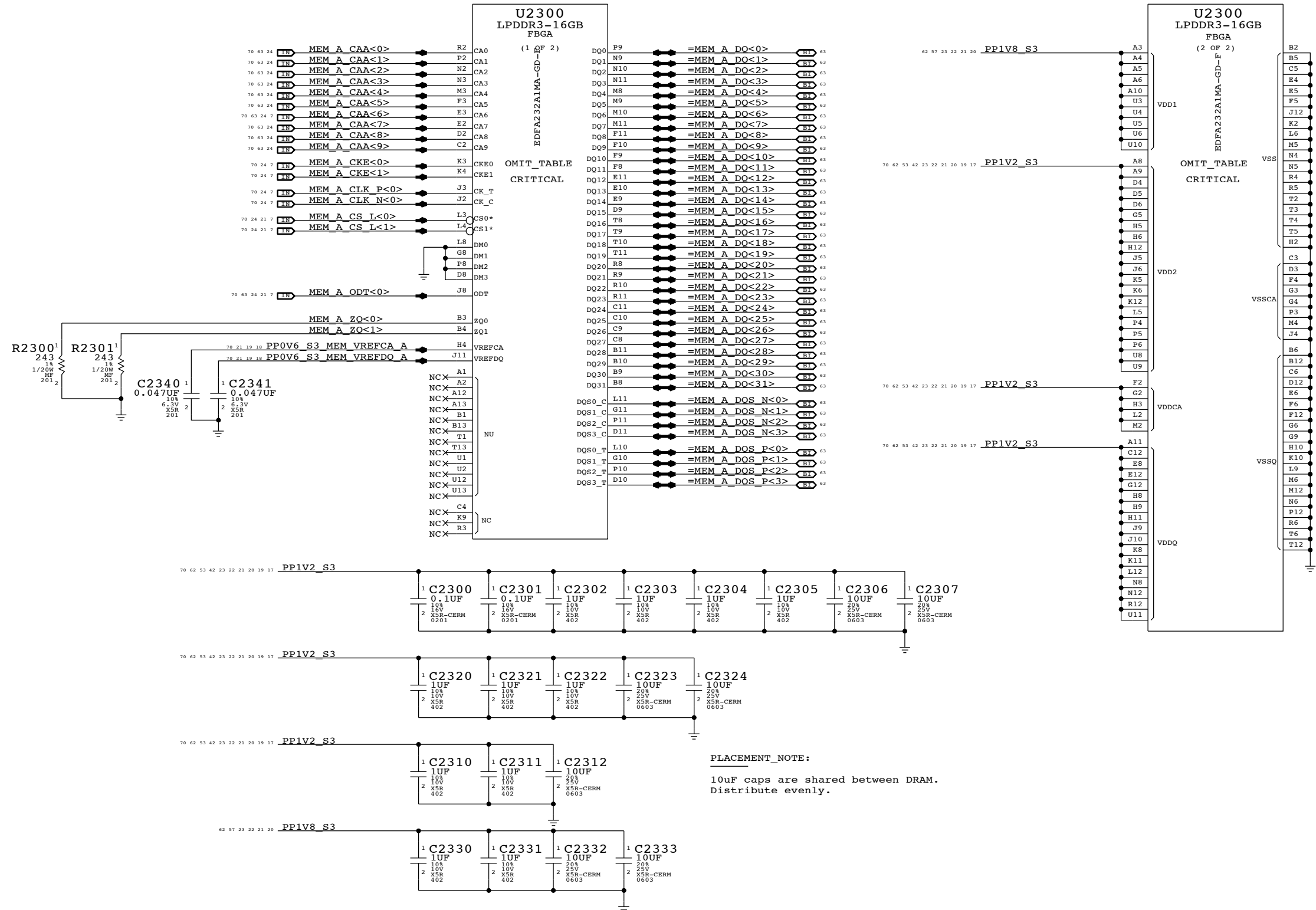
NOTE: LPDDR3 assumes TPS51916 supply with 28.7k/57.6k divider  
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider


Always used, regardless  
of margining option.



SYMC MASTER=J41 MLB		SYMC DATE=02/12/2013	
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 Apple Inc.		DRAWING NUMBER	
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LPDDR3 CHANNEL A (0-31)



SYNC MASTER=J41 MLB		SYNC DATE=02/06/2013	
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LPDDR3 DRAM Channel A		(0-31)	
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## D



B

A

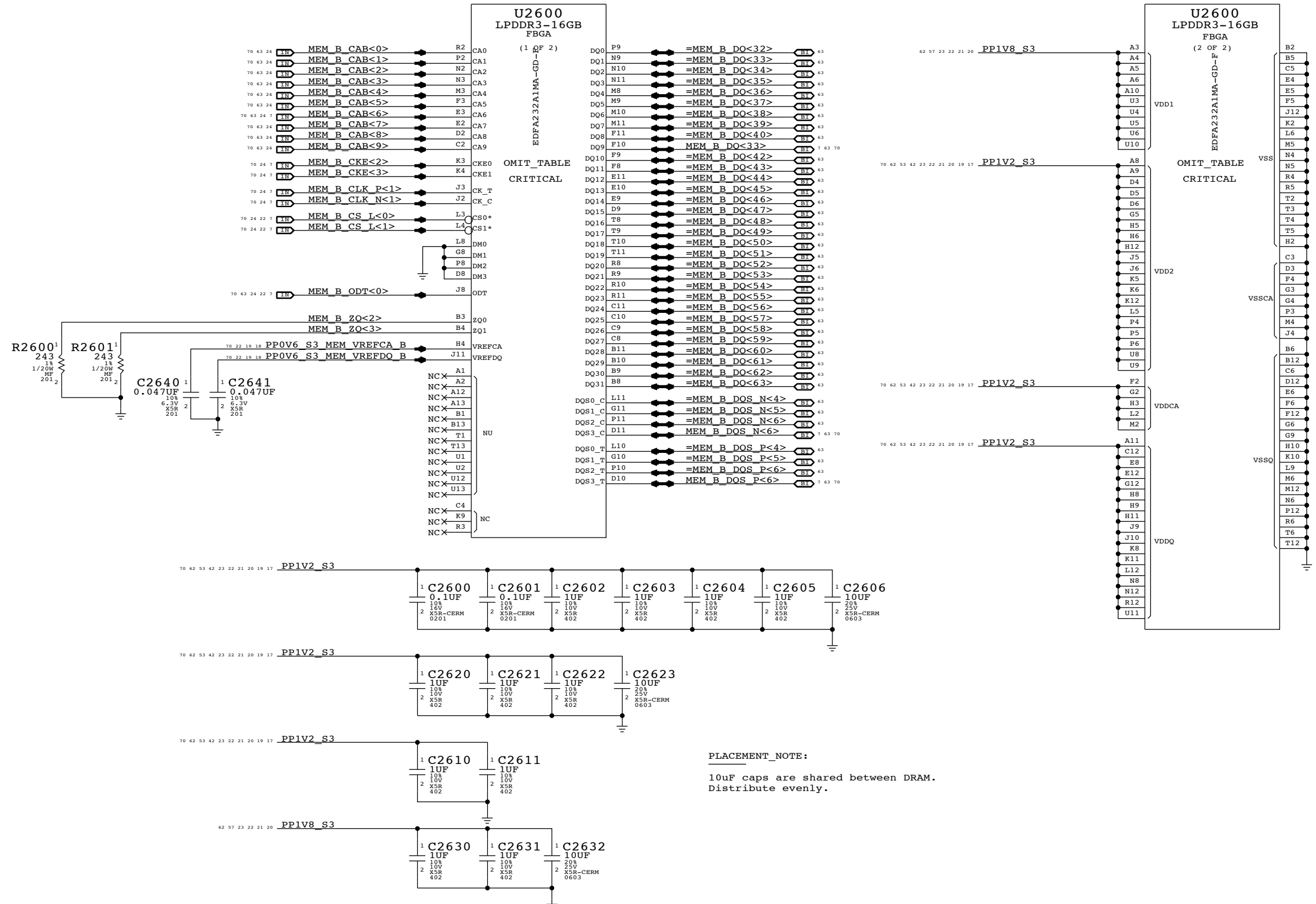
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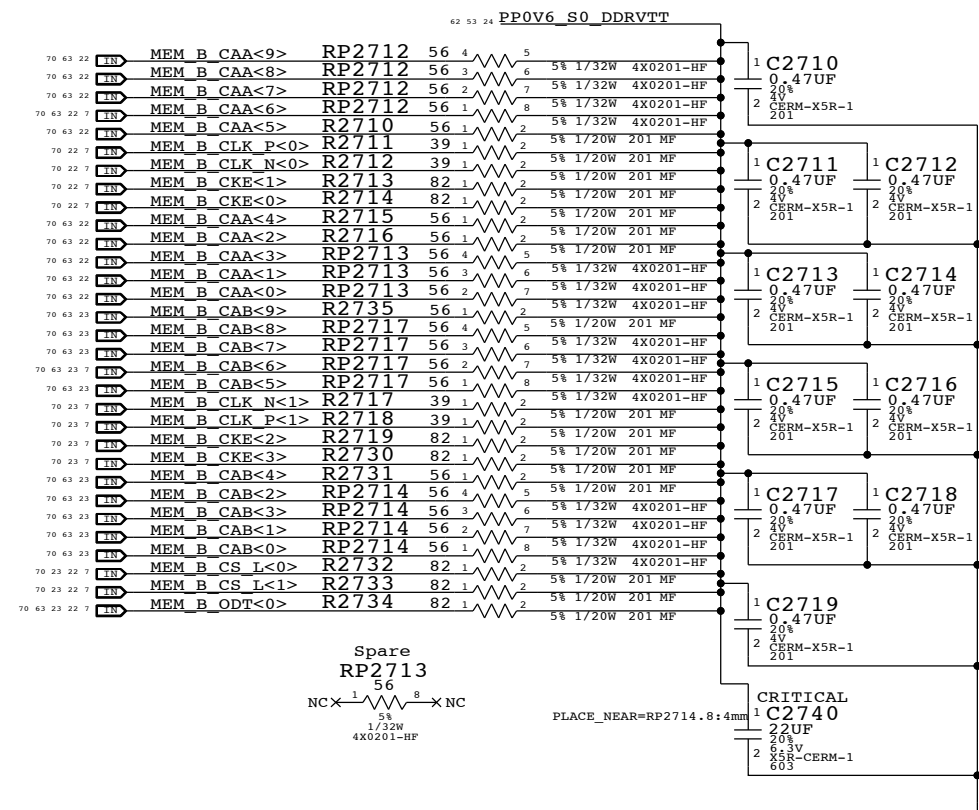
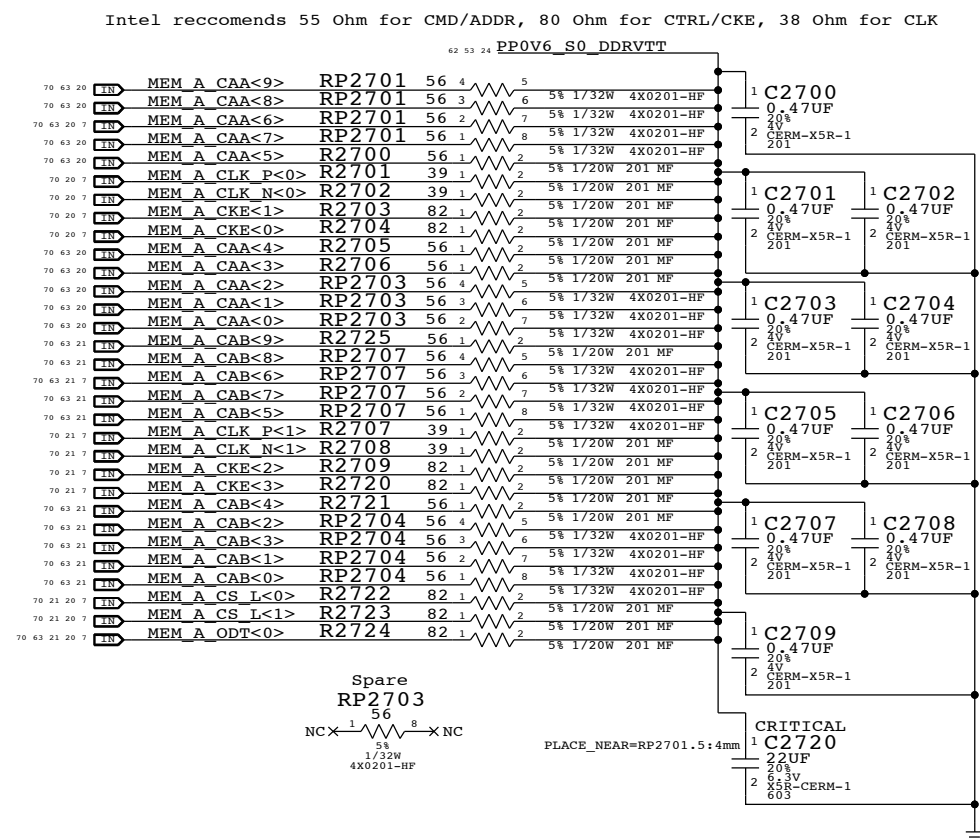
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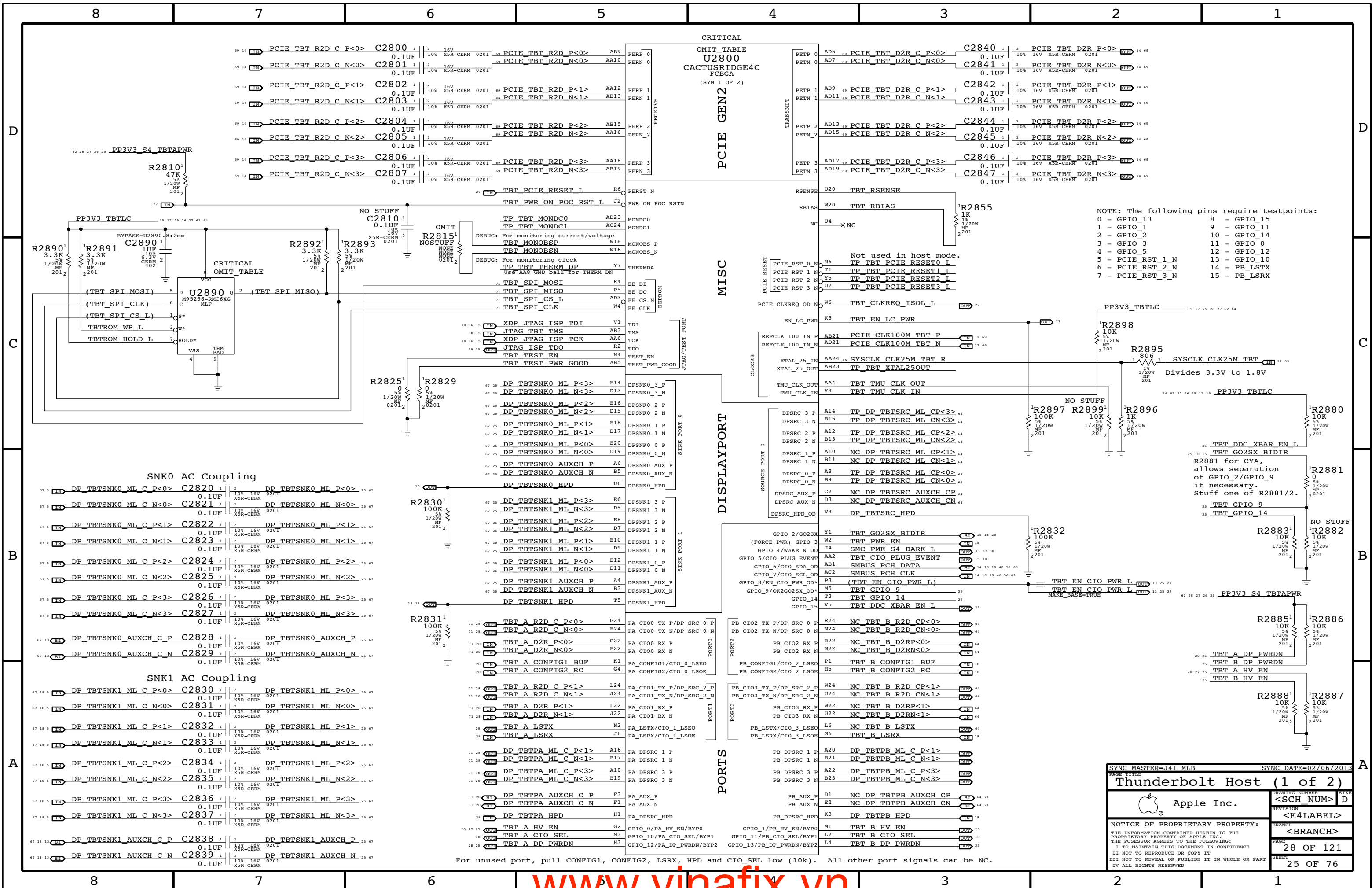
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LPDDR3 CHANNEL B (32-63)











## Page Notes

Power aliases required by this page:

- PPVIN\_SW\_TBTBST (8-13V Boost Input)
- PP15V\_TBT\_REG (15V Boost Output)
- PP3V3\_TBT\_P3V3TBTFTET (3.3V FET Input)
- PP3V3\_TBT\_FET (3.3V FET Output)
- PP3V3\_S0\_TBTTPWRCTL
- PP1V05\_TBT\_P1V05TBTFTET (1.05V FET Input)
- PP1V05\_TBT\_FET (1.05V FET Output)

Signal aliases required by this page:

- TBT\_CLKREQ\_L
- TBT\_RESET\_L

BOM options provided by this page:

(NONE)

## TBT 15V Boost Regulator

SI8409DB:  
Vds(max): -30V  
Vgs(max): +/-12V  
Vgs(th): -1.4V  
Rds(on): 46mOhm @ 4.5V Vgs  
Id(max): 3.7A @ 70C

CRITICAL  
Q3080  
SI8409DB

CRITICAL  
L3095  
6.8UH-4.0A

CRITICAL  
D3095  
POWERDI-123

PP15V\_TBT  
Vout = 15.1V  
Max Current = 1.0A  
Freq = 300KHz

## Supervisor & CLKREQ# Isolation

## TBT "POC" Power-up Reset

## 3.3V TBT "LC" Switch

U3010  
TPS22924  
CSP  
Max Current = 2A (85C)

Part	TPS22924C
Type	Load Switch
R(on)	18.5 mOhm Typ 25.8 mOhm Max

## 1.05V TBT "LC" Switch

U3015  
TPS22920  
CSP  
Max Current = 4A (85C)

Part	TPS22920
Type	Load Switch
R(on)	6.1 mOhm Typ 10.4 mOhm Max

## 1.05V TBT "CIO" Switch

U3020  
TPS22920  
CSP  
Max Current = 4A (85C)

Part	TPS22920
Type	Load Switch
R(on)	6.1 mOhm Typ 10.4 mOhm Max

SYNC MASTER=J41 MLB	SYNC DATE=02/06/2013
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TBT Power Support	
Apple Inc.	DRAWING NUMBER <SCH_NUM>
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	PAGE 30 OF 121
	SHEET 27 OF 76




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D



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

B

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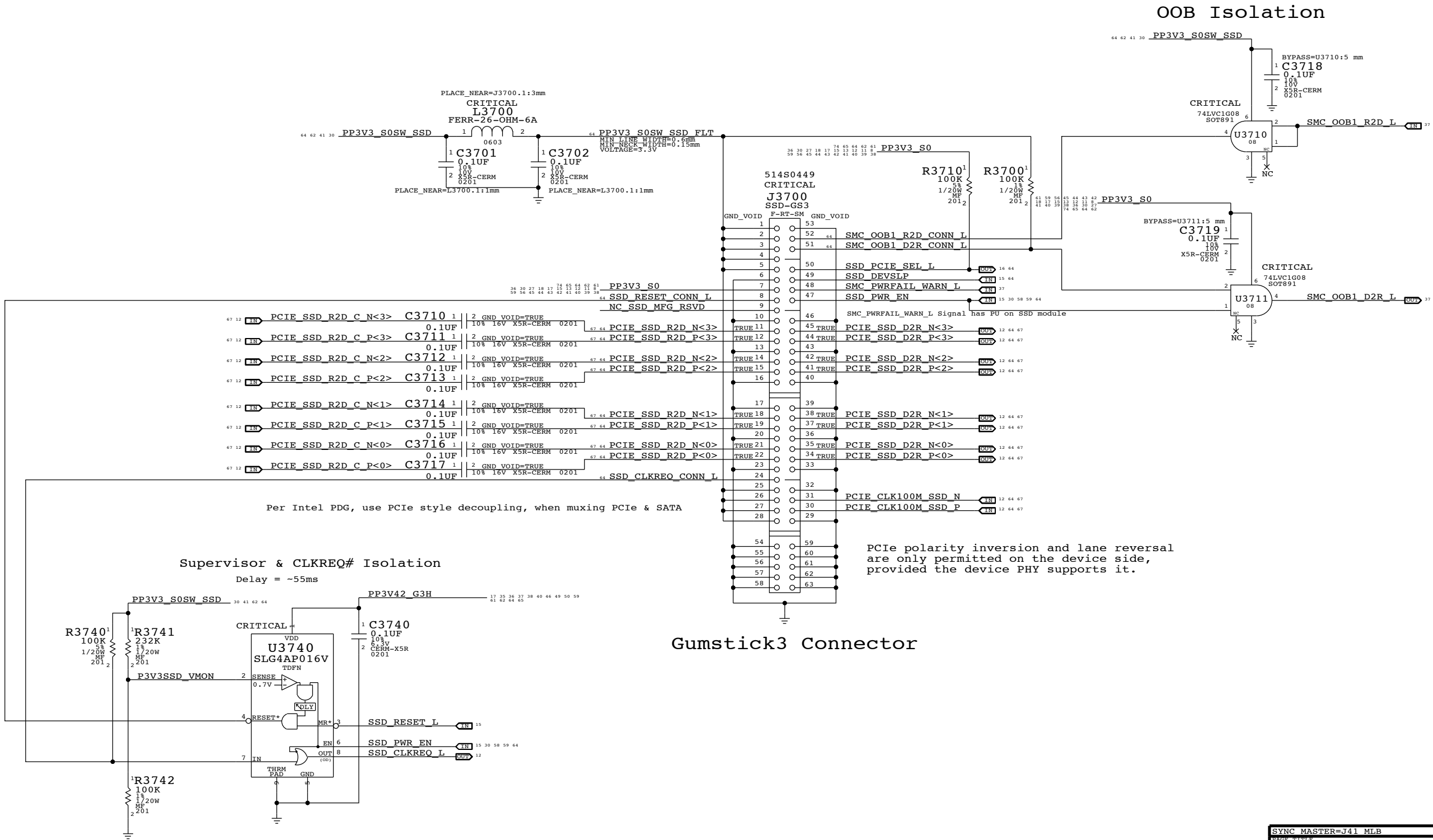
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
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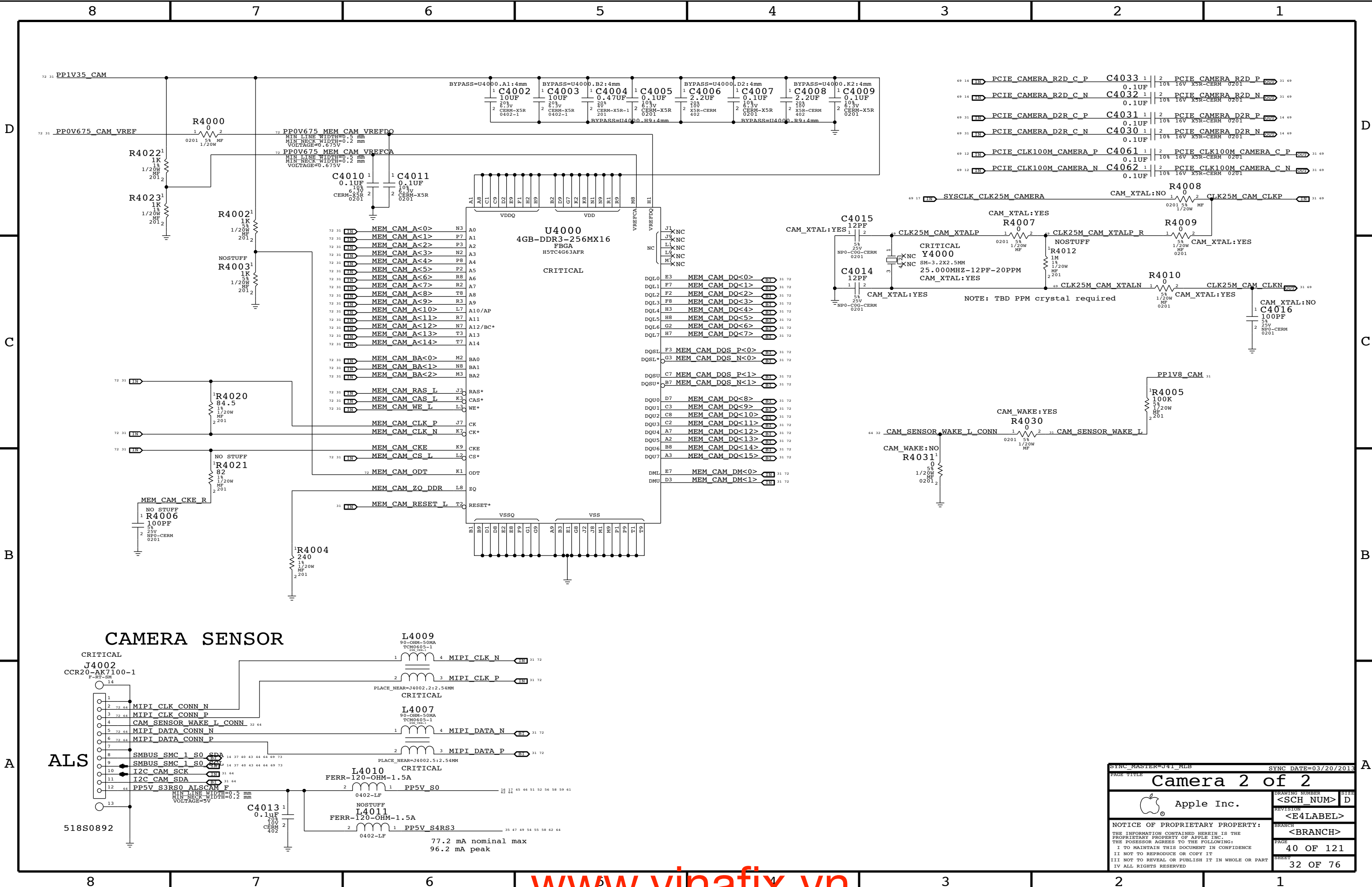
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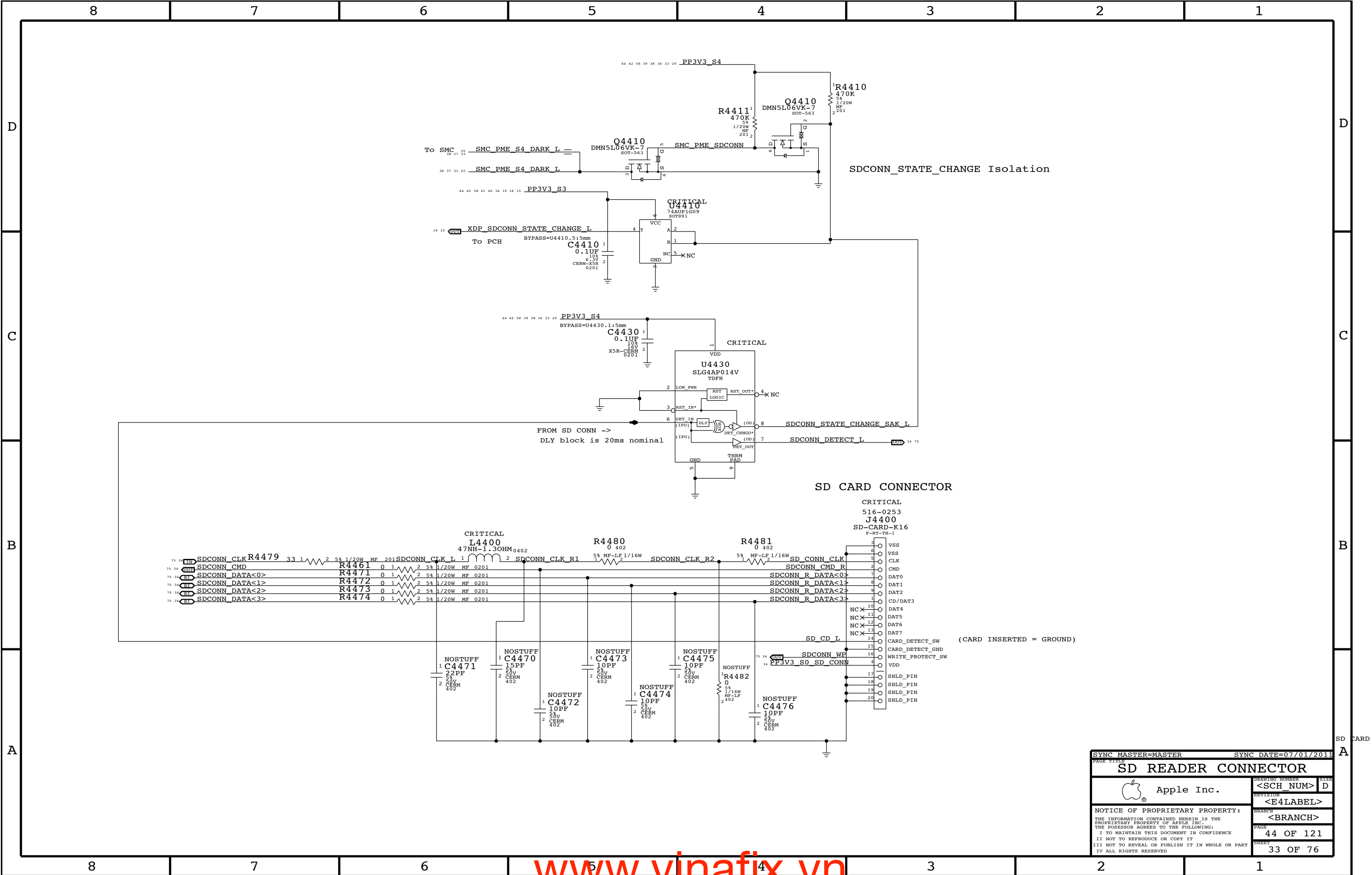



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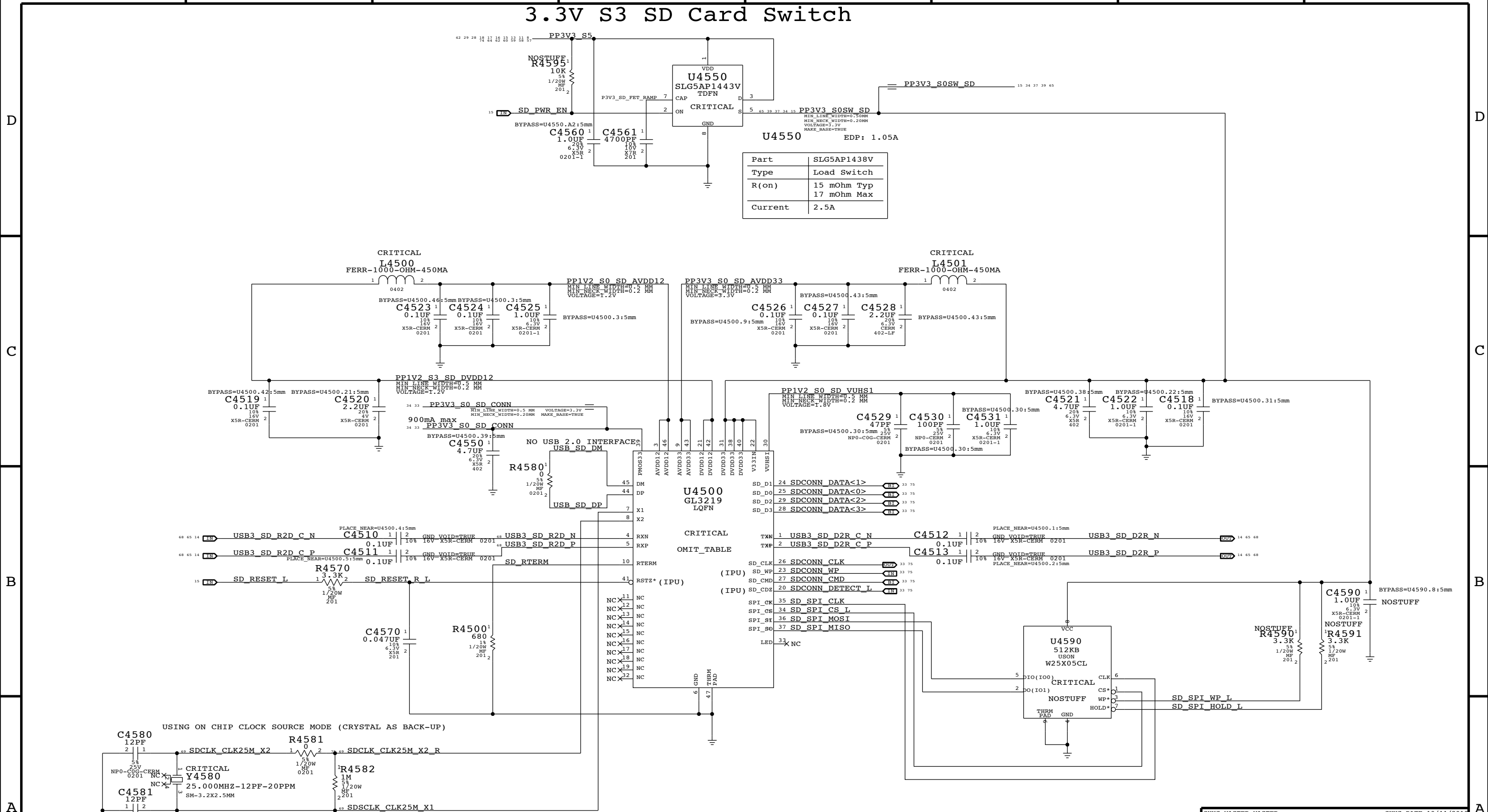
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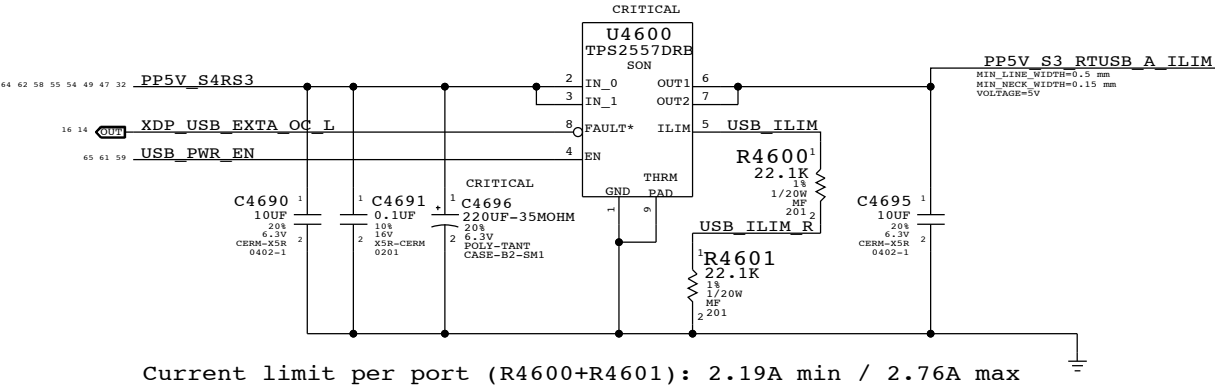
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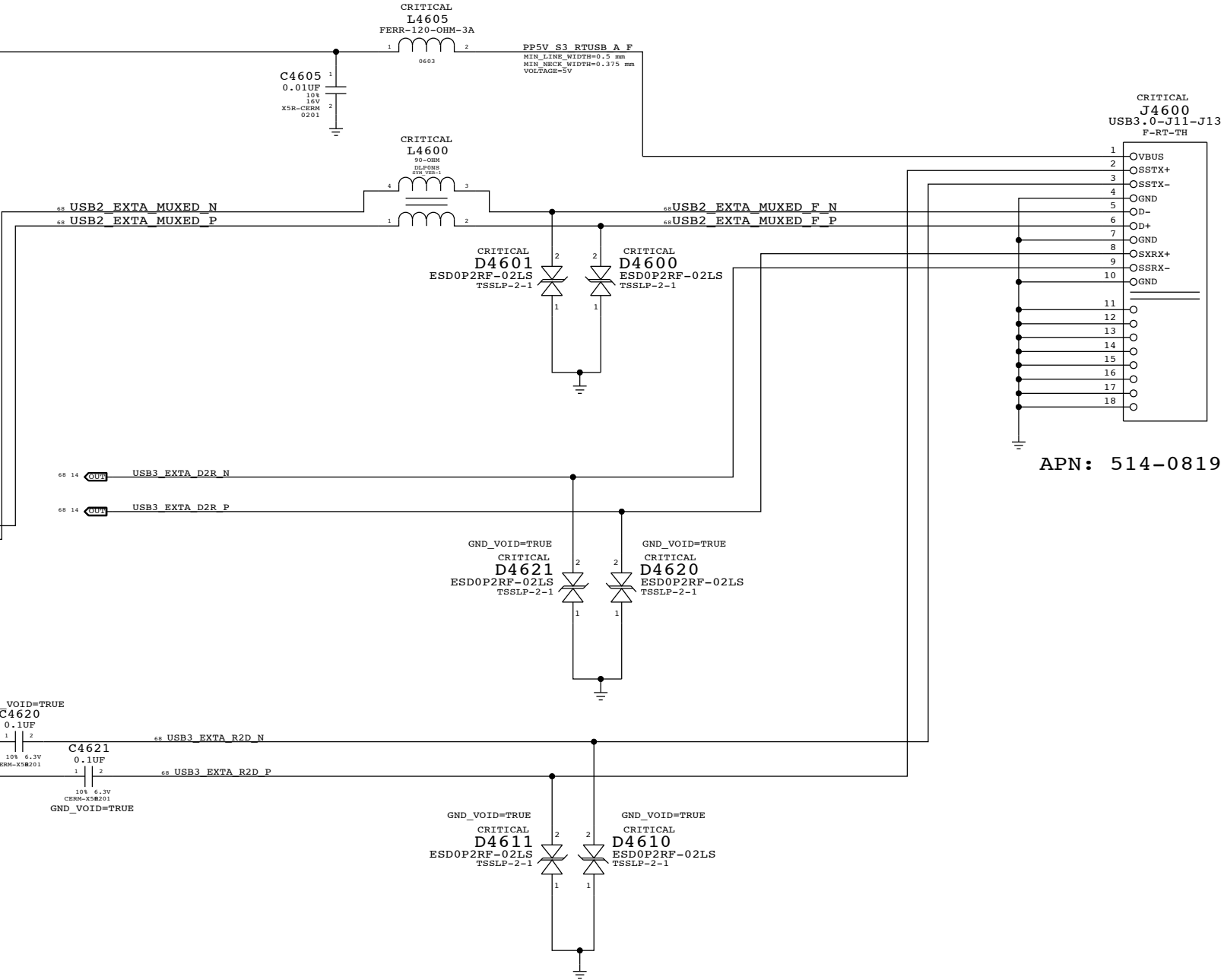
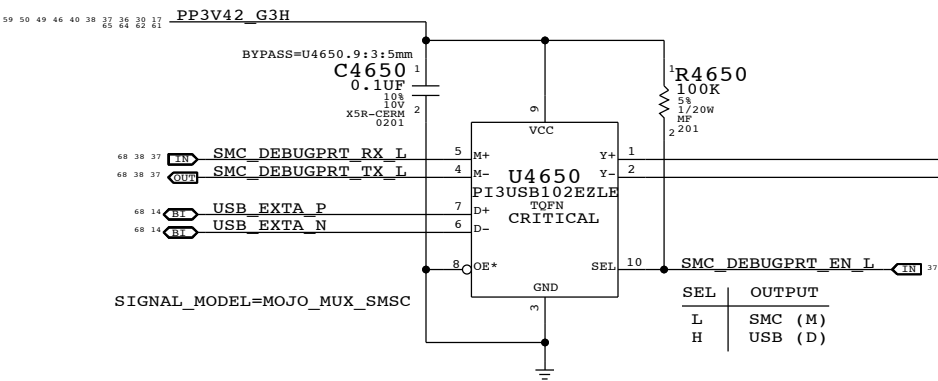
The diagram shows a power supply circuit. A 5V voltage source is connected to two pins of a component. Pin 1 is labeled SDSCLK and pin 2 is labeled CLK25M\_X1. The ground connection is labeled NP0-00G-CERM 0201.

Right USB Port A


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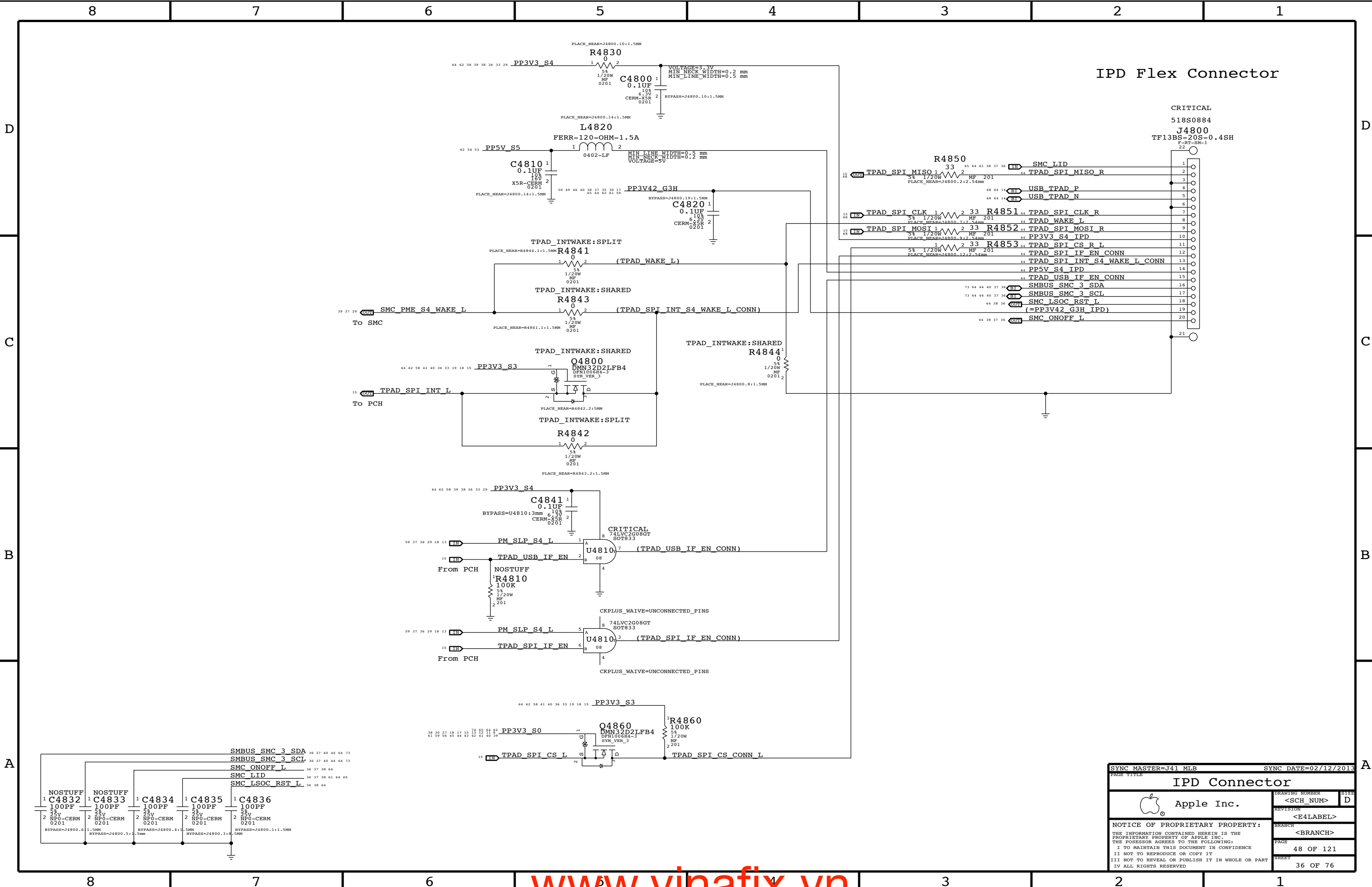


Mojo SMC Debug Mux




APN: 514-0819

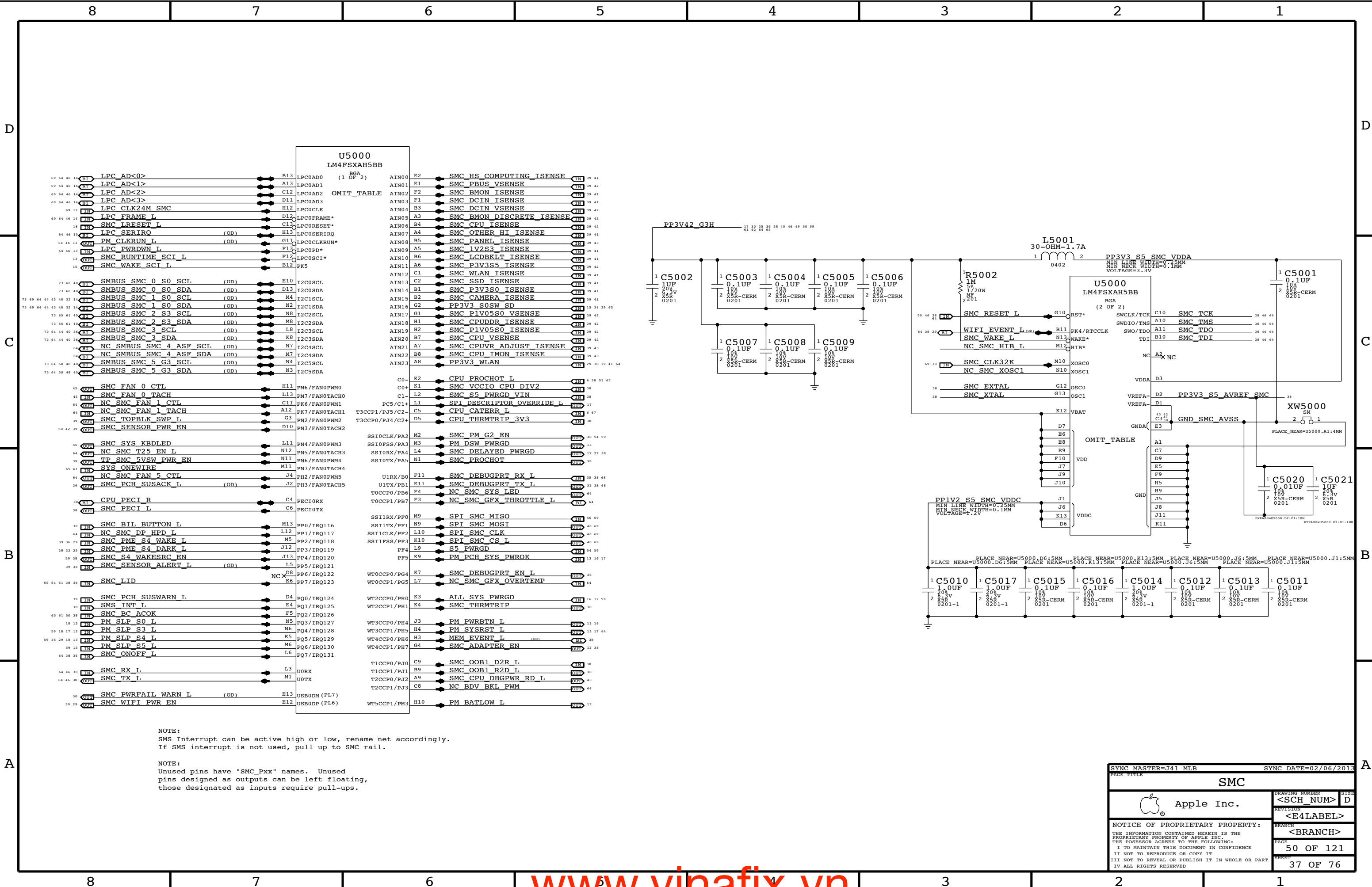
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IPD Flex Connector

CRITICAL	
518S0884	
J4800	
TF13BS-20S-0.4SH	
F-RT-SM-1	
22	
1	
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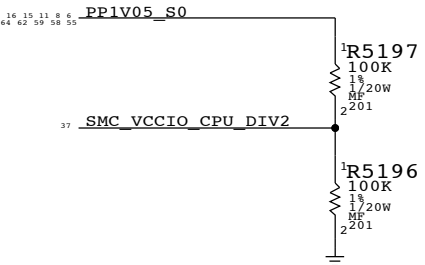
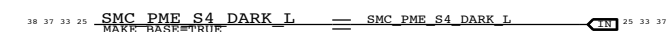
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## A

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## D

A

D

C

B

A

D

C

B

A

41 39 37

SMC\_HS\_COMPUTING\_ISENSE

SMC\_HS\_COMPUTING\_ISENSE

37 39 41

42 39 37

SMC\_PBUS\_VSENSE

SMC\_PBUS\_VSENSE

37 39 42

41 39 37

SMC\_BMON\_ISENSE

SMC\_BMON\_ISENSE

37 39 41

41 39 37

SMC\_DCIN\_ISENSE

SMC\_DCIN\_ISENSE

37 39 41

42 39 37

SMC\_DCIN\_VSENSE

SMC\_DCIN\_VSENSE

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43 39 37

SMC\_BMON\_DISCRETE\_ISENSE

SMC\_BMON\_DISCRETE\_ISENSE

37 39 43

42 39 37

SMC\_CPU\_ISENSE

SMC\_CPU\_ISENSE

37 39 42

41 39 37

SMC\_OTHER\_HI\_ISENSE

SMC\_OTHER\_HI\_ISENSE

37 39 41

43 39 37

SMC\_PANEL\_ISENSE

SMC\_PANEL\_ISENSE

37 39 43

41 39 37

SMC\_IV2S3\_ISENSE

SMC\_IV2S3\_ISENSE

37 39 41

41 39 37

SMC\_LCDBKLT\_ISENSE

SMC\_LCDBKLT\_ISENSE

37 39 41

42 39 37

SMC\_P3V3S5\_ISENSE

SMC\_P3V3S5\_ISENSE

37 39 42

41 39 37

SMC\_WLAN\_ISENSE

SMC\_WLAN\_ISENSE

37 39 41

41 39 37

SMC\_SSD\_ISENSE

SMC\_SSD\_ISENSE

37 39 41

41 39 37

SMC\_P3V3S0\_ISENSE

SMC\_P3V3S0\_ISENSE

37 39 41

41 39 37

SMC\_CAMERA\_ISENSE

SMC\_CAMERA\_ISENSE

37 39 41

PP3V3\_S0SW\_SD

SD alias on page 103

42 39 37

SMC\_P1V05S0\_VSENSE

SMC\_P1V05S0\_VSENSE

37 39 42

42 39 37

SMC\_CPUDDR\_ISENSE

SMC\_CPUDDR\_ISENSE

37 39 42

42 39 37

SMC\_P1V05S0\_ISENSE

SMC\_P1V05S0\_ISENSE

37 39 42

42 39 37

SMC\_CPU\_VSENSE

SMC\_CPU\_VSENSE

37 39 42

43 39 37

SMC\_CPUVR\_ADJUST\_ISENSE

SMC\_CPUVR\_ADJUST\_ISENSE

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SMC\_CPU\_IMON\_ISENSE

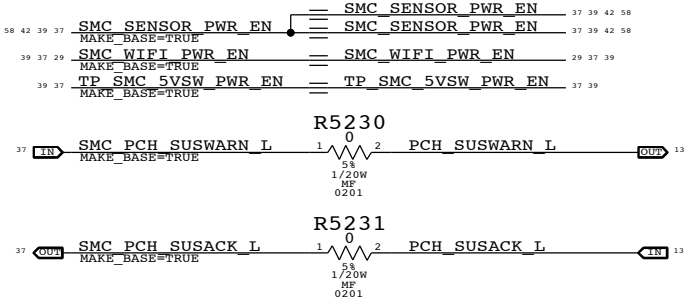
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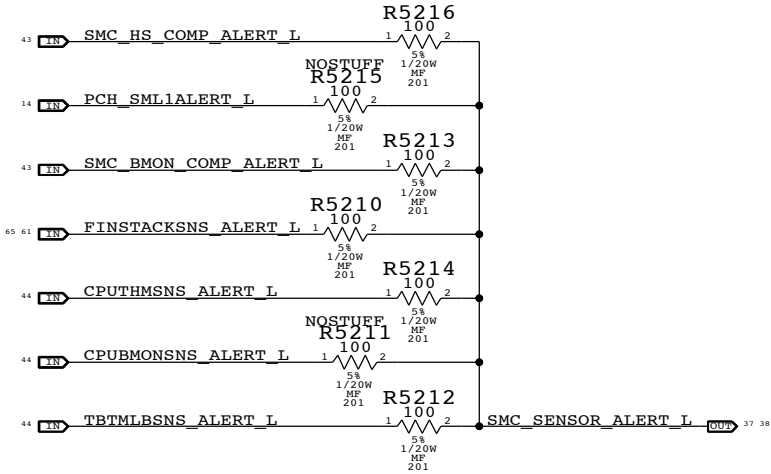
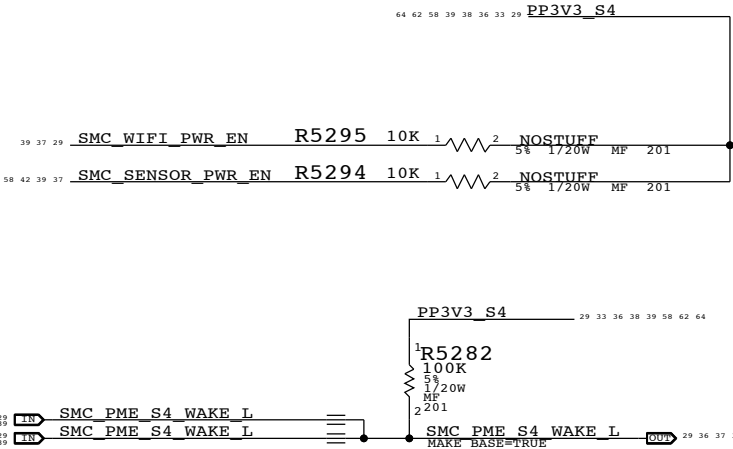
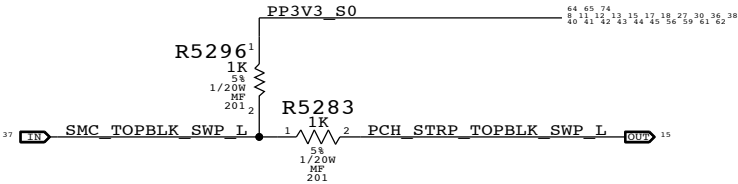
PP3V3\_WLAN

PP3V3\_WLAN

29 37 38 39 41 64



Top-Block Swap



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SYNC DATE=02/06/2013

SMC Project Support

Apple Inc.

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6

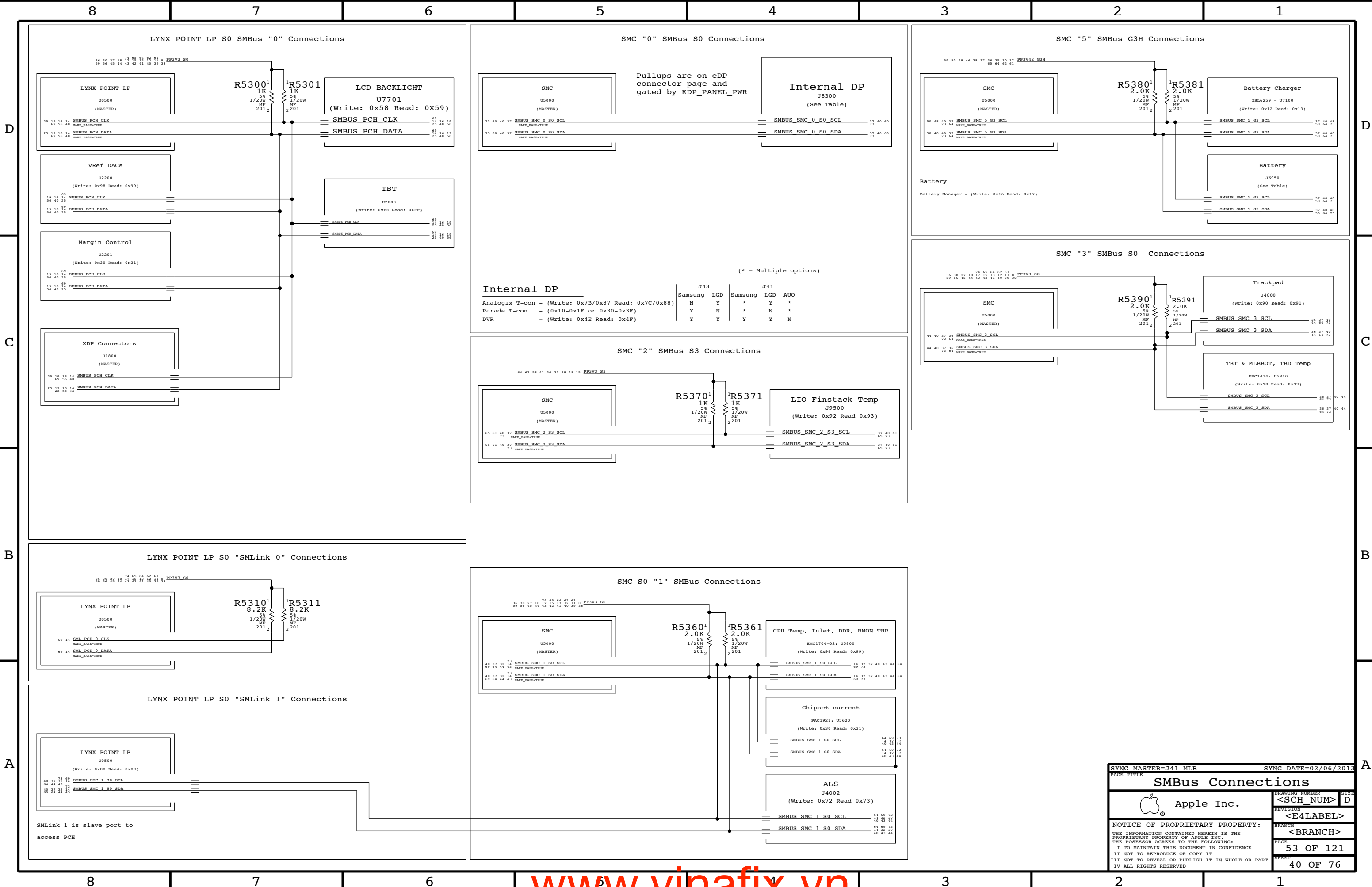
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SYNC DATE=02/06/2013

SMBus Connections

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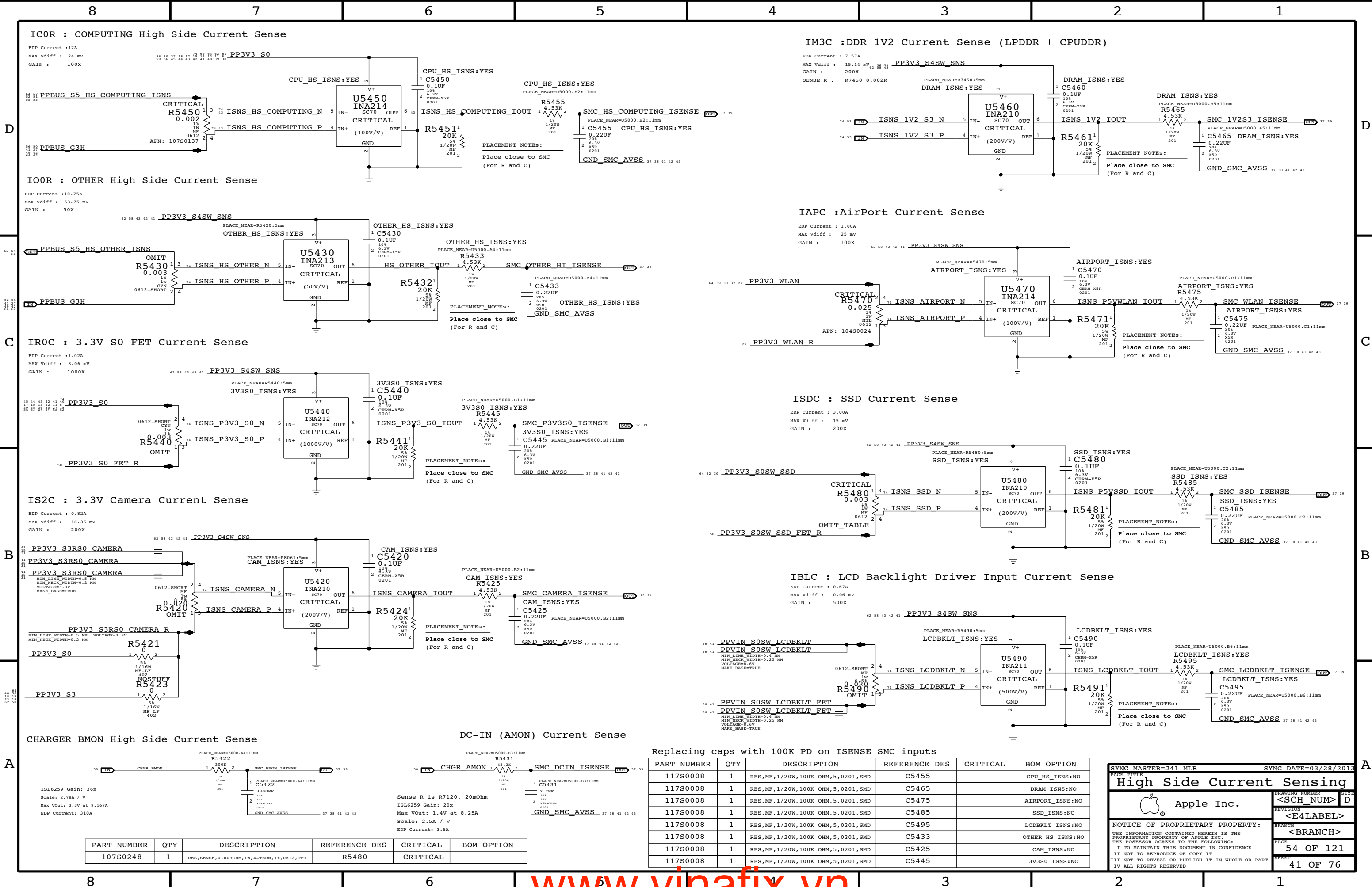
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
107S0248	1	RES,SENSE,0.0030HM,1W,4-TERM,1%,0612,TFT	R5480	CRITICAL	

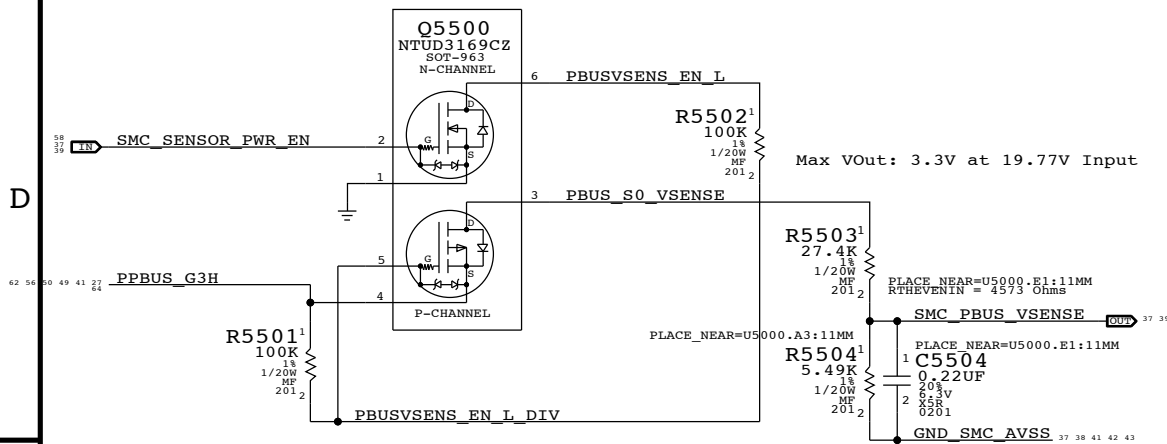
Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5455		CPU_HS_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5465		DRAM_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5475		AIRPORT_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5495		SSD_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5433		LCDBKLT_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5425		OTHER_HS_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5445		CAM_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5445		3V3S0_ISNS:NO

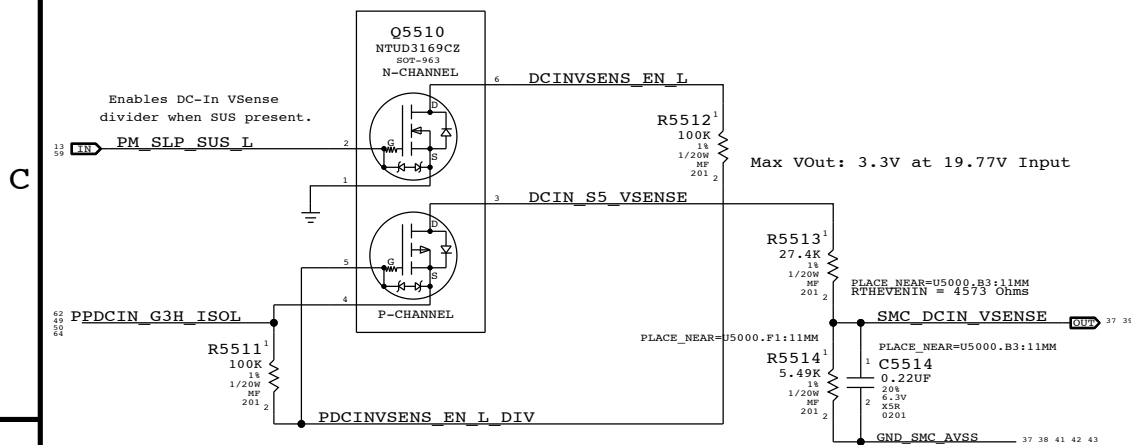
PAGE TITLE		PAGE NUMBER	
High Side Current Sensing		54 OF 121	
Apple Inc.		41 OF 76	
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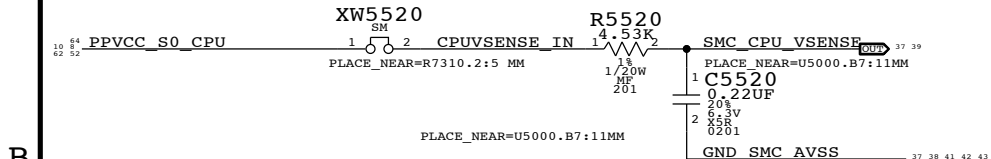
## VP0R: PBUS Voltage Sense Enable & Filter



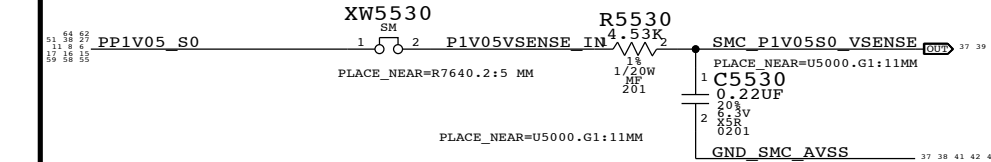
## VD0R: DC-In Voltage Sense Enable & Filter



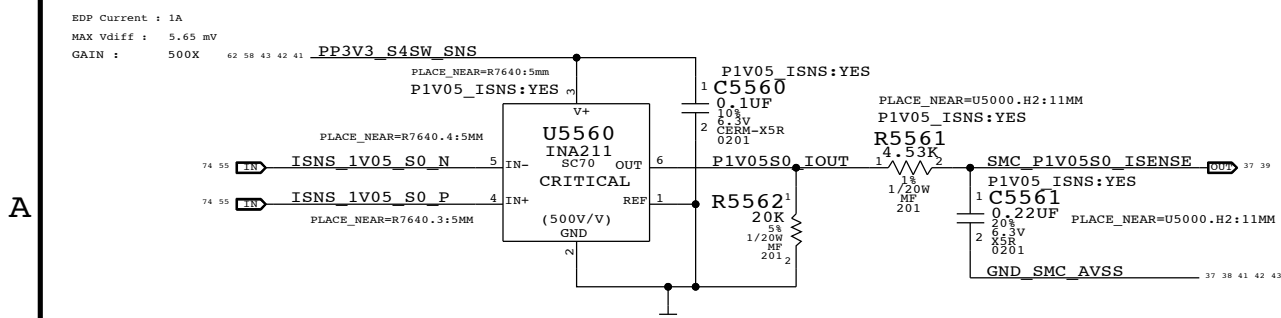
## CPU Vcore Voltage Sense / Filter



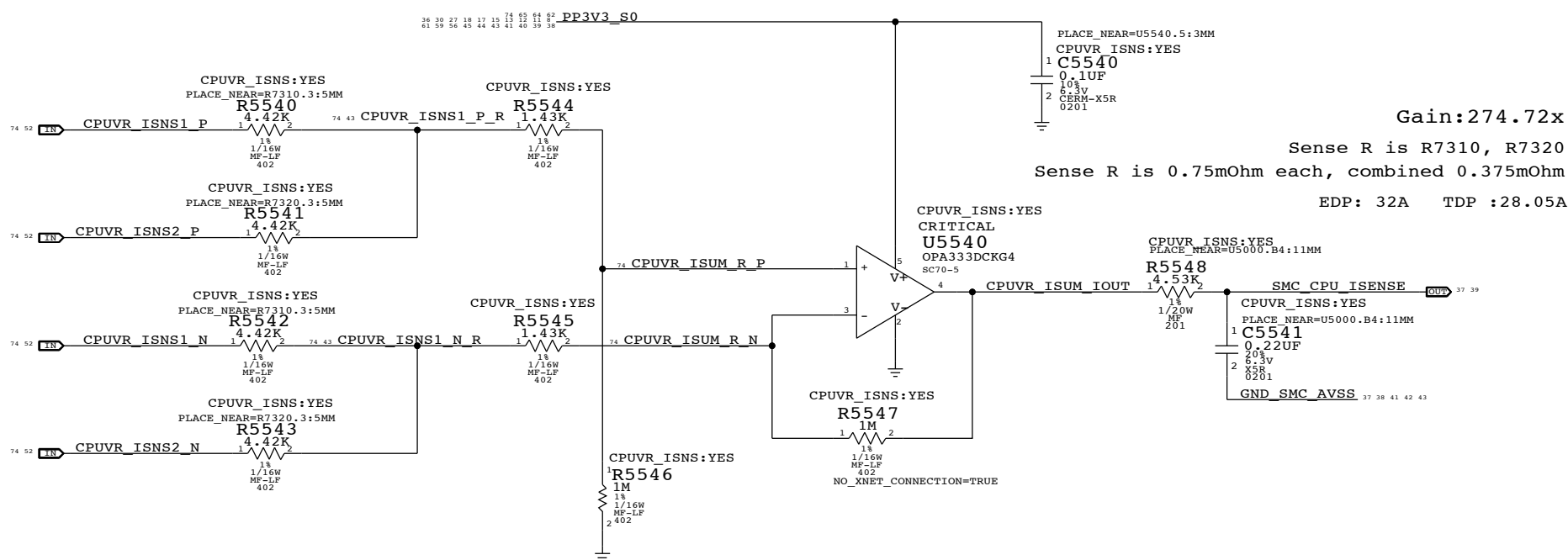
## 1.05V Voltage Sense / Filter



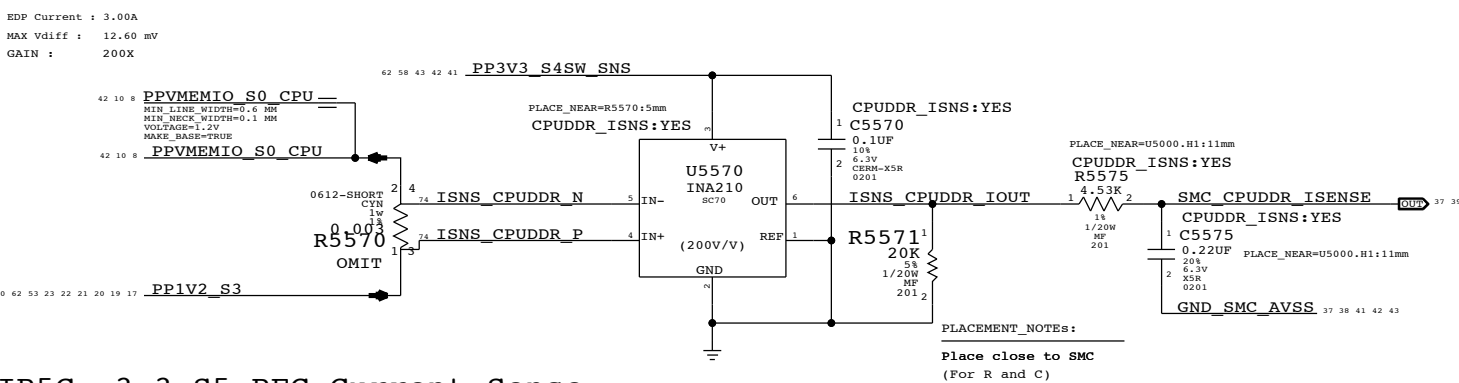
## IC1C: 1.05V S0 CURRENT SENSE / FILTER



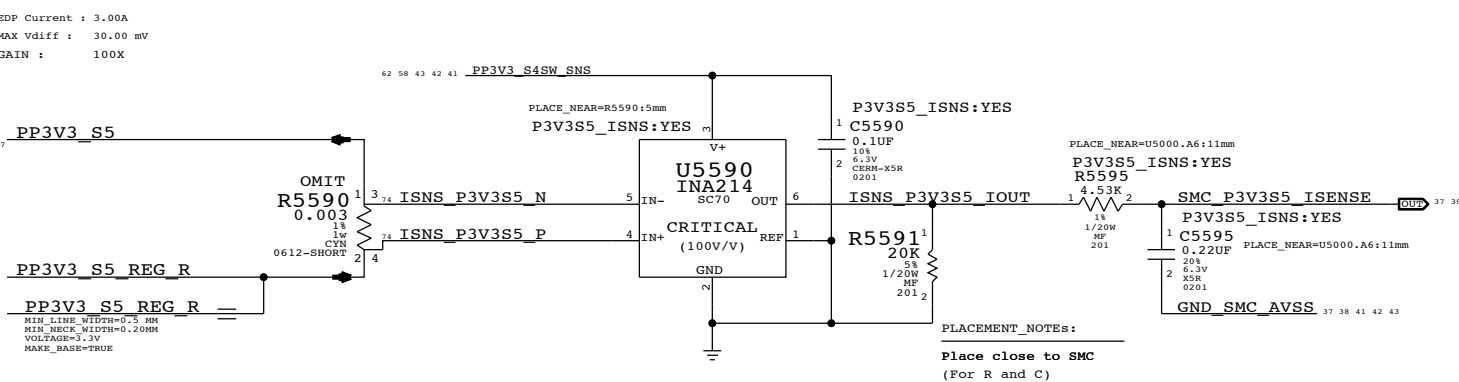
## ICS0 : CPU VCore Load Side Current Sense



## IM0C : CPU DDR Current Sense



## IR5C :3.3 S5 REG Current Sense



Replacing caps with 100K PD on ISENSE SMC inputs

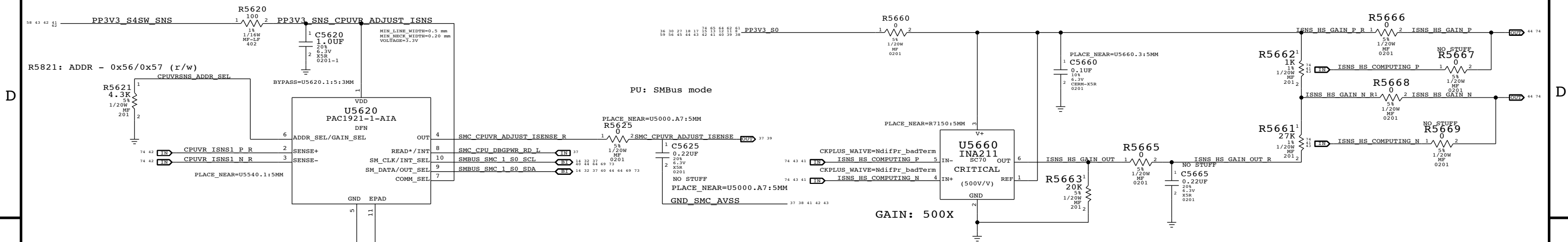
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5541		CPUVR_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5561		P1V05_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5595		P3V3S5_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5575		CPUDDR_ISNS:NO

Voltage & Load Side Current Sensing

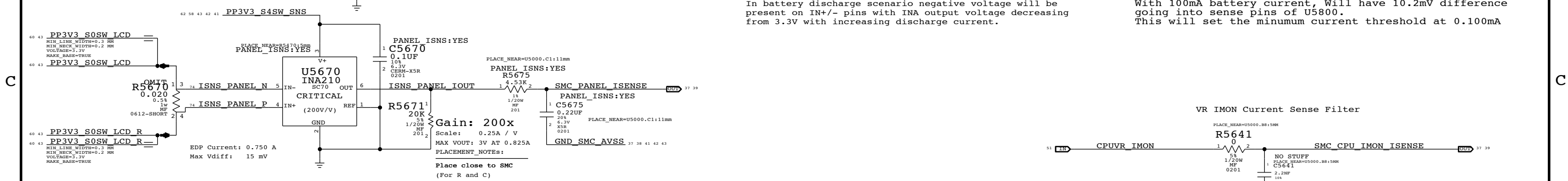
SYNC MASTER=J41 MLB	SYNC DATE=03/28/2013
Apple Inc.	<SCH_NUM> D
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	<BRANCH>
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ICS3 : Adjustable Gain CPU VR Current

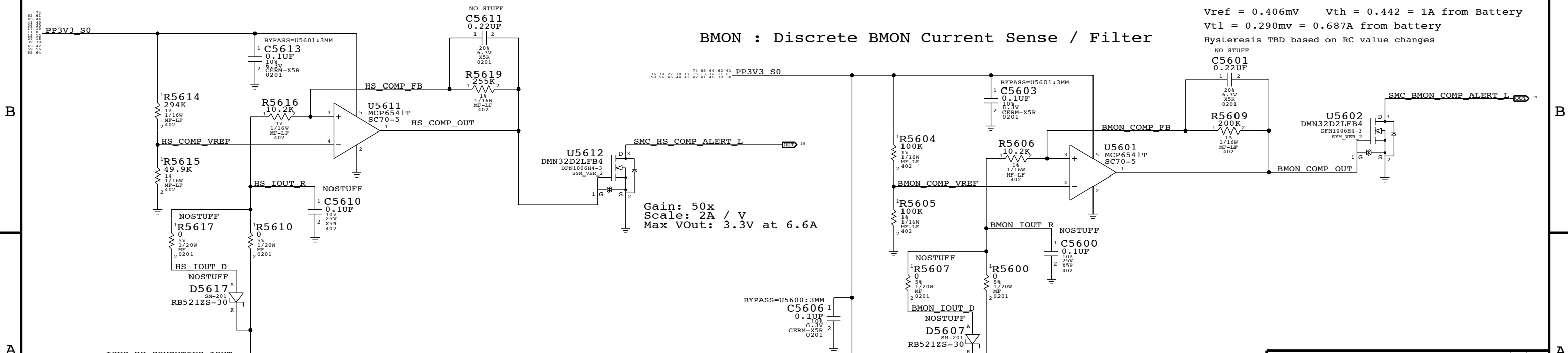
Sense Pins gain stage for U5800 (EMC1704)



ILDC :LCD Panel Current Sense / Filter



Discrete High side Current threshold

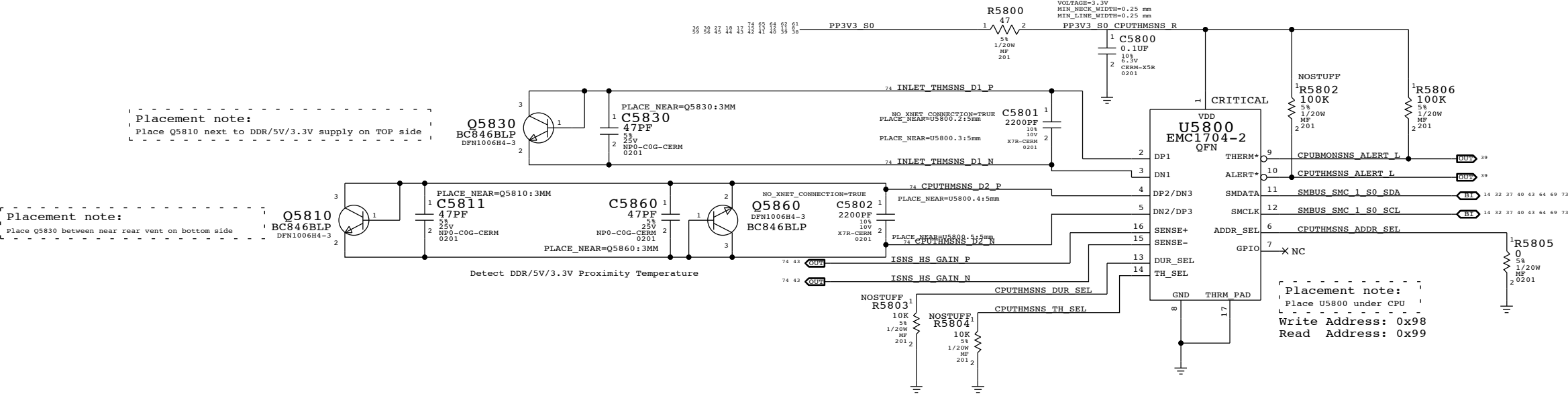


Replacing caps with 100K PD on ISENSE SMC inputs

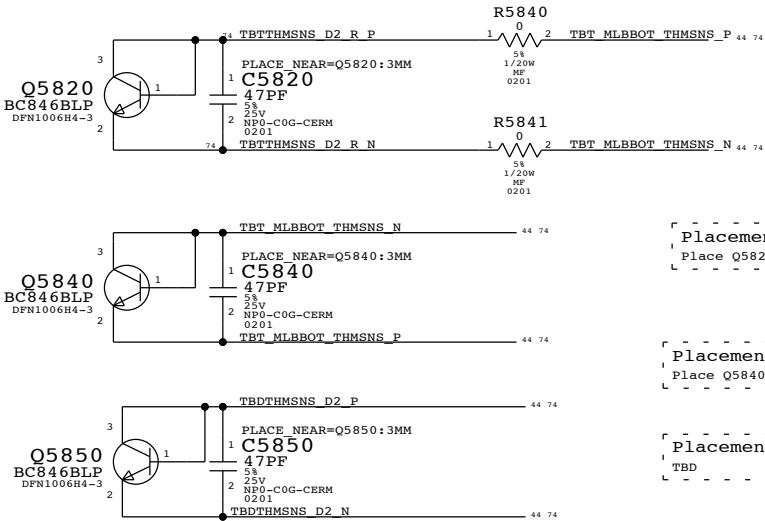
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,SMD	C5675		PANEL_ISNS:NO

SYNC MASTER=J41 MLB		SYNC DATE=03/28/2013	
PAGE TITLE		Debug Sensors 1	
Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
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		<BRANCH>	
		PAGE	56 OF 121
		SHEET	43 OF 76
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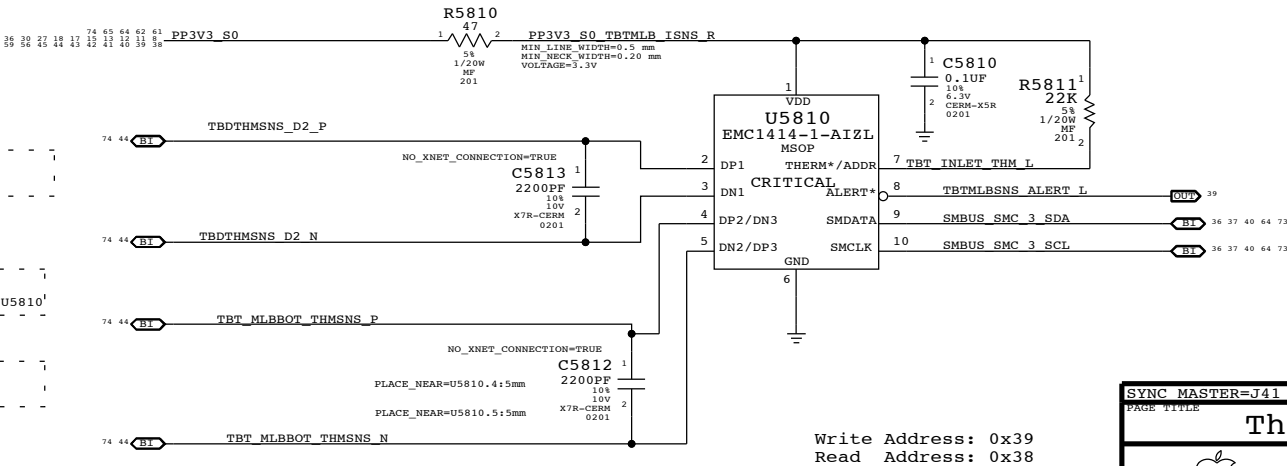
CPU Proximity, Inlet ,DDR and BMON THR Sensor




TBT,MLB Bottom Proximity Sensors



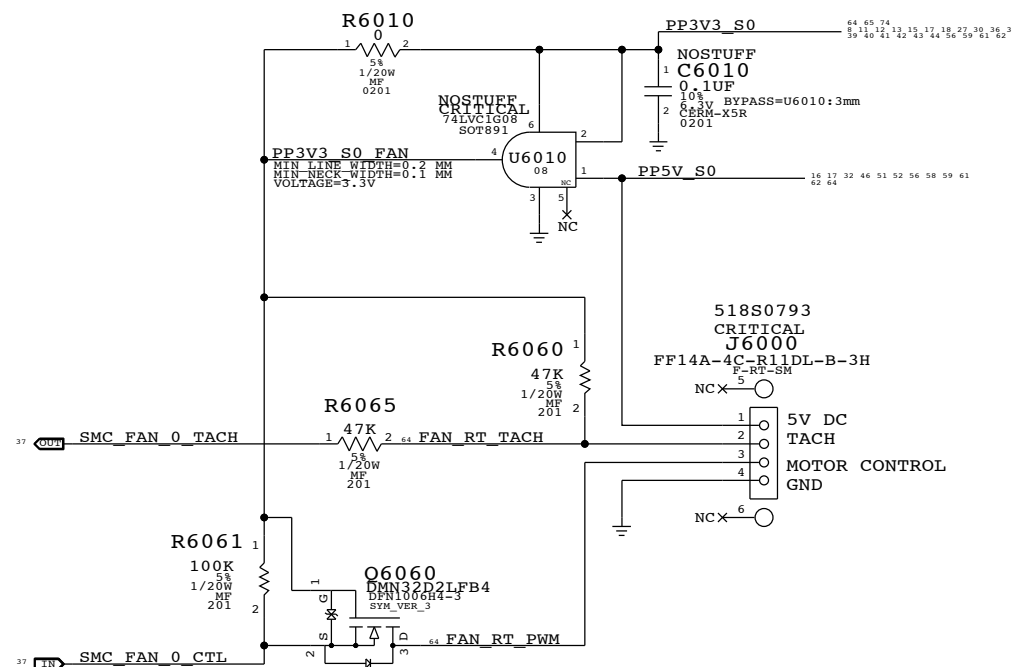
TBT, MLBBOT and TBD Temp Sensor



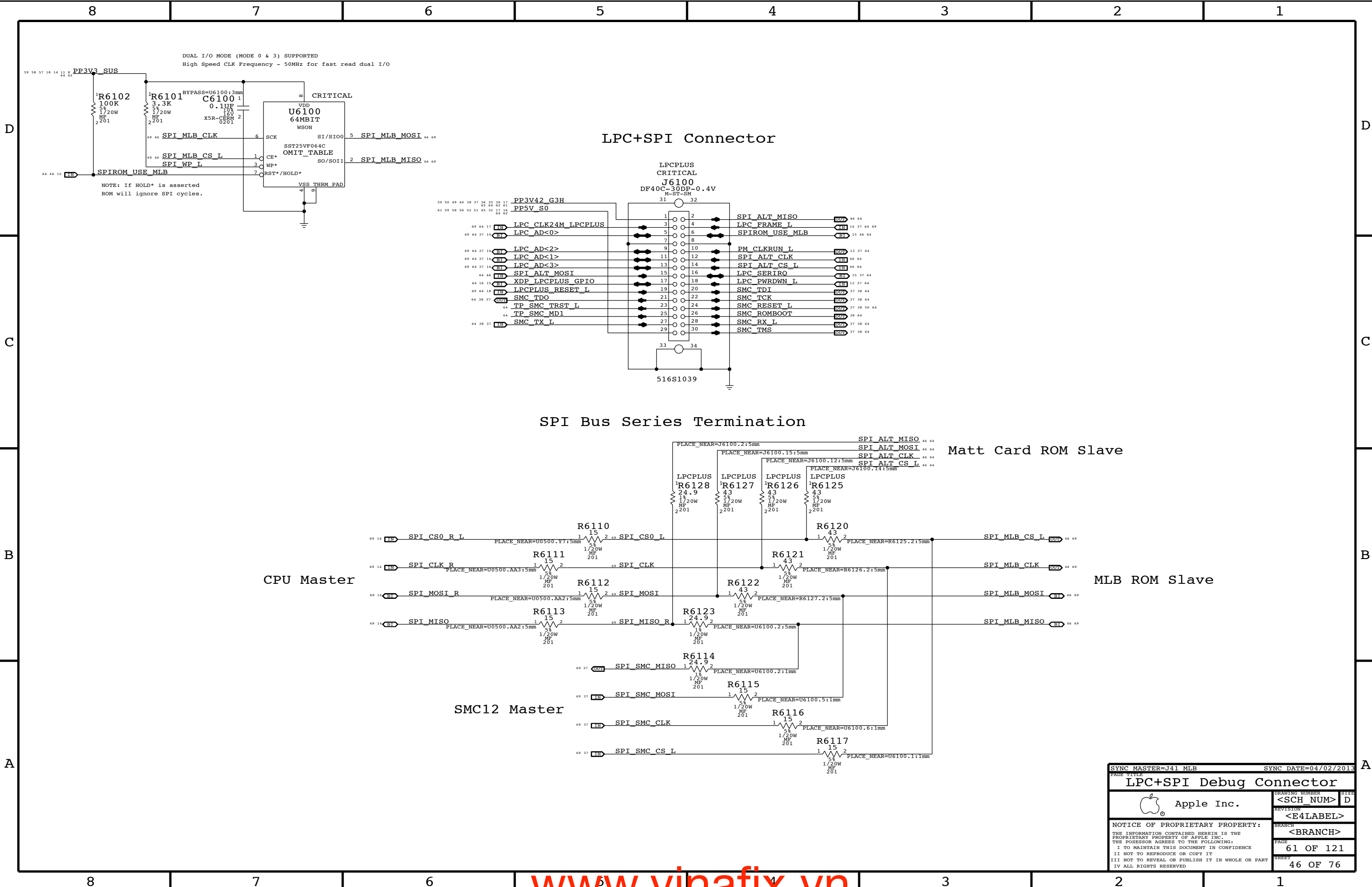
TBT MLBBOT THMSNS\_P  
TBT MLBBOT THMSNS\_P  
TBT MLBBOT THMSNS\_P  
TBT MLBBOT THMSNS\_N  
TBT MLBBOT THMSNS\_N  
TBT MLBBOT THMSNS\_N


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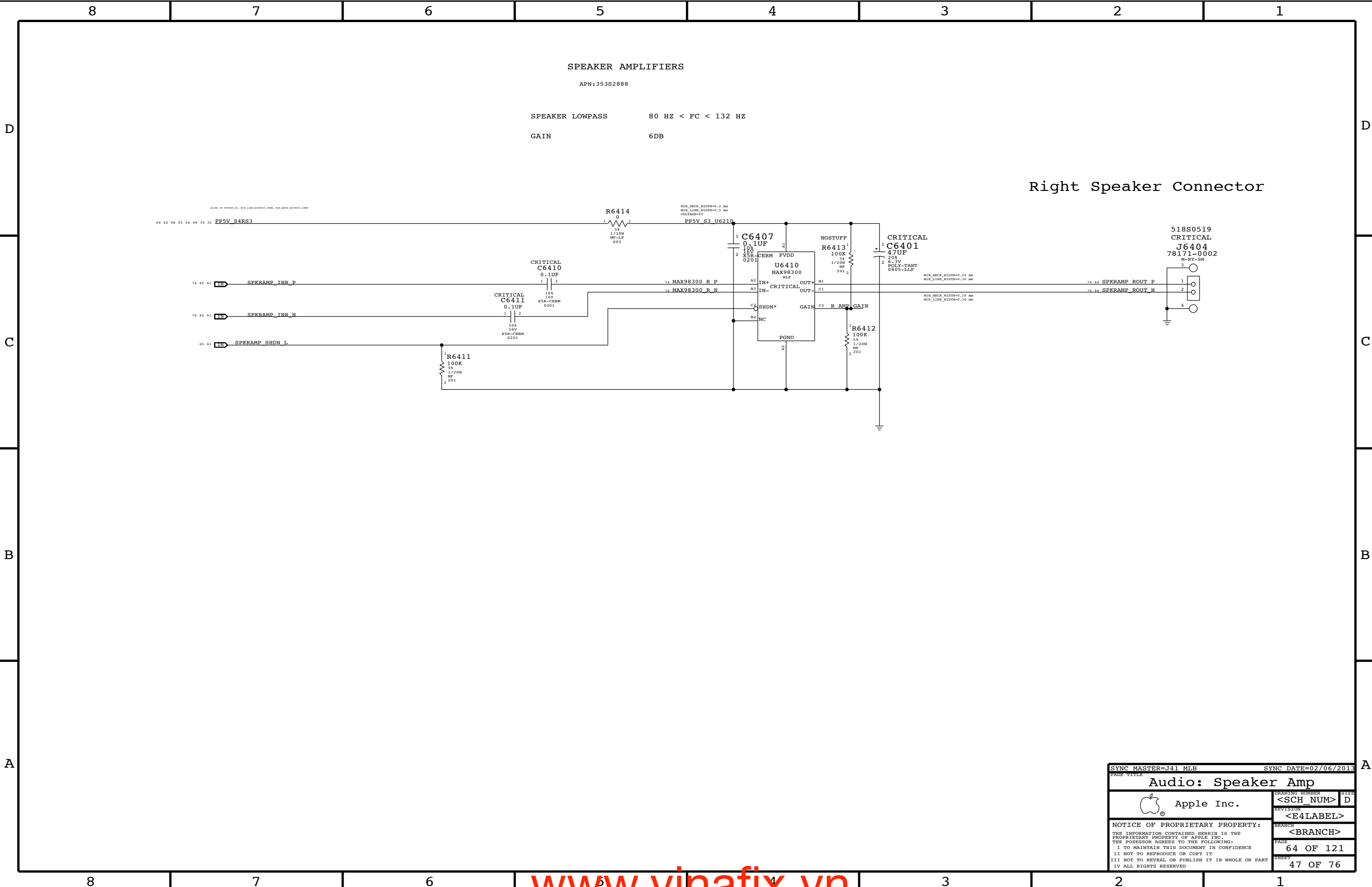
# FAN CONNECTOR

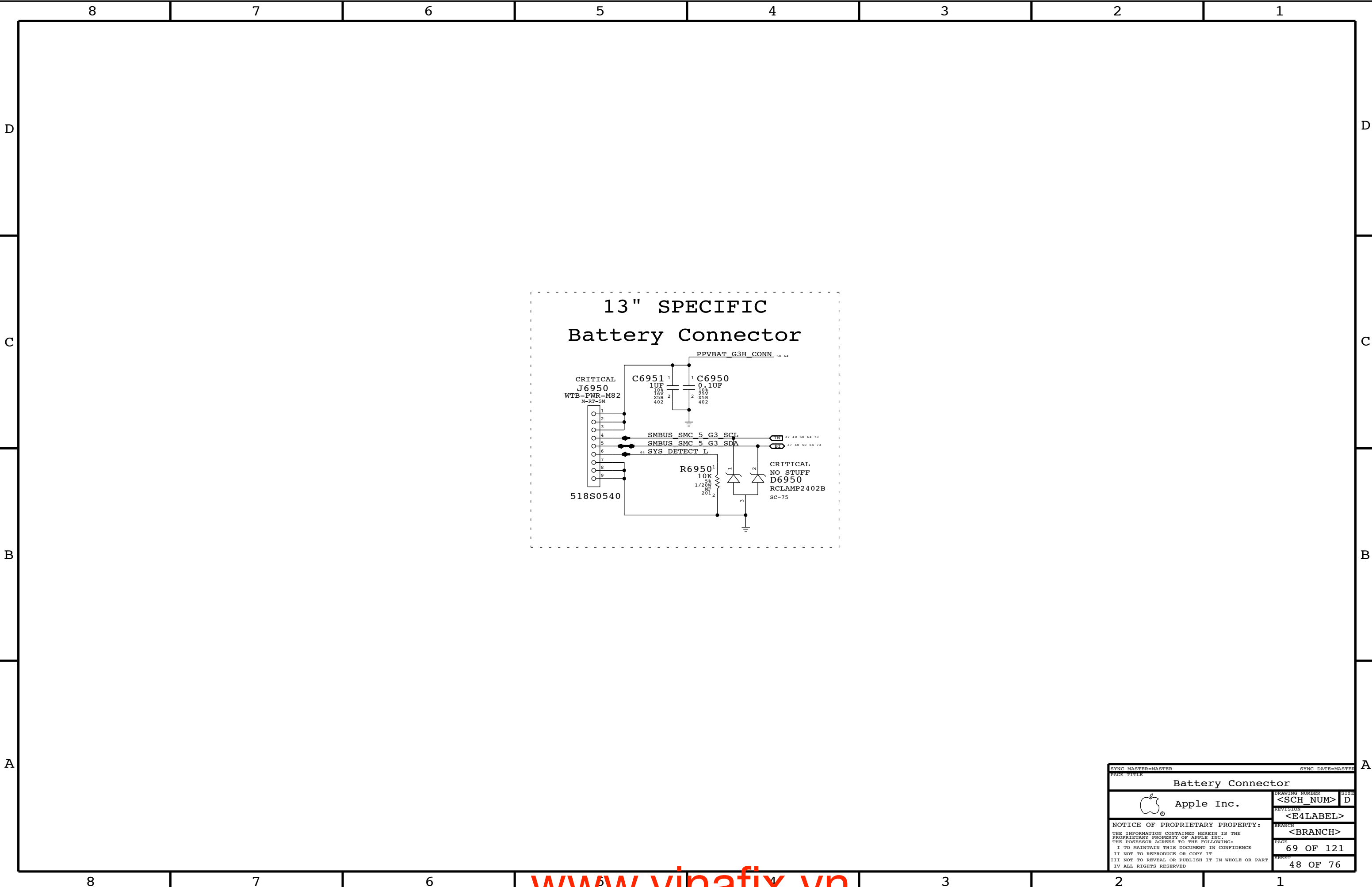


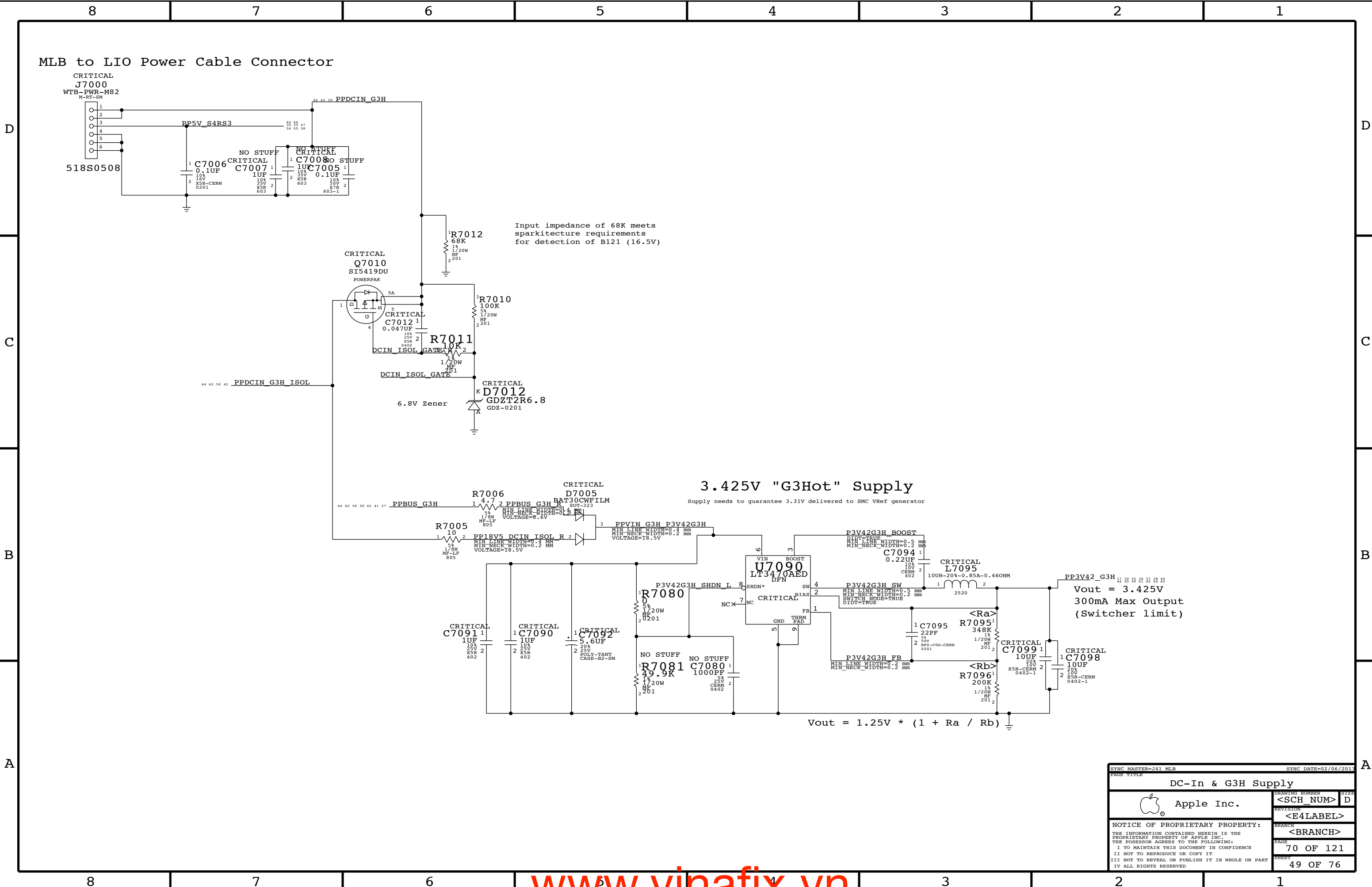





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LPC+SPI Debug Connector			
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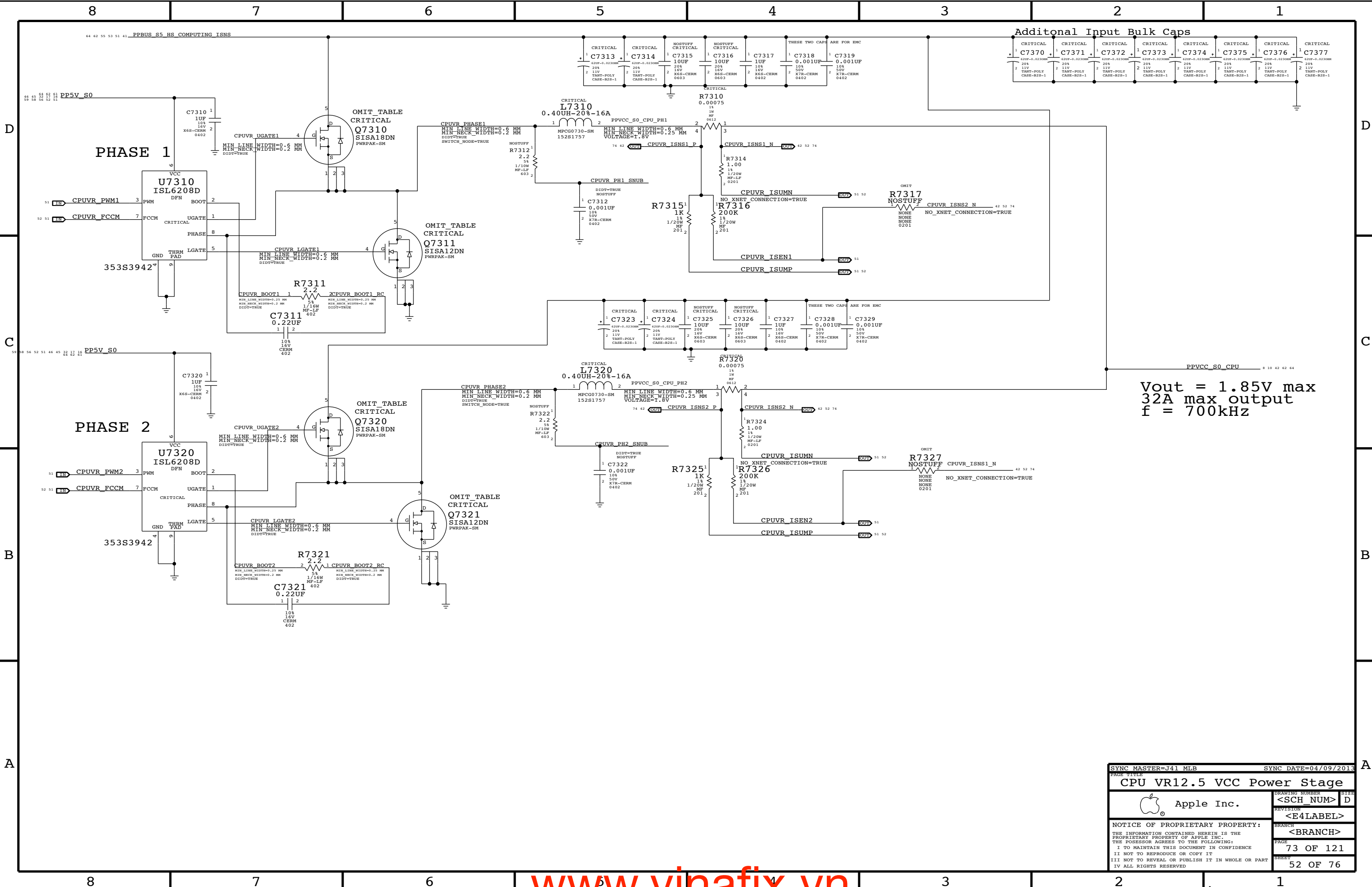


SYNC MASTER=J41 MLB		SYNC DATE=02/06/2013	
PAGE TITLE			
DC-In & G3H Supply			
 Apple Inc.	DRAWING NUMBER	SIZE	
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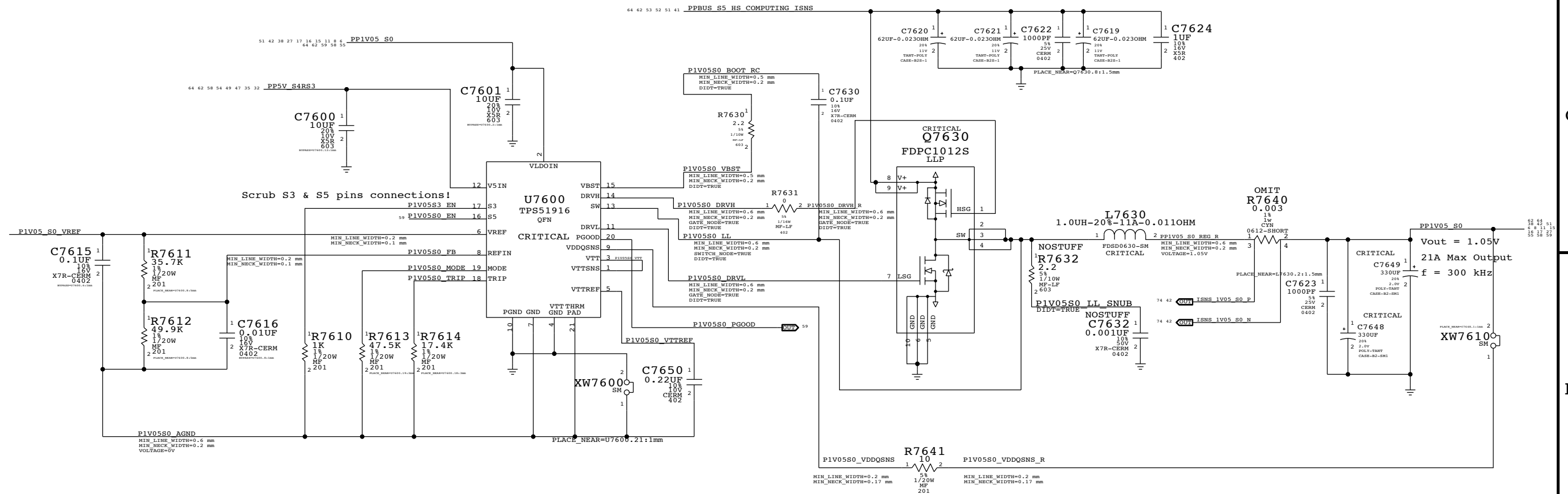
Vout = 1.85V max  
32A max output  
f = 700kHz


SYNC MASTER=J41 MLB		SYNC DATE=04/09/2013	
PAGE TITLE			
CPU VR12.5 VCC Power Stage			
	Apple Inc.		
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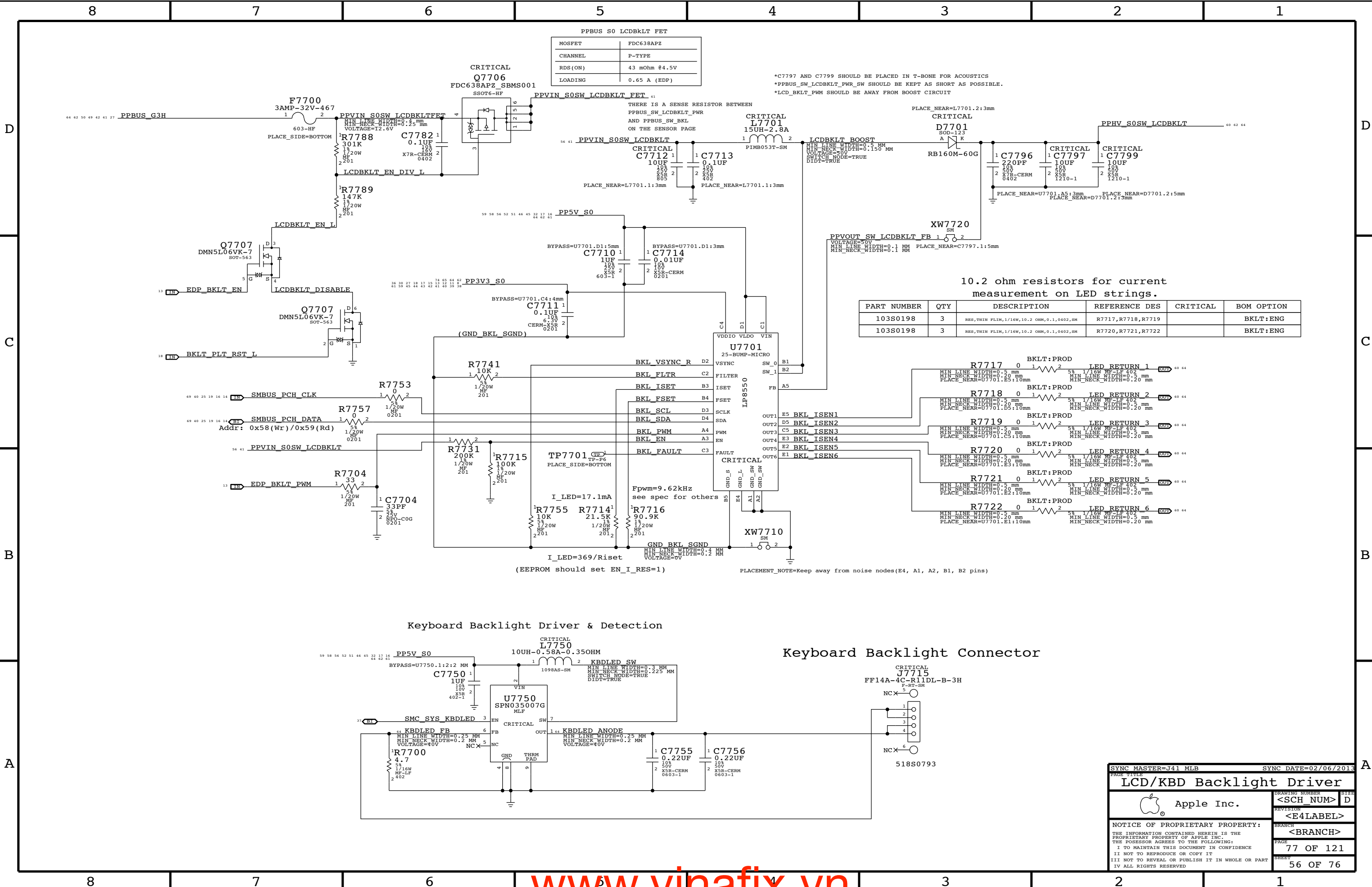


# 1.05V S0 Regulator



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PAGE TITLE			
1.05V S0 Power Supply			
 Apple Inc.	DRAWING NUMBER	SIZE	
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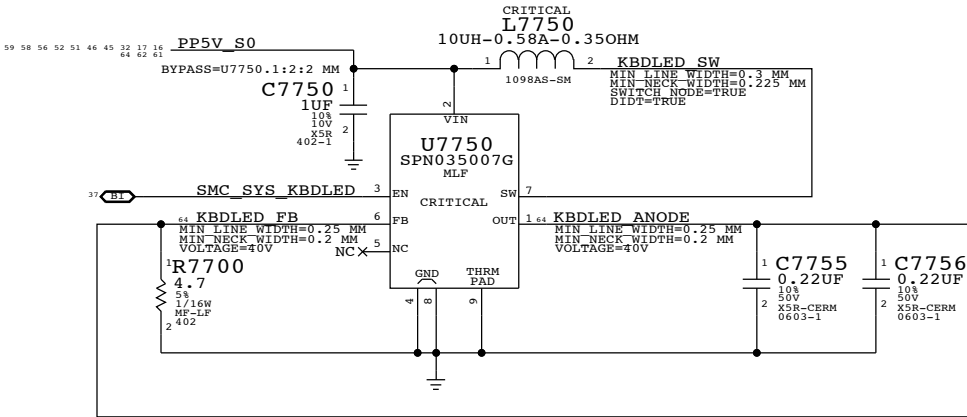


PPBUS S0 LCDBKLT FET	
MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.65 A (EDP)

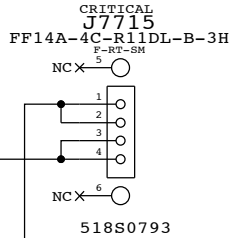
\*C7797 AND C7799 SHOULD BE PLACED IN T-BONE FOR ACOUSTICS  
\*PPBUS\_SW LCDBKLT\_PWR\_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.  
\*LCD\_BKLT\_PWM SHOULD BE AWAY FROM BOOST CIRCUIT


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES, THIN FILM, 1/16W, 10.2 OHM, 0.1, 0402, SM	R7717, R7718, R7719		BKLT:ENG
103S0198	3	RES, THIN FILM, 1/16W, 10.2 OHM, 0.1, 0402, SM	R7720, R7721, R7722		BKLT:ENG

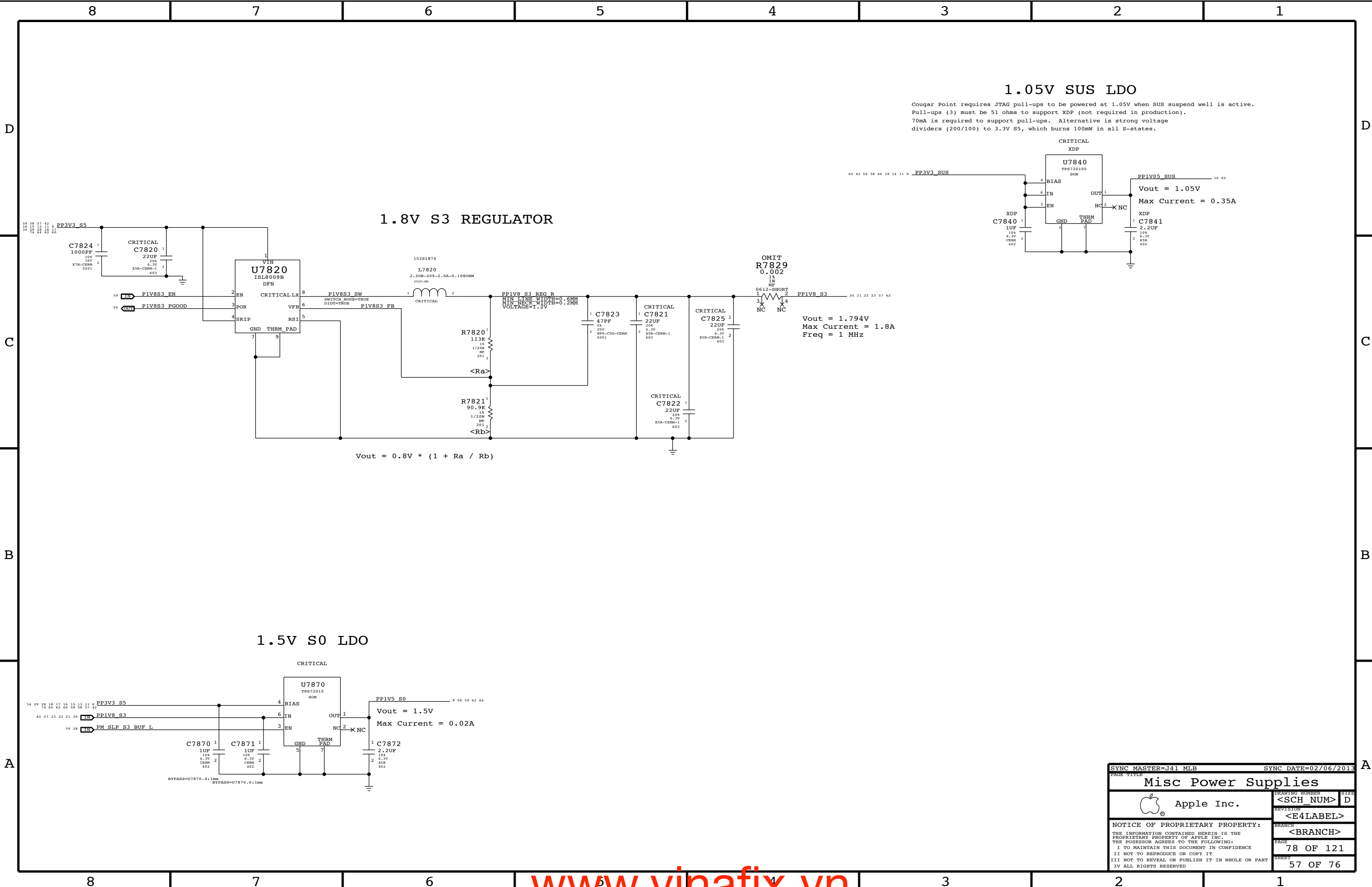
Keyboard Backlight Driver & Detection



Keyboard Backlight Connector

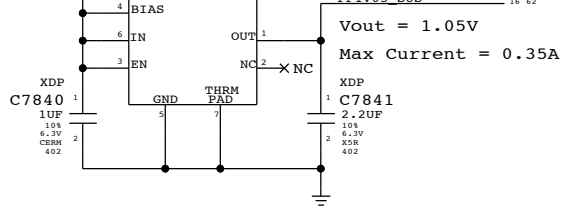


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LCD/KBD Backlight Driver			
 Apple Inc.		DRAWING NUMBER	SIZE
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**1.05V SUS LDO**

Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.




**1.8V S3 REGULATOR**

OMIT  
R7829  
0.002

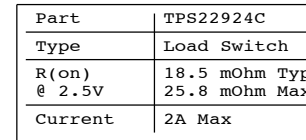
Vout = 1.794V  
Max Current = 1.8A  
Freq = 1 MHz

**1.5V S0 LDO**

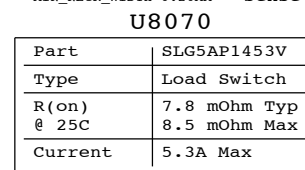
Vout = 1.5V  
Max Current = 0.02A

SYNC MASTER=J41 MLB		SYNC DATE=02/06/2013	
PAGE TITLE			
Misc Power Supplies			
 Apple Inc.		DRAWING NUMBER	SIZE
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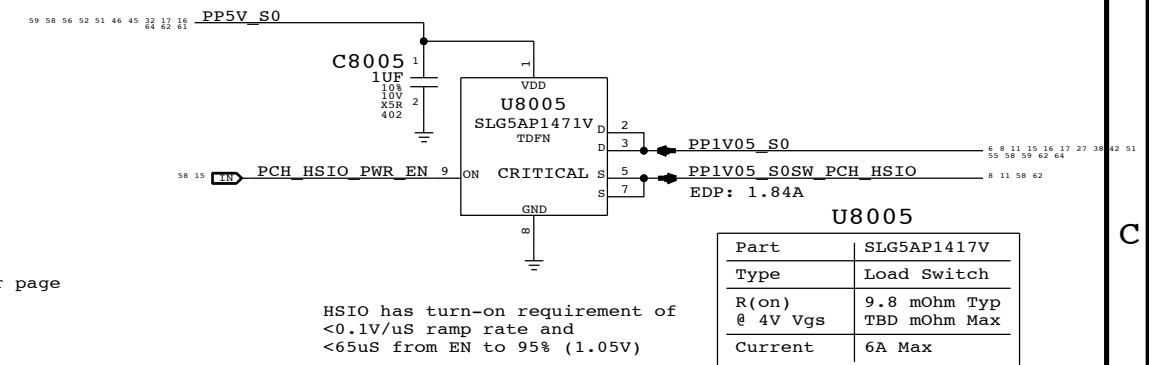
## Loading specs per J41/43\_PowerBudget\_Riviera\_rev0.99e



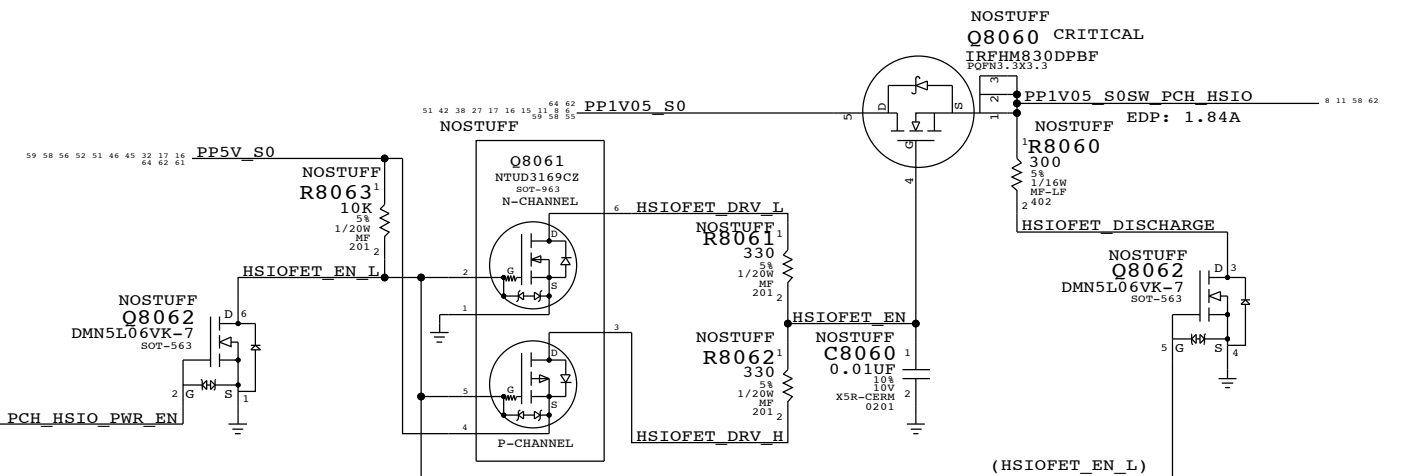
### 3.3V SSD Switch



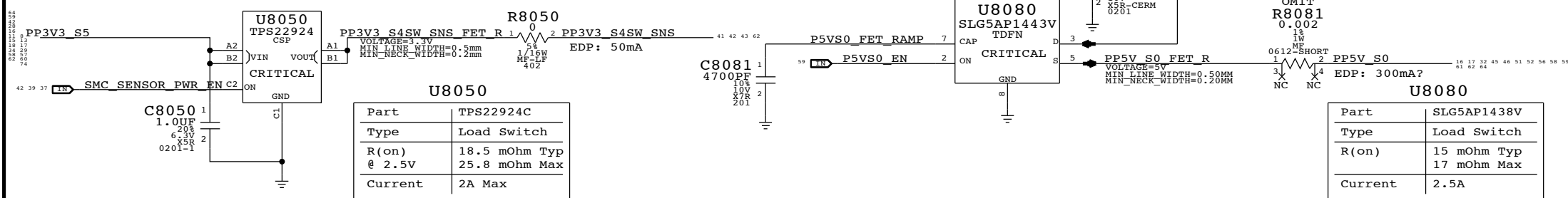
## 1.05V PCH HSIO Switch




5V S0 Switch

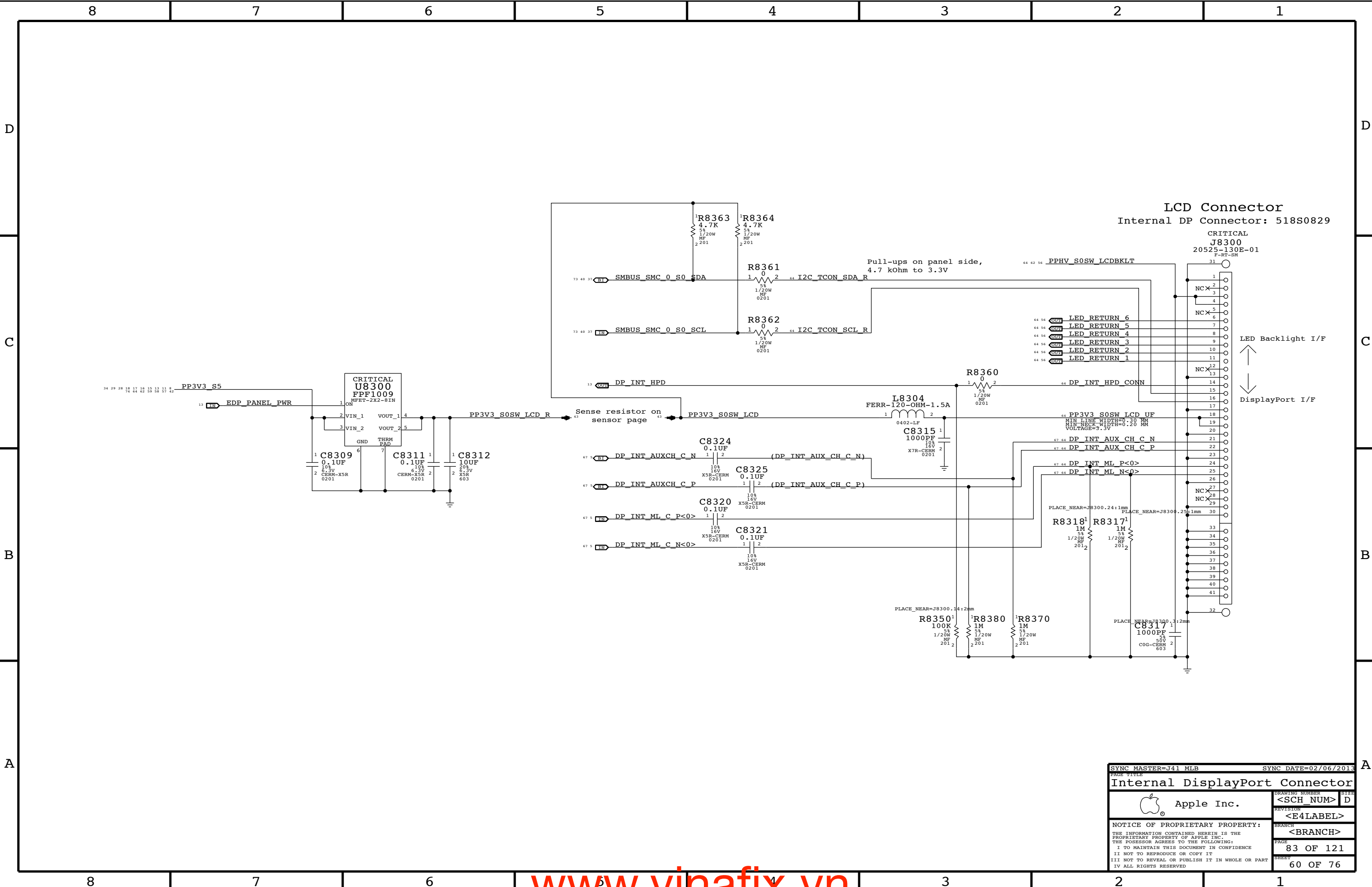



www.vinafix.vn



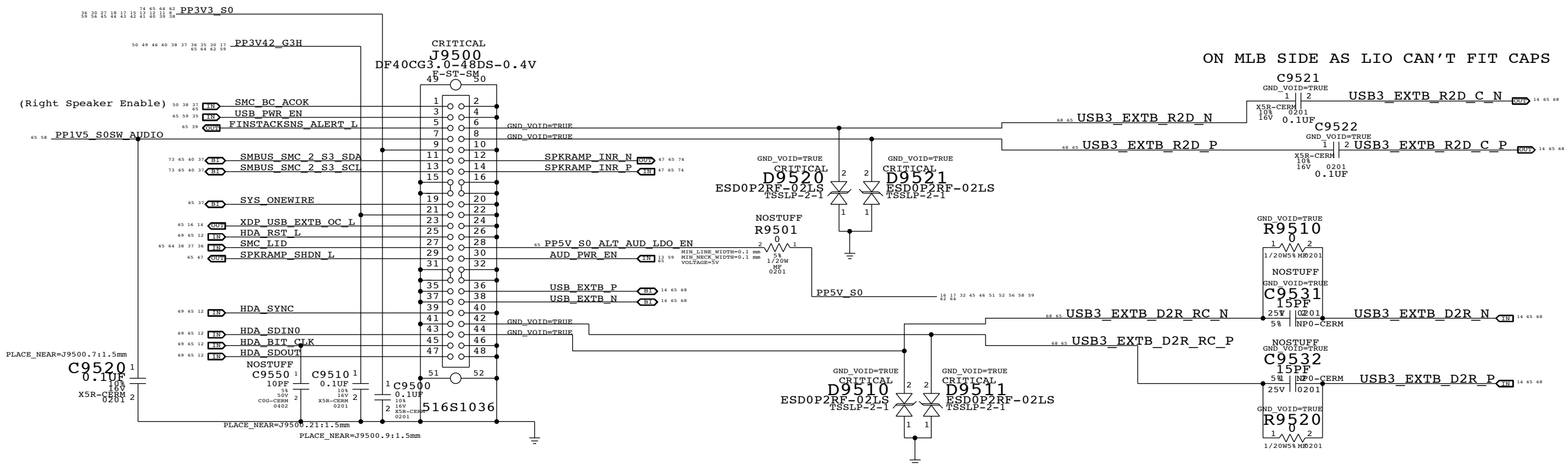
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Power FETs			
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Internal DisplayPort Connector			
 Apple Inc.		DRAWING NUMBER	SIZE
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SYNC MASTER=CLEAN J43		SYNC DATE=11/13/2012	
PAGE TITLE			
Left I/O (LIO) Connector			
 Apple Inc.		DRAWING NUMBER	SIZE
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Memory Bit/Byte Swizzle															
D															
C															
B															
A															
www.vinafix.vn															
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## NO\_TEST Nets


		NO TEST		MAKE BASE	
64	NC_PCIE_CLK100M_SDP	TRUE	TRUE	NC_PCIE_CLK100M_SDP	64
	NC_PCIE_CLK100M_SDN	TRUE	TRUE	NC_PCIE_CLK100M_SDN	
64 12	NC_PCIE_CLK100M_FWP	TRUE	TRUE	NC_PCIE_CLK100M_FWP	12
64 12	NC_PCIE_CLK100M_FWN	TRUE	TRUE	NC_PCIE_CLK100M_FWN	12
64 14	NC_PCIE_FW_D2RP	TRUE	TRUE	NC_PCIE_FW_D2RP	14
64 14	NC_PCIE_FW_D2RN	TRUE	TRUE	NC_PCIE_FW_D2RN	14
64 14	NC_PCIE_FW_R2D_CP	TRUE	TRUE	NC_PCIE_FW_R2D_CP	14
64 14	NC_PCIE_FW_R2D_CN	TRUE	TRUE	NC_PCIE_FW_R2D_CN	14
64 14	NC_USB_IRP	TRUE	TRUE	NC_USB_IRP	14
64 14	NC_USB_IRN	TRUE	TRUE	NC_USB_IRN	14
64 14	NC_USB_CAMERAP	TRUE	TRUE	NC_USB_CAMERAP	14
64 14	NC_USB_CAMERAN	TRUE	TRUE	NC_USB_CAMERAN	14
64 14	NC_USB_SDP	TRUE	TRUE	NC_USB_SDP	14
64 14	NC_USB_SDN	TRUE	TRUE	NC_USB_SDN	14
67	DP_INT_ML_C_P<3..1>	TRUE	TRUE	NC_INT_ML_CP<3..1>	6
67	DP_INT_ML_C_N<3..1>	TRUE	TRUE	NC_INT_ML_CN<3..1>	6
64 12	NC_HDA_SDI1	TRUE	TRUE	NC_HDA_SDI1	12
64 13	NC_PCI_PME_L	TRUE	TRUE	NC_PCI_PME_L	13
64 14	NC_CLINK_CLK	TRUE	TRUE	NC_CLINK_CLK	14
64 14	NC_CLINK_DATA	TRUE	TRUE	NC_CLINK_DATA	14
64 14	NC_CLINK_RESET_L	TRUE	TRUE	NC_CLINK_RESET_L	14

64	37	NC_SMC_SYS_LED	TRUE	TRUE	NC_SMC_SYS_LED	37	64
64		NC_IR_RX_OUT_RC	TRUE	TRUE	NC_IR_RX_OUT_RC		64
64		NC_USB_SMC_P	TRUE	TRUE	NC_USB_SMC_P		64
64		NC_USB_SMC_N	TRUE	TRUE	NC_USB_SMC_N		64
64	37	NC_SMC_GFX_OVERTEMP	TRUE	TRUE	NC_SMC_GFX_OVERTEMP	37	64
64	37	NC_SMC_GFX_THROTTLE_L	TRUE	TRUE	NC_SMC_GFX_THROTTLE_L	37	64
64	37	NC_SMC_FAN_1_CTL	TRUE	TRUE	NC_SMC_FAN_1_CTL	37	64
64	37	NC_SMC_FAN_1_TACH	TRUE	TRUE	NC_SMC_FAN_1_TACH	37	64
64	37	NC_SMC_FAN_5_CTL	TRUE	TRUE	NC_SMC_FAN_5_CTL	37	64
64		NC_ENET_ASF_GPIO	TRUE	TRUE	NC_ENET_ASF_GPIO		64
64		NC_SMC_MPM5_LED_PWR	TRUE	TRUE	NC_SMC_MPM5_LED_PWR		64
64		NC_SMC_MPM5_LED_CHG	TRUE	TRUE	NC_SMC_MPM5_LED_CHG		64
64	37	NC_SMC_T25_EN_L	TRUE	TRUE	NC_SMC_T25_EN_L	37	64
64	37	NC_SMC_DP_HPD_L	TRUE	TRUE	NC_SMC_DP_HPD_L	37	64
64	37	NC_SMBUS_SMC_4_ASF_SCL	TRUE	TRUE	NC_SMBUS_SMC_4_ASF_SCL	37	64
64	37	NC_SMBUS_SMC_4_ASF_SDA	TRUE	TRUE	NC_SMBUS_SMC_4_ASF_SDA	37	64
64	37	NC_BDV_BKL_PWM	TRUE	TRUE	NC_BDV_BKL_PWM	37	64

71	TBT_B R2D_C P<1..0>	TRUE	TRUE	NC	TBT_B R2D_CP<1..0>	25
71	TBT_B R2D_C N<1..0>	TRUE	TRUE	NC	TBT_B R2D_CN<1..0>	25
71	TBT_B D2R_P<1..0>	TRUE	TRUE	NC	TBT_B D2R_P<1..0>	25
71	TBT_B D2R_N<1..0>	TRUE	TRUE	NC	TBT_B D2R_N<1..0>	25
64 25	NC_TBT_B LSTX	TRUE	TRUE	NC	TBT_B LSTX	25 64
71 64	NC_DP_TBTBP ML_CP<3..1:2>	TRUE	TRUE	NC	DP_TBTBP ML_CP<3..1:2>	64 71
71 64	NC_DP_TBTBP ML_CN<3..1:2>	TRUE	TRUE	NC	DP_TBTBP ML_CN<3..1:2>	64 71
71 64 25	NC_DP_TBTBP_AUXCH_CP	TRUE	TRUE	NC	DP_TBTBP_AUXCH_CP	25 64 71
	NC_DP_TBTBP_AUXCH_CN	TRUE	TRUE	NC	DP_TBTBP_AUXCH_CN	

64	25	NC	DP	TBTBP	AUXCH	CN		TRUE	TRUE	NC	DP	TBTBP	AUXCH	CN		25	64
		TP	DP	TBTSRC	ML	CP<3>		TRUE	TRUE	NC	DP	TBTSRC	ML	CP<3>			
	25	TP	DP	TBTSRC	ML	CN<3>		TRUE	TRUE	NC	DP	TBTSRC	ML	CN<3>			
		TP	DP	TBTSRC	ML	CP<2>		TRUE	TRUE	NC	DP	TBTSRC	ML	CP<2>			
	25	TP	DP	TBTSRC	ML	CN<2>		TRUE	TRUE	NC	DP	TBTSRC	ML	CN<2>			
64	25	NC	DP	TBTSRC	ML	CP<1>		TRUE	TRUE	NC	DP	TBTSRC	ML	CP<1>		25	64
		NC	DP	TBTSRC	ML	CN<1>		TRUE	TRUE	NC	DP	TBTSRC	ML	CN<1>			
64	25	TP	DP	TBTSRC	ML	CP<0>		TRUE	TRUE	NC	DP	TBTSRC	ML	CP<0>		25	64
	25	TP	DP	TBTSRC	ML	CN<0>		TRUE	TRUE	NC	DP	TBTSRC	ML	CN<0>			
64	25	NC	DP	TBTSRC	AUXCH	CP		TRUE	TRUE	NC	DP	TBTSRC	AUXCH	CP		25	64
		NC	DP	TBTSRC	AUXCH	CN		TRUE	TRUE	NC	DP	TBTSRC	AUXCH	CN			

HDD_PWR_EN	15
WOL_EN	14
BT_PWRST_L	15
HDMITBTMUX_FLAG_L	15
FW_PWR_EN	15
FW_PME_L	15
ENET_MEDIA_SENSE	15
LCD_PSR_EN	15
LCD_IRQ_L	15
ODD_PWR_EN_L	15
ENET_LOW_PWR	13
AUD_IP_PERIPHERAL_DET	13
AUD_I2C_INT_L	13
AUD_IPHS_SWITCH_EN	13

SYNC MASTER=J41 MLB		SYNC DATE=02/01/2013	
PAGE TITLE			
Func Test / No Test			
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## Functional Test Points

## SD Card Aliases

J9500: LIO Connector

FUNC\_TEST

TRUE	PP3V42_G3H	17	26	35	37	38	40	46	49	50
TRUE	PP3V3_S0	58	61	62	64					
TRUE	PP1V5_S0SW_AUDIO	8	21	22	13	62	64	74		
TRUE	SYS_ONEWIRE	39	40	41	42	43	44	45	56	59
TRUE	SMC_BC_ACOK	37	61							
TRUE	USB_PWR_EN	37	38	50	61					
TRUE	SMBUS_SMC_2_S3_SDA	35	59	61						
TRUE	SMBUS_SMC_2_S3_SCL	37	40	61	73					
TRUE	SPKRAMP_SHDN_L	37	40	61	73					
		47	61							

MAKE\_BASE

68	65	34	14	<u>USB3_SD_D2R_P</u>	<u>==</u>	<u>TRUE</u>	<u>USB3_SD_D2R_P</u>	14	34	65	68
68	65	34	14	<u>USB3_SD_D2R_N</u>	<u>==</u>	<u>TRUE</u>	<u>USB3_SD_D2R_N</u>	14	34	65	68
68	65	34	14	<u>USB3_SD_R2D_C_P</u>	<u>==</u>	<u>TRUE</u>	<u>USB3_SD_R2D_C_P</u>	14	34	65	68
68	65	34	14	<u>USB3_SD_R2D_C_N</u>	<u>==</u>	<u>TRUE</u>	<u>USB3_SD_R2D_C_N</u>	14	34	65	68
65	39	37	34	<u>PP3V3_S0SW_SD</u>	<u>==</u>	<u>PP3V3_S0SW_SD</u>		15	34	37	39

(MAKE\_BASE=TRUE on page 45)







## SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ICOMP	*	=4x_DIELECTRIC	?

SOURCE: 471984\_Chief River\_MS\_PDQ 1.0 and the spacing rule is adjusted per SI team feedback.

## UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x_DIELECTRIC	?

## USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?	USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905\_v1.5), Section 3.8

## USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_PCH_TX	USB3_PCH_TX	*	USB3_TX2TX	USB3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_RX	USB3_PCH_RX	*	USB3_RX2RX	USB3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2OTHERTX	USB3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2OTHERRX	USB3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_TX	*_PCH_RX	*	USB3_TX2RX	USB3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_PCH_RX	*_PCH_TX	*	USB3_RX2TX	USB3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_PCH_TX	*_TX	*	USB3_2OTHERHS	USB3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_PCH_RX	*_TX	*	USB3_2OTHERHS	USB3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_TX	*_RX	*	USB3_2OTHERHS				
USB3_PCH_RX	*_RX	*	USB3_2OTHERHS				
USB3_PCH_TX	*	*	USB3_2OTHER				
USB3_PCH_RX	*	*	USB3_2OTHER				

SOURCE: 471984 Cheif River MS PDG 1.0 and the spacing rule is adjusted per SI team feedback.

## PCH Net Properties


ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP
	USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_P
	USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_N
	USB_BT	USB_80D	USB	USB_BT_P
	USB_BT	USB_80D	USB	USB_BT_N
		USB_80D	USB	USB_BT_CONN_P
		USB_80D	USB	USB_BT_CONN_N
		USB_80D	USB	USB_BT_WAKE_P
		USB_80D	USB	USB_BT_WAKE_N
	USB_TPAD	USB_80D	USB	USB_TPAD_P
	USB_TPAD	USB_80D	USB	USB_TPAD_N
		USB_80D	USB	USB_TPAD_CONN_P
		USB_80D	USB	USB_TPAD_CONN_N
		USB_80D	USB	TPAD_SPI_MOSI_USB_P
		USB_80D	USB	TPAD_SPI_MISO_USB_N
	USB_TPAD_M	USB_80D	USB	USB_TPAD_M_P
	USB_TPAD_M	USB_80D	USB	USB_TPAD_M_N
	USB_SD_CARD	USB_80D	USB	USB_SD_CARD_P
	USB_SD_CARD	USB_80D	USB	USB_SD_CARD_N
		SPT_45S	SPT	TPAD_SPI_MOSI
		SPT_45S	SPT	TPAD_SPI_MISO
		SPT_45S	SPT	TPAD_SPI_CLK
	USB_EXT_A	USB_80D	USB	USB_EXT_A_P
	USB_EXT_A	USB_80D	USB	USB_EXT_A_N
		UART_45S	UART	SMC_DEBUGPRT_TX_L
		UART_45S	UART	SMC_DEBUGPRT_RX_L
	USB2_EXT_A	USB_80D	USB	USB2_EXT_A_MUXED_P
	USB2_EXT_A	USB_80D	USB	USB2_EXT_A_MUXED_N
	USB2_EXT_A	USB_80D	USB	USB2_EXT_A_MUXED_F_P
	USB2_EXT_A	USB_80D	USB	USB2_EXT_A_MUXED_F_N
	USB3_EXT_A_RX	USB_80D	USB3_PCH_RX	USB3_EXT_A_D2R_P
	USB3_EXT_A_RX	USB_80D	USB3_PCH_RX	USB3_EXT_A_D2R_N
	USB3_EXT_A_TX	USB_80D	USB3_PCH_TX	USB3_EXT_A_R2D_P
	USB3_EXT_A_TX	USB_80D	USB3_PCH_TX	USB3_EXT_A_R2D_N
		USB_80D	USB3_PCH_RX	USB3_EXT_A_D2R_F_P
		USB_80D	USB3_PCH_RX	USB3_EXT_A_D2R_F_N
		USB_80D	USB3_PCH_TX	USB3_EXT_A_R2D_F_P
		USB_80D	USB3_PCH_TX	USB3_EXT_A_R2D_F_N
		USB_80D	USB3_PCH_TX	USB3_EXT_A_R2D_C_P
		USB_80D	USB3_PCH_TX	USB3_EXT_A_R2D_C_N
	USB_EXT_B	USB_80D	USB	USB_EXT_B_P
	USB_EXT_B	USB_80D	USB	USB_EXT_B_N
	USB3_EXT_B_RX	USB_80D	USB3_PCH_RX	USB3_EXT_B_D2R_P
	USB3_EXT_B_RX	USB_80D	USB3_PCH_RX	USB3_EXT_B_D2R_N
		USB_80D	USB3_PCH_RX	USB3_EXT_B_D2R_RC_P
		USB_80D	USB3_PCH_RX	USB3_EXT_B_D2R_RC_N
	USB3_EXT_B_TX	USB_80D	USB3_PCH_TX	USB3_EXT_B_R2D_P
	USB3_EXT_B_TX	USB_80D	USB3_PCH_TX	USB3_EXT_B_R2D_N
		USB_80D	USB3_PCH_TX	USB3_EXT_B_R2D_C_P
		USB_80D	USB3_PCH_TX	USB3_EXT_B_R2D_C_N
	USB3_SD_RX	USB_80D	USB3_PCH_RX	USB3_SD_D2R_P
	USB3_SD_RX	USB_80D	USB3_PCH_RX	USB3_SD_D2R_N
	USB3_SD_TX	USB_80D	USB3_PCH_TX	USB3_SD_R2D_C_P
	USB3_SD_TX	USB_80D	USB3_PCH_TX	USB3_SD_R2D_C_N
		USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_P
		USB_80D	USB3_PCH_TX	USB3_SD_D2R_C_N
		USB_80D	USB3_PCH_TX	USB3_SD_R2D_P
		USB_80D	USB3_PCH_TX	USB3_SD_R2D_N
	PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS
	PCH_DIFFCLK_UNUSED	CLK_PCTE_80D	CLK_PCTE	PCTE_CLK100M_PCH_P
	PCH_DIFFCLK_UNUSED	CLK_PCTE_80D	CLK_PCTE	PCTE_CLK100M_PCH_N
	PCH_DIFFCLK_UNUSED	CLK_PCTE_80D	CLK_PCTE	PCH_CLK96M_DOT_P
	PCH_DIFFCLK_UNUSED	CLK_PCTE_80D	CLK_PCTE	PCH_CLK96M_DOT_N
	PCH_DIFFCLK_UNUSED	CLK_PCTE_80D	CLK_PCTE	PCH_CLK100M_SATA_P
	PCH_DIFFCLK_UNUSED	CLK_PCTE_80D	CLK_PCTE	PCH_CLK100M_SATA_N
		CPU_45S	CLK_PCTE	PCH_CLK14P3M_REFCLK

## USB Hucopyb nets

TP SPI nets

USB EXTA nets (Right USB port)

USB EXTB nets (Left USB port)

SYNCH MASTER=CLEAN J43		SYNCH DATE=11/13/2012	
PAGE TITLE			
PCH Constraints 1			
 Apple Inc.		DRAWING NUMBER <b>&lt;SCH NUM&gt;</b>	
		SIZE <b>D</b>	
		REVISION <b>&lt;E4LABEL&gt;</b>	
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## LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x_DIELECTRIC	?
CLK_LPC	*	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905\_v1.5), Section 3.15

## SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S_R_50S	TOP,BOTTOM	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE		
SMB_45S_R_50S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

## HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905\_v1.5), Section 3.15

## SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?

## SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x_DIELECTRIC	?

## XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_ITP	*	=2:1_SPACING	?

## DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	*	=3x_DIELECTRIC	?
DP_2OTHERHS	*	=4x_DIELECTRIC	?
DP_2OTHER	*	=3x_DIELECTRIC	?
DP_AUX	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_AUX	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_TX	DP_TX	*	DP_2DP
DP_TX	*_TX	*	DP_2OTHERHS
DP_TX	*_RX	*	DP_2OTHERHS
DP_TX	*	*	DP_2OTHER

## System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
















SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

## PCH Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
	PHYSICAL	SPACING		
LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	14 37 46 64
LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L	14 37 46 64
LPC_CLK33M	LPC_45S	LPC	LPCPLUS_RESET_L	18 46 64
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC	17 37
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC_R	12 17
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS	17 46 64
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS_R	12 17
SMBUS_PCH_CLK	SMB_45S_R_50S	SMB	SMBUS_PCH_CLK	14 16 19 25 40 56
SMBUS_PCH_DATA	SMB_45S_R_50S	SMB	SMBUS_PCH_DATA	14 16 19 25 40 56
SMBUS_PCH_0_CLK	SMB_45S_R_50S	SMB	SMB_PCH_0_CLK	14 40
SMBUS_PCH_0_DATA	SMB_45S_R_50S	SMB	SMB_PCH_0_DATA	14 40
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL	14 32 37 40 43 44 64
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA	14 32 37 40 43 44 64
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	12 61 65
HDA_BIT_CLK_R	HDA_45S	HDA	HDA_BIT_CLK_R	12
HDA_SYNC	HDA_45S	HDA	HDA_SYNC	12 61 65
HDA_SYNC_R	HDA_45S	HDA	HDA_SYNC_R	12
HDA_RST_L	HDA_45S	HDA	HDA_RST_R_L	12
HDA_RST_L	HDA_45S	HDA	HDA_RST_L	12 61 65
HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0	12 61 65
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	12 61 65
HDA_SDOUT_R	HDA_45S	HDA	HDA_SDOUT_R	12 17
PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM_CLK32K_SUSCLK_R	13 38
SPT_CLK	CLK_SLOW_45S	CLK_SLOW	SMC_CLK32K	37 38
SPT_CLK	SPT_45S	SPT	SPI_CLK_R	14 46
SPT_CLK	SPT_45S	SPT	SPI_CLK	46
SPT_MOSI	SPT_45S	SPT	SPI_MOSI_R	14 46
SPT_MOSI	SPT_45S	SPT	SPI_MOSI	46
SPT_MISO	SPT_45S	SPT	SPI_MISO	14 46
SPT_MISO	SPT_45S	SPT	SPI_MISO_R	46
SPT_CS0	SPT_45S	SPT	SPI_CS0_R_L	14 46
SPT_CS0	SPT_45S	SPT	SPI_CS0_L	46
SPT_CS0	SPT_45S	SPT	SPI_SMC_CLK	37 46
SPT_CS0	SPT_45S	SPT	SPI_SMC_MOSI	37 46
SPT_CS0	SPT_45S	SPT	SPI_SMC_MISO	37 46
SPT_CS0	SPT_45S	SPT	SPI_SMC_CS_L	37 46
SPT_CS0	SPT_45S	SPT	SPI_MLB_CLK	46
SPT_CS0	SPT_45S	SPT	SPI_MLB_MOSI	46
SPT_CS0	SPT_45S	SPT	SPI_MLB_MISO	46
SPT_CS0	SPT_45S	SPT	SPI_MLB_CS_L	46
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_P	29 64
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_N	29 64
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_P	14 29
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_N	14 29
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_P	14 29 64
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_N	14 29 64
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_P	12 29 64
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_N	12 29 64
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_P<3..0>	25
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_N<3..0>	25
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_P<3..0>	14 25
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_N<3..0>	14 25
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_P<3..0>	14 25
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_N<3..0>	14 25
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_P<3..0>	25
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_N<3..0>	25
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_P	12 25
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_N	12 25
CLK_PCIE_80D	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_P	
CLK_PCIE_80D	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_N	
XDP_TDI	PCH_45S	PCH_ITP	XDP_PCH_TDI	12 16 64
XDP_TDO	PCH_45S	PCH_ITP	XDP_PCH_TDO	12 16 64
XDP_TMS	PCH_45S	PCH_ITP	XDP_PCH_TMS	12 16 64
XDP_TCK	PCH_45S	PCH_ITP	XDP_PCH_TCK	12 16 64
PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_P	31 32
PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_N	31 32
PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_P	14 32
PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_N	14 32
PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_P	14 32
PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_N	14 32
PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_P	31 32
PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_N	31 32
PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_P	12 32
PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_N	12 32
PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P	31 32
PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N	31 32

## Clock Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTCX1
	SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA
		CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKP
		CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP_R
		CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP
		CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALN
		CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKN
	SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT
		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R
	SYSCLK_CLK25M_XTAL	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1
		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2
		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R
		CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2
		CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2_R
		CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X1



## Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_73D	*	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF

## Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DATA2OTHERMEM	*	=8x_DIELECTRIC	?
MEM_QS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM_CMD2CTRL	*	=3x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	10000
MEM_2GND	*	=2x_DIELECTRIC	10000
MEM_2OTHER	*	=6x_DIELECTRIC	?

## Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_70D	MEM_TERM	MEM_73D
MEM_40S	MEM_TERM	MEM_50S

## Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

## Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_QS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_QS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_QS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_QS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_QS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_QS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_QS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_QS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_QS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_QS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_QS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_QS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_QS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_QS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_QS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_QS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	MEM_*	*	MEM_DATA2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	*	*	MEM_2OTHER
MEM_A_DQS_1	*	*	MEM_2OTHER
MEM_A_DQS_2	*	*	MEM_2OTHER
MEM_A_DQS_3	*	*	MEM_2OTHER
MEM_A_DQS_4	*	*	MEM_2OTHER
MEM_A_DQS_5	*	*	MEM_2OTHER
MEM_A_DQS_6	*	*	MEM_2OTHER
MEM_A_DQS_7	*	*	MEM_2OTHER
MEM_B_DQS_0	*	*	MEM_2OTHER
MEM_B_DQS_1	*	*	MEM_2OTHER
MEM_B_DQS_2	*	*	MEM_2OTHER
MEM_B_DQS_3	*	*	MEM_2OTHER
MEM_B_DQS_4	*	*	MEM_2OTHER
MEM_B_DQS_5	*	*	MEM_2OTHER
MEM_B_DQS_6	*	*	MEM_2OTHER
MEM_B_DQS_7	*	*	MEM_2OTHER

MEM_A_DATA_0	*	*	MEM_2OTHER
MEM_A_DATA_1	*	*	MEM_2OTHER
MEM_A_DATA_2	*	*	MEM_2OTHER
MEM_A_DATA_3	*	*	MEM_2OTHER
MEM_A_DATA_4	*	*	MEM_2OTHER
MEM_A_DATA_5	*	*	MEM_2OTHER
MEM_A_DATA_6	*	*	MEM_2OTHER
MEM_A_DATA_7	*	*	MEM_2OTHER
MEM_B_DATA_0	*	*	MEM_2OTHER
MEM_B_DATA_1	*	*	MEM_2OTHER
MEM_B_DATA_2	*	*	MEM_2OTHER
MEM_B_DATA_3	*	*	MEM_2OTHER
MEM_B_DATA_4	*	*	MEM_2OTHER
MEM_B_DATA_5	*	*	MEM_2OTHER
MEM_B_DATA_6	*	*	MEM_2OTHER
MEM_B_DATA_7	*	*	MEM_2OTHER


MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM

## Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE		
	PHYSICAL	SPACING	
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_P<0>
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_N<0>
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_P<1>
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_N<1>
MEM_A_CTRL	MEM_40S	MEM_CTRL	MEM_A_CS_L<1..0>
MEM_A_CTRL	MEM_40S	MEM_CTRL	MEM_A_ODT<0>
MEM_A_CKE0	MEM_40S	MEM_CMD	MEM_A_CKE<1..0>
MEM_A_CKE1	MEM_40S	MEM_CMD	MEM_A_CKE<3..2>
MEM_A_CMD0	MEM_40S	MEM_CMD	MEM_A_CAA<9..0>
MEM_A_CMD1	MEM_40S	MEM_CMD	MEM_A_CAB<9..0>
MEM_A_DQ_BYTE0	MEM_40S	MEM_A_DATA_0	MEM_A_DQ<7..0>
MEM_A_DQ_BYTE1	MEM_40S	MEM_A_DATA_1	MEM_A_DQ<15..8>
MEM_A_DQ_BYTE2	MEM_40S	MEM_A_DATA_2	MEM_A_DQ<23..16>
MEM_A_DQ_BYTE3	MEM_40S	MEM_A_DATA_3	MEM_A_DQ<31..24>
MEM_A_DQ_BYTE4	MEM_40S	MEM_A_DATA_4	MEM_A_DQ<39..32>
MEM_A_DQ_BYTE5	MEM_40S	MEM_A_DATA_5	MEM_A_DQ<47..40>
MEM_A_DQ_BYTE6	MEM_40S	MEM_A_DATA_6	MEM_A_DQ<55..48>
MEM_A_DQ_BYTE7	MEM_40S	MEM_A_DATA_7	MEM_A_DQ<63..56>
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_P<0>
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_N<0>
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_P<1>
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_N<1>
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_P<2>
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_N<2>
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_P<3>
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_N<3>
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_P<4>
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_N<4>
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_P<5>
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_N<5>
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_P<6>
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_N<6>
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_P<7>
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_N<7>

		MEM_PWR	PP1V2_S3
		MEM_PWR	PP0V6_S3 MEM_VREFCA_A
		MEM_PWR	PP0V6_S3 MEM_VREFDO_A
		MEM_PWR	PP0V6_S3 MEM_VREFCA_B
		MEM_PWR	PP0V6_S3 MEM_VREFDO_B

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### MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

### Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

### Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

### Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

### Memory to Power Spacing


NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

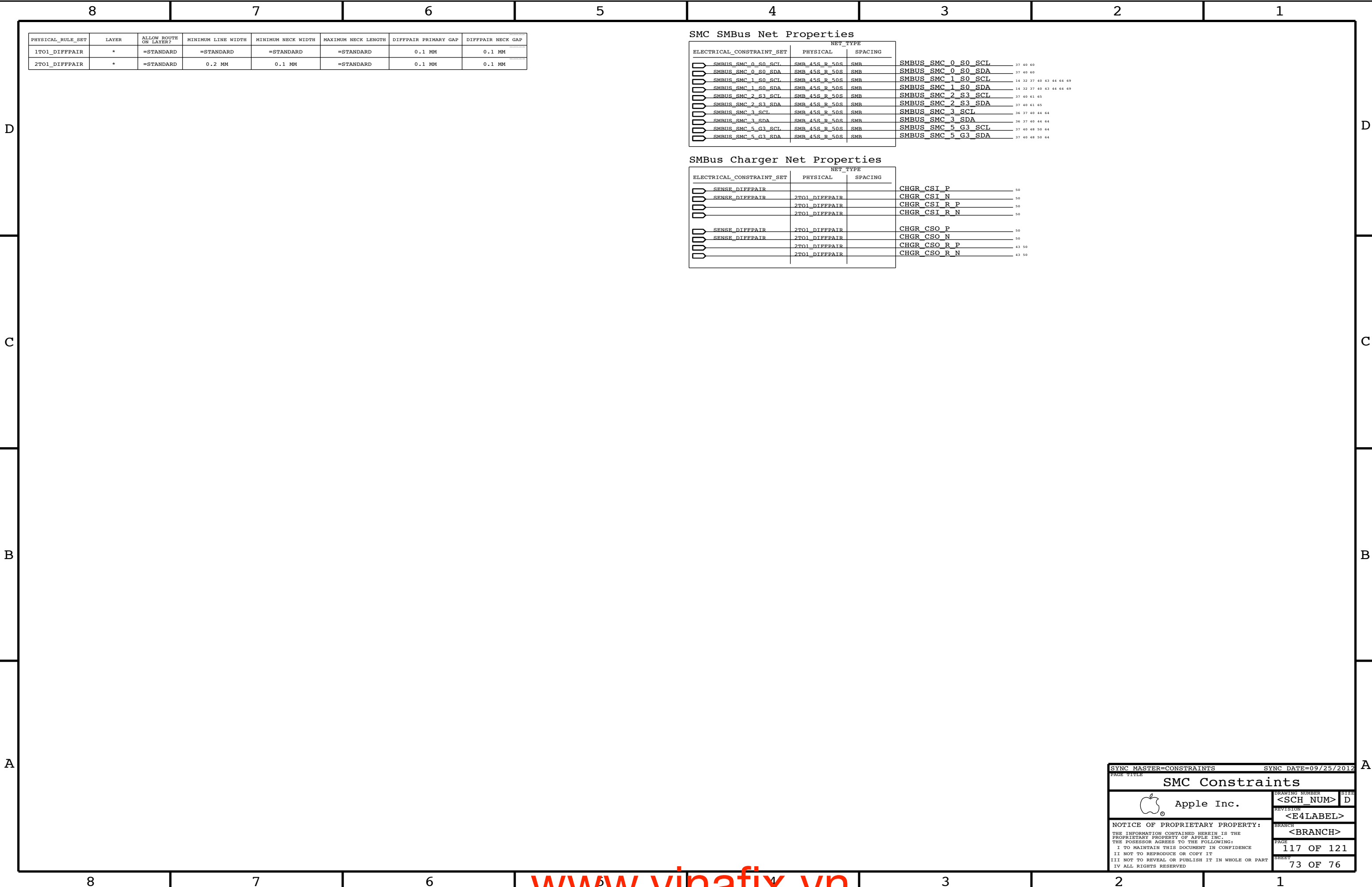
### Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

### Camera Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
S2_MEM_CLK	S2_MFM_85D	S2_MEM_CLK	MEM_CAM_CLK_P	31 32
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N	31 32
S2_MEM_CNTL	S2_MFM_45S	S2_MEM_CTRL	MEM_CAM_CKE	31 32
S2_MEM_CNTL	S2_MFM_45S	S2_MEM_CTRL	MEM_CAM_CS_L	31 32
S2_MEM_CMD	S2_MFM_45S	S2_MEM_CTRL	MEM_CAM_ODT	32
S2_MEM_CMD	S2_MFM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L	31 32
S2_MEM_CMD	S2_MFM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L	31 32
S2_MEM_CMD	S2_MFM_45S	S2_MEM_CMD	MEM_CAM_WE_L	31 32
S2_MEM_CMD	S2_MFM_45S	S2_MEM_CMD	MEM_CAM_BA<0>	31 32
S2_MEM_CMD	S2_MFM_45S	S2_MEM_CMD	MEM_CAM_BA<1>	31 32
S2_MEM_CMD	S2_MFM_45S	S2_MEM_CMD	MEM_CAM_BA<2>	31 32
S2_MEM_DQS0	S2_MFM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0>	31 32
S2_MEM_DQS0	S2_MFM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0>	31 32
S2_MEM_DQS1	S2_MFM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1>	31 32
S2_MEM_DQS1	S2_MFM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1>	31 32
S2_MEM_DATA_0	S2_MFM_45S	S2_MEM_DATA0	MEM_CAM_DM<0>	31 32
S2_MEM_DATA_1	S2_MFM_45S	S2_MEM_DATA1	MEM_CAM_DM<1>	31 32
S2_MEM_A	S2_MFM_45S	S2_MEM_CMD	MEM_CAM_A<14..0>	31 32
S2_MEM_DATA_0	S2_MFM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0>	31 32
S2_MEM_DATA_1	S2_MFM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8>	31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P	31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N	31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P	32 64
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N	32 64
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P	31 32
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N	31 32
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P	32 64
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N	32 64
		S2_MEM_PWR	PP1V35_CAM	31 32
		S2_MEM_PWR	PP0V675_CAM_VREF	31 32
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA	32
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ	32

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SMC SMBus Net Properties

NET TYPE

ELECTRICAL\_CONSTRAINT\_SET

PHYSICAL

SPACING

SMBUS\_SMC\_0\_S0\_SCL

SMB\_45S\_R\_50S

SMB

SMBUS\_SMC\_0\_S0\_SCL

37

40

60

SMBUS\_SMC\_0\_S0\_SDA

SMB\_45S\_R\_50S

SMB

SMBUS\_SMC\_0\_S0\_SDA

37

40

60

SMBUS\_SMC\_1\_S0\_SCL

SMB\_45S\_R\_50S

SMB

SMBUS\_SMC\_1\_S0\_SCL

14

32

37

40

43

44

64

69

SMBUS\_SMC\_1\_S0\_SDA

SMB\_45S\_R\_50S

SMB

SMBUS\_SMC\_1\_S0\_SDA

14

32

37

40

43

44

64

69

SMBUS\_SMC\_2\_S3\_SCL

SMB\_45S\_R\_50S

SMB

SMBUS\_SMC\_2\_S3\_SCL

37

40

61

65

SMBUS\_SMC\_2\_S3\_SDA

SMB\_45S\_R\_50S

SMB

SMBUS\_SMC\_2\_S3\_SDA

37

40

61

65

SMBUS\_SMC\_3\_SCL

SMB\_45S\_R\_50S

SMB

SMBUS\_SMC\_3\_SCL

36

37

40

44

64

SMBUS\_SMC\_3\_SDA

SMB\_45S\_R\_50S

SMB

SMBUS\_SMC\_3\_SDA

36

37

40

44

64

SMBUS\_SMC\_5\_G3\_SCL

SMB\_45S\_R\_50S

SMB

SMBUS\_SMC\_5\_G3\_SCL

37

40

48

50

64

SMBUS\_SMC\_5\_G3\_SDA

SMB\_45S\_R\_50S

SMB

SMBUS\_SMC\_5\_G3\_SDA

37

40

48

50

64

SMBus Charger Net Properties

NET TYPE

ELECTRICAL\_CONSTRAINT\_SET

PHYSICAL

SPACING

SENSE\_DIFFPAIR

2TO1\_DIFFPAIR

CHGR\_CSI\_P

50

SENSE\_DIFFPAIR

2TO1\_DIFFPAIR

CHGR\_CSI\_N

50

2TO1\_DIFFPAIR

CHGR\_CSI\_R\_P

50

2TO1\_DIFFPAIR

CHGR\_CSI\_R\_N

50

SENSE\_DIFFPAIR

2TO1\_DIFFPAIR

CHGR\_CSO\_P

50

SENSE\_DIFFPAIR

2TO1\_DIFFPAIR

CHGR\_CSO\_N

50

2TO1\_DIFFPAIR

CHGR\_CSO\_R\_P

43

50

2TO1\_DIFFPAIR

CHGR\_CSO\_R\_N

43

50

8

7

6

5

4

3

2

1

8

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