

Orta Block Diagram

Project code: 91.4U101.001
PCB P/N : 48.4U101.0SA
REVISION : 06245-SA

PCB Layer Stackup

L1: Signal 1
L2: VCC
L3: Inner Signal 2
L4: Inner Signal 3
L5: GND
L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

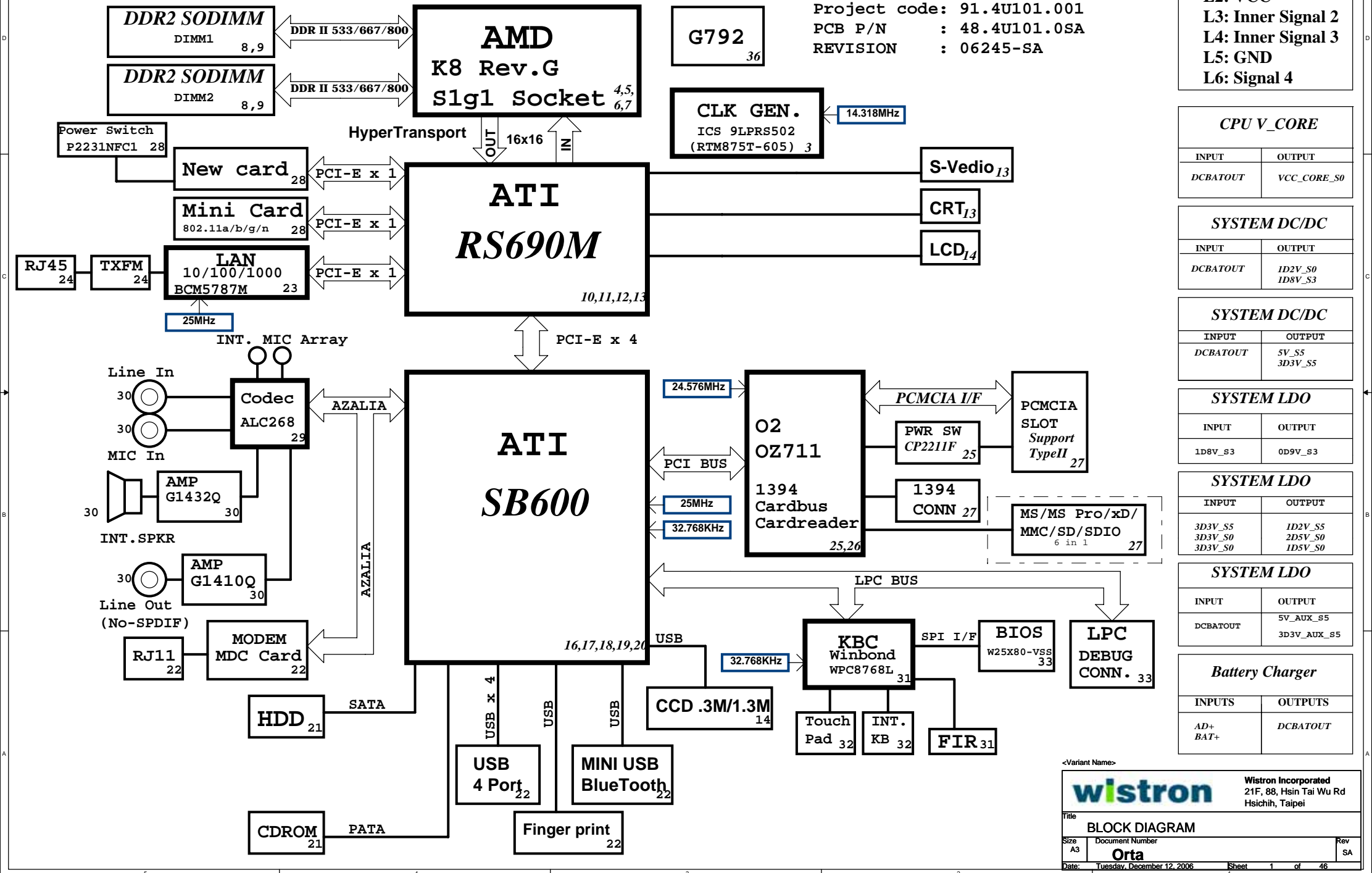
Title
BLOCK DIAGRAM

Size A3 Document Number

Date: Tuesday, December 12, 2006

Sheet 1 of 46

Rev SA



SA: 07/31/06 Start

- SB change
power team
- 1.change L7, L9 to 68.1R510.10D
 - 2.changge U12 to 84.04706.037
 - 3.change R66 to 10K ohm

<Core Design>

緯創資通

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Title

CHANGE HISTORY

Size

A3

Document Number

Orta

Date:

Tuesday, December 12, 2006

Sheet

2

of

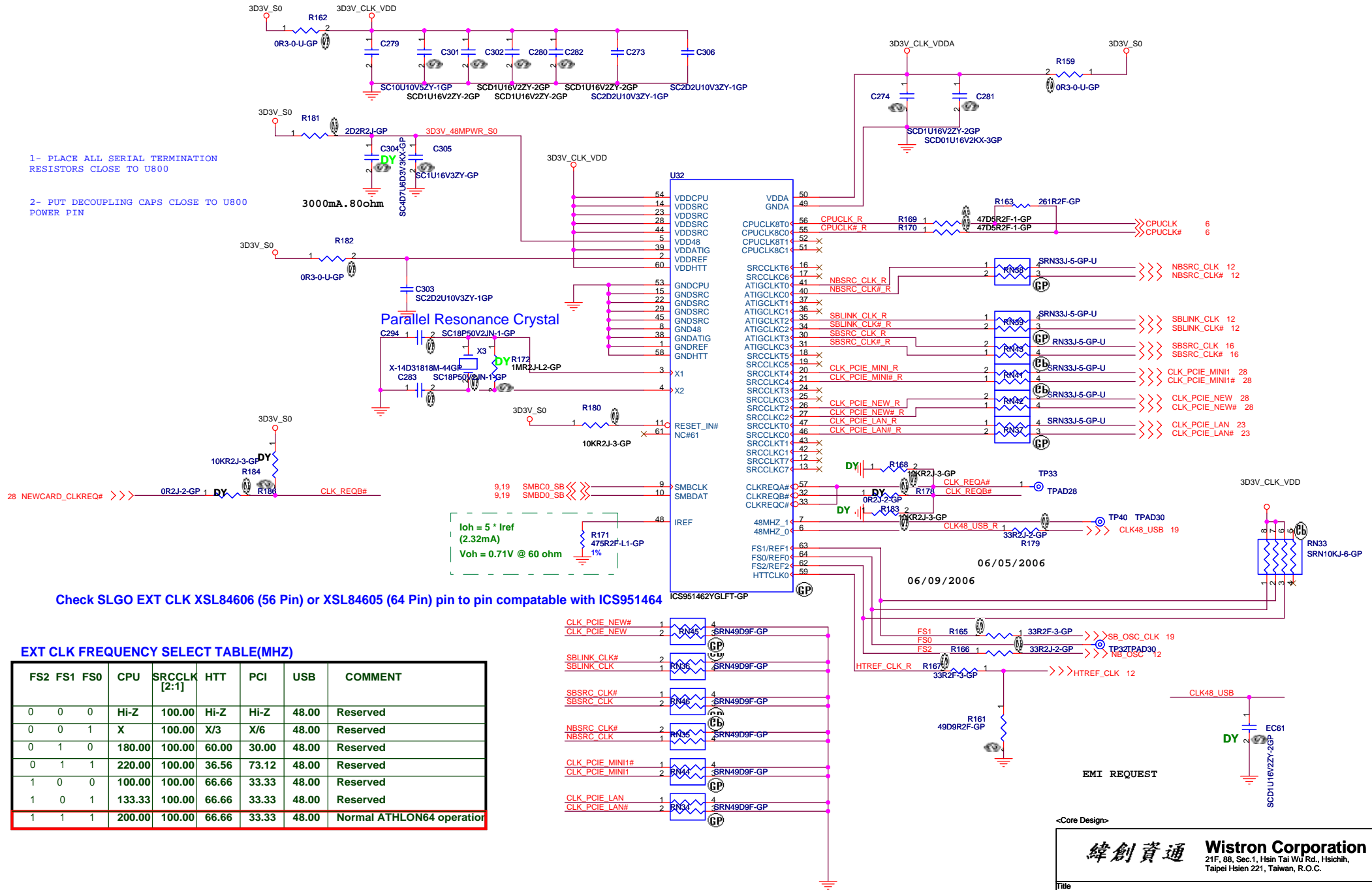
46

Rev

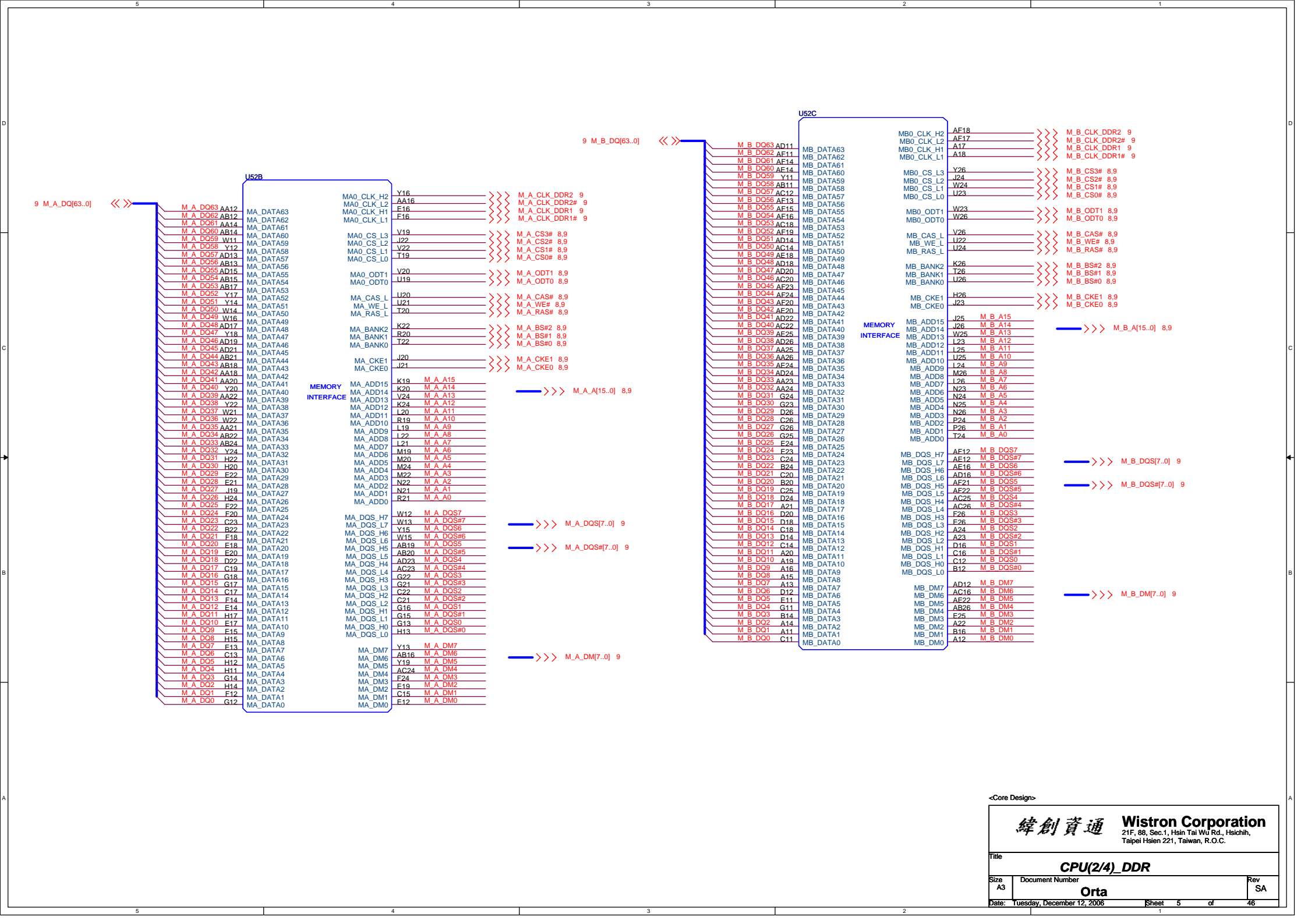
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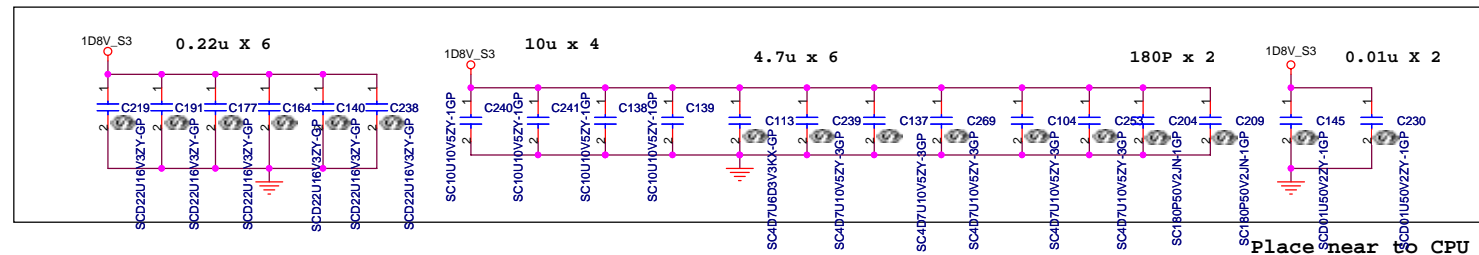
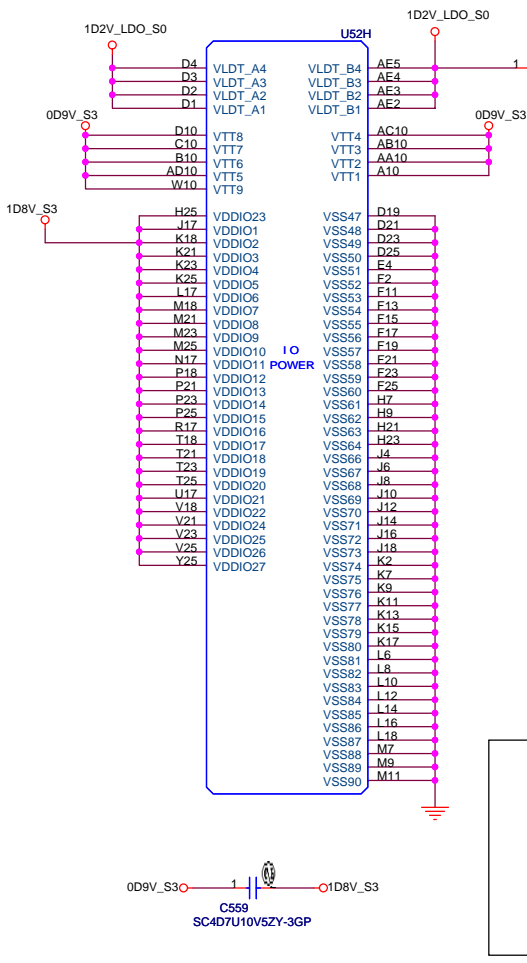
1- PLACE ALL SERIAL TERMINATION
RESISTORS CLOSE TO U800

2- PUT DECOUPLING CAPS CLOSE TO U800
POWER PIN

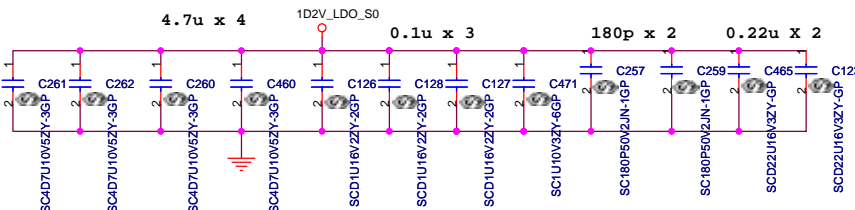
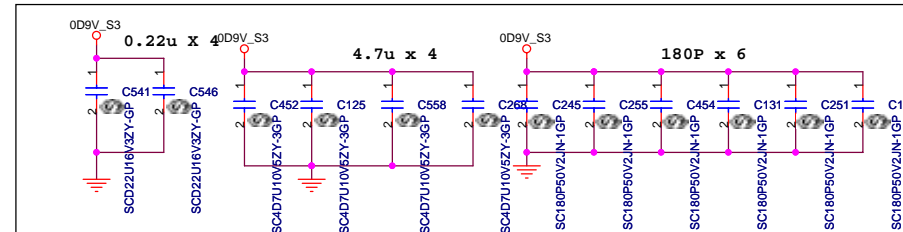
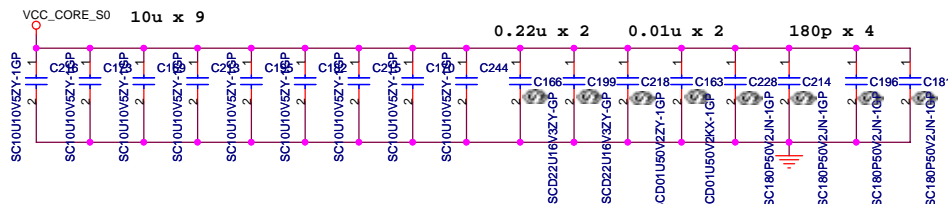








LAYOUT: Place on backside of processor.



<Core Design>

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Title: **CPU(4/4)_Power**

Size A3 Document Number: **Orta** Rev SA

Date: Tuesday, December 12, 2006 Sheet 7 of 46

PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

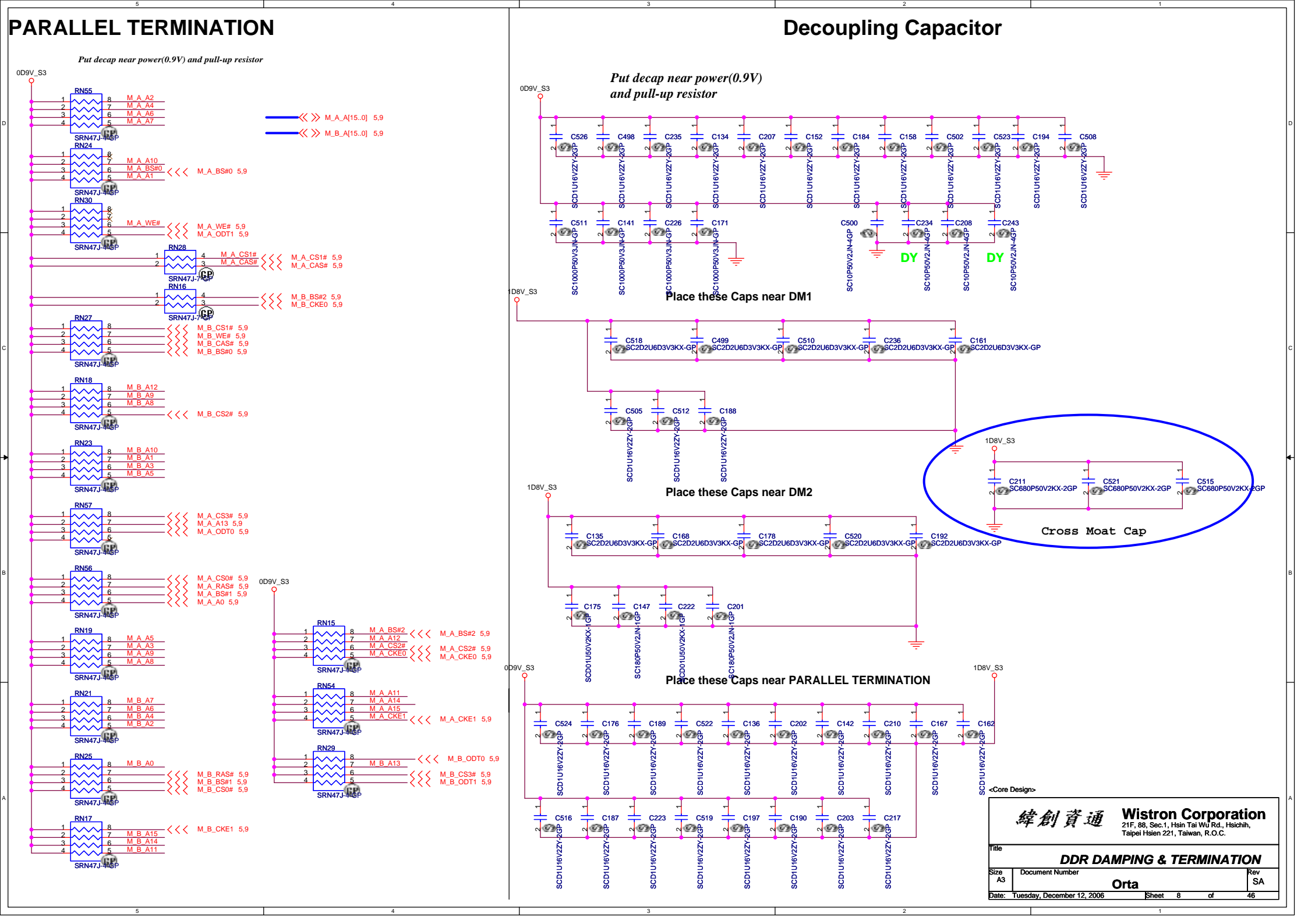
Place these Caps near DM1

Place these Caps near DM2

Place these Caps near PARALLEL TERMINATION

Cross Moat Cap

Title	
DDR DAMPING & TERMINATION	
Size A3	Document Number
Orta	
Date: Tuesday, December 12, 2006	Sheet 8 of 46

[illegible]

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Place these Caps near DM2

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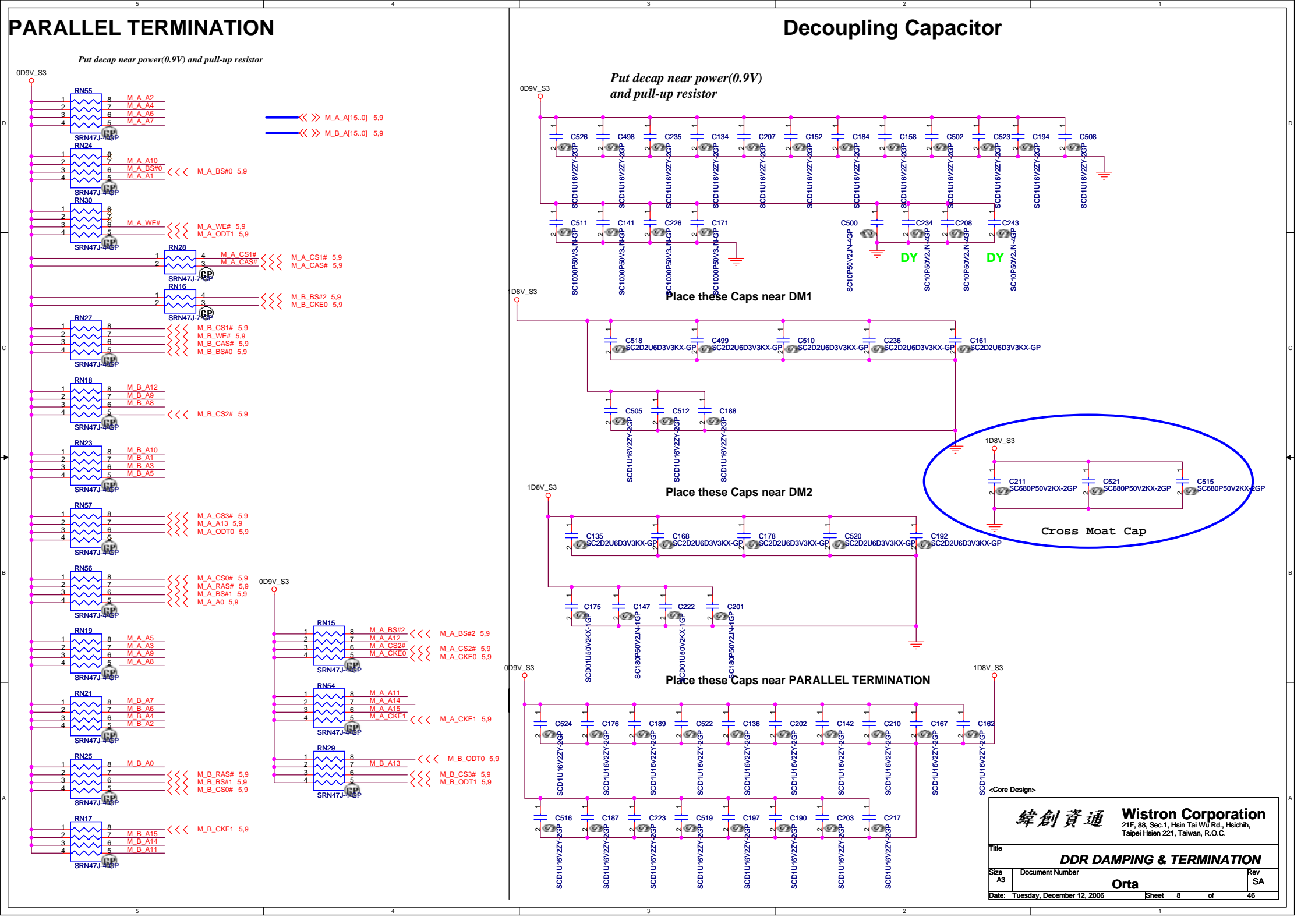
Cross Moat Cap

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DDR DAMPING & TERMINATION

Orta

Date: Tuesday, December 12, 2006 Sheet 8 of 46

[illegible][illegible][illegible]

Decoupling Capacitor

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Place these Caps near DM2

Place these Caps near PARALLEL TERMINATION

Cross Moat Cap

Parallel Termination

Decoupling Capacitor

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DDR DAMPING & TERMINATION			
Title			
Size	Document Number	Rev	
A3		Orta	SA
Date:	Tuesday, December 12, 2006	Sheet	8 of 46

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Size	Document Number	Rev	
A3	Orta	SA	
Date:	Tuesday, December 12, 2006	Sheet	8 of 46

NORMAL TYPE

NORMAL TYPE

DDR_VREF

62.10017.A61

High 9.2mm

Hi 9.2 mm High 5.2mm
Main Source: 62.10017.A61

LAYOUT: Locate close to DIMM

<Core Design>

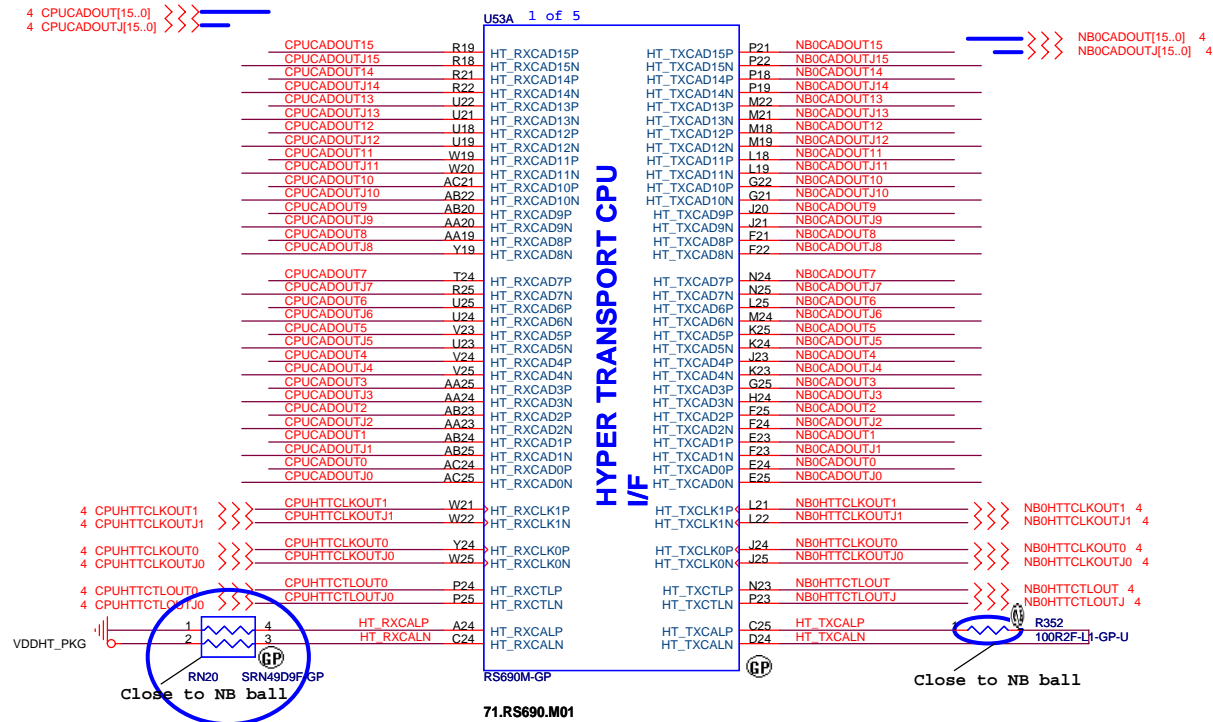
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Size		SA	
Custom		Orta	
Date: Tuesday, December 12, 2006		Sheet 9 of 46	

DDR SO-DIMM SKT

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CLAW HAMMER TO NB

NB TO CLAW HAMMER



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

NB-RS690M HT

Size
A3

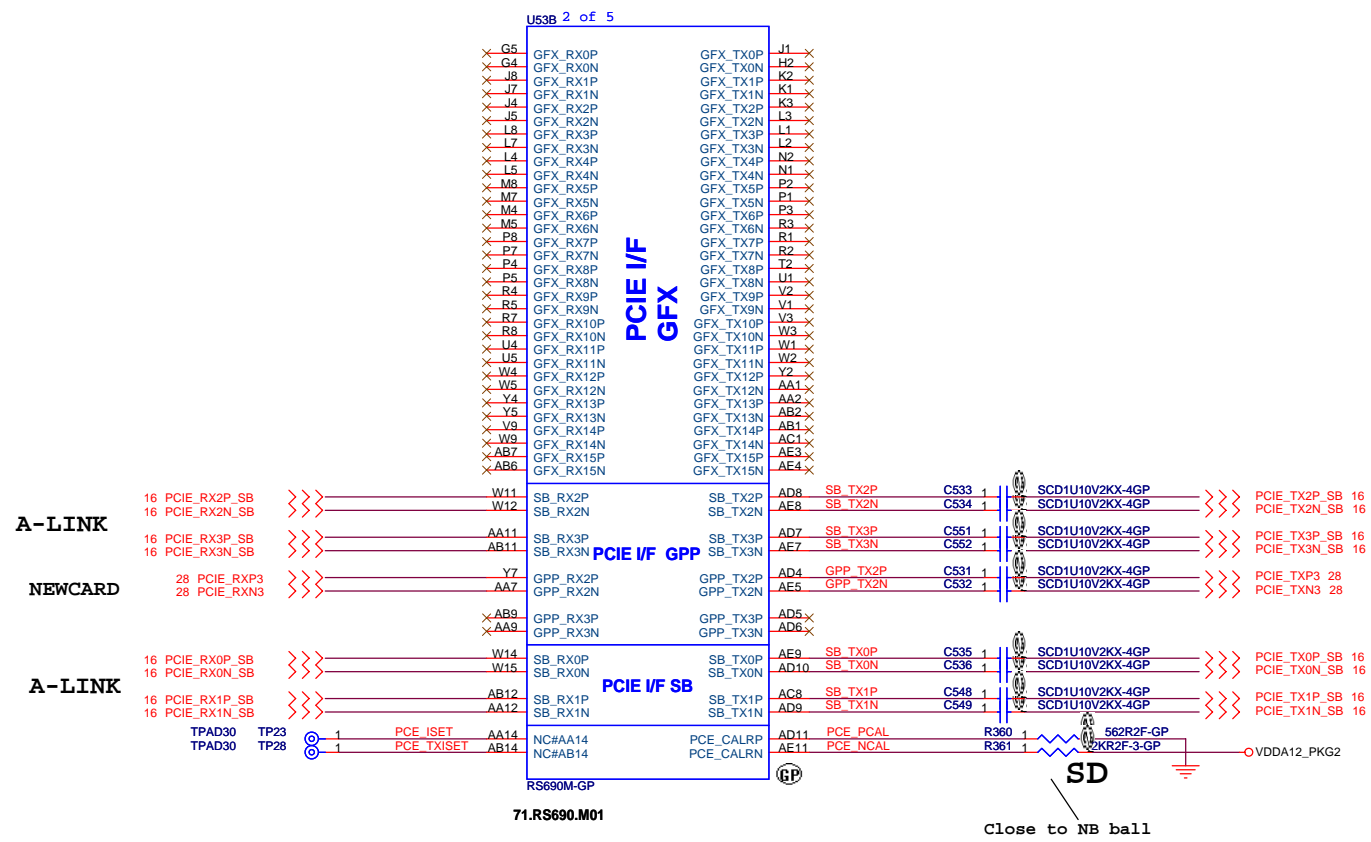
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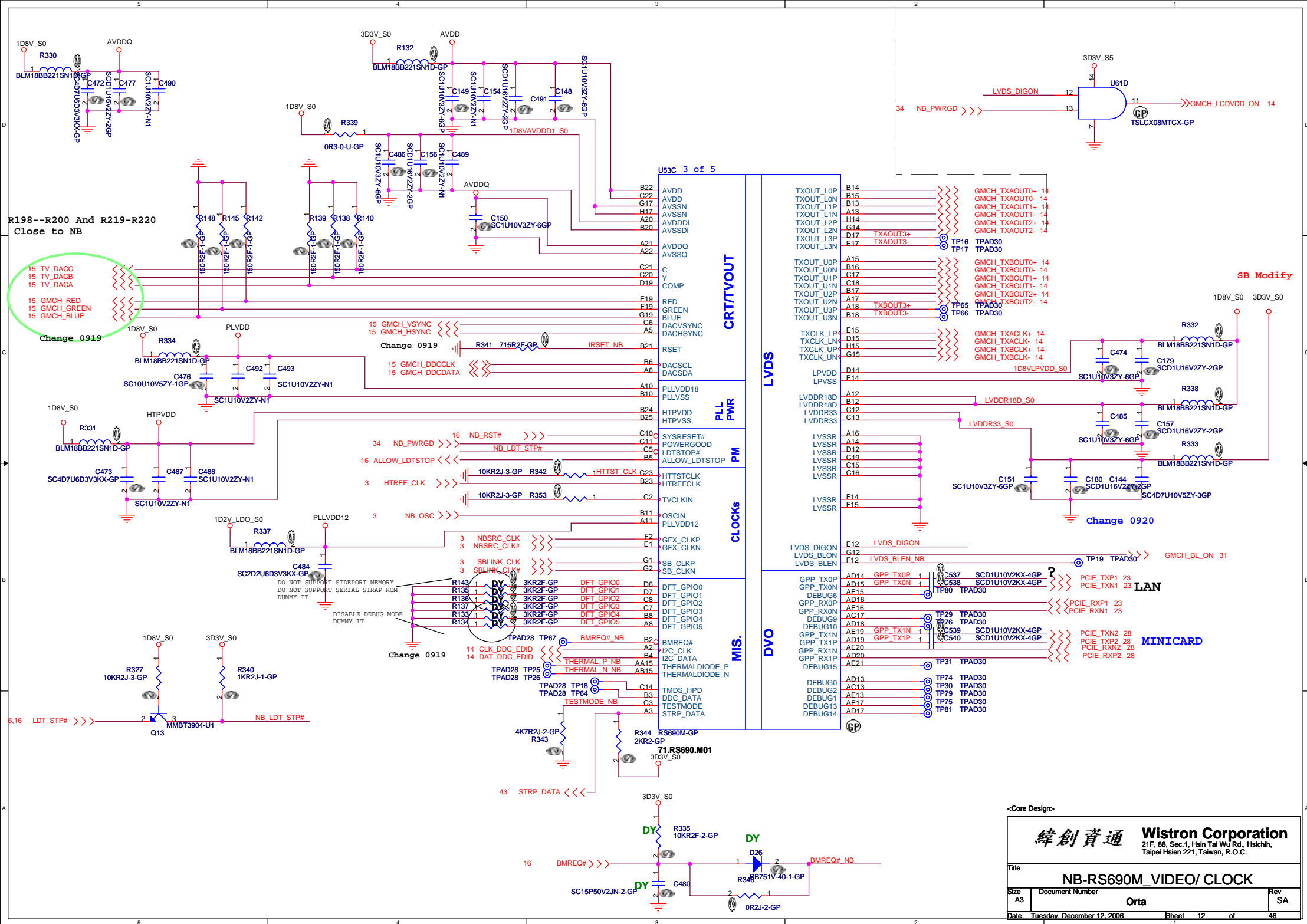
Rev
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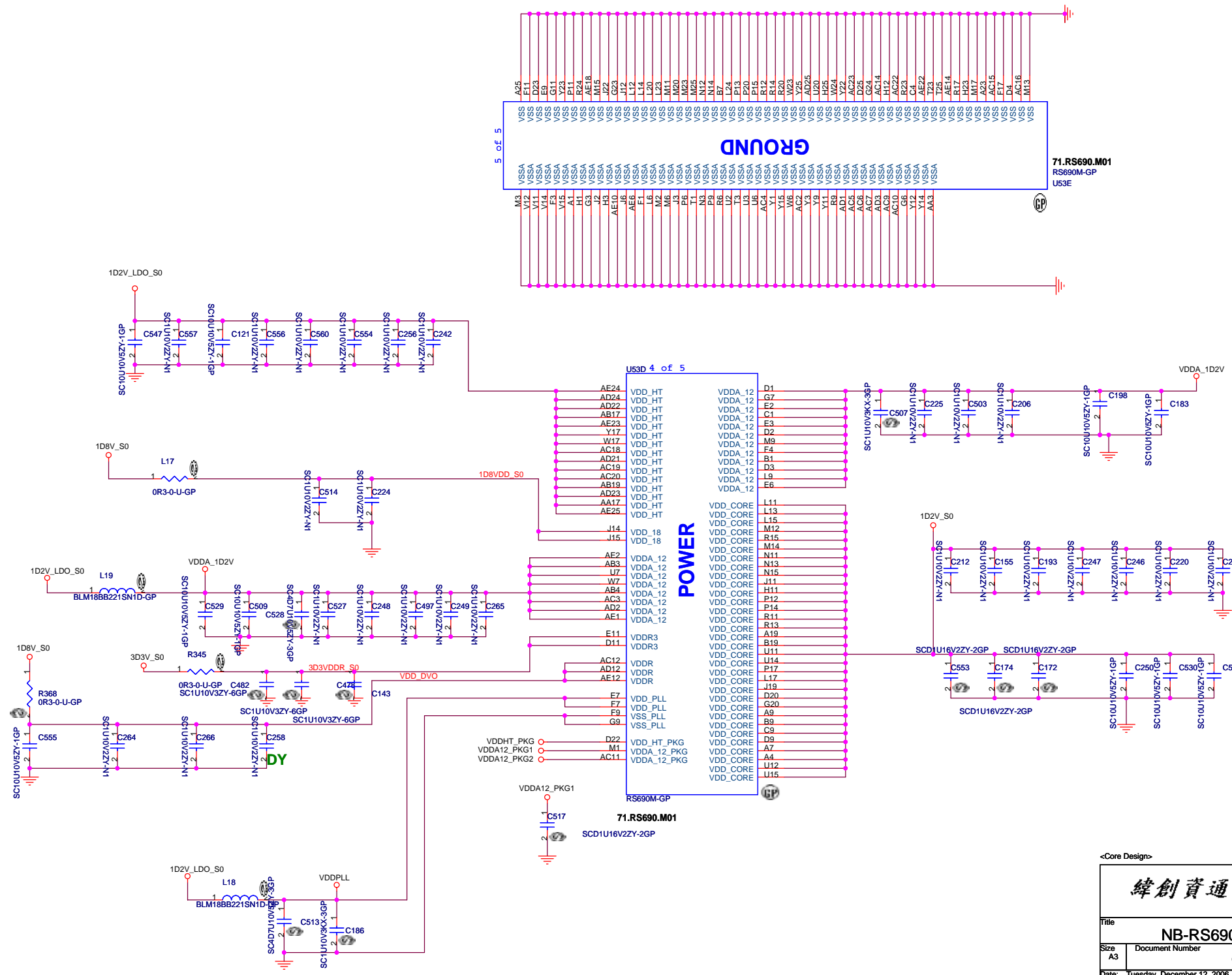
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Sheet 10 of 46



A-LINK
CLOSE TO NB





5 of 5

U53D 4 of 5

71.RS690.M01

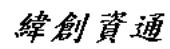
SCD1U16V2ZY-2GP

GROUND

POWER

71.RS690.M01
RS690M-GP
U53E

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title
NB-RS690M_POWER

Size
A3

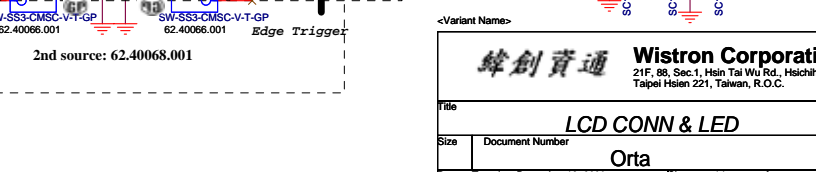
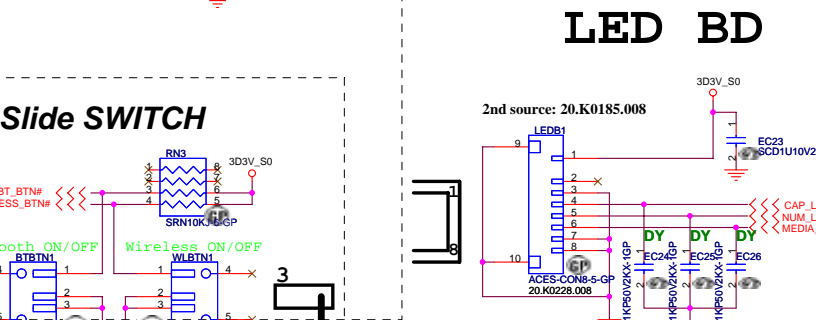
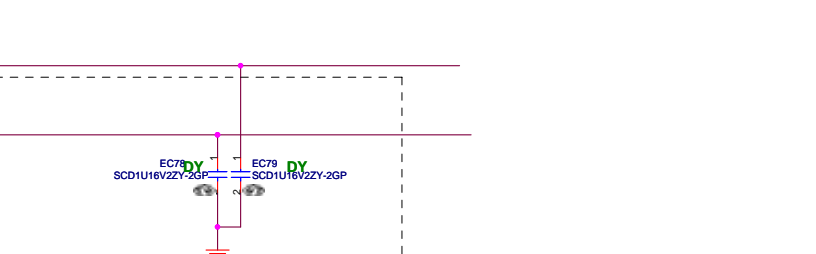
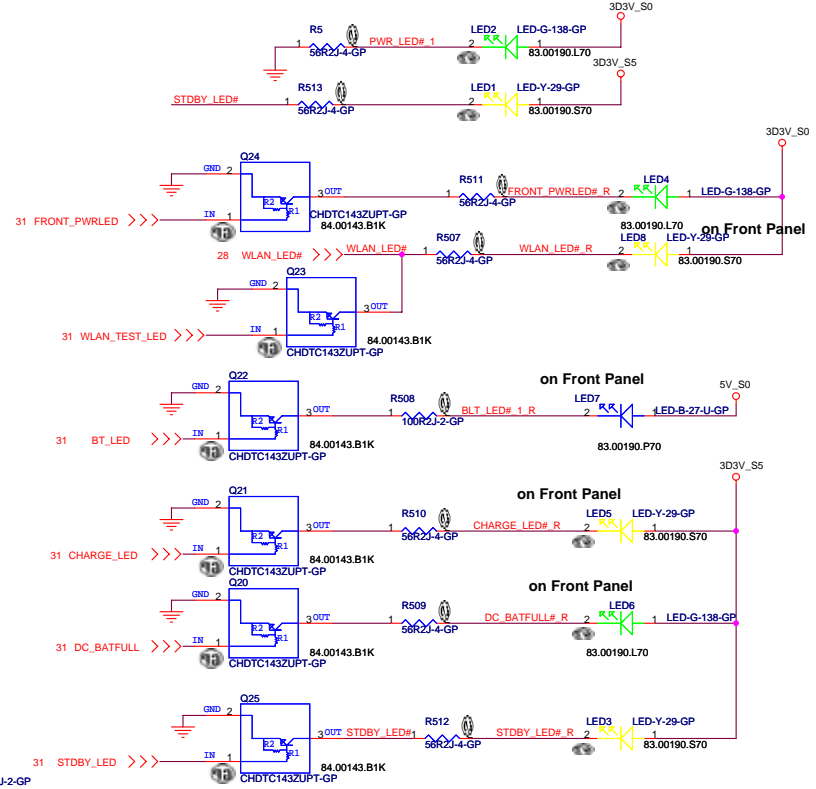
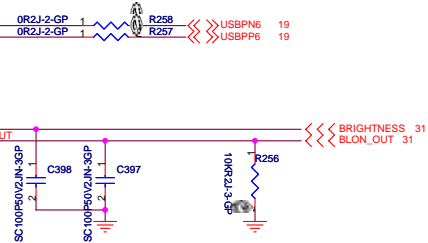
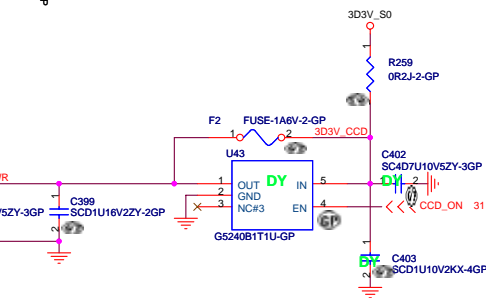
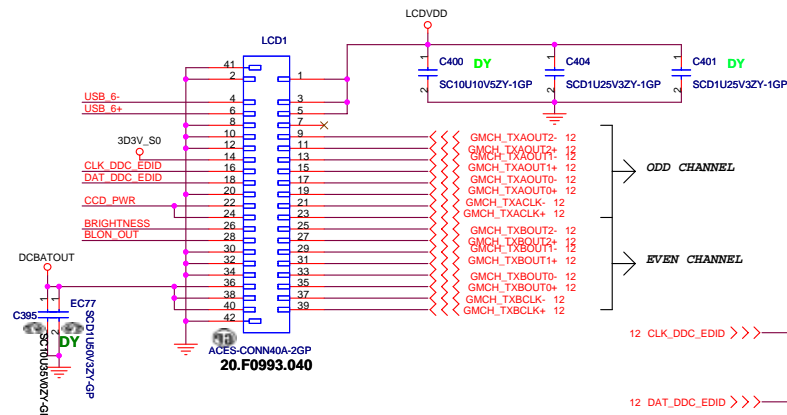
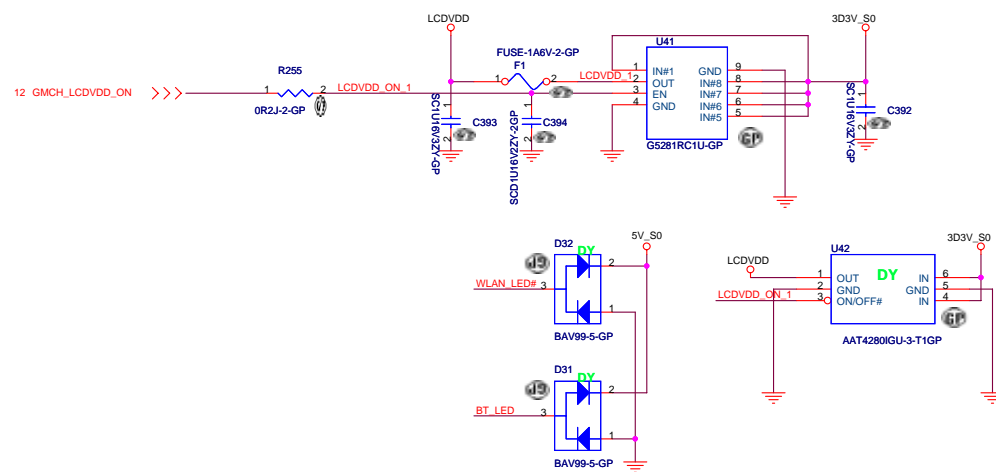
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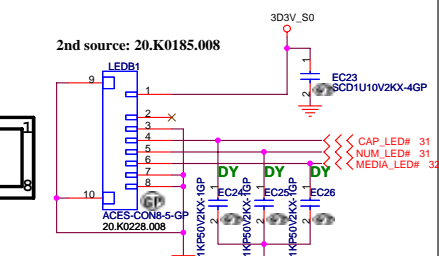
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Sheet 13 of 46

LCD/INVERTER CONN

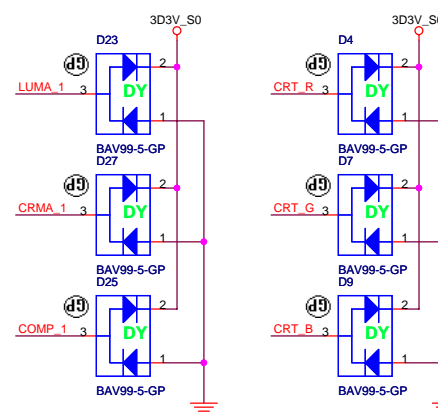
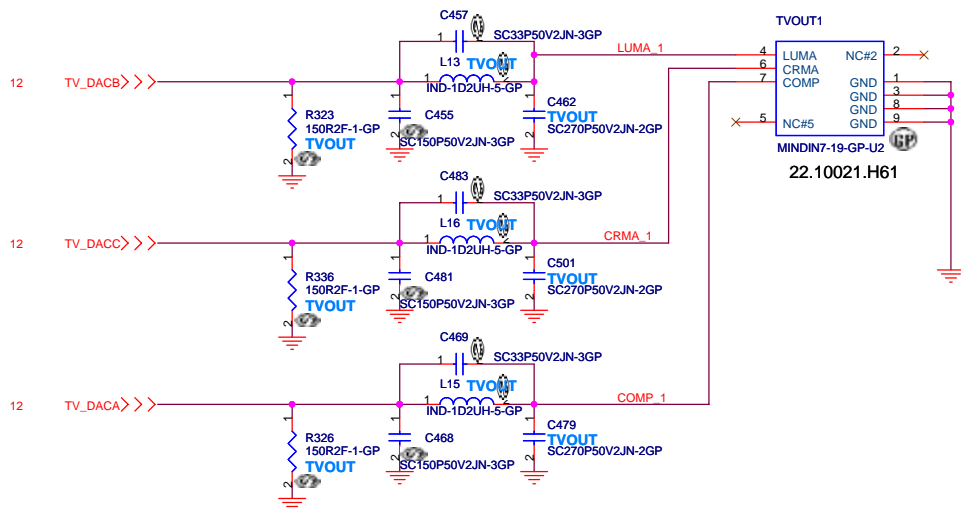
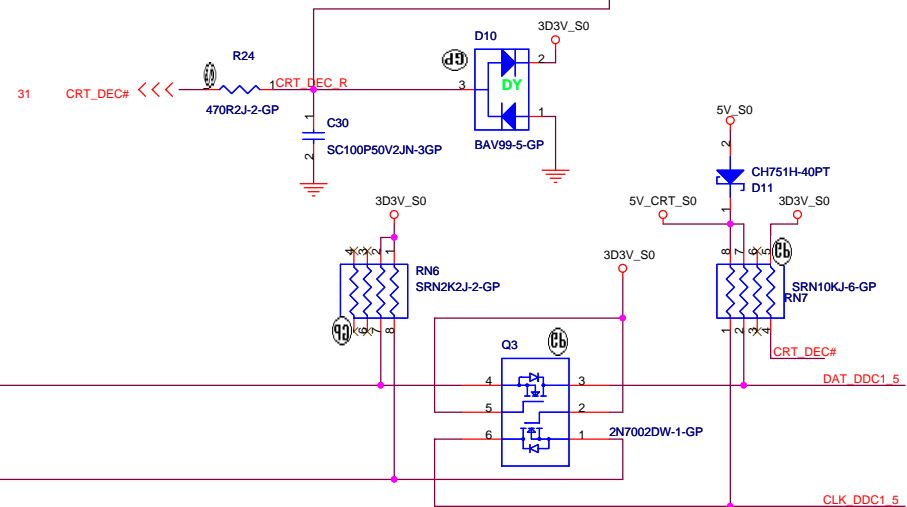
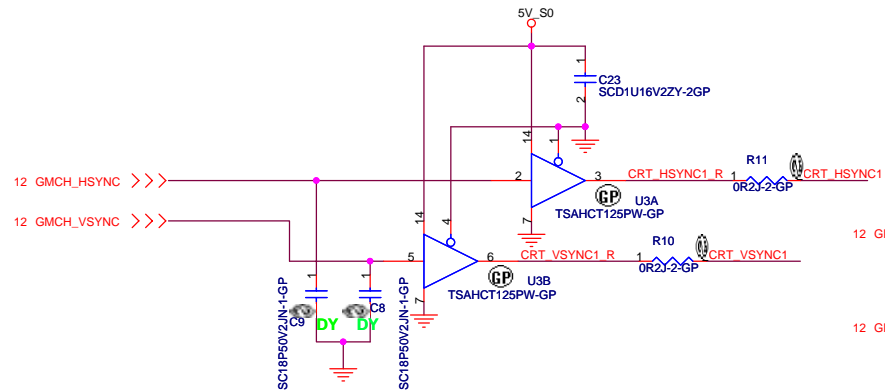
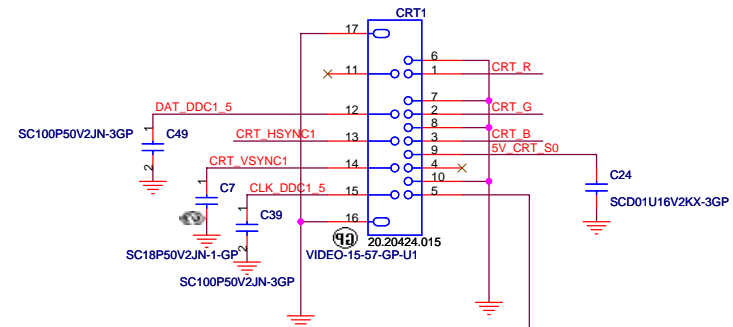
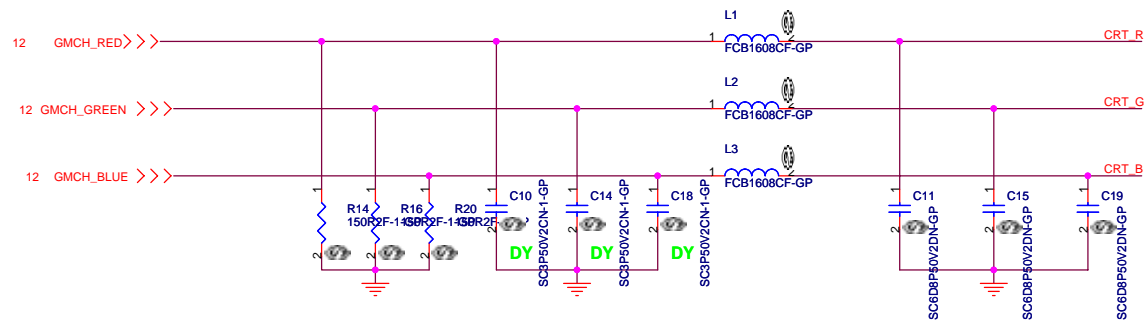


LED BD

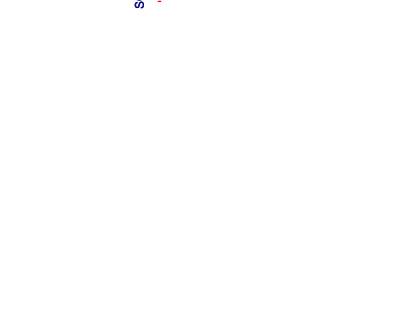
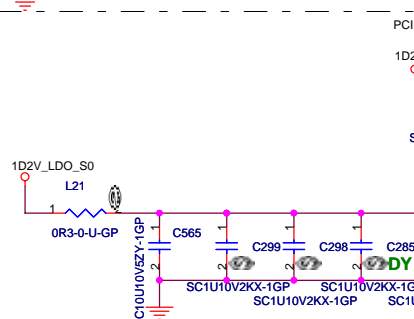
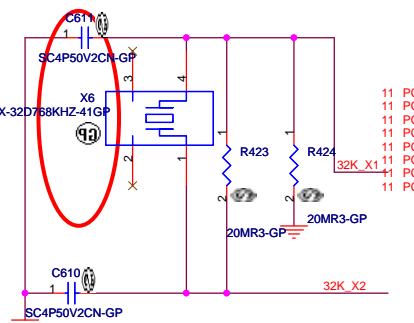


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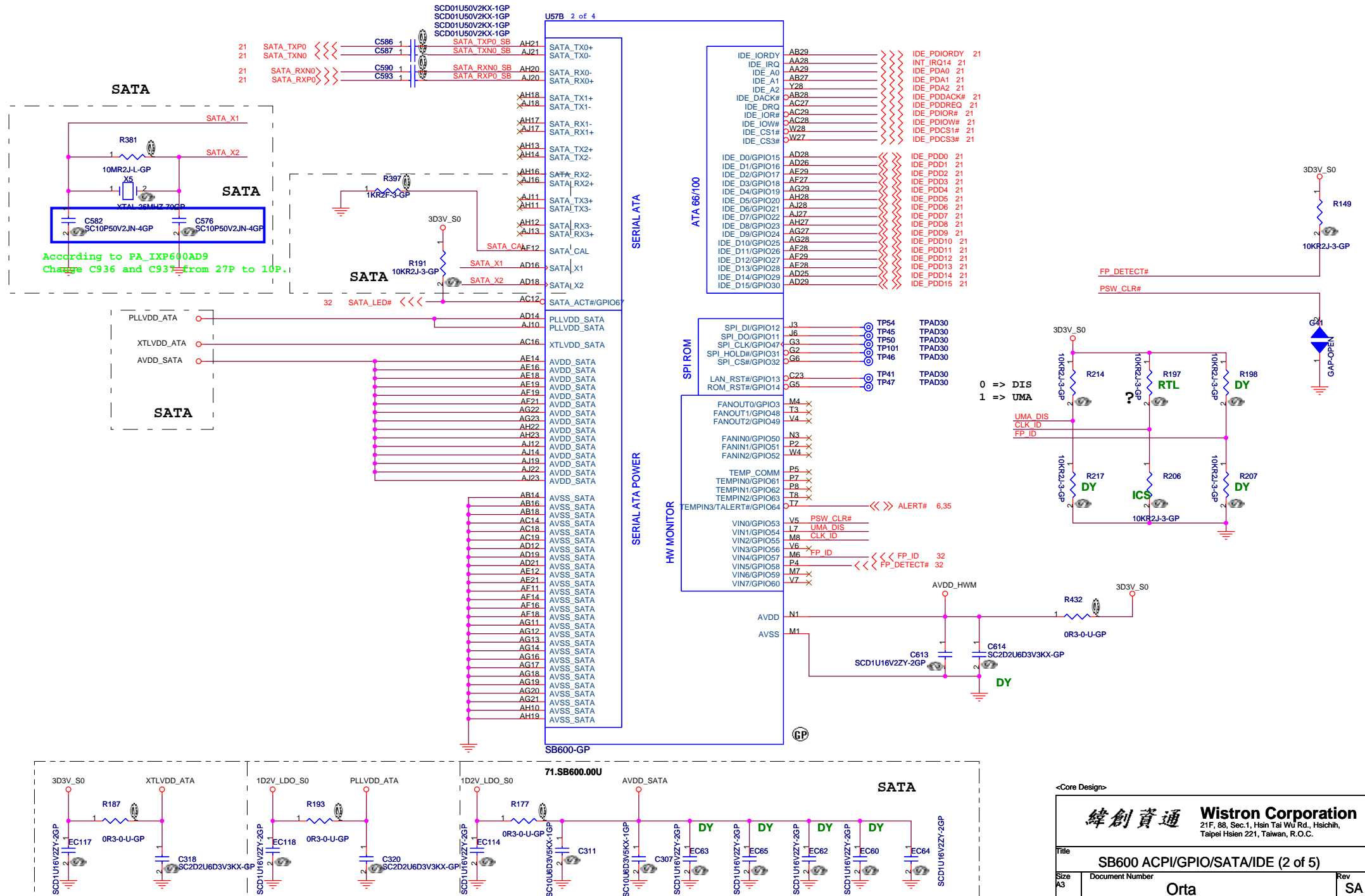
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Date: Tuesday, December 12, 2006 Sheet 14 of 46

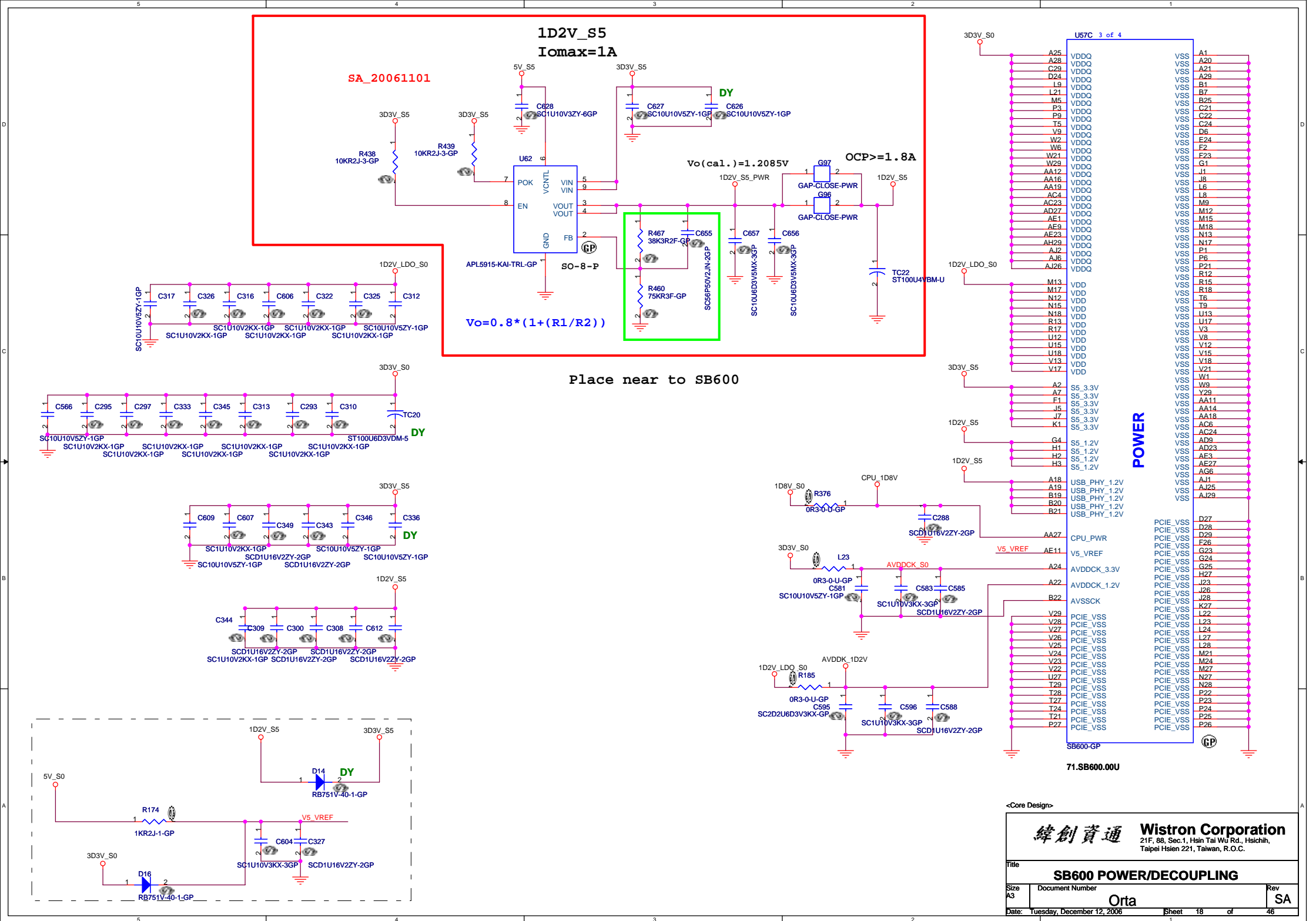


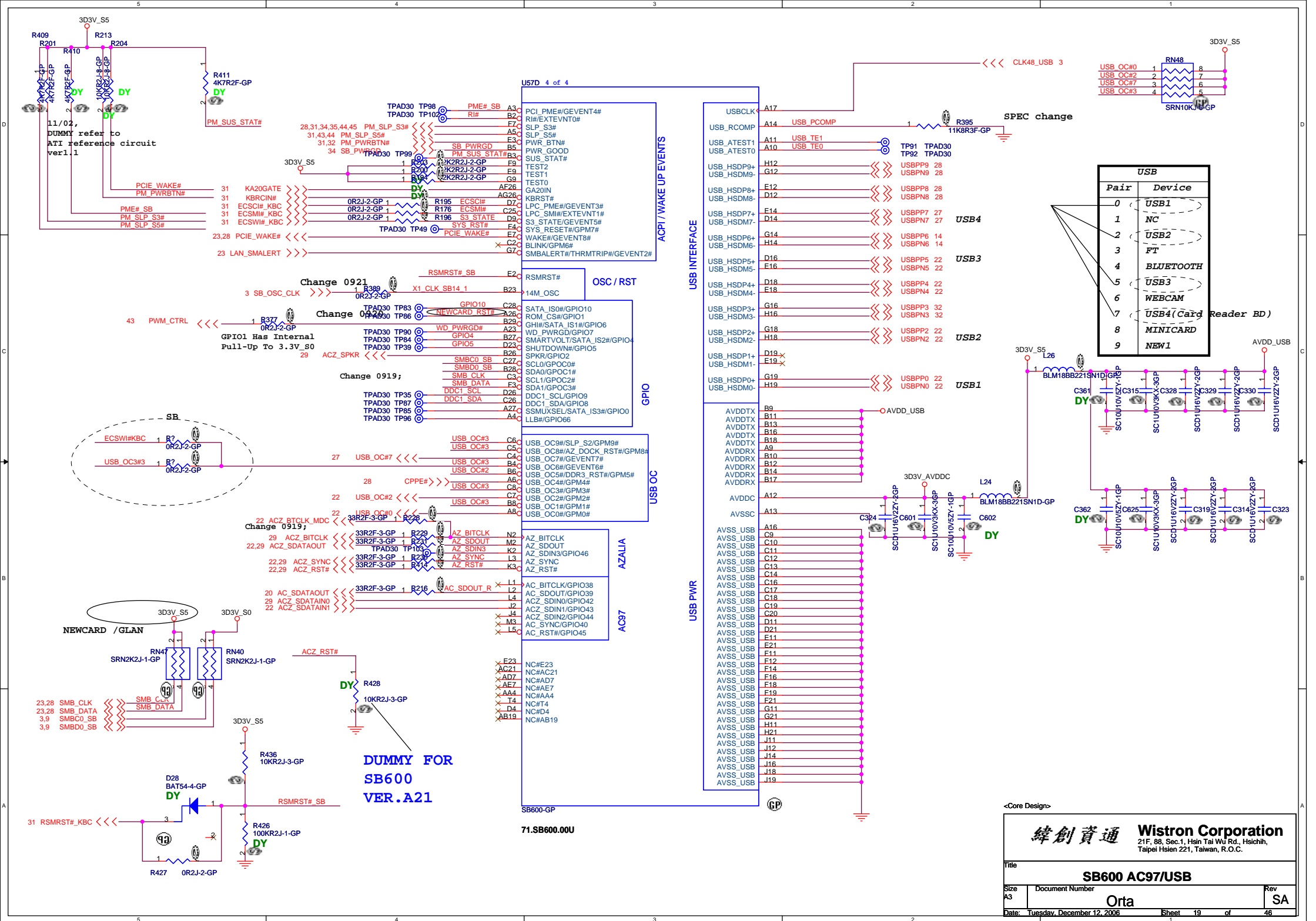
Place these components close to U13
and use ground guard for 32K_X1 and 32K_X2.



PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB460

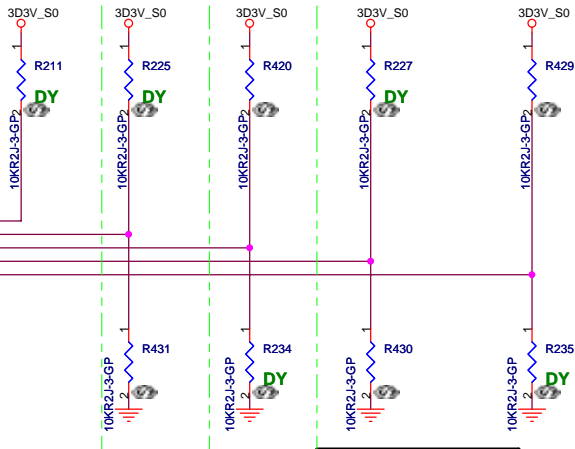






PCI_CLK4
PCI_CLK6
PCI_CLK0
PCI_CLK1

19 AC_SDATAOUT
16,31 PCLK_KBC
16 CLK33_LPCROM
16 PCI_CLK0
16,25 PCLK_PCM

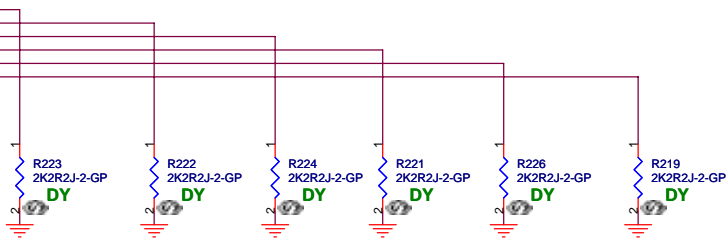


REQUIRED SYSTEM STRAPS

SB600					
	AC_SDOUT	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	DEFAULT
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4		

SB600 HAS 15K INTERNAL PU FOR PCI_AD[23..28]

16,25 PCI_AD28
16,25 PCI_AD27
16,25 PCI_AD26
16,25 PCI_AD25
16,25 PCI_AD24
16,25 PCI_AD23



DEBUG STRAPS

	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH	RESERVED	RESERVED	RESERVED	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOT FAIL TIMER DISABLE DEFAULT
STRAP LOW				USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOT FAIL TIMER ENABLE

<Core Design>

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Title

SB600 STRAPPING PIN

Size

Document Number

Rev

A3

Orta

SA

Date:

Tuesday, December 12, 2006

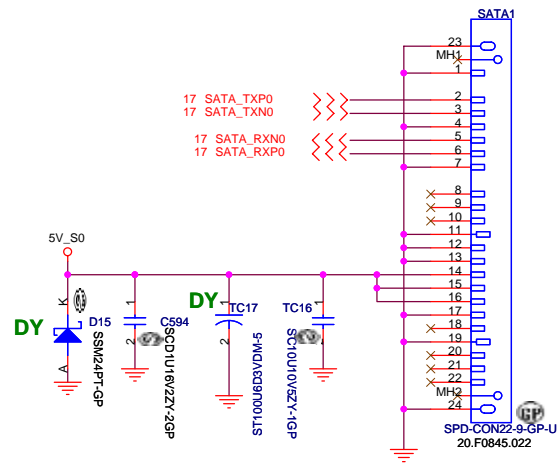
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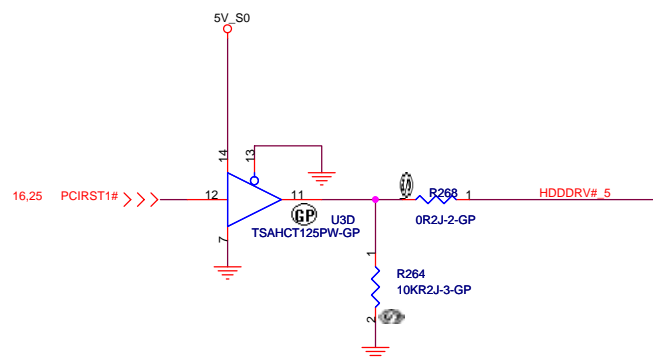
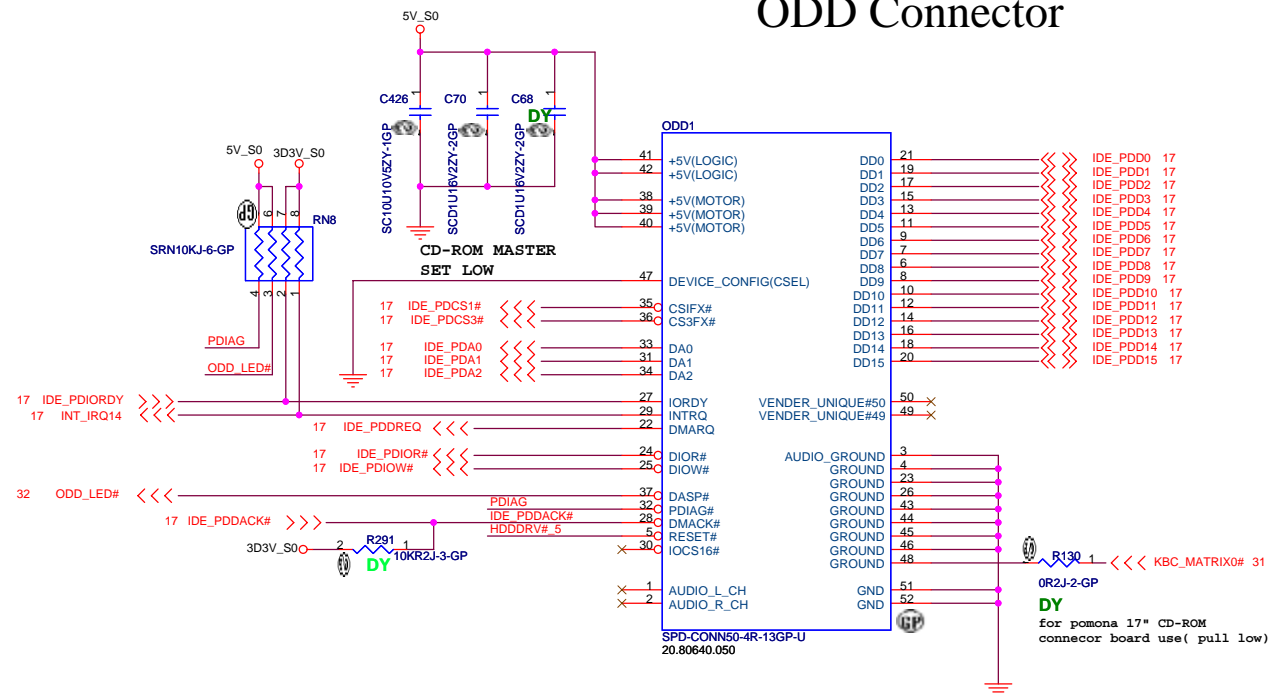
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46

SATA HD Connector

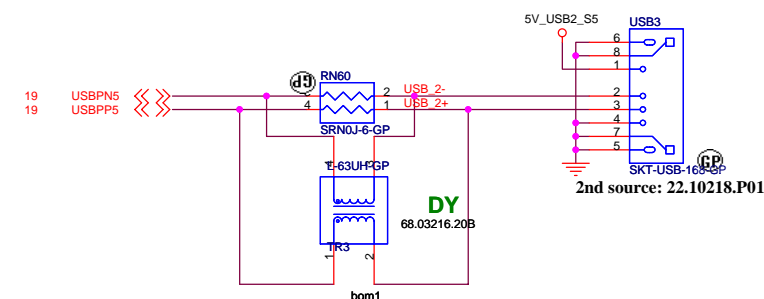


ODD Connector



bom1

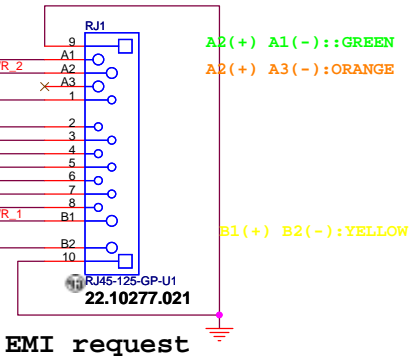
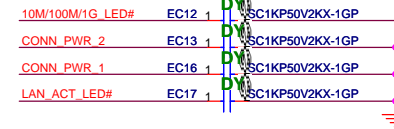
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Size	
Document Number	
Date: Tuesday, December 12, 2006	
Sheet 21 of 46	
Rev SA	



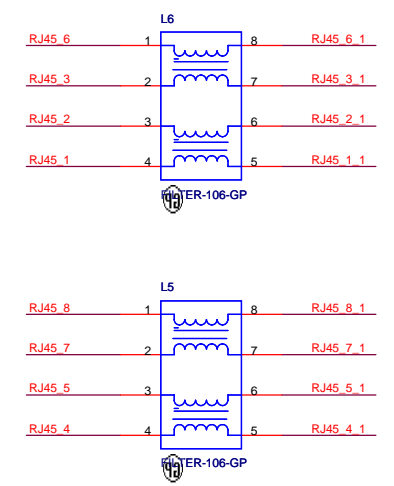
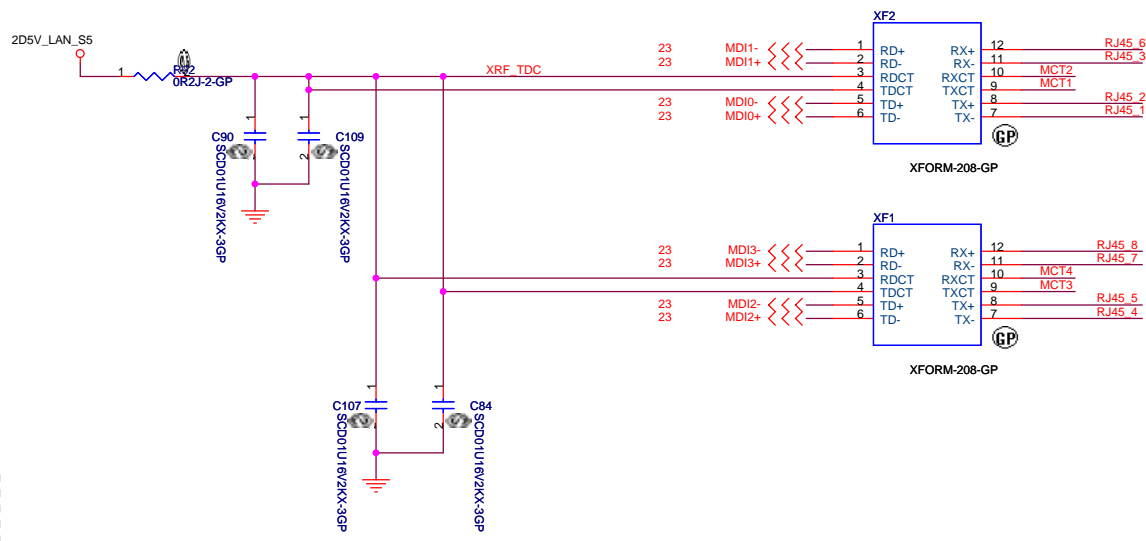
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USB / MDC / BLUETOOTH			
Size	Document Number		Rev
	Orta		SA
Date:	Tuesday, December 12, 2006	Sheet 22 of	46



LAN Connector



GIGA Lan Transformer

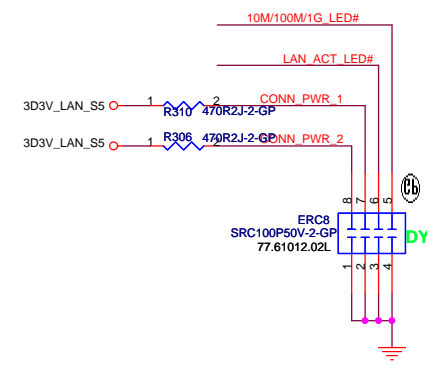
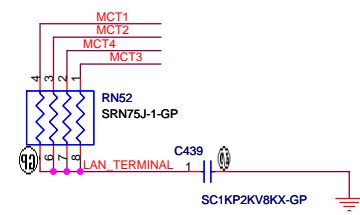


- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
 W/S : 10/100 @ Surface layers
 10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6



<Variant Name>

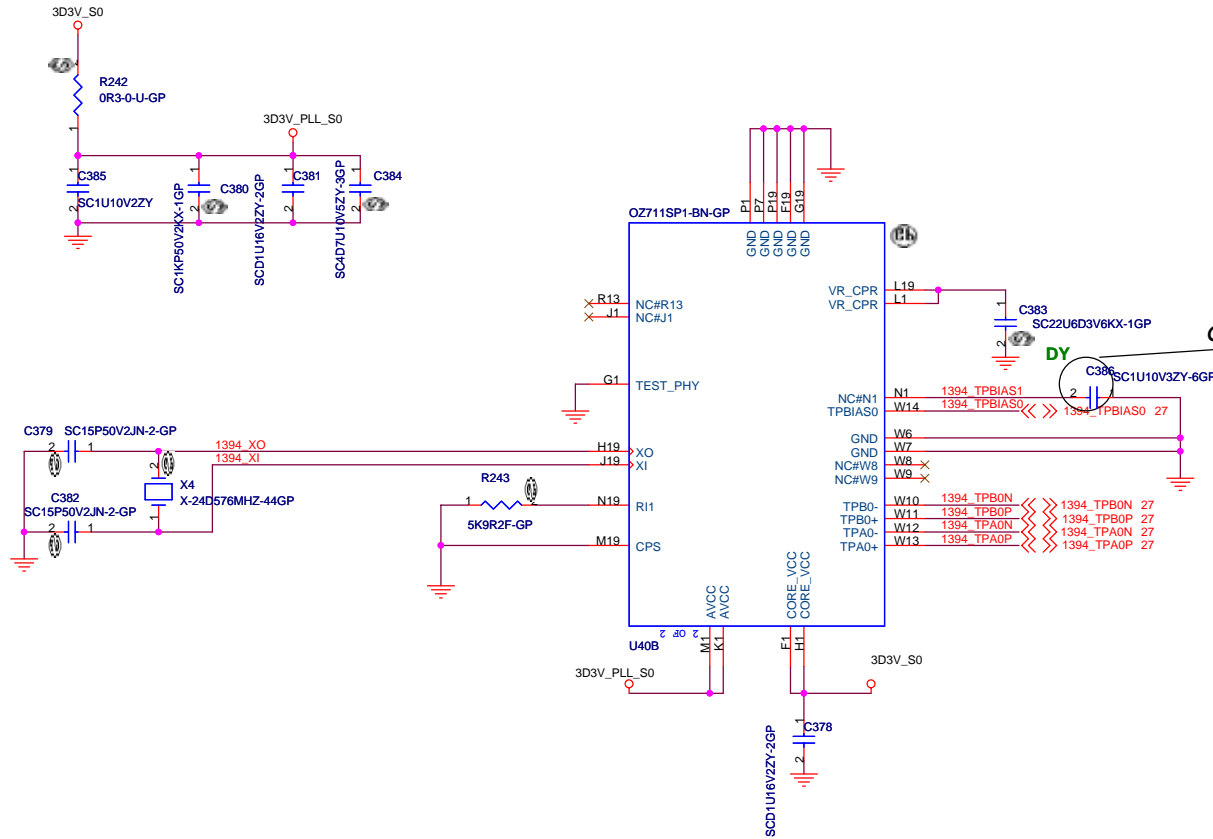
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title
LAN Connector

Size A3 Document Number
Orta

Date: Tuesday, December 12, 2006 Sheet 24 of 46

Rev SA



<Variant Name>

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Title		OZ711SP1 (2 of 2)	
Size	Document Number	Rev	SA
Date: Tuesday, December 12, 2006		Sheet 26 of 46	

PCMCIA Socket

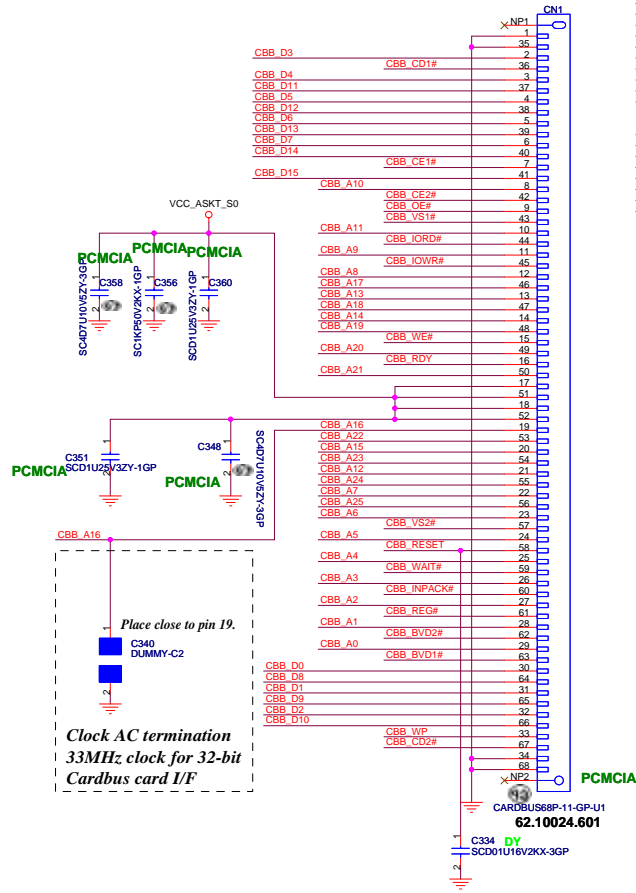
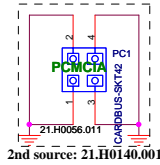
Cardbus I/F

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CBB_A[25..0] << CBB_A[25..0] 25

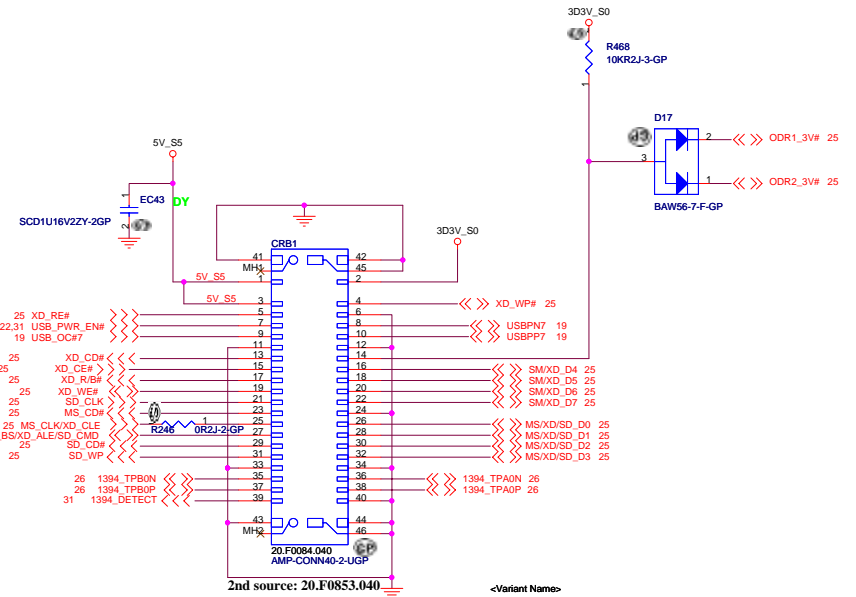
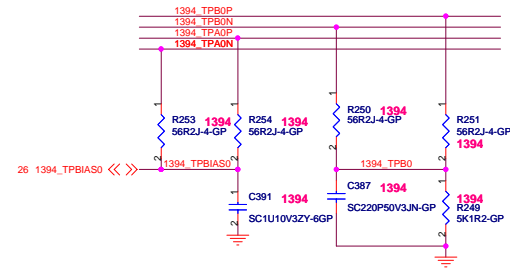
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CBB_OE# 25
CBB_WE# 25
CBB_REG# 25

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CBB_CE2# 25
CBB_BVD1# 25
CBB_BVD2# 25
CBB_CD1# 25
CBB_CD2# 25
CBB_VS1# 25
CBB_VS2# 25

CBB_ROY 25
CBB_WP 25
CBB_RESET 25
CBB_WAIT# 25
CBB_INPACK# 25



CLOSE TO CHIP



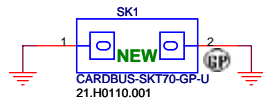
XD
MS / MS PRO
SD / SD IO / MMC

<Variant Name>

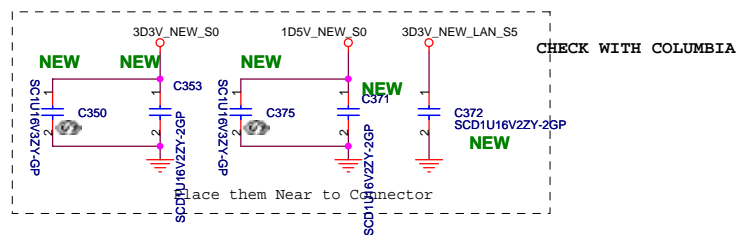
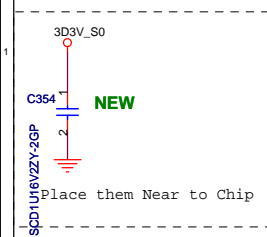
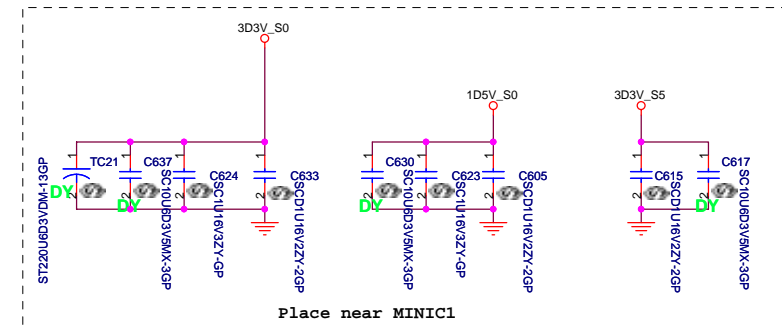
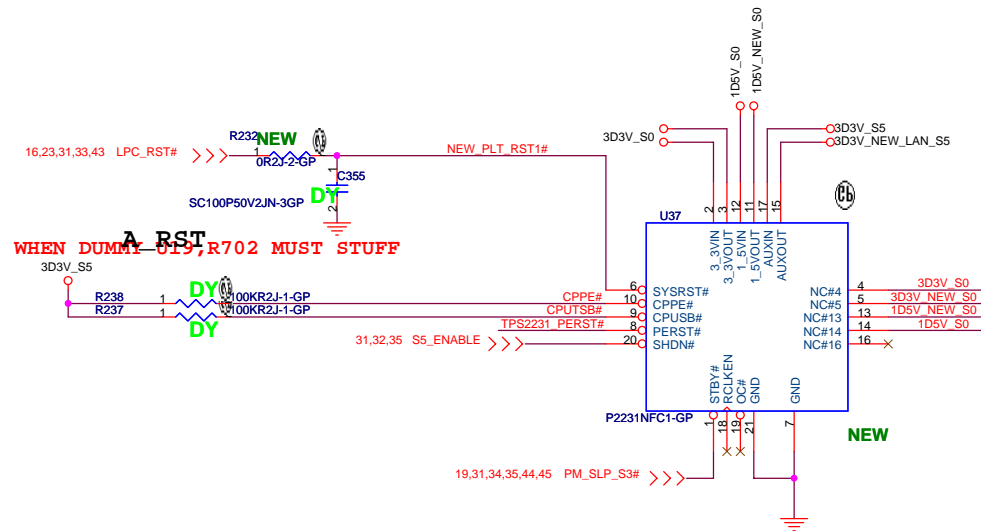
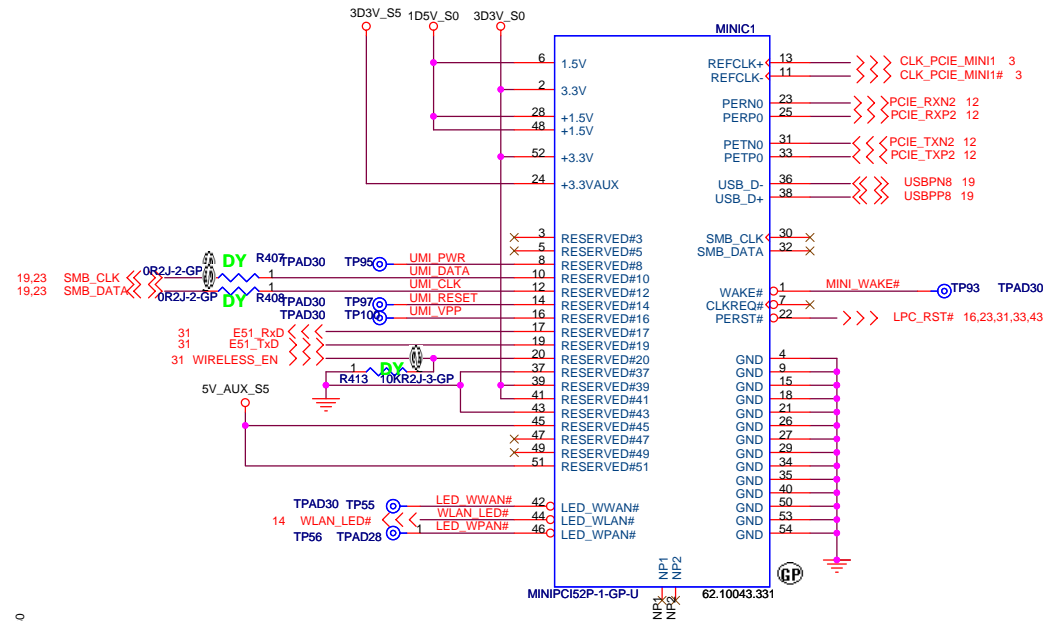
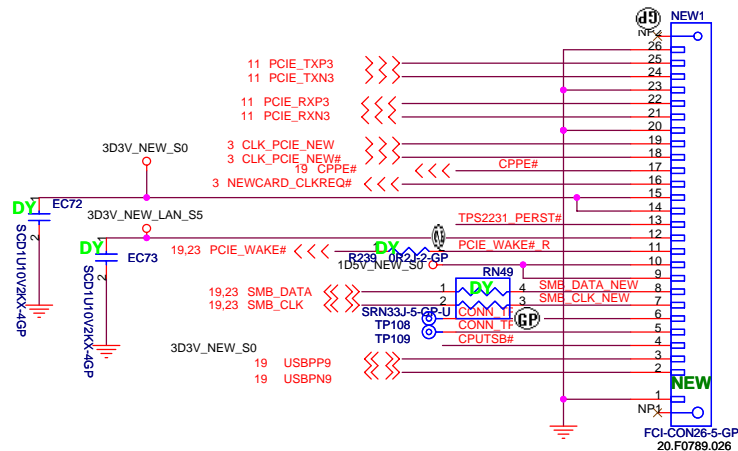
Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsiehshih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
PCMCIA / 1394 / CARD READER		
Size	Document Number	Rev
	Orta	SA
Date: Tuesday, December 12, 2006		
Sheet 27 of 46		

Mini Card Connector

NEWCARD Connector



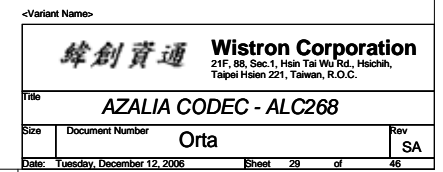
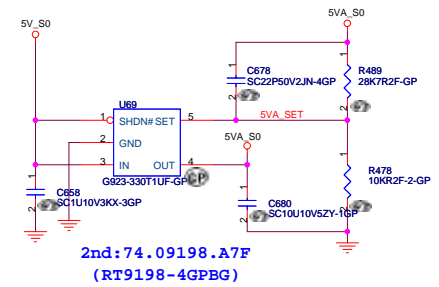
Reserve the symbol
for bottom side
connector



born1

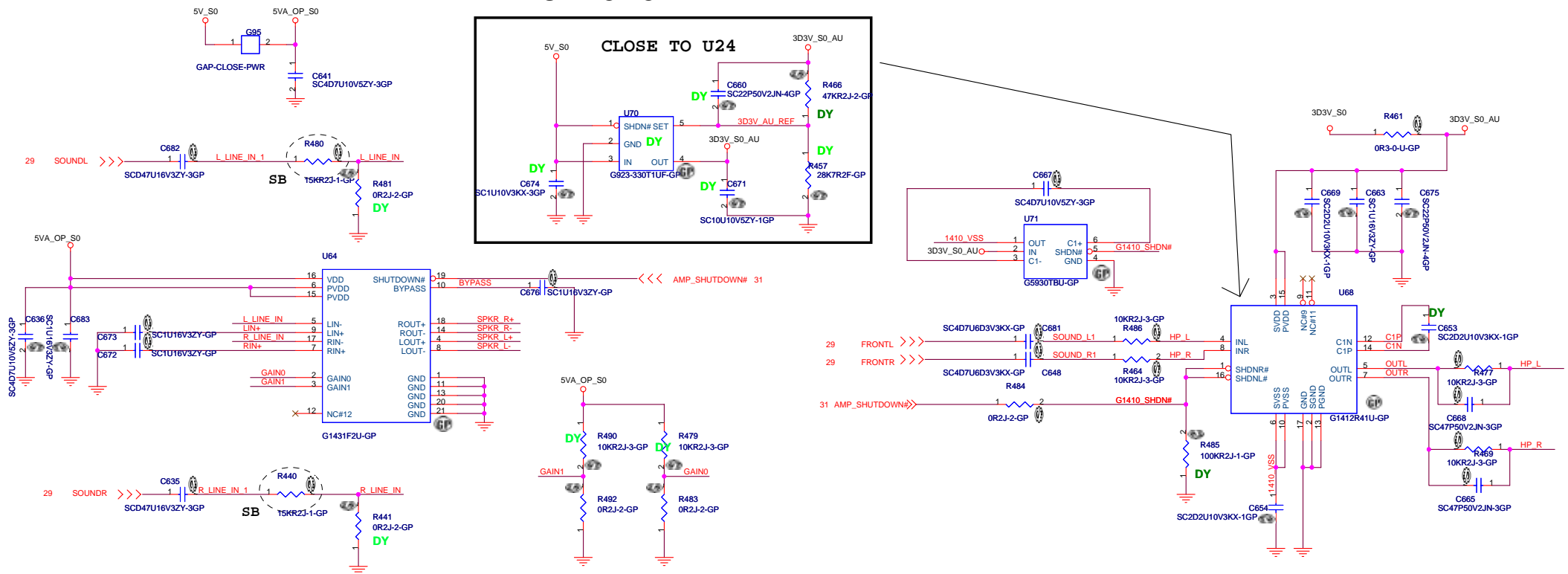
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
MINI CARD / NEW CARD			
Size	Document Number		Rev
	Orta		SA
Date:	Tuesday, December 12, 2006	Sheet 28 of 46	

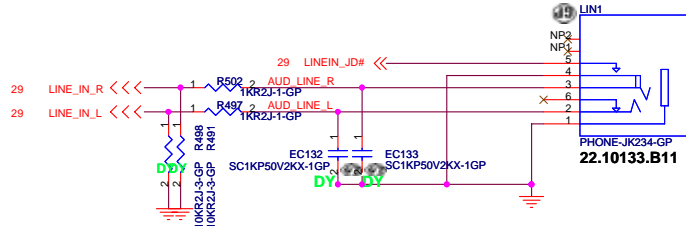


AUDIO OP AMPLIFIER

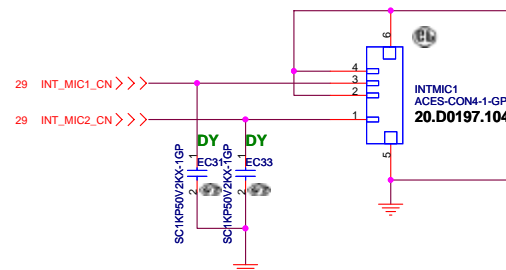
KBC_MUTE_GPIO8



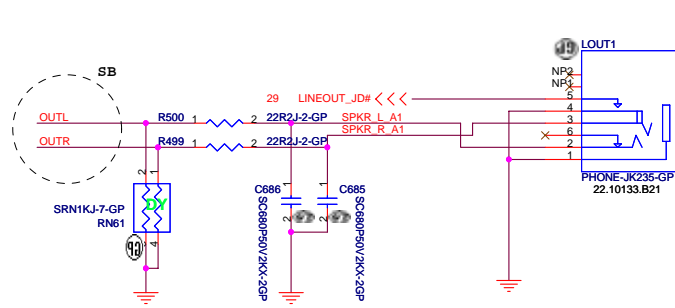
LINE IN



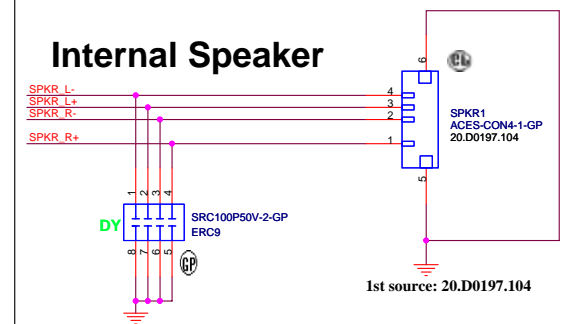
Internal Microphone



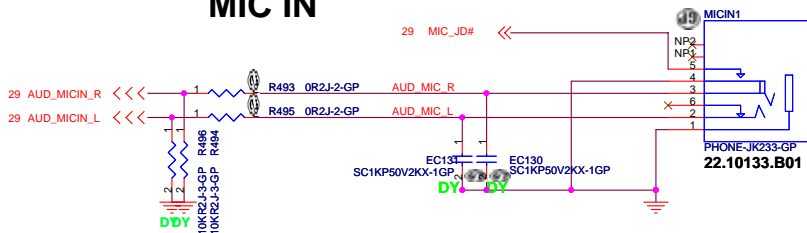
LINE OUT

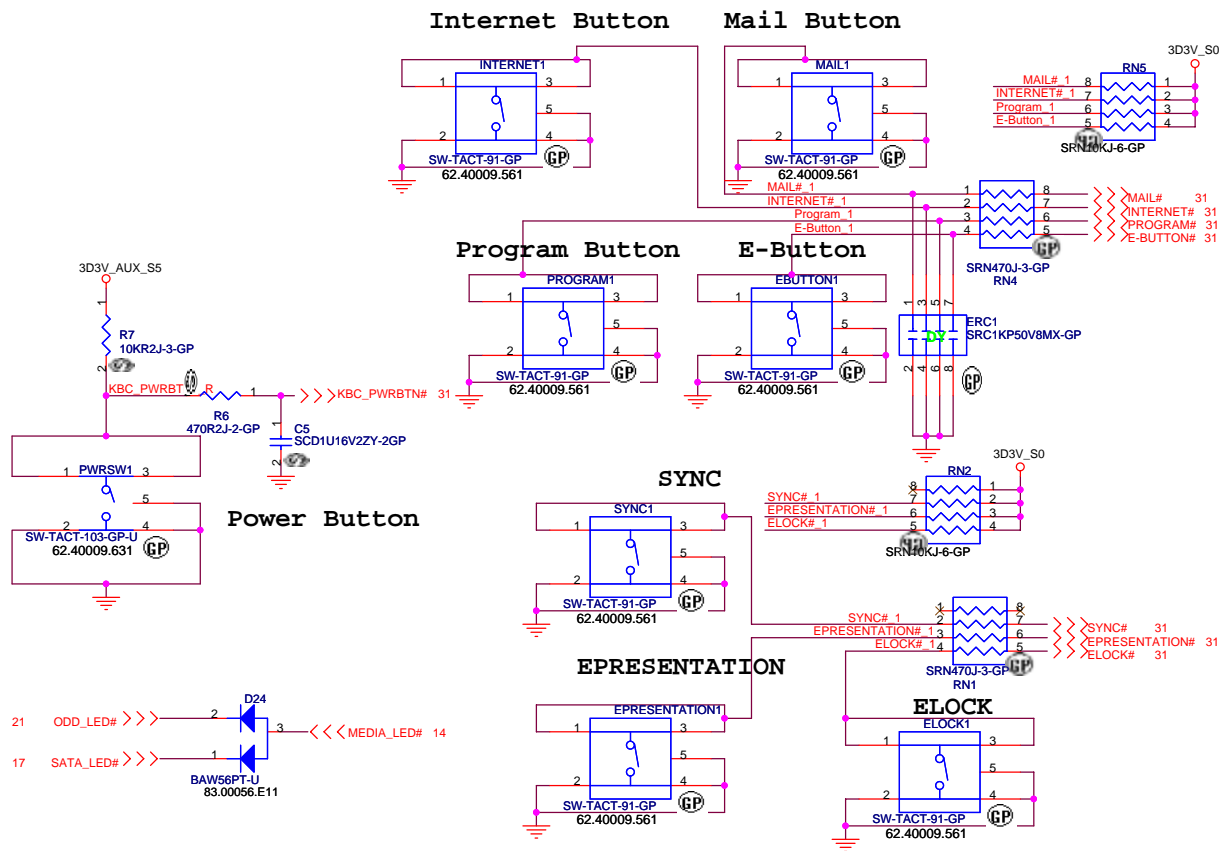


Internal Speaker



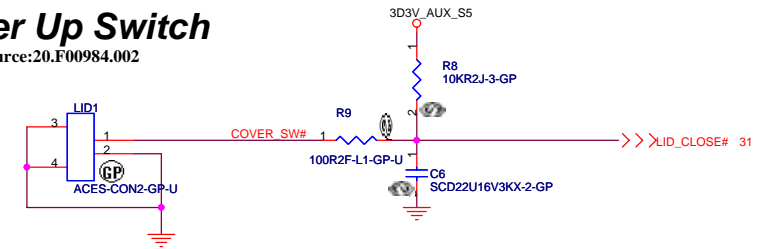
MIC IN



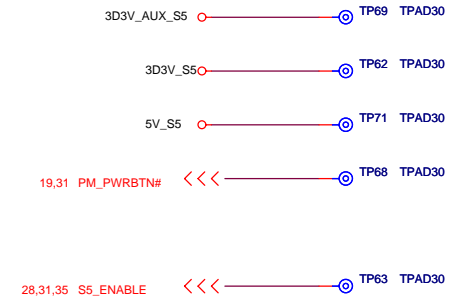


Cover Up Switch

2nd source:20.F00984.002

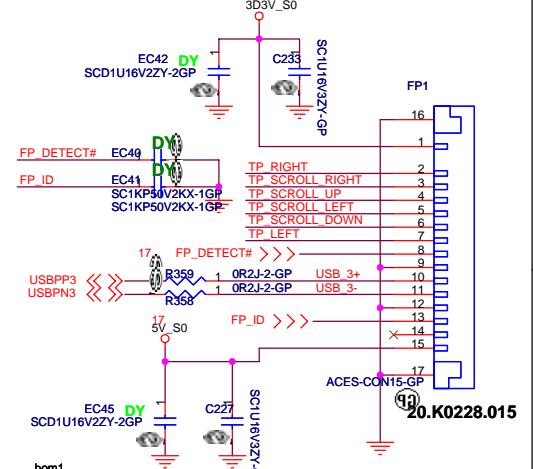
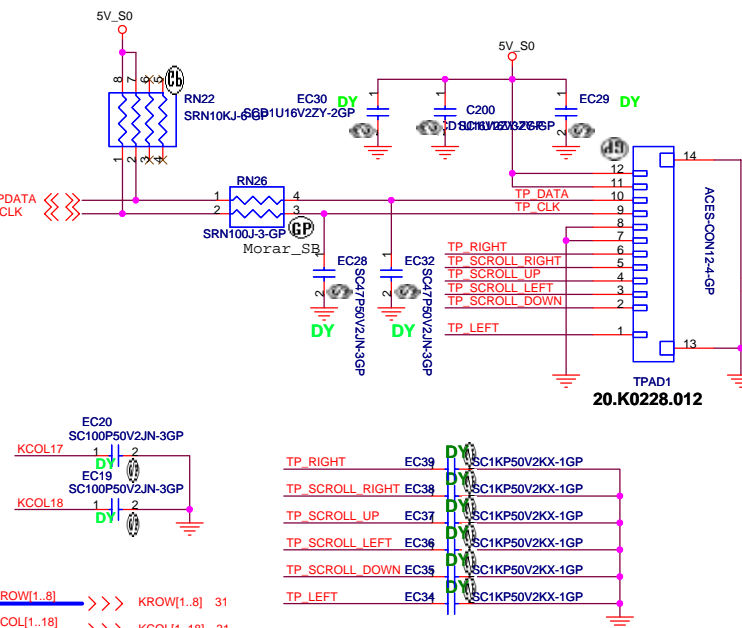
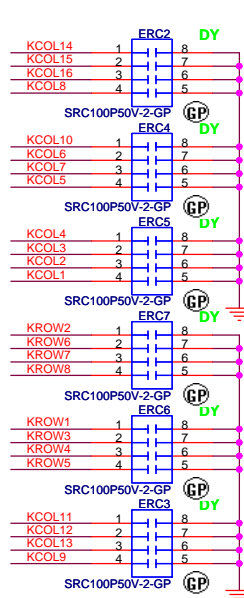
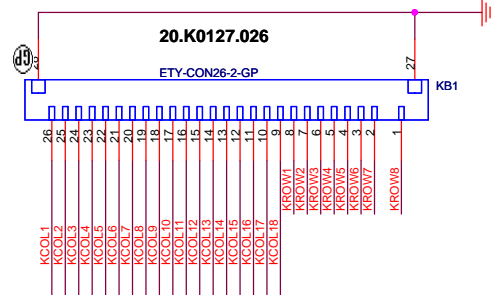


Check test point



Test Point放在Dimm Door打開可量測處

EMI Bypass cap.



緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.

Title: **BUTTONS / KB / TOUCHPAD**

Size: **Orta**

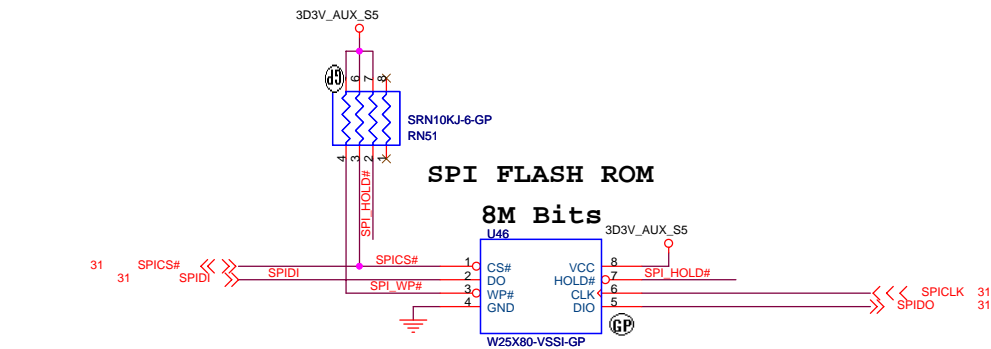
Date: Tuesday, December 12, 2006

Sheet: 32 of 46

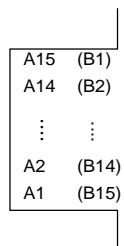
Rev: SA

Internal KeyBoard CONN

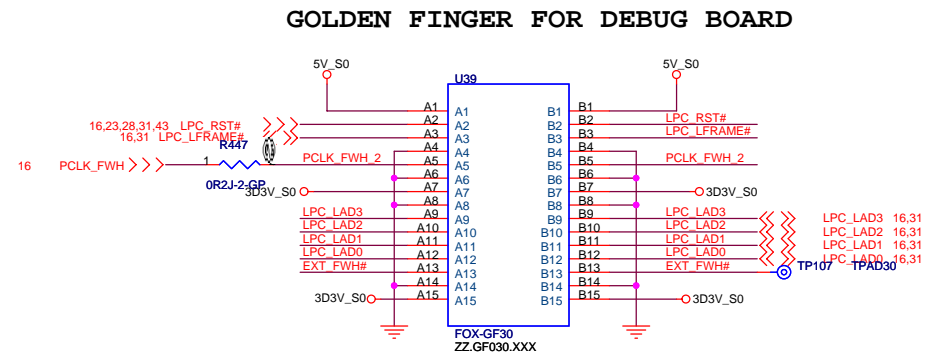




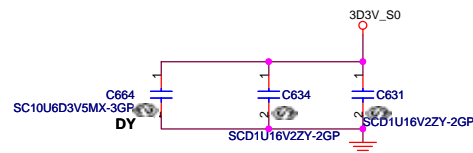
TOP VIEW



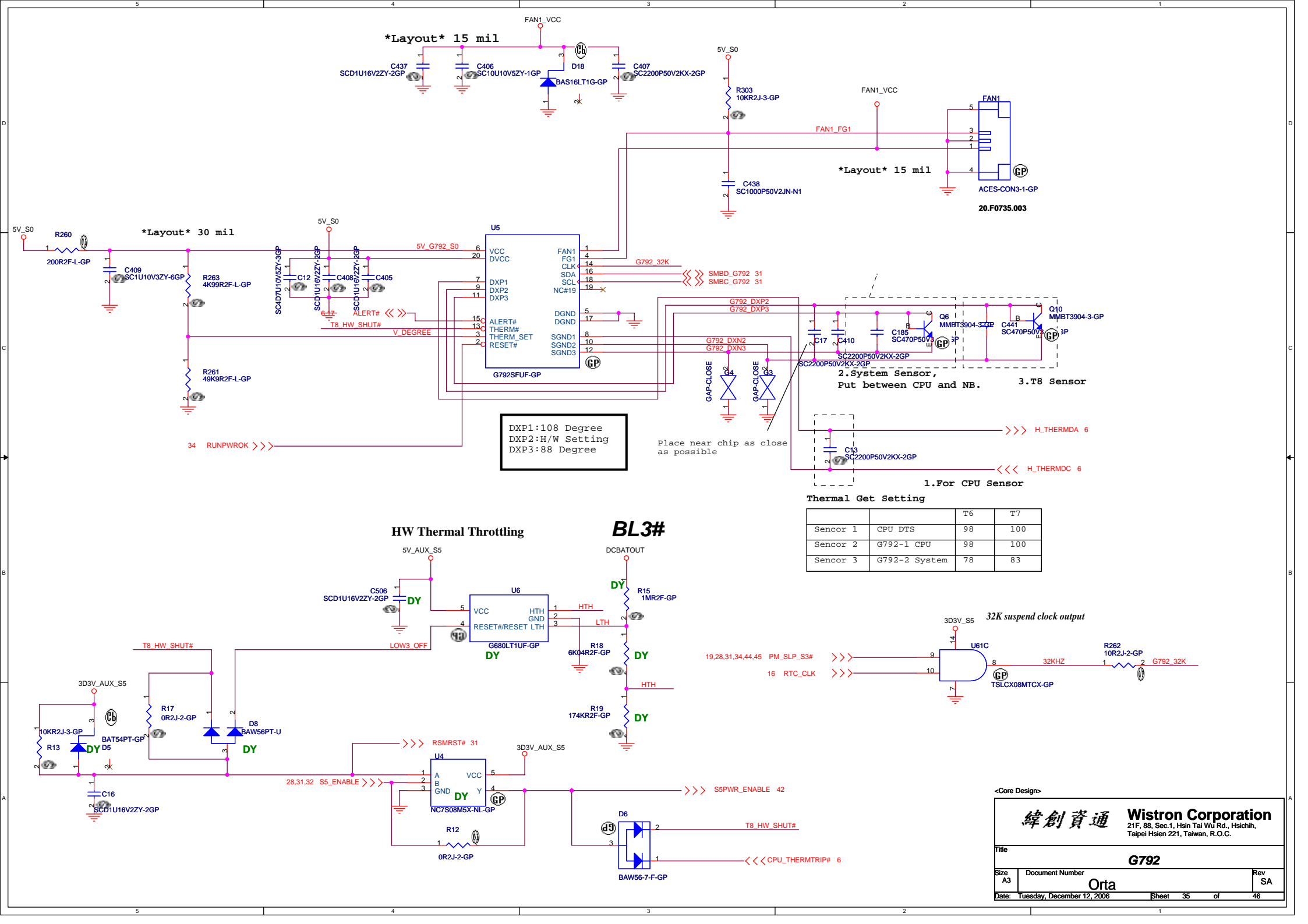
(BOTTOM VIEW)



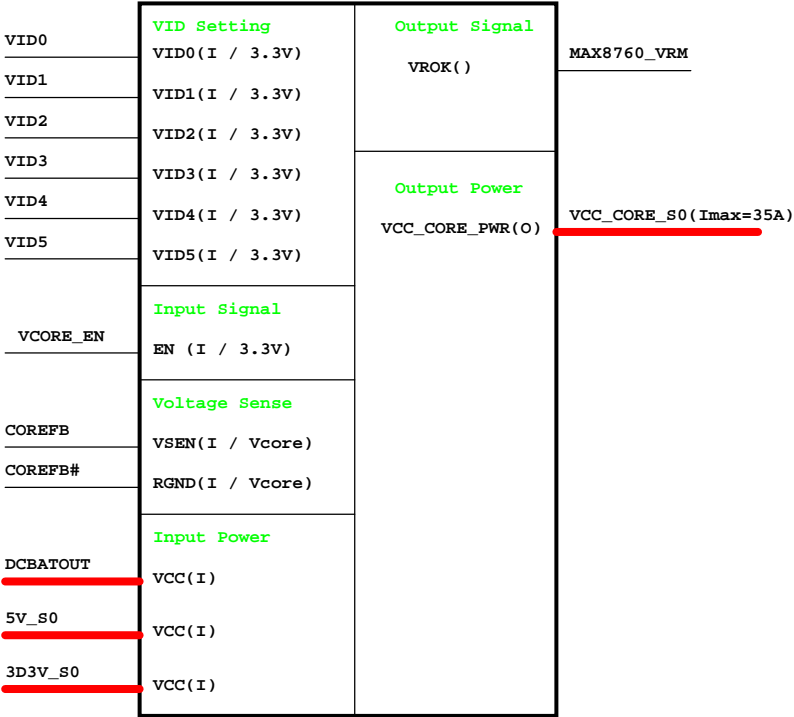
Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



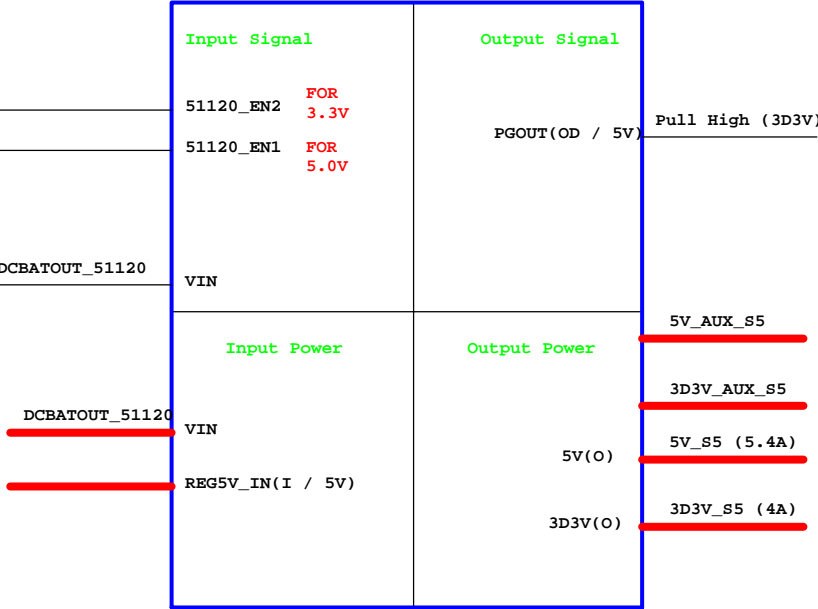
<Core Design>



CPU_CORE
ISL6264CRZ



TI TPS51120
3D3V/5V



2D5V_S0



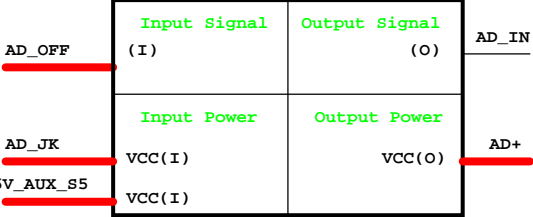
APL5913

1D8V_S5

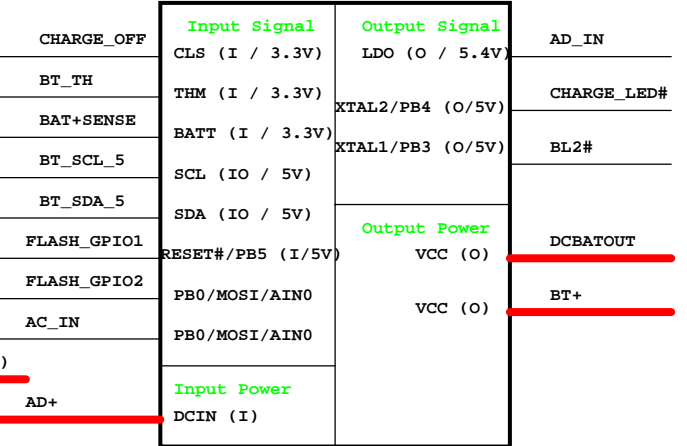


APL5332KAC-TRLGP

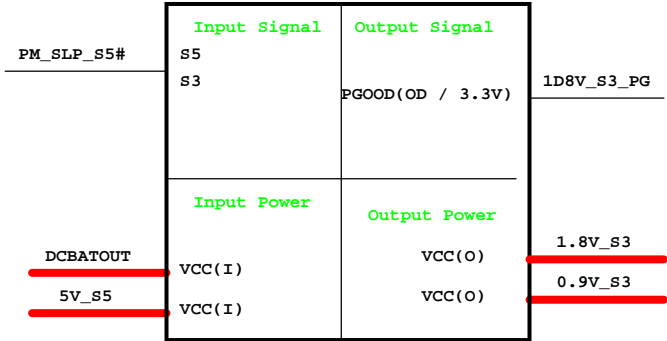
Adapter



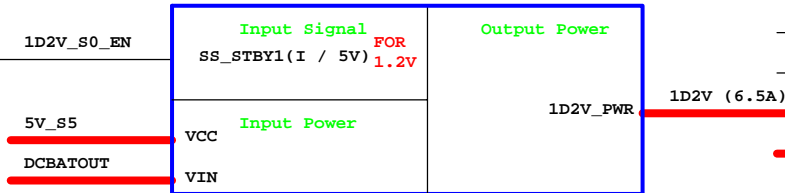
Charger_ISL6255



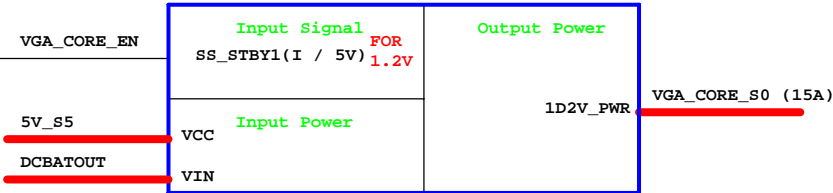
TI TPS51116
1.8V / 0.9V



ISL6268_1D2V



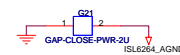
ISL6268_VGA_CORE

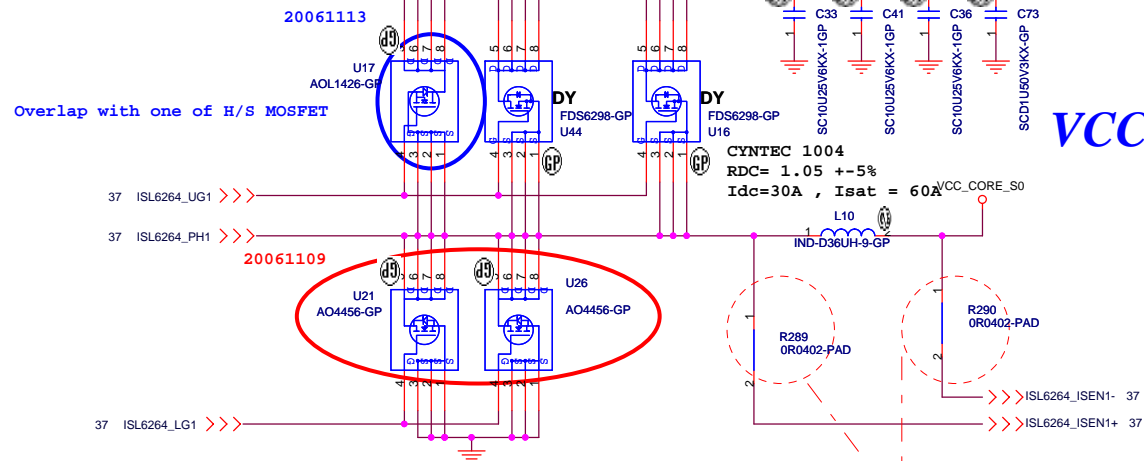


<Core Design>

VID=1.20V(25W)/1.15V(35W)
Iomax=21A(25W)/35A (35W)
OCP=40A~45A

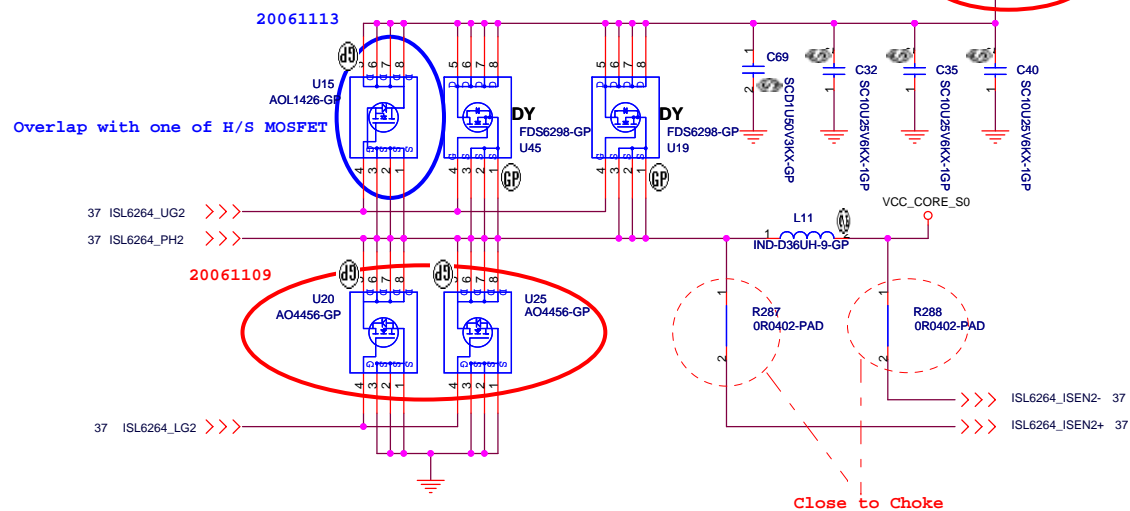
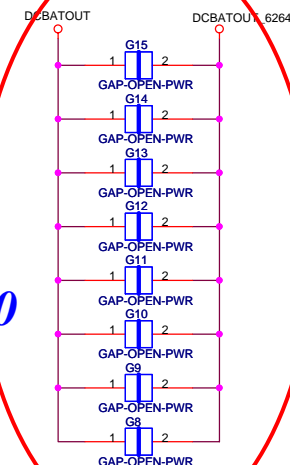
vDbs	vD4	vD3	vD2	vD1	vD0	dAc
0	0	0	0	0	0	1.550
0	0	0	0	0	1	1.525
0	0	0	0	1	0	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	1	0	0	0	1.375
0	0	1	0	0	1	1.350
0	0	1	0	0	1	1.325
0	0	1	1	0	0	1.300
0	0	1	1	0	1	1.275
0	0	1	1	1	0	1.250
0	0	1	1	1	1	1.225
0	0	1	1	1	0	1.200
0	0	1	1	1	1	1.175
0	1	0	0	0	0	1.150
0	1	0	0	0	1	1.125
0	1	0	0	1	0	1.100
0	1	0	0	1	1	1.075
0	1	0	1	0	0	1.050
0	1	0	1	0	1	1.025
0	1	0	1	1	0	1.000
0	1	0	1	1	1	0.975
0	1	1	0	0	0	0.950
0	1	1	0	0	1	0.925
0	1	1	0	1	0	0.900
0	1	1	1	0	0	0.875
0	1	1	1	0	1	0.850
0	1	1	1	1	0	0.825
0	1	1	1	1	0	0.800
0	1	1	1	1	1	0.775
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.75
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.725
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7
1	1	1	1	1	1	0.375



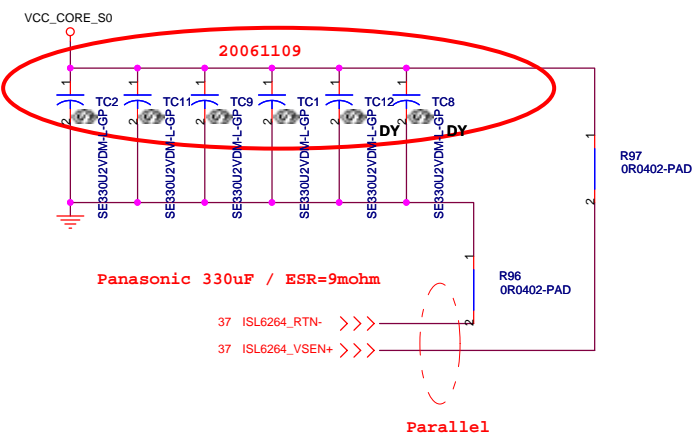


VCC_CORE_S0

20061109



20061109



<Core Design>

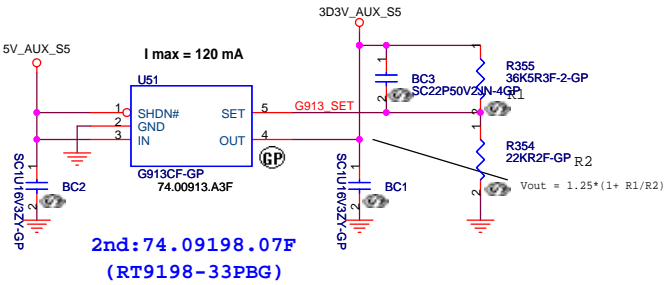
緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title			
CPU Vcore Power_2			
Size	Document Number		Rev
A3	Orta		SA
Date:	Tuesday, December 12, 2006	Sheet 38 of	46

Aux Power

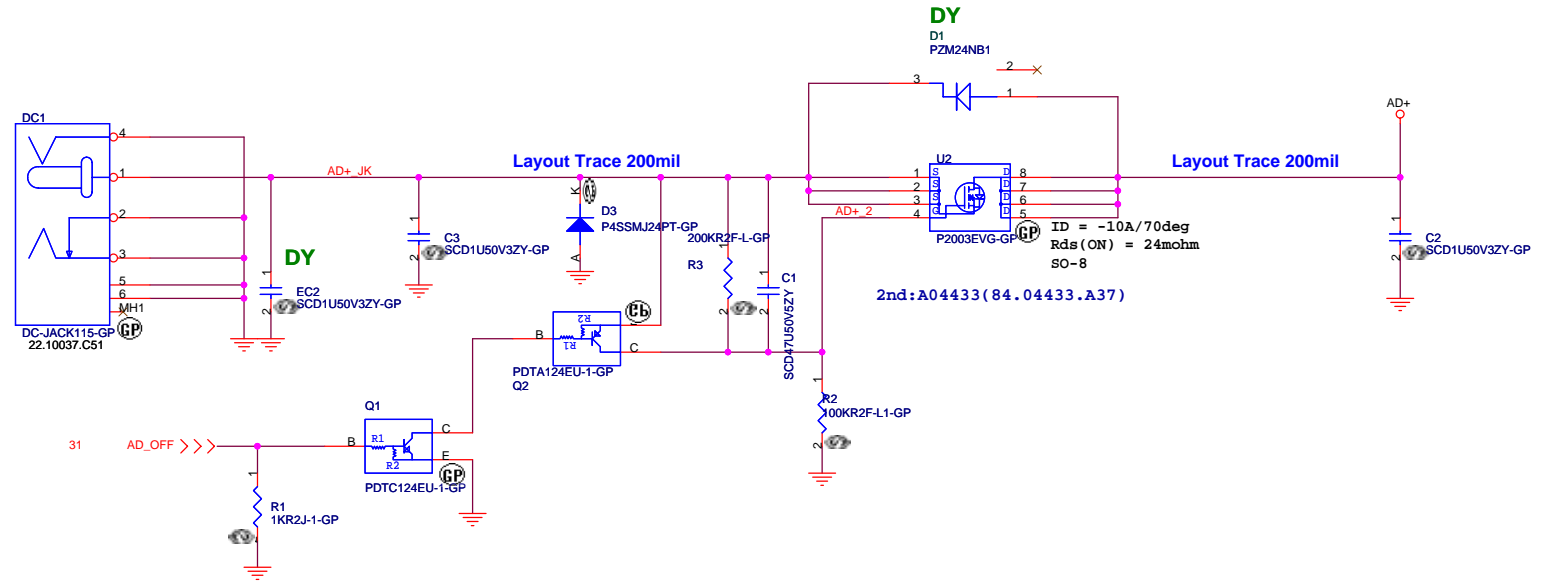
3D3V_AUX_S5



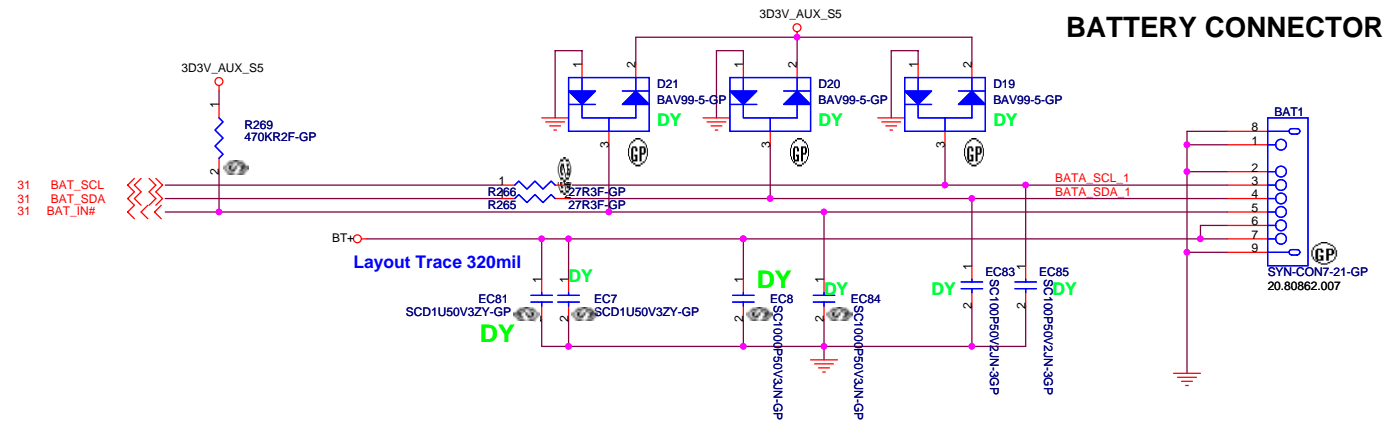
<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
3D3V AUX			
Size	Document Number		Rev
A3	Orta		SA
Date:	Tuesday, December 12, 2006	Sheet 39 of 46	

Adaptor in to generate DCBATOUT

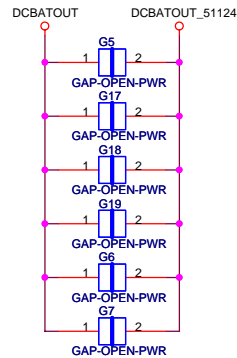


BATTERY CONNECTOR



<Variant Name>

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
AD/BATT CONN			
Size	Document Number	Rev	
A3		SA	
Date: Tuesday, December 12, 2006		Sheet	41 of 46



Id=9.6A
Qg=18~nC,
Rdson=13.5~16.5mohm

Id=13.2A
Qg=27nC,
Rdson=6.8~8.2mohm

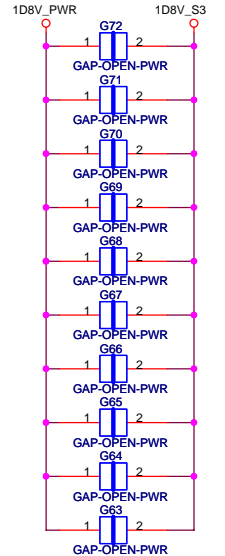
Tai-Tech
DCR=3.5m ohm
Irms=20A, Isat=28A

1D8V Iomax=8A
OCP>16A

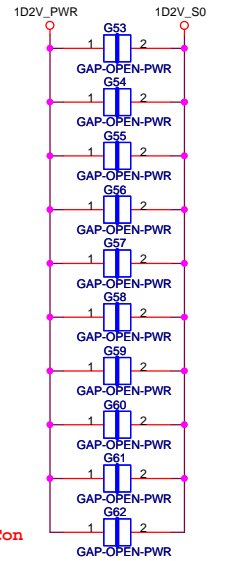
Voutsetting=1.8046V

Nippon
Chemi-Con
Al Cap.
390uF/2D5V
ESR=15mohm

Kemet
220uF/ 4V
ESR=15mohm



$$V_{out} = 0.758V * (R1 + R2) / R2$$



1D2V Iomax=8A
OCP>16A

Voutsetting=1.2047V

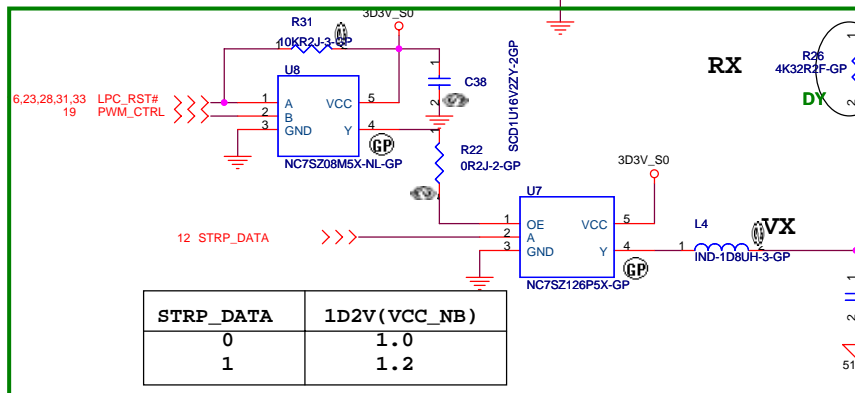
Kemet
220uF/ 4V
ESR=15mohm

Nippon
Chemi-Con
Al Cap.
390uF/2D5V
ESR=15mohm

$$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$$

$$I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in} - V_{out}) * V_{out}) / V_{in}))$$

	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2



STRP_DATA	1D2V(VCC_NB)
0	1.0
1	1.2

<Core Design>

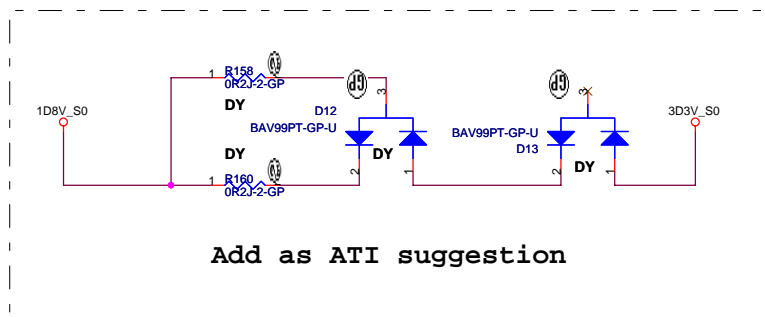
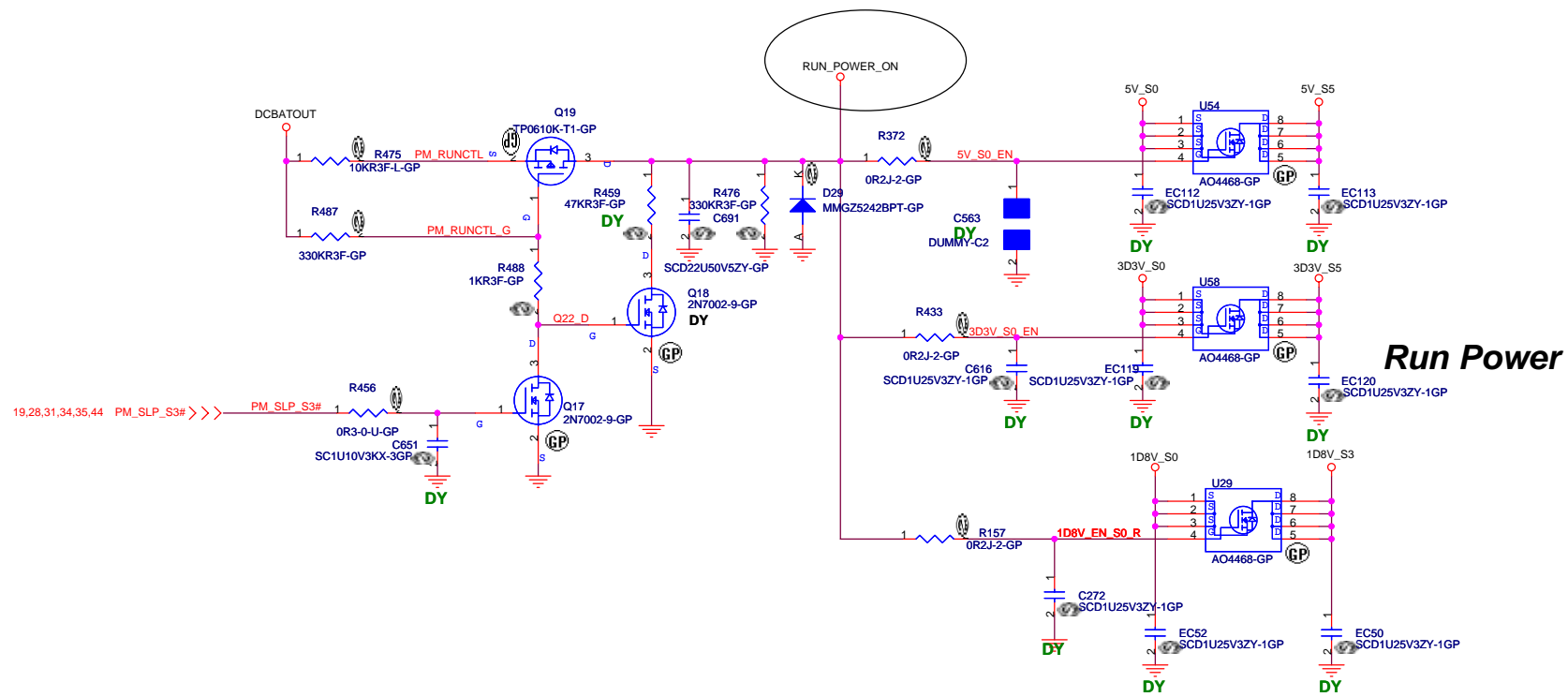
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

TPS51124 1D8V 1D2V

Title: **Orta** Rev: **SA**

Size: A3 Document Number: **Orta**

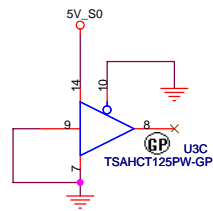
Date: Tuesday, December 12, 2006 Sheet 43 of 46



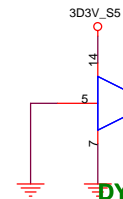
Power On Logic

<Core Design>

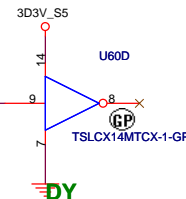
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title PWR CTL LOGIC / PWR PLANE			
Size A3	Document Number Orta	Rev SA	
Date: Tuesday, December 12, 2006		Sheet 45	of 46



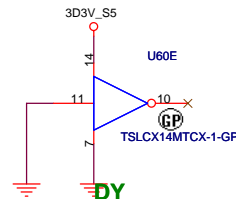
DUMMY in SA



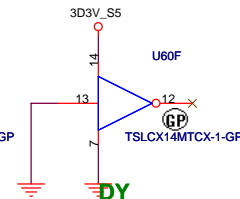
34.42Y01.001



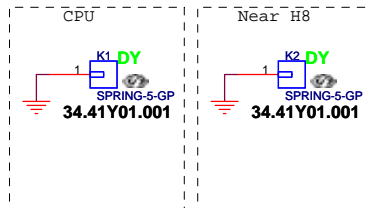
34.42Y01.001



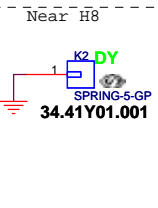
34.4G502.001



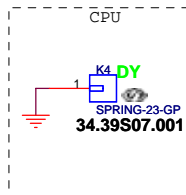
DY



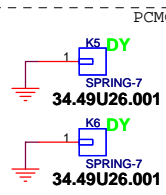
34.42Y01.001



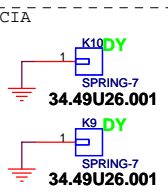
34.42Y01.001



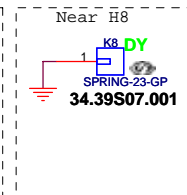
34.39S07.001



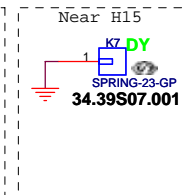
34.49U26.001



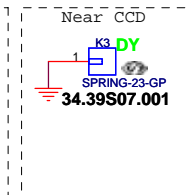
34.49U26.001



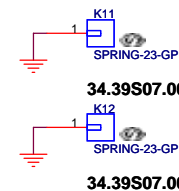
34.39S07.001



34.39S07.001

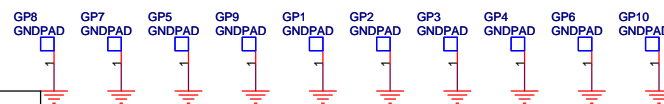
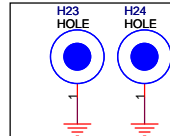
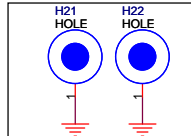
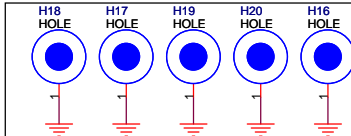
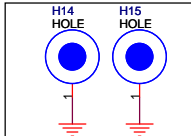
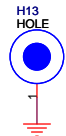
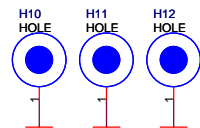
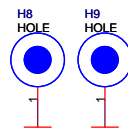
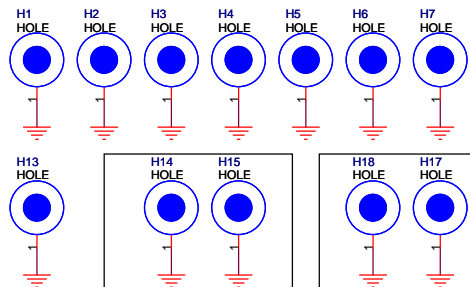


34.39S07.001



34.39S07.001

TOP(CARD READER BD)
34.42Y01.011

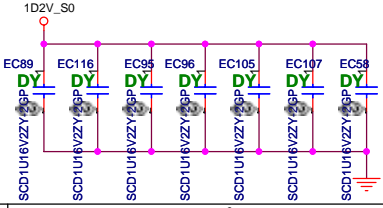
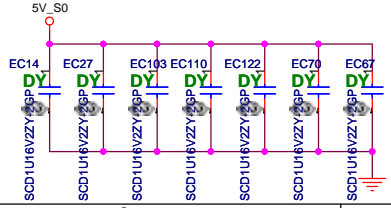
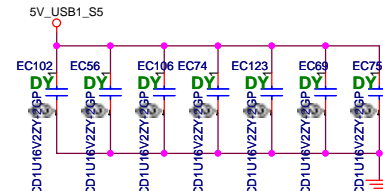
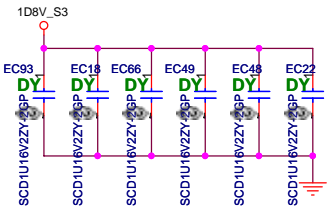
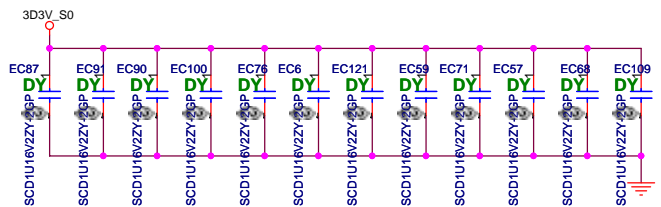
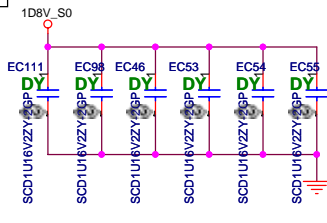
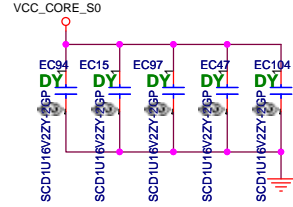
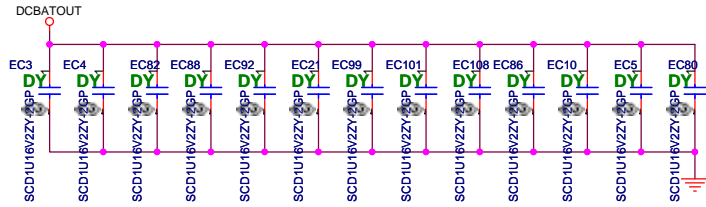


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34.42Y01.011

BOT(CPU)
34.42Y01.011

BOT(SB)
34.42Y01.011

BOT(MINI CARD)
34.4G502.001



<Core Design>

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Size	Document Number	SA
Date: Tuesday, December 12, 2006		Sheet 46 of 46