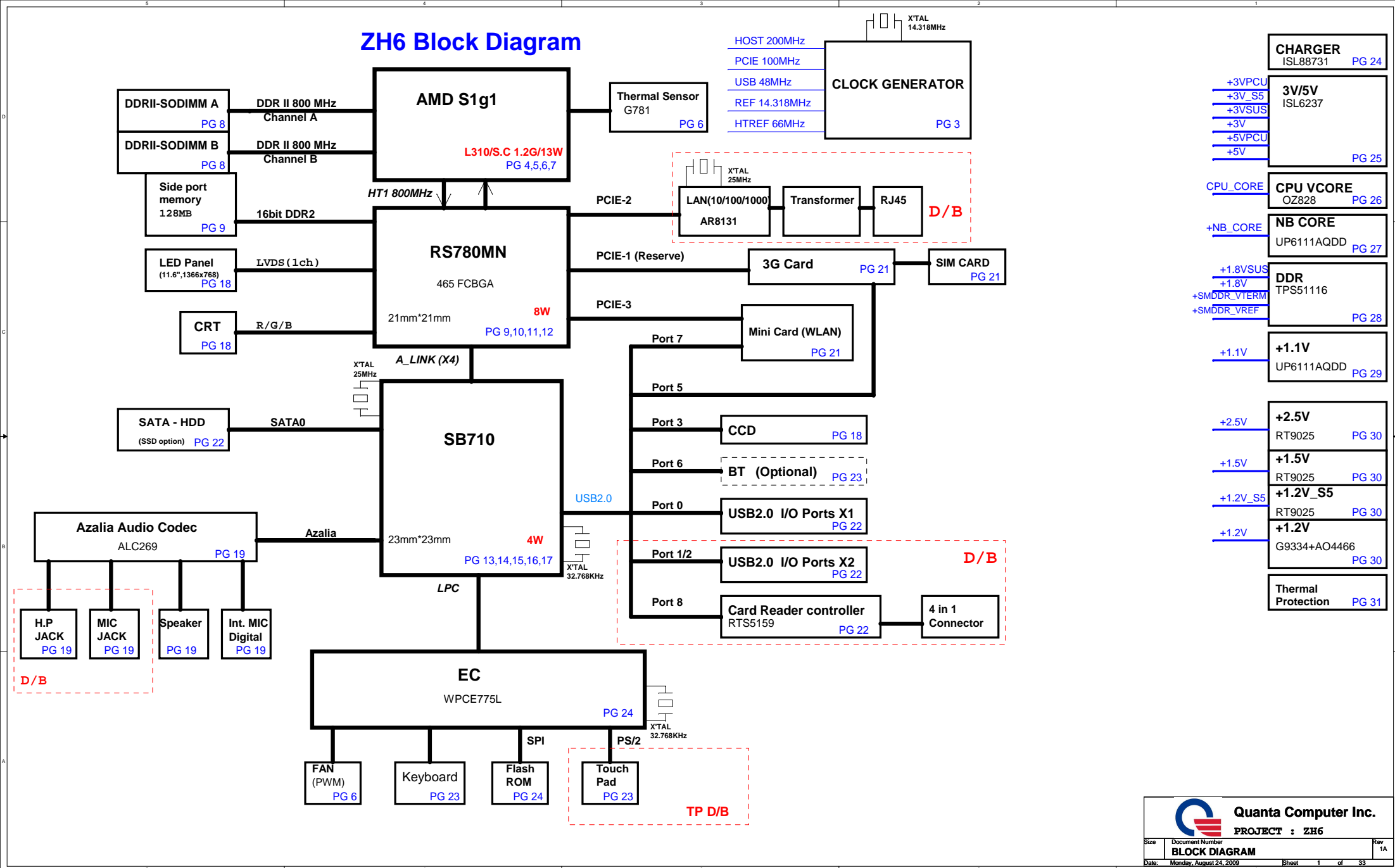
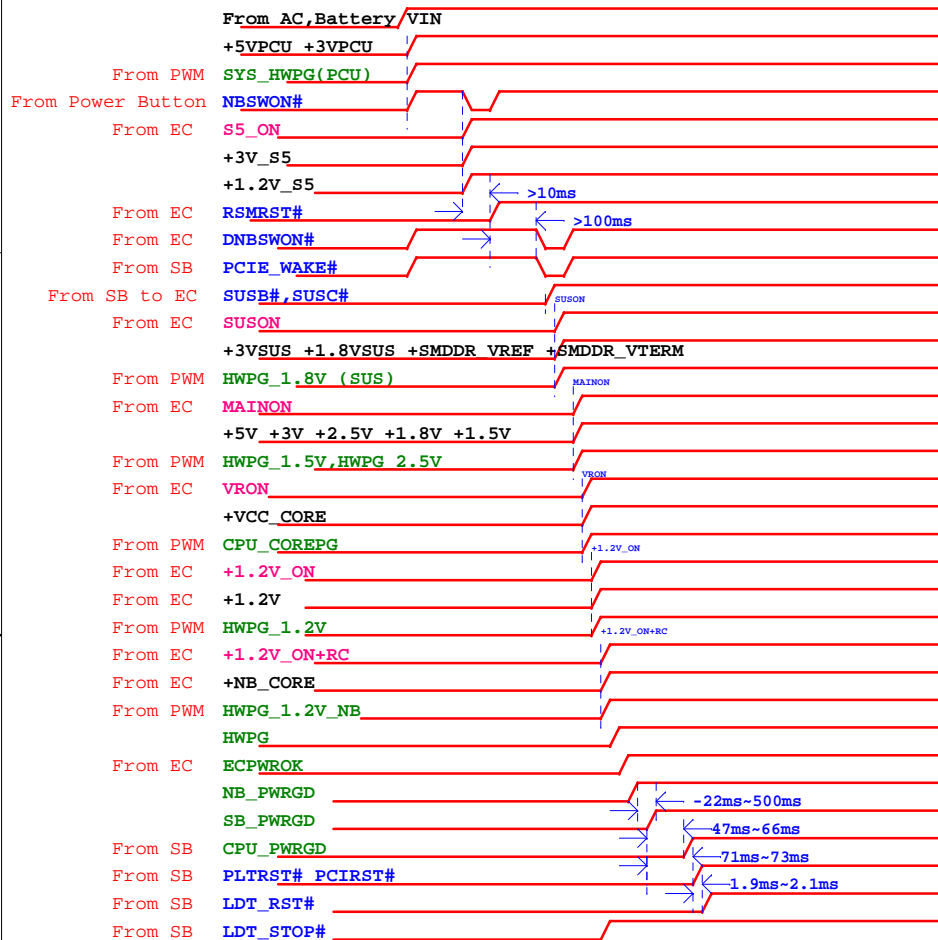


ZH6 Block Diagram



ZH6 Power On Sequence



*Note: EC will sampling SUSB# & SUSC# every 5ms.

AMD SB710 SMBUS Table

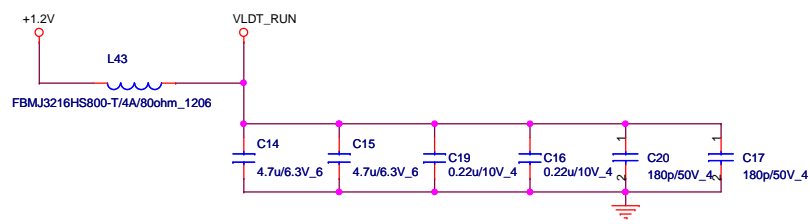
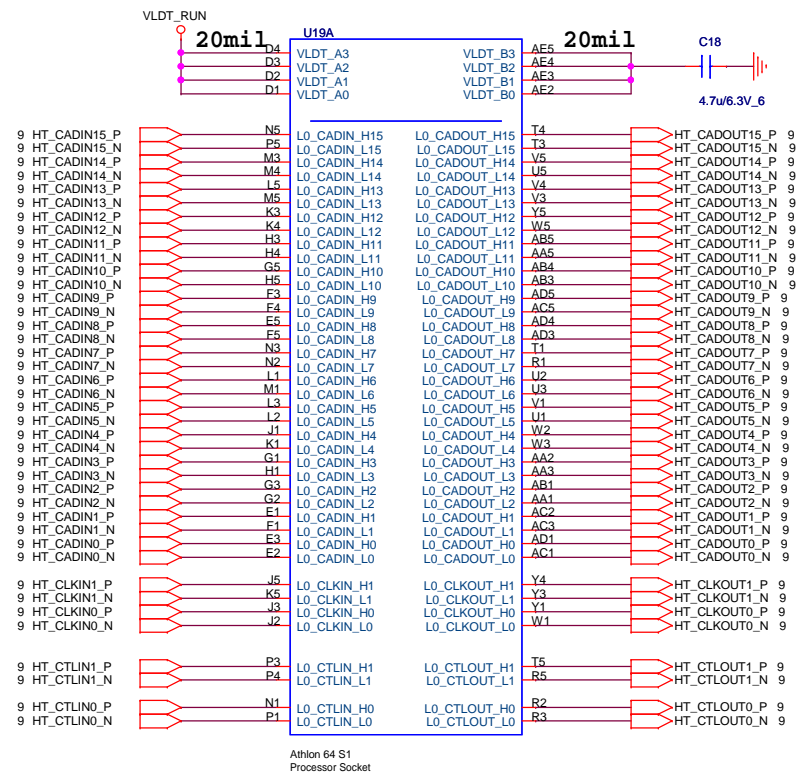
	CLK GEN	RAM	Mini Card (WLAN)
SB710 SDATA0/SCLK0(+3V)	V	V	V
SB710 SDATA1/SCLK1(+3V_S5)			
Power Plane	+3V	+3V	+3V
MOS CKT	Reserve	Reserve	Reserve

BOM naming rule

Items	Function	Name	Description
1	3G Module	3G@	
2	HDT debug function	HDT@	
3			
4			
5			
6			
7			
8			
9			
10			
11			
12			
13			
14			
15			
16			
17			
18			
19			
20			
21			
22			
23			
24			
25			

EC SMBUS Table

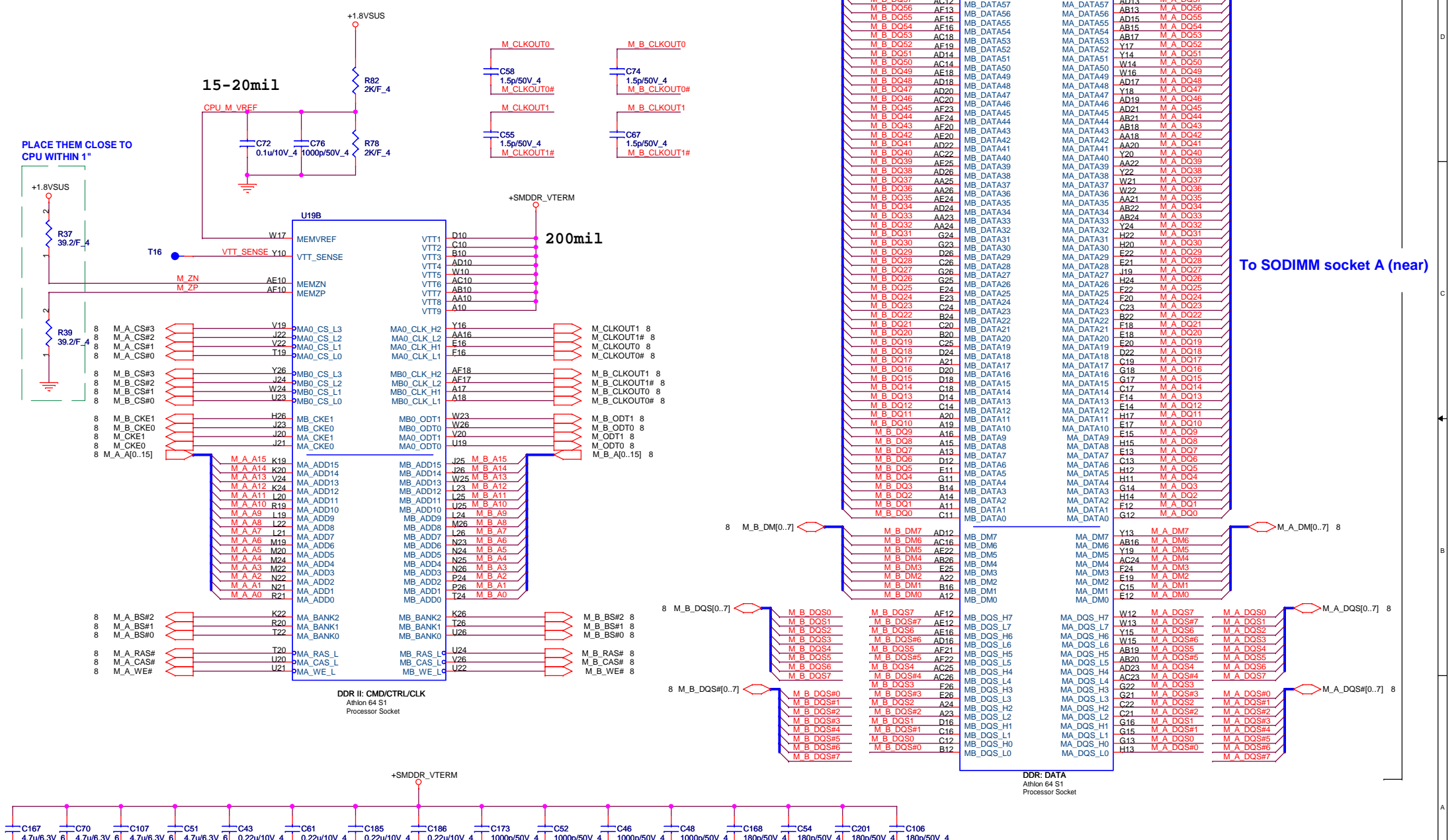
	Battery	CPU thermal Sensor	EC EEPROM
EC775 SDATA1/SCLK1(+3VPCU)	V		
EC775 SDATA2/SCLK2(+3VPCU)		V	
EC775 SDATA3/SCLK3(+3VPCU)			V
EC775 SDATA4/SCLK4(+3VPCU)			
Power Plane	+3VPCU	+3V	+3VPCU
MOS CKT	X	X	X




Power name	Description	Voltage
VLDT_A/B	HyperTransport I/O ring power supply	1.2V

(CPU)

Processor DDR2 Memory Interface



Power name	Description	Voltage
VTT	VTT Power	0.9V



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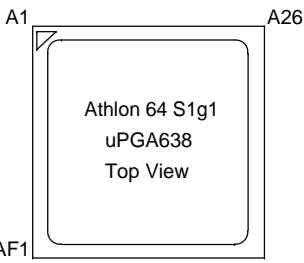
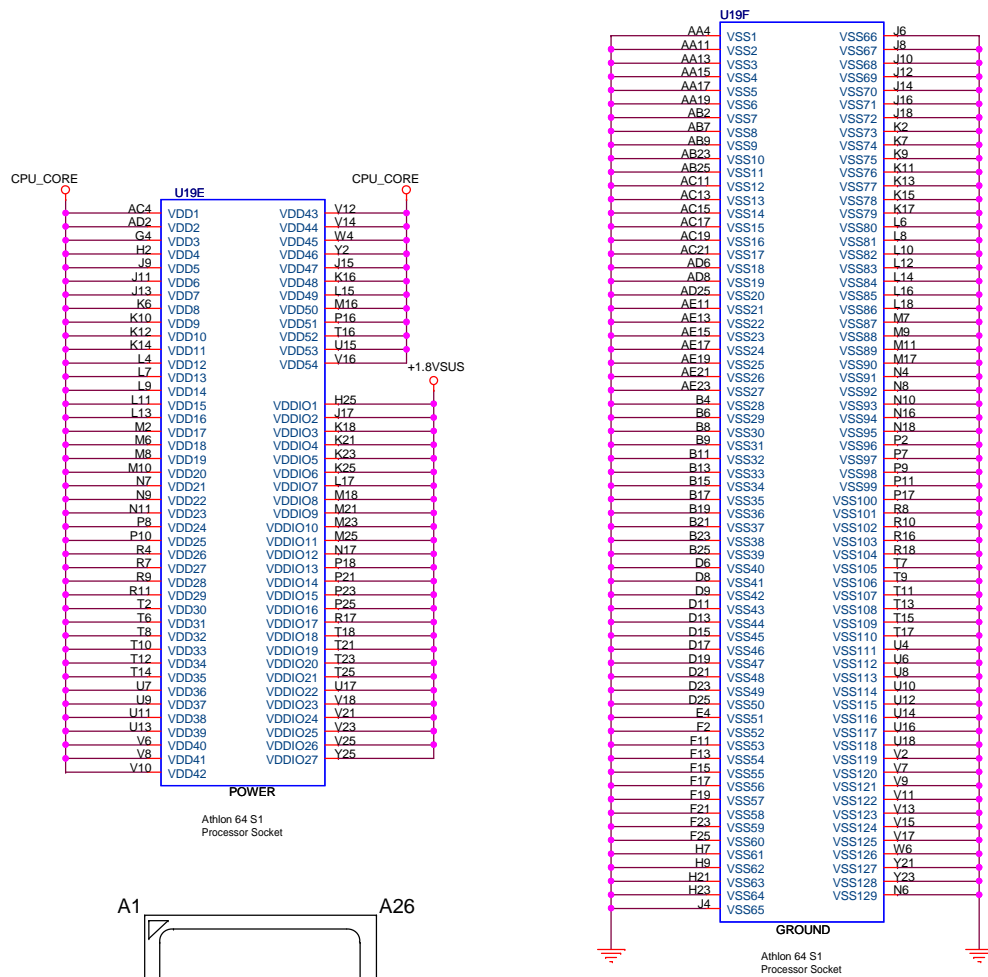
PROJECT : ZH6

TURION 64 DDRII I/F

Size	Document Number	Rev
		1A

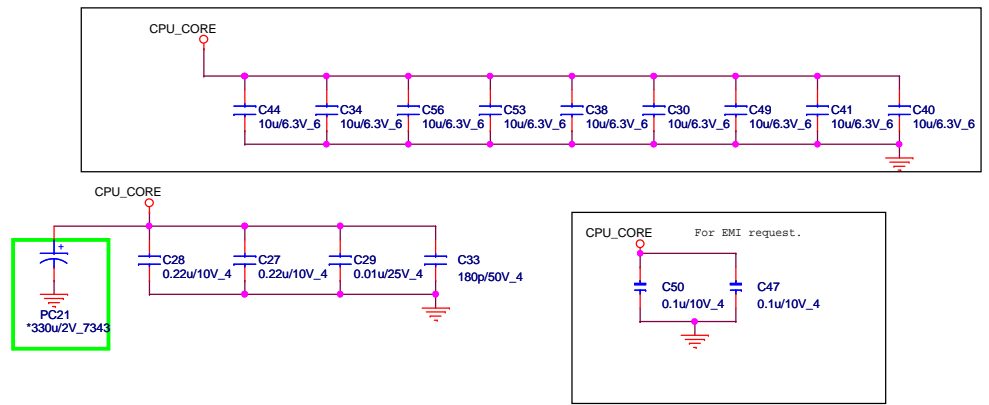
Date: Monday, August 24, 2009 Sheet 5 of 33

PROCESSOR POWER AND GROUND(CPU)

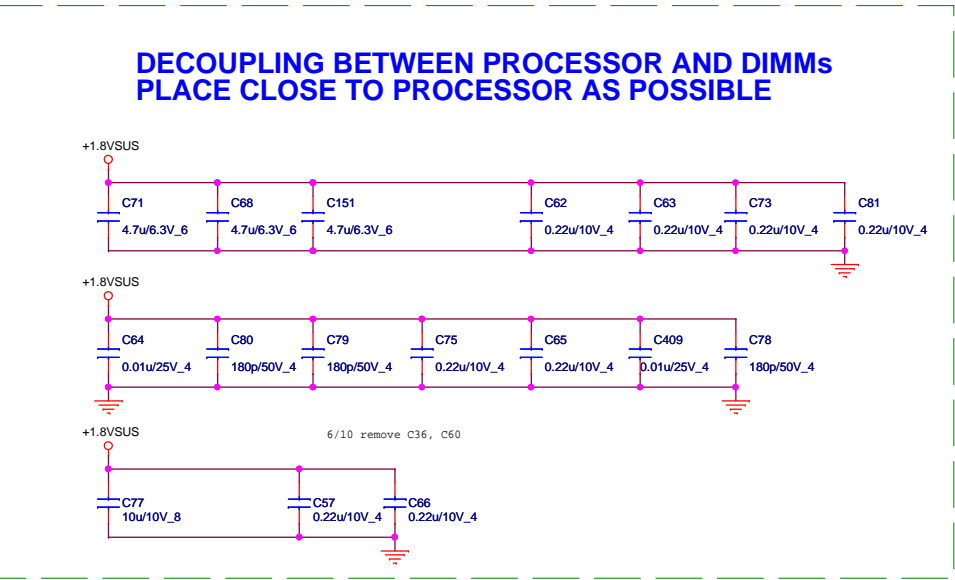



Power name	Description	Voltage
VDD	Core power supply	1.05V
VDDIO	DDR SDRAM I/O ring power supply	1.8V

BOTTOMSIDE DECOUPLING



DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE

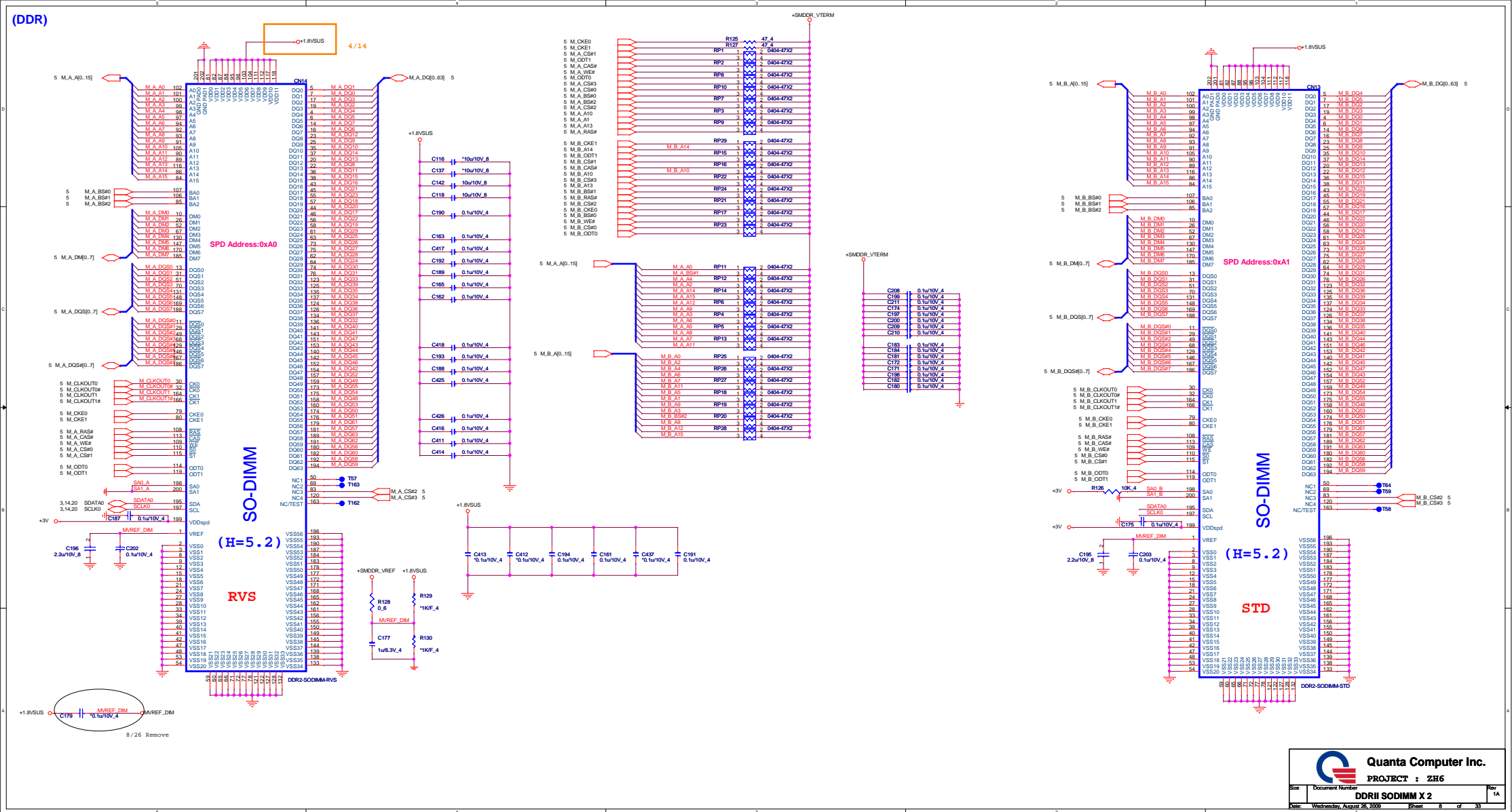




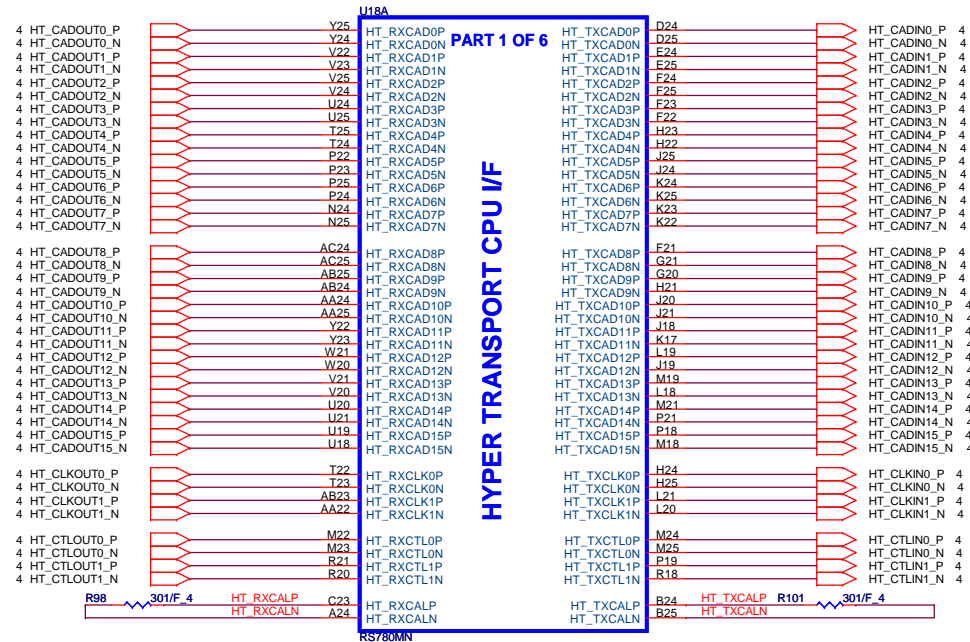
Quanta Computer Inc.
PROJECT : ZH6
TURION 64 PWR & GND

Size	Document Number	Rev
		1A

Date: Monday, August 24, 2009Sheet 7 of 33



RS780(CLG)



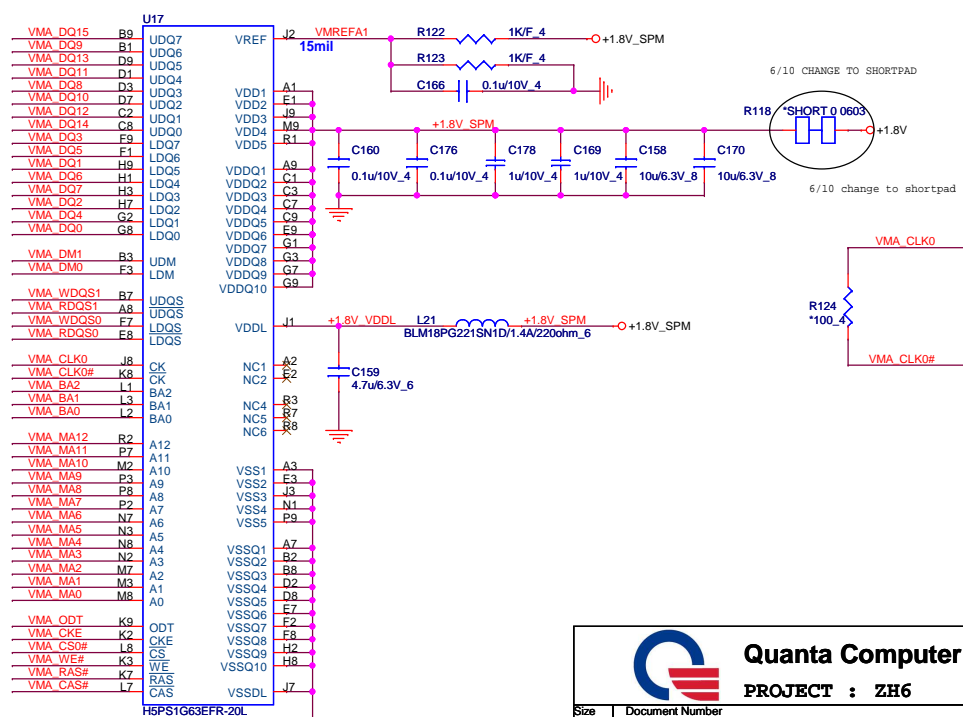
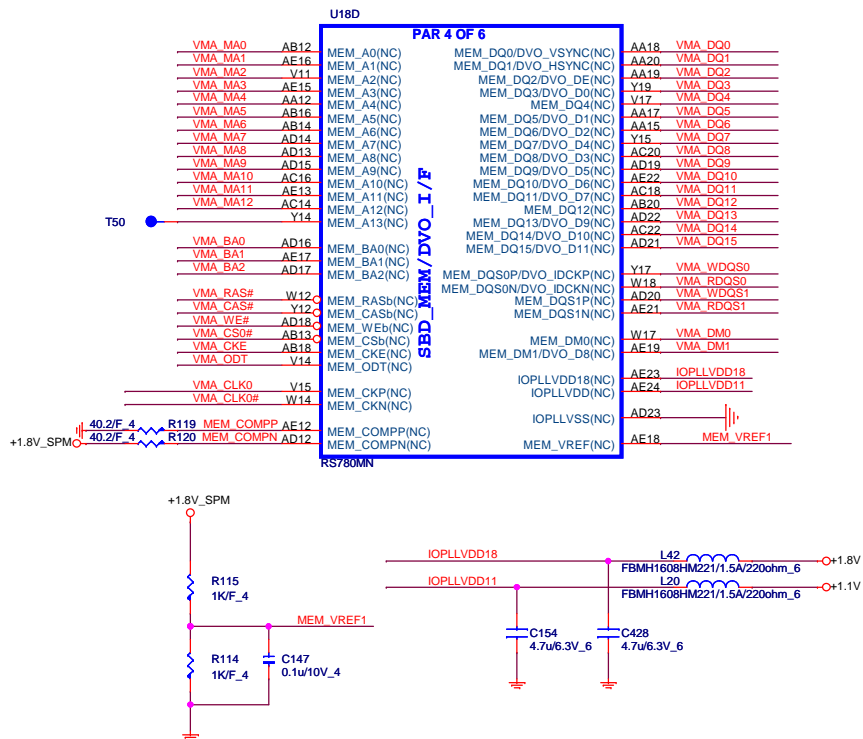
signals	RS780	RX780
HT_TXCALP	R2364 301 ohm 1%	R2364 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R2365 301 ohm 1%	R2365 1.21k ohm 1%
HT_RXCALN		

RS780(CLG)

SIDE-PORT Reserved

This block is for UMA RS780 only , RX780 NC

SPM(CLG)



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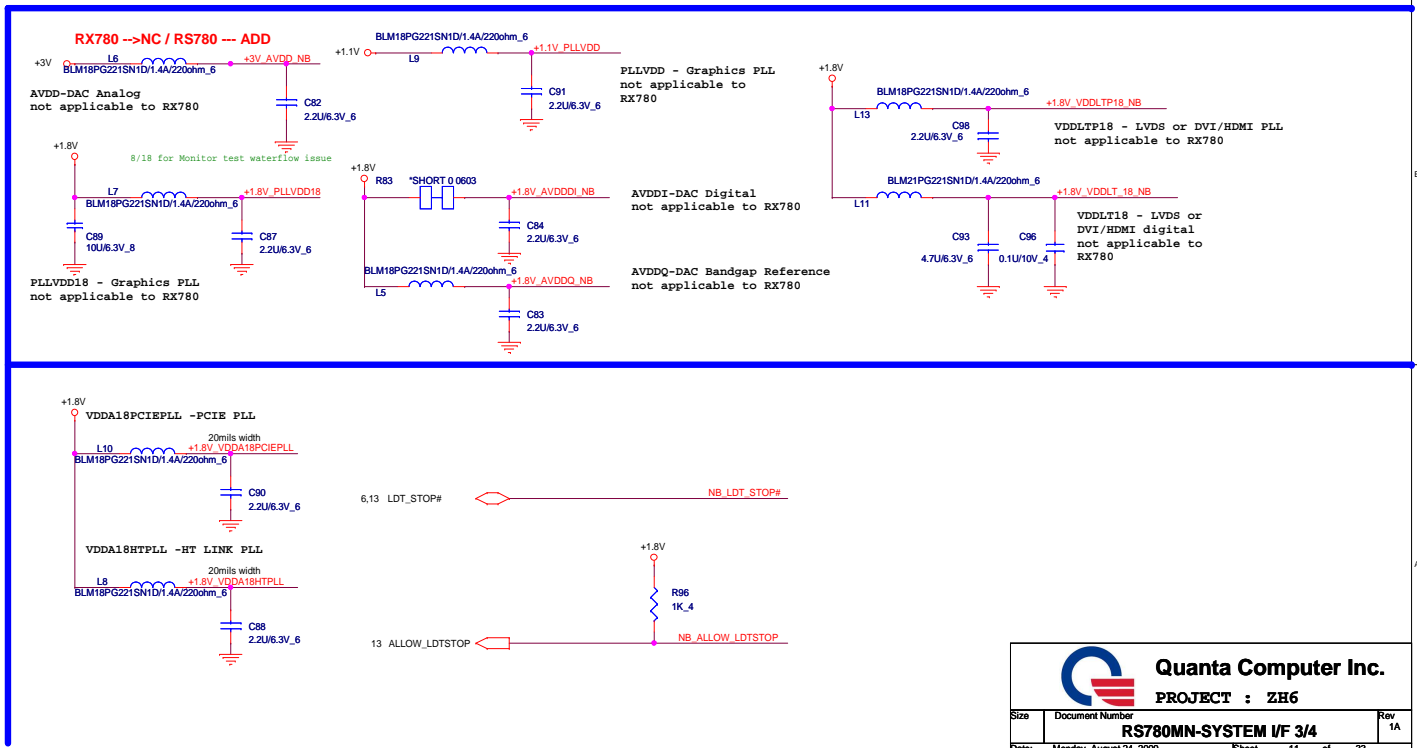
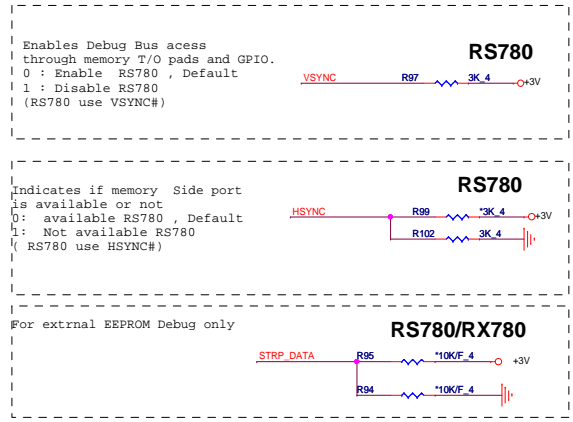
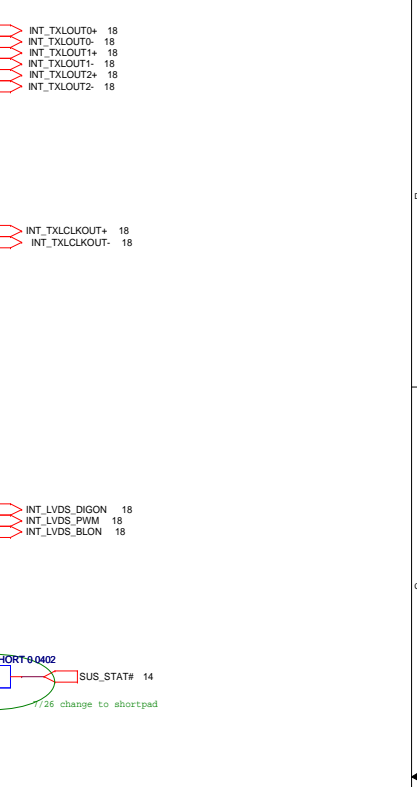
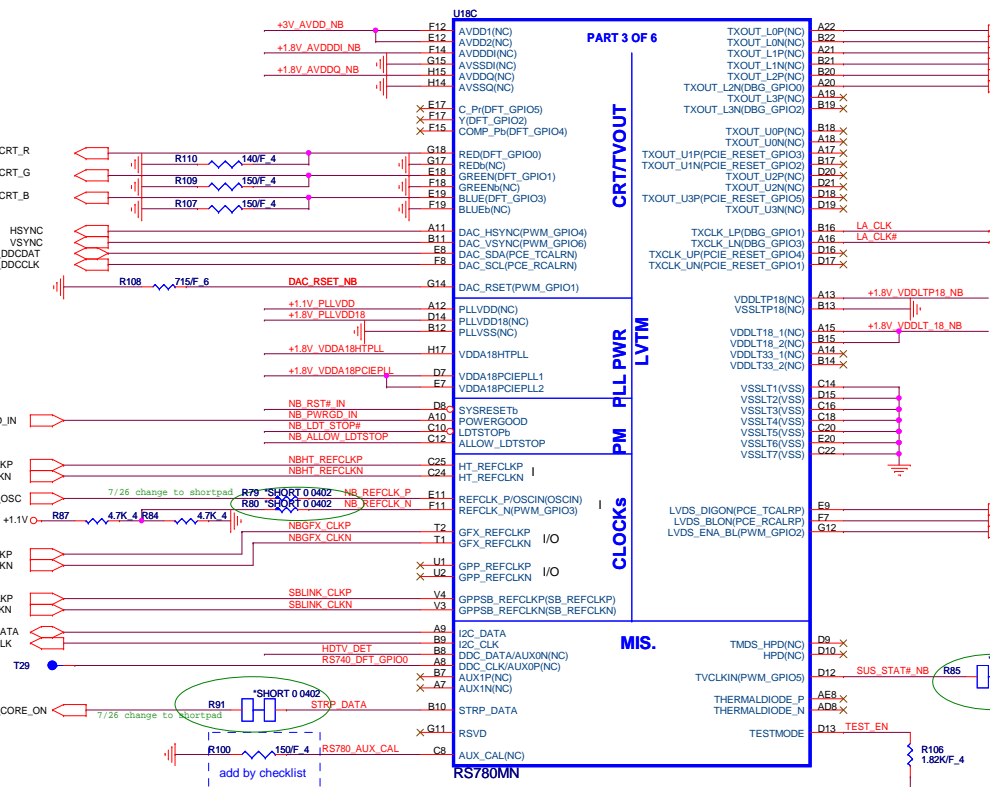
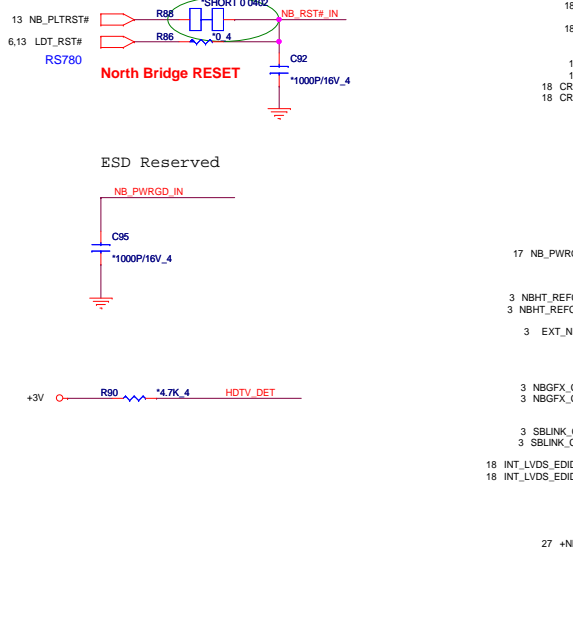
PROJECT : ZH6

Size	Document Number	Rev
	RS780MN-HT LINK I/F 1/4	1A
Date:	Monday, August 24, 2009	Sheet 9 of 33

RS780(CLG)

RX780: Powered from the 1.8-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.

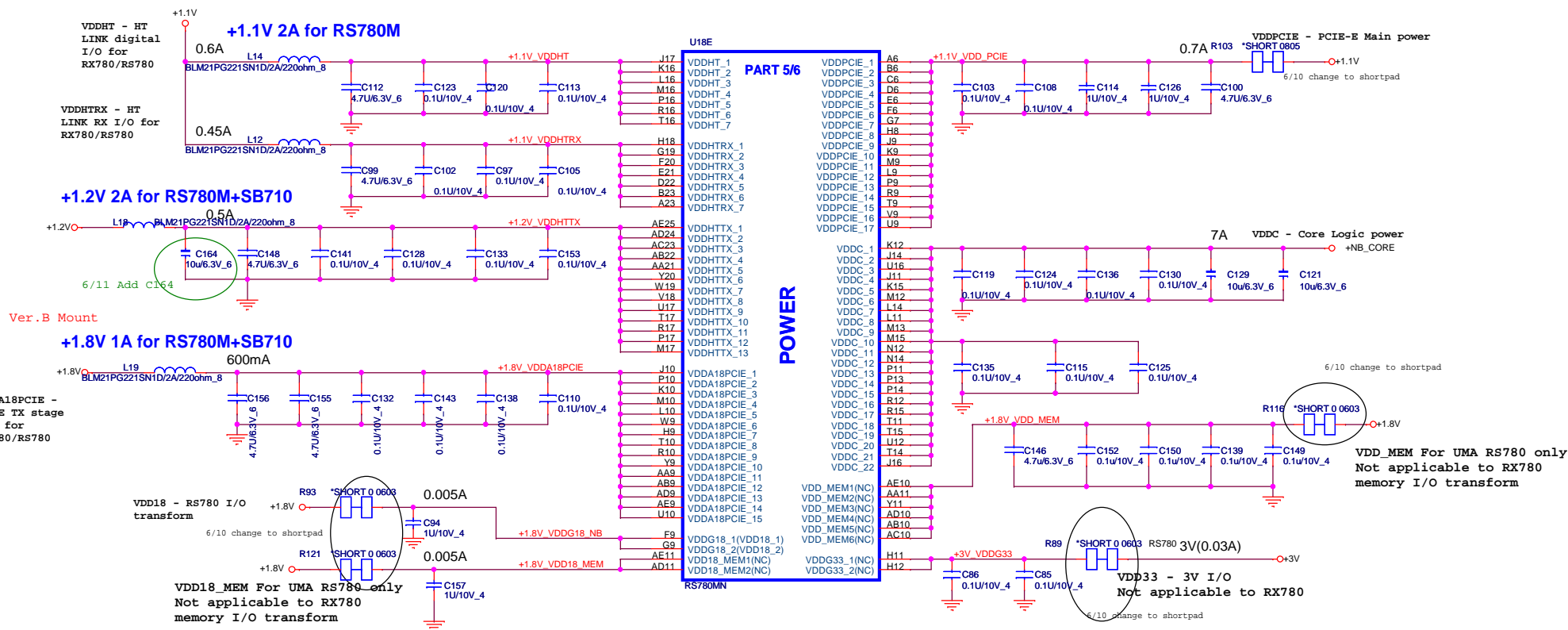
RS780: Powered from the 3.3-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.



The diagram illustrates a complex PCB layout for a 100-pin connector. The layout is organized into several functional blocks, each with its own set of pins and connections. The top and bottom edges of the PCB are labeled '100PIN', indicating the connector pins. The central area of the PCB is divided into sections by dashed lines, representing different functional blocks. The top section is labeled 'VSSAFCIE1' through 'VSSAFCIE10'. The middle section is labeled 'VSSAHT1' through 'VSSAHT12'. The bottom section is labeled 'VSSAFCIE1' through 'VSSAFCIE10'. The right side of the PCB is labeled 'VSSAFCIE1' through 'VSSAFCIE10'. The left side of the PCB is labeled 'VSSAFCIE1' through 'VSSAFCIE10'. The diagram also shows various other components and connections, including a 'GROUND' label and a '100PIN' label.

RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDLTP18	NC	+1.8V
IOPLLVD18	NC	+1.8V	VDDLTP33	NC	NC



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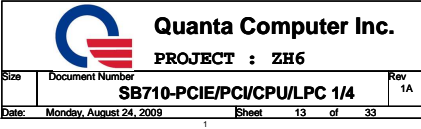
PROJECT : ZH6

RS780MN-POWER 4/4

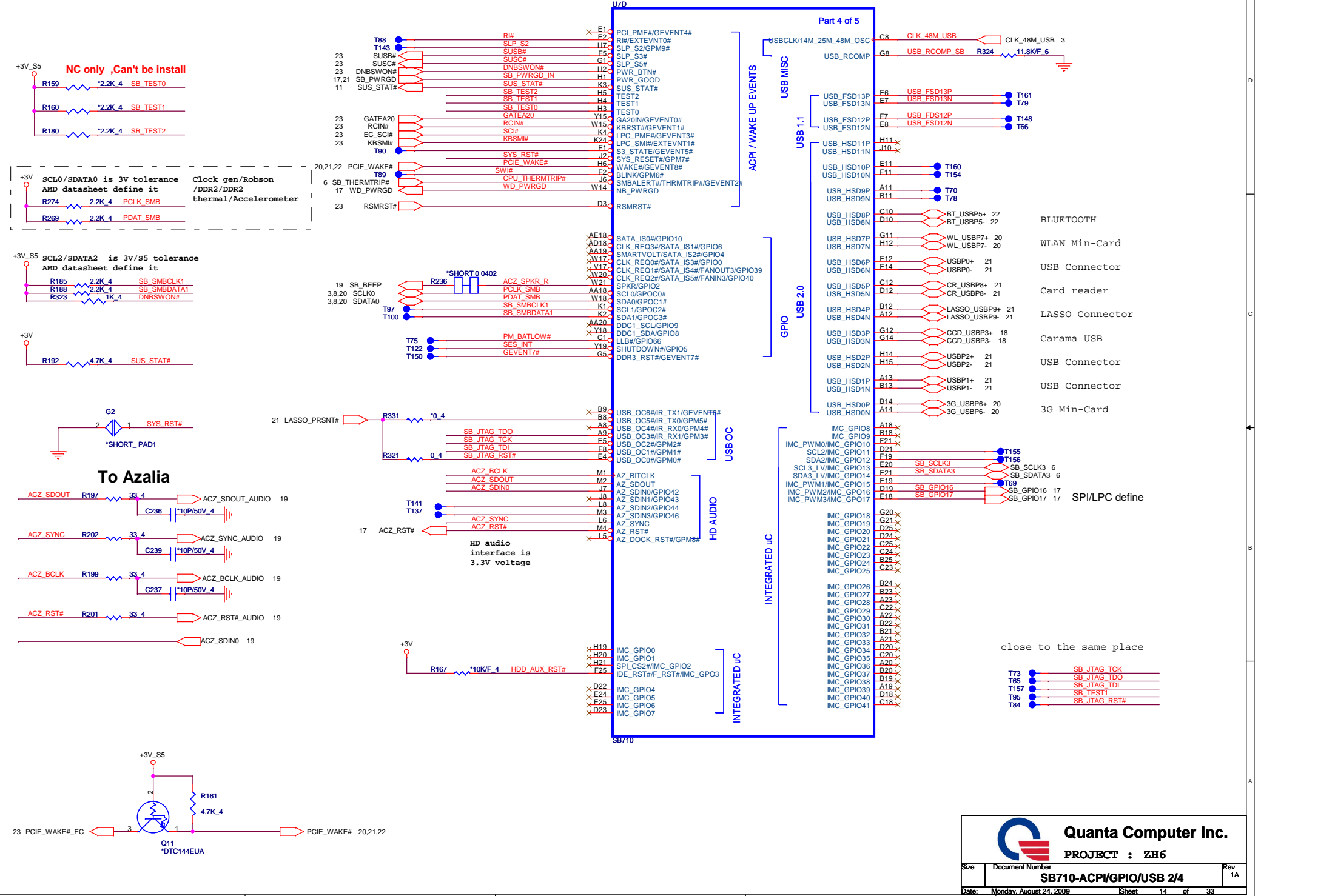
Date: Monday, August 24, 2009 Sheet 12 of 33

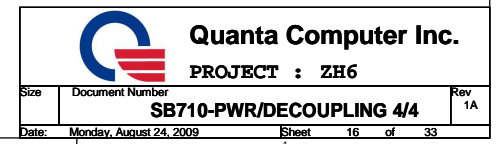
Rev
1A

PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO U600



SB710(GLC)

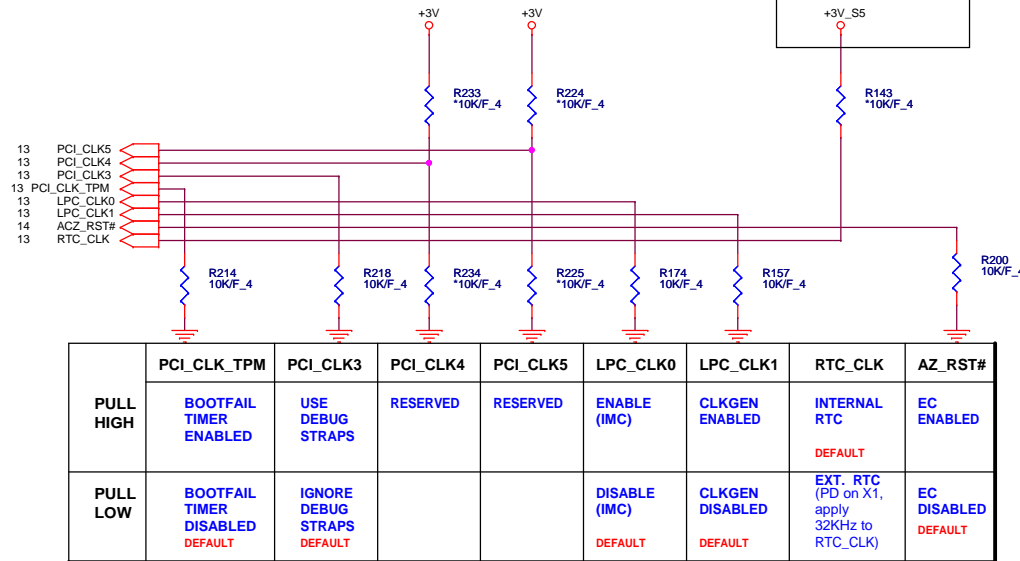




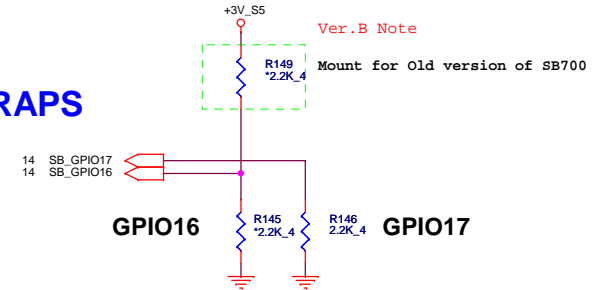


OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

It must ready
before RSMRST#



REQUIRED STRAPS



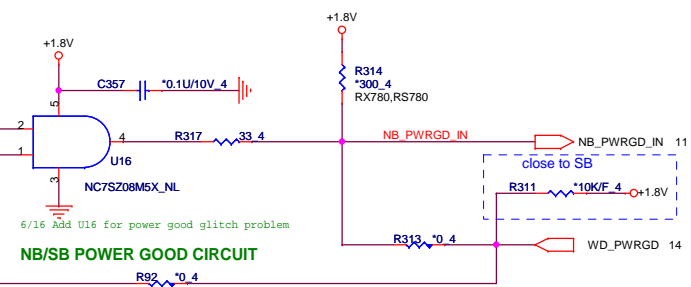
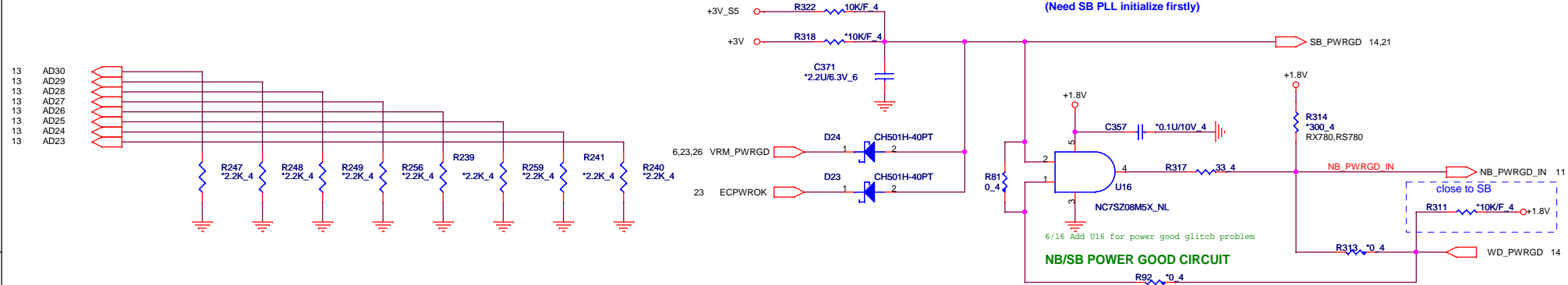
GPIO16 GPIO17

TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

DEBUG STRAPS

SB710 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)

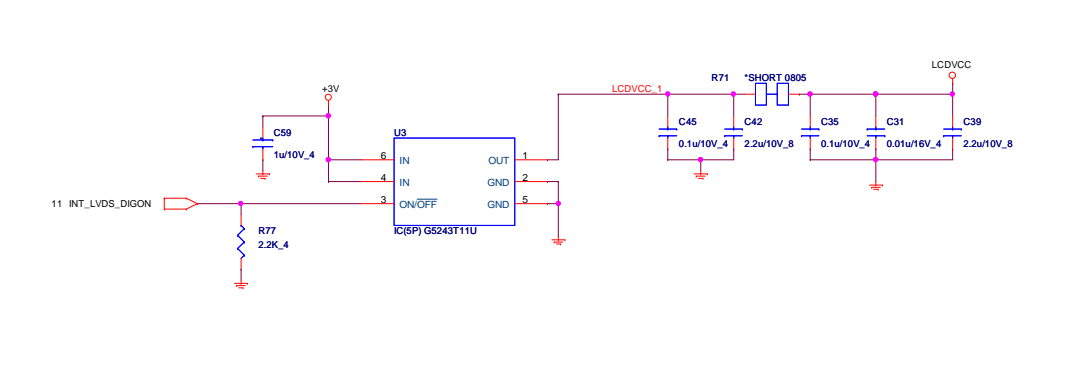


AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

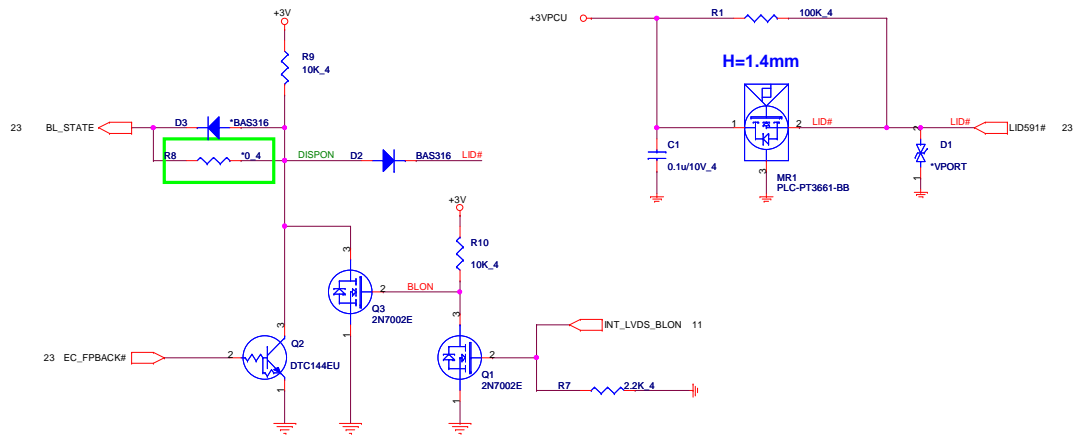


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PROJECT : ZH6

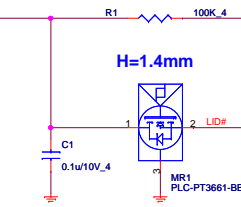
Panel Power(LDS)



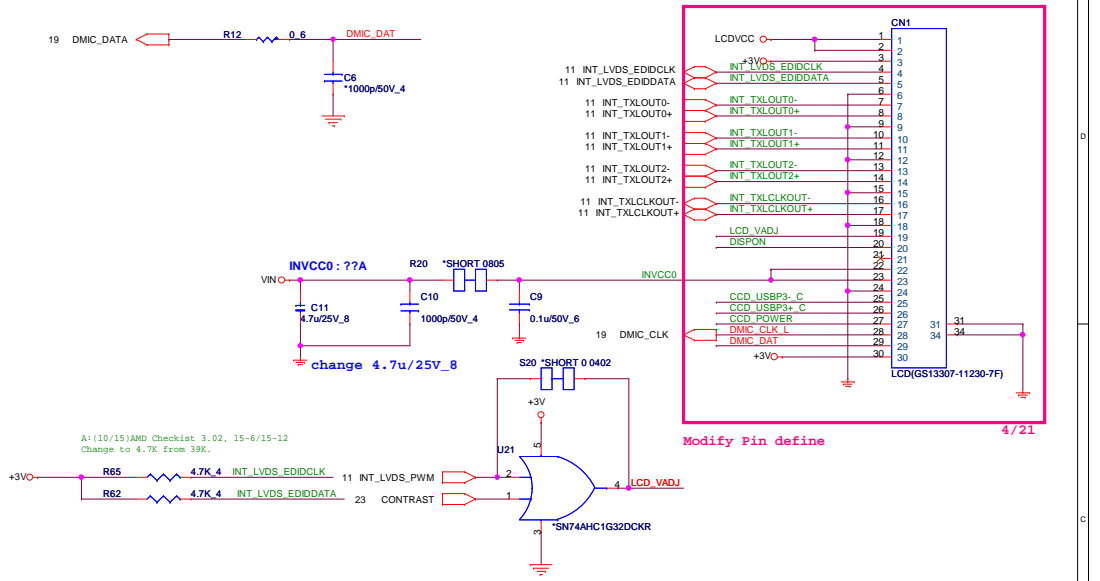
Backlight(LDS)



HALL SENSOR (HSR)



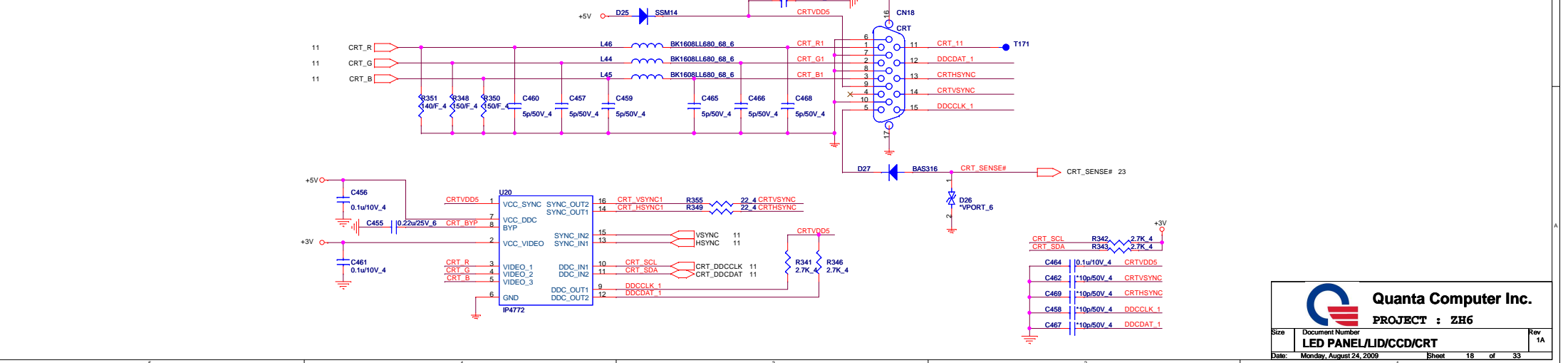
LVDS Connector(LDS)



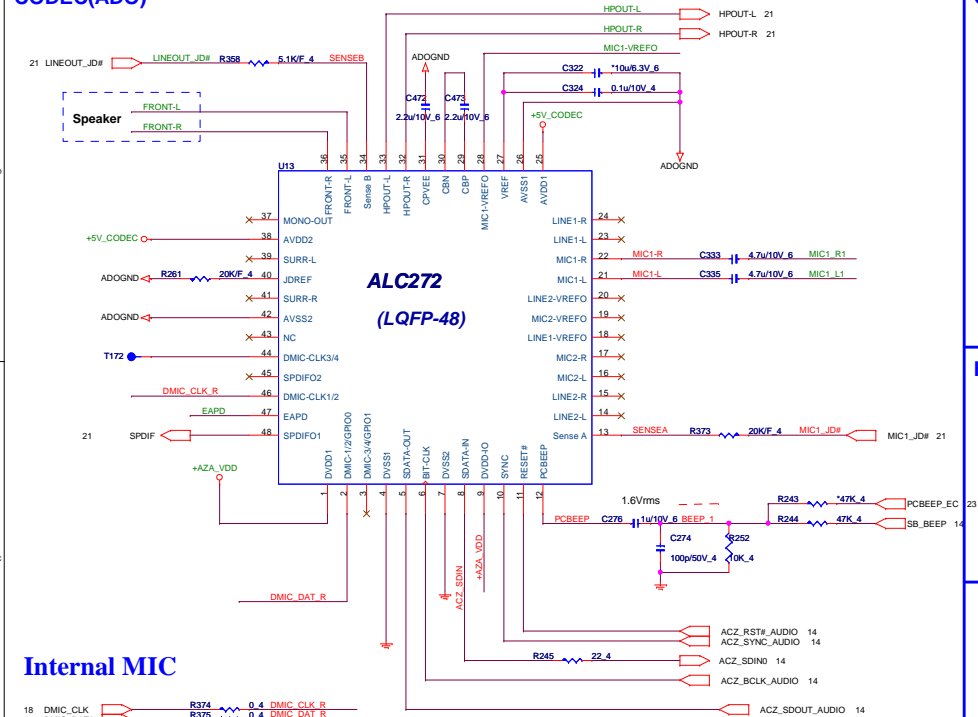
CAMERA Module (CMOS sensor)(CCD)



CRT (CRT)



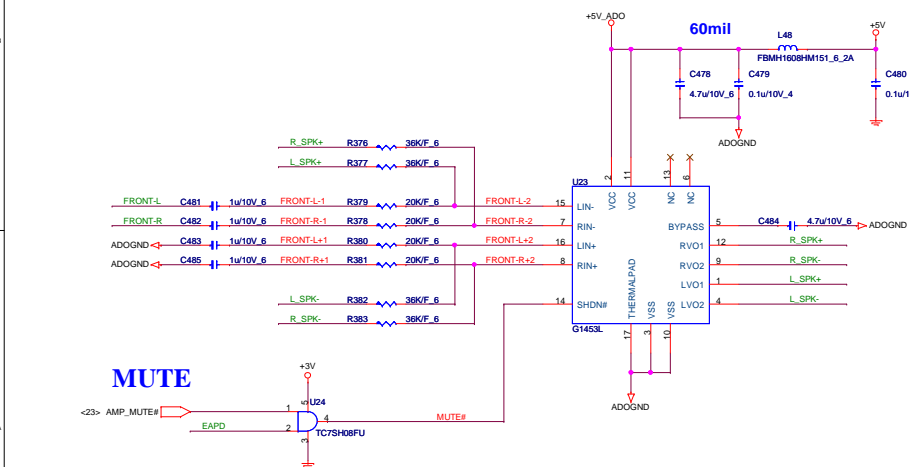
CODEC(ADO)



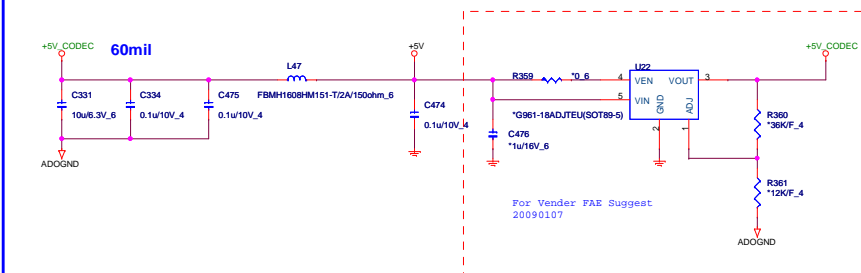
Internal MIC



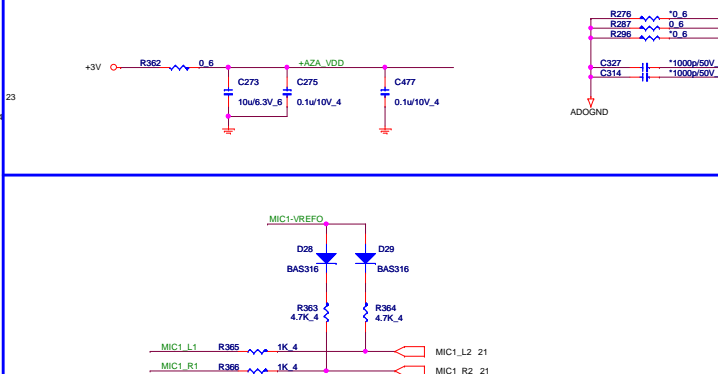
Speaker Amplifier(AMP)



Codec Power(ADO)



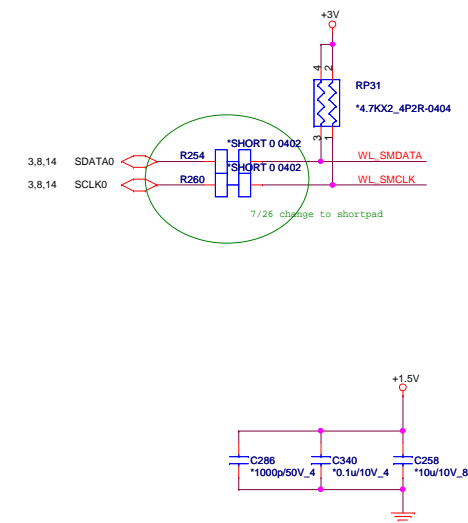
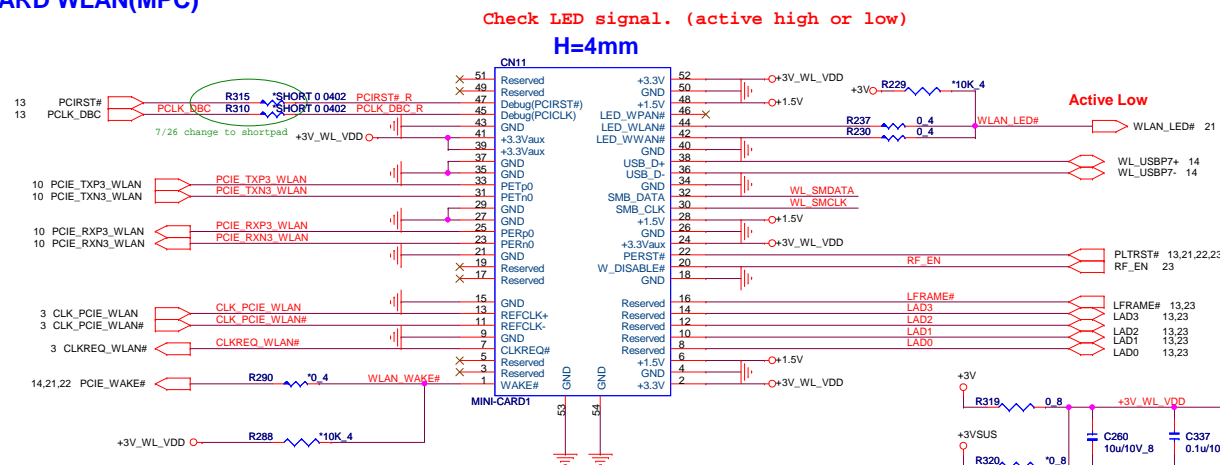
HDA Power(ADO)



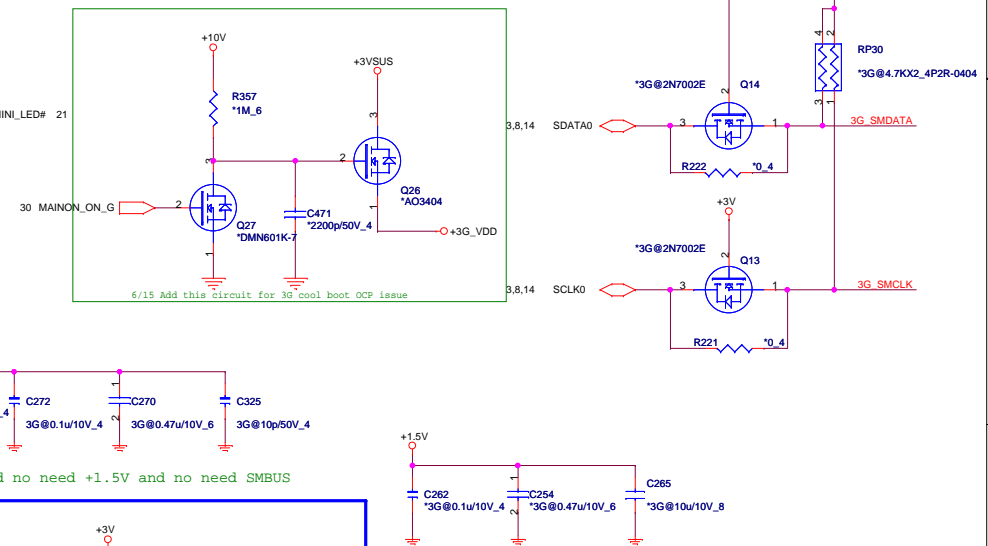
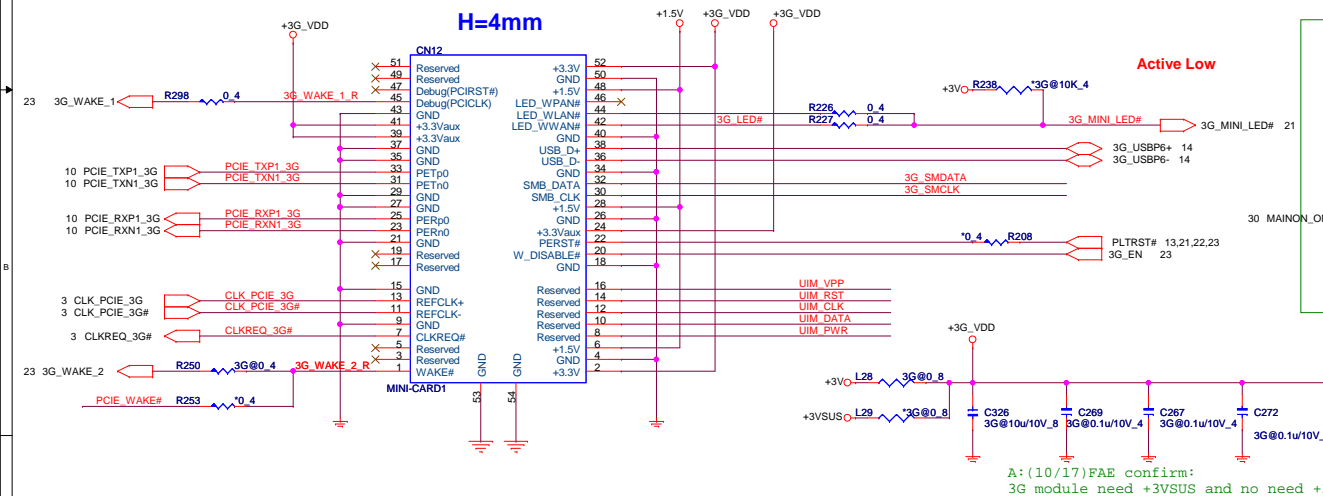
Speaker(AMP)



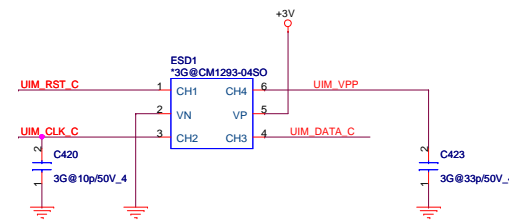
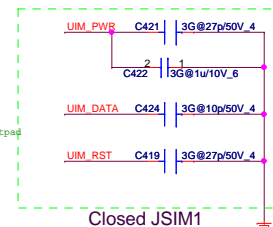
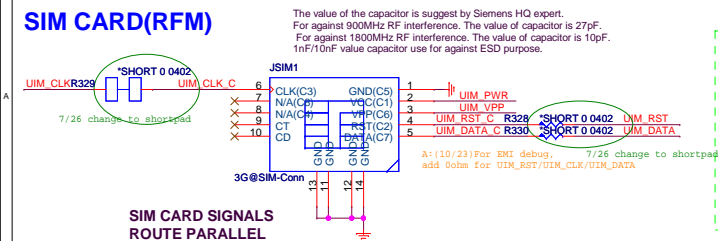
MINI-CARD WLAN(MPC)



MINI-CARD 3G(MNC)

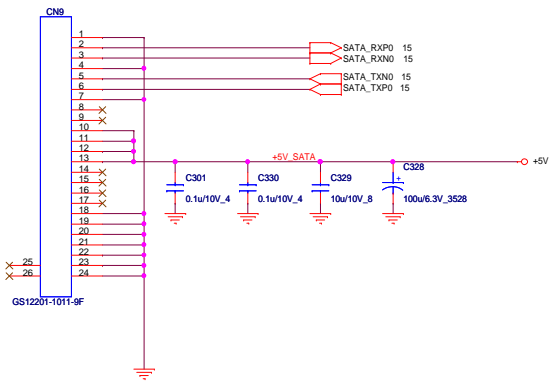


SIM CARD(RFM)



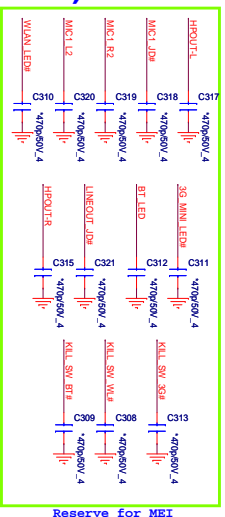
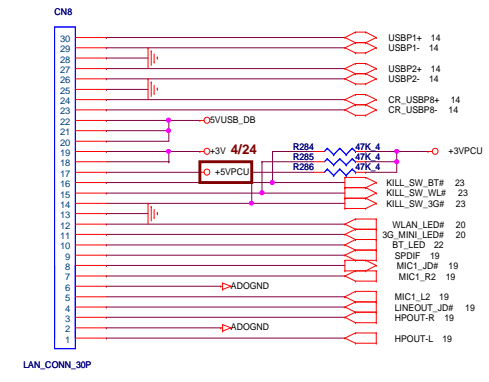
2.5" SATA HDD OR SSD(HDD)

Check SATA HDD in AVL for +3V

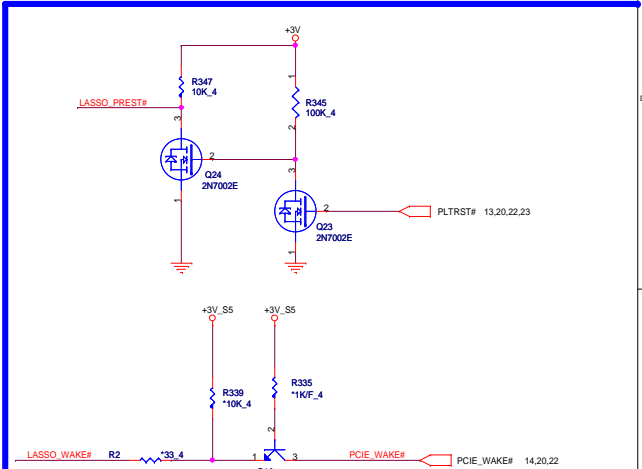


Audio, Cardreader ,Kill SW DB (AMP)

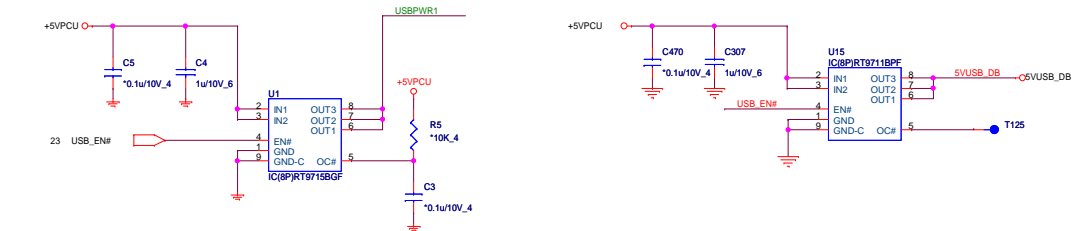
Ipin=0.5A (ACES)



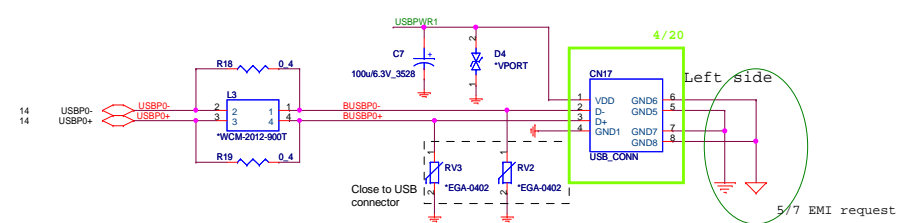
5VUSB_DB	USB_PWR	2A	2A
+3V	Card reader	250mA	275mA



(USB)

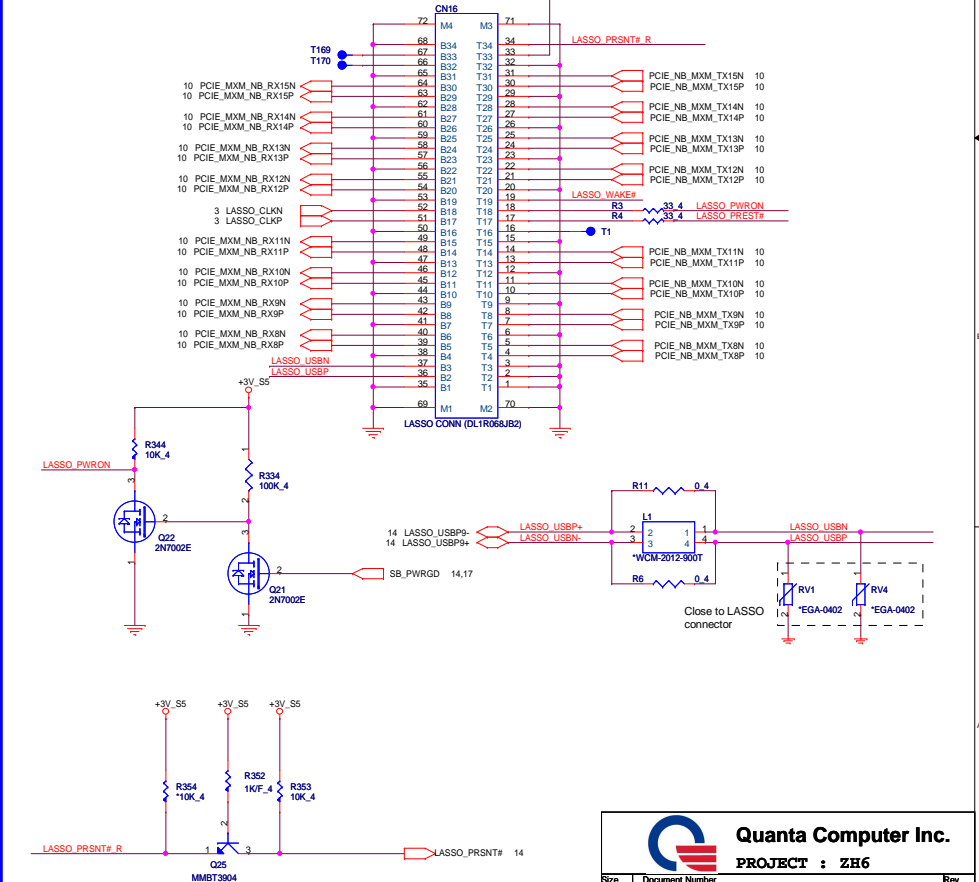


Please reserve Cin = 1uF(stuff),Cout = 10uF(don't stuff) for Richtek RT9711BPFP
Please reserve Cin = 4.7uF(stuff),Cout = 10uF(don't stuff) for GNT solution

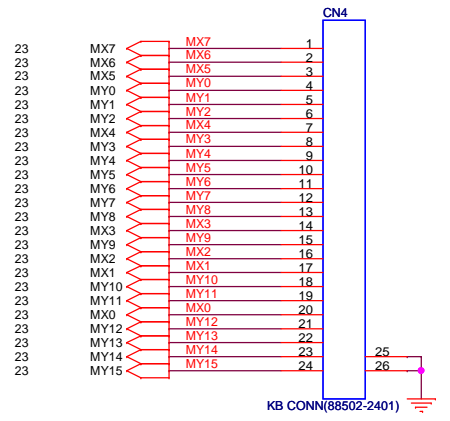


Placed common mode chokes within 1.0" of the USB connectors

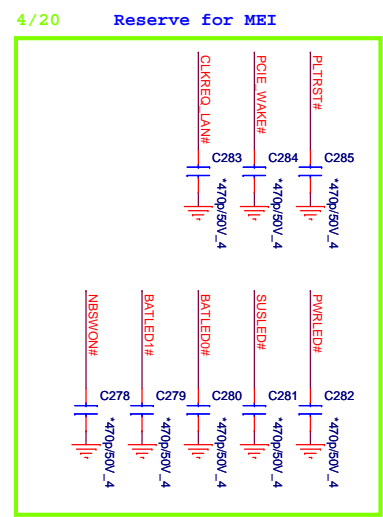
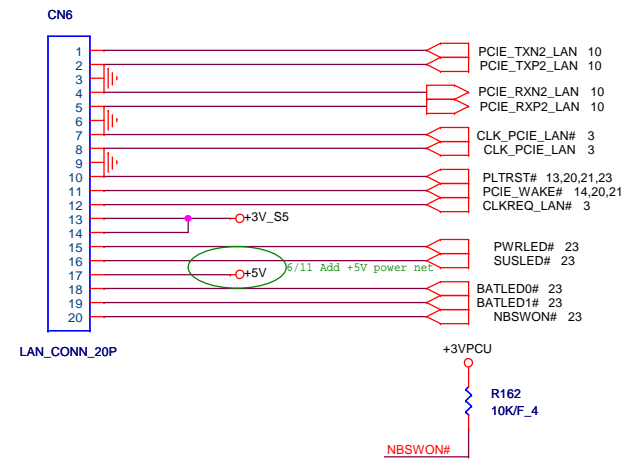
Display Port (DPP)



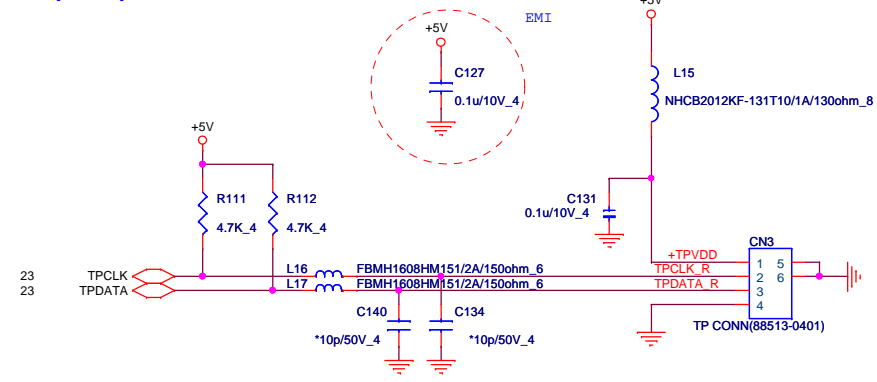
Keyboard(KBC)



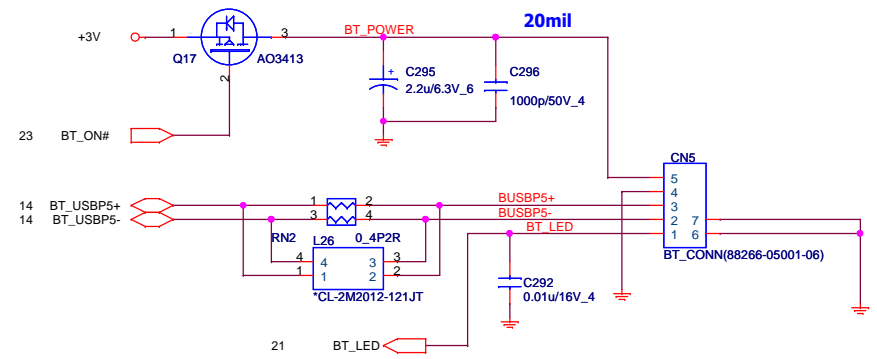
LAN , USBx2 D/B CONNECTER(LAN)



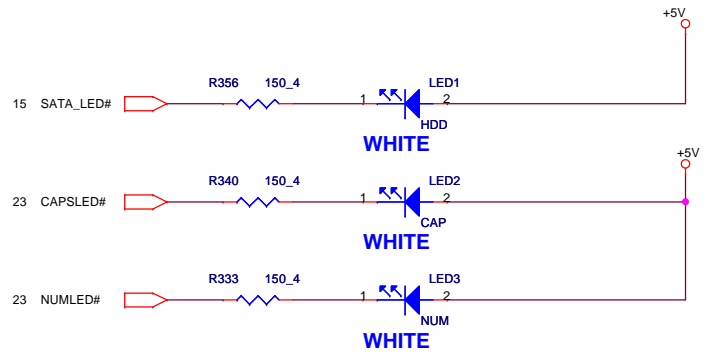
T/P(TPD)




BT(BTM)



LED(UIF)



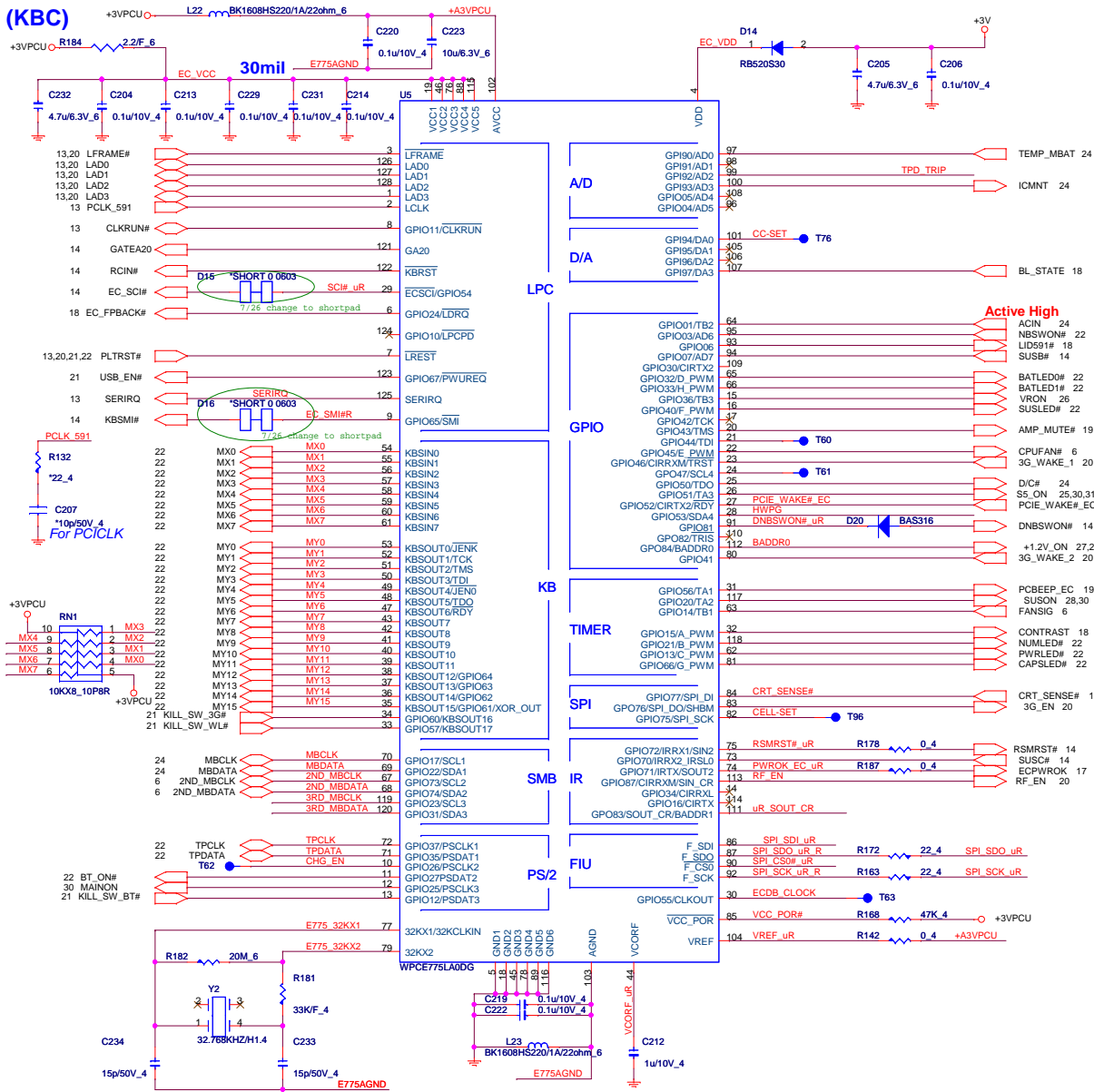


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	TP/ USB/ KB / LED	1A
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(KBC)



I/O ADDRESS SETTING(KBC)

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

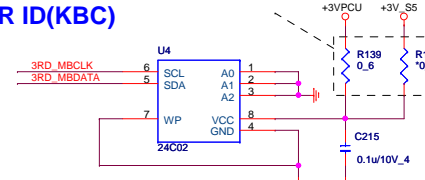


1/13 Confirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

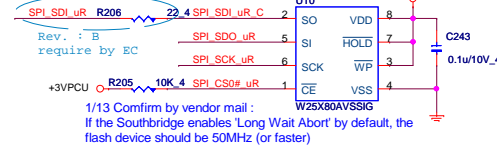
SM BUS PU(KBC)



ACER ID(KBC)

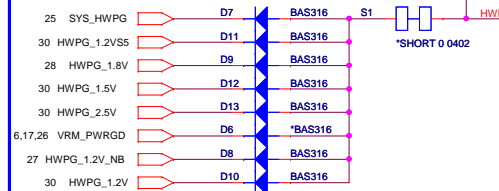


SPI FLASH(KBC)

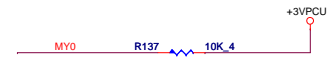


1/13 Confirm by vendor mail : **W25X80AVSSIG**
If the Southbridge enables 'Long Wait Abort' by default, the
flash device should be 50MHz (or faster)

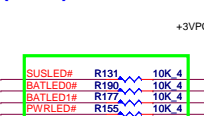
HWPG(KBC)



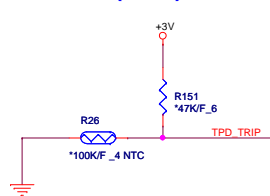
INTERNAL KEYBOARD STRIP SET(KBC)



(KBC)



Thermistor (THM)

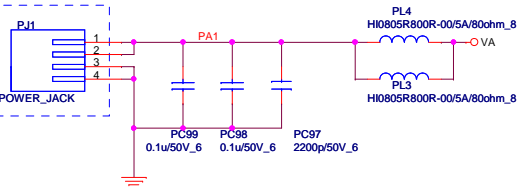


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Size	Document Number WPCE775L & FLASH	Rev 1A
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DC-IN JACK

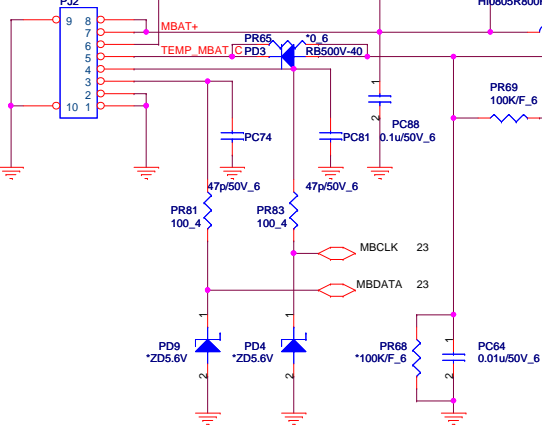
65W Yellow DFPJ05MR007



Change footprint & P/N

ACIN

C114F3-108A1-L_Batt_Conn



Add ESD diode base on EC FAR suggestion

Temp_MBAT_C3

Temp_MBAT_C3

Temp_MBAT_C3

Temp_MBAT_C3

Temp_MBAT_C3

Temp_MBAT_C3

Temp_MBAT_C3

Temp_MBAT_C3

Temp_MBAT_C3

Temp_MBAT_C3

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Temp_MBAT_C3

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Temp_MBAT_C3

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Temp_MBAT_C3

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Temp_MBAT_C3

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Temp_MBAT_C3

Temp_MBAT_C3

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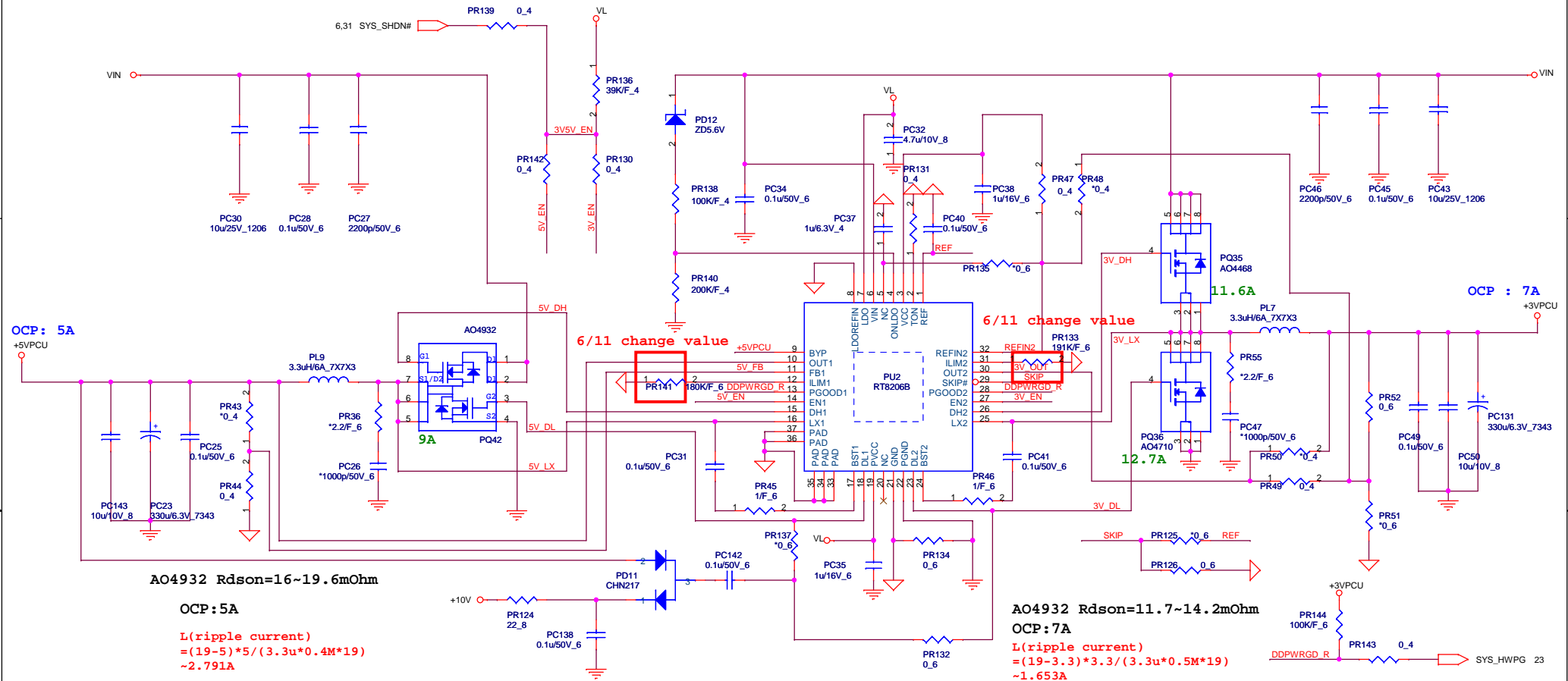
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MAIND 28,30
SUSD 30



AO4932 Rdson=16~19.6mOhm

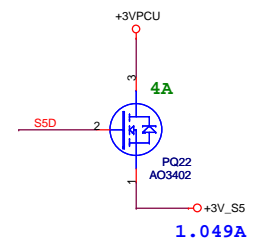
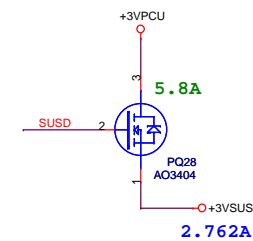
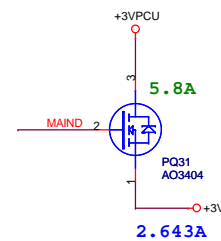
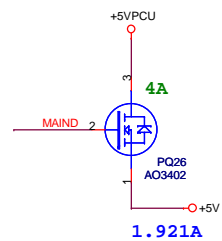
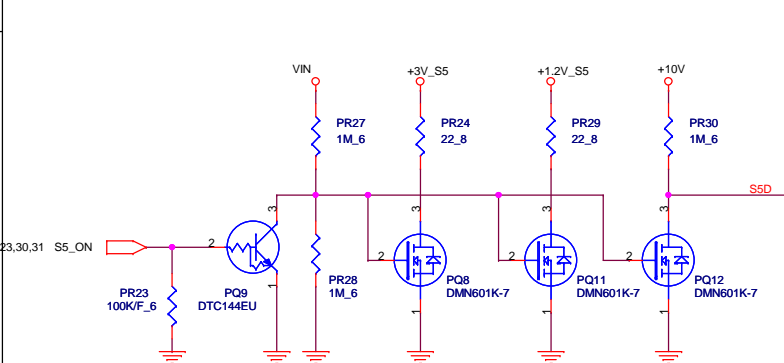
OCP:5A

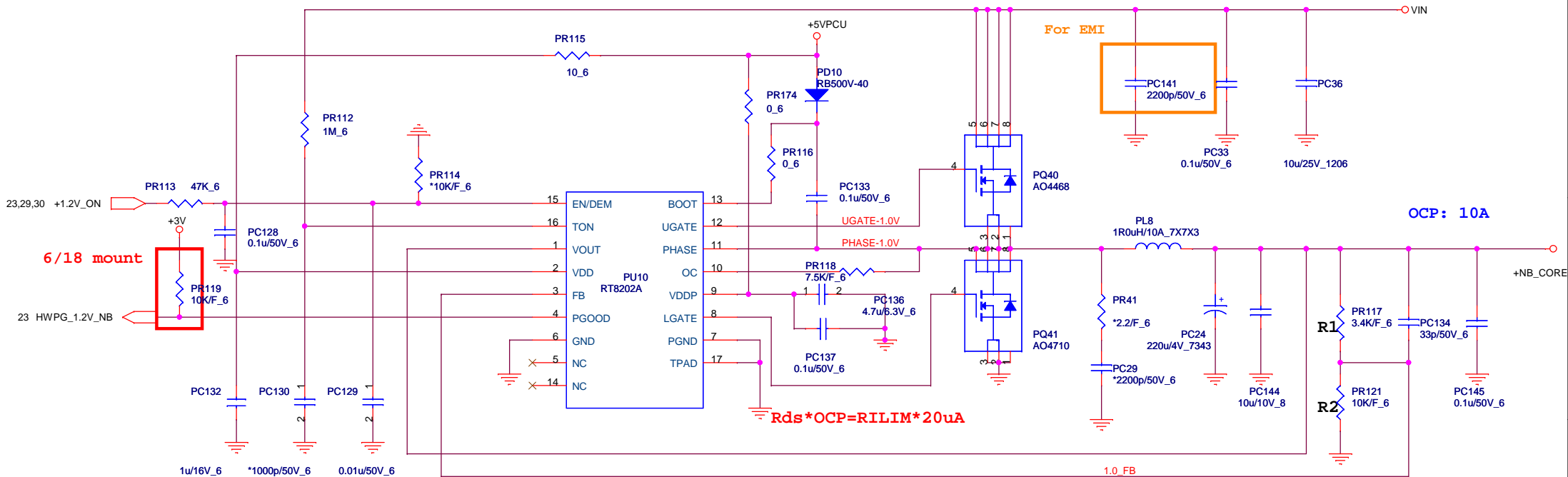
L(ripple current)
 $= (19-5) * 5 / (3.3u * 0.4M * 19)$
 $\sim 2.791A$
 $I_{ocp} = 5 - (2.791 / 2) = 3.6045A$
 $V_{th} = 3.6045A * 14.2mOhm = 70.6482mV$
 $R(I_{lim}) = (70.6482mV * 10) / 5uA$
 $\sim 141K(143K)$

AO4932 Rdson=11.7~14.2mOhm

OCP:7A

L(ripple current)
 $= (19-3.3) * 3.3 / (3.3u * 0.5M * 19)$
 $\sim 1.653A$
 $I_{ocp} = 7 - (1.653 / 2) = 6.1735A$
 $V_{th} = 6.1735A * 14.2mOhm = 87.6637mV$
 $R(I_{lim}) = (87.6637mV * 10) / 5uA$
 $\sim 175K(178K)$





$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin * TON)$$

$$TON = 3.85p * 1M * 1 / (Vin - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

$$AO4710 \text{ Rdson} = 11.7 \sim 14.2m\Omega$$

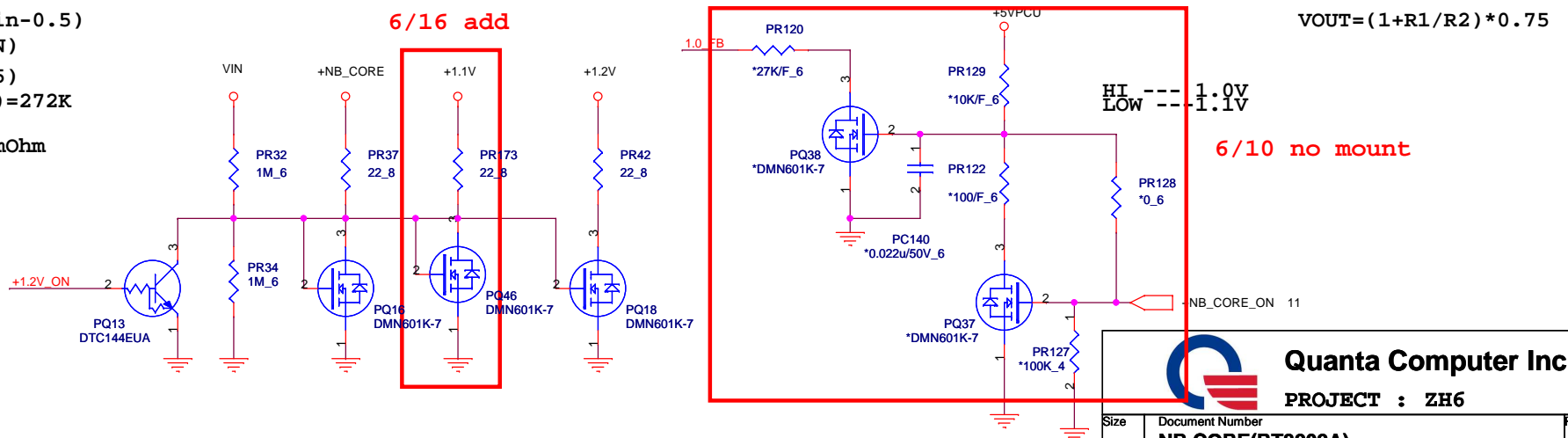
L(ripple current)

$$= (19-1) * 1 / (1u * 272k * 19)$$

$$\sim 3.483A$$

$$14.2m * 10 = RILIM * 20uA$$

$$RILIM = 7.1K (7.5K)$$



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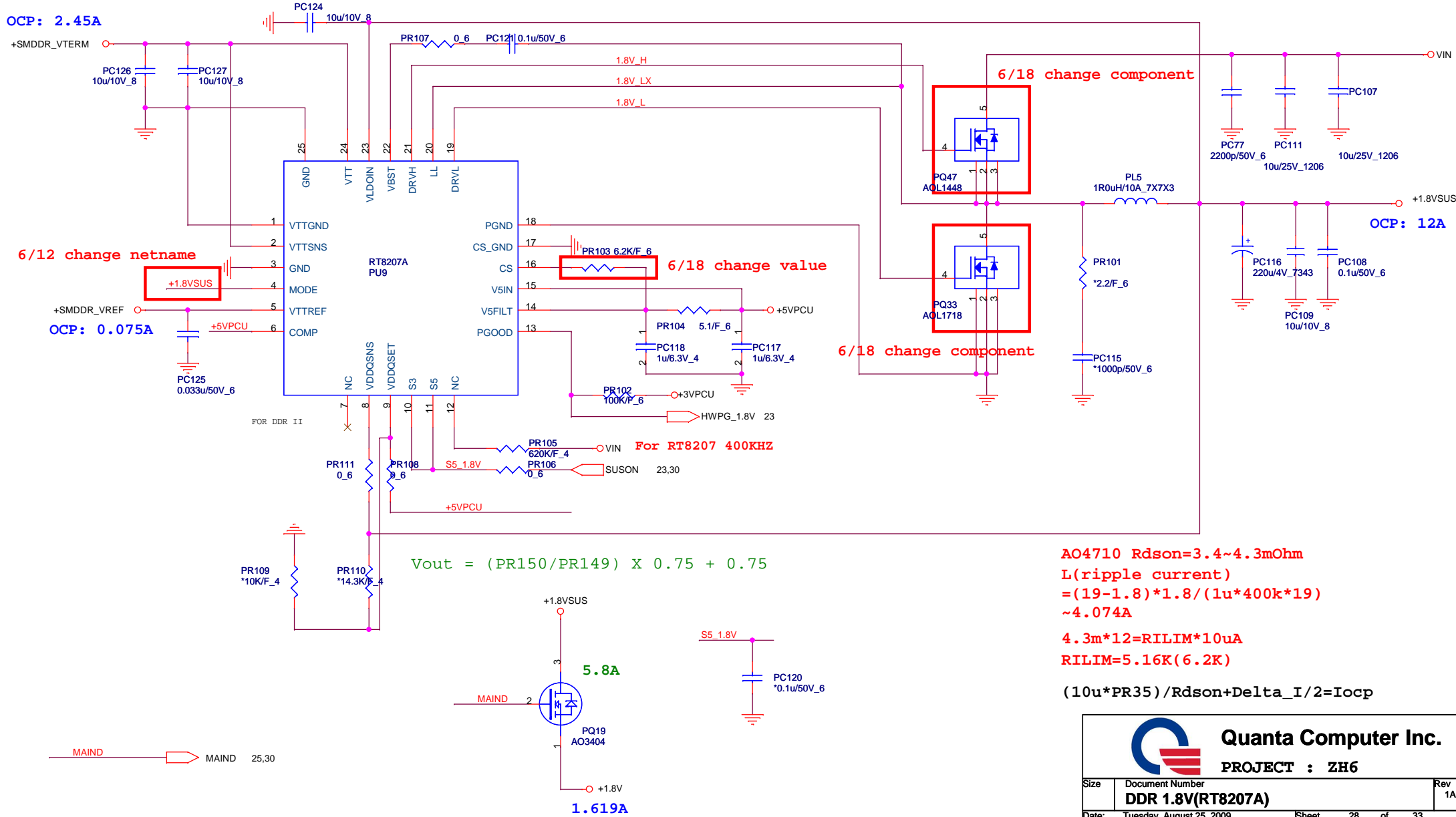
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	NB CORE(RT8202A)	1A
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OCP: 2.45A

6/12 change netname

OCP: 0.075A




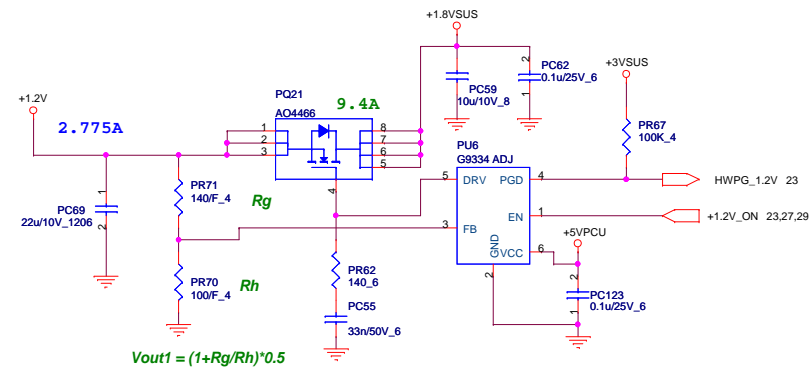
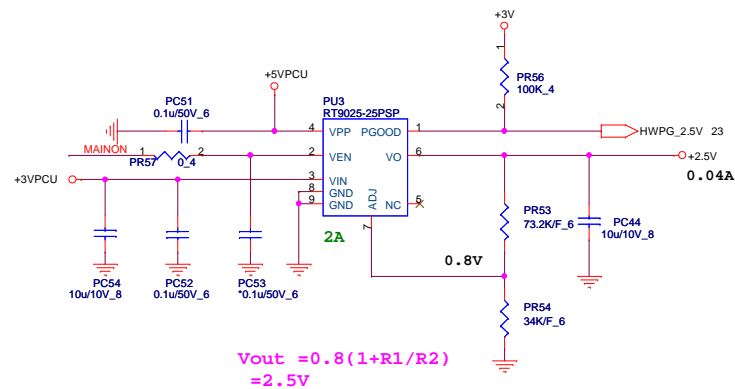
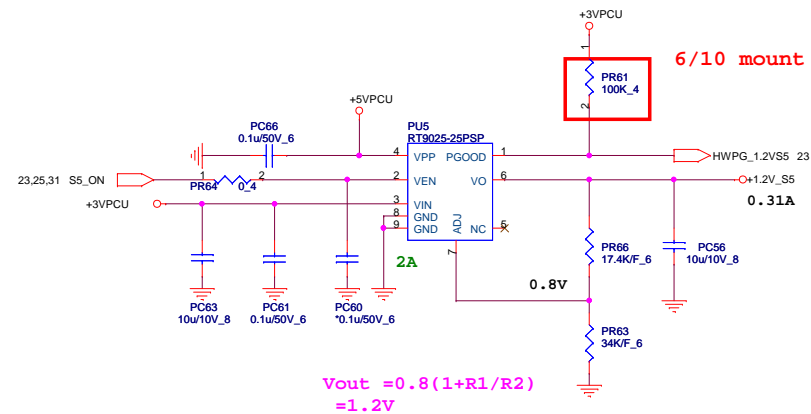
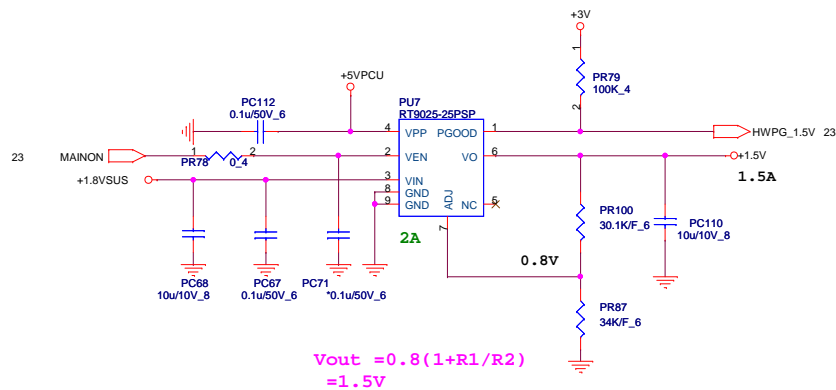
$$V_{out} = (PR150/PR149) \times 0.75 + 0.75$$

AO4710 $R_{dson}=3.4\sim4.3m\Omega$
 $L(\text{ripple current})$
 $= (19-1.8) \times 1.8 / (1\mu \times 400k \times 19)$
 $\sim 4.074A$

$4.3m \times 12 = RILIM \times 10\mu A$
 $RILIM = 5.16K (6.2K)$

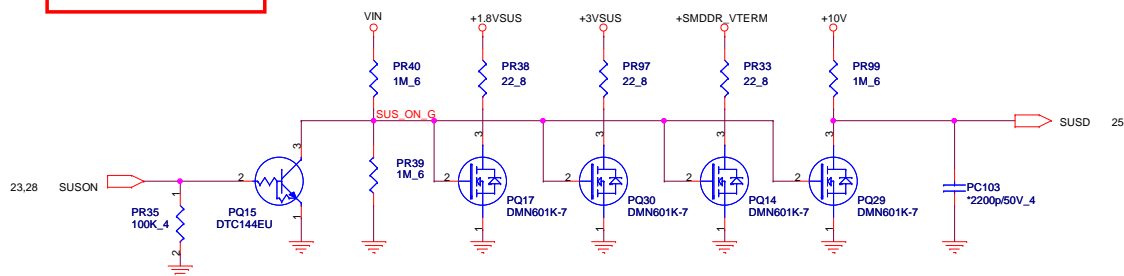
$$(10\mu \times PR35) / R_{dson} + \Delta I / 2 = I_{ocp}$$

 Quanta Computer Inc. PROJECT : ZH6		
Size	Document Number	Rev
	DDR 1.8V(RT8207A)	1A
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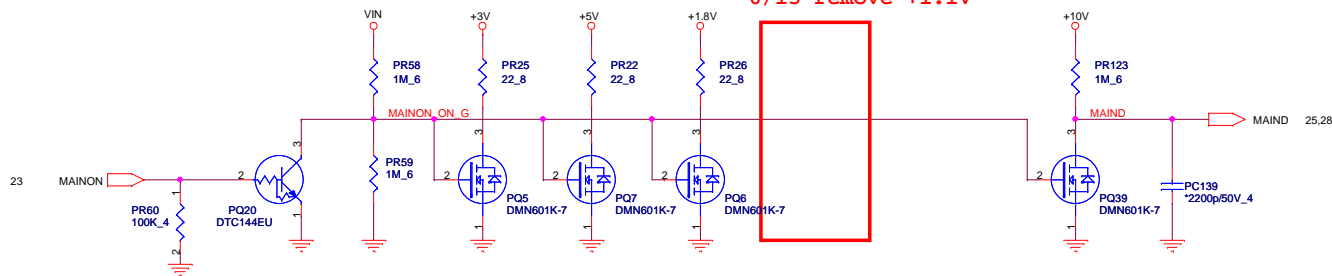


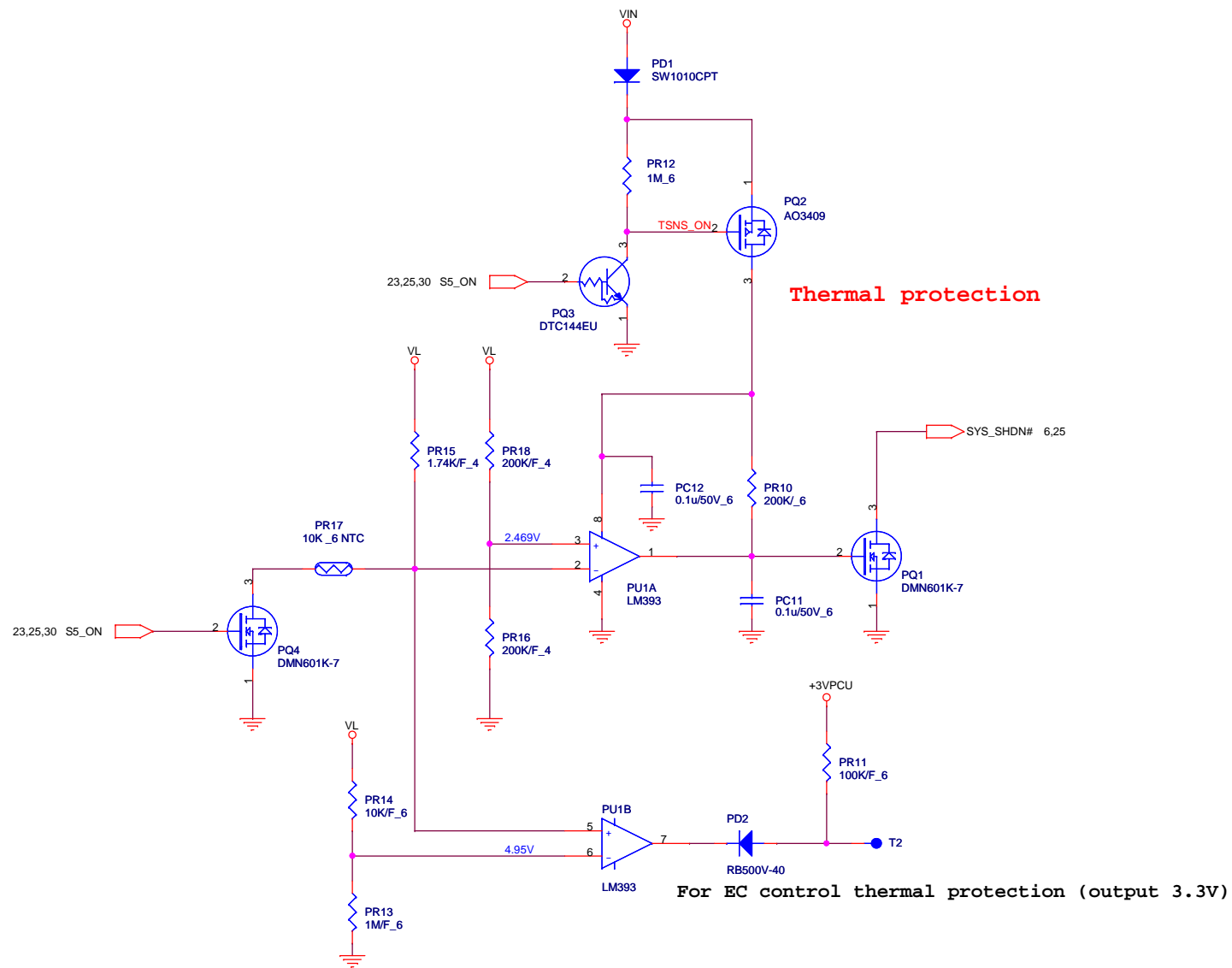
6/18 Add

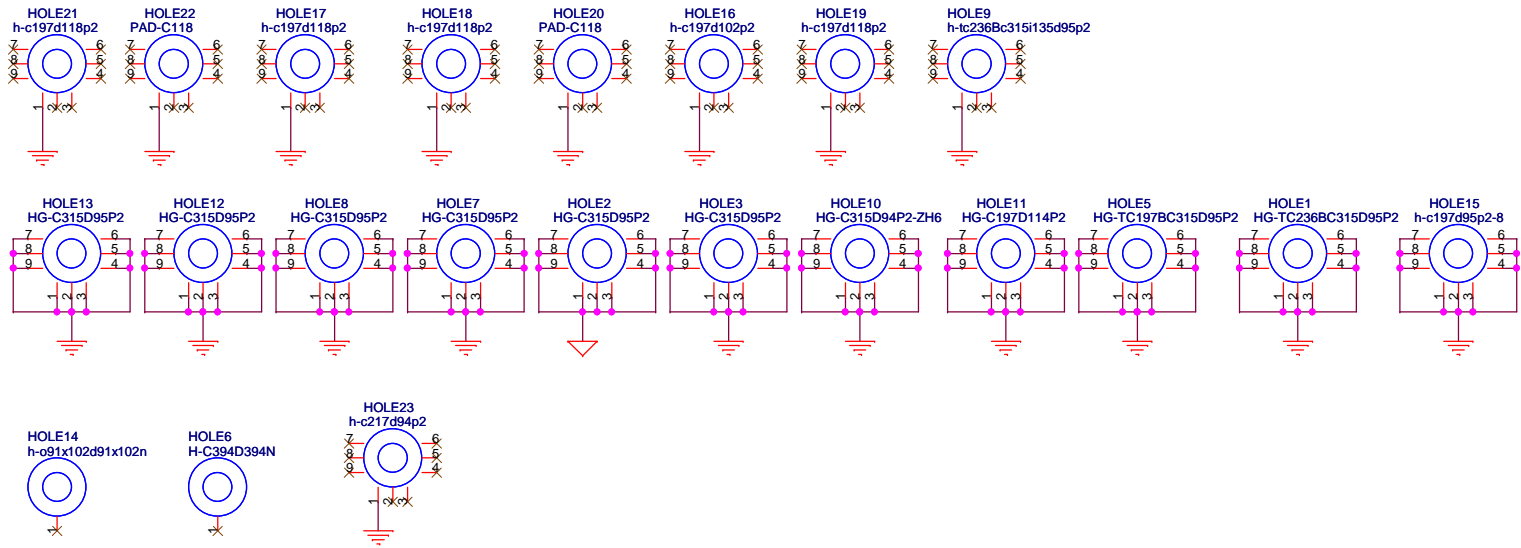
20 MAINON_ON_G



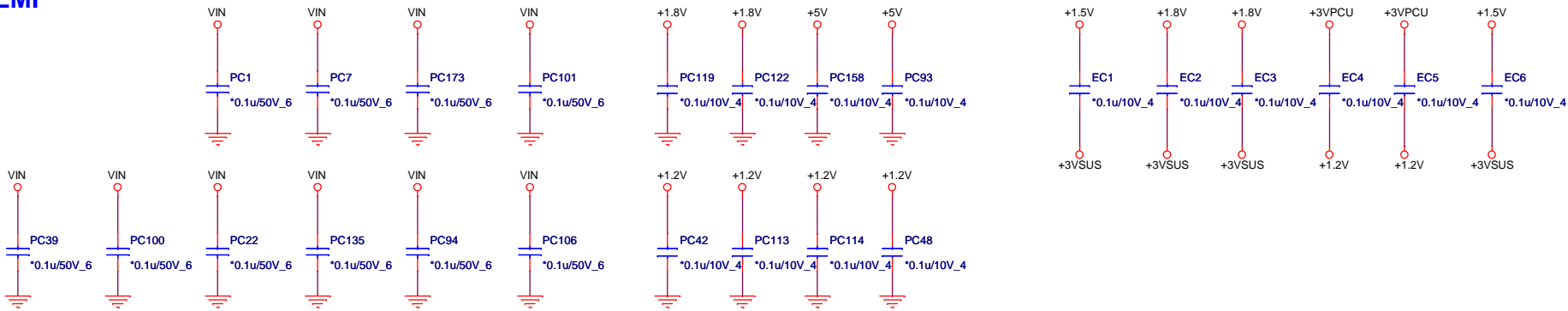
6/15 remove +1.1V







EMI



Quanta Computer Inc.
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	HOLE /EMI	1A
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