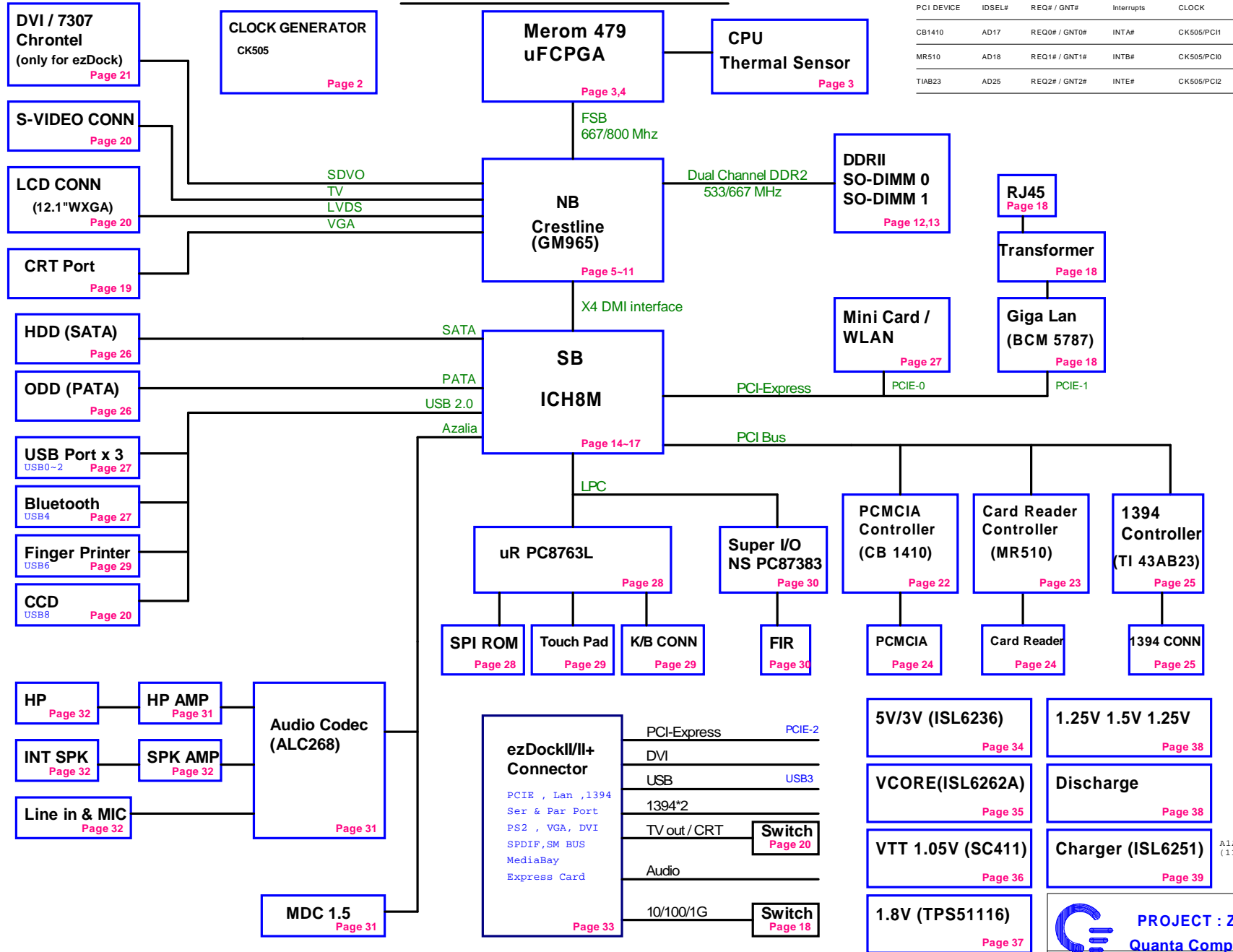
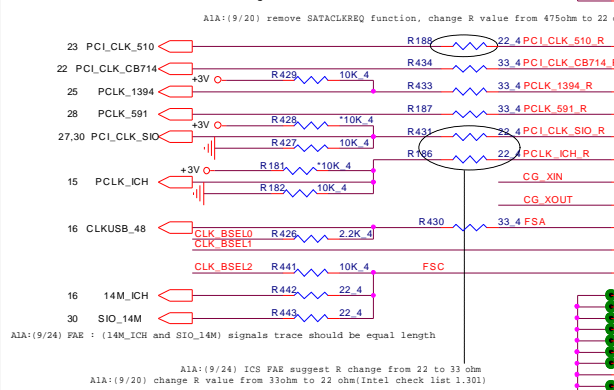


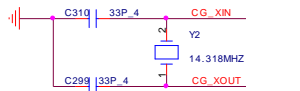
# ZU1 SYSTEM BLOCK DIAGRAM



PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts	CLOCK
CB1410	AD17	REQ0# / GNT0#	INTA#	CK505/PC11
MR510	AD18	REQ1# / GNT1#	INTB#	CK505/PC10
TIAB23	AD25	REQ2# / GNT2#	INTE#	CK505/PC12

[illegible]

AlA:(9/24) ICS FAE suggest R change from 22 to 33 ohm  
AlA:(9/20) change R value from 33ohm to 22 ohm(Intel check list 1.301)

[illegible]

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

Pin	Active	Control signal
32	Low	SRC9/9#
33	Low	SRC10/10#

A circuit diagram showing a +3V supply connected to a resistor R184 (10K 4) which is then connected to the PCIE CLKREQ# pin.

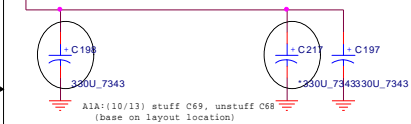
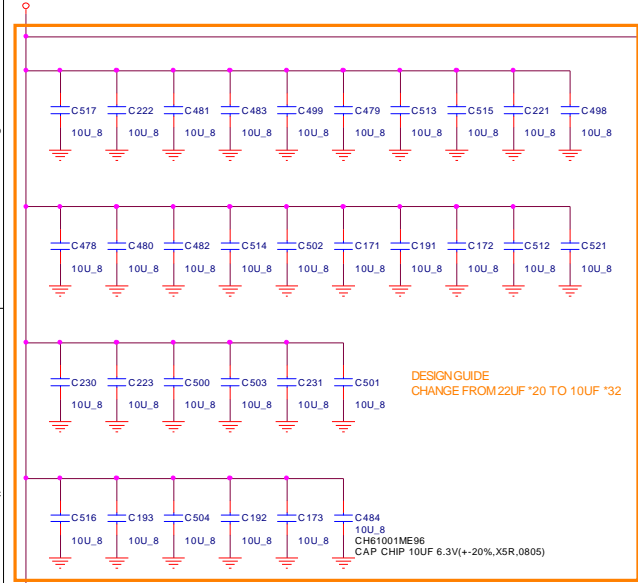
```
A1A:(9/24) Add PCIE_CLKREQ# PU to +3V
```

The schematic shows a power supply rail labeled VDD\_10V\_8. A series of capacitors are connected to this rail: C320 (10U\_8), C309 (10U\_8), C300 (10U\_8), C301 (10U\_8), C316 (1U\_4), C314 (1U\_4), C317 (1U\_4), C290 (1U\_4), C315 (1U\_4), C291 (1U\_4), and C298 (1U\_4). Following these capacitors, there is a common-mode filter L26 (BKP1608HS181-T.6) connected to ground. A note indicates "0.1U close to each VDD\_IO Power pin".

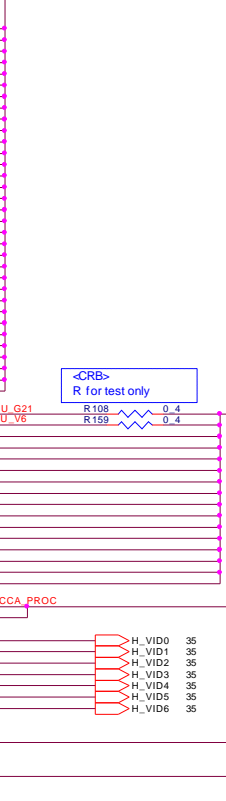
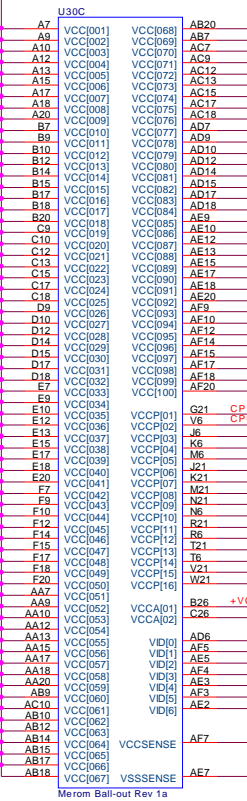


# CPU(Power)

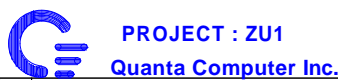
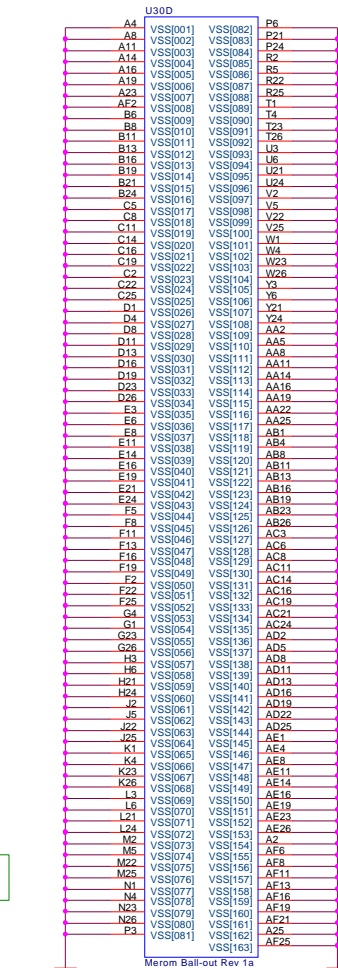
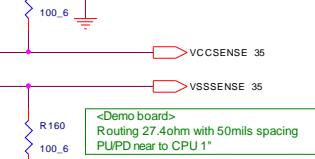
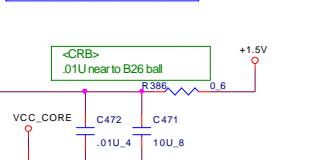
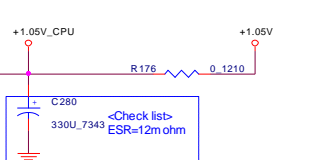
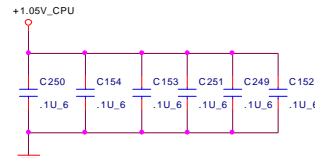
VCC\_CORE



<Check list>  
Option1:330U\*6(ESR=1.5m ohm aggregate , ESL=0.8nH/6) and 22U\*20(ESR=3mohm typ/20 , ESL=0.6nH/20)  
Option2:330U\*6(ESR=1.5m ohm aggregate , ESL=1.8nH/6) and 22U\*32(ESR=3mohm typ/32 , ESL=0.6nH/32)



<REV.NO.0.5/REF.NO.19343>  
Ivcc Max 52A  
Ivccp Max 6A(VCCP supply before Vcc stable)  
Max 2A(VCCP supply after Vcc stable)  
Ivcca Max 130mA



# NB(HOST)

+1.05V\_GMCH

R86  
221.4

H\_SWING

R85  
100.4

C137  
.1U\_4

<check list>  
0.1U close to B3

H\_RCOMP

R95  
24.9\_4

<check list>  
10:20 mils(Width:Spacing)

+1.05V\_GMCH

R87  
54.9\_4

H\_SCOMP

<check list>  
Impedance 55ohm

+1.05V\_GMCH

R88  
54.9\_4

H\_SCOMP#

<check list>  
Impedance 55ohm

+1.05V\_GMCH

R392  
1K\_4

H\_CPURST#  
H\_CPUSLP#

R391  
2K\_4

C473  
.1U\_4

<check list>  
0.1U close to B9

H\_SWING B3  
H\_RCOMP C2

H\_SCOMP W1  
H\_SCOMP# W2

B6 H\_CPURST#  
E5 H\_CPUSLP#

B9 H\_AVREF  
A9 H\_DVREF

CRESTLINE\_1p0

U29A

H\_D#0 E2 H\_D#\_0  
H\_D#1 G2 H\_D#\_1  
H\_D#2 G7 H\_D#\_2  
H\_D#3 M6 H\_D#\_3  
H\_D#4 H7 H\_D#\_4  
H\_D#5 H3 H\_D#\_5  
H\_D#6 G4 H\_D#\_6  
H\_D#7 F3 H\_D#\_7  
H\_D#8 N8 H\_D#\_8  
H\_D#9 H2 H\_D#\_9  
H\_D#10 M10 H\_D#\_10  
H\_D#11 N12 H\_D#\_11  
H\_D#12 N9 H\_D#\_12  
H\_D#13 H5 H\_D#\_13  
H\_D#14 P13 H\_D#\_14  
H\_D#15 K9 H\_D#\_15  
H\_D#16 M2 H\_D#\_16  
H\_D#17 W10 H\_D#\_17  
H\_D#18 Y8 H\_D#\_18  
H\_D#19 V4 H\_D#\_19  
H\_D#20 M3 H\_D#\_20  
H\_D#21 J1 H\_D#\_21  
H\_D#22 N5 H\_D#\_22  
H\_D#23 N3 H\_D#\_23  
H\_D#24 W6 H\_D#\_24  
H\_D#25 W9 H\_D#\_25  
H\_D#26 Y2 H\_D#\_26  
H\_D#27 Y7 H\_D#\_27  
H\_D#28 Y9 H\_D#\_28  
H\_D#29 P4 H\_D#\_29  
H\_D#30 W3 H\_D#\_30  
H\_D#31 N1 H\_D#\_31  
H\_D#32 AD12 H\_D#\_32  
H\_D#33 AE3 H\_D#\_33  
H\_D#34 AD9 H\_D#\_34  
H\_D#35 AC9 H\_D#\_35  
H\_D#36 AC7 H\_D#\_36  
H\_D#37 AC14 H\_D#\_37  
H\_D#38 AD11 H\_D#\_38  
H\_D#39 AC11 H\_D#\_39  
H\_D#40 AB2 H\_D#\_40  
H\_D#41 AD7 H\_D#\_41  
H\_D#42 AB1 H\_D#\_42  
H\_D#43 Y3 H\_D#\_43  
H\_D#44 AC6 H\_D#\_44  
H\_D#45 AE2 H\_D#\_45  
H\_D#46 AC5 H\_D#\_46  
H\_D#47 AG3 H\_D#\_47  
H\_D#48 AJ9 H\_D#\_48  
H\_D#49 AH8 H\_D#\_49  
H\_D#50 AJ14 H\_D#\_50  
H\_D#51 AE9 H\_D#\_51  
H\_D#52 AE11 H\_D#\_52  
H\_D#53 AH12 H\_D#\_53  
H\_D#54 AJ5 H\_D#\_54  
H\_D#55 AE6 H\_D#\_55  
H\_D#56 AJ6 H\_D#\_56  
H\_D#57 AE7 H\_D#\_57  
H\_D#58 AJ7 H\_D#\_58  
H\_D#59 AJ2 H\_D#\_59  
H\_D#60 AE5 H\_D#\_60  
H\_D#61 AJ3 H\_D#\_61  
H\_D#62 AH2 H\_D#\_62  
H\_D#63 AH13 H\_D#\_63

HOST

H\_A#\_3  
H\_A#\_4  
H\_A#\_5  
H\_A#\_6  
H\_A#\_7  
H\_A#\_8  
H\_A#\_9  
H\_A#\_10  
H\_A#\_11  
H\_A#\_12  
H\_A#\_13  
H\_A#\_14  
H\_A#\_15  
H\_A#\_16  
H\_A#\_17  
H\_A#\_18  
H\_A#\_19  
H\_A#\_20  
H\_A#\_21  
H\_A#\_22  
H\_A#\_23  
H\_A#\_24  
H\_A#\_25  
H\_A#\_26  
H\_A#\_27  
H\_A#\_28  
H\_A#\_29  
H\_A#\_30  
H\_A#\_31  
H\_A#\_32  
H\_A#\_33  
H\_A#\_34  
H\_A#\_35

J13 H\_A#3  
B11 H\_A#4  
C11 H\_A#5  
M11 H\_A#6  
C15 H\_A#7  
F16 H\_A#8  
L13 H\_A#9  
G17 H\_A#10  
C14 H\_A#11  
K16 H\_A#12  
B13 H\_A#13  
L16 H\_A#14  
J17 H\_A#15  
B14 H\_A#16  
K19 H\_A#17  
P15 H\_A#18  
R17 H\_A#19  
B16 H\_A#20  
H20 H\_A#21  
L19 H\_A#22  
D17 H\_A#23  
M17 H\_A#24  
N16 H\_A#25  
J19 H\_A#26  
B18 H\_A#27  
E19 H\_A#28  
B17 H\_A#29  
B15 H\_A#30  
E17 H\_A#31  
C18 H\_A#32  
A19 H\_A#33  
B19 H\_A#34  
N19 H\_A#35

H\_A#[35:32] are not supported in  
Calero Interposer  
Crestline support 36 bit address

H\_ADS#  
H\_ADSTB#\_0  
H\_ADSTB#\_1  
H\_BNR#  
H\_BPRI#  
H\_BREQ#  
H\_DEFER#  
H\_DBSY#  
HPLL\_CLK  
H\_DPWR#  
H\_DRDY#  
H\_HIT#  
H\_HITM#  
H\_LOCK#  
H\_TRDY#

G12 H\_ADS# 3  
H17 H\_ADSTB0# 3  
G20 H\_ADSTB1# 3  
C8 H\_BNR# 3  
F8 H\_BPRI# 3  
F12 H\_BREQ# 3  
D6 H\_DEFER# 3  
C10 H\_DBSY# 3  
AM5 CLK\_MCH\_BCLK 2  
AM7 CLK\_MCH\_BCLK# 2  
H8 H\_DPWR# 3  
K7 H\_DRDY# 3  
E4 H\_HIT# 3  
C6 H\_HITM# 3  
G10 H\_LOCK# 3  
B7 H\_TRDY# 3

H\_DINV#\_0  
H\_DINV#\_1  
H\_DINV#\_2  
H\_DINV#\_3

K5 H\_DINV#0  
L2 H\_DINV#1  
AD13 H\_DINV#2  
AE13 H\_DINV#3

H\_DSTBN#\_0  
H\_DSTBN#\_1  
H\_DSTBN#\_2  
H\_DSTBN#\_3

M7 H\_DSTBN#0  
K3 H\_DSTBN#1  
AD2 H\_DSTBN#2  
AH11 H\_DSTBN#3

H\_DSTBP#\_0  
H\_DSTBP#\_1  
H\_DSTBP#\_2  
H\_DSTBP#\_3

L7 H\_DSTBP#0  
K2 H\_DSTBP#1  
AC2 H\_DSTBP#2  
AJ10 H\_DSTBP#3

H\_REQ#\_0  
H\_REQ#\_1  
H\_REQ#\_2  
H\_REQ#\_3  
H\_REQ#\_4

M14 H\_REQ#0  
E13 H\_REQ#1  
A11 H\_REQ#2  
H13 H\_REQ#3  
B12 H\_REQ#4

H\_RS#\_0  
H\_RS#\_1  
H\_RS#\_2

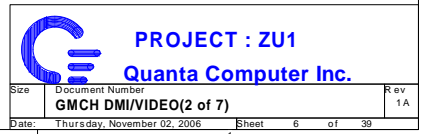
E12 H\_RS#0  
D7 H\_RS#1  
D8 H\_RS#2

A1A: (9/20) remove R74 (0 ohm)



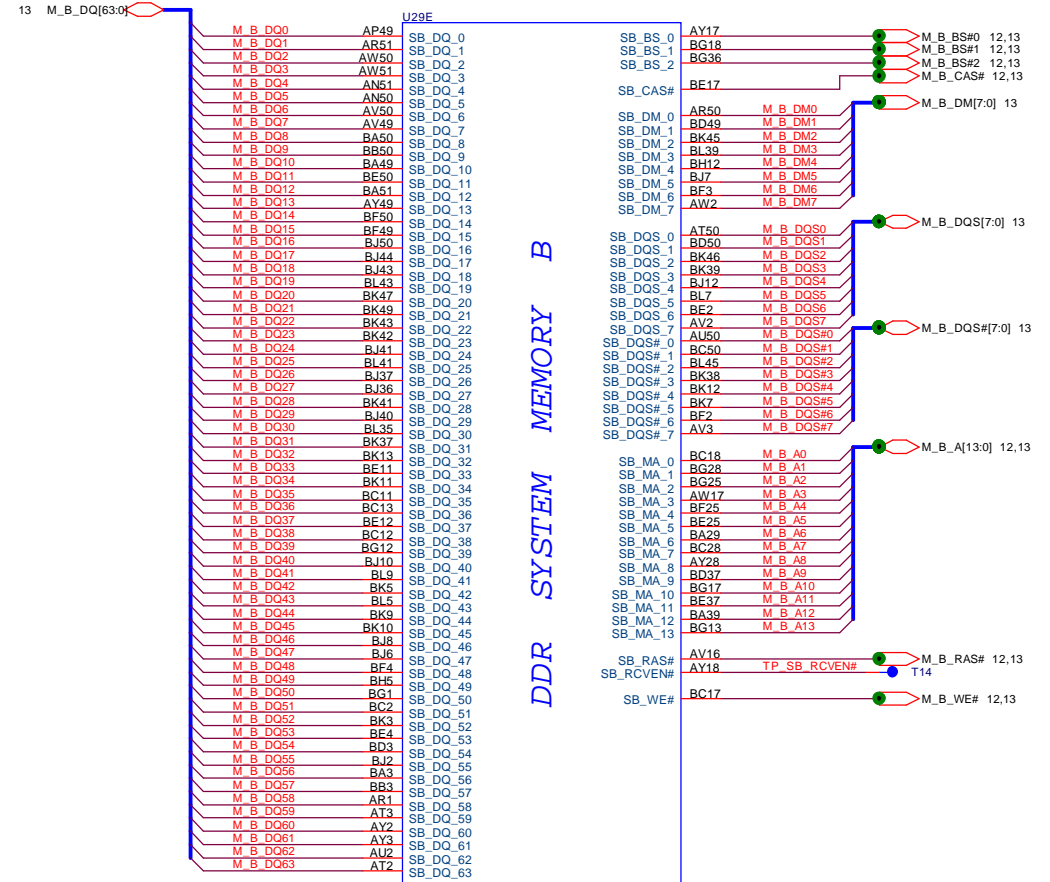
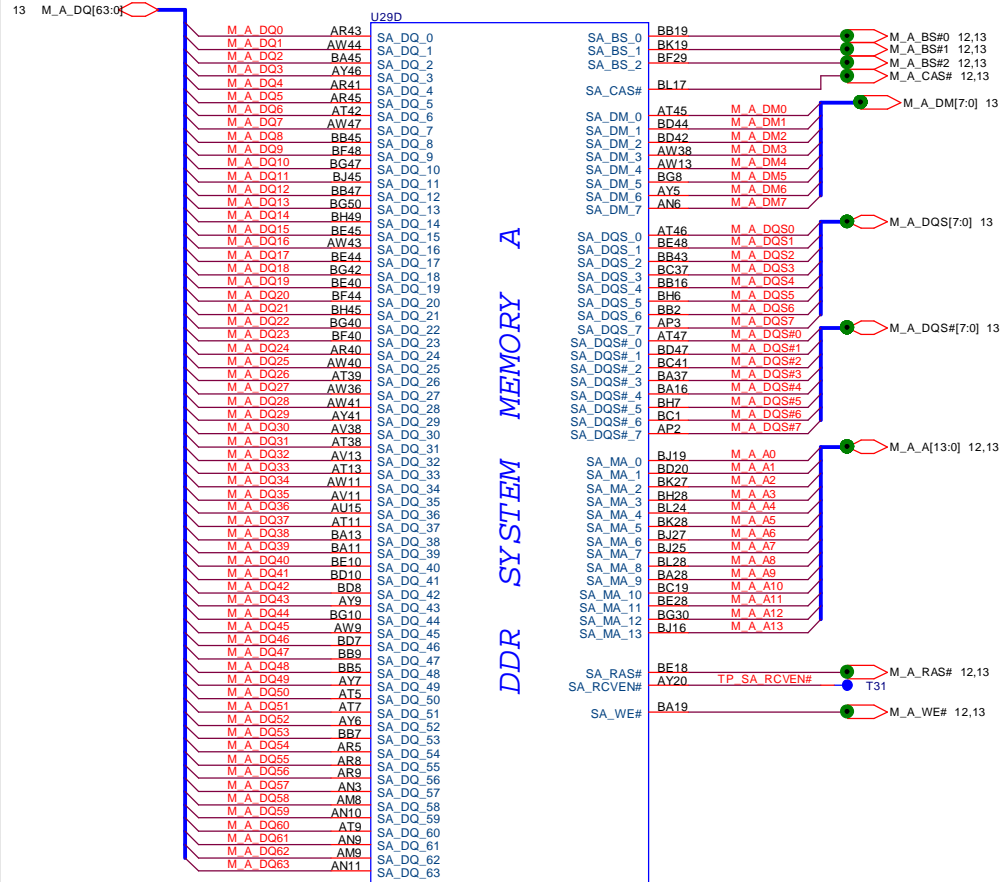
PROJECT : ZU1  
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH HOST(1 of 7)	1A
Date:	Thursday, November 02, 2006	Sheet 5 of 39

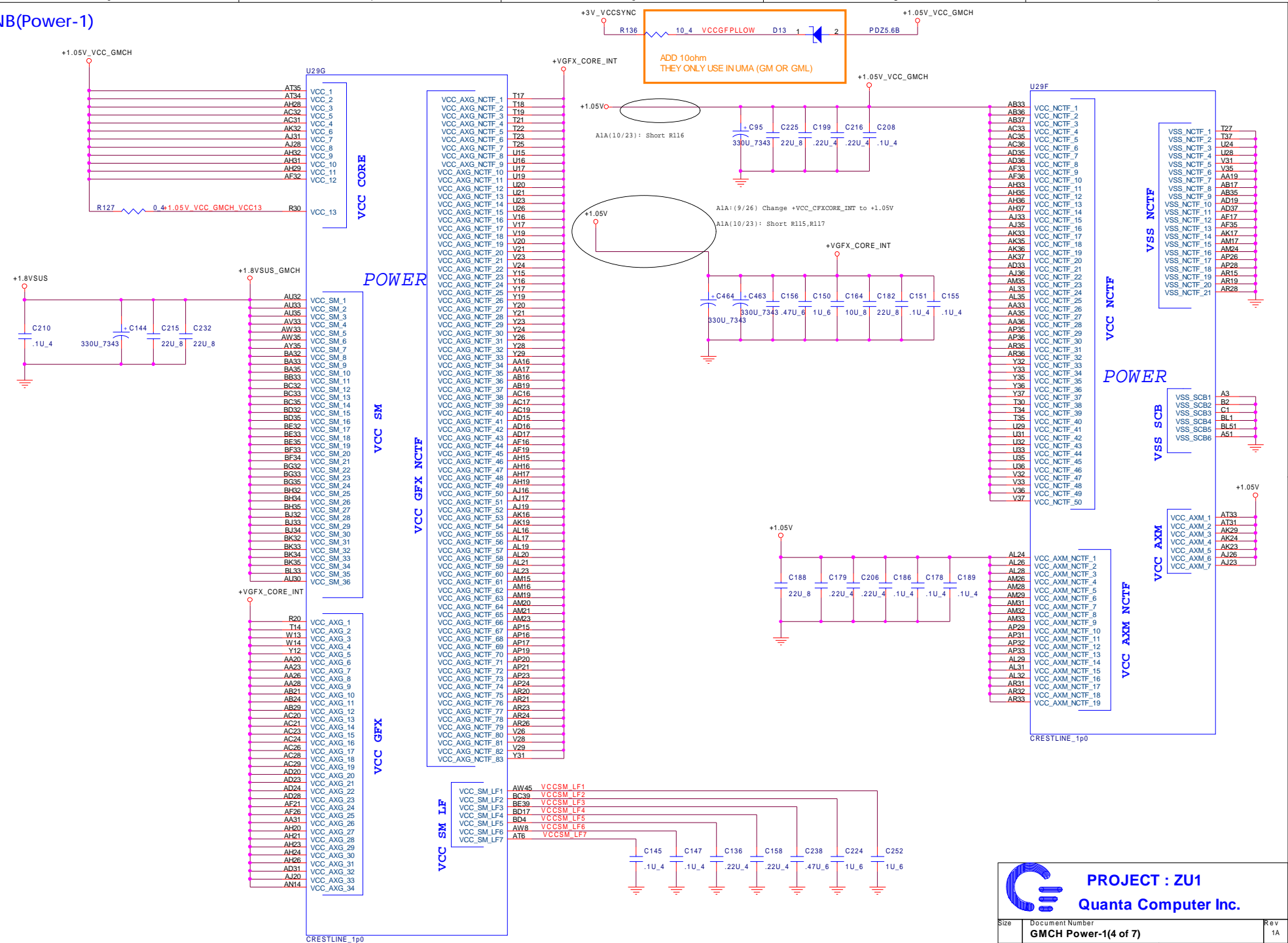




# NB(Memory controller)



NB(Power-1)



**PROJECT : ZU1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>GMCH Power-1(4 of 7)</b>	1A
Date:	Thursday, November 02, 2006	Sheet 8 of 39



# NB(Power-2)

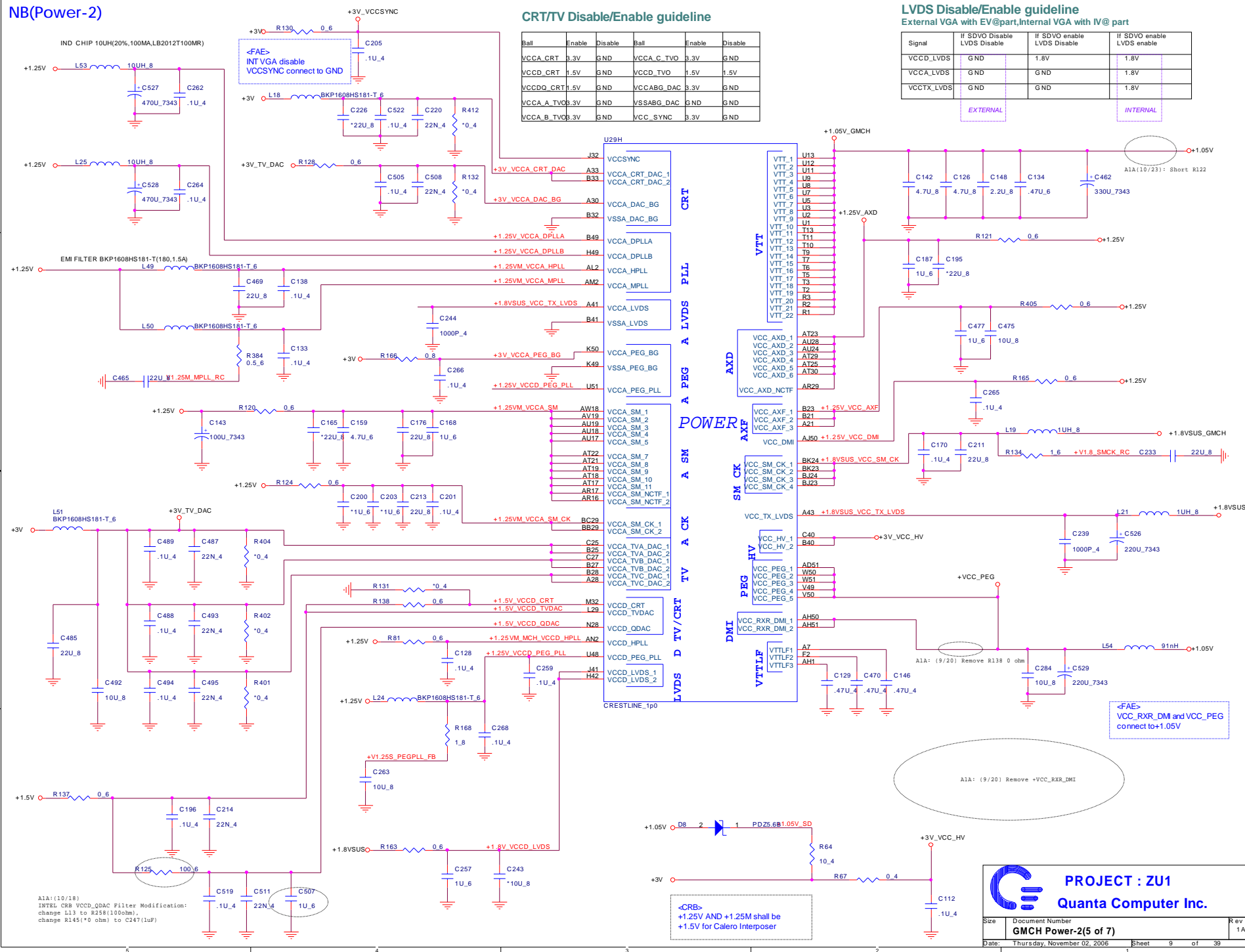
## CRT/TV Disable/Enable guideline

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT	3.3V	GND	VCCA_C_TV0	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TV0	1.5V	1.5V
VCCDQ_CRT	1.5V	GND	VCCABG_DAC	3.3V	GND
VCCA_A_TV0	3V	GND	VSSABG_DAC	GND	GND
VCCA_B_TV0	3V	GND	VCC_SYNC	3.3V	GND

## LVDS Disable/Enable guideline

External VGA with EV@part, Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If SDVO enable LVDS Disable	If SDVO enable LVDS enable
VCCD_LVDS	GND	1.8V	1.8V
VCCA_LVDS	GND	GND	1.8V
VCCTX_LVDS	GND	GND	1.8V



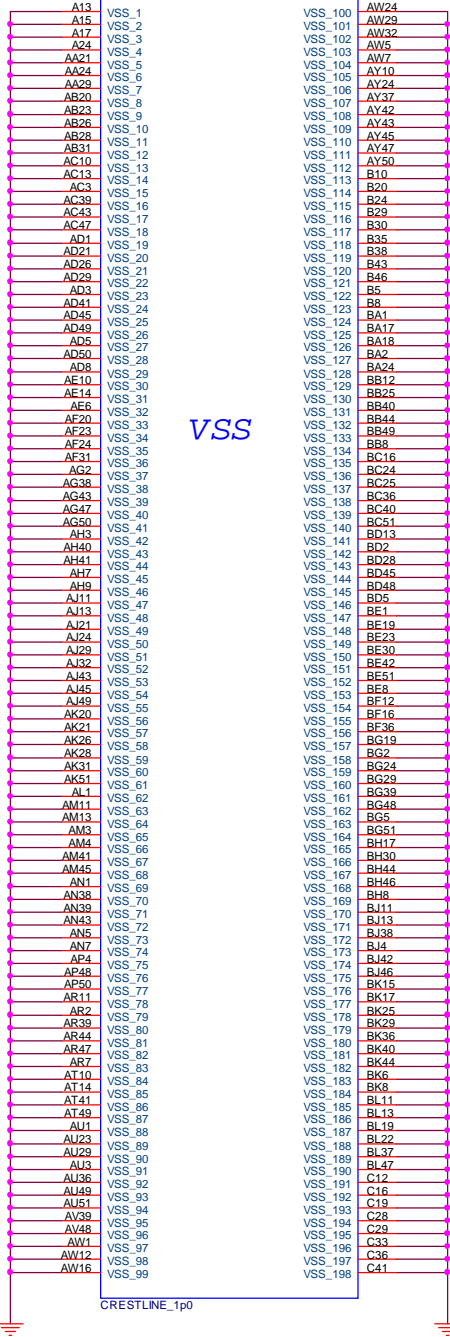
**PROJECT : ZU1**  
**Quanta Computer Inc.**

Size	Document Number	Sheet	Rev
	GMCH Power-2(5 of 7)	9 of 30	1A

Date: Thursday, November 02, 2006

# NB(Power-3)

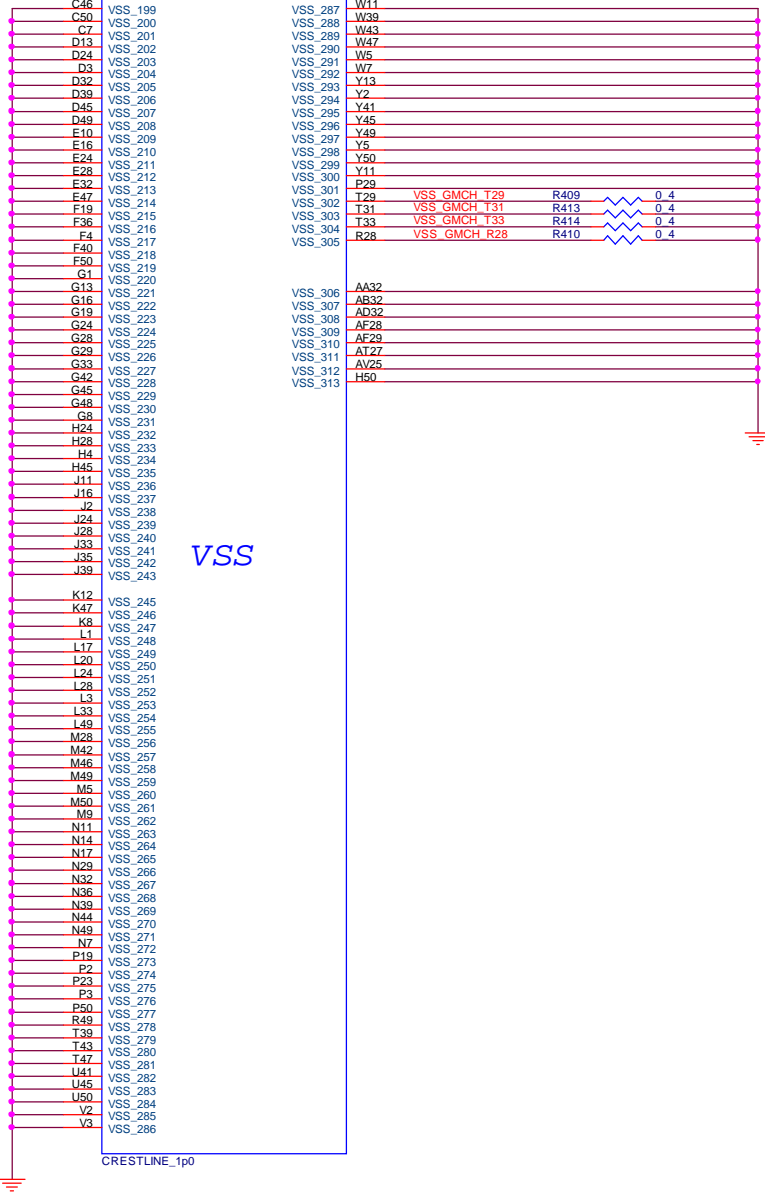
U29I



VSS

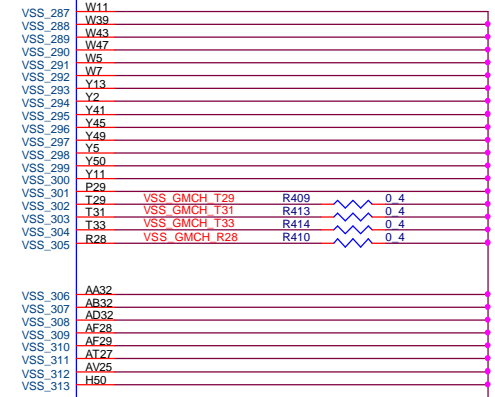
CRESTLINE\_1p0

U29J



VSS

CRESTLINE\_1p0



**PROJECT : ZU1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>GMCH Power-3(6 of 7)</b>	1A
Date:	Thursday, November 02, 2006	Sheet 10 of 39

## Strap table

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CFG[17:3] Have internal Pull-up

CFG[18:19] Have internal Pull-down

Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIe x1 is operation(Default) 1 = SDVO and PCIe x1 are operating simultaneously via the PEG port

### DMI X2 Select

MCH_CFG_5	Low = DMIx2 High = IDMIx4(Default)
-----------	---------------------------------------



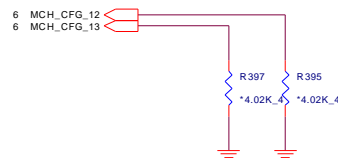
### DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane
------------	--



### XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)



### PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)
-----------	--

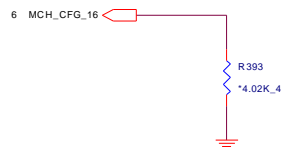


### SDVO Present

Strap define at External  
DVI control page

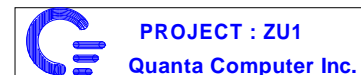
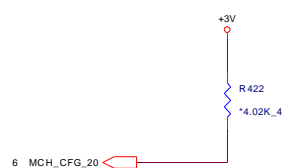
### FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)
------------	---



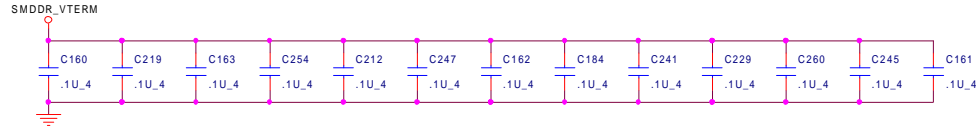
### SDVO/PCIe Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIe X1 is operational(Default) High = SDVO and PCIe X1 are operating simultaneously via the PEG port
------------	---



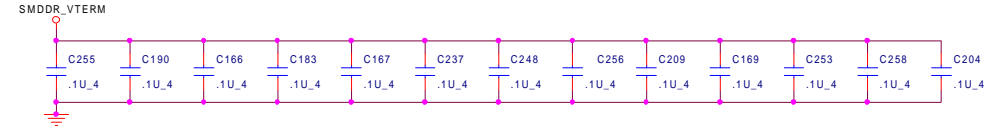
# DDR2 Dual channel A/B PU

## DDRII A CHANNEL

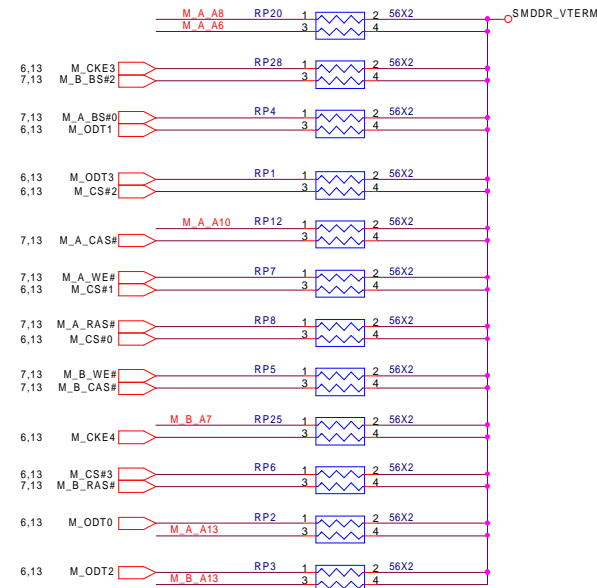
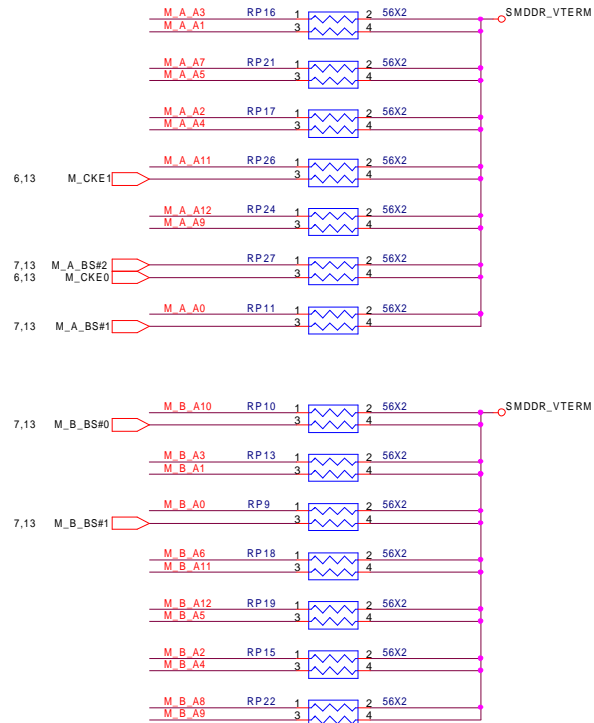


M\_A\_A[13..0] M\_A\_A[13..0] 7,13  
M\_B\_A[13..0] M\_B\_A[13..0] 7,13

## DDRII B CHANNEL



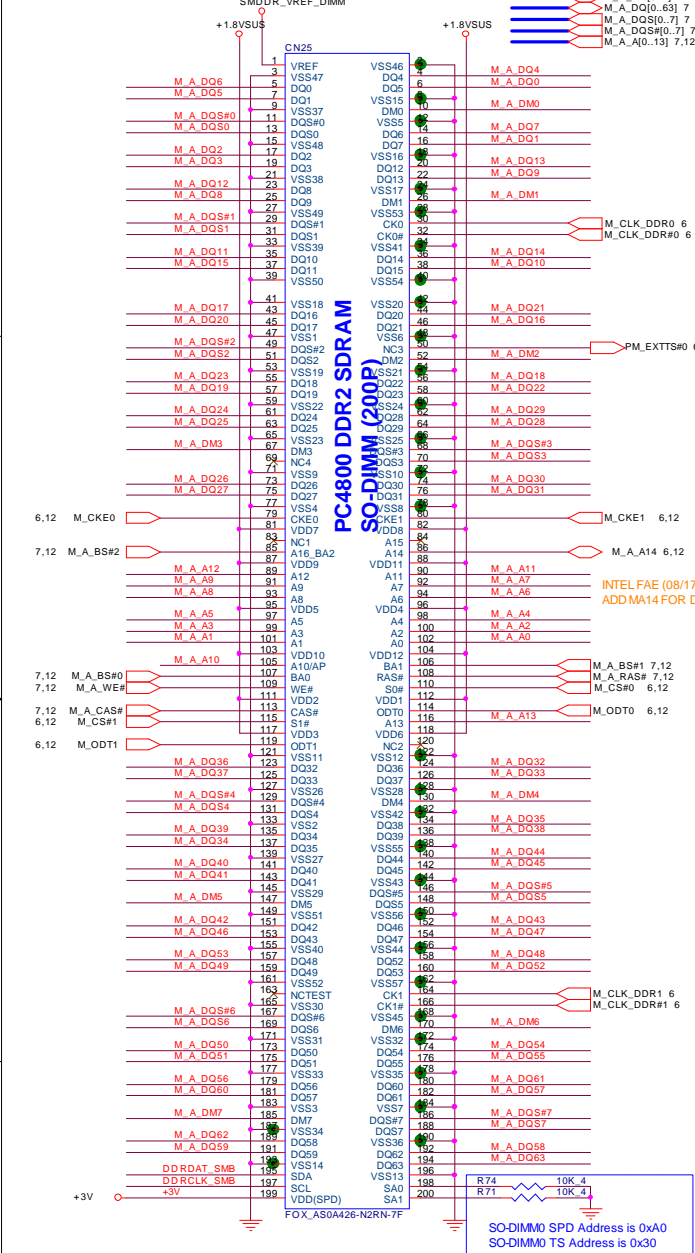
Place one cap close to every 2 pull-up resistor terminated to SMDR\_VTERM



INTEL FAE (08/17)  
ADD MA14 FOR DUAL LAYERS RAM

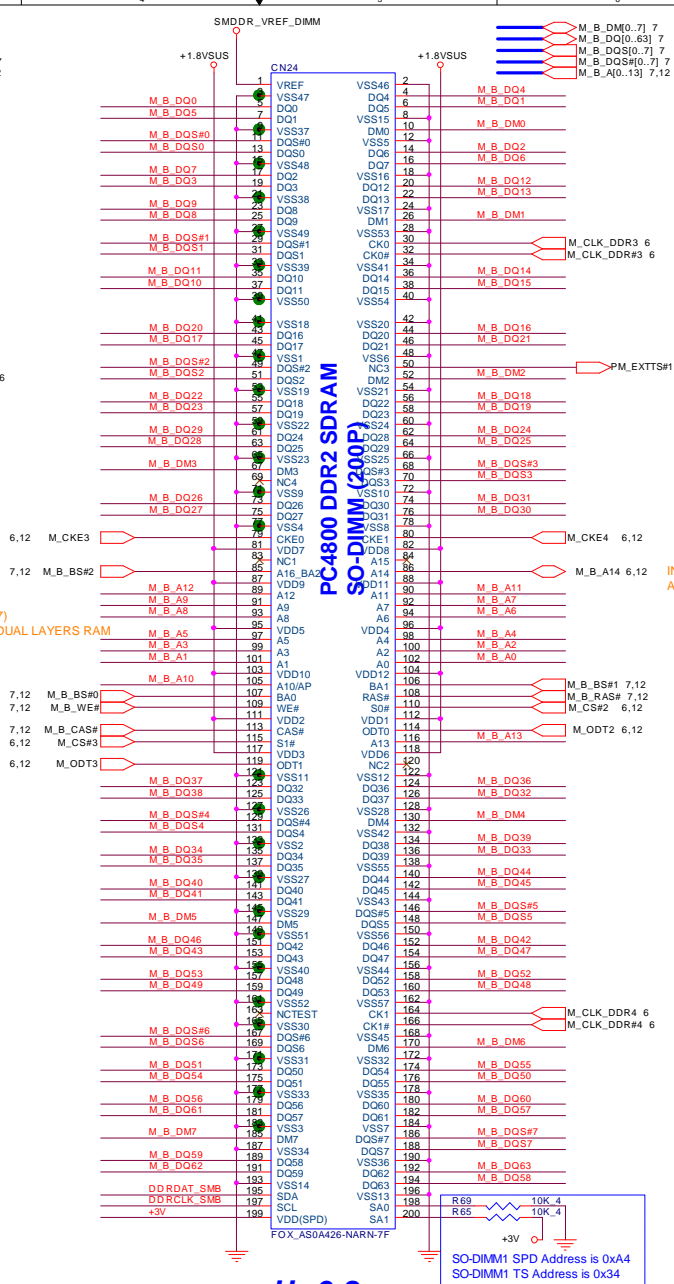


DDR2 Dual channel A/B CONN



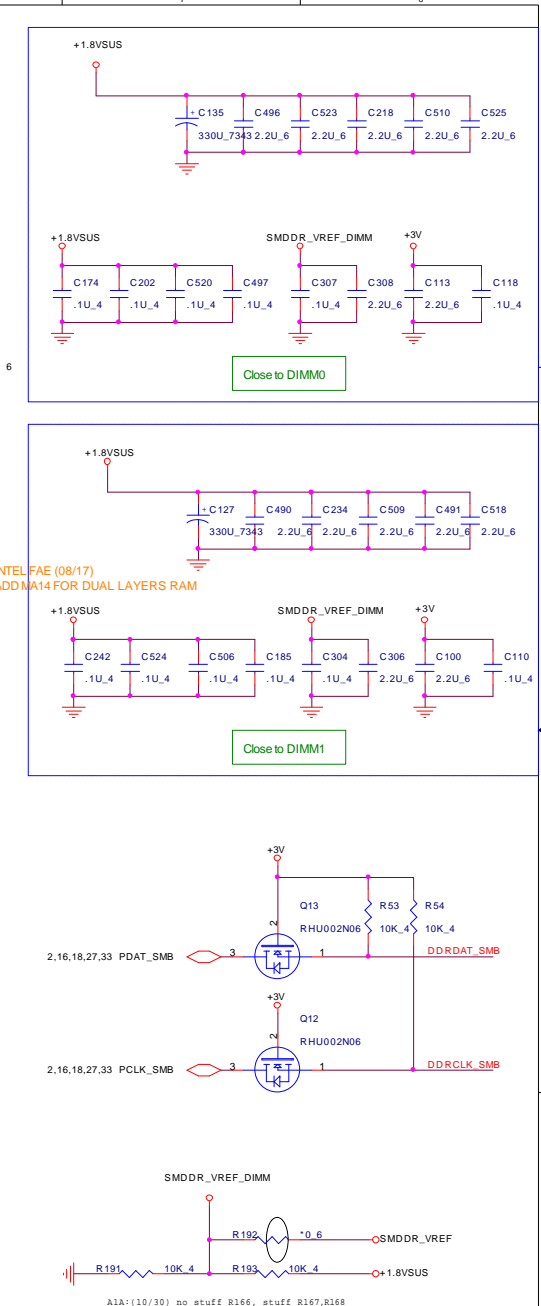
***H: 5.2mm***

CLOCK 0,1  
CKE 0,1



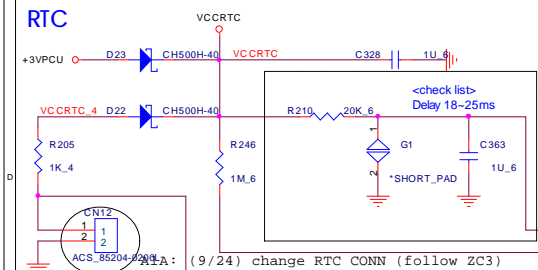
***H: 9.2mm***

**CLOCK 3,4**  
**CKE 2,3**



**PROJECT : ZU1**  
**Quanta Computer Inc.**

## RTC



## SATA Disable

- 1.Connect to GND: SATA[2:0]RXp/n, SATARBIAS, SATARBIAS#, SATA\_CLKP, SATACLKN
- 2.NC: SATA[2:0]TXp/n, SATALED#
- 3.VccSATAPLL should be connected directly to Vcc1\_5. Filter cap are not required
- 4.BIOS disable

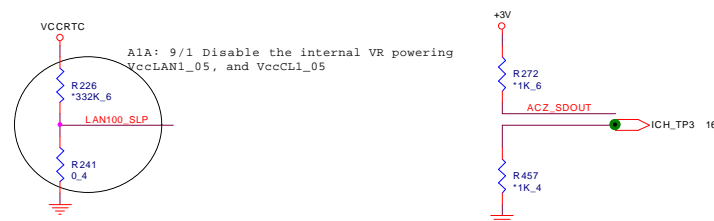
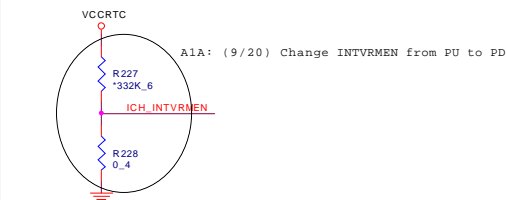
## SB Strap

### ICH8-M Internal VR Enable strap (Internal VR for Vccsus1\_05, Vccsus1\_5 and VccCL1\_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)
----------	---

### ICH8-M LAN100\_SLP Strap (Internal VR for VccLAN1\_05 and VccCL1\_05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)
------------	---

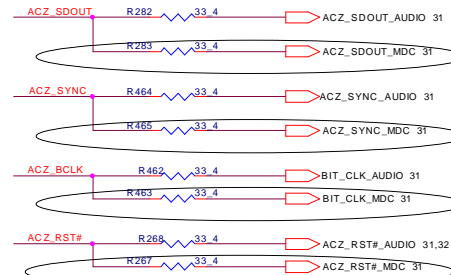


### XOR Chain Entrance Strap

ICH_RSVD	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1

## HDA

A1A: 9/6 base on Intel design guide, add it.



**PROJECT : ZU1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	ICH8M HOST(1 of 4)	1A
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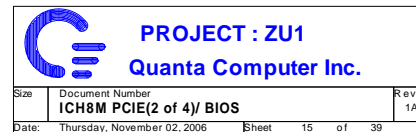
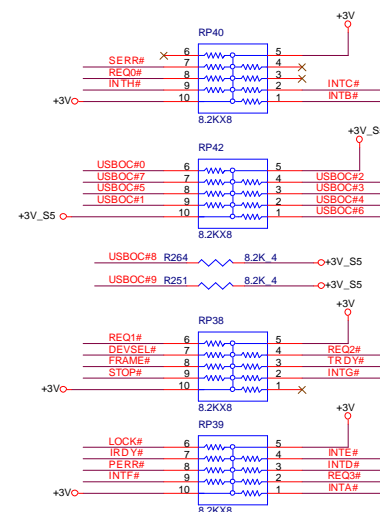
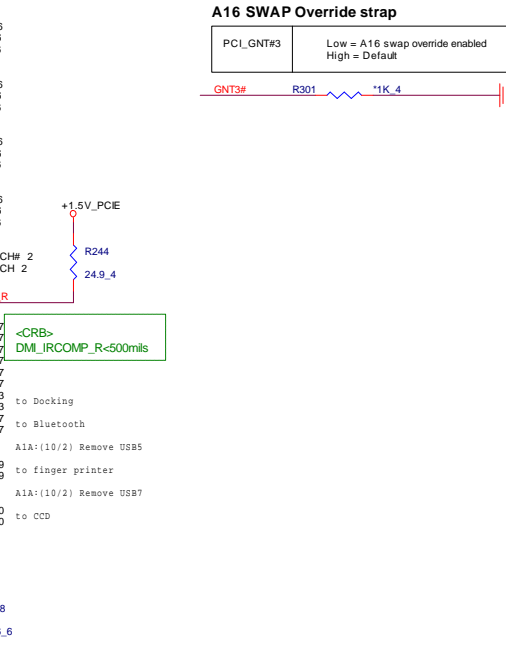
[illegible]

**U32B**

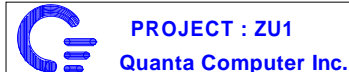
Pin	Signal	Function
22, 23, 25	AD[0..31]	Address
A0	D20	Data
A1	E19	Data
A2	D19	Data
A3	A20	Address
A4	D17	Data
A5	A21	Address
A6	A19	Address
A7	C19	Control
A8	A18	Address
A9	A18	Address
A10	B16	Control
A11	E16	Data
A12	A14	Address
A13	A16	Address
A14	B16	Control
A15	A15	Address
A16	B6	Control
A17	A8	Address
A18	D11	Data
A19	B12	Control
A20	D10	Data
A21	C7	Control
A22	C7	Control
A23	F13	Control
A24	E11	Data
A25	E13	Data
A26	E12	Data
A27	A6	Address
A28	D8	Data
A29	E8	Data
A30	D6	Data
A31	A3	Address

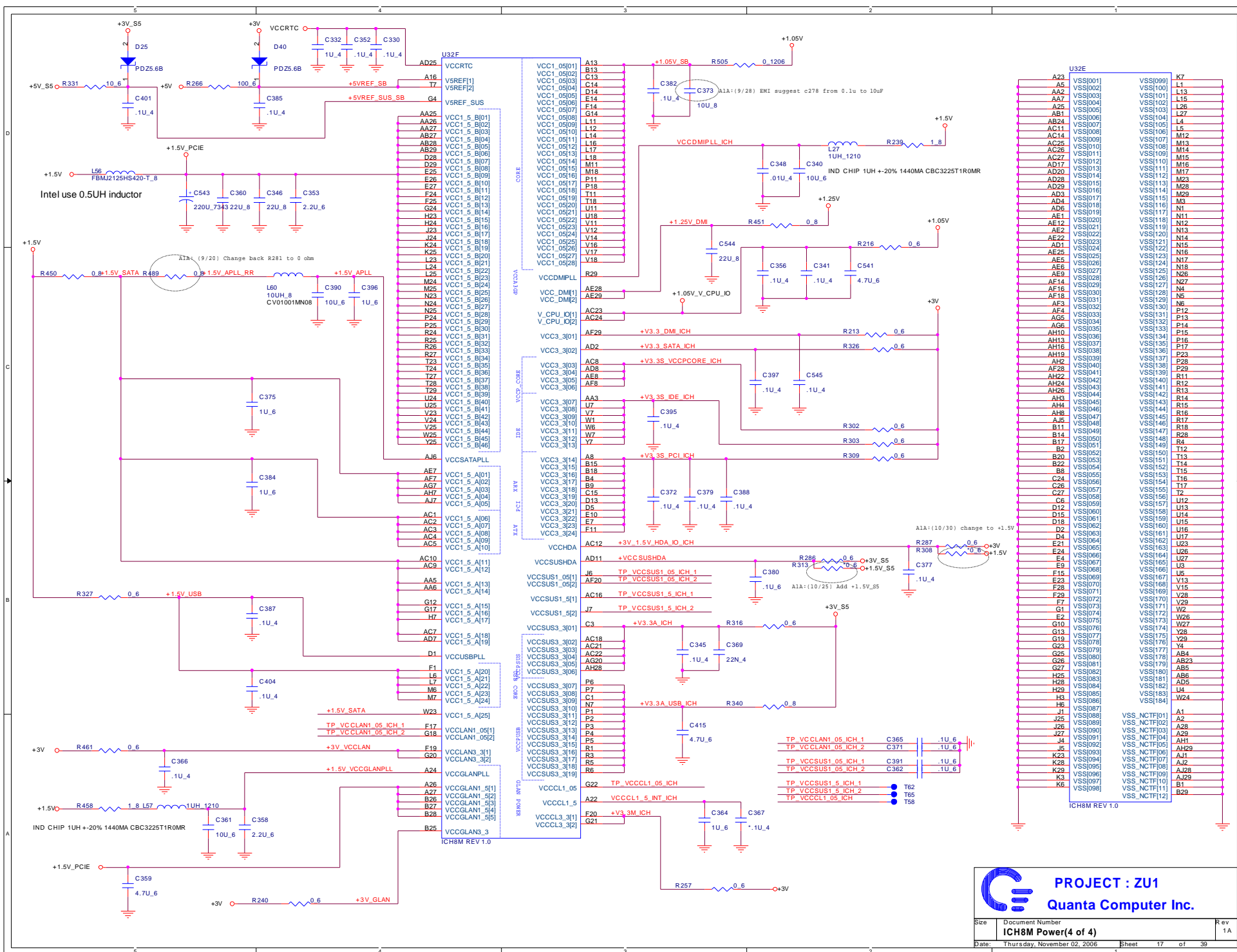
**PCI**

Pin	Signal	Function
REQ0#	GNT0#	Request/Grant
REQ1#	GNT1#	Request/Grant
REQ2#	GNT2#	Request/Grant
REQ3#	GNT3#	Request/Grant
REQ0#	GNT0#	Request/Grant
REQ1#	GNT1#	Request/Grant
REQ2#	GNT2#	Request/Grant
REQ3#	GNT3#	Request/Grant
REQ0#	GNT0#	Request/Grant
REQ1#	GNT1#	Request/Grant
REQ2#	GNT2#	Request/Grant
REQ3#	GNT3#	Request/Grant
REQ0#	GNT0#	Request/Grant
REQ1#	GNT1#	Request/Grant
REQ2#	GNT2#	Request/Grant
REQ3#	GNT3#	Request/Grant
REQ0#	GNT0#	Request/Grant
REQ1#	GNT1#	Request/Grant
REQ2#	GNT2#	Request/Grant
REQ3#	GNT3#	Request/Grant
REQ0#	GNT0#	Request/Grant
REQ1#	GNT1#	Request/Grant
REQ2#	GNT2#	Request/Grant
REQ3#	GNT3#	Request/Grant
REQ0#	GNT0#	Request/Grant
REQ1#	GNT1#	Request/Grant
REQ2#	GNT2#	Request/Grant
REQ3#	GNT3#	Request/Grant
REQ0#	GNT0#	Request/Grant
REQ1#	GNT1#	Request/Grant
REQ2#	GNT2#	Request/Grant
REQ3#	GNT3#	Request/Grant
REQ0#	GNT0#	Request/Grant
REQ1#	GNT1#	Request/Grant
REQ2#	GNT2#	Request/Grant
REQ3#	GNT3#	Request/Grant
REQ0#	GNT0#	Request/Grant
REQ1#	GNT1#	Request/Grant
REQ2#	GNT2#	Request/Grant
REQ3#	GNT3#	Request/Grant
REQ0#	GNT0#	Request/Grant
REQ1#	GNT1#	Request/Grant
REQ2#	GNT2#	Request/Grant
REQ3#	GNT3#	Request/Grant
REQ0#	GNT0#	Request/Grant
REQ1#	GNT1#	Request/Grant
REQ2#	GNT2#	Request/Grant
REQ3#	GNT3#	Request/Grant
REQ0#	GNT0#	Request/Grant
REQ1#	GNT1#	Request/Grant
REQ2#	GNT2#	Request/Grant
REQ3#	GNT3#	Request/Grant
REQ0#	GNT0#	Request/Grant
REQ1#	GNT1#	Request/Grant
REQ2#	GNT2#	Request/Grant
REQ3#	GNT3#	Request/Grant
REQ0#	GNT0#	Request/Grant
REQ1#	GNT1#	Request/Grant
REQ2#	GNT2#	Request/Grant
REQ3#	GNT3#	Request/Grant
REQ0#	GNT0#	Request/Grant
REQ1#	GNT1#	Request/Grant
REQ2#	GNT2#	Request/Grant
REQ3#	GNT3#	Request/Grant
REQ0#	GNT0#	Request/Grant
REQ1#	GNT1#	Request/Grant
REQ2#	GNT2#	Request/Grant
REQ3#	GNT3#	Request/Grant
REQ0#	GNT0#	Request/Grant
REQ1#	GNT1#	Request/Grant
REQ2#	GNT2#	Request/Grant
REQ3#	GNT3#	Request/Grant
REQ0#	GNT0#	Request/Grant
REQ1#	GNT1#	Request/Grant
REQ2#	GNT2#	Request/Grant
REQ3#	GNT3#	Request/Grant
REQ0#	GNT0#	Request/Grant
REQ1#	GNT1#	Request/Grant
REQ2#	GNT2#	Request/Grant
REQ3#	GNT3#	Request/Grant
REQ0#	GNT0#	Request/Grant
REQ1#	GNT1#	Request/Grant
REQ2#	GNT2#	Request/Grant
REQ3#	GNT3#	Request/Grant
REQ0#	GNT0#	Request/Grant
REQ1#	GNT1#	Request/Grant
REQ2#	GNT2#	Request/Grant</



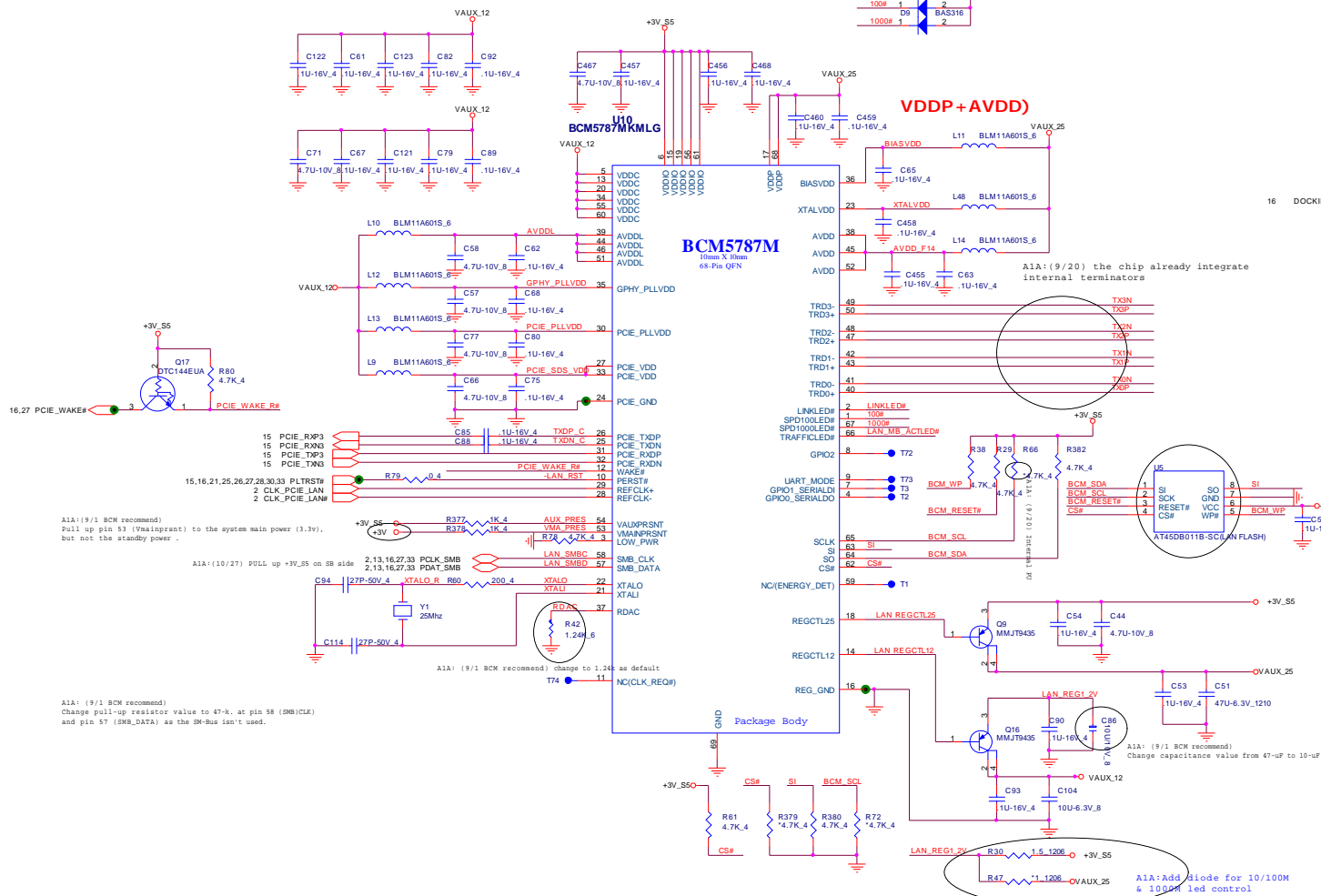
<FAE>  
CRB STP\_PC1# PU is no stuff.  
CRB STP\_CPU# always keeps high to  
ensure ME alive in M1 state.  
(CLK\_MCH\_BCLK/# must keep alive to  
make ME work)  
I think there will be update for this design  
I suggest you to keep PU and 0  
isolation resistors for this signal.





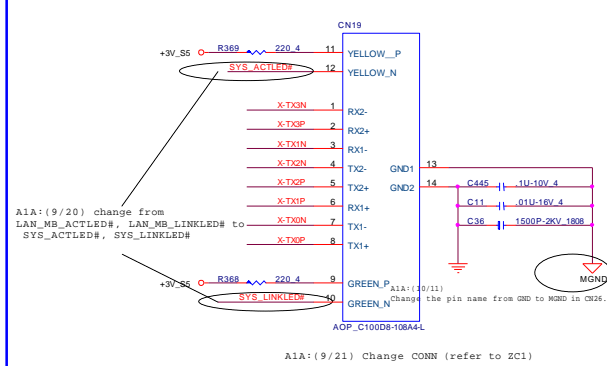
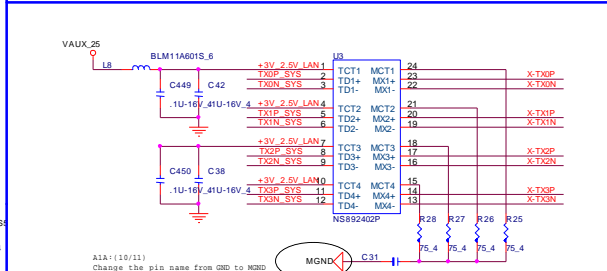
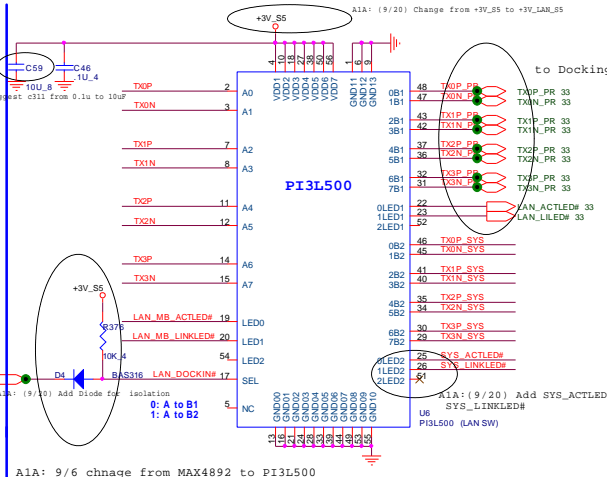
Giga LAN BCM5787M

A1A:(9/27) Change +3V\_LAN\_S5 to +3V

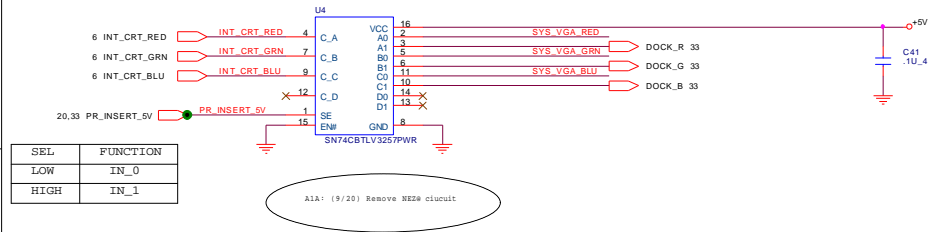


EEPROM Strapping

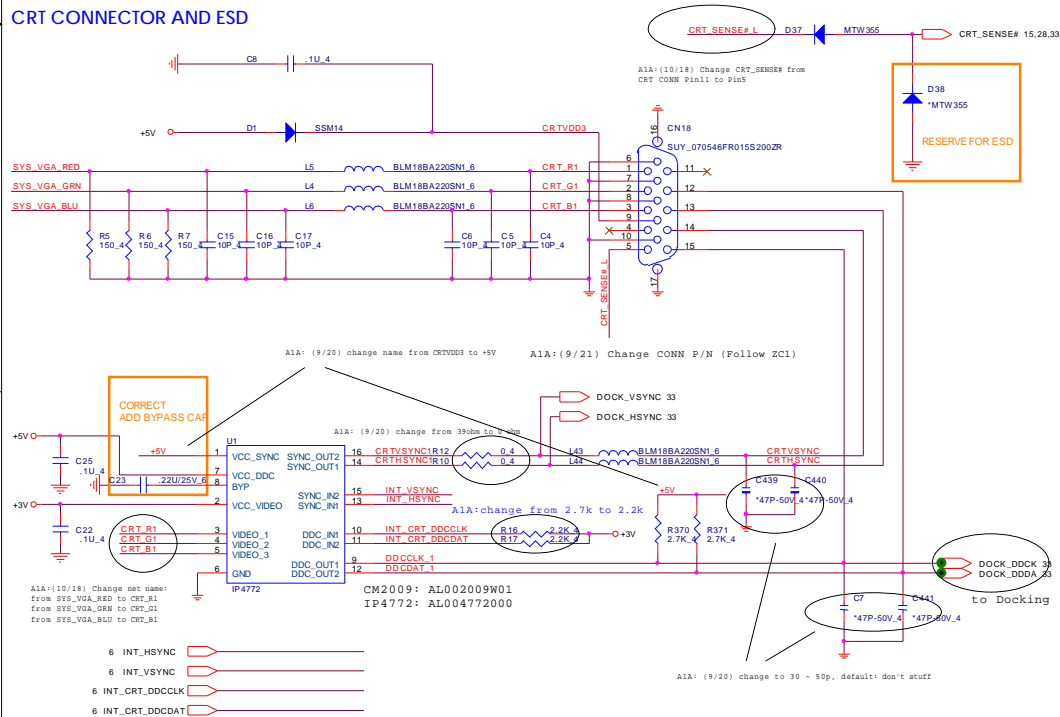
	SO	SI	CS#	SCLK
24c64	1	1	0	1
AT45DB011B	1	0	1	1



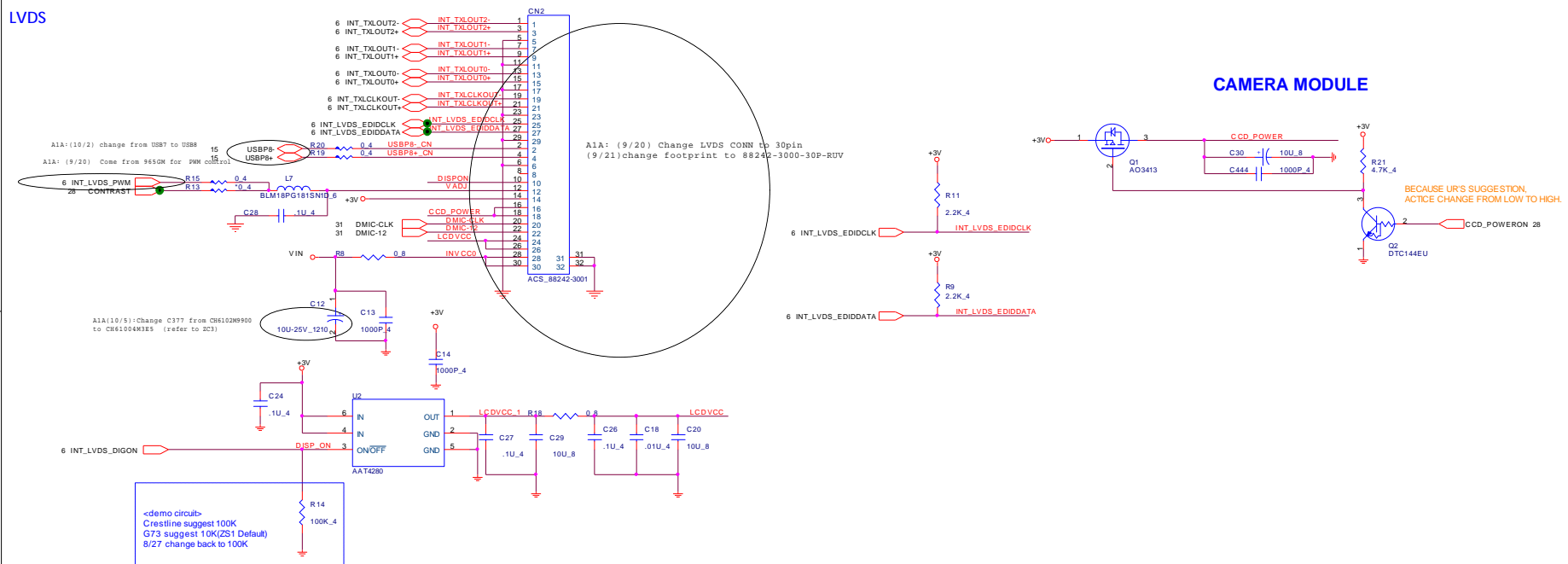
CRT Select



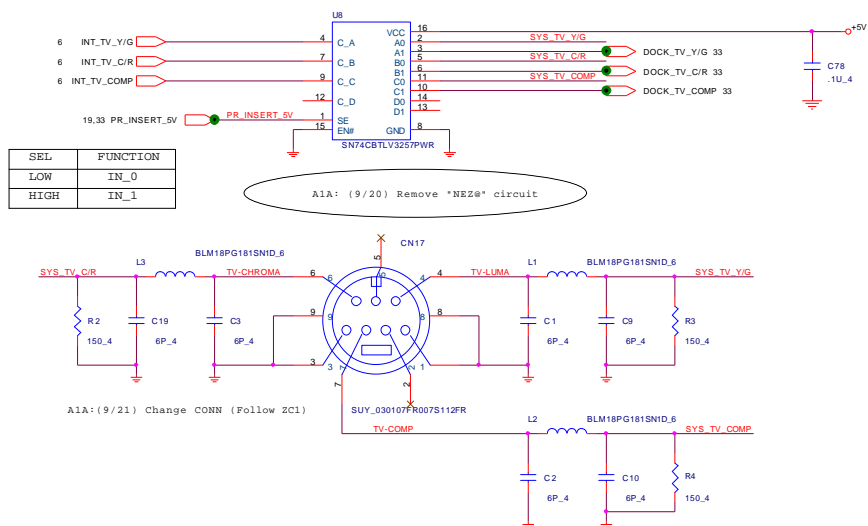
## CRT CONNECTOR AND ESD



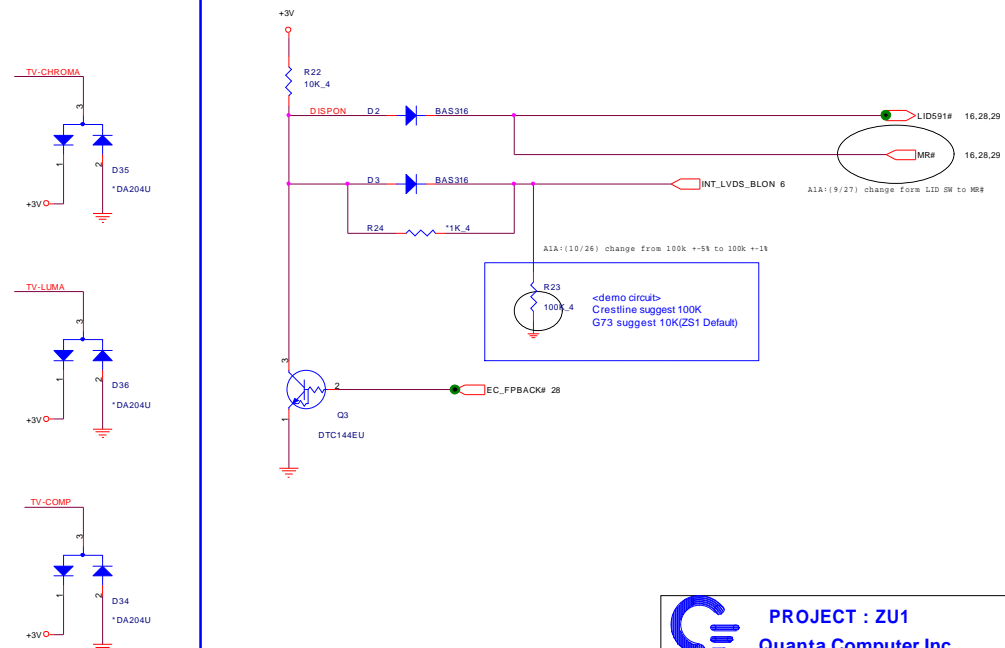
## LVDS



TV Out (SVHS) MiniDIN 7-pin

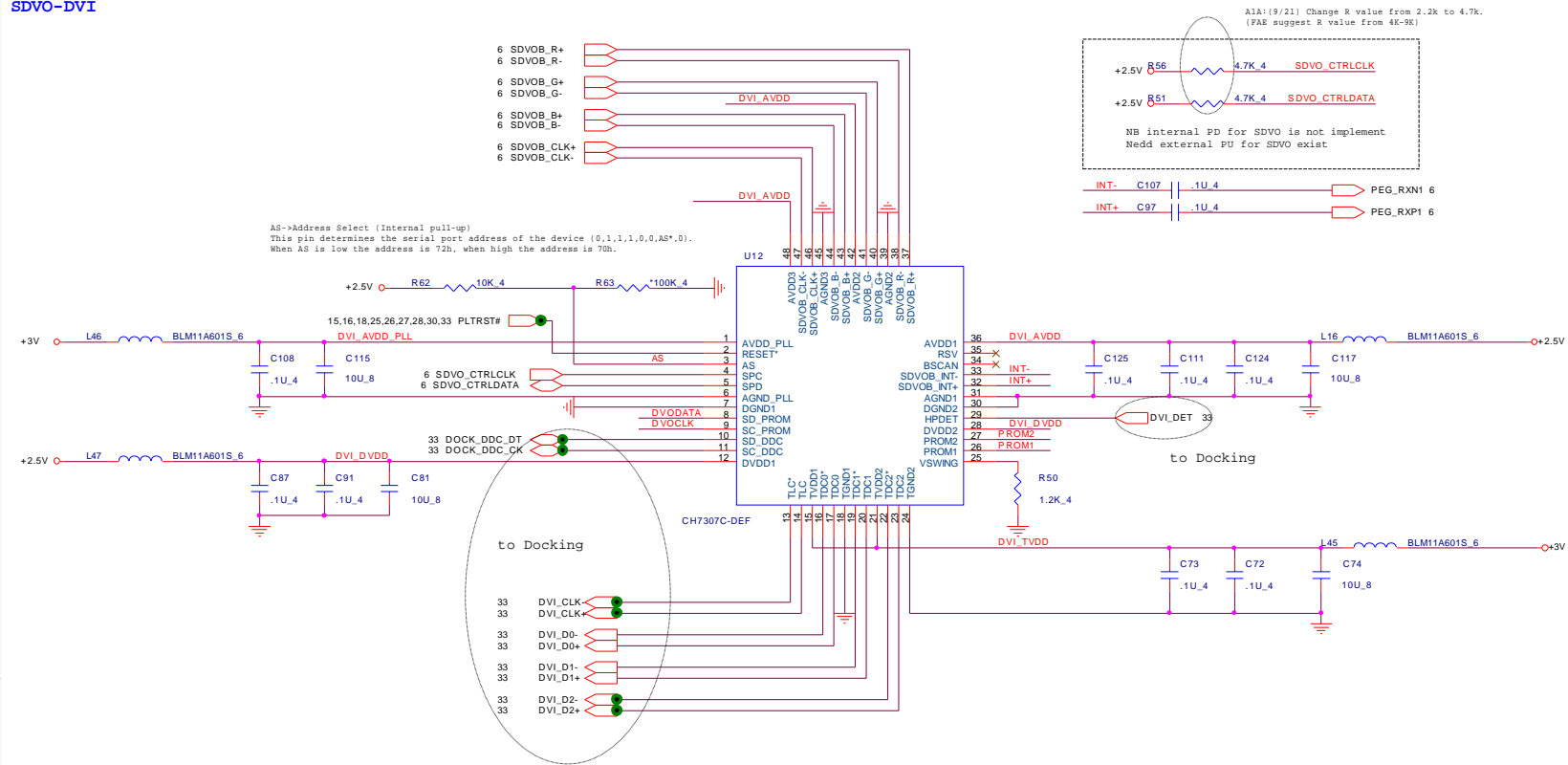


## MR Sensor

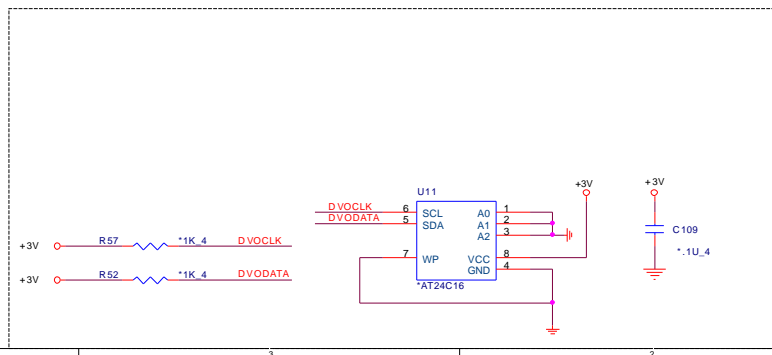
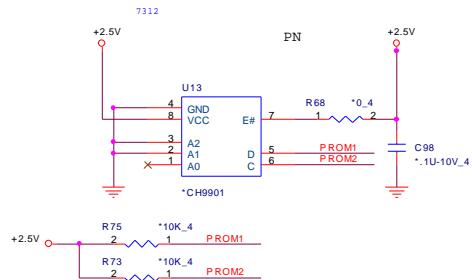




## SDVO-DVI

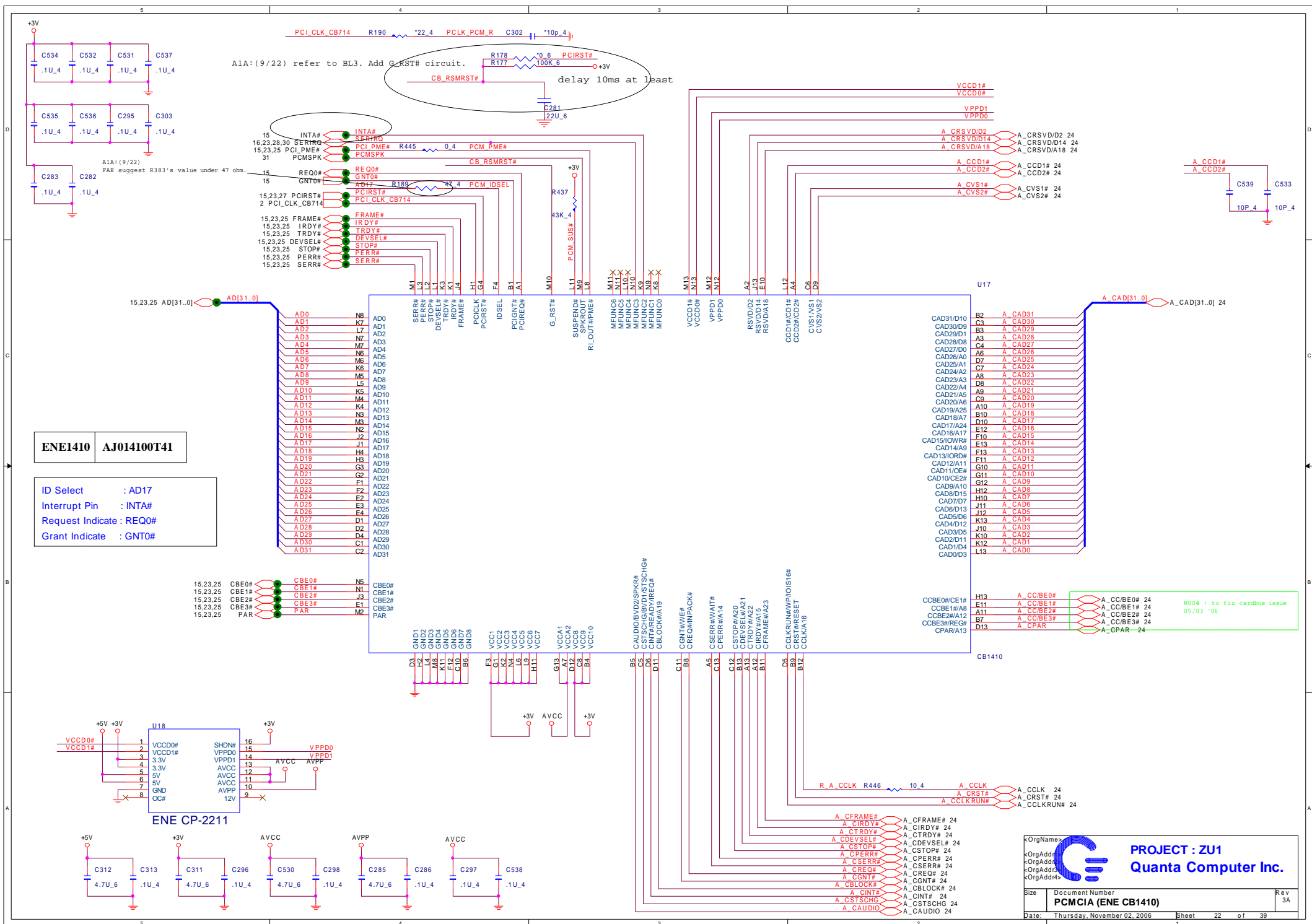


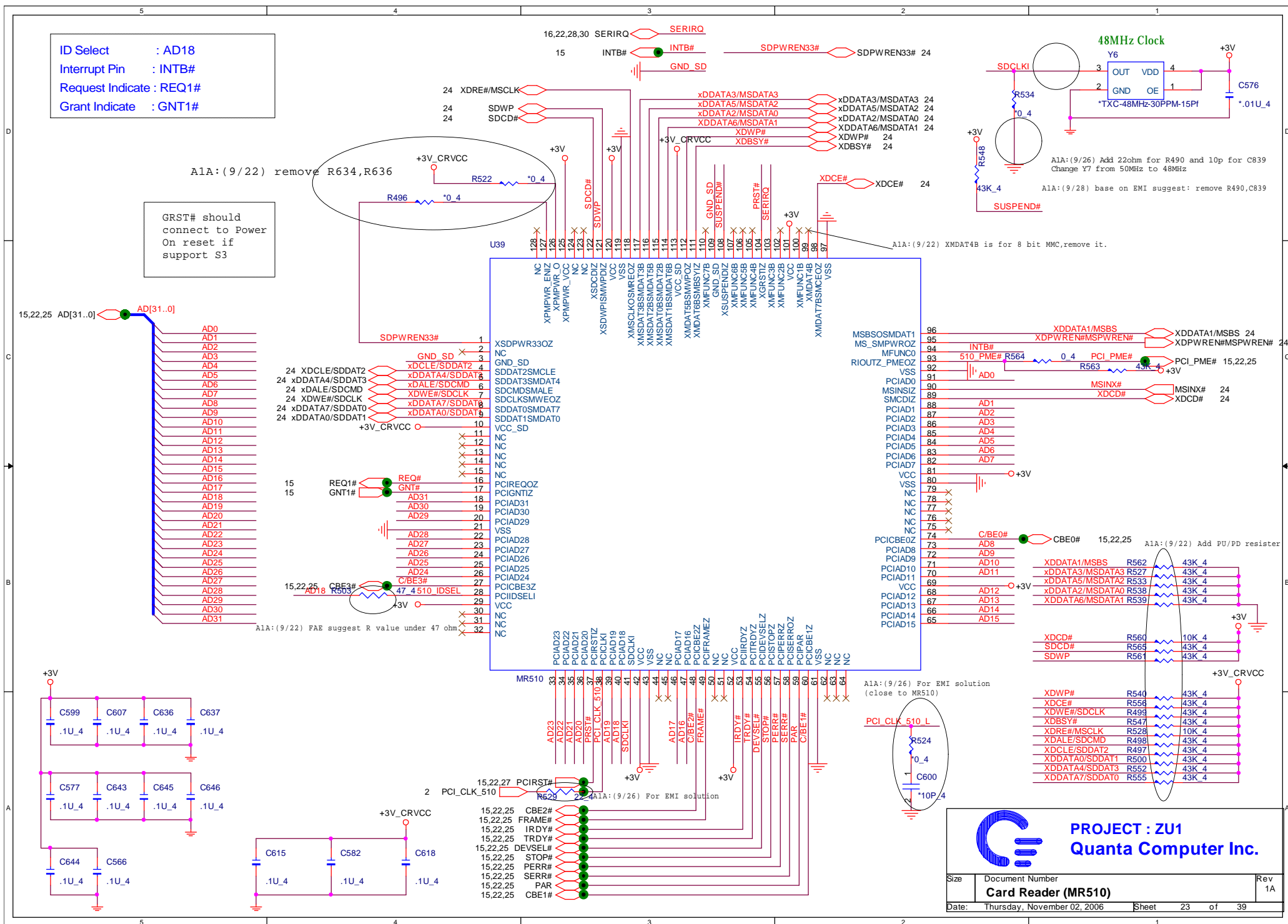
FOR CH7312 HDCP USE

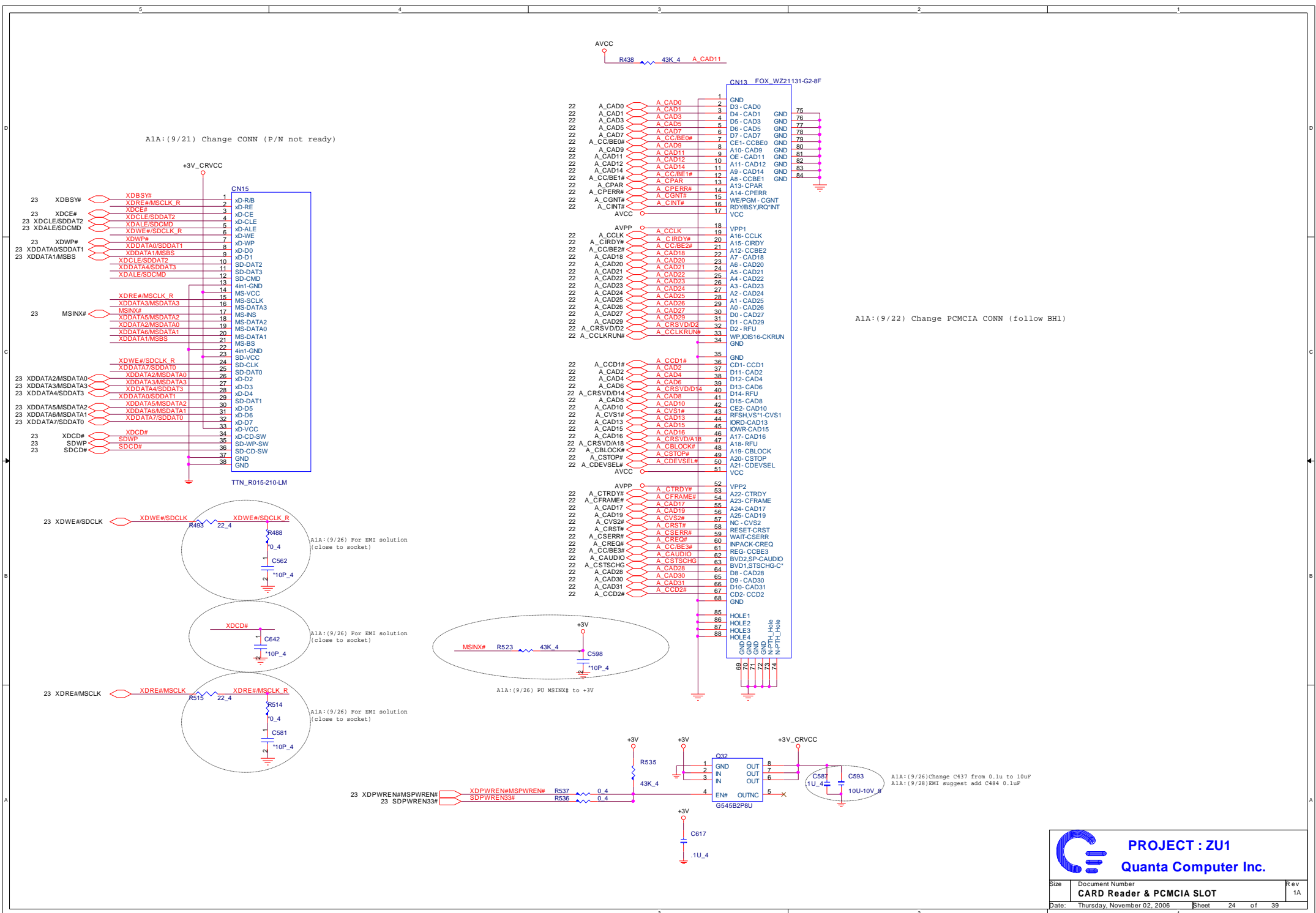


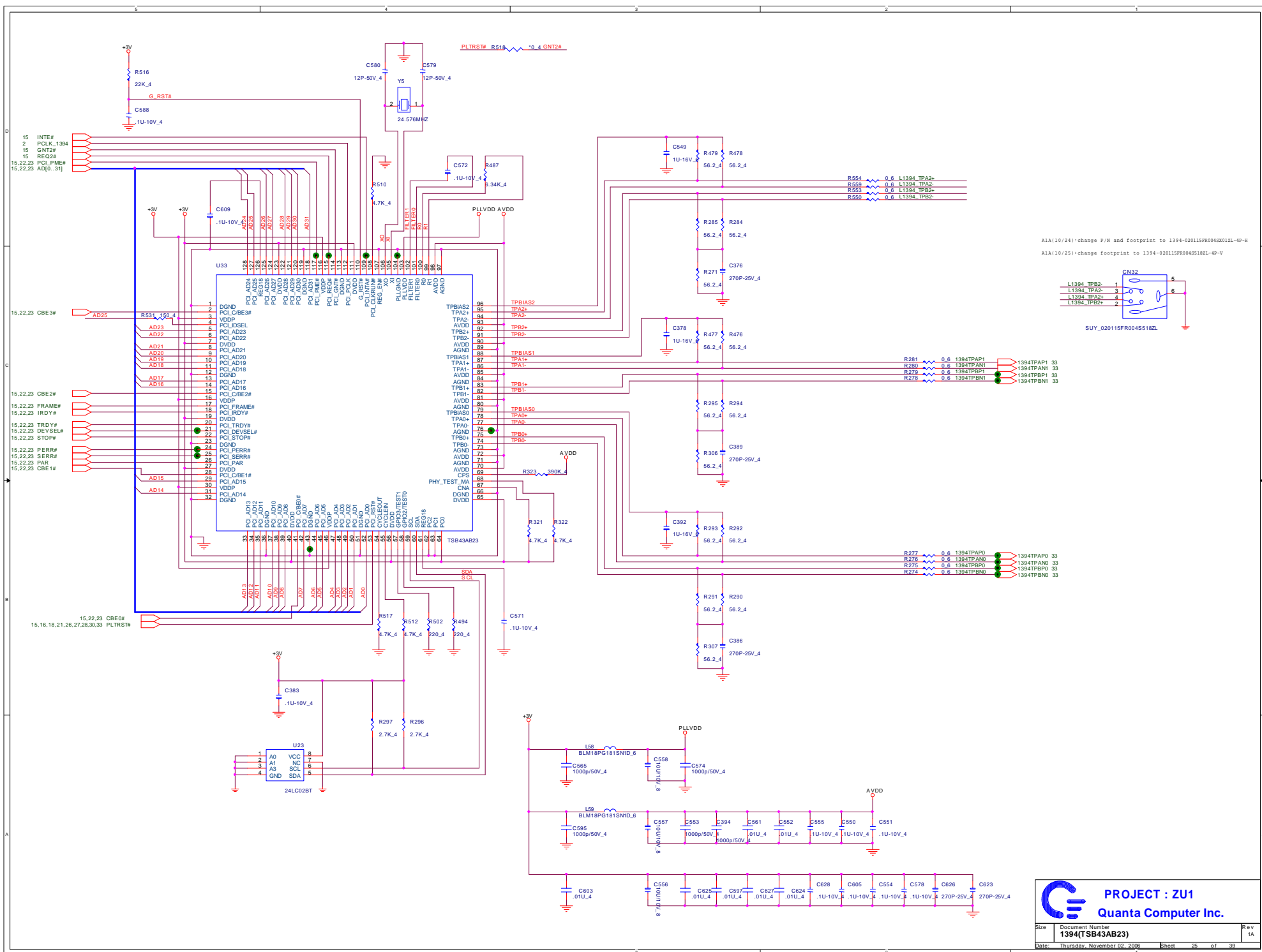
PROJECT : ZU1  
Quanta Computer Inc.

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	<b>DVI (CH7307)</b>	1 A
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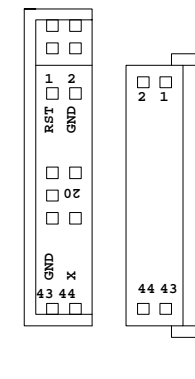
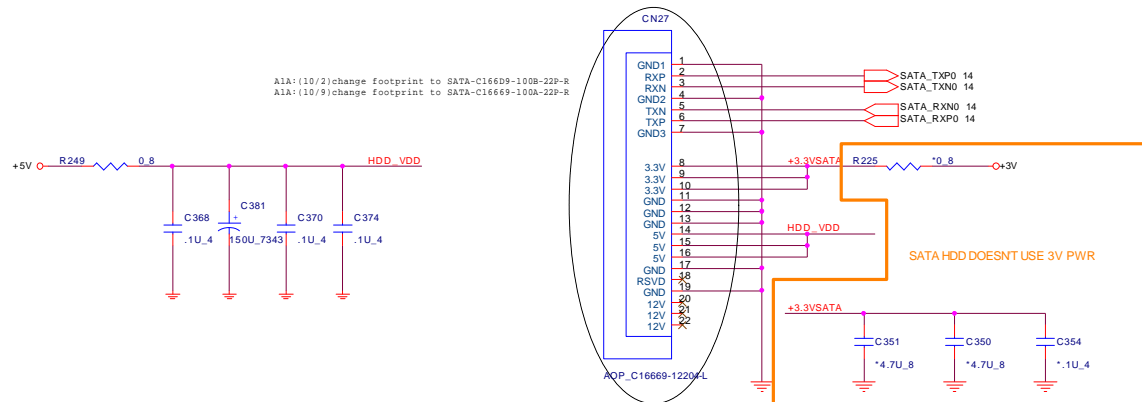




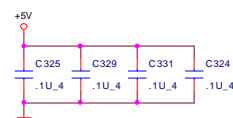
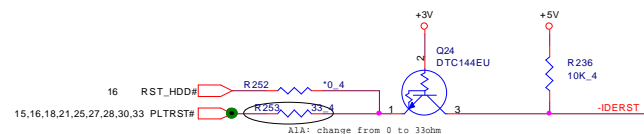




**SATA HDD**

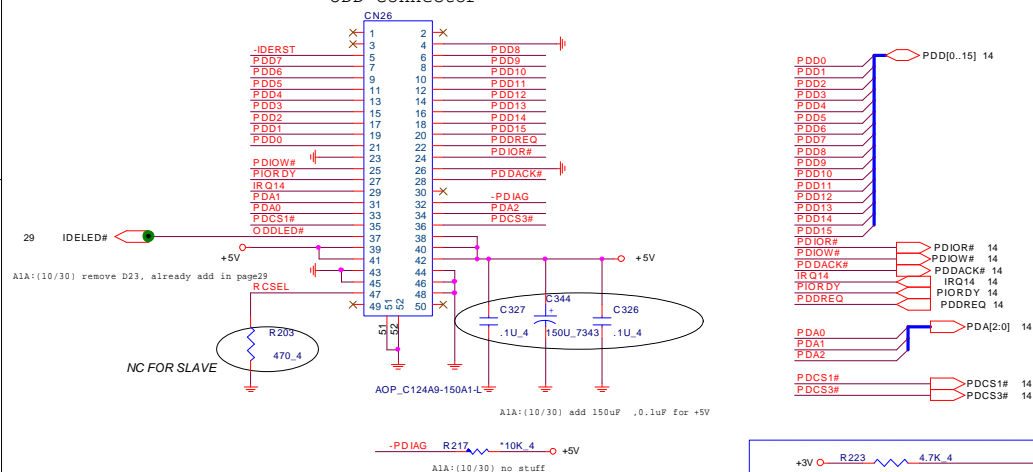


## PATA ODD



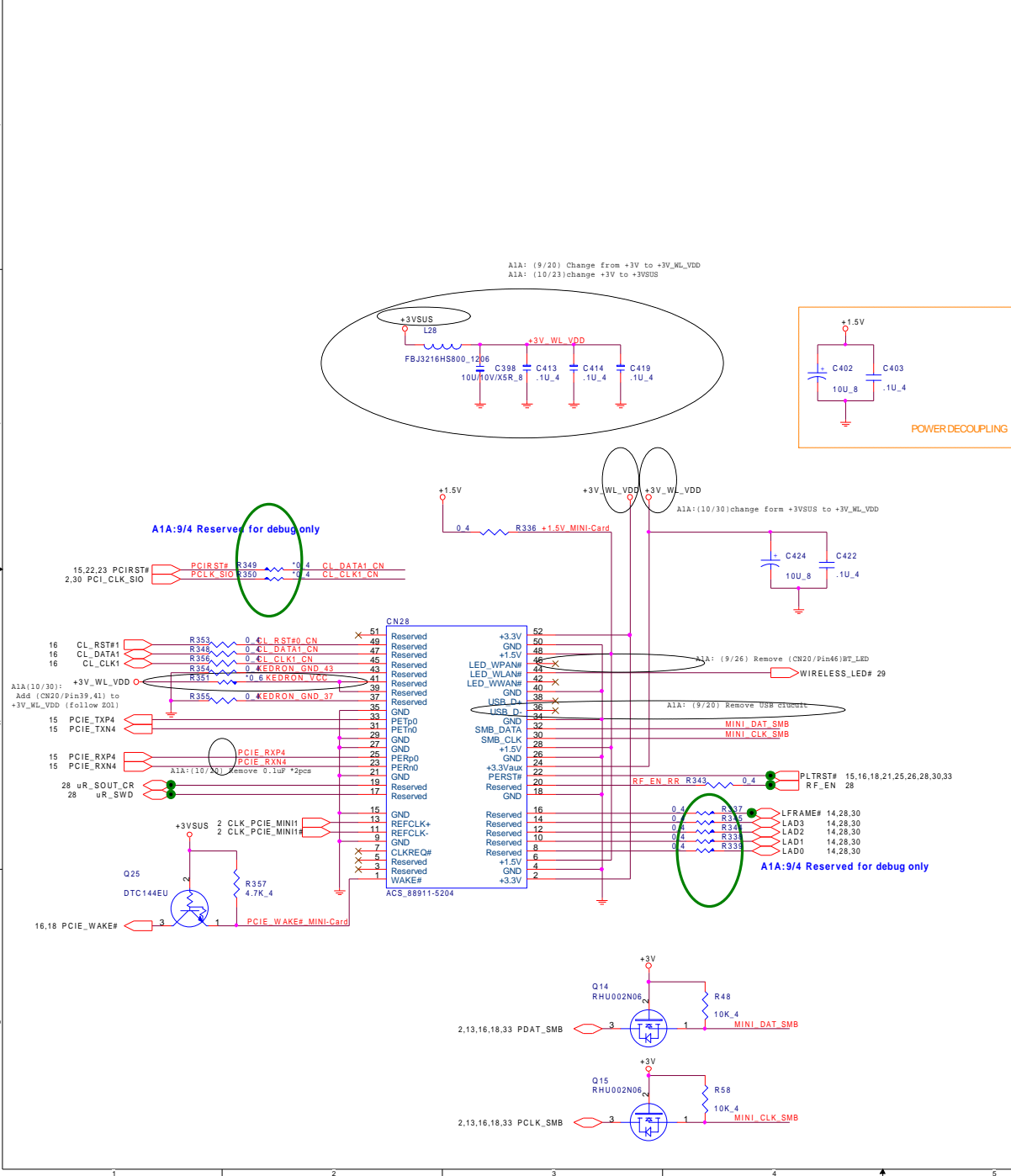
AlA:(9/29) change footprint: CDR-C124A9-100C-50P

### ODD Connector

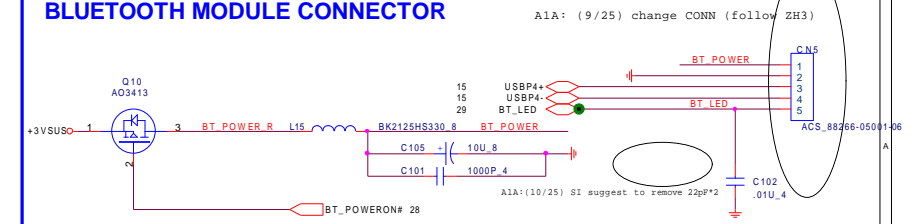




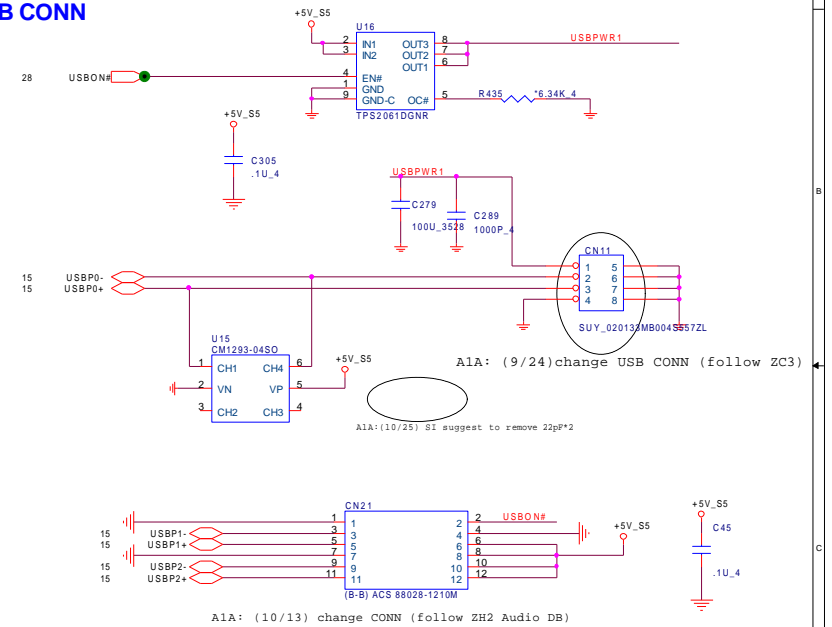
### MINI-Card



## BLUETOOTH MODULE CONNECTOR

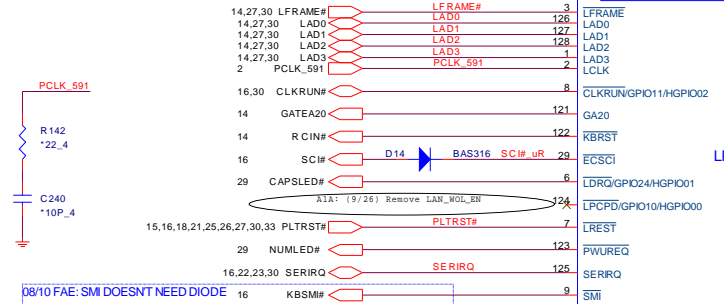


## USB CONN



A1A:(9/16)Change from WPC8769 to WPC8763

A1A: (9/25) place the above capacitors as close to the pins as possible



08/10 FAE: SMI DOESNT NEED DIODE

FOLLOW INTEL ME-EC INTERFACE SPECIFICATION.  
2ND\_SMB IS DEDICATED FOR ICH8 CONTROLLER LINK BUS.

A1A: (9/26) Remove MY16

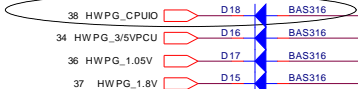


A1A: (9/25)  
PAB: PUT V6 with EC in the same side

08/10 FAE:  
ADD ONE GAD PAD UNDER X'TAL,  
AND KEEP CLEAN.

1/13 Confirm by vendor mail:  
Connect to AGND

A1A: (9/26) Add HWPG\_CPUIO



08/10 FAE:  
L83 CAN CHANGE FROM BEAD TO SHORT.  
BUT, PLEASE PUT AGND & 32K CAP & AVCC CAP AT ONE POINT.

ZS1 STILL USE BEAD FOR SAFE.

A1A: (9/25) change VBAT from +3VPCU to +A3VPCU

1/13 Confirm by vendor mail:  
VDD must power up after VCC/AVCC

1/13 Confirm by vendor mail:  
VBAT for keep PLL power let power up can quick  
If no VBAT will switch to VCCpower.  
If PLL no power will cause boot time delay.

A1A: (9/26) Add it. Capacitors as close to EC as possible

A1A: (9/24) remove ME\_EC\_ALERT#

A1A: (9/29)SWAP GPIO3 & GPIO6 (follow EC team)

A1A: (9/26) Remove M/A#

A1A: (9/26) Remove BL/CH

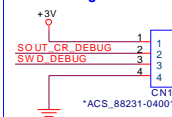
08/10 FAE: ADD TP FOR DEBUG

08/14 FAE:  
Please connect VREF(uRider pin104) to +A3VPCU instead of +3VPCU.

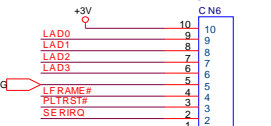
## DEBUG PORTS

A1A(10/5):Change LPC debug CONN to DPFC10P8103

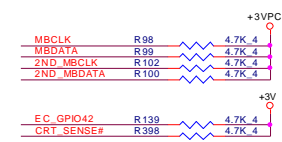
### EC Debug Port



### Reserved for LPC debug card



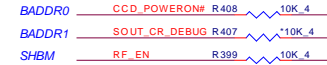
## SM BUS PU



## I/O ADDRESS SETTING

I/O Address		
BADDR1-0	Index	Data
0 0		XORTREE TEST MODE
0 1		CORE DEFINED
1 0	2Eh	2Fh
1 1	164Eh	164Fh

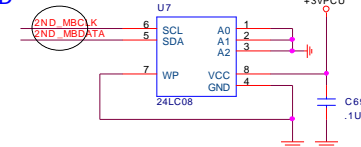
SHBM=0: Enable shared memory with host BIOS



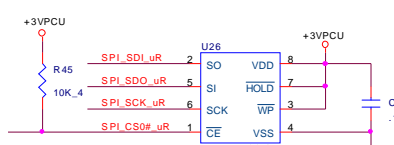
1/13 Confirm by vendor mail:  
Disabled ('1') if using FW device on LPC.  
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

## ACER ID

A1A:(9/29) change from MBCLK/MBDATA to 2ND\_MBCLK/2ND\_MBDATA



## SPI FLASH



1/13 Confirm by vendor mail:  
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

## BUTTON ON KEYBOARD MATRIX

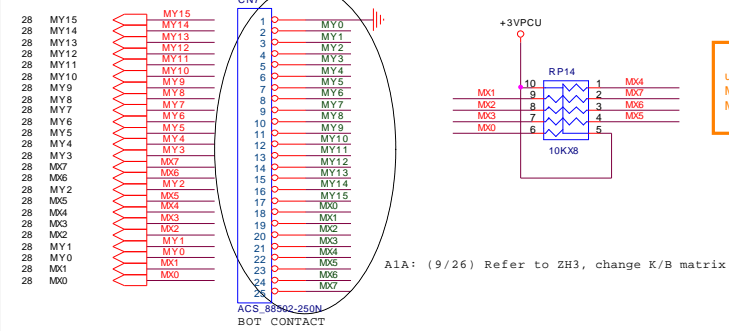


## INTERNAL KEYBOARD STRIP SET



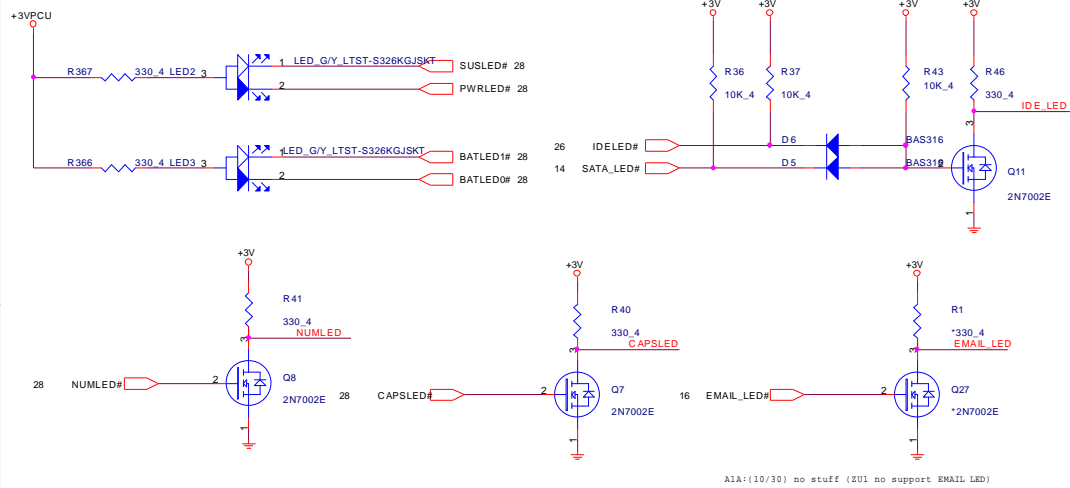
PROJECT : ZU1  
Quanta Computer Inc.

## INT K/B

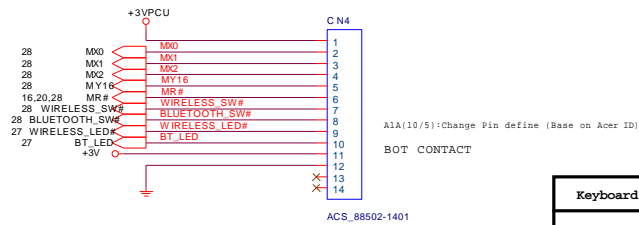


IR REQUEST  
 MY DOES NOT NEED PU.  
 MY CANNOT USE EM BYPASS CAP, DUE TO FLASH.

## LED

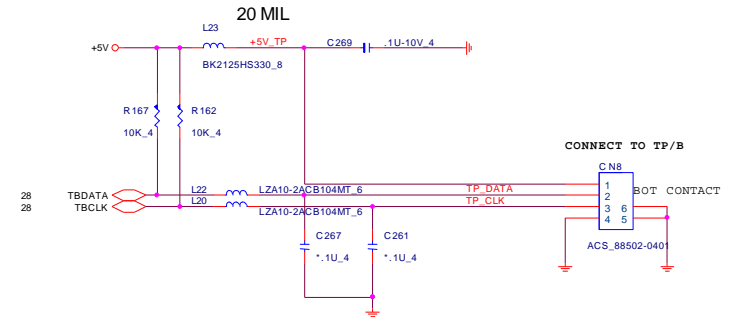


## Function Board

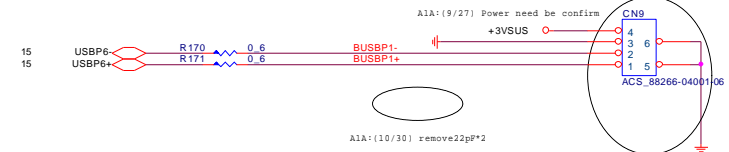


Keyboard Matrix	Button
MX0/MY16	acer EAP Button
MX1/MY16	acer EMAIL Button
MX2/MY16	acer WWW Button
MX3/MY16	acer EPM Button
MX4/MY16	WIRELESS Button
MX5/MY16	BLUETOOTH Button

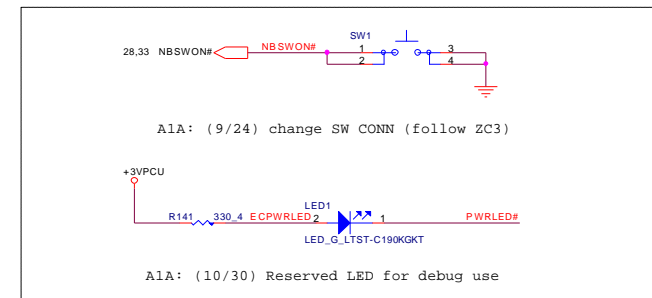
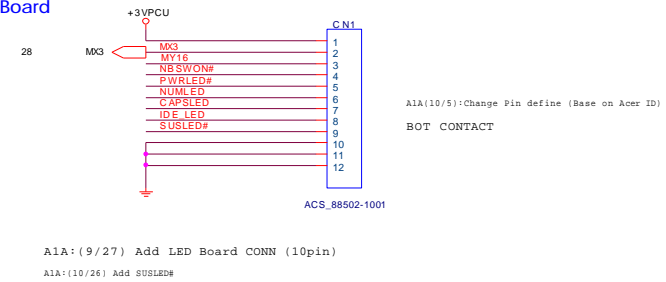
## TOUCH PAD



## Finger Printer

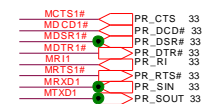
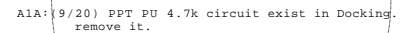


## LED Board



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**Quanta Computer Inc.**

Size	Document Number	Rev
	SWITCH,LED,KB,Finger,TP	1A
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OPEN : normal Device operation  
LOW : XOR pin tree

[illegible]

VIN

C333

0.1u/X7R-50V\_6

VIN

C33

0.1u/X7R-50V\_6

VIN

C35

0.1u/X7R-50V\_60.1u/X7R-50V\_6

VIN

C116

0.1u/X7R-50V\_6

VIN

C83

0.1u/X7R-50V\_6

VIN

C347

0.1u/X7R-50V\_6

VIN

C349

0.1u/X7R-50V\_6

VIN

C40

0.1u/X7R-50V\_60.1u/X7R-50V\_6

VIN

C39

0.1u/X7R-50V\_6

VIN

C447

0.1u/X7R-50V\_6

+3VPCU

C443

.1u-10V\_4

+3VPCU

C103

.1u-10V\_4

+3VPCU

C32

.1u-10V\_4

**LINE OUT Amplifier**

A1A:(9/20) Refer to ZD1,  
change R580,R581 to 10k

A1A:(10/5) Refer to ZD1,  
change R585,R586 to 10k

A1A:(9/28) BNC suggest to change from AGND to GND

A1A:(9/21)  
refer to ZD1,  
add it.

Change C19 to 4.7u

**SYS / EZ MIC**  
**SYS Line-in**  
**EZ Line-in**  
**SYS/EZ Line-out**  
**EZ MIC (reserve)**

SN74LVC1G68DCKR

**MDC**

A1A:(10/13) change R598 from 22ohm to 33 ohm

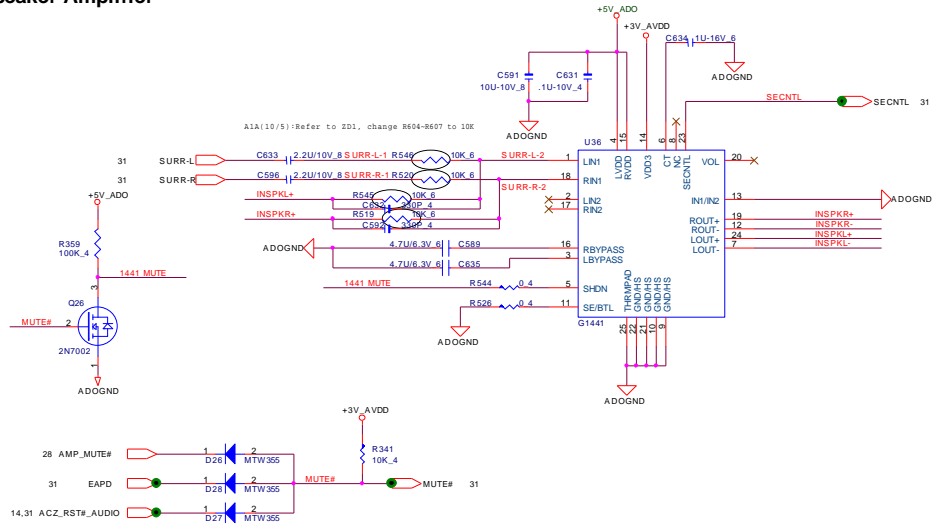
A1A:(9/27)change P/M (follow ZC3)

**PROJECT : ZU1**  
**Quanta Computer Inc.**

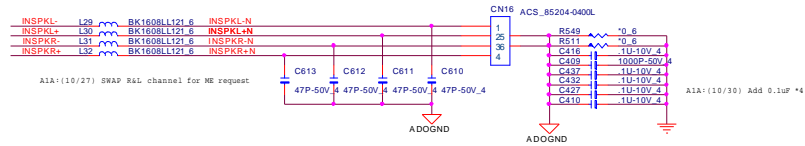
Size: Document Number  
**AUDIO(ALC268)/AMP/MDC**

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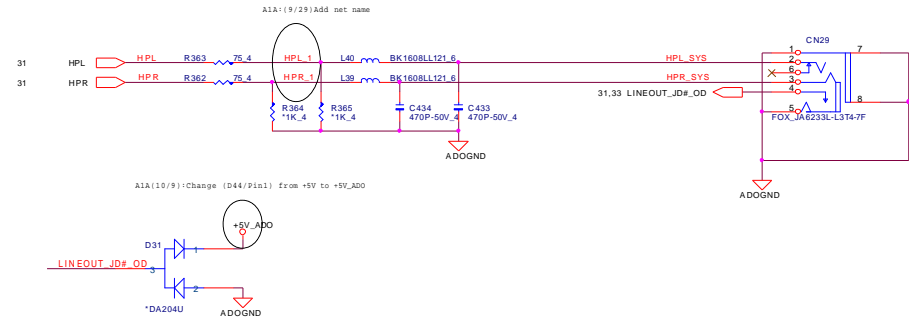
## Speaker Amplifier



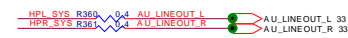
## SPEAKER



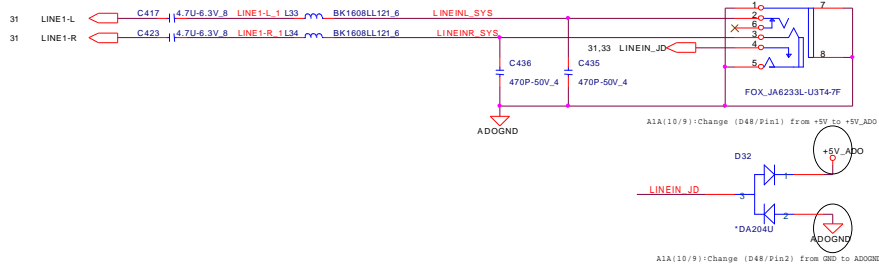
## SYSTEM LINE OUT



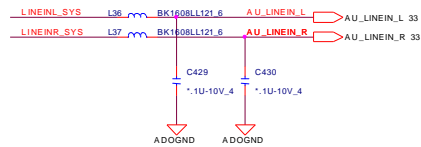
## Docking LINE OUT/SPDIF



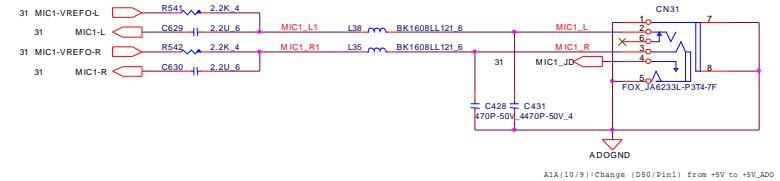
## SYSTEM LINE IN



## Docking LINE IN



## SYSTEM MIC



## Docking MIC

