

Compal Confidential

DCL56 Schematics Document

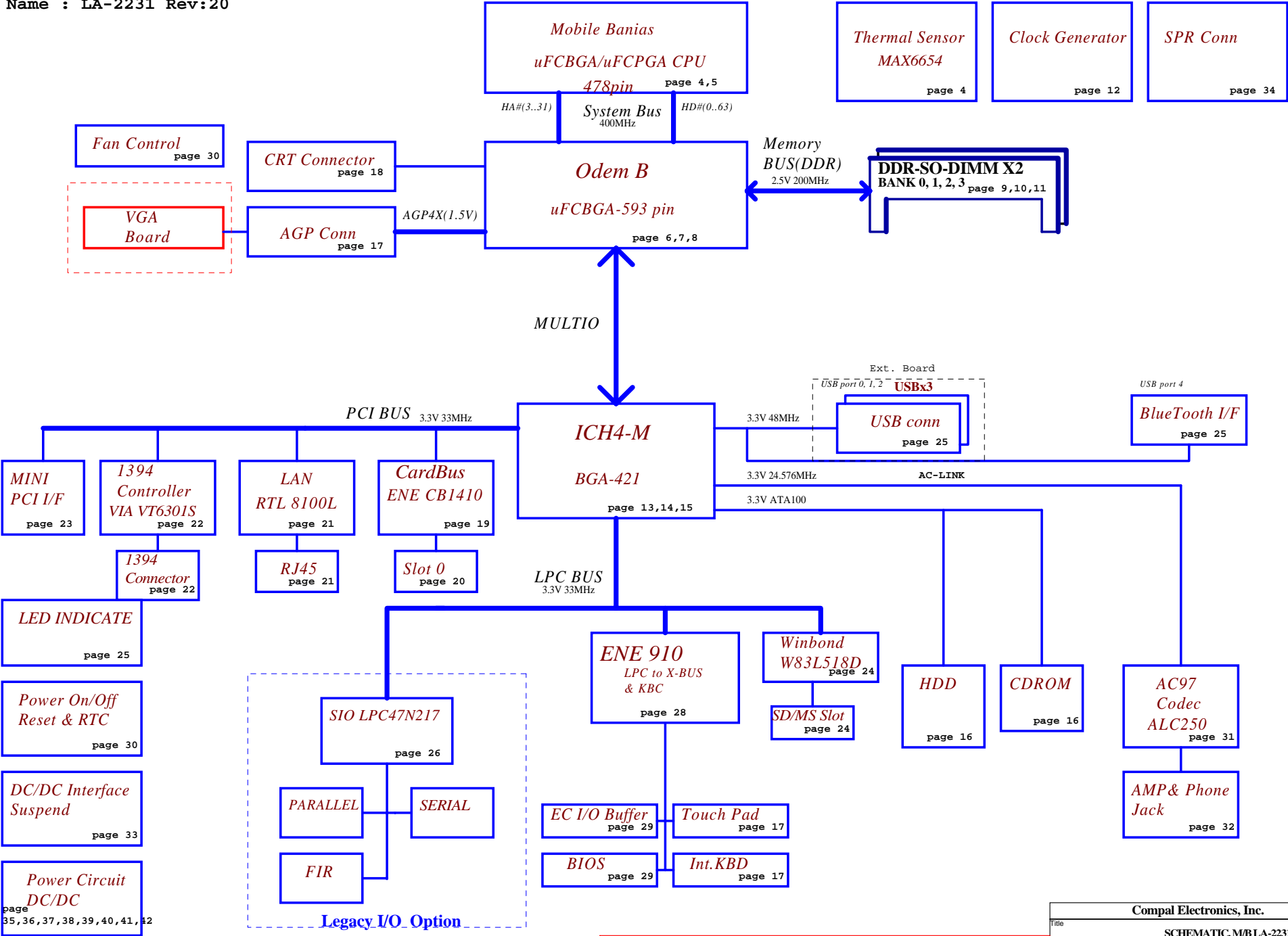
Banias uFCBGA/uFCPGA Package with Odem Core Logic

2004-05-07 for MP

REV:20

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Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V rail for Processor I/O	ON	OFF	OFF
+1.2VS	1.2VS switched power rail for MCH	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VALW	1.5V power rail	ON	ON	ON
+1.5V	1.5V power rail	ON	ON	OFF
+1.5VS	AGP 4X	ON	OFF	OFF
+1.8VALW	1.8V power rail	ON	ON	ON*
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Board ID Table

BID2	BID1	BID0	PCB Revision
0	0	0	0.1
0	0	1	0.2
0	1	0	0.3
0	1	1	0.4
1	0	0	
1	0	1	
1	1	0	
1	1	1	

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
VGA			PIRQA
CardBus	AD19	2	PIRQC
LAN	AD17	3	PIRQD
Mini-PCI	AD18,AD22	1/4	PIRQC/PIRQD
1394	AD16	0	PIRQB

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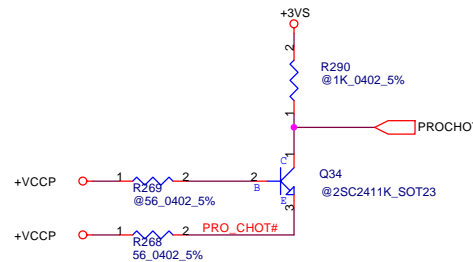
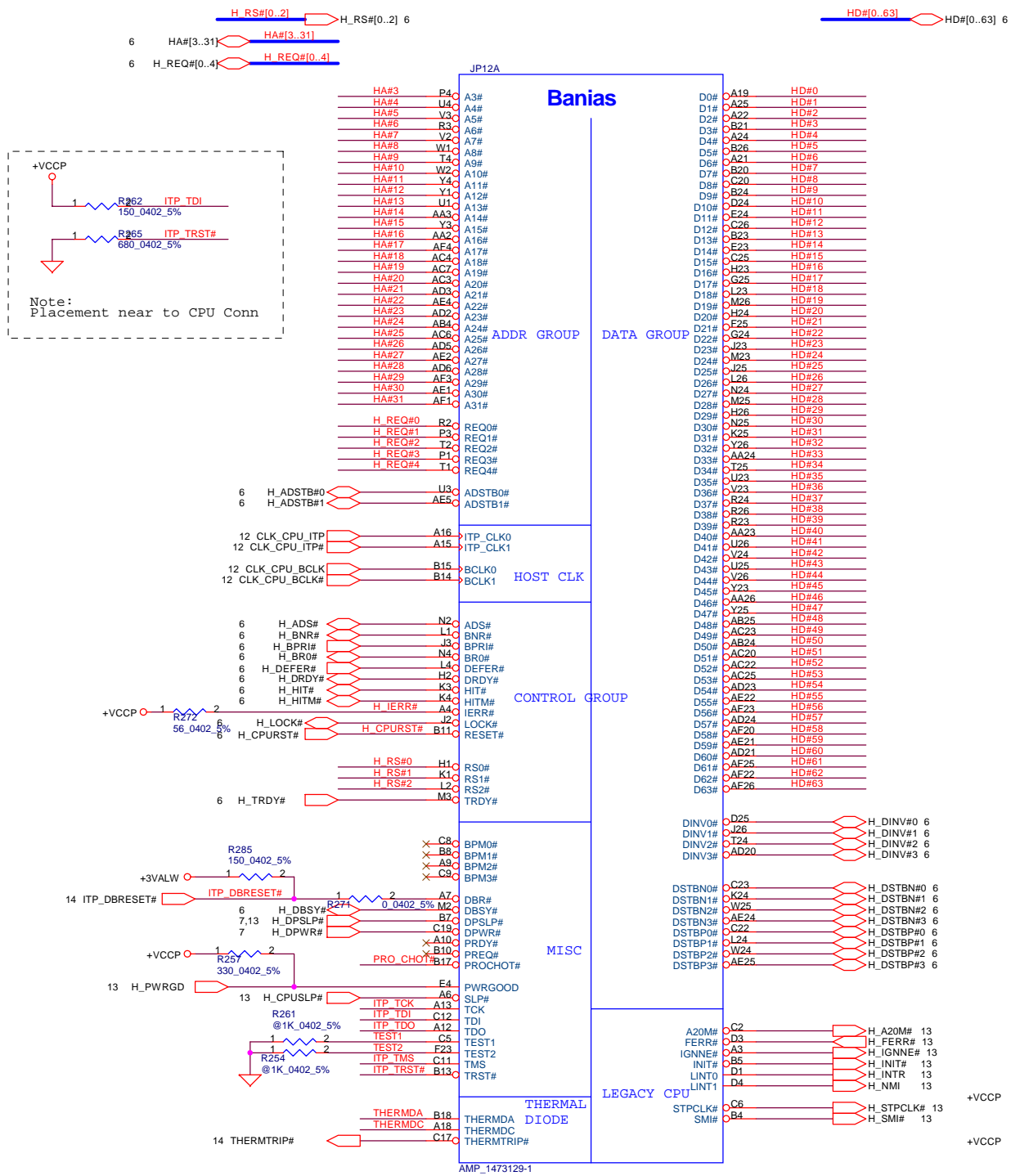
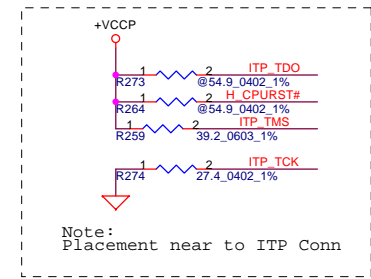
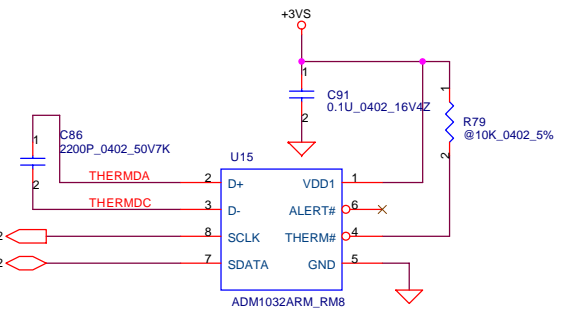
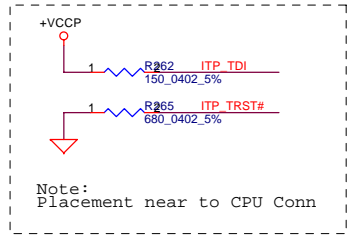
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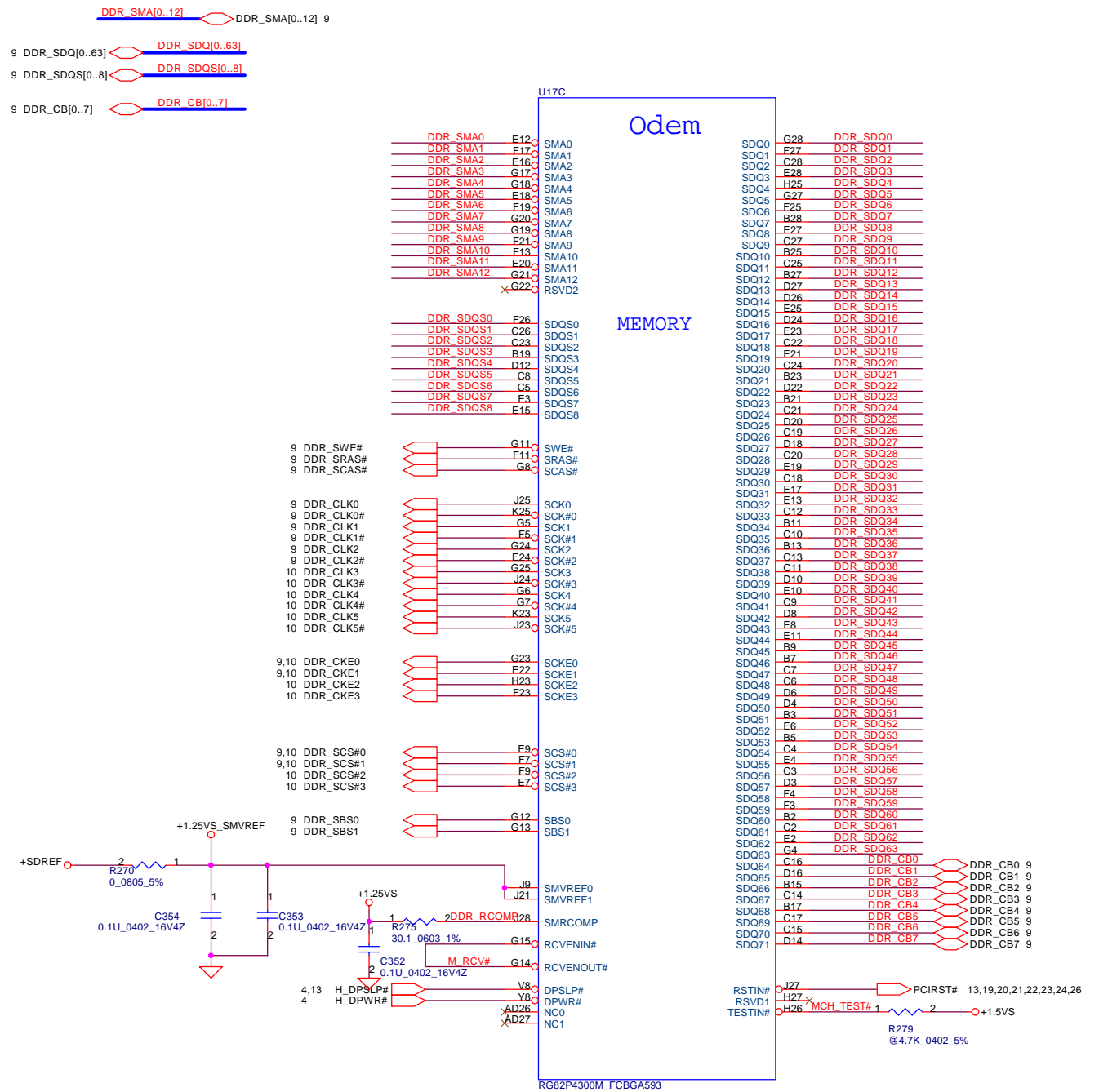
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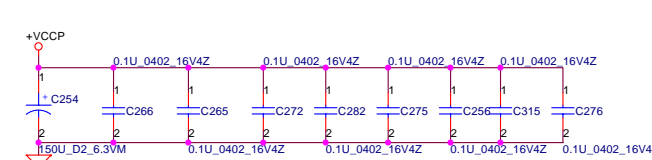
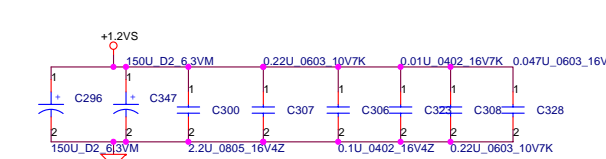
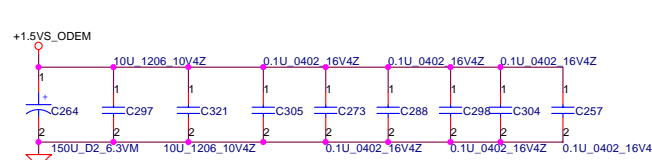
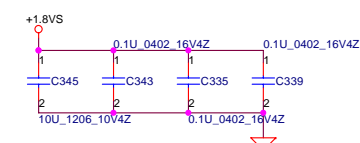
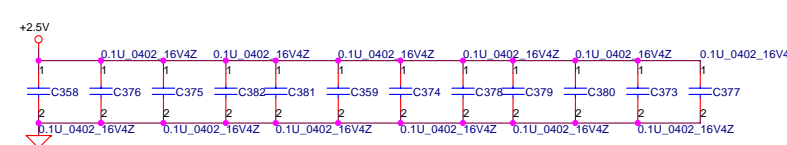
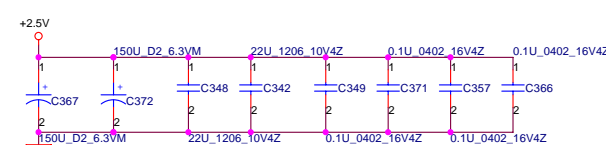
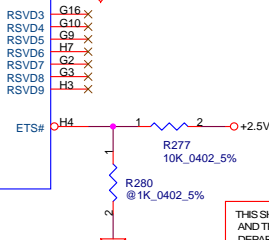
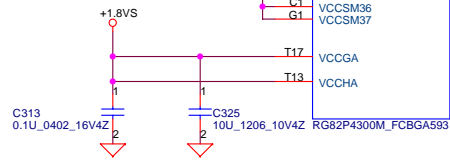
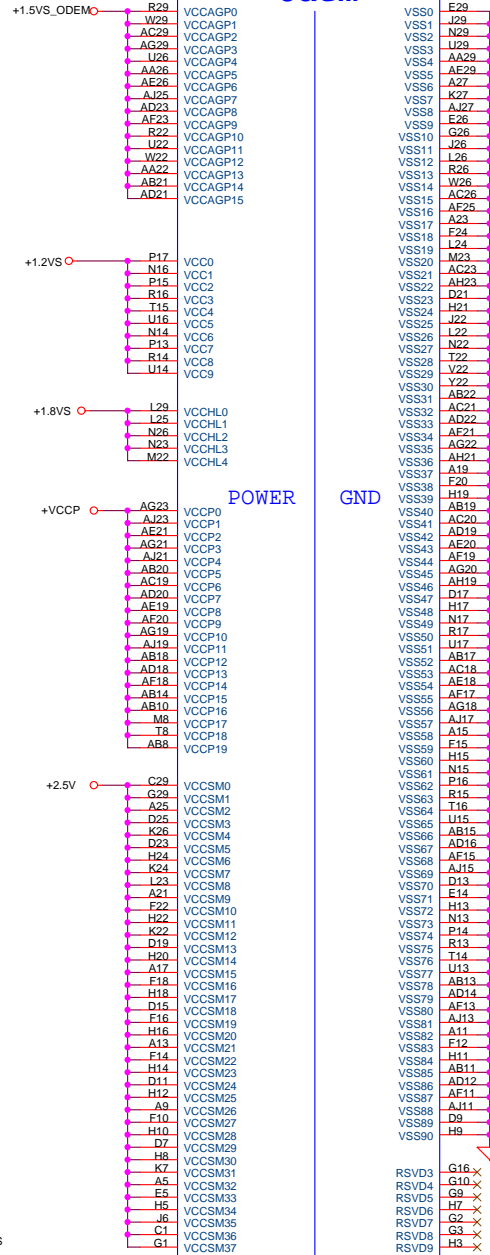
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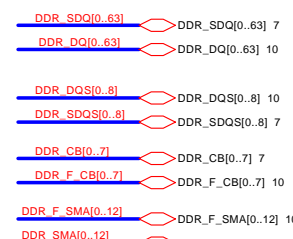
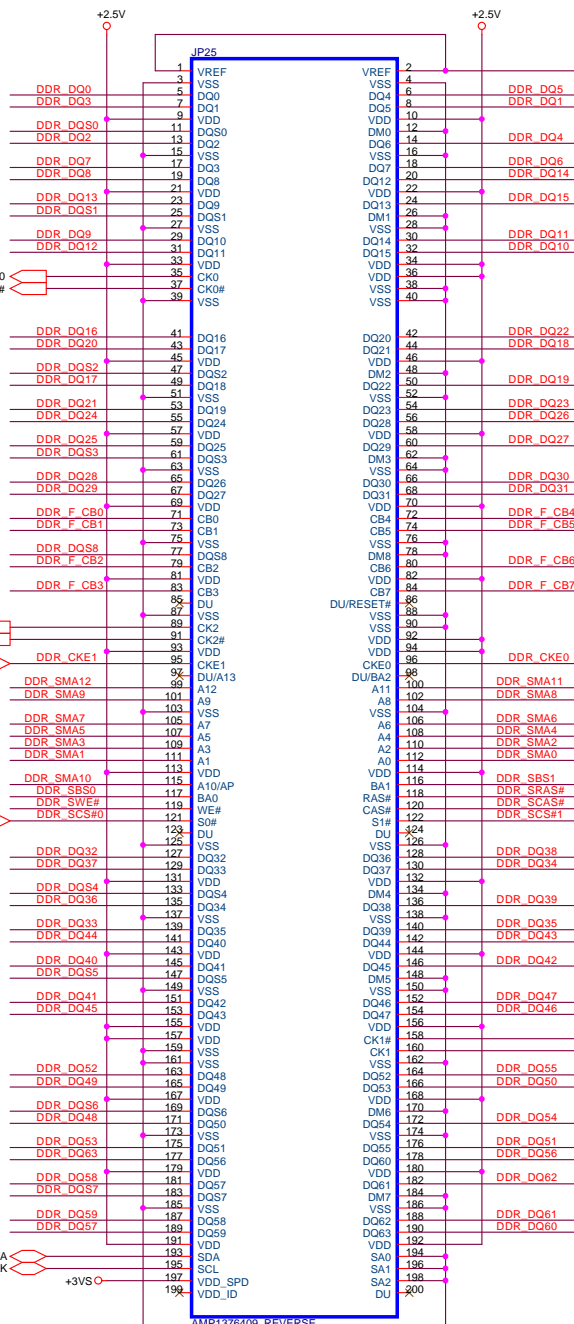
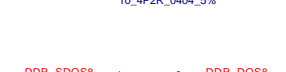
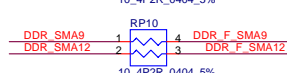
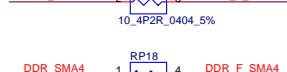
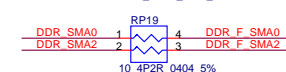
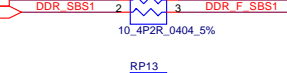
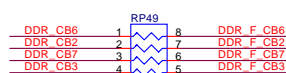
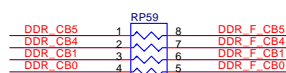
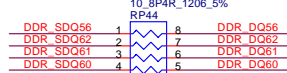
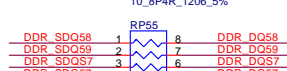
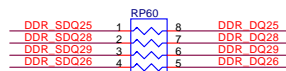
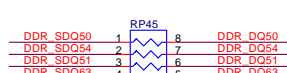
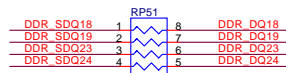
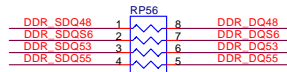
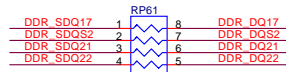
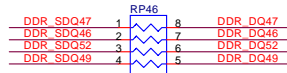
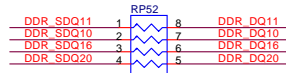
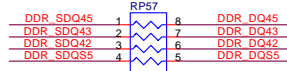
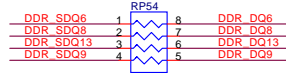
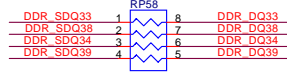
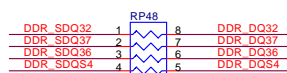
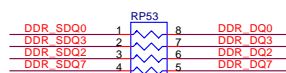
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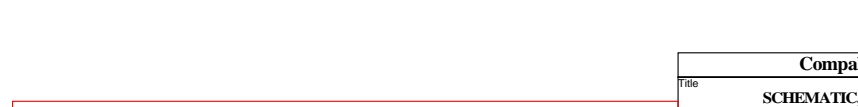
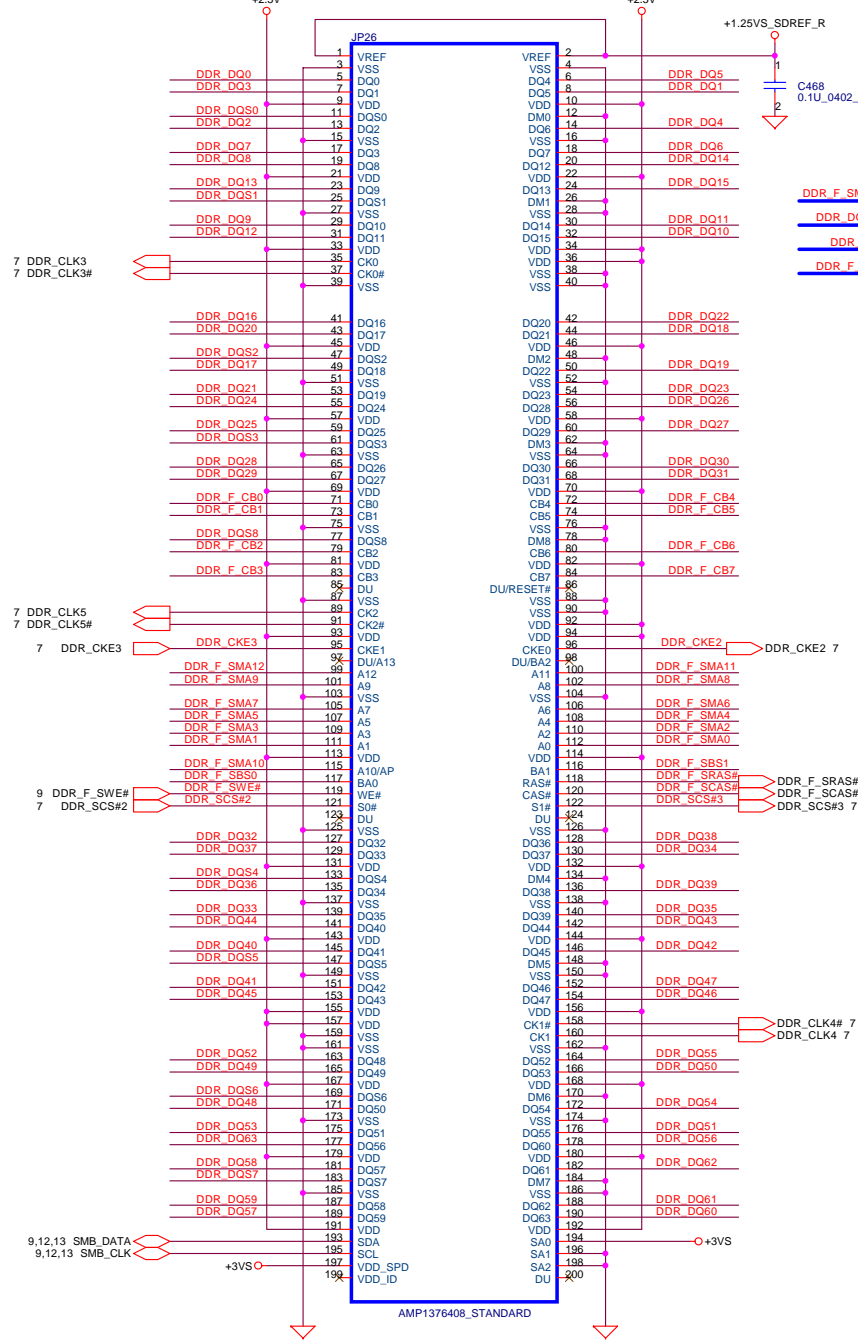
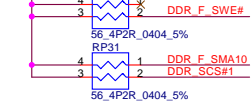
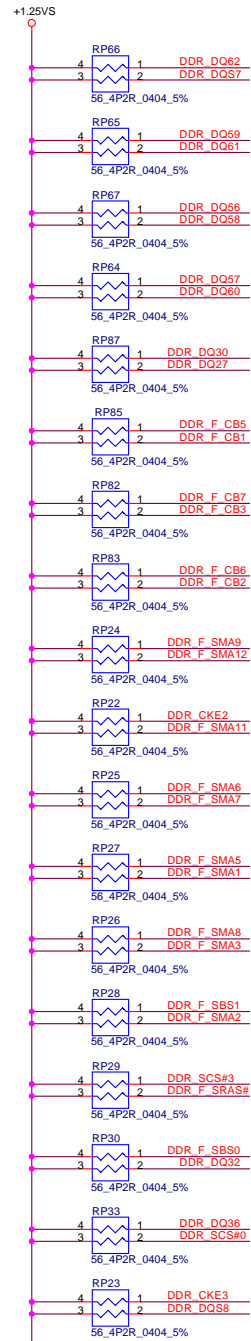
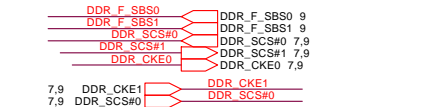
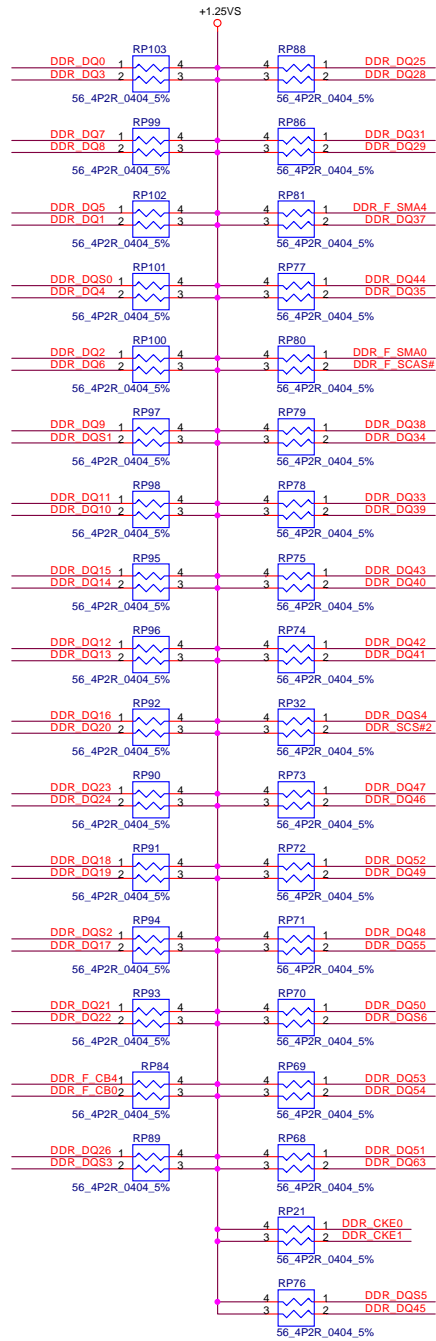
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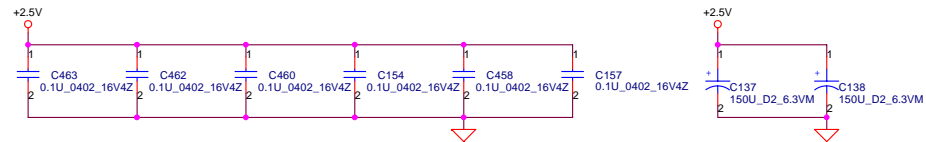
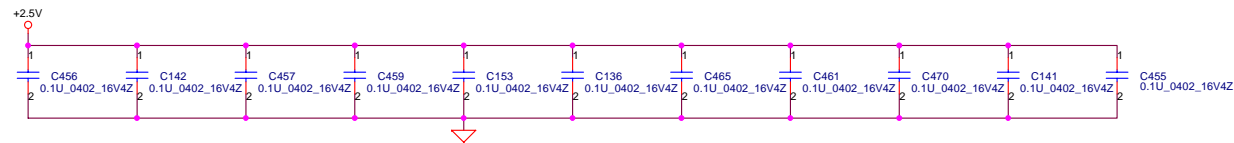
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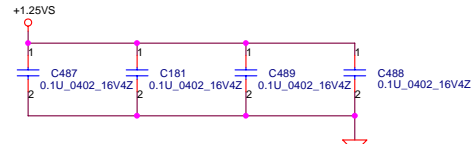
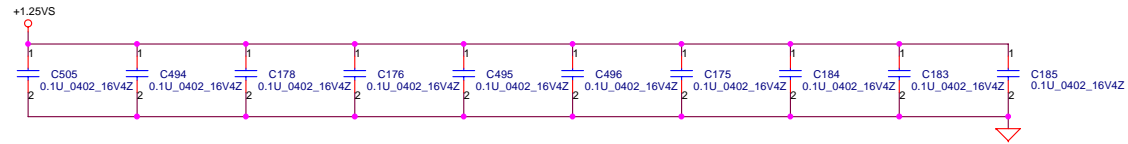
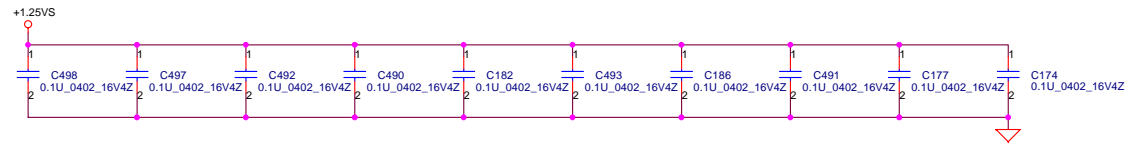
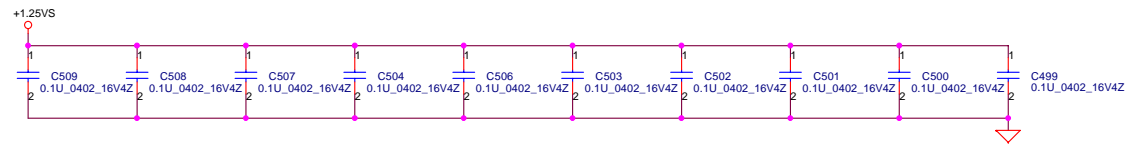
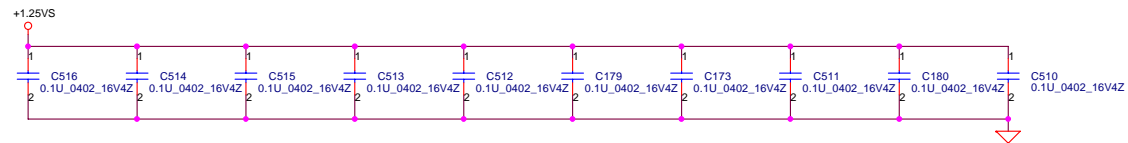
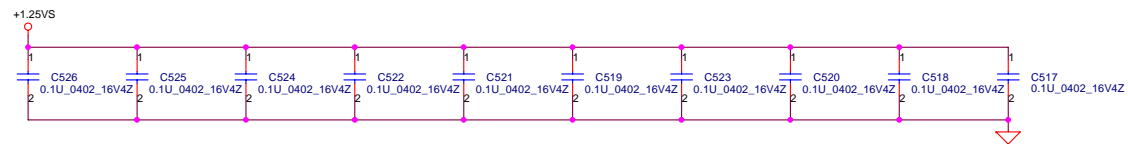
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Layout note :
Distribute as close as possible
to DDR-SODIMM.



Layout note :
Place one cap close to every 2 pull up resistors termination to
+1.25V

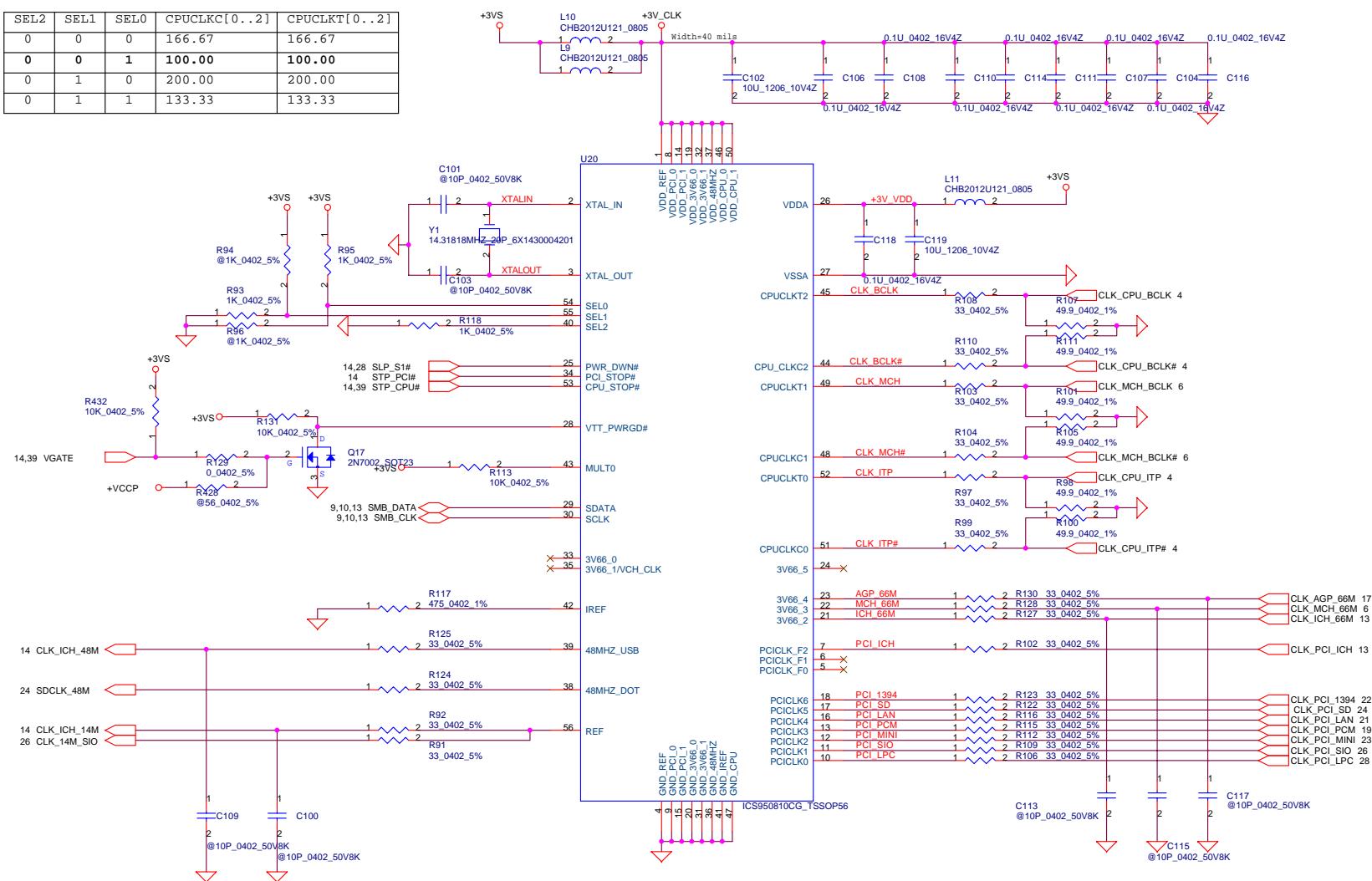


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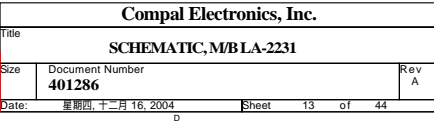
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Clock Generator

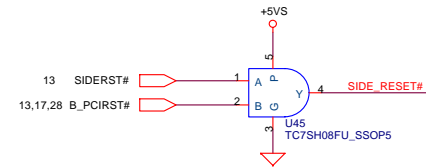
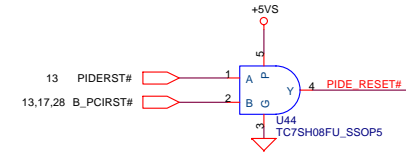
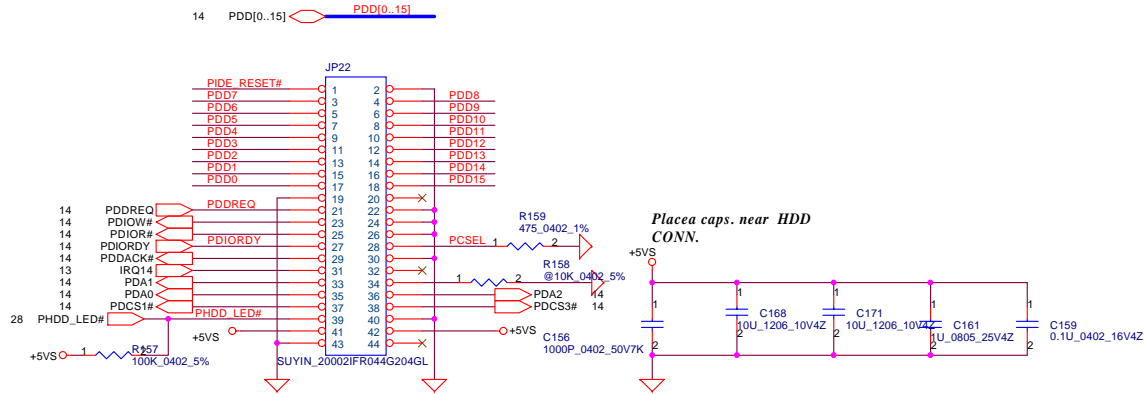
SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
0	0	0	166.67	166.67
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33



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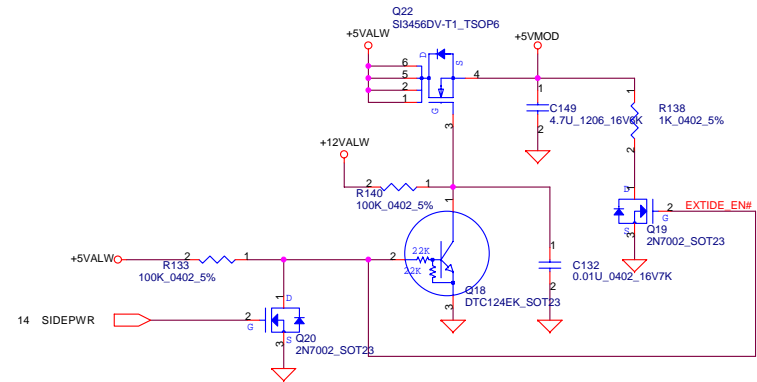
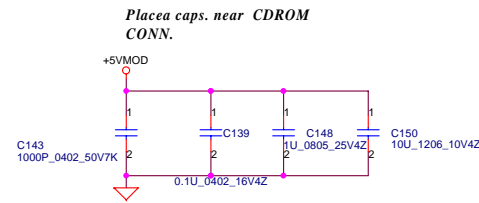
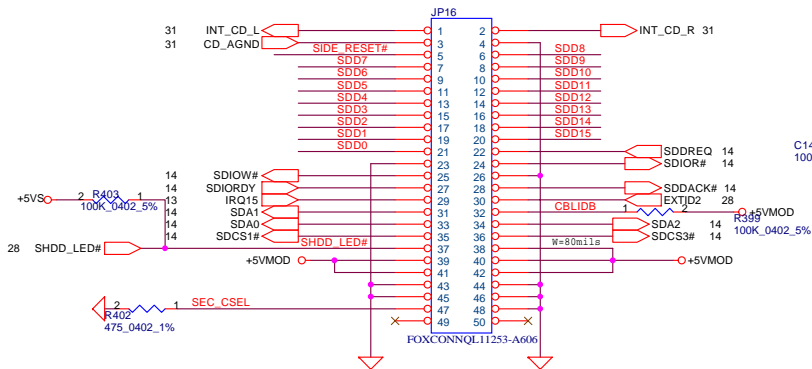


HDD Connector



CD-ROM Connector

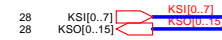
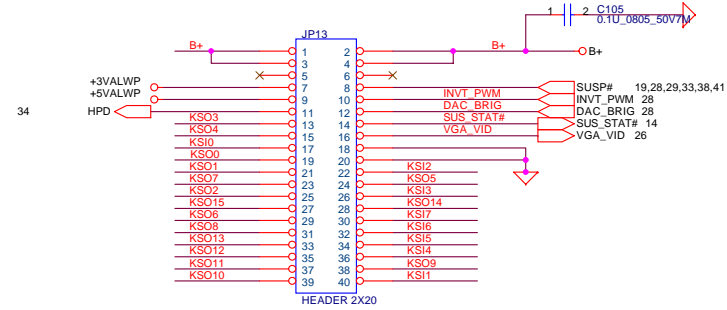
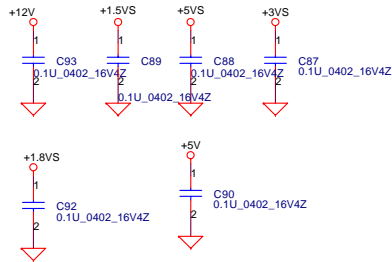
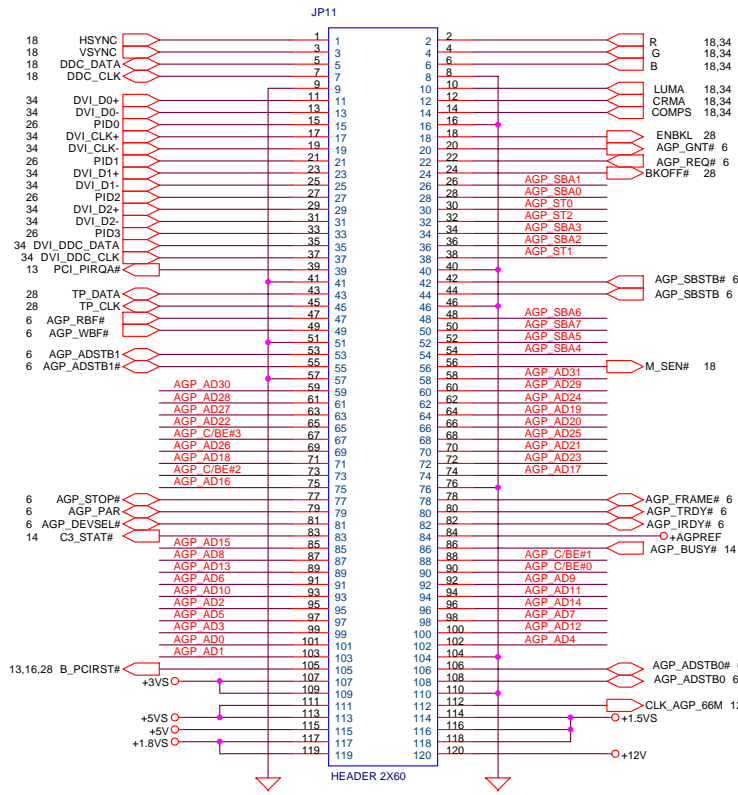
SDD[0..15]



SI3456DV: N CHANNEL
VGS: 4.5V, RDS: 65 mOHM
Id(MAX): 5.1A
VGS,+20V

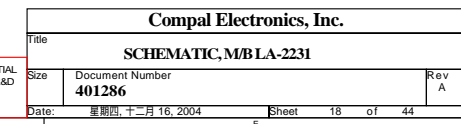
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13,21,22,23 PCI_AD[0..31]

PCI_AD31 3
PCI_AD30 4
PCI_AD29 5
PCI_AD28 7
PCI_AD27 8
PCI_AD26 9
PCI_AD25 10
PCI_AD24 11
PCI_AD23 15
PCI_AD22 16
PCI_AD21 17
PCI_AD20 19
PCI_AD19 23
PCI_AD18 24
PCI_AD17 25
PCI_AD16 26
PCI_AD15 38
PCI_AD14 39
PCI_AD13 40
PCI_AD12 43
PCI_AD11 45
PCI_AD10 46
PCI_AD9 47
PCI_AD8 49
PCI_AD7 51
PCI_AD6 52
PCI_AD5 53
PCI_AD4 54
PCI_AD3 55
PCI_AD2 56
PCI_AD1 57
AD0

PQFP 144
22.2 X 22.2 X 1.60

13,21,22,23 PCI_C/BE#3 12
13,21,22,23 PCI_C/BE#2 27
13,21,22,23 PCI_C/BE#1 37
13,21,22,23 PCI_C/BE#0 48
C/BE#3
C/BE#2
C/BE#1
C/BE#0

7,13,20,21,22,23,24,26 PCIRST# 20
13,21,22,23 PCI_FRAME# 28
13,21,22,23 PCI_IRDY# 29
13,21,22,23 PCI_TRDY# 32
13,21,22,23 PCI_DEVSEL# 33
13,21,22,23 PCI_STOP# 34
13,21,22,23 PCI_PERR# 35
13,21,23 PCI_SERR# 36
13,21,23 PCI_PAR# 38
13 PCI_REQ# 1
13 PCI_GNT#2 2
12 CLK_PCI_PCM 21
RST#
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
PERR#
SERR#
PAR#
REQ#
GNT#
CLK

+3V
R227 10K_0402_5%
D16 @RB751V_SOD323

CLK_PCI_PCM
R250 10_0402_5%
C319 18P_0402_50V8K

17,28,29,33,38,41 SUSP#
21,22,23,28 PCM_PME#
PCI_AD19
13,23 PCI_PIRQ#
28 PCM_RI#
13,24,26,28 SIRQ#
14,23,26,28 PM_CLKRUN#
20 CBRST#
RI_OUT#/PME#
SUSPEND#
IDSEL
MFUNC0
MFUNC1
MFUNC2
MFUNC3
MFUNC4
MFUNC5
MFUNC6
VCC/GRST#

GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
RSVD/D14
RSVD/A18
RSVD/D2

CAD31/D10 144
CAD30/D9 142
CAD29/D1 141
CAD28/D8 140
CAD27/D0 139
CAD26/A0 129
CAD25/A1 128
CAD24/A2 127
CAD23/A3 124
CAD22/A4 121
CAD21/A5 120
CAD20/A6 118
CAD19/A25 116
CAD18/A7 115
CAD17/A24 113
CAD16/A17 98
CAD15/IOWR# 96
CAD14/A9 97
CAD13/IORD# 93
CAD12/A11 95
CAD11/OE# 92
CAD10/CE2# 91
CAD9/A10 89
CAD8/A15 87
CAD7/D7 85
CAD6/D13 82
CAD5/D6 83
CAD4/D12 80
CAD3/D5 81
CAD2/D11 77
CAD1/D4 79
CAD0/D3 76
S1_D10
S1_D9
S1_D1
S1_D8
S1_D0
S1_A0
S1_A1
S1_A2
S1_A3
S1_A4
S1_A5
S1_A6
S1_A25
S1_A7
S1_A24
S1_A17
S1_IOWR#
S1_A9
S1_IORD#
S1_OE#
S1_CE2#
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S1_D11
S1_D4
S1_D3

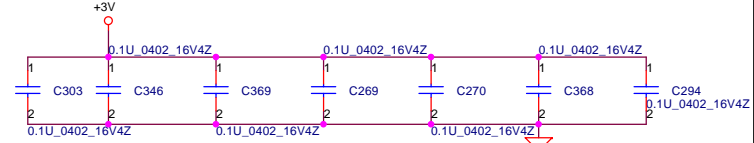
CC/BE3#/REG# 125
CC/BE2#/A12 112
CC/BE1#/A8 99
CC/BE0#/CE1# 88
S1_REG#
S1_A12
S1_A8
S1_CE1#

CRST#/RESET 119
CFRAME#/A23 111
CIRDY#/A15 110
CTRDY#/A22 109
CDEVSEL#/A21 107
CSTOP#/A20 105
CPERR#/A14 104
CSERR#/WAIT# 133
CPAR#/A13 101
CREQ#/INPACK# 123
CGNT#/WE# 106
CCLK/A16 108
S1_RST
S1_A23
S1_A15
S1_A22
S1_A21
S1_A20
S1_A14
S1_WAIT#
S1_A13
S1_INPACK#
S1_WE#
A16 CLK
S1_BVD1
S1_BVD2
S1_WP
S1_A19
S1_RDY#
PCM_SPK#
S1_BVD2

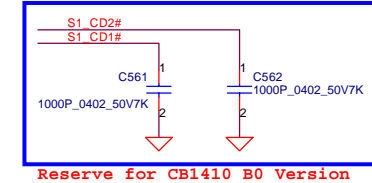
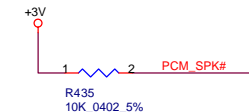
CSTSCHG/BVD1 135
CCLKRUN#/WP 136
CBLOCK#/A19 103
CINT#/READY 132
SPKOUT 62
CAUDIO/BVD2 134
S1_REG#
S1_A12
S1_A8
S1_CE1#
S1_RST
S1_A23
S1_A15
S1_A22
S1_A21
S1_A20
S1_A14
S1_WAIT#
S1_A13
S1_INPACK#
S1_WE#
A16 CLK
S1_BVD1
S1_BVD2
S1_WP
S1_A19
S1_RDY#
PCM_SPK#
S1_BVD2

CCD2#/CD2# 137
CCD1#/CD1# 125
CVS2/V2# 117
CVS1/V1# 131
S1_CD2#
S1_CD1#
S1_VS2
S1_VS1

CB1410_LQFP144
S1_D2
S1_A18
S1_D14



S1_A[0..25]
S1_D[0..15]



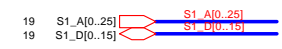
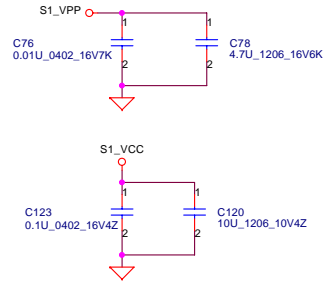
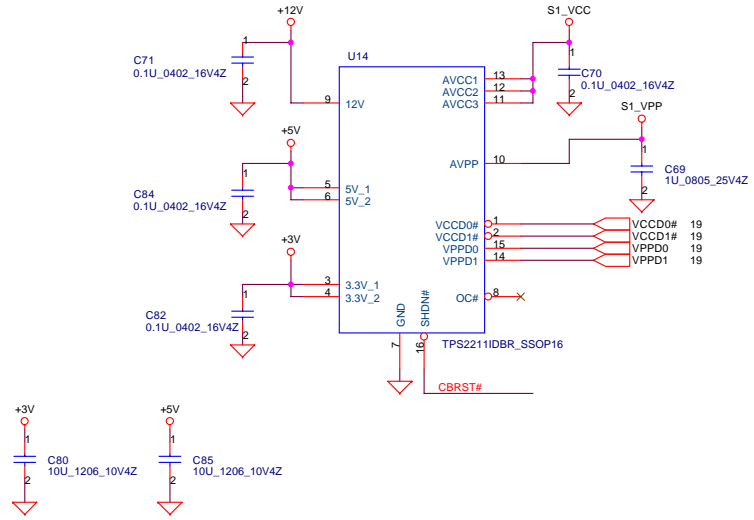
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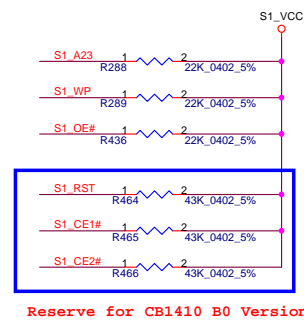
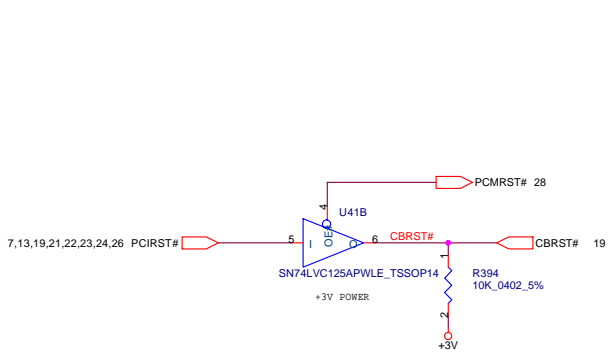
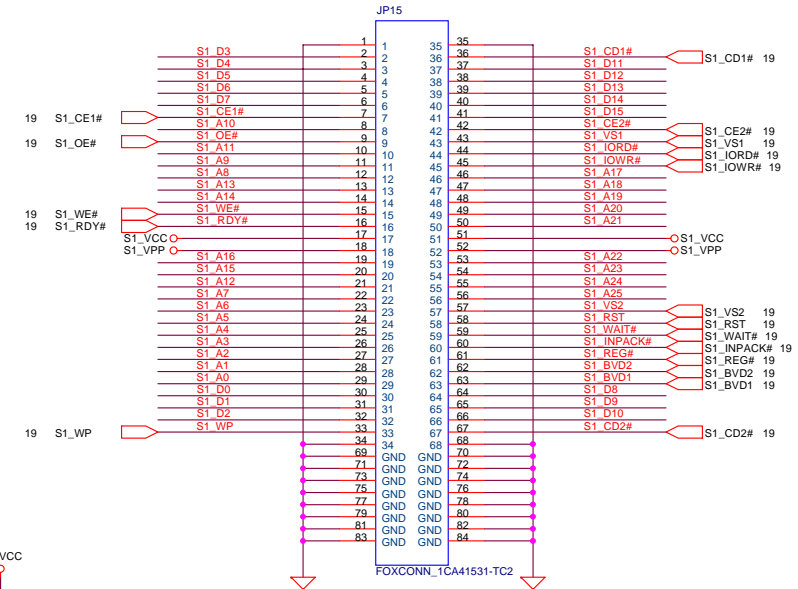
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PCMCIA Power Controller



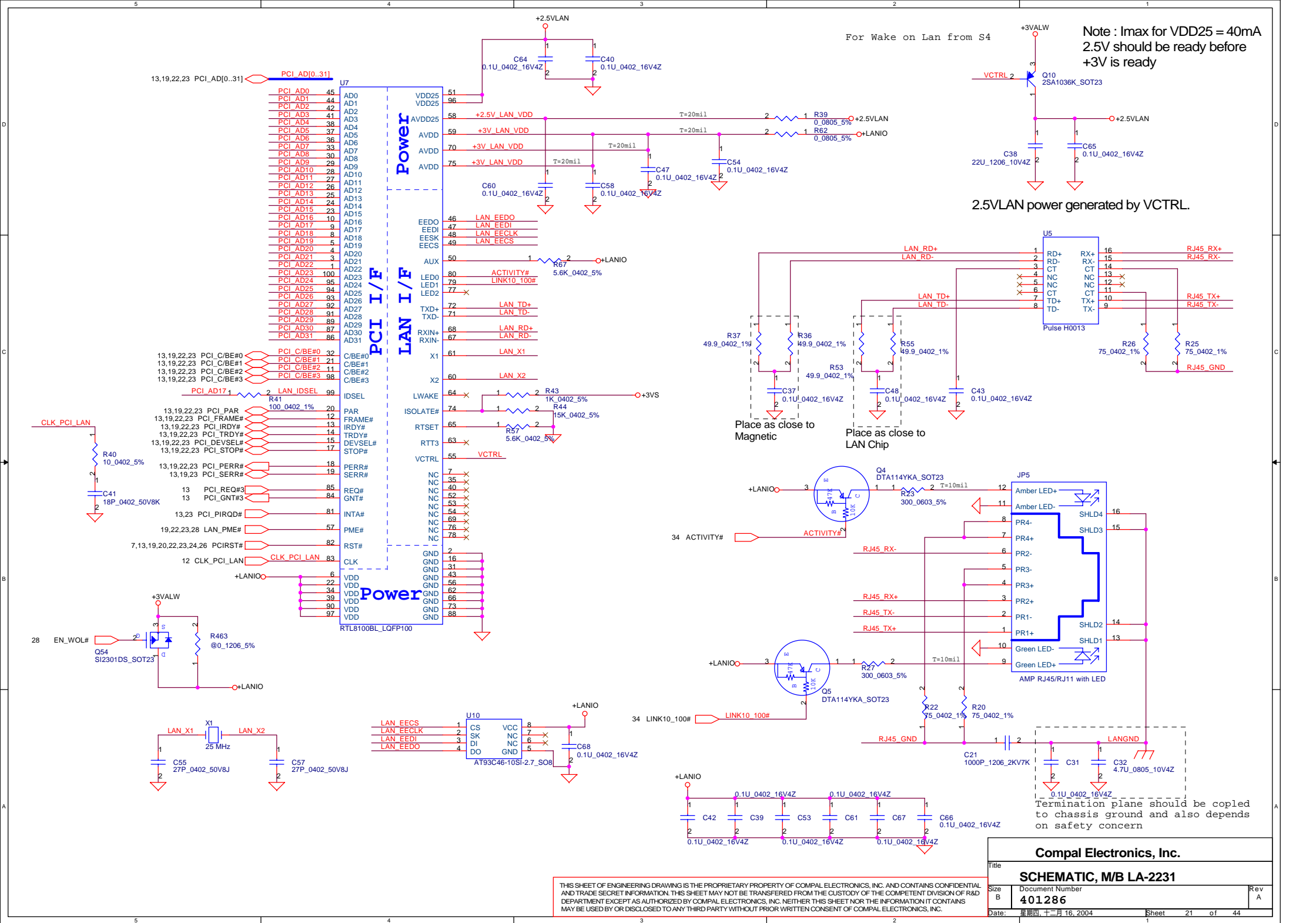
CardBus Socket



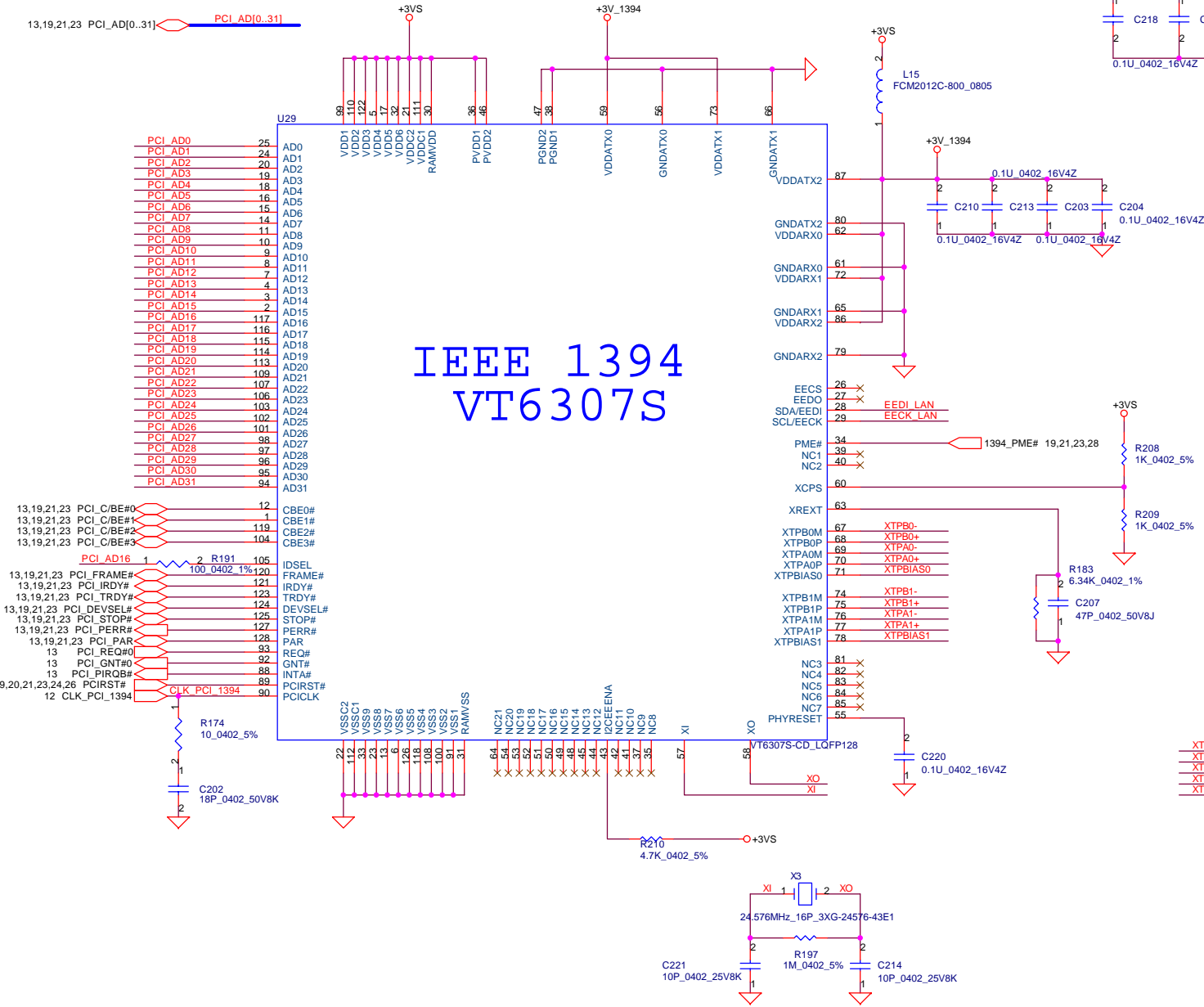
Reserve for CB1410 B0 Version

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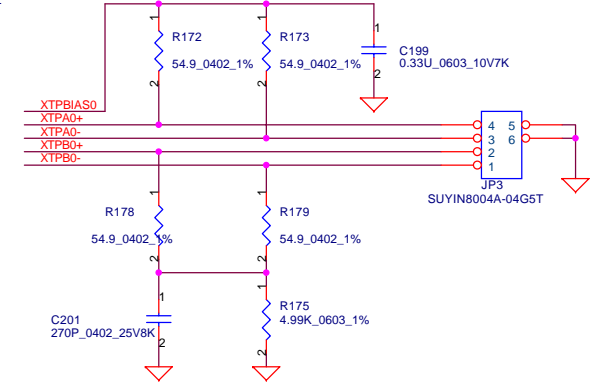
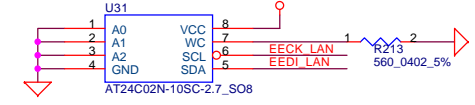
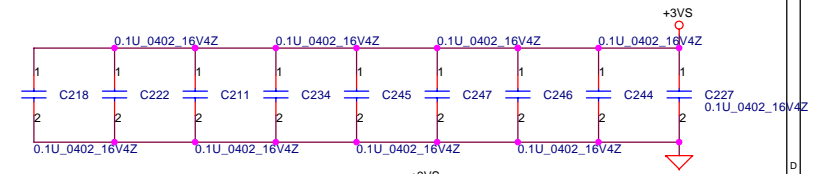
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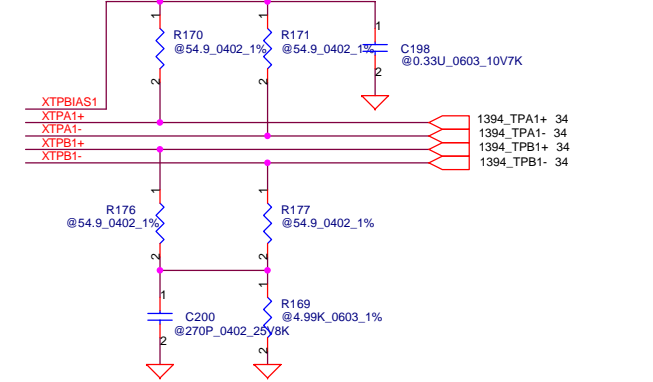
13,19,21,23 PCI_AD[0..31] PCI_AD[0..31]



IEEE 1394
VT6307S



Note: These components need to be close to chip pins.

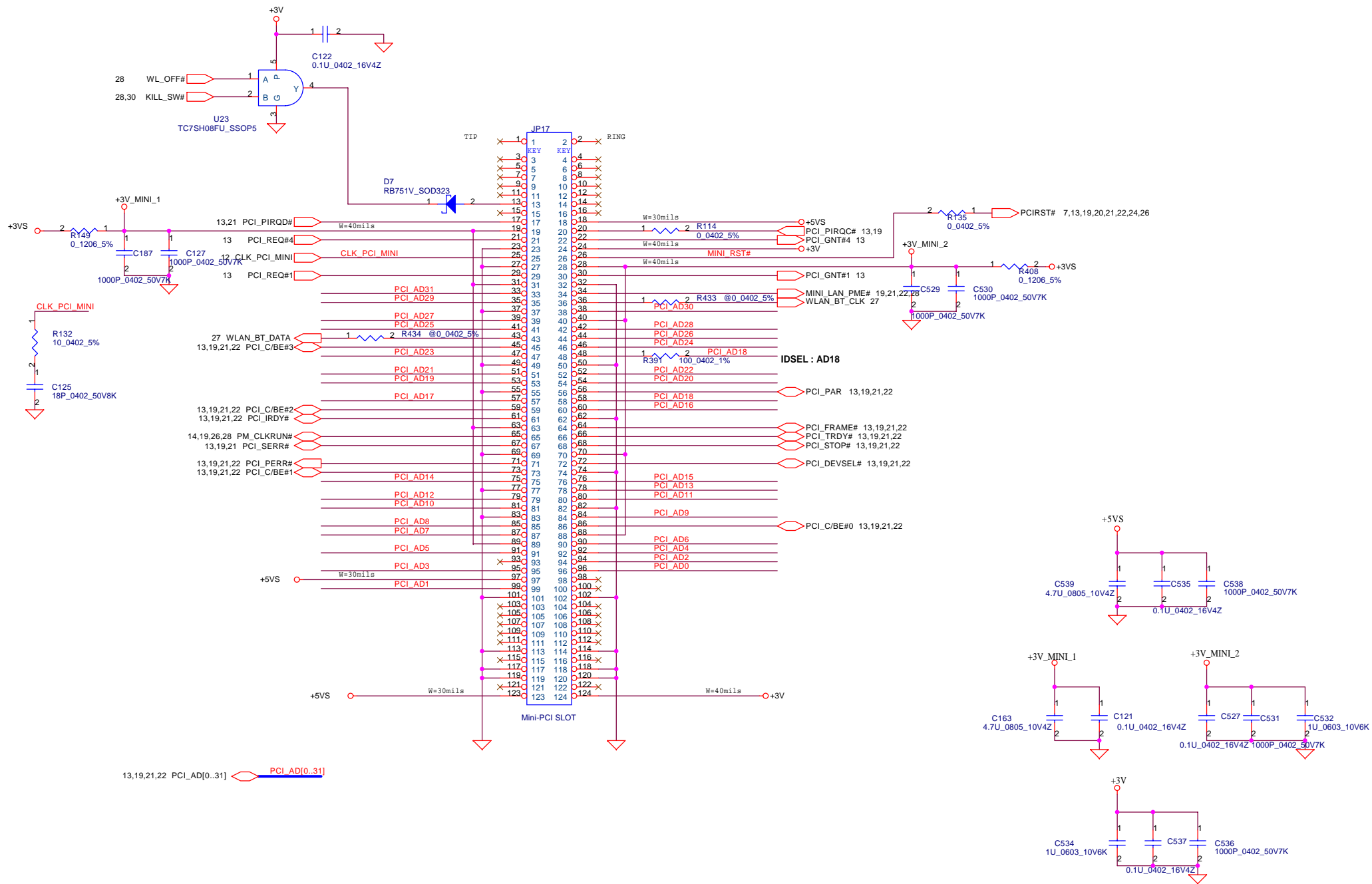


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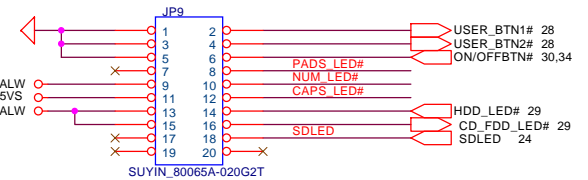
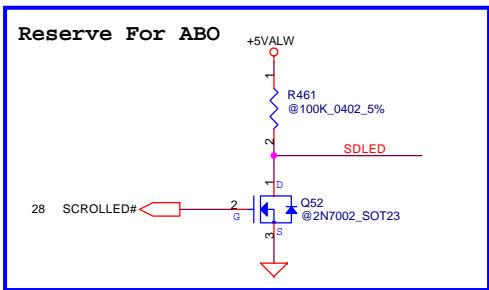
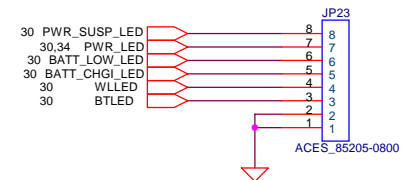
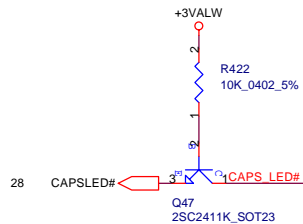
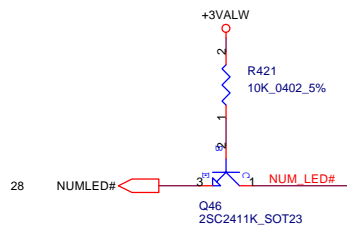
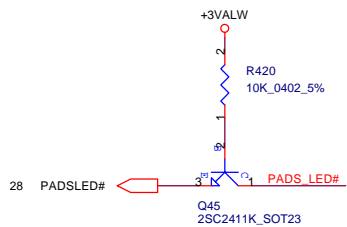
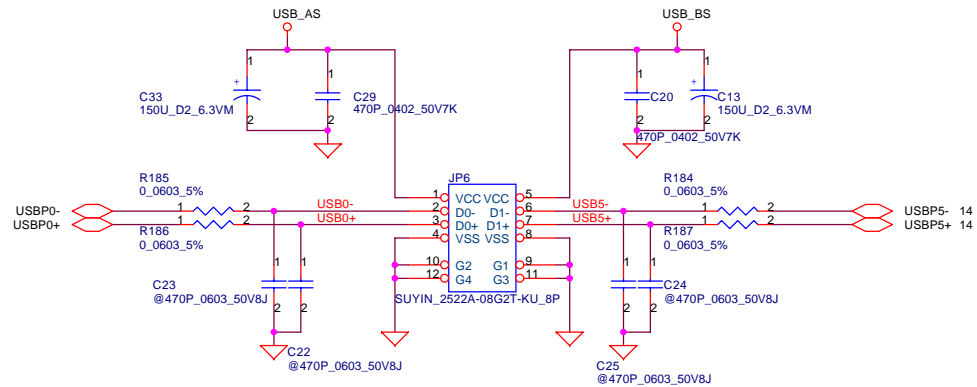
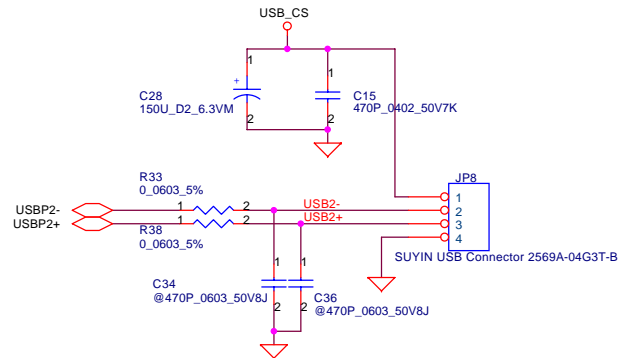
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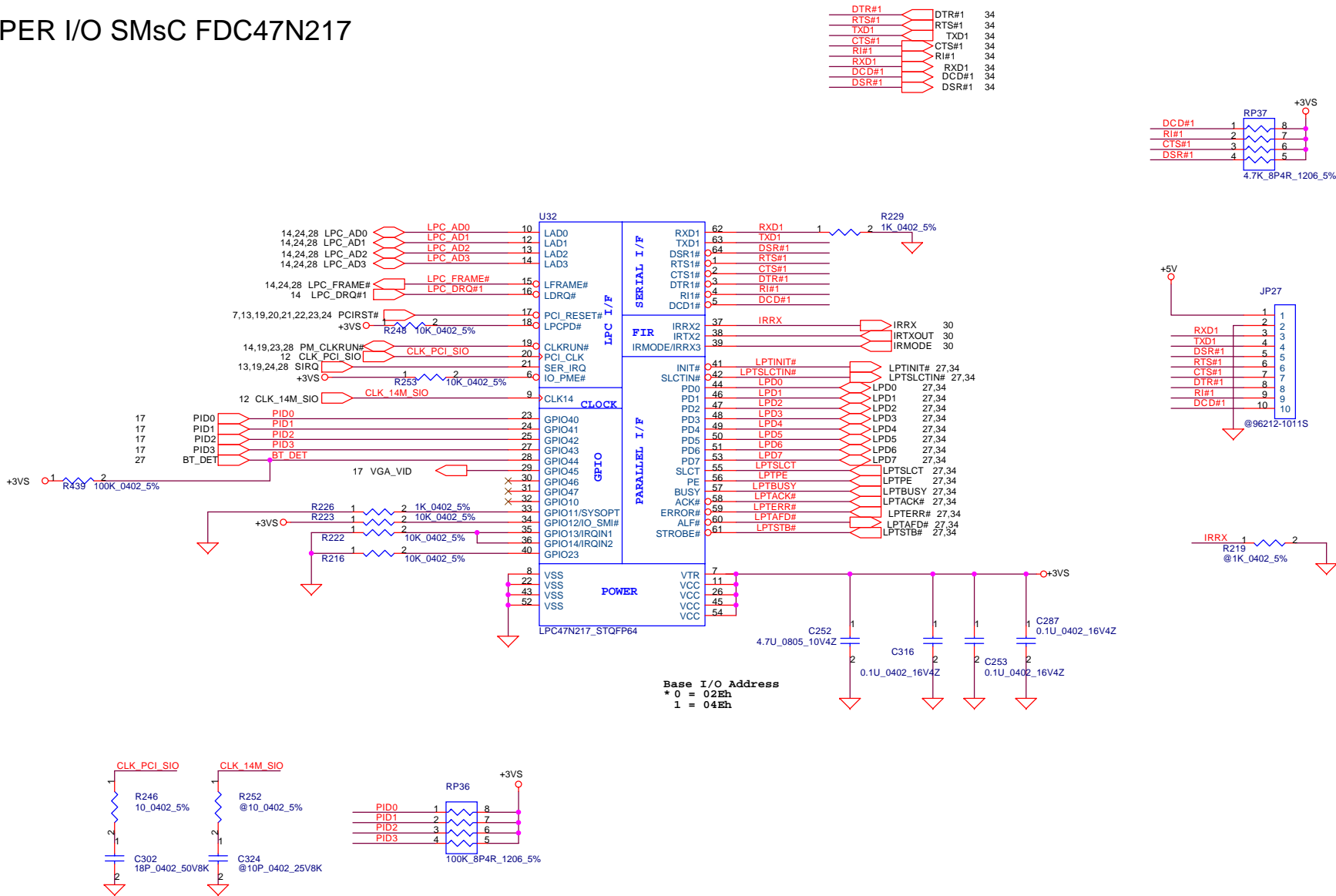
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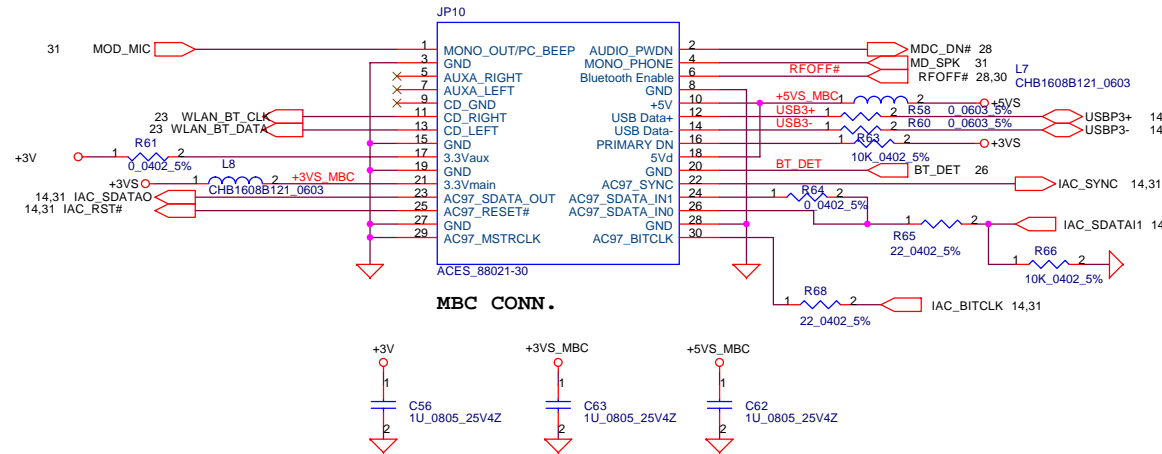


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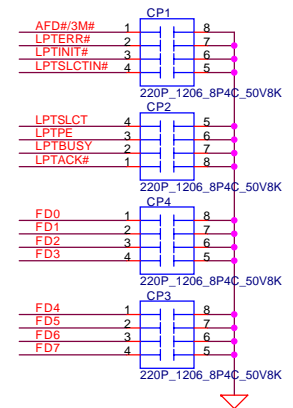
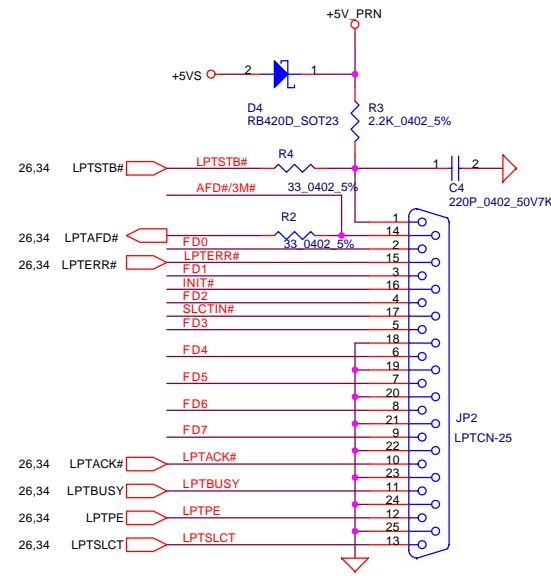
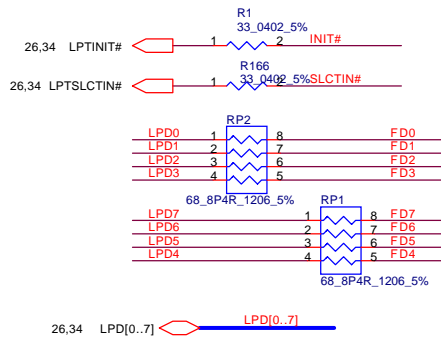
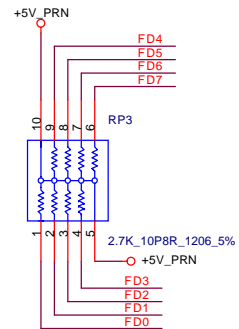
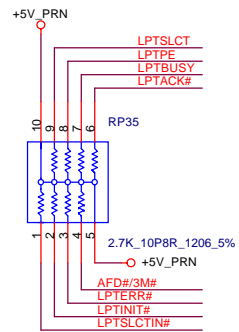
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SUPER I/O SMsC FDC47N217





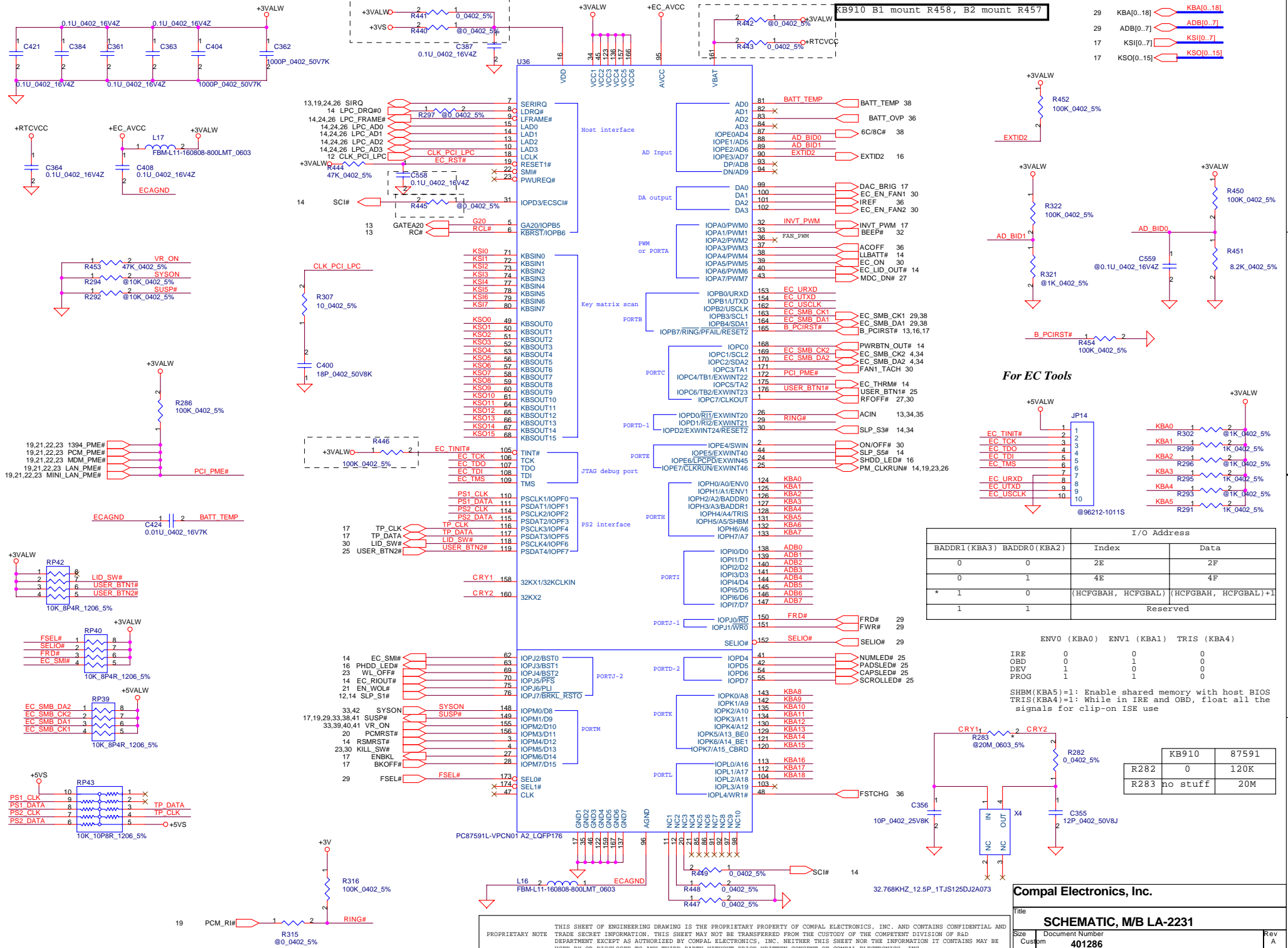
PARALLEL PORT



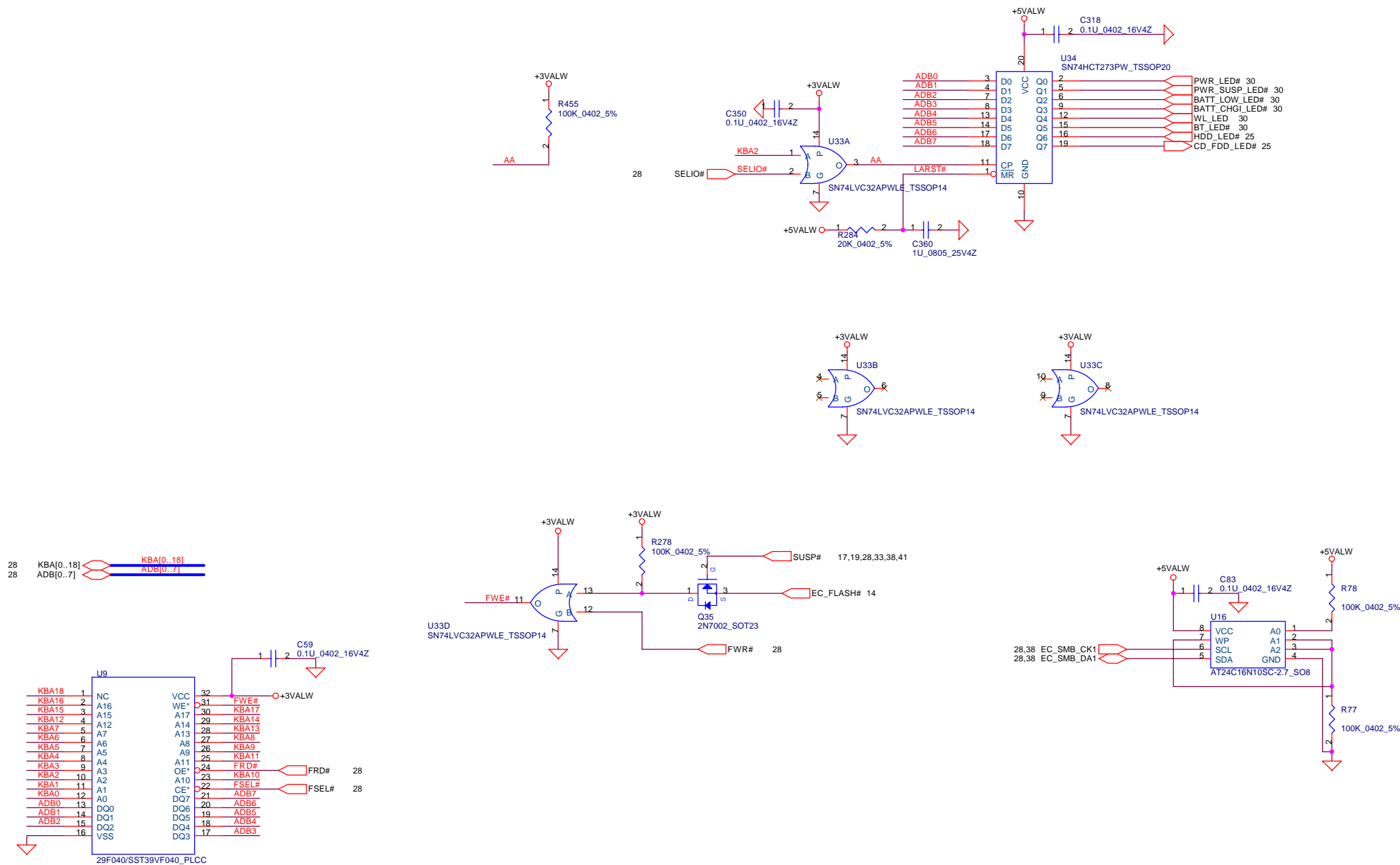
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SCHEMATIC, M/B LA-2231

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401286

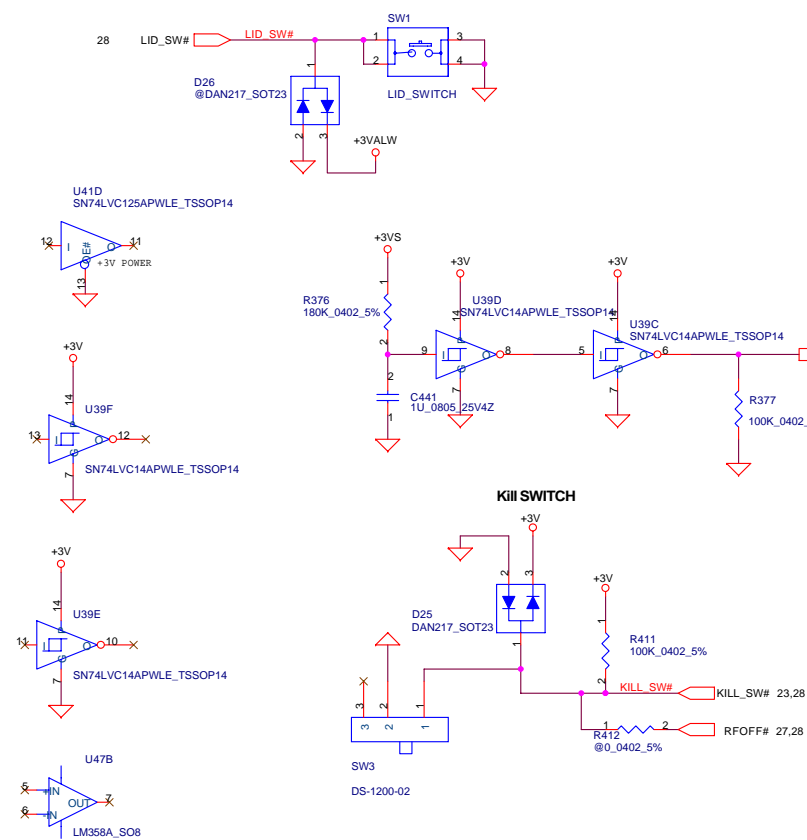
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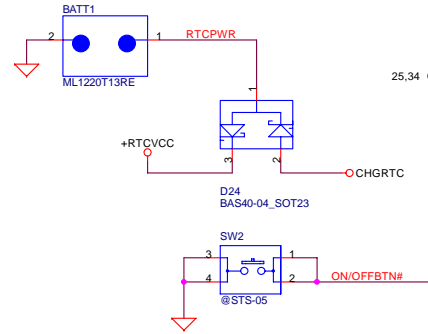
Rev A

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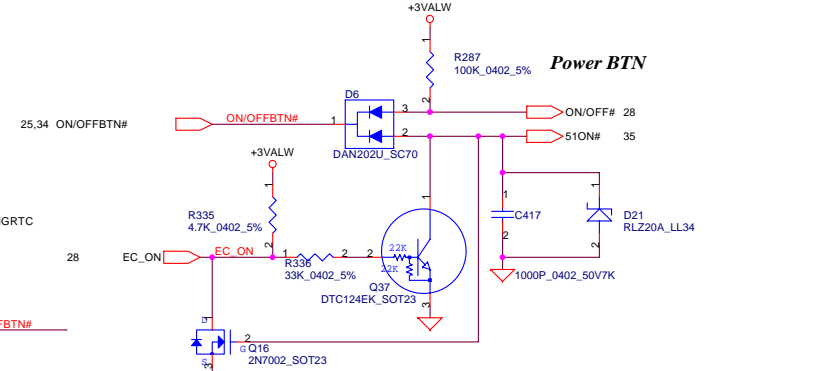
Power ON Circuit



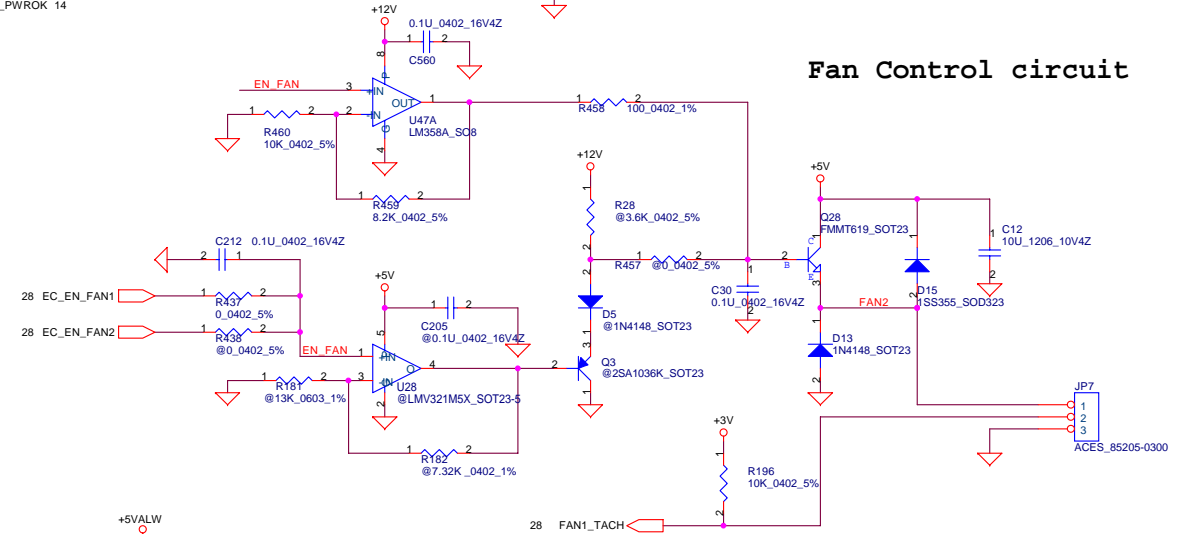
RTC Battery



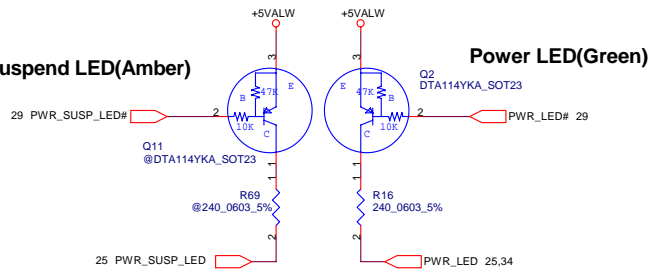
Power BTN



Fan Control circuit

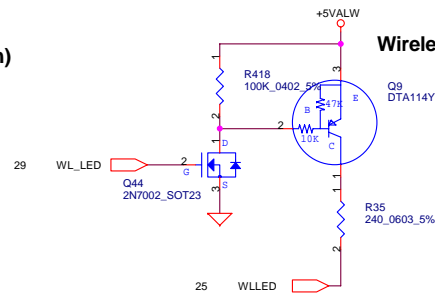


Suspend LED(Amber)

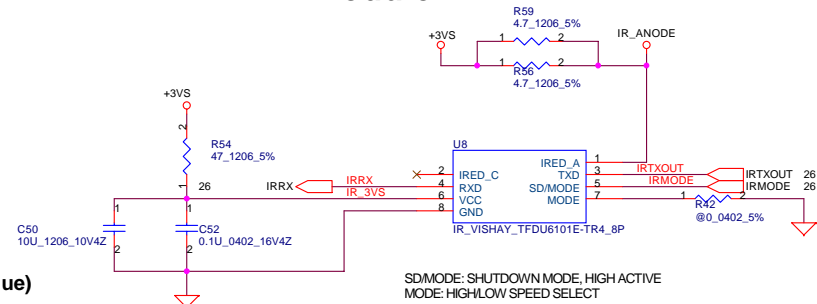


Power LED(Green)

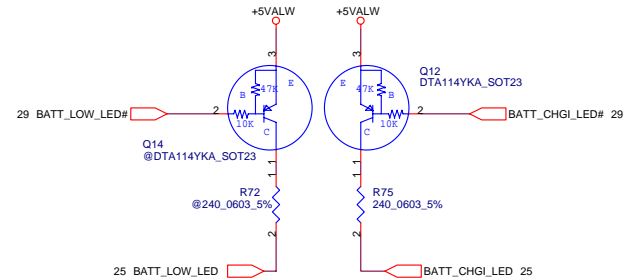
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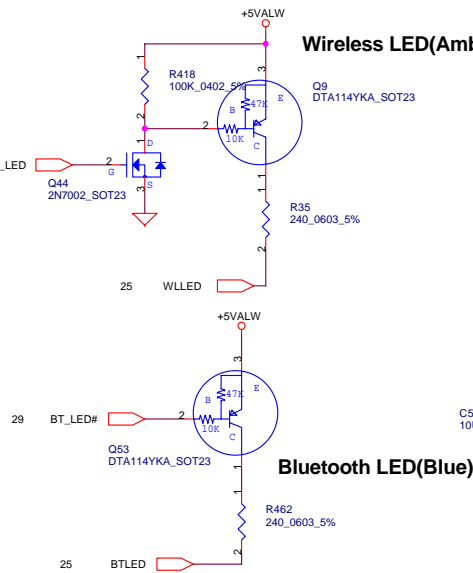
FIR Module



BATT Low LED(Amber)

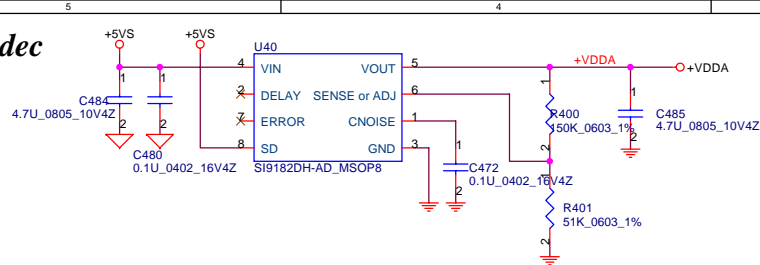


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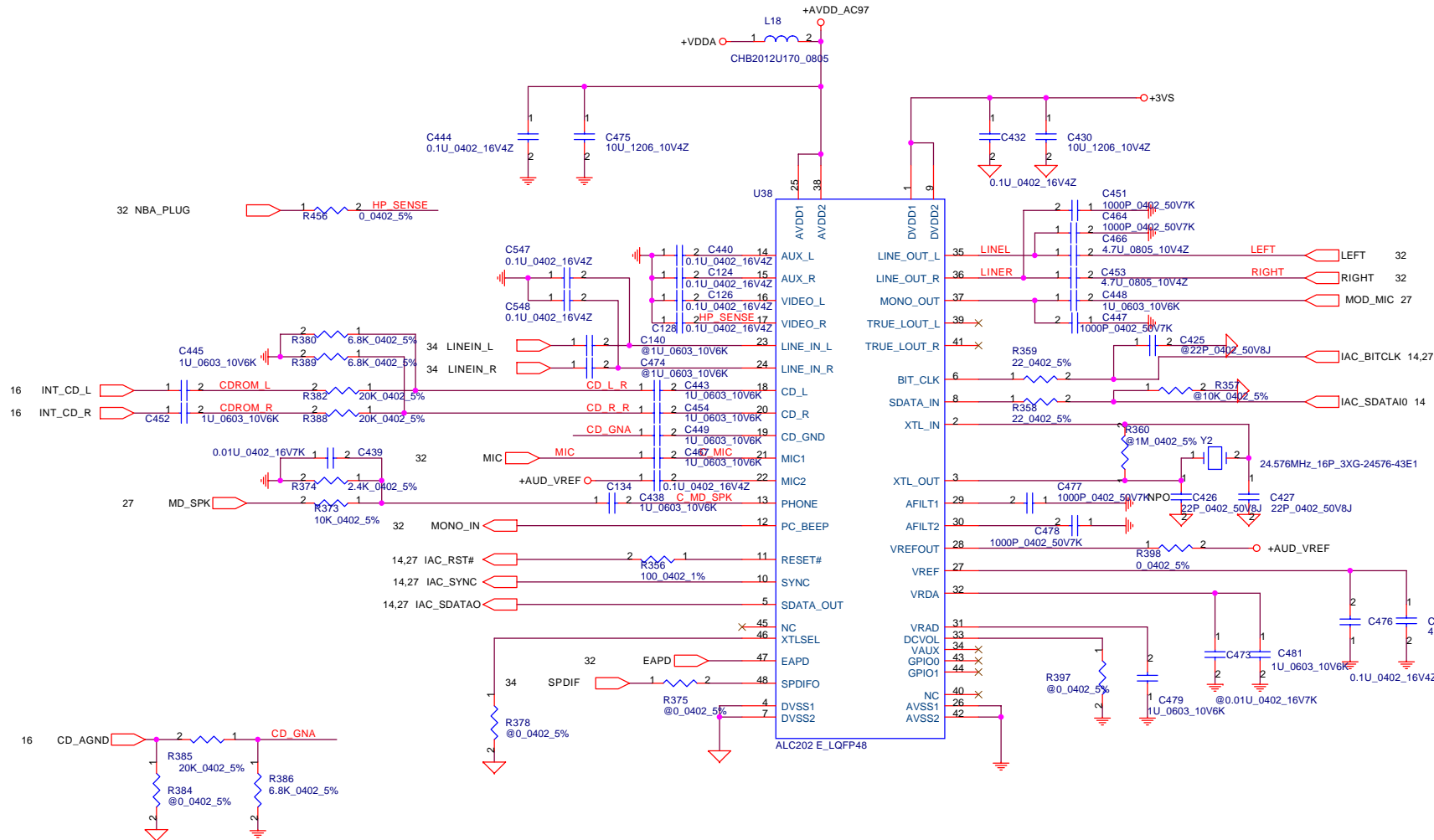
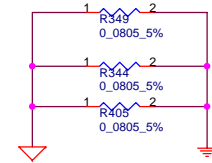
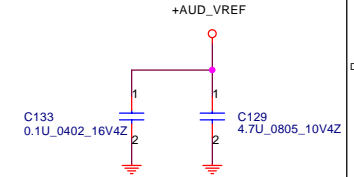
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AC97 Codec



R740	MODE
Stuff	14.318MHz External
No-Stuff	24.576MHz Crysta or External Colck

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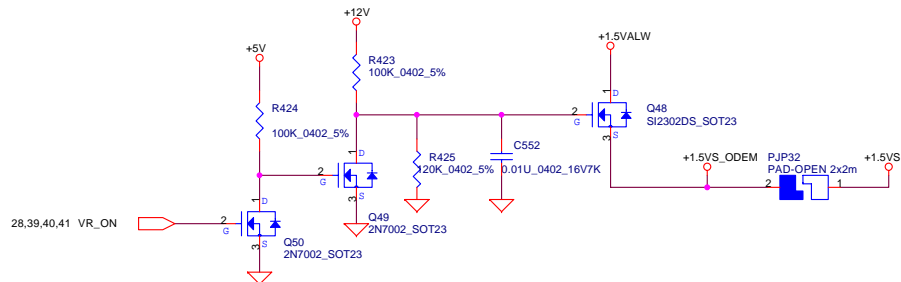
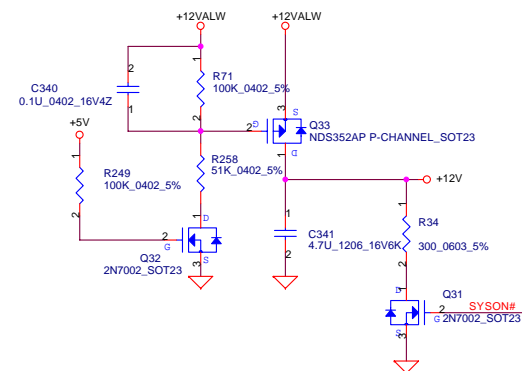
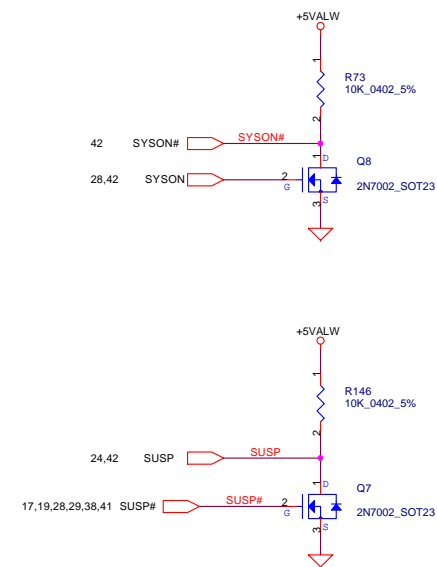
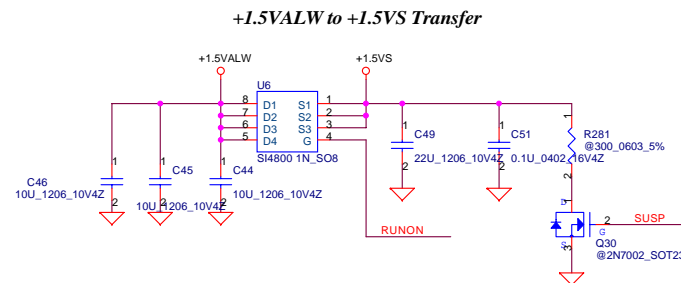
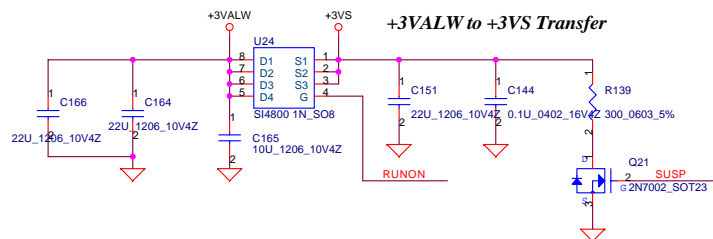
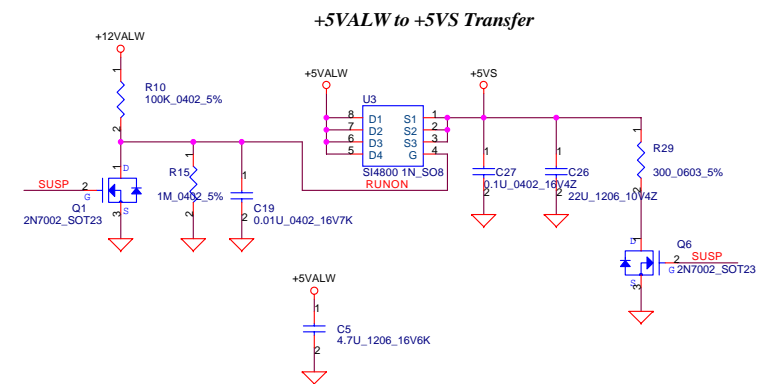
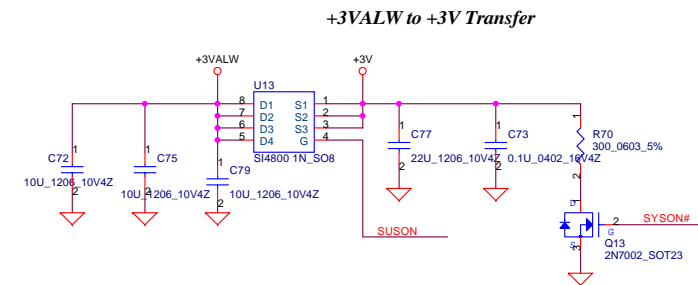
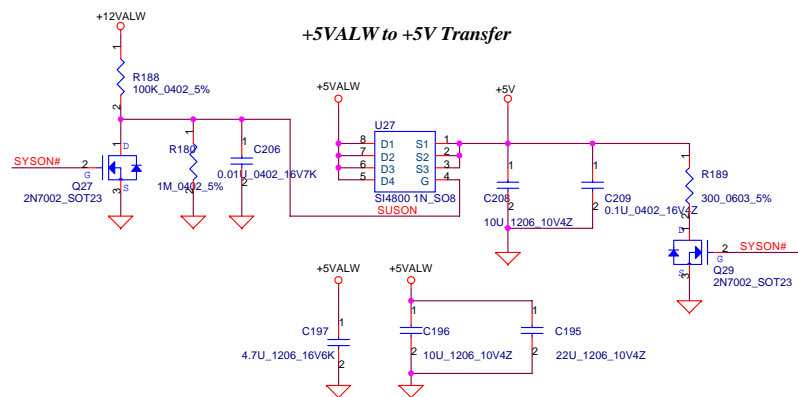
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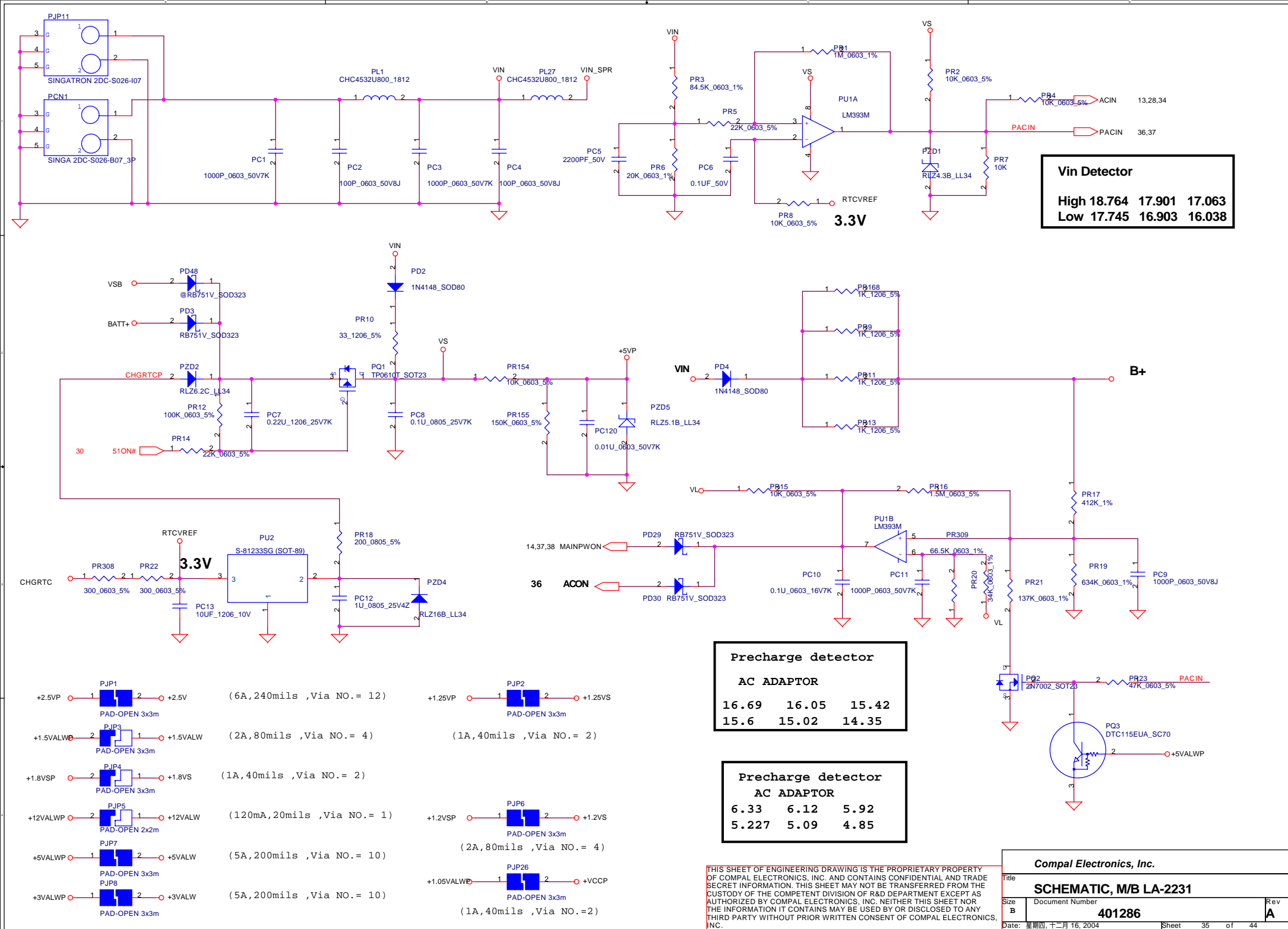
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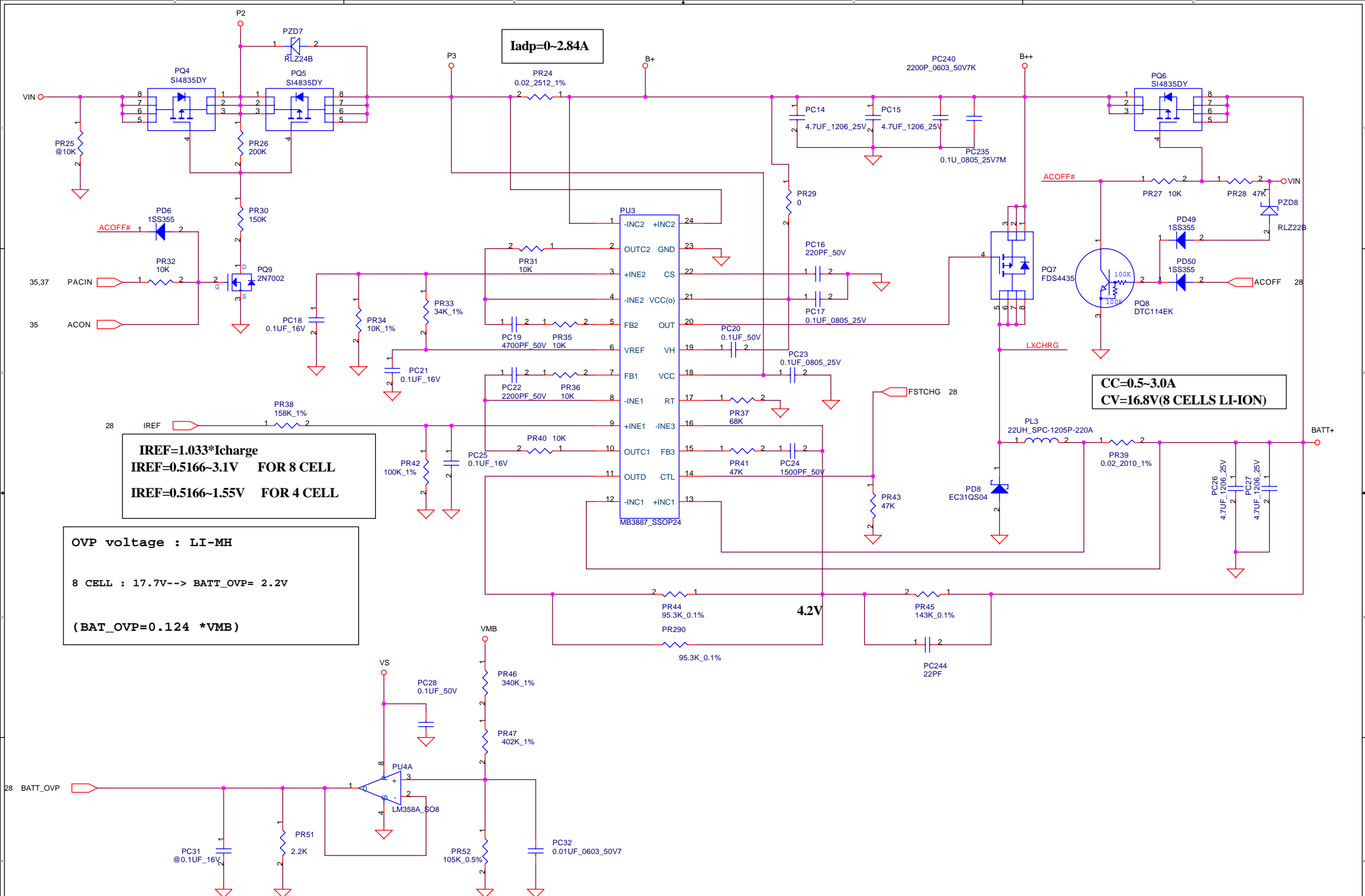
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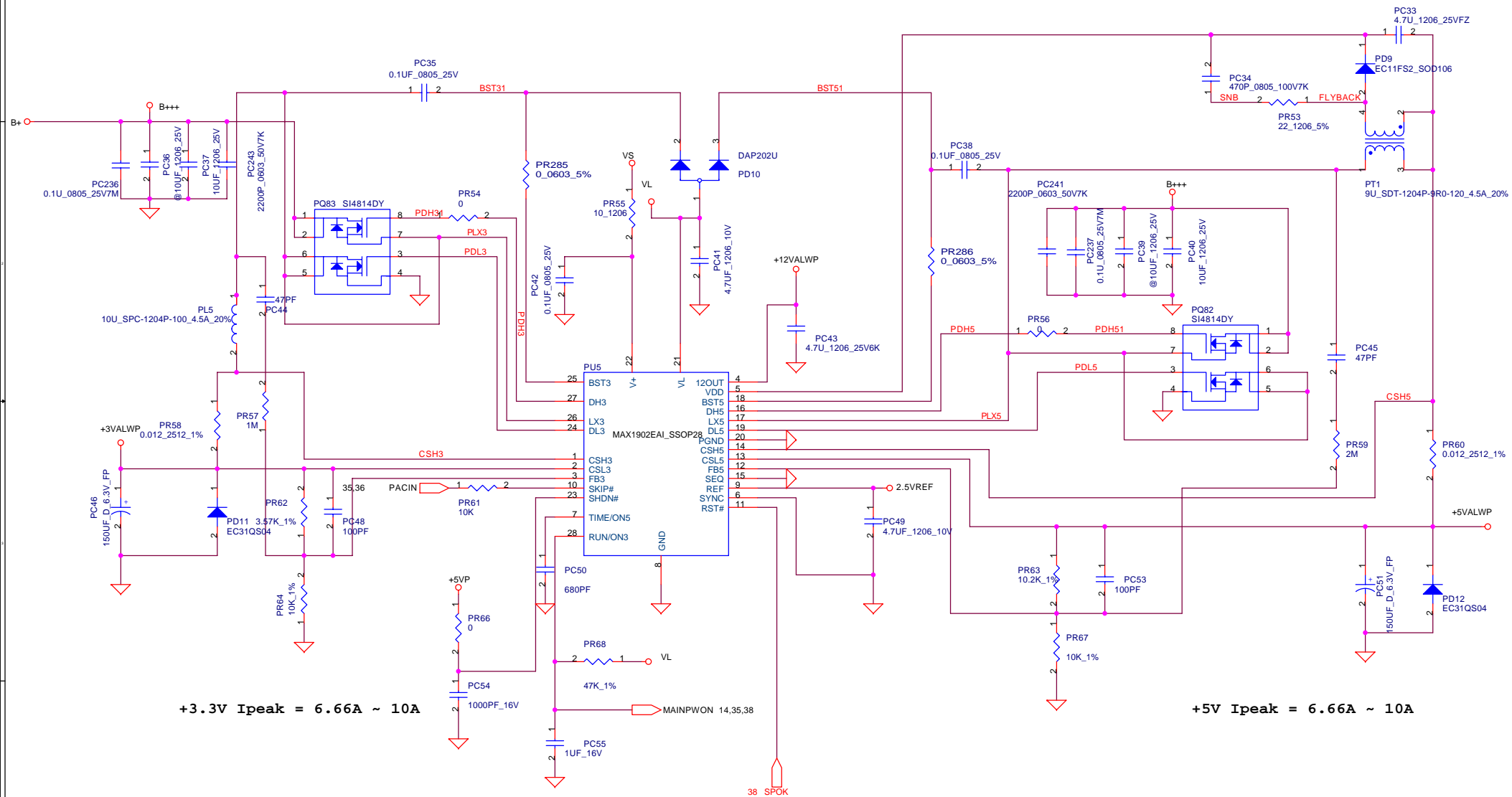




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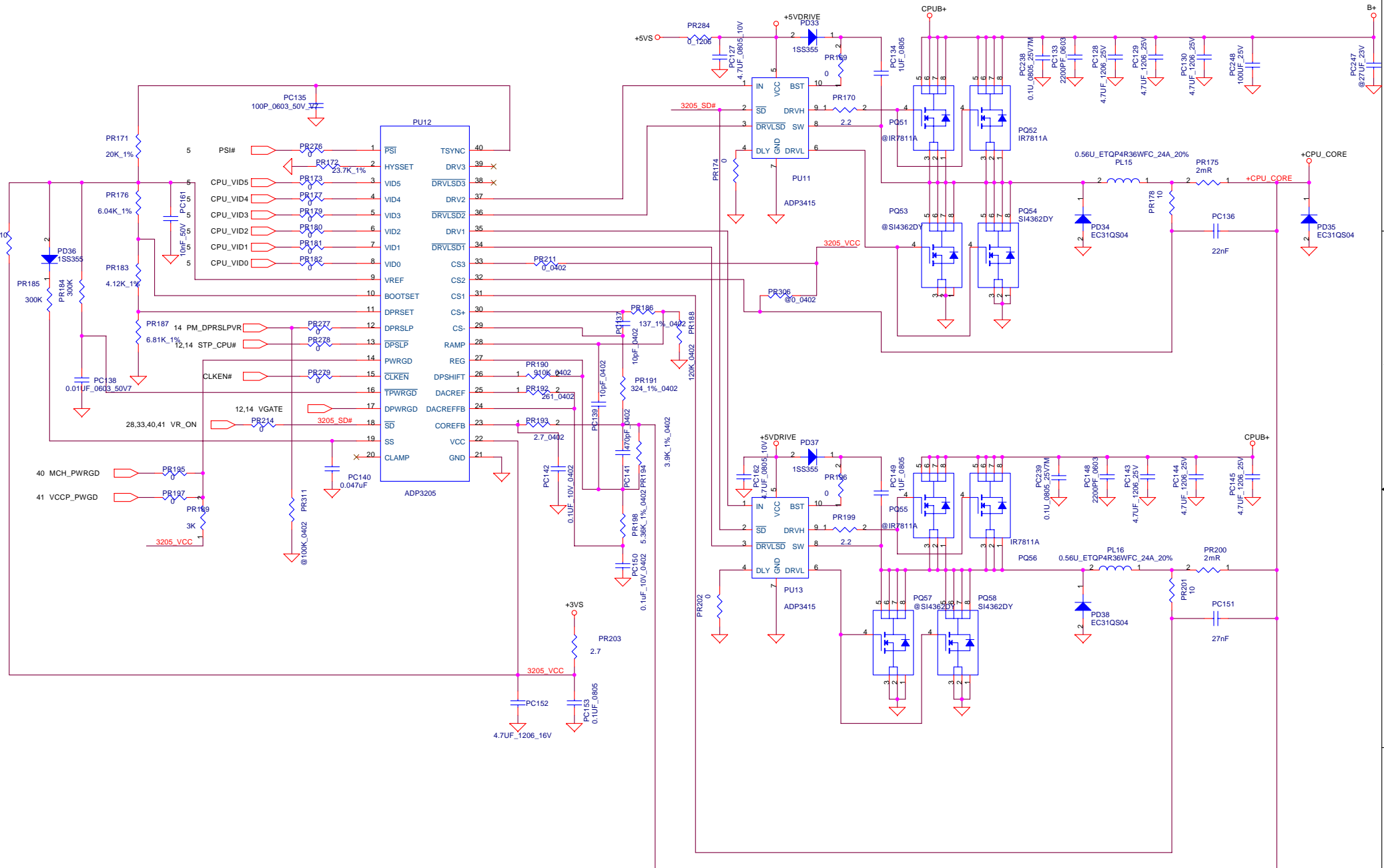


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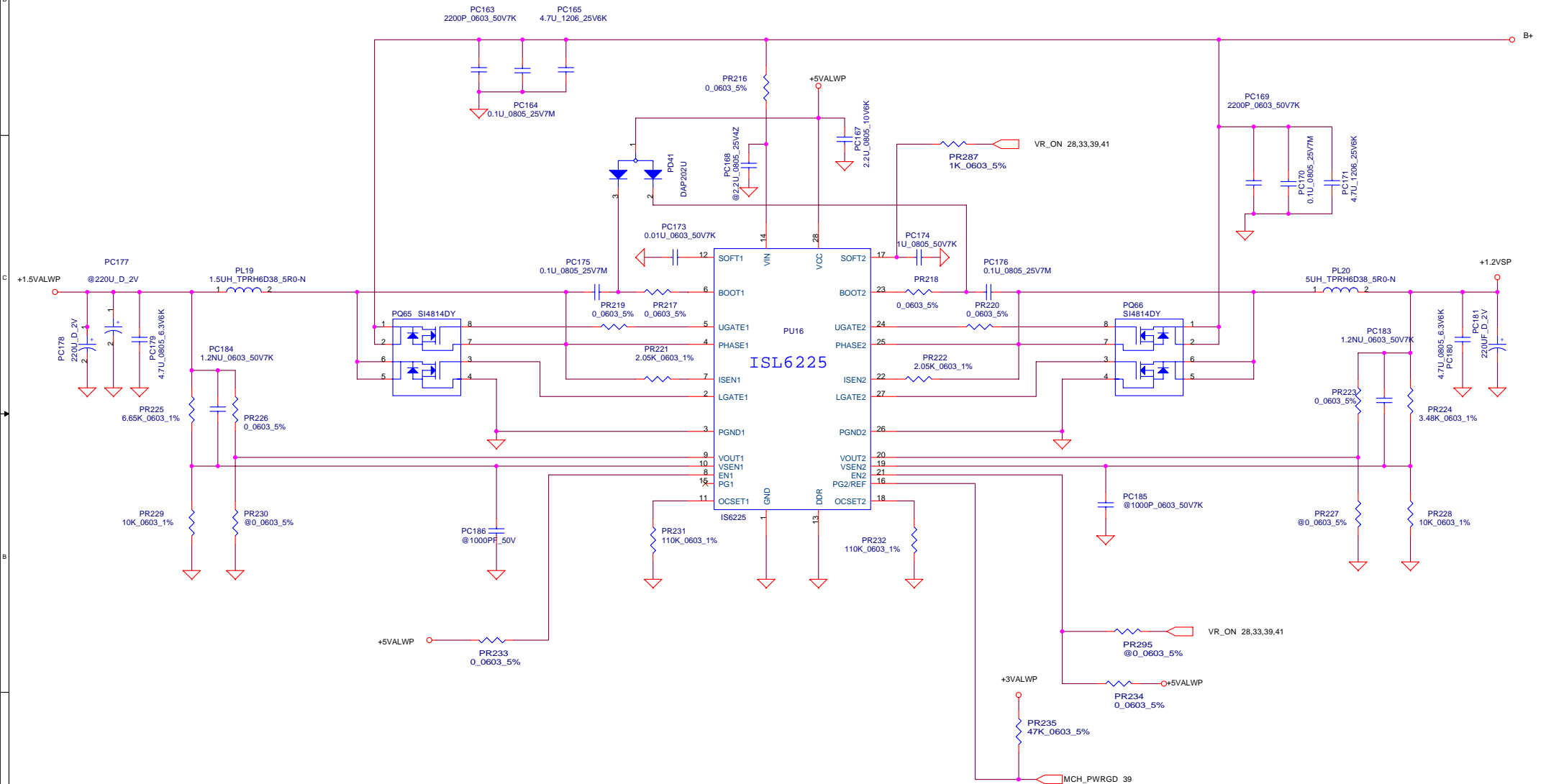
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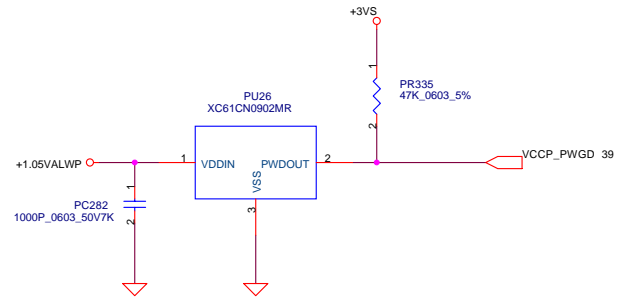
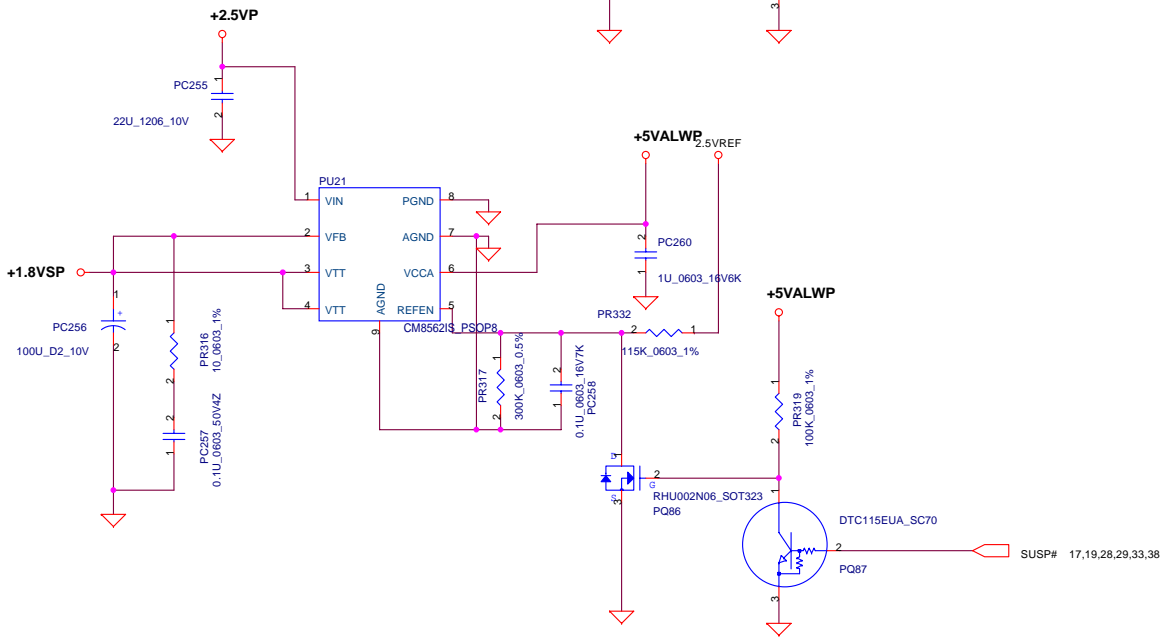
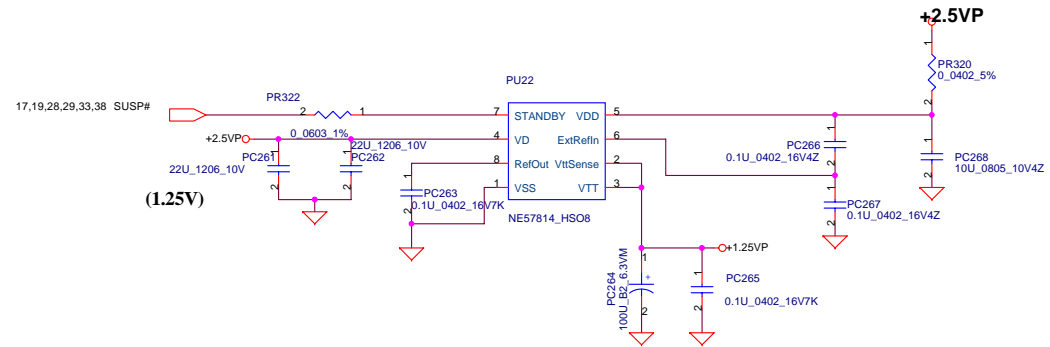
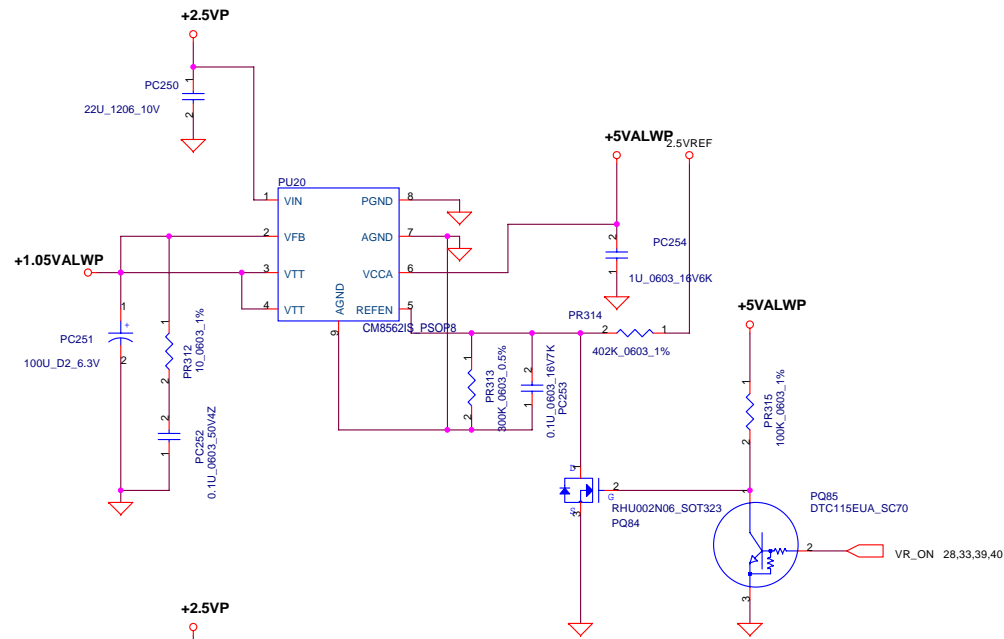
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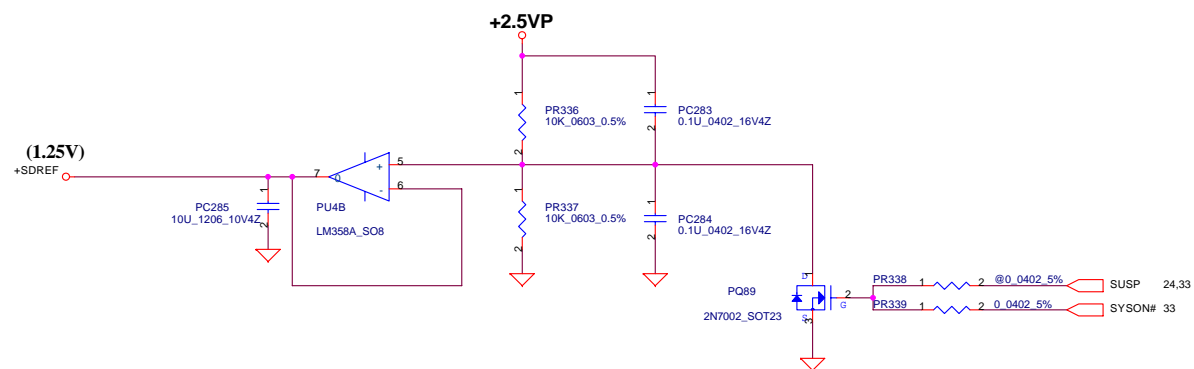
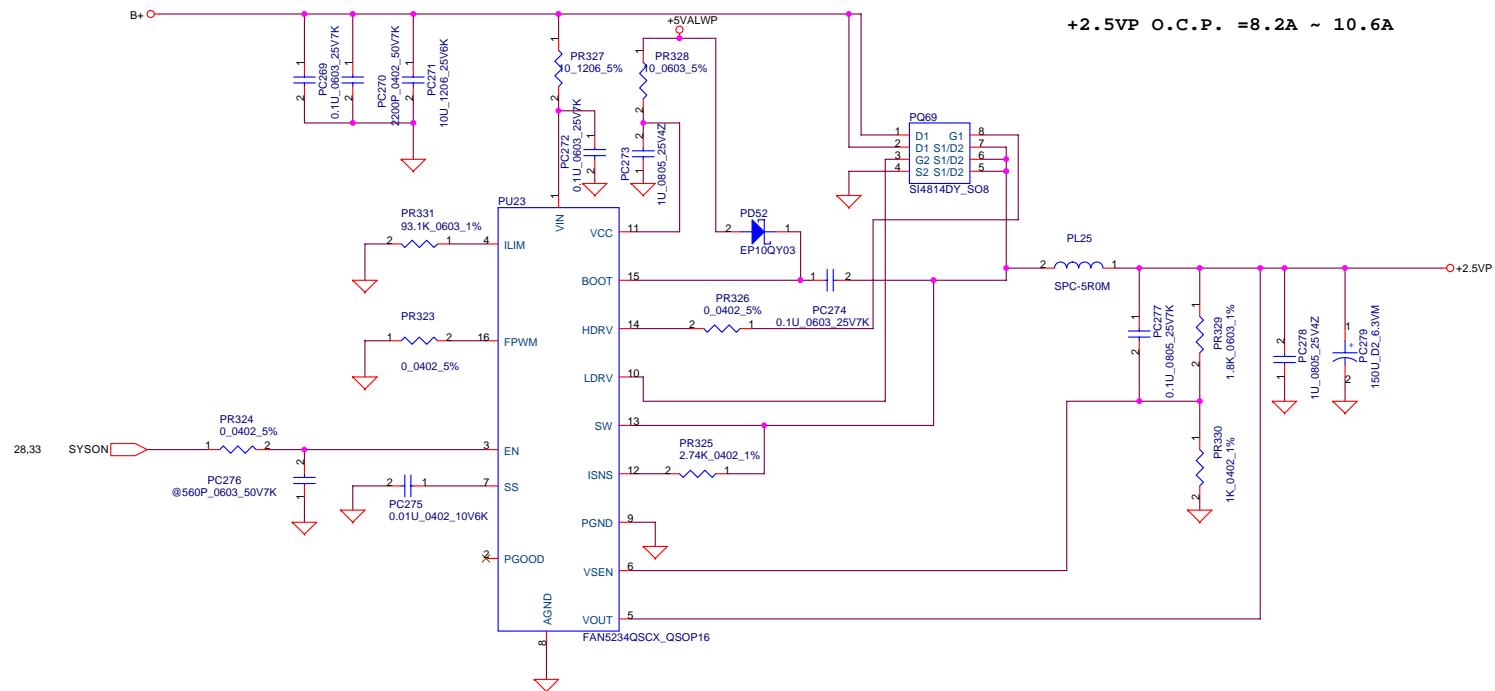
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Version change list (P.I.R. List)

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for HW

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1.	IDE reset signal level error	Change signal level from 3V to 5V		P16	Delete D8,D9,R144,R147 Add U44,U45		DVT
2.	LED light not enough	Change VCC from +3VALW to +5VALW		P25	Add Q45,Q46,Q47 Add R420,R421,R422		DVT
3.	Change flash ROM size	Change from 4Mb to 8Mb		P29	Delete U9 Add U42		DVT
4.	Change flash ROM size	Change from 8Mb to 4Mb		P29	Delete U42, C549, R419, JP28 Add U9, C59		PVT
5.	Change USB Power	Change USB Power from +5VALW to +5V		P25	Change U2.2, U4.2 form +5VALW to +5V		PVT
6.	Noise when system boot	Change PCM_SPK# sequence		p19	Add R435 on PCM_SPK# and pull up to +3V		PVT
7.	Some CF card can't read	Pull up S1_OE#		P20	Add R436 on S1_OE# to pull up to S1_VCC		PVT
8.	Change FAN Connector	Change FAN Connector		P30	Change FAN Connector JP7 from 4-Pin to 3-Pin		PVT
9.	Add Bluetooth Detect Pin	Add Bluetooth Detect Pin		P30	Add Bluetooth Detect Pin form Super I/O GPIO20 to JP10 Pin20		PVT

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1		to decrease inrushing current		41	1.Change PC256 from 220u to 100u PC251 from 150uF to 100uF PC264 from 220U to 100U		DVT
2		To decrease noise coupling		42	1. change PR331 from 110k to 93.1k, change PR235 from 2k to 2.74k ,change PC275 from 0.1u to 0.01u ,change PR329 from18k to 1k, change PR330 from 10k to1k		PVT
3							
4		for EMI					
5					DELETE PL2,,PL4,PL14,,PL18,PL28		PVT
6		CHANGE PU5 from MAX1631 to MAX1902 (BECAUSE MAX1631 shortage)		38	CHANGE PT1 from 10u_1205P to 9u_sdt-1204p-9r0-120;delete PU19;CHANGE pl5 FROM 10U_SPC-1205P-100 to 10u_1204p-100_4.5A;change PC39 from 180PF to 470PF;DELETE PZD6;change PU5 from max1631 to max1902		
7							
8							
9							

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