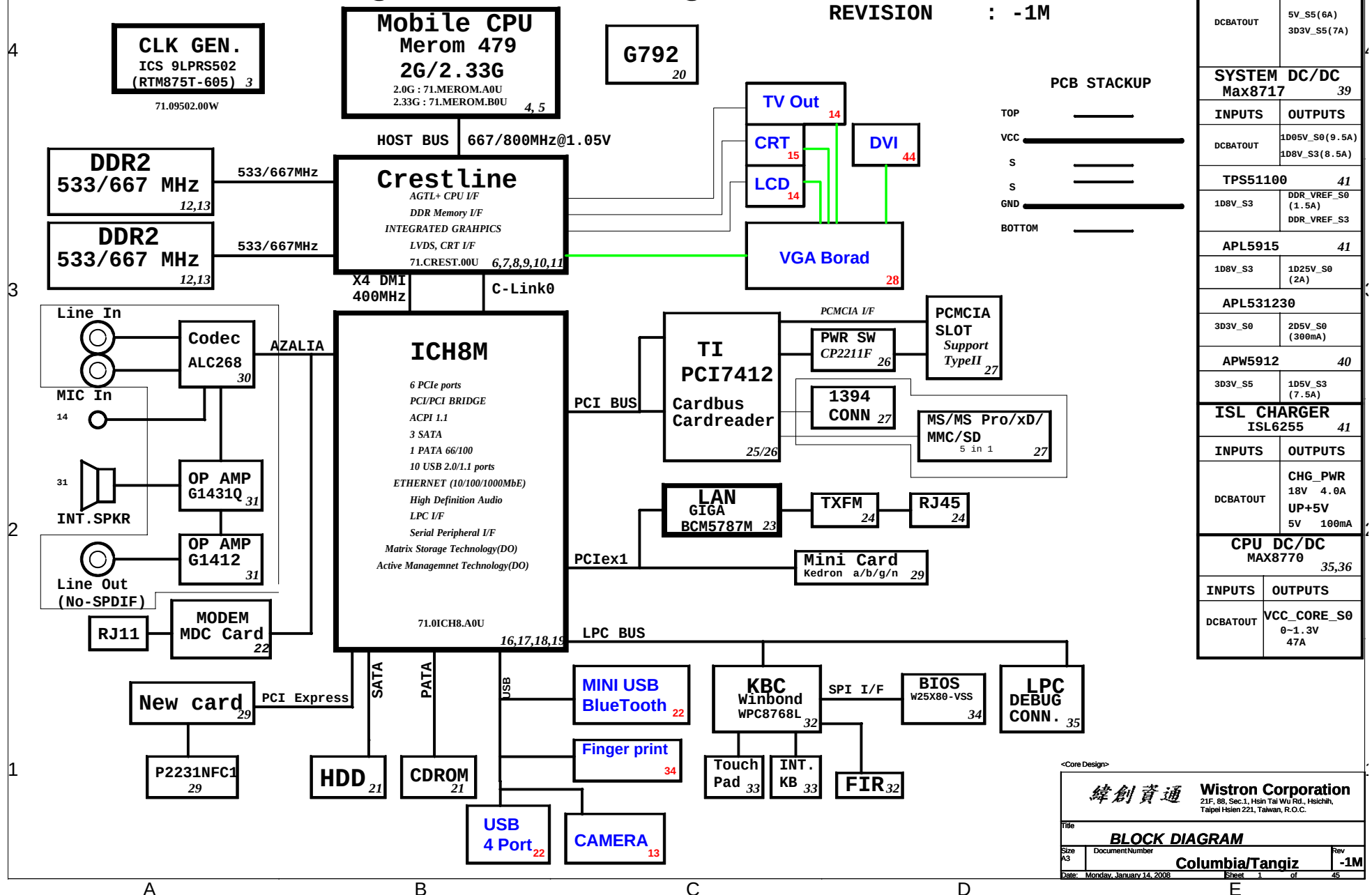


Columbia/Tangiz Block Diagram

Project code: 91.4T301.001
PCB P/N : 48.4T301.01M
REVISION : -1M



<Core Design>

緯創資通 Wistron Corporation 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	BLOCK DIAGRAM
Size A3	Document Number
Date: Monday, January 14, 2008	Sheet 1 of 45
Columbia/Tangiz Rev -1M	

A B

ICH8M Functional Strap Definitions

ICH8-M EDS 21762 2.0V1 page 16

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPI020	Reserved	This signal should not be pulled high.
GNT1#/ GPI051	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSusi_05, VccSusi1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSusi_05, VccSusi1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPI033/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

2

ICH8M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

1

PCI Routing

page 17

	IDSEL	INT	REQ	GNT
IT7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB	
Pair	Device
0	USB1
1	NC
2	USB2
3	USB4
4	USB3
5	BLUETOOTH
6	WEBCAM
7	FT
8	MINICARD
9	NEW1

C

ICH8M Integrated Pull-up and Pull-down Resistors

ICH8-M EDS 21762 2.0V1

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPI0[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPI023	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

History

D E

Crestline Strapping Signals and Configuration

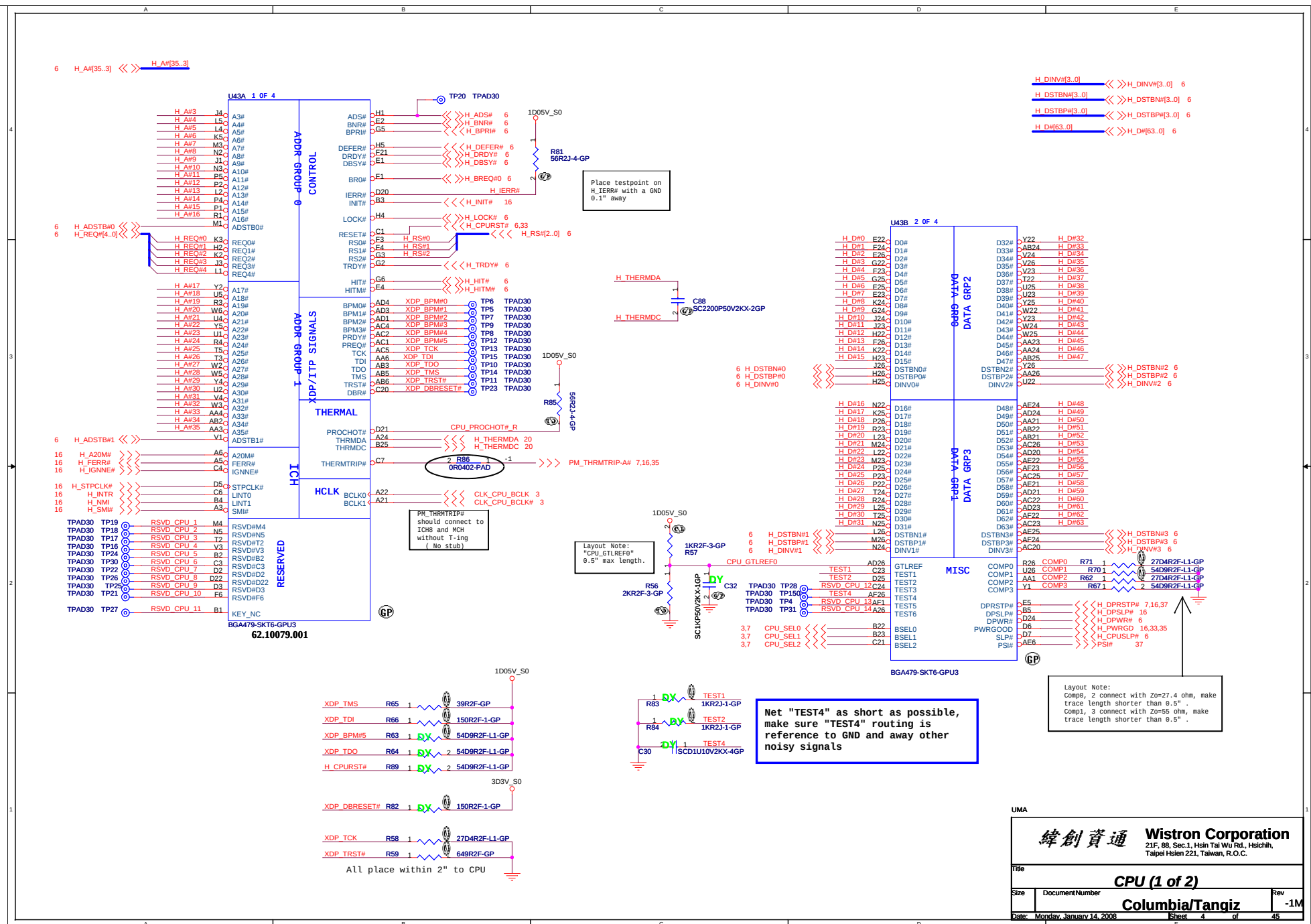
Crestline EDS 20954 1.0
page 7

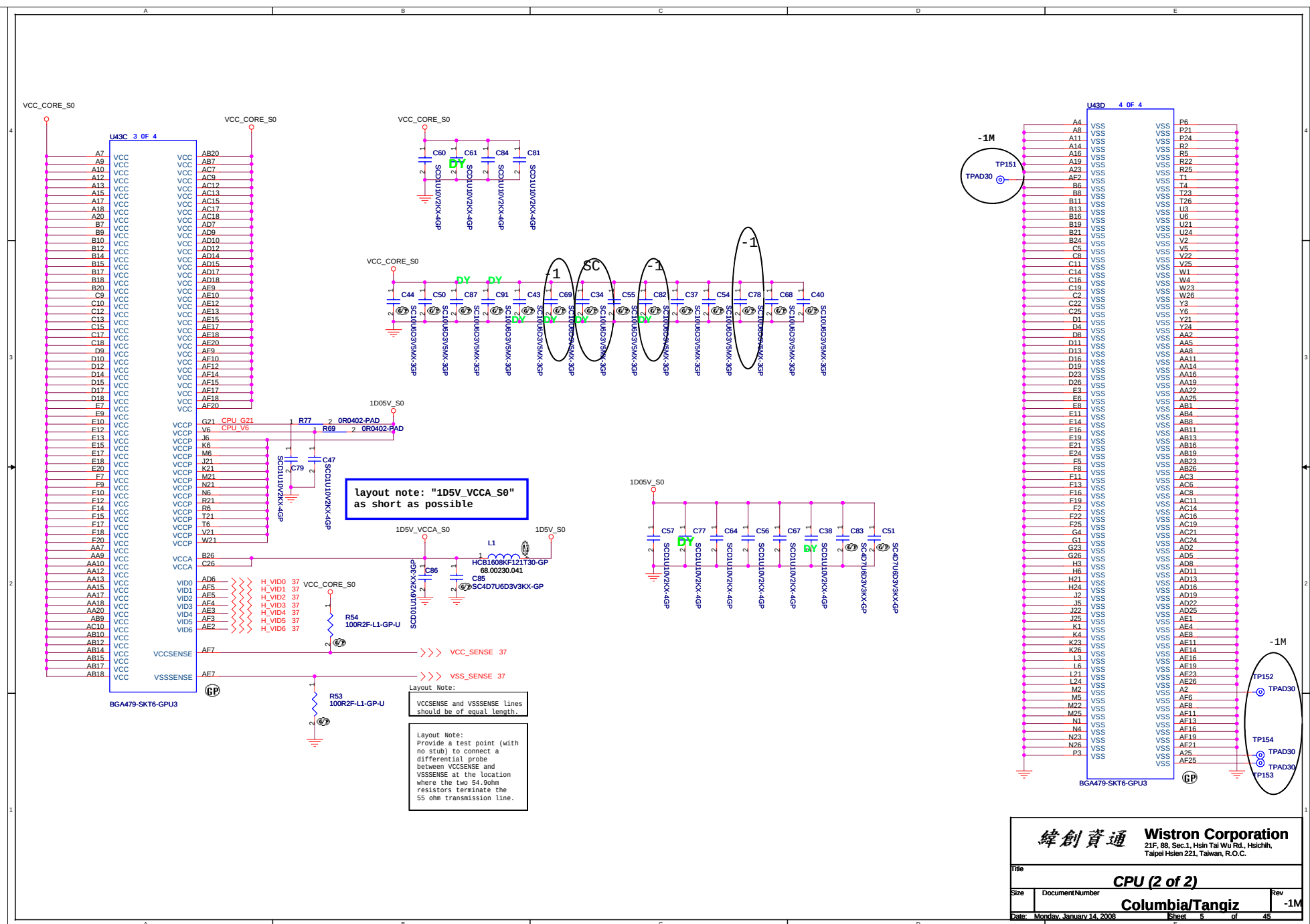
Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode 1 = Low Power mode (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCTRL _DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading
edge of the Crestline GMCH PWROK in signal.

UMA

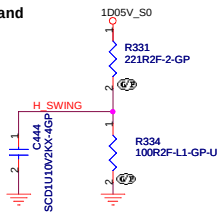
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipai Hsien 221, Taiwan, R.O.C.	
Title	
Reference	
Size A3	Document Number
Columbia/Tangiz	
Date: Monday, January 14, 2008	Sheet 2 of 45
Rev -1M	





H_SWING routing Trace width and Spacing use 10 / 20 mil

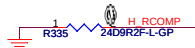
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_SCOMP and H_SCOMP# Resistors and Capacitors close MCH 500 mil (MAX)

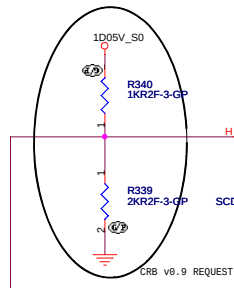


H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")

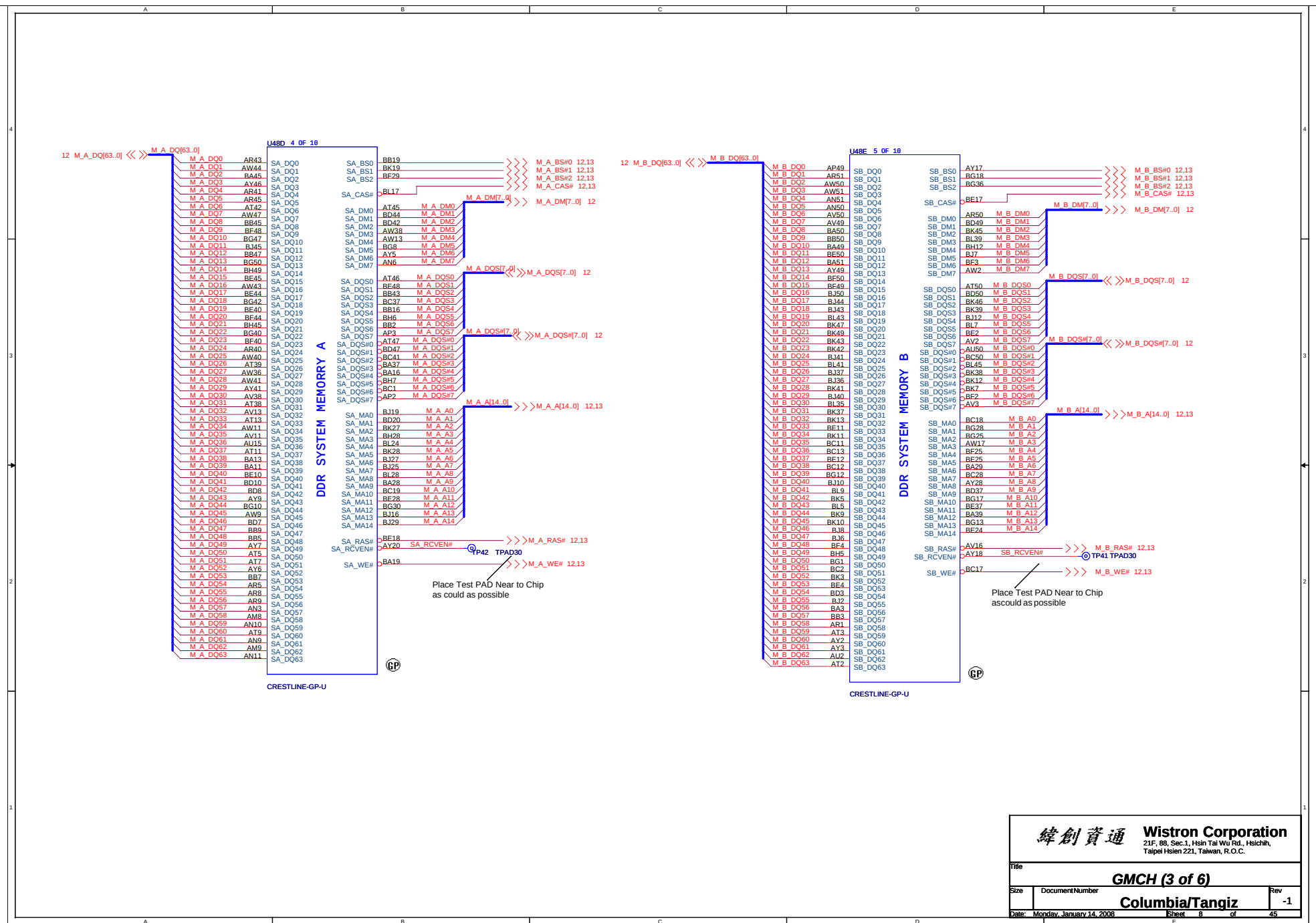
H_REF Decoupling Crestline
close Crestline 100 mil



UMA

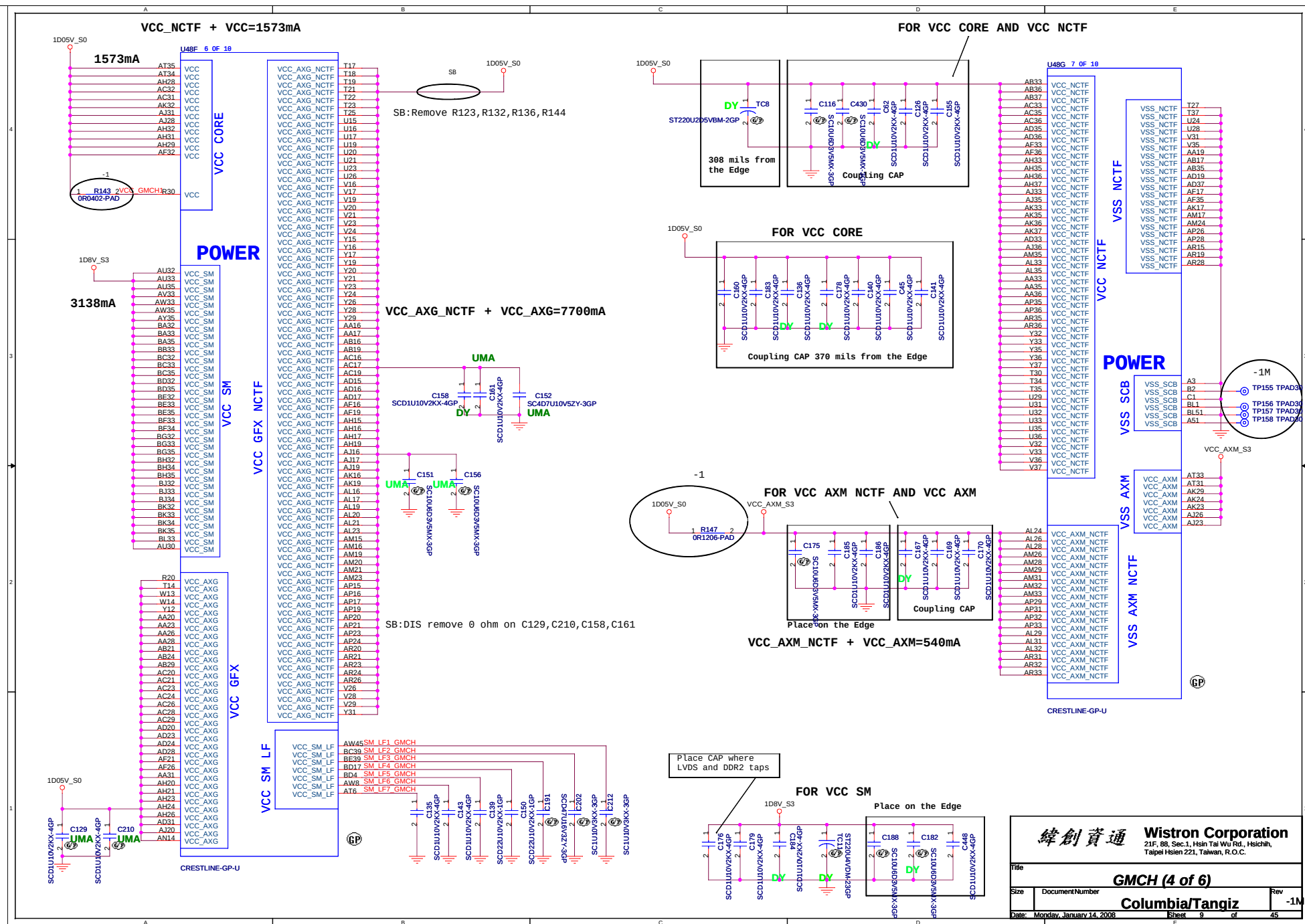
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Taippei Hsien 221, Taiwan, R.O.C.

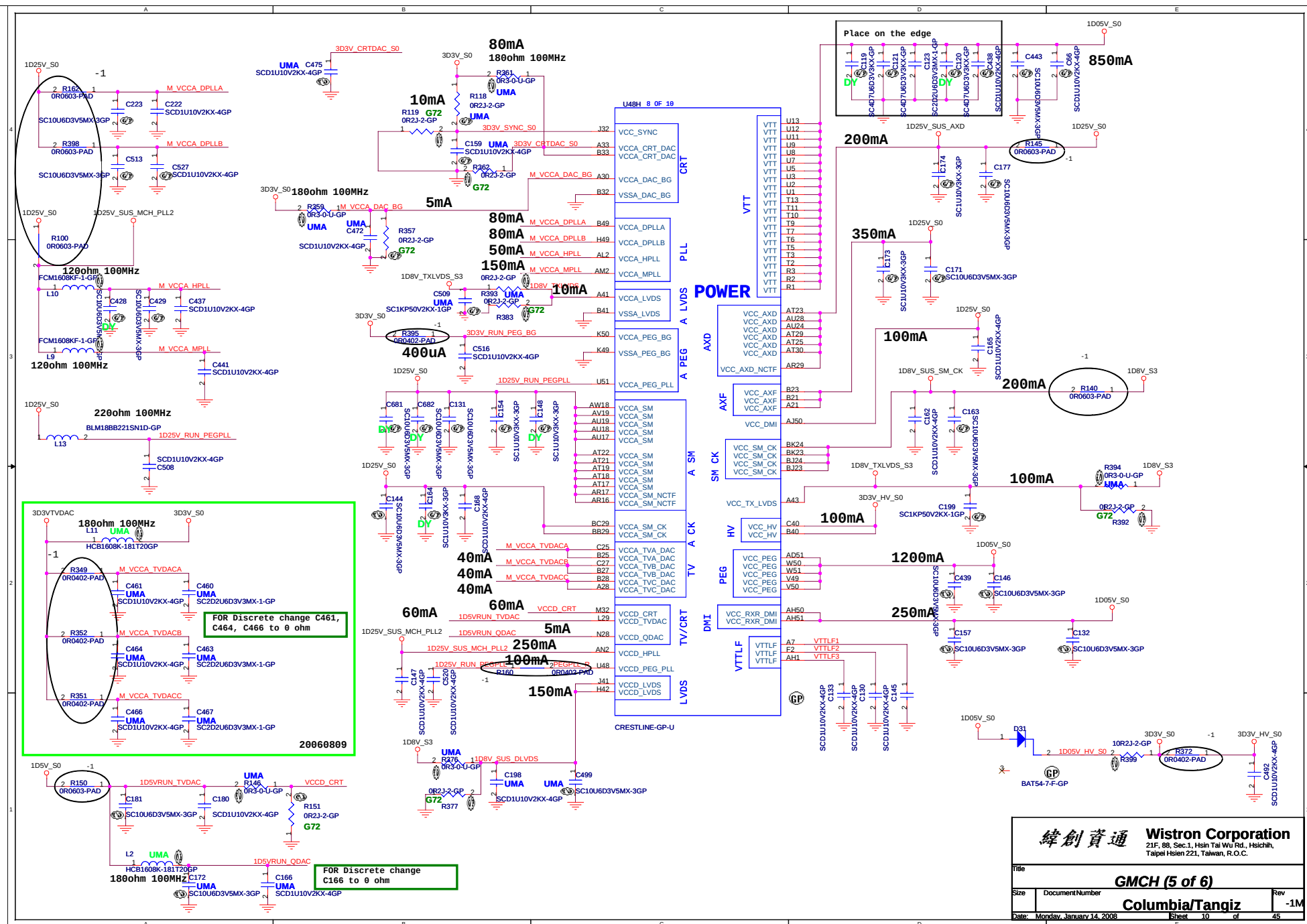
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Size	Document Number		Rev	-1M
Date: Monday, January 14, 2008			Sheet 6 of 45	



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Title			GMCH (3 of 6)
Size	DocumentNumber	Rev	-1
Date			Monday, January 14, 2008
Sheet			8 of 45





U48I 9 OF 10

A13	VSS	VSS	AW24
A15	VSS	VSS	AW29
A17	VSS	VSS	AW32
A24	VSS	VSS	AW5
AA21	VSS	VSS	AW7
AA24	VSS	VSS	AY10
AA29	VSS	VSS	AY24
AB20	VSS	VSS	AY37
AB23	VSS	VSS	AY42
AB26	VSS	VSS	AY43
AB28	VSS	VSS	AY45
AB31	VSS	VSS	AY47
AC10	VSS	VSS	AY50
AC13	VSS	VSS	B10
AC3	VSS	VSS	B20
AC39	VSS	VSS	B24
AC43	VSS	VSS	B29
AC47	VSS	VSS	B30
AD1	VSS	VSS	B35
AD21	VSS	VSS	B38
AD26	VSS	VSS	B43
AD28	VSS	VSS	B46
AD3	VSS	VSS	B5
AD41	VSS	VSS	B8
AD45	VSS	VSS	BA1
AD48	VSS	VSS	BA17
AD5	VSS	VSS	BA18
AD50	VSS	VSS	BA2
AD8	VSS	VSS	BA24
AE10	VSS	VSS	BB12
AE14	VSS	VSS	BB25
AE6	VSS	VSS	BB40
AF20	VSS	VSS	BB44
AF23	VSS	VSS	BB49
AF24	VSS	VSS	BB8
AF31	VSS	VSS	BC16
AG2	VSS	VSS	BC24
AG38	VSS	VSS	BC25
AG43	VSS	VSS	BC36
AG47	VSS	VSS	BC40
AG50	VSS	VSS	BC51
AH3	VSS	VSS	BD13
AH40	VSS	VSS	BD2
AH41	VSS	VSS	BD28
AH7	VSS	VSS	BD45
AH9	VSS	VSS	BD48
AJ11	VSS	VSS	BD5
AJ13	VSS	VSS	BE1
AJ21	VSS	VSS	BE19
AJ24	VSS	VSS	BE23
AJ29	VSS	VSS	BE30
AJ32	VSS	VSS	BE42
AJ43	VSS	VSS	BE51
AJ45	VSS	VSS	BE8
AJ49	VSS	VSS	BE12
AK20	VSS	VSS	BE16
AK21	VSS	VSS	BE36
AK26	VSS	VSS	BG19
AK28	VSS	VSS	BG2
AK31	VSS	VSS	BG24
AK51	VSS	VSS	BG29
AL1	VSS	VSS	BG39
AM11	VSS	VSS	BG48
AM13	VSS	VSS	BG5
AM3	VSS	VSS	BG51
AM4	VSS	VSS	BH17
AM41	VSS	VSS	BH30
AM45	VSS	VSS	BH44
AN1	VSS	VSS	BH46
AN38	VSS	VSS	BH8
AN39	VSS	VSS	BJ11
AN43	VSS	VSS	BJ13
AN5	VSS	VSS	BJ38
AN7	VSS	VSS	BJ4
AP4	VSS	VSS	BJ42
AP48	VSS	VSS	BJ46
AP50	VSS	VSS	BK15
AR11	VSS	VSS	BK17
AR2	VSS	VSS	BK25
AR38	VSS	VSS	BK29
AR44	VSS	VSS	BK36
AR47	VSS	VSS	BK40
AR7	VSS	VSS	BK44
AT10	VSS	VSS	BK6
AT14	VSS	VSS	BK8
AT41	VSS	VSS	BL11
AT49	VSS	VSS	BL13
AU1	VSS	VSS	BL19
AU23	VSS	VSS	BL22
AU29	VSS	VSS	BL37
AU3	VSS	VSS	BL47
AU36	VSS	VSS	C12
AU49	VSS	VSS	C16
AU51	VSS	VSS	C19
AV39	VSS	VSS	C28
AV48	VSS	VSS	C29
AW1	VSS	VSS	C33
AW12	VSS	VSS	C36
AW16	VSS	VSS	C41

VSS

CRESTLINE-GP-U

U48J10 OF 10

C46	VSS	VSS	W11
C50	VSS	VSS	W39
C7	VSS	VSS	W43
D13	VSS	VSS	W47
D24	VSS	VSS	W5
D3	VSS	VSS	W7
D32	VSS	VSS	Y13
D39	VSS	VSS	Y2
D45	VSS	VSS	Y41
D49	VSS	VSS	Y45
E10	VSS	VSS	Y49
E16	VSS	VSS	Y5
E24	VSS	VSS	Y50
E29	VSS	VSS	Y11
E32	VSS	VSS	P29
E37	VSS	VSS	T29
F19	VSS	VSS	T31
F36	VSS	VSS	T33
F4	VSS	VSS	R28
F40	VSS		
F50	VSS		
G1	VSS		
G13	VSS		
G16	VSS	VSS	AA32
G19	VSS	VSS	AB32
G24	VSS	VSS	AD32
G28	VSS	VSS	AF28
G29	VSS	VSS	AF29
G33	VSS	VSS	AT27
G42	VSS	VSS	AV25
G45	VSS	VSS	H50
G48	VSS		
G8	VSS		
H24	VSS		
H28	VSS		
H4	VSS		
H45	VSS		
J11	VSS		
J16	VSS		
J2	VSS		
J24	VSS		
J28	VSS		
J33	VSS		
J35	VSS		
J39	VSS		
K12	VSS		
K47	VSS		
K8	VSS		
L1	VSS		
L17	VSS		
L20	VSS		
L24	VSS		
L28	VSS		
L3	VSS		
L33	VSS		
L49	VSS		
M28	VSS		
M42	VSS		
M46	VSS		
M49	VSS		
M5	VSS		
M50	VSS		
M9	VSS		
N11	VSS		
N14	VSS		
N17	VSS		
N29	VSS		
N32	VSS		
N36	VSS		
N39	VSS		
N44	VSS		
N49	VSS		
N7	VSS		
P19	VSS		
P2	VSS		
P23	VSS		
P3	VSS		
P50	VSS		
R49	VSS		
T39	VSS		
T43	VSS		
T47	VSS		
U41	VSS		
U45	VSS		
U50	VSS		
V2	VSS		
V3	VSS		

VSS

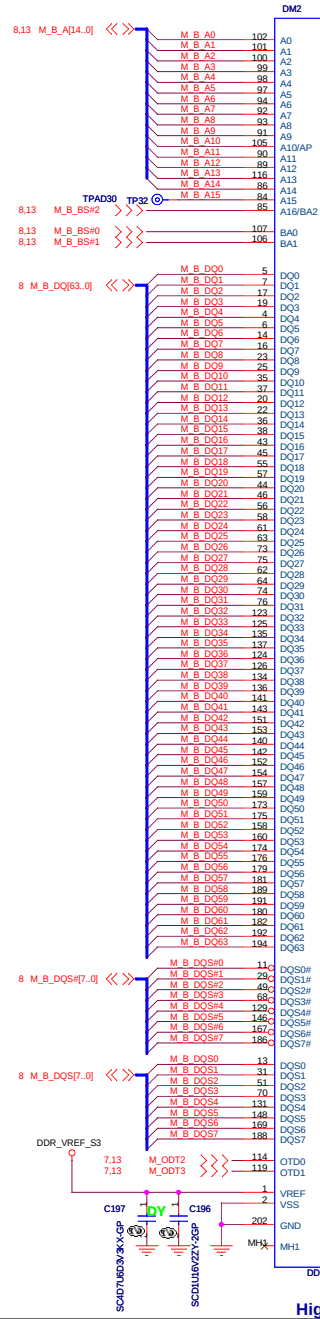
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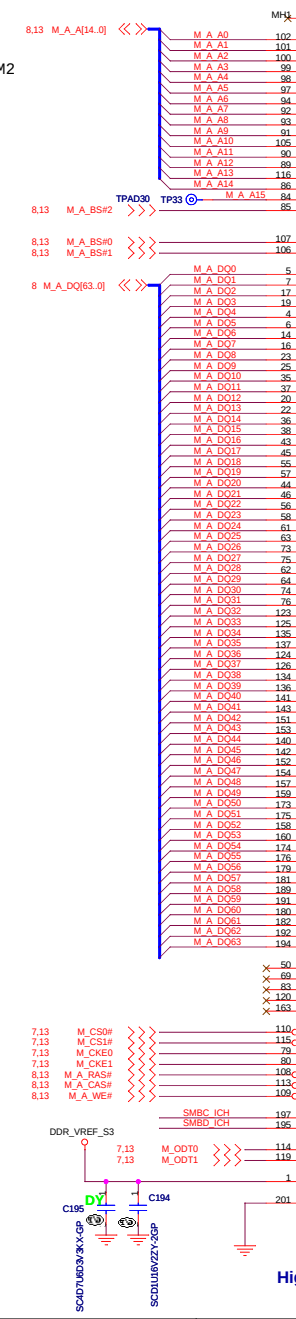
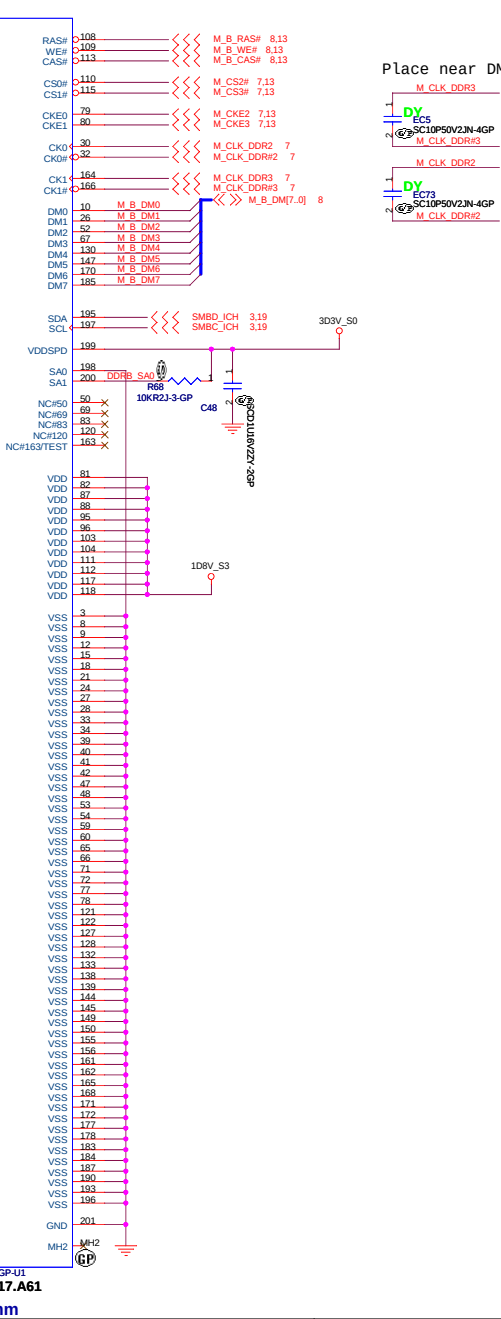
緯創資通

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Taipai Hsien 221, Taiwan, R.O.C.

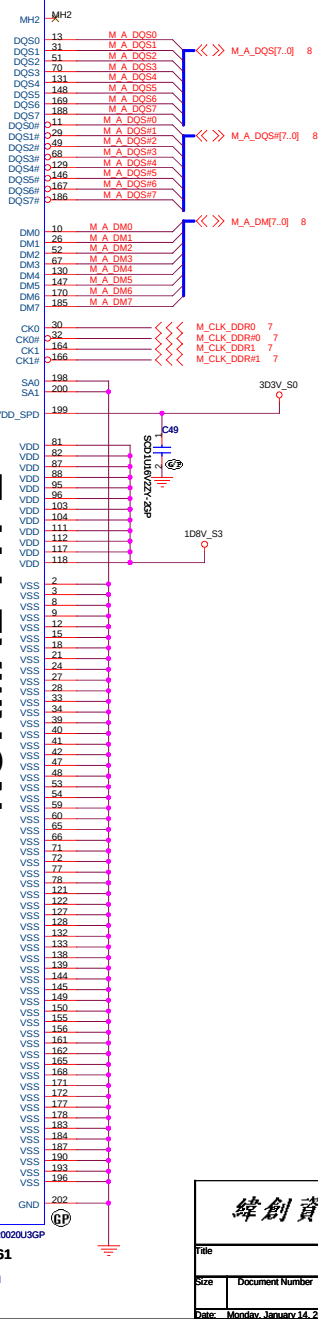
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Size	DocumentNumber		Rev	-1M
Date: Monday, January 14, 2008			Sheet 11 of 45	



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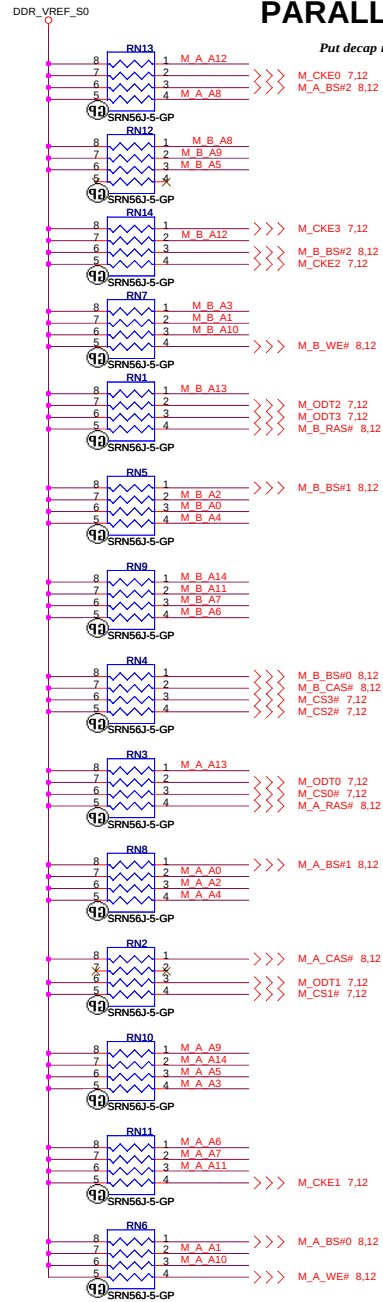


NORMAL TYPE



PARALLEL TERMINATION

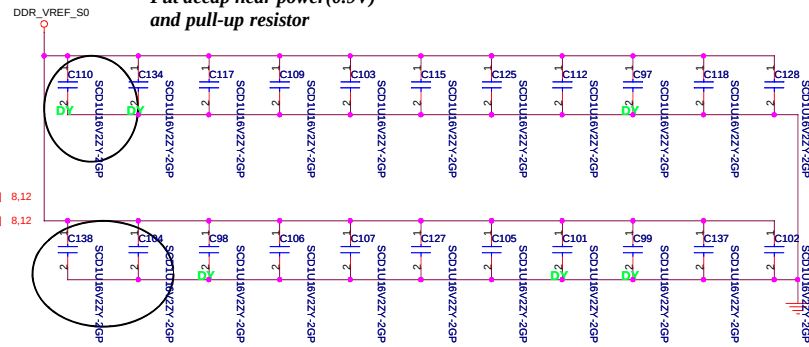
Put decap near power(0.9V) and pull-up resistor



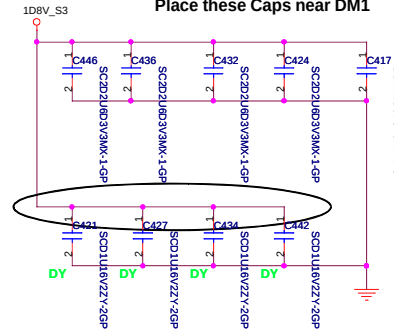
M_A A[14..0] >>> M_A_A[14..0] 8,12
M_B A[14..0] >>> M_B_A[14..0] 8,12

Decoupling Capacitor

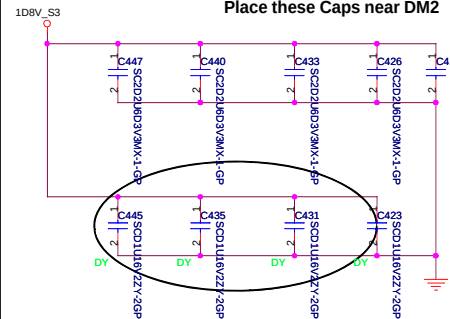
Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM1



Place these Caps near DM2



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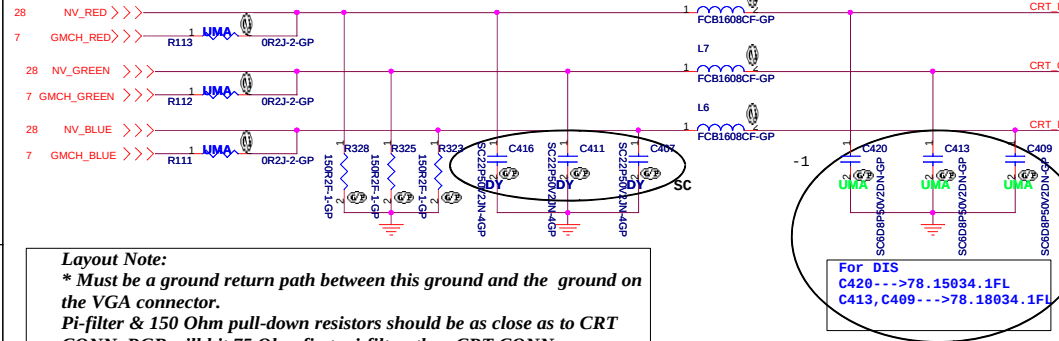
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Size	Document Number	Rev	-1M
Date	Monday, January 14, 2008	Sheet	13 of 45

Columbia/Tangiz

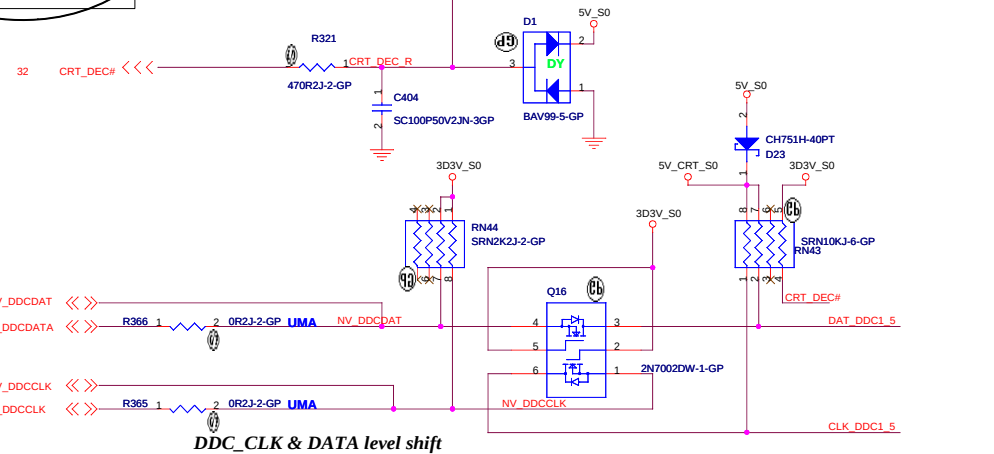
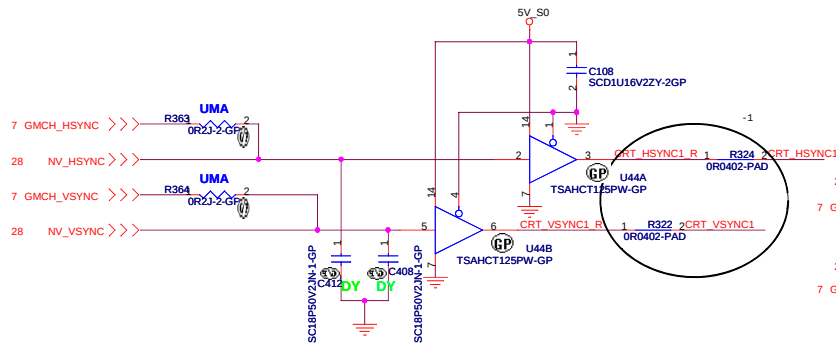
CRT I/F & CONNECTOR

Layout Note:
Place these resistors
close to the CRT-out
connector

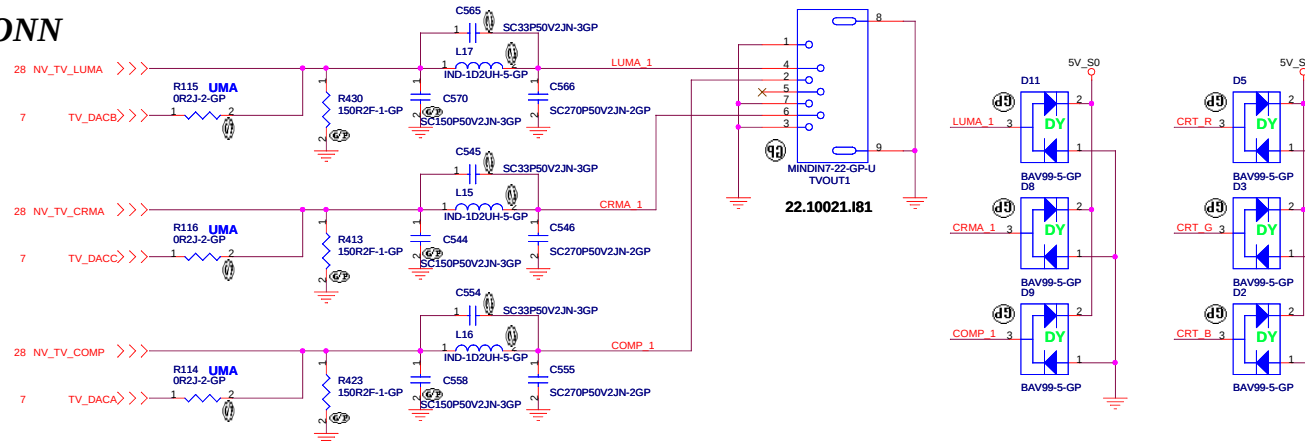
Ferrite bead impedance: 10 ohm@100MHz



Hsync & Vsync level shift

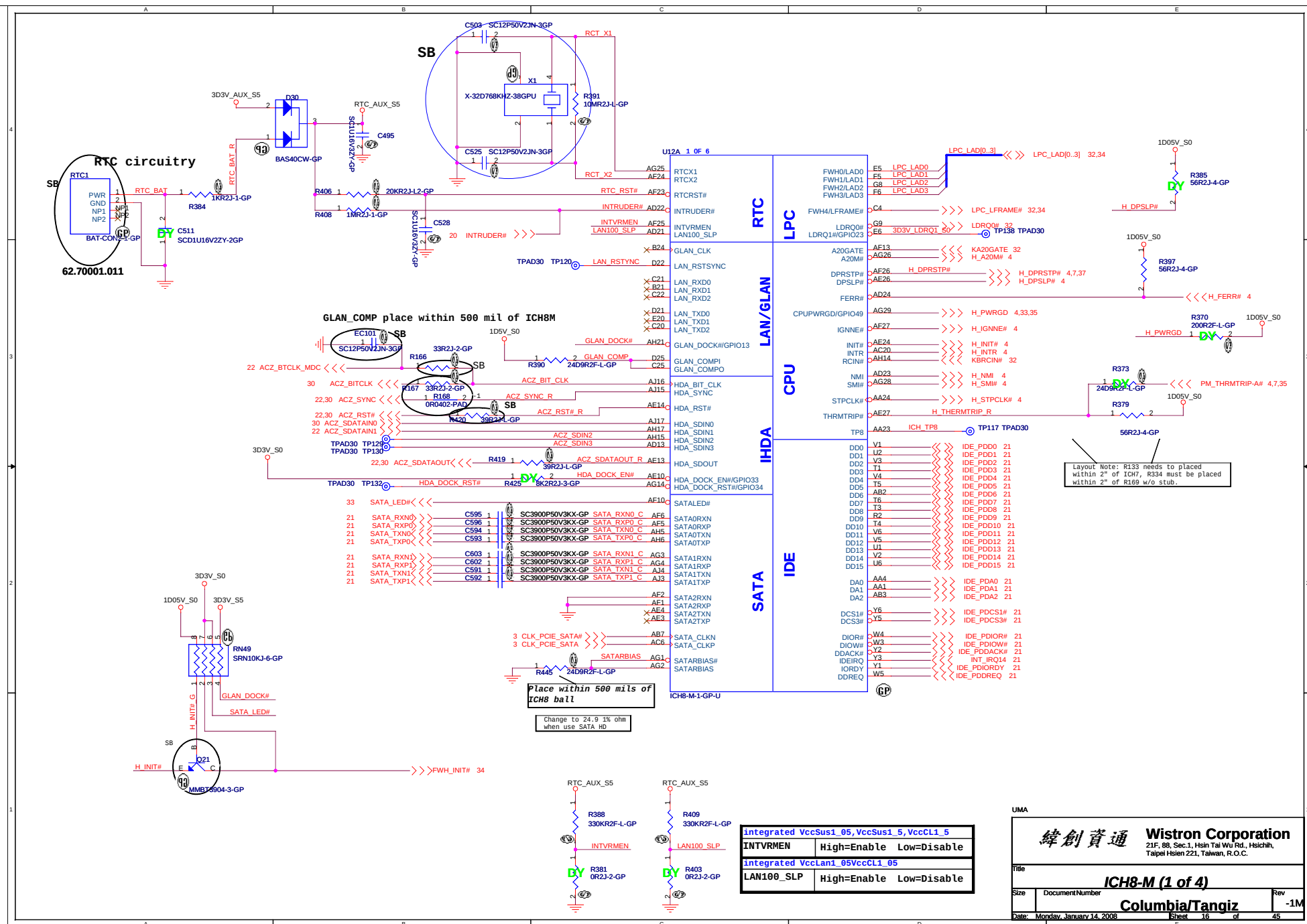


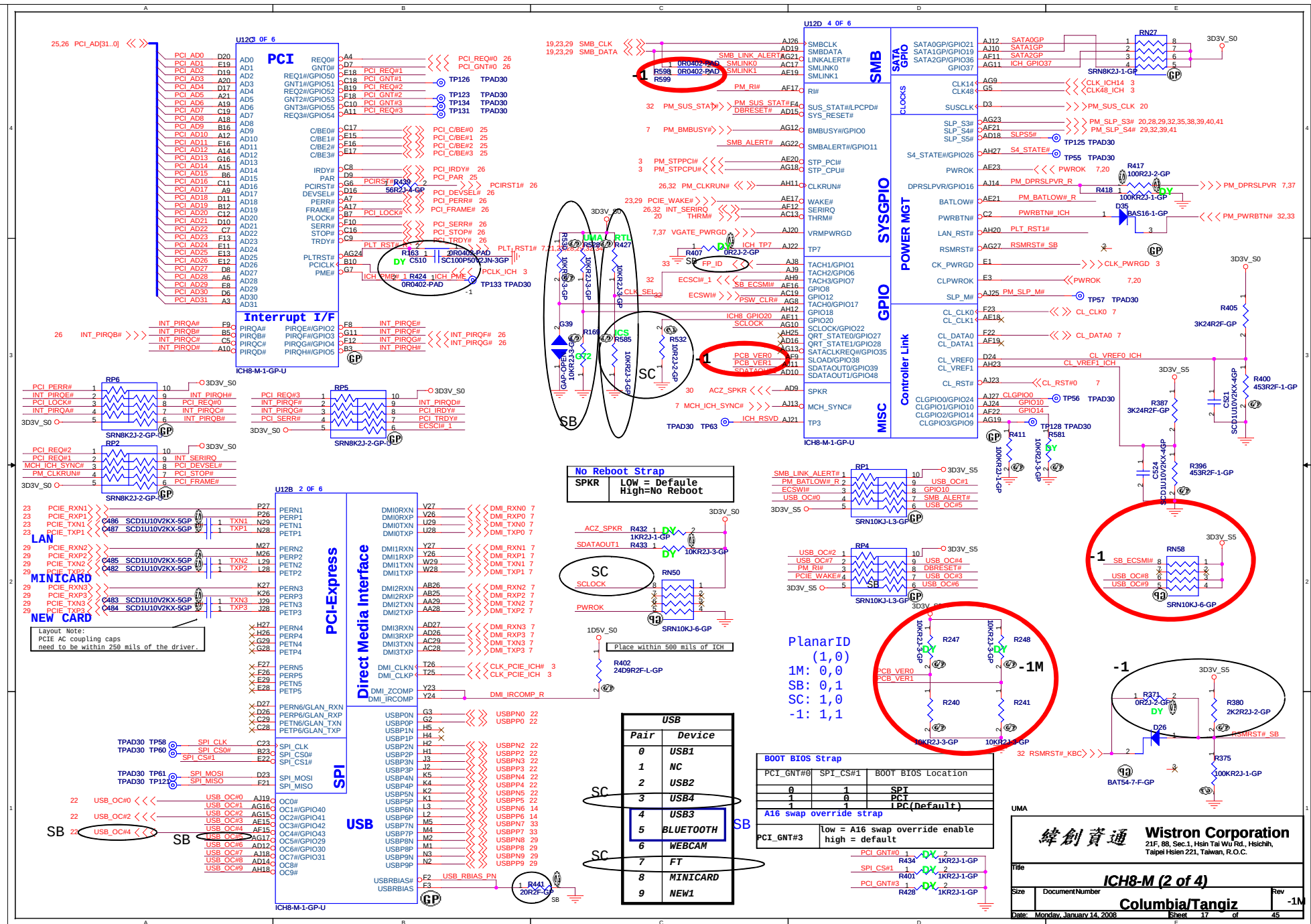
TV CONN

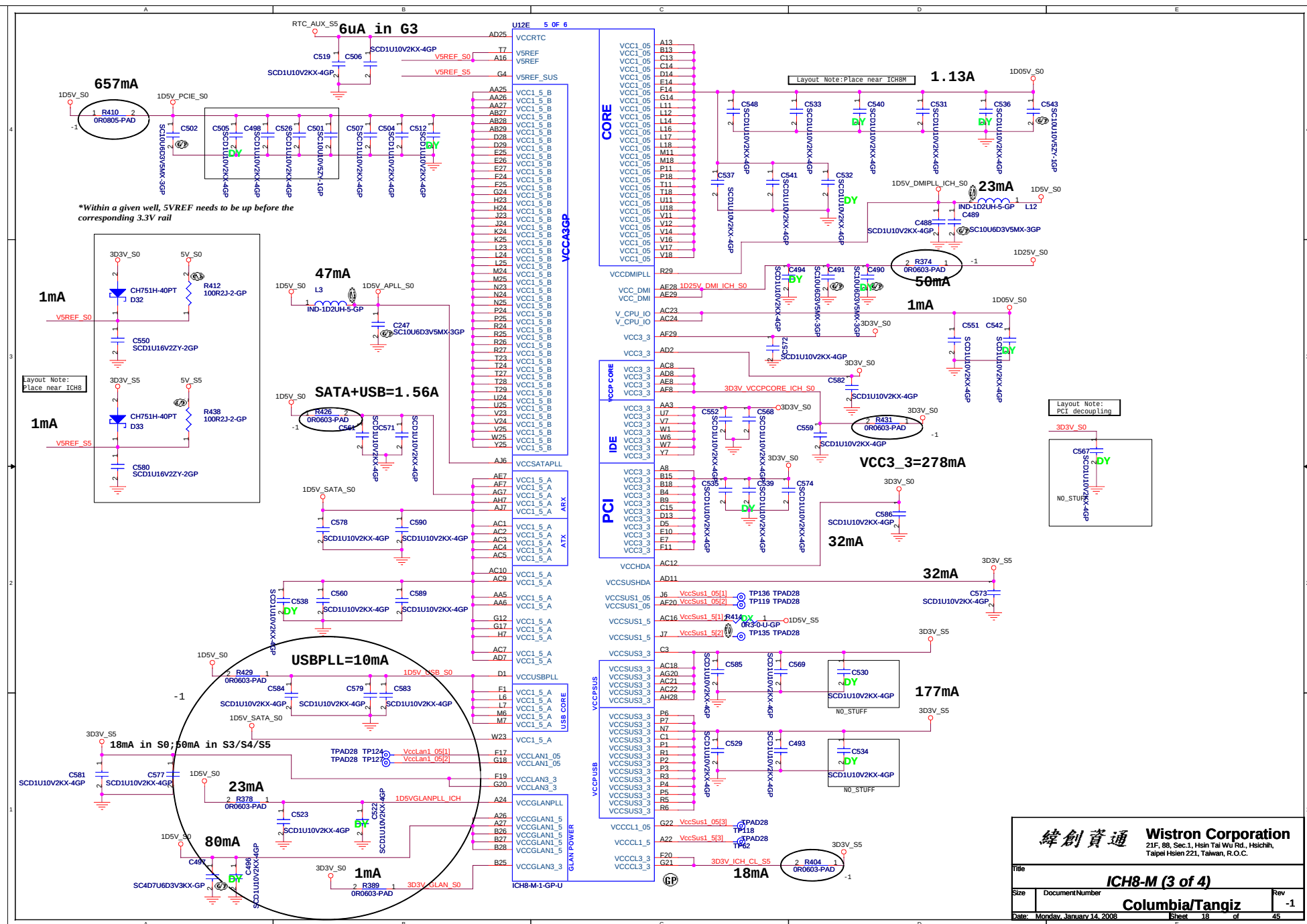


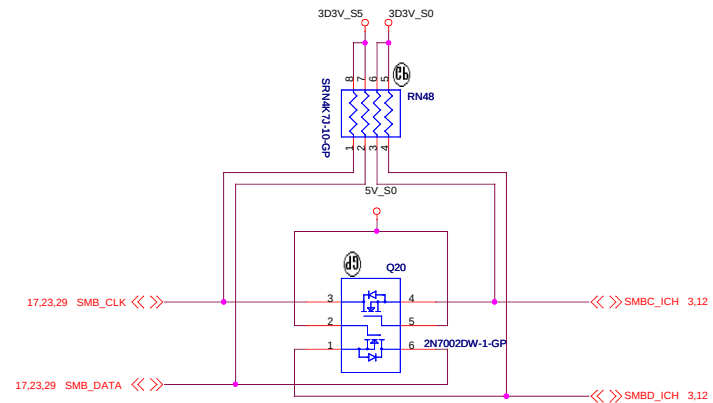
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CRT/TV Connector		
Size	Document Number	Rev
	Columbia/Tangiz	-1
Date	Monday, January 14, 2008	Sheet 15 of 45





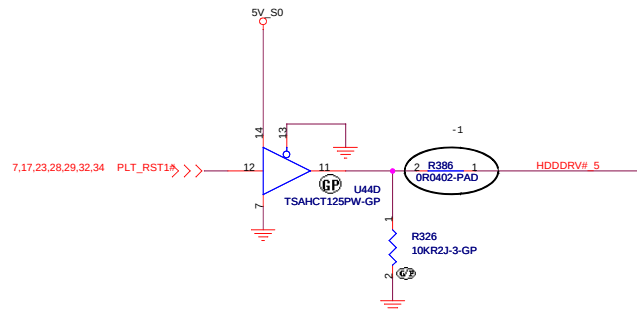
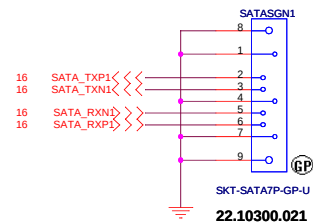
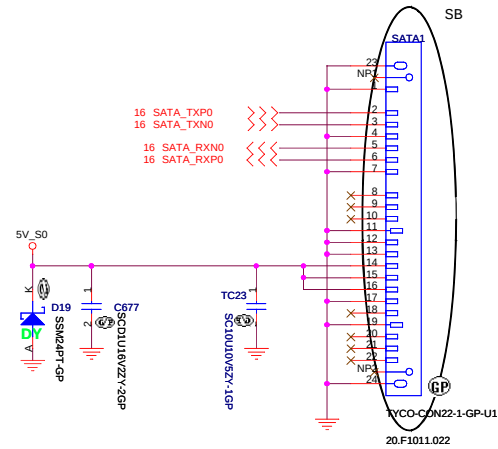




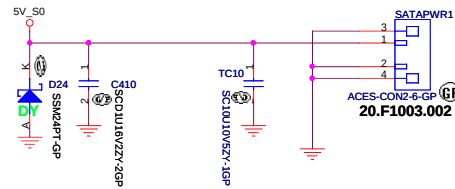
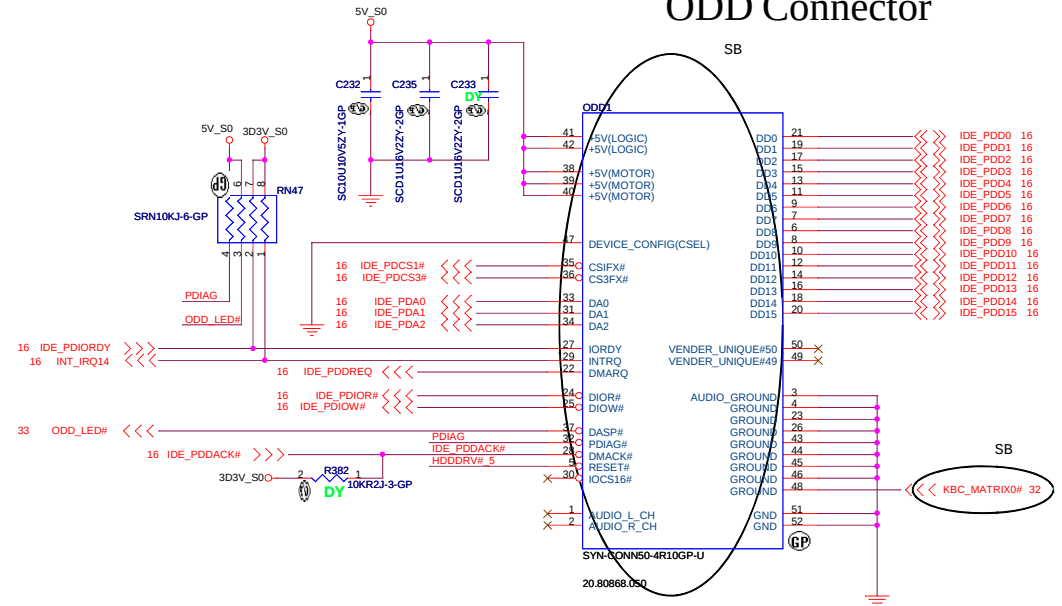
SMBUS

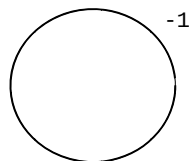
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Heichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
ICH8-M (4 of 4)	
Size	Document Number
Columbia/Tangiz	
Date: Monday, January 14, 2008	Sheet 19 of 45
-1	

SATA HD Connector



ODD Connector



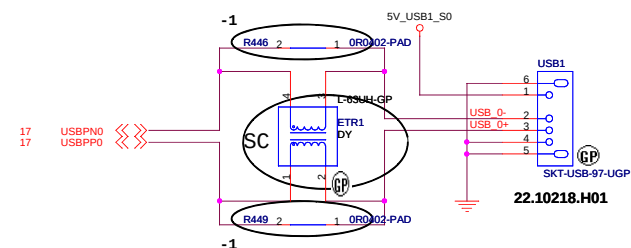
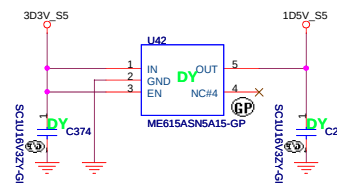


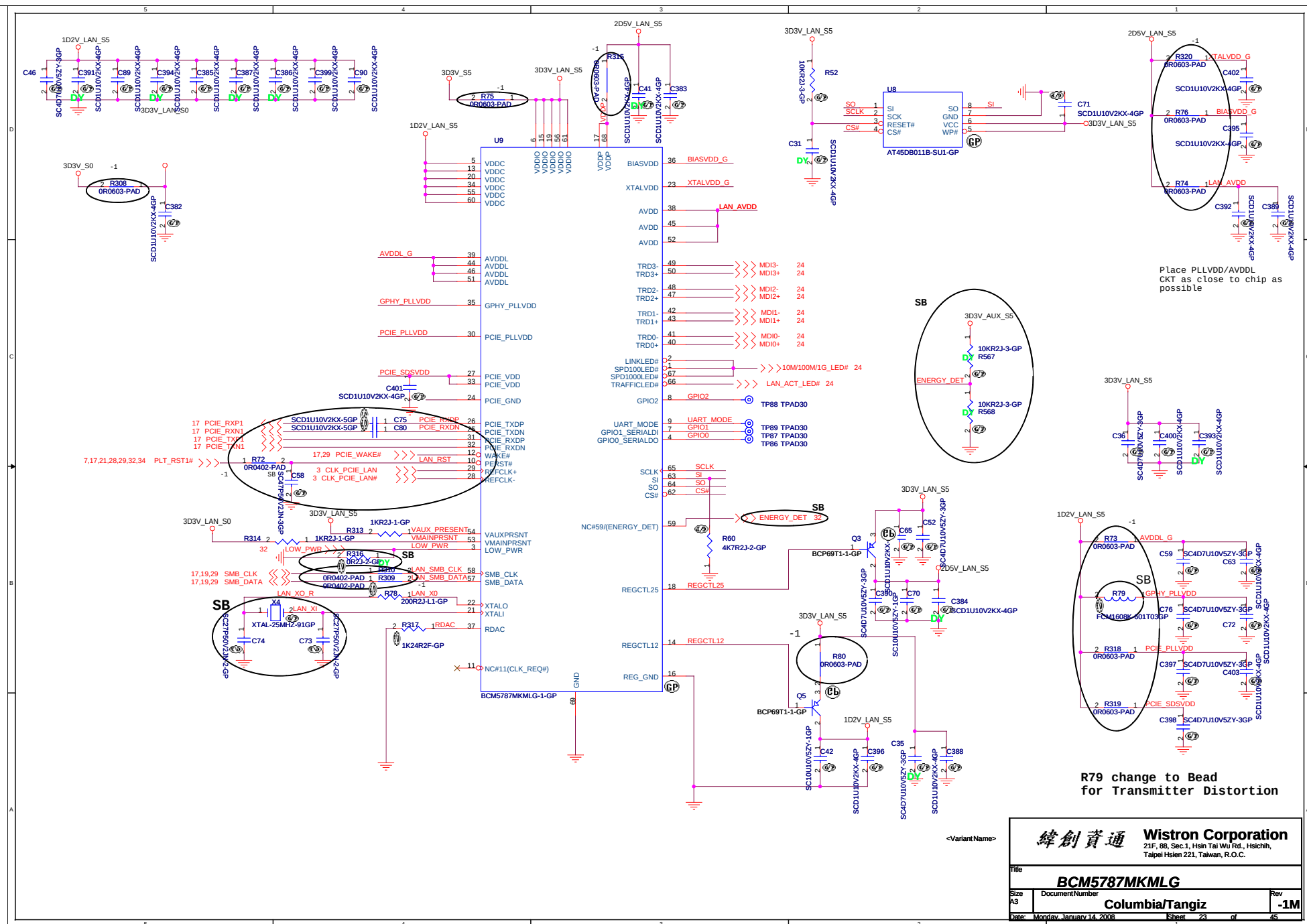
Pin 1 connection diagram for U16 (G528P11F-GP). The diagram shows the following connections:

- Pin 1 (GND) is connected to 5V_S5.
- Pin 2 (OUT) is connected to USB_PWR_EN#.
- Pin 3 (IN) is connected to 5V_USB1_S0.
- Pin 4 (EN#/EN) is connected to USB_OC#0.
- Pin 7 (OUT) is connected to 5V_USB1_S0.
- Pin 8 (OUT) is connected to 5V_USB1_S0.
- Pin 6 (OUT) is connected to 5V_USB1_S0.
- Pin 5 (OUT) is connected to 5V_USB1_S0.
- Pin 4 (EN#/EN) is connected to USB_OC#0.

[illegible]

20.D0197.104

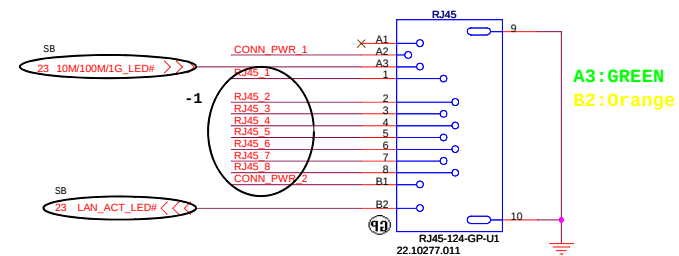
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LAN Connector

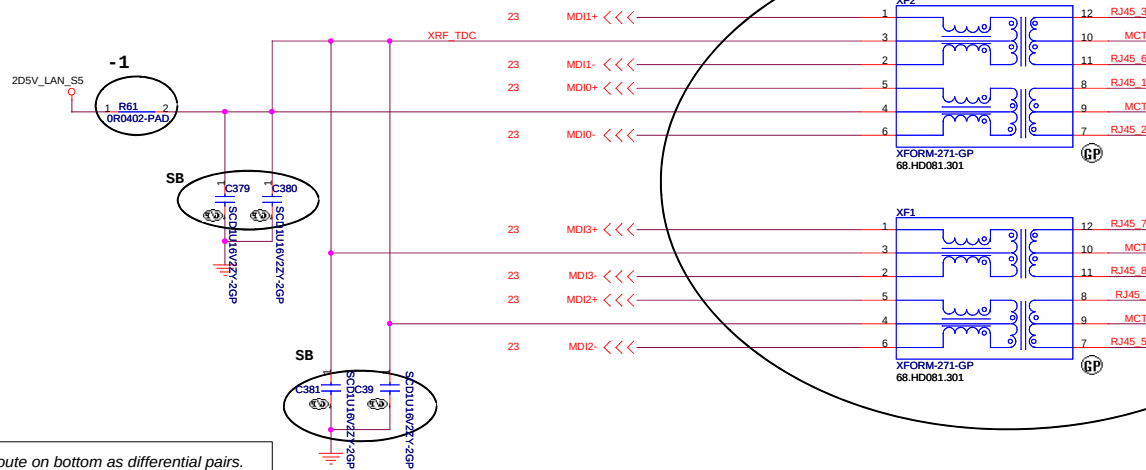
Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	

GIGA Lan Transformer



LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transferring data.

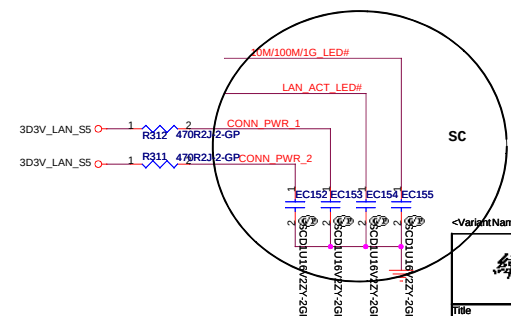
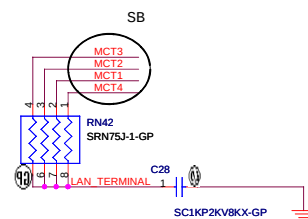


- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

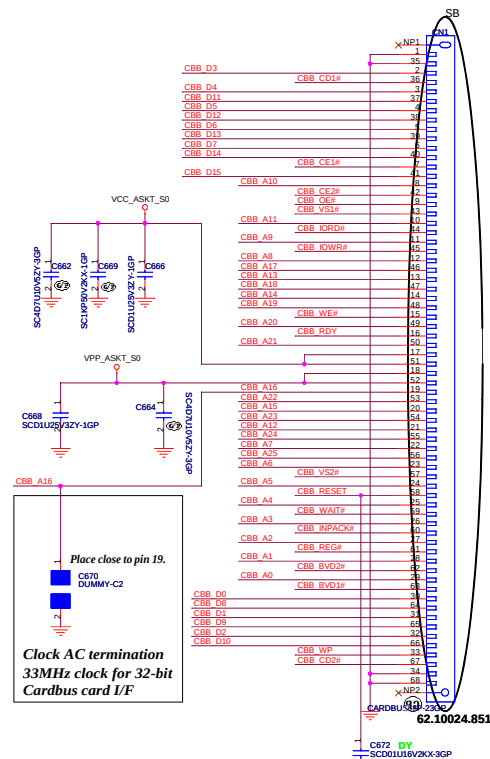
10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6



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Title: LAN Connector
Size: A3
Document Number: Columbia/Tangiz
Date: Monday, January 14, 2008
Sheet: 24 of 45
Rev: -1M

PCMCIA Socket

**Cardbus I/F**

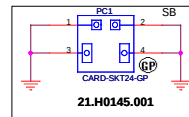
```

CBB_D[15..0]  << CBB_D[15..0]  25.26
CBB_A[25..0]  << CBB_A[25..0]  25.26

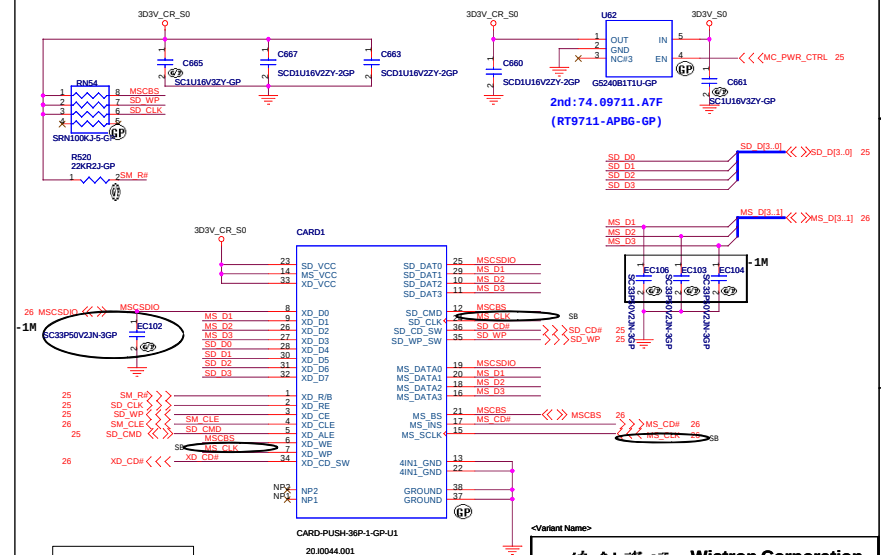
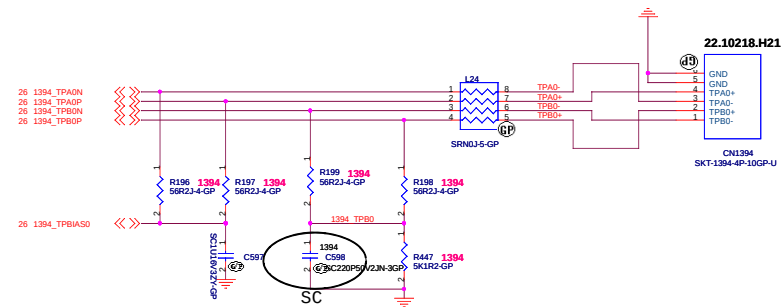
-- << CBB_IORD#  25
-- << CBB_IOWR#  25
-- << CBB_OE#   25
-- << CBB_WE#   25
-- << CBB_REG#  25
-- << CBB_RDY   26
-- << CBB_WP    26
-- << CBB_RESET
-- << CBB_WAIT# 26
-- << CBB_INPCK# 26

-- << CBB_CE1#  25
-- << CBB_CE2#  25
-- << CBB_BVD1# 26
-- << CBB_BVD2# 26
-- << CBB_CD1#  26
-- << CBB_CD2#  26
-- << CBB_VS1#  26
-- << CBB_VS2#  26

```

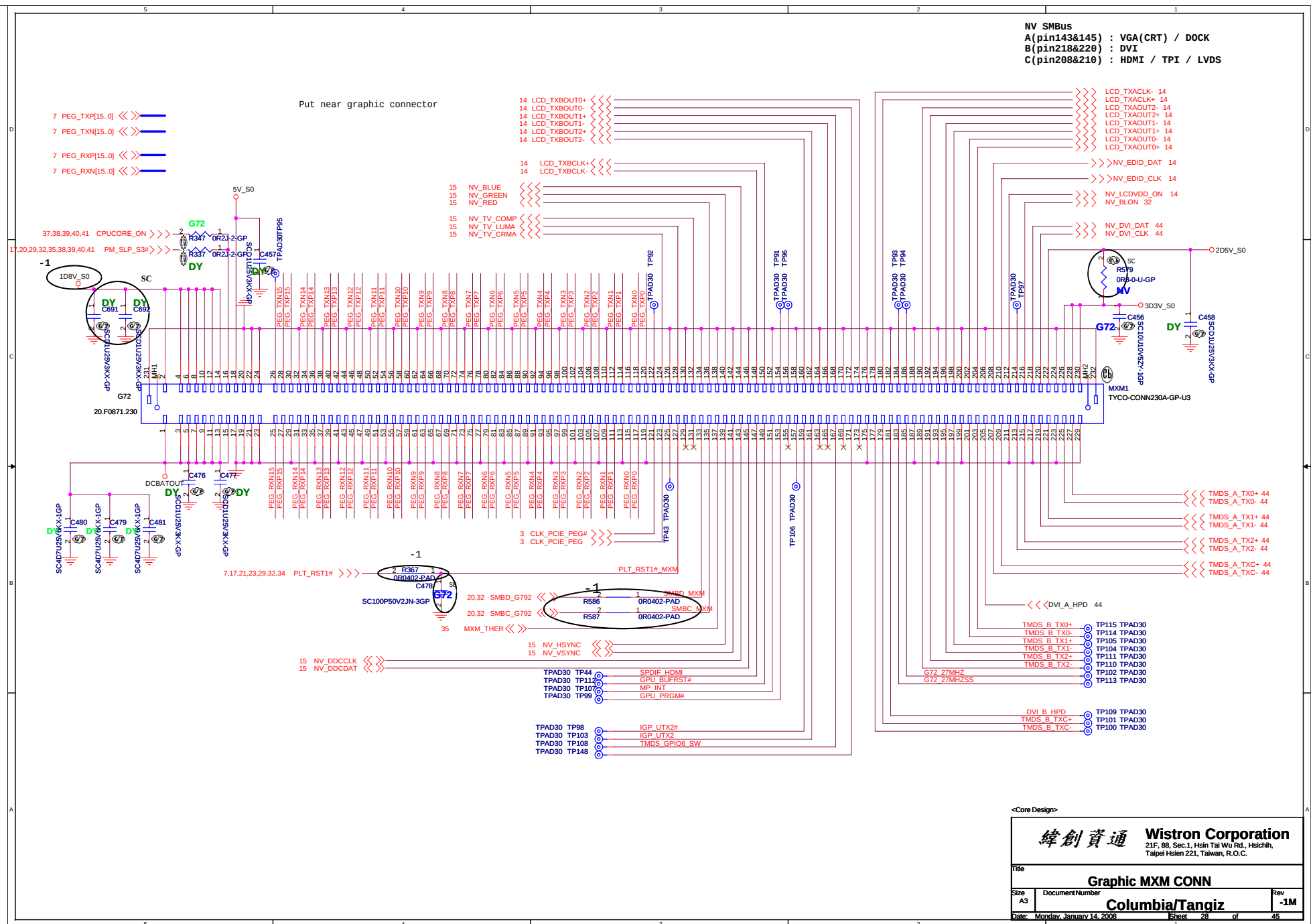


1394 Connector

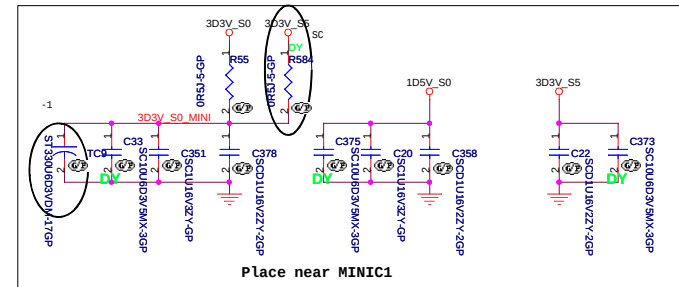
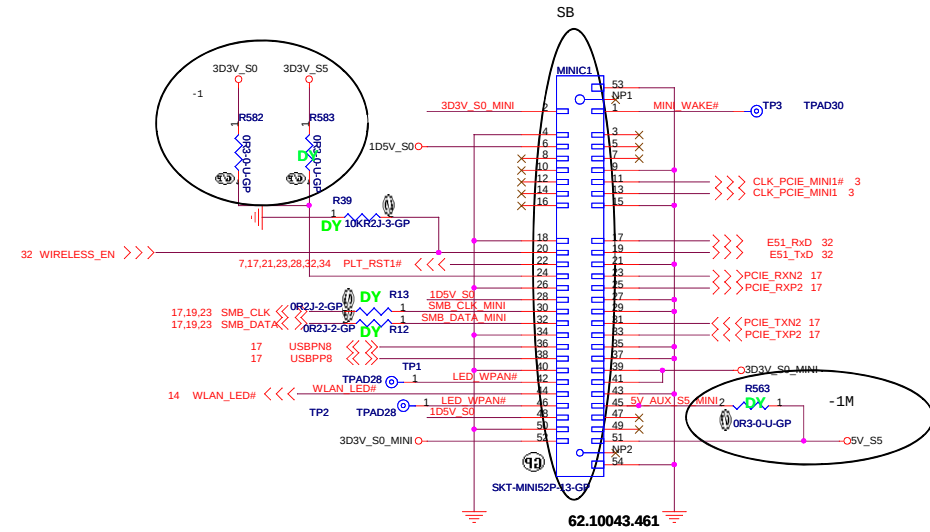
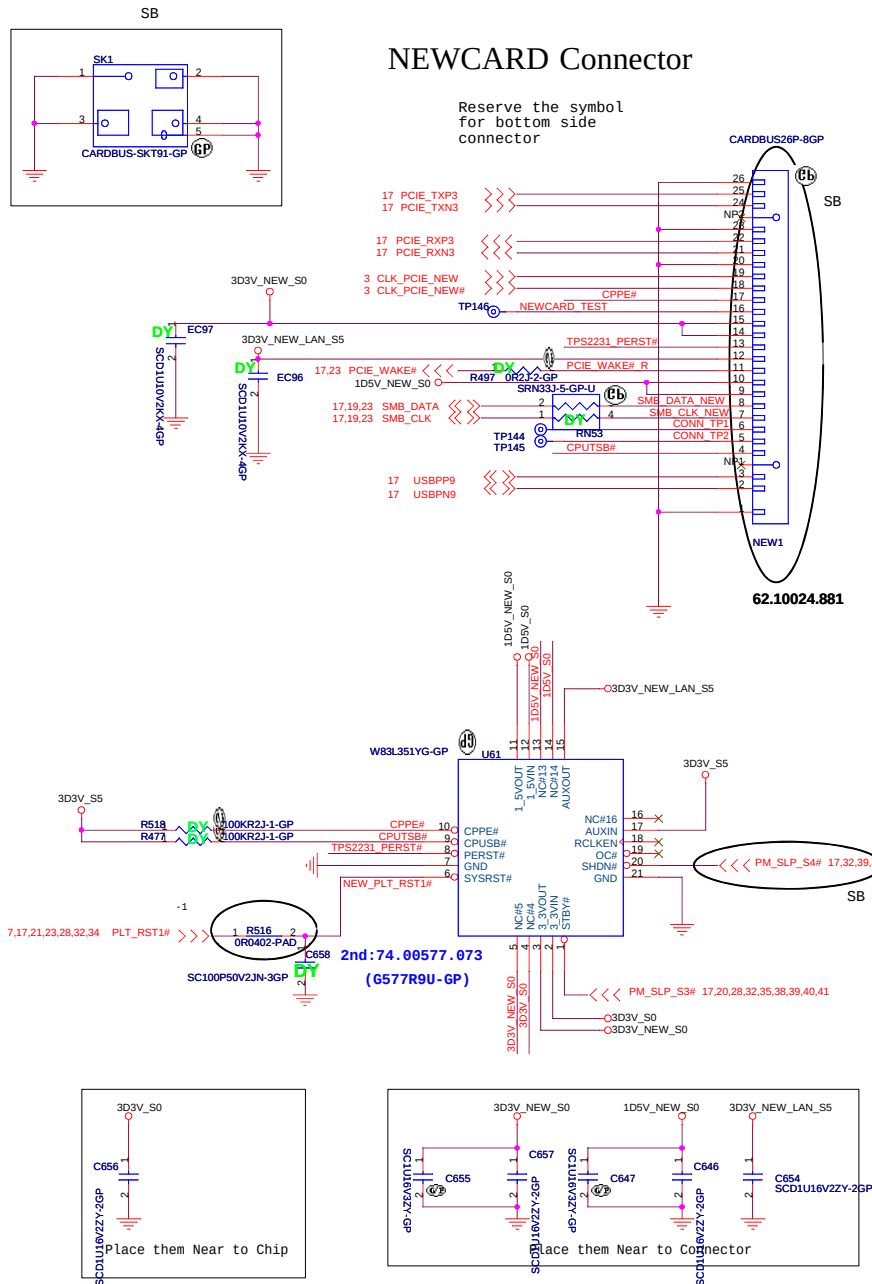


XD
MS / MS PRO
SD / SD IO / MMC

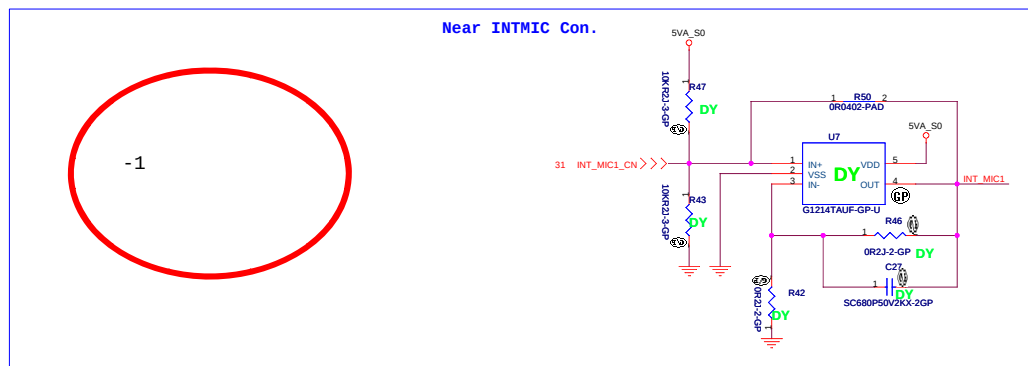
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Title PCMCIA / 1394 / CARD READER					
Size Document Number				Rev -1M	
Date Monday, January 14, 2008		Sheet 77		of 85	
Columbia/Tangiz					



Mini Card Connector



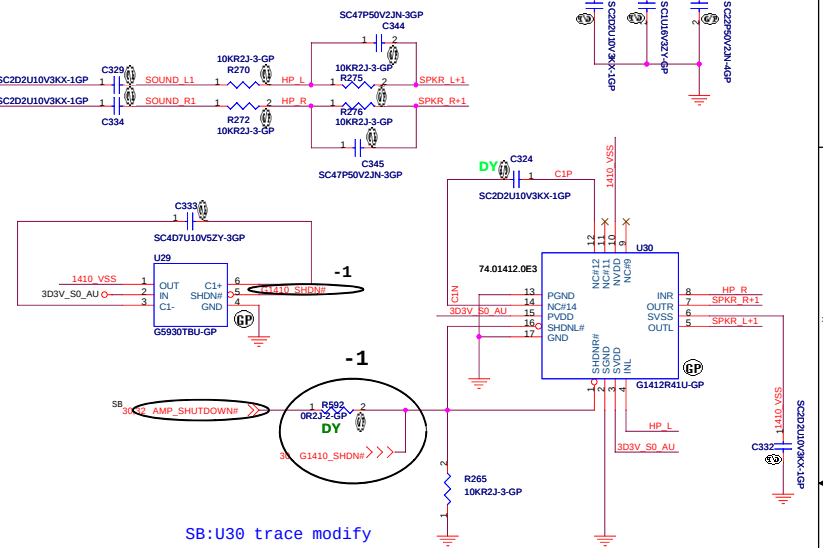
bom1	
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
MINI CARD / NEW CARD Columbia/Tangiz	
Size	Rev
Document Number	-1M
Date: Monday, January 14, 2008	Sheet 20 of 45



```
R, L 1.5W Speaker
mount R274, R281
R269->63.363334.1DL
R268->63.333334.1DL

R, L 1W Speaker
mount R280, R281
R269->63.153334.1DL
R268->63.123334.1DL

R, L 1.2W Speaker
mount R280, R281
R269->63.103334.1DL
R268->63.682334.1DL
```



The schematic diagram illustrates the audio input section of the 22.10133.B11 board. It features a -1M resistor network connected to LINE_IN_R and LINE_IN_L. The signals pass through a 1K resistor (R290) and a 1K resistor (R288) to the inputs of the IC1 (SC1KP50VZX1-GP) and IC2 (SC1KP50VZX1-GP). The outputs of the ICs are connected to the PHONE-JK234-GP connector. The diagram also shows a 30V supply and a 1M resistor (R291) connected to the inputs.

SPKR L-
SPKR L+
SPKR R-
SPKR R+

1M1G0402220VW
EC156
dP-DP

1M1G0402220VW
EC157
dP-DP

1M1G0402220VW
EC158
dP-DP

1M1G0402220VW
EC159
dP-DP

-1M

SPKR1
ACES-CON4-1-GP
20D1197.104
-1

30 MIC_JD1

AUD_MIC_R

AUD_MIC_L

-1M

R291 1K

R292 1K

R293 1K

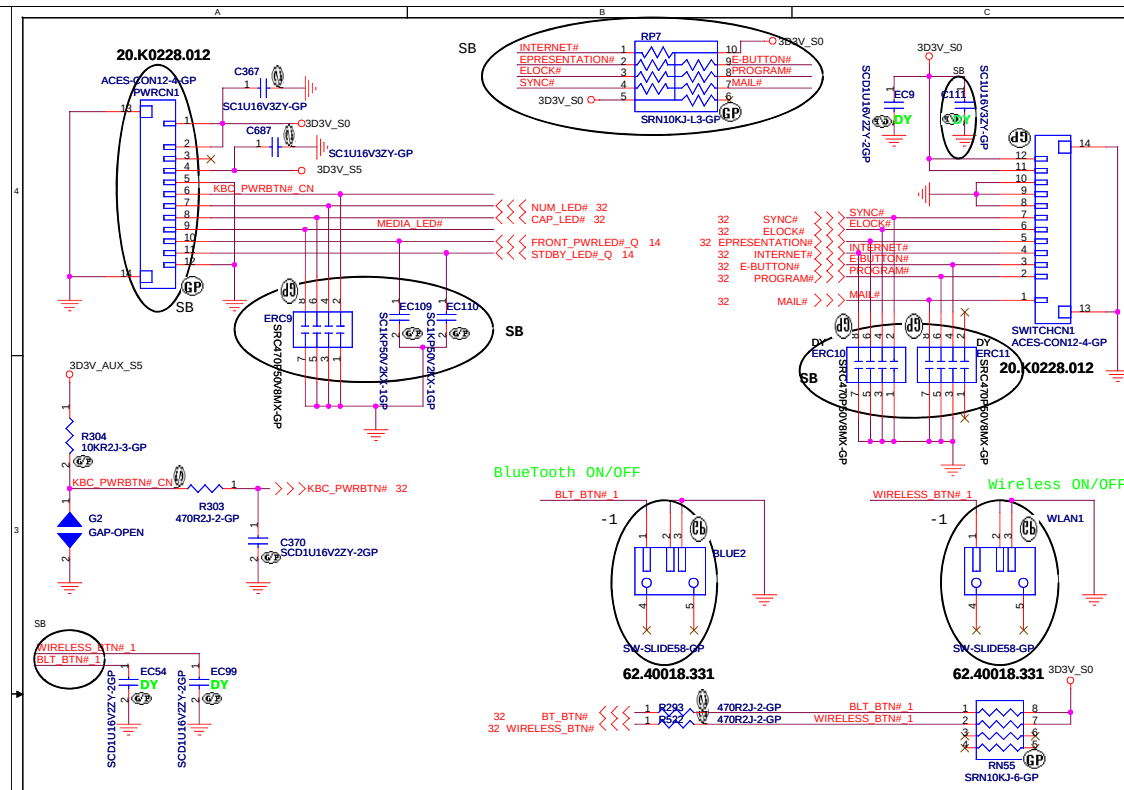
R294 10K

EC50 SC1KP50V2K-1GP

EC53 SC1KP50V2K-1GP

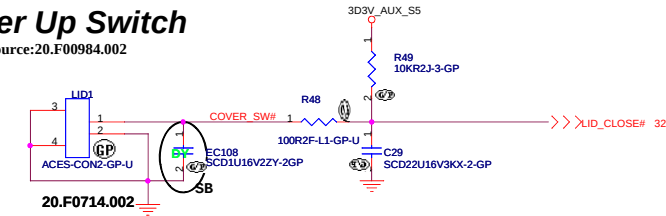
PHONE_J2233-GP

22.1033.B01

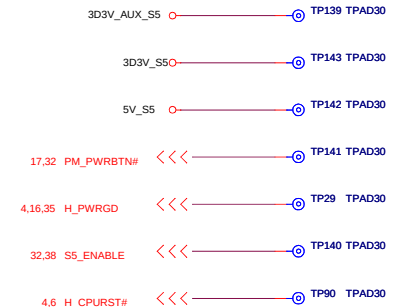


Cover Up Switch

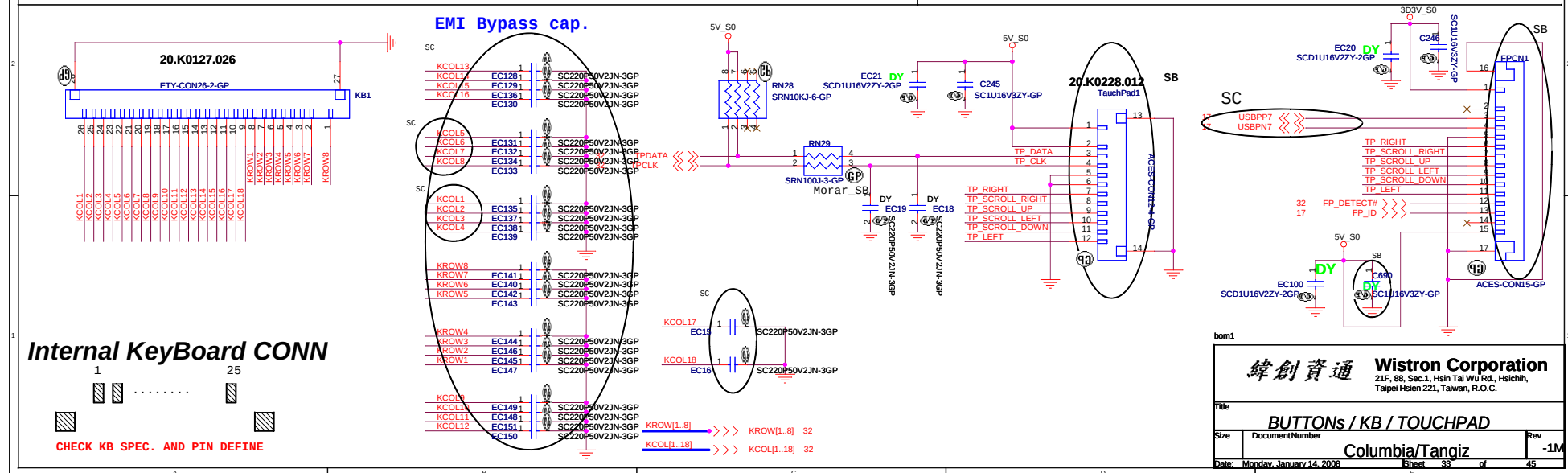
2nd source:20.F00984.002



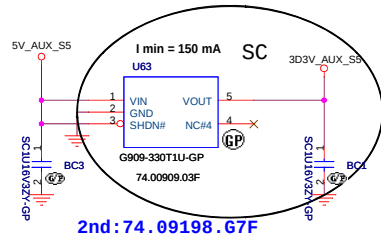
Check test point



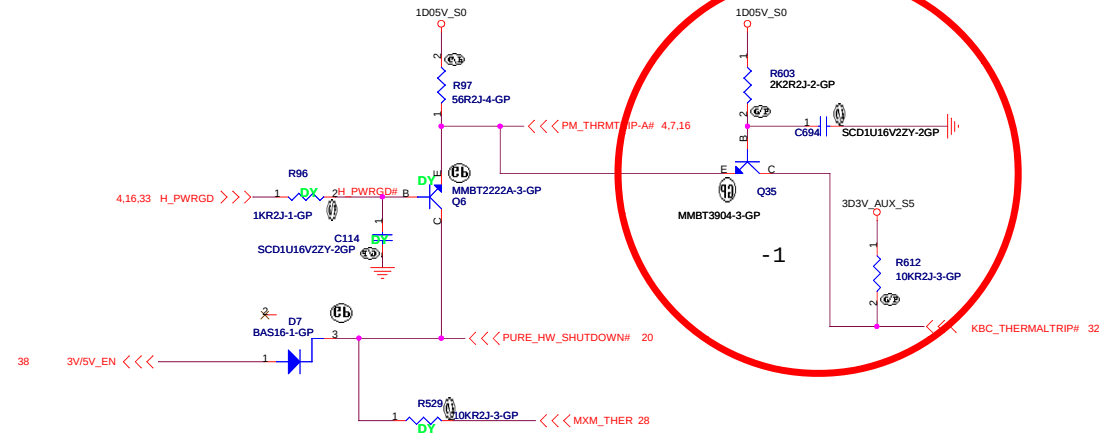
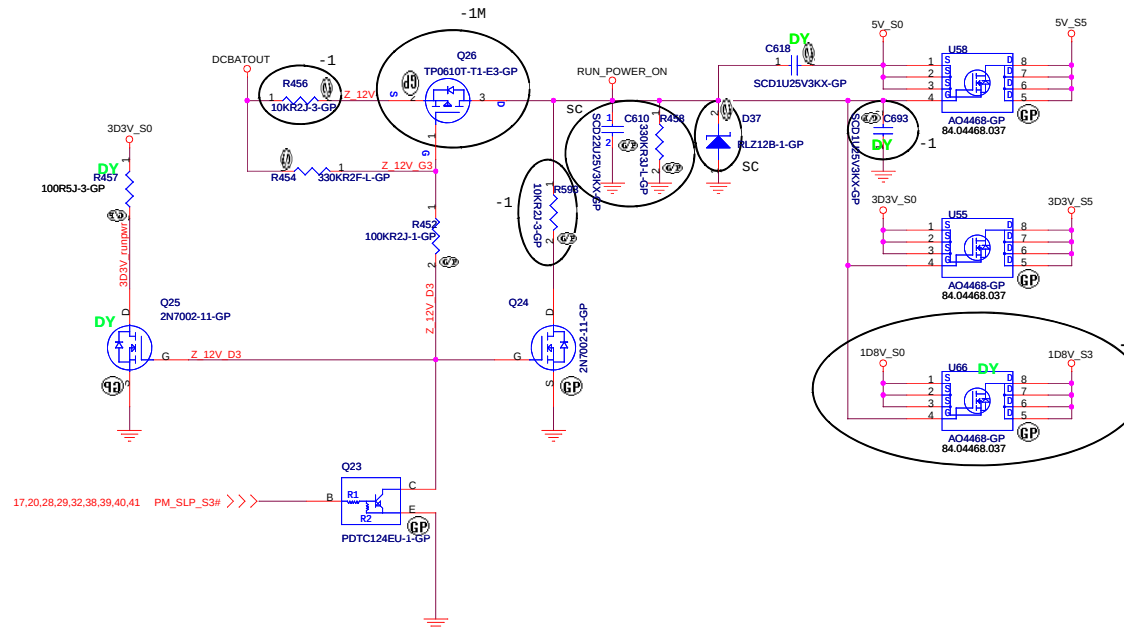
Test Point放在Dimm Door打開可量測處



Aux Power 3D3V_AUX_S5



Run Power



UMA

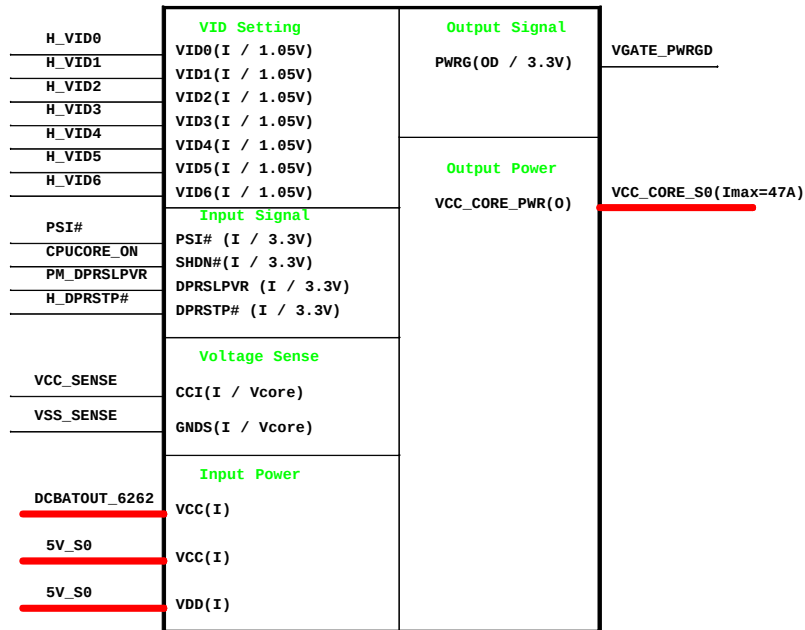
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Heilich,
Taipei Hsien 221, Taiwan, R.O.C.

Title **RUN POWER and 3D3V_AUX_S5**

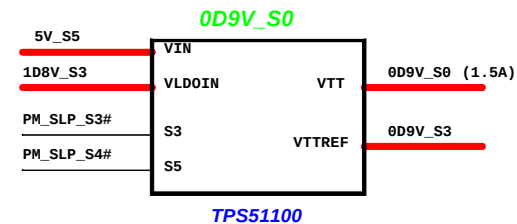
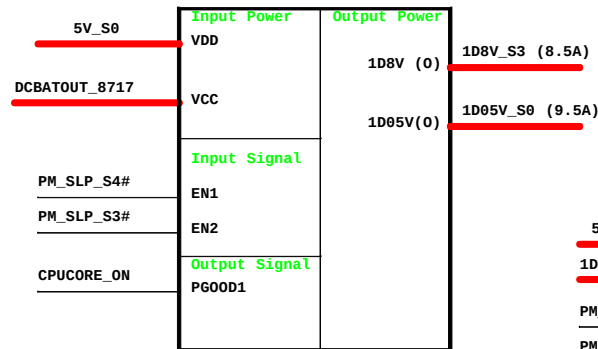
Size Document Number **Columbia/Tangiz** Rev **-1M**

Date: Monday, January 14, 2008 Sheet 35 of 45

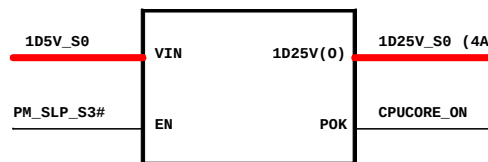
CPU_CORE
MAX8770



MAX8717
1D8V/1D05V

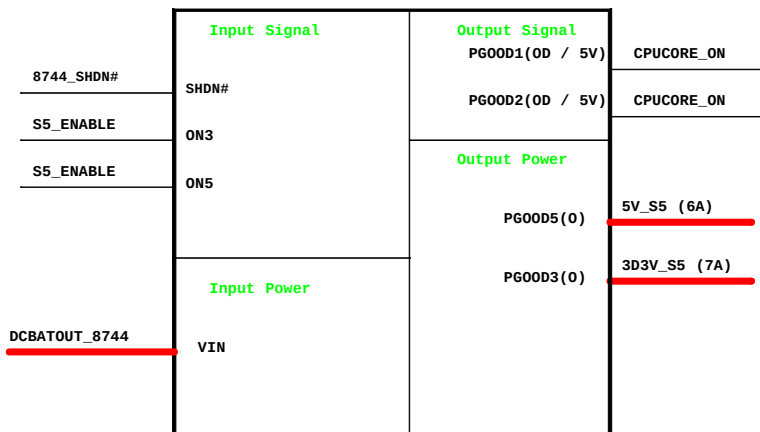


1D25V_S0

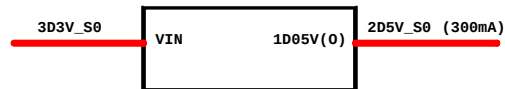


APL5915

MAX8744
5V/3D3V

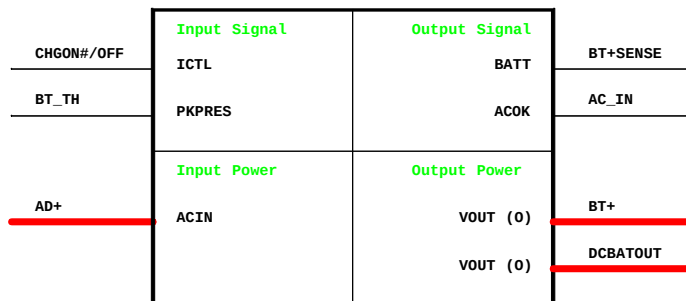


2D5V_S0

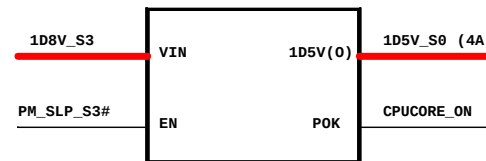


APL5308

Charger ISL6255



1D5V_S0

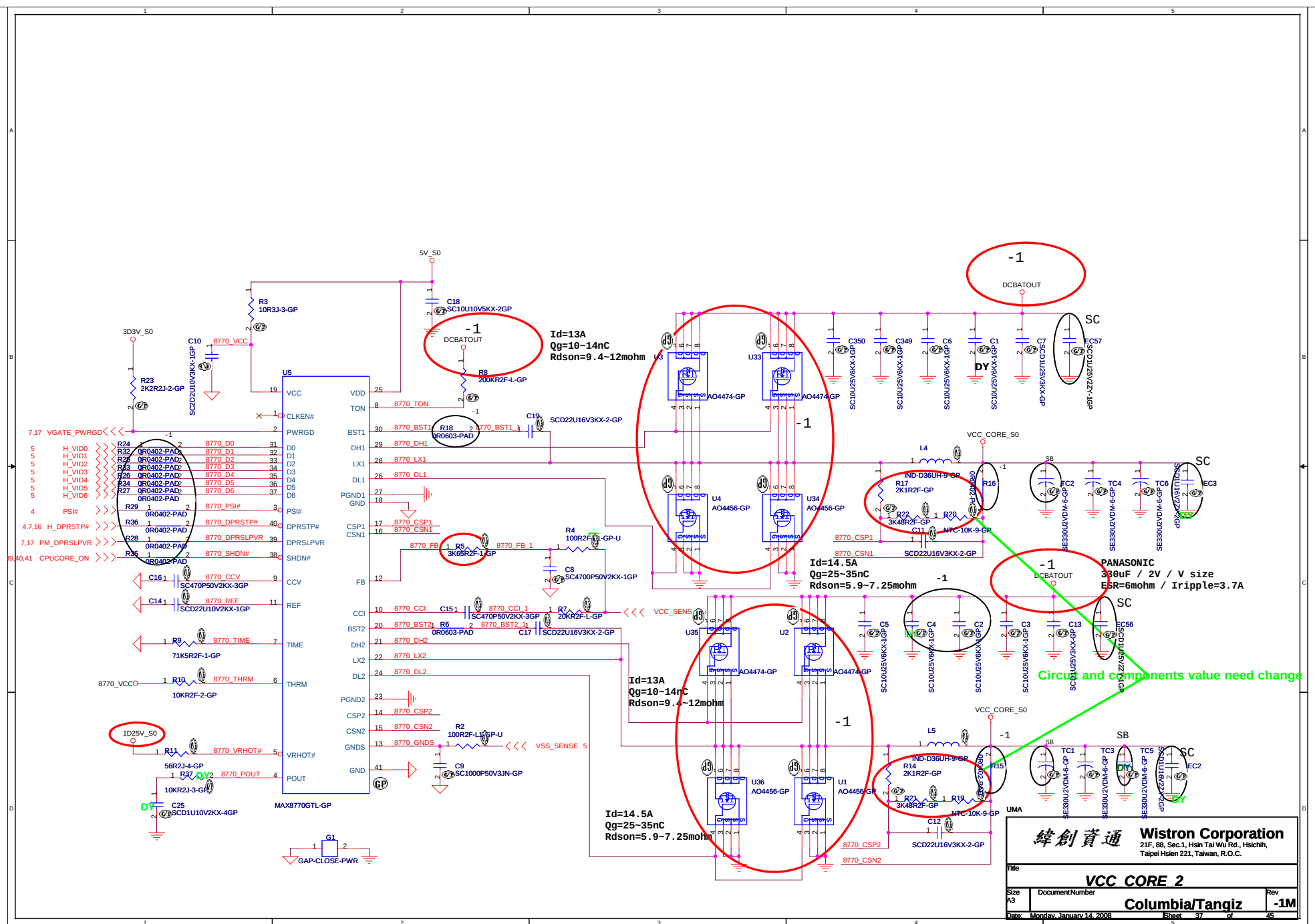


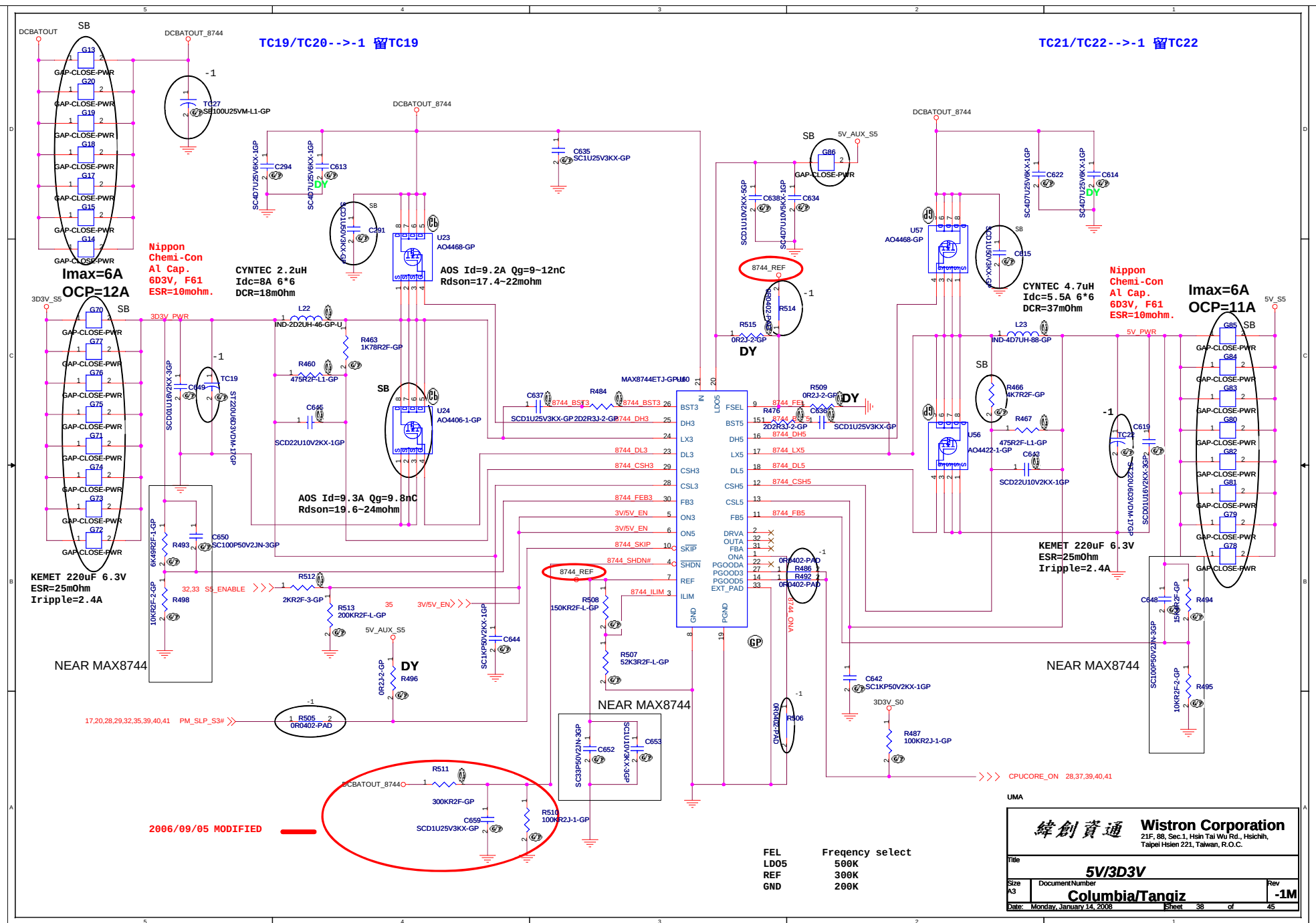
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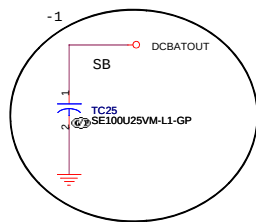
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緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Power Block Diagram	
Size	Document Number
A3	
Date	Monday, January 14, 2008
Sheet	36 of 45
Rev	-1M

Columbia/Tangiz



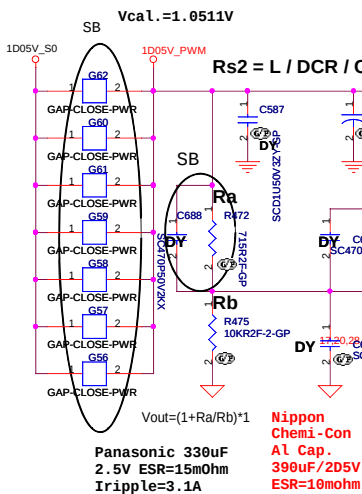




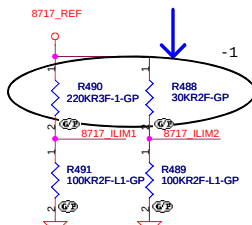
TC15/TC16-->-1 留TC15

TC17/TC18-->-1 留TC17

1D05V Iomax=12A
OCP>19A

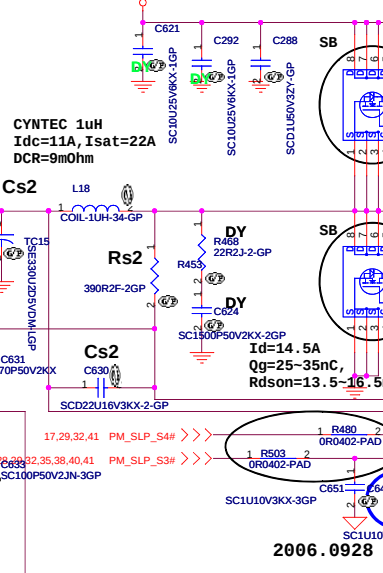


Adjust the current limit threshold from R14, R15

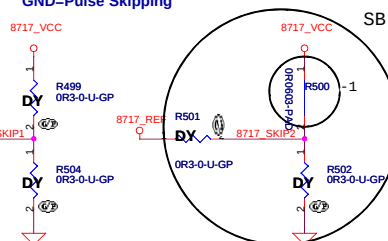


VILIM = 0.5V~2.0V
Output Current =
ILIM / 10 / LDCR - di/2

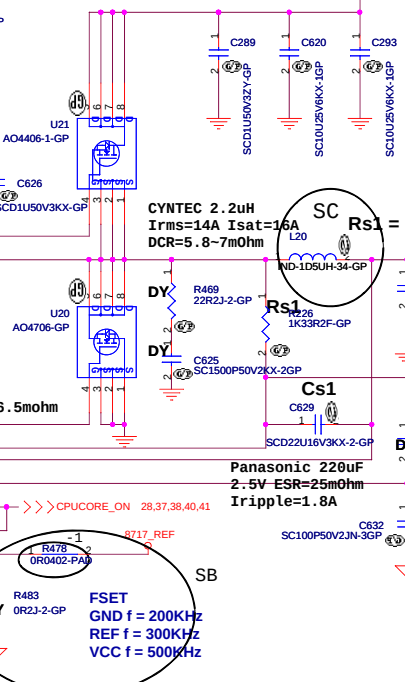
Id=13A
Qg=18~14nC,
Rdson=9.4~12mohm



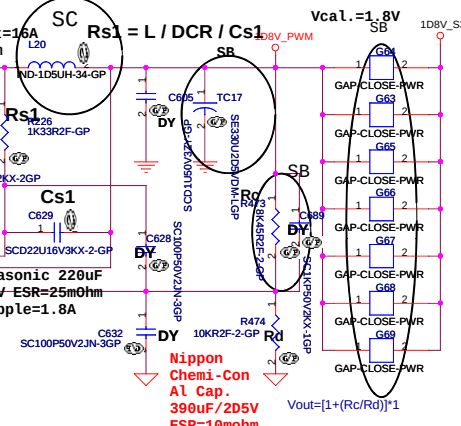
SKIP
VCC=Force PWM
REF=Low noise
GND=Pulse Skipping



Id=9.2A
Qg=9~12nC,
Rdson=17.4~22mohm



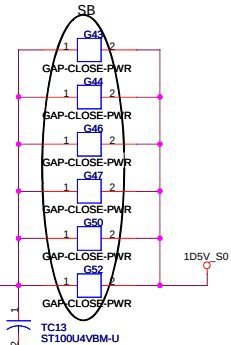
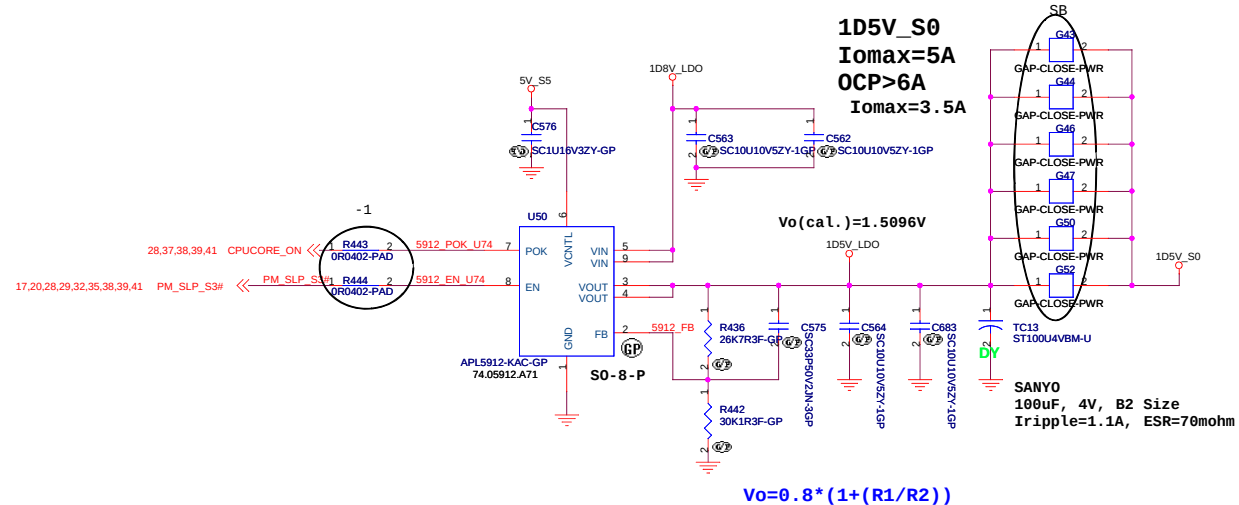
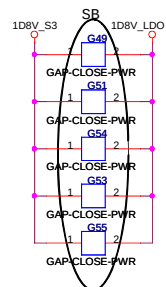
1D8V Iomax=9.5A
OCP>17A



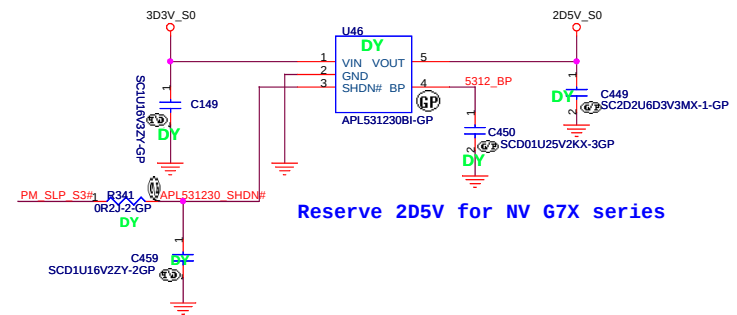
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taippei Hsien 221, Taiwan, R.O.C.

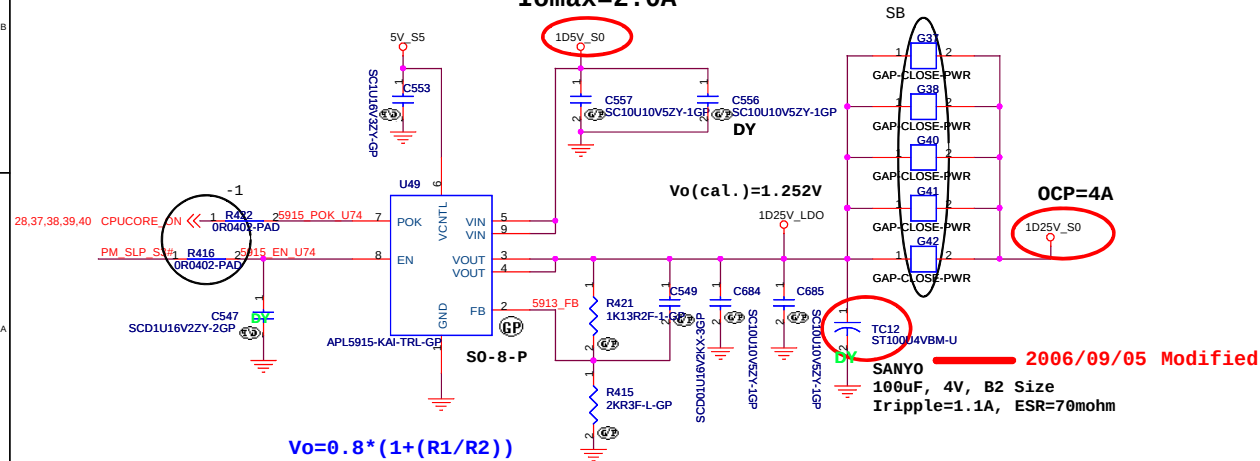
MAX8717 1D8V 1D05V			
Size	Document Number		Rev
A3		Columbia/Tangiz	-1M
Date	Monday, January 14, 2008	Sheet	39 of 45



2D5V
Iomax=130mA



1D25V_S0
Iomax=2.0A


$$V_0 = 0.8 * (1 + (R_1/R_2))$$

UMA

緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

1	Title	Date	Page
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1D25V/2D5V//1D05V/0D9V

Size

Document Number

Columbia/Tangiz

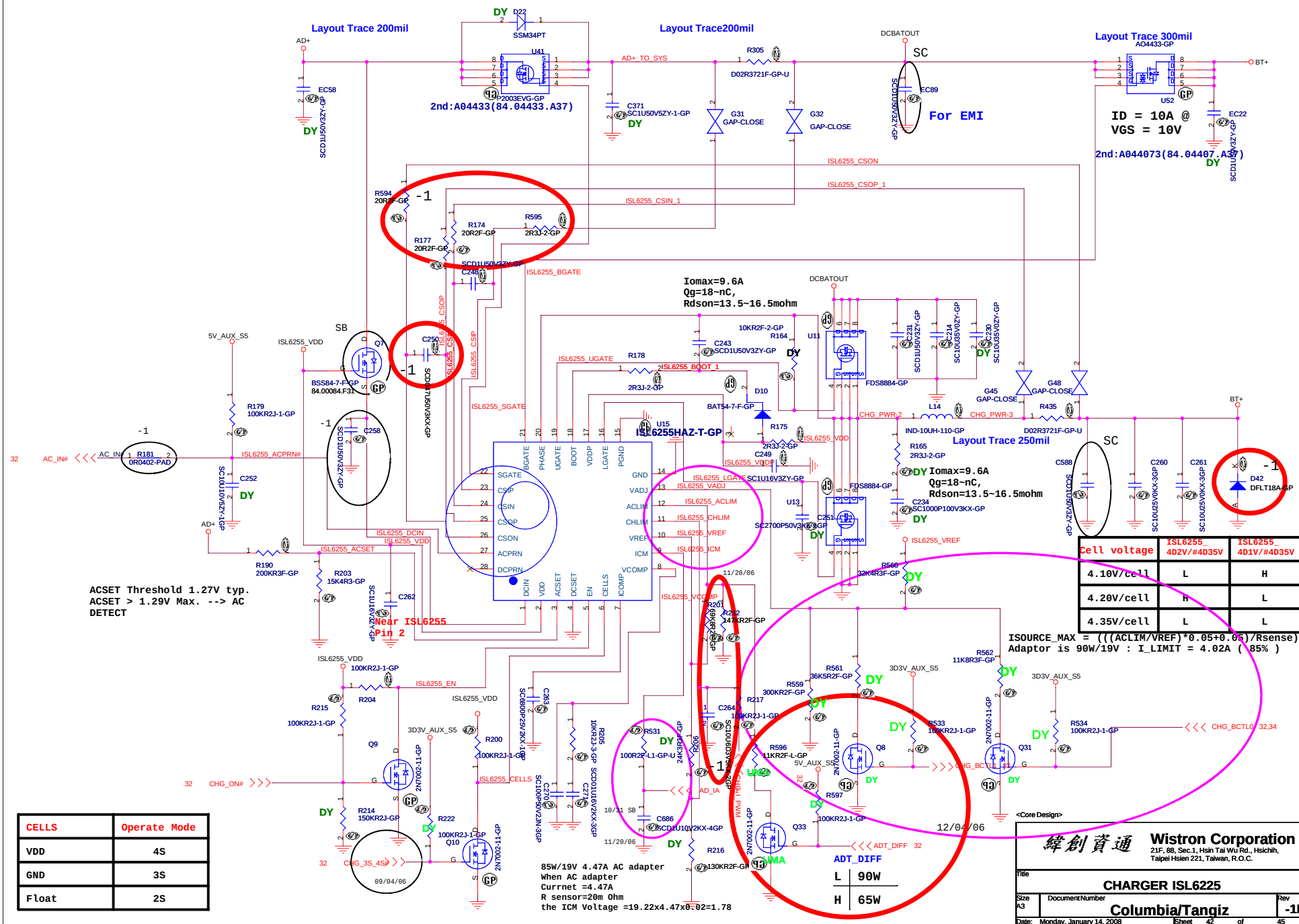
Date: Monday, January 14, 2008

Sheet

41

Rev	
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REV
-1M



CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

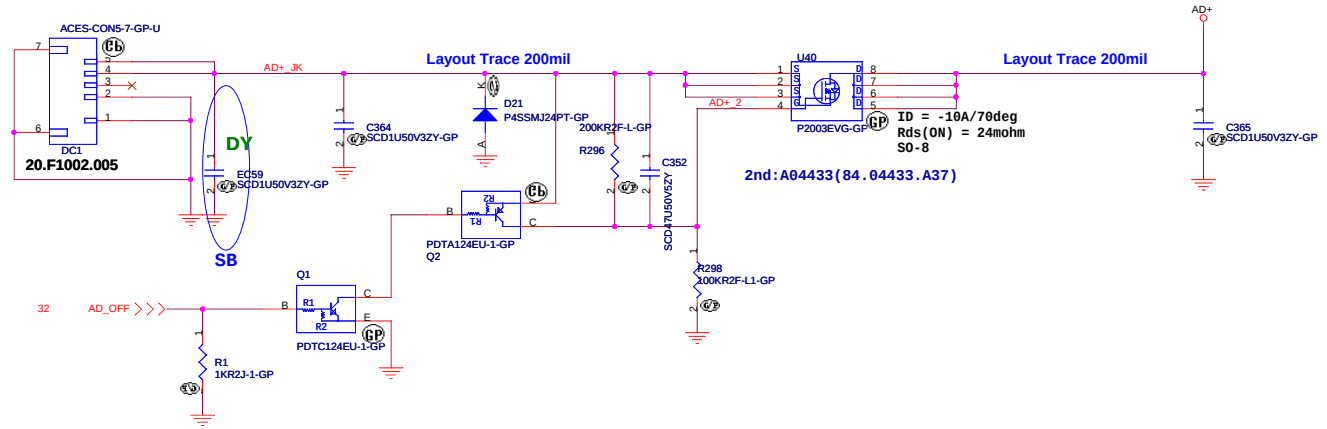
Cell voltage	ISL6255_ 4D2V/#4D35V	ISL6255_ 4D1V/#4D35V
4.10V/cell	L	H
4.20V/cell	H	L
4.35V/cell	L	L

ISOURCE_MAX = (((ACLIM/VREF)*0.05+0.05)/Rsense)
Adaptor is 90W/19V : I_LIMIT = 4.02A (85%)

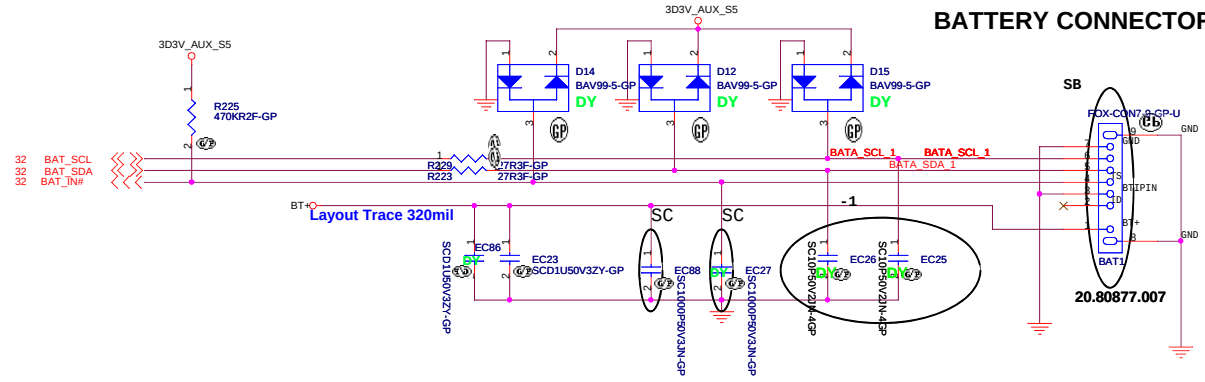
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Tainan Hsien 221, Taiwan, R.O.C.

Title			
CHARGER ISL6225			
Size A3	Document Number		Rev
	Columbia/Tangiz		-1
Date:	Monday, January 14, 2008	Sheet 42 of 45	

Adaptor in to generate DCBATOUT

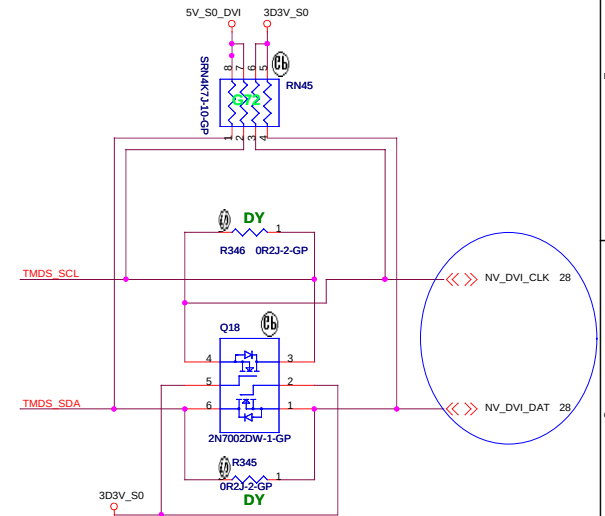
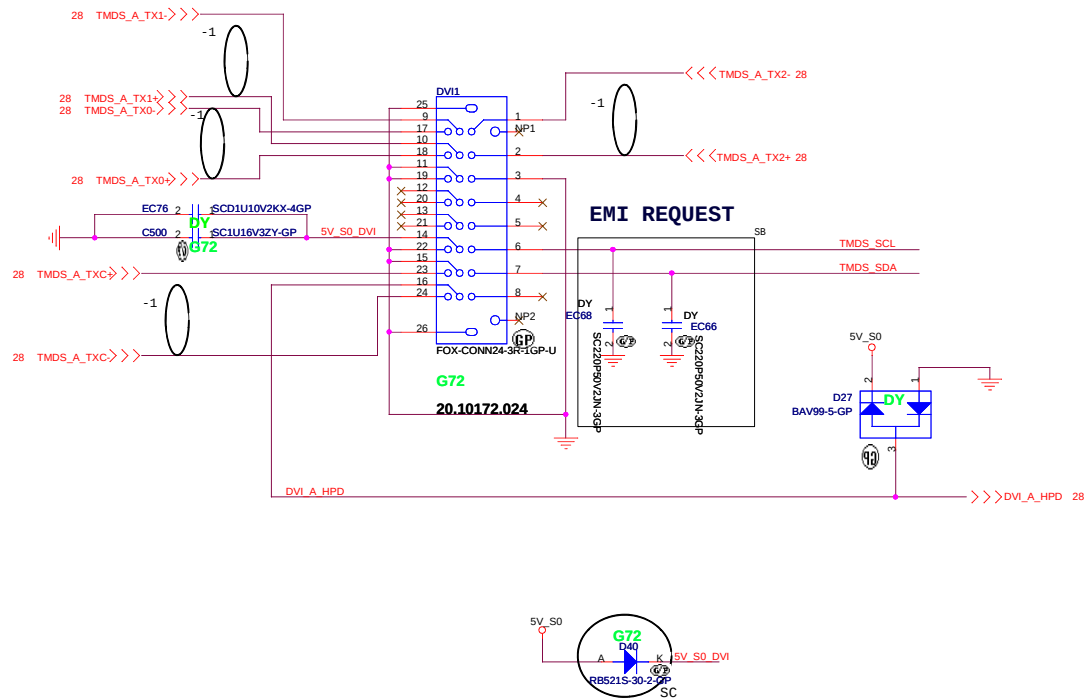


BATTERY CONNECTOR



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		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipet Hsien 221, Taiwan, R.O.C.	
Title			
AD/BATT CONN			
Size	Document Number	Rev	
A3		-1M	
Columbia/Tangiz			
Date:	Monday, January 14, 2008	Sheet	43 of 45



<VariantName>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
DVI CONNECTOR			
Size	Document Number	ColumbiaTangiz	Rev
A3			-1M
Date: Monday, January 14, 2008		Sheet 44 of	45

