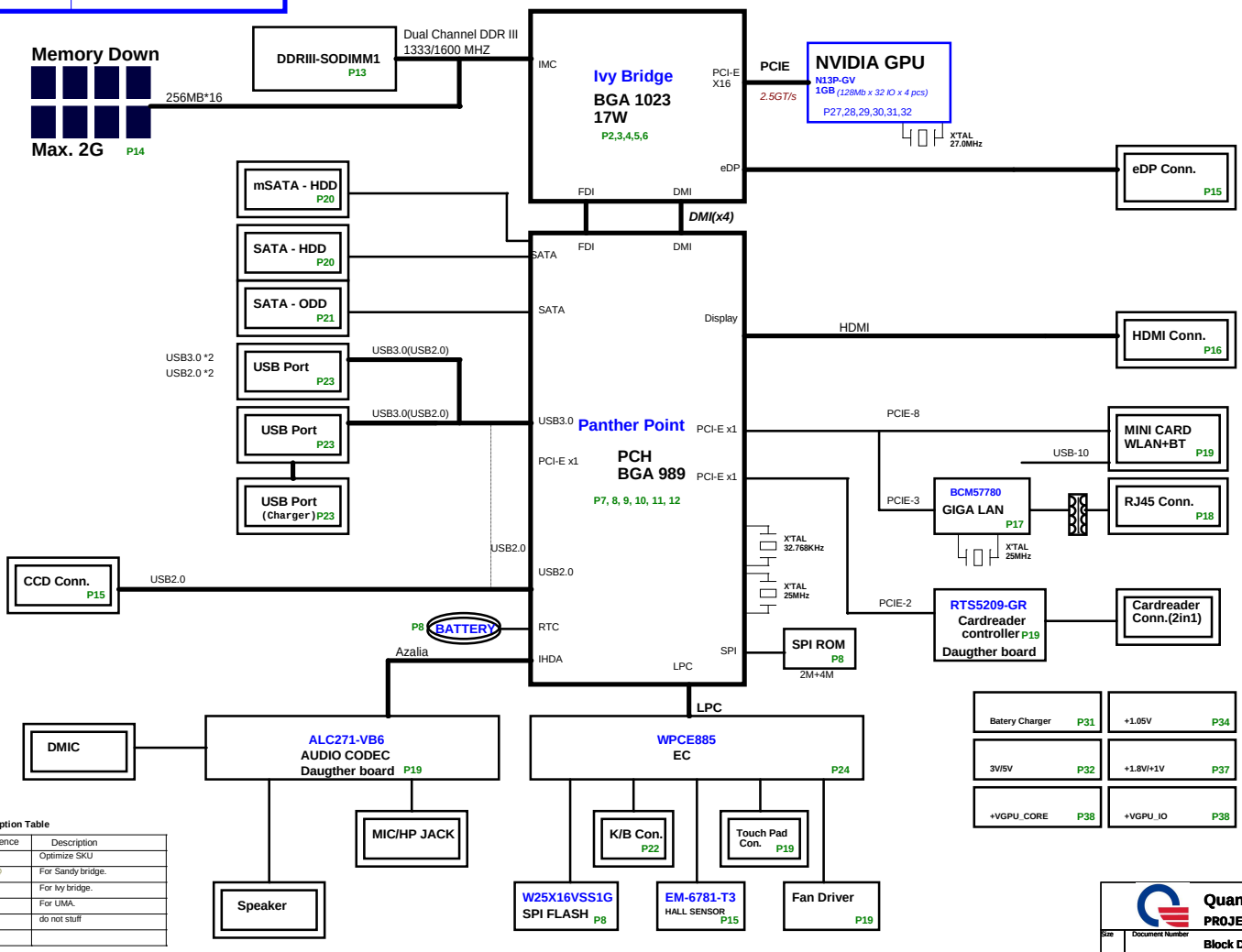
VER : 3A

BOM P/N	Description

Z09 SYSTEM BLOCK DIAGRAM



BOM Option Table

Reference	Description
EV@	Optimize SKU
SNB@	For Sandy bridge.
IVB@	For Ivy bridge.
IV@	For UMA.
*	do not stuff

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	Block Diagram	3A

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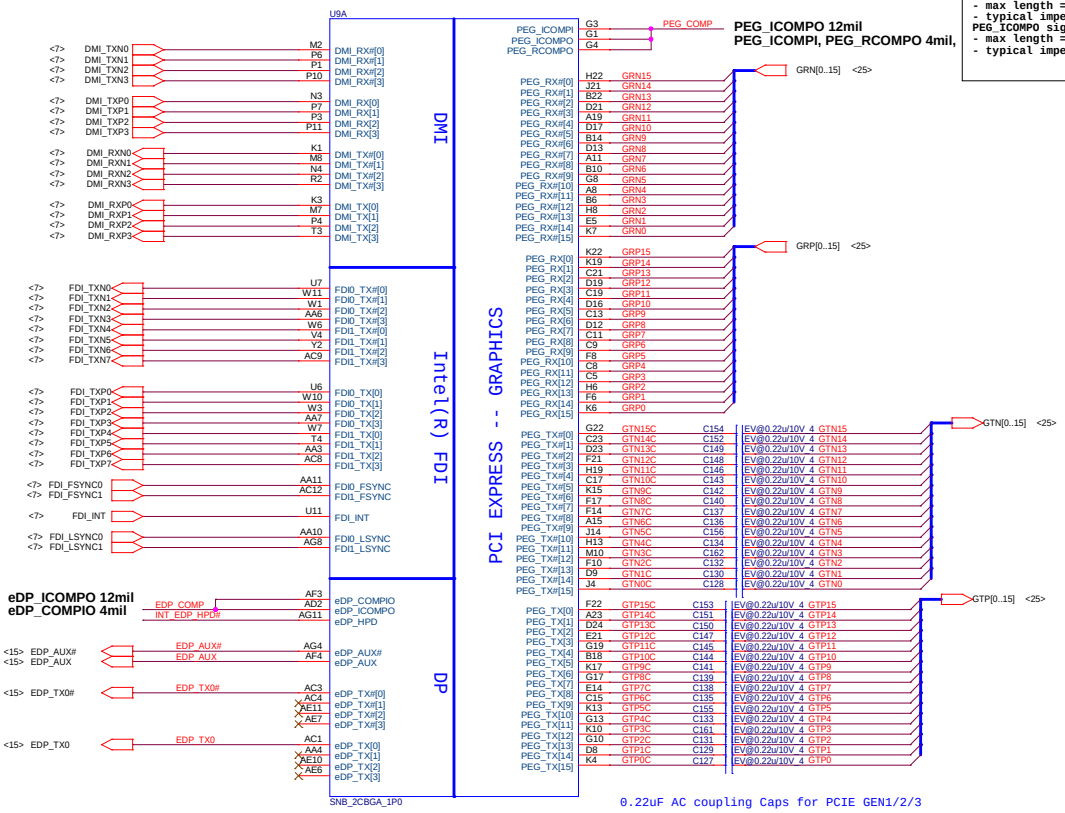
Ivy Bridge Processor (DMI,PEG,FDI)

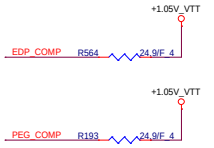
PEG_ICOMPI and RCOMPO signals
should be shorted and routed with
- max length = 500 mils
- typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with
- max length = 500 mils
- typical impedance = 14.5 mohms



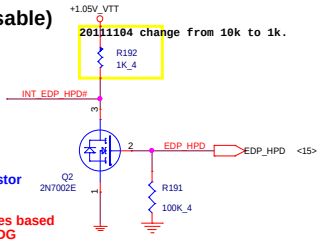
DG 1.0 :
The recommended AC cap value is changed to 220nF for compatibility with
PCIe Gen3 on future platforms.
For Gen2 only designs, it is acceptable to continue to use the 100nF capacitor.

DP_COMPIO and ICOMPO signals
should be shorted near balls and routed with
- typical impedance < 25 mohms

DP & PEG Compensation



eDP Hot-plug (Disable)



CAD Note: Place PU resistor
within 2 inches of CPU

HPD PU/PD resistor values based
on CRB and different to DG

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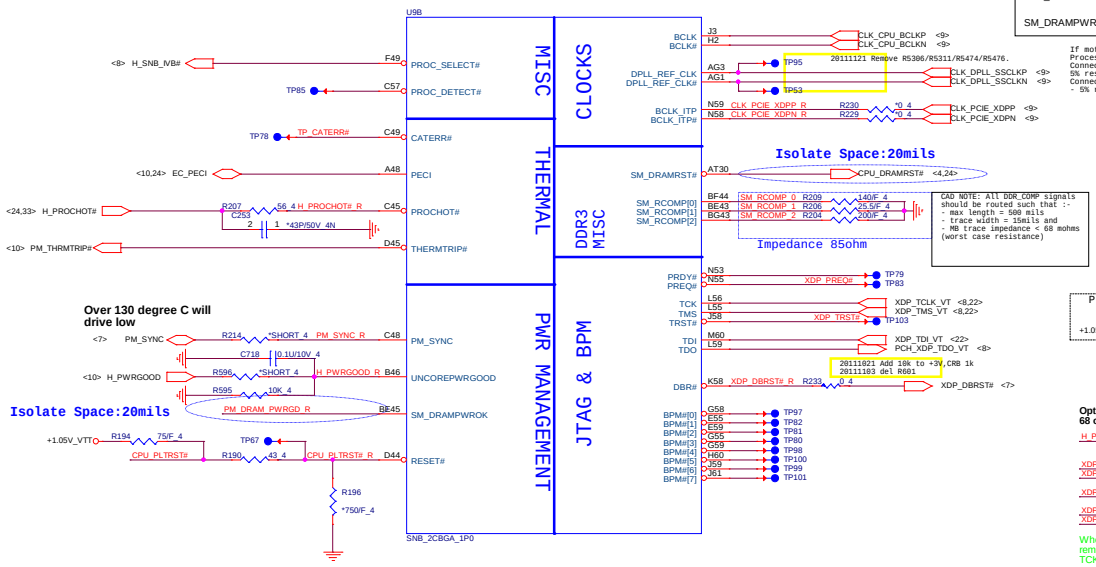
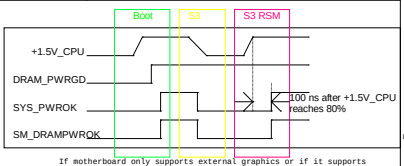
Ivy Bridge Processor (CLK,MISC,JTAG)





If motherboard only supports external graphics or if it supports Processor Graphics but without eDP:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/ - 5% resistor

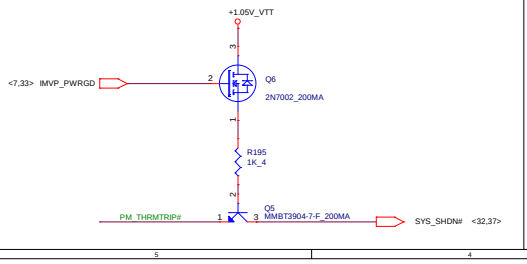
CAD NOTE: All DDR_COMP signals should be routed such that :-
- max length = 500 mils
- trace width = 15mils and
- MB trace impedance < 68 mohms
(worst case resistance)

Place near to XDP connector

Option for Prochot# function
68 ohm for unused, 62 ohm for used

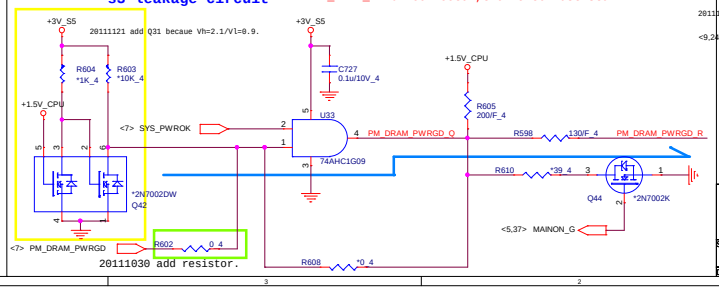
When MP, JTAG PU/PD resistor can be removed? (Yes Intel, TDI, TDO, TMS, TRST#, TCK,PREQ#, PRDY#)

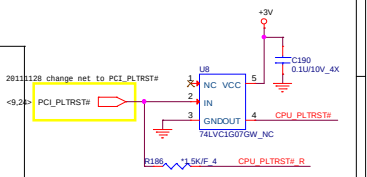
Thermal Trip <CPU>



s3 leakage circuit

If PM_DRAM_PWEGD connector,the R5180 must stuff.





IN	OUT
L	L
H	High-Z

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	Ivy Bridge 2/5	3A

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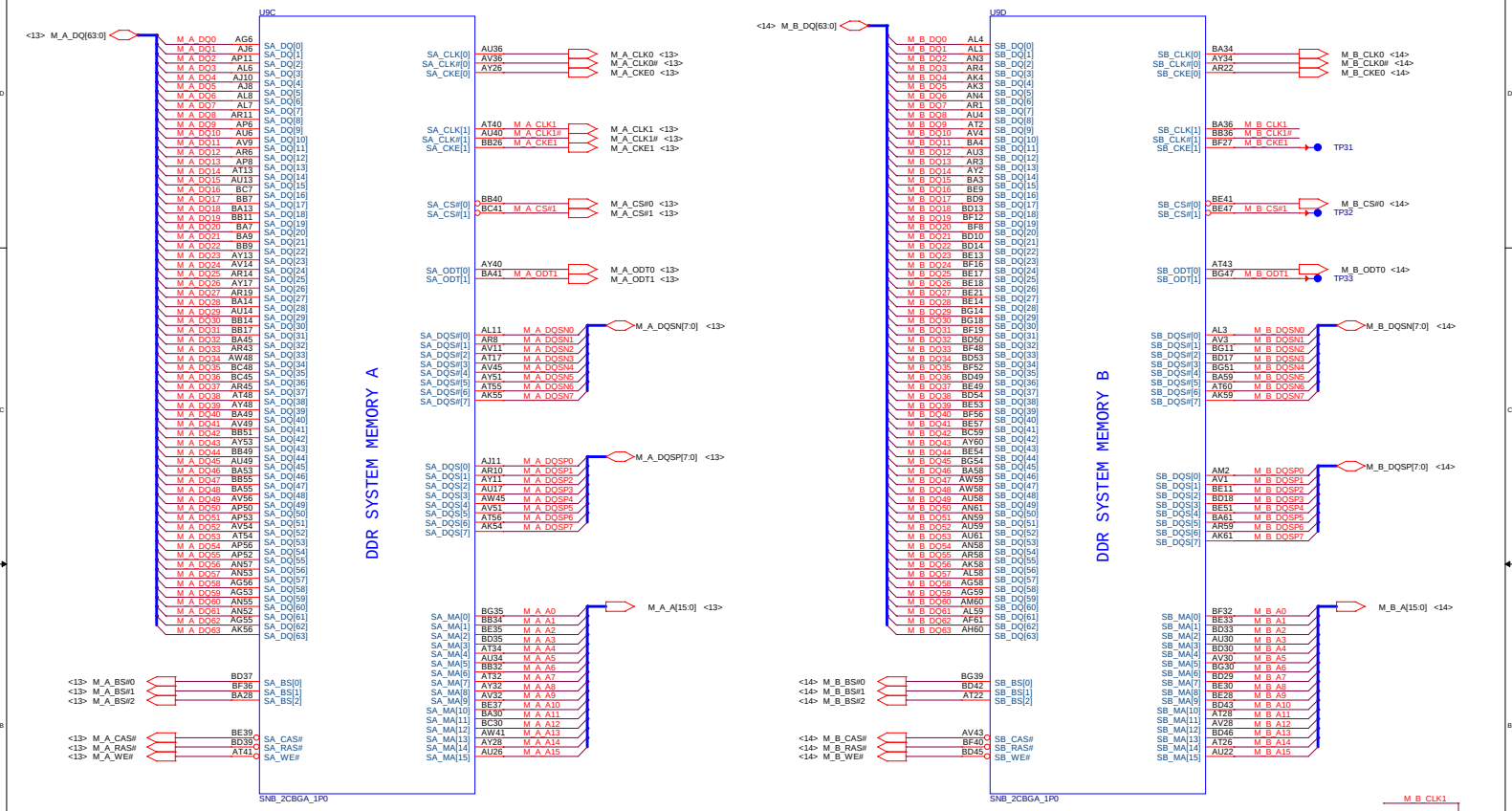
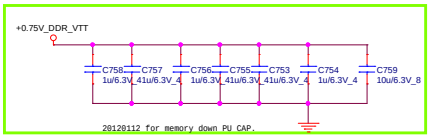
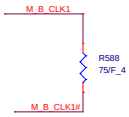
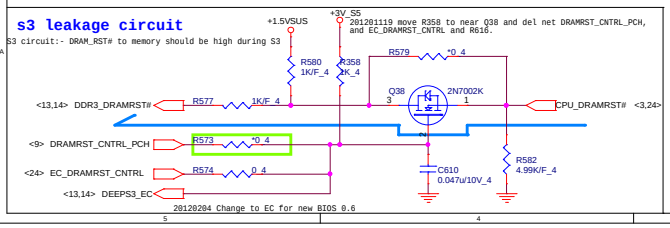
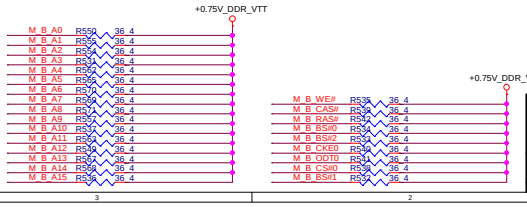
Sandy Bridge Processor (DDR3)











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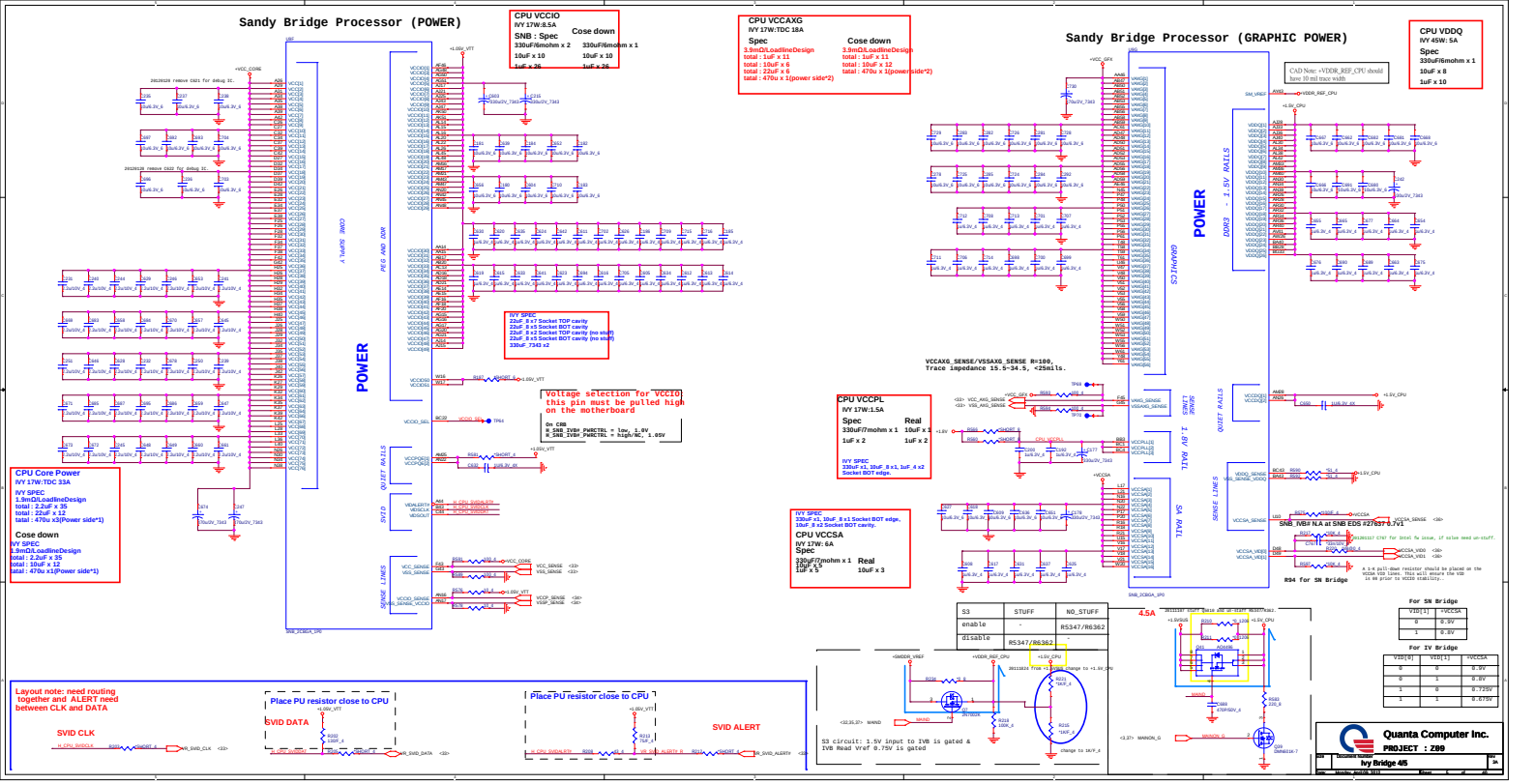
Sandy Bridge Processor (POWER)
Sandy Bridge Processor (GRAPHIC POWER)
CPU VCCIO
IVY 17W:8.5A
SNB : Spec
330uF/6mohm x 2
10uF x 10
1uF x 26
Cose down
330uF/6mohm x 1
10uF x 10
1uF x 26
CPU VCCAXG
IVY 17W:TDC 18A
Spec
3.9mDLoadlineDesign
total : 1uF x 11
total : 10uF x 6
total : 22uF x 6
total : 470u x 1(power side*2)
Cose down
3.9mDLoadlineDesign
total : 1uF x 11
total : 10uF x 12
total : 470u x 1(powerside*2)
CPU VDDQ
IVY 45W: 5A
Spec
330uF/6mohm x 1
10uF x 8
1uF x 10
CAD Note: +VDDR_REF_CPU should have 10 mil trace width
IVY SPEC
22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF_8 x2 Socket TOP cavity (no stuff)
22uF_8 x5 Socket BOT cavity (no stuff)
33uF_7343 x2
Voltage selection for VCCIO
this pin must be pulled high
on the motherboard
On CRB
H_SNB_IVB#_PWRCTRL = low, 1.0V
H_SNB_IVB#_PWRCTRL = high/NC, 1.05V
VCCAXG_SENSE/VSSAXG_SENSE R=100,
Trace impedance 15.5~34.5, <25mils.
CPU VCCPL
IVY 17W:1.5A
Spec
330uF/7mohm x 1
1uF x 2
Real
10uF x 1
1uF x 2
IVY SPEC
33uF x1, 10uF_8 x1, 1uF_4 x2
Socket BOT edge.
IVY SPEC
330uF x1, 10uF_8 x1 Socket BOT edge,
10uF_8 x2 Socket BOT cavity.
CPU VCCSA
IVY 17W: 6A
Spec
330uF/7mohm x 1
10uF x 5
Real
10uF x 3
SNB_IVB# N.A at SNB EDS #276370.7v1
R94 for SN Bridge
For SN Bridge
For IV Bridge
CPU Core Power
IVY 17W:TDC 33A
IVY SPEC
1.9mDLoadlineDesign
total : 2.2uF x 35
total : 10uF x 12
total : 470u x1(Power side*1)
Cose down
IVY SPEC
1.9mDLoadlineDesign
total : 2.2uF x 35
total : 10uF x 12
total : 470u x1(Power side*1)
Layout note: need routing
together and ALERT need
between CLK and DATA
SVID CLK
Place PU resistor close to CPU
SVID DATA
Place PU resistor close to CPU
SVID ALERT
S3 circuit: 1.5V input to IVB is gated &
IVB Read Vref 0.75V is gated
change to 1K/F_8
4.5A
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Ivy Bridge 4/5
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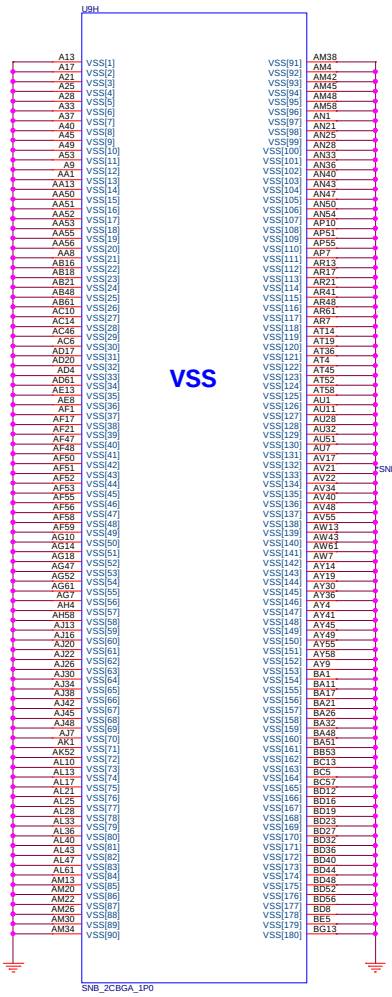
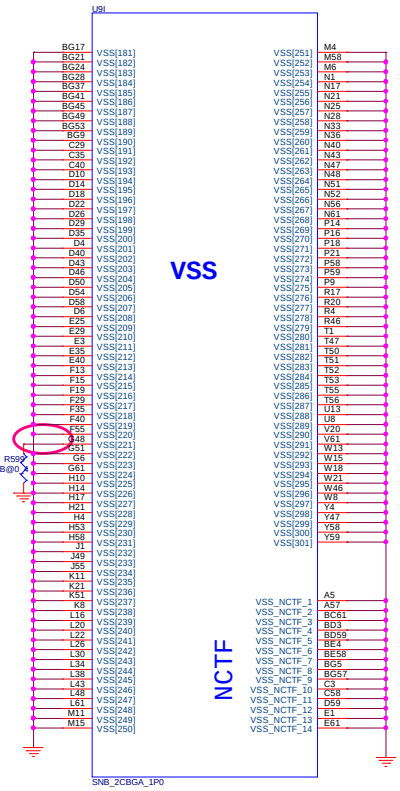
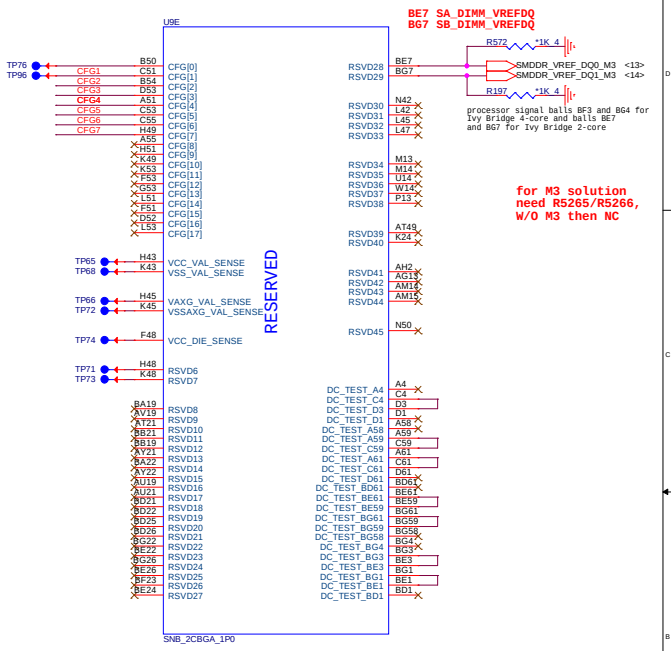
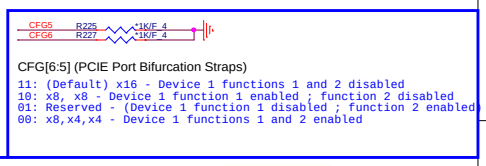
Sandy Bridge Processor (GND)





Sandy Bridge Processor (RESERVED, CFG)





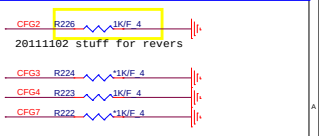
CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	**Lane Reversed**
CFG3 (PCI-E Static x4 Lane Reversal)	**Normal Operation**	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	**Enable; An ext DP device is connected to eDP**
CFG7 (PEG Defer Training)	**PEG train immediately following xxRESETB de assertion**	PEG wait for BIOS training



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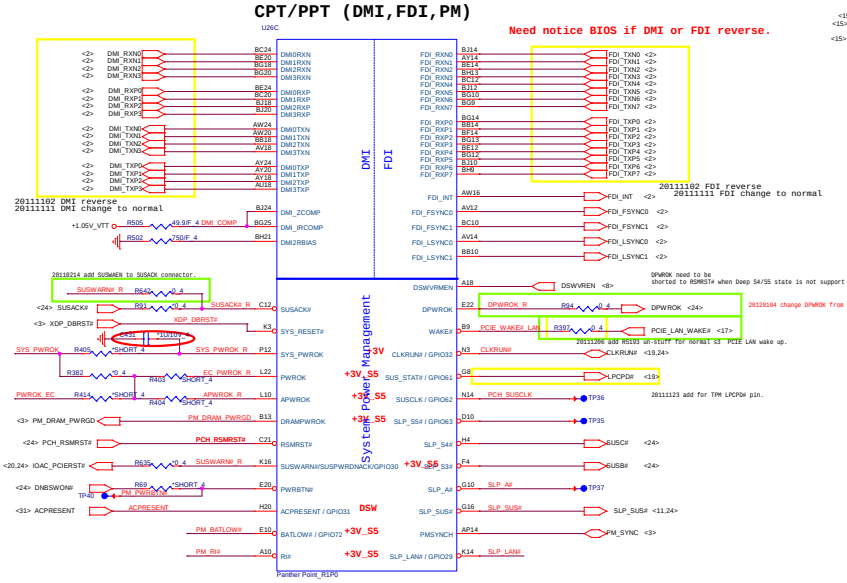
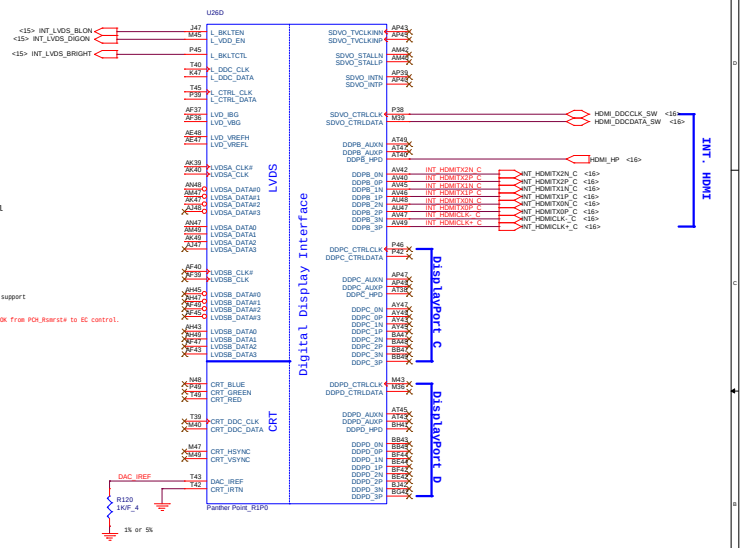
CPT/PPT (DMI,FDI,PM)

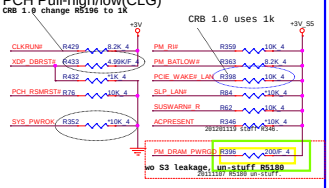
Need notice BIOS if DMI or FDI reverse.



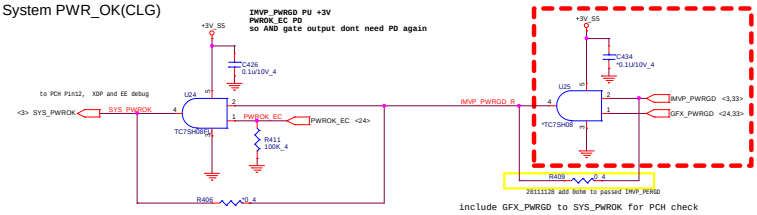
CPT/PPT (LVDS,DDI)



PCH Pull-high/low(CLG)



System PWR_OK(CLG)



include GFX_PWRGD to SYS_PWROK for PCH check

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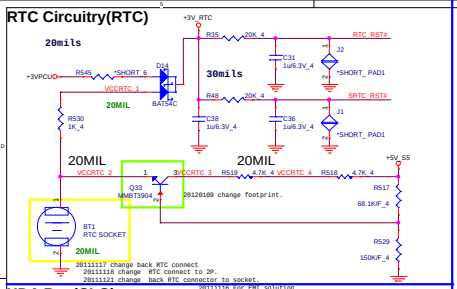
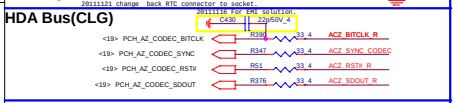
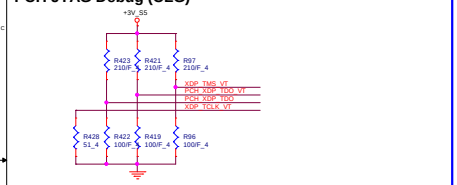
RTC Circuitry(RTC)



HDA Bus(CLG)



PCH JTAG Debug (CLG)

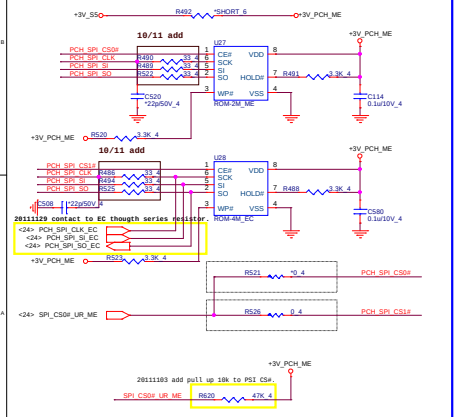


PCH Dual SPI (CLG)

(Default for WIN8)

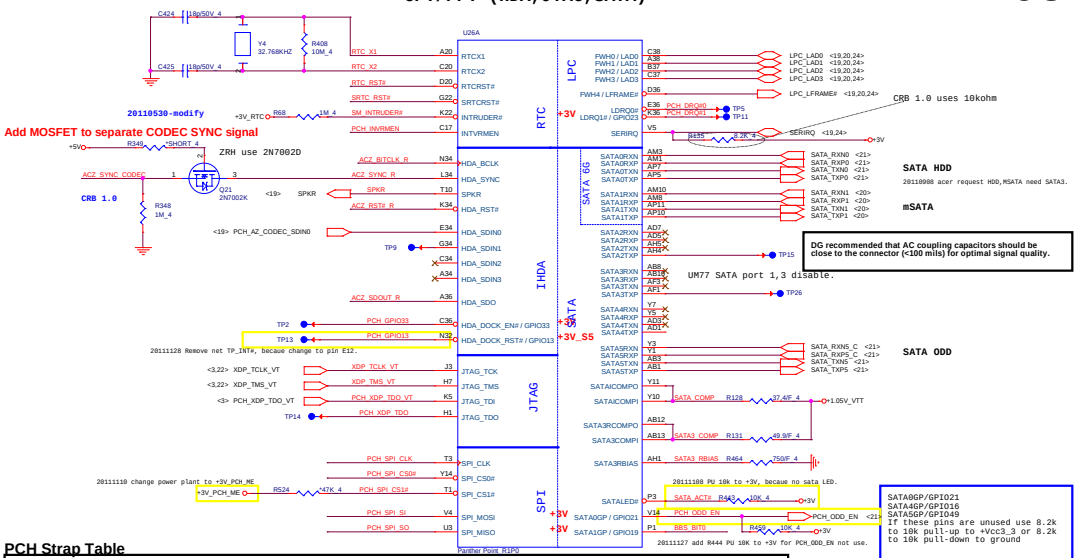
W25Q32BVSSIG / AKE391P0N00----->4MB

W25Q16BVSSIG / AKE38FP0N01----->2MB



PCH2(CLG)

CPT/PPT (HDA,JTAG,SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R460 *1K_4 SPKR
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R418 *1K_4 PCI_GNT3# <9> — Used as GPIO only. at chklist 1.2
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R391 330K_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location 1 / 1 / SPI * 0 / 0 / LPC	R412 *1K_4 BBS_BIT1 <9> — Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		R448 *1K_4 BBS_BIT0
HDA_SDO	Flash Descriptor Security	RSMRST	0 = effect (default)(weak pull-down 20K) 1 = overridden	<24> ME_WR# R372 *SHORT_4 ACZ_SDOUT_R — ME_WR default EC setting folating
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss (weak pull-down 20K) 1 = Set to Vcc	R482 2.2K_4 +1.8V; R483 1K_4 DF_TVS <10> H_SNB_VBS# <3> — for future CPU, Sandy Bridge NC DF_TVS needs to be pulled up to VccDFTERM power rail through 2.2 kOhm ±5% - RB361 change to 0 or not??
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)	R439 *1K_4 PLL_ODVR_EN <10>
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 R350 1K_4 ACZ_SYNC_R — Needs to be pulled High for Huron River platform. chklist 1.2
GPIO15	Intel ME Crypto Transport Layer Security (TLS) cipher suite internal PD	RSMRST	0 = Disable (Default) 1 = Enable	+3V_S5 R413 1K_4 PCH_GPIO15 <10>
DSWVREN	DEEP S4/S5 well On Die DSW VR Enable	DSW	High = Enable (Default) Low = Disable	+3V_RTC R60 330K_4 R59 *330K_4 DSWVREN <7>
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R479 *1K_4 NV_ALE <9>

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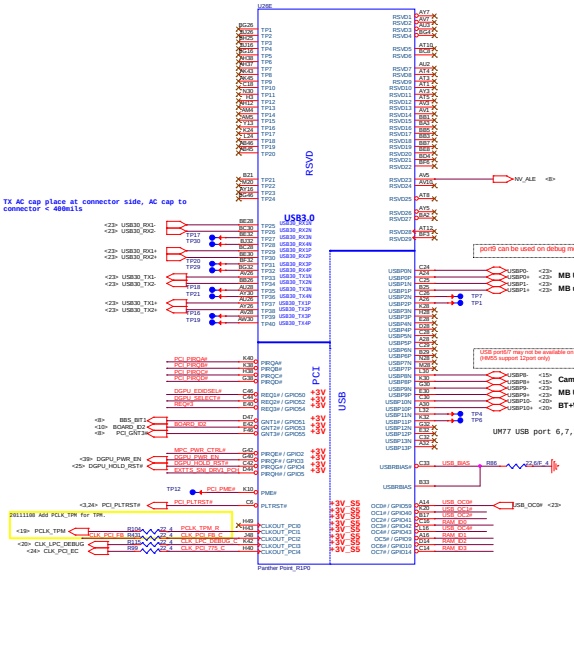
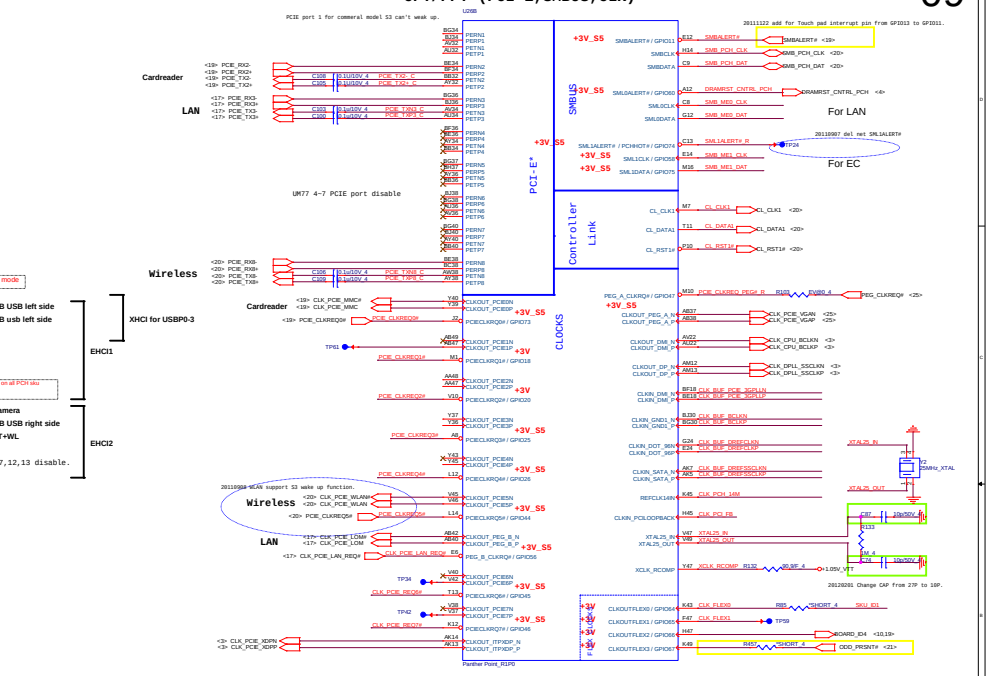
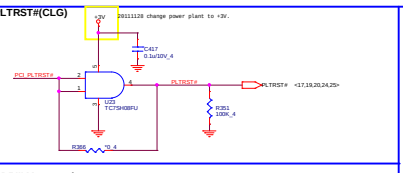
CPT/PPT (PCI,USB,NVRAM)



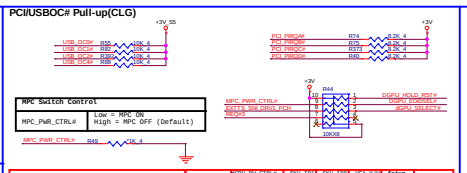
CPT/PPT (PCI-E,SMBUS,CLK)



PLTRST#(CLG)

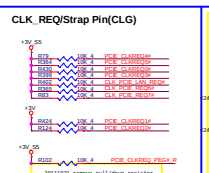


PCI/USBOC# Pull-up(CLG)

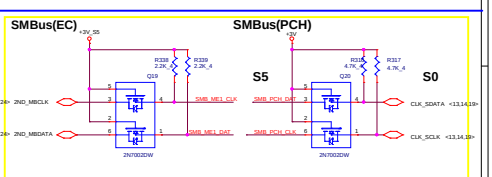


MPC Switch Control	
MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

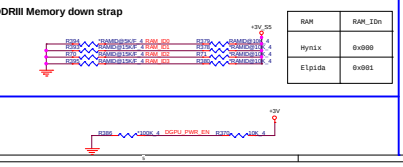
CLK_REQ/Strap Pin(CLG)



SMBus(EC) / SMBus(PCH)

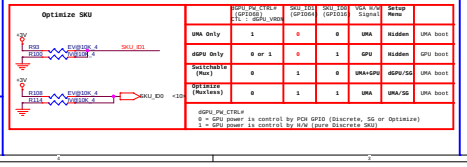


DDRIII Memory down strap



RAM	RAM_IDn
Hynix	0x000
Elpida	0x001

Optimize SKU



	dGPU_PW_CTRL# (GPIO68) Pin : dGPU_VROM	SKU_ID1 (GPIO64)	SKU_ID0 (GPIO10)	VGA H/W Signal	Setup Menu	
UMA Only	1	0	0	UMA	Hidden	UMA boot
dGPU Only	0 or 1	0	1	GPU	Hidden	GPU boot
Switchable (Mux)	0	1	0	UMA+GPU	dGPU/SG	UMA boot
Optimize (Muxless)	0	1	1	UMA	UMA/SG	UMA boot

dGPU_PW_CTRL#
0 = GPU power is control by PCH GPIO (Discrete, SG or Optimize)
1 = GPU power is control by H/W (pure Discrete SKU)

if net DRAMRST_CNTRL_PCH change to PCH control need stuff R358.

Quanta Computer Inc.

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Panther Point 3/6

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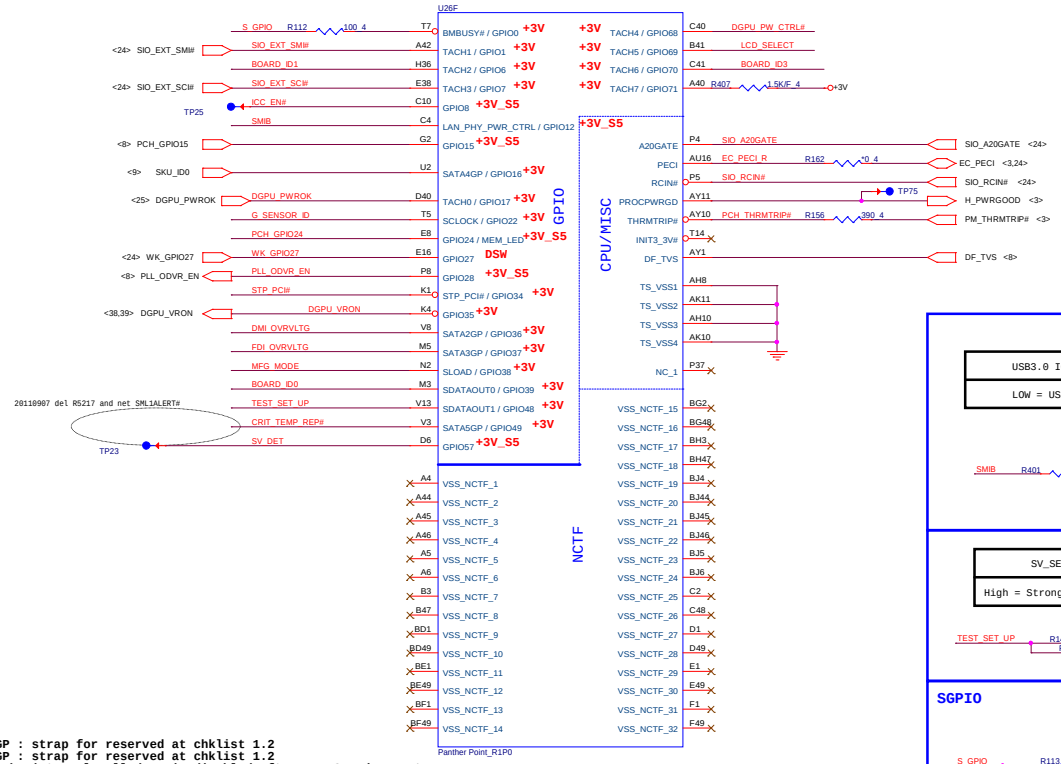
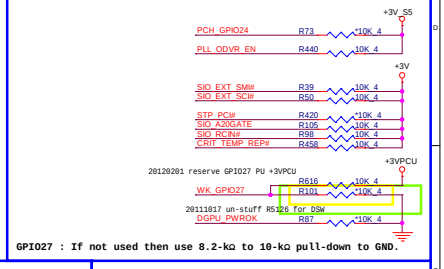
CPT/PPT (GPIO,VSS_NCTF,RSVD)



SATA2GP : strap for reserved at chklist 1.2
SATA3GP : strap for reserved at chklist 1.2
NOTE: The internal pull-down is disabled after PLTRST# deasserts.
NOTE: This signal should not be pulled high when strap is sampled.

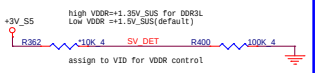
GPIO Pull-up/Pull-down(CLG)



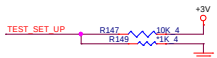
GPIO27 : If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

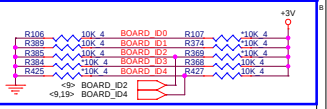
USB3.0 IC CTL
LOW = USB3.0 IC

DMI TERMINATION VOLTAGE OVERRIDE	LOW = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)



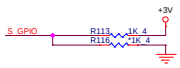
SV_SET_UP
High = Strong (Default)



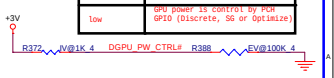


Board_ID4 Hight=Symatic, LOW=ELAN.

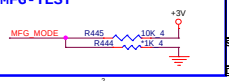
SGPIO

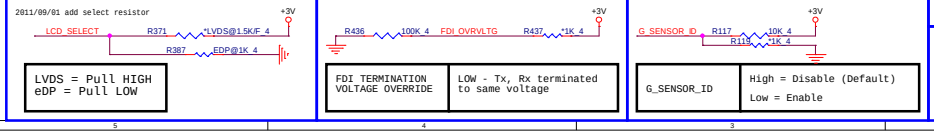


high	GPU power is control by H/W (pure Discrete SKU)
low	GPU power is control by PCH GPIO (Discrete, SG or Optimize)



MFG-TEST





Quanta Computer Inc.

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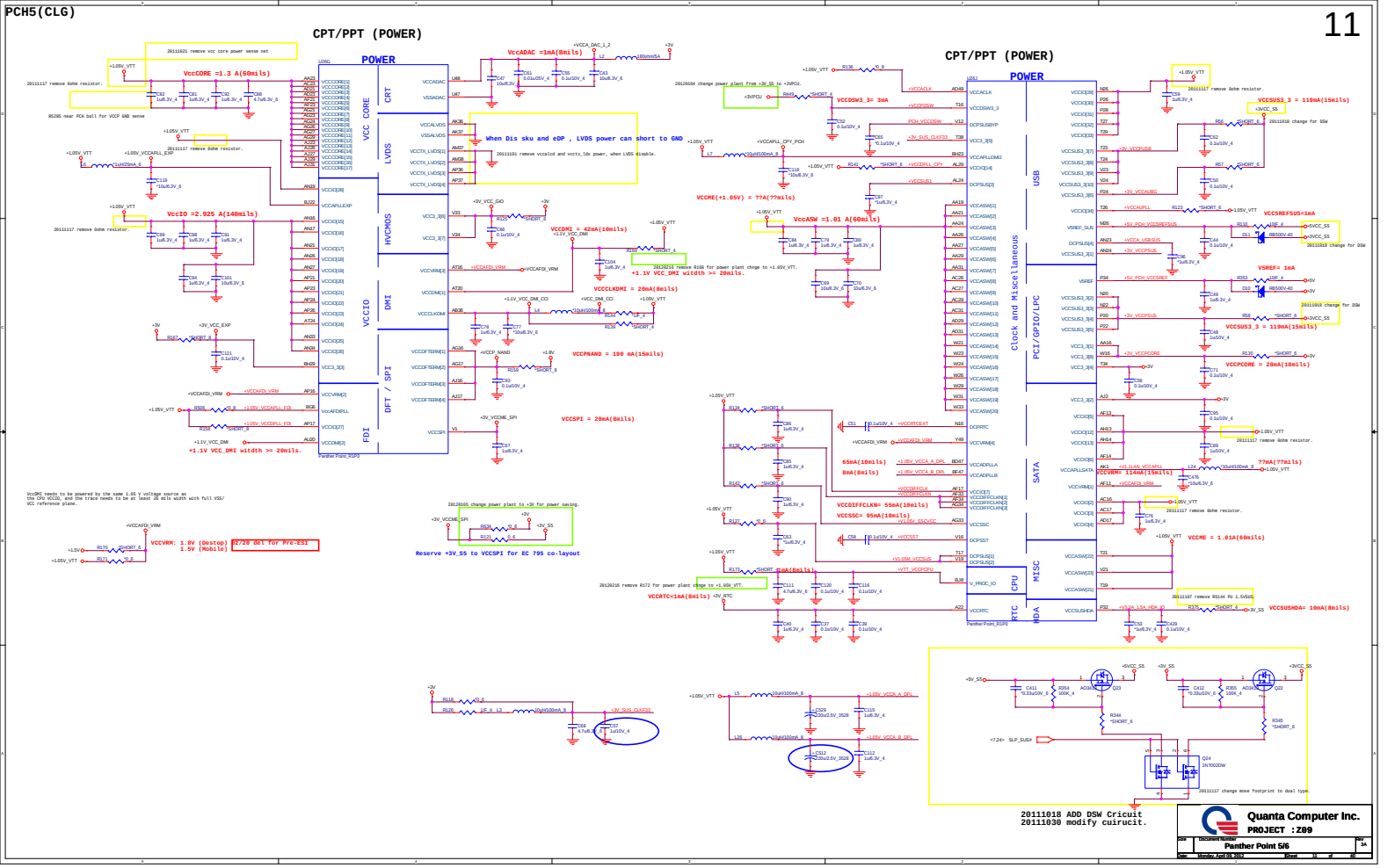
CPT/PPT (POWER)
POWER
VccCORE =1.3 A(60mils)
VccIO =2.925 A(140mils)
VCC CORE
LVDS
HVCMOS
DMI
DFT / SPI
FDI
VCCIO
CRT
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA
When Dis sku and eDP , LVDS power can short to GND
VccADAC =1mA(8mils)
VCCDSW3_3= 3mA
VccASW =1.01 A(60mils)
VCCME(+1.05V) = ??A(??mils)
VCCDMI = 42mA(10mils)
VCCCLKDMI = 20mA(8mils)
VCCPNAND = 190 mA(15mils)
VCCSPI = 20mA(8mils)
VCCDIFFCLKN= 55mA(10mils)
VCCSSC= 95mA(10mils)
VCCRTC<1mA(8mils)
VCCSUS3_3 = 119mA(15mils)
VCCSUS3_3 = 119mA(15mils)
VCCPCORE = 28mA(10mils)
VCCME = 1.01A(60mils)
VCCSUSHDA= 10mA(8mils)
VCCVRM: 1.8V (Desktop)
1.5V (Mobile)
Reserve +3V_SS to VCCSPI for EC 795 co-layout
20111018 ADD DSW Cricuit
20111030 modify cuirucit.
Quanta Computer Inc.
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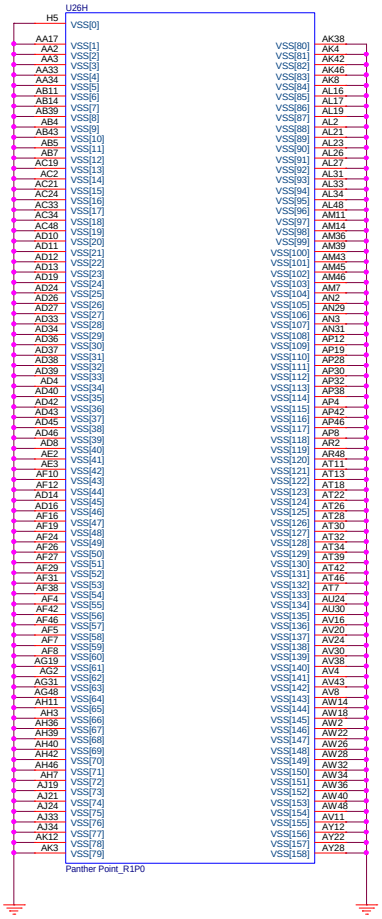
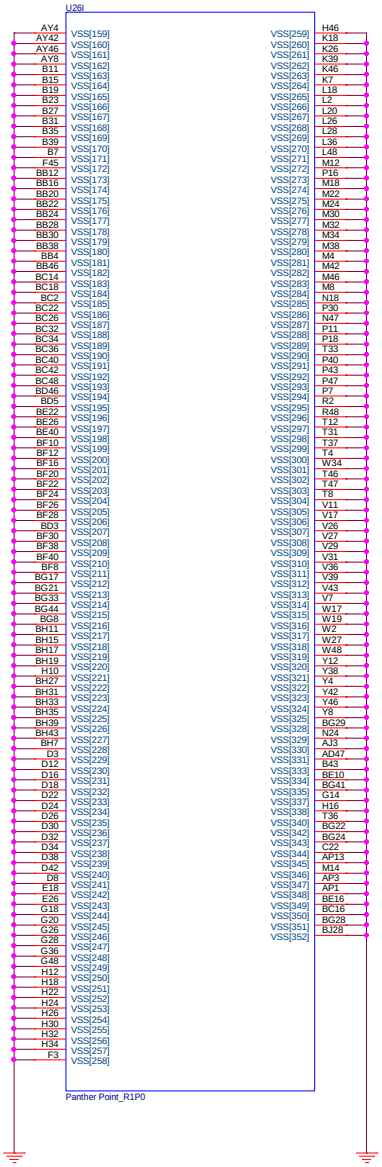
IBEX PEAK-M (GND)





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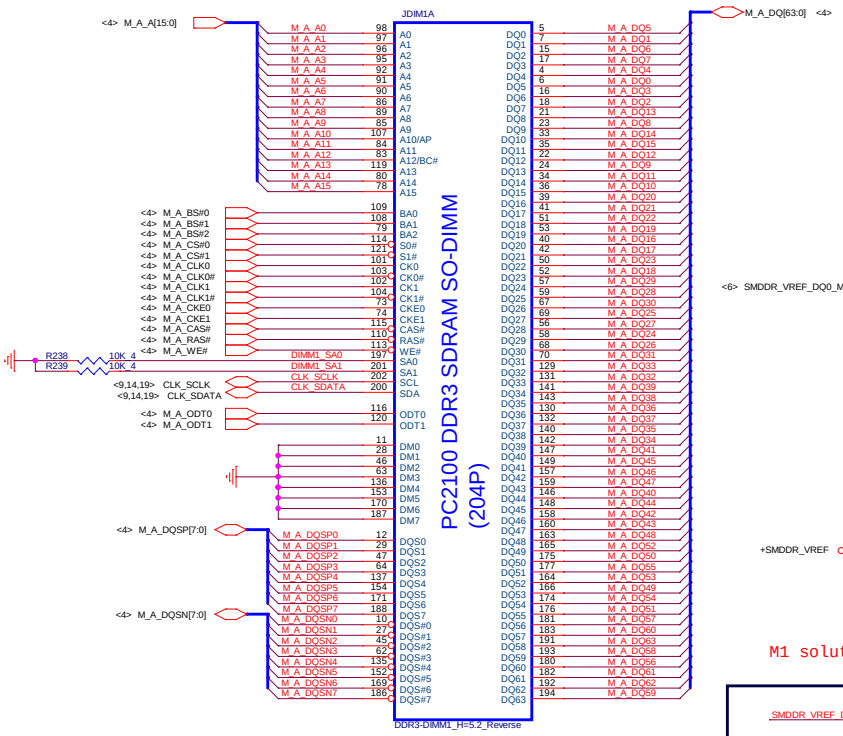
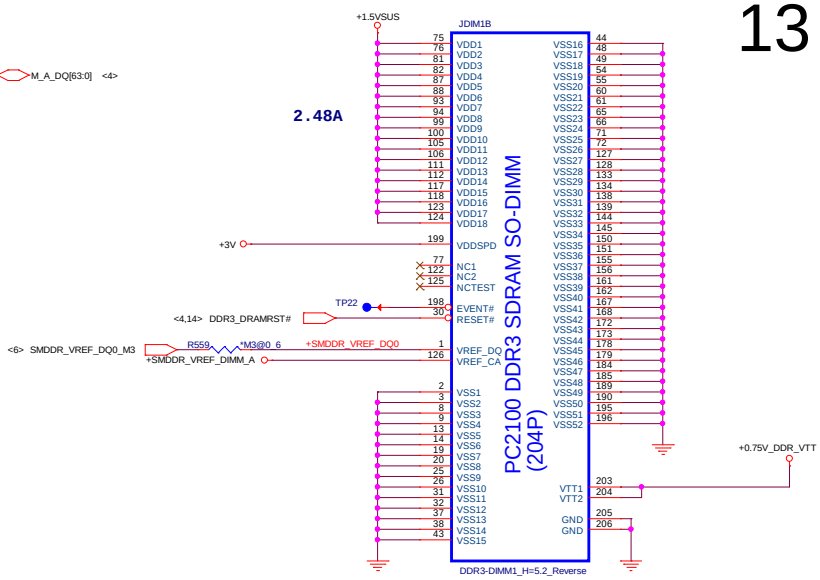
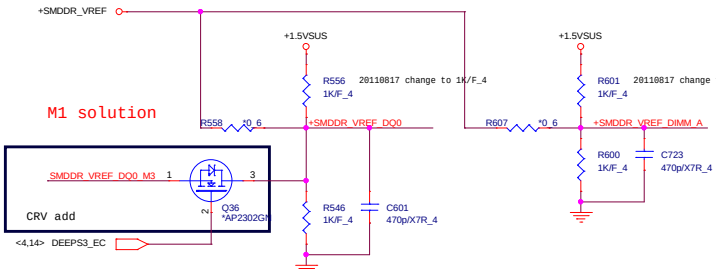
DDR3 DIMM-A

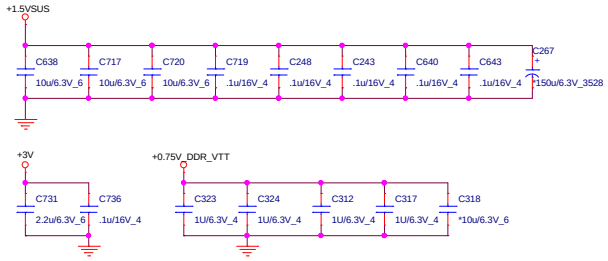




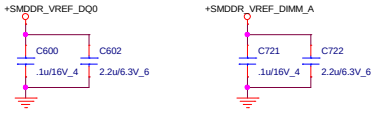


M1 solution

Place these Caps near So-Dimm0.



	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1



Quanta Computer Inc.

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Size	Document Number	Rev
	DDRIII SO-DIMM-0	3A

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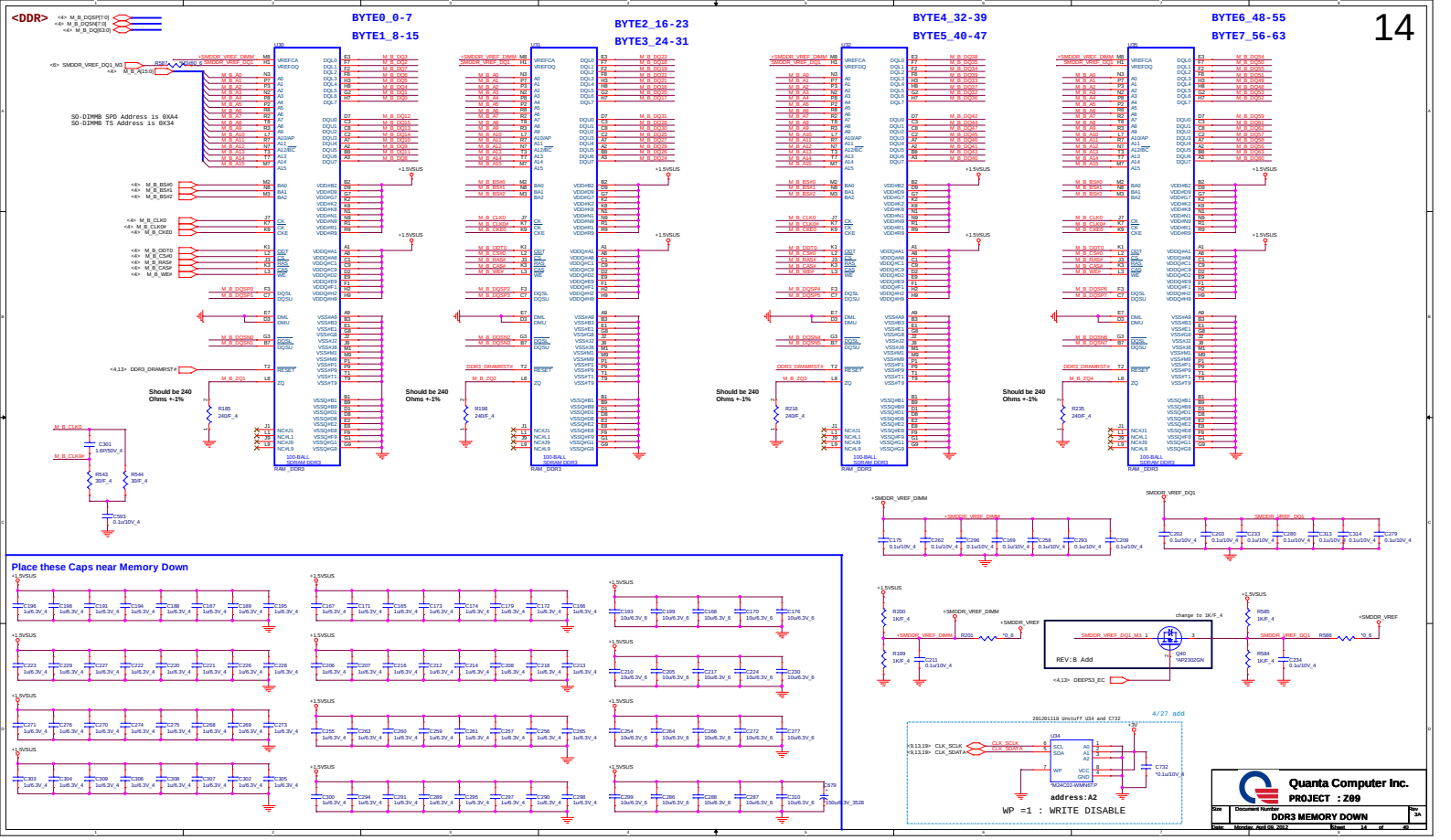

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Size	Document Number	Rev
	DDR3 MEMORY DOWN	3A

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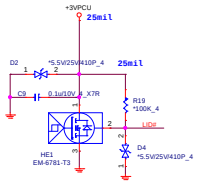
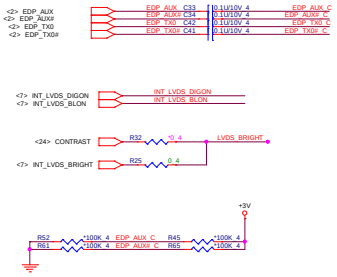
Lid Switch (Hall sensor)



PT3661-BB : AL003661003

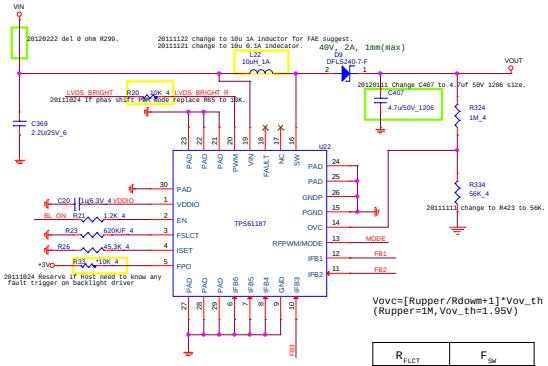
eDP

7/28 modify



LED Driver-IC

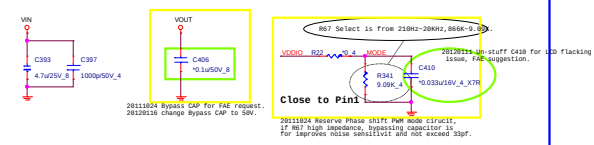
Penal SPEC:
Iout:78~79.5mA
Vout:32~34V



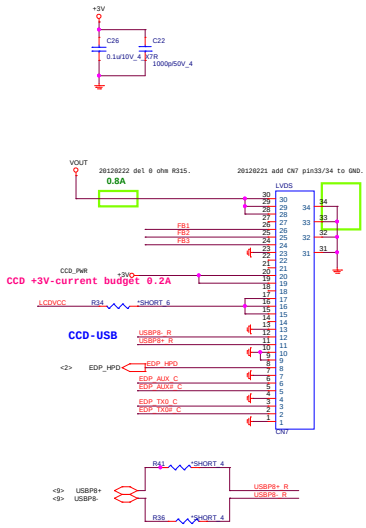
20111013 Create LED D-IC

Vovc=[Rupper/Rdown+1]*Vov_th
(Rupper=1M,Vov_th=1.95V)

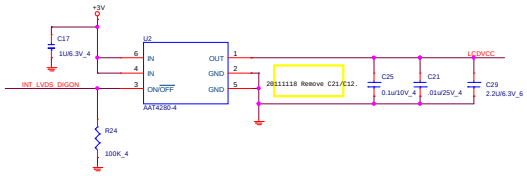
R_{FLCT}	F_{SW}
833K	600KHz
625K	800KHz
499K	1MHz



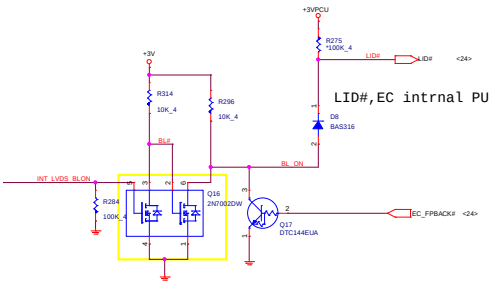
LCD CONNECTOR



LCD Power



Backlight Control



20111117 change mose footprint to dual type.

Quanta Computer Inc.
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	LVDS/CAMERA/LID	3A

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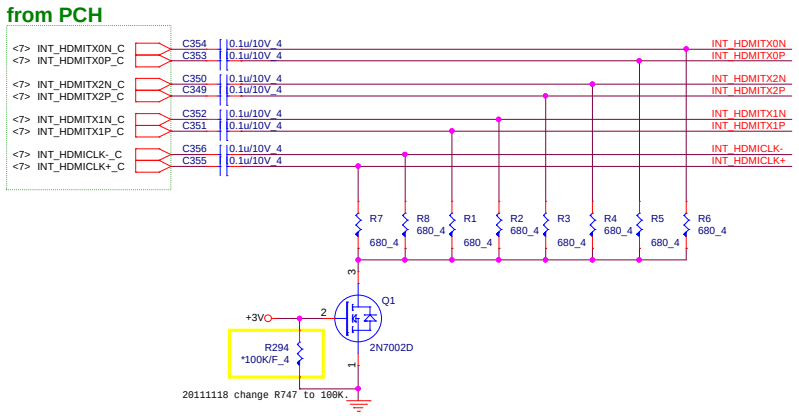
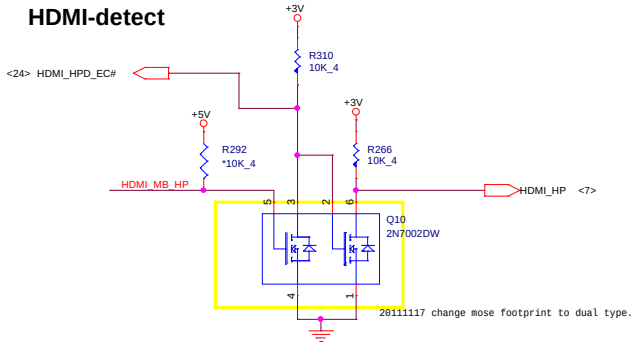
HDMI

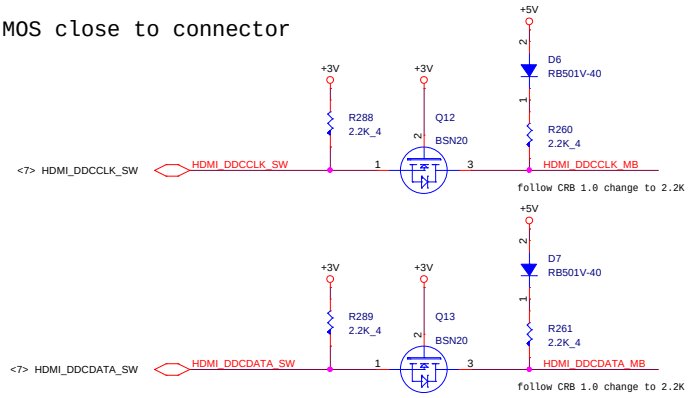


HDMI-detect

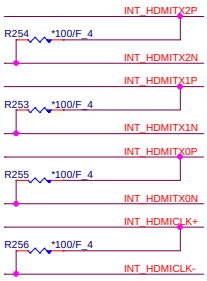


I2C

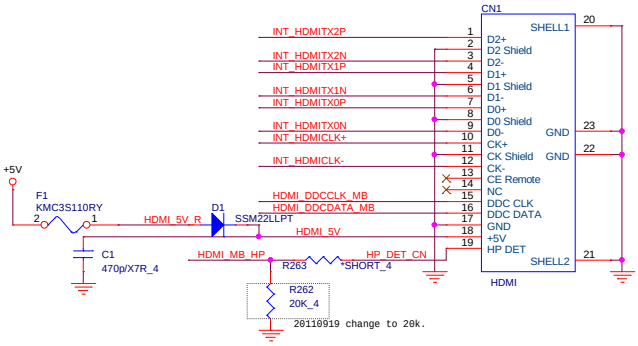
MOS close to connector



EMI



HDMI connector



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	HDMI (PS8101)	3A
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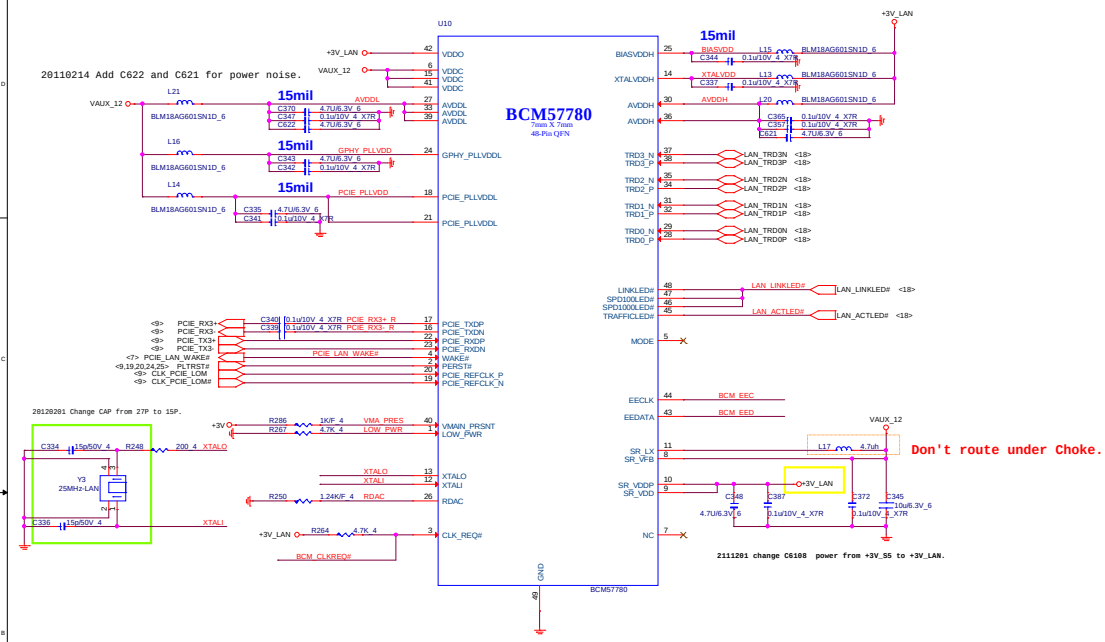
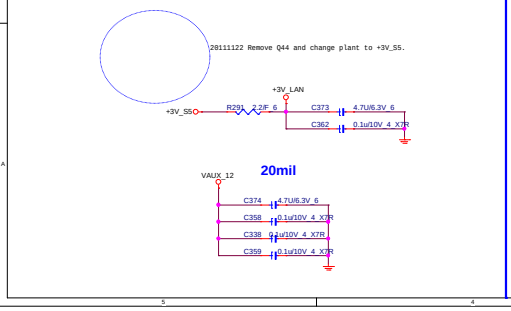
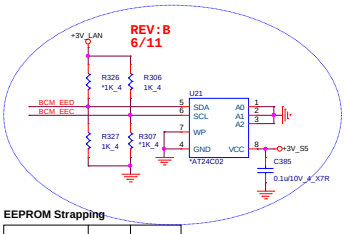
Giga-LAN BCM57780



LAN POWER

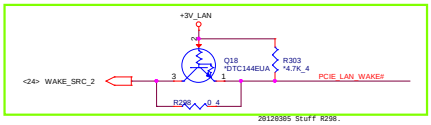


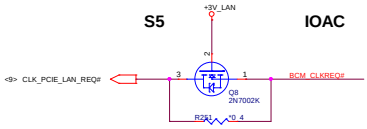
EEPROM



EEPROM Strapping

EEPROM Type	EECLK	EEDATA
24LC02	1	1
Internal	1	0





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	GLAN BCM57780	3A

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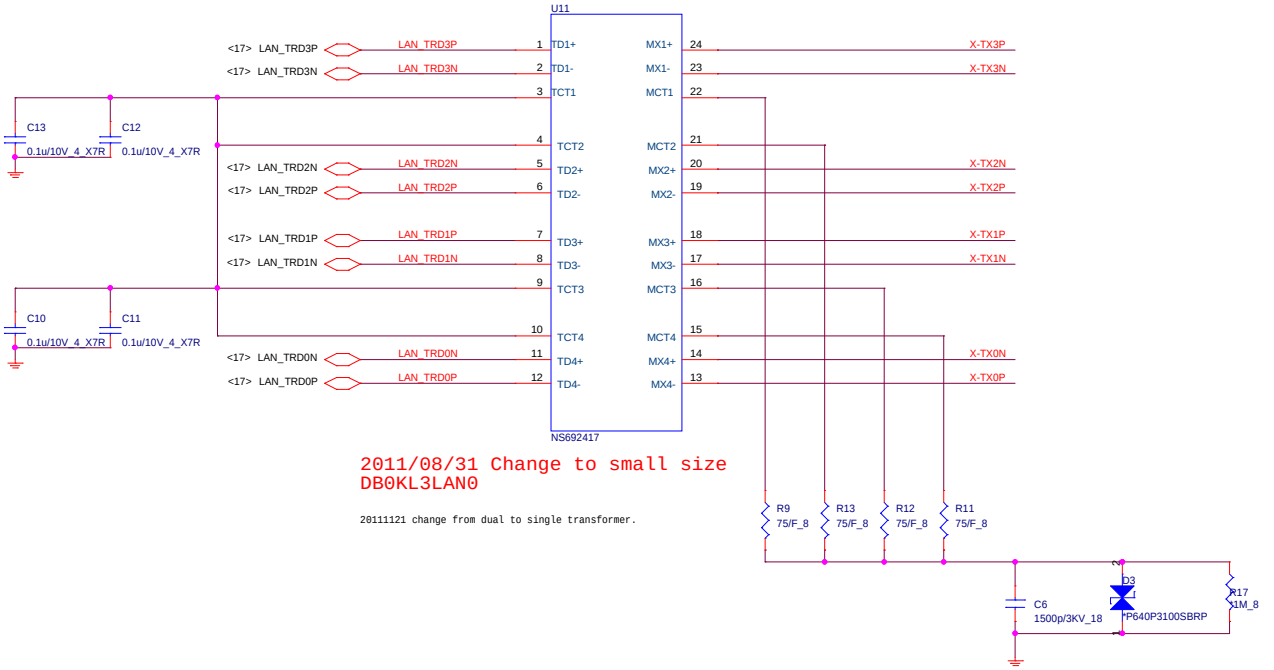
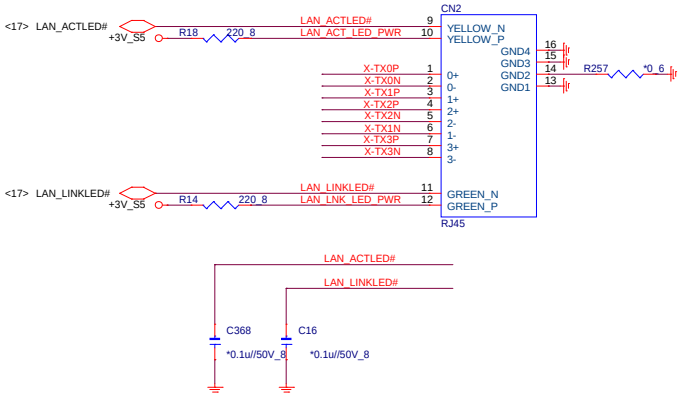
TRANSFORMER

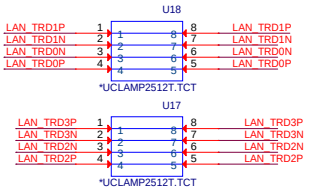


2011/08/31 Change to small size
DB0KL3LAN0

20111121 change from dual to single transformer.



For EMI



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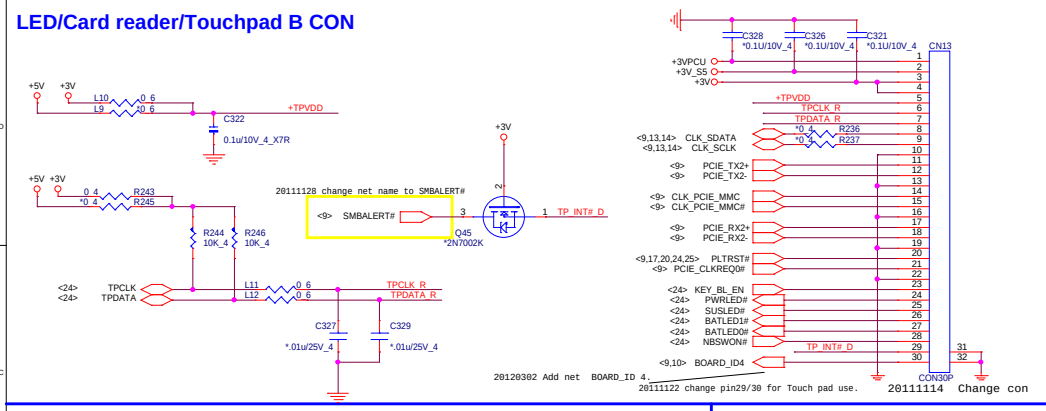
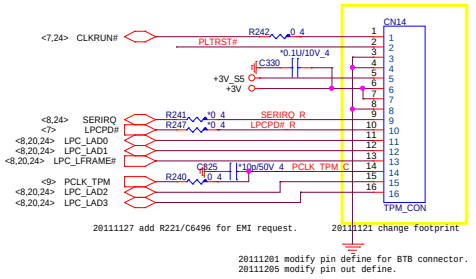
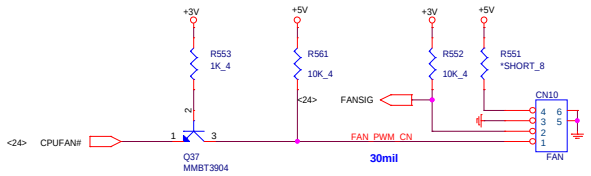
LED/Card reader/Touchpad B CON



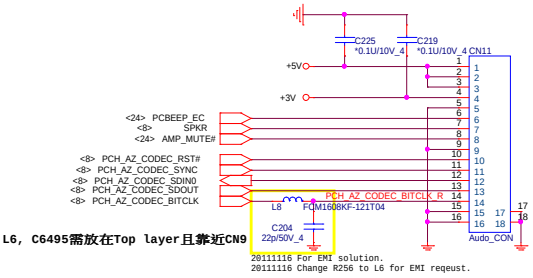
TPM



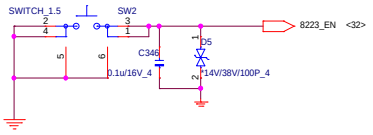
CPU FAN



Audio Connector



3/5VPCU reset switch



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	mSATA/CR/LED	3A

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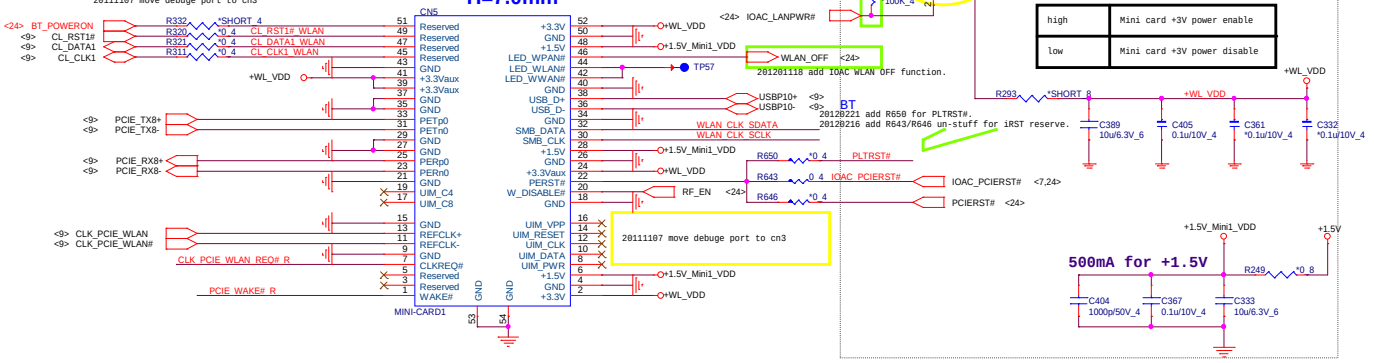
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

Check LED signal. (active high or low)

H=7.0mm

20111207 change Pin51 net name to BT_POWERON
20111107 move debuge port to cn3

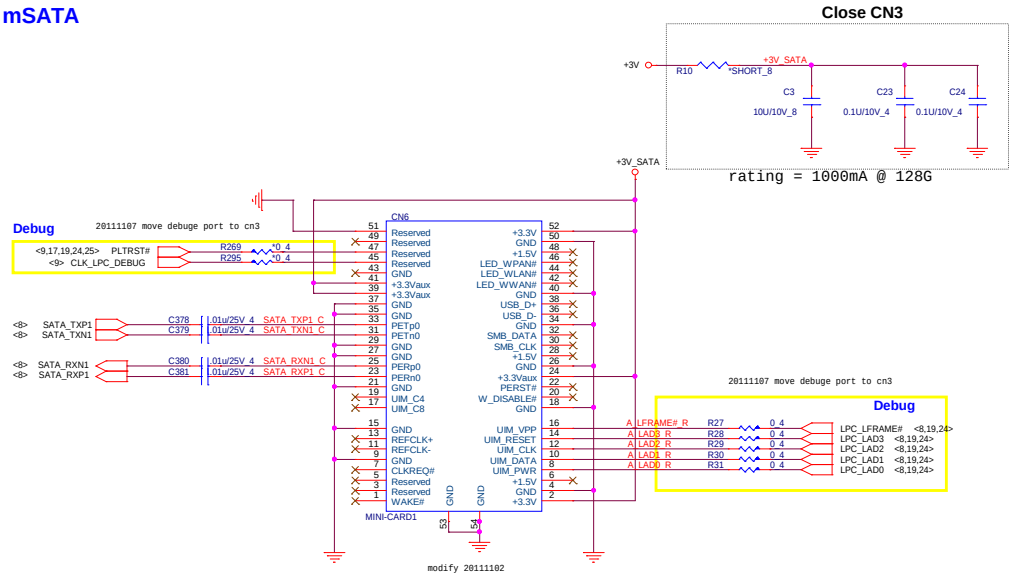


Close CN13

2011017 : stuff q21 to enable wake function on WLAN for IOAC
check IOAC power rail can reduce Q21

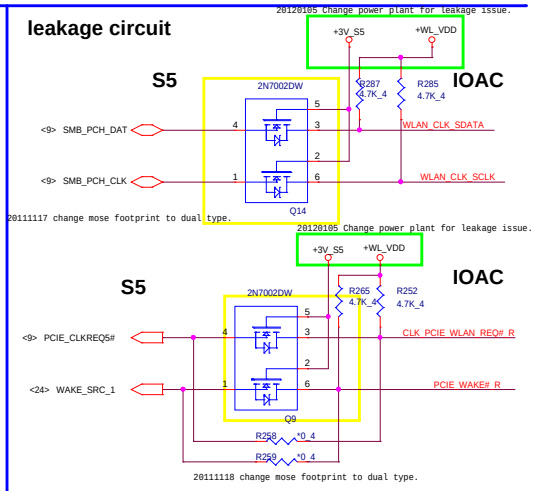
mSATA

Close CN3



leakage circuit

20120105 Change power plant for leakage issue.



Quanta Computer Inc.

PROJECT : Z09

Size	Document Number	Rev
	MINI PCI-E card/TV	3A

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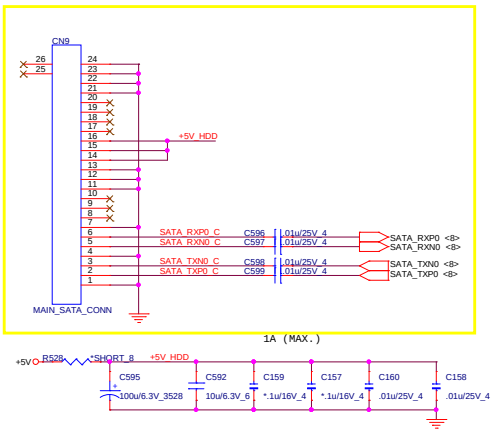
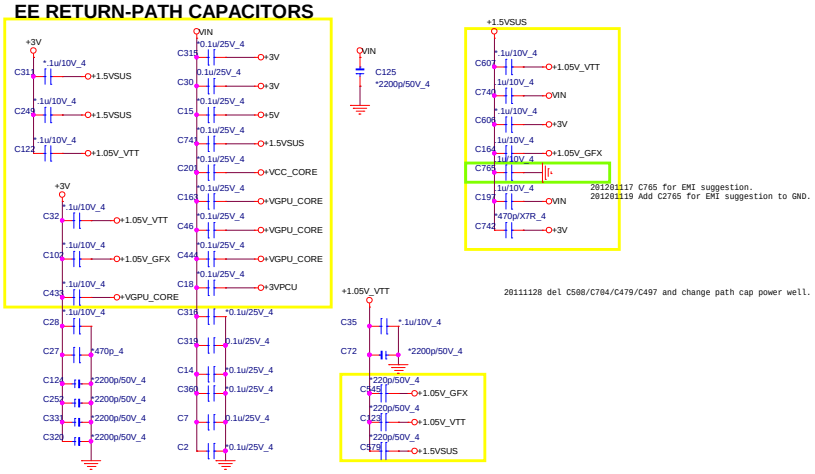
MAIN SATA HDD RE-DRIVER

MAIN SATA HDD

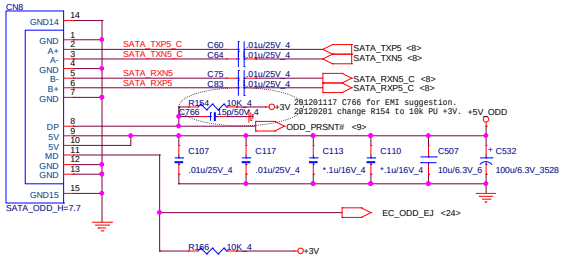
21111207 change Cn12 Pin define following ZHA.



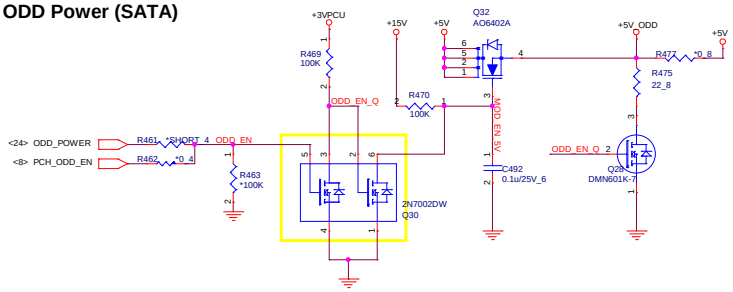
EE RETURN-PATH CAPACITORS



ODD (SATA)



ODD Power (SATA)



Quanta Computer Inc.

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Size	Document Number	Rev
	SATA-HDD/ODD/USB-ESATA	3A

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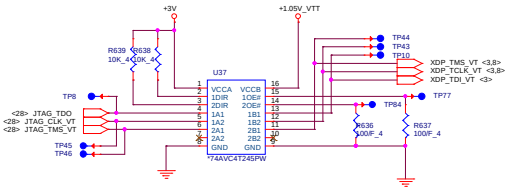
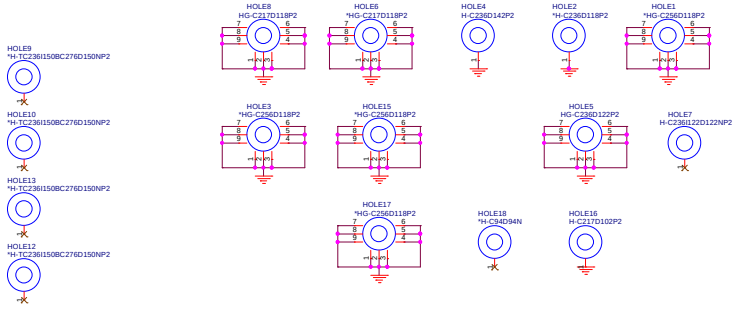
K/B

20111125 modify pin define

ICT TEST FIXTURE(VOLTAGE TRANSLATOR)



SCREW HOLE



BATT Enable short pad

20111208 Change Hole8 to BATT short pad.

Quanta Computer Inc.		
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Size	Document Number: XDP/ Hole	Rev 3A
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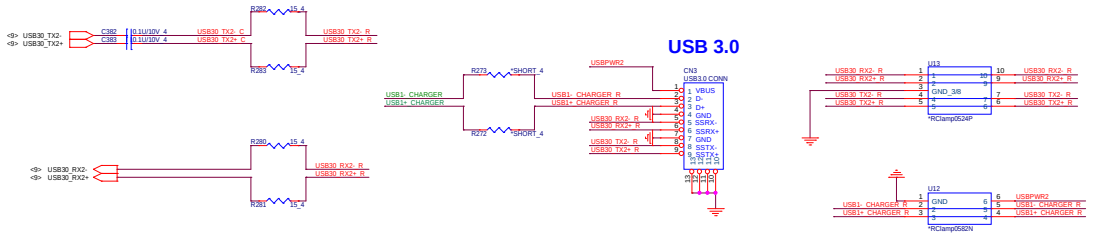
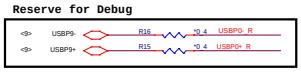
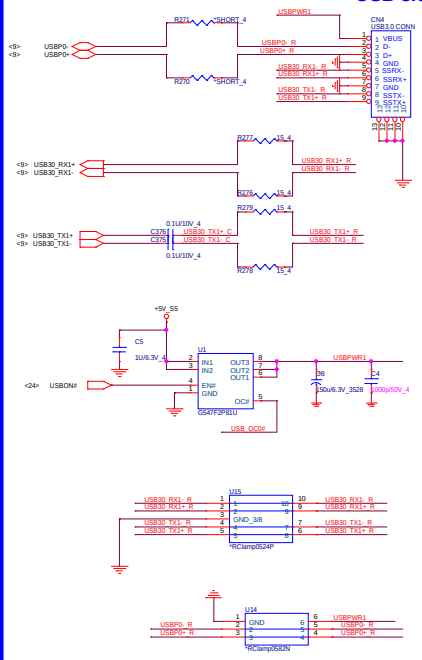
USB3.0 CONN



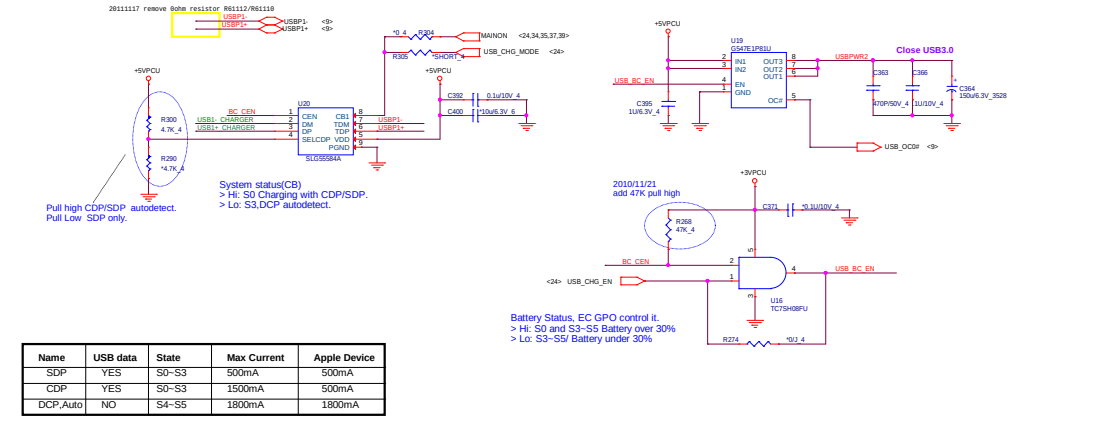
Reserve for Debug



USB 3.0



USB charger



Name	USB data	State	Max Current	Apple Device
SDP	YES	S0~S3	500mA	500mA
CDP	YES	S0~S3	1500mA	500mA
DCP,Auto	NO	S4~S5	1800mA	1800mA

Quanta Computer Inc.

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	USB 3.0	3A

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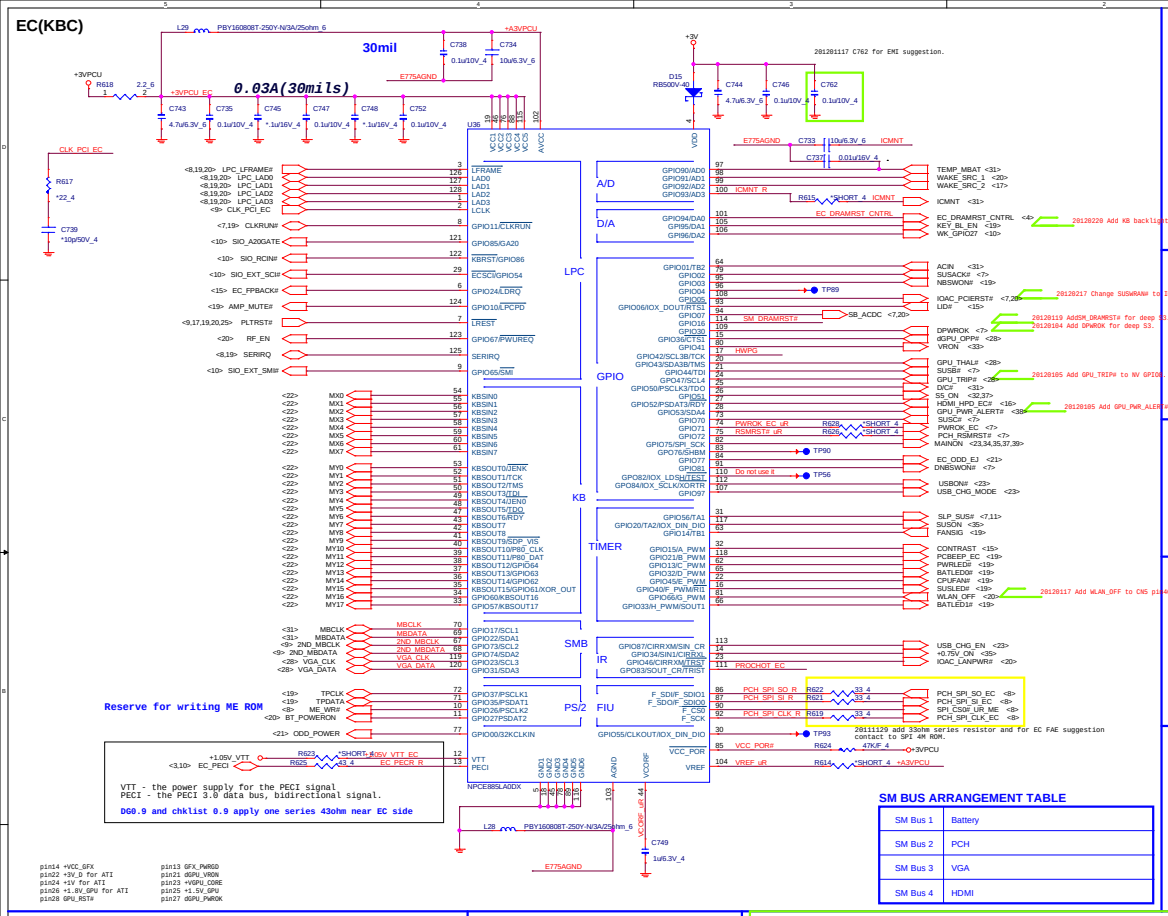
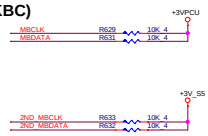
EC(KBC)

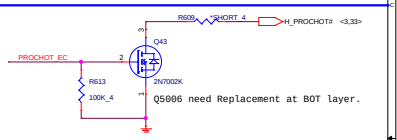


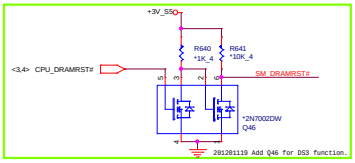
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	VGA
SM Bus 4	HDMI

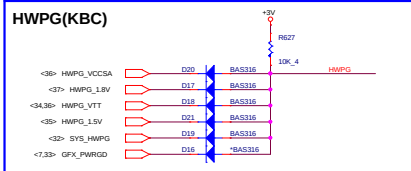
SM BUS PU(KBC)



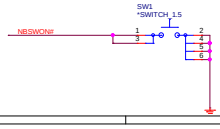




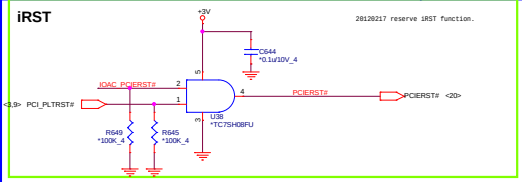
HWPG(KBC)



RSVD for power on



iRST



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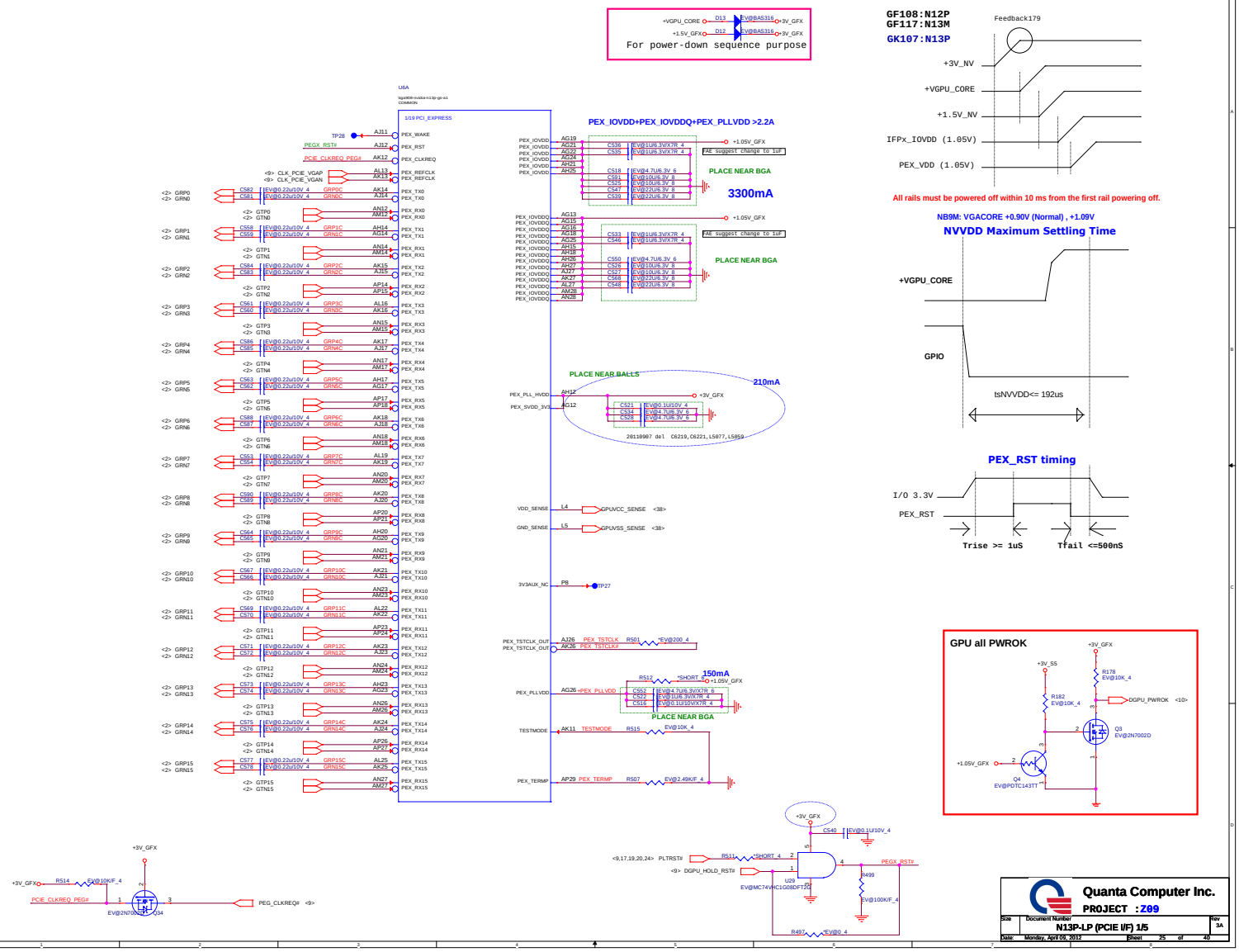


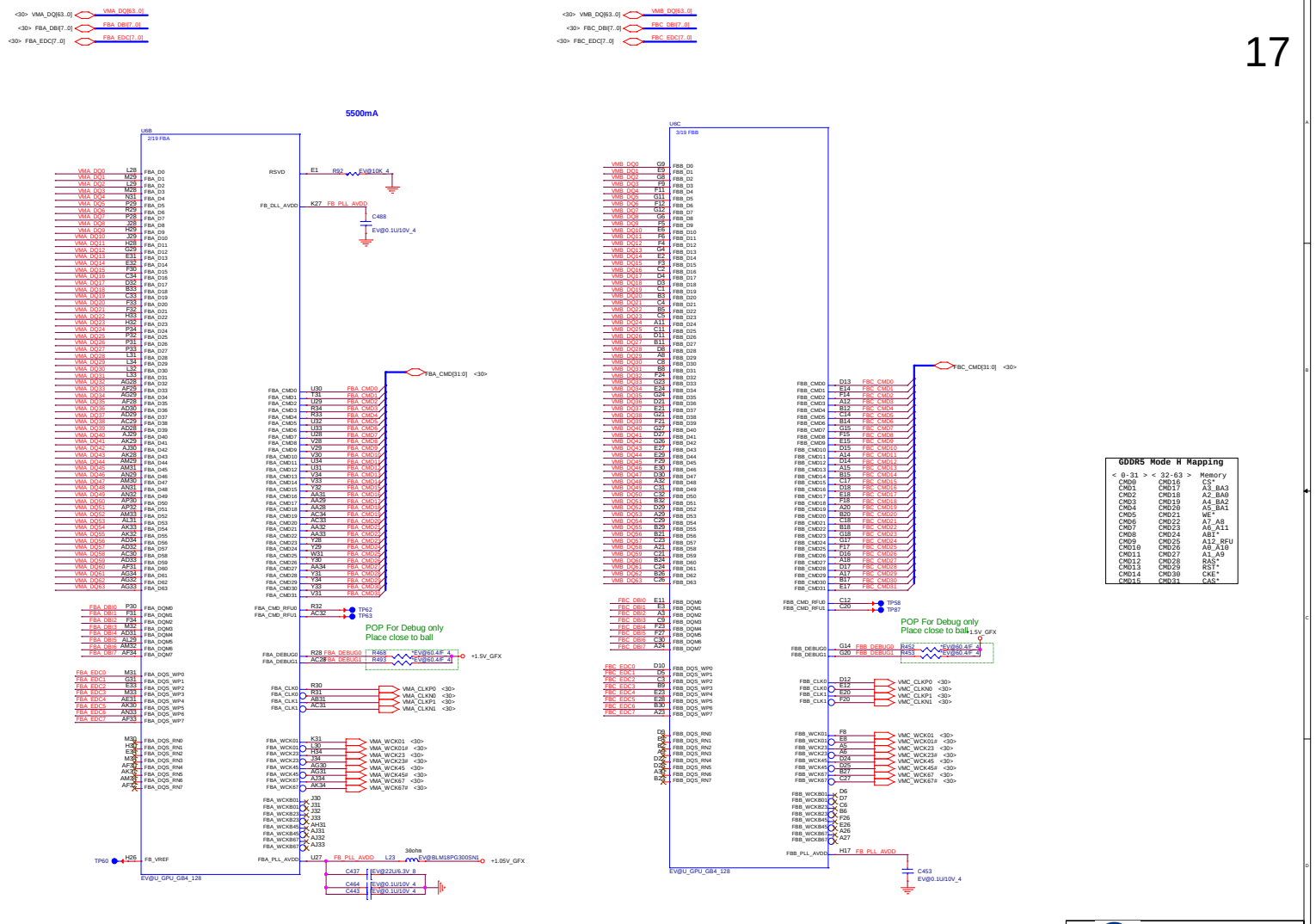
GF108:N12P
GF117:N13M
GK107:N13P

All rails must be powered off within 10 ms from the first rail powering off.

NB9M: VGACORE +0.90V (Normal) , +1.09V

NVVDD Maximum Settling Time

PEX_RST timing



Quanta Computer Inc.

PROJECT :Z09

Size	Document Number	Rev
	N13P-LP (MEMORY I/F) 2/5	3A

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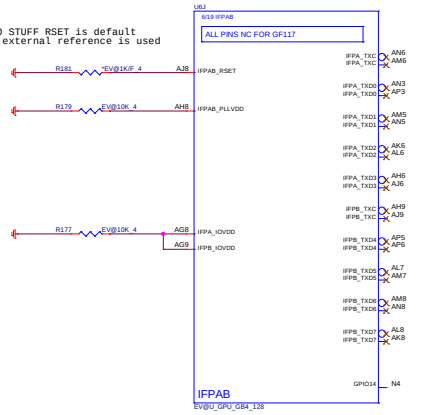
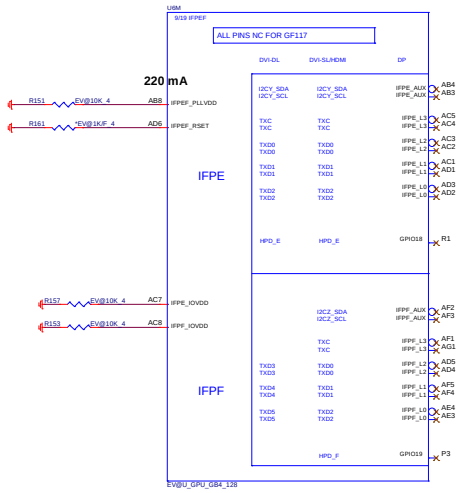
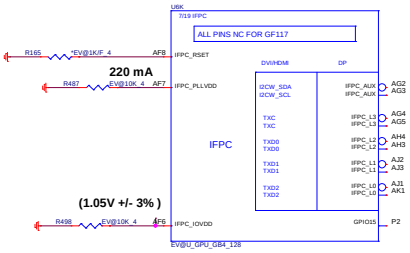
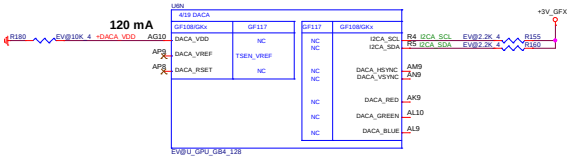
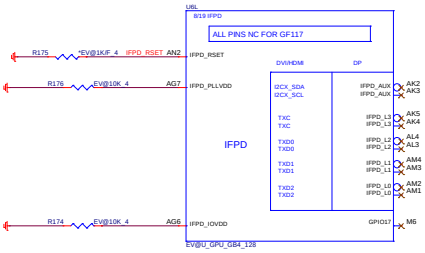
IFPAB ONLY: NO STUFF RSET is default
Required when external reference is used

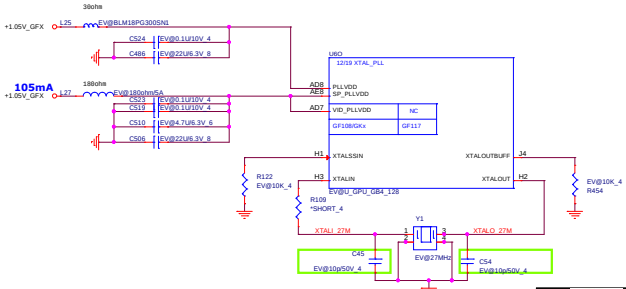












20120201 Change CAP from 27P to 10P.

Quanta Computer Inc.
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Size	Document Number	Rev
	N13P-LP (DISPLAY) 3/5	3A

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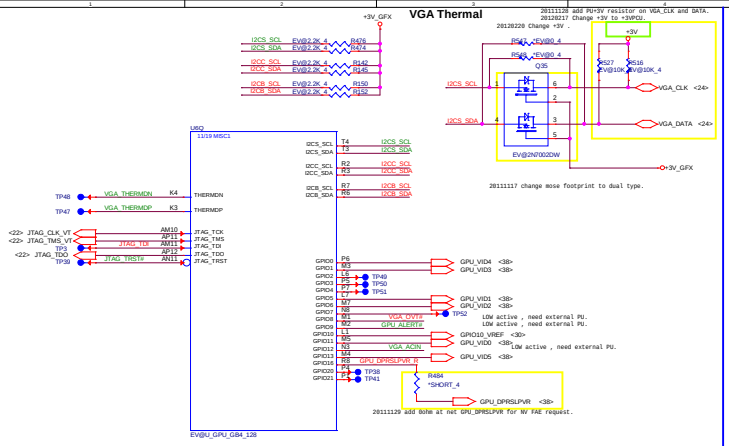
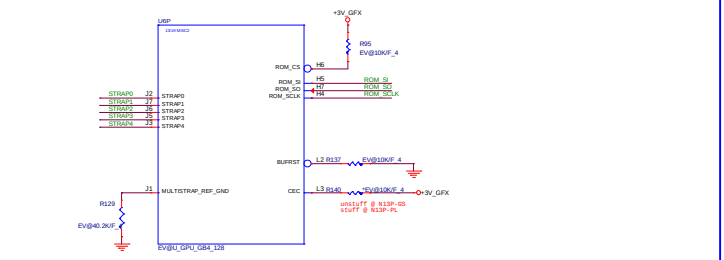
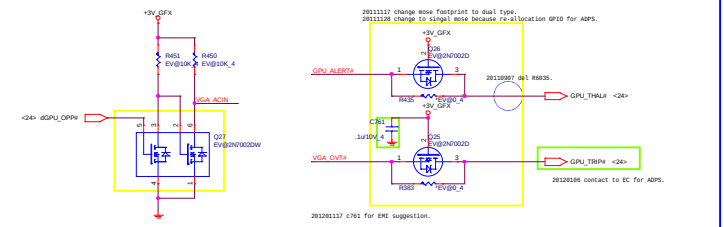
VGA Thermal







ADDRESS:
98H

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	N13P-GS	N13P-GL
ROM_SO	N13P-LP FB[1] N13P-GL XCLK_417	N13P-LP FB[0] N13P-GL FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	1001	
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	N13P-LP PCI_DEVIDE[5] N13P-GL SLOT_CLK_CFG	PEX_PLL_EN_TERM	1010	
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	xxxx	
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111	
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110	
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0011	
STRAP3	SOR_EXPOSED[3]	SOR_EXPOSED[2]	SOR_EXPOSED[1]	SOR_EXPOSED[0]	0000	
STRAP4	Reserve	PCIE_SPEED CHANGE_GEN3	PCI_MAX_SPEED	DP_PLL_VDD33V	0001	

	PU to VDD33	PD to GND
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

4.99K/F_4 ==> CS24992FB26
10K/F_4 ==> CS31002FB26
15K/F_4 ==> CS31502FB24
20K/F_4 ==> CS32002FB29
24.9K/F_4 ==> CS32492FB16
30.1K/F_4 ==> CS33012FB18
34.8K/F_4 ==> CS33482FB22
35.7K/F_4 ==> CS33572FB13
45.3K/F_4 ==> CS34532FB18

GF108:N12P
GF117:N13M
GK107:N13P

VRAM Configuration Table

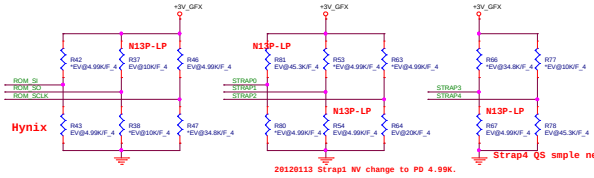
RAMCFG [3:0]	DESCRIPTION	Quanta PN(Q buy)	Quanta PN(W buy)	Vendor PN
* 0x1(0001)	1250MHz 2GB(64M*32) Samsung	AKG5MWDT505		K4G20325FD-FC04
0x0(0000)	1250MHz 2GB(64M*32) Hynix	AKG5MWUTW01		H5GQ2H24MFR-T2C
0x0(0100)	1250MHz 2GB(64M*32) Hynix	AKG5MWUTW10		H5GQ2H24AFR-T2C
	1250MHz 2GB(64M*32) Elpida	AKG5MGUT400		EDW2032BBBG-50-F

Elpida Need confirmation with NV RVL
Hynix H5GQ2H24AFR-T2C will build next or MP.

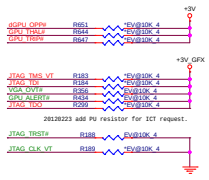
	Register value
ROM_SO	N13P-LP 10K pull up.
ROM_SCLK	N13P-LP need 4.99K pull up;
ROM_SI	2G:Hynix =4.99k pull down(M-die) 2G:Hynix =24.9k pull down(A-die)
STRAP0	N13P-LP 45.3K pull high
STRAP1	N13P-LP 4.99k pull down
STRAP2	N13P-LP need 20K pull down.
STRAP3	STRAP3 N13P-LP need 4.99K pull down.
STRAP4	STRAP4 N13P-LP need 45.3K pull down for GEN3.

ROM_SI Strap Bit for RAM Mapping

N13P-LP DID => 0X0FD3



20120113 Strap1 NV change to PD 4.99K.



GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	**OUT**	N/A	NVVDD VID4
1	OUT	N/A	NVVDD VID3
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID1
6	OUT	N/A	NVVDD VID2
7	OUT	N/A	3D STEREO
8	I/O	LOW	GPU Overtemp
9	I/O	LOW	GPU ALERT
10	OUT	N/A	FB Vref Control (not used sDDR3)
11	OUT	N/A	NVVDD VID0
12	IN	N/A	PWR_Level AC Detect
13	OUT	N/A	NVVDD VID5
14	IN	N/A	HPD for IFP AB (not used)
15	IN	N/A	HPD for IFP C (HDMI)
16	OUT	N/A	MEM_VDD_CTL
17	IN	N/A	HPD for IFP D (not used)
18	IN	N/A	HPD for IFP E (TMDS)
19	IN	N/A	HPD for IFP F (not used)
20	N/A	N/A	NVGEM Debug GPIO13
21	N/A	N/A	NVGEM Debug GPIO14

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Size	Document Number	Rev
	N13P-LP (GPIO&STRAPS)4/5	3A

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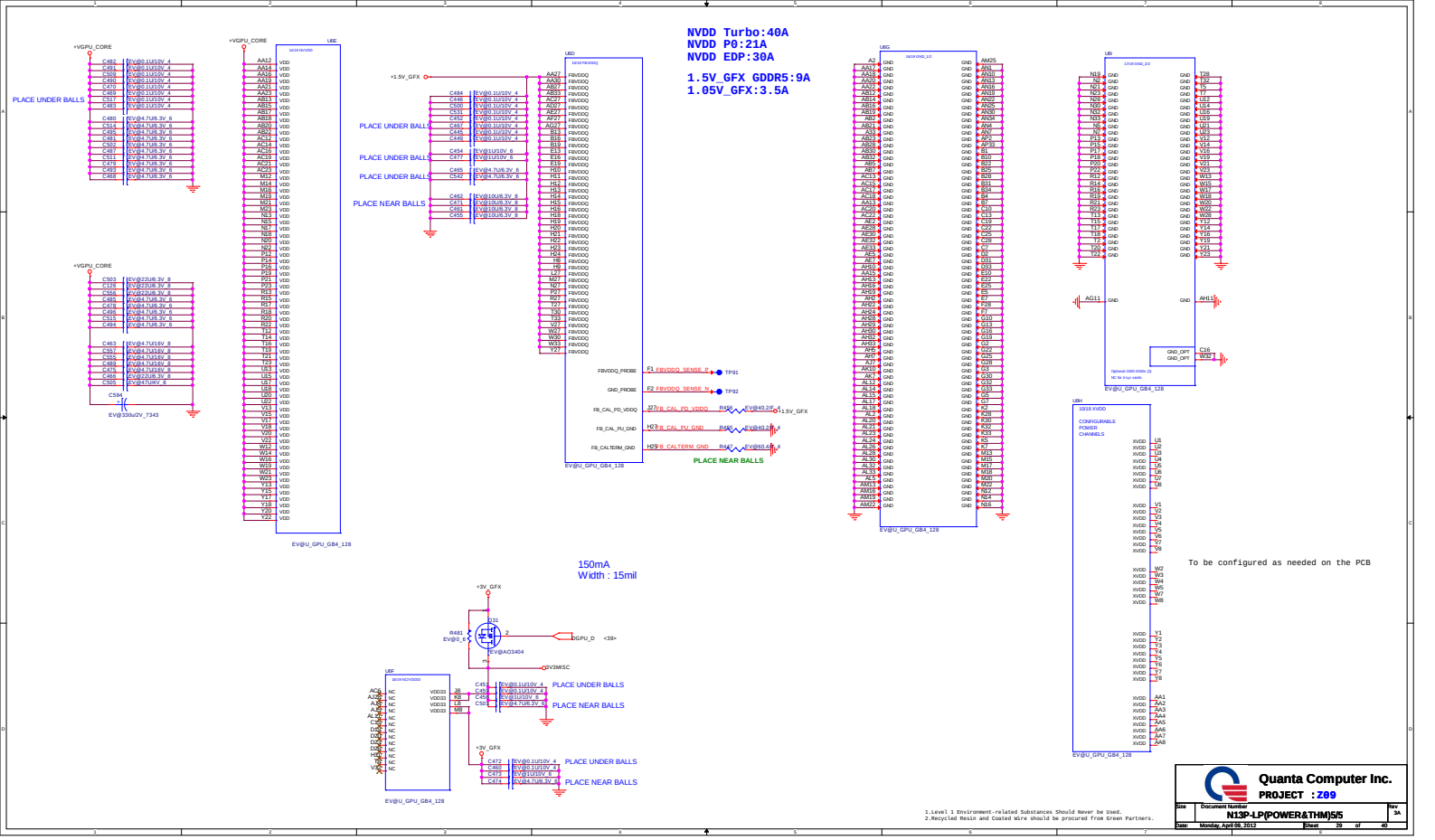

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
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Size	Document Number	Rev
	N13P-LP(POWER&THM)5/5	3A

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CHANNEL A: 1024MB GDDR5x32

LOWER HALF

Channel 0 <0-31>
MF=0 Non-mirrored

QD24~31
QD16~23
QD8~15
QD0~7

Channel 0 <32-63>
MF=1 Mirrored

QD32~39
QD40~47
QD48~55
QD56~63

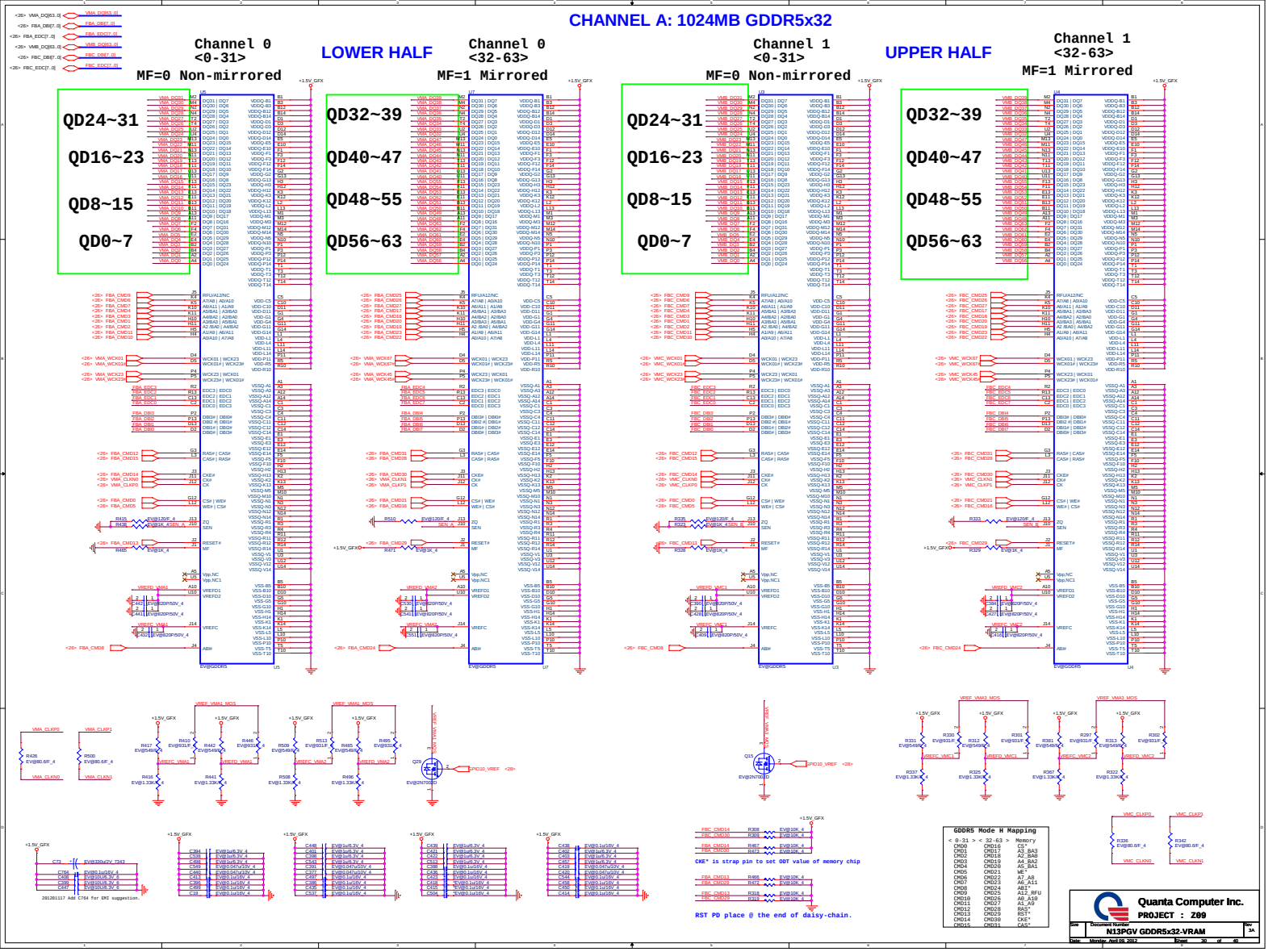
UPPER HALF

Channel 1 <0-31>
MF=0 Non-mirrored

QD24~31
QD16~23
QD8~15
QD0~7

Channel 1 <32-63>
MF=1 Mirrored

QD32~39
QD40~47
QD48~55
QD56~63



CKE* is strap pin to set ODT value of memory chip

RST PD place @ the end of daisy-chain.

20120117 Add C764 for EMI suggestion.

GDDR5 Mode H Mapping

< 8-31 >	< 32-63 >	Memory
CMD0	CMD16	CS*
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	AB1*
CMD9	CMD25	A12_RFU
CMD10	CMD26	A9_A10
CMD11	CMD27	A8_A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CAS*

Quanta Computer Inc.
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Size	Document Number	Rev
	N13PGV GDDR5x32-VRAM	3A

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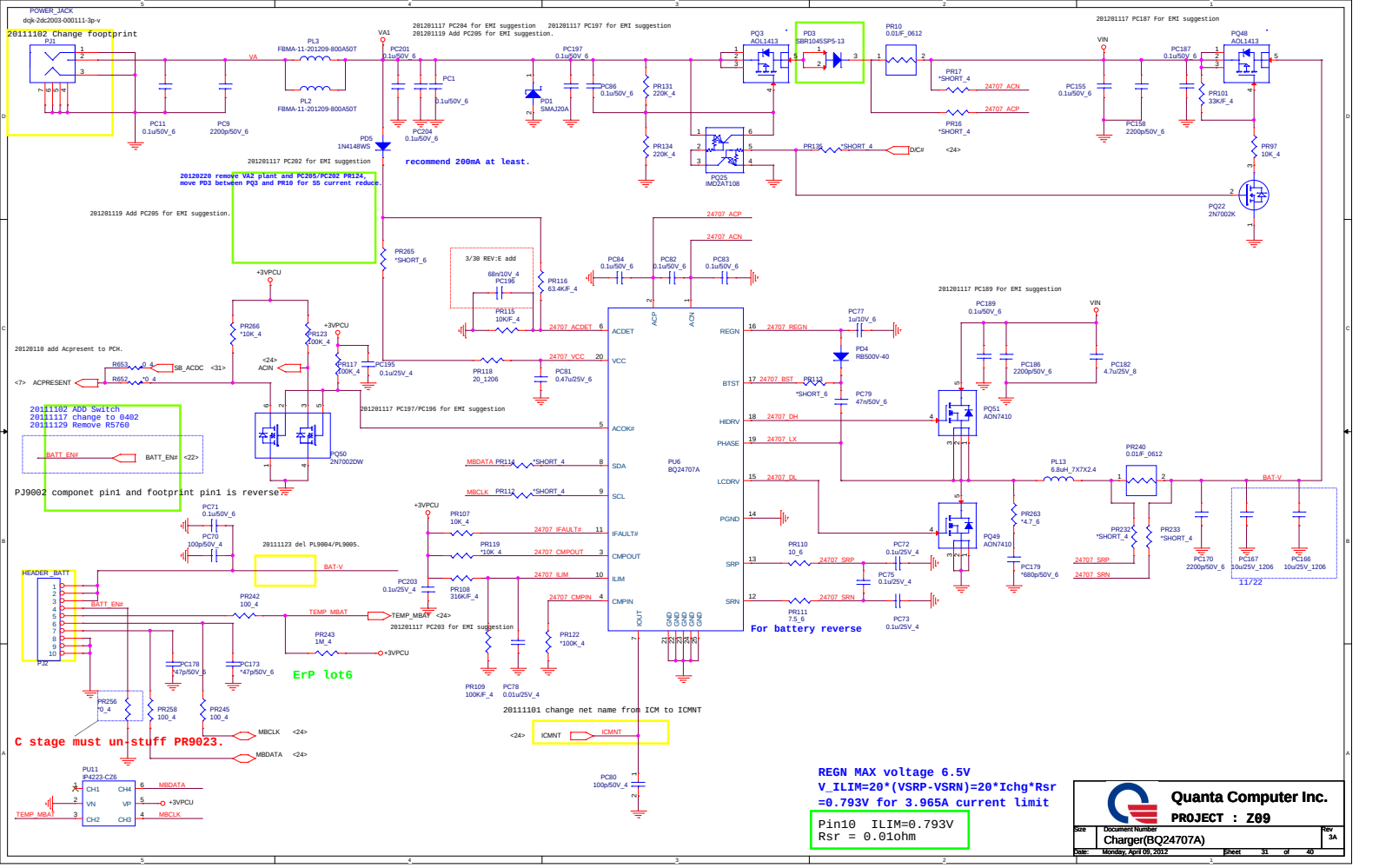
POWER_JACK
dcjk-2dc2003-000111-3p-v
20111102 Change footprint
PJ1
PL3
FBMA-11-201209-800A50T
PL2
FBMA-11-201209-800A50T
VA
VA1
PC201
0.1u/50V_6
PC1
0.1u/50V_6
PC204
0.1u/50V_6
PC11
0.1u/50V_6
PC9
2200p/50V_6
PD5
1N4148WS
201201117 PC204 for EMI suggestion
201201117 PC197 for EMI suggestion
201201119 Add PC205 for EMI suggestion.
PC197
0.1u/50V_6
PD1
SMAJ20A
PC86
0.1u/50V_6
PR131
220K_4
PR134
220K_4
PQ3
AOL1413
PD3
SBR1045SP5-13
PR10
0.01/F_0612
PR17
*SHORT_4
24707_ACN
PR16
*SHORT_4
24707_ACP
PR135
*SHORT_4
D/C#
<24>
PQ25
IMD2AT108
201201117 PC187 For EMI suggestion
VIN
PC155
0.1u/50V_6
PC158
2200p/50V_6
PC187
0.1u/50V_6
PQ48
AOL1413
PR101
33K/F_4
PR97
10K_4
PQ22
2N7002K
recommend 200mA at least.
20120220 remove VA2 plant and PC205/PC202 PR124,
move PD3 between PQ3 and PR10 for S5 current reduce.
201201117 PC202 for EMI suggestion
201201119 Add PC205 for EMI suggestion.
PR265
*SHORT_6
3/30 REV:E add
68n/10V_4
PC196
PR115
10K/F_4
PR116
63.4K/F_4
24707_ACDET
PC84
0.1u/50V_6
PC82
0.1u/50V_6
PC83
0.1u/50V_6
24707_ACP
24707_ACN
+3VPCU
PR266
*10K_4
PR123
100K_4
20120110 add Acpresent to PCH.
R653
0_4
SB_ACDC
<31>
R652
0_4
<7>
ACPRESENT
<24>
ACIN
PR117
100K_4
PC195
0.1u/25V_4
PR118
20_1206
24707_VCC
PC81
0.47u/25V_6
20111102 ADD Switch
20111117 change to 0402
20111129 Remove R5760
BATT_EN#
BATT_EN#
<22>
PQ60
2N7002DW
201201117 PC197/PC196 for EMI suggestion
MBDATA
PR114
*SHORT_4
MBCLK
PR112
*SHORT_4
PJ9002 componet pin1 and footprint pin1 is reverse
PU6
BQ24707A
ACDET
VCC
ACOK#
SDA
SCL
IFAULT#
CMPOUT
ILIM
CMPIN
ACP
ACN
IOUT
REGN
BTST
HIDRV
PHASE
LCDRV
PGND
SRP
SRN
24707_REGN
24707_BST
24707_DH
24707_LX
24707_DL
24707_IFAULT#
24707_CMPOUT
24707_ILIM
24707_CMPIN
PC77
1u/10V_6
PD4
RB500V-40
PR113
*SHORT_6
PC79
47n/50V_6
201201117 PC189 For EMI suggestion
PC189
0.1u/50V_6
PC186
2200p/50V_6
PC182
4.7u/25V_8
PQ51
AON7410
PR240
0.01/F_0612
PL13
6.8uH_7X7X2.4
BAT-V
PC71
0.1u/50V_6
PC70
100p/50V_4
20111123 del PL9004/PL9005.
BAT-V
HEADER_BATT
PJ2
BATT_EN#
PR342
100_4
TEMP_MBAT
TEMP_MBAT
<24>
PR243
1M_4
+3VPCU
PC178
*47p/50V_6
PC173
*47p/50V_6
ErP lot6
PR256
*0_4
PR258
100_4
PR245
100_4
MBCLK
<24>
MBDATA
<24>
C stage must un-stuff PR9023.
PU11
IP4223-CZ6
CH1
CH4
VN
VP
CH2
CH3
MBDATA
+3VPCU
MBCLK
TEMP_MBAT
+3VPCU
PR107
10K_4
PR119
*10K_4
PC203
0.1u/25V_4
PR108
316K/F_4
201201117 PC203 for EMI suggestion
PR109
100K/F_4
PC78
0.01u/25V_4
PR122
*100K_4
20111101 change net name from ICM to ICMNT
<24>
ICMNT
ICMNT
PC80
100p/50V_4
PR110
10_6
24707_SRP
PC72
0.1u/25V_4
PC75
0.1u/25V_4
PR111
7.5_6
24707_SRN
PC73
0.1u/25V_4
For battery reverse
PQ49
AON7410
PR263
*4.7_6
PC179
*680p/50V_6
PR232
*SHORT_4
PR233
*SHORT_4
PC170
2200p/50V_6
PC167
10u/25V_1206
PC166
10u/25V_1206
11/22
REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit
Pin10 ILIM=0.793V
Rsr = 0.01ohm
Quanta Computer Inc.
PROJECT : Z09
Size
Document Number
Charger(BQ24707A)
Rev
3A
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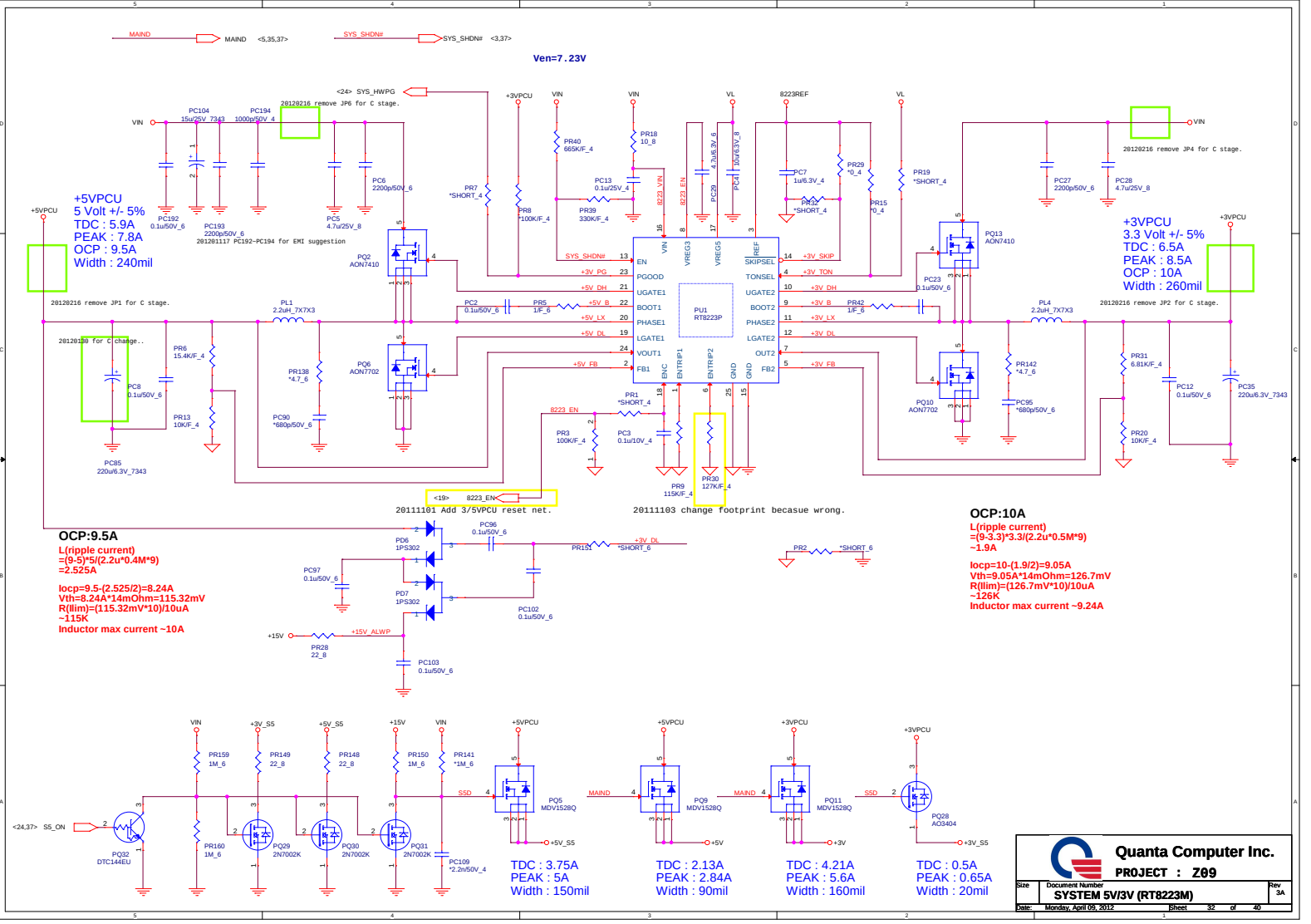
MAIND
MAIND <5,35,37>
SYS_SHDN#
SYS_SHDN# <3,37>
Ven=7.23V
<24> SYS_HWPG
20120216 remove JP6 for C stage.
+5VPCU
5 Volt +/- 5%
TDC : 5.9A
PEAK : 7.8A
OCP : 9.5A
Width : 240mil
20120216 remove JP1 for C stage.
20120216 remove JP4 for C stage.
+3VPCU
3.3 Volt +/- 5%
TDC : 6.5A
PEAK : 8.5A
OCP : 10A
Width : 260mil
20120216 remove JP2 for C stage.
PU1
RT8223P
20111101 Add 3/5VPCU reset net.
20111103 change footprint becasue wrong.
OCP:9.5A
L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)
=2.525A
Iocp=9.5-(2.525/2)=8.24A
Vth=8.24A*14mOhm=115.32mV
R(Ilim)=(115.32mV*10)/10uA
~115K
Inductor max current ~10A
OCP:10A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*9)
~1.9A
Iocp=10-(1.9/2)=9.05A
Vth=9.05A*14mOhm=126.7mV
R(Ilim)=(126.7mV*10)/10uA
~126K
Inductor max current ~9.24A
TDC : 3.75A
PEAK : 5A
Width : 150mil
TDC : 2.13A
PEAK : 2.84A
Width : 90mil
TDC : 4.21A
PEAK : 5.6A
Width : 160mil
TDC : 0.5A
PEAK : 0.65A
Width : 20mil
Quanta Computer Inc.
PROJECT : Z09
SYSTEM 5V/3V (RT8223M)
Rev 3A
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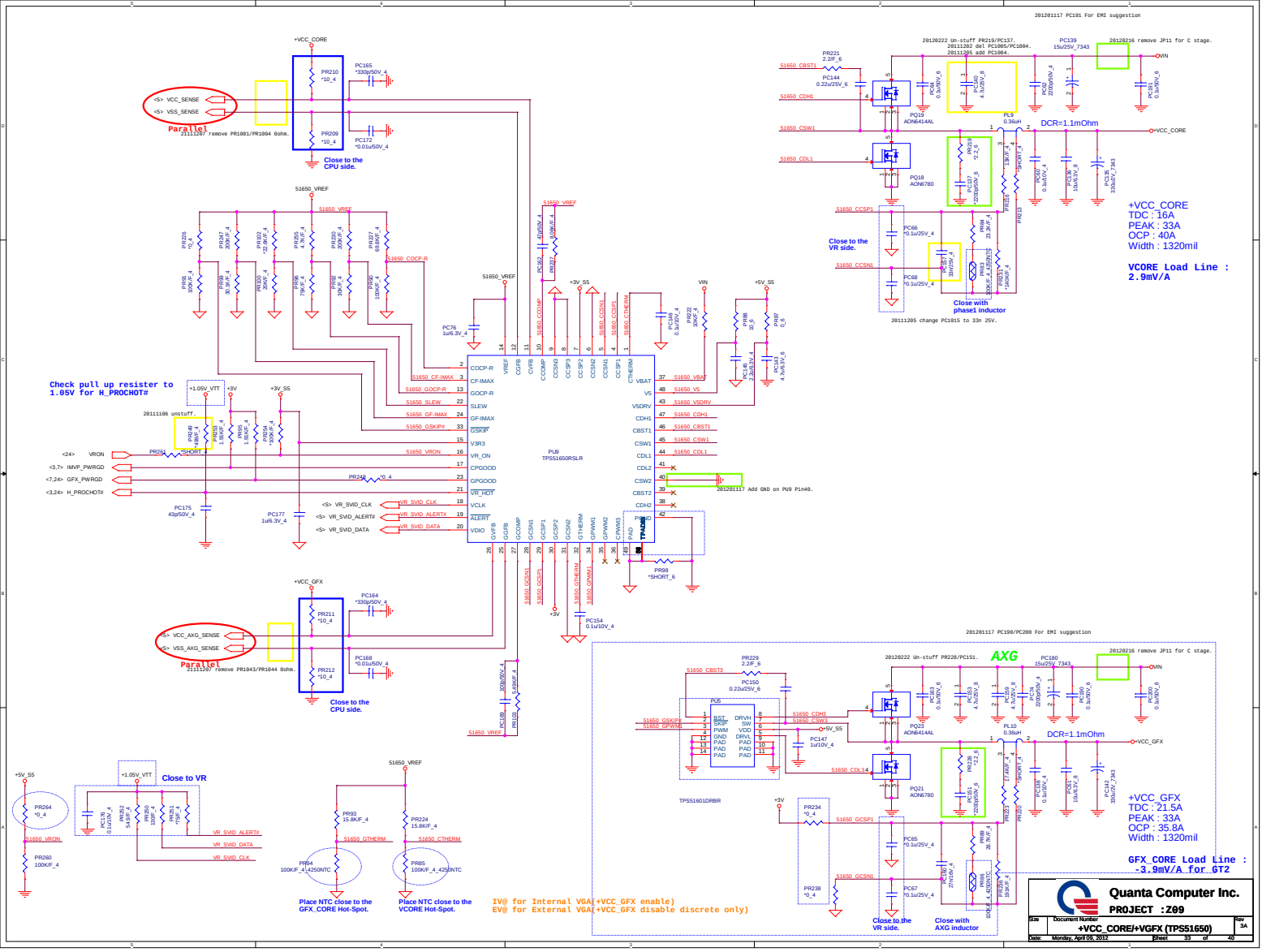
20120117 PC191 For EMI suggestion
+VCC_CORE
<5> VCC_SENSE
<5> VSS_SENSE
Parallel
20111207 remove PR1001/PR1004 0ohm.
Close to the CPU side.
51650_VREF
51650_COCP-R
51650_CF-IMAX
51650_GOCP-R
51650_SLEW
51650_GF-IMAX
51650_GSKIP#
51650_VRON
51650_VBAT
51650_V5
51650_VSDRV
51650_CDH1
51650_CBST1
51650_CSW1
51650_CDL1
Check pull up resister to 1.05V for H_PROCHOT#
20111106 unstuff.
<24> VRON
<3,7> IMVP_PWRGD
<7,24> GFX_PWRGD
<3,24> H_PROCHOT#
<5> VR_SVID_CLK
<5> VR_SVID_ALERT#
<5> VR_SVID_DATA
PU9
TPS51650RSLR
20111117 Add GND on PU9 Pin40.
+VCC_GFX
<5> VCC_AXG_SENSE
<5> VSS_AXG_SENSE
Parallel
20111207 remove PR1043/PR1044 0ohm.
Close to the CPU side.
Close to VR
Place NTC close to the GFX_CORE Hot-Spot.
Place NTC close to the VCORE Hot-Spot.
IV@ for Internal VGA(+VCC_GFX enable)
EV@ for External VGA(+VCC_GFX disable discrete only)
20120222 Un-stuff PR219/PC137.
20111202 del PC1005/PC1004.
20111205 add PC1004.
20120216 remove JP11 for C stage.
DCR=1.1mOhm
+VCC_CORE
TDC : 16A
PEAK : 33A
OCP : 40A
Width : 1320mil
VCORE Load Line : 2.9mV/A
Close to the VR side.
Close with phase1 inductor
20111205 change PC1015 to 33n 25V.
20120117 PC190/PC200 For EMI suggestion
AXG
20120222 Un-stuff PR228/PC151.
TPS51601DRBR
+VCC_GFX
TDC : 21.5A
PEAK : 33A
OCP : 35.8A
Width : 1320mil
GFX_CORE Load Line : -3.9mV/A for GT2
Close to the VR side.
Close with AXG inductor
Quanta Computer Inc.
PROJECT :Z09
+VCC_CORE/+VGFX (TPS51650)
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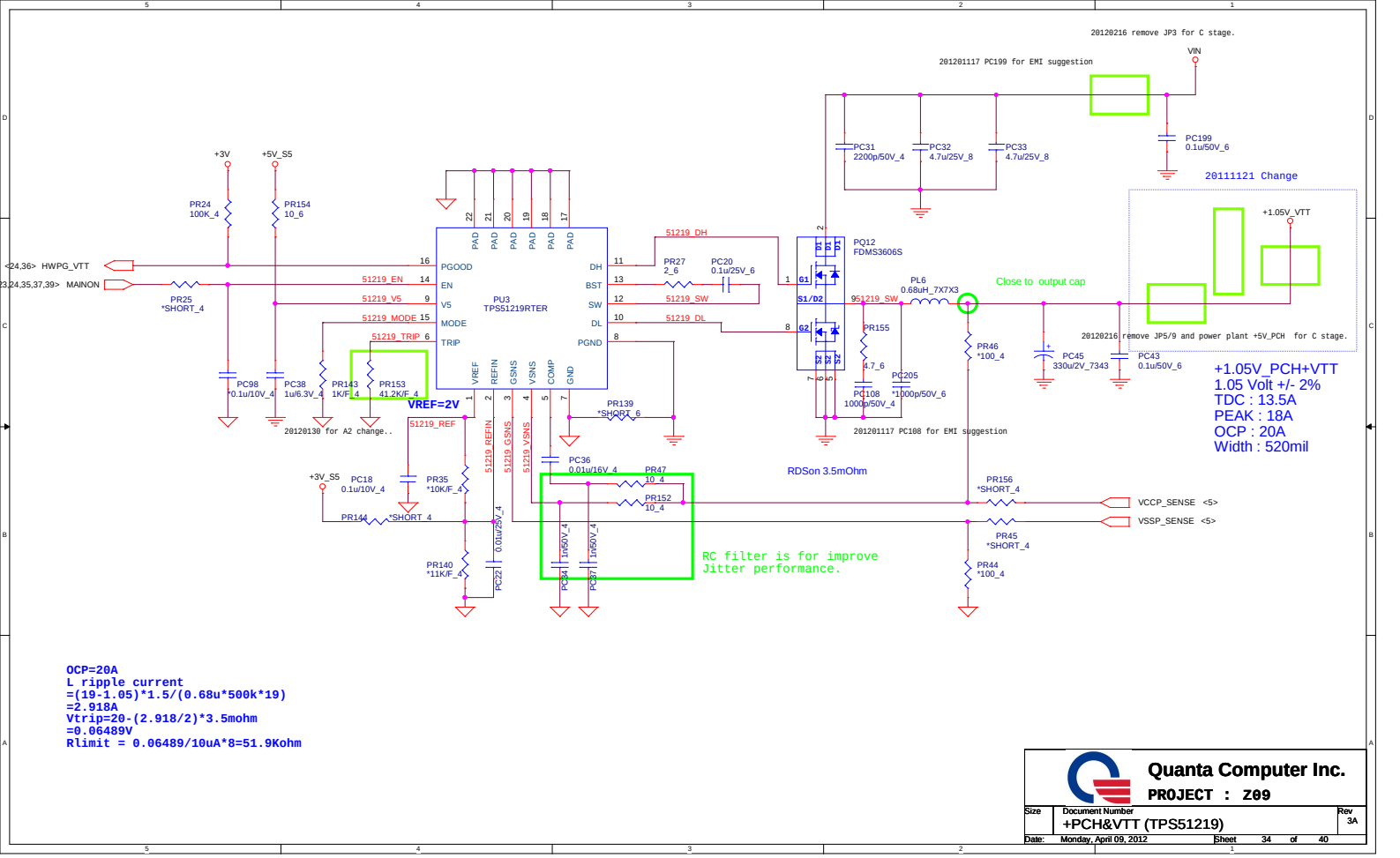

OCP=20A
L ripple current
=(19-1.05)*1.5/(0.68u*500k*19)
=2.918A
Vtrip=20-(2.918/2)*3.5mohm
=0.06489V
Rlimit = 0.06489/10uA*8=51.9Kohm

Quanta Computer Inc.			
PROJECT : Z09			
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	+PCH&VTT (TPS51219)		3A
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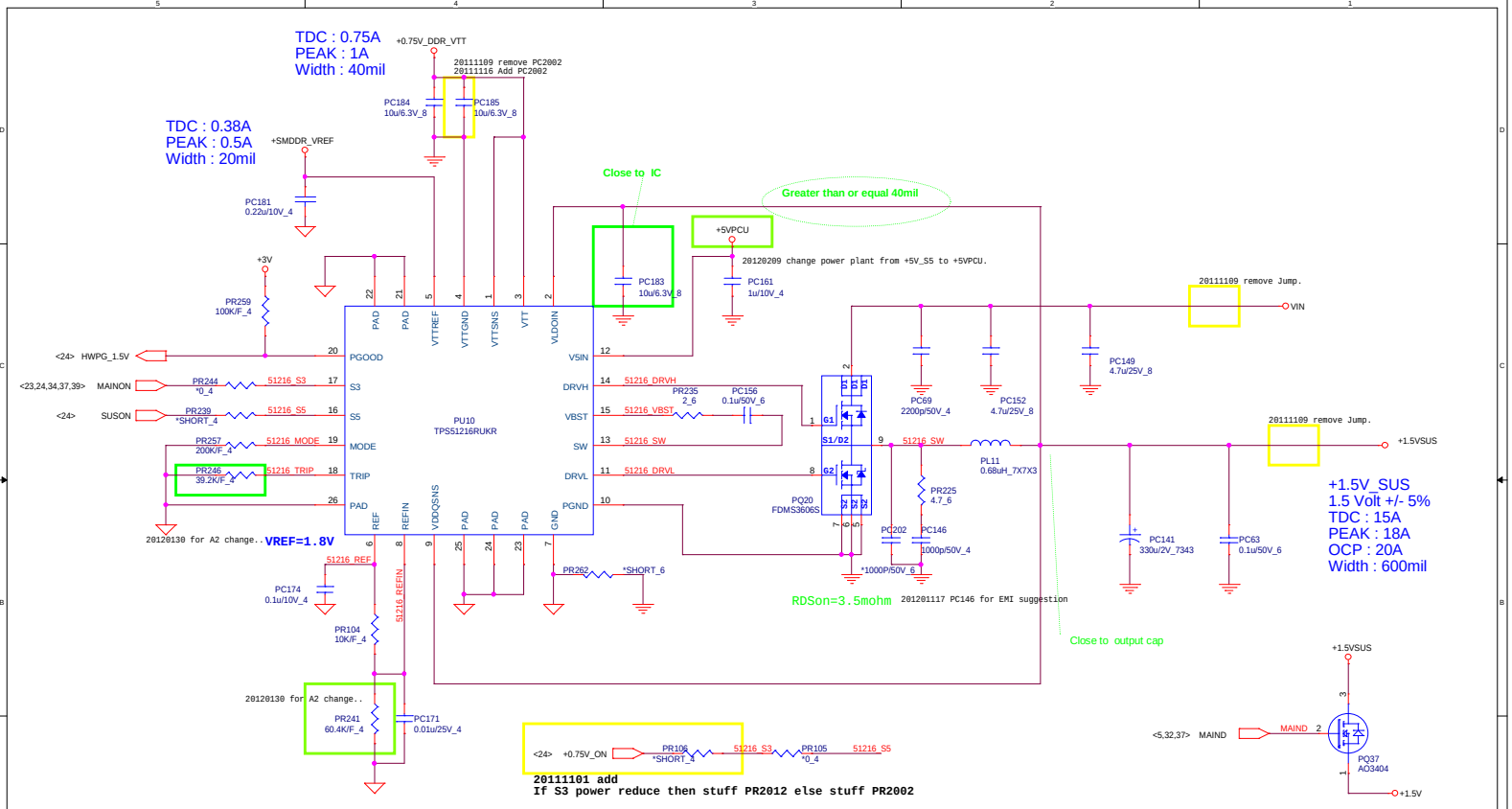

OCP=20A
L ripple current
=(19-1.5)*1.5/(0.68u*400k*19)
=5.079A
Vtrip=20-(5.079/2)*3.5mohm
=0.06111V
Rlimit=0.06111/10uA*8=48.88Kohm

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : Z09

Size	Document Number	Rev
	DDR 1.5V(TPS51216)	3A

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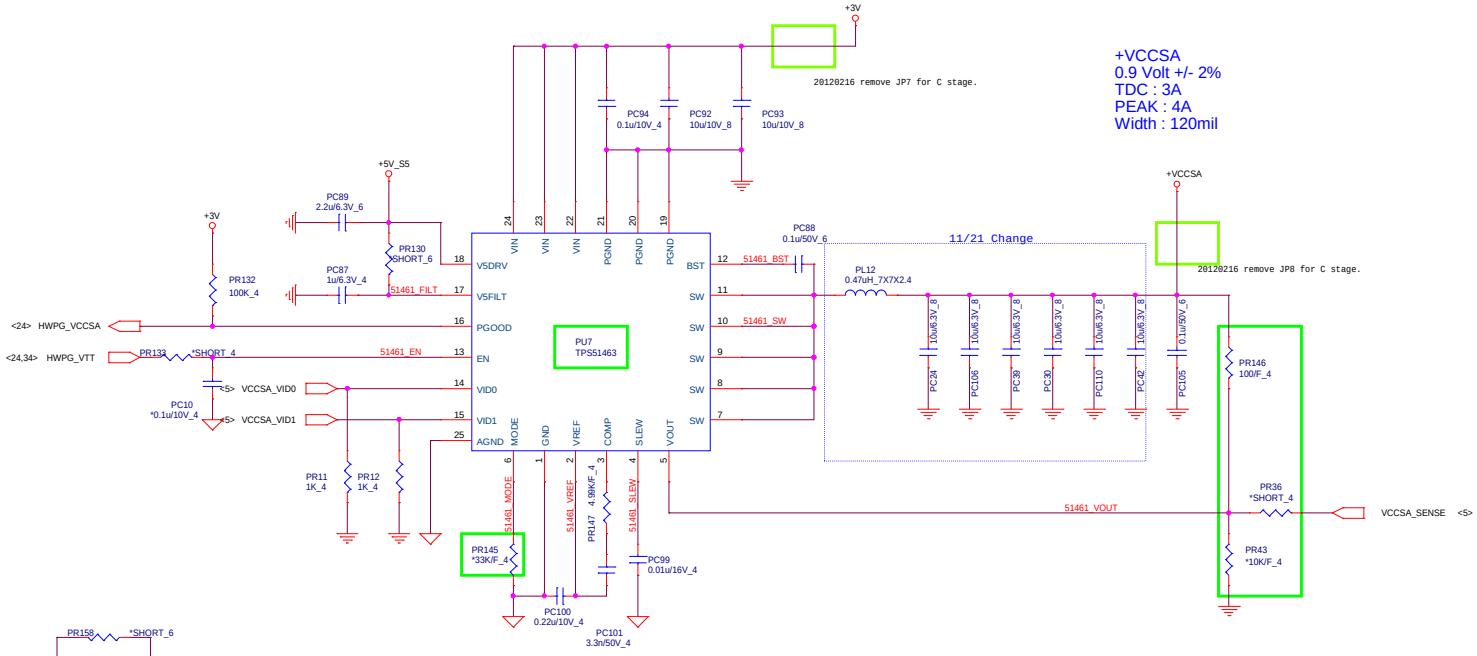

201201117 PR146 change to 365ohm,un-stuff PR36,stuff PR43,stuff PR145, PU7 change to TPS51463.
20120220 PR145 un-stuff,PR145 change to 100,PR43 un-stuff, PR36 short pad.

VID0	VID1	+VCCSA
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

default 0.9V

PR145 33kohm
PR146 change to 365ohm
PR36 nc
PR43 10kohm
PU7 Change to 51463

Quanta Computer Inc.
PROJECT : Z09

Size	Document Number	Rev
	VCCSA(TPS51461)	3A

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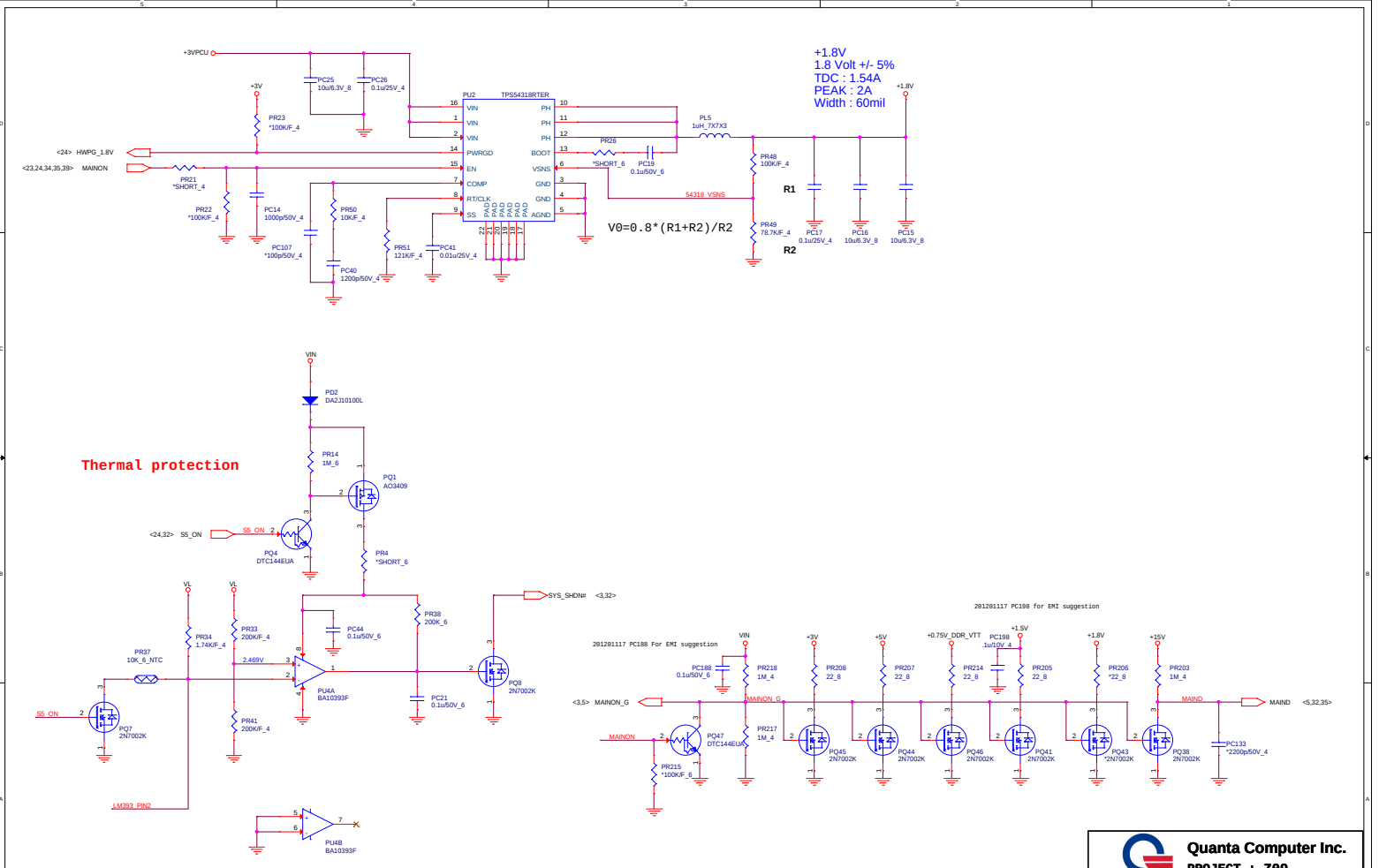

Quanta Computer Inc.

PROJECT : Z09

Size	Document Number	Rev
	+1.8V/Discharge/Thermal	3A

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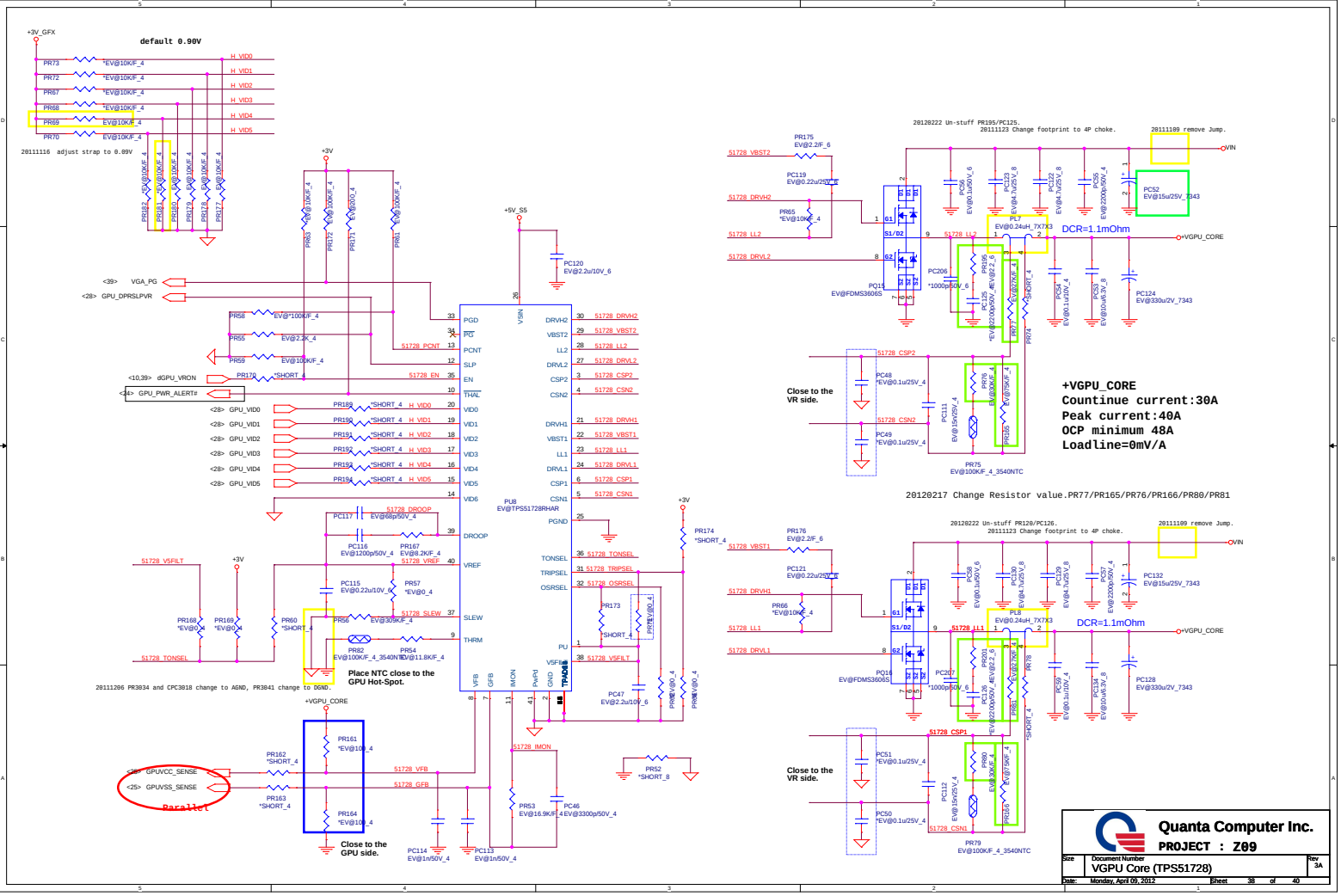
default 0.90V
20111116 adjust strap to 0.89V
20120222 Un-stuff PR195/PC125.
20111123 Change footprint to 4P choke.
20111109 remove Jump.
DCR=1.1mOhm
+VGPU_CORE
Countinue current:30A
Peak current:40A
OCP minimum 48A
Loadline=0mV/A
20120217 Change Resistor value.PR77/PR165/PR76/PR166/PR80/PR81
20120222 Un-stuff PR120/PC126.
20111123 Change footprint to 4P choke.
20111109 remove Jump.
DCR=1.1mOhm
Close to the VR side.
Place NTC close to the GPU Hot-Spot.
20111206 PR3034 and CPC3018 change to AGND, PR3041 change to DGND.
Parallel
Close to the GPU side.
PU8
EV@TPS51728RHAR
TPS51728
Quanta Computer Inc.
PROJECT : Z09
Size
Document Number
VGPU Core (TPS51728)
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3A
Date: Monday, April 09, 2012
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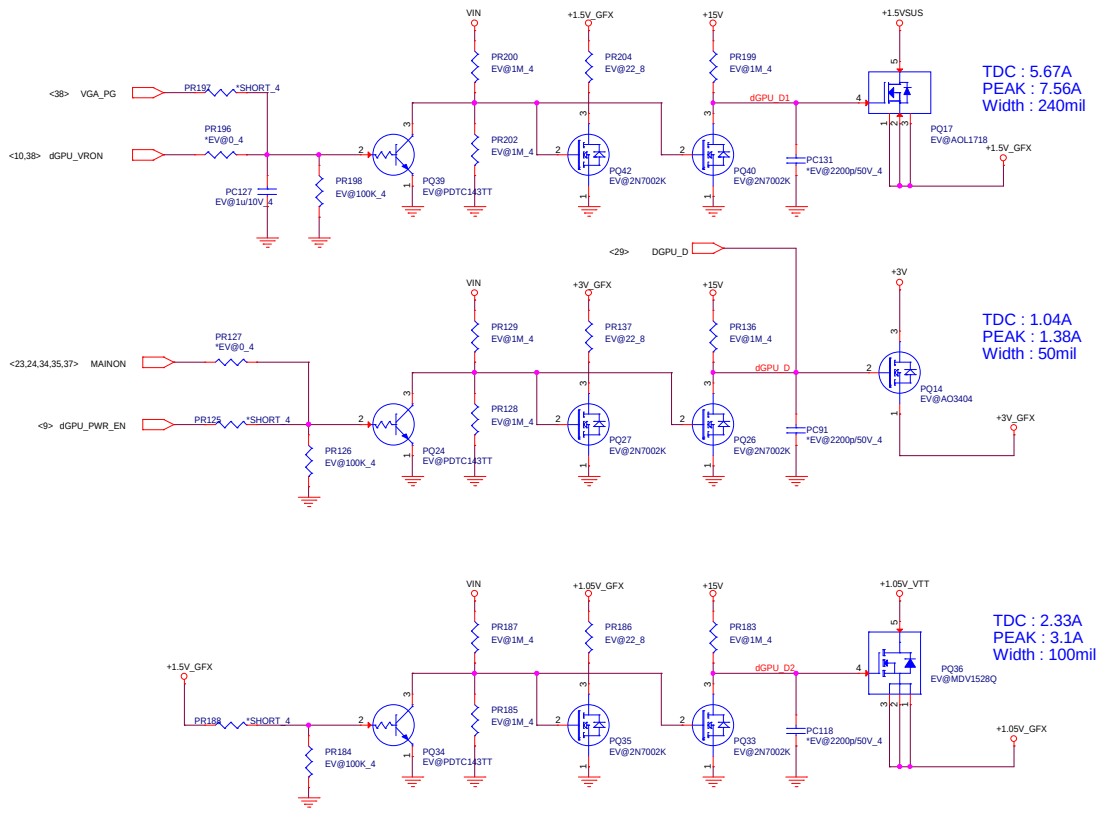

Quanta Computer Inc.

PROJECT : Z09

Size	Document Number	Rev
	GPU_PWR	3A

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Model	REV	CHANGE LIST	MODEL Z09 FROM	To
	10.28	FIRST RELEASED		
Z09	1A	1. 20111031 Modify U18 symbol(Add PAD gnd*9).		
		2. 20111031 Page 19 Add LED/Cardreader con.(only Power and Battery)		
		3. 20111031 Page 20/21 remove mSATA/Main HDD re-driver IC.		
		4. 20111031 Page24 Change U5639 USB power switch power well from +5VPCU to +5V_S5.		
		5. 20111031 Page 24 Un-staff USB9+/- resistor because it si reserve only debug use.		
		6. 20111031 Page 11 Add Q18/19 mose for DSW circuit.		
		7. 20111101 Page 07 Remove LVDS Data/clock.		
		8. 20111101 Page 03 Add Resistor R182/R185.		
		9. 20111101 Page 28 stuff R304 for BT power.		
		10. 20111101 Page 32-40 Power update circuit.		
		12. 20111102 Page17 Change R554 from 0ohm to 2.2ohm for Prevent EDS issue.		
		13. 20111102 del R160		
		14. 20111102 page7 PDI and DMI reverse.		
		15. 20111102 page8 R5757 stuff for PGE reverse.		
		16. 20111102 page8 Ball G48 connect test point.		
		17. 20111102 update connector list without LVDS/HDMI/Audio/USB3/RJ45/ODD/KB.		
		18. 20111102 Page 02 Reverse PEG.		
		19. 20111103 page 25 add pull up 10k R305 to PSI CS#.		
		20. 20111103 page 9 remove dGPU_PWM_SELECT# change to dGPU_PBW_RN PD.		
		21. 20111104 page 3 R5332 PU from +1.5VSUS TO +1.5V_CPU because leakage issue.		
		22. 20111104 page 40,41 add memory down.		
		23. 20111104 page 26-31 change GPU solution from 13P-GV to 13P-PL.		
		24. 20111104 page 02 change R5453 from 10K to 1K PU_PR1029		
		25. 20111106 page 32 Un-stuf PR1029.base on CRB.20111107 R5180 un-stuff.		
		26. 20111107 page 07 R5180 un-stuff. because DRAMPWEGD change to +5V_CPU.		
		27. 20111107 page 14 unstuff R5347/R3E2 and stuff Q5810 for Deep S3.		
		28. 20111107 page 14 remove R5144 PU +1.5VSUS.		
		29. 20111107 page 20 move debuge port to CN3.		
		29. 20111107 page 07 R469 change from 10k to 4.99k.		
		30. 20111108 page08 PU 10k to +3V, because no sata LED.		
		31. 20111108 page15 add feature board con.		
		32. 20111108 page19 add TPM con.		
		33. 20111109 page09 VCC core CAP change to.		
		total : 22uF x 12		
		22uF : 470u x 3(power side*1)		
		ADL:		
		tatal : 470u x 1(power side*1)		
		34. 20111109 page36 remove PC2002 and JUMP.		
		35. 20111109 page39 remove JUMP.		
		36. 20111109 page14 remove XDP.		
		37. 20111109 page02 add PEG tox16.		
		38. 20111110 page07 remove R630/R601.		
		39. 20111110 page08 R411 change power plant to +3V_PCH_ME		
		40. 20111110 Move R6168 to page04.		
		41. 20111111 page07 Reverse DMI/PSI to normal.		
		42. 20111111 page16 R423 change to 56K(Vout=3SV,R65 to 10K, R3E un-stuff,stuff R57/C37 and R67 change to 9.09K (for phas shif mode). R5312	2A	3A
		43. 20111111 page07 add 0ohm R5312 on DMBx.	2A	3A
		44. 20111111 Remove codec to D8 board.	2A	3A
		45. 20111111 page20 Remove Feature con and CRT cricuit, add RJ45.	2A	3A
		46. 20111114 Update CN25,CN5868,CN5807 footprint .	2A	3A
		47. 20111114 Page19 Un-stuff D8/R45.	2A	3A
		48. 20111114 Page20 CN17 from 24pin change to 30pin, add TP function and add TPM and Audio connector	2A	3A
		49. 20111115 Update CN23 footprint.	2A	3A
		50. 20111116 page36 add PC2002.	2A	3A
		51. 20111116 page08 Base on EMI request add C2404 22P on PCH BITCLK and R256/C6495 and Stuff R411.	2A	3A
		52. 20111116 page25 EC add GPIO26 dGPU_OVT# to GPU for ADPS,Change net name GPIO27 to USB_CHG_EN, GPIO97 to USB_CHG_MODE,GPIO43 net name change to GPU_THAL#.	2A	3A
		53. 20111116 page19 change transformer from GigaLan to 10/100*2, remove ESD U8/12.	3A	3B
		54. 20111116 page08 Change RTC connector and un-stuff Q36,R415,R416,R422,R414.	3A	3B
		55. 20111116 page08 Change back RTC connector and stuff Q36,R415,R416,R422,R414.	3A	3B
		56. 20111117 page32 BTT_EN# from push button change to short pad and connect to D8 board.	3A	3B
		57. 20111117 page11 Remove 0ohm short pad,R5051/R5044/R5834/R5149/R5220/R5939/R5042.	3A	3B
		58. 20111117 update CN3/Cn18/CN12/CN17/SW2 footprint.	3A	3B
		59. 20111117 page24 remove R61112/R61110 no charge option.R5176,del PQ35 change Q48 for dul mose type.	3A	3B
		60. 20111117 page09 R5176 change to singal resistor because GPIO40-42 GPIO9 for memory down ID.	3A	3B
		61. 20111117 change Q5603/Q23/Q16/Q38/Q26/Q41/Q4646/Q5043 footprint to dual type mose Del Q17/Q31/Q27/Q42/Q5041/Q5045.	3A	3B
		62. 20111117 page20 Change R355 to L6 for EMI request.	3A	3B
		63. 20111118 page17 Change R474 to 100kohm.	3A	3B
		64. 20111118 page16 Remove LCD power C21/C12	3A	3B
		65. 20111118 page16 Change RTC connector.	3A	3B
		66. 20111118 change Q21/Q39 footprint to dual type mose Del Q43/Q40, mose return back to Q26/Q27.	3A	3B
		67. 20111118 page09 GPIO40-42,GPIO69 change net name to RAM_IDD-3.	3A	3B
		68. 20111121 page08 Change RTC battery back to socket.	3A	3B
		69. 20111121 page21 change back transformer to single giga LAN.	3A	3B
		70. 20111121 page23 Add screw hole*13.	3A	3B
		71. 20111121 page16 change L96 to 10u 0.1A .	3A	3B
		72. 20111121 page03 remove R5306/R5311/R5474/R5475 _CX12B900000	3A	3B
		73. 20111121 page16 L2 change P/N to CX12B900000.	3A	3B
		74. 20111121 page06 add R95 for G48 ball to GND for sandy bridge.	3A	3B
		75. 20111121 page03 add Q31 and R182 to 1k/R185 10K.	3A	3B
		76. 20111121 page20 change CN8 footprint and update CN9 footprint.	3A	3B
		77. 20111121 page23 modify all hole footprint.	3A	3B
		78. 20111122 page19 Swap USB3 pin define for layout.	3A	3B
		79. 20111122 page20 modify CN8/cn17 pin define, cn17 pin29/30 for TP.	3A	3B
		80. 20111122 Update footprint PJ9002.	3A	3B
		81. 20111122 page35 add a jump JP8000 at 1.05V.	3A	3B
		82. 20111122 Q37 change to P mose and remove Q44 change power plant to +3V_S5.		
		83. 20111122 page16 L97 Change inductor to 1A for FAE request.		
		83. 20111122 page08 add net TP_INT# pin at CN17 pin29 to PCH N32 and add Q5005 and R444 for leakage issue..		
		84. 20111123 page20 CN8 add LPCPD# net to PCH G8.		
		85. 20111123 change PJ9002 pin define.		
		86. 20111123 update Hole3/4/10 footprint.		
		87. 20111123 page30 PL3002/PL3001 change footprint to 4pin.		
		88. 20111123 page32 Del PL9004/PL9005.		
		89. 20111123 page23 modify Keyboard Pin define for match matrix.		
		90. 20111124 midfy CN5868/CN5807 USB footprint.		
		91. 20111124 page09 modify RAM_ID from GPIO40-42,GPIO69 change to GPIO42,9,10,14.		
		92. 20111124 page14 DDRIII on board RAM change to 256x16.		
		93. 20111125 Update Cn11/JEDEC/R245 footprint.		
		94. 20111125 Update KB pin define.		
		95. 20111128 Update CN5910/CN2/U12-U35 footprint.		
		96. 20111128 page28 change Q5644 to dual mose and del Q5042, GPIO12 ACIN high DC low prevent backdriver add mose. add PU +3V resistor R5305/R5308 reserve.		
		97. 20111128 page08 change net TP_INT# to pin E12 GPIO11 and net name to SMBALERTL. add R444 10K to PCH_ODD_EN not use.		
		98. 20111128 page19 add R221/C5498 for EMI request and change Cn8 pin8 to LPC_LFRAME#,Pin10,pin12 to GND,Pin11 PCLK_TPM.		
		99. 20111129 page29 change Q5043 to singal mose and add back Q5045, VGA_OVT# connect to SYS_SHDN# un-stuff, GPU_ALERT# to EC GPU_THAL, DGPO_OPP# to VGA_ACIN.		
		100. 20111129 page22 Remove BKT1 and add hole14-16.		
		101. 20111129 page03 change U5013.3 net to PCI_PLTRST#.		
		102. 20111129 page09 change U5901 power plant to +3V.		
		103. 20111129 page21 change path cap power well and del C497/C764/C473/C508.		
		104. 20111129 page28 add R27 0ohm at net GPU_SPRSLPWR.		
		105. 20111129 page31remove R5068 because double connect GND.		
		106. 20111129 page24 add R437-R439 SPI series resistor,and SPI net contact to SPI 4M ROM.		
		107. 20111130 page22 add hole18.		
		108. 20111130 page18 CN5910 add two GND pin15/16.		
		109. 20111130 page09 change PCIE_CLKREQ0# PU +3V_S5, PCIE_CLKREQ2# PU +3V.		
		109. 20111201 page17 change C5108 power from +3V_S5 to +3V_LAN.		
		110. 20111201 page19 update CN8 footprint.		
		111. 20111201 Power Update : a.PL3001 and PL3002 change to 0.24uH inductor. b.PR3019 and PR3040 change to 20.14kohm. c.PR3021 and PR3040 change to 29.65kohm. d.PR3023 and PR3053 change to 75.49kohm. e.PC3013 and PC3030 change to 15nF. f.Change PR3049 to 312.5kohm. g.Change PR3055 to 2.74kohm. h.Change PC3014 to 1200PF. i.Change PC3015 to 1200PF. j.Change PC3015 to 68PF. k.change PR3011 to 200ohm. l.Change PR1007 to 13.07kohm. m.Change PR1015 to 23.02kohm. n.Change PR1022 to 300ohm o.Change PR1013 to 261.8kohm. p.Add PR1006 for default test mode.		
		112. 20111202 Hole18 change footprint to NG-C25ED118P2-V3		
		113. 20111202 page03 ADD NET DEEPS3_EC .connect to Q15 , Q5050.		
		114. 20111202 page33 Del PC1004/PC1005 for Power request.		
		115. 20111205 page19 Change CN8 pin define and add 0ohm R222 on net SERIRQ.		
		116. 20111205 page33 add back PC1004.		
		117. 20111206 page38 PR3034 and CPC3032 change to AGND, PR3041 change to DGND.		
		118. 20111206 page07 add R5192 un-stuff for normal s3 PCIE LAN wake up.		
		119. 20111207 page33 remove PR1001/PR1004/ PR1043/PR1044 0ohm		
		120. 20111207 page21 Modify CN12 Pin define following up ZHA.		
		121. 20111207 page20 CN3 Pin31 to GND.		
		122. 20111207 page20 change CN13 Pin5/U5006.11 net name BT_POWERON# to BT_POWERON.		
		123. 20111207 page38 swap PR3042 and PR3041.		
		124. 20111207 page08 Change Y5000 footprint.		
		125. 20111207 page22 modify hole8 footprint and add net BATT_EN at Pin2.		
		126. 20111207 page22 modify hole8 footprint and change net BATT_EN to Pin3.		
1B		1. 20120104 page11 VCCSSW3_3 change power plant to +3VPCU.		
		2. 20120104 page07 Change GPU#EOK from RERESET# to EC.		
		3. 20120109 page08 change Q33 footprint.		
		4. 20120105 page11 +3V_VCCM_SPI change to +3V_S5 and reserve +3V.		
		5. 20120105 page28 Q14/Q9 change transistor direct and power plant to +3V_S5.		
		6. 20120111 page15 Change C407 to 50V CAP and un-stuff C410 and change C406 to 50V 0805 size.		
		7. 20120112 page04 Add C753-C758 1uf CAP on +0.75V_DDR_VTT.		
		8. 20120113 page22 Change KB con footprint.		
		9. 20120113 page28 Change Q15.2 to GPU_TRIP# EC.		
		10. 20120113 page28 Change GPU Strap1 PD4.99k,strap4 PD 45.3k.		
		11. 20120113 page31 stuff PR256 for Battery enable, change PQ50 to dual mose of ACIN to EC and PCH acpresent# pin.		
		12. 20120117 Update EMI CAP.		
		13. 20120117 page24 Add net WLAN_OFF for IOAC on U36.81 to CN5.64.		
		12. 20120117 page36 PR146 change to 365ohm,un-stuff PR36,stuff PR43,stuff PR145, PU7 change to TPS51463.		
		13. 20120118 page22 Change CN12 footprint.		
		14. 20120118 page22 Add u37 for ICT test use.		
		15. 20120119 page24 Add Q46 to EC U30.114.		
		16. 20120119 Unstuff PR260 and stuff R346 .		
		17. 20120119 move R358 to near Q38 and del net DRAMRST_CNTRL_PCH,and EC_DRAMRST_CNTRL and R616.		
		18. 20120119 Change PR266 from 100k to 10k .		
		19. 20120120 Remove C644/C621/C622.		
		20. 20120120 Page 24 change R640/R61 power plant to +3V_S5.		
		21. 20120120 unstuff R573 and stuff R574 for DS3 function.		
1C		1. 20120214 Page17Add c613 and c614 for LAN power noise.		
		2. 20120214 Page07 Add R642 between SUSWARN to SUSACK.		
		3. 20120216 Page24 Add 1R5T Gate and change 100pin SUSWRAN# to IOAC_PCIERST#.		
		4. 20120216 Page20 CN5 pin22 reserve IOAC_PCIERST# solution.		
		5. 20120217 Page28 un-stuff R547/R548, stuff Q35,un-stuff R383/R435, stuff Q26/Q25,add PU 10k +3V GPU_THAL# and GPU_TRIP#. R543/R548 PU from+3V to +3VPCU, for S5 current reduce.		
		6. 20120217 Page38 change PR77/PR81 to 27k,PR105/PR106 to 75k,PR76/PR80 to 30k		
		7. 20120217 change 0ohm to short pad.		
		8. 20120220 page 31 remove VA2 plant and PC205/PC202 PR124, move PD3 between PQ3 and PR10 for S5 current reduce.		
		9. 20120220 change PQ11, PQ2, PQ6, PQ10, PQ13, PQ5, PQ9, PQ49, PQ51 footprint to WDFN5-3_05X3_05-G5.		
		10. 20120220 page7 Change net suswarn# to suswarn#_0 PU.		
		11. 20120220 page36 PR145 un-stuff,PR145 change to 100,PR43 un-stuff, PR36 short pad.		
		12. 20120220 page24 add U36.105 GPIO KB_BL_EN pin to CN13.23.		
		13. 20120220 page20 Change CN6 footprint		
		14. 20120221 page28 R527/R516 change power plant to +3V.		
		15. 20120221 page08 Change R620/R534 to 47K and stuff R620, R524 un-stuff		
		16. 20120221 page20 Add R659 for 1R5T selection.		
		17. 20120221 page15 CN7 pin33/34 connect to GND.		
		18. 20120222 page38 Unstuff PR219/PC137/PR288PC151.		
		19. 20120222 page38 Unstuff PR195/PC125/PR201/PC126.		
		20. 20120222 page15 del R295/R315.		
		21. 20120222 page14 Change Footprint U30/31/32/35.		
		22. 20120223 page15 Change Footprint L22.		
		23. 20120223 page08 Change JTAG TDI fore CPU TDO, TCK and TMS form U37 and CPU .		
		24. 20120223 page28 add dGPU_OPP# PU reserve R651.		
		25. 20120223 page28 add JTAG_TDO PU reserve R299.		
2C		1. 20120302 page10 add CN13.30 net to BIOARD_ID4.		
		2. 20120305 page07 R397 from short pad to RC0402 footprint.		
		3. 20120322 page23 Remove RP1/RP2/RP3/RP4/L18/L19		
		4. 20120322 page31&37 , delete PR120 & PR121.		
		5. 20120322 page32 Reserve PC196 for PU1_PIN13		
		6. 20120322 page15 delete L1		
		7. 20120322 page24&31 Add NET<SB_ACDC> , add R653,Unstuff PR266 & R652 Wait for EC confirm by the result.		
		8. 20120328 page32 Remove PC196		
		9. 20120328 page35 Reserve PC202		
		10. 20120328 page34 Reserve PC205		
		11. 20120328 page38 Reserve PC206 , PC207		
		12. 20120328 page3 R204,R605 CS12002FB00 change to CS12002FB25		
		13. 20120328 page22 HOLE14 follow Hole11		
		14. 20120329 page22 HOLE11,HOLE14 footprint change to H-TE256X256I118BC256D118P2		
		14. 20120330 page23 R280/R281/R282/R283/R276/R277/R278/R279 change back to 0 ohm resistor.		
		15. 20120330 page31 PC196 add		
		15. 20120405 page23 R276,R277,R278,R279,R280,R281,R282,R283 change to 15 ohm		

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