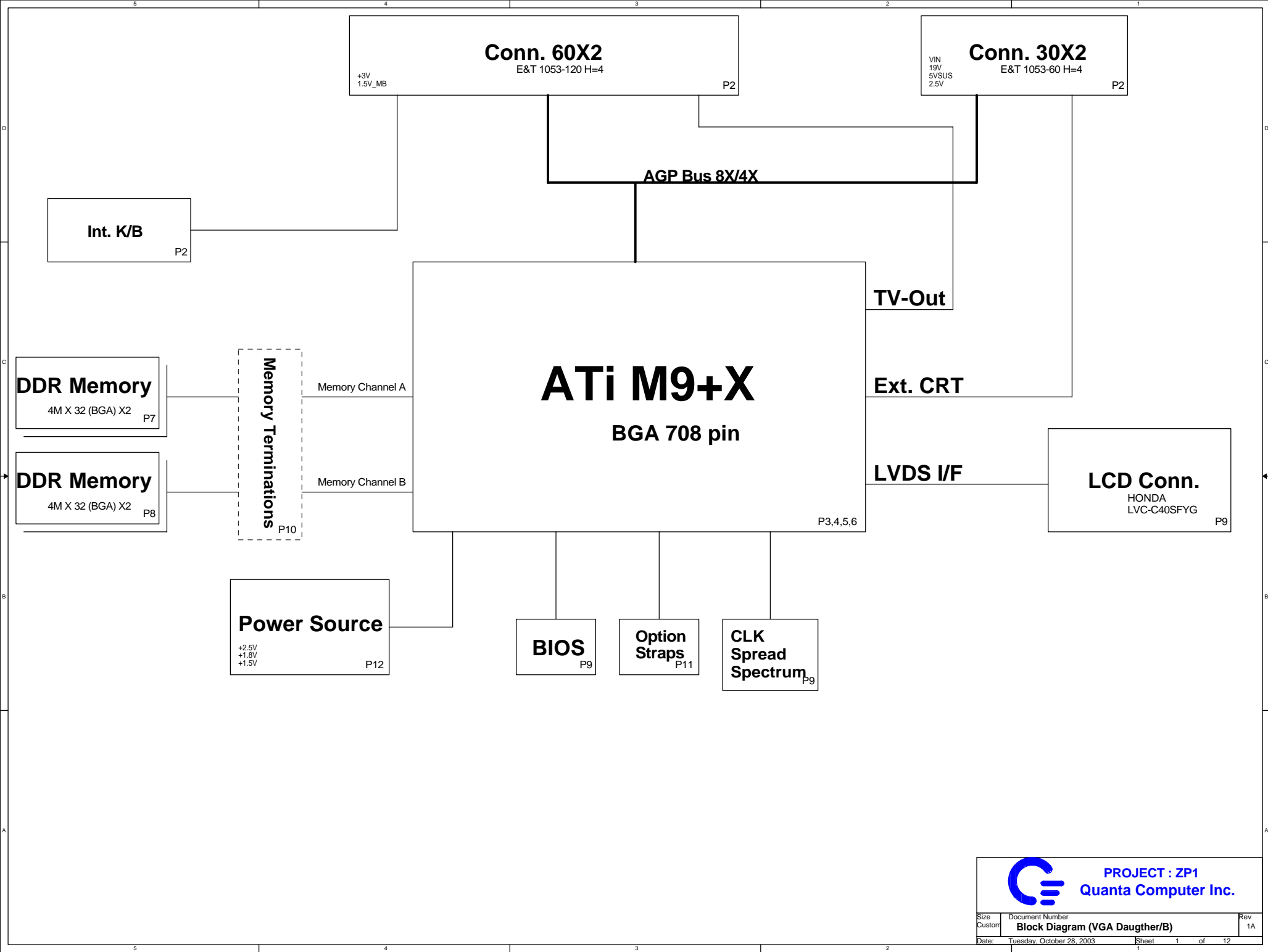
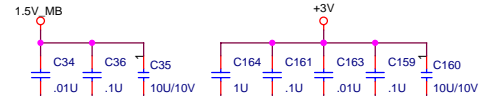
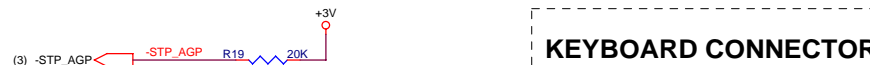
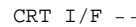
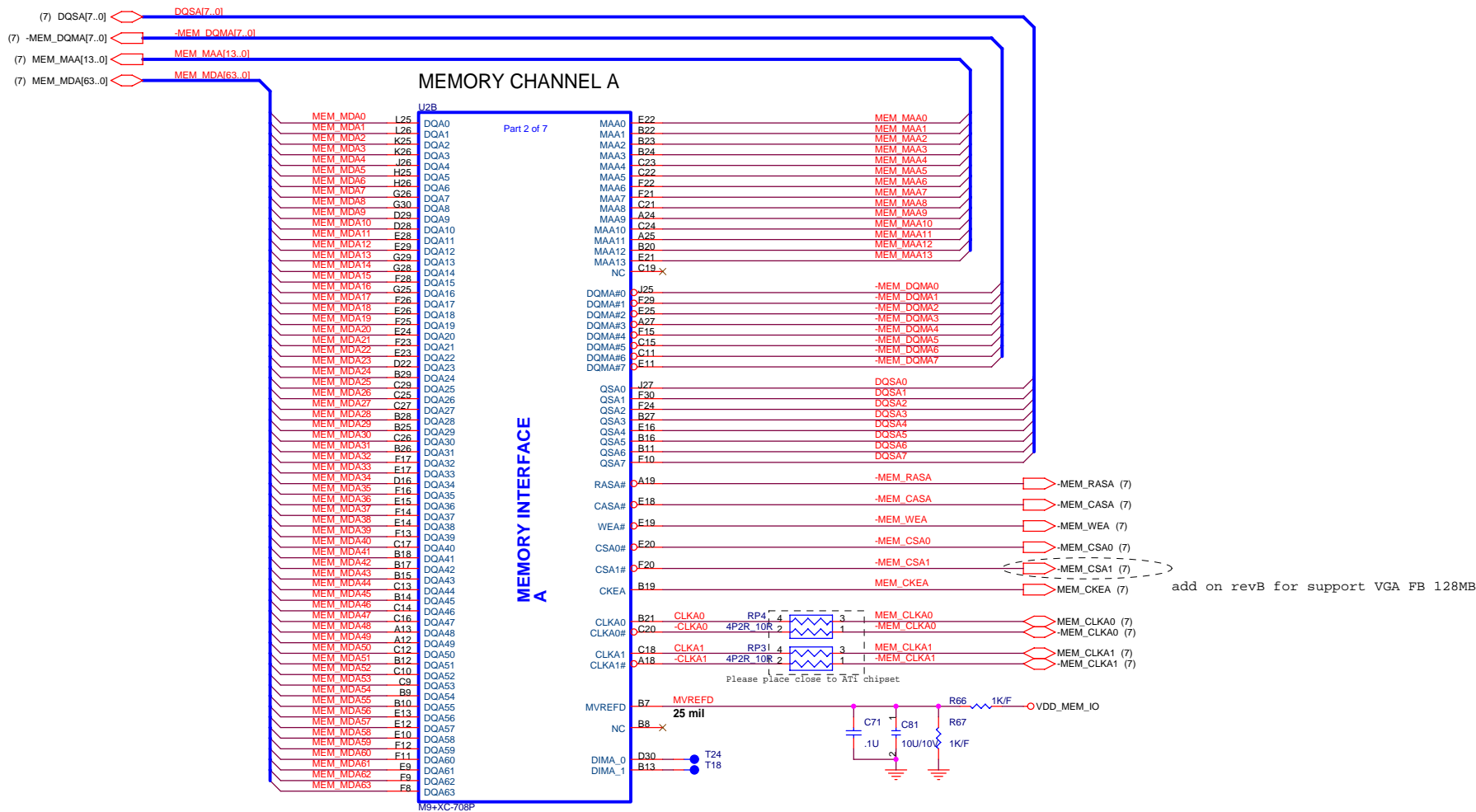


MODEL	REV	CHANGE LIST				Model	ZP1 VGA BOARD	
						Page	FM	TO
ZP1 VGA BOARD	1A	First Release				1	1A	
	2A	Reference ECN E200305-1522				2	2A	
	3A	Reference ECN E200307-1199				3	3B	
	3B	Reference ECN E200307-3020				4	2A	
	3C	Reference ECN E200309-0293				5	2A	
						6	2A	
						7	2A	3C
						8	2A	3C
						9	1A	
						10	1A	
						11	1A	
						12	1A	3C
PROJECT : ZP1		PCBA NO.35ZP1VB0007		REV:3C		DOC. NO: 204		
APPROVED BY : Jason Liu		CHECK BY: Jason Liu		DRAWING BY: Kent Chen		DATE :08/22/2003		SHEET 1

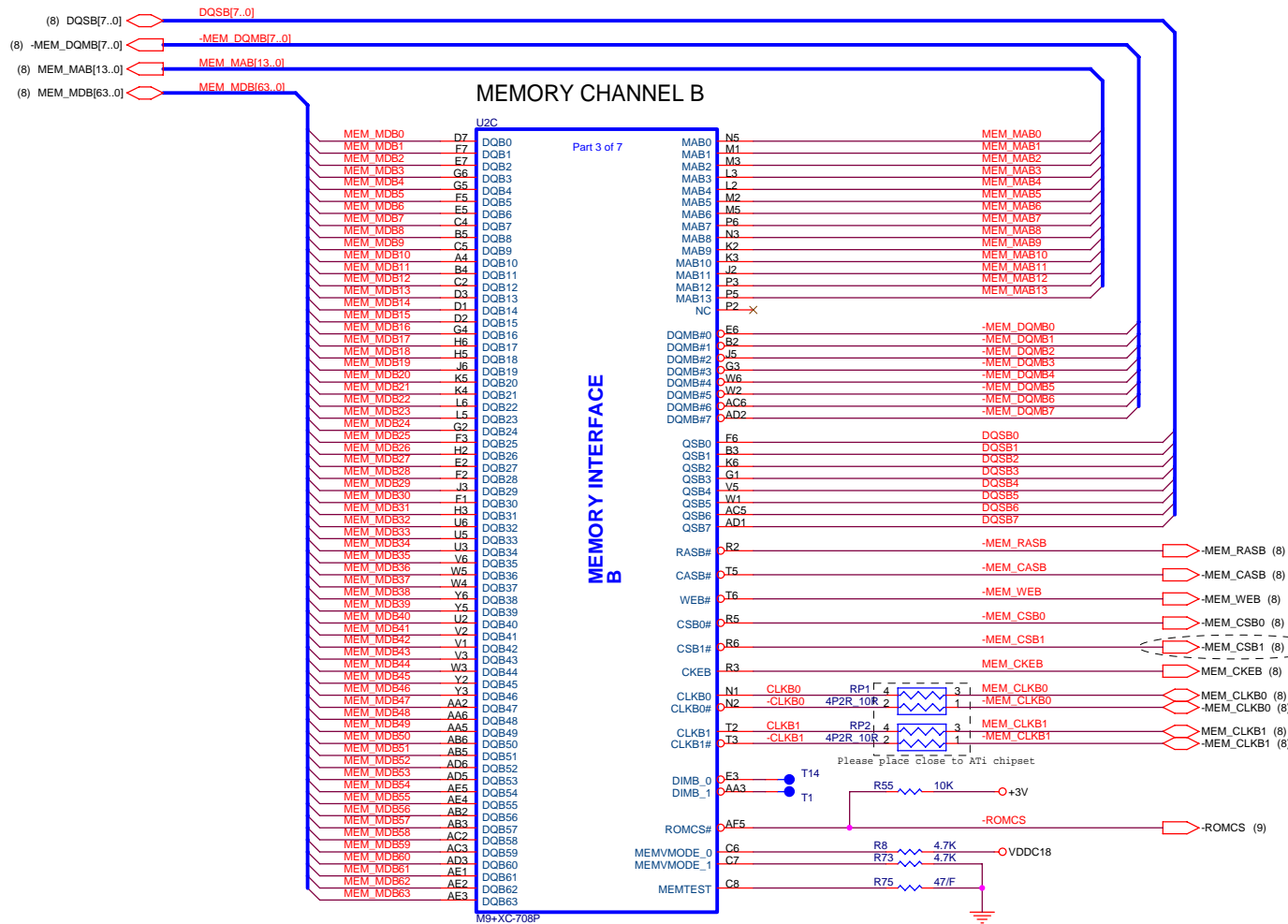






PROJECT : ZP1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	M9+X Memory Bus A	2A
Date:	Tuesday, October 28, 2003	Sheet 4 of 12

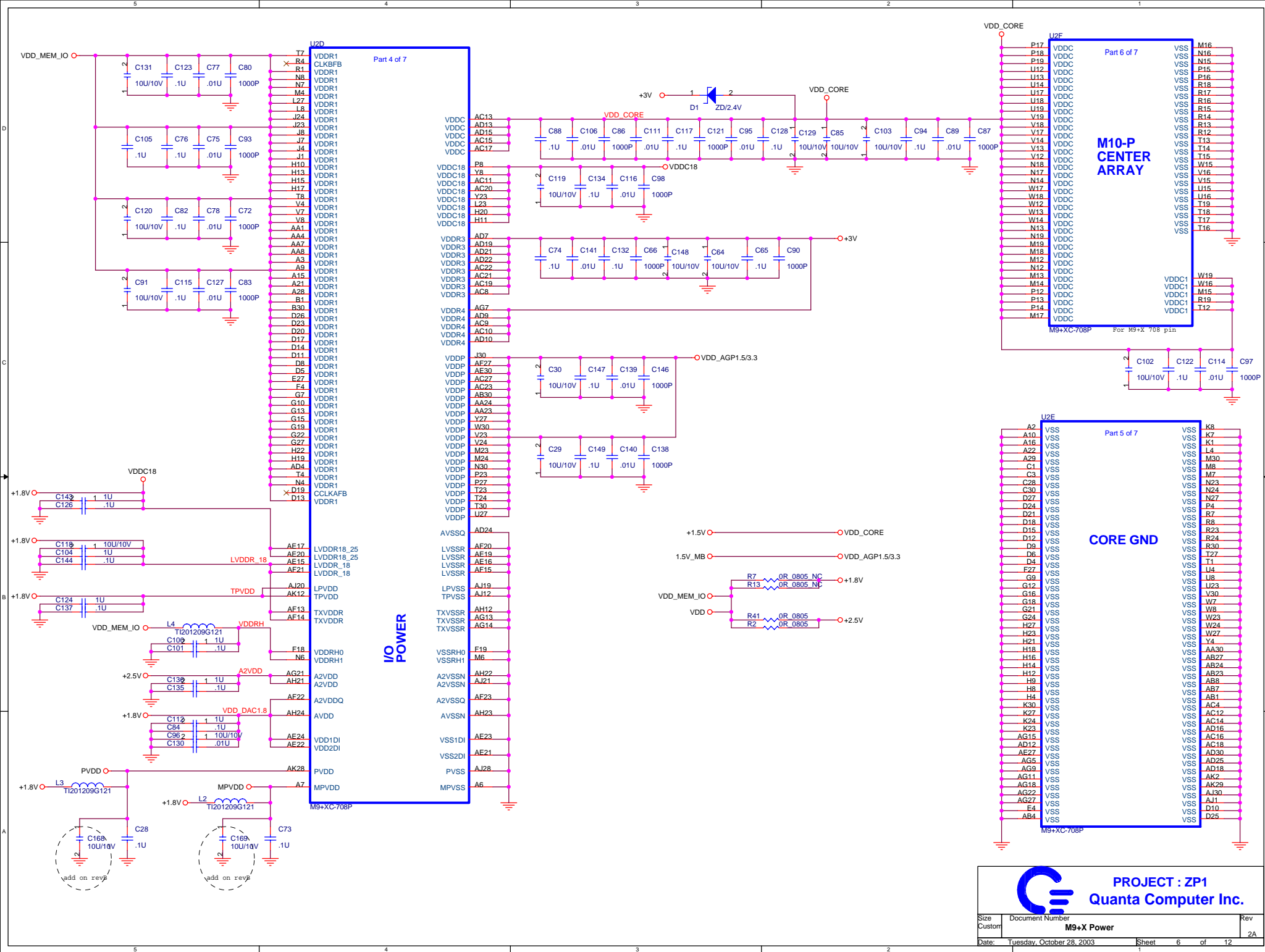


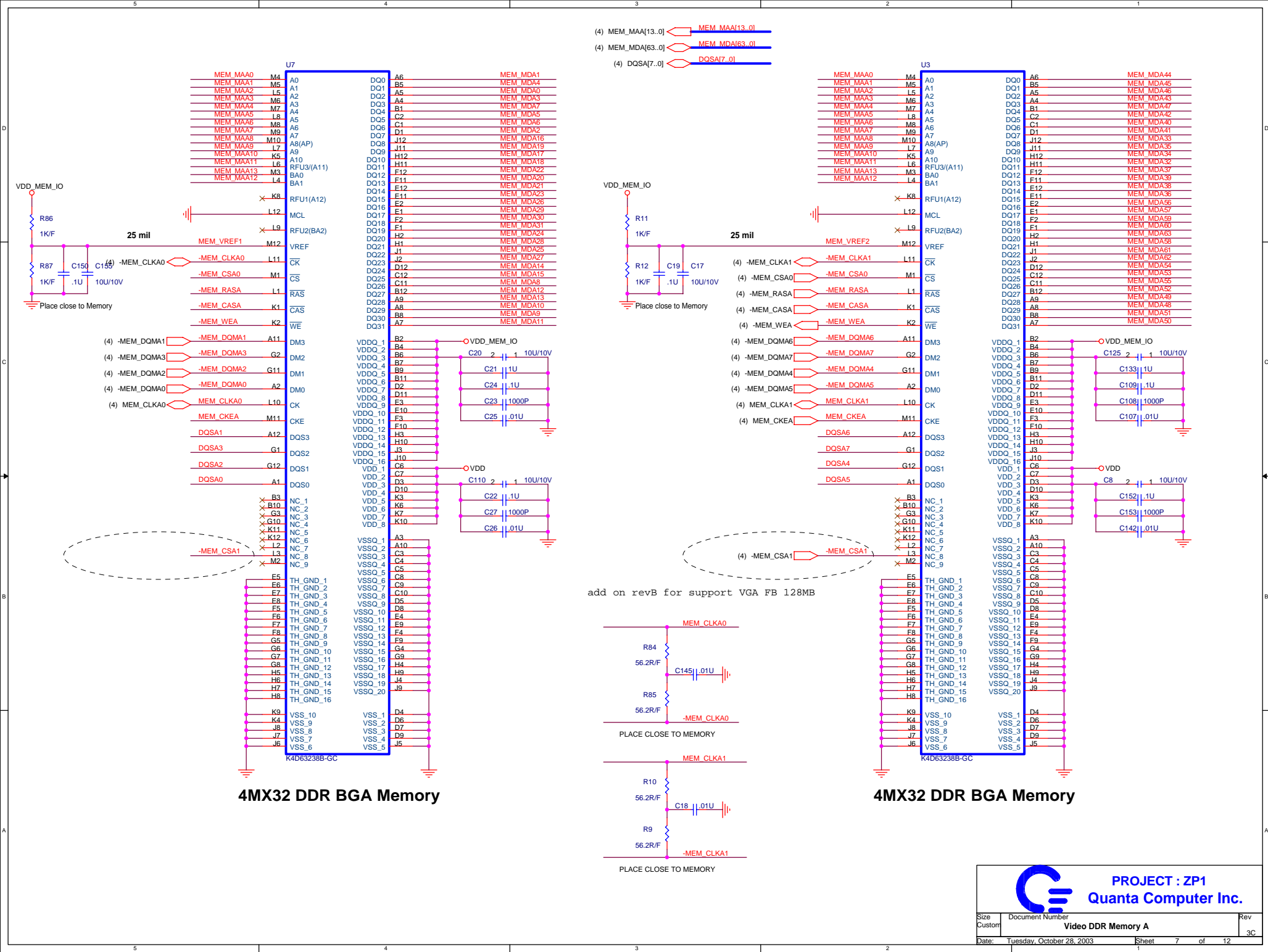
MEMV0[1:0]	MEMORY IO VOLTAGE
0 1	2.5V (DDR)
1 0	1.8V (DDR)
1 1	3.3V (SDR)

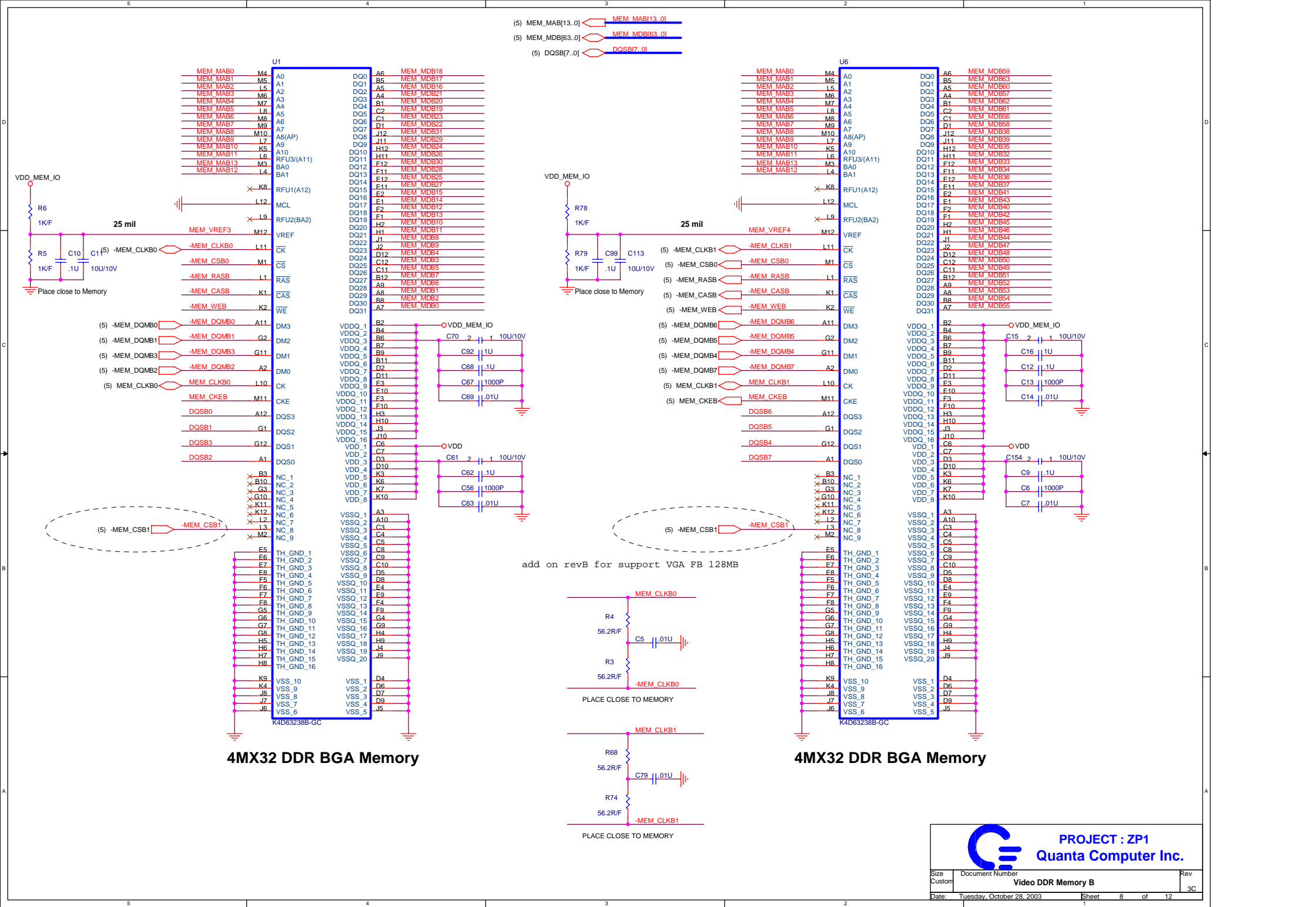


PROJECT : ZP1
Quanta Computer Inc.

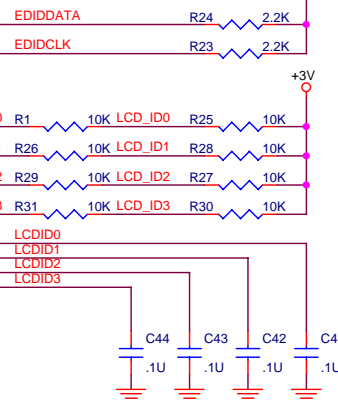
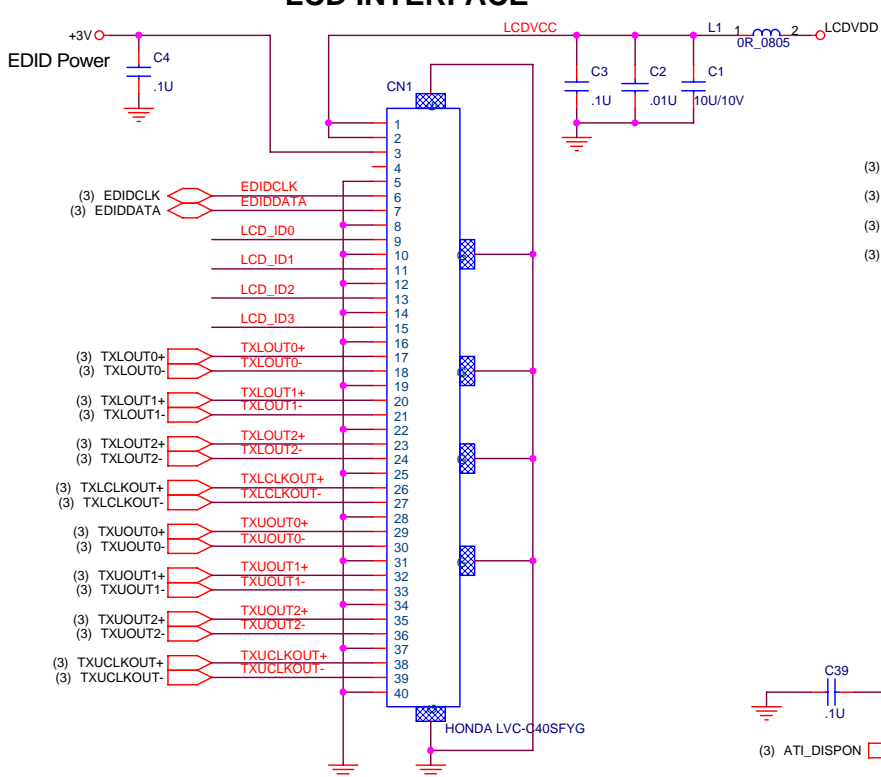
Size	Document Number	Rev
Custom	M9+X Memory Bus B	2A
Date:	Tuesday, October 28, 2003	Sheet 5 of 12



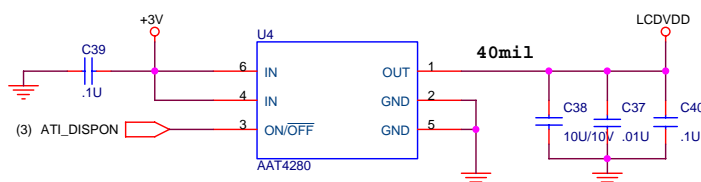




LCD INTERFACE

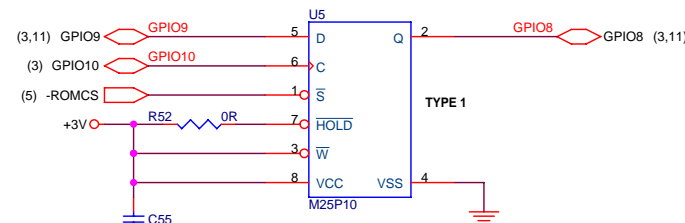


PANEL VCC CONTROL

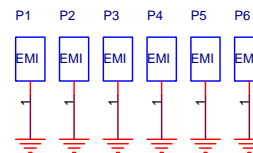
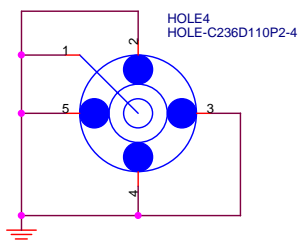
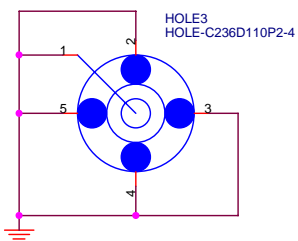
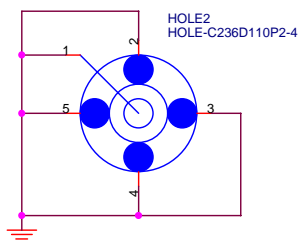


*** NOTE: THIS BIOS PAGE IS NOT APPLICABLE TO MOTHERBOARD DESIGNS
SO IF NO ROMS ARE USED, LEAVE ROMCS# AS NO CONNECT

Video BIOS



SERIAL EEPROM BIOS



EMIPAD118X177 * 19



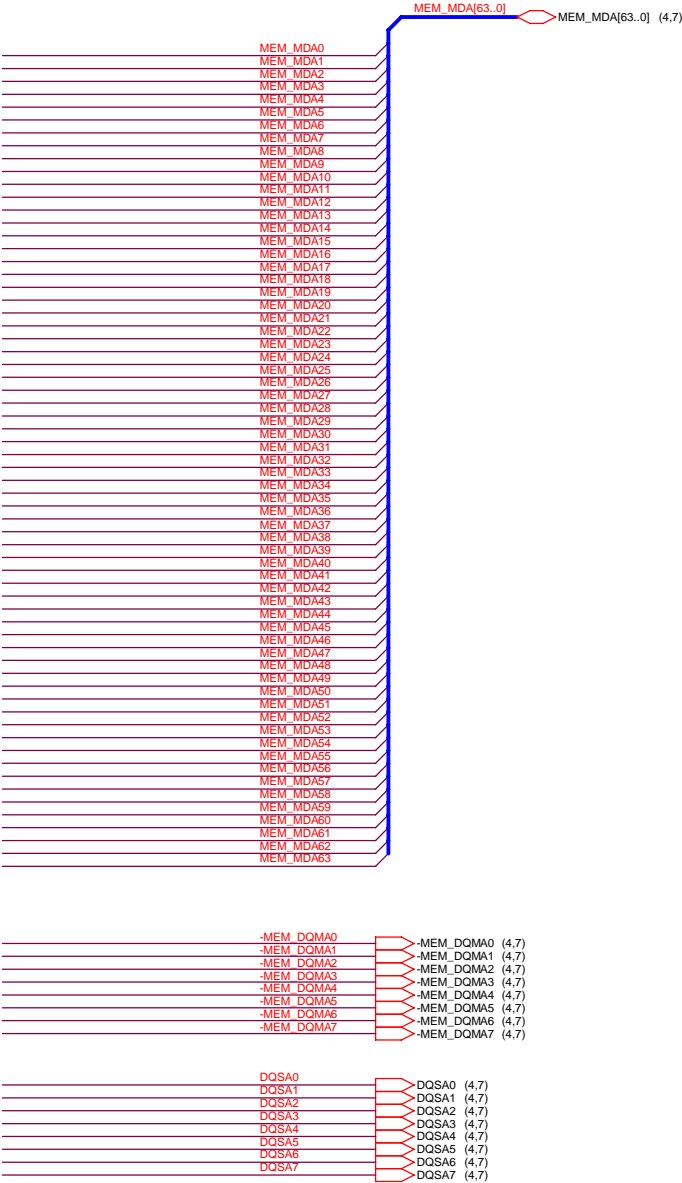
PROJECT : ZP1
Quanta Computer Inc.

Size B	Document Number	Rev 1A
Date: Tuesday, October 28, 2003	Sheet 9 of 12	

TERMINATION FOR MEMORY

CHANNEL A

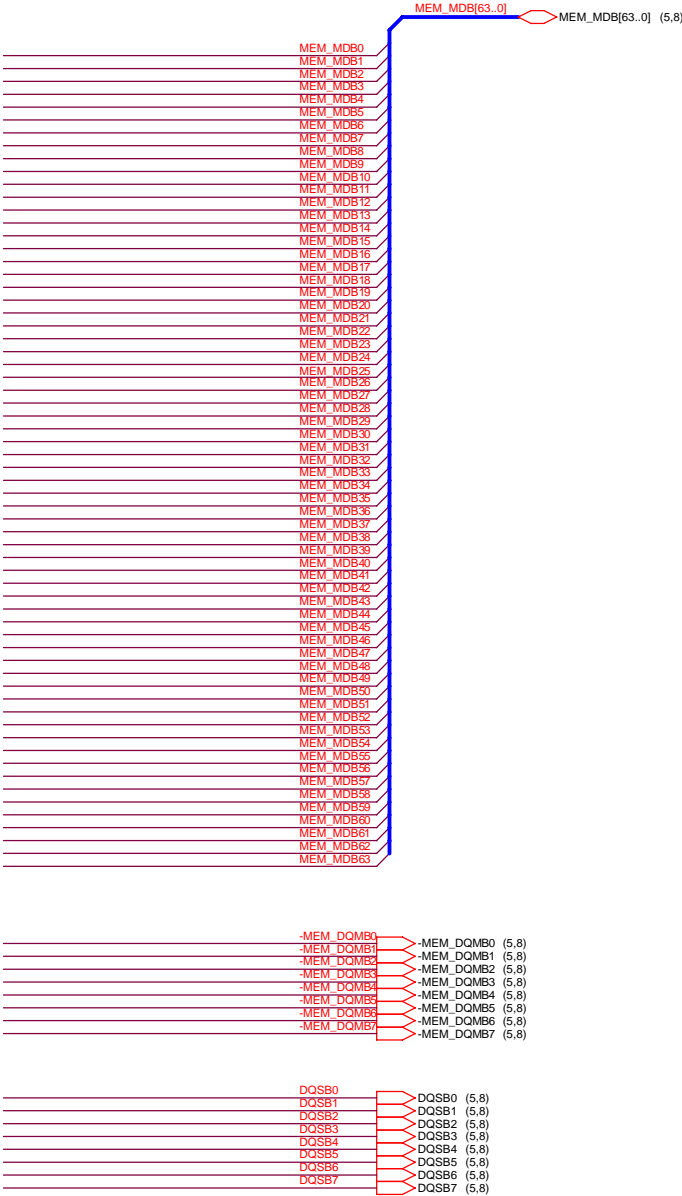
PARALLEL TERMINATION
PLACE CLOSE TO MEMORIES



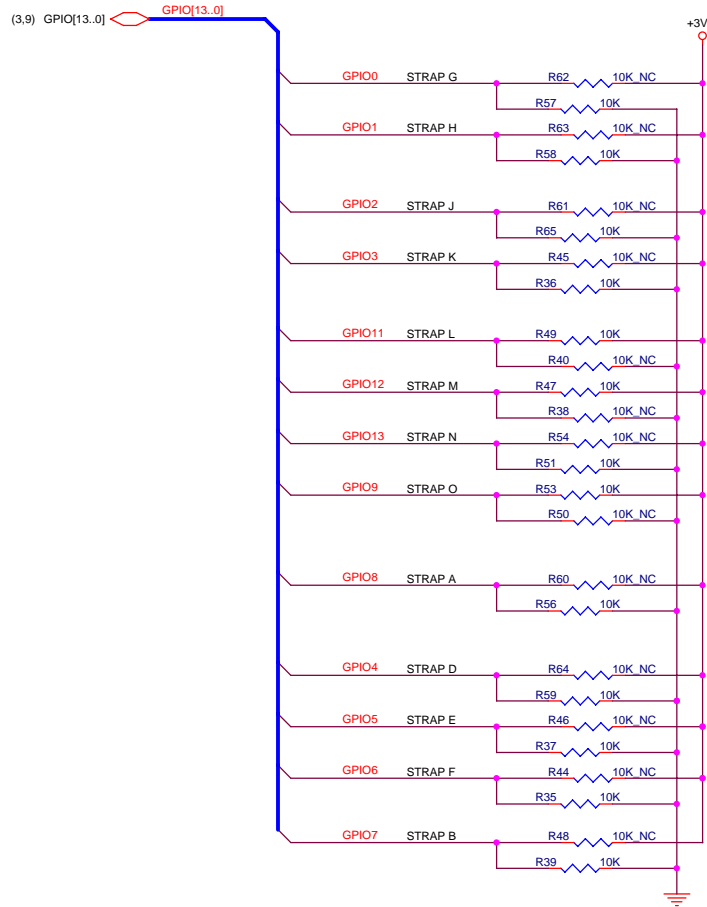
TERMINATION FOR MEMORY

CHANNEL B

PARALLEL TERMINATION
PLACE CLOSE TO MEMORIES



OPTION STRAPS



STRAP H	STRAP G	AGP1X CLOCK FEEDBACK PHASE ADJUSTMENT WRT REFCLK (CPUCLK)	
LOW	LOW	(DEFAULT)	SEE PINOUT SPEC FOR OPTION SETTINGS

STRAP K	STRAP J	AGP CLOCK PHASE ADJUSTMENT BETWEEN X1 AND X2 CLOCK	
LOW	LOW	(DEFAULT)	SEE PINOUT SPEC FOR OPTION SETTINGS

STRAP O	STRAP N	STRAP M	STRAP L	ROM IDENTIFIER
HIGH	LOW	HIGH	HIGH	(DEFAULT) SEE PINOUT SPEC FOR OPTION SETTINGS

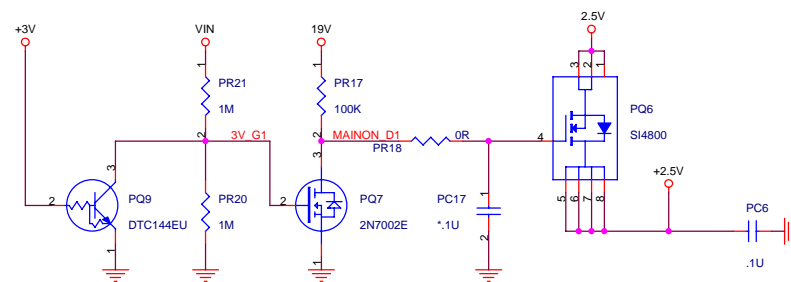
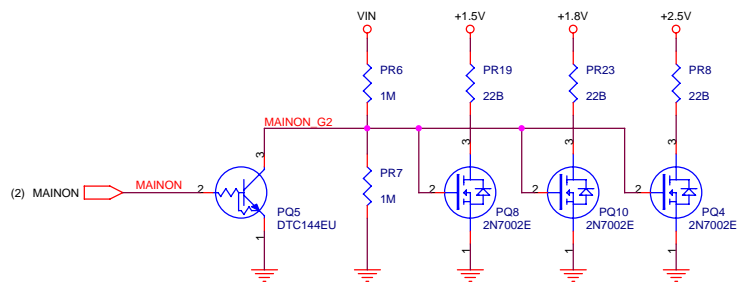
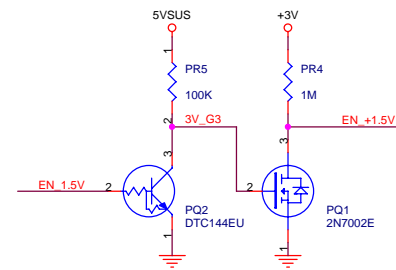
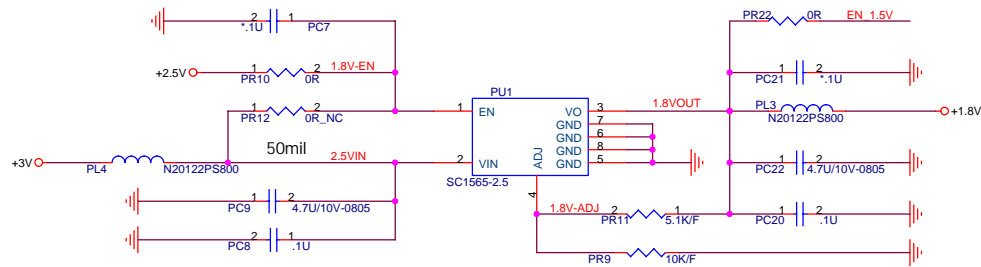
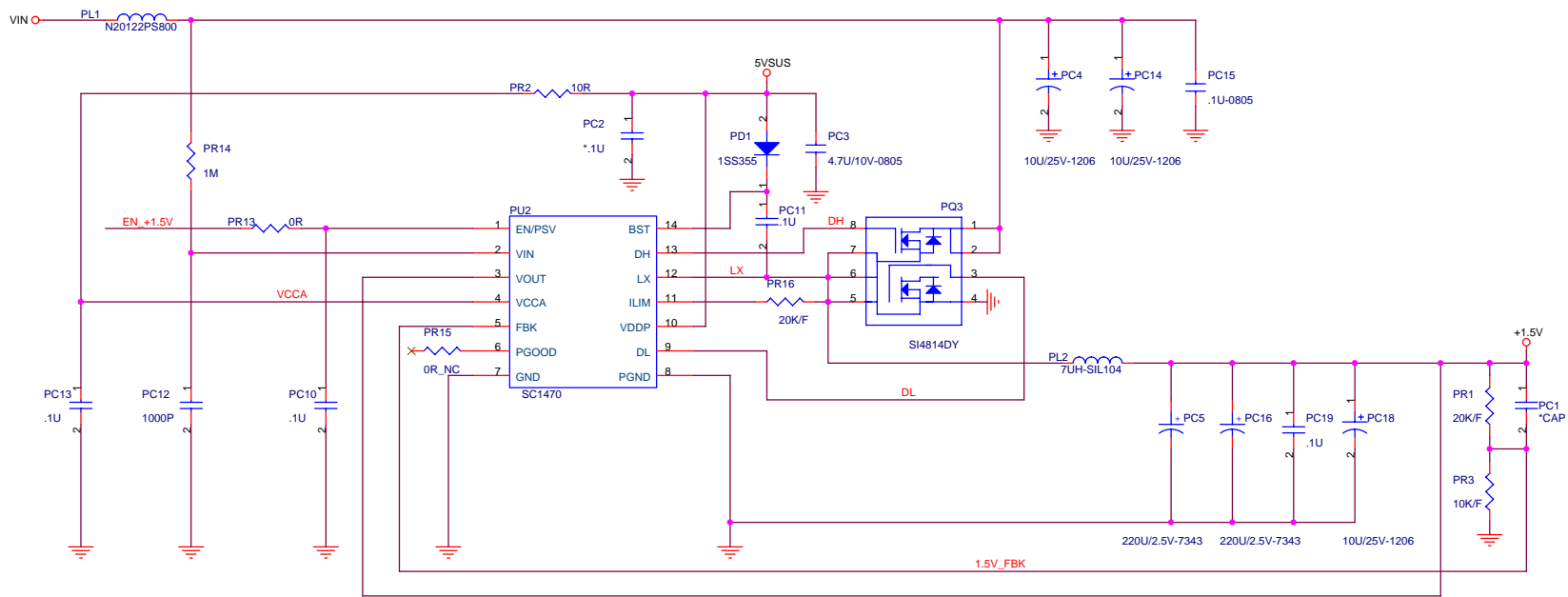
STRAP A	ID DISABLE
LOW	NORMAL OPERATION (DEFAULT)
HIGH	SHUT DOWN

STRAP D	STRAP E	STRAP F	BUS_TYPE
LOW	LOW	LOW	(DEFAULT) SEE PIN BASED STRAPS IN PINOUT SPEC

STRAP B	VGA
LOW	ENABLE (DEFAULT)
HIGH	DISABLE

NOTE: THE M7 SUPPORTS THE USE OF STRAP RESISTORS (AS AN ALTERNATIVE TO CUSTOMIZED BIOS) TO CONFIGURE CERTAIN ASPECTS OF THE GRAPHICS SUBSYSTEM. THE USE OF EXTERNAL STRAPS PROVIDES ADDED FLEXIBILITY AND EASE OF FUTURE UPGRADE. STRAPPED VALUES ARE LOADED INTO INTERNAL REGISTERS ON THE FIRST PCI COMMAND AFTER RESET# IS INACTIVE.

NOTE:
THE I/O BUFFERS USE INTERNAL PULLDOWN RESISTOR. THIS DICTATES THE FOLLOWING STRAP CONFIGURATION:
STRAP TO VCC VIA 10K RESISTOR.
THIS PROVIDES THE LOGIC LEVELS SHOWN:
'0' WHEN 10K RESISTOR NOT INSTALLED
'1' WHEN 10K RESISTOR INSTALLED.



PROJECT : ZP1
Quanta Computer Inc.