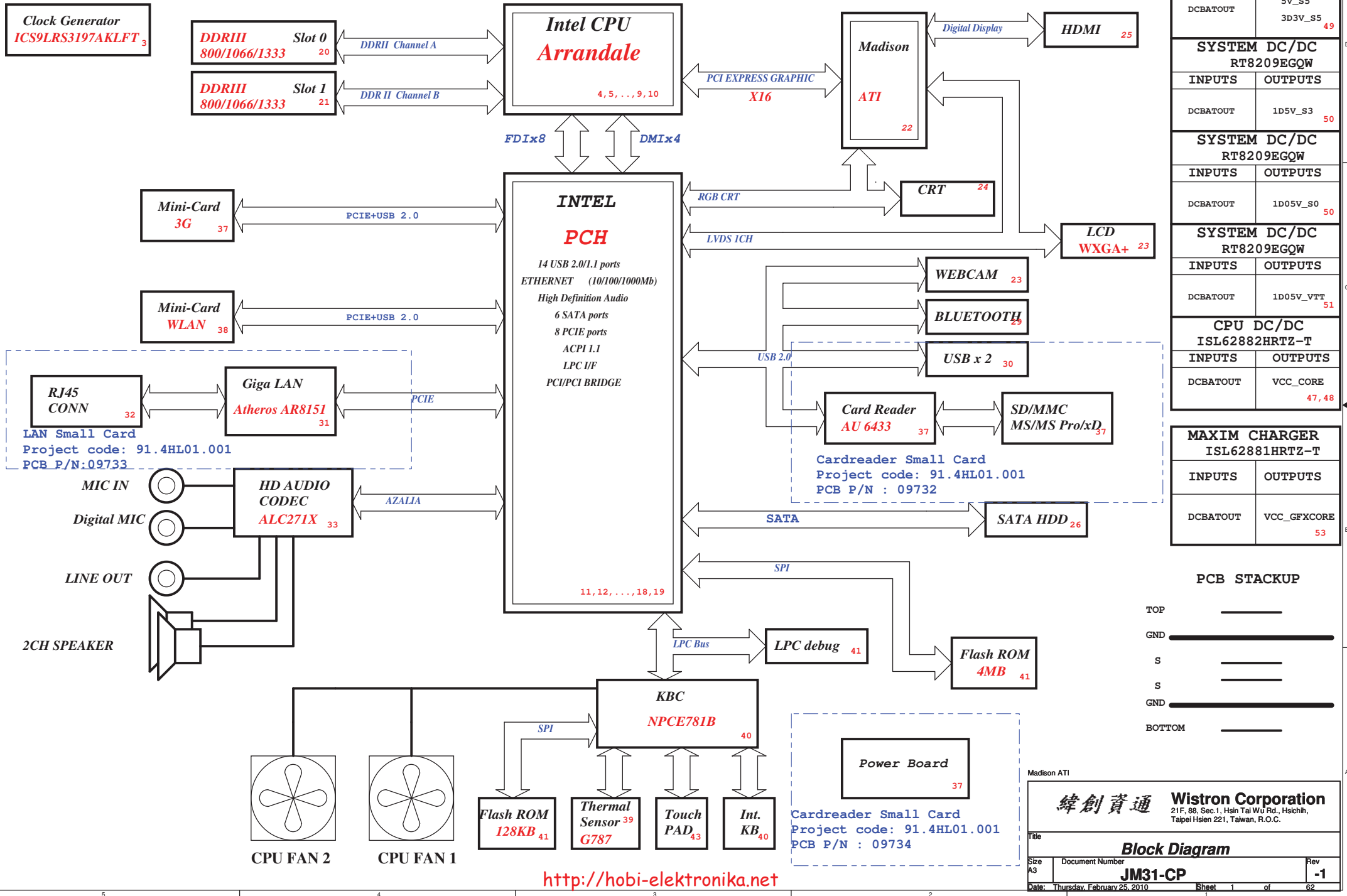


JM31-CP Block Diagram

Project code: 91.4HL01.001

PCB P/N : 48.4HL01.031

REVISION : 09921-3



PCH Strapping

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	Default - Internal pull-up. Low (0)= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIE Routing

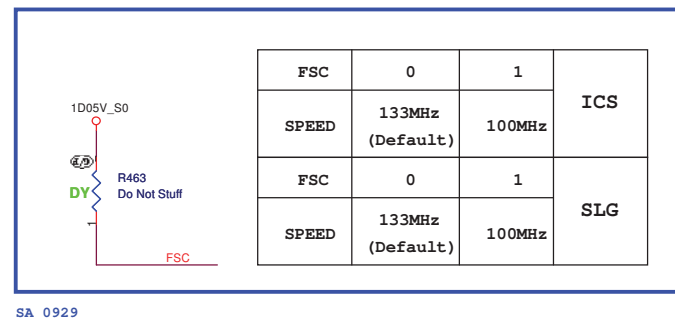
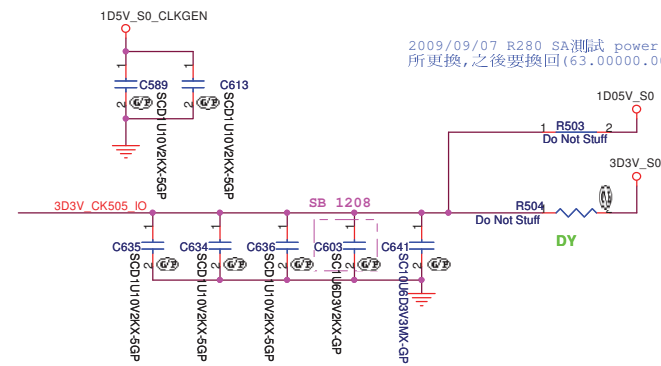
LANE1	LAN
LANE2	MiniCard1
LANE3	MiniCard2

USB Table

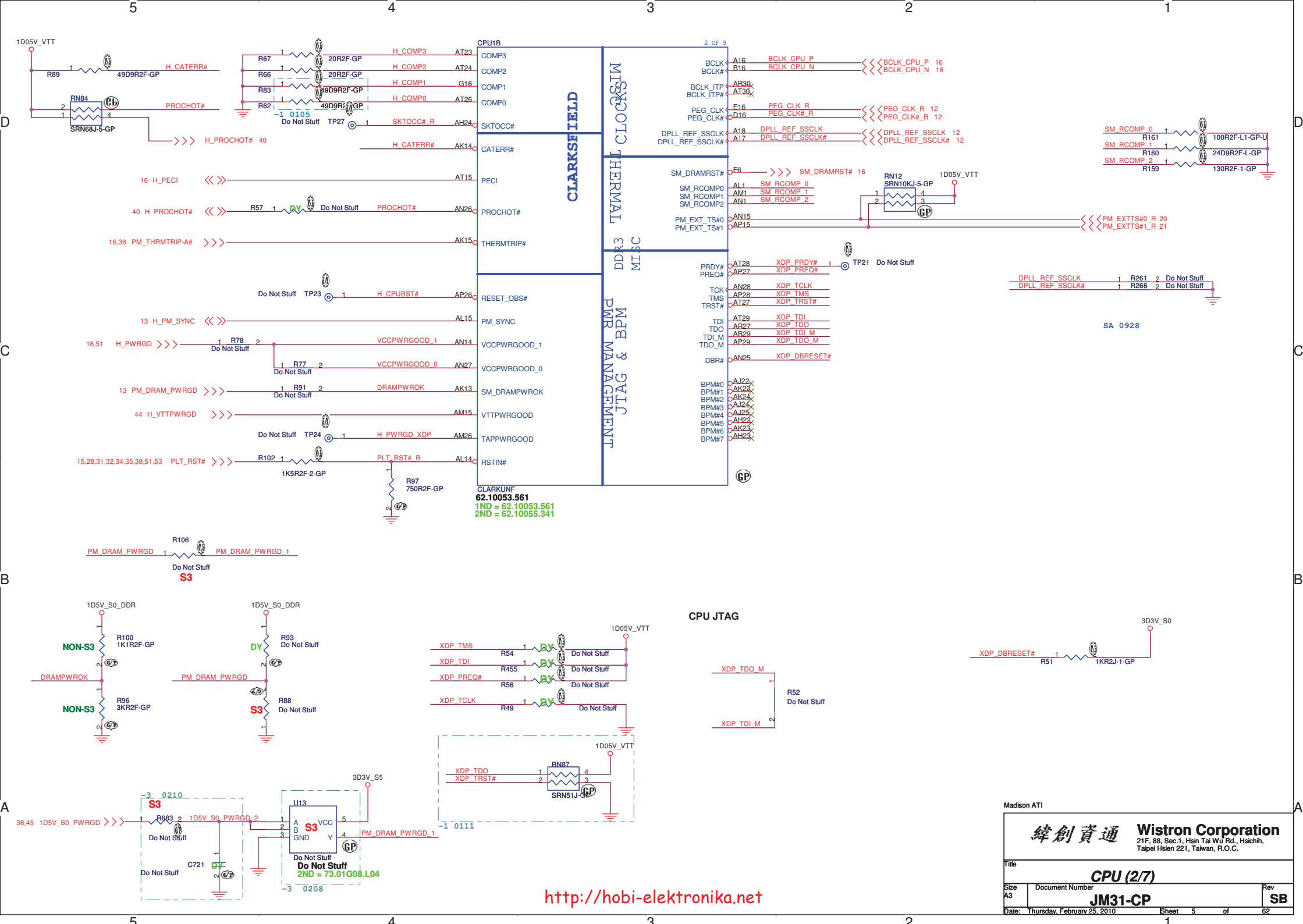
Pair	Device
0	USB1
1	USB2
2	USB4
3	MINICARD2
4	WECAM
5	Blue Tooth
6	MINIC1
7	Cardreader
8	NC
9	NC
10	NC
11	NC
12	NC
13	NC

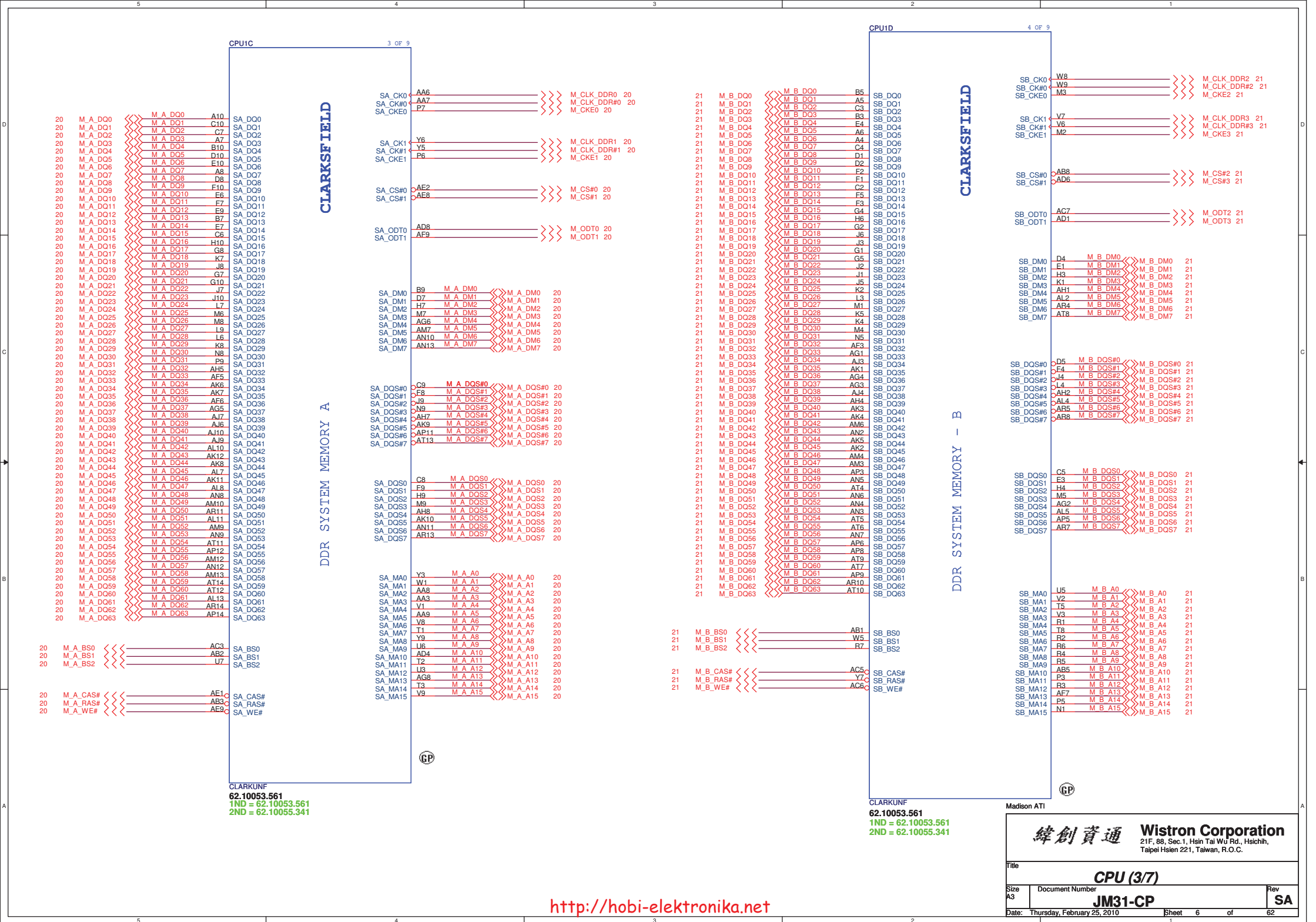
Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0



FSC	0	1	ICS
SPEED	133MHz (Default)	100MHz	
FSC	0	1	SLG
SPEED	133MHz (Default)	100MHz	





VCC_CORE

PROCESSOR CORE POWER

48A

VCC_CORE

CPU1F

6 OF 9

CLARKSFIELD

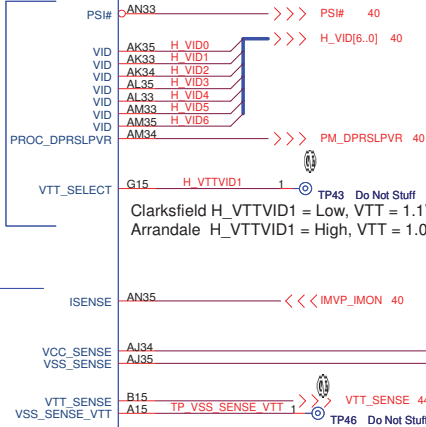
1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE



CLARKUNF

62.10053.561

1ND = 62.10053.561

2ND = 62.10055.341

<http://hobi-elektronika.net>

1D05V_VTT

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

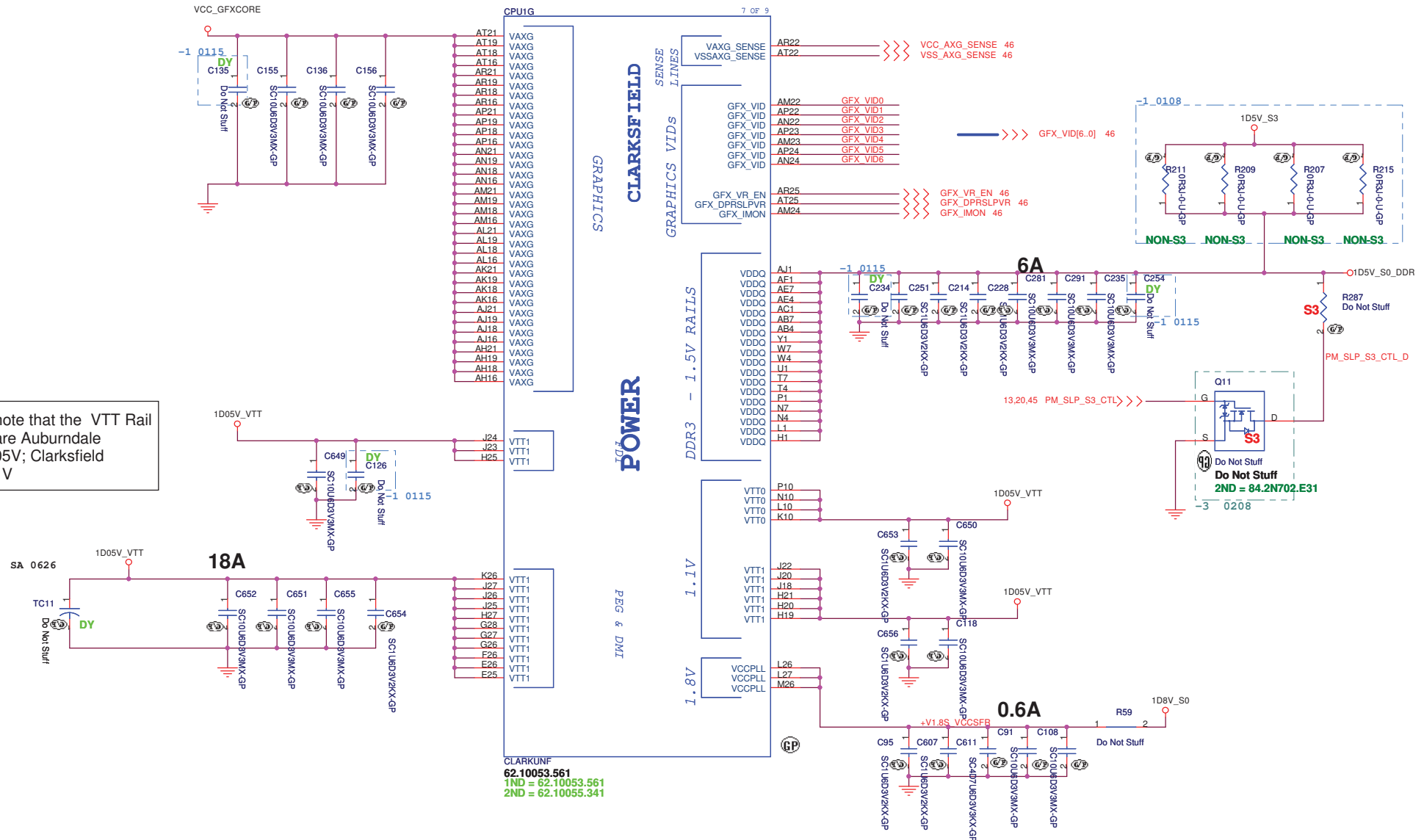
Please note that the VTT Rail Values are Auburndale
VTT=1.05V; Clarkfield
VTT=1.1V

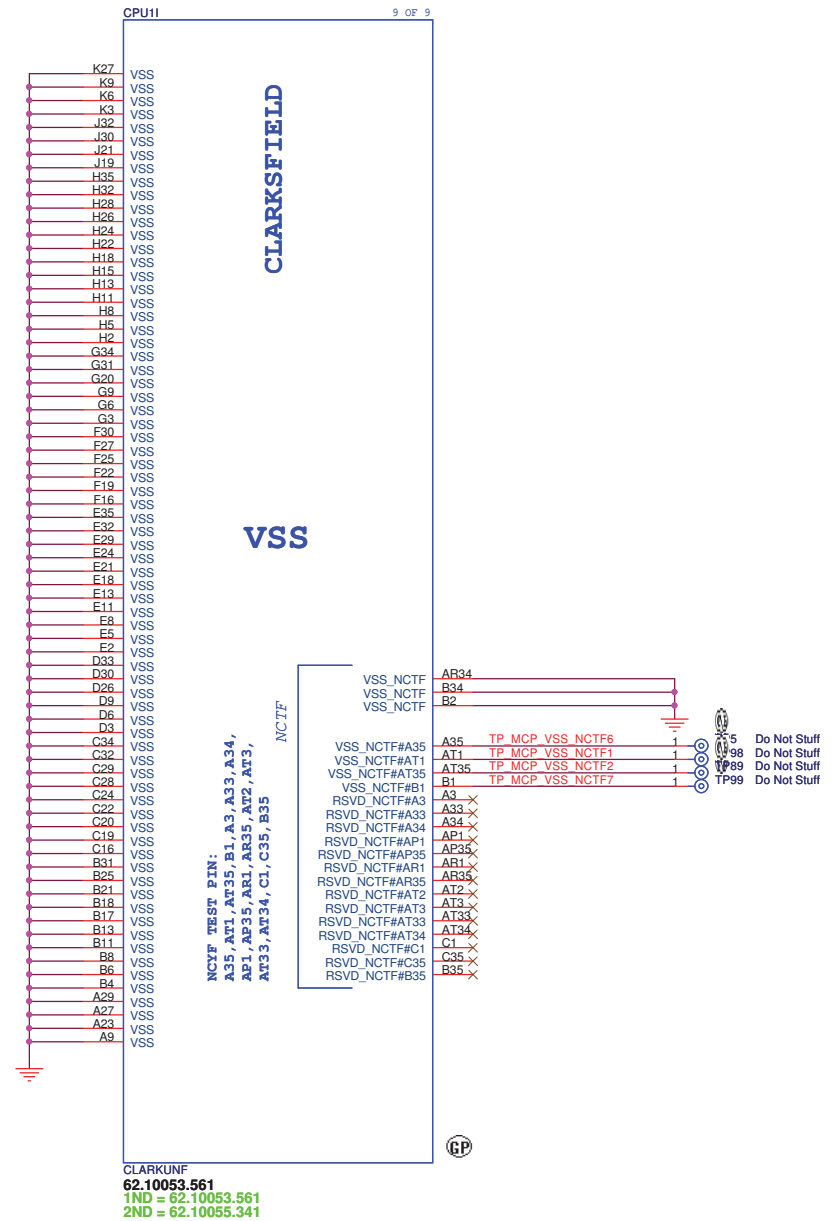
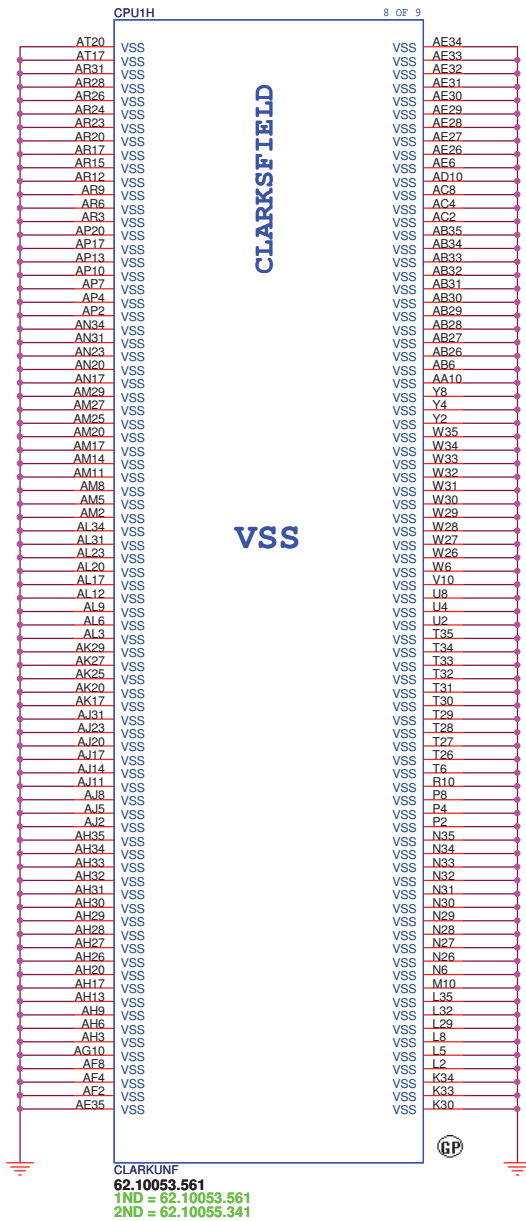
Madison ATI

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.

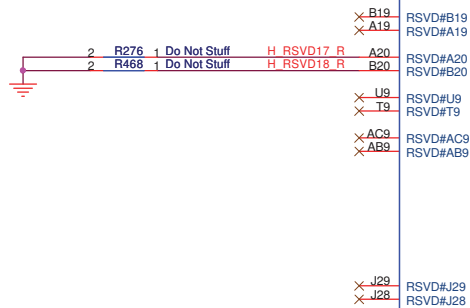
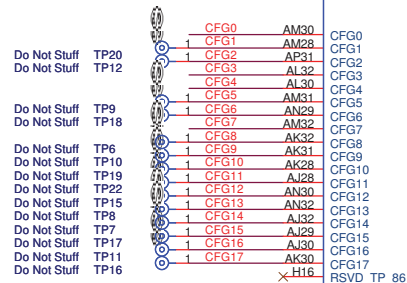
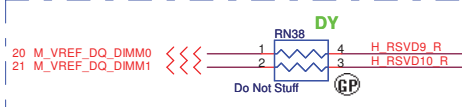
Title		CPU (4/7)	
Size	Document Number	JM31-CP	
Custom			Rev SA
Date: Thursday, February 25, 2010		Sheet 7	of 62

Please note that the VTT Rail Values are Auburndale
VTT=1.05V; Clarksfield
VTT=1.1V



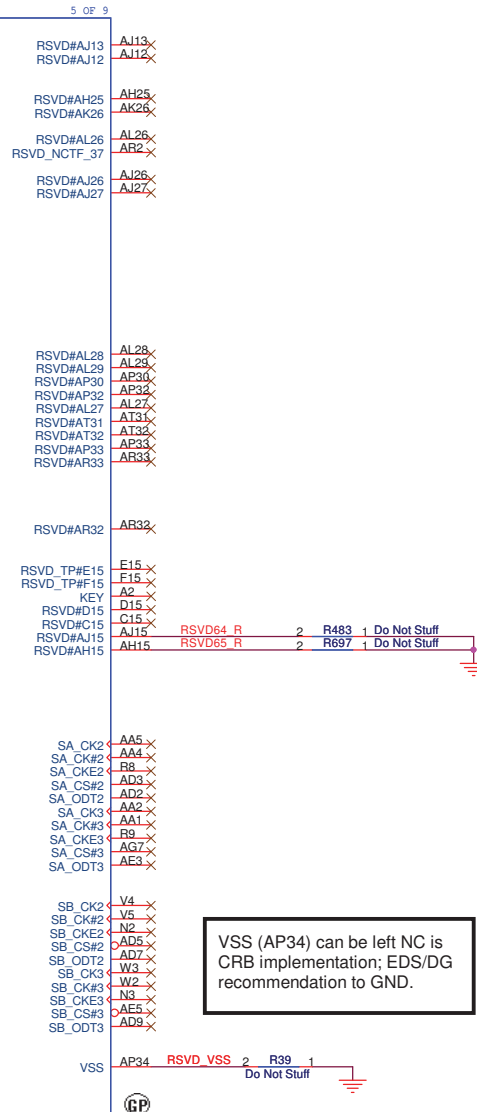


20 M_VREF_DQ_DIMM0 <<< 1 RN38 4 H_RSVD9_R DY
21 M_VREF_DQ_DIMM1 <<< 2 3 H_RSVD10_R
Do Not Stuff (P)

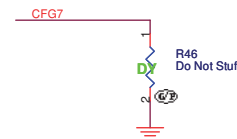
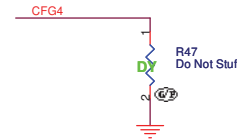
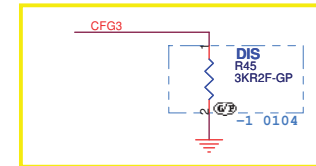
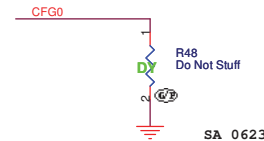


CLARKUNF
62.10053.561
1ND = 62.10053.561
2ND = 62.10055.341

RESERVED



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

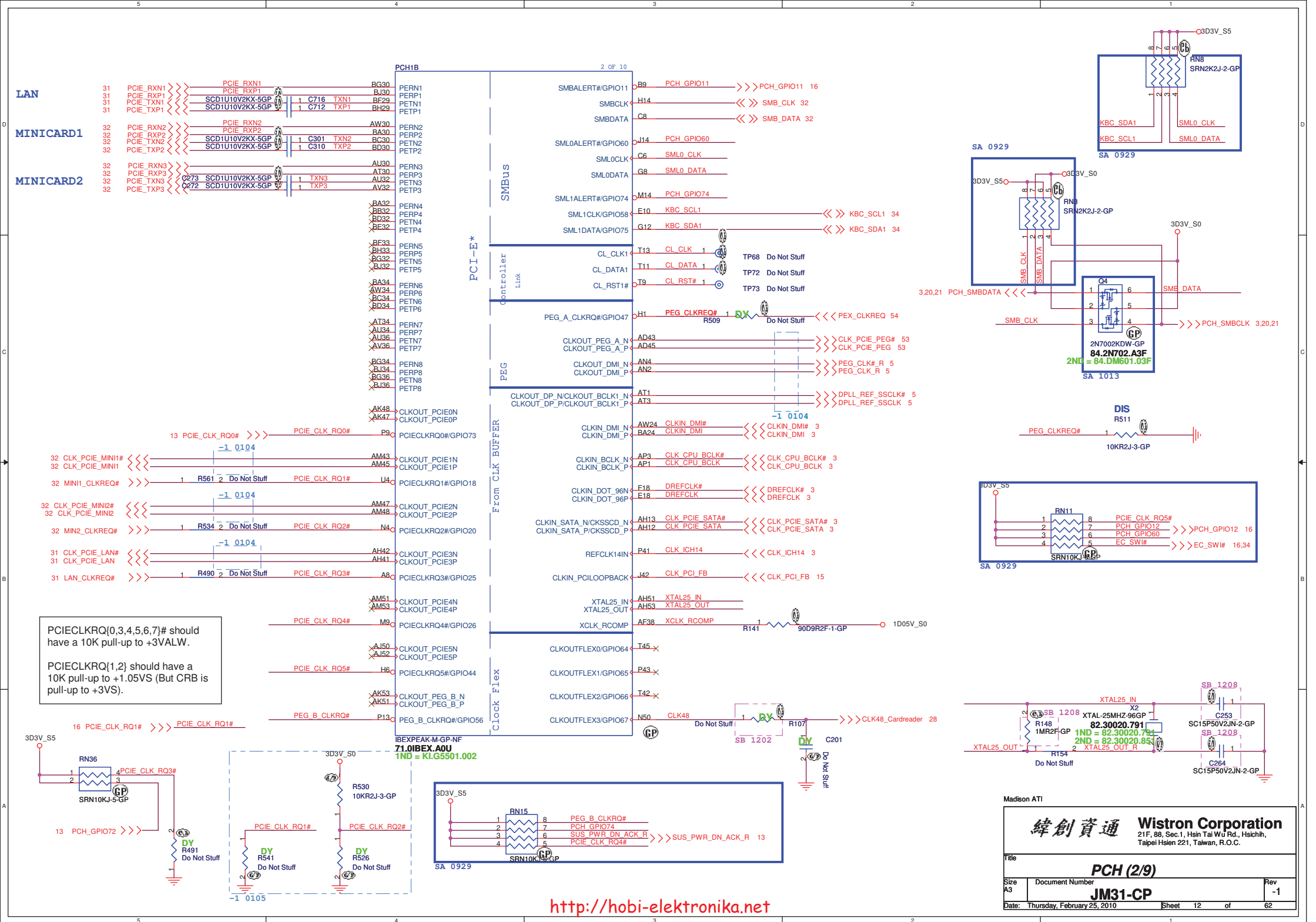


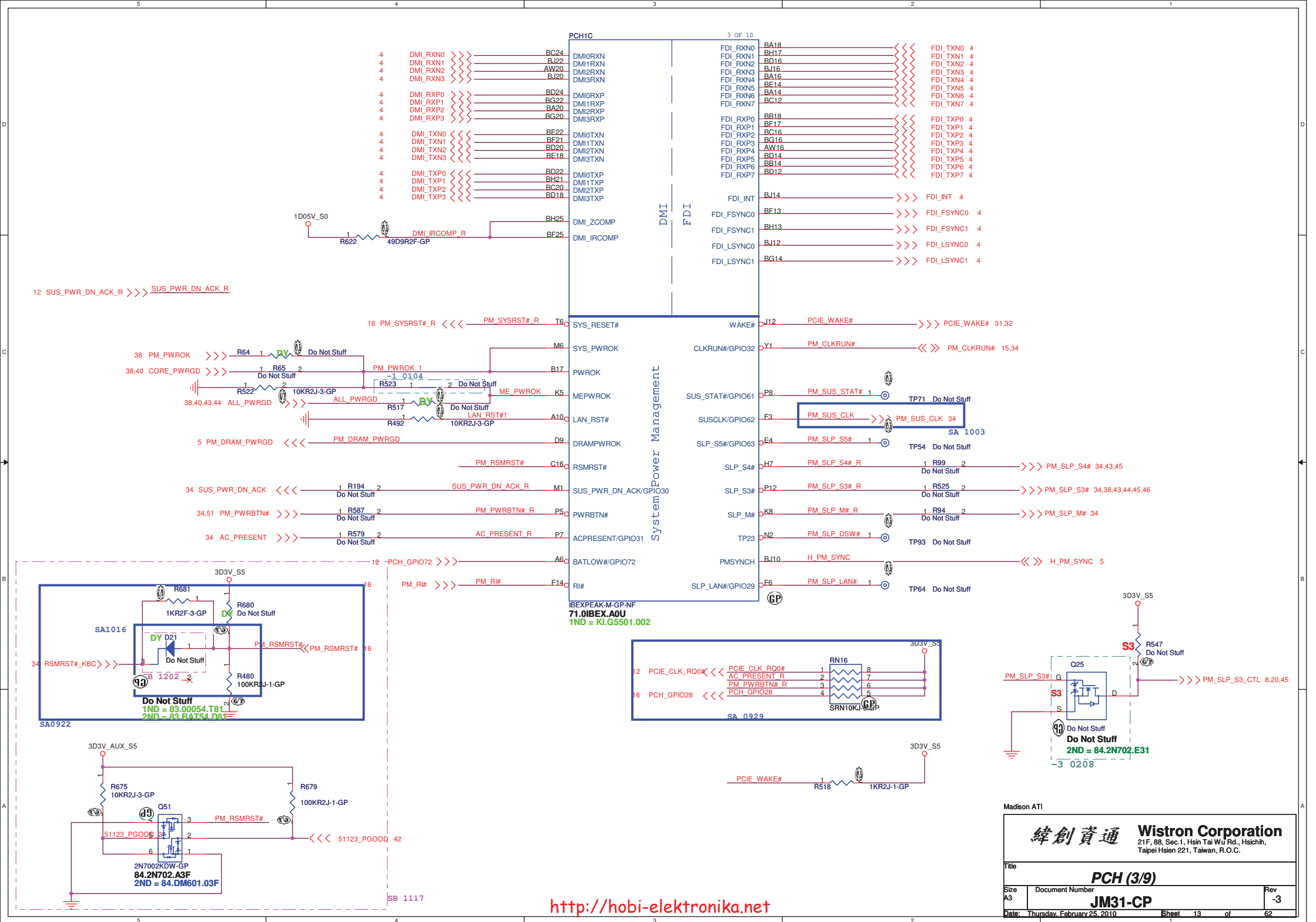
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

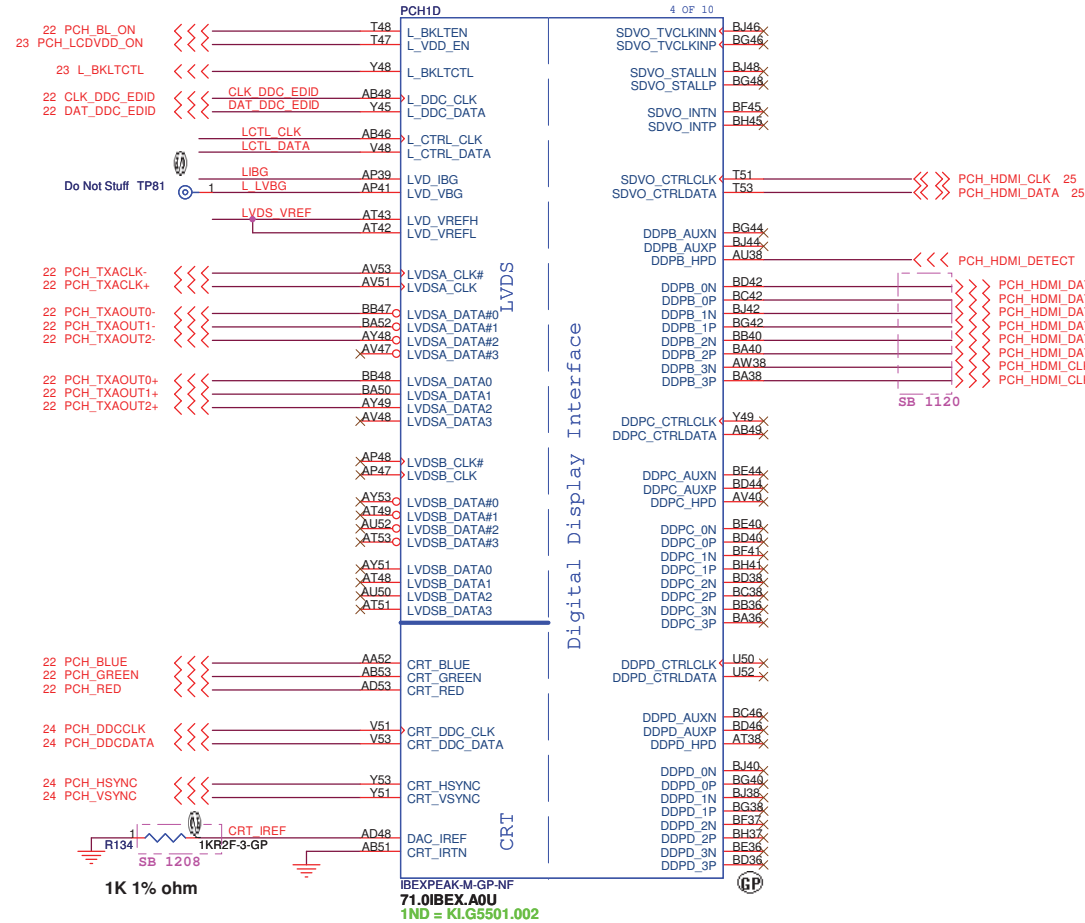
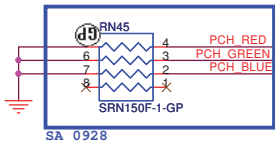
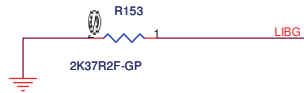
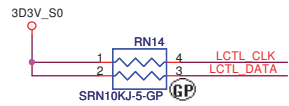
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

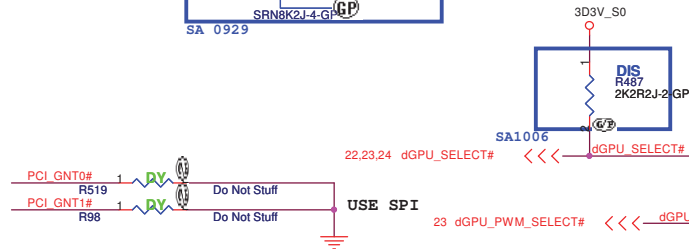
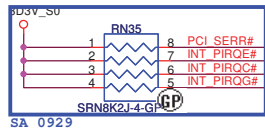
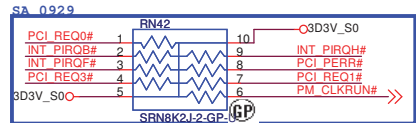
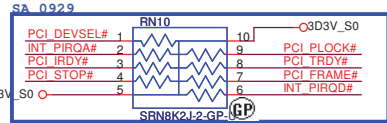
CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	<p>Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor.</p> <p>Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report].</p> <p>For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.</p>





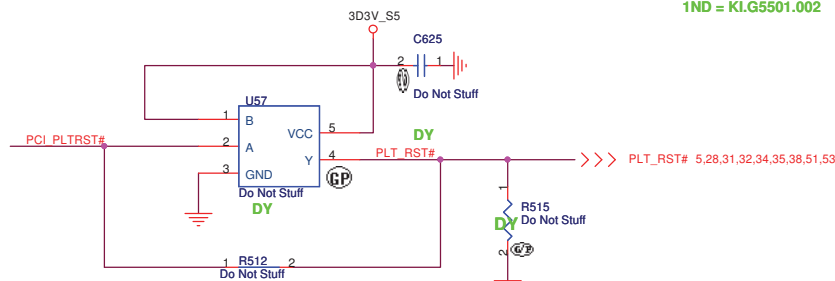
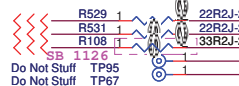


These pins are left as NC,
because the function is disable.



BOOT BIOS Strap		
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC (Default)
1	0	Reserved
0	1	PCI
1	1	SPI

35 POLK_FWH
12 CLK_PCI_FB
34 CLK_PCI_KBC



PCH1E

H40 AD0
N34 AD1
C44 AD2
A38 AD3
C36 AD4
J34 AD5
A40 AD6
D45 AD7
E36 AD8
H48 AD9
E40 AD10
C40 AD11
M48 AD12
M45 AD13
F53 AD14
M40 AD15
M43 AD16
J36 AD17
K46 AD18
F40 AD19
K46 AD20
M51 AD21
J52 AD22
K51 AD23
L34 AD24
F42 AD25
J40 AD26
G46 AD27
F44 AD28
M47 AD29
AD30
H36 AD31

J50 C/BE0#
G42 C/BE1#
H47 C/BE2#
G34 C/BE3#

INT PIROA# G38
INT PIROB# H51
INT PIROF# B37
INT PIROD# A44

PCI REQ0# F51
PCI REQ1# A46
PCI REQ3# M53

PCI GNT0# F48
PCI GNT1# K46
PCI GNT3# H53

INT PIROE# B41
INT PIROF# K53
INT PIROG# A36
INT PIROH# A48

PCI SERR# E44
PCI PERR# E50

PCI IRDY# A42
PCI DEVSSEL# H44
PCI FRAME# C46

PCI PLOCK# D49
PCI STOP# D41
PCI TRDY# C48

ICH PME# M7
PCI PLTRST# D5

CLK PCI SIO R N52
CLK PCI FB R P53
CLK PCI KBC R P46
CLK PCI 3 P51
CLK PCI 4 P48

IBEXPEAK-M-GP-NF
71.0IBEX.AOU
1ND = KL.G5501.002

5 OF 10

NV_CE#0 AY9
NV_CE#1 BD1
NV_CE#2 AP15
NV_CE#3 BD8
NV_DQ#0 NV_DQ#1
NV_DQ#2 NV_DQ#3
NV_DQ#4 NV_DQ#5
NV_DQ#6 NV_DQ#7
NV_DQ#8 NV_DQ#9
NV_DQ#10 NV_DQ#11
NV_DQ#12 NV_DQ#13
NV_DQ#14 NV_DQ#15
NV_DQ#16 NV_DQ#17
NV_DQ#18 NV_DQ#19
NV_DQ#20 NV_DQ#21
NV_DQ#22 NV_DQ#23
NV_DQ#24 NV_DQ#25
NV_DQ#26 NV_DQ#27
NV_DQ#28 NV_DQ#29
NV_DQ#30 NV_DQ#31

USBPN0 H18
USBPN1 J18
USBPN2 C18
USBPN3 M20
USBPN4 J20
USBPN5 L20
USBPN6 F20
USBPN7 G20
USBPN8 A20
USBPN9 C20
USBPN10 M22
USBPN11 N22
USBPN12 D21
USBPN13 D21
USBPN14 H22
USBPN15 E22
USBPN16 F22
USBPN17 A22
USBPN18 C22
USBPN19 G24
USBPN20 L24
USBPN21 M24
USBPN22 A24
USBPN23 C24
USBPN24

OC0#/GPIO59 NI16
OC1#/GPIO40 J16
OC2#/GPIO41 E16
OC3#/GPIO42 E16
OC4#/GPIO43 E16
OC5#/GPIO44 G16
OC6#/GPIO45 E12
OC7#/GPIO46 I15

These pins are left as NC,
because the function is disable.

DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.

NV_CLE

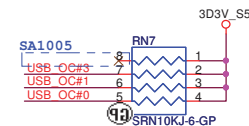
+V_NVRAM_VCCQ

Danbury Technology:
Disabled when Low.
Enable when High.

NV_ALE

USB

Pair	Device
0	EXT USB1
1	USB1 (on board)
2	EXT USB2
3	MINICARD1
4	WECAM
5	SIM Card
6	NC
7	NC
8	NC
9	NC
10	NC
11	Blue Tooth
12	MINIC2
13	Cardreader



A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

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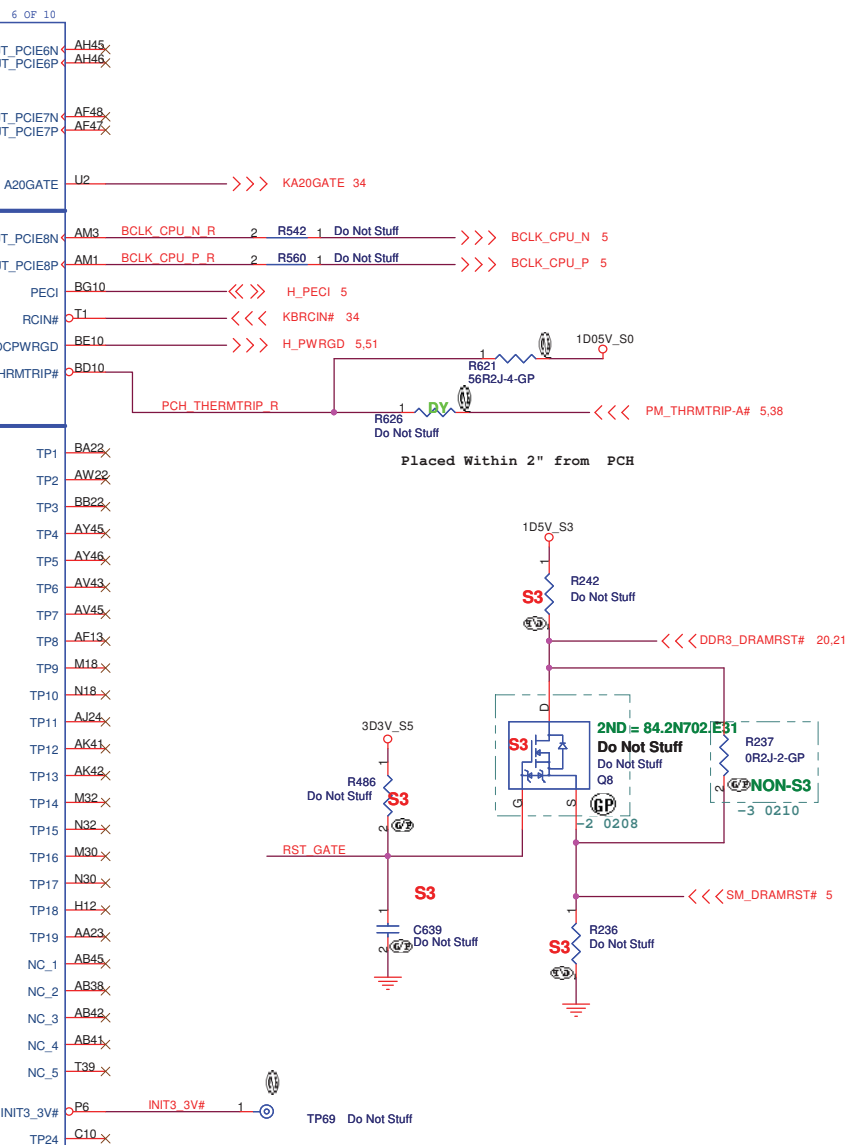
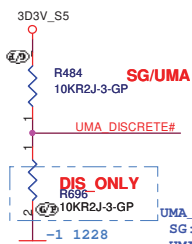
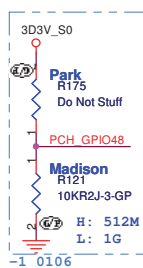
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

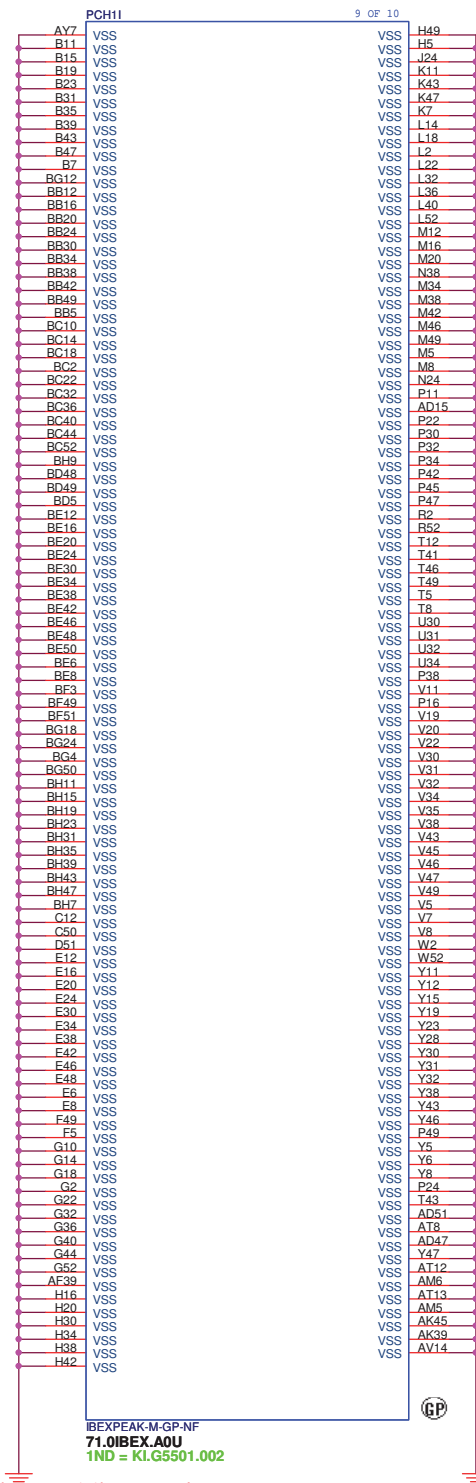
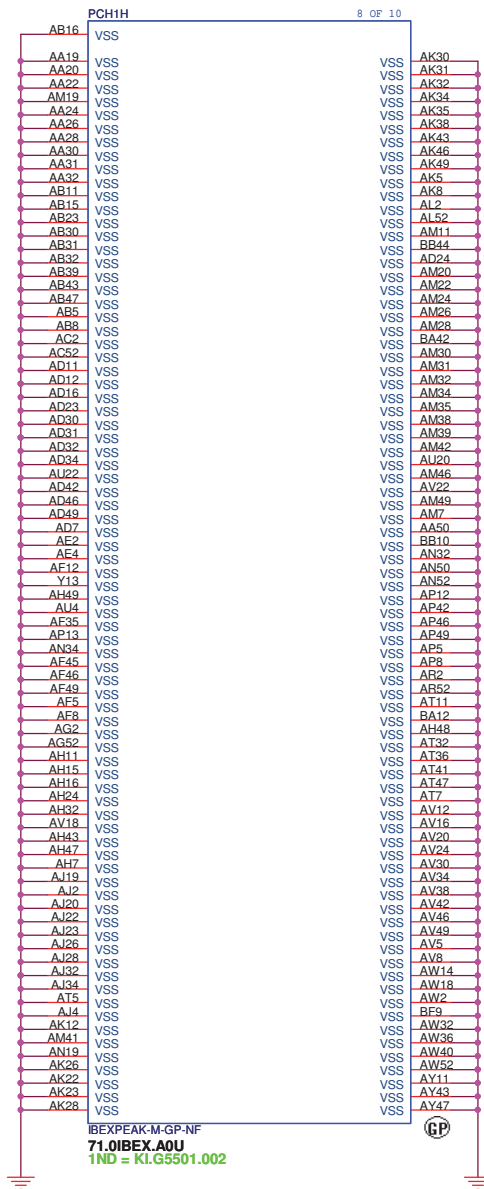
Title PCH (5/9)

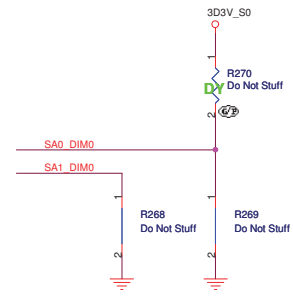
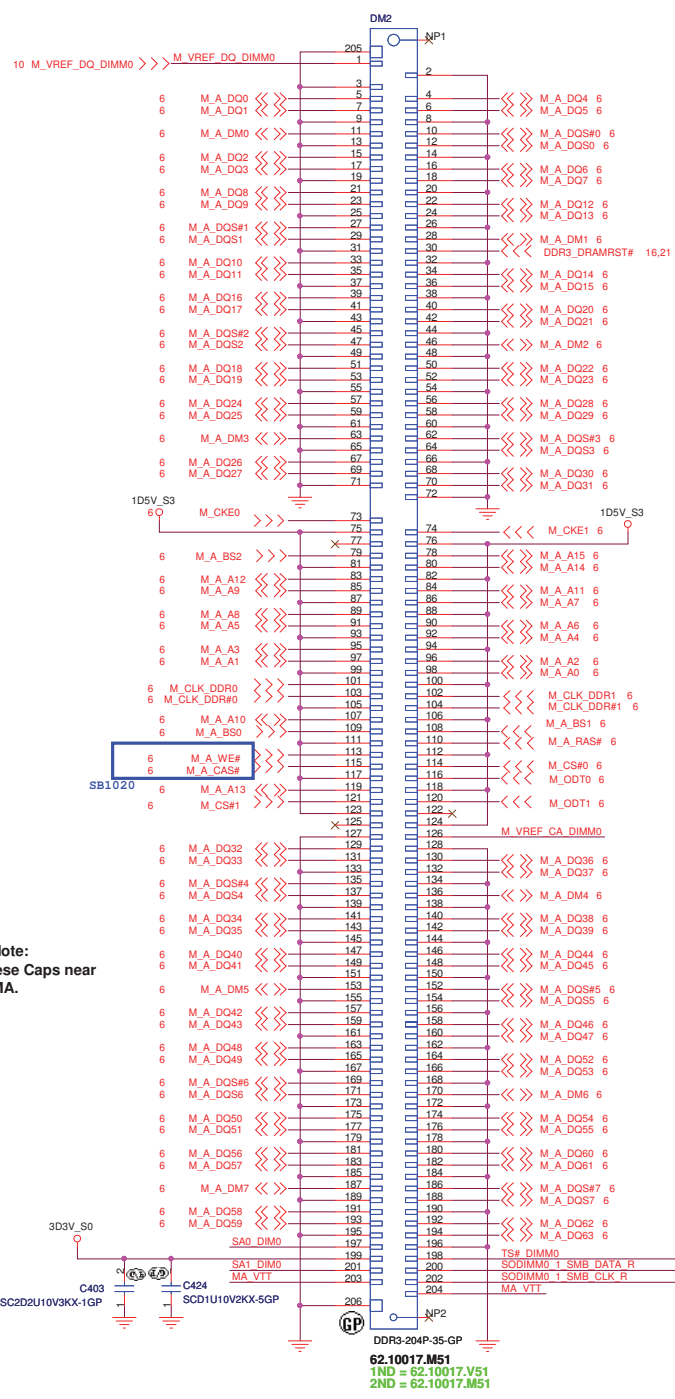
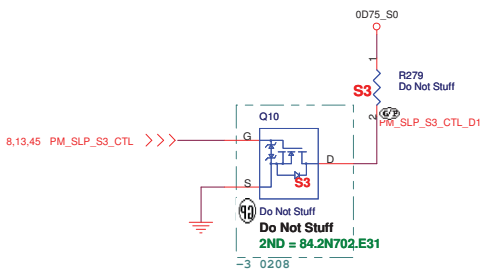
Size A3 Document Number JM31-CP Rev SB

Date: Thursday, February 25, 2010 Sheet 15 of 62

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.



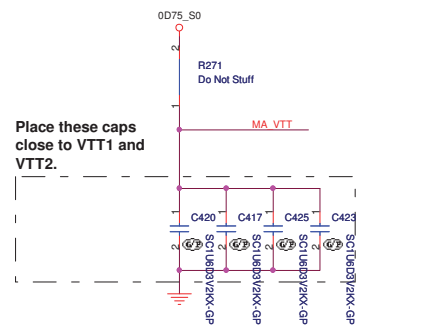
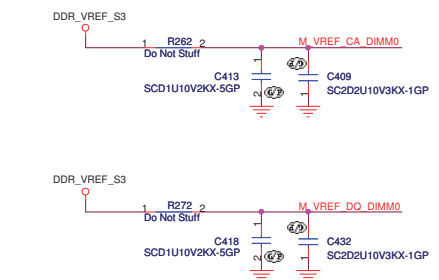
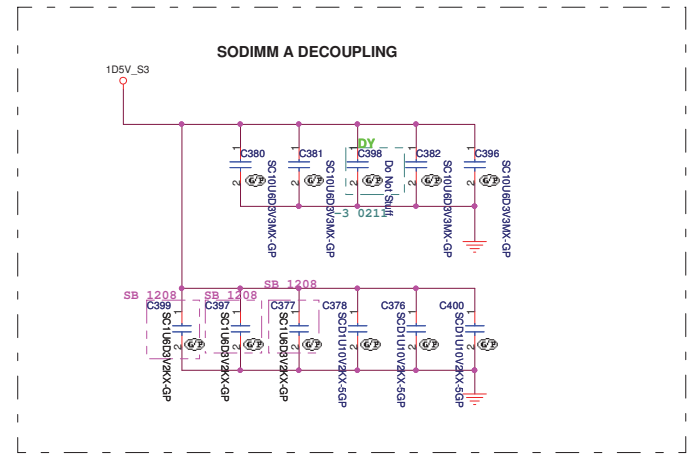




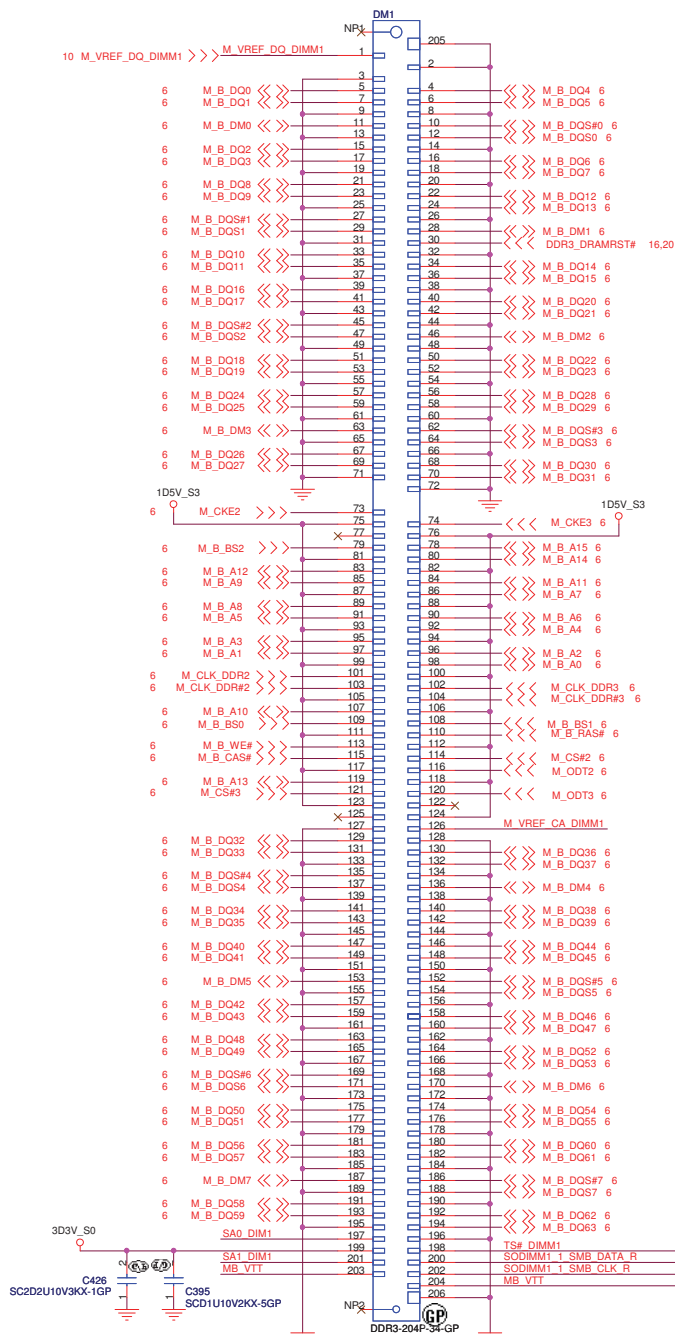
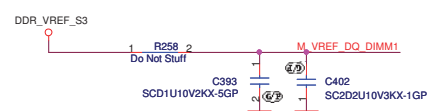
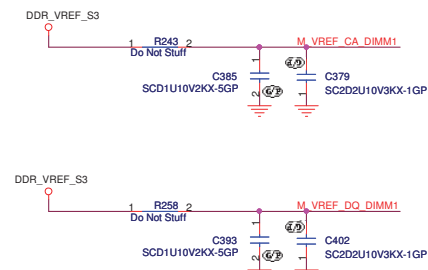
Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Layout Note:
Place these Caps near
SO-DIMMA.



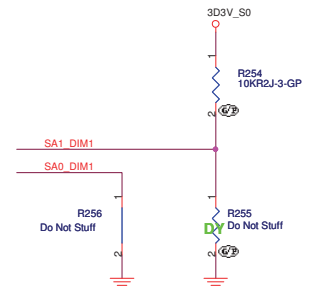
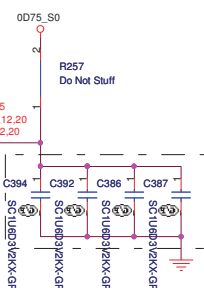
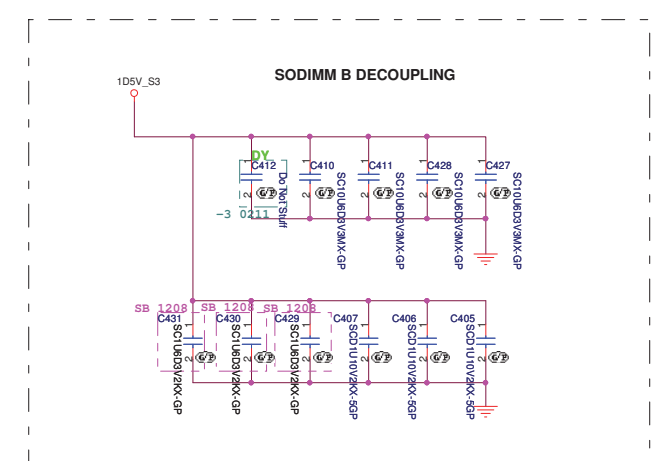
<http://hobi-elektronika.net>



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

Place these caps close to VTT1 and VTT2.



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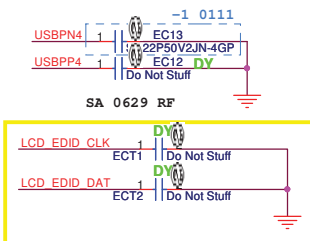
緯創資通 Wistron Corporation
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Title: **DDRIII Socket DM2**

Size: Custom Document Number: **JM31-CP** Rev: **SA**

Date: Thursday, February 25, 2010 Sheet: 21 of 62

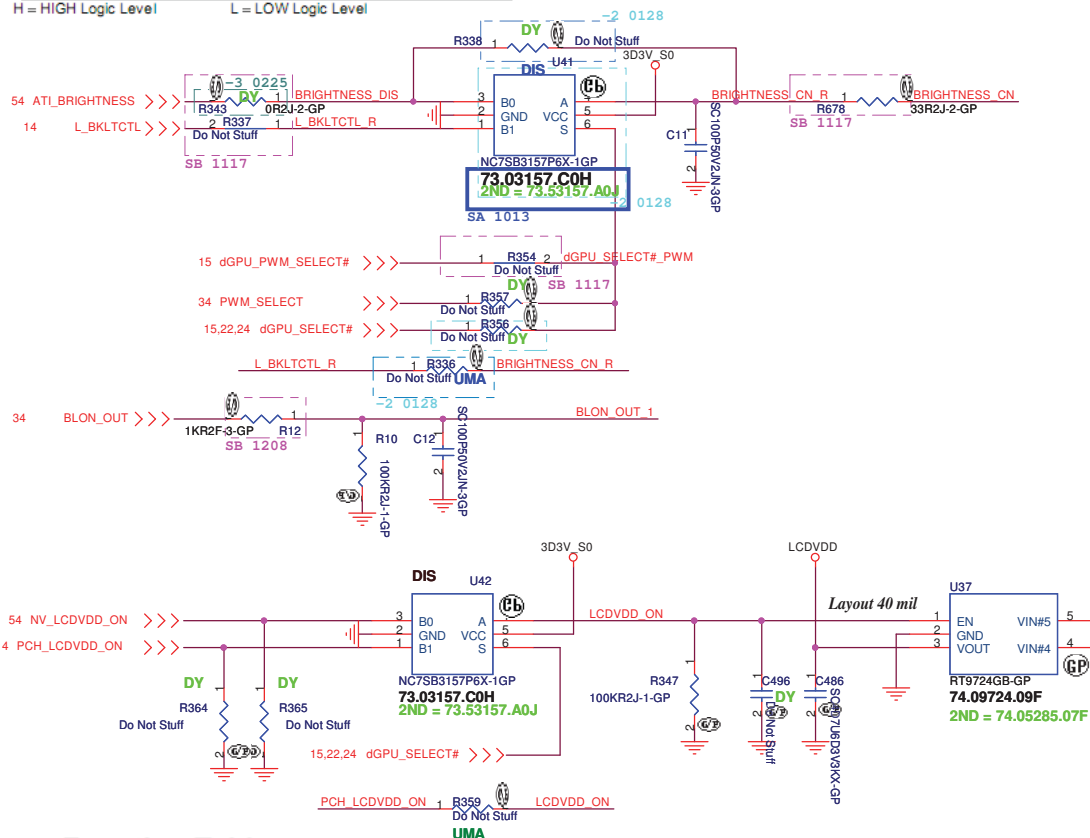
LCD/INVERTER/CCD CONN



Function Table

Input (S)	Function
L	B ₀ Connected to A
H	B ₁ Connected to A

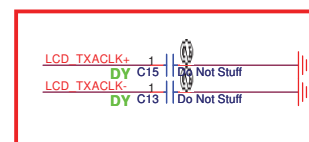
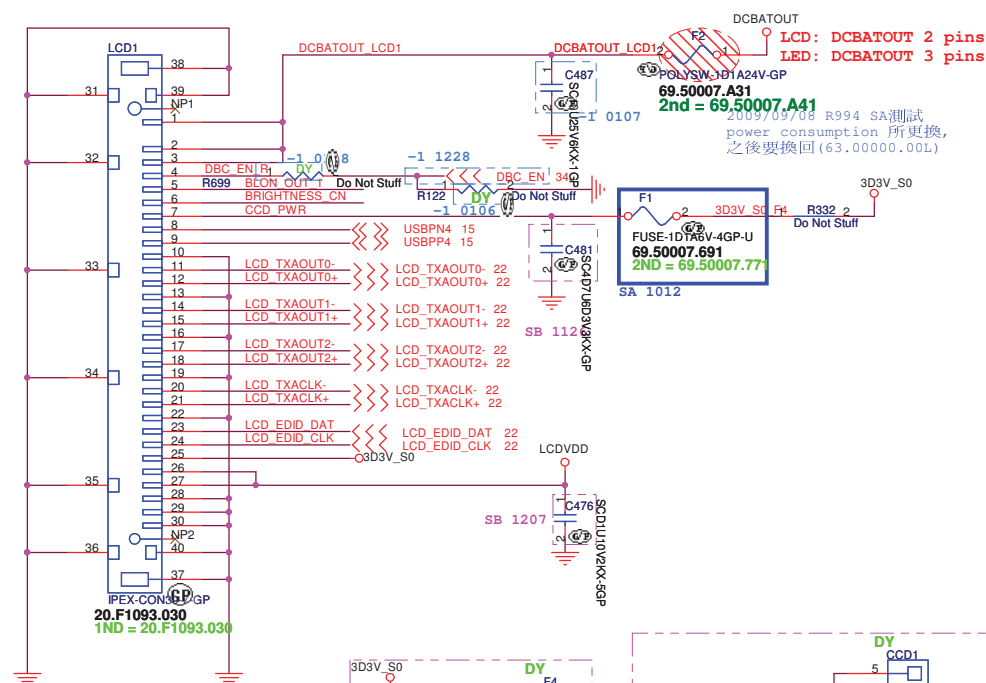
H = HIGH Logic Level L = LOW Logic Level



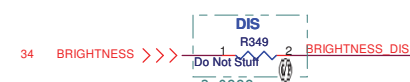
Function Table

Input (S)	Function
L	B ₀ Connected to A
H	B ₁ Connected to A

H = HIGH Logic Level L = LOW Logic Level



modify by RF



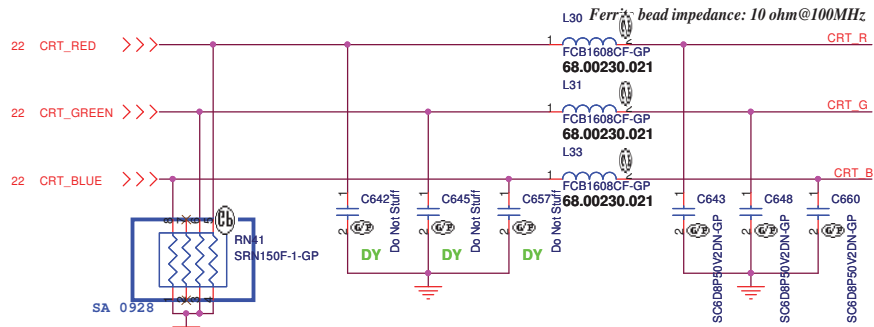
Reserve direct connector to KBC

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Taipei Hsien 221, Taiwan, R.O.C.

LCD CONN			
Size A3	Document Number	JM31-CP	Rev -1
Date: Thursday, February 25, 2010	Sheet 23	of 62	

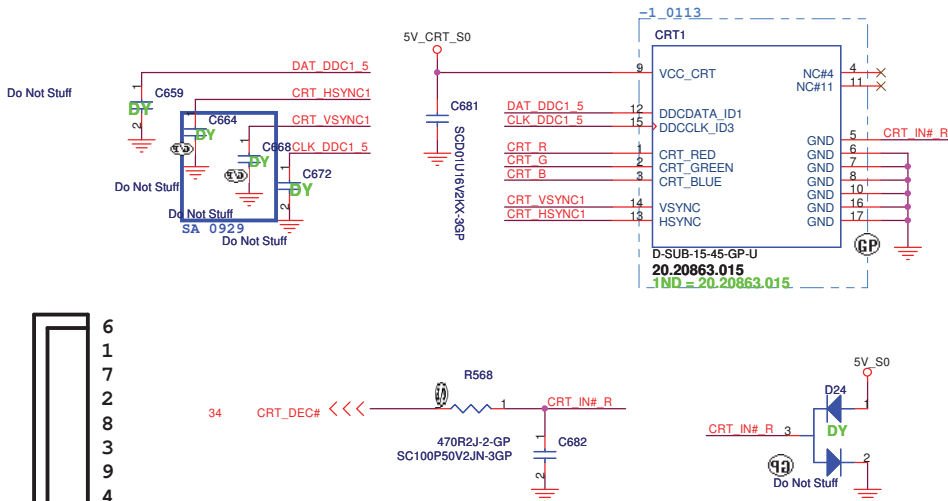
Layout Note:
Place these resistors
close to the CRT-out
connector



Layout Note:

* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT I/F & CONNECTOR



L=>B0 -DIS
H=>B1 -UMA

15,22,23 dGPU_SELECT#

For DIS CRT

54,57 NV_CRT_HSYNC

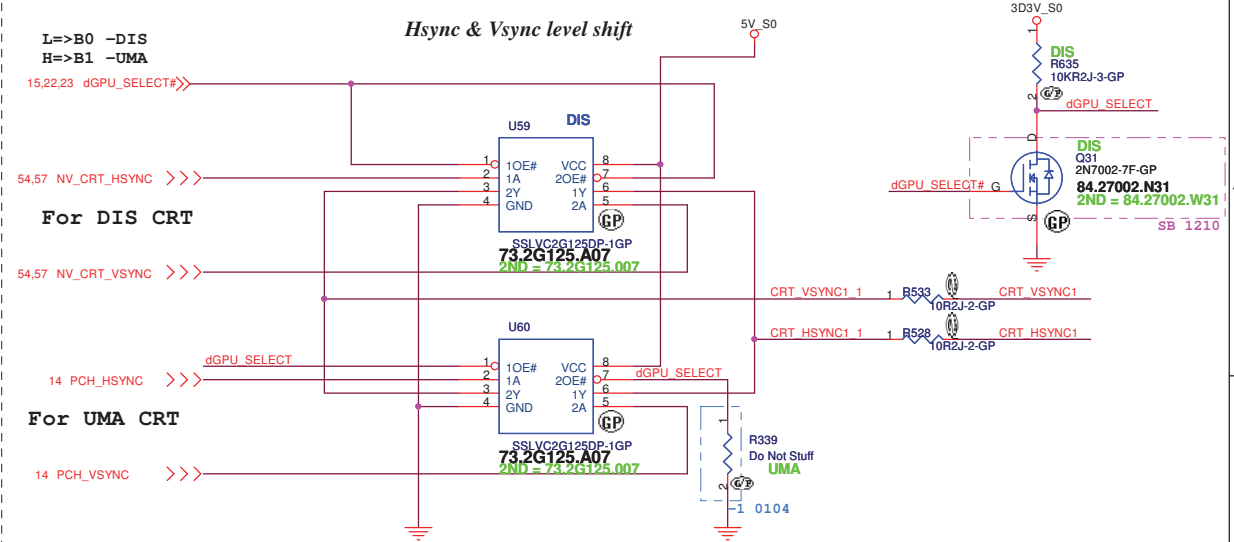
54,57 NV_CRT_VSYNC

For UMA CRT

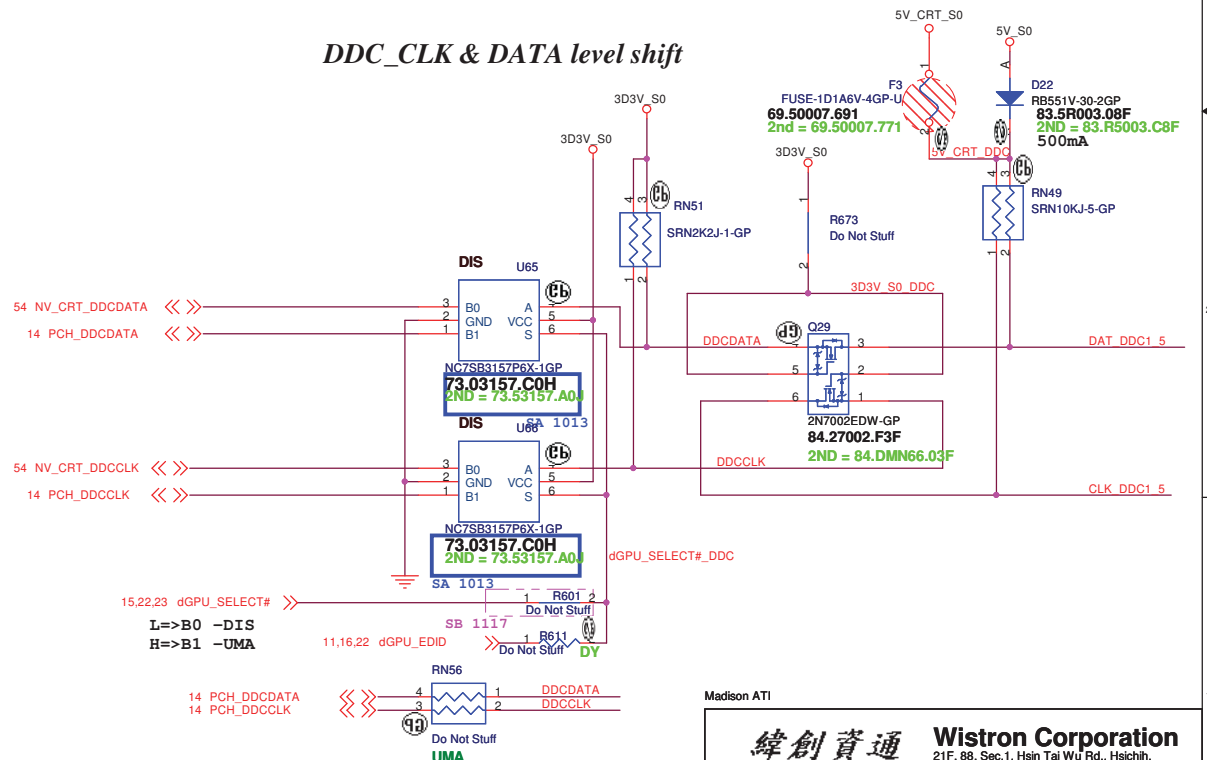
14 PCH_HSYNC

14 PCH_VSYNC

Hsync & Vsync level shift



DDC_CLK & DATA level shift

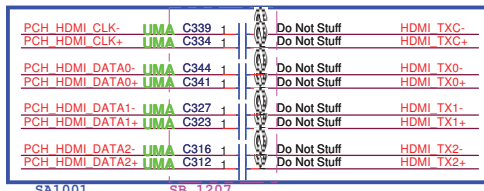
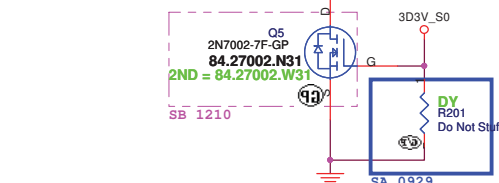
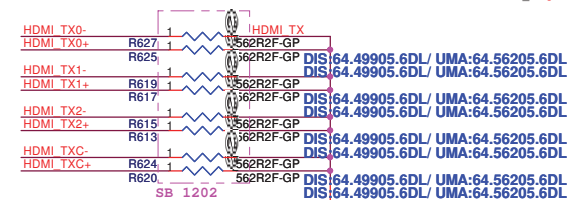
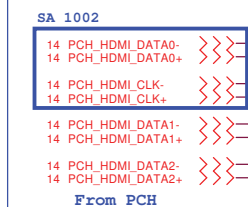
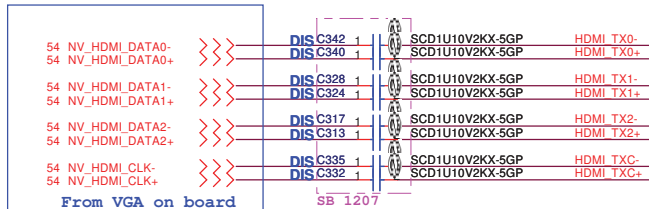
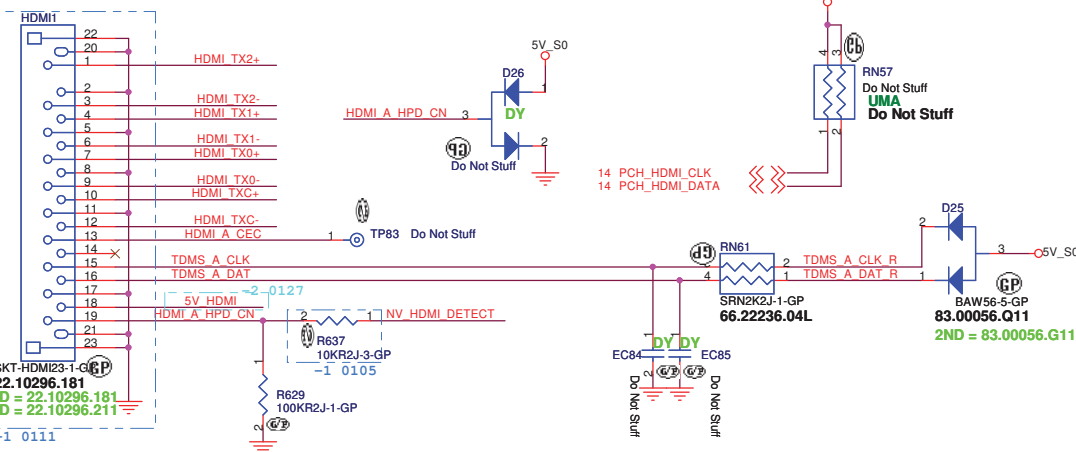


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Taipai Hsien 221, Taiwan, R.O.C.

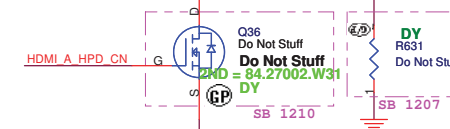
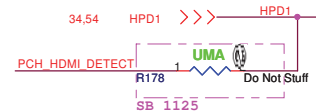
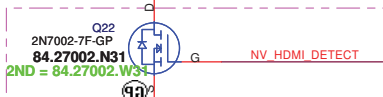
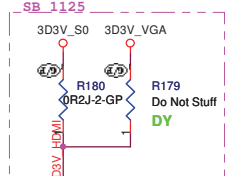
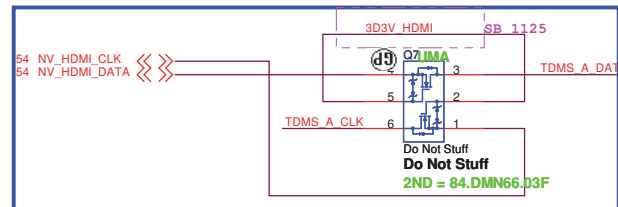
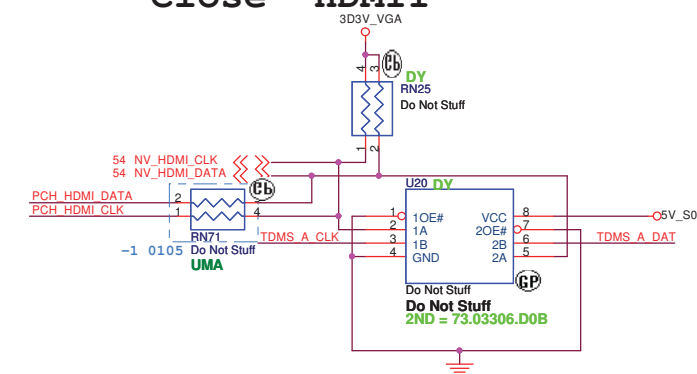
Title			CRT CONN		
Size	Document Number	JM31-CP			Rev
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SB 1209



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Close HDMI1



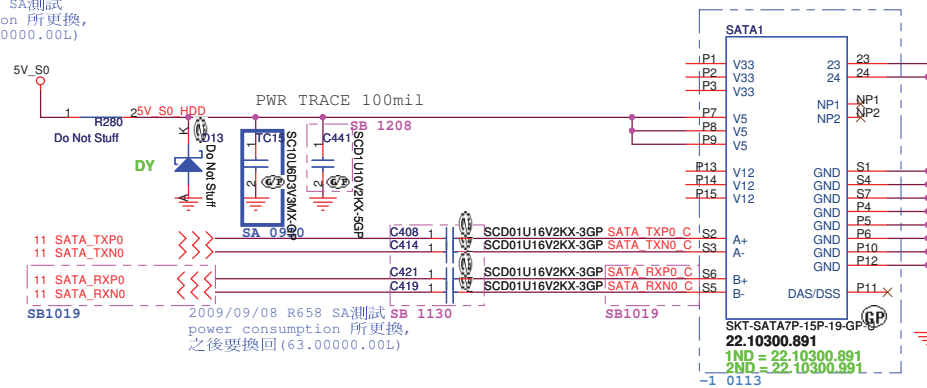
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

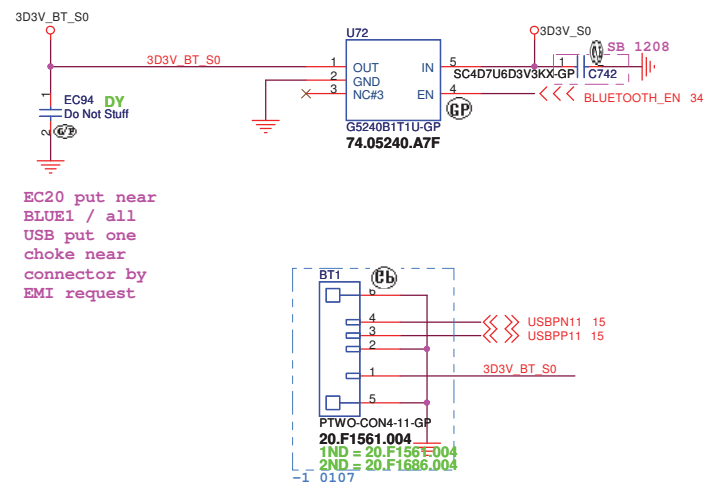
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Size: A3 Document Number: **JM31-CP** Rev: -1
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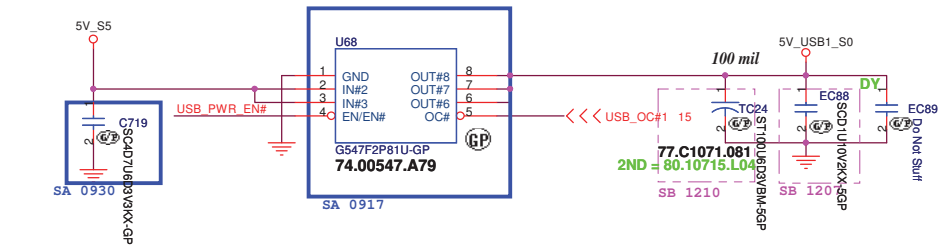
SATA Connector

2009/09/08 R658 SA測試
power consumption 所更換,
之後要換回 (63.00000.00L)



BLUETOOTH MODULE





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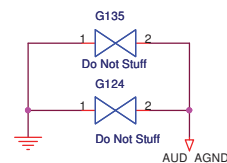
USB CONN

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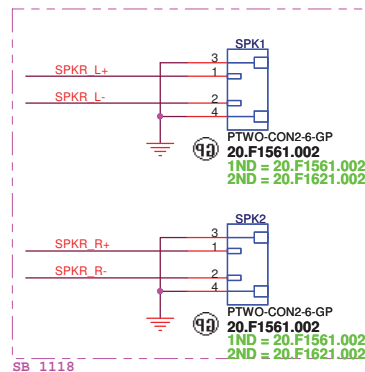
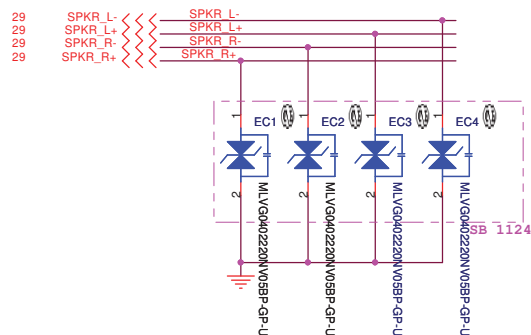
<http://hobi-elektronika.net>



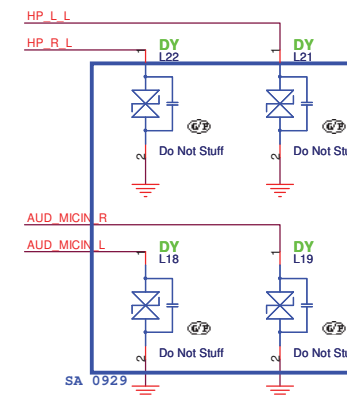
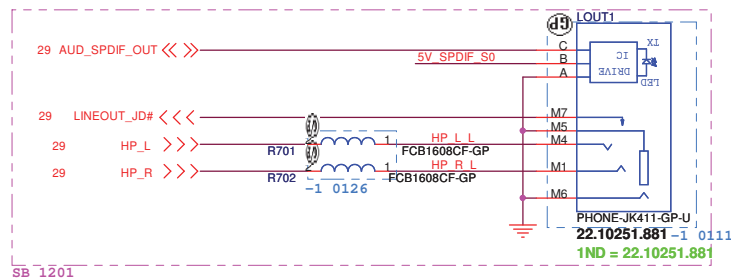
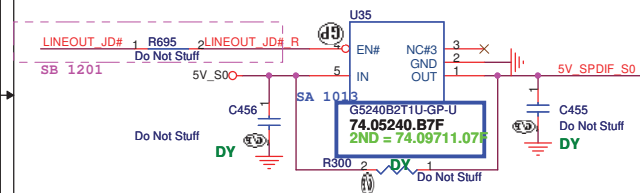
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

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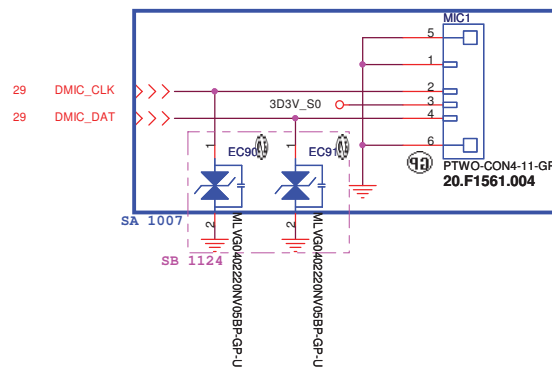
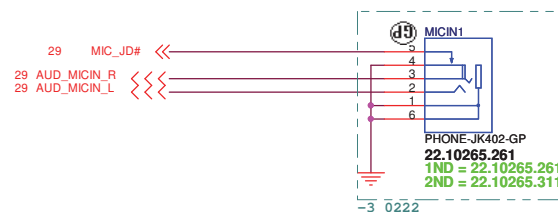
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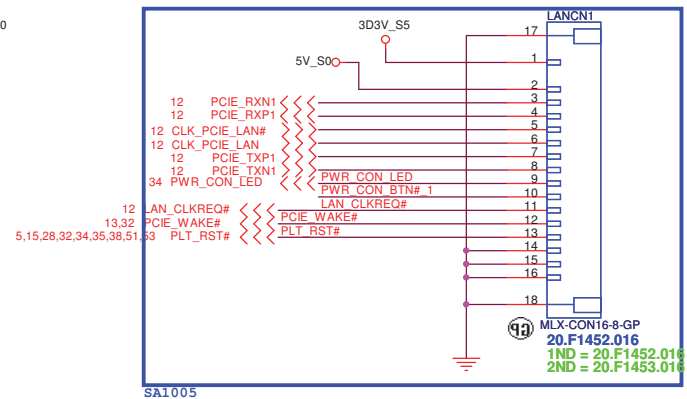
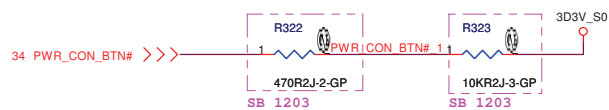


LINE OUT



MIC IN





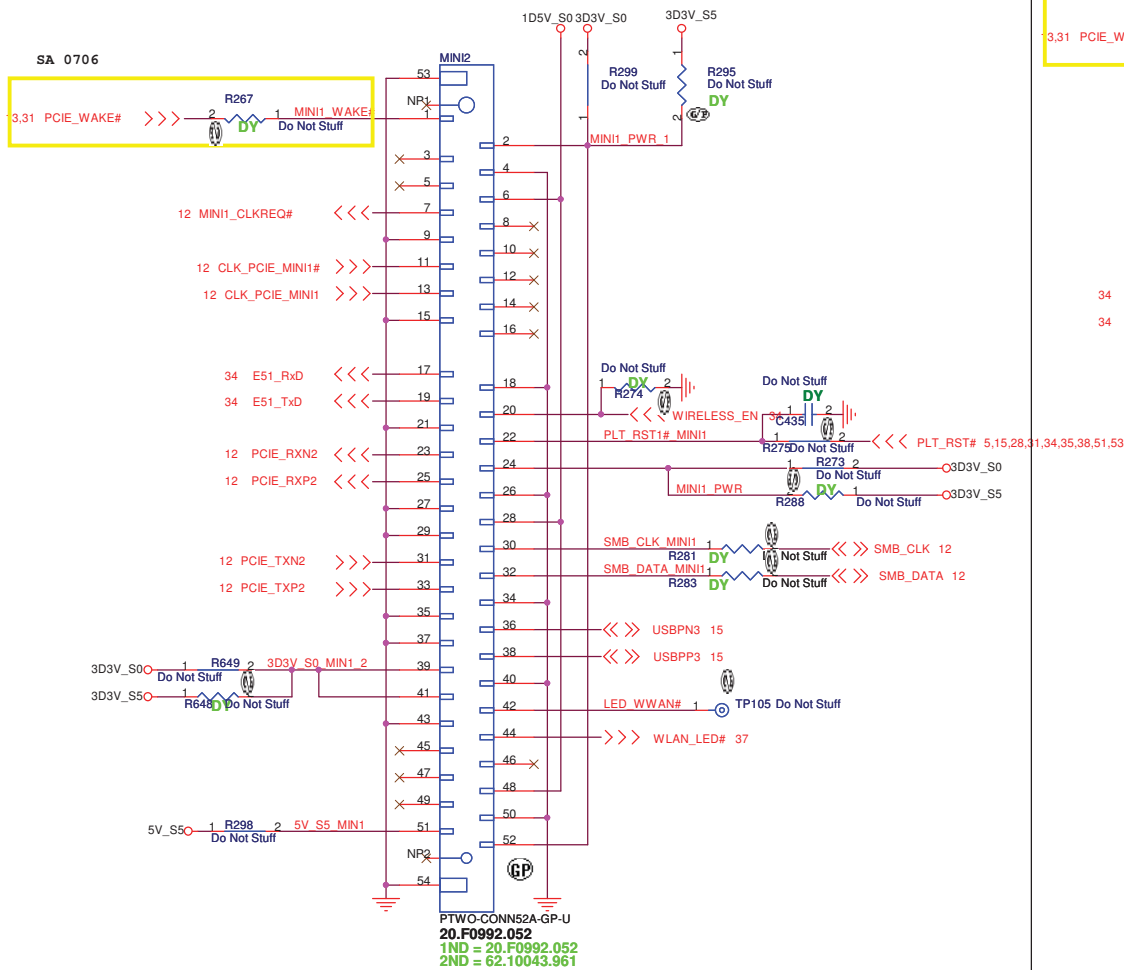
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Taipei Hsien 221, Taiwan, R.O.C.

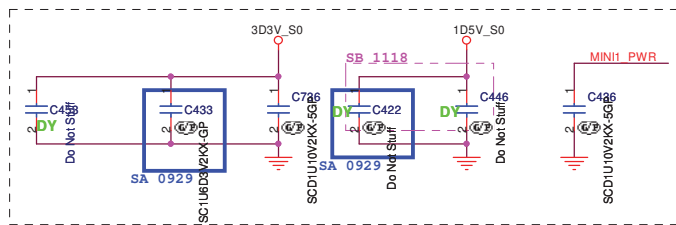
Title			
LAN CONN			
Size A3	Document Number JM31-CP	Rev SB	
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Mini Card Connector(WLAN)

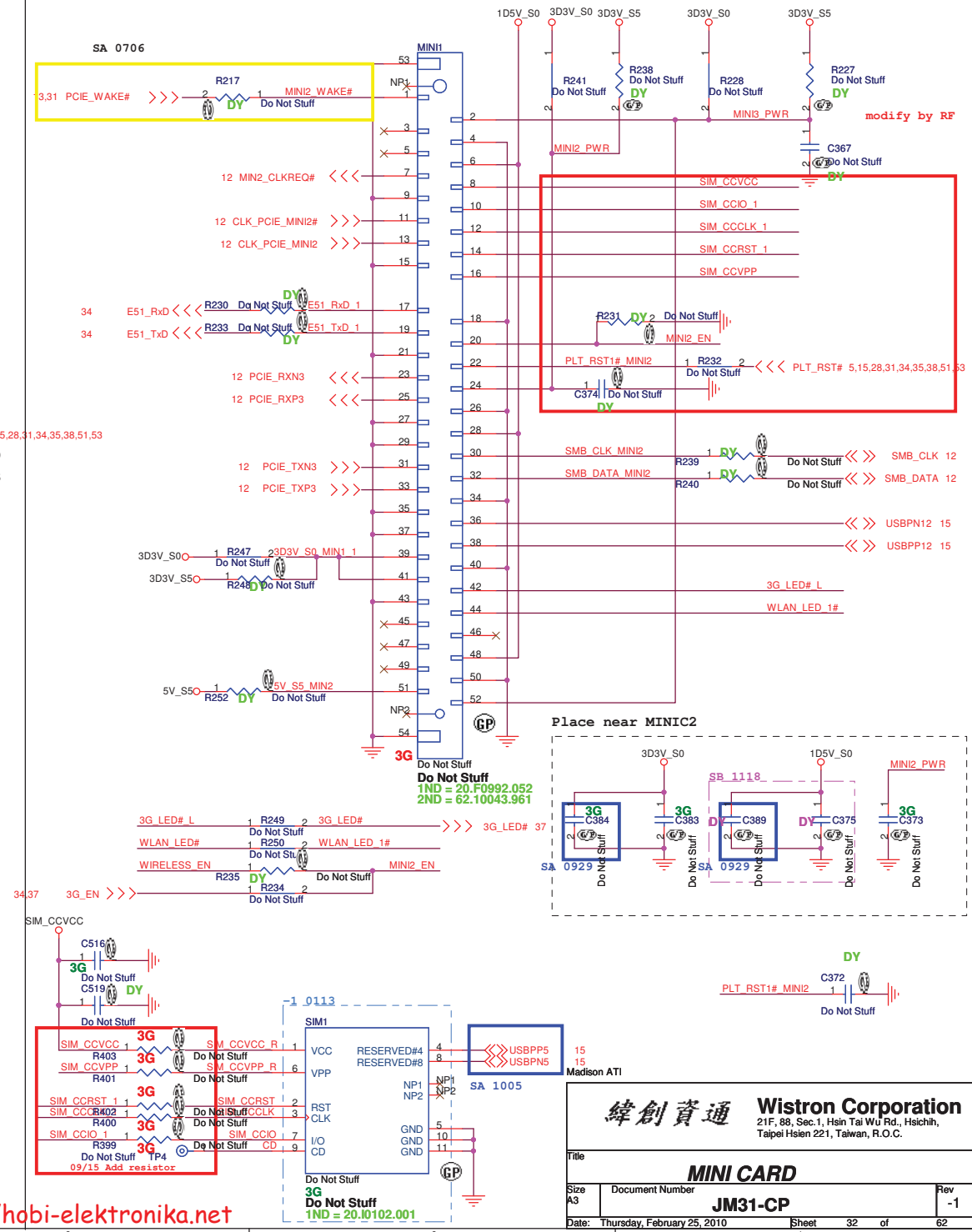
Support debug-card

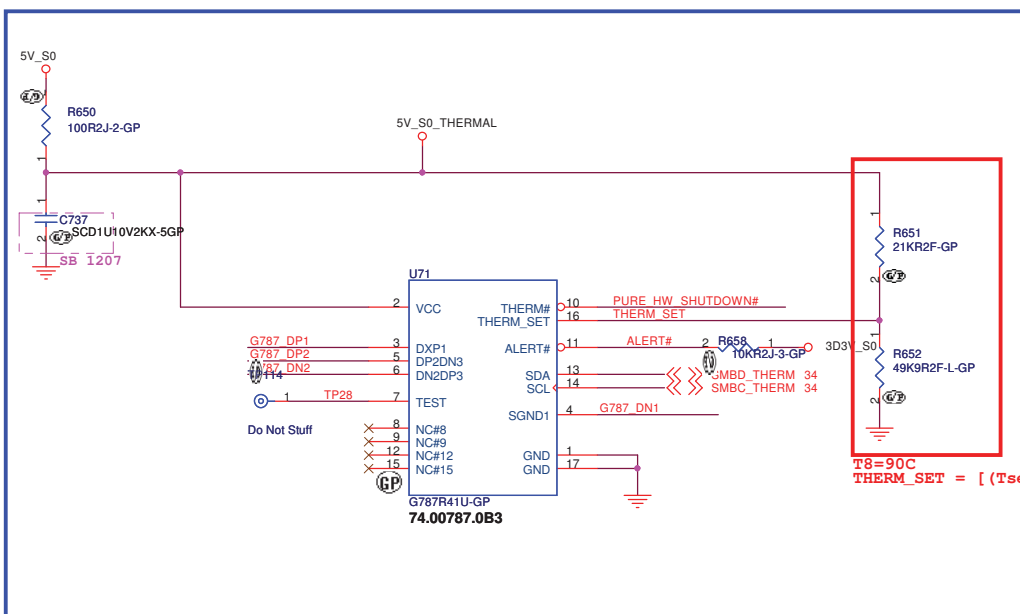
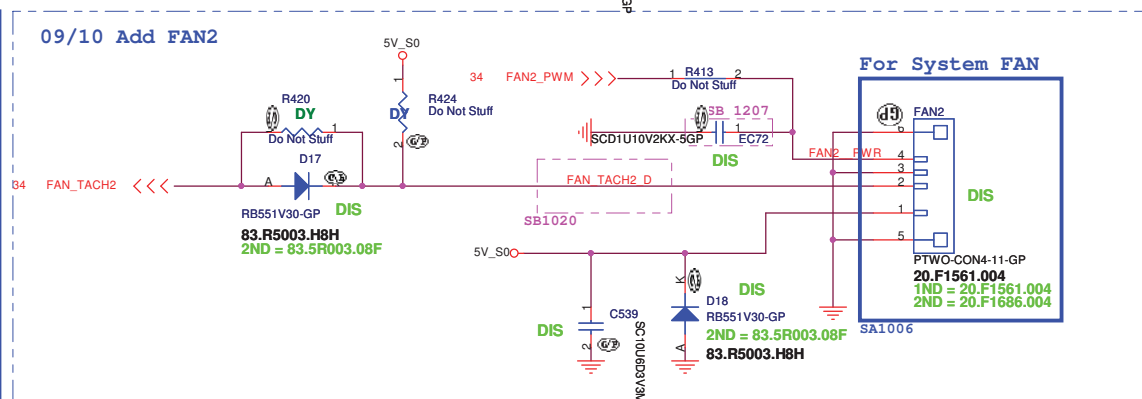
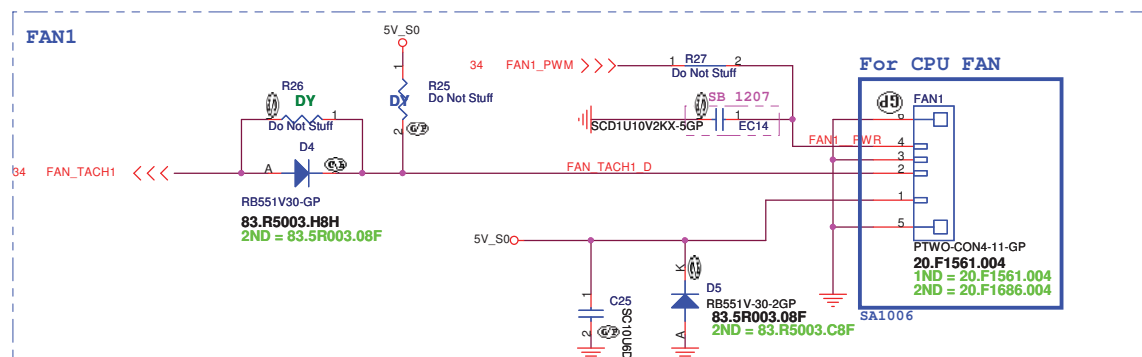
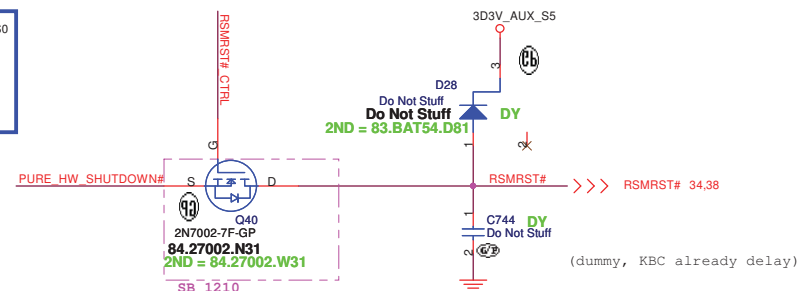
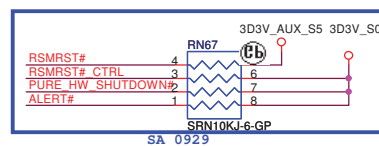
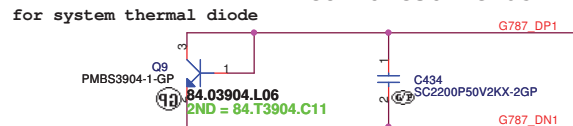
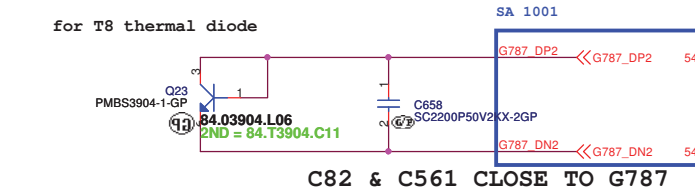


Place near MINI1



Mini Card Connector(Robson2 and 3G)





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Taipei Hsien 221, Taiwan, R.O.C.

Title Thermal/Fan Connector

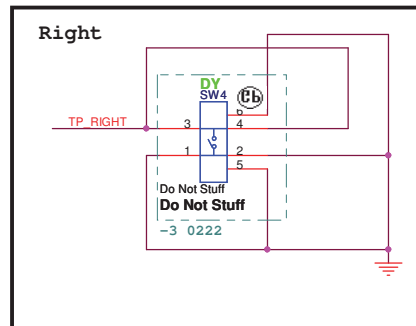
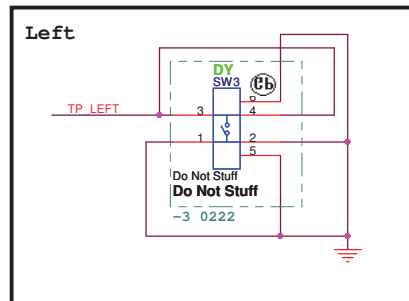
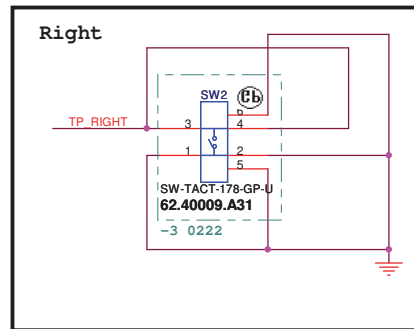
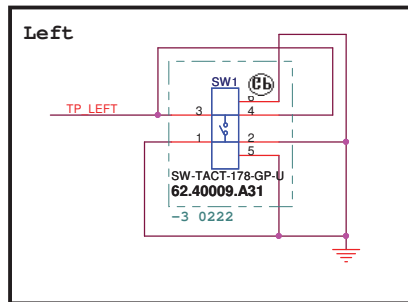
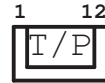
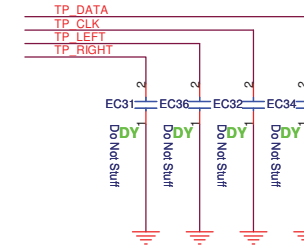
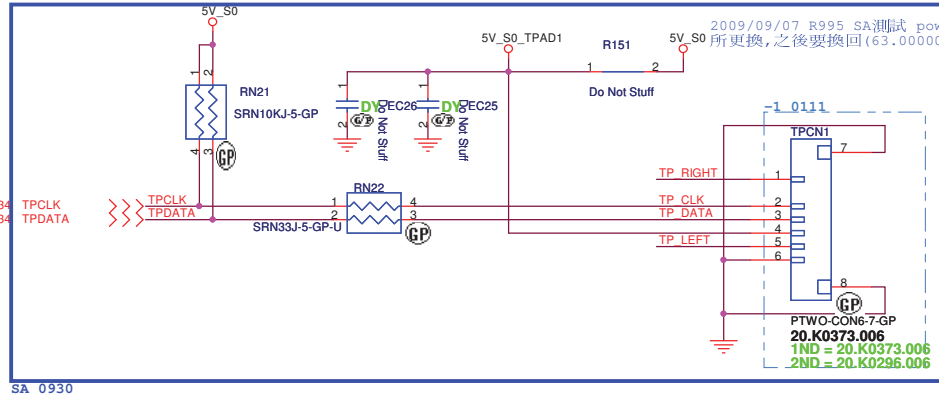
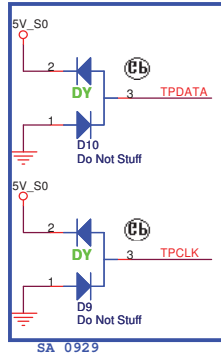
Size A3 Document Number JM31-CP

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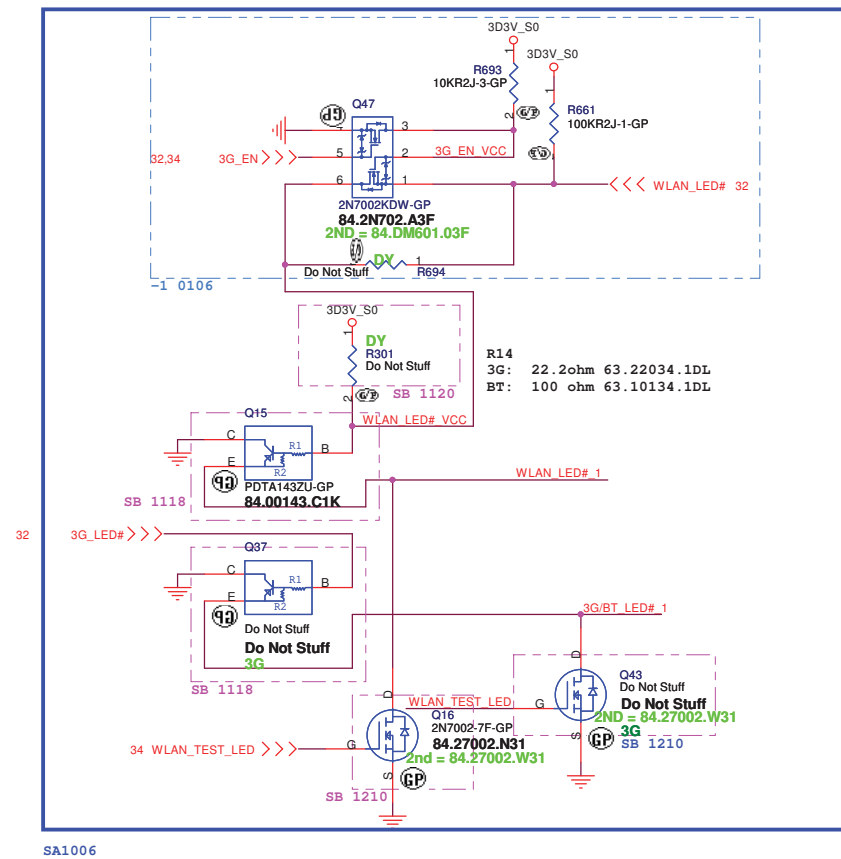
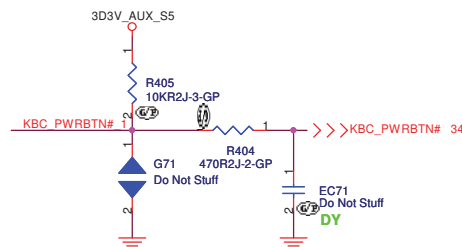
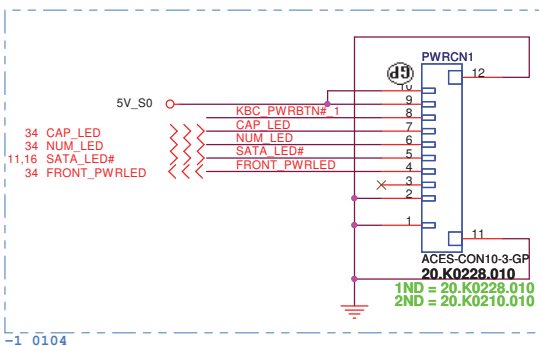
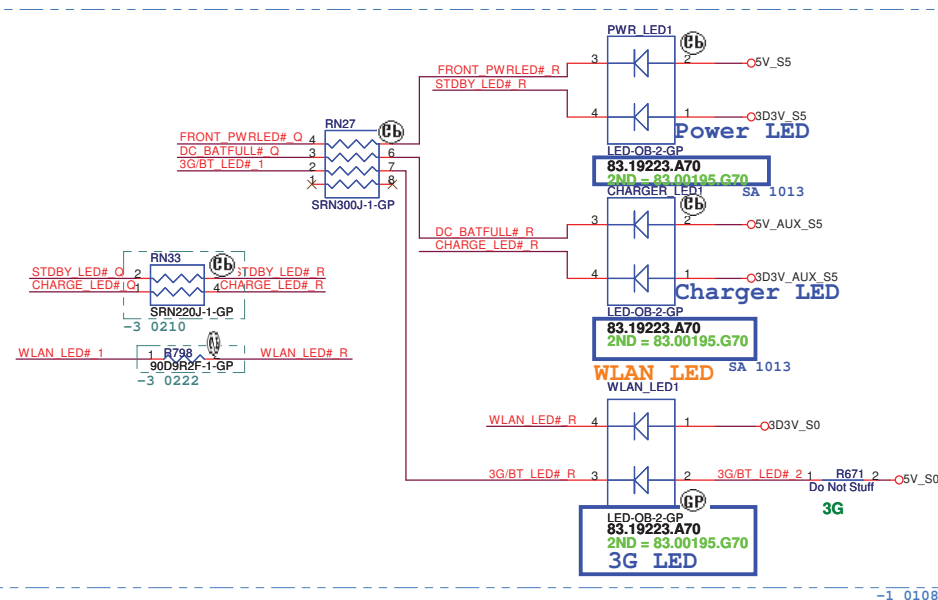
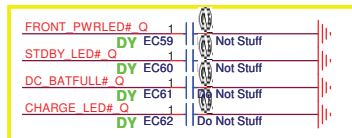
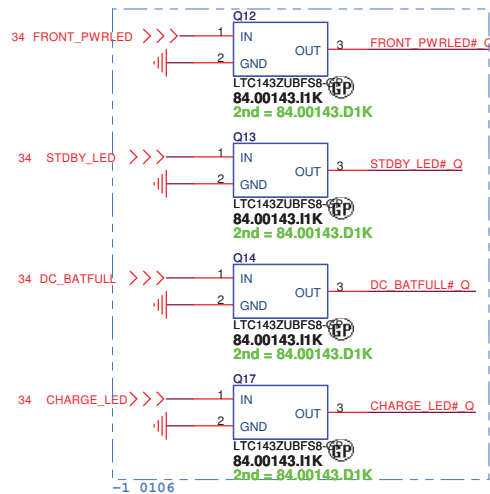
TOUCH PAD



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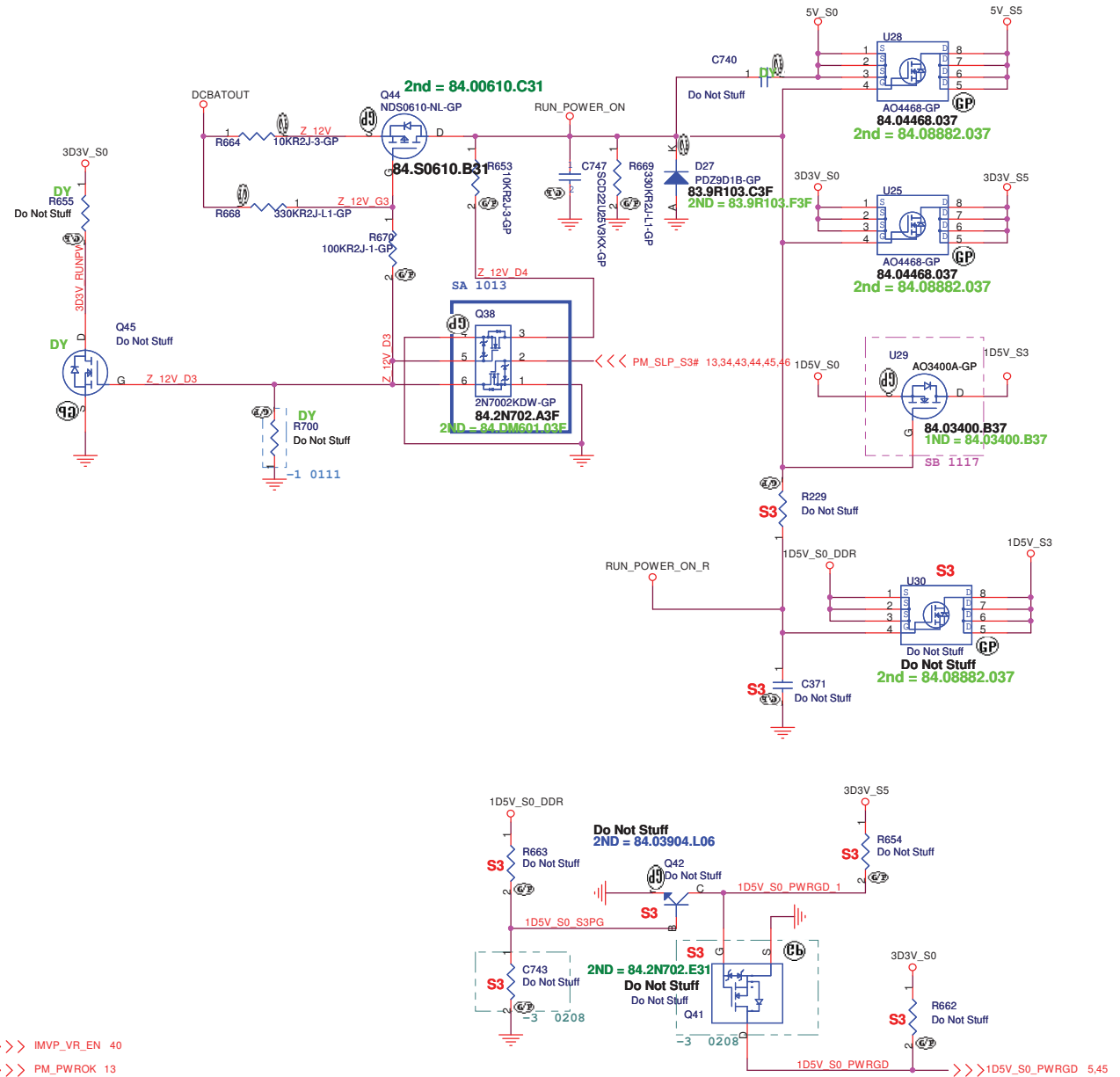
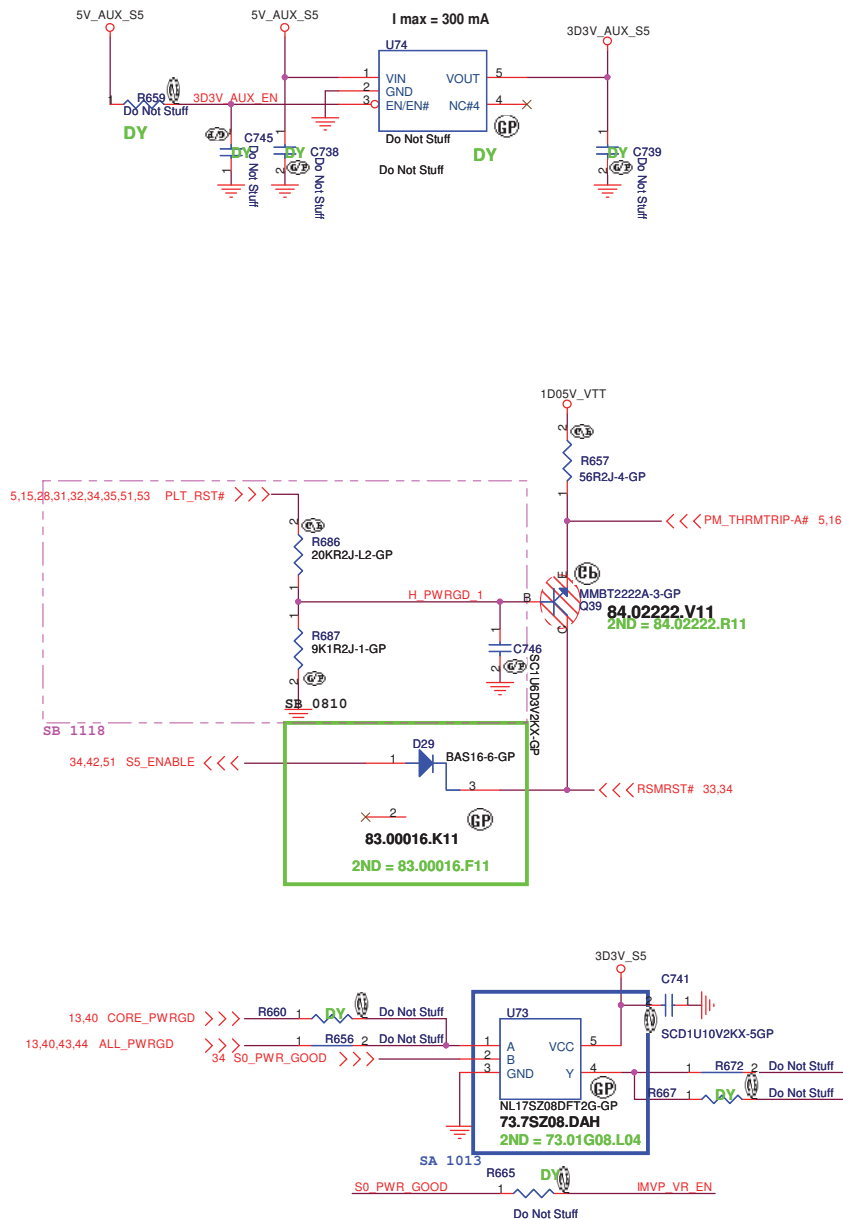
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Title		Touch PAD	
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Run Power

Aux Power

3D3V_AUX_S5



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Taipei Hsien 221, Taiwan, R.O.C.

Title

RUN POWER and 3D3V AUX S5

Size

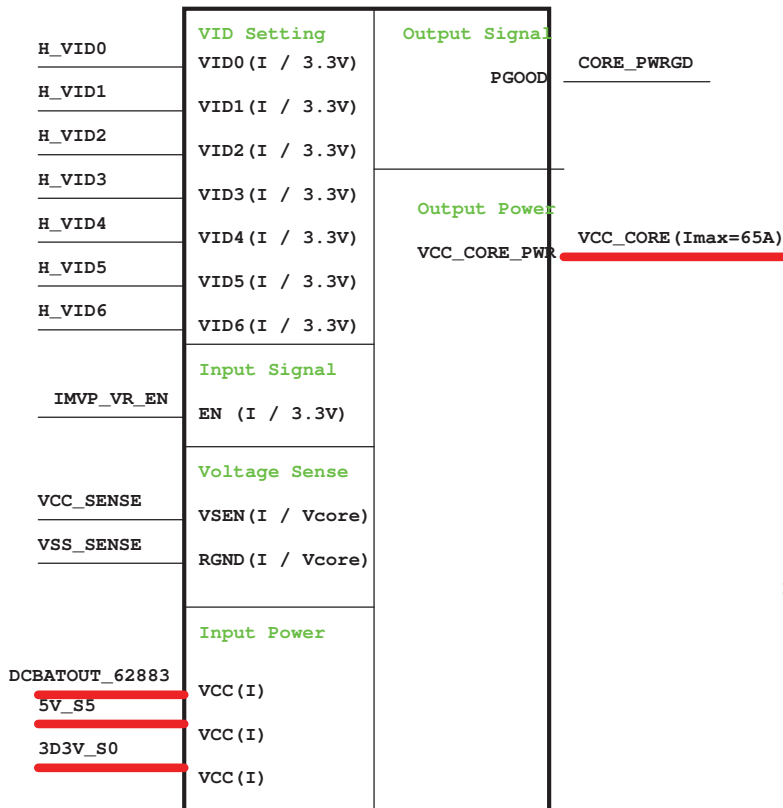
A3 **JM31-CP**

-3

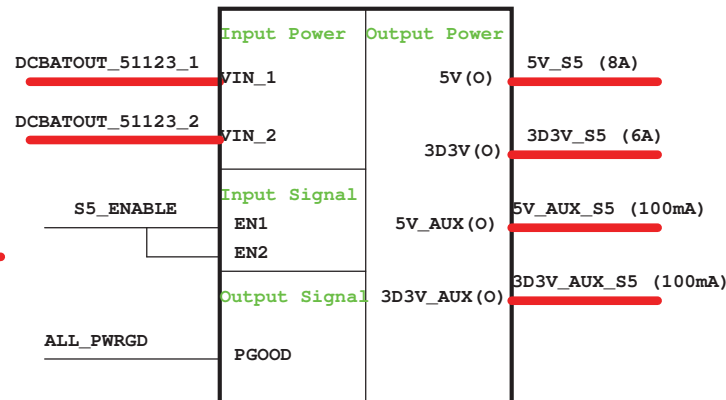
Date: Thursday, February 25, 2010

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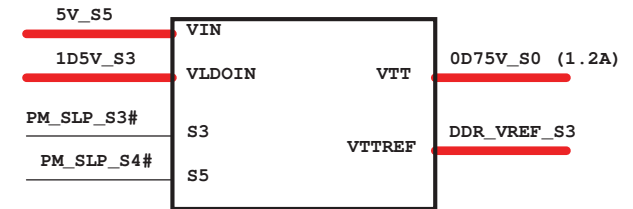
ISL62883 VCC_CORE



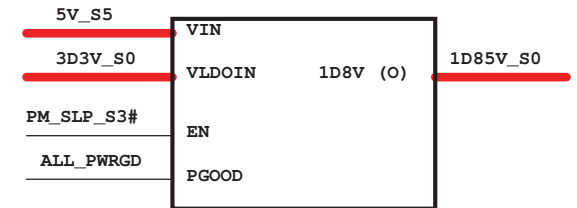
TPS51123 5V/3D3V



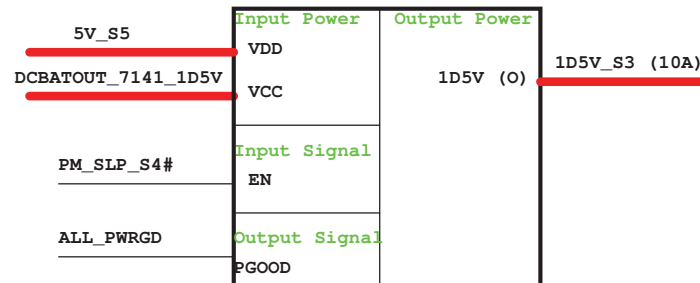
RT9026 0D75V_S0



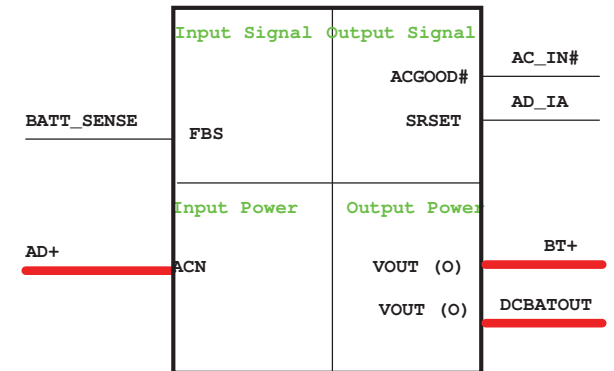
RT9025 1D8V



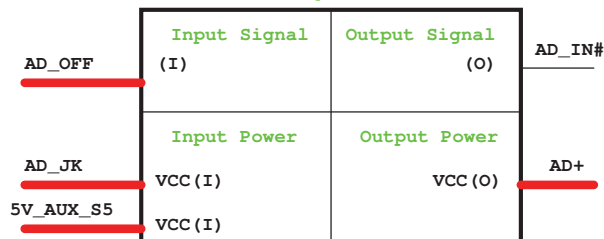
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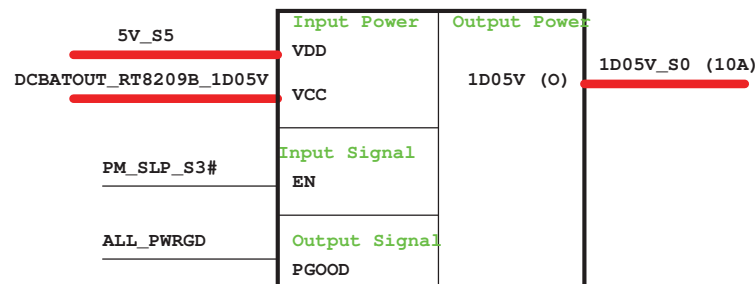
Charger BQ24745



Adapter



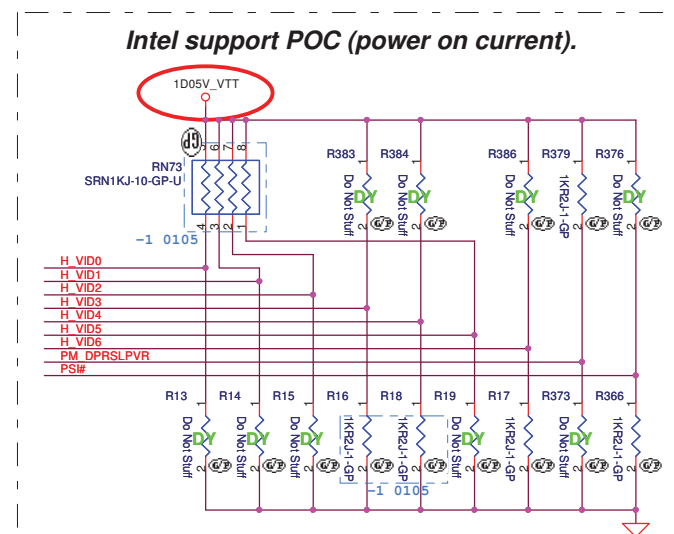
RT8209B 1D05V



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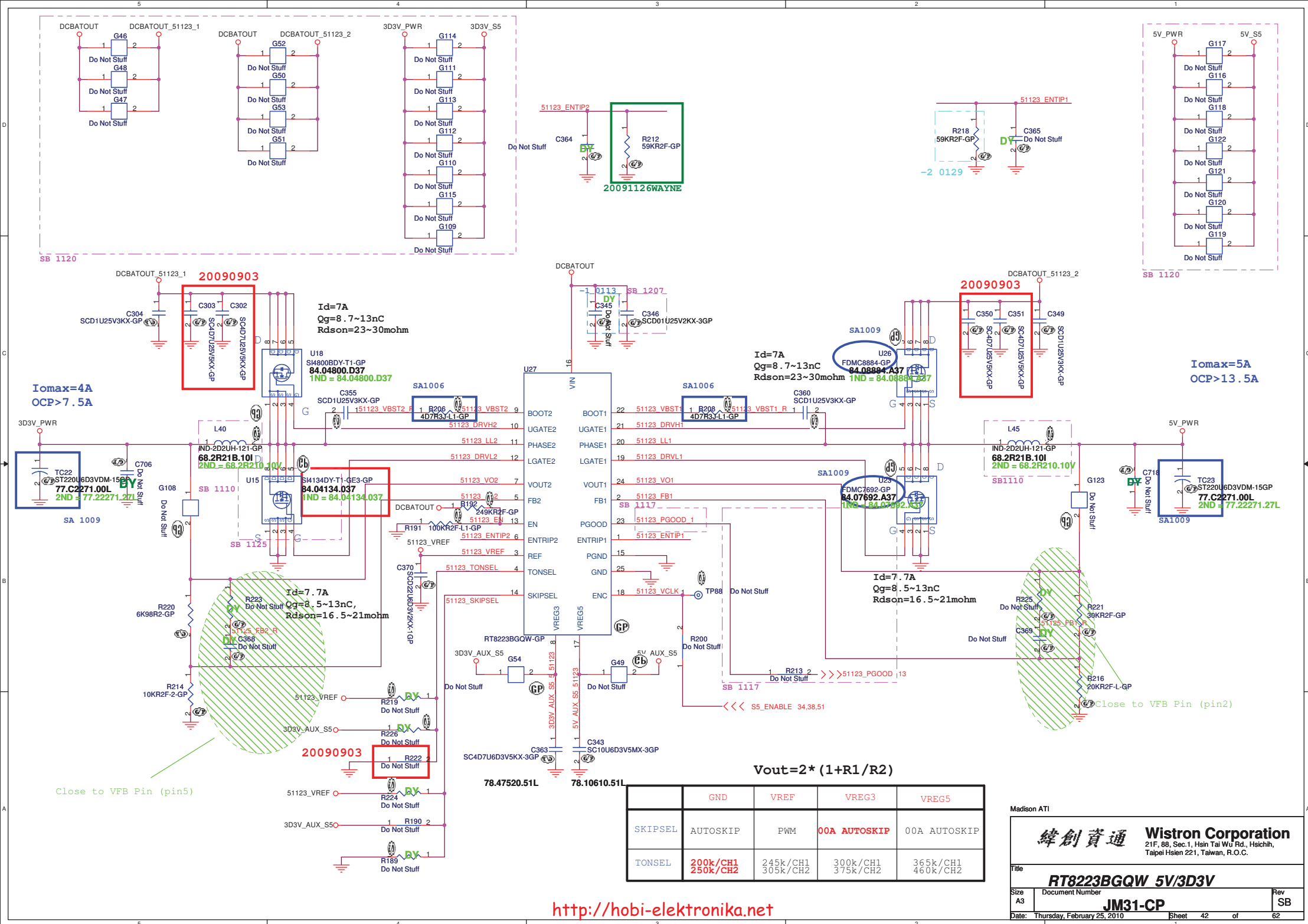
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Power Block Diagram		
Size	Document Number	Rev
	JM31-CP	SA
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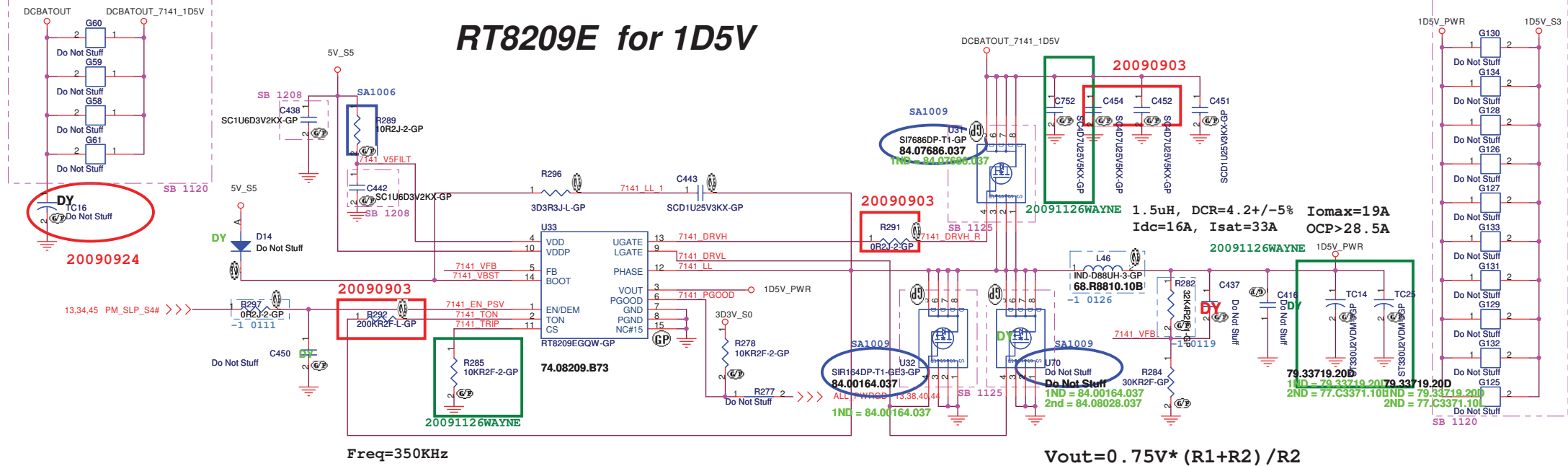
緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Size A3	Document Number JM31-CP	Rev -1
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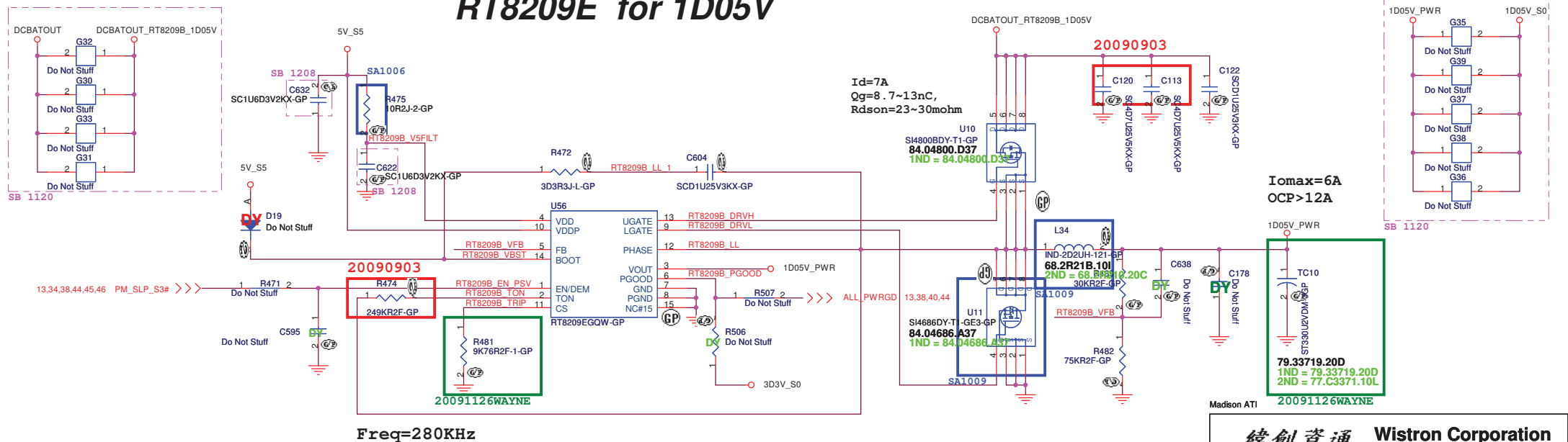
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RT8209E for 1D5V



RT8209E for 1D05V

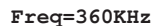


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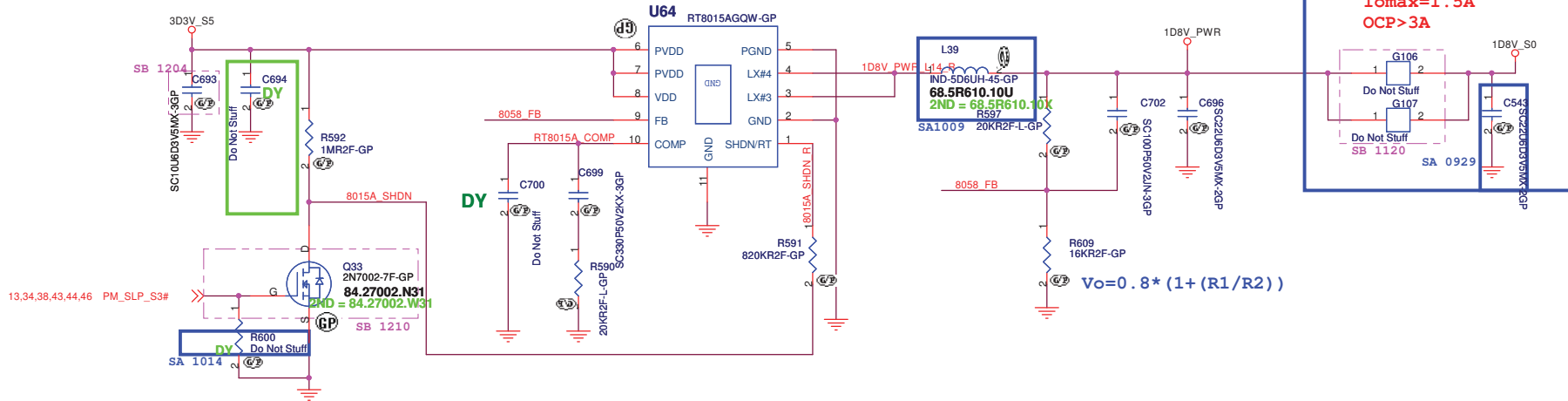
緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

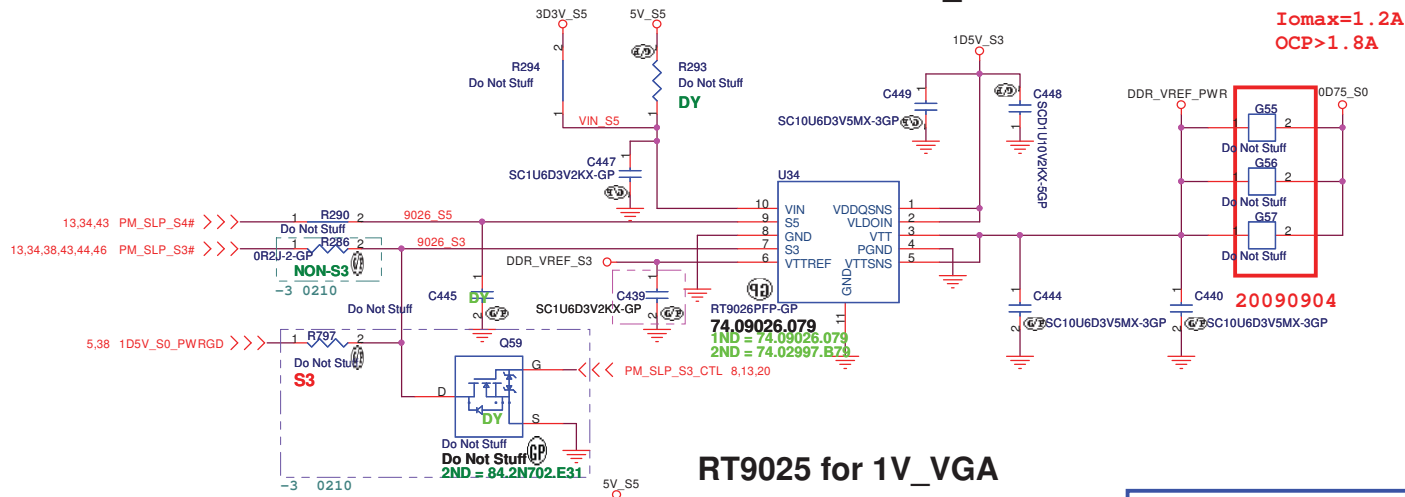
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Size	Document Number	JM31-CP	
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		SB	



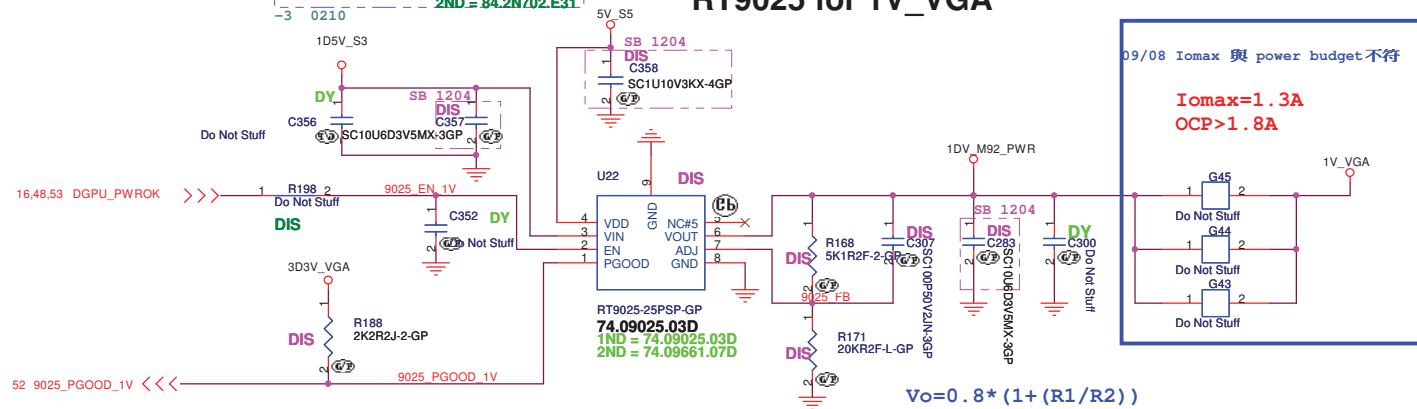
RT8015A for 1D8V_S0



09/08 add 3D3V_S5,R837,R836 RT9026 for 0D75V_S3



RT9025 for 1V_VGA


$$V_o = 0.8 * (1 + (R_1/R_2))$$

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Title

RT9025 1D8V 1V/RT9026 0D75

Size

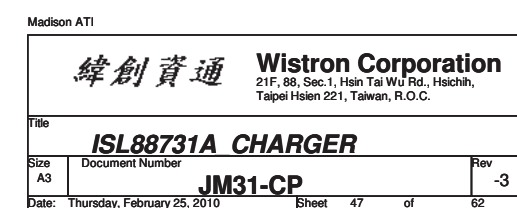
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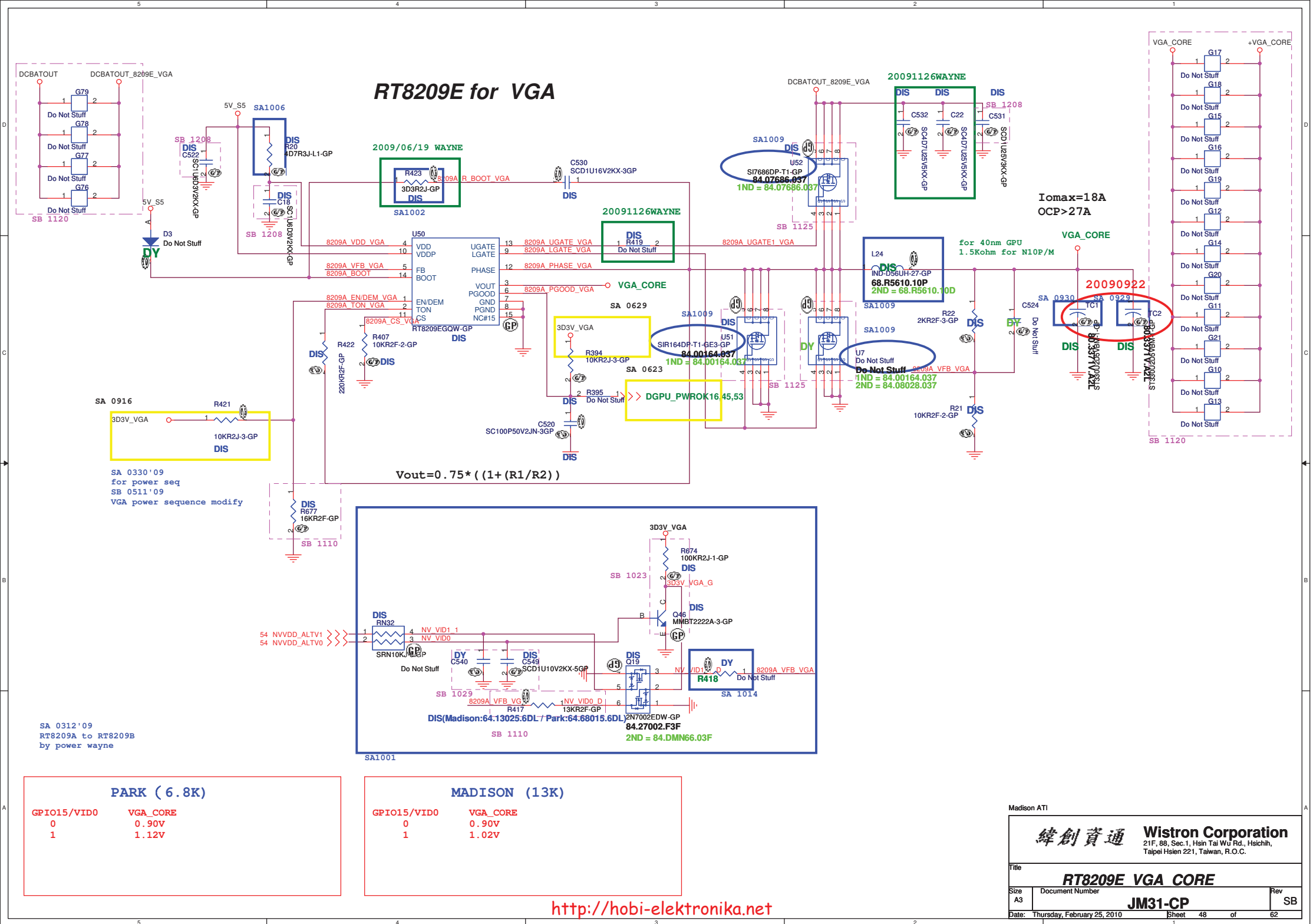
JM31-CP

Date: Thursday, February 25, 2010

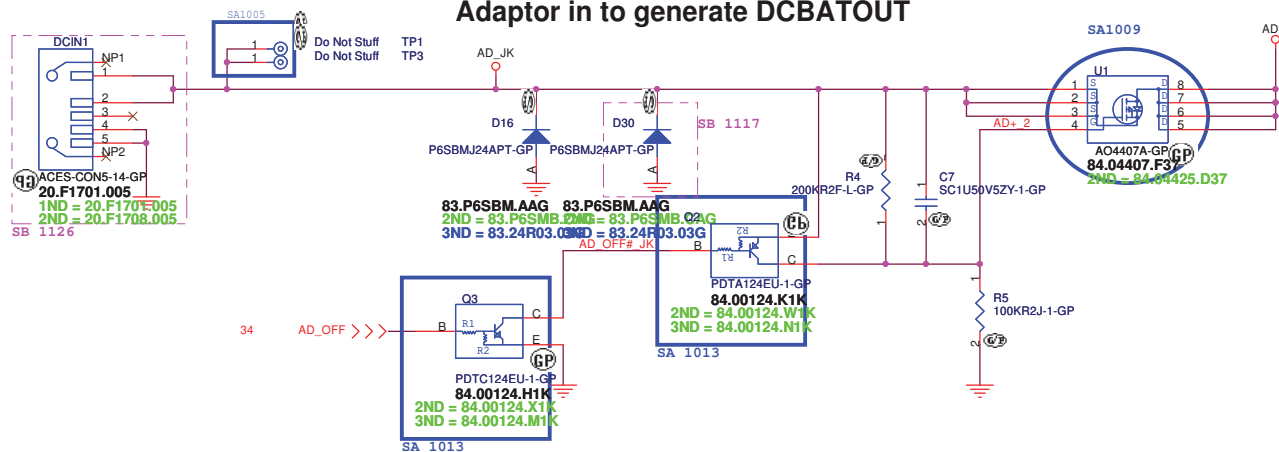
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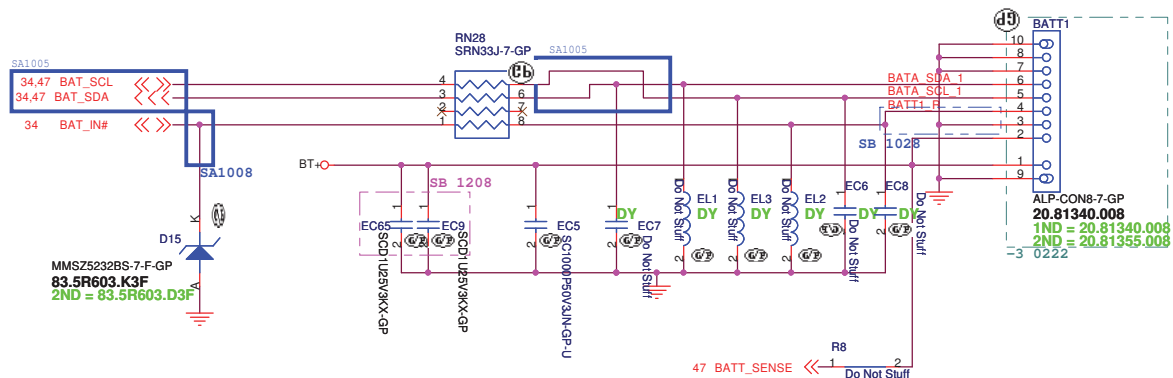


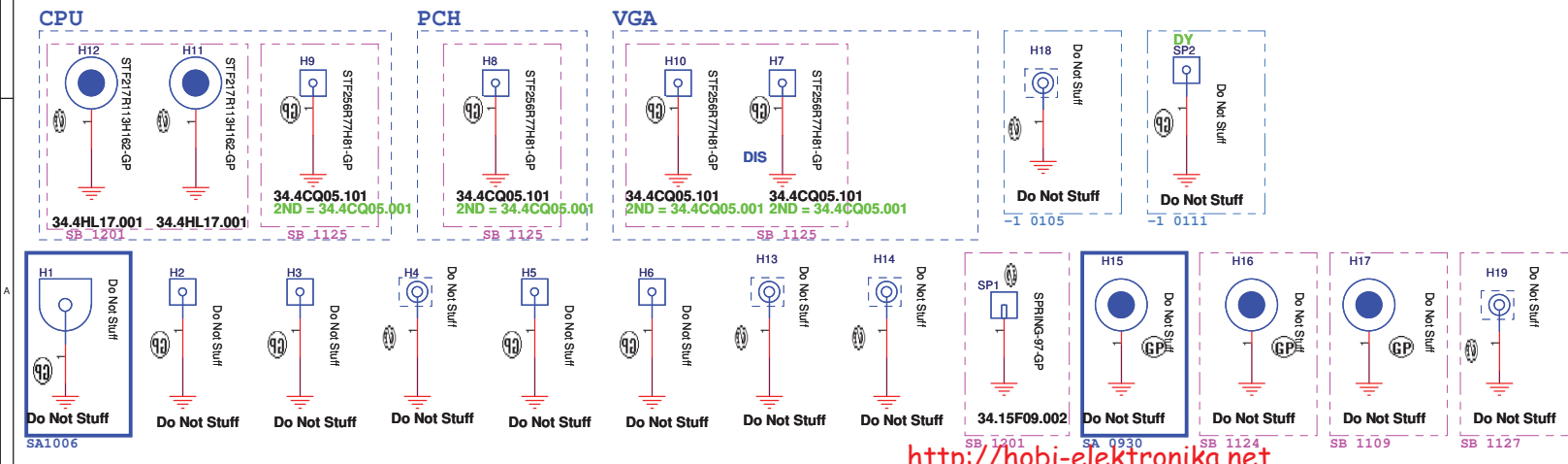
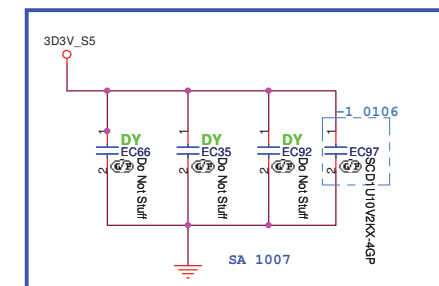
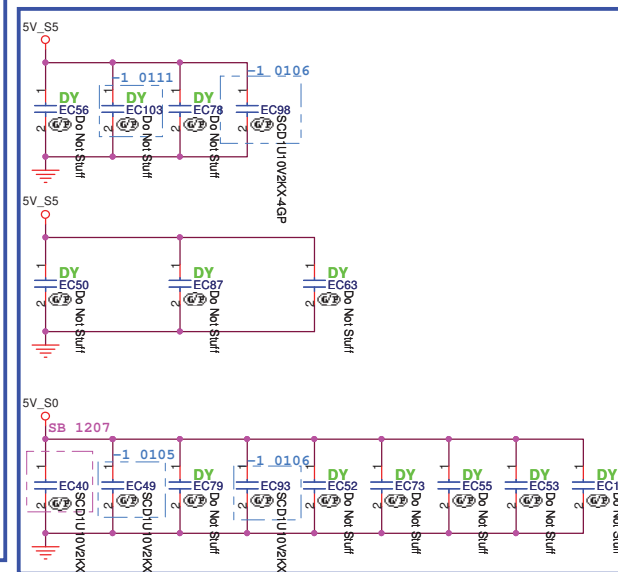
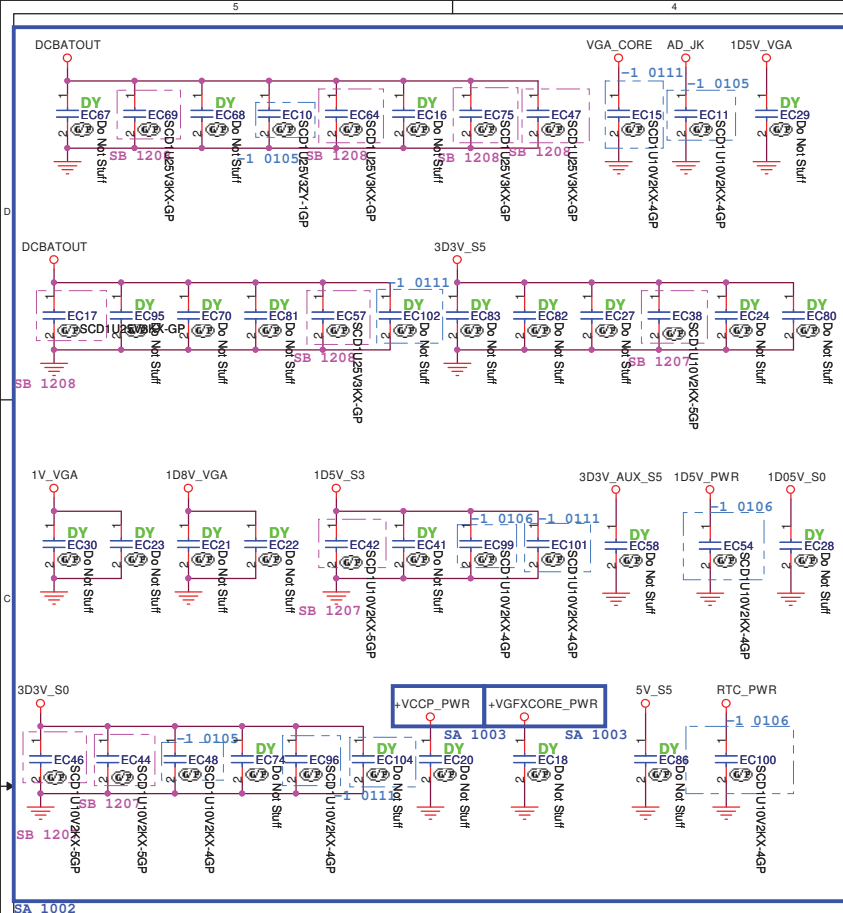


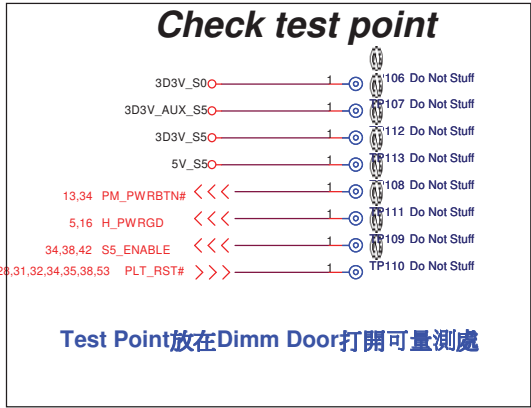
Adaptor in to generate DCBATOUT



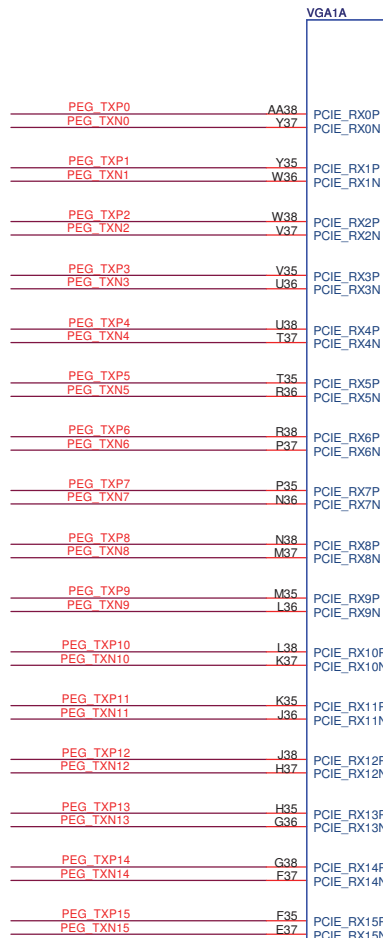
BATTERY CONNECTOR





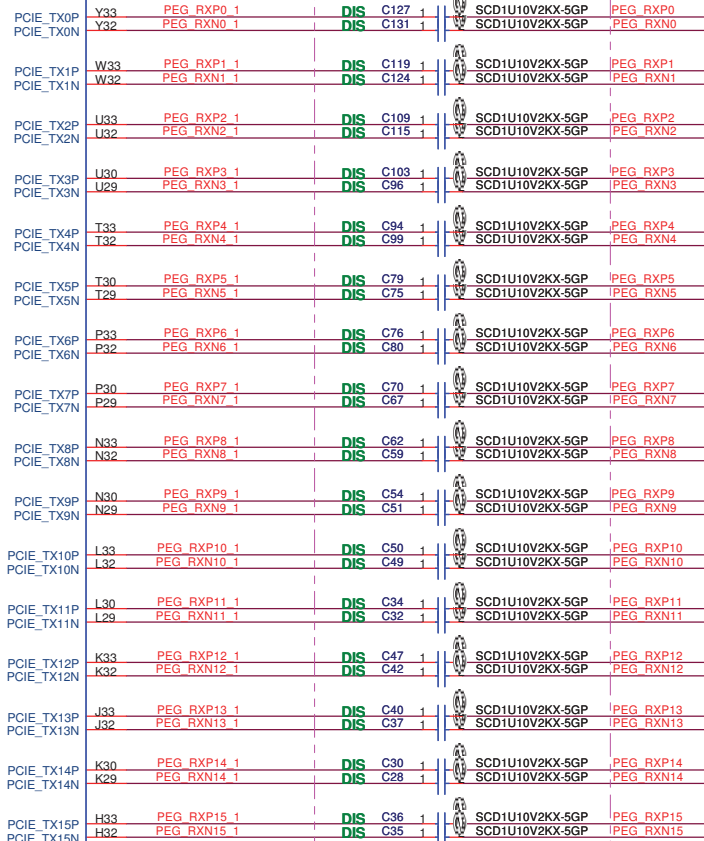


4 PEG_TXP[15..0] << PEG_TXP[15..0]
4 PEG_TXN[15..0] << PEG_TXN[15..0]

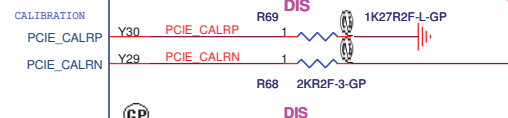
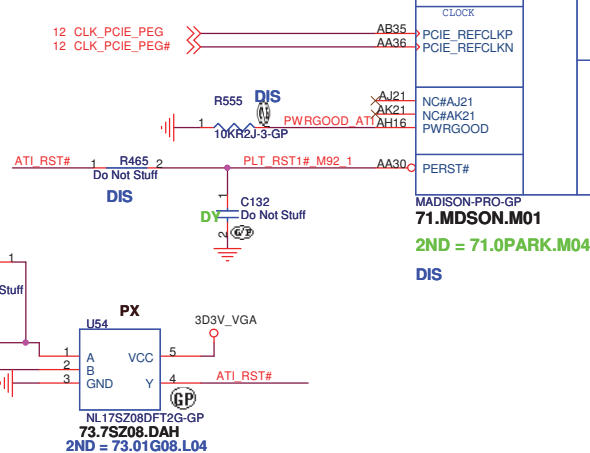


PCI EXPRESS INTERFACE

1 OF 8



4 PEG_RXP[15..0] << PEG_RXP[15..0]
4 PEG_RXN[15..0] << PEG_RXN[15..0]



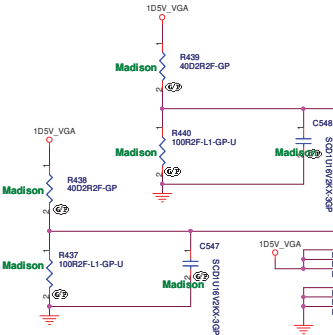
Madison ATI

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title Madison PCIE	
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For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R



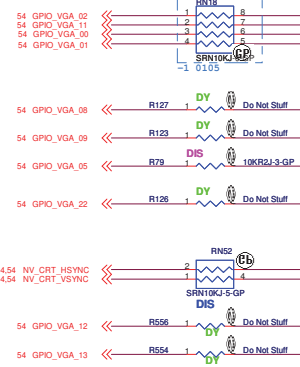
Madison: MEM_CALRP[0,2] signals are used.
Park: MEM_CALRP1 and MEM_CALRN1 are used.

71.MDS0N.M01
2ND = 71.0PARK.M04
DIS

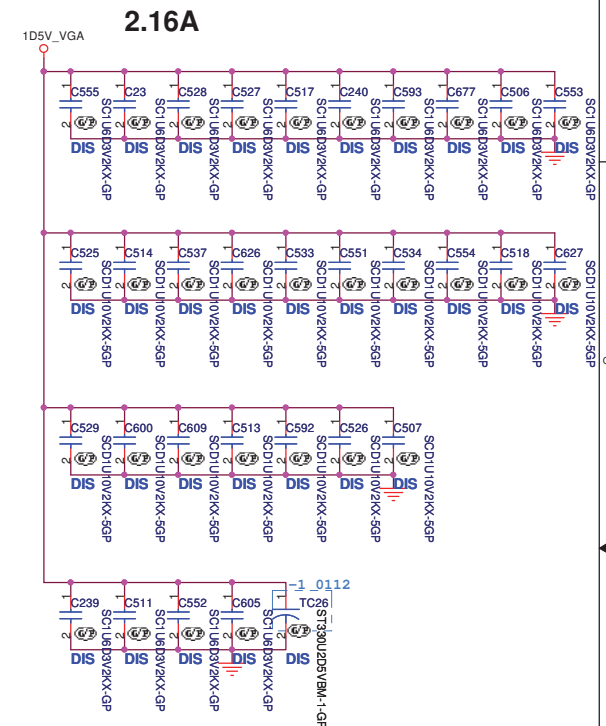
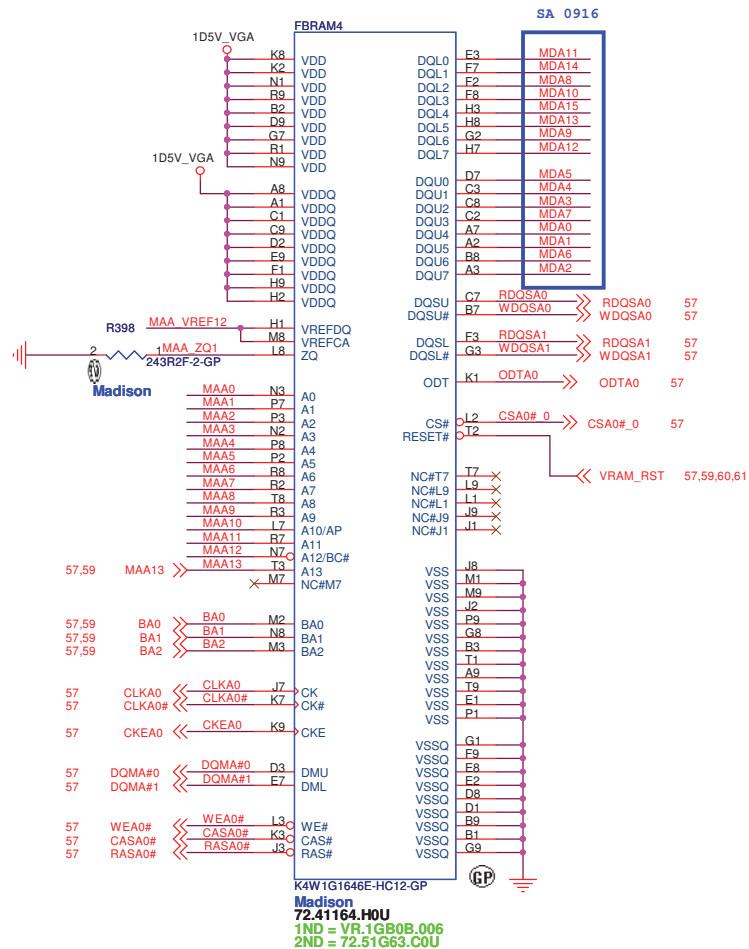
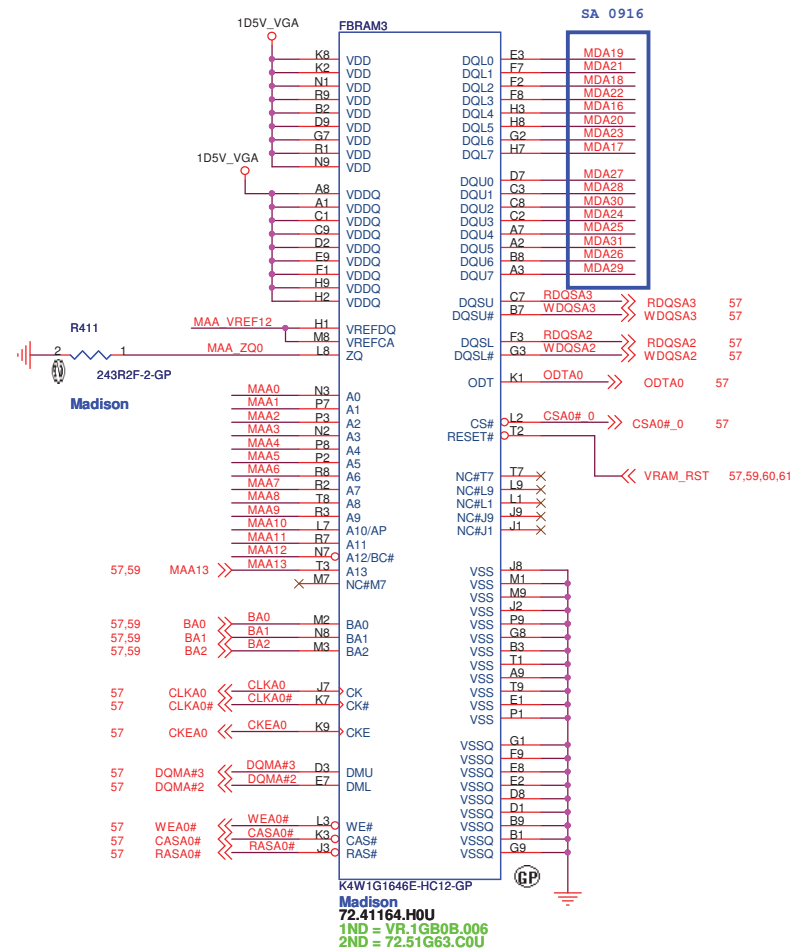
STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS
TX_PWRS_ENB (Internal PD)	GPIO0	PCI FULL TX OUTPUT SWING Transmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1, then Config[3:0] defines the ROM type if BIOS_ROM_EN=0, then Config[3:0] defines the primary memory aperture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
H2SYNC, GENERIC, GPIO2, GPIO21	

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1	
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number
128MB	x000	ST Microelectronics	M25P05A 0100
256MB	x001		M25P10A 0101
64MB	x010		M25P20 0101
32MB	x		M25P40 0101
512MB	x	Chingis (formerly PMC)	M25P80 0101
1GB	x		Pm25LV512A 0100
2GB	x		Pm25LV010A 0101
4GB	x		



DDR3



57,59 DQMA#[0..7] <<>

57,59 RDQSA#[0..7] <<>

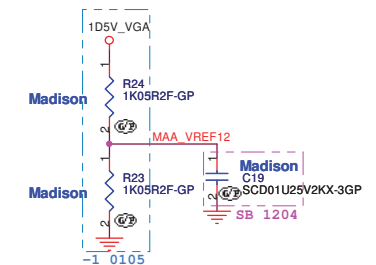
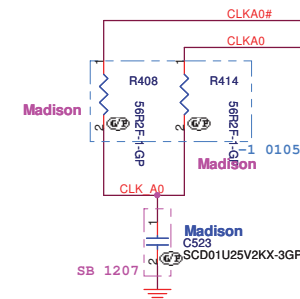
57,59 WDQSA#[0..7] <<>

57,59 MAA#[0..12] <<>

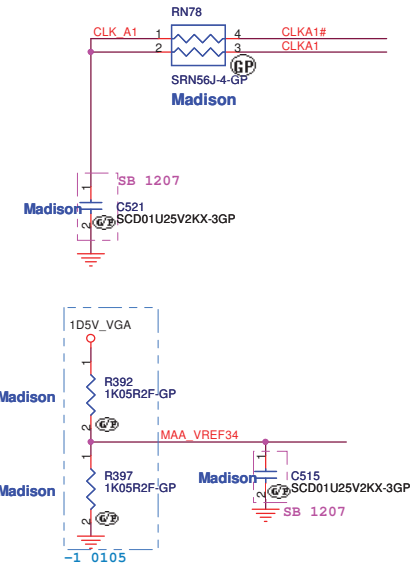
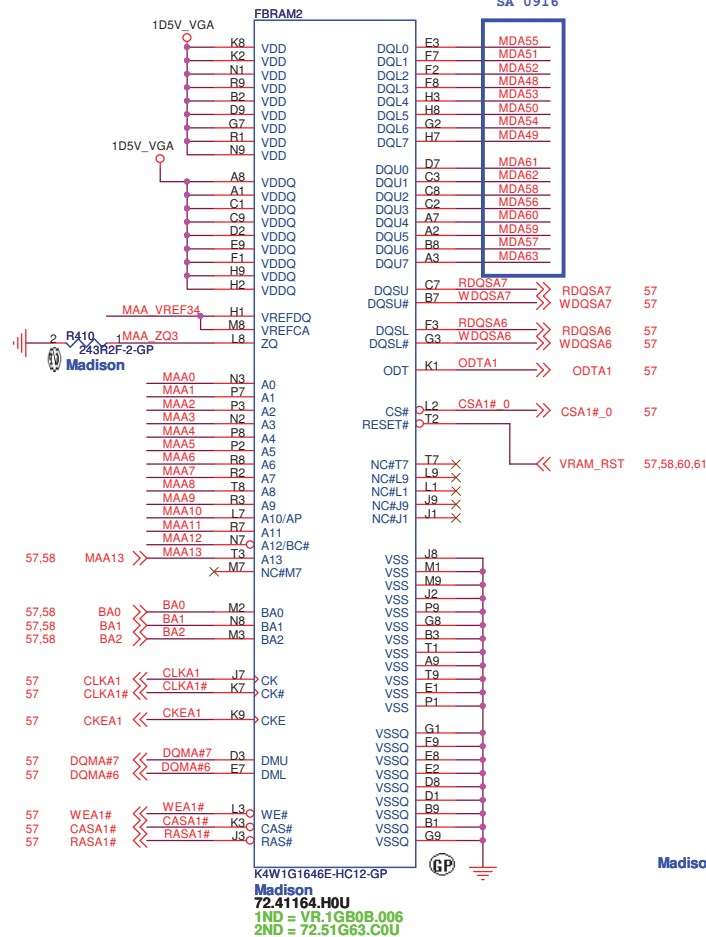
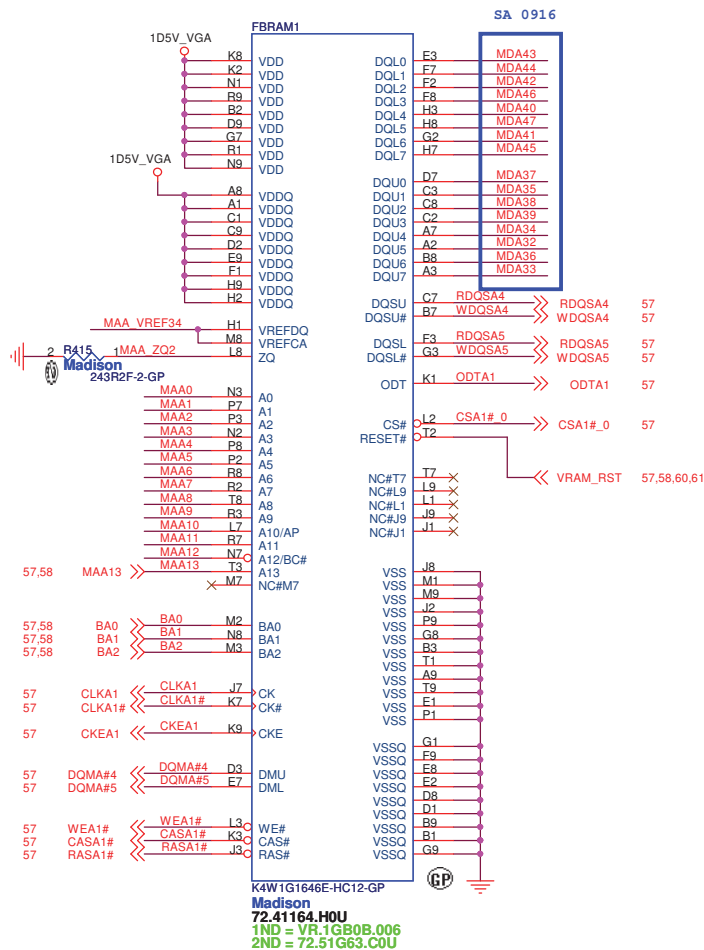
57,59 MDA#[0..63] <<>

SAMSUNG: 72.41164.H0U (VR.1GB0B.006)

HYNIX: 72.51G63.C0U (VR.1GB0G.004)



DDR3



SAMSUNG: 72.41164.H0U (VR.1GB0B.006)

HYNIX: 72.51G63.C0U (VR.1GB0G.004)

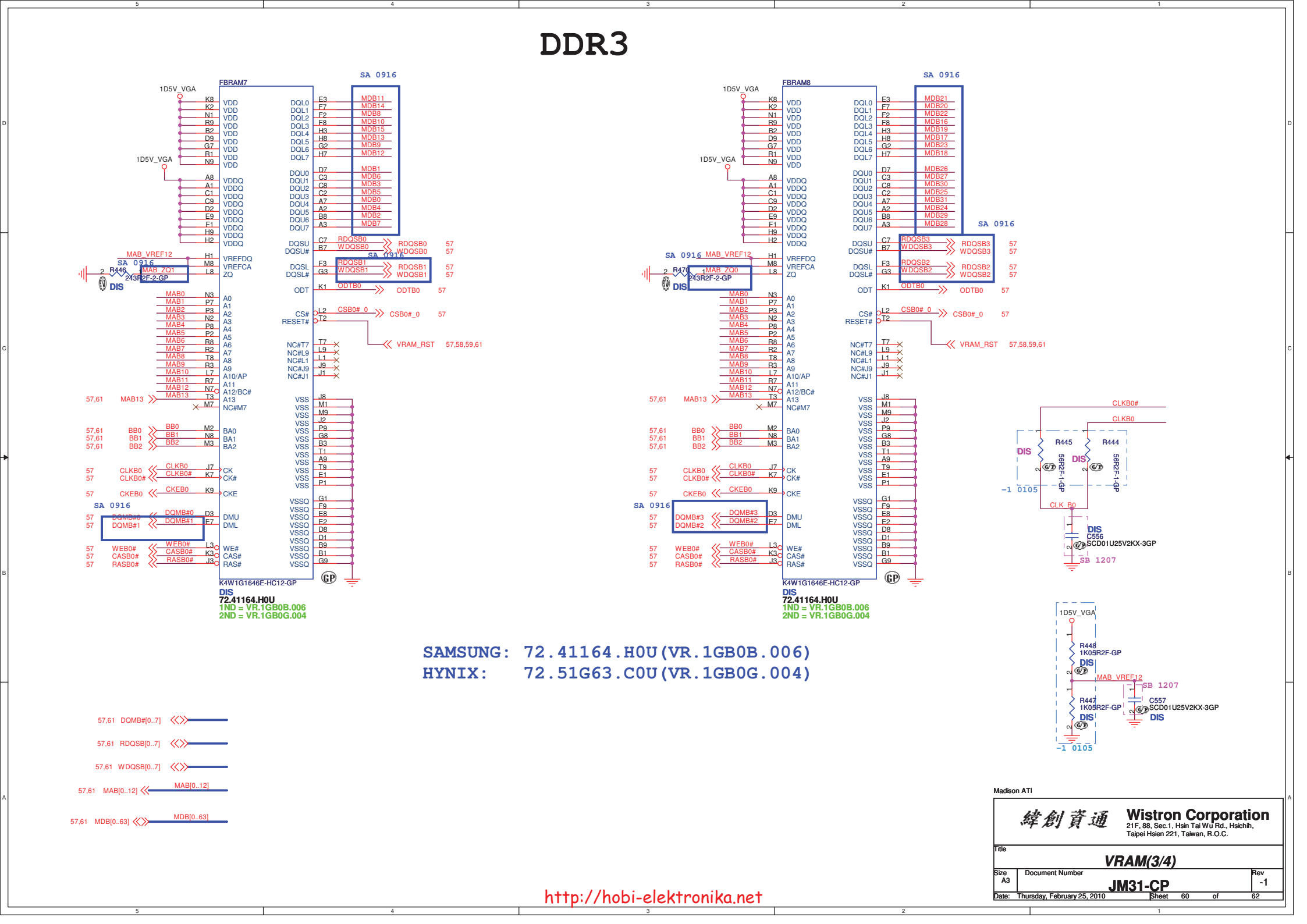
57,58 DQMA#0..7 <<>

57,58 RDQSA#0..7 <<>

57,58 WDQSA#0..7 <<>

57,58 MAA#0..12 <<>

57,58 MDA#0..63 <<>

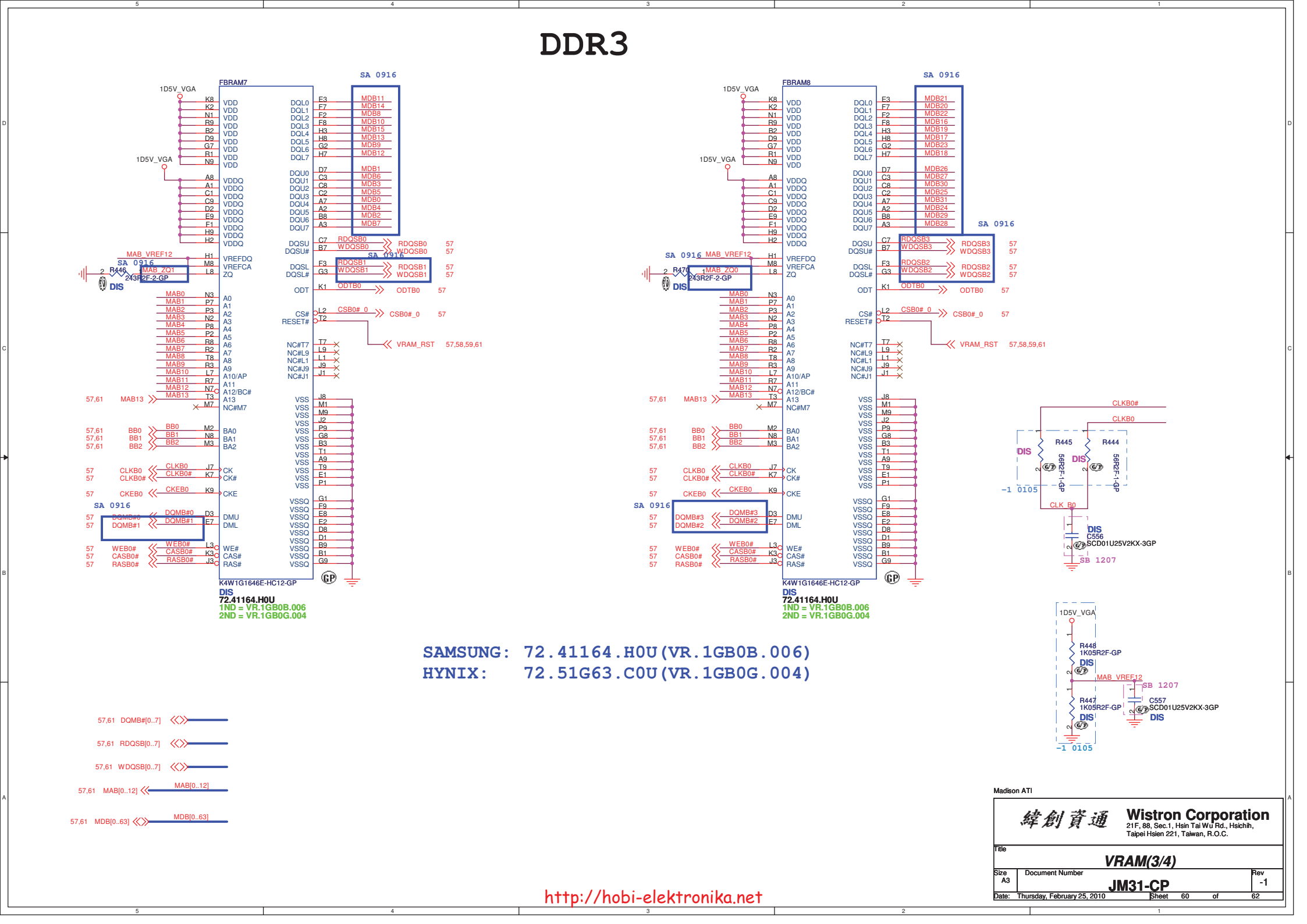
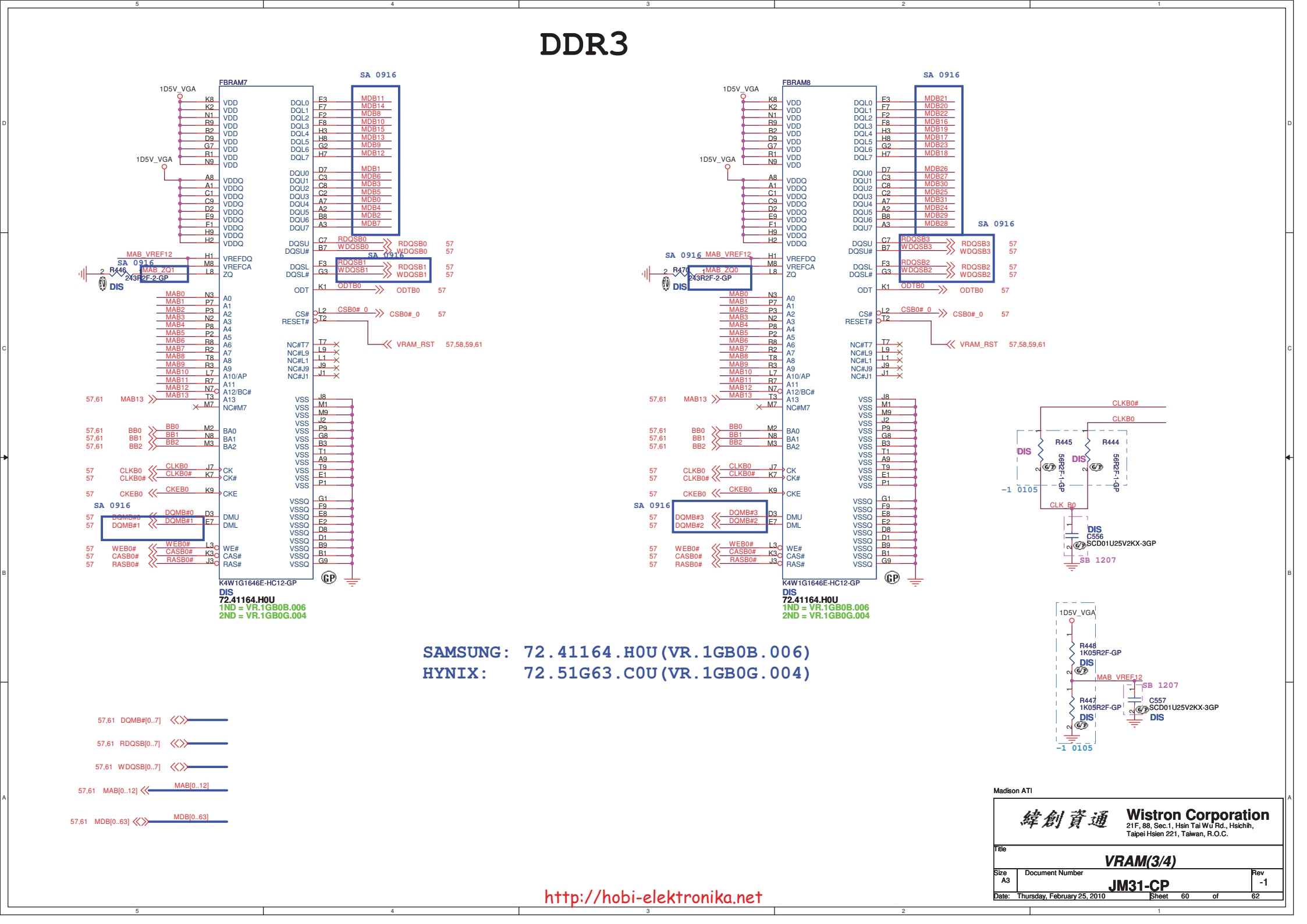
[illegible]

DDR3

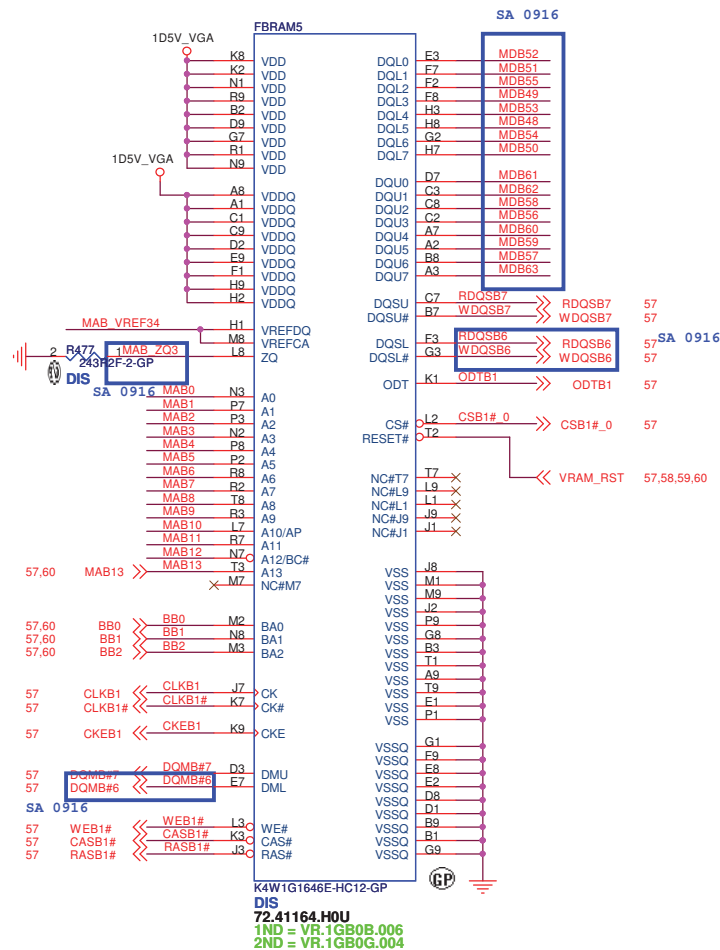
SAMSUNG: 72.41164.H0U (VR.1GB0B.006)
HYNIX: 72.51G63.C0U (VR.1GB0G.004)

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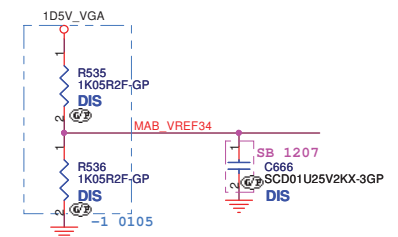
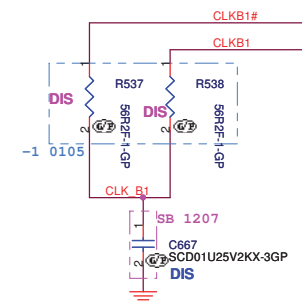
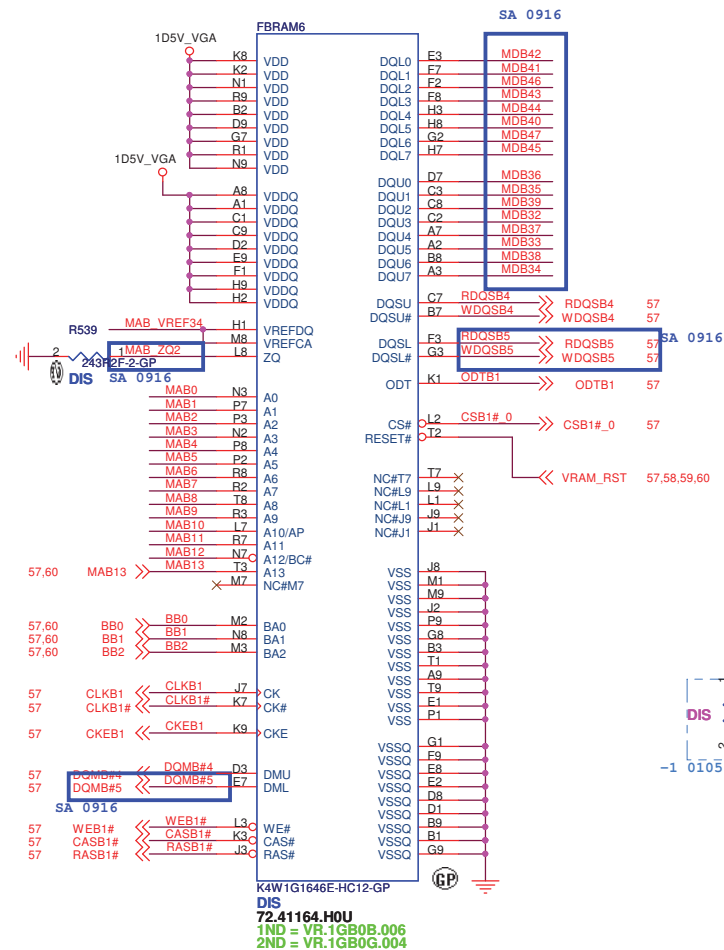


<http://hobi-elektronika.net>



SAMSUNG: 72.41164.H0U (VR.1GB0B.006)

HYNIX: 72.51G63.C0U (VR.1GB0G.004)



Madison AT1

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Taipei Hsien 221, Taiwan, R.O.C.

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