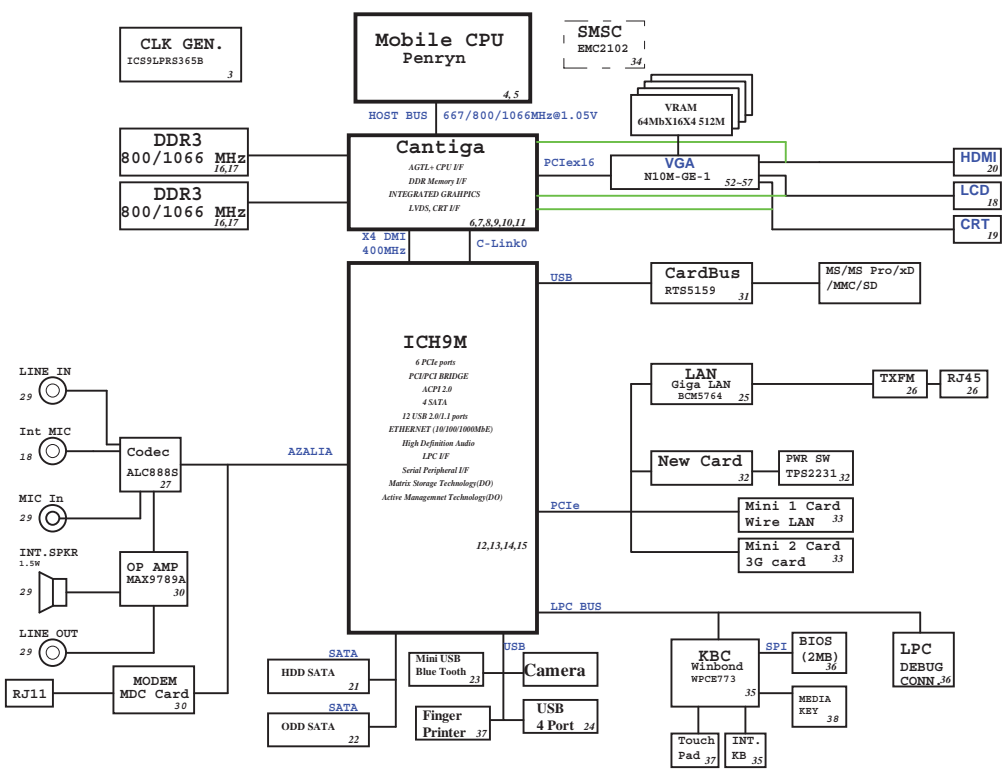


# JV50 Block Diagram

Project code: 91.4CG01.001  
PCB P/N : 48.4CG01.0SA  
REVISION : 08245-SA



PCB STACKUP	
TOP	L1
GND	L2
S	L3
S	L4
GND	L5
BOTTOM	L6

SYSTEM DC/DC	
ISL62392	42
INPUTS	OUTPUTS
DCRAT00T	SV_55 (6A) 10SV_55 (7A) SV_ADR_55 10SV_ADR_55

SYSTEM DC/DC	
TPS51124	43
INPUTS	OUTPUTS
DCRAT00T	10SV_50 (9A) 10SV_53 (12A)

SYSTEM DC/DC	
RT9026	44
INPUTS	OUTPUTS
10SV_53	D0R_VREF_53 (1.2A)

SYSTEM DC/DC	
RT9018	44
INPUTS	OUTPUTS
10SV_53	10SV_50 (2A)

SYSTEM DC/DC	
TPS51117	45
INPUTS	OUTPUTS
DCRAT00T	PRVDD (4A)

CHARGER	
ISL88731A	47
INPUTS	OUTPUTS
DCRAT00T	BT+

CPU DC/DC	
ISL6266A	41
INPUTS	OUTPUTS
DCRAT00T	VCC_CORE (3A)

VGA CORE	
RT6202A	47
INPUTS	OUTPUTS
DCRAT00T	VGA_CORE (1A)

GFXCORE	
ISL6263A	46
INPUTS	OUTPUTS
DCRAT00T	VCC_GFXCORE (1A)

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Wistron Corporation

200, No. 1, Sec. 1, Hsinchu, Taiwan, R.O.C.

Block Diagram

JV50

SB

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A

B

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIe config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIe config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space) . Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	BOOT BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via BOOT BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10) . GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage Reversal, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal, Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of NPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature) . The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. XOR Chain testing.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

C

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSILPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

D

CantigaD Chipset and ICH9M I/O Controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	ITPM Host Interface	0= The ITPM Host Interface is enabled(Note2) 1=The ITPM Host Interface is disabled(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIe Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default) Lane Numbered in order
CFG10	PCIe Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes x4 mode[MCH -> ICH]: (3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]: (3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	0 = Only Digital Display Port or PCIe is operational (Default) 1 =Digital Display Port and PCIe are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIe disabled

NOTE:  
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.  
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.  
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

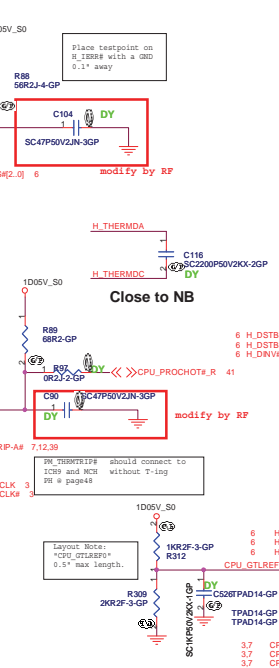
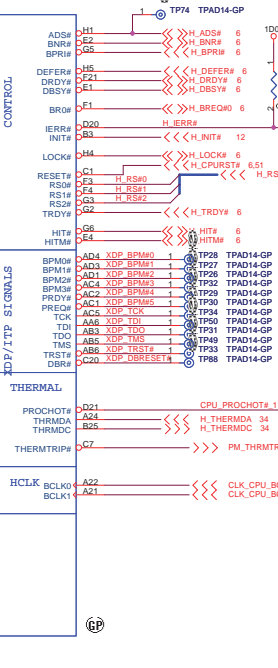
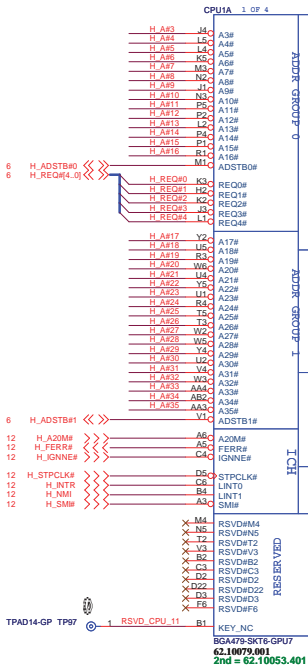
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JV50

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Size	Document Number		Rev
A3	<b>JV50</b>		<b>SB</b>
Date: Thursday, January 08, 2009		Sheet 2 of	60



6 H\_ADSTB#3 <<> H\_ADSTB#3



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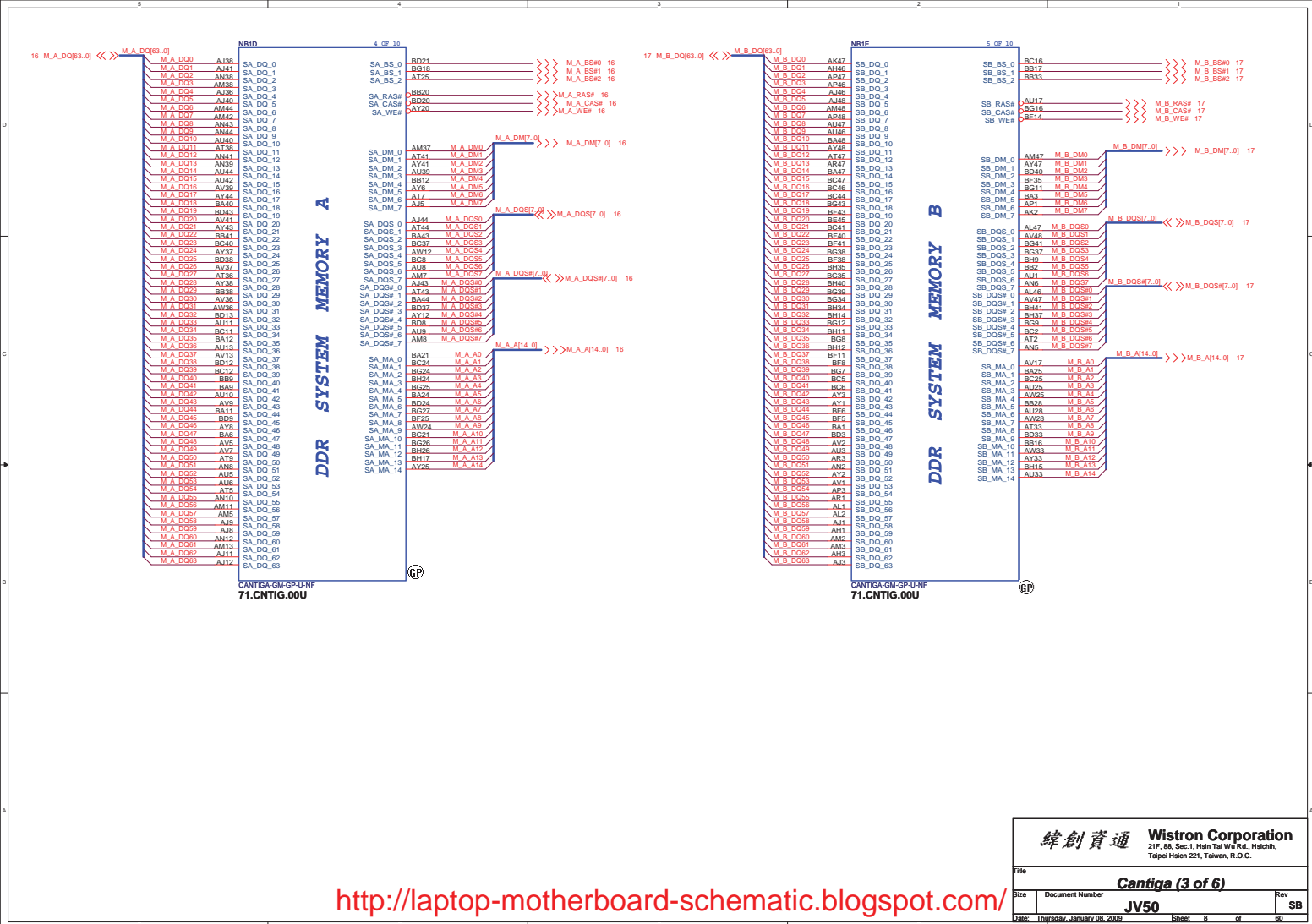
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File CPU (1 of 2)  
Date: Thursday, January 06, 2009 Sheet 4 of 50



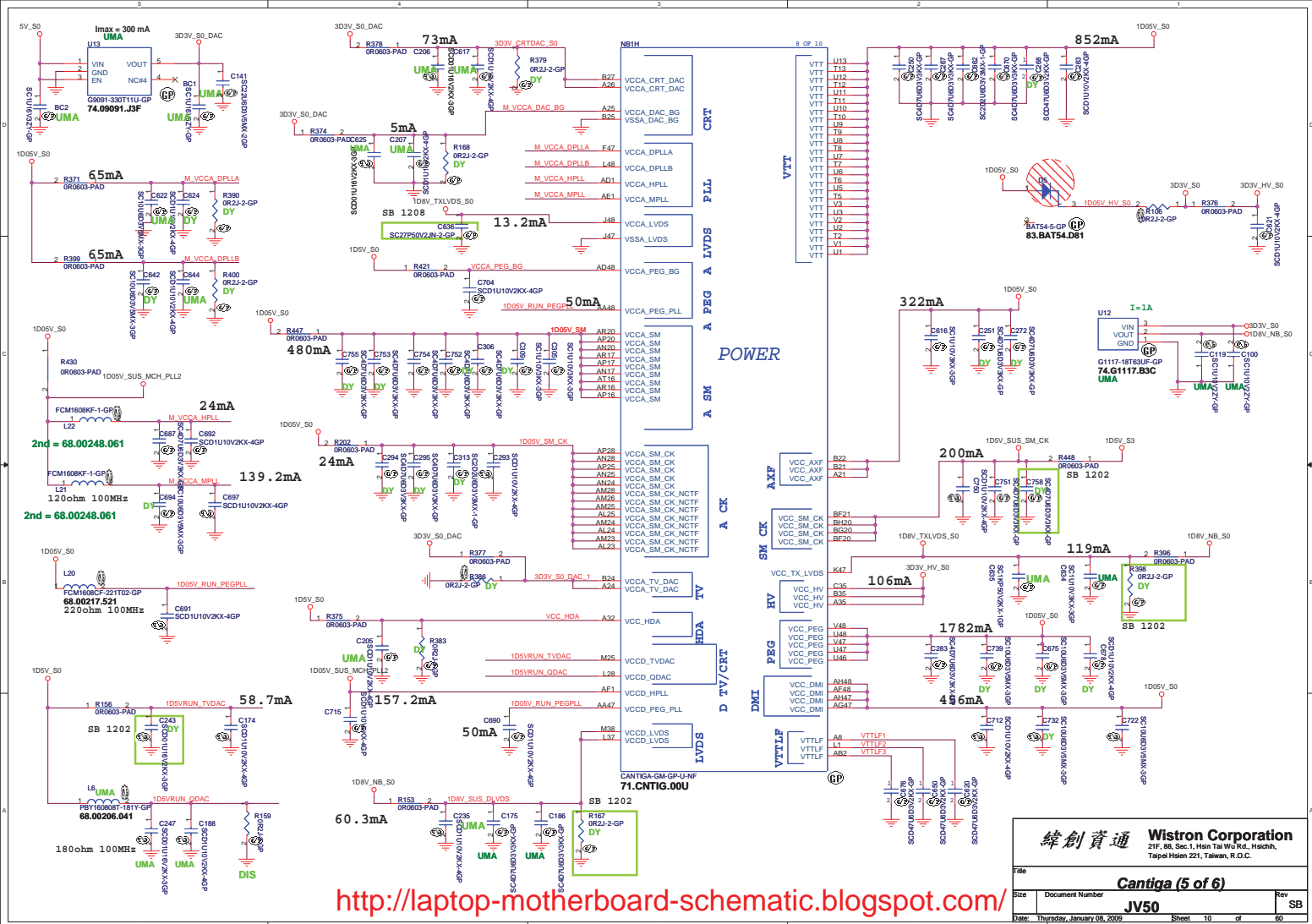


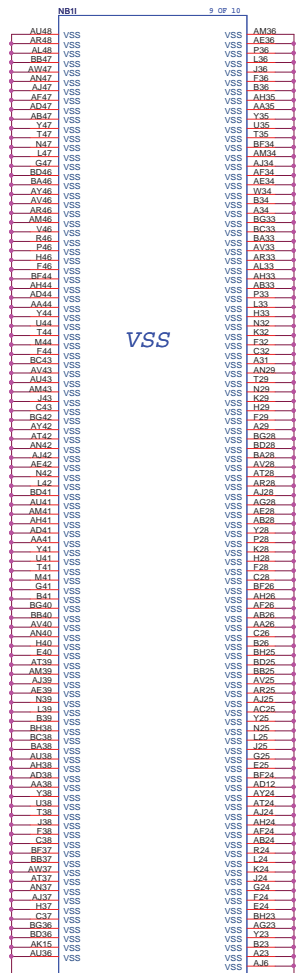




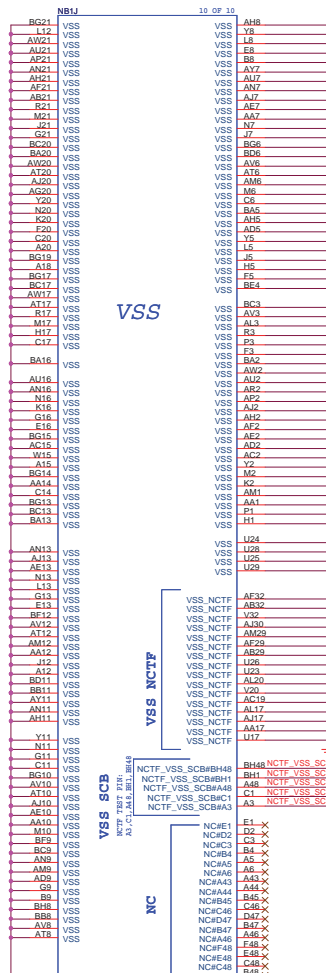








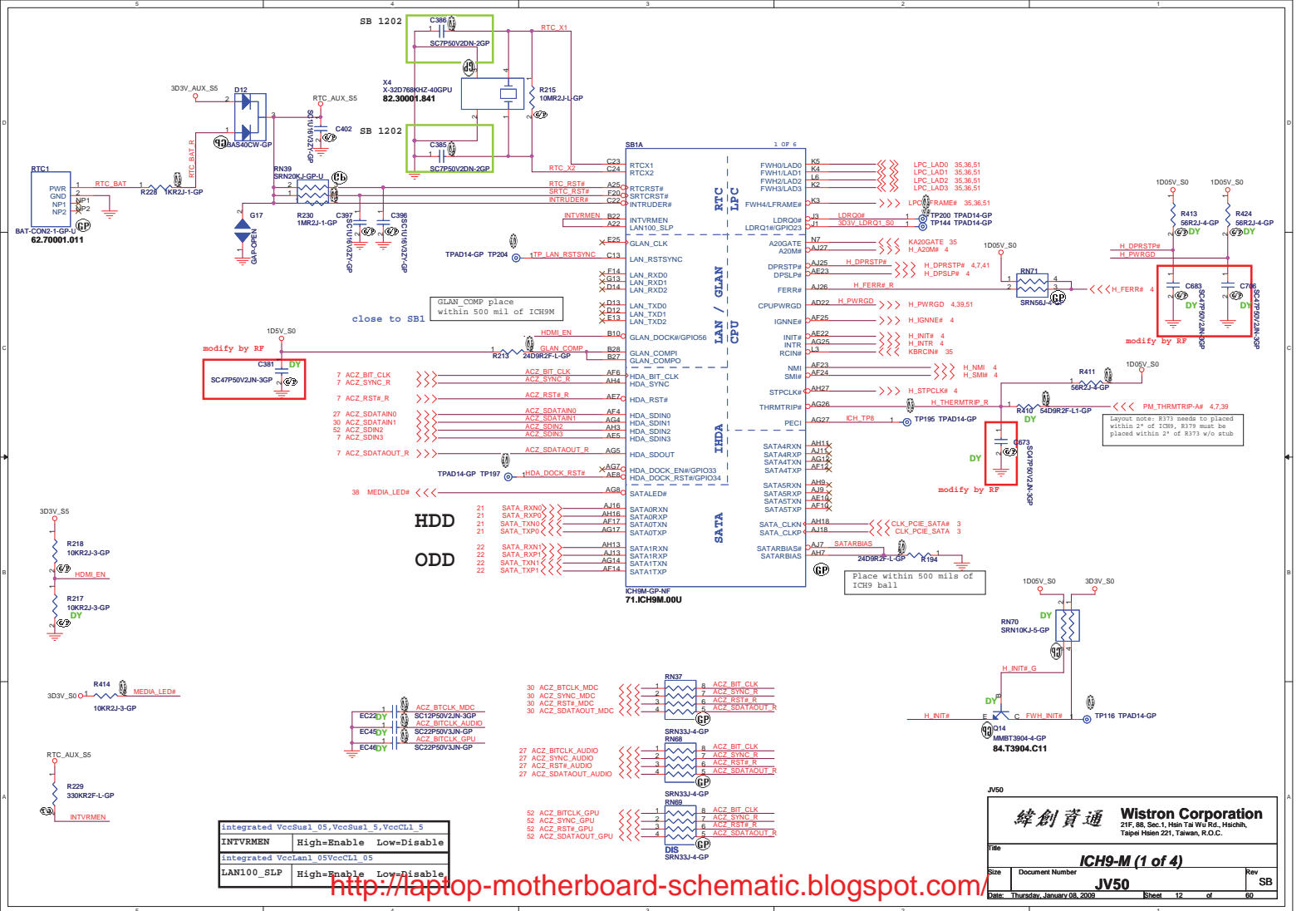
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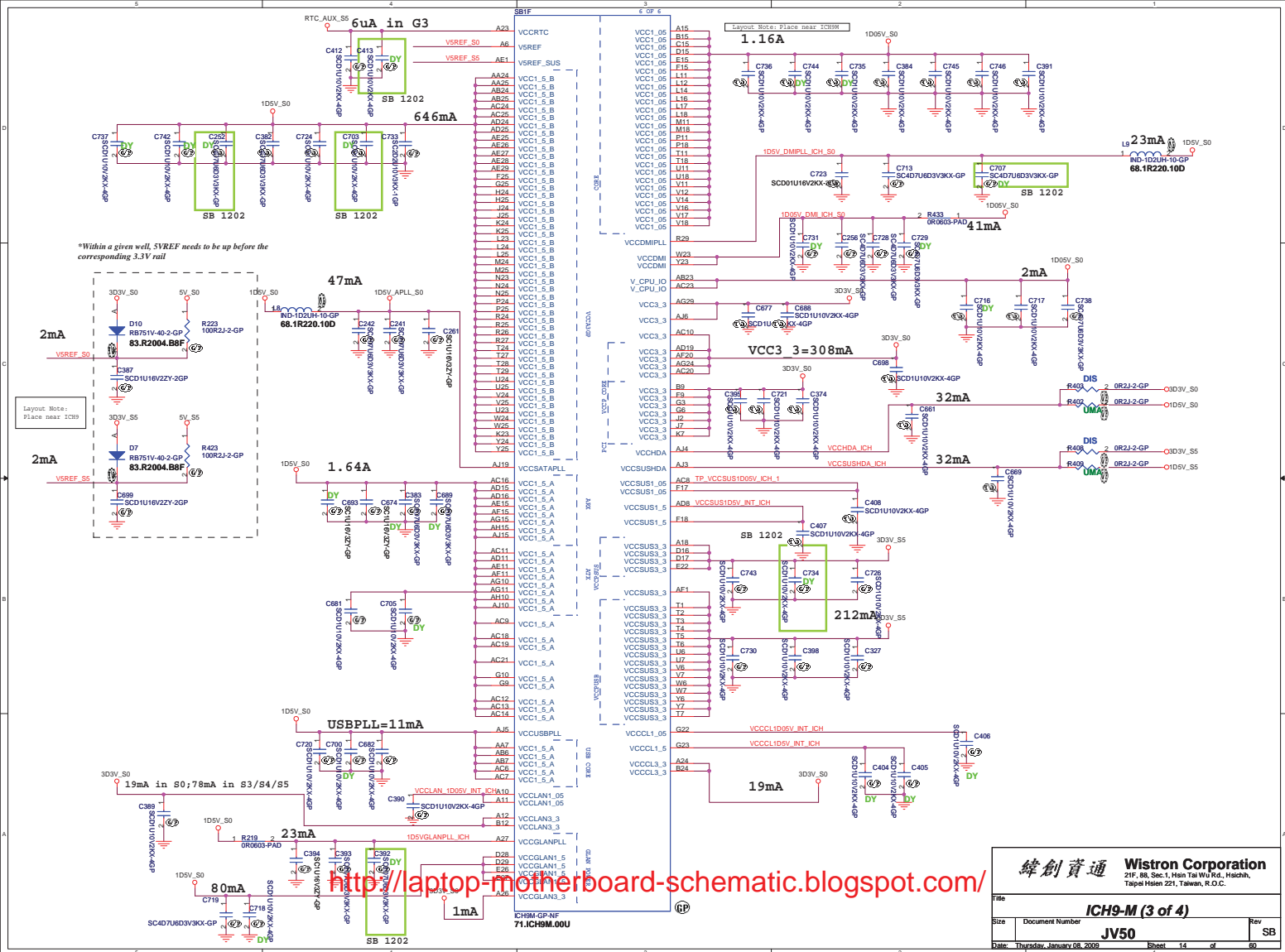
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71.CNTIG.000

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Size	Document Number
Date	Thursday, January 06, 2009
Sheet	11 of 60
Rev	SB



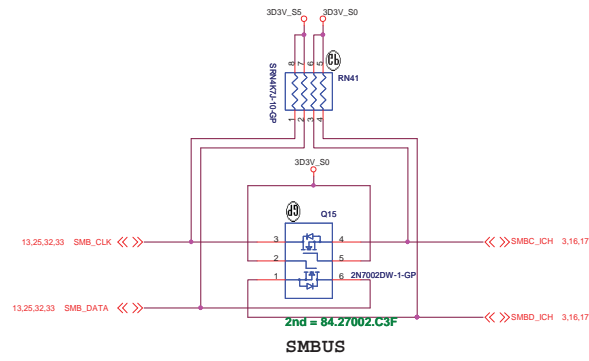




AA26	VSS	H5
AA27	VSS	J23
AA3	VSS	J26
AA6	VSS	J27
AB1	VSS	AC22
AA23	VSS	K28
AB28	VSS	K29
AB29	VSS	L13
AB4	VSS	L15
AB5	VSS	L2
AC17	VSS	L26
AC26	VSS	L27
AC27	VSS	L6
AC3	VSS	L7
AD1	VSS	M12
AD10	VSS	M13
AD12	VSS	M14
AD13	VSS	M15
AD14	VSS	M16
AD17	VSS	M17
AD18	VSS	M23
AD21	VSS	M28
AD28	VSS	M29
AD29	VSS	N11
AD4	VSS	N12
AD5	VSS	N13
AD6	VSS	N14
AD7	VSS	N15
AD9	VSS	N16
AE12	VSS	N17
AE13	VSS	N18
AE14	VSS	N26
AE16	VSS	N27
AE17	VSS	P12
AE2	VSS	P13
AE20	VSS	P14
AE4	VSS	P15
AE3	VSS	P16
AE4	VSS	P17
AE6	VSS	P2
AE9	VSS	P23
AF13	VSS	P28
AF16	VSS	P29
AF18	VSS	P4
AF22	VSS	P7
AH26	VSS	R11
AF26	VSS	R12
AF27	VSS	R13
AF5	VSS	R14
AF7	VSS	R15
AF9	VSS	R16
AG13	VSS	R17
AG16	VSS	R18
AG18	VSS	R26
AG20	VSS	T12
AG23	VSS	T13
AG3	VSS	T14
AG6	VSS	T15
AG9	VSS	T16
AH12	VSS	T17
AH14	VSS	T23
AH17	VSS	B26
AH19	VSS	U12
AH2	VSS	U13
AH22	VSS	U14
AH25	VSS	U15
AH28	VSS	U16
AH5	VSS	U17
AH8	VSS	AD23
AJ12	VSS	U26
AJ14	VSS	U27
AJ17	VSS	U3
AB	VSS	V1
B11	VSS	V13
B14	VSS	V15
B17	VSS	V23
B2	VSS	V28
B20	VSS	V29
B23	VSS	V4
B5	VSS	V5
B8	VSS	W26
C26	VSS	W27
C27	VSS	W3
E11	VSS	Y1
E14	VSS	Y28
E18	VSS	Y29
E2	VSS	Y4
E21	VSS	Y5
E24	VSS	AG28
ES	VSS	AH6
F8	VSS	AF2
F8	VSS	B25
F29	VSS	
G12	VSS	
G14	VSS	
G18	VSS	
G21	VSS	
G24	VSS	
G26	VSS	
G27	VSS	
G8	VSS	
H2	VSS	
H23	VSS	
H28	VSS	
H29	VSS	

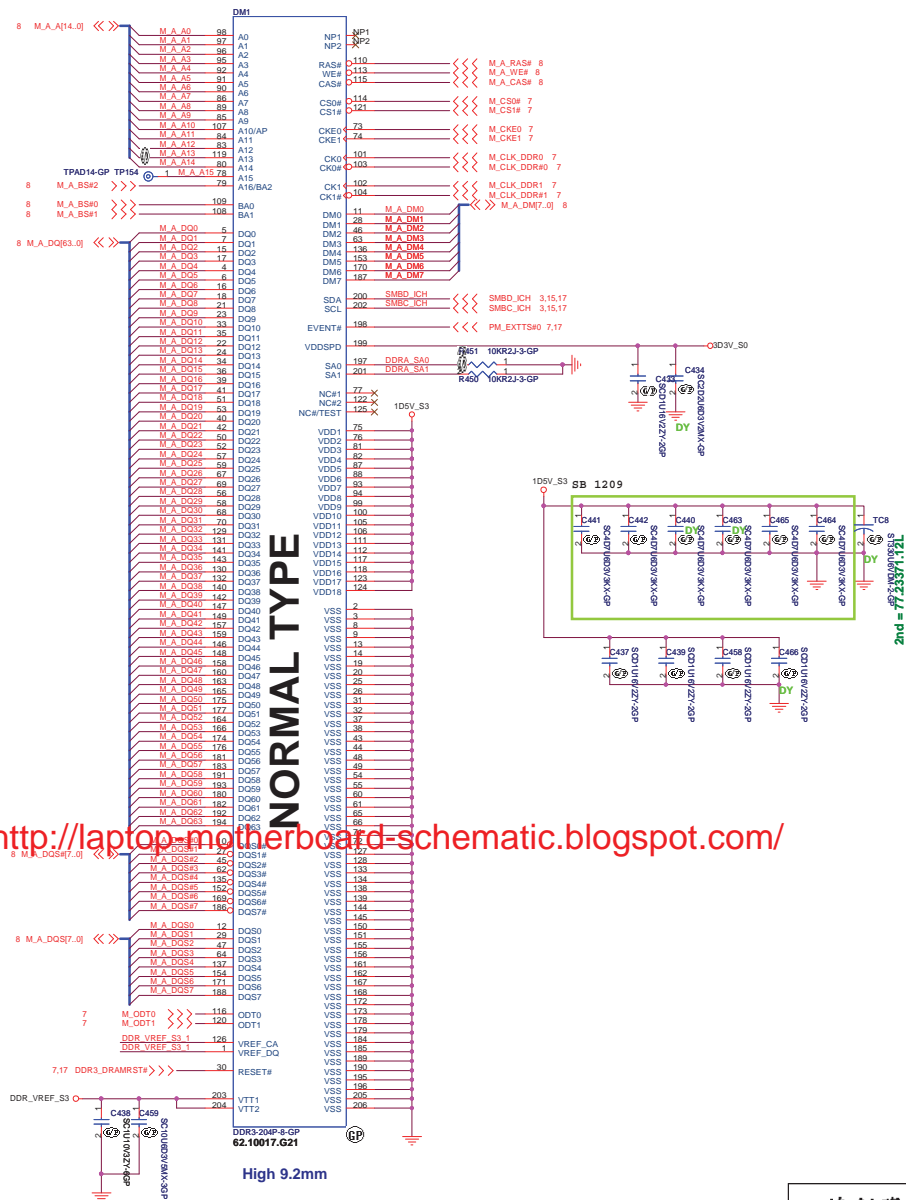
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NCTF_VSS#A2	A2	TP A2	1	TP151	TPAD14-GP
NCTF_VSS#B1	B1	TP B1	1	TP147	TPAD14-GP
NCTF_VSS#A28	A28	TP A28	1	TP149	TPAD14-GP
NCTF_VSS#B29	B29	TP B29	1	TP150	TPAD14-GP
NCTF_VSS#A1	A1	TP A1	1	TP148	TPAD14-GP
NCTF_VSS#A2	A2	TP A2	1	TP120	TPAD14-GP
NCTF_VSS#A1	A1	TP A1	1	TP121	TPAD14-GP
NCTF_VSS#A28	A28	TP A28	1	TP130	TPAD14-GP
NCTF_VSS#A1	A1	TP A1	1	TP119	TPAD14-GP
NCTF_VSS#A29	A29	TP A29	1	TP118	TPAD14-GP
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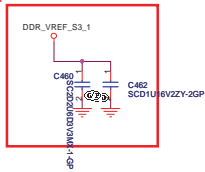


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Date	Thursday, January 06, 2009
Sheet	15 of 60
Rev	SB

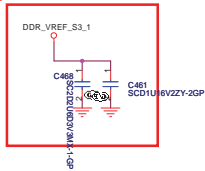
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Layout Note : Near Pin 126



Layout Note : Near Pin 1



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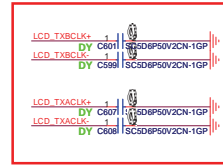
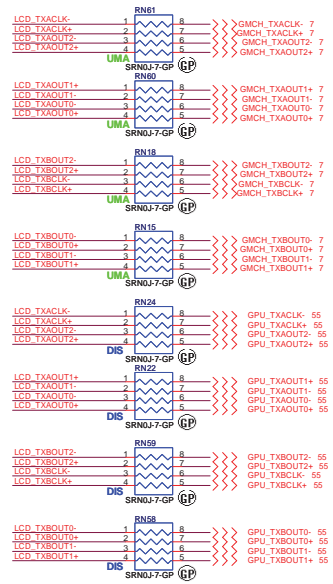
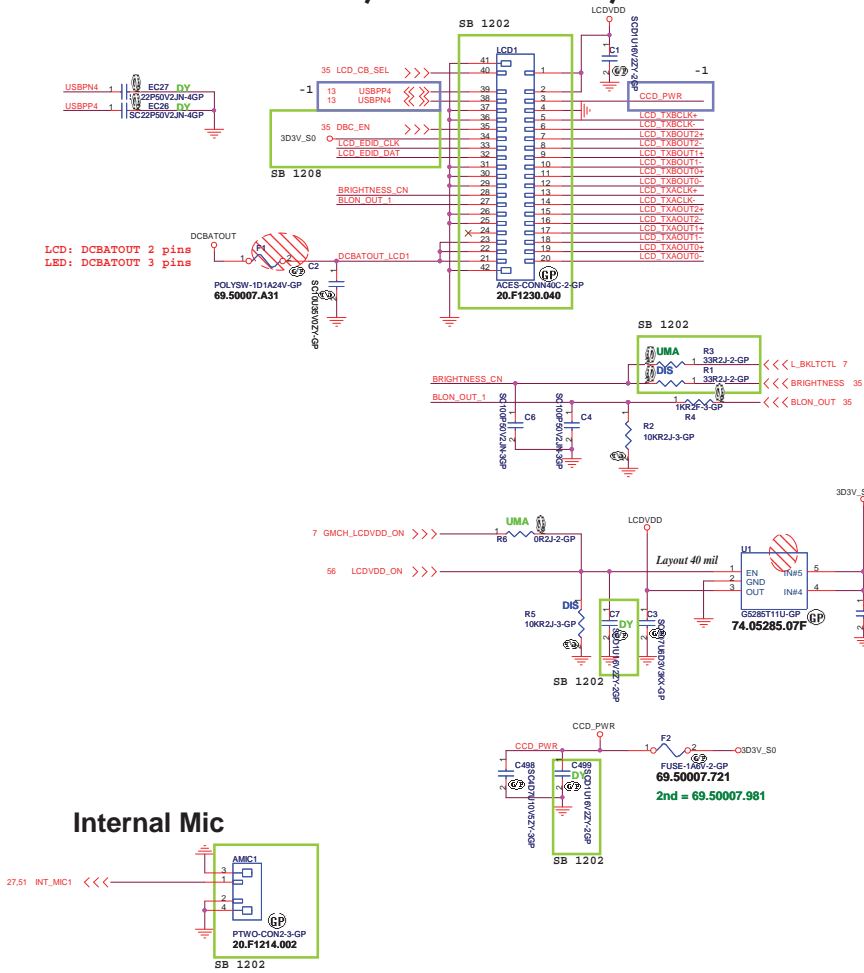
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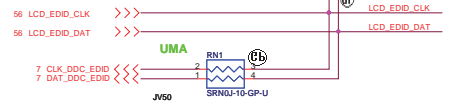
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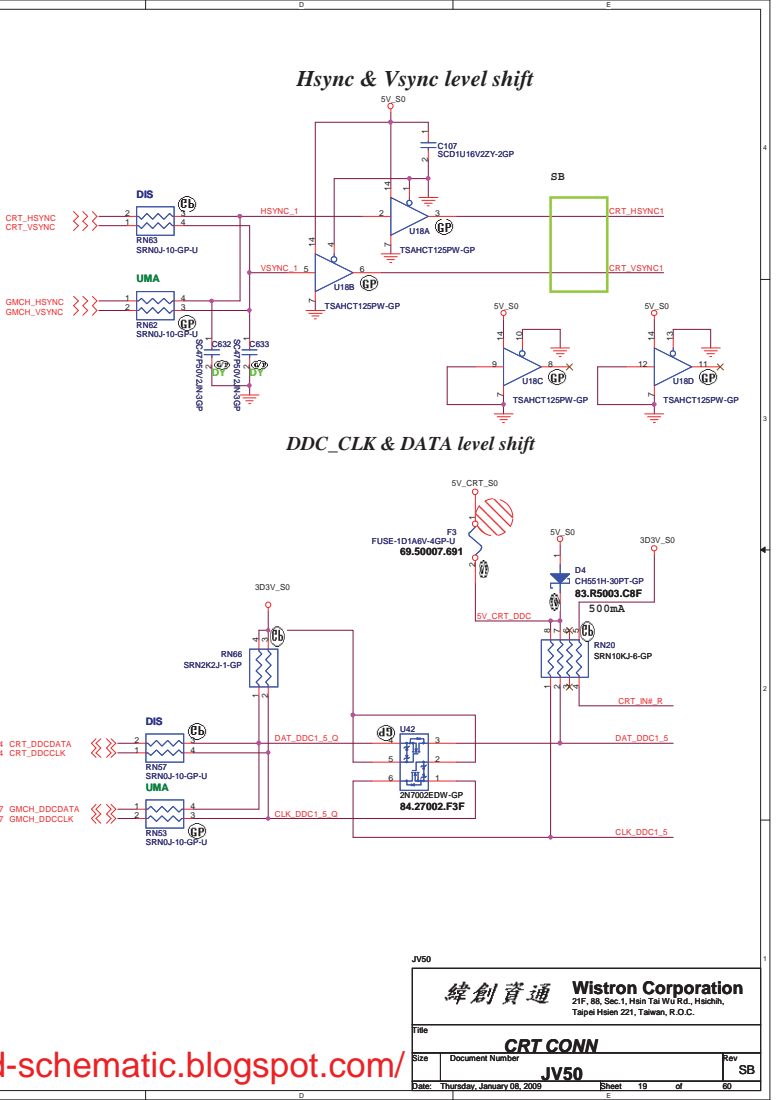
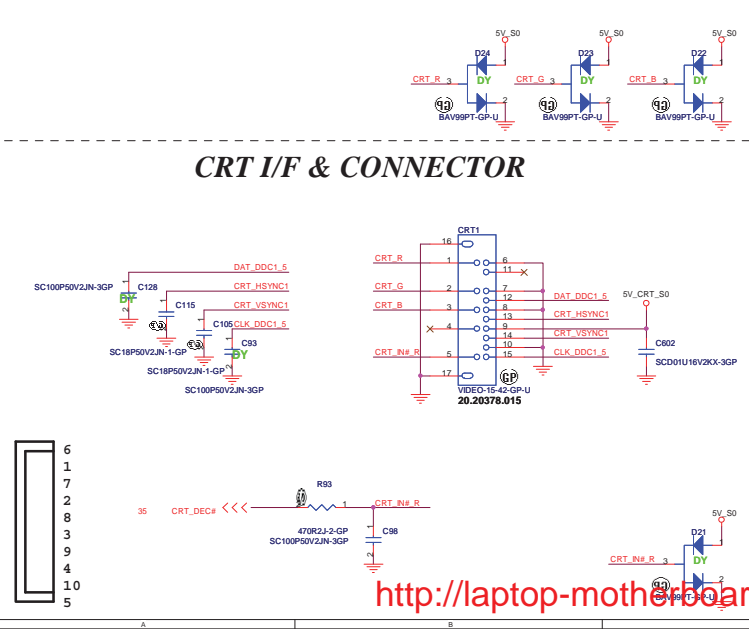
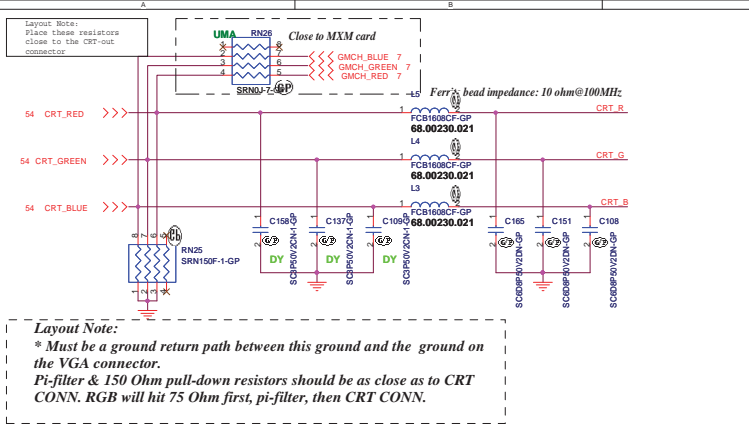
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modify by RF



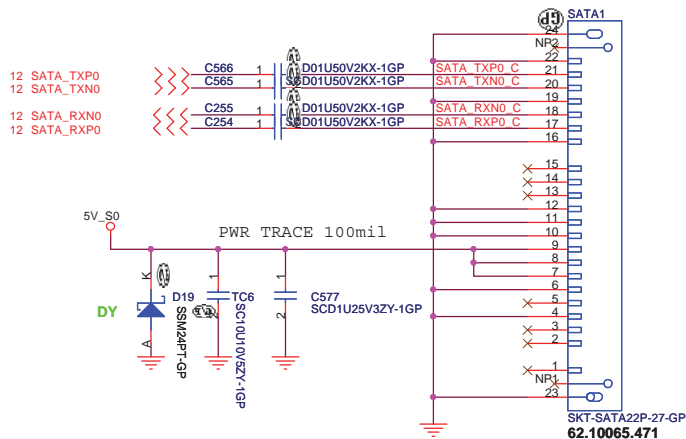
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Date: Thursday, January 08, 2009		Sheet 18 of	60



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# SATA Connector

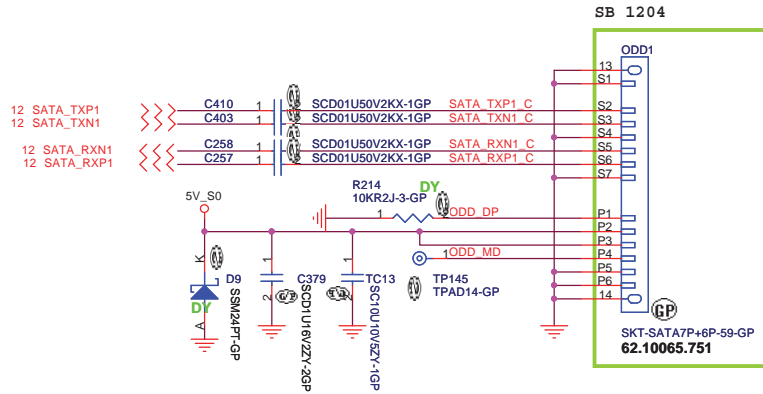


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JV50	
Date: Thursday, January 08, 2009	Sheet 21 of 60
Rev SB	

# ODD Connector



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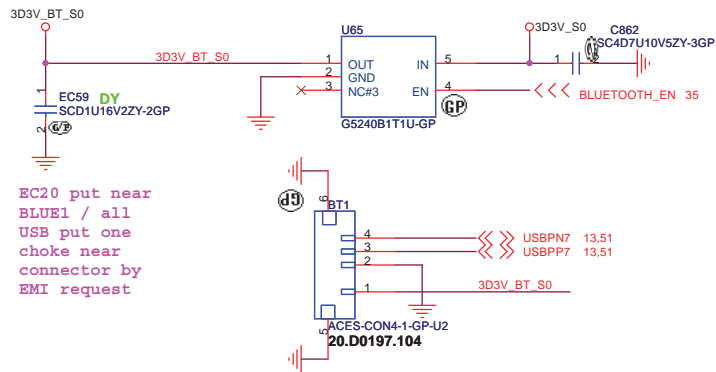
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Sheet 22 of 60

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# BLUETOOTH MODULE



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Thursday, January 08, 2009

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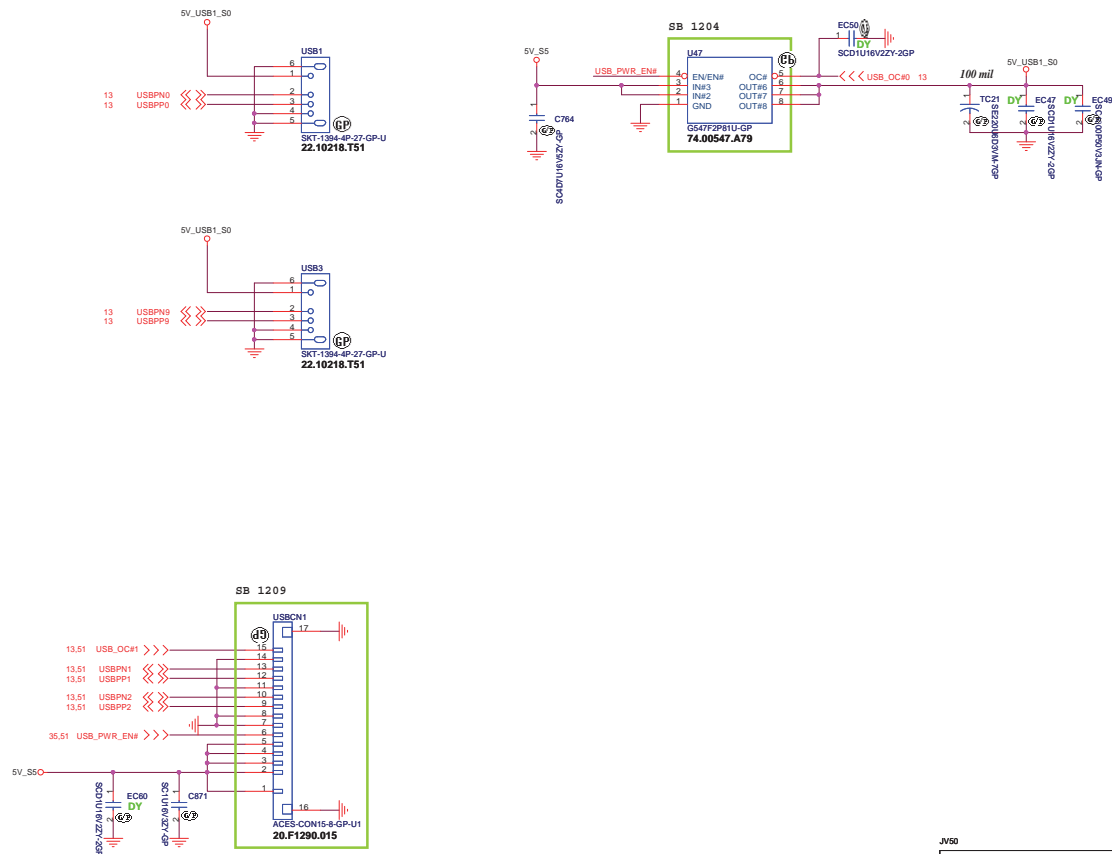
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**JV50**

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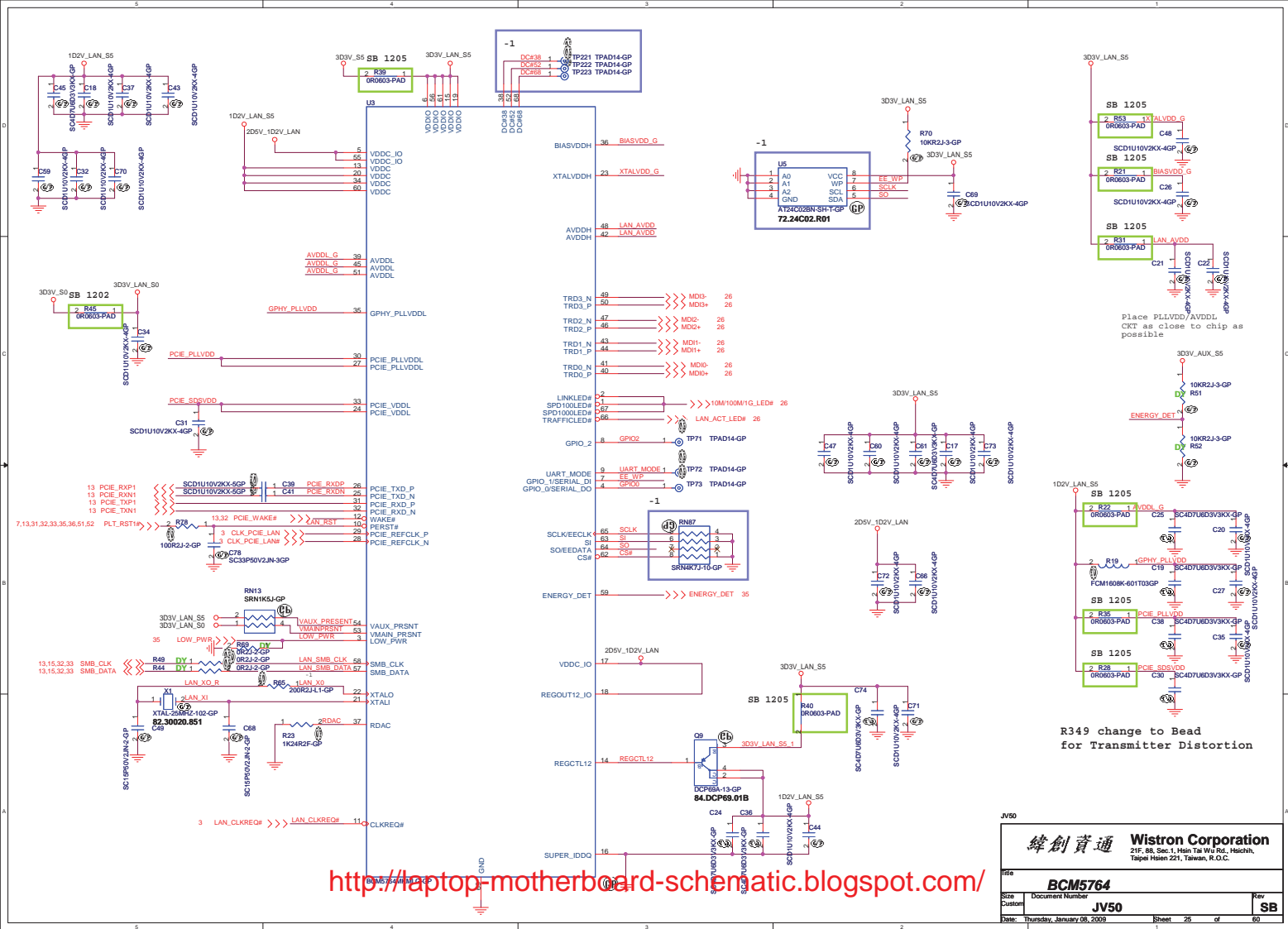
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Size	Document Number	Rev	SB
Date: Thursday, January 08, 2009	Sheet 24 of 60	JV50	





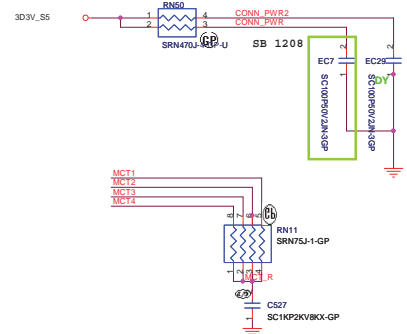
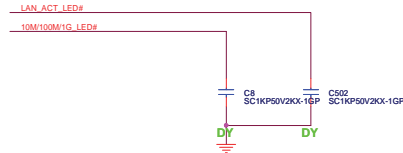
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Rev	Rev
SB	60
Document Number	BCM5764
Size	Custom
Date	Thursday, January 06, 2009
Sheet	25 of 60

### LAN Connector

- ### GIGA Lan Transformer

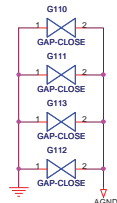
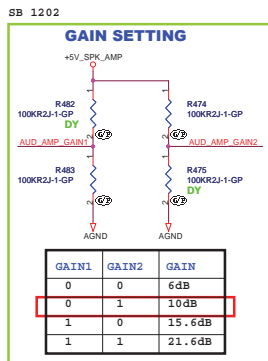
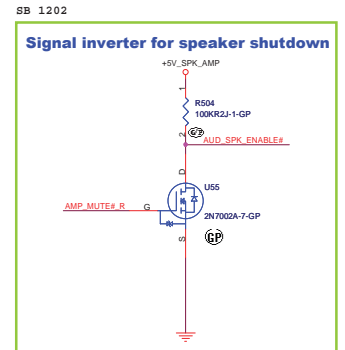


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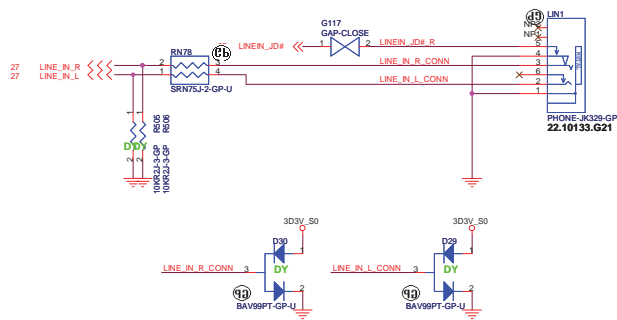
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Date:	Thursday, January 08, 2009			Sheet		26	of 20

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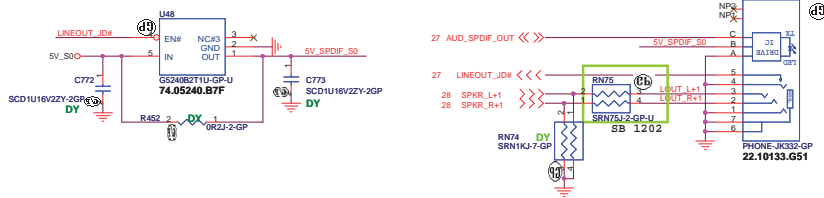




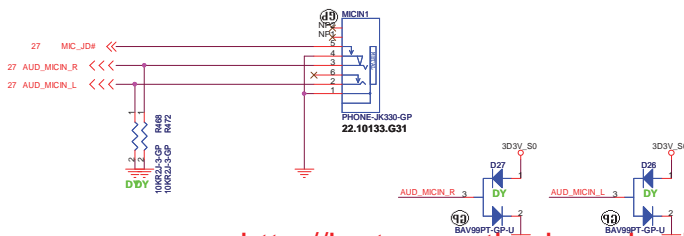
## LINE IN



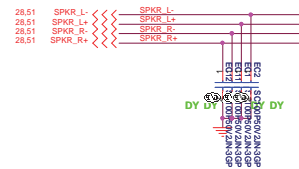
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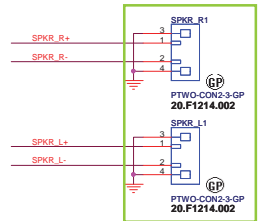
## MIC IN



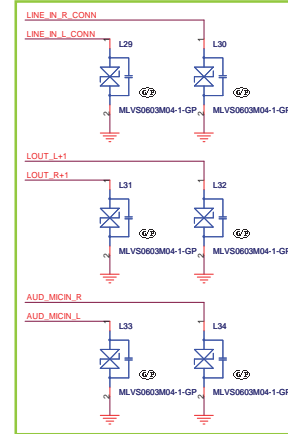
## Internal Speaker



SB 1202



SB 1202

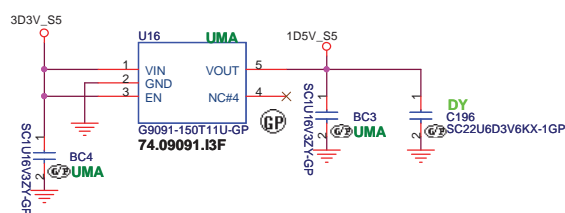



JV50

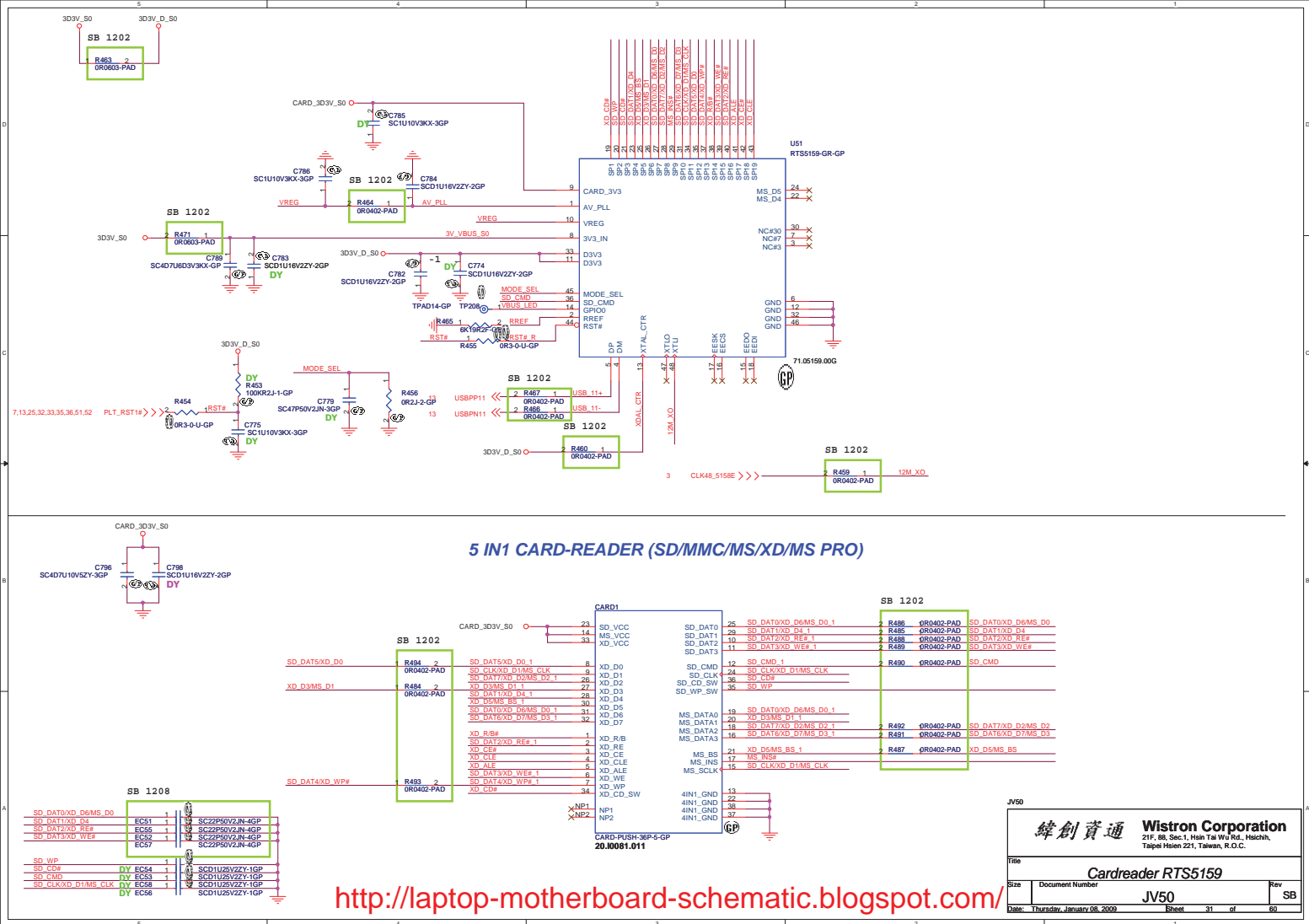
緯創資通 Wistron Corporation  
21F, 8th Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 321, Taiwan, R.O.C.

Title			
AUDIO jack			
Size	Document Number	Rev	SB
JV50			
Date: Thursday, January 06, 2009	Sheet 25	of 60	

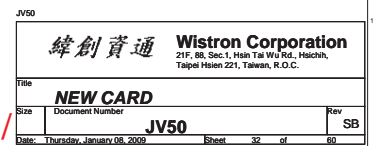
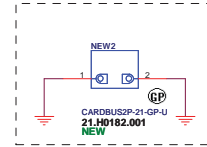
<http://laptop-motherboard-schematic.blogspot.com/>

[illegible]

 <b>緯創資通</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
<b>MDC</b> Size Document Number Rev	
<b>JY50</b> Date: 08/08/2009 Sheet 30 of 60 SB	



<http://laptop-motherboard-schematic.blogspot.com/>













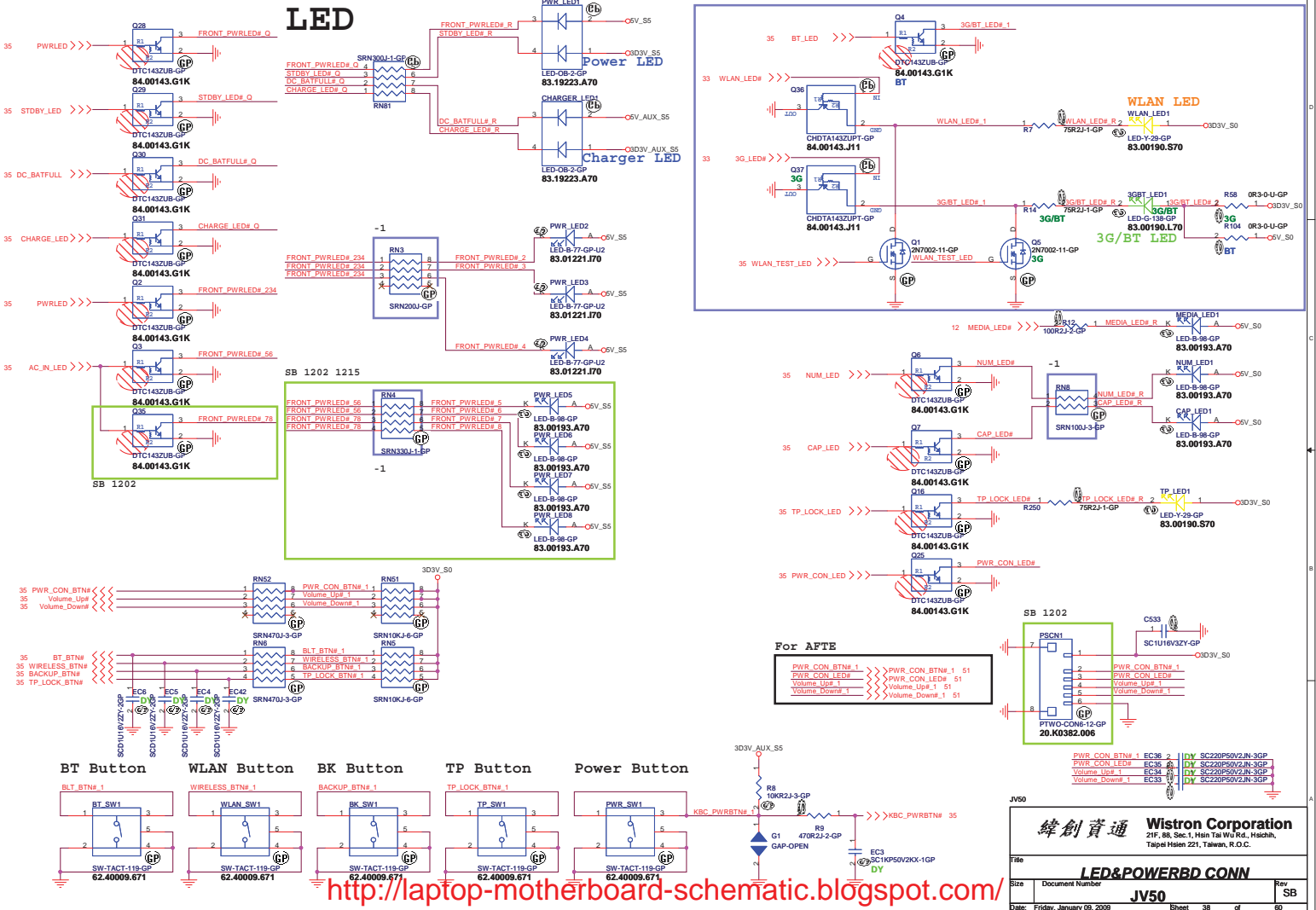
For AFTE



Title			
Touch PAD and FP			
Size	Document Number		Rev
	JV50		SB
Date: Thursday, January 08, 2009	Sheet	37 of	60

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# LED



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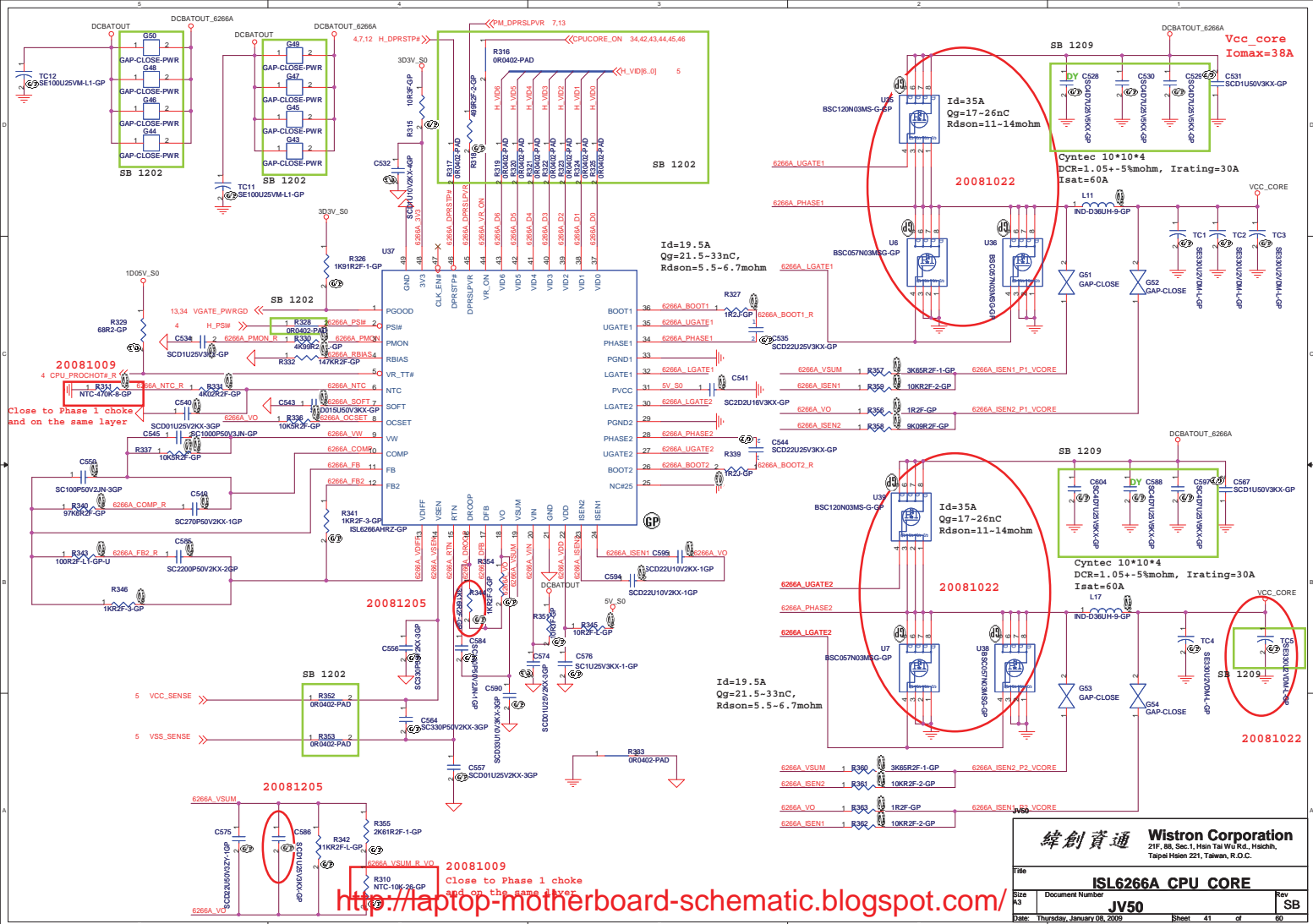
**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

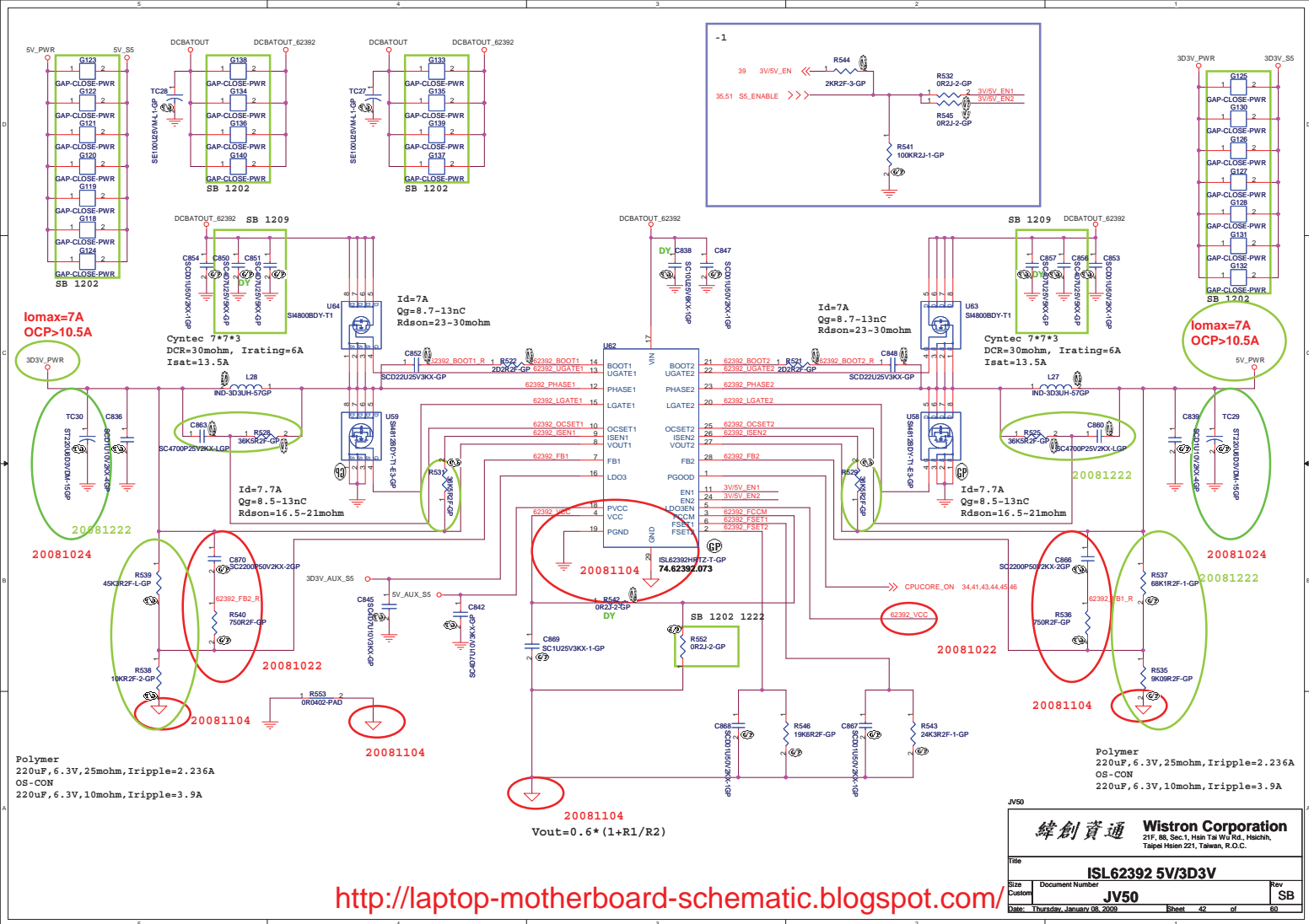
File: **LED&POWERBD\_CONN**  
 Size: Document Number **JV50** Rev: SB  
 Date: Friday, January 09, 2009 Sheet: 38 of 60

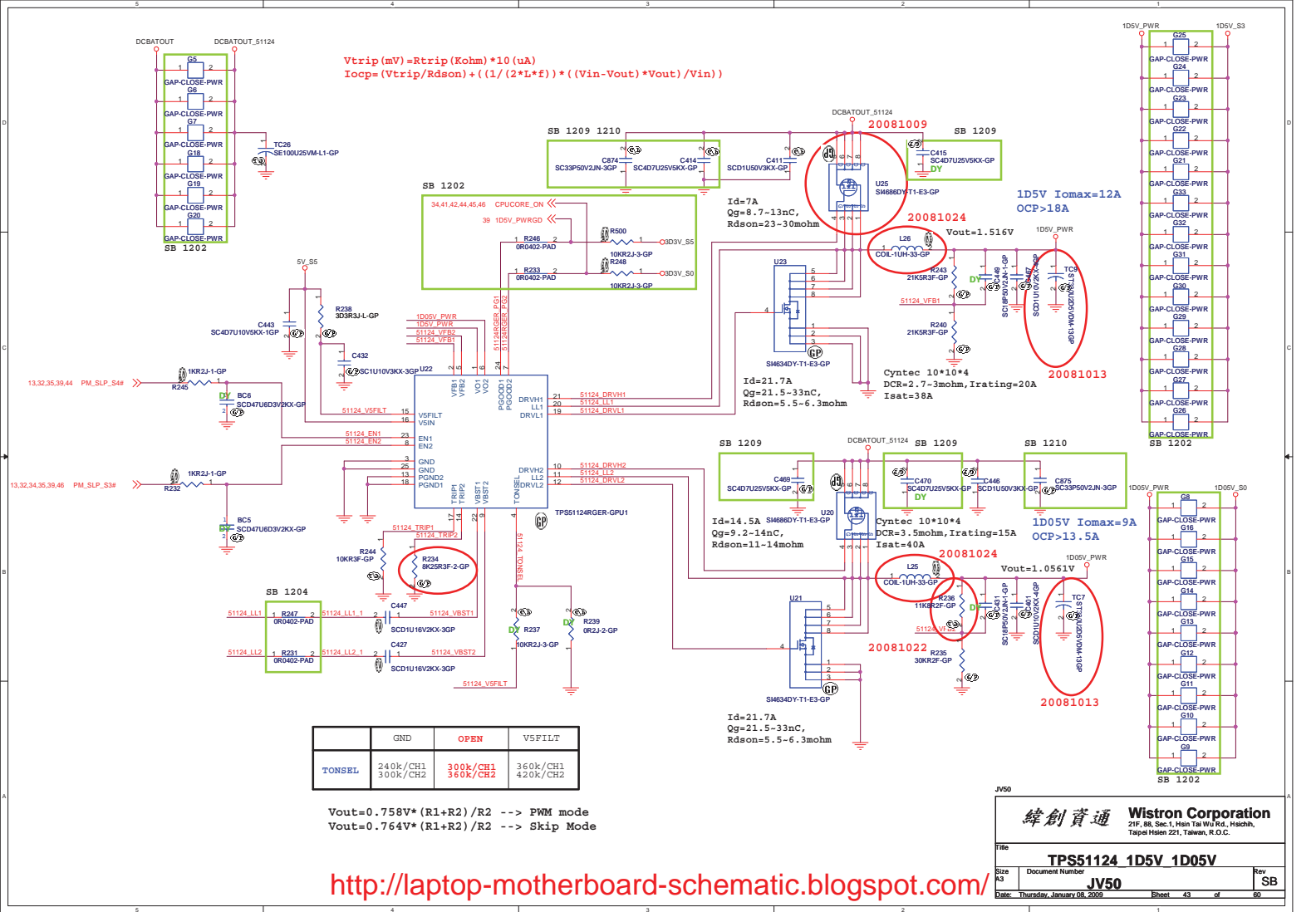








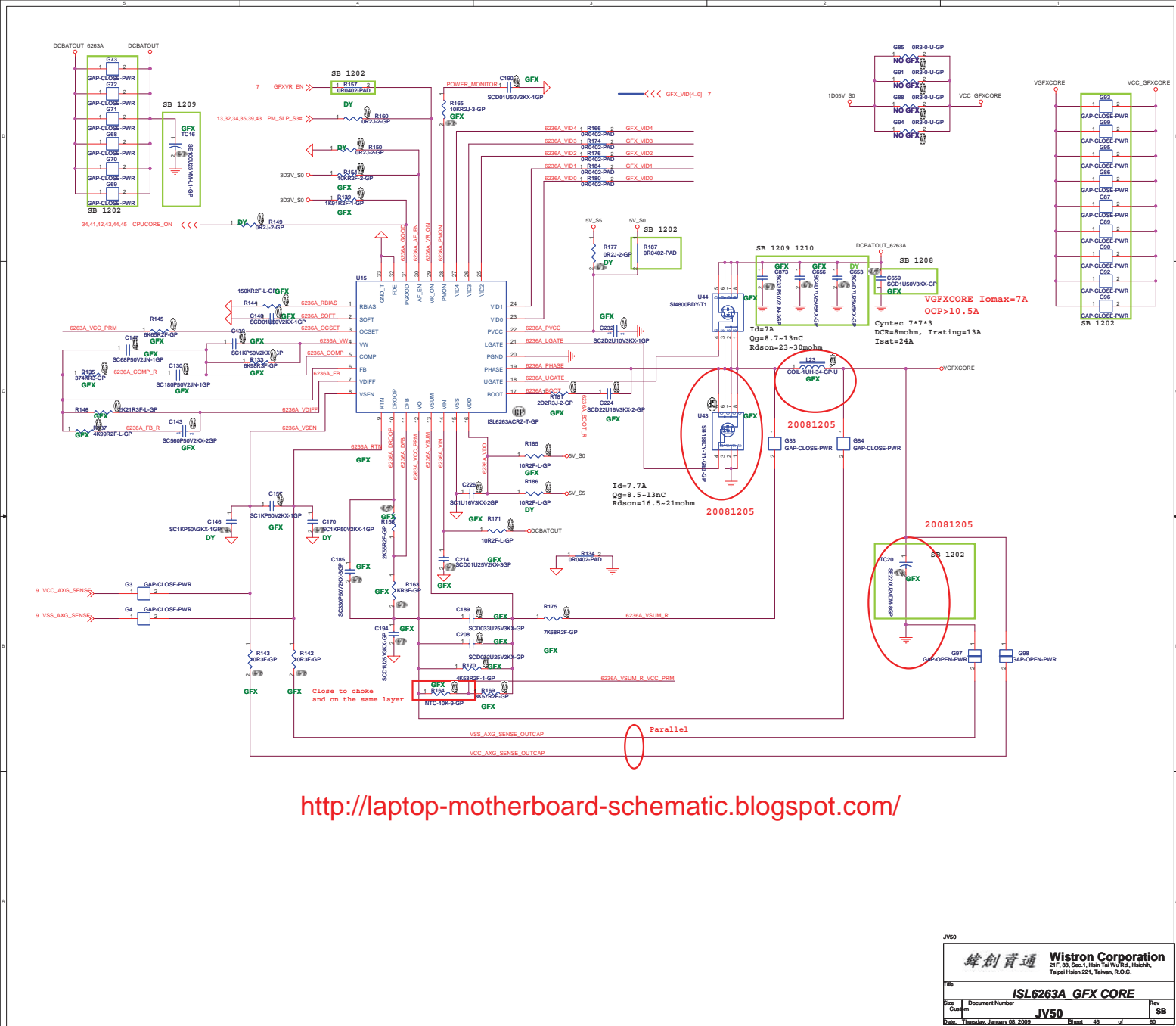




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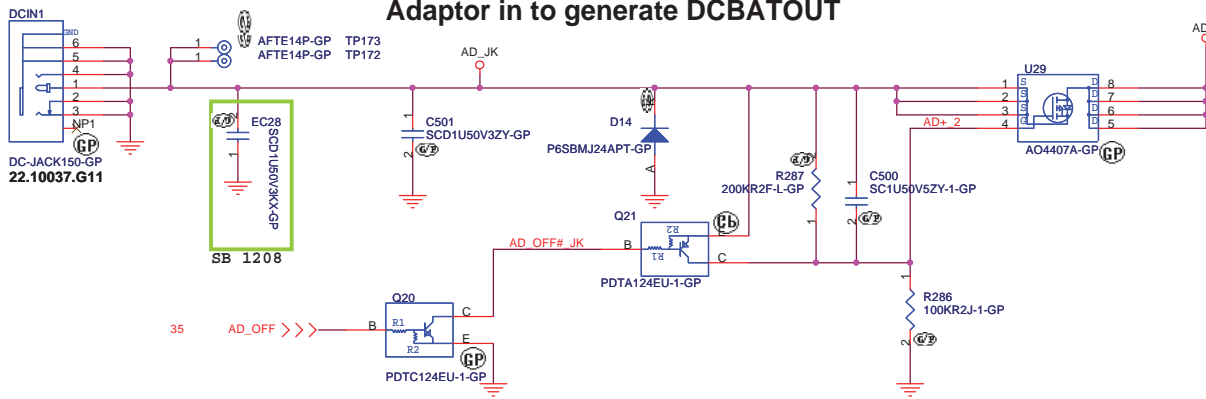


JV50		 <b>Wistron Corporation</b> 21F, 88, Sec. 1, Main Tai Wu rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>TPS51117 1D8V</b> <b>JV50</b>		Rev	
Size A3	Document Number	SB	
Date: Thursday, January 08, 2009	Sheet 45	of 60	

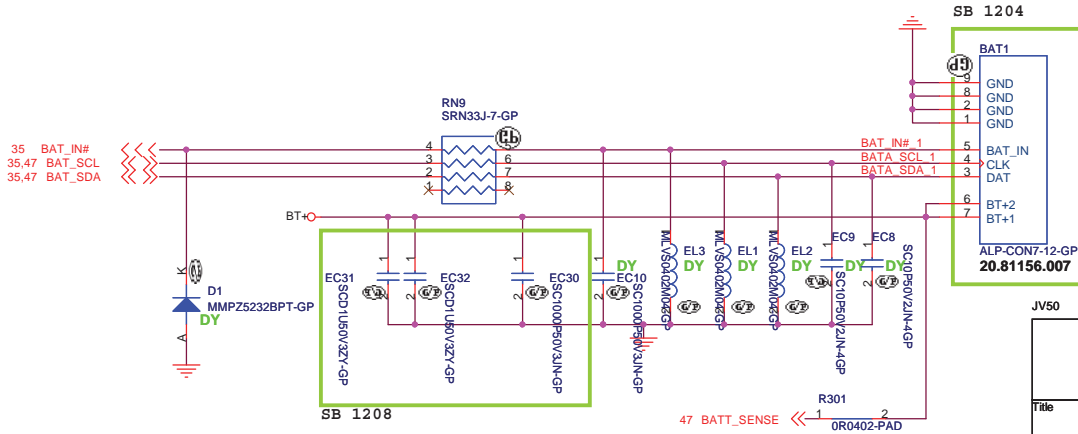




## Adaptor in to generate DCBATOUT



## BATTERY CONNECTOR



For AFTE

51 BATA\_SDA\_1 >>> BATA\_SDA\_1  
51 BATA\_SCL\_1 >>> BATA\_SCL\_1  
51 BAT\_IN#\_1 >>> BAT\_IN#\_1

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緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**AD/BATT CONN**

Size

Document Number

Rev

Date

Thursday, January 08, 2009

Sheet

48

of

60

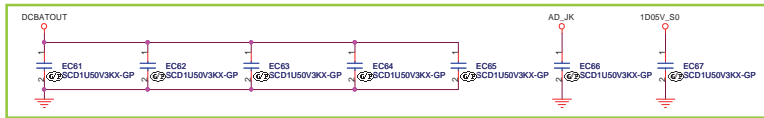
**JV50**

SB

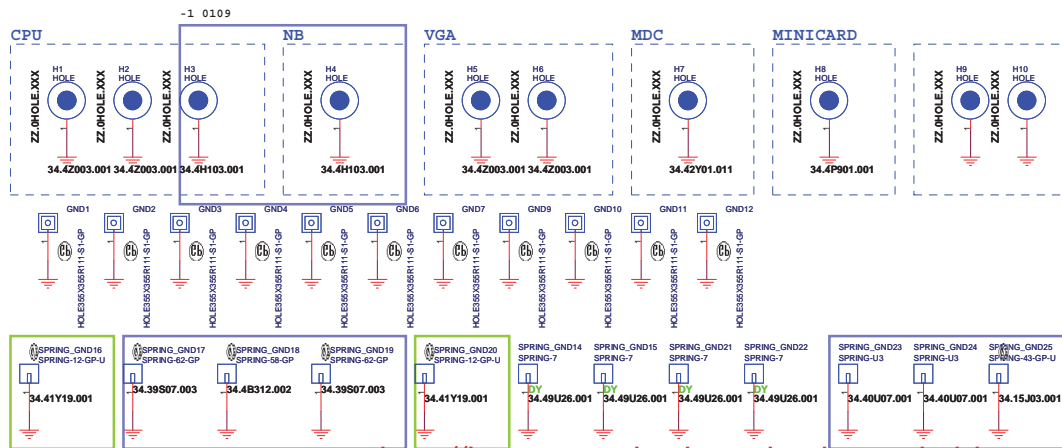
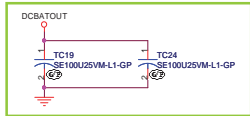




SB 1208



SB 1209

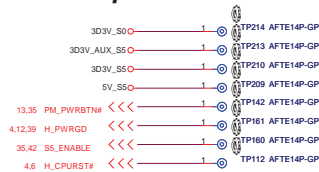


JV50

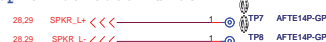
緯創資通 Wistron Corporation	
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsinchu, Taipei 305, Taiwan, R.O.C.	
Title EMI/Spring/Boss	
JV50	
Date: Friday, January 08, 2009	Rev SB
Sheet 50 of 60	

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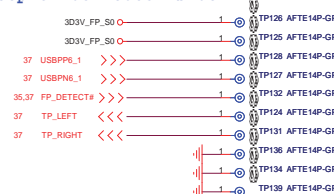
## Check test point



## SPKR\_L1 Conn. Test Point keep on connector side



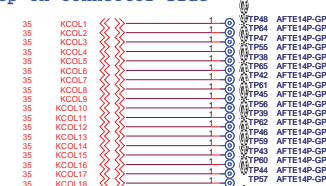
## FPCN1 Conn. Test Point keep on connector side



## FAN1 Conn. Test Point keep on connector side



## KB1 Conn. Test Point keep on connector side



## PSCN1 Conn. Test Point keep on connector side



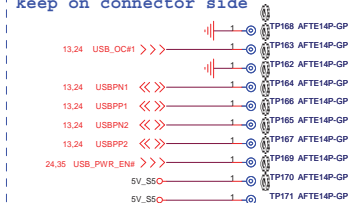
## AMIC1 Conn. Test Point keep on connector side



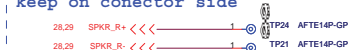
## BT1 Conn. Test Point keep on connector side



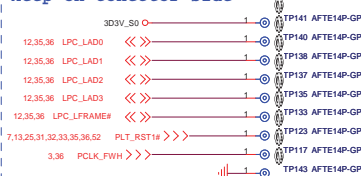
## USBCN1 Conn. Test Point keep on connector side



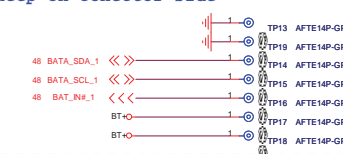
## SPKR\_R1 Conn. Test Point keep on connector side



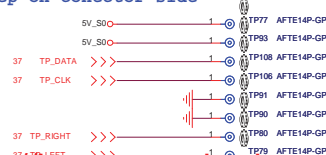
## DB1 Conn. Test Point keep on connector side



## TPCN1 Conn. Test Point keep on connector side



## TPCN1 Conn. Test Point keep on connector side

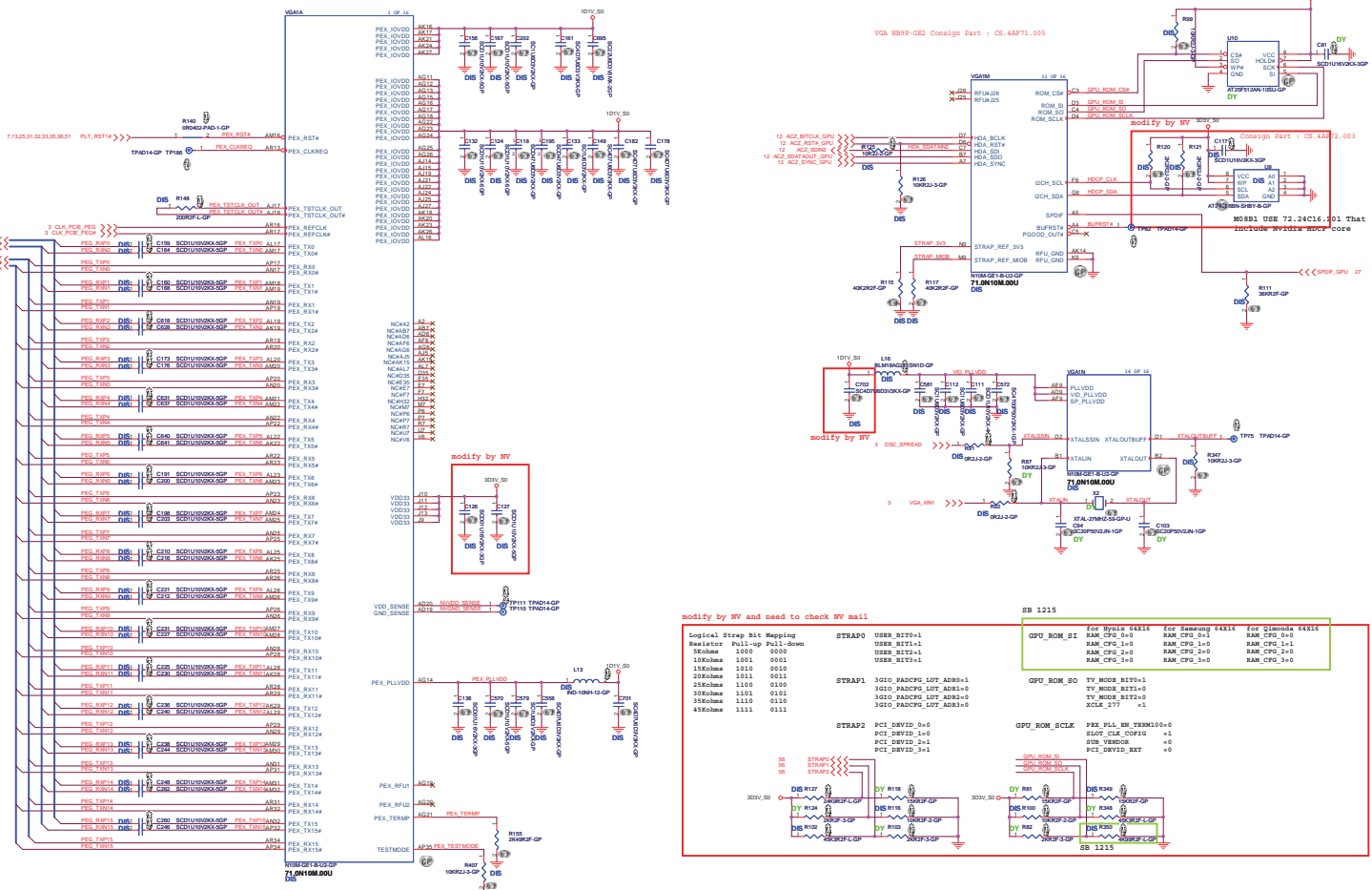


JV50

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

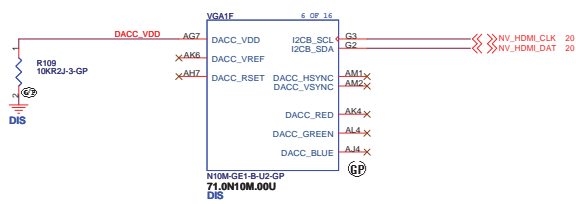
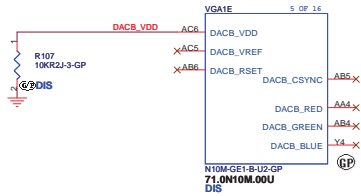
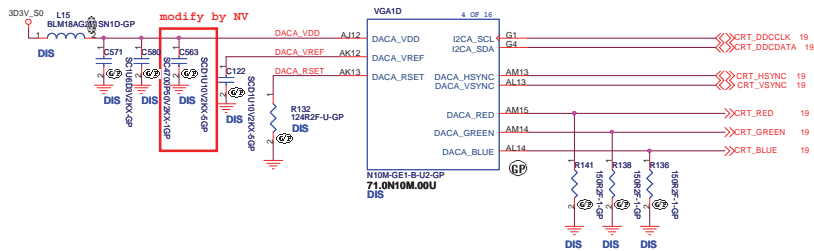
Title		AFTE TP	
Size	Document Number	JV50	
Date	Thursday, January 06, 2009	Sheet	51 of 60
Rev		SB	

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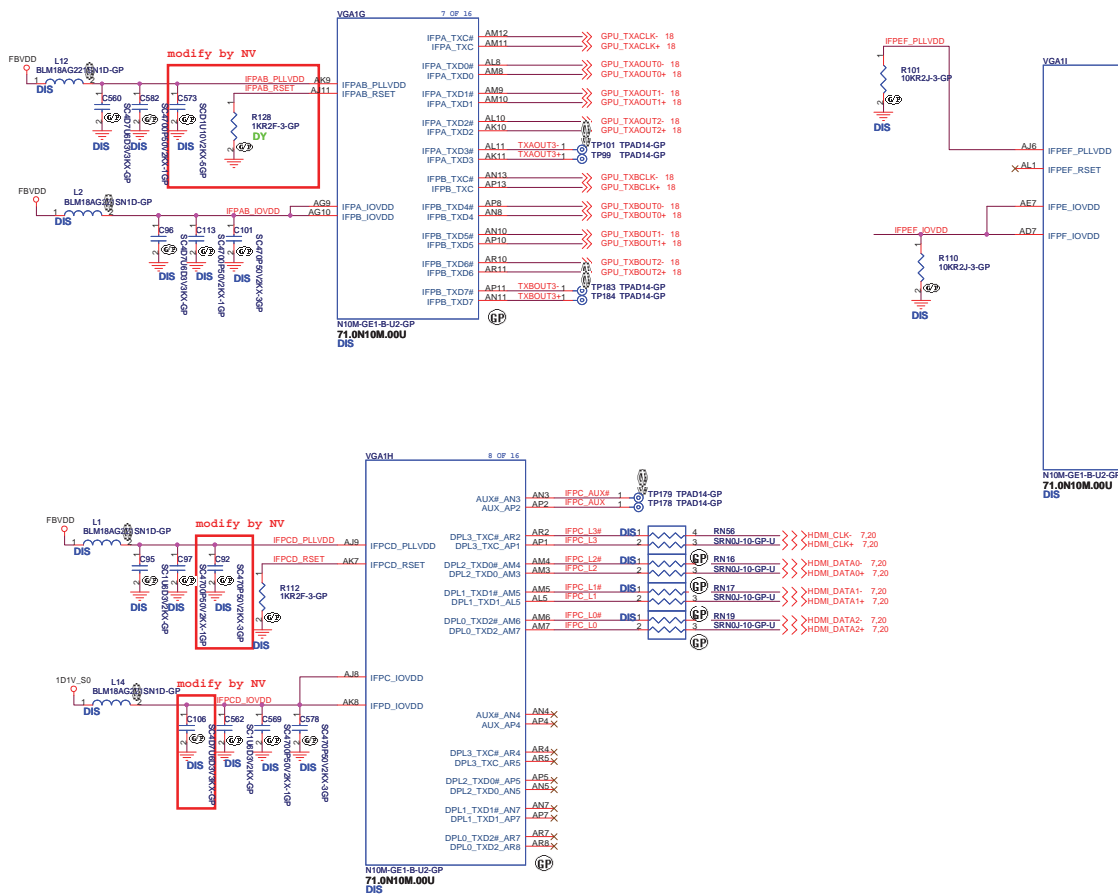


<http://laptop-motherboard-schematic.blogspot.com/>

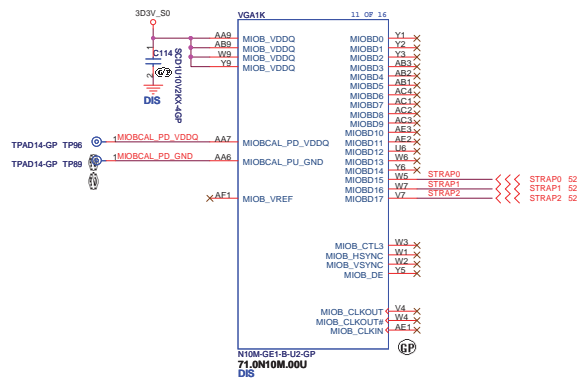
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,  
Taipei Hsien 321, Taiwan, R.O.C.

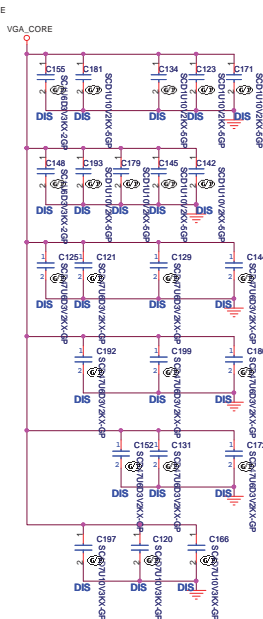
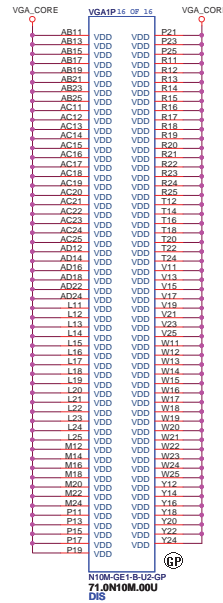
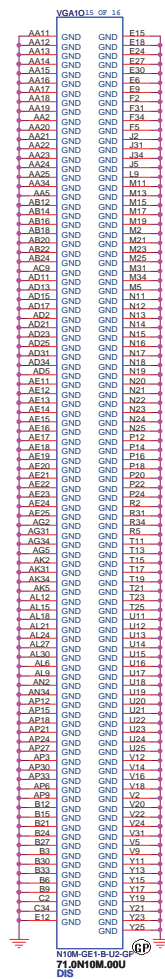
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Size	A3	Document Number	JV50
Date:	Thursday, January 08, 2009	Sheet	54 of 90
		Rev	SB



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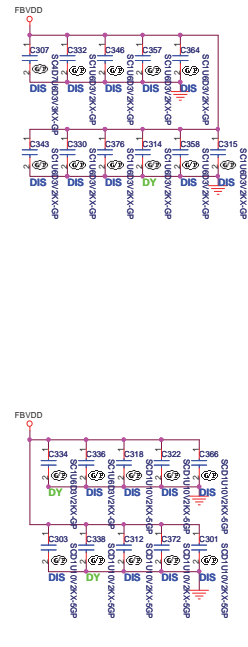
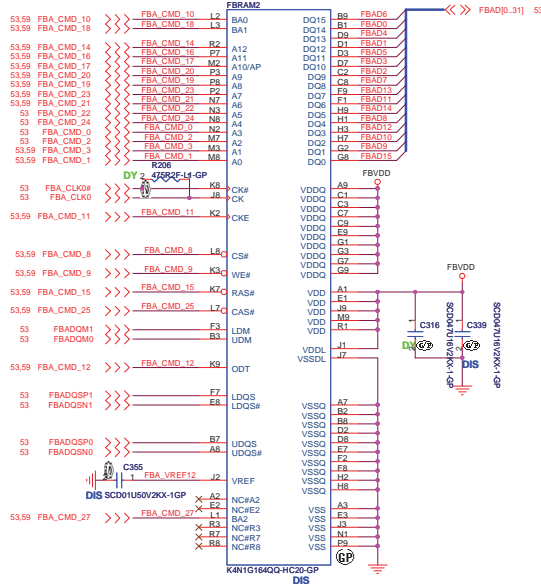
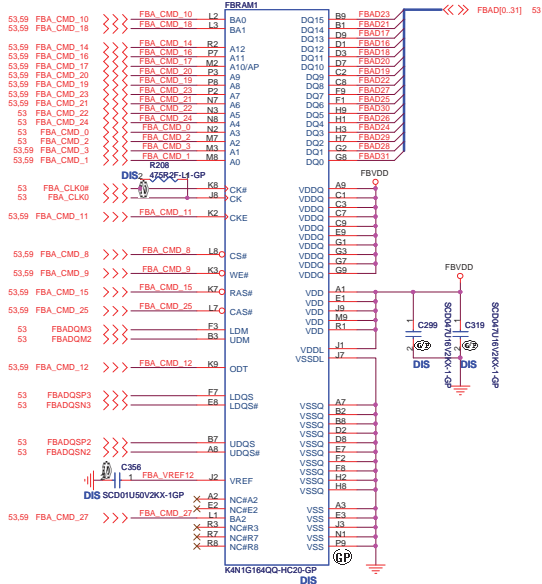




JV50

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
N10M(6/6) POWER			
Size	Document Number		Rev
A3	JV50		SB
Date: Thursday, January 08, 2009		Sheet 57 of	90

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modify by NV

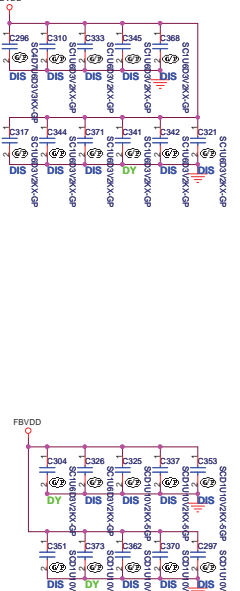
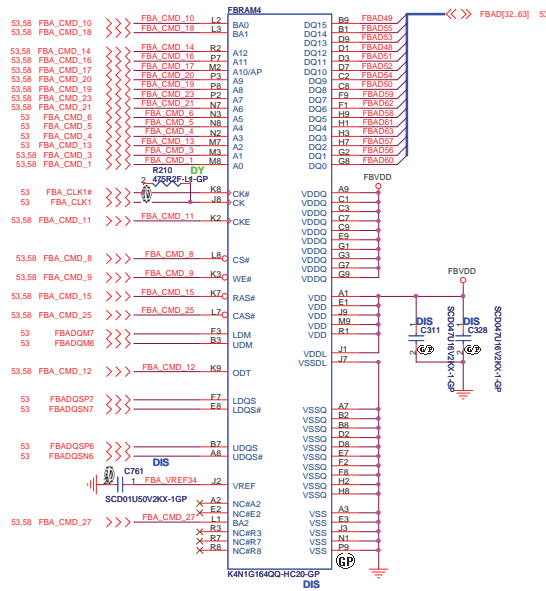
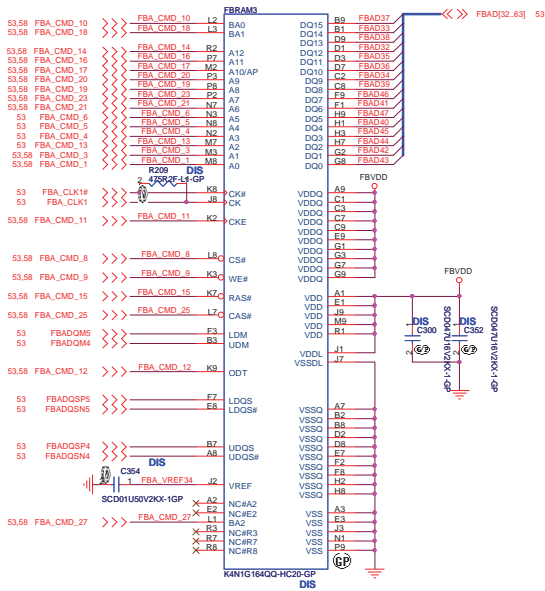


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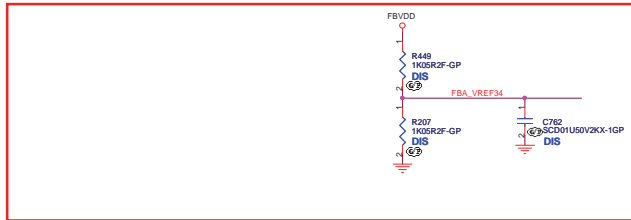
JV50

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,  
Taipei Hsien 301, Taiwan, R.O.C.

File	Document Number	Rev
Size A3	JV50	SB
Date: Thursday, January 28, 2009	Sheet 58 of 90	



modify by NV



SB  
All Component for NB9P-GE2

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JV50

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File	VRAM(22)	Rev	SB
Size	Document Number		
A3	JV50		
Date	Thursday, January 28, 2009	Sheet	59 of 60

SB SA SC -1  
12/02 change C452 C453 from 27P to 33P by vendor's request  
Page3: change C452 C453 from 27P to 33P by vendor's request  
Page33: add C872 33P for SIV  
Page29: change SPKR\_R1 SPKR\_L1 from 20.F1396.002 to 20.F1214.002 by CE's request  
Page18: change LCD1 from 20.F1296.040 to 20.F1230.040 by CE's request  
Page24: change USBNC1 from 20.F1290.015 to 20.F1035.015 by CE's request  
Page38: change PSCN1 from 20.K0356.006 to 20.K0382.006 by CE's request  
Page18: change AMIC1 from 20.F1396.002 to 20.F1214.002 by CE's request  
Page3: add R554 and change U24 pin16 from 3D3V\_S0 to 3D3V\_VDD48\_S0  
Page3: change C457 C450 C416 C430 C418 from mount to DY and change C456 from DY to mount  
Page7: change R192 R195 from 0ohm resistor to 0ohm pad and add R555 RN82 RN83 RN84 RN85 for reflection  
Page9: change C275 from UMA to DY and change C349 from mount to DY  
Page10: change C243 C758 from mount to DY and change R167 R398 from DIS to DY  
Page13: change R216 from 0ohm resistor to 0ohm pad  
Page14: change C413 C252 C703 C392 C707 C734 from mount to DY  
Page17: change C426 C429 from mount to DY  
Page18: change C7 C499 from mount to DY and change R1 from mount to DIS and change R3 from DY to UMA  
Page20: add RN86 for DIS HDMI SMBus  
Page25: change R45 from 0ohm resistor to 0ohm pad  
Page27: change R523 from 0ohm resistor to 0ohm pad  
Page7: add R556 pull-low DY for A1 NB  
Page28: change AGND & GND and change R509 from 0ohm resistor to 0ohm pad  
Page28: change C795 C790 C792 from mount to DY and change R480 R479 from 0ohm to 6K2 and 8K2  
Page28: combine C801 C802 two 1u to C801 4.7u  
Page28: delete C815 C814 C809 R500 R503 R513 R507 R502 R508 D31 U56 and change U55 to 84.2N702.E31  
Page28: change R474 from DY to mount and change R475 from mount to DY for 10dB  
Page29: add L29 L30 L31 L32 L33 L34 for ESD  
Page31: change R463 R464 R471 R467 R466 R460 R459 R494 R484 R493 R486 R485 R488 R489 R490 R492 R491 R487 from 0ohm resistor to 0ohm pad  
Page32: change C487 C477 from mount to DY and change R269 from 0ohm resistor to 0ohm pad  
Page12: change C385 C386 from 10p to 7p by vendor's request  
Page35: change C136 C169 from 15p to 7p by vendor's request  
Page33: change R15 R29 R34 from 0ohm resistor to 0ohm pad and change C542 from mount to DY  
Page34: change C42 from mount to DY  
Page35: change C615 C626 C638 R395 from mount to DY and change R394 from DY to mount for PCB version  
Page36: change DB1 from mount to DY  
Page38: add Q35 PWR\_LED7 PWR\_LED8 and change RN4 from 4P2R to 8P4R and change PWR\_LED5 PWR\_LED6 from 83.01221.I70 to 83.00193.A70 for LED type  
Page39: change U66 pin1 from CPUCORE\_ON to 1D5V\_PWRGD and change D13 pin1 from S5\_ENABLE to 3V/SV\_EN  
Page40: update power sequence logic  
Page41: change G43-G50 from open gap to close gap and change R328 R352 R353 R317 R316 R319-R325 from 0ohm resistor to 0ohm pad  
Page42: change R532 R545 R552 from 0ohm resistor to 0ohm pad and change G118-G128 G130-G140 from open gap to close gap  
Page43: change R246 R233 from 0ohm resistor to 0ohm pad and change G5-G16 G18-G33 from open gap to close gap  
Page43: change R246 pin2 from CPUCORE\_ON to 1D5V\_PWRGD and add R500 pull-high 10K 3D3V\_S5  
Page45: change G100-G109 from open gap to close gap  
Page46: change R157 R187 from 0ohm resistor to 0ohm pad and change G68-G73 G86 G87 G89 G90 G92 G93 G95 G96 G99 from open gap to close gap  
Page46: delete TC19 and change TC20 from DY to GFX  
Page49: change G55-G67 G74-G77 from open gap to close gap  
Page29: change RN75 from 47ohm to 75ohm  
Page28: change C804 C807 from 4.7u to 1u 25V X5R  
Page45: delete TC24  
Page19: delete R104 R129

12/04  
Page24: change U47 from 74.00545.A79 to 74.00547.A79  
Page20: swap HDMI signals for routing  
Page28: change U53 pin22 from AUD\_HP1\_EN to AMP\_MUTEN\_R  
Page48: change BAT1 from 20.81094.007 to 20.81156.007  
Page22: change ODD1 from 62.10065.541 to 62.10065.751  
Page22: change R231 R247 from 0ohm resistor to 0ohm pad  
  
12/05  
Page28: change R39 R53 R21 R31 R22 R35 R28 from 0ohm resistor to 0ohm pad  
Page46: change L23 from 68.R8210.10V to 68.1R01A.20B and change U43 from 84.04812.A37 to 84.04168.037 by power team's request  
Page41: change R344 from 2K87 to 3K16 and change C586 from 0.47u to 0.1u by power team's request  
Page41: change U35 U39 from 84.01426.037 to 84.12003.A37 and change U6 U7 U36 U38 from 84.01712.037 to 84.57N03.A37 by power team's request  
Page45: change R457 from 11K to 3K48 and change TC23 from 390u to 220u by power team's request  
  
12/08  
Page26: change EC7 from DY to mount EMI's request  
Page48: change EC28 EC30 EC31 EC32 from DY to mount EMI's request  
Page31: change EC51 EC52 EC55 EC57 from 0.1u DY to 22p mount EMI's request  
Page5: change C79 C80 from DY to mount EMI's request  
Page46: change C659 from DY to GFX EMI's request  
Page50: change SPRING\_GND16-SPRING\_GND20 from DY to mount EMI's request  
Page50: add EC61-EC67 0.1u by EMI's request  
Page20: change R313 R314 from 10K 100K to 18K 47K by NV's request  
Page35: change U14 pin83 RN65 pin2 from SHBM to DBC\_EN by annie's request  
Page18: change LCD1 pin35 from NC to DBC\_EN by annie's request  
Page20: add ER1-ER8 0ohm pad by EMI's request  
Page10: change C636 from 1000p DY to 27p mount by RF's request  
  
12/09  
Page49: change R406 from 6K2 to 4K75 by power team's request  
Page46: change TC16 from mount to GFX  
Page50: add TC19 TC24 100u  
Page41: change C528 C529 S30 C588 C597 C604 from 10u to 4.7u and change C528 C588 from mount to DY  
Page46: change C656 C653 from 10u to 4.7u and change C653 from GFX to DY  
Page42: change C856 C857 C851 C850 from 10u to 4.7u and change C857 C850 from mount to DY  
Page41: change TC5 from DY to mount  
Page5: change C553 C538 C552 C539 C547 C536 C548 C537 from DY to mount  
Page17: change C426 C428 C429 from 10u to 4.7u and change C429 from DY to mount  
Page16: change C440-C442 C463-C465 from 10u to 4.7u and change C440 from DY to mount and change C464 from DY to mount  
Page20: change HDMI from 62.10078.161 to 62.10078.171 by CE's request  
Page24: change USBNC1 from 20.F1035.015 to 20.F1290.015 by CE's request  
  
12/10  
Page46: add C873 33p GFX by RF's request  
Page43: add C874 C875 33p by RF's request  
Page20: swap U8 pin13 14 47 48  
Page33: change R16 from DY to mount  
Page47: change R292 from 0ohm resistor to 0ohm pad  
  
12/11  
Page33: change U55 pin1 from SV\_S5\_MIN1 to SV\_S5\_MIN2  
12/15  
Page52: change VRAM strap R350

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A00	
Wistron Corporation 23F, 28, Sec. 1, Hsin-Tsai Rd., Hsinchu, Taiwan 305, R.O.C.	
HISTORY	
No.	Document Number
JV50	
Date	Thursday, January 24, 2008
Print	SB

SB SS SC -1  
12/22  
Page49: change R427 from 30K 47K and R428 from 47K to 30K  
  
SC  
12/22  
Page42: modify by power team's request  
Page35: change R372 R395 from DY to mount and change R373 R394 from mount to DY  
  
-1  
01/06  
Page17: change C400 from mount to DY and change C399 from DY to mount  
Page30: change R267 from 39R to 0ohm pad  
Page38: delete RN7 and add Q36 Q37  
Page25: change U3 pin 38 52 from LAN\_AVDD to TP and change U3 pin 68 from NC to TP  
Page25: delete R58 and add RN87 and change U5 to 72.24C02.R01  
Page3: change R255 from 22R to 33R and change RN42 from 0ohm to 33R  
Page33: change R268 R275 R259 from 0ohm resistor to 0ohm pad  
Page35: change R394 from DY to mount and change R395 from mount to DY  
Page28: change R526 from 0ohm resistor to 0ohm pad  
Page35: change R401 from 0ohm resistor to 0ohm pad  
Page35: delete Q12 and add R502 R503  
Page35: change RN23 pin 5 6 from 3D3V\_AUX\_S5 to 3D3V\_S0  
Page44: change U46 to APL5930 by power team's request  
Page38: add 3G and BT option  
Page28: change R479 from 8K2 to 10K and change R480 from 6K2 to 4K99 for audio speaker gain  
Page28: merge C0D1 to LCD1  
  
01/07  
Page44: change R437 from 0ohm pad to 0ohm resistor  
Page9: change TC18 from UMA to DY and change C276 from DY to mount  
Page35: delete RN21 and add R507 10K DY  
Page38: change RN4 to 330R and change RN8 to 100R and delete R10 and change RN3 to 8P4R 200R  
Page47: change C515 to 78.15322.2FL by power team's request  
Page3: mount 33p on EC23 EC24 EC25 EC39 EC48 for RF's request  
Page3: add EC68 EC69 33p DY by RF's request  
Page20: add R129 4K7 for different vendor  
  
01/08  
Page42: change R541 from 200K to 100K and change R544 location  
Page42: change R532 R545 from 0ohm pad to 0ohm resistor  
  
01/09  
Page38: change name from 3G/ST LED1 to 3GBT LED1  
Page50: add SPRING\_GND23 34.40U07.001, SPRING\_GND24 34.40U07.001, SPRING\_GND25 34.15J03.001  
Page50: SPRING\_GND17, SPRING\_GND19 change from 34.41Y19.001 to 34.39S07.003  
Page50: SPRING\_GND18 change from 34.41Y19.001 to 34.4B312.002

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JV50		Wistron Corporation	
緯創資通		23F, 8F, Sec. 1, Hsin-Tai Rd., Hsinchu, Taipei Hsien 321, Taiwan, R.O.C.	
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